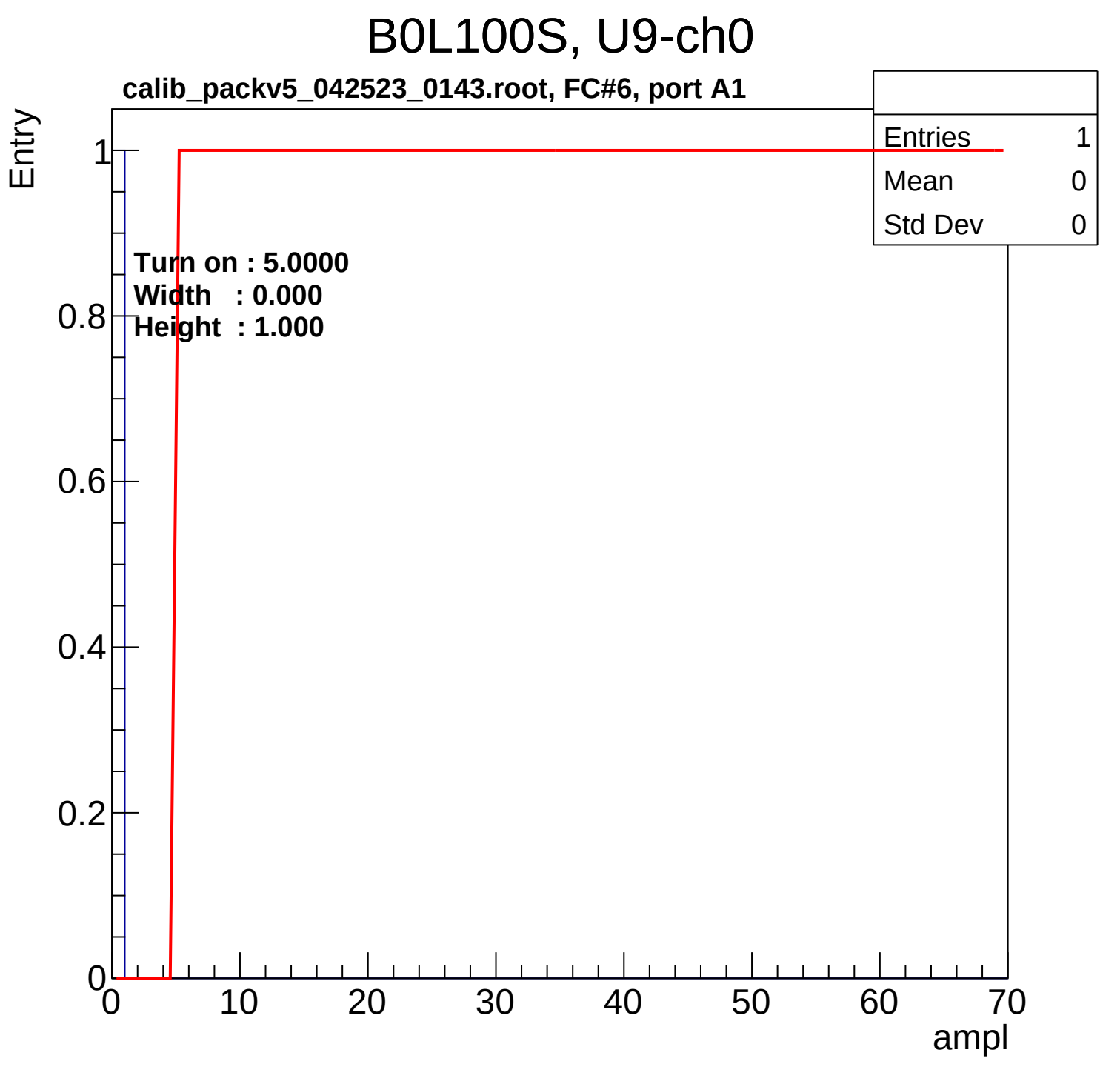
B0L100S, U9-ch0
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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0.6
0.4
0.2
0
0
10
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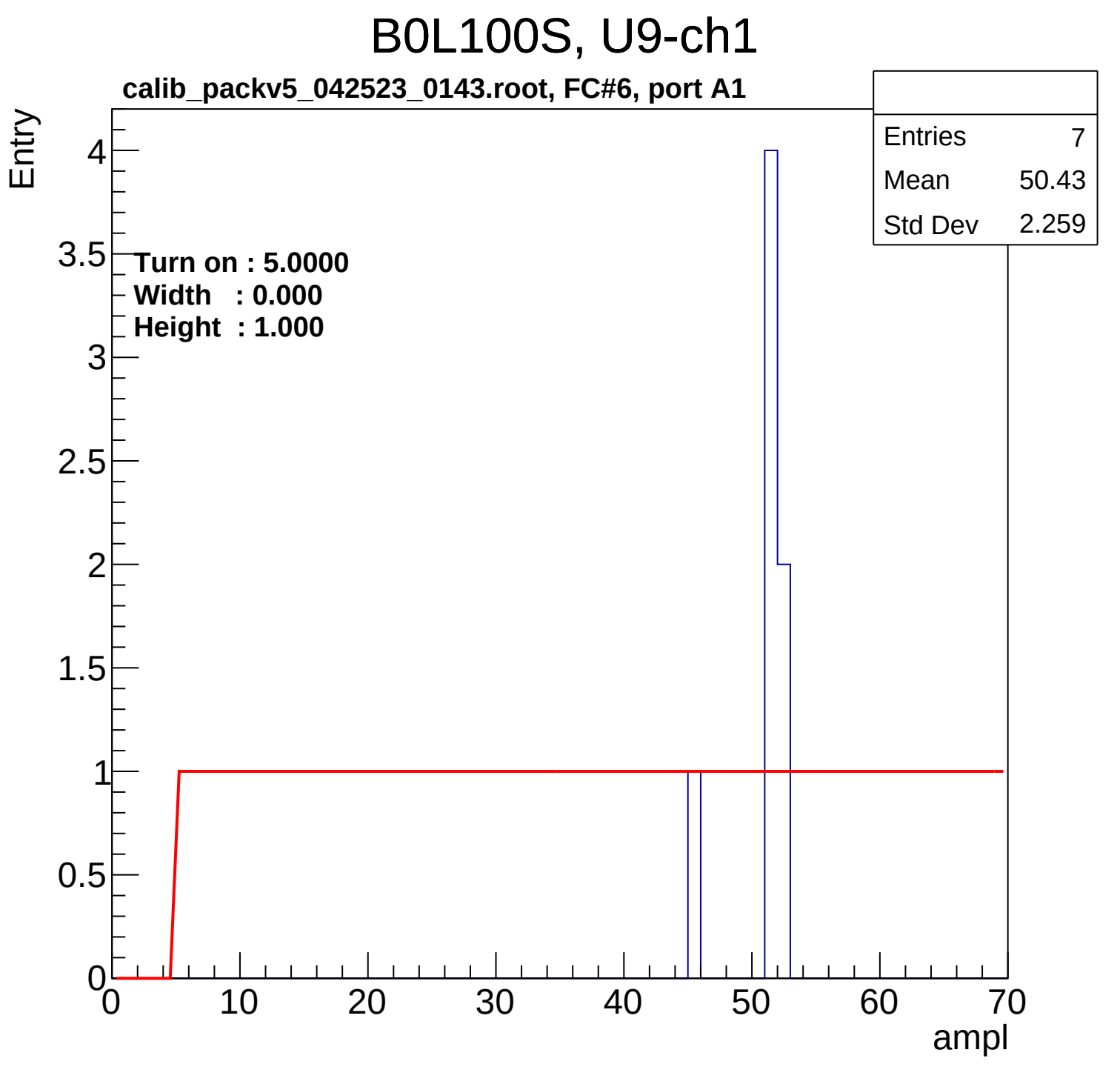
70
ampl


B0L100S, U9-ch1
calib_packv5_042523_0143.root, FC#6, port A1
Entries 7
Mean 50.43
Std Dev 2.259
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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40
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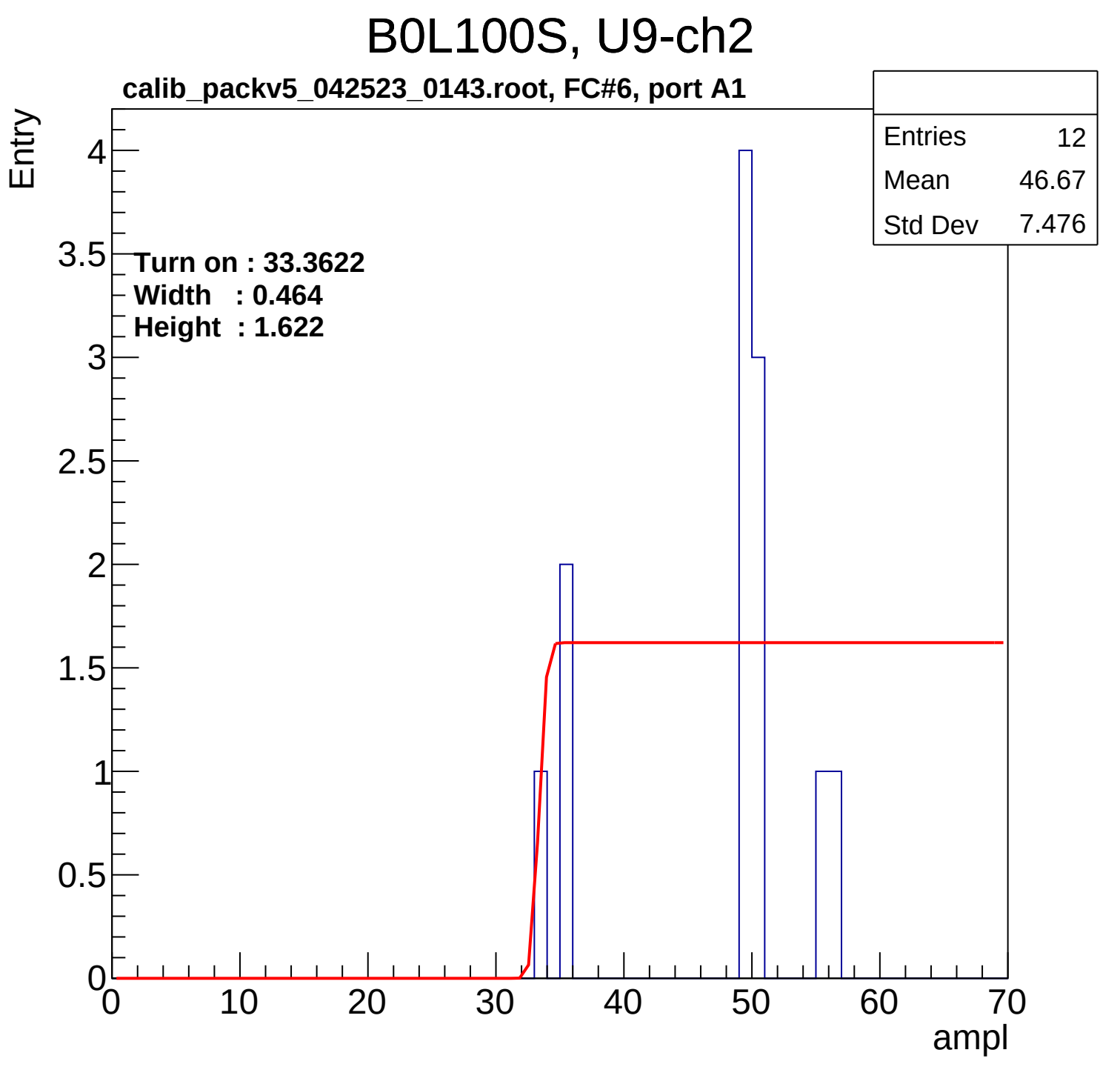
60
70


B0L100S, U9-ch2
calib_packv5_042523_0143.root, FC#6, port A1
Entries 12
Mean 46.67
Std Dev 7.476
Turn on : 33.3622
Width : 0.464
Height : 1.622
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
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0
10
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40
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60
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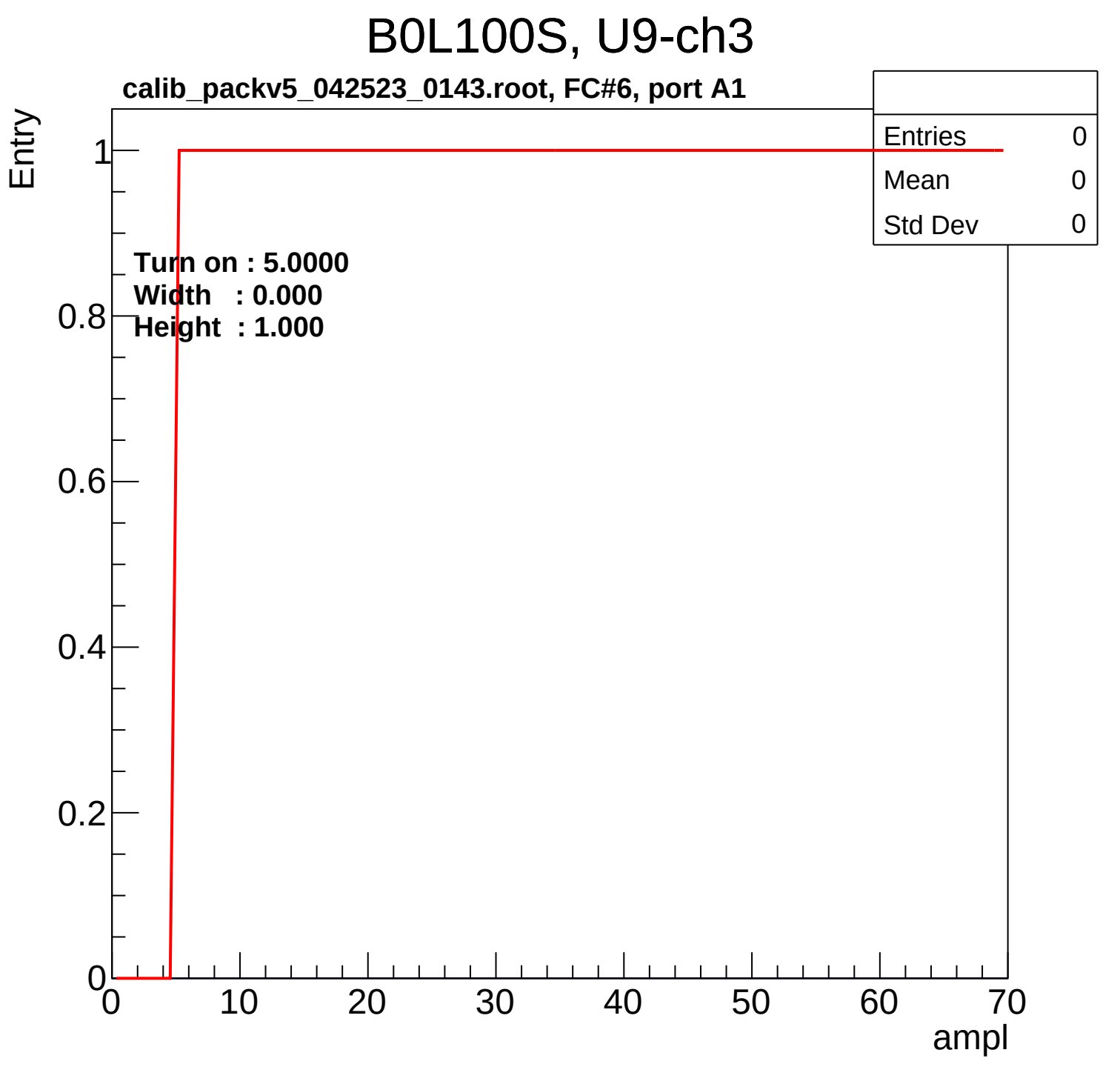
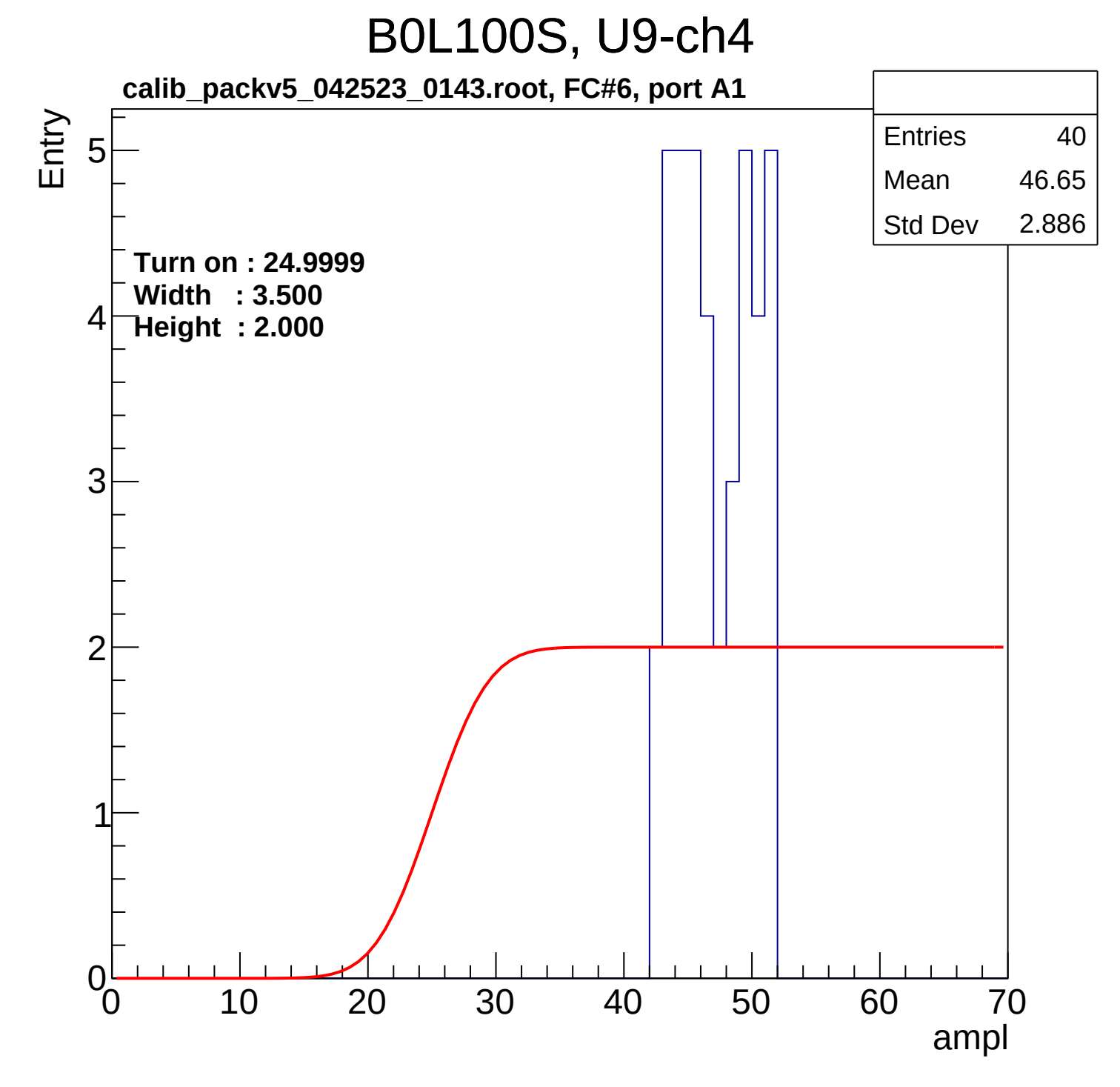

B0L100S, U9-ch3
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U9-ch4
calib_packv5_042523_0143.root, FC#6, port A1
Entries 40
Mean 46.65
Std Dev 2.886
Turn on : 24.9999
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
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40
50
60
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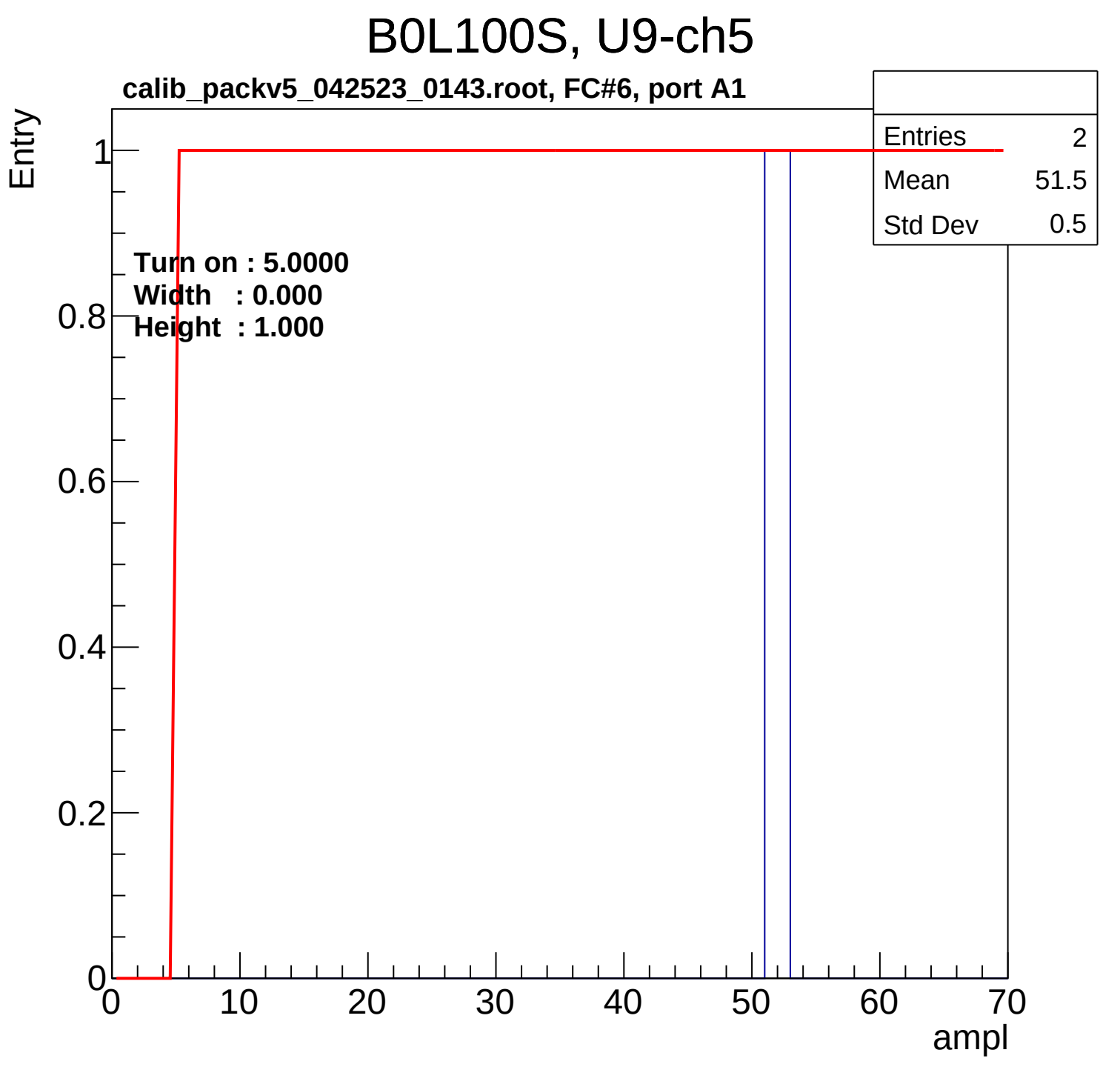
B0L100S, U9-ch5
calib_packv5_042523_0143.root, FC#6, port A1
Entries 2
Mean 51.5
Std Dev 0.5
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
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60
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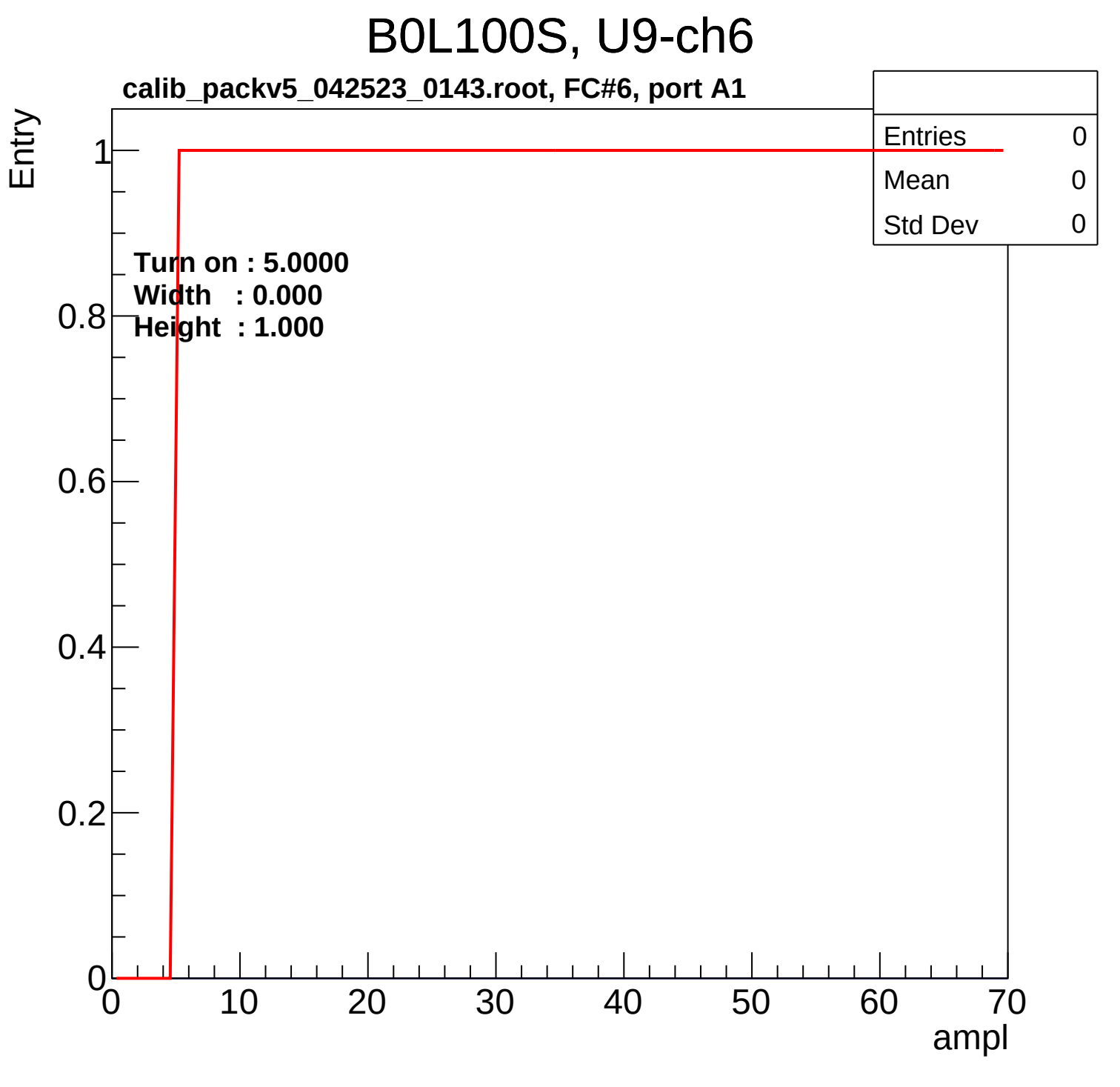
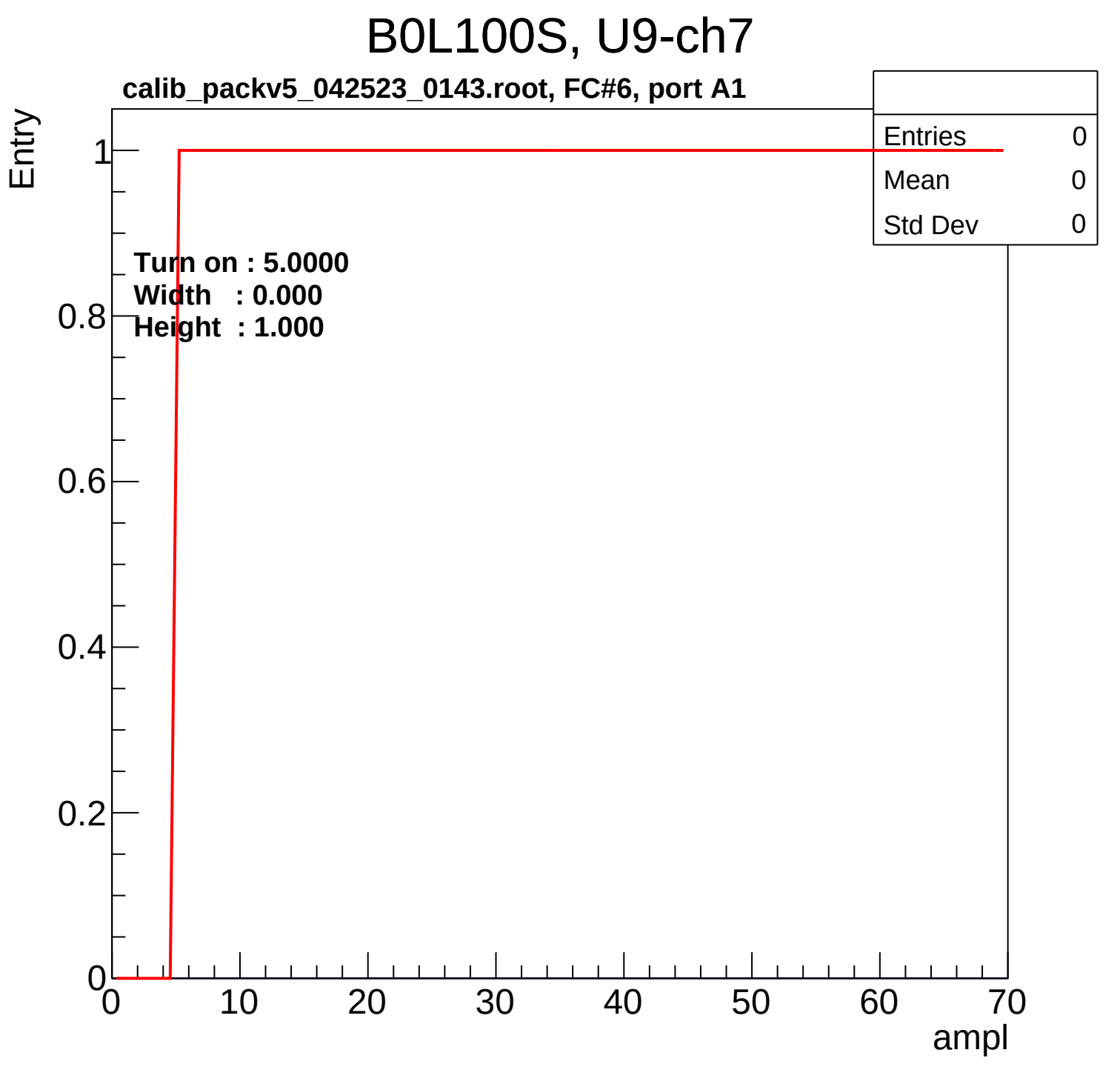
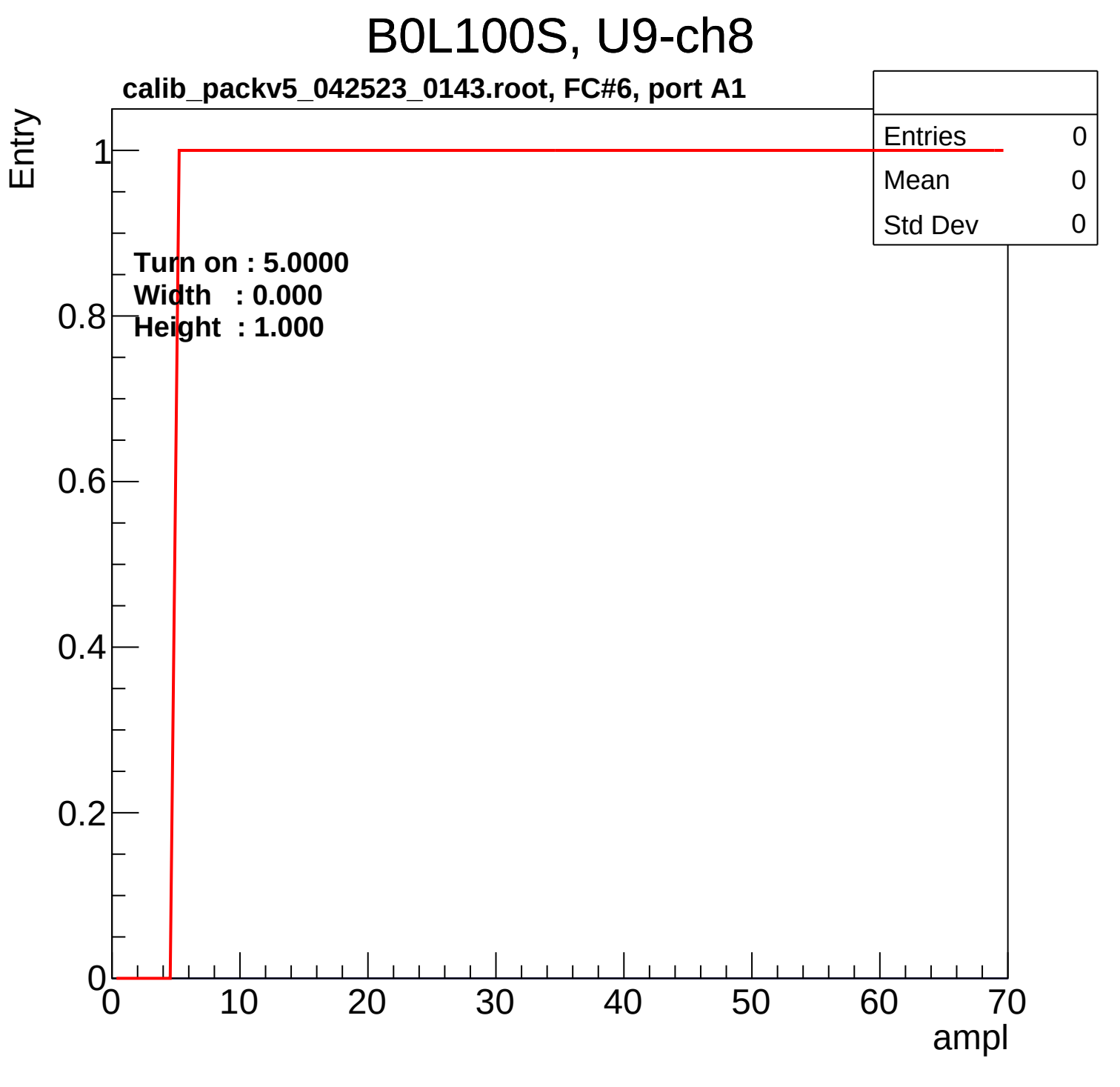
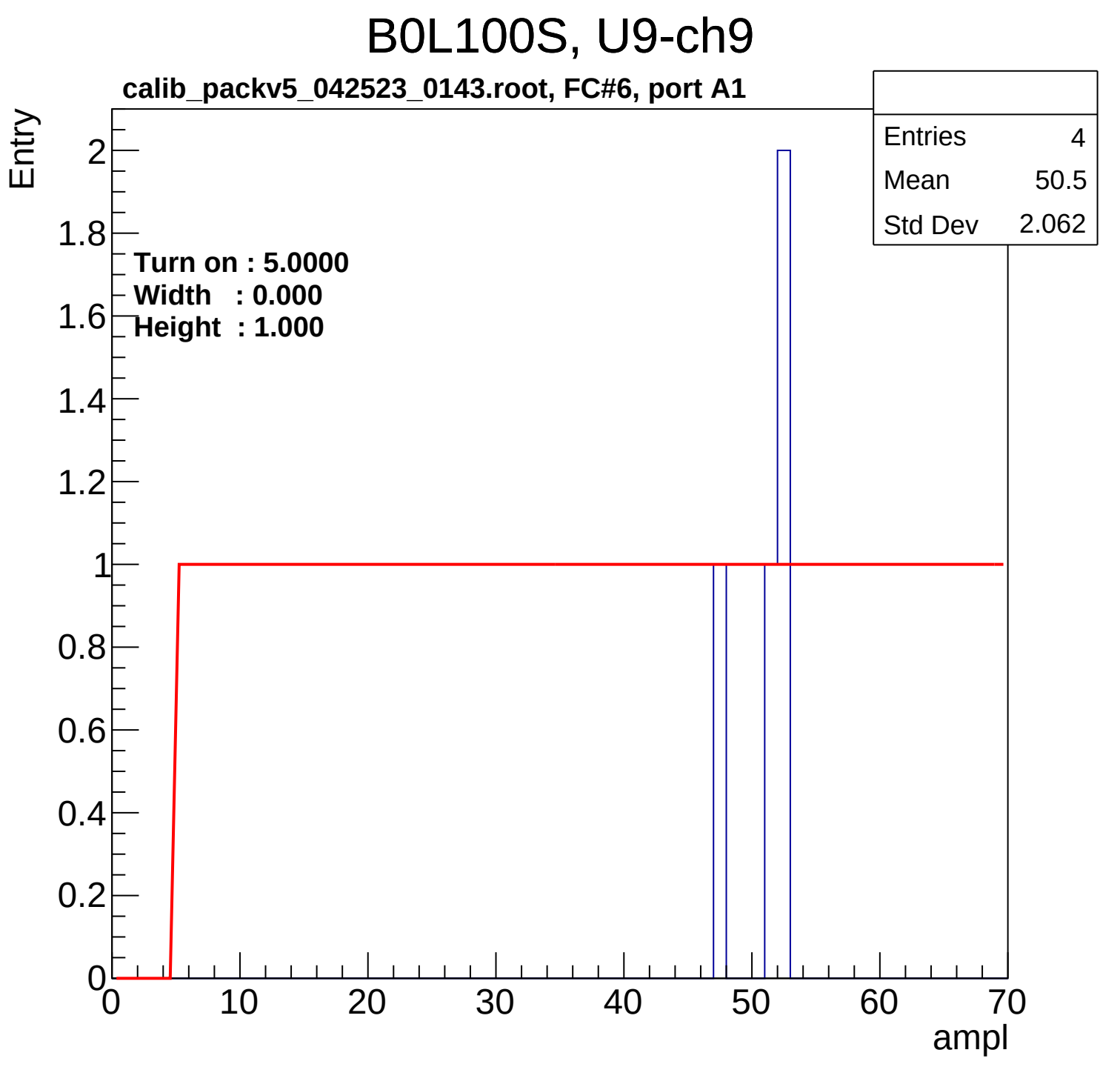

B0L100S, U9-ch6
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U9-ch7
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U9-ch8
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U9-ch9
calib_packv5_042523_0143.root, FC#6, port A1
Entries 4
Mean 50.5
Std Dev 2.062
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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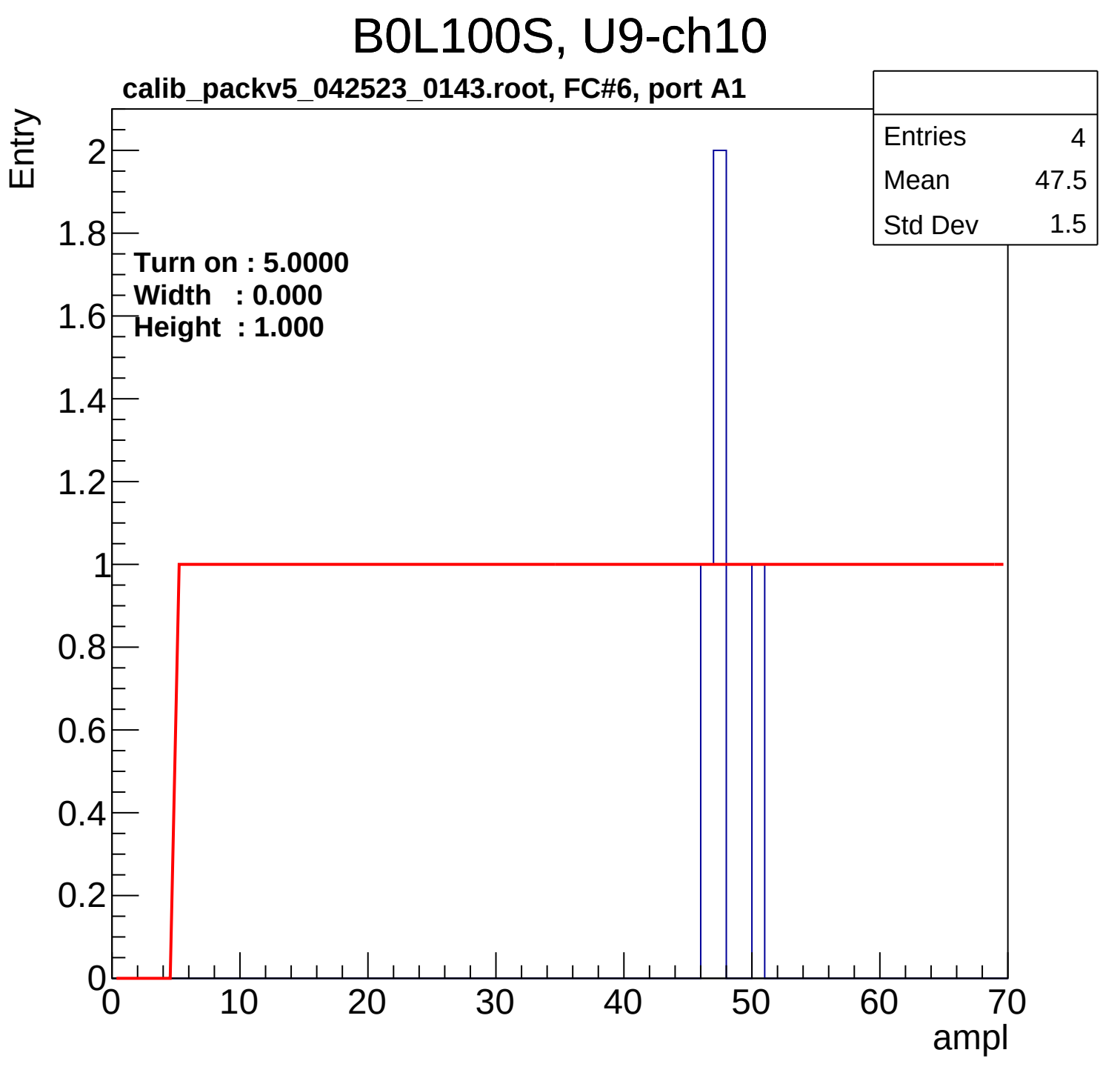
B0L100S, U9-ch10
calib_packv5_042523_0143.root, FC#6, port A1
Entries 4
Mean 47.5
Std Dev 1.5
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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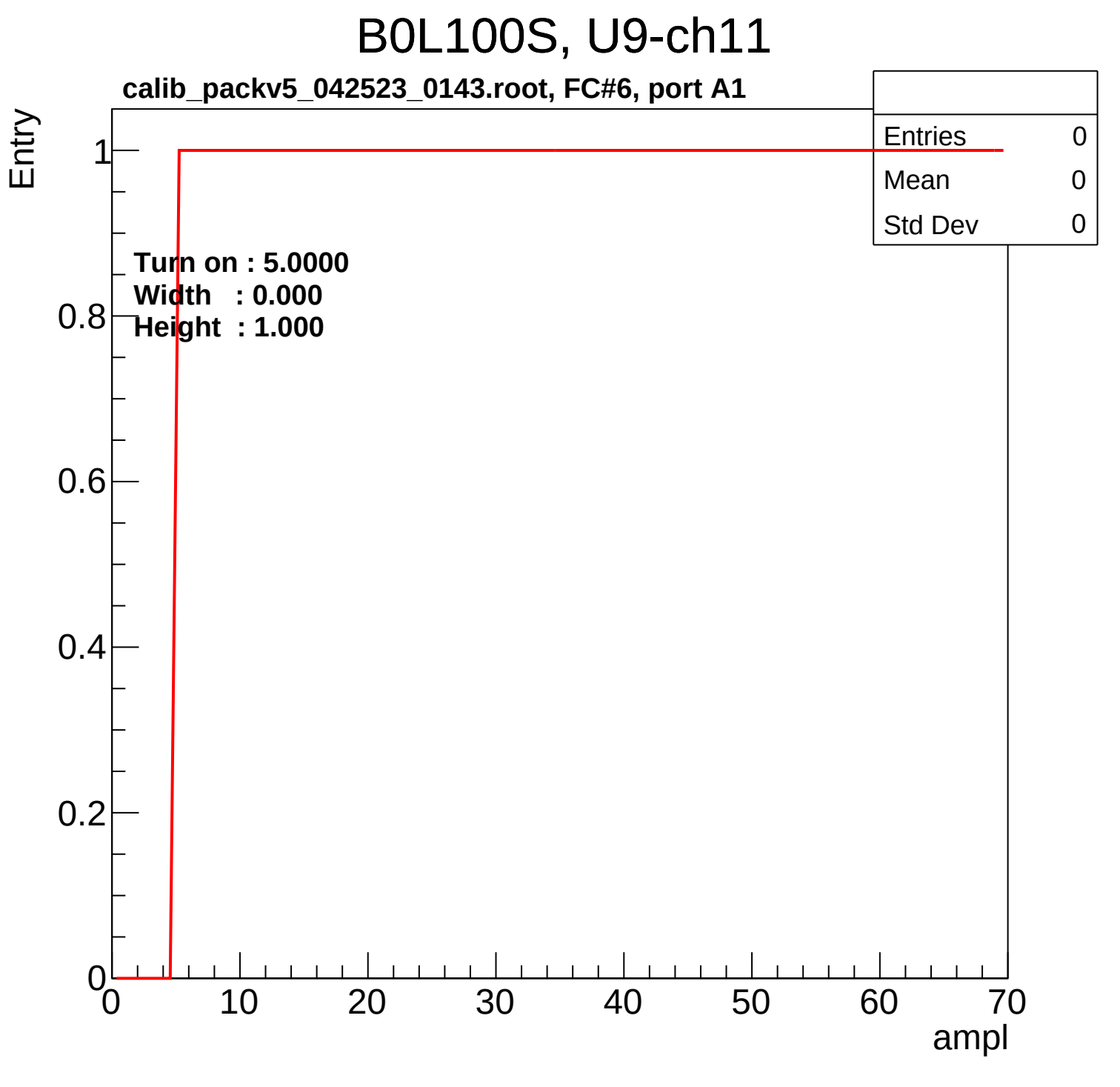
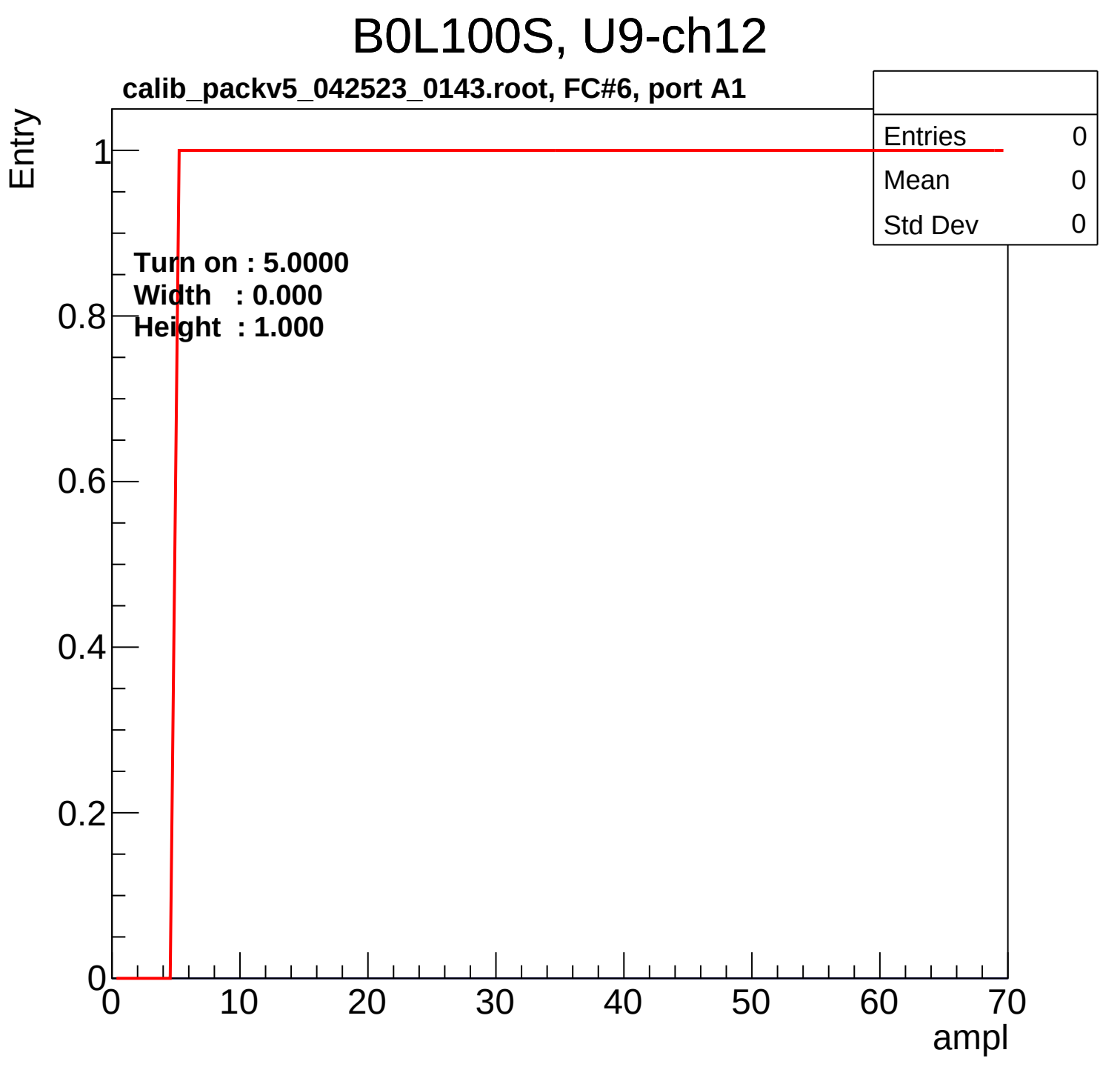
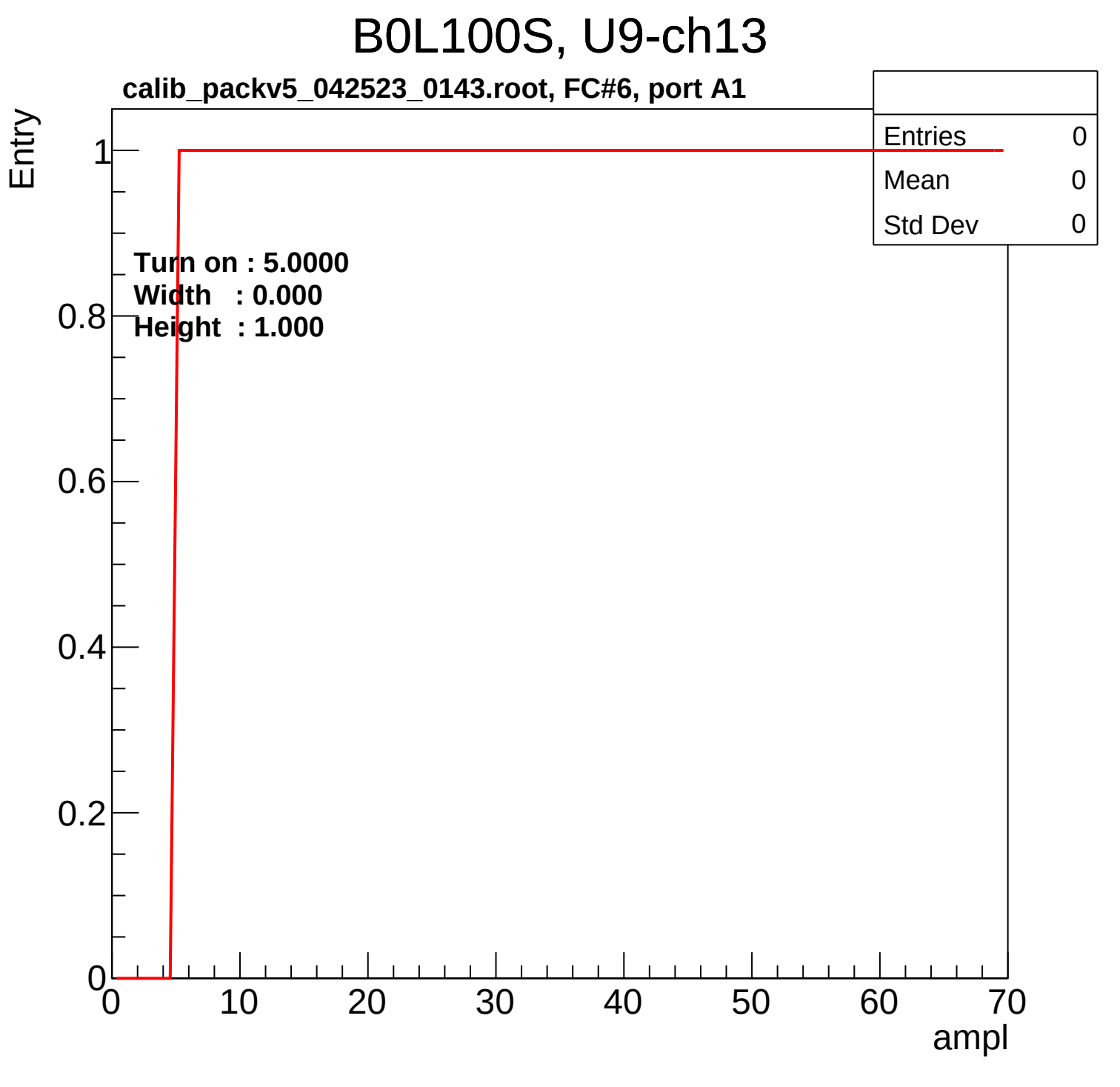
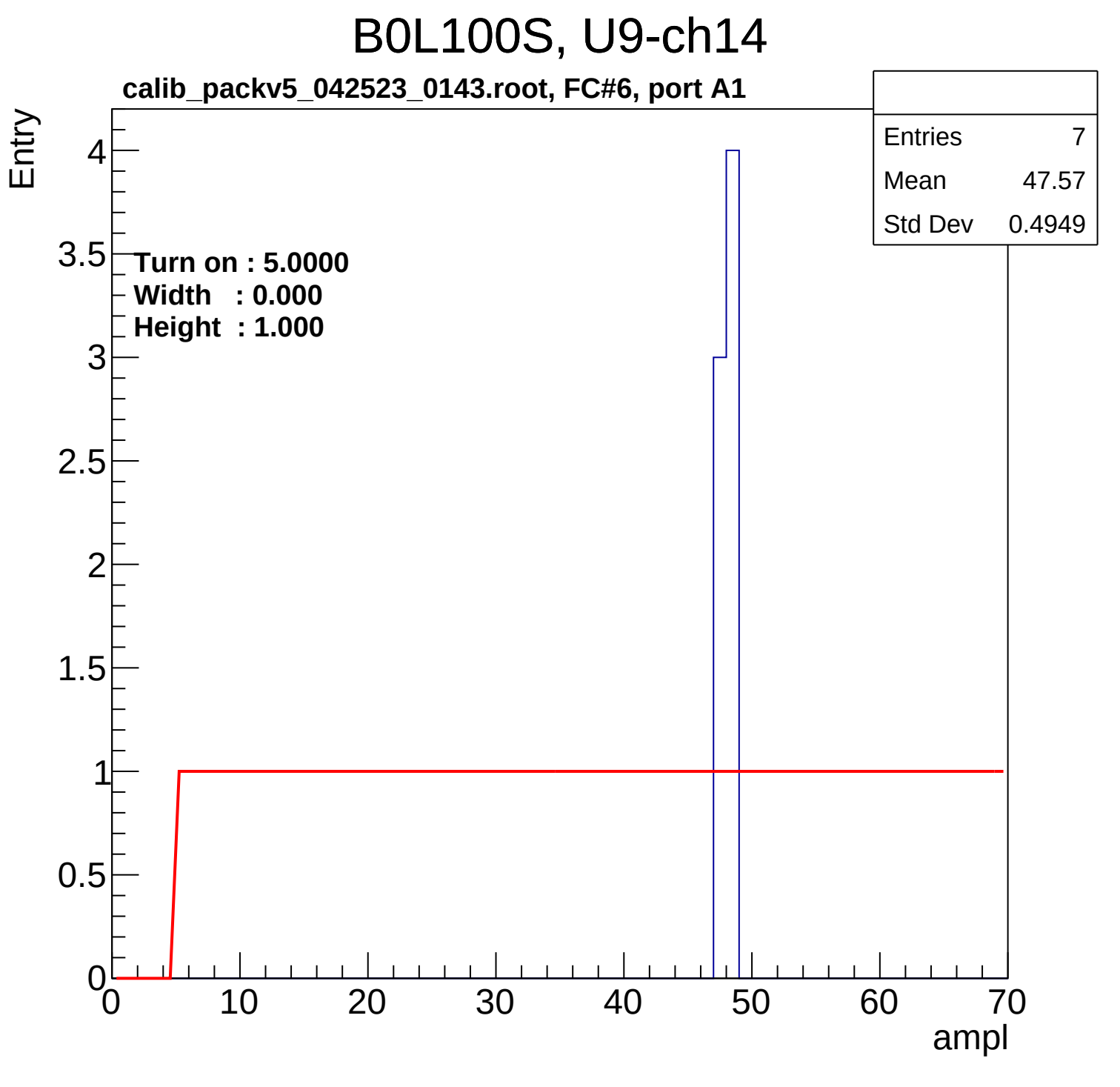

B0L100S, U9-ch11
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U9-ch12
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B0L100S, U9-ch13
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U9-ch14
calib_packv5_042523_0143.root, FC#6, port A1
Entries 7
Mean 47.57
Std Dev 0.4949
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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1.5
2
2.5
3
3.5
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0
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40
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60
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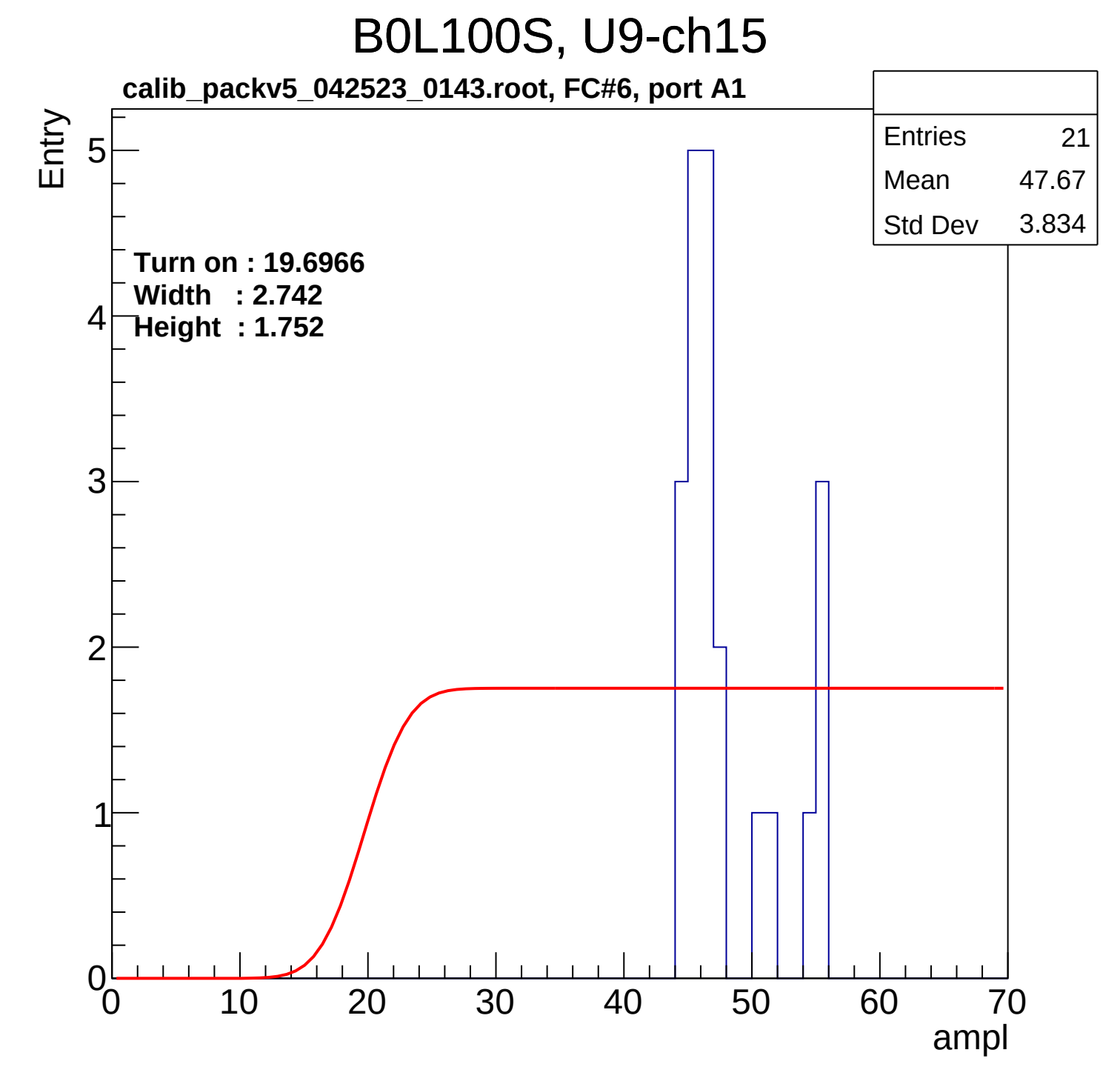
B0L100S, U9-ch15
calib_packv5_042523_0143.root, FC#6, port A1
Entries 21
Mean 47.67
Std Dev 3.834
Turn on : 19.6966
Width : 2.742
Height : 1.752
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
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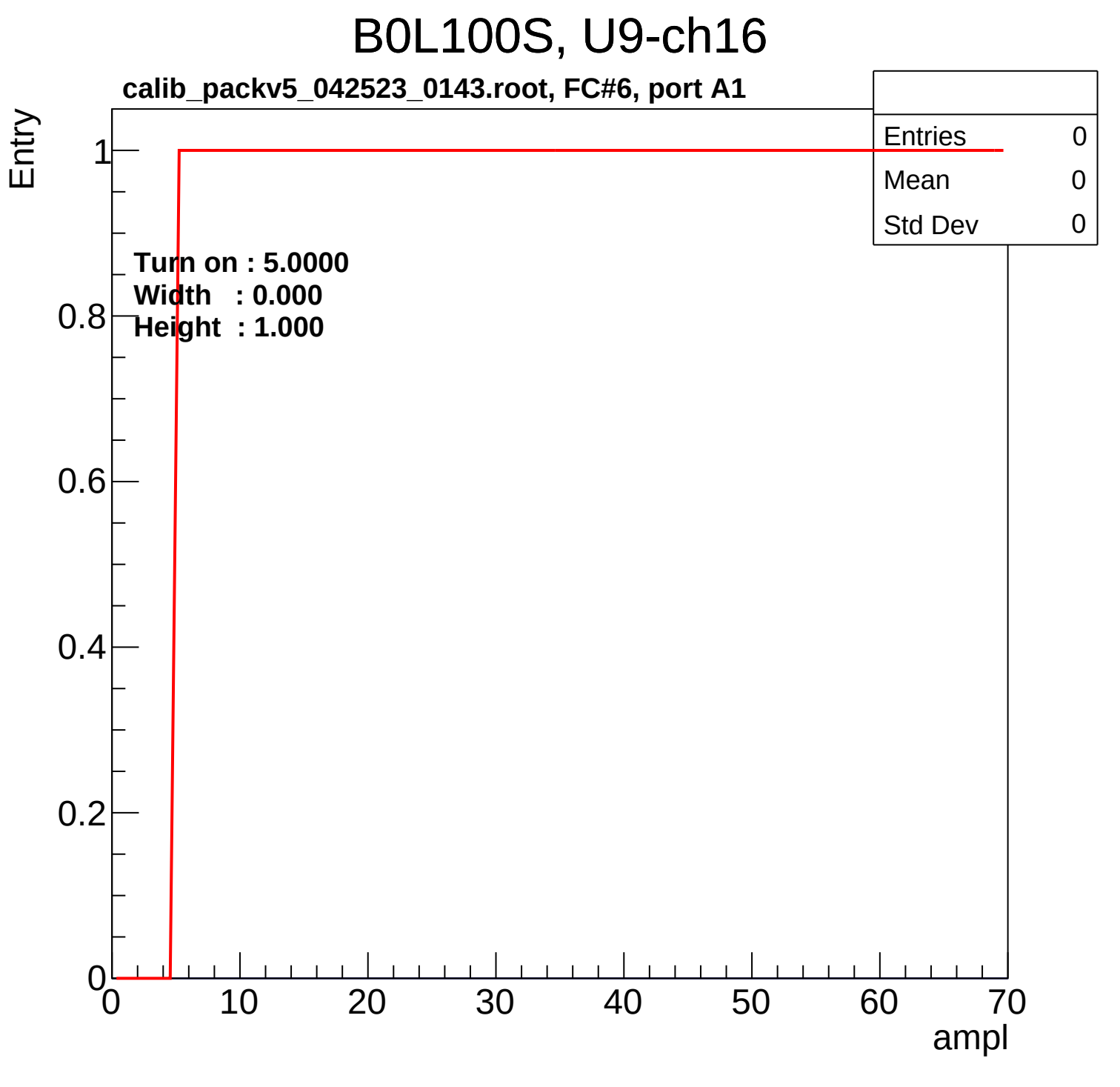
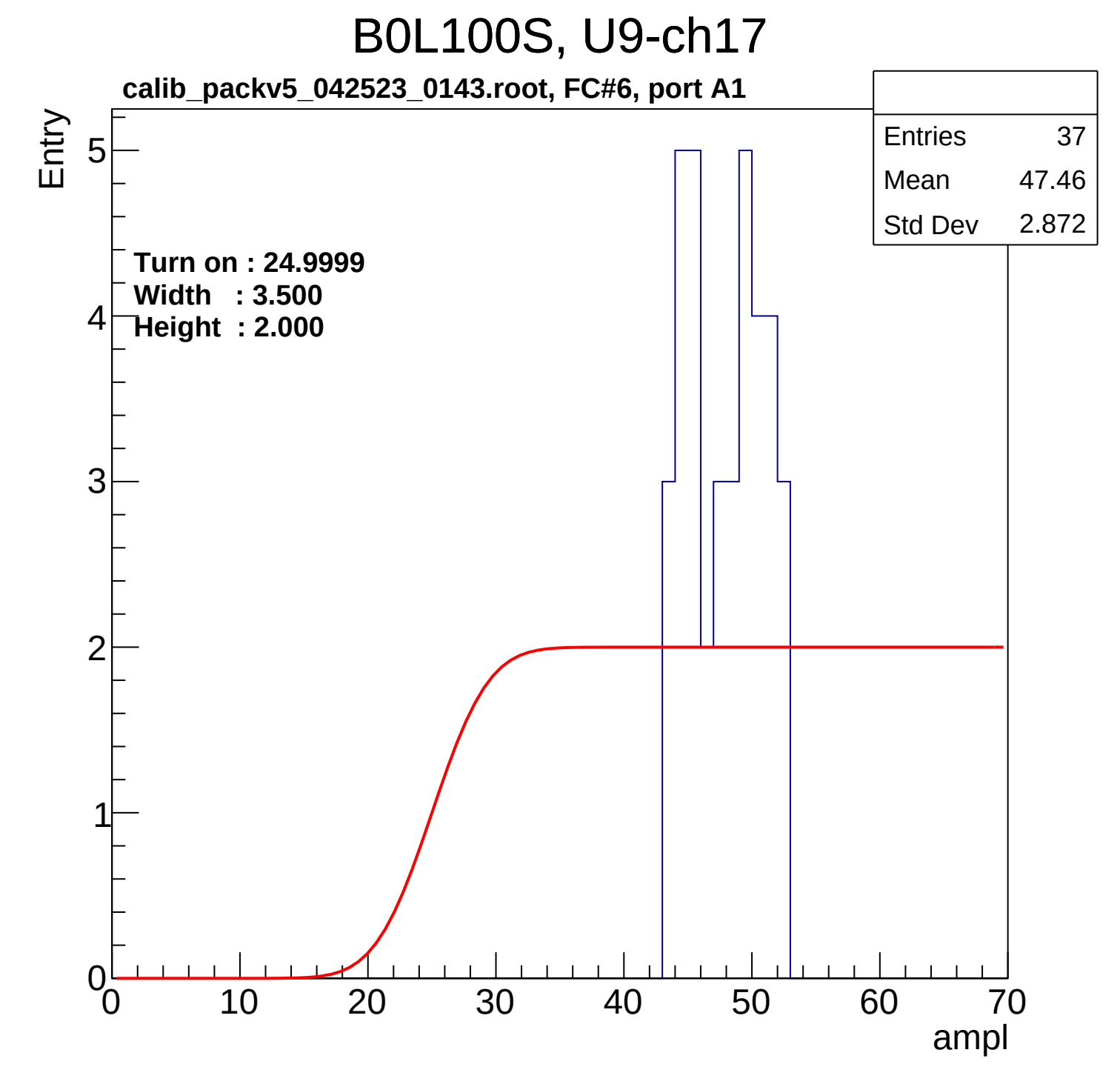

B0L100S, U9-ch16
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U9-ch17
calib_packv5_042523_0143.root, FC#6, port A1
Entries 37
Mean 47.46
Std Dev 2.872
Turn on : 24.9999
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
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40
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60
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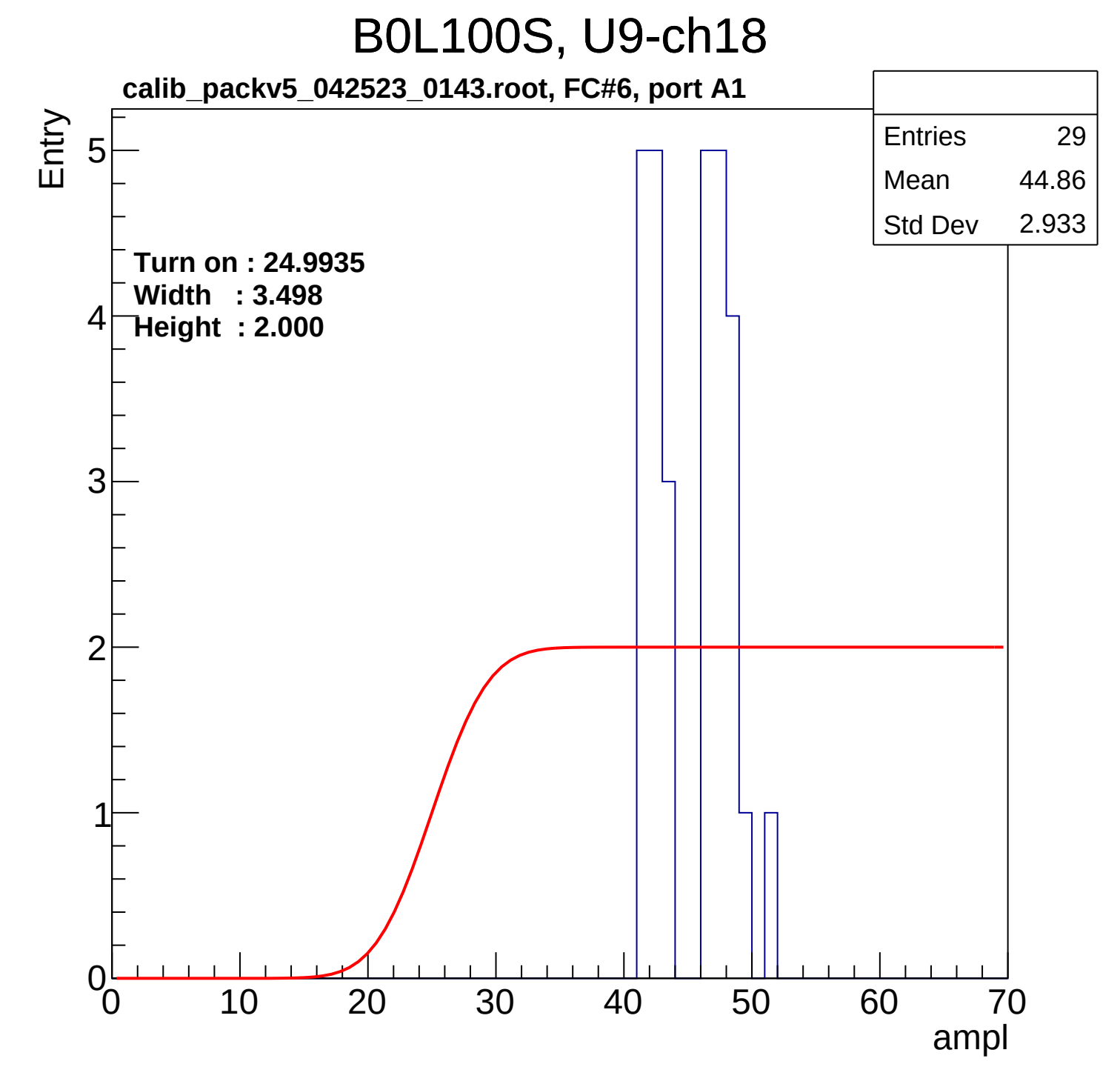
B0L100S, U9-ch18
calib_packv5_042523_0143.root, FC#6, port A1
Entries 29
Mean 44.86
Std Dev 2.933
Turn on : 24.9935
Width : 3.498
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
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20
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40
50
60
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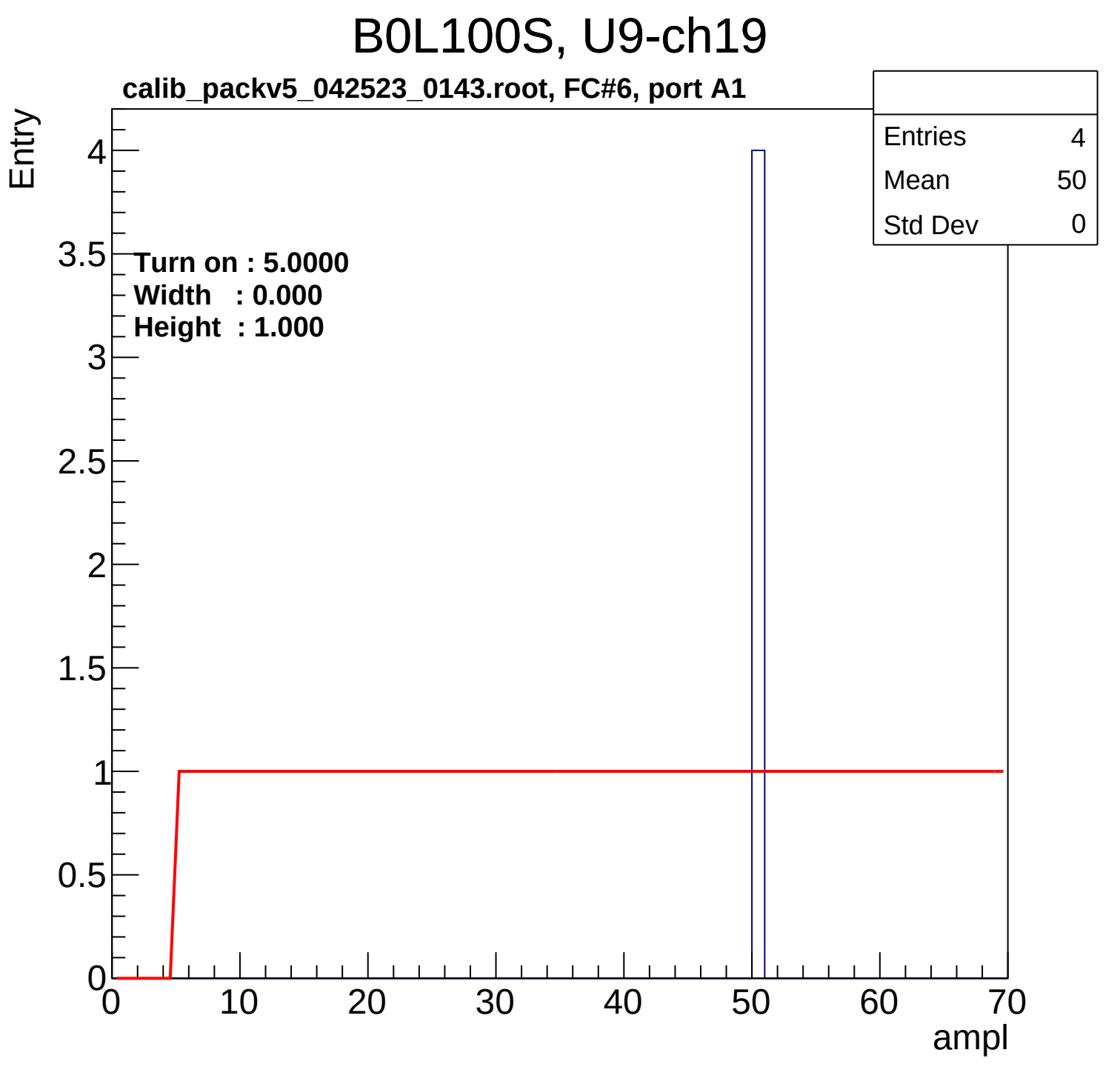
B0L100S, U9-ch19
calib_packv5_042523_0143.root, FC#6, port A1
Entries 4
Mean 50
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
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0
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60
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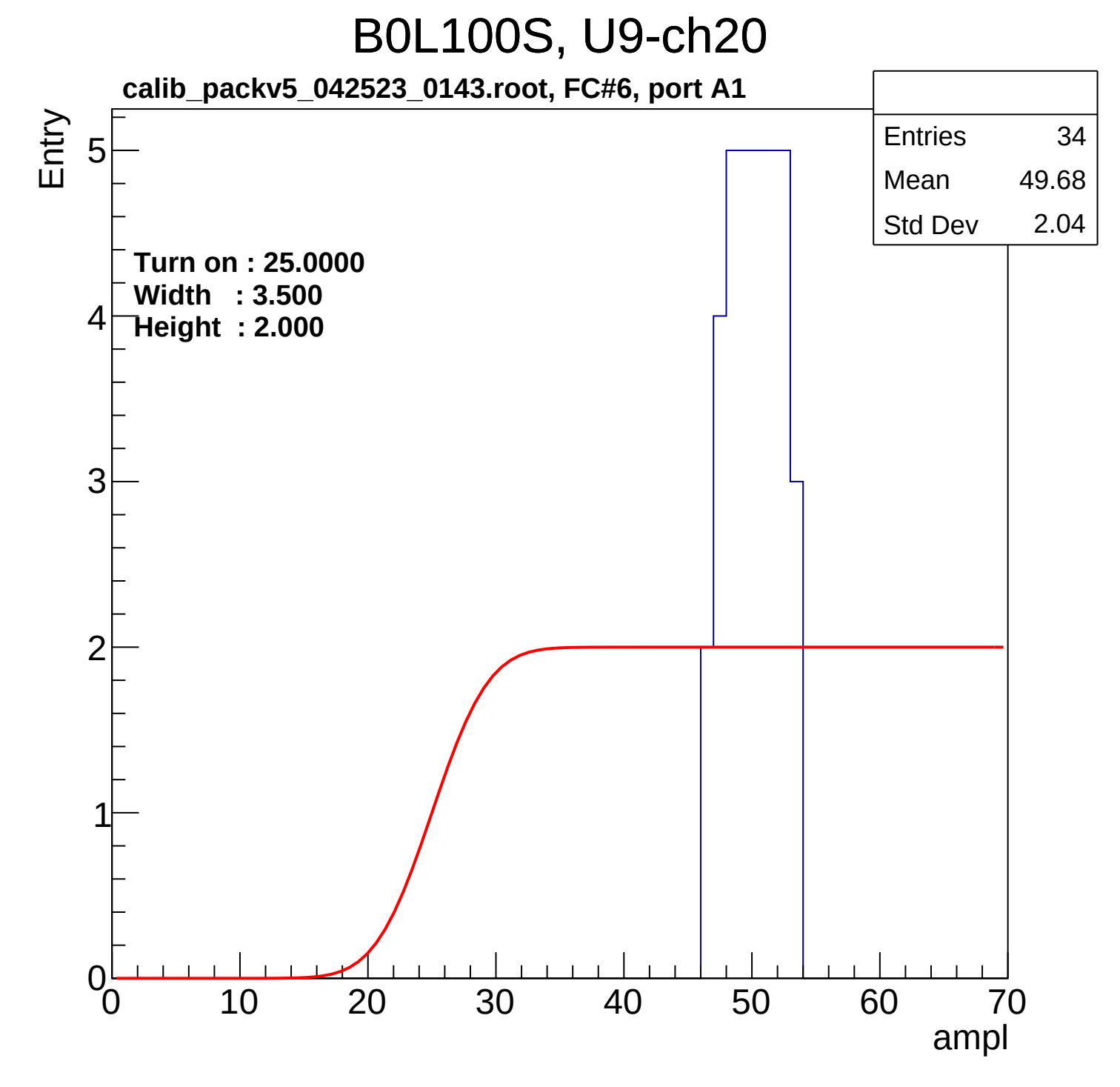
B0L100S, U9-ch20
calib_packv5_042523_0143.root, FC#6, port A1
Entries 34
Mean 49.68
Std Dev 2.04
Turn on : 25.0000
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
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40
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60
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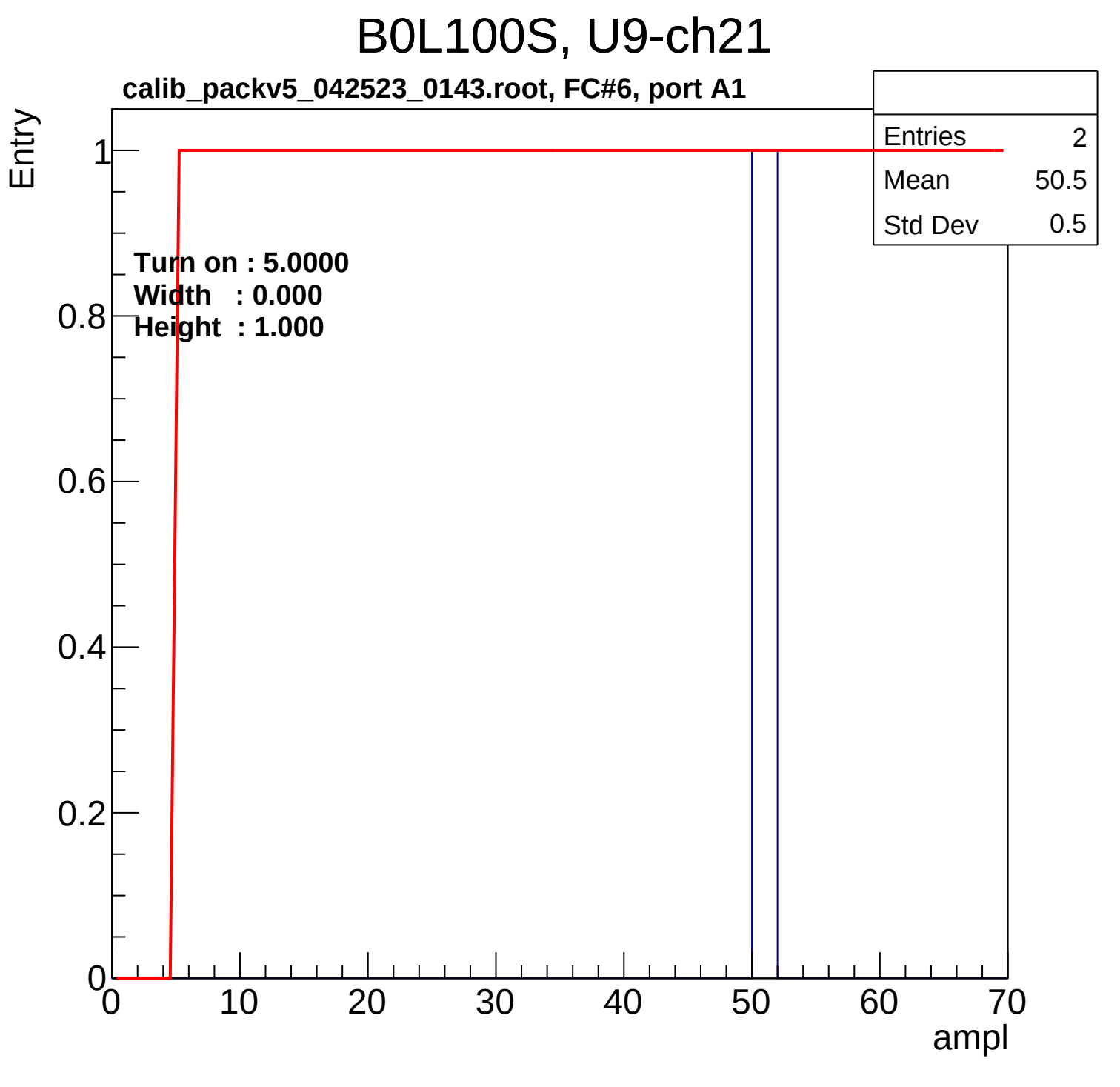
B0L100S, U9-ch21
calib_packv5_042523_0143.root, FC#6, port A1
Entries 2
Mean 50.5
Std Dev 0.5
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
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40
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60
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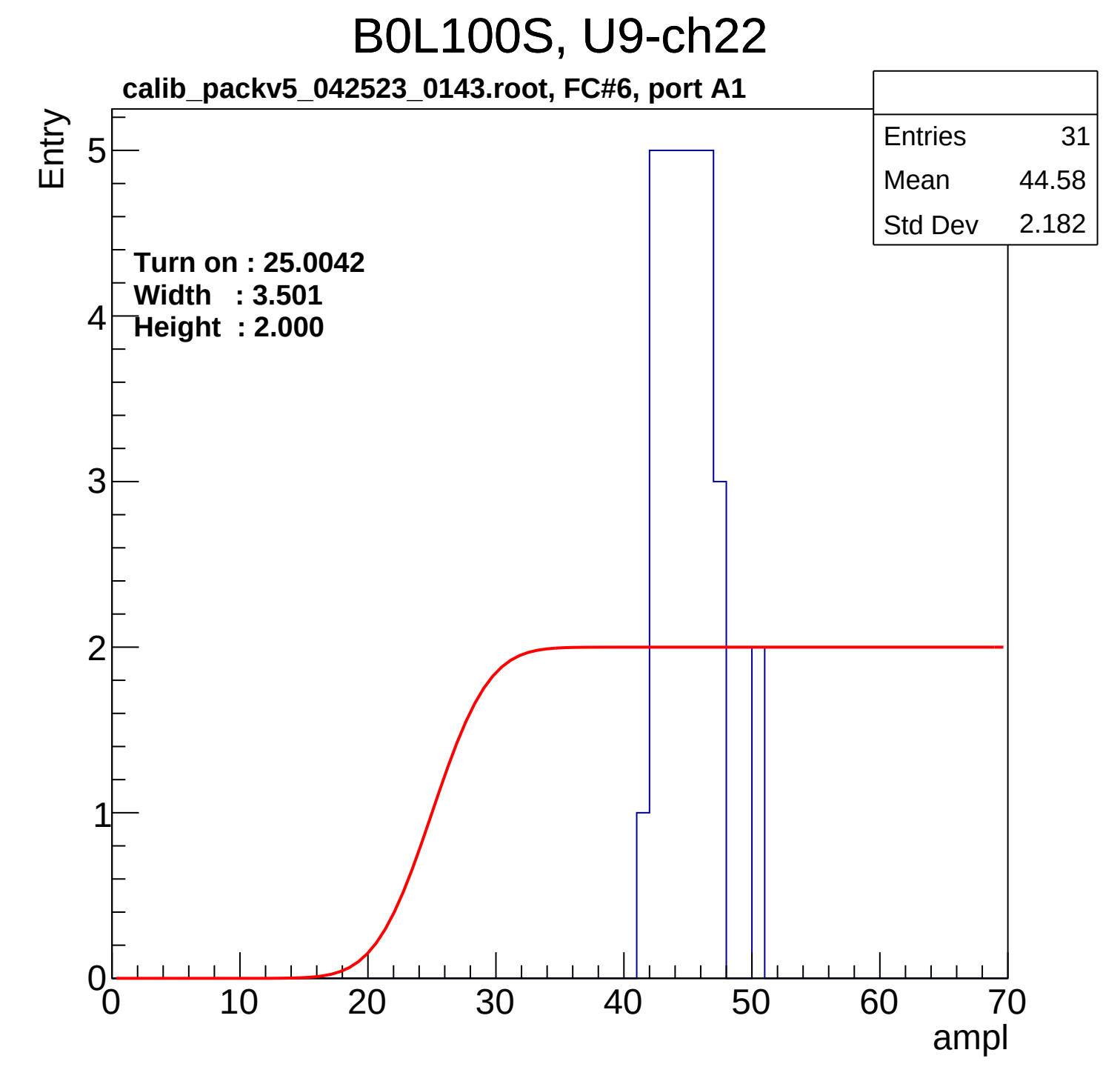
B0L100S, U9-ch22
calib_packv5_042523_0143.root, FC#6, port A1
Entries 31
Mean 44.58
Std Dev 2.182
Turn on : 25.0042
Width : 3.501
Height : 2.000
Entry
ampl
0
1
2
3
4
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0
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60
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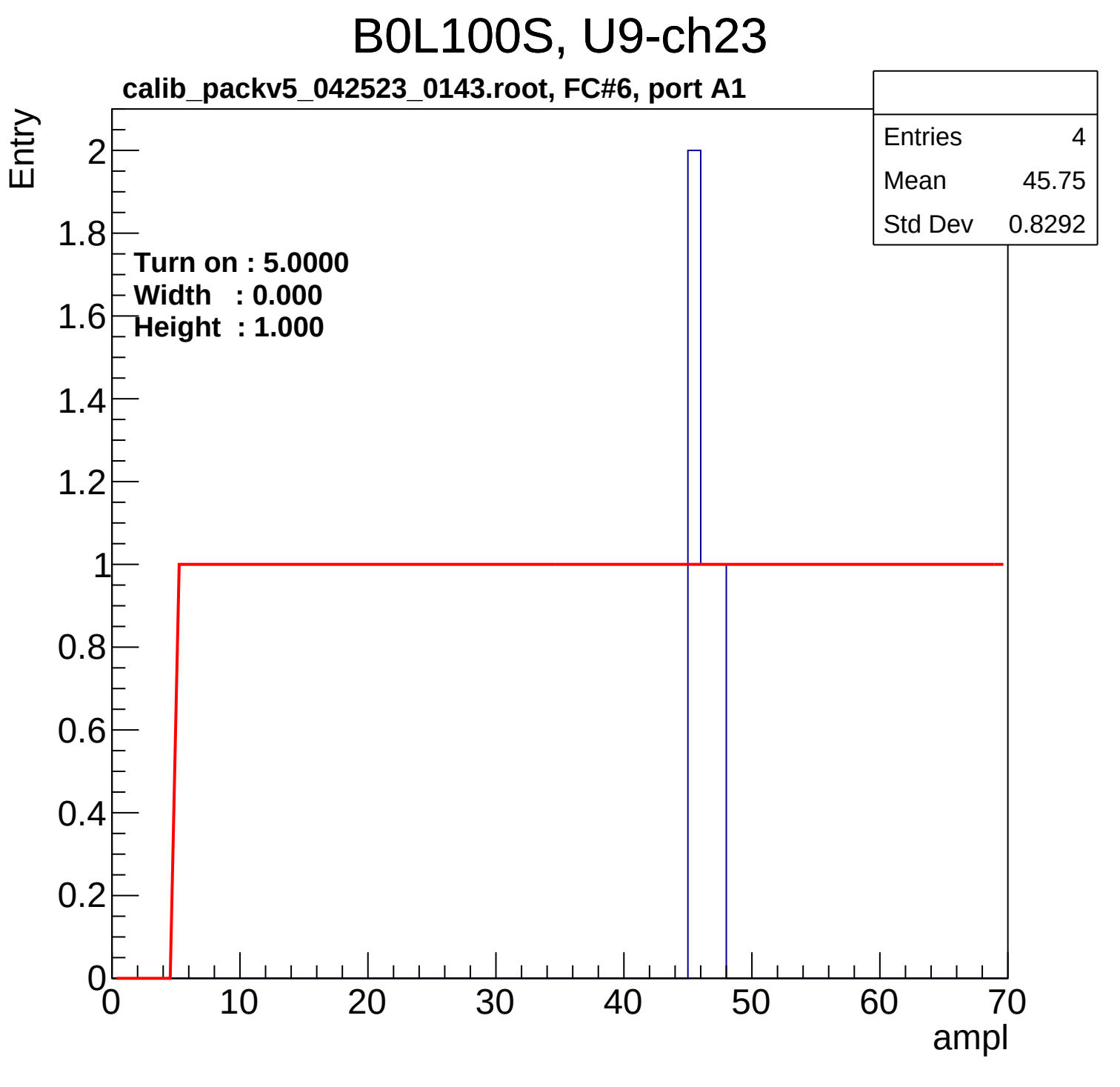
B0L100S, U9-ch23
calib_packv5_042523_0143.root, FC#6, port A1
Entries 4
Mean 45.75
Std Dev 0.8292
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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60
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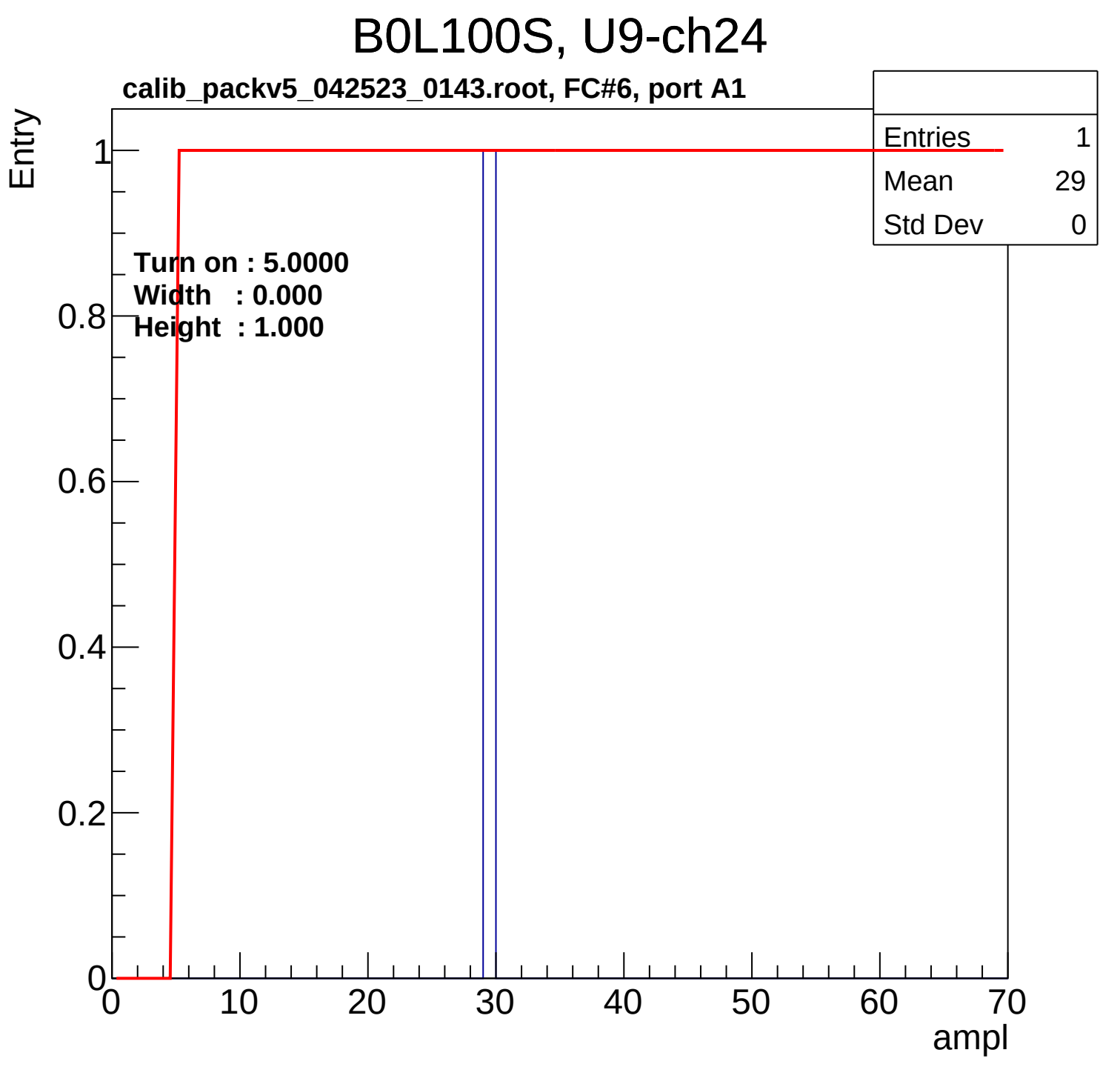
B0L100S, U9-ch24
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 29
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
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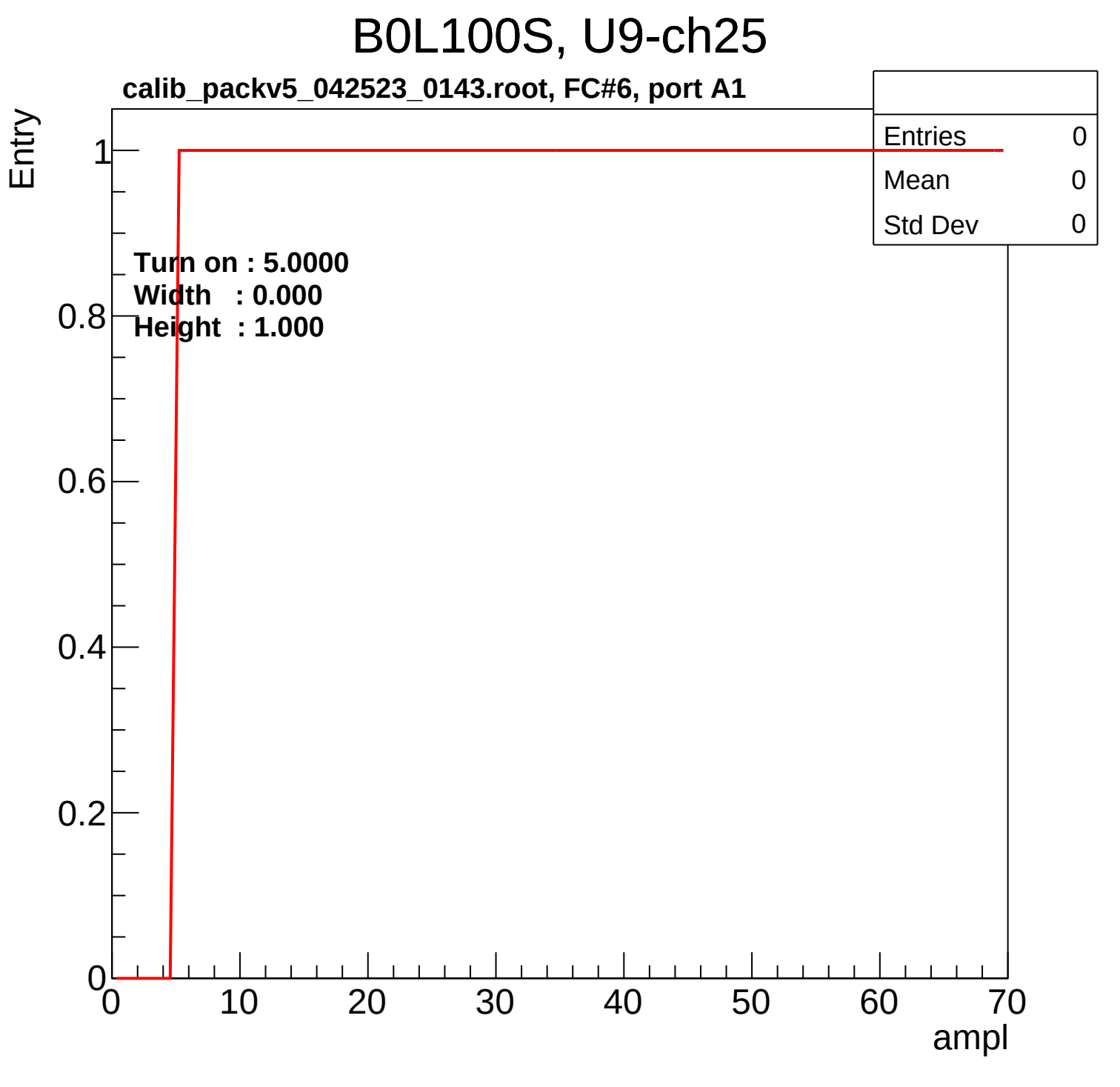
40
50
60
70


B0L100S, U9-ch25
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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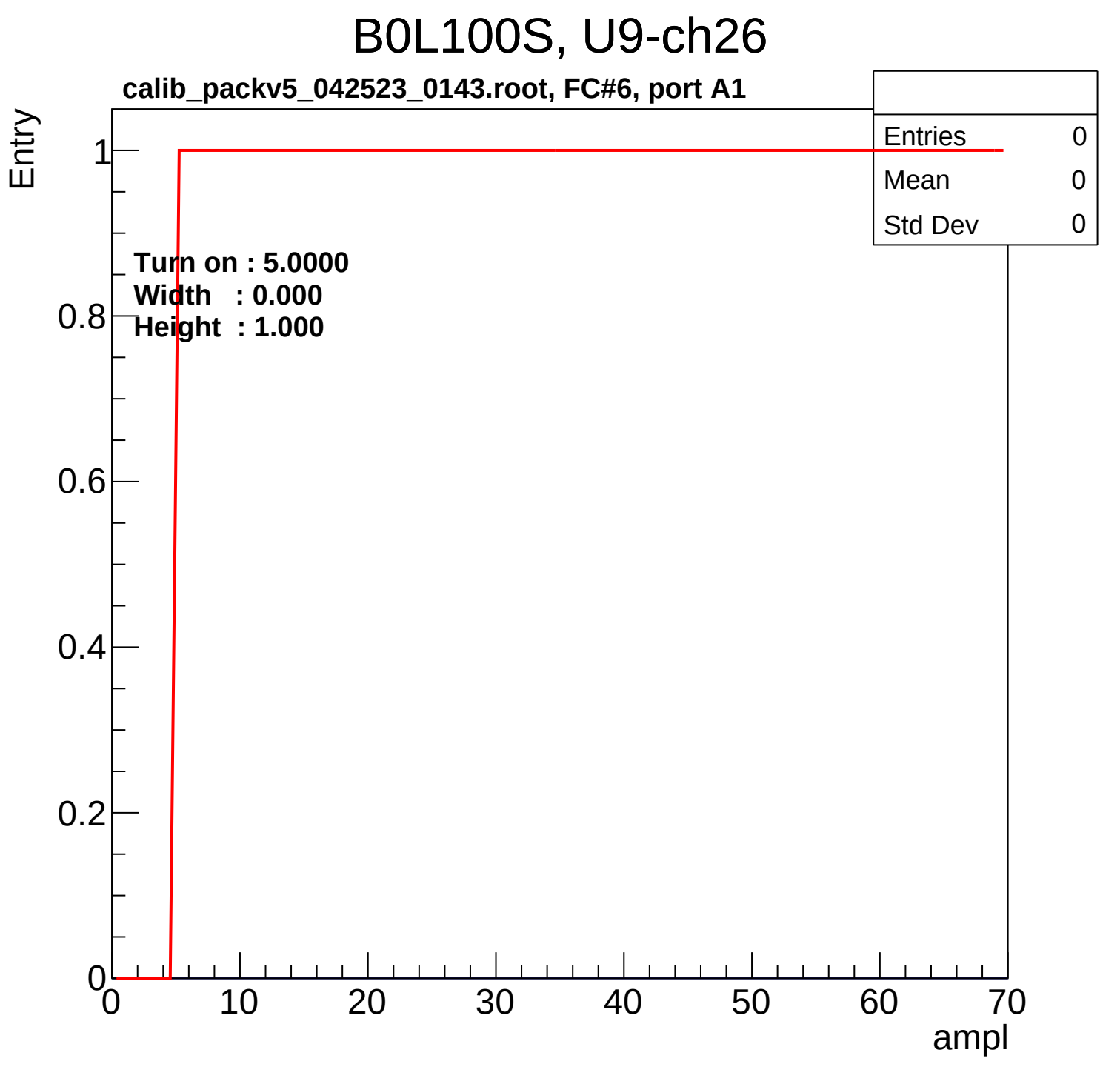
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U9-ch26
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
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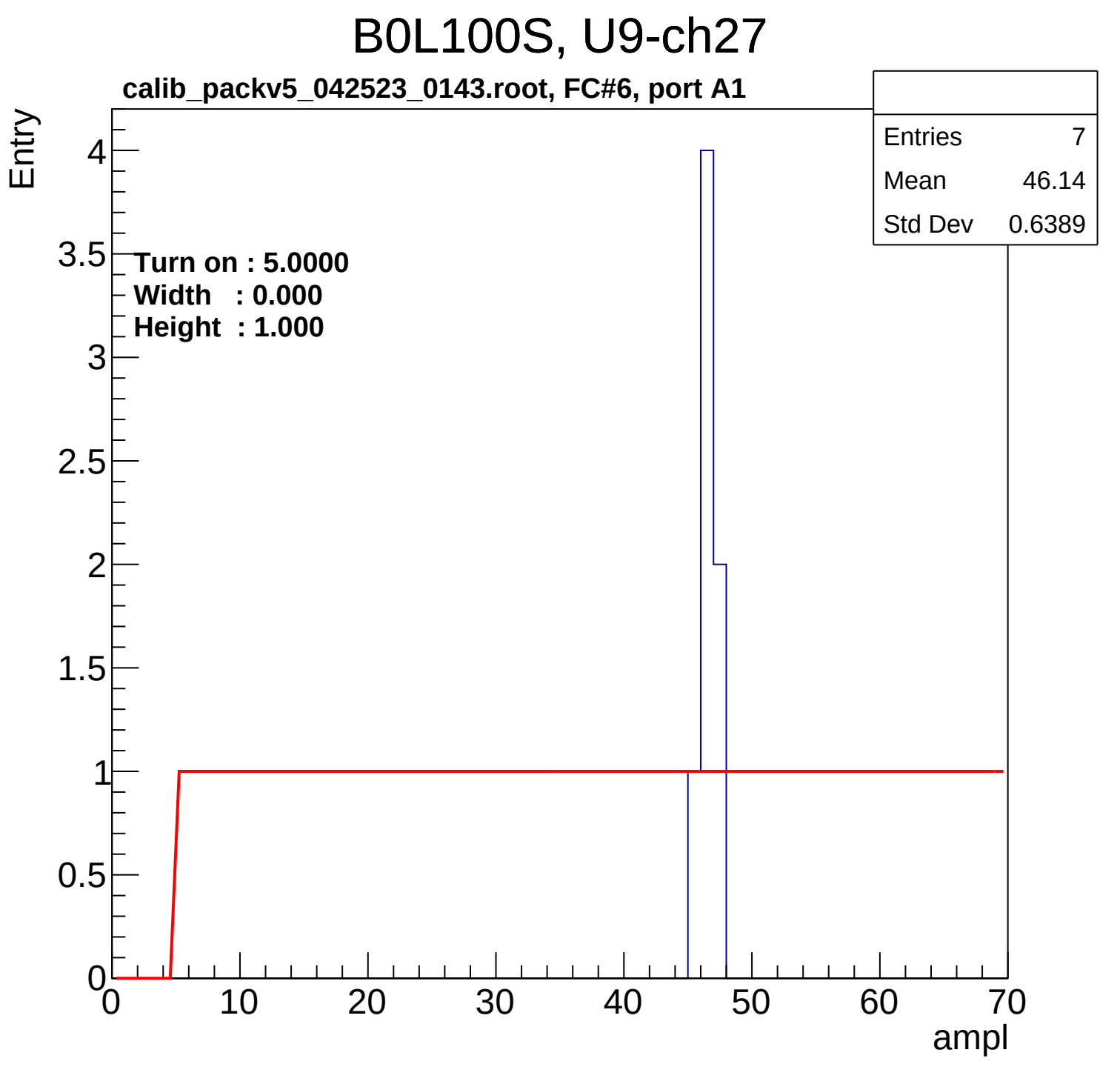
B0L100S, U9-ch27
calib_packv5_042523_0143.root, FC#6, port A1
Entries 7
Mean 46.14
Std Dev 0.6389
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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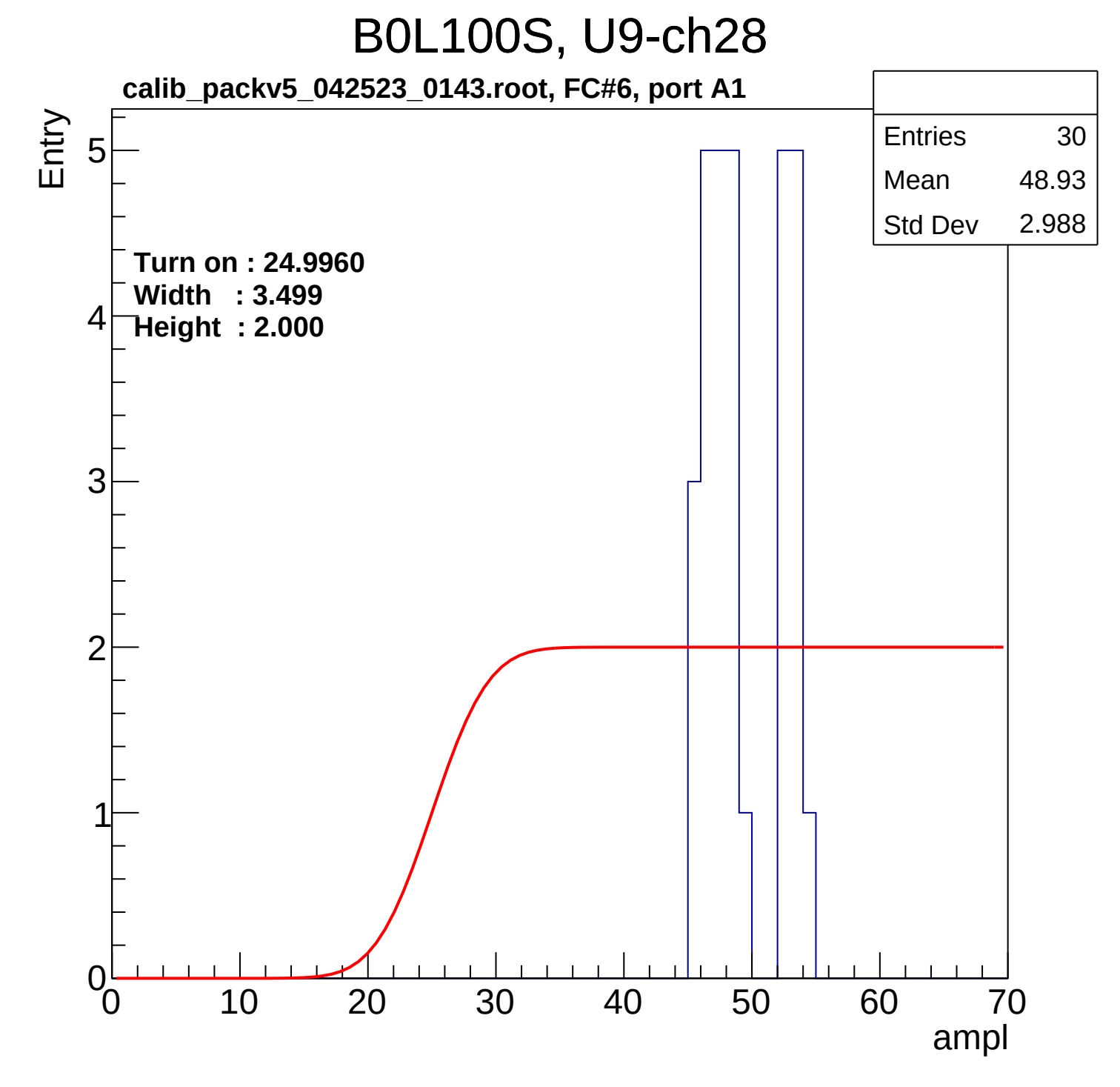
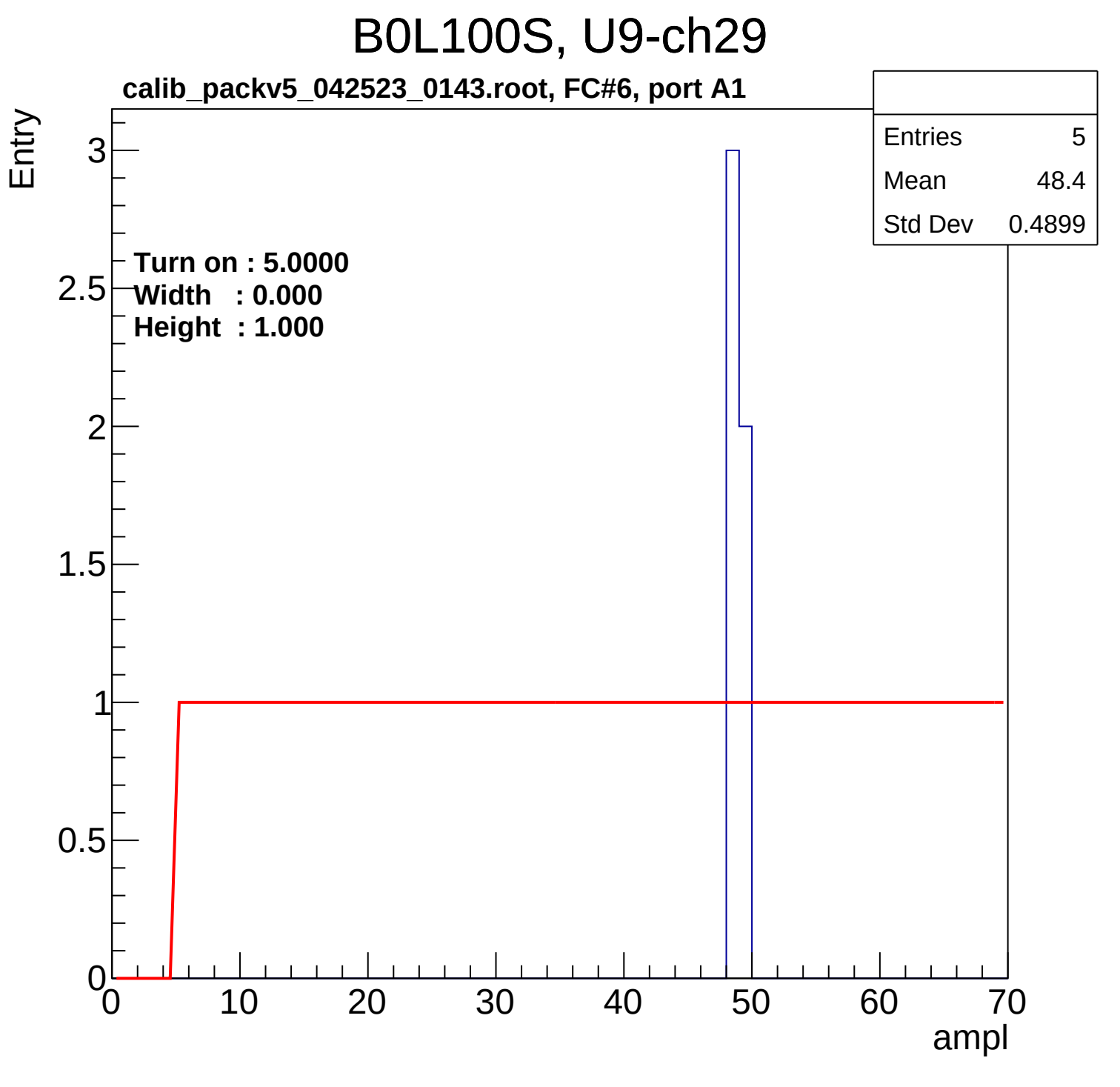
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B0L100S, U9-ch28
calib_packv5_042523_0143.root, FC#6, port A1
Entries 30
Mean 48.93
Std Dev 2.988
Turn on : 24.9960
Width : 3.499
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B0L100S, U9-ch29
calib_packv5_042523_0143.root, FC#6, port A1
Entries 5
Mean 48.4
Std Dev 0.4899
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
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50
60
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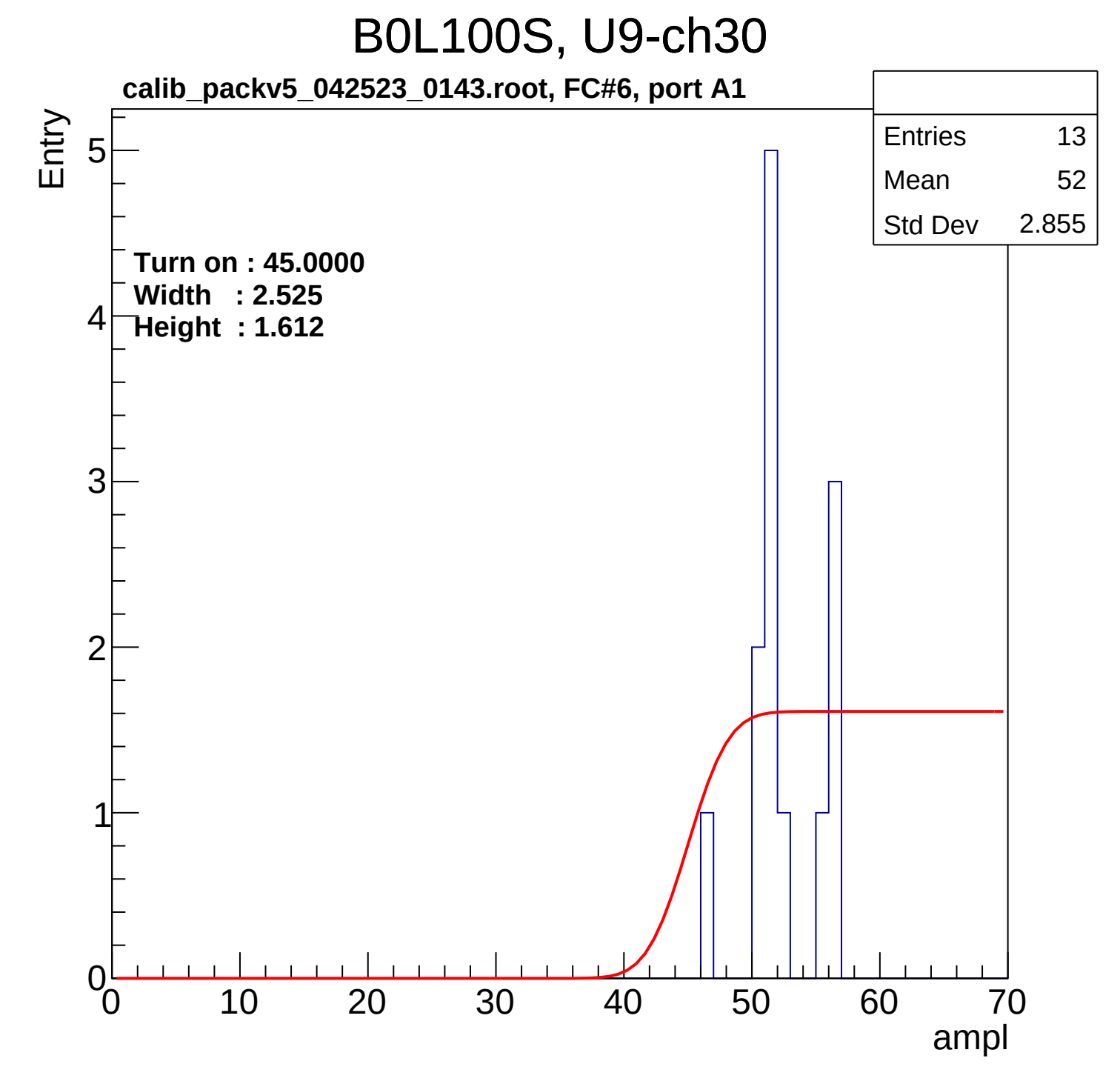
B0L100S, U9-ch30
calib_packv5_042523_0143.root, FC#6, port A1
Entries 13
Mean 52
Std Dev 2.855
Turn on : 45.0000
Width : 2.525
Height : 1.612
Entry
ampl
0
1
2
3
4
5
0
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40
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60
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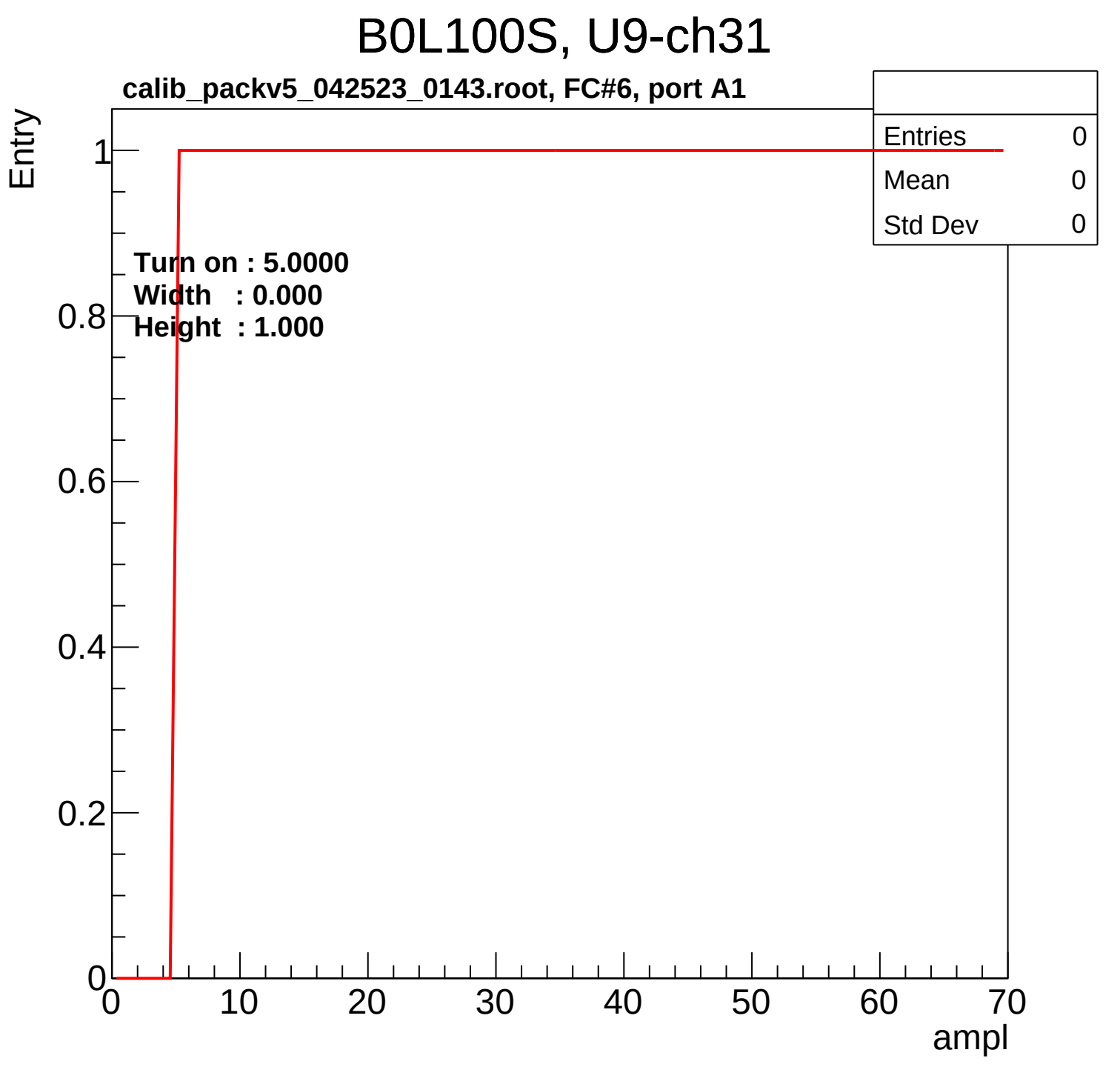
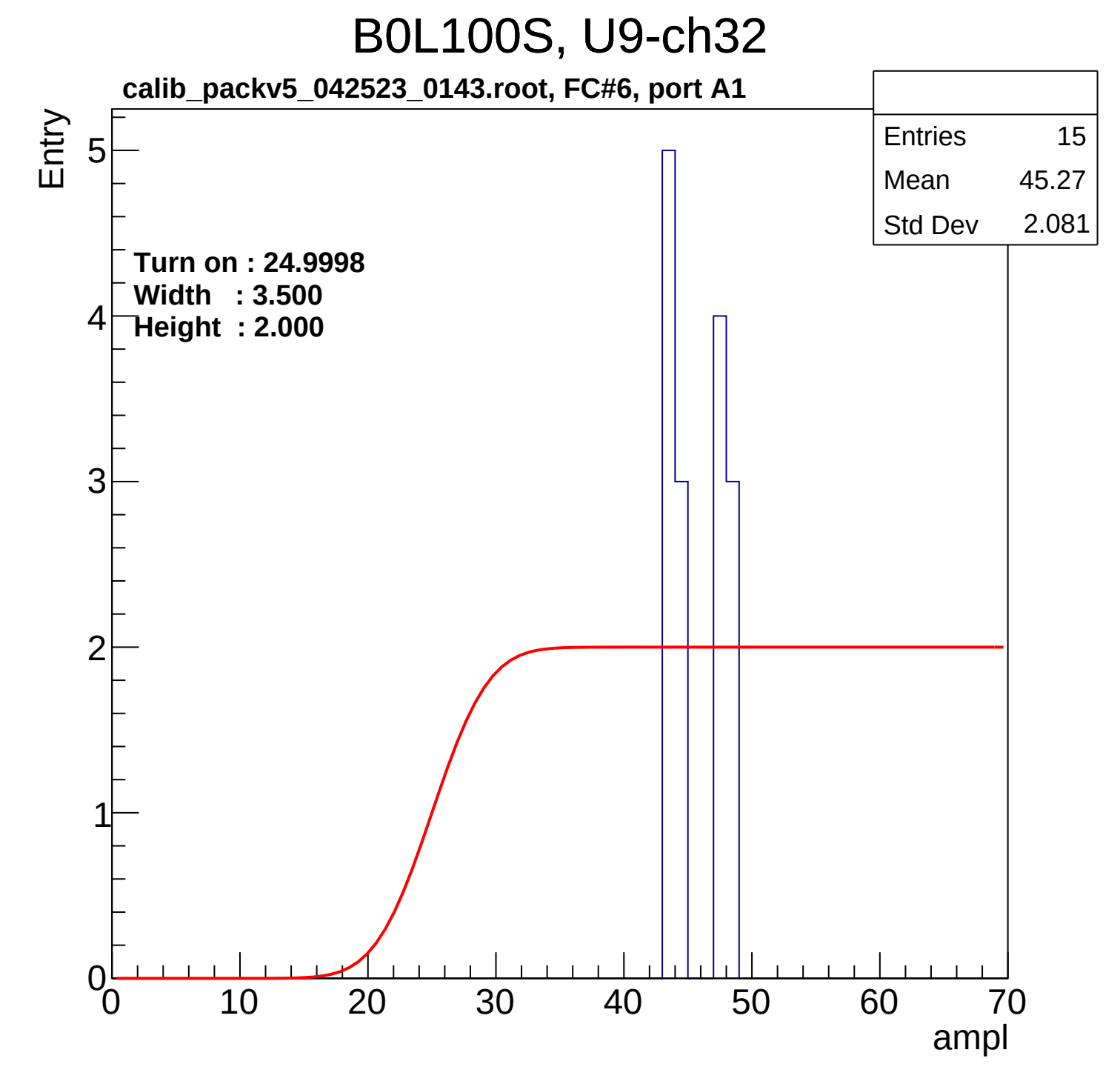
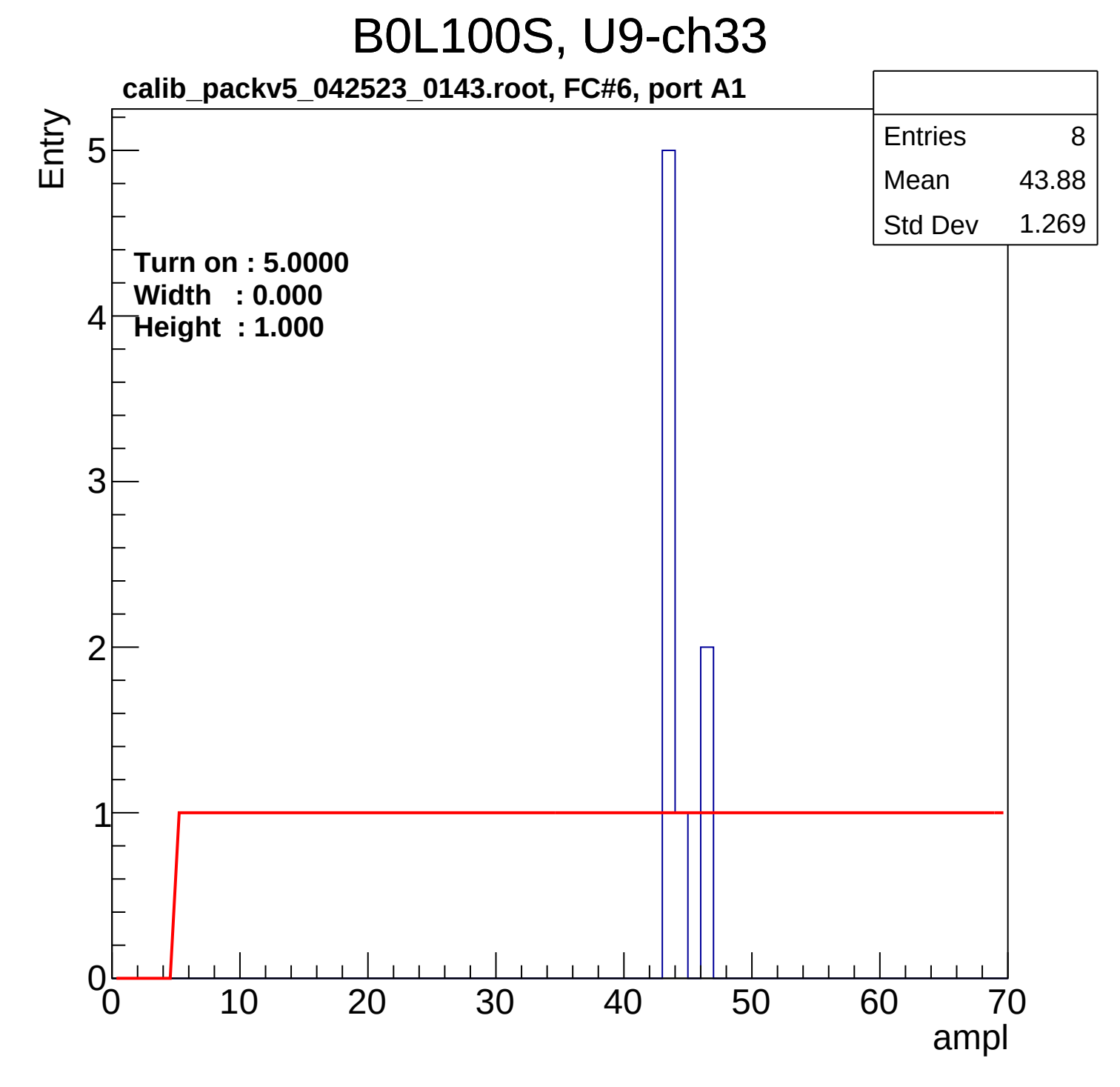

B0L100S, U9-ch31
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U9-ch32
calib_packv5_042523_0143.root, FC#6, port A1
Entries 15
Mean 45.27
Std Dev 2.081
Turn on : 24.9998
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B0L100S, U9-ch33
calib_packv5_042523_0143.root, FC#6, port A1
Entries 8
Mean 43.88
Std Dev 1.269
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
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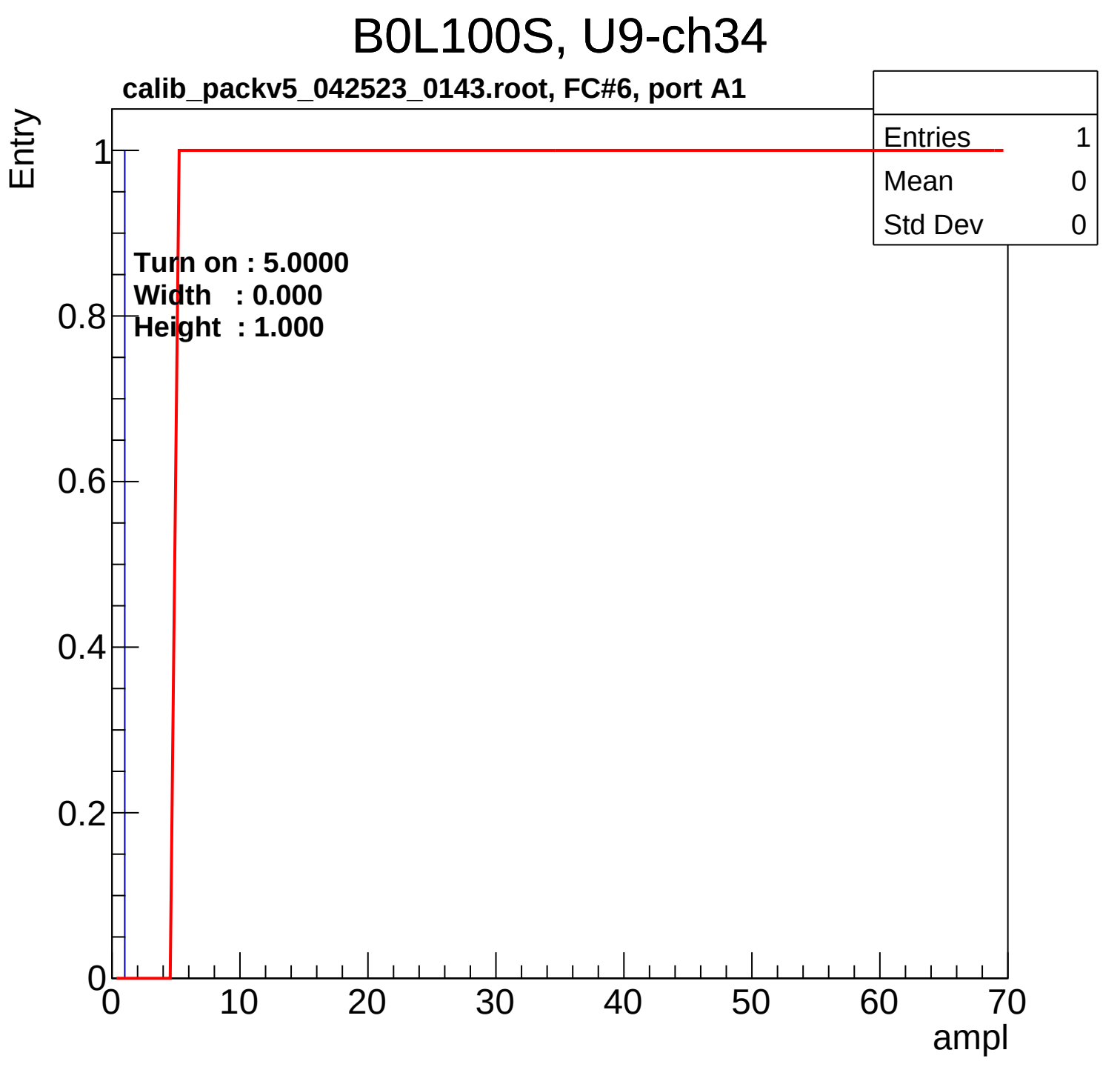
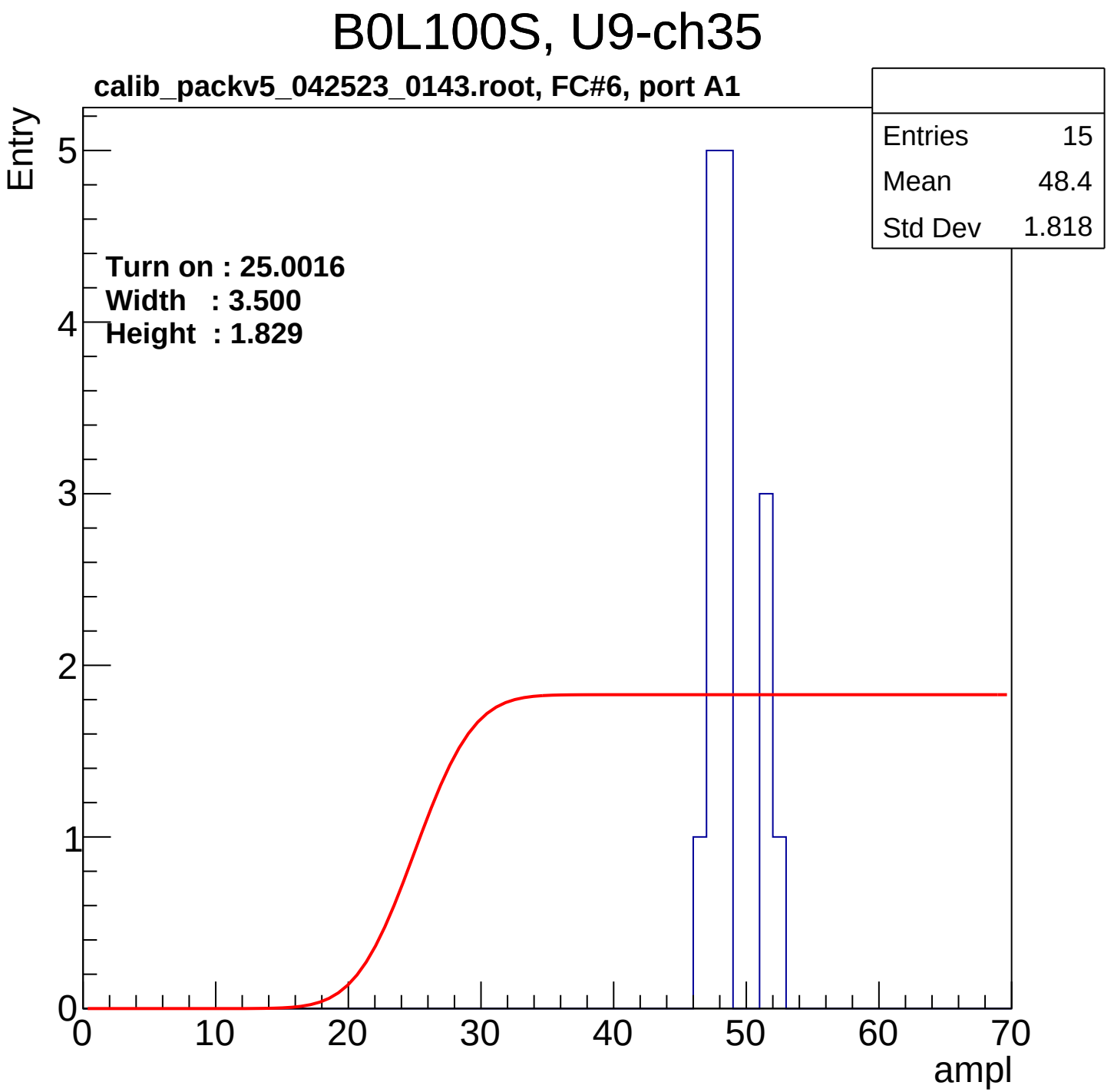

B0L100S, U9-ch34
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U9-ch35
calib_packv5_042523_0143.root, FC#6, port A1
Entries 15
Mean 48.4
Std Dev 1.818
Turn on : 25.0016
Width : 3.500
Height : 1.829
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
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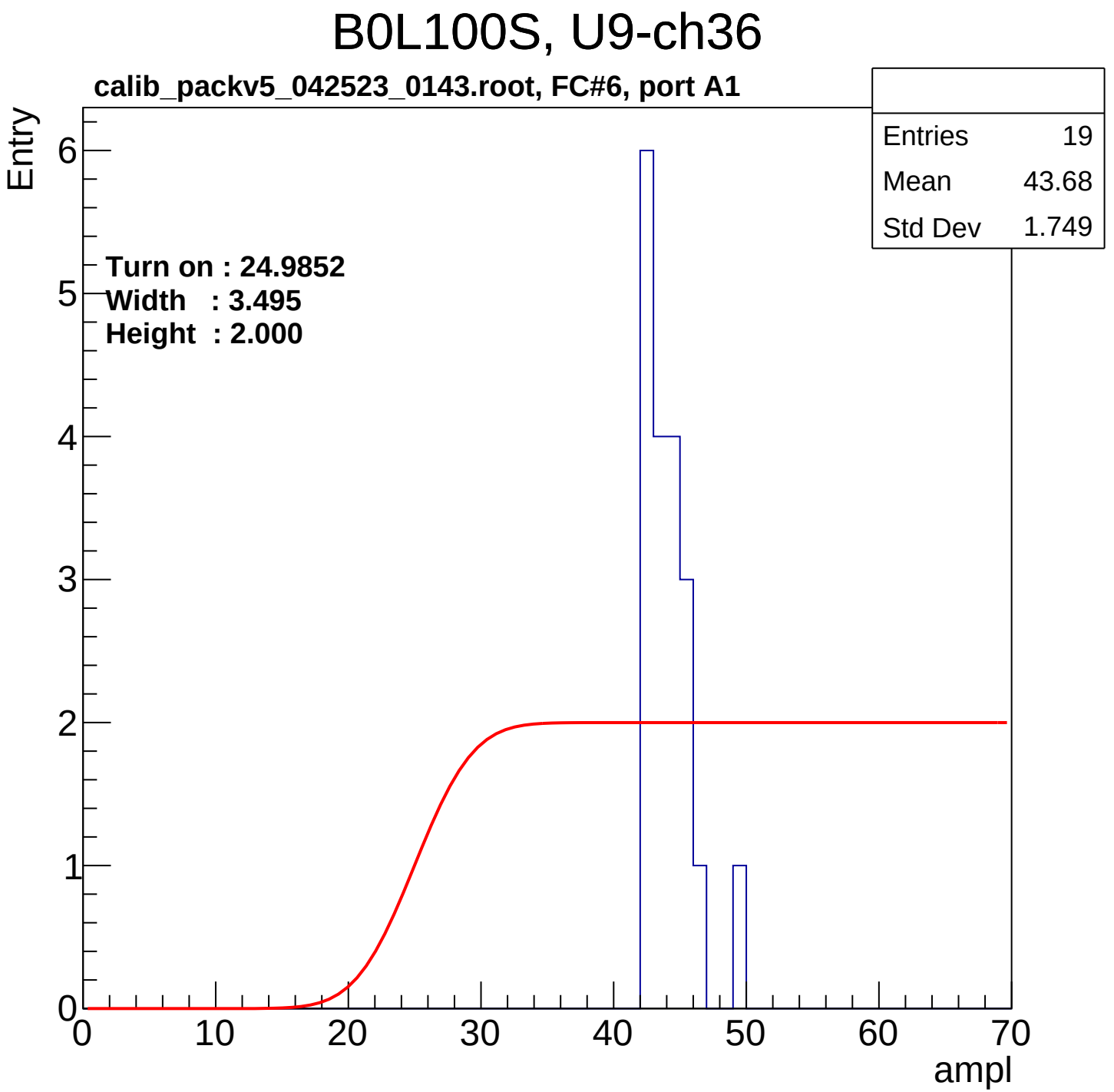
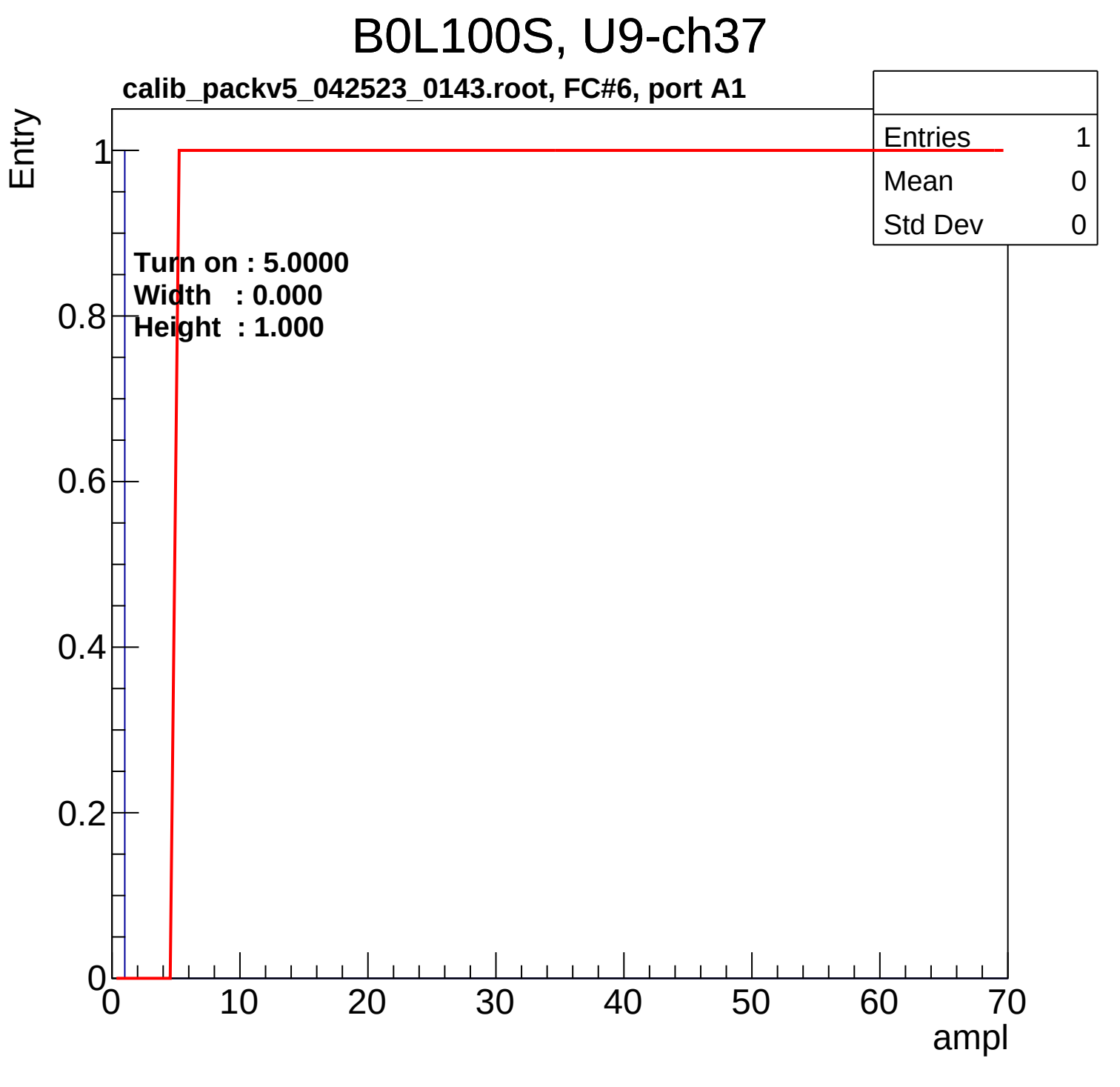
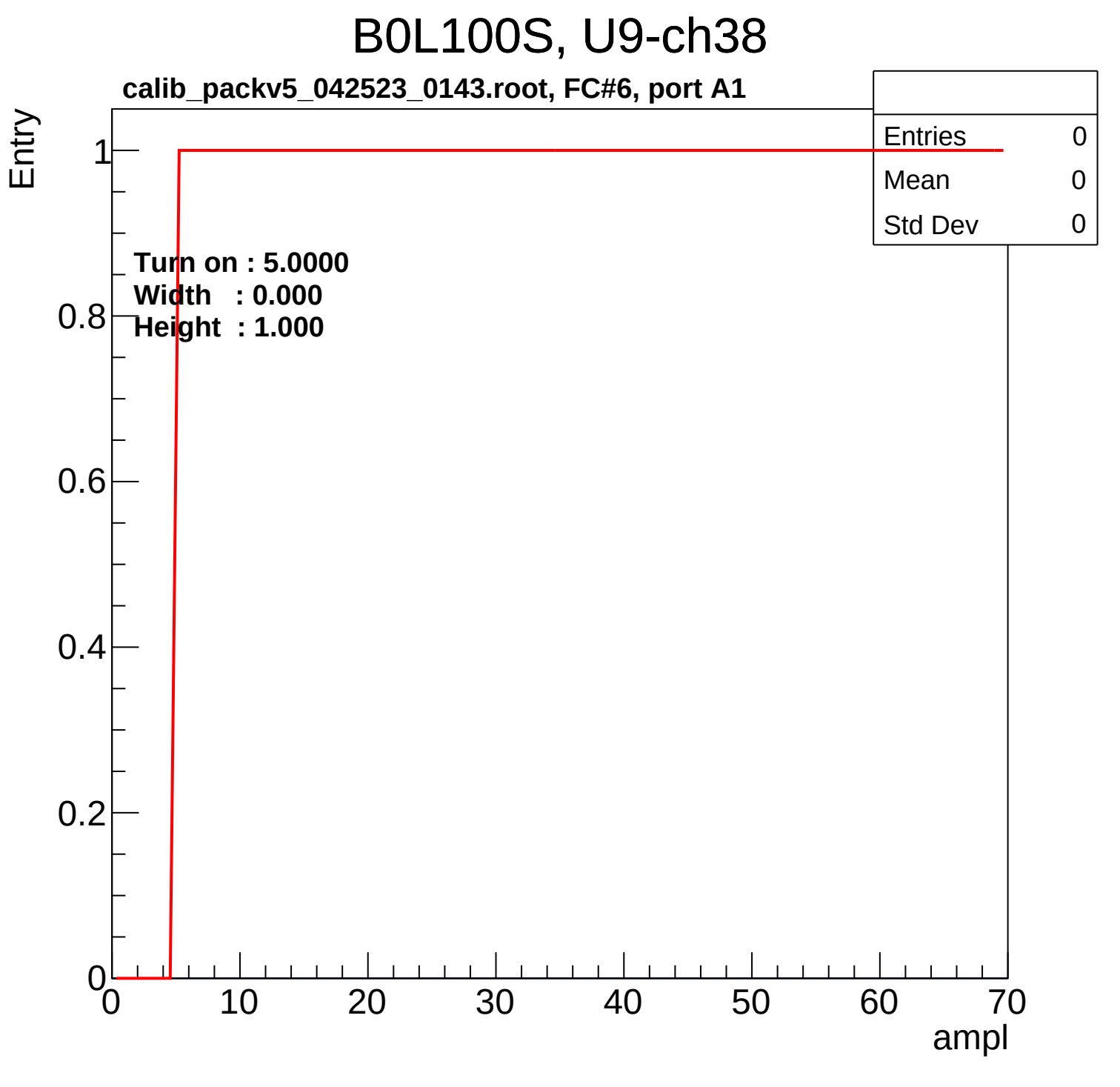
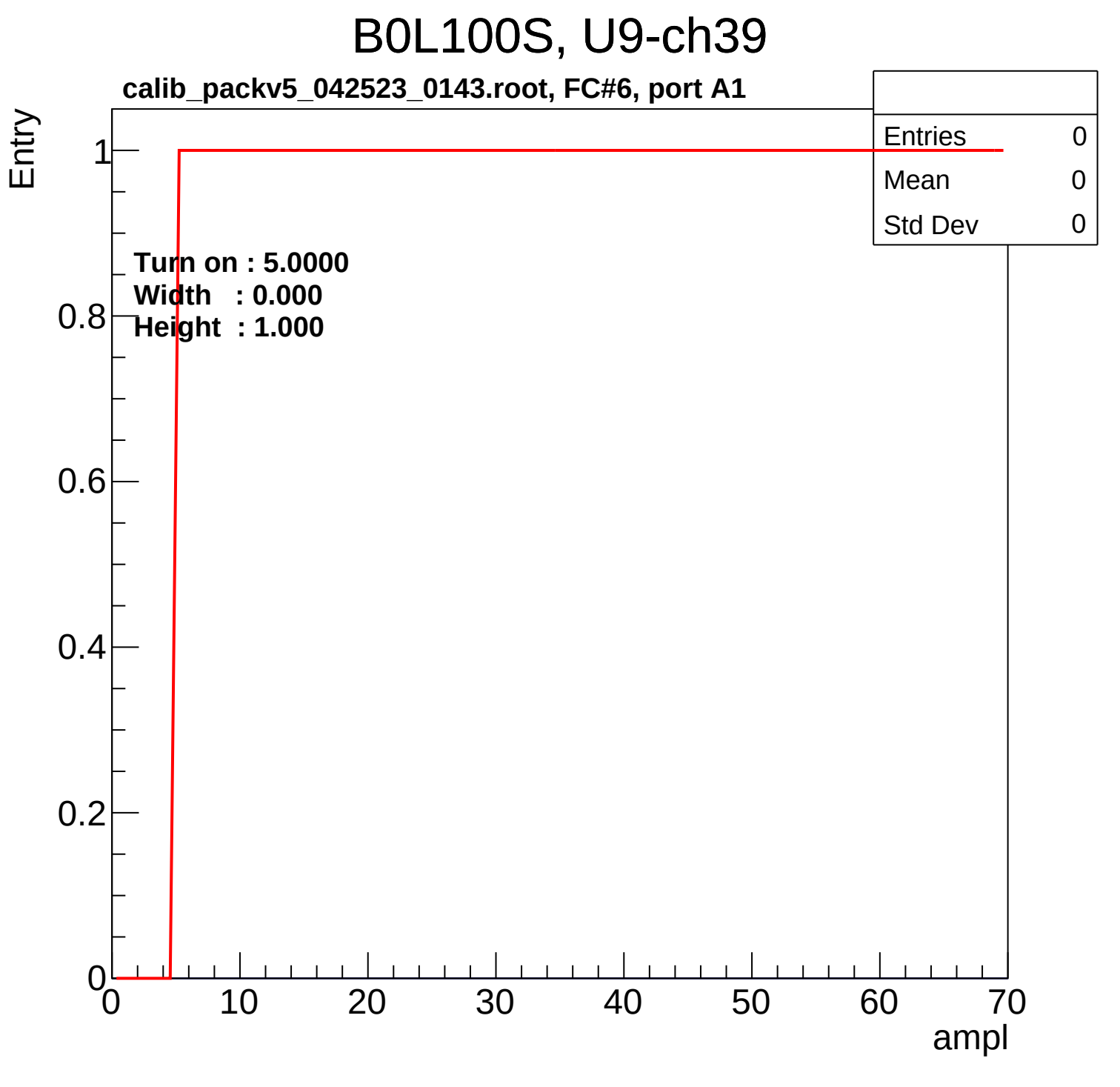
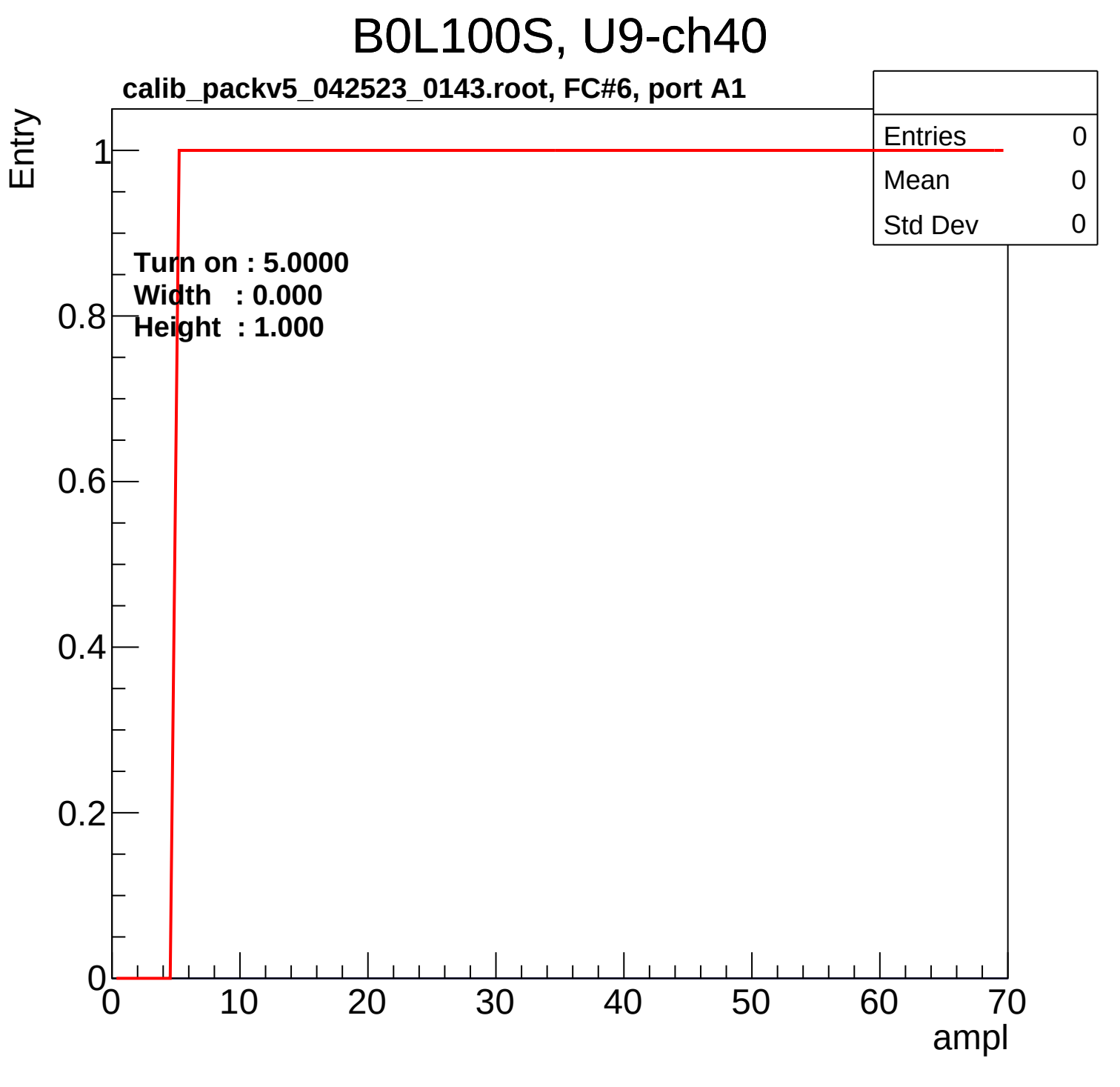
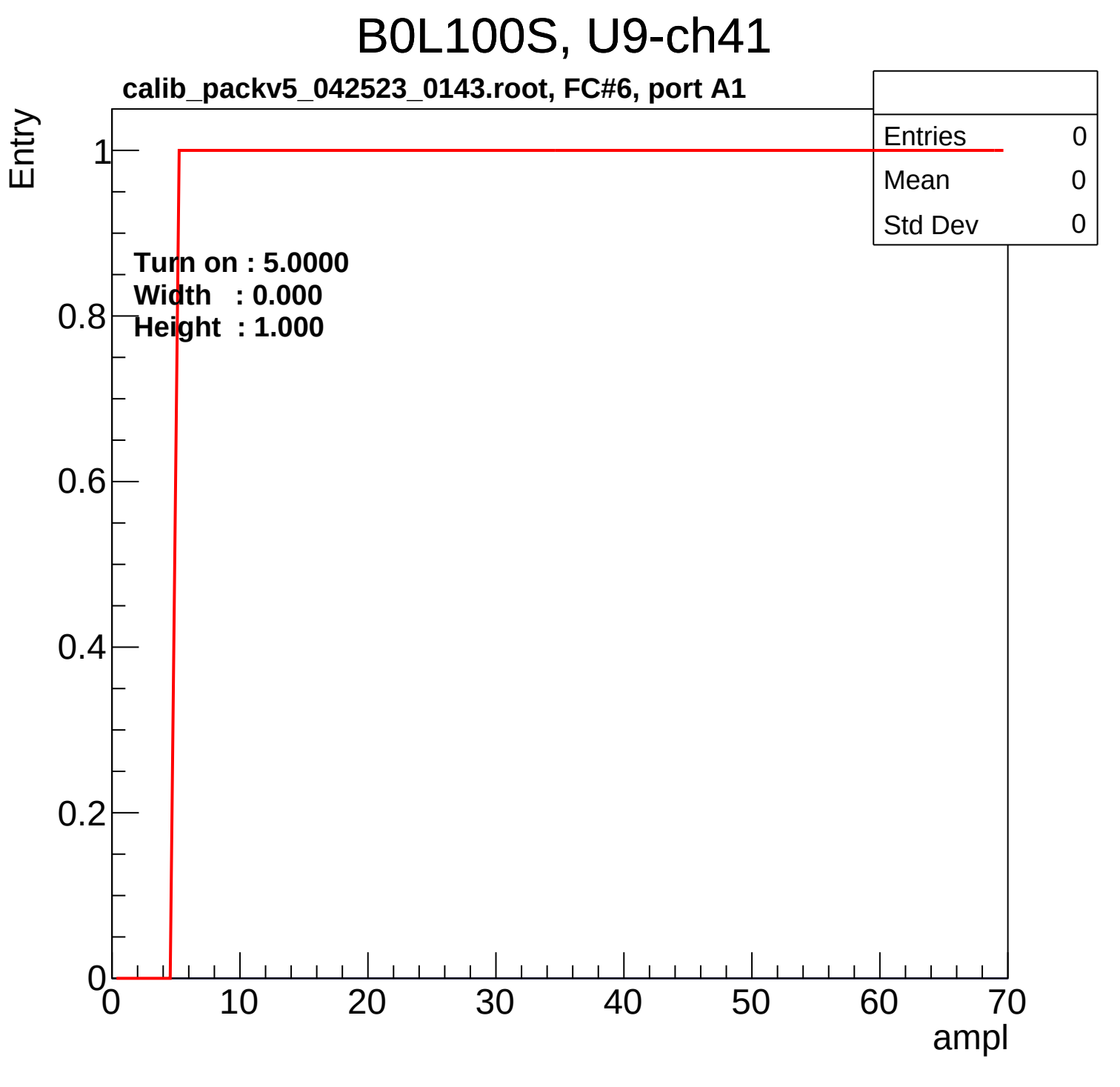

B0L100S, U9-ch36
calib_packv5_042523_0143.root, FC#6, port A1
Entries 19
Mean 43.68
Std Dev 1.749
Turn on : 24.9852
Width : 3.495
Height : 2.000
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

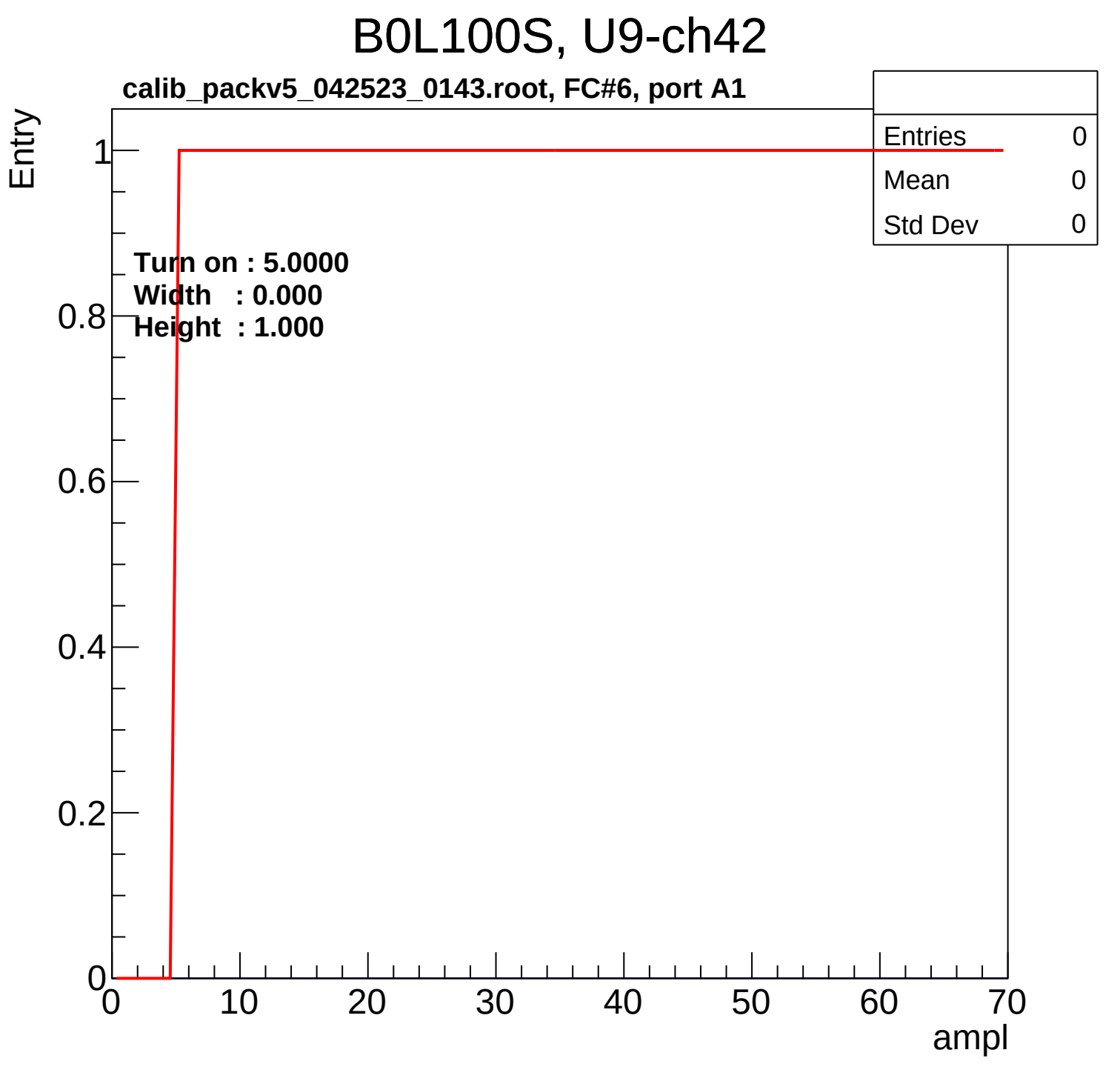

B0L100S, U9-ch37
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

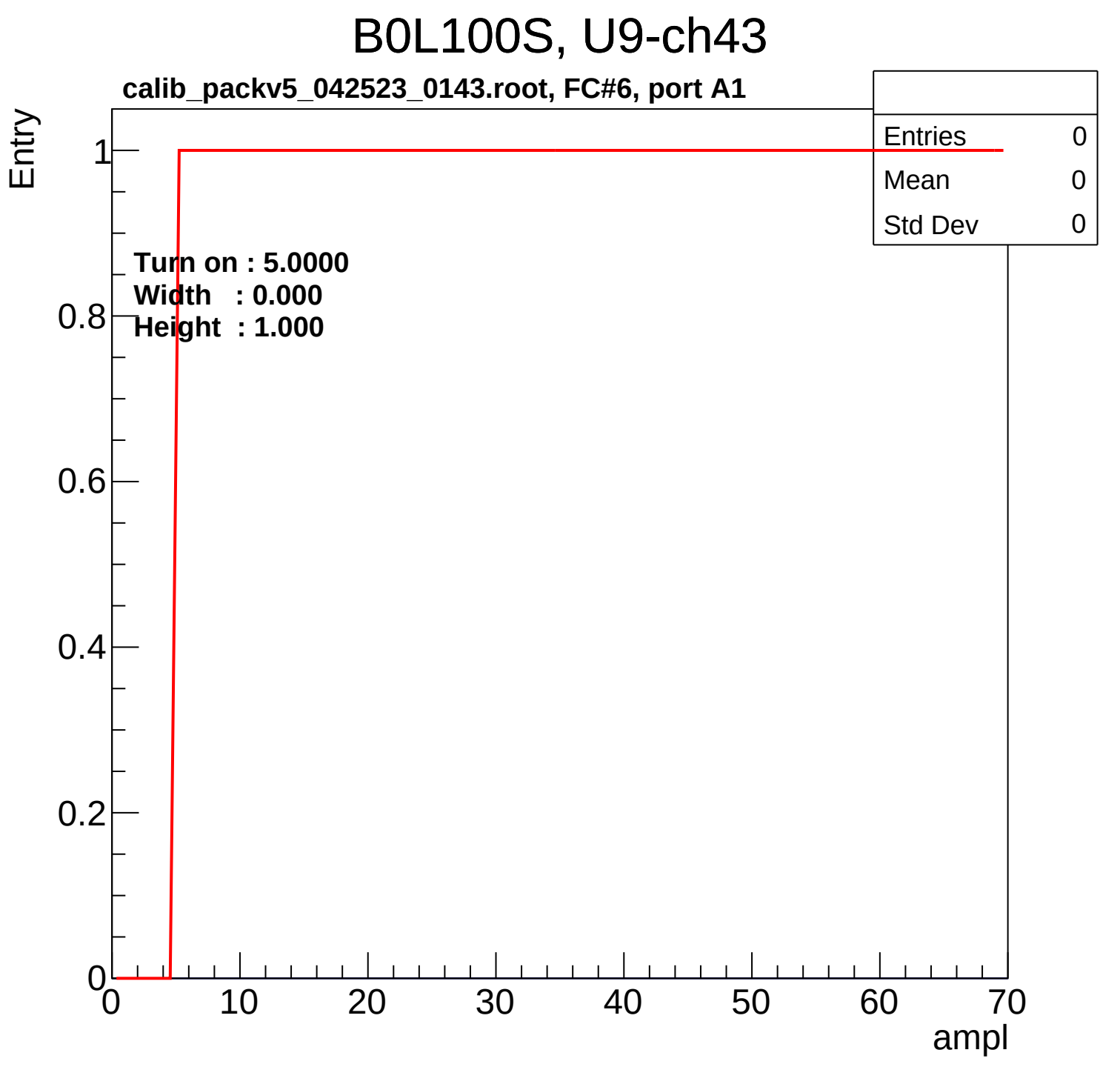

B0L100S, U9-ch38
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

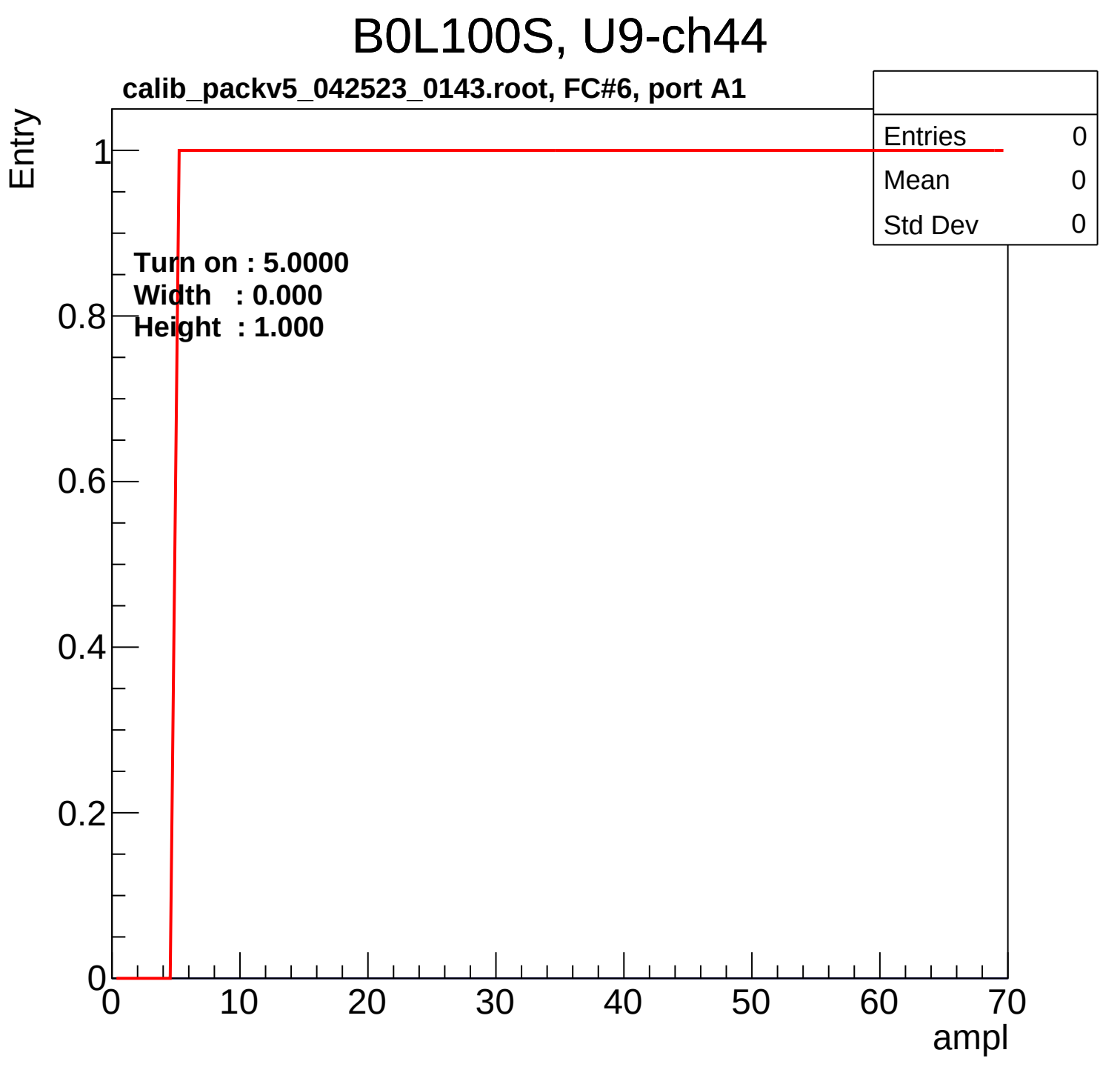

B0L100S, U9-ch39
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

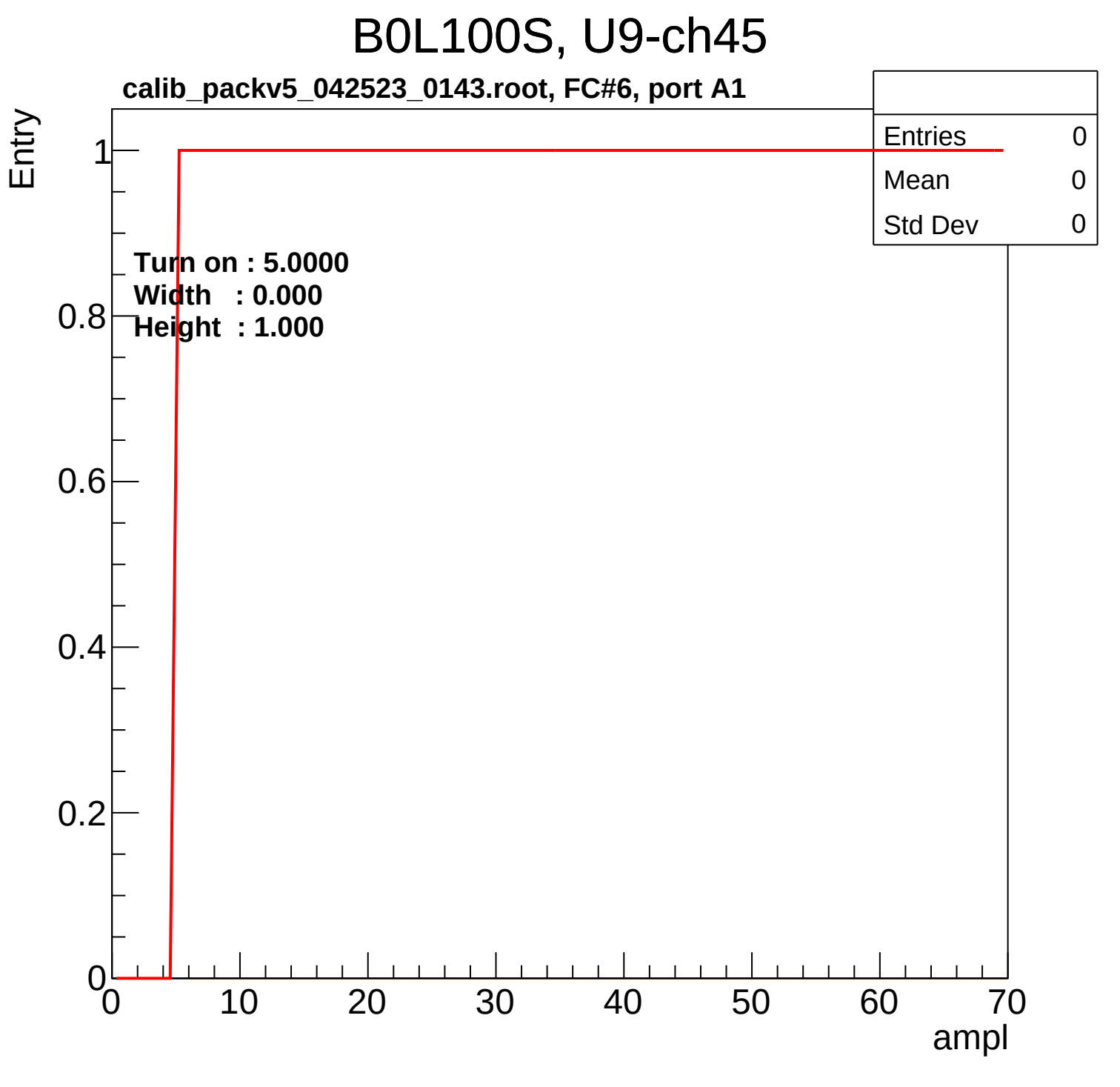

B0L100S, U9-ch40
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

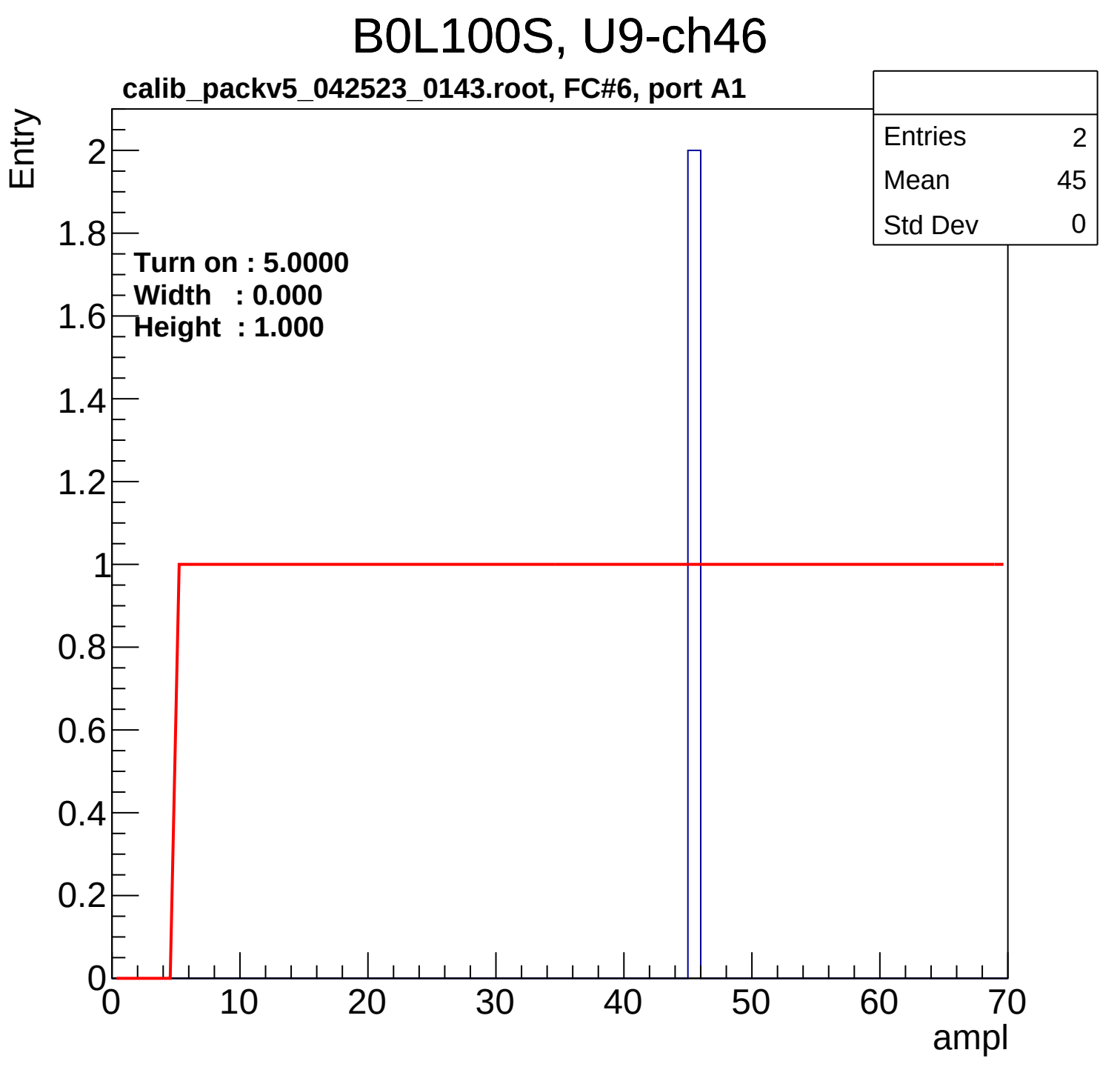

B0L100S, U9-ch41
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

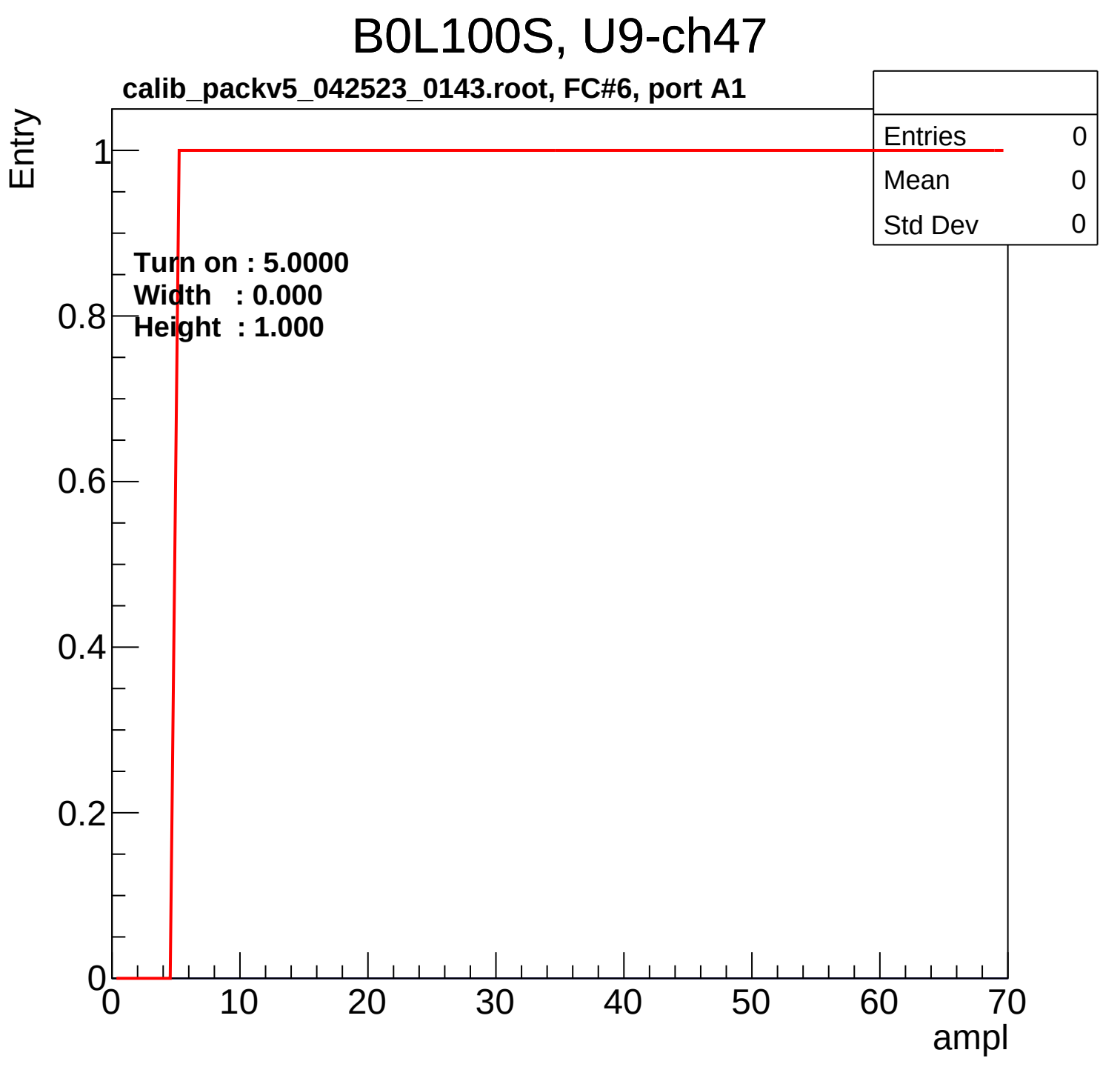

B0L100S, U9-ch42
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

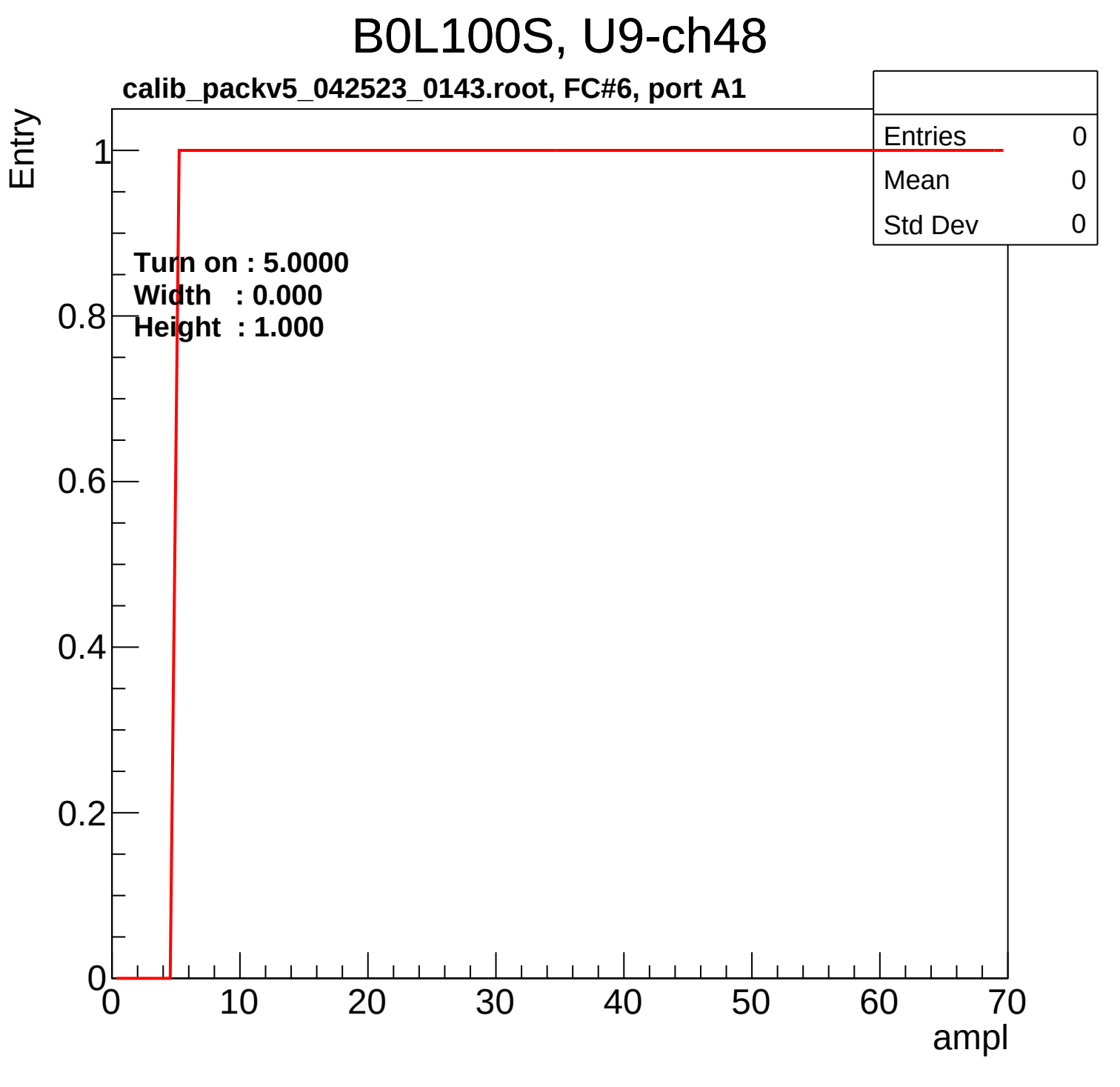

B0L100S, U9-ch43
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

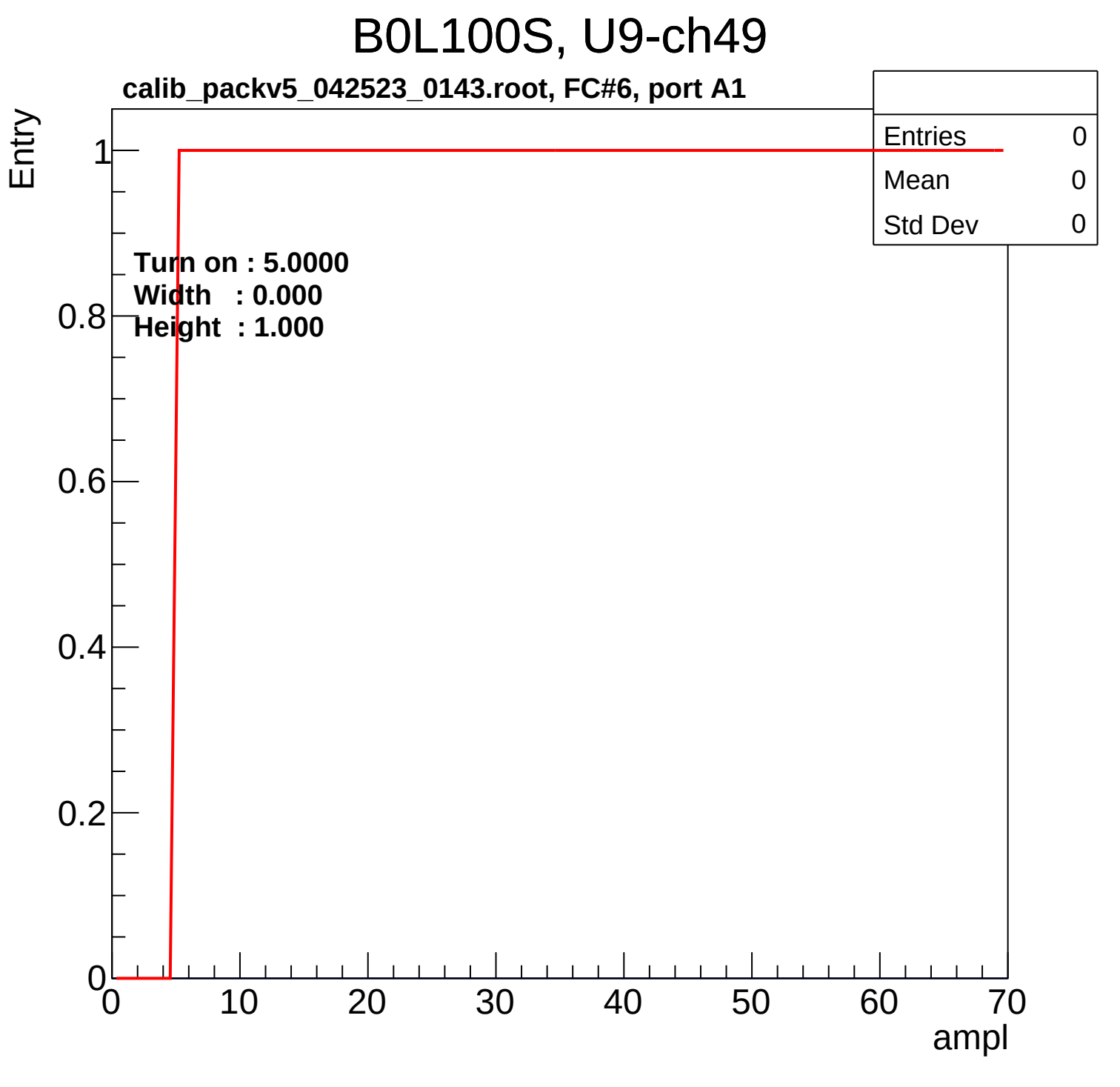

B0L100S, U9-ch44
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

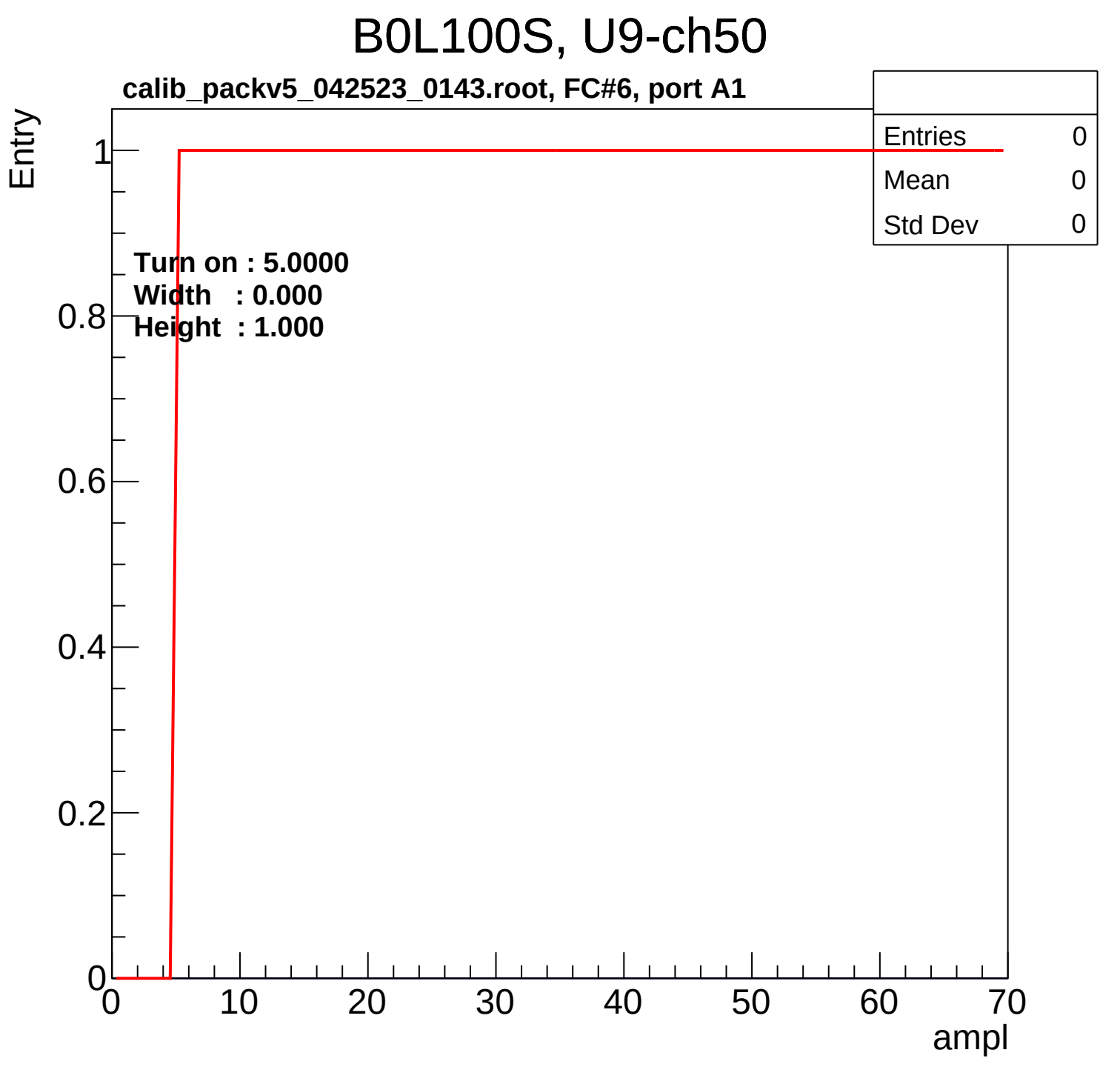

B0L100S, U9-ch45
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

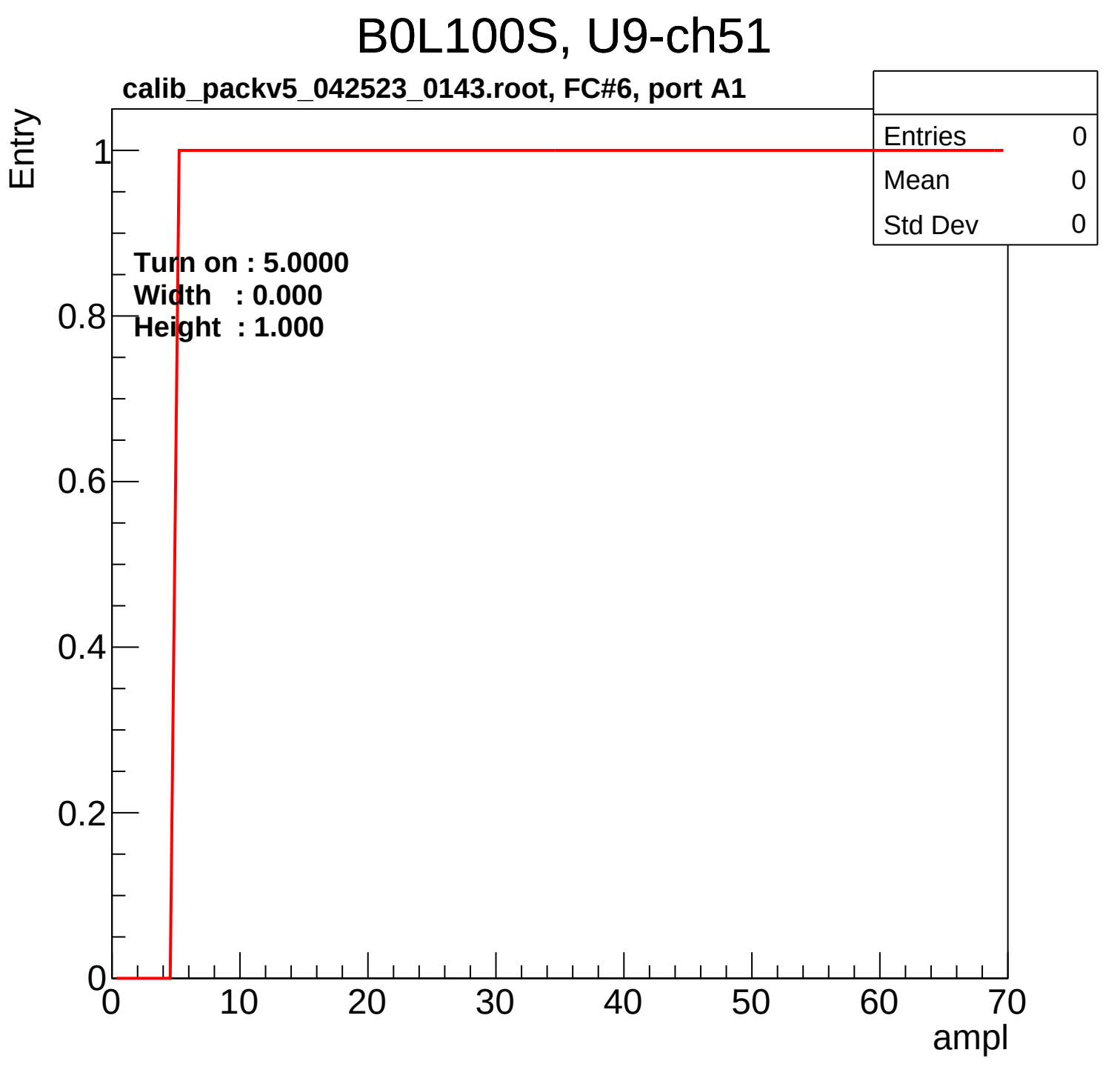

B0L100S, U9-ch46
calib_packv5_042523_0143.root, FC#6, port A1
Entries 2
Mean 45
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

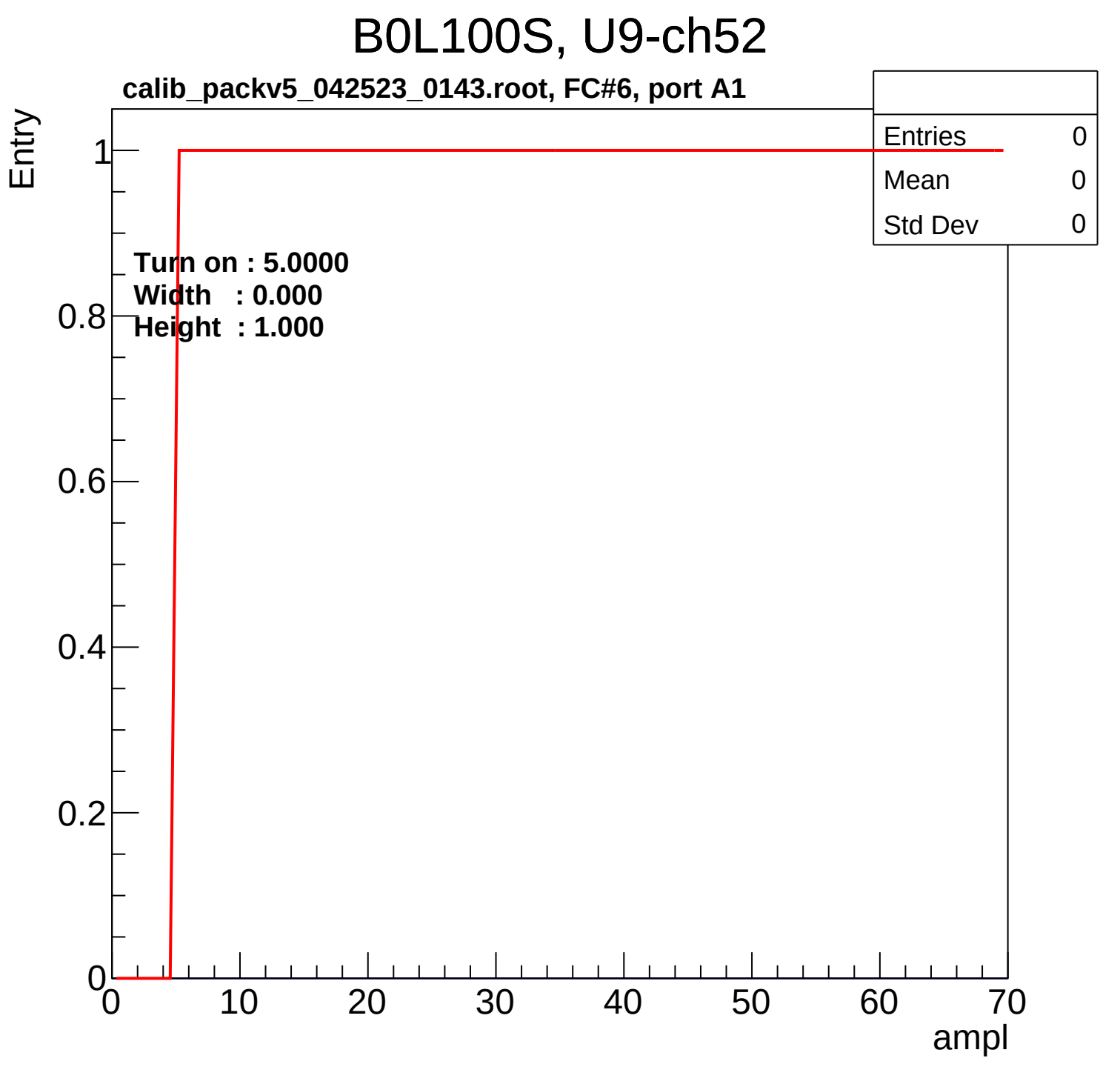

B0L100S, U9-ch47
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U9-ch48
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U9-ch49
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U9-ch50
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U9-ch51
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U9-ch52
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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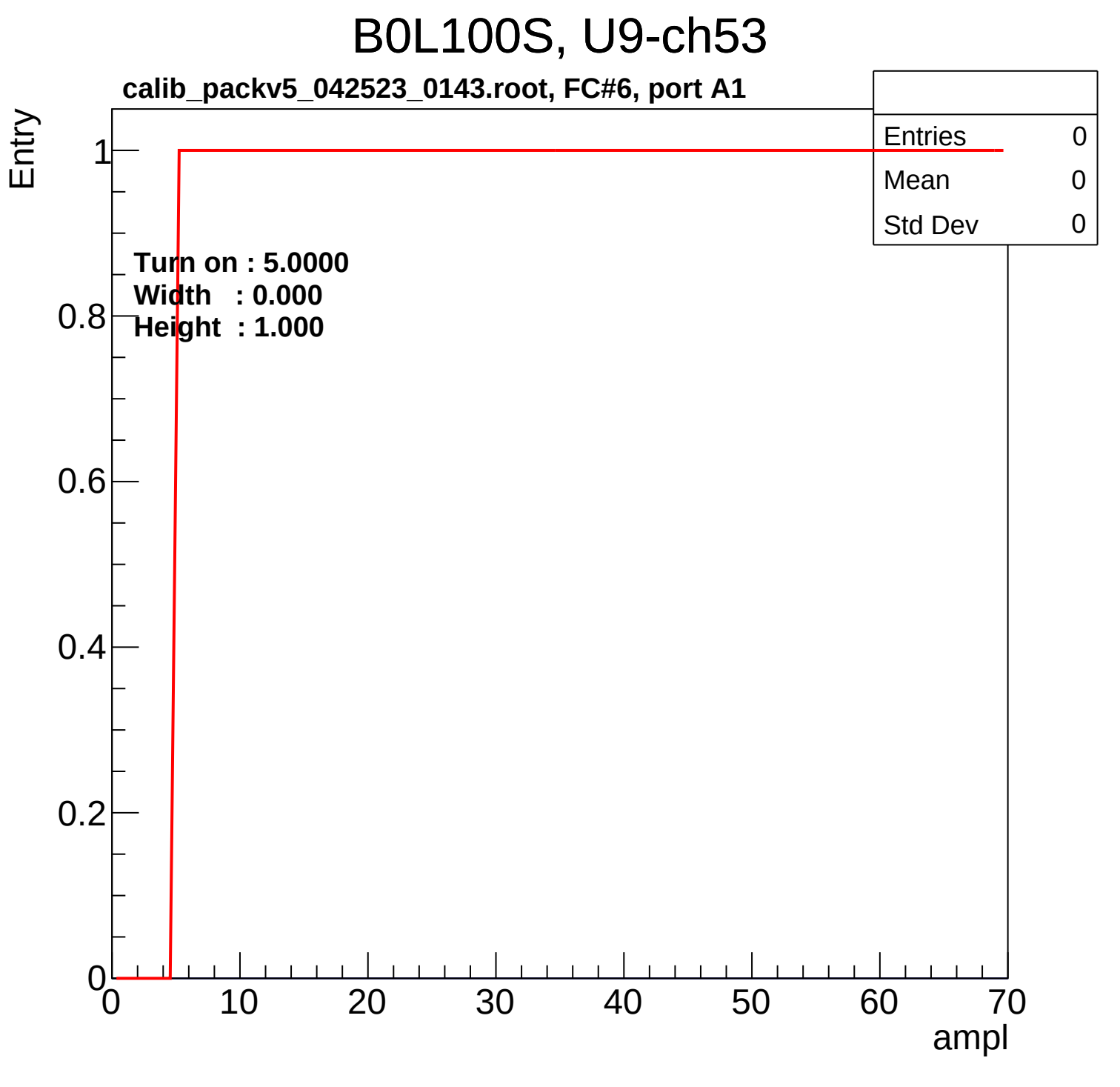
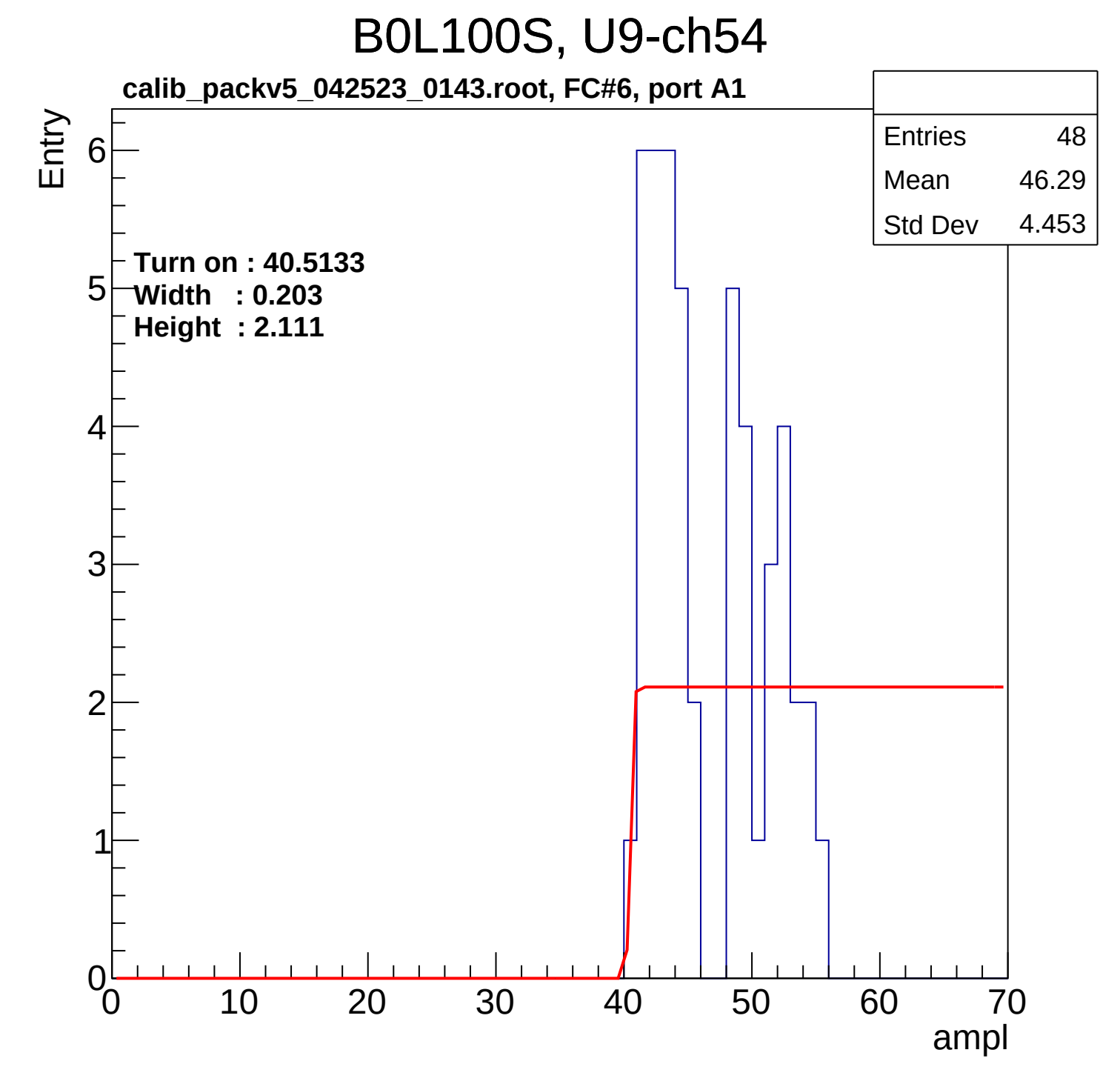
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U9-ch53
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U9-ch54
calib_packv5_042523_0143.root, FC#6, port A1
Entries 48
Mean 46.29
Std Dev 4.453
Turn on : 40.5133
Width : 0.203
Height : 2.111
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
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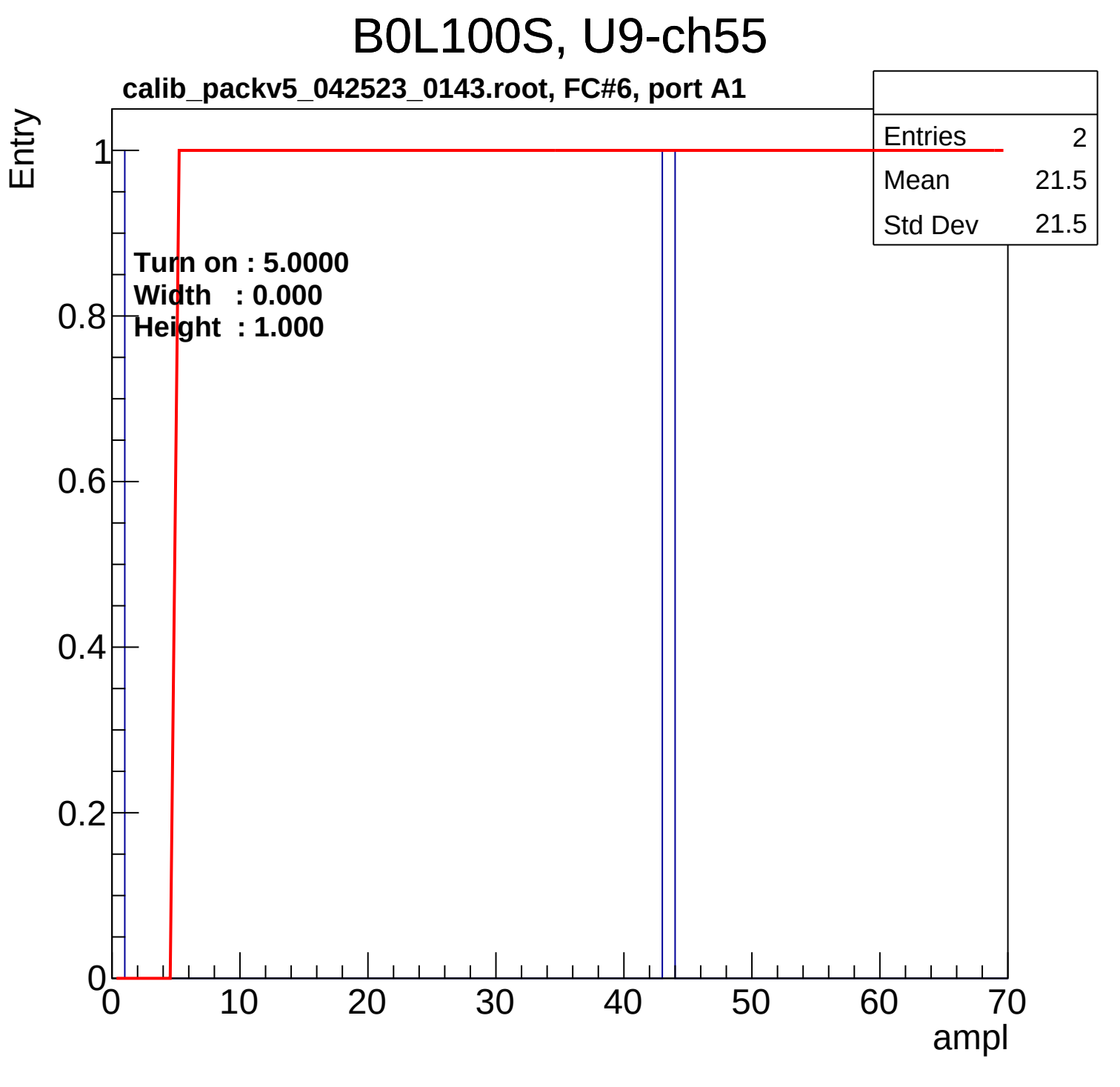
B0L100S, U9-ch55
calib_packv5_042523_0143.root, FC#6, port A1
Entries 2
Mean 21.5
Std Dev 21.5
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
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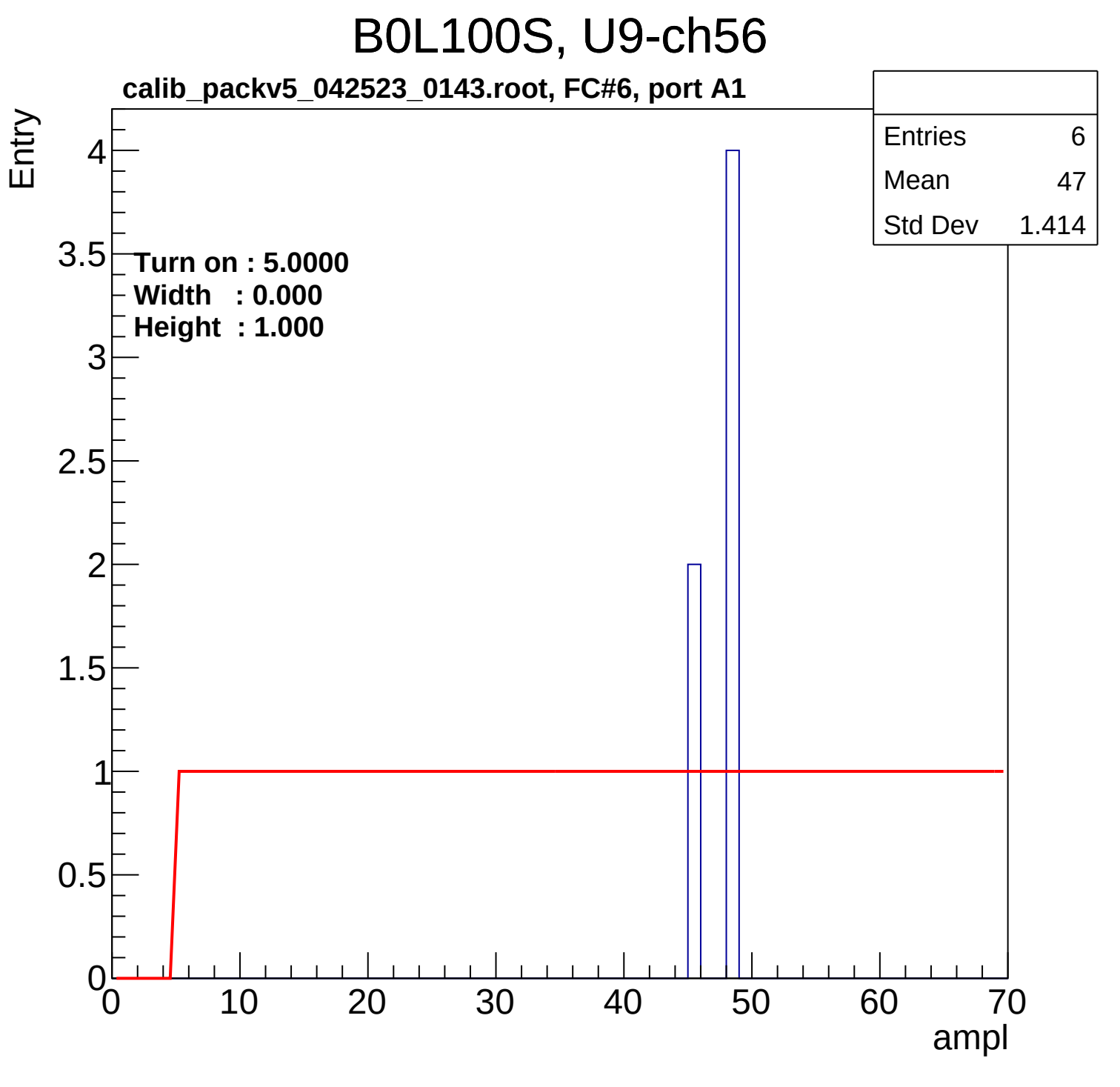
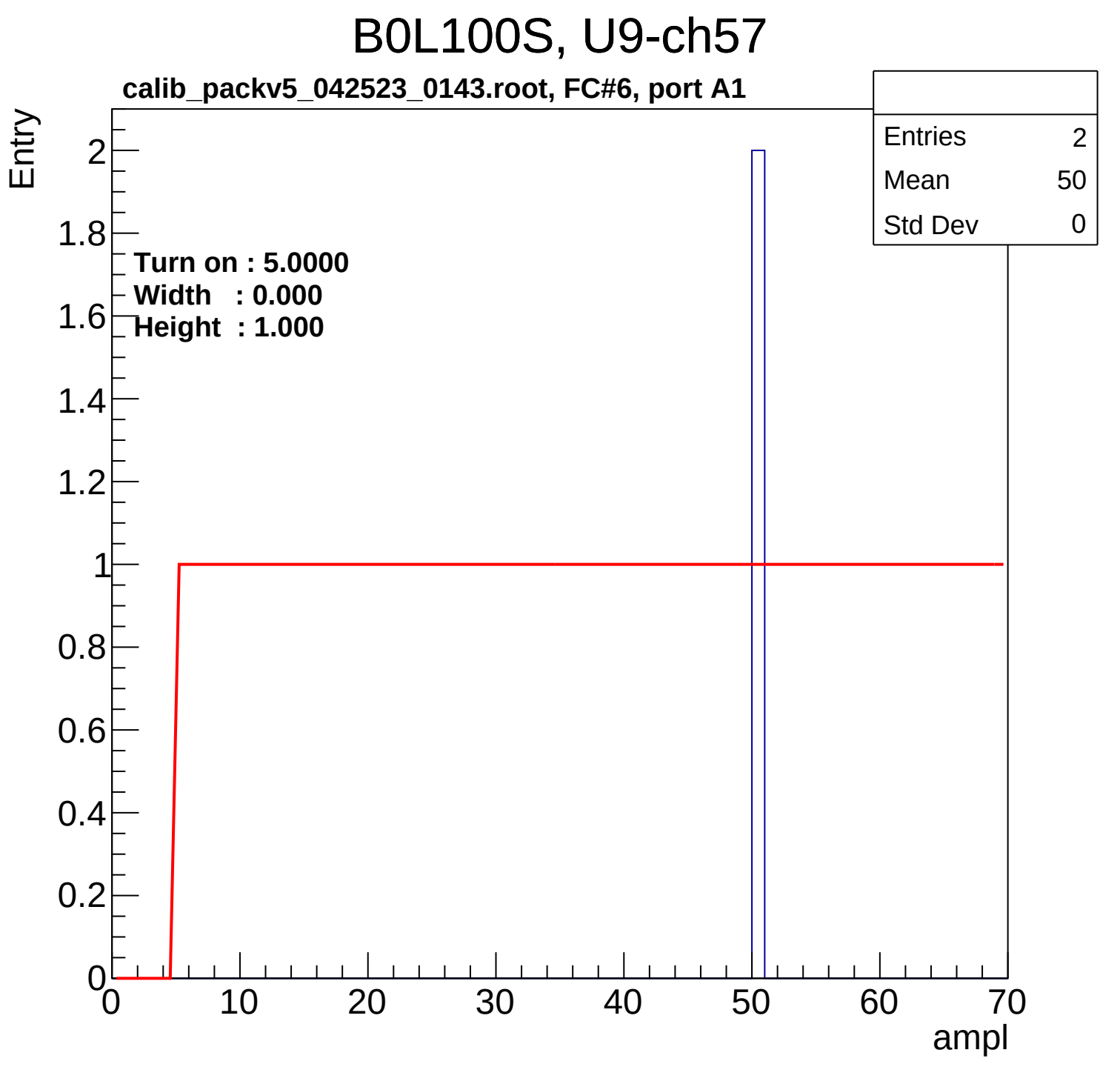
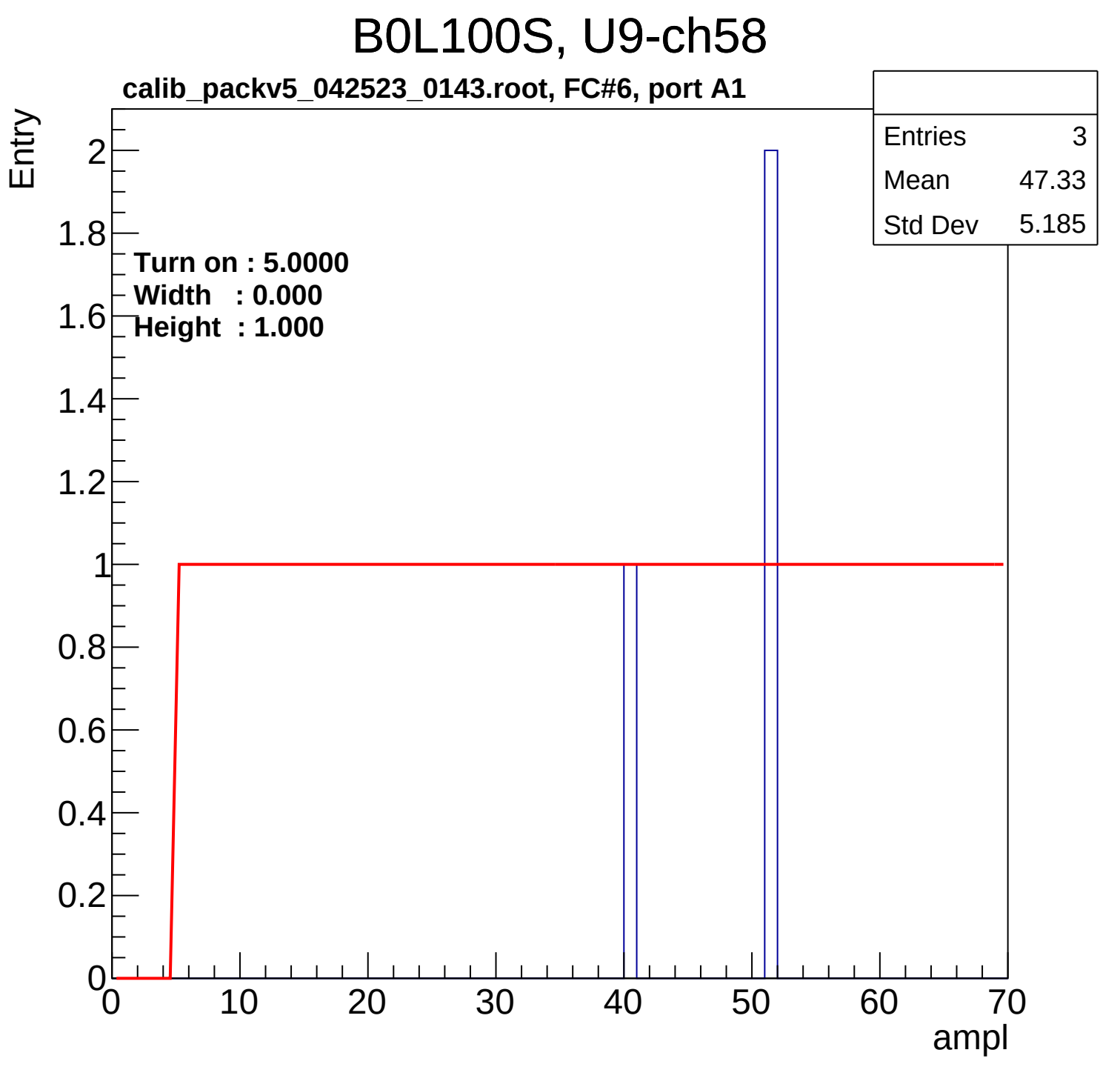

B0L100S, U9-ch56
calib_packv5_042523_0143.root, FC#6, port A1
Entries 6
Mean 47
Std Dev 1.414
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B0L100S, U9-ch57
calib_packv5_042523_0143.root, FC#6, port A1
Entries 2
Mean 50
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B0L100S, U9-ch58
calib_packv5_042523_0143.root, FC#6, port A1
Entries 3
Mean 47.33
Std Dev 5.185
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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60
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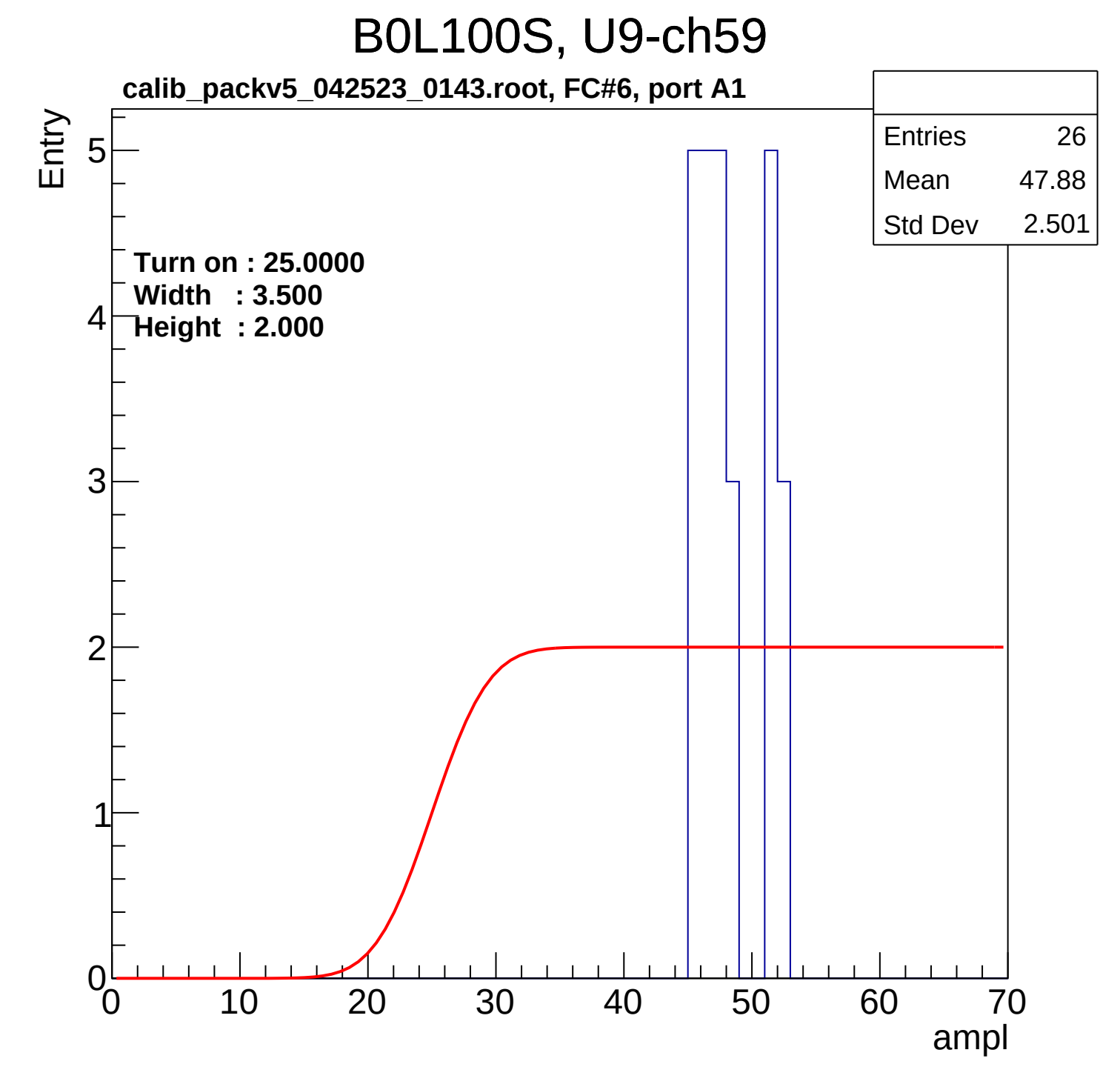
B0L100S, U9-ch59
calib_packv5_042523_0143.root, FC#6, port A1
Entries 26
Mean 47.88
Std Dev 2.501
Turn on : 25.0000
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
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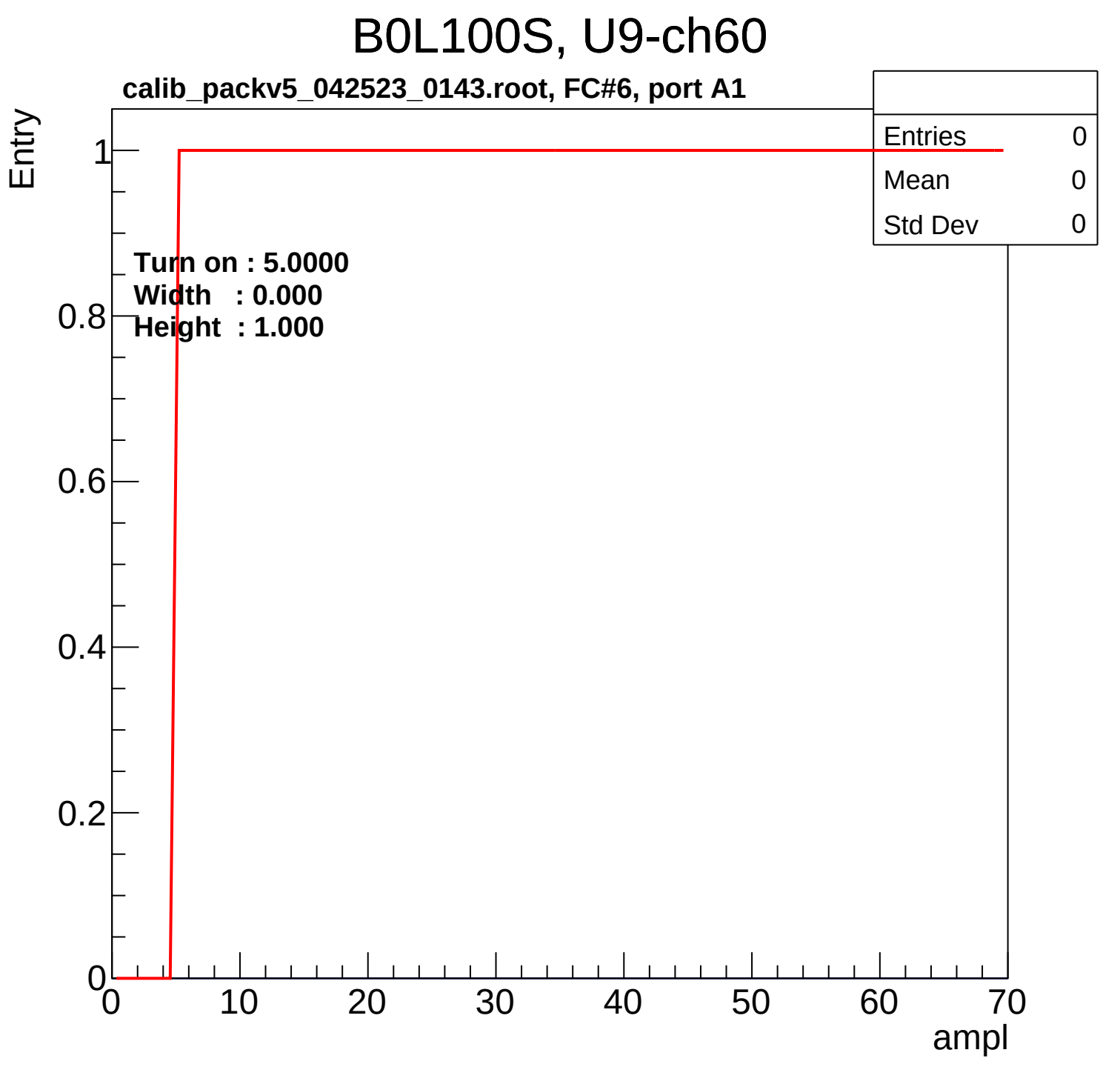
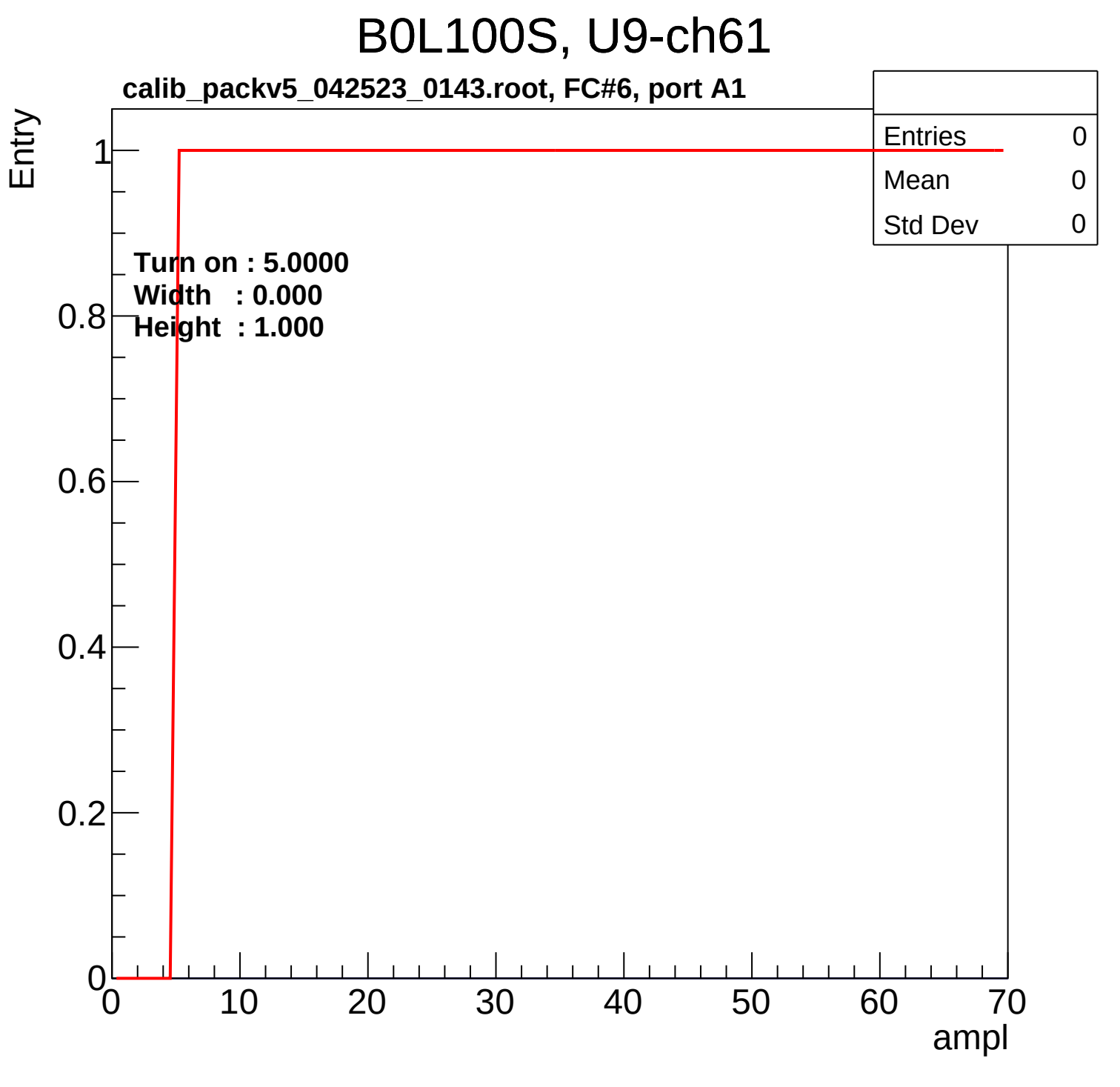
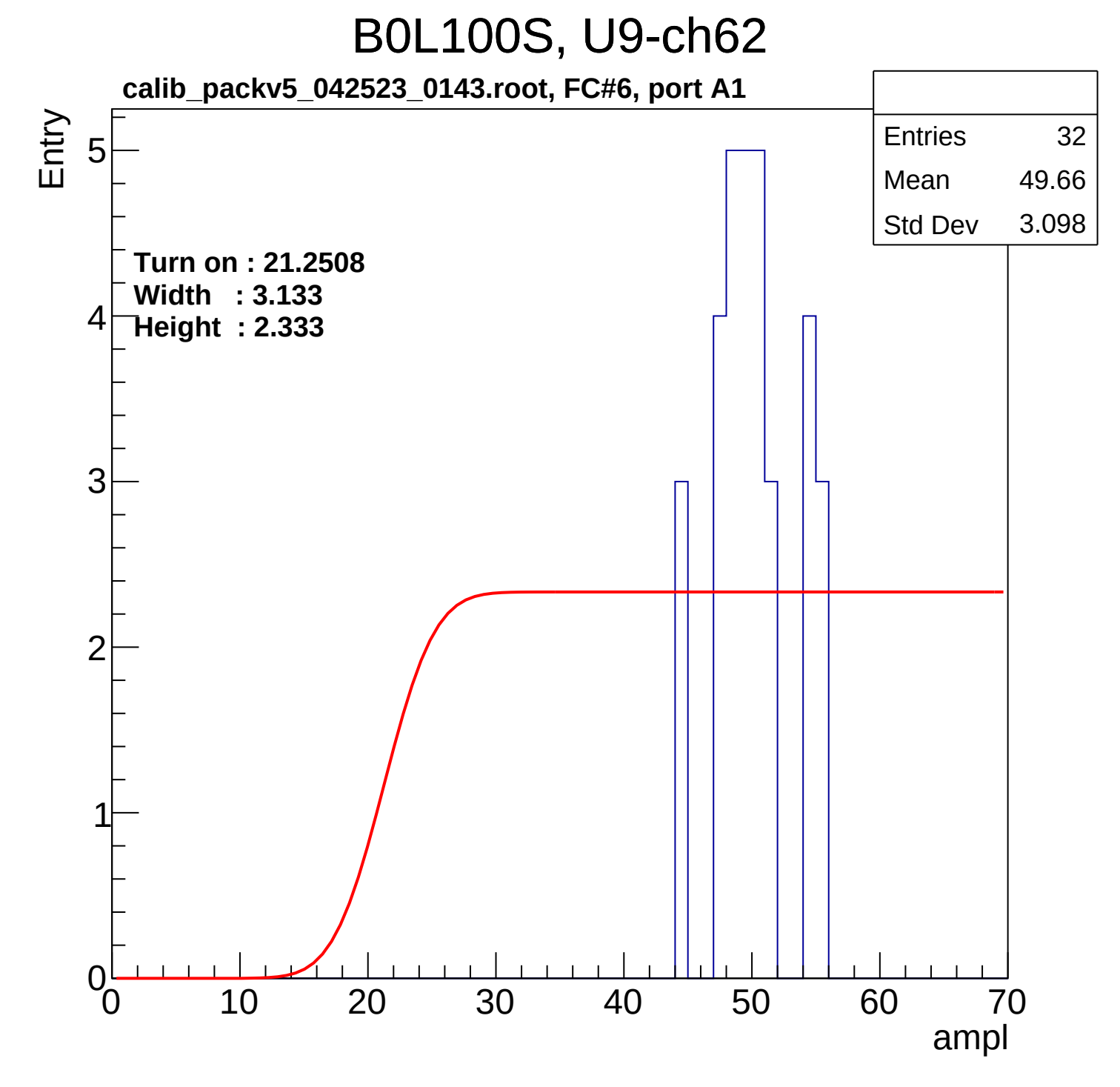

B0L100S, U9-ch60
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U9-ch61
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U9-ch62
calib_packv5_042523_0143.root, FC#6, port A1
Entries 32
Mean 49.66
Std Dev 3.098
Turn on : 21.2508
Width : 3.133
Height : 2.333
Entry
ampl
0
1
2
3
4
5
0
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40
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60
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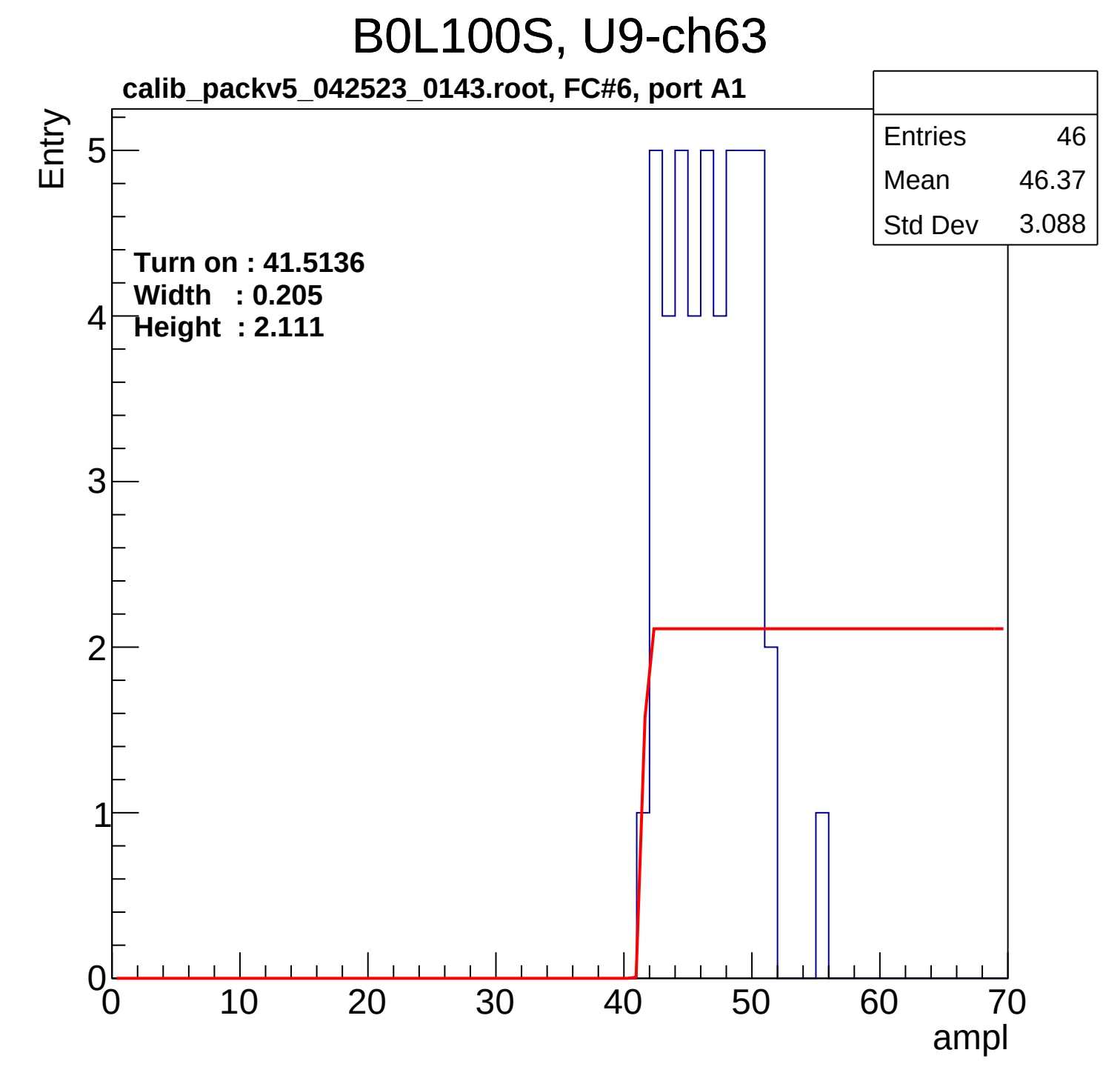
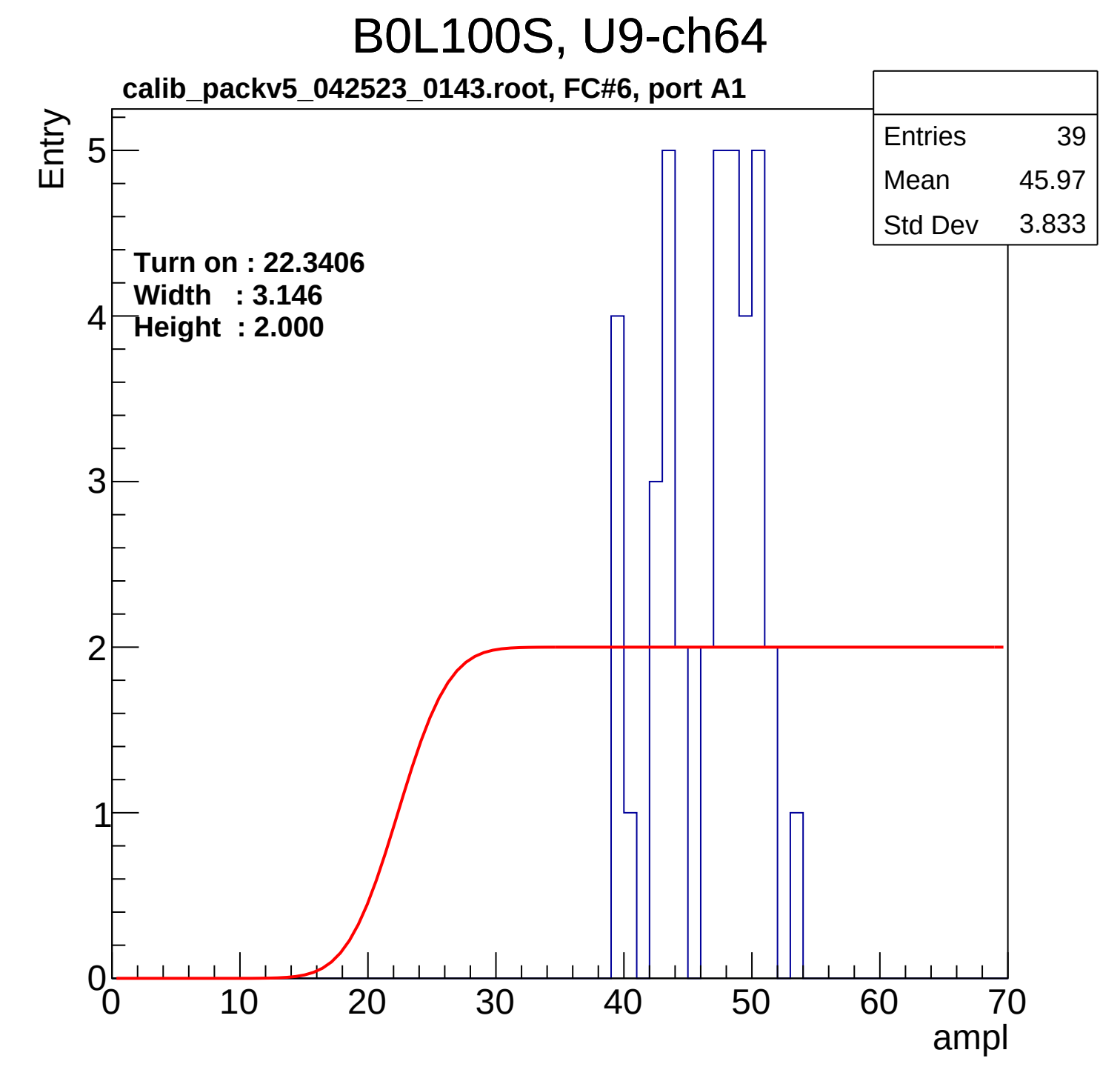

B0L100S, U9-ch63
calib_packv5_042523_0143.root, FC#6, port A1
Entries 46
Mean 46.37
Std Dev 3.088
Turn on : 41.5136
Width : 0.205
Height : 2.111
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B0L100S, U9-ch64
calib_packv5_042523_0143.root, FC#6, port A1
Entries 39
Mean 45.97
Std Dev 3.833
Turn on : 22.3406
Width : 3.146
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
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20
30
40
50
60
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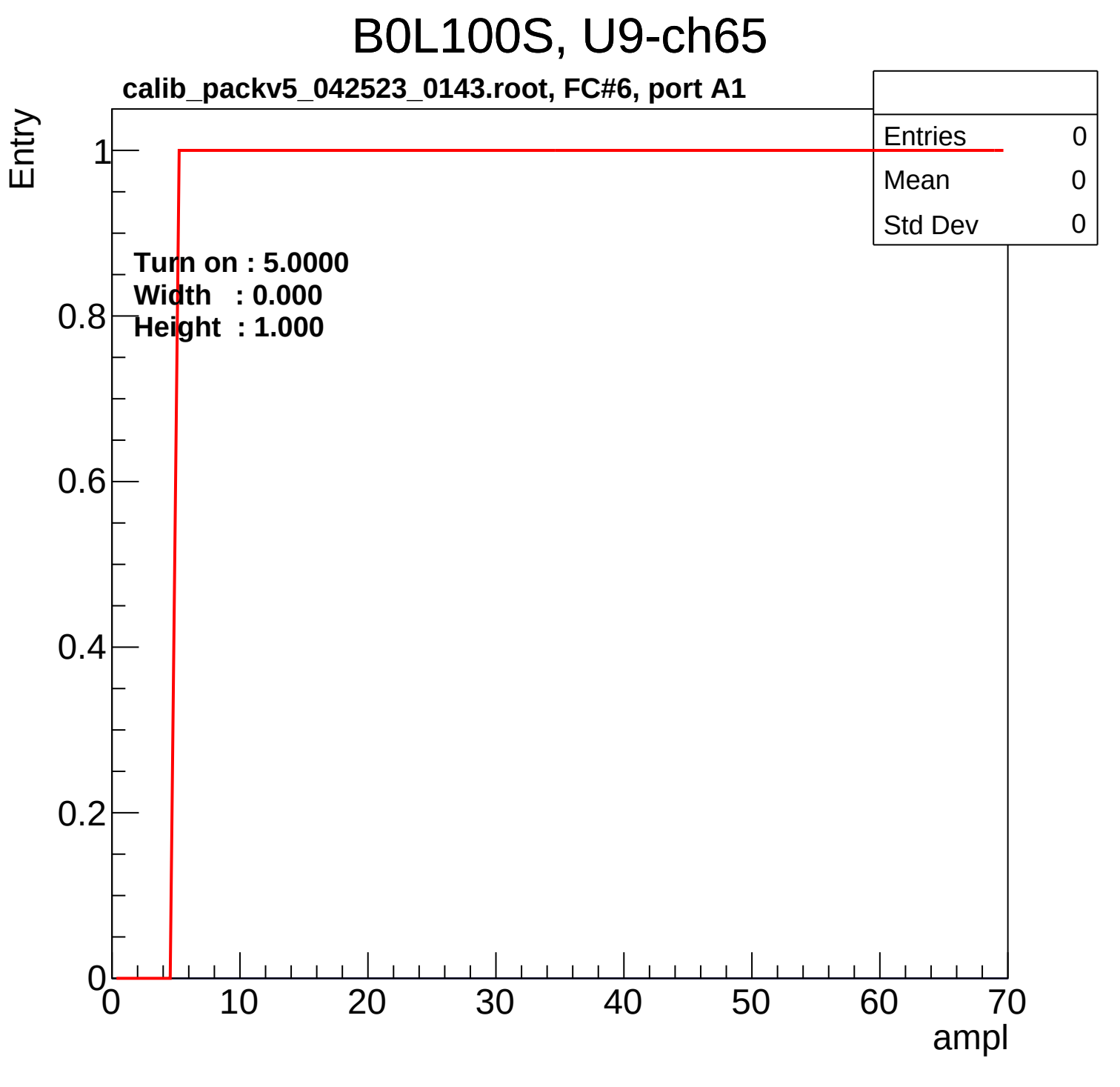
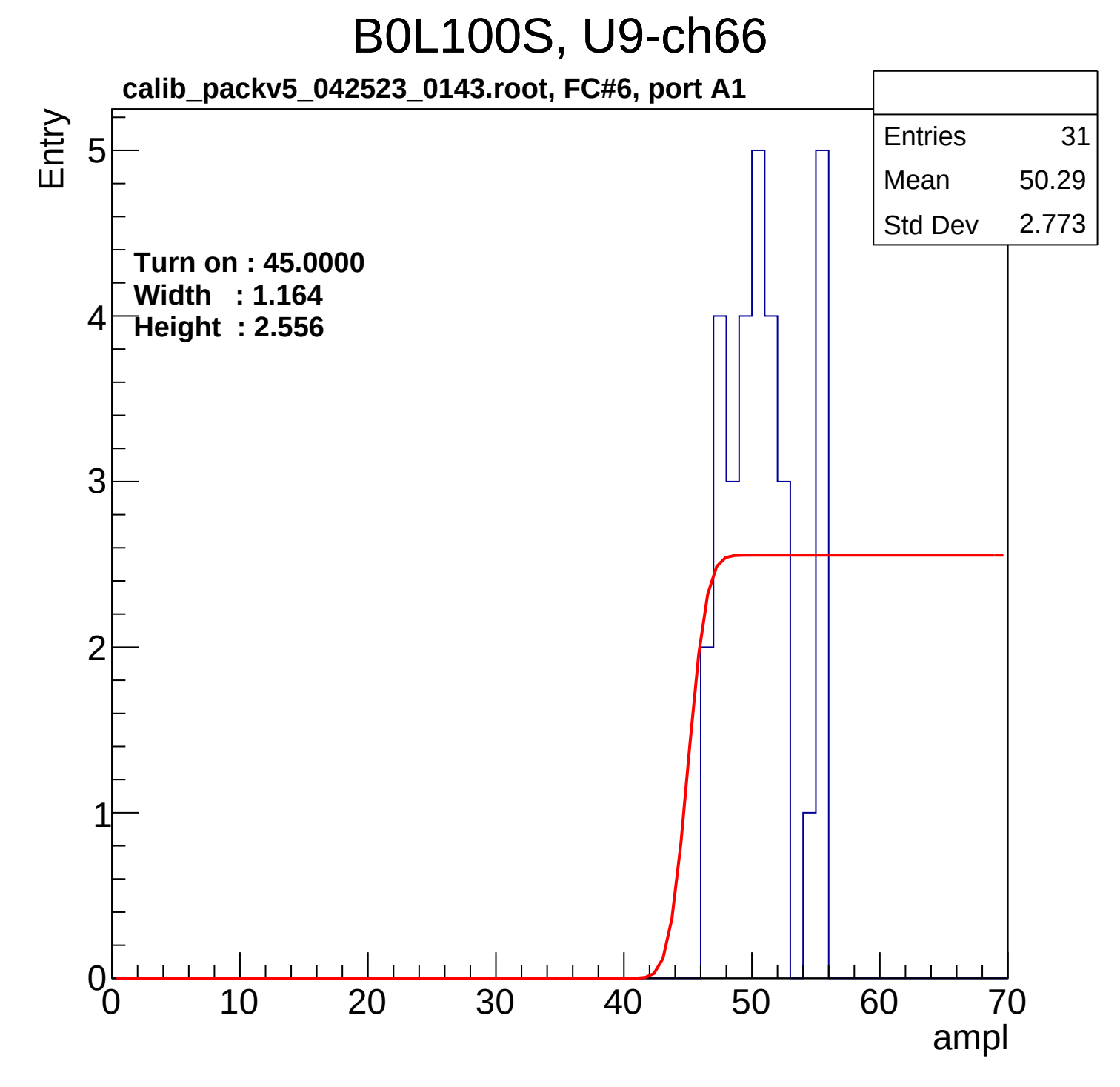

B0L100S, U9-ch65
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U9-ch66
calib_packv5_042523_0143.root, FC#6, port A1
Entries 31
Mean 50.29
Std Dev 2.773
Turn on : 45.0000
Width : 1.164
Height : 2.556
Entry
ampl
0
1
2
3
4
5
0
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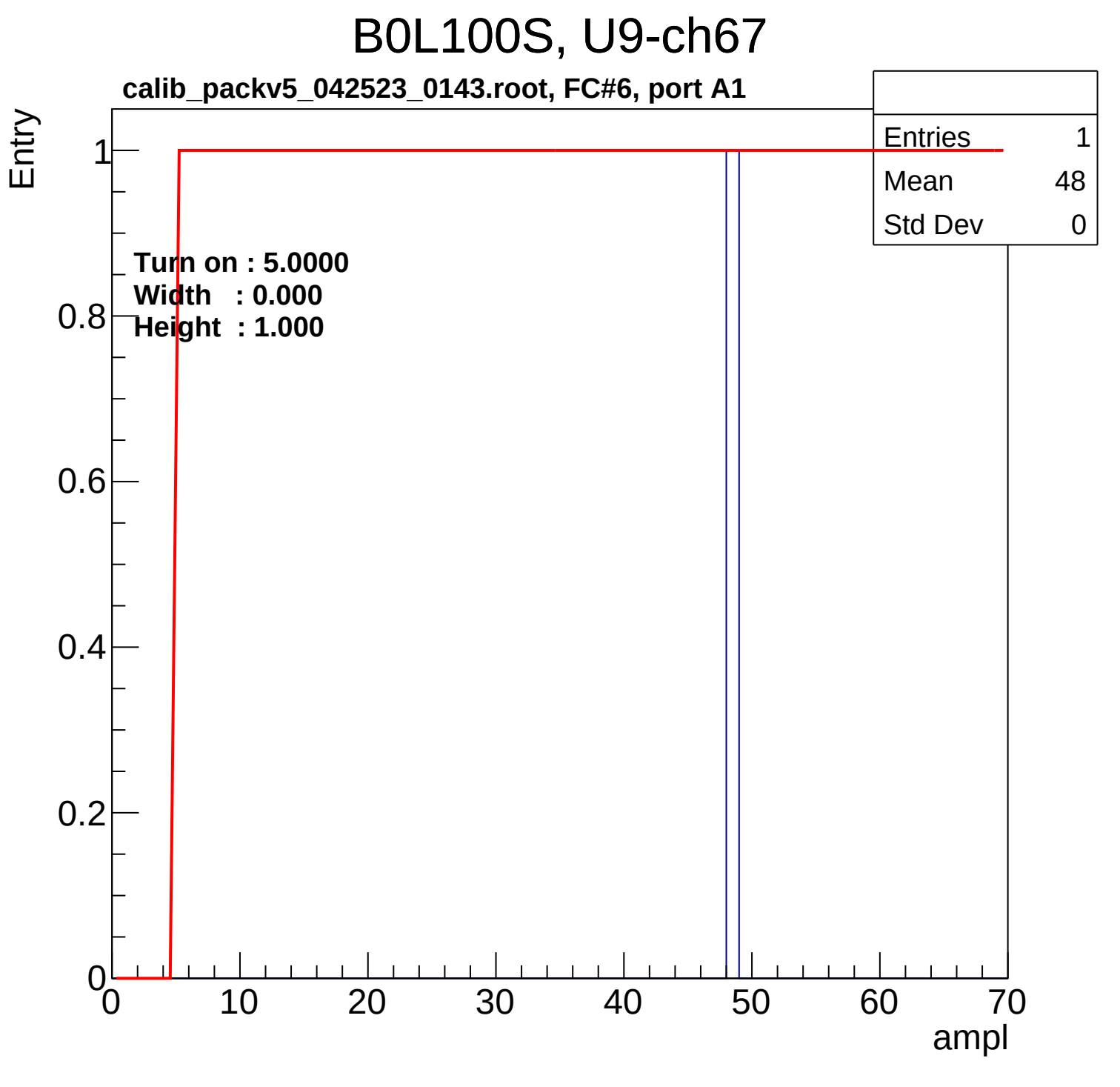
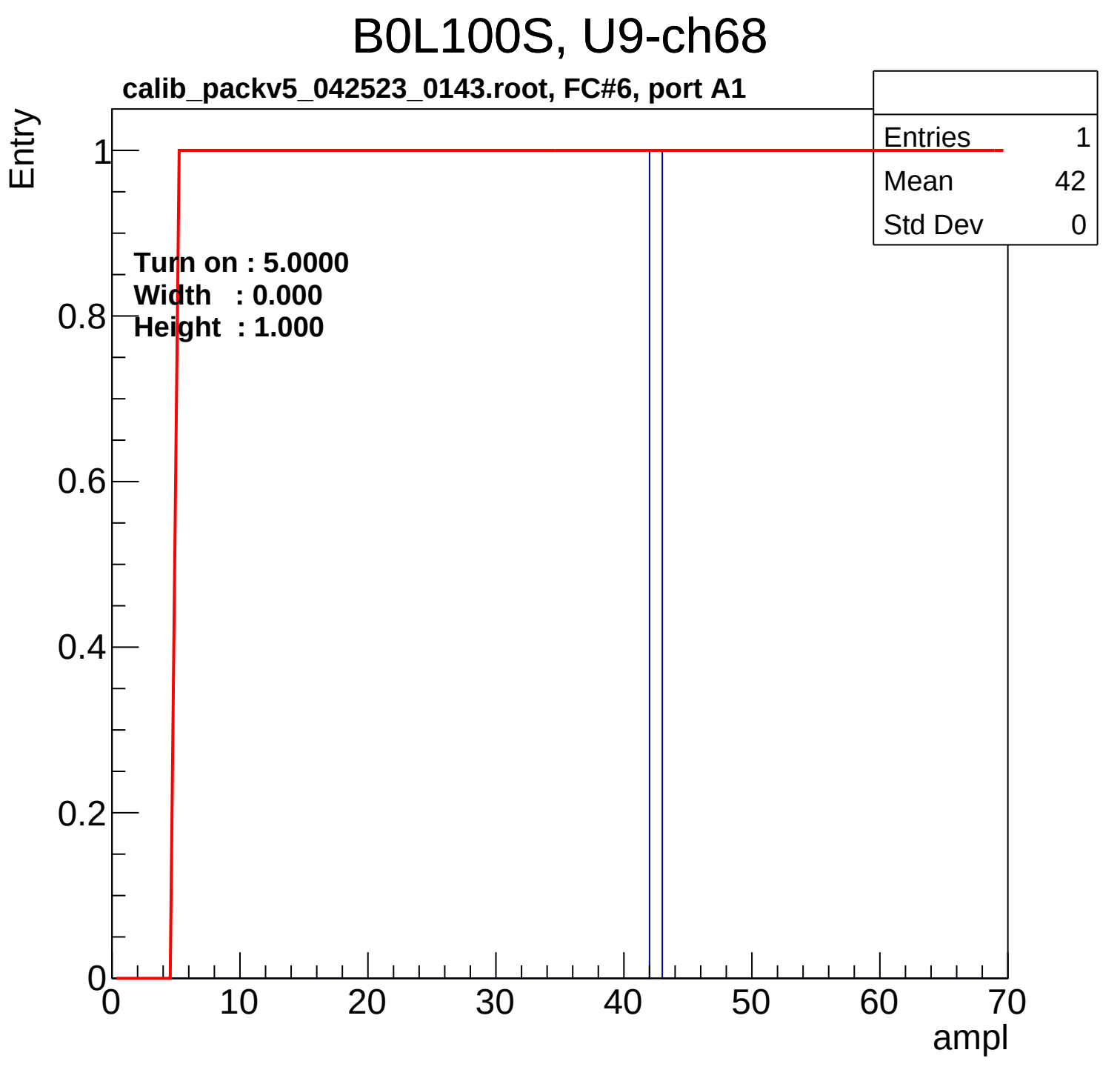
20
30
40
50
60
70


B0L100S, U9-ch67
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 48
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B0L100S, U9-ch68
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 42
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
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20
30
40
50
60
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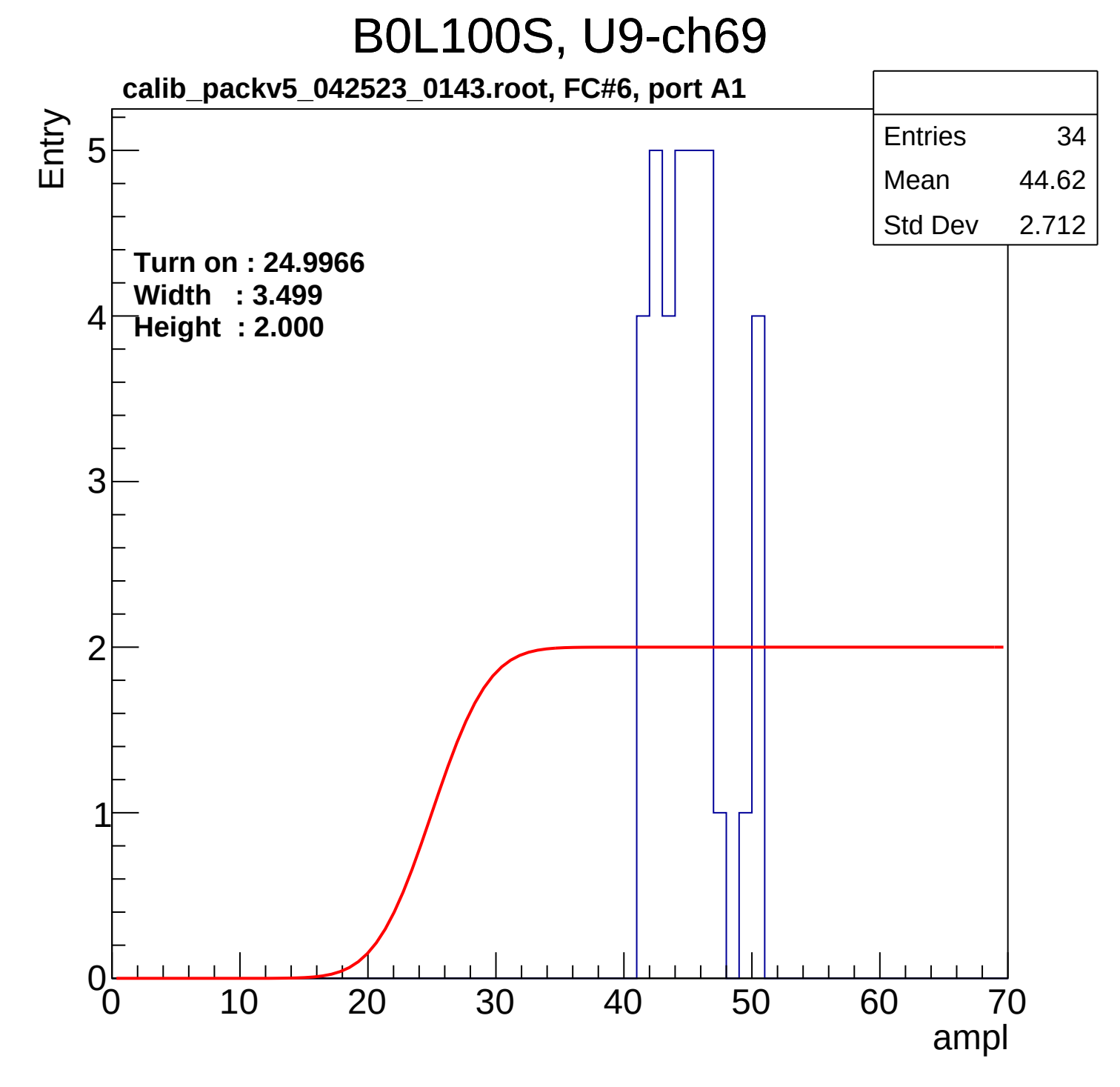
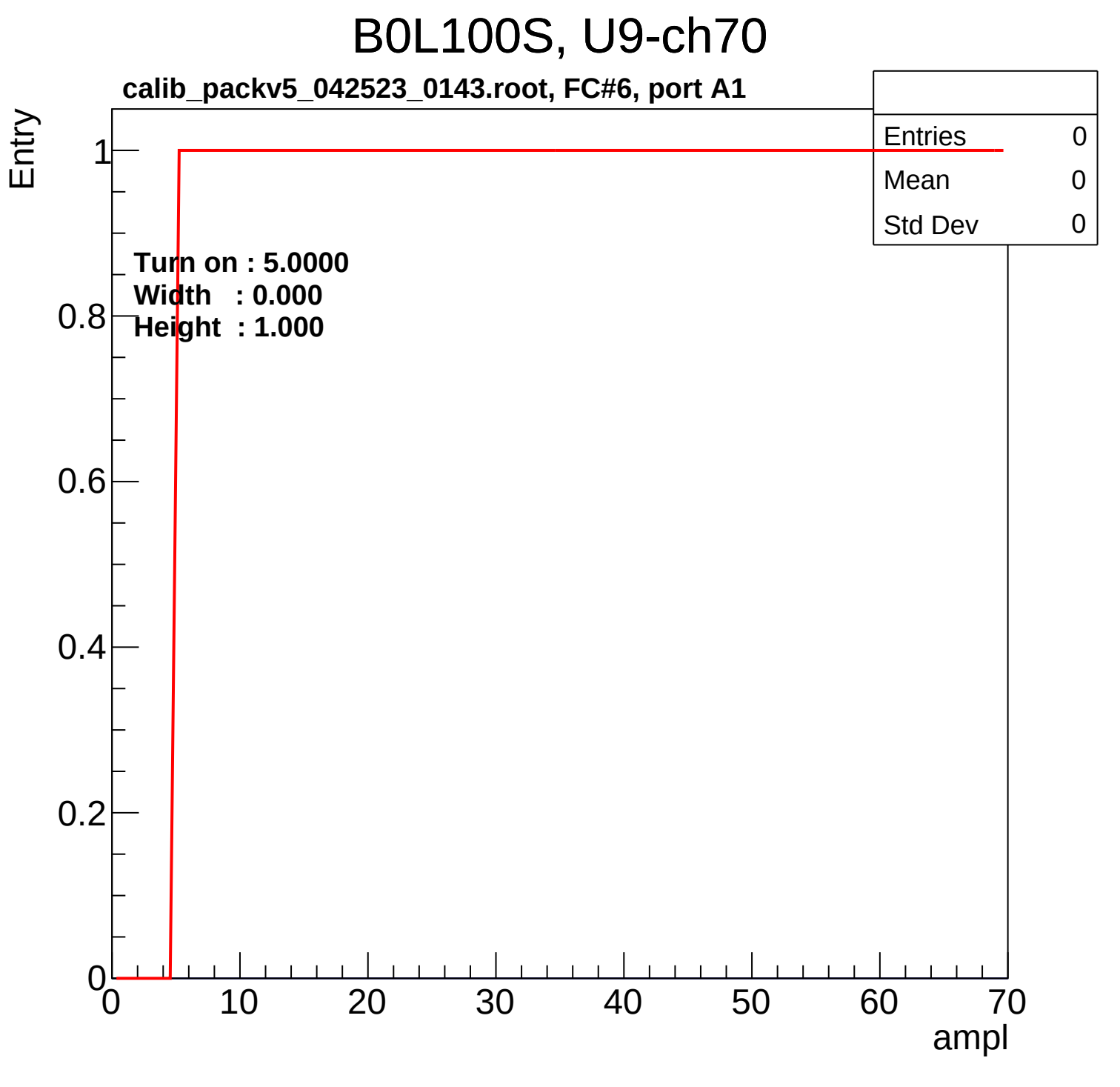

B0L100S, U9-ch69
calib_packv5_042523_0143.root, FC#6, port A1
Entries 34
Mean 44.62
Std Dev 2.712
Turn on : 24.9966
Width : 3.499
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B0L100S, U9-ch70
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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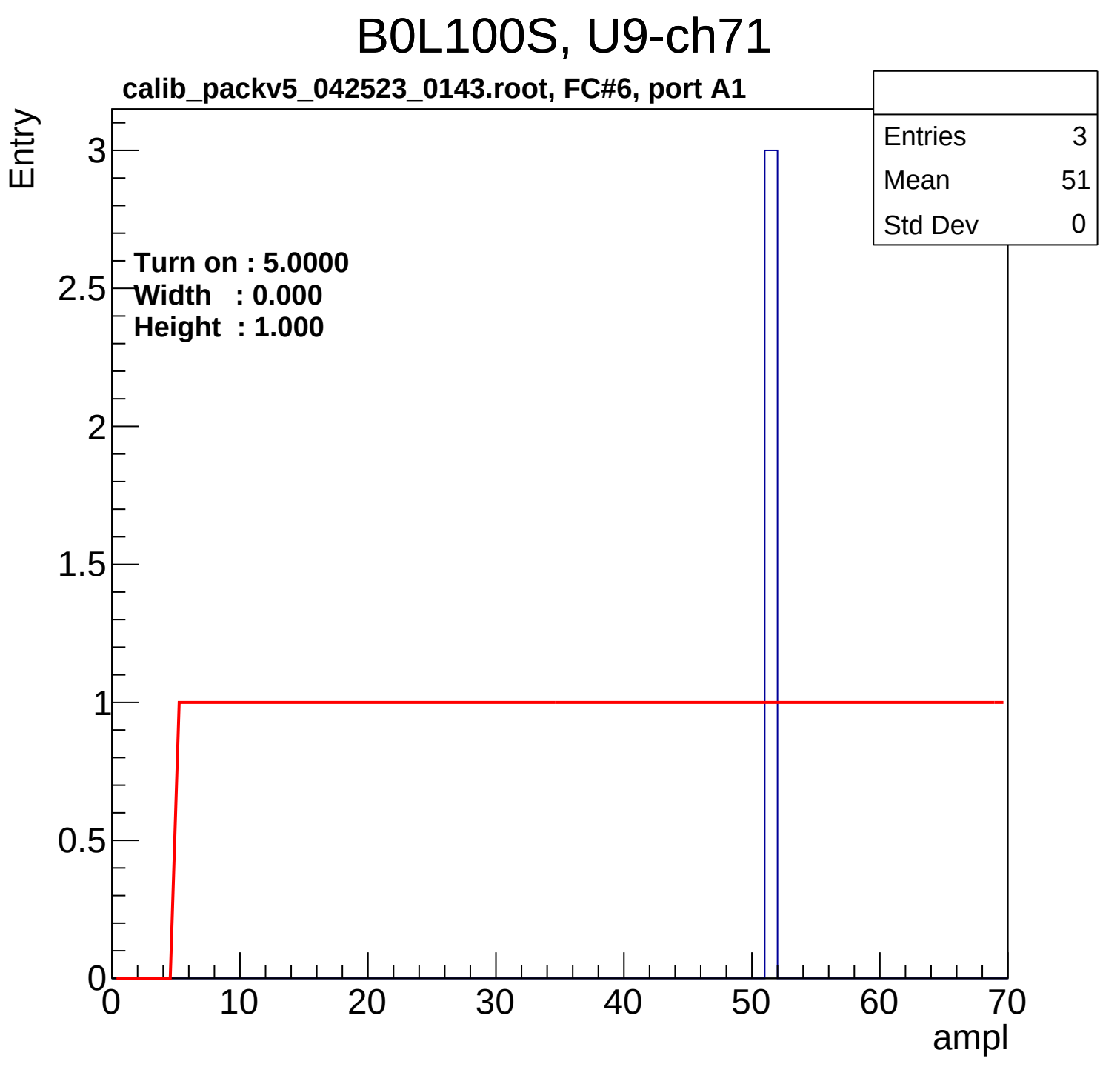
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U9-ch71
calib_packv5_042523_0143.root, FC#6, port A1
Entries 3
Mean 51
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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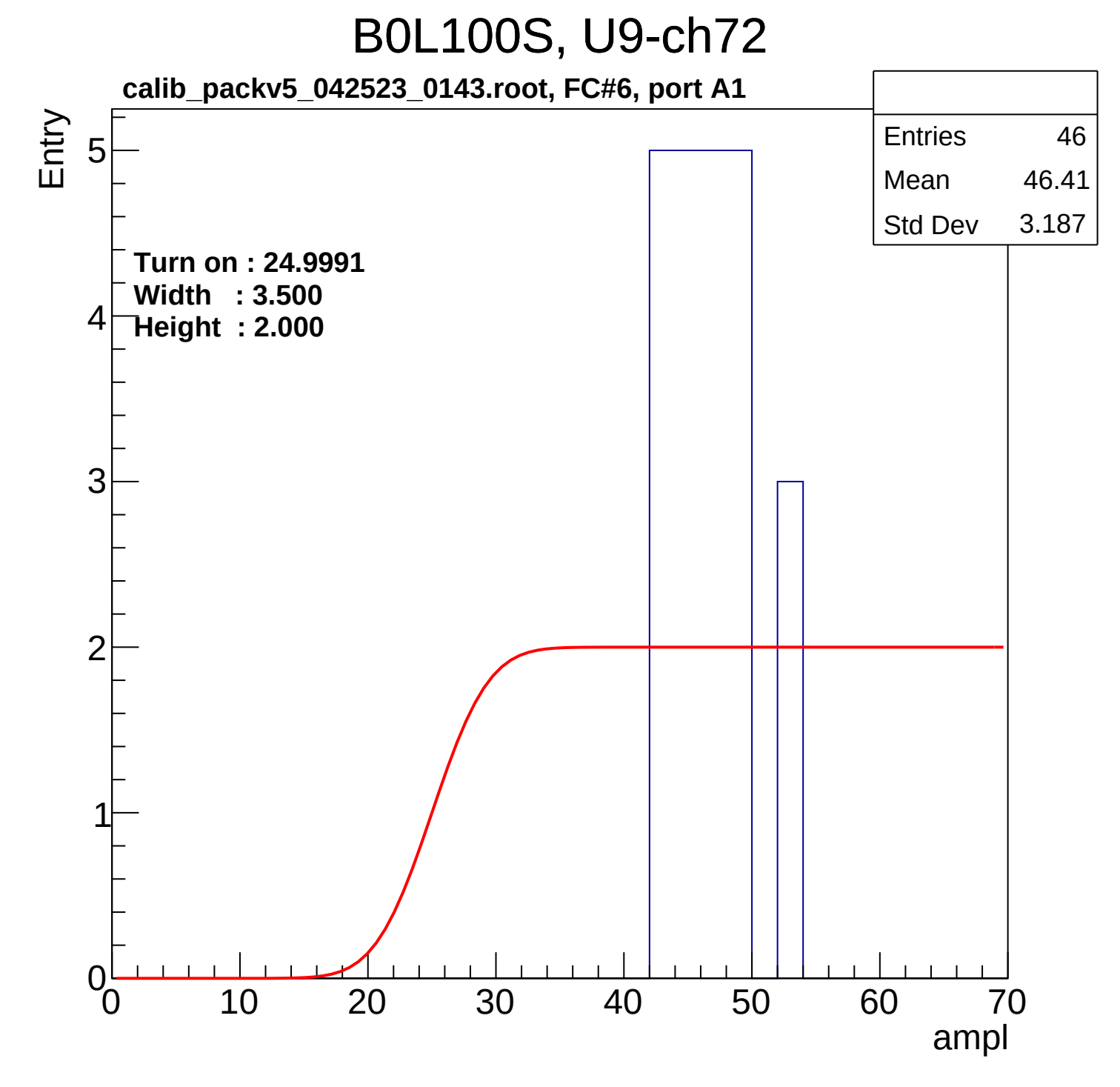
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B0L100S, U9-ch72
calib_packv5_042523_0143.root, FC#6, port A1
Entries 46
Mean 46.41
Std Dev 3.187
Turn on : 24.9991
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
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20
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40
50
60
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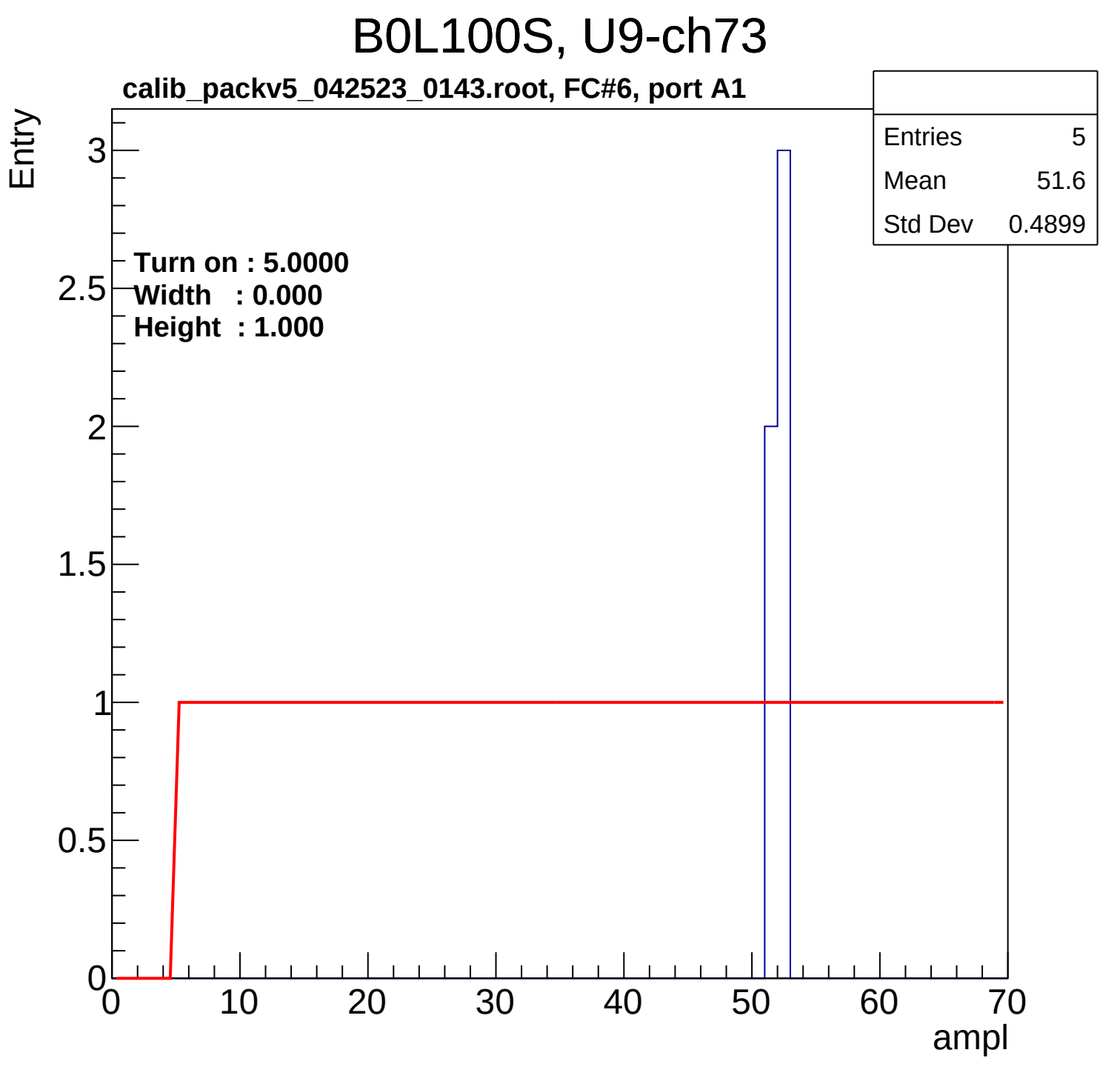
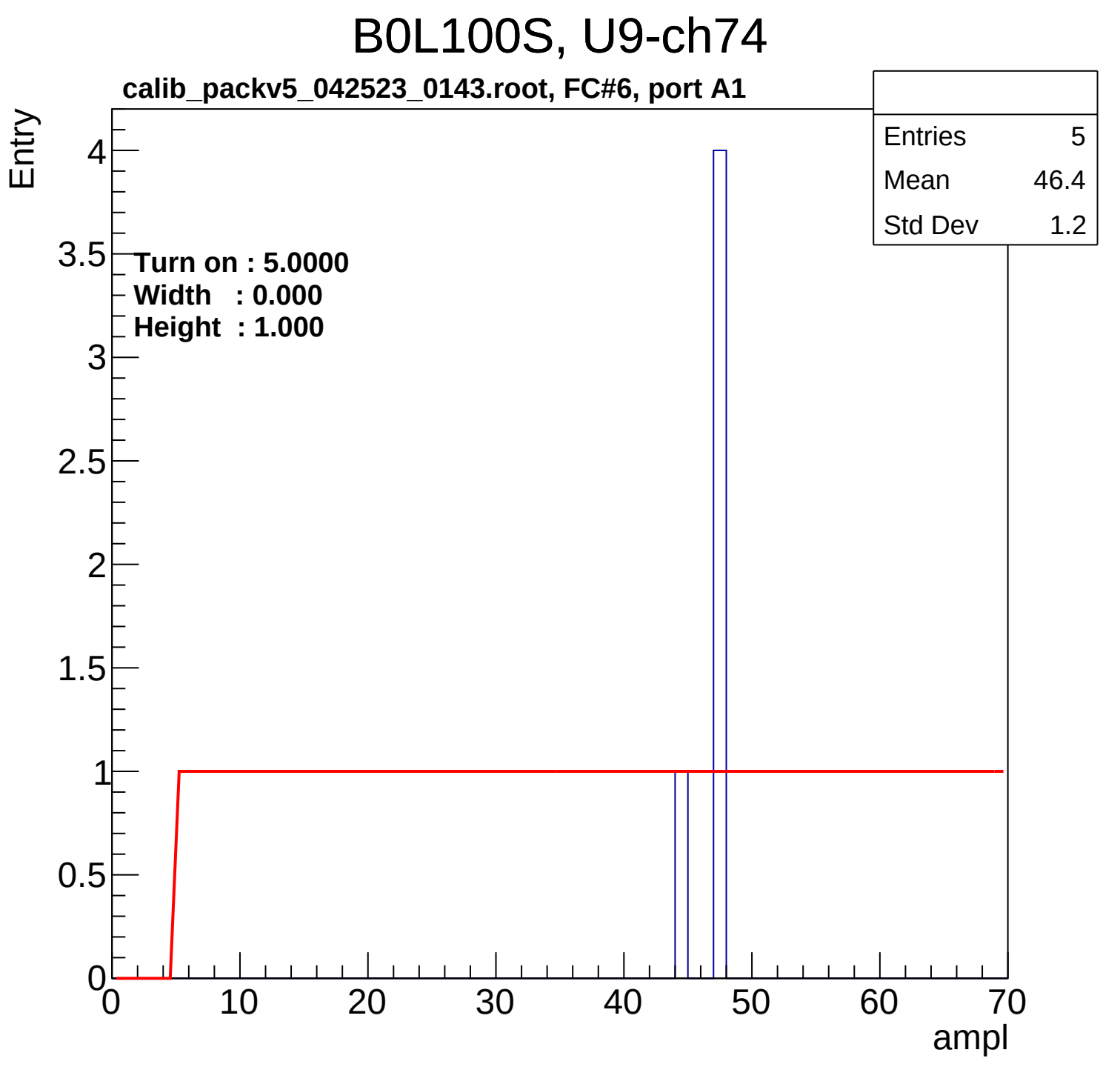
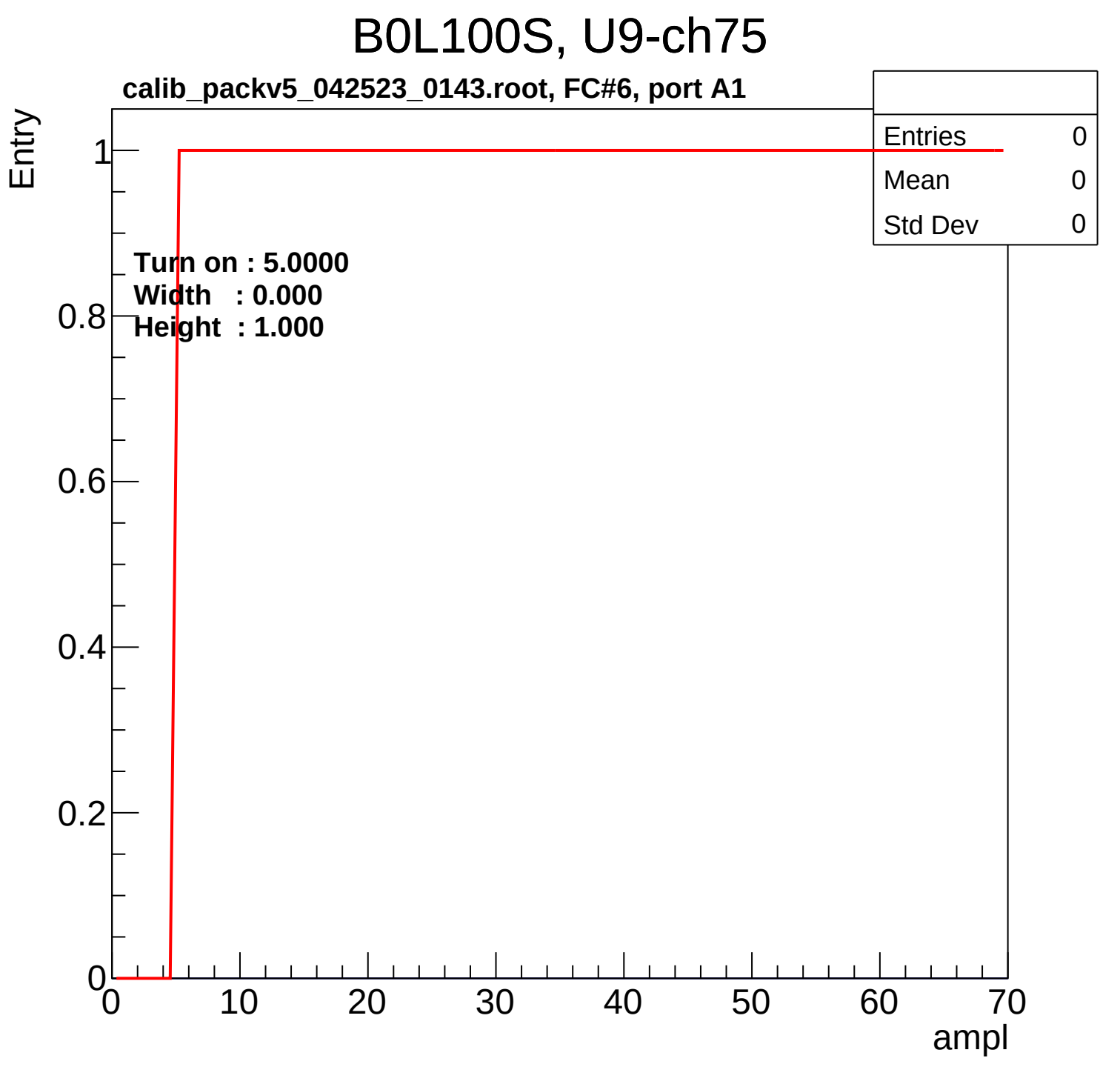

B0L100S, U9-ch73
calib_packv5_042523_0143.root, FC#6, port A1
Entries 5
Mean 51.6
Std Dev 0.4899
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B0L100S, U9-ch74
calib_packv5_042523_0143.root, FC#6, port A1
Entries 5
Mean 46.4
Std Dev 1.2
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B0L100S, U9-ch75
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
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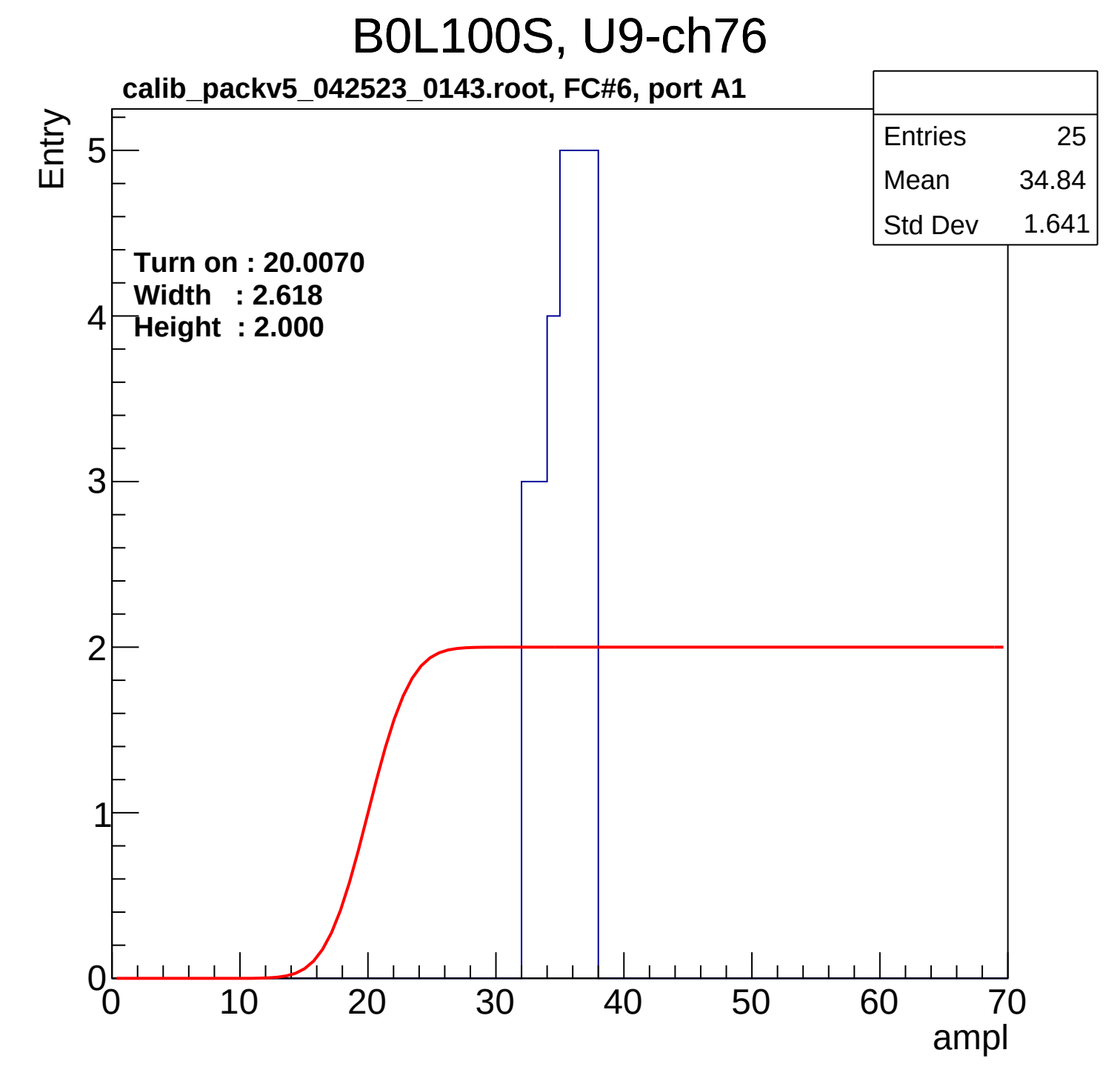
50
60
70
ampl


B0L100S, U9-ch76
calib_packv5_042523_0143.root, FC#6, port A1
Entries 25
Mean 34.84
Std Dev 1.641
Turn on : 20.0070
Width : 2.618
Height : 2.000
Entry
ampl
0
1
2
3
4
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0
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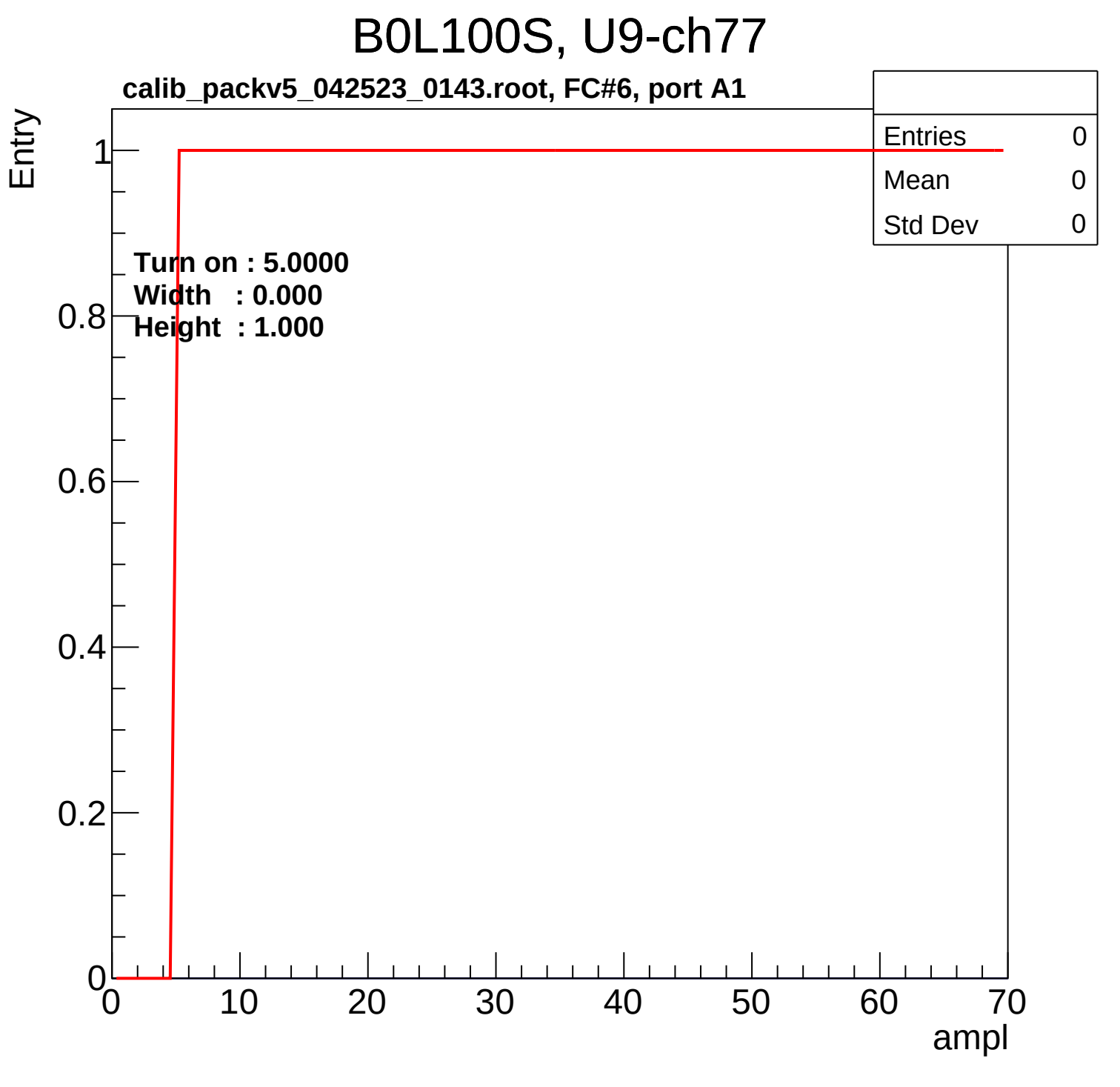
B0L100S, U9-ch77
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
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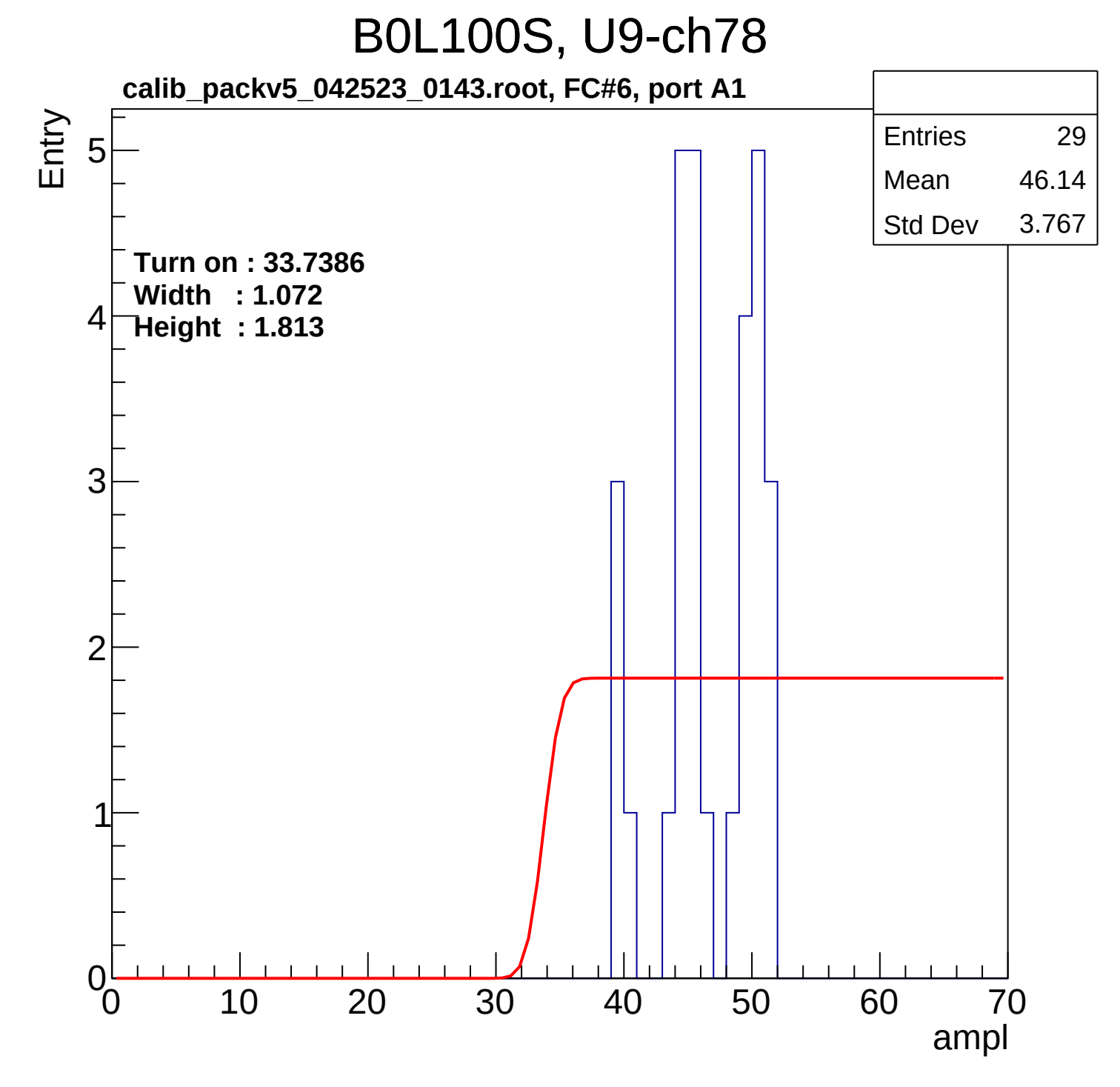
40
50
60
70
ampl


B0L100S, U9-ch78
calib_packv5_042523_0143.root, FC#6, port A1
Entries 29
Mean 46.14
Std Dev 3.767
Turn on : 33.7386
Width : 1.072
Height : 1.813
Entry
ampl
0
1
2
3
4
5
0
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20
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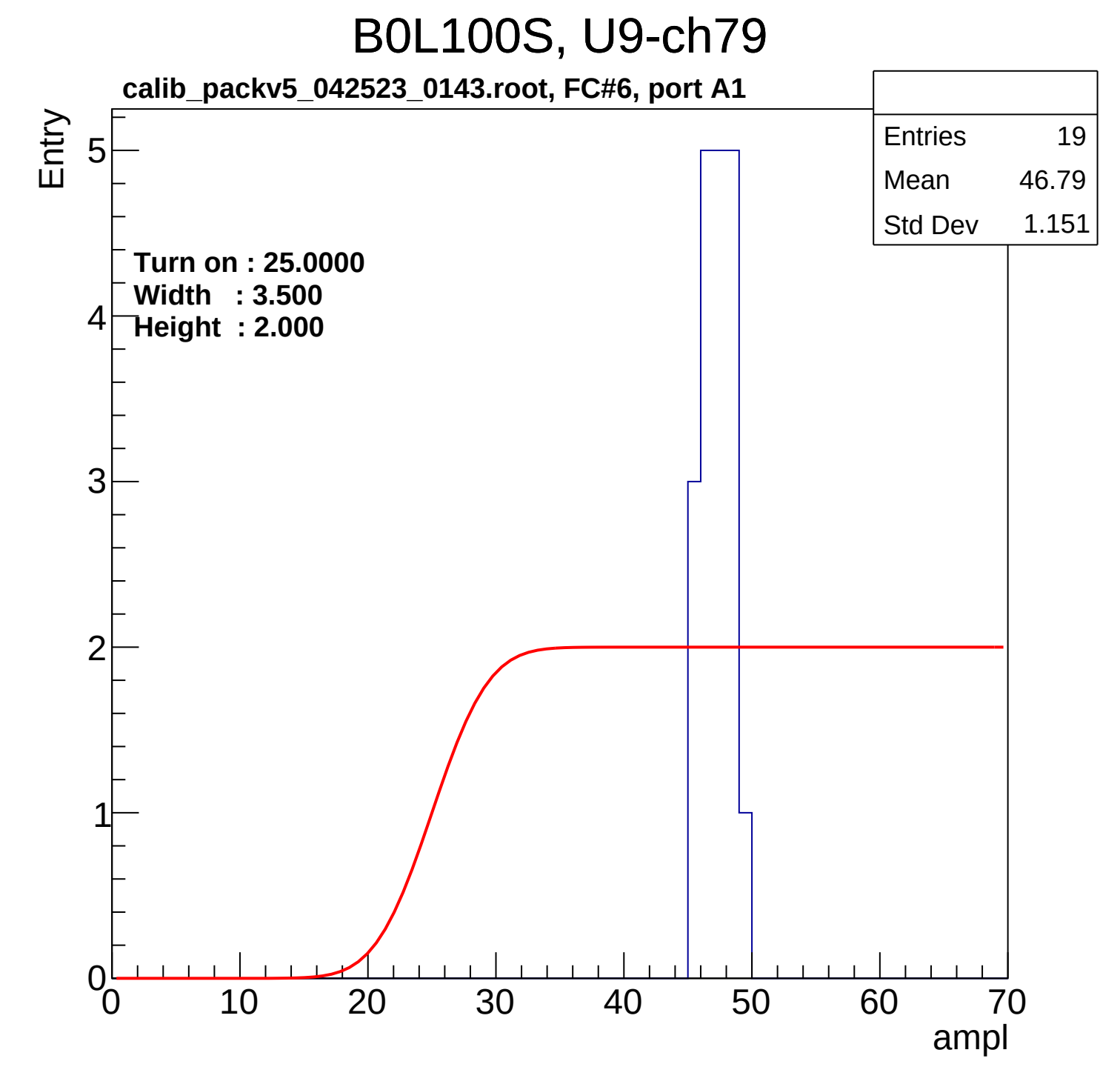
B0L100S, U9-ch79
calib_packv5_042523_0143.root, FC#6, port A1
Entries 19
Mean 46.79
Std Dev 1.151
Turn on : 25.0000
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
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0
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20
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60
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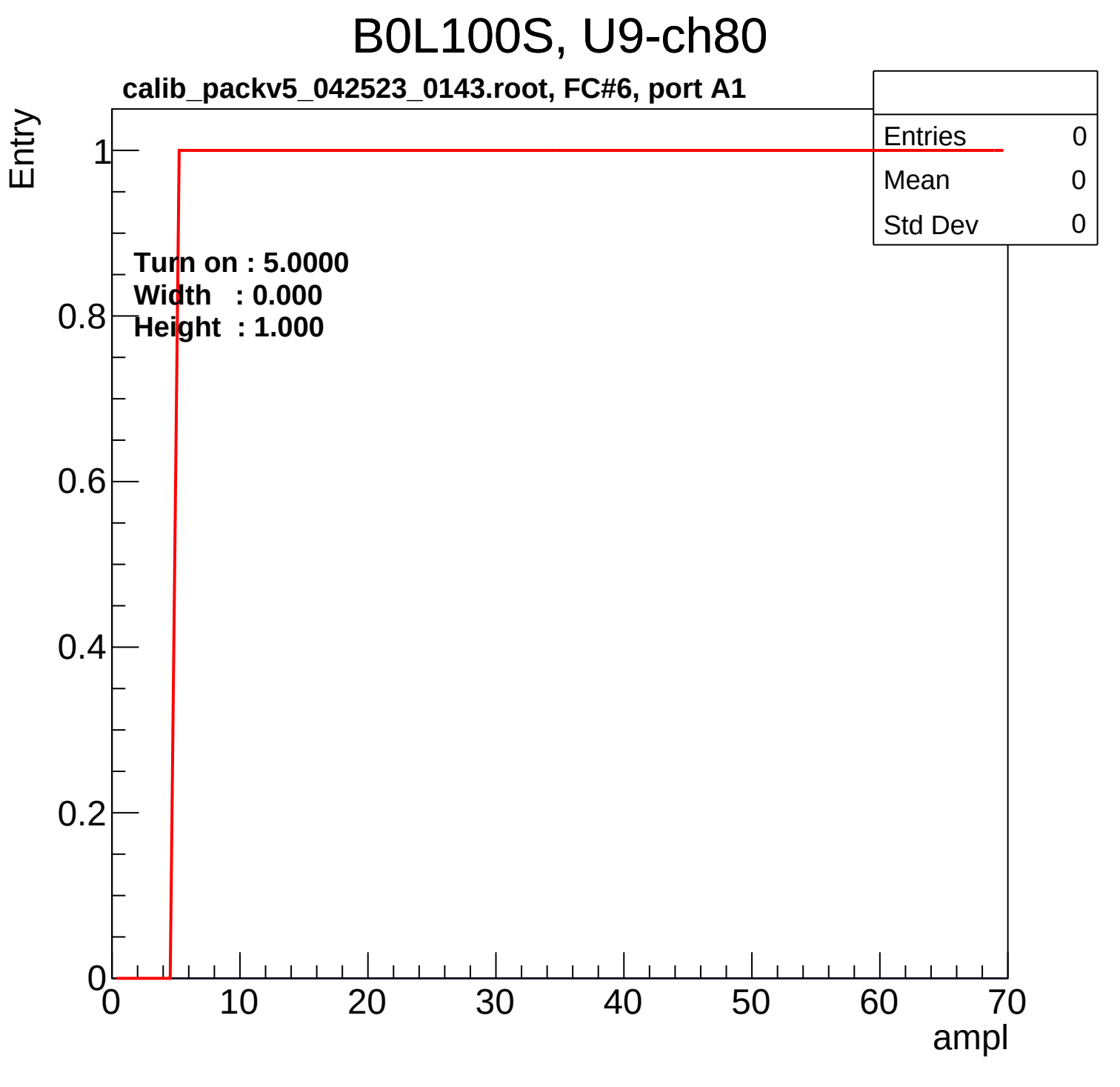
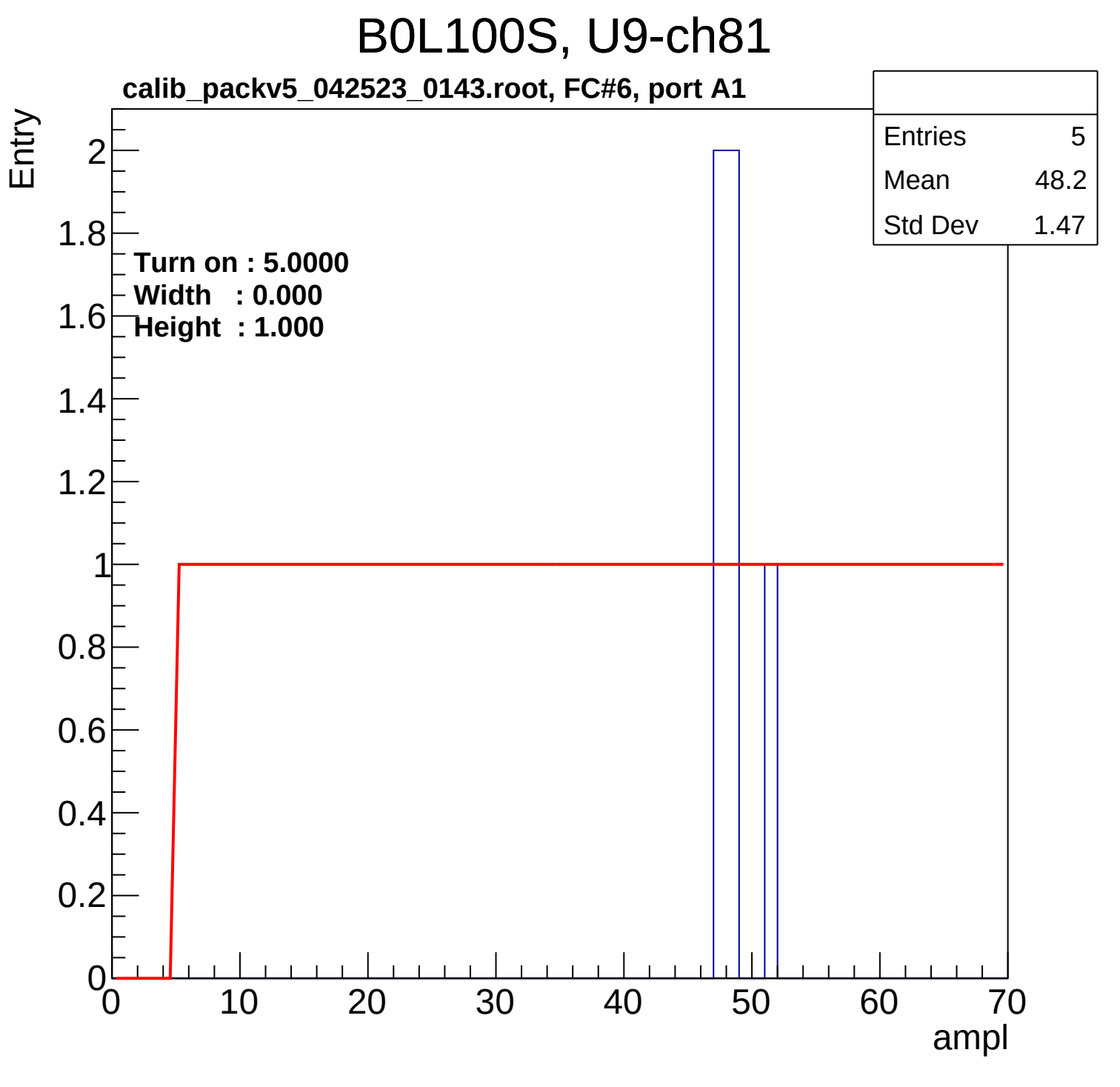
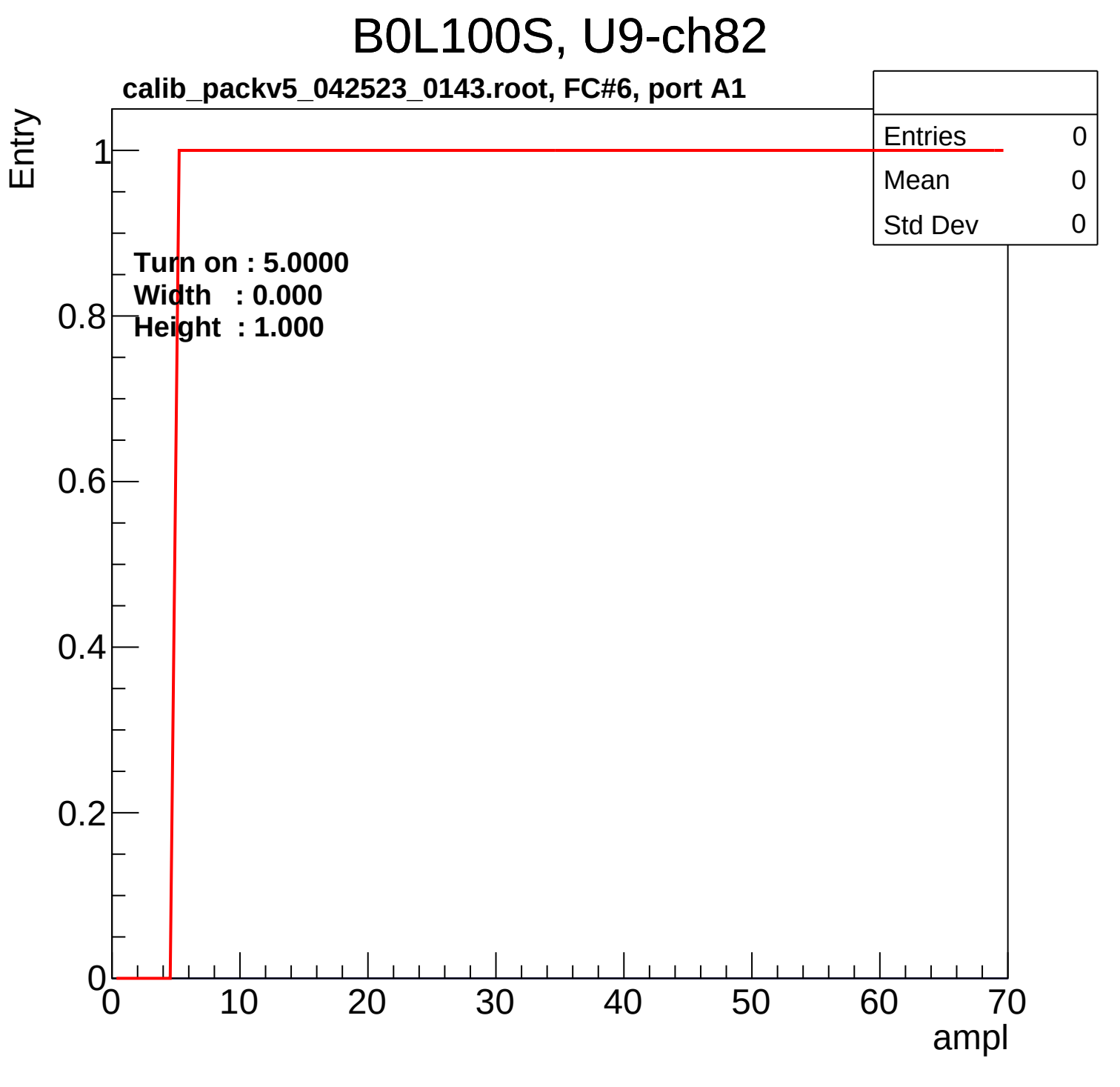
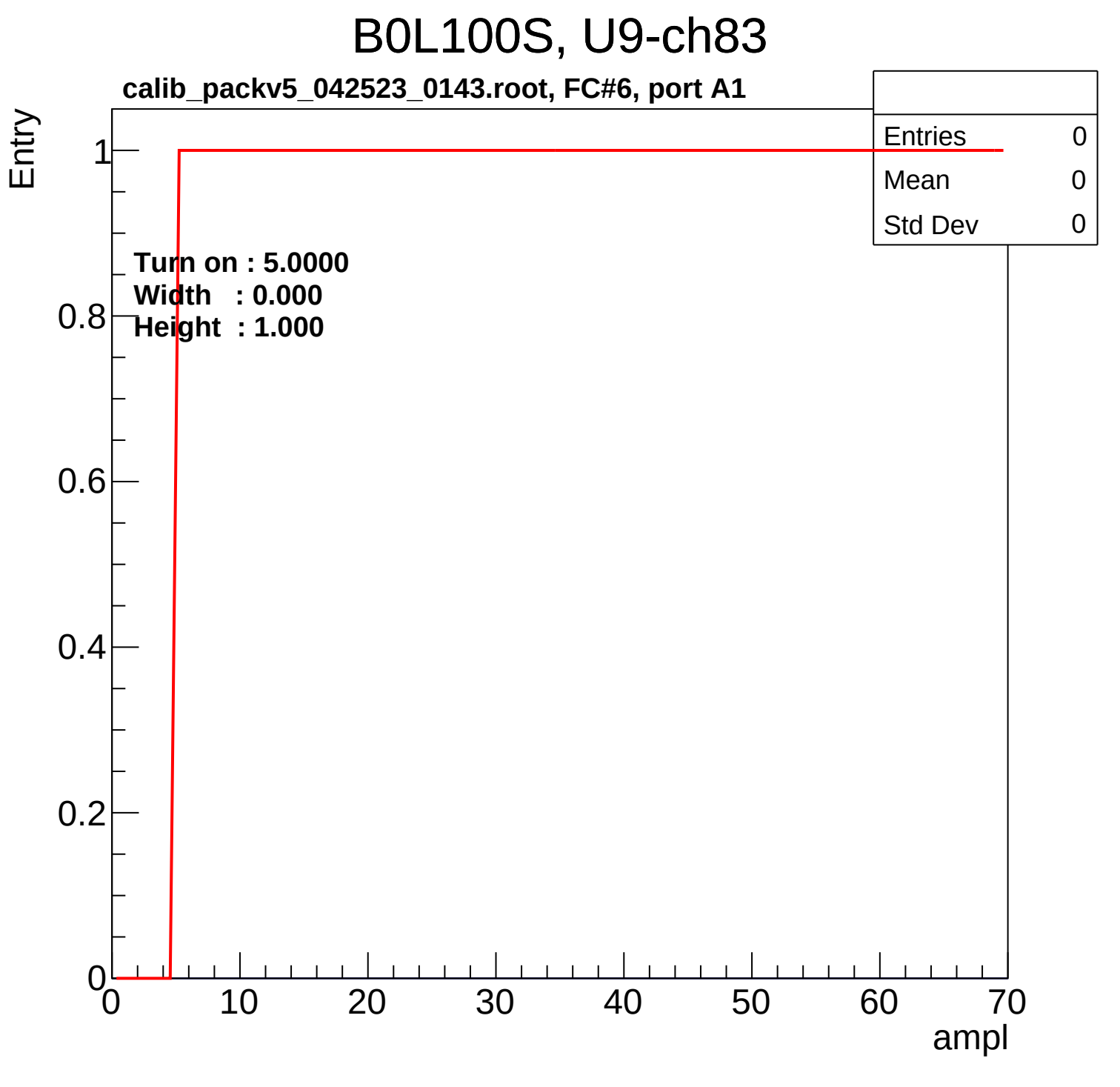
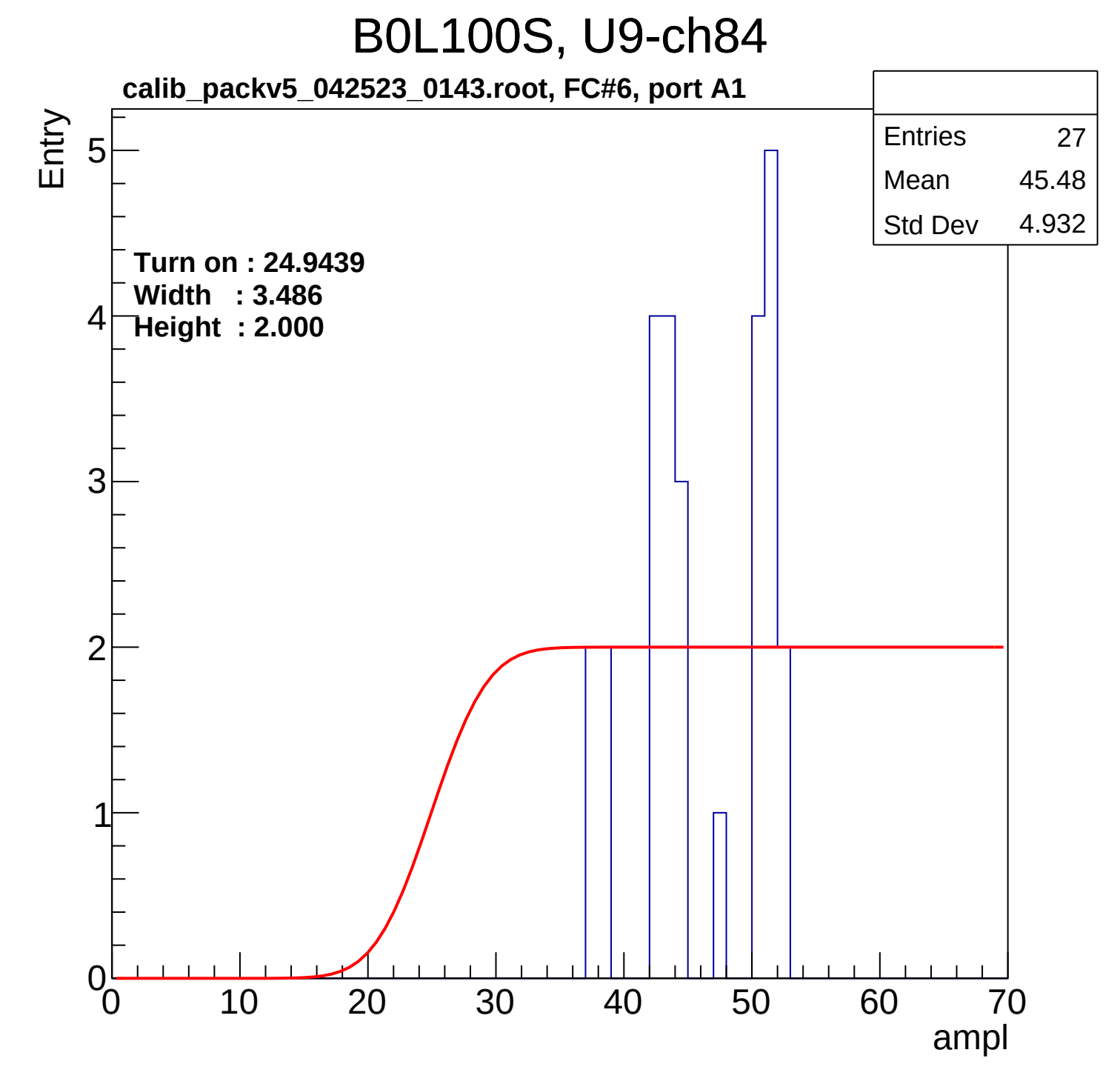

B0L100S, U9-ch80
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U9-ch81
calib_packv5_042523_0143.root, FC#6, port A1
Entries 5
Mean 48.2
Std Dev 1.47
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B0L100S, U9-ch82
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U9-ch83
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U9-ch84
calib_packv5_042523_0143.root, FC#6, port A1
Entries 27
Mean 45.48
Std Dev 4.932
Turn on : 24.9439
Width : 3.486
Height : 2.000
Entry
ampl
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4
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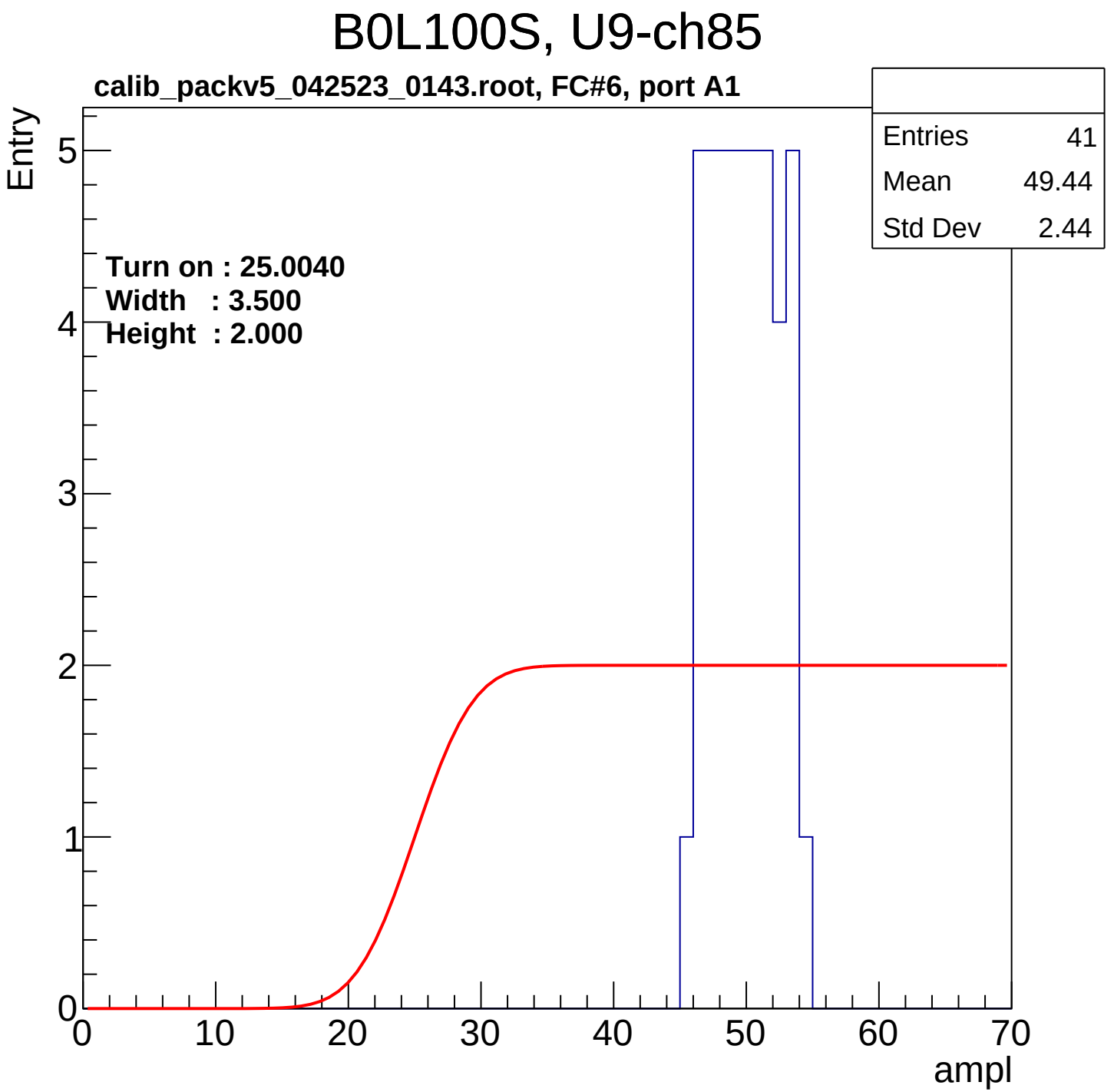
B0L100S, U9-ch85
calib_packv5_042523_0143.root, FC#6, port A1
Entries 41
Mean 49.44
Std Dev 2.44
Turn on : 25.0040
Width : 3.500
Height : 2.000
Entry
ampl
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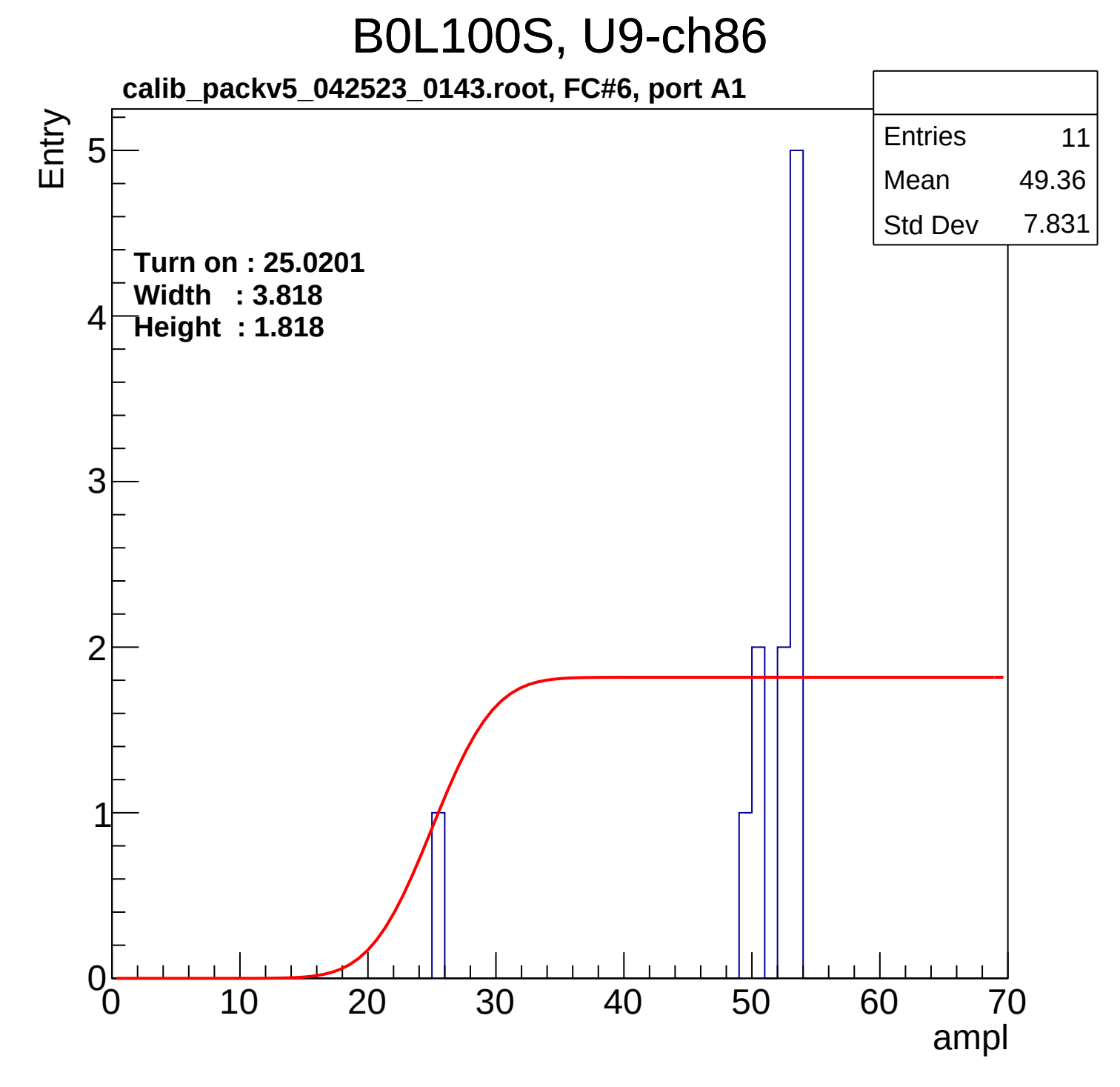
B0L100S, U9-ch86
calib_packv5_042523_0143.root, FC#6, port A1
Entries 11
Mean 49.36
Std Dev 7.831
Turn on : 25.0201
Width : 3.818
Height : 1.818
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
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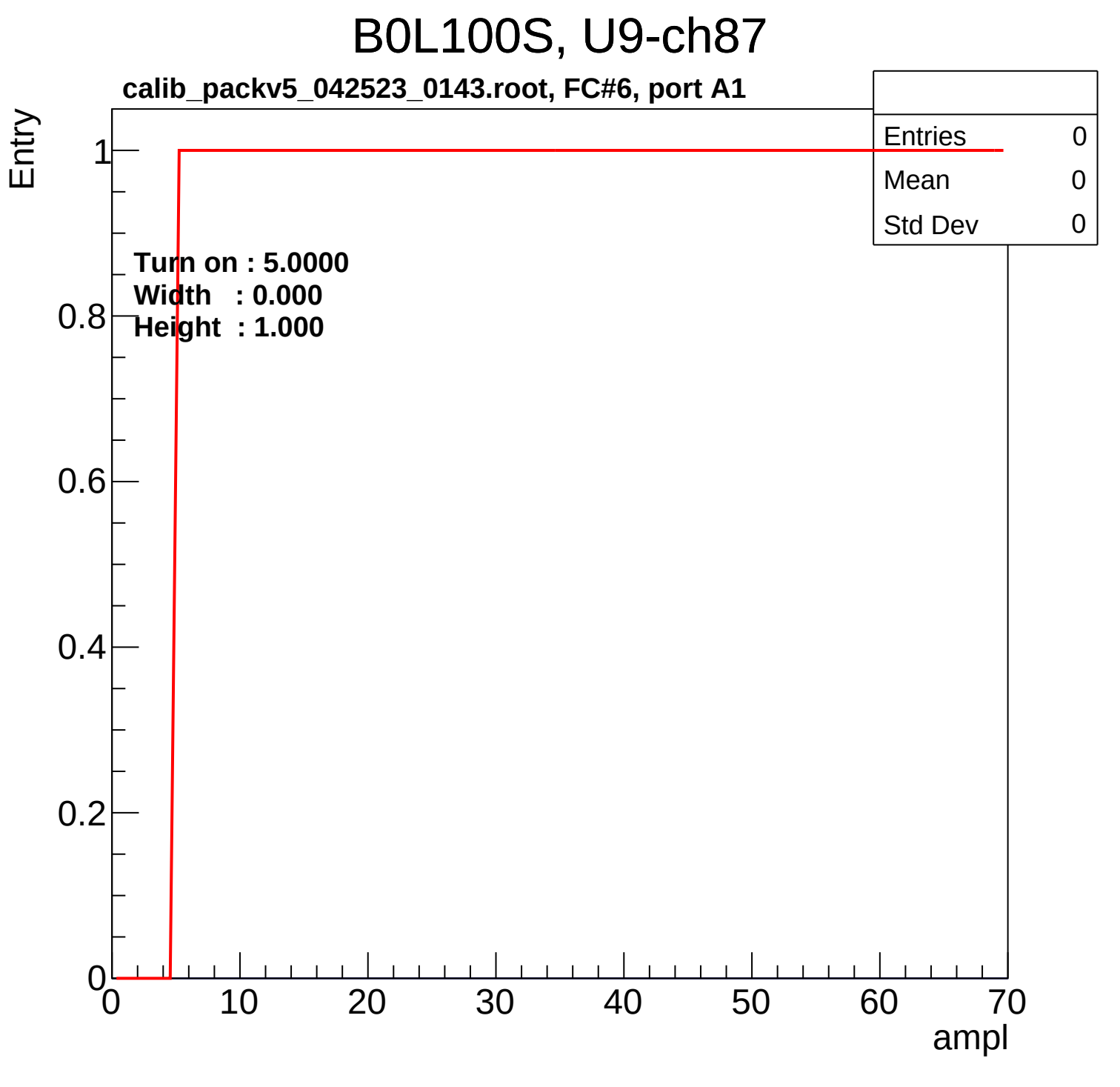
B0L100S, U9-ch87
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
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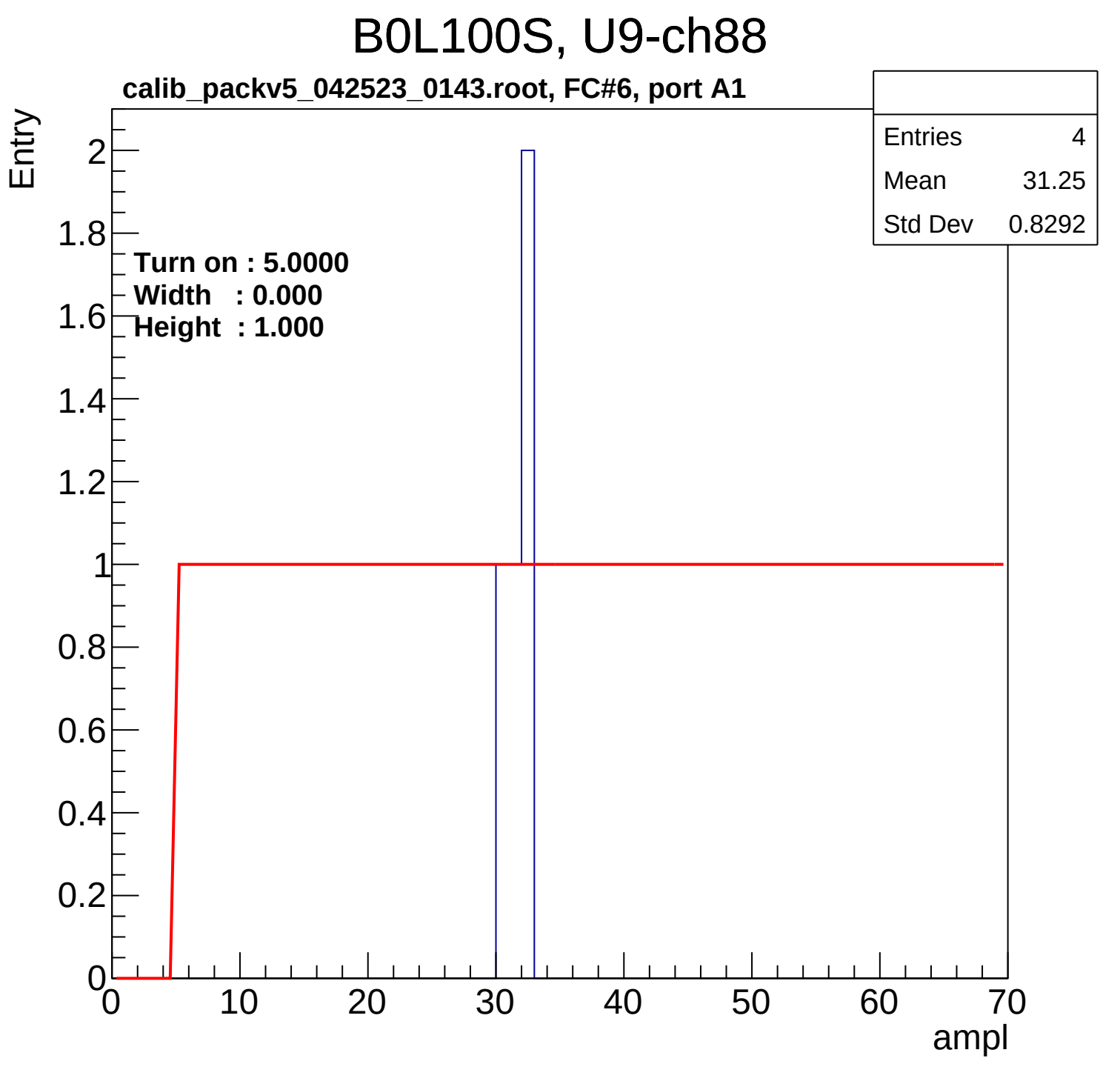
ampl


B0L100S, U9-ch88
calib_packv5_042523_0143.root, FC#6, port A1
Entries 4
Mean 31.25
Std Dev 0.8292
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
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1
1.2
1.4
1.6
1.8
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0
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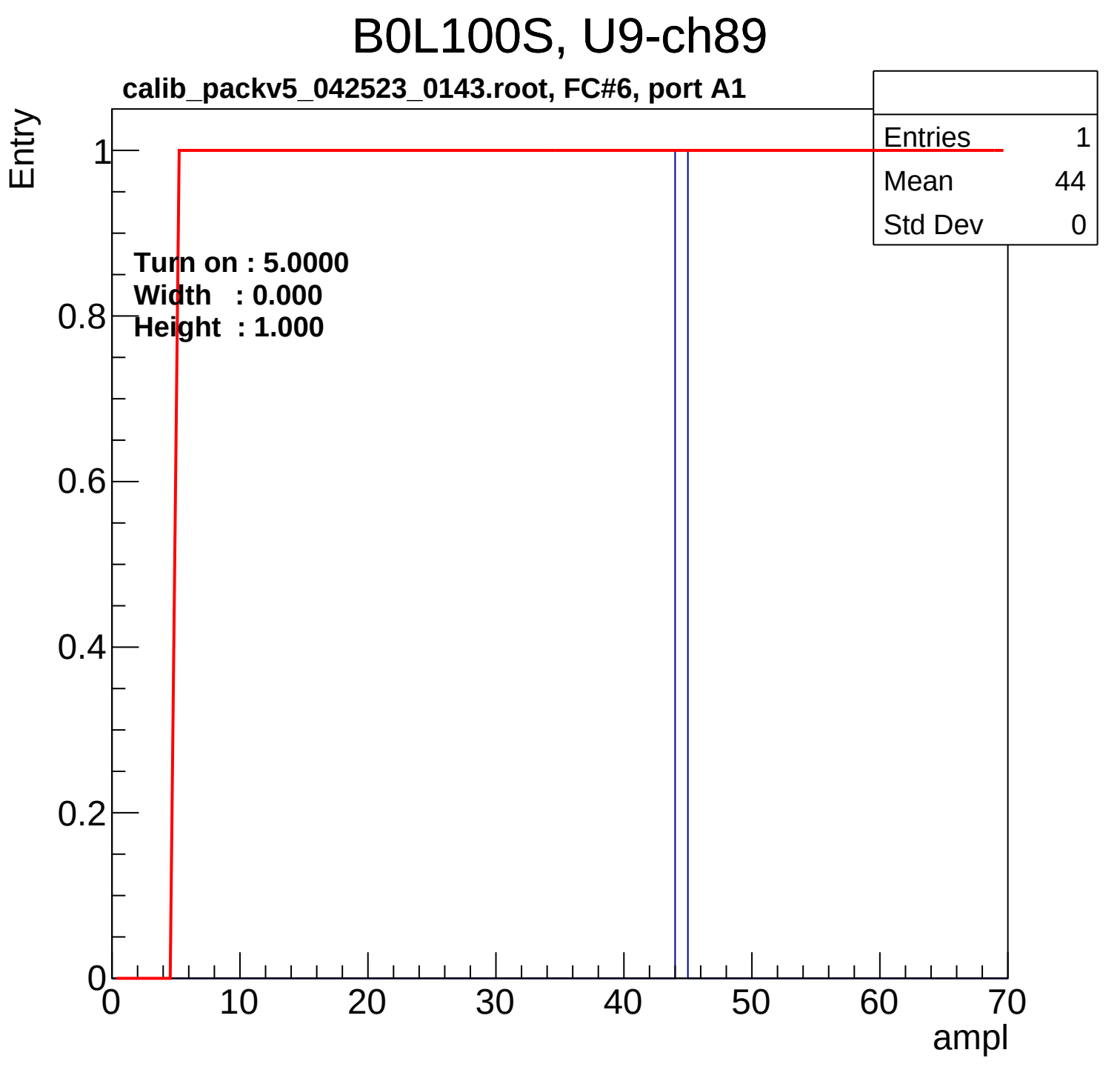
B0L100S, U9-ch89
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 44
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
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60
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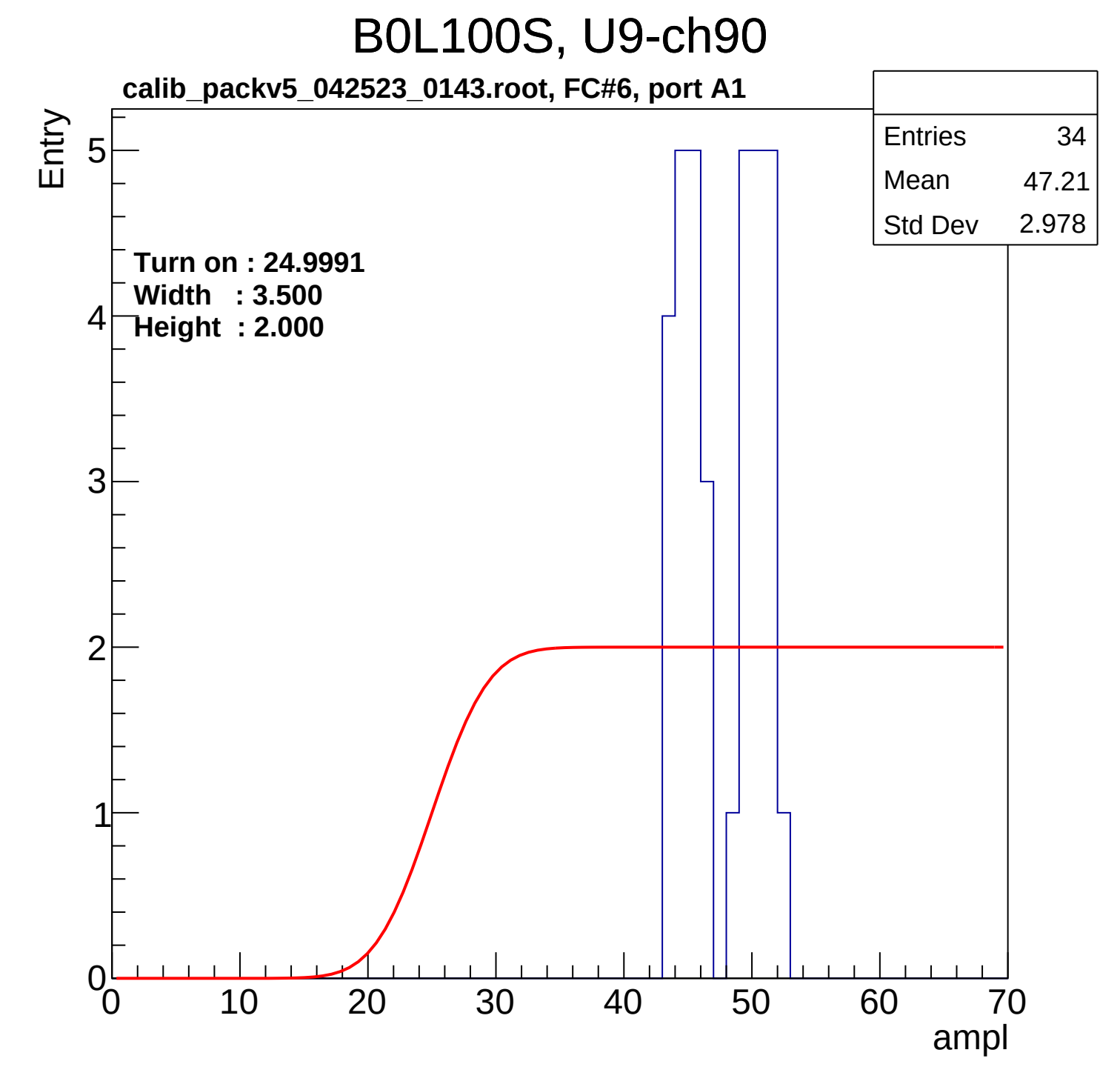
B0L100S, U9-ch90
calib_packv5_042523_0143.root, FC#6, port A1
Entries 34
Mean 47.21
Std Dev 2.978
Turn on : 24.9991
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
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40
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60
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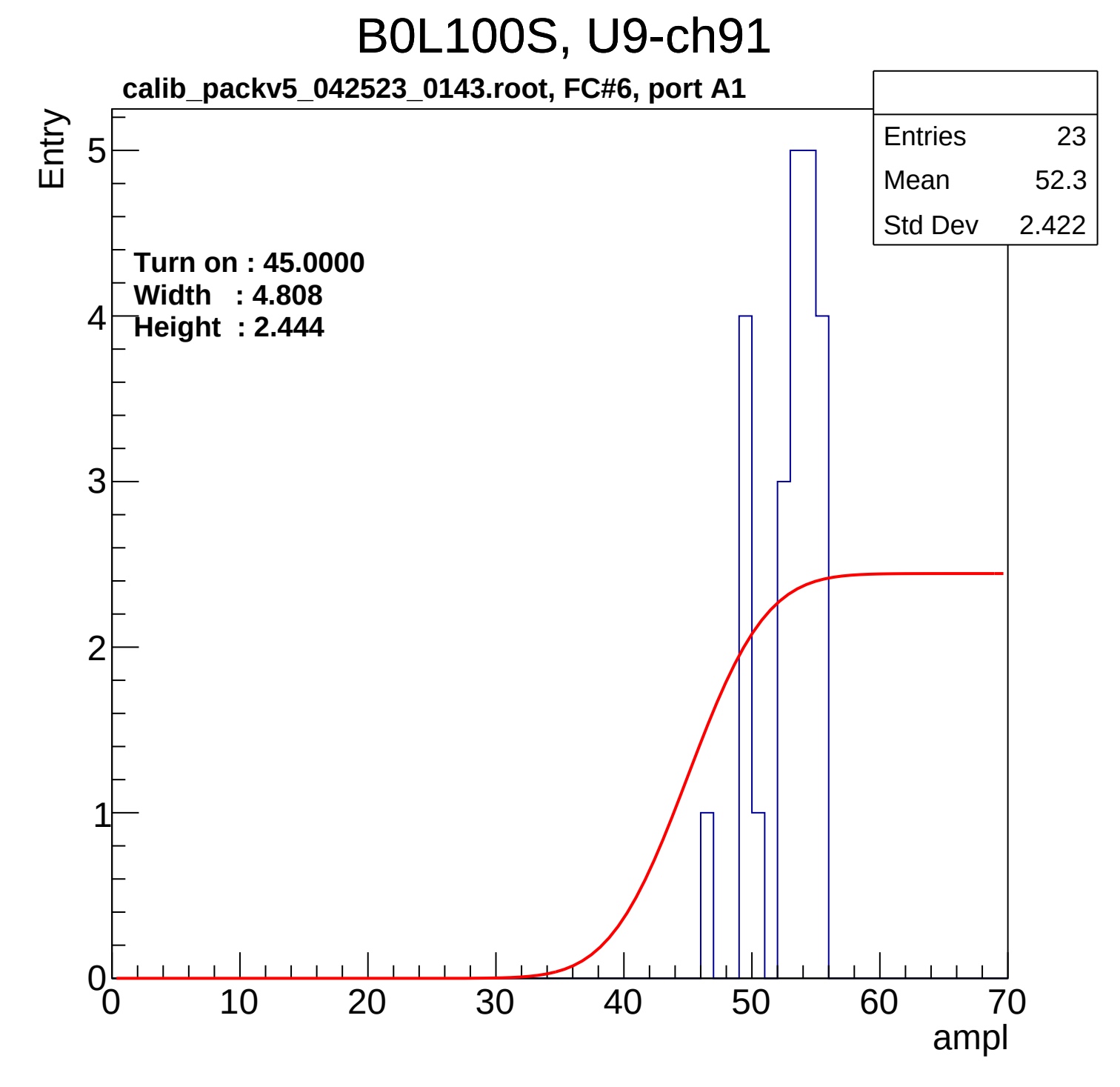
B0L100S, U9-ch91
calib_packv5_042523_0143.root, FC#6, port A1
Entries 23
Mean 52.3
Std Dev 2.422
Turn on : 45.0000
Width : 4.808
Height : 2.444
Entry
ampl
0
1
2
3
4
5
0
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40
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60
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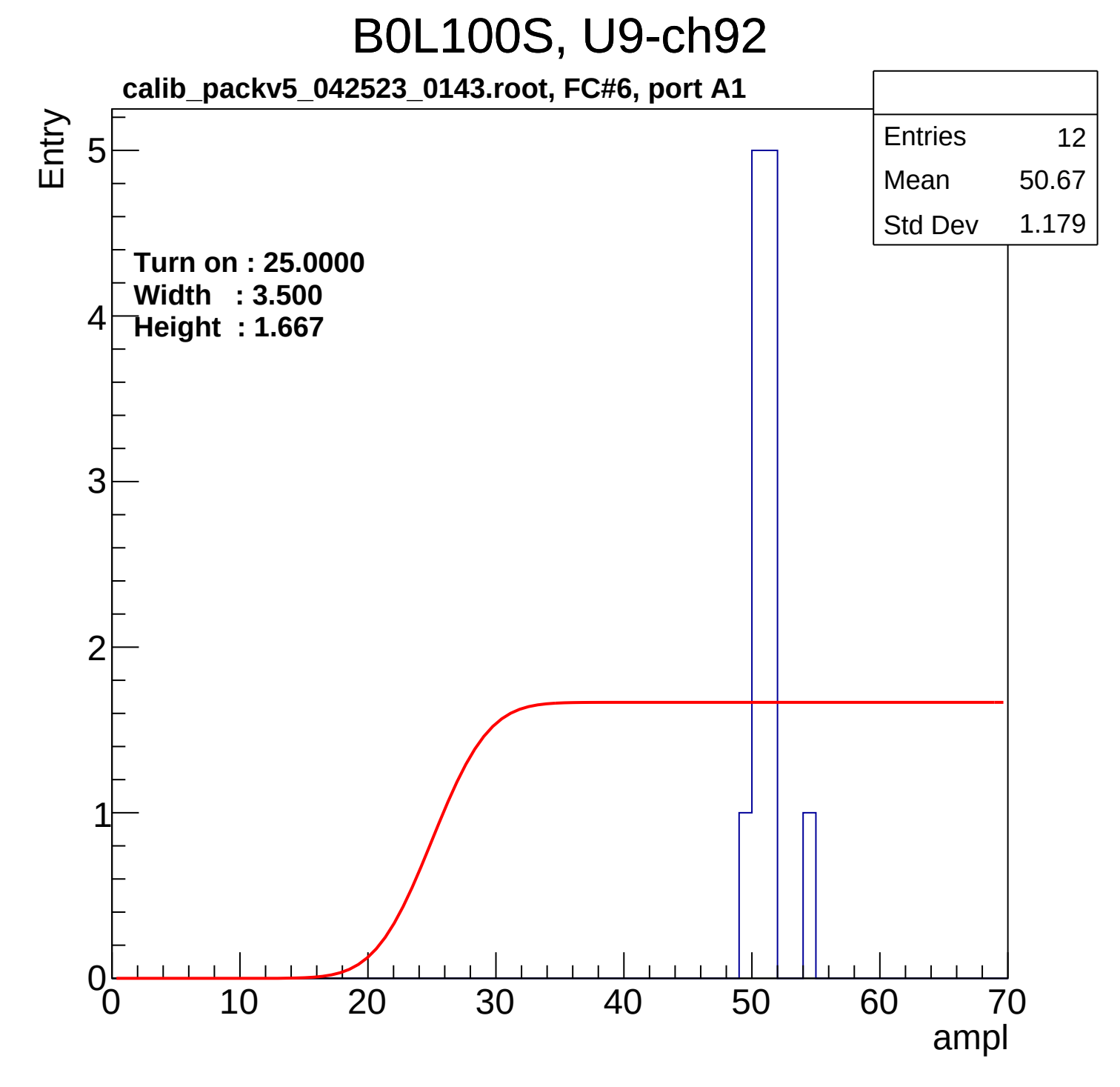
B0L100S, U9-ch92
calib_packv5_042523_0143.root, FC#6, port A1
Entries 12
Mean 50.67
Std Dev 1.179
Turn on : 25.0000
Width : 3.500
Height : 1.667
Entry
ampl
0
1
2
3
4
5
0
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40
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60
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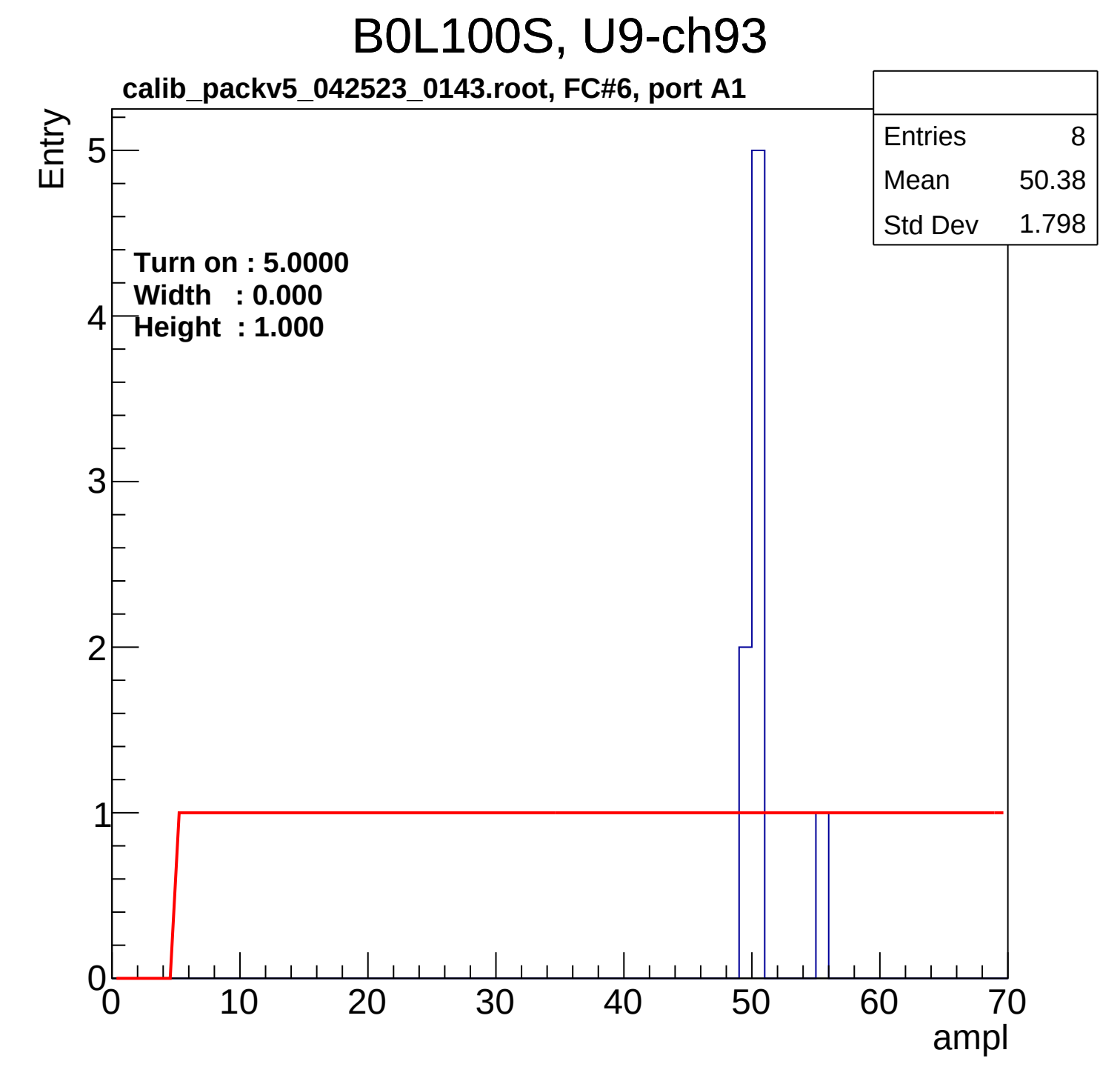
B0L100S, U9-ch93
calib_packv5_042523_0143.root, FC#6, port A1
Entries 8
Mean 50.38
Std Dev 1.798
Turn on : 5.0000
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Height : 1.000
Entry
0
1
2
3
4
5
0
10
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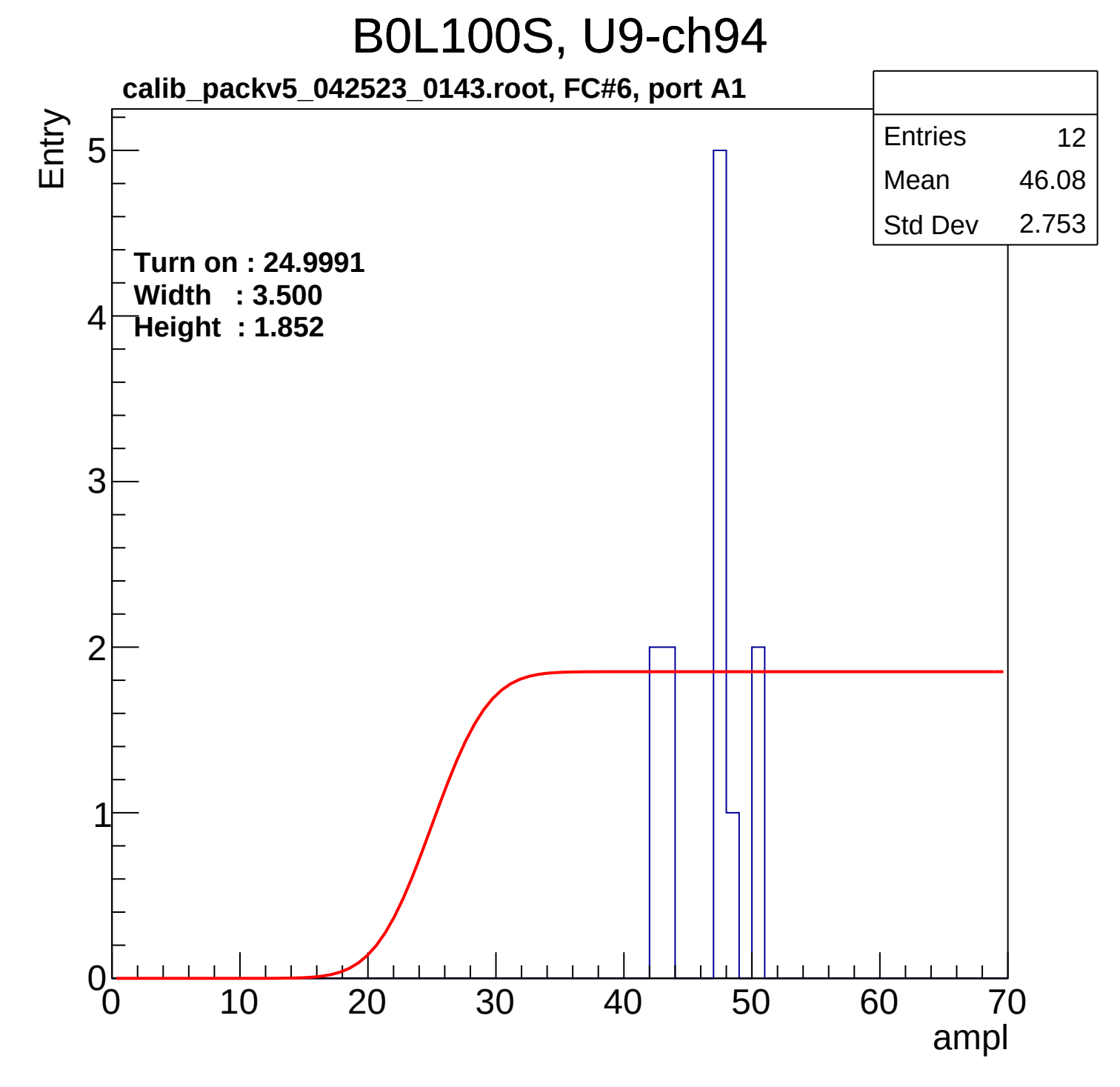
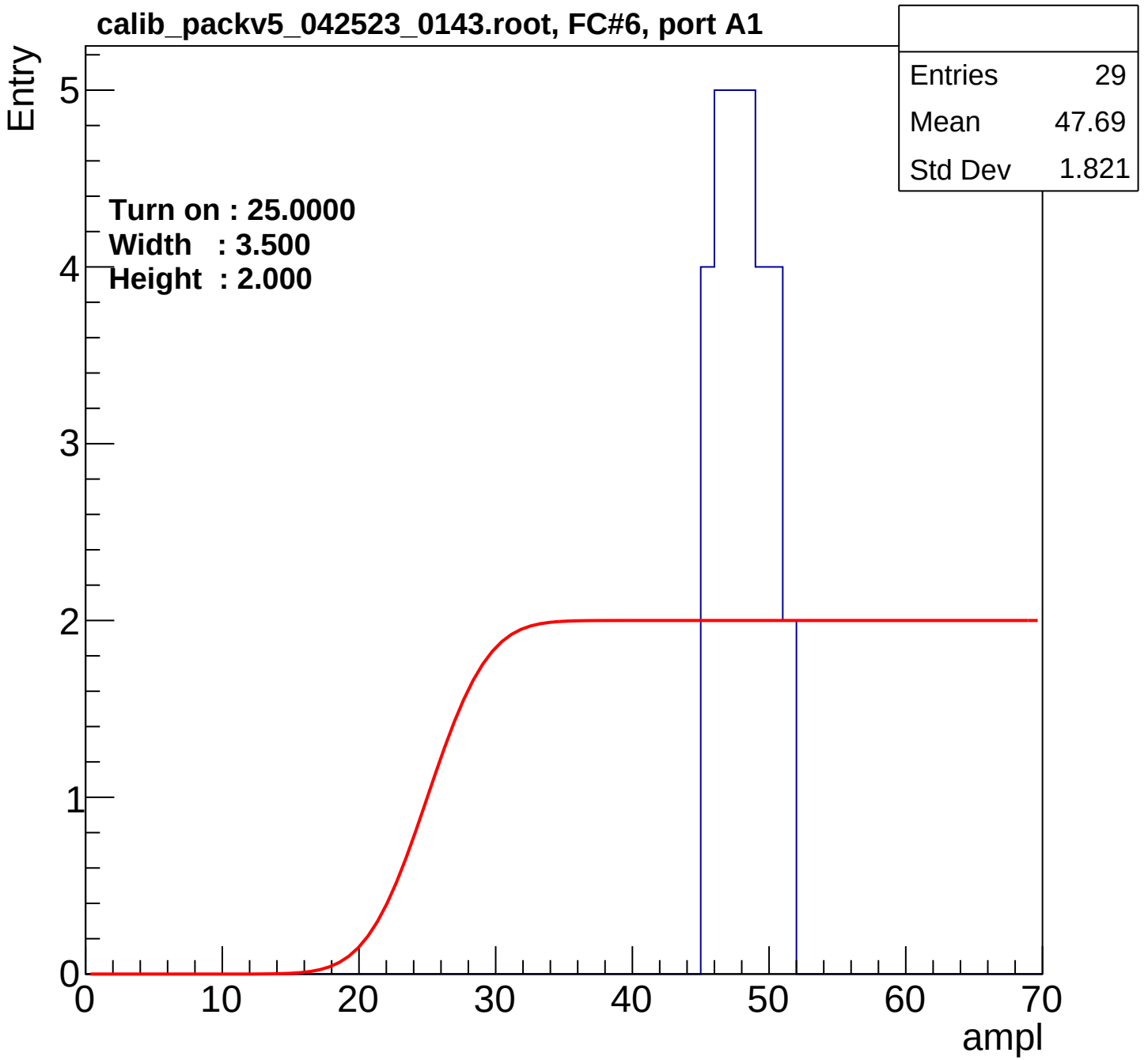
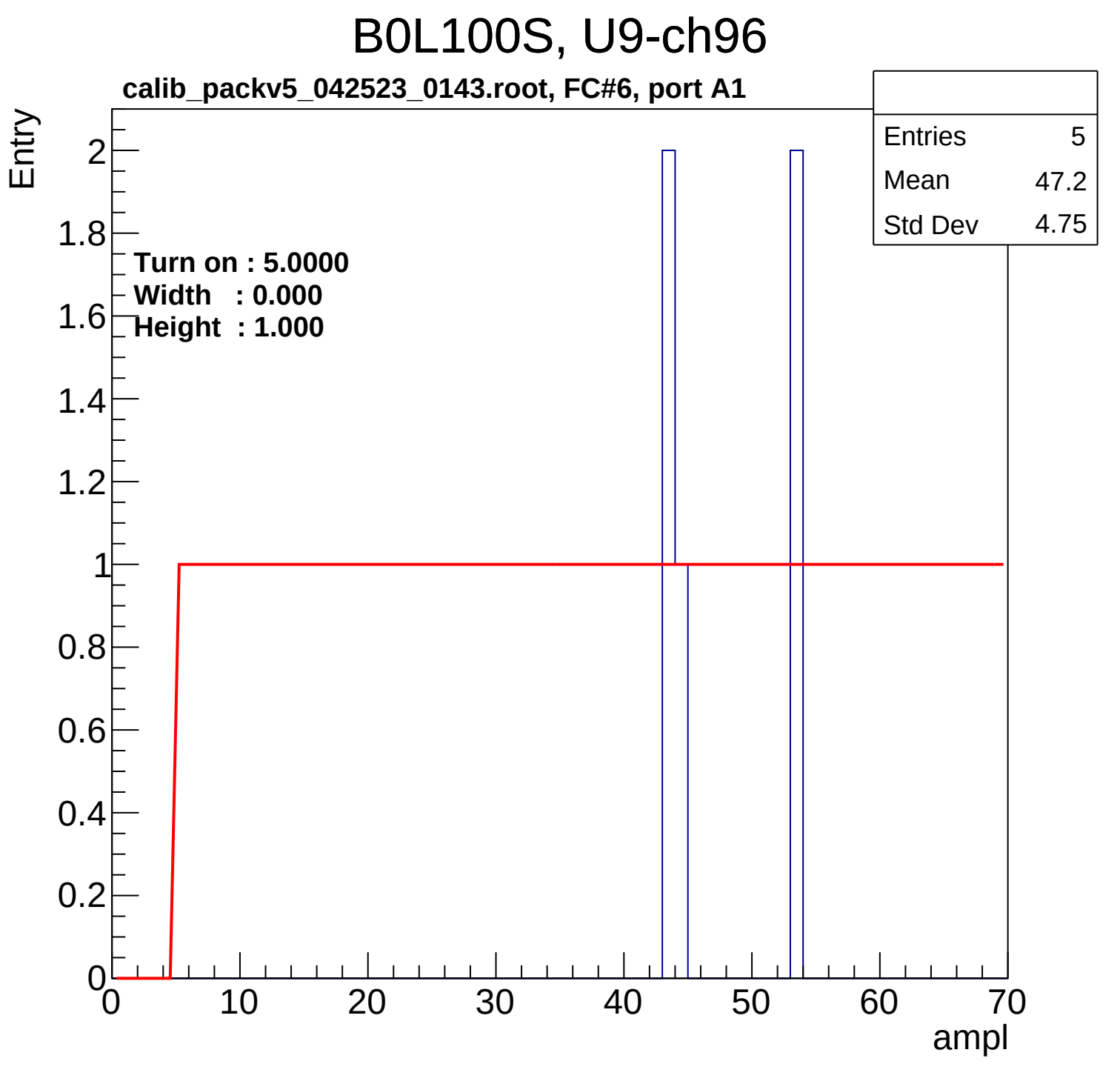
50
60
70
ampl


B0L100S, U9-ch94
calib_packv5_042523_0143.root, FC#6, port A1
Entries 12
Mean 46.08
Std Dev 2.753
Turn on : 24.9991
Width : 3.500
Height : 1.852
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B0L100S, U9-ch95
calib_packv5_042523_0143.root, FC#6, port A1
Entries 29
Mean 47.69
Std Dev 1.821
Turn on : 25.0000
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B0L100S, U9-ch96
calib_packv5_042523_0143.root, FC#6, port A1
Entries 5
Mean 47.2
Std Dev 4.75
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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20
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40
50
60
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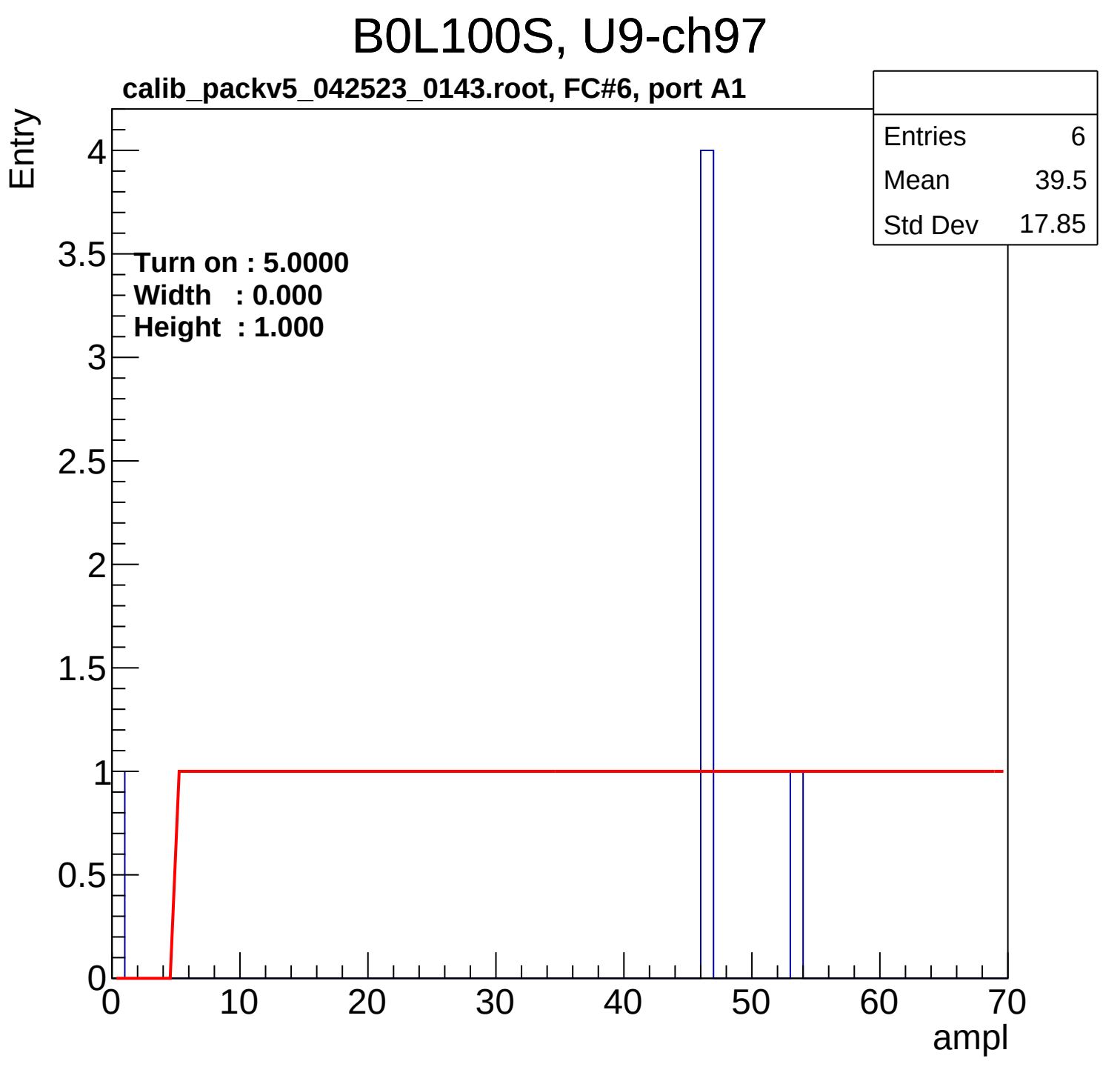
B0L100S, U9-ch97
calib_packv5_042523_0143.root, FC#6, port A1
Entries 6
Mean 39.5
Std Dev 17.85
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
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40
50
60
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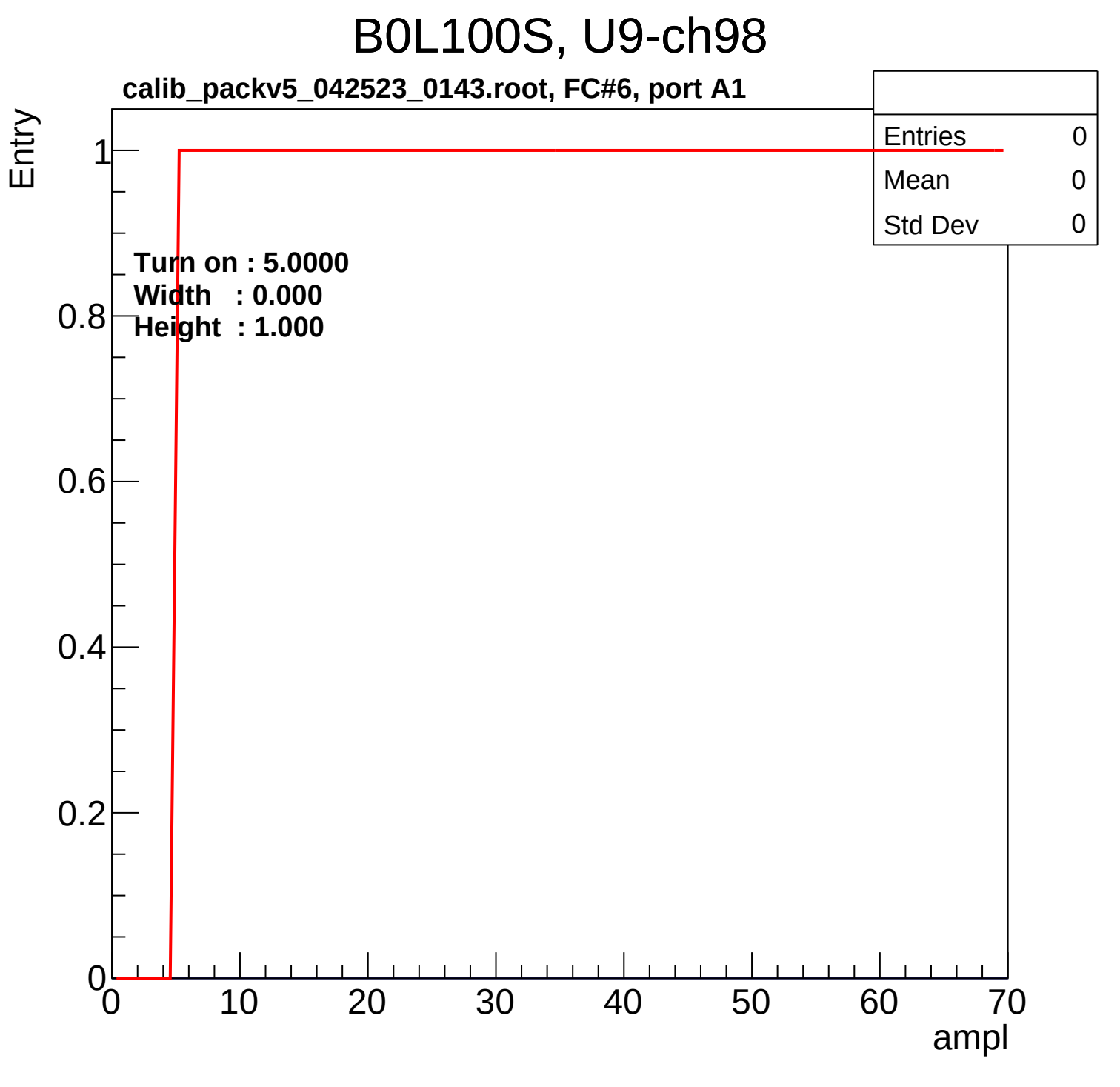
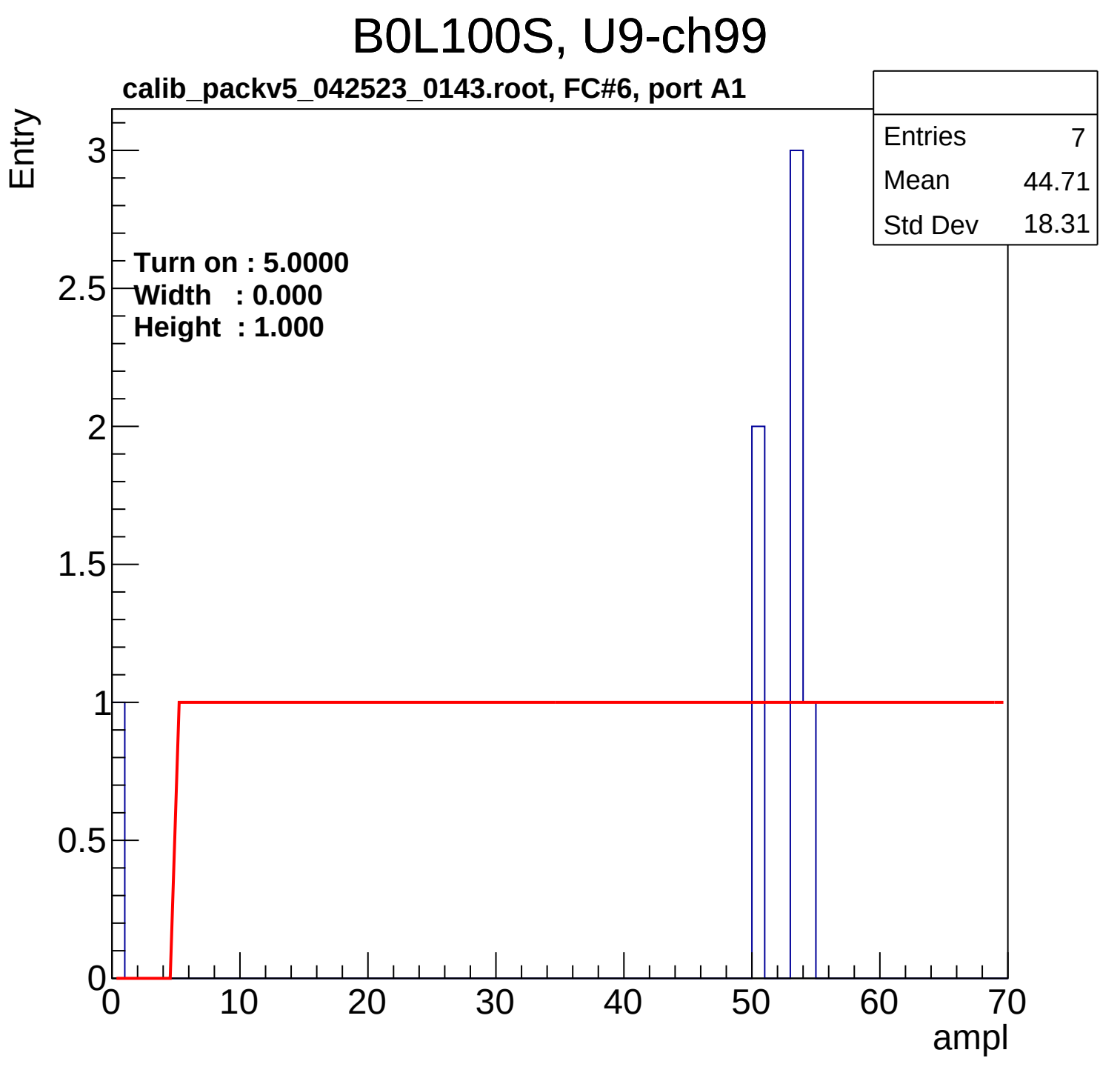

B0L100S, U9-ch98
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U9-ch99
calib_packv5_042523_0143.root, FC#6, port A1
Entries 7
Mean 44.71
Std Dev 18.31
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
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40
50
60
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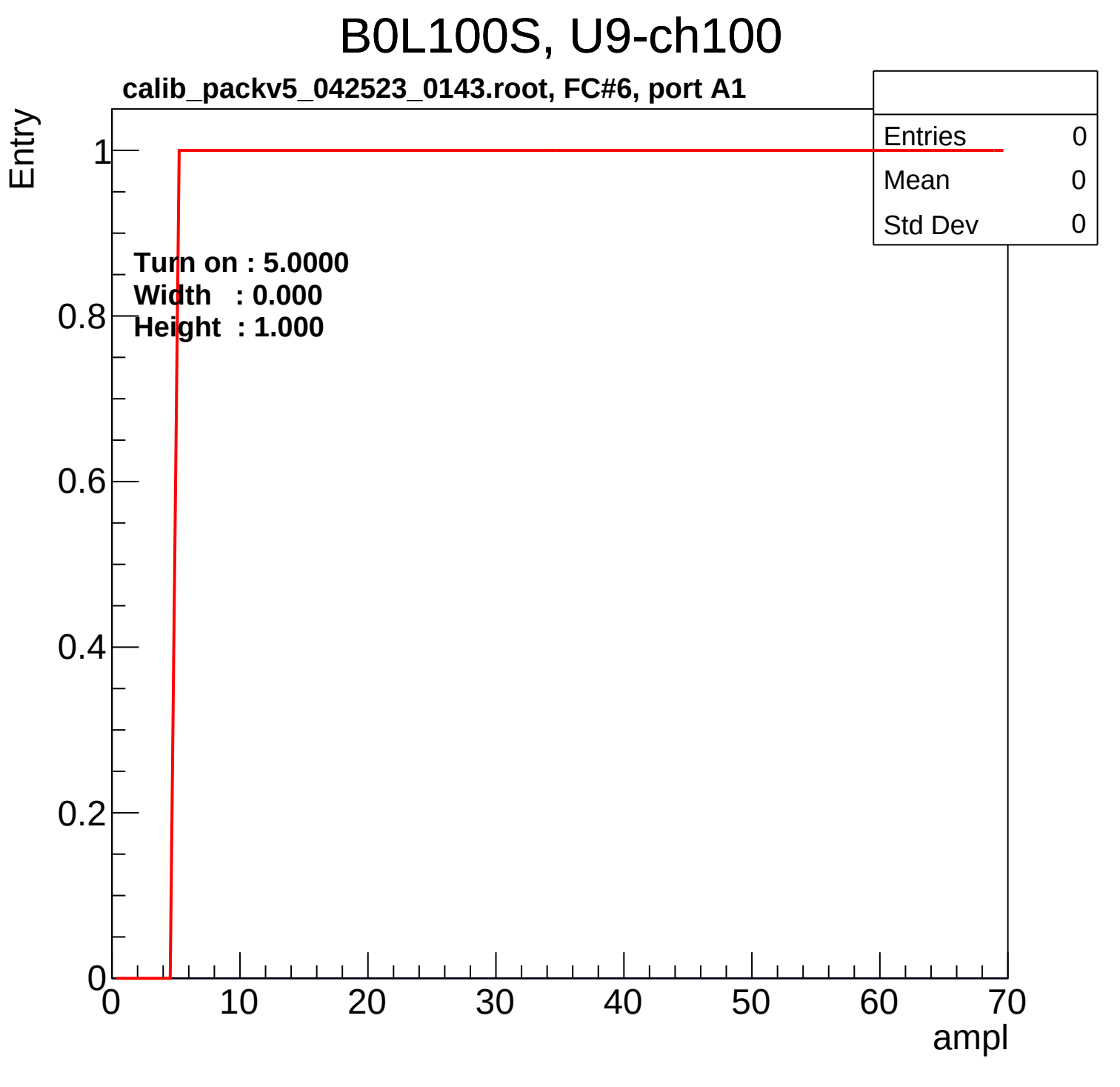
B0L100S, U9-ch100
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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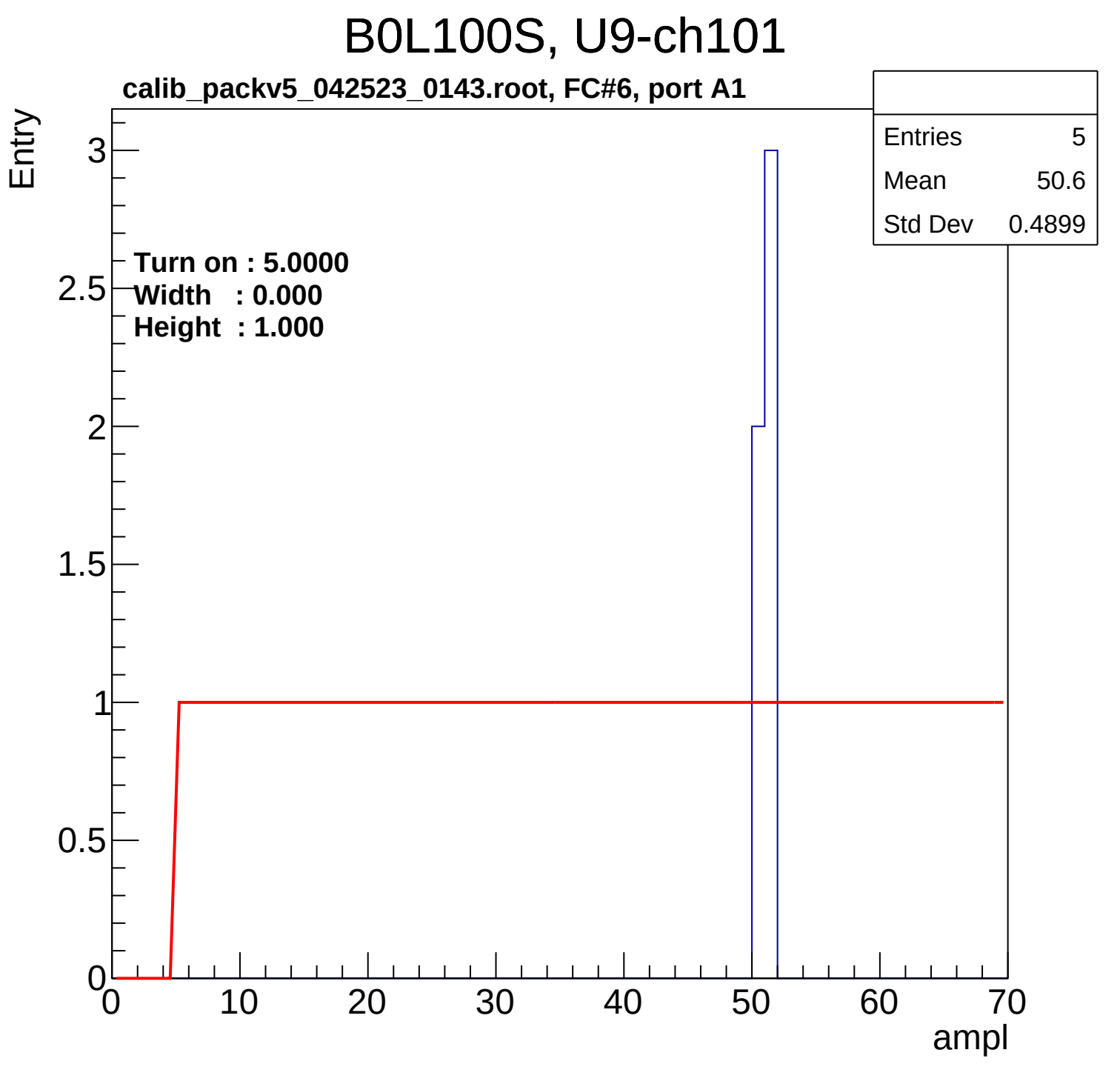
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U9-ch101
calib_packv5_042523_0143.root, FC#6, port A1
Entries 5
Mean 50.6
Std Dev 0.4899
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
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20
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40
50
60
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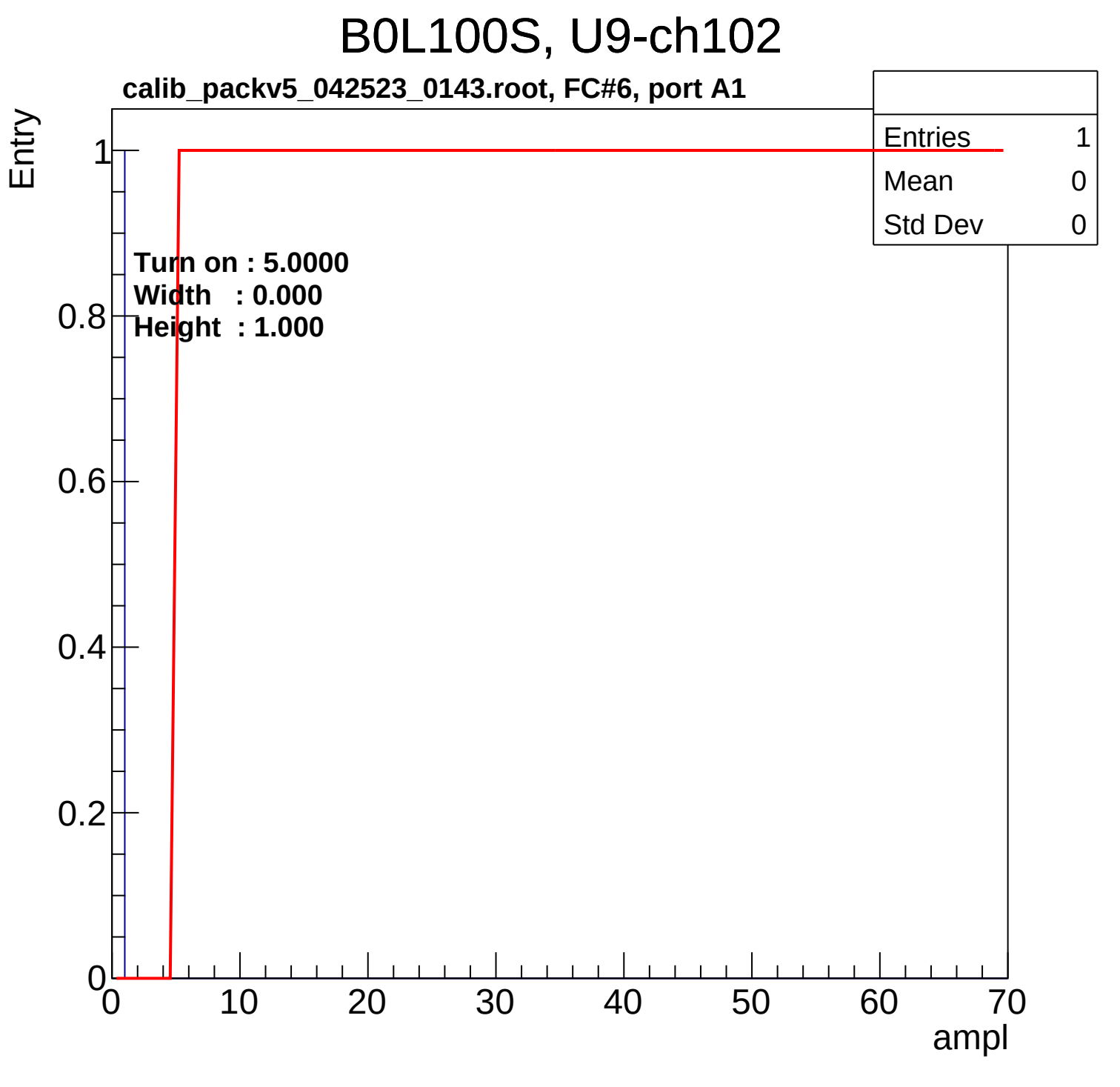
B0L100S, U9-ch102
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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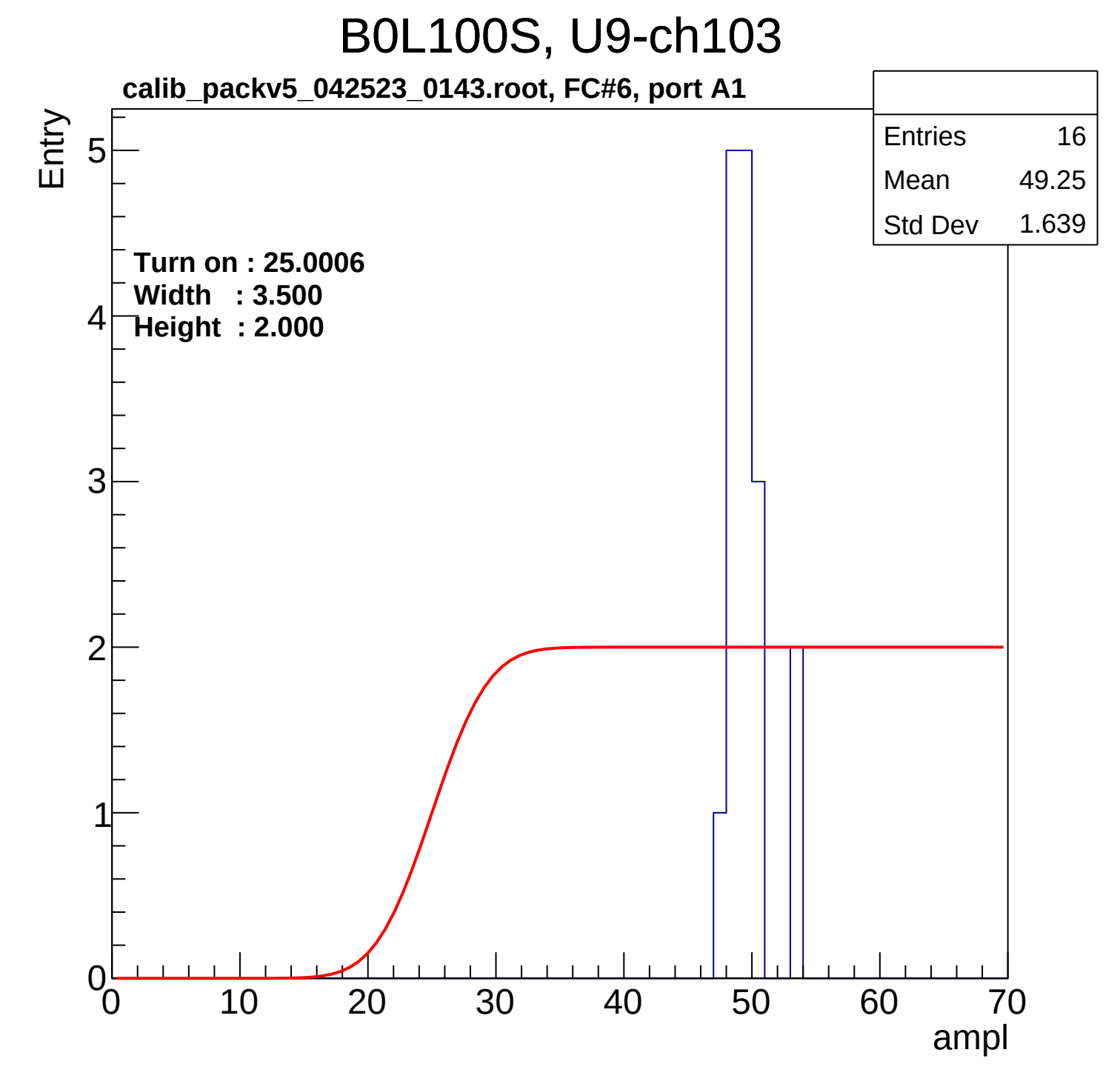
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U9-ch103
calib_packv5_042523_0143.root, FC#6, port A1
Entries 16
Mean 49.25
Std Dev 1.639
Turn on : 25.0006
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
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20
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60
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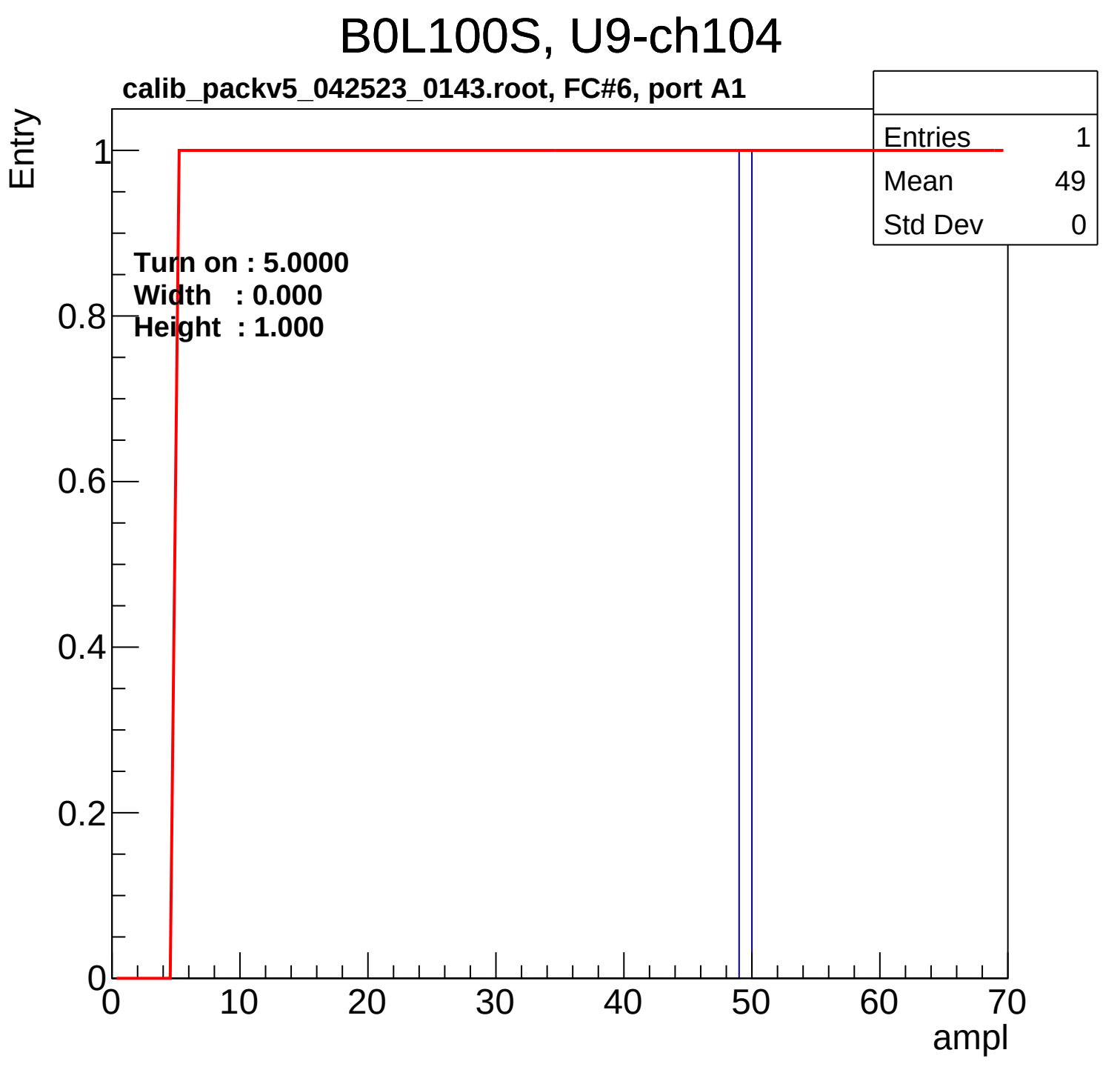
B0L100S, U9-ch104
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 49
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.2
0.4
0.6
0.8
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0
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60
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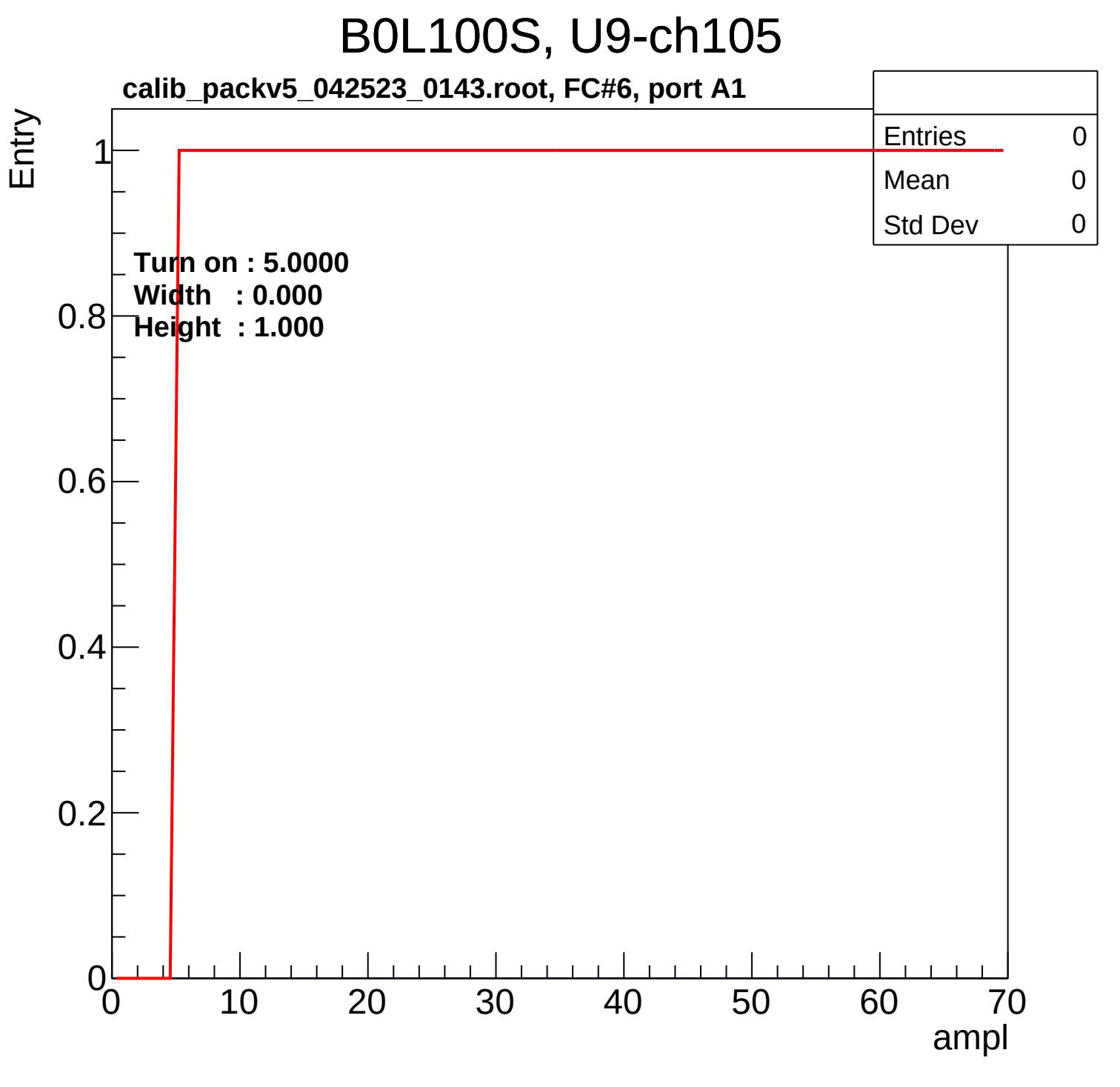
B0L100S, U9-ch105
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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0.4
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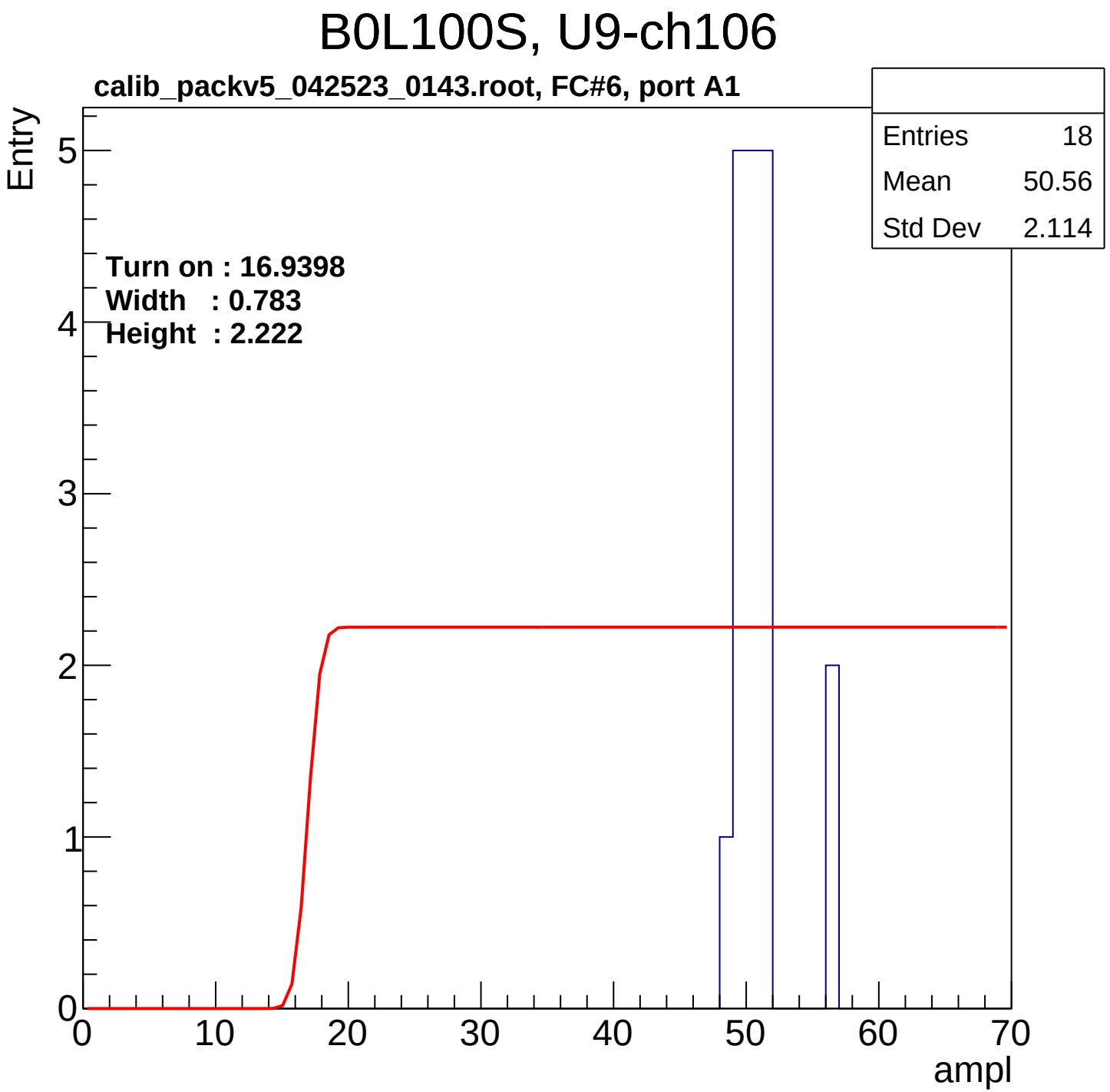
ampl


B0L100S, U9-ch106
calib_packv5_042523_0143.root, FC#6, port A1
Entries 18
Mean 50.56
Std Dev 2.114
Turn on : 16.9398
Width : 0.783
Height : 2.222
Entry
ampl
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4
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0
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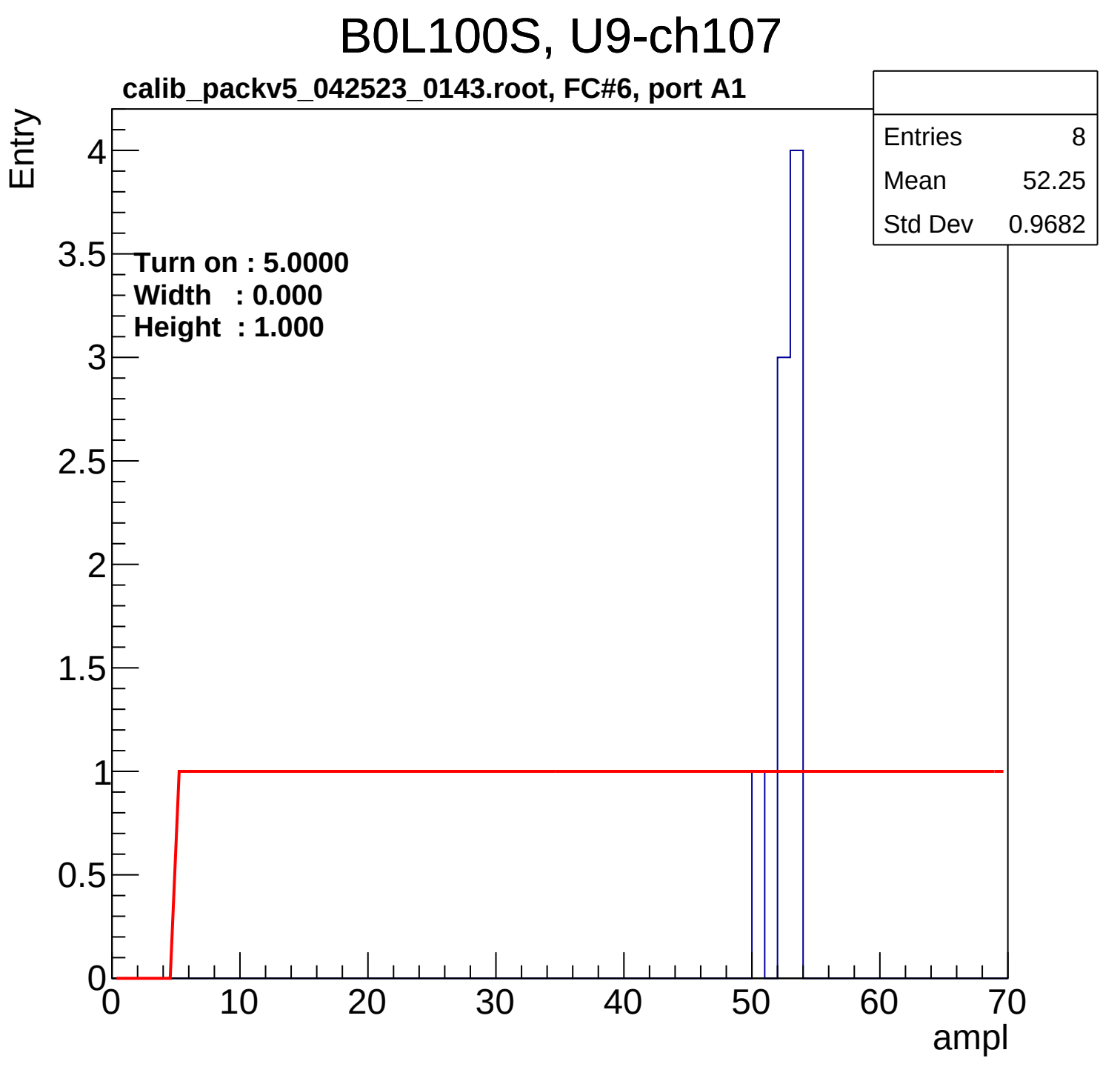
B0L100S, U9-ch107
calib_packv5_042523_0143.root, FC#6, port A1
Entries 8
Mean 52.25
Std Dev 0.9682
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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1
1.5
2
2.5
3
3.5
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0
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60
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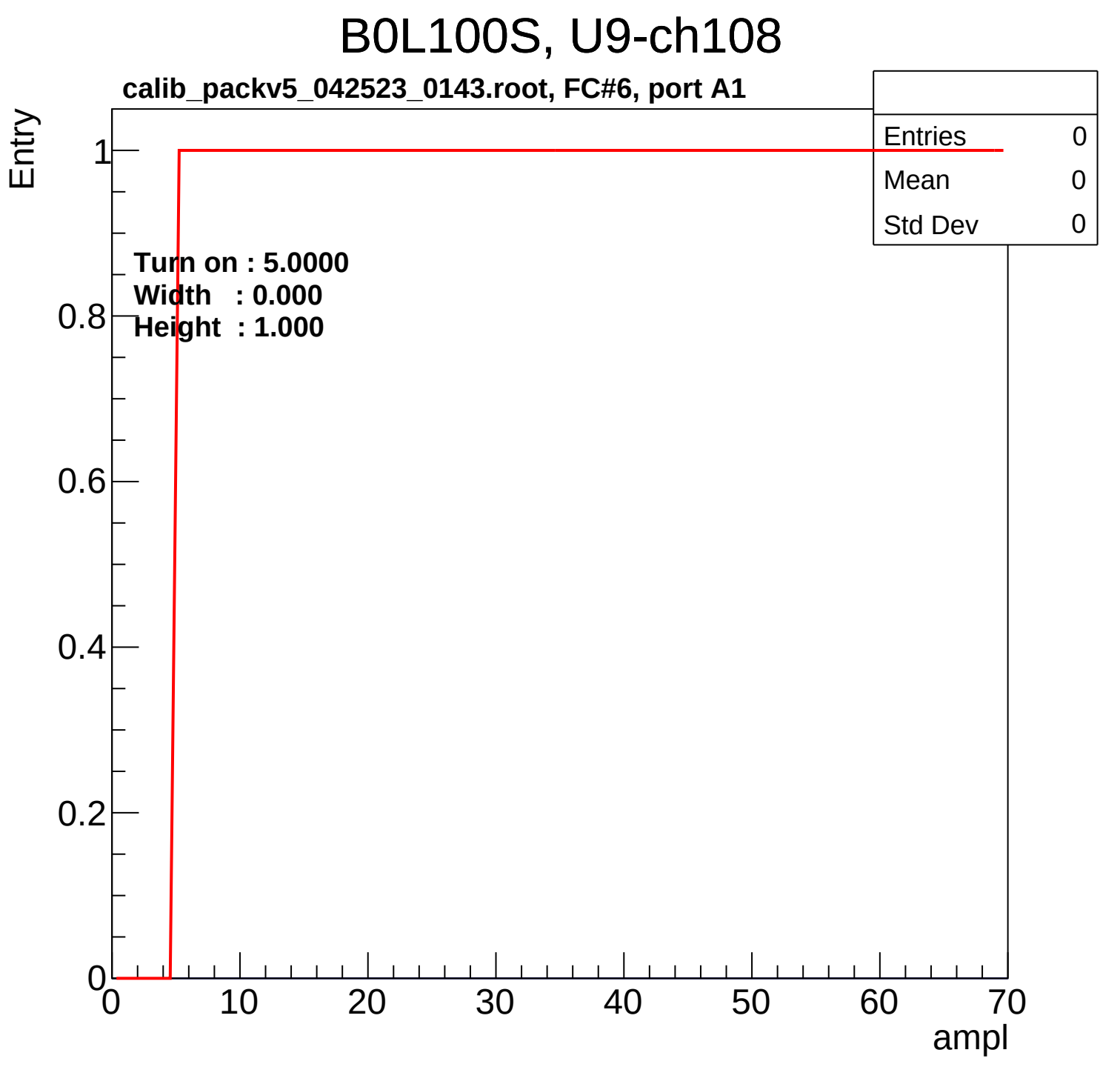
B0L100S, U9-ch108
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
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Height : 1.000
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0.6
0.4
0.2
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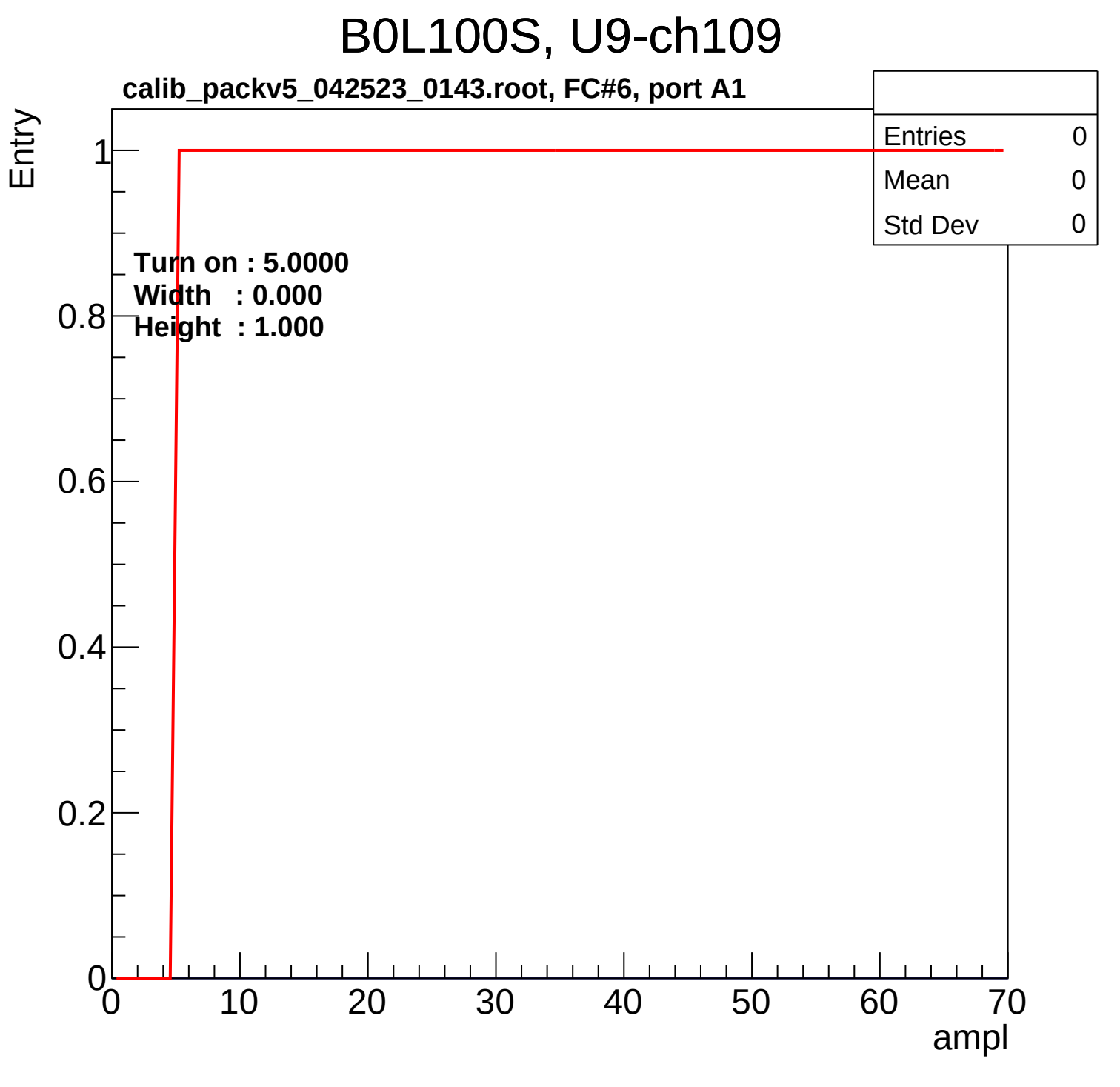
70
ampl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calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
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50
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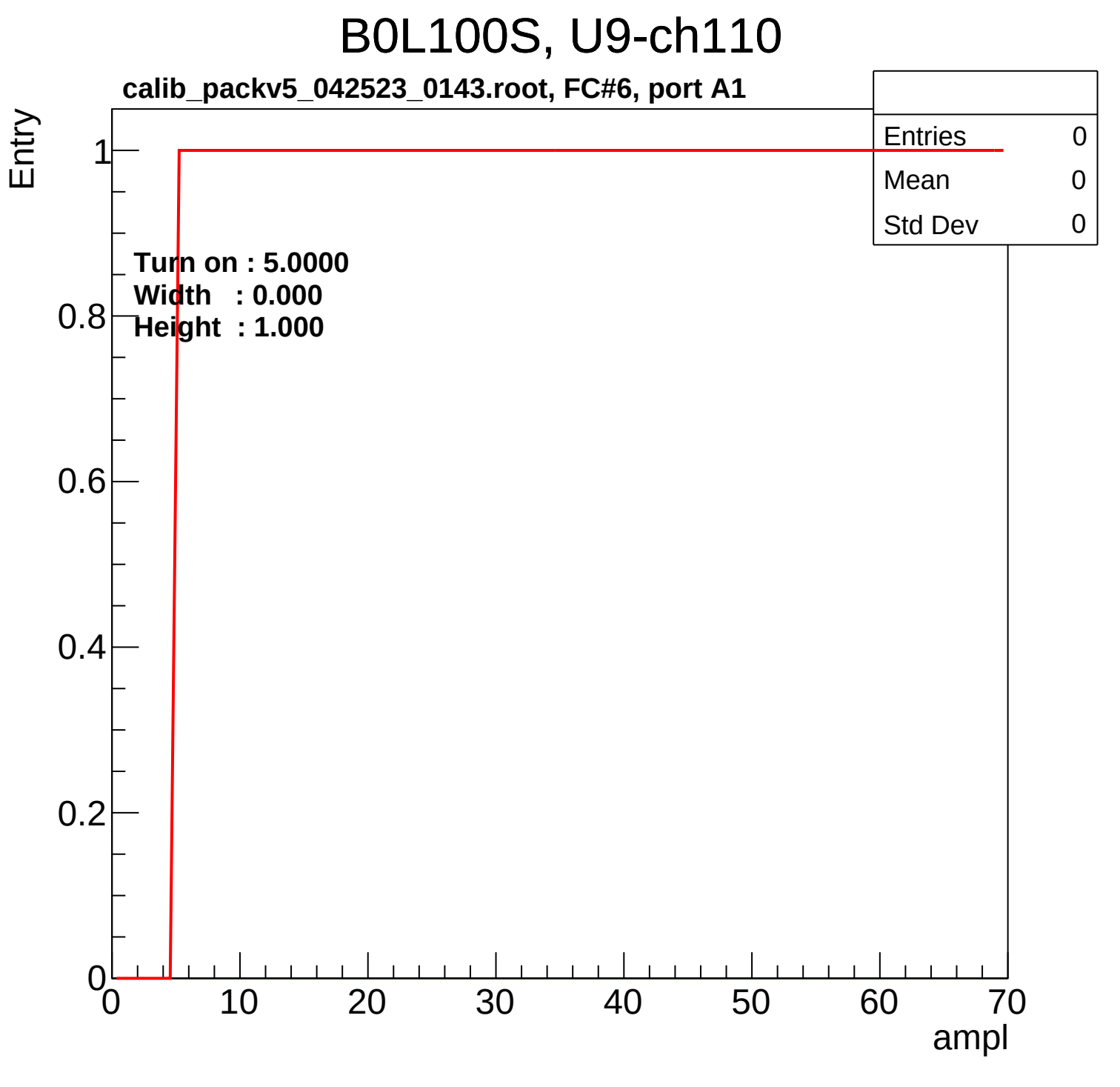
70
ampl


B0L100S, U9-ch110
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
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0.6
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0.2
0
0
10
20
30
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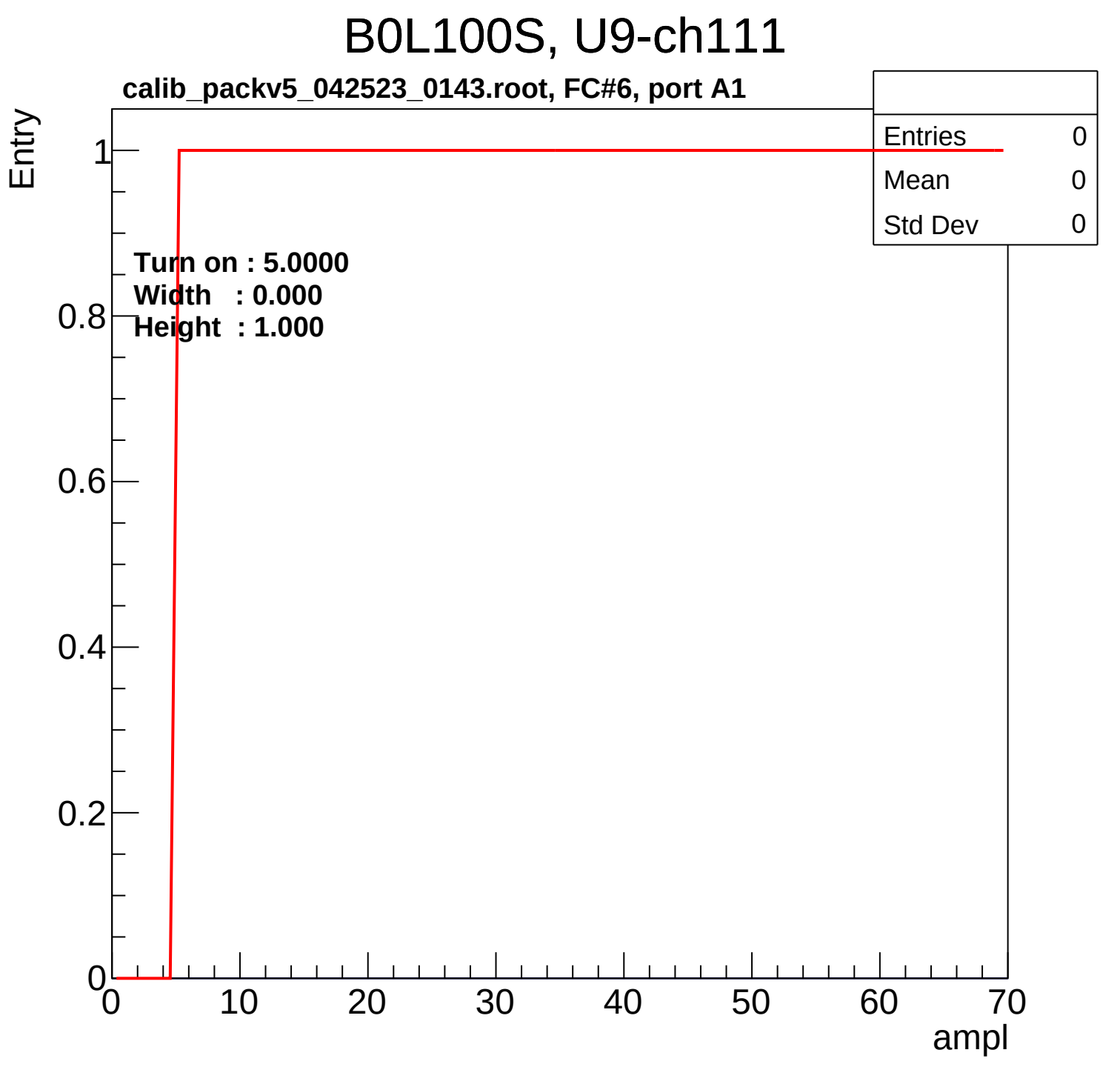
50
60
70
ampl


B0L100S, U9-ch111
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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0.4
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30
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50
60
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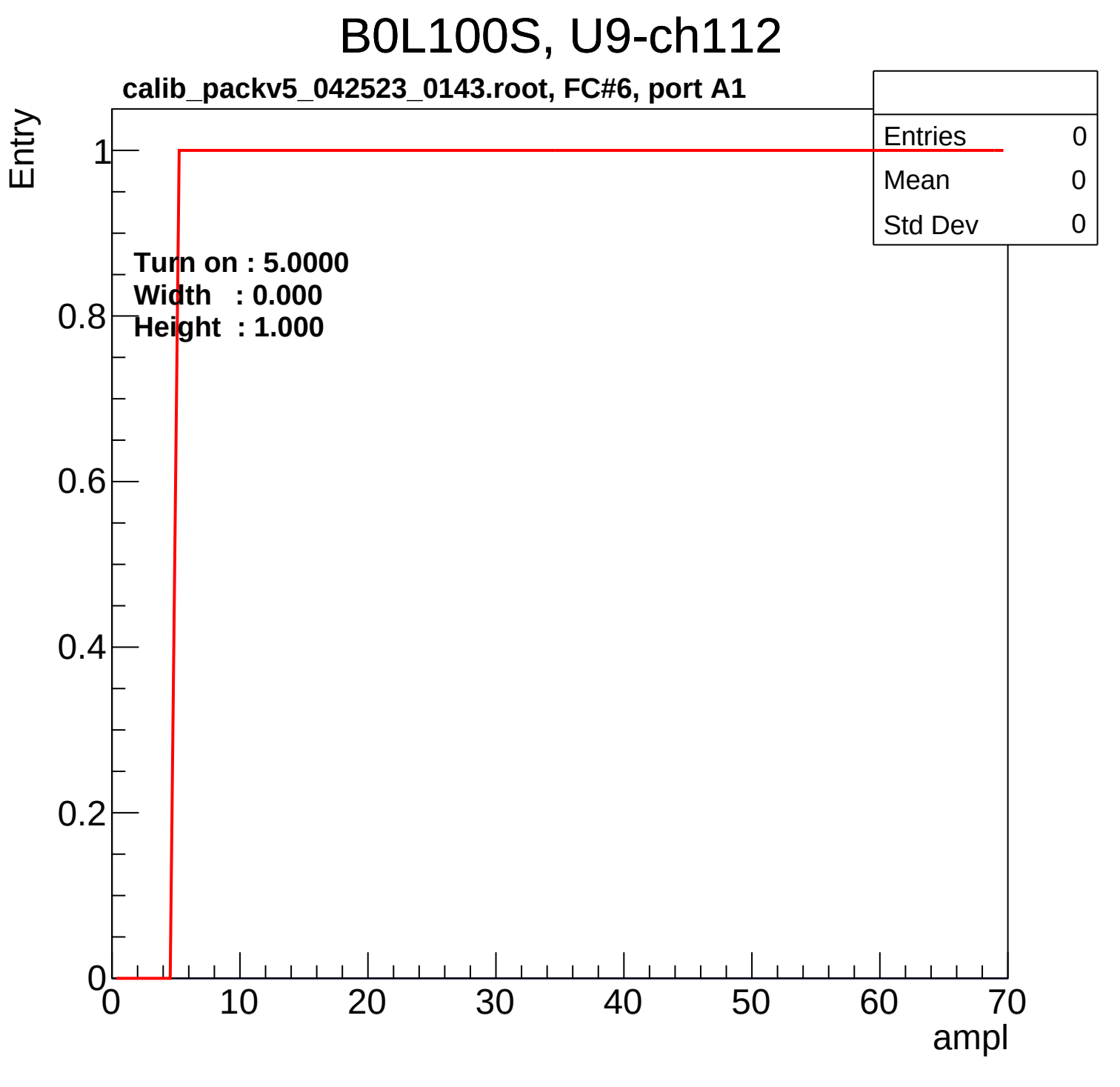
ampl


B0L100S, U9-ch112
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
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0.4
0.2
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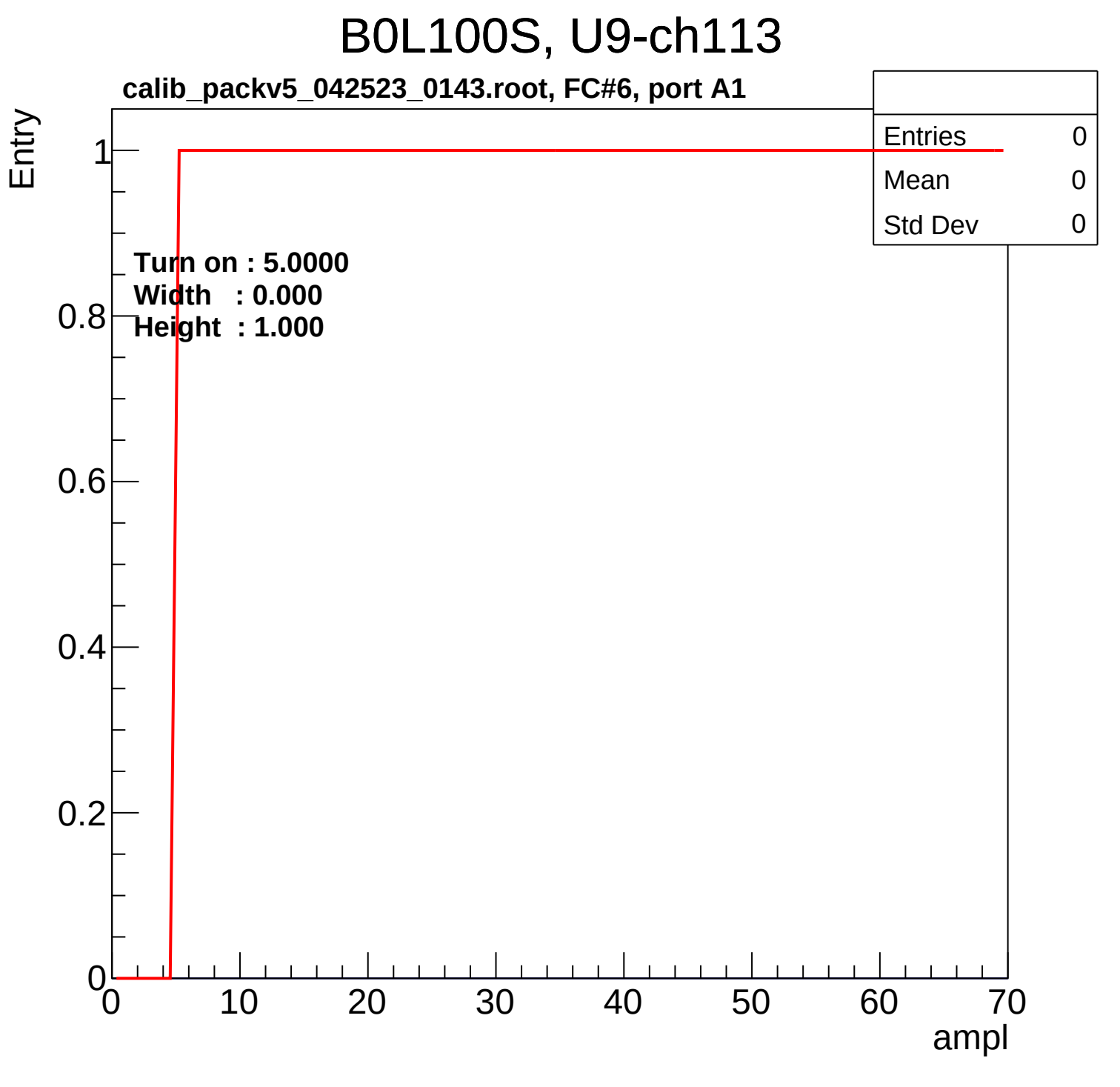
0
10
20
30
40
50
60
70
ampl


B0L100S, U9-ch113
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
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0.4
0.2
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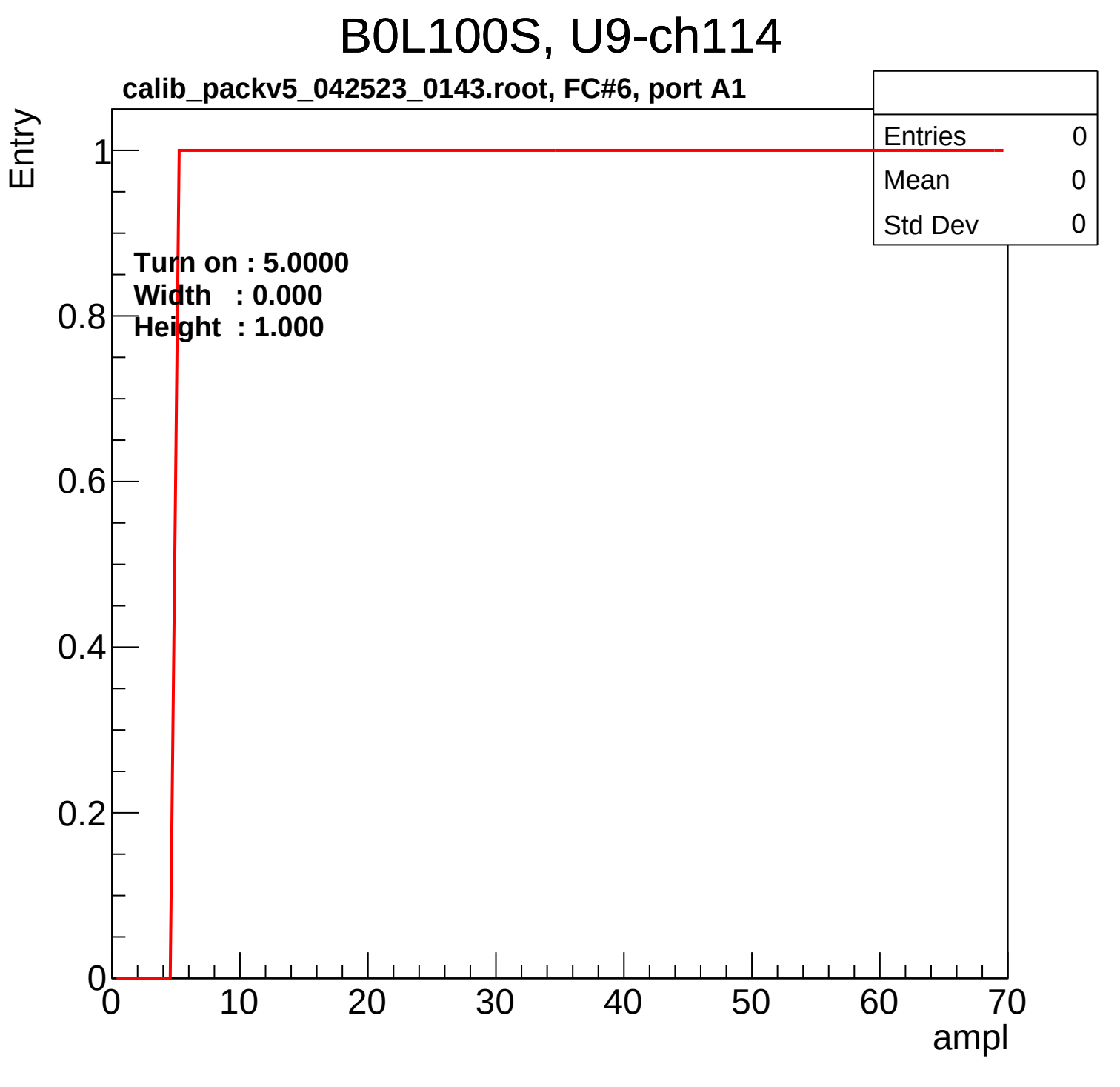
ampl


B0L100S, U9-ch114
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Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
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Height : 1.000
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0.4
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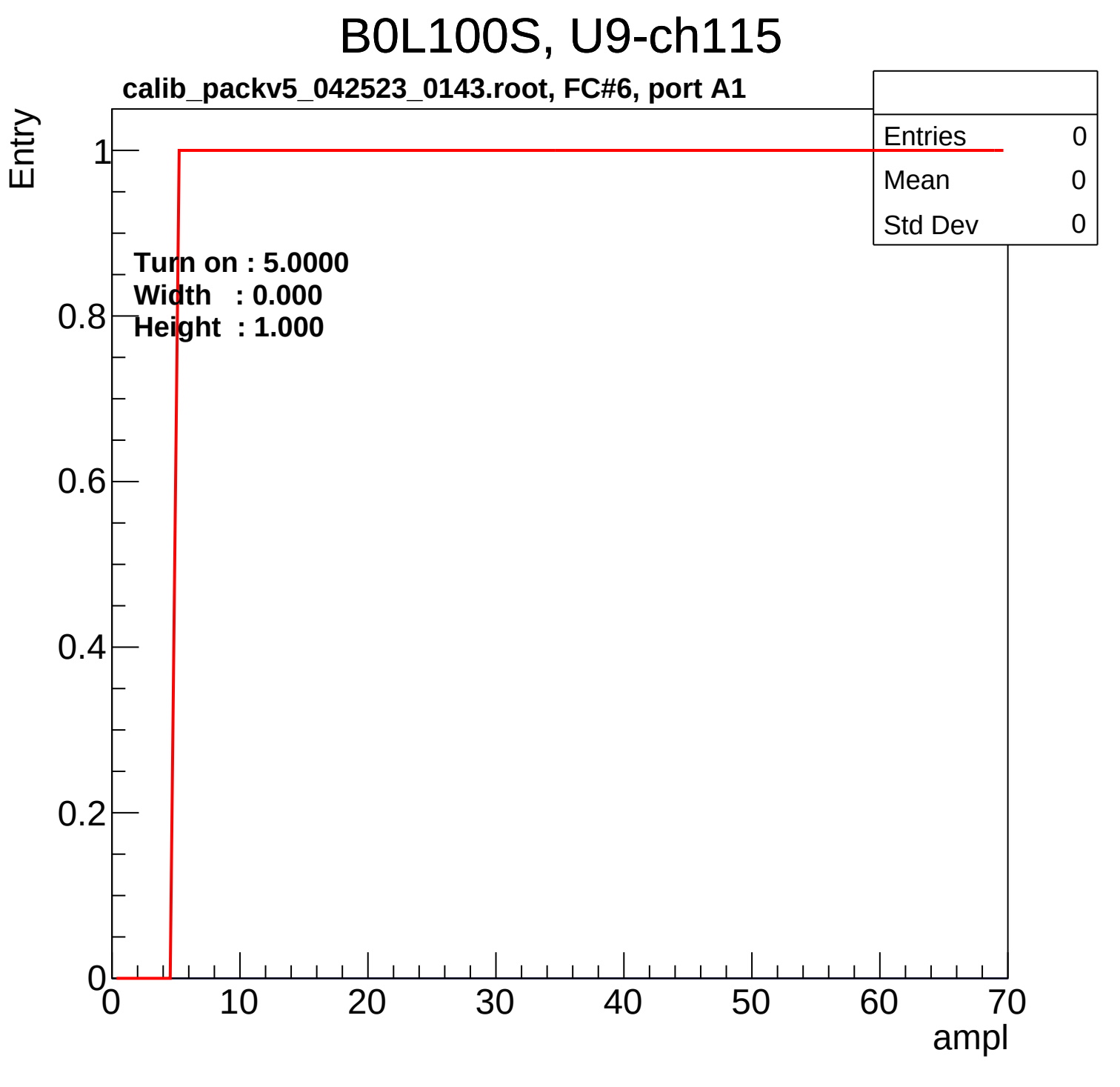
ampl


B0L100S, U9-ch115
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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0.6
0.4
0.2
0
0
10
20
30
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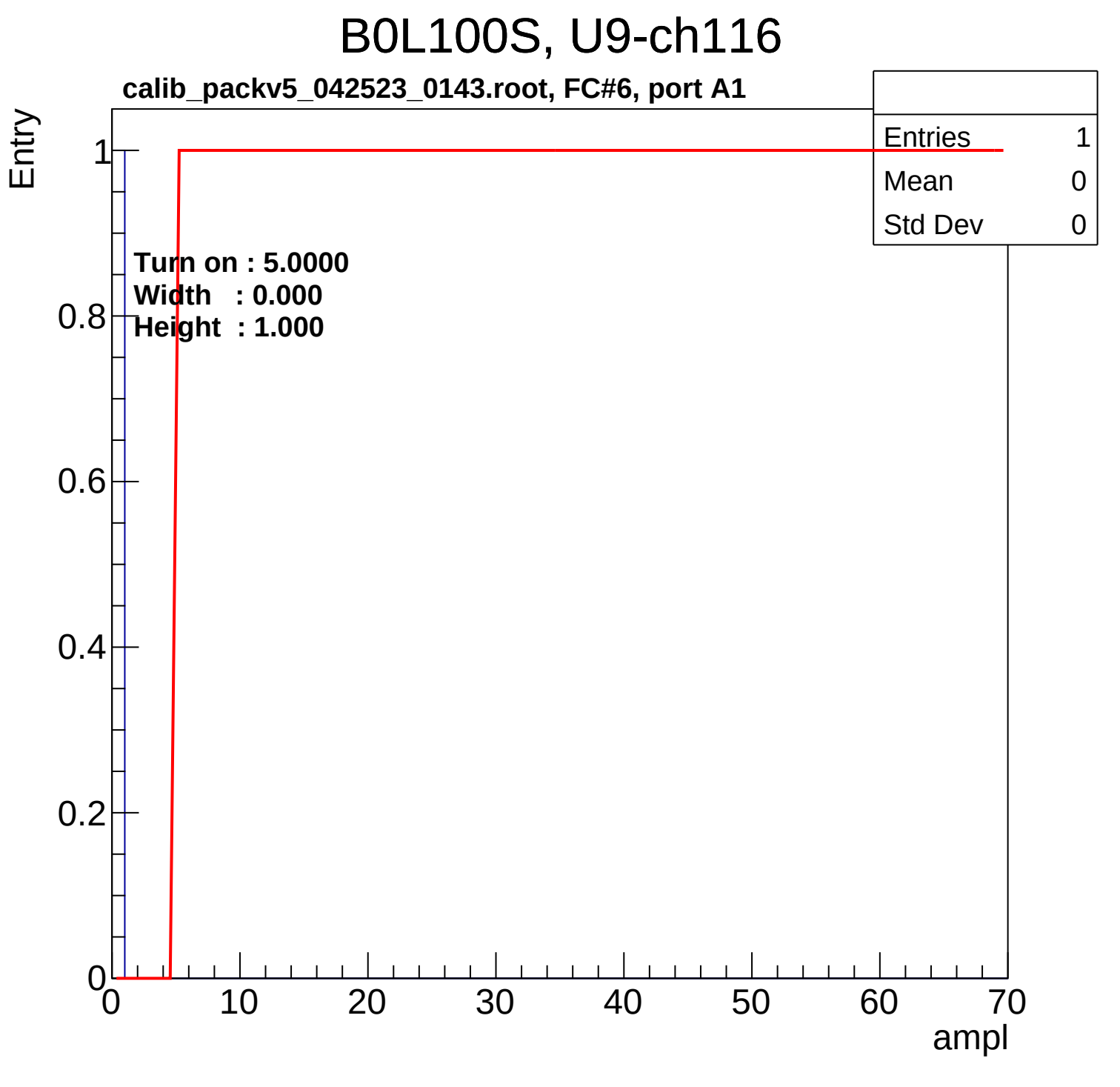
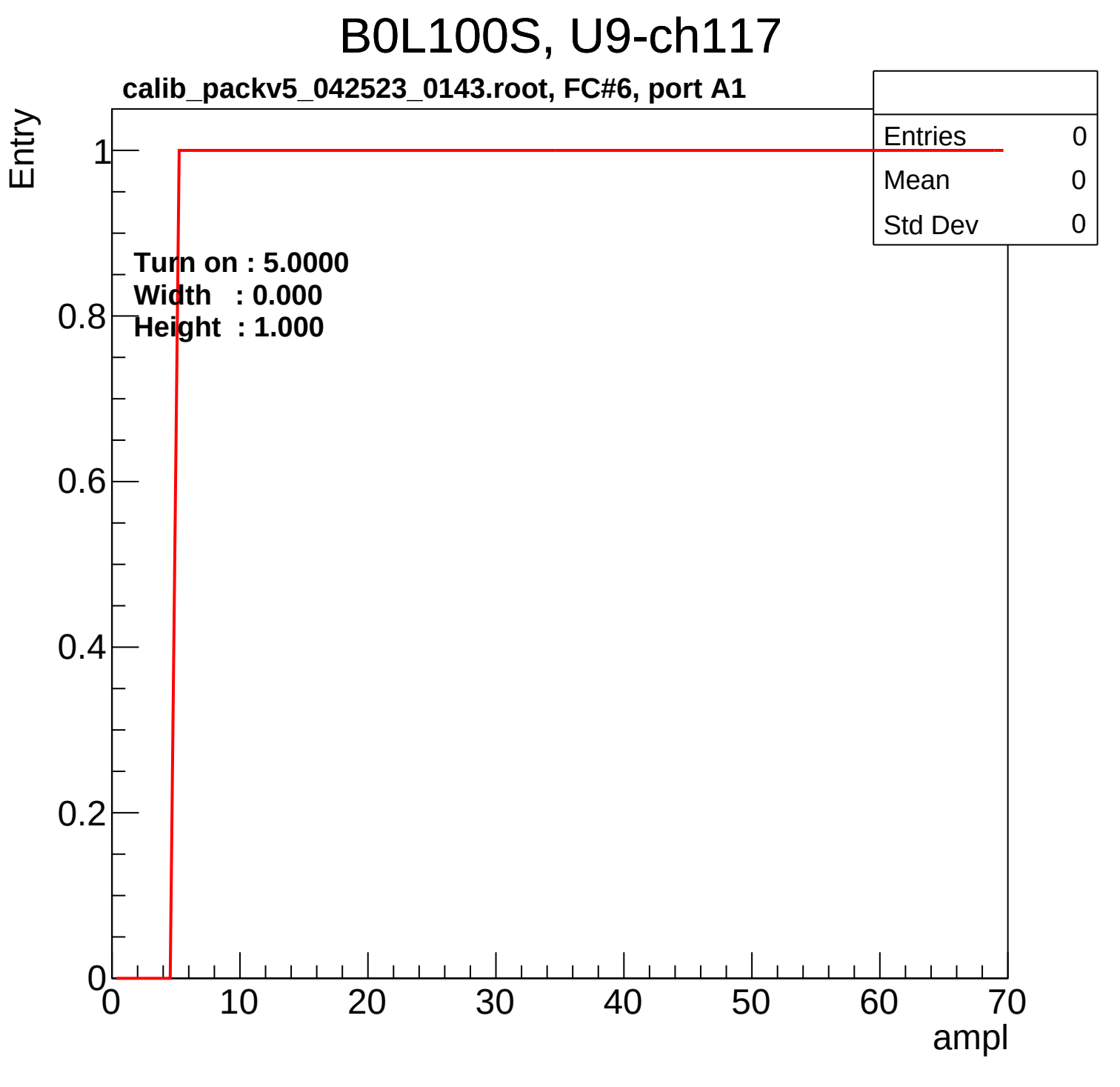
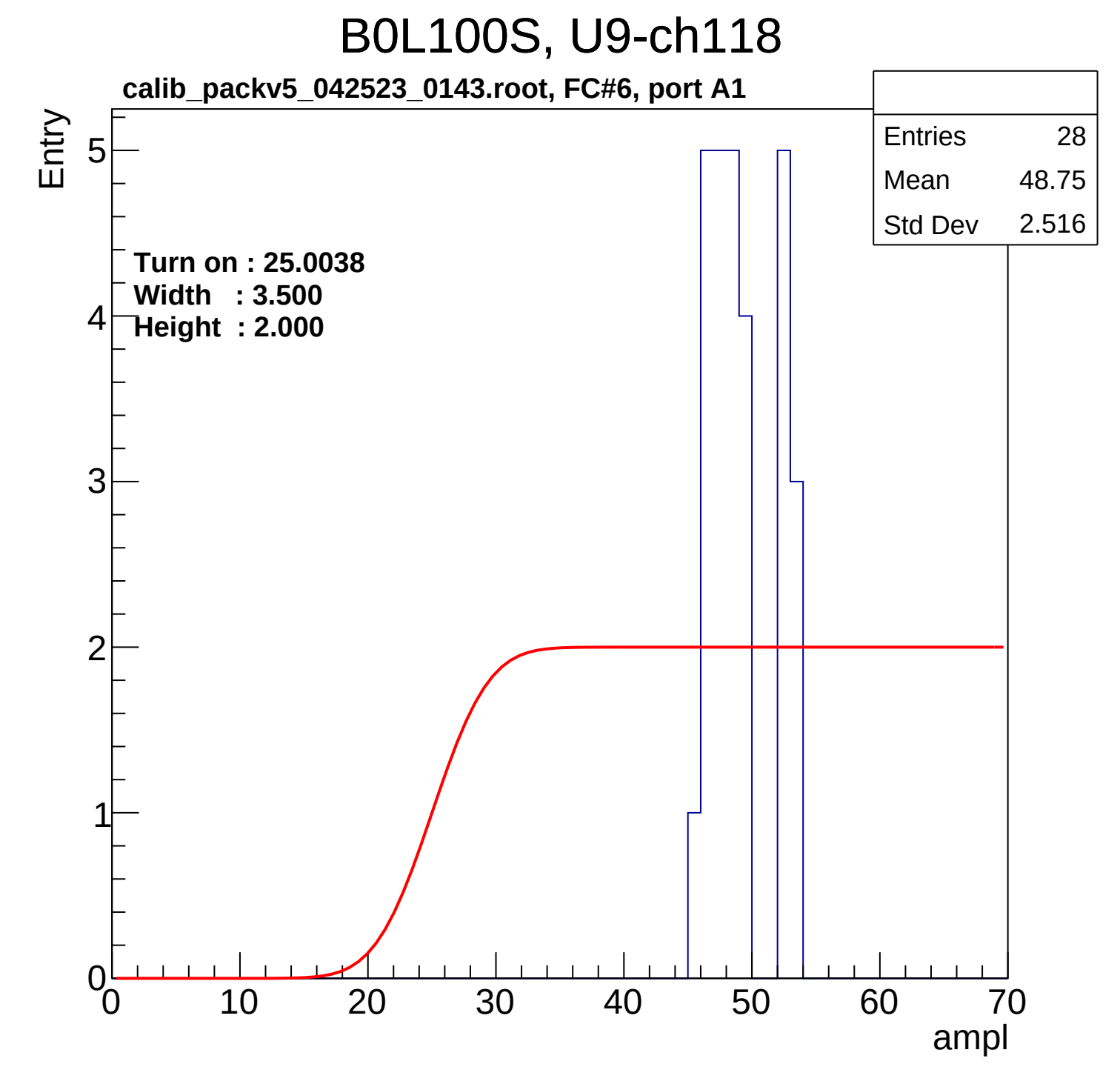
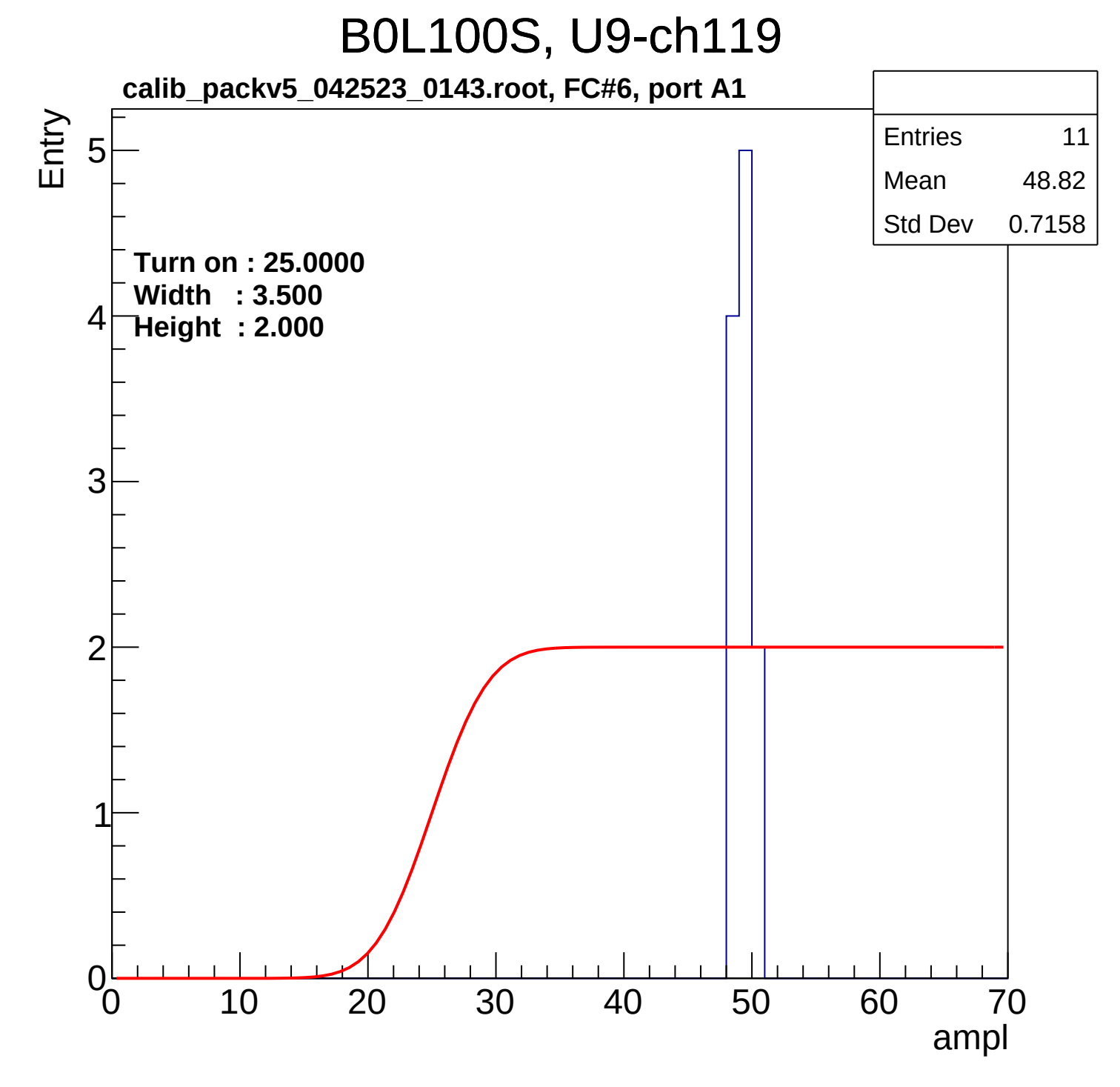
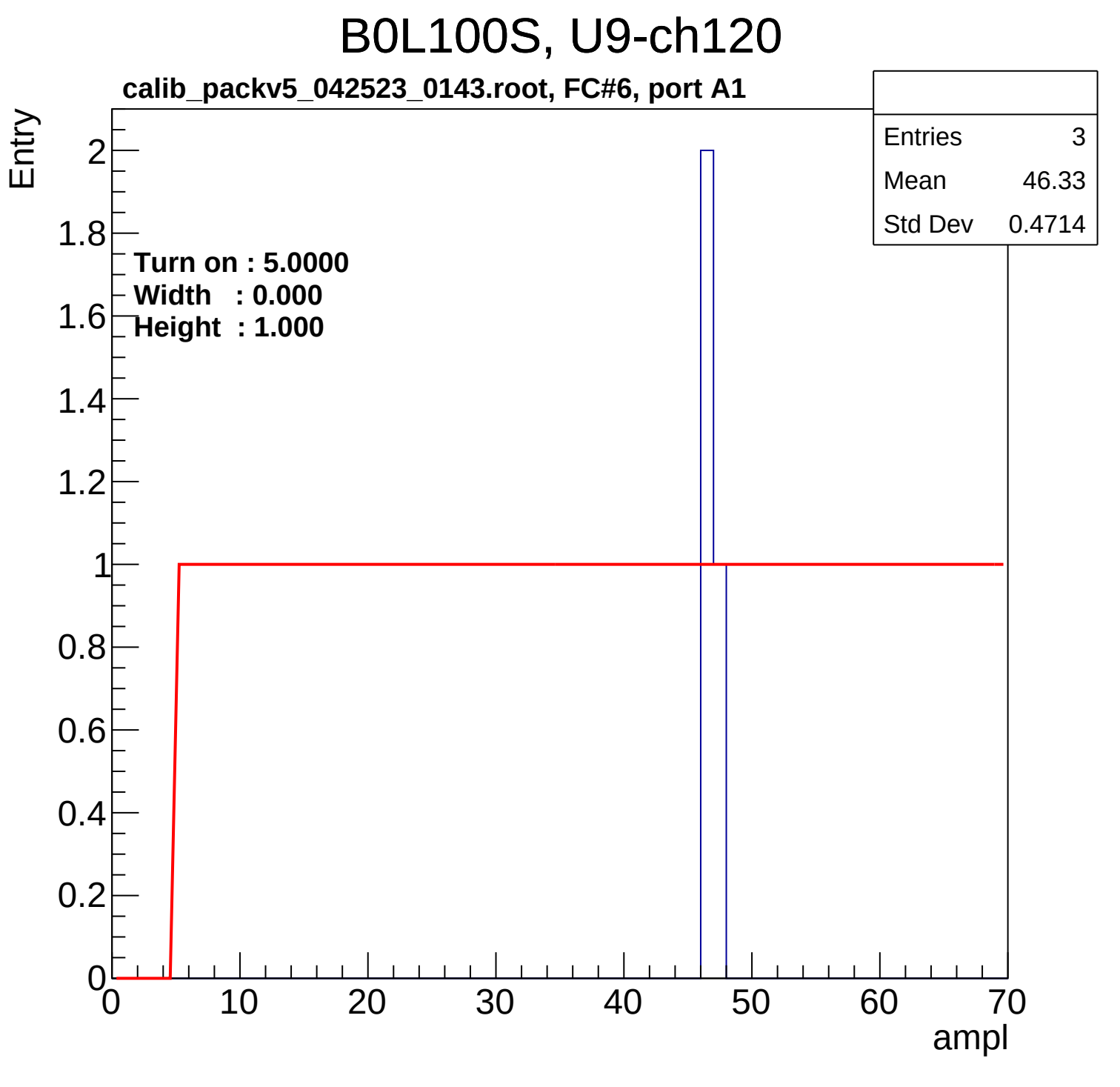
50
60
70
ampl

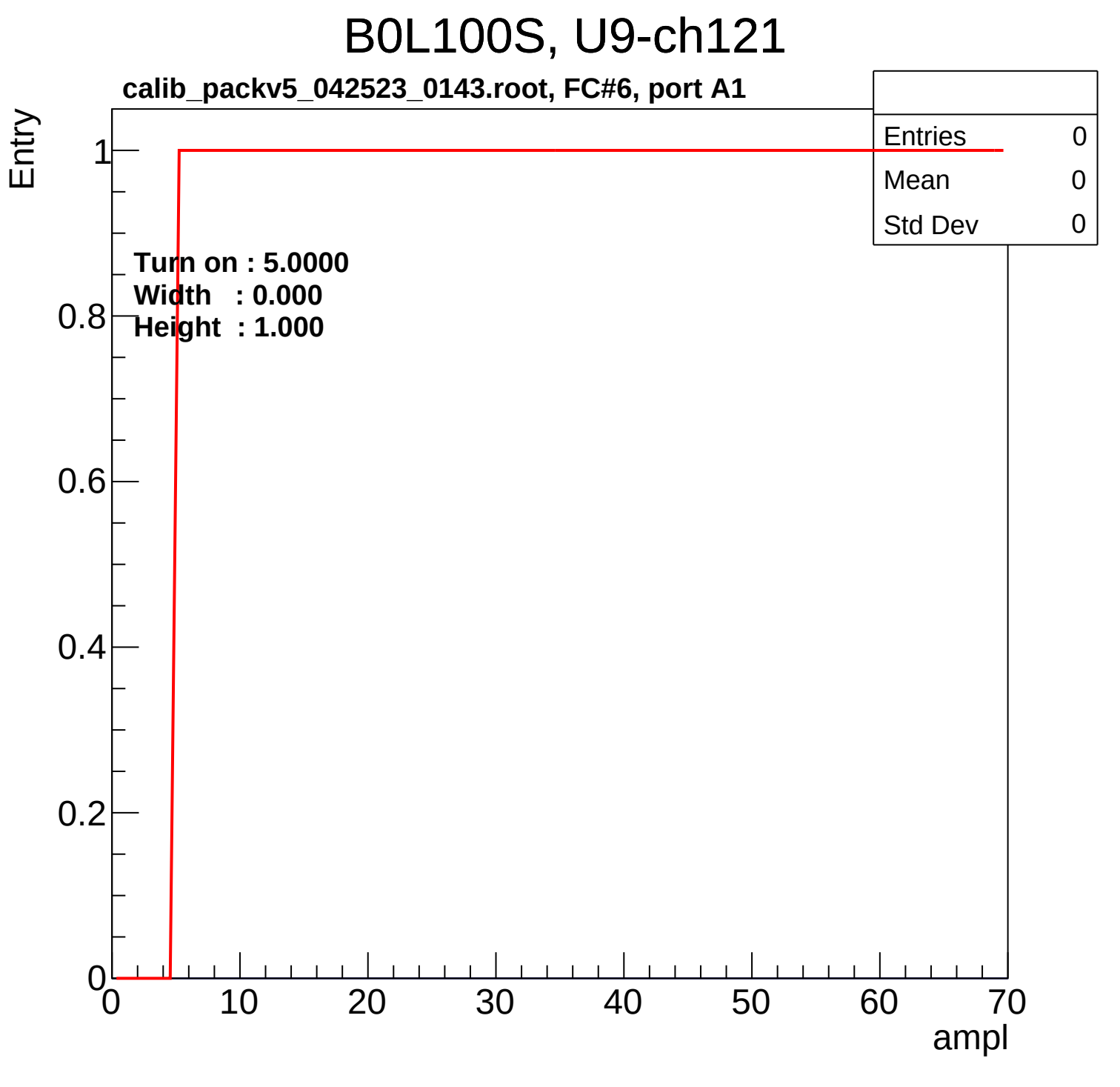

B0L100S, U9-ch116
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

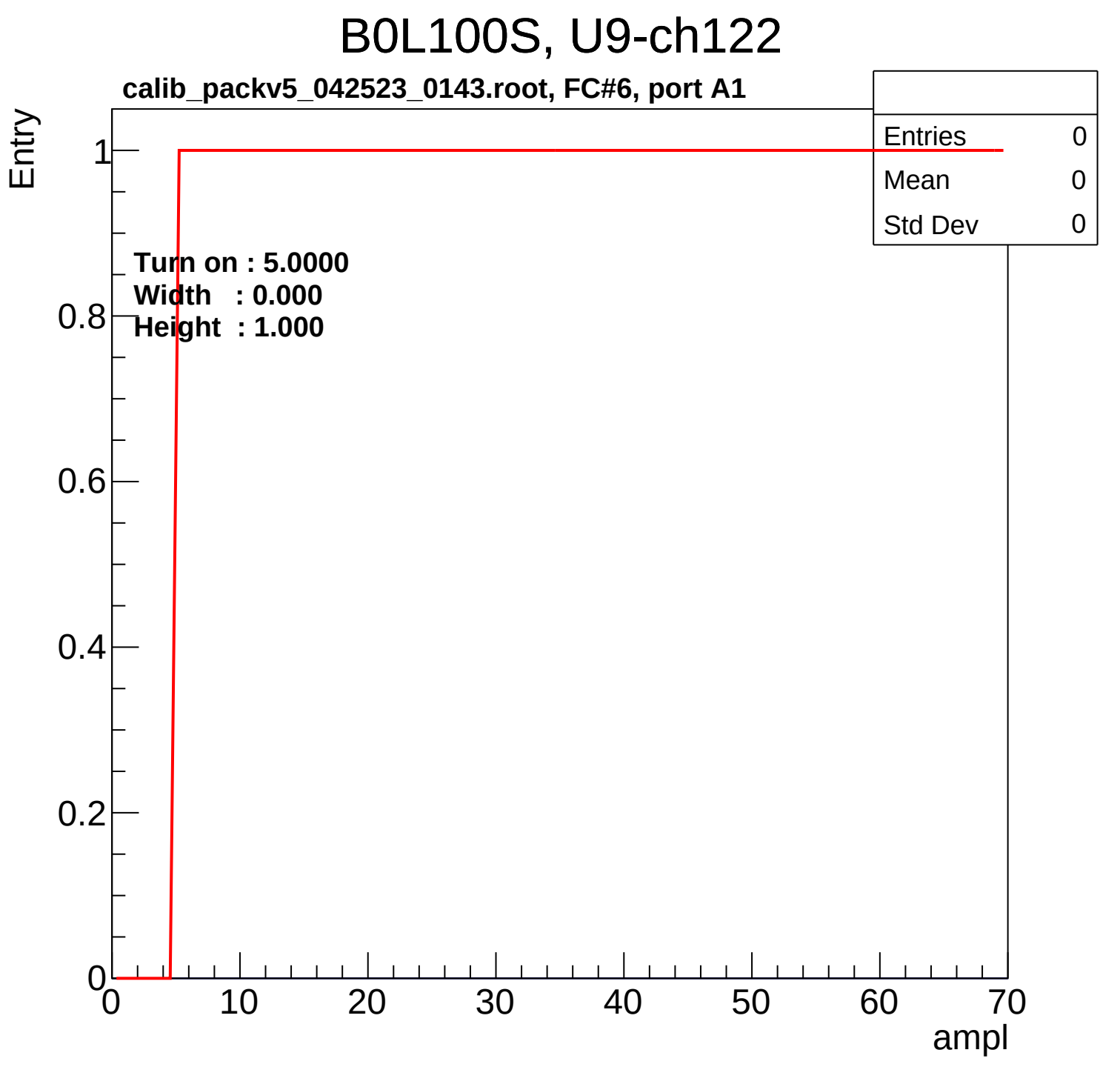

B0L100S, U9-ch117
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

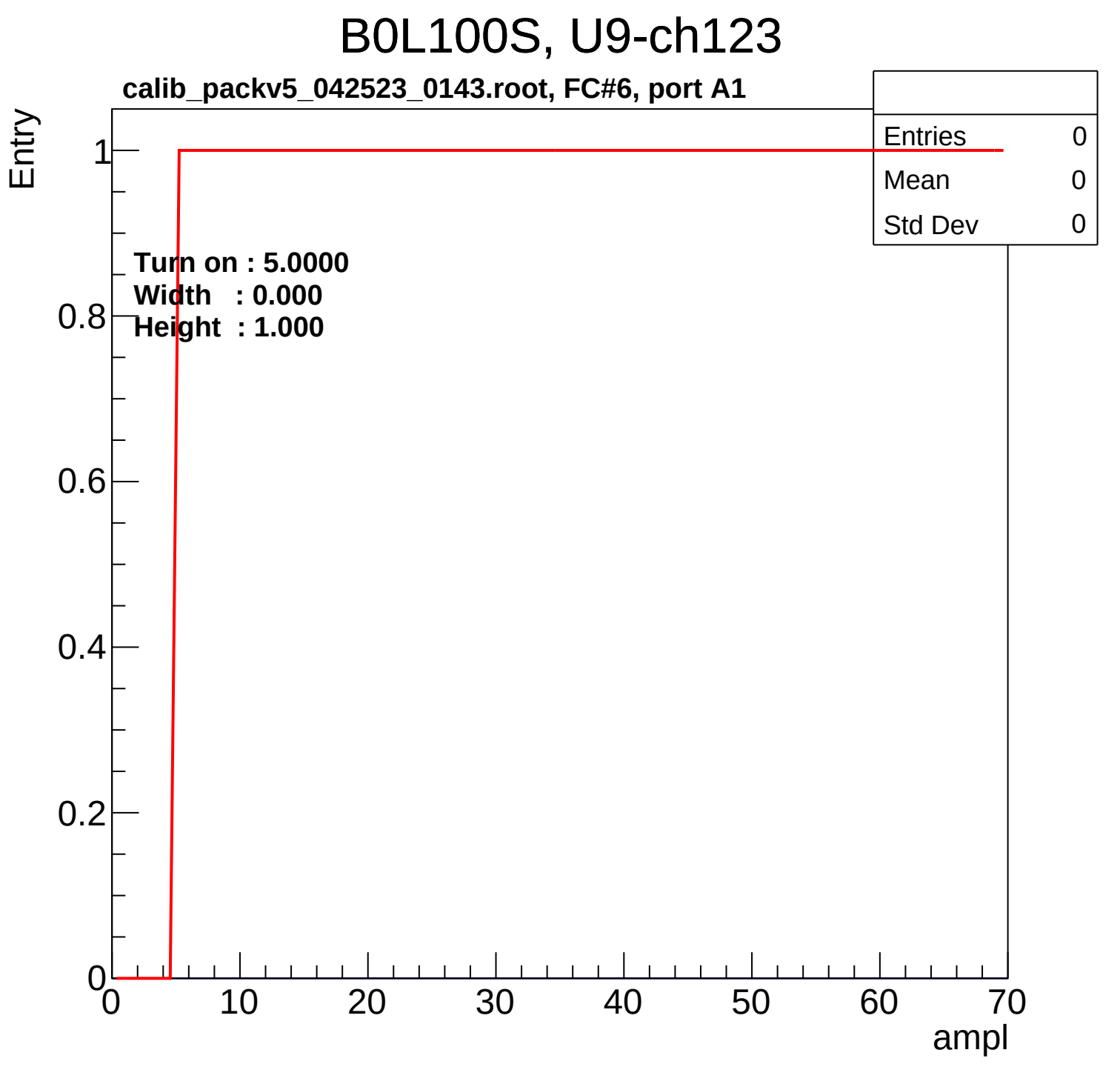

B0L100S, U9-ch118
calib_packv5_042523_0143.root, FC#6, port A1
Entries 28
Mean 48.75
Std Dev 2.516
Turn on : 25.0038
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

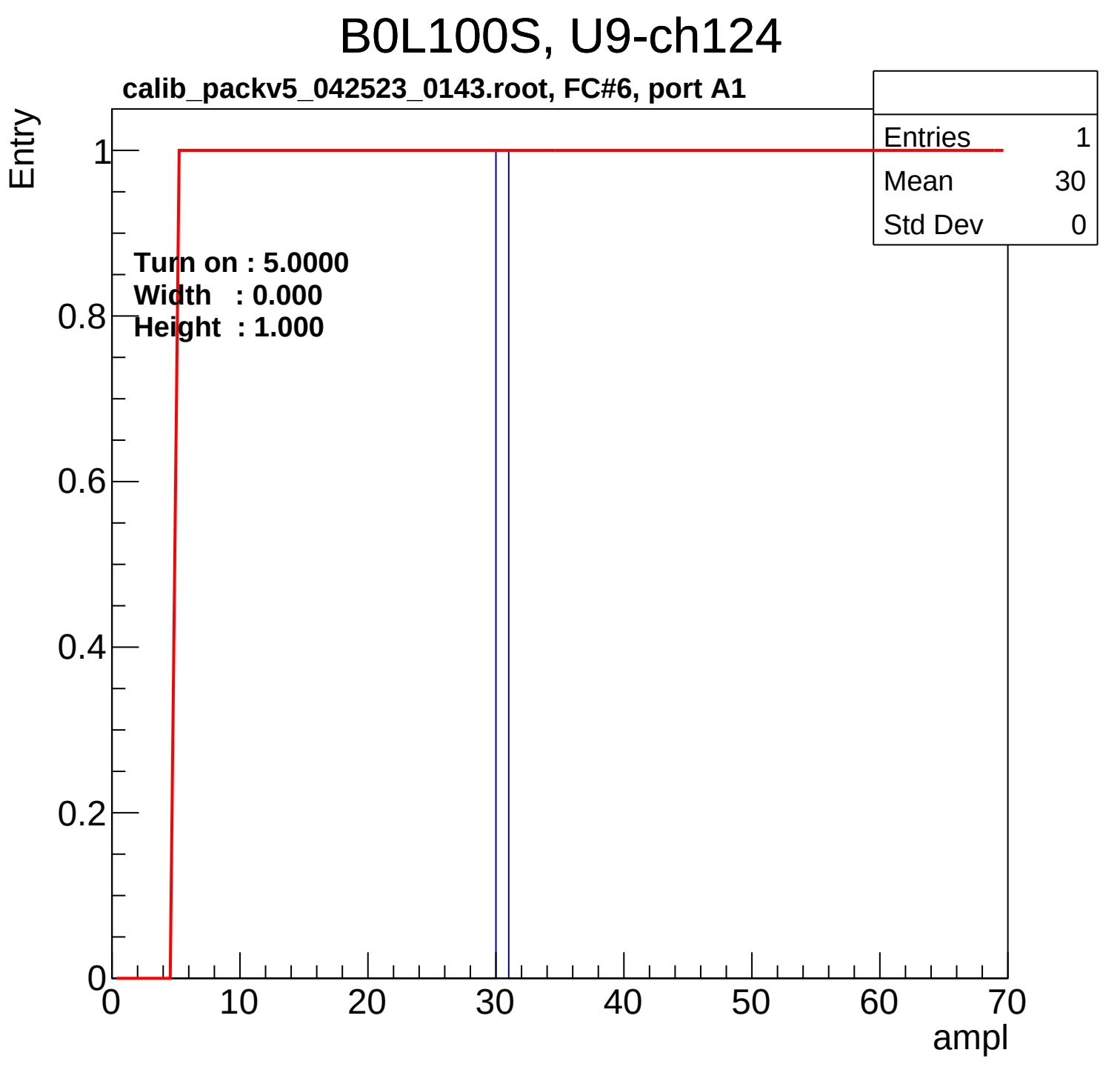

B0L100S, U9-ch119
calib_packv5_042523_0143.root, FC#6, port A1
Entries 11
Mean 48.82
Std Dev 0.7158
Turn on : 25.0000
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

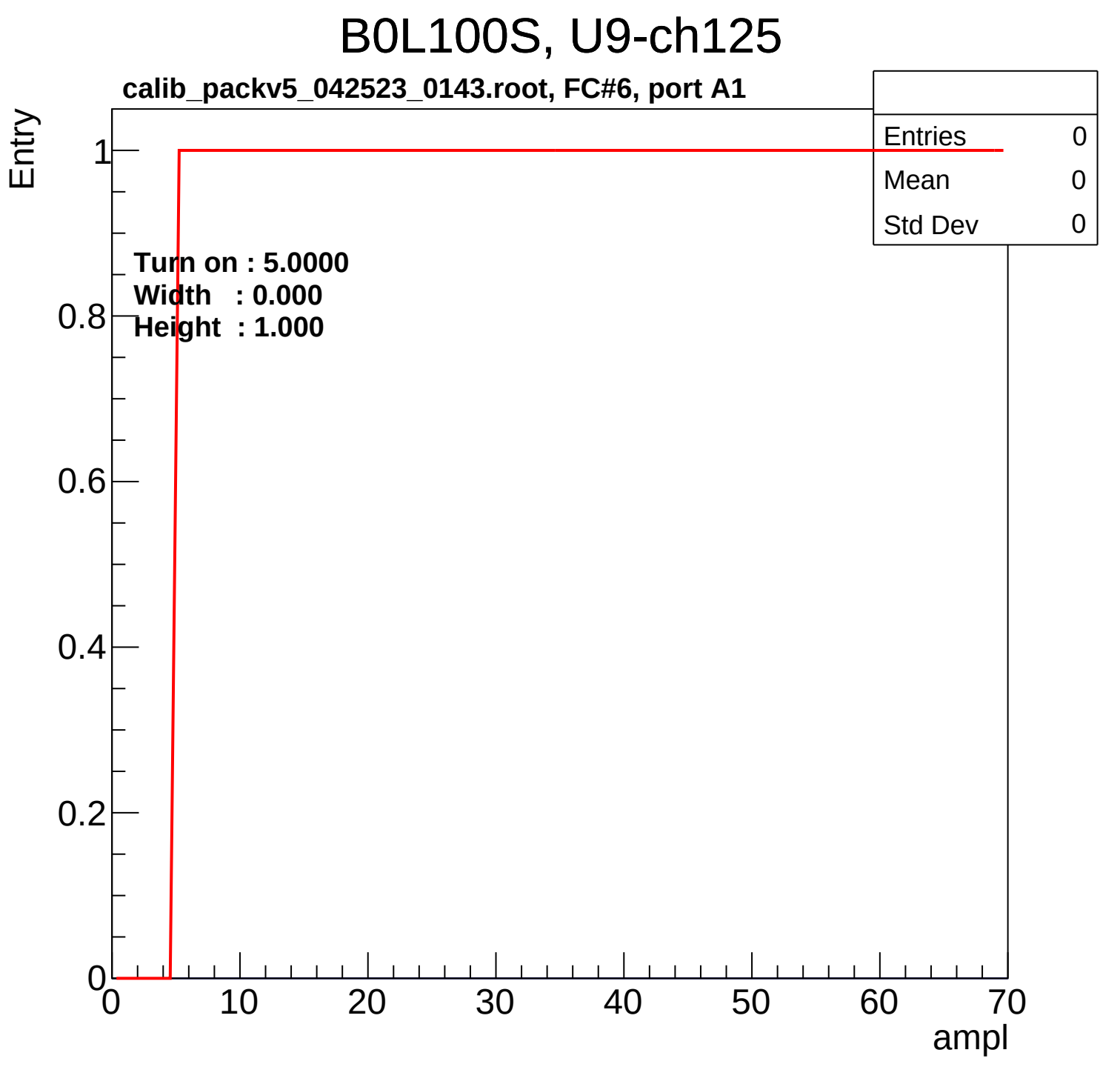

B0L100S, U9-ch120
calib_packv5_042523_0143.root, FC#6, port A1
Entries 3
Mean 46.33
Std Dev 0.4714
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

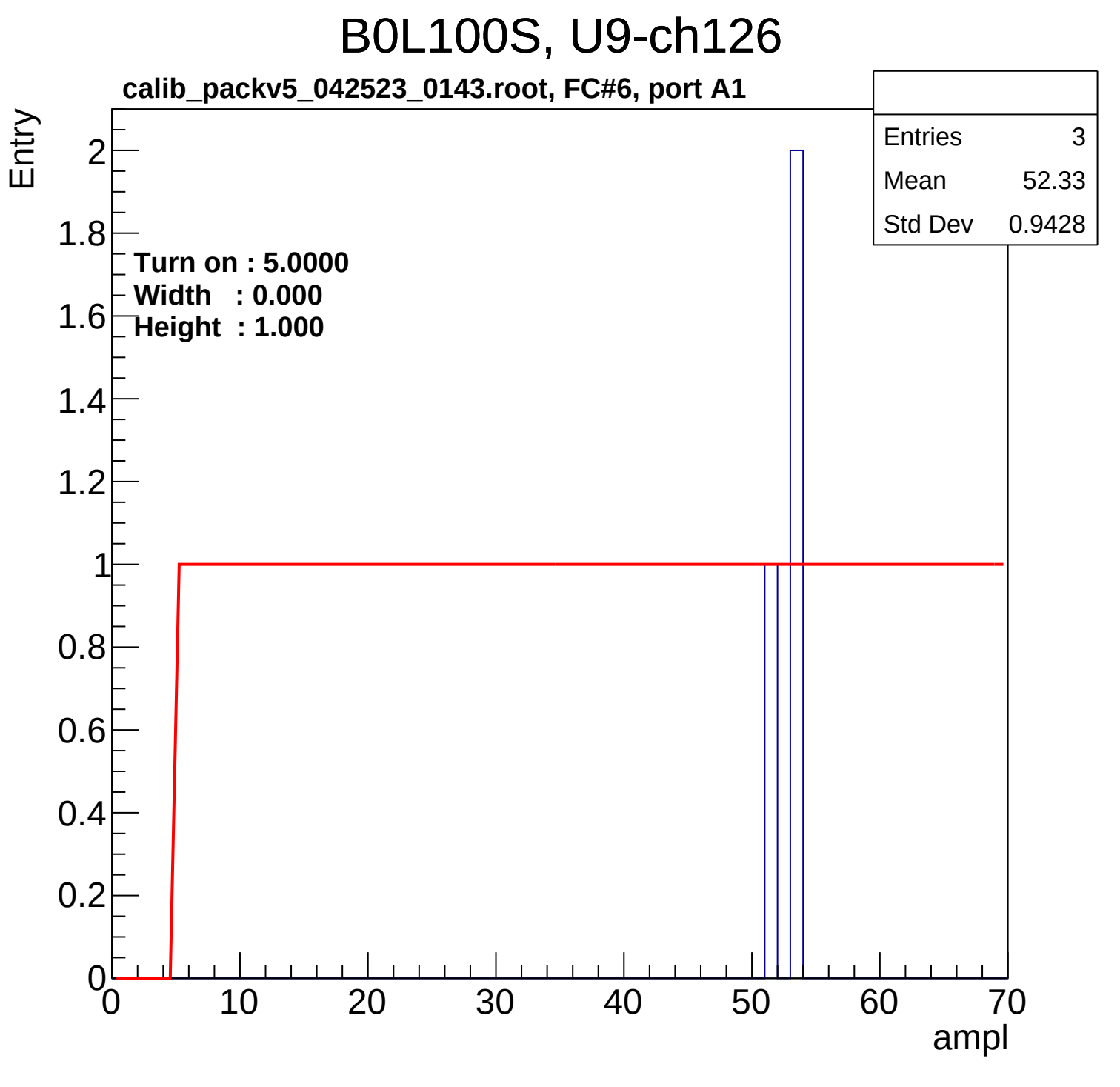

B0L100S, U9-ch121
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

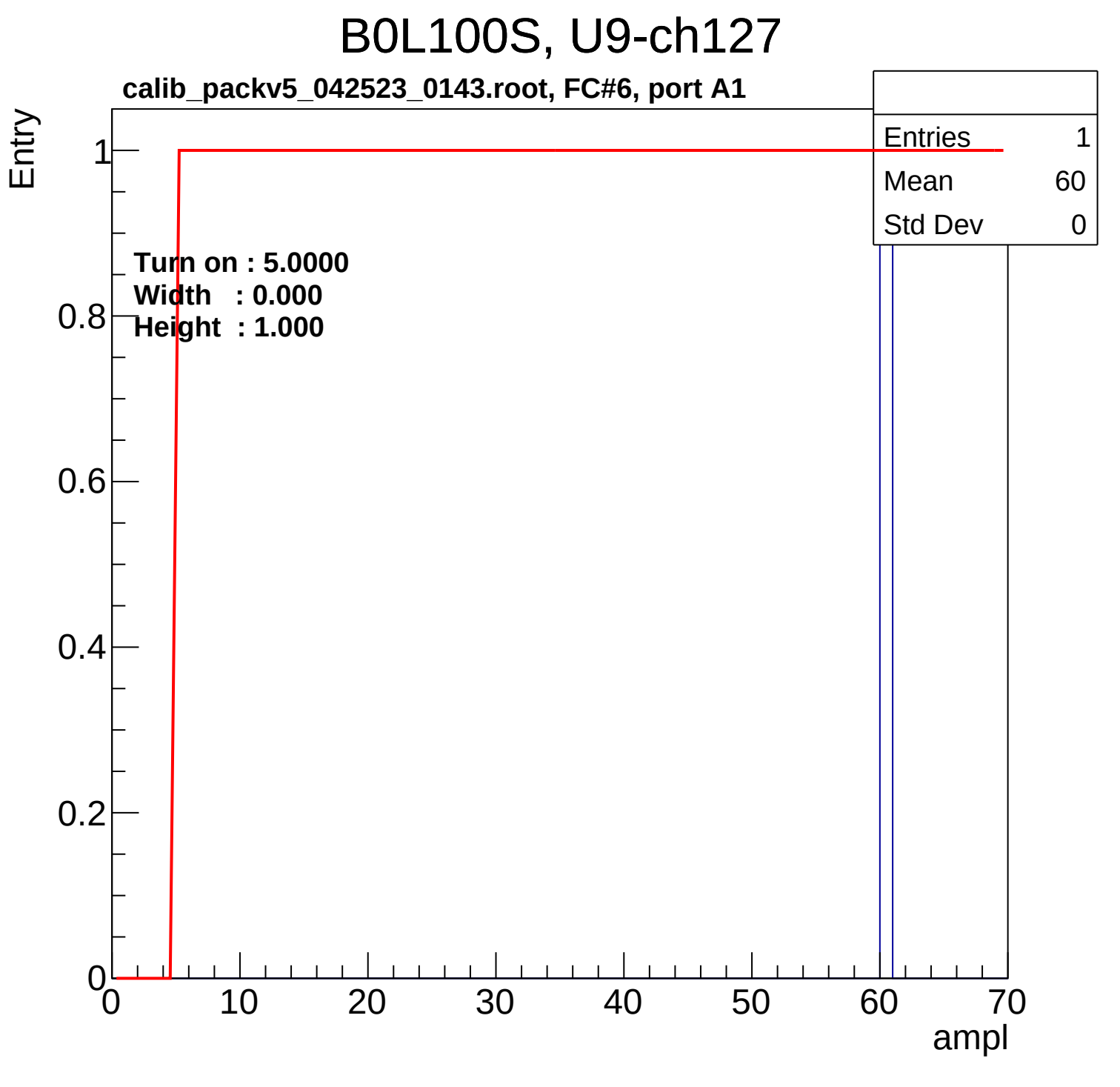

B0L100S, U9-ch122
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

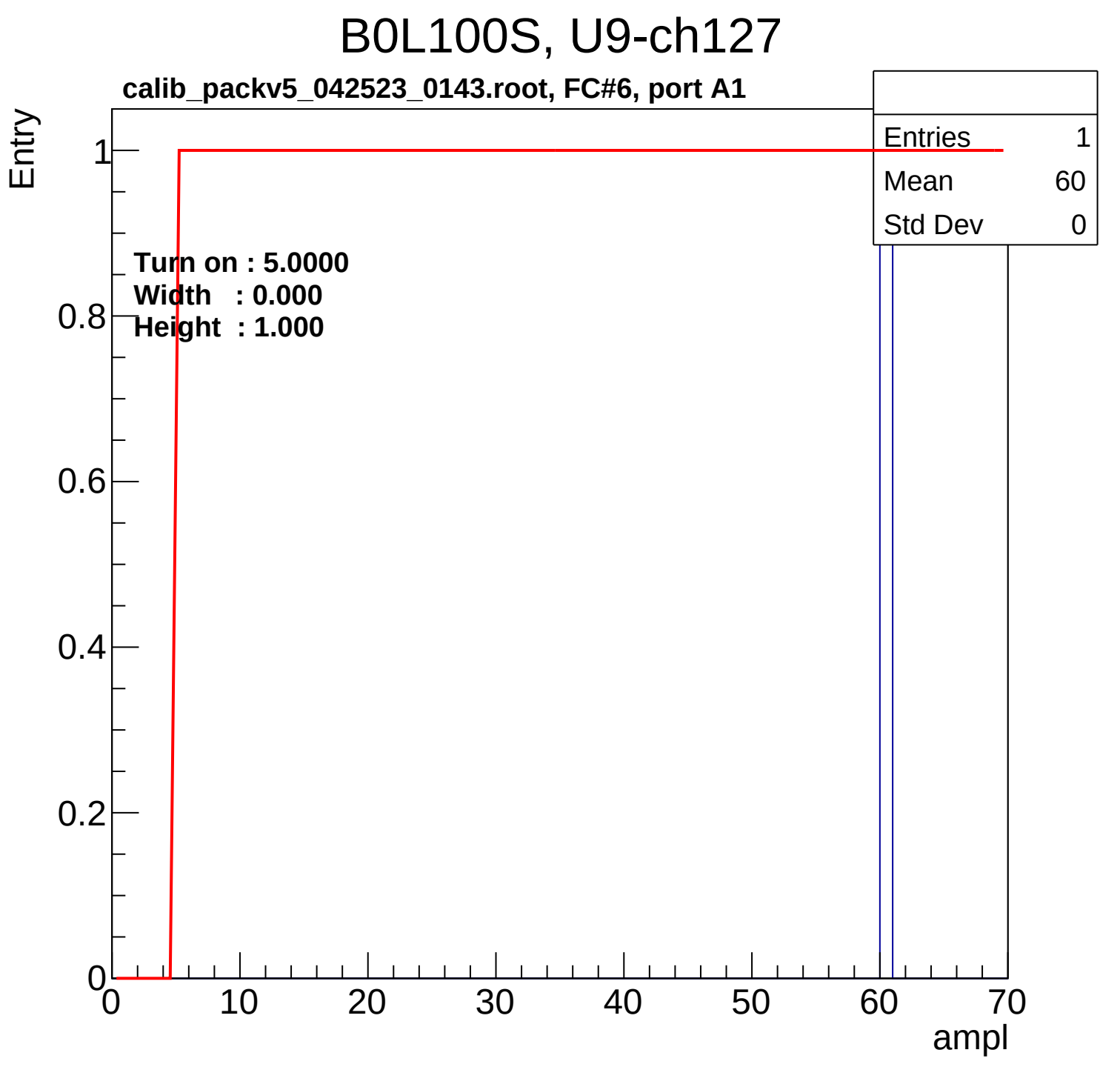

B0L100S, U9-ch123
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U9-ch124
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 30
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B0L100S, U9-ch125
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U9-ch126
calib_packv5_042523_0143.root, FC#6, port A1
Entries 3
Mean 52.33
Std Dev 0.9428
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B0L100S, U9-ch127
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 60
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B0L100S, U9-ch127
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 60
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70