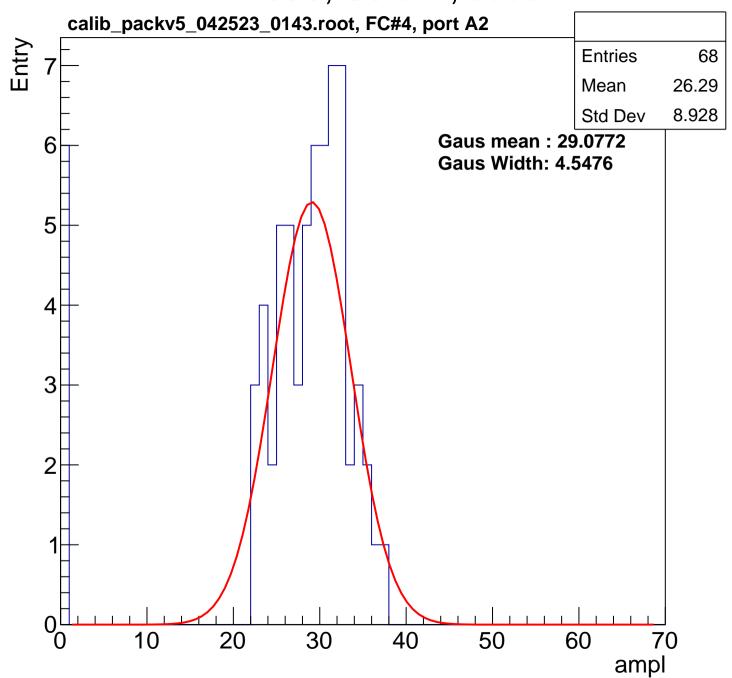
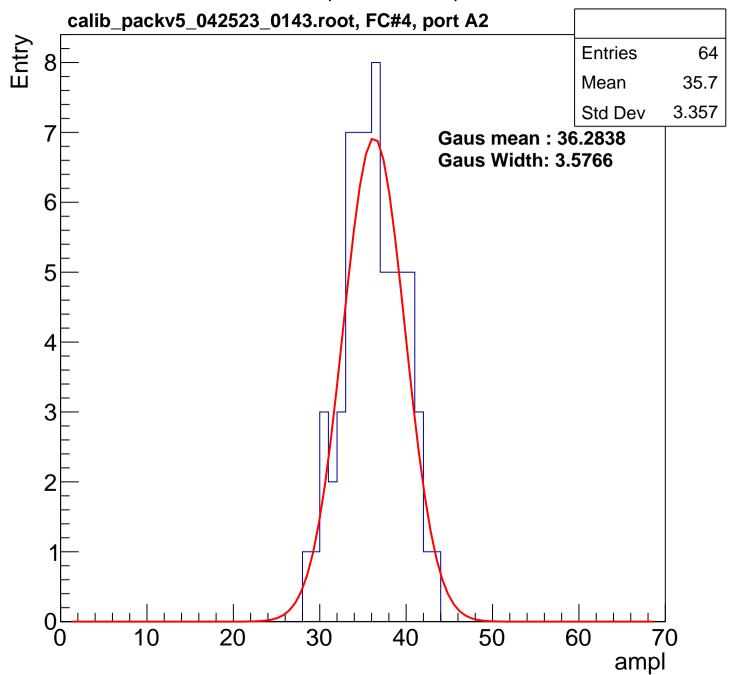
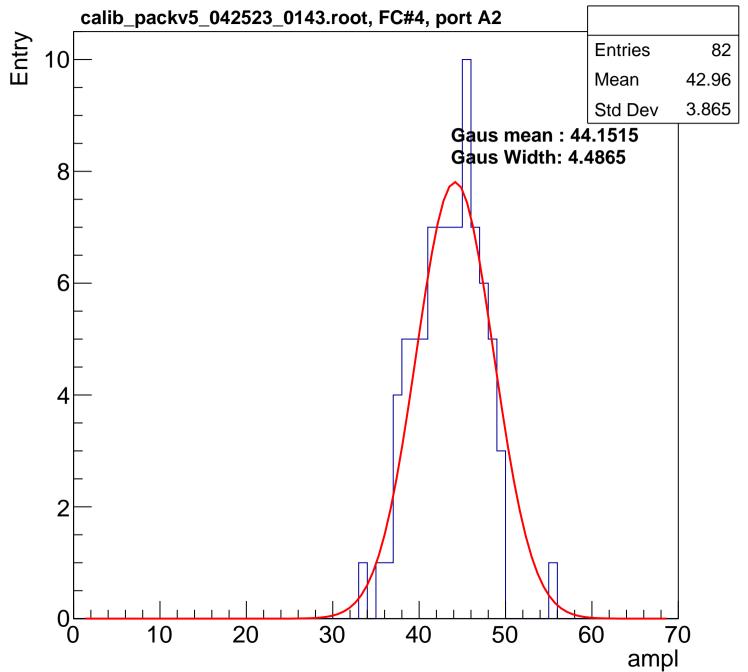
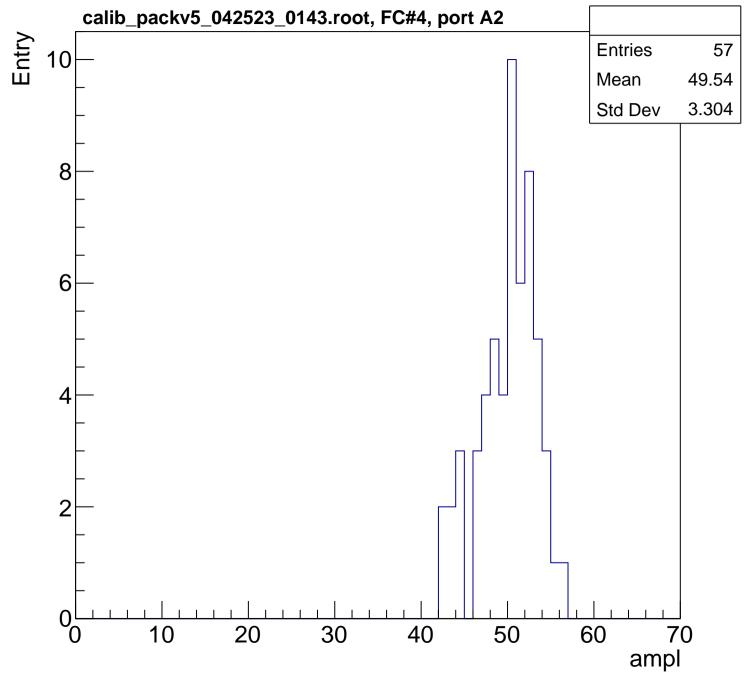


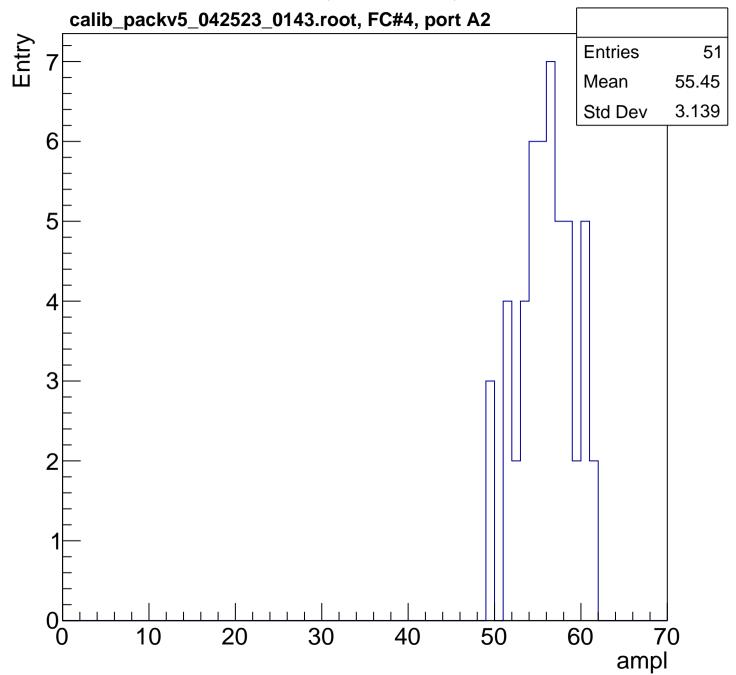
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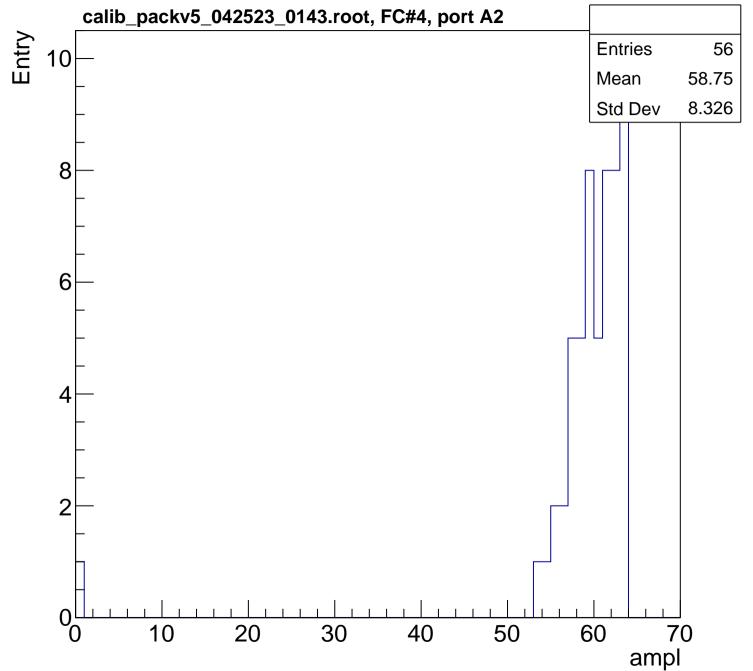


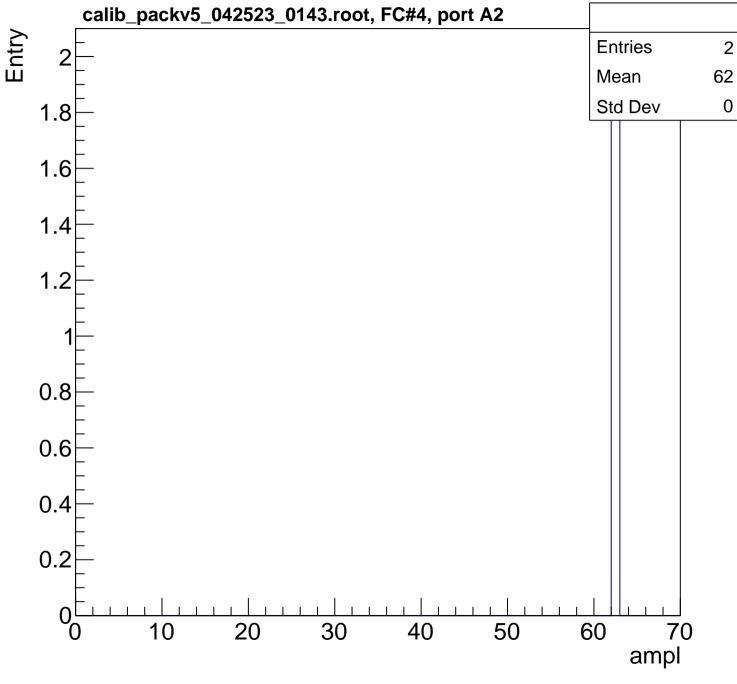




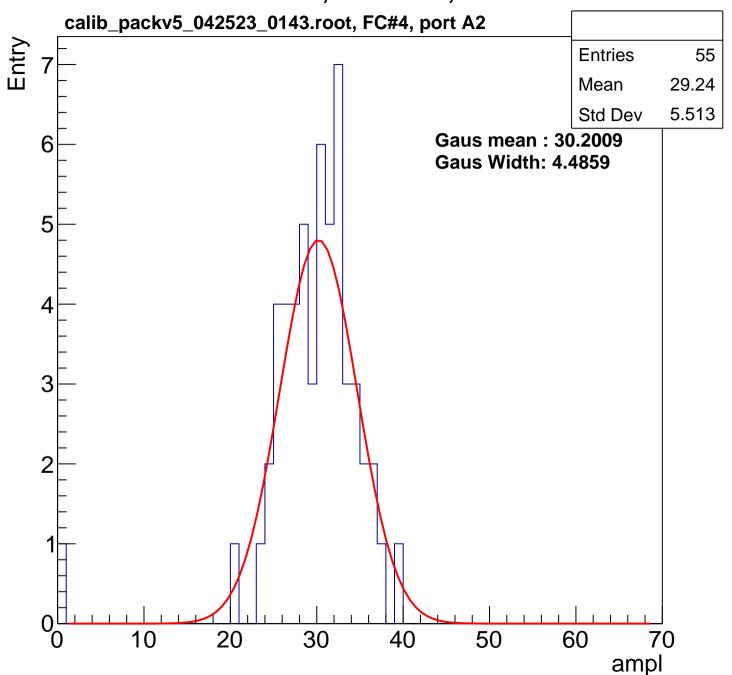


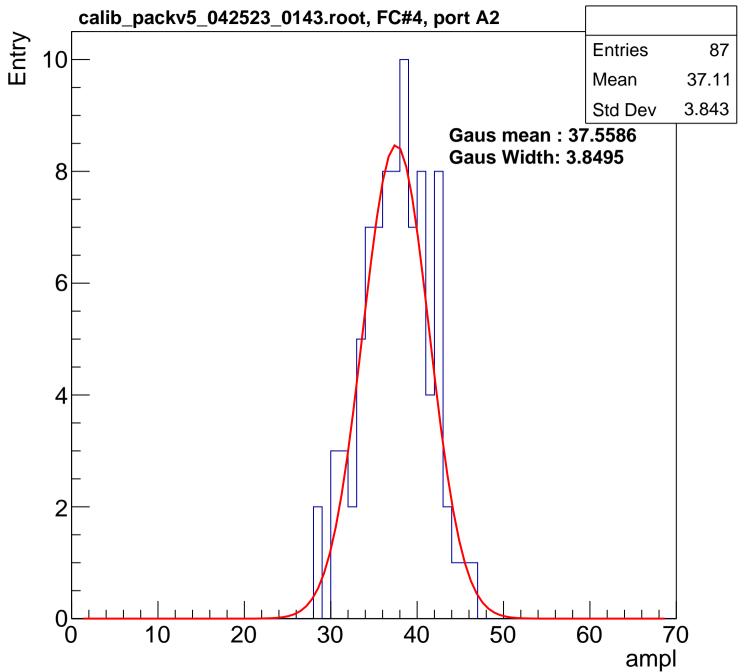


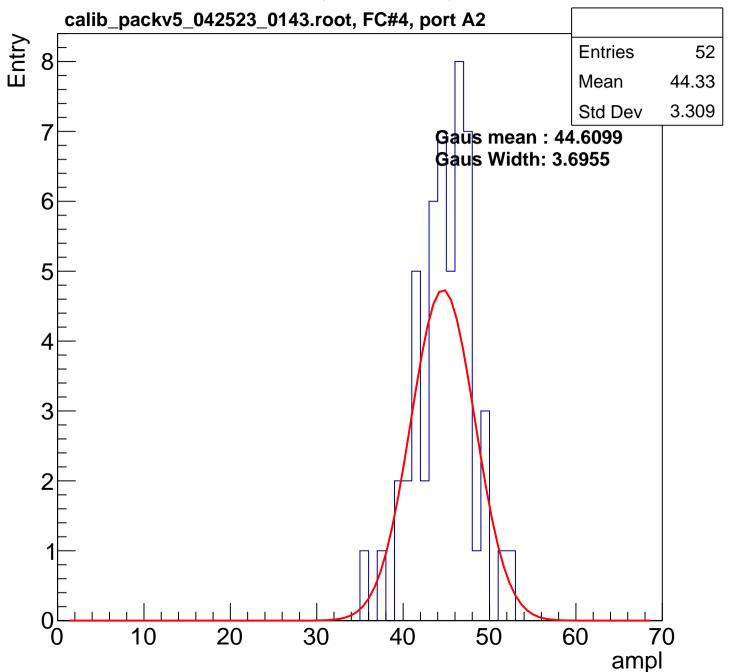


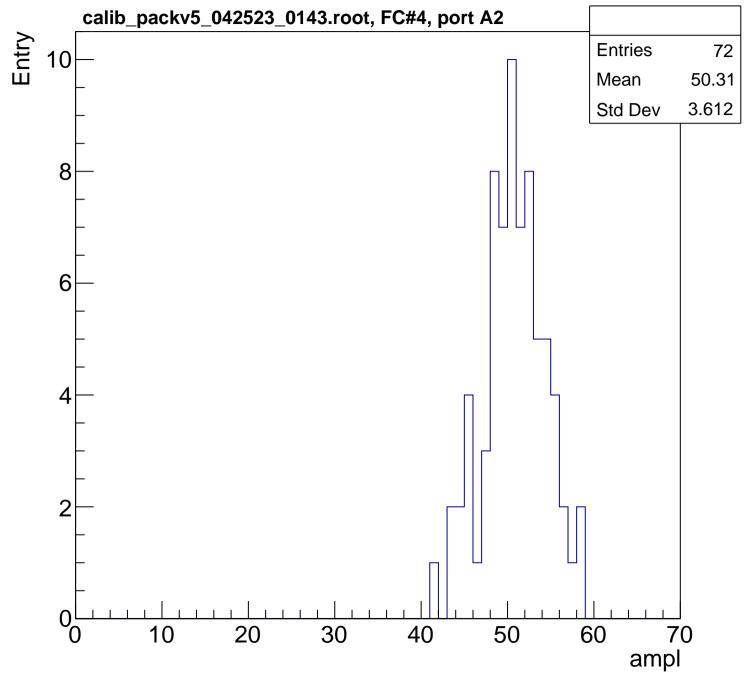


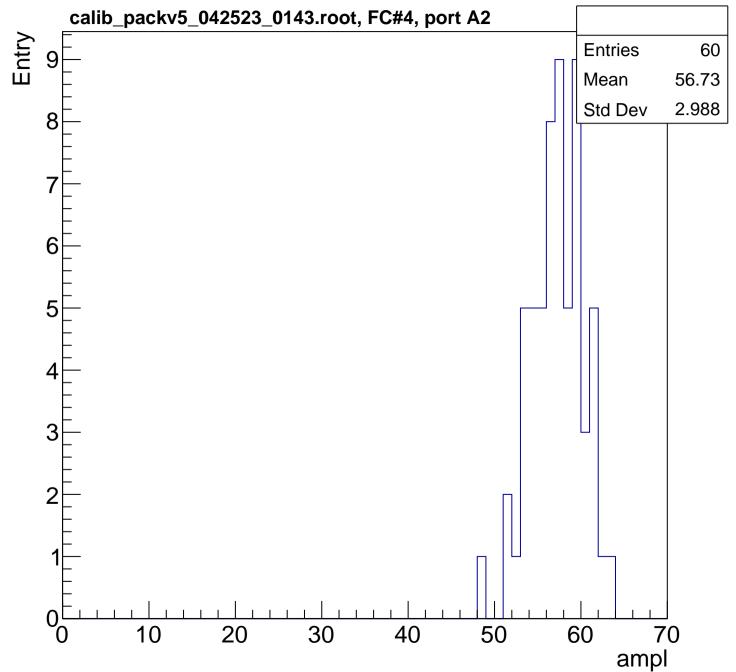
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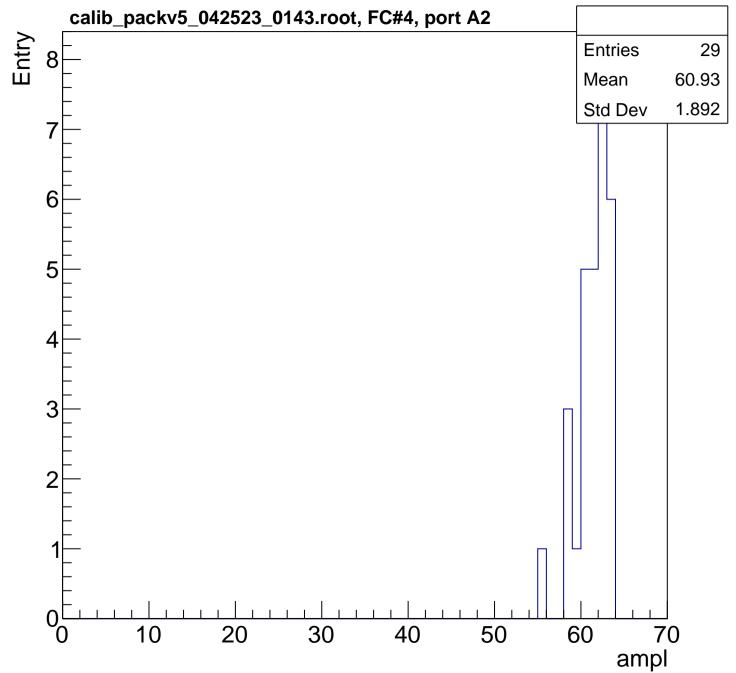


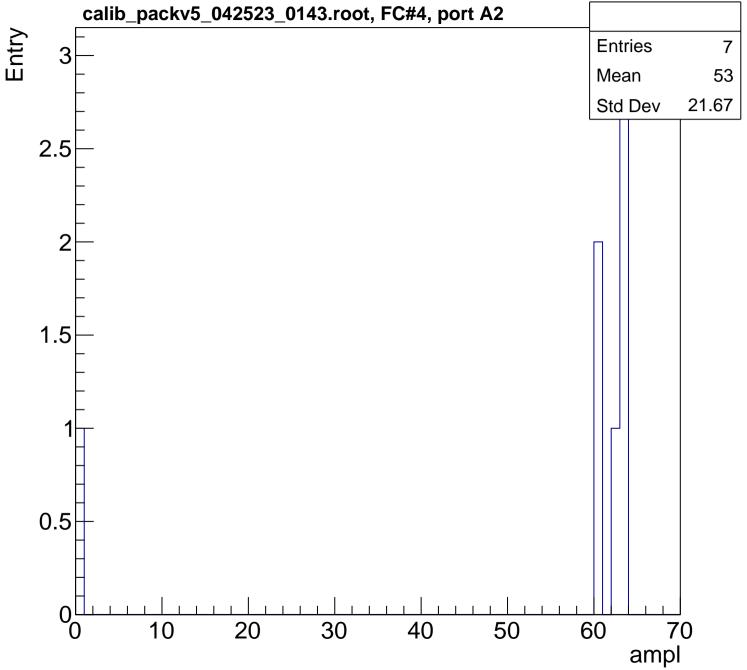


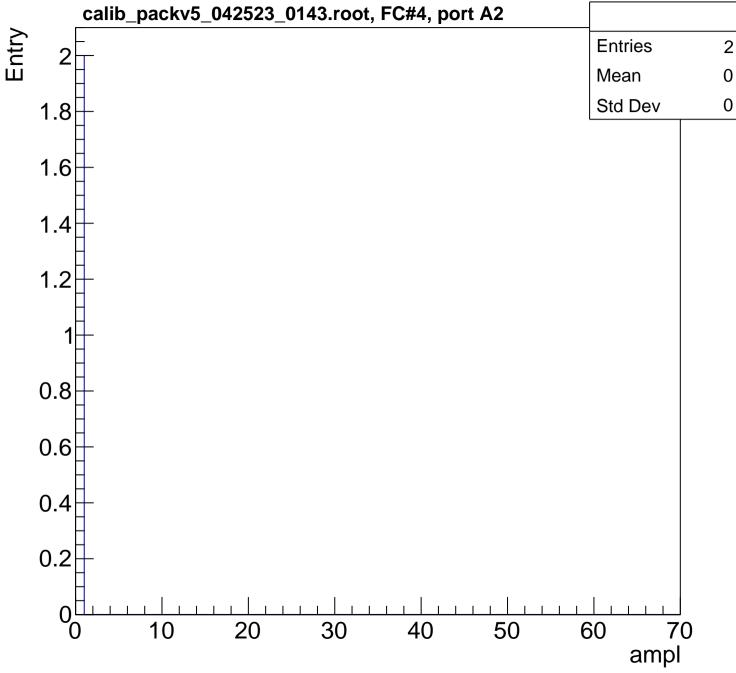


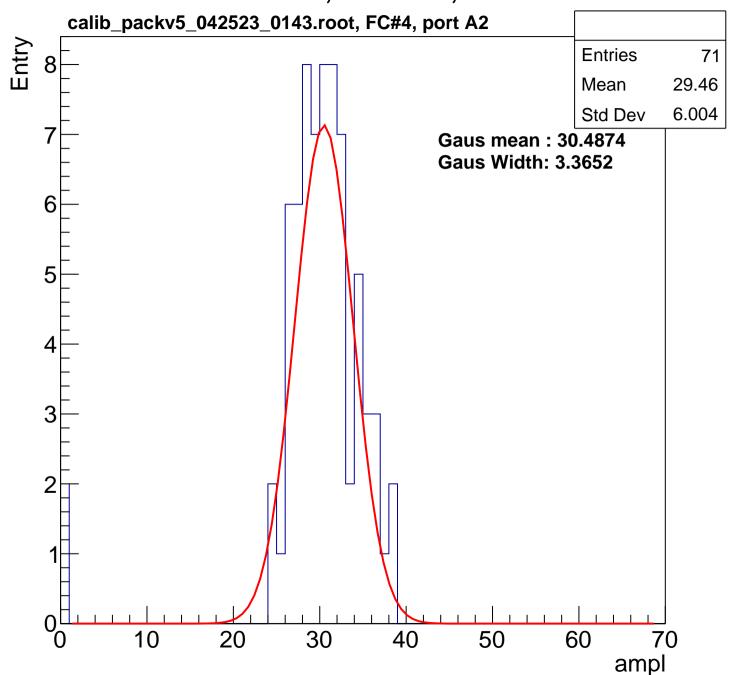


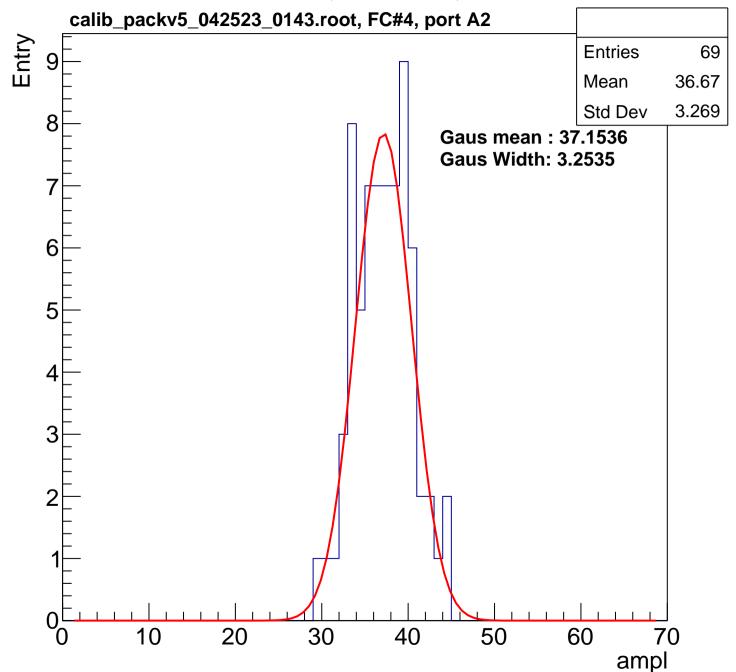


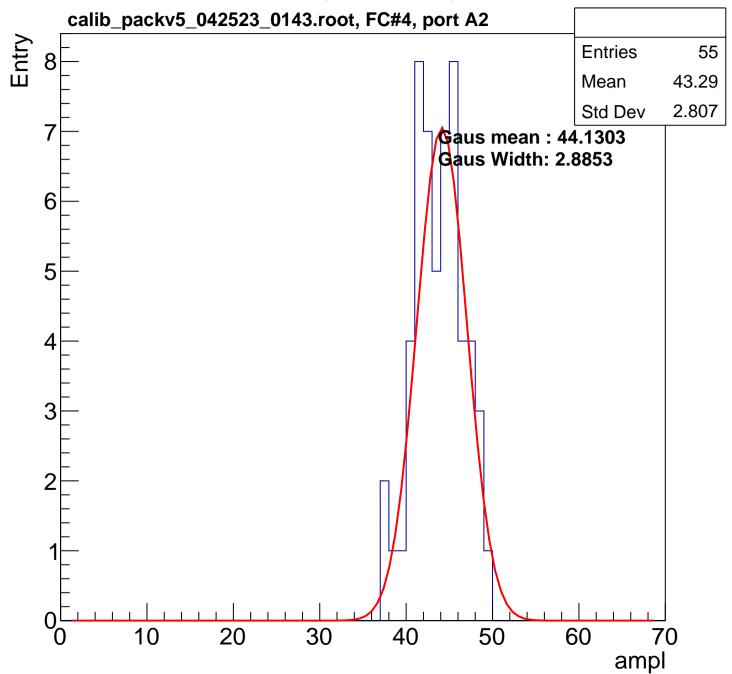


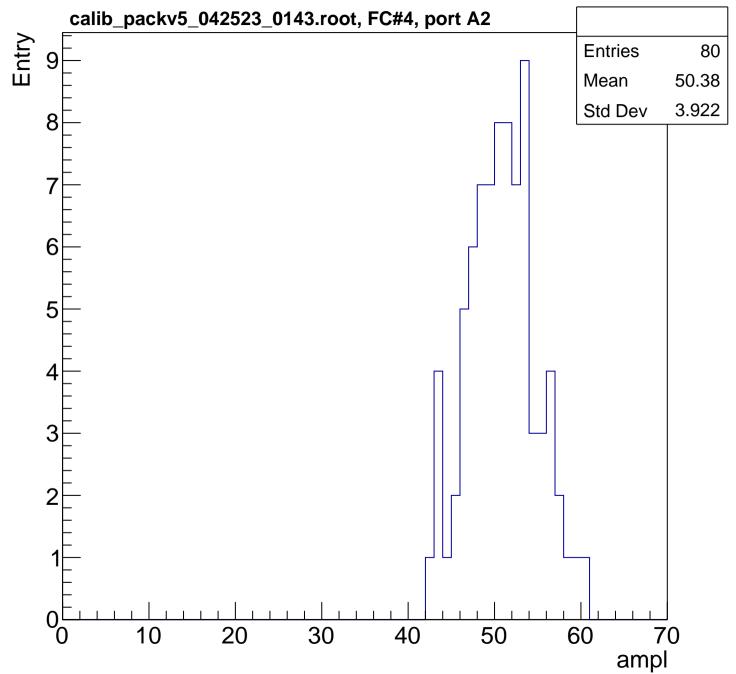


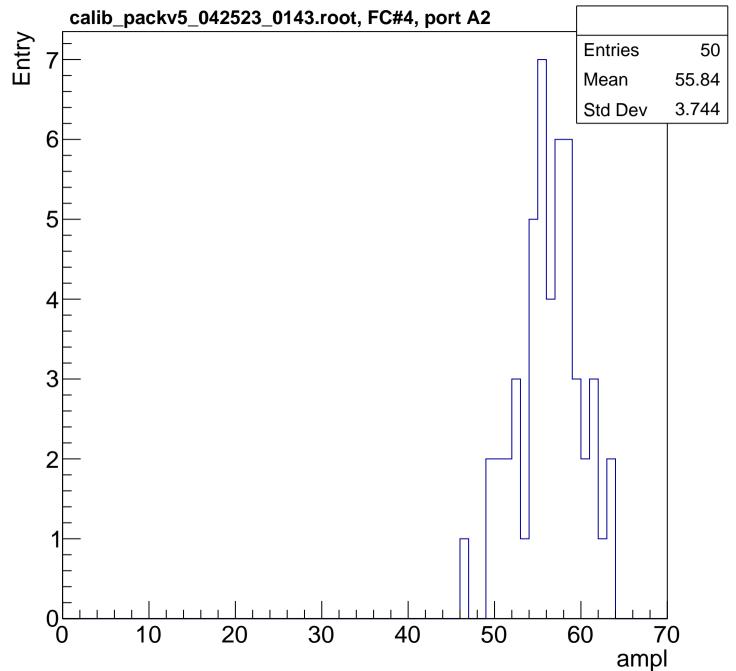


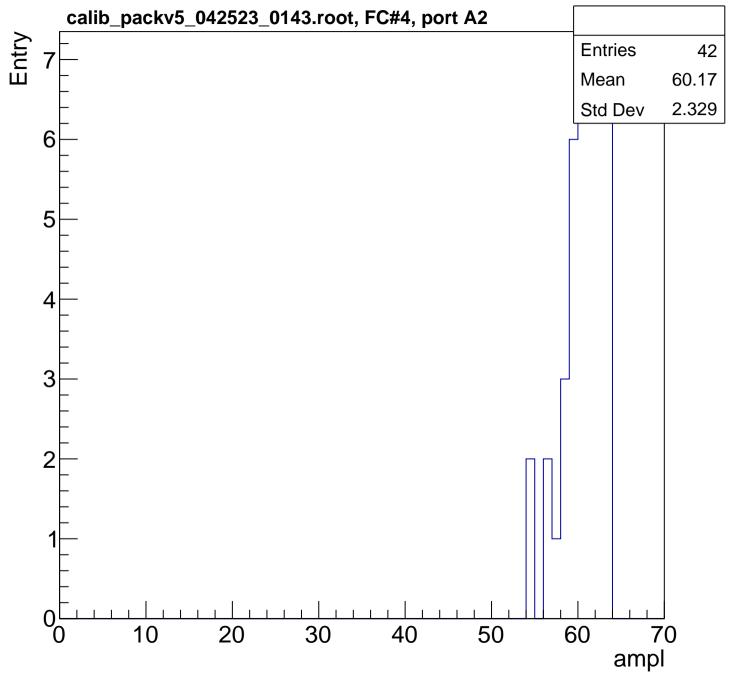


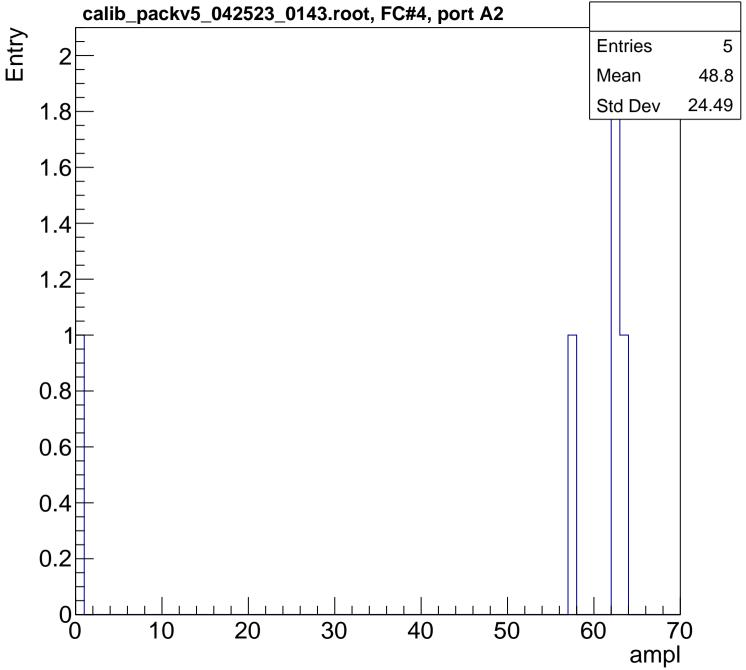




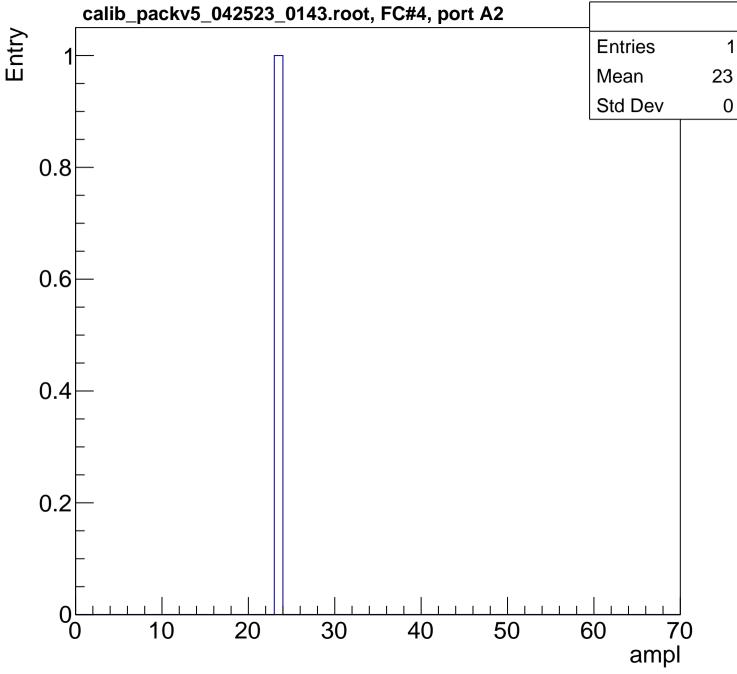


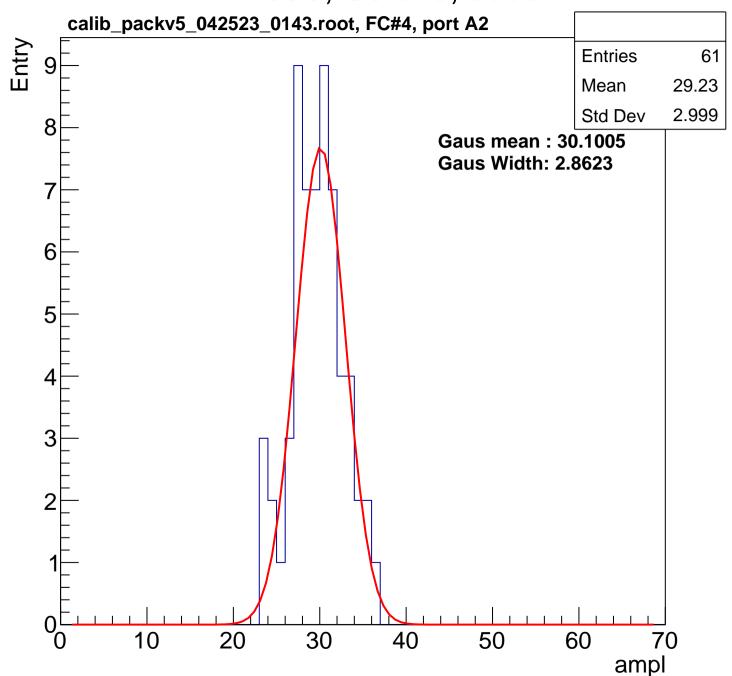


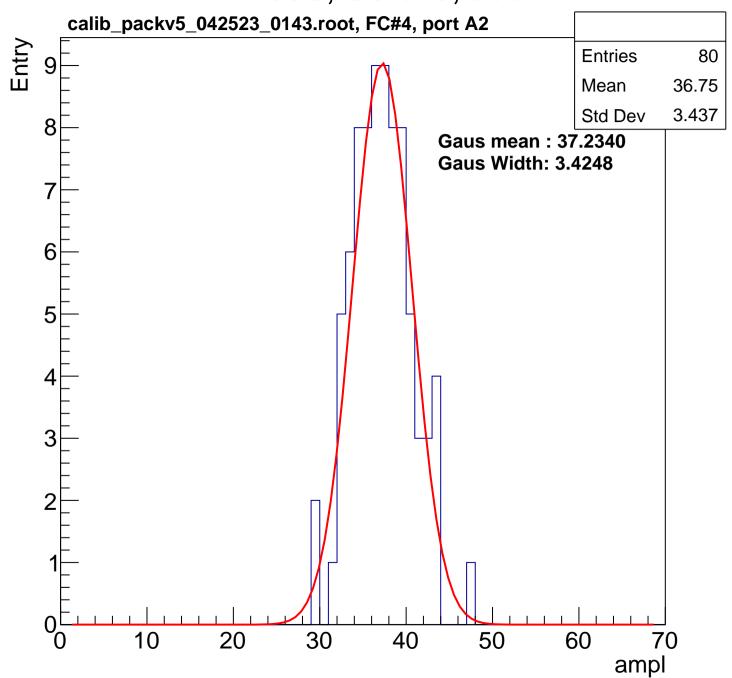


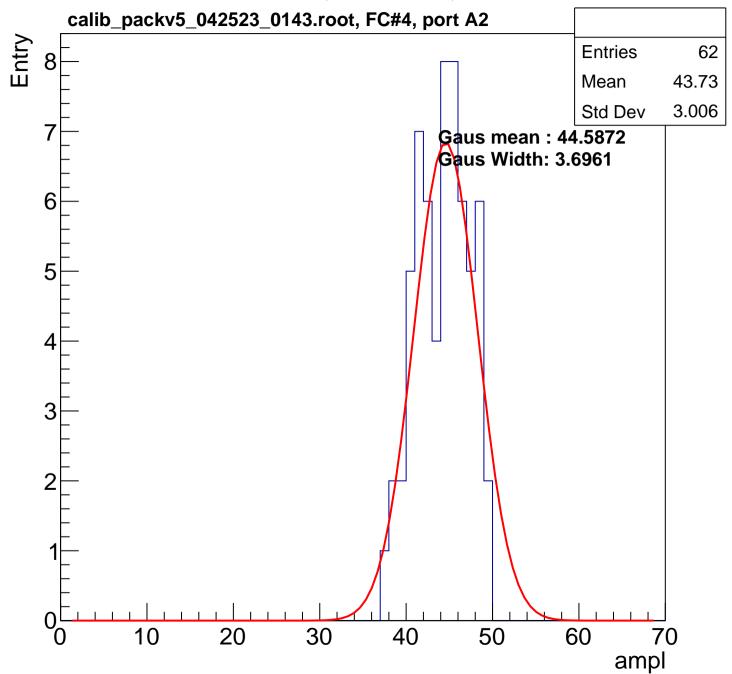


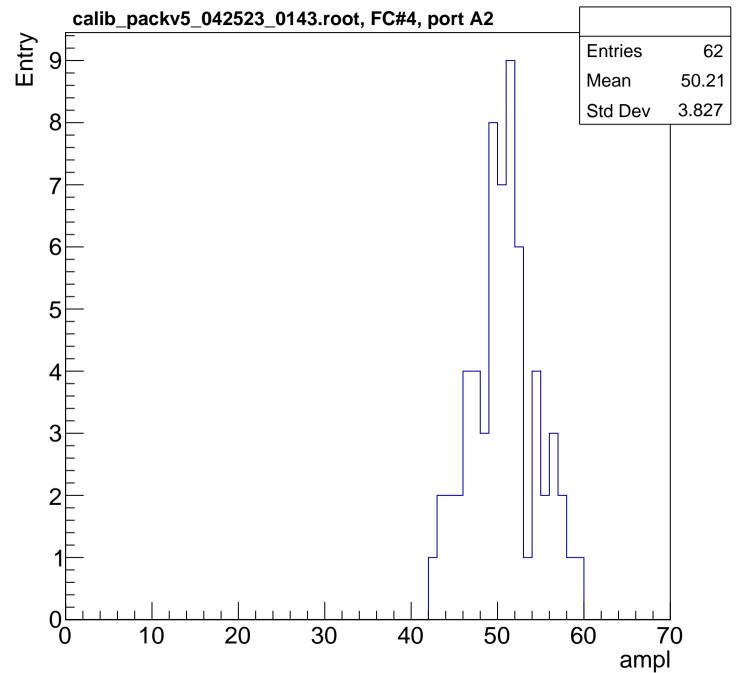
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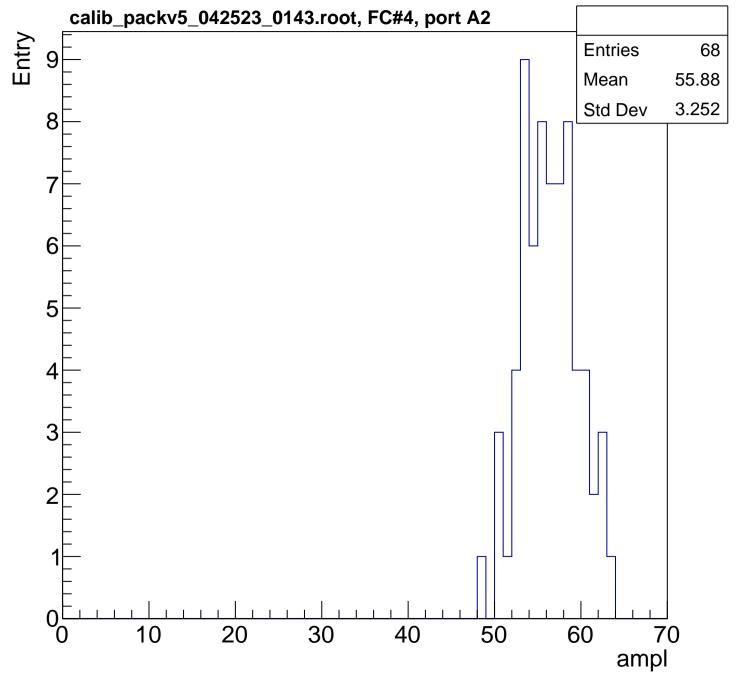


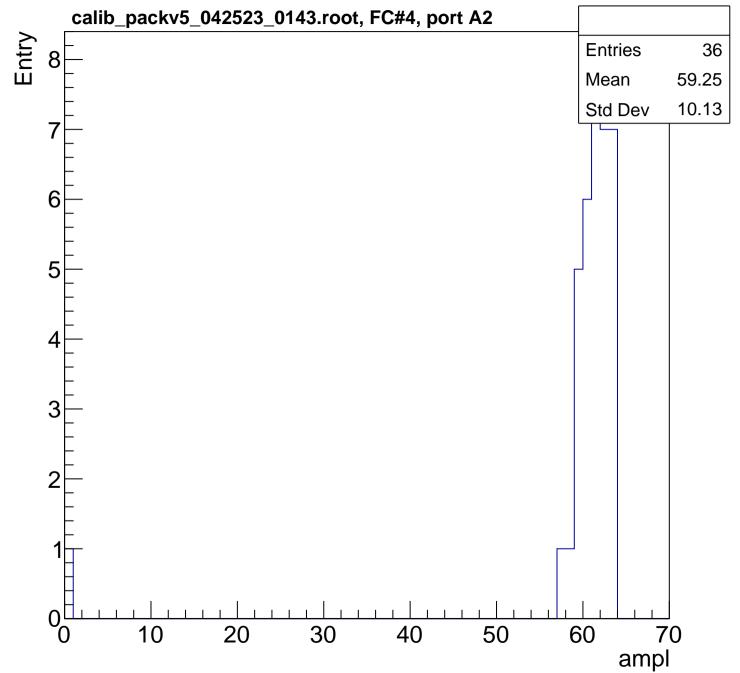


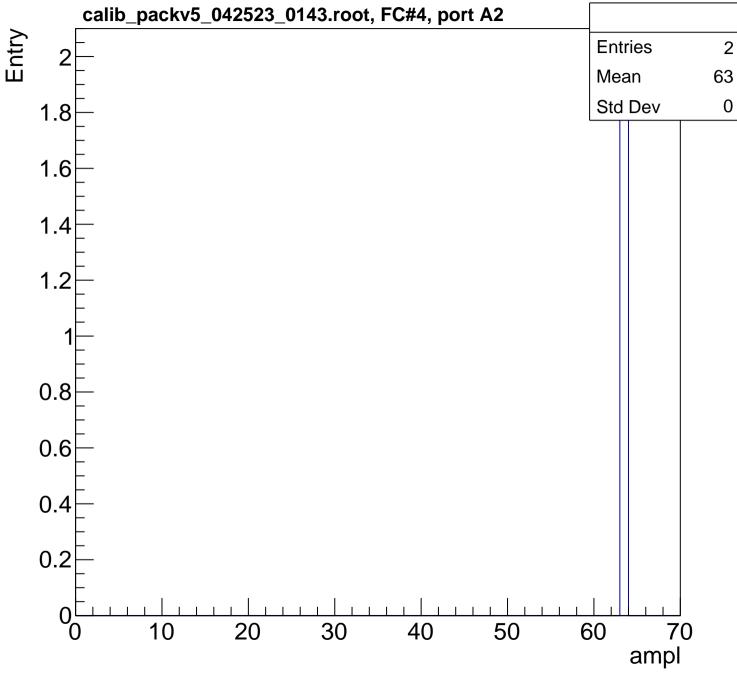


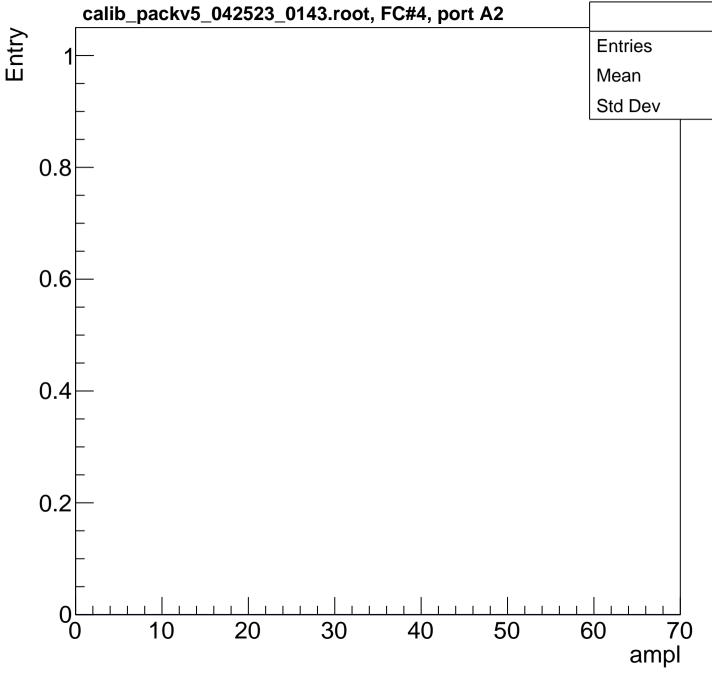


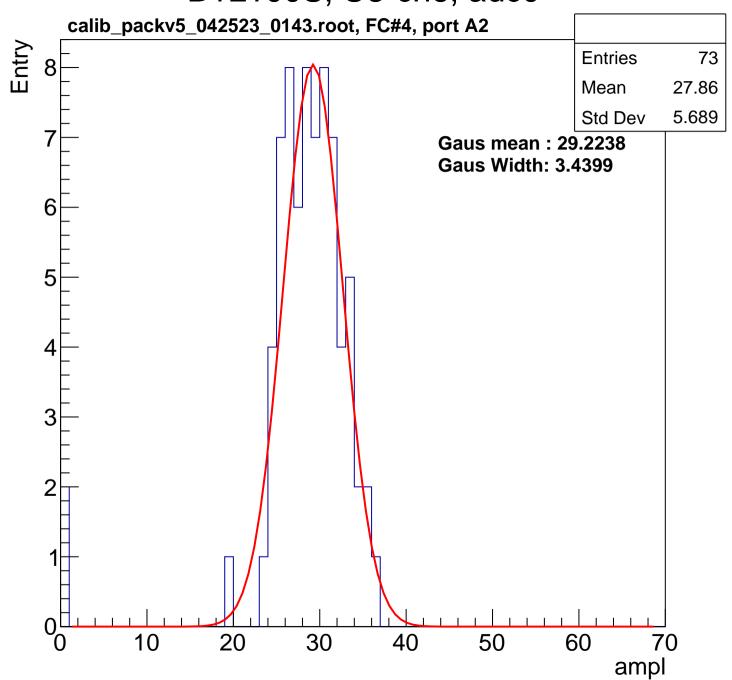


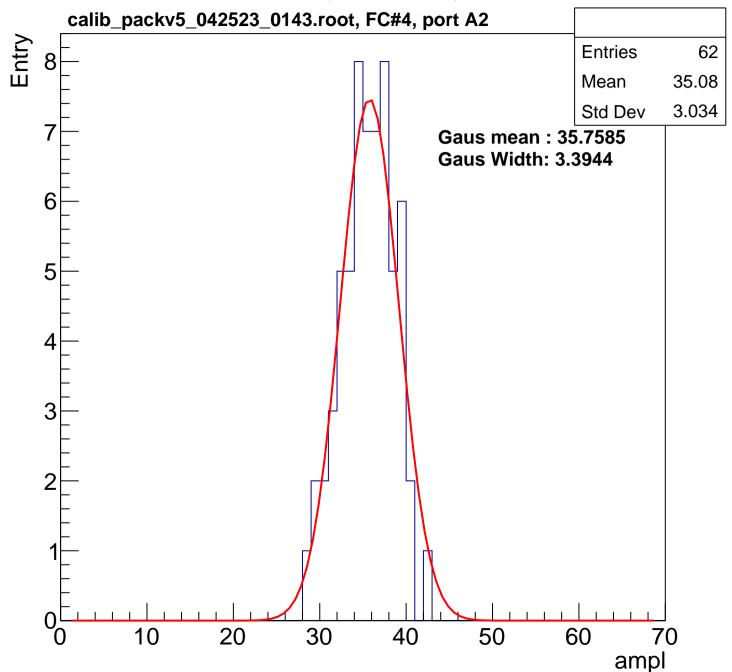


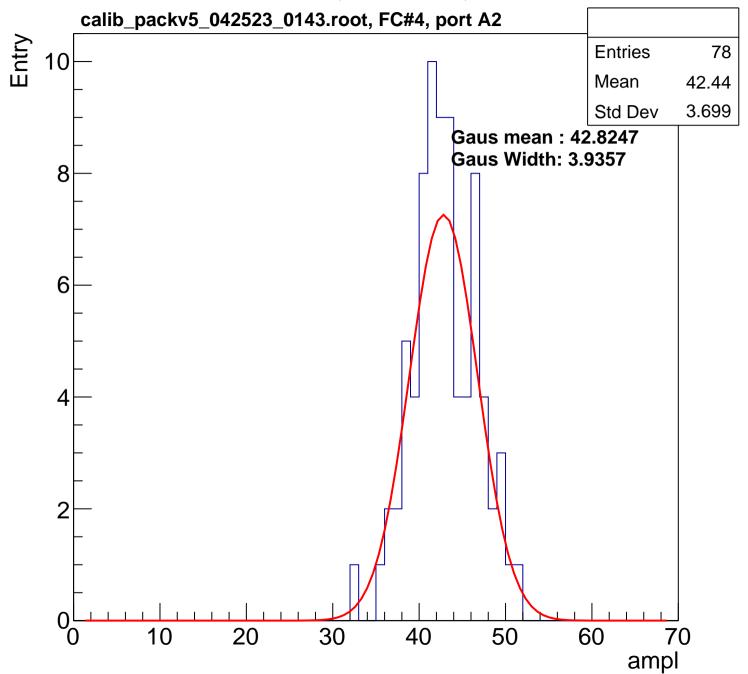


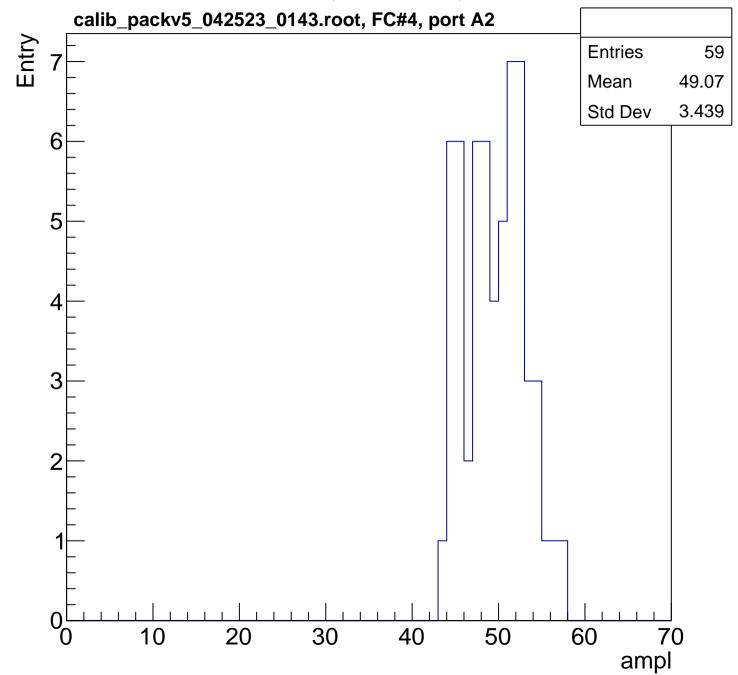


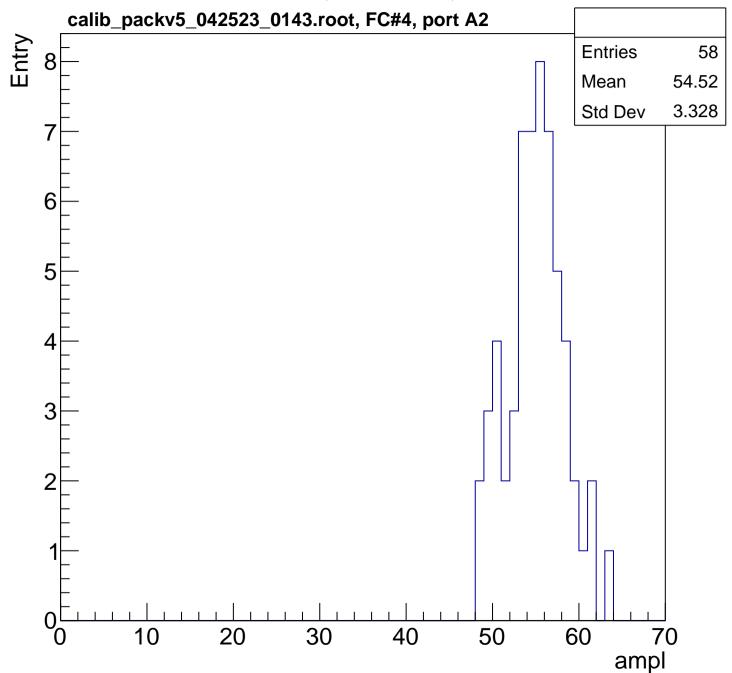


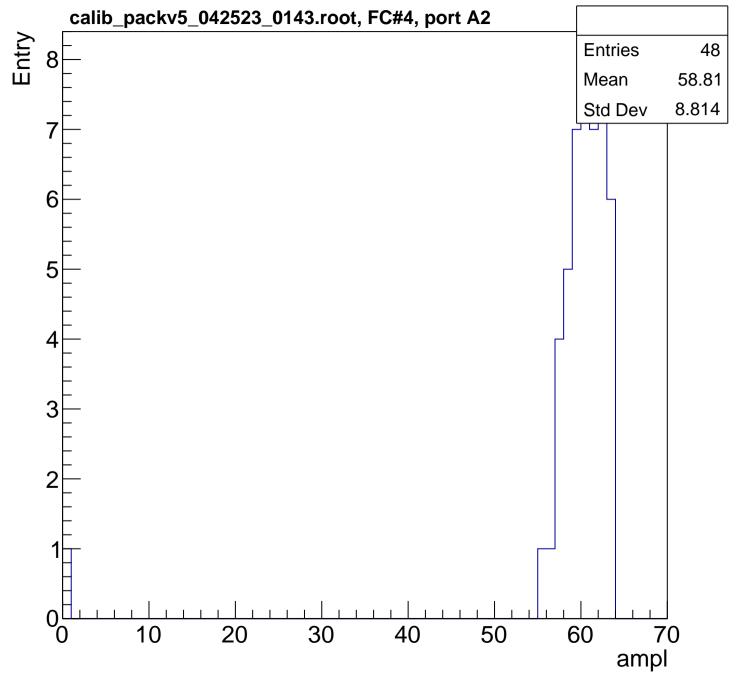


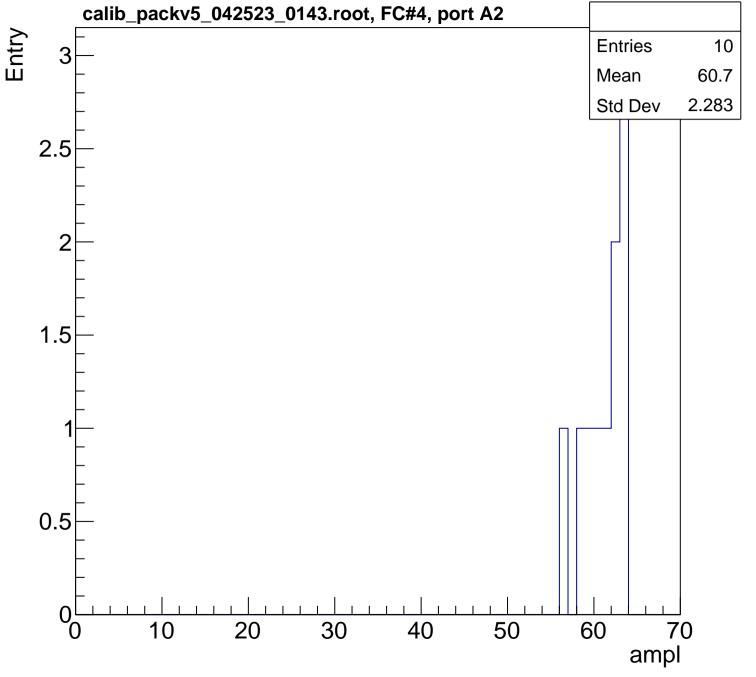




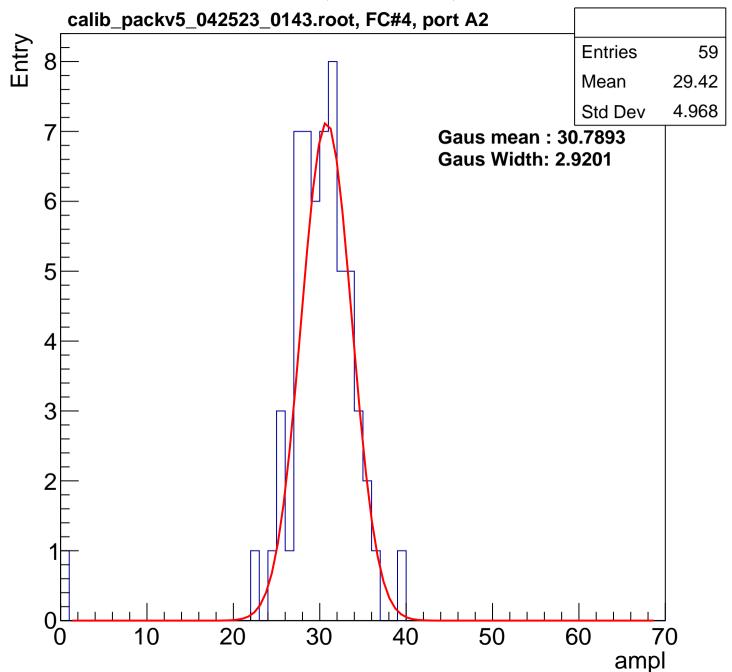


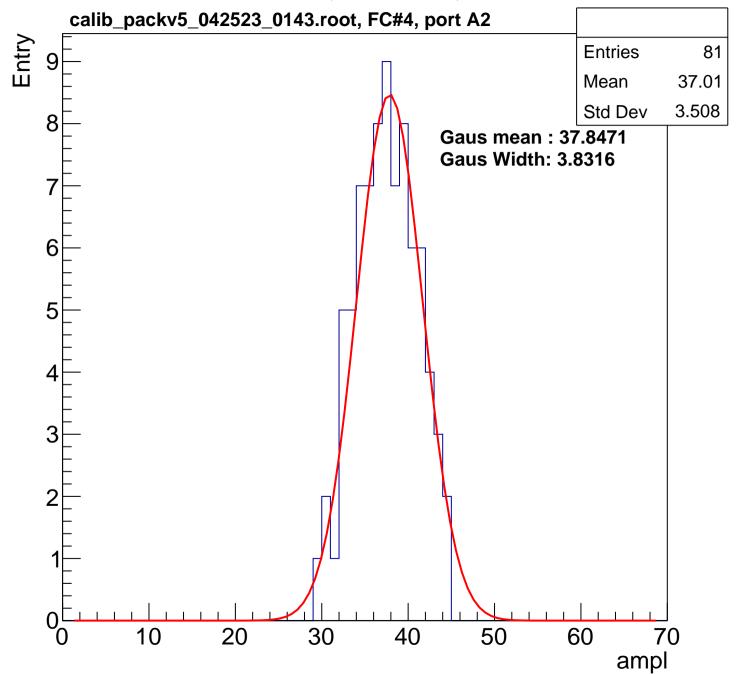


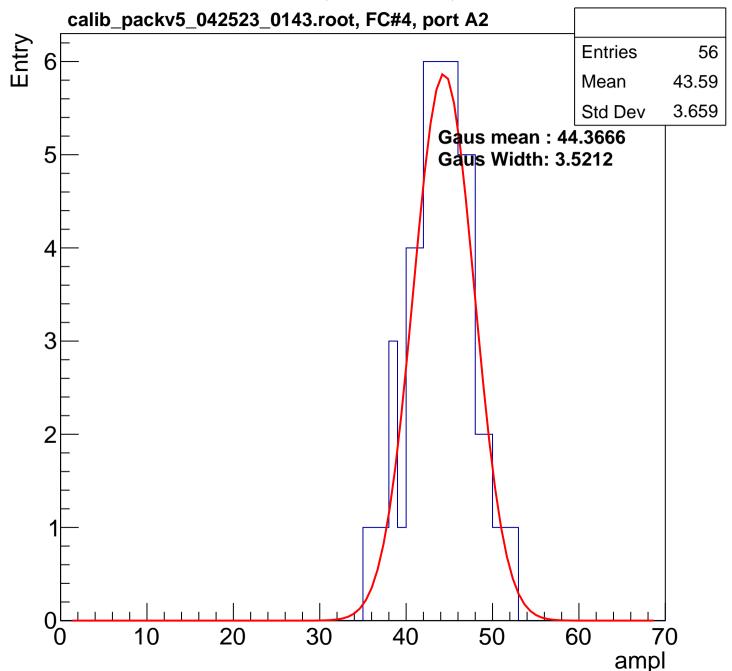


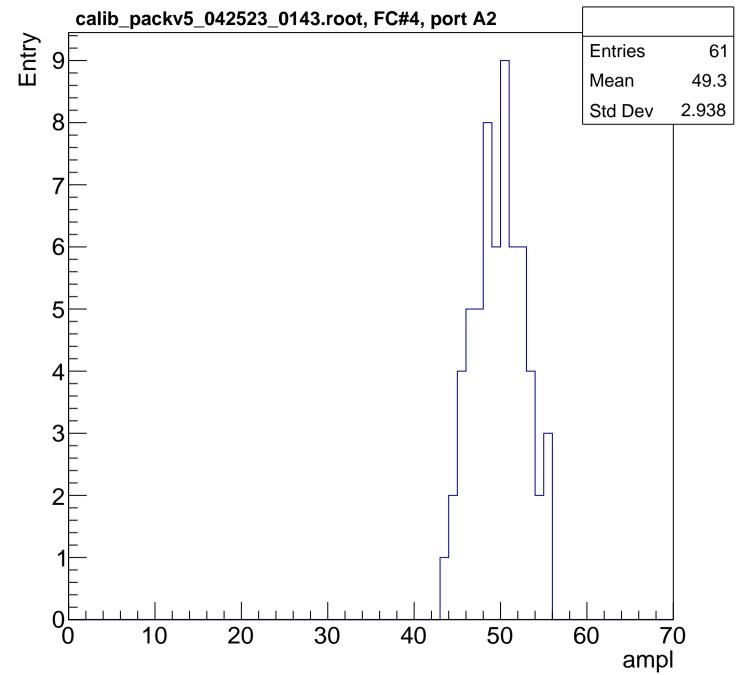


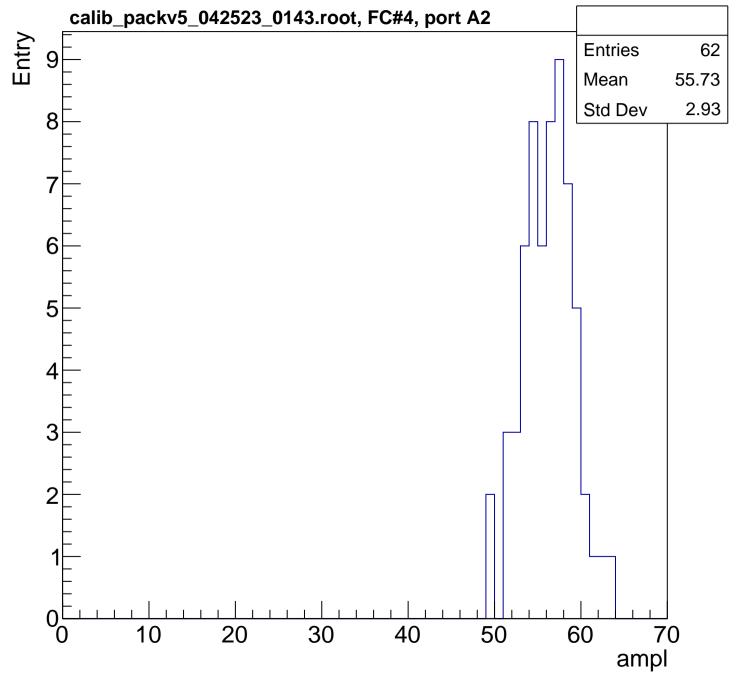
B1L100S, U3-ch6, adc7 calib_packv5_042523_0143.root, FC#4, port A2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

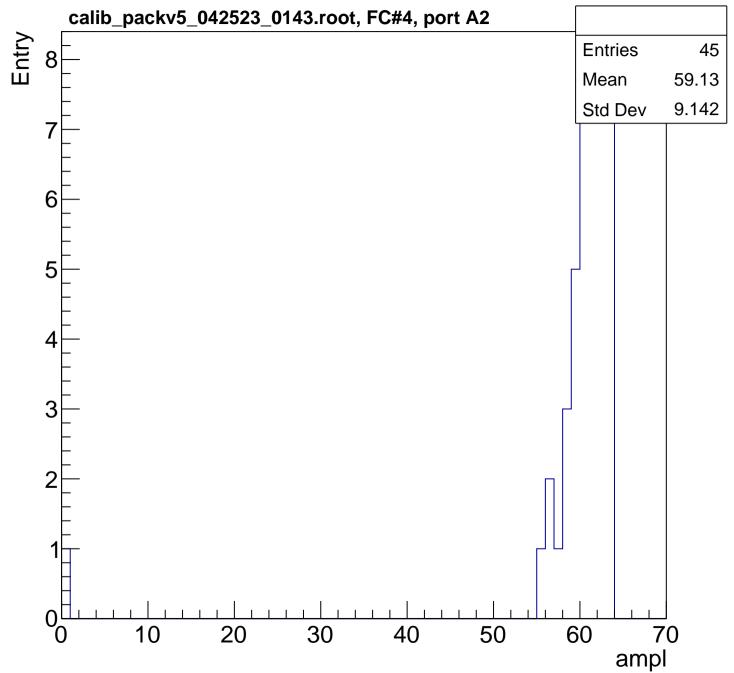


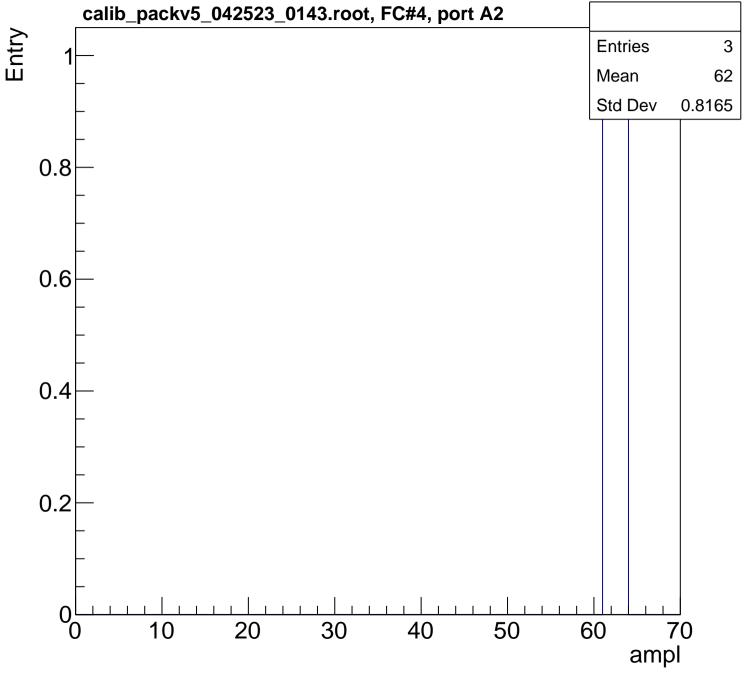


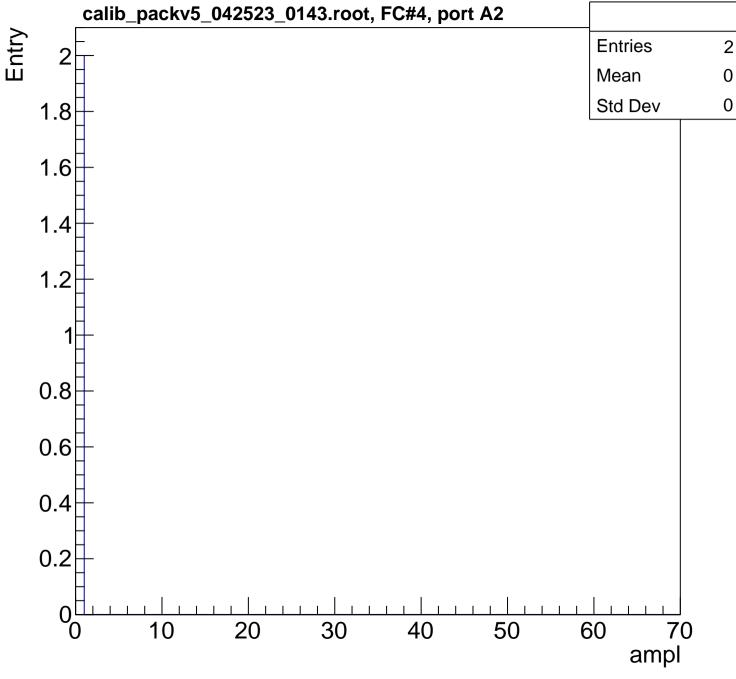


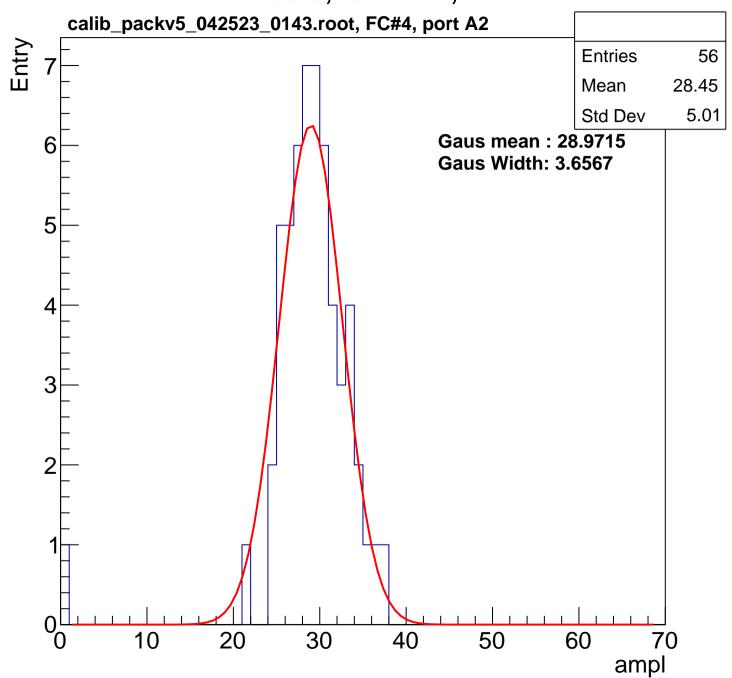


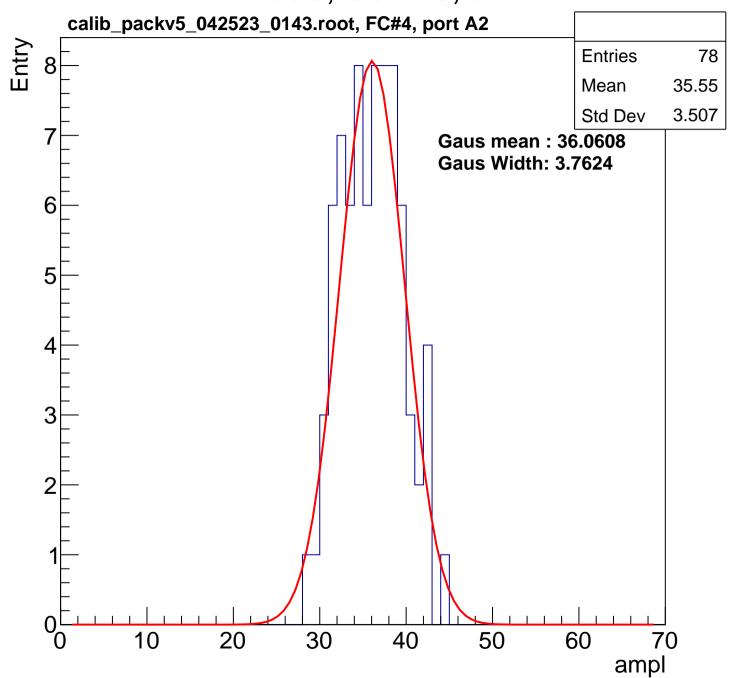


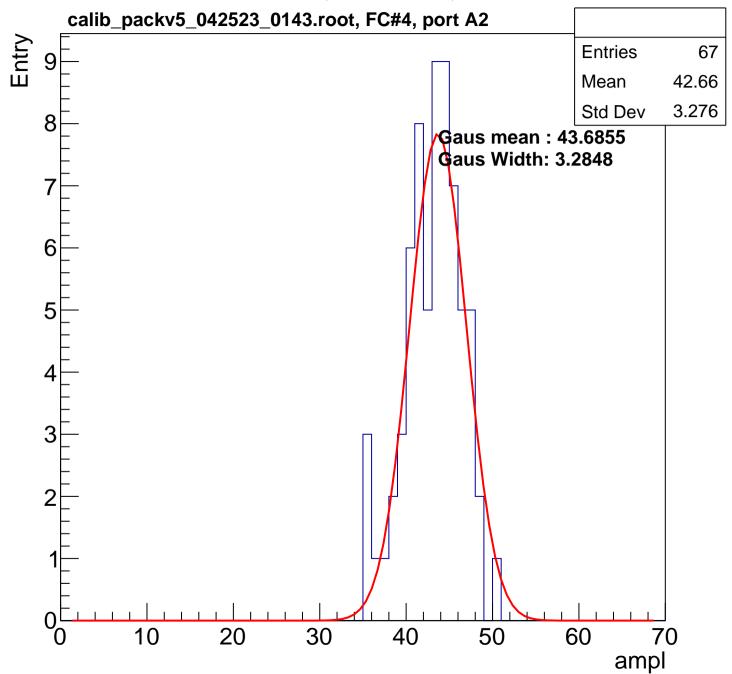


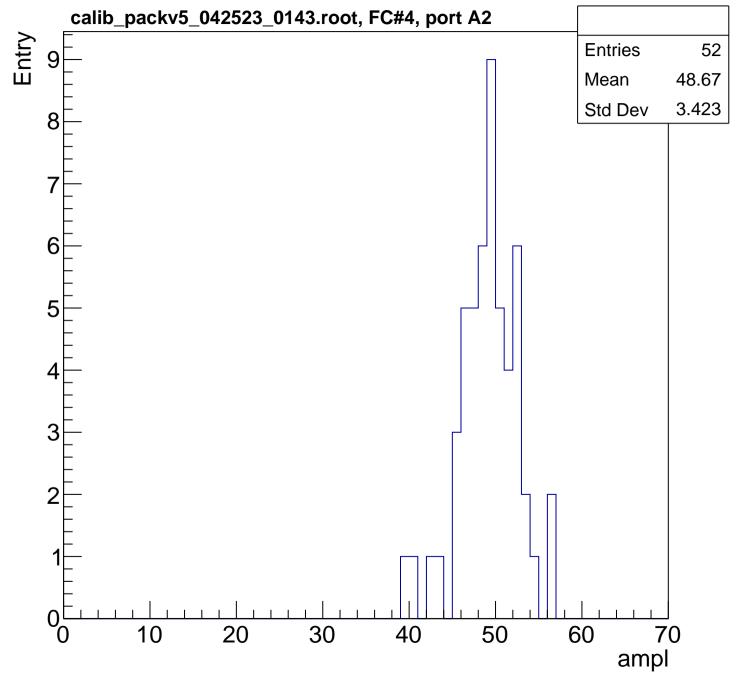


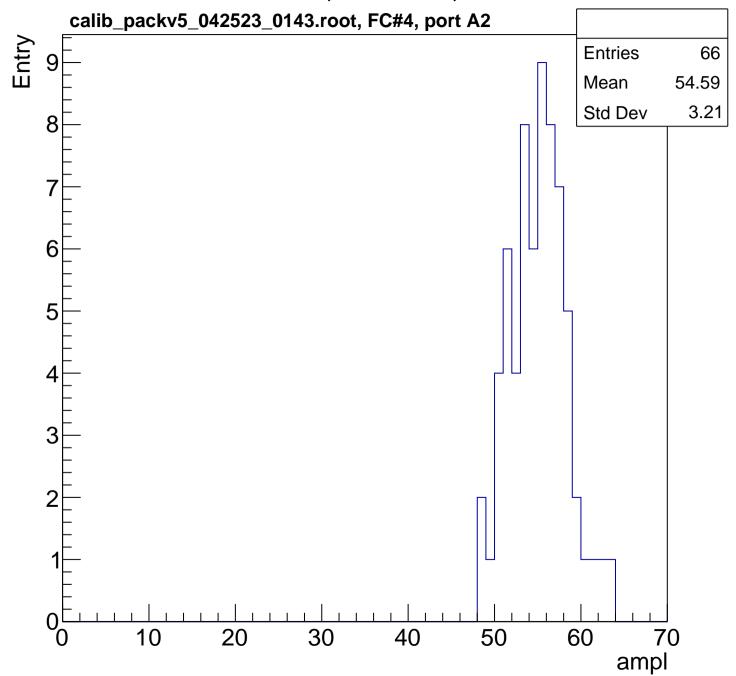


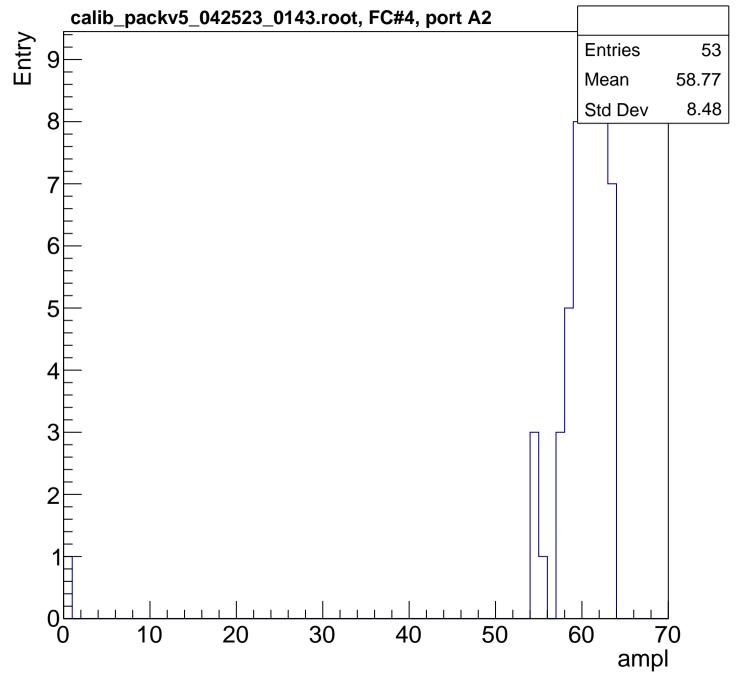


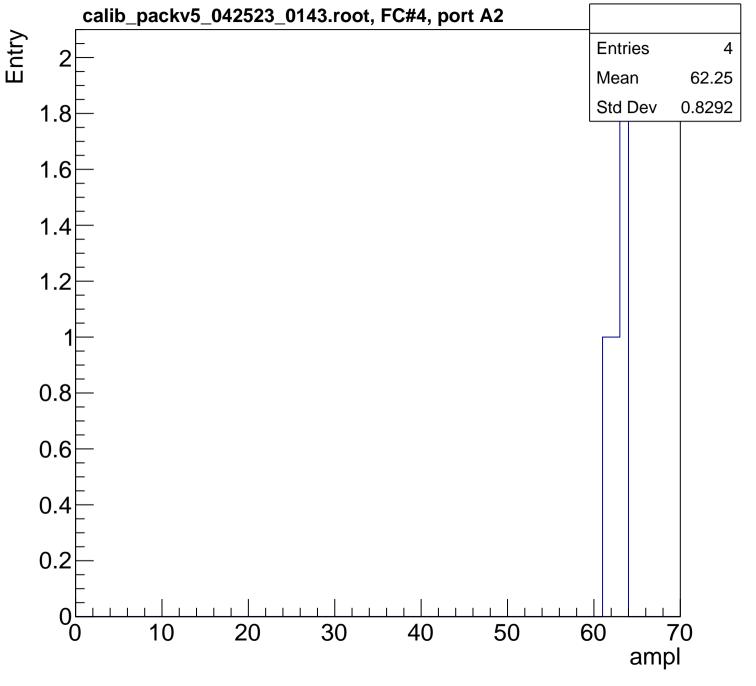


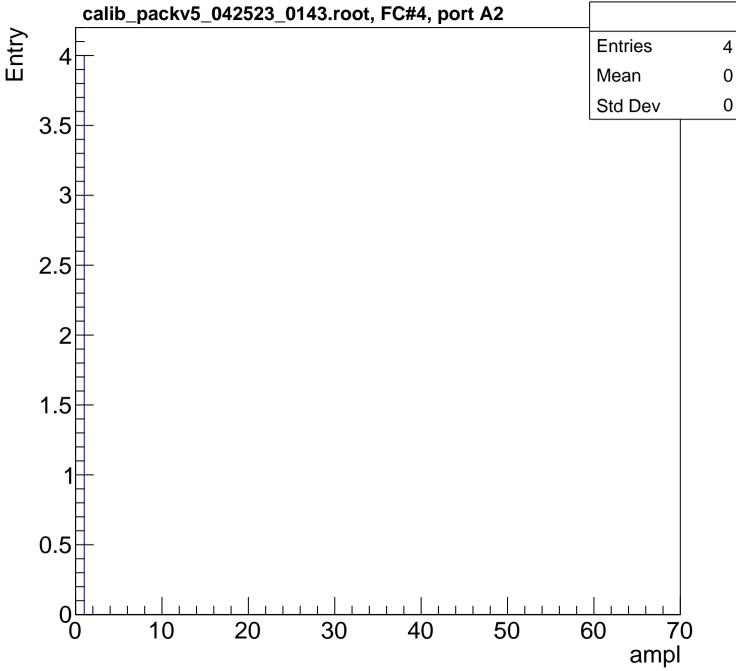


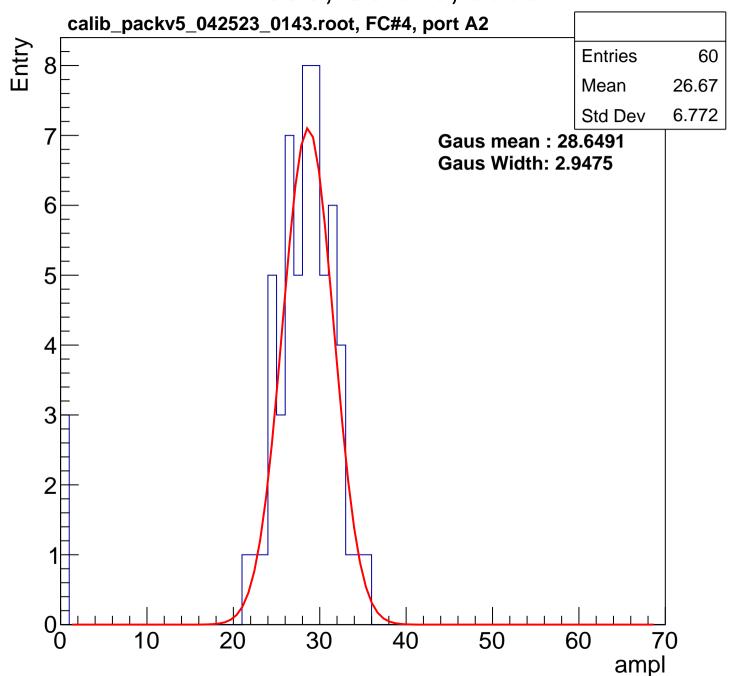


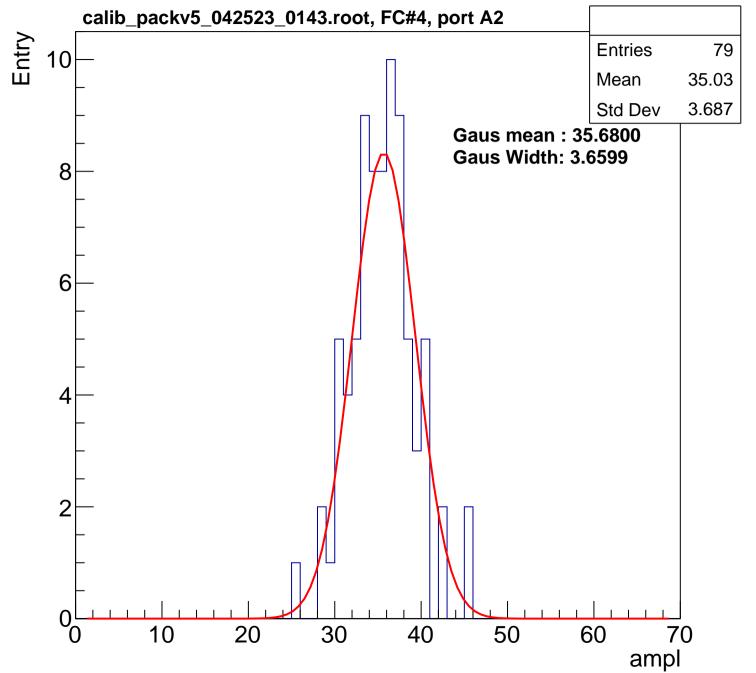


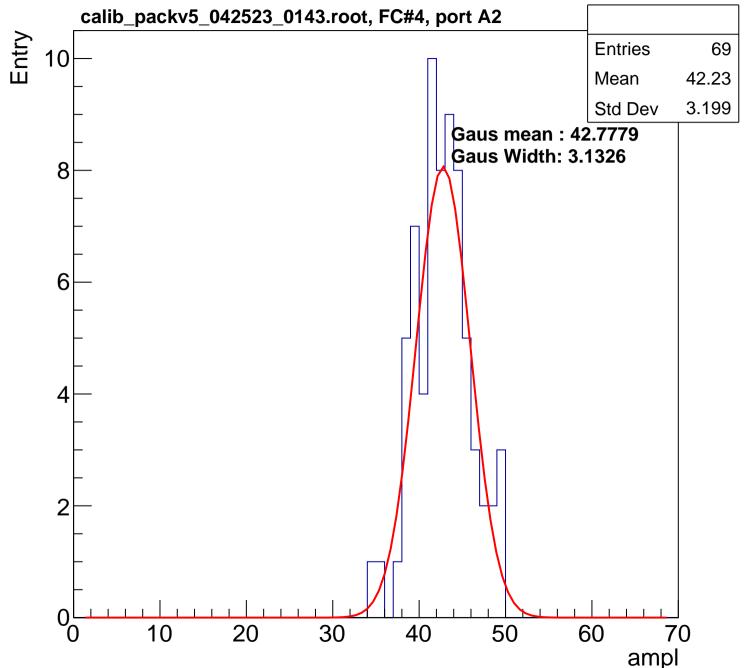


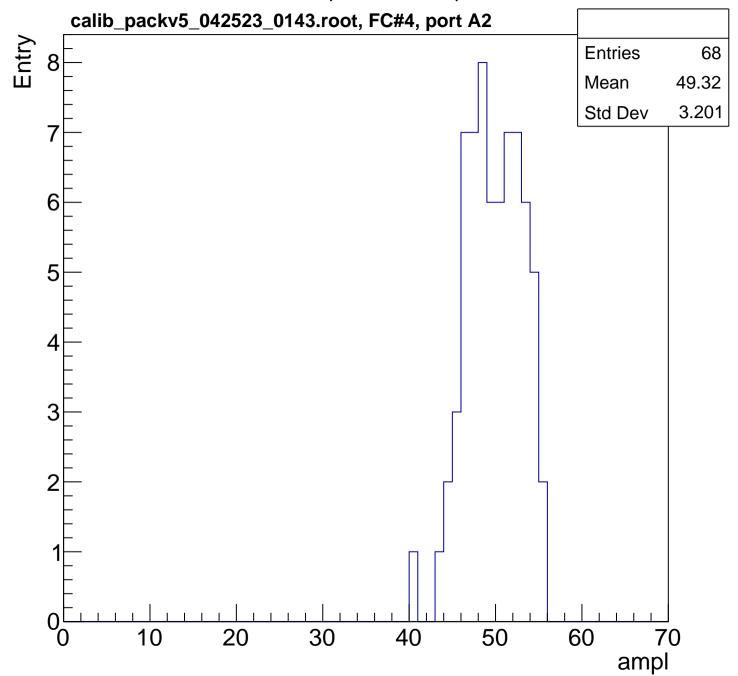


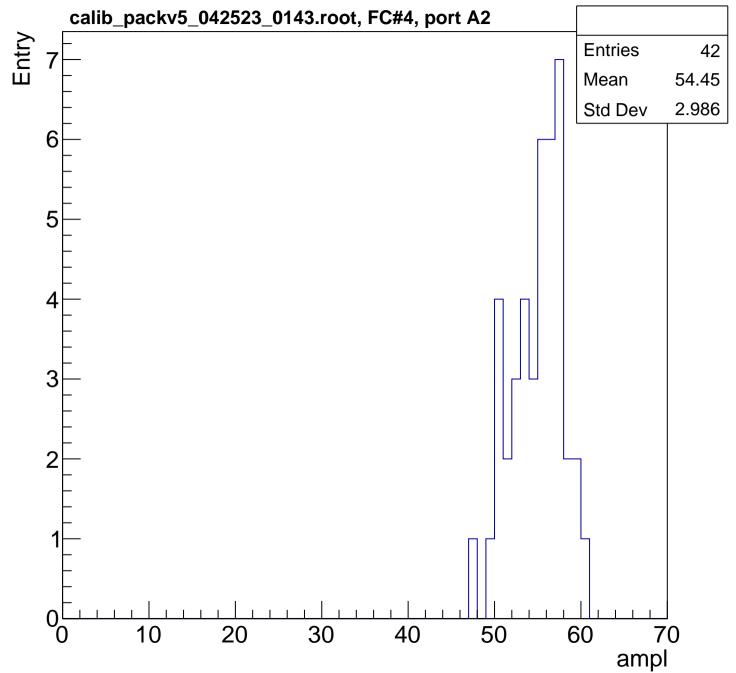


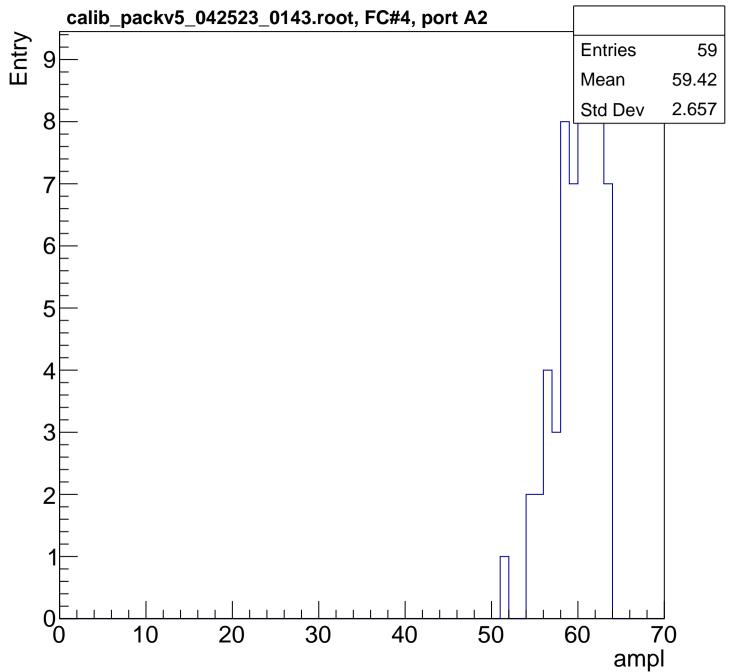


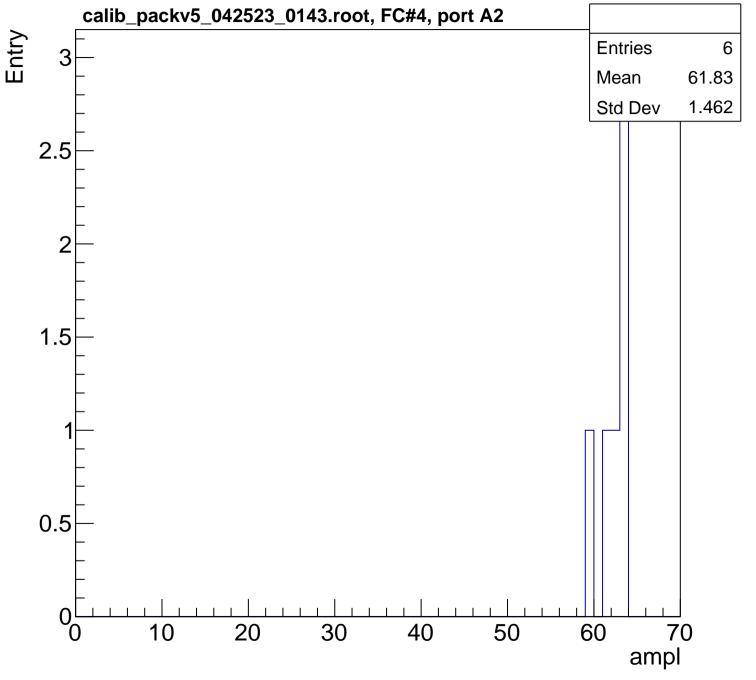


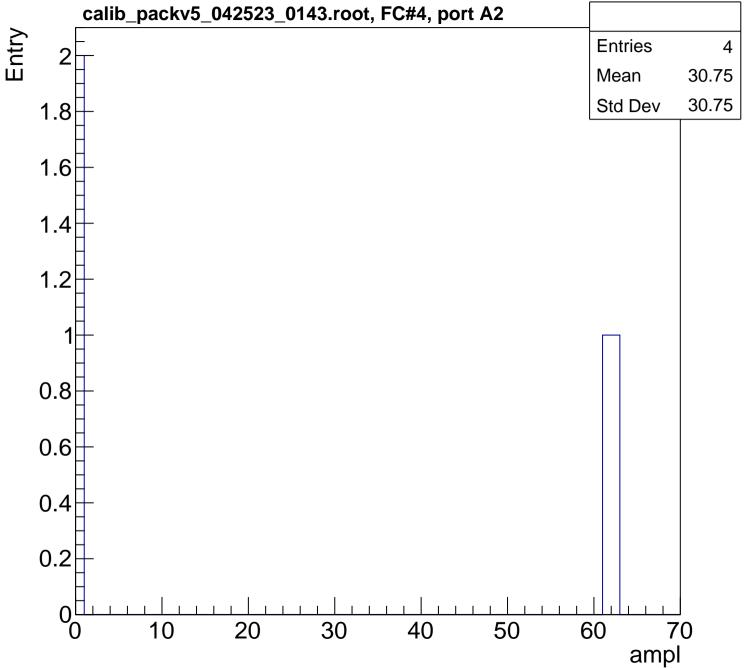


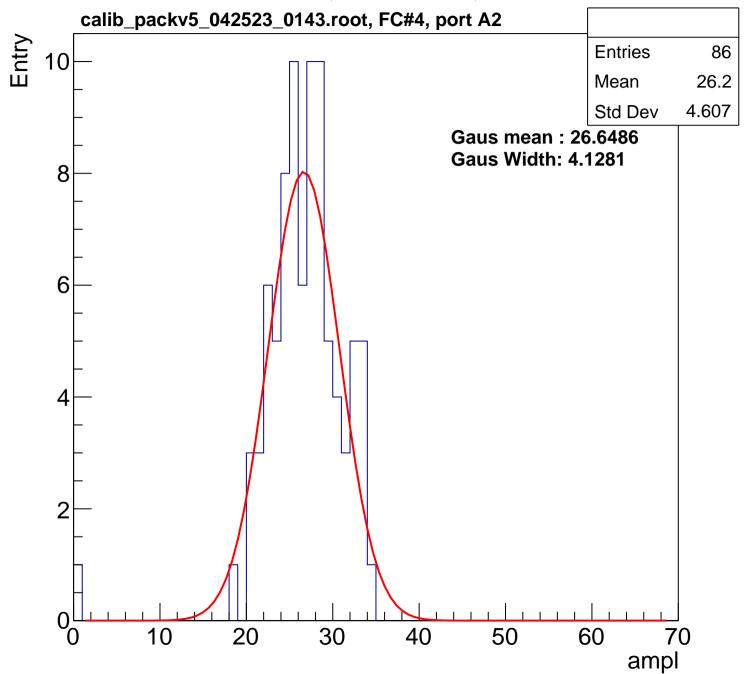


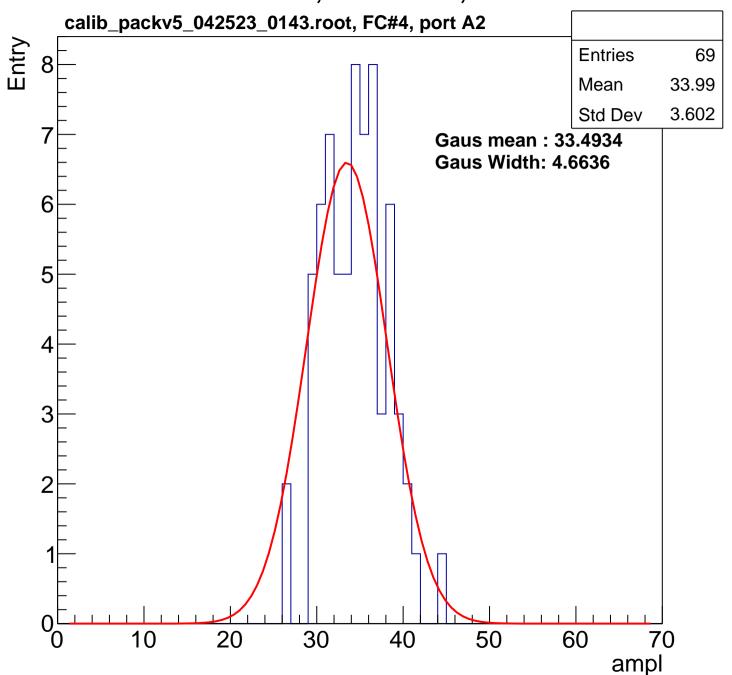


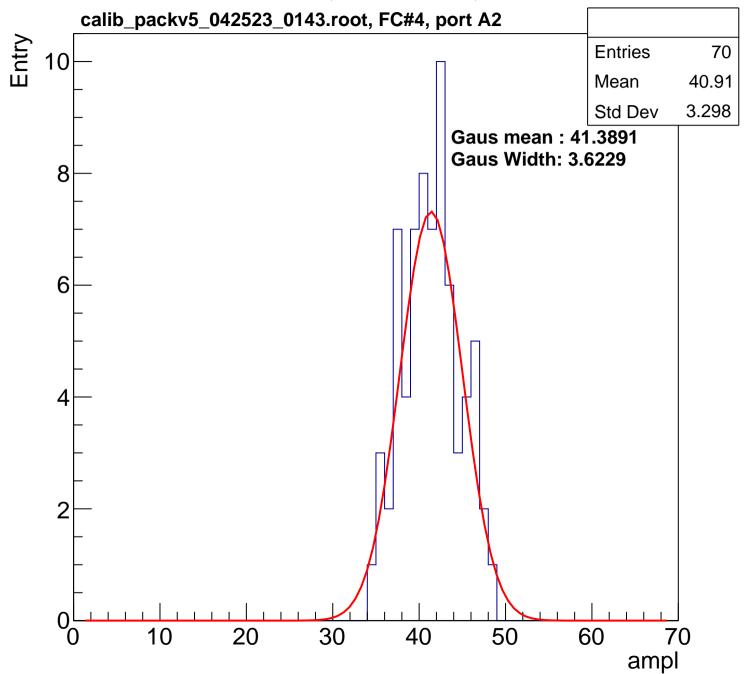


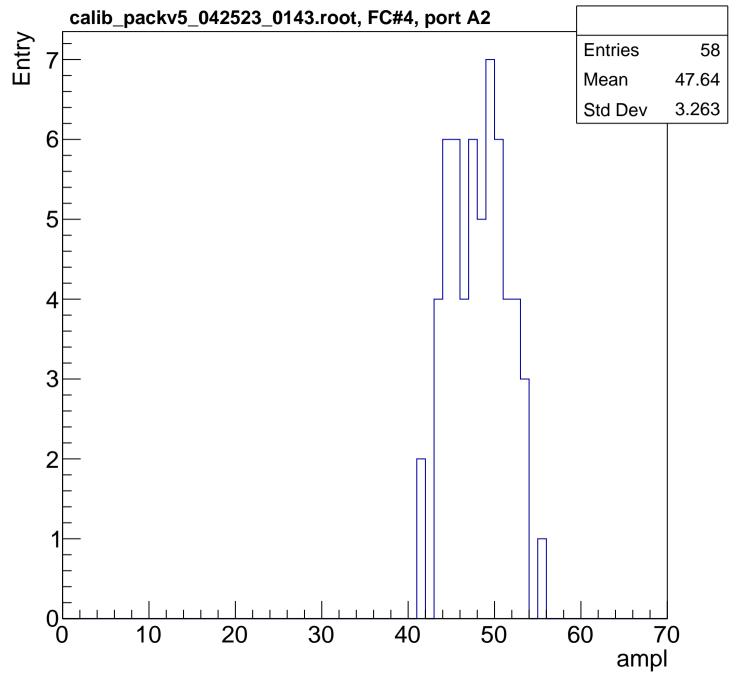


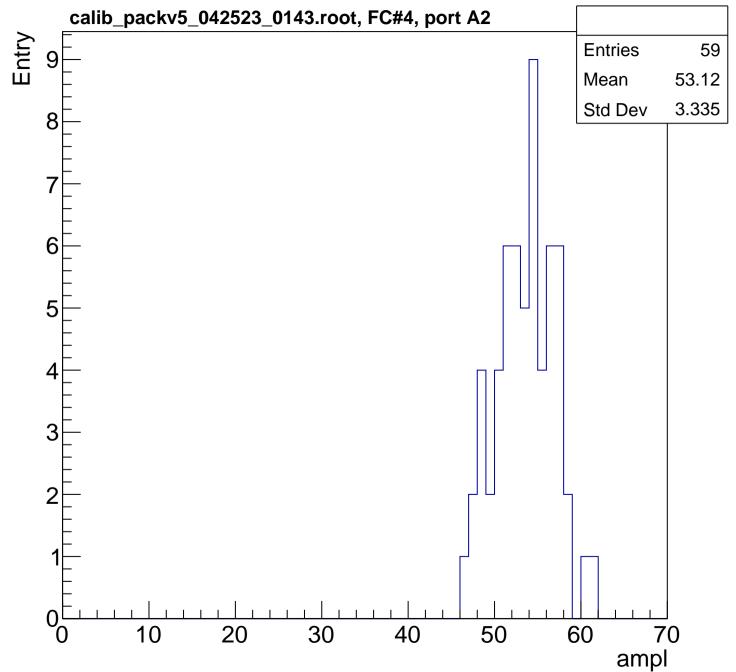


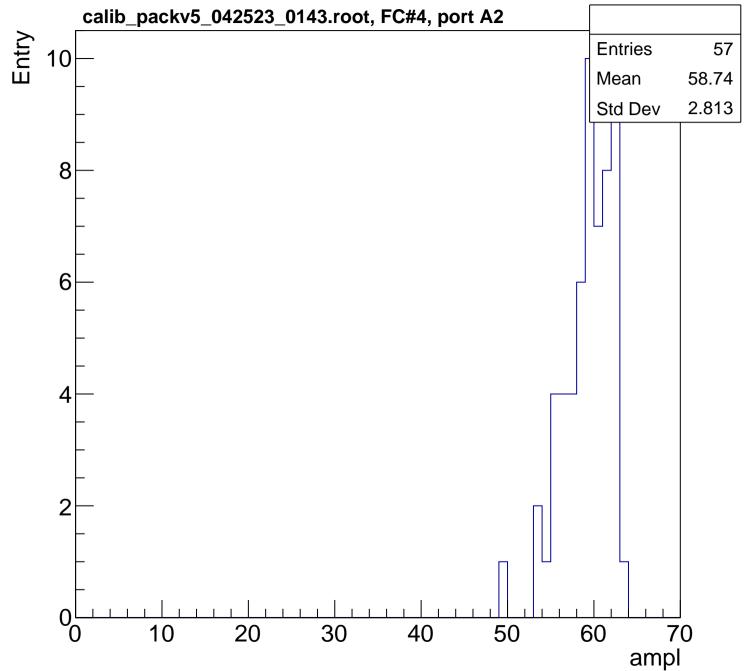


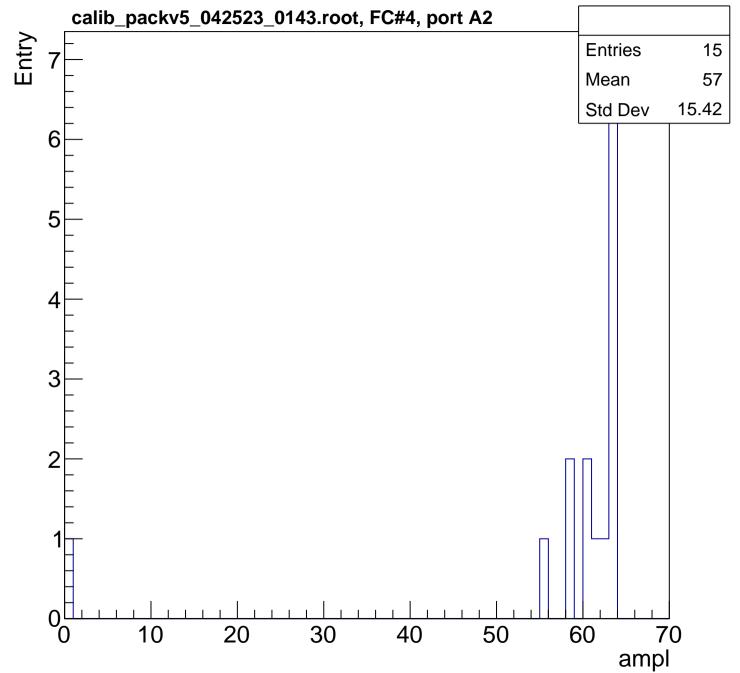


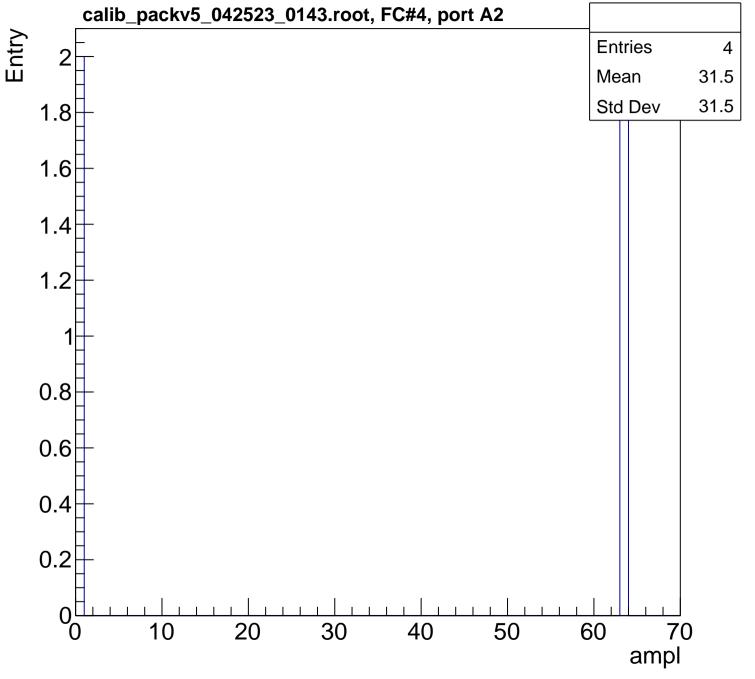


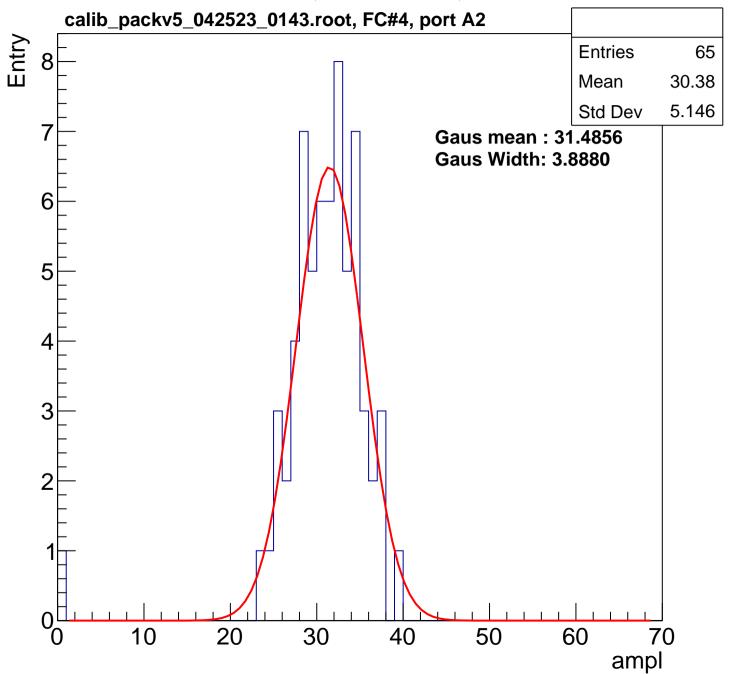


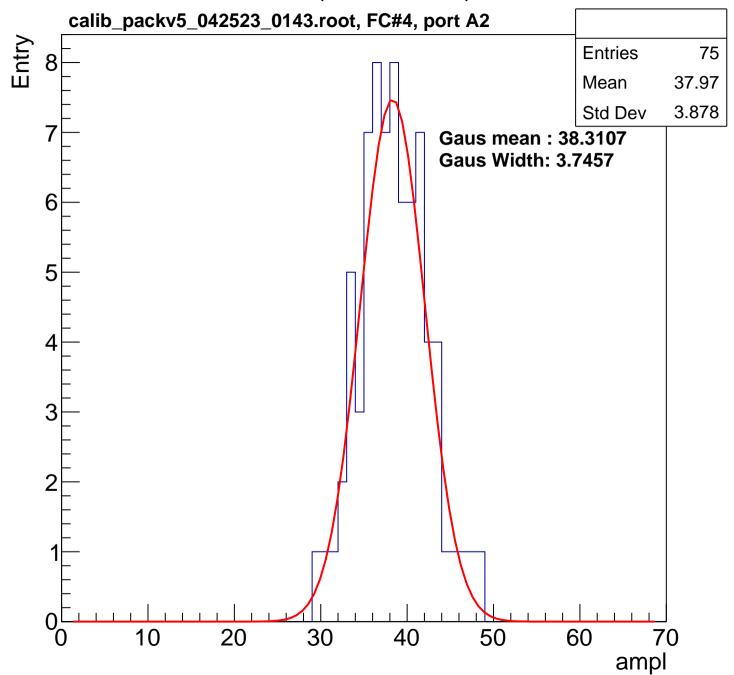


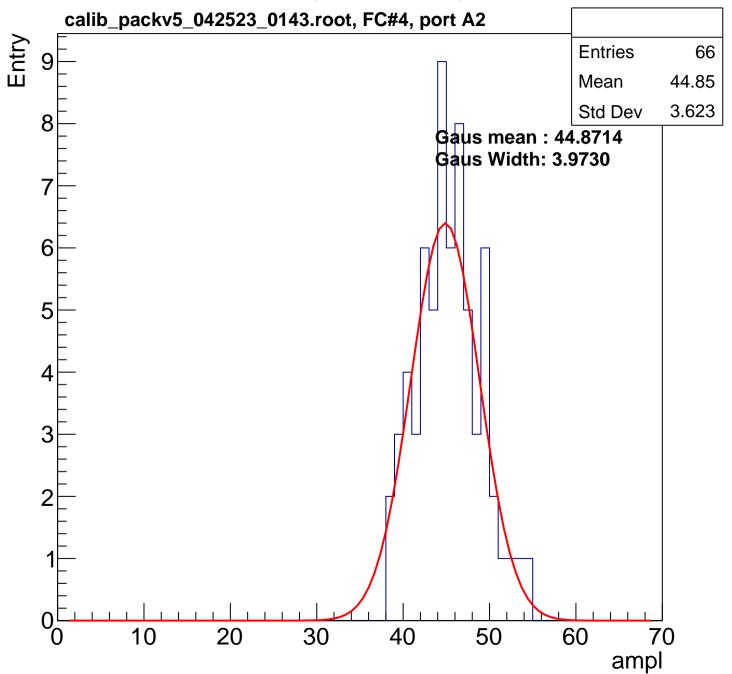


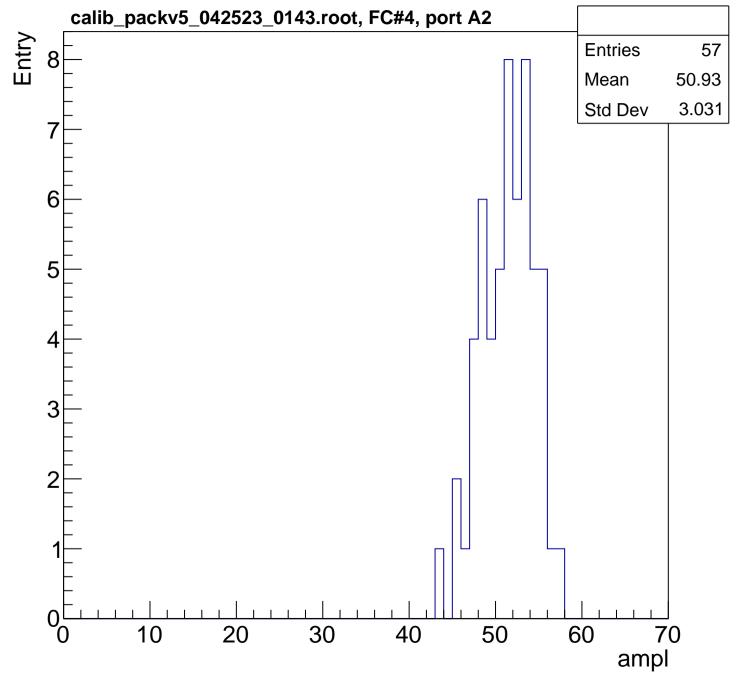


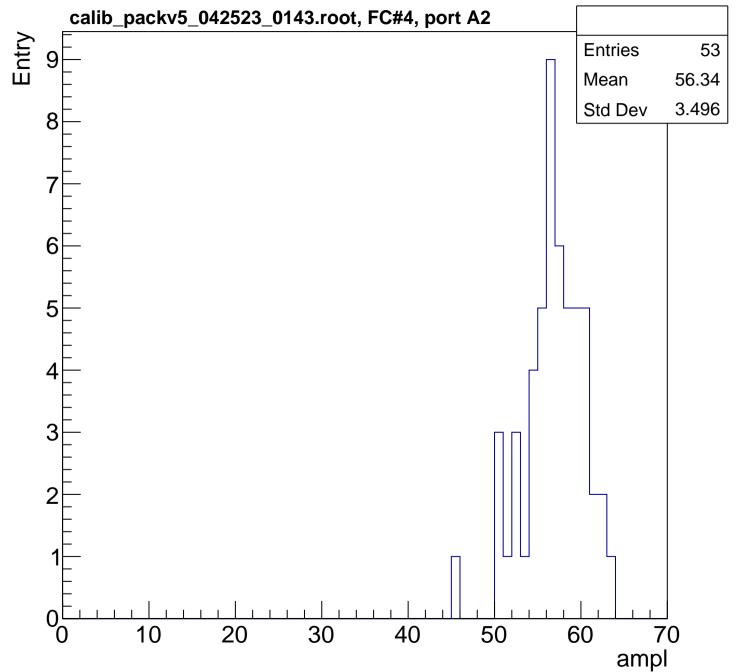


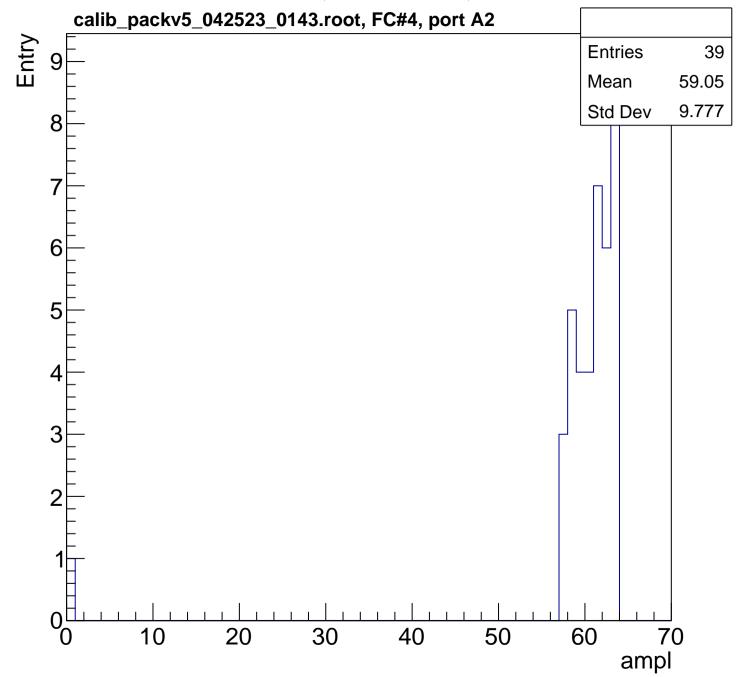


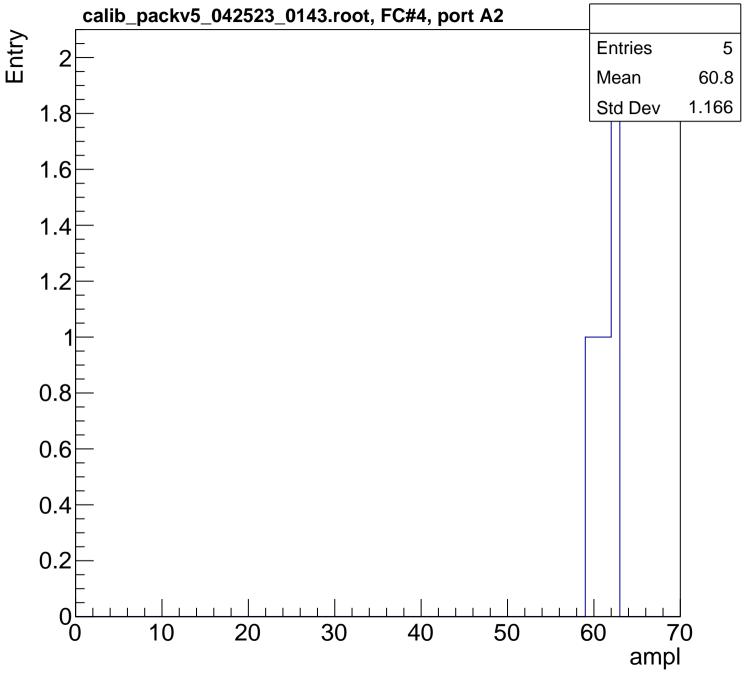






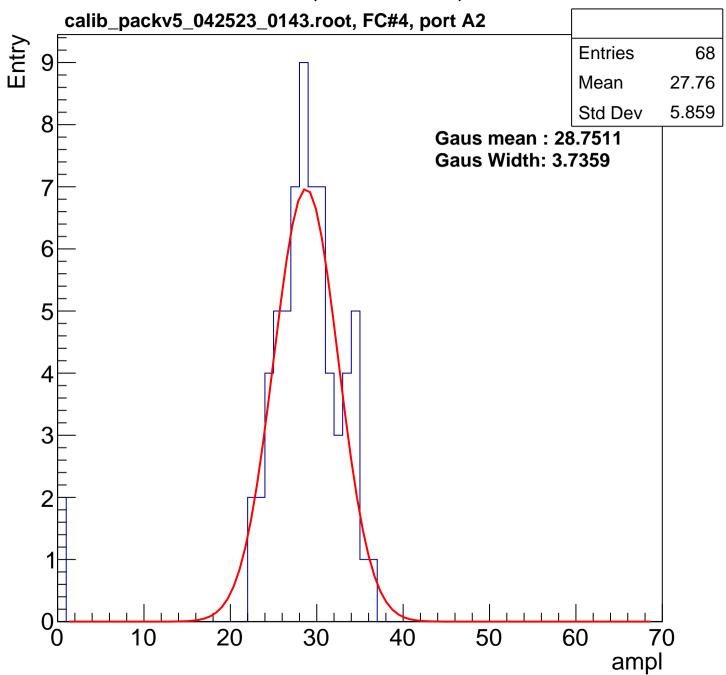


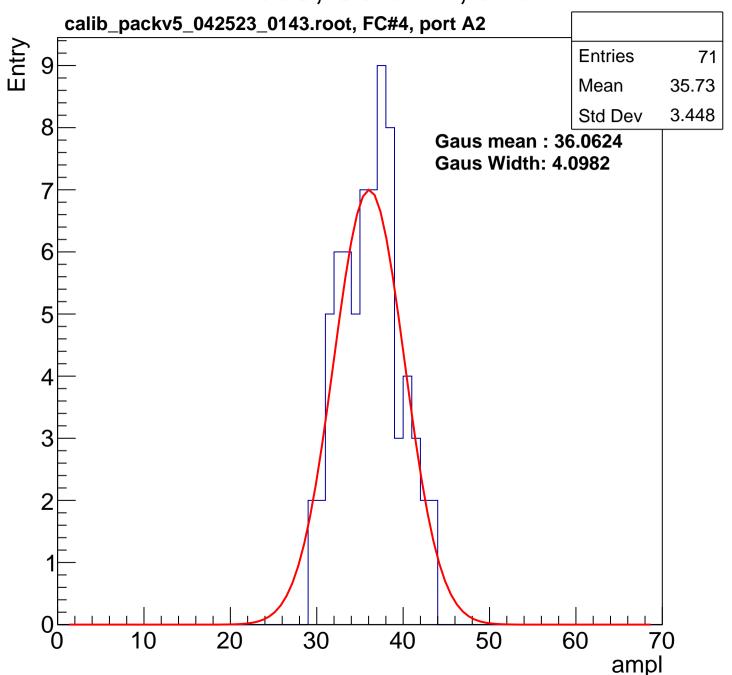


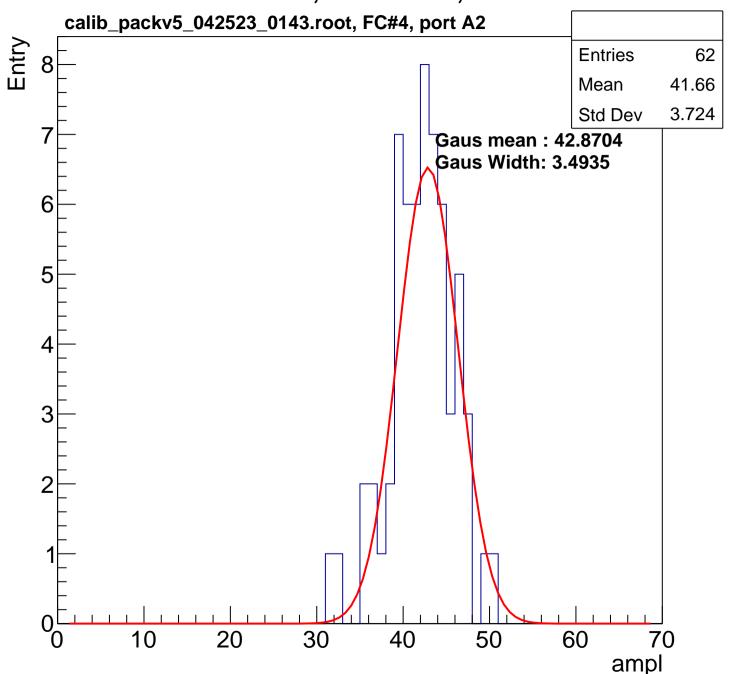


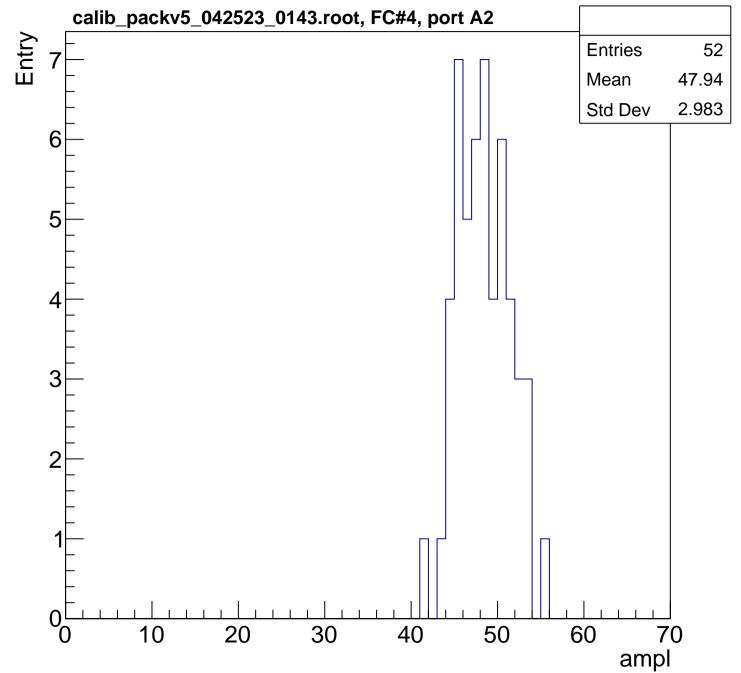
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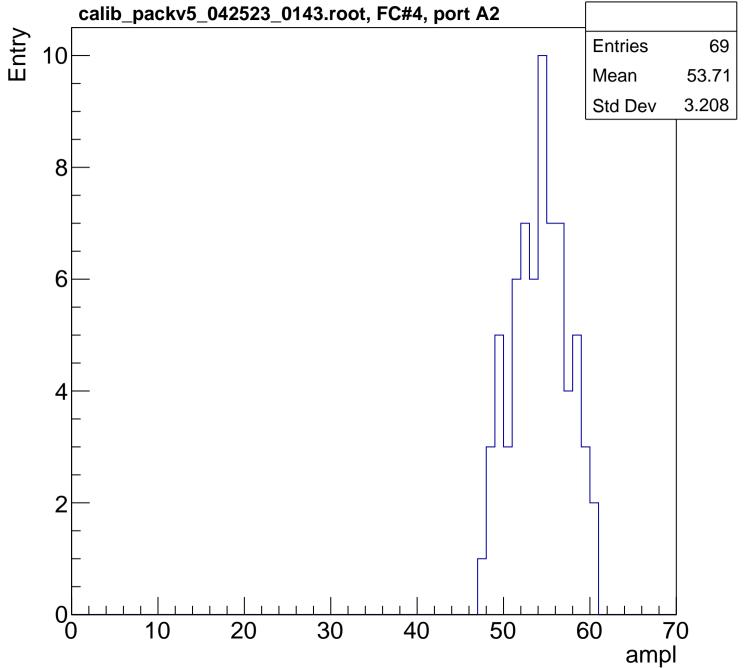
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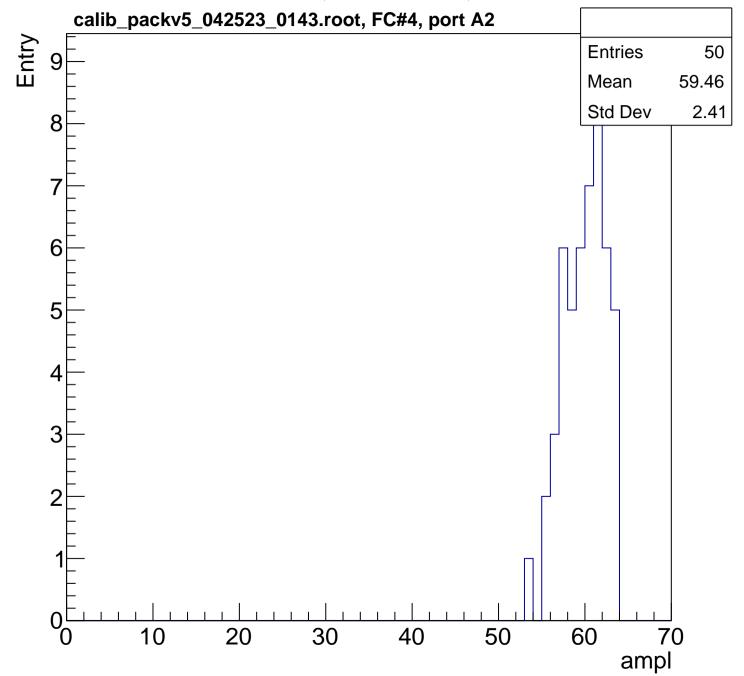


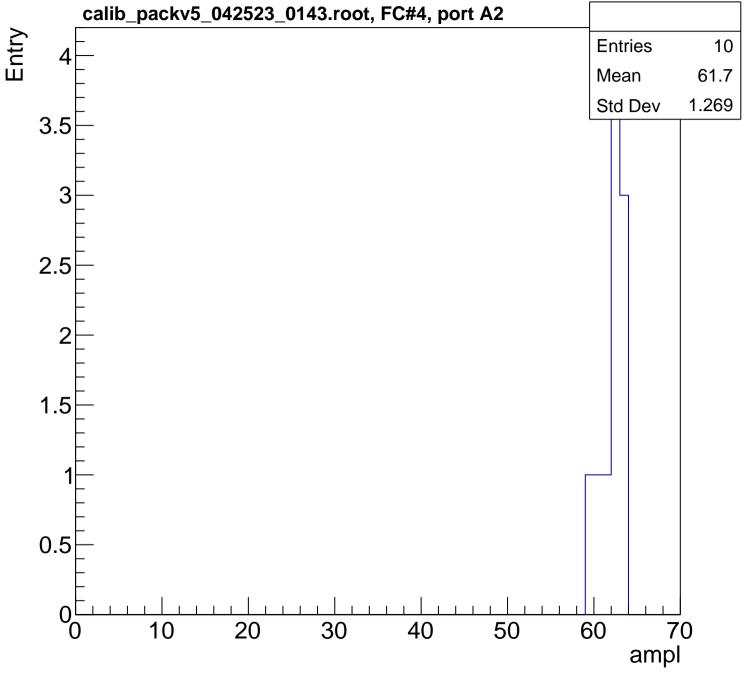


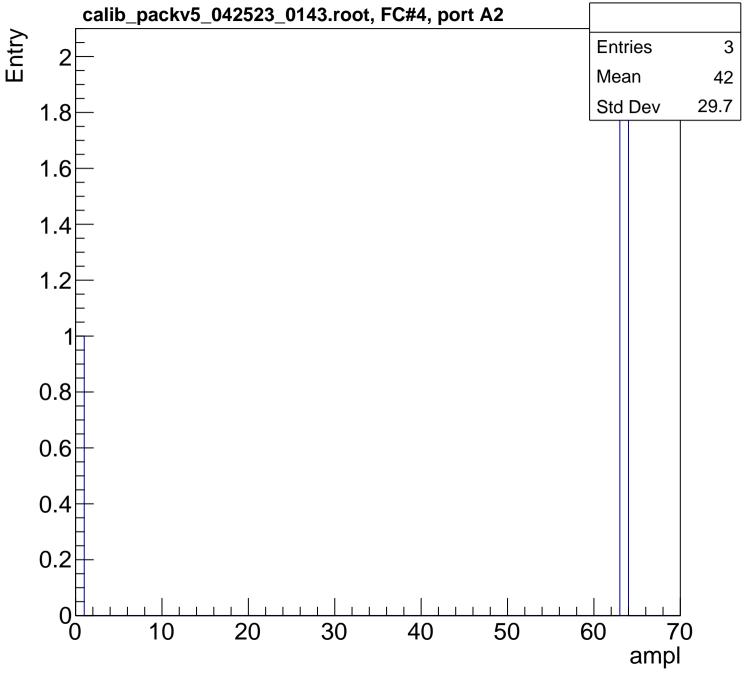


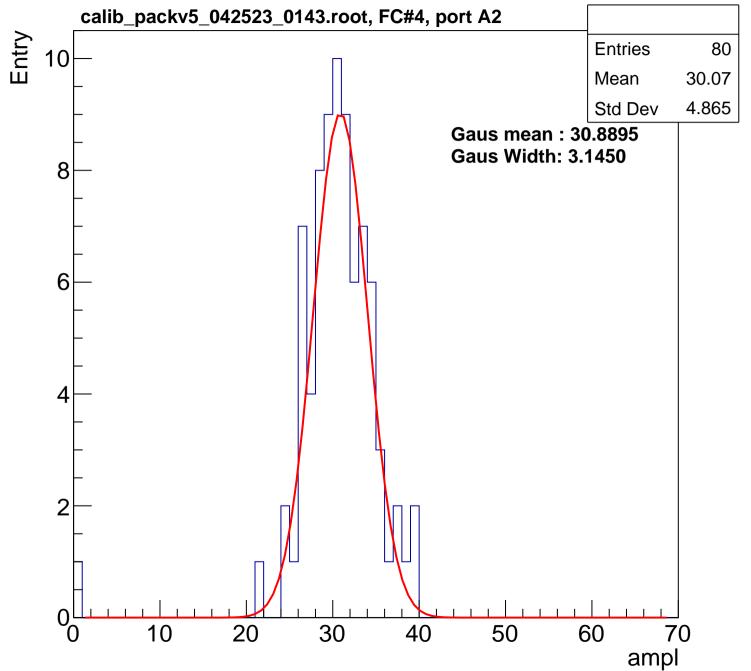


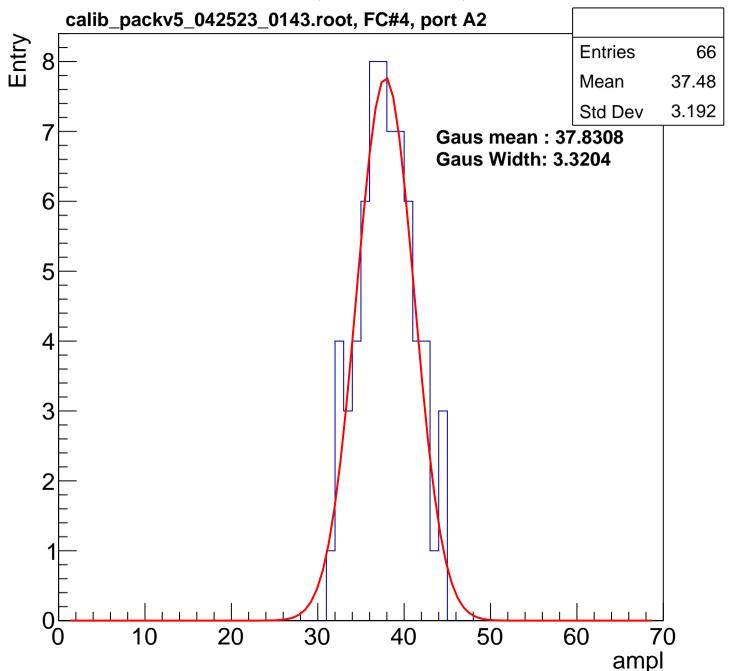


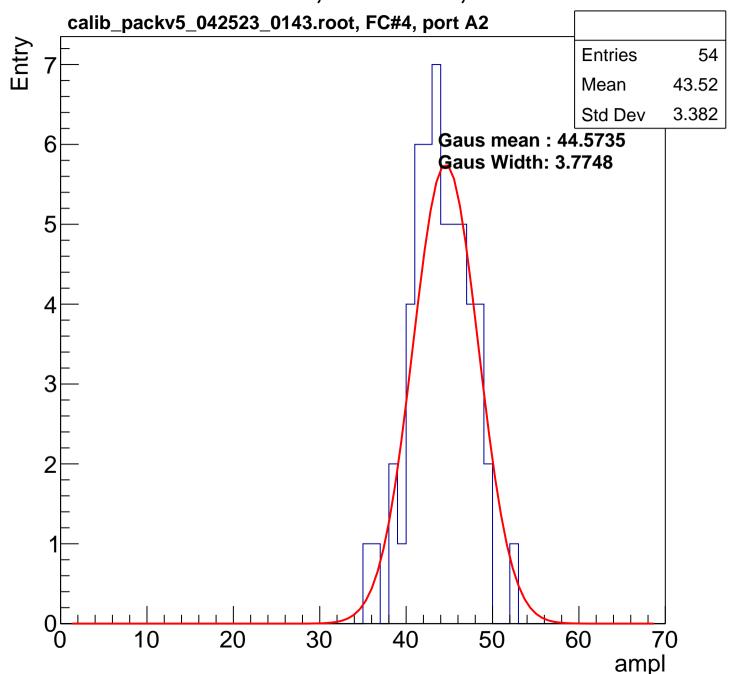


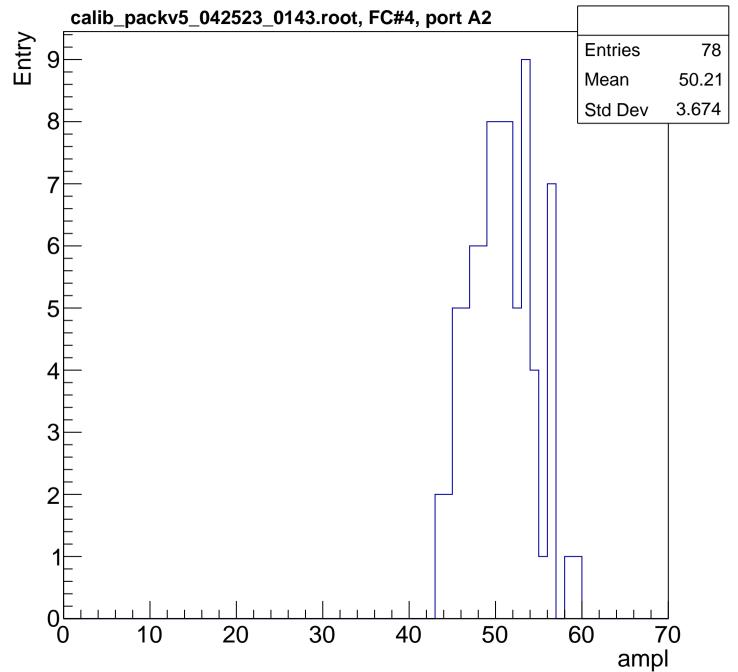


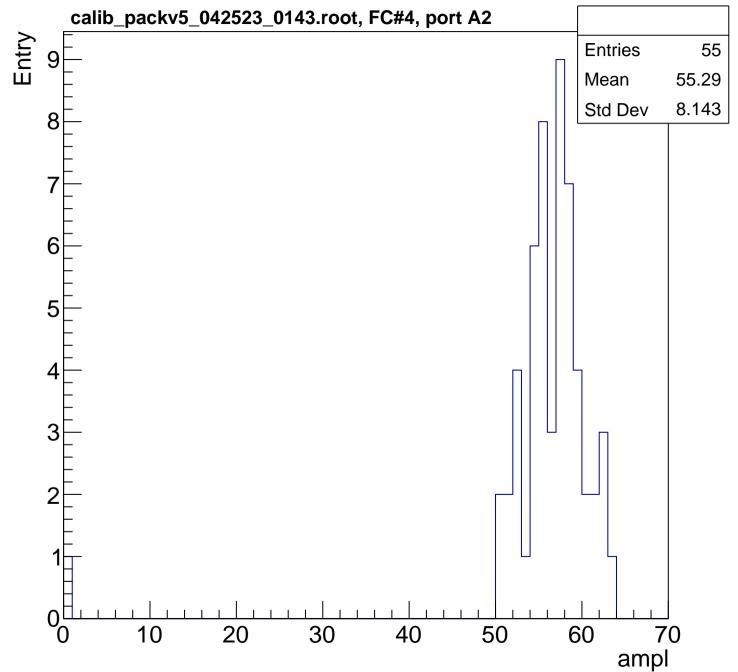


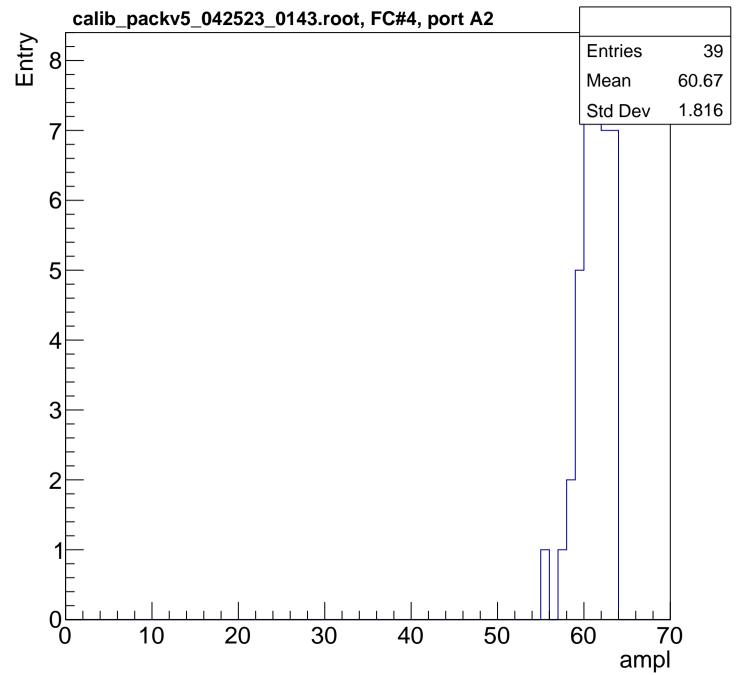


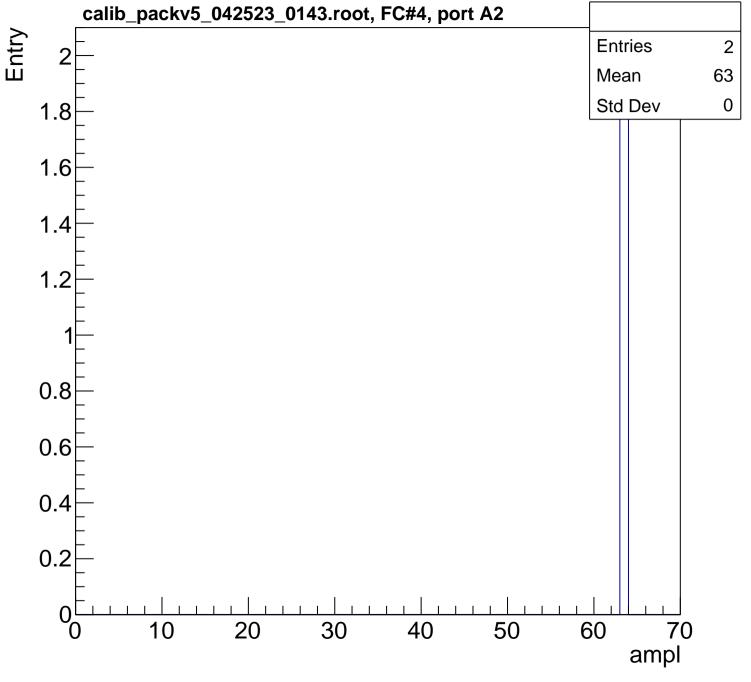


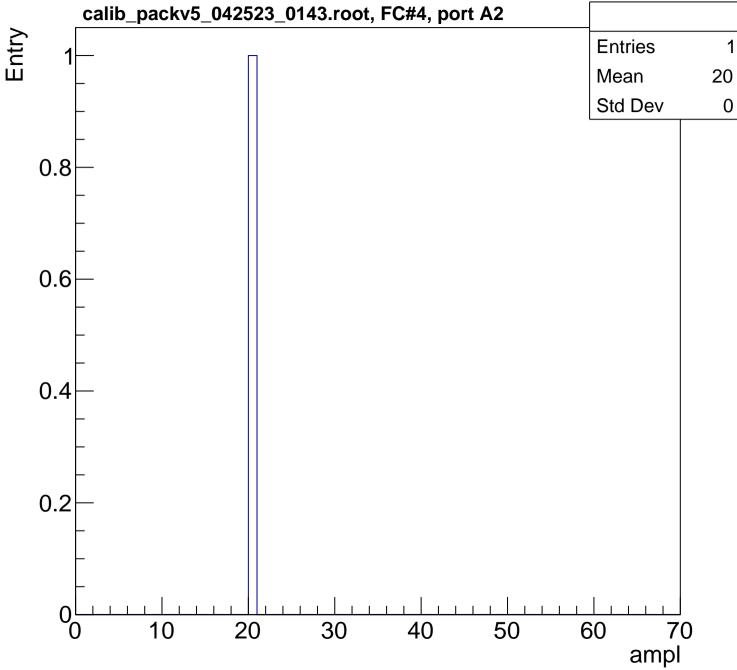


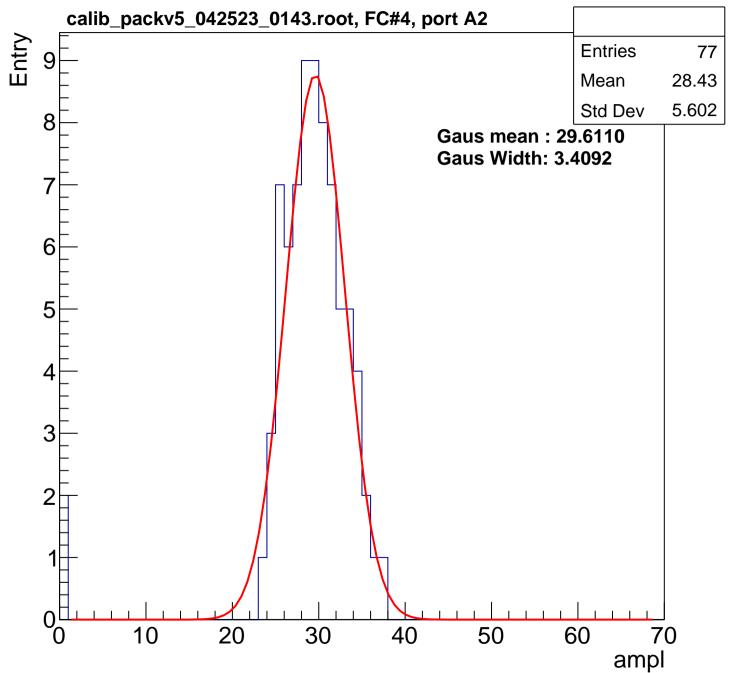


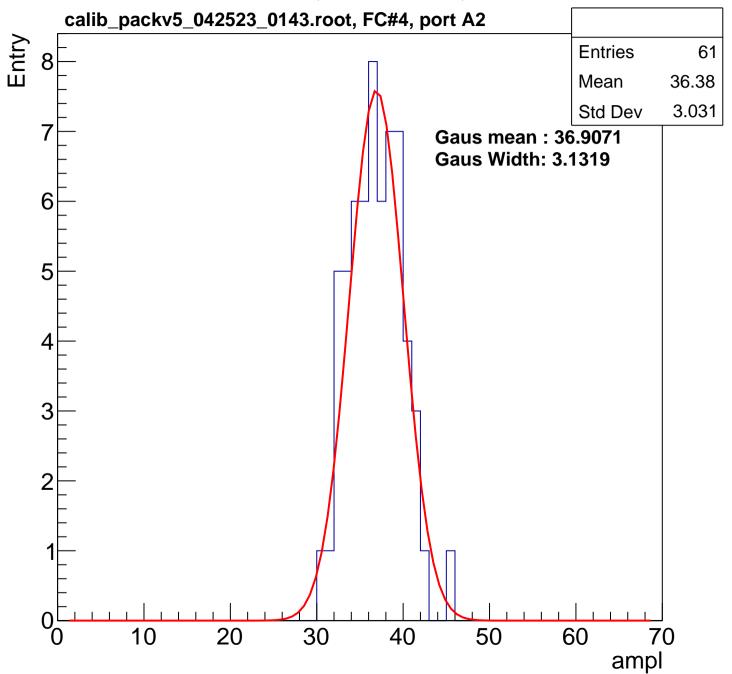


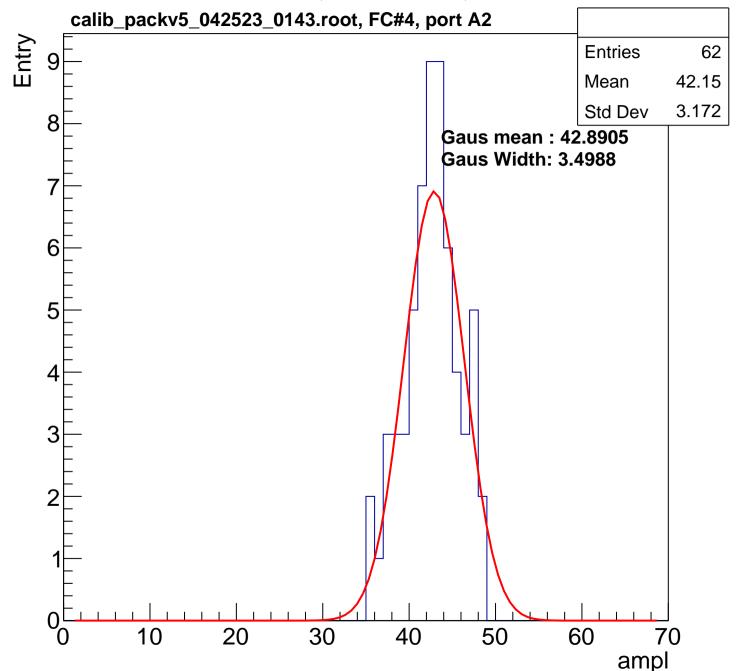


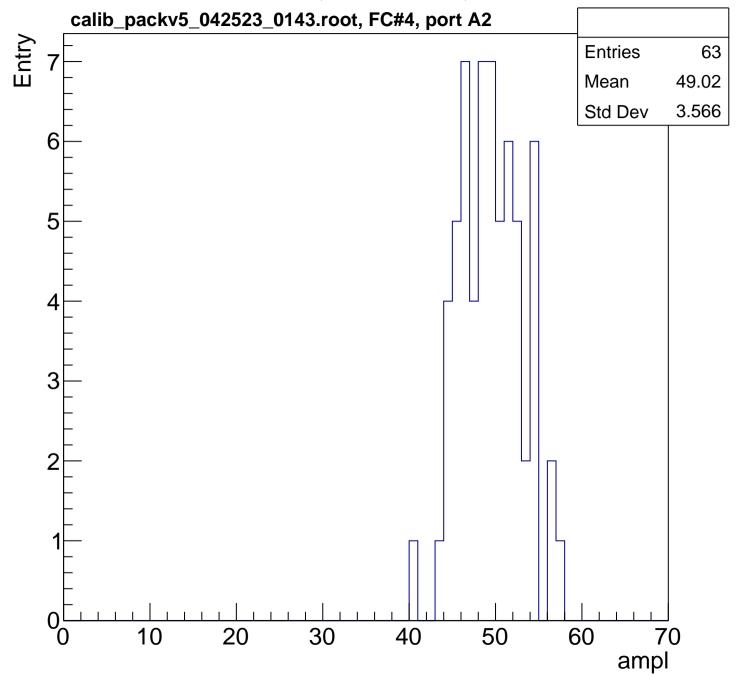


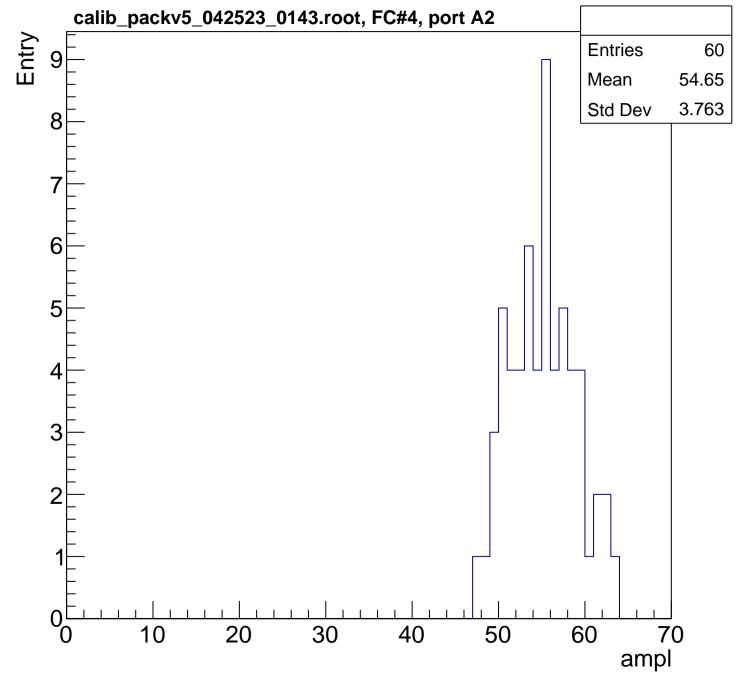


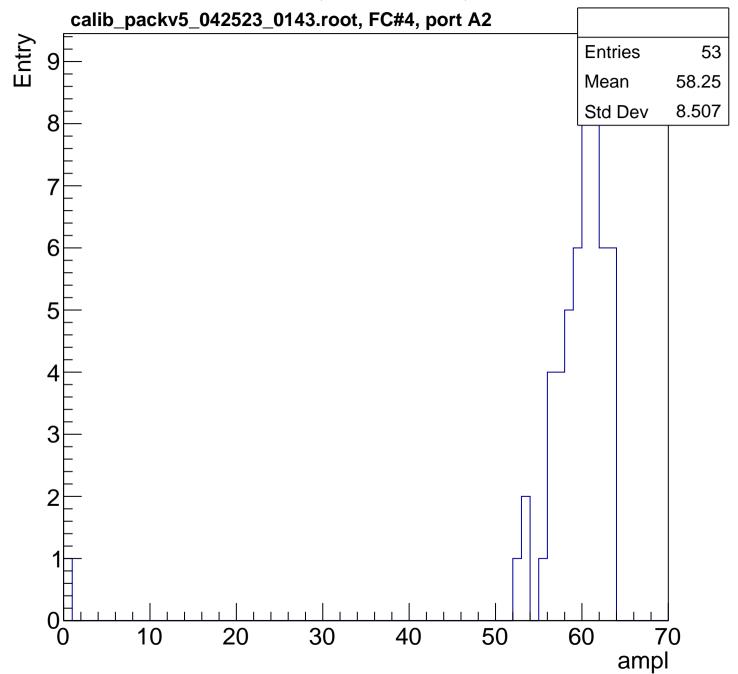


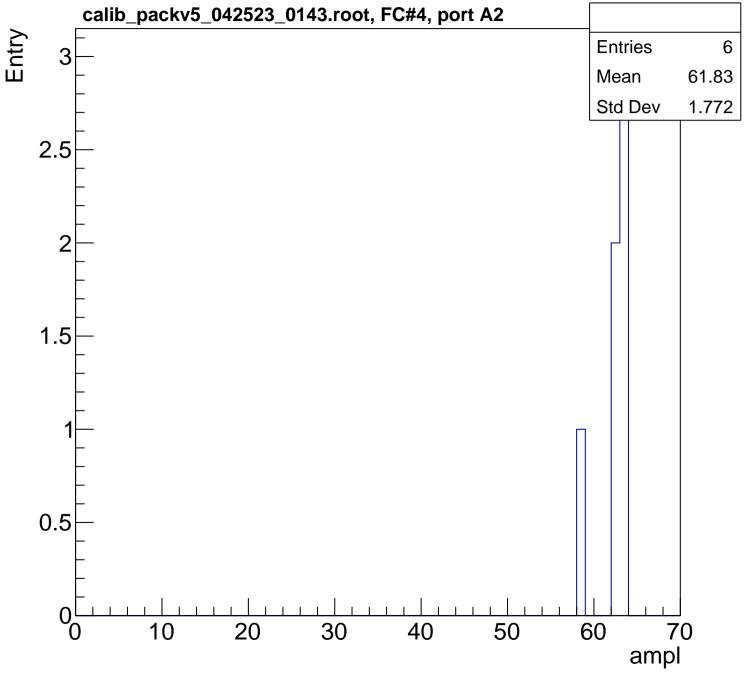


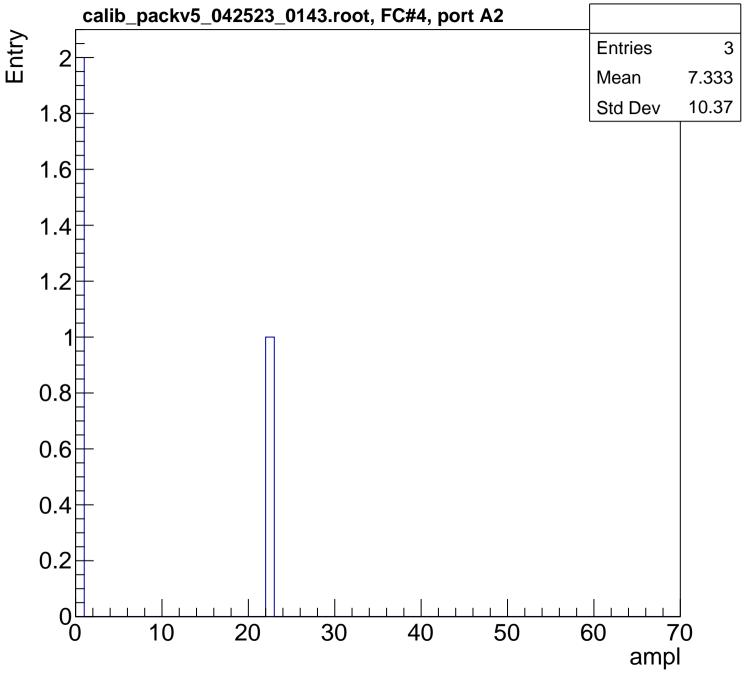


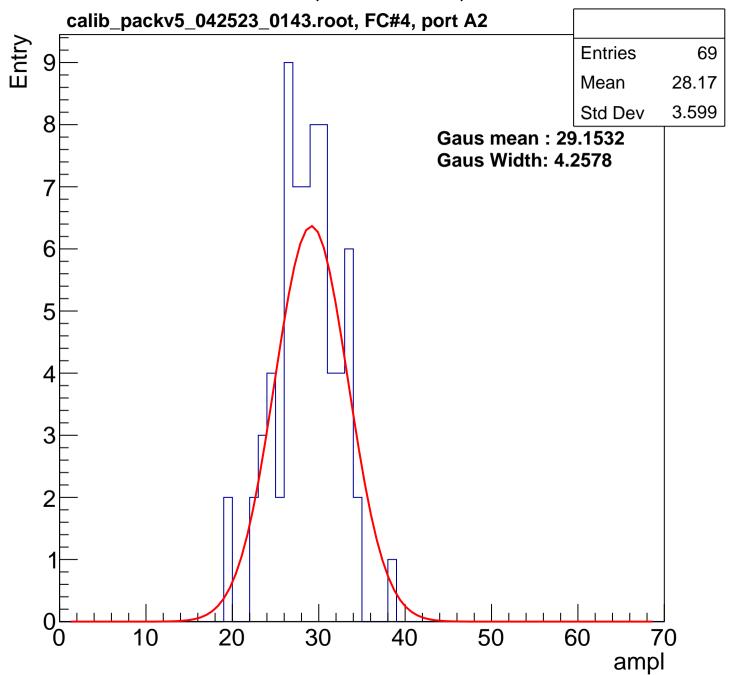


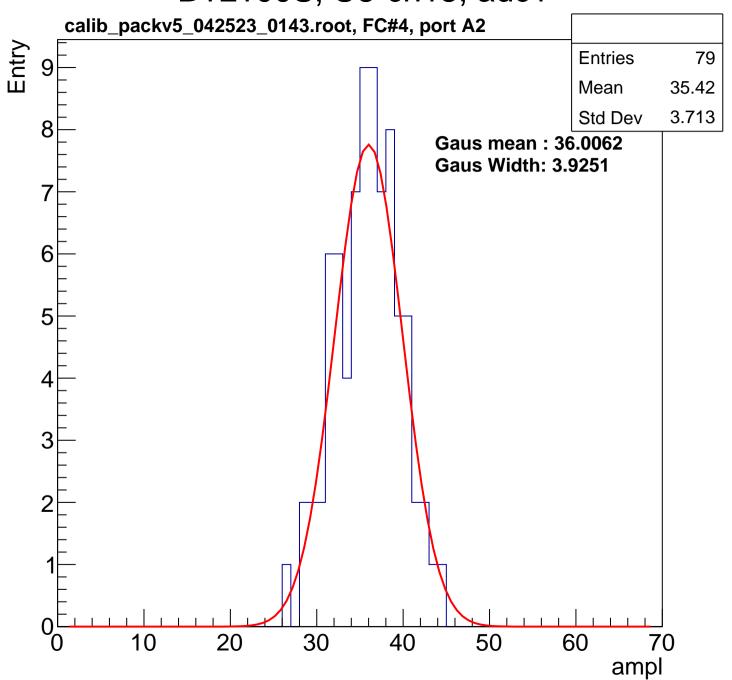


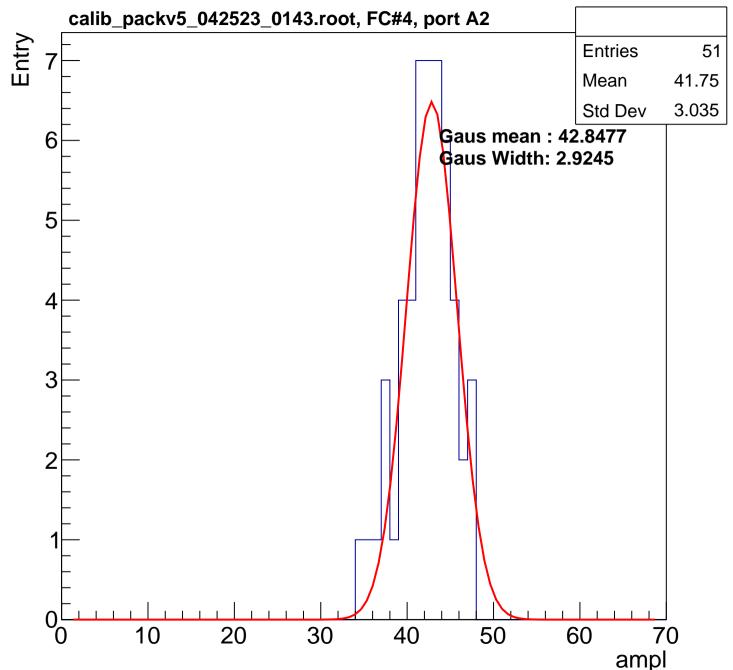


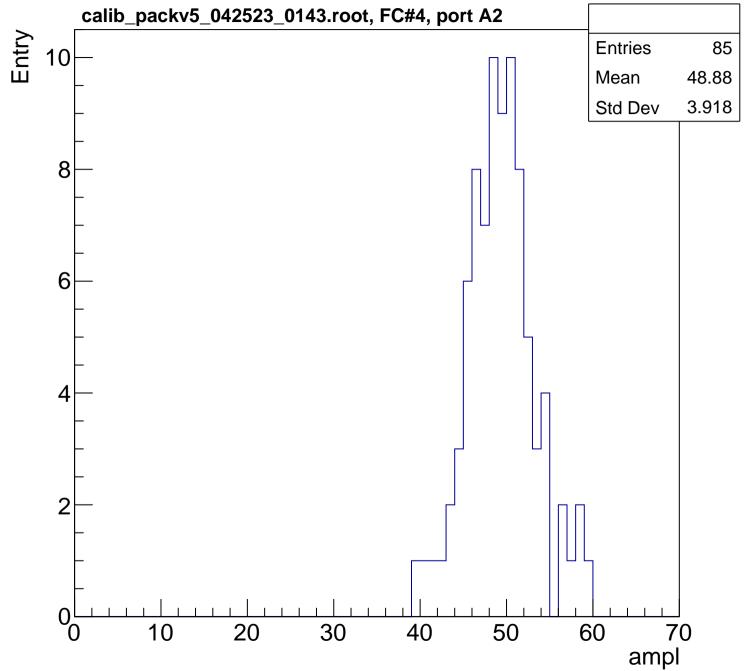


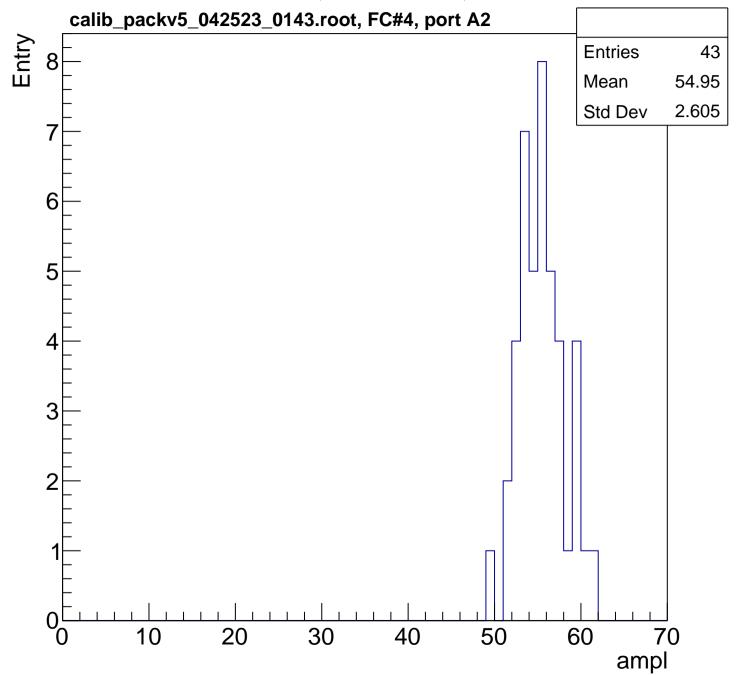


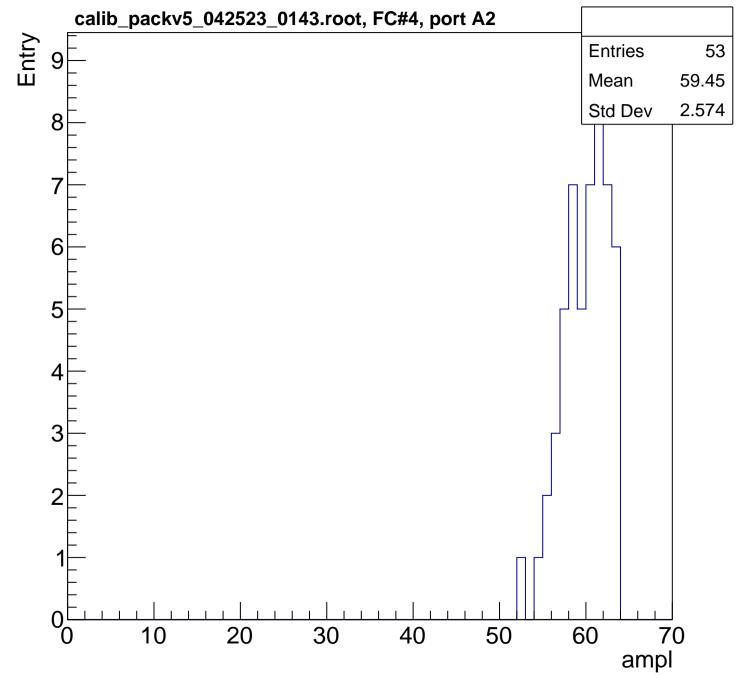


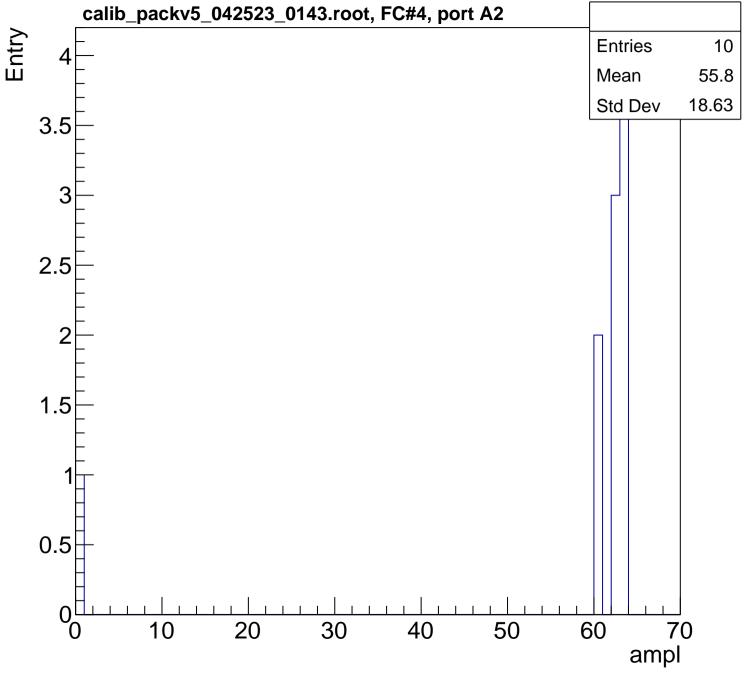










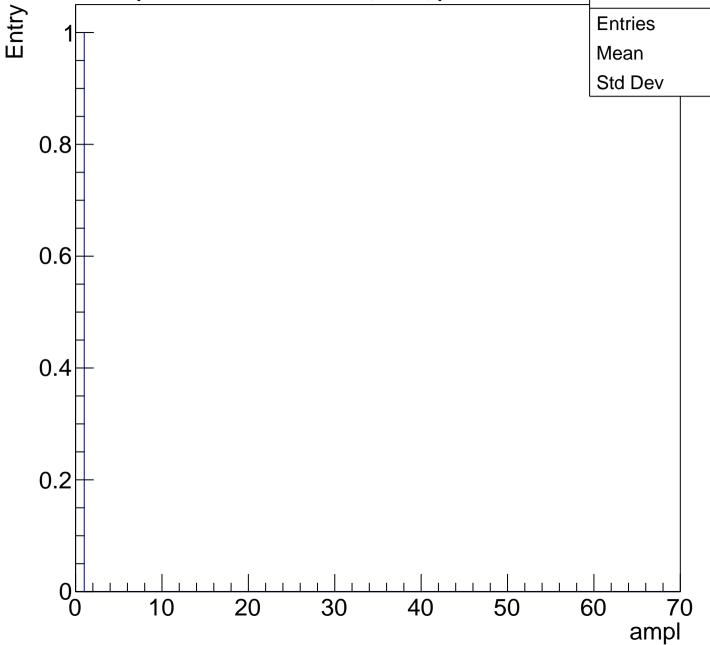


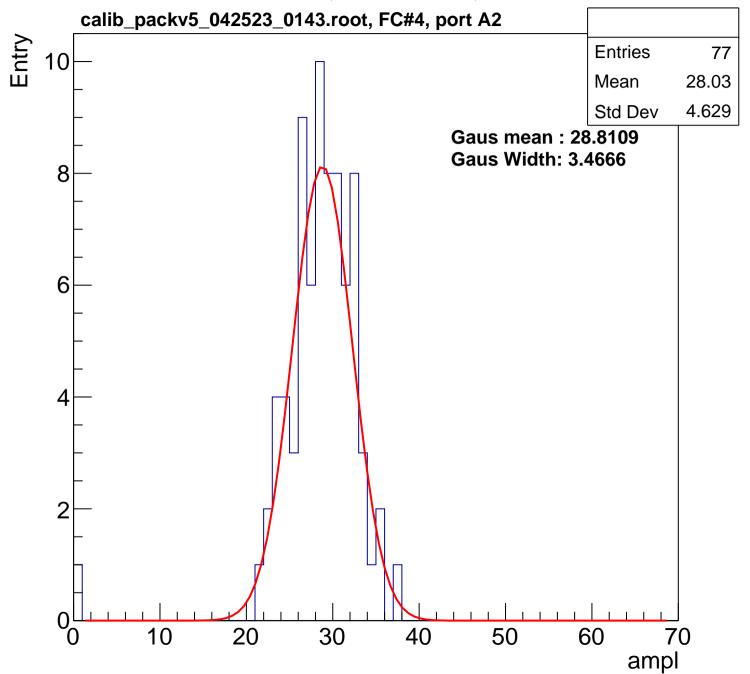
B1L100S, U3-ch15, adc7 calib_packv5_042523_0143.root, FC#4, port A2

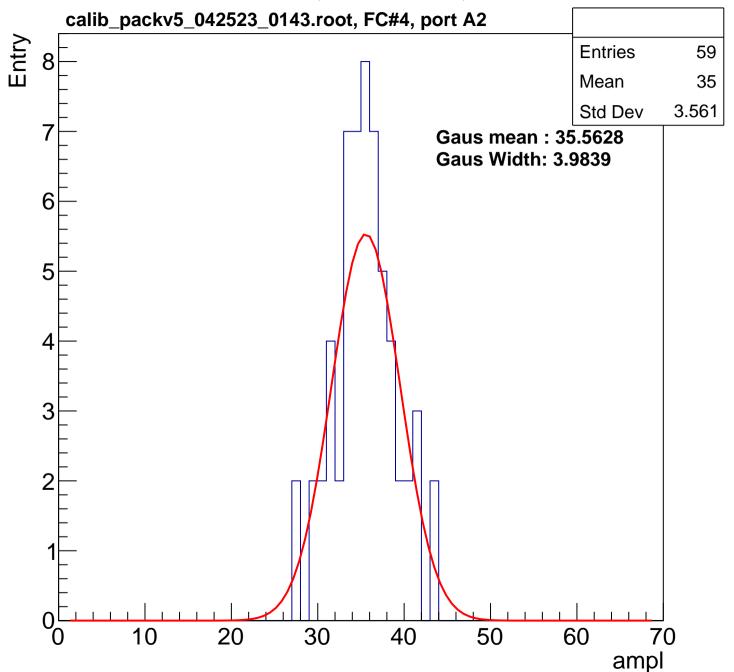
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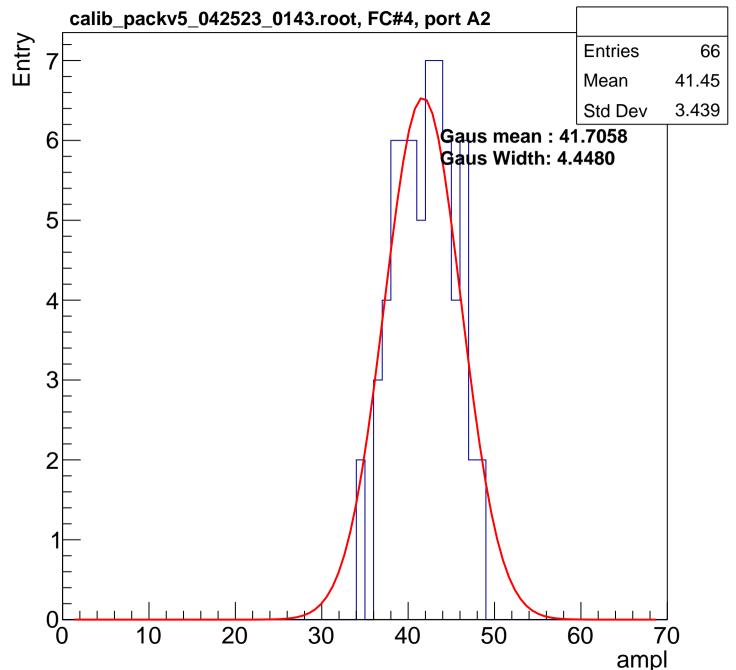
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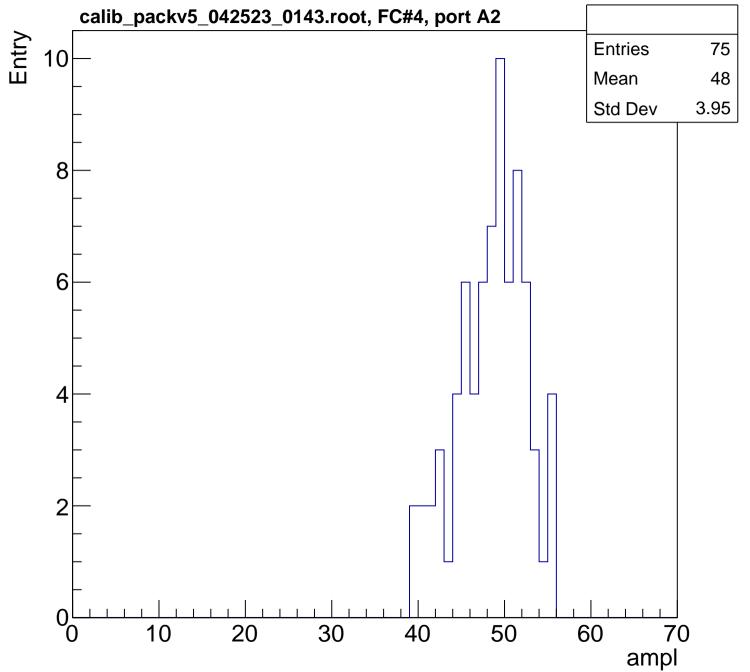
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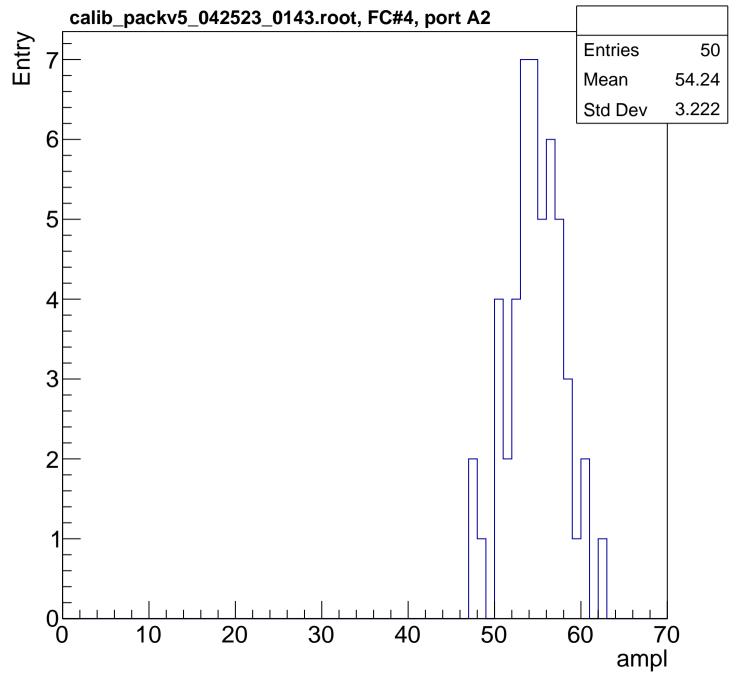


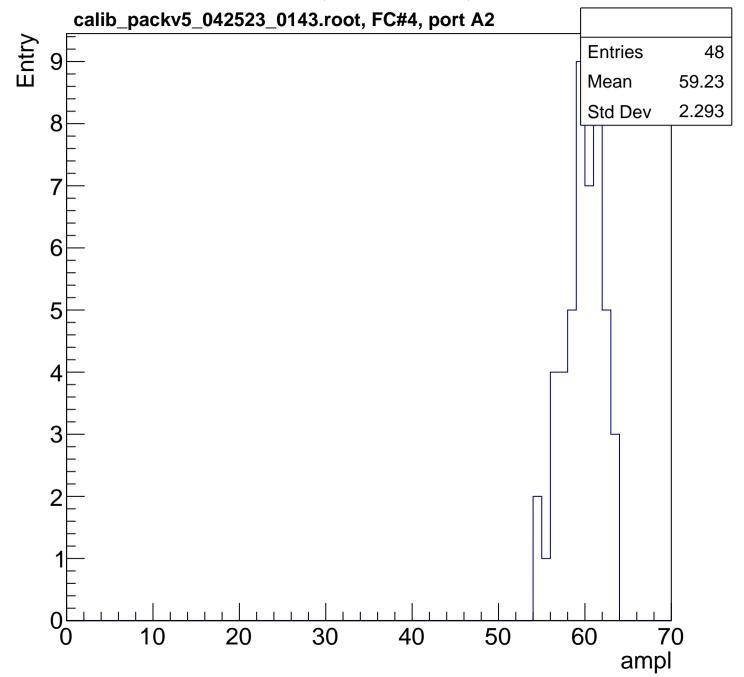


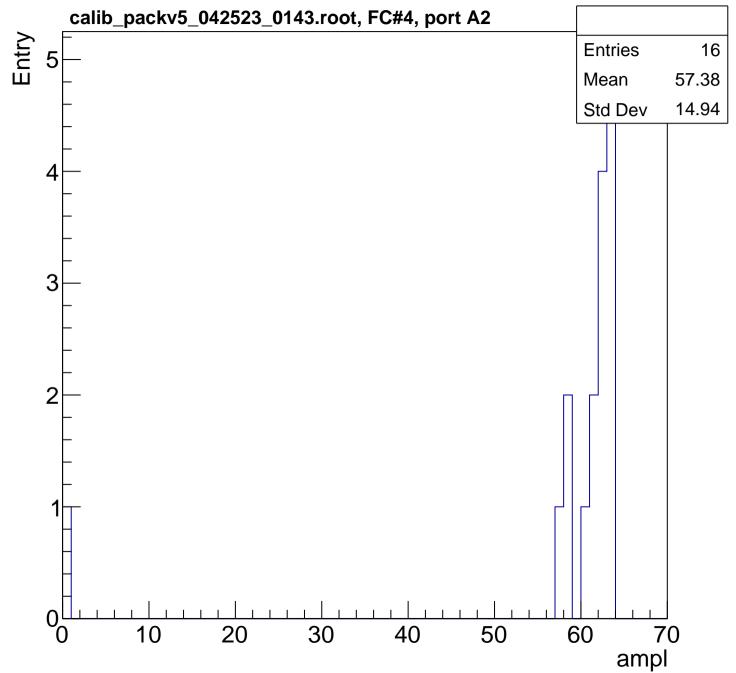


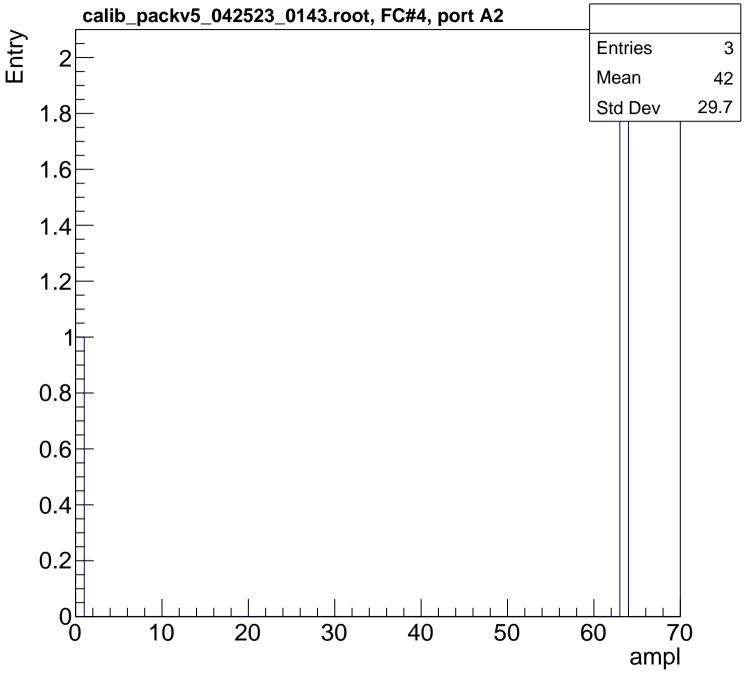


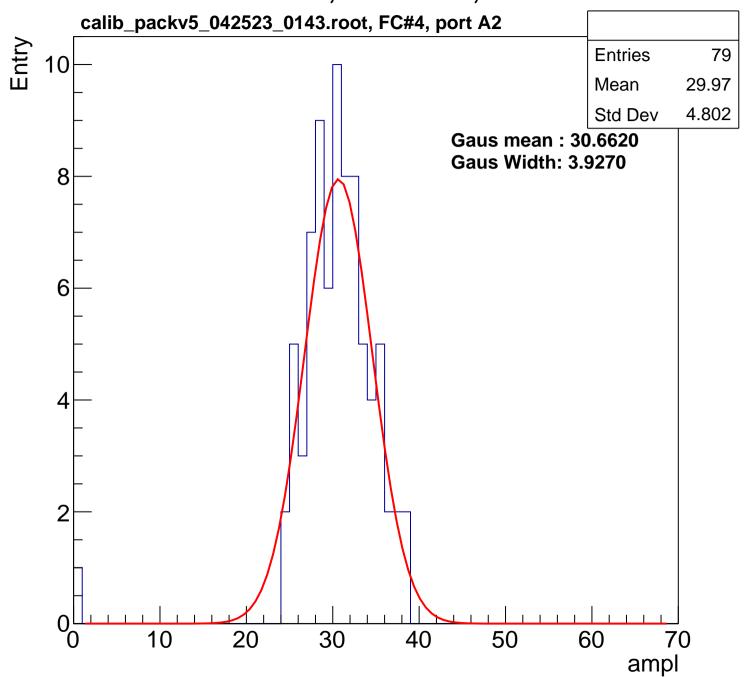


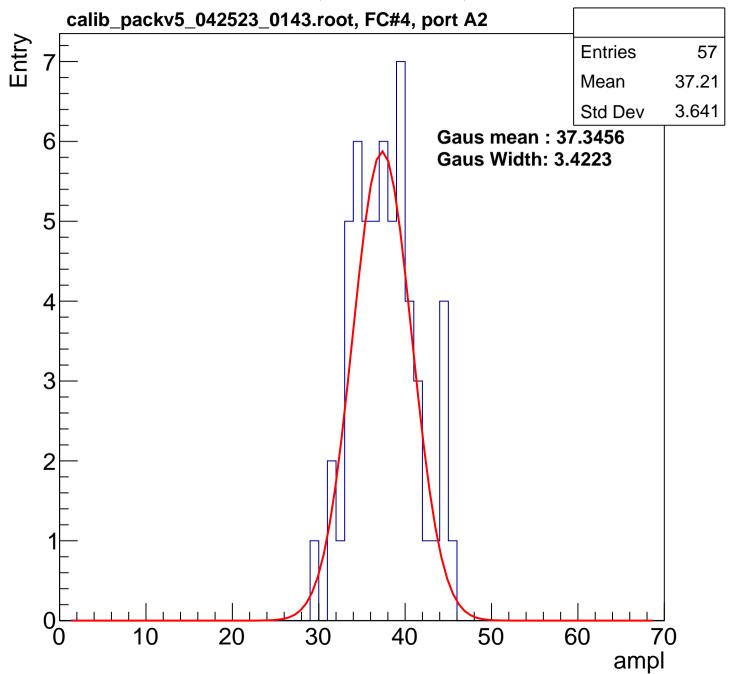


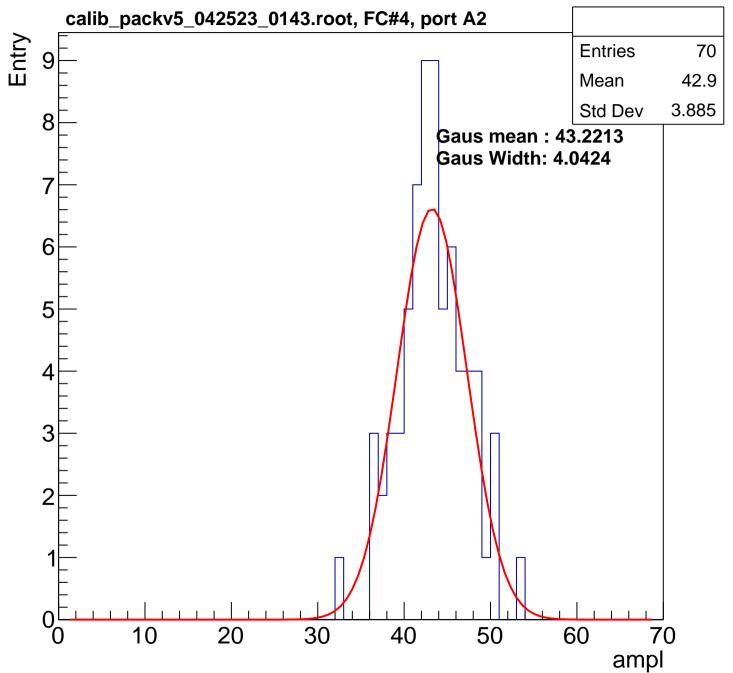


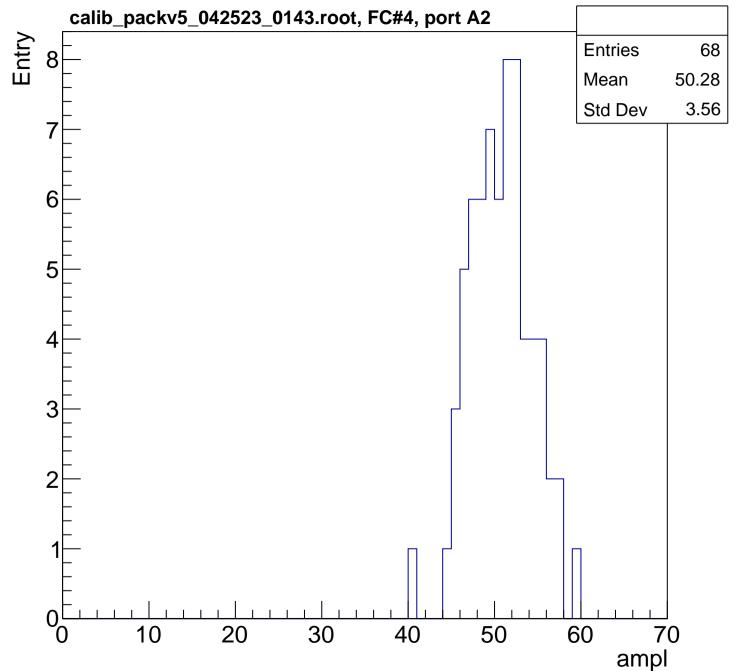


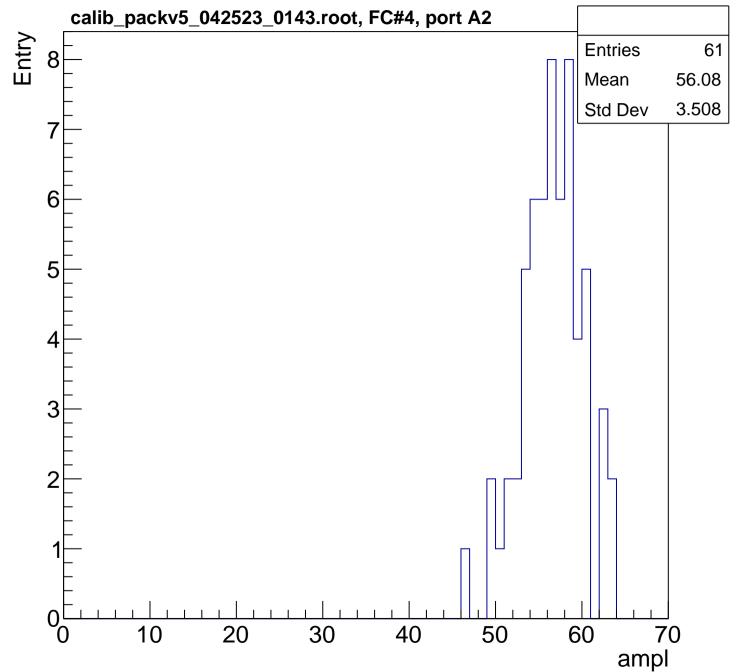


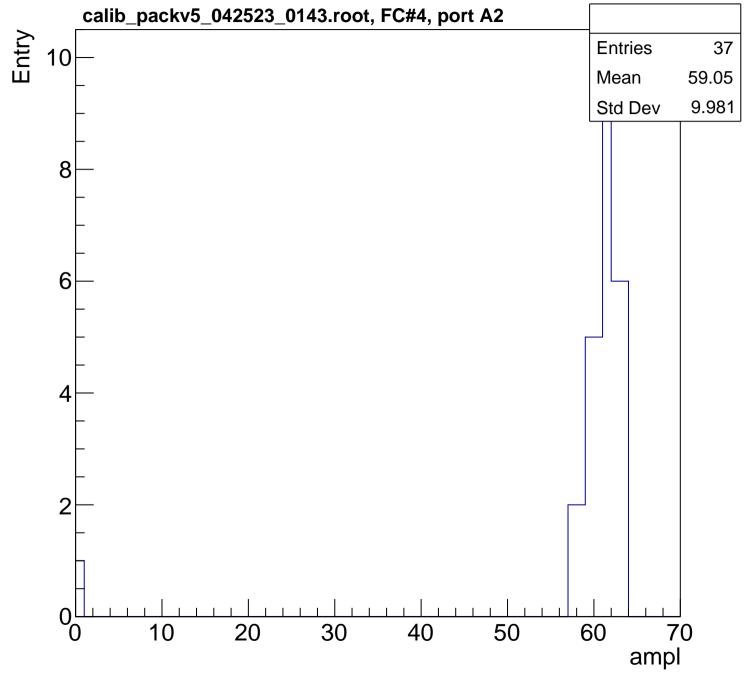






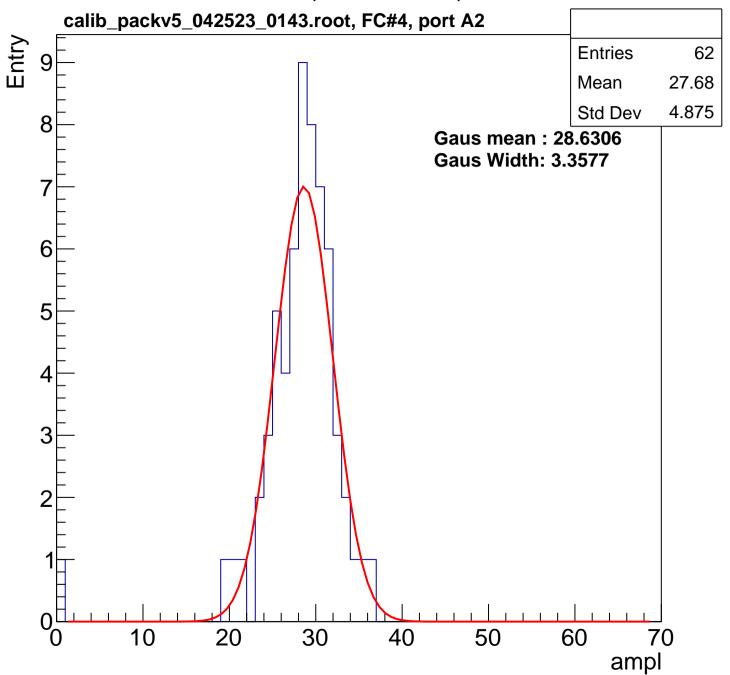


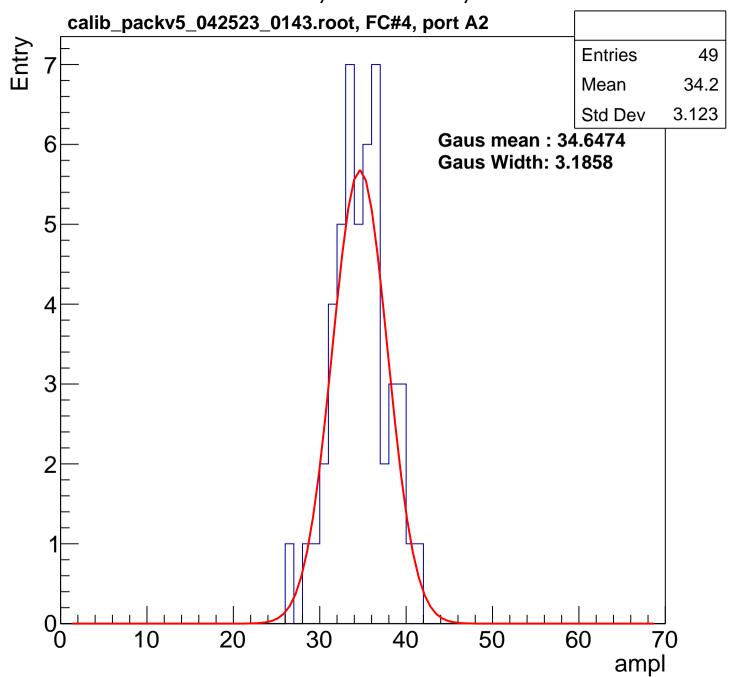


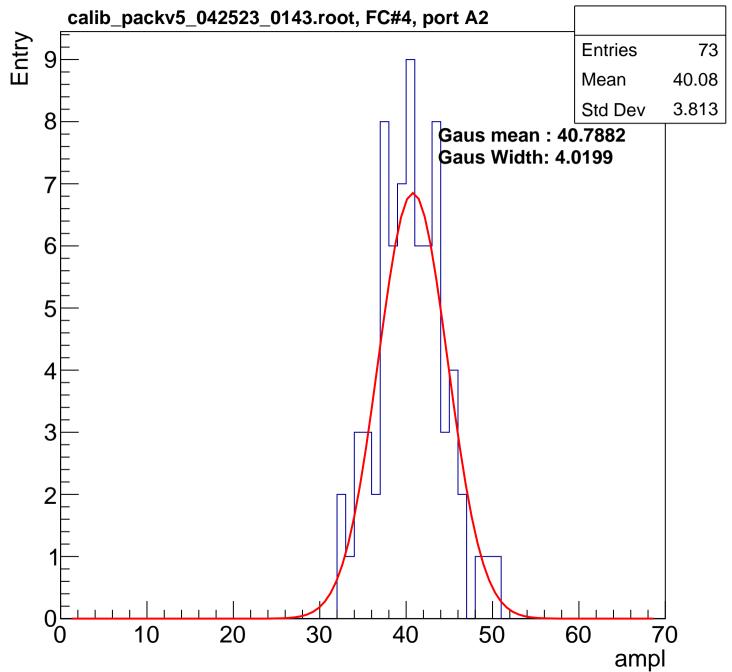


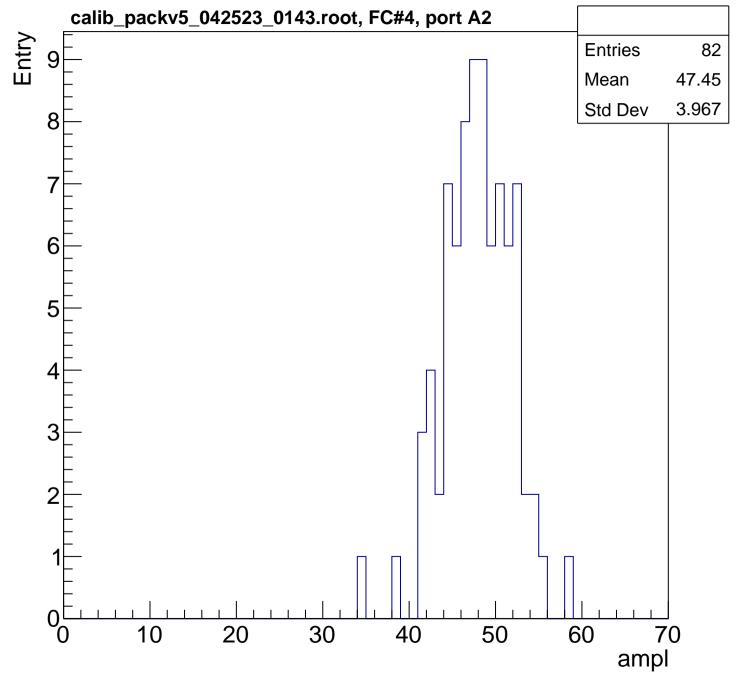


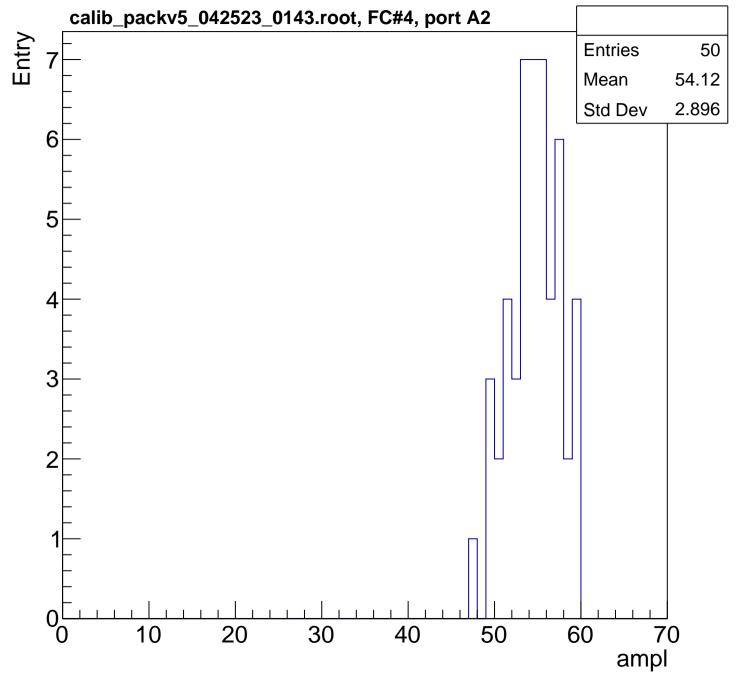


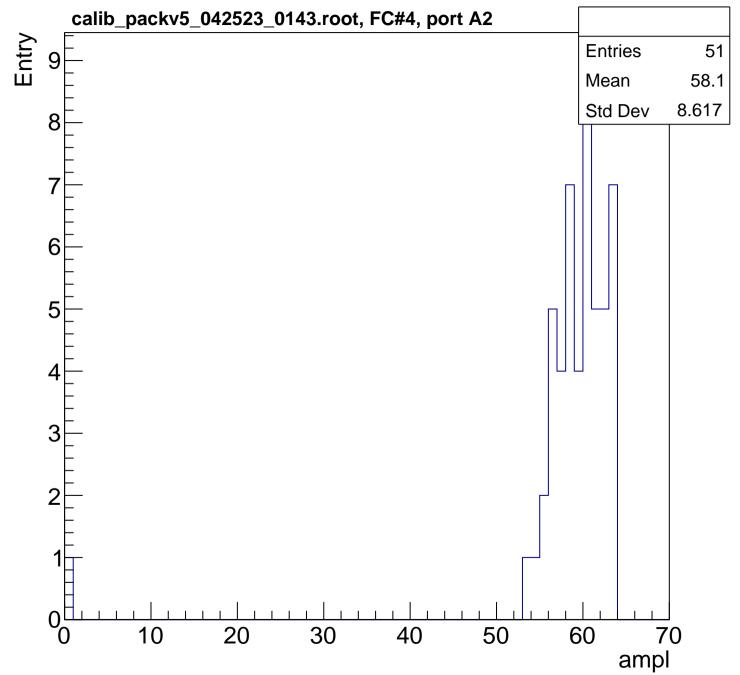


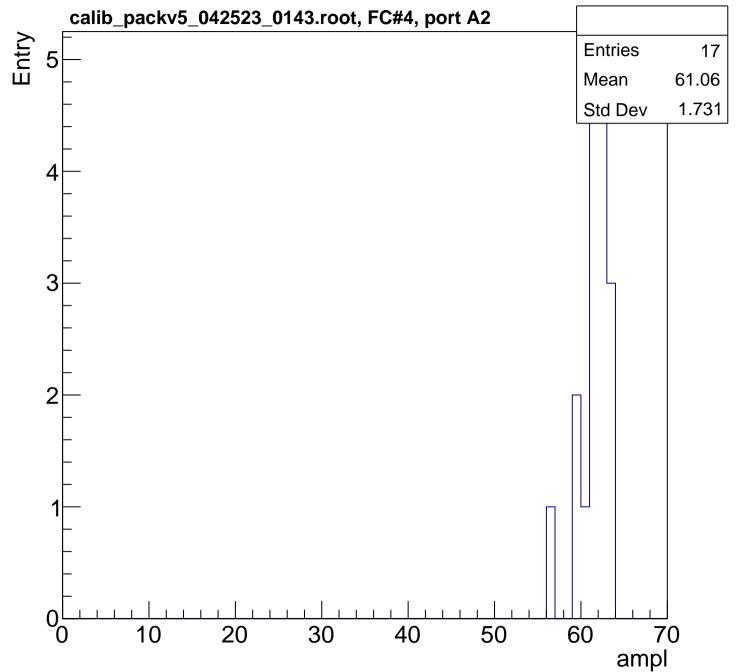




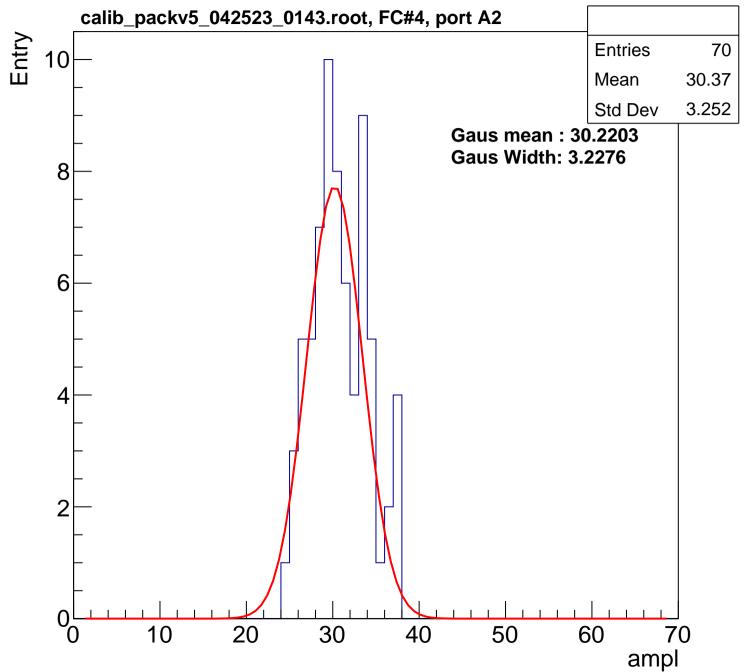


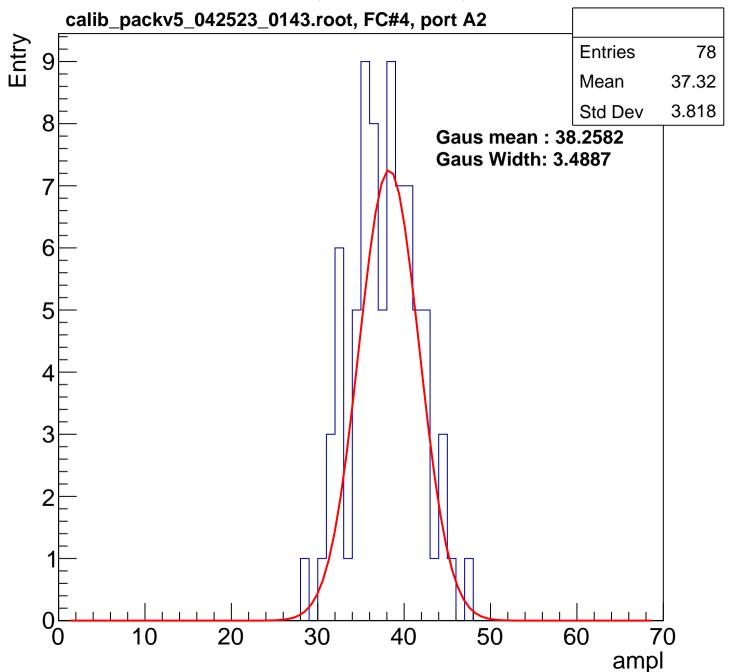


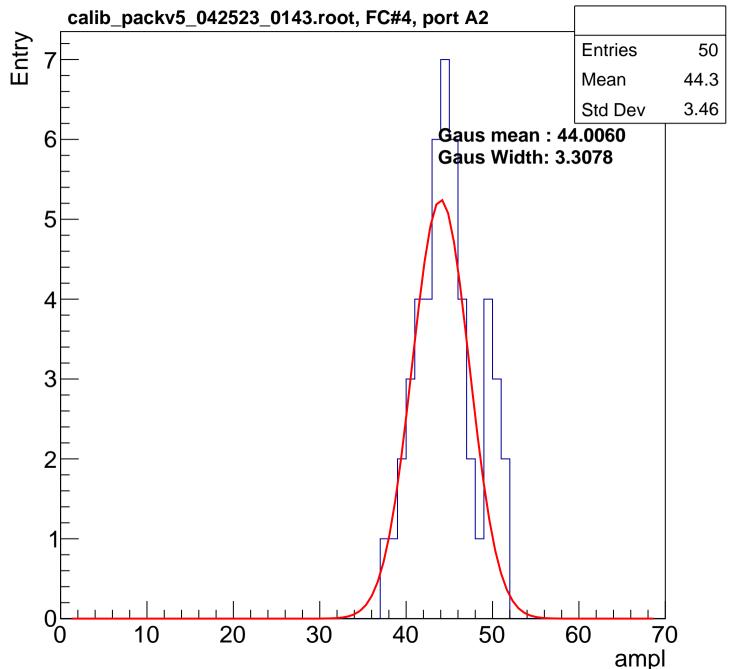


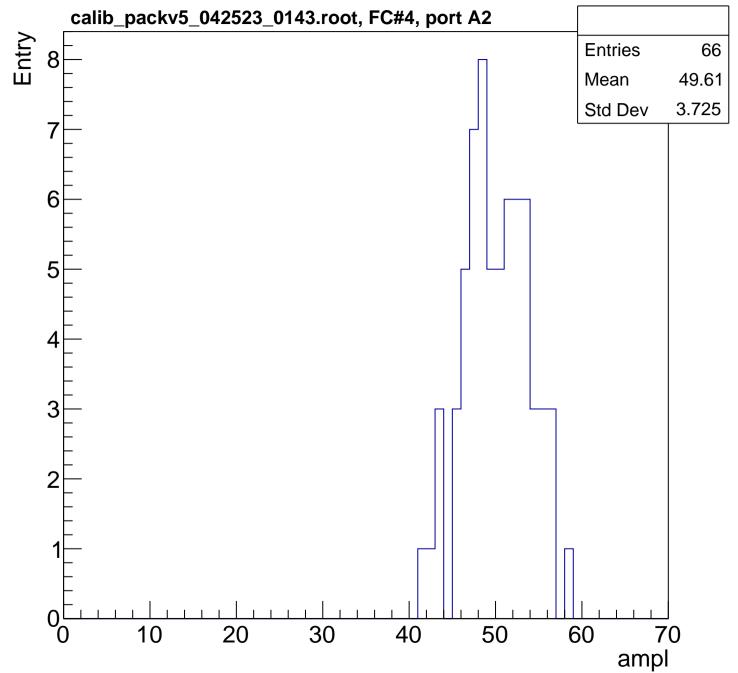


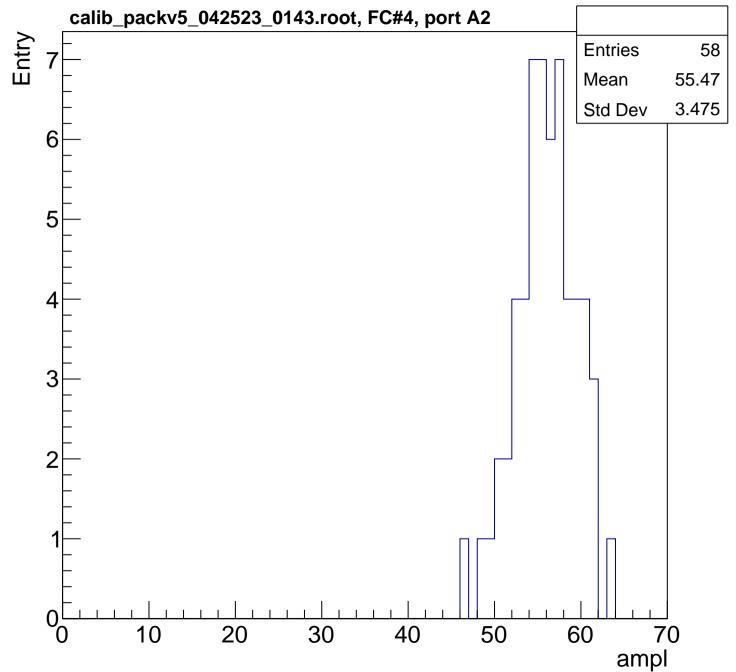
B1L100S, U3-ch18, adc7 calib_packv5_042523_0143.root, FC#4, port A2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

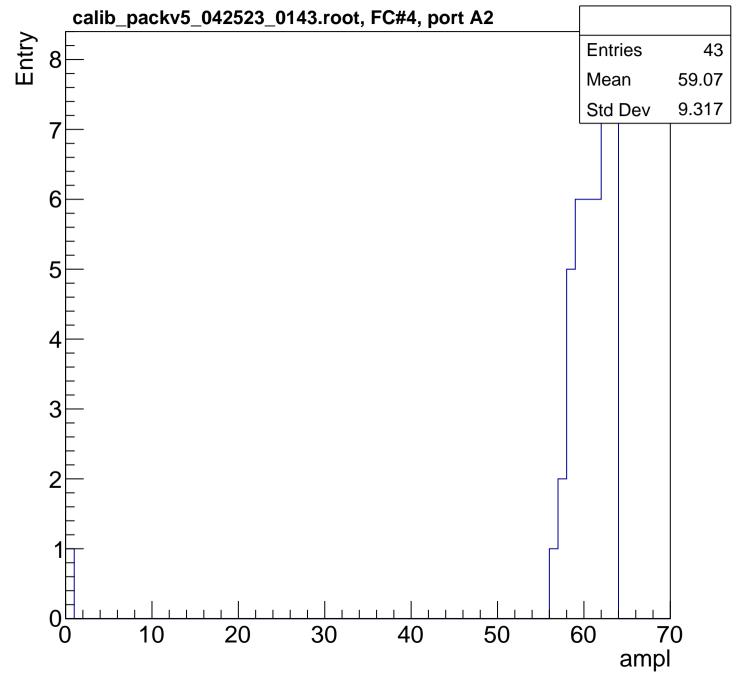


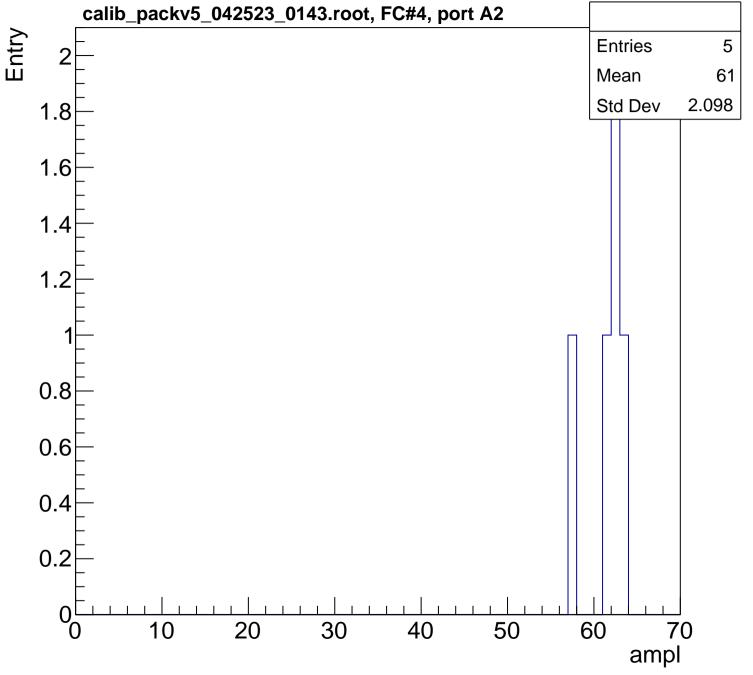




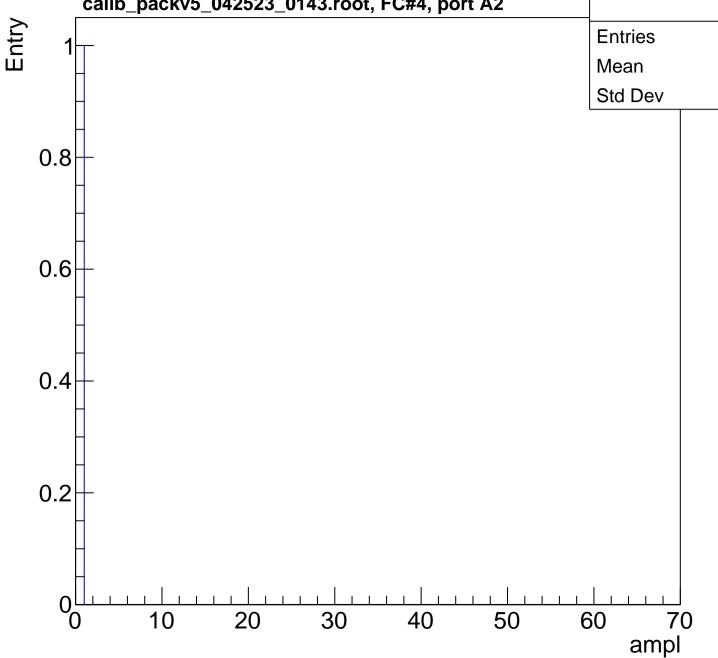


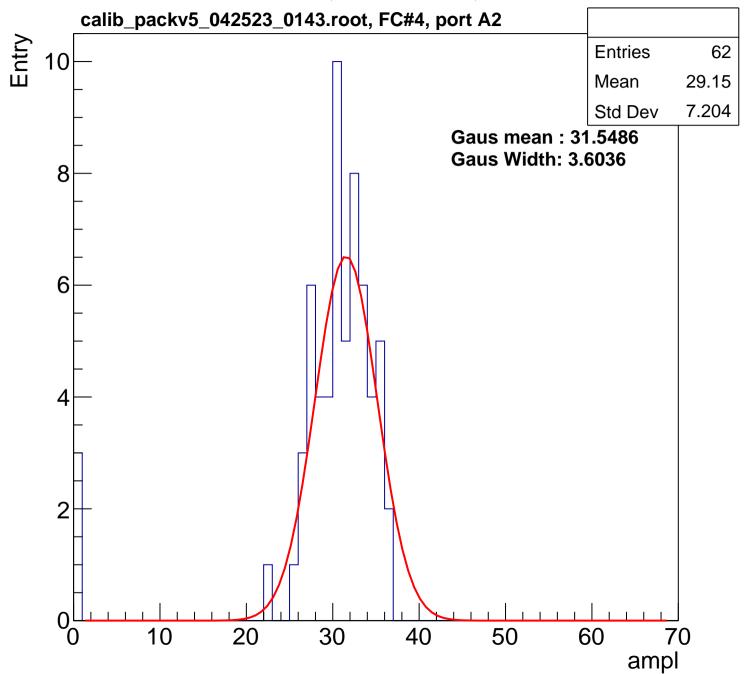


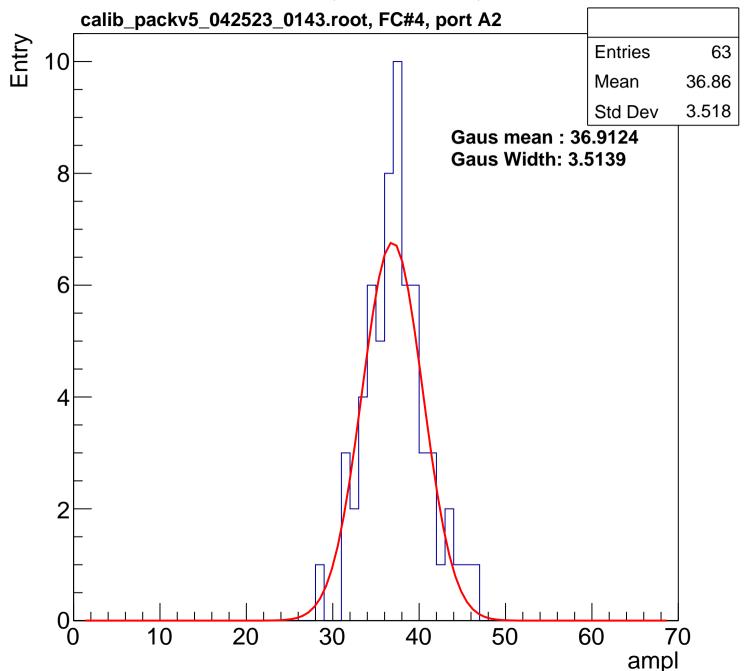


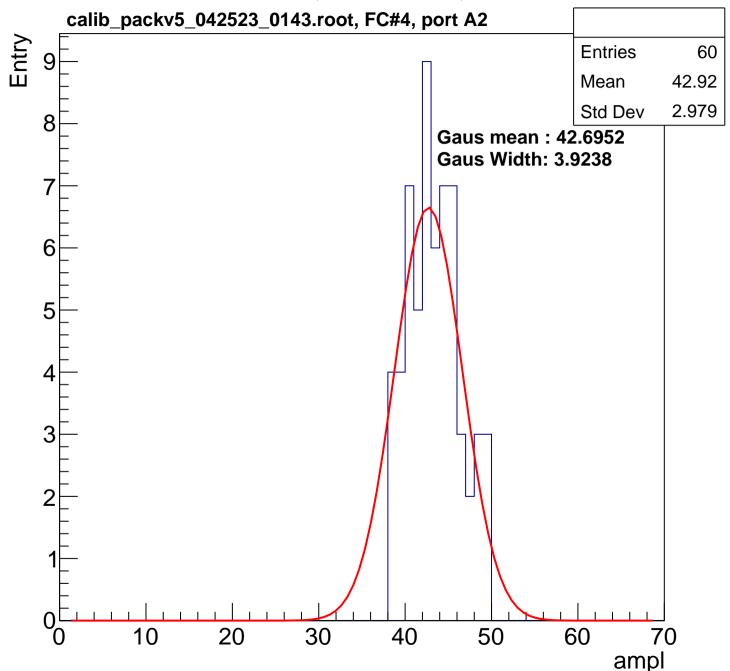


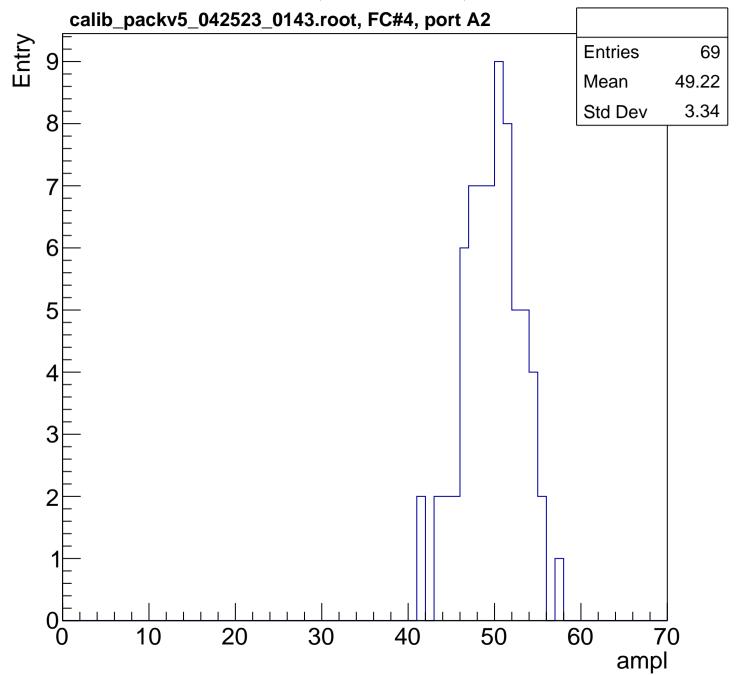
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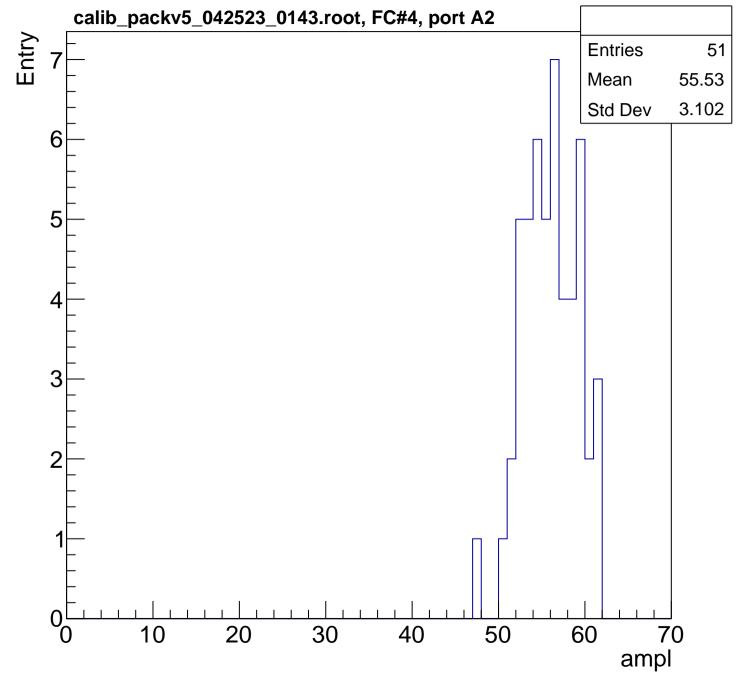


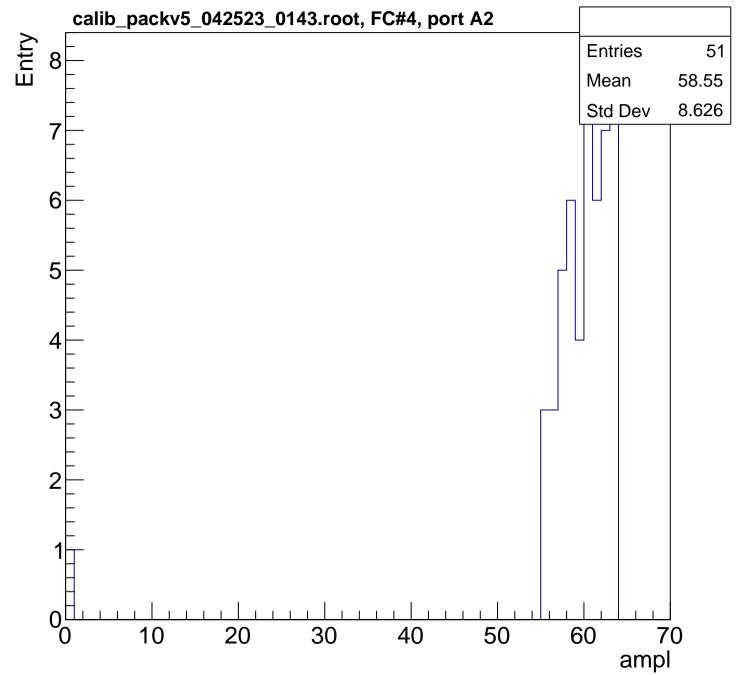


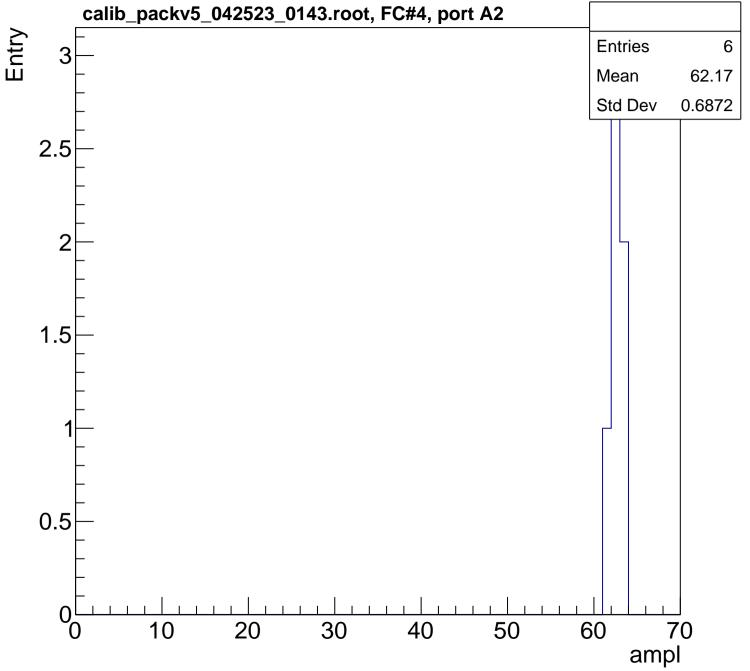




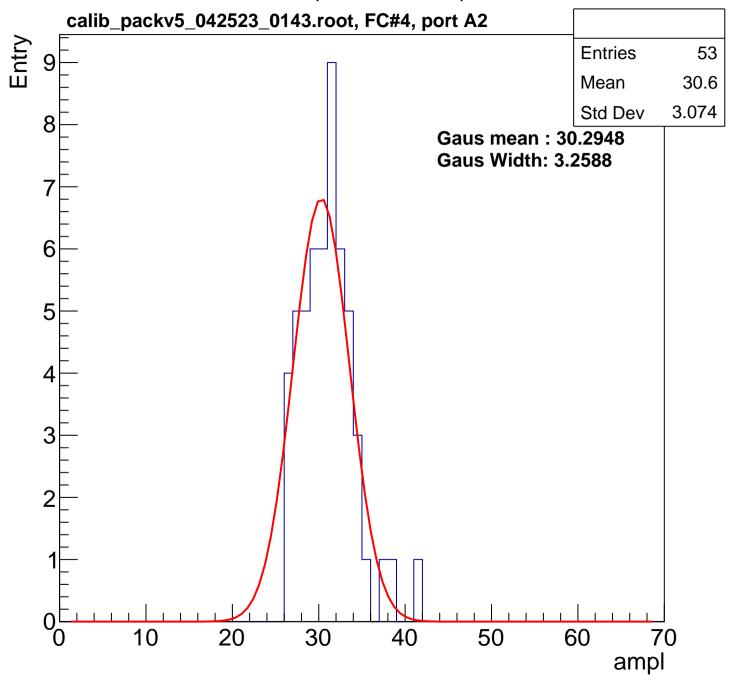


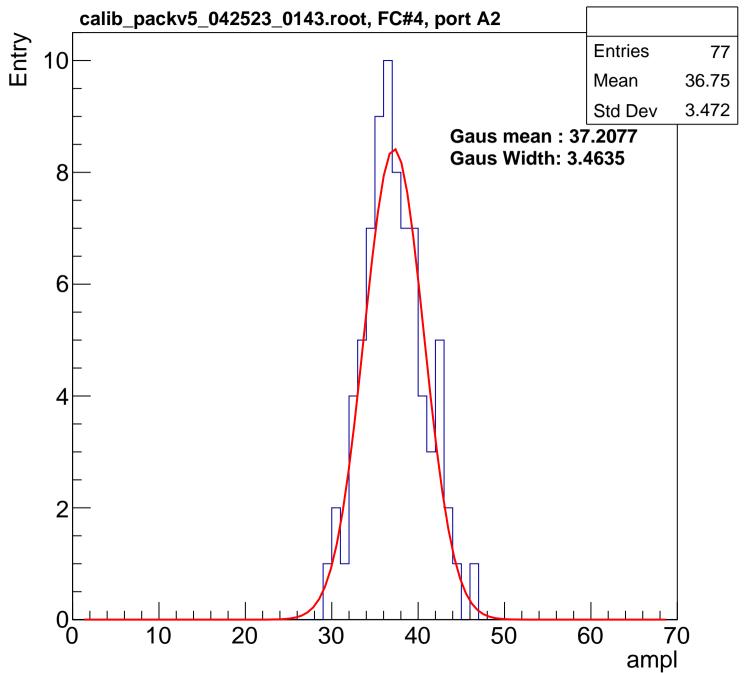


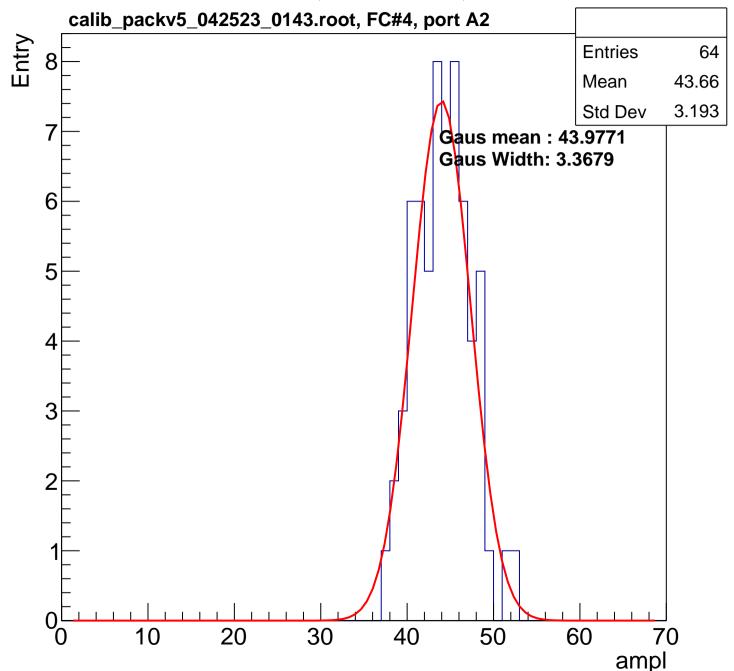


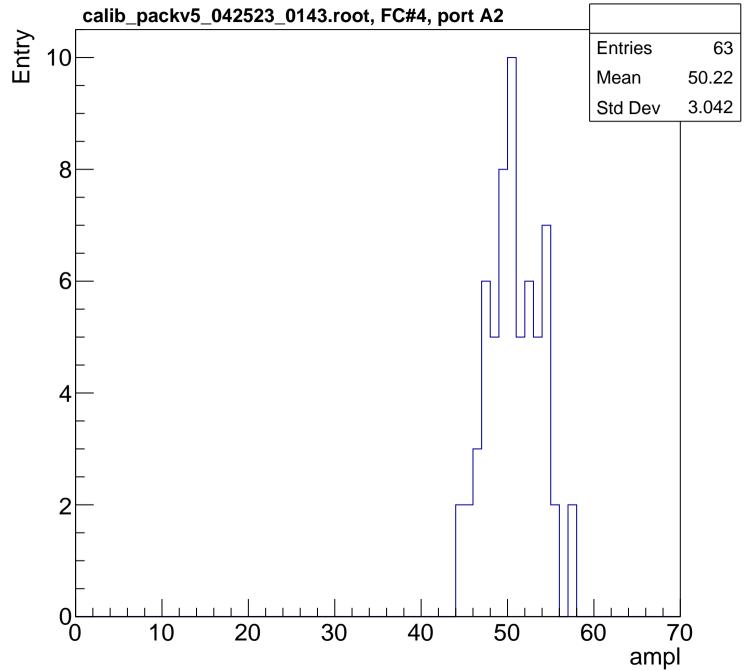


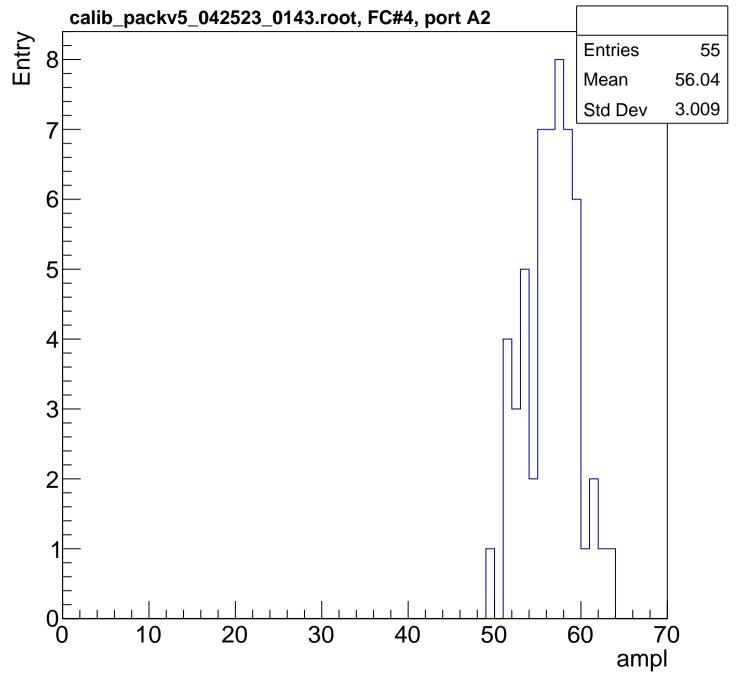


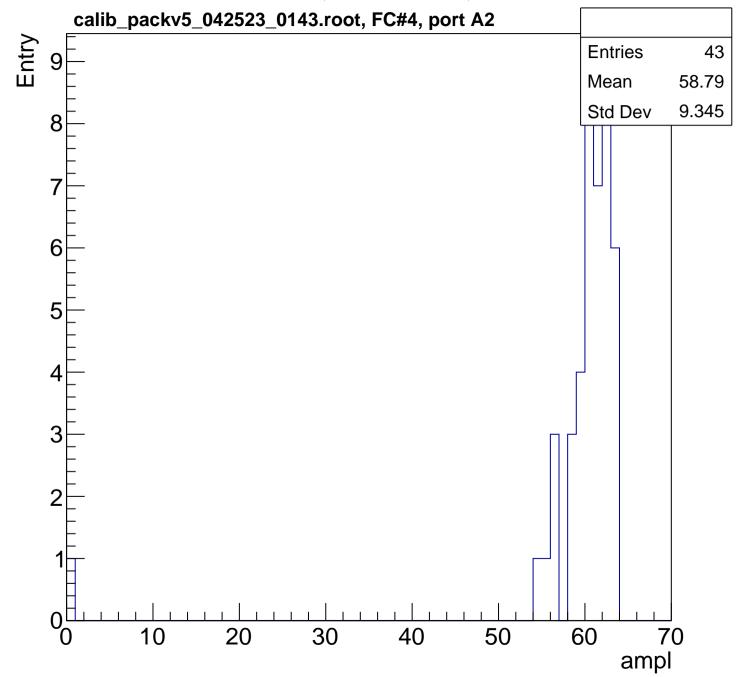


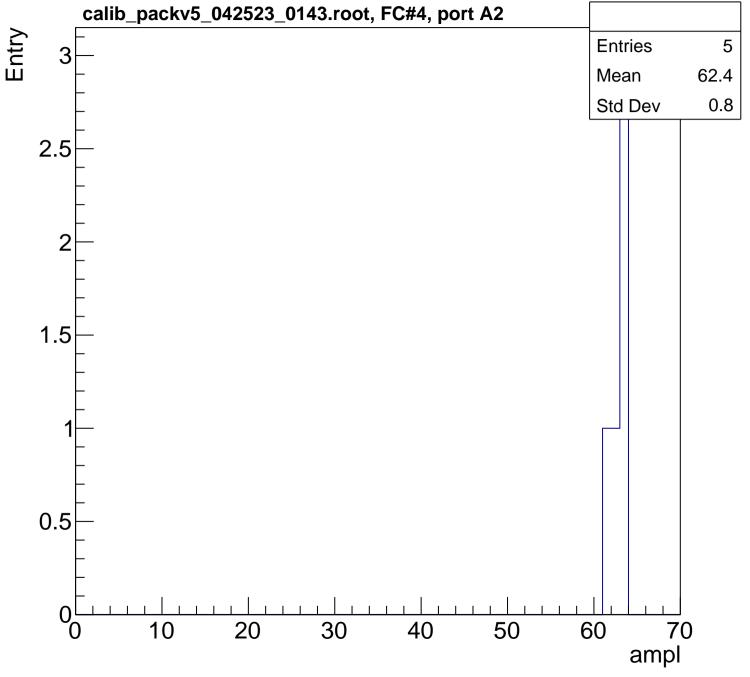


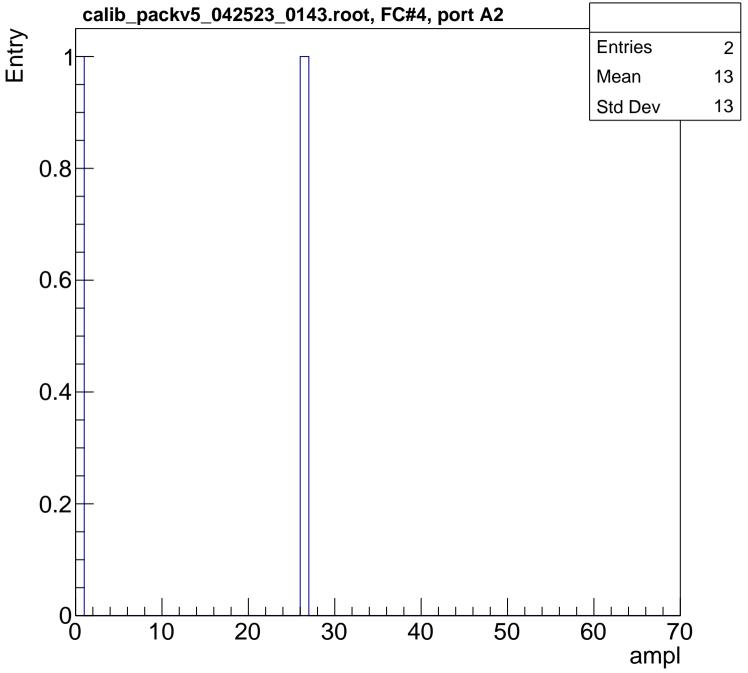


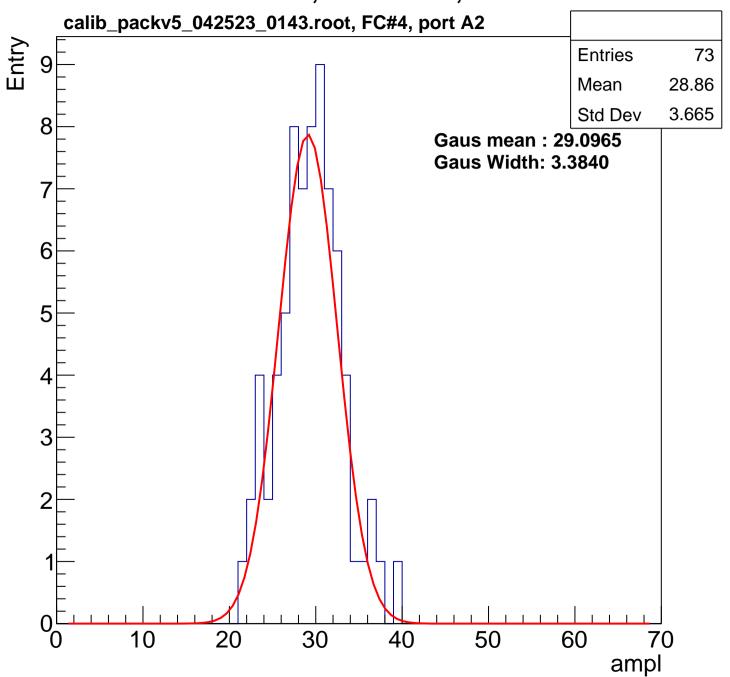


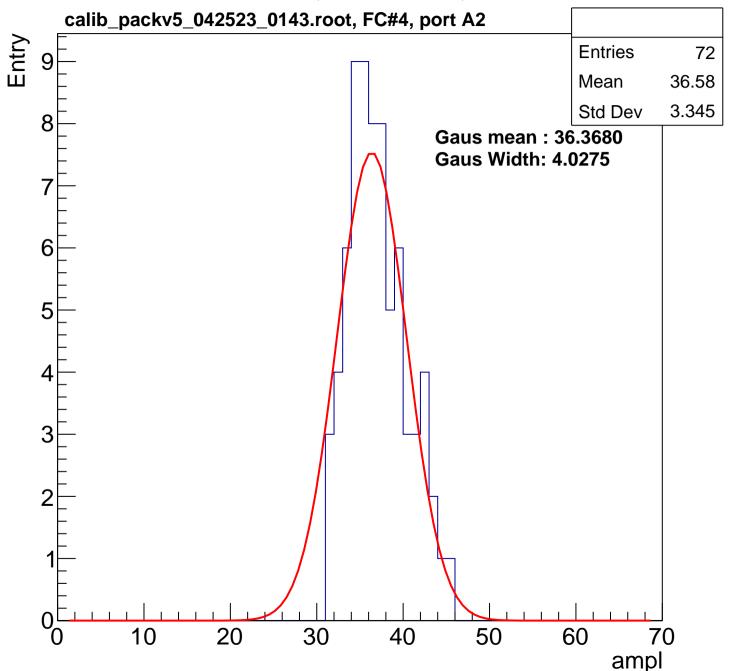


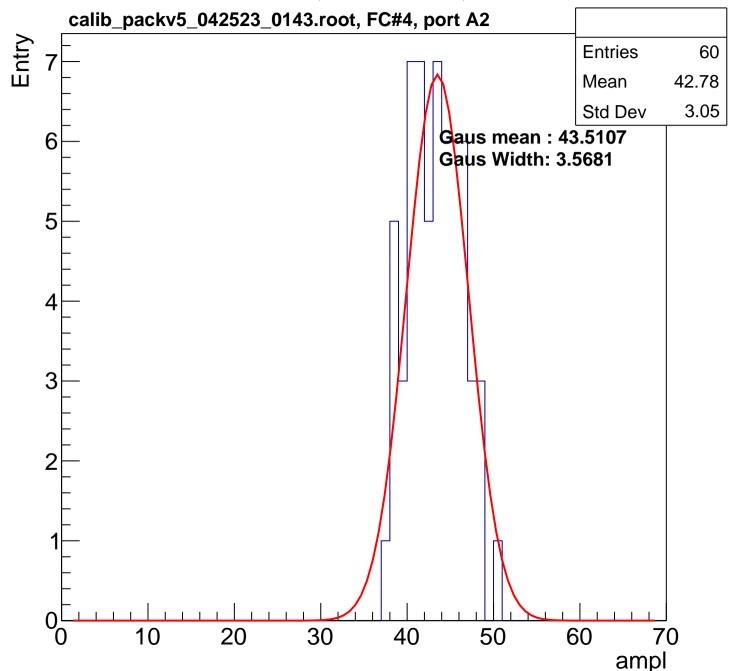


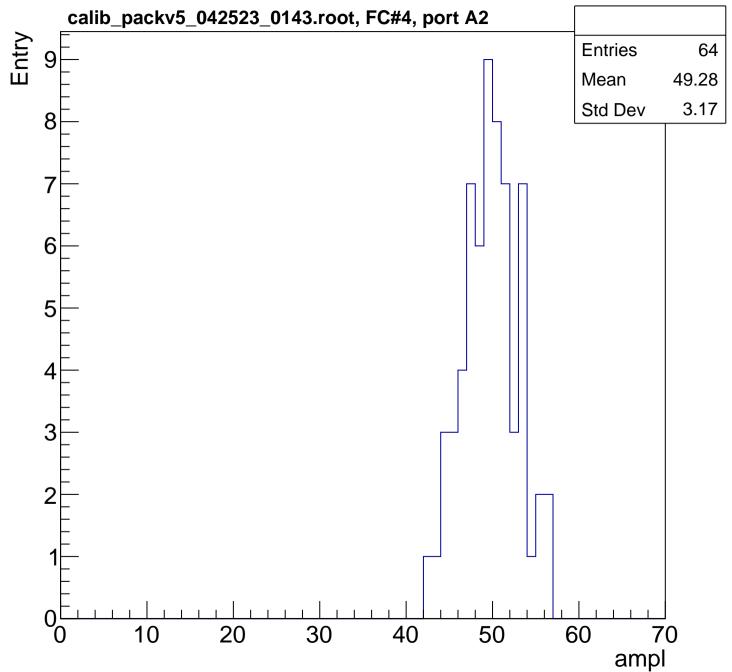


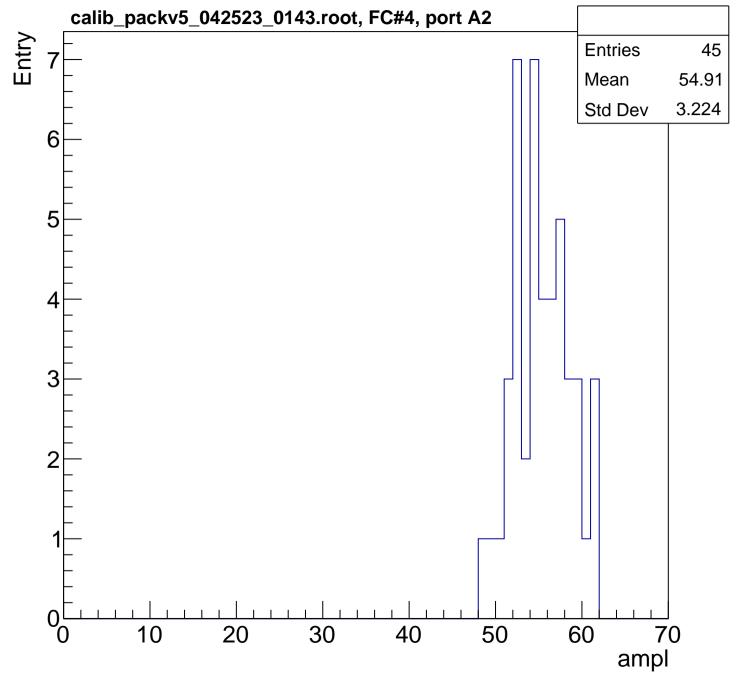


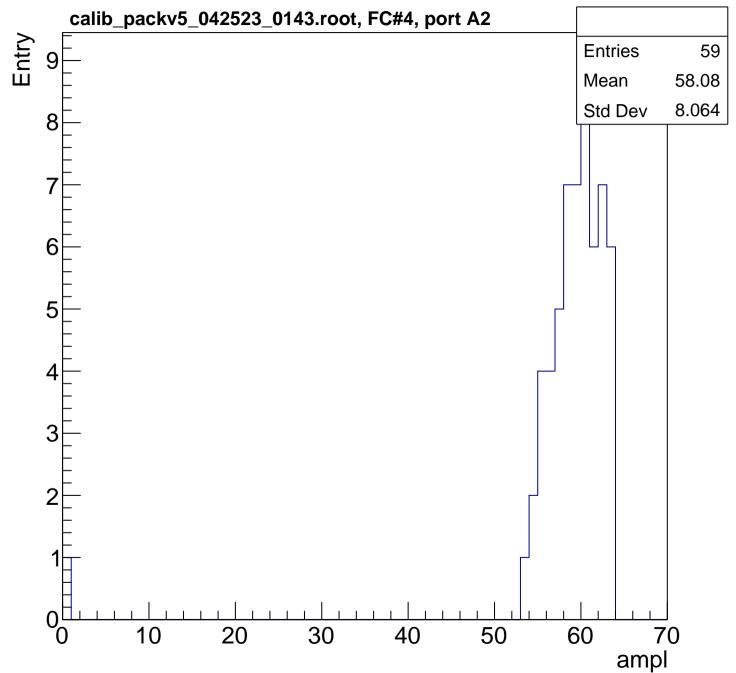


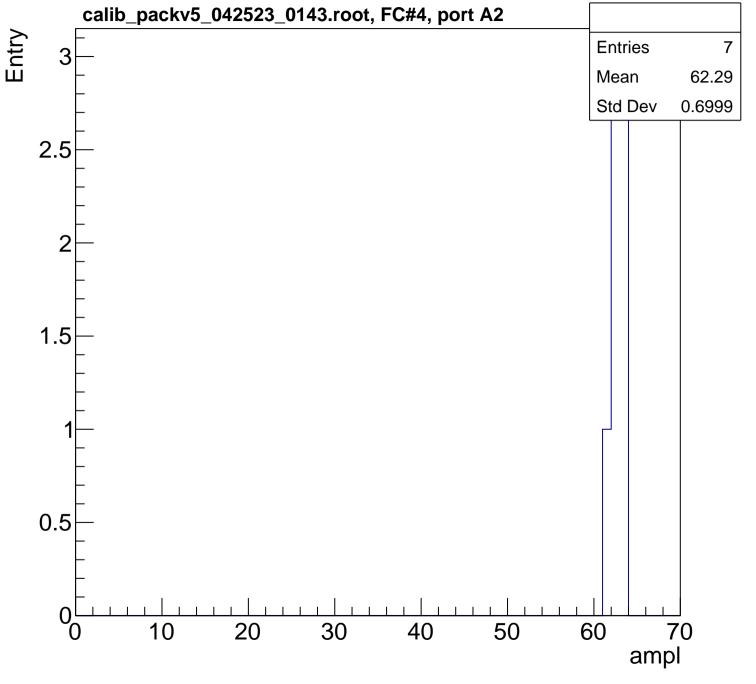


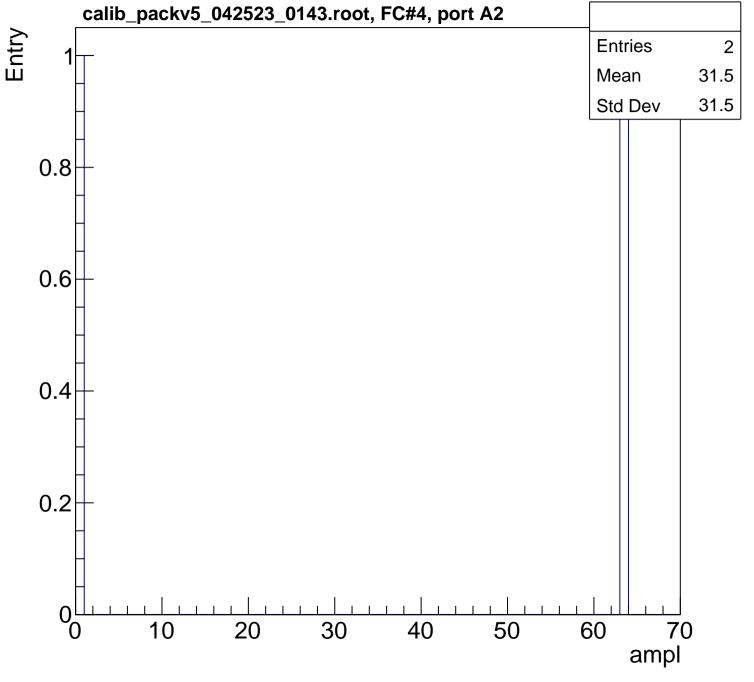


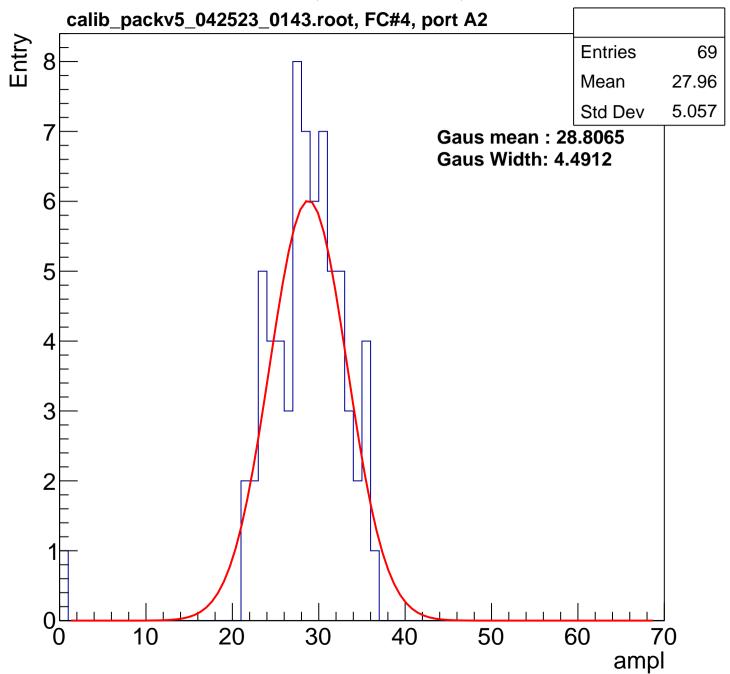


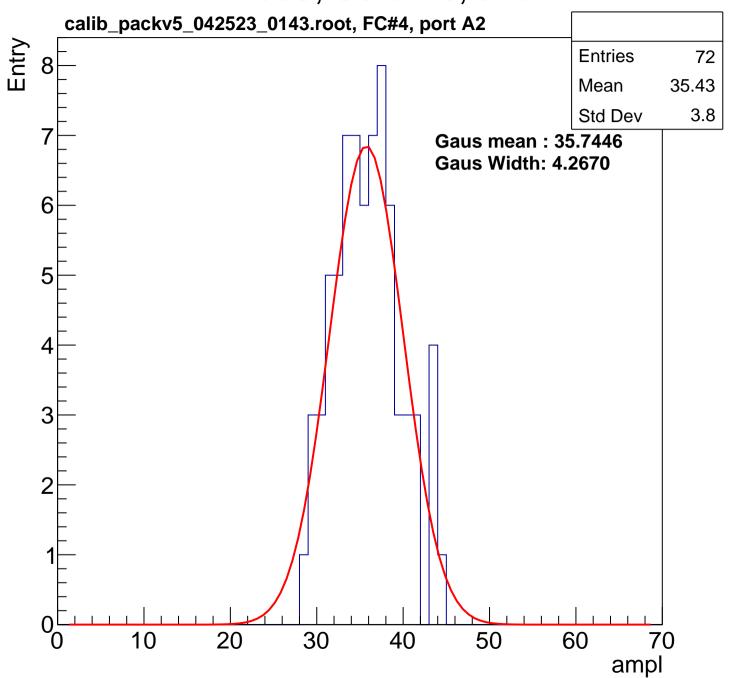


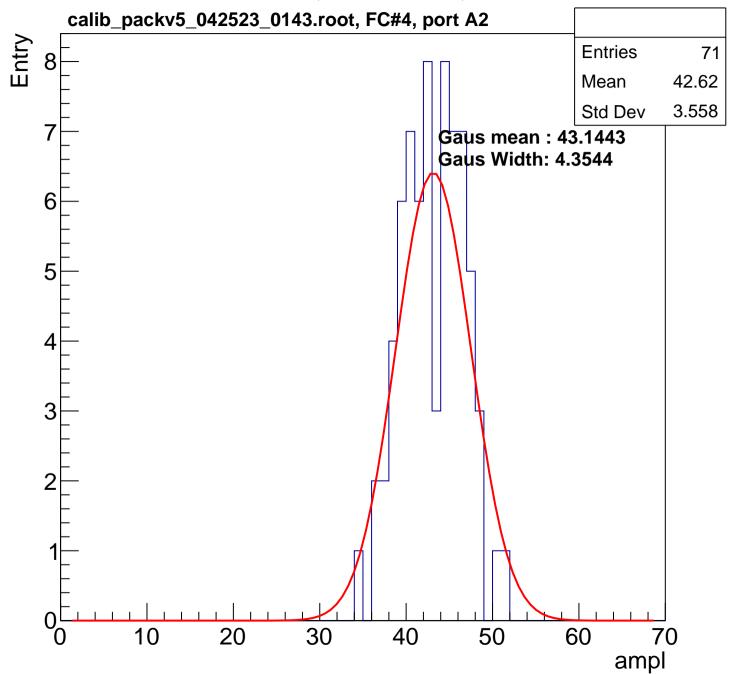


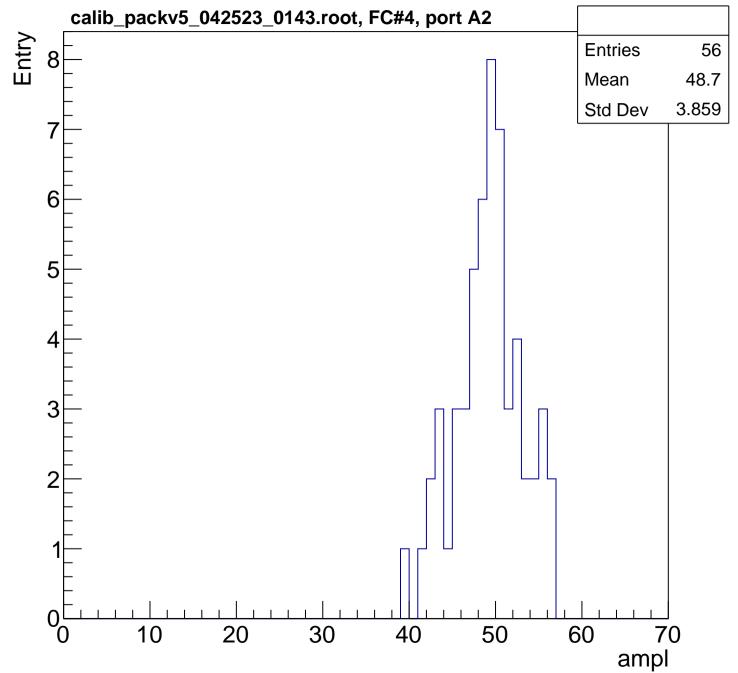


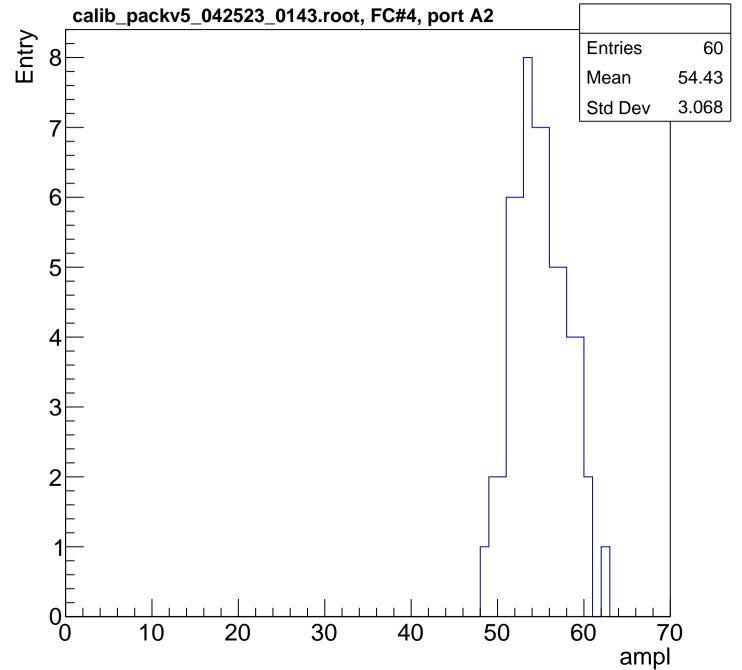


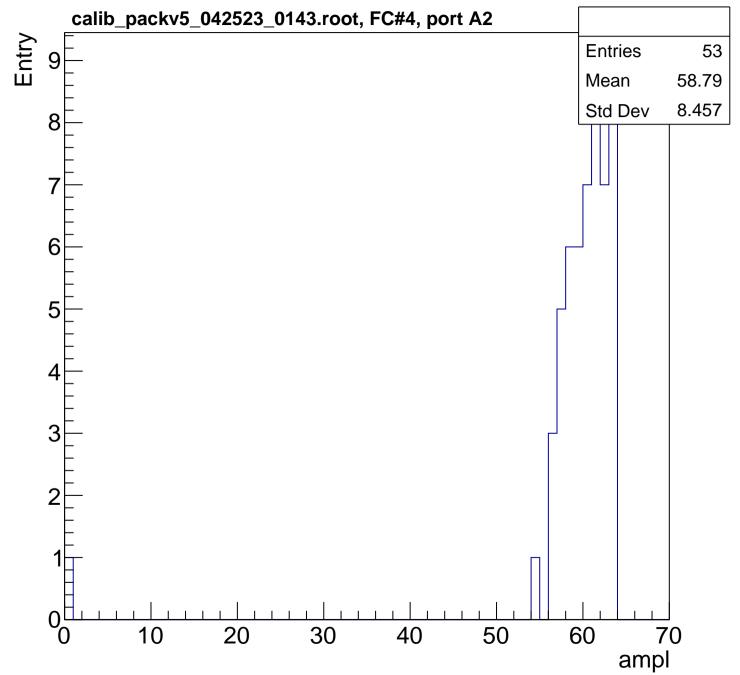


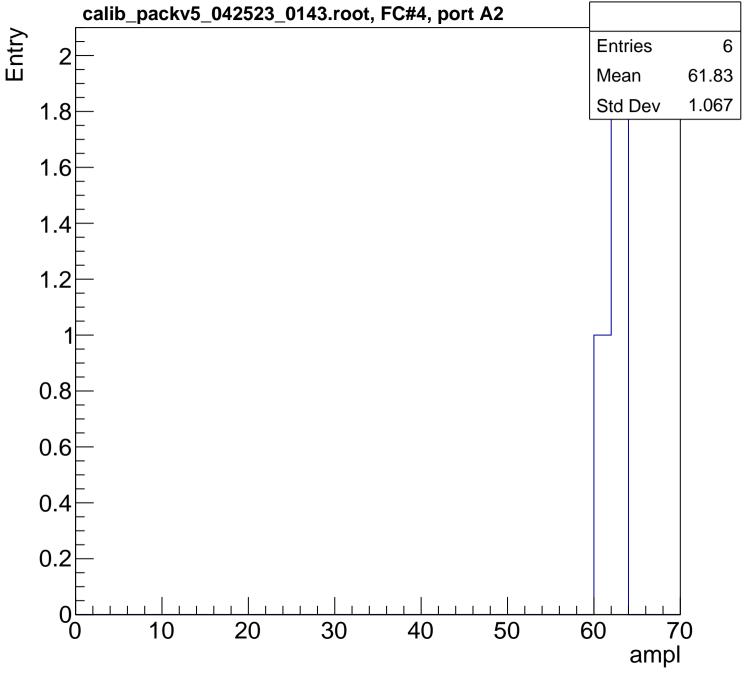


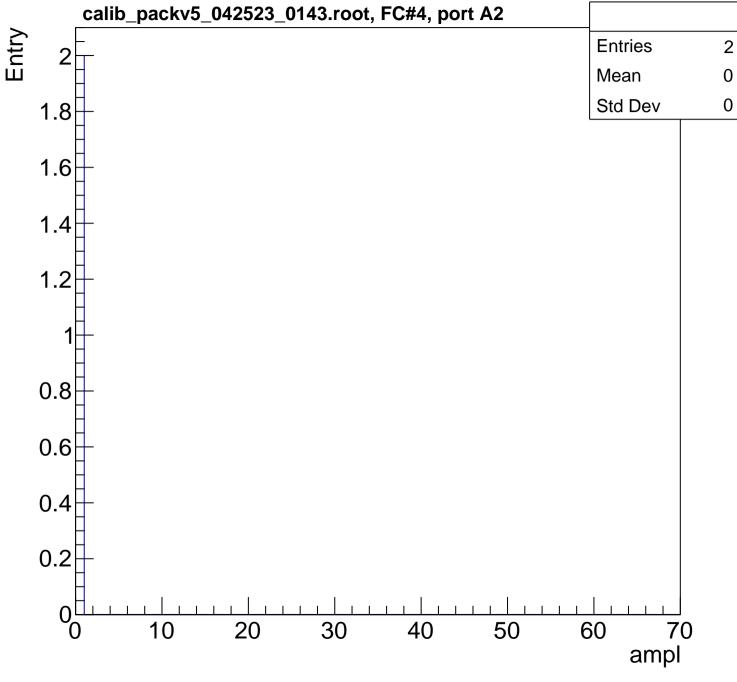


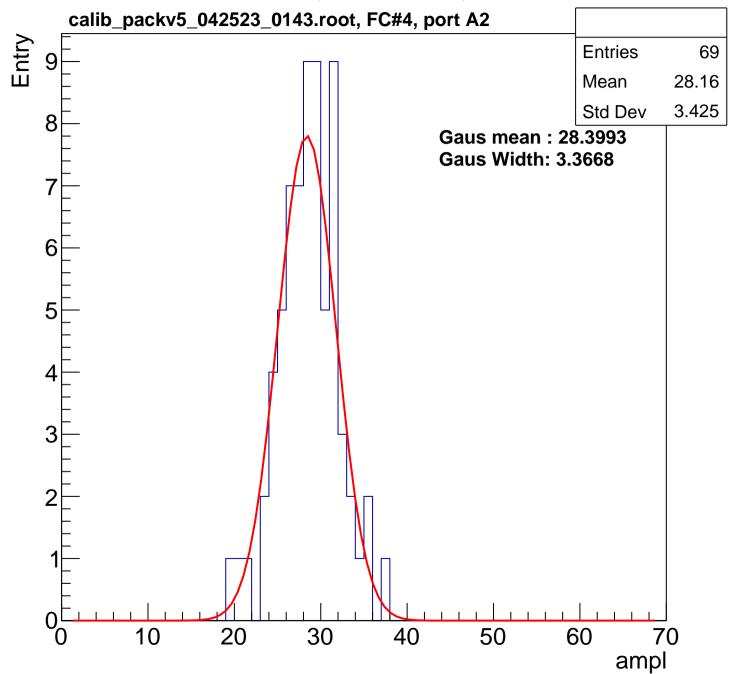


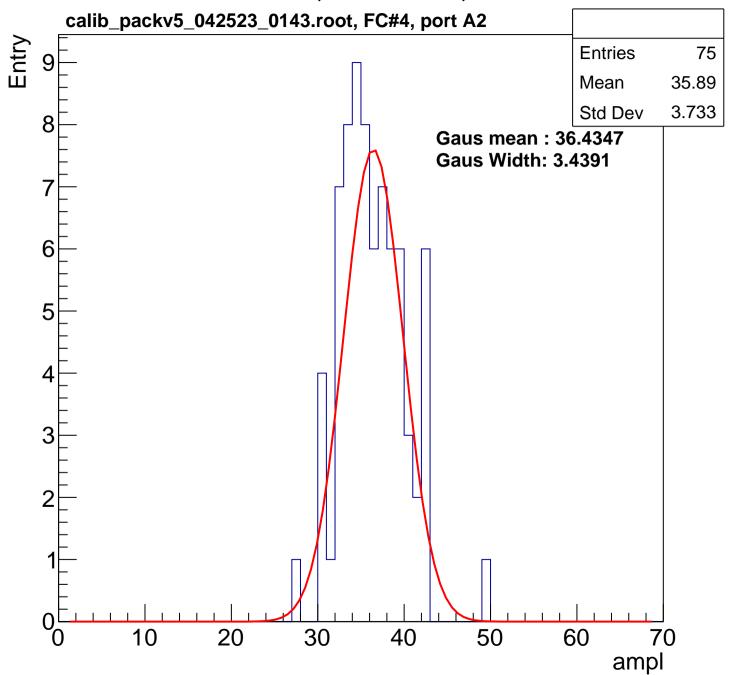


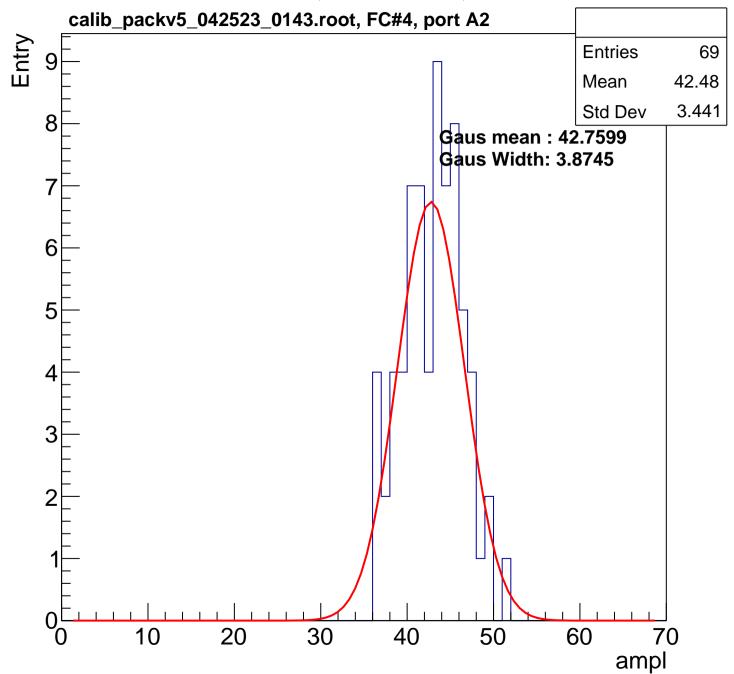


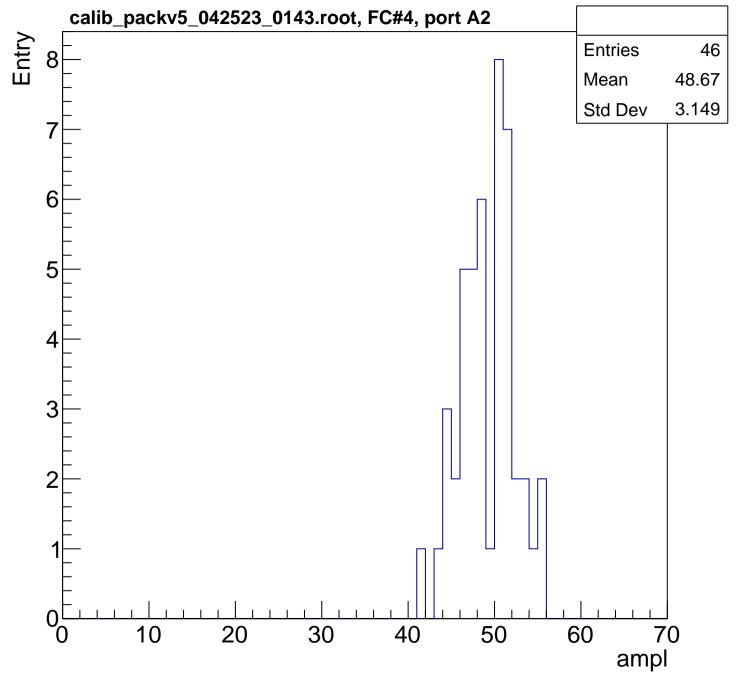


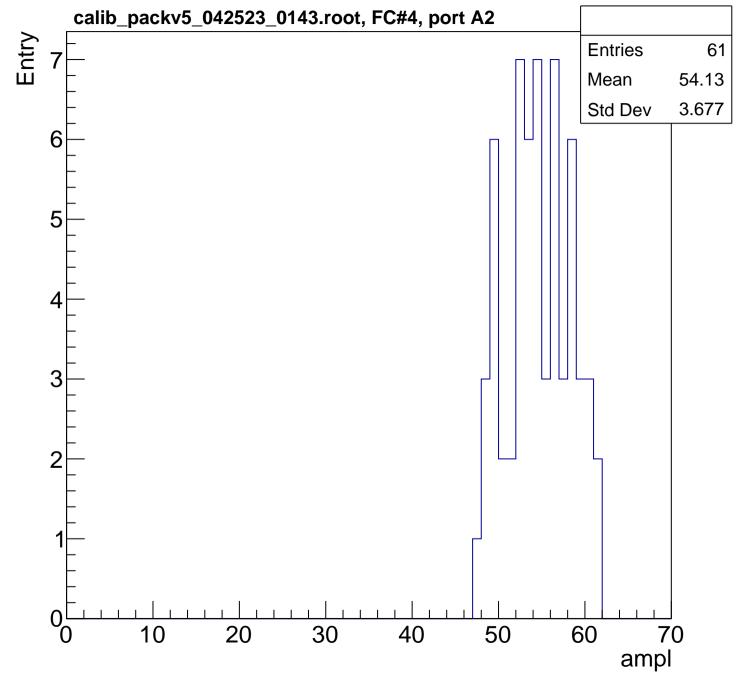


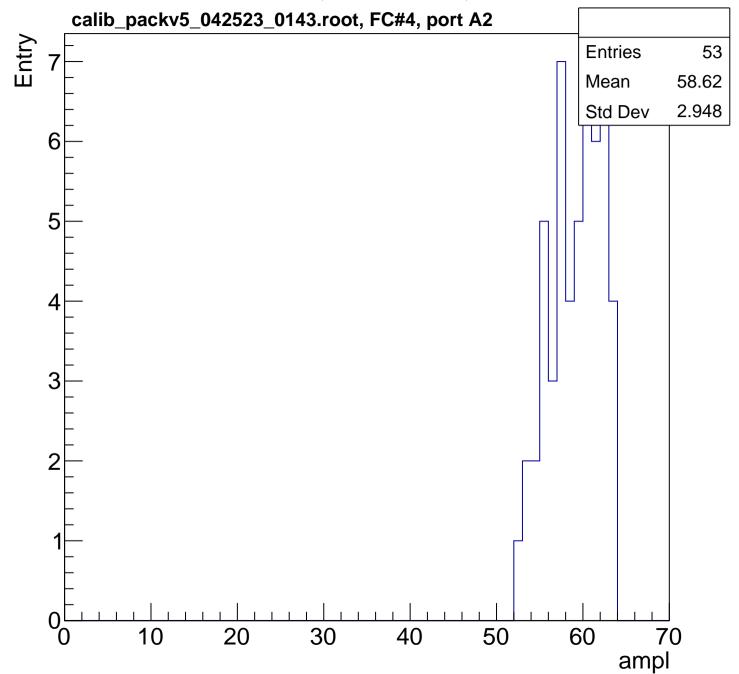


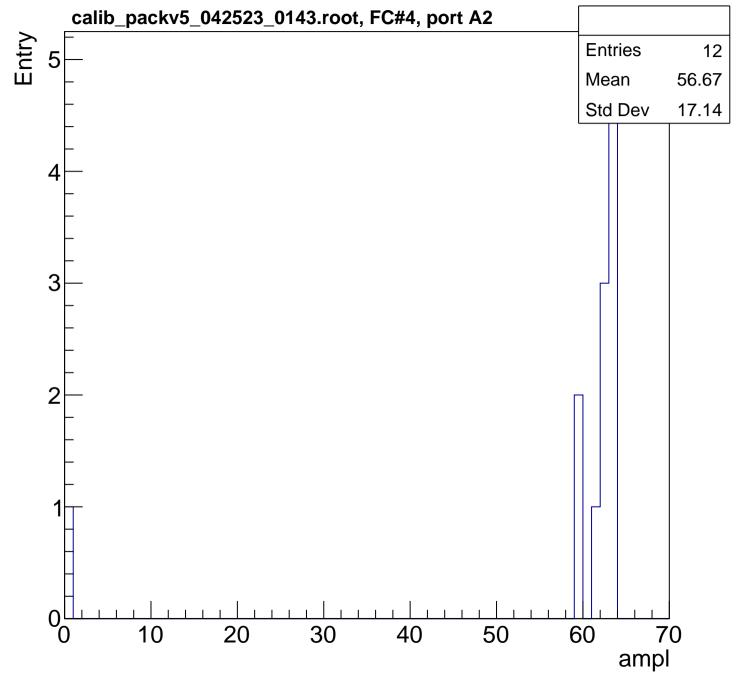


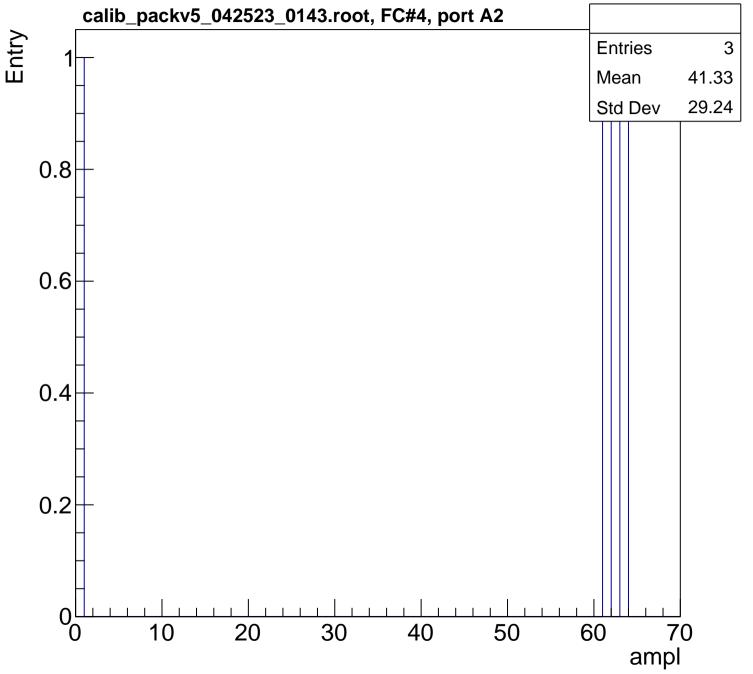


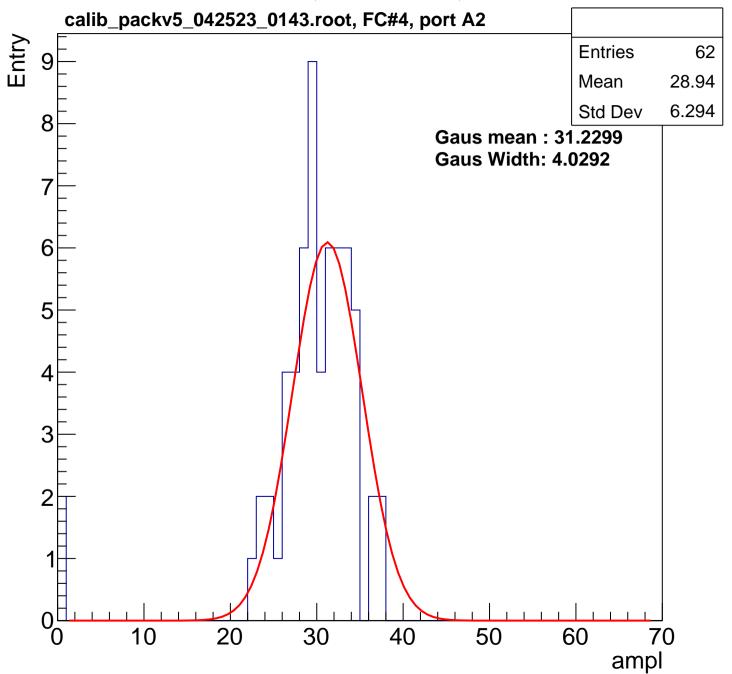


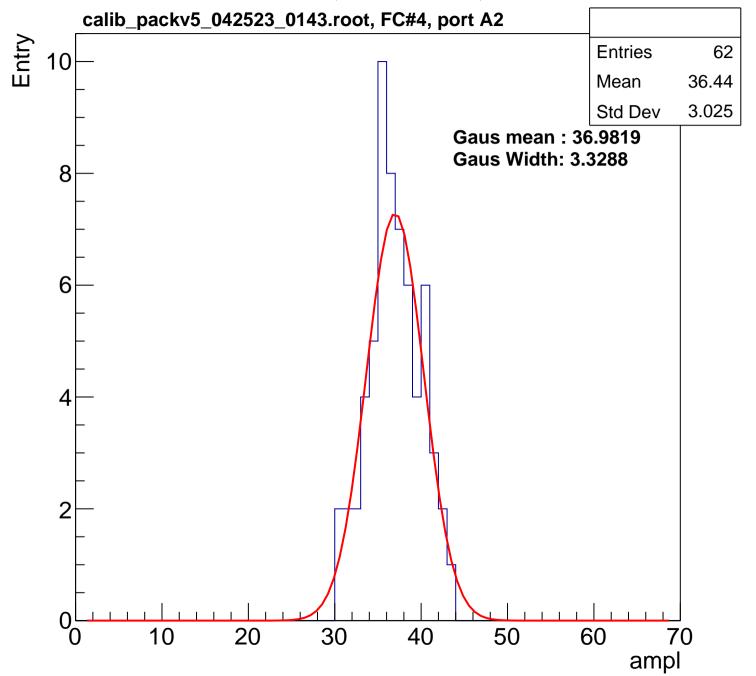


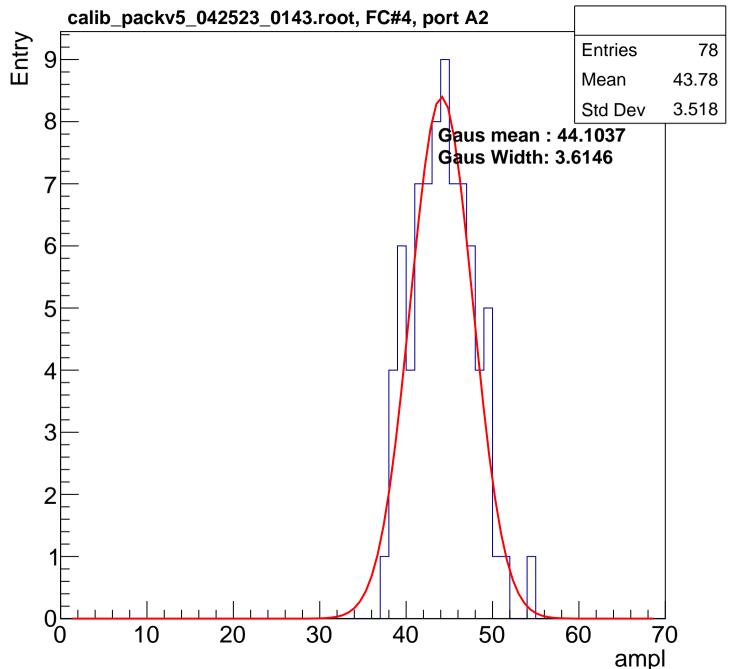


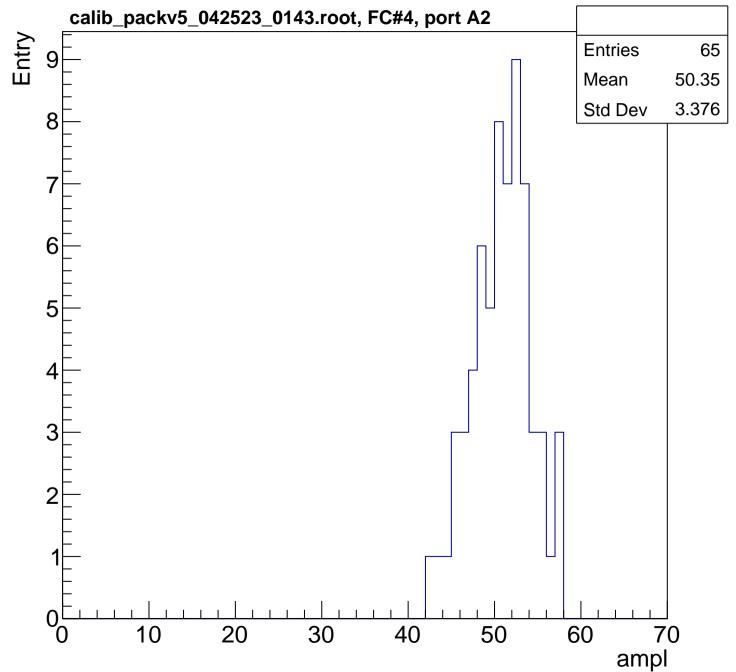


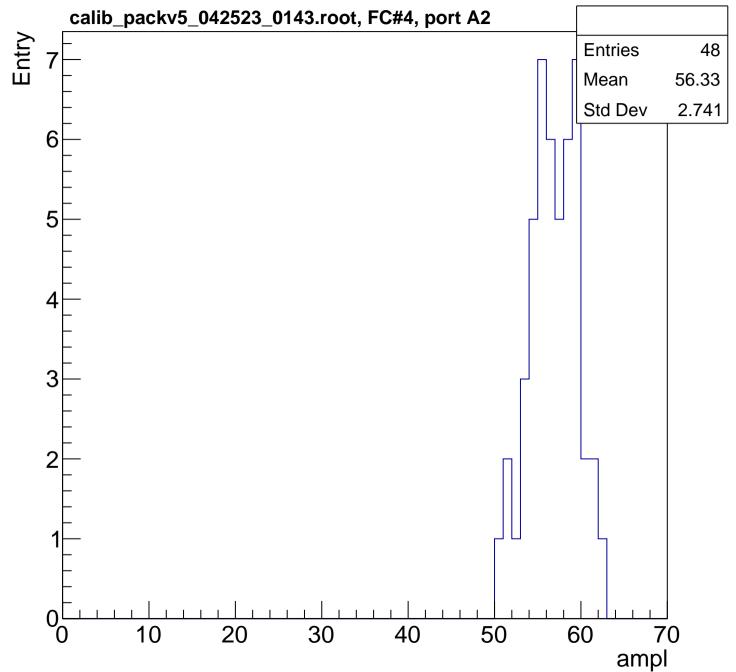


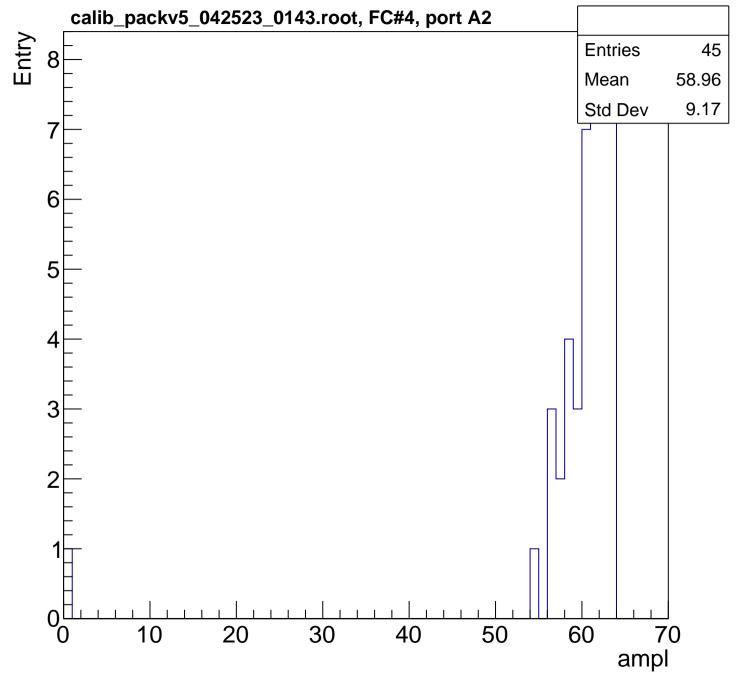


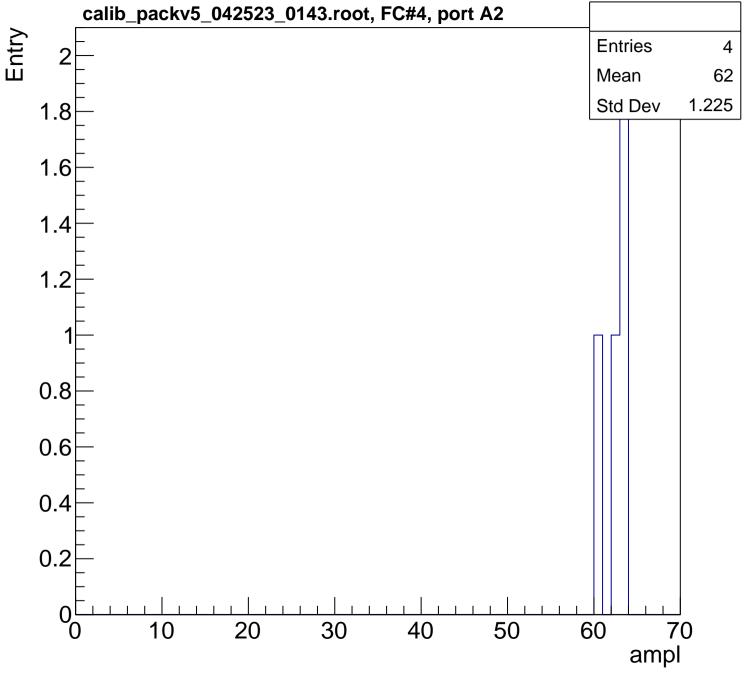


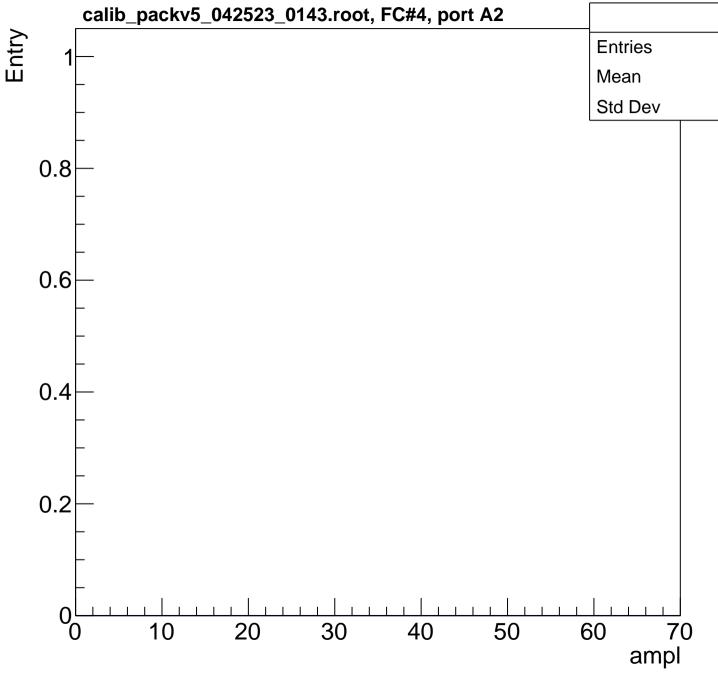


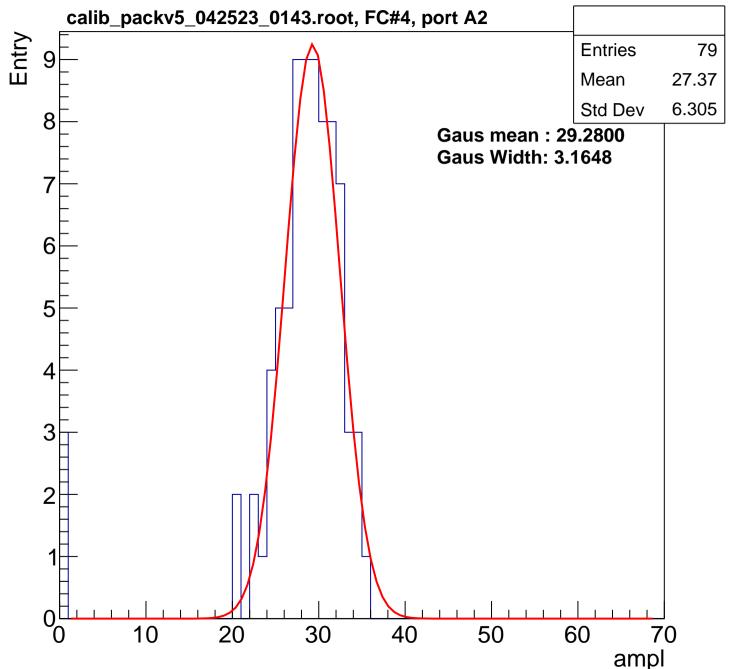


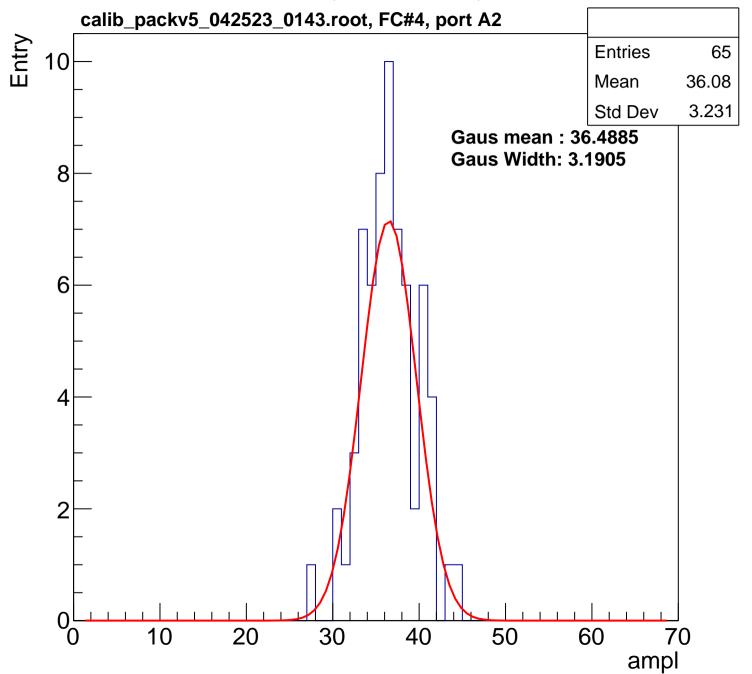


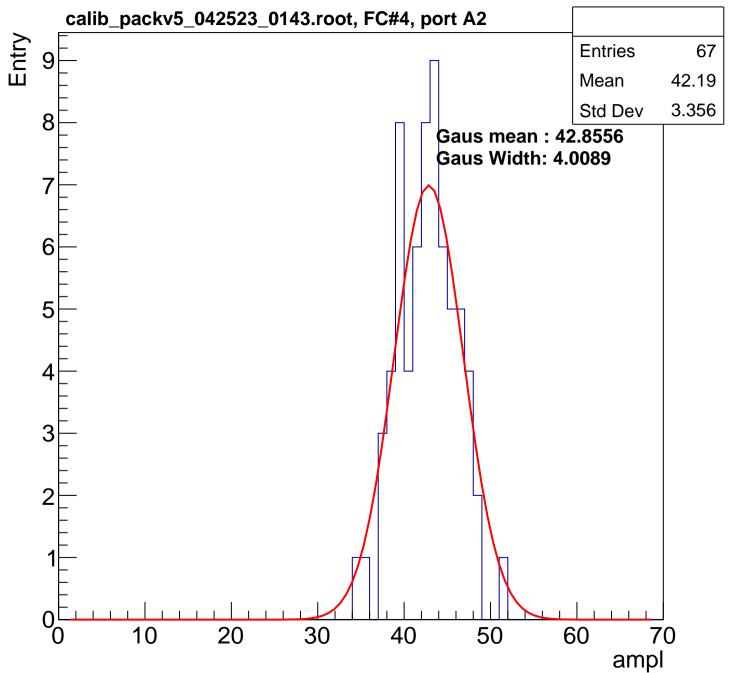


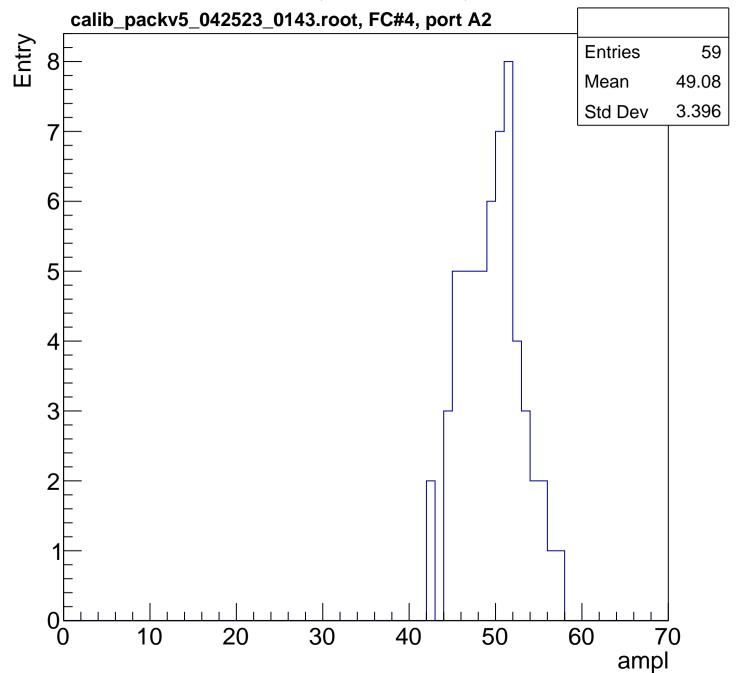


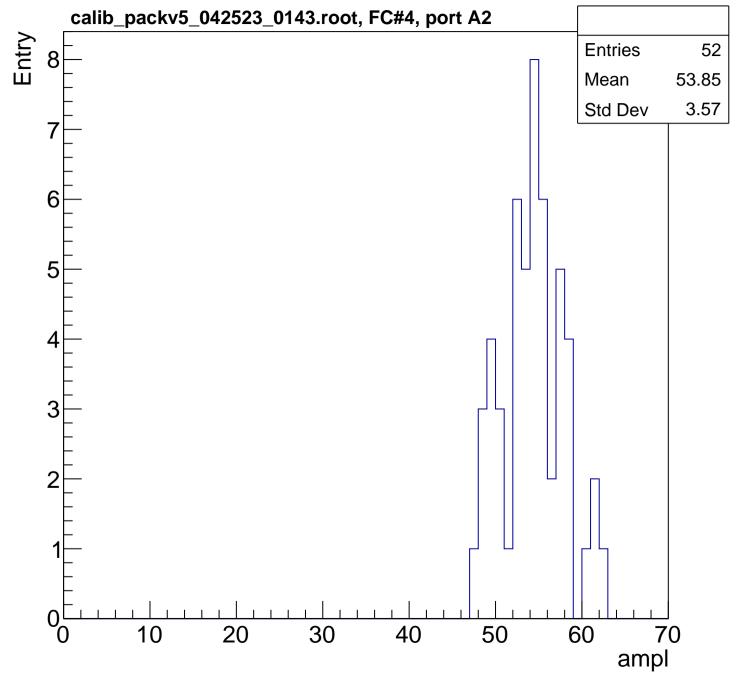


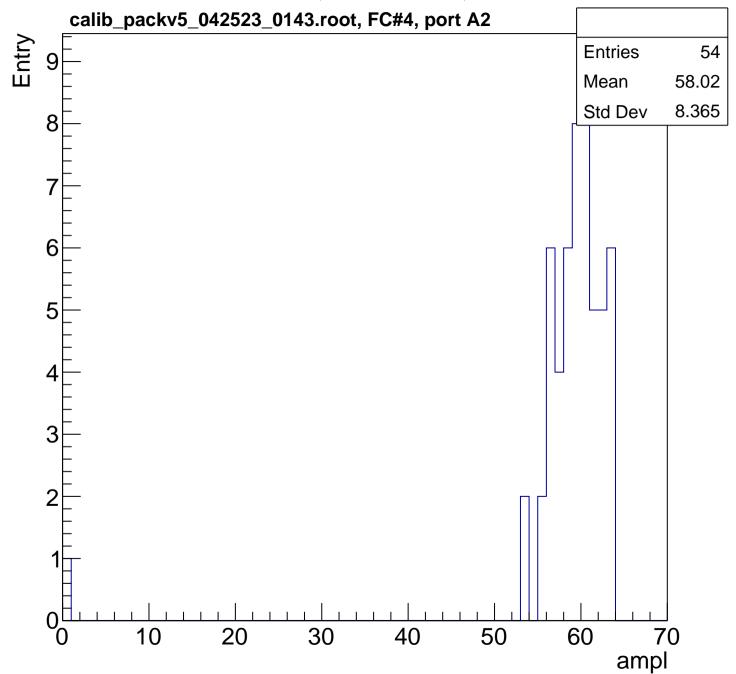


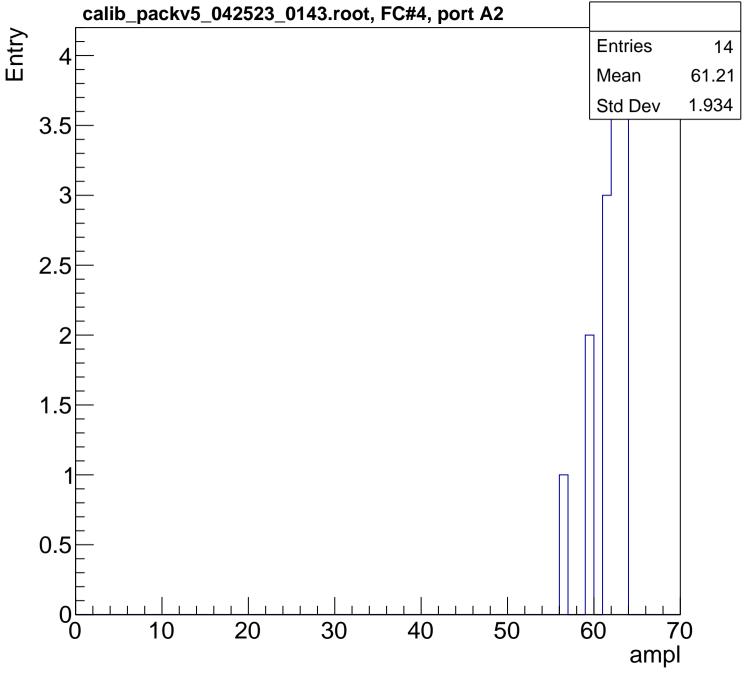










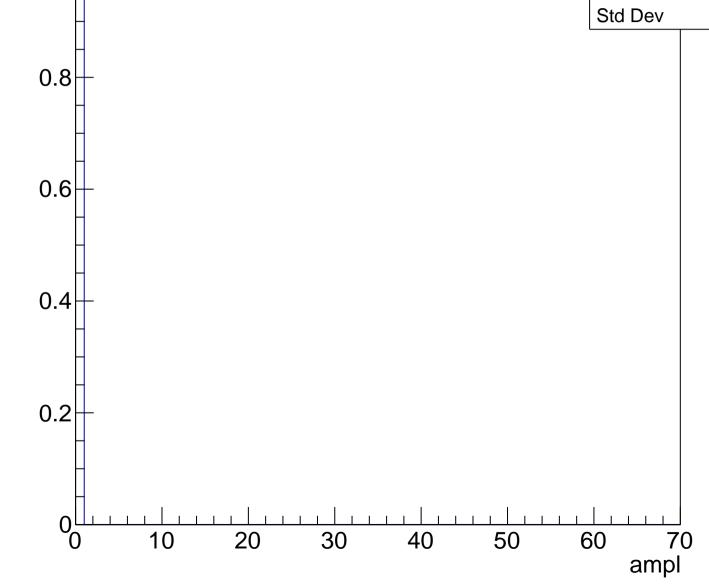


B1L100S, U3-ch26, adc7 calib_packv5_042523_0143.root, FC#4, port A2 **Entries** Mean Std Dev

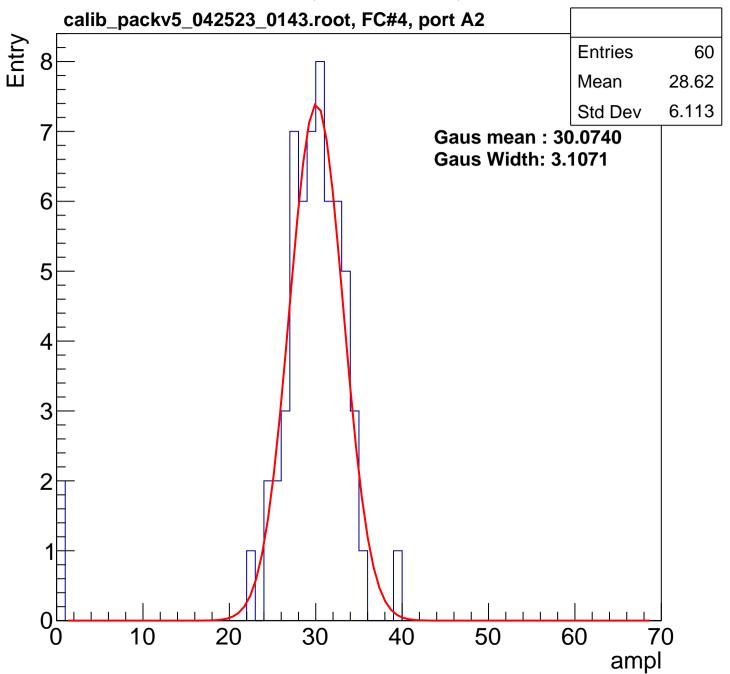
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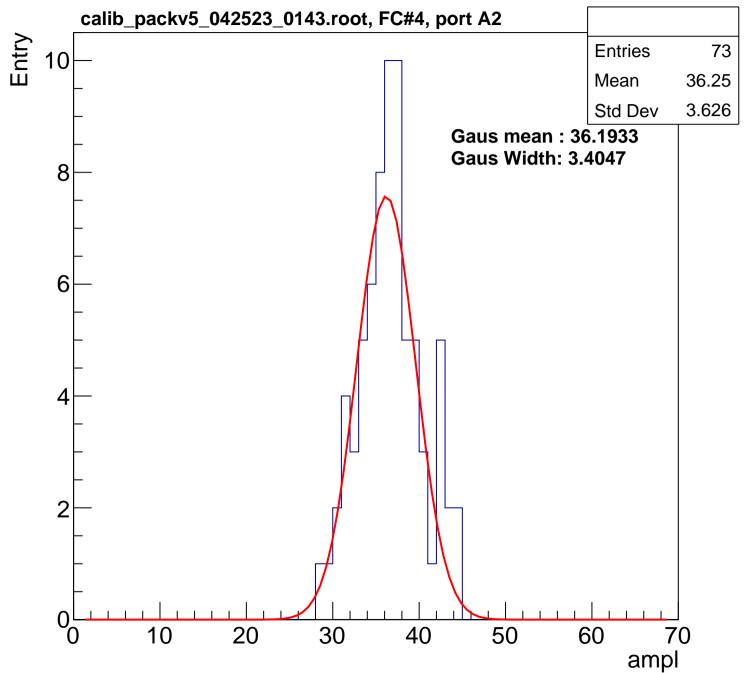
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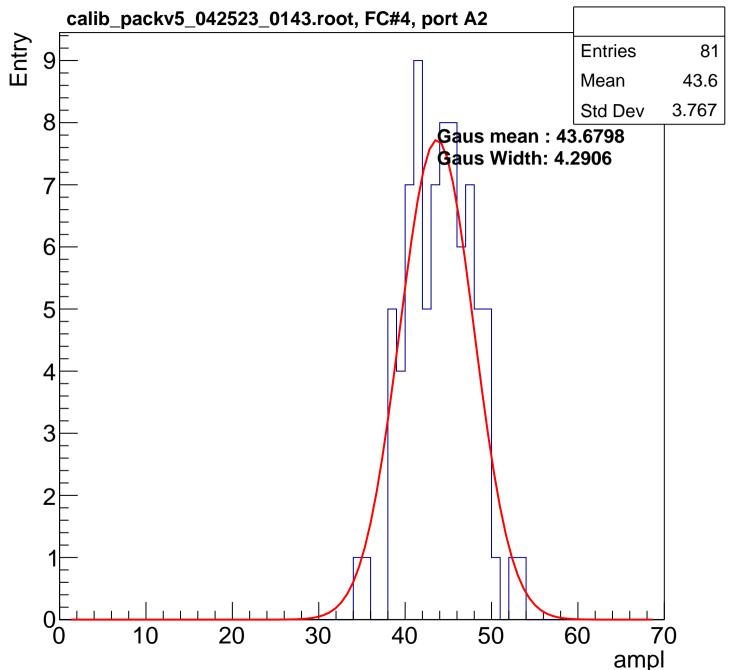
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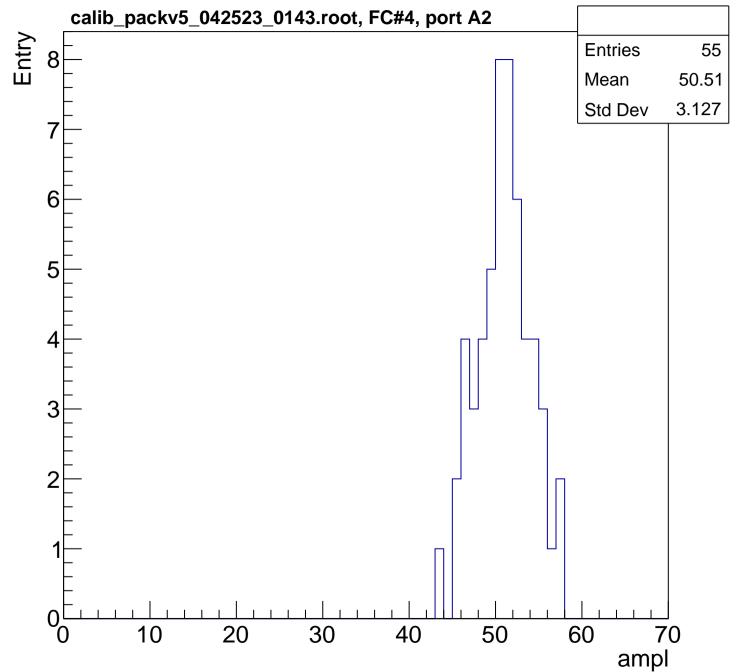


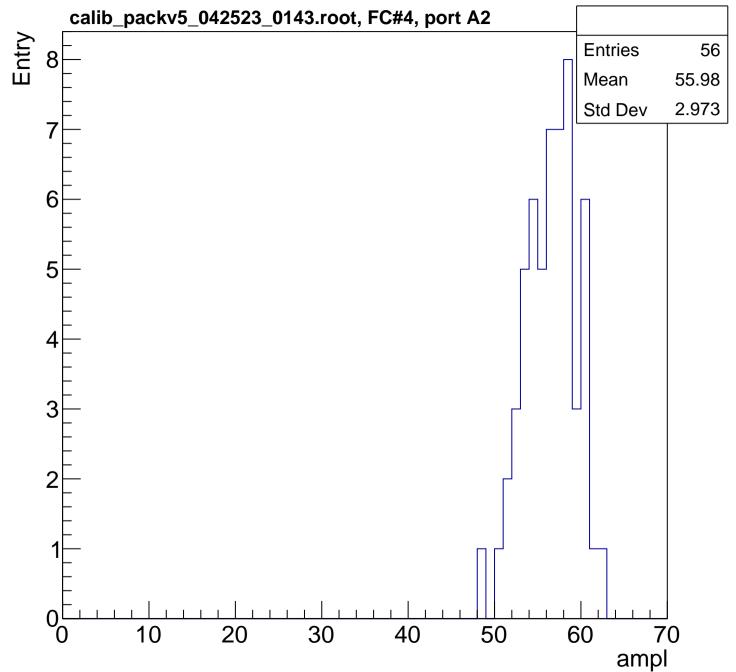
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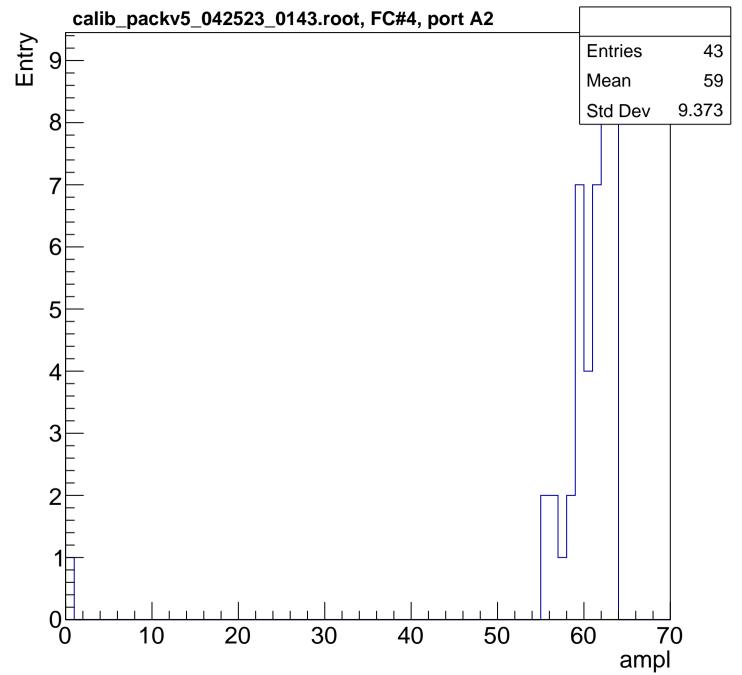


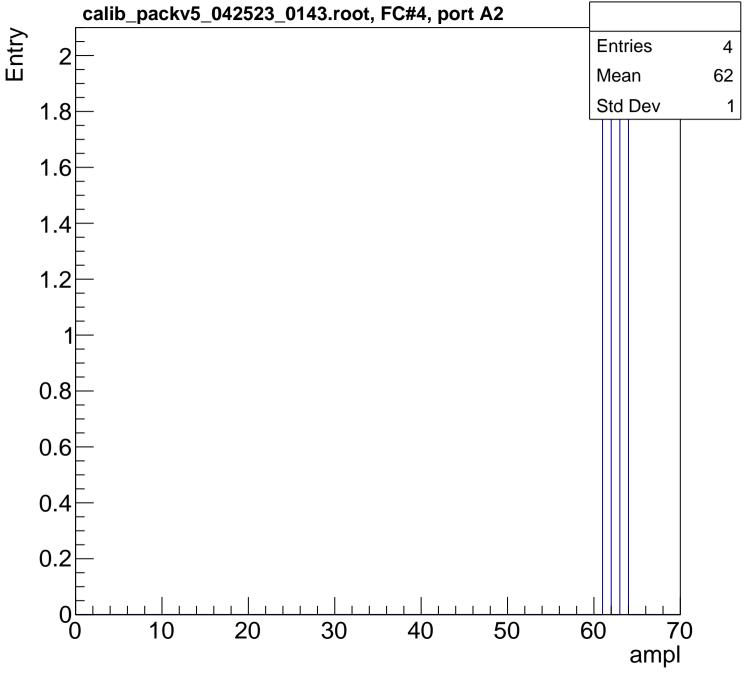




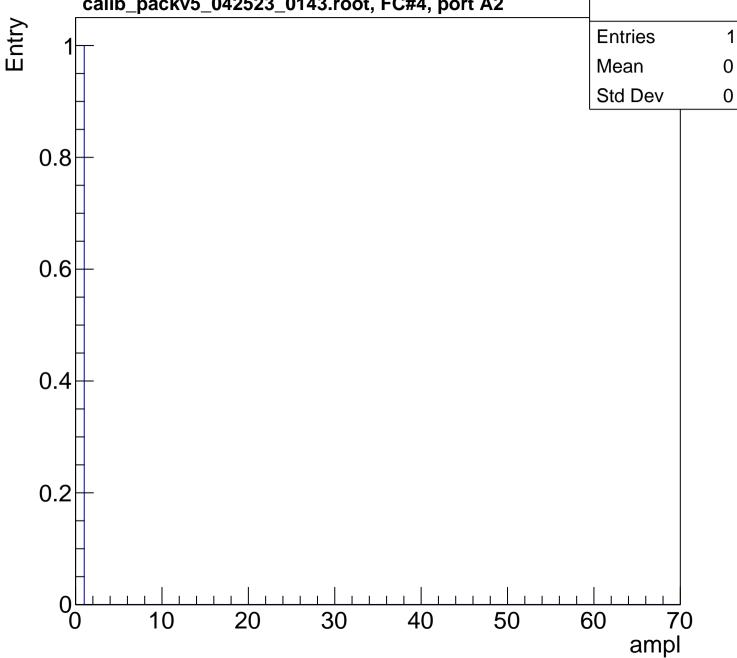


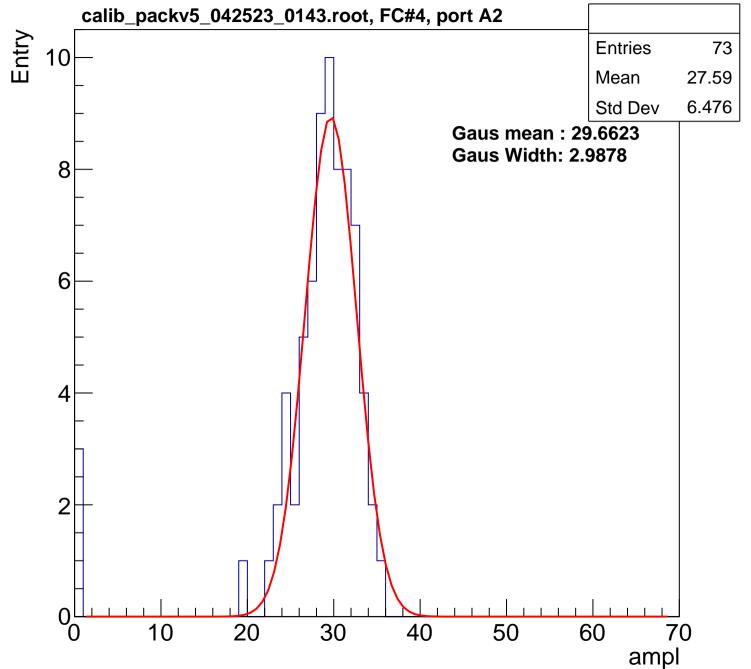


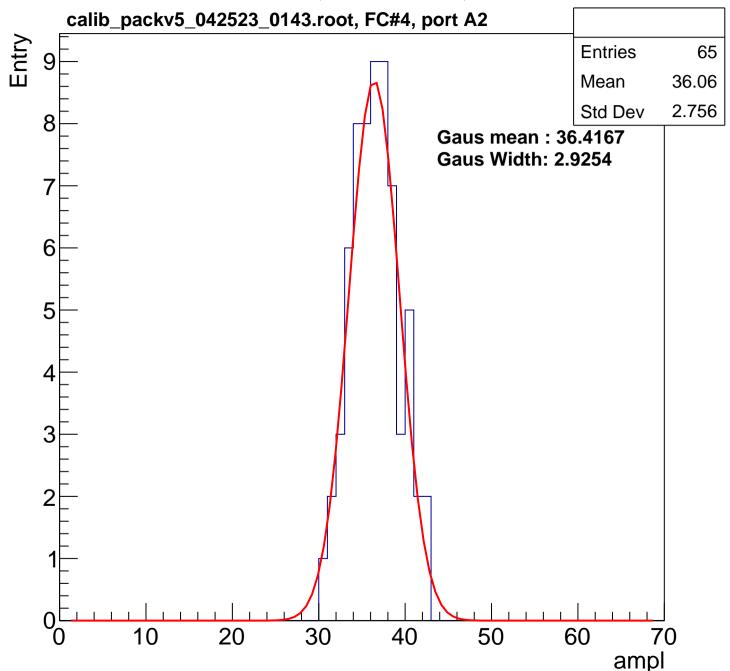


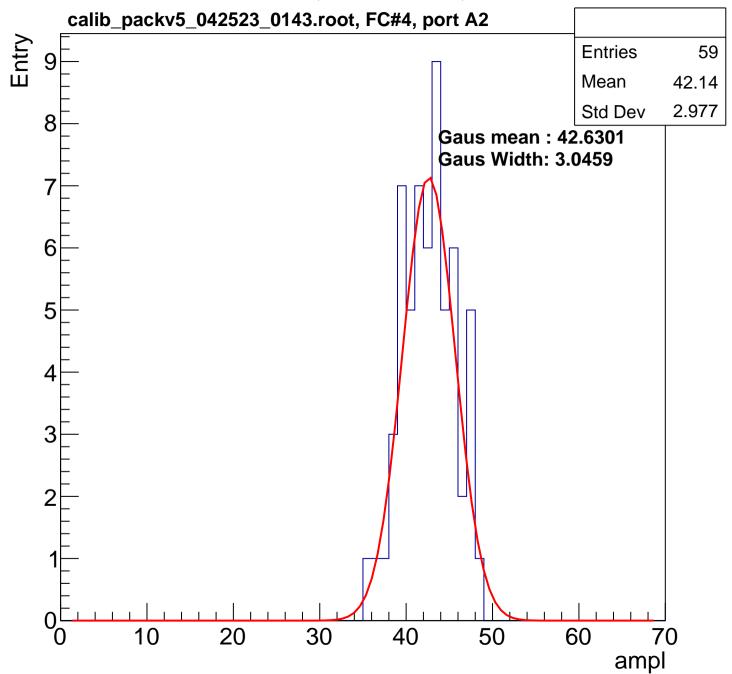


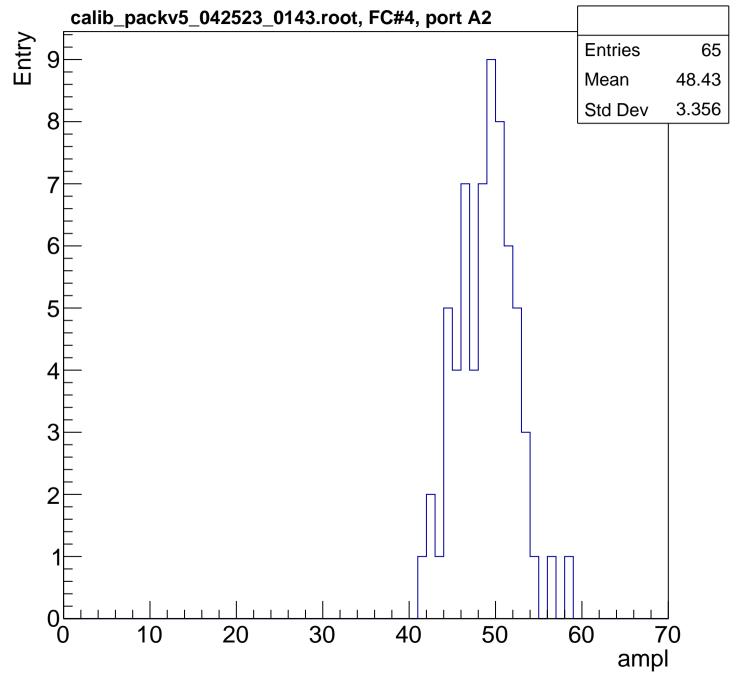
B1L100S, U3-ch27, adc7 calib_packv5_042523_0143.root, FC#4, port A2

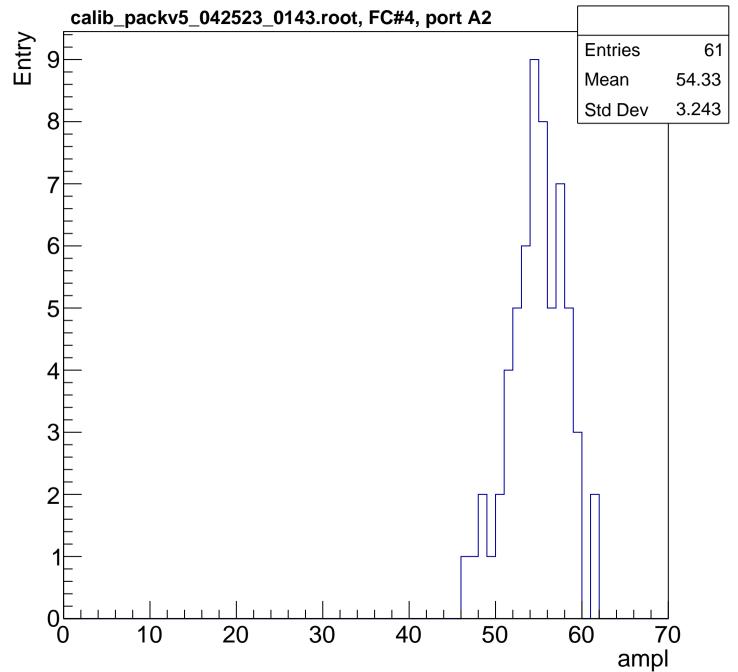


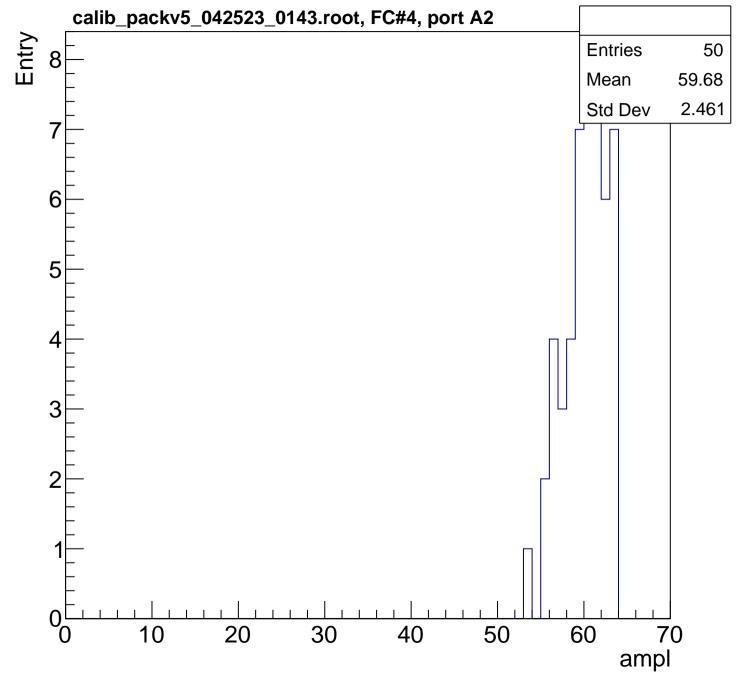


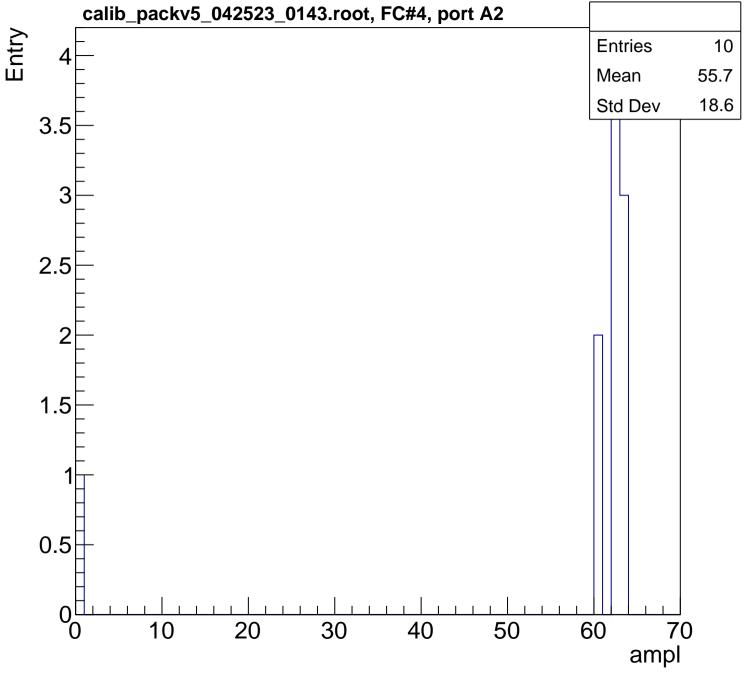




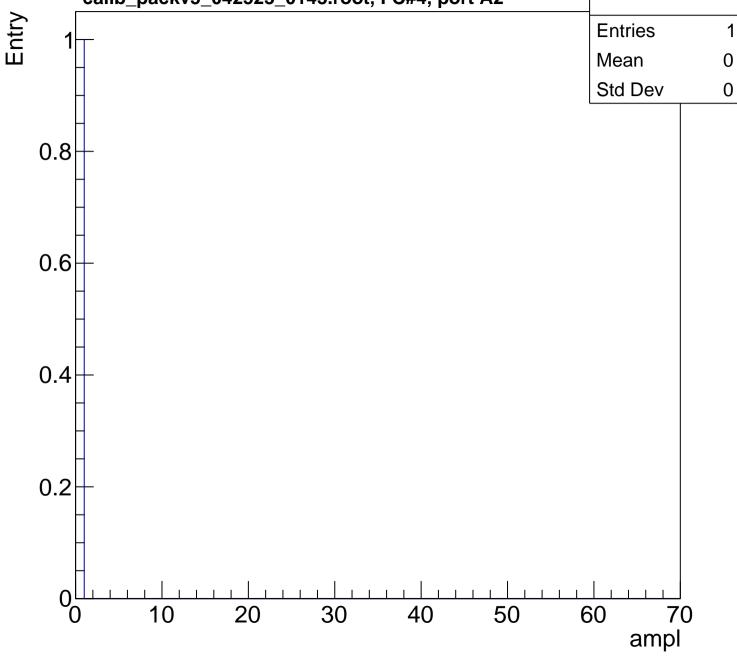


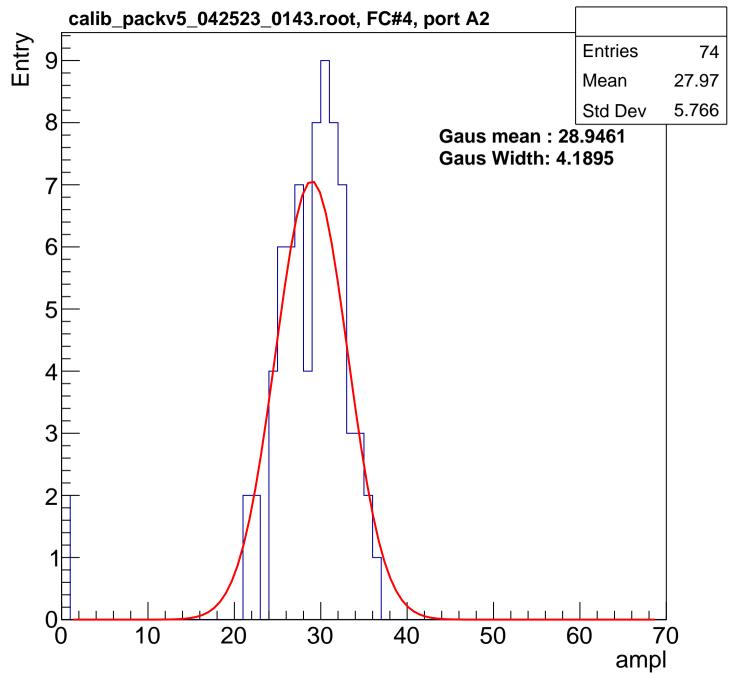


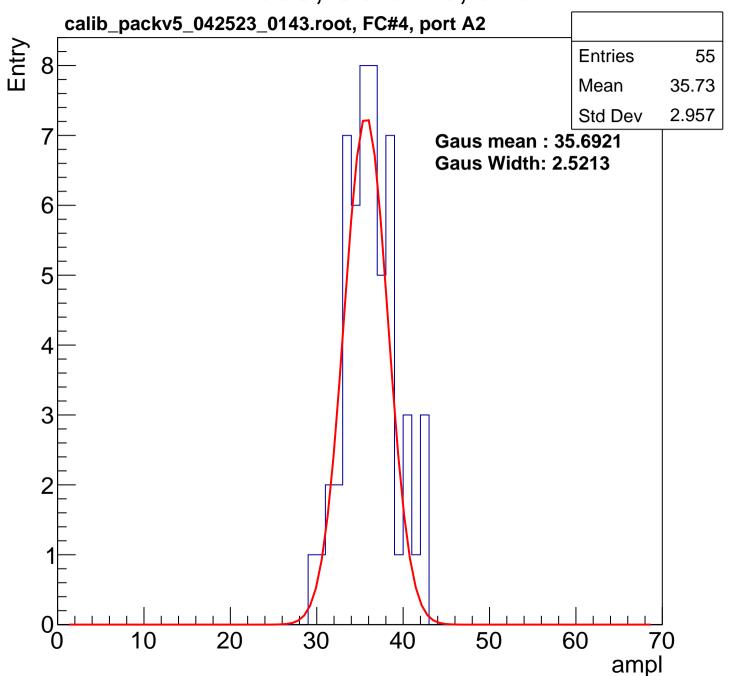


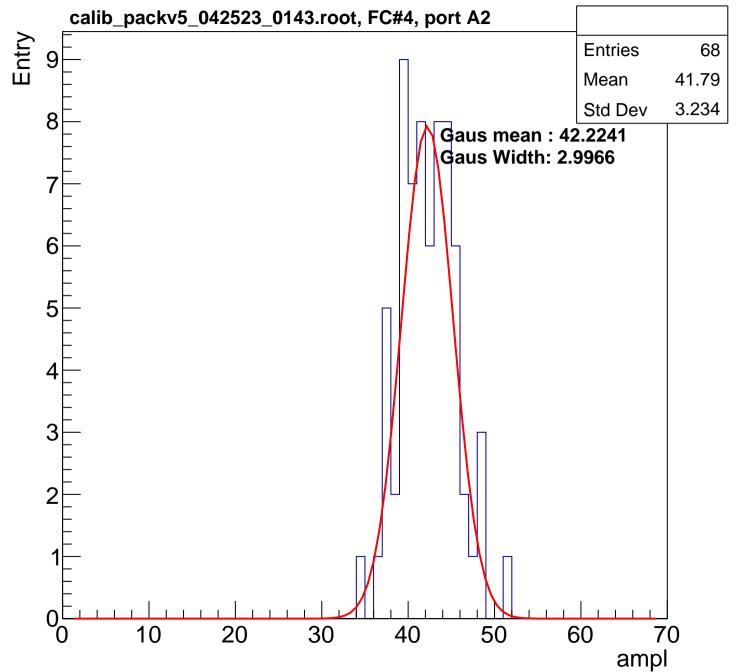


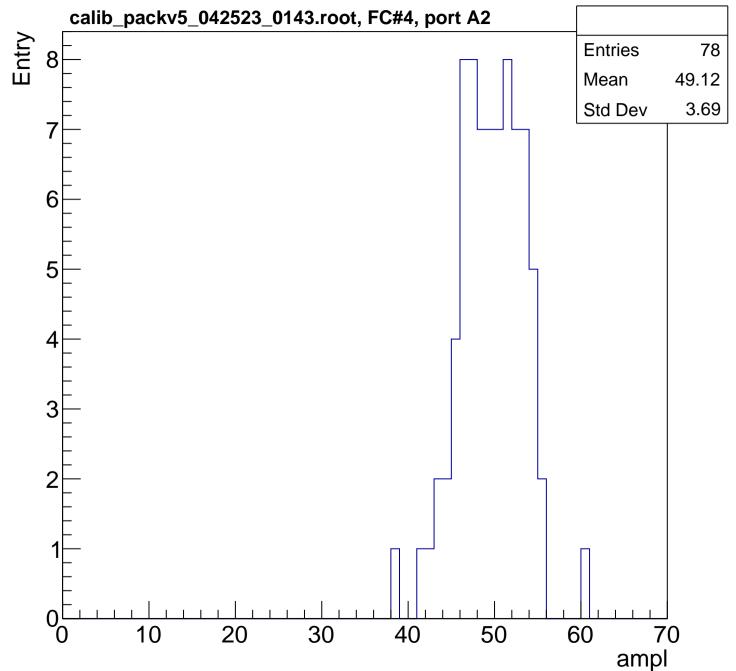
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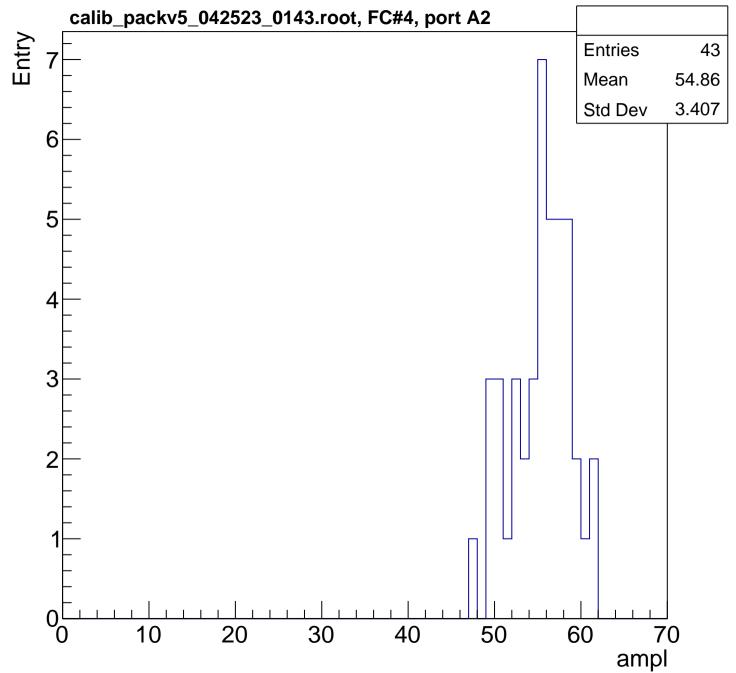


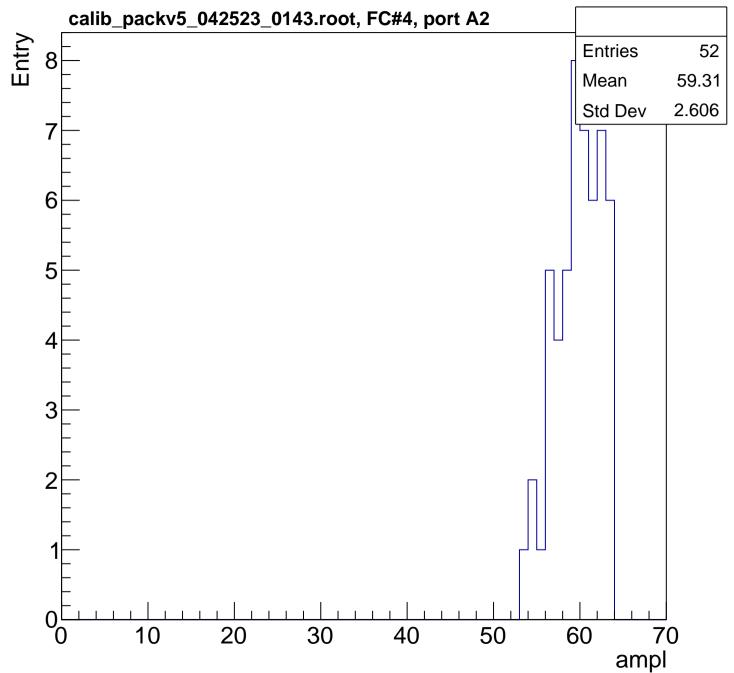


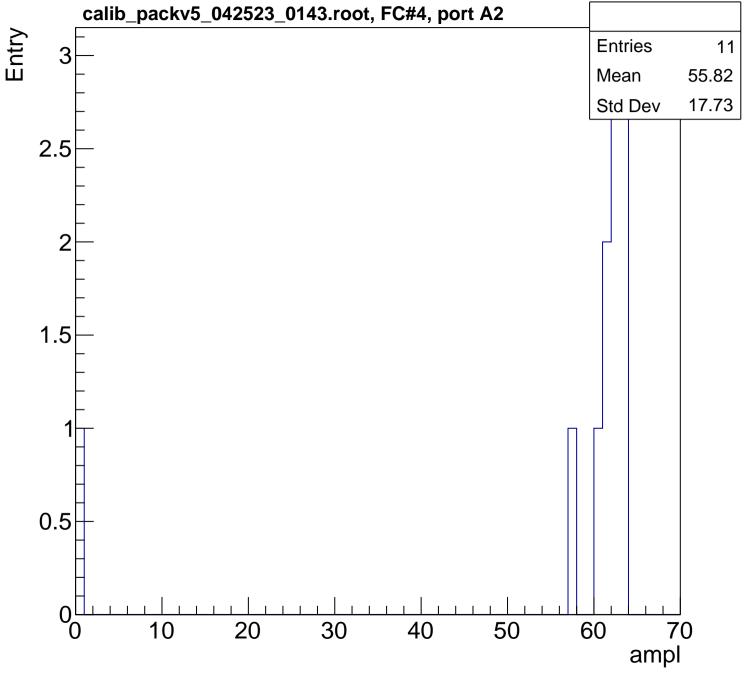


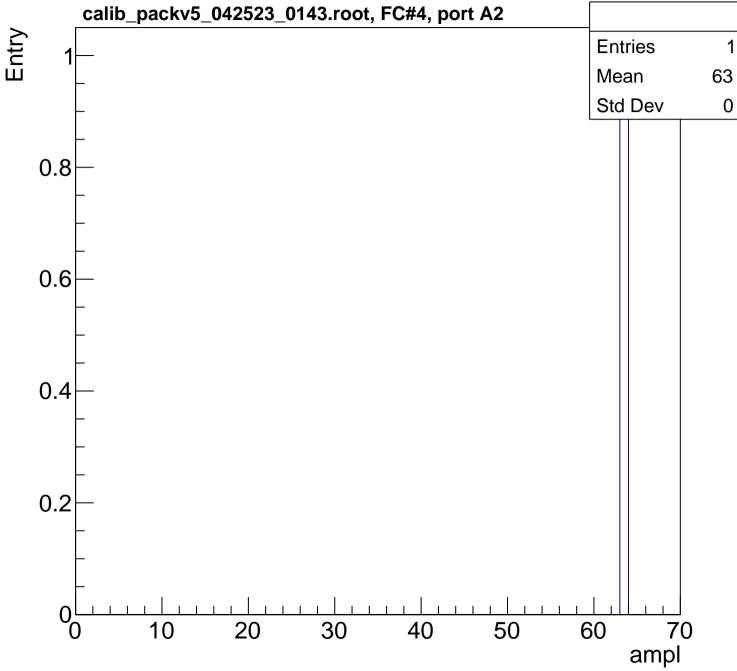


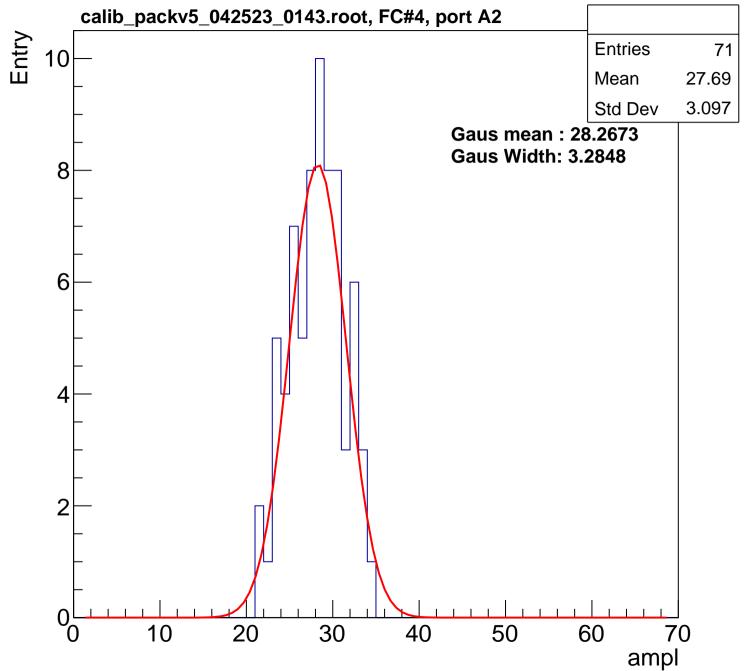


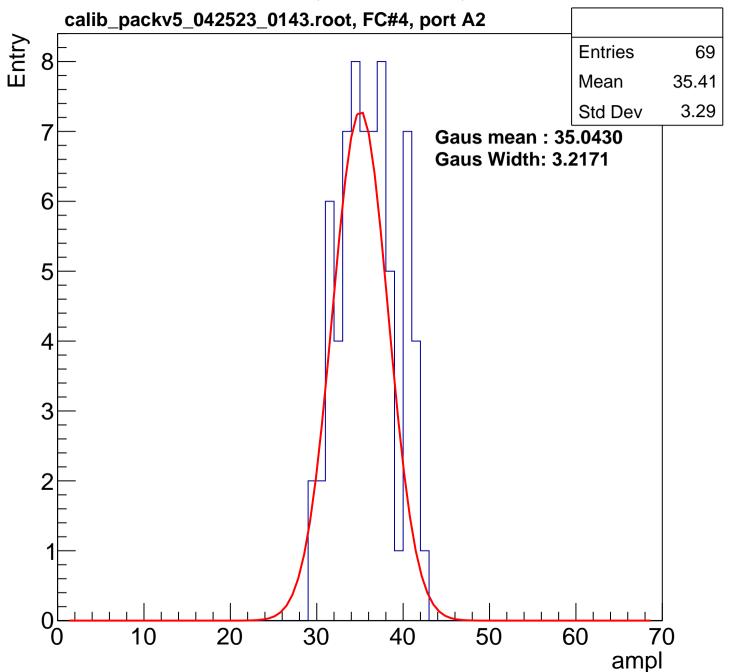


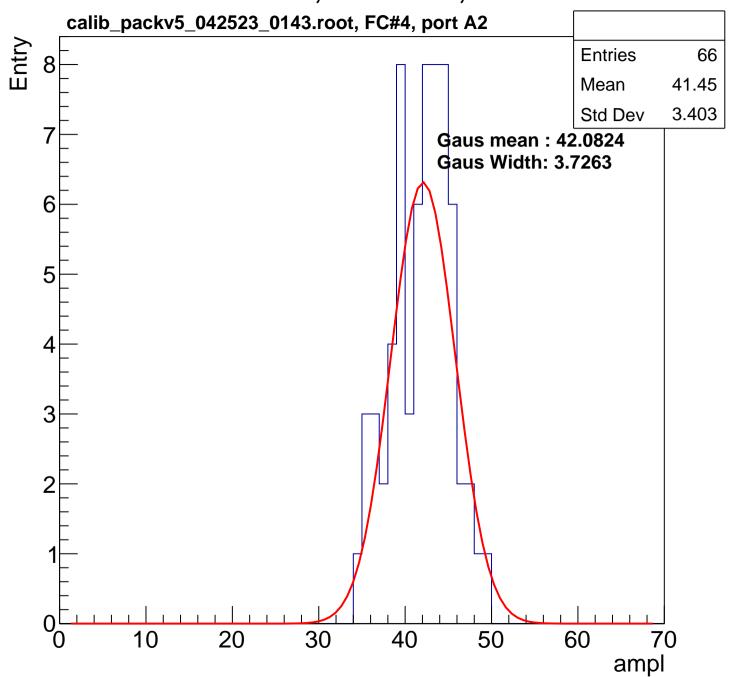


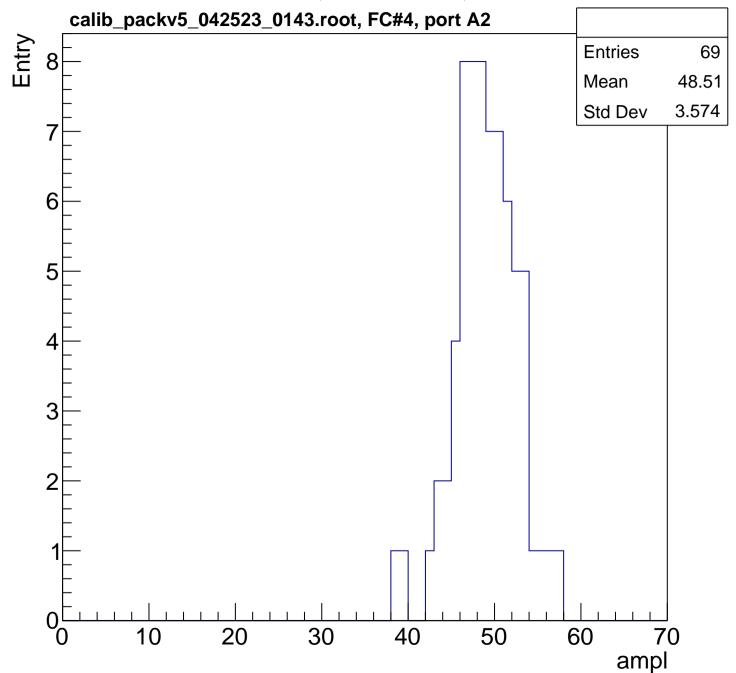


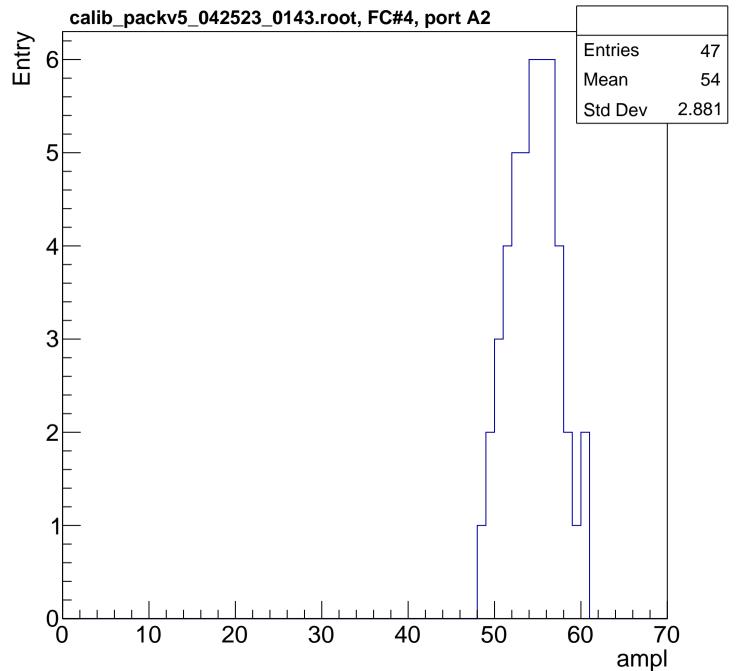


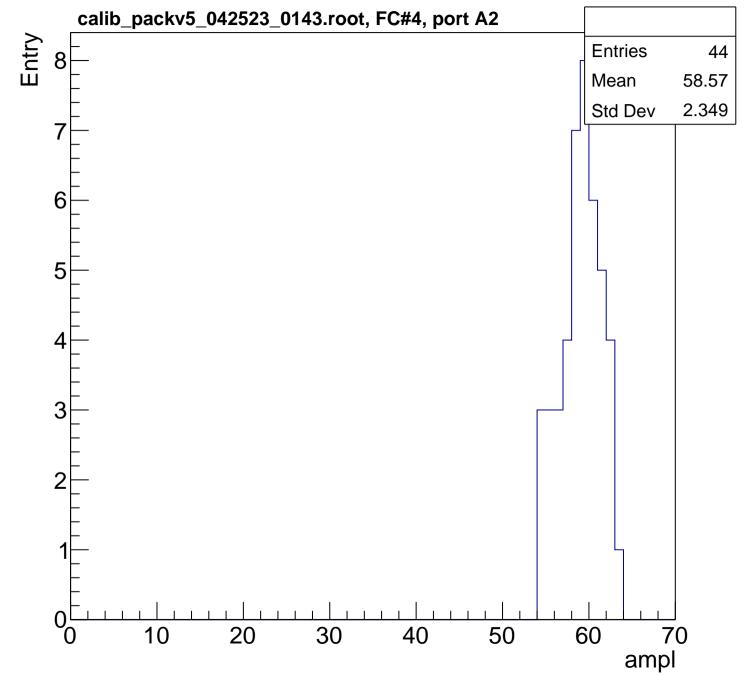


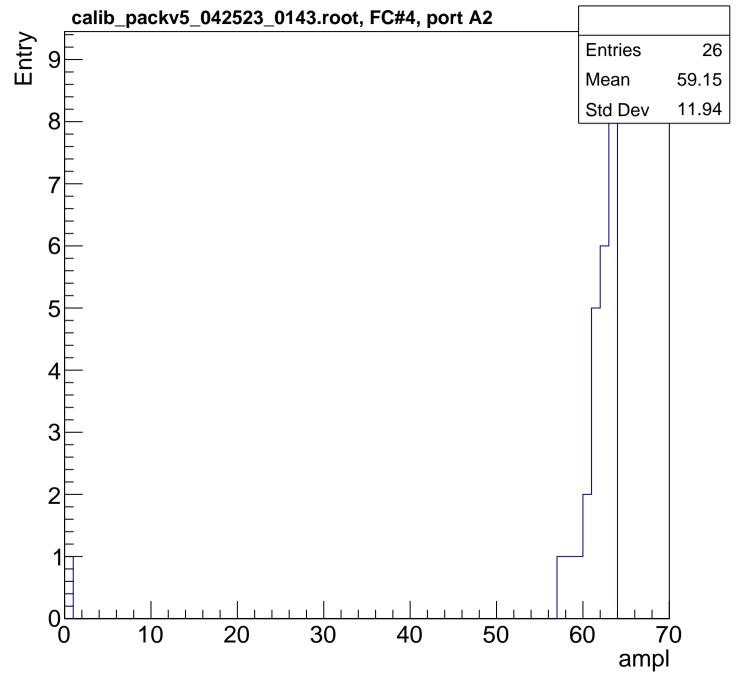


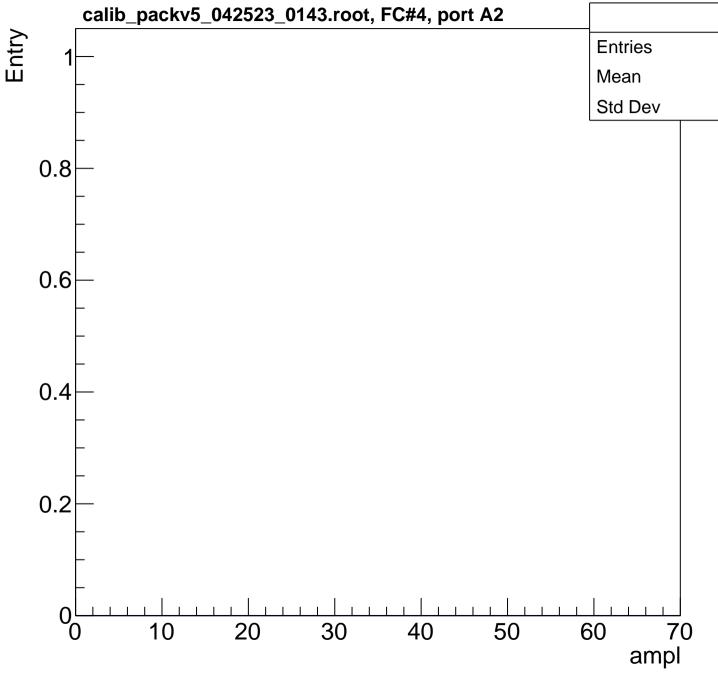


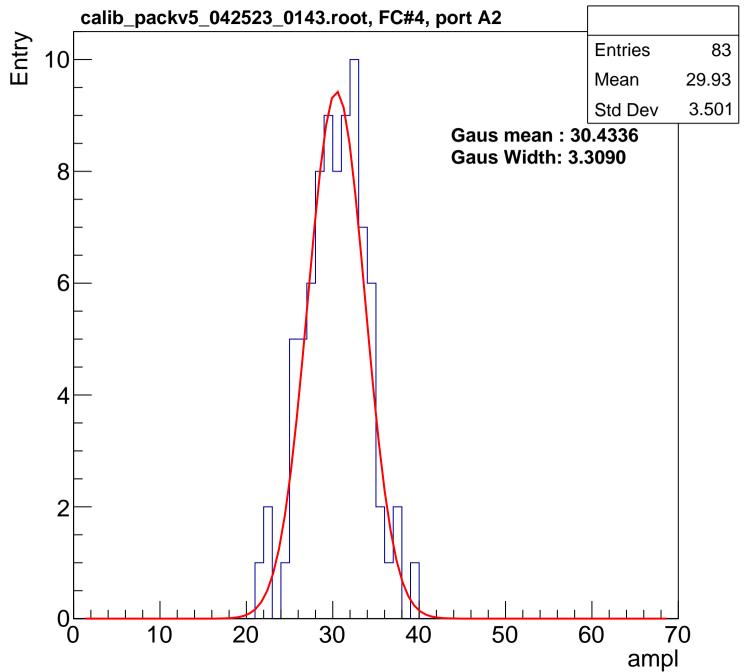


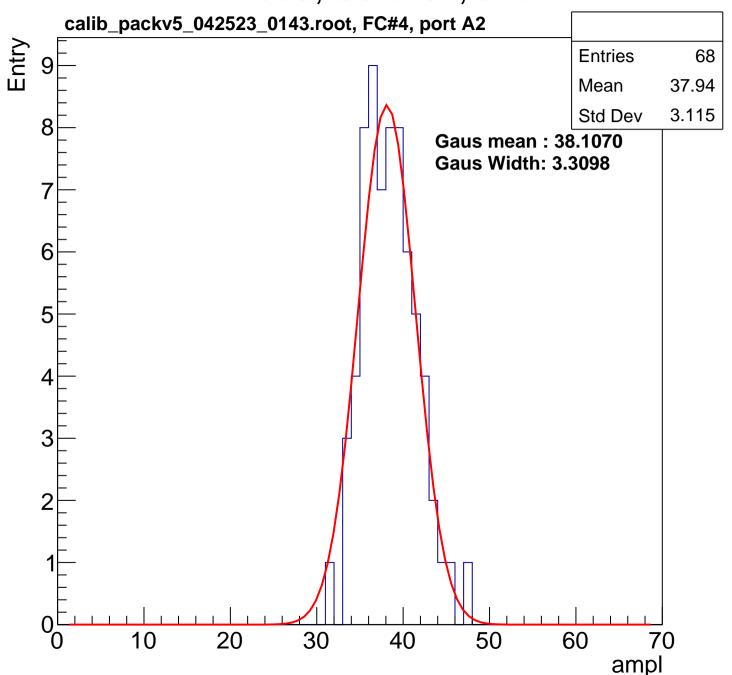


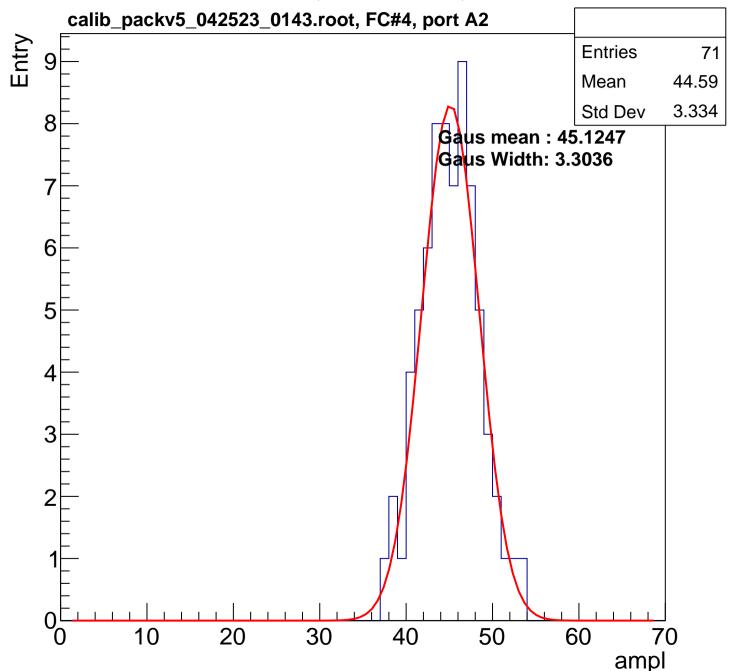


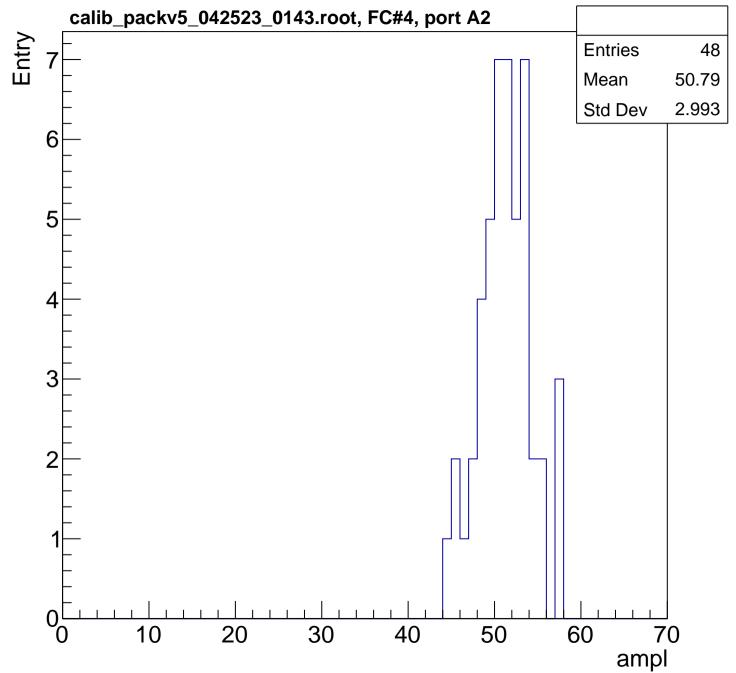


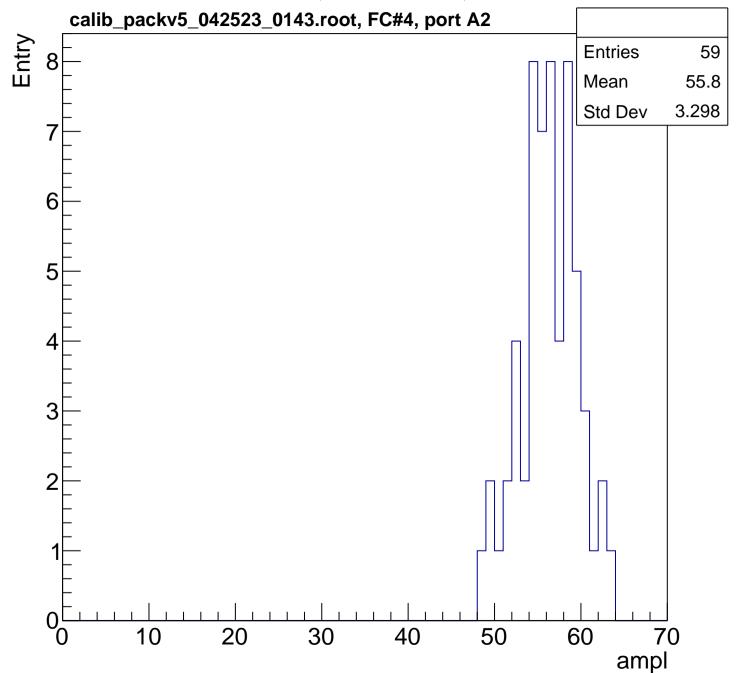


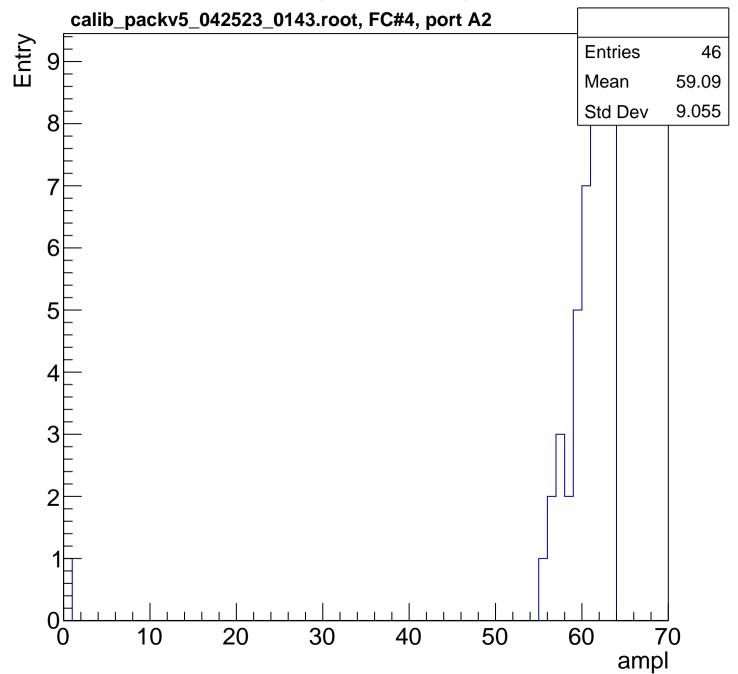


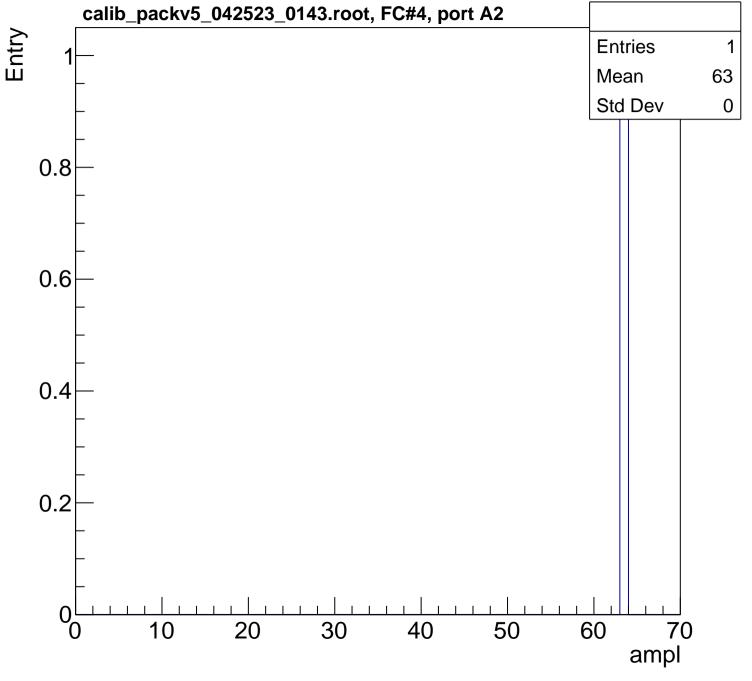




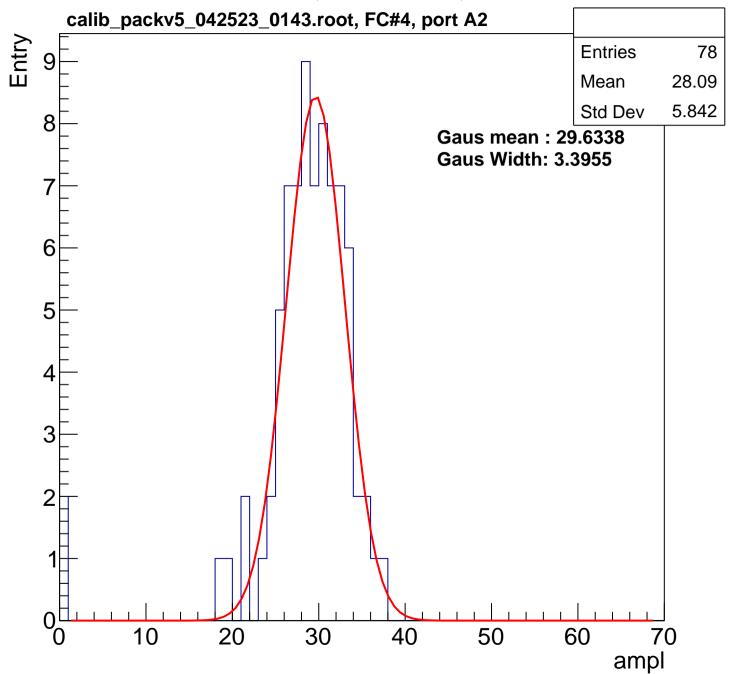


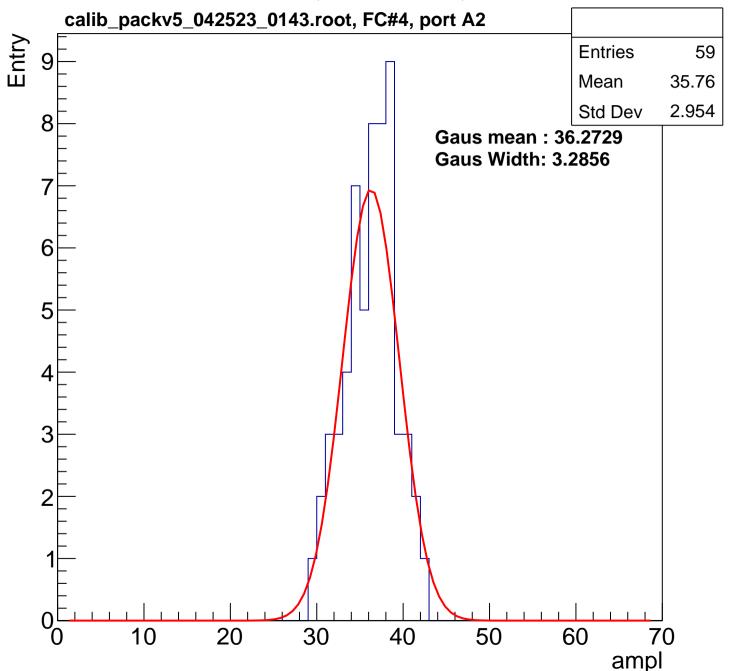


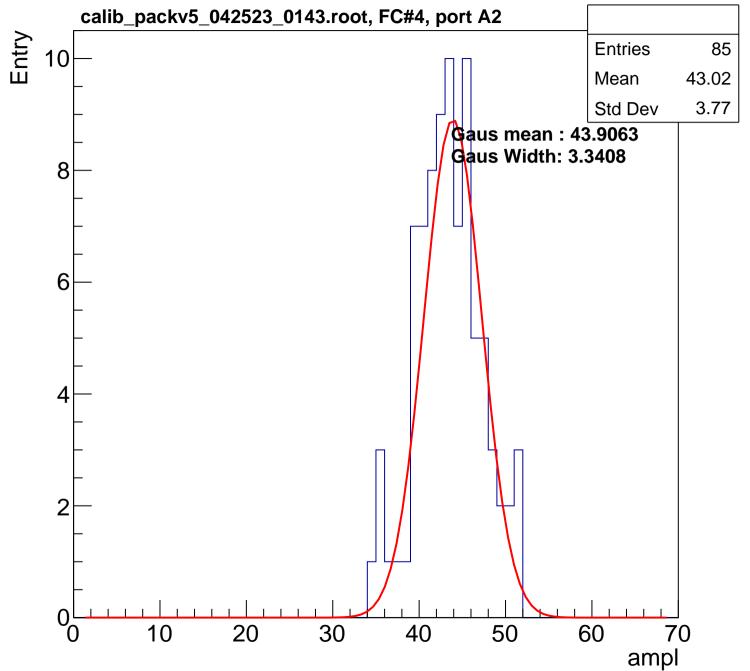


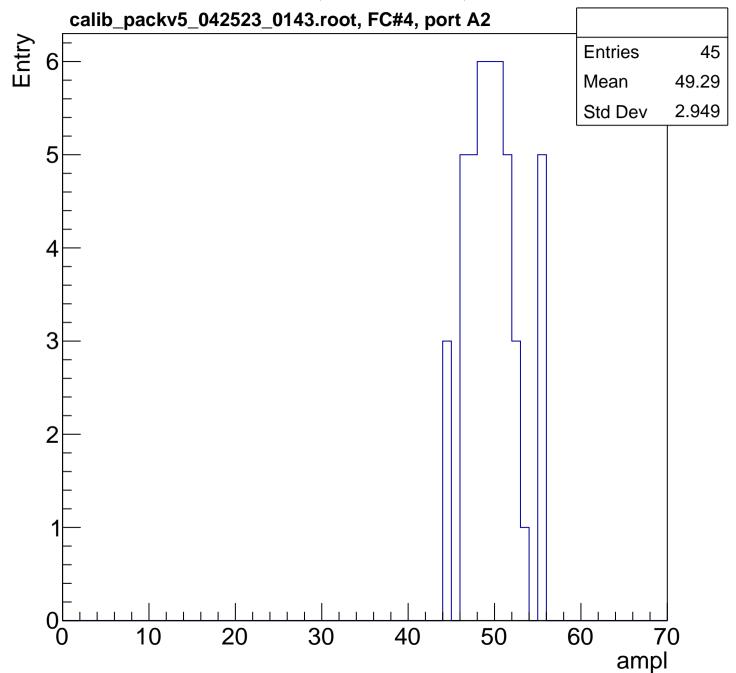


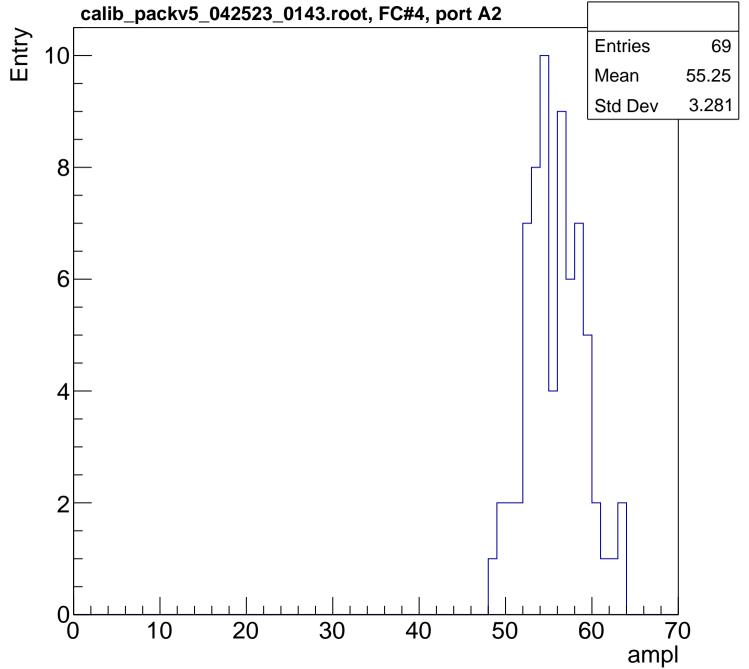


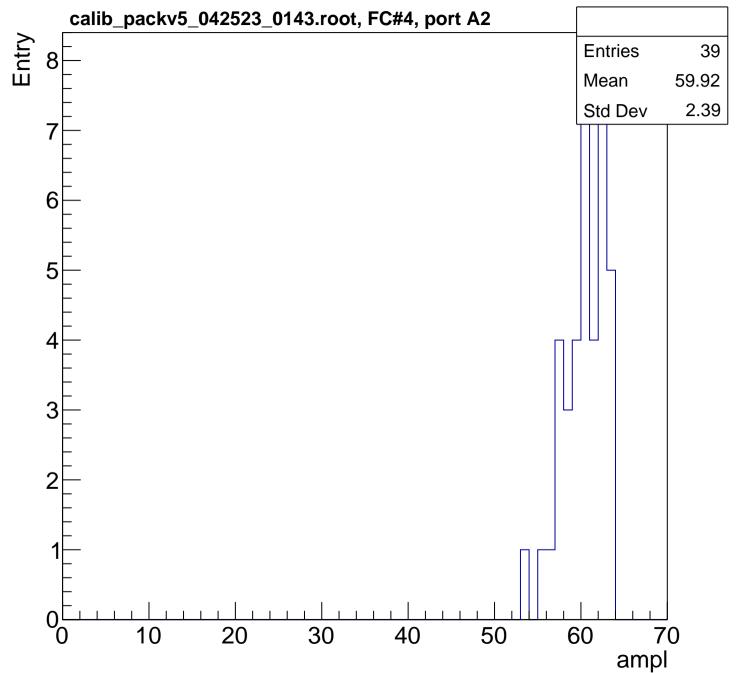


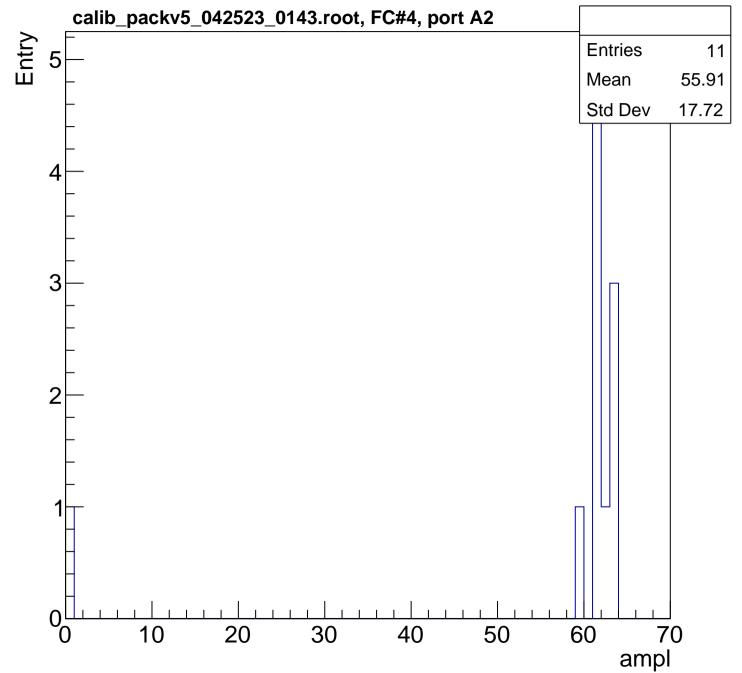




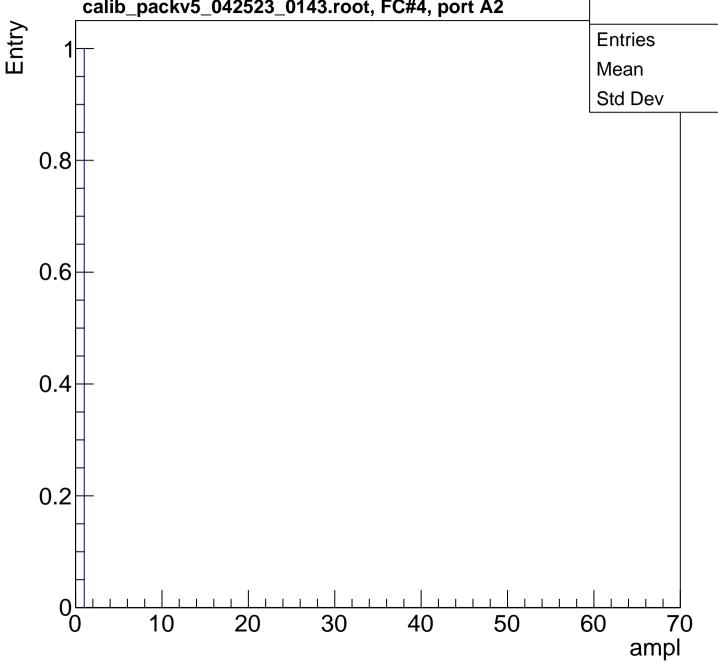


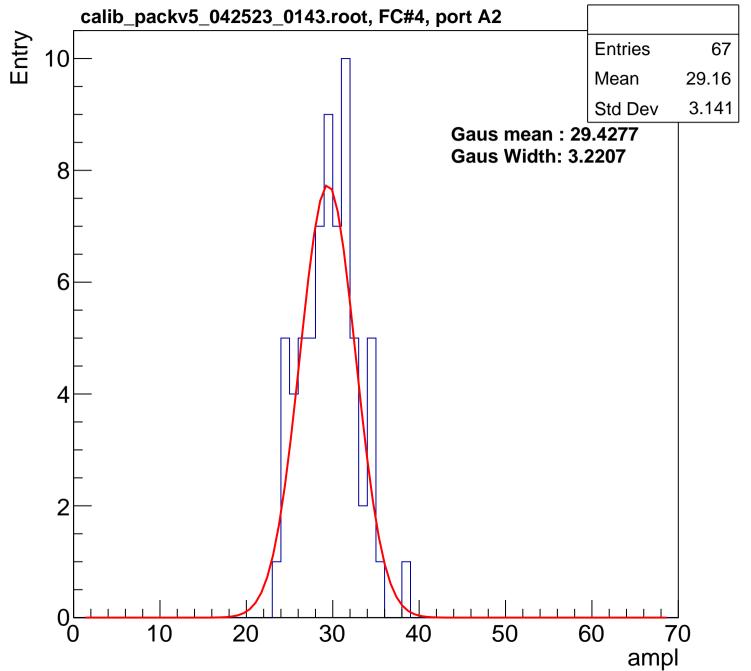


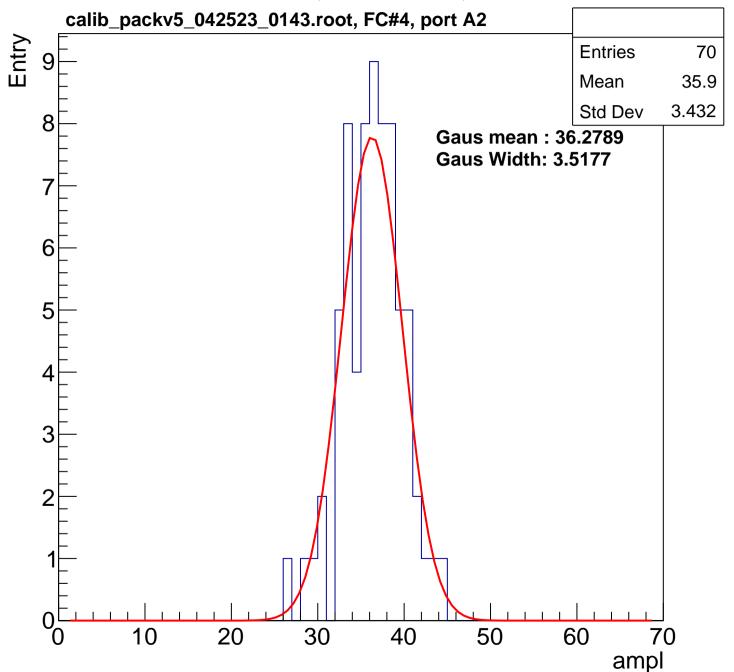


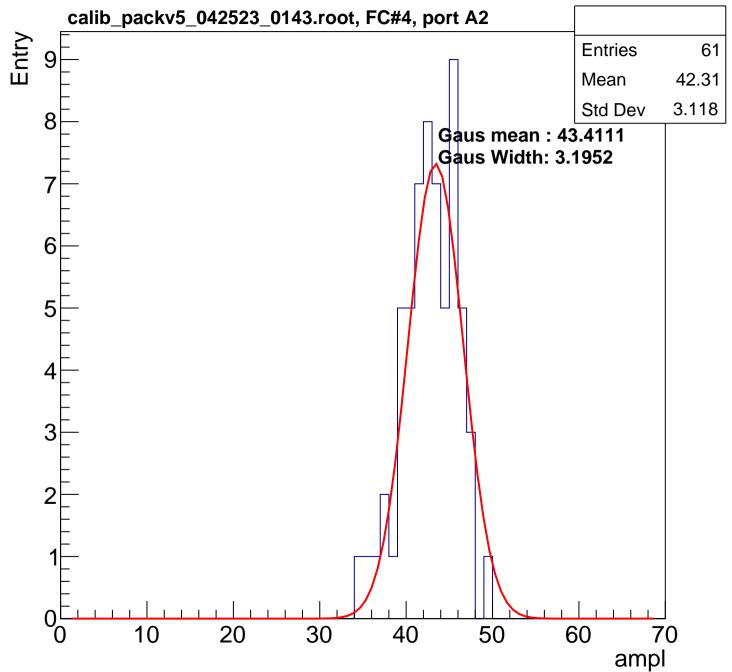


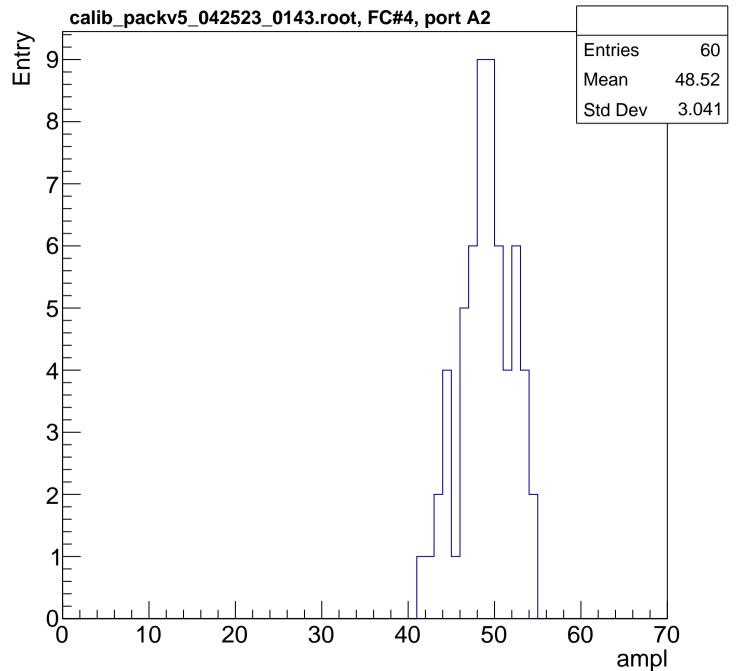
B1L100S, U3-ch32, adc7 calib_packv5_042523_0143.root, FC#4, port A2

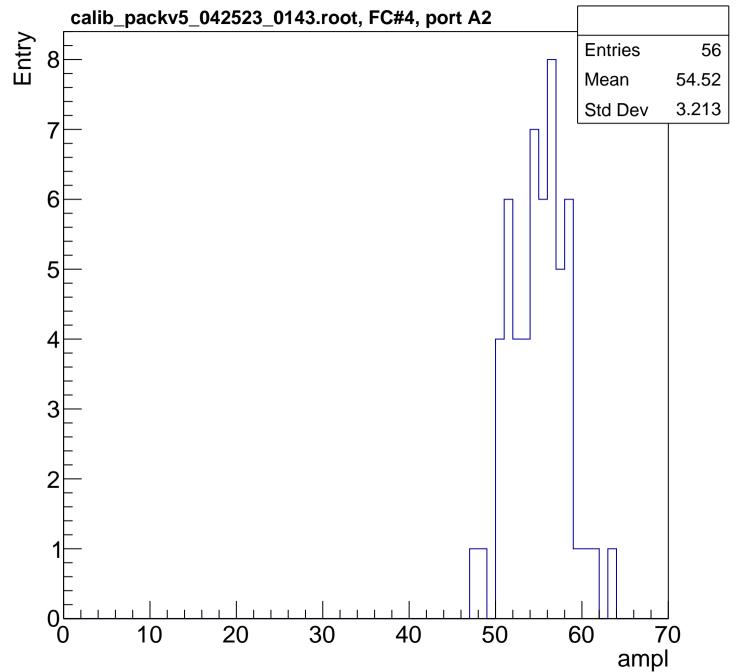


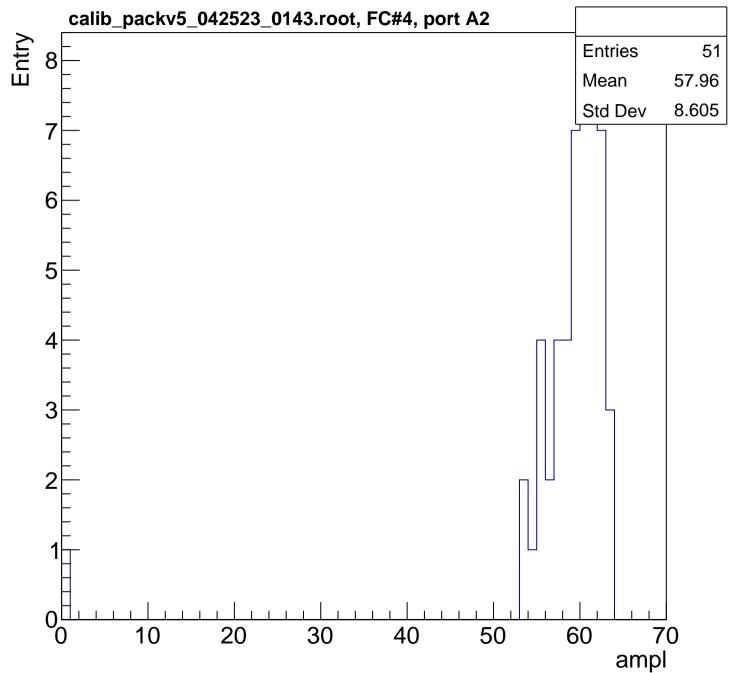


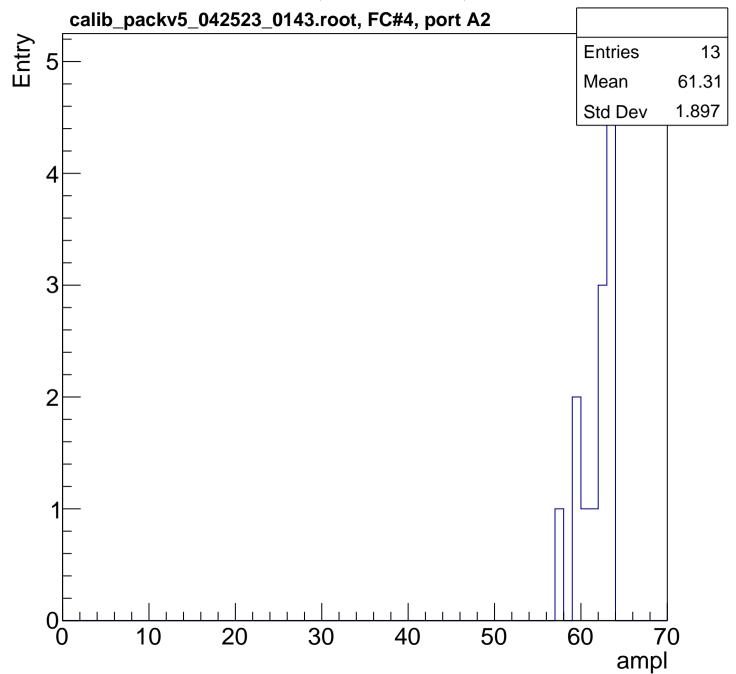


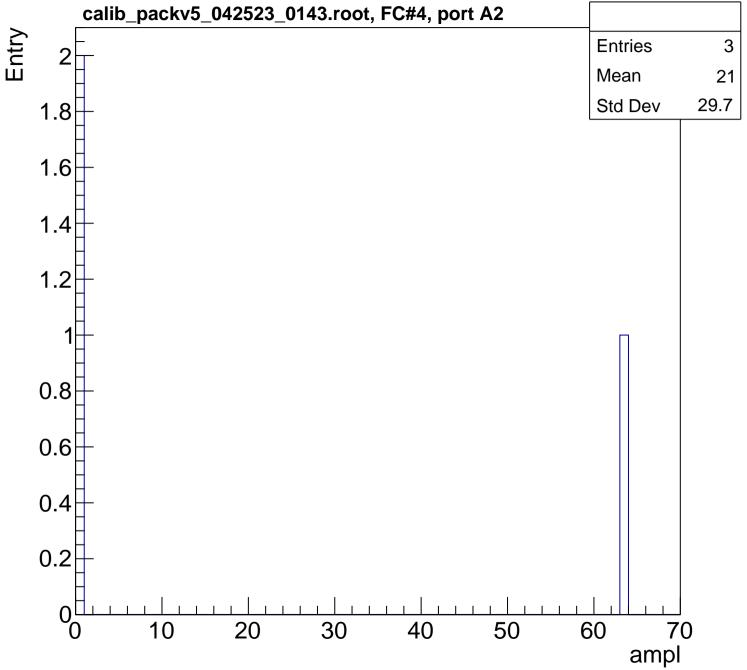


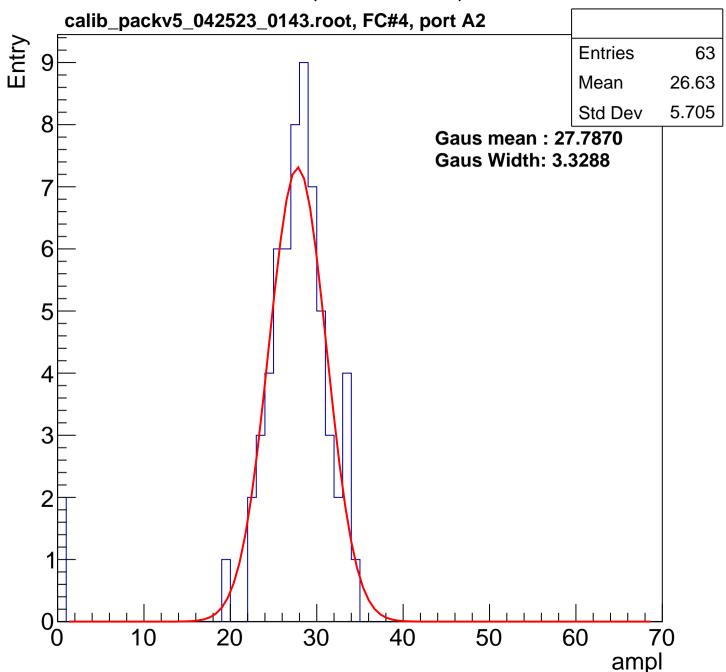


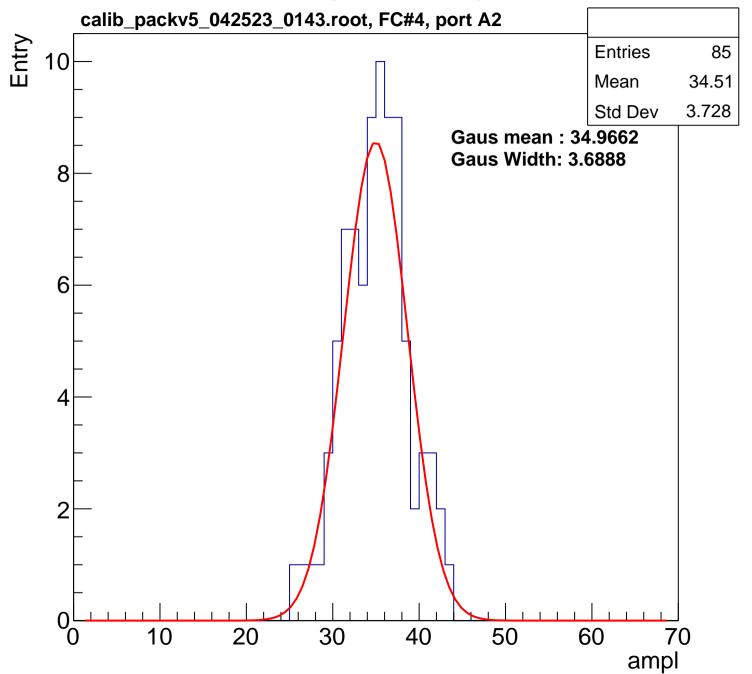


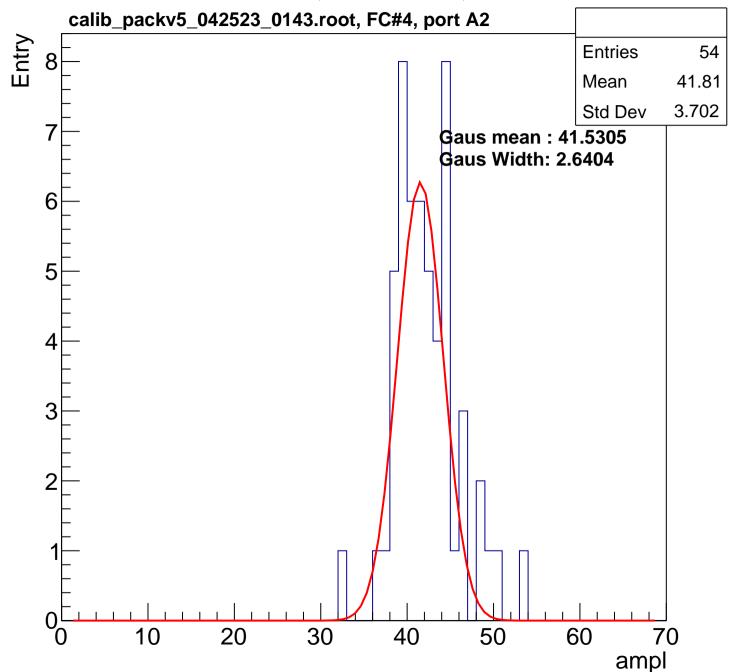


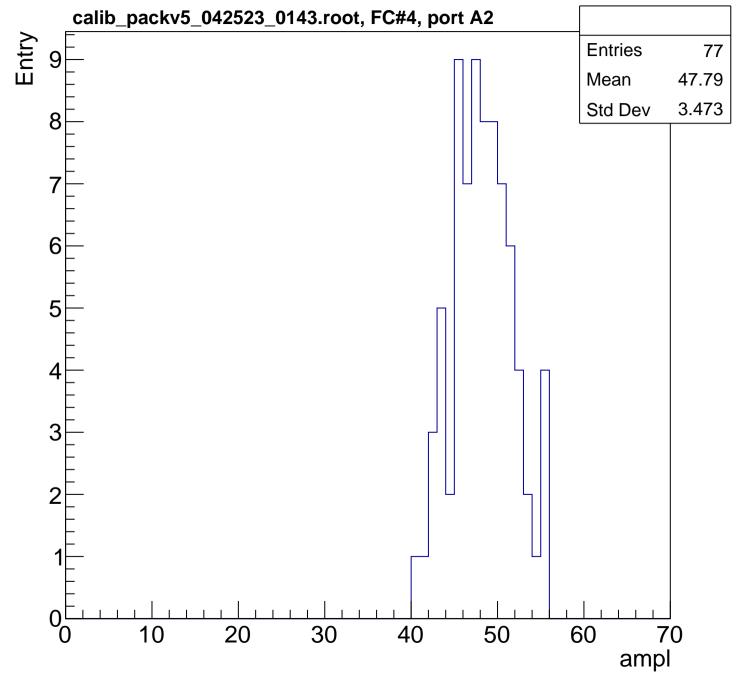


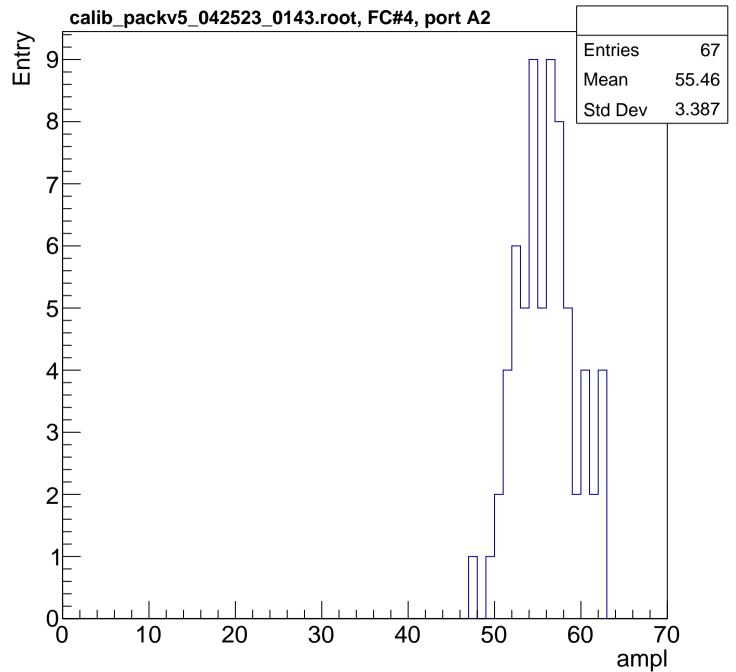


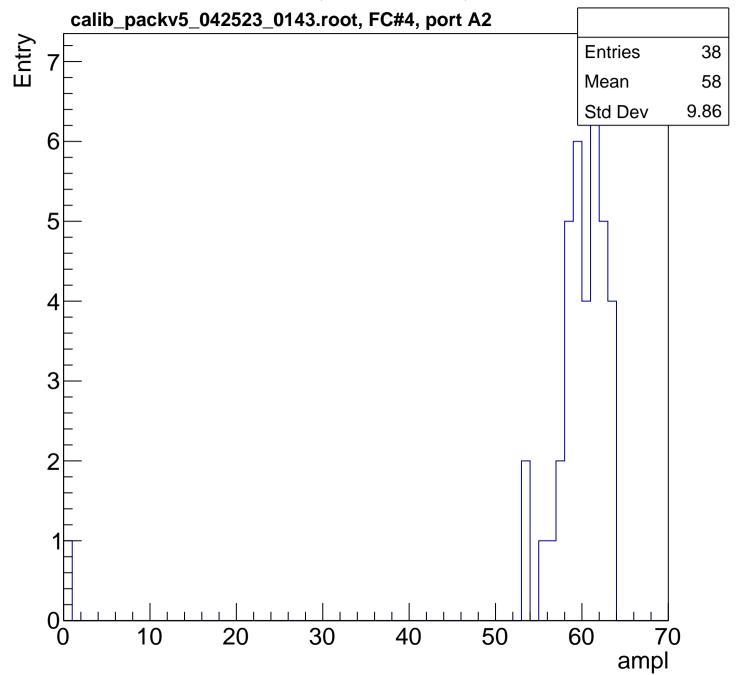


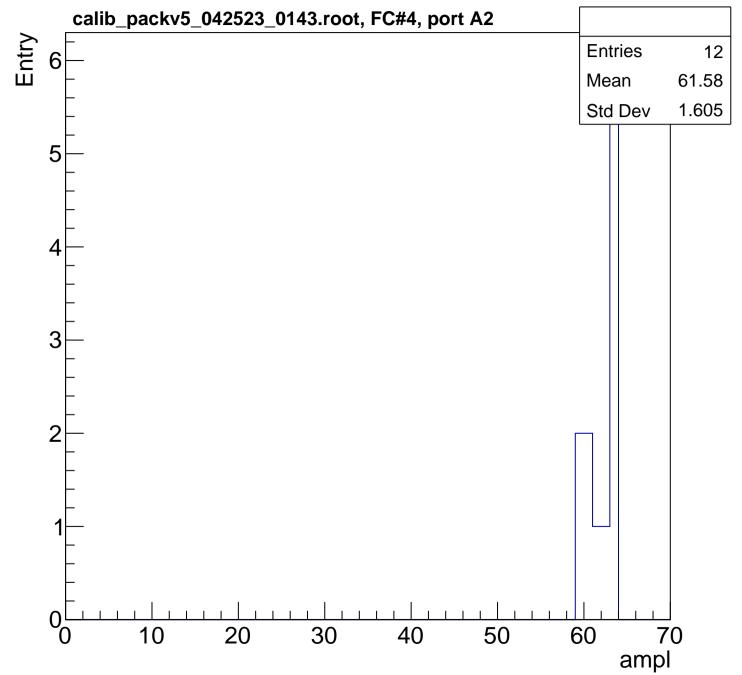










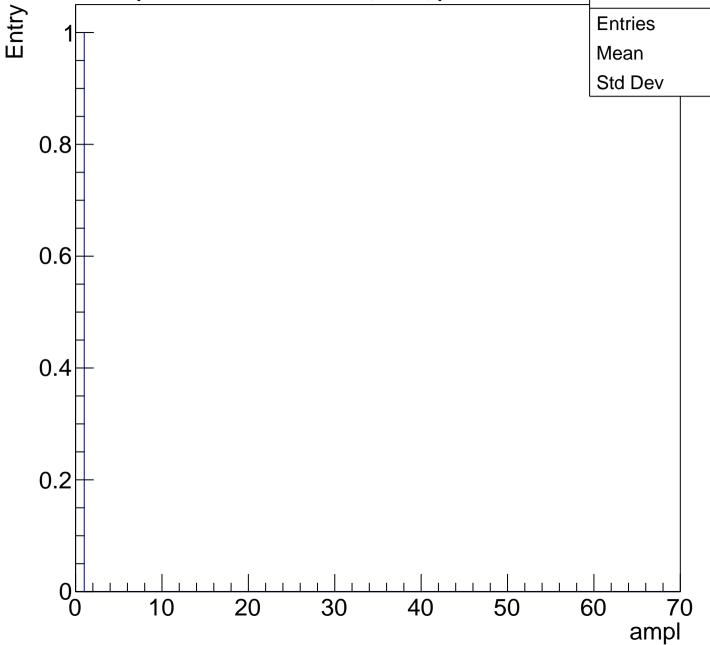


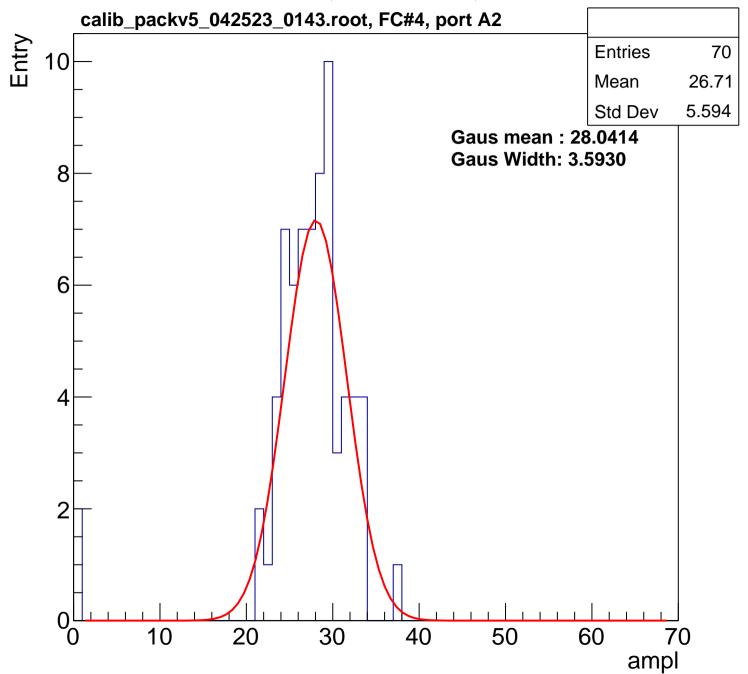
B1L100S, U3-ch34, adc7 calib_packv5_042523_0143.root, FC#4, port A2 **Entries** Mean

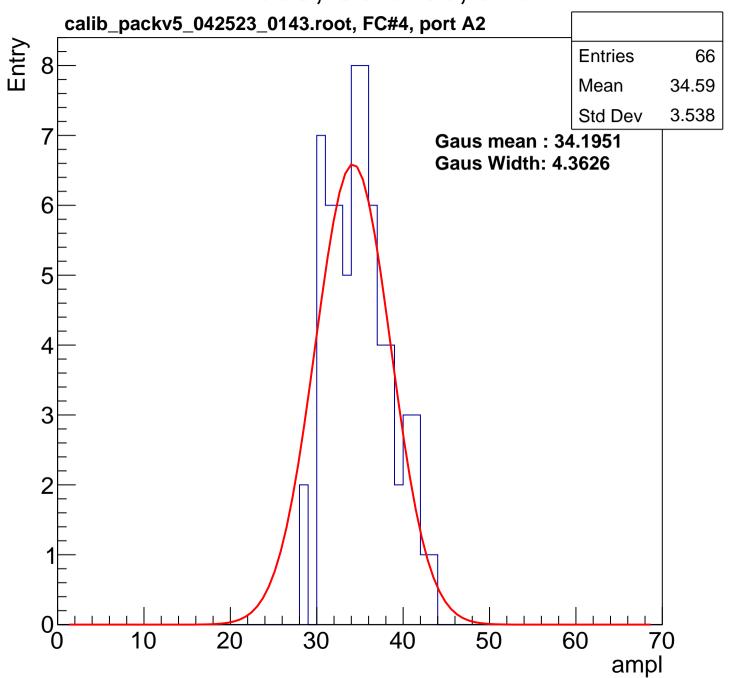
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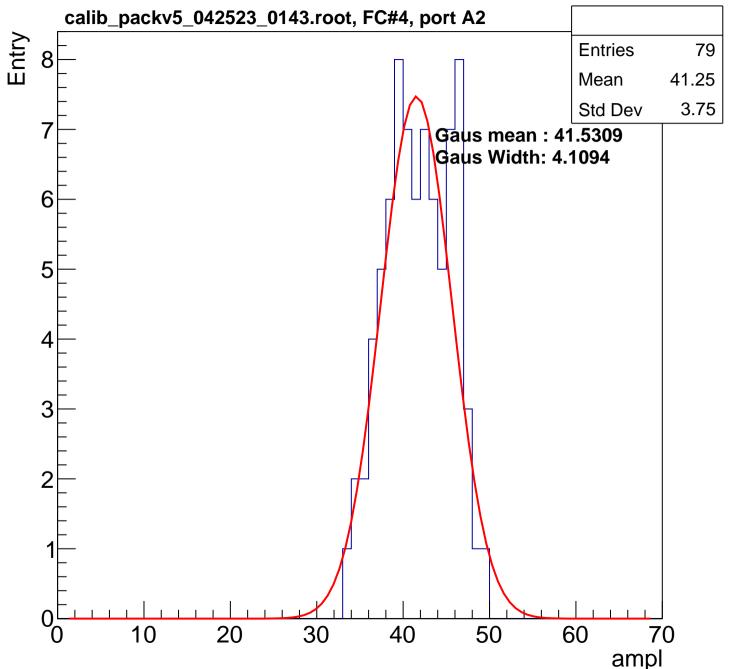
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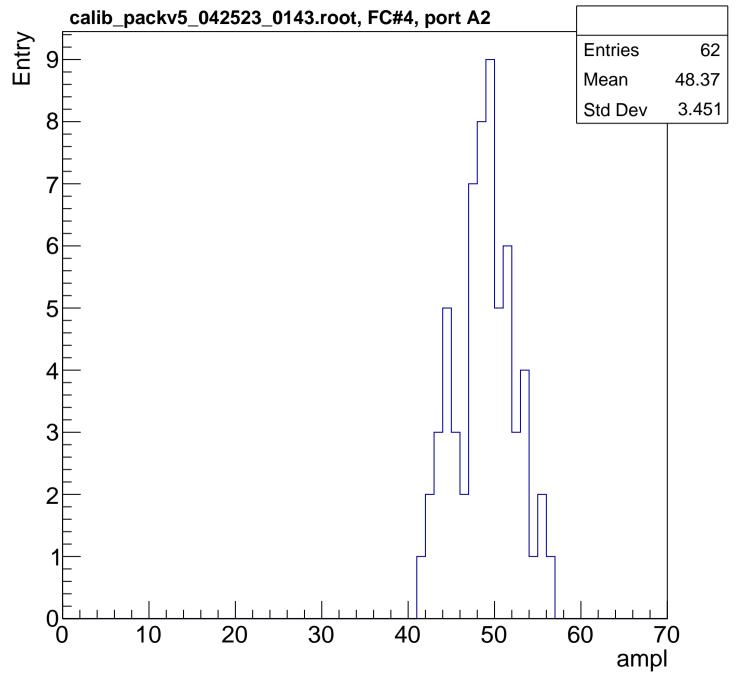
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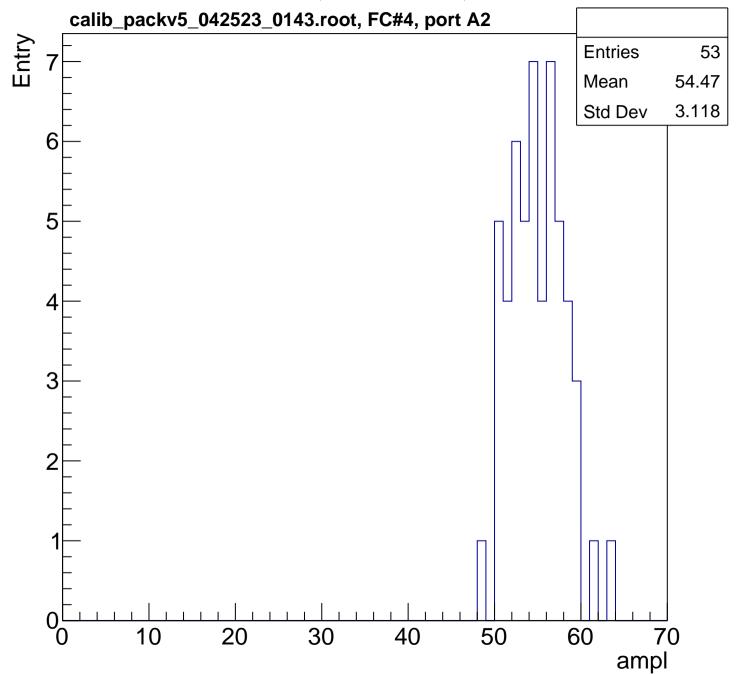


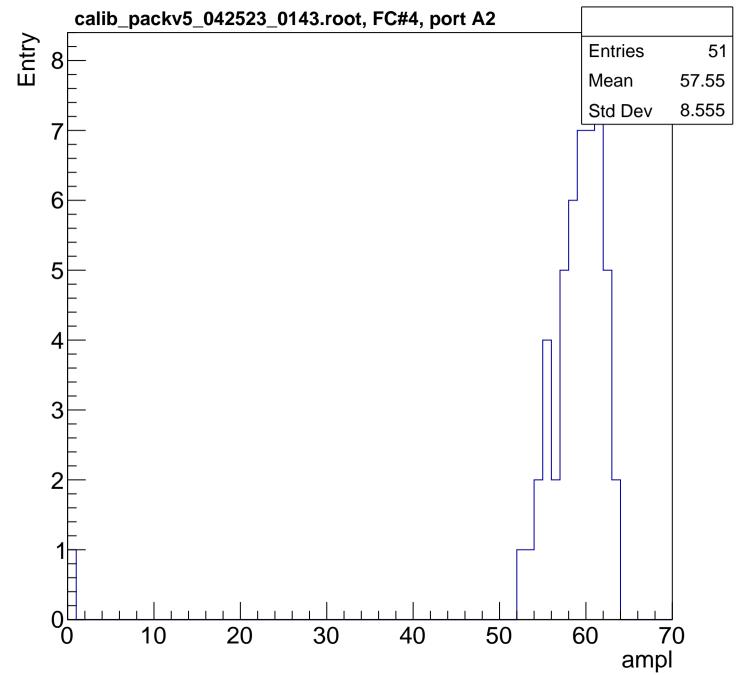


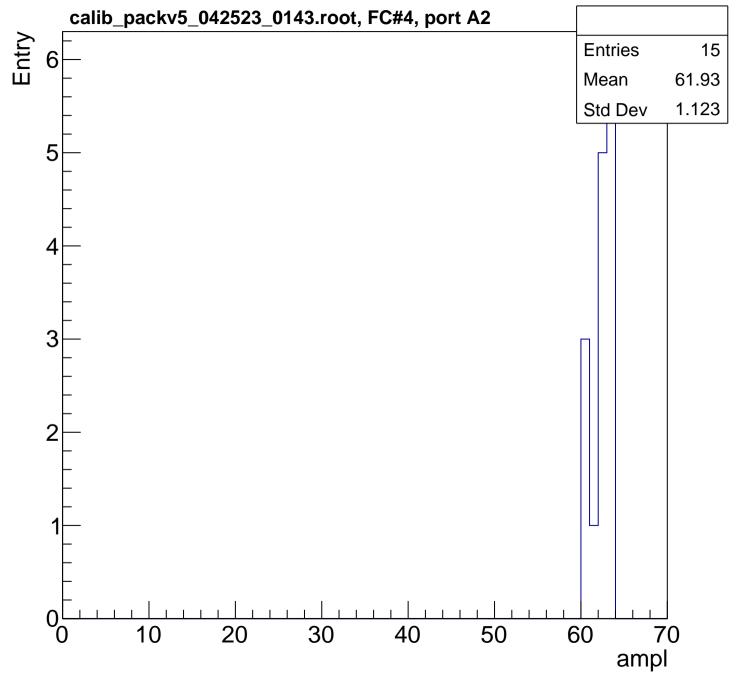


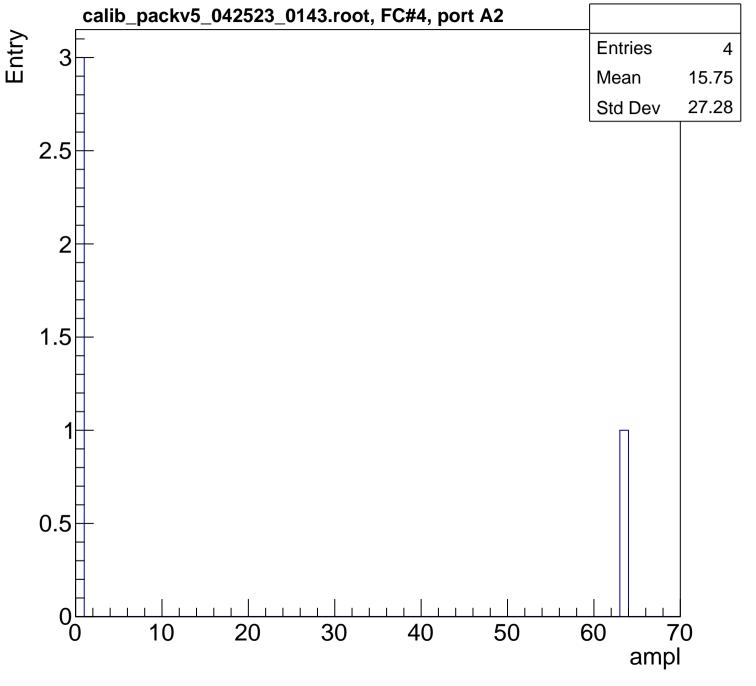


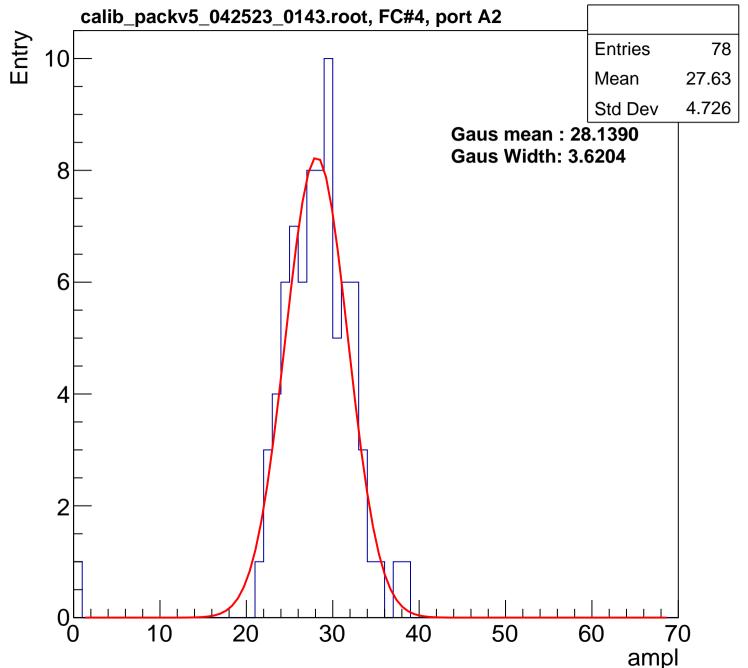


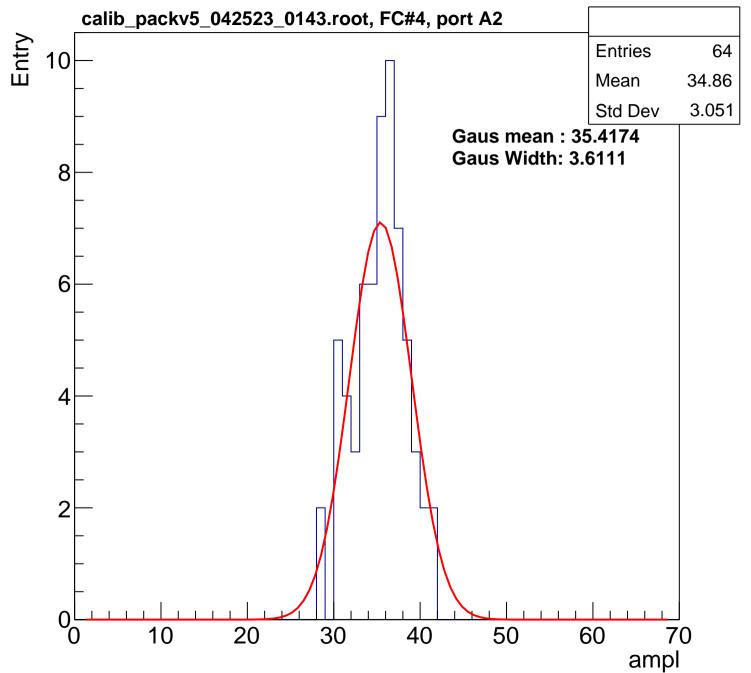


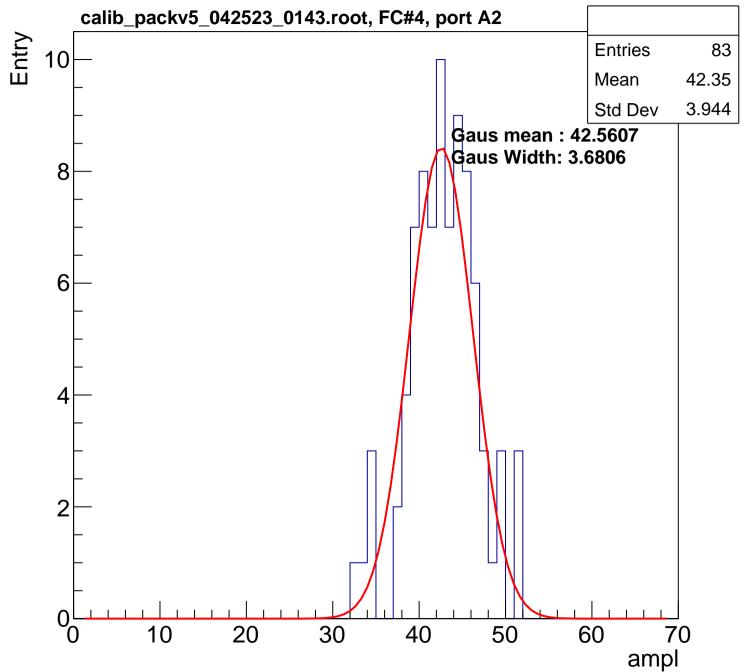


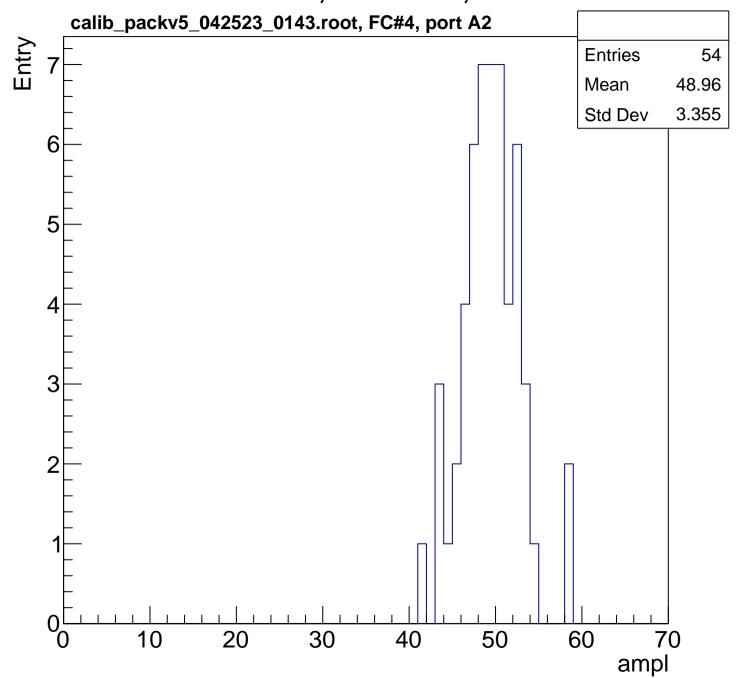


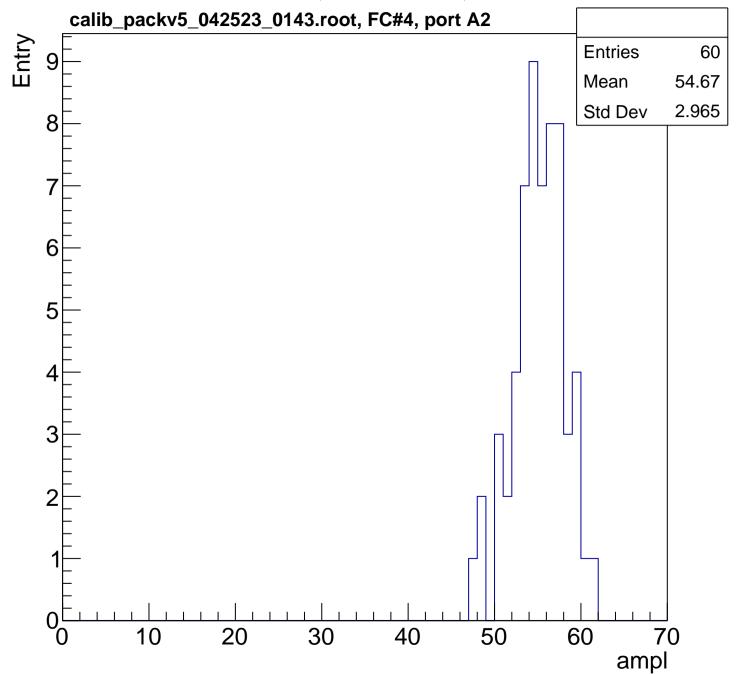


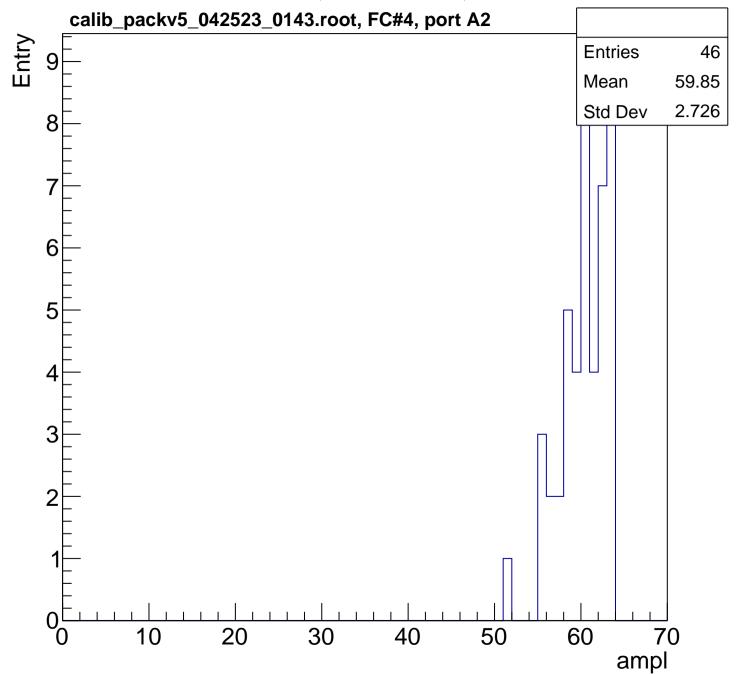


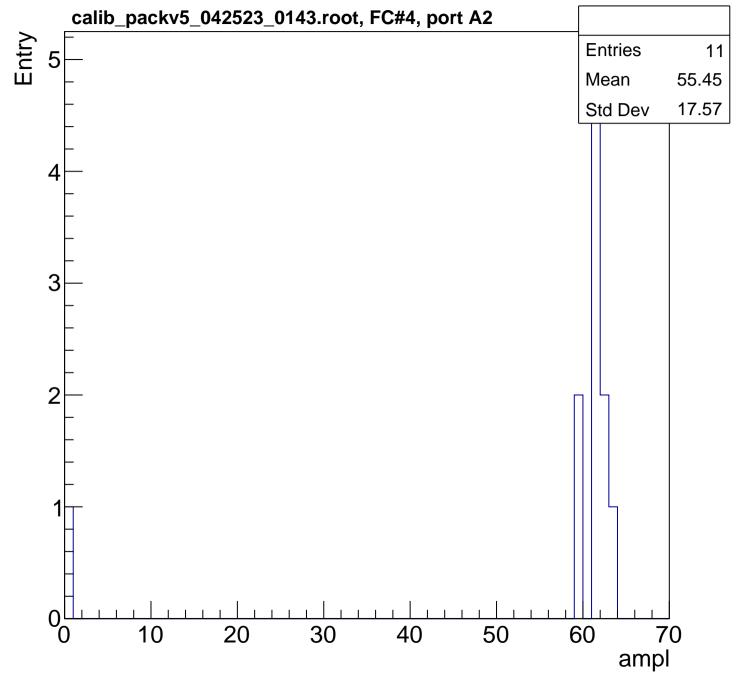


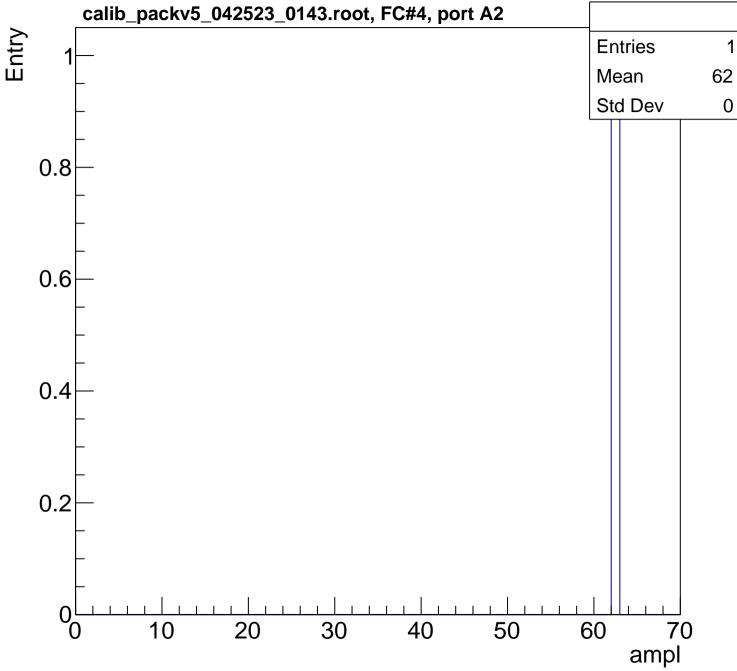


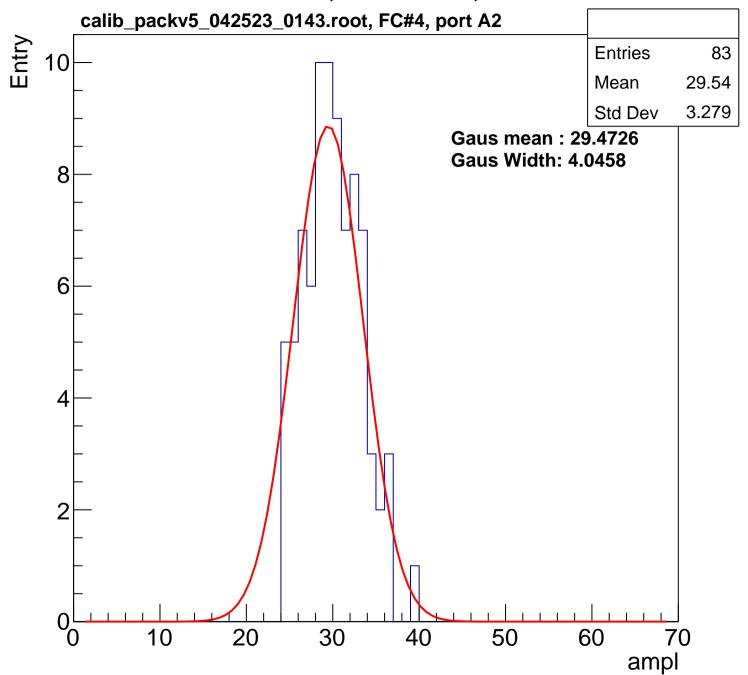


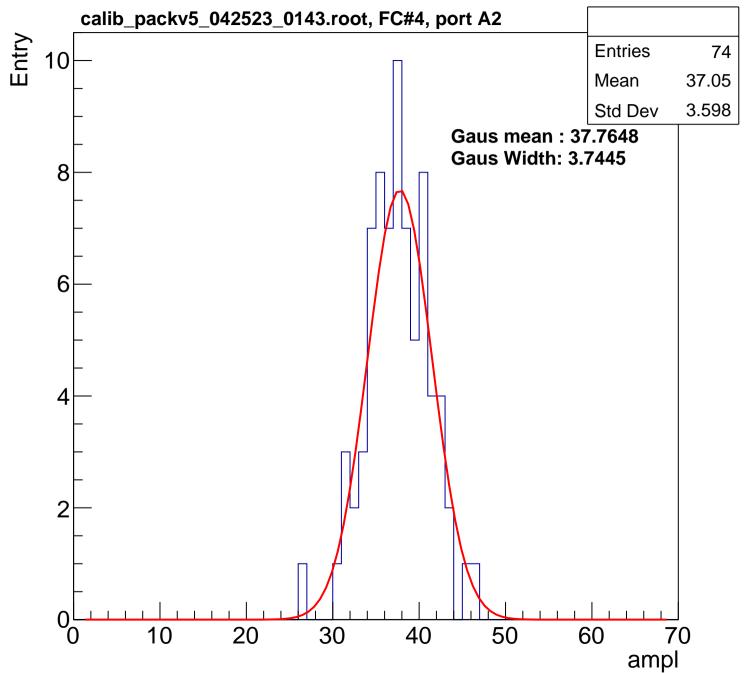


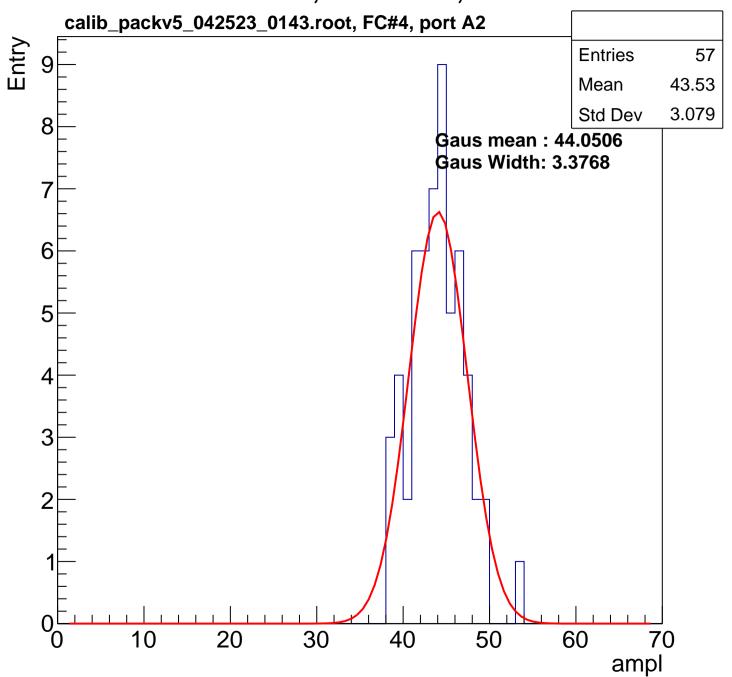


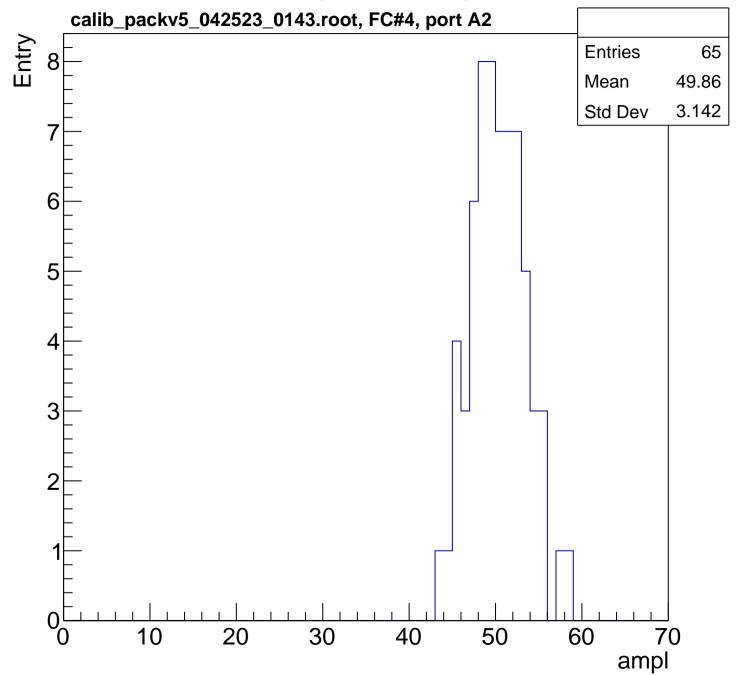


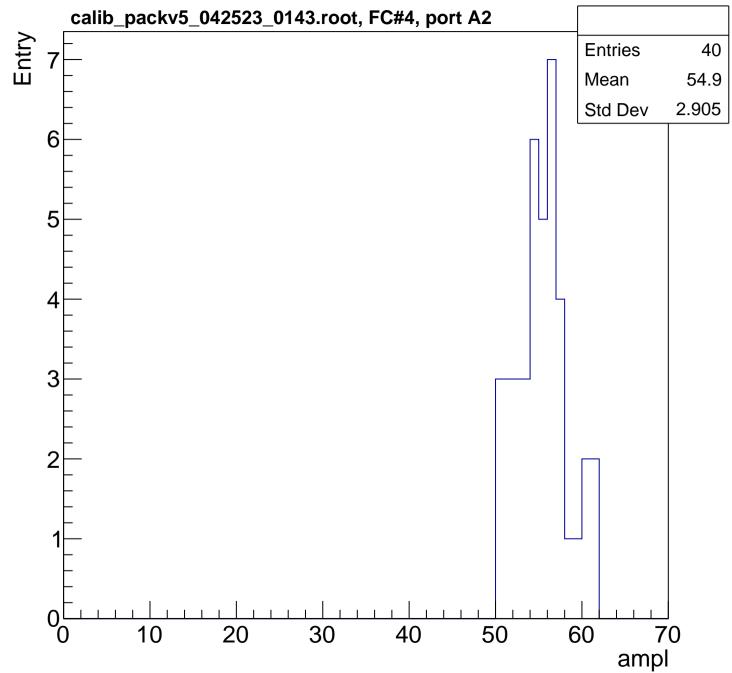


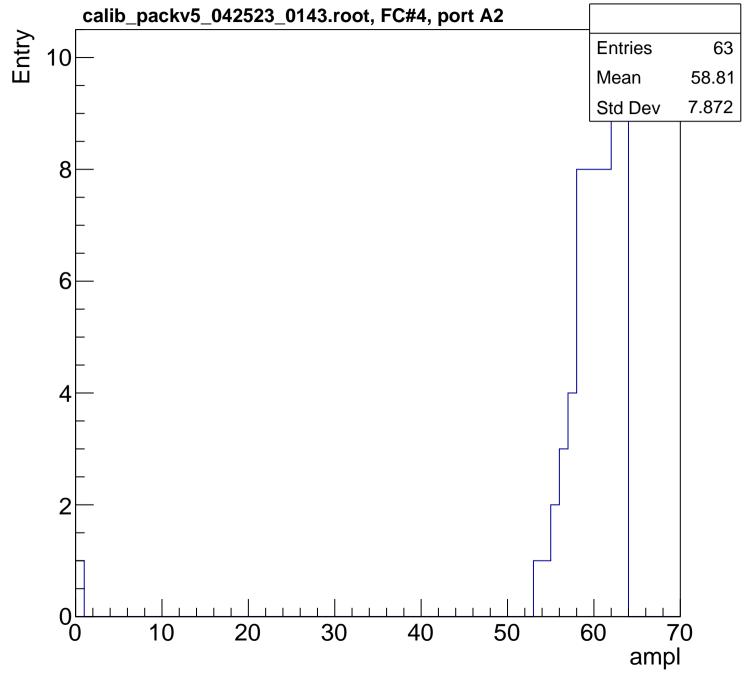


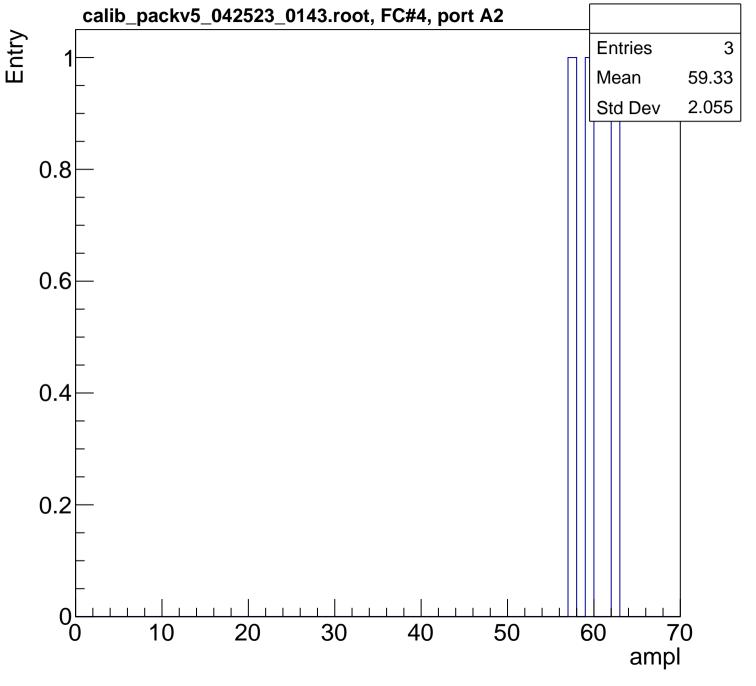


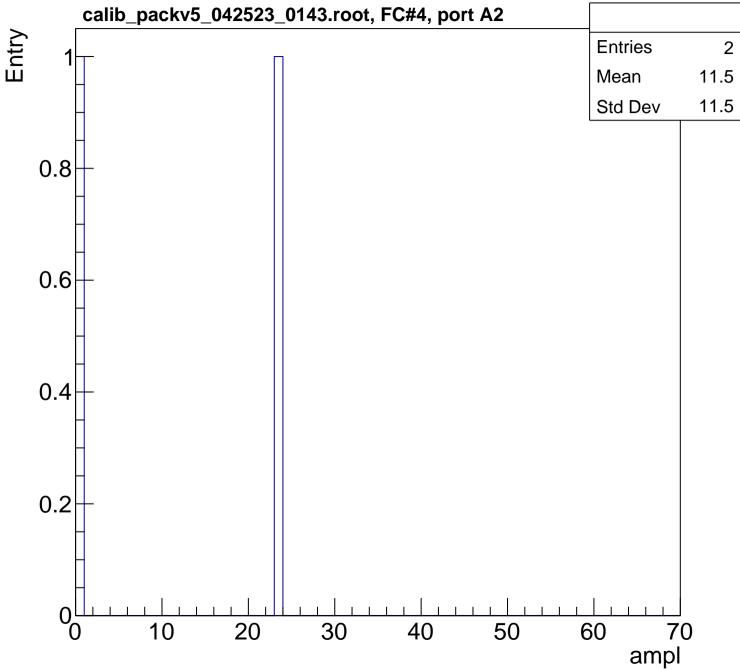


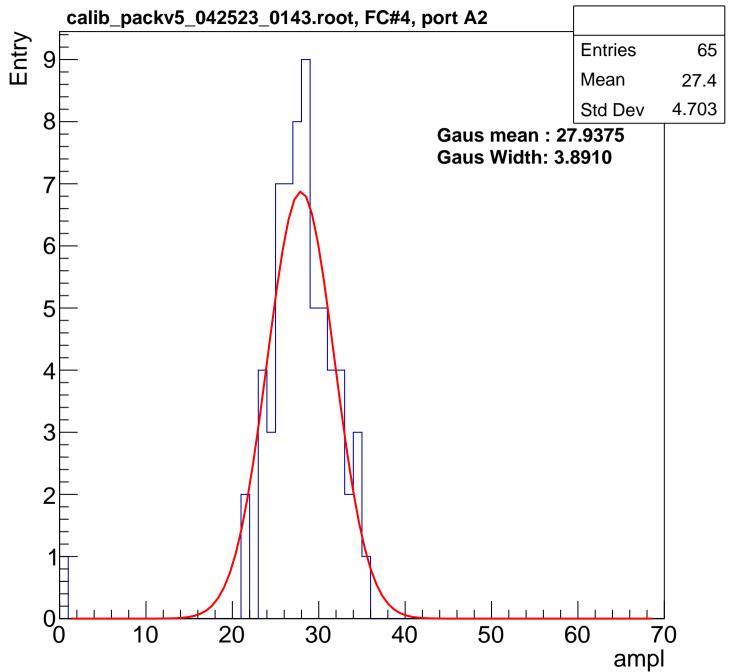


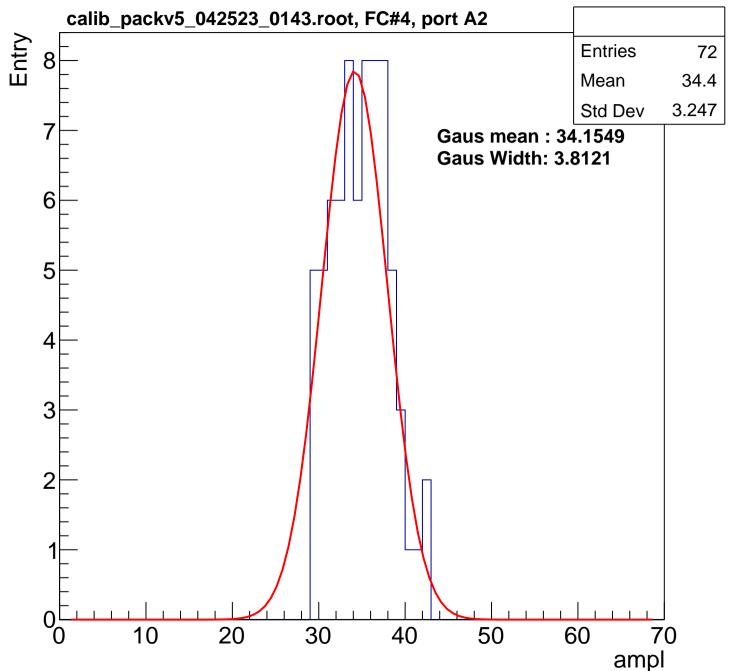


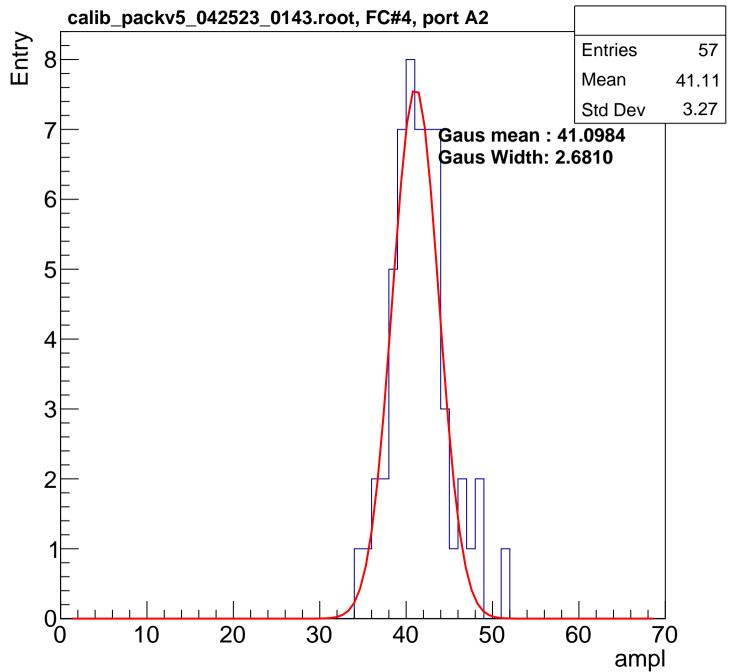


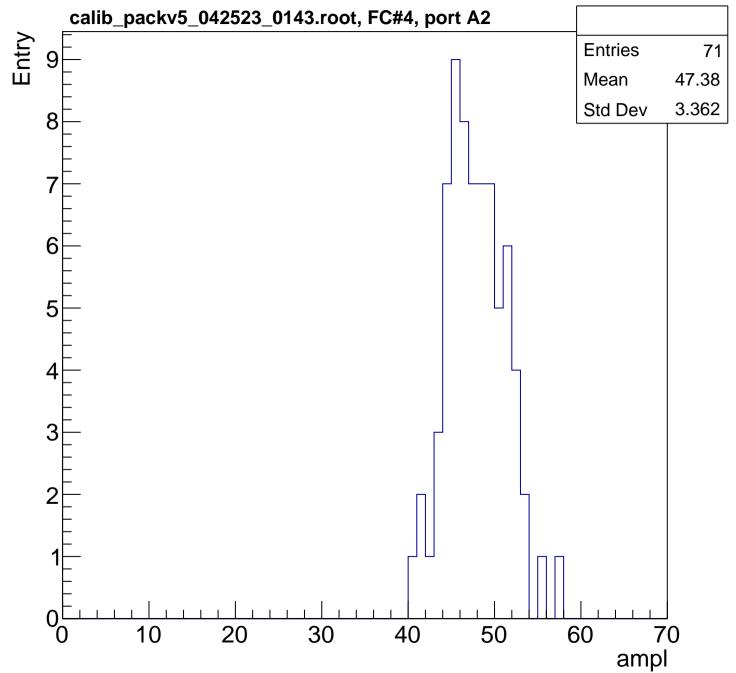


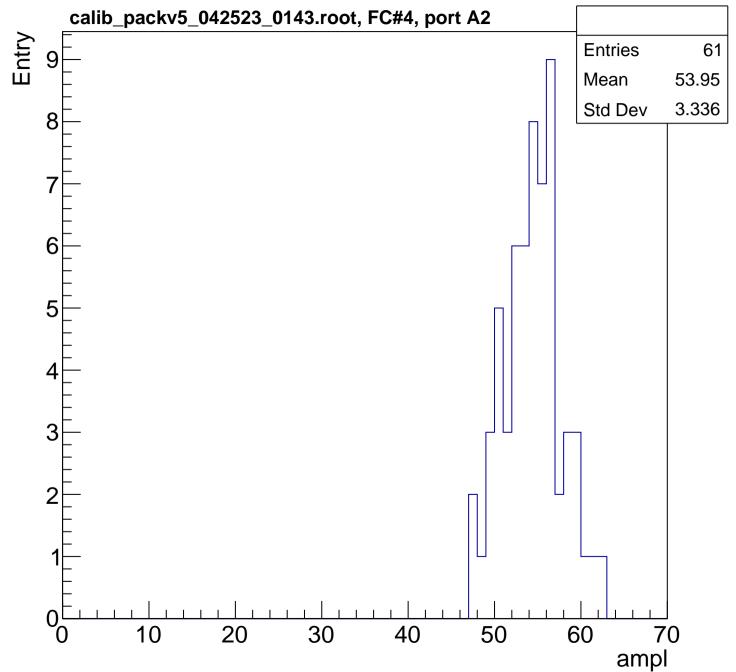


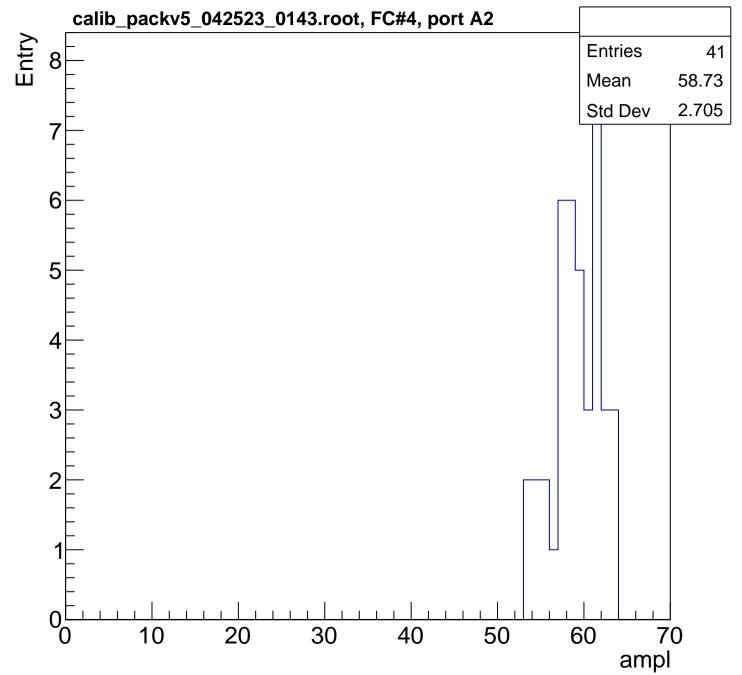


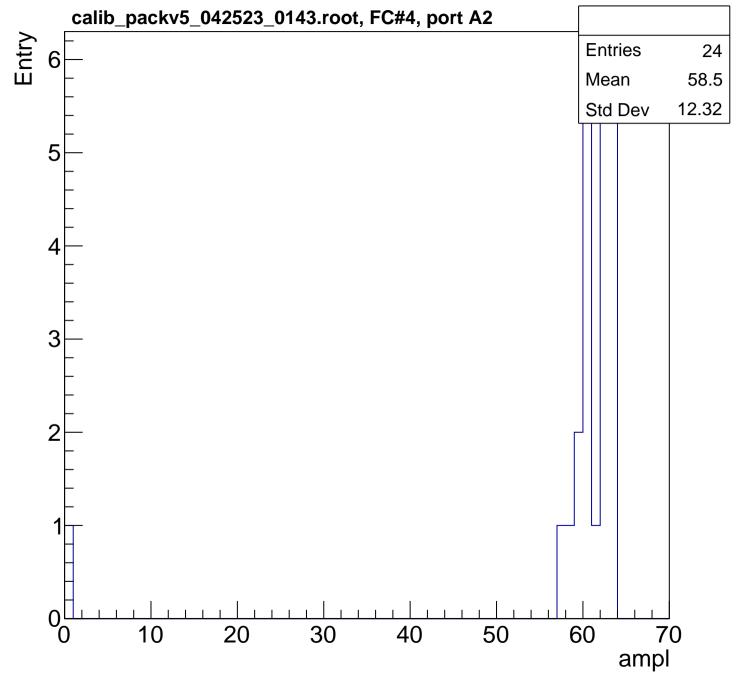


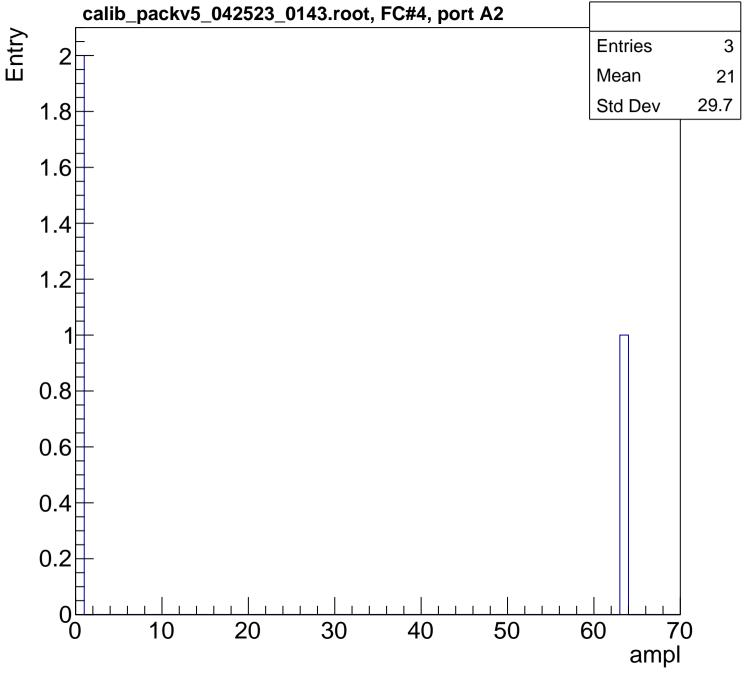


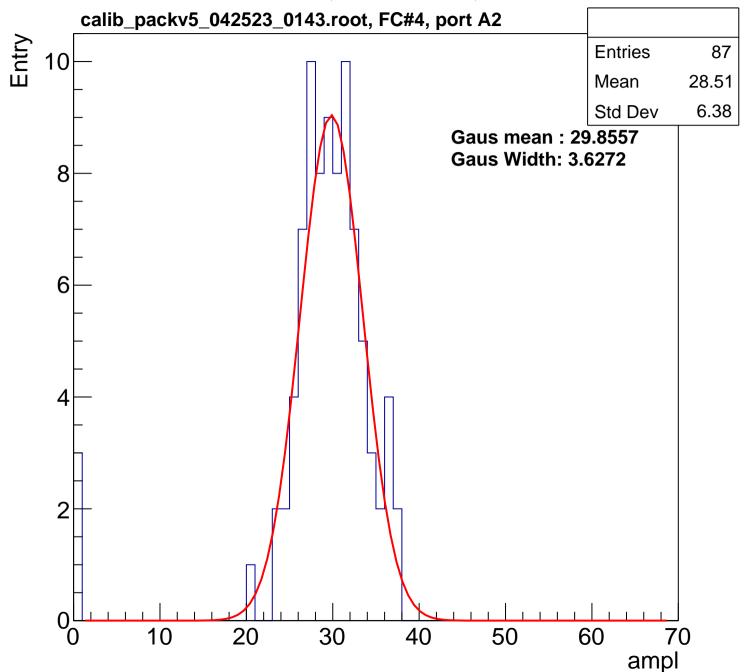


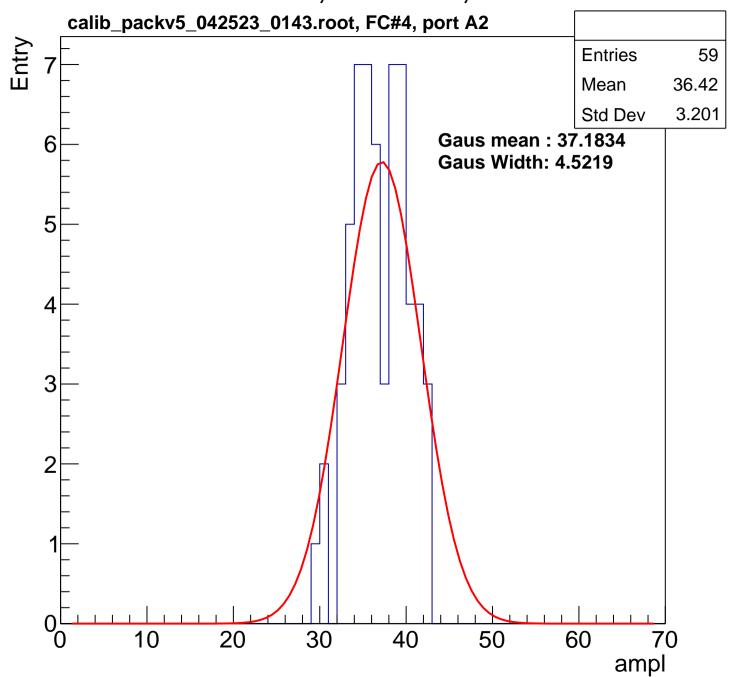


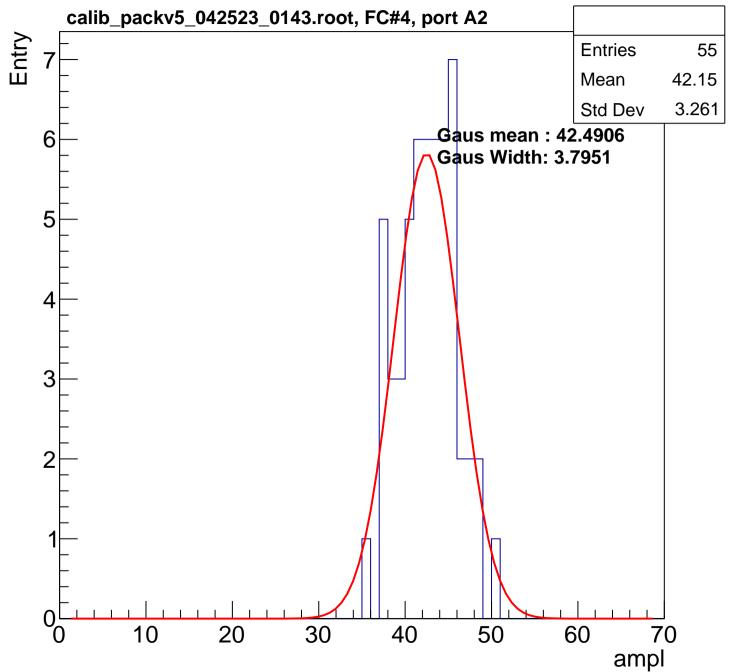


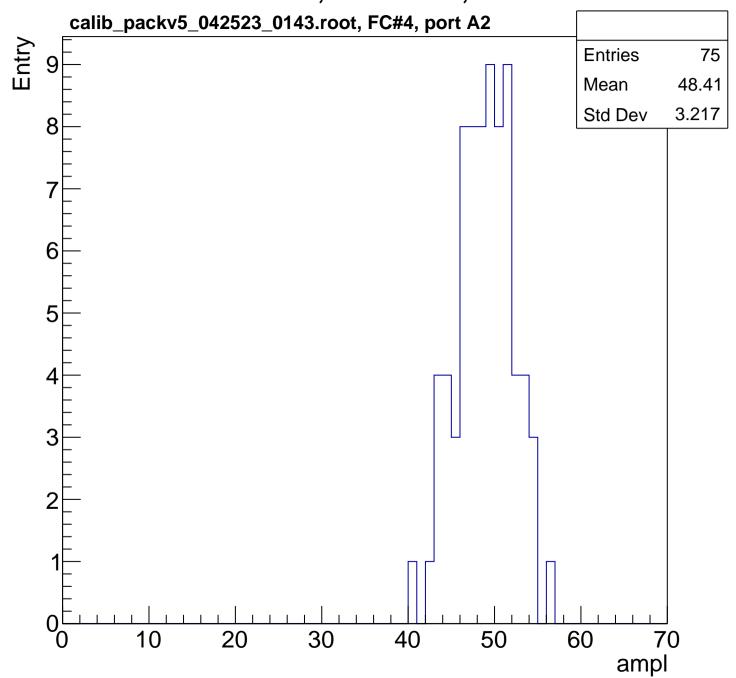


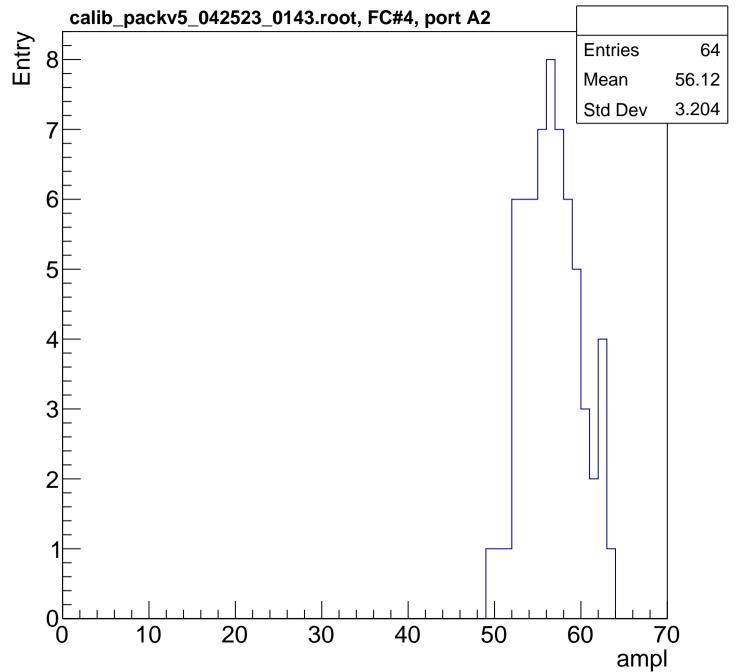


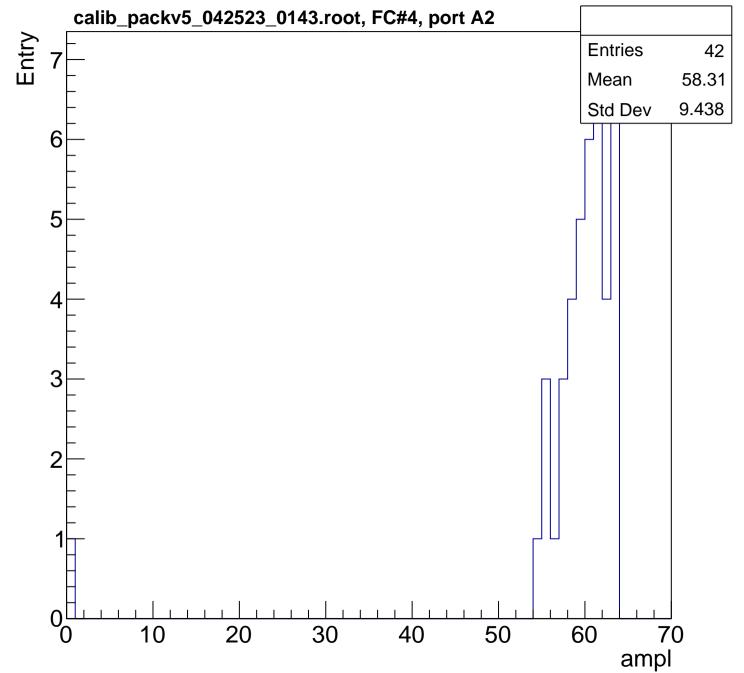


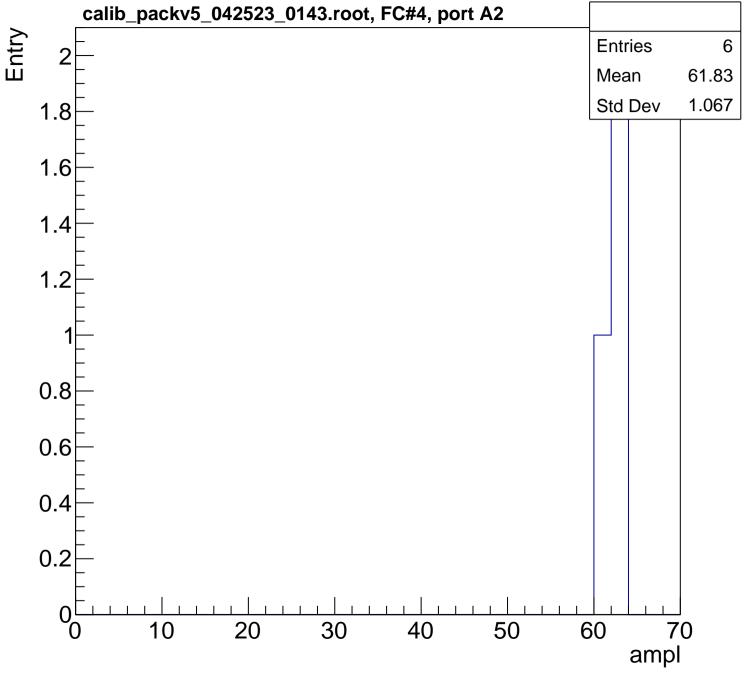


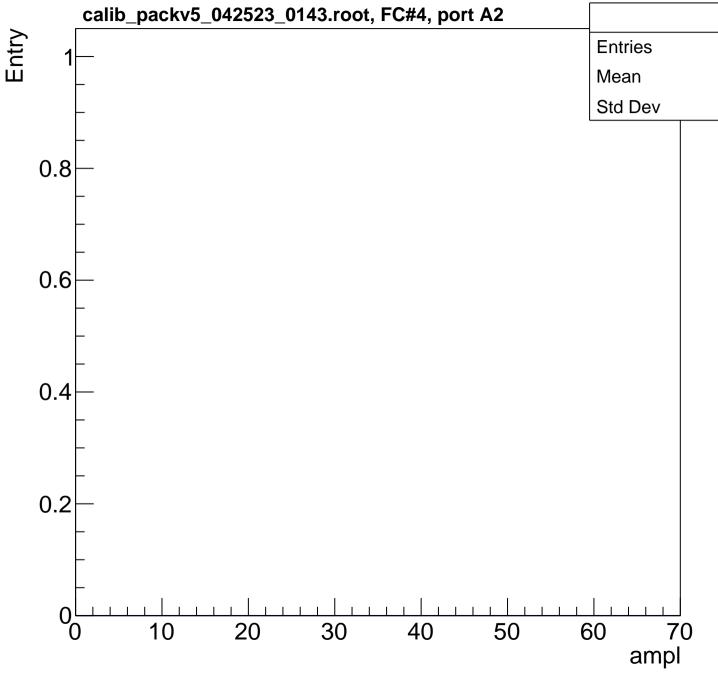


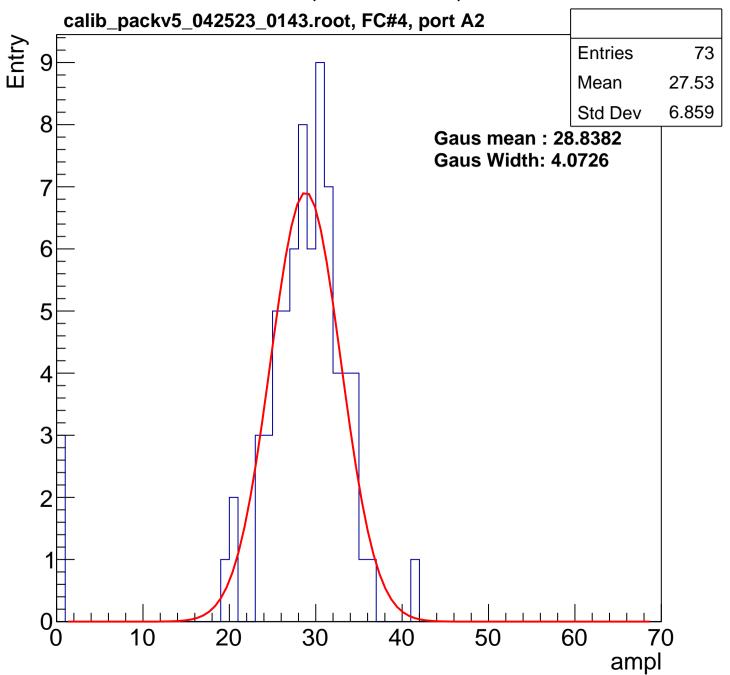


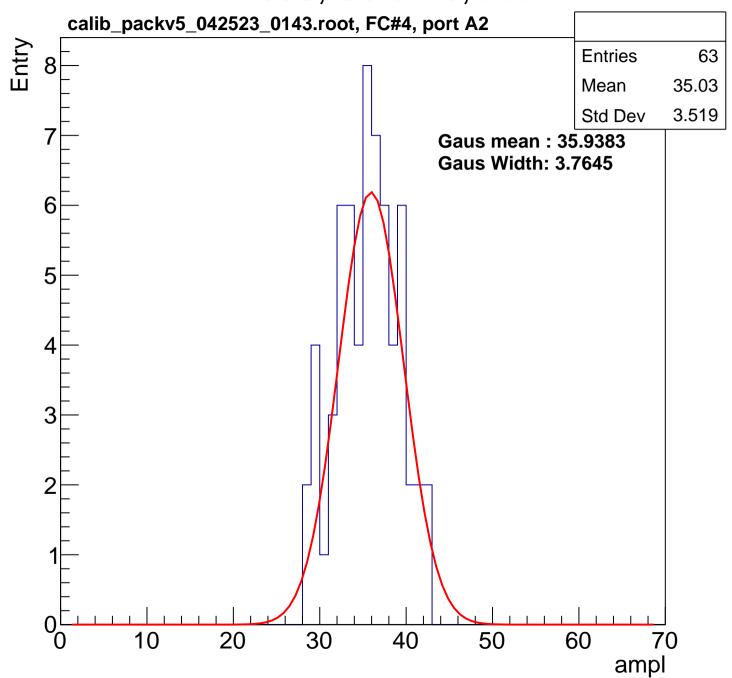


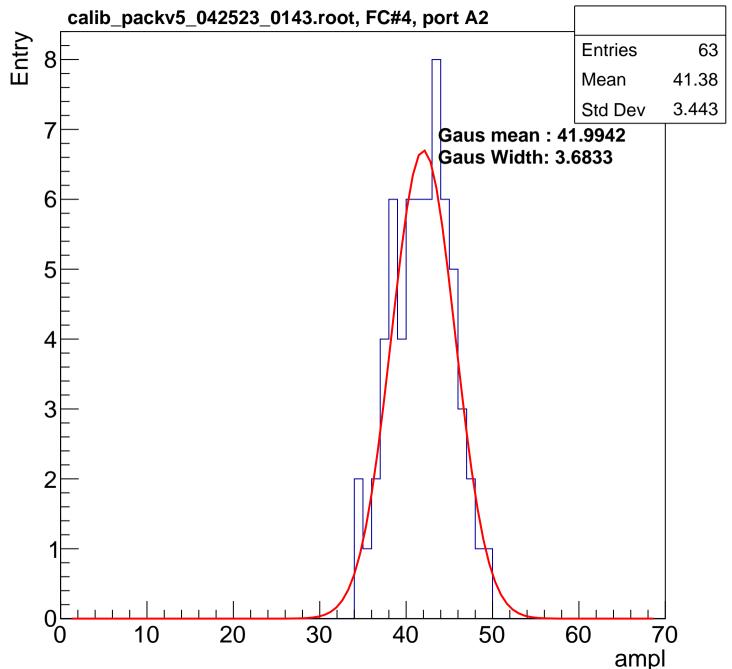


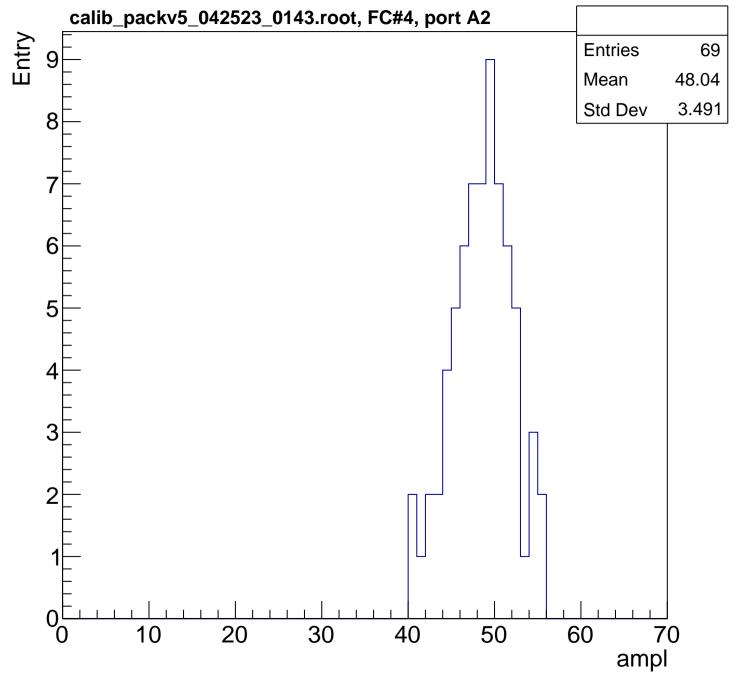


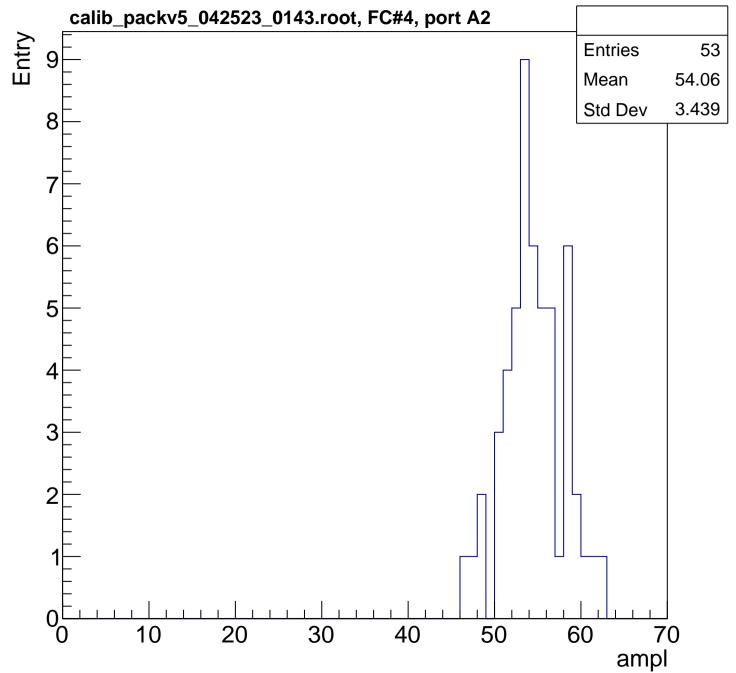


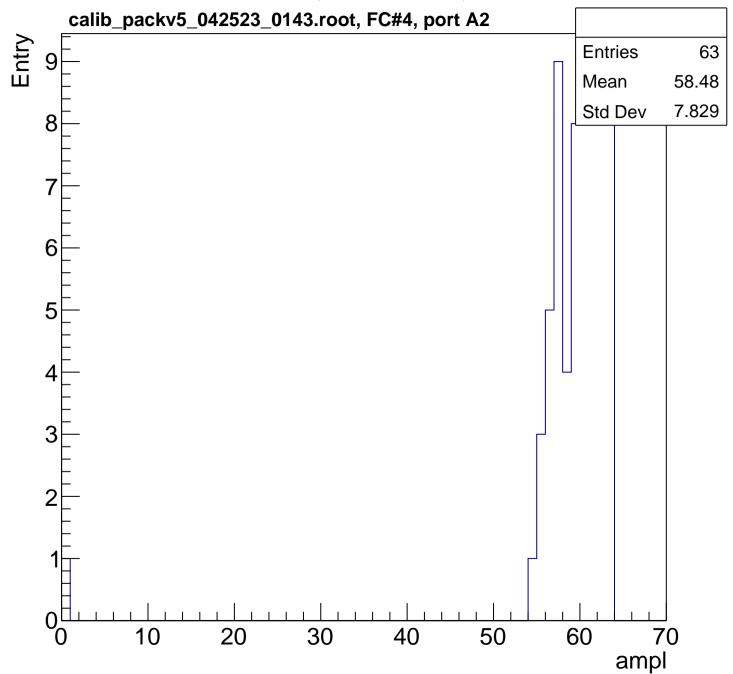


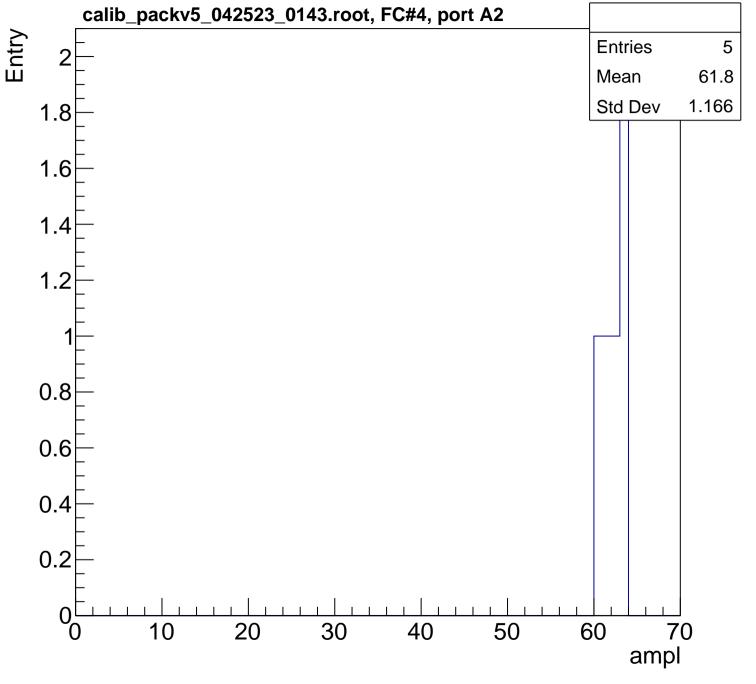




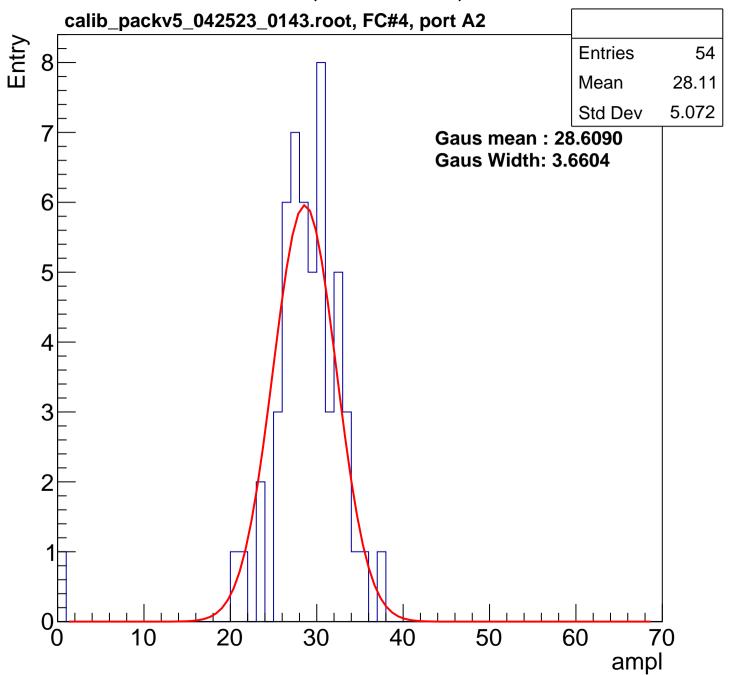


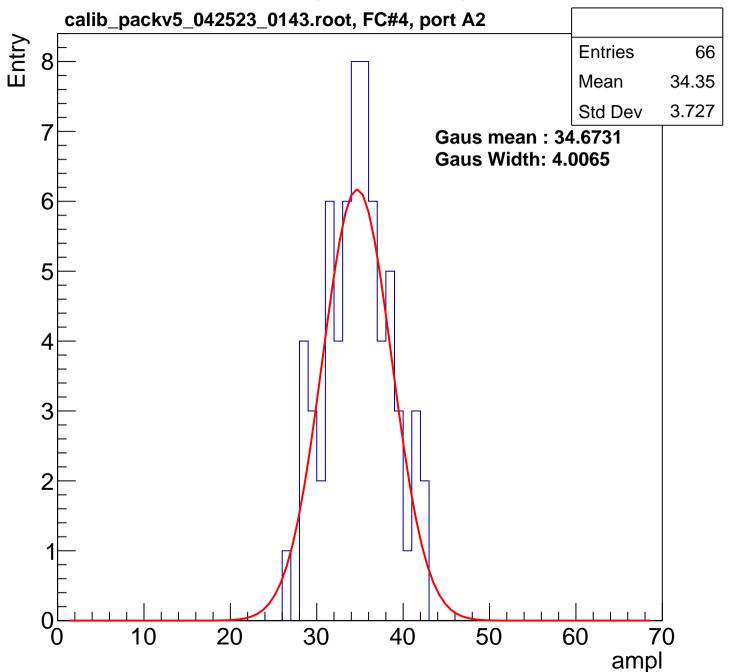


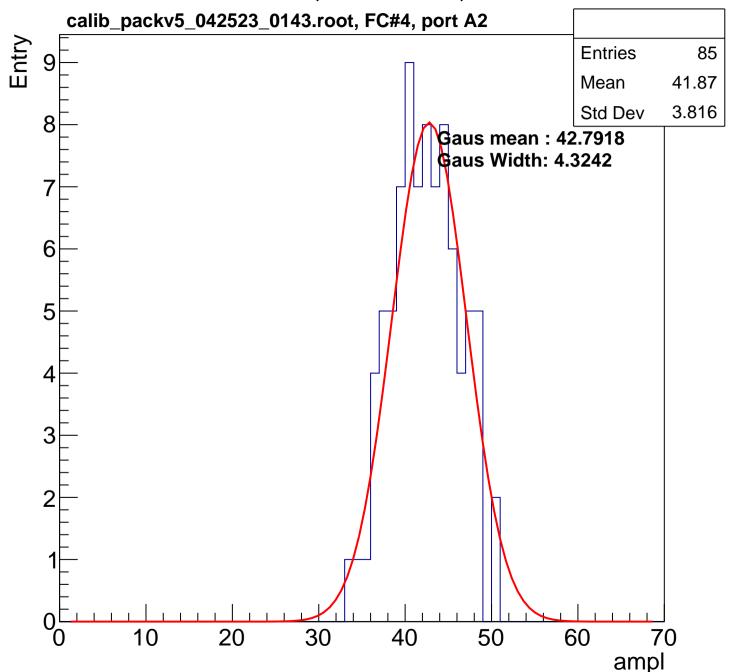


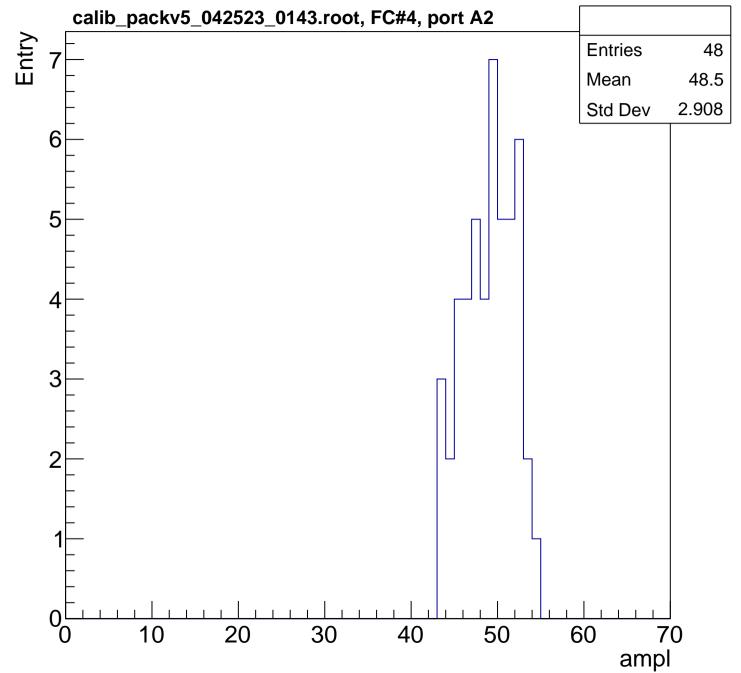


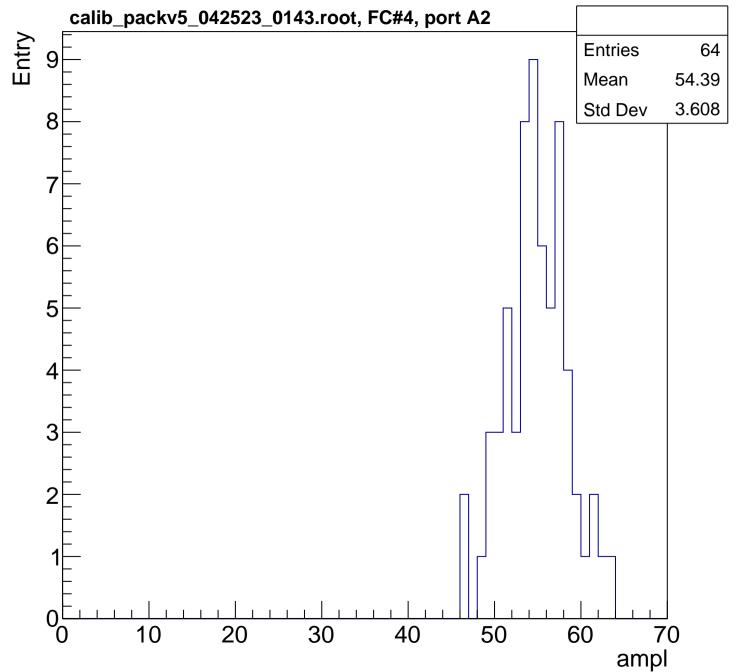
B1L100S, U3-ch40, adc7 calib_packv5_042523_0143.root, FC#4, port A2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

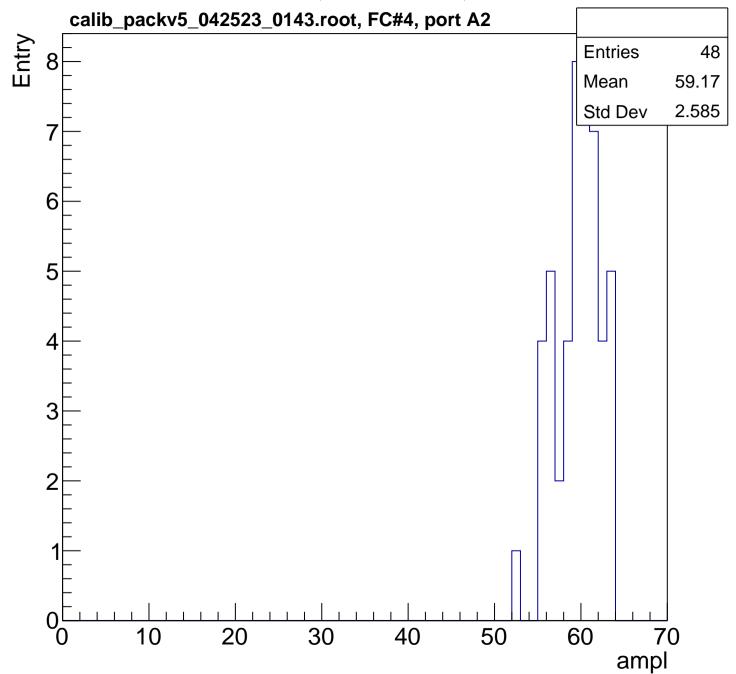


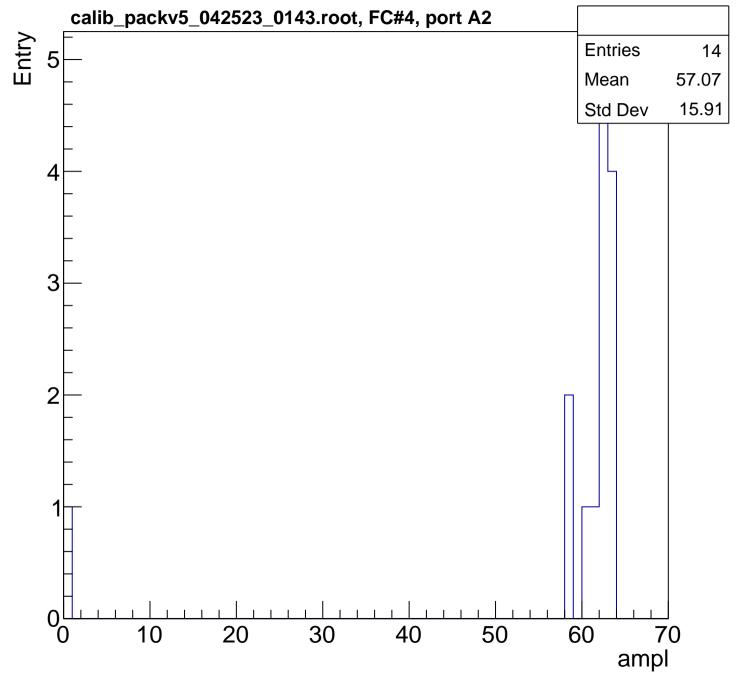




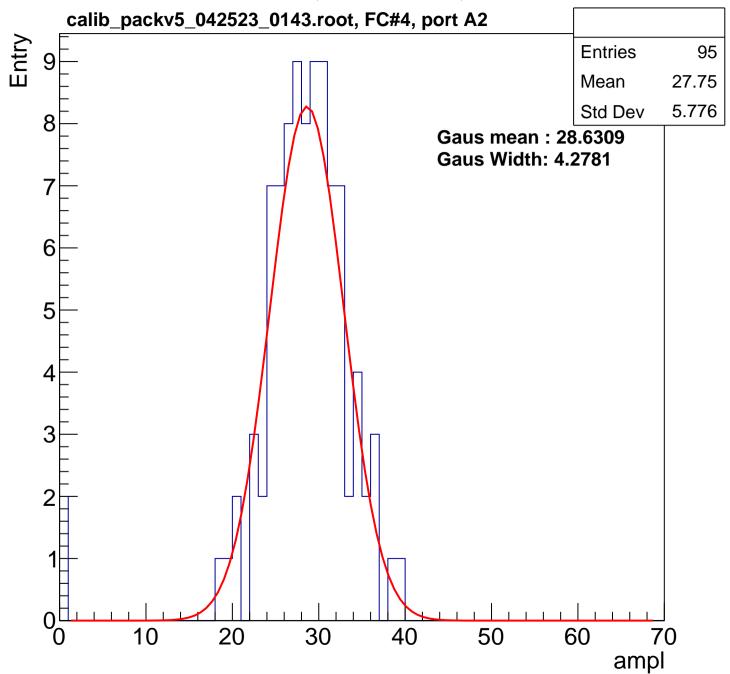


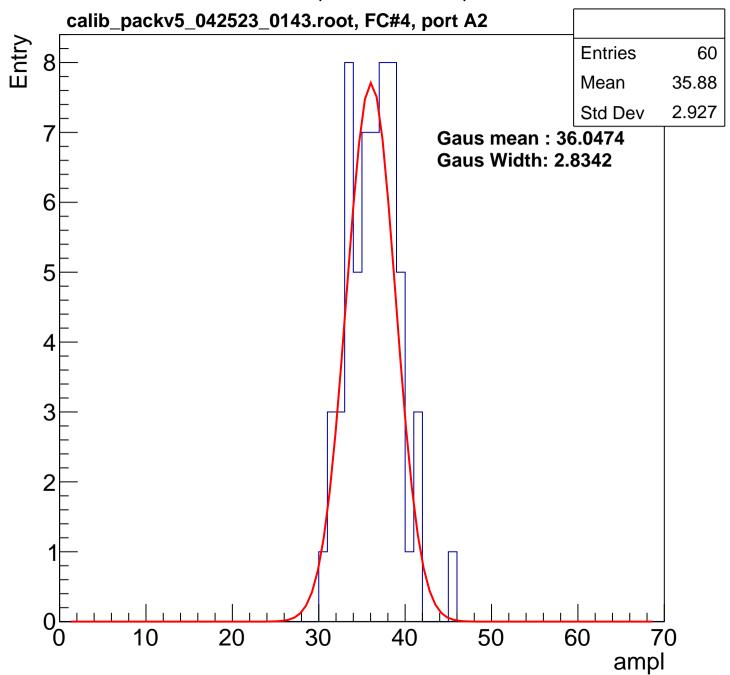


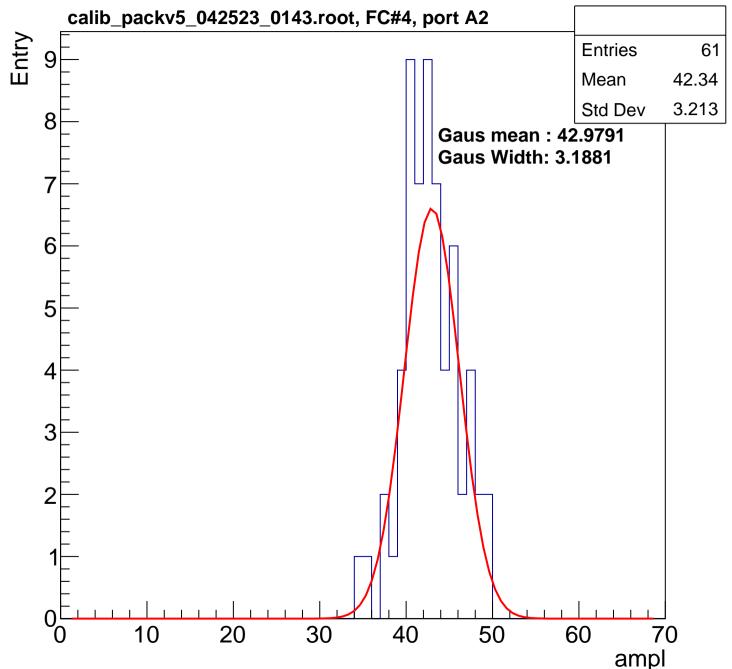


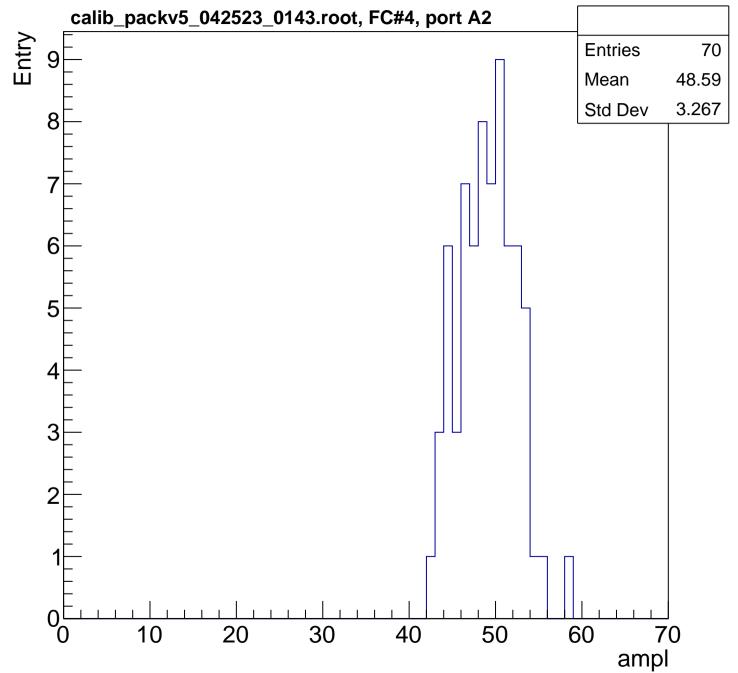


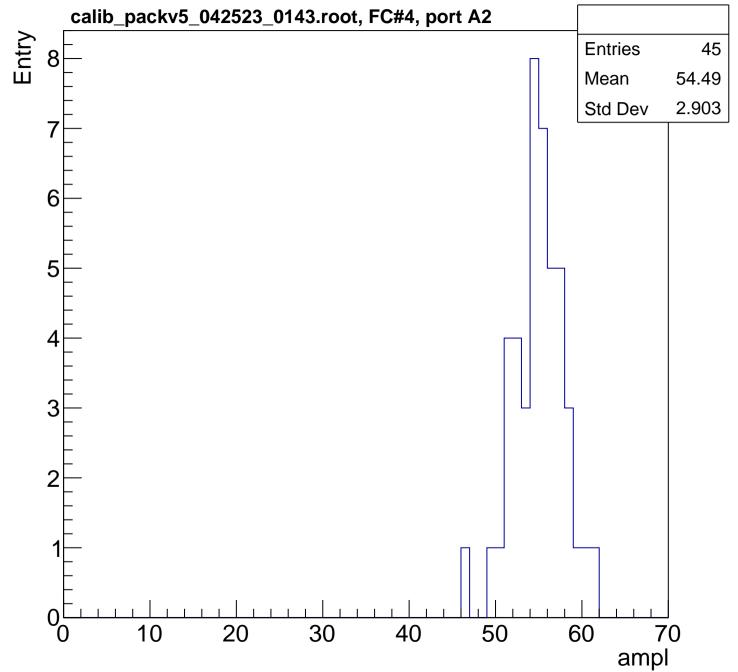


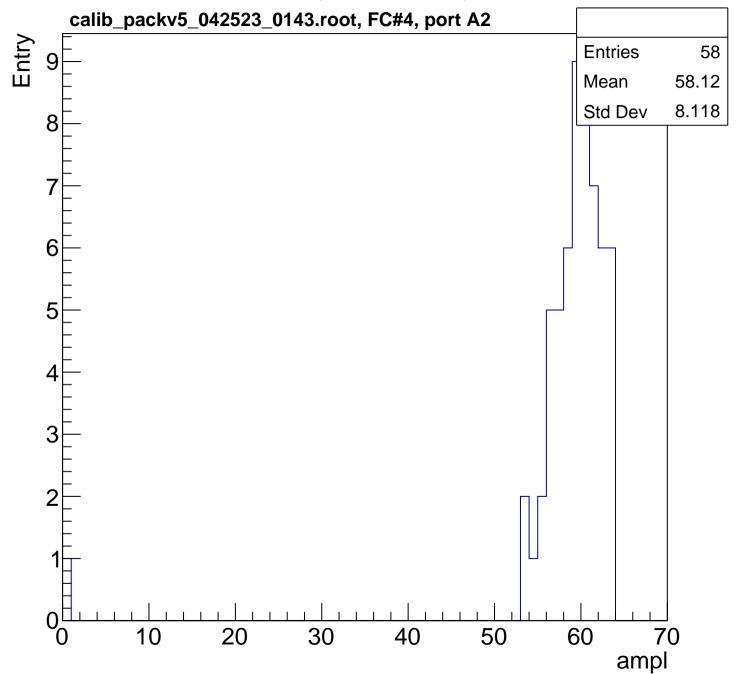


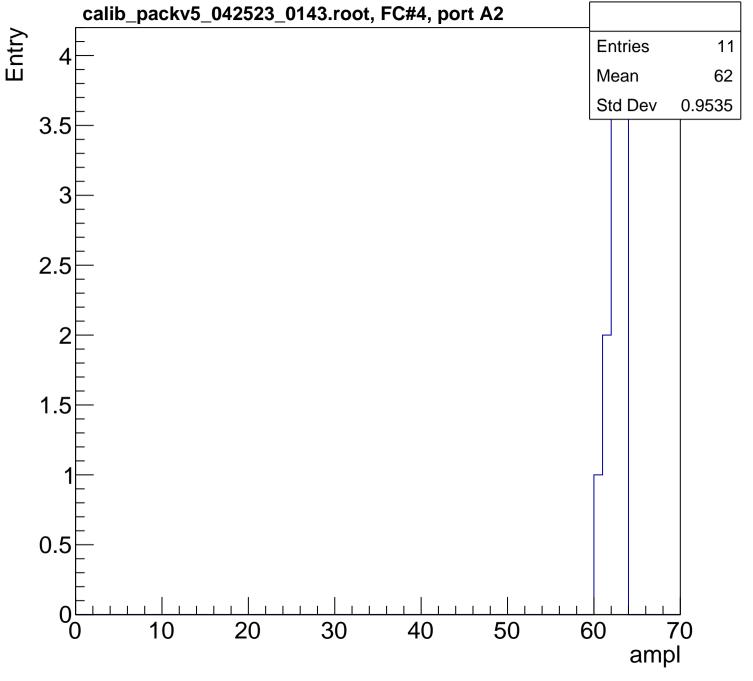




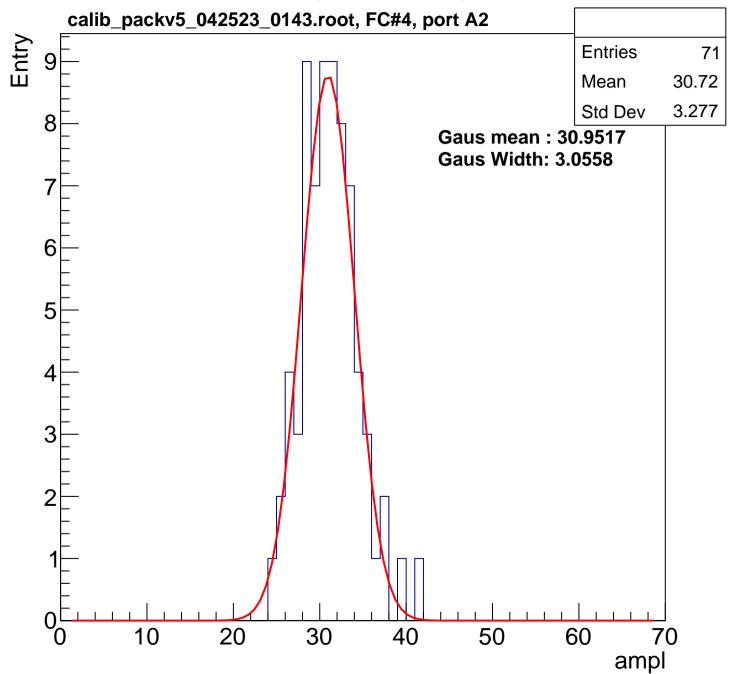


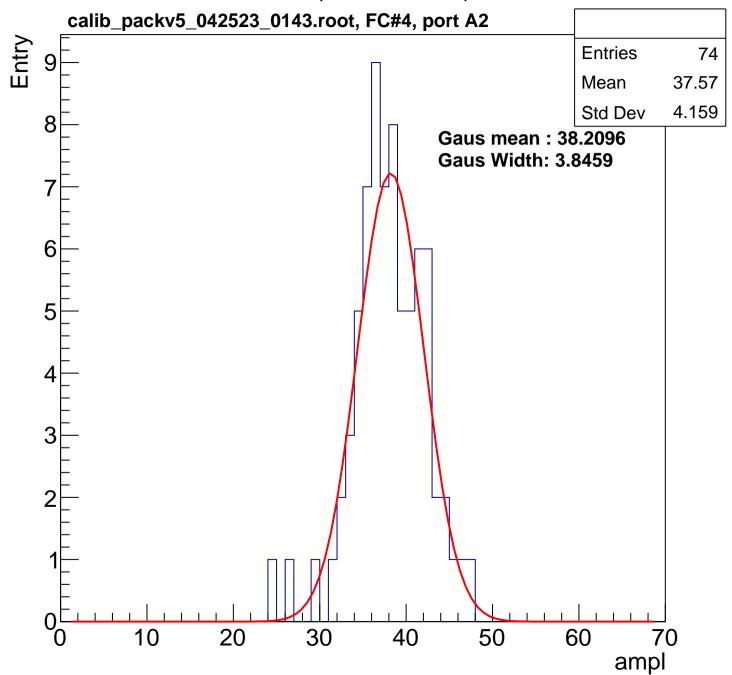


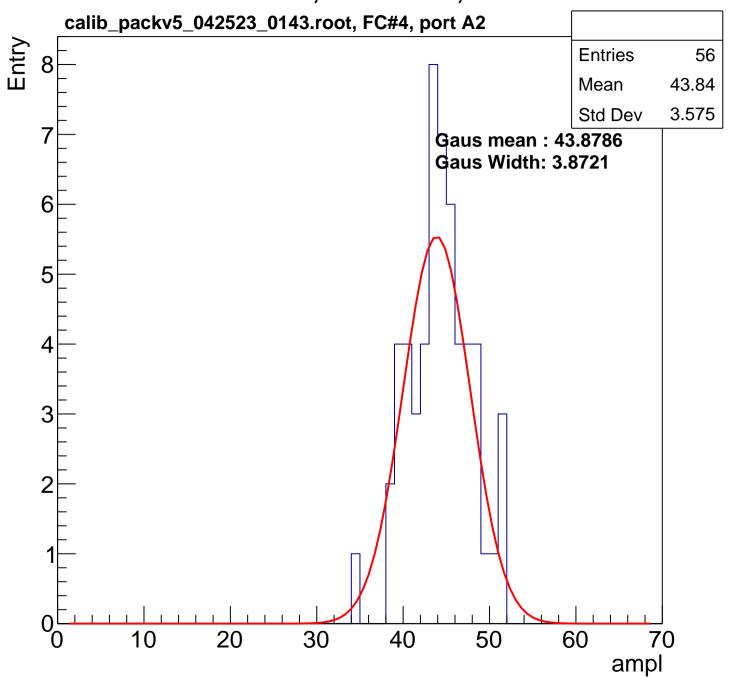


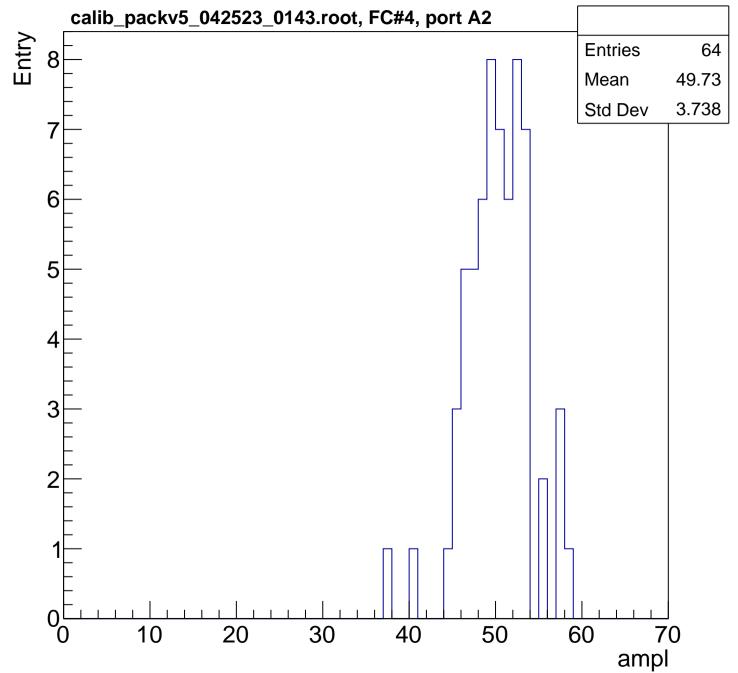


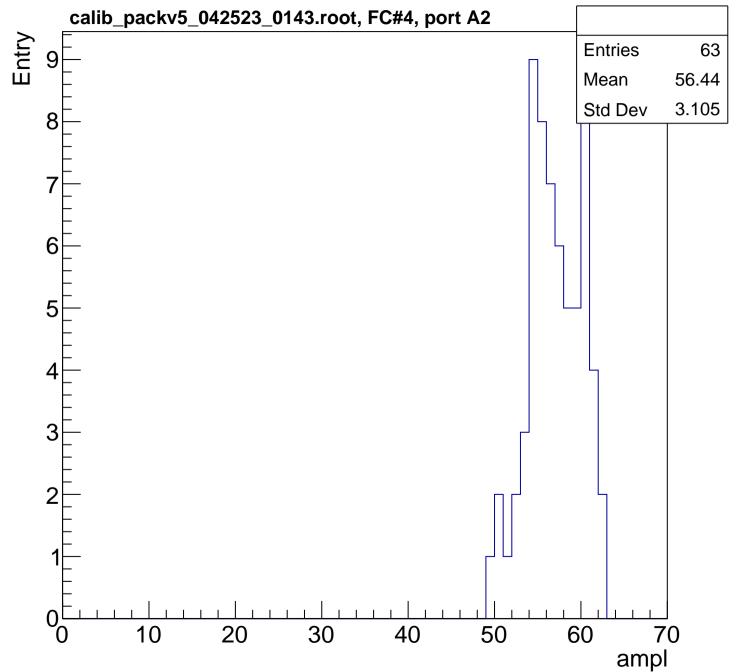


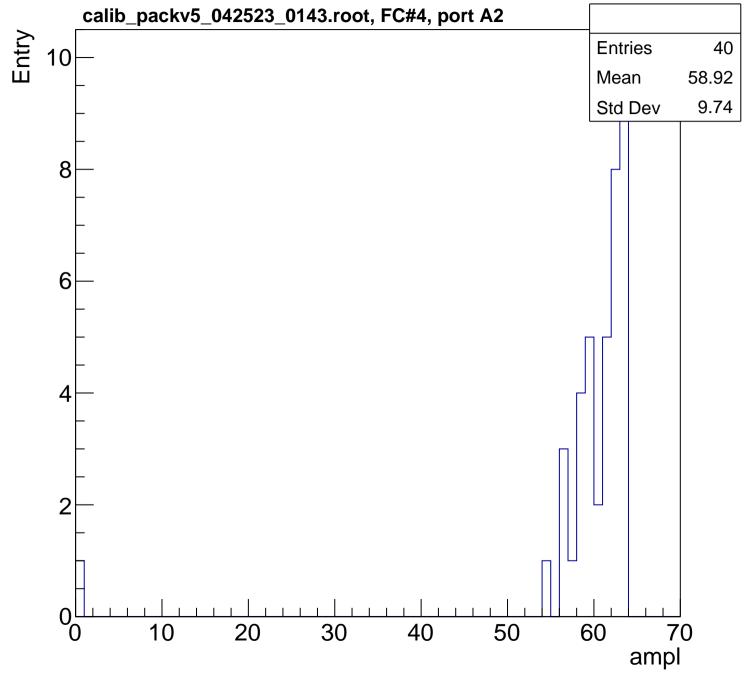


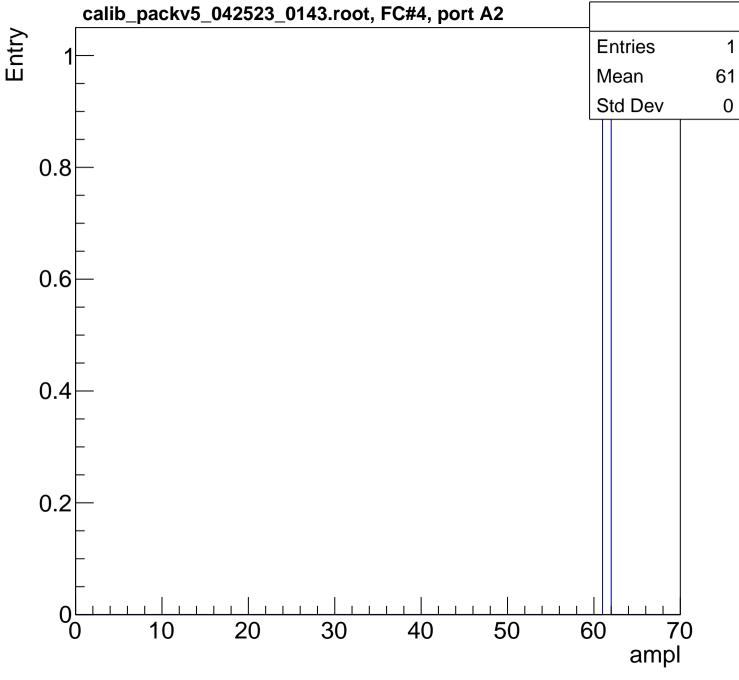


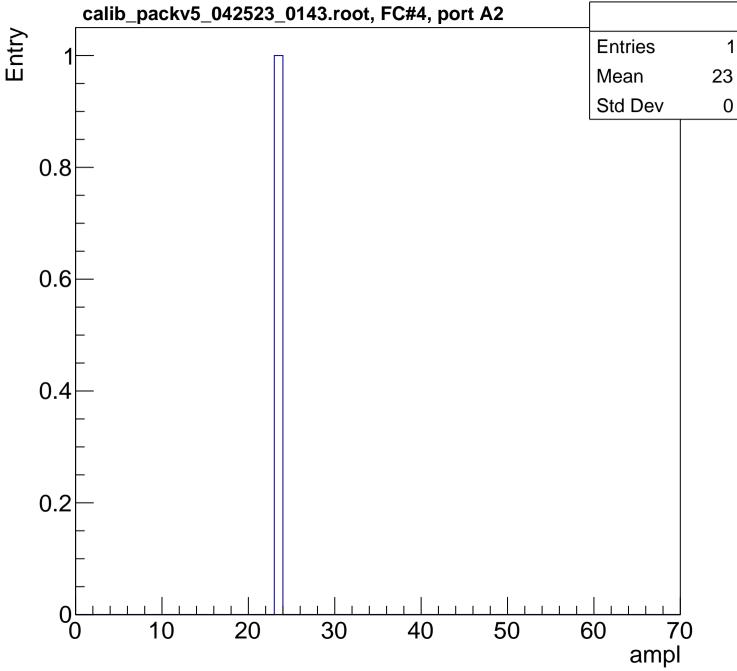


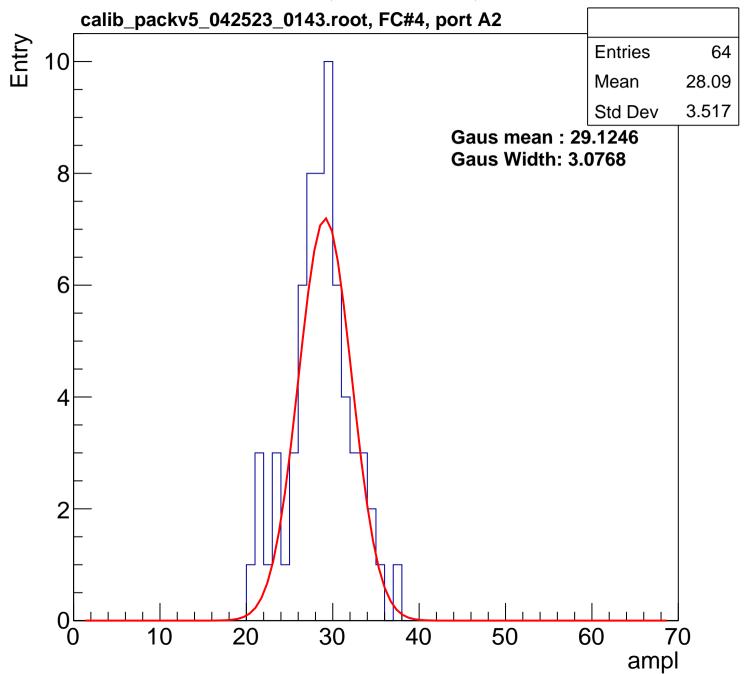


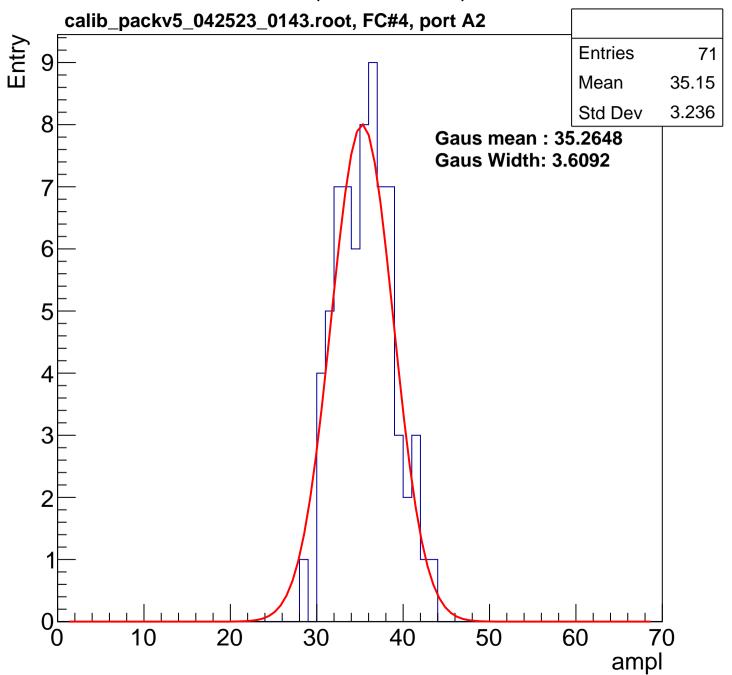


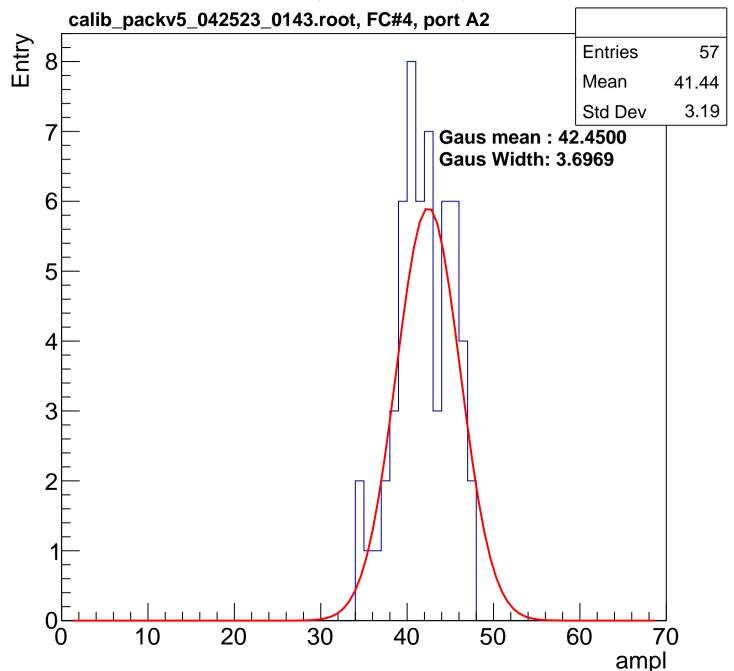


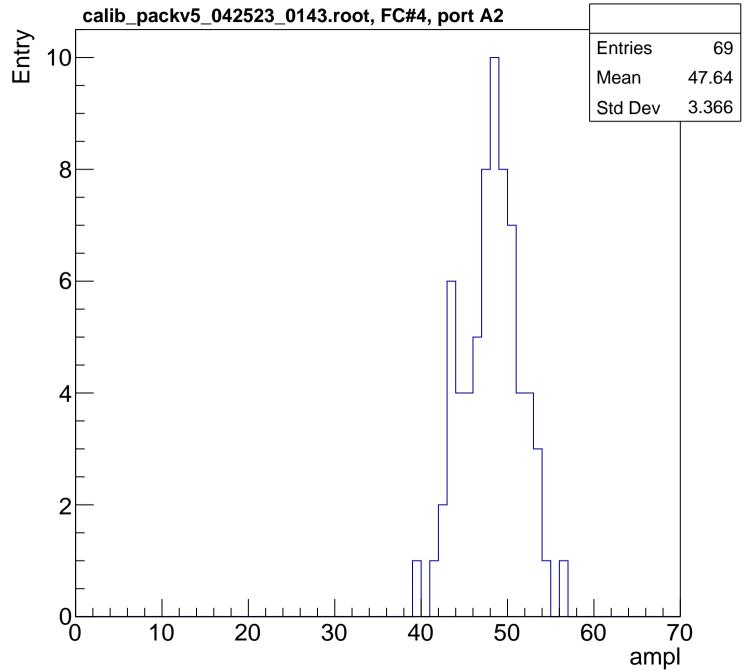


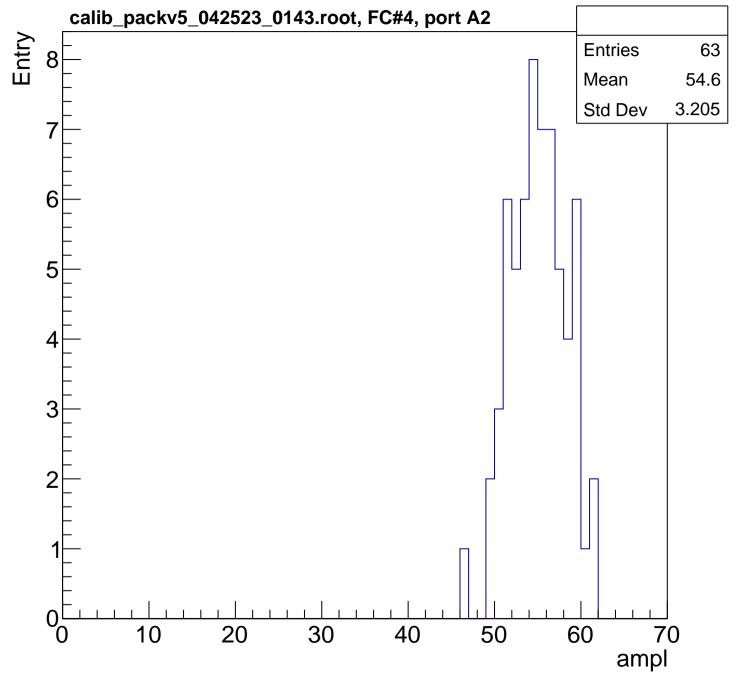


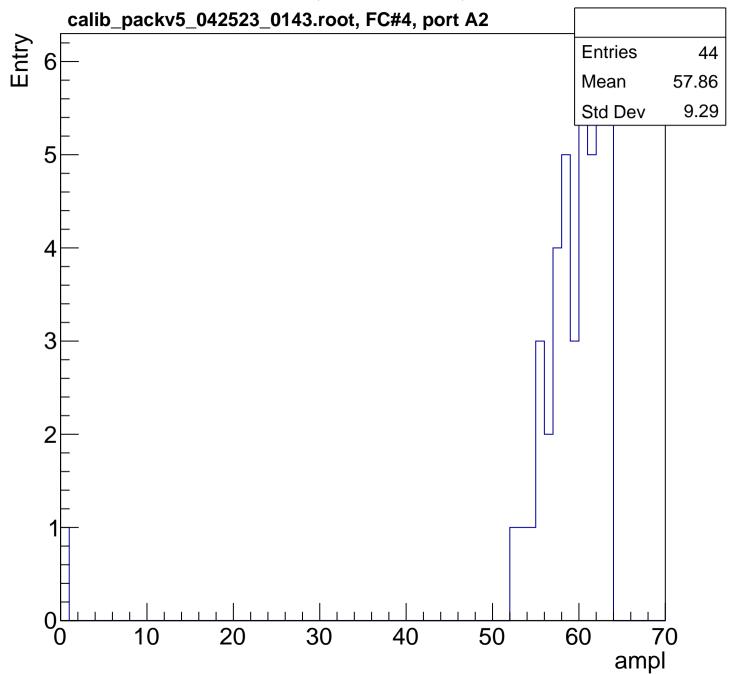


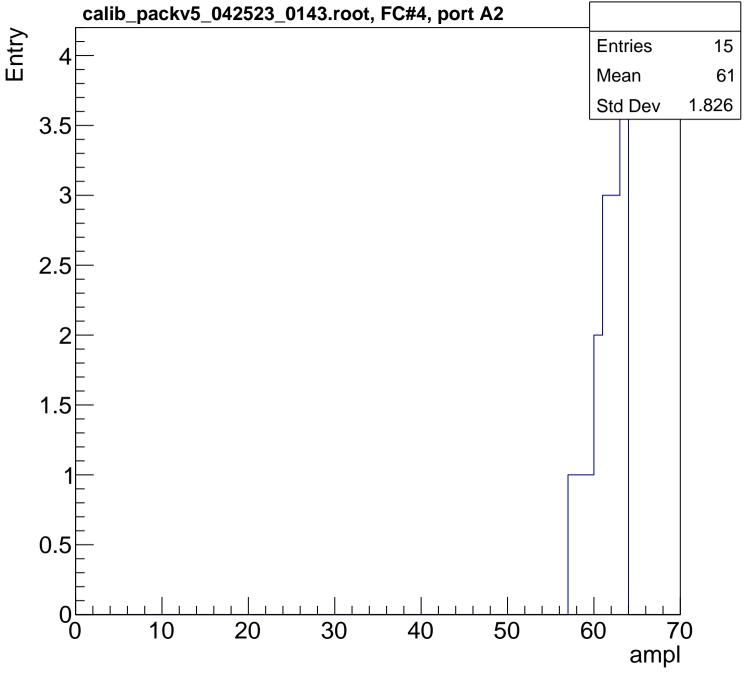


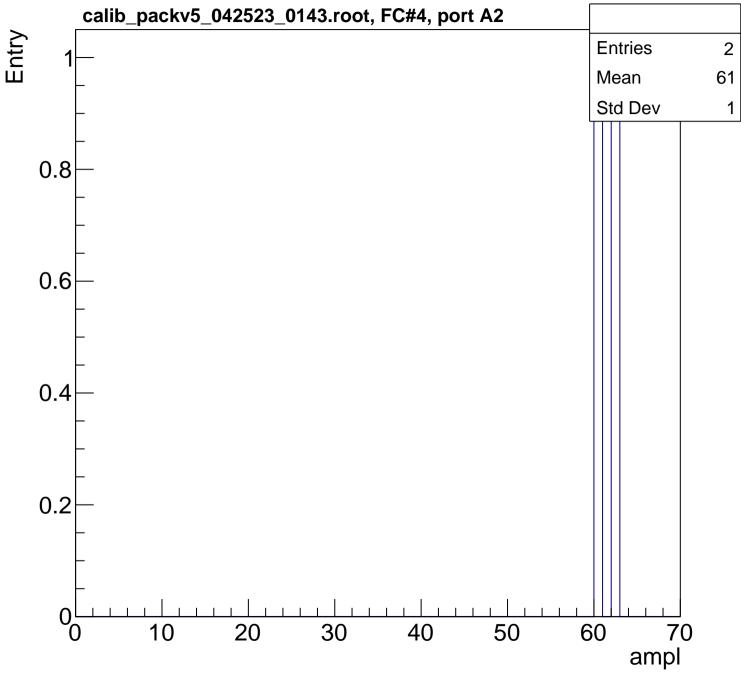


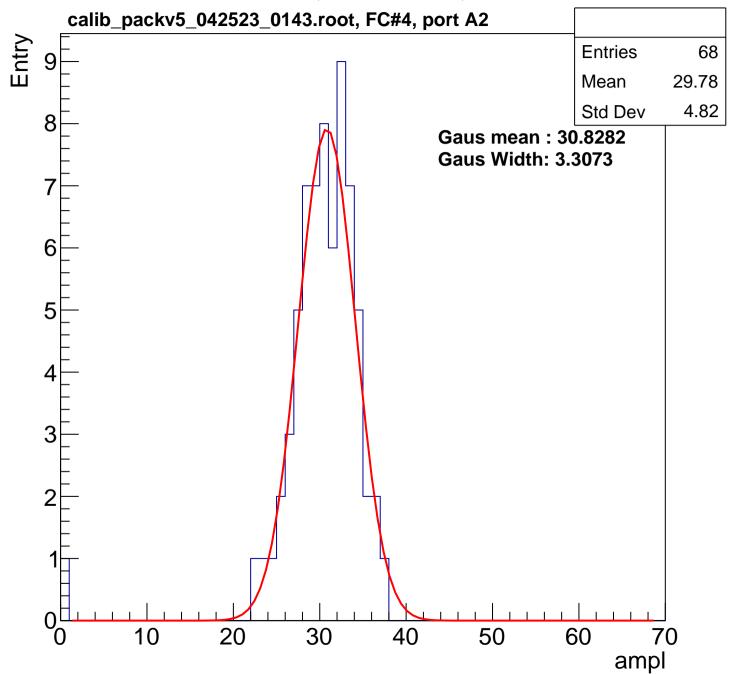


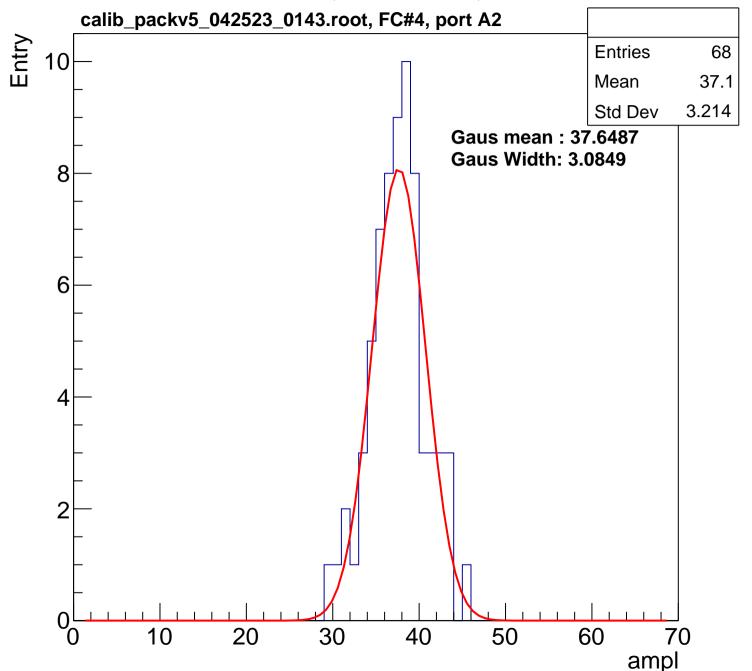


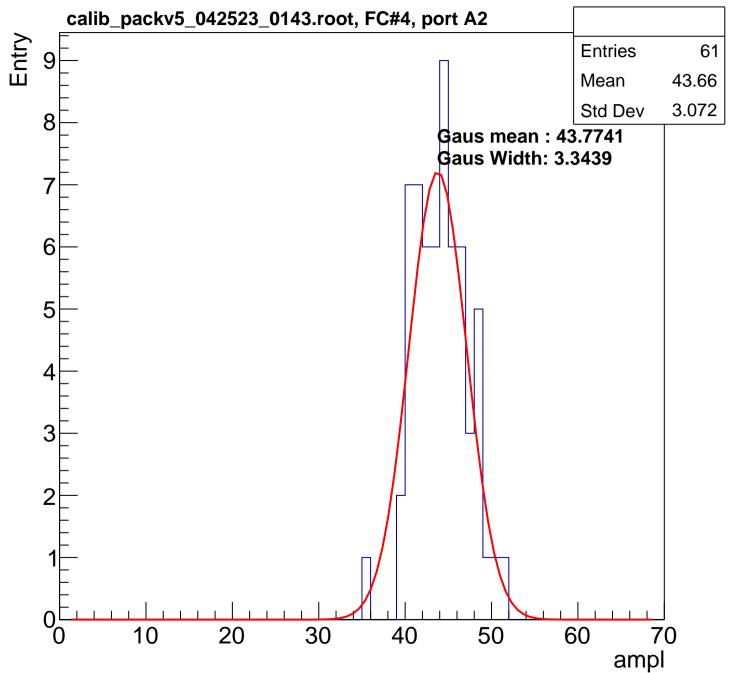


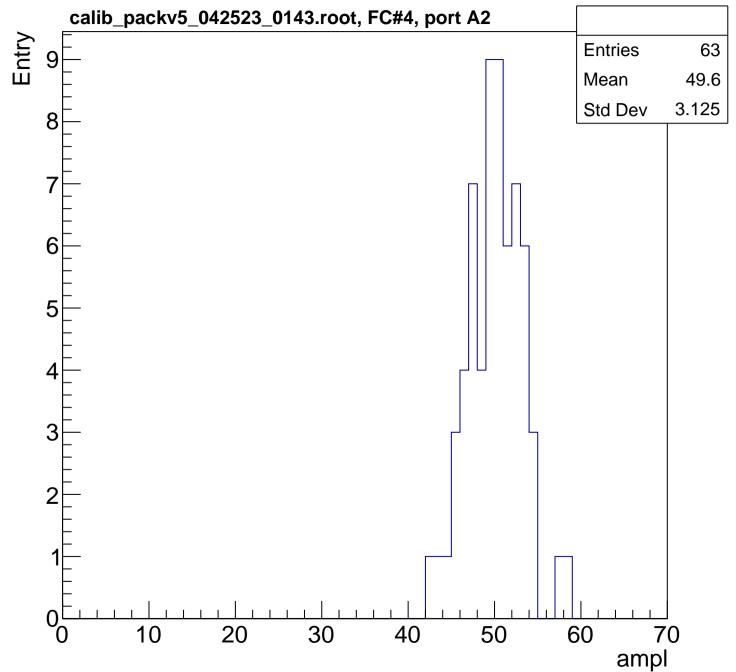


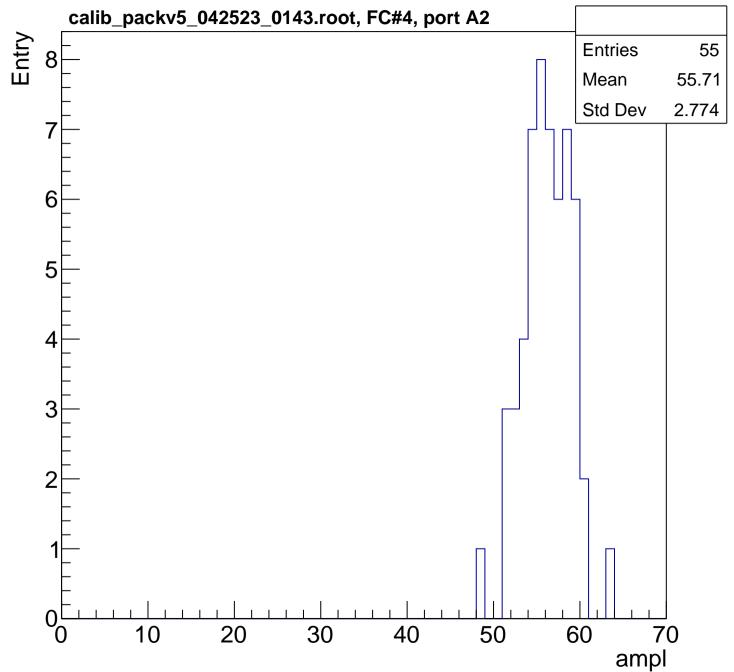


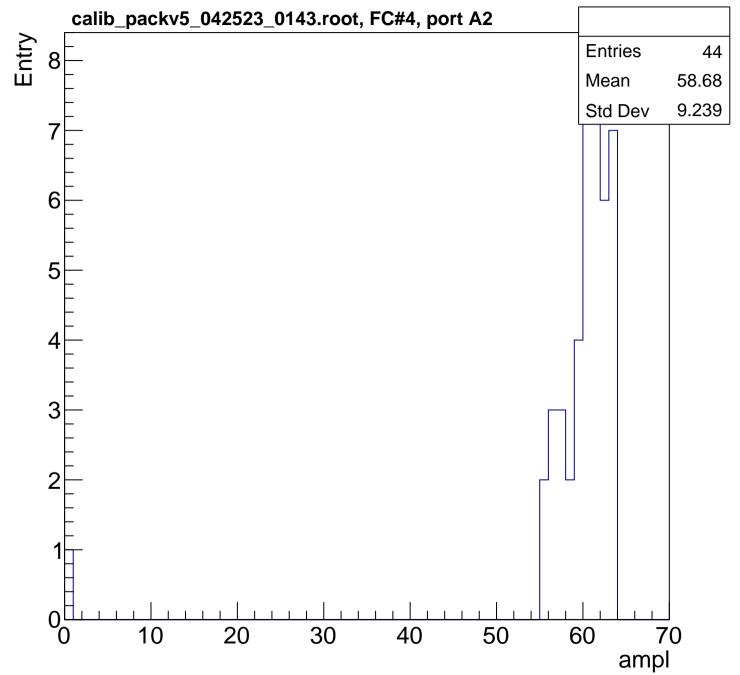


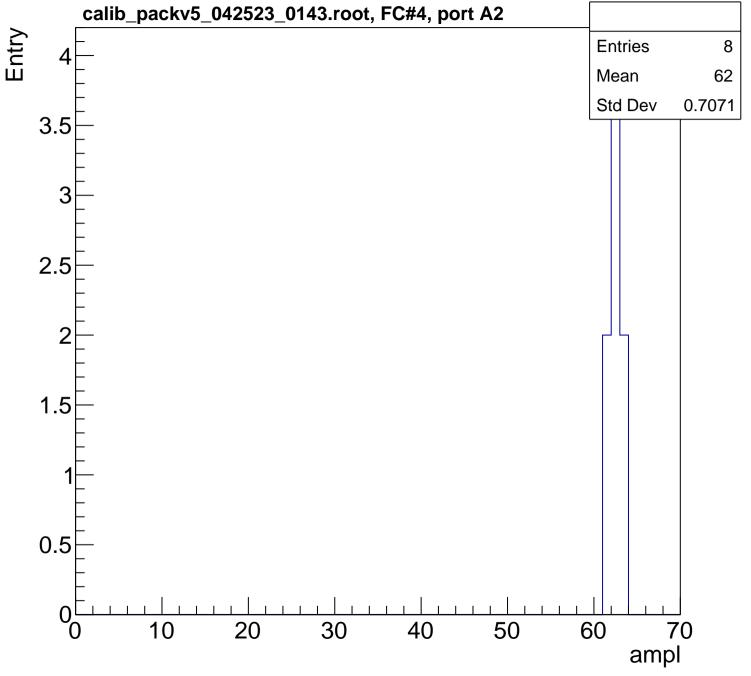




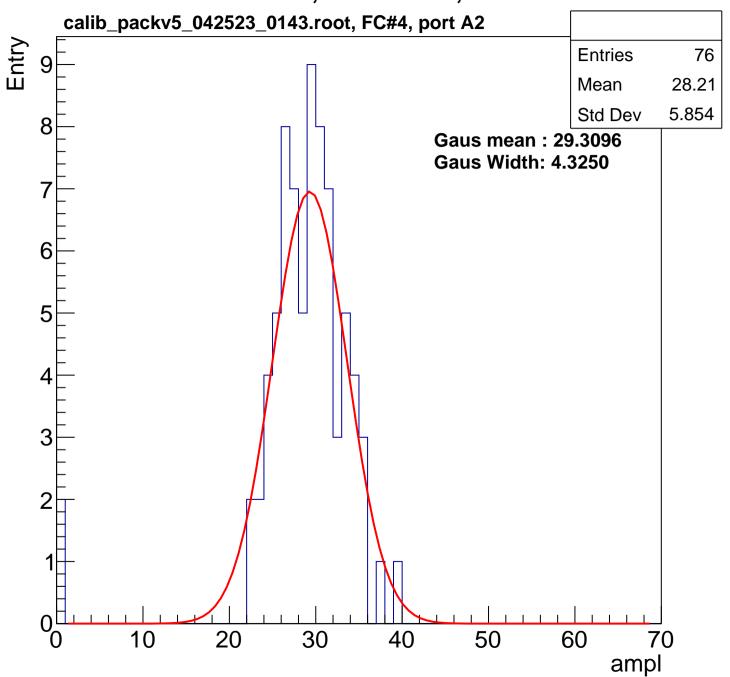


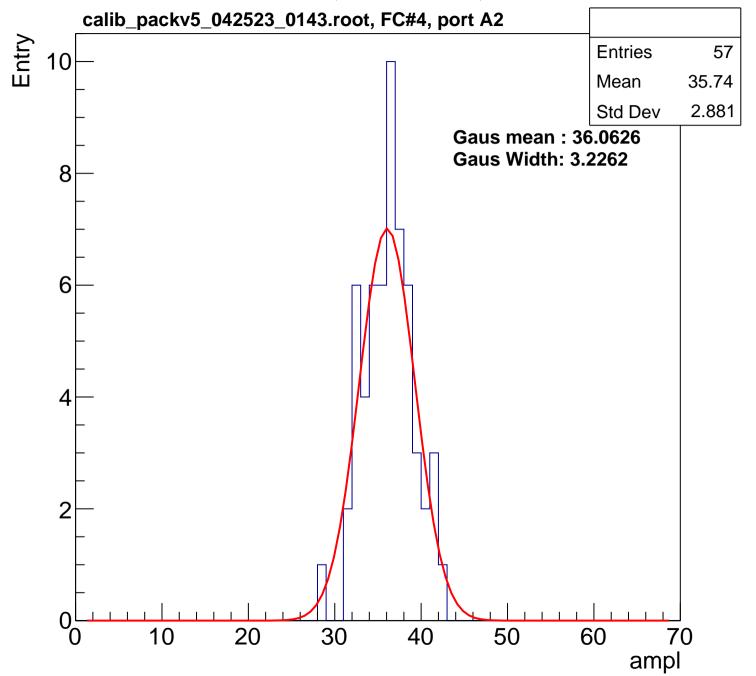


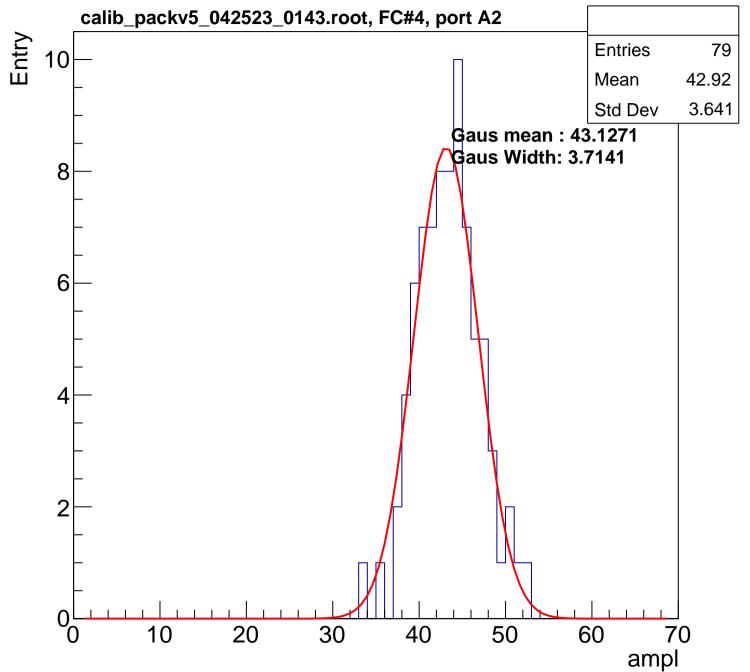


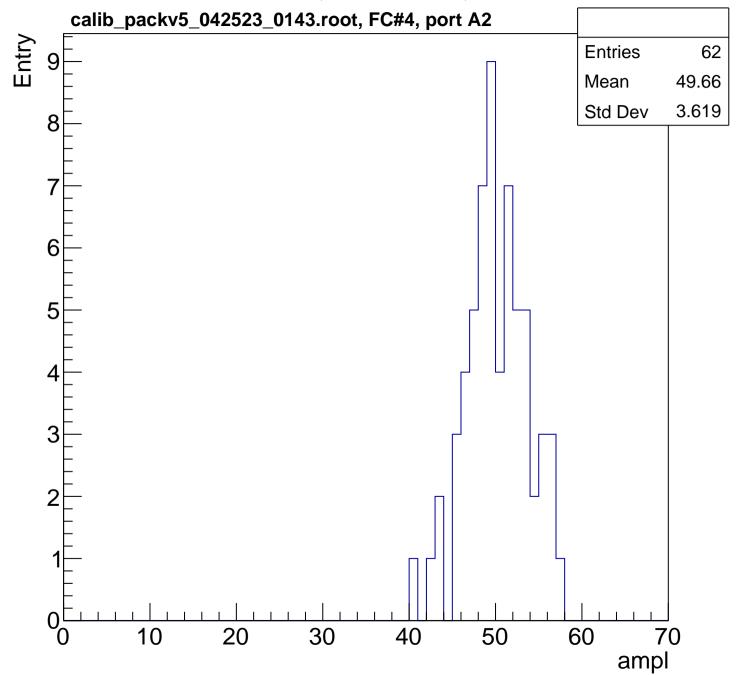


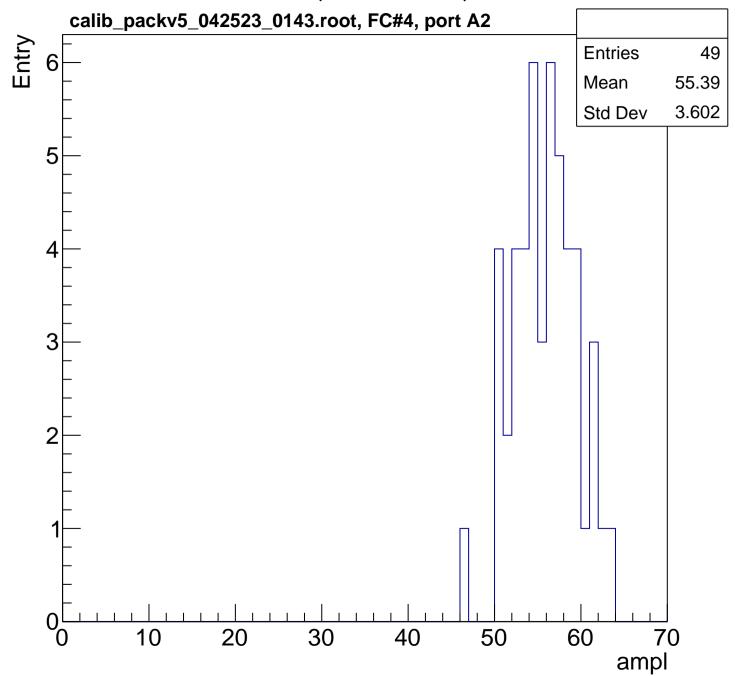
B1L100S, U3-ch45, adc7 calib_packv5_042523_0143.root, FC#4, port A2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

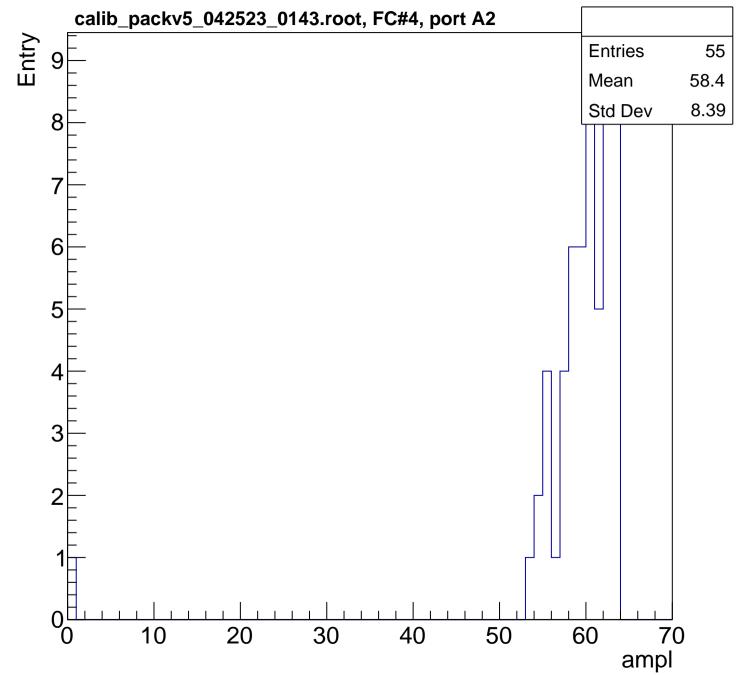


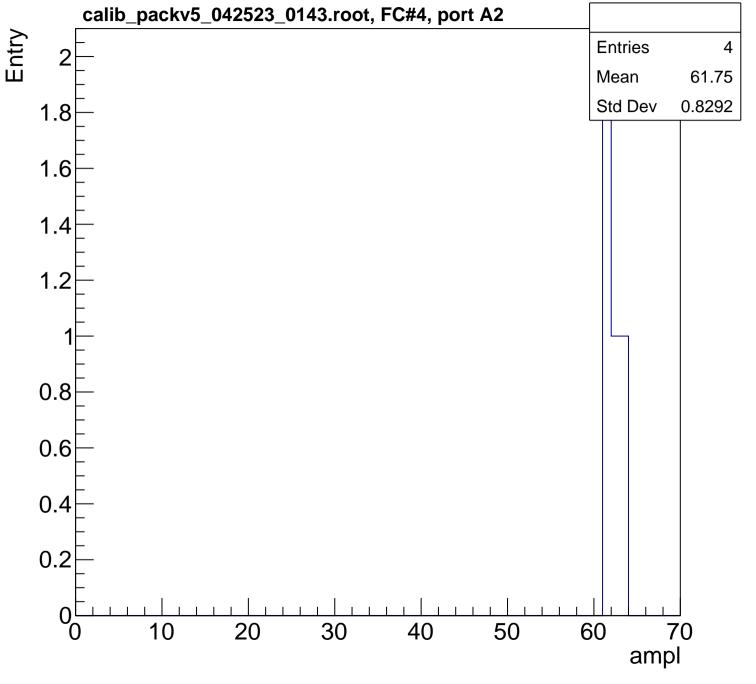




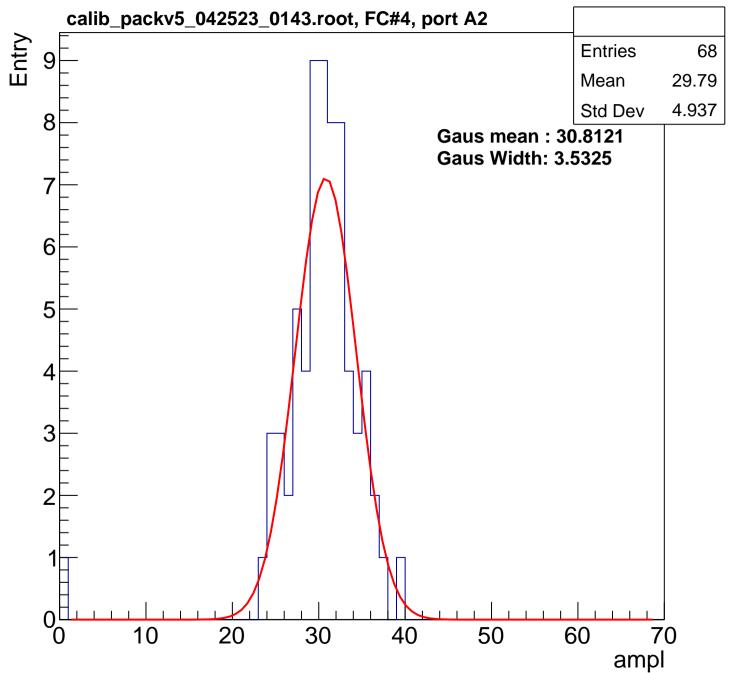


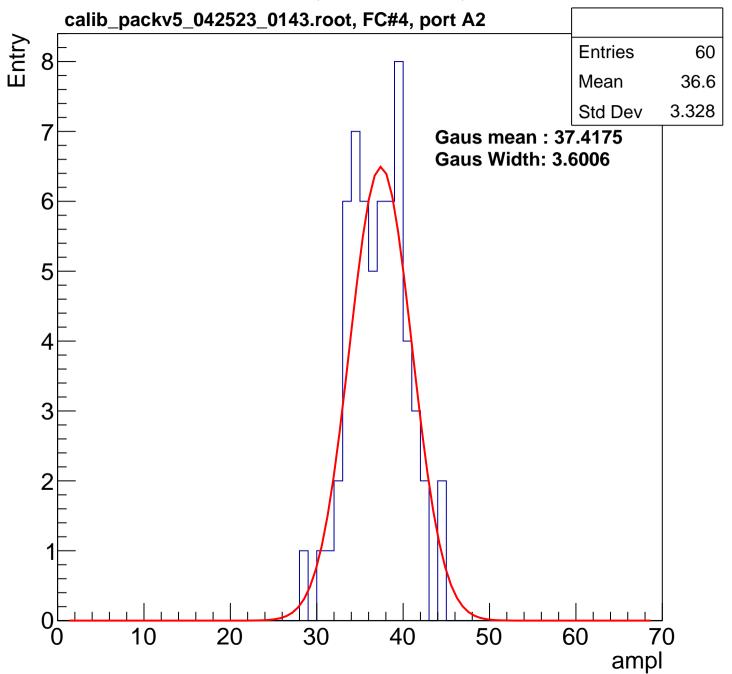


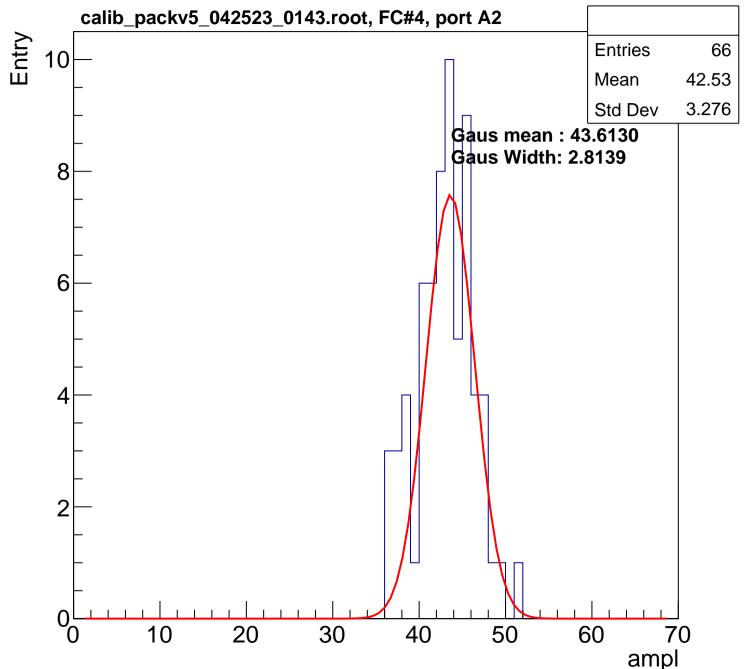


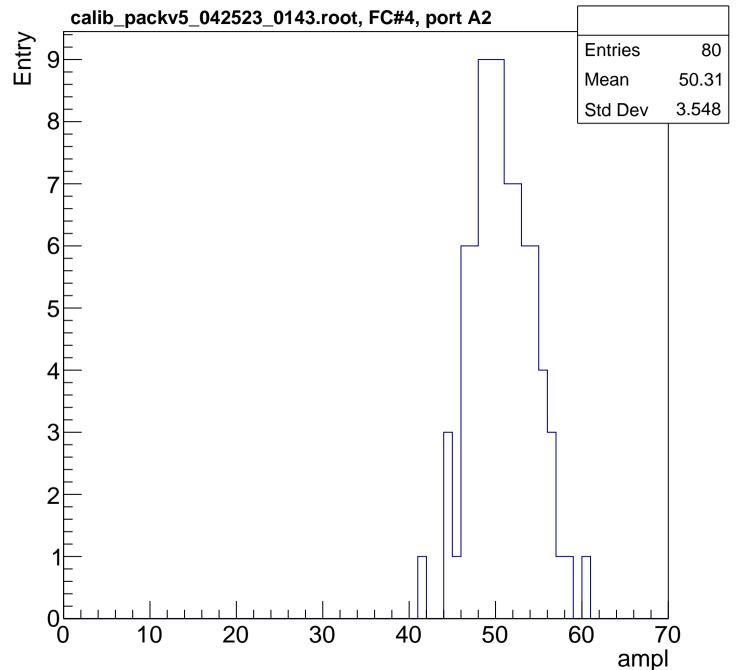


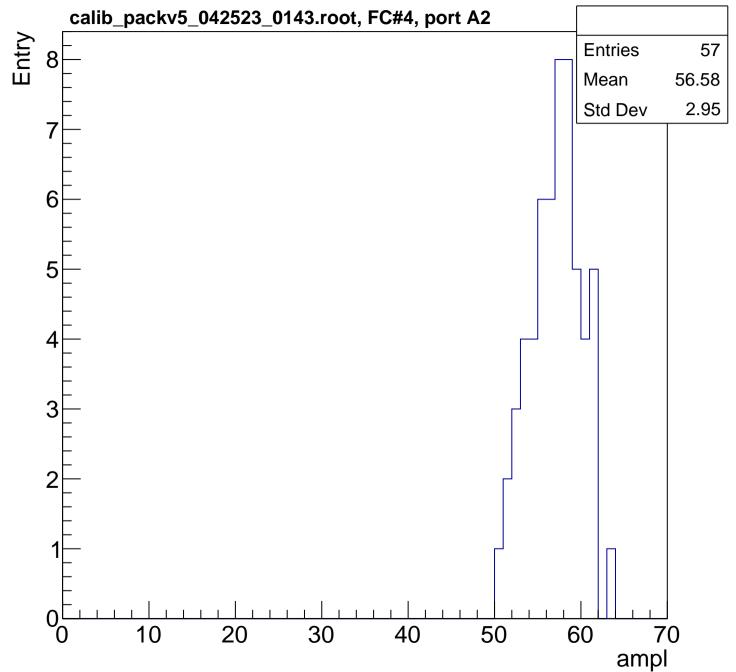
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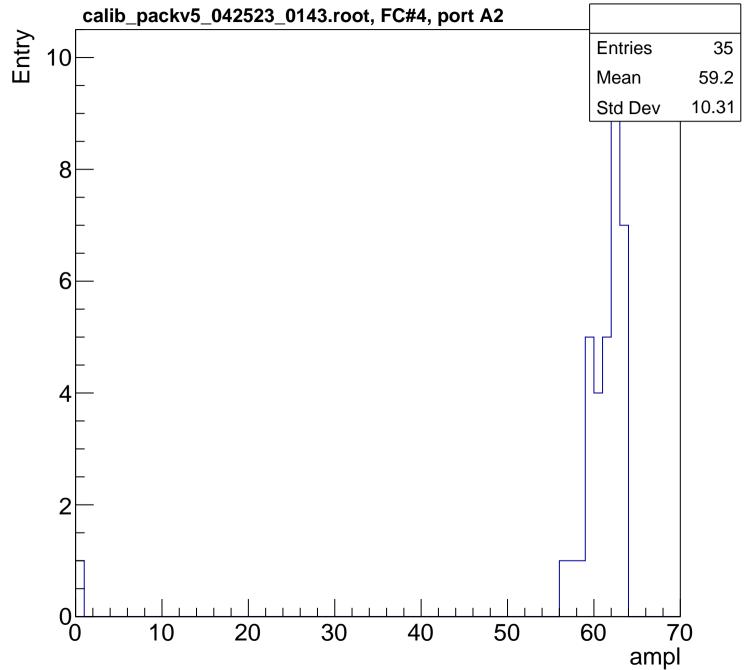


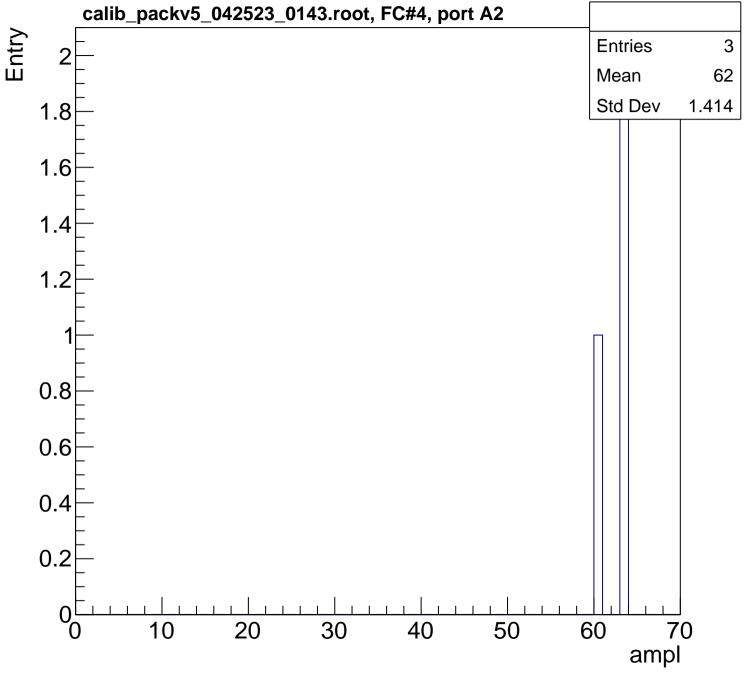




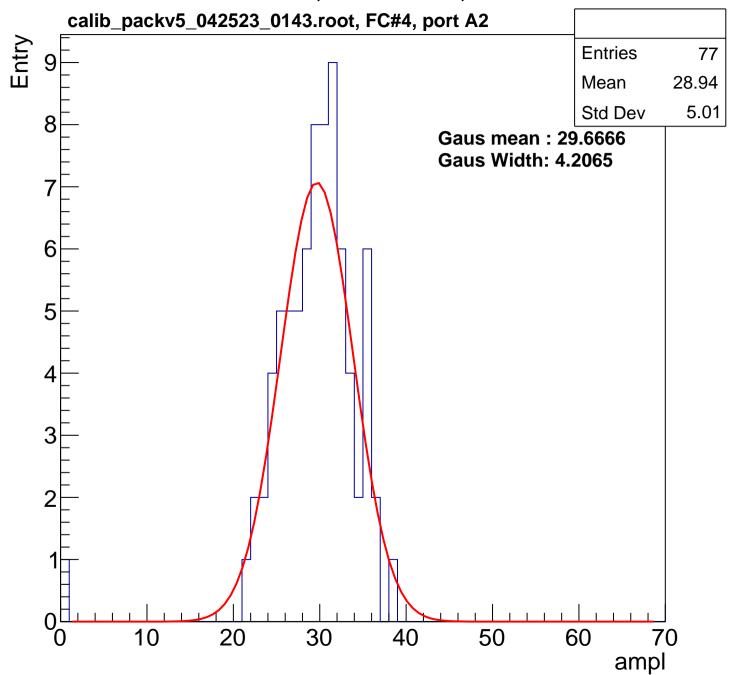


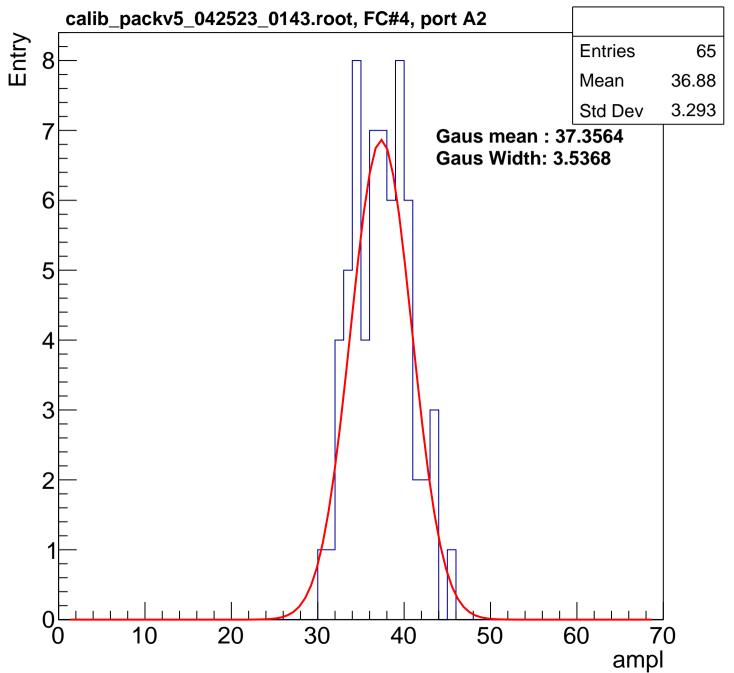


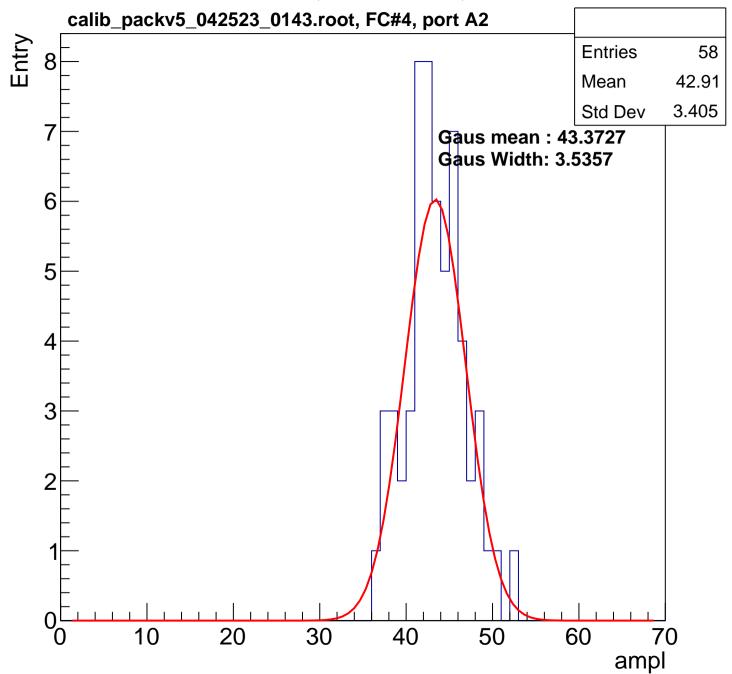


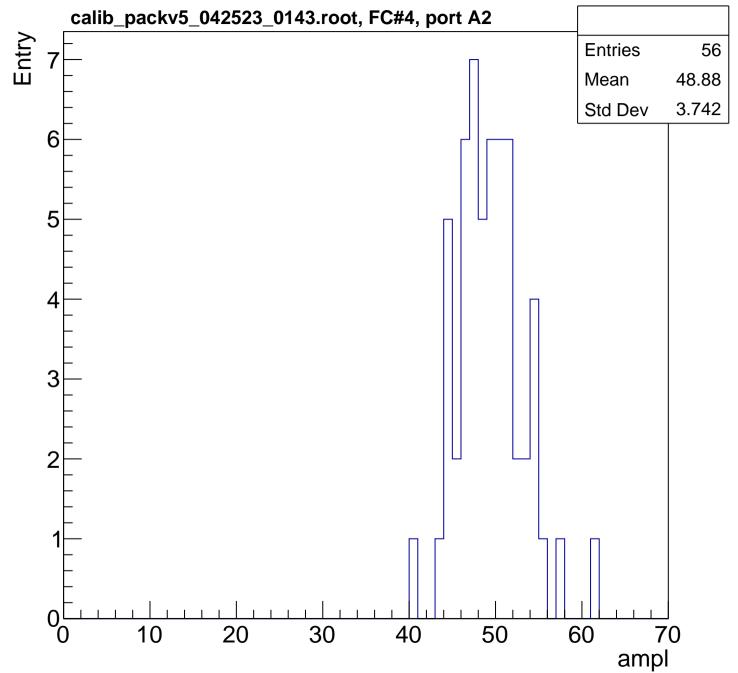


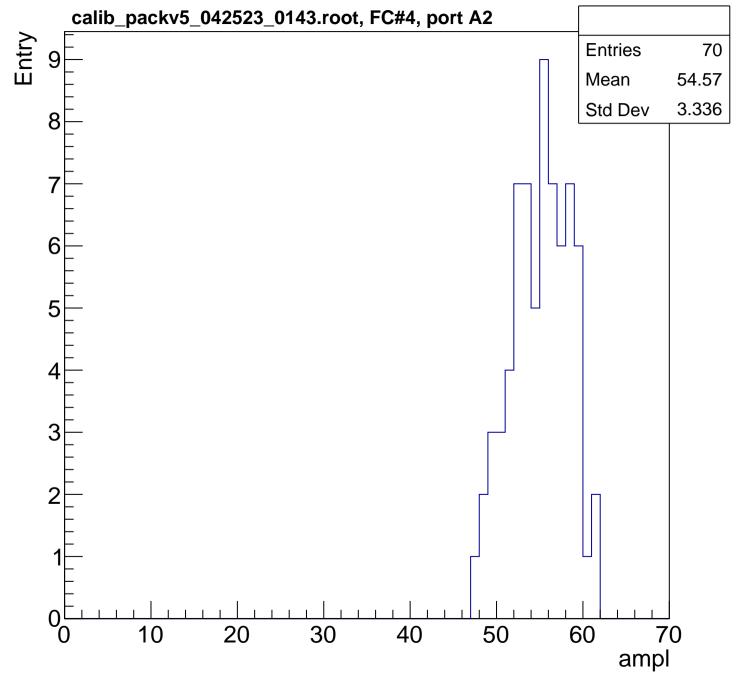


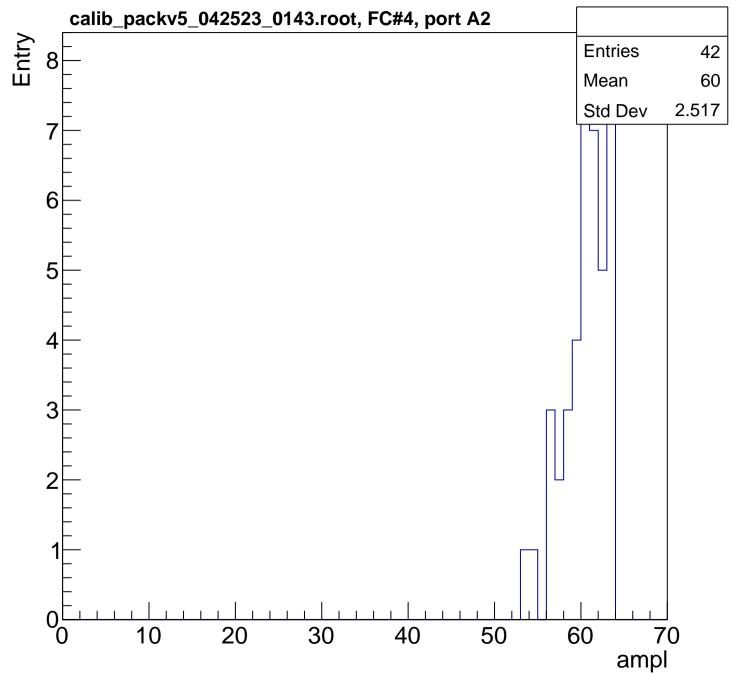


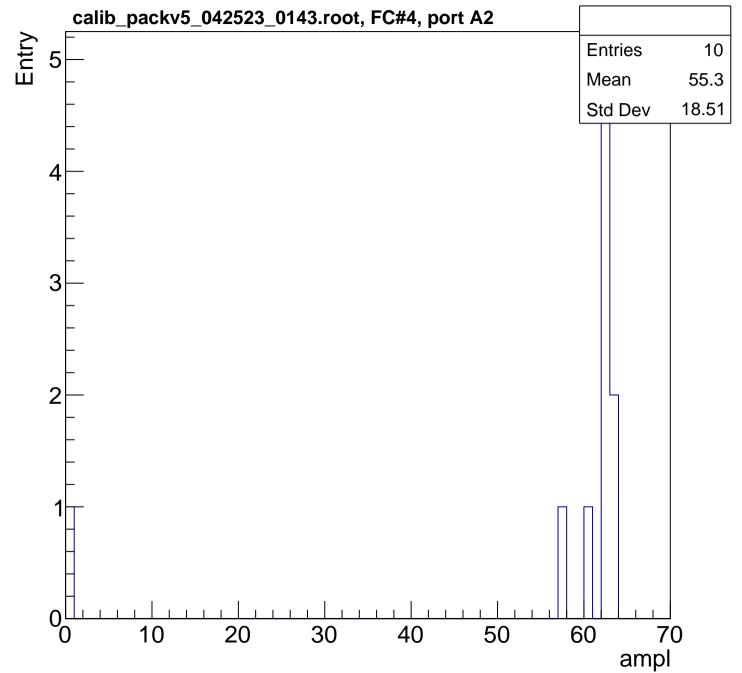




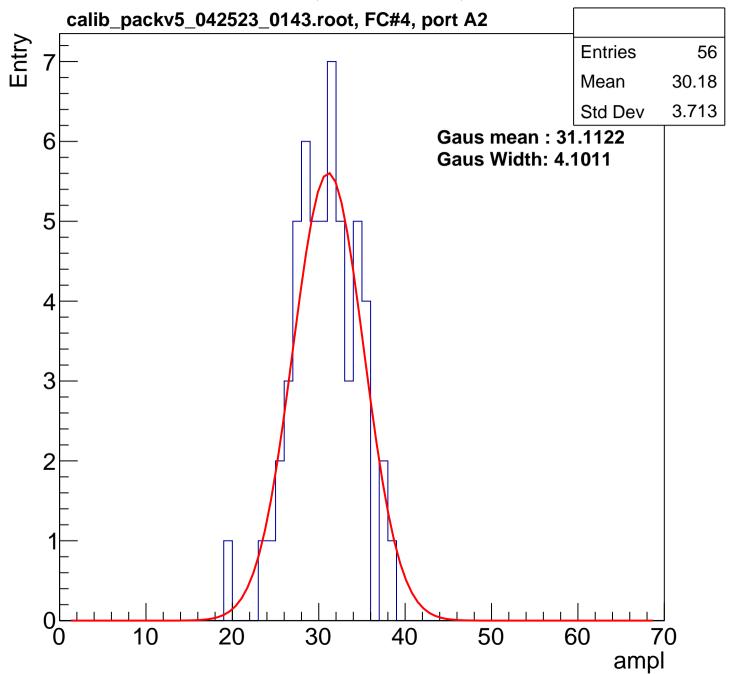


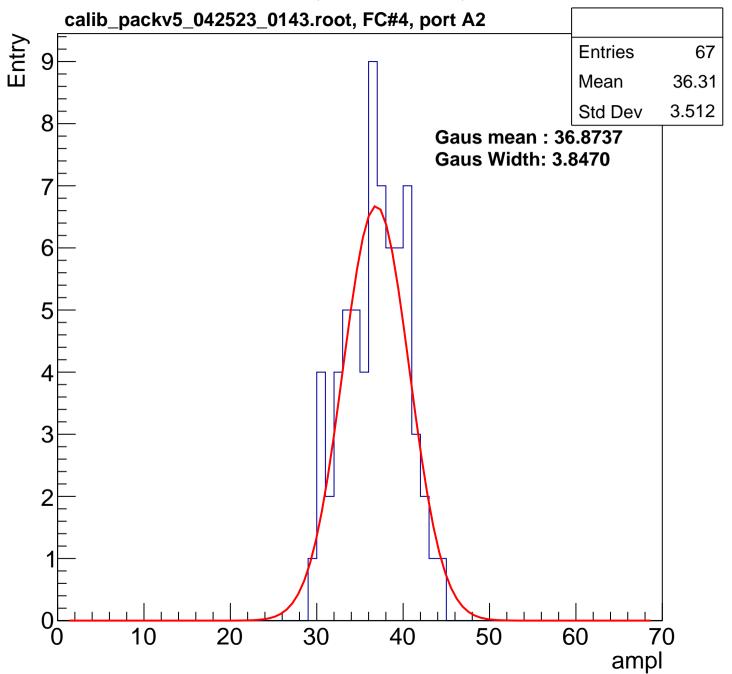


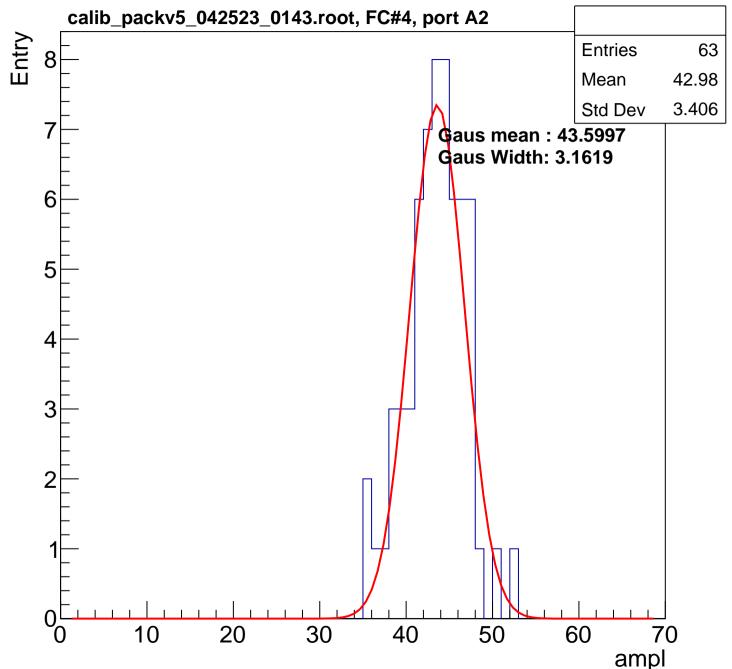


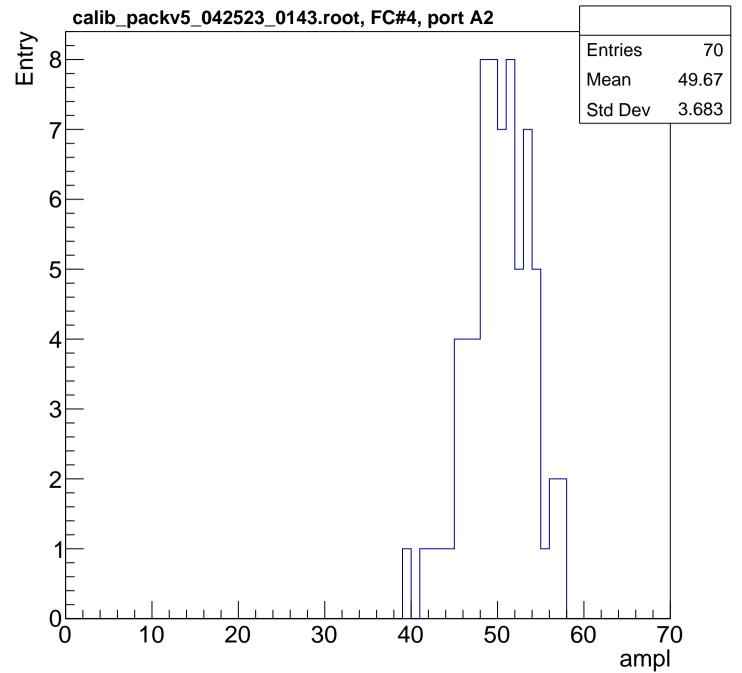


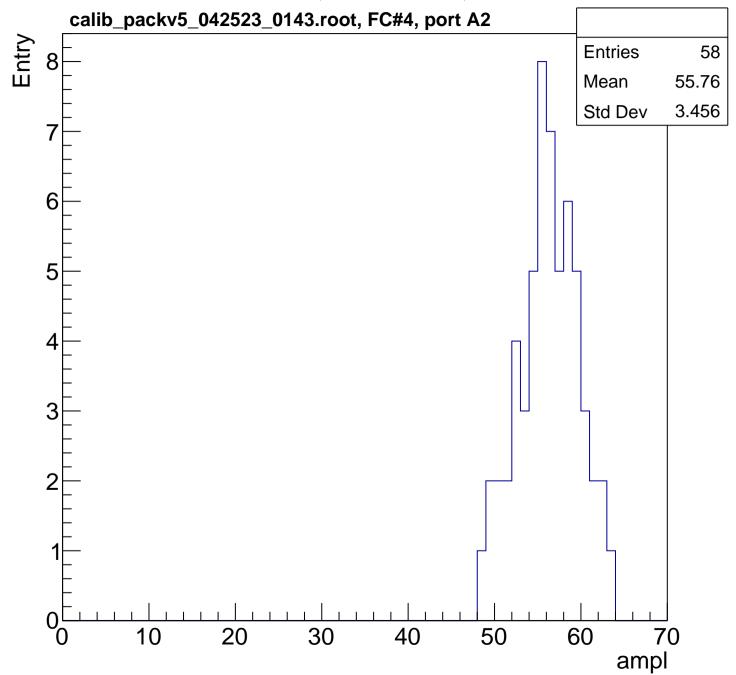
B1L100S, U3-ch48, adc7 calib_packv5_042523_0143.root, FC#4, port A2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

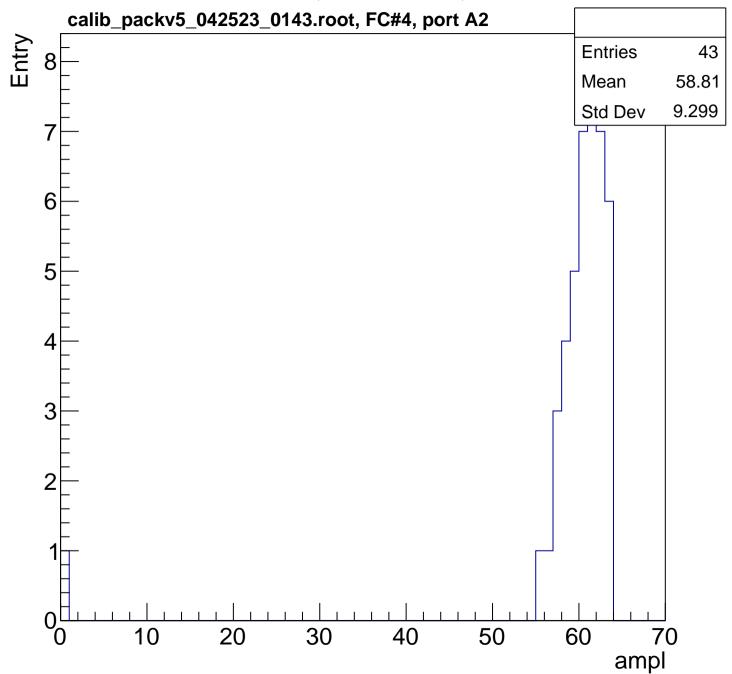


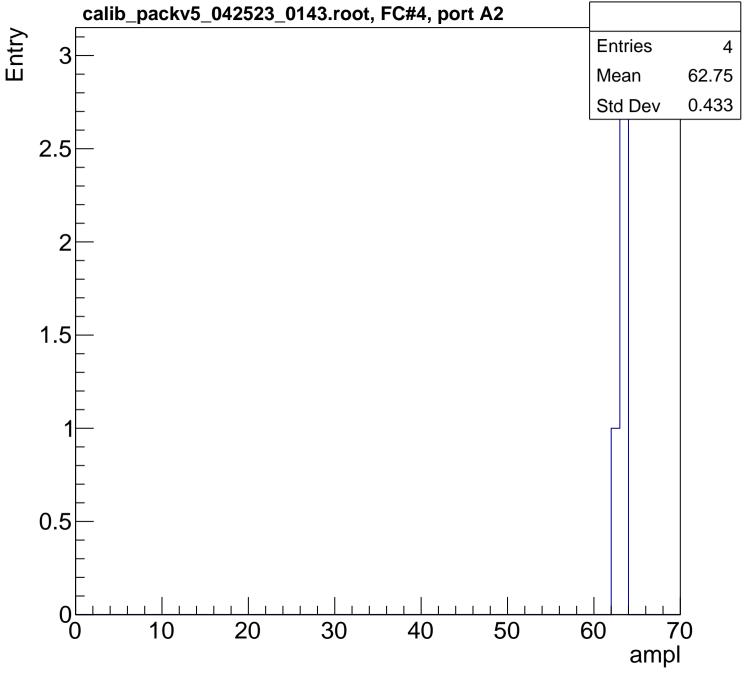


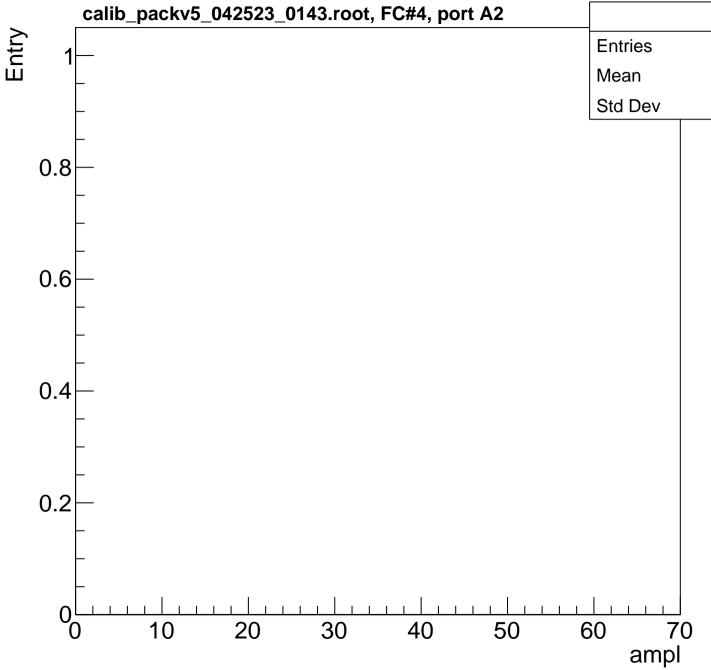


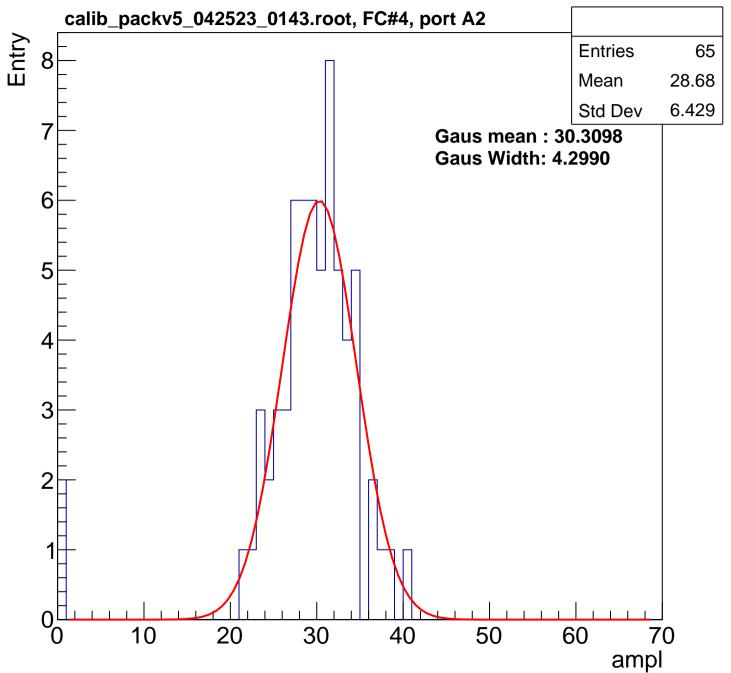


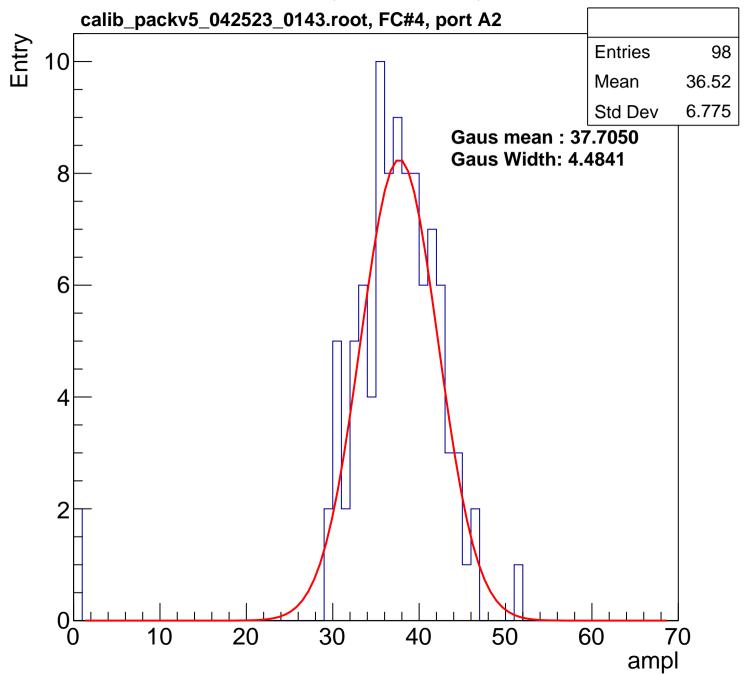


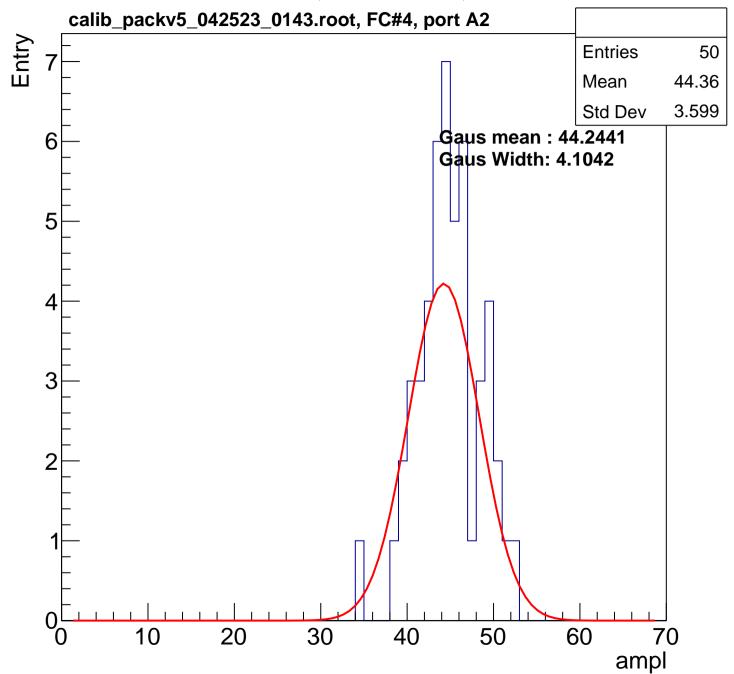


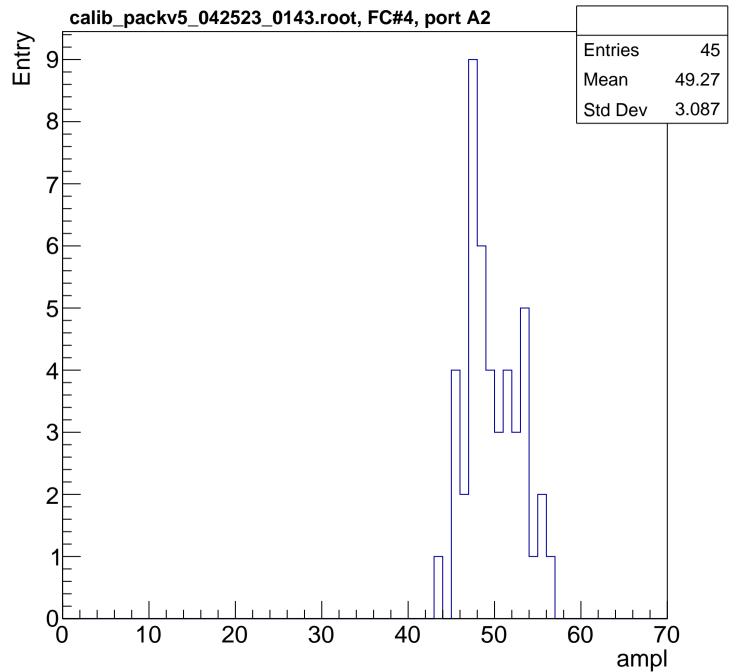


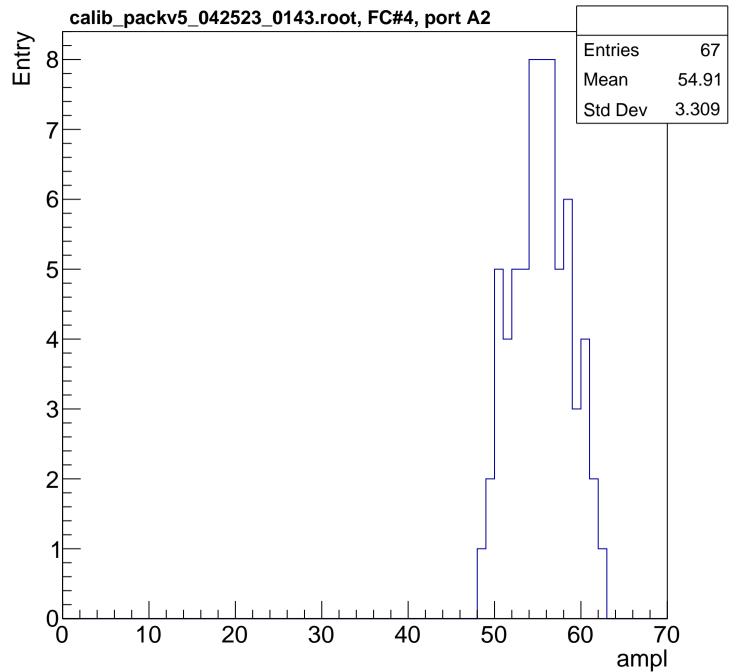


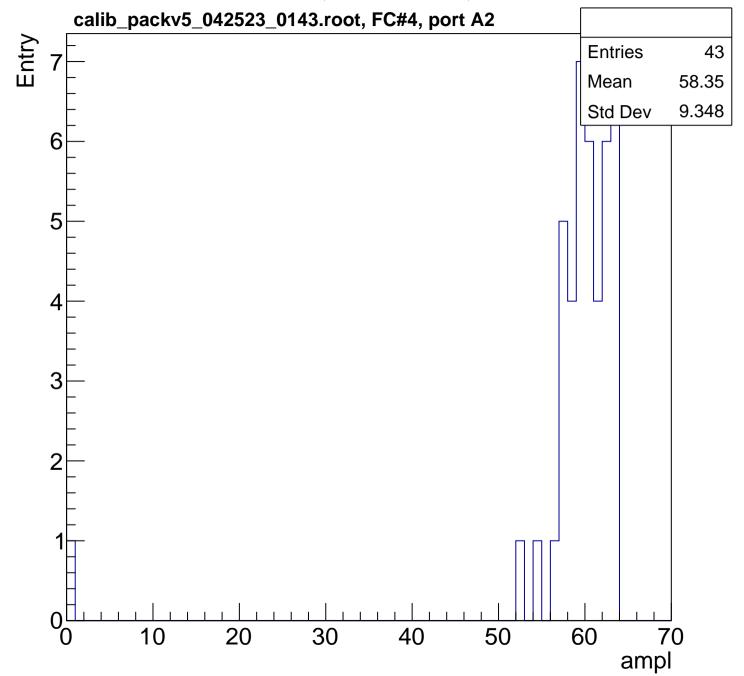


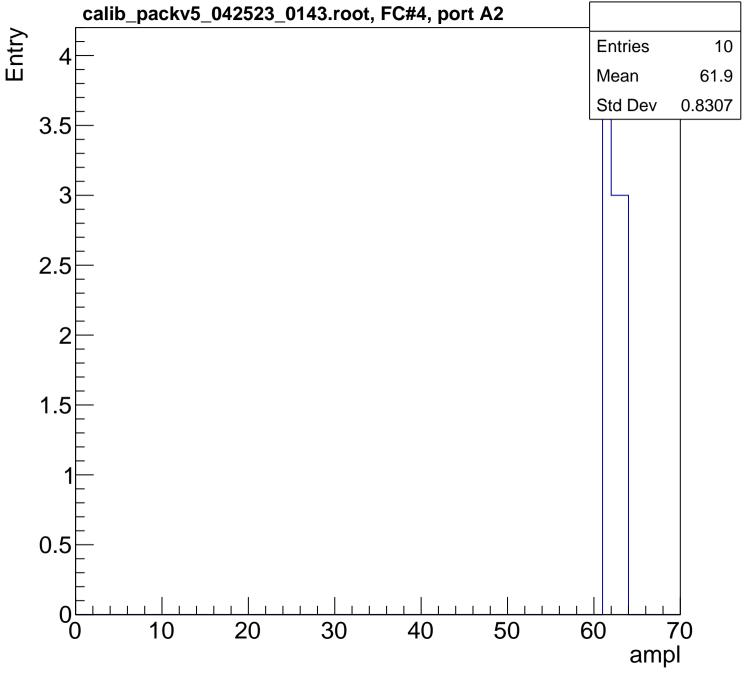


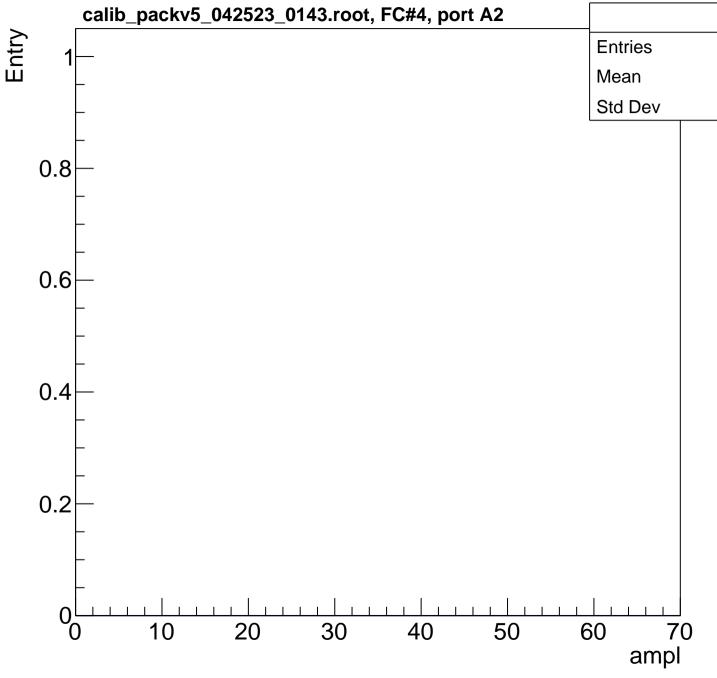


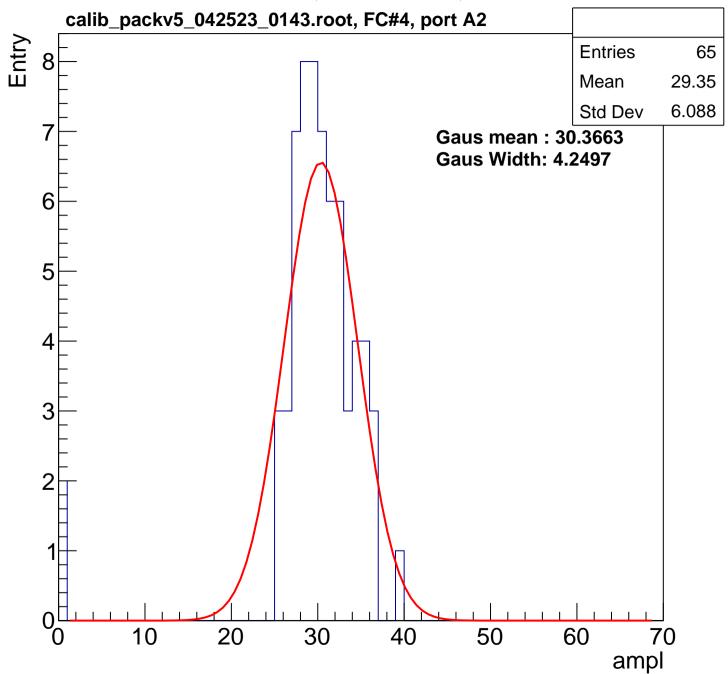


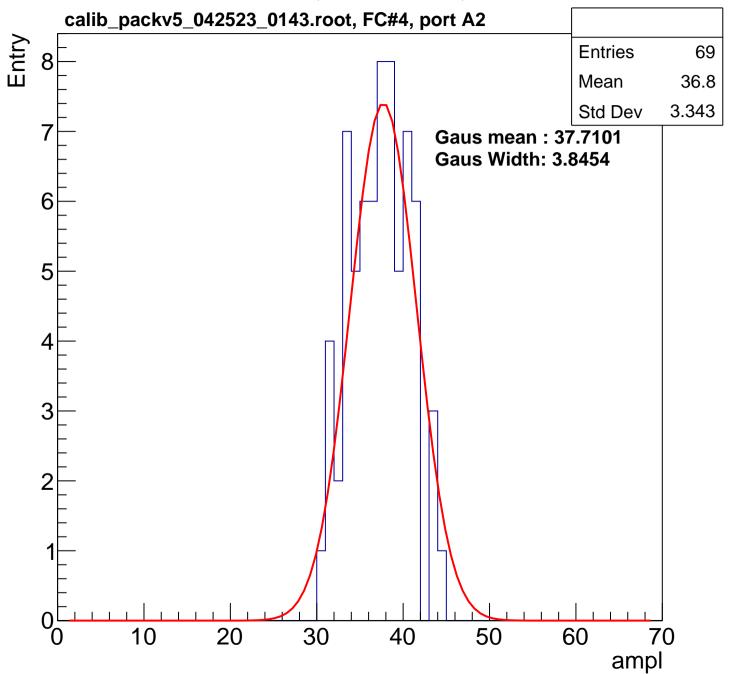


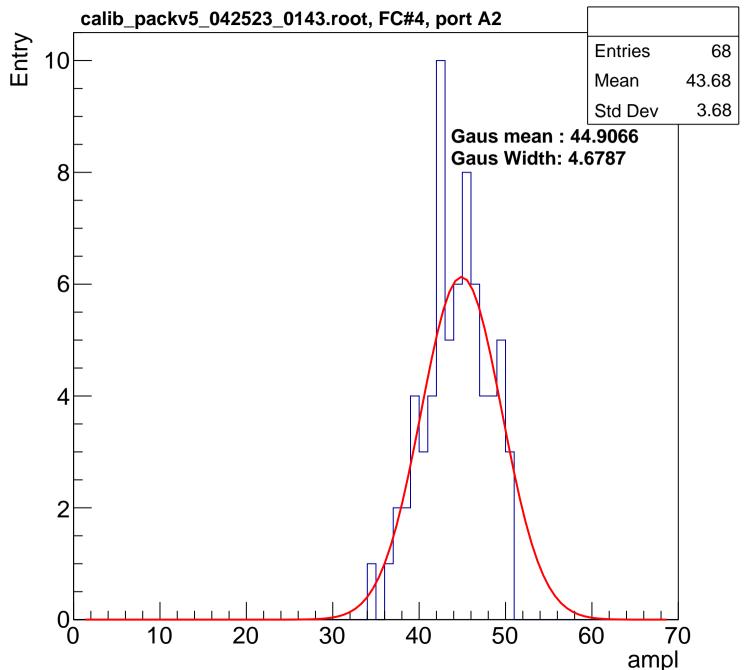


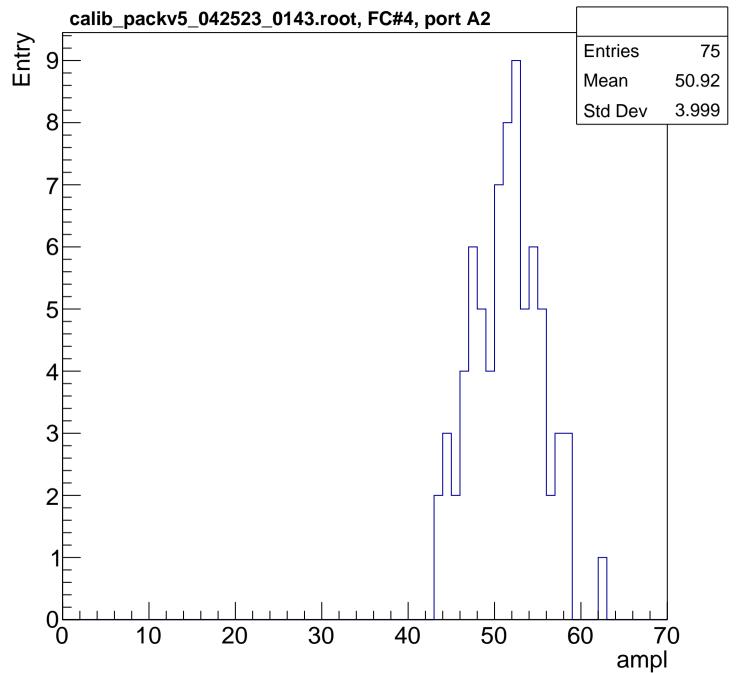


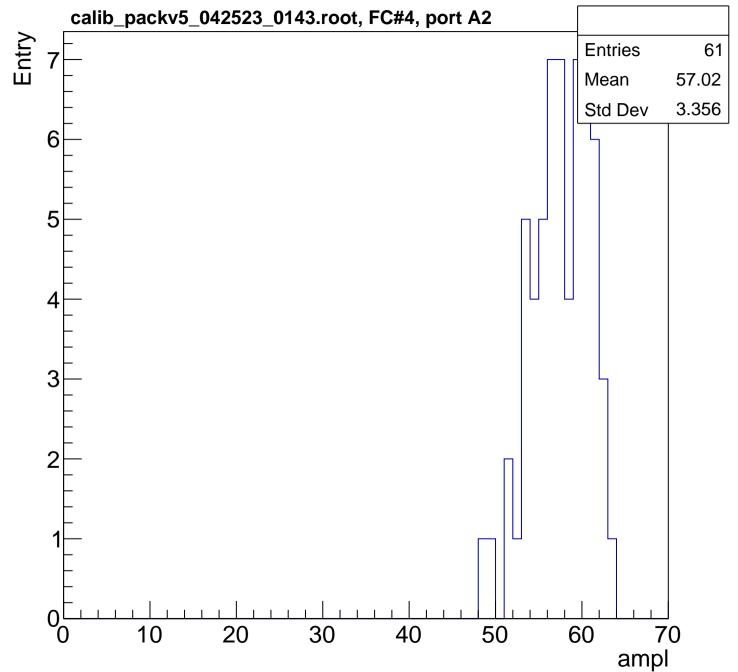


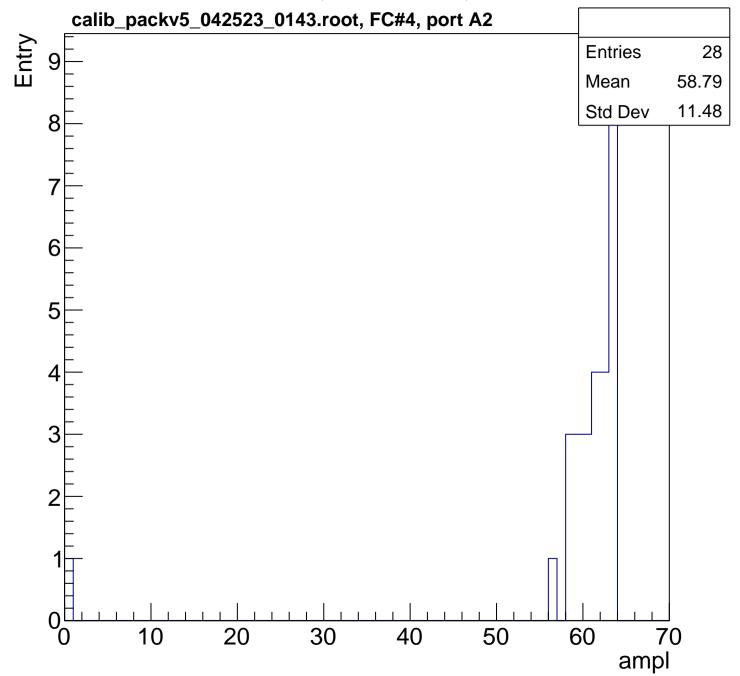


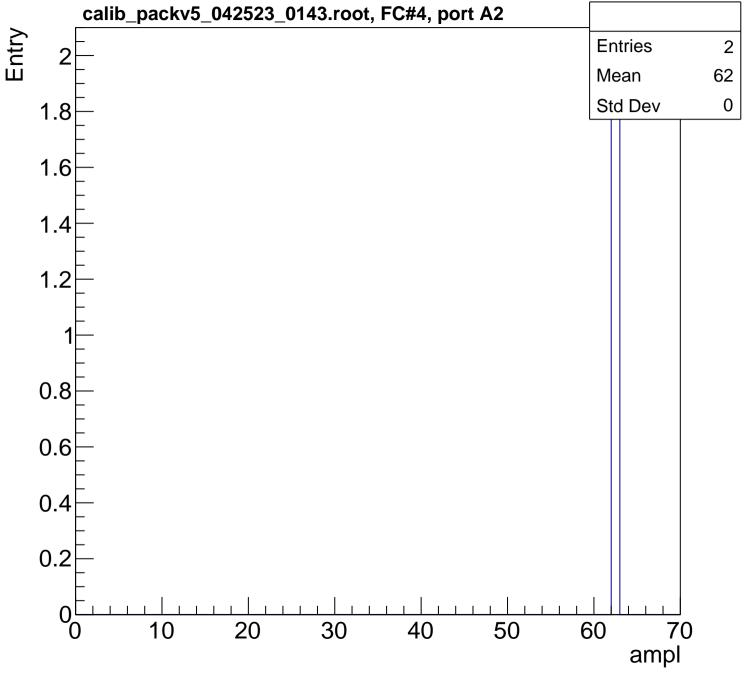


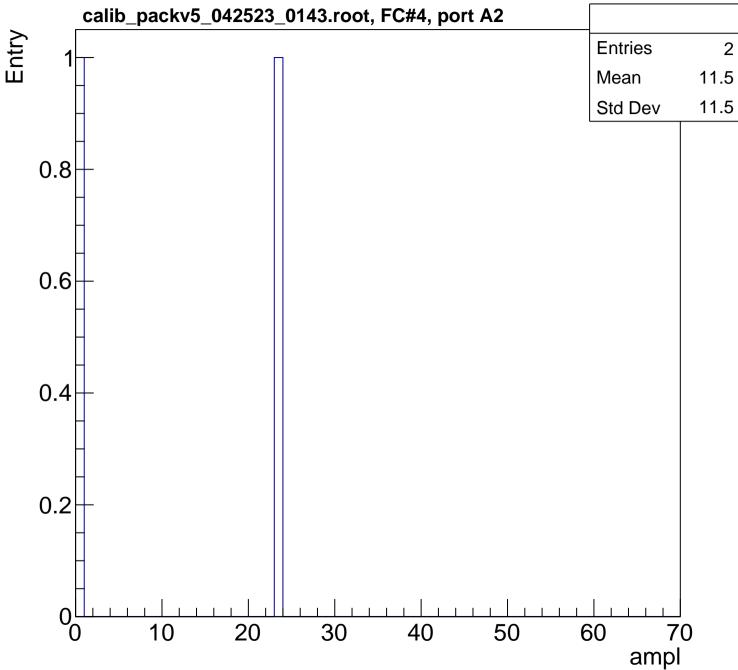


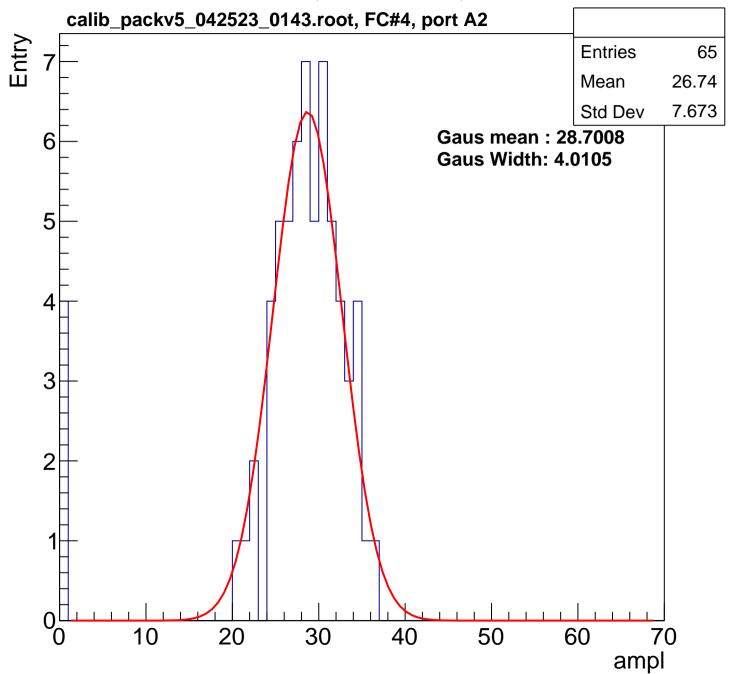


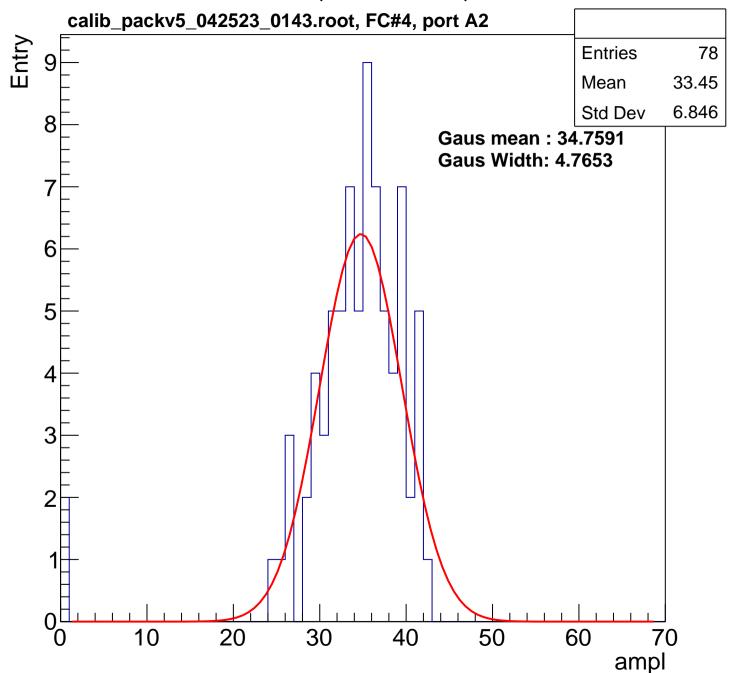


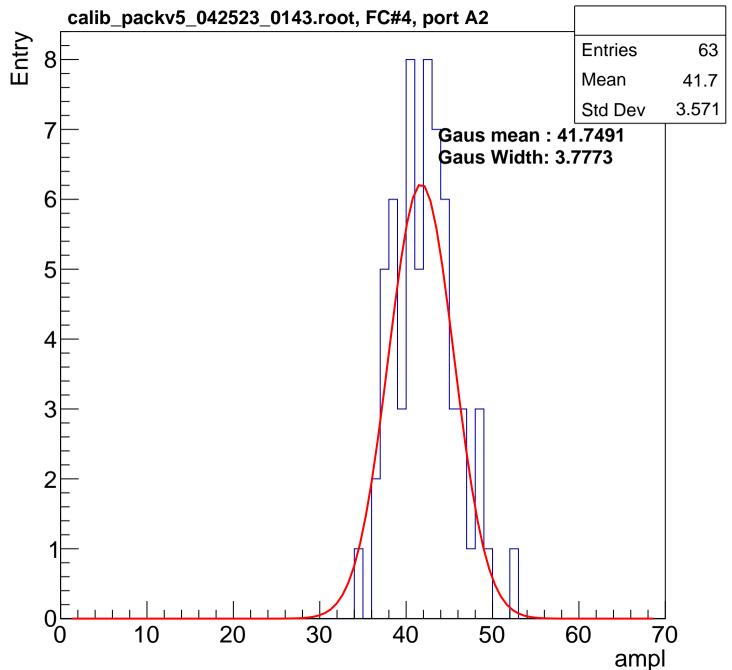


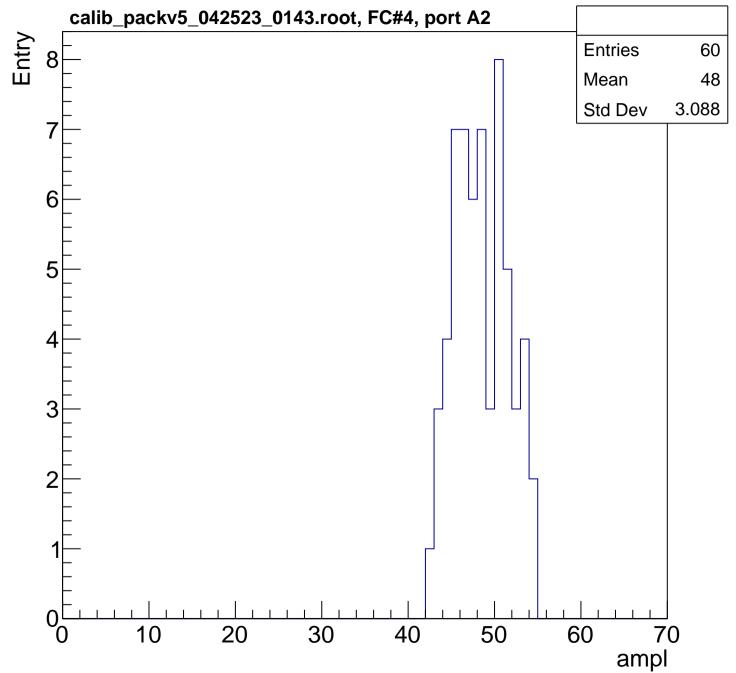


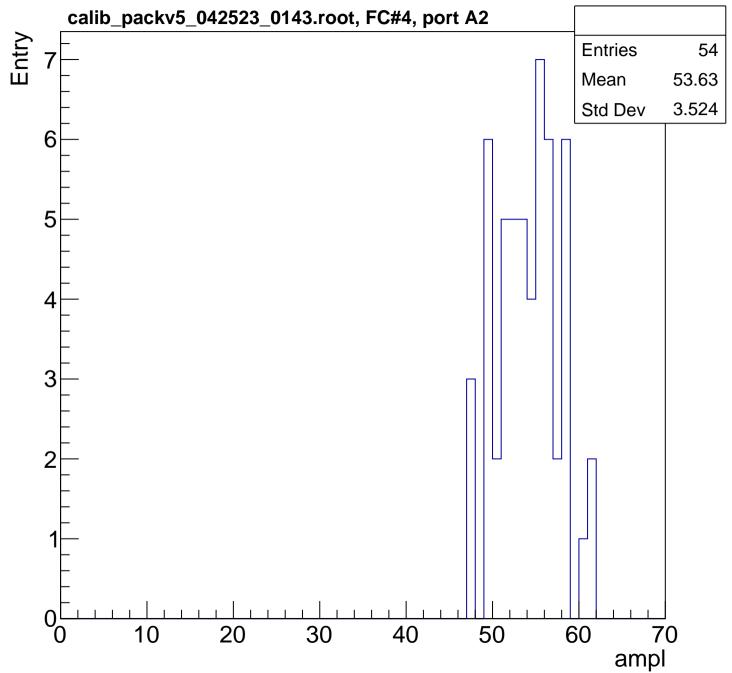


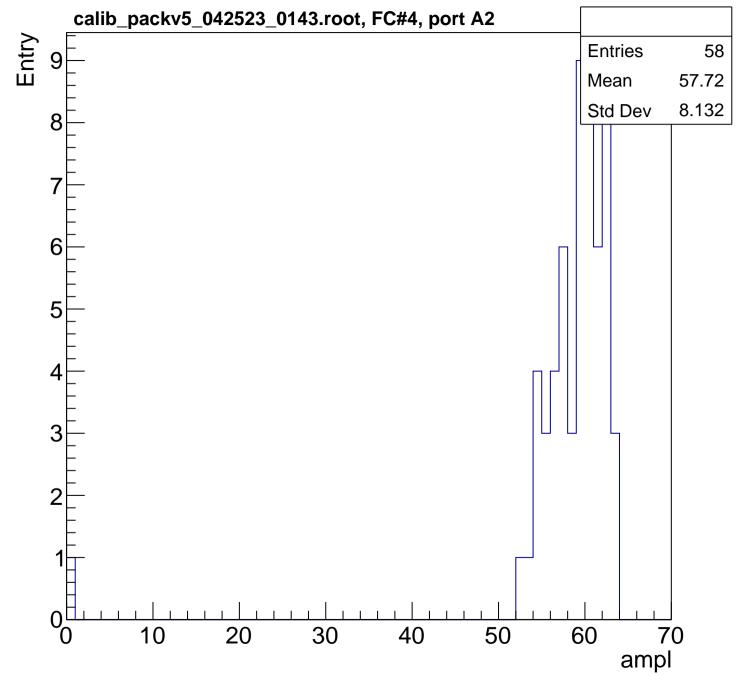


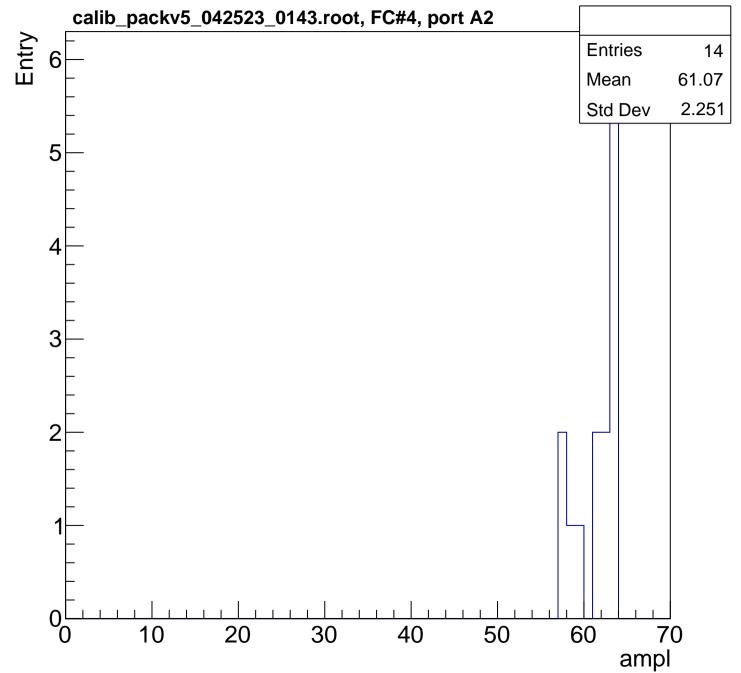


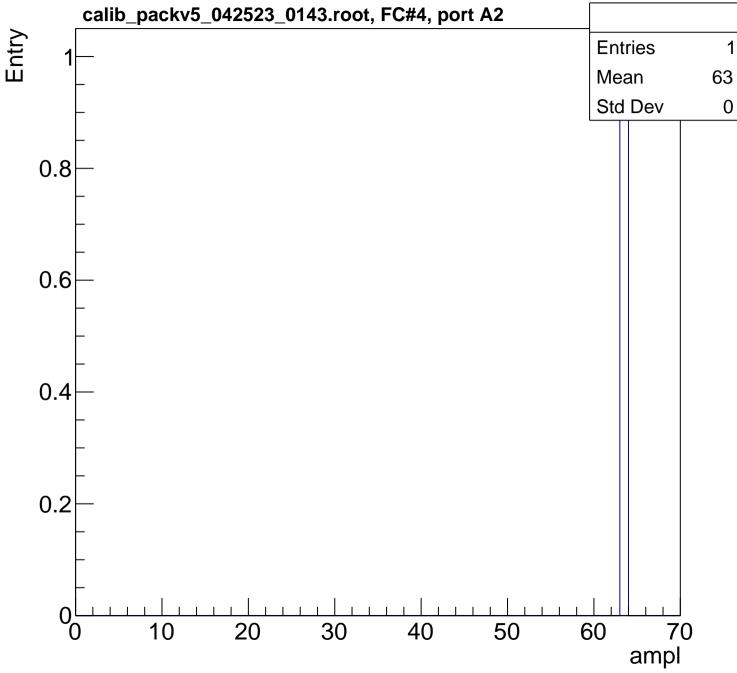


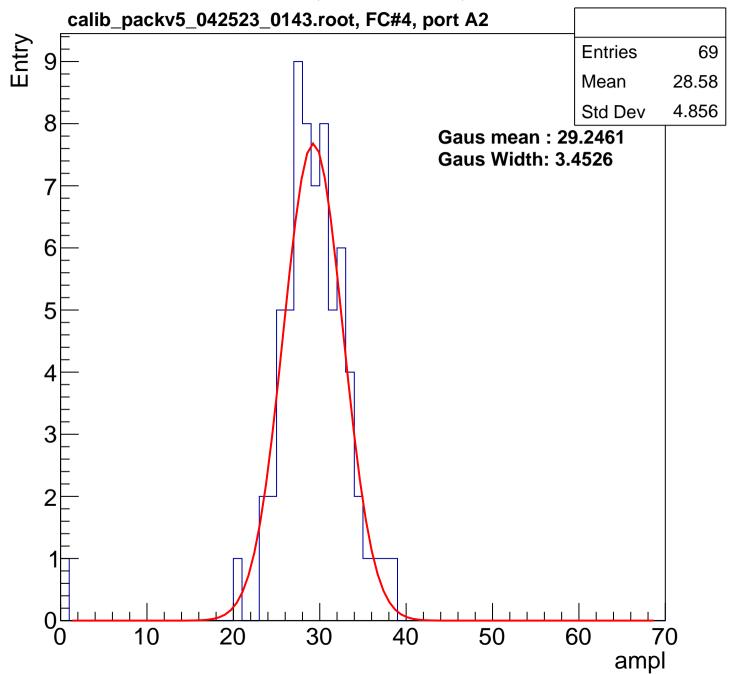


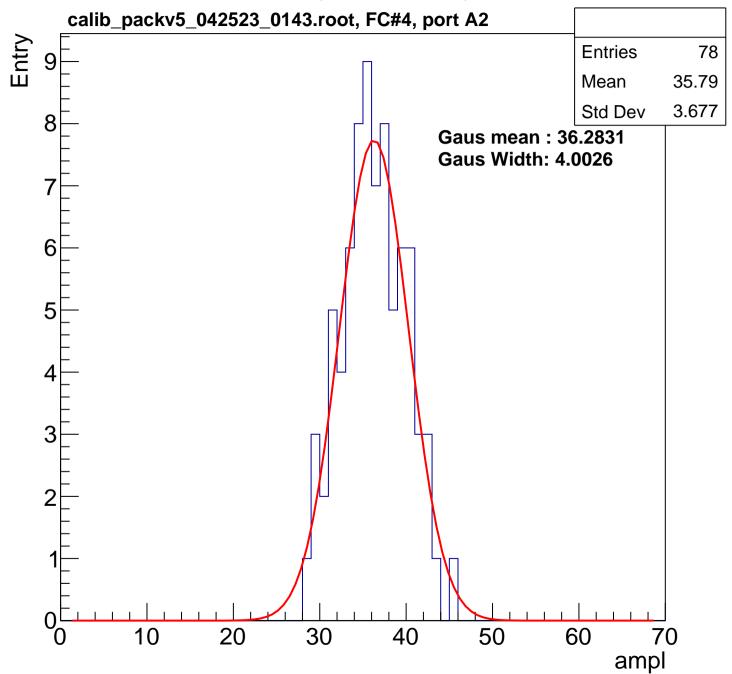


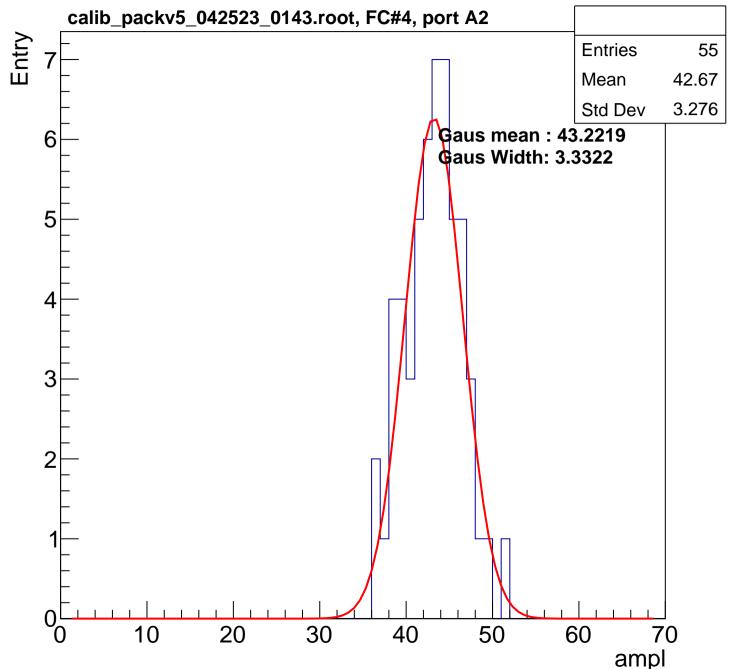


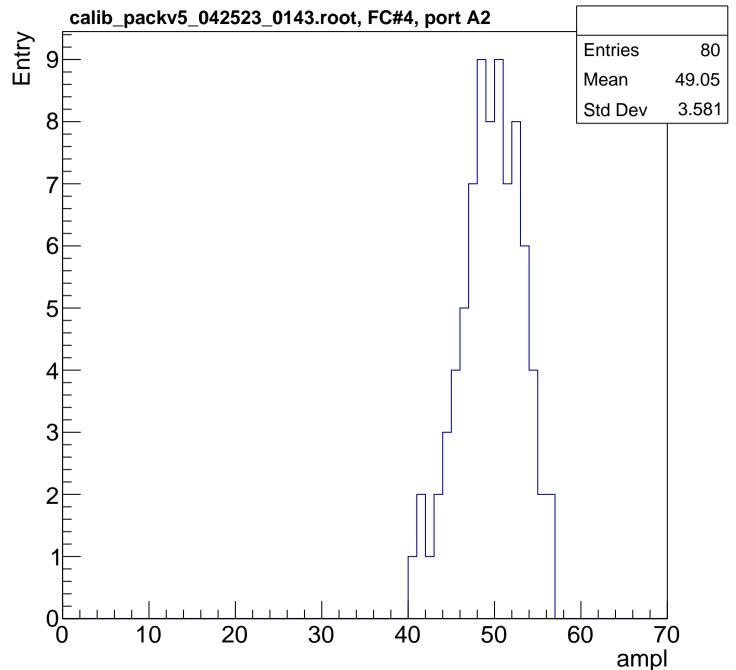


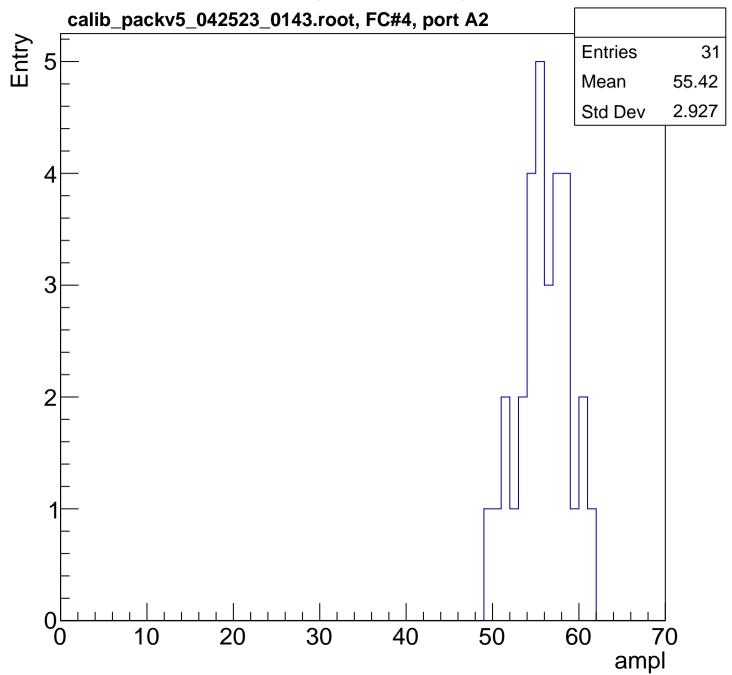


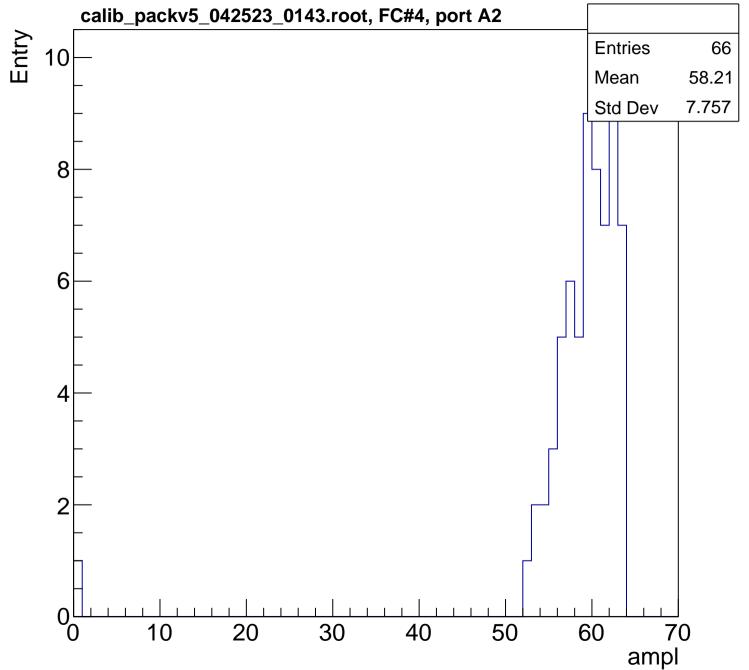


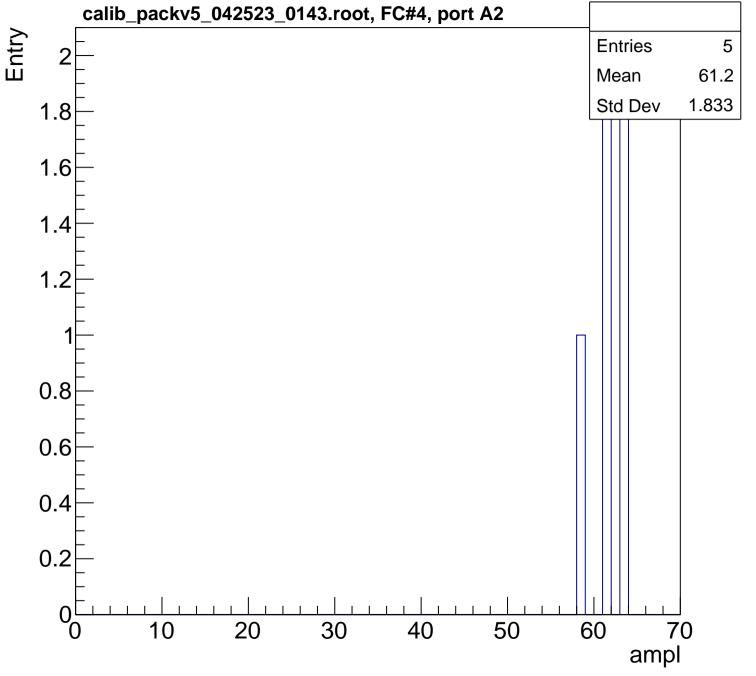


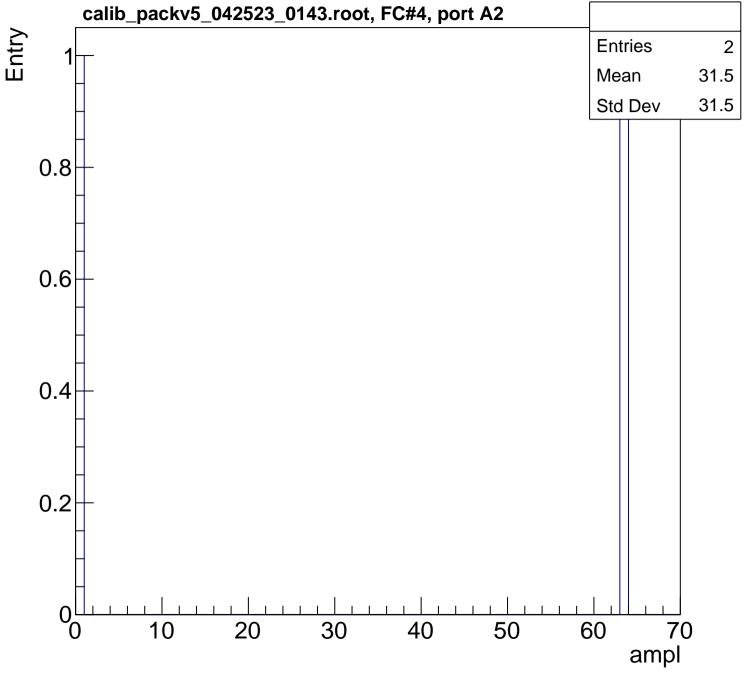


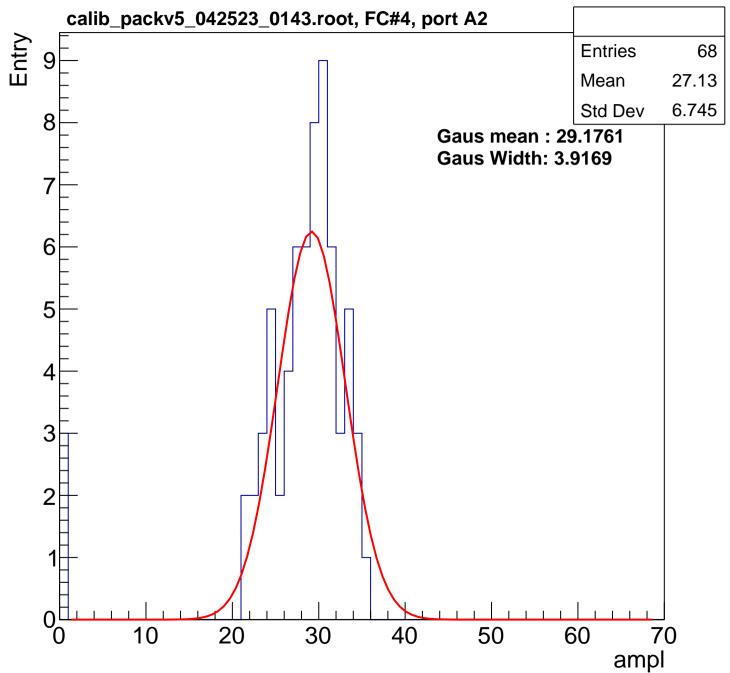


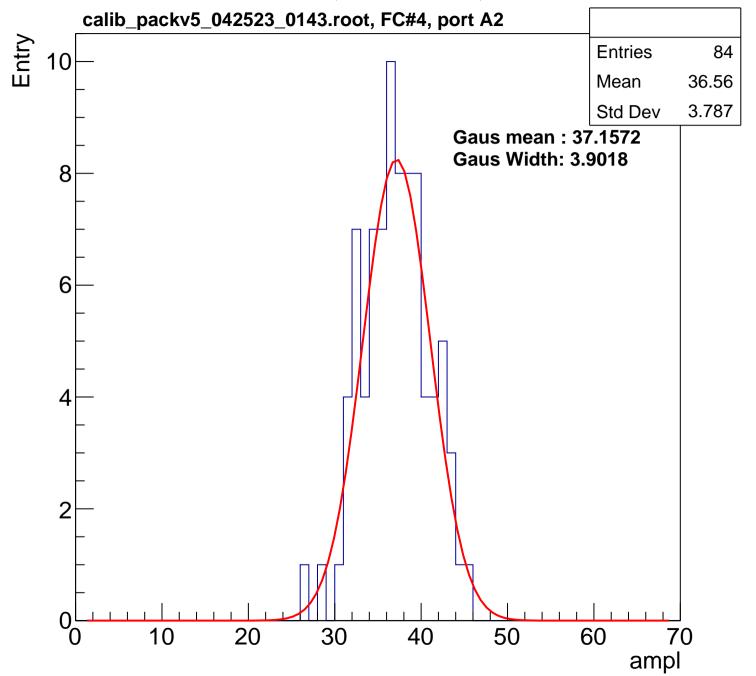


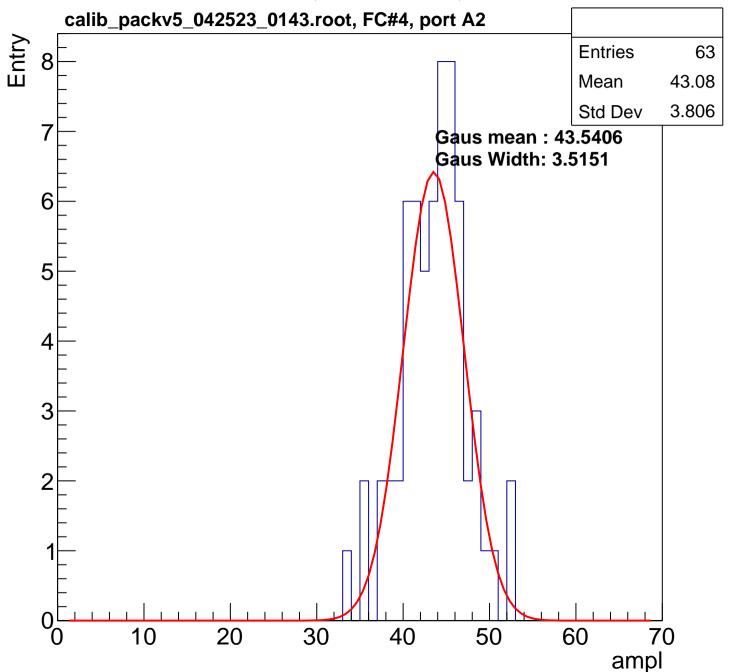


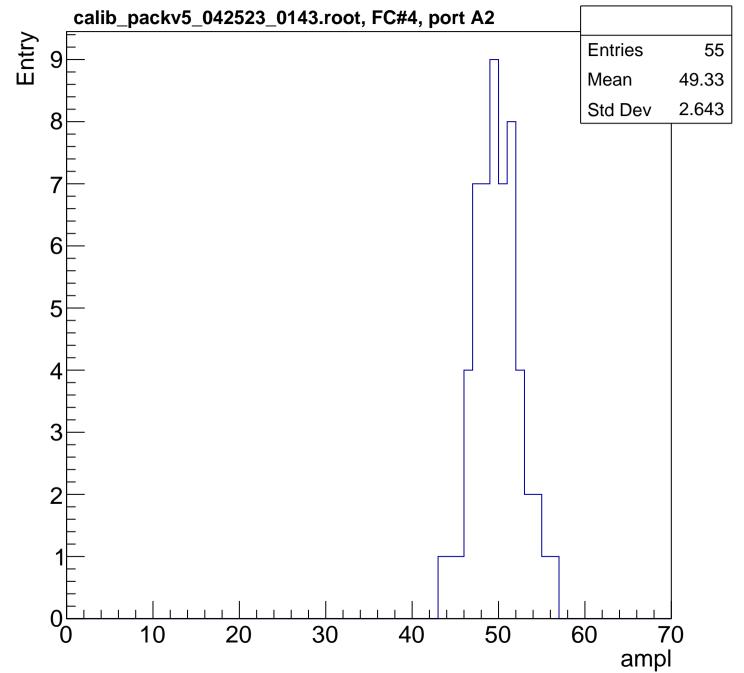


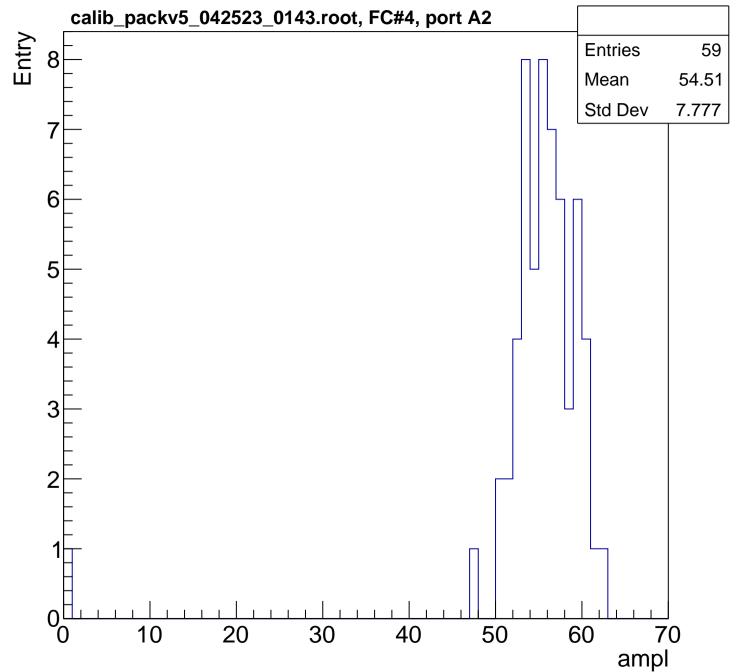


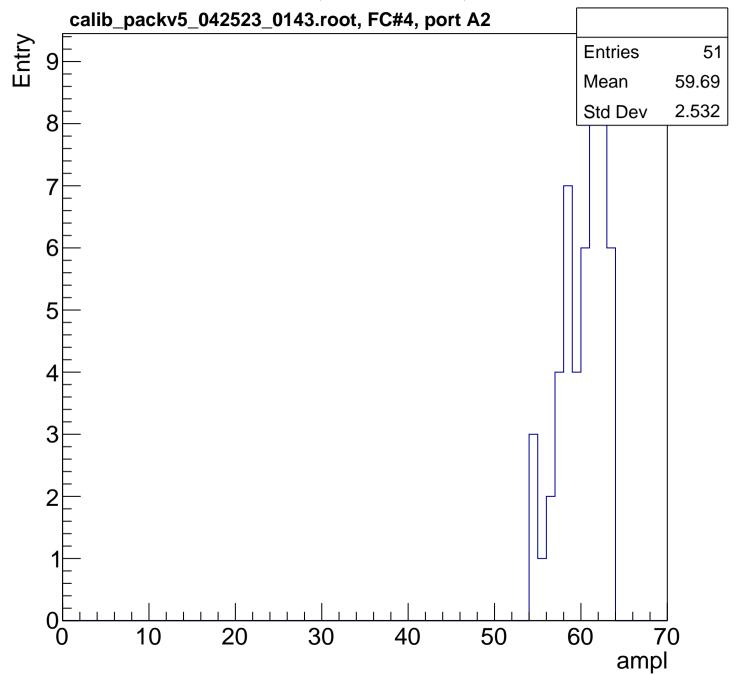


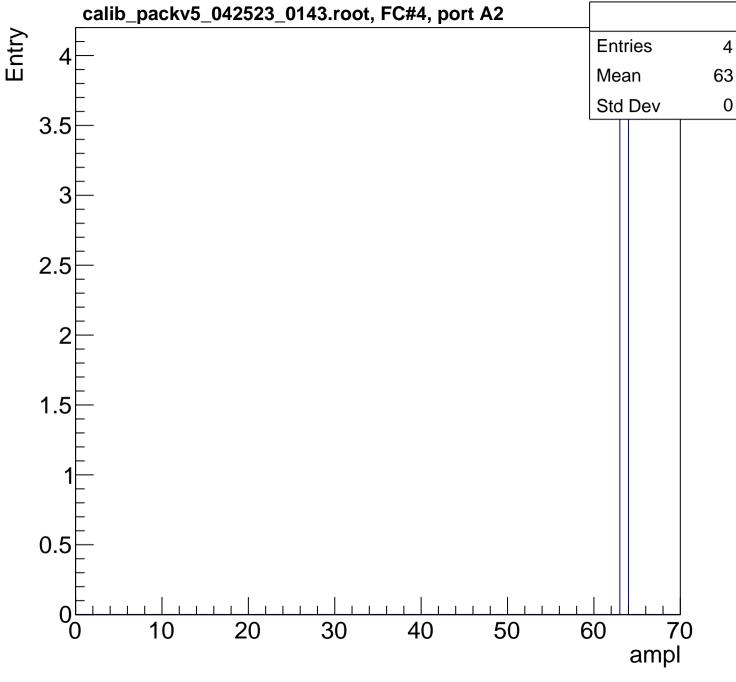


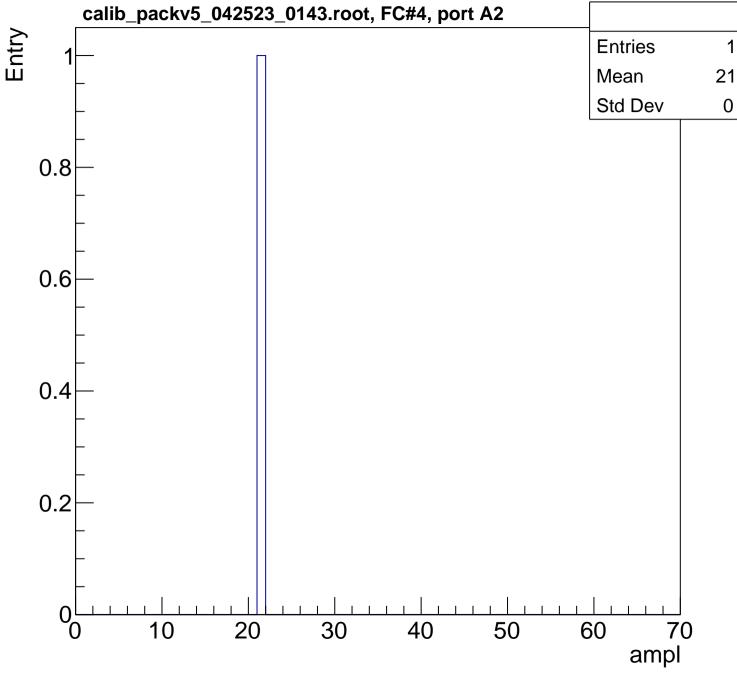


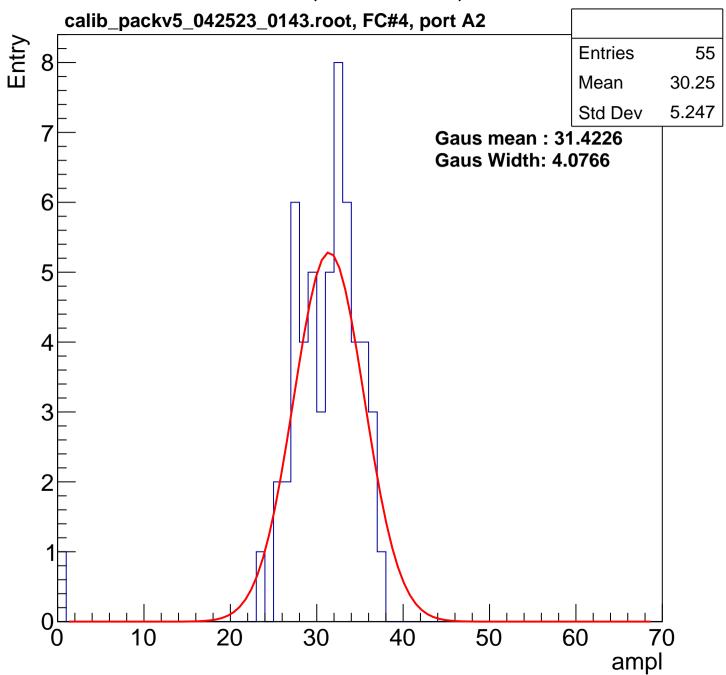


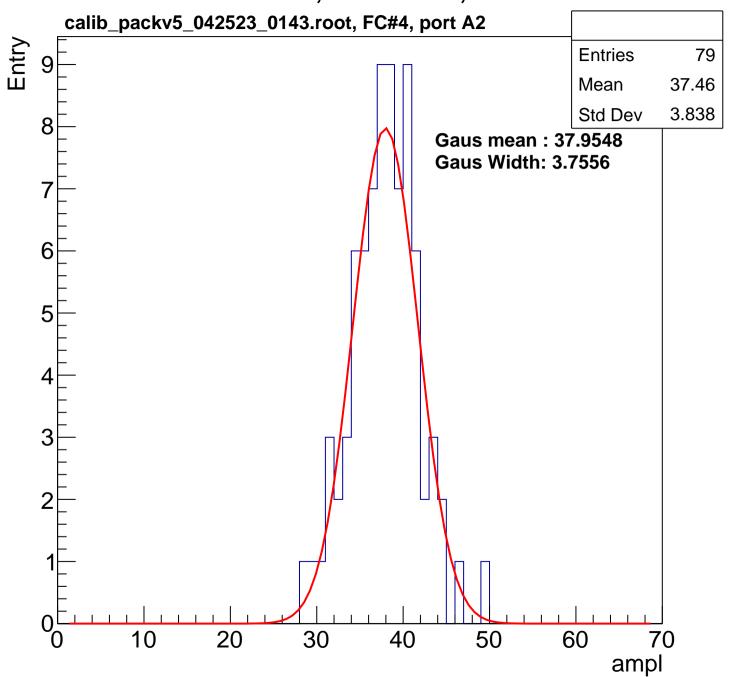


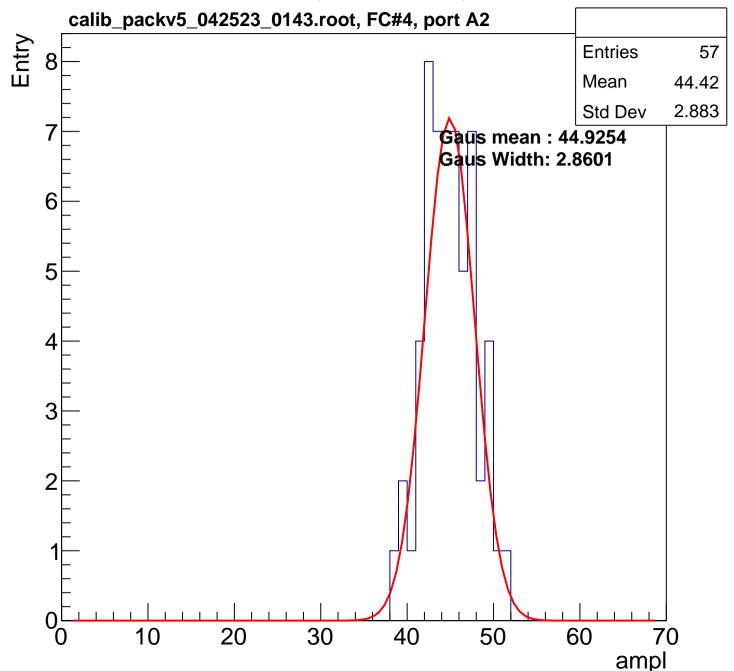


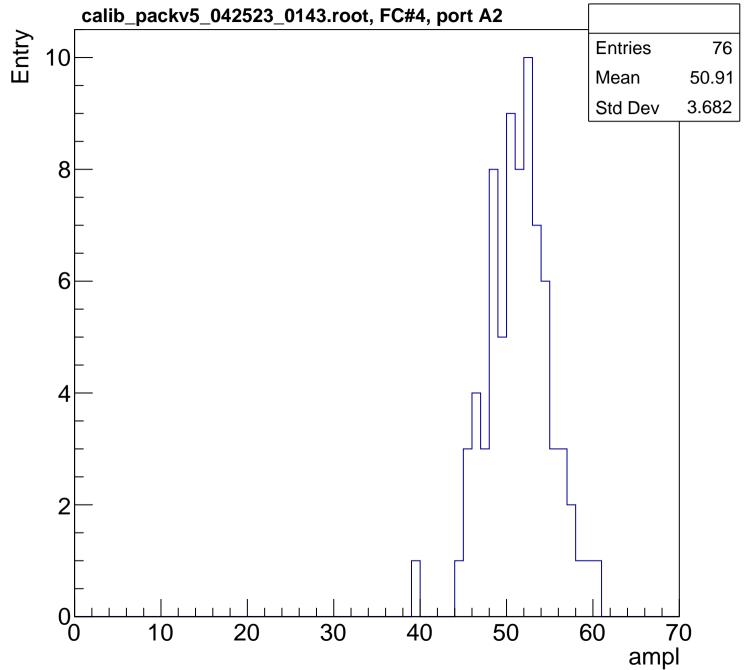


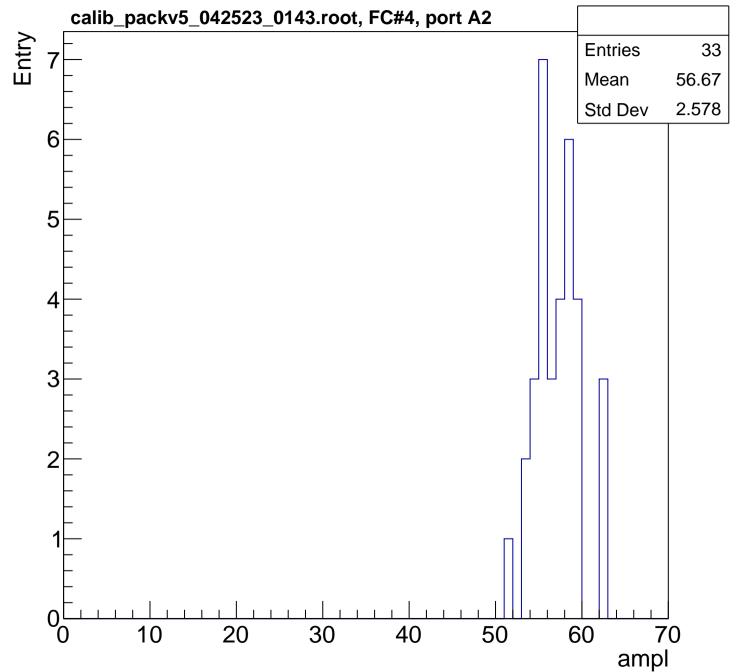


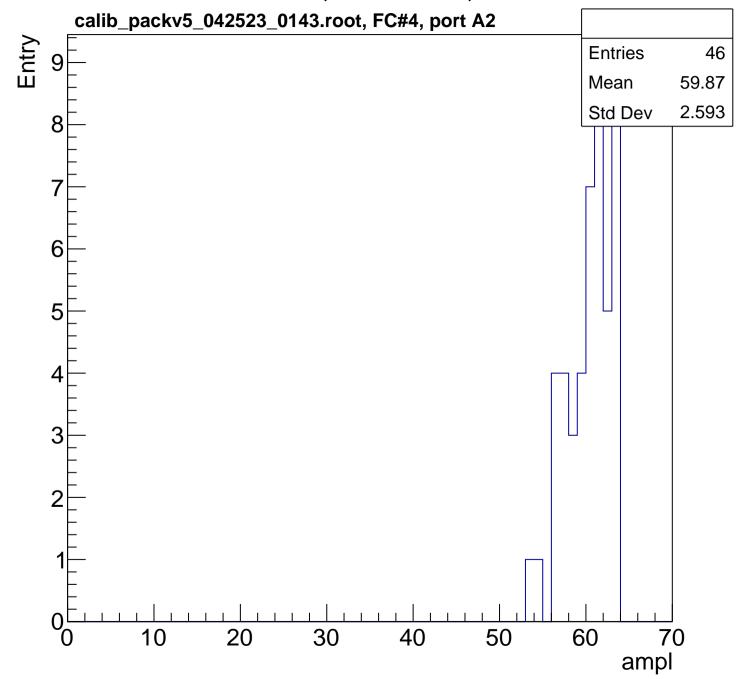


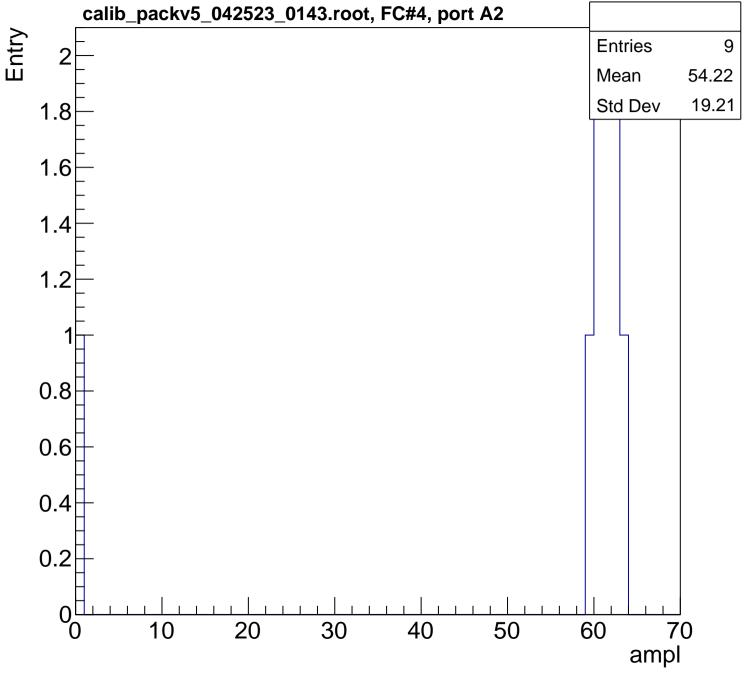




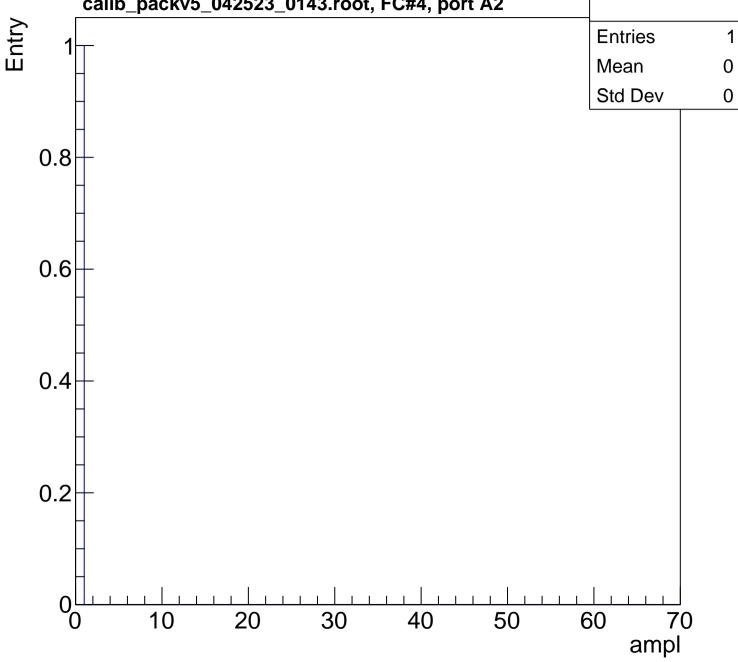


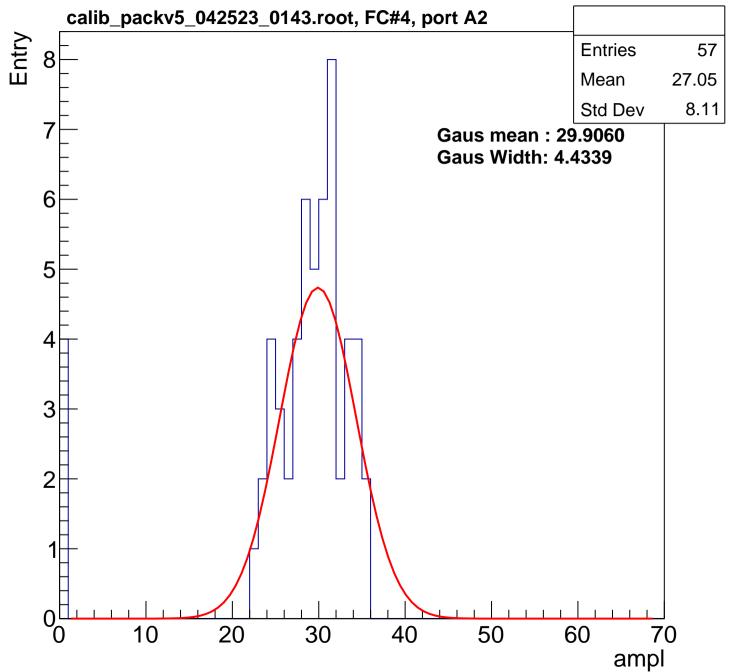


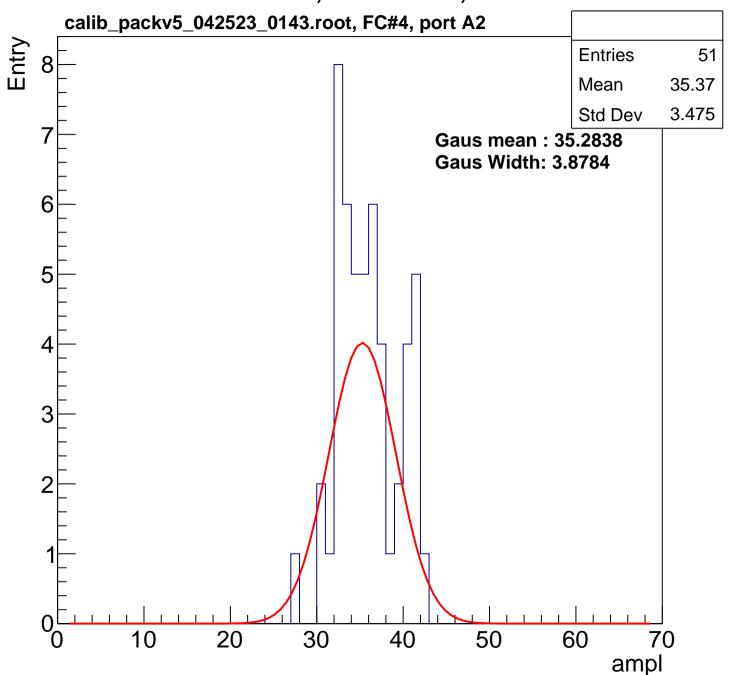


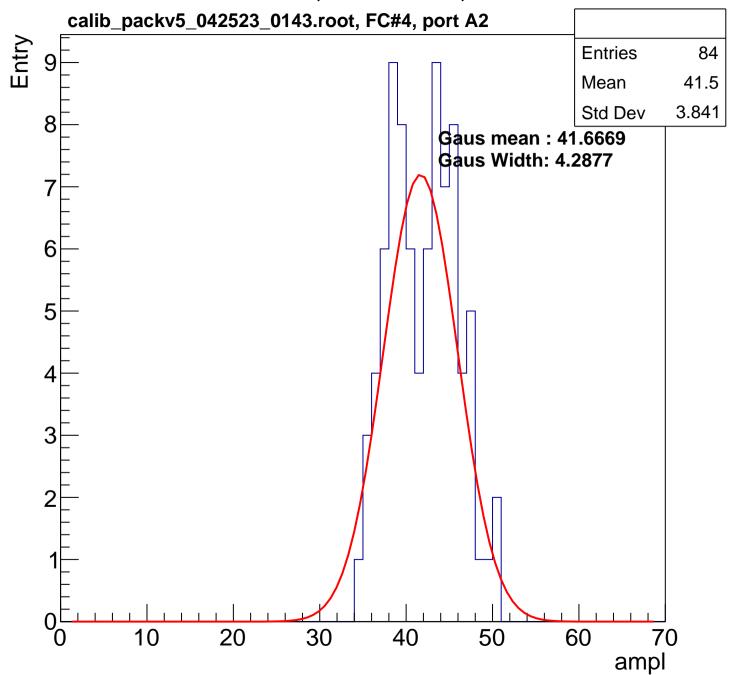


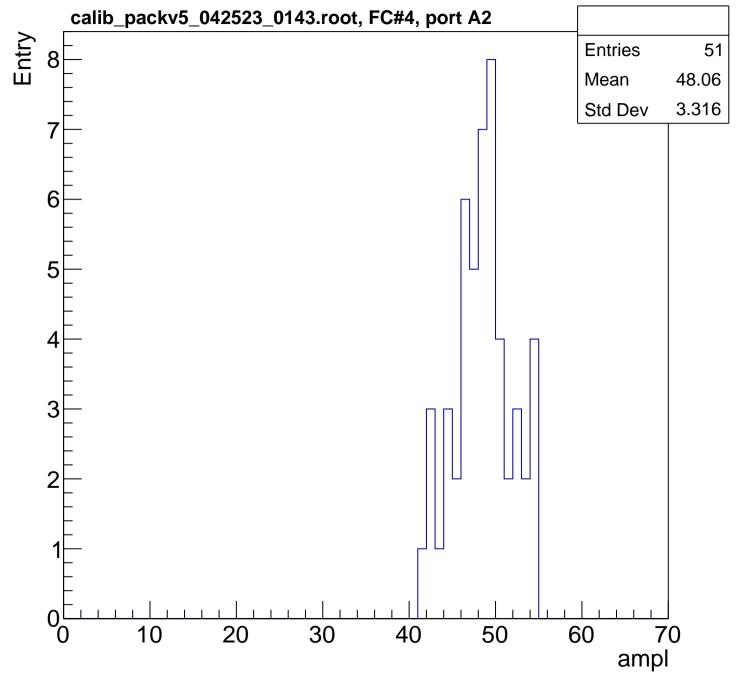
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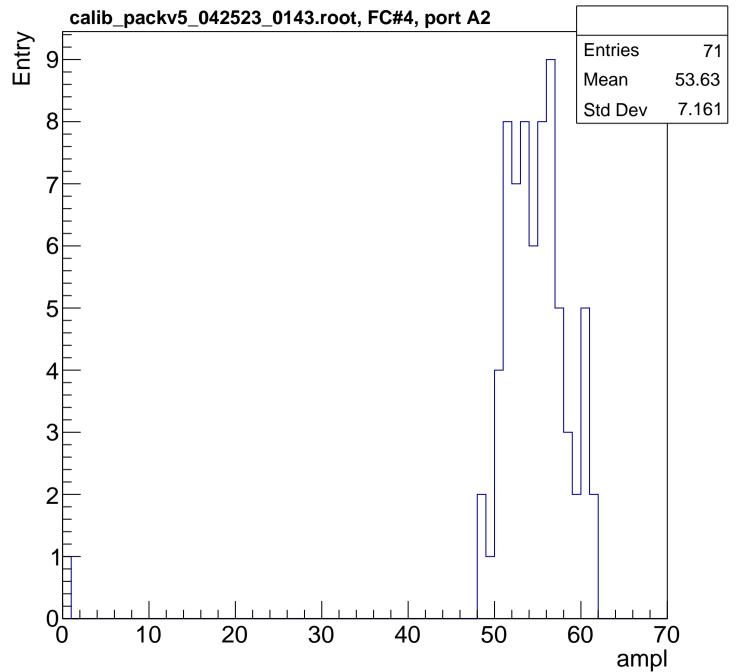


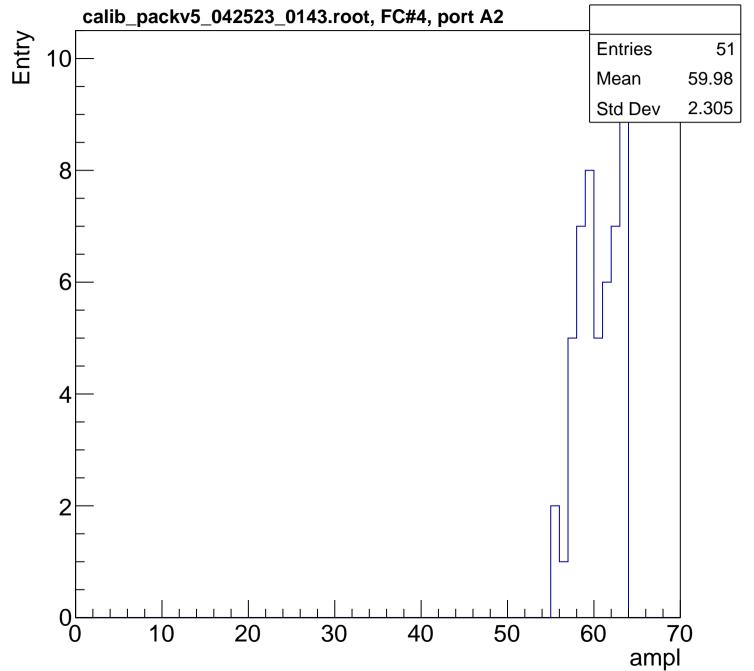


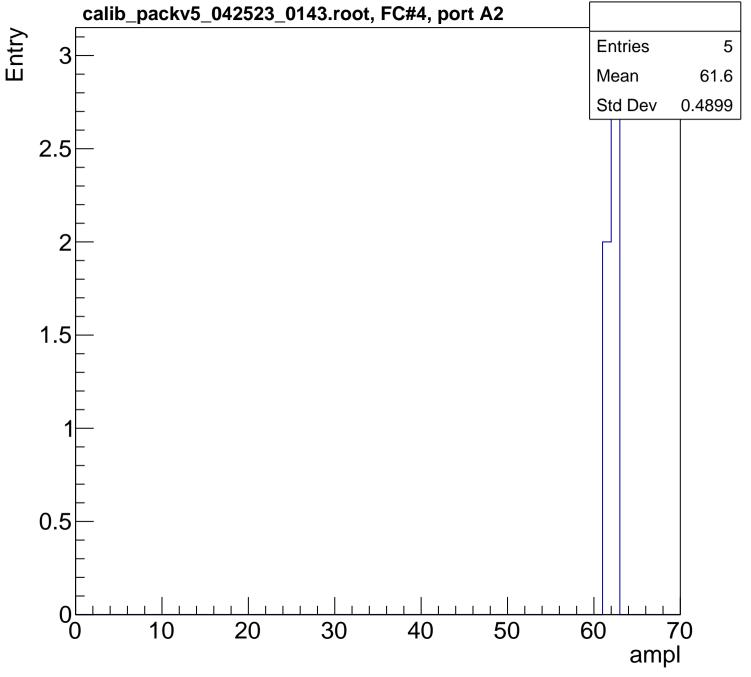




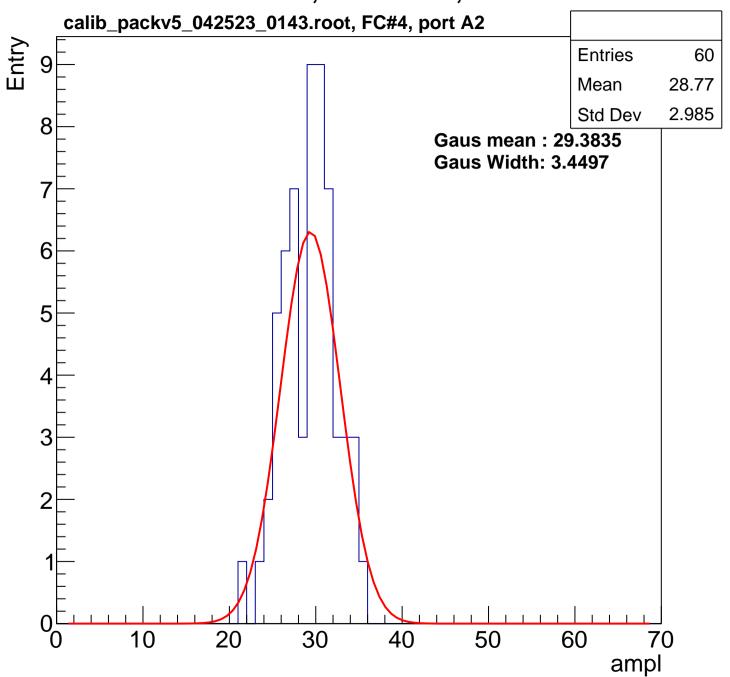


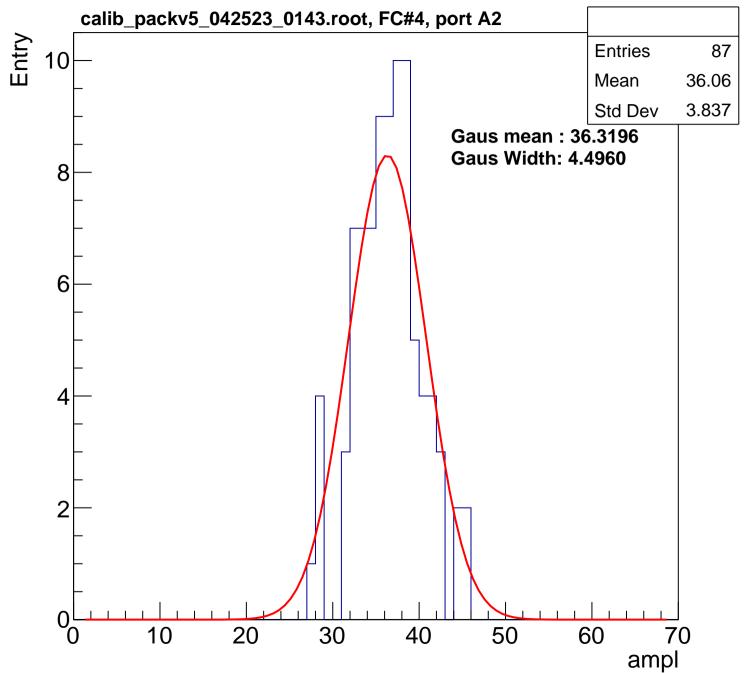


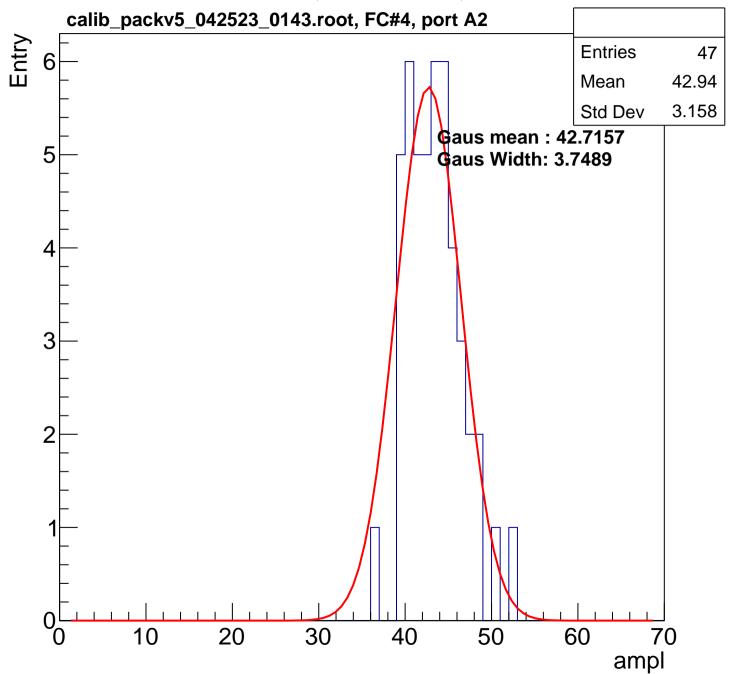


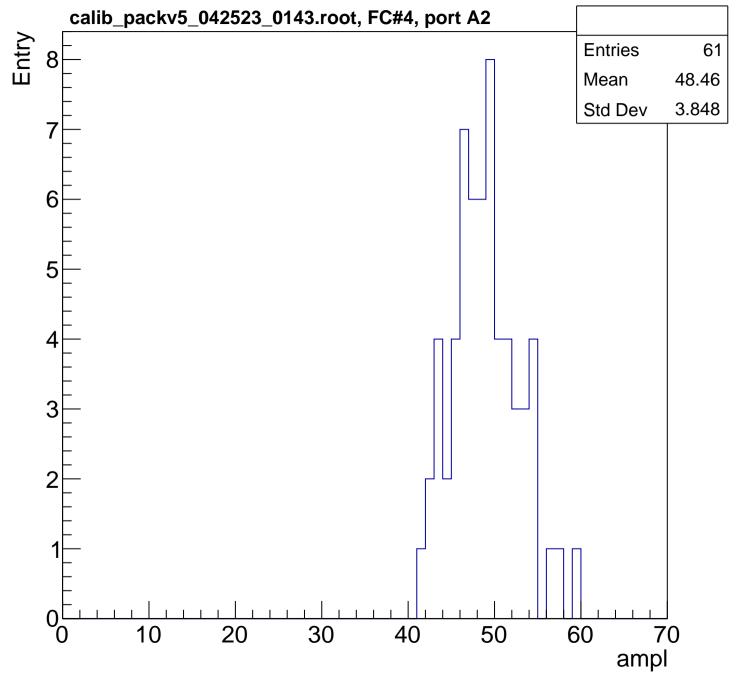


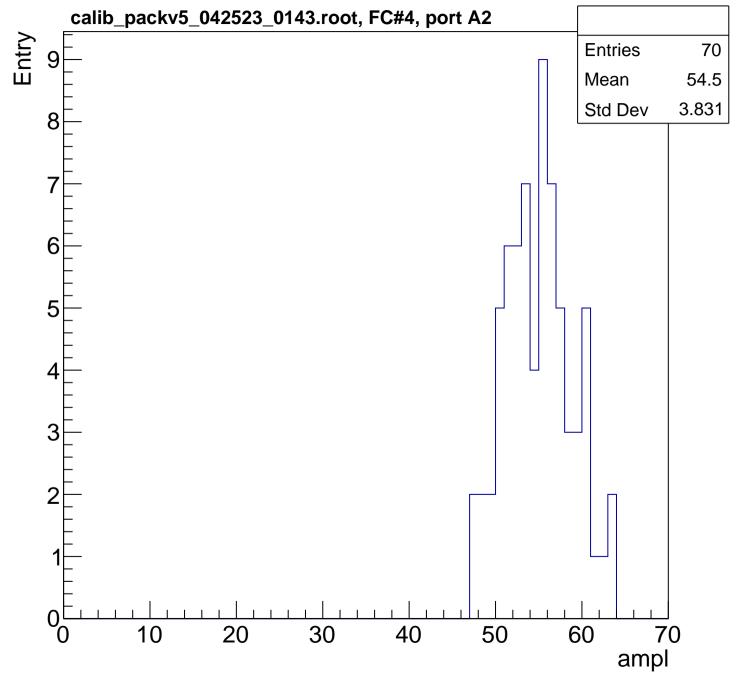


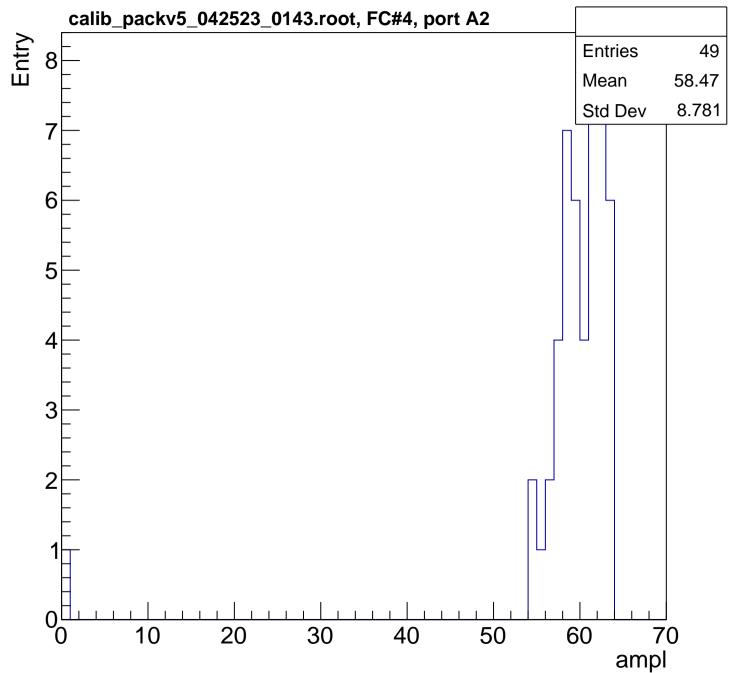


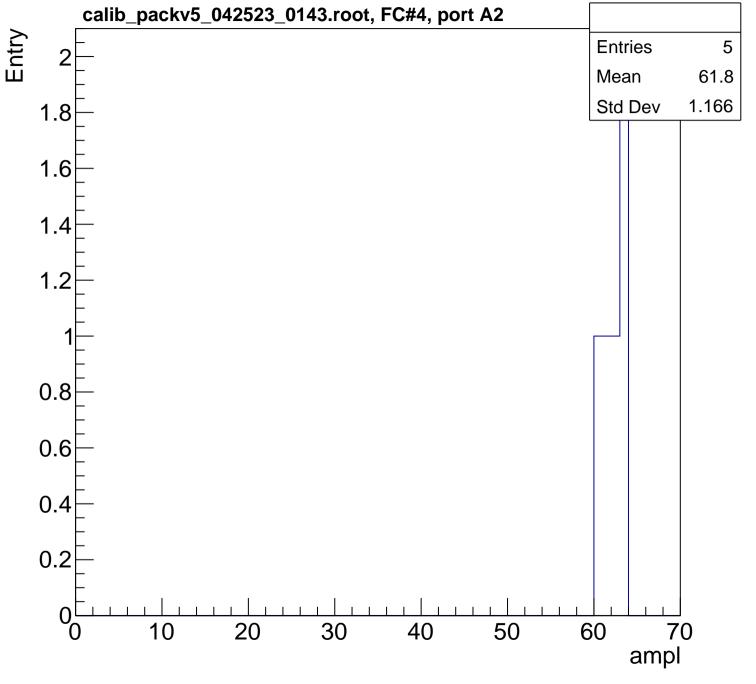




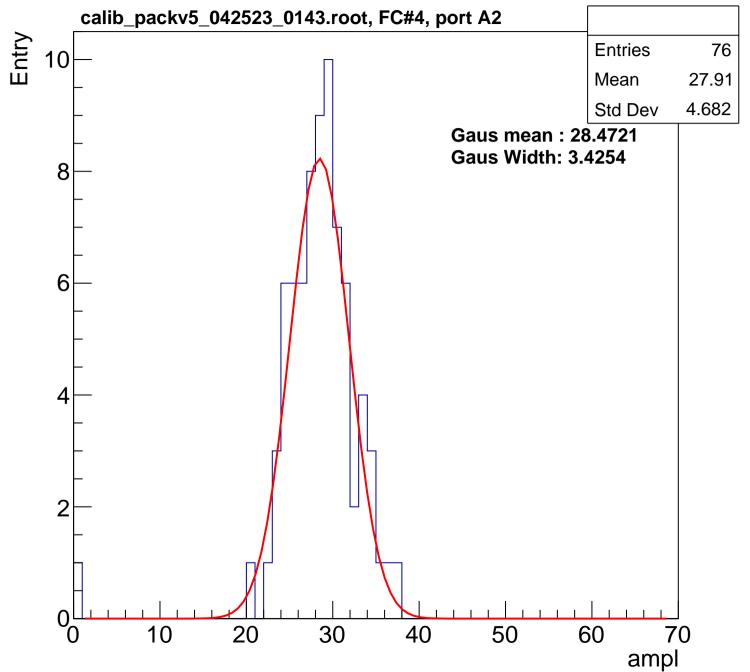


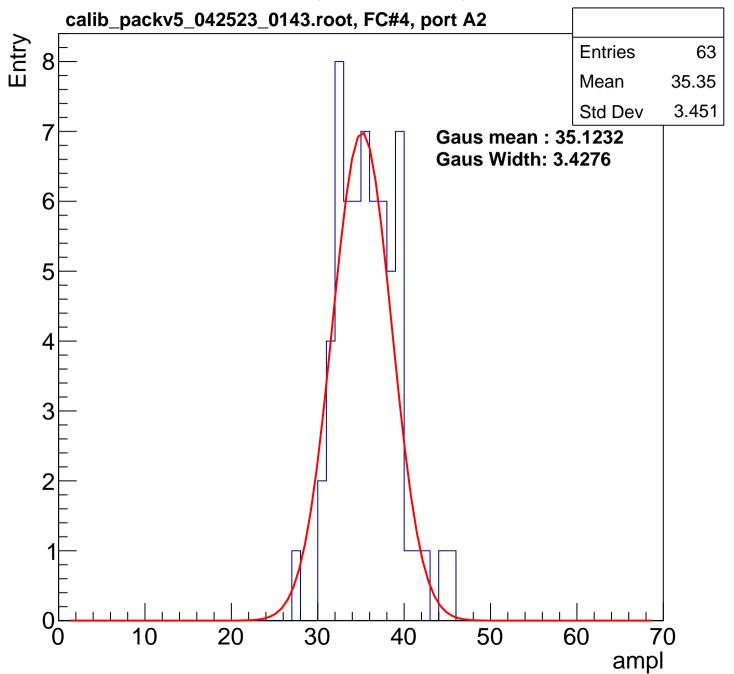


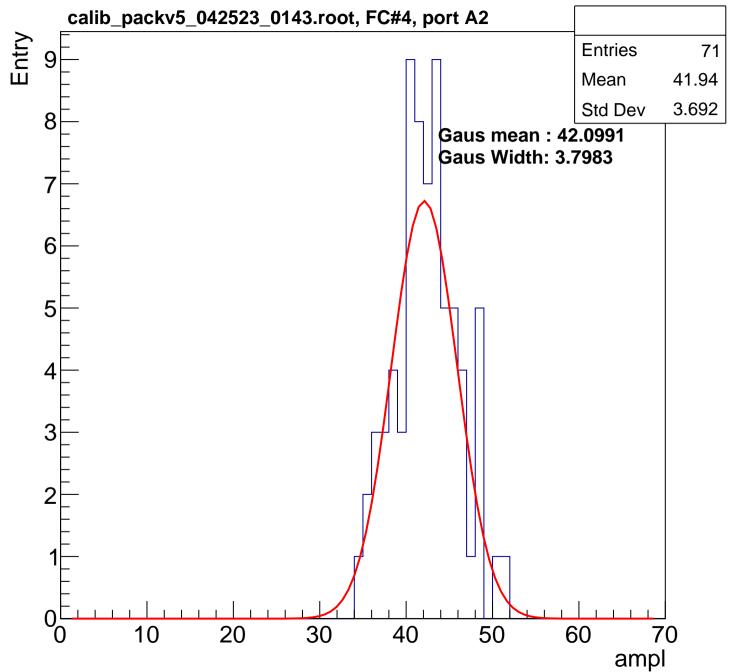


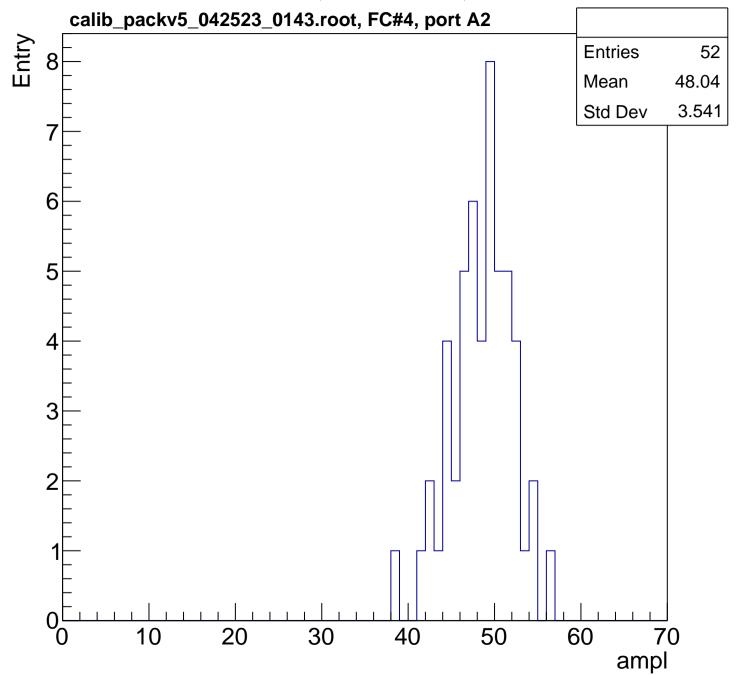


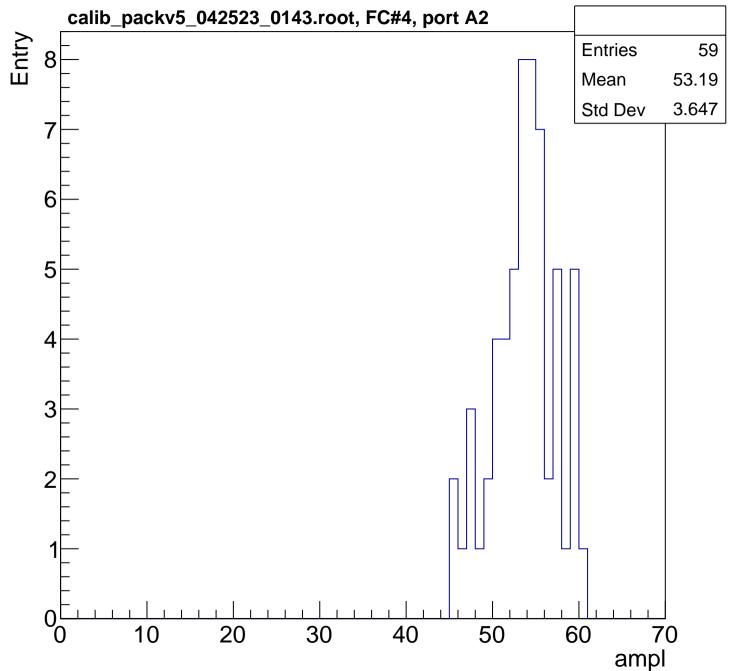


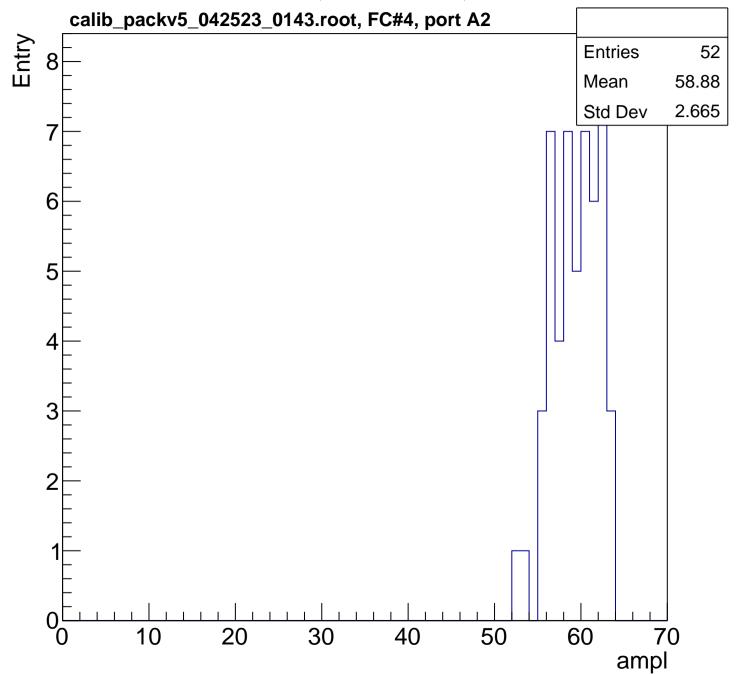


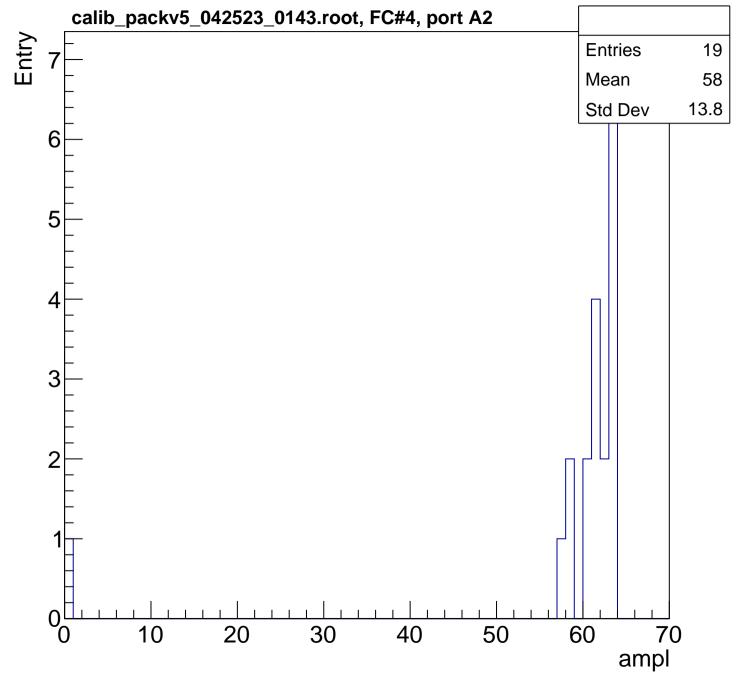




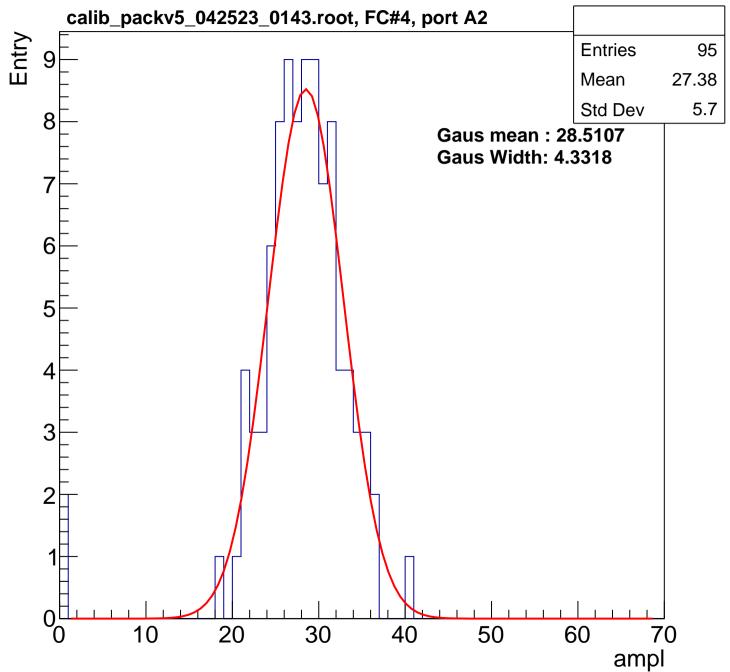


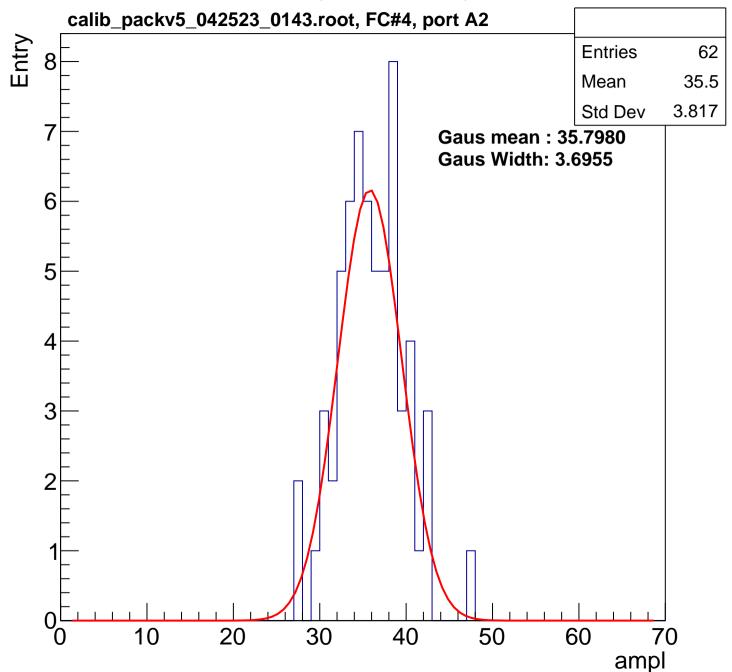


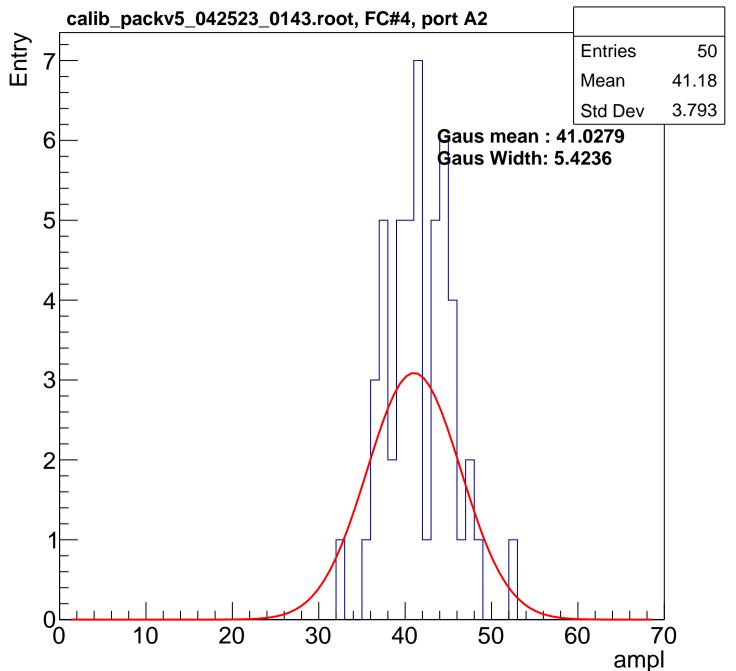


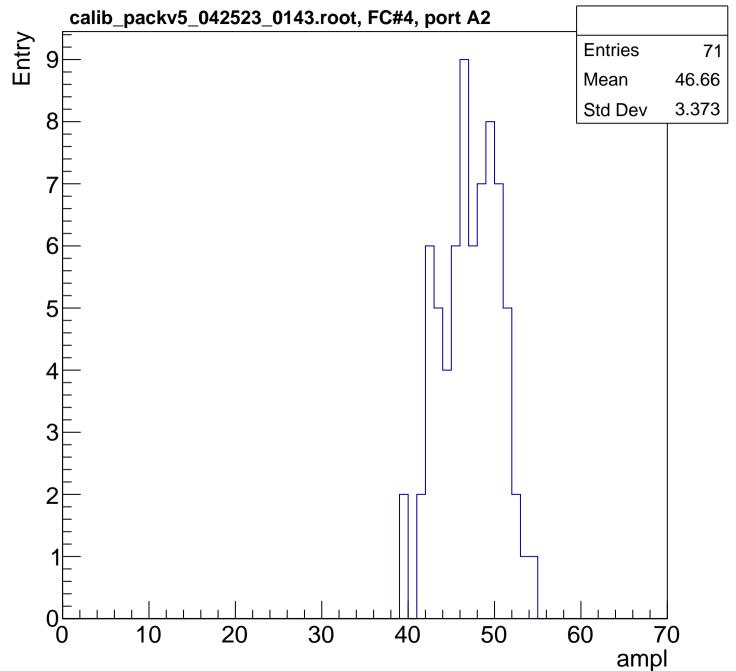


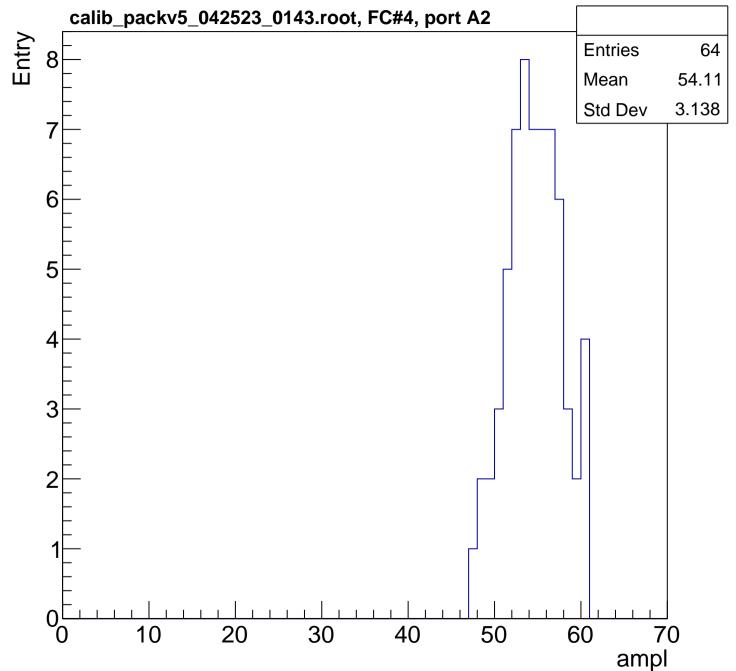


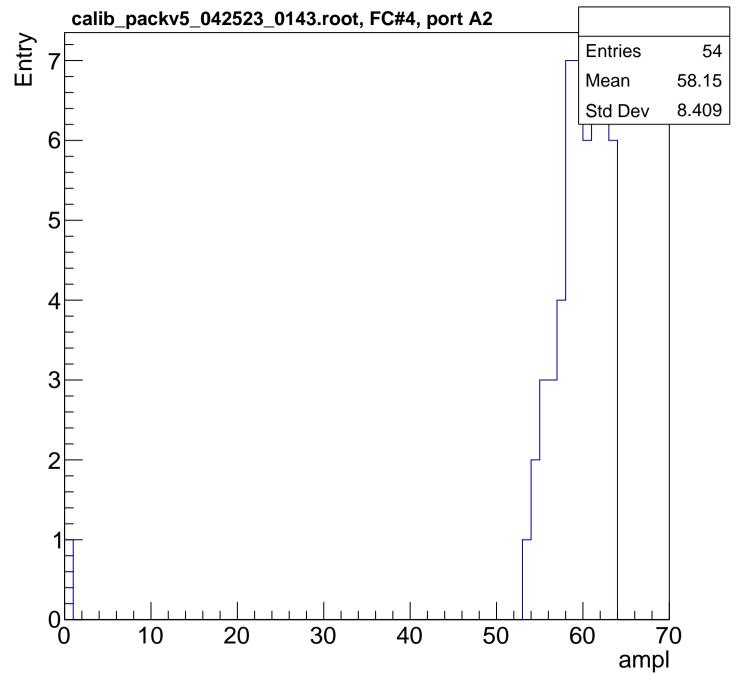


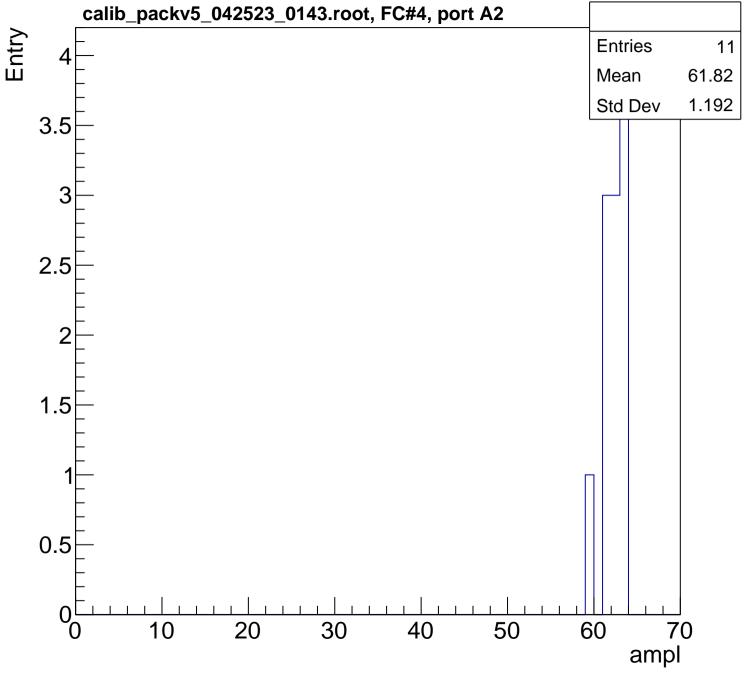




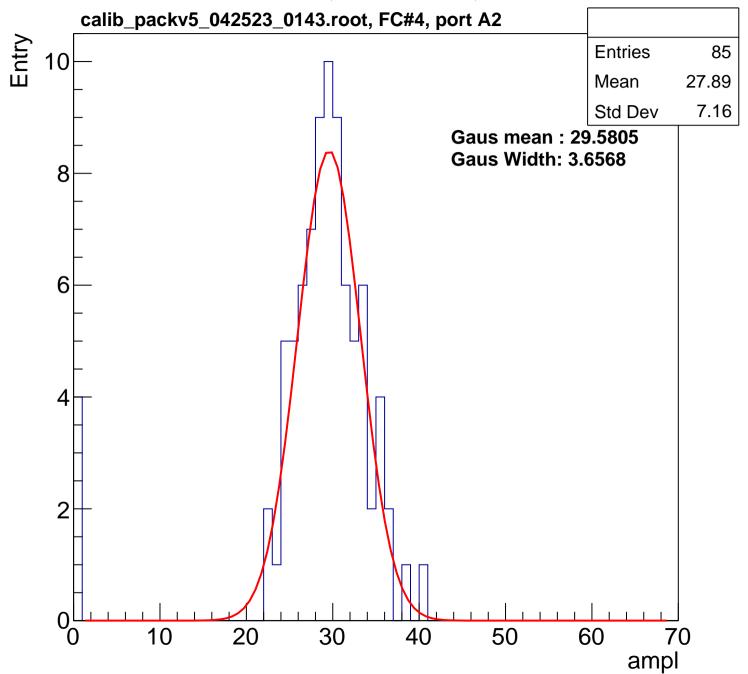


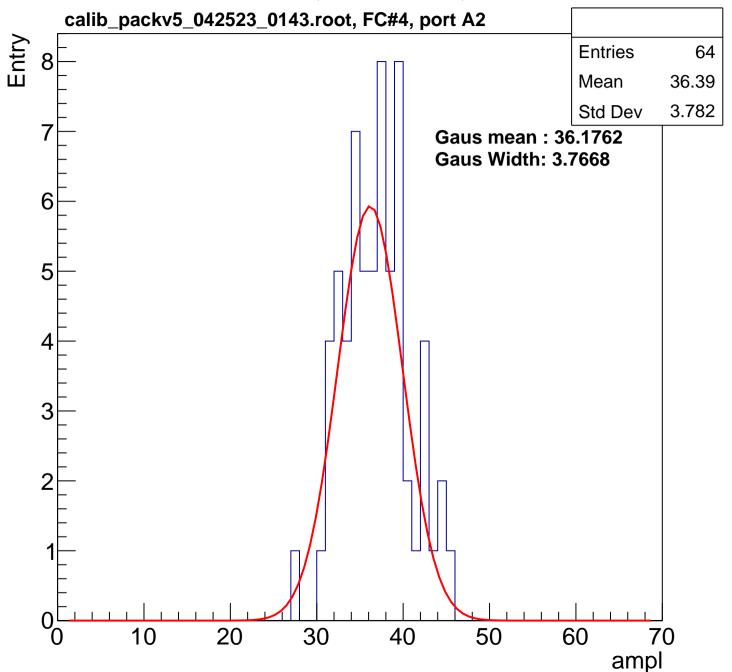


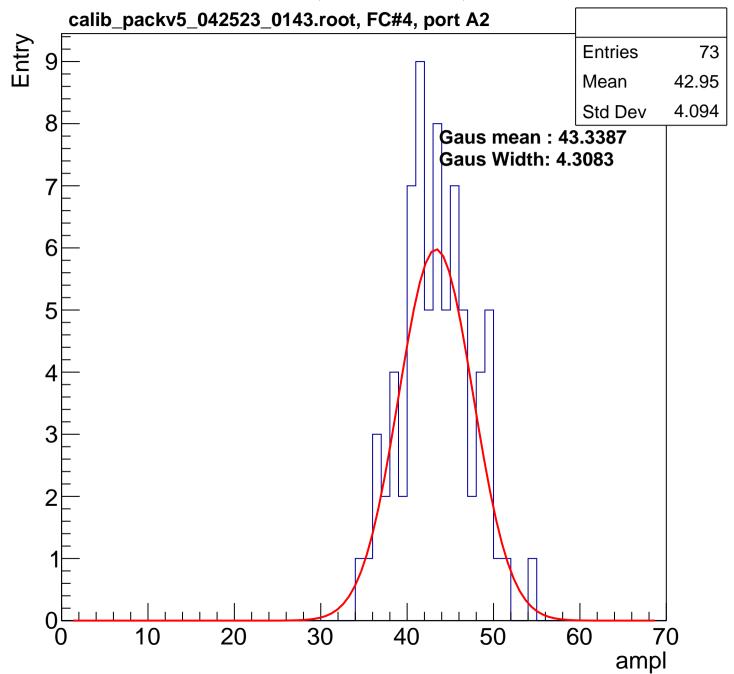


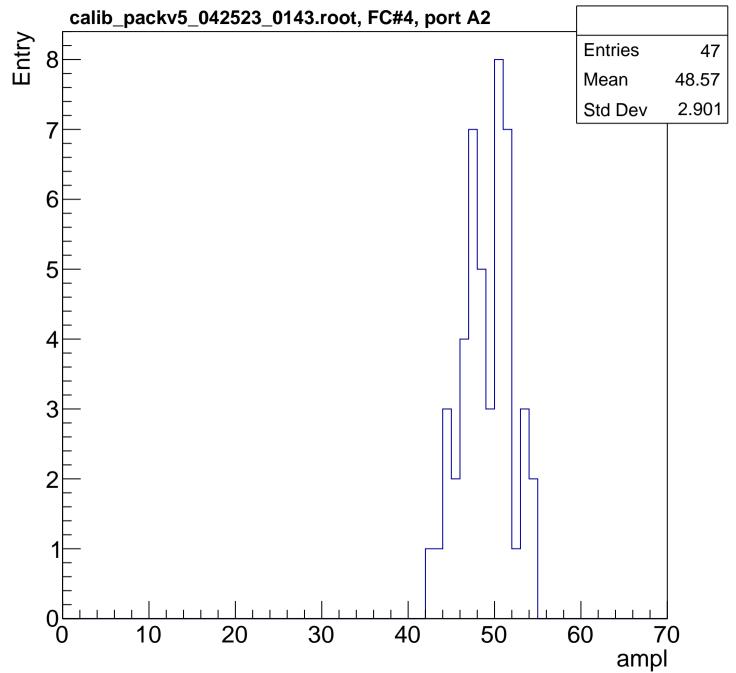


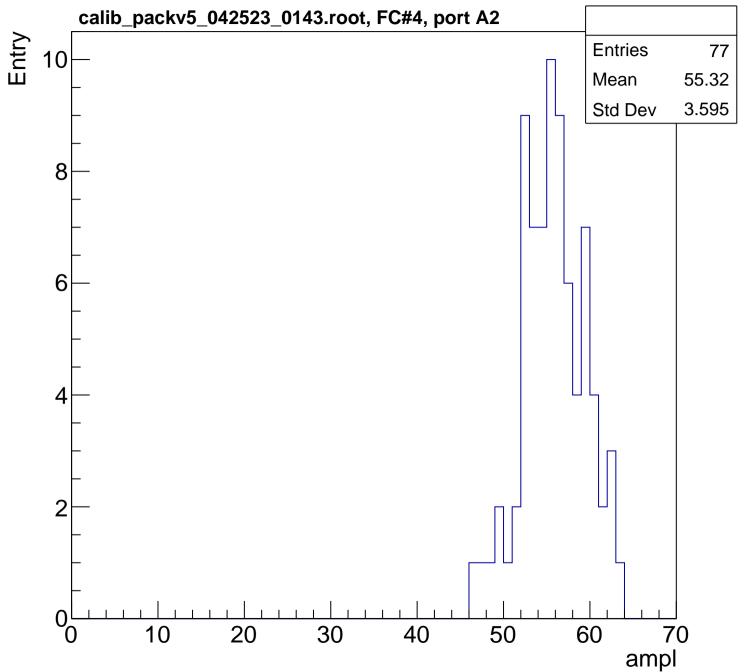


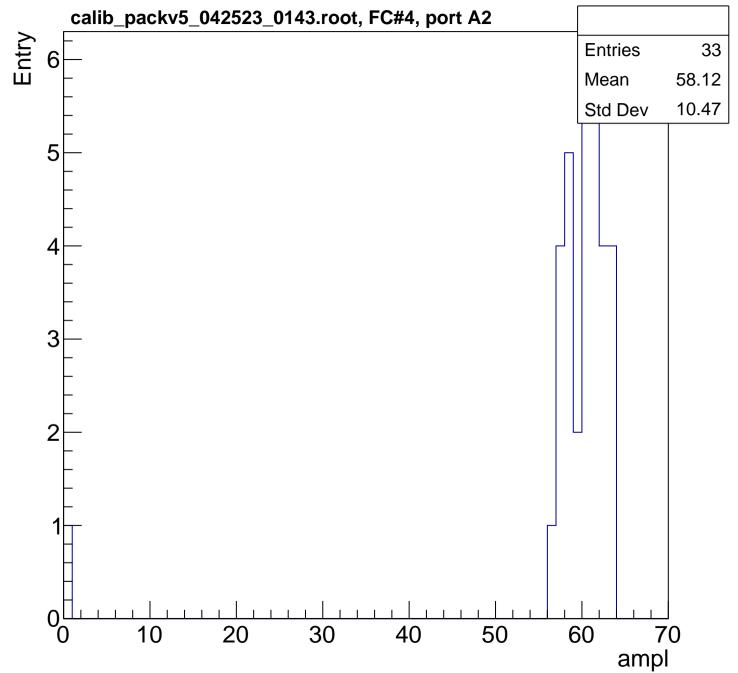


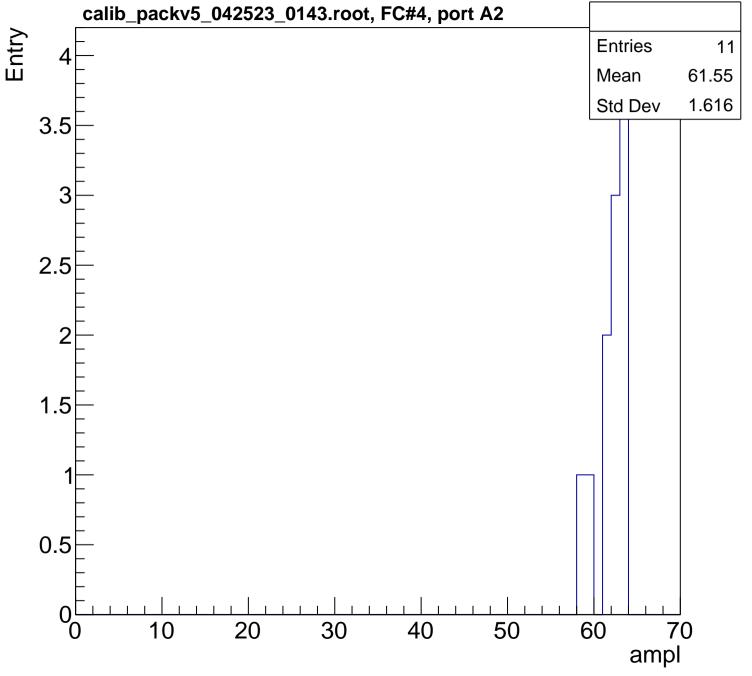


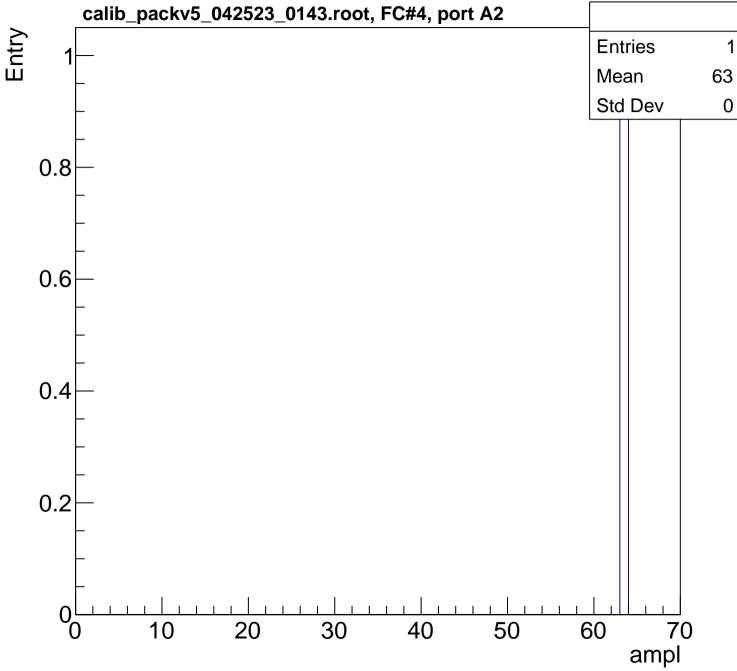


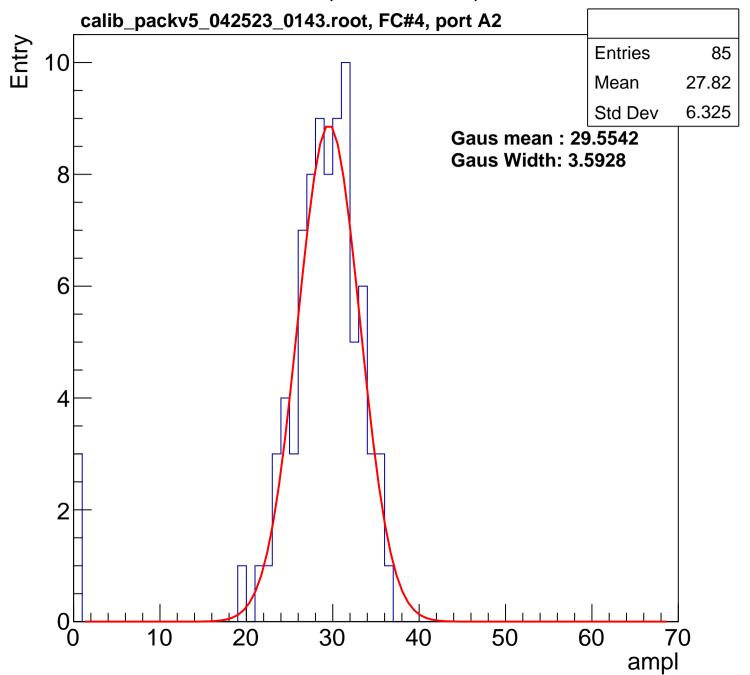


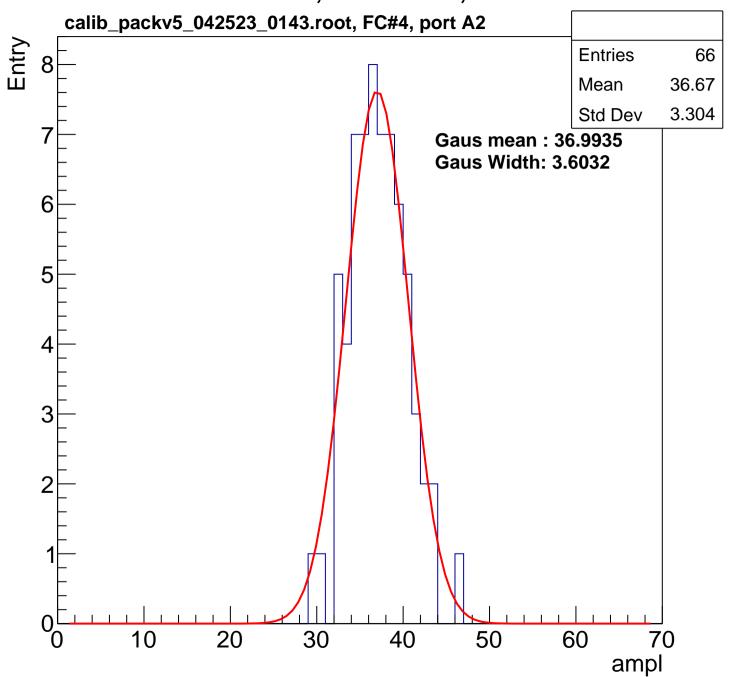


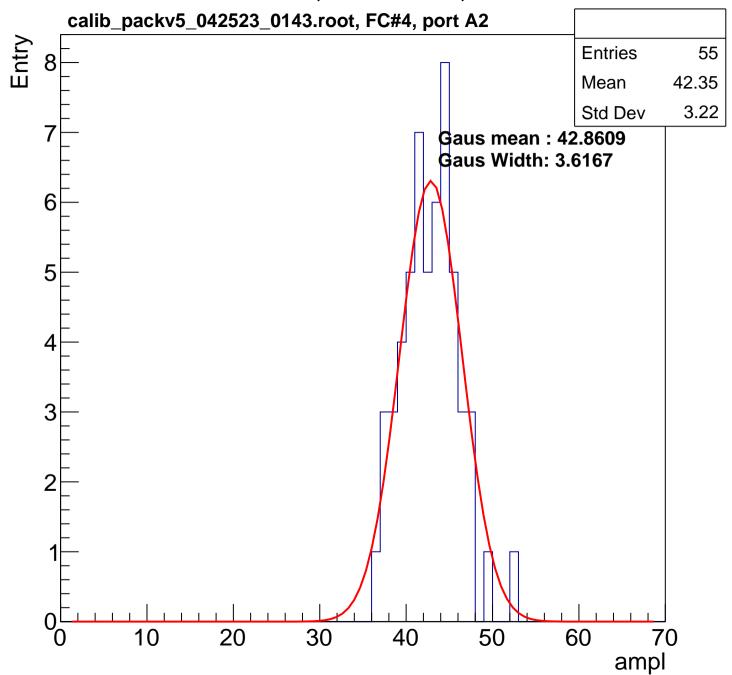


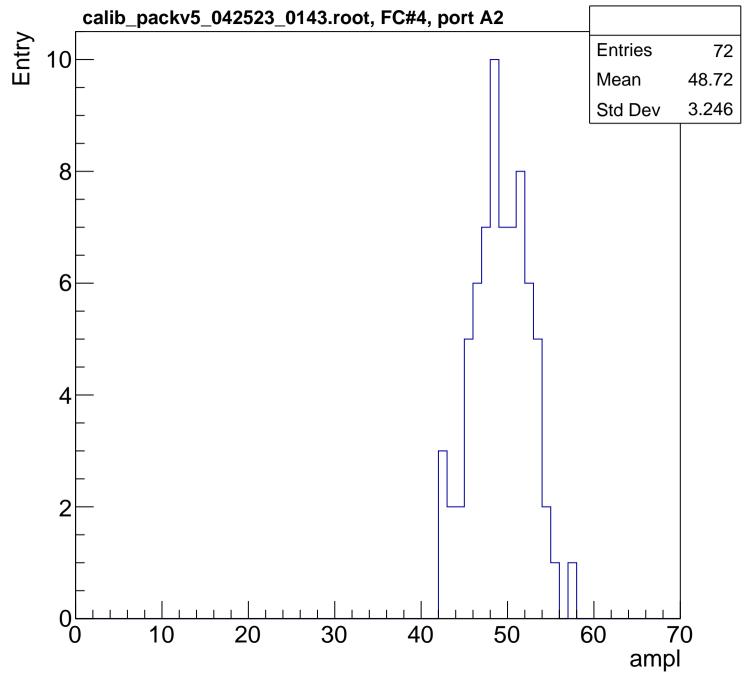


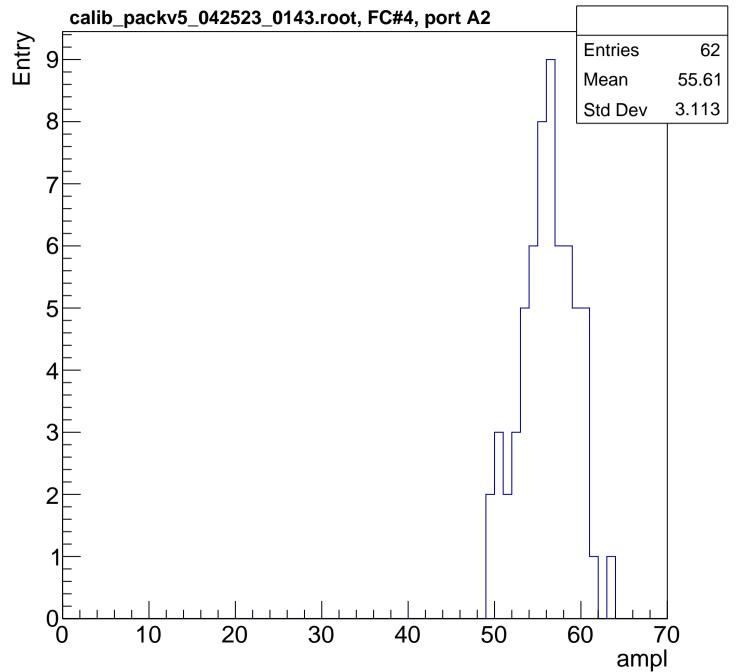


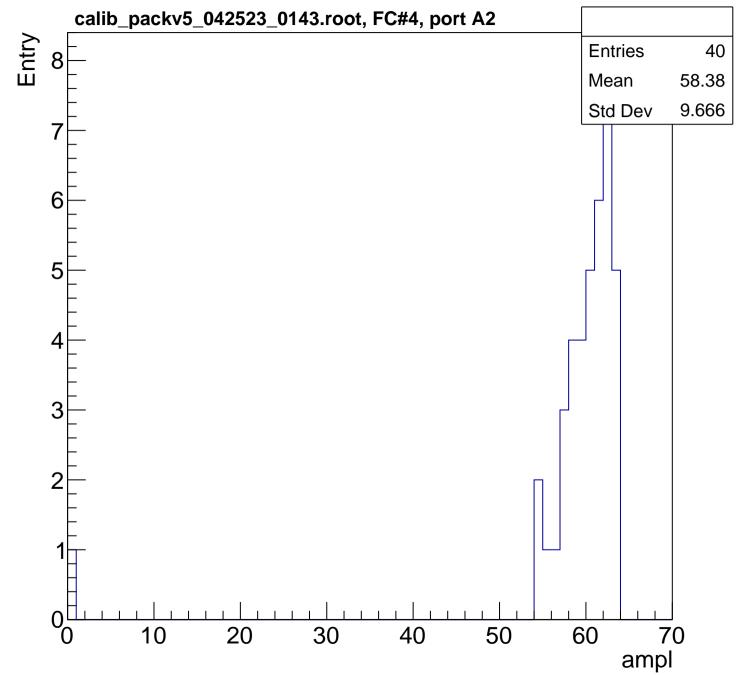


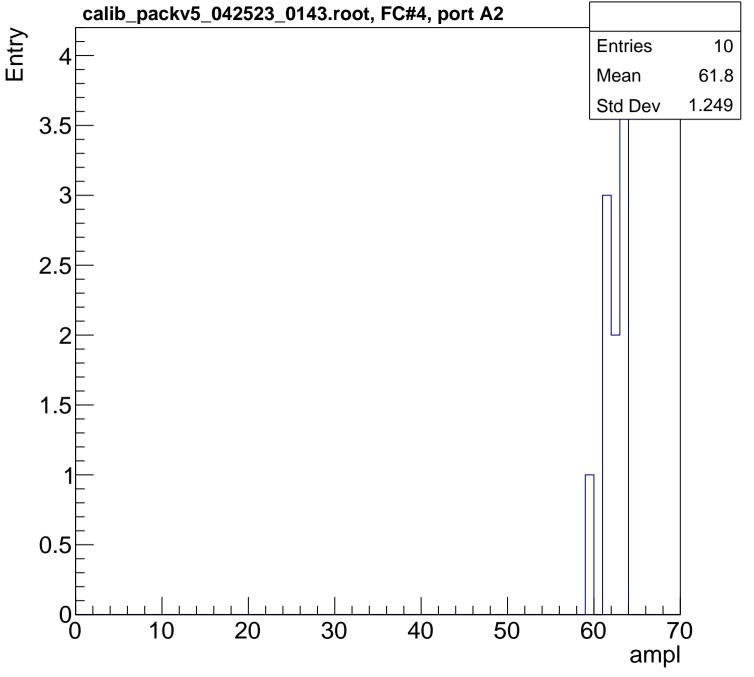




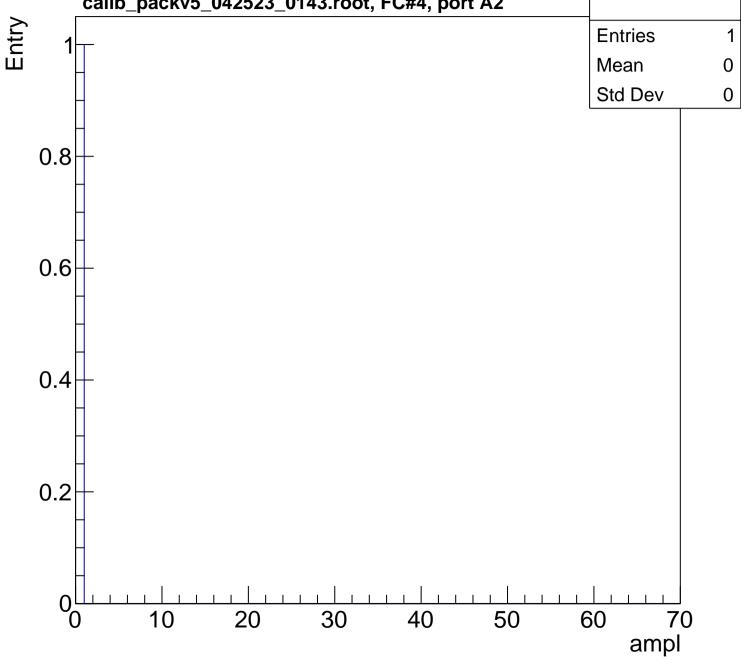


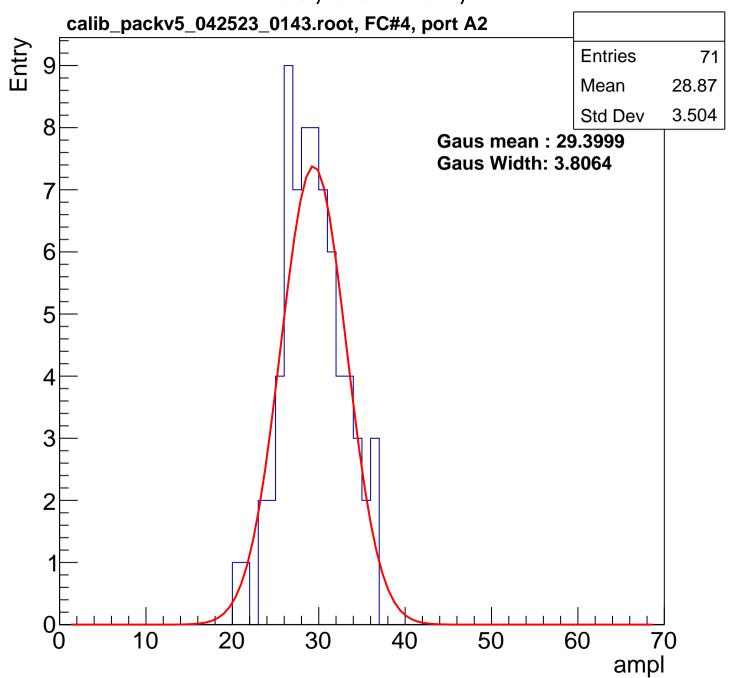


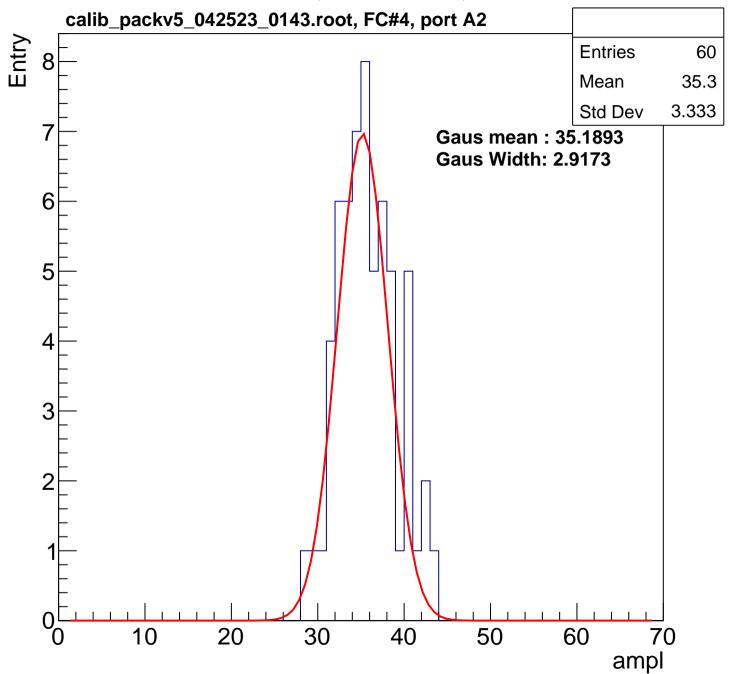


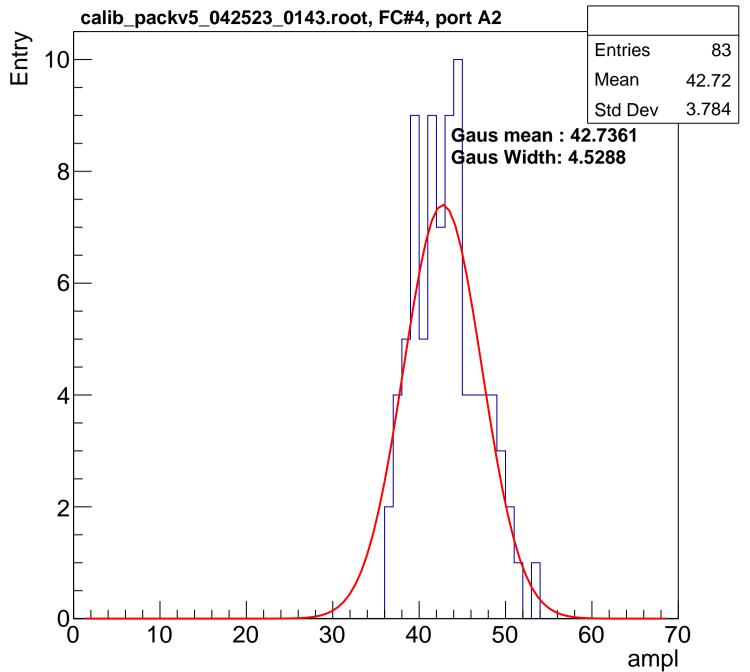


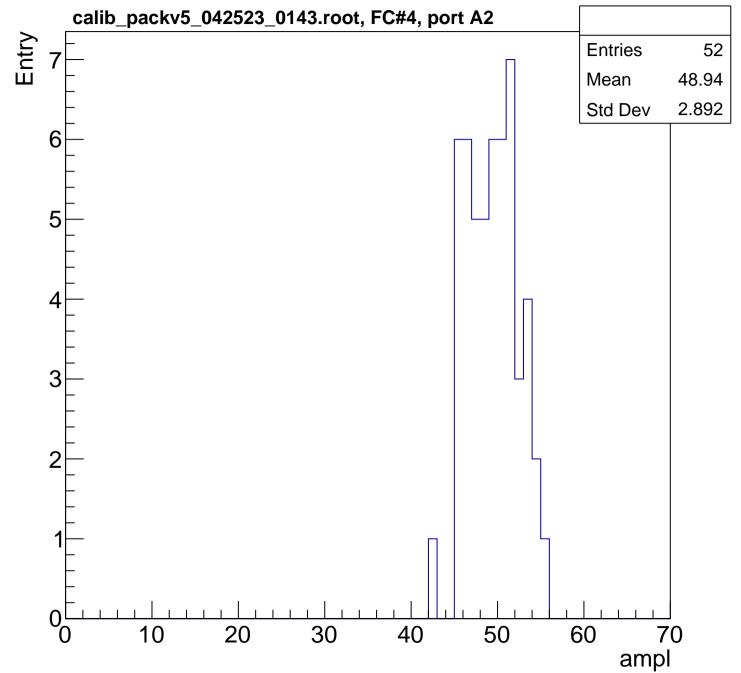
B1L100S, U3-ch61, adc7 calib_packv5_042523_0143.root, FC#4, port A2

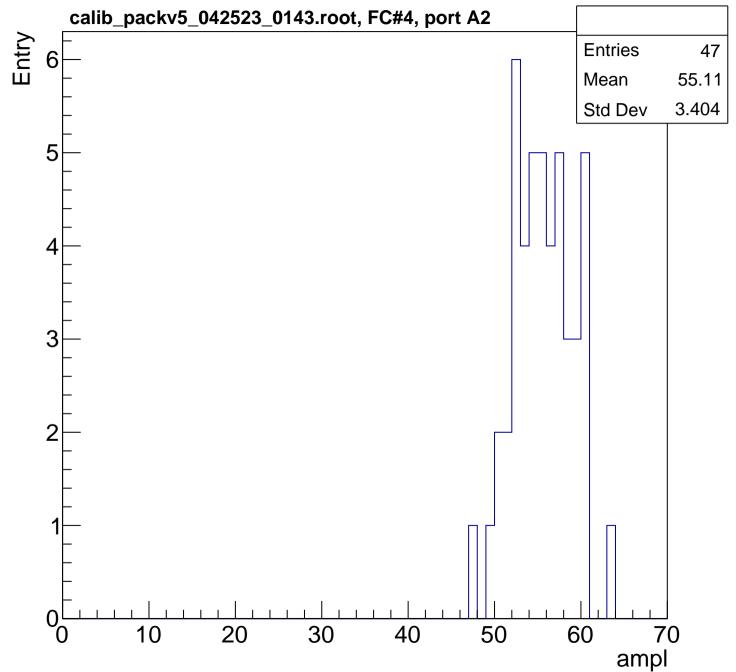


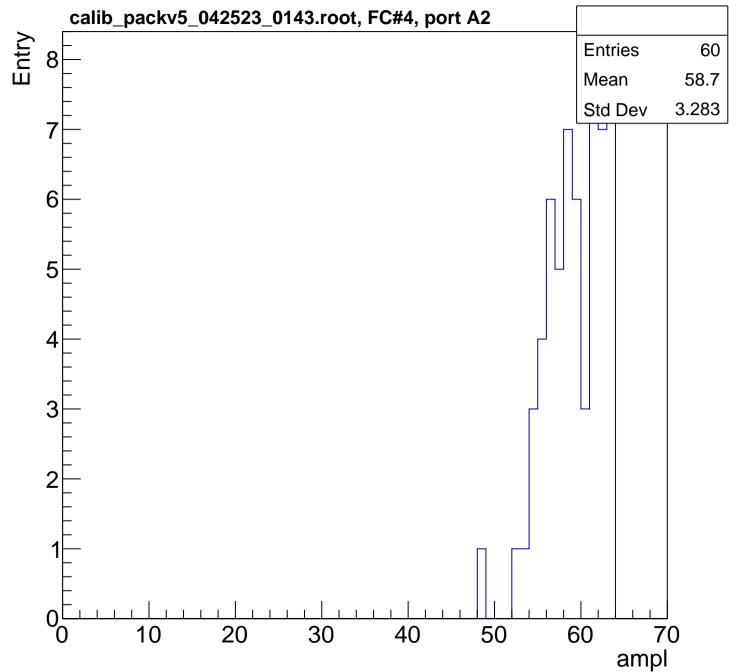


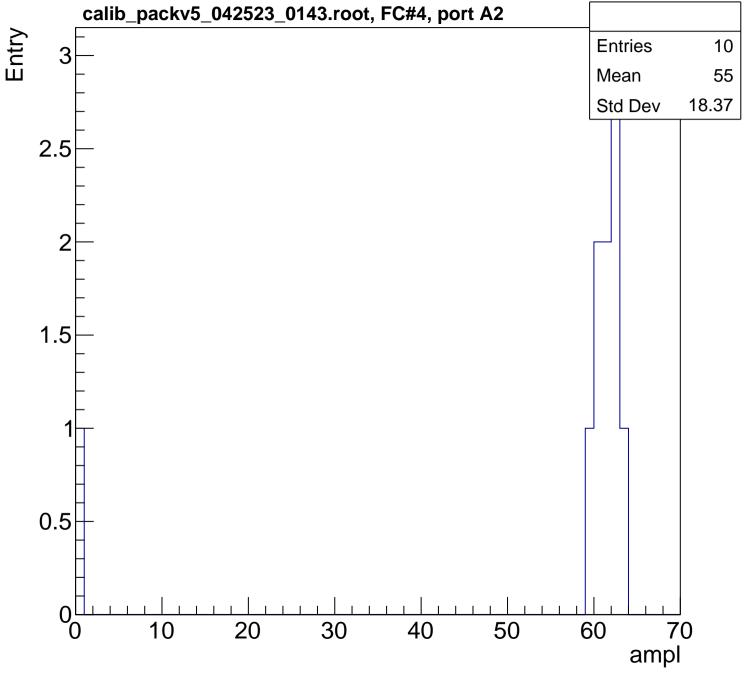




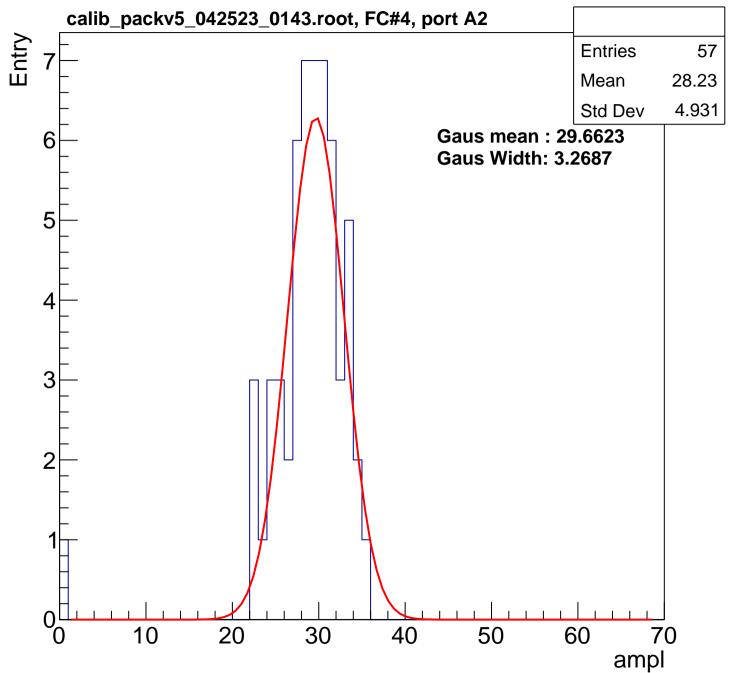


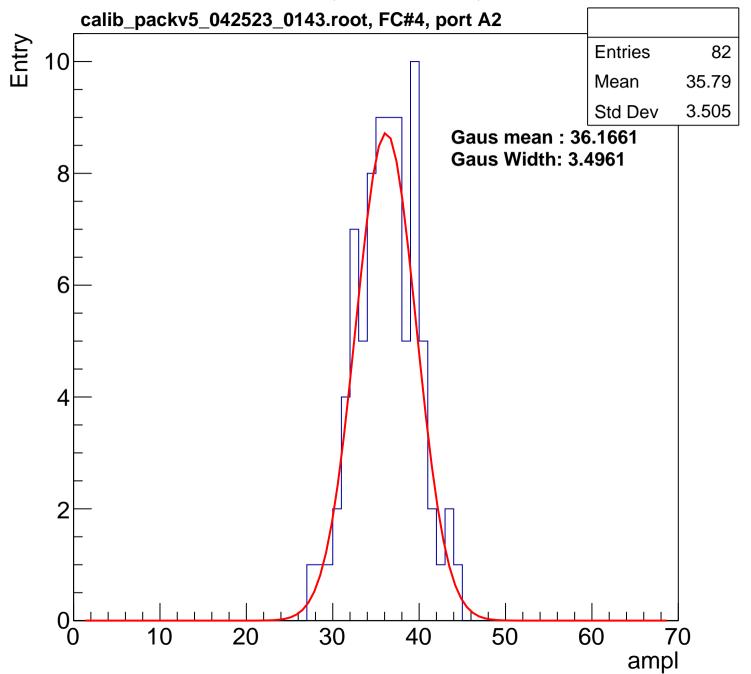


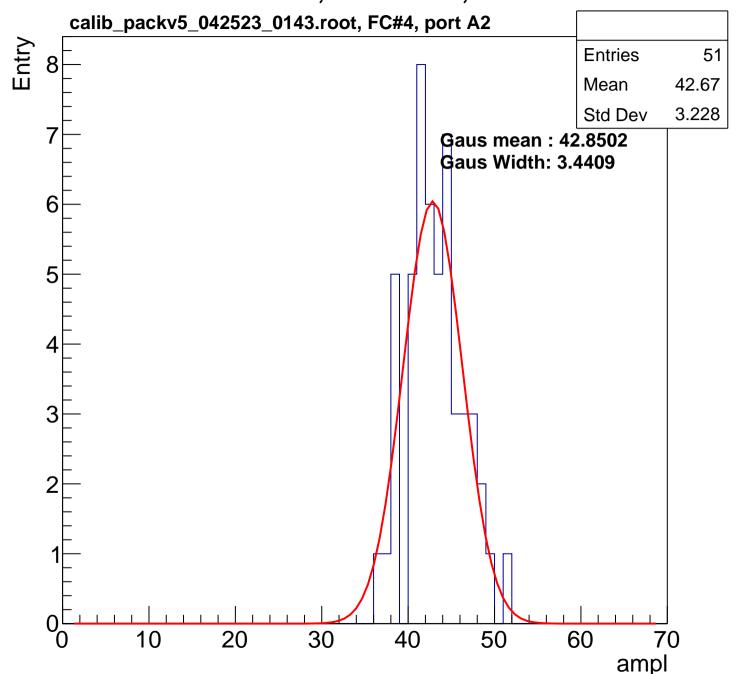


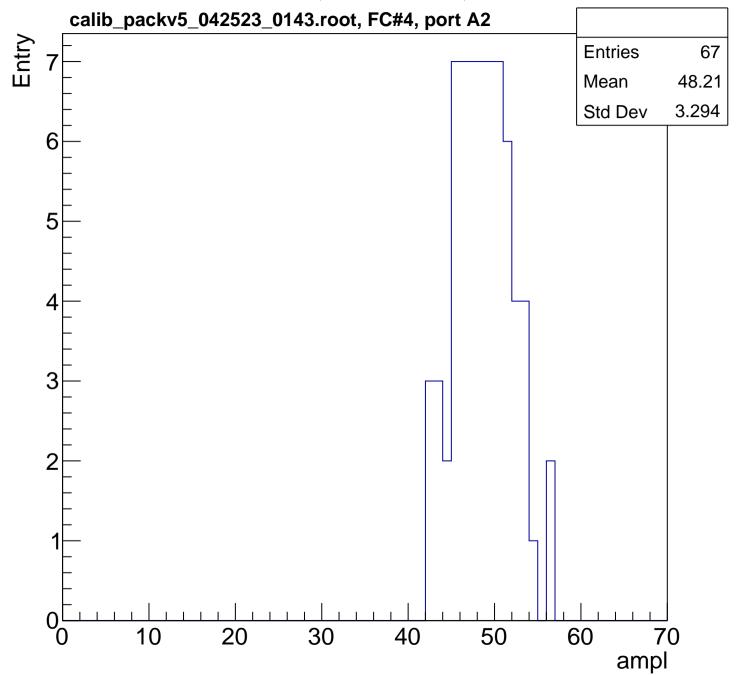


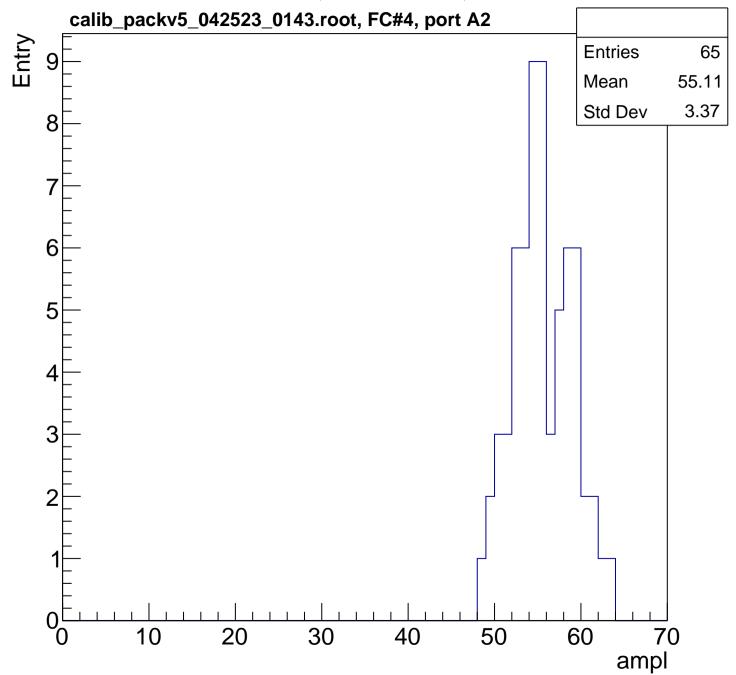
B1L100S, U3-ch62, adc7 calib_packv5_042523_0143.root, FC#4, port A2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

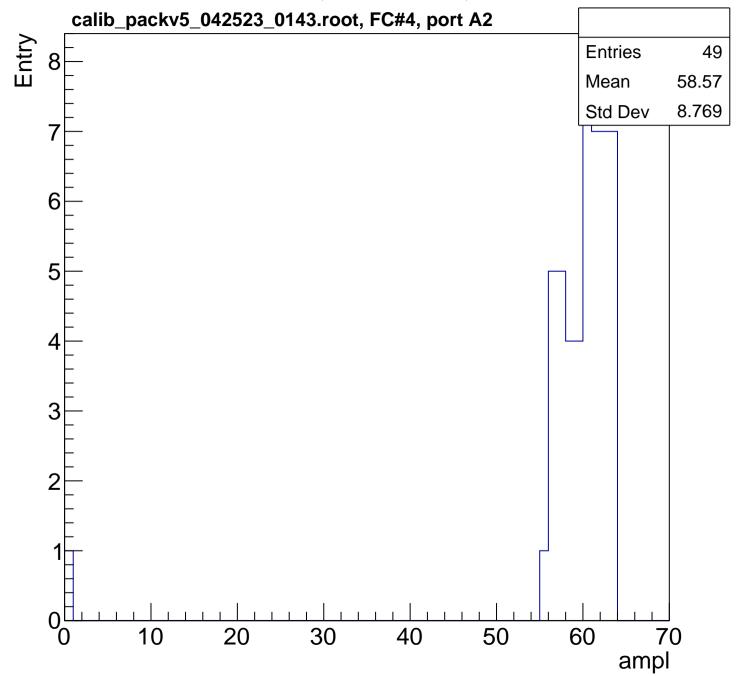


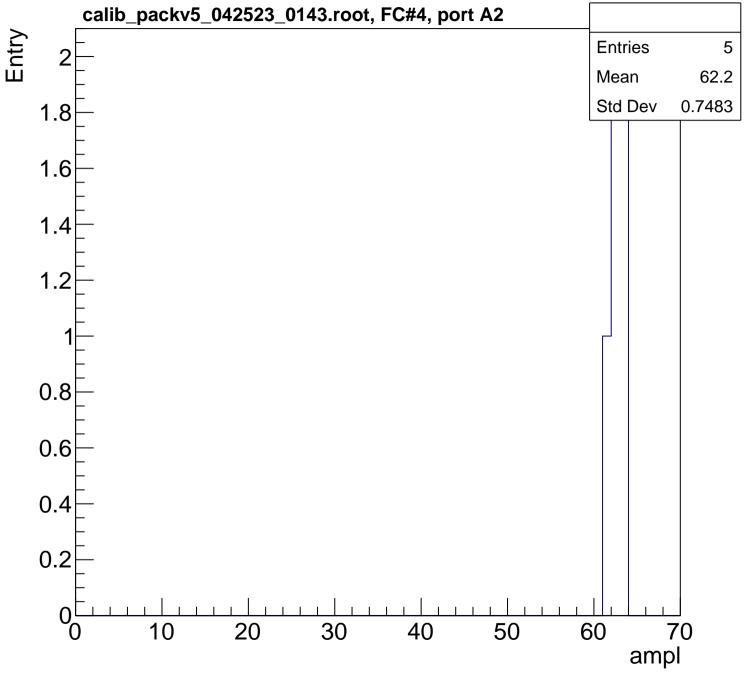


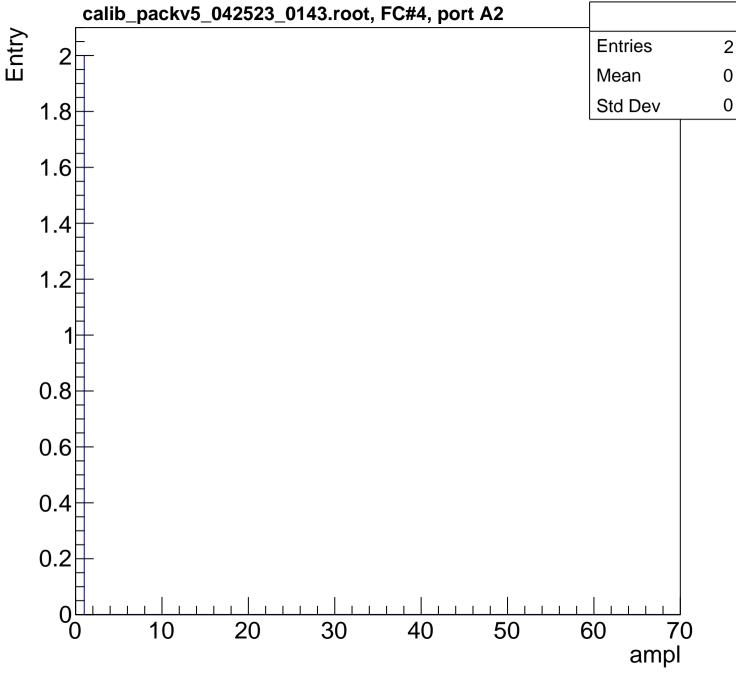


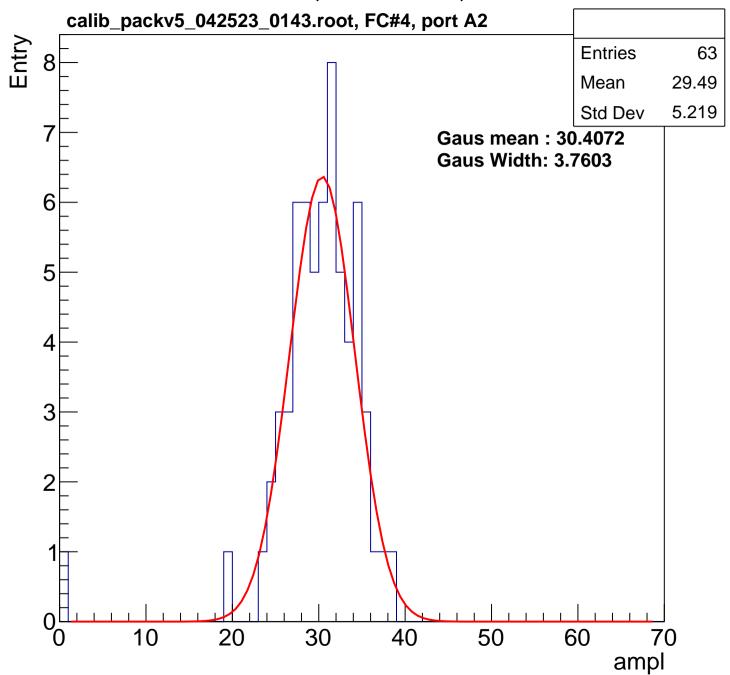


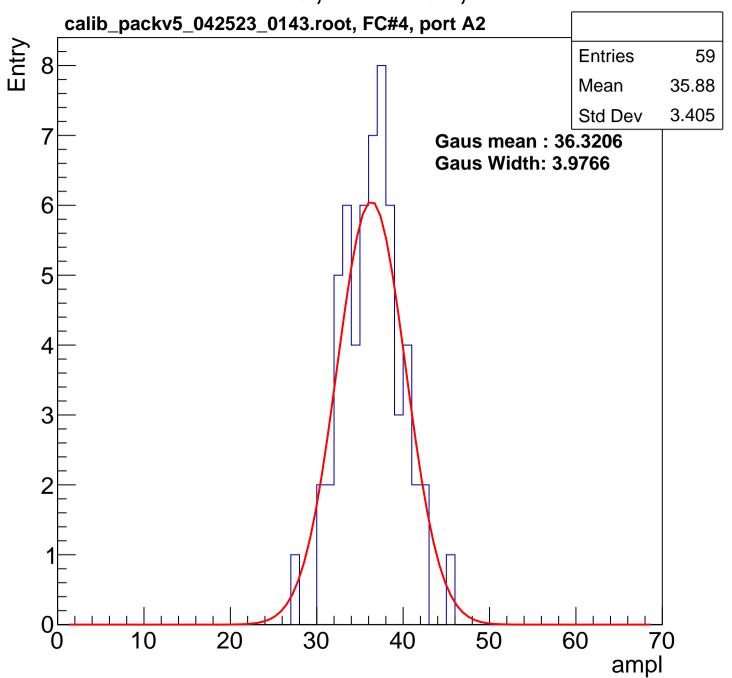


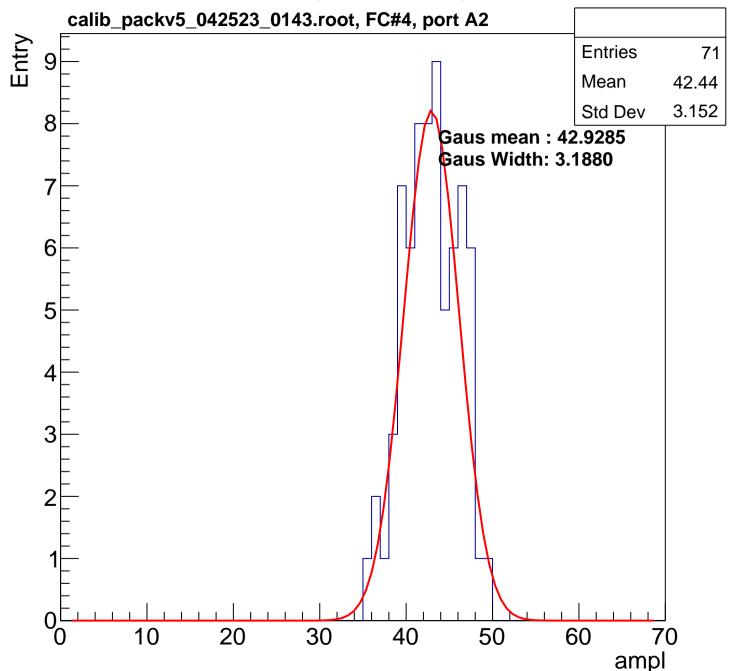


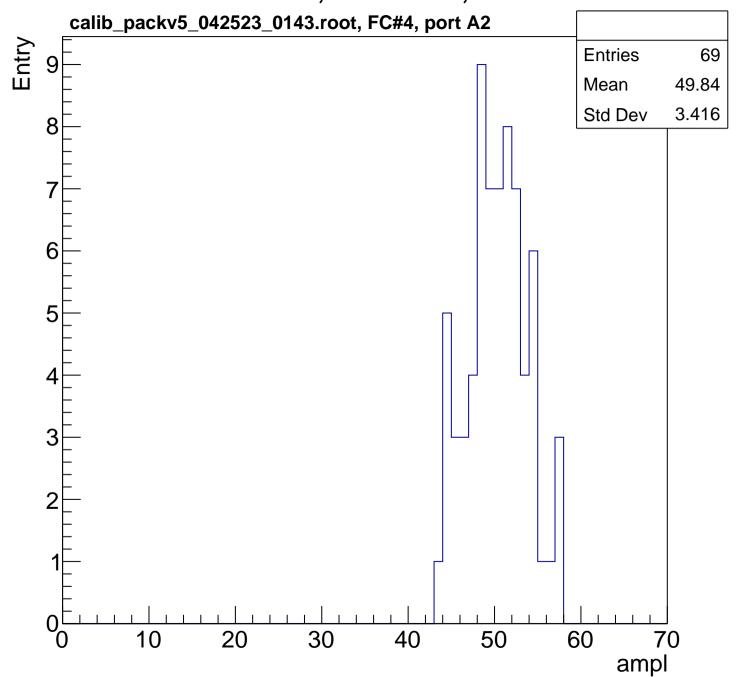


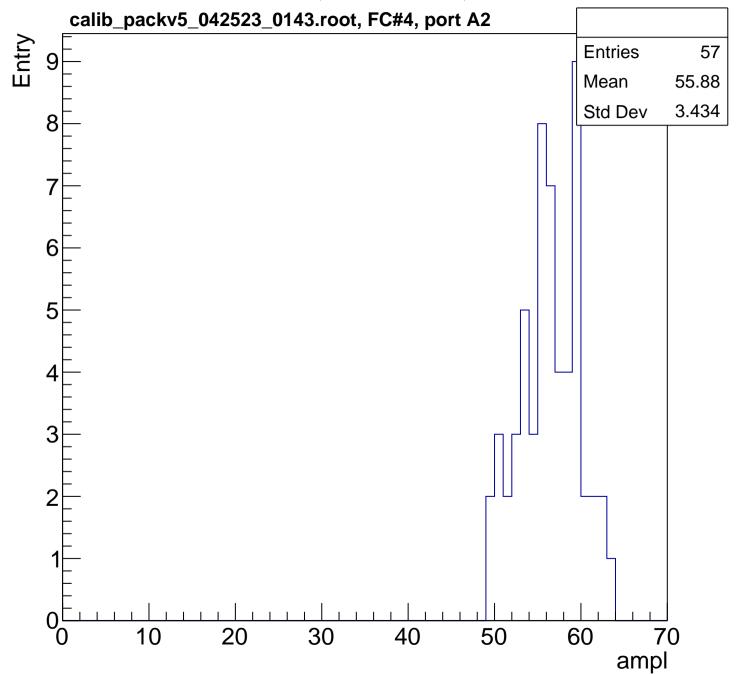


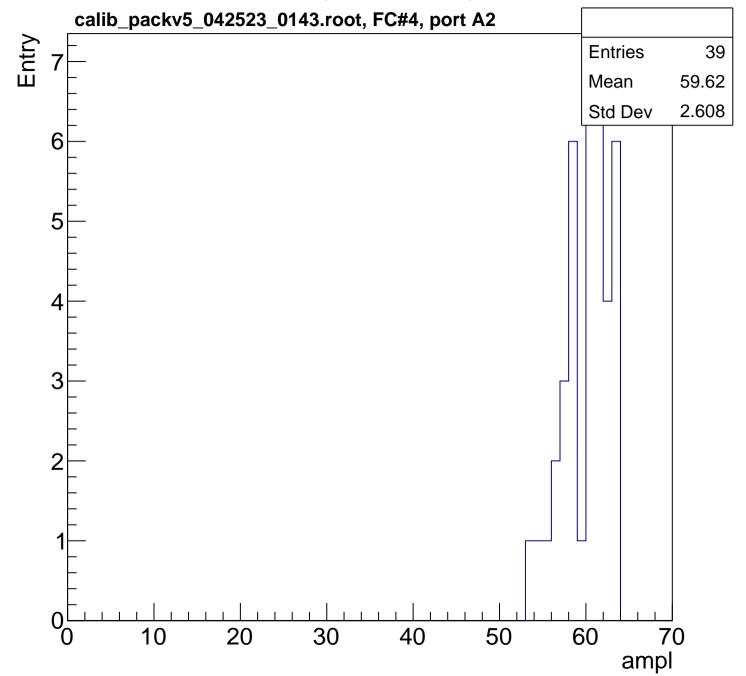


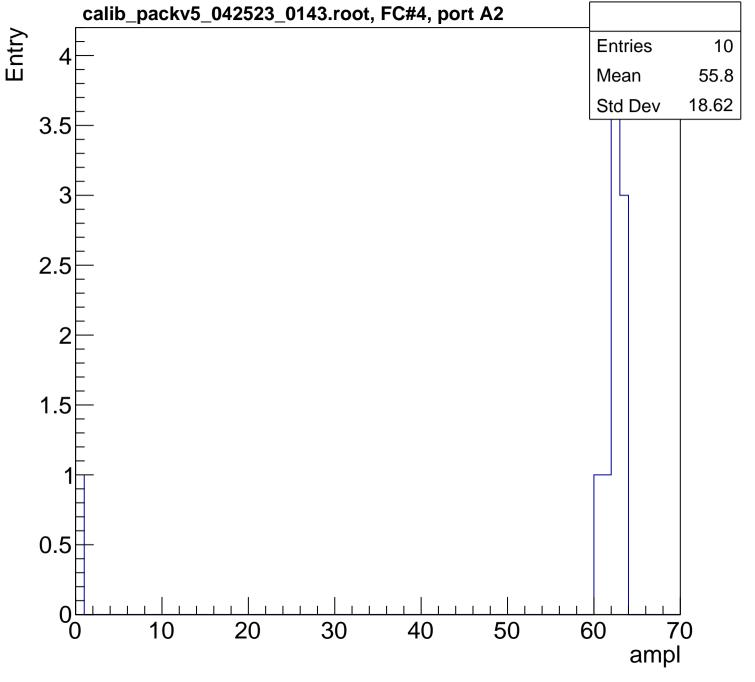




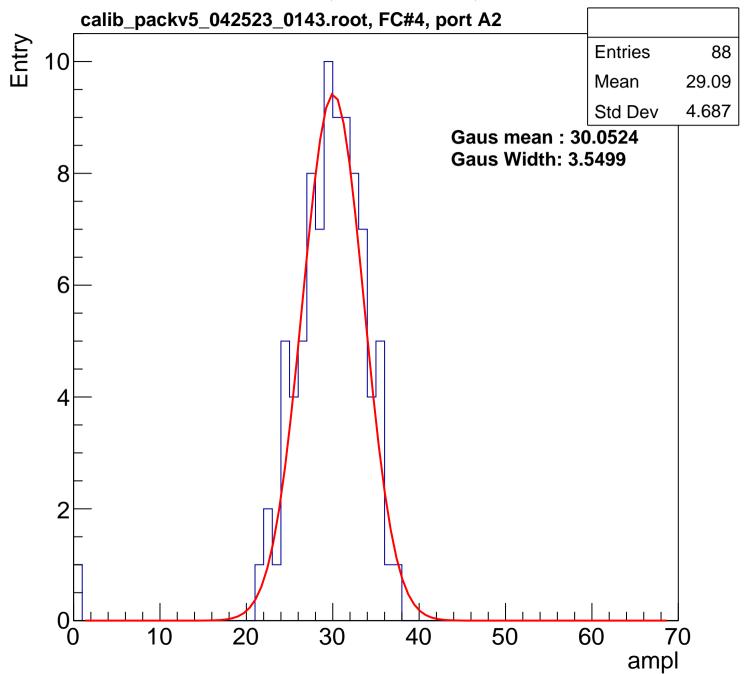


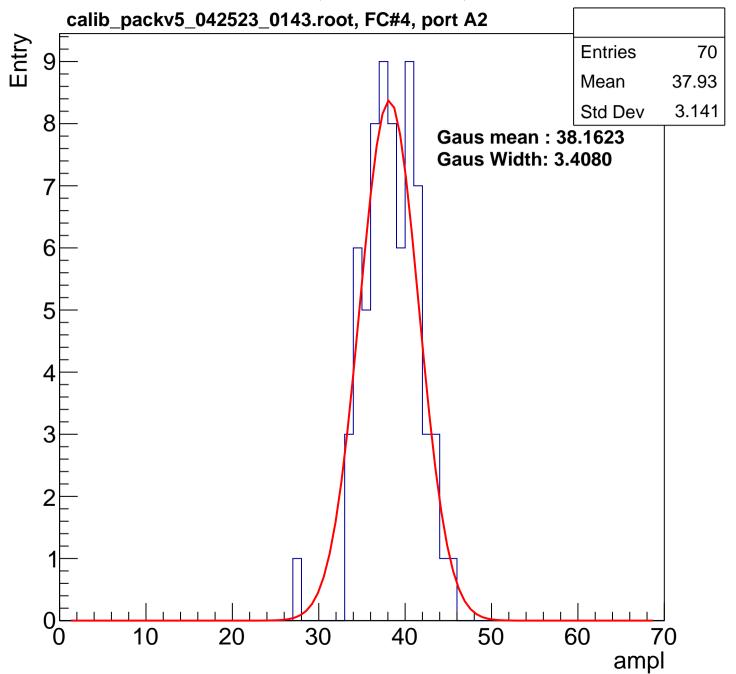


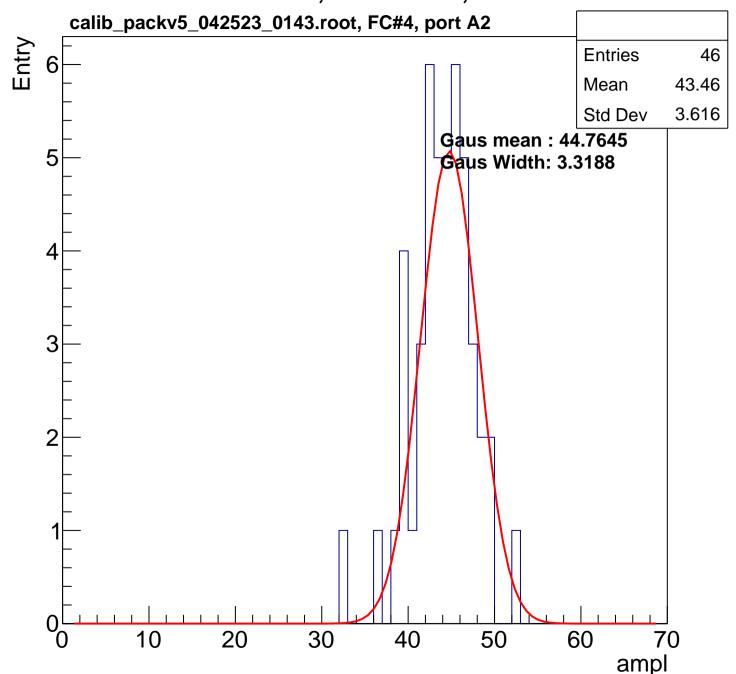




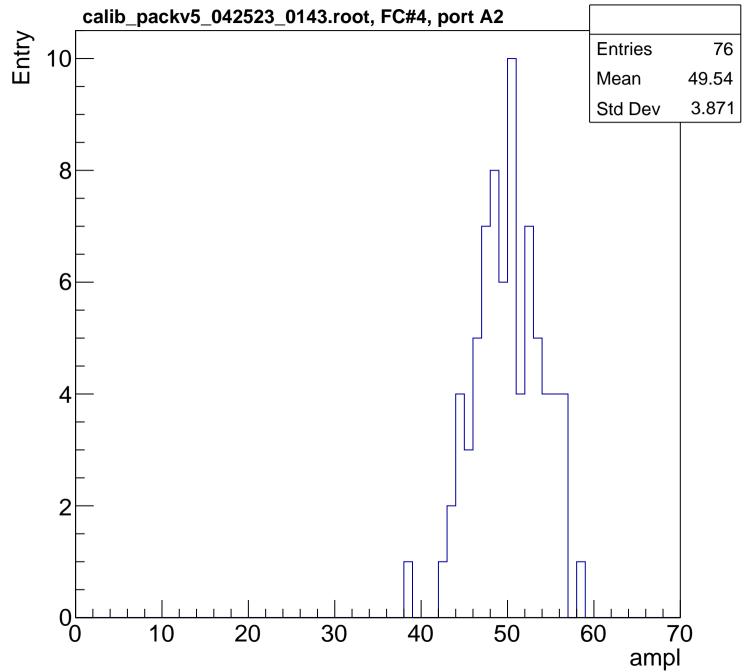
B1L100S, U3-ch64, adc7 calib_packv5_042523_0143.root, FC#4, port A2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

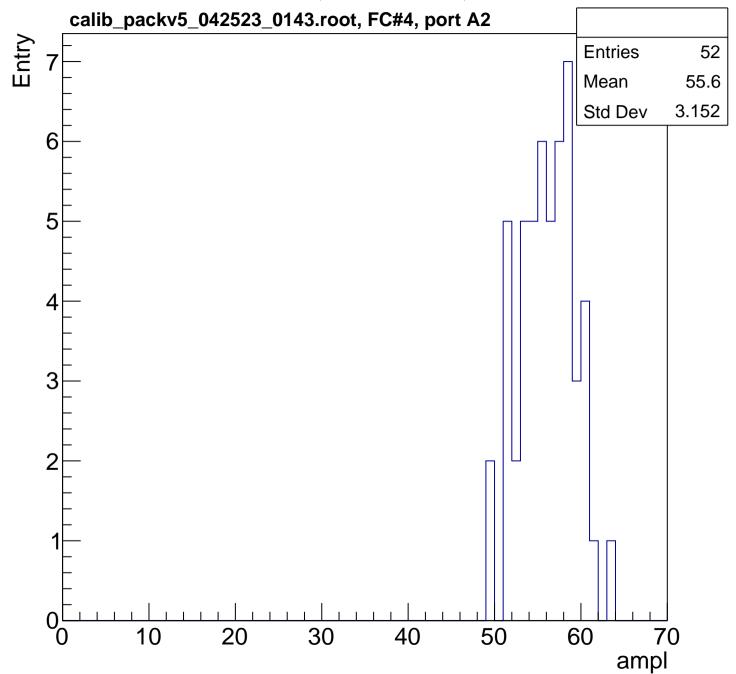


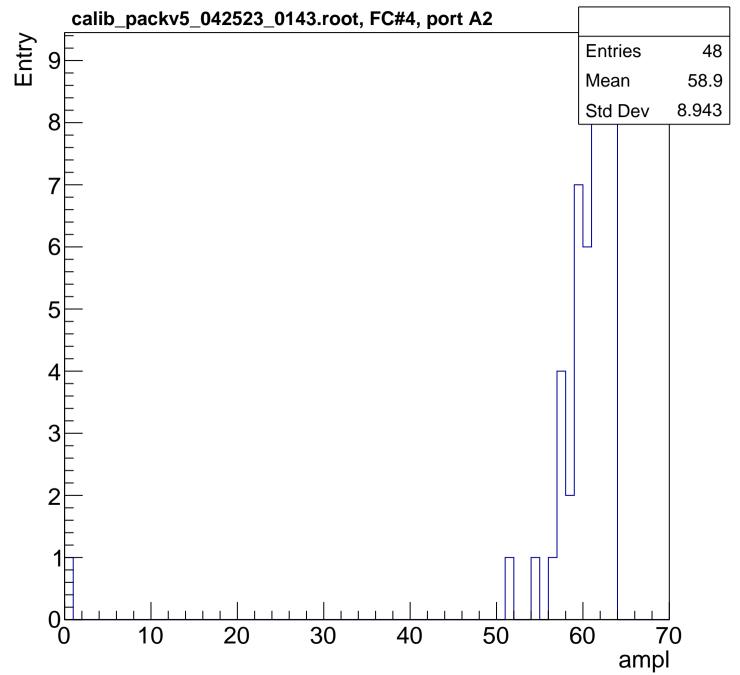


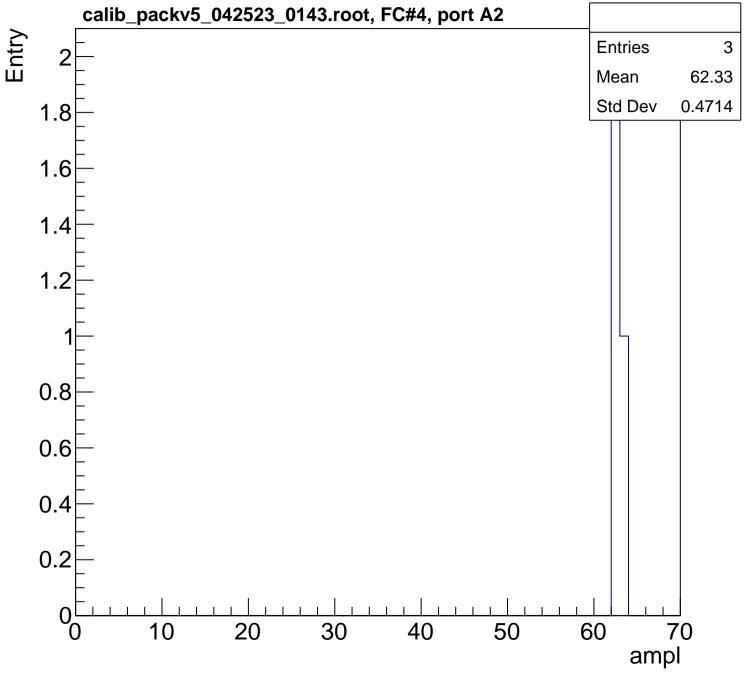


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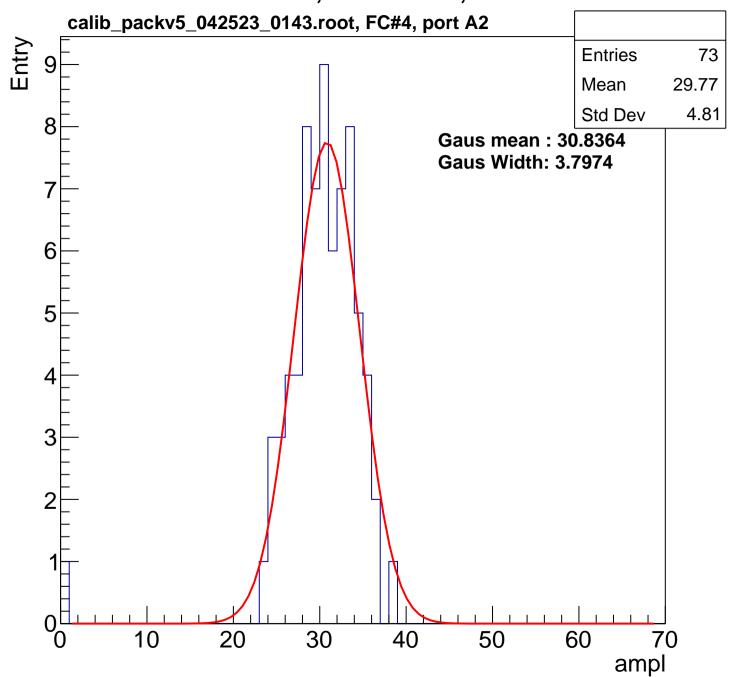


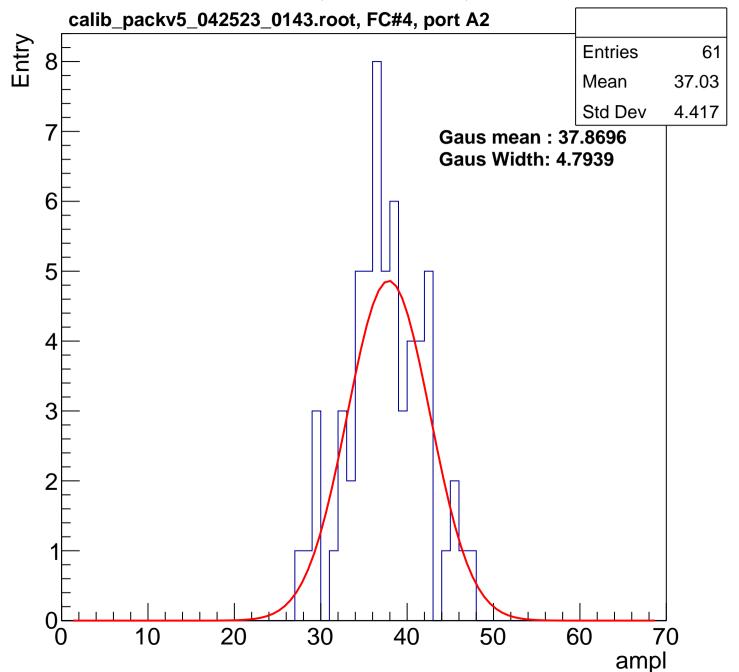


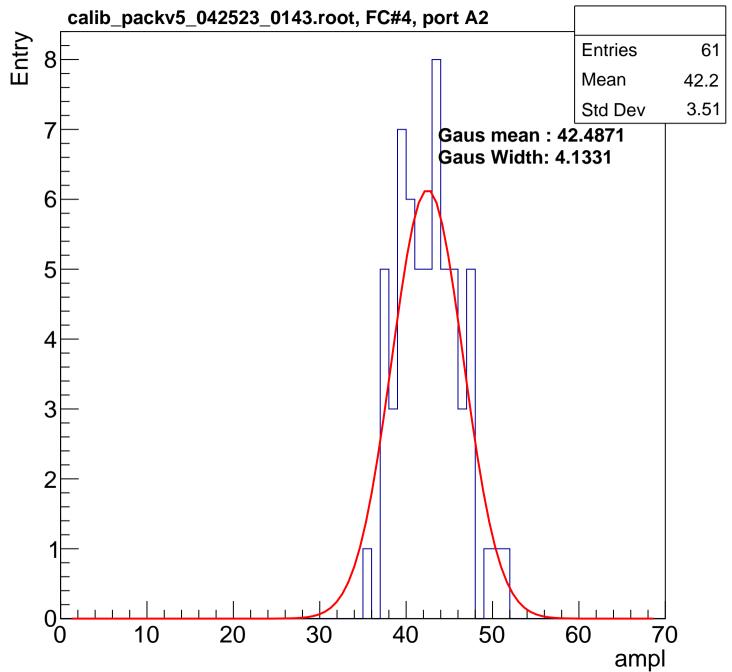


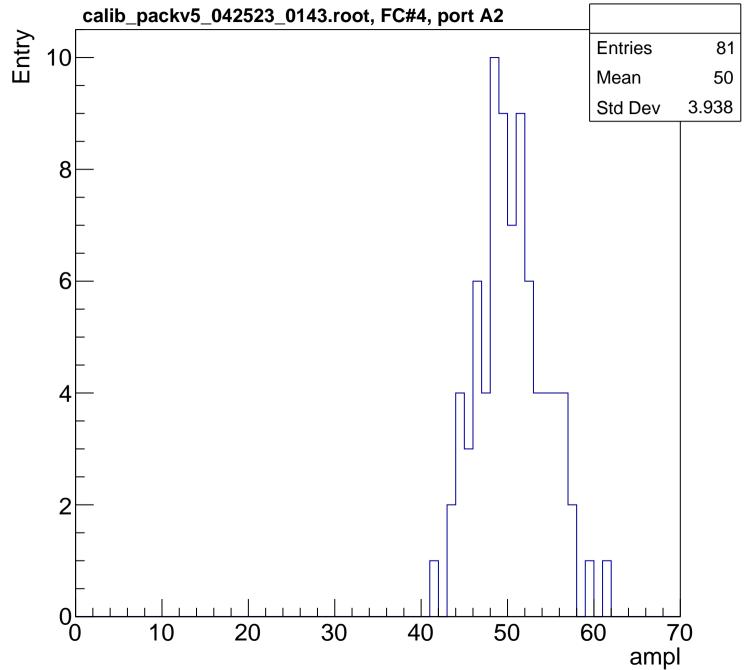
B1L100S, U3-ch65, adc7 calib_packv5_042523_0143.root, FC#4, port A2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70

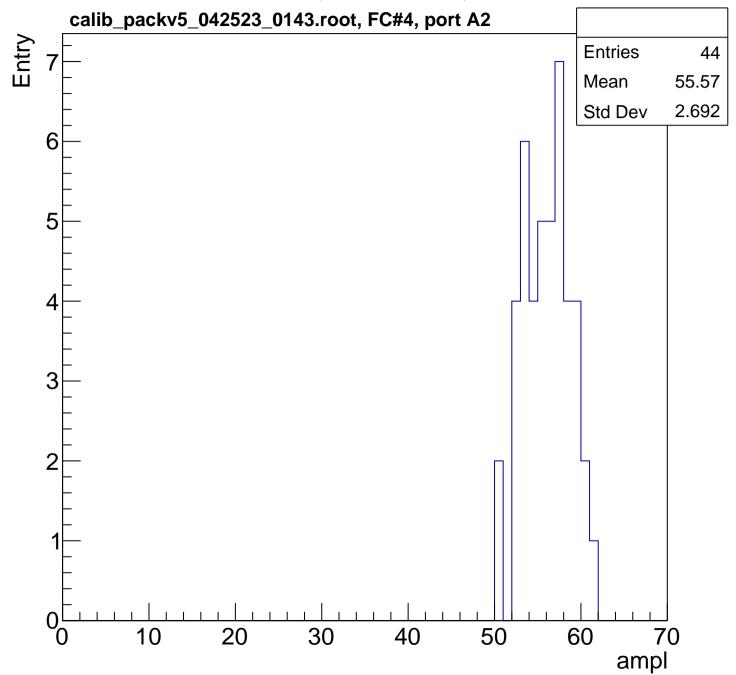
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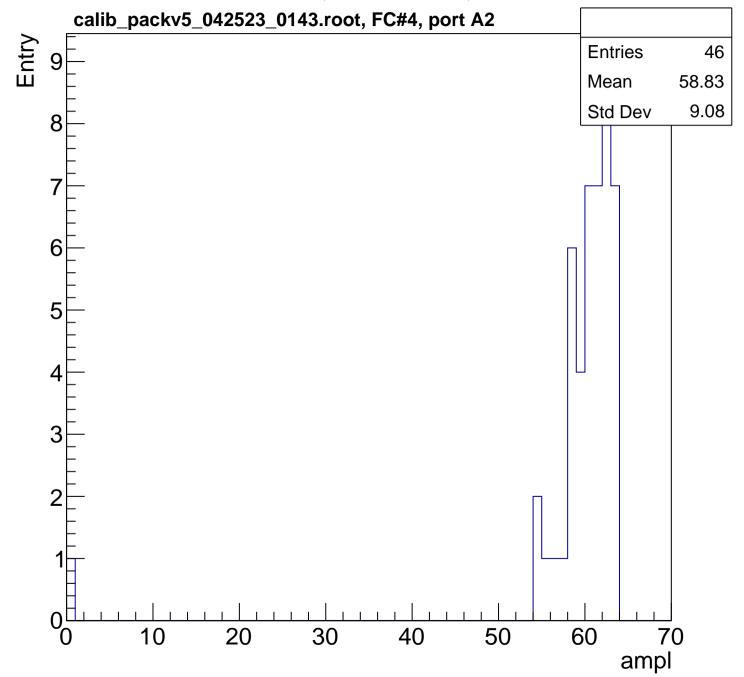


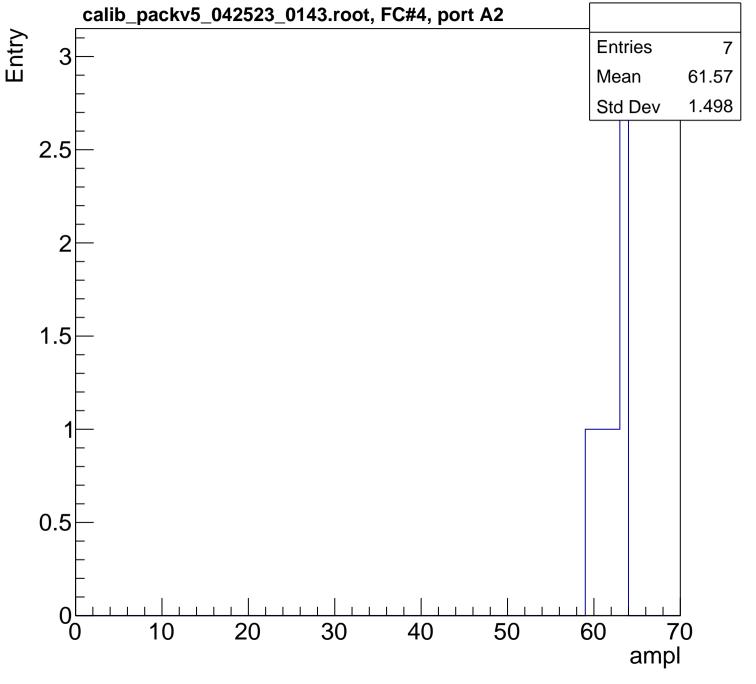






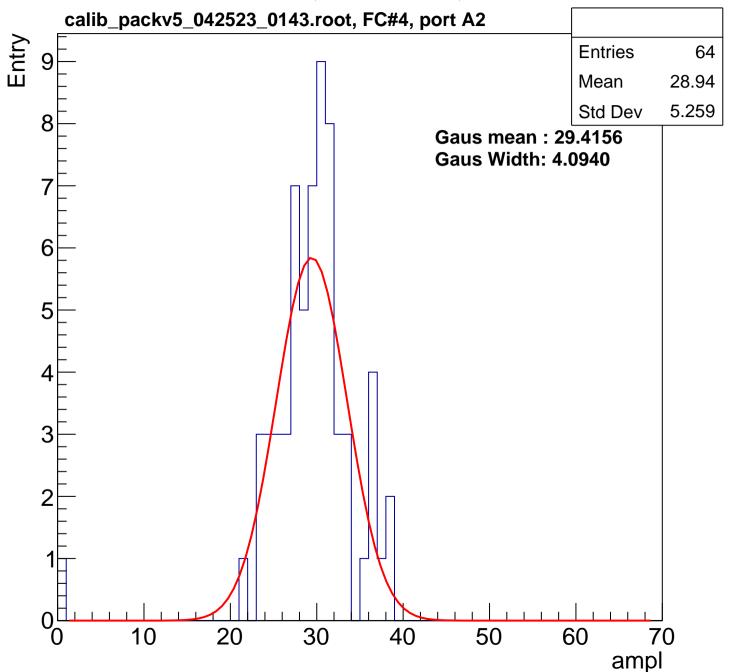


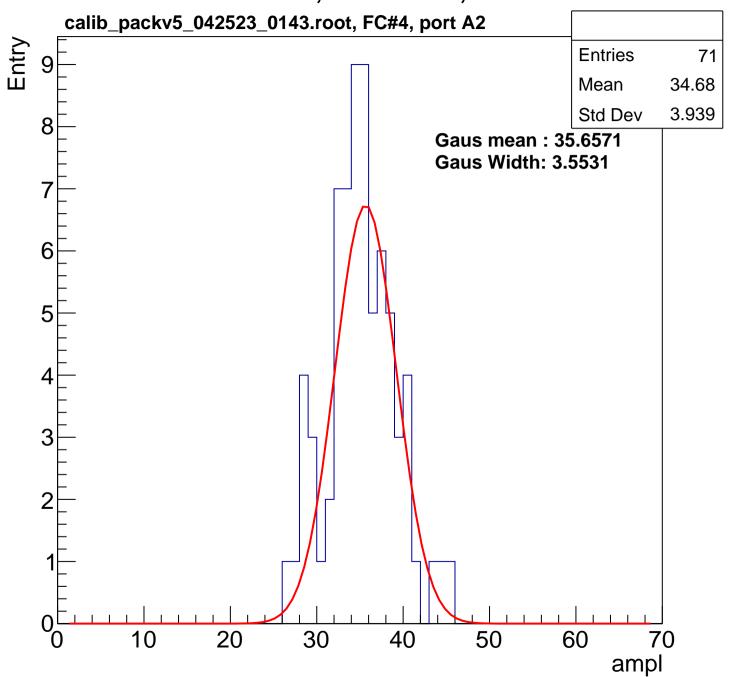


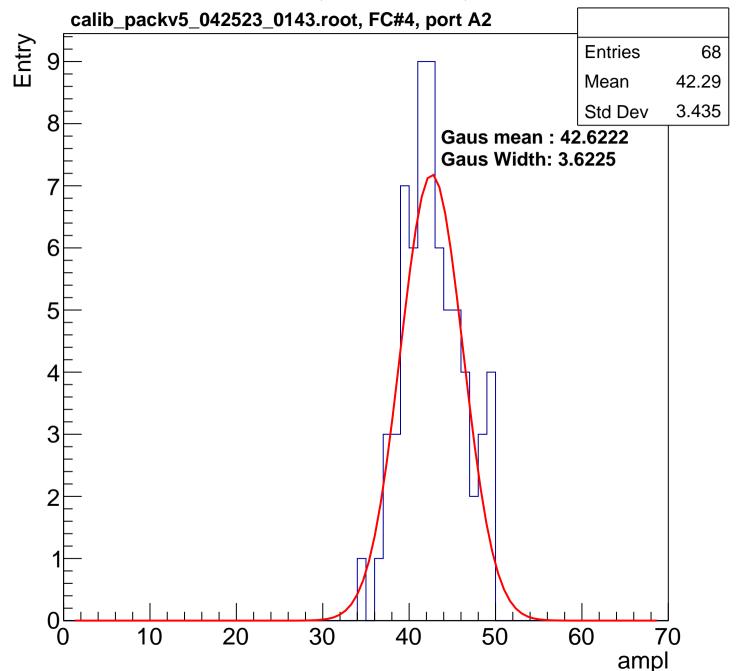


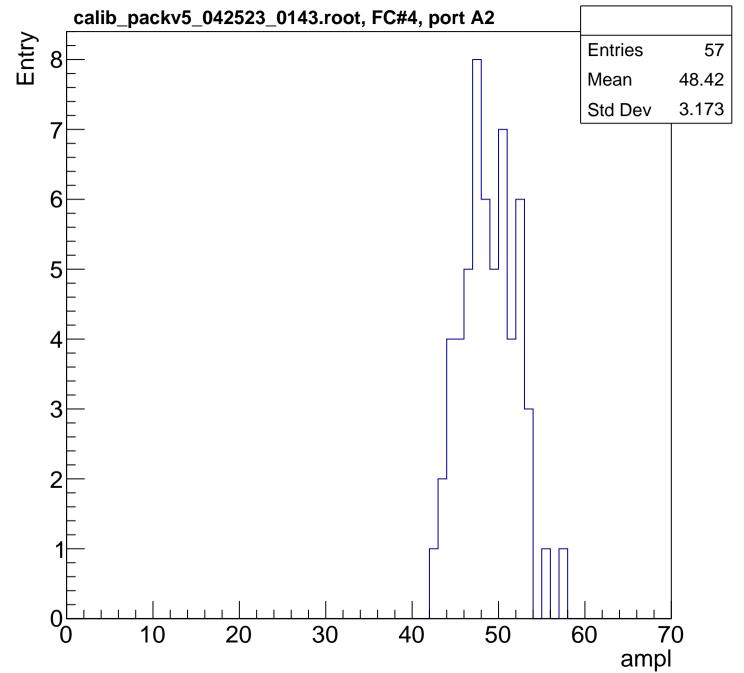
B1L100S, U3-ch66, adc7 calib_packv5_042523_0143.root, FC#4, port A2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70

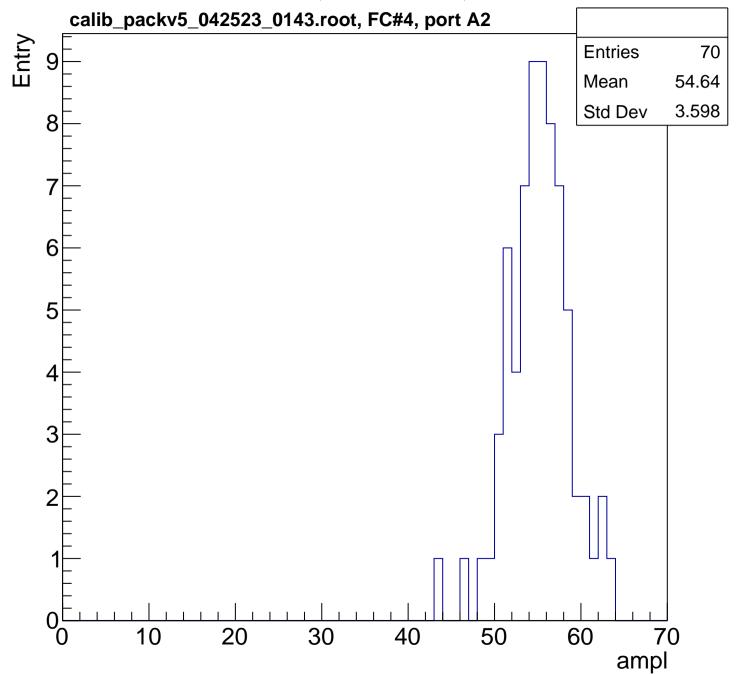
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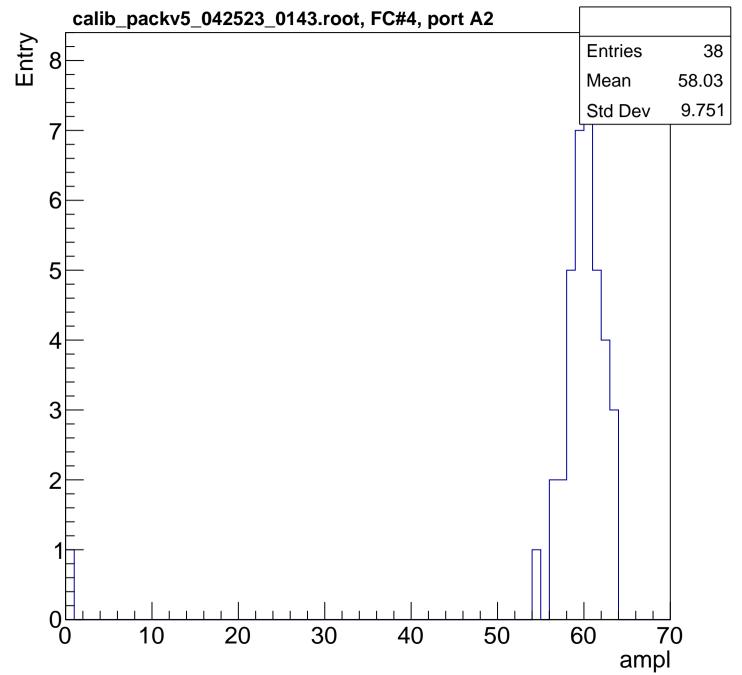


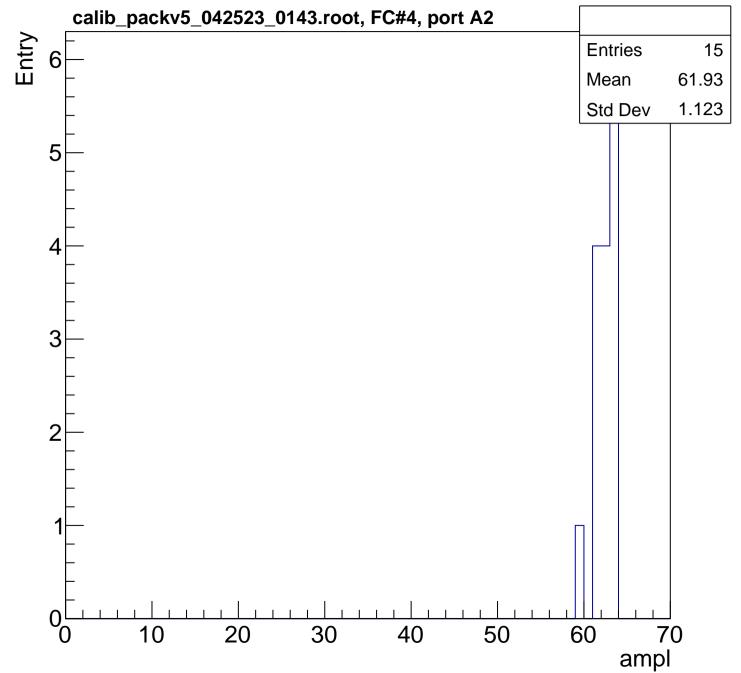




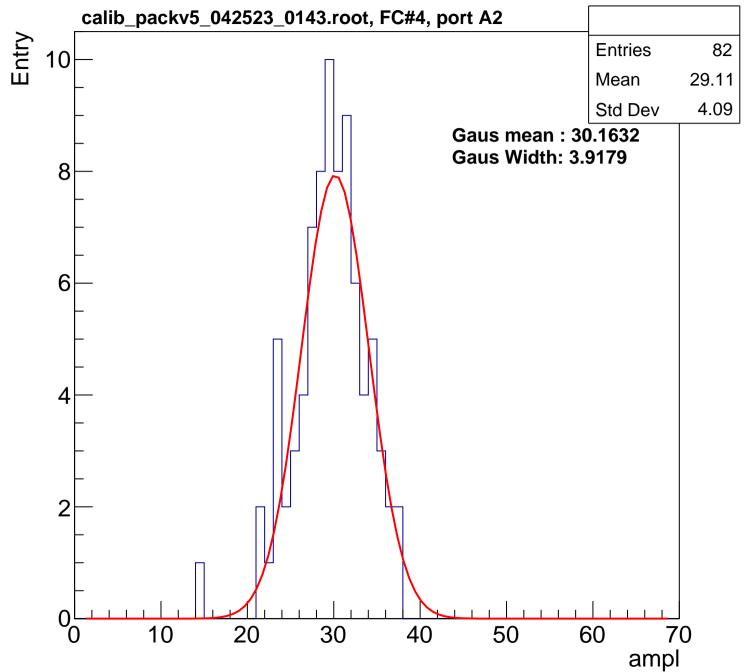


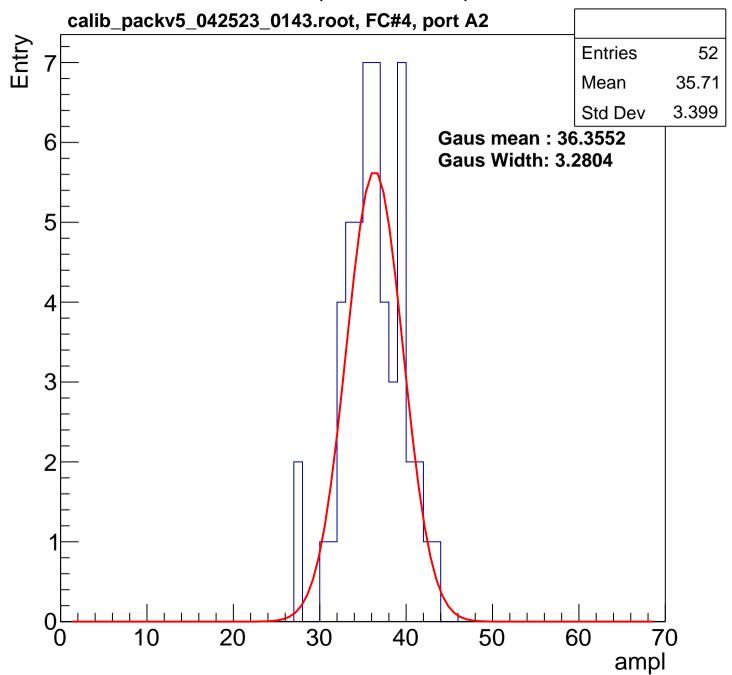


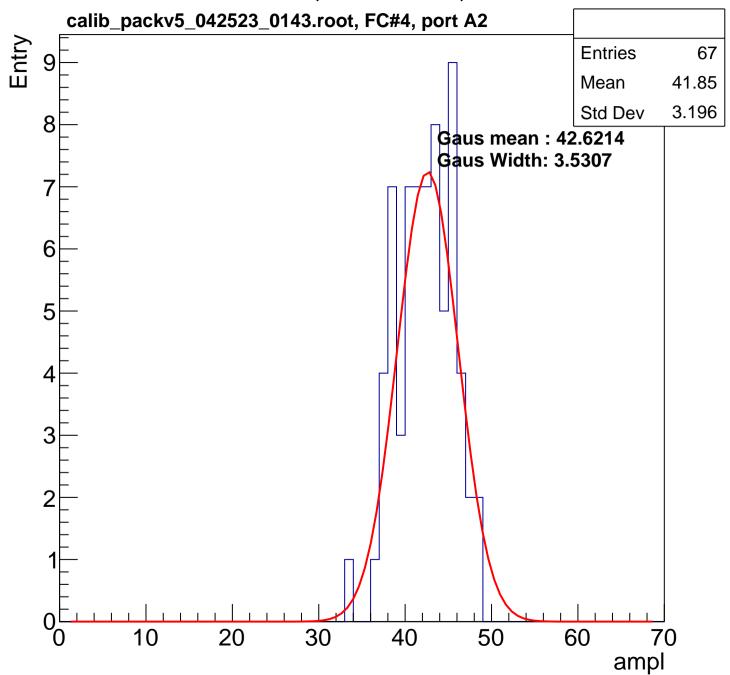


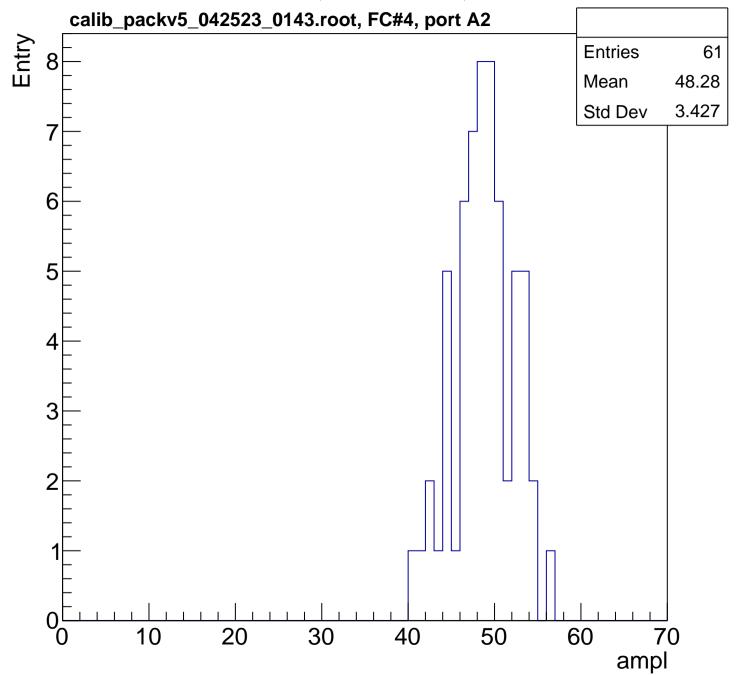


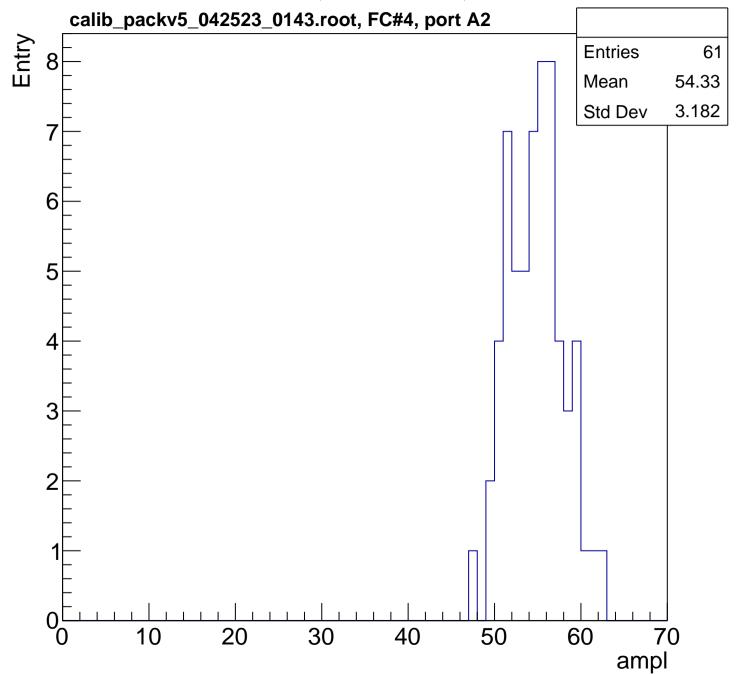


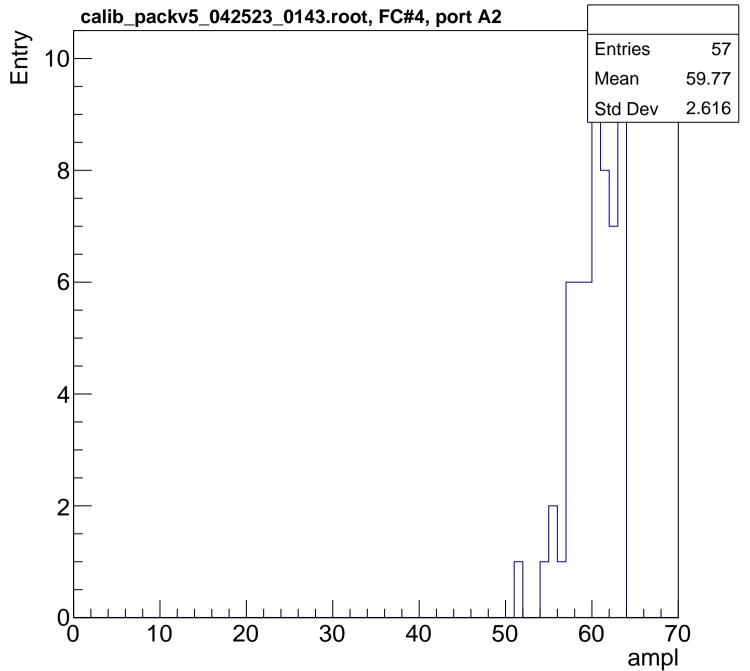


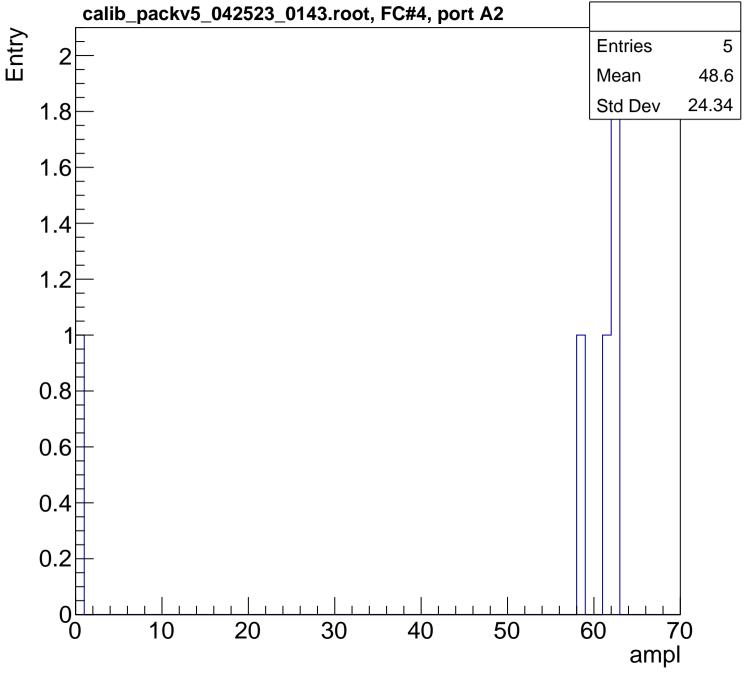




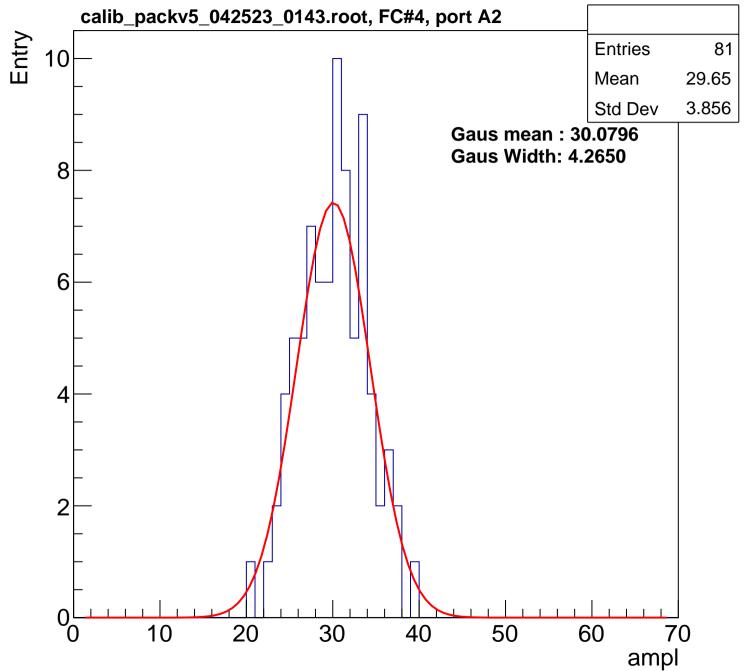


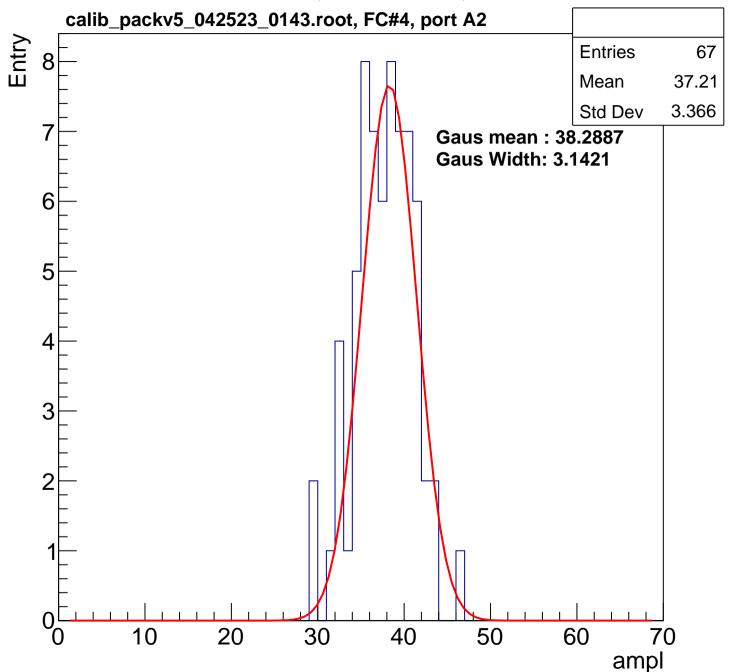


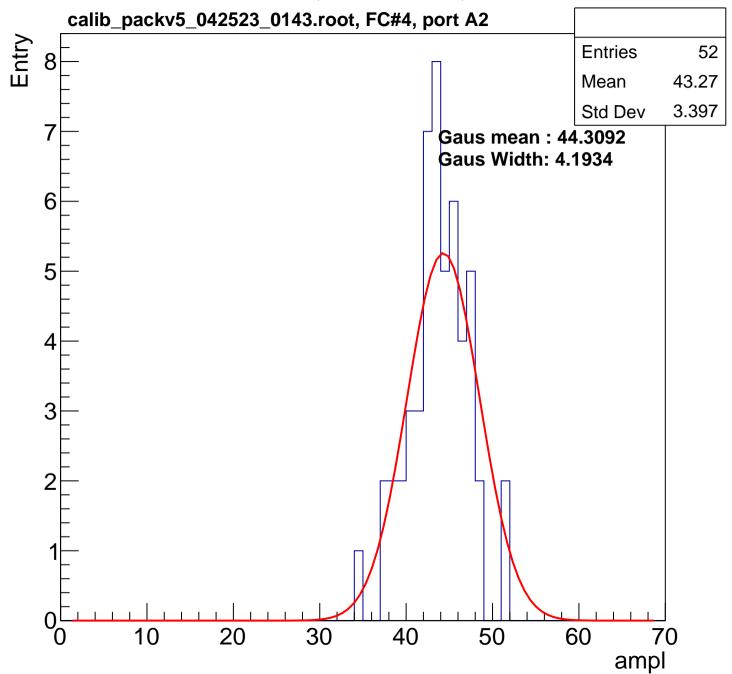


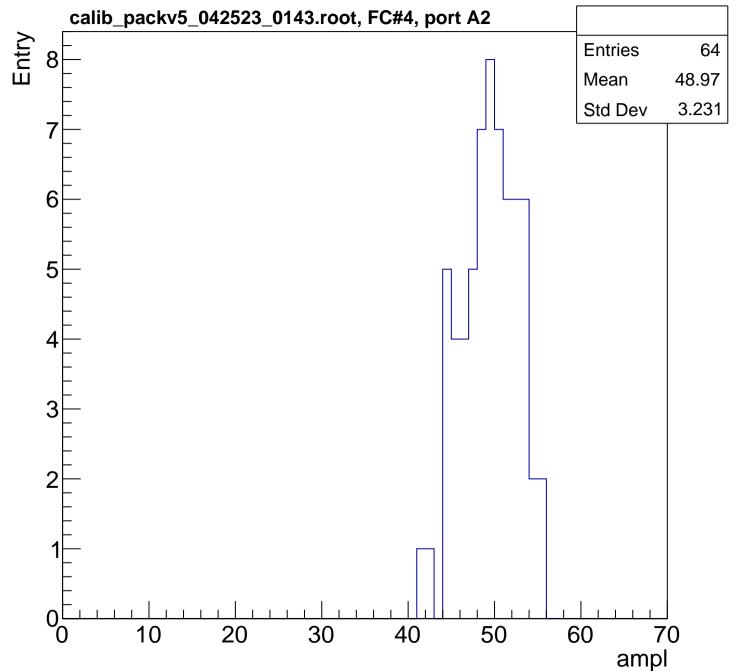


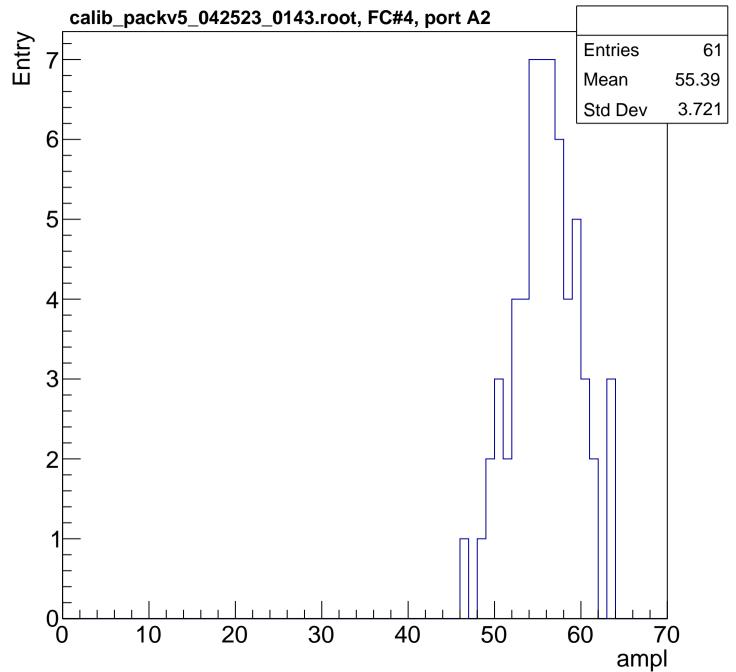


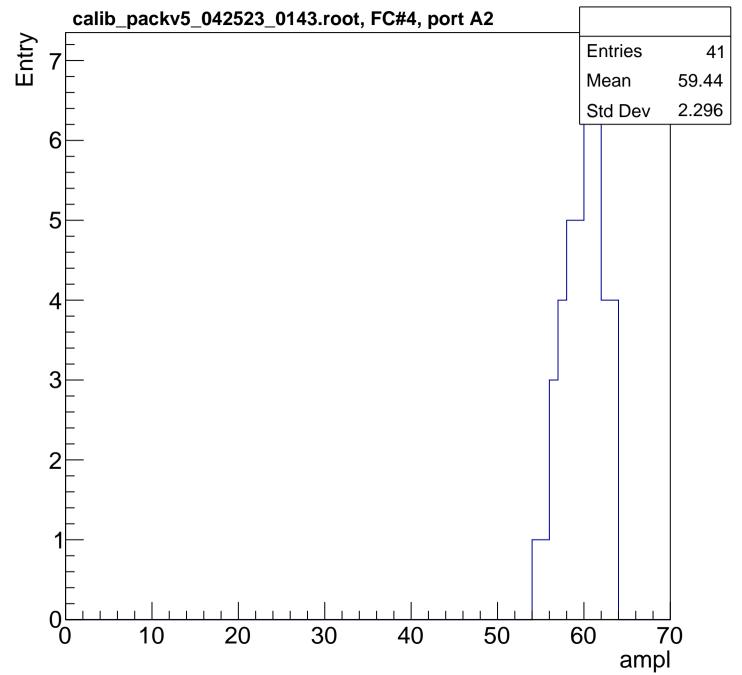


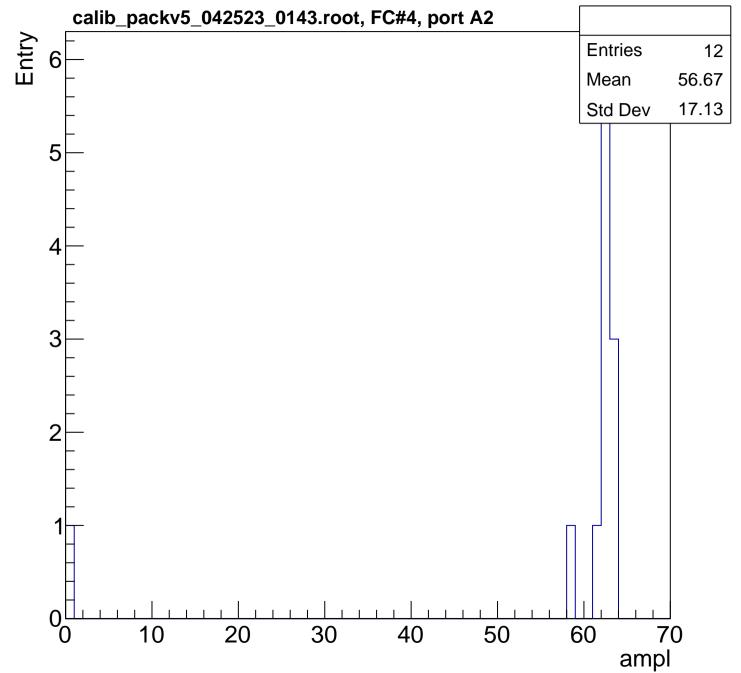


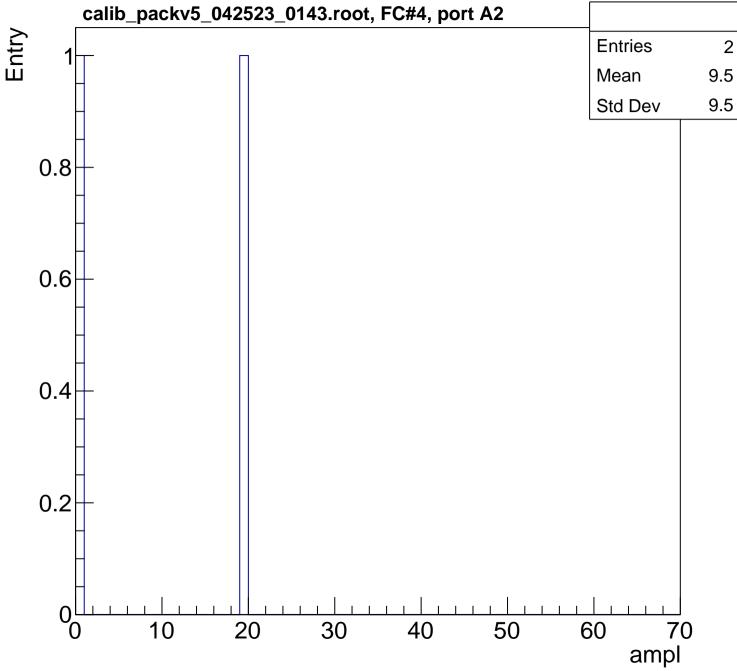


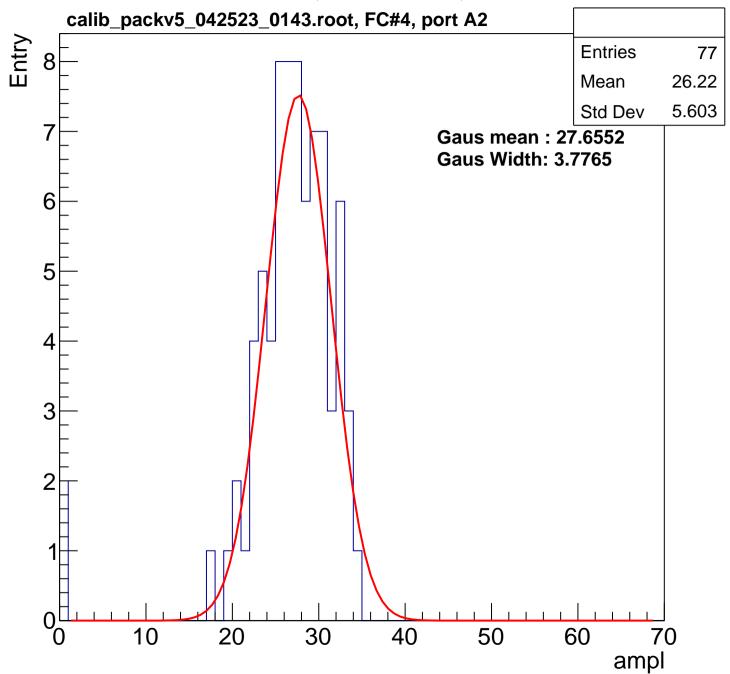


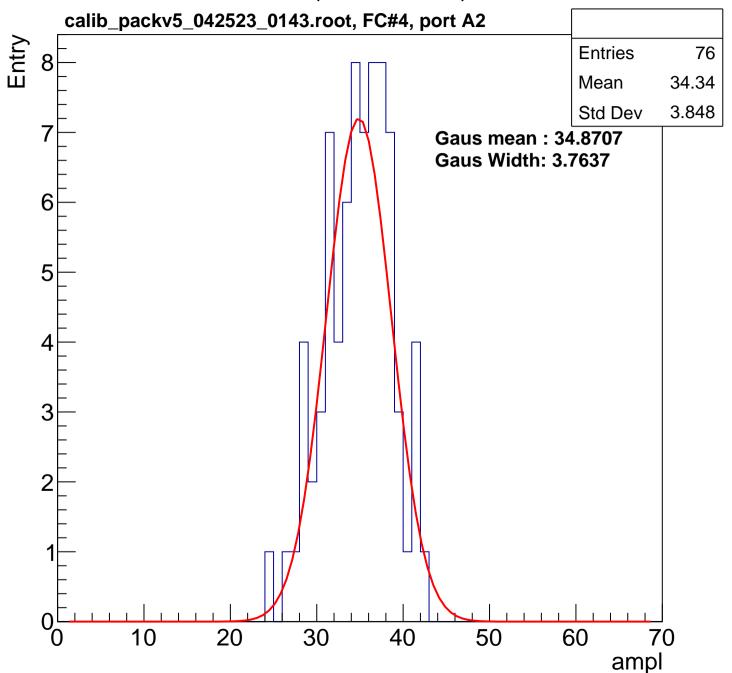


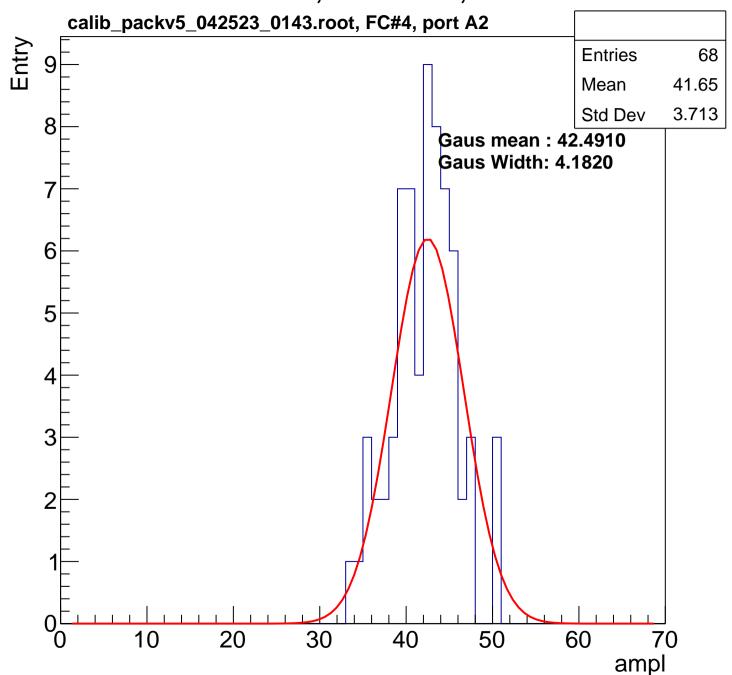


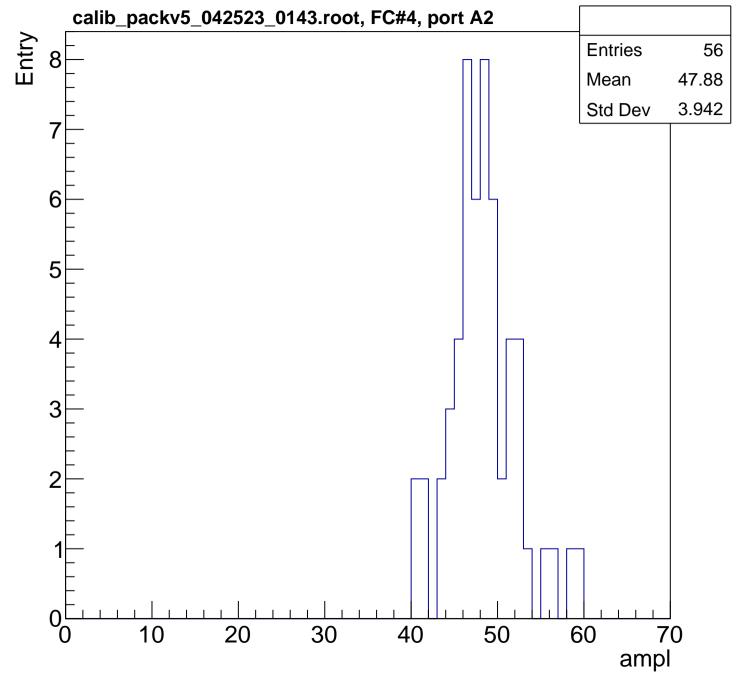


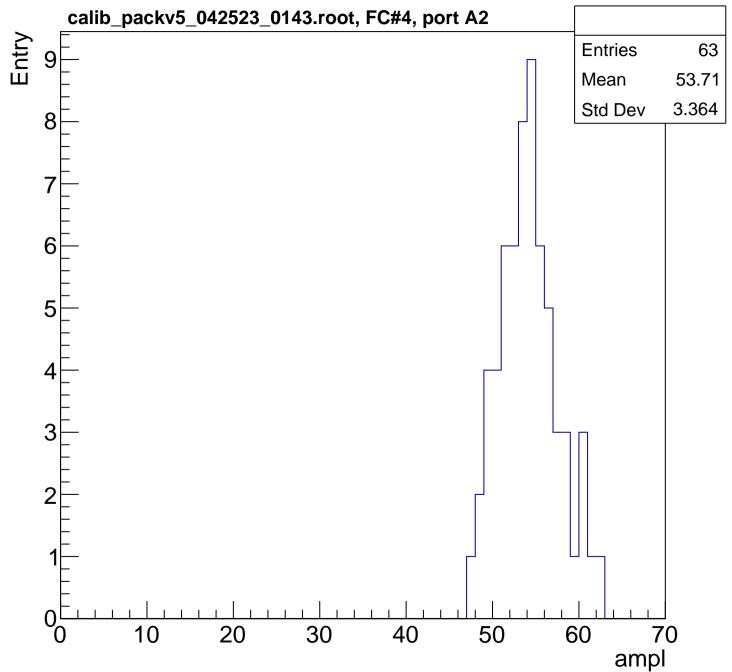


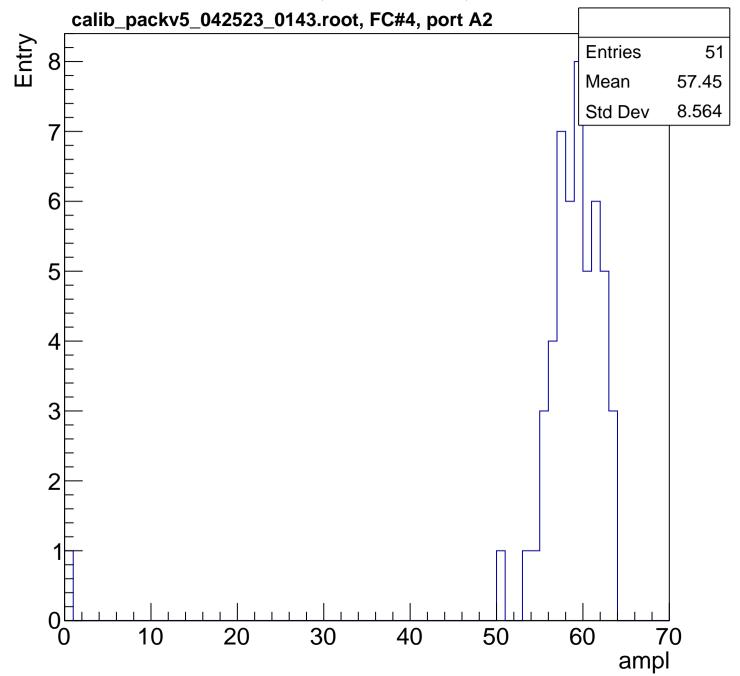


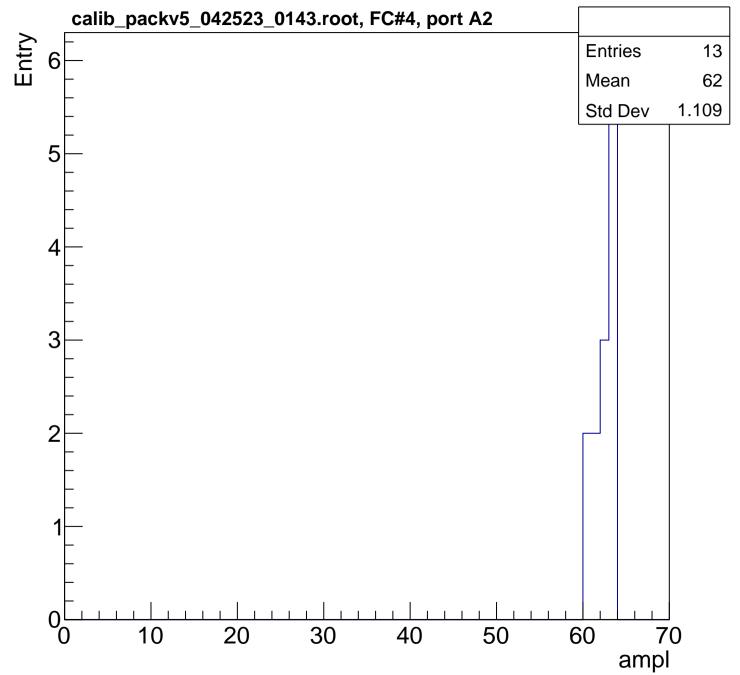


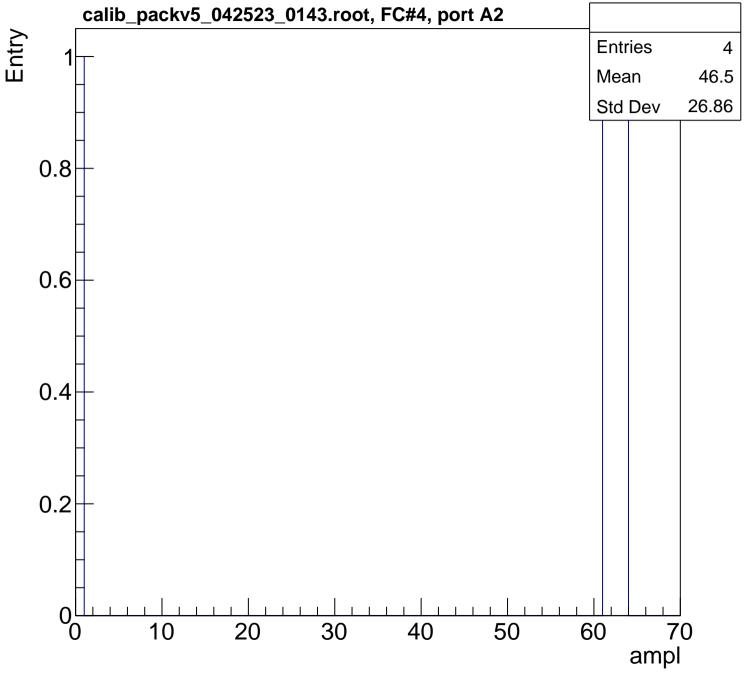


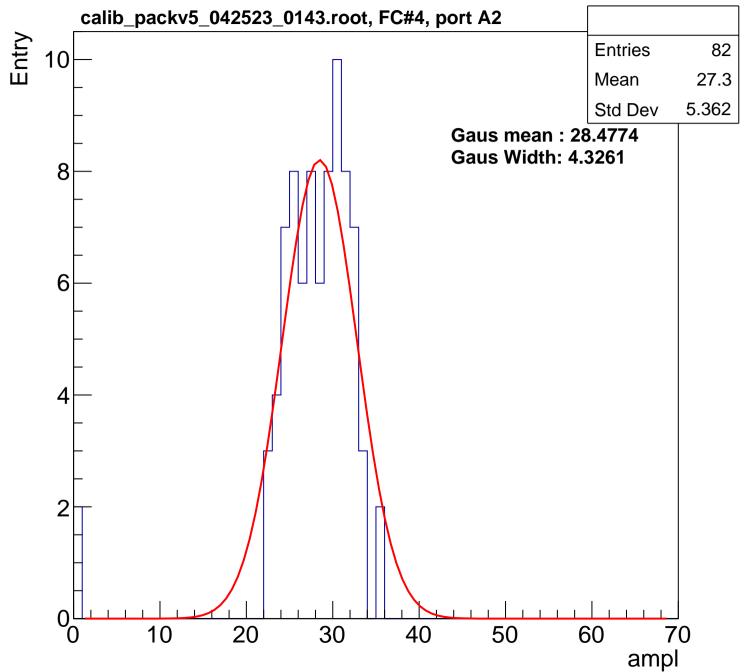


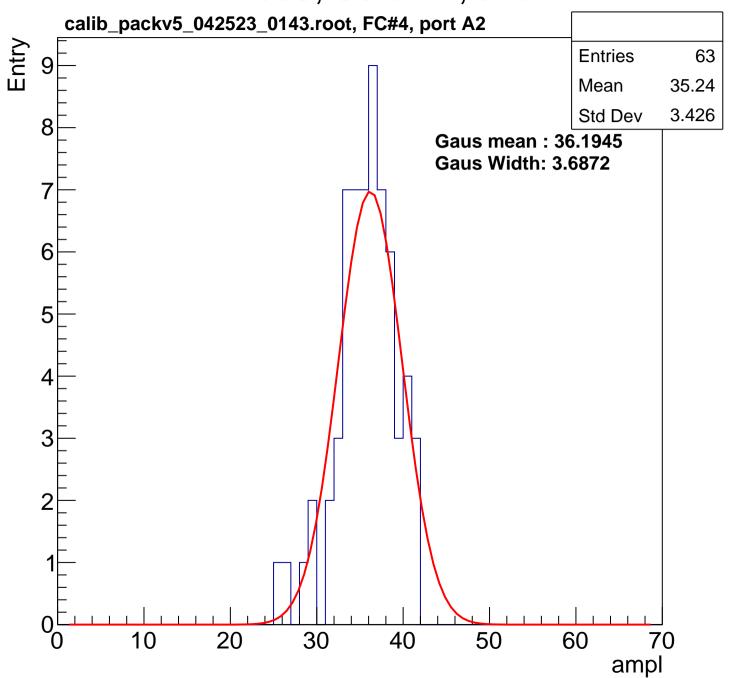


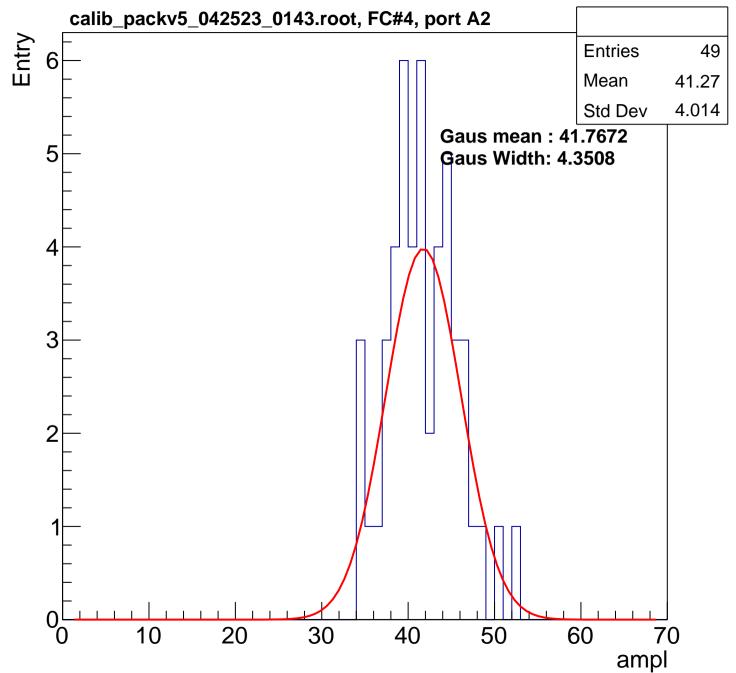


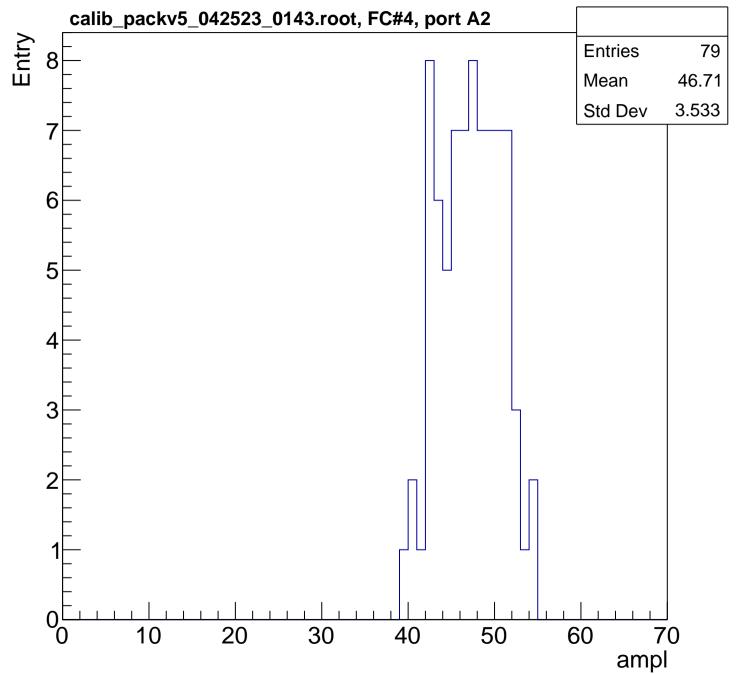


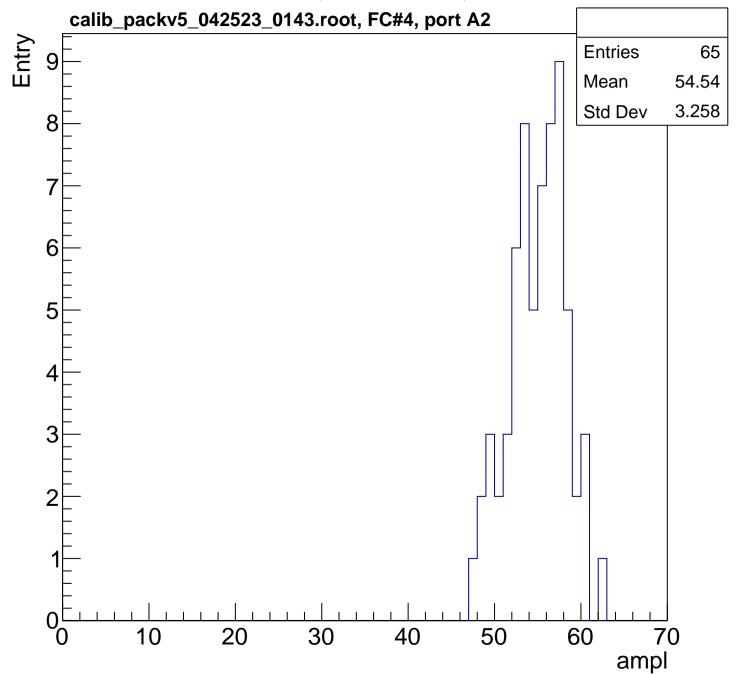


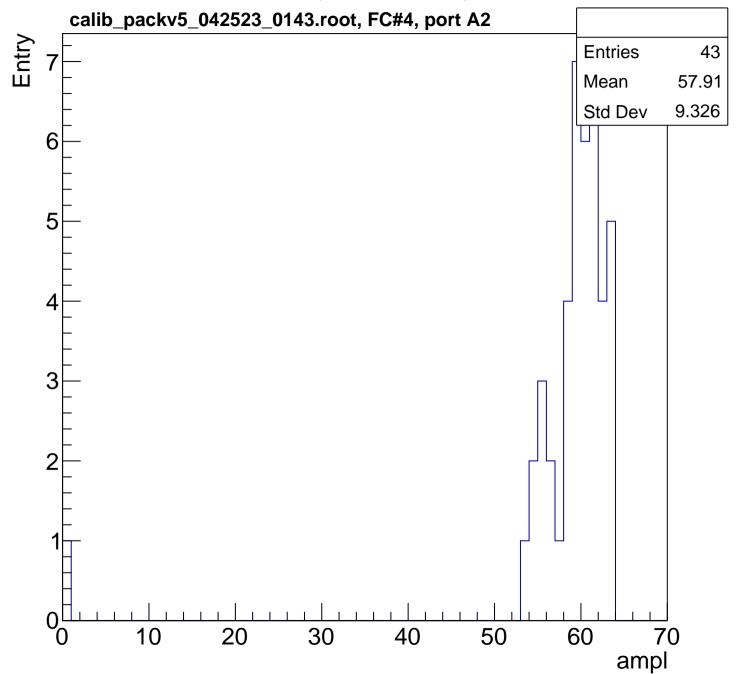


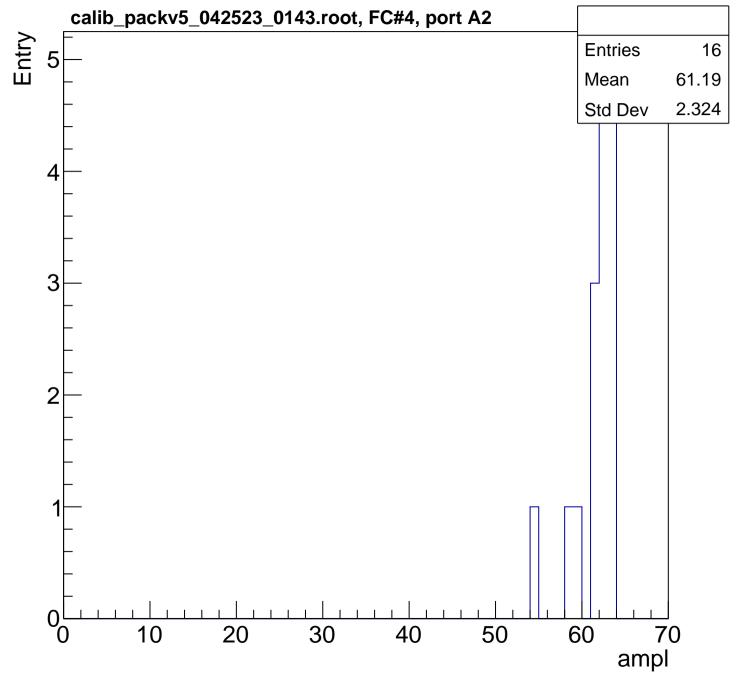


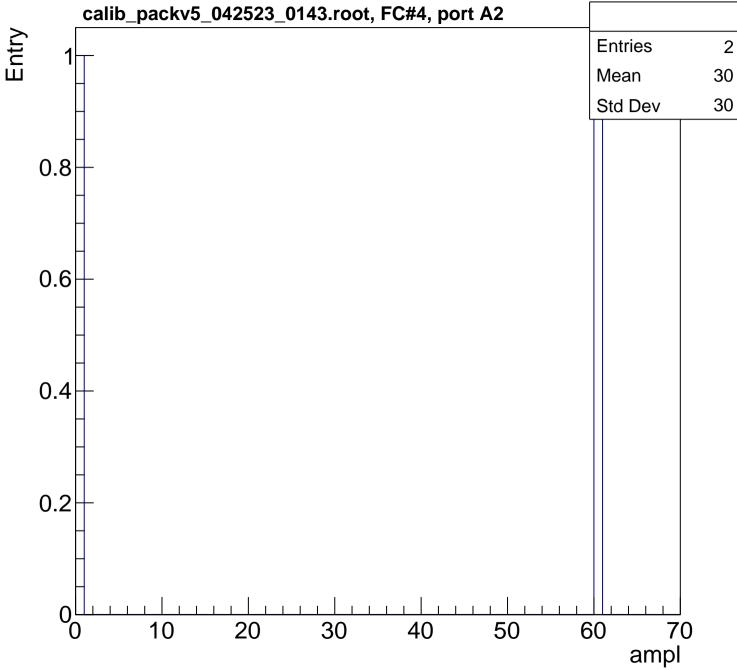


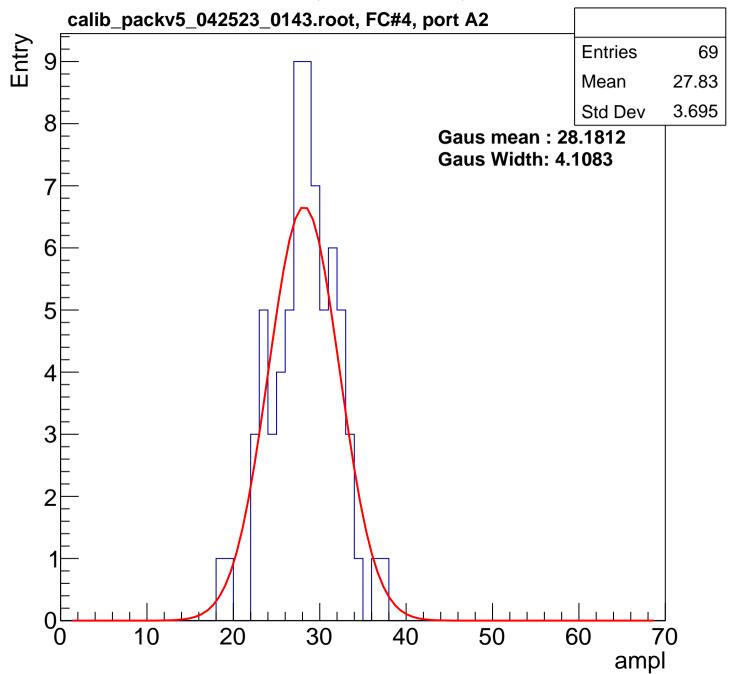


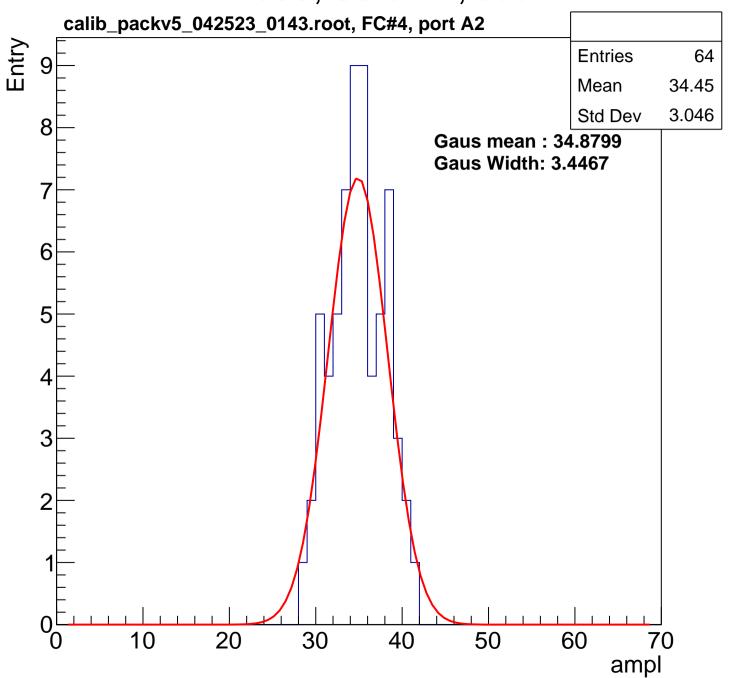


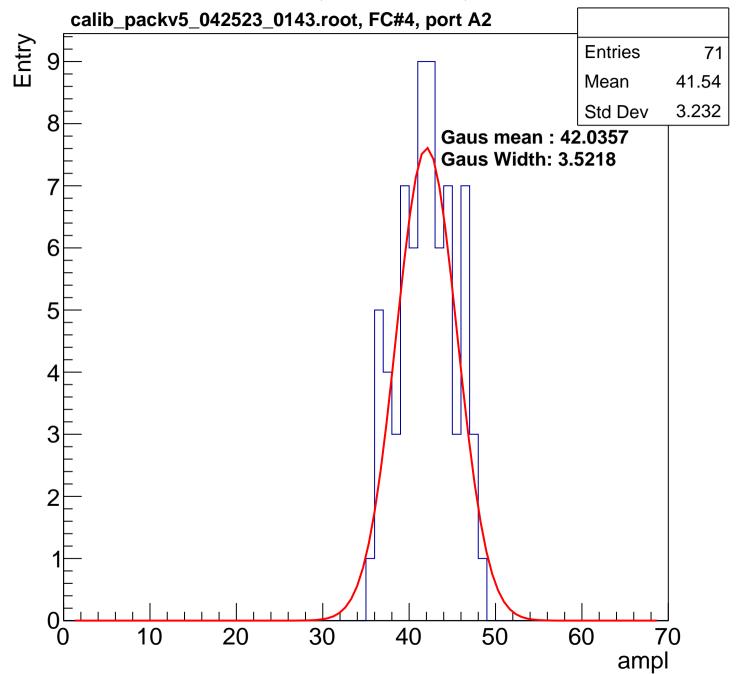


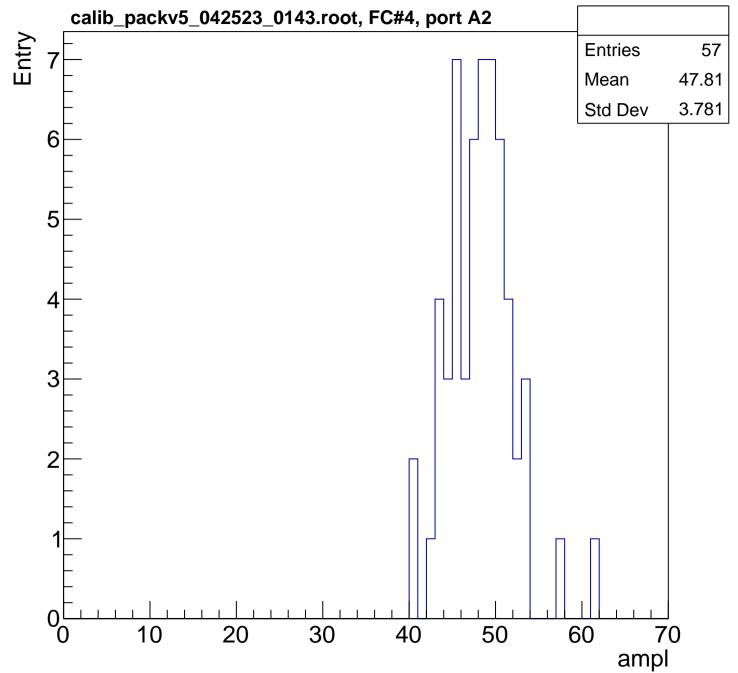


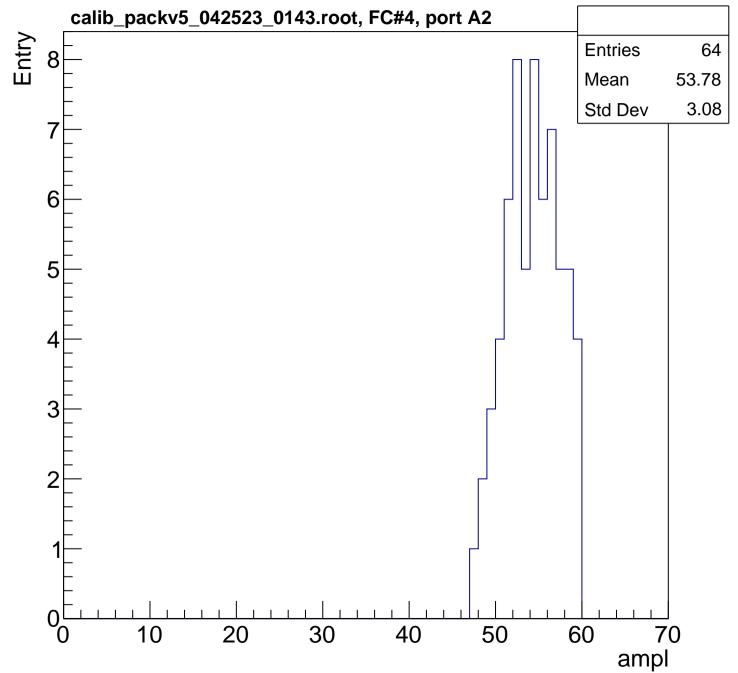


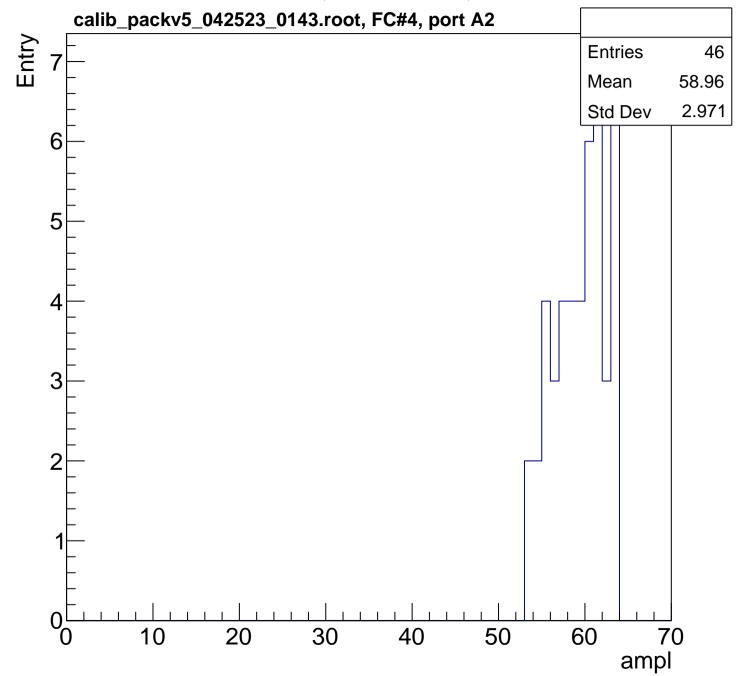


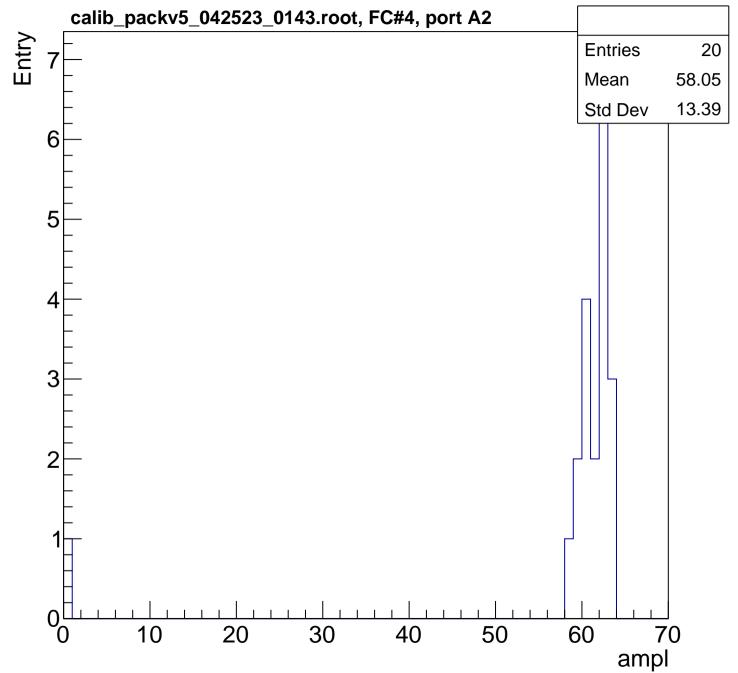




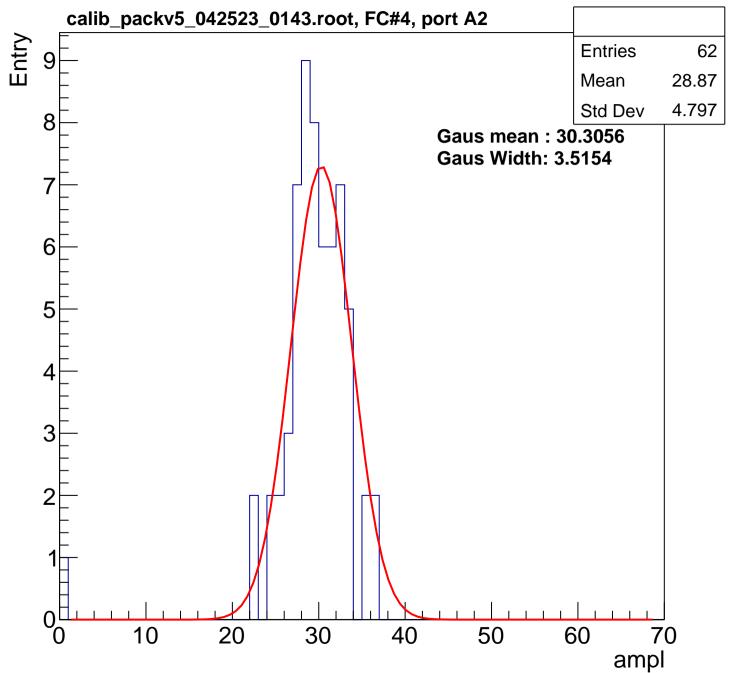


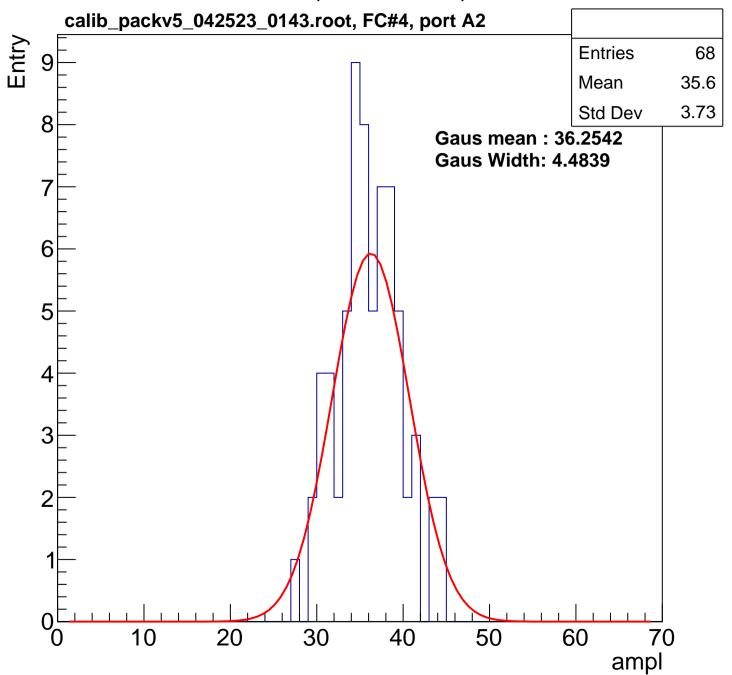


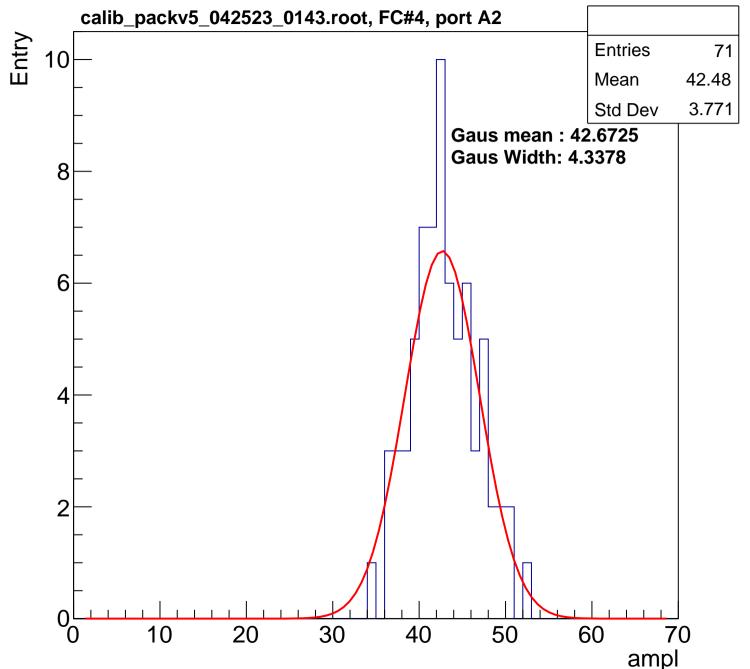


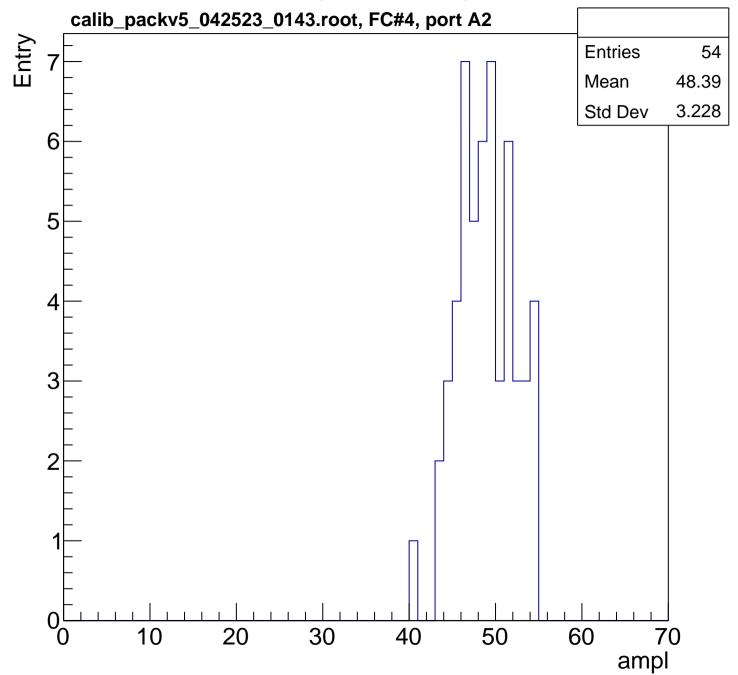


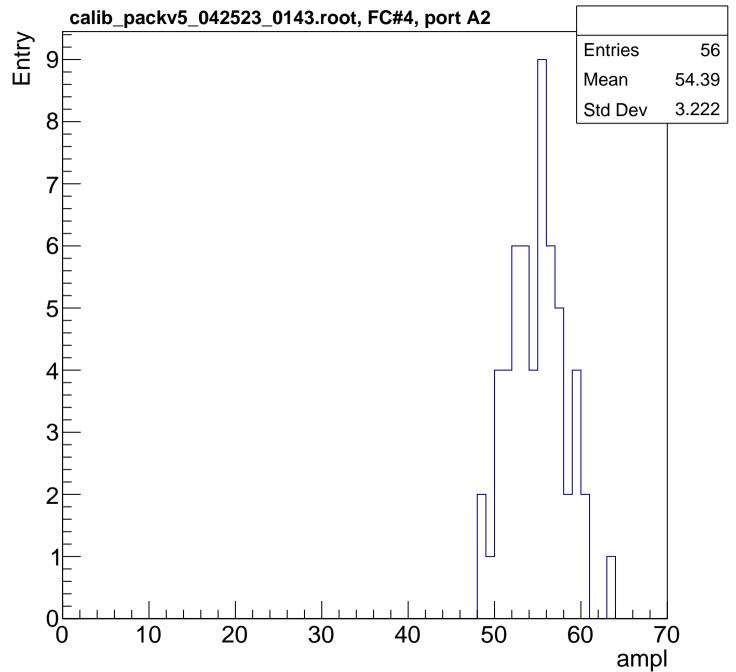
B1L100S, U3-ch72, adc7 calib_packv5_042523_0143.root, FC#4, port A2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

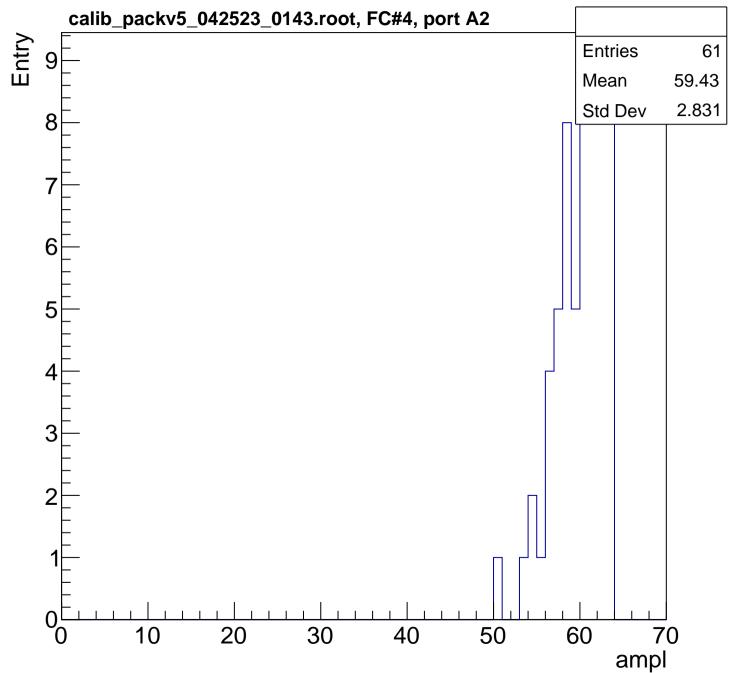


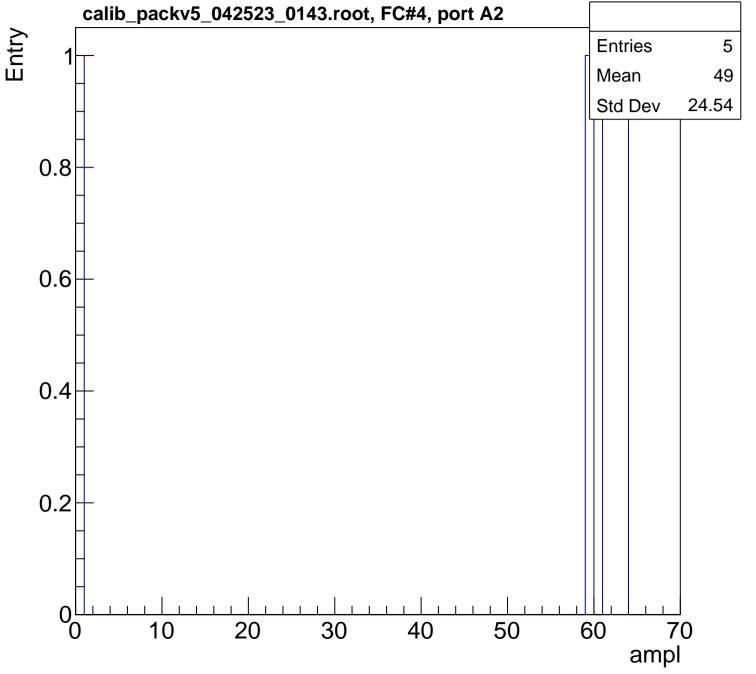


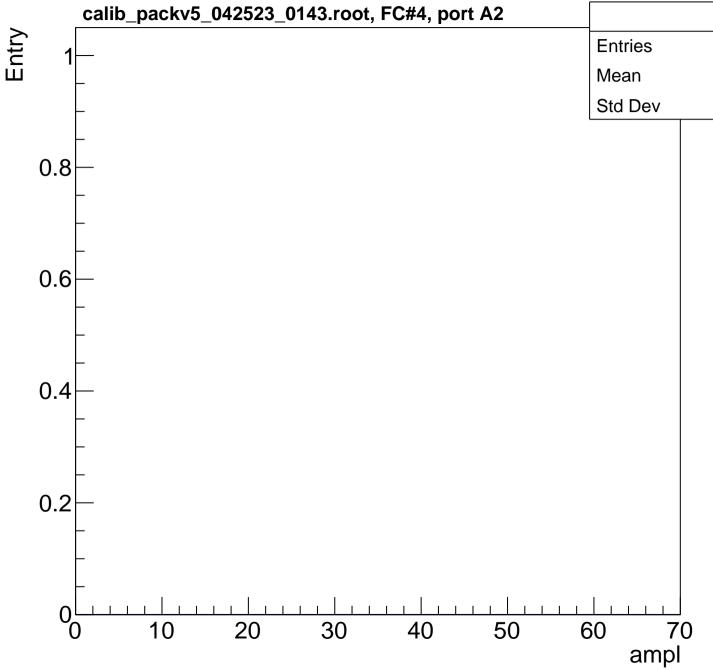


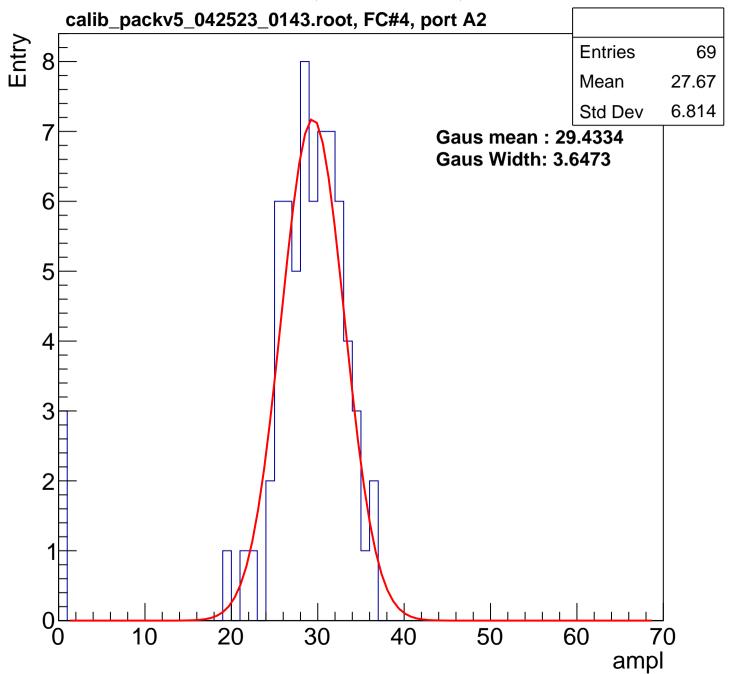


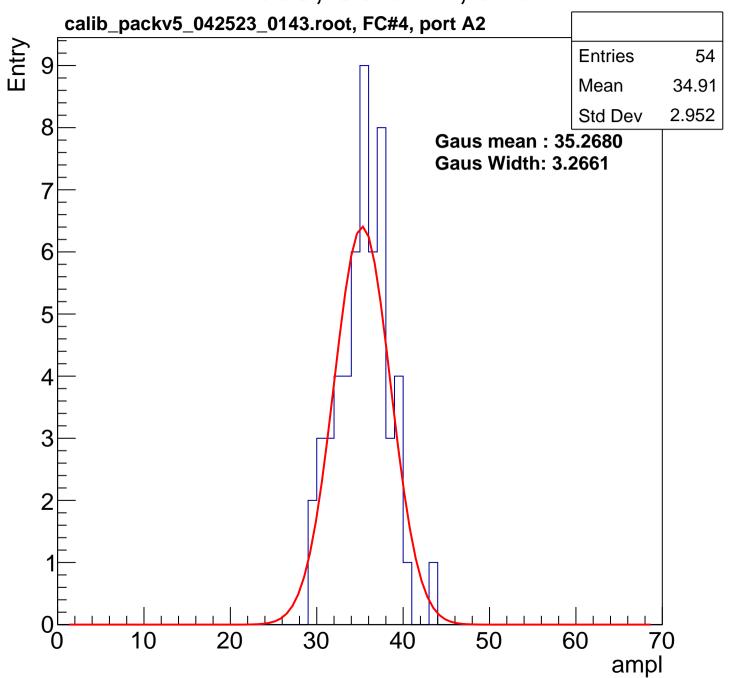


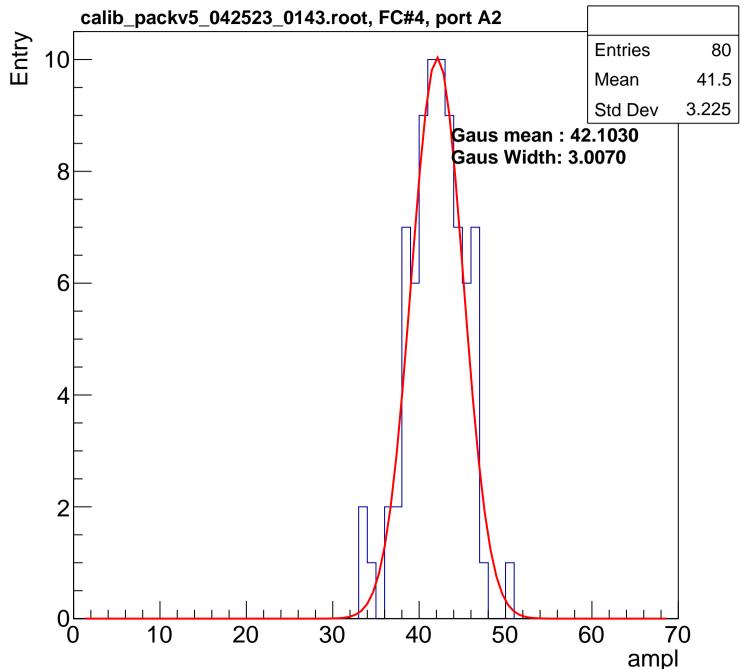


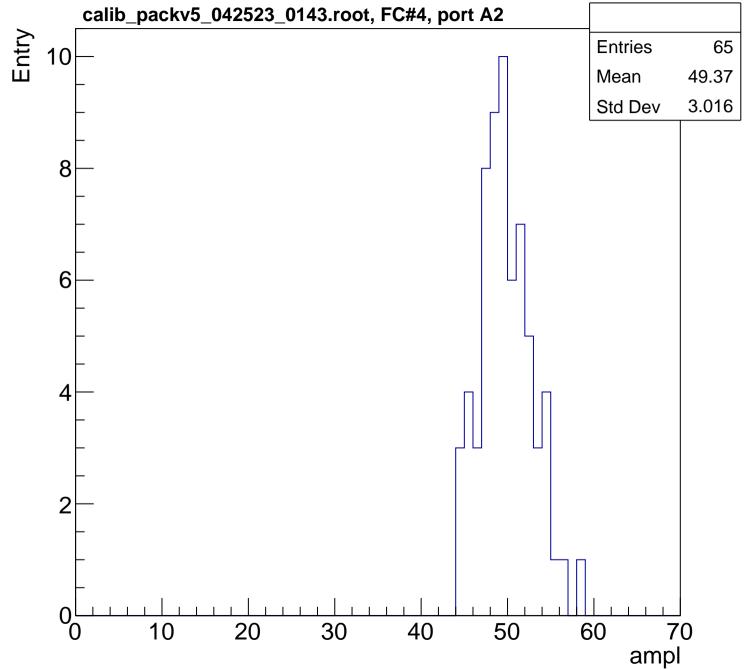


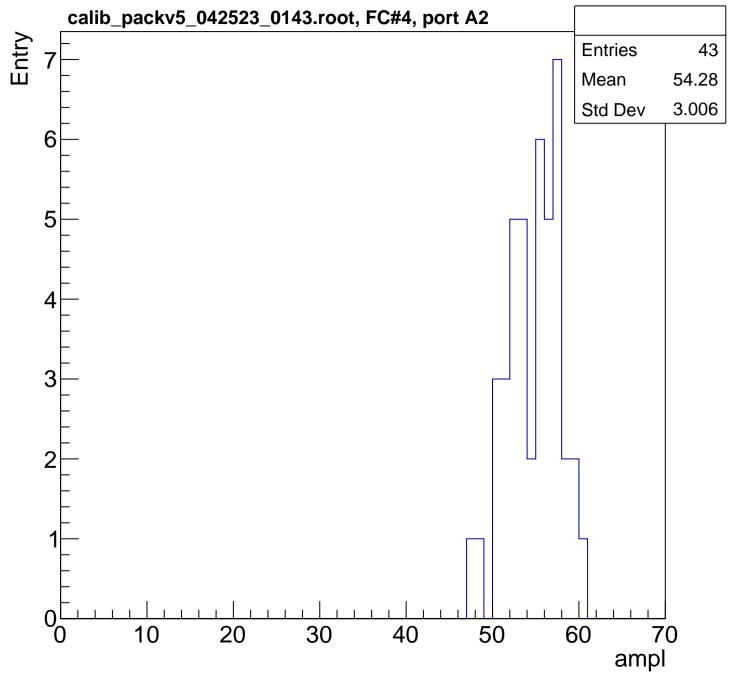


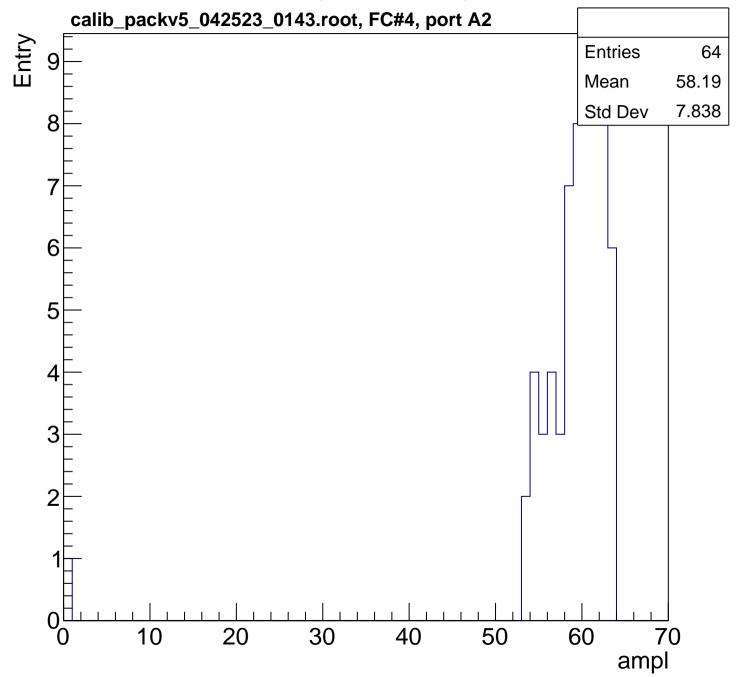


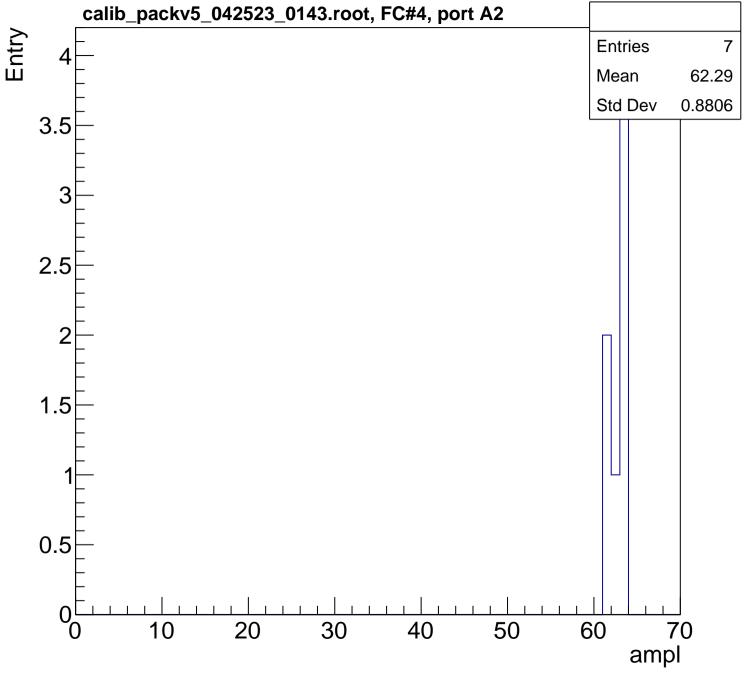


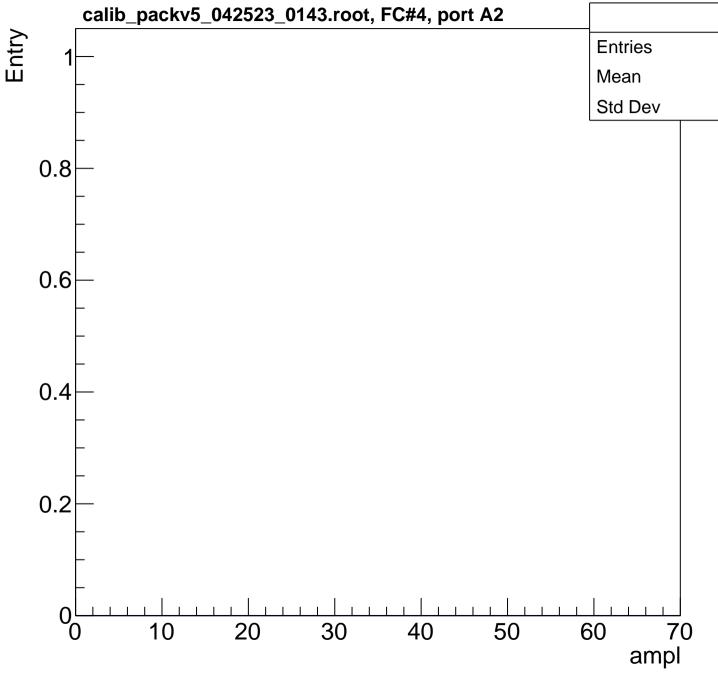


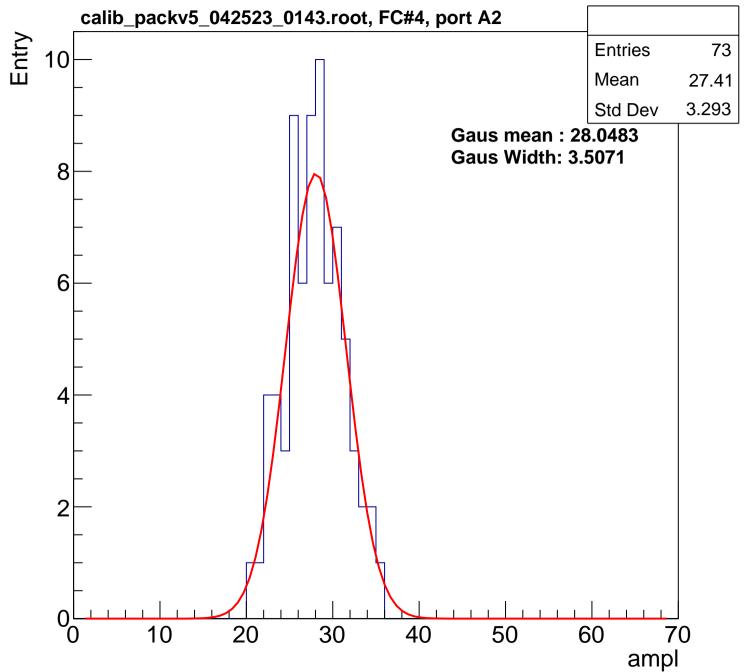


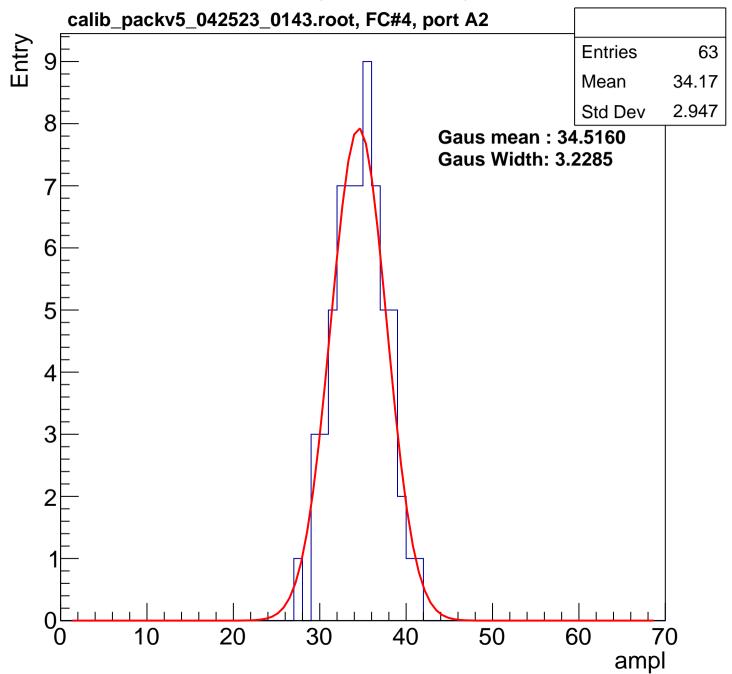


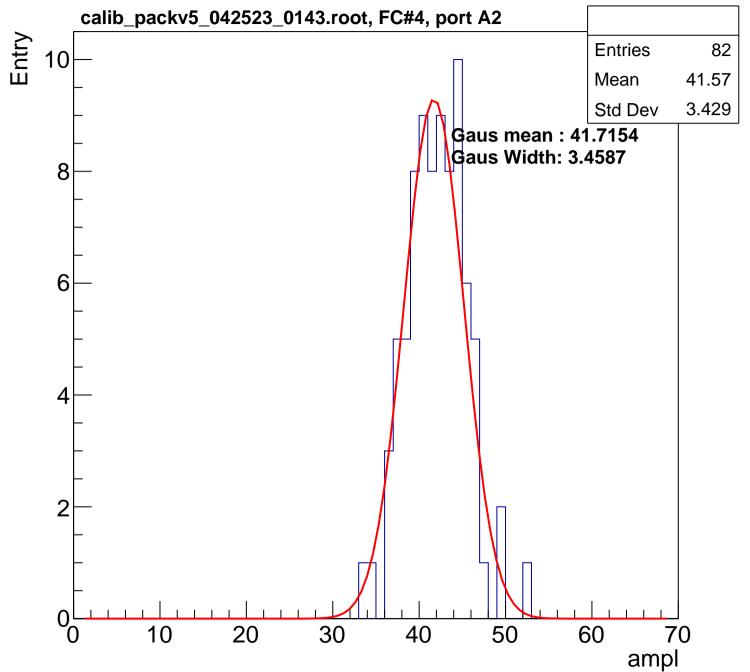


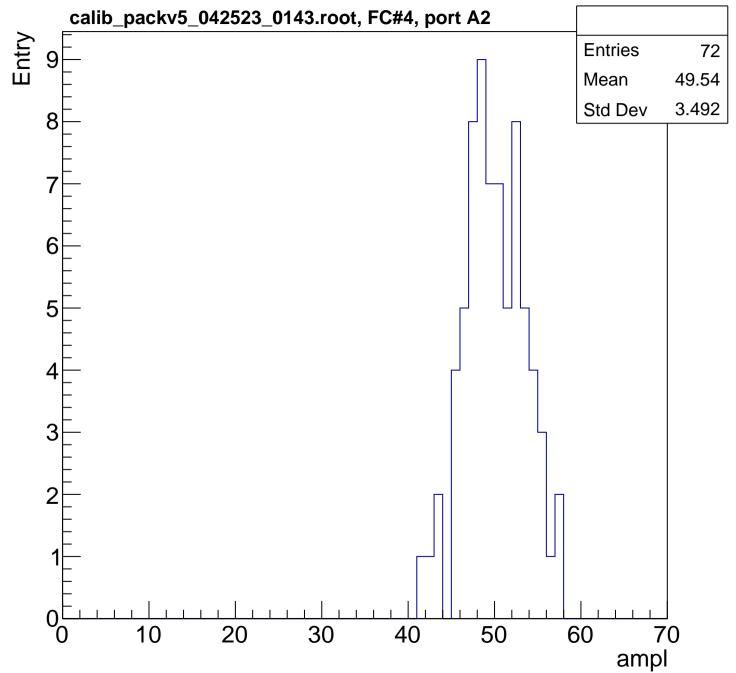


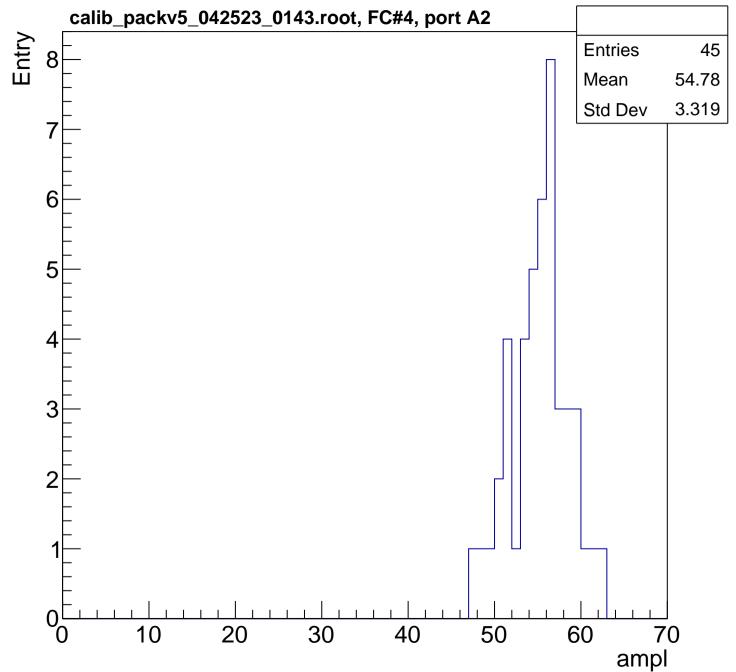


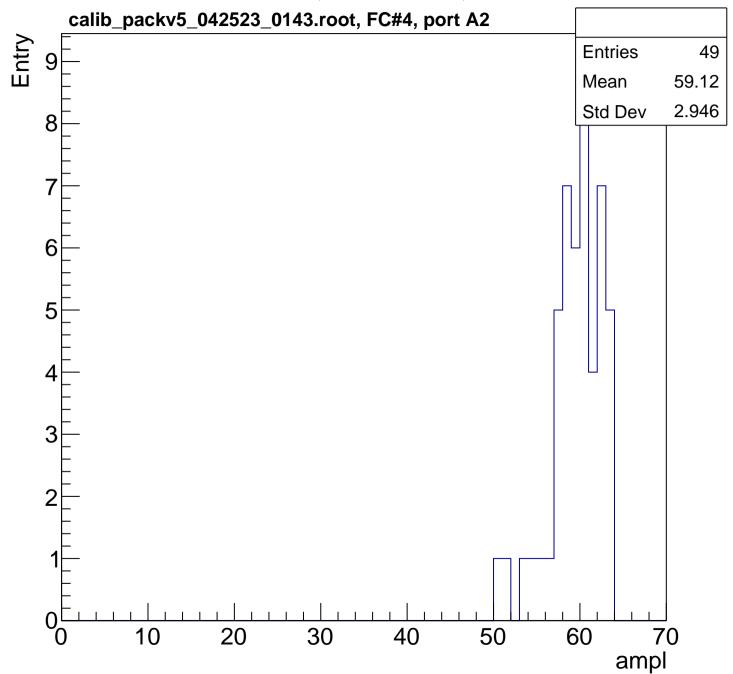


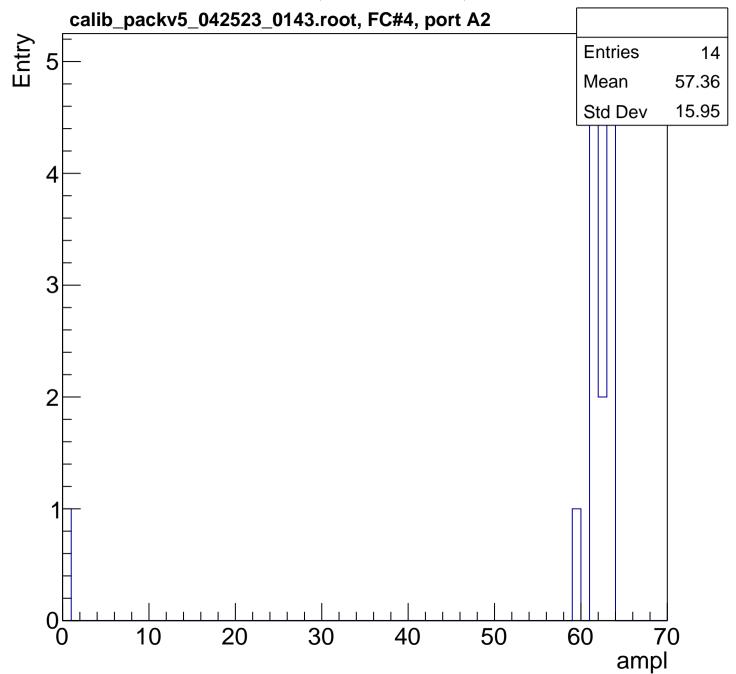




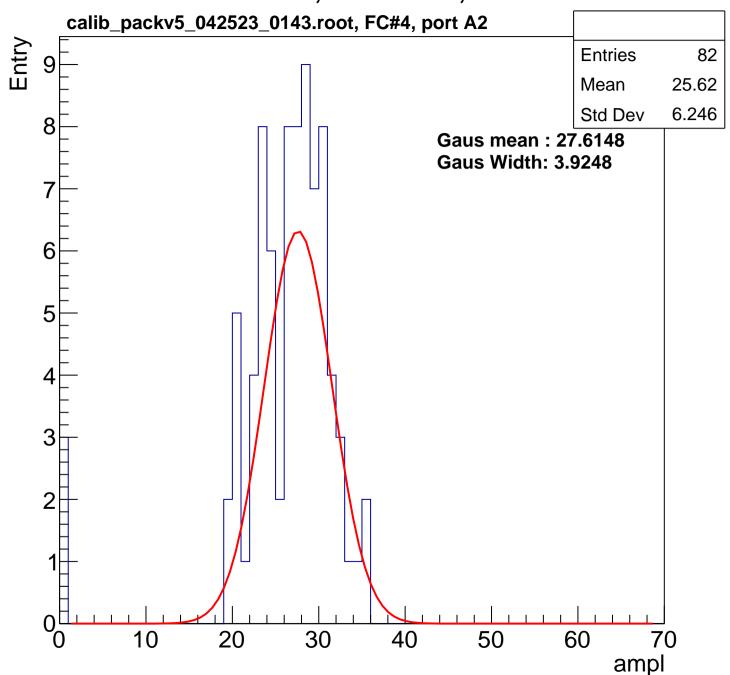


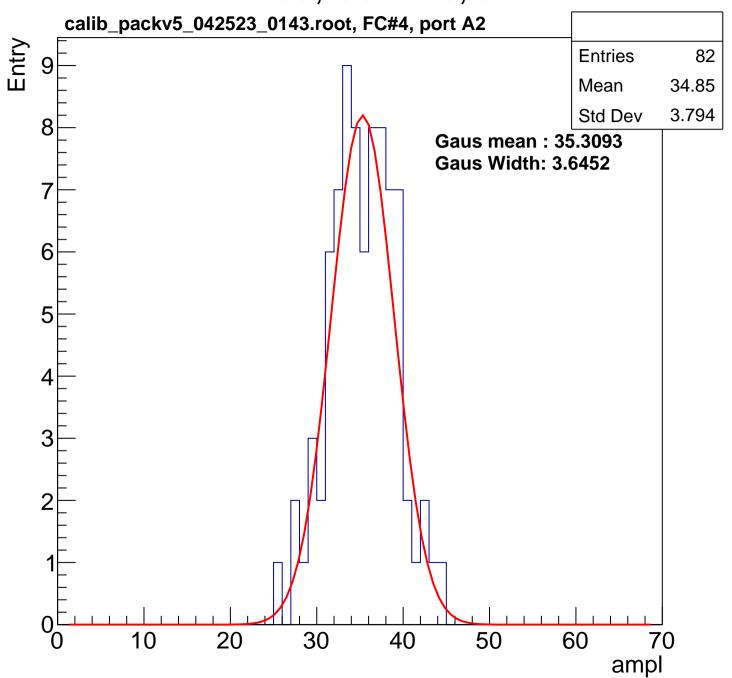


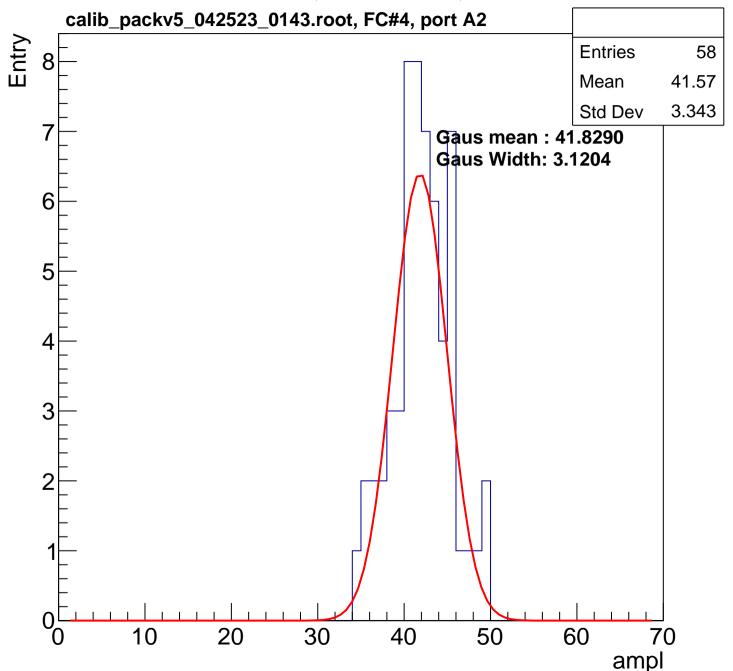


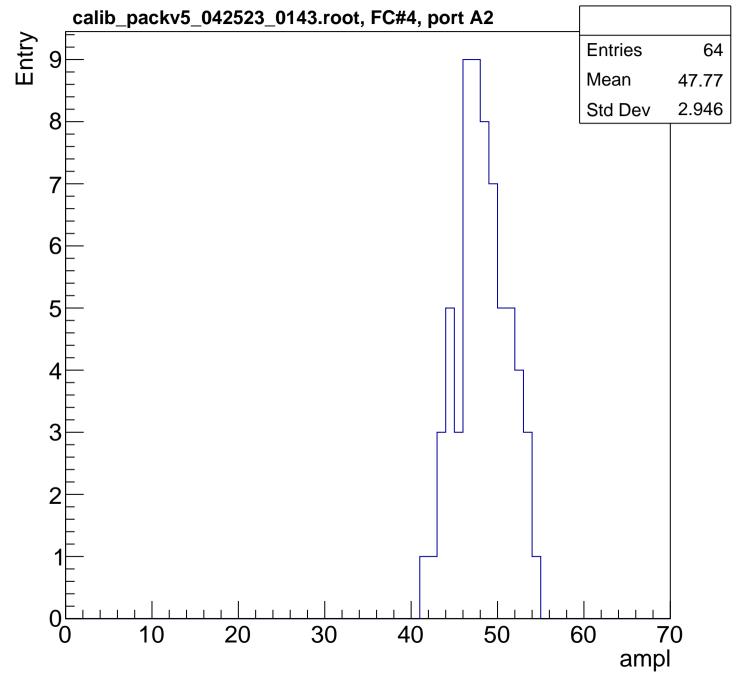


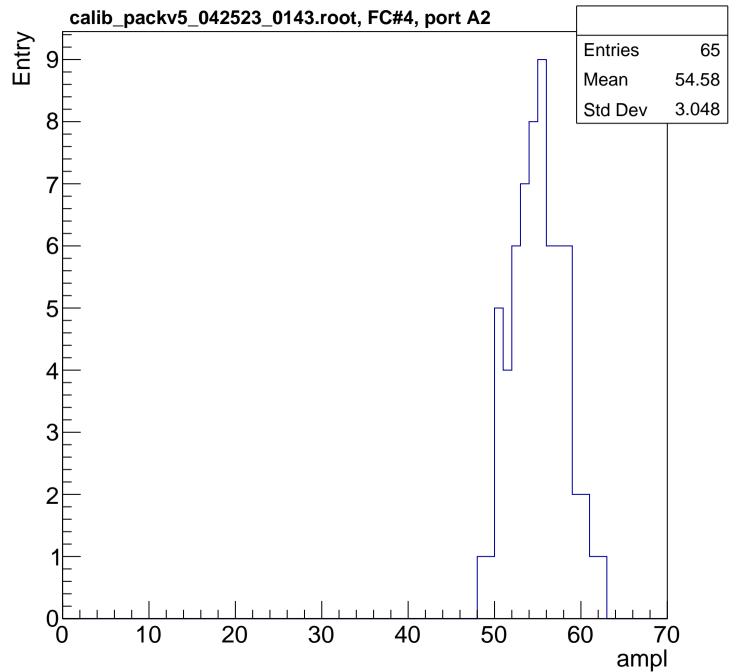


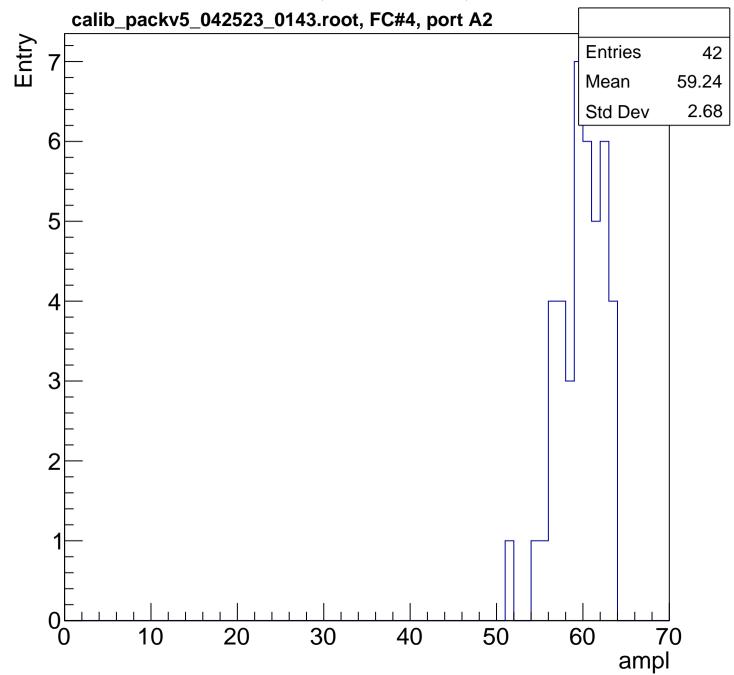


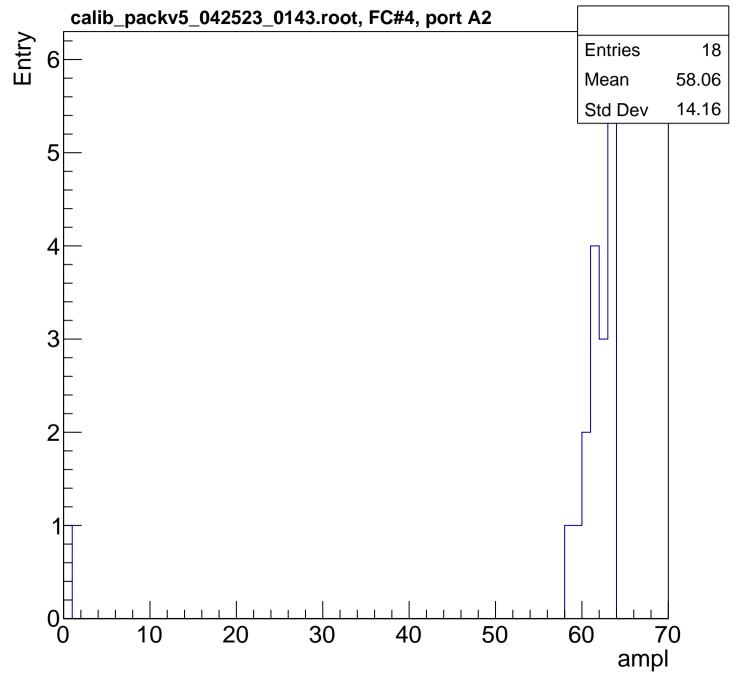




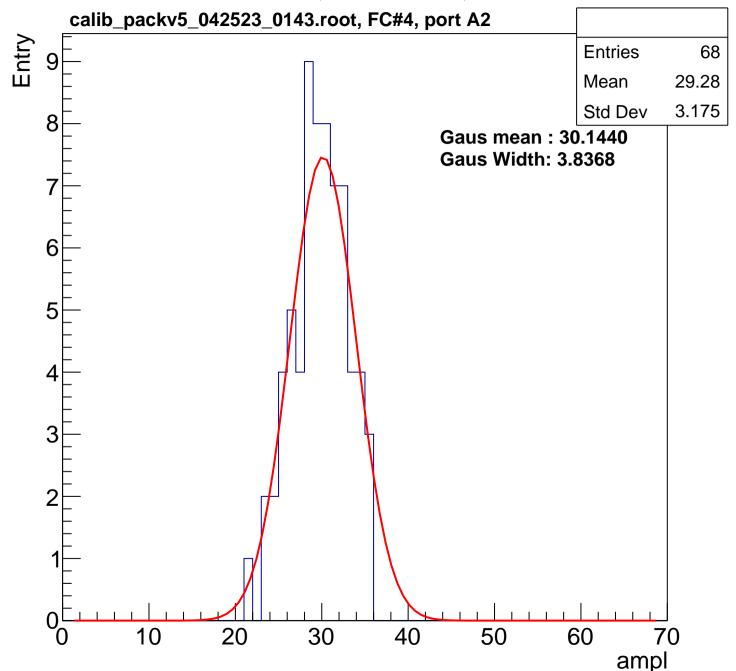


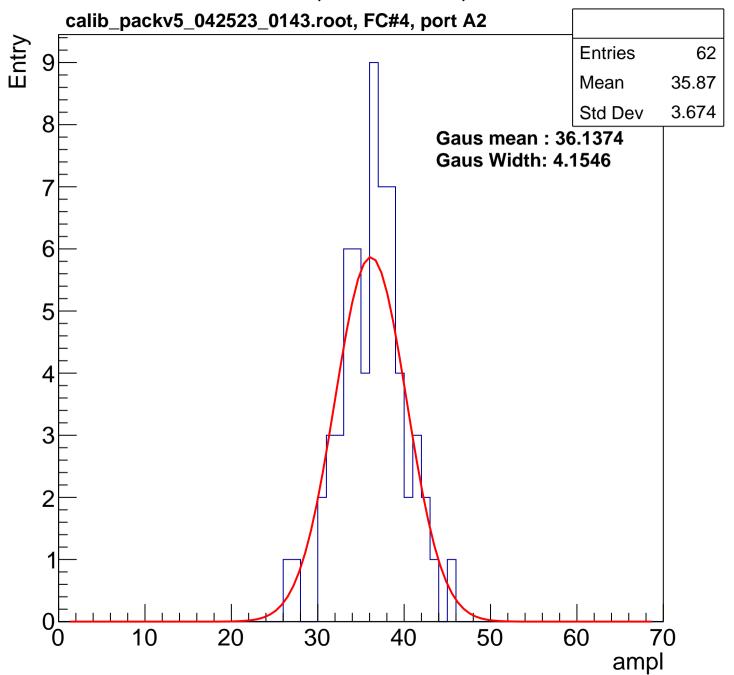


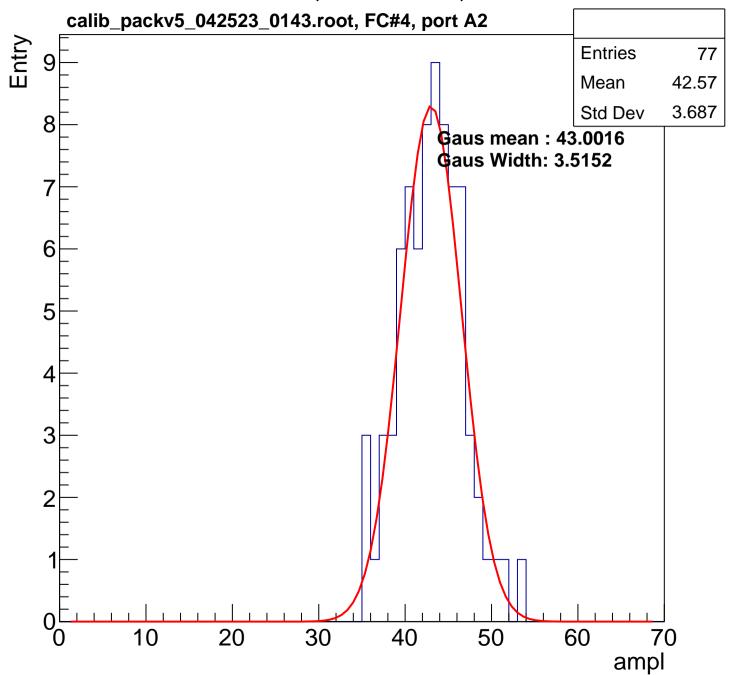


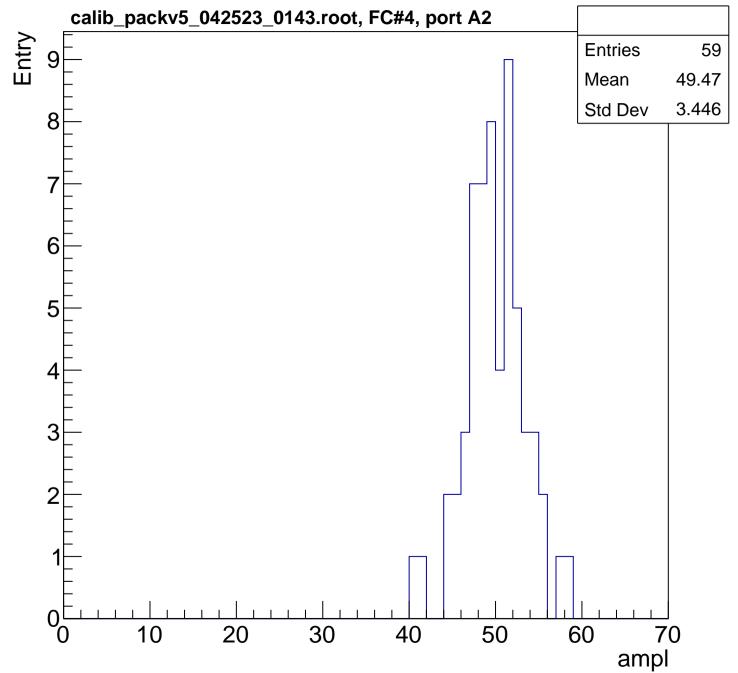


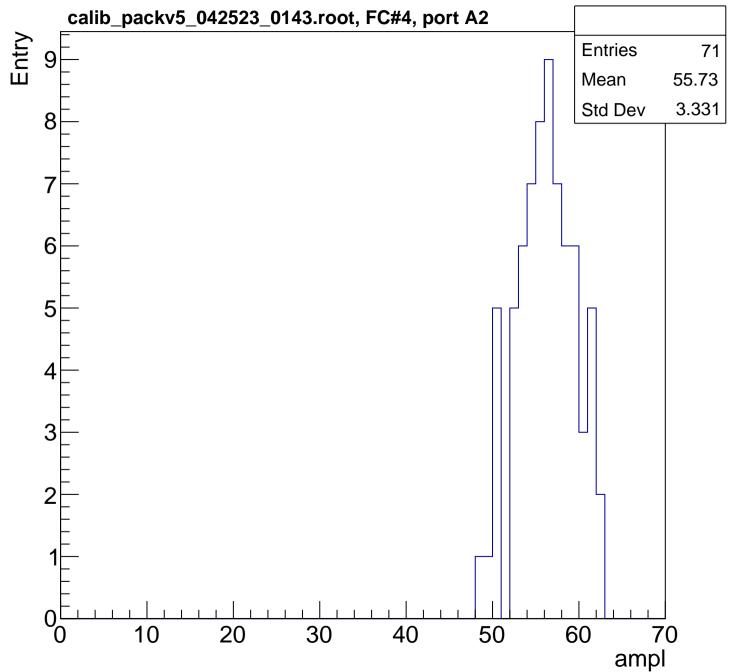
B1L100S, U3-ch76, adc7 calib_packv5_042523_0143.root, FC#4, port A2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

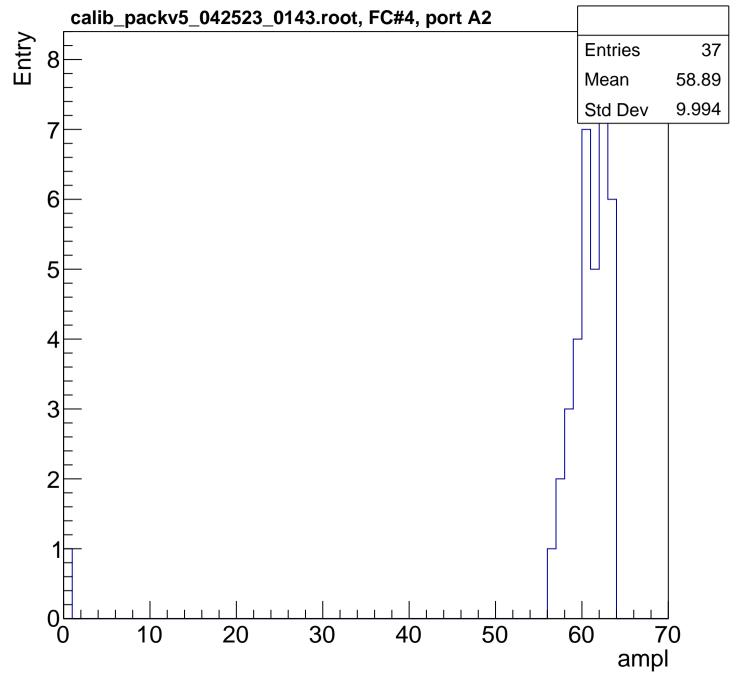


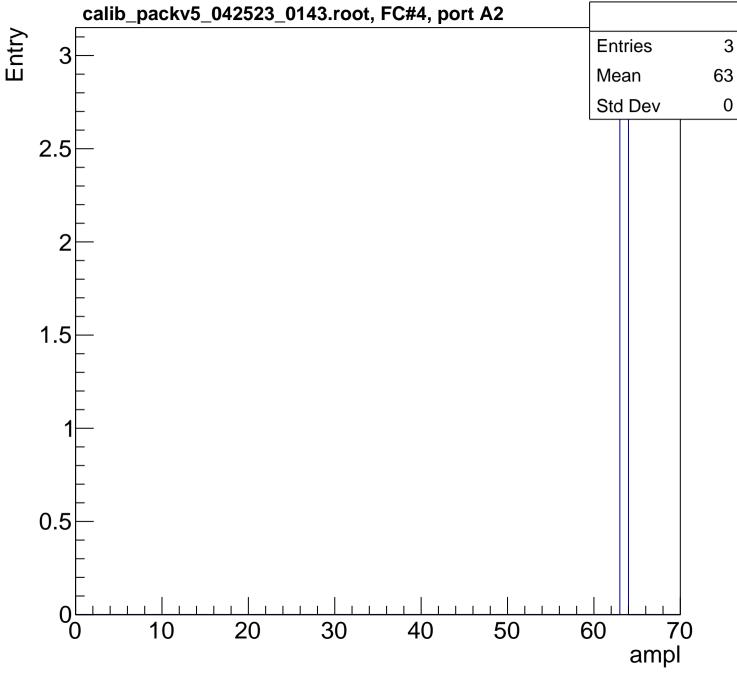


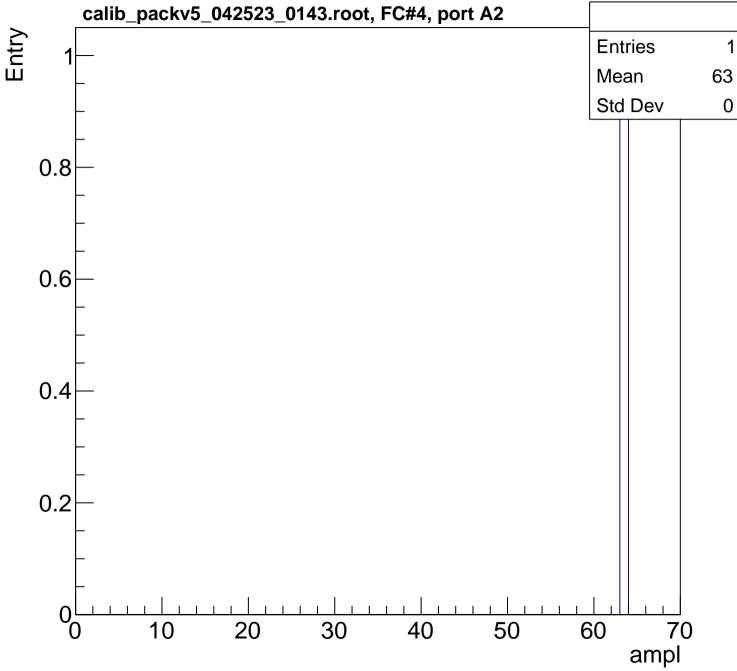


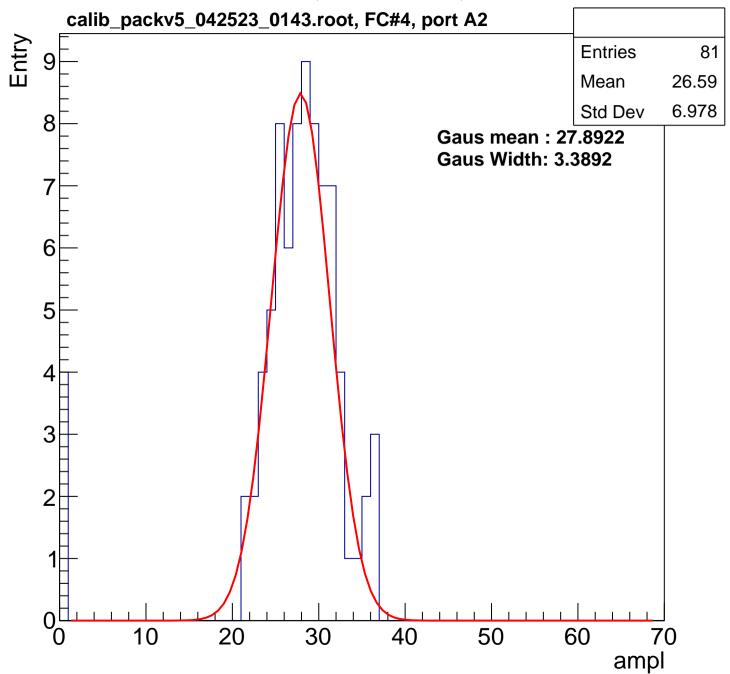


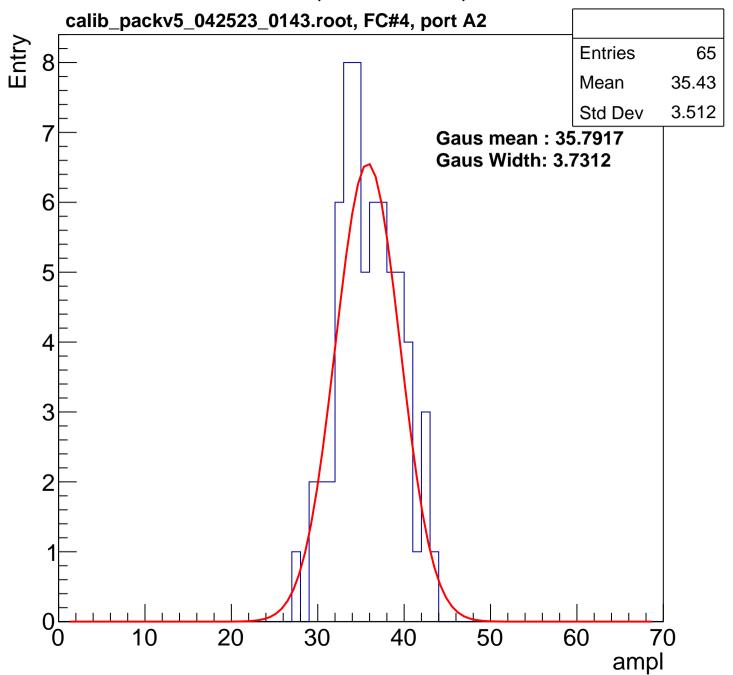


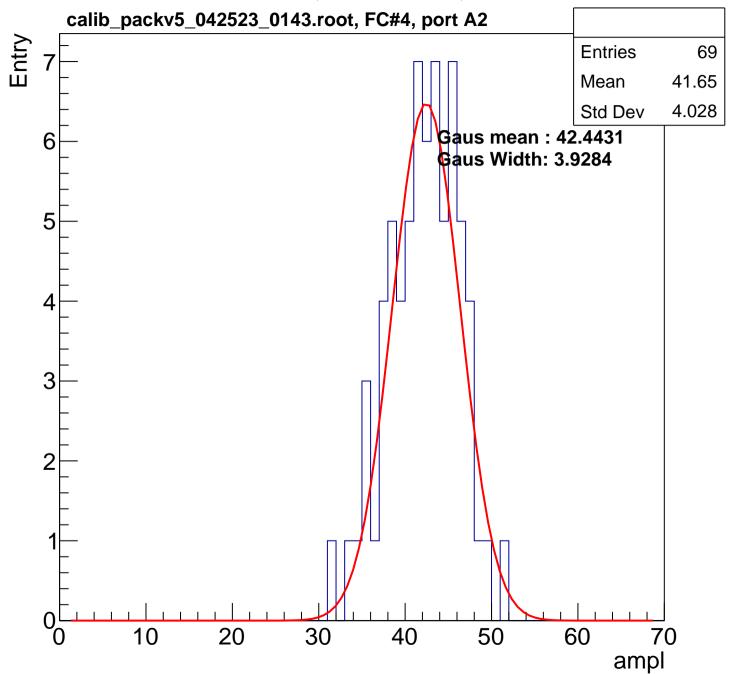


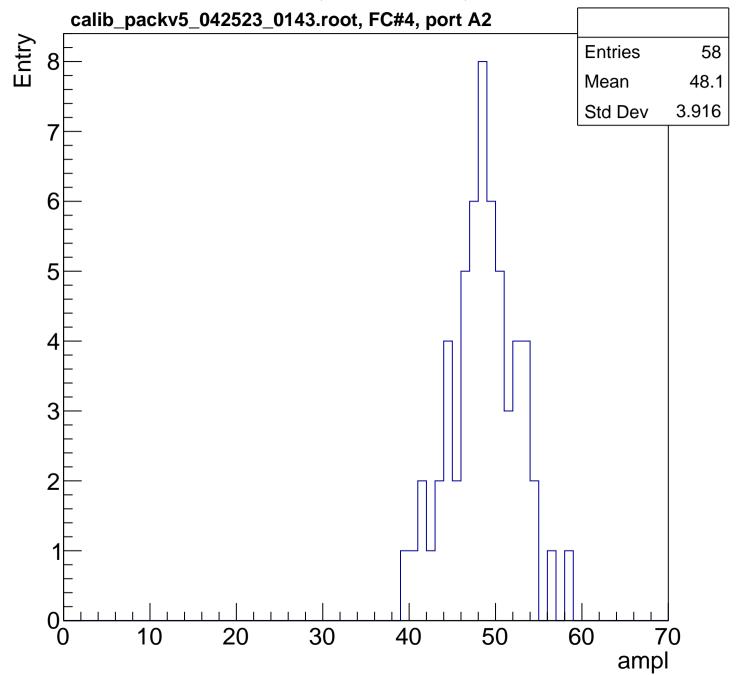


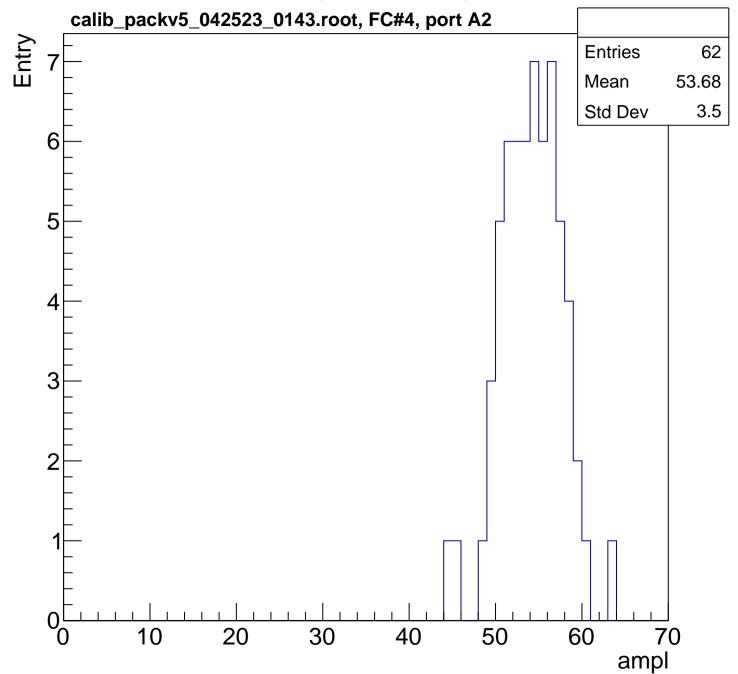


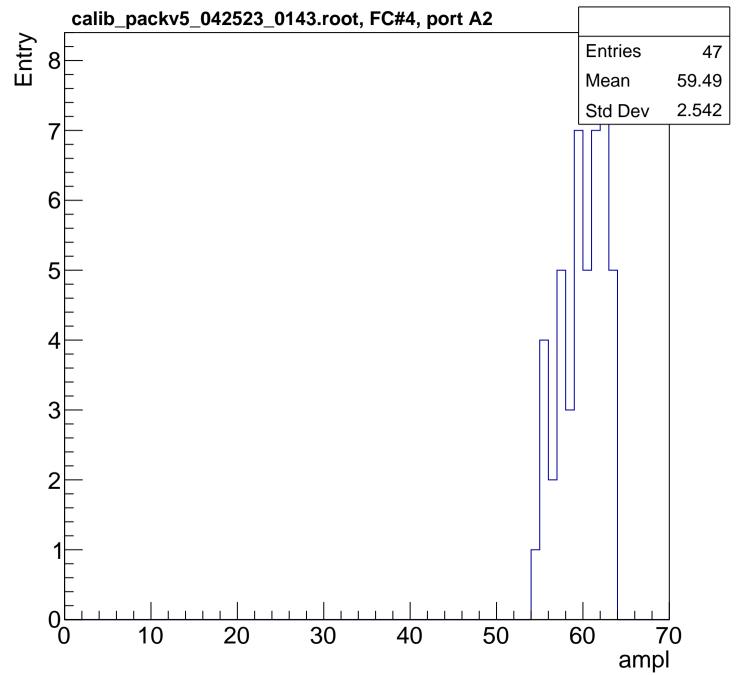


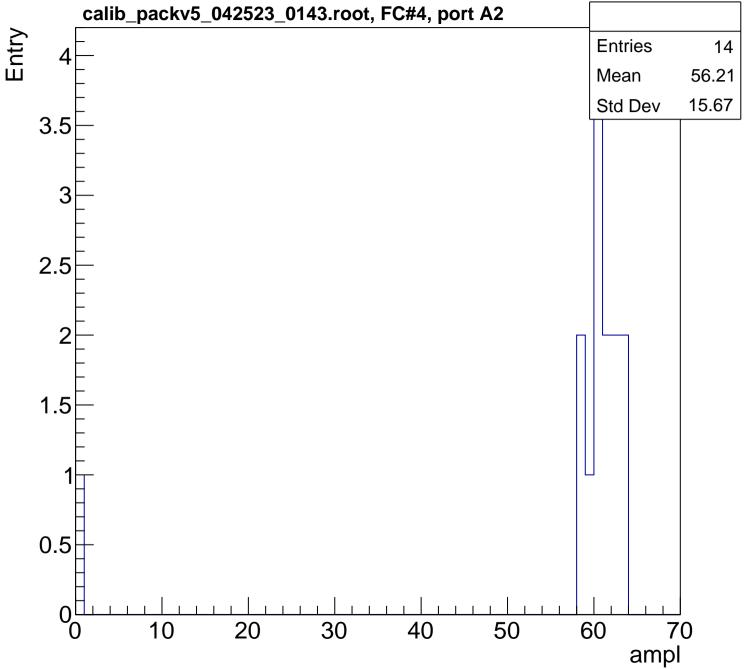


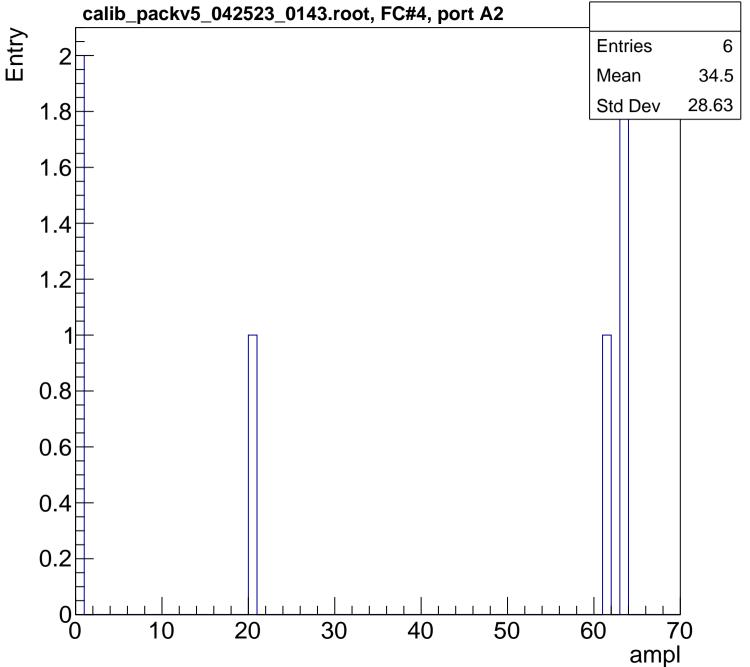


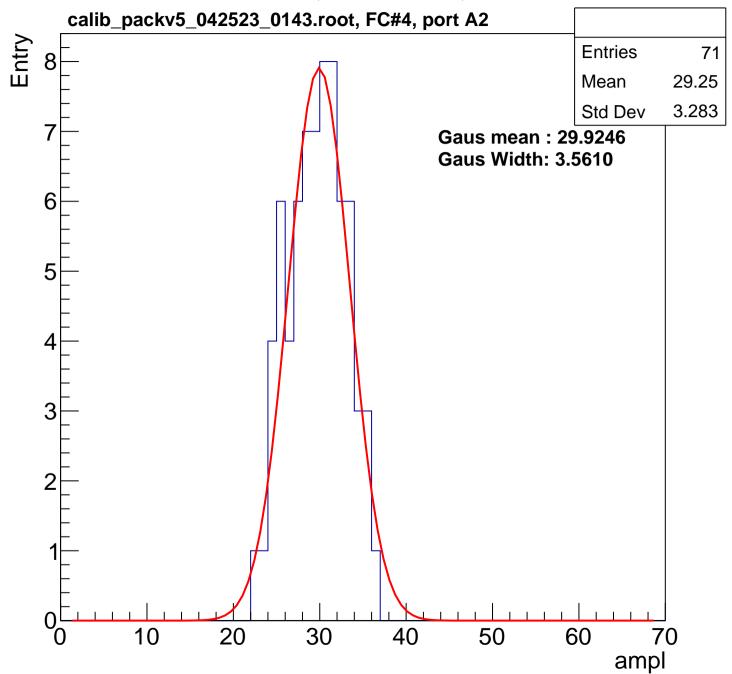


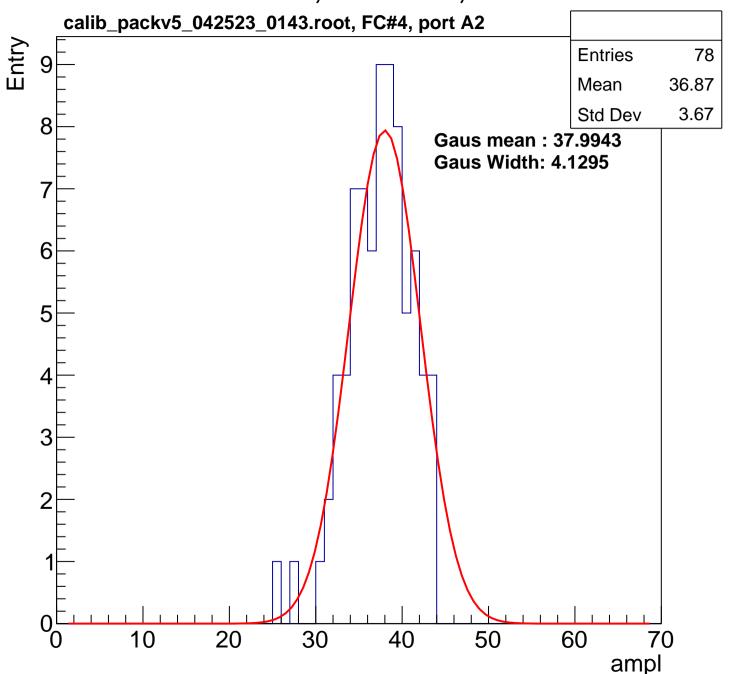


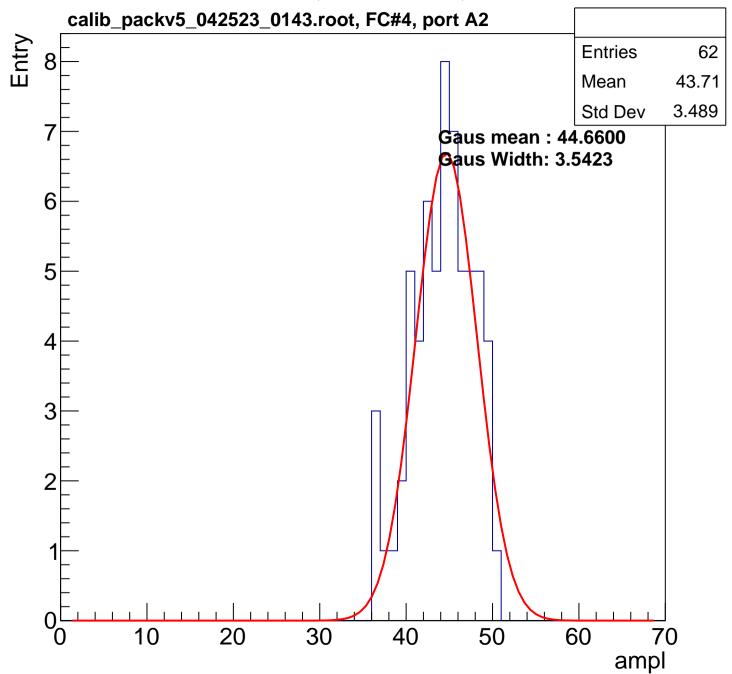


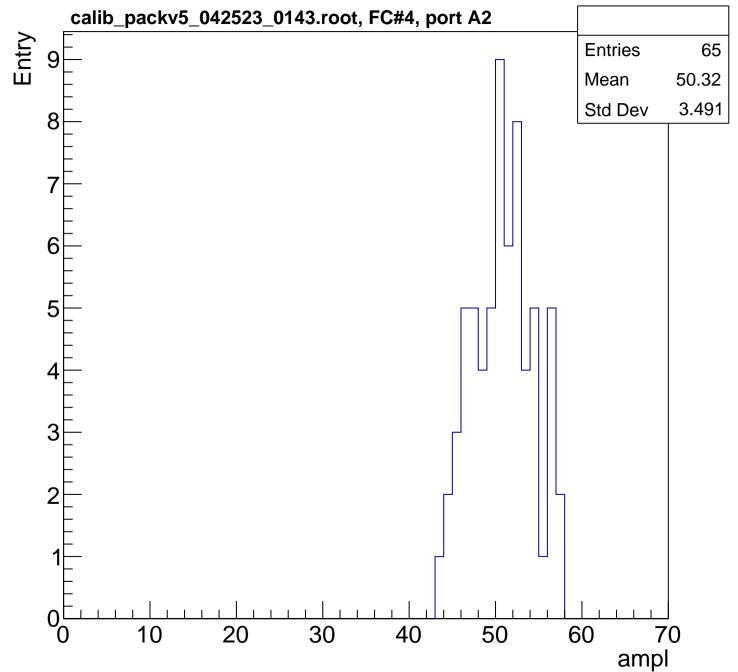


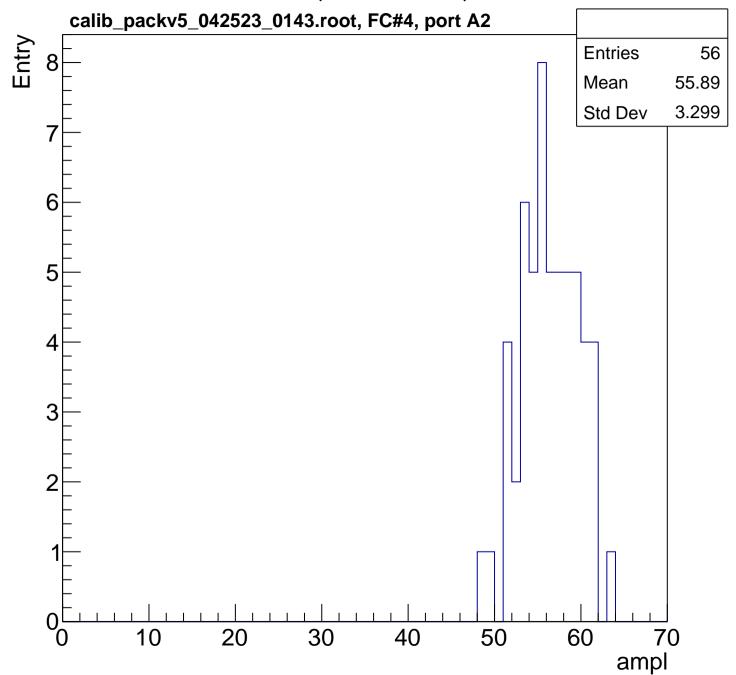


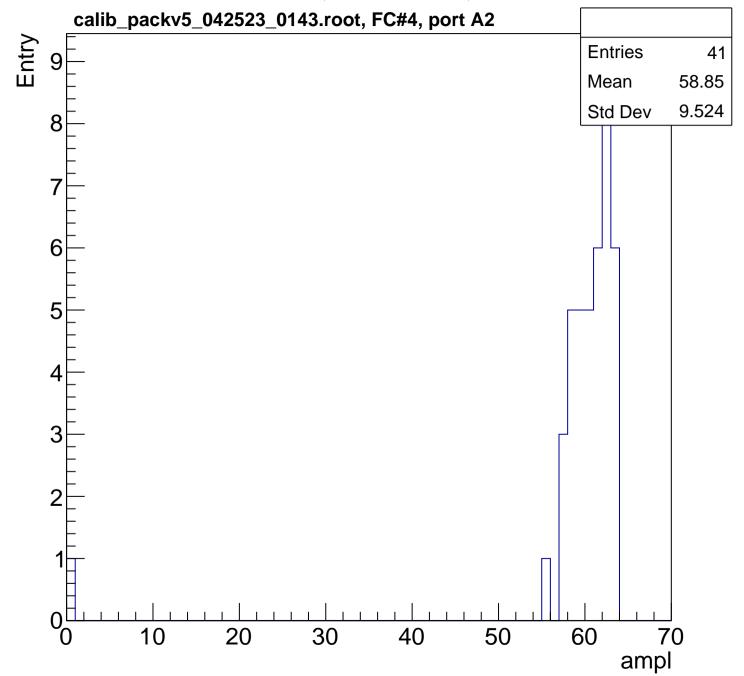


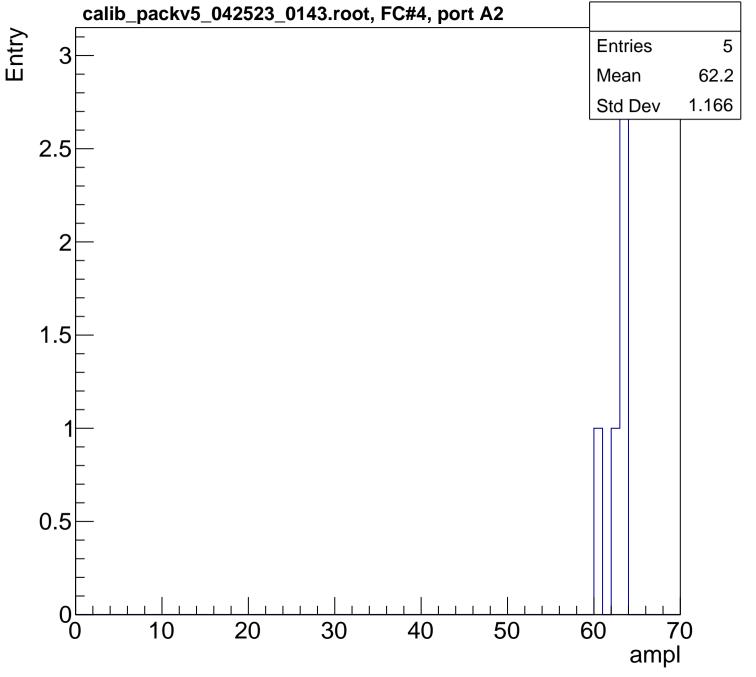




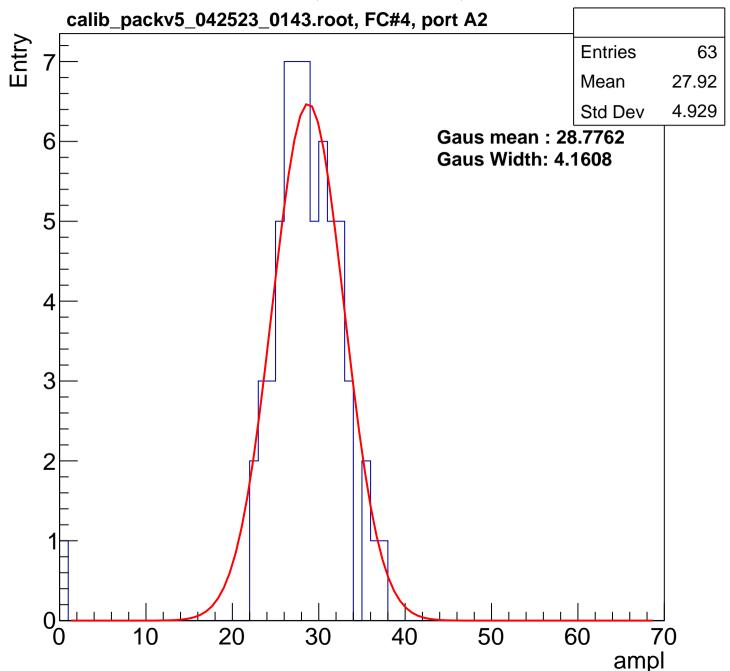


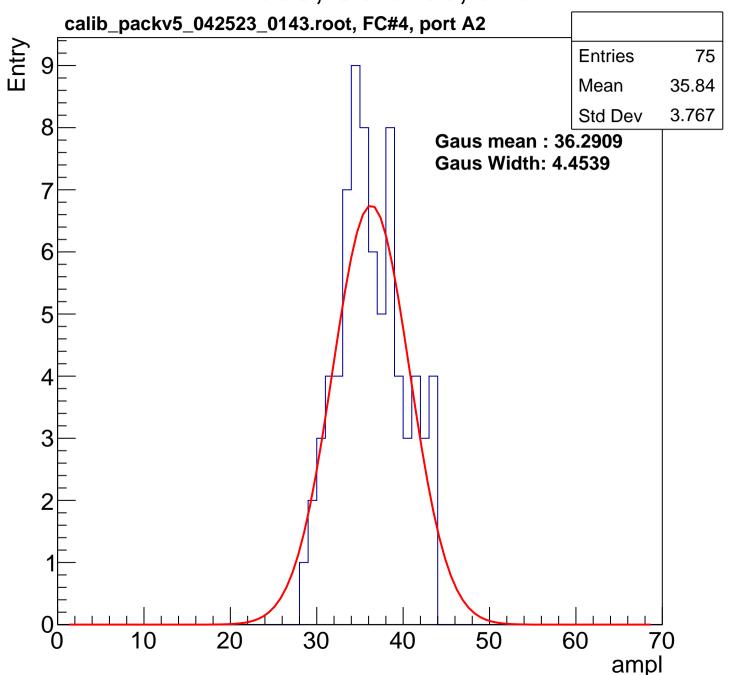


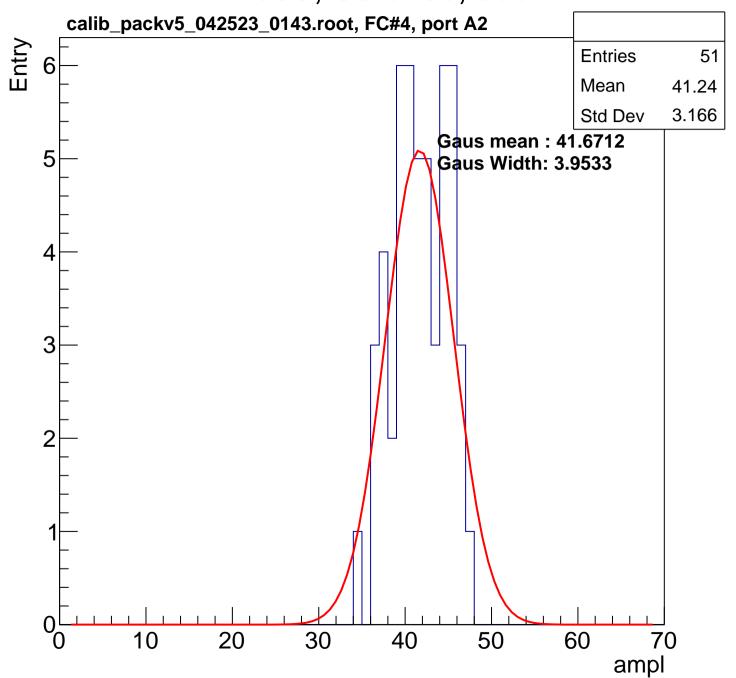


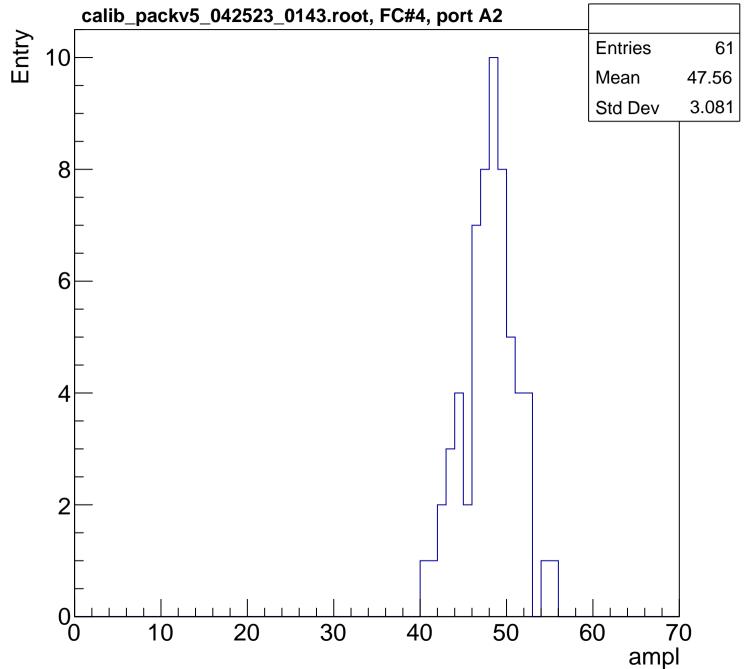


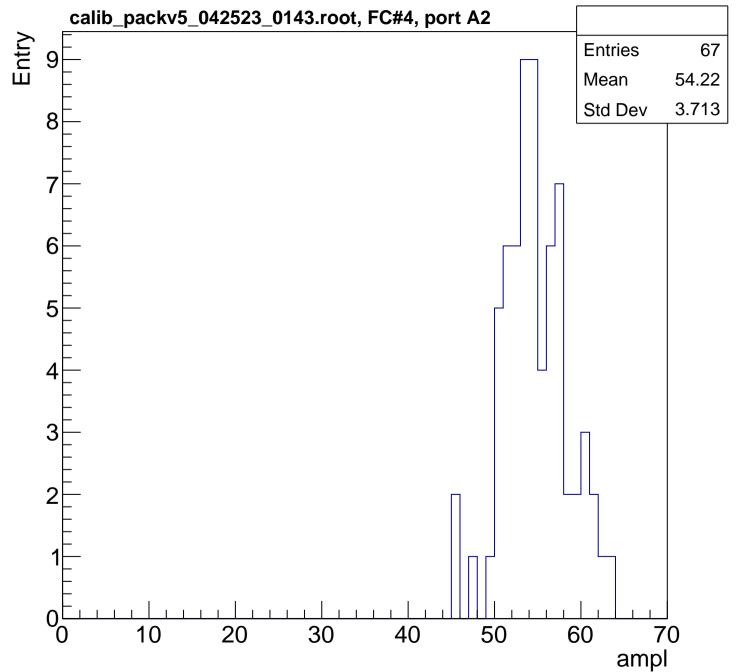


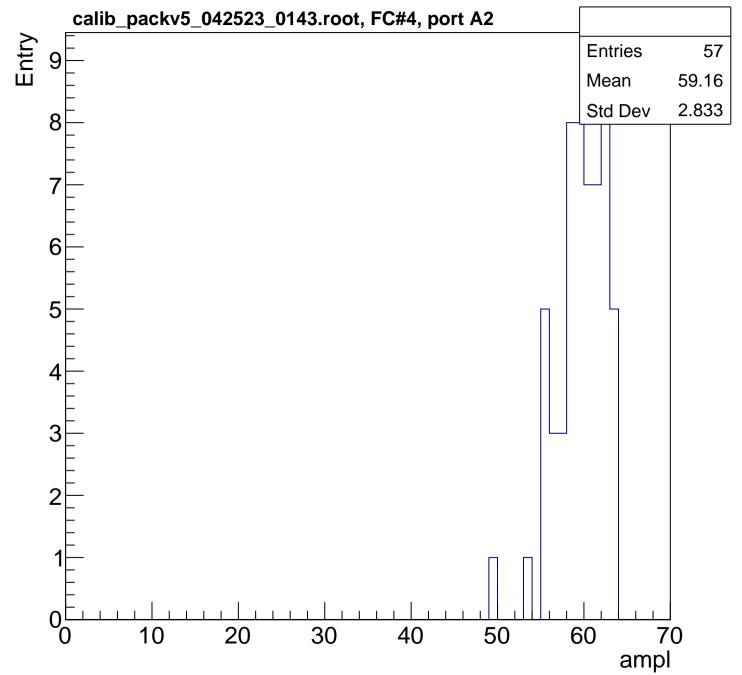


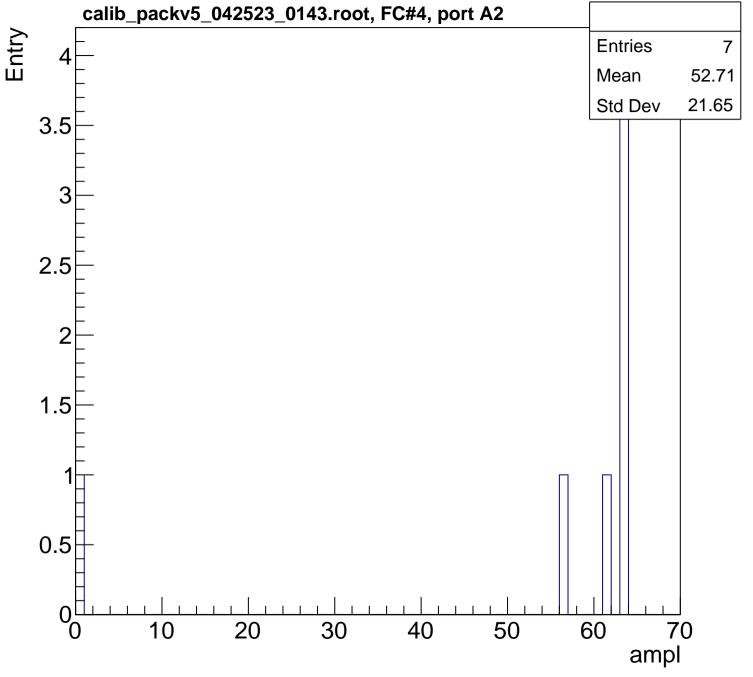


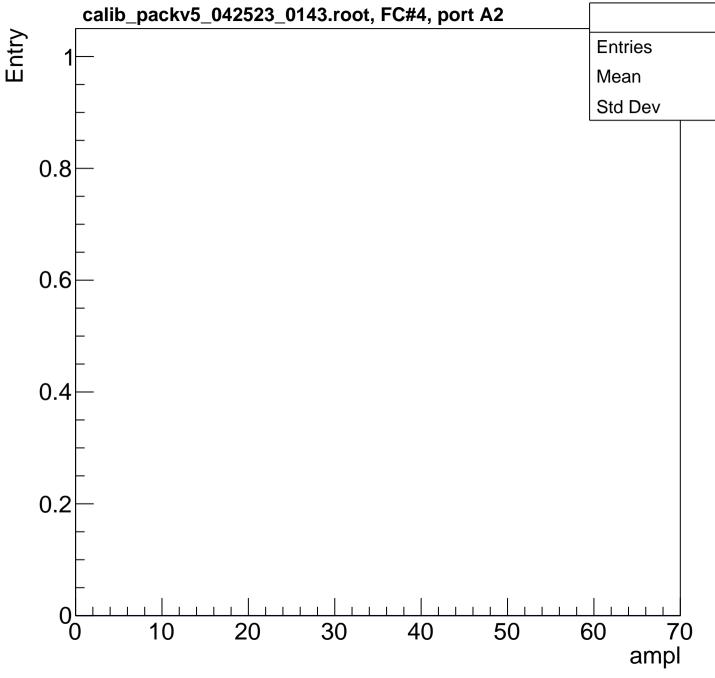


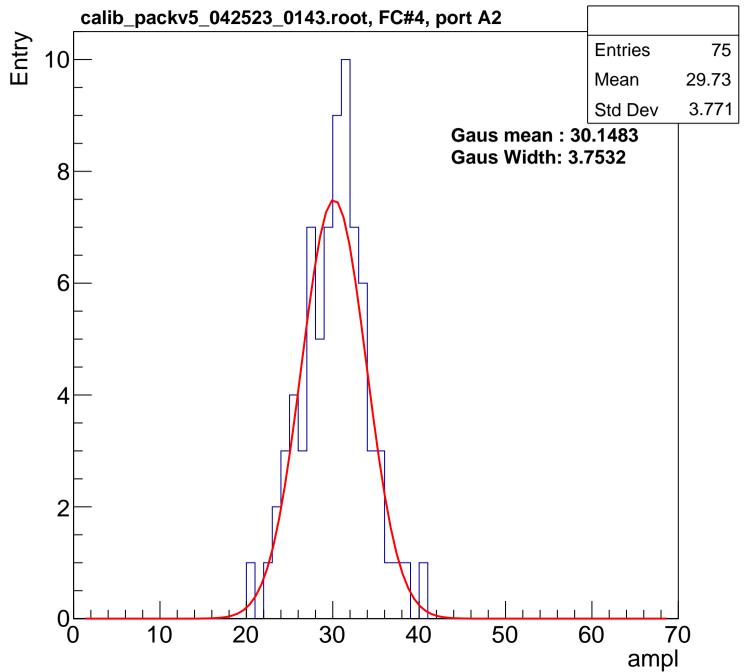


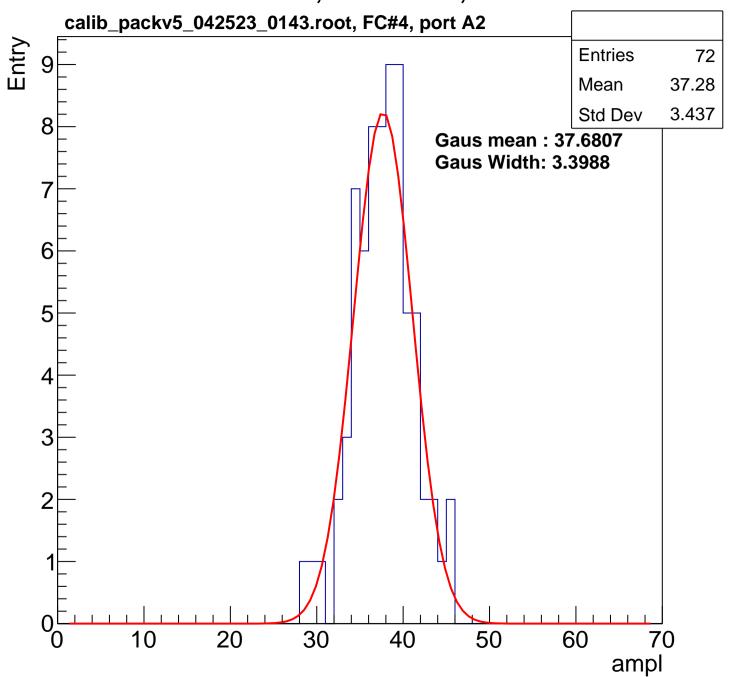


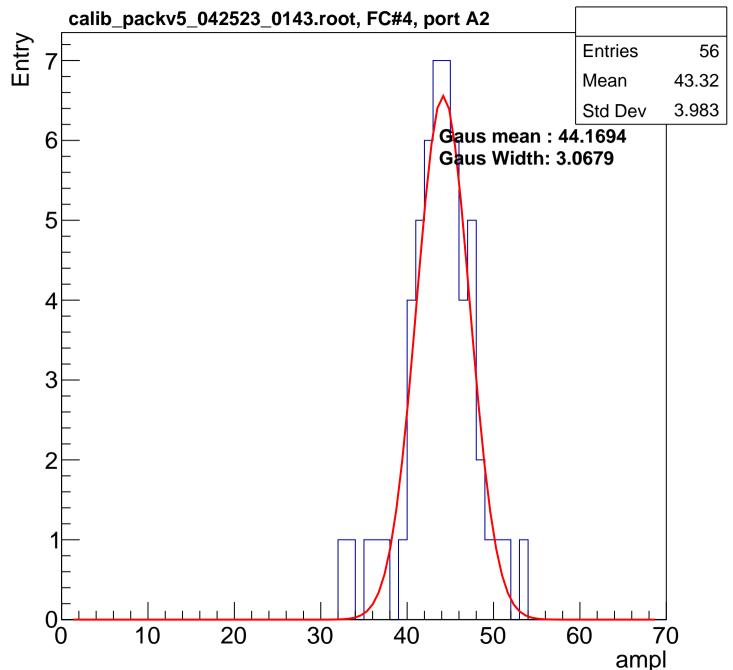


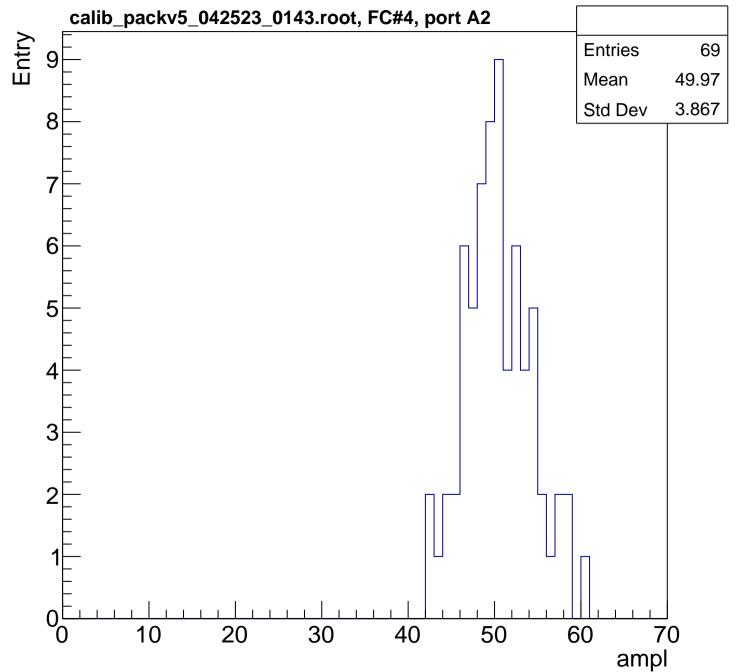


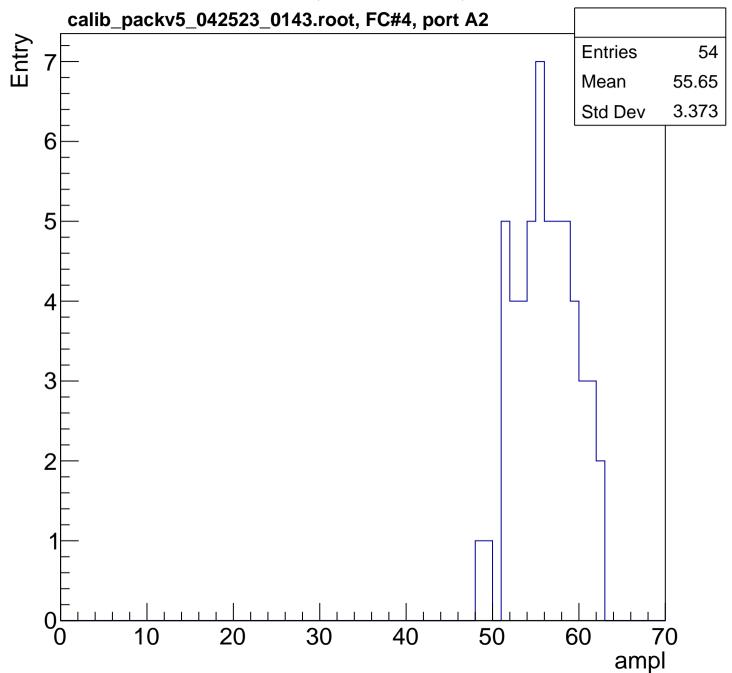


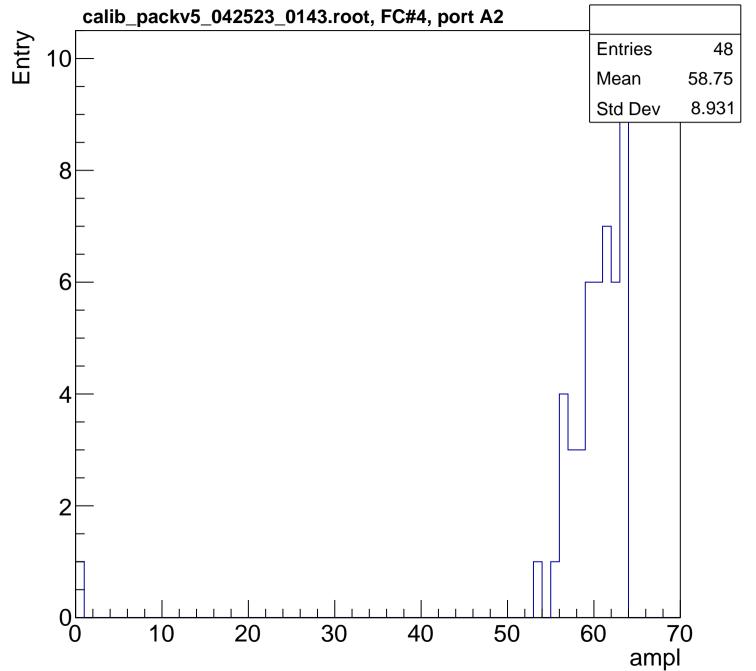


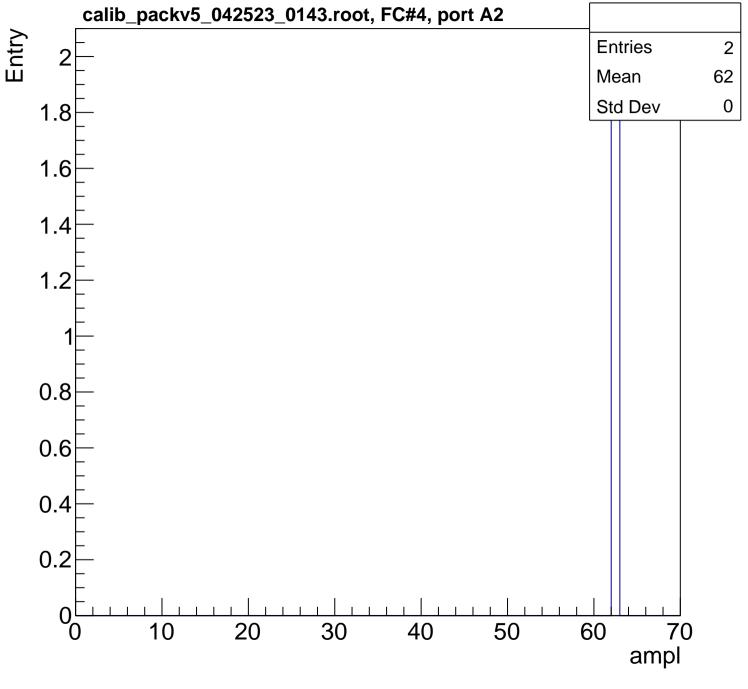


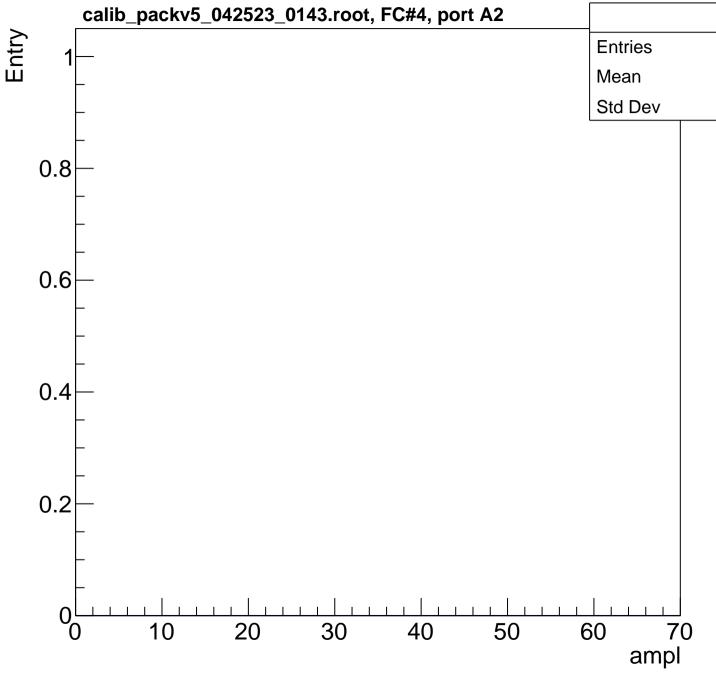


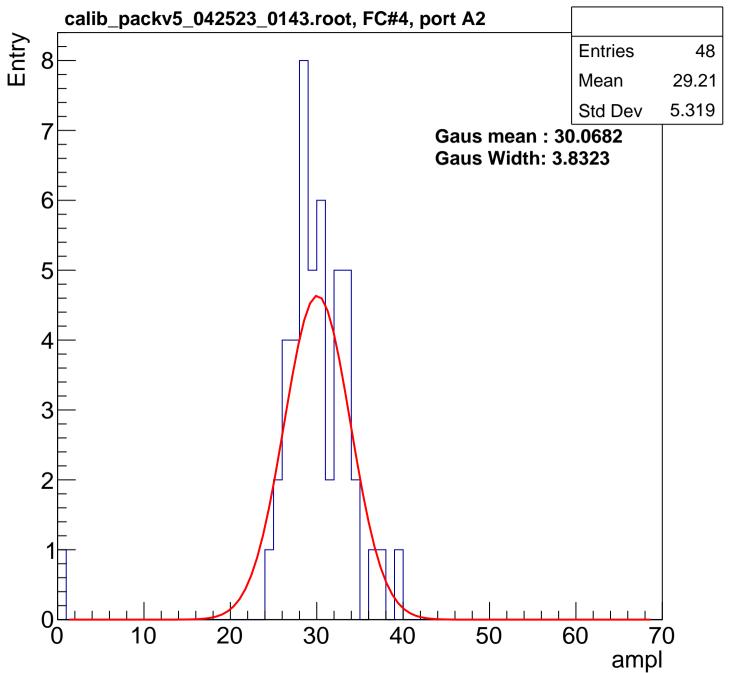


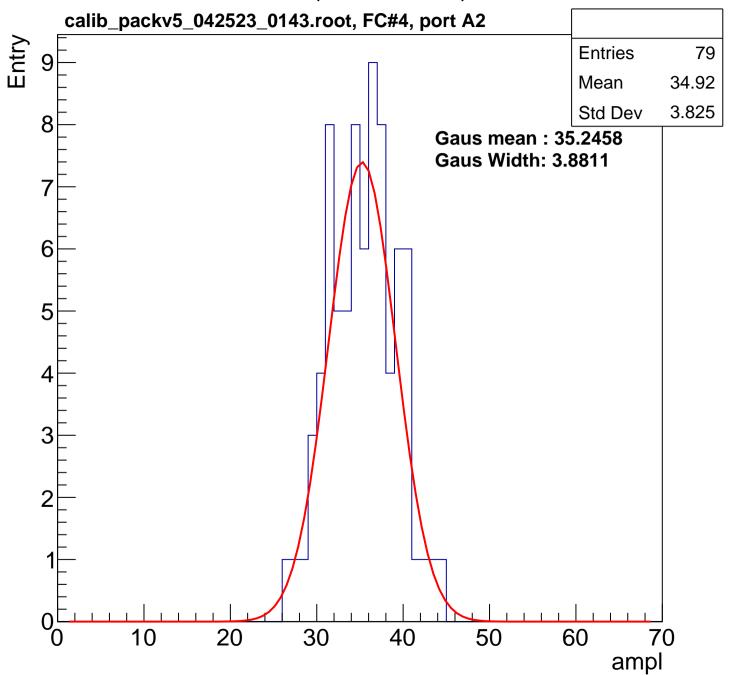


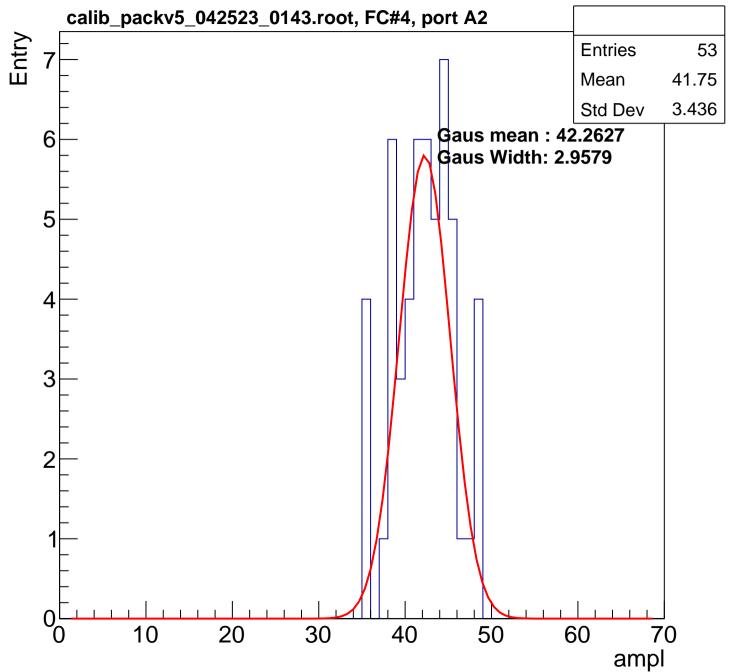


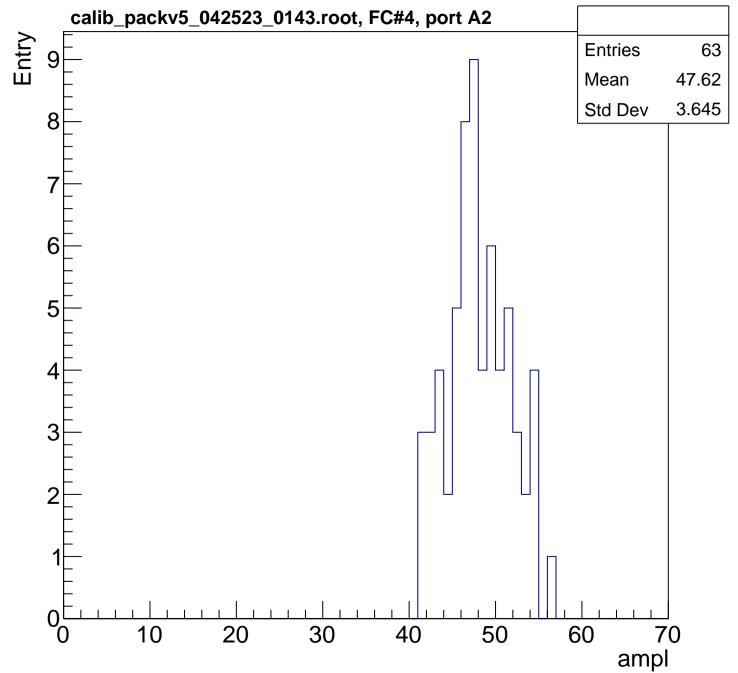


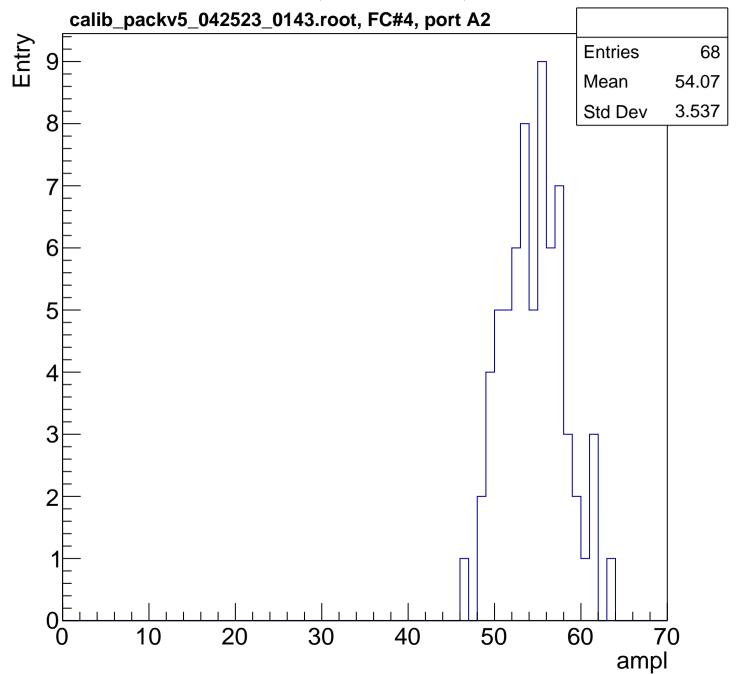


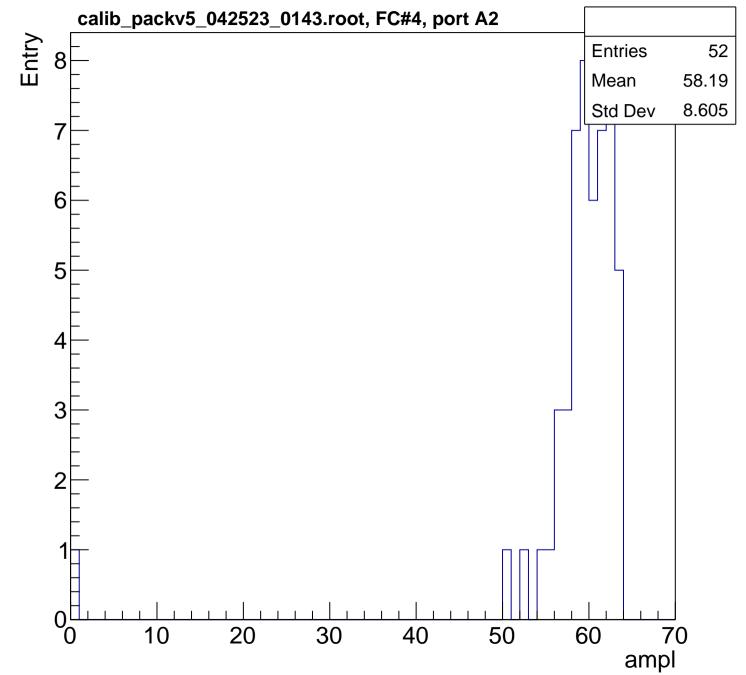


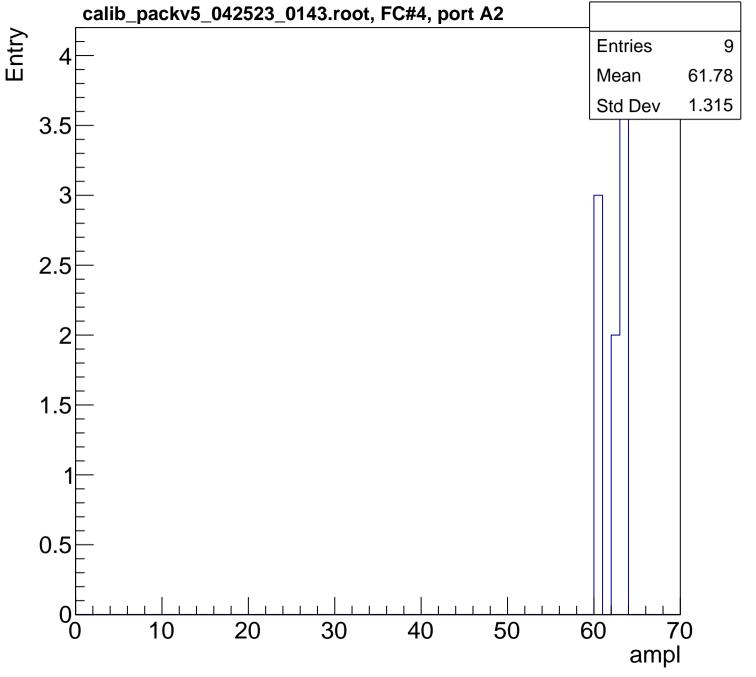




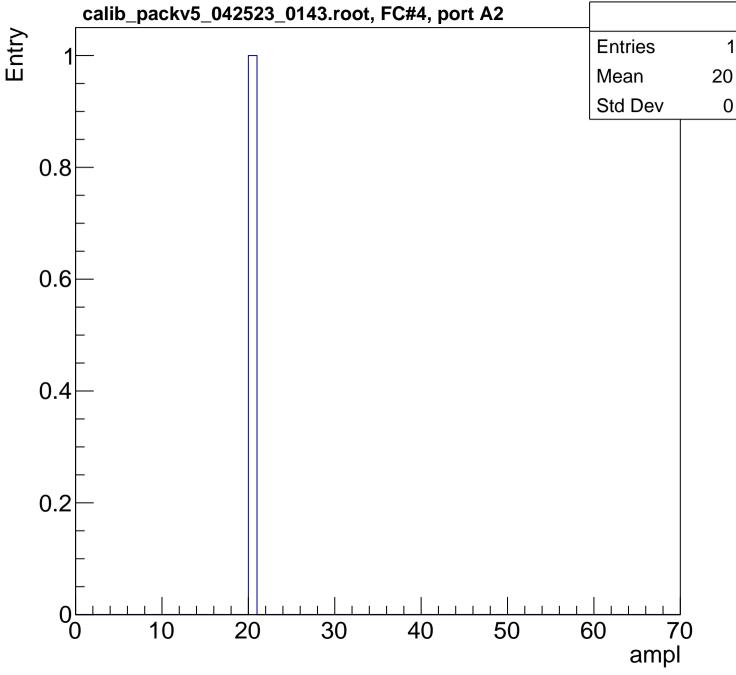


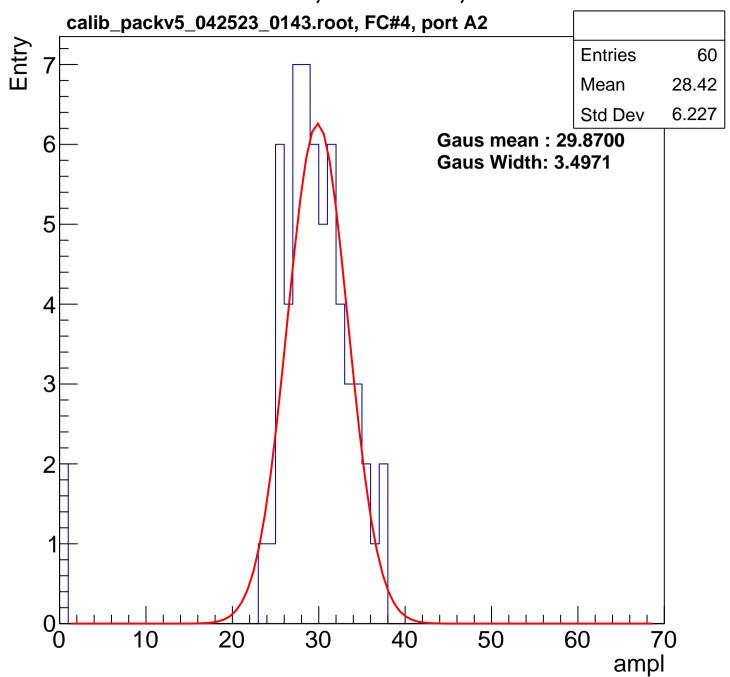


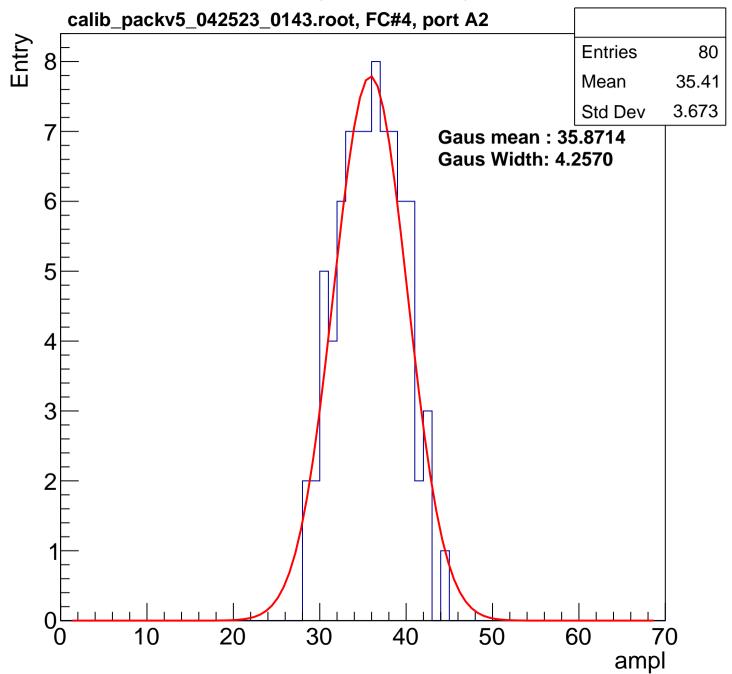


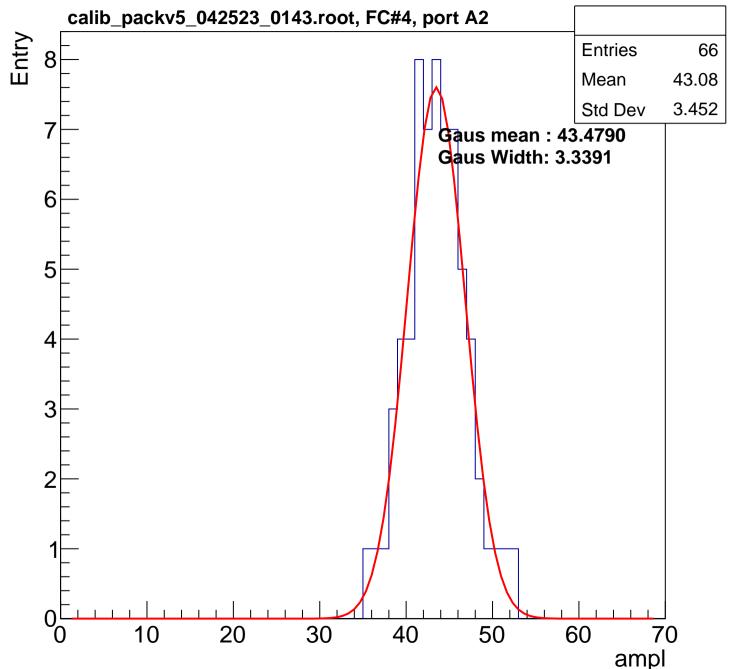


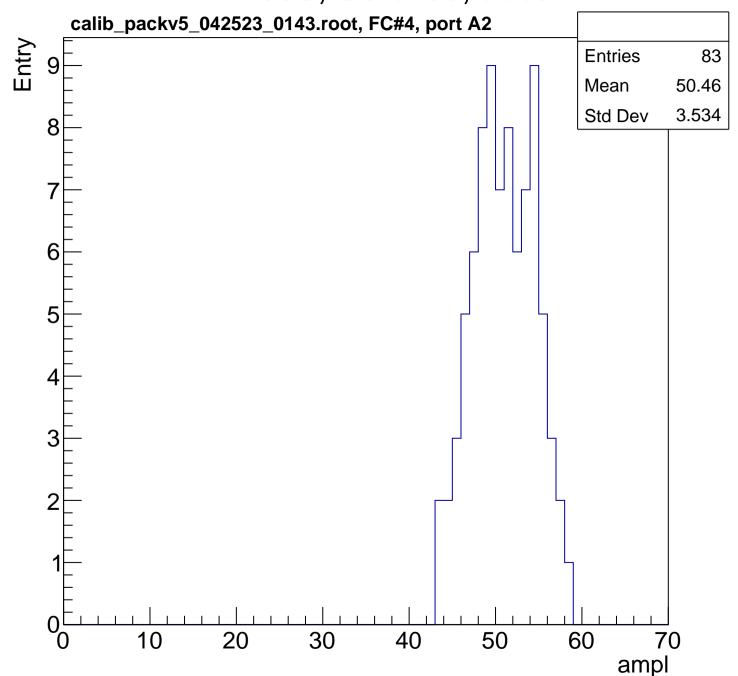
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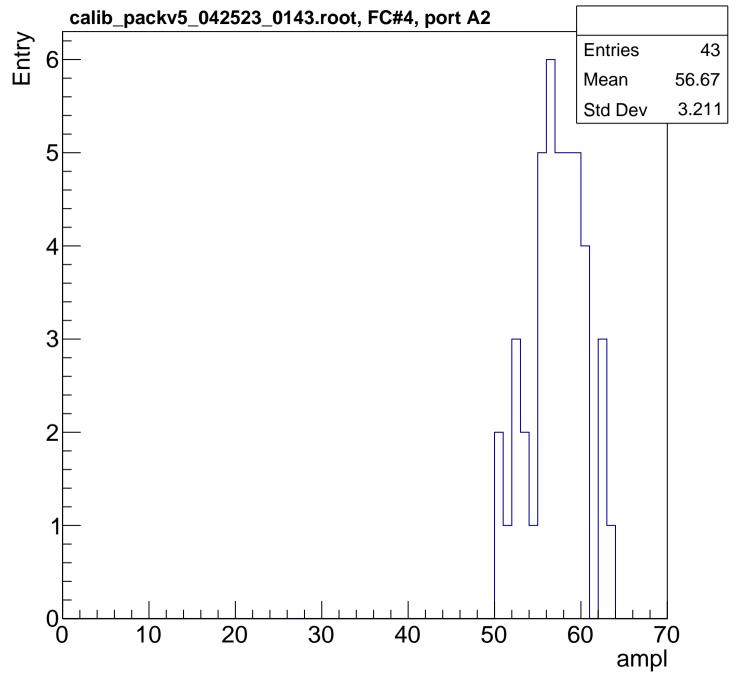


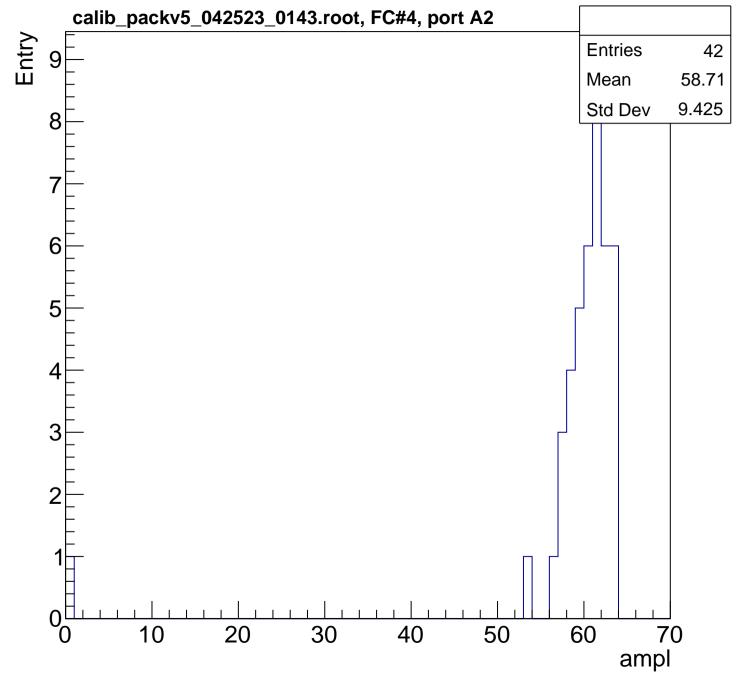


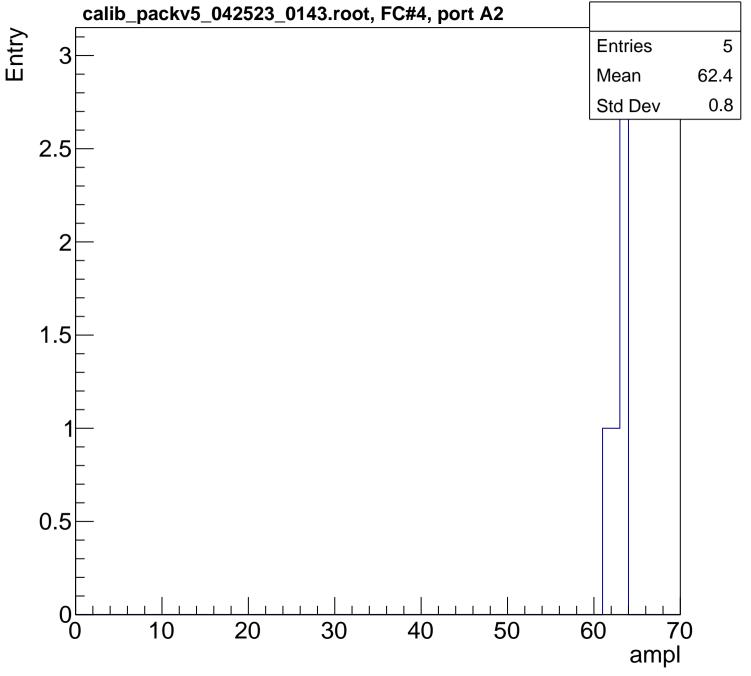


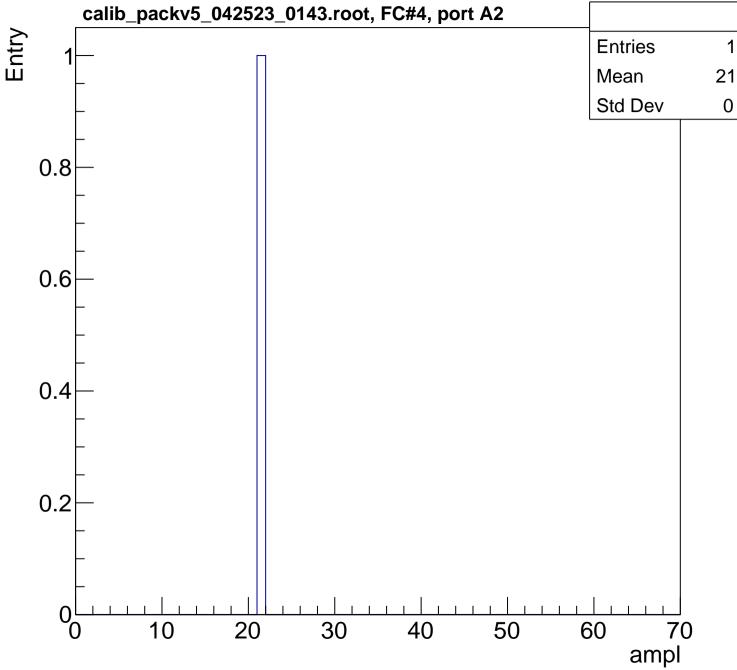


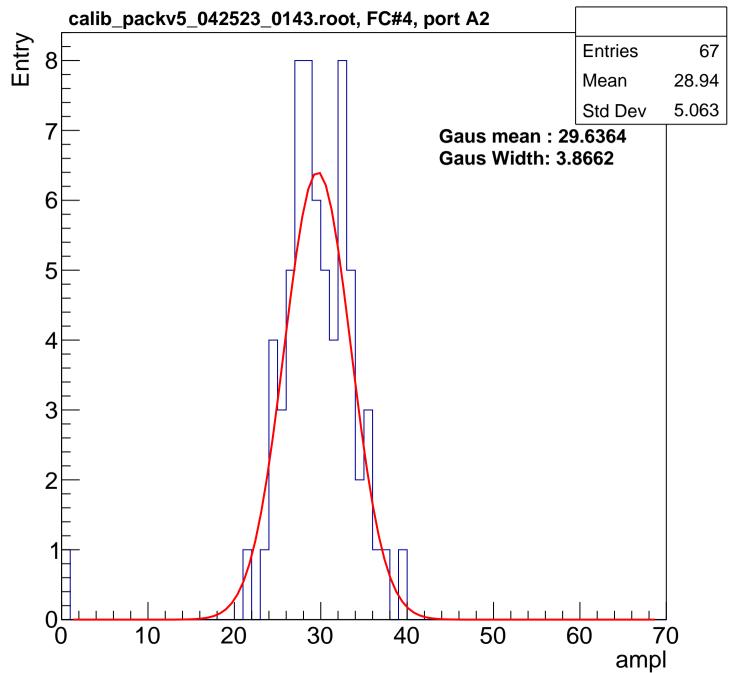


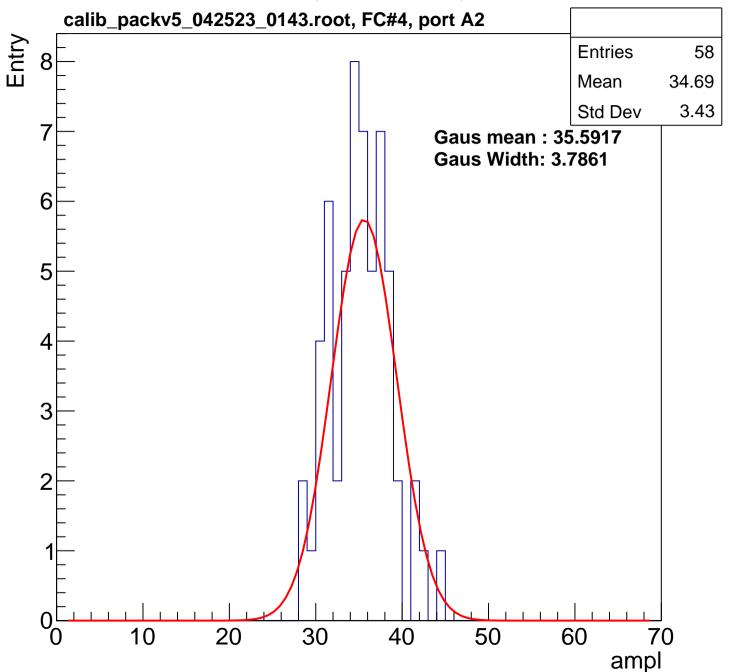


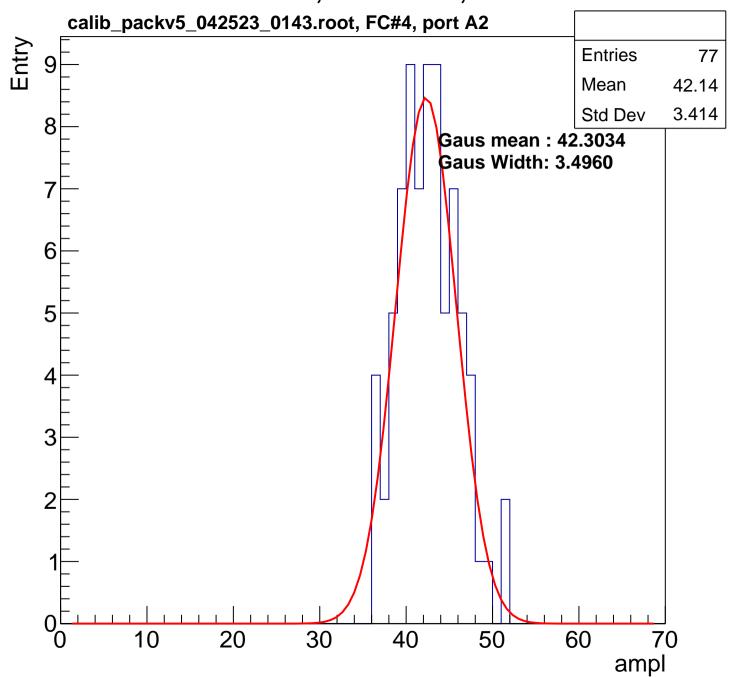


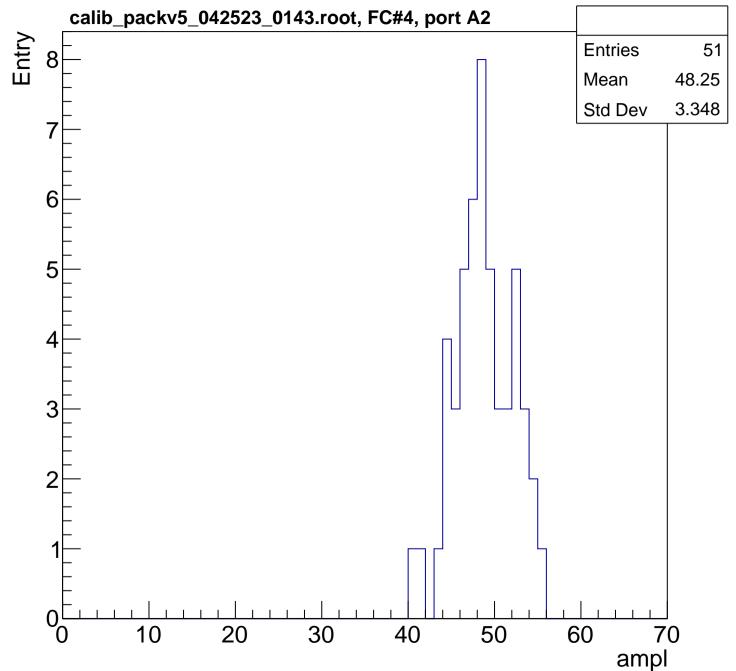


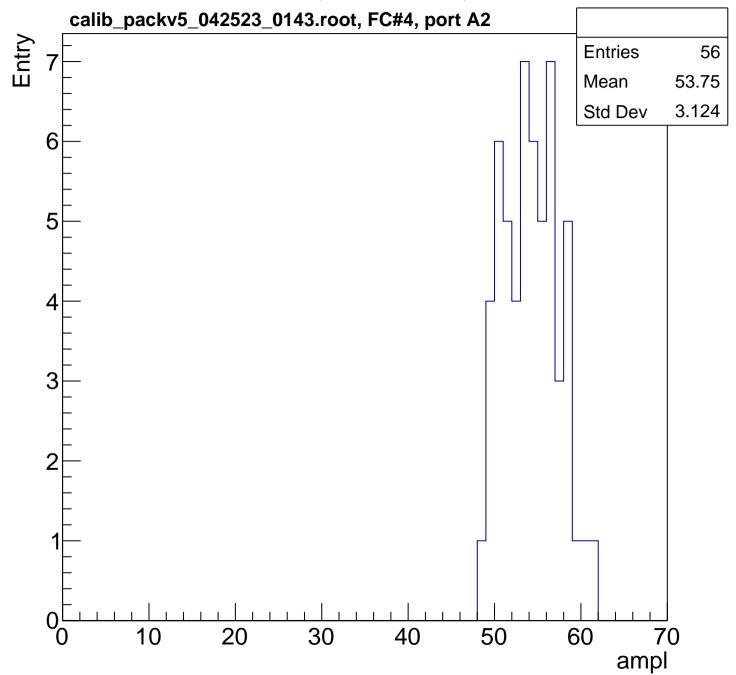


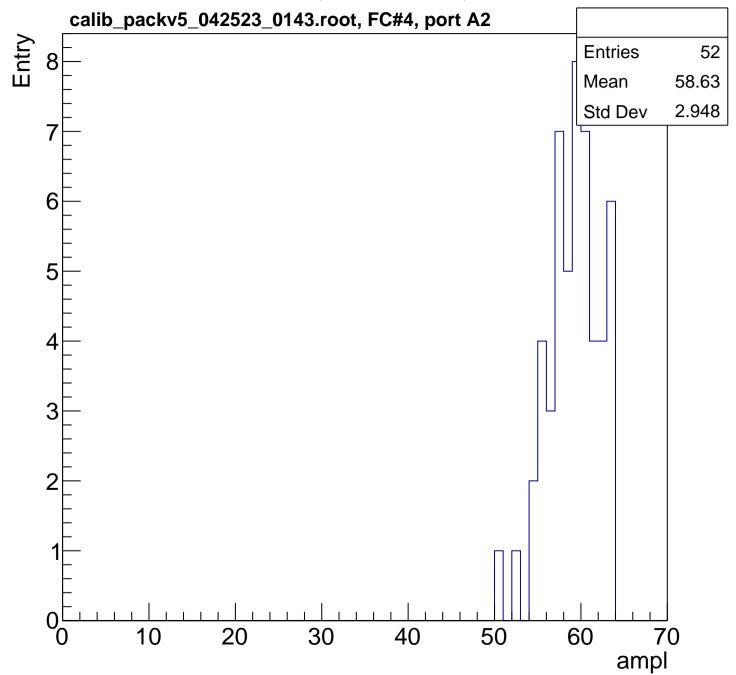


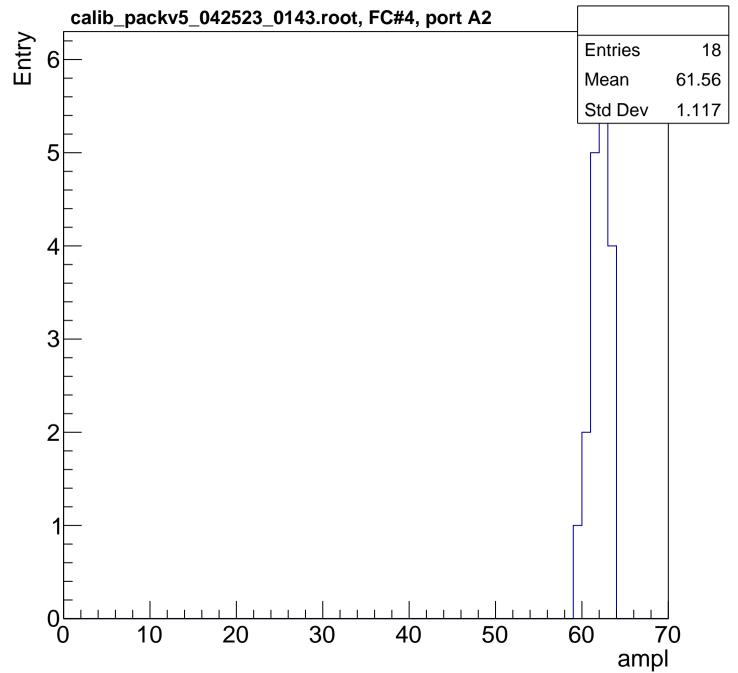




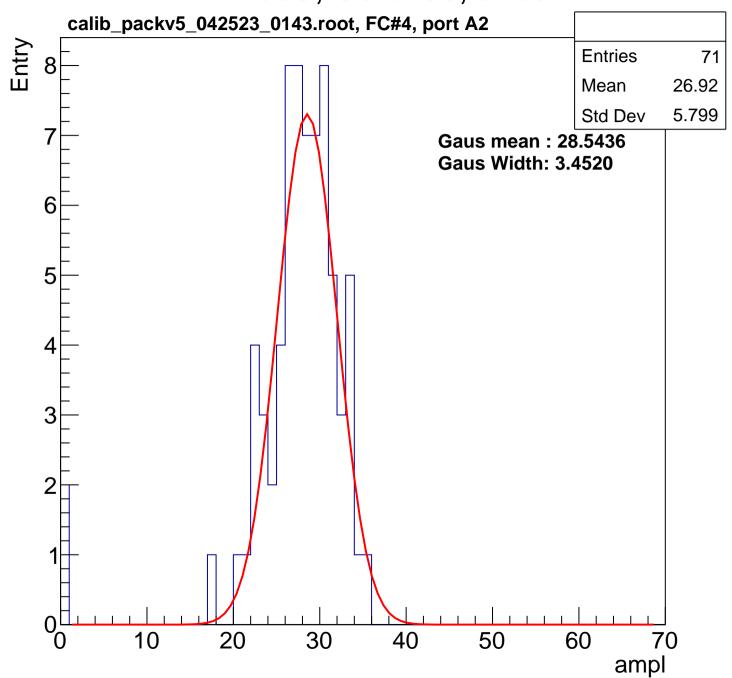


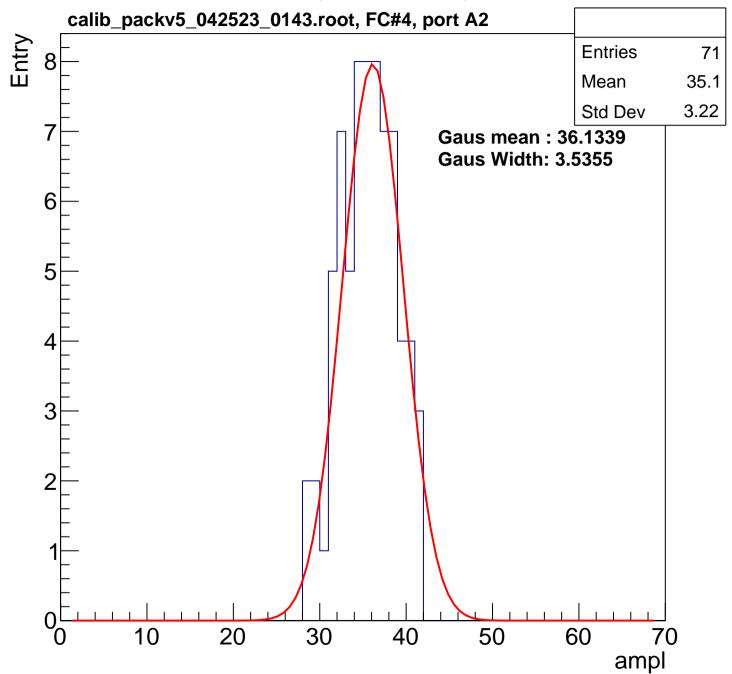


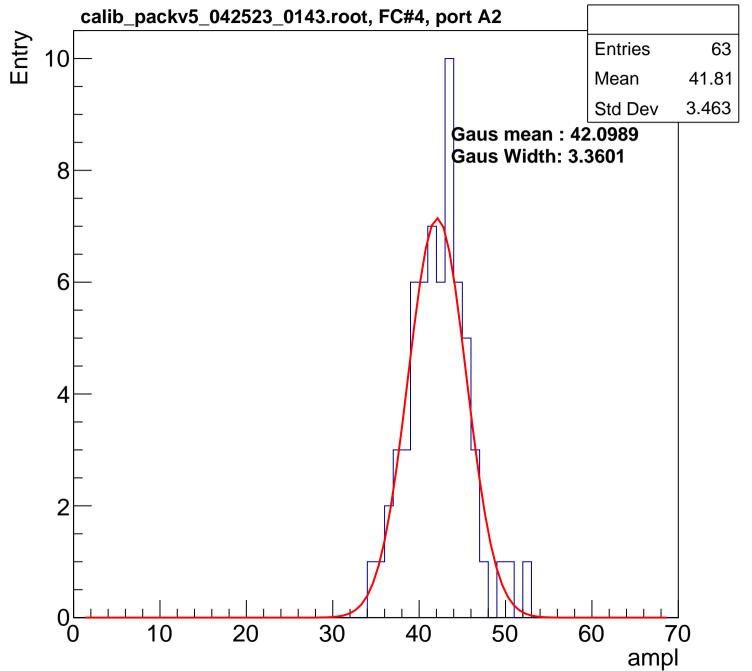


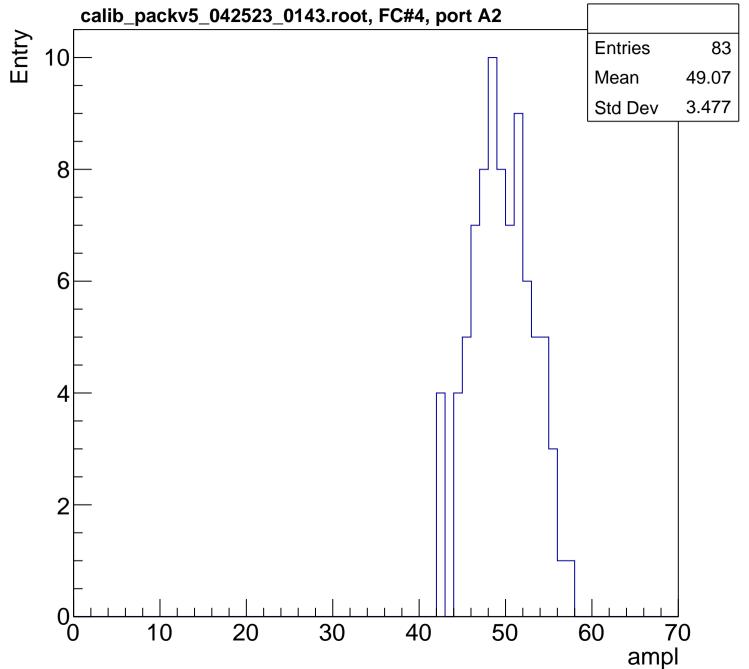


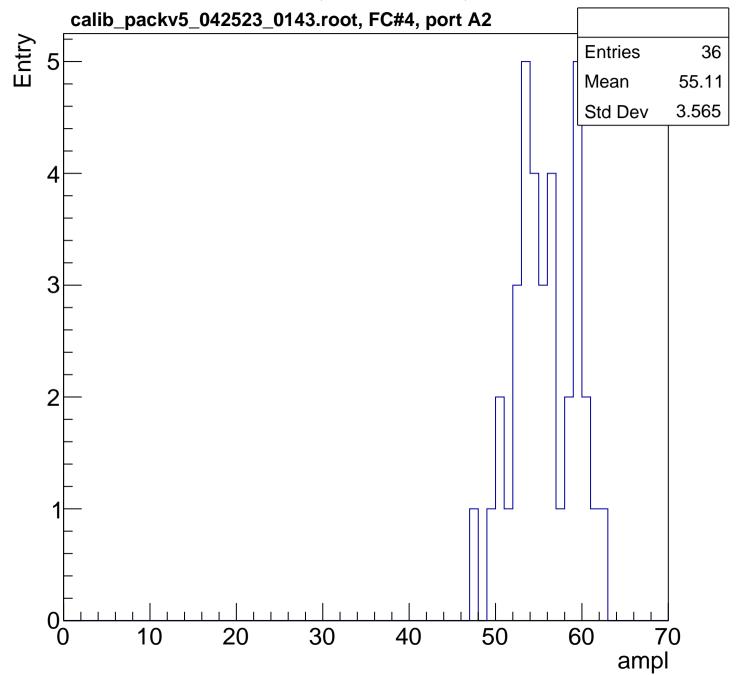
B1L100S, U3-ch84, adc7 calib_packv5_042523_0143.root, FC#4, port A2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

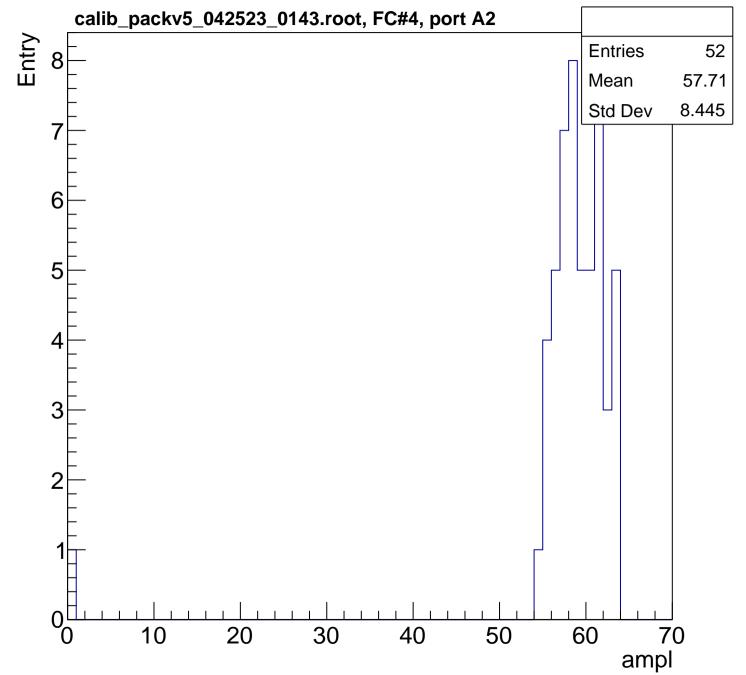


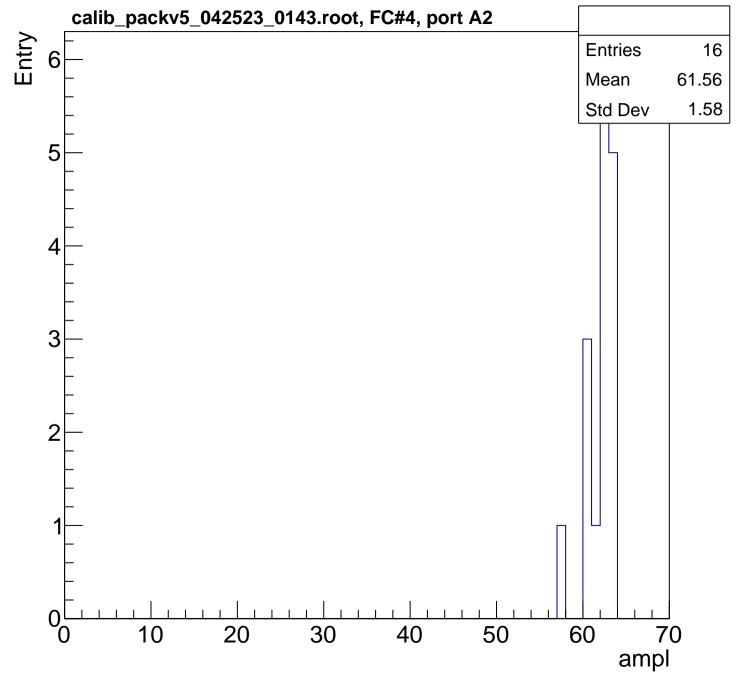




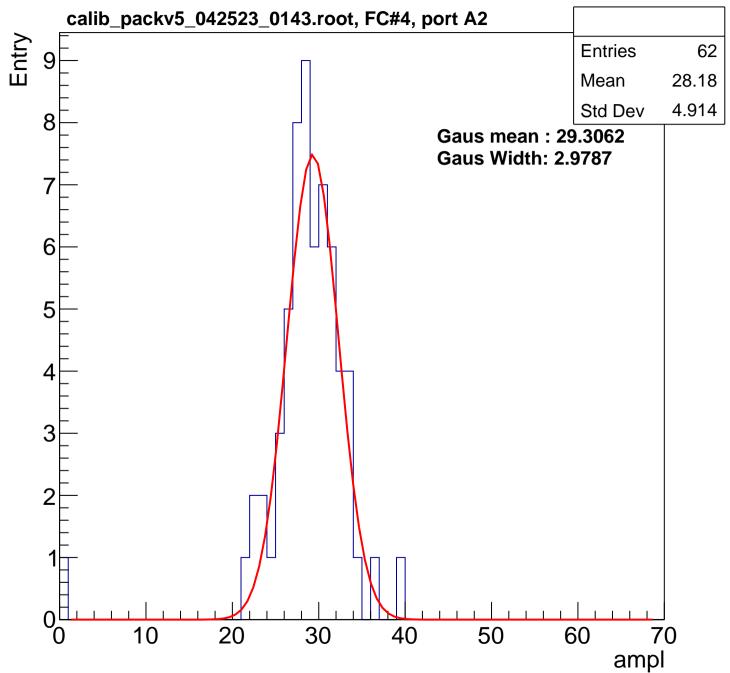


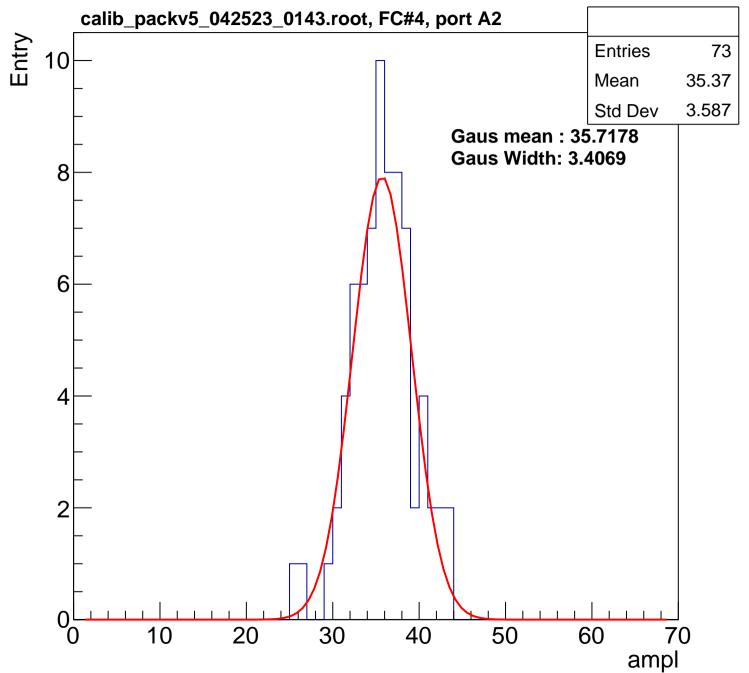


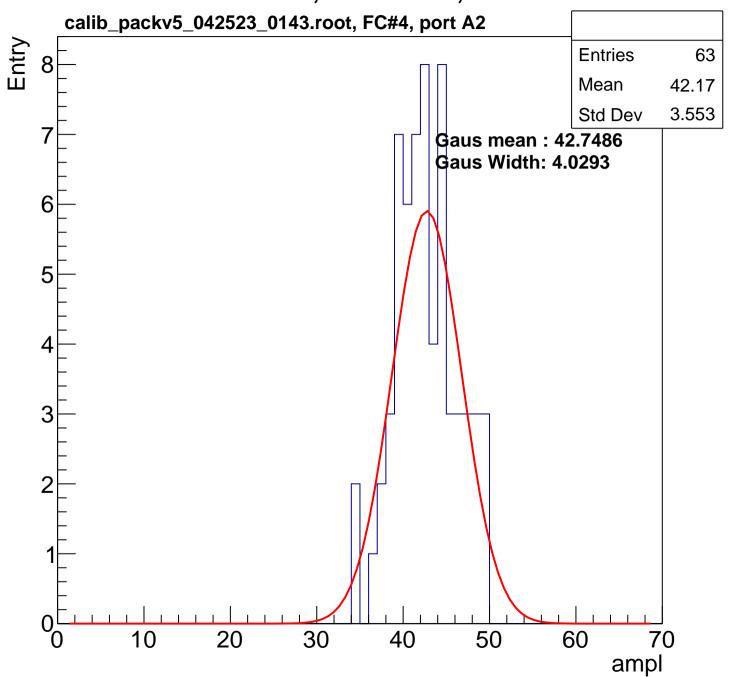


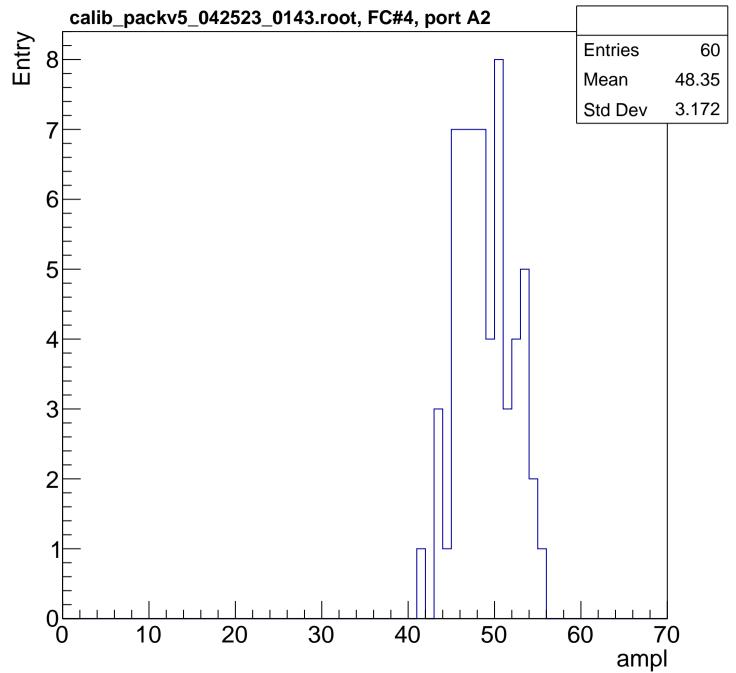


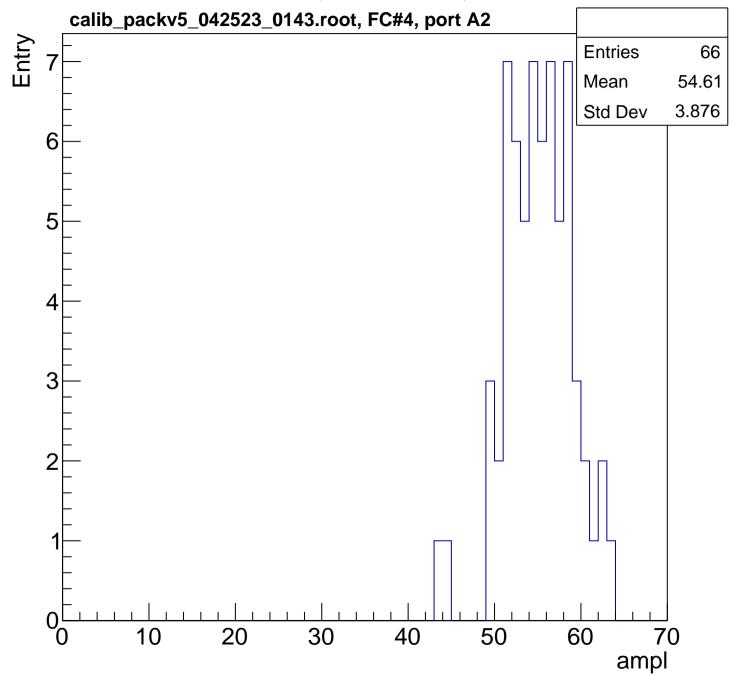
B1L100S, U3-ch85, adc7 calib_packv5_042523_0143.root, FC#4, port A2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

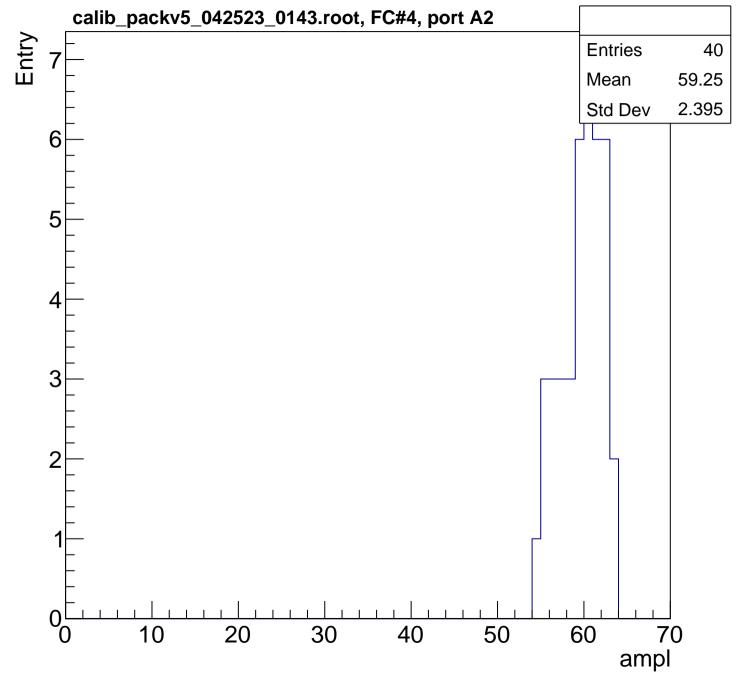


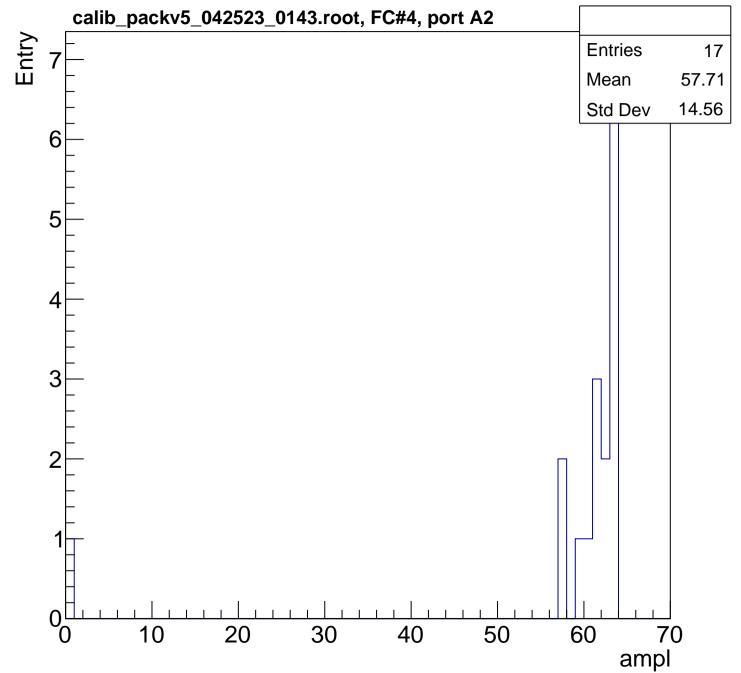




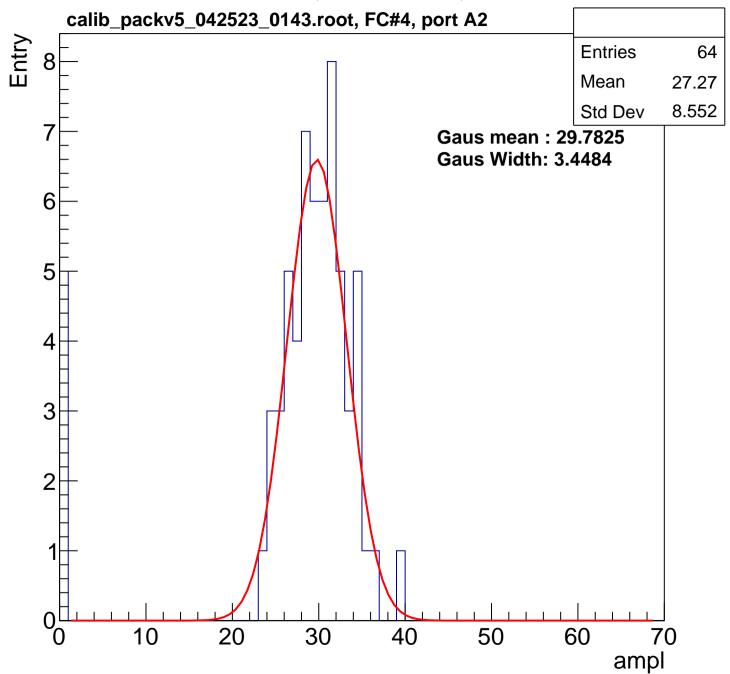


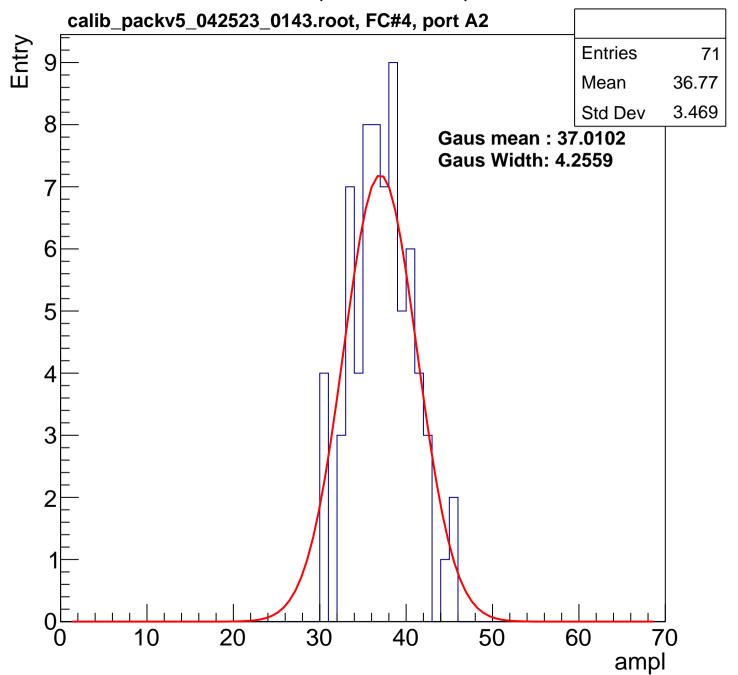


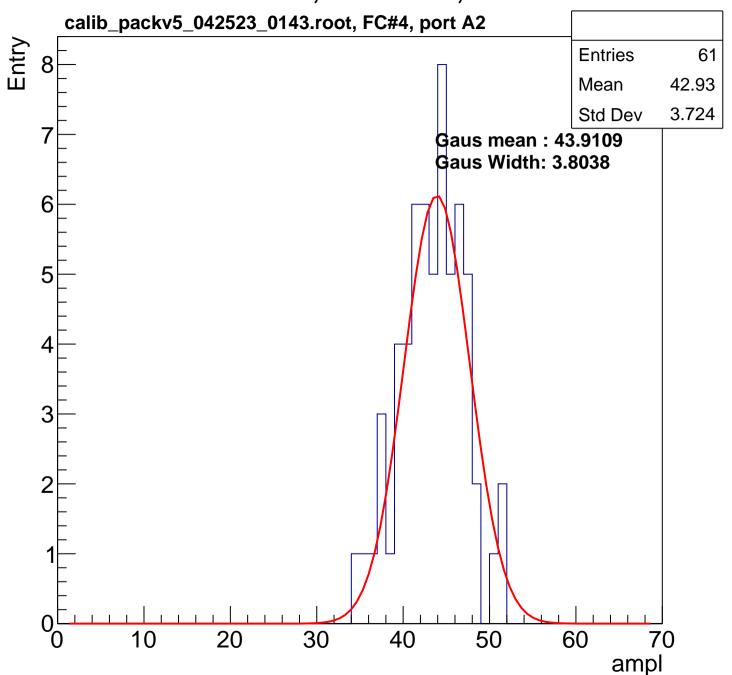


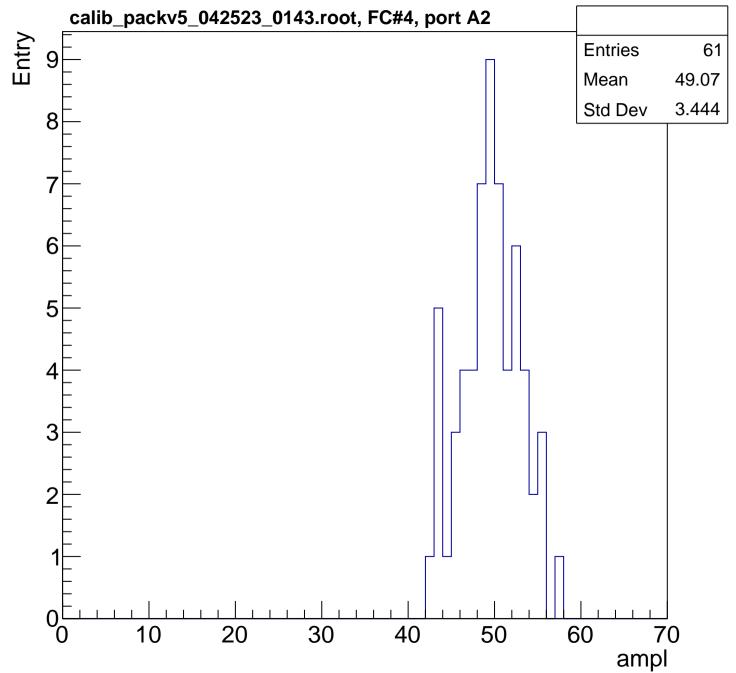


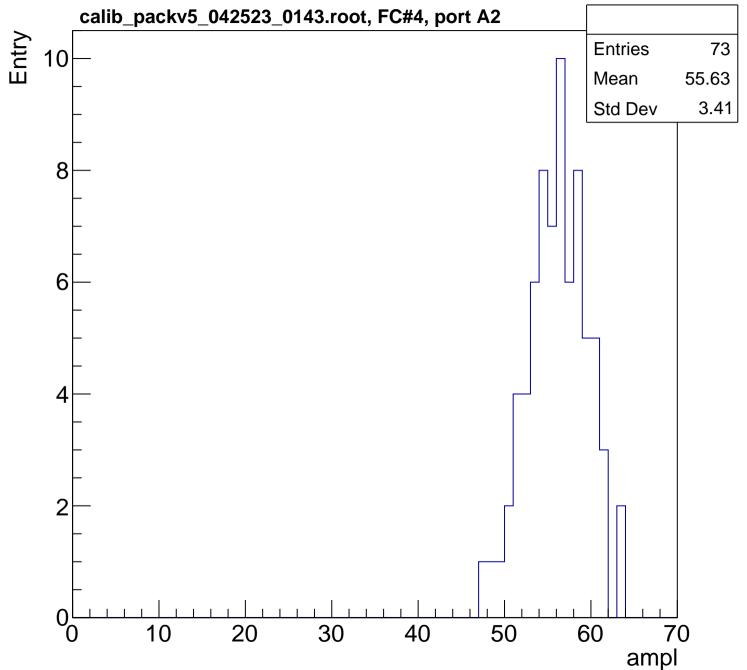
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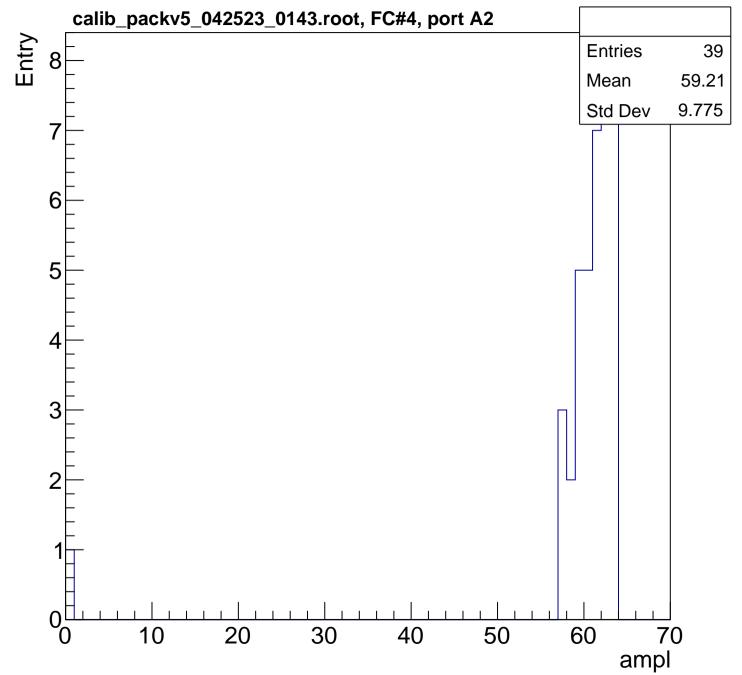


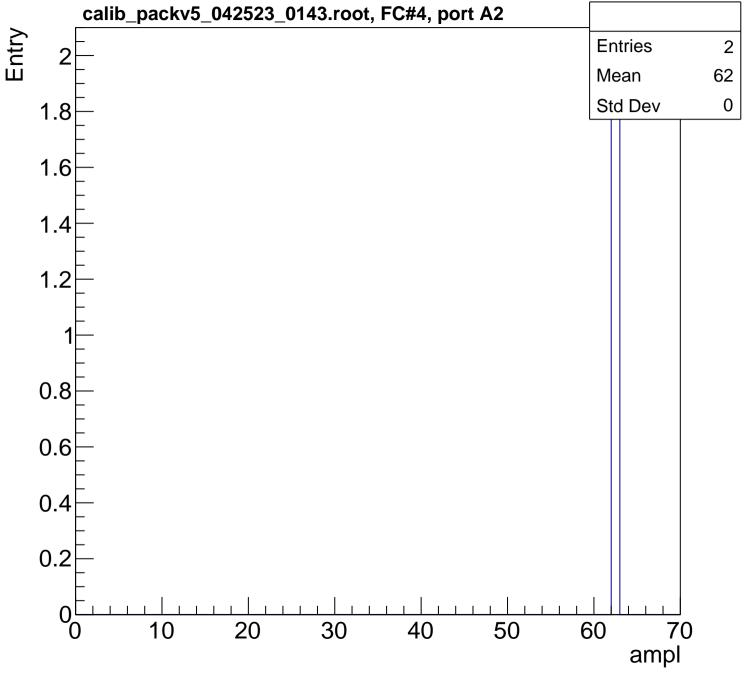




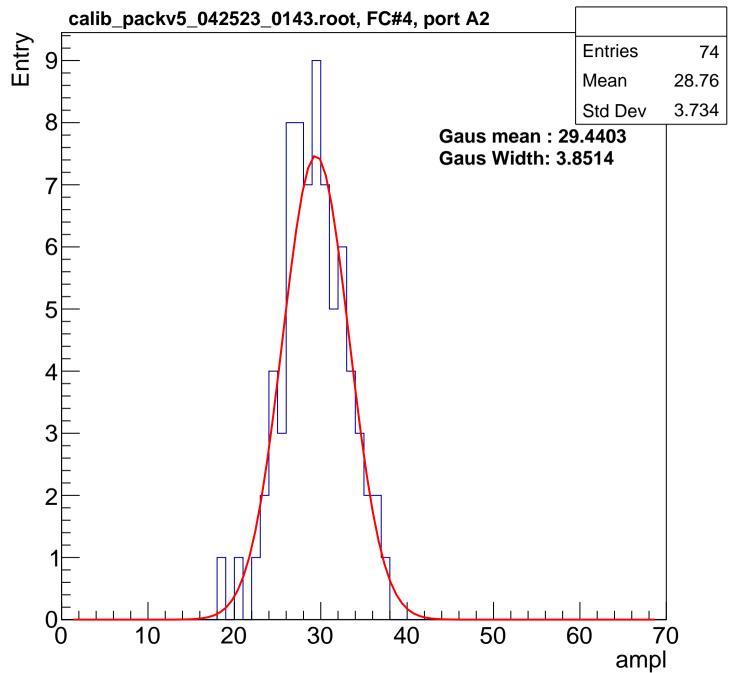


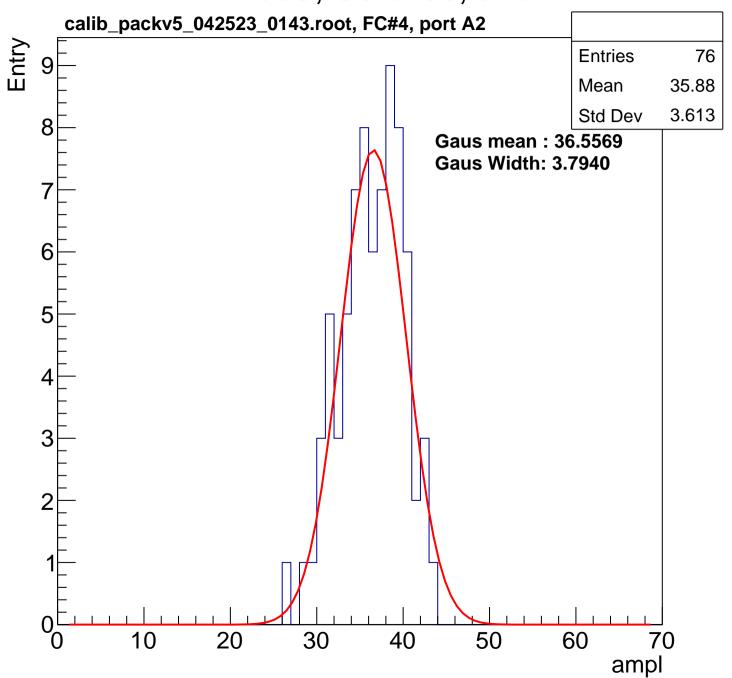


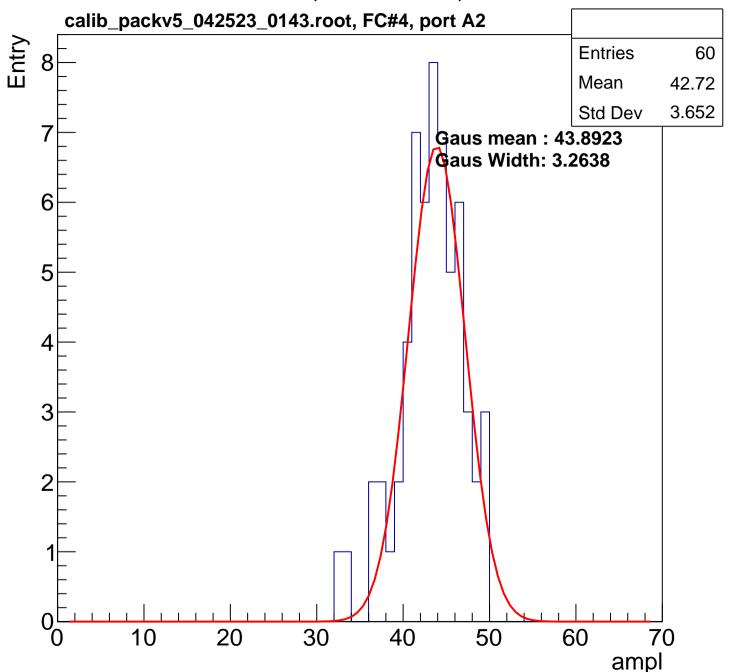


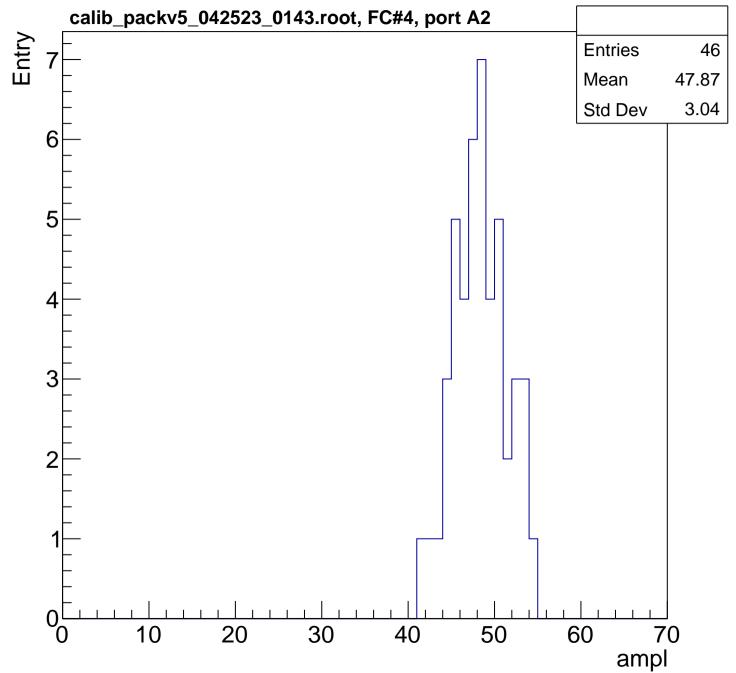


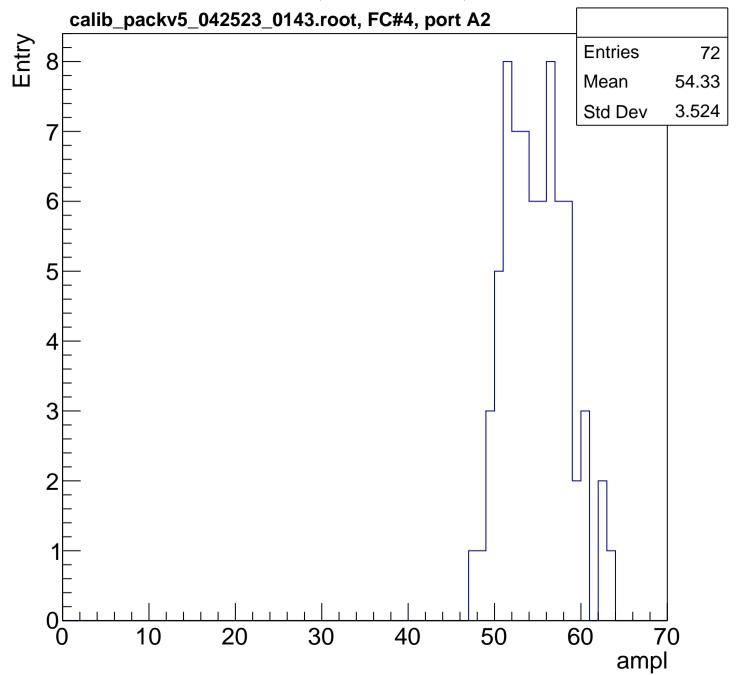


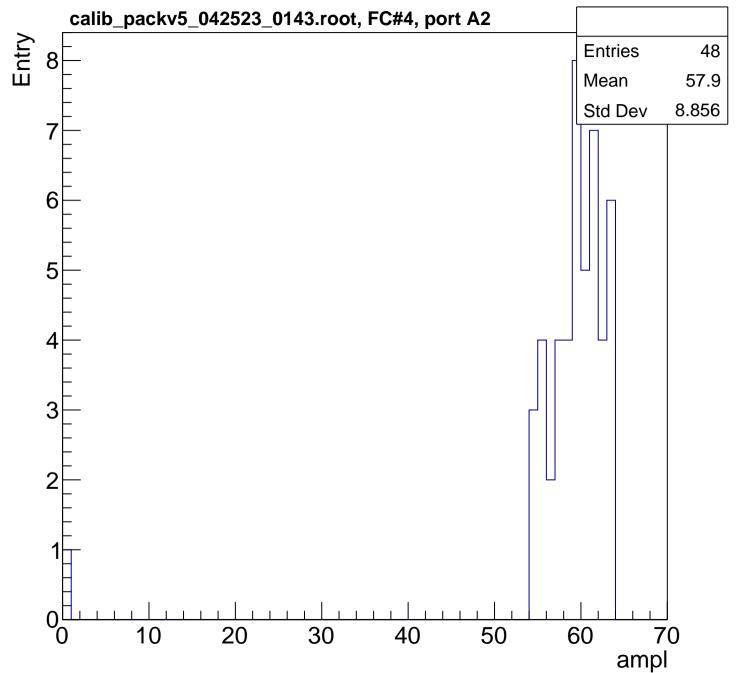


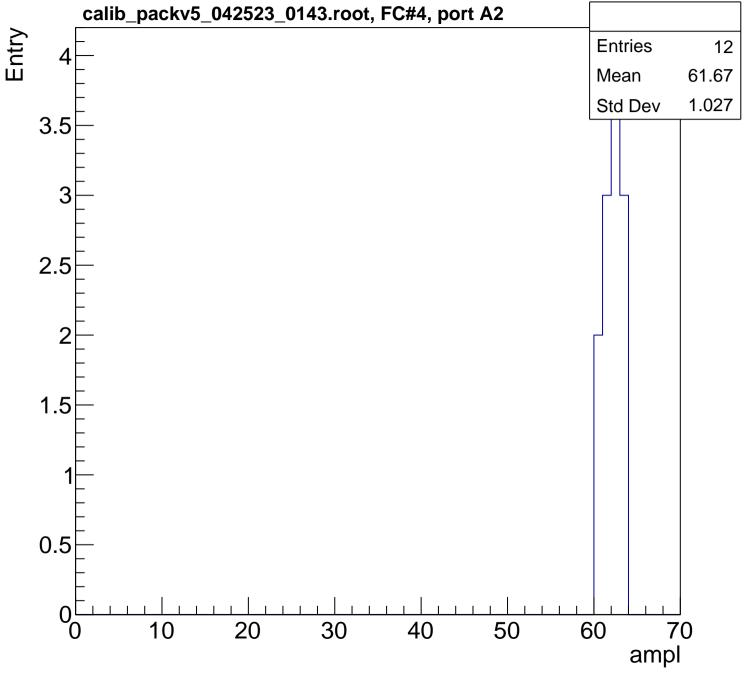




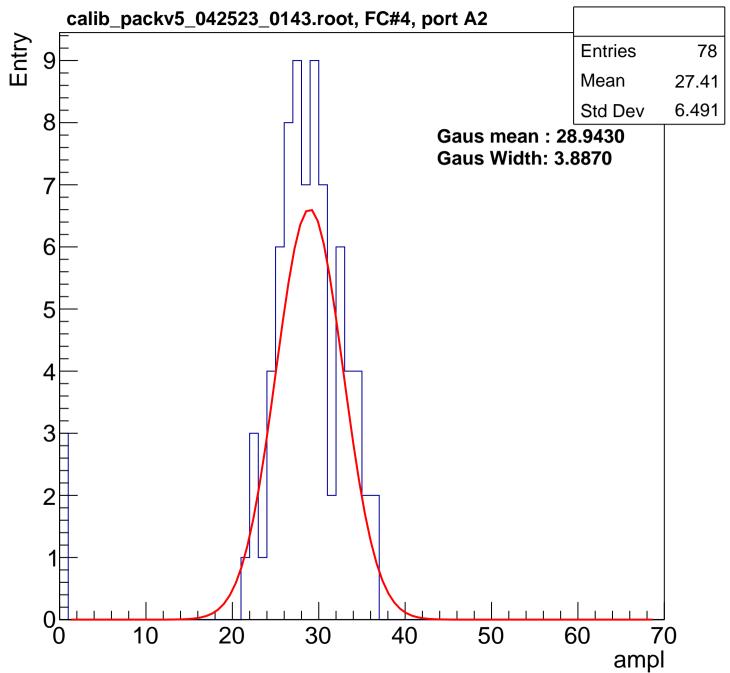


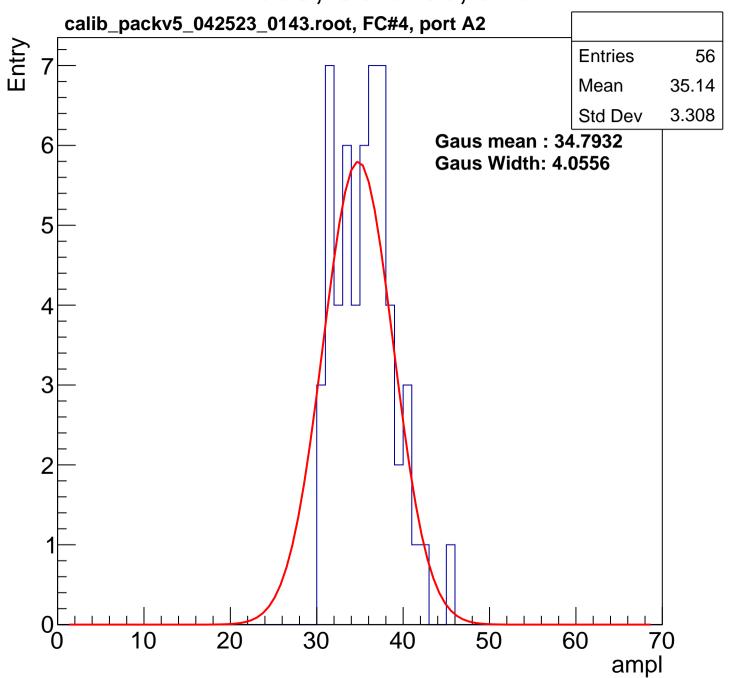


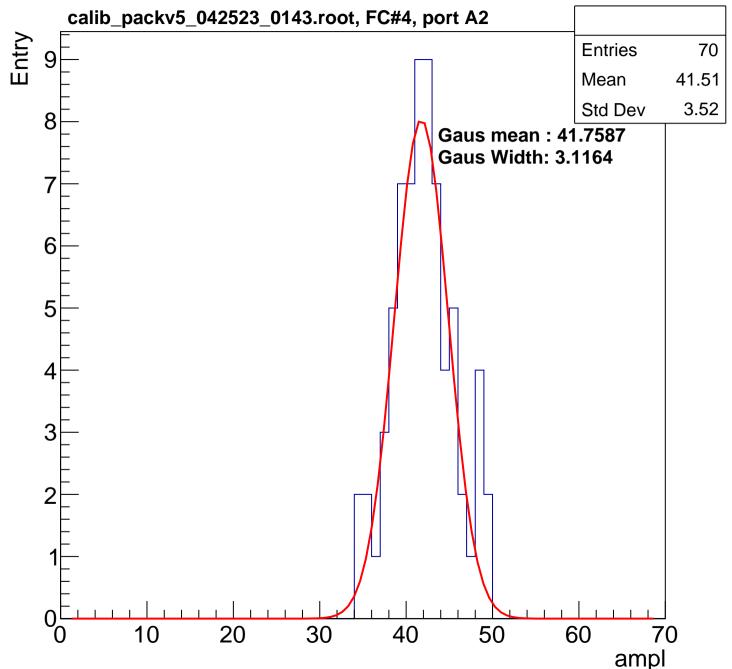


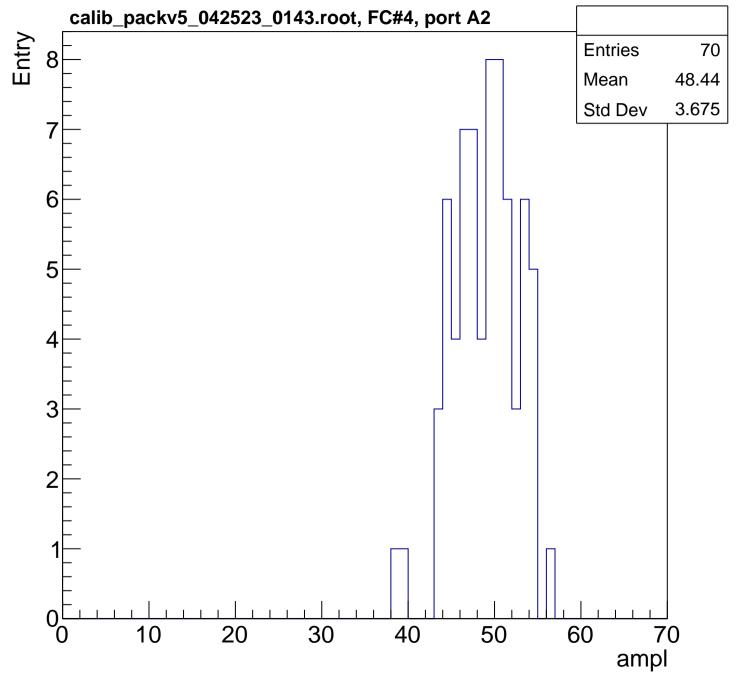


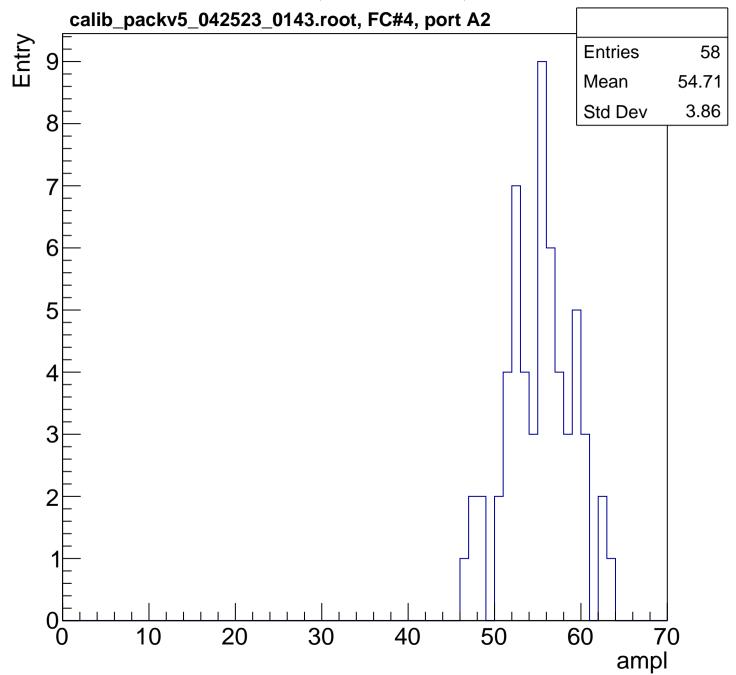


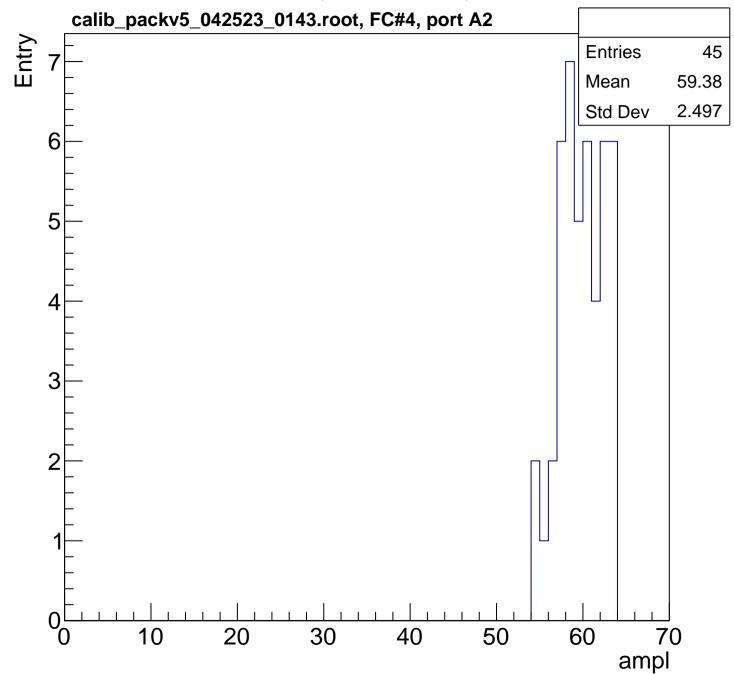


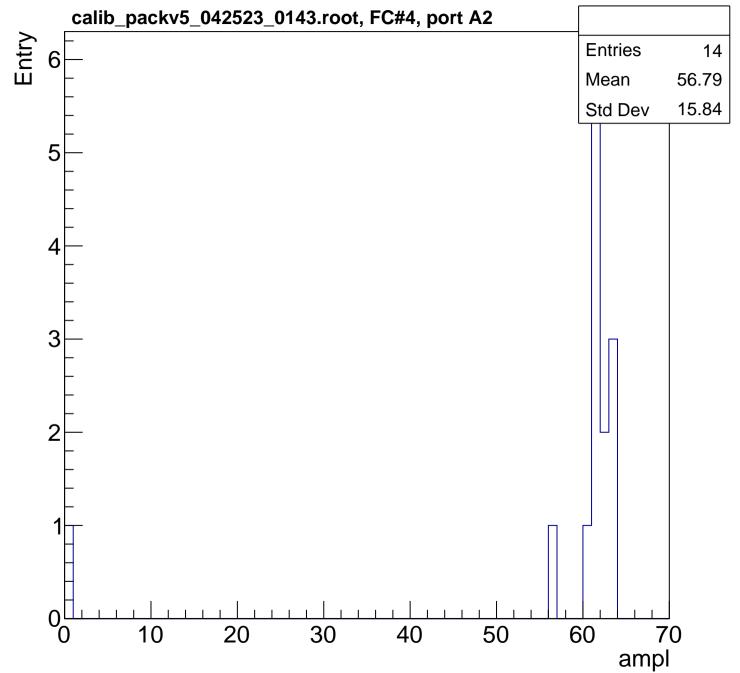






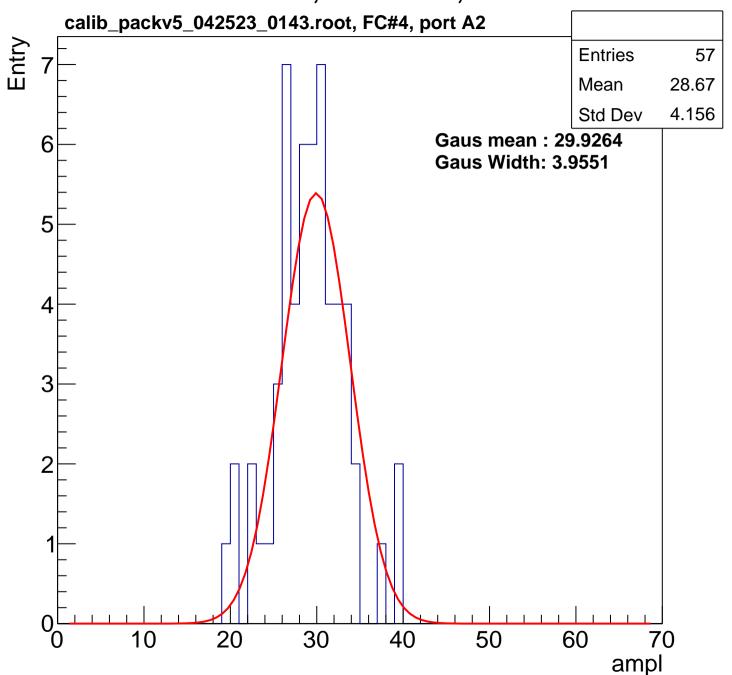


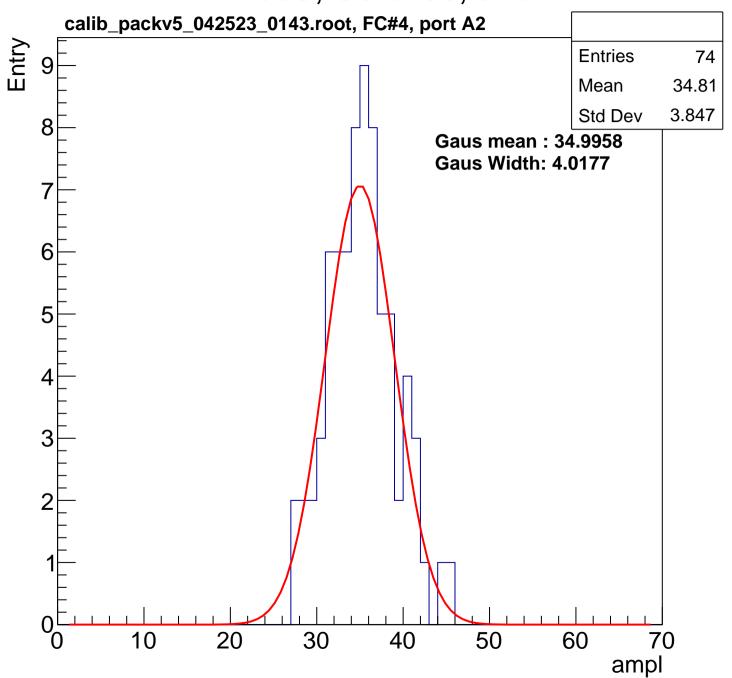


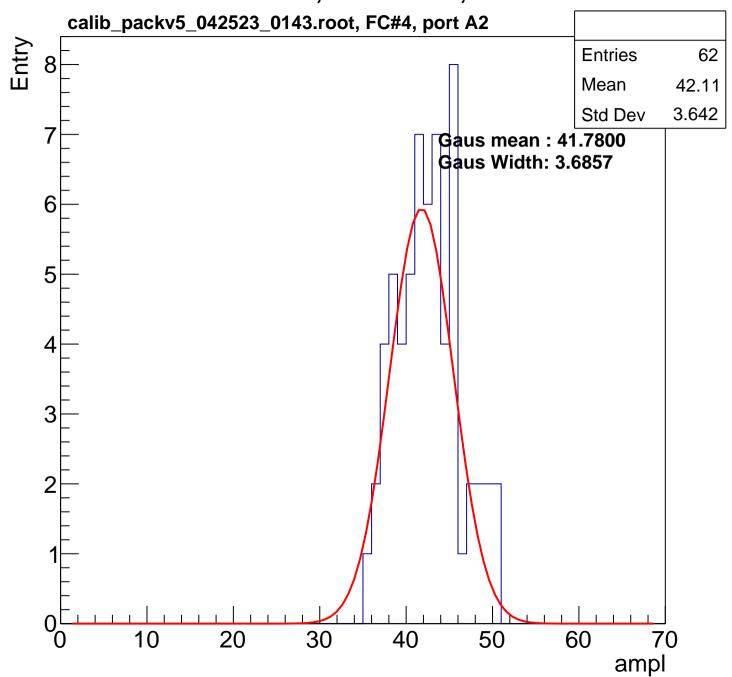


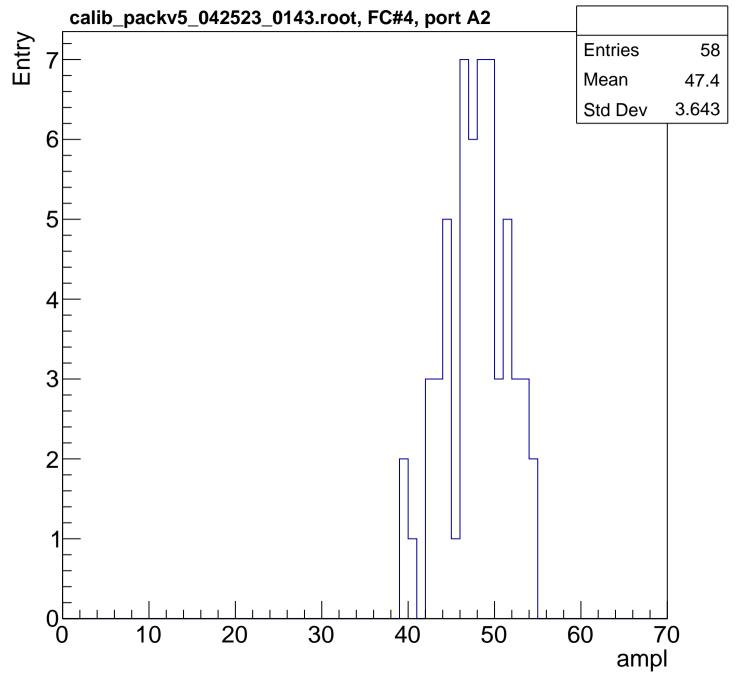
B1L100S, U3-ch89, adc7 calib_packv5_042523_0143.root, FC#4, port A2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70

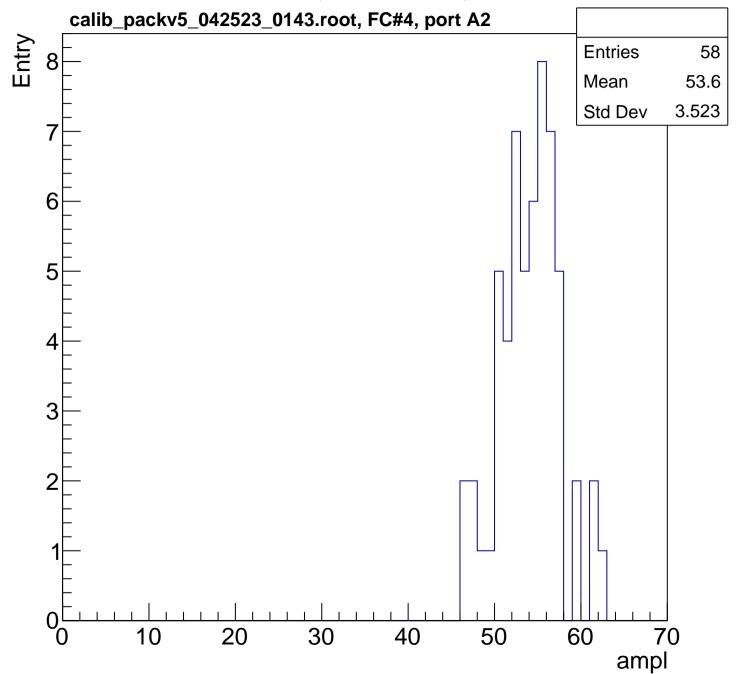
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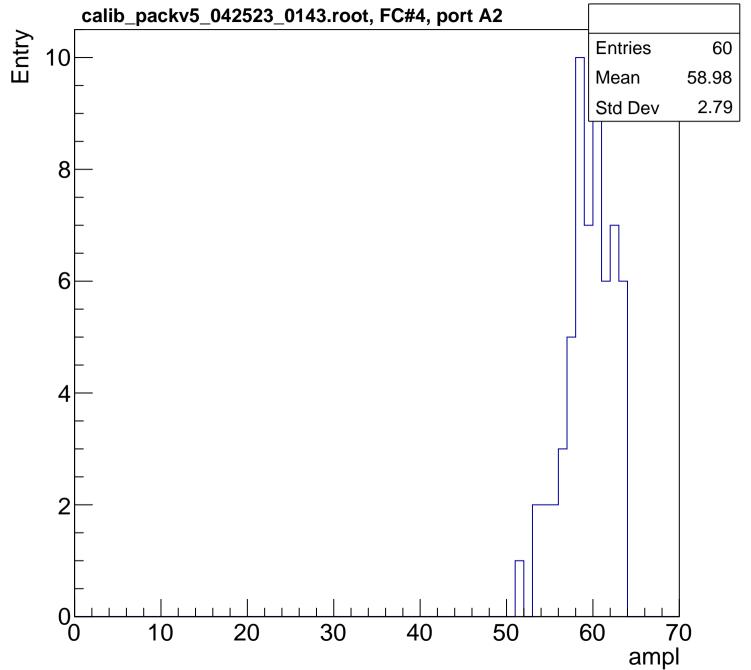


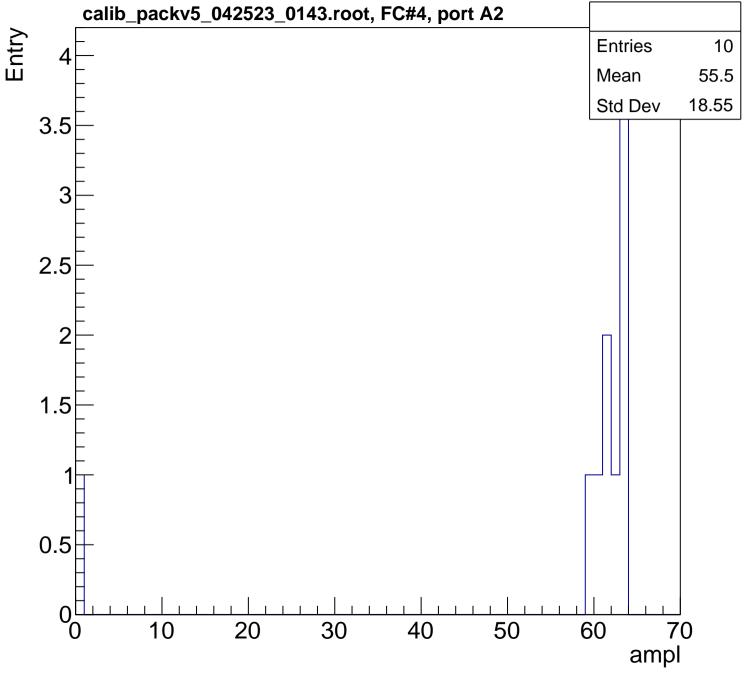


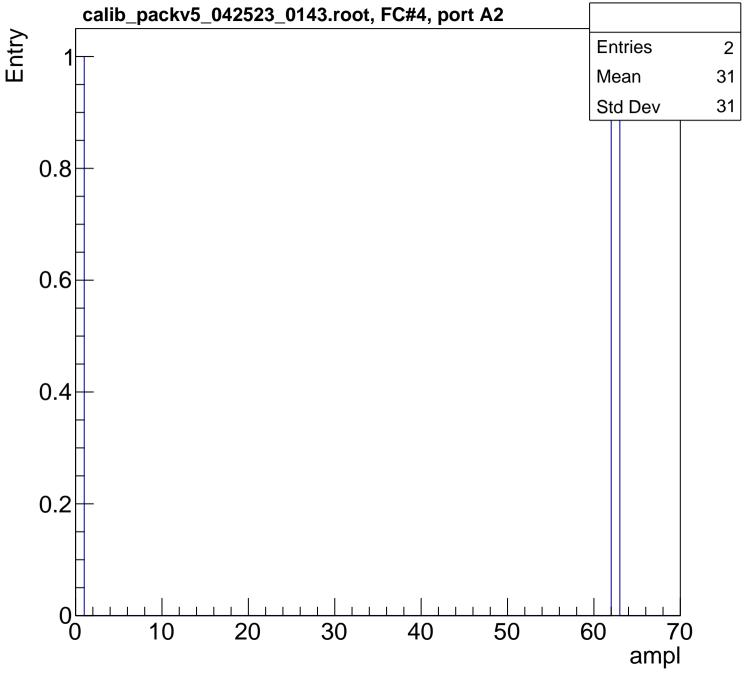


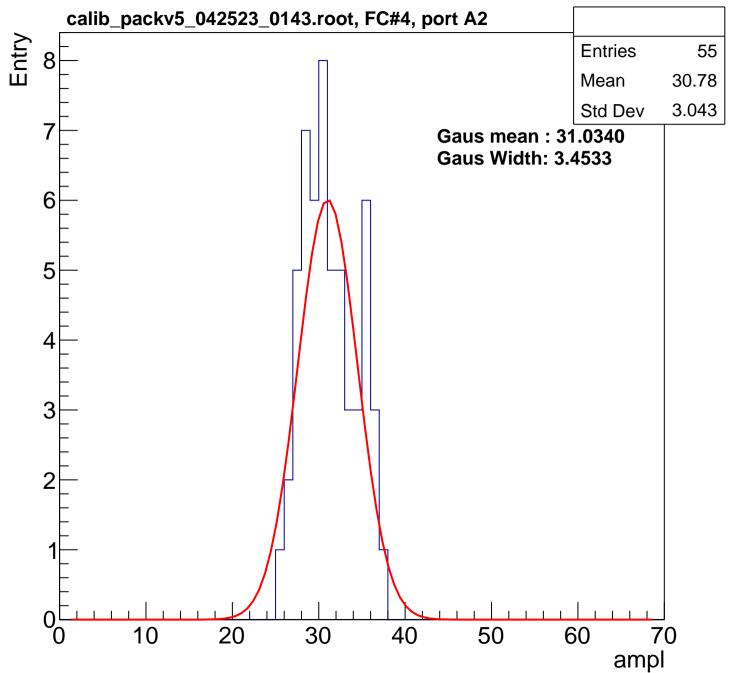


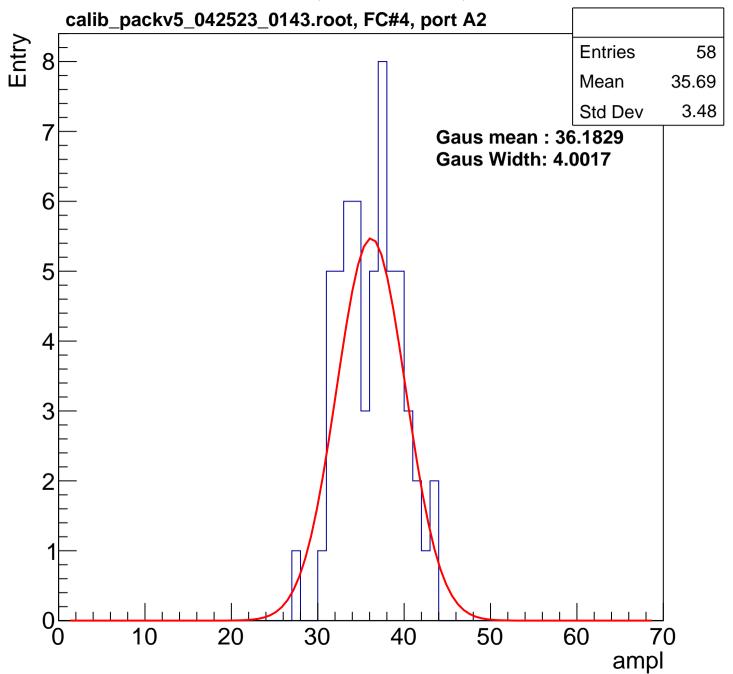


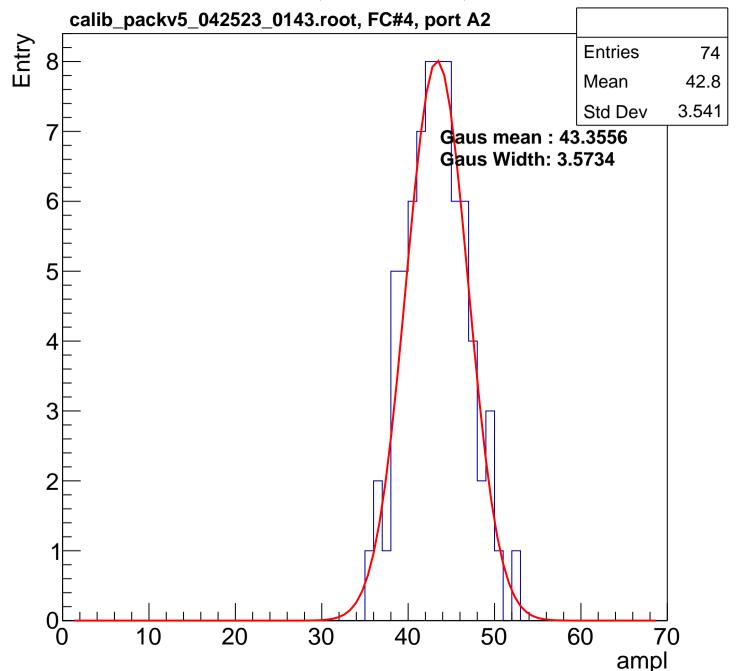


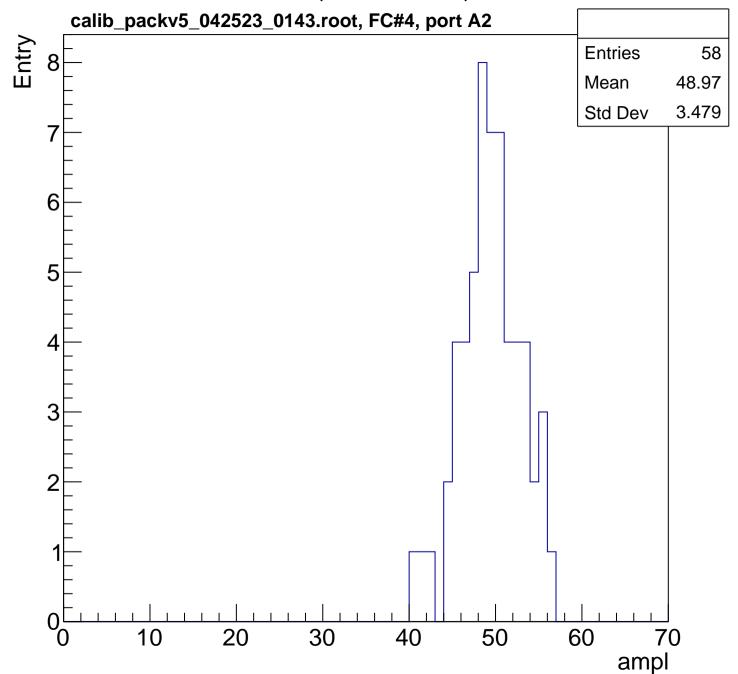


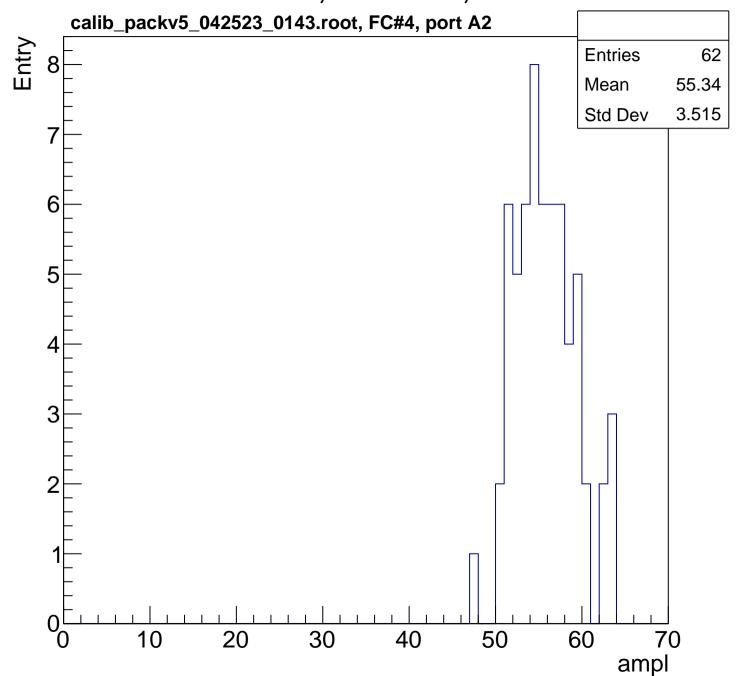


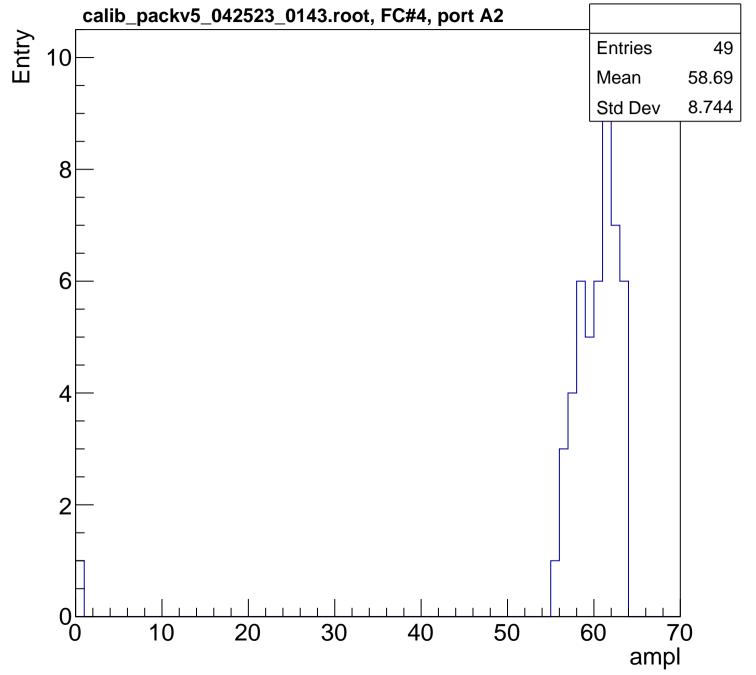


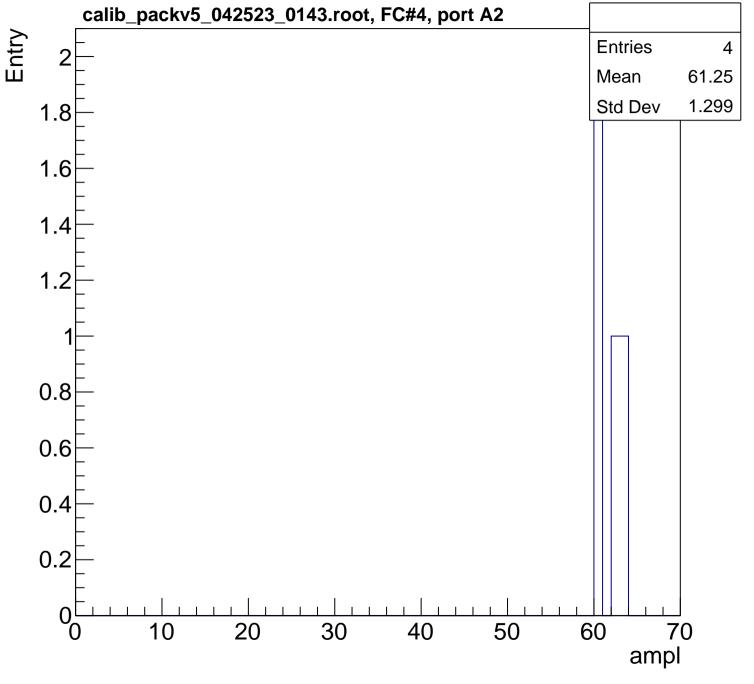


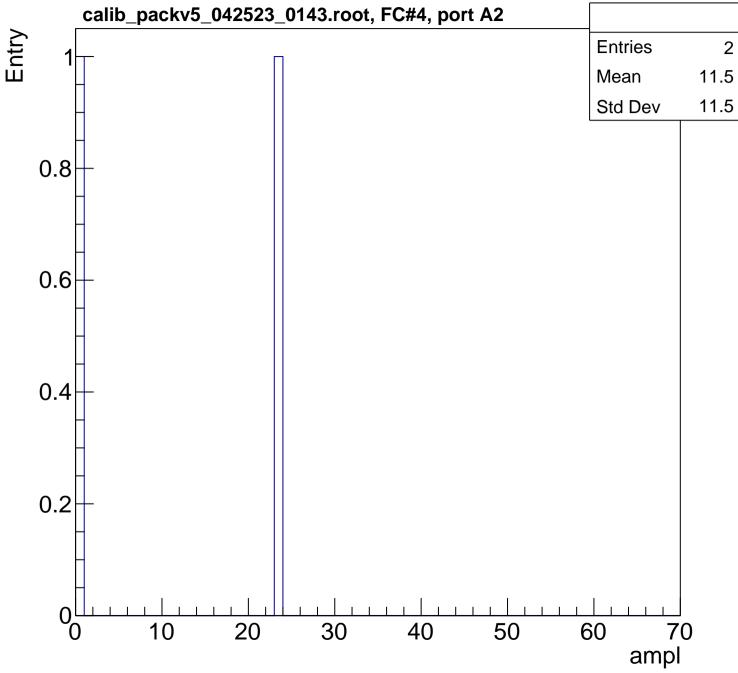


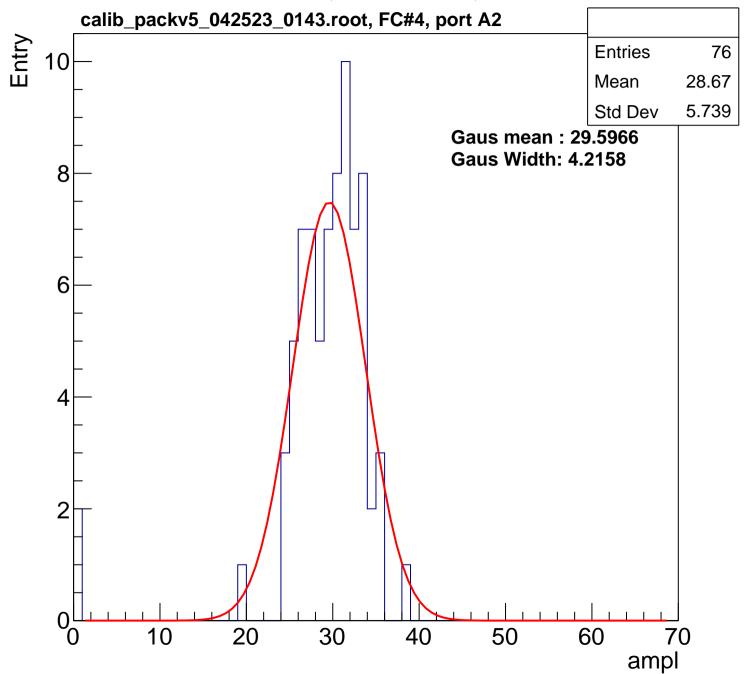


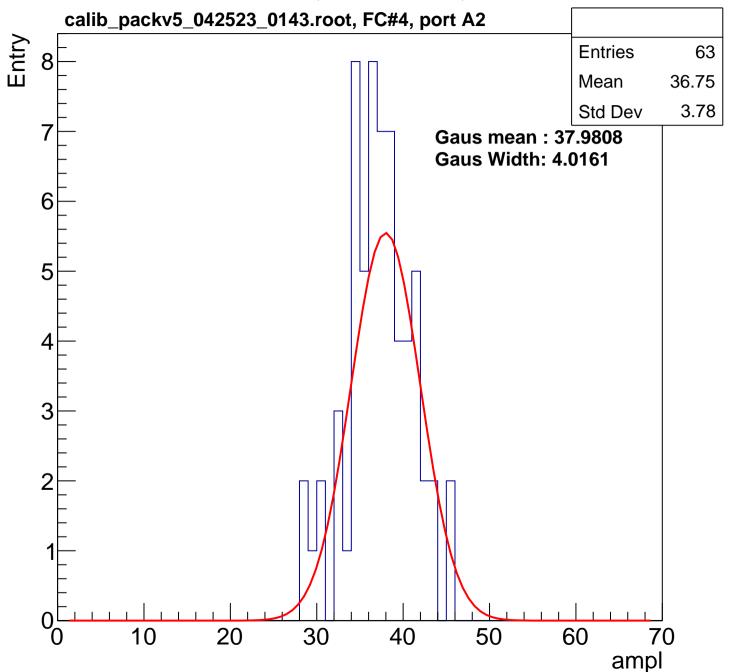


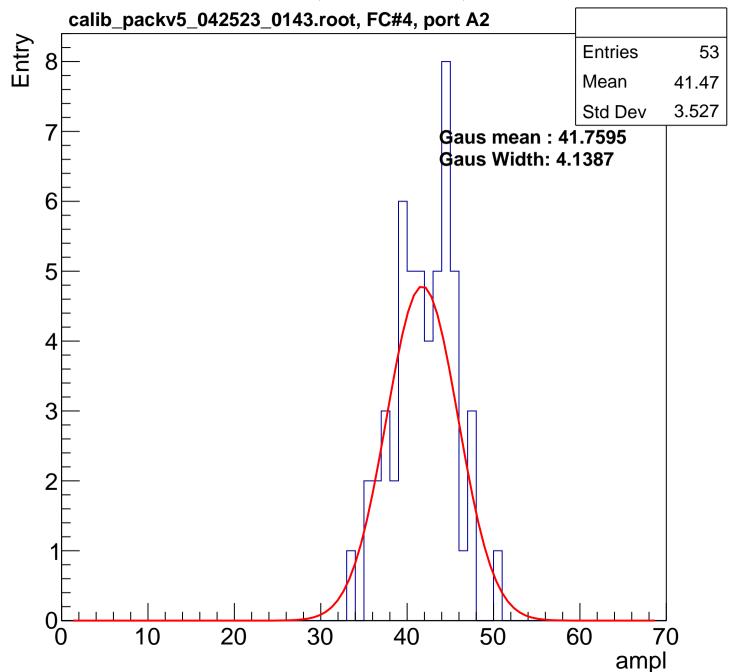


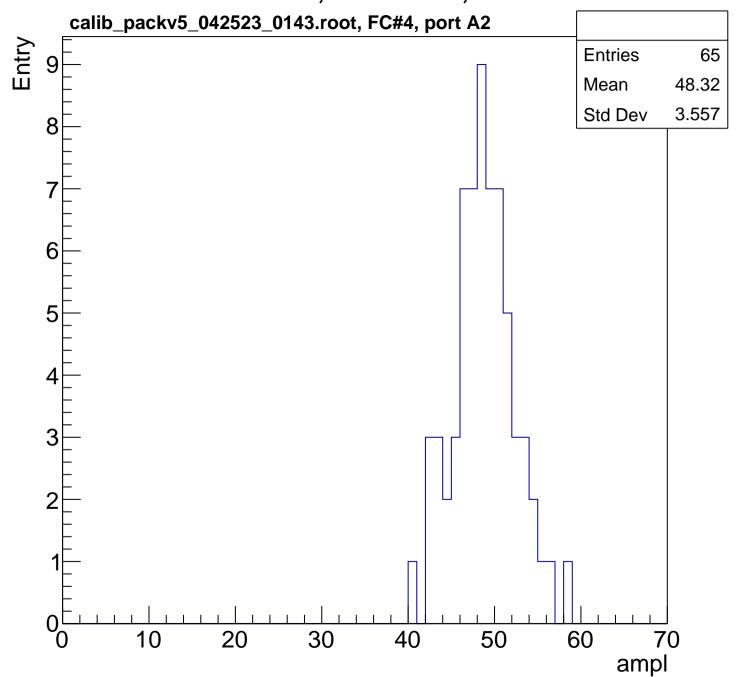


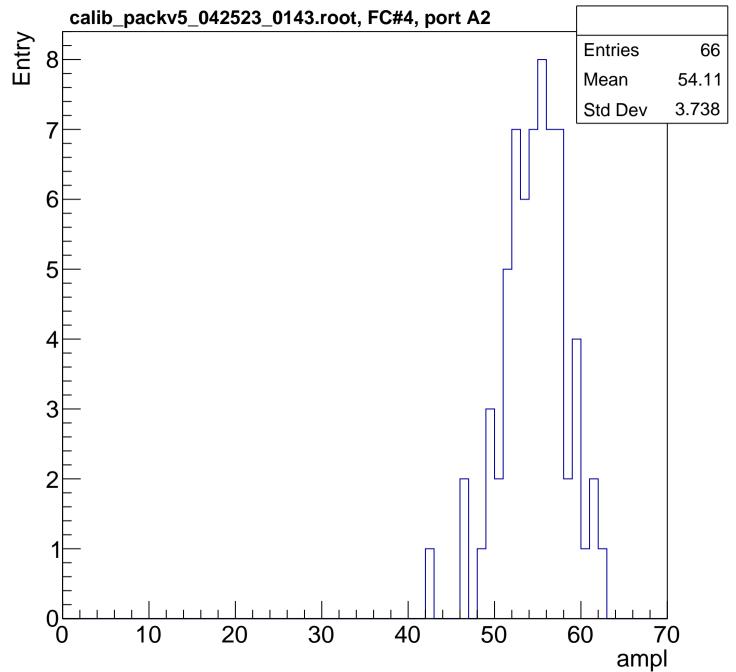


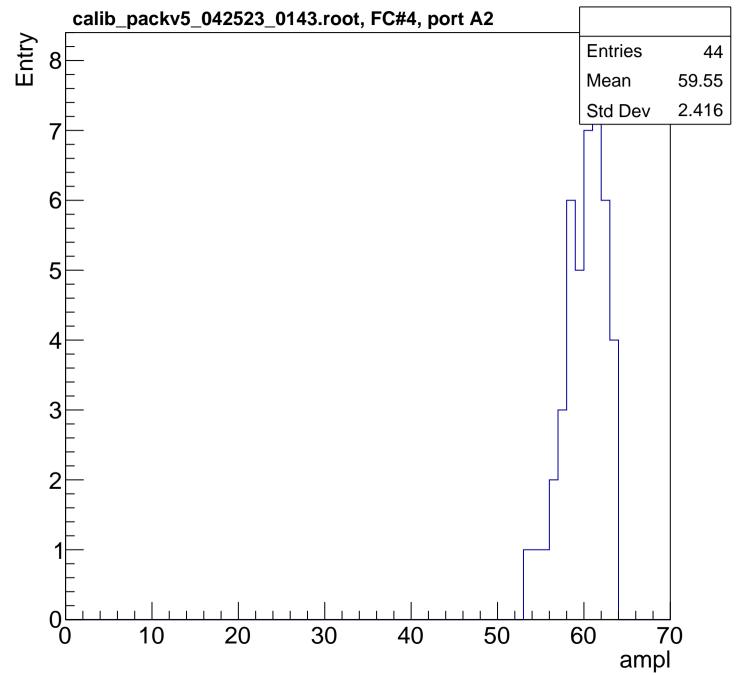


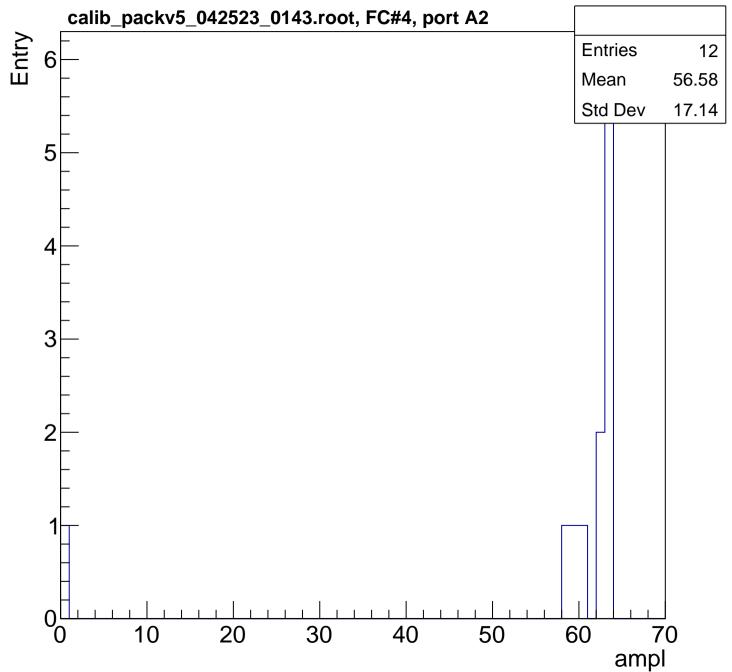


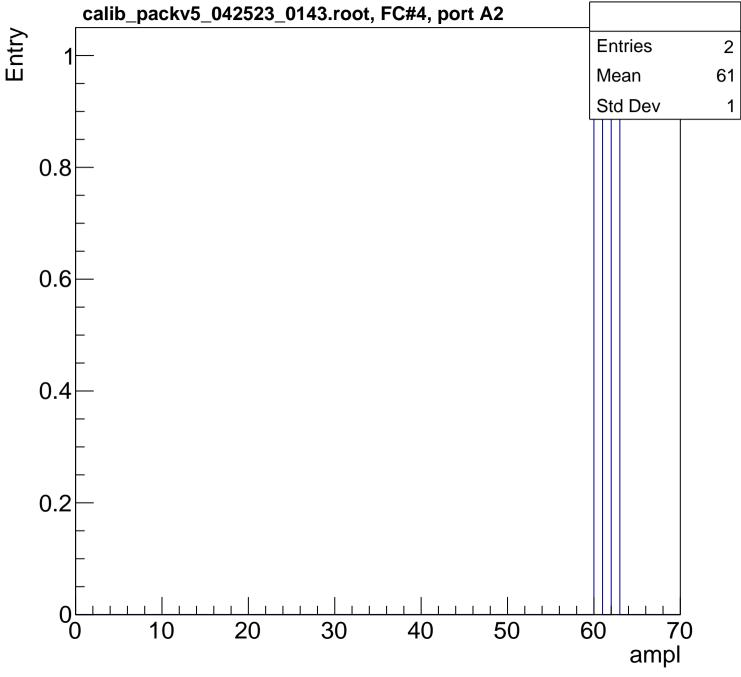


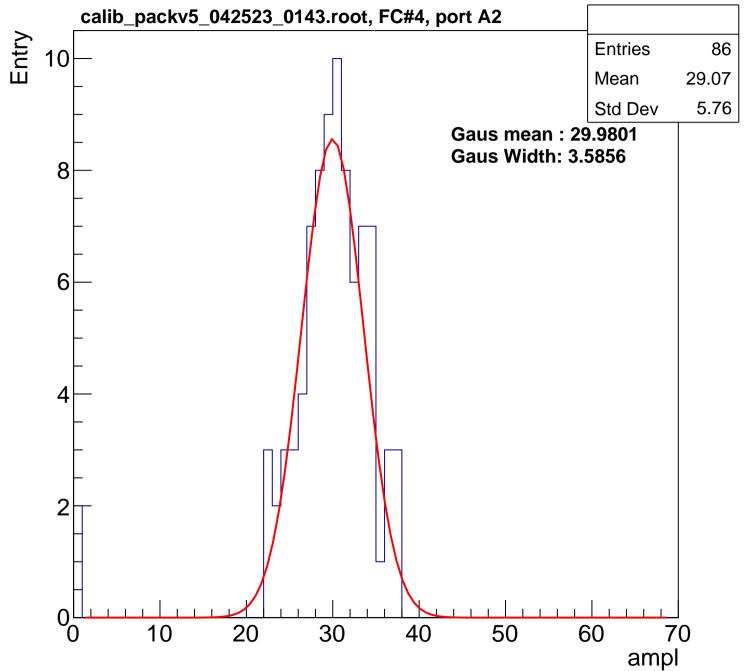


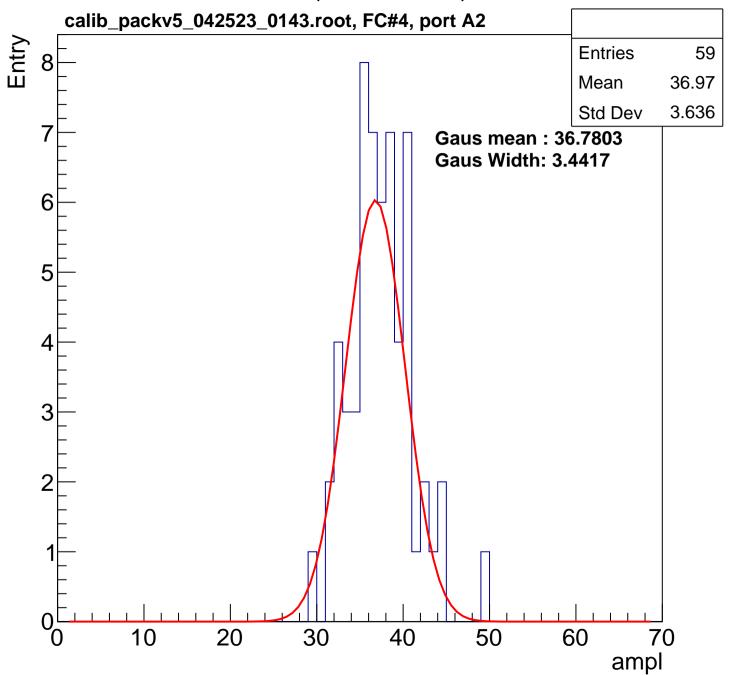


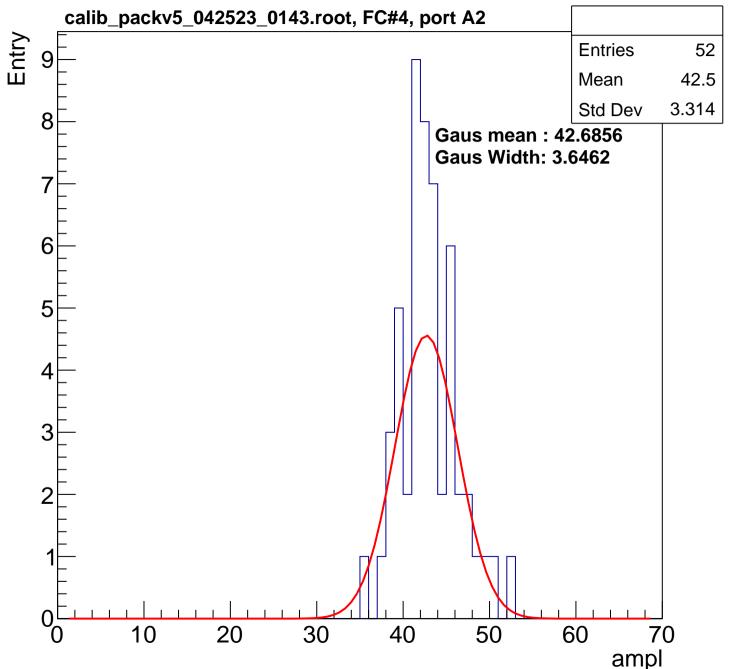


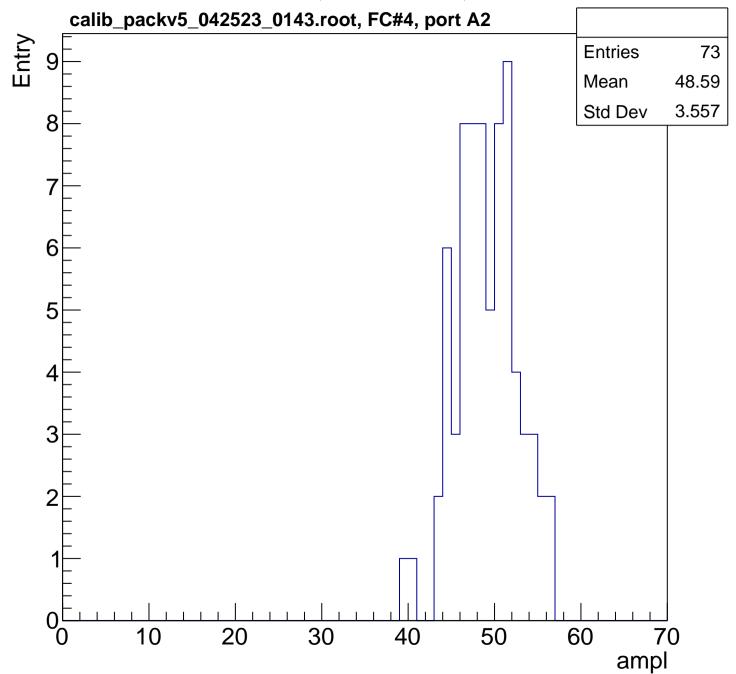


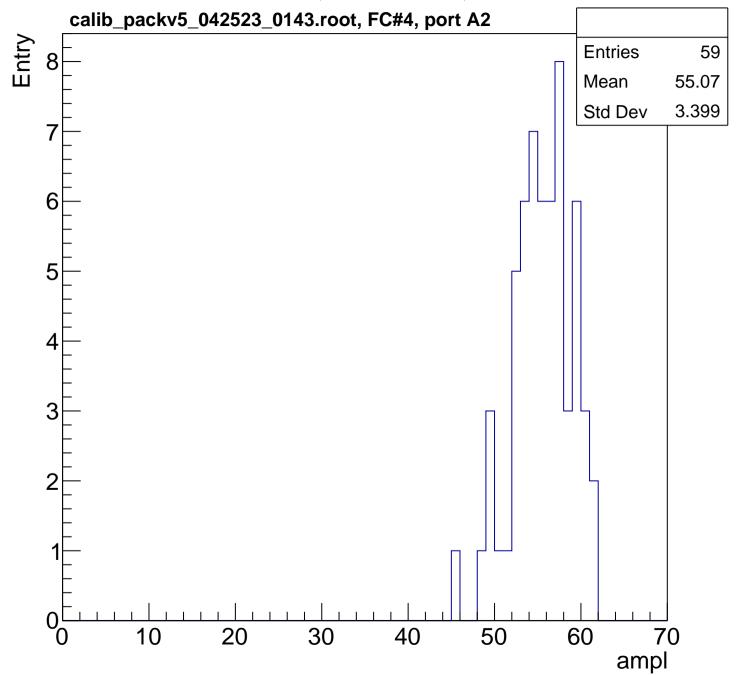


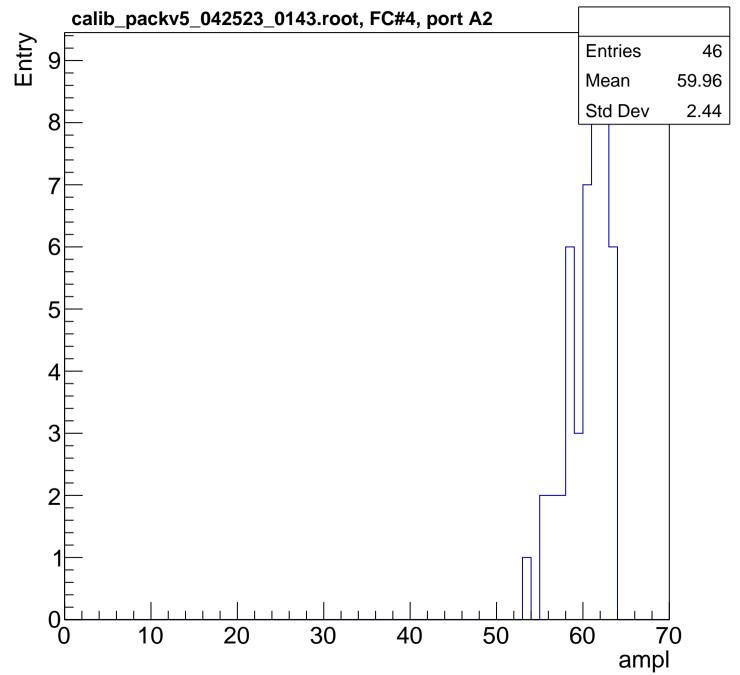


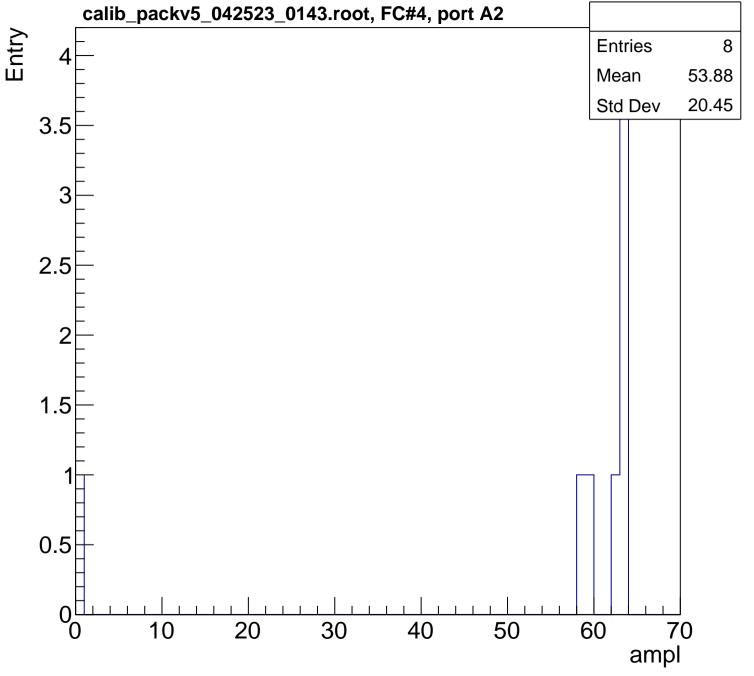


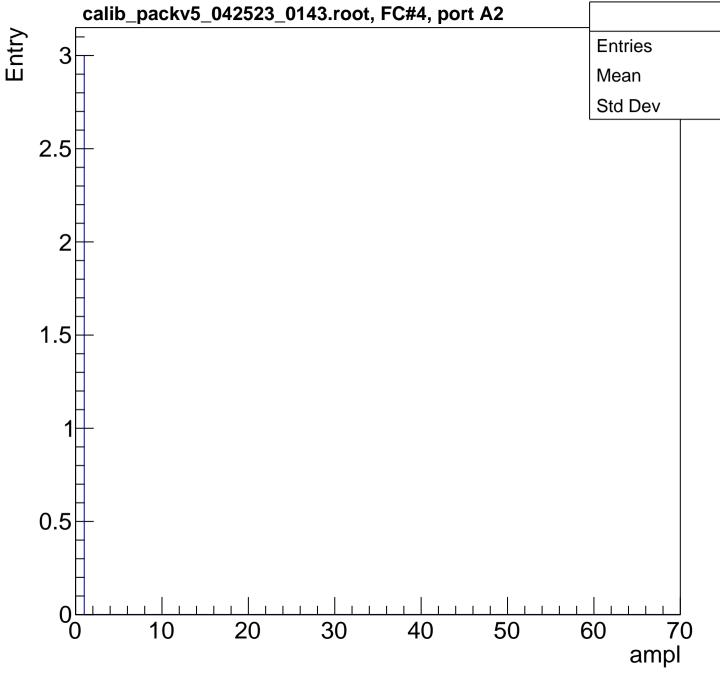


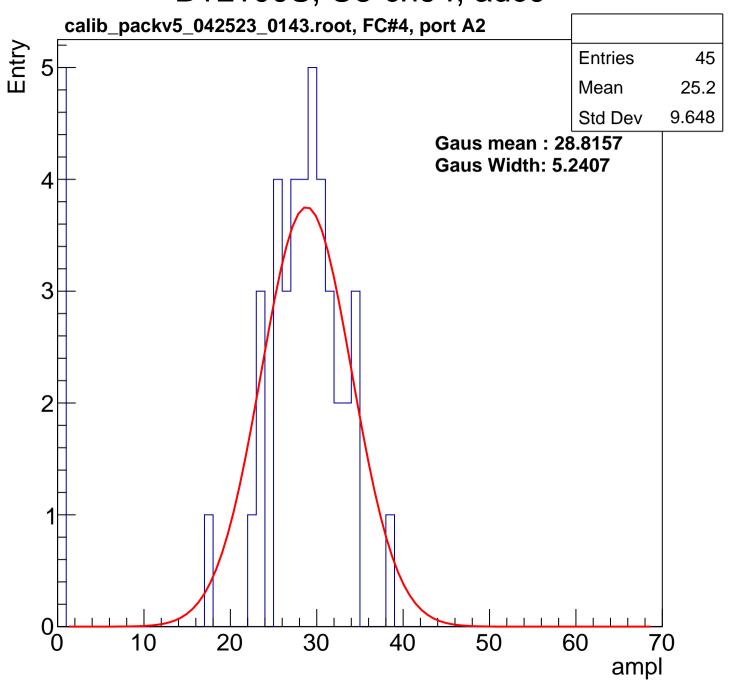


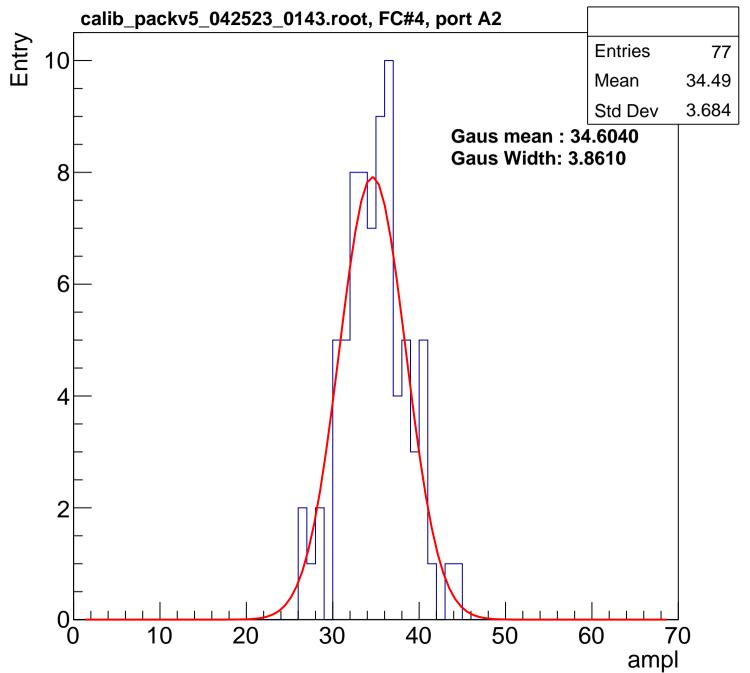


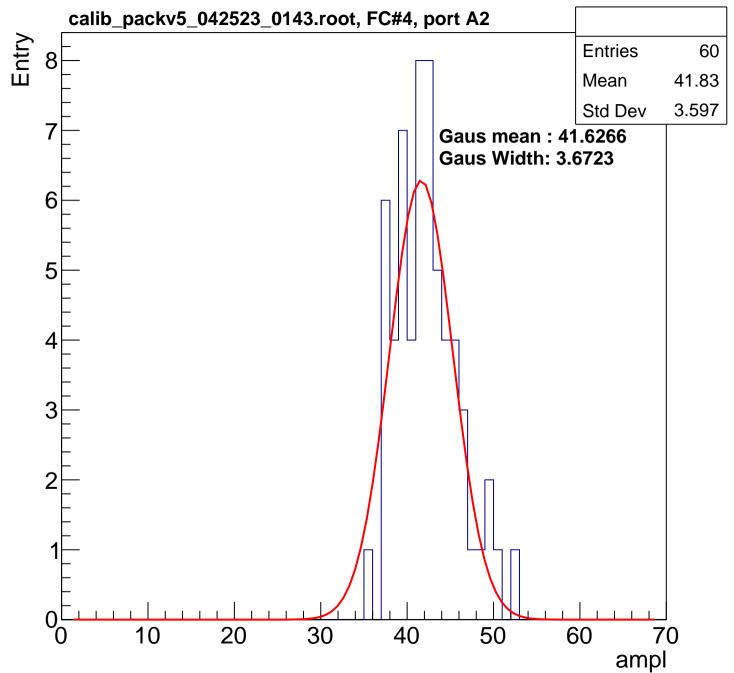


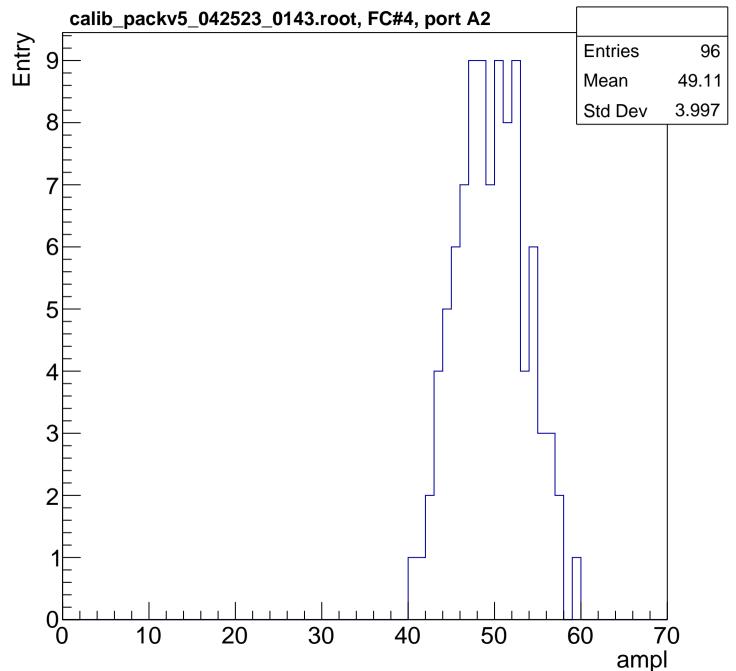


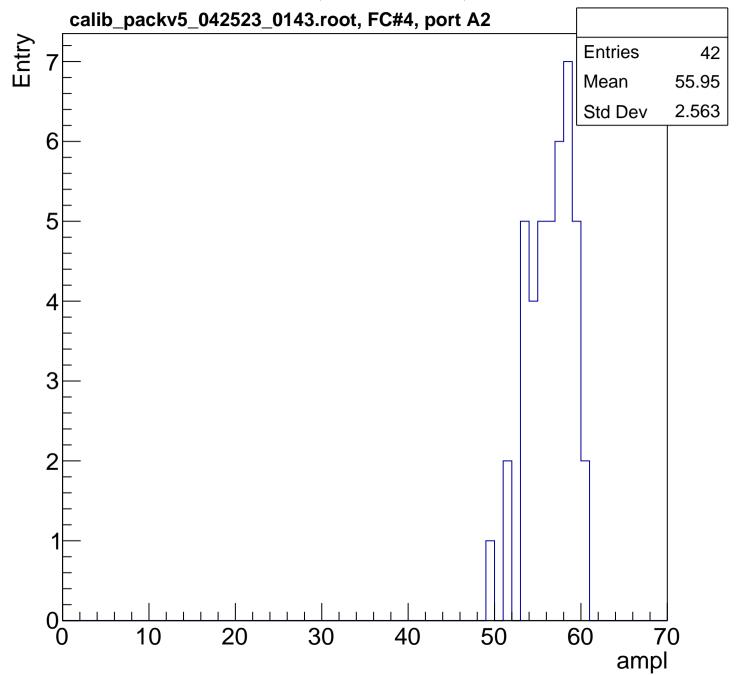


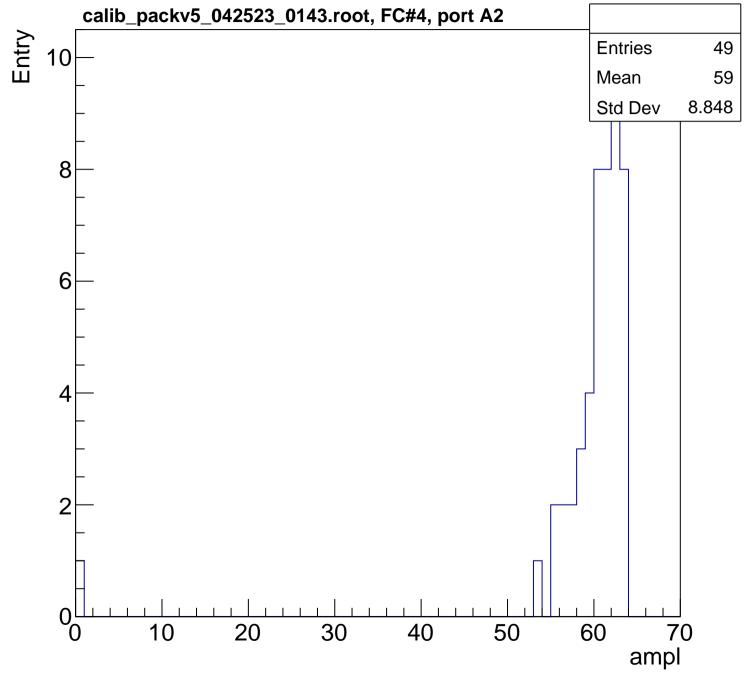


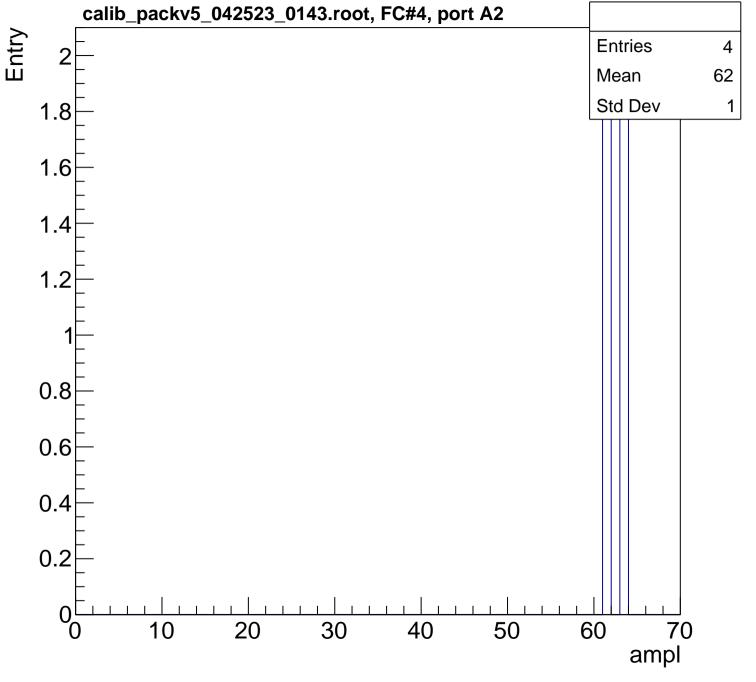




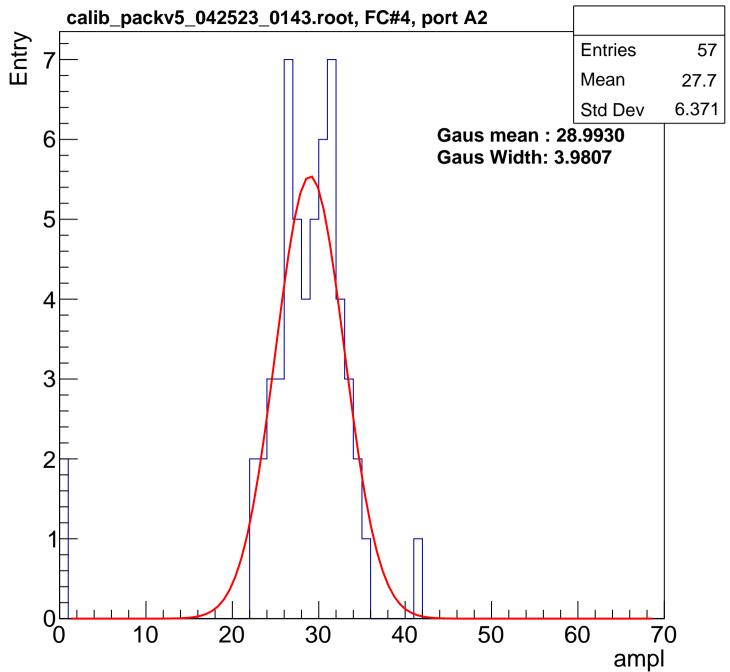


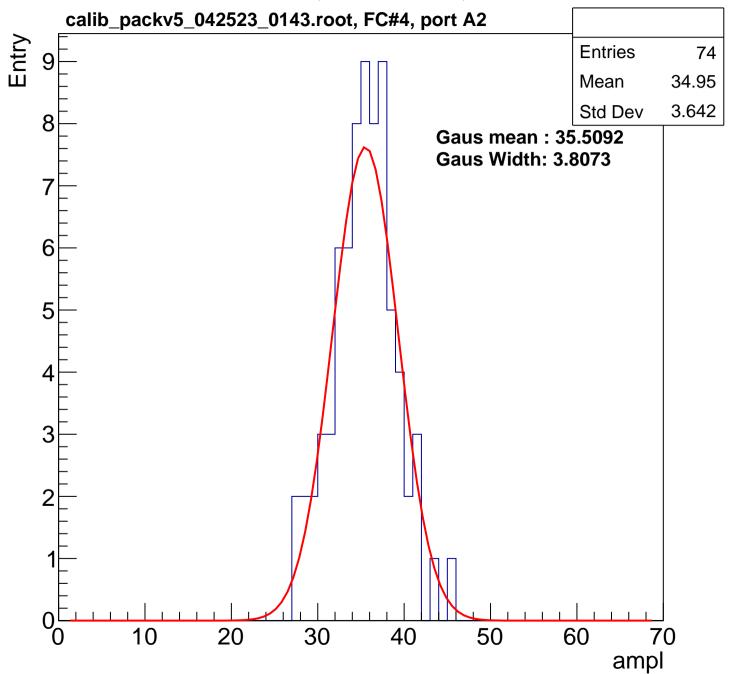


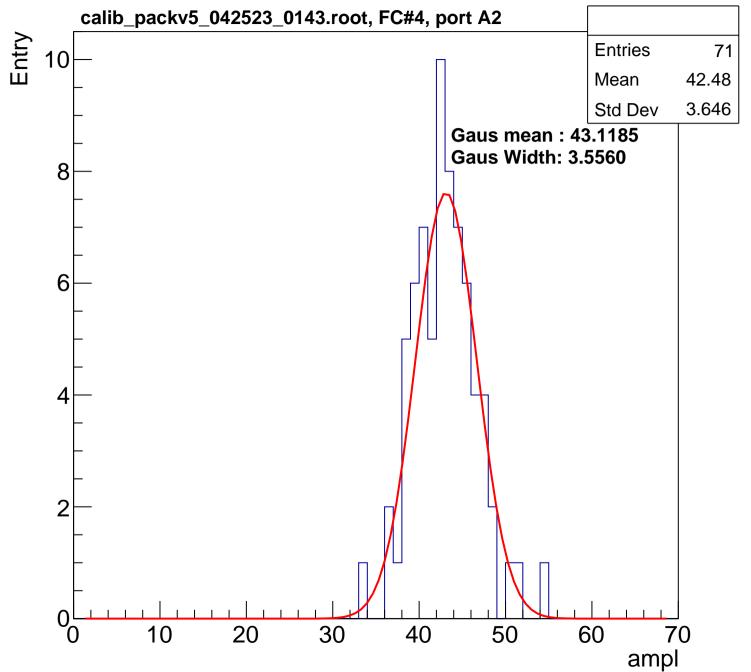


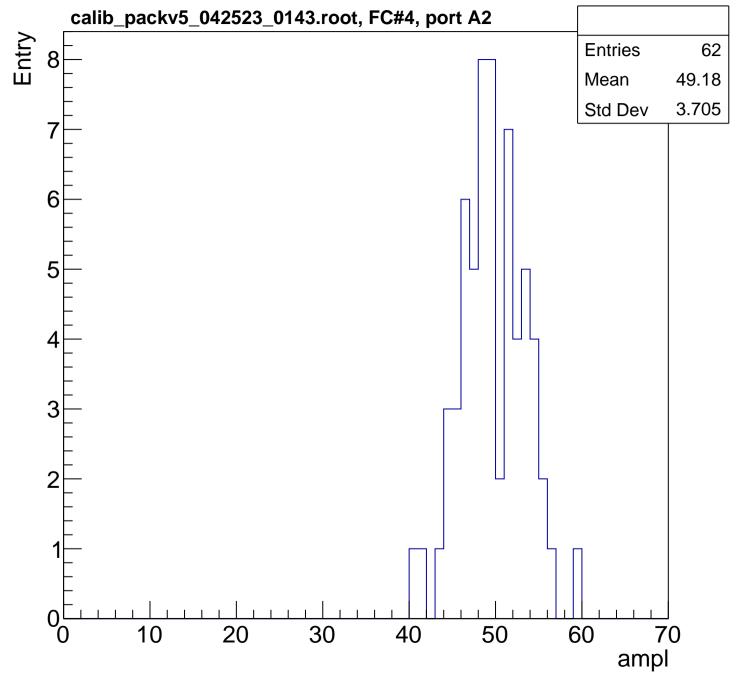


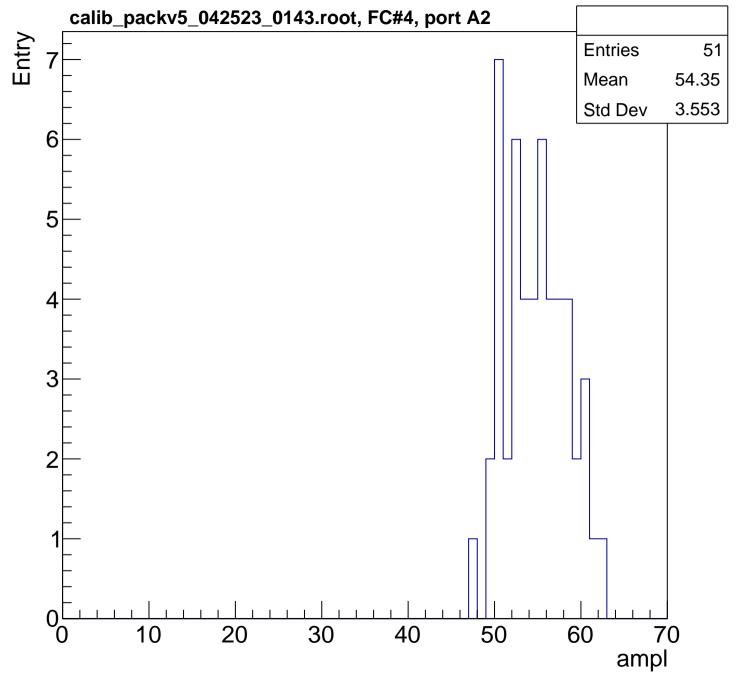


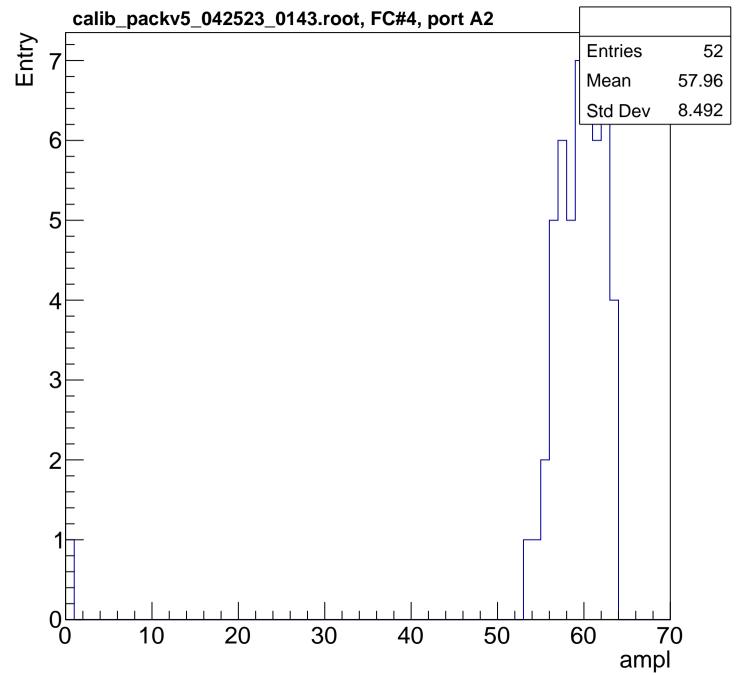


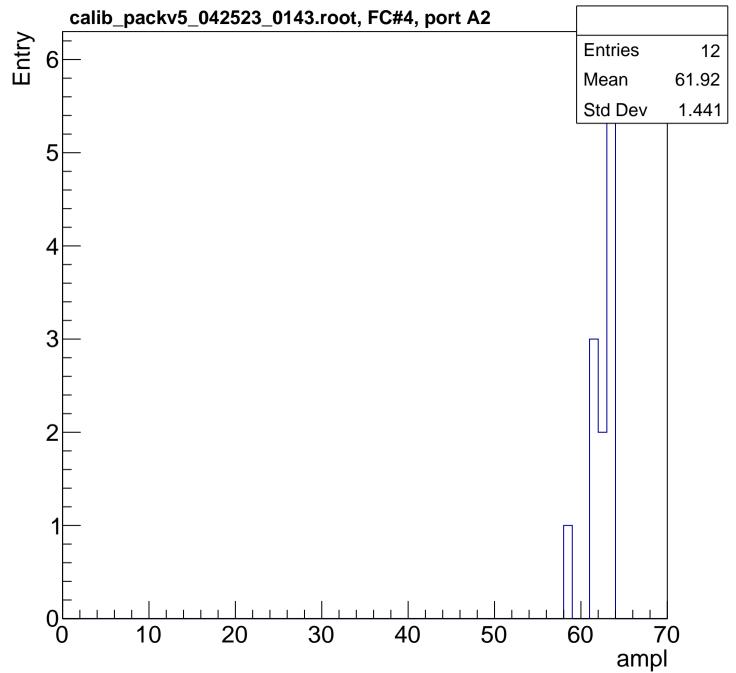


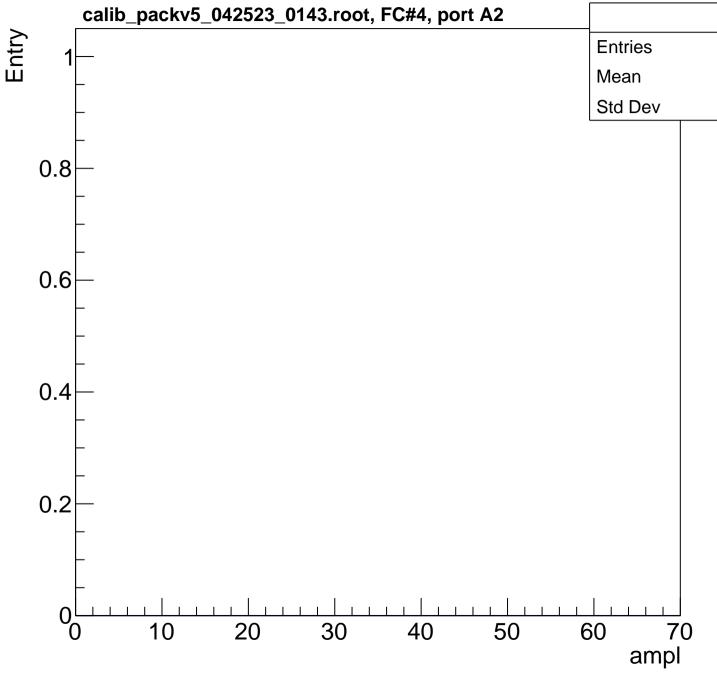


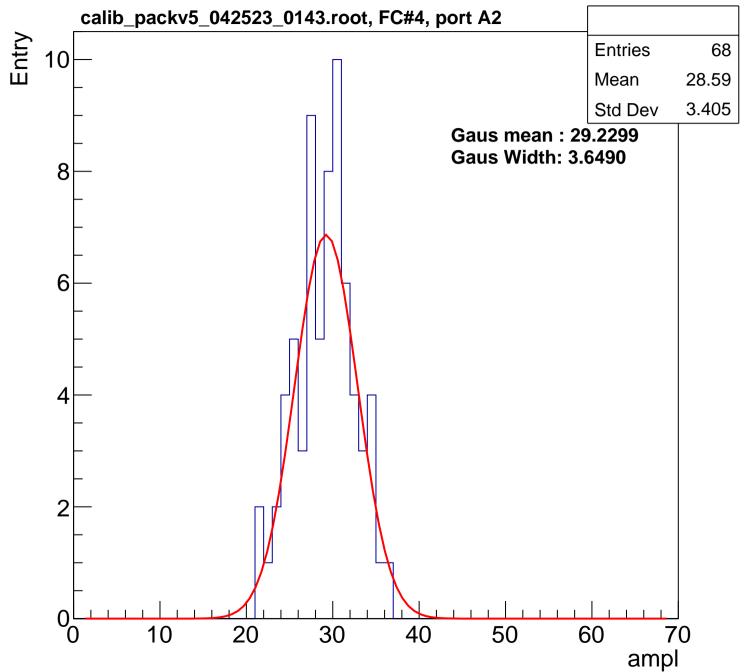


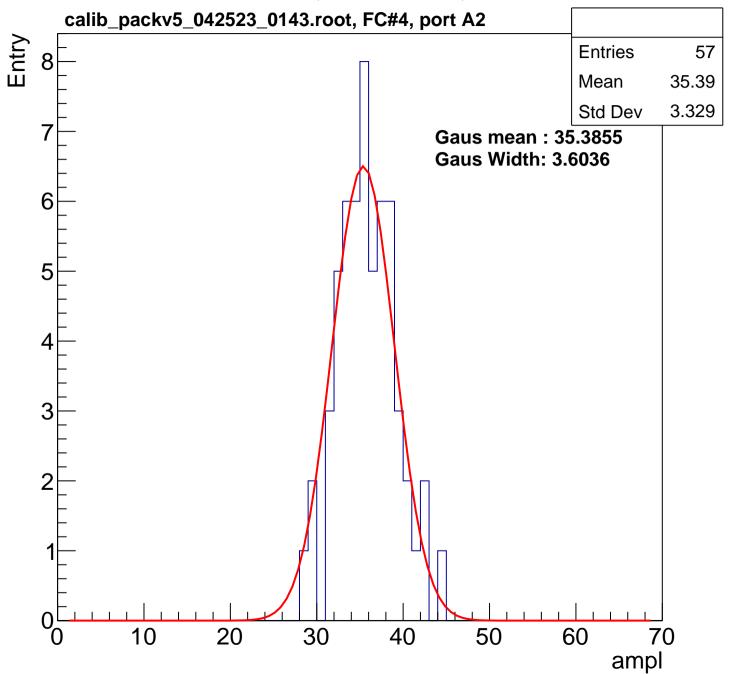


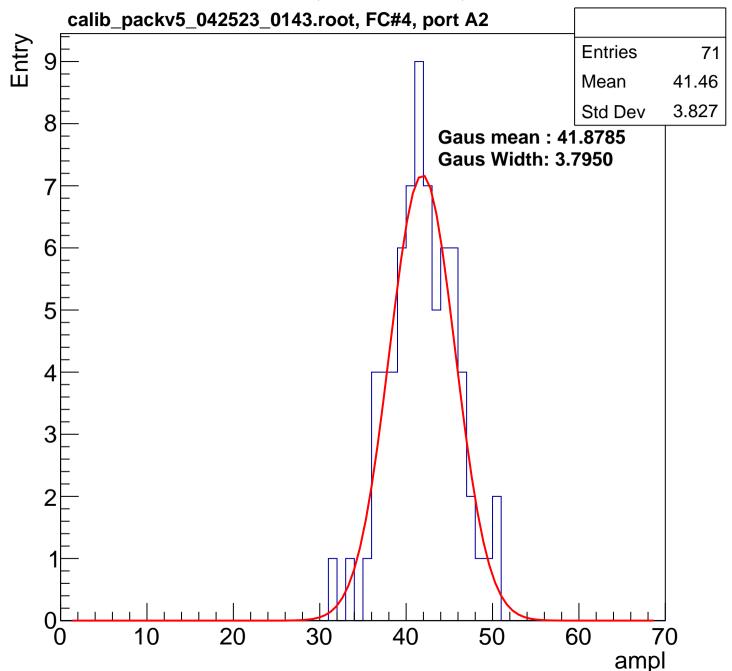


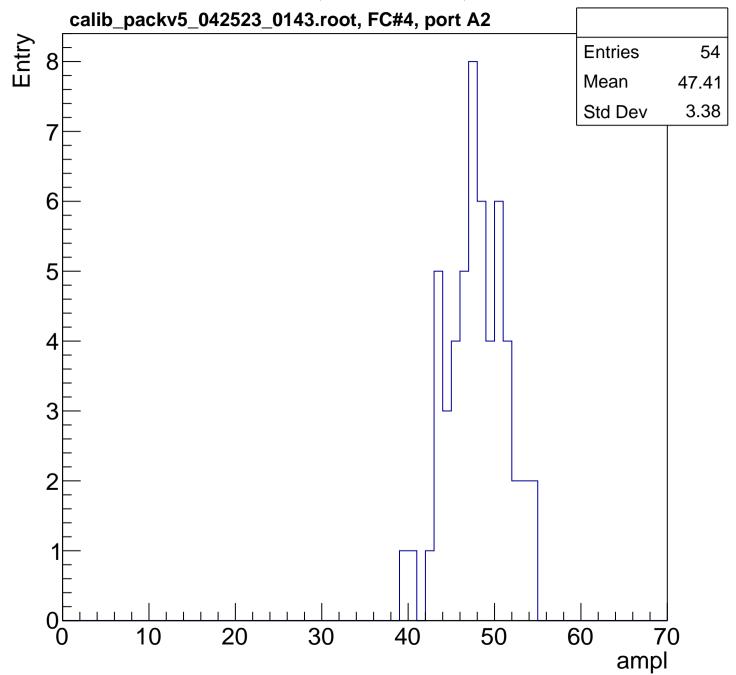


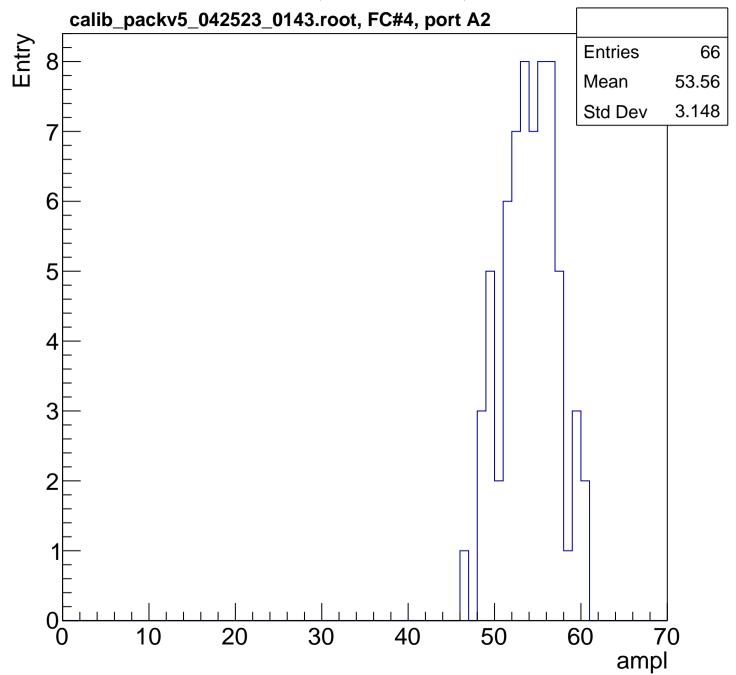


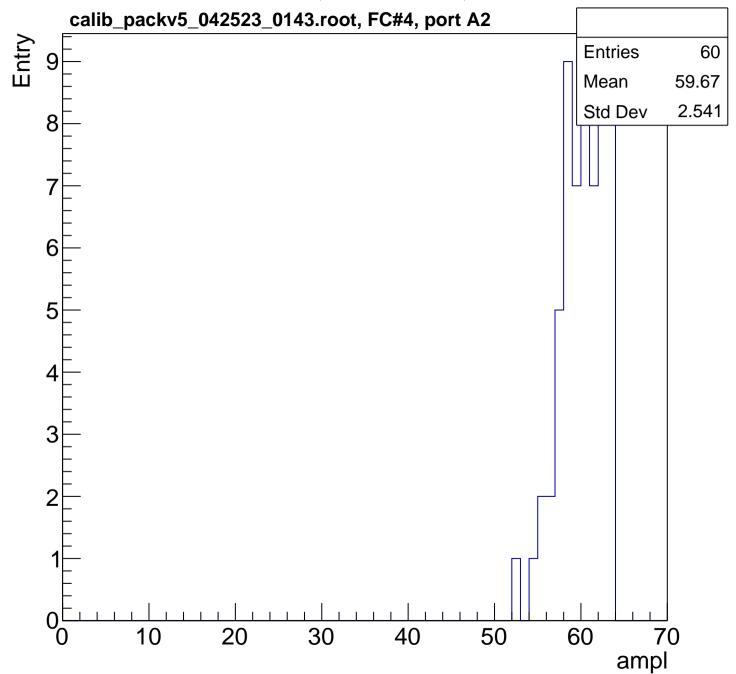


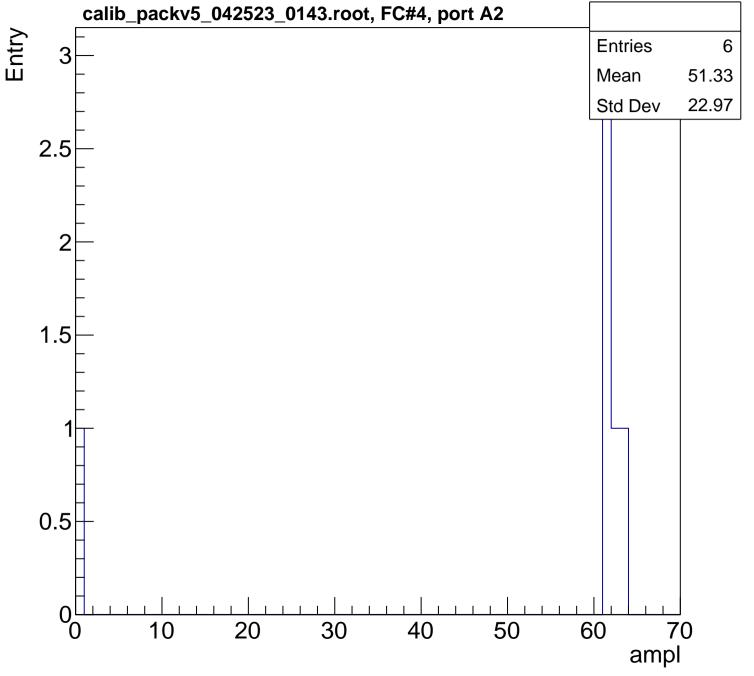










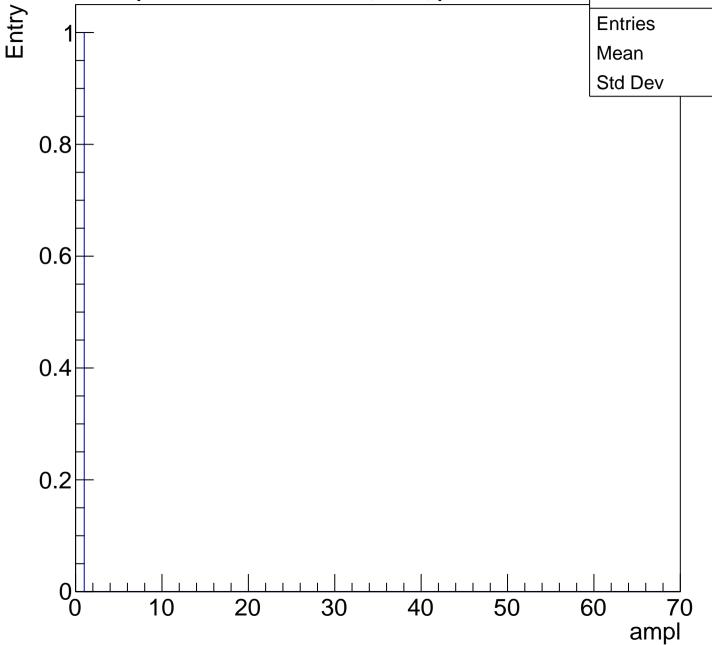


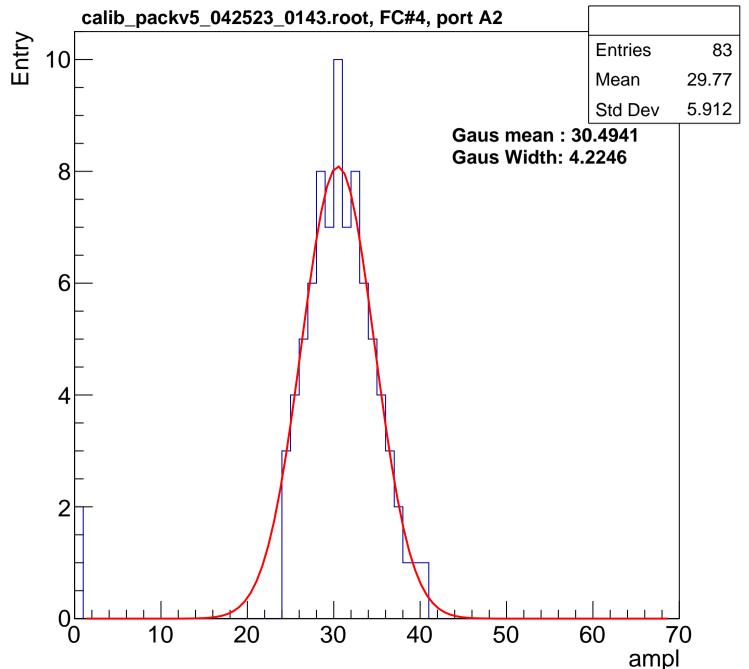
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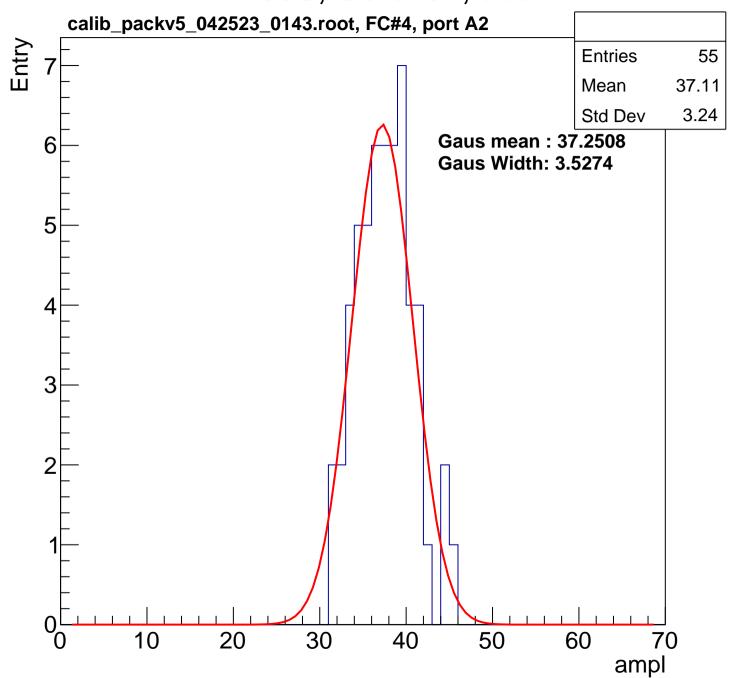
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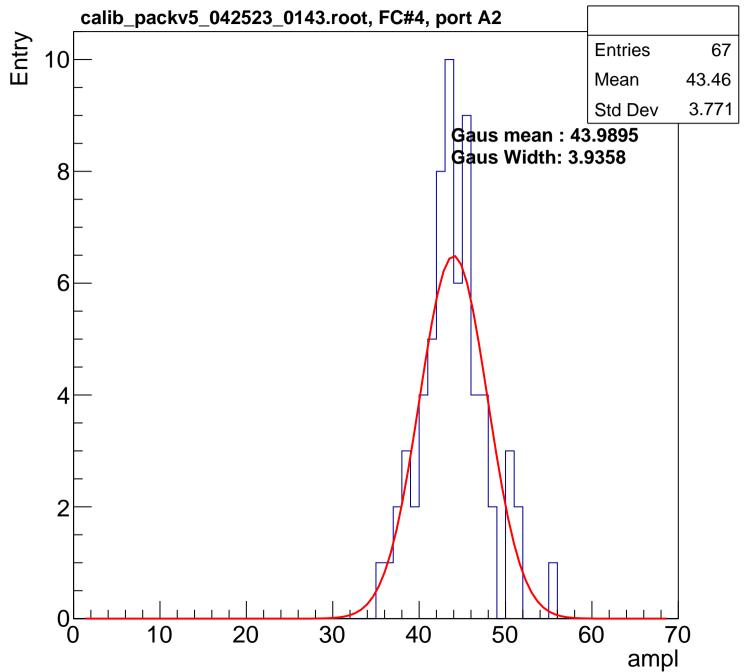
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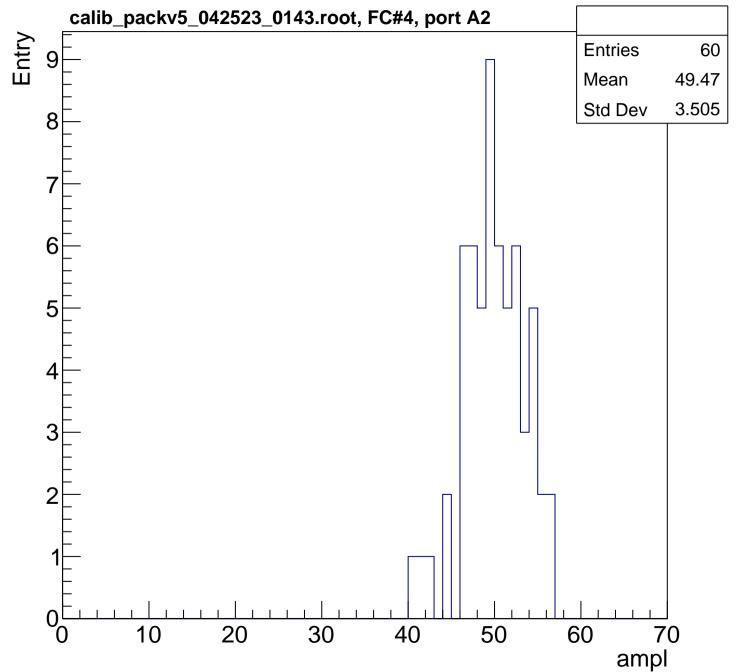
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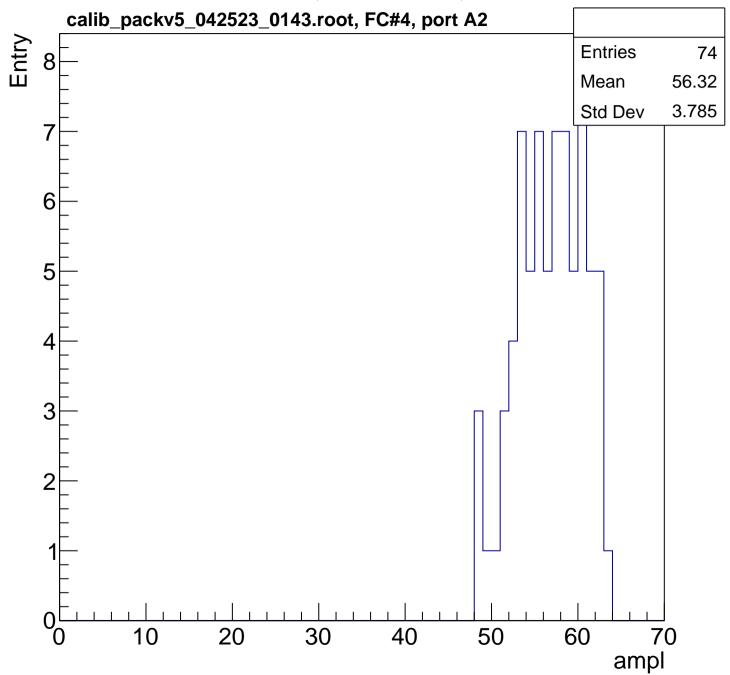


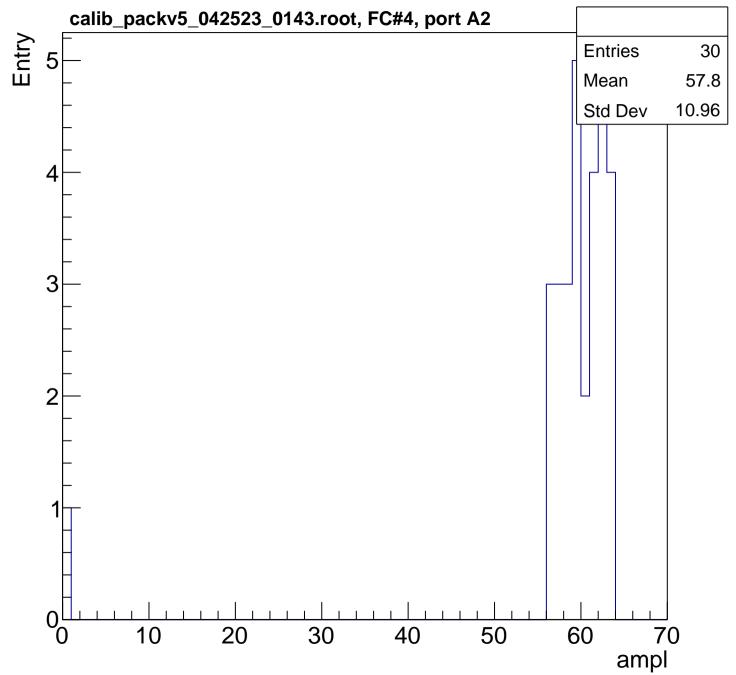


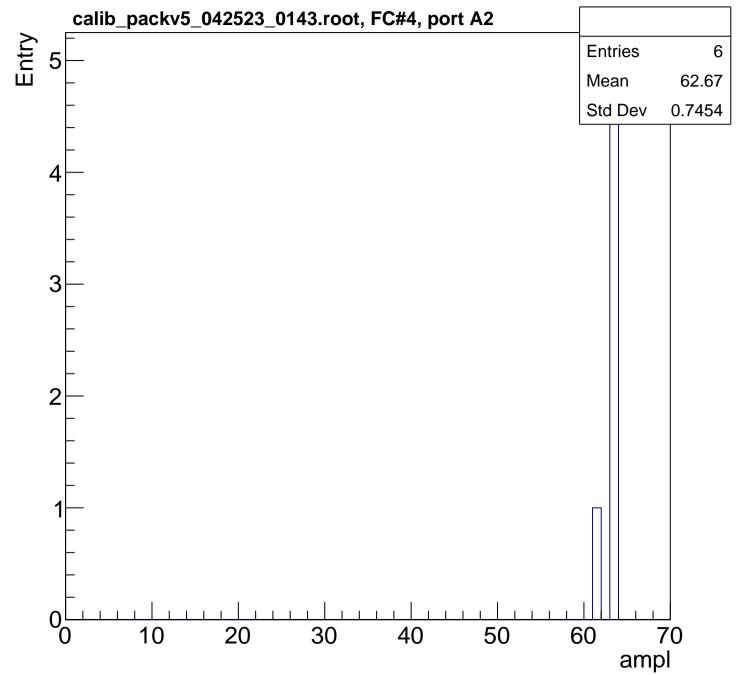










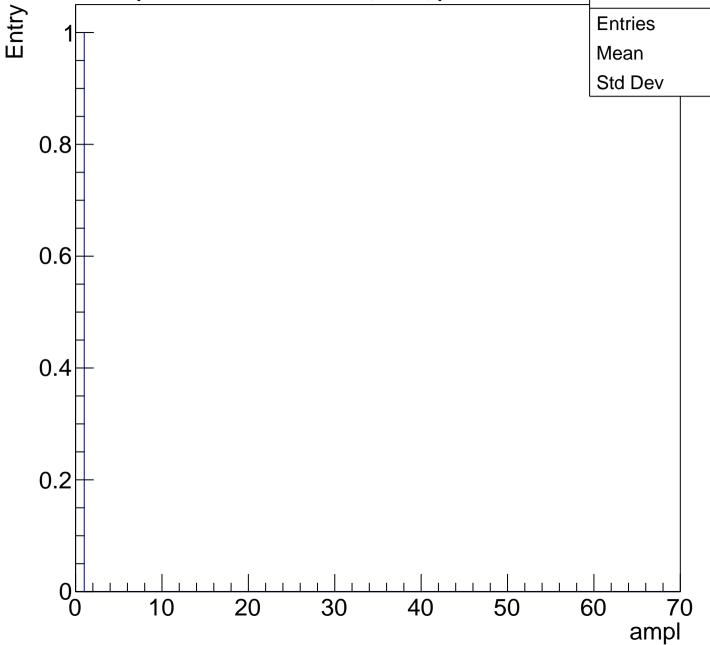


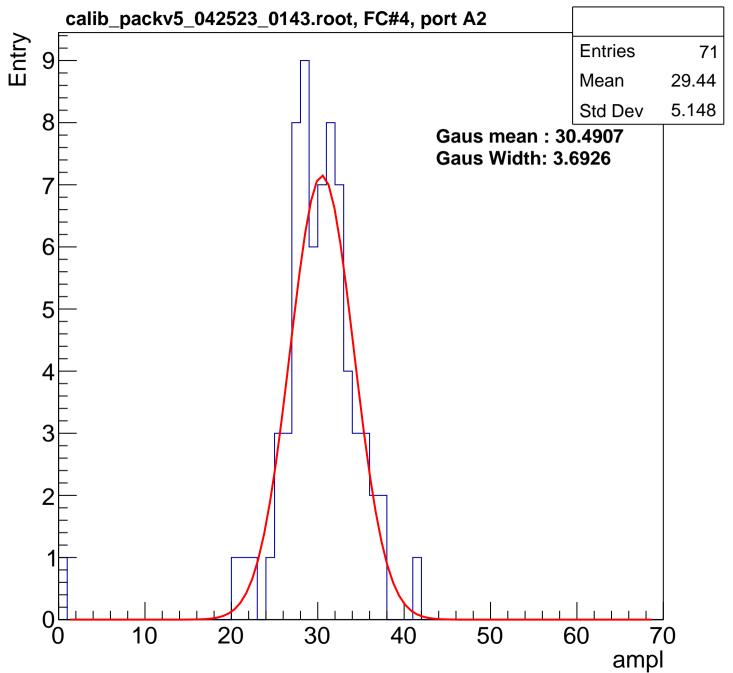
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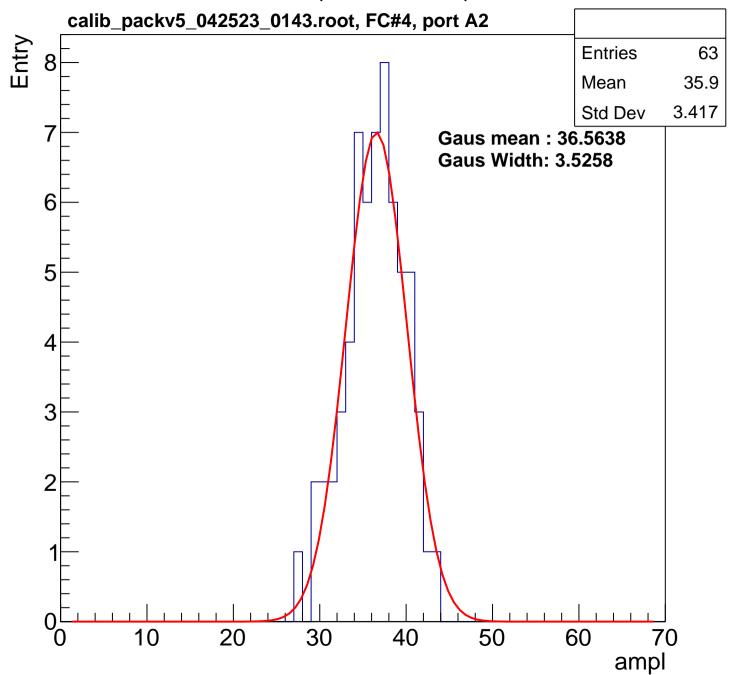
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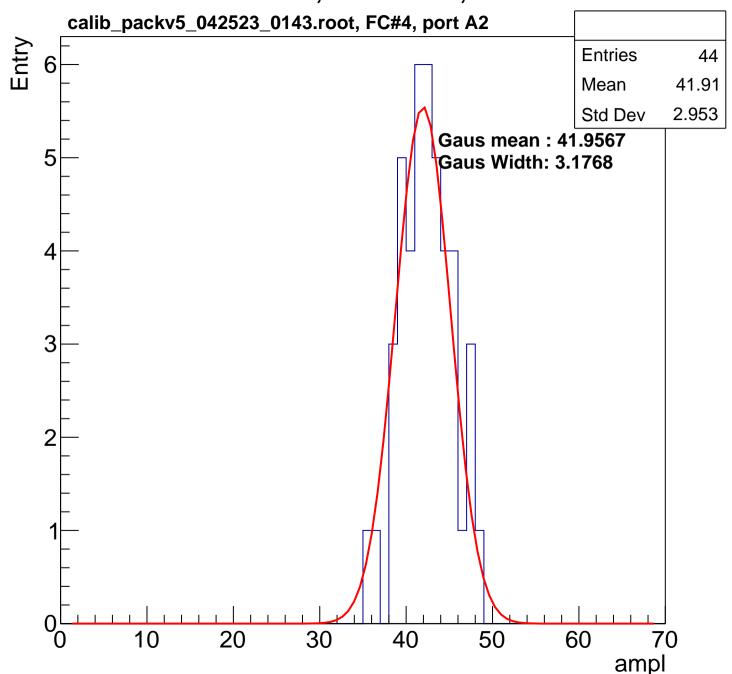
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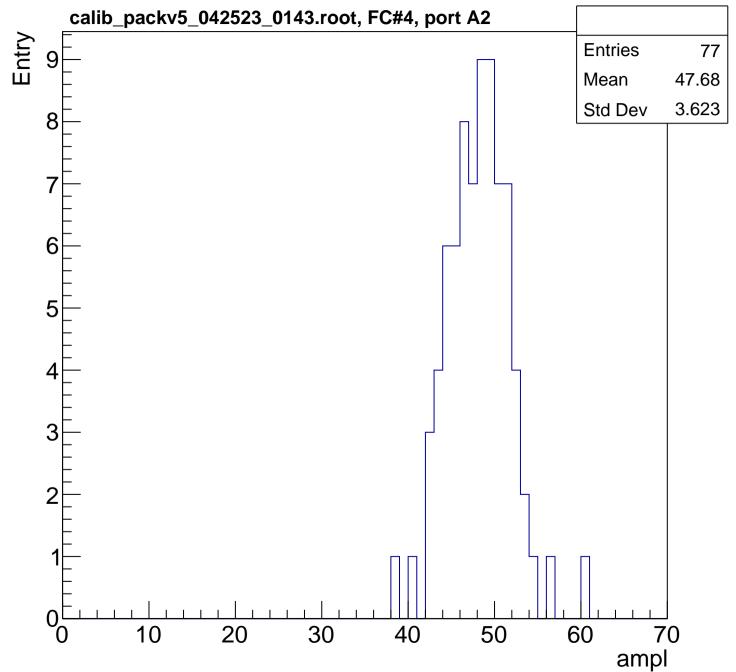
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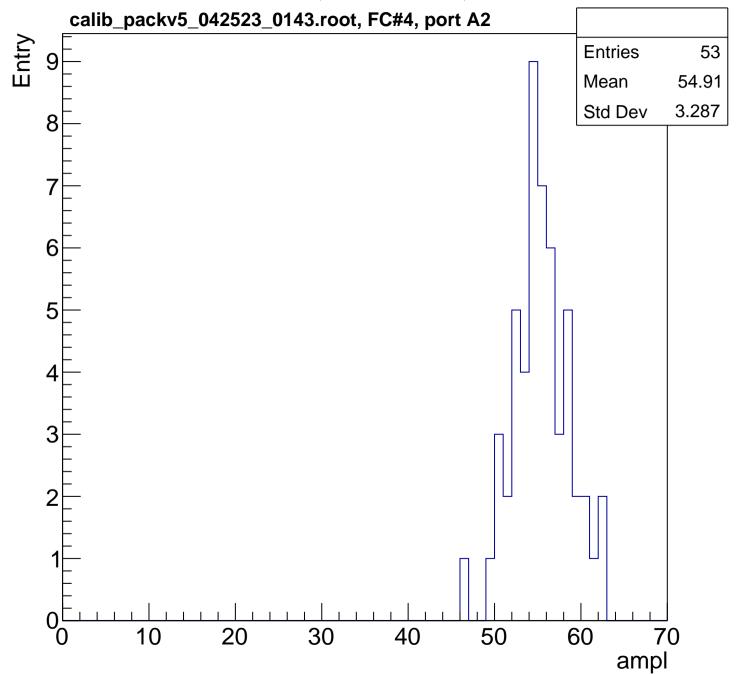


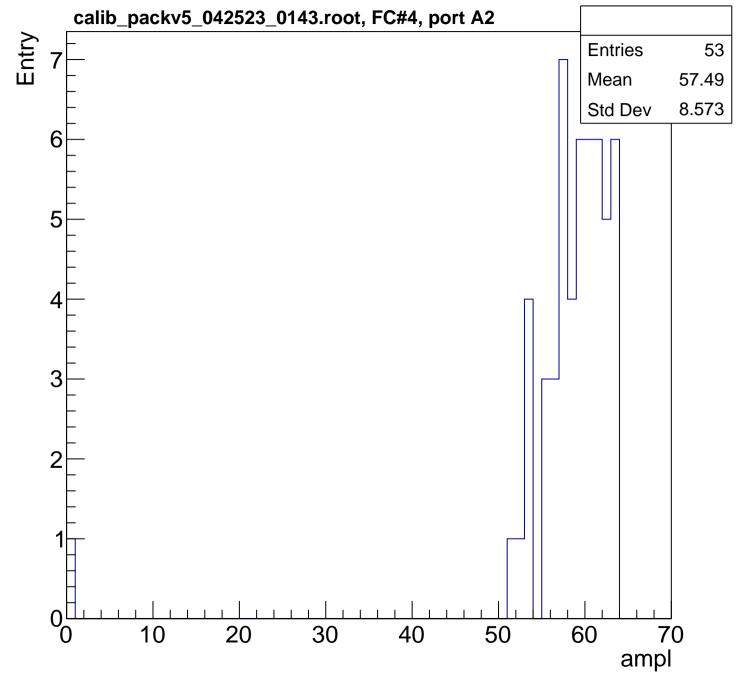


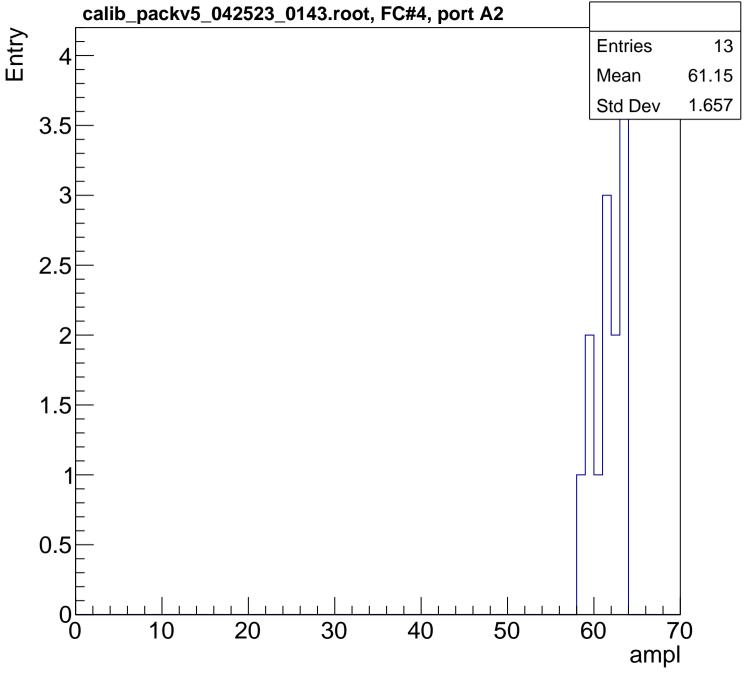


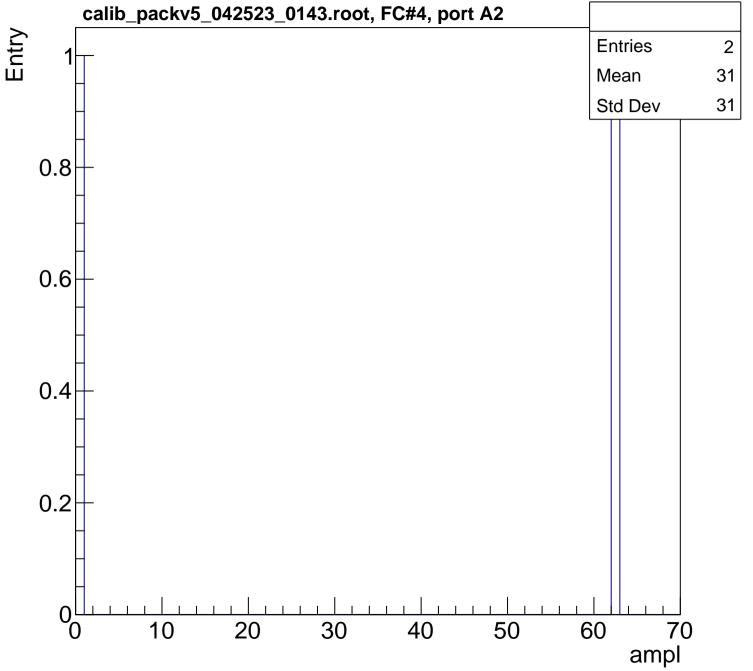


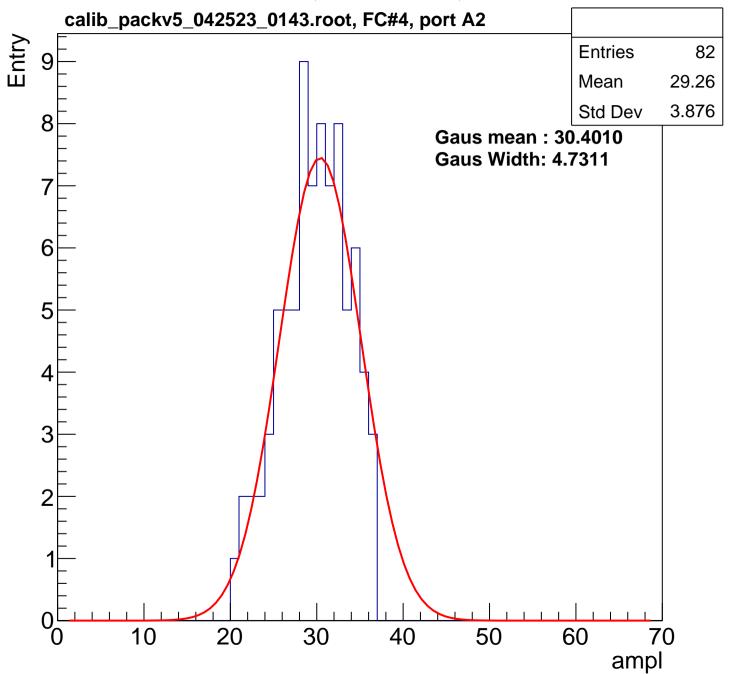


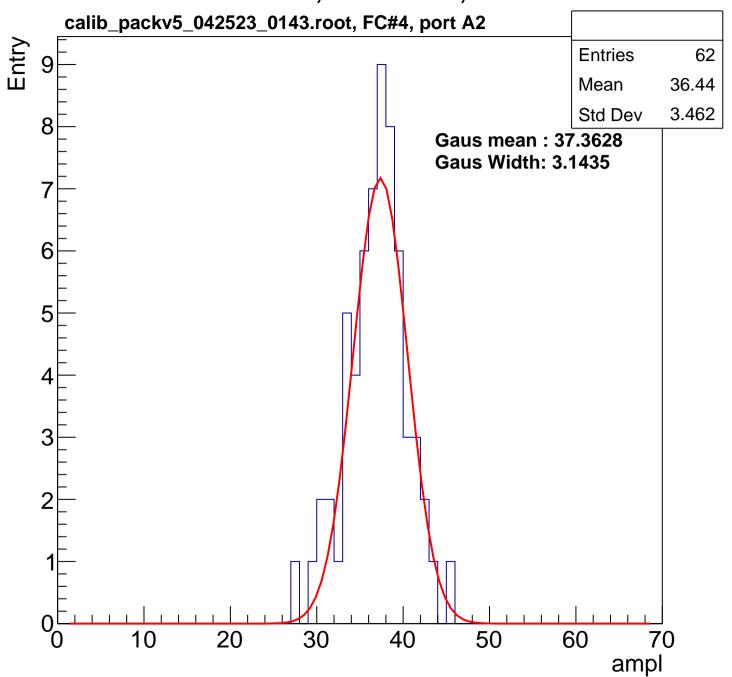


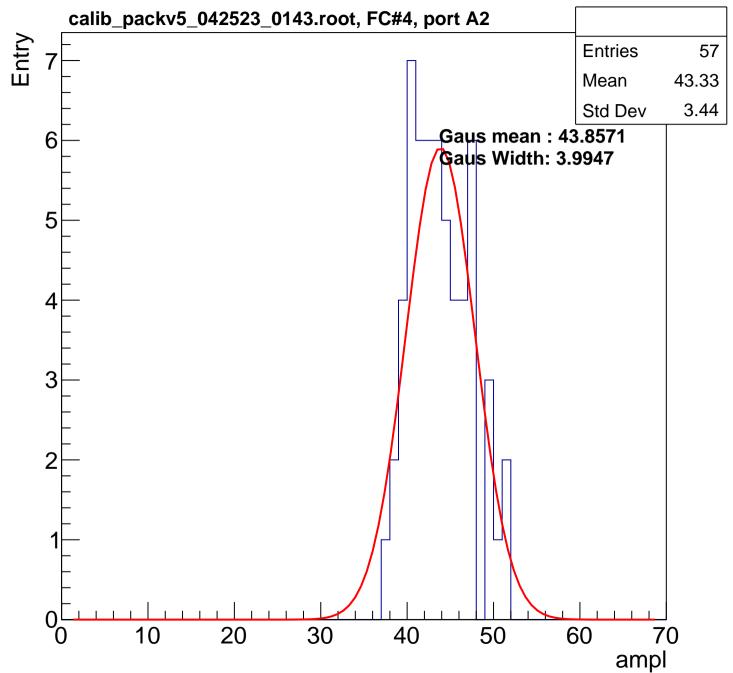


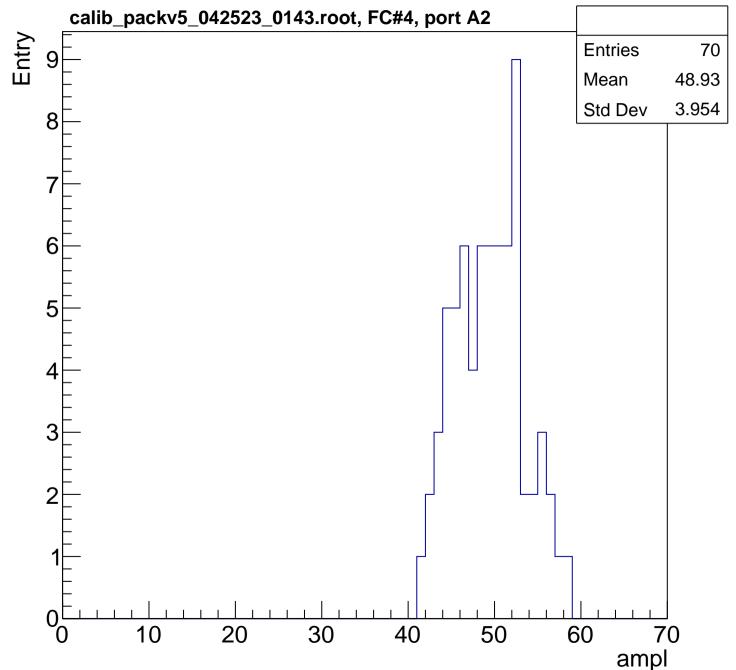


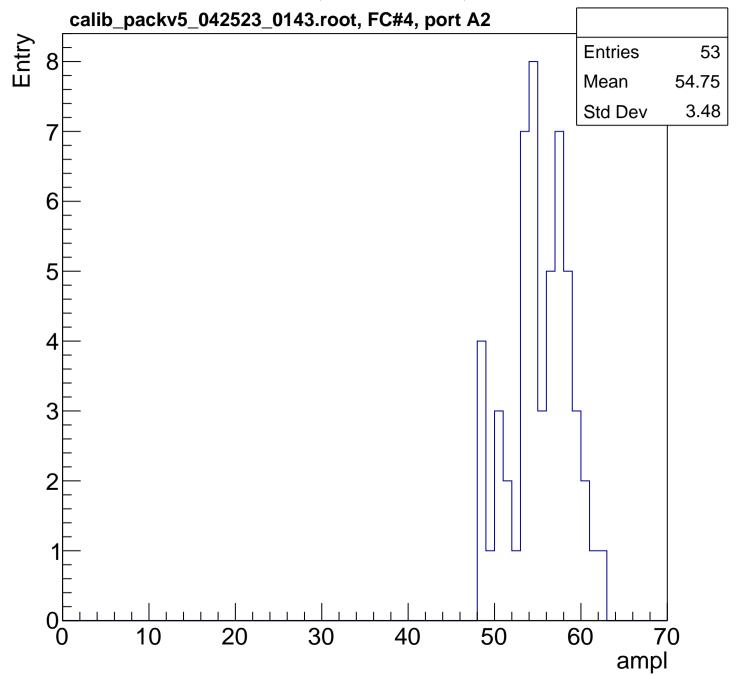


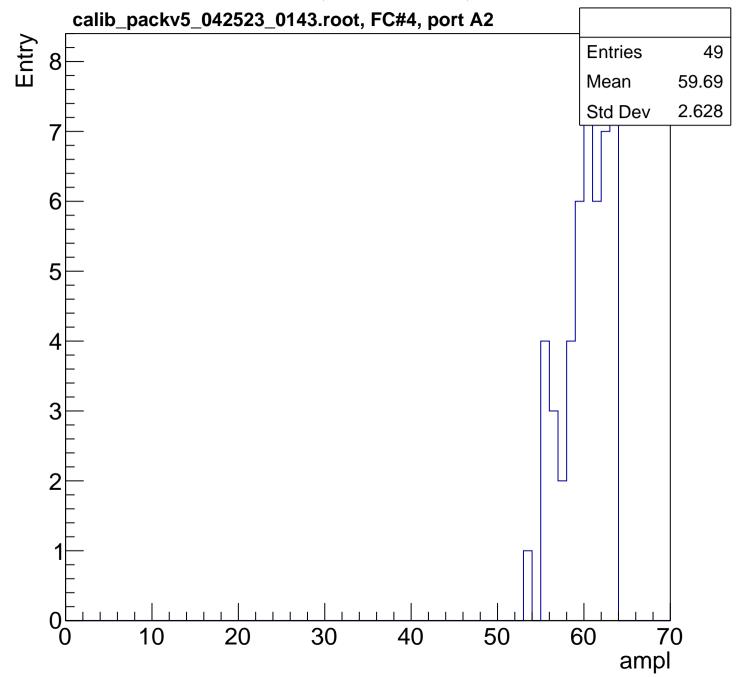


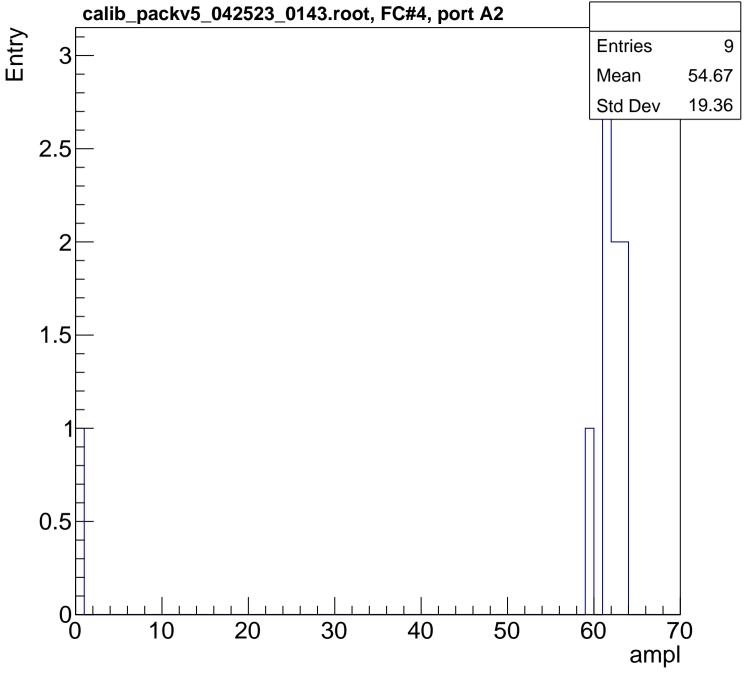












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