



# B1L003S, U26-ch0, adc0

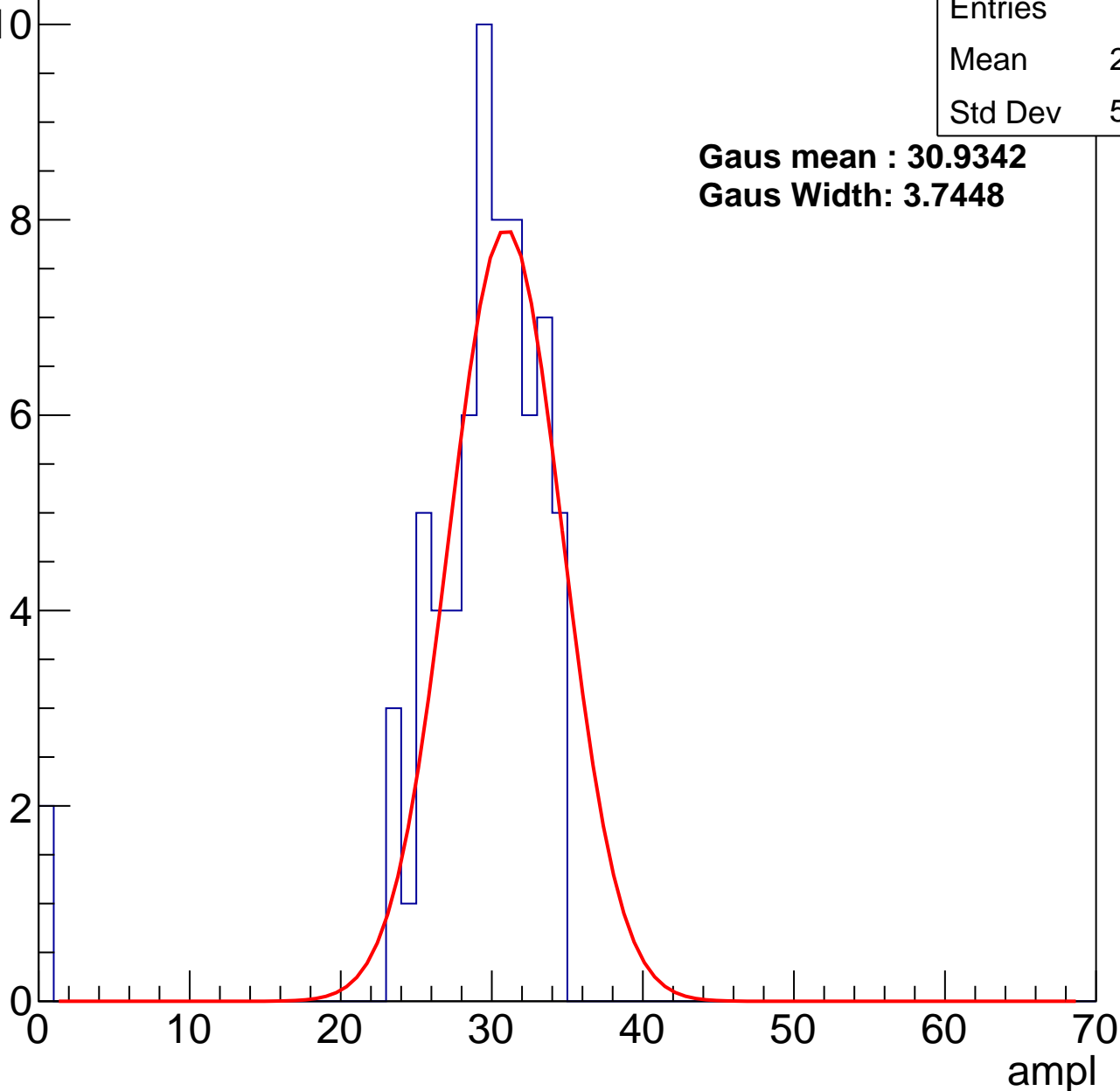
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	28.54
Std Dev	5.735

**Gaus mean : 30.9342**

**Gaus Width: 3.7448**



# B1L003S, U26-ch0, adc1

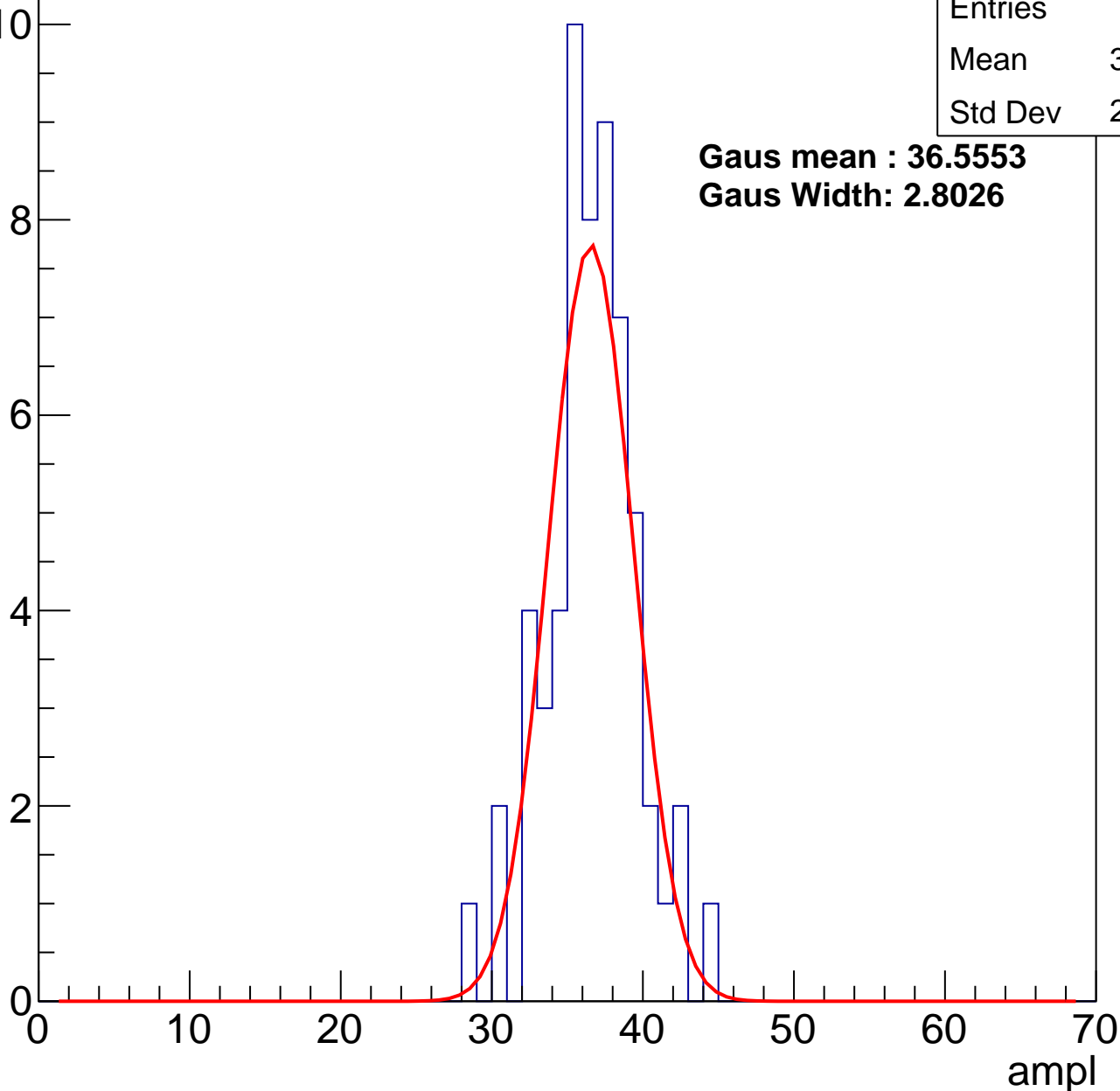
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	36.14
Std Dev	2.988

**Gaus mean : 36.5553**

**Gaus Width: 2.8026**



# B1L003S, U26-ch0, adc2

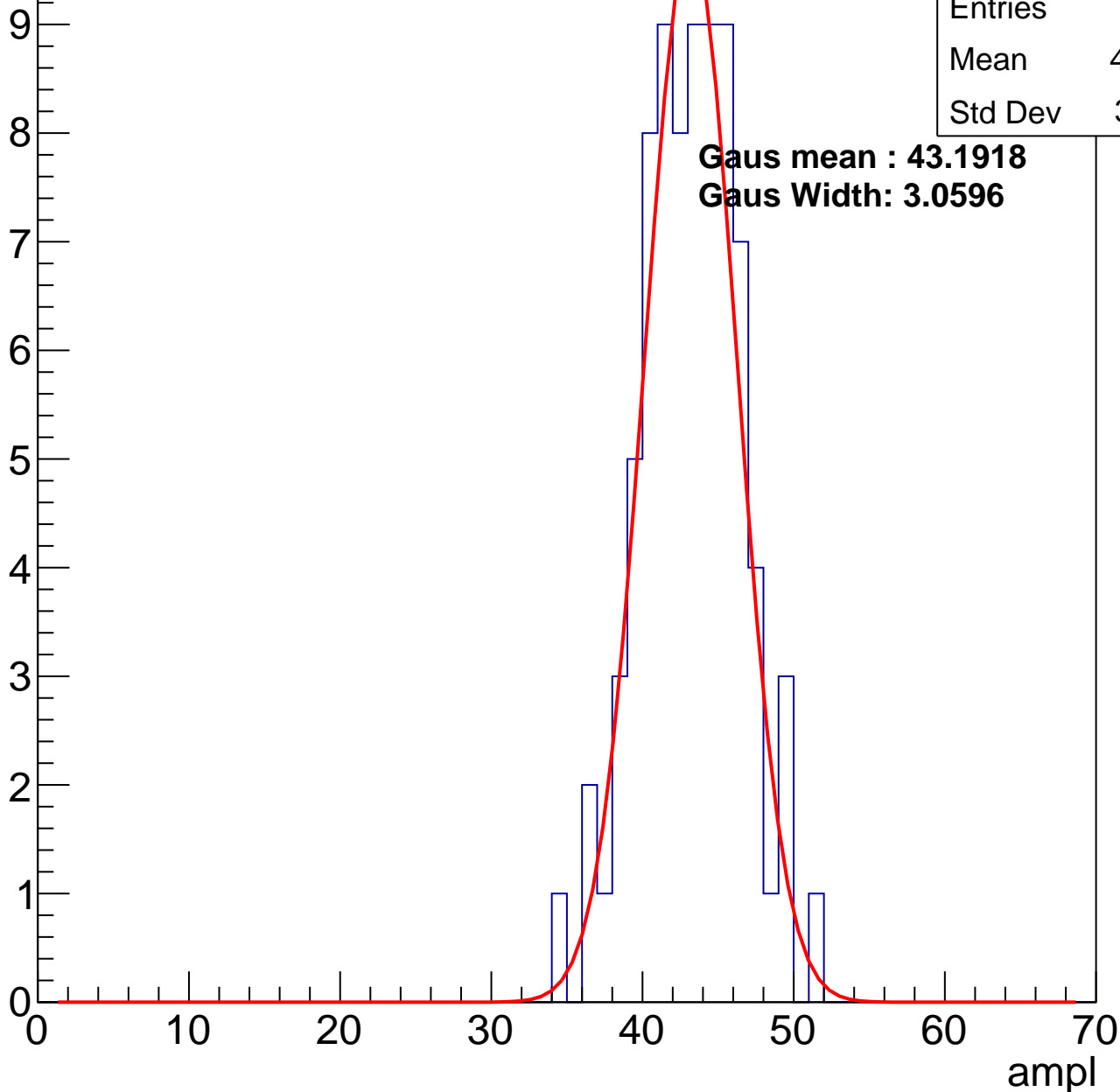
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	80
Mean	42.76
Std Dev	3.261

**Gaus mean : 43.1918**

**Gaus Width: 3.0596**

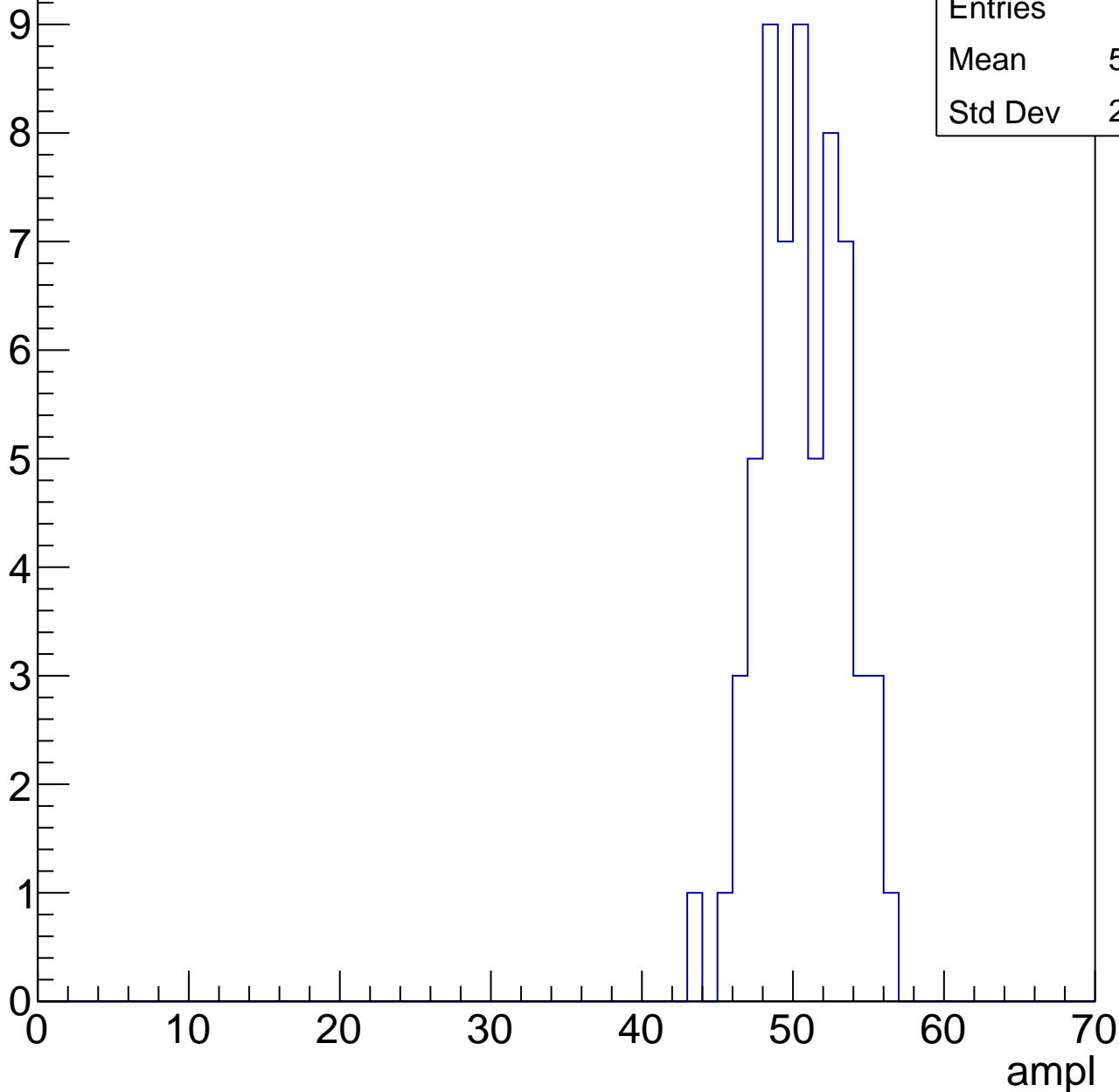


# B1L003S, U26-ch0, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	50.18
Std Dev	2.745

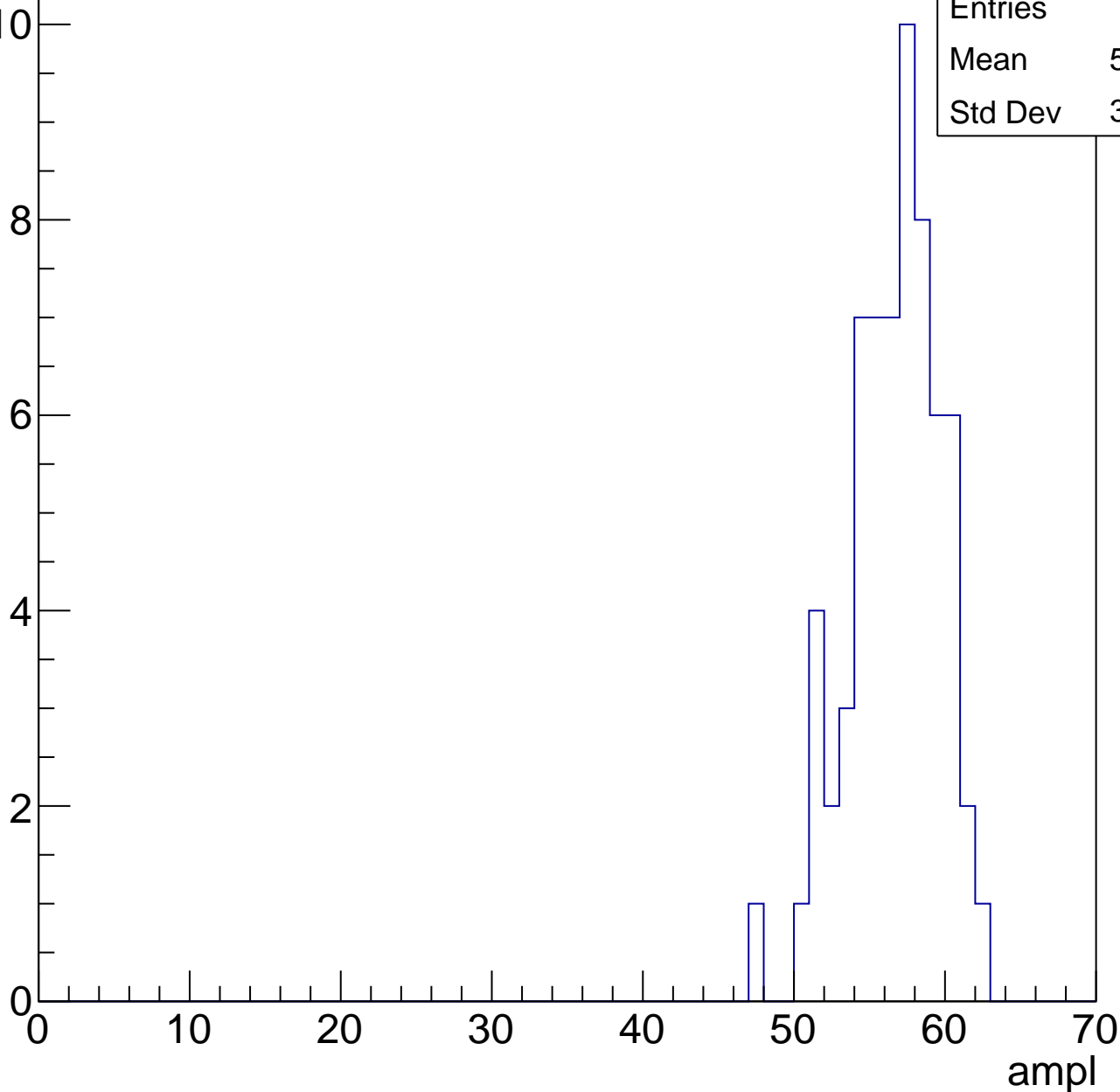


# B1L003S, U26-ch0, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	56.17
Std Dev	3.005

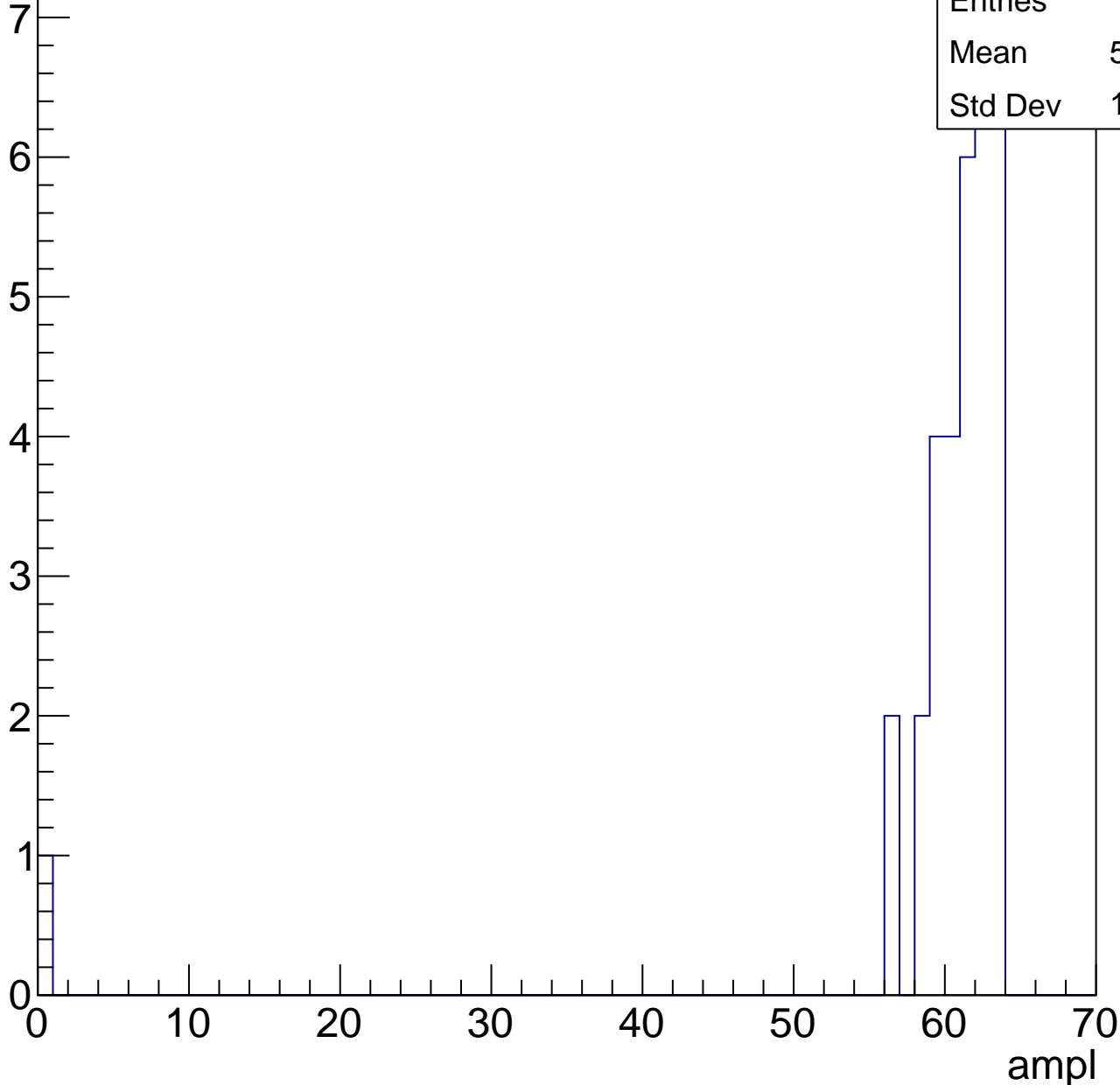


# B1L003S, U26-ch0, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	33
Mean	58.94
Std Dev	10.59



# B1L003S, U26-ch0, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

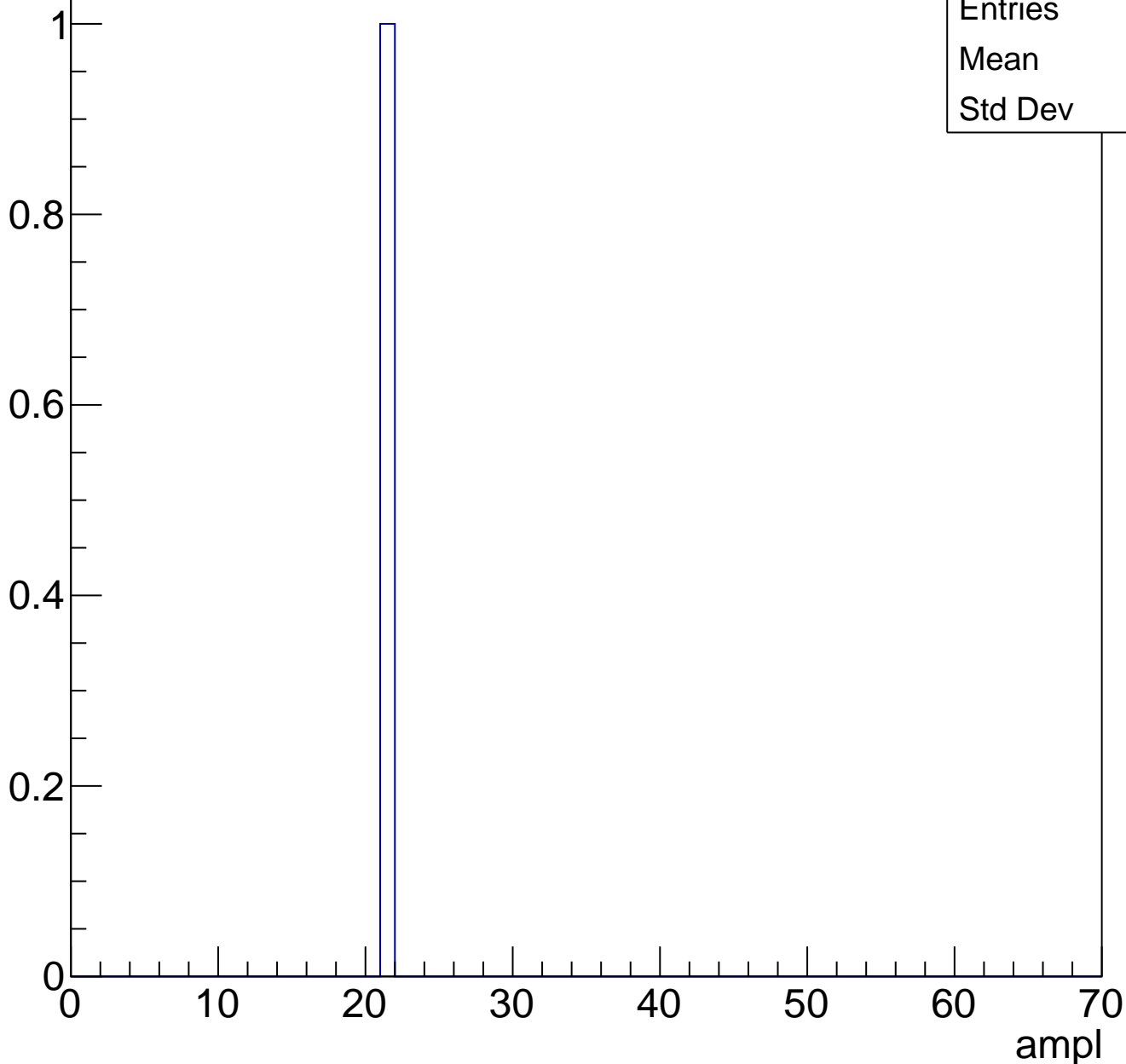




# B1L003S, U26-ch0, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U26-ch1, adc0

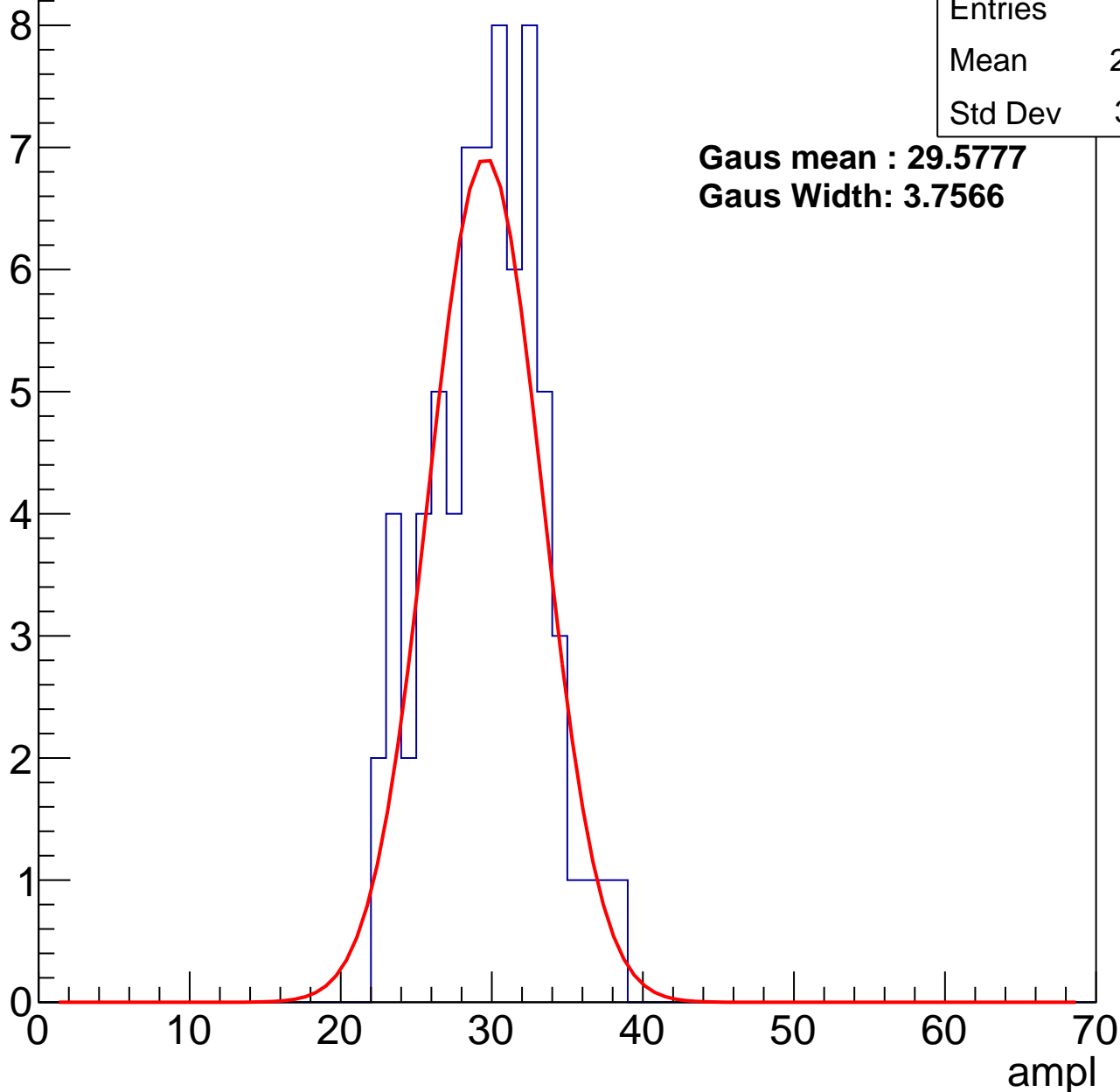
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	29.22
Std Dev	3.631

**Gaus mean : 29.5777**

**Gaus Width: 3.7566**



# B1L003S, U26-ch1, adc1

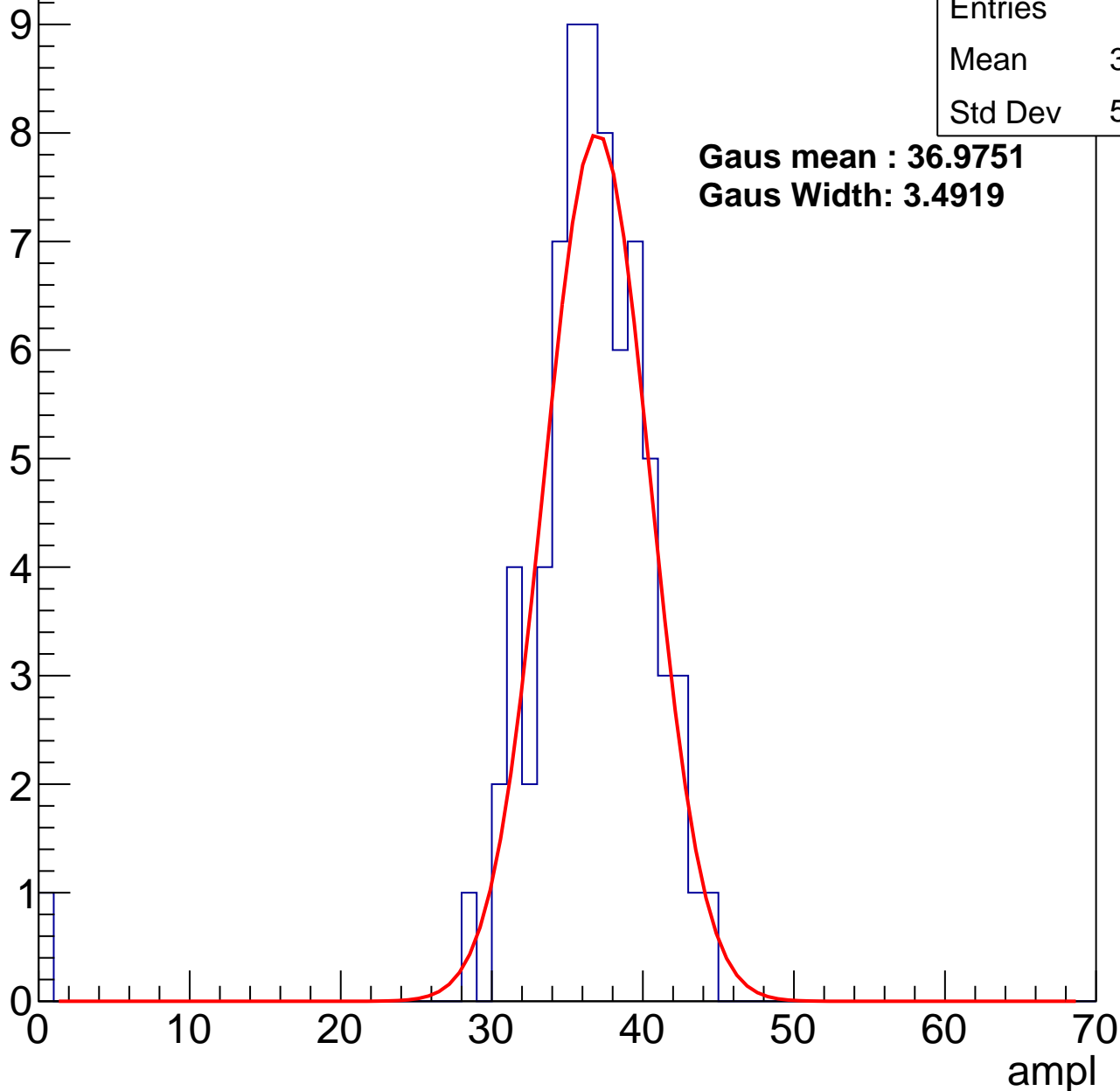
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	73
Mean	35.86
Std Dev	5.372

**Gaus mean : 36.9751**

**Gaus Width: 3.4919**



# B1L003S, U26-ch1, adc2

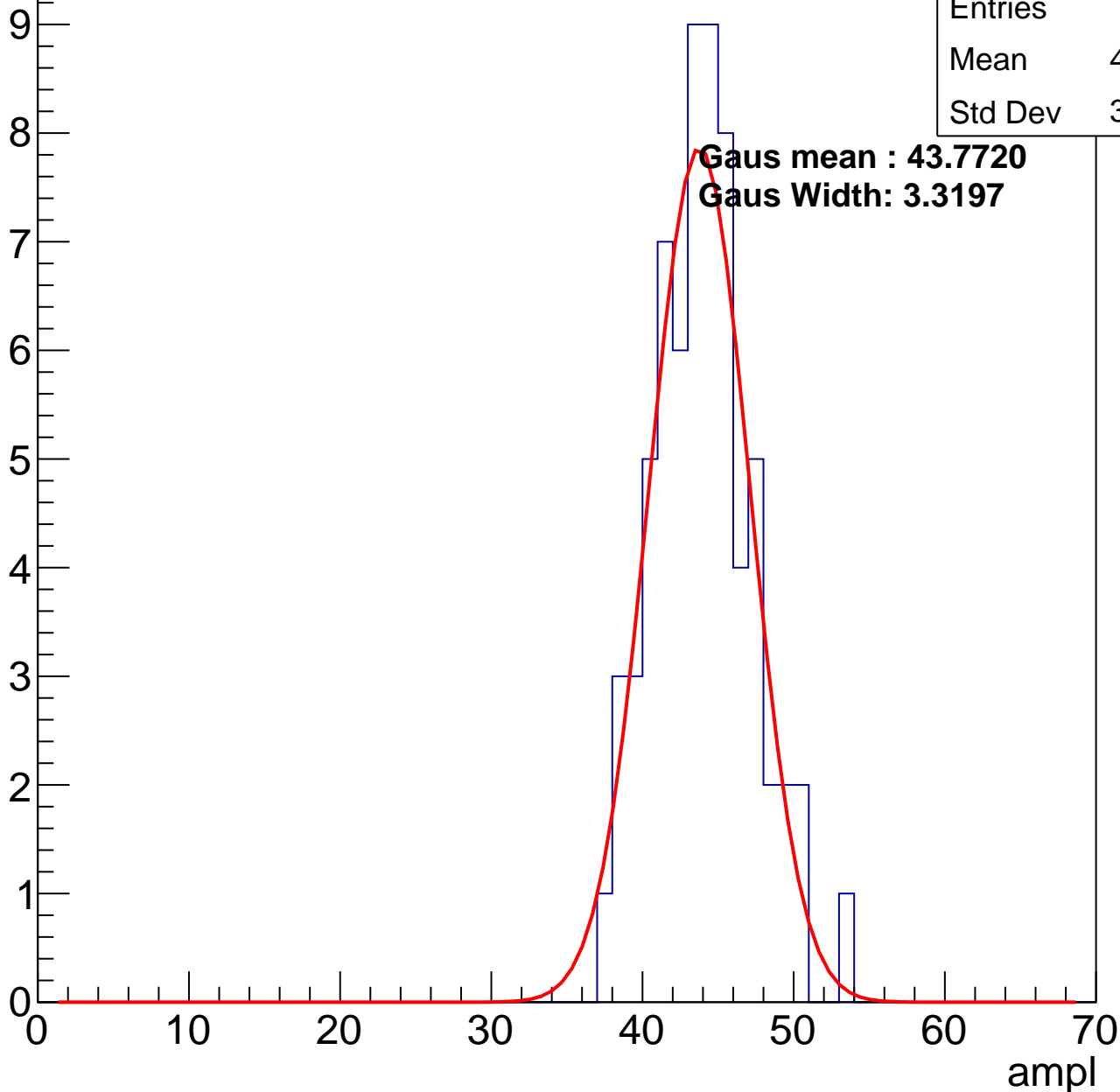
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	43.52
Std Dev	3.225

**Gaus mean : 43.7720**

**Gaus Width: 3.3197**

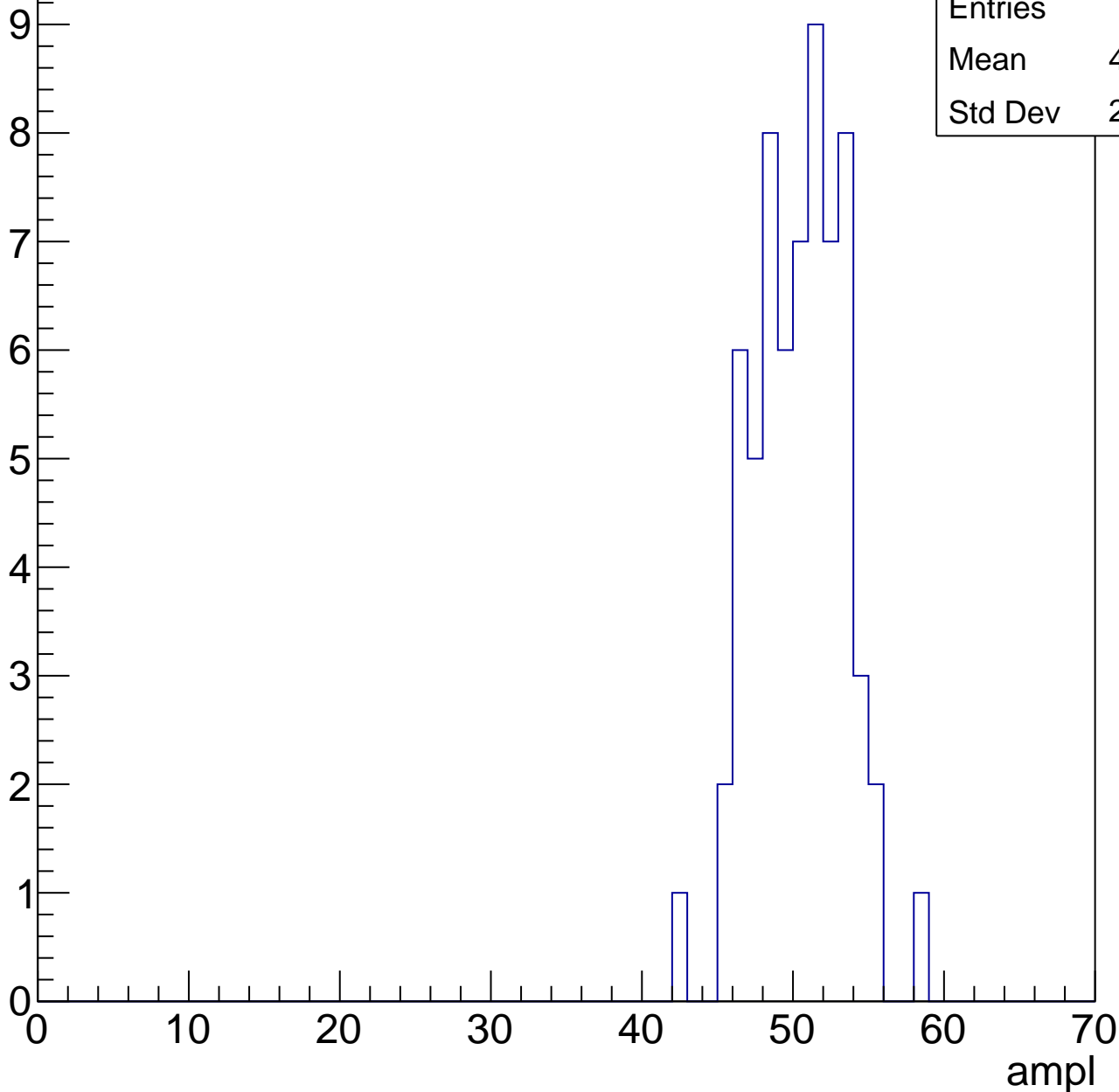


# B1L003S, U26-ch1, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	49.97
Std Dev	2.946

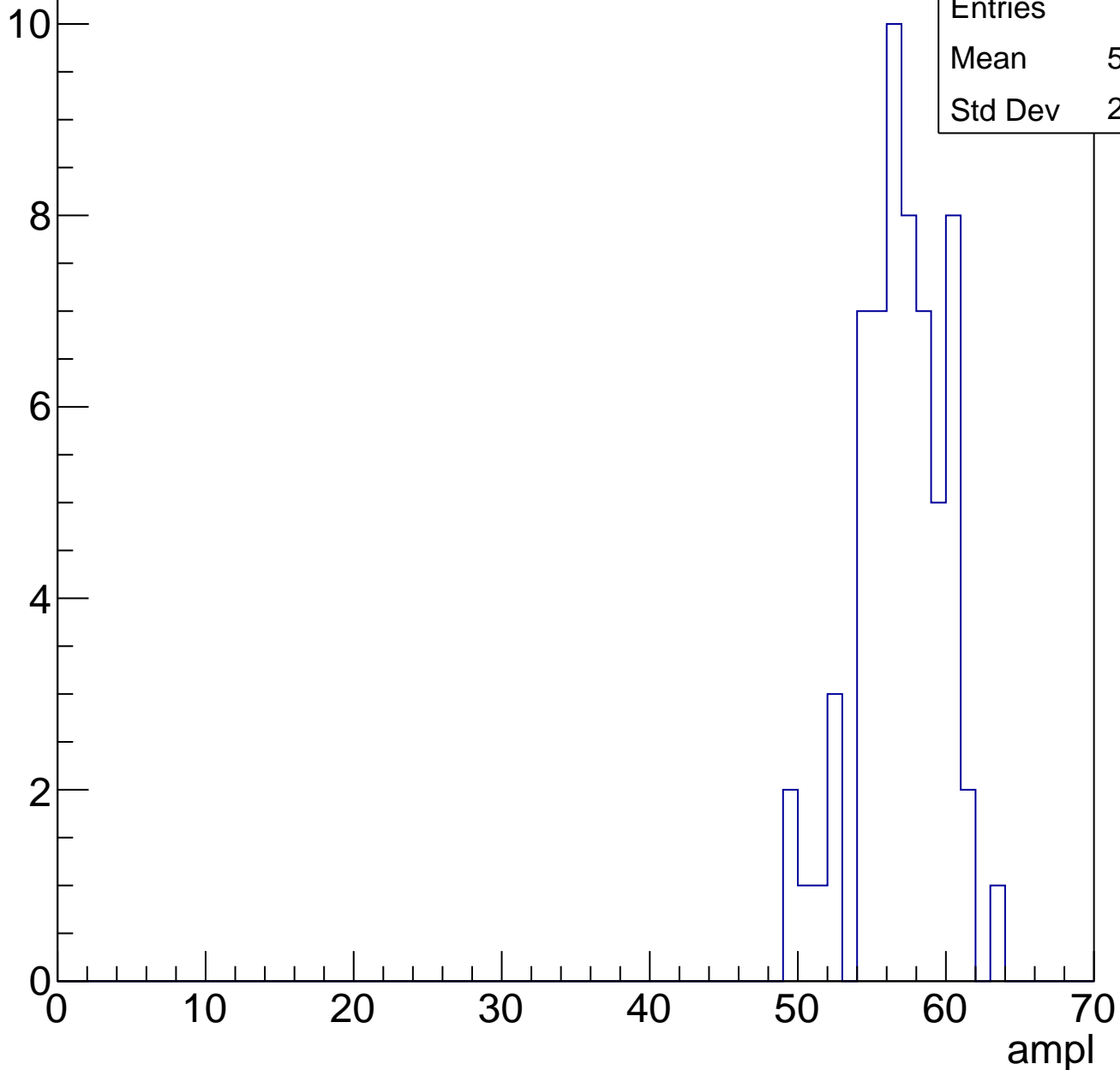


# B1L003S, U26-ch1, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	62
Mean	56.45
Std Dev	2.944

Entry

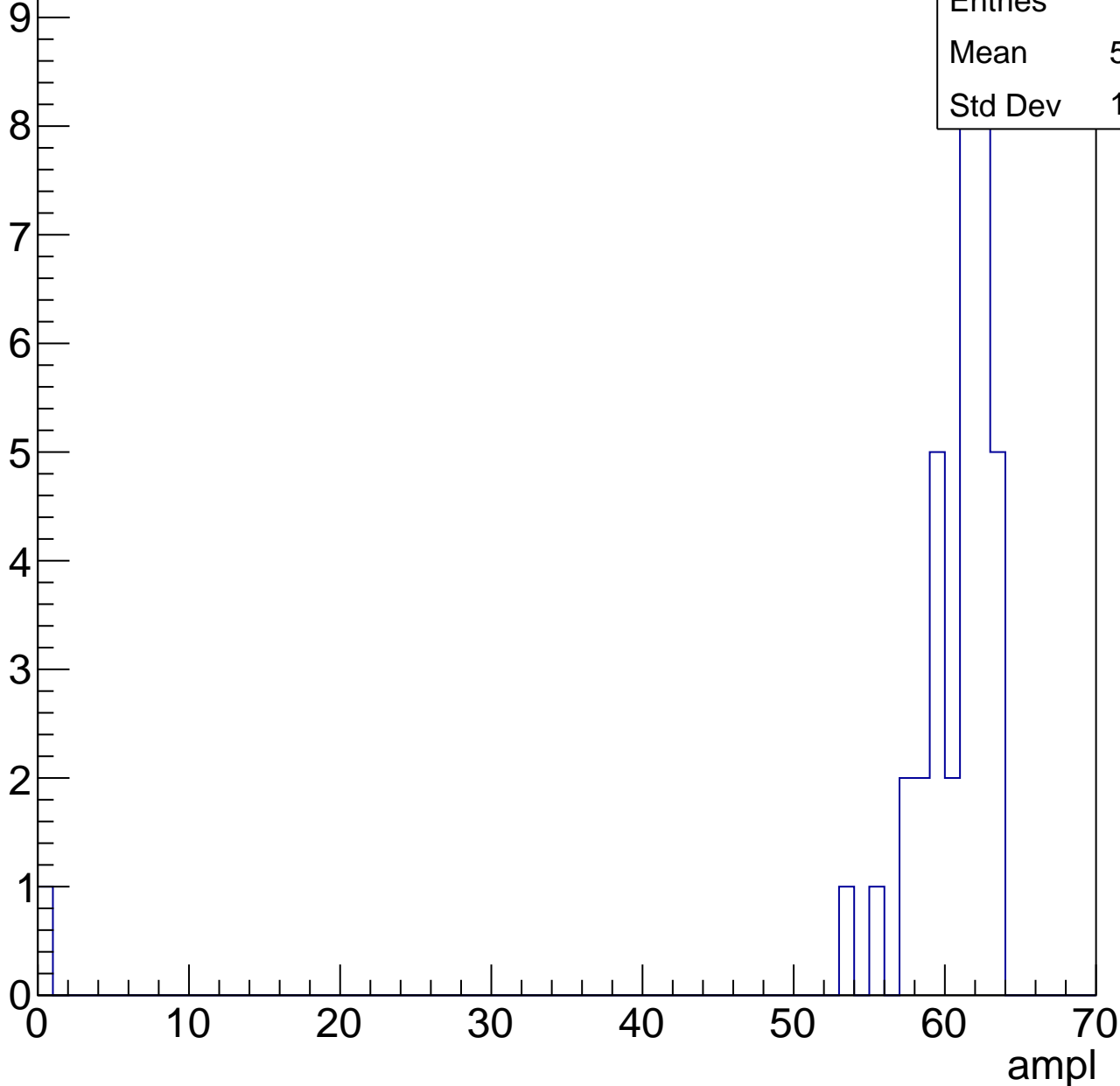


# B1L003S, U26-ch1, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

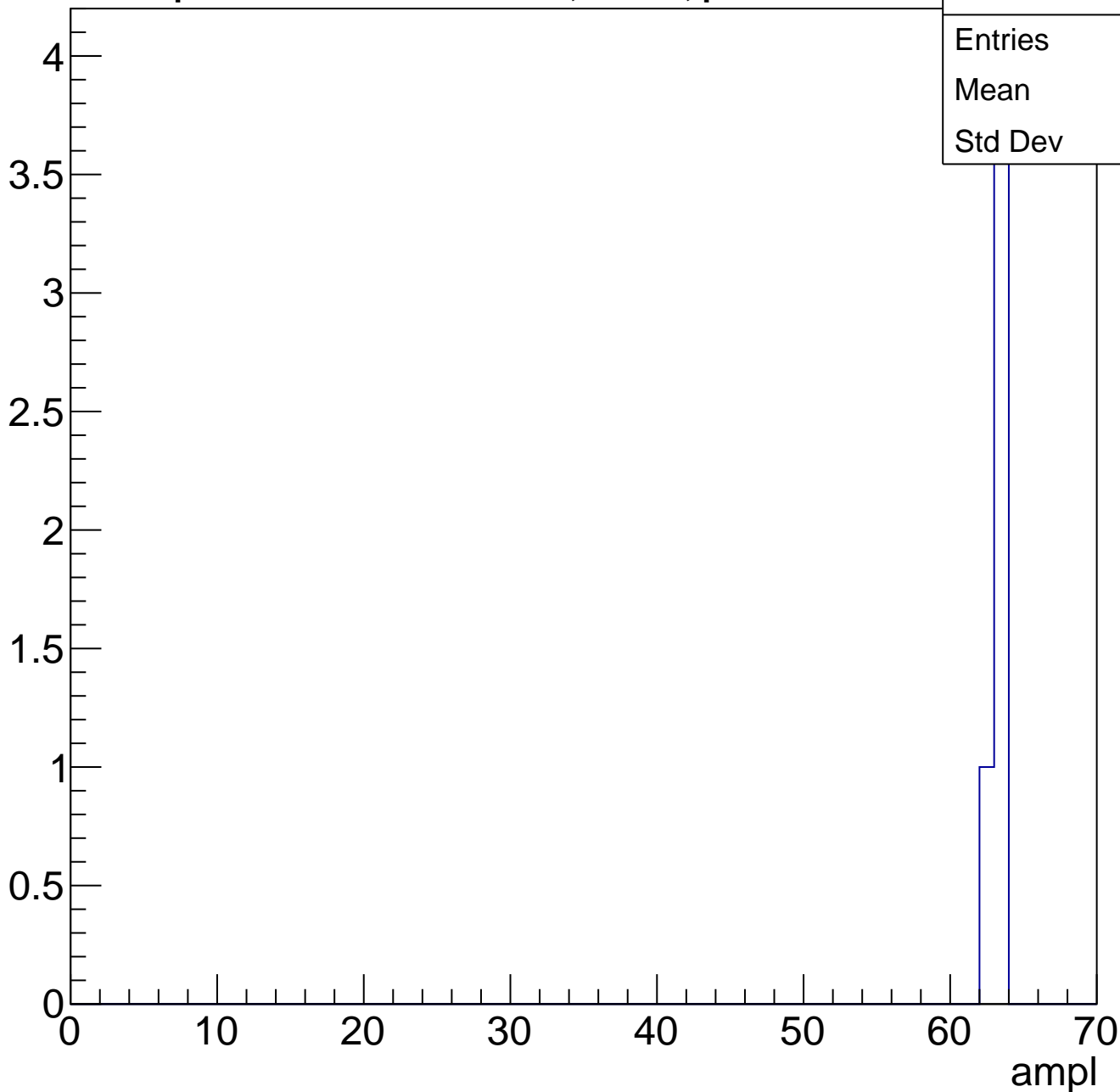
Entries	36
Mean	58.72
Std Dev	10.19



# B1L003S, U26-ch1, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch1, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L003S, U26-ch2, adc0

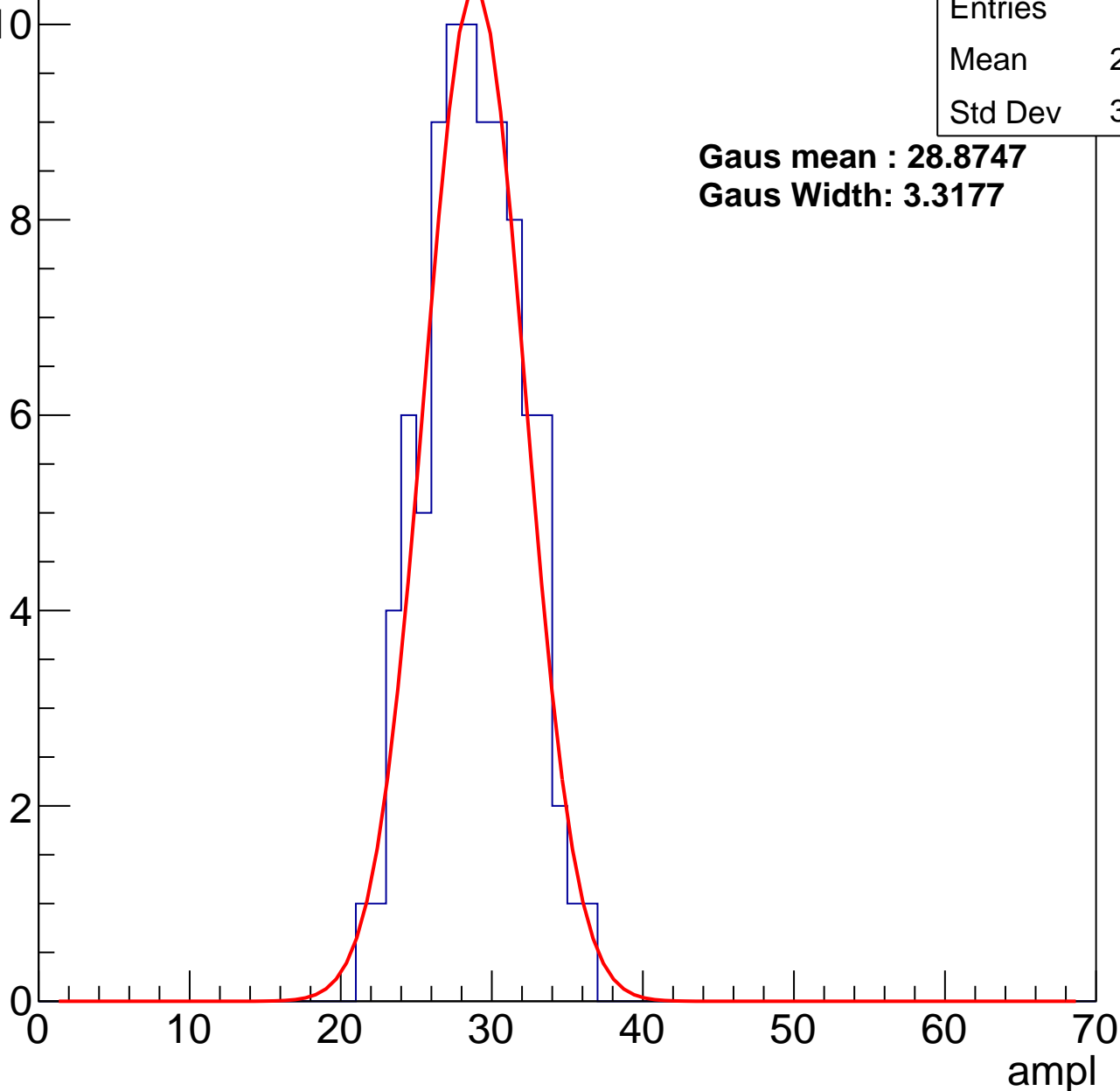
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	88
Mean	28.36
Std Dev	3.213

**Gaus mean : 28.8747**

**Gaus Width: 3.3177**



# B1L003S, U26-ch2, adc1

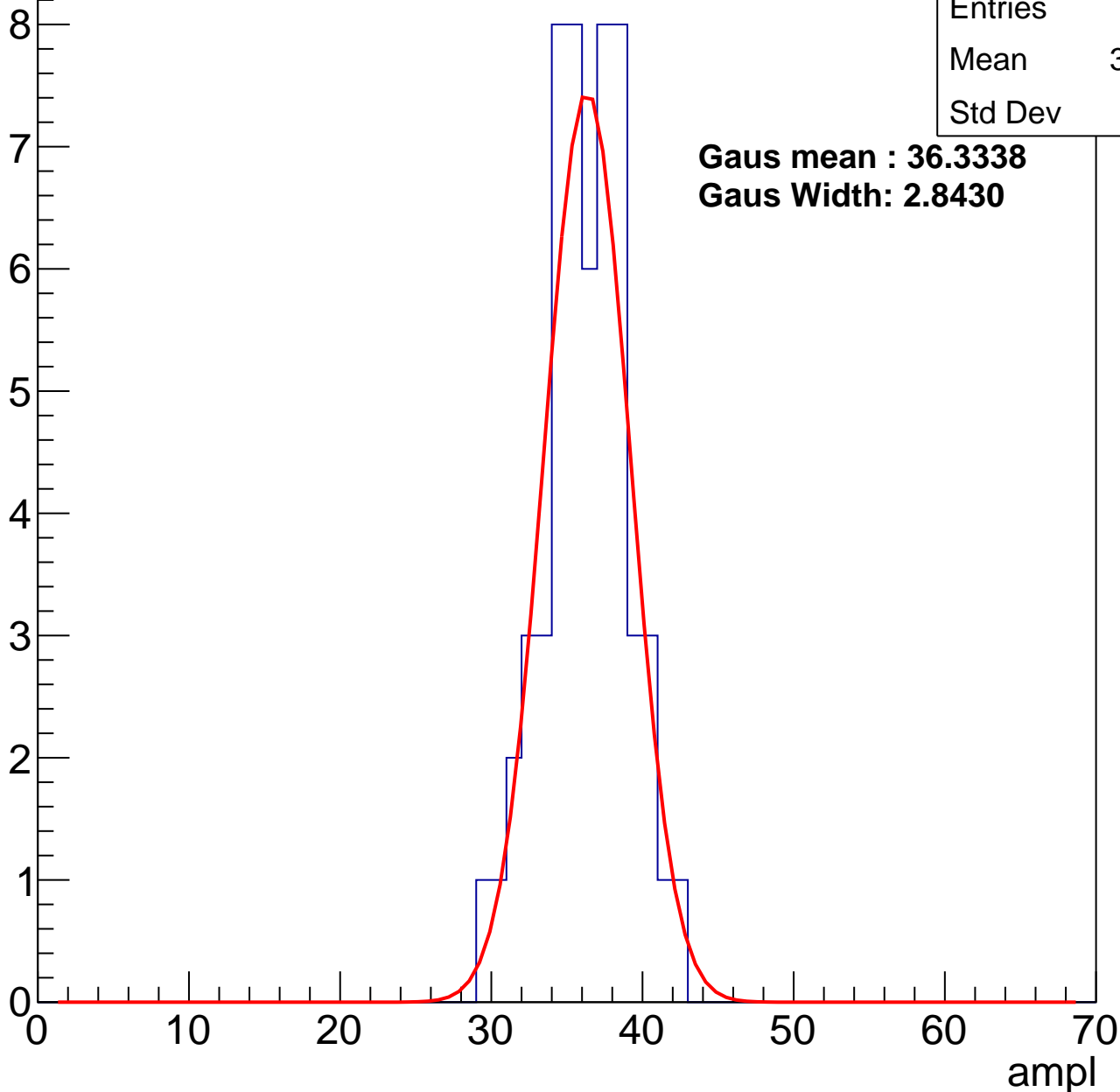
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	35.79
Std Dev	2.75

**Gaus mean : 36.3338**

**Gaus Width: 2.8430**



# B1L003S, U26-ch2, adc2

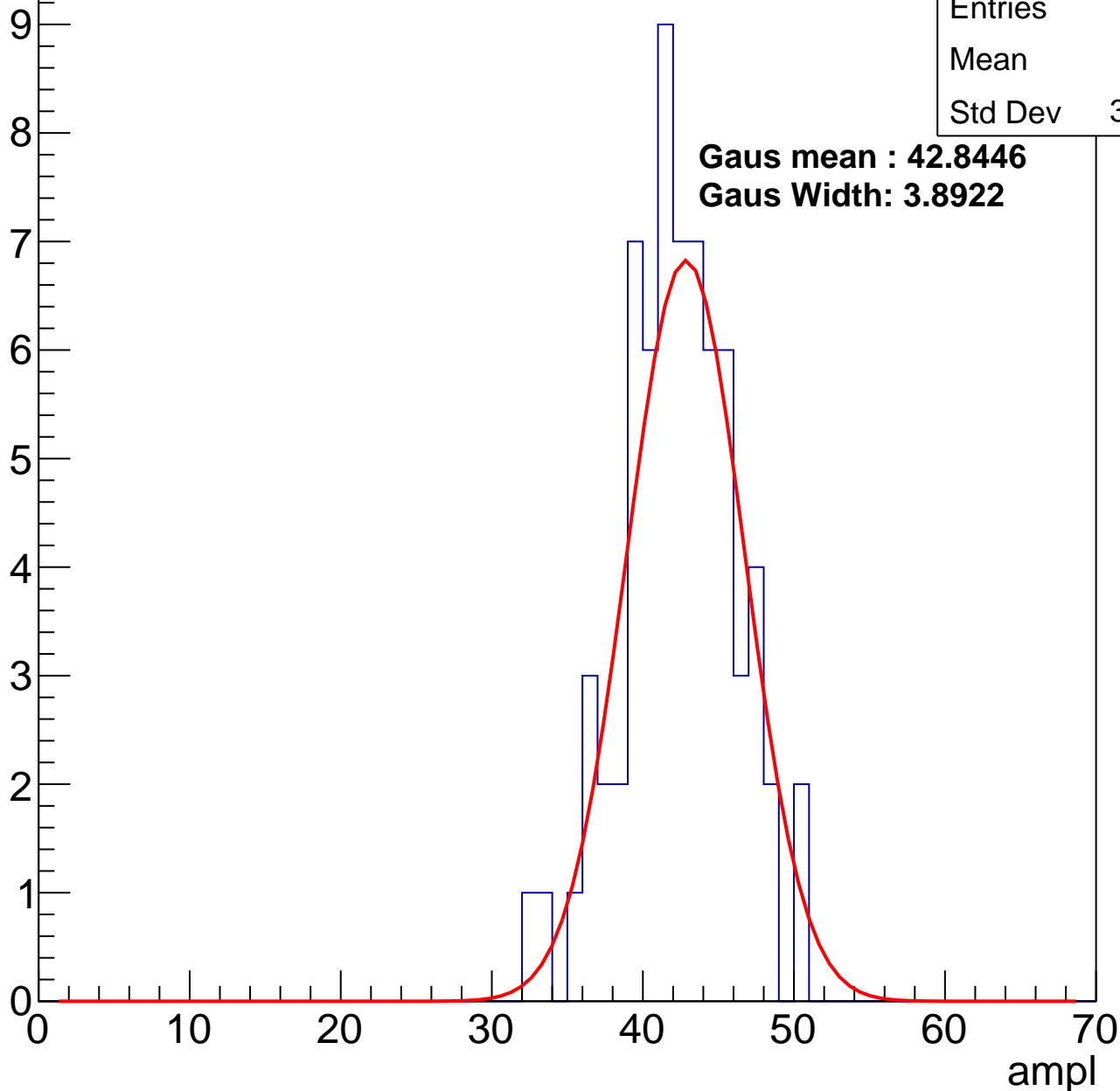
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	41.9
Std Dev	3.707

**Gaus mean : 42.8446**

**Gaus Width: 3.8922**

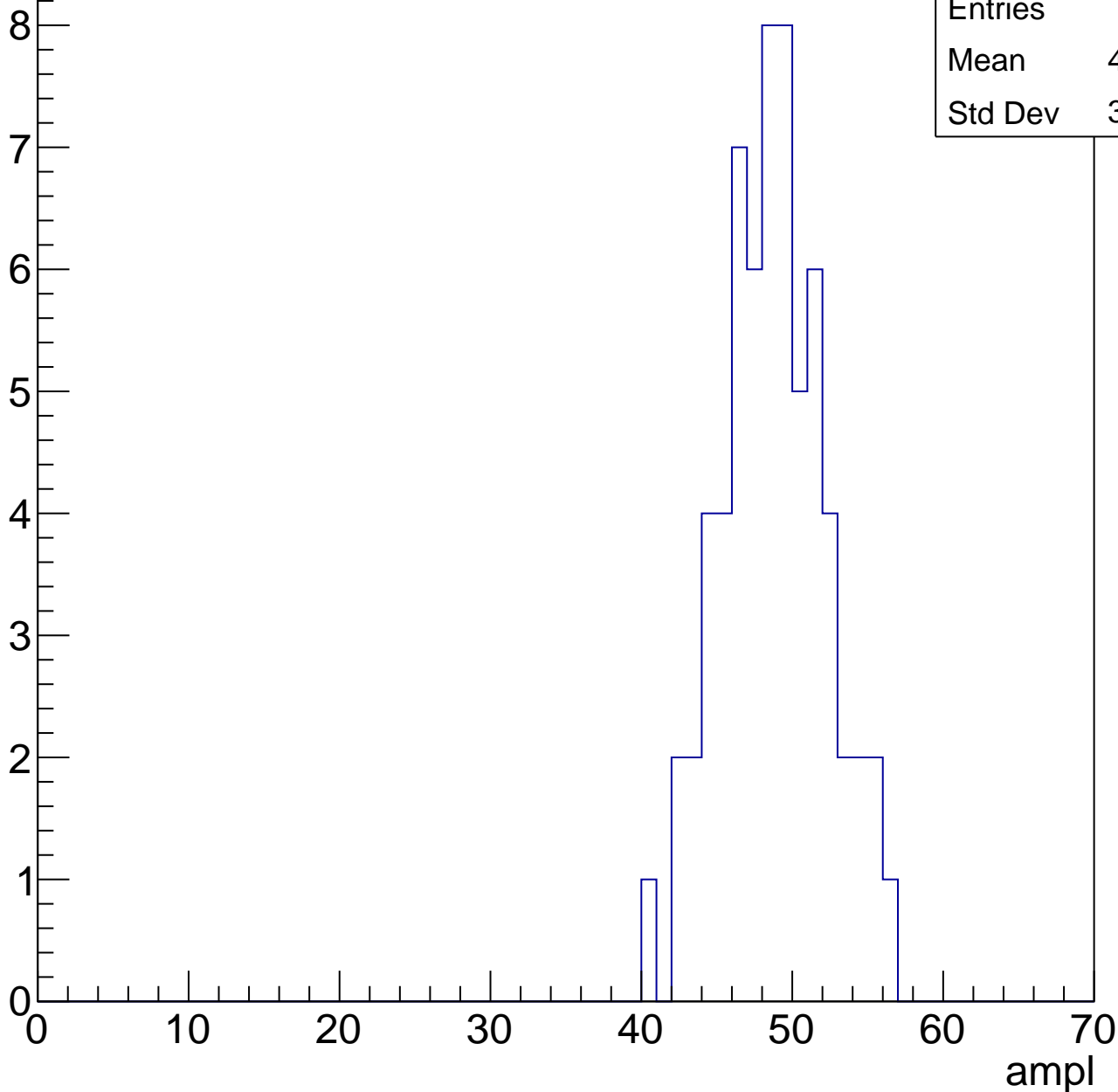


# B1L003S, U26-ch2, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	48.28
Std Dev	3.412

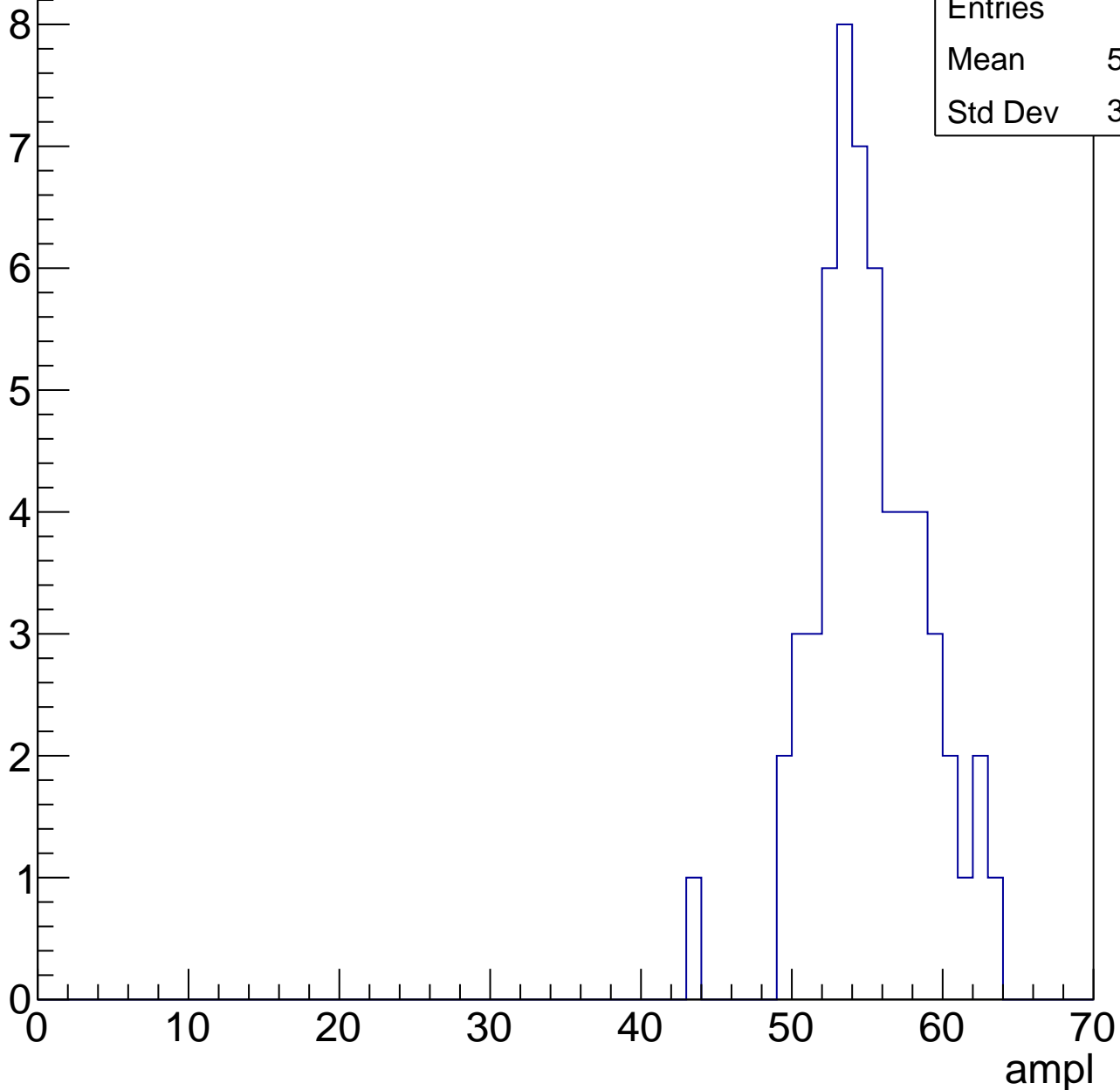


# B1L003S, U26-ch2, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	54.68
Std Dev	3.695

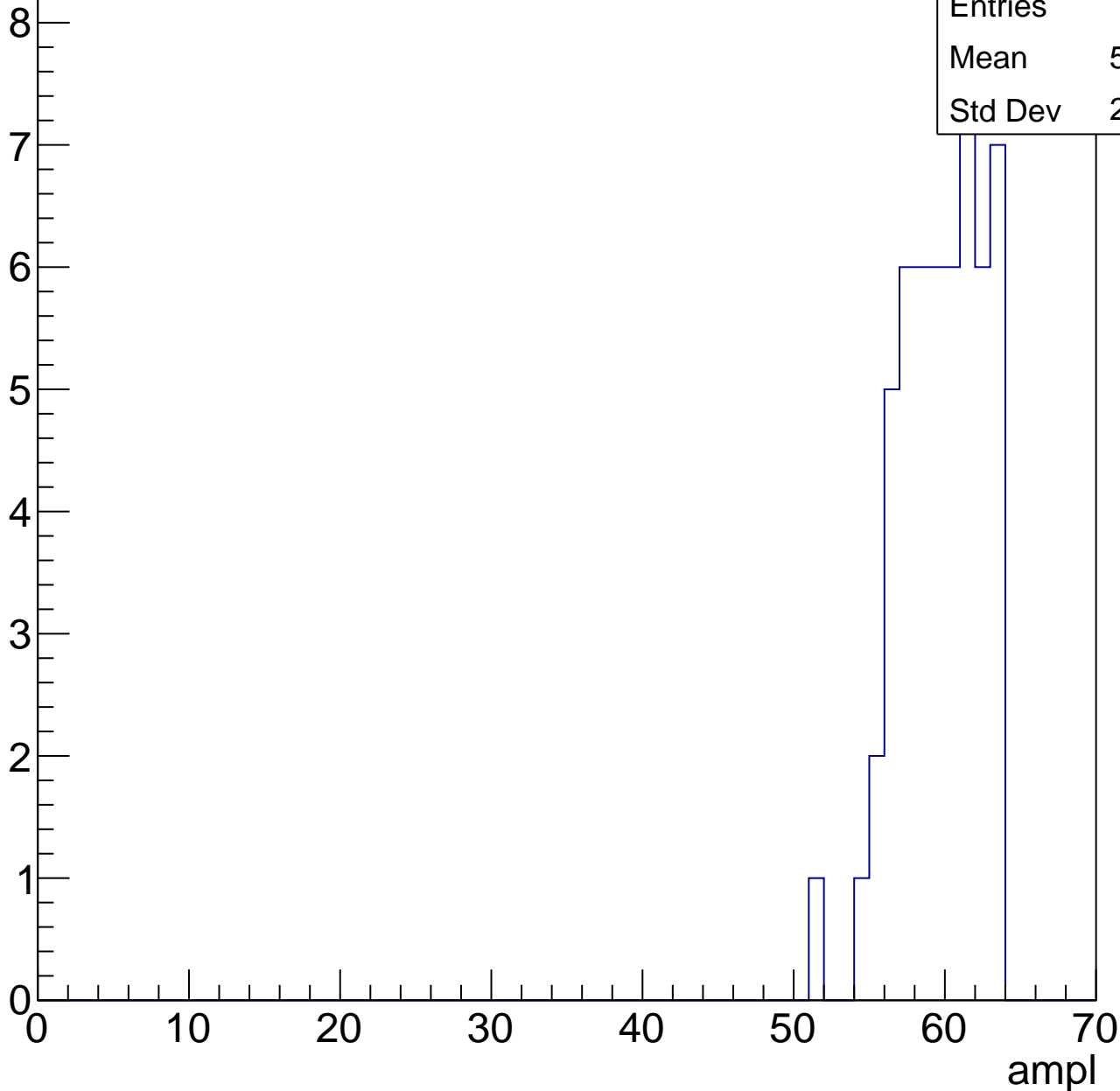


# B1L003S, U26-ch2, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	54
Mean	59.26
Std Dev	2.709



# B1L003S, U26-ch2, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	9
Mean	54.44
Std Dev	19.29

ampl

0 10 20 30 40 50 60 70



# B1L003S, U26-ch2, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U26-ch3, adc0

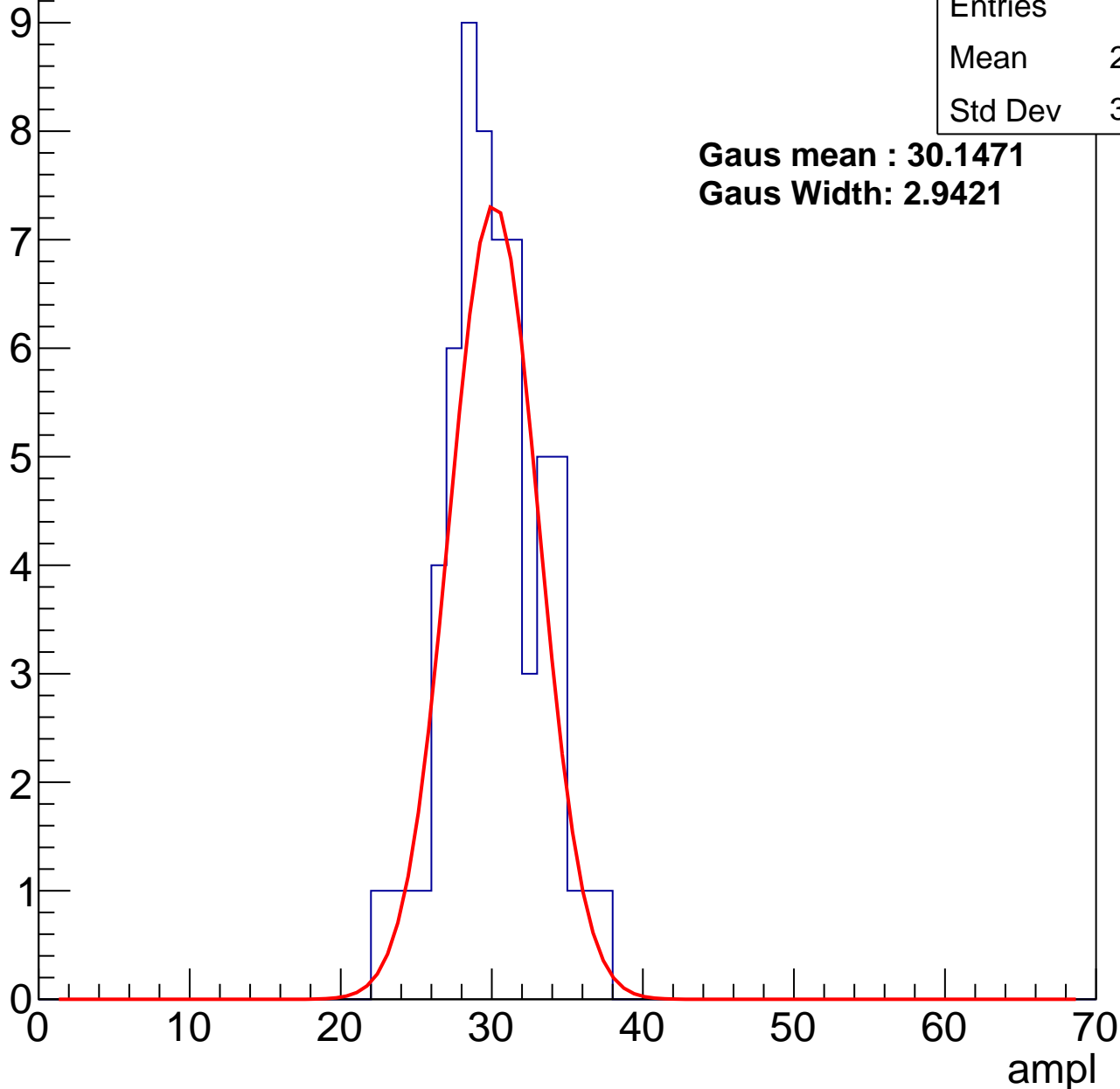
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	29.67
Std Dev	3.093

**Gaus mean : 30.1471**

**Gaus Width: 2.9421**



# B1L003S, U26-ch3, adc1

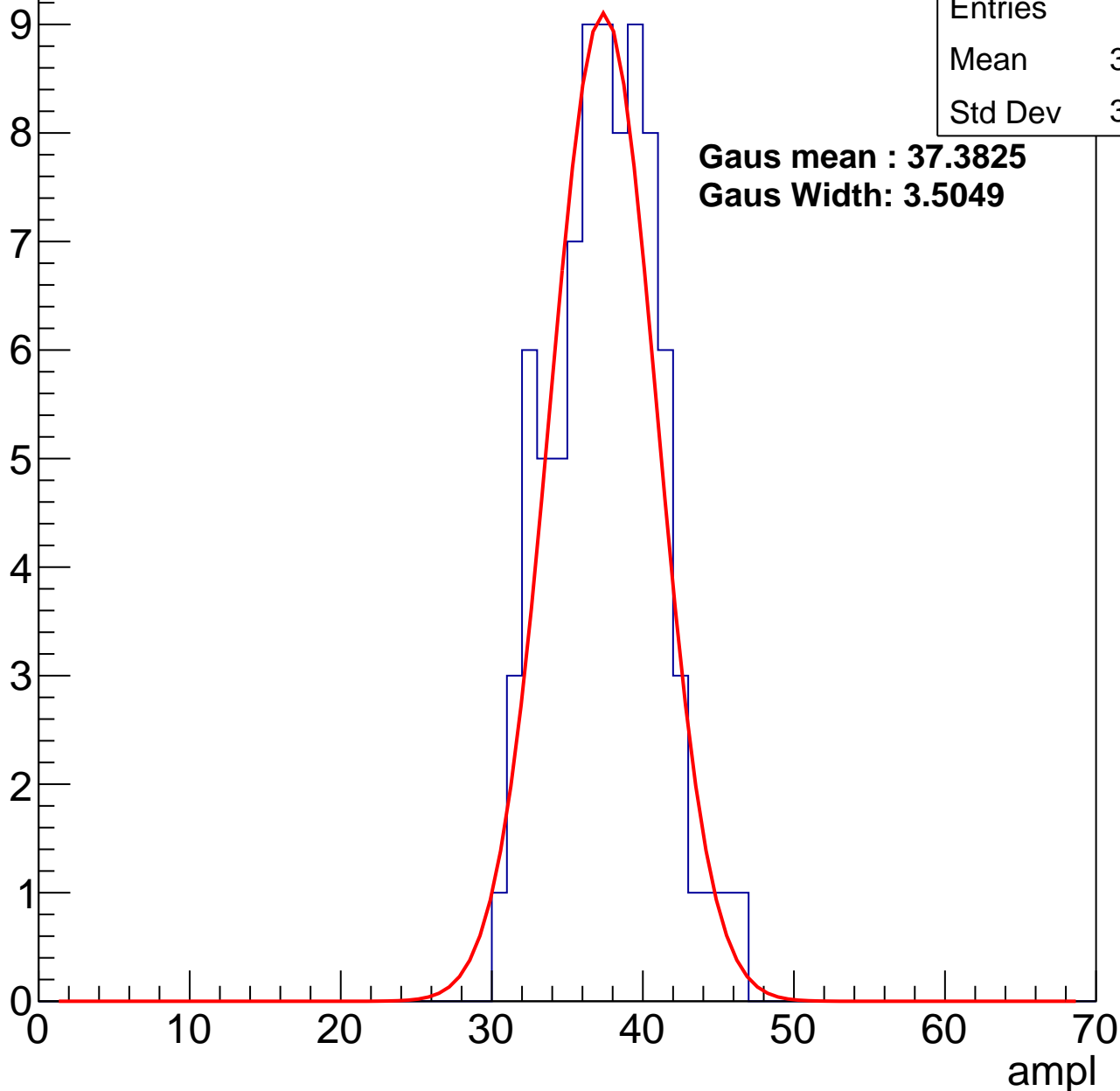
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	83
Mean	37.07
Std Dev	3.446

**Gaus mean : 37.3825**

**Gaus Width: 3.5049**



# B1L003S, U26-ch3, adc2

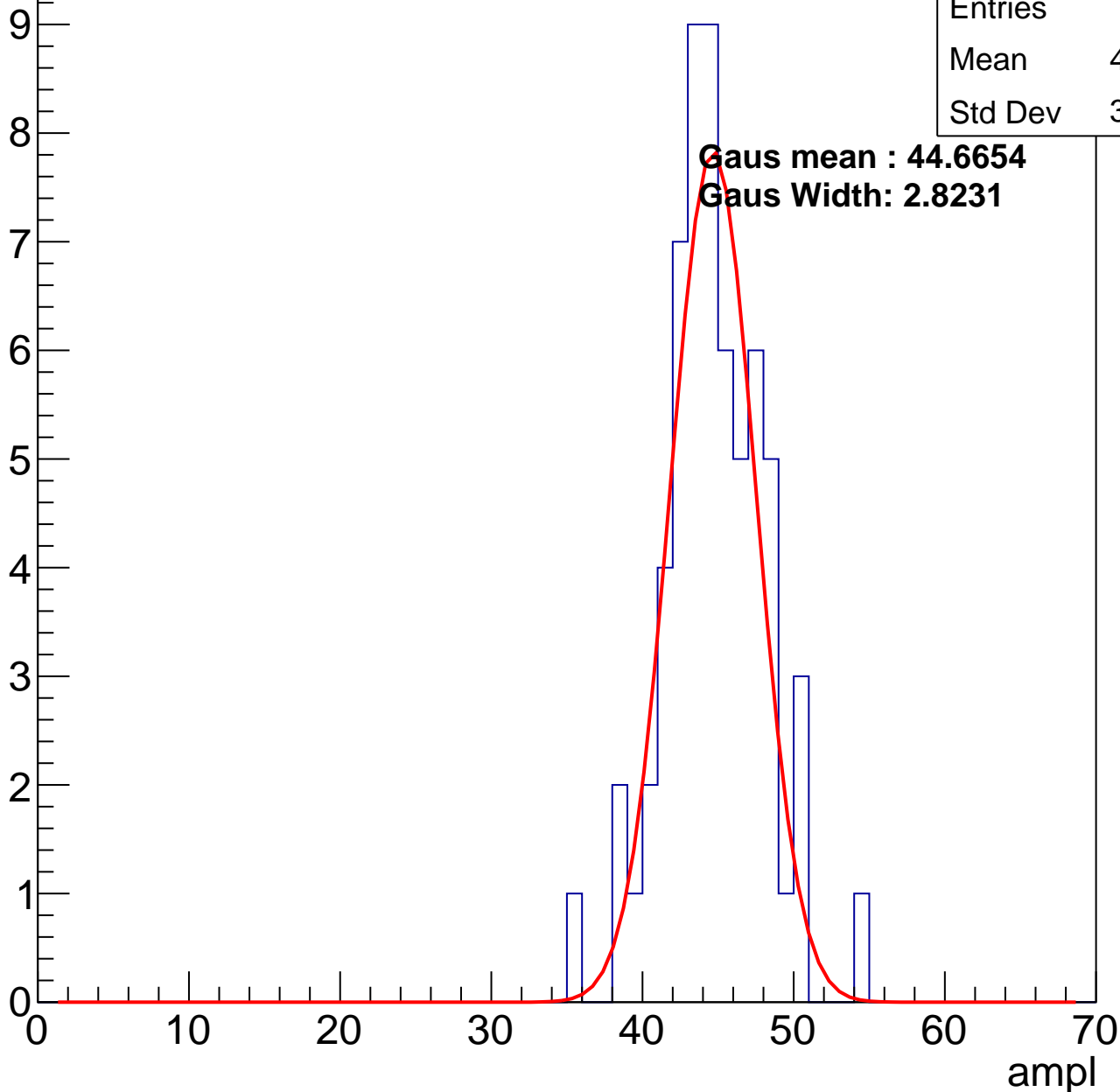
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	44.29
Std Dev	3.289

**Gaus mean : 44.6654**

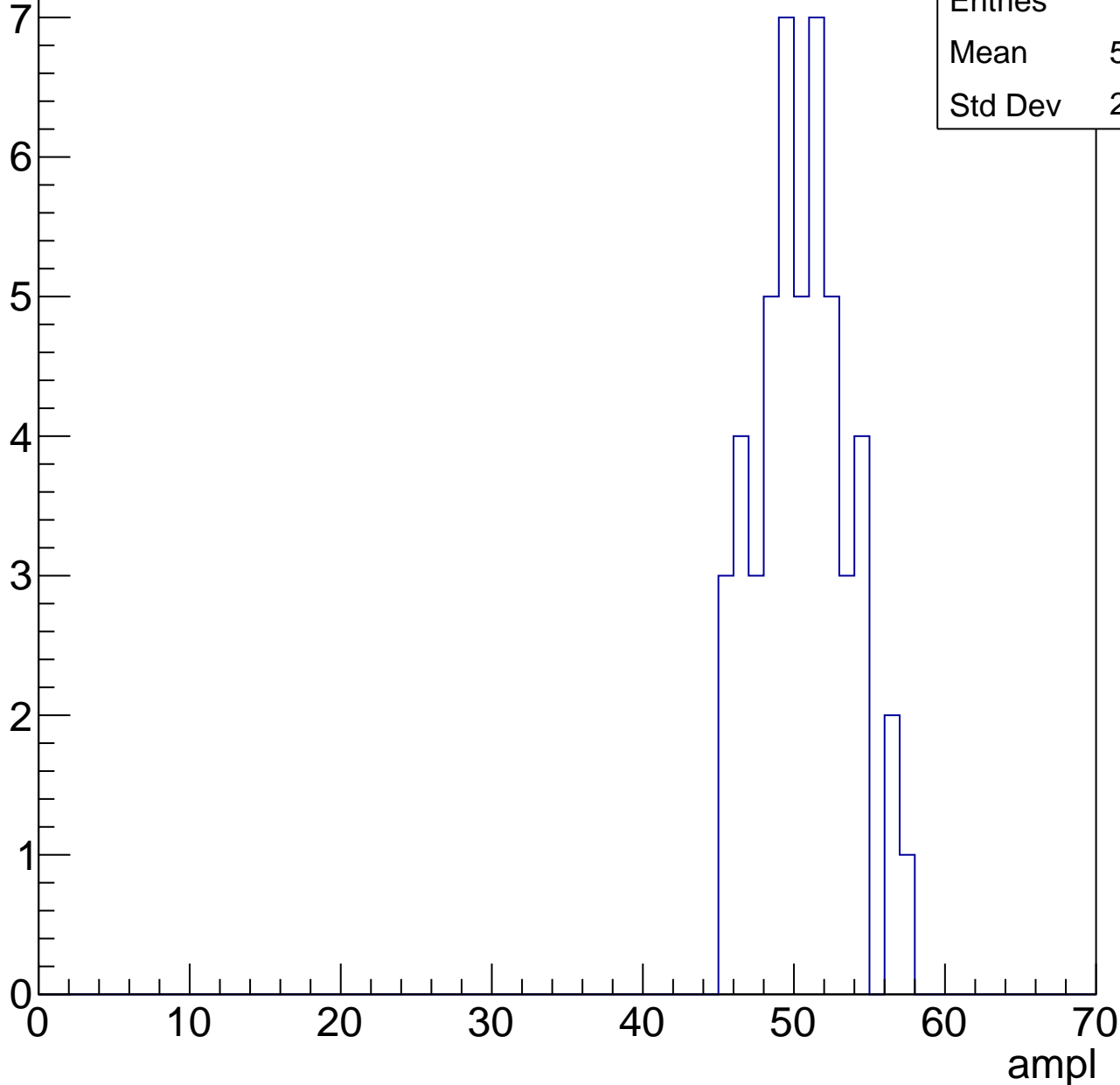
**Gaus Width: 2.8231**



# B1L003S, U26-ch3, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

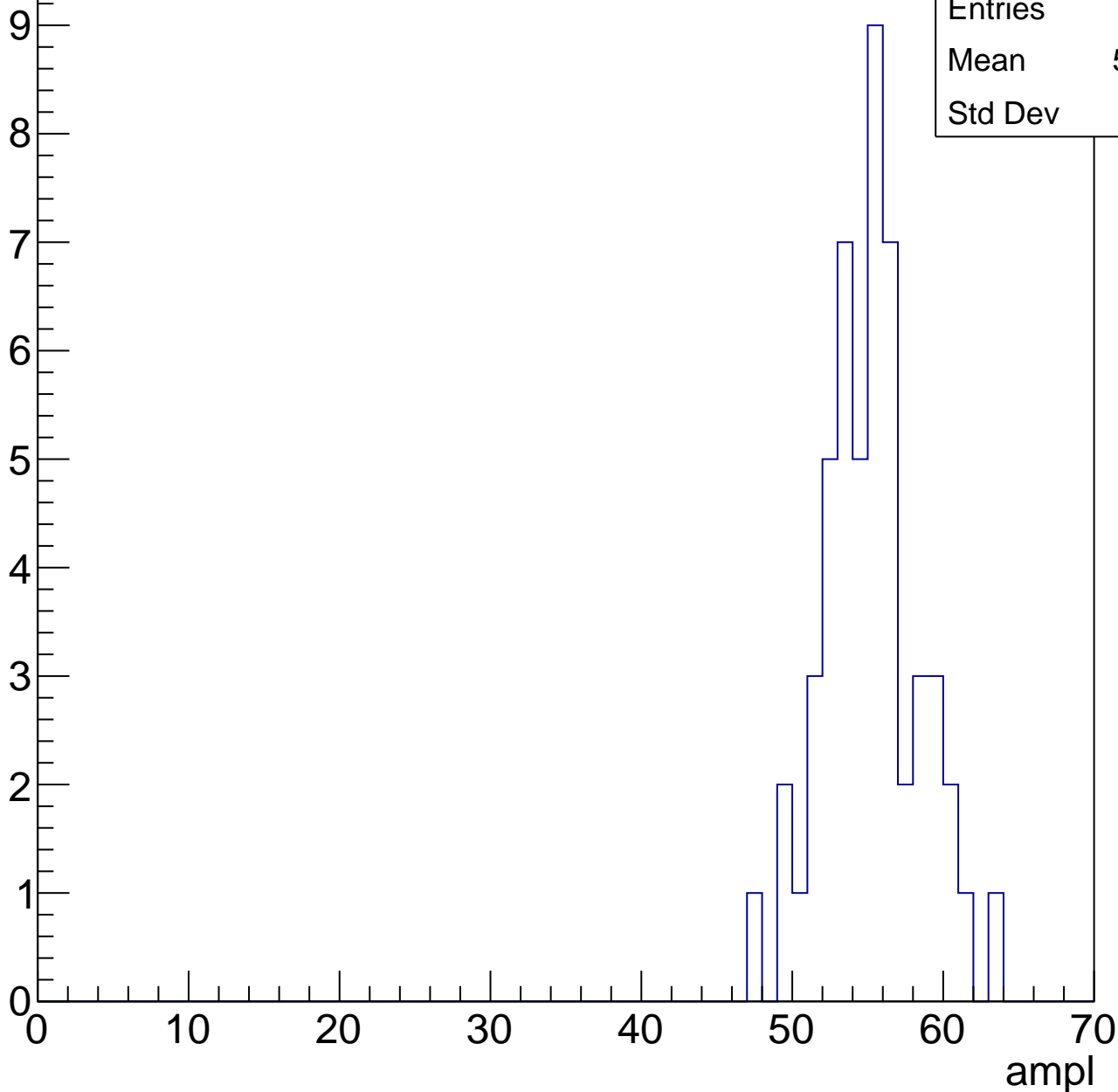


# B1L003S, U26-ch3, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	52
Mean	54.71
Std Dev	3.17

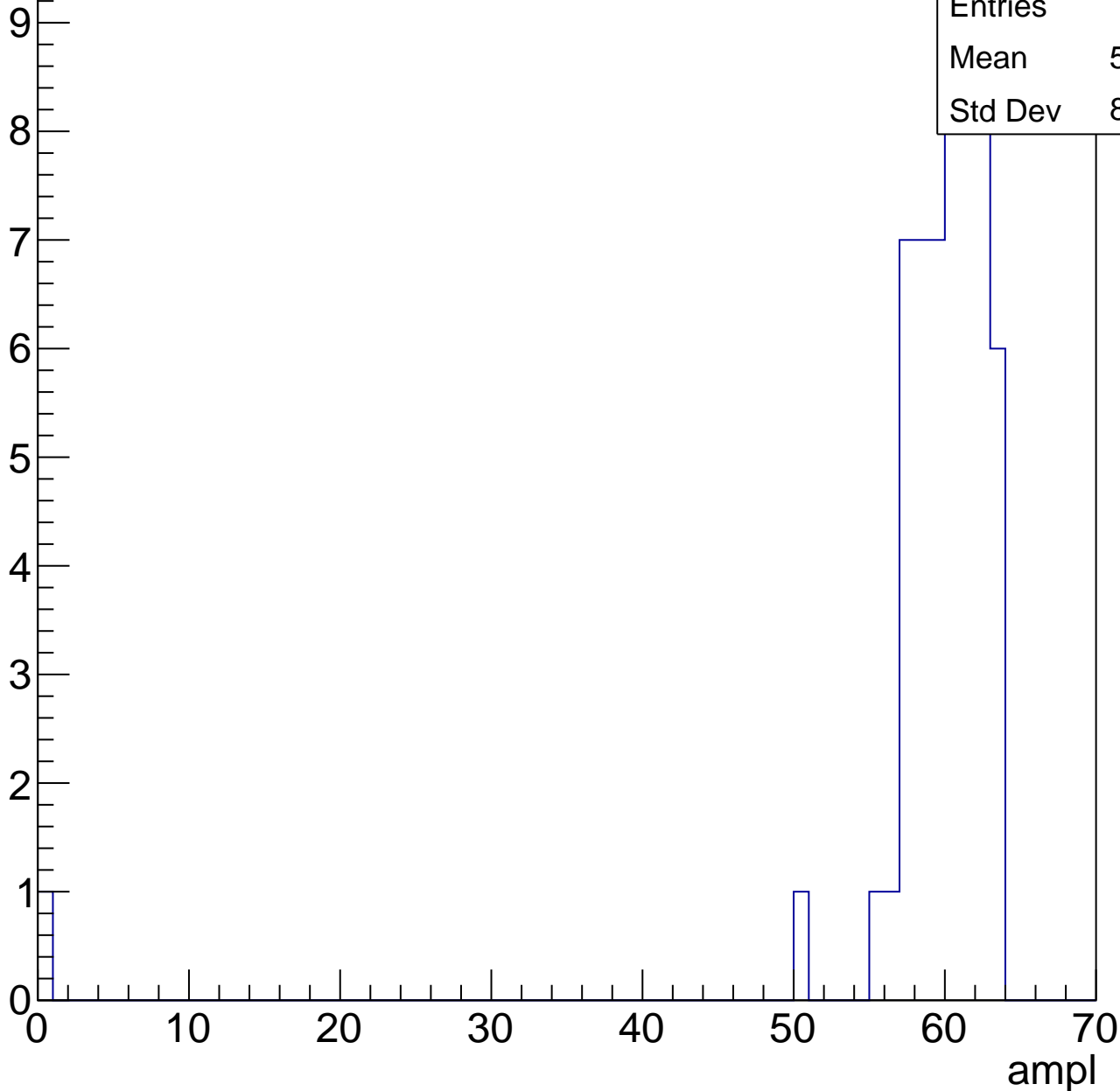


# B1L003S, U26-ch3, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	58.67
Std Dev	8.204



# B1L003S, U26-ch3, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	4
Mean	62.75
Std Dev	0.433



# B1L003S, U26-ch3, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U26-ch4, adc0

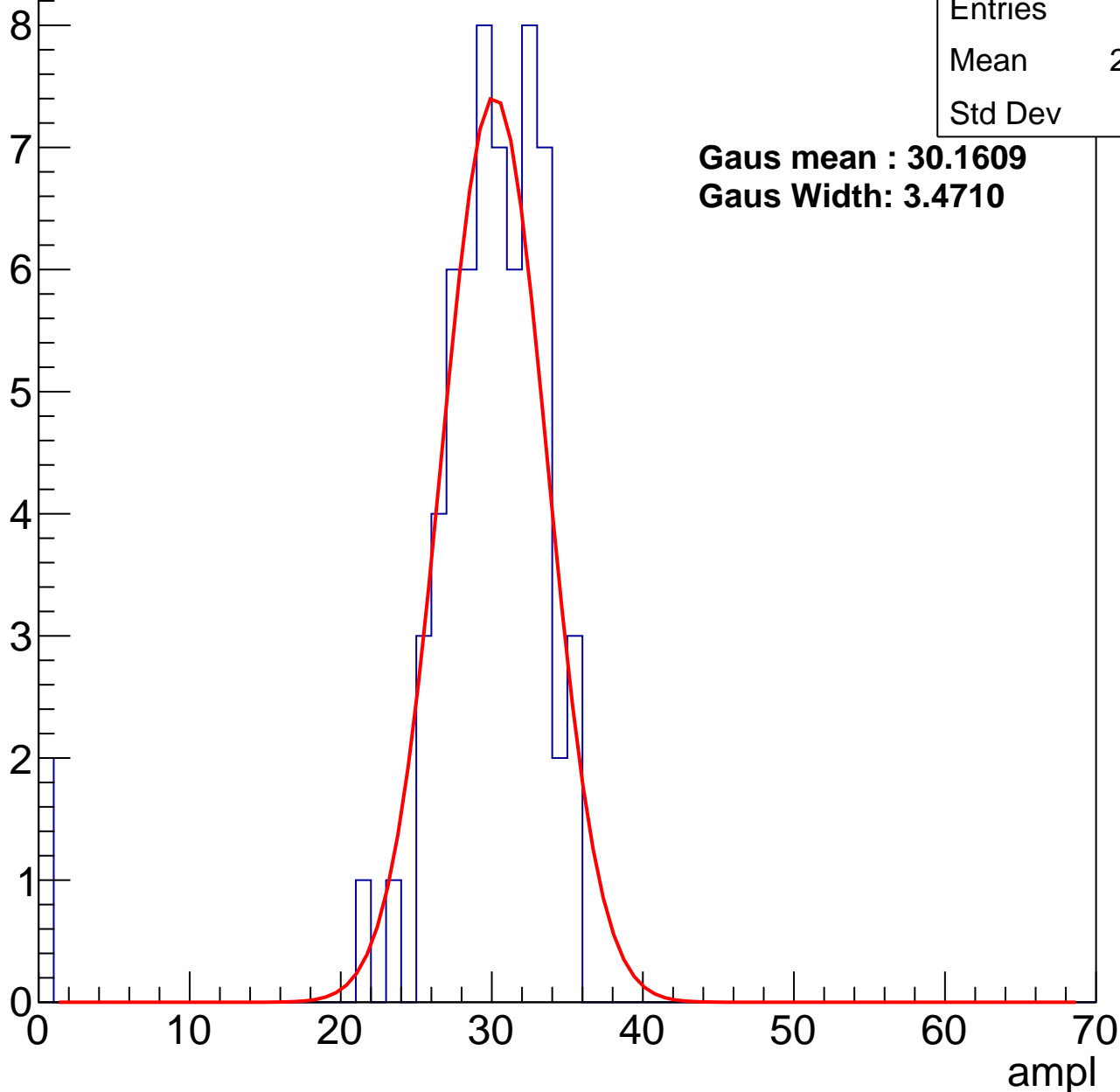
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	28.77
Std Dev	5.95

**Gaus mean : 30.1609**

**Gaus Width: 3.4710**



# B1L003S, U26-ch4, adc1

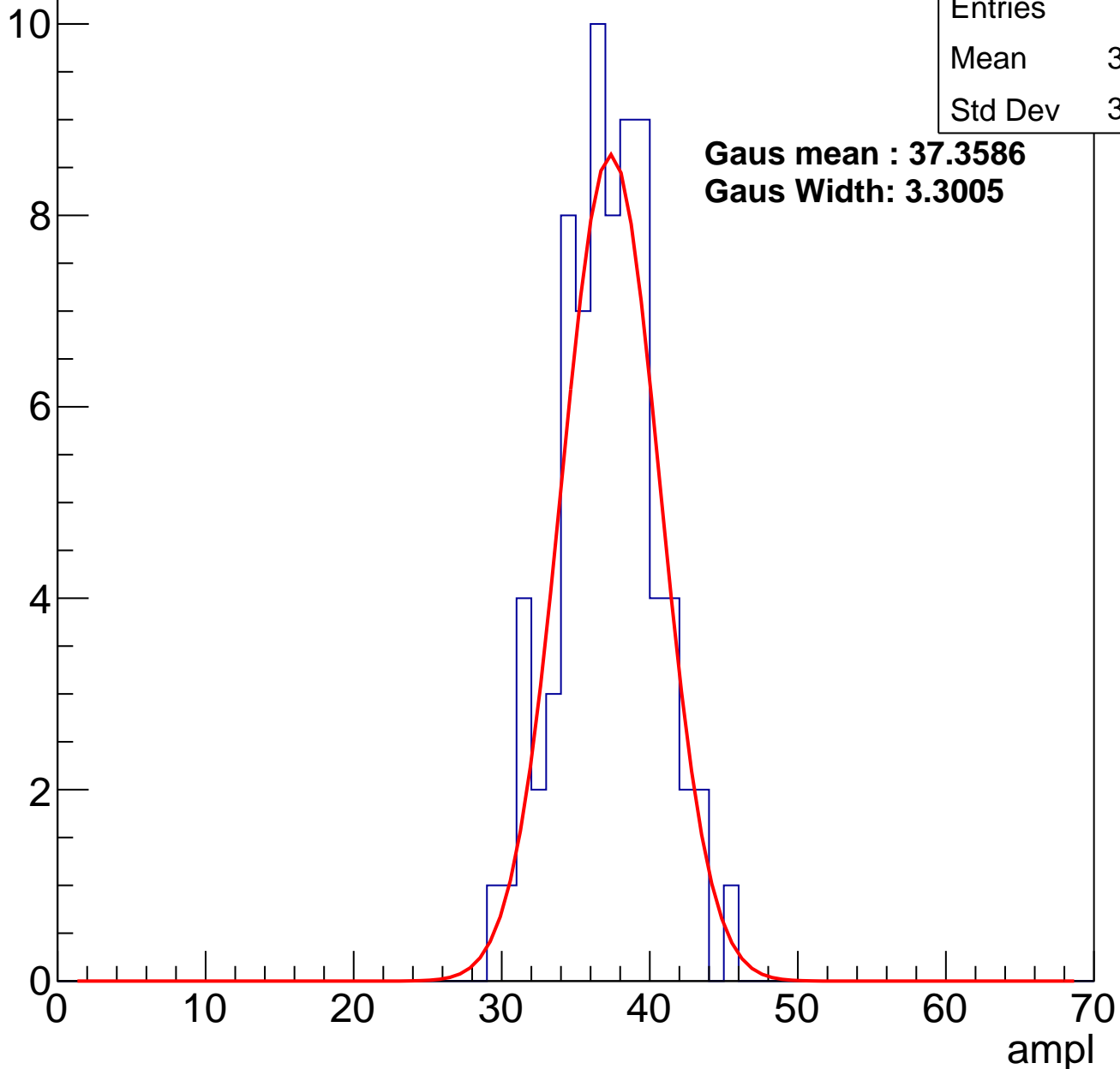
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	75
Mean	36.68
Std Dev	3.242

**Gaus mean : 37.3586**

**Gaus Width: 3.3005**

Entry



# B1L003S, U26-ch4, adc2

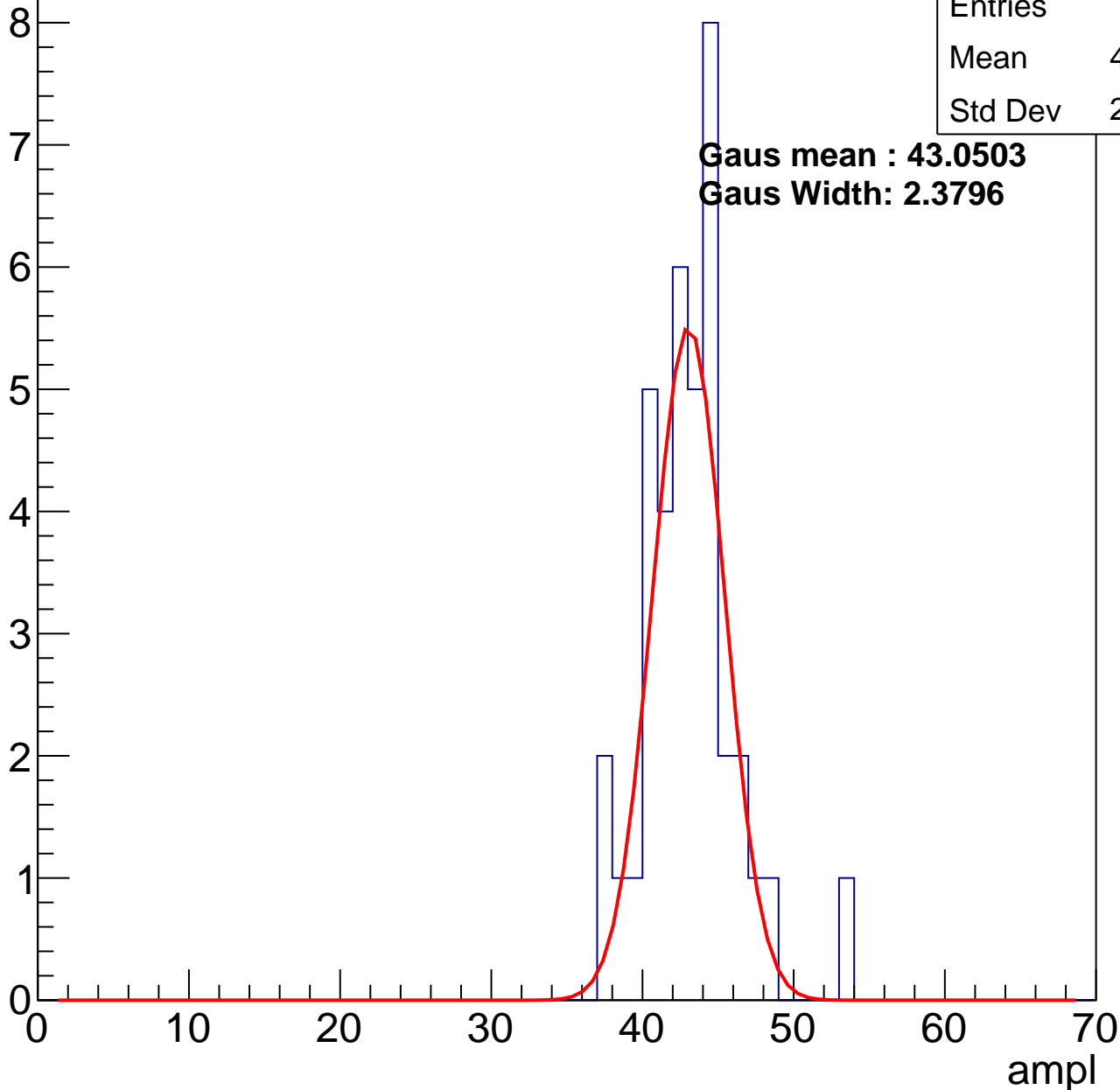
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	39
Mean	42.67
Std Dev	2.999

**Gaus mean : 43.0503**

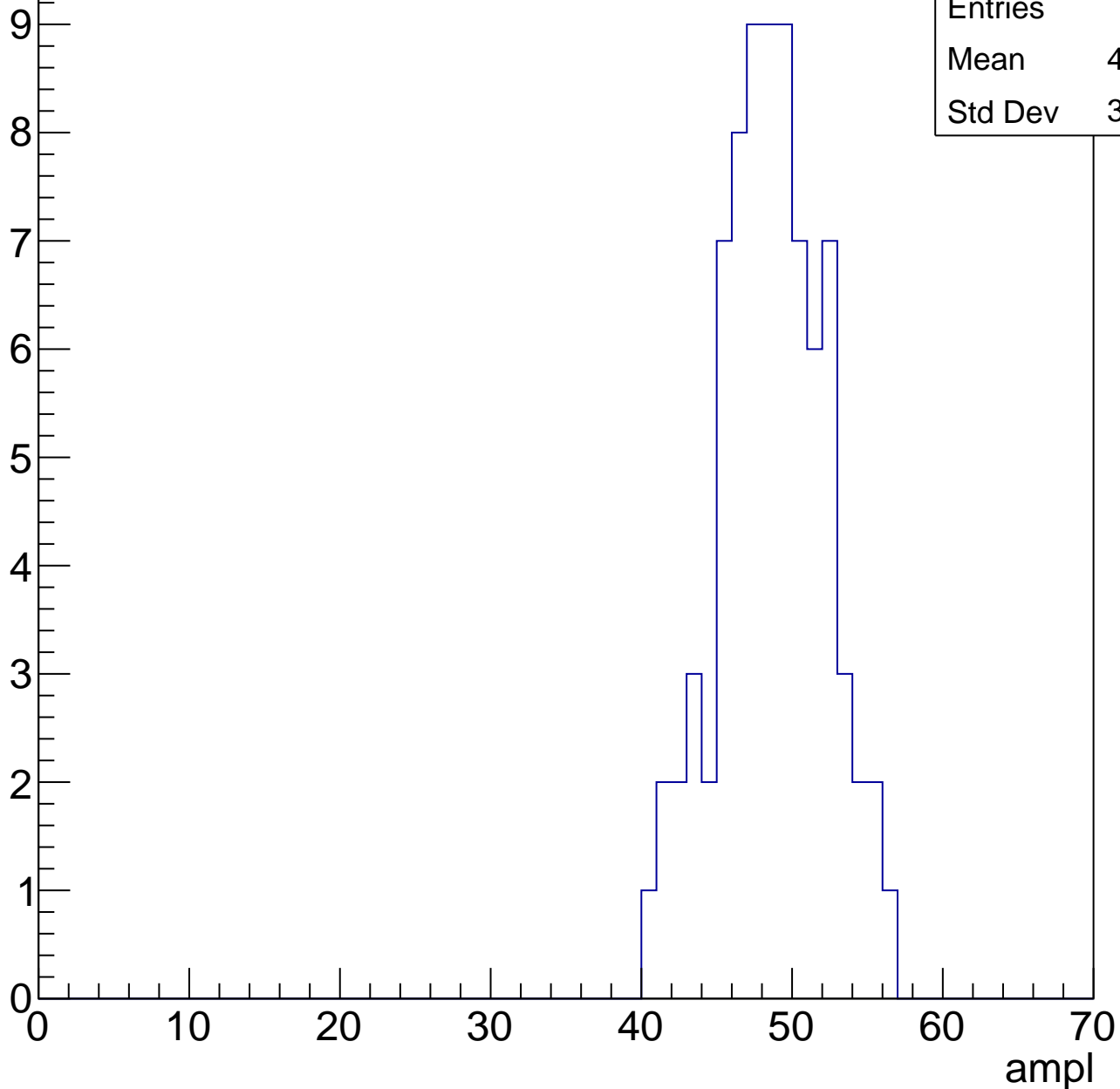
**Gaus Width: 2.3796**



# B1L003S, U26-ch4, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

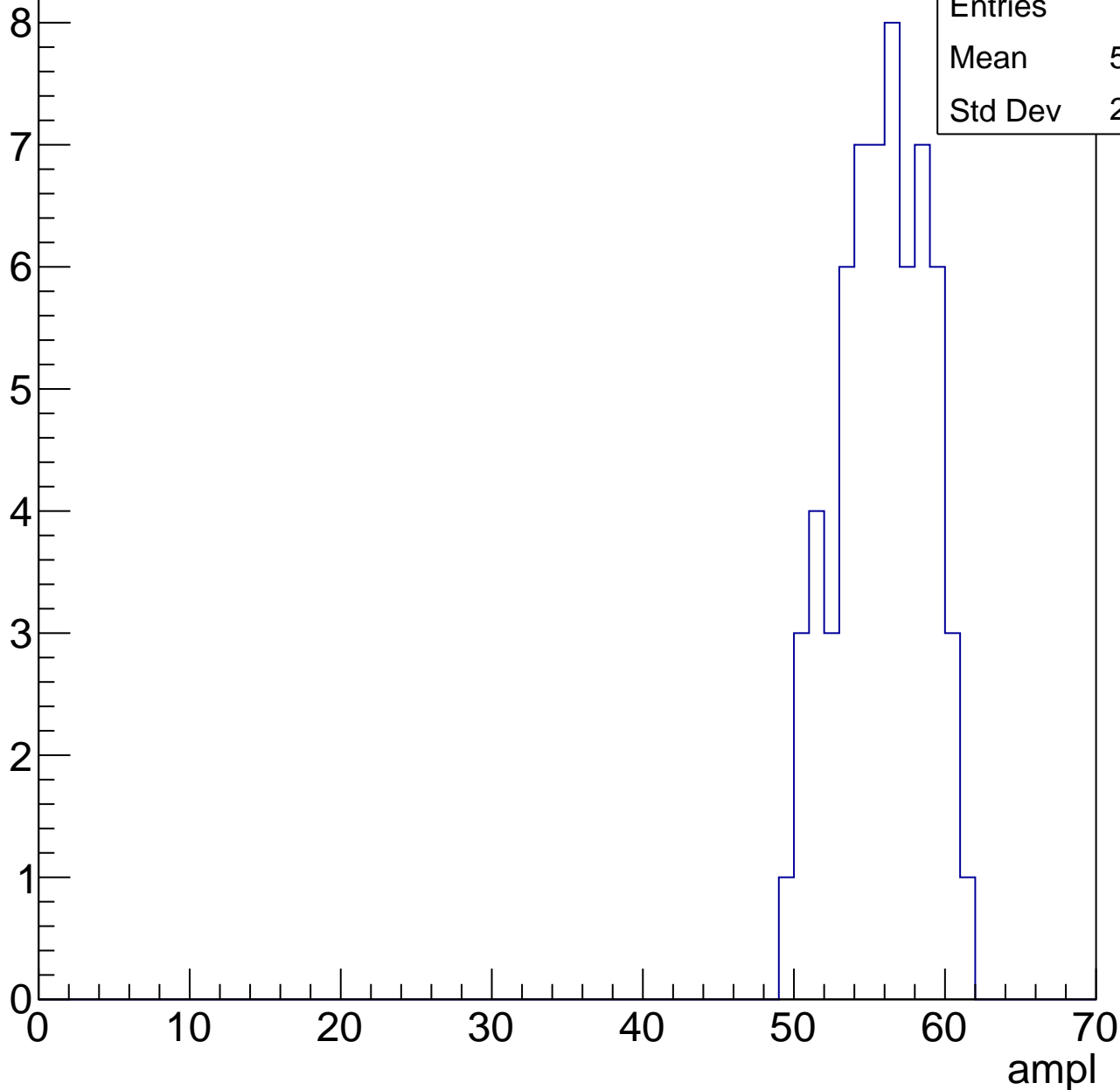


Entries	80
Mean	48.19
Std Dev	3.454

# B1L003S, U26-ch4, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



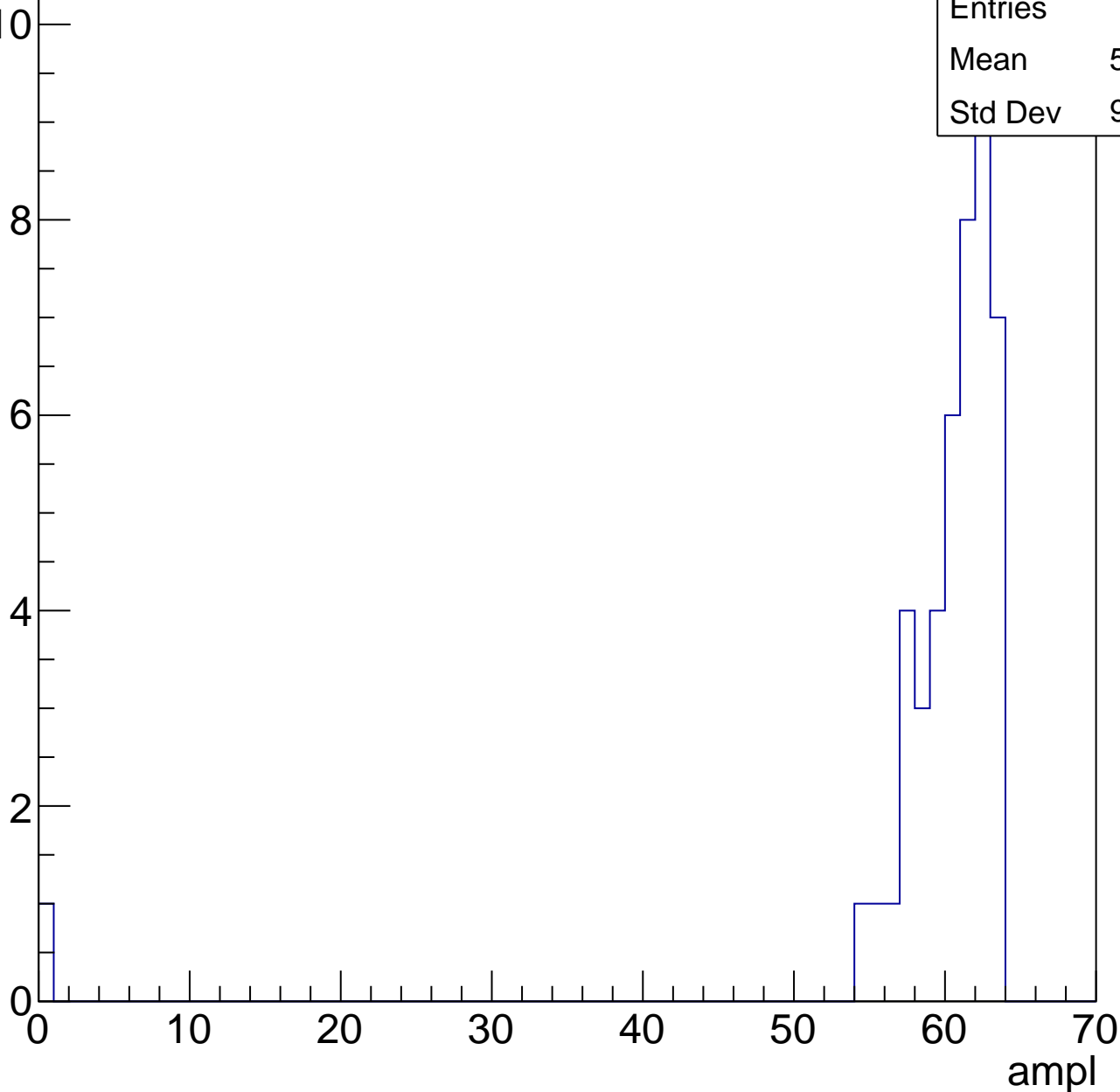
Entries	62
Mean	55.34
Std Dev	2.918

# B1L003S, U26-ch4, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

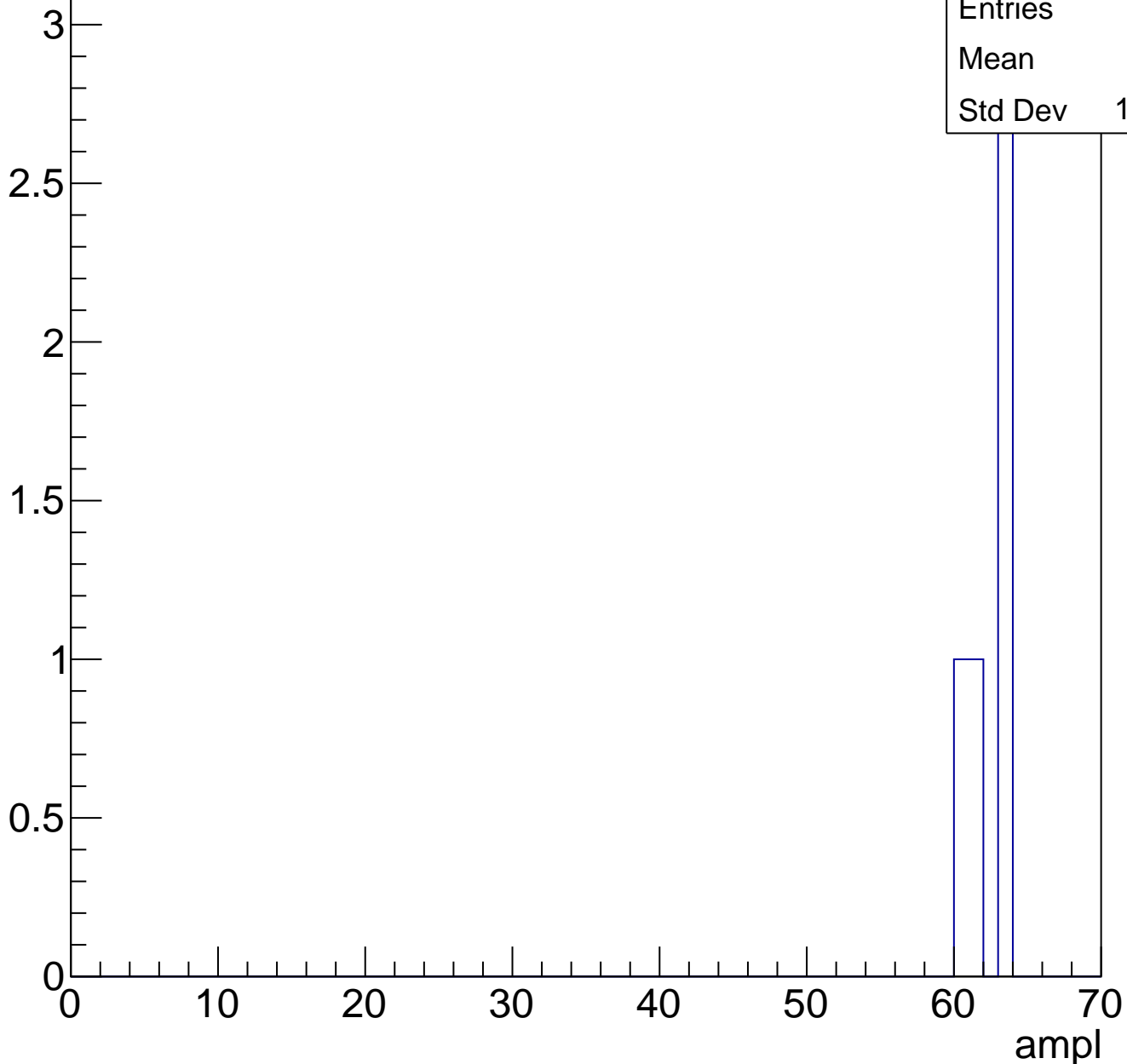
Entries	46
Mean	58.96
Std Dev	9.077



# B1L003S, U26-ch4, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch4, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U26-ch5, adc0

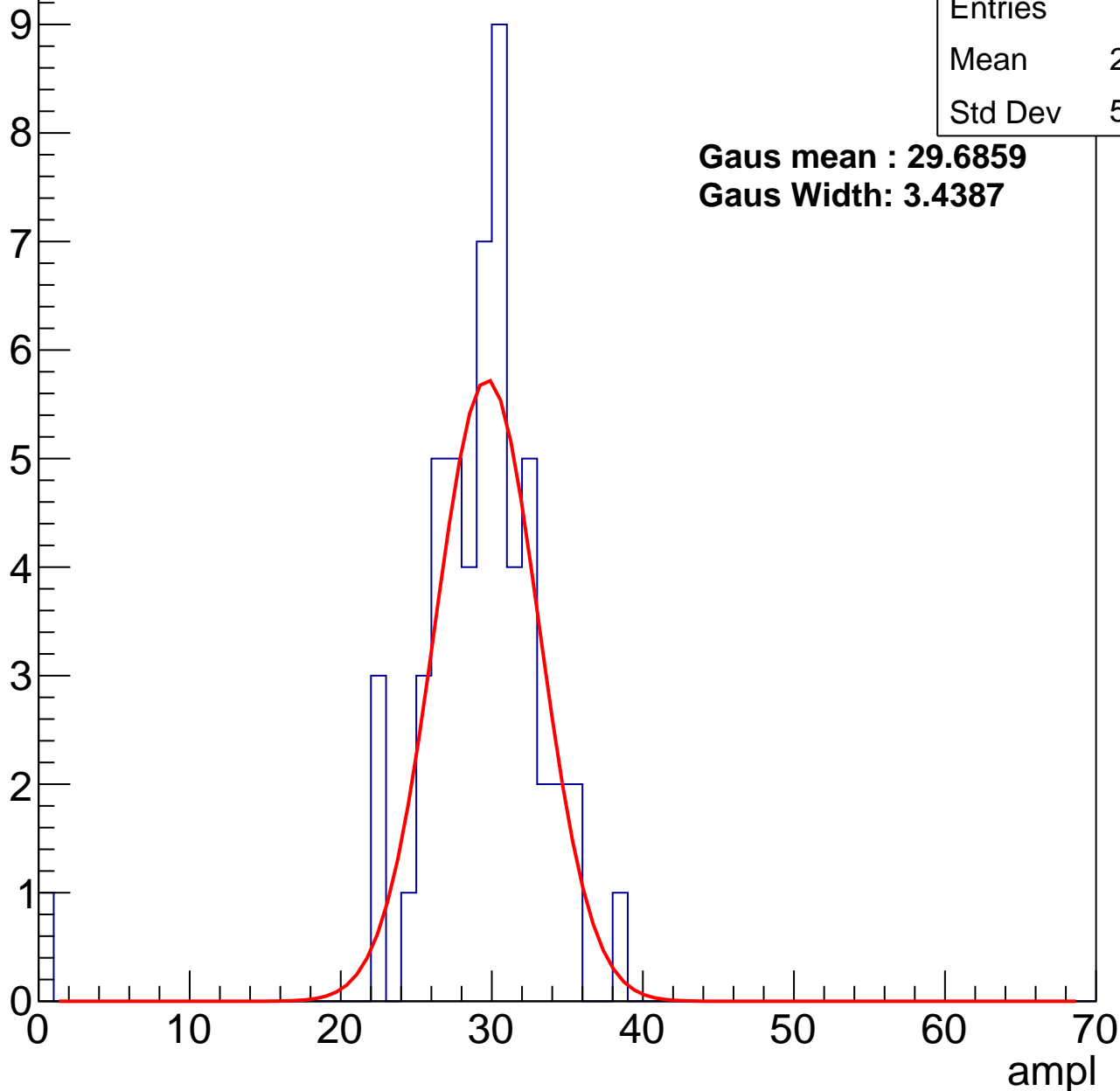
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	54
Mean	28.54
Std Dev	5.134

**Gaus mean : 29.6859**

**Gaus Width: 3.4387**



# B1L003S, U26-ch5, adc1

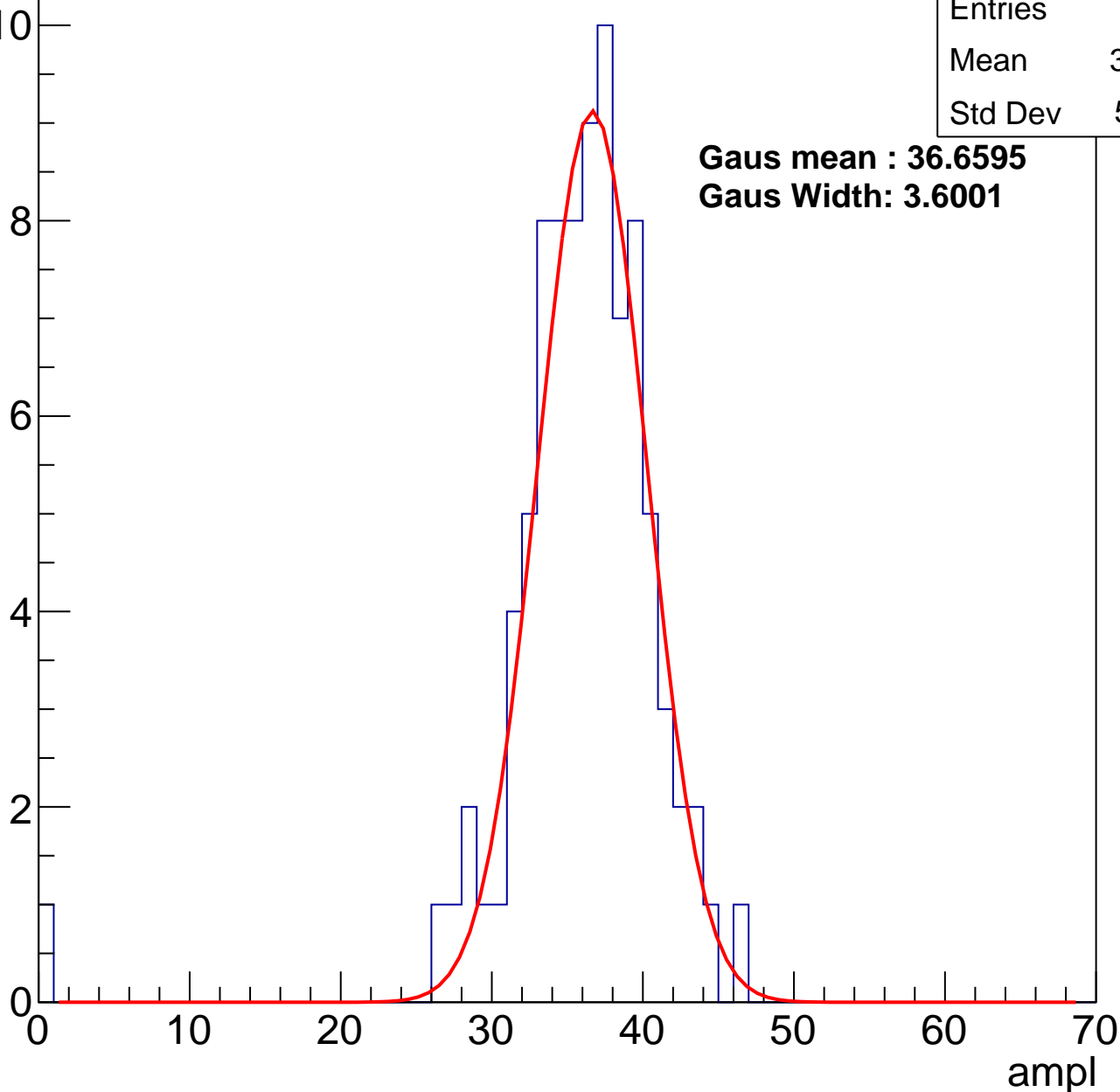
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	88
Mean	35.49
Std Dev	5.391

**Gaus mean : 36.6595**

**Gaus Width: 3.6001**

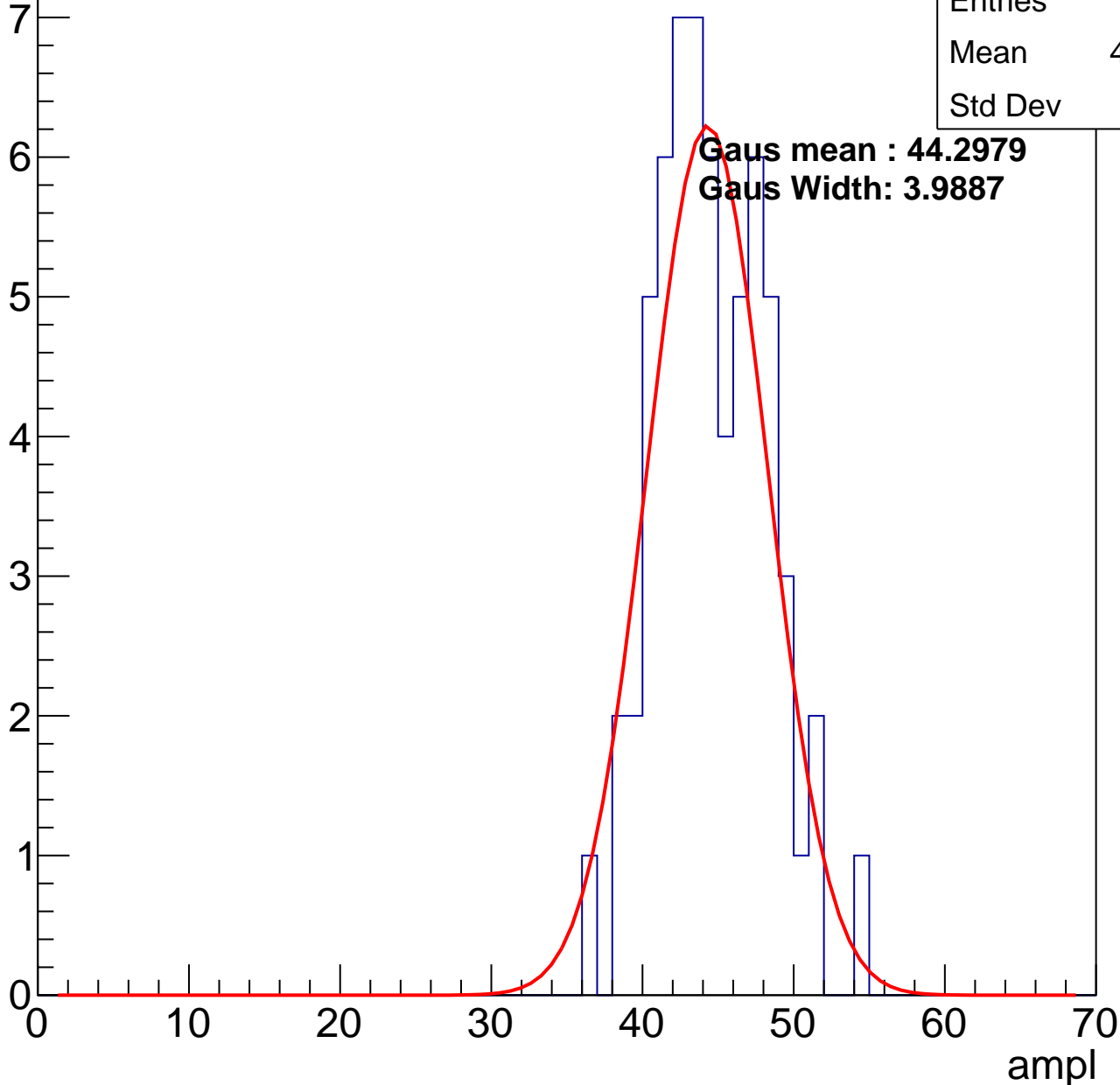


# B1L003S, U26-ch5, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	44.13
Std Dev	3.61

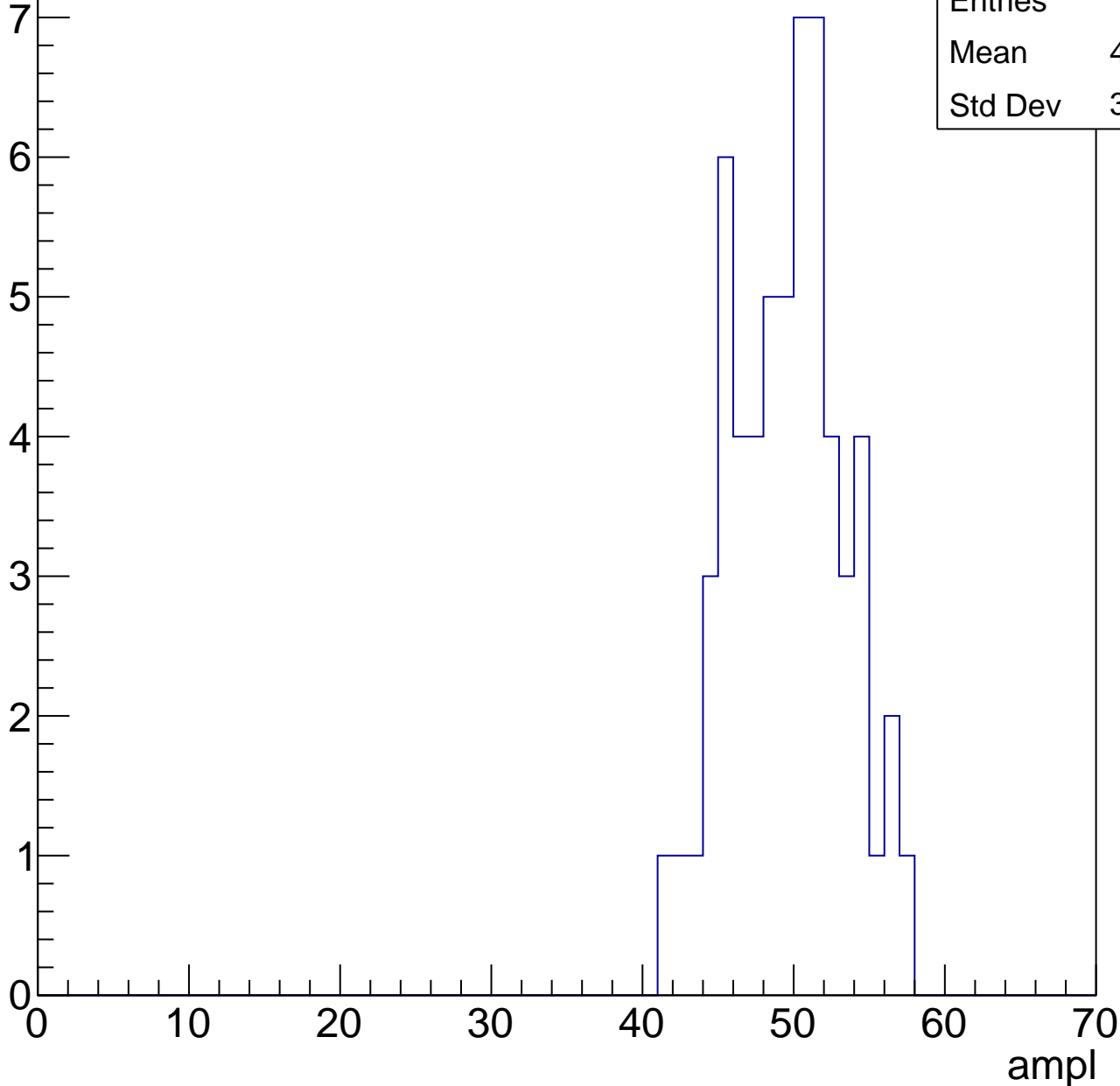


# B1L003S, U26-ch5, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

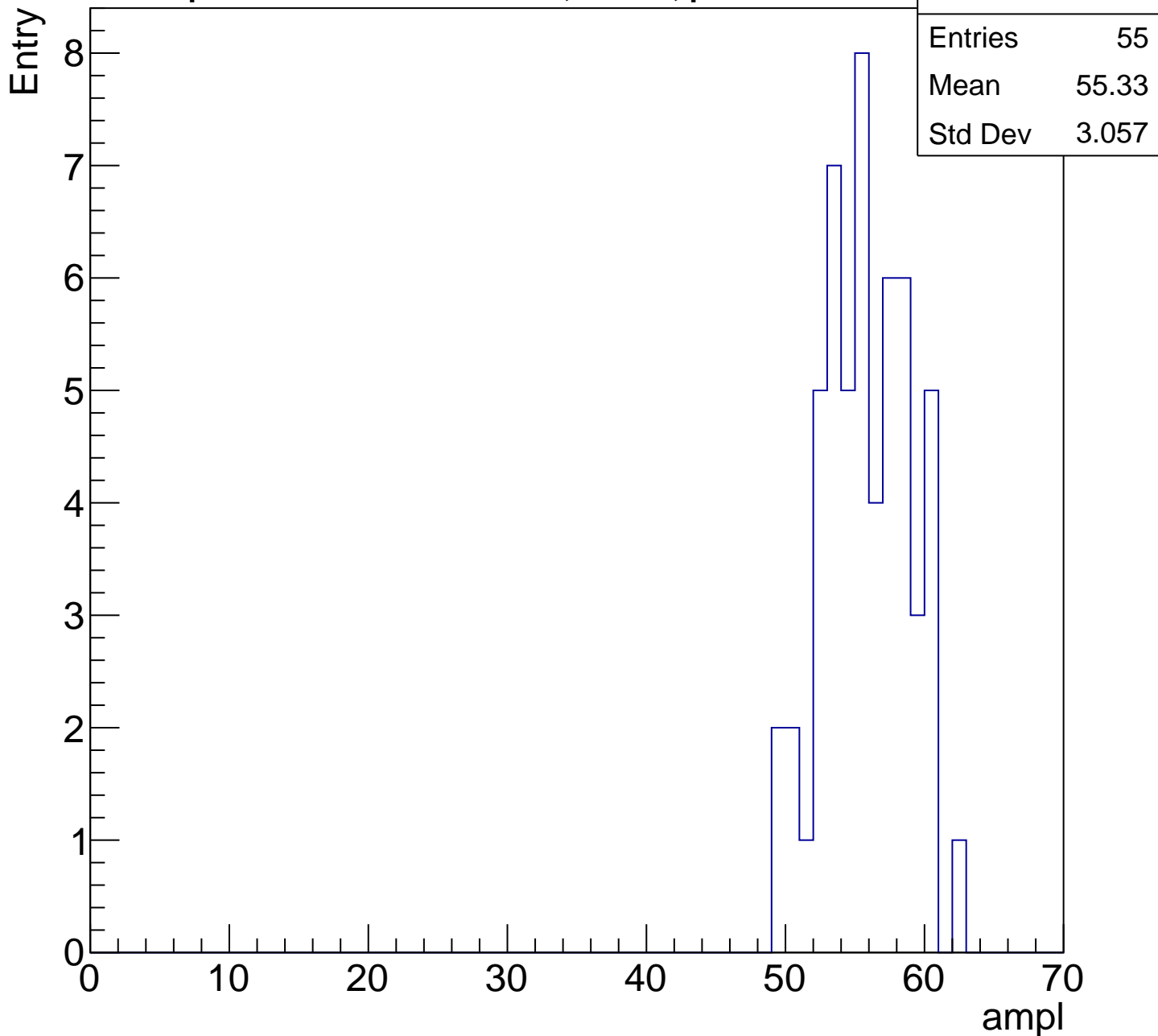
Entry

Entries	59
Mean	49.14
Std Dev	3.666



# B1L003S, U26-ch5, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

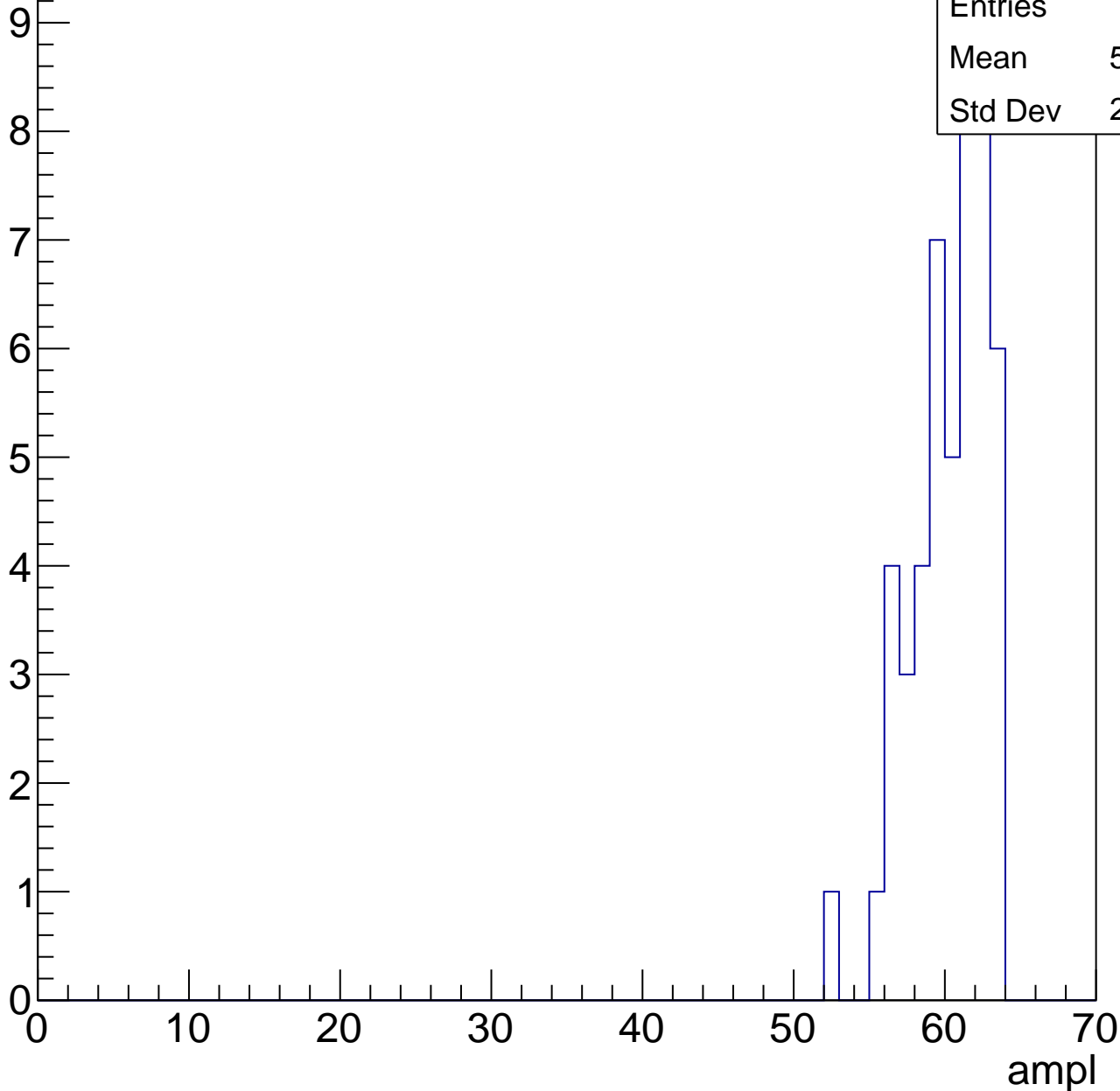


# B1L003S, U26-ch5, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

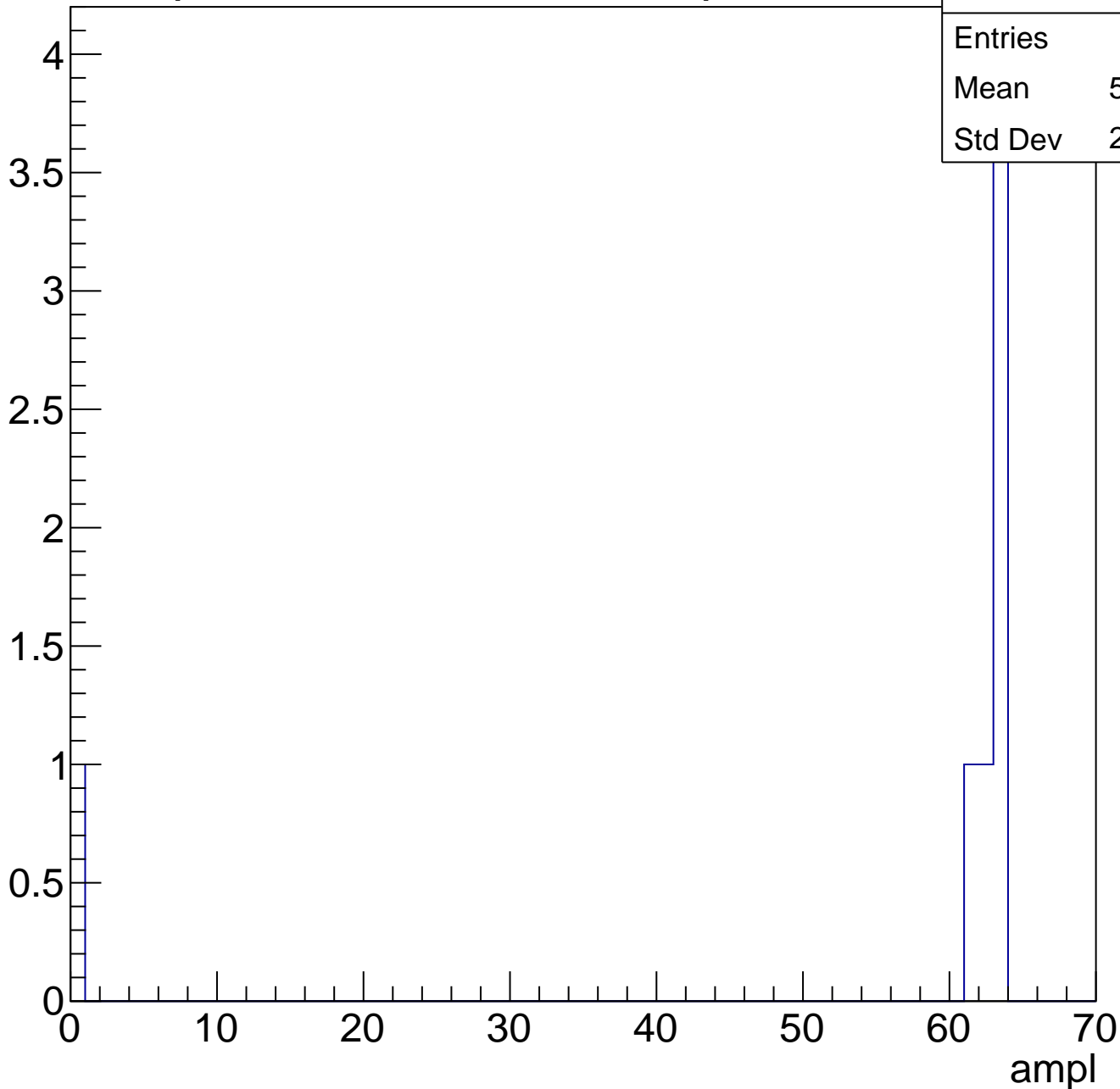
Entries	48
Mean	59.79
Std Dev	2.483



# B1L003S, U26-ch5, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch5, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U26-ch6, adc0

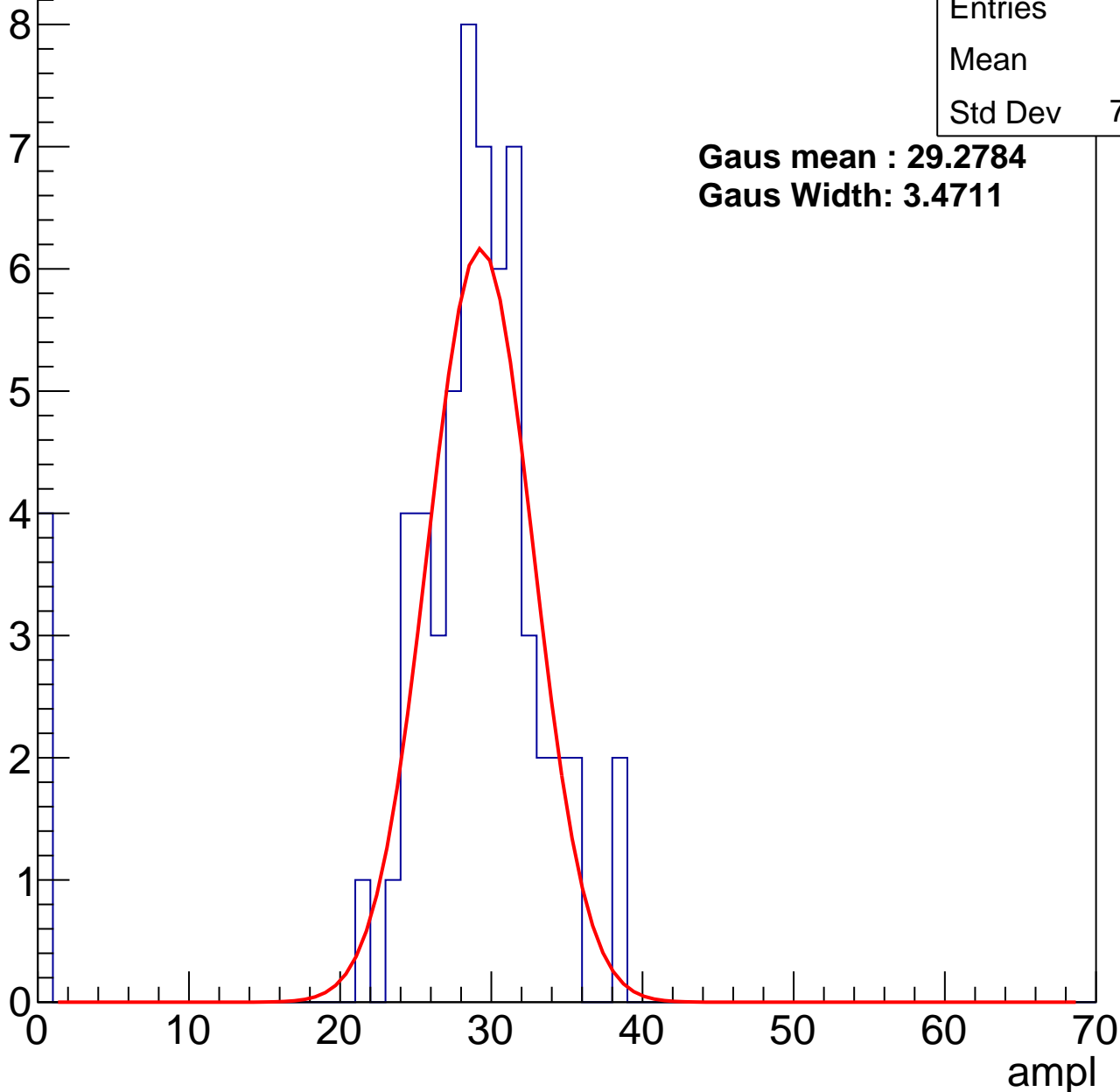
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	27.1
Std Dev	7.934

**Gaus mean : 29.2784**

**Gaus Width: 3.4711**



# B1L003S, U26-ch6, adc1

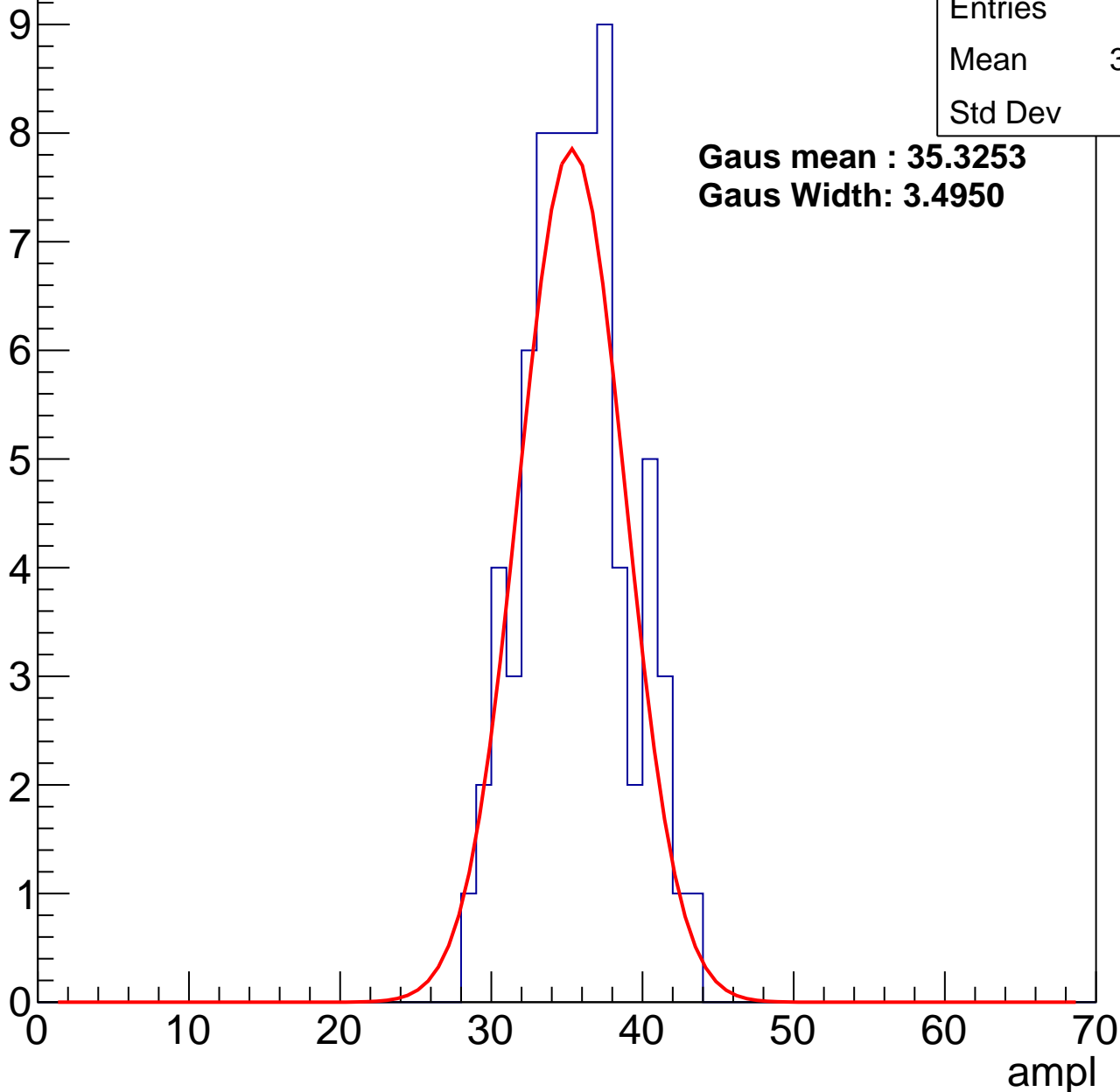
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	73
Mean	35.15
Std Dev	3.35

**Gaus mean : 35.3253**

**Gaus Width: 3.4950**



# B1L003S, U26-ch6, adc2

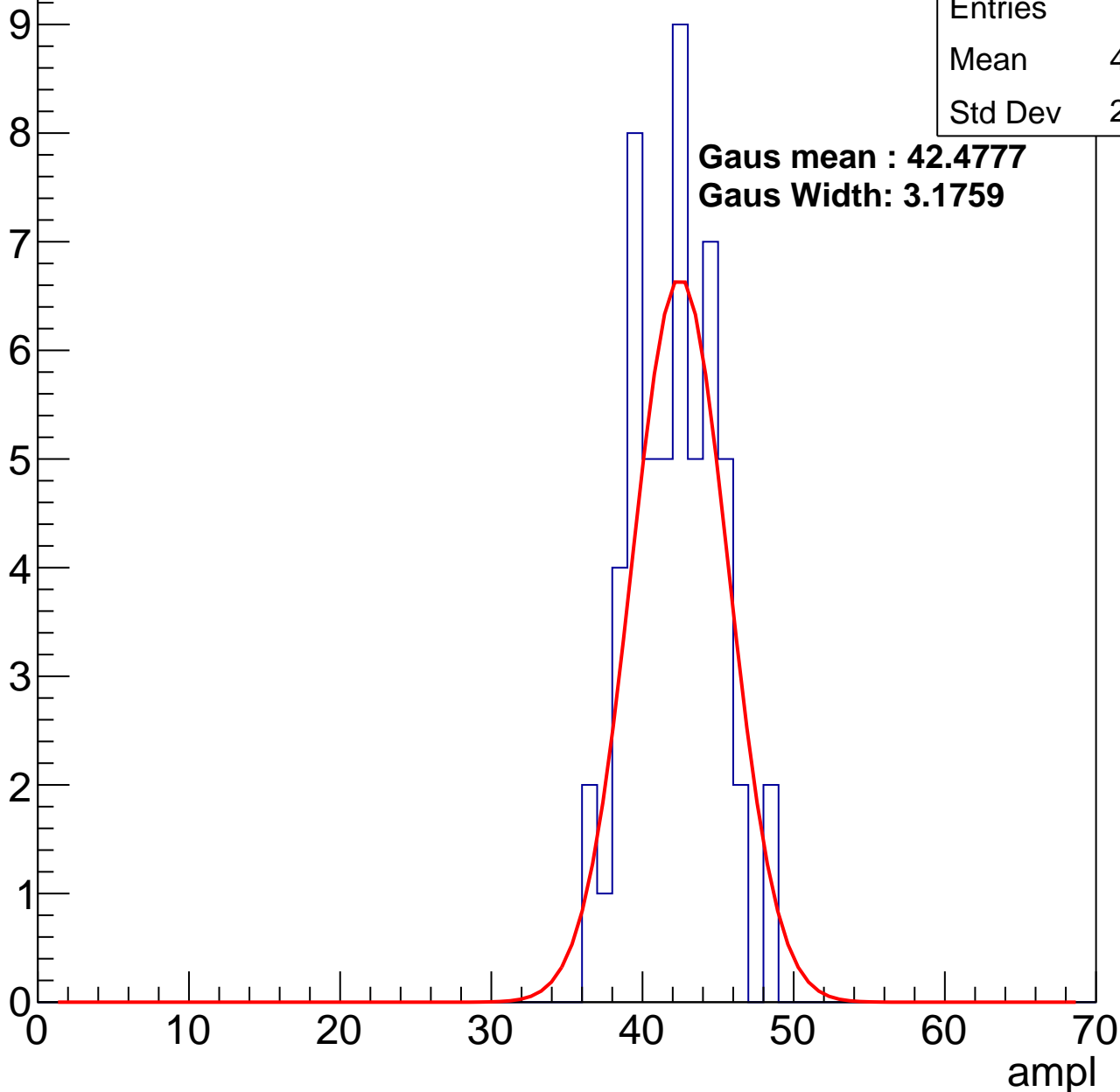
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	41.67
Std Dev	2.809

**Gaus mean : 42.4777**

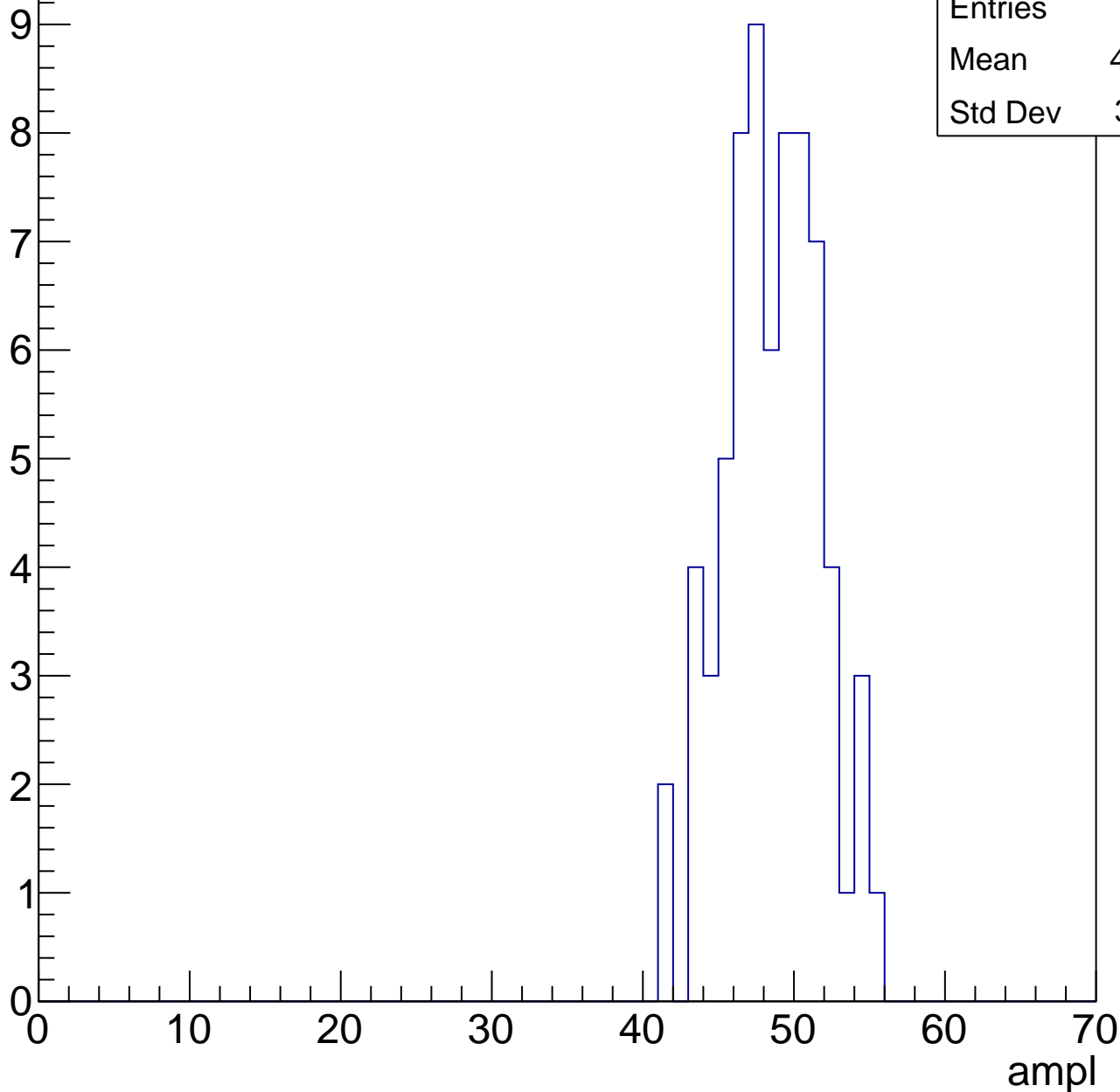
**Gaus Width: 3.1759**



# B1L003S, U26-ch6, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



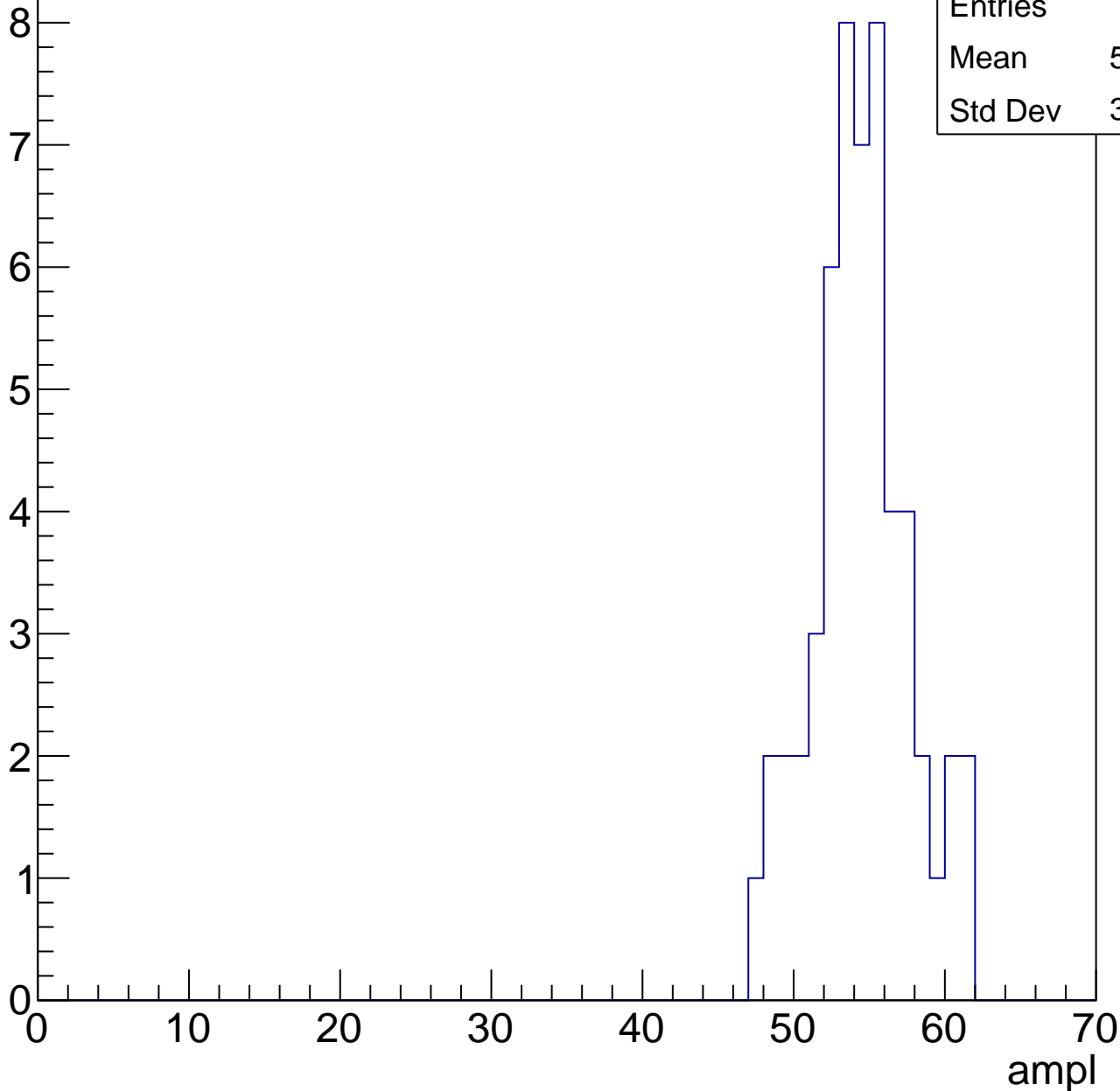
Entries	69
Mean	48.07
Std Dev	3.141

# B1L003S, U26-ch6, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	54
Mean	54.02
Std Dev	3.188

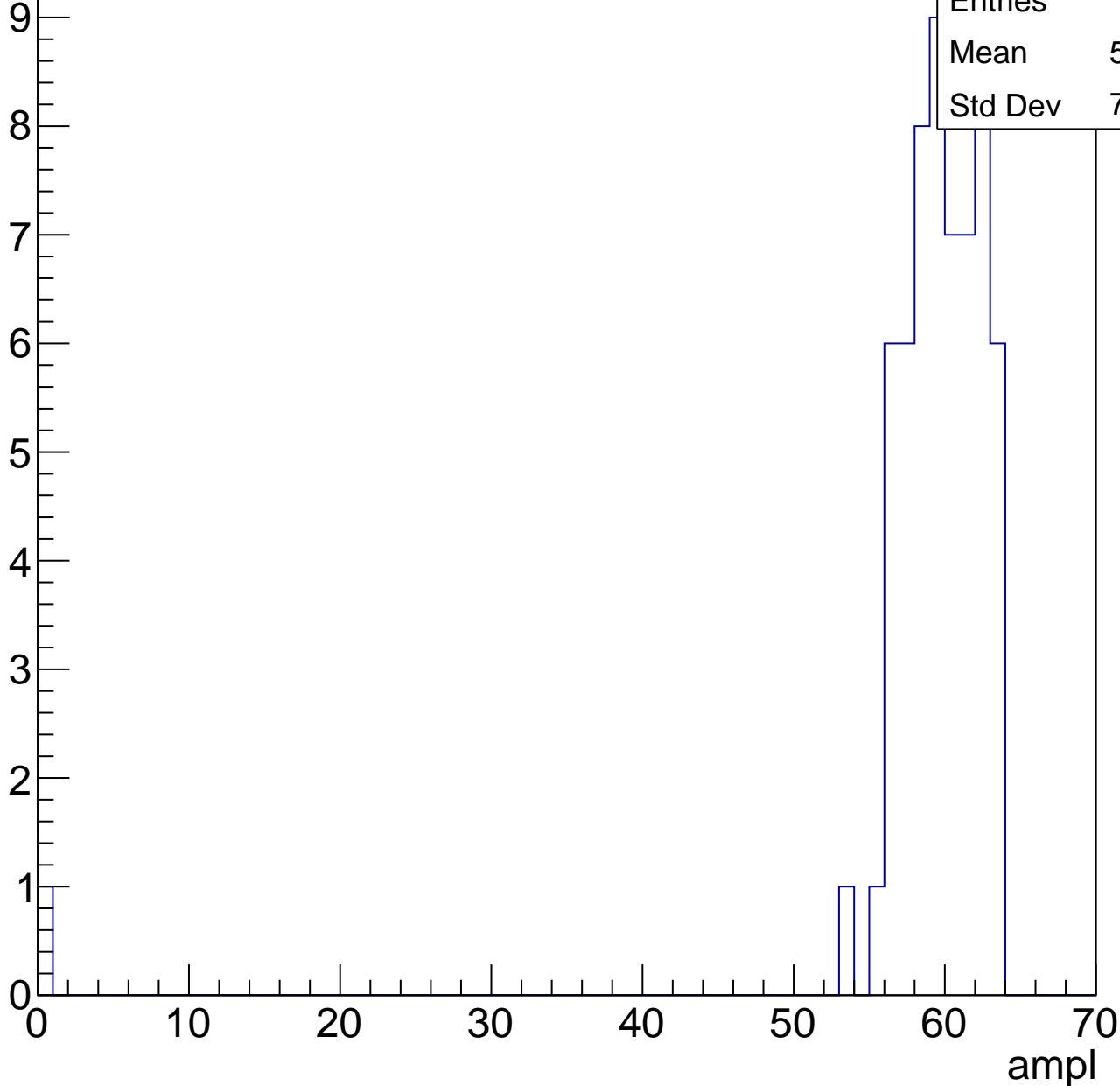


# B1L003S, U26-ch6, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

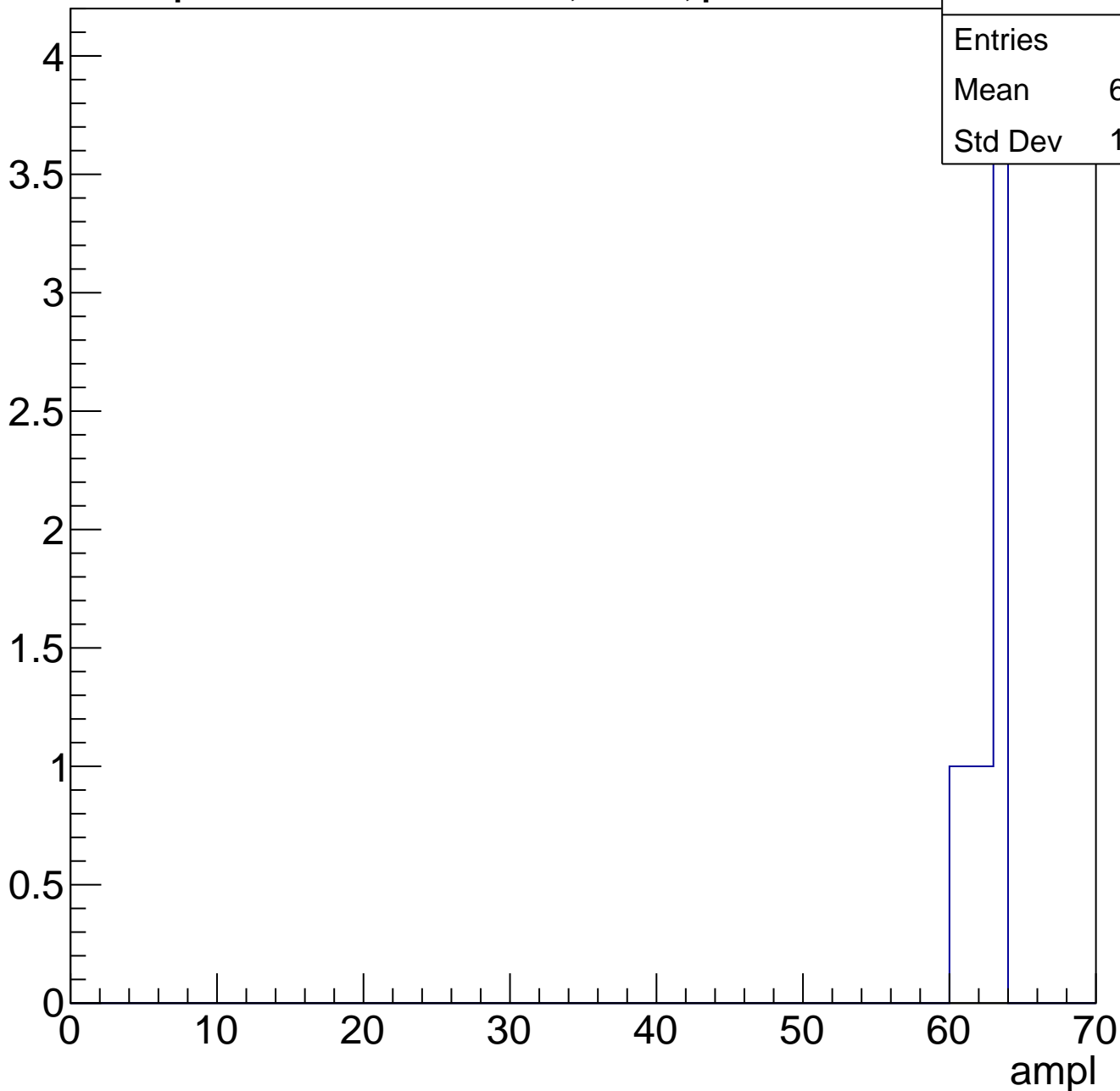
Entries	61
Mean	58.43
Std Dev	7.904



# B1L003S, U26-ch6, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch6, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U26-ch7, adc0

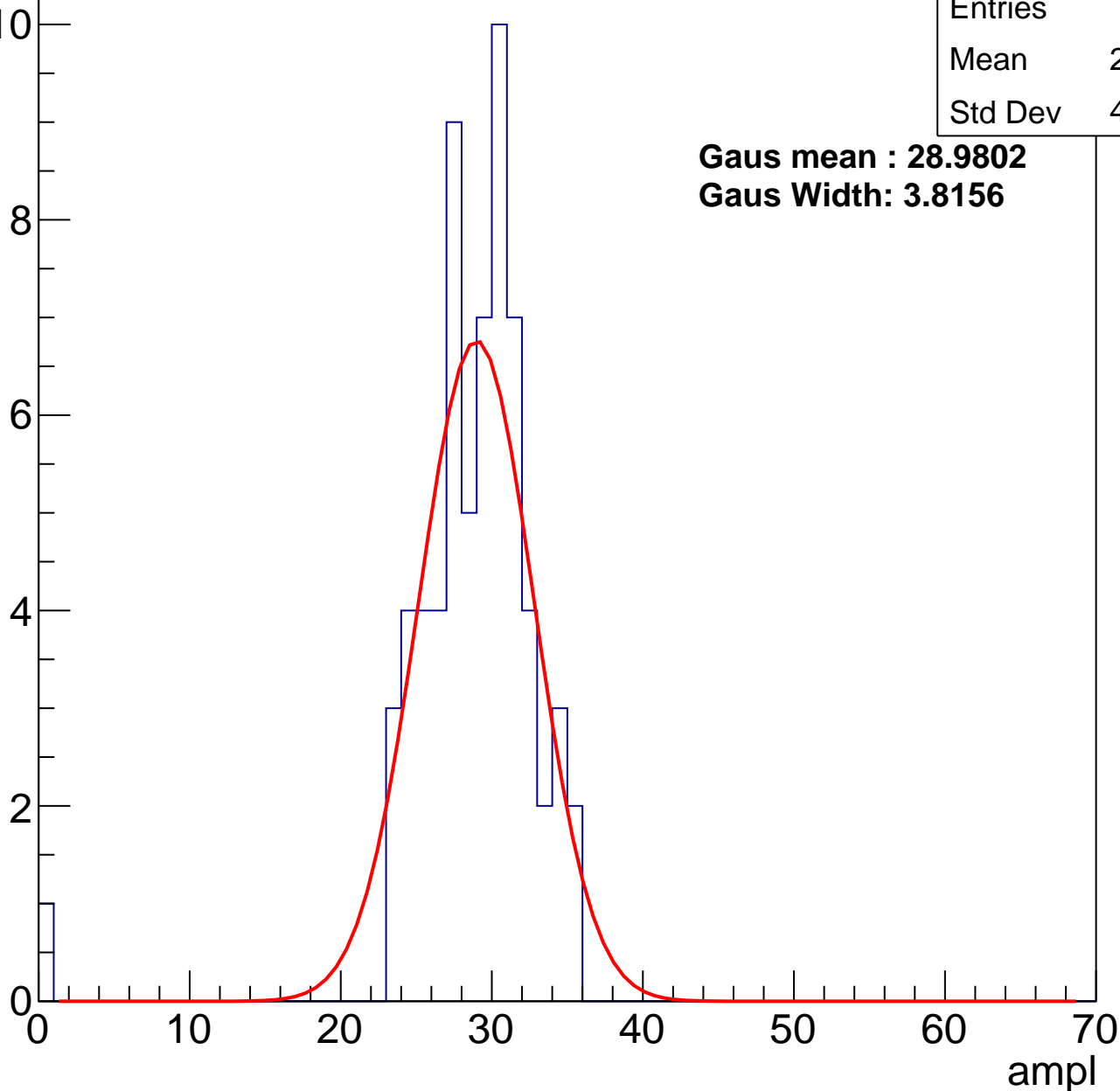
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	28.28
Std Dev	4.656

**Gaus mean : 28.9802**

**Gaus Width: 3.8156**



# B1L003S, U26-ch7, adc1

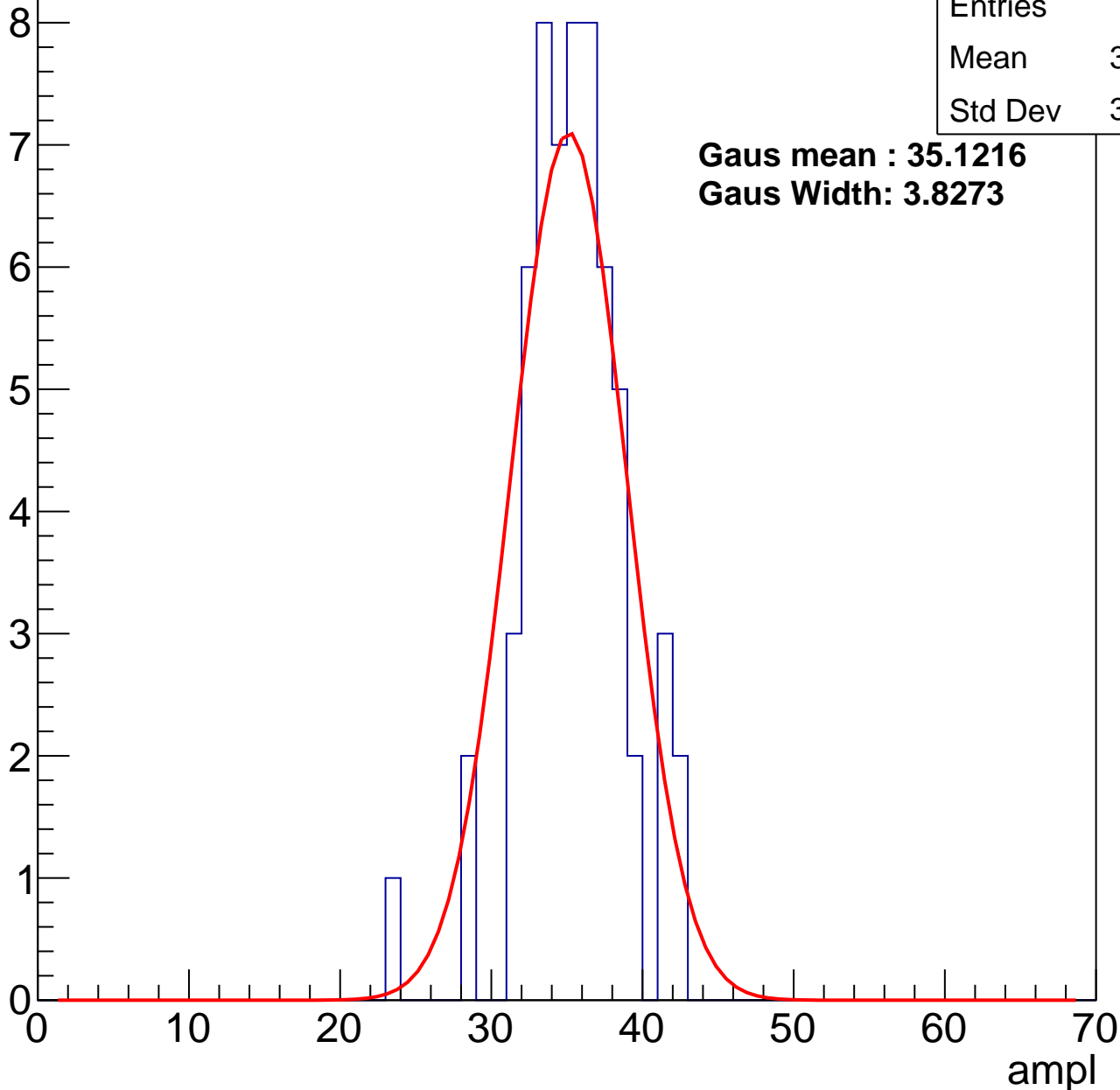
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	34.93
Std Dev	3.382

**Gaus mean : 35.1216**

**Gaus Width: 3.8273**



# B1L003S, U26-ch7, adc2

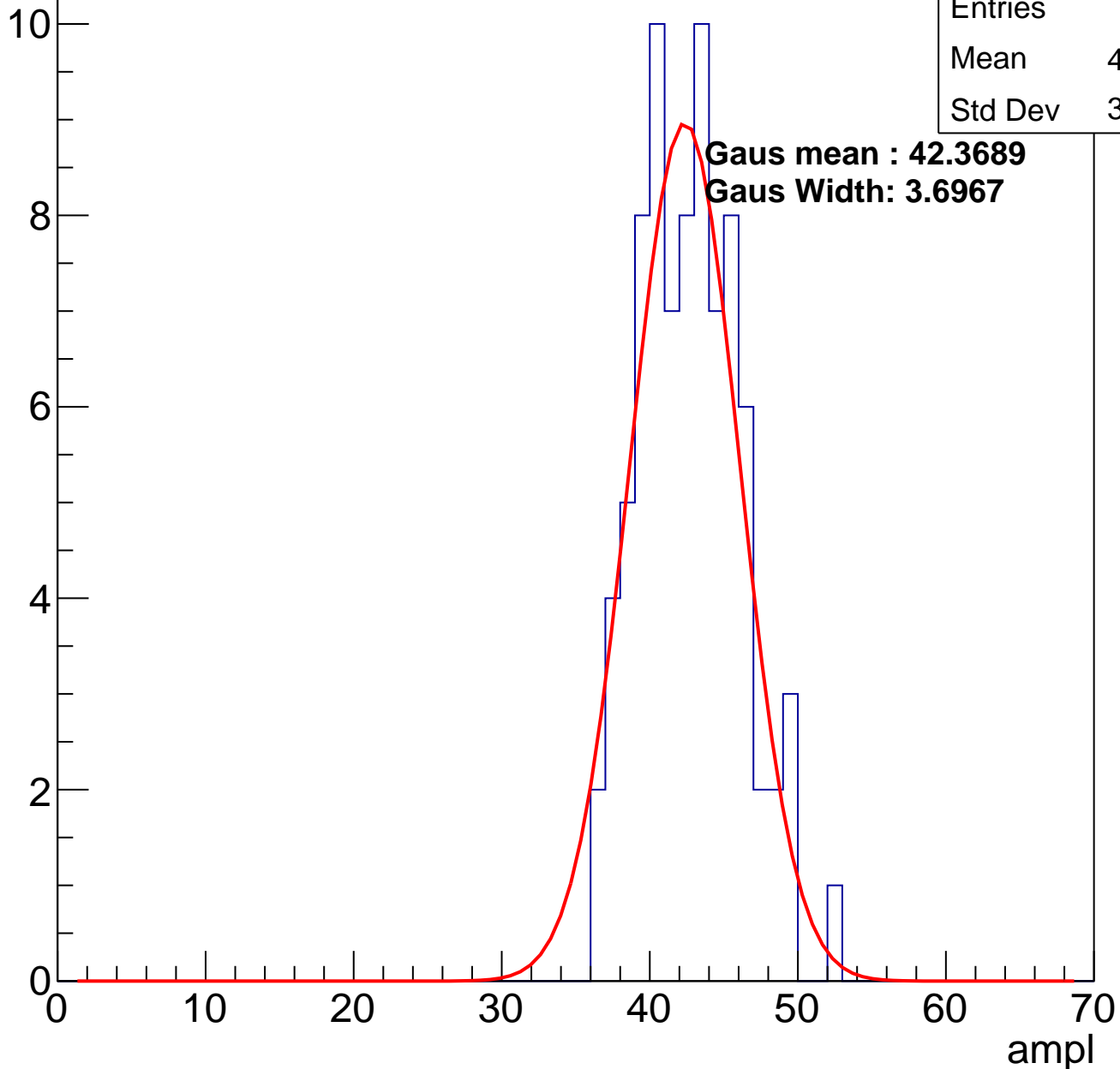
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	83
Mean	42.27
Std Dev	3.366

**Gaus mean : 42.3689**

**Gaus Width: 3.6967**

Entry

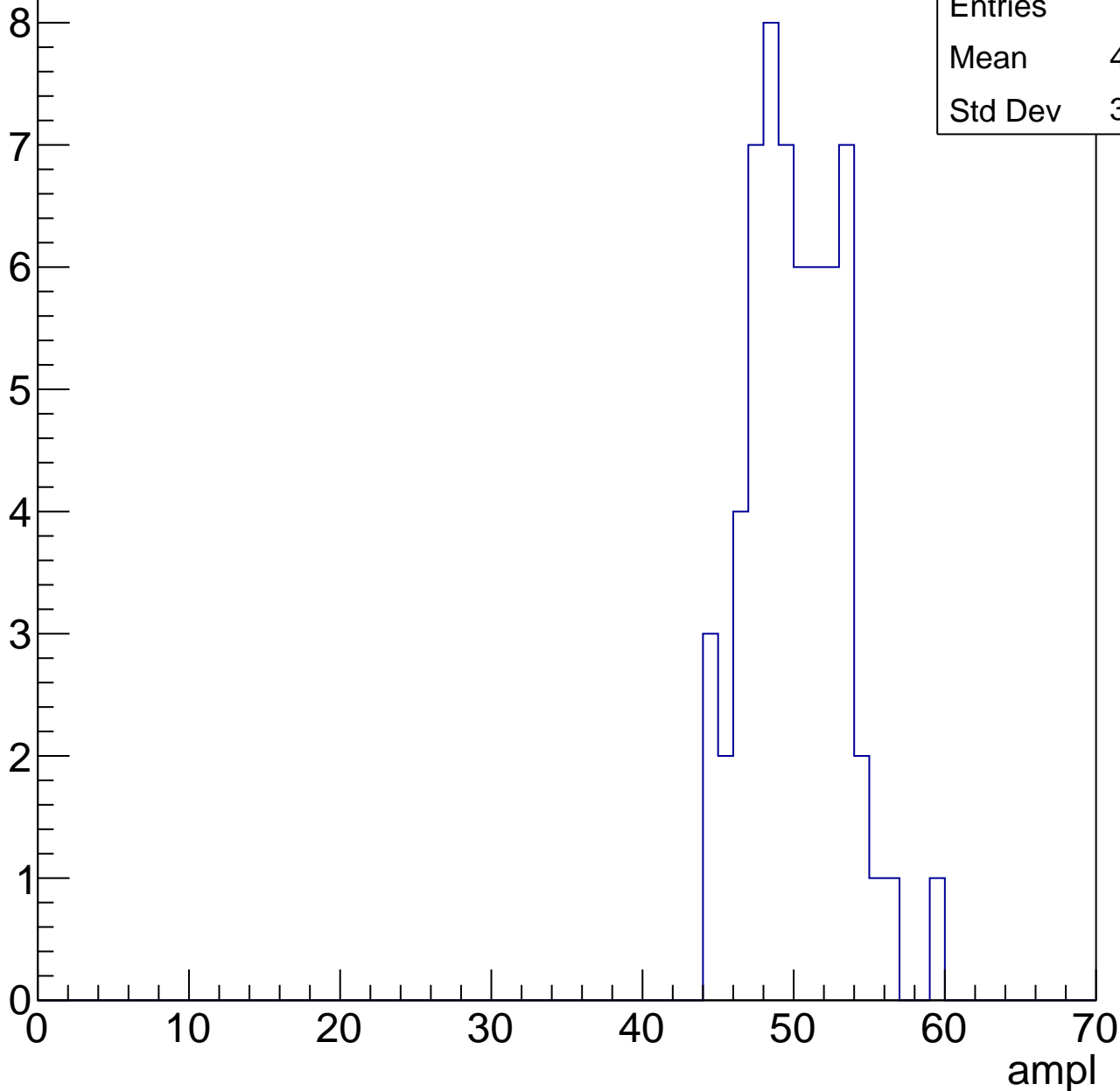


# B1L003S, U26-ch7, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	49.66
Std Dev	3.094

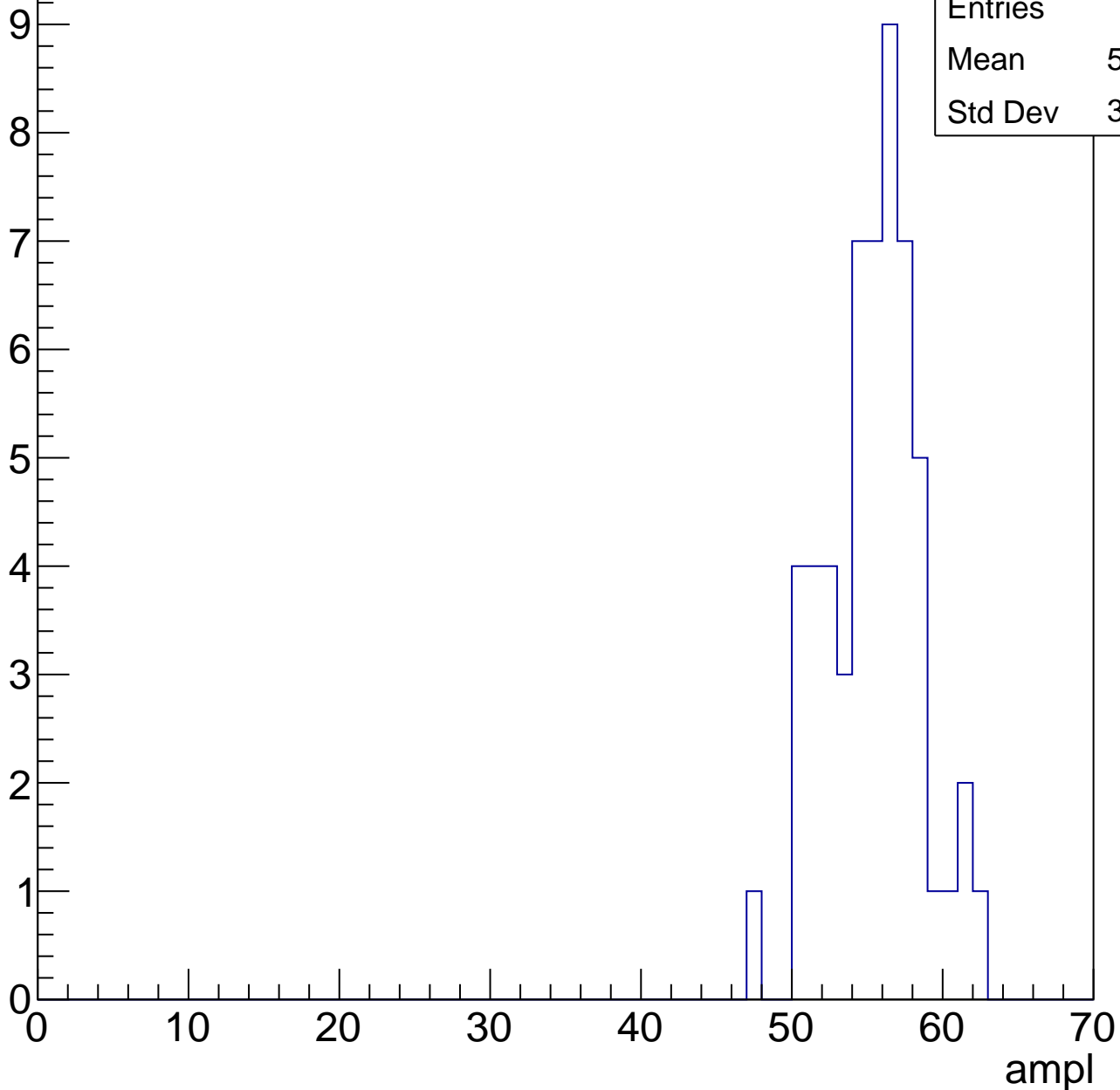


# B1L003S, U26-ch7, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

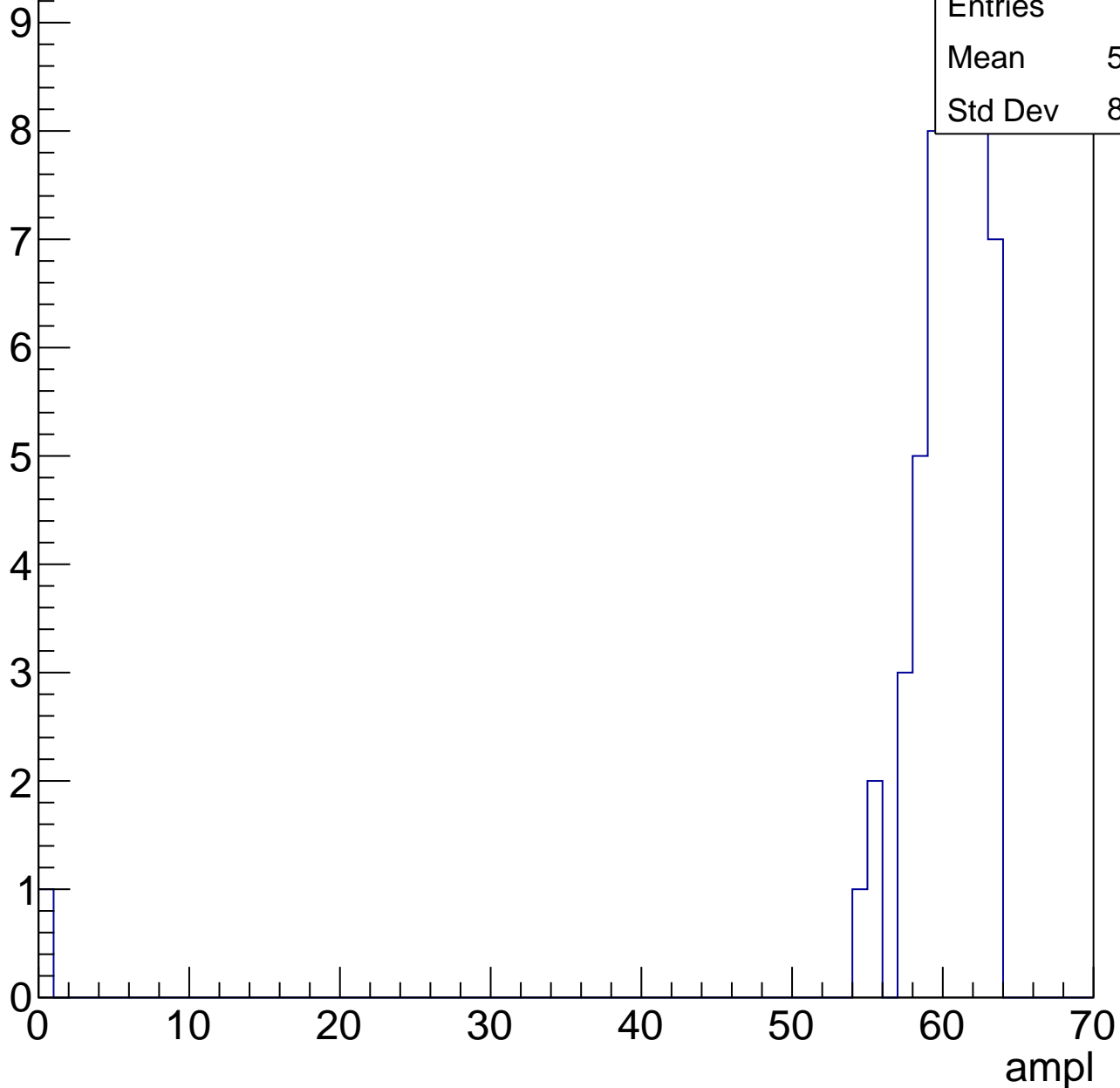
Entries	56
Mean	54.95
Std Dev	3.067



# B1L003S, U26-ch7, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U26-ch7, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	4
Mean	62.75
Std Dev	0.433



# B1L003S, U26-ch7, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U26-ch8, adc0

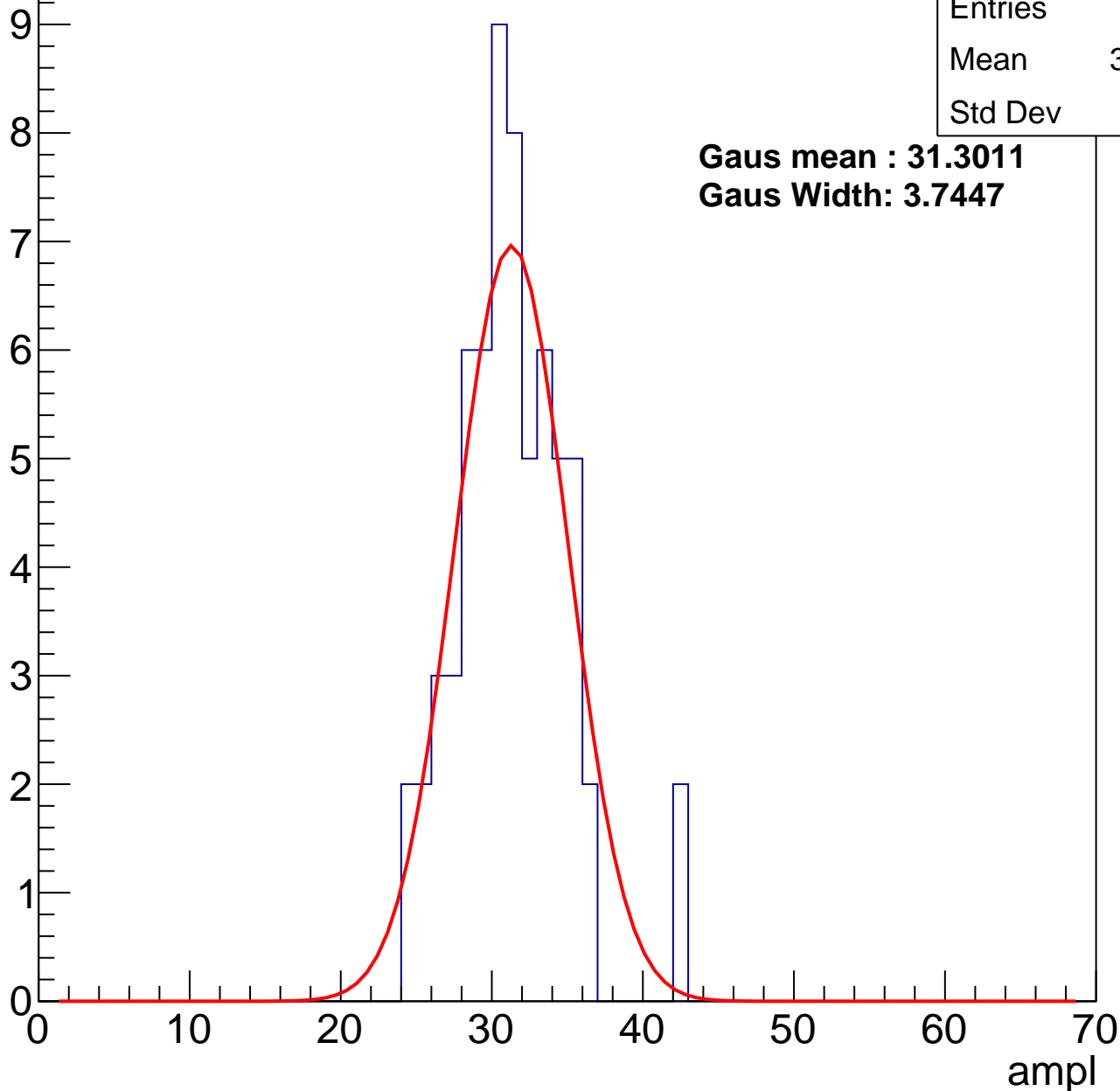
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	30.88
Std Dev	3.59

**Gaus mean : 31.3011**

**Gaus Width: 3.7447**



# B1L003S, U26-ch8, adc1

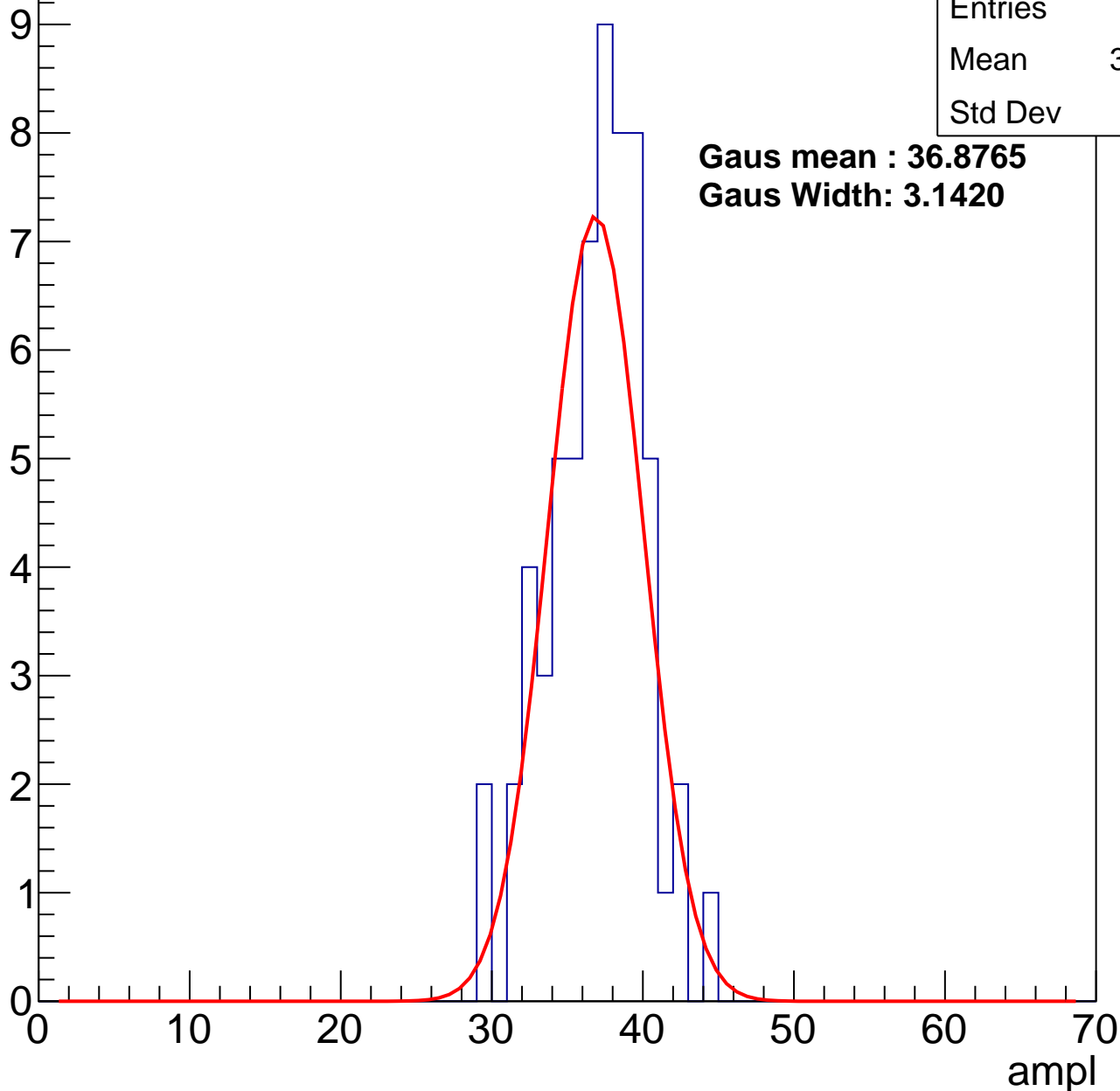
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	36.48
Std Dev	3.12

**Gaus mean : 36.8765**

**Gaus Width: 3.1420**



# B1L003S, U26-ch8, adc2

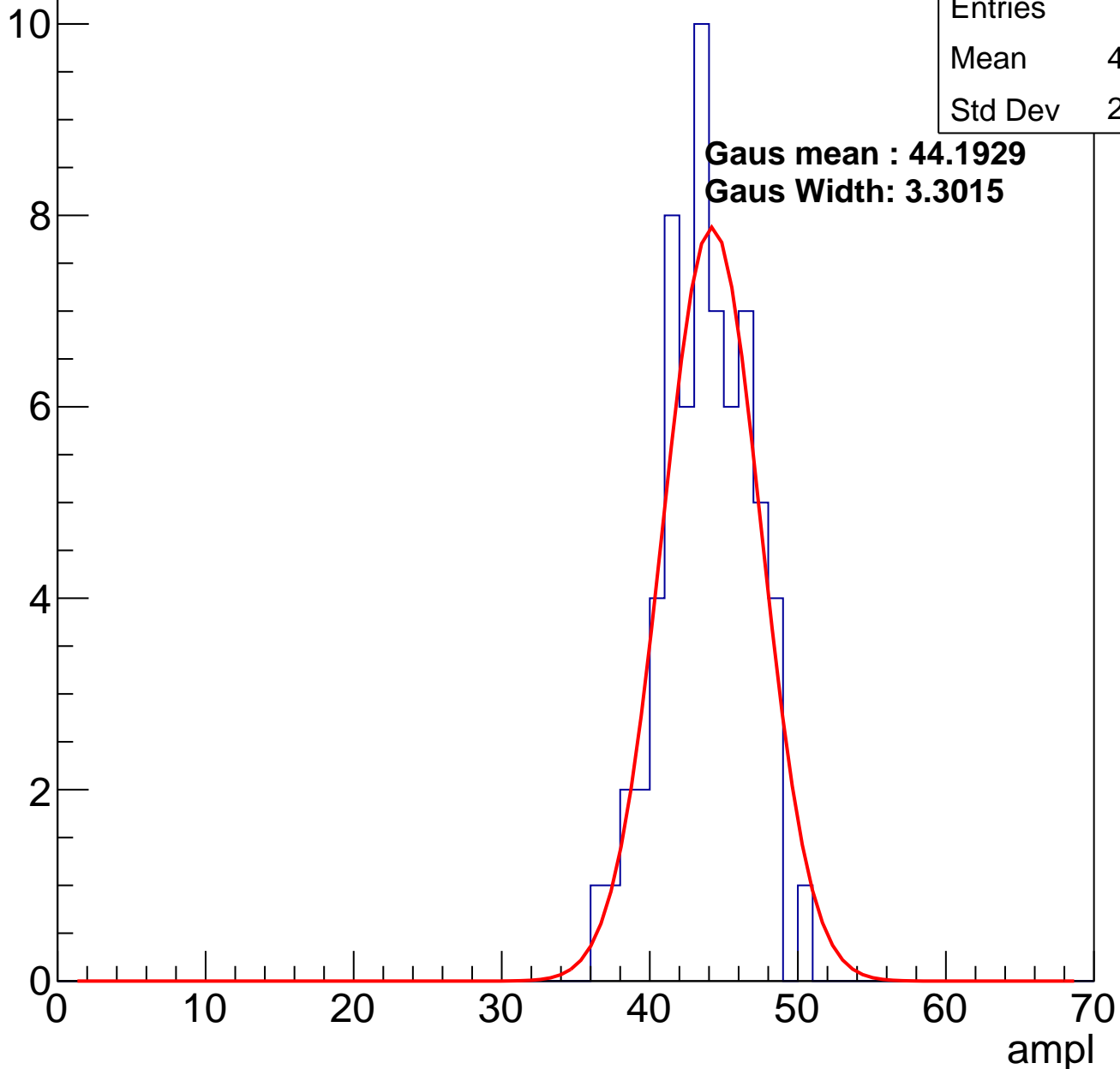
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	64
Mean	43.34
Std Dev	2.949

**Gaus mean : 44.1929**

**Gaus Width: 3.3015**

Entry

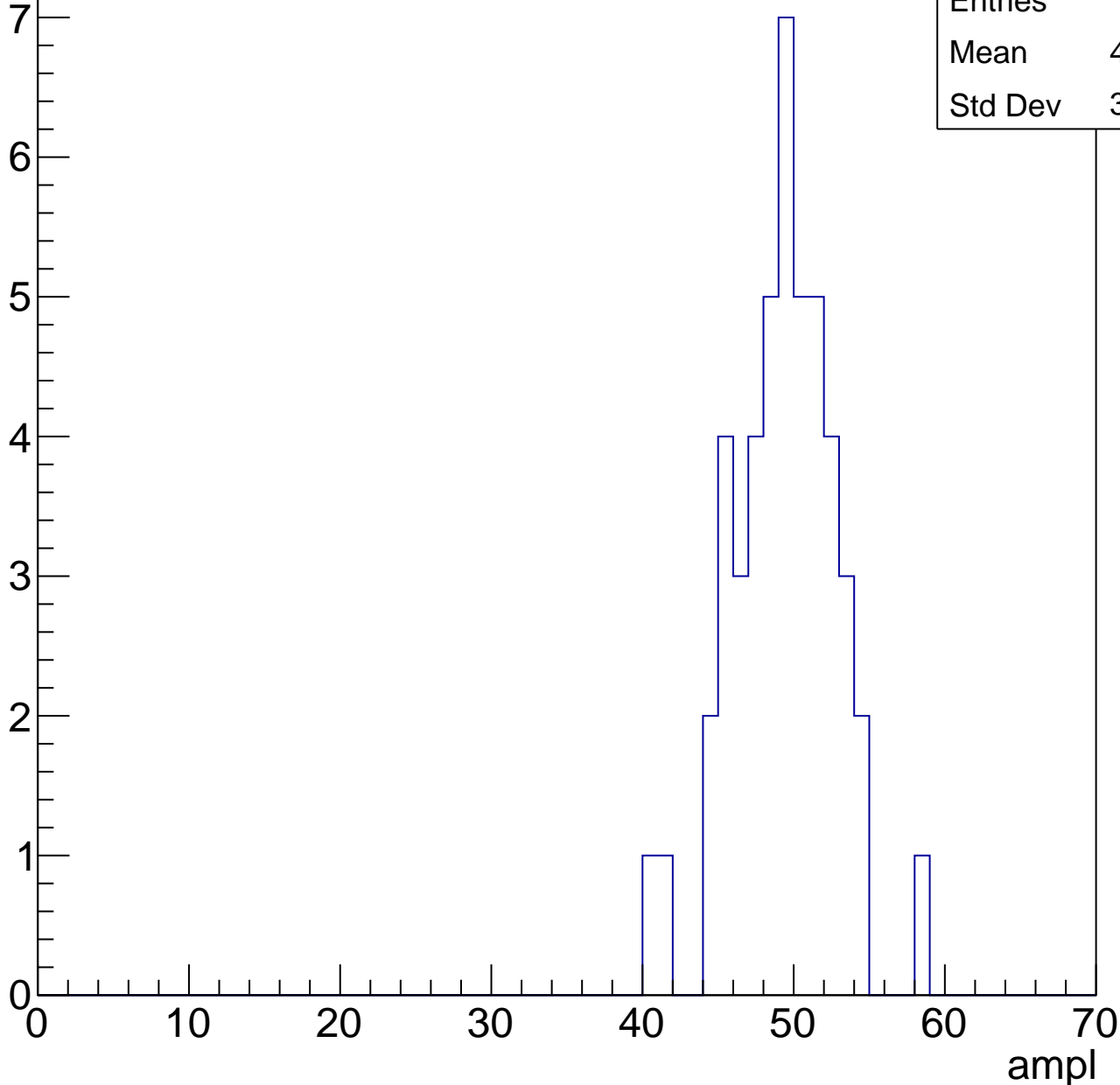


# B1L003S, U26-ch8, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

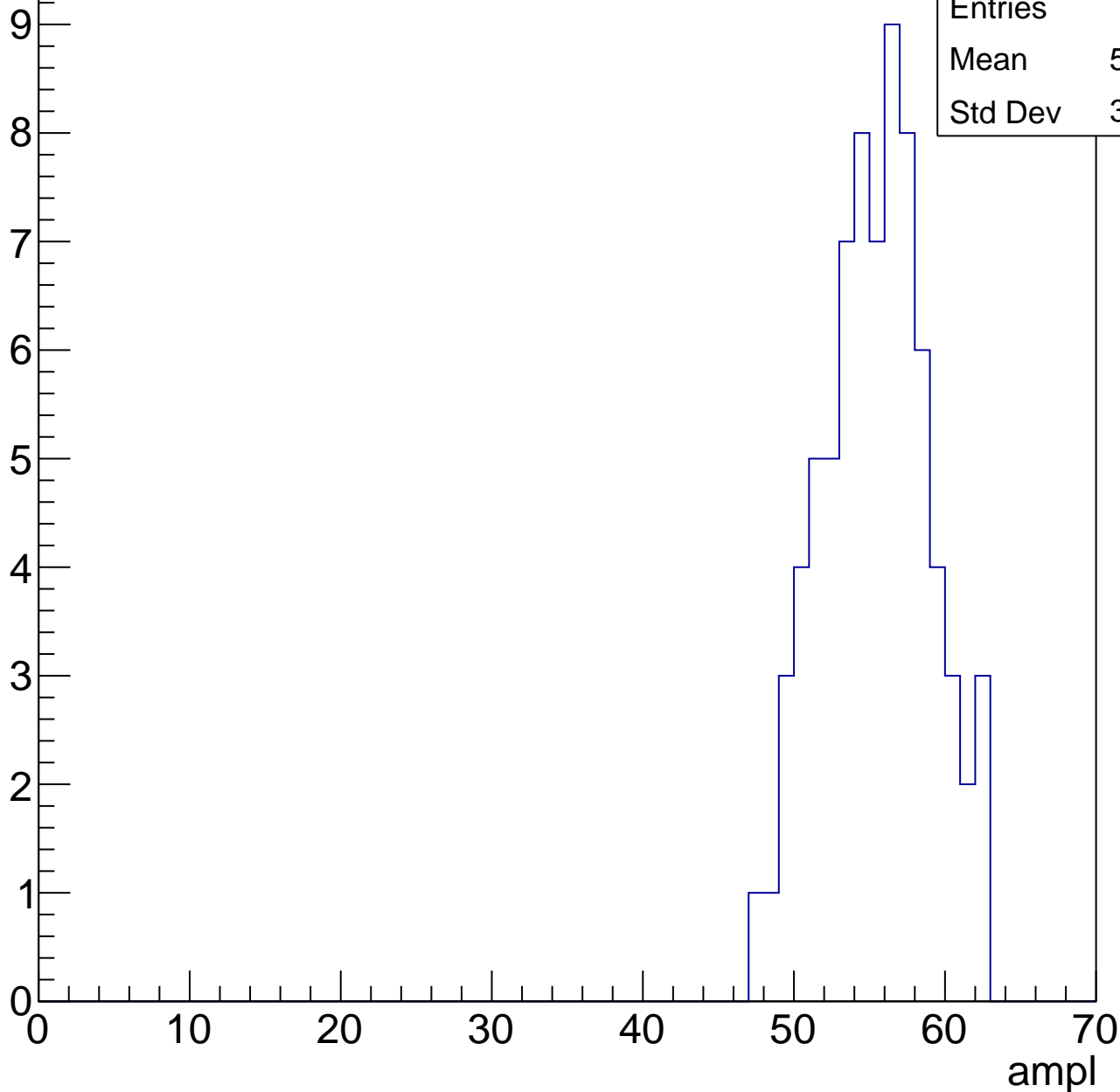
Entries	47
Mean	48.85
Std Dev	3.408



# B1L003S, U26-ch8, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

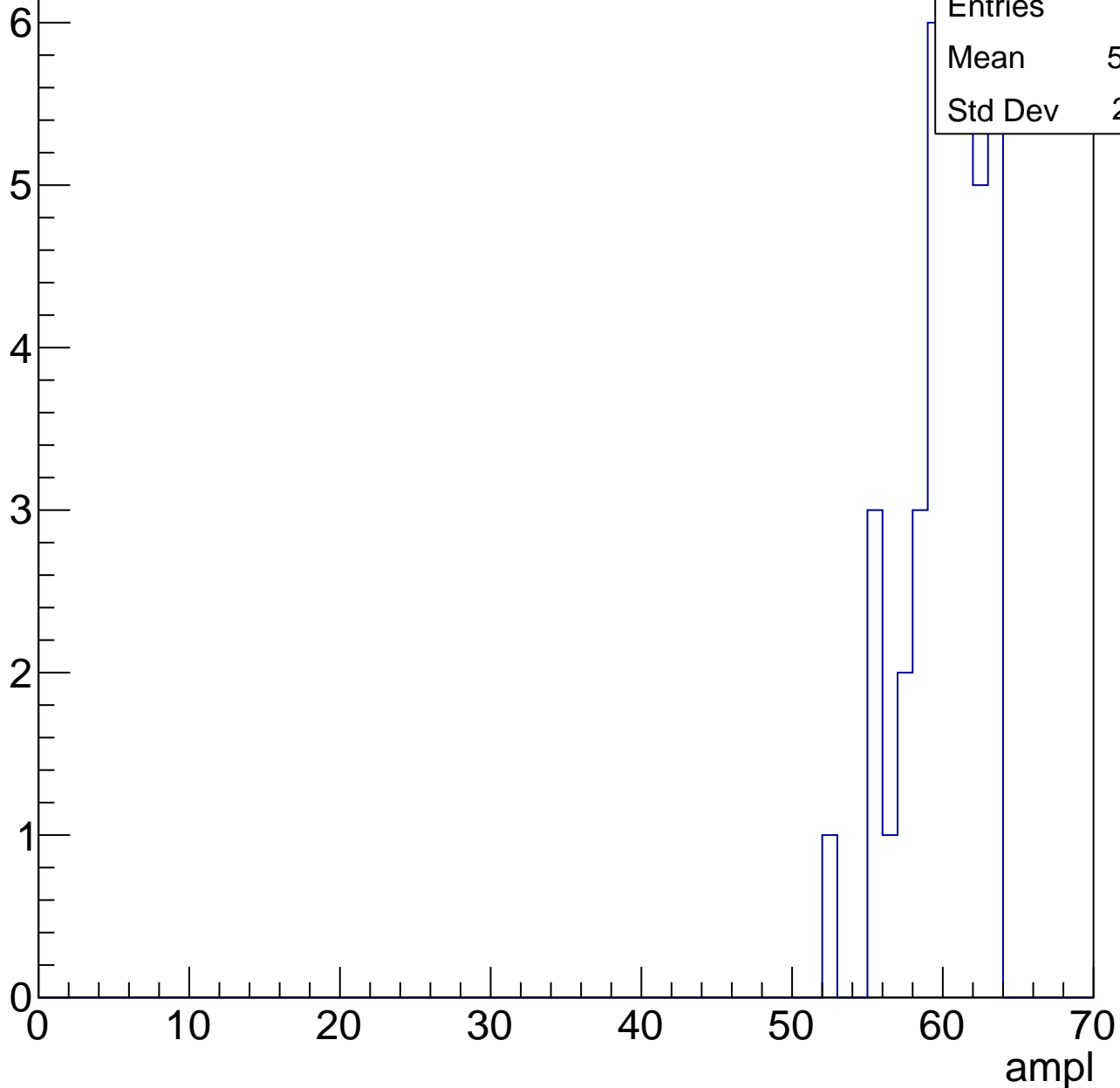
Entry



# B1L003S, U26-ch8, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

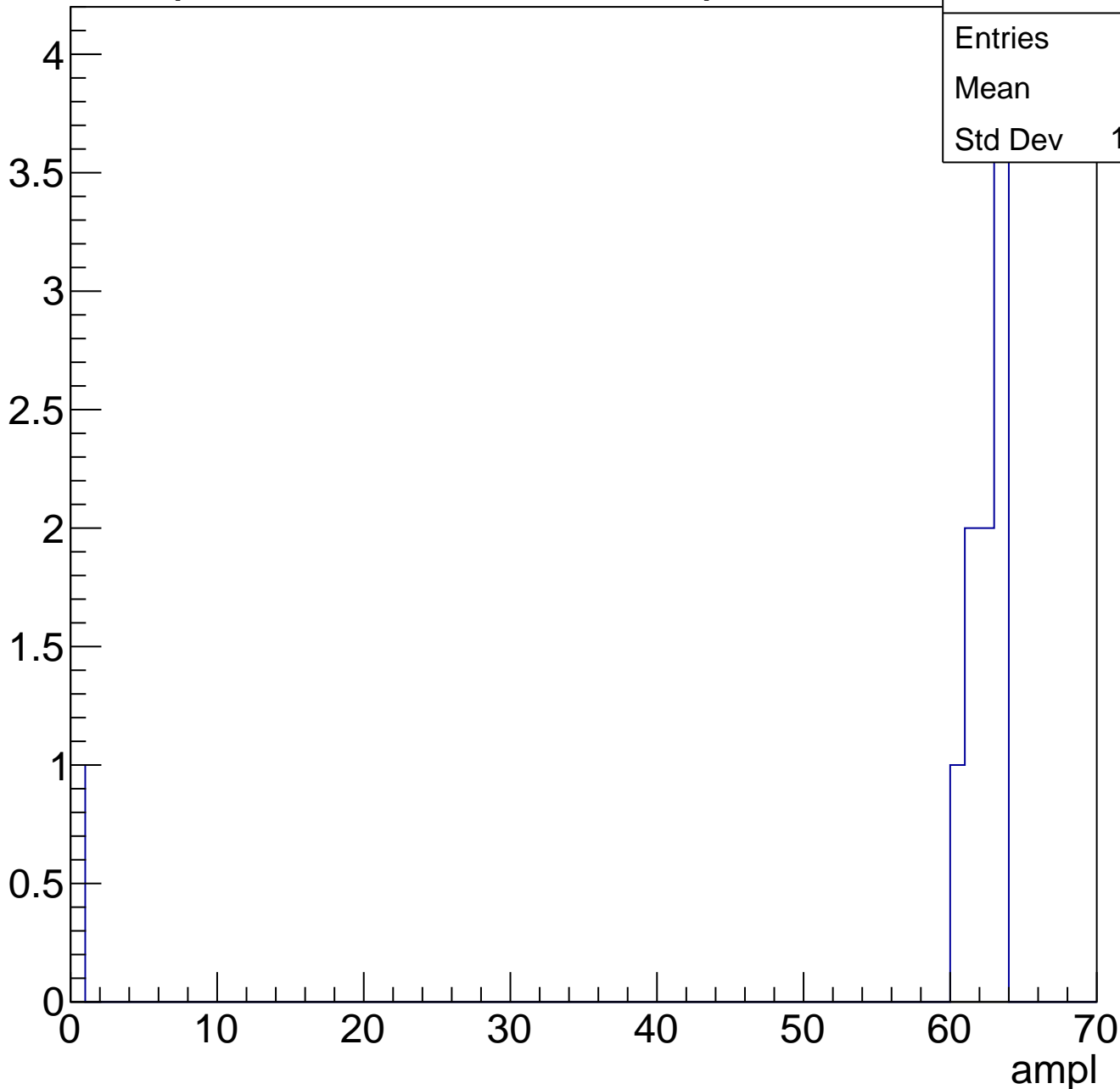
Entry



# B1L003S, U26-ch8, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch8, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U26-ch9, adc0

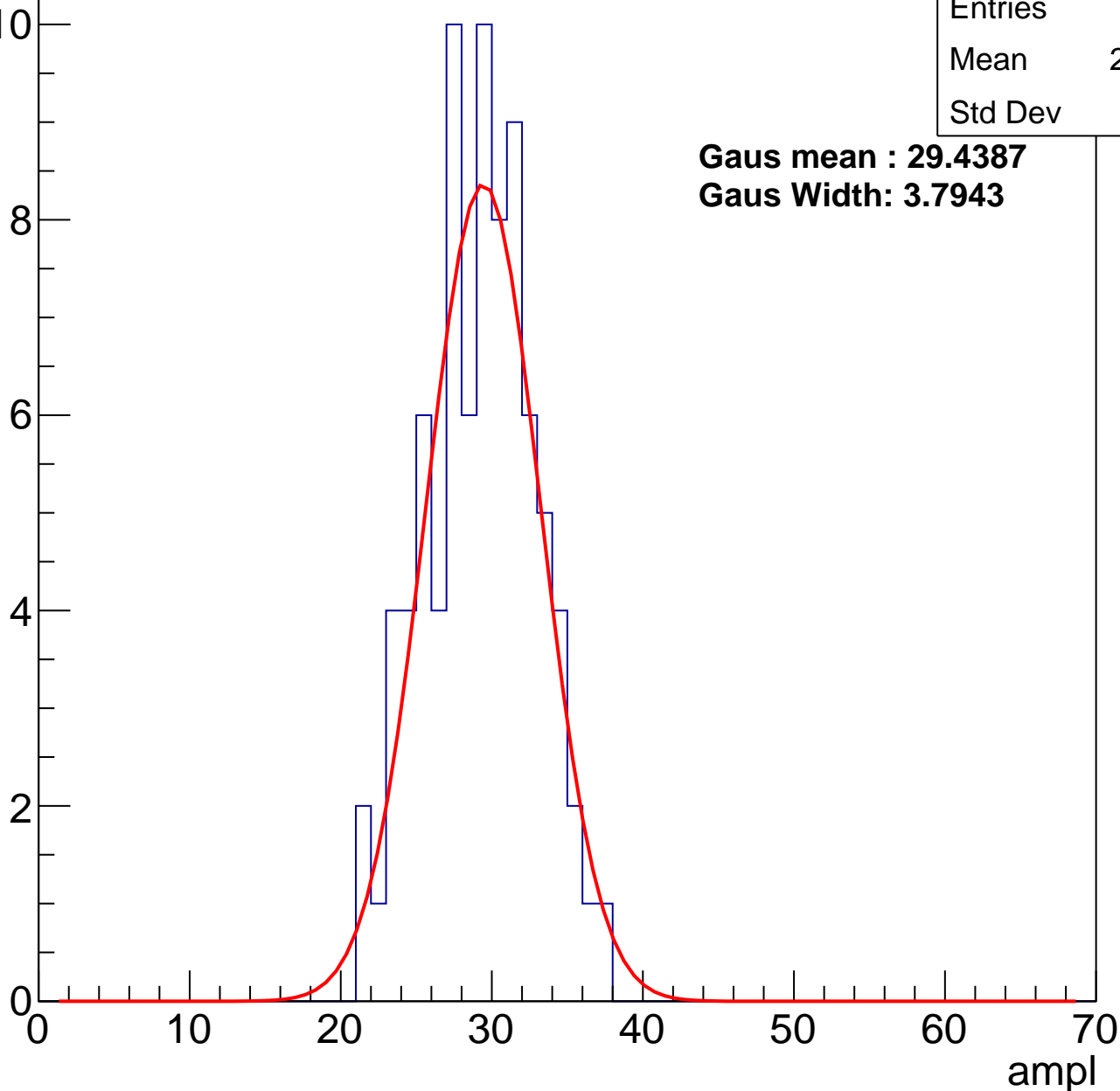
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	83
Mean	28.78
Std Dev	3.57

**Gaus mean : 29.4387**

**Gaus Width: 3.7943**



# B1L003S, U26-ch9, adc1

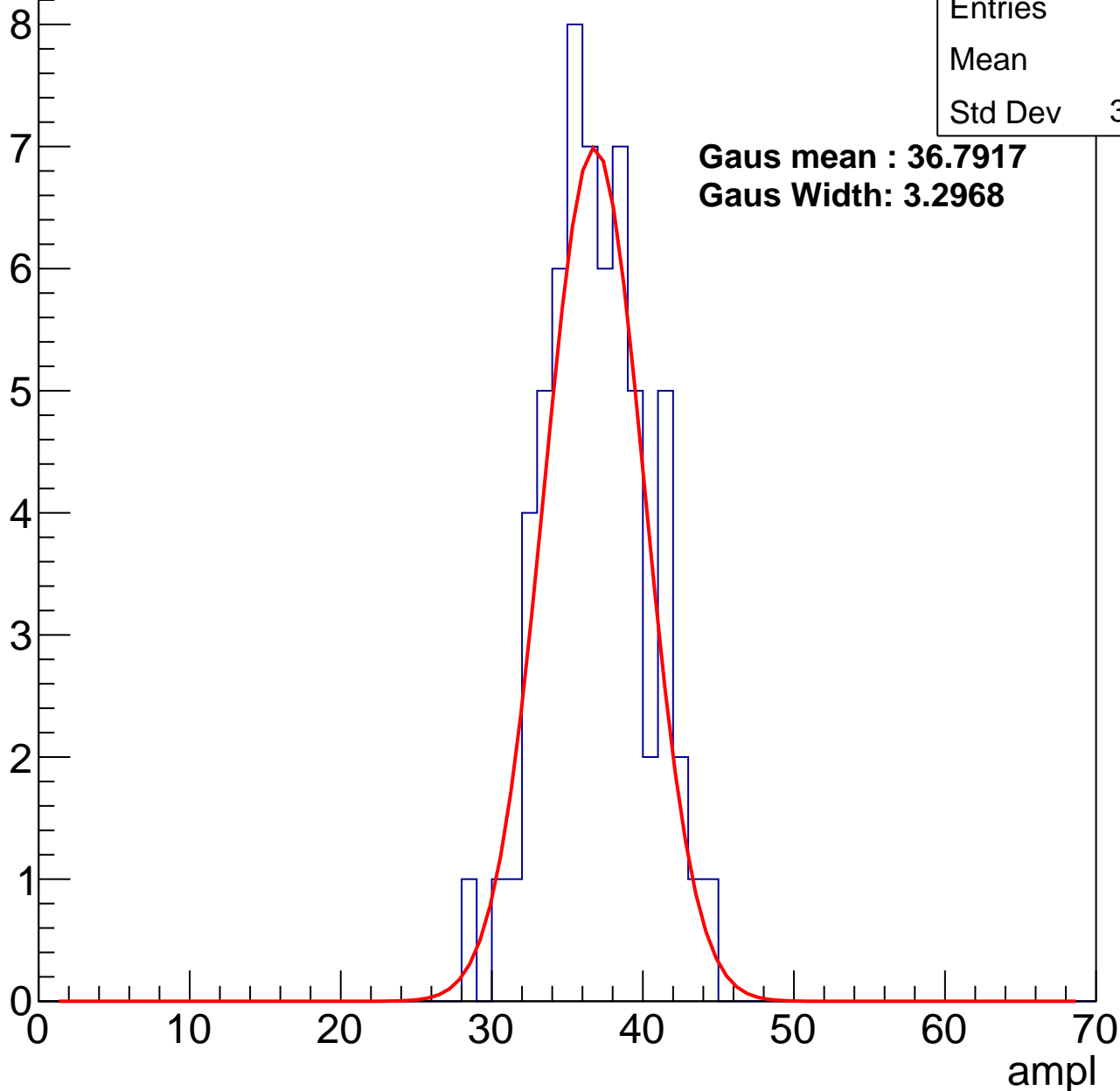
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	36.4
Std Dev	3.304

**Gaus mean : 36.7917**

**Gaus Width: 3.2968**

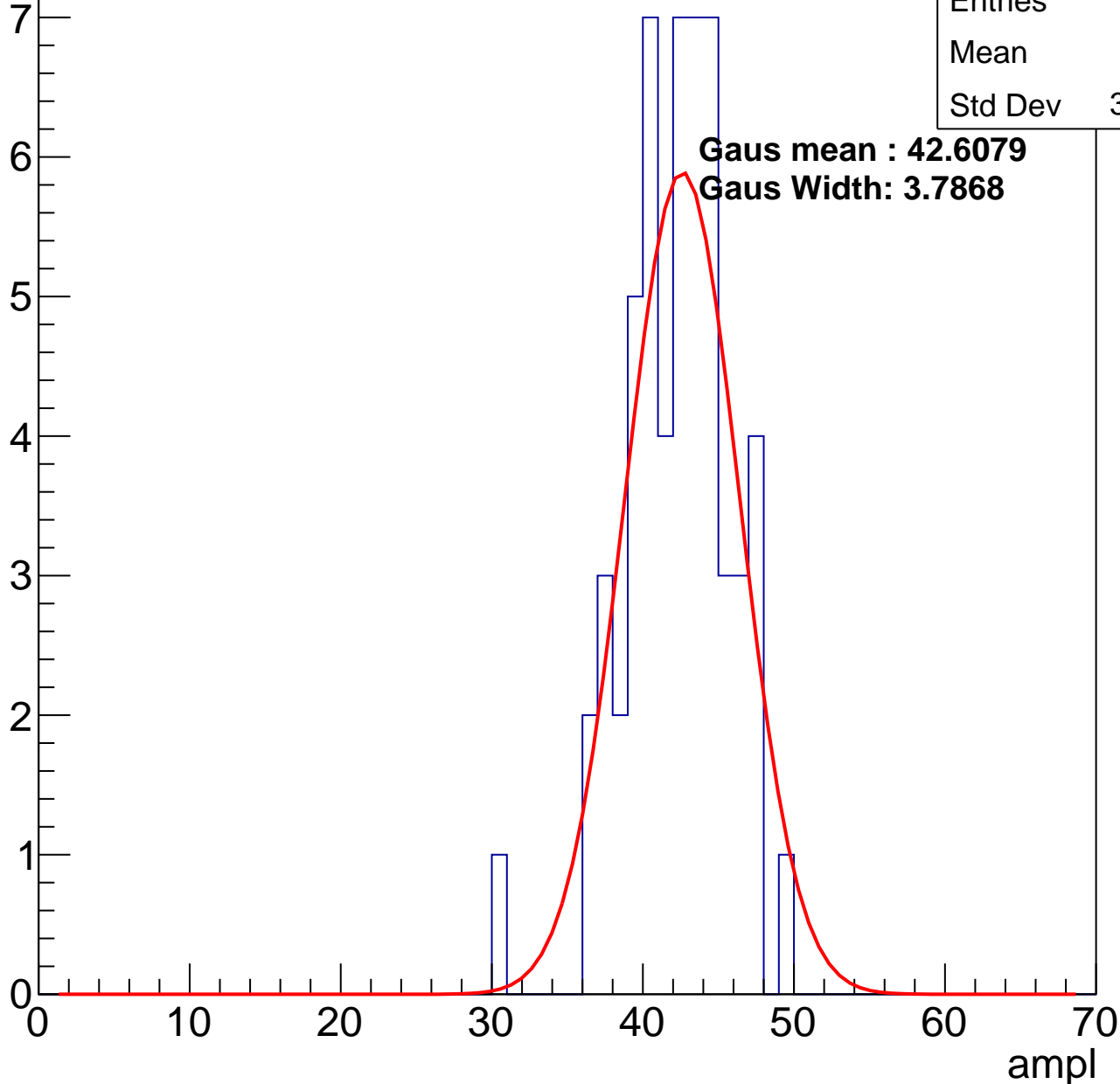


# B1L003S, U26-ch9, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	41.8
Std Dev	3.425

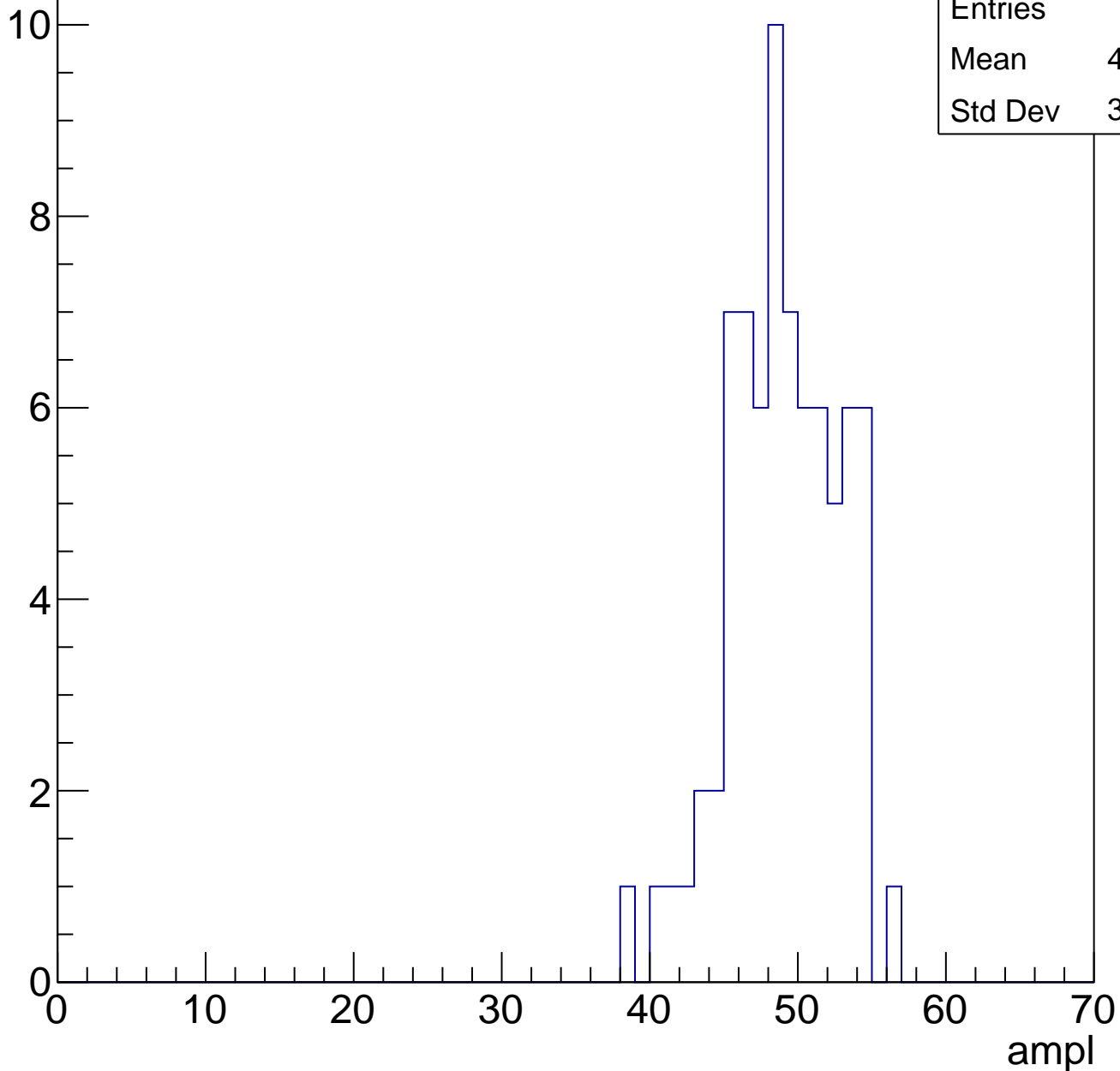


# B1L003S, U26-ch9, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	75
Mean	48.55
Std Dev	3.653

Entry

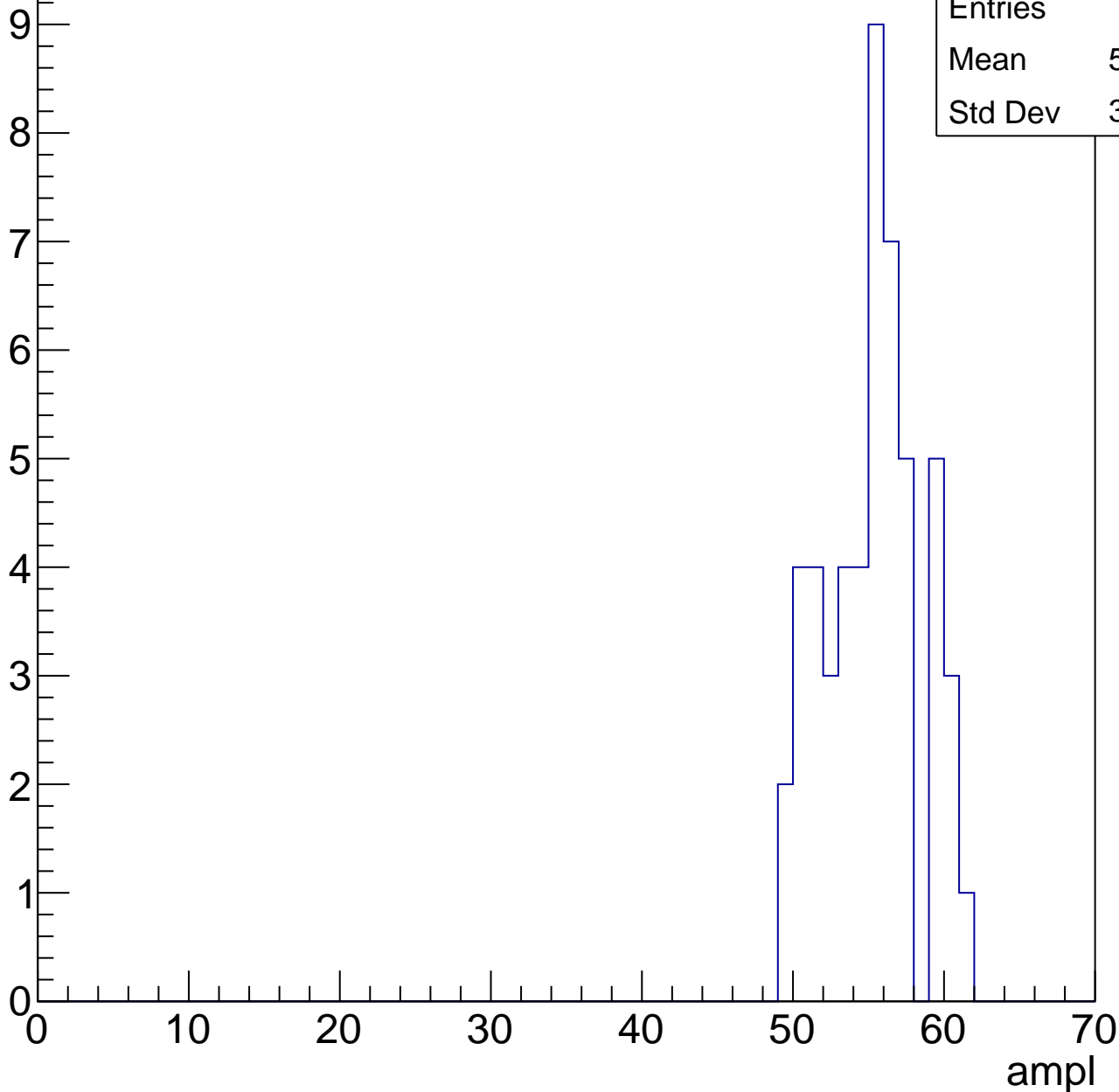


# B1L003S, U26-ch9, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	51
Mean	54.78
Std Dev	3.127



# B1L003S, U26-ch9, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

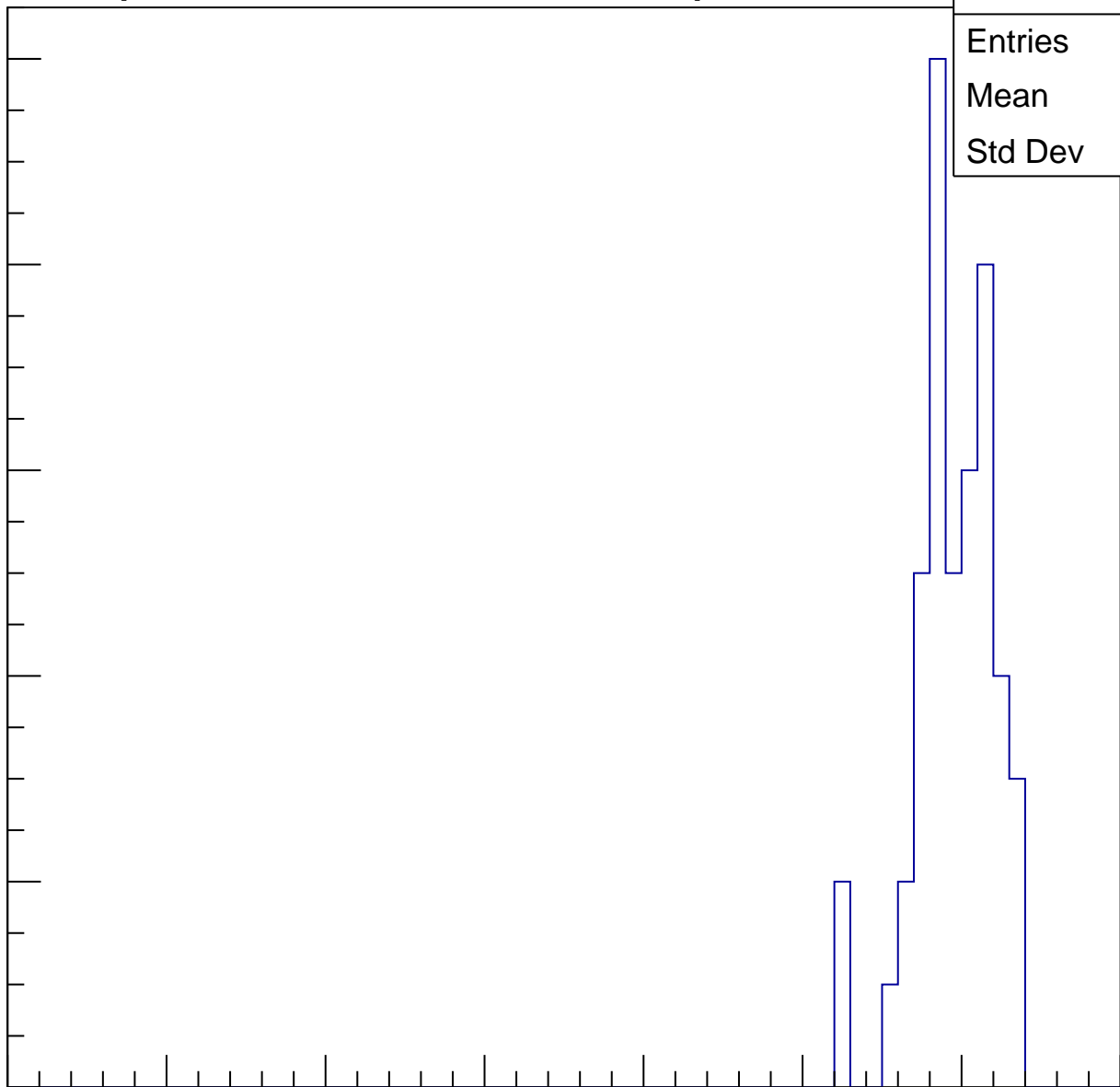
Entries	46
Mean	59.04
Std Dev	2.484

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

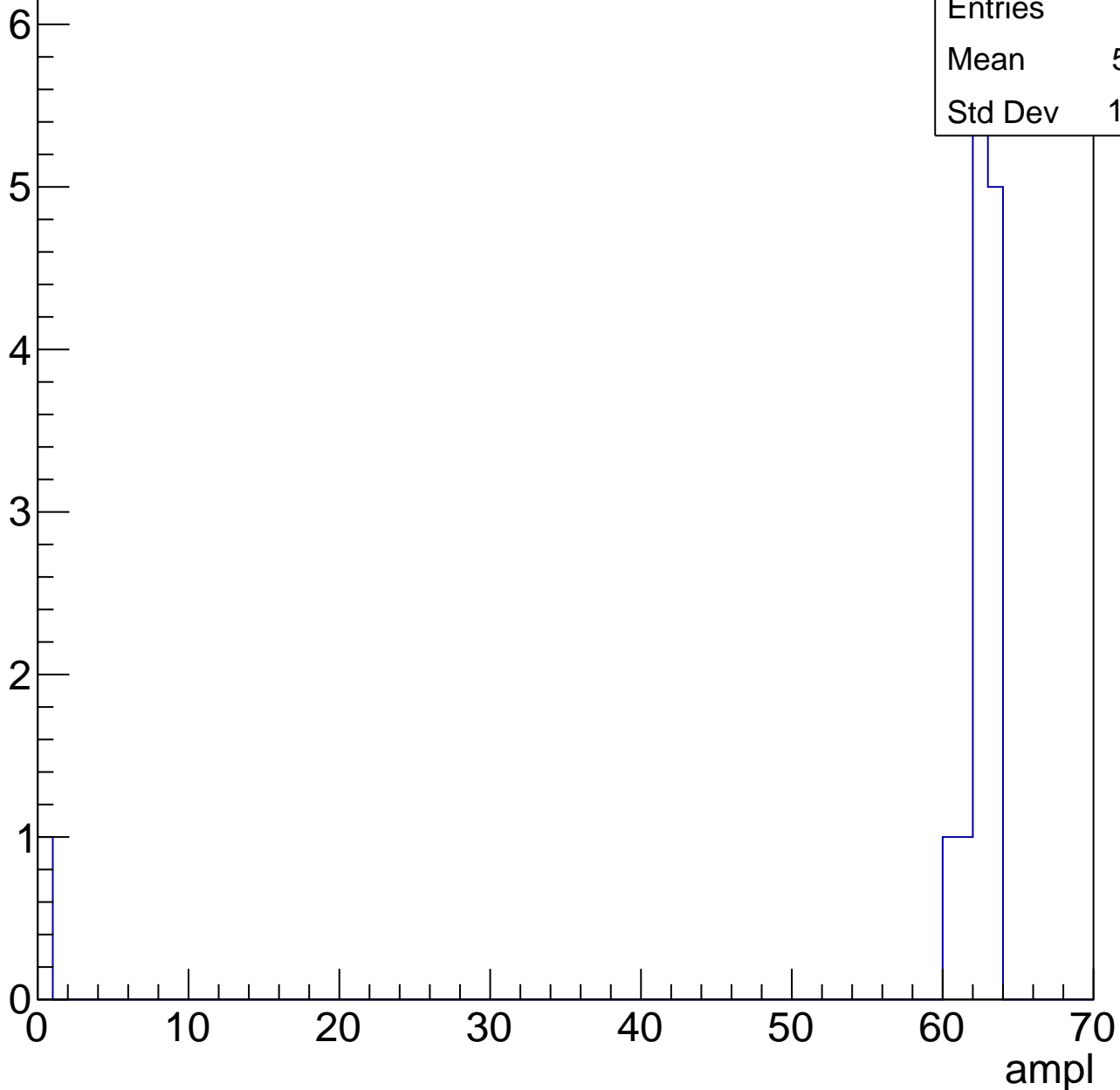


# B1L003S, U26-ch9, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	14
Mean	57.71
Std Dev	16.03

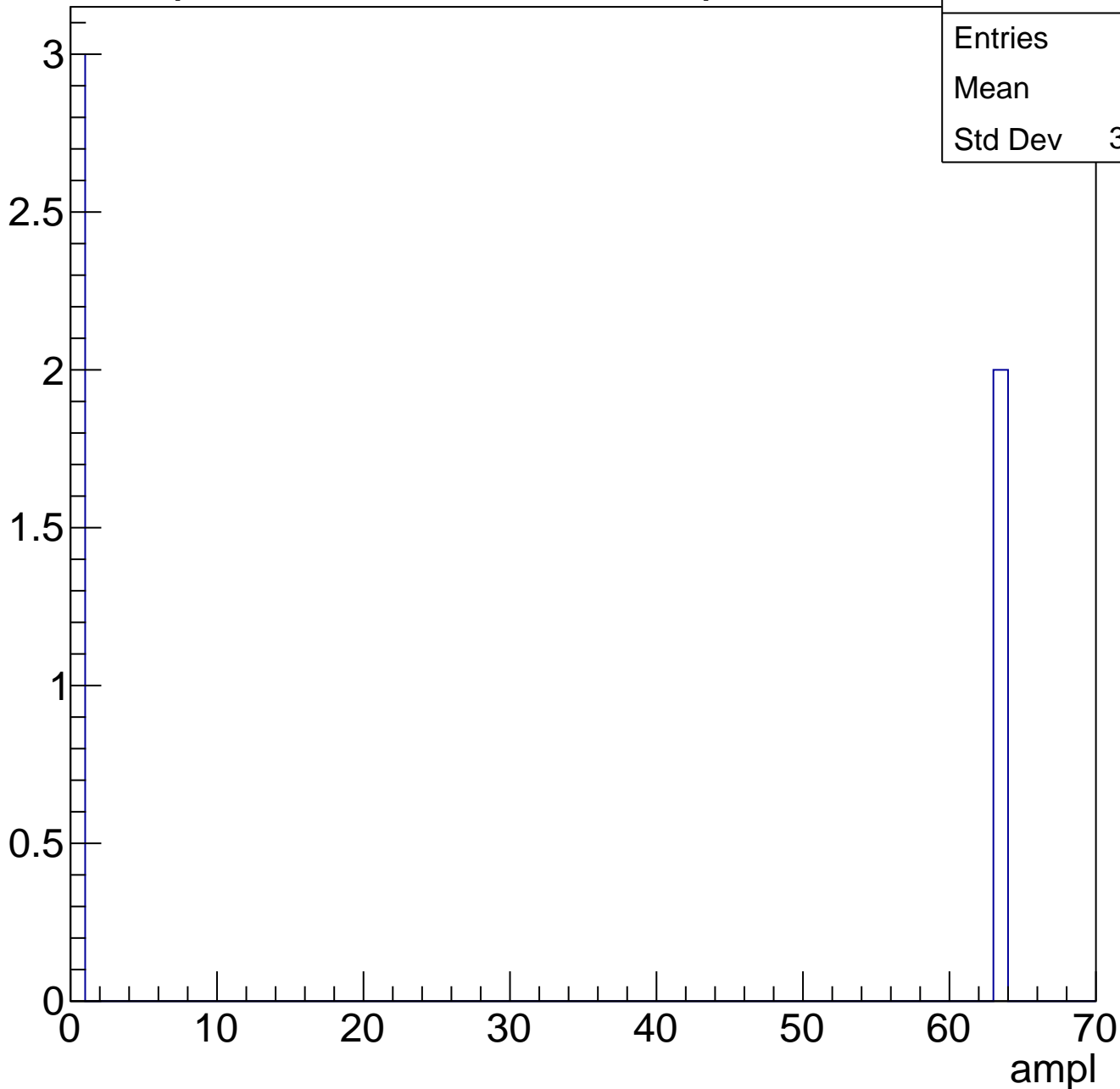




# B1L003S, U26-ch9, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U26-ch10, adc0

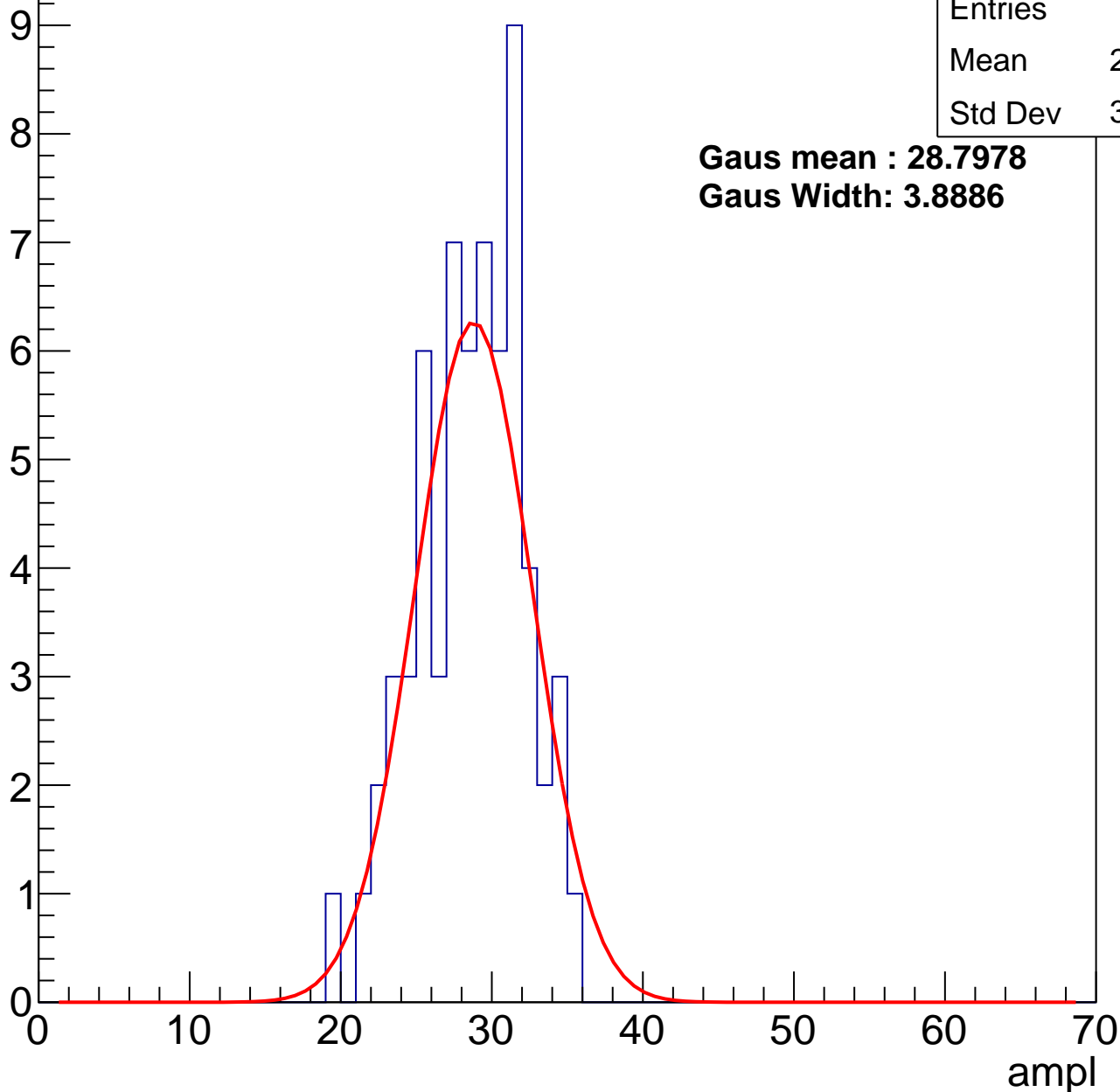
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	28.17
Std Dev	3.489

**Gaus mean : 28.7978**

**Gaus Width: 3.8886**



# B1L003S, U26-ch10, adc1

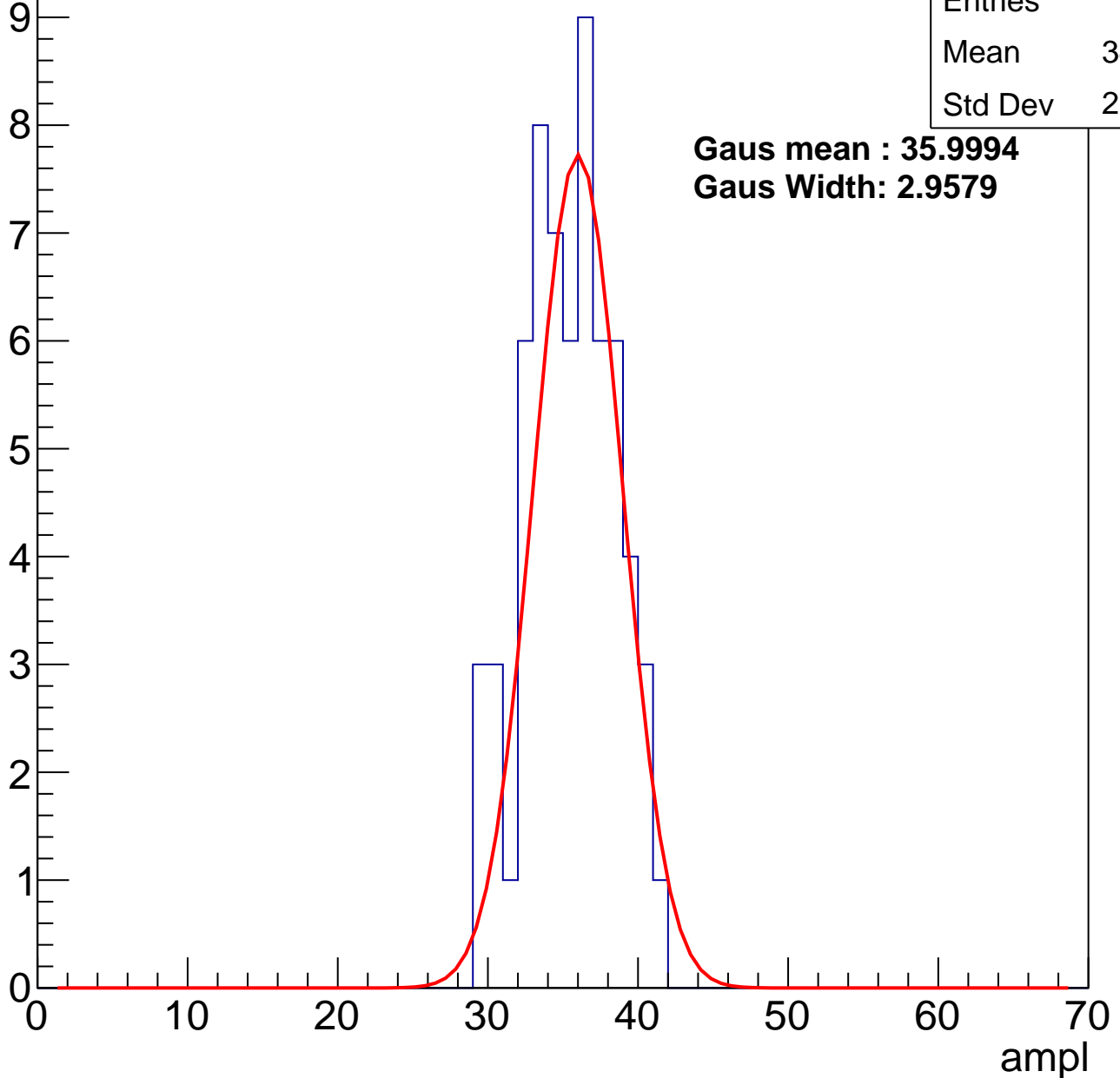
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	34.97
Std Dev	2.965

**Gaus mean : 35.9994**

**Gaus Width: 2.9579**



# B1L003S, U26-ch10, adc2

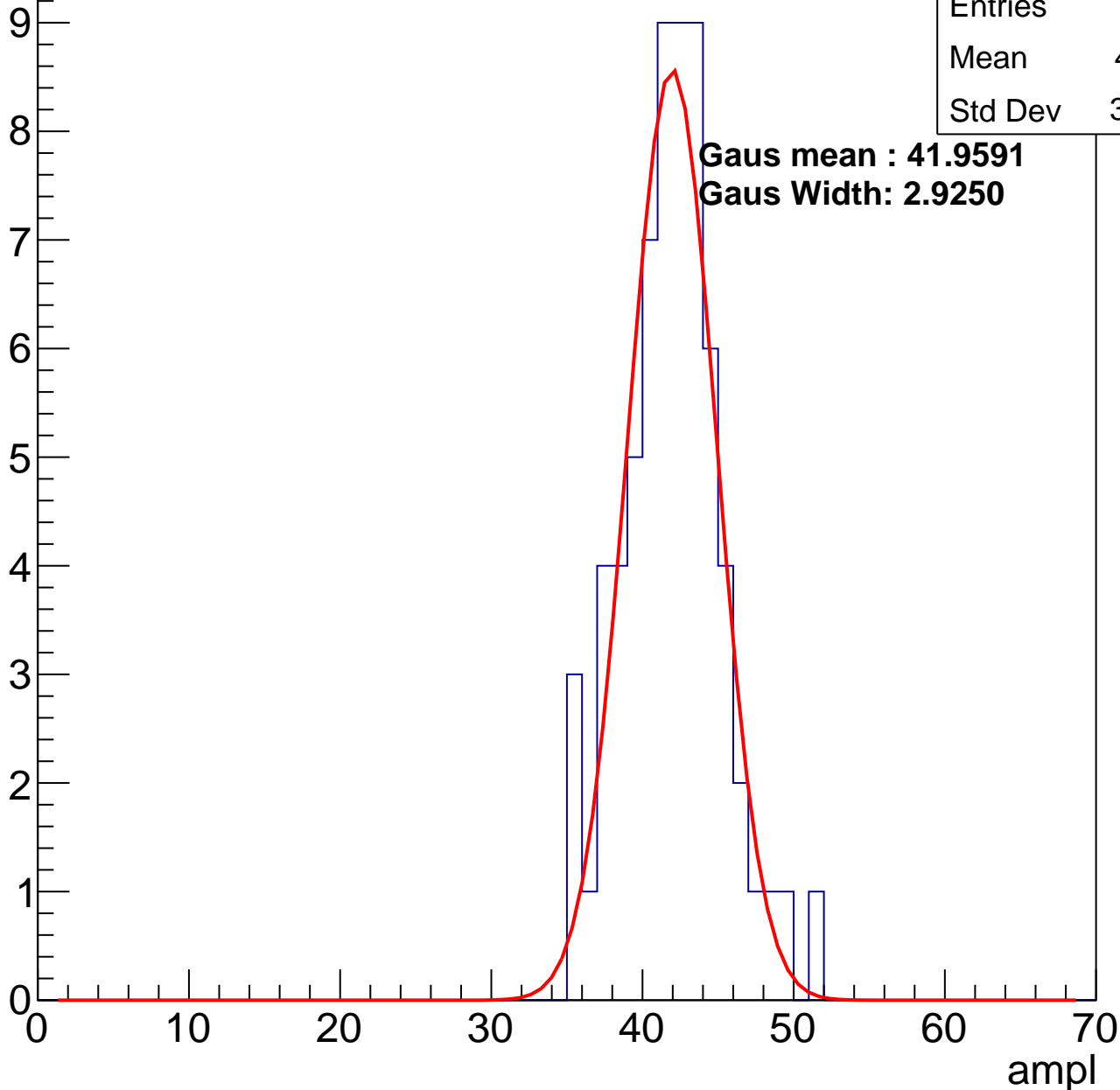
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	41.51
Std Dev	3.243

**Gaus mean : 41.9591**

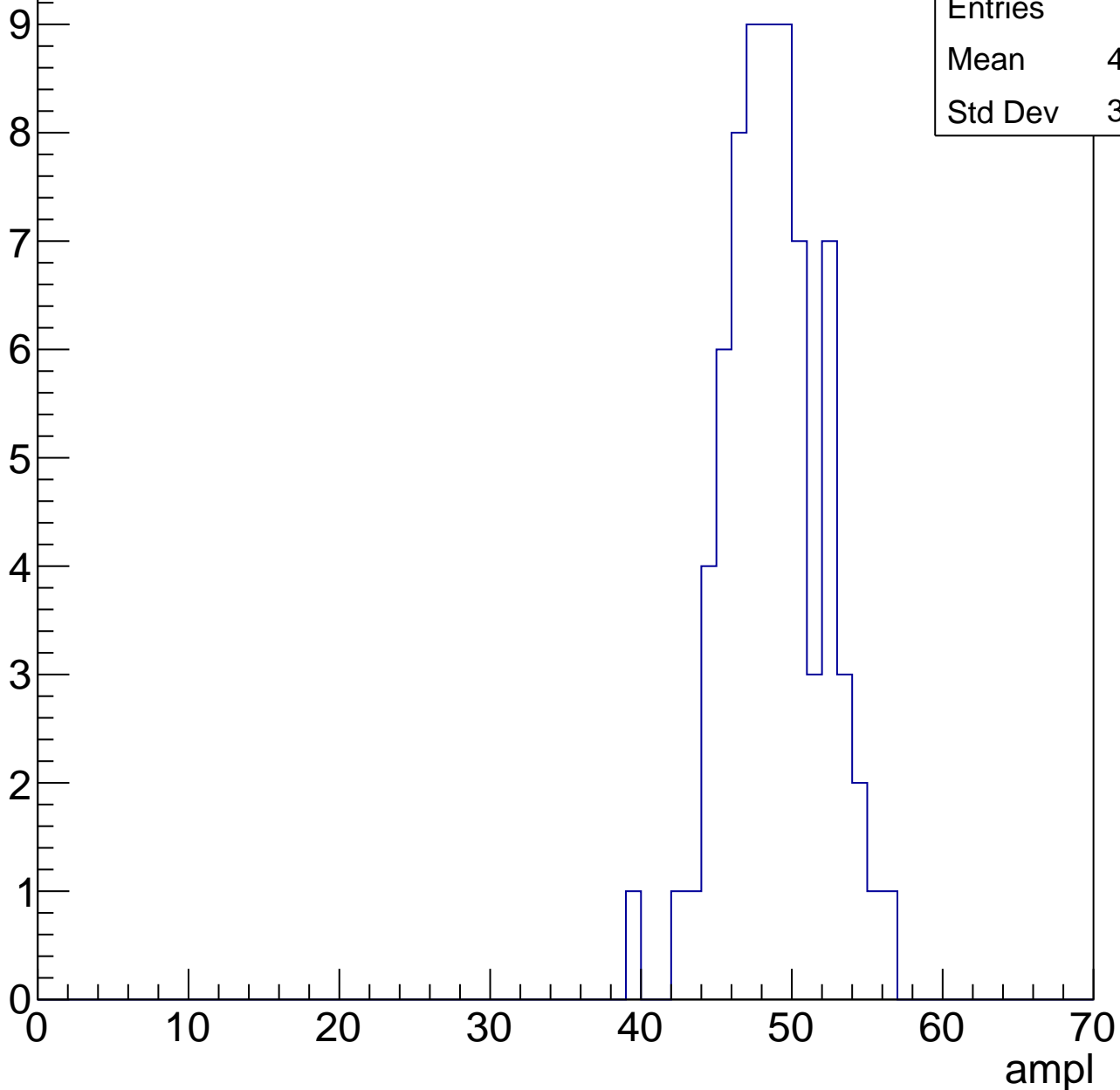
**Gaus Width: 2.9250**



# B1L003S, U26-ch10, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

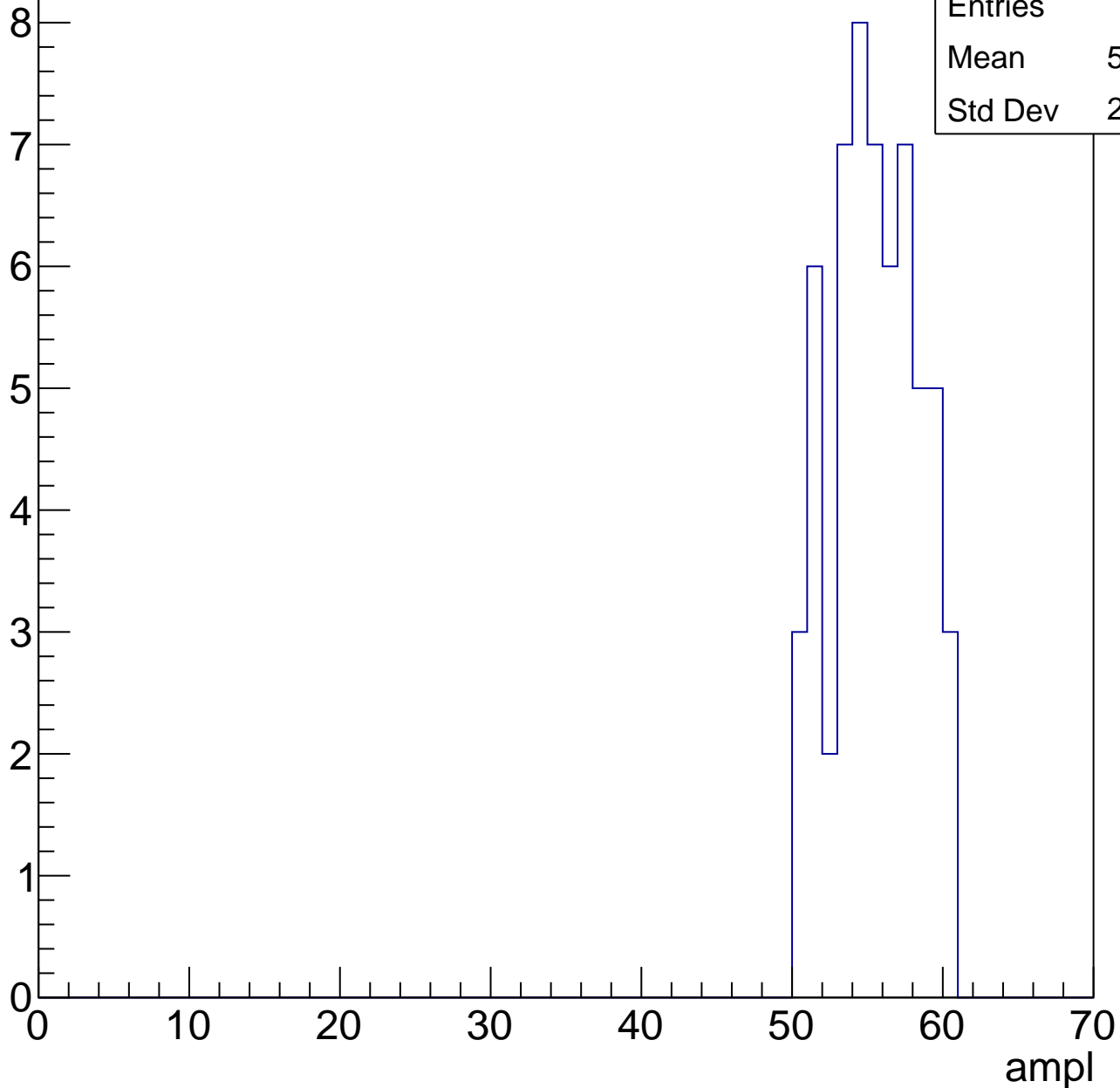


Entries	72
Mean	48.32
Std Dev	3.183

# B1L003S, U26-ch10, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

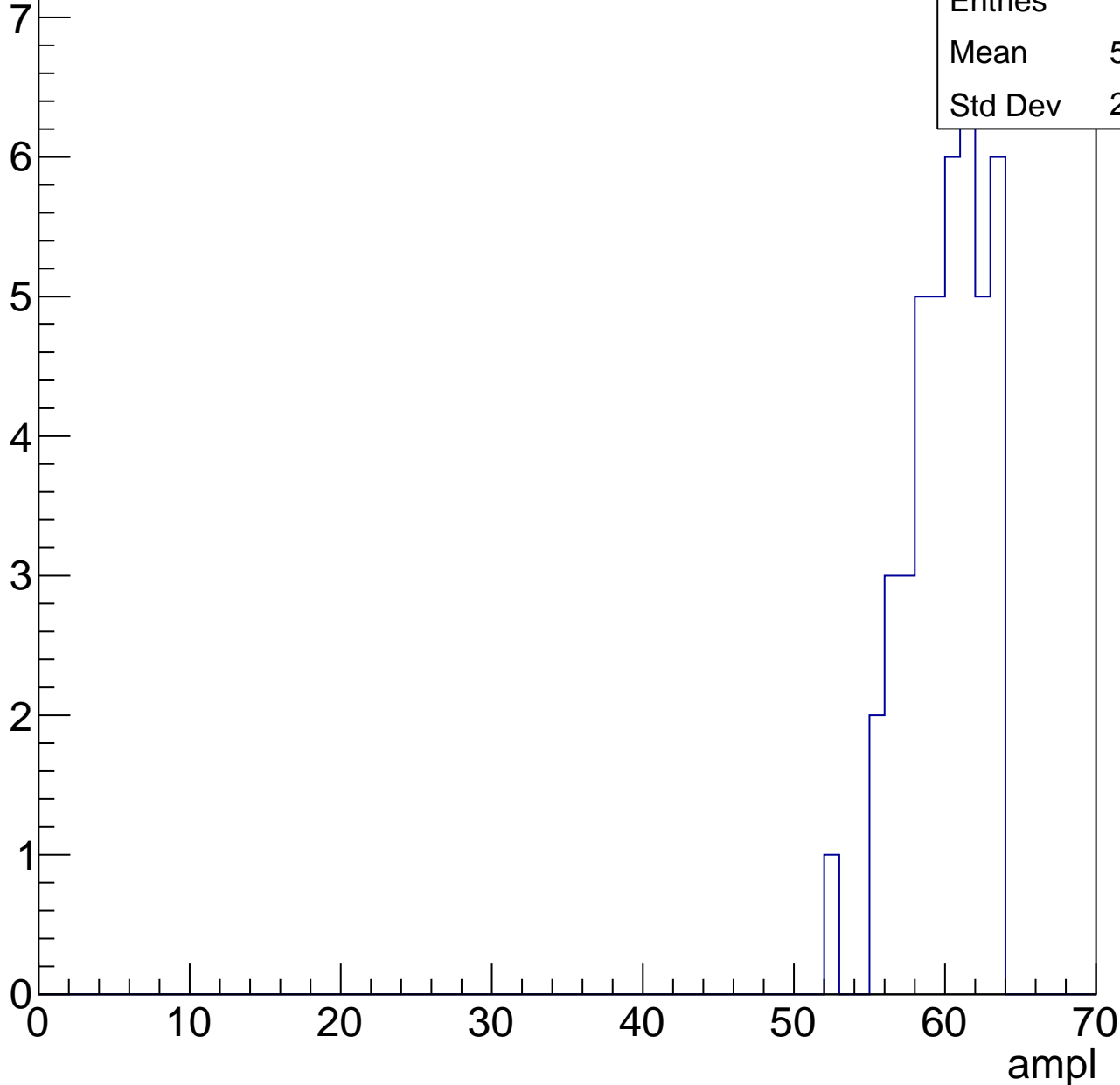


# B1L003S, U26-ch10, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	43
Mean	59.56
Std Dev	2.582

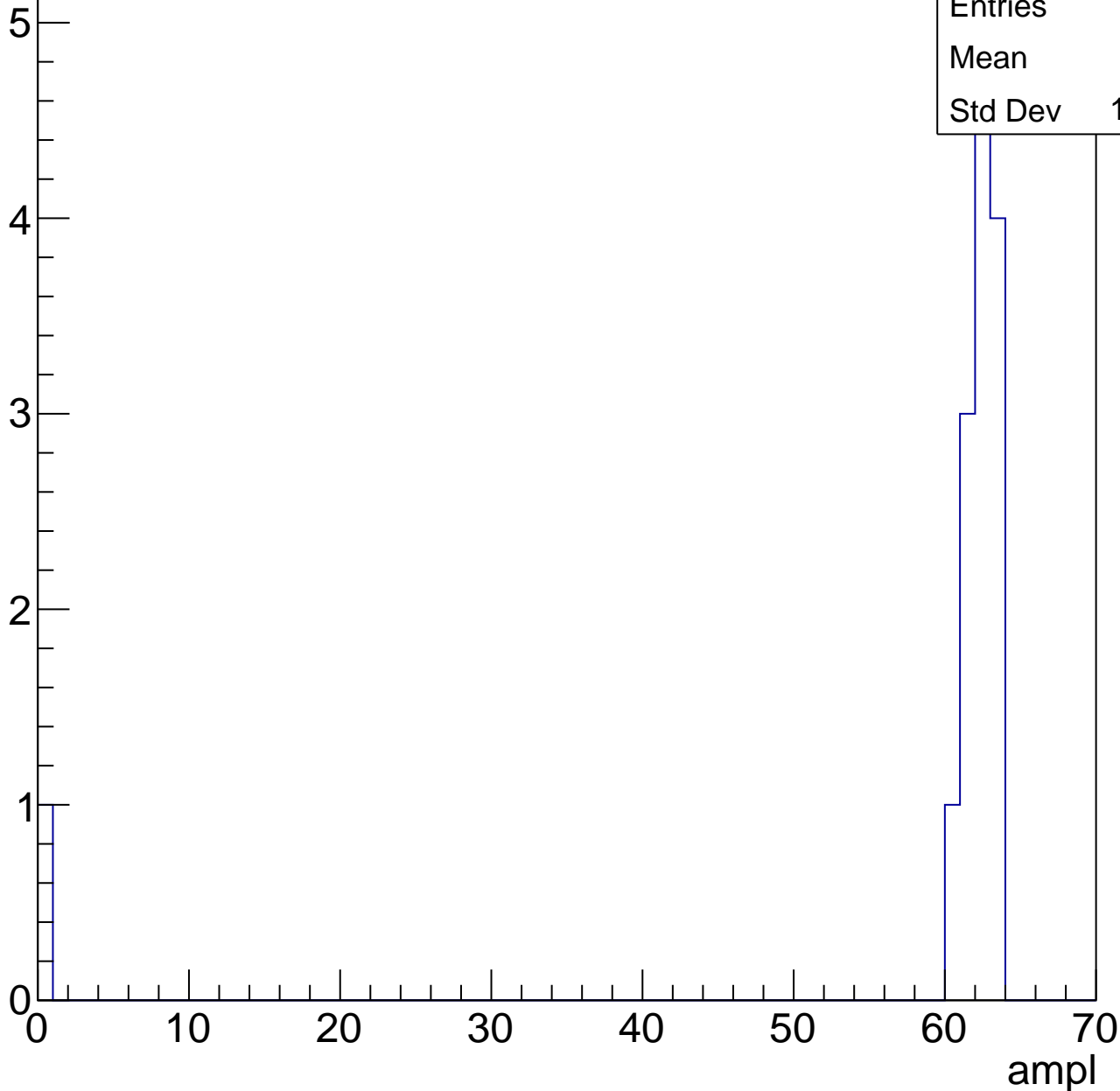


# B1L003S, U26-ch10, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	14
Mean	57.5
Std Dev	15.97





# B1L003S, U26-ch10, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U26-ch11, adc0

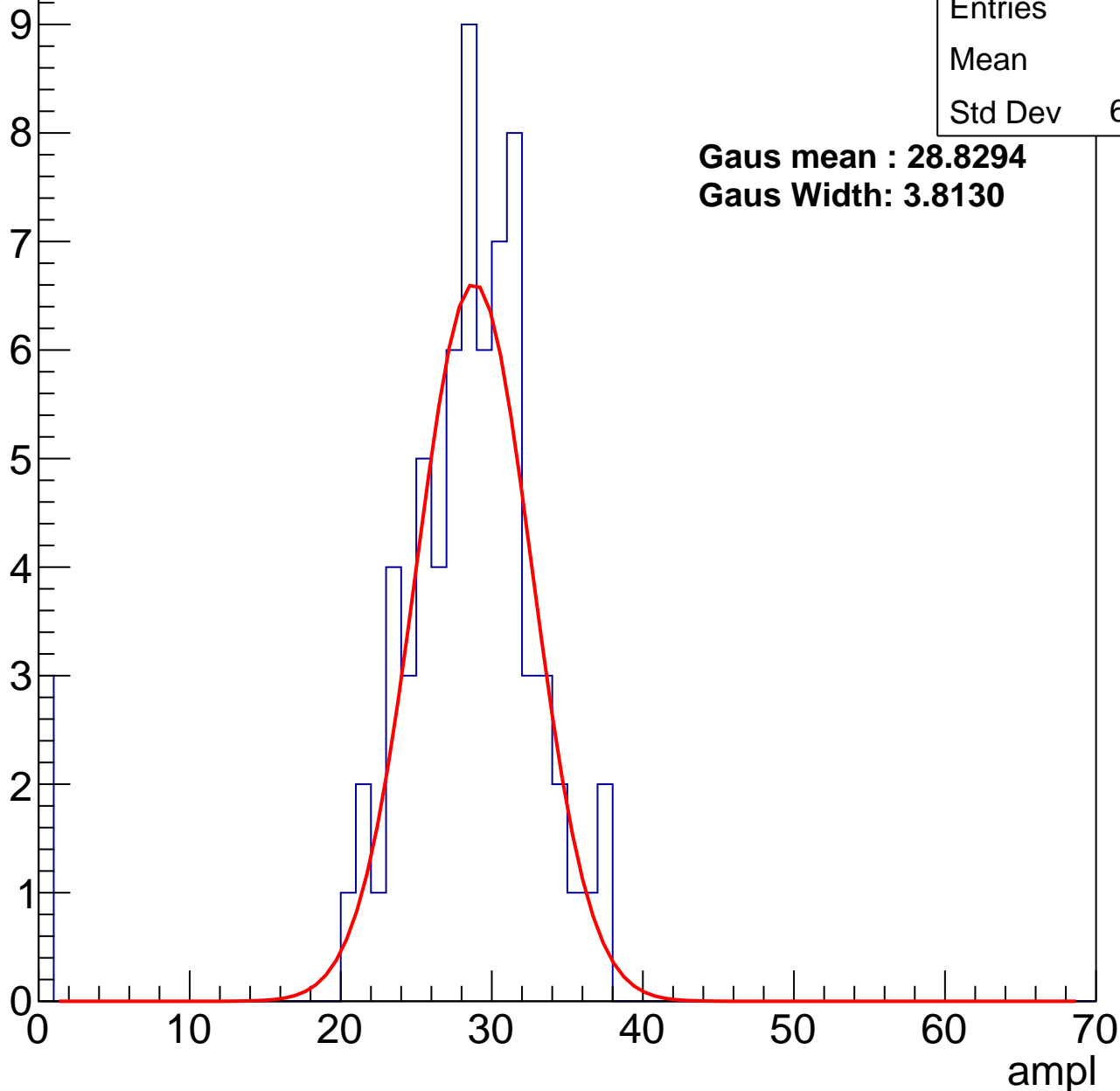
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	71
Mean	27.2
Std Dev	6.813

**Gaus mean : 28.8294**

**Gaus Width: 3.8130**



# B1L003S, U26-ch11, adc1

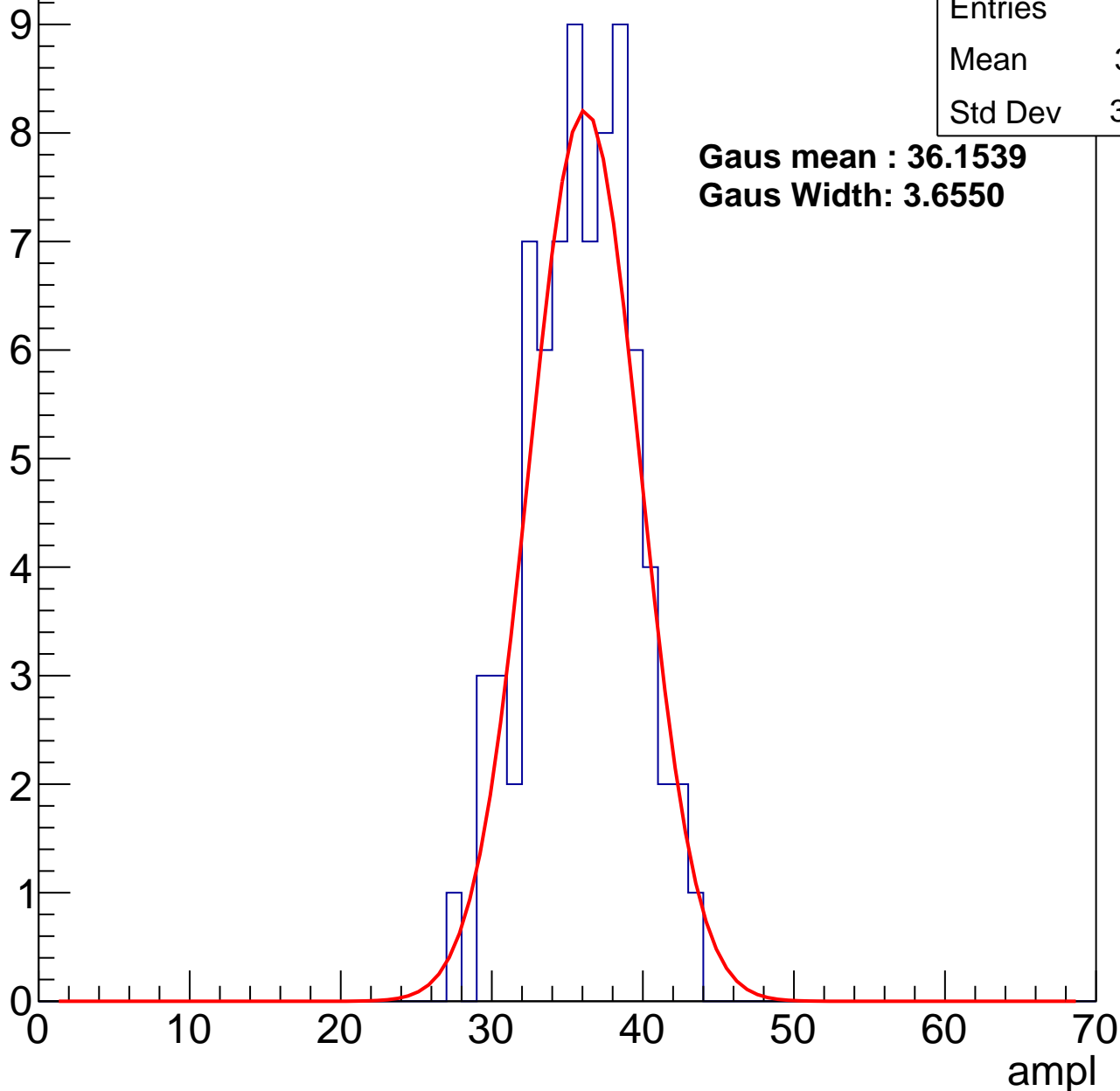
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	77
Mean	35.51
Std Dev	3.425

**Gaus mean : 36.1539**

**Gaus Width: 3.6550**



# B1L003S, U26-ch11, adc2

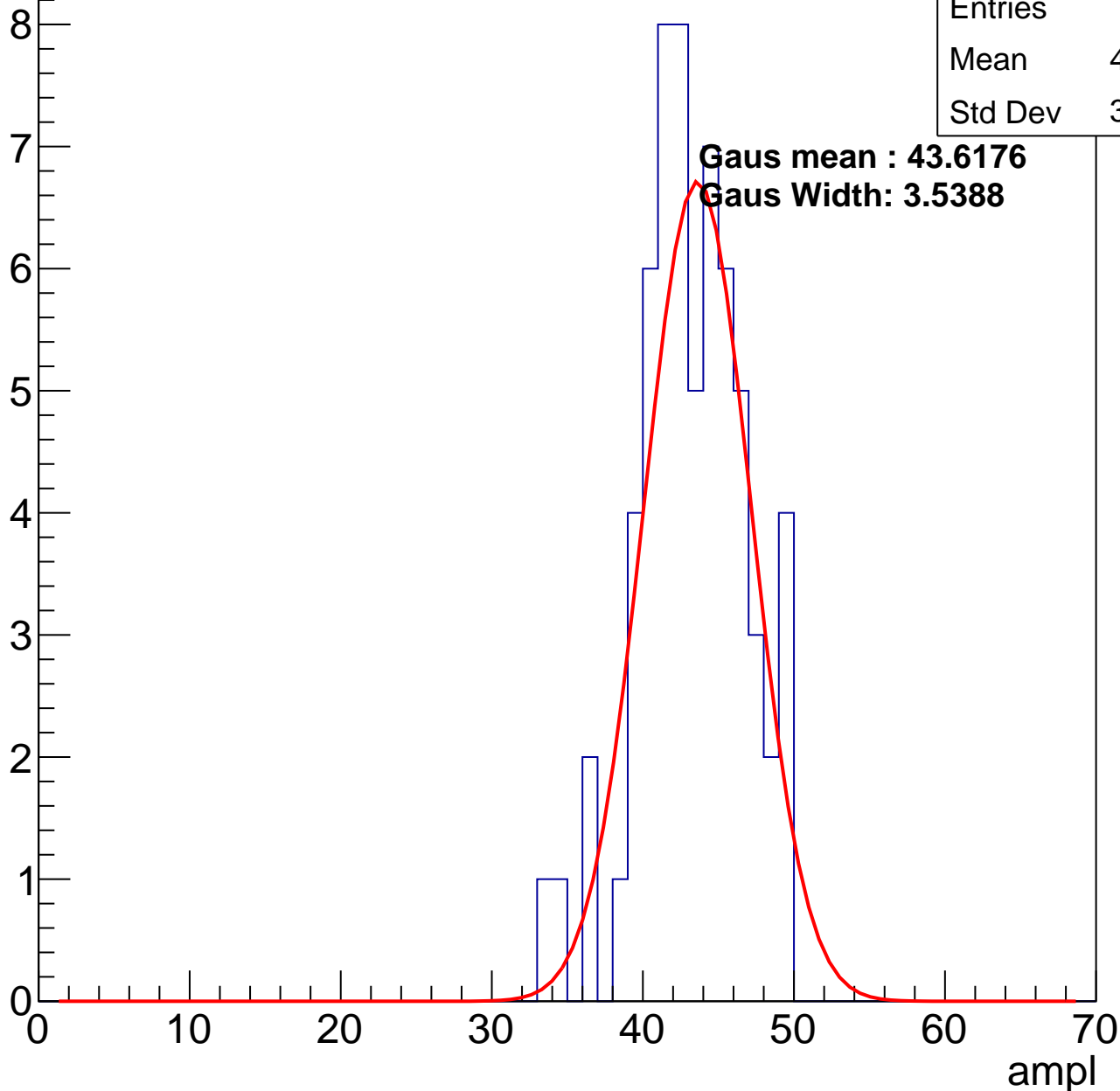
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	42.75
Std Dev	3.509

**Gaus mean : 43.6176**

**Gaus Width: 3.5388**

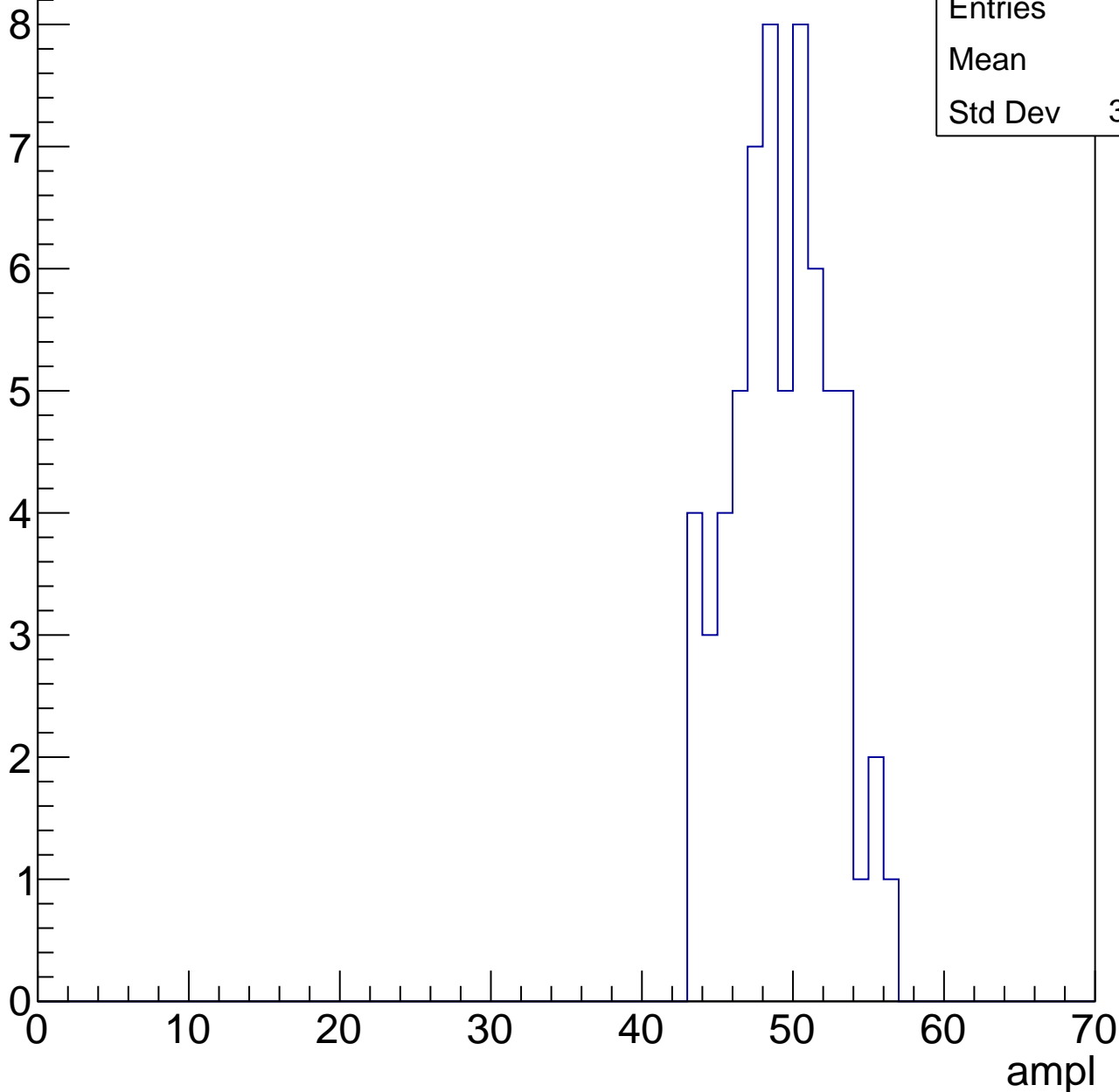


# B1L003S, U26-ch11, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	48.8
Std Dev	3.222

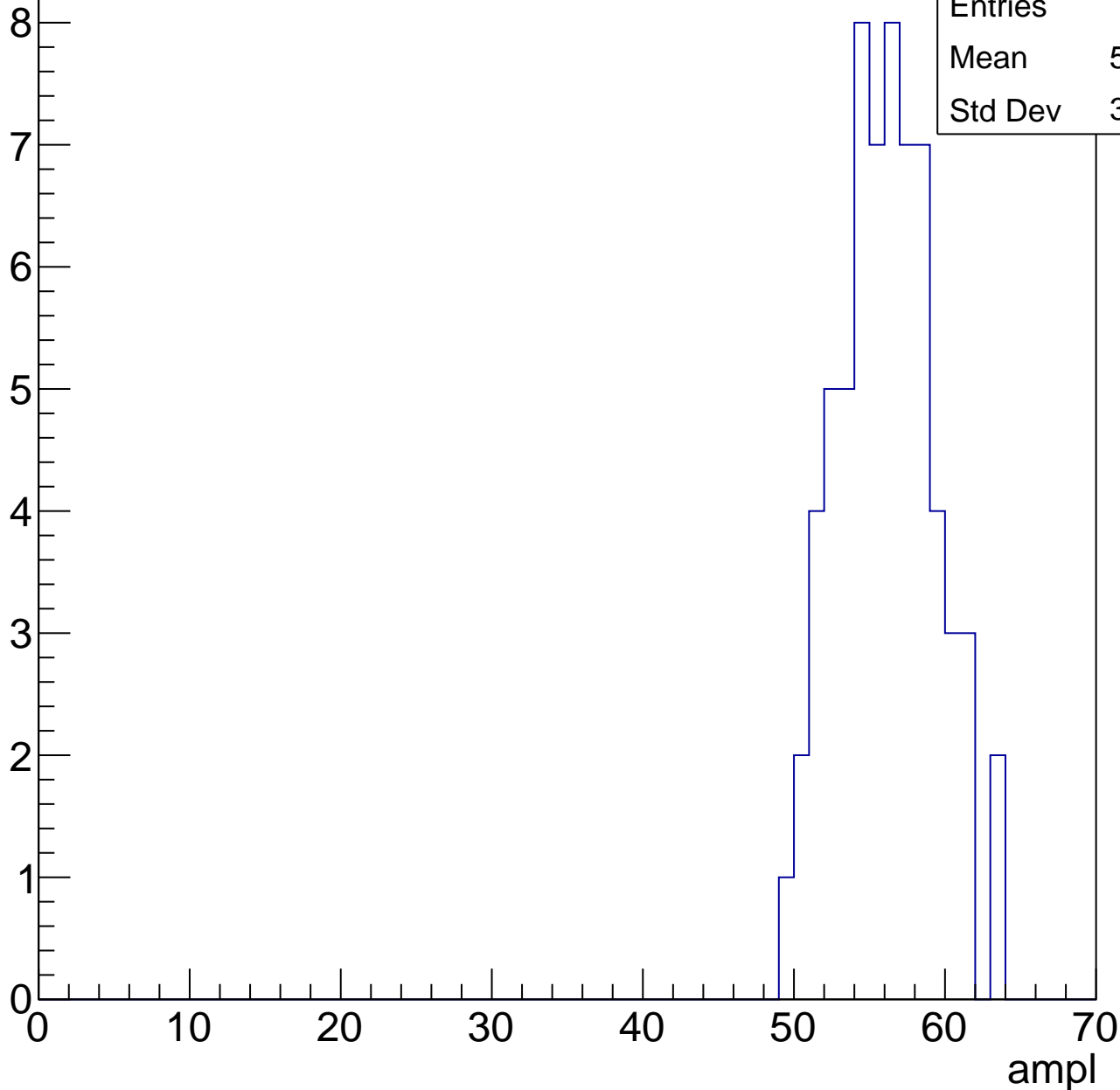


# B1L003S, U26-ch11, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	55.65
Std Dev	3.184



# B1L003S, U26-ch11, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

7

6

5

4

3

2

1

0

Entries

37

Mean

60.05

Std Dev

2.37

0

10

20

30

40

50

60

70

ampl

0

10

20

30

40

50

60

70

ampl

# B1L003S, U26-ch11, adc6

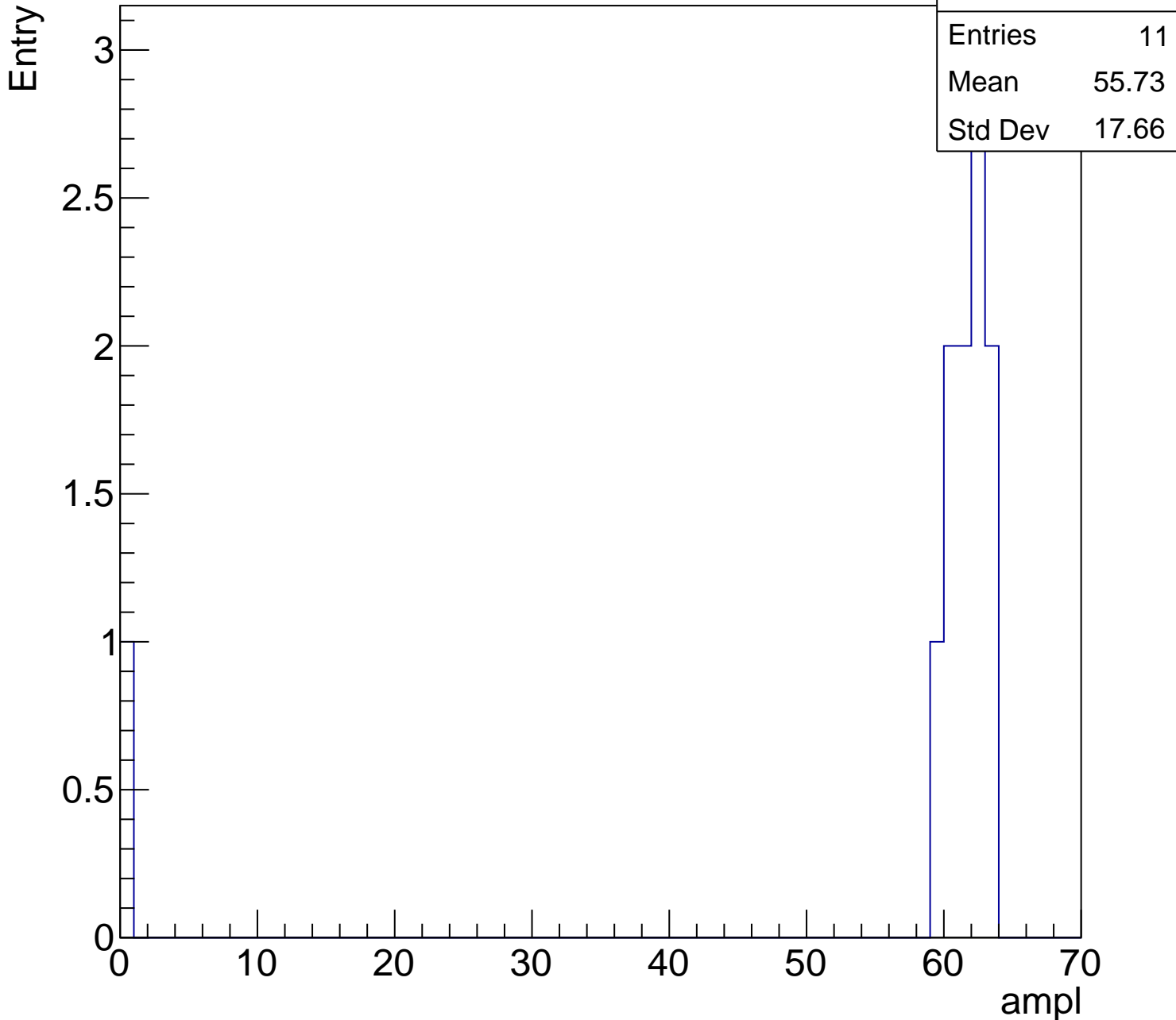
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

3  
2.5  
2  
1.5  
1  
0.5  
0

Entries	11
Mean	55.73
Std Dev	17.66

ampl





# B1L003S, U26-ch11, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U26-ch12, adc0

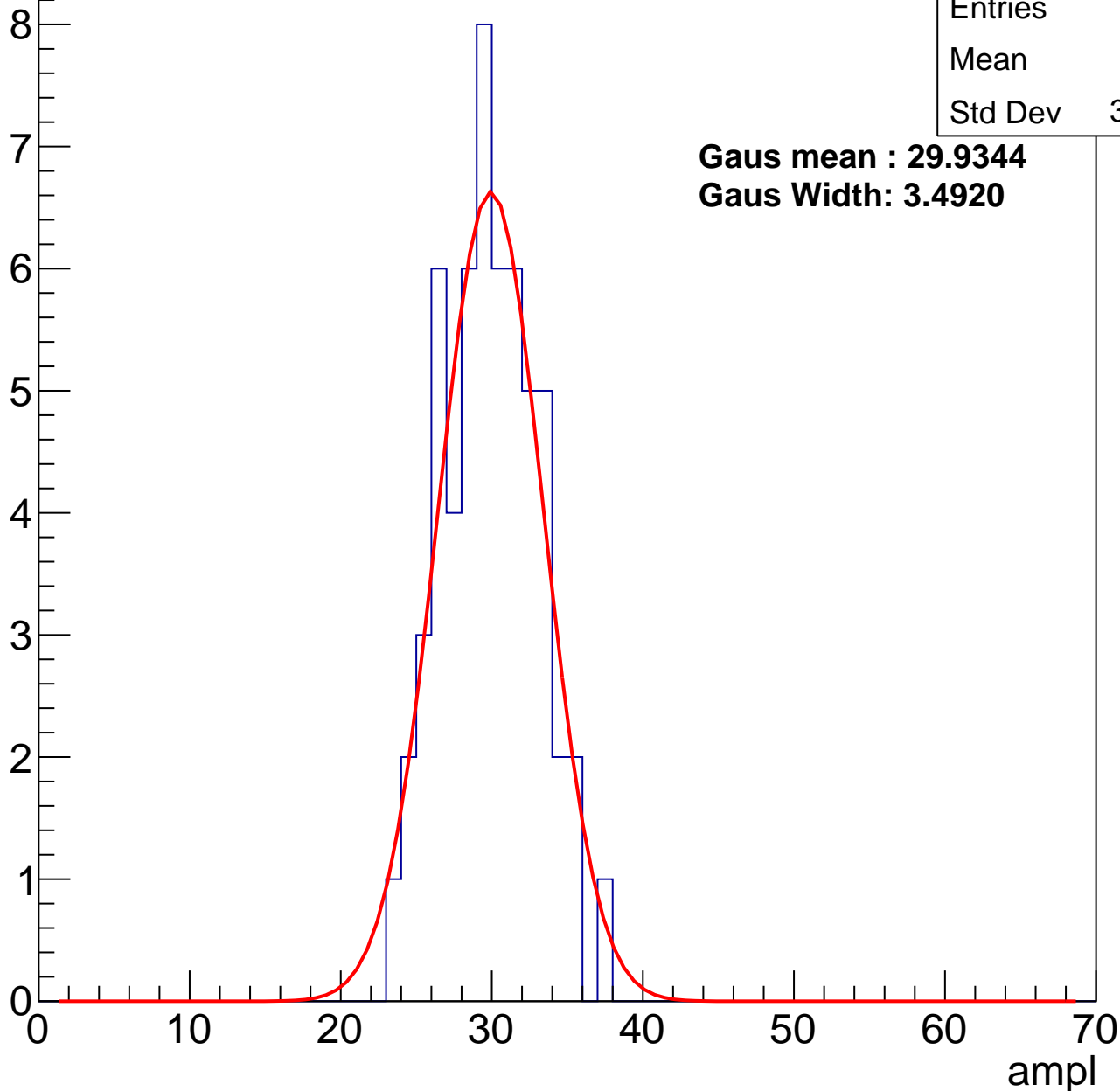
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	29.4
Std Dev	3.083

**Gaus mean : 29.9344**

**Gaus Width: 3.4920**



# B1L003S, U26-ch12, adc1

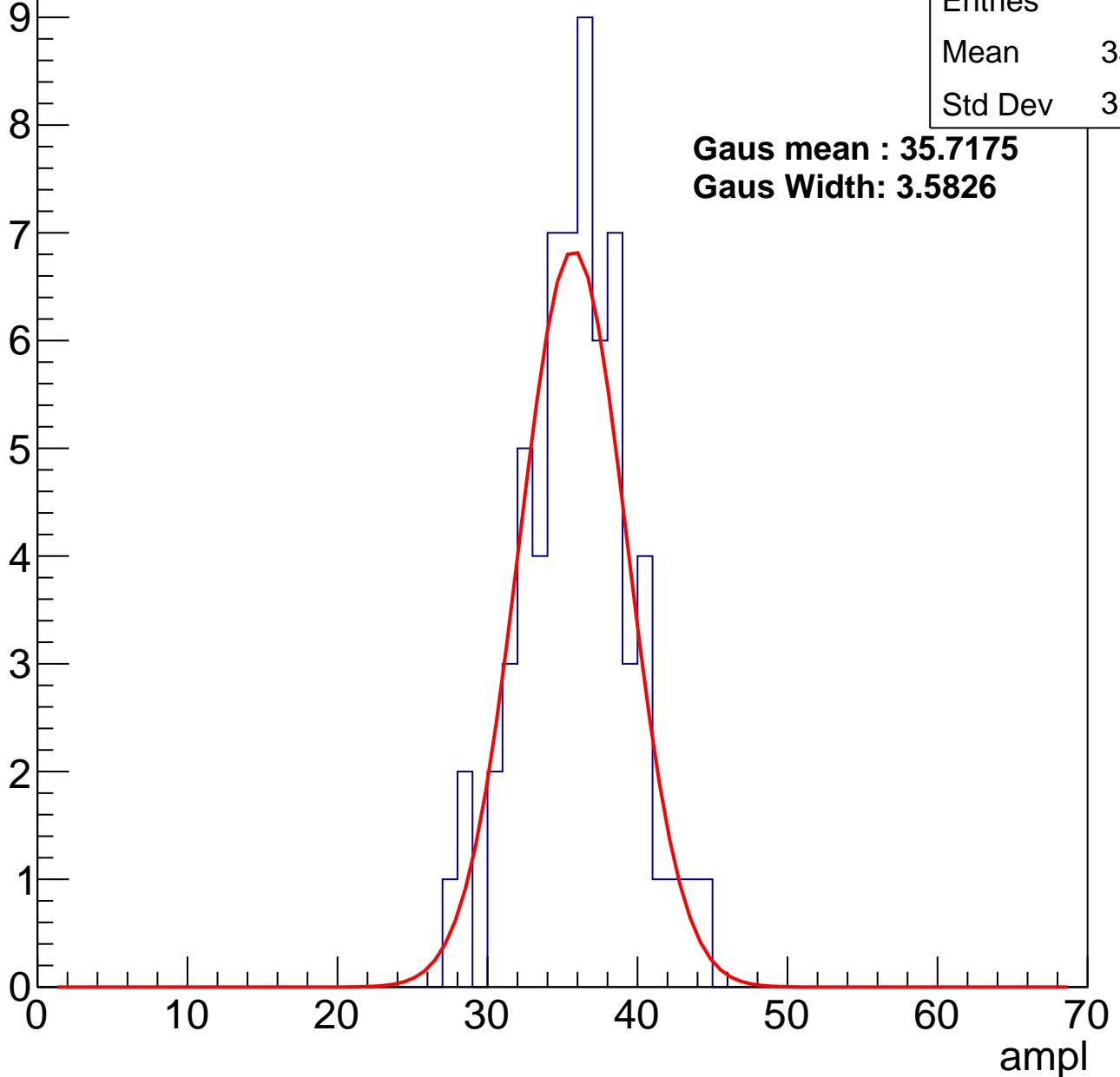
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	35.47
Std Dev	3.509

**Gaus mean : 35.7175**

**Gaus Width: 3.5826**



# B1L003S, U26-ch12, adc2

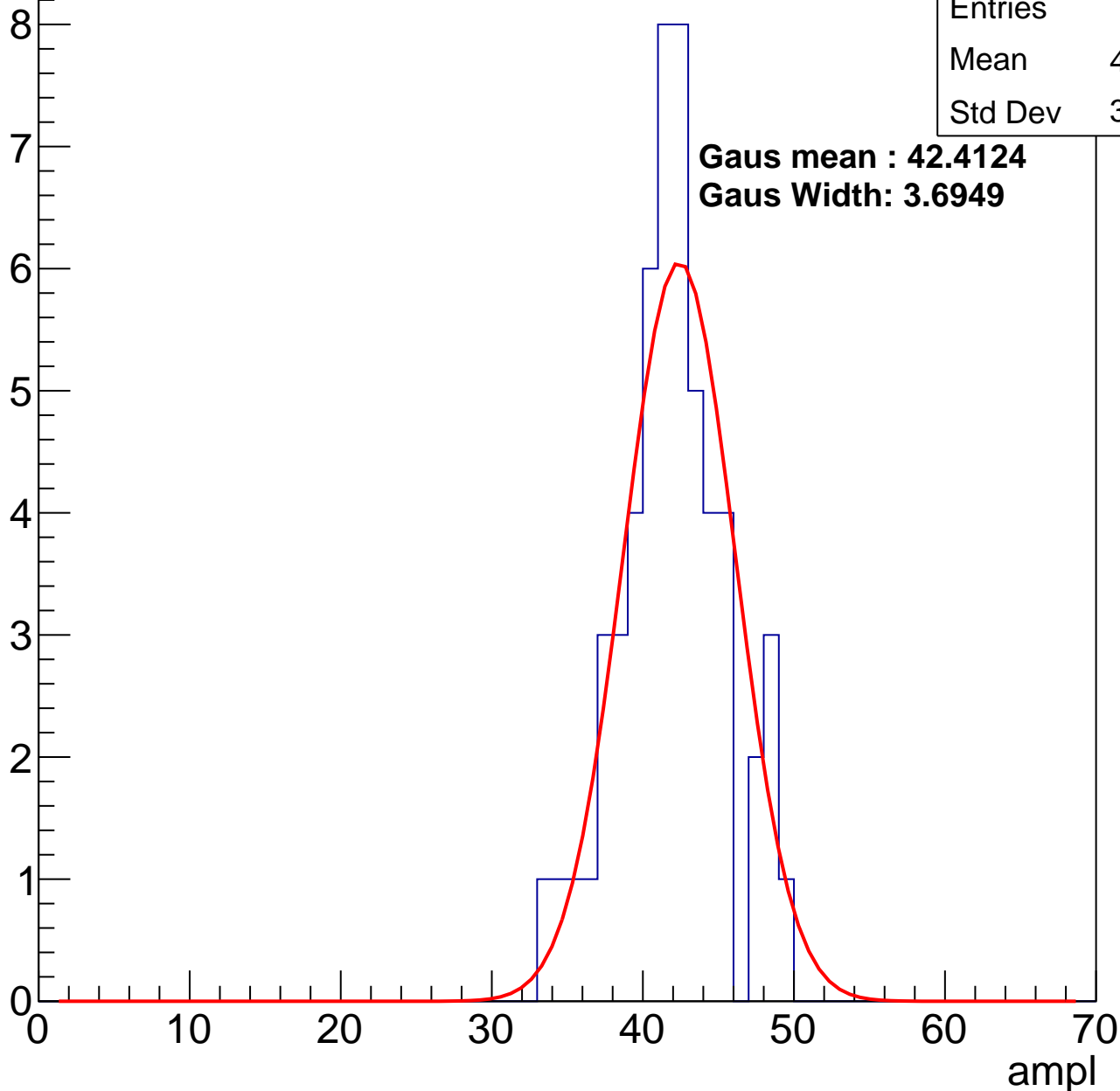
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	41.47
Std Dev	3.489

**Gaus mean : 42.4124**

**Gaus Width: 3.6949**



# B1L003S, U26-ch12, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

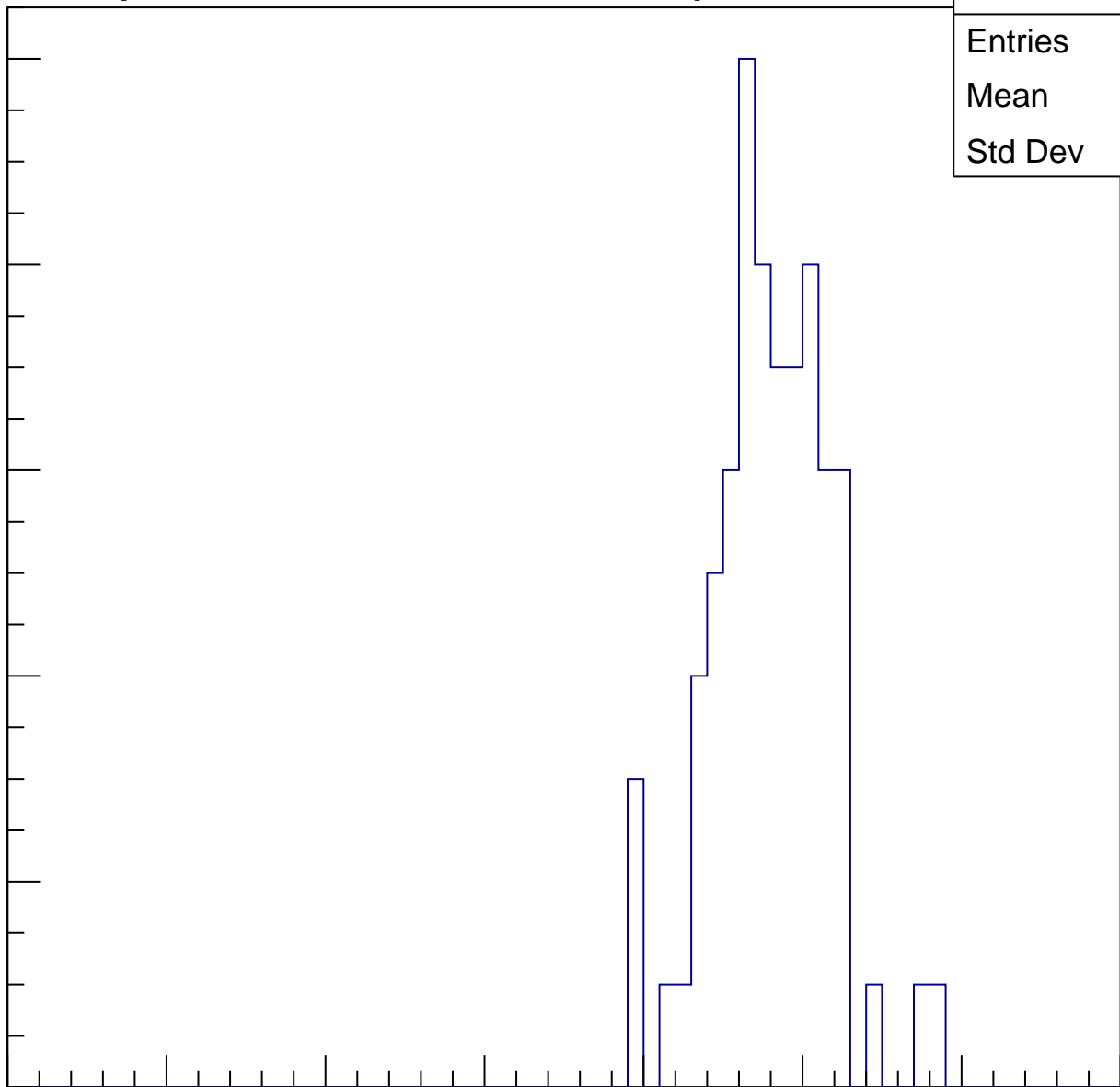
Entries	75
Mean	47.52
Std Dev	3.649

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

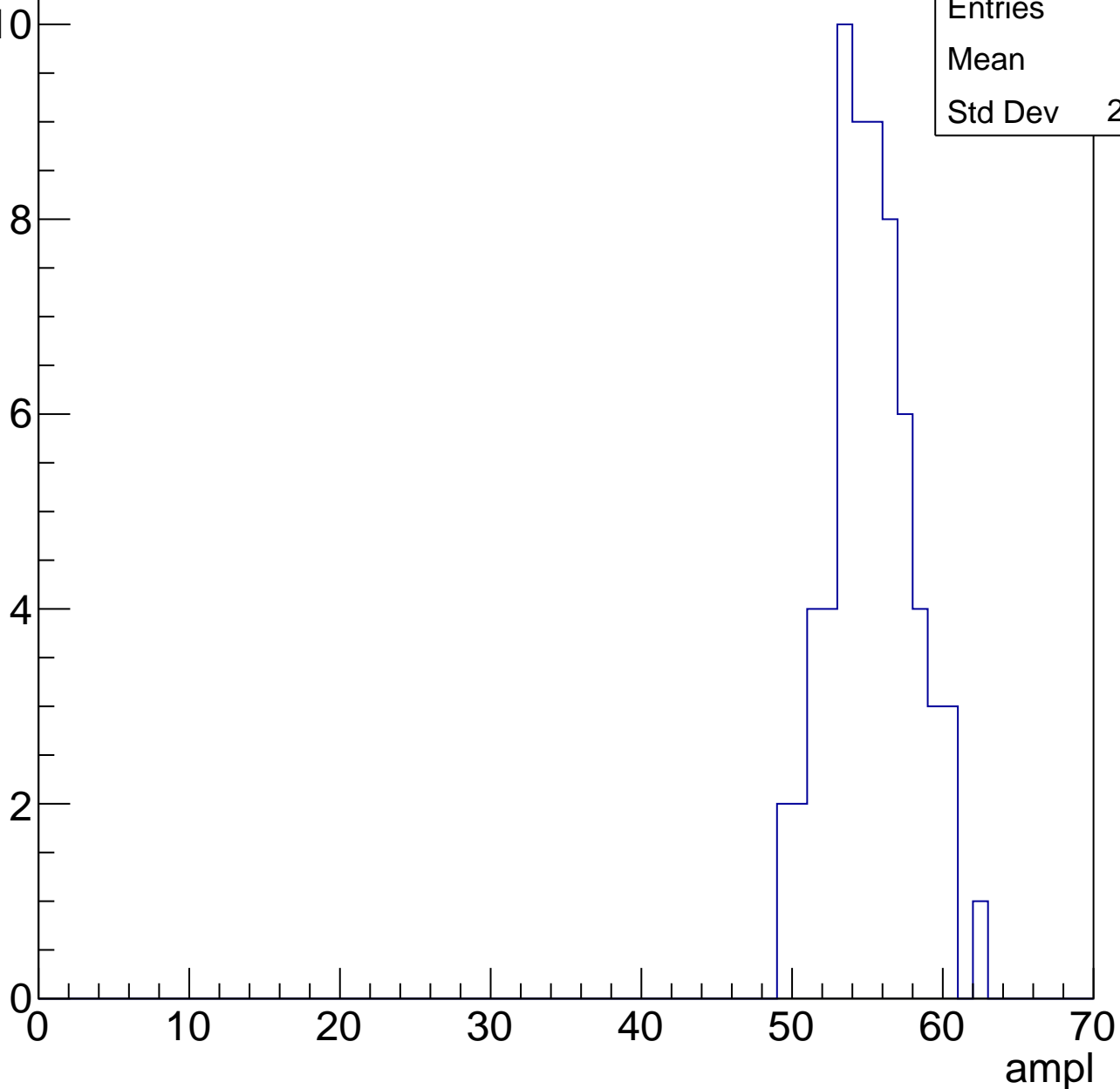


# B1L003S, U26-ch12, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	54.8
Std Dev	2.797

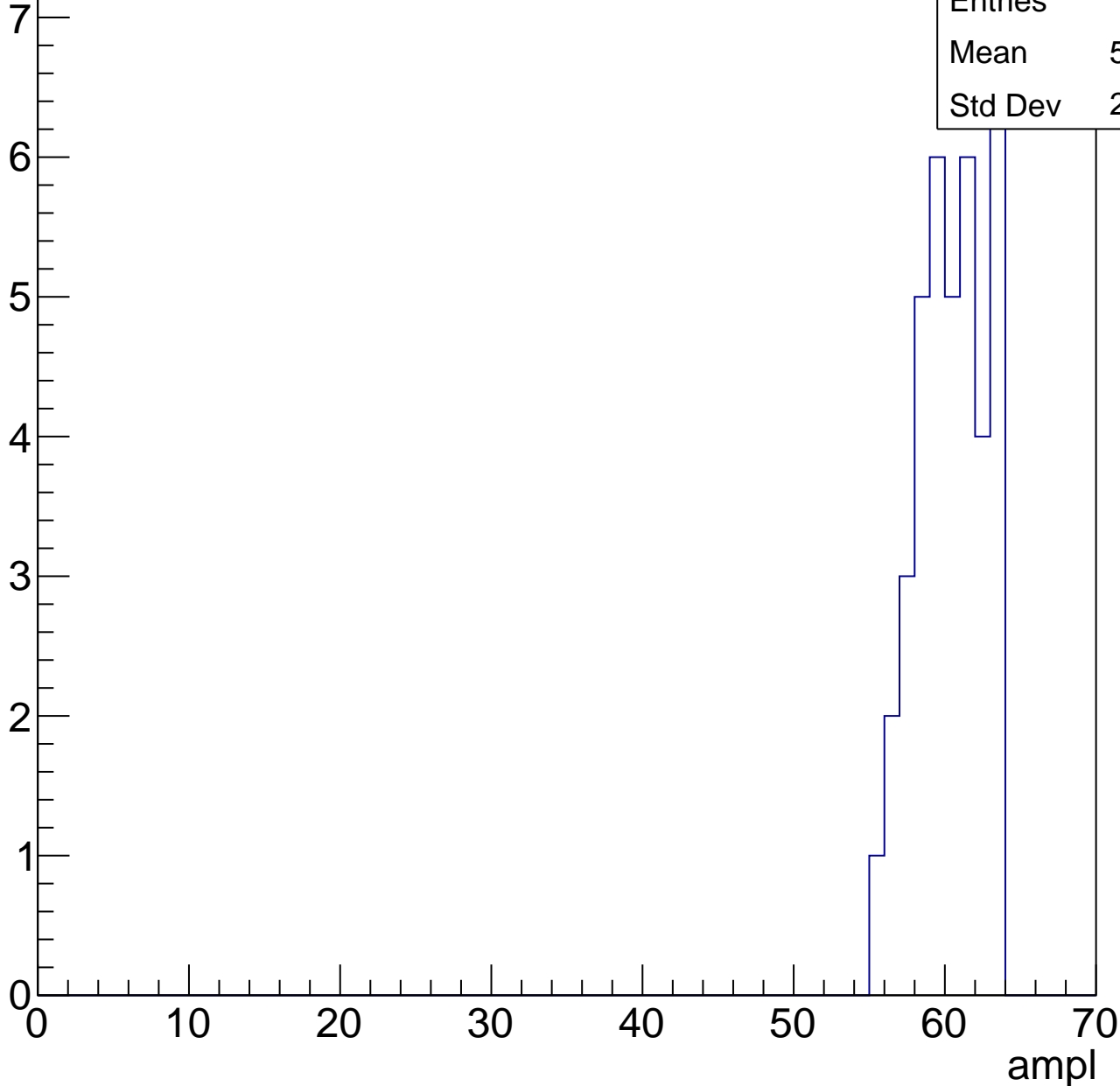


# B1L003S, U26-ch12, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	39
Mean	59.92
Std Dev	2.235

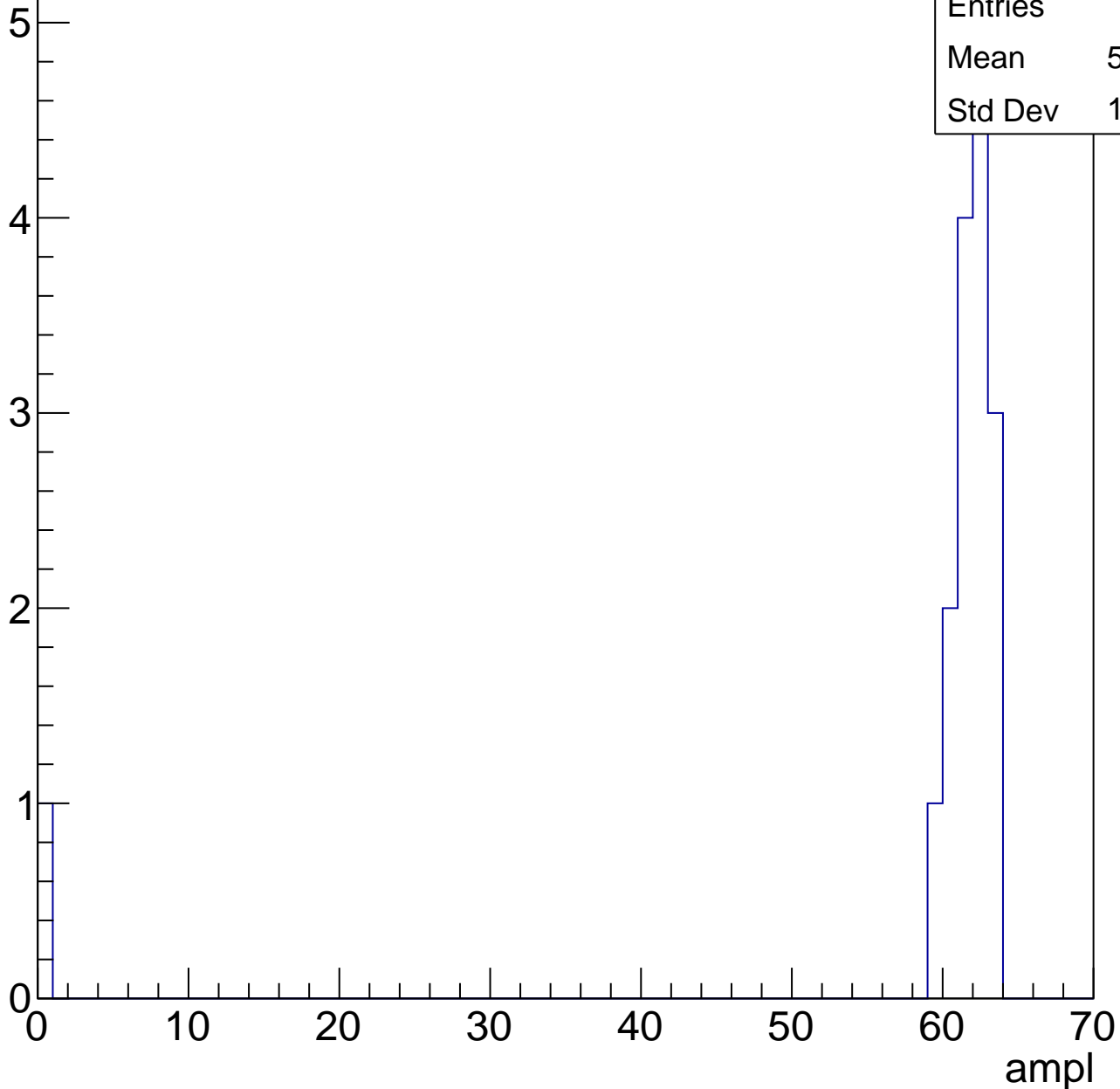


# B1L003S, U26-ch12, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	16
Mean	57.62
Std Dev	14.92





# B1L003S, U26-ch12, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U26-ch13, adc0

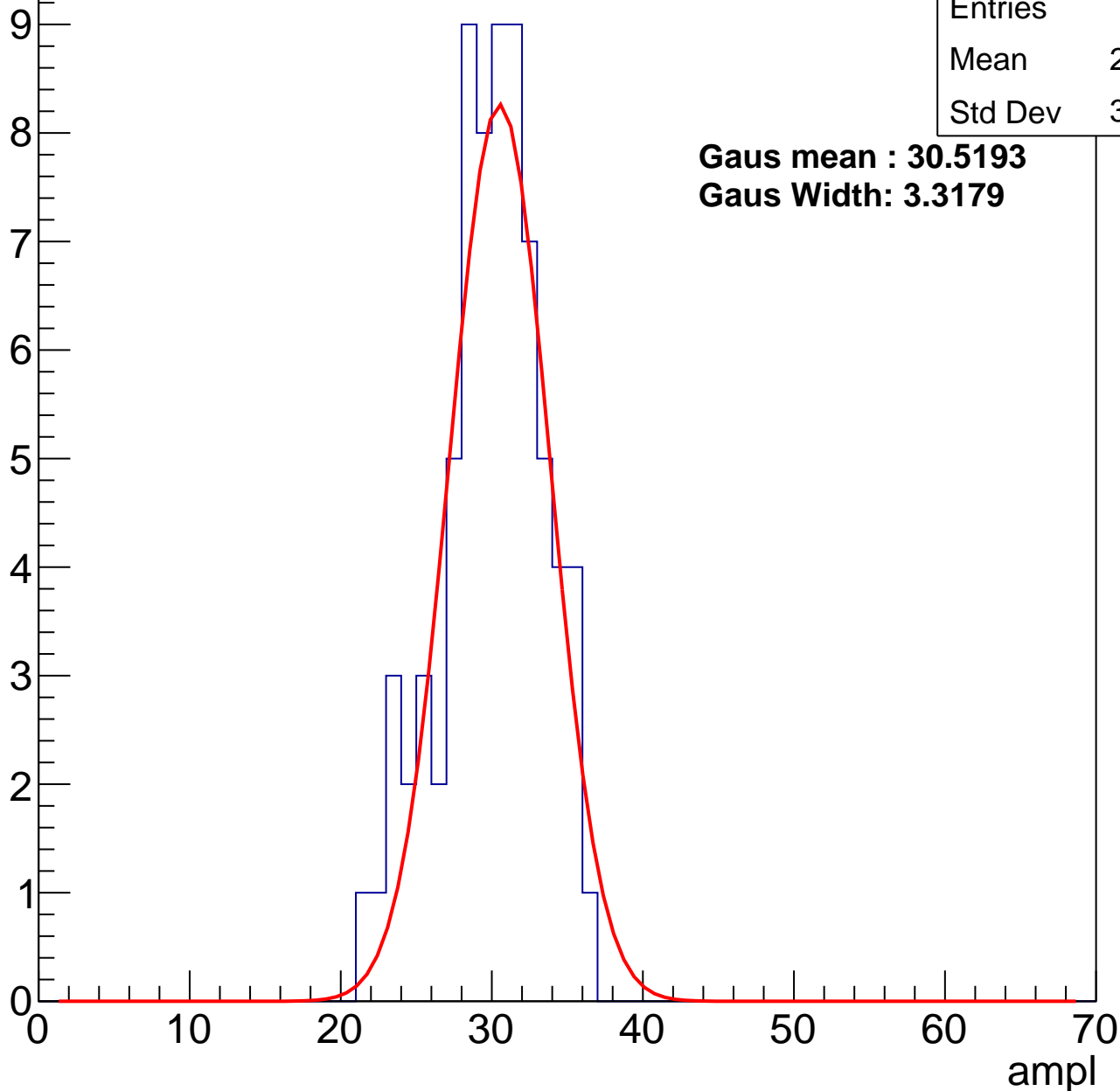
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	73
Mean	29.53
Std Dev	3.364

**Gaus mean : 30.5193**

**Gaus Width: 3.3179**



# B1L003S, U26-ch13, adc1

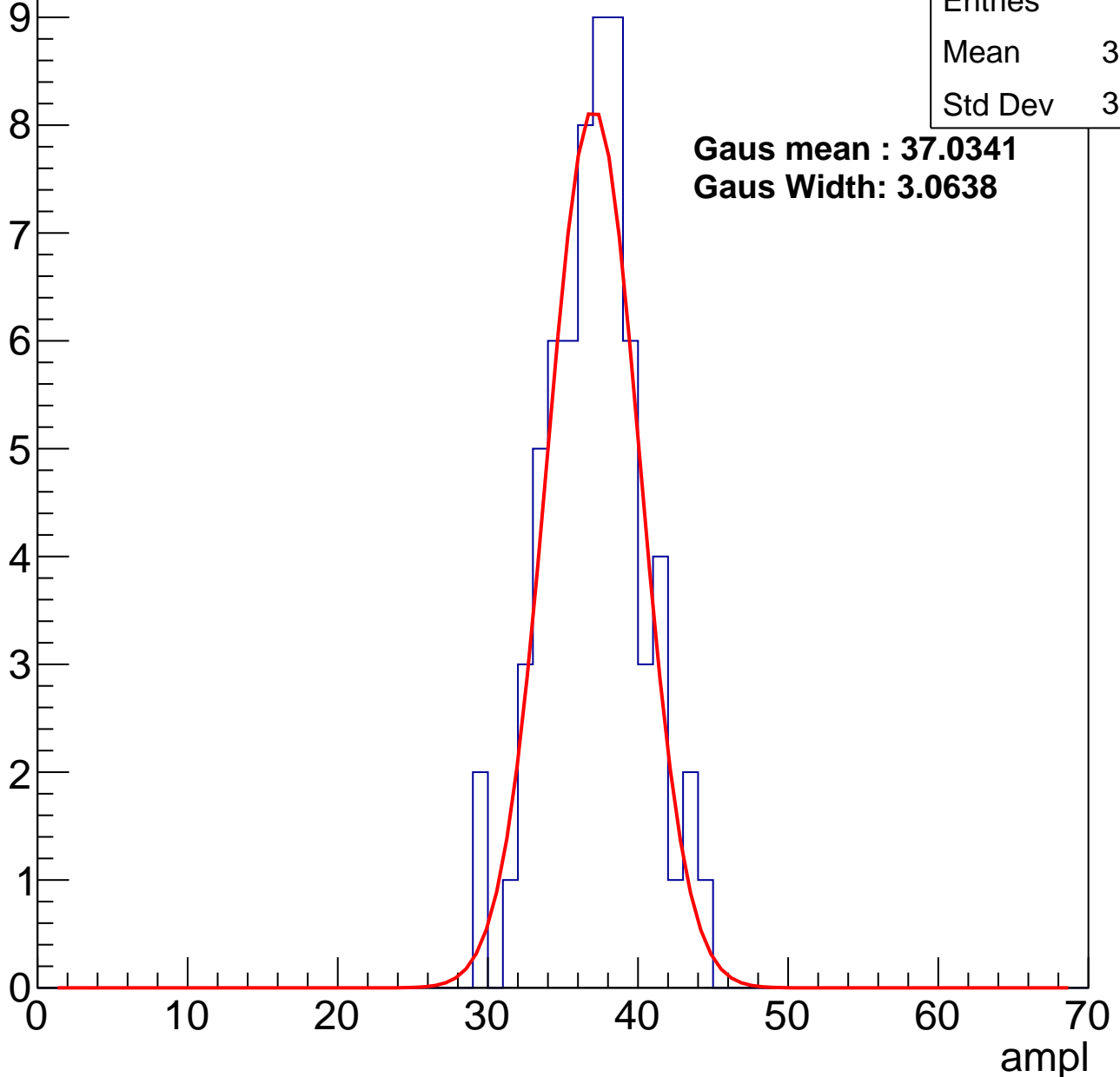
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	36.62
Std Dev	3.175

**Gaus mean : 37.0341**

**Gaus Width: 3.0638**



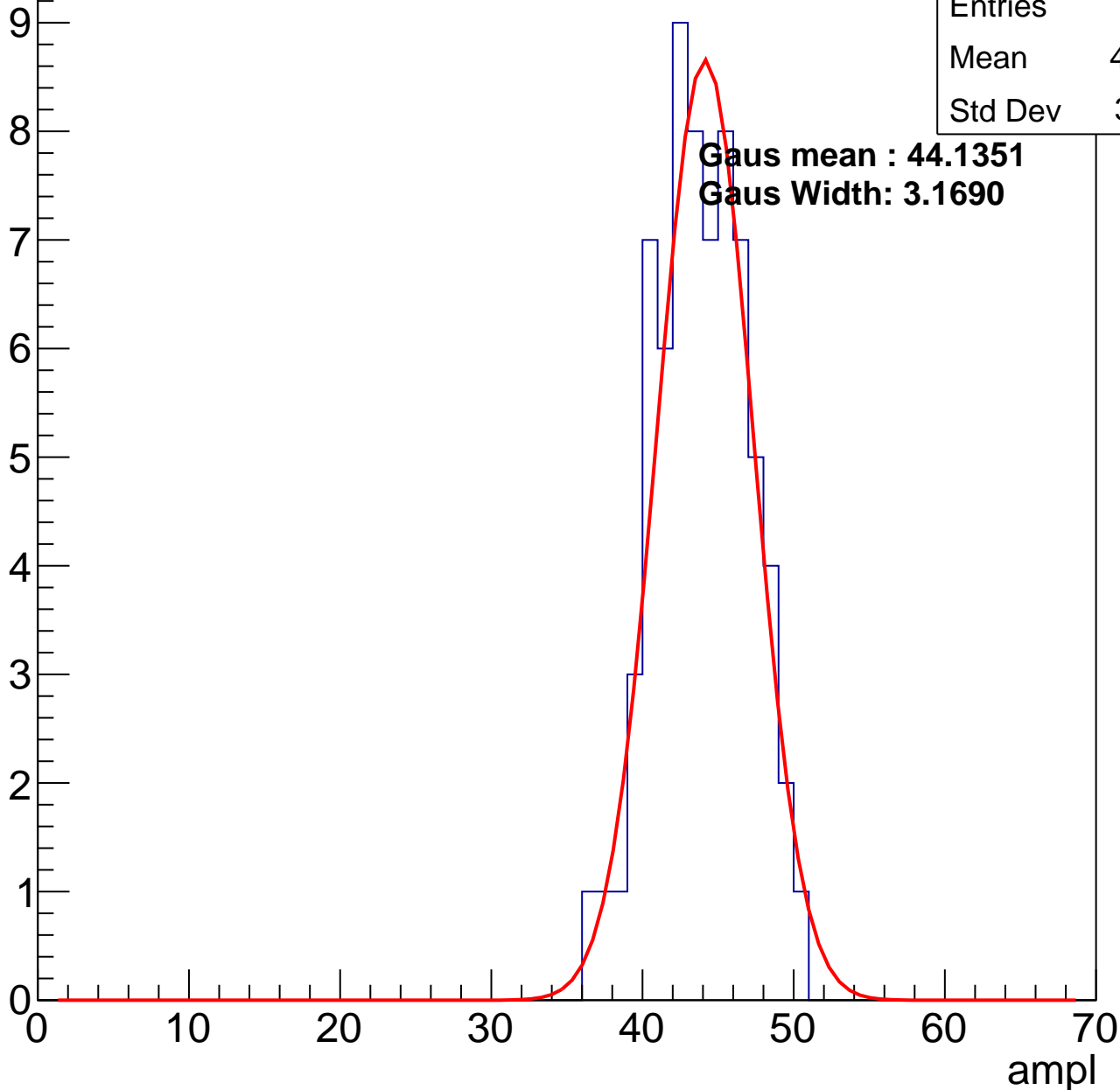
# B1L003S, U26-ch13, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	43.44
Std Dev	3.031

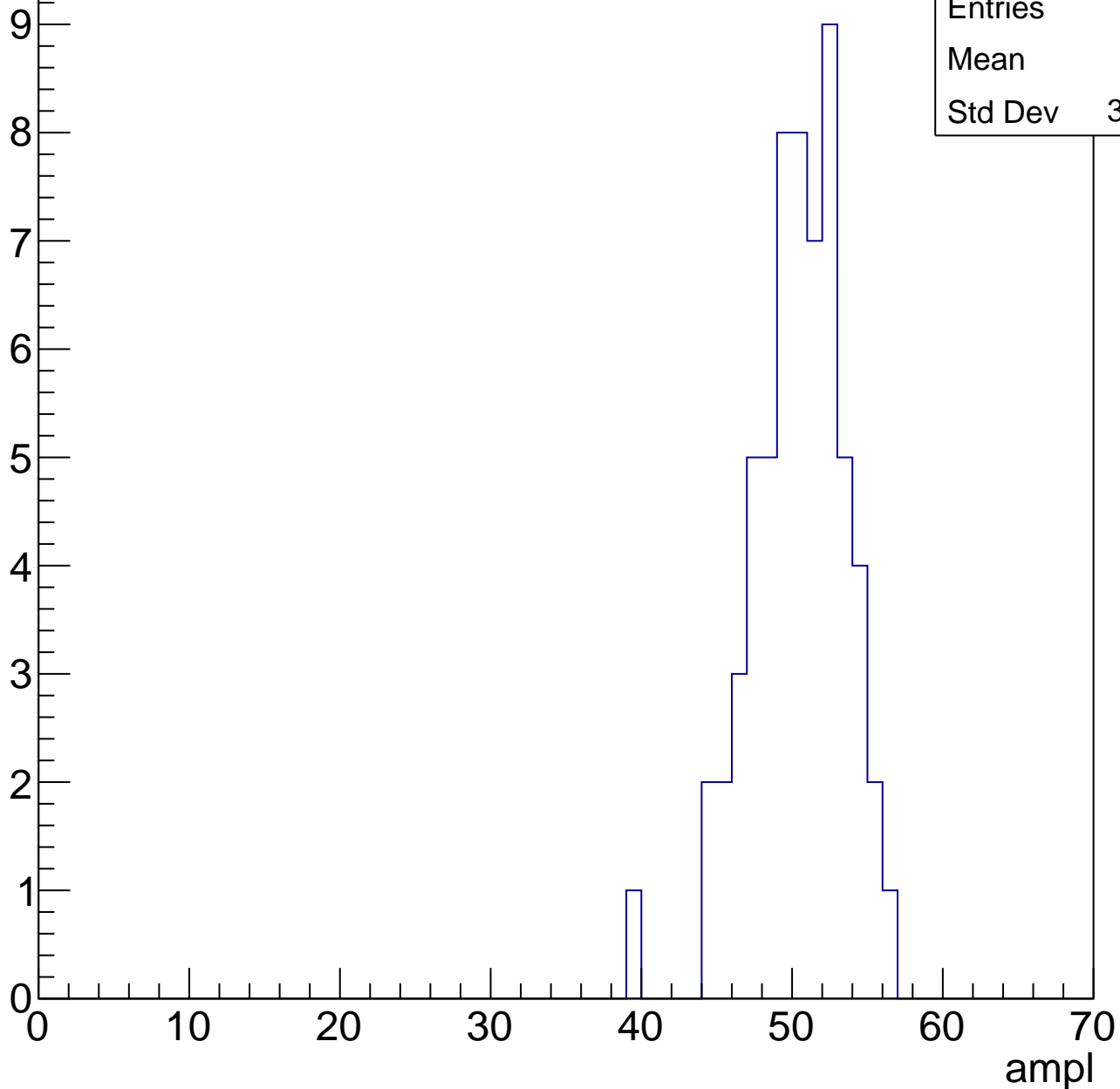
**Gaus mean : 44.1351**  
**Gaus Width: 3.1690**



# B1L003S, U26-ch13, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

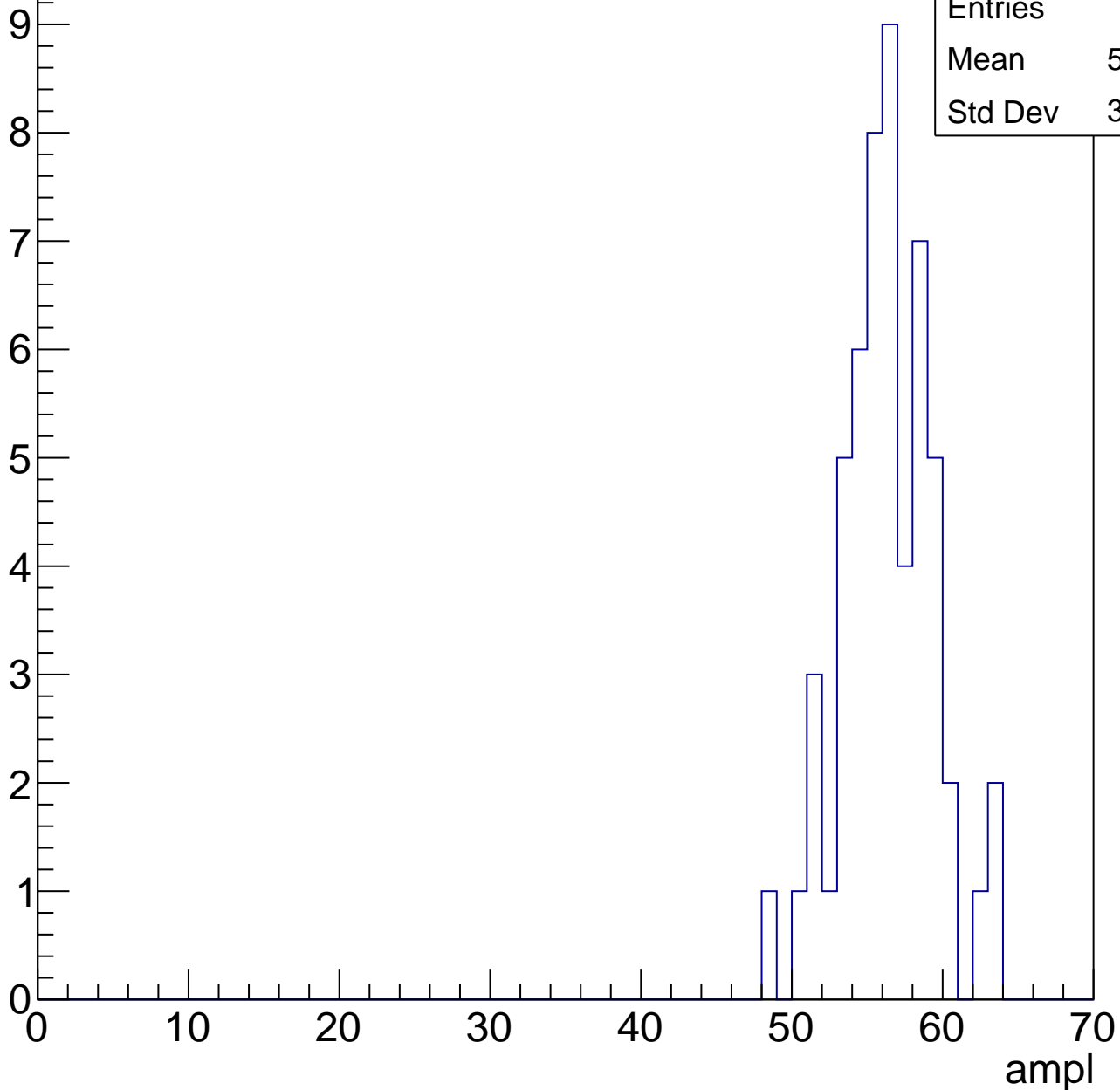


# B1L003S, U26-ch13, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	55.87
Std Dev	3.045

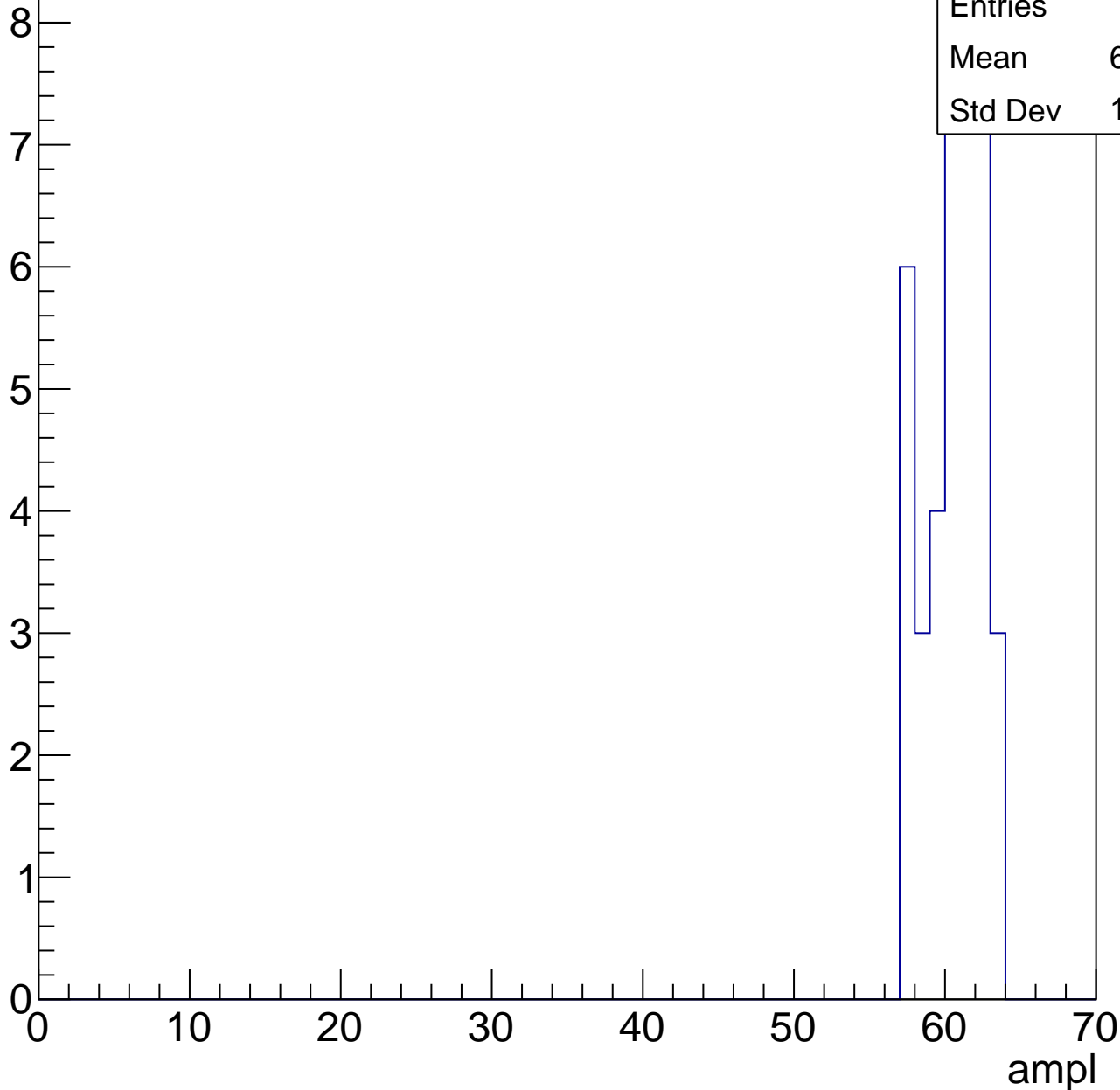


# B1L003S, U26-ch13, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	40
Mean	60.12
Std Dev	1.846

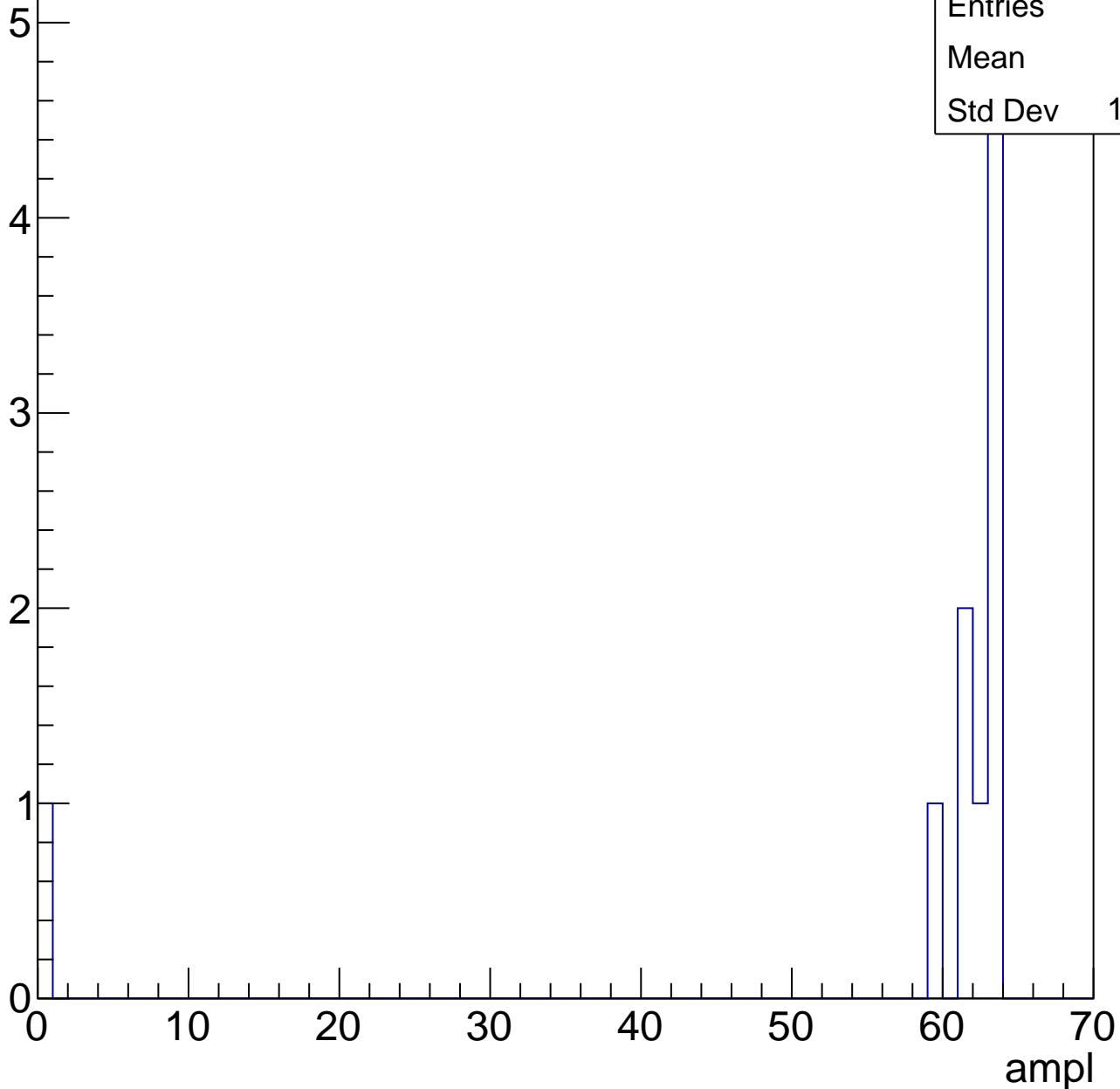


# B1L003S, U26-ch13, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	10
Mean	55.8
Std Dev	18.64





# B1L003S, U26-ch13, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U26-ch14, adc0

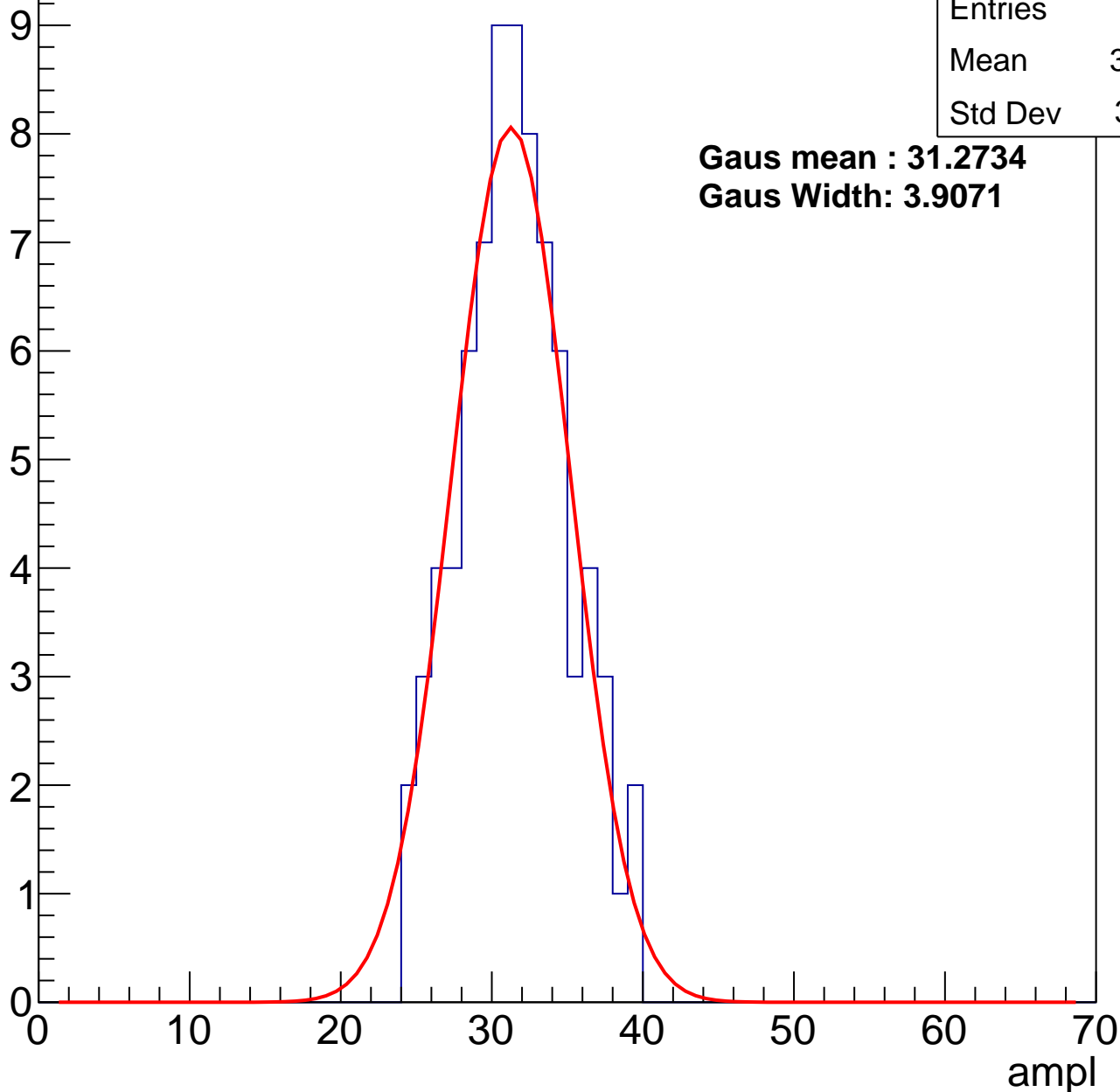
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	78
Mean	31.05
Std Dev	3.551

**Gaus mean : 31.2734**

**Gaus Width: 3.9071**



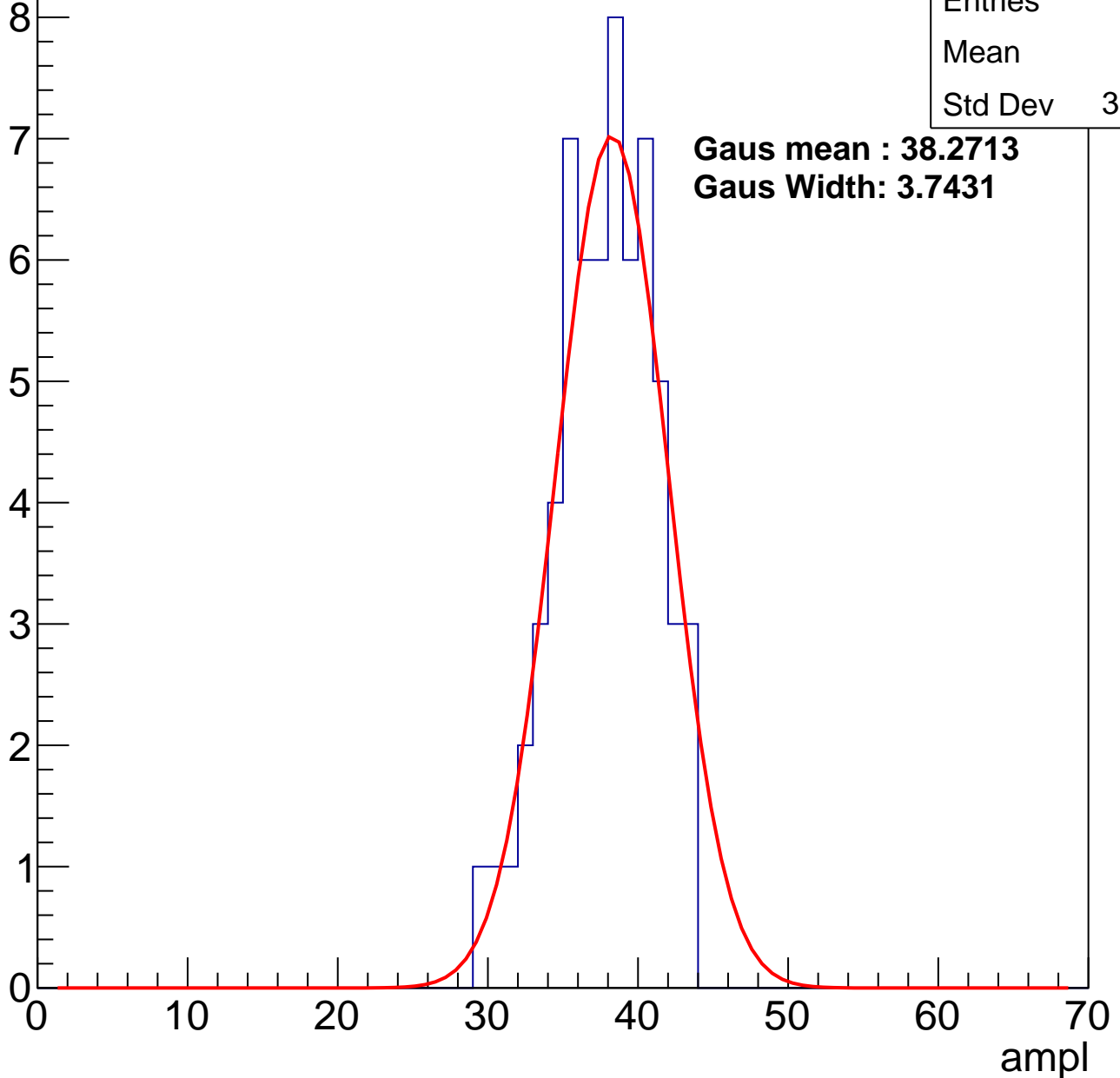
# B1L003S, U26-ch14, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	37.3
Std Dev	3.259

**Gaus mean : 38.2713**  
**Gaus Width: 3.7431**



# B1L003S, U26-ch14, adc2

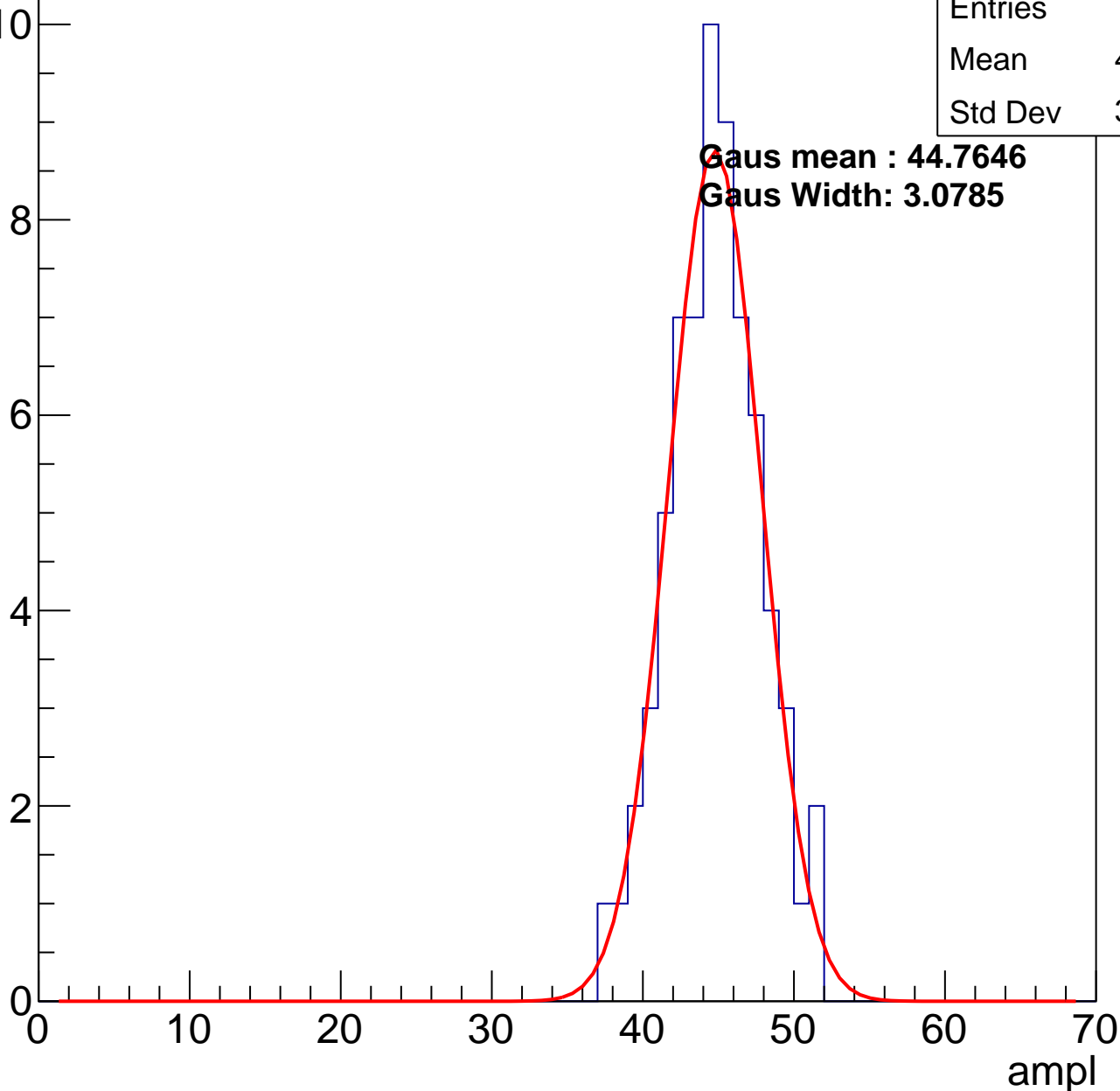
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	44.31
Std Dev	3.021

Gaus mean : 44.7646

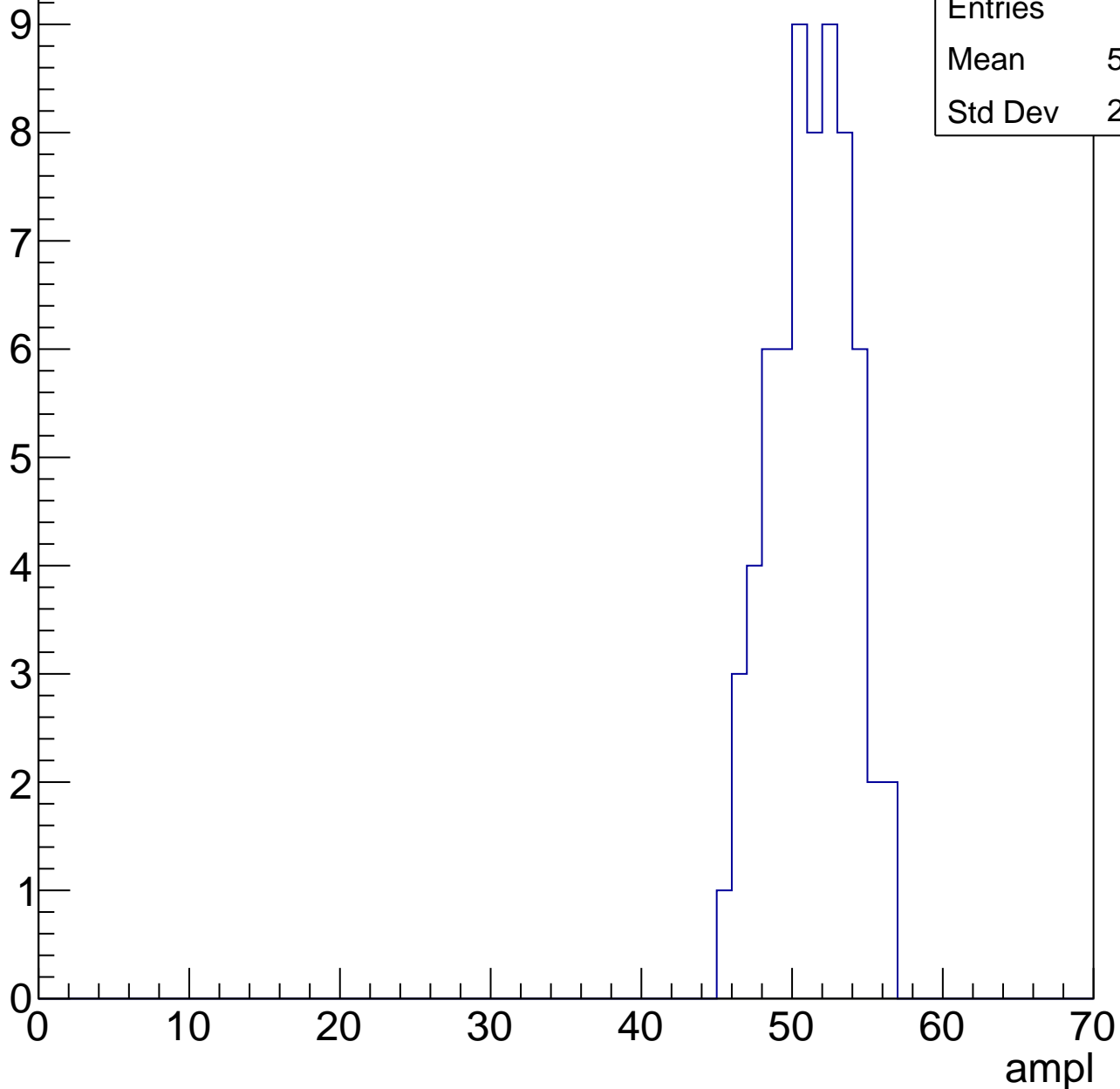
Gaus Width: 3.0785



# B1L003S, U26-ch14, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U26-ch14, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

10

8

6

4

2

0

0

10

20

30

40

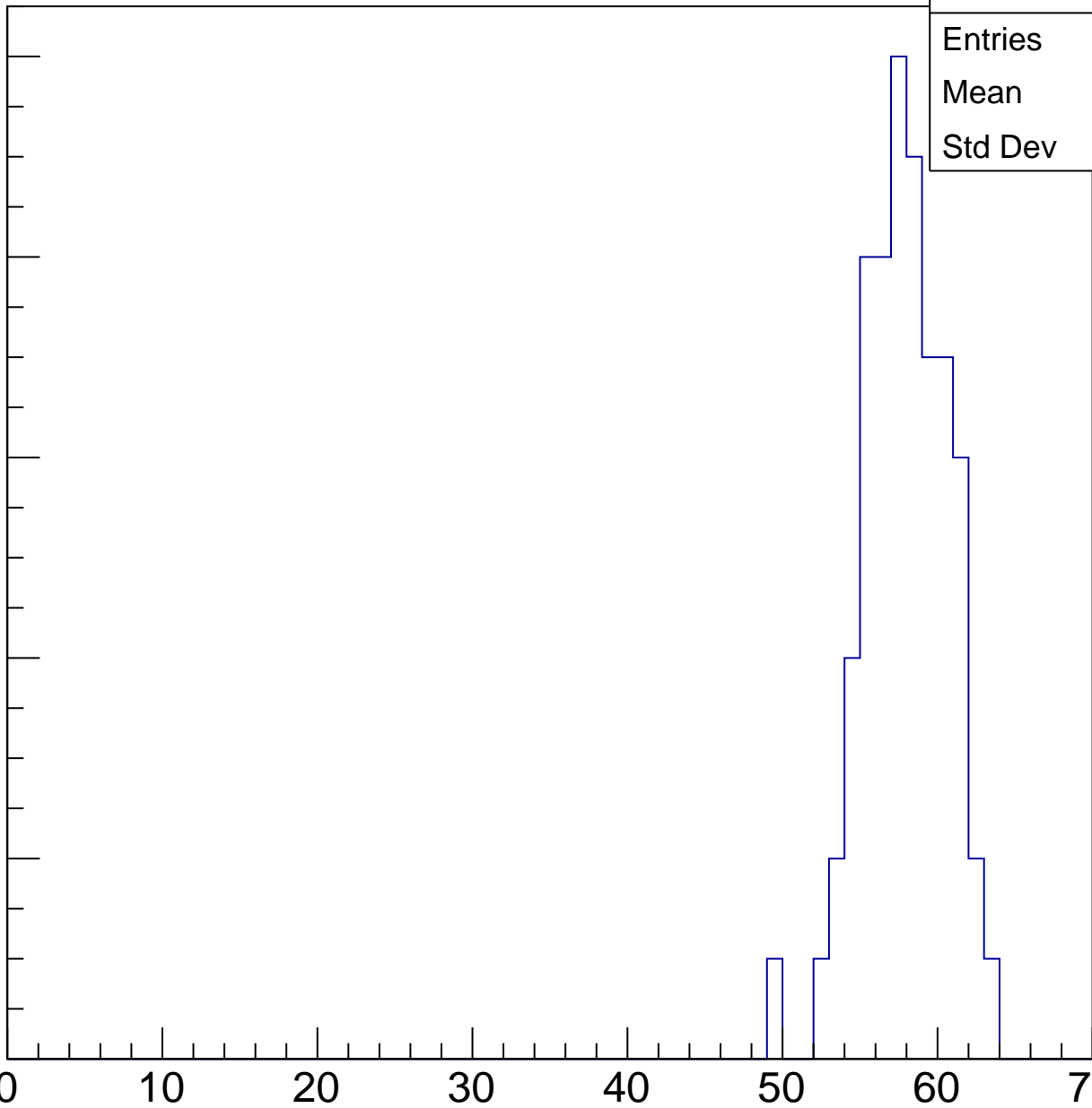
50

60

70

ampl

Entries	66
Mean	57.41
Std Dev	2.663

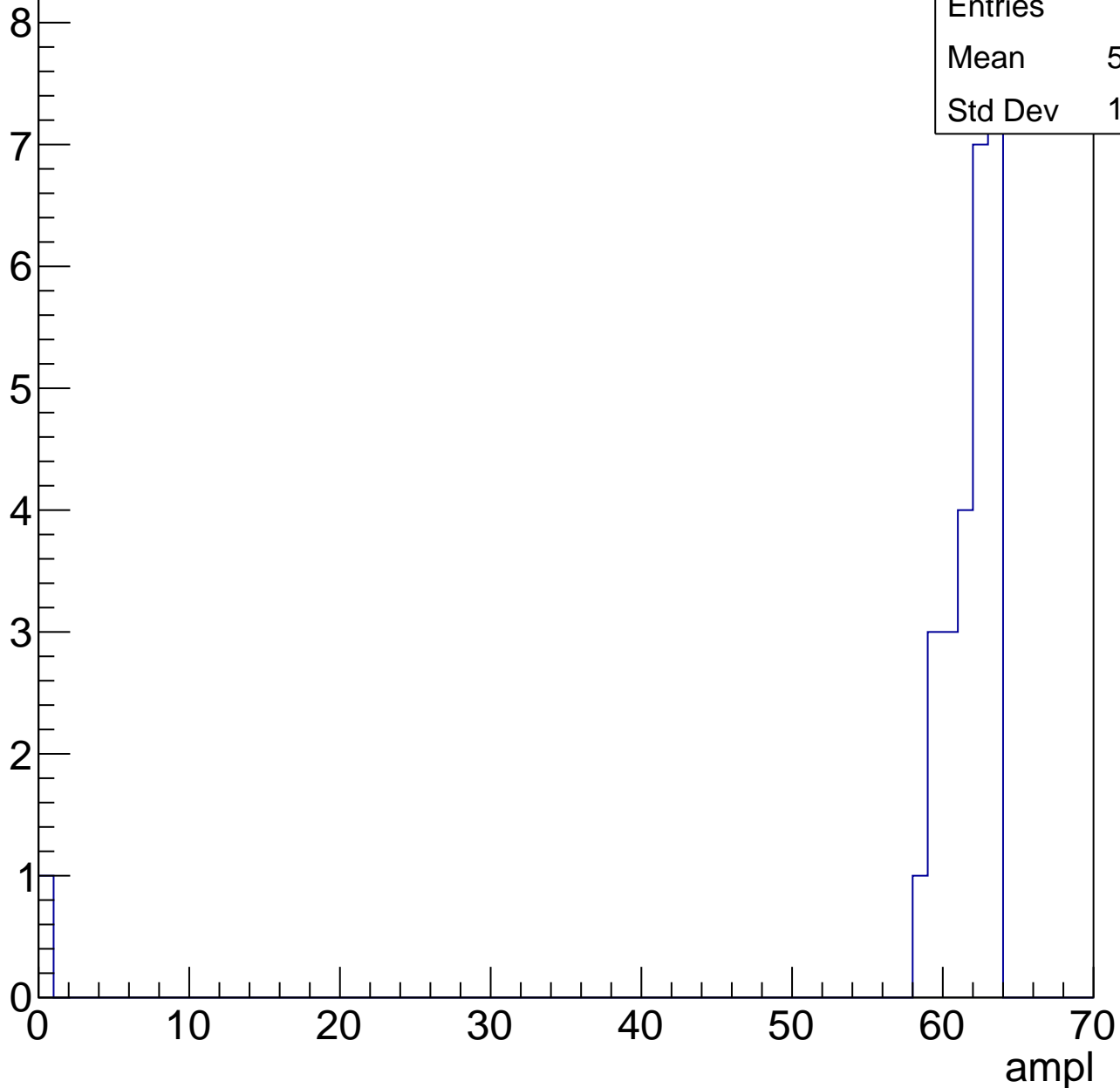


# B1L003S, U26-ch14, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	27
Mean	59.15
Std Dev	11.69



# B1L003S, U26-ch14, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch14, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U26-ch15, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	72
Mean	30.25
Std Dev	3.213

**Gaus mean : 30.4244**

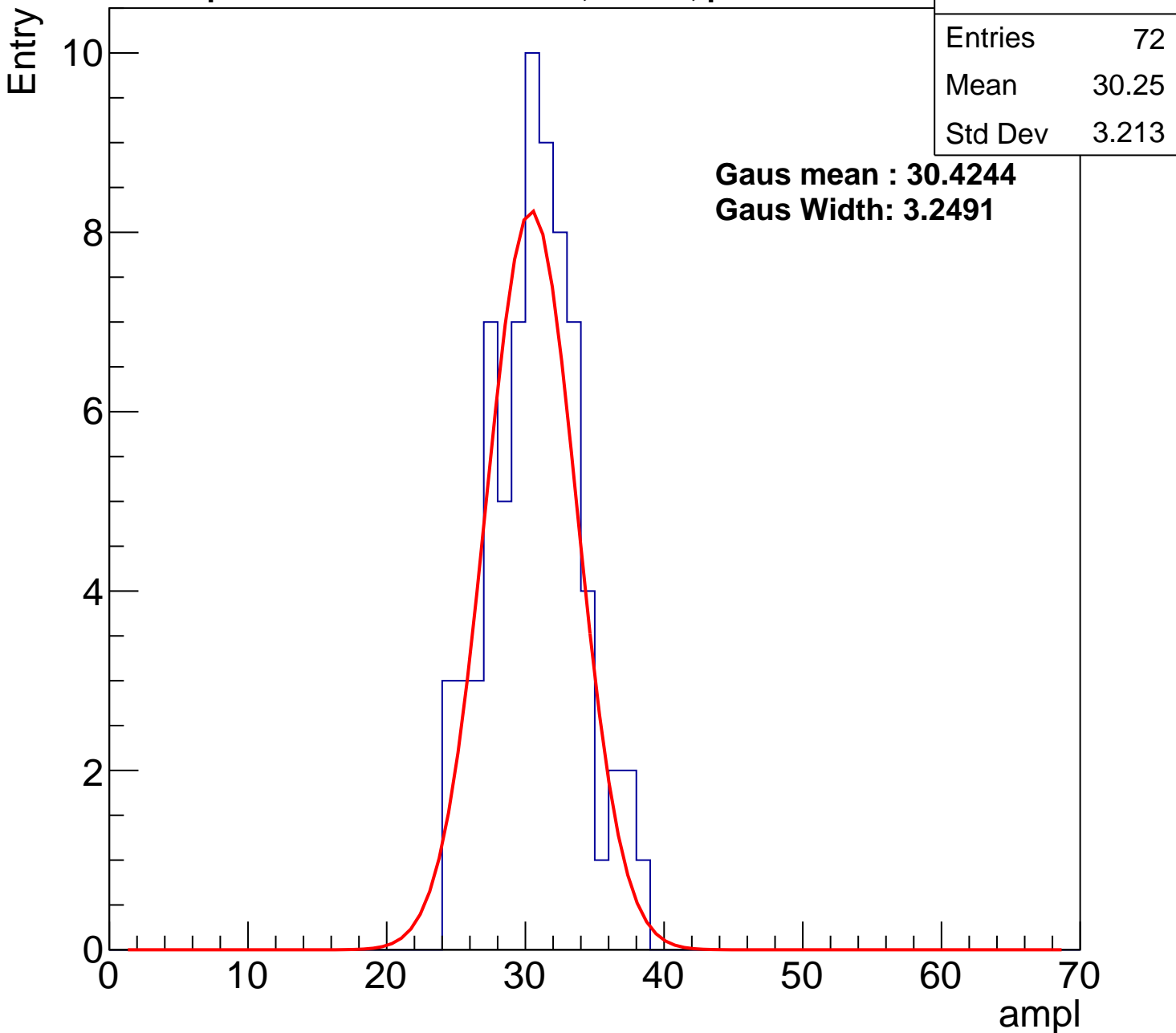
**Gaus Width: 3.2491**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U26-ch15, adc1

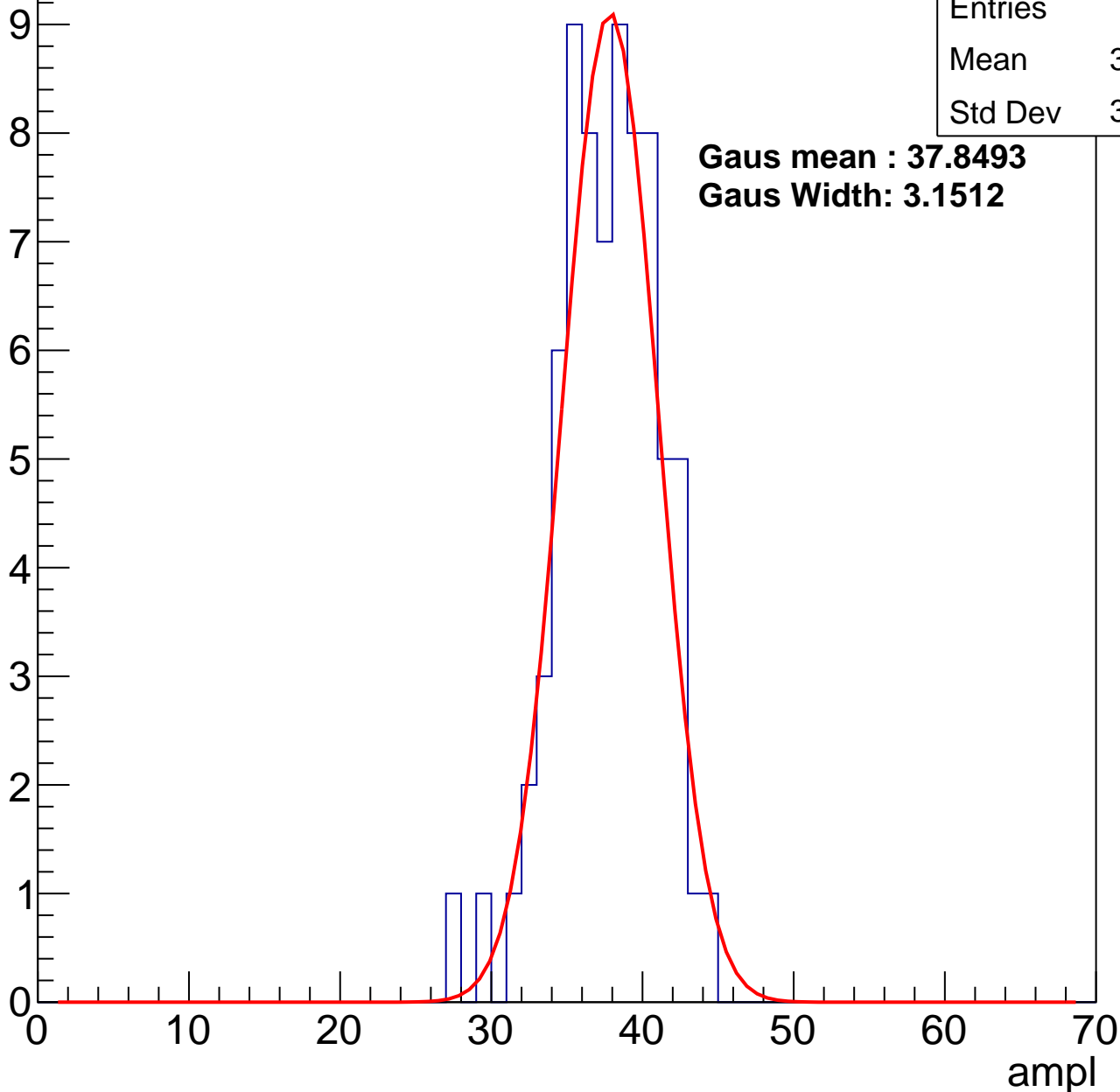
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	75
Mean	37.23
Std Dev	3.256

**Gaus mean : 37.8493**

**Gaus Width: 3.1512**



# B1L003S, U26-ch15, adc2

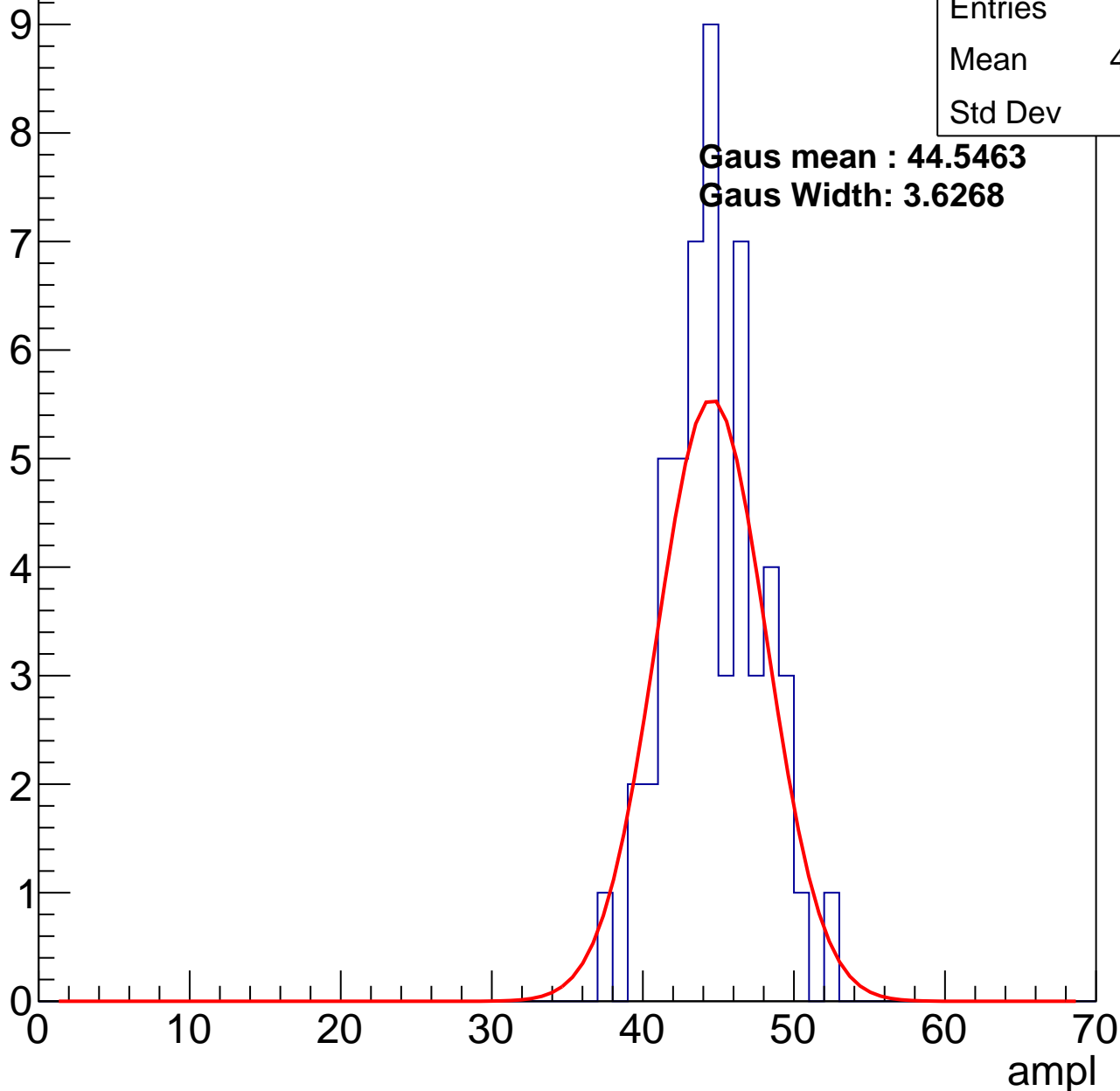
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	44.26
Std Dev	3.06

**Gaus mean : 44.5463**

**Gaus Width: 3.6268**



# B1L003S, U26-ch15, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	83
Mean	50.63
Std Dev	3.606

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

ampl

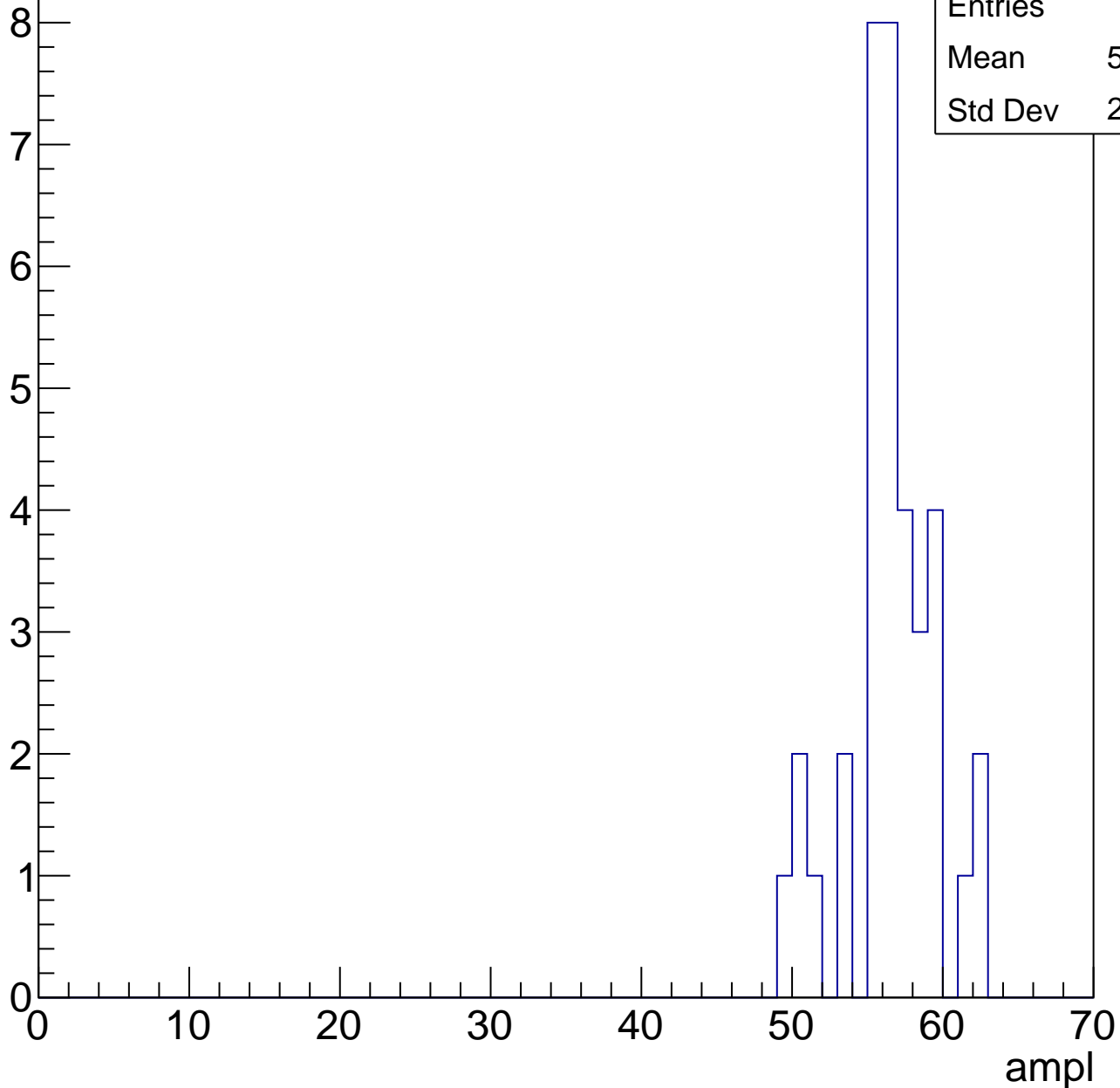
70

# B1L003S, U26-ch15, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	36
Mean	56.03
Std Dev	2.986

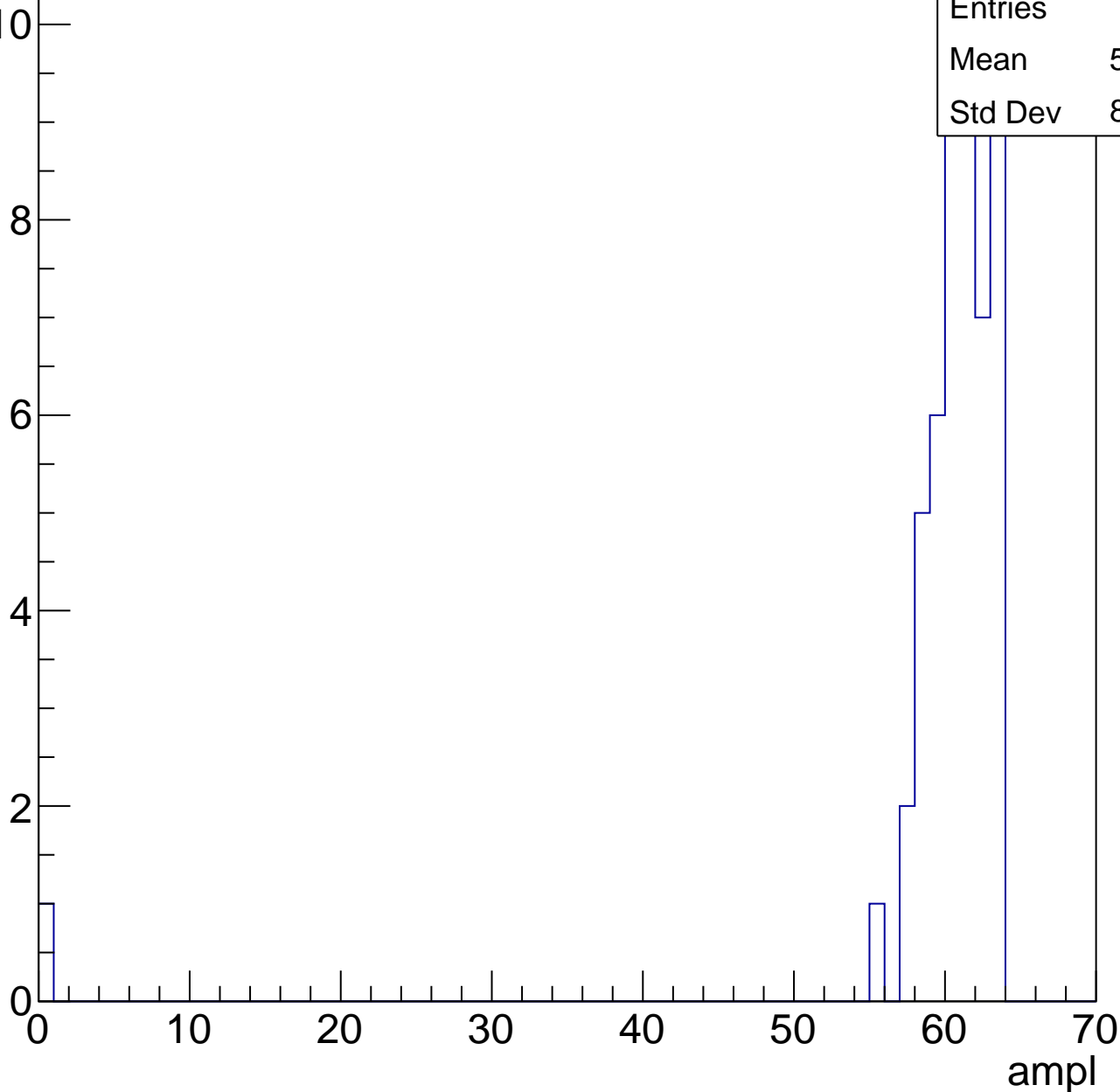


# B1L003S, U26-ch15, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	51
Mean	59.33
Std Dev	8.602



# B1L003S, U26-ch15, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch15, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U26-ch16, adc0

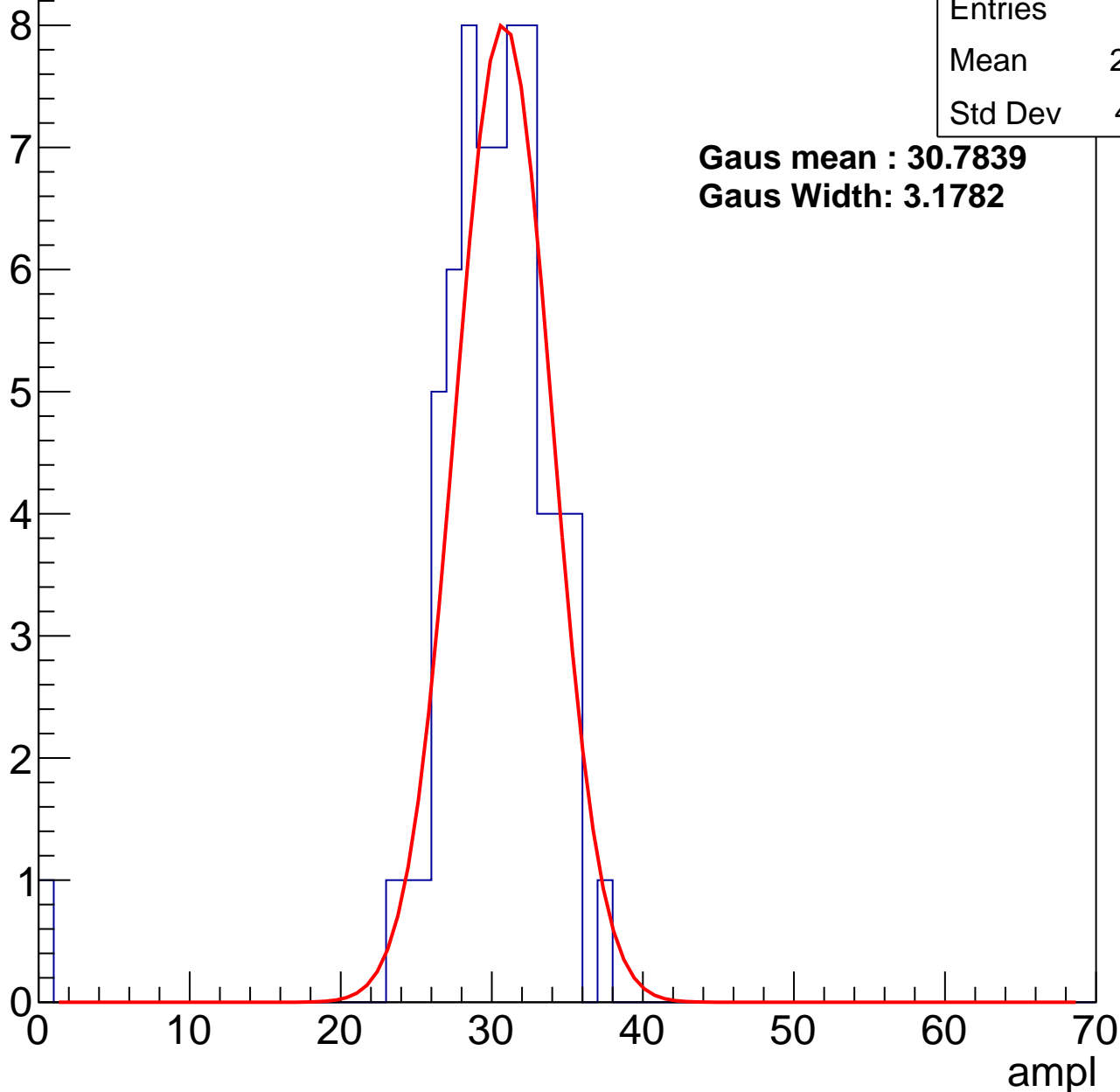
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	29.55
Std Dev	4.701

**Gaus mean : 30.7839**

**Gaus Width: 3.1782**



# B1L003S, U26-ch16, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	65
Mean	36.54
Std Dev	3.491

**Gaus mean : 37.3094**

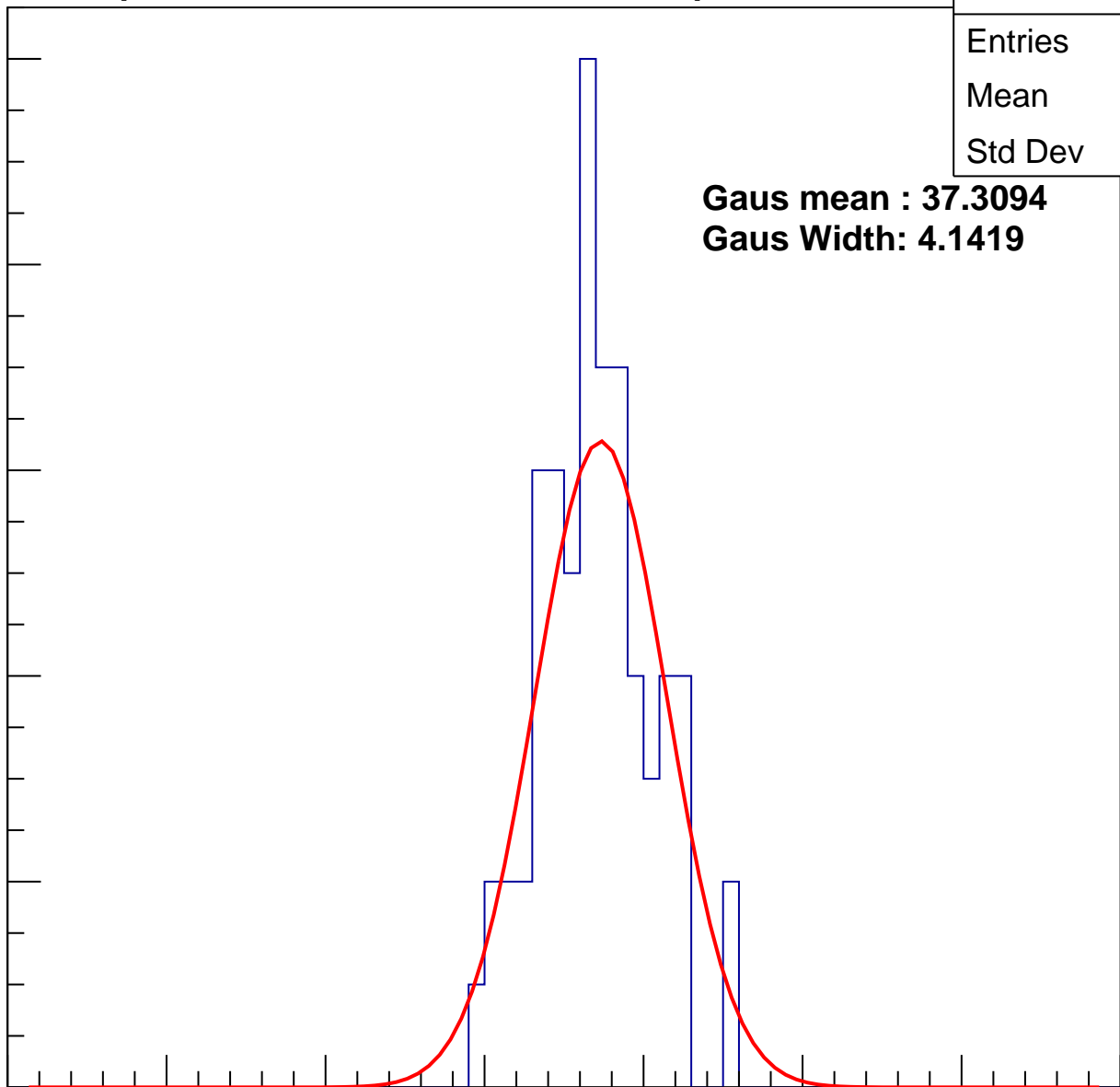
**Gaus Width: 4.1419**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U26-ch16, adc2

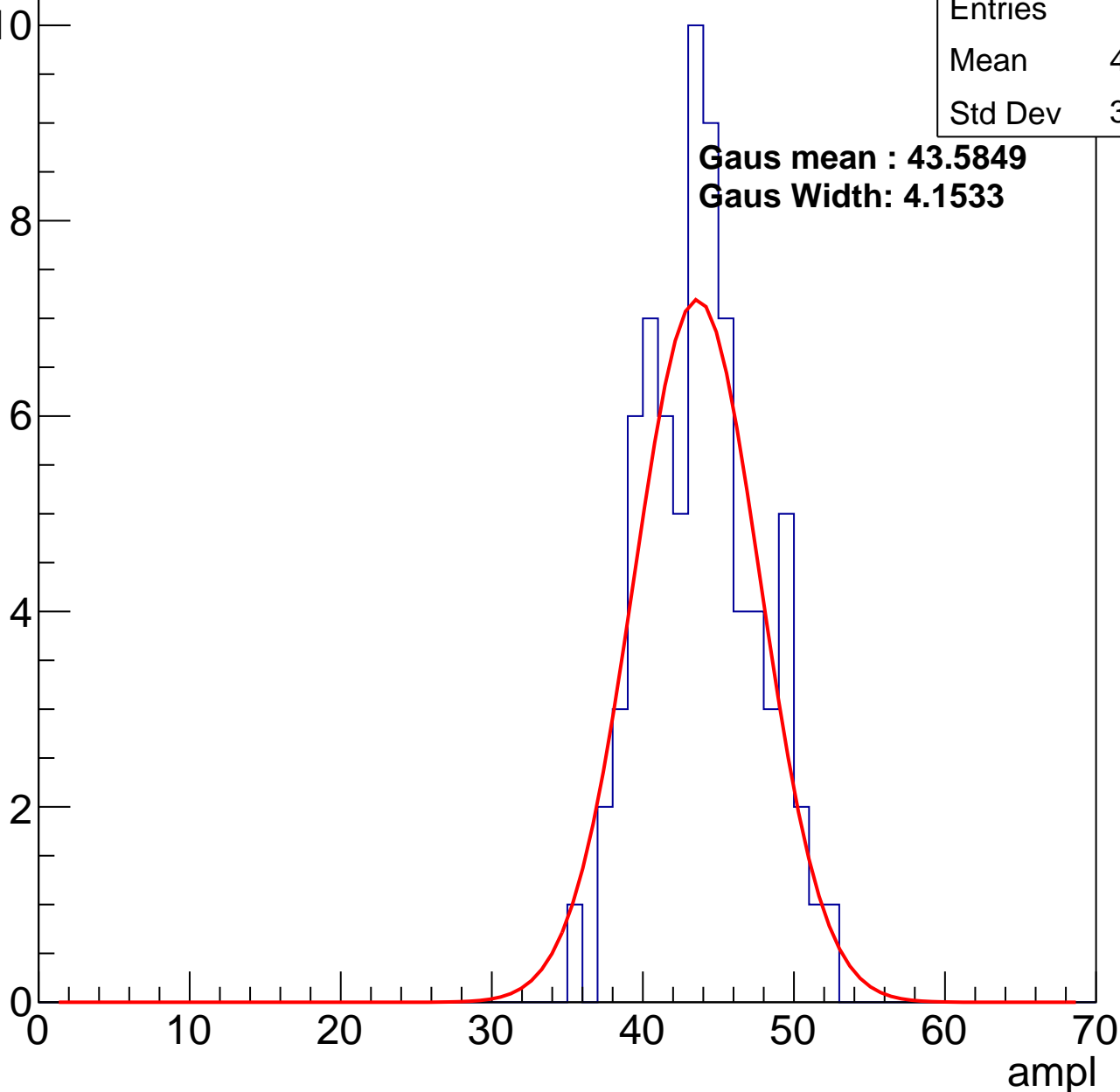
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	76
Mean	43.39
Std Dev	3.667

**Gaus mean : 43.5849**

**Gaus Width: 4.1533**

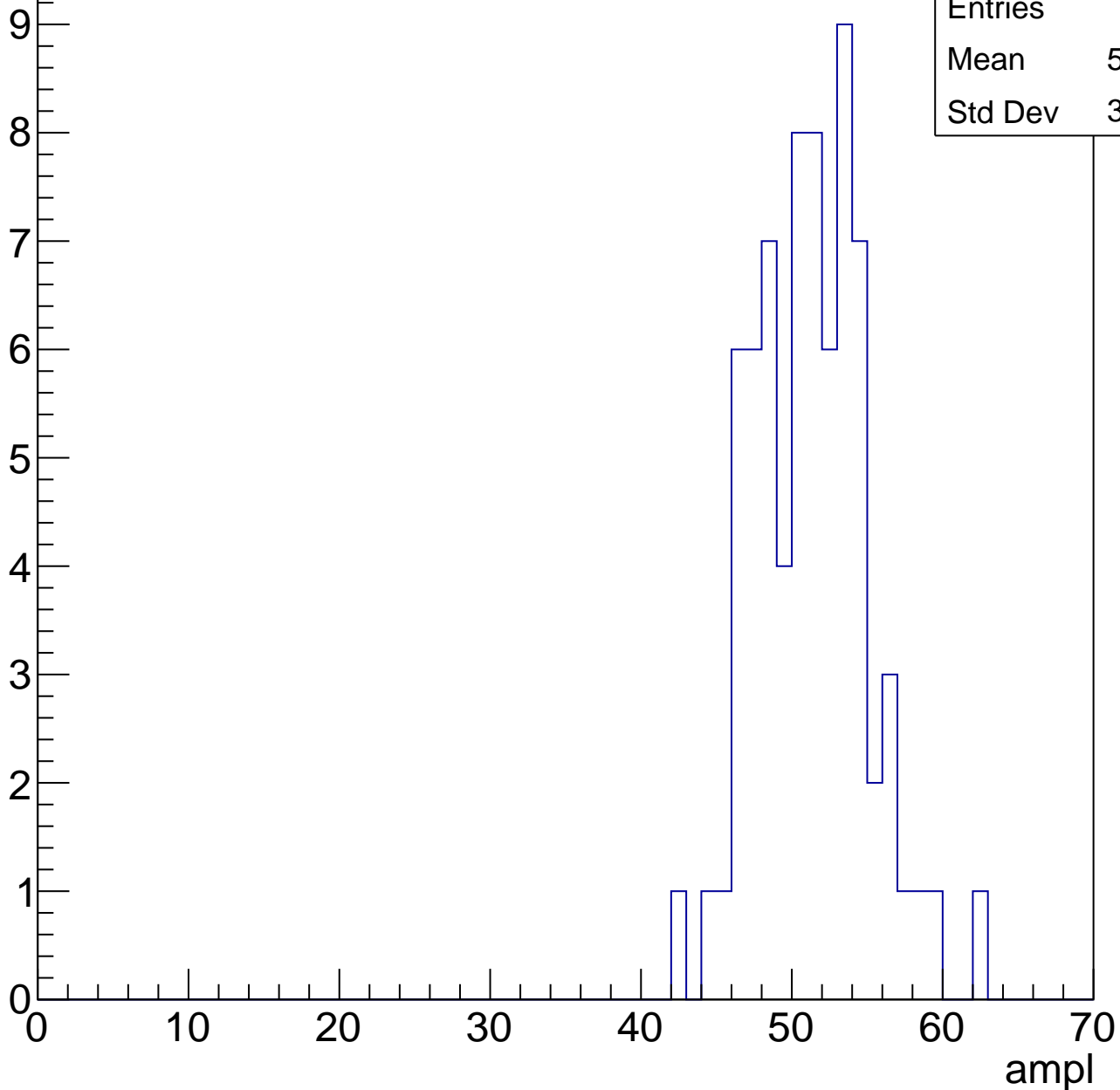


# B1L003S, U26-ch16, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	73
Mean	50.82
Std Dev	3.662

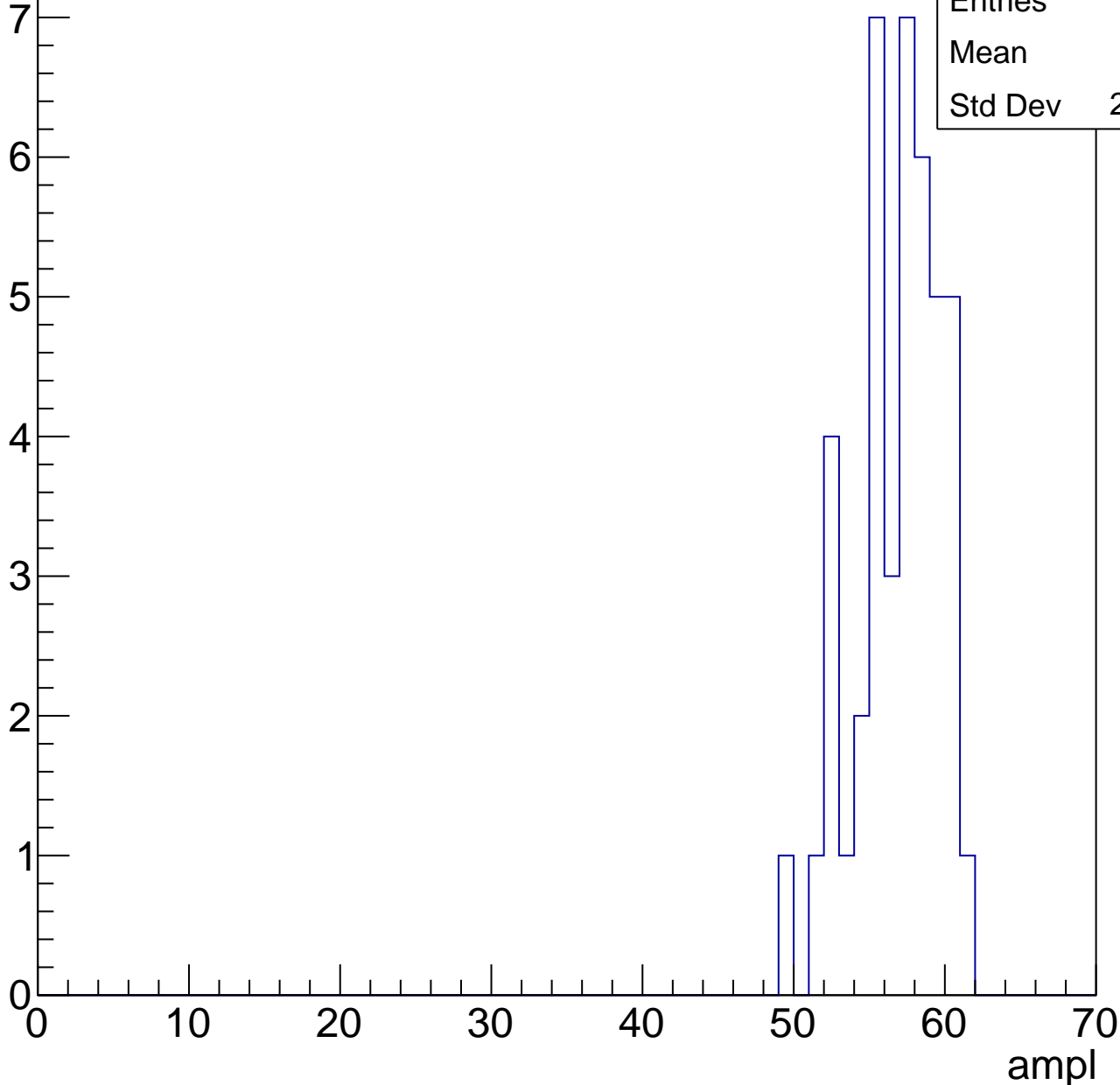


# B1L003S, U26-ch16, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	43
Mean	56.4
Std Dev	2.797

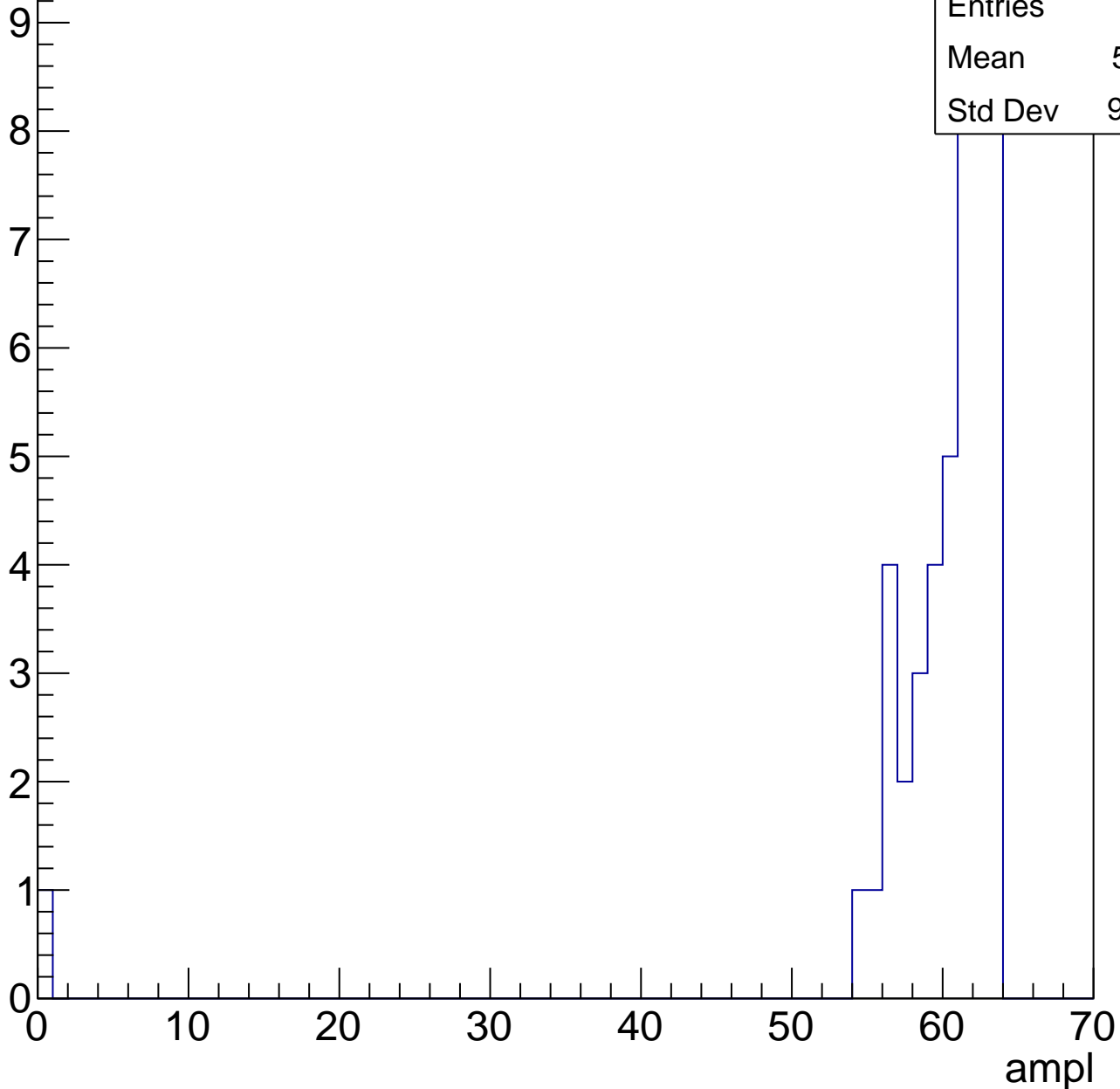


# B1L003S, U26-ch16, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	47
Mean	58.91
Std Dev	9.022



# B1L003S, U26-ch16, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

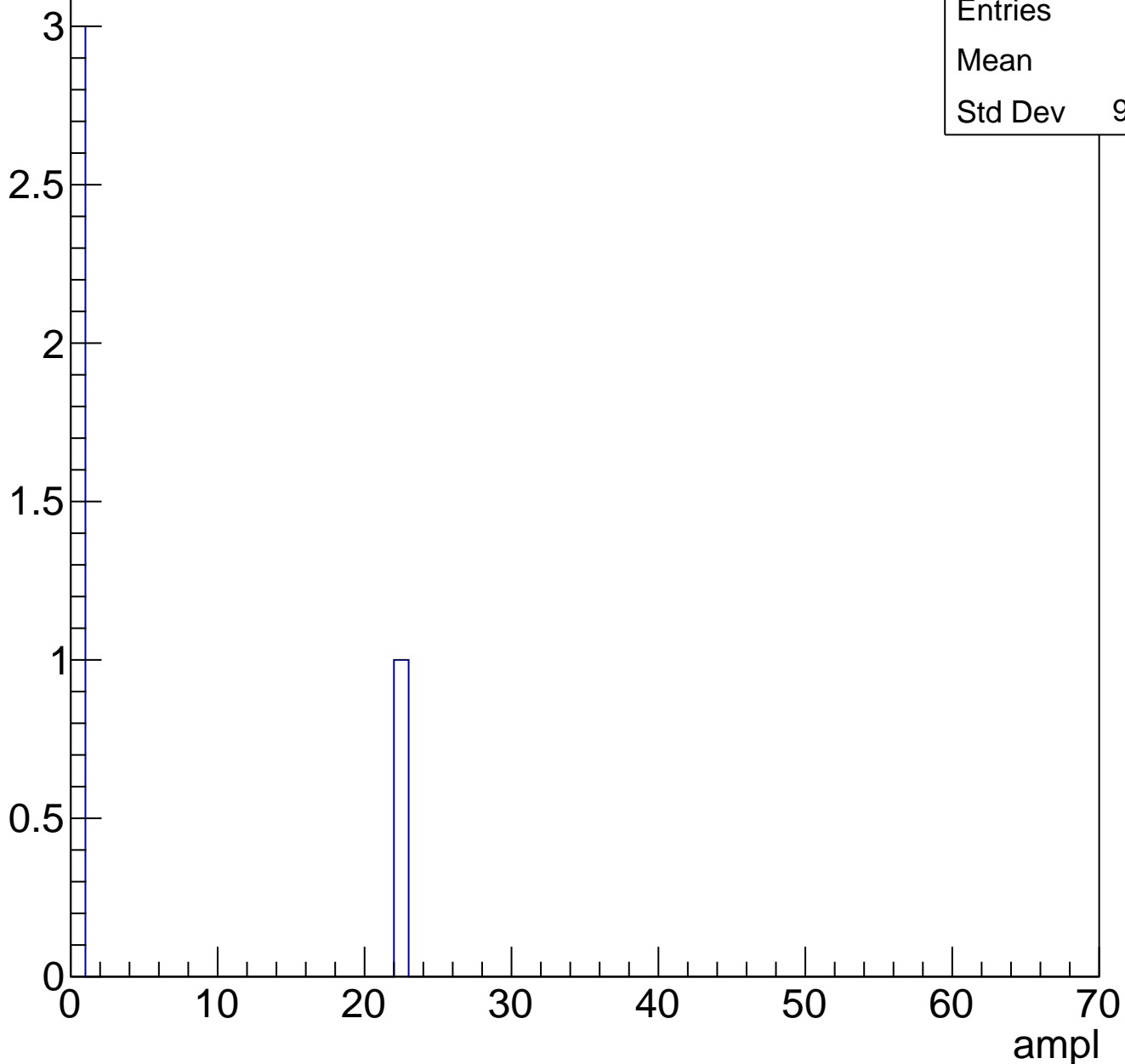




# B1L003S, U26-ch16, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	4
Mean	5.5
Std Dev	9.526

# B1L003S, U26-ch17, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	71
Mean	27.39
Std Dev	6.581

**Gaus mean : 29.3687**

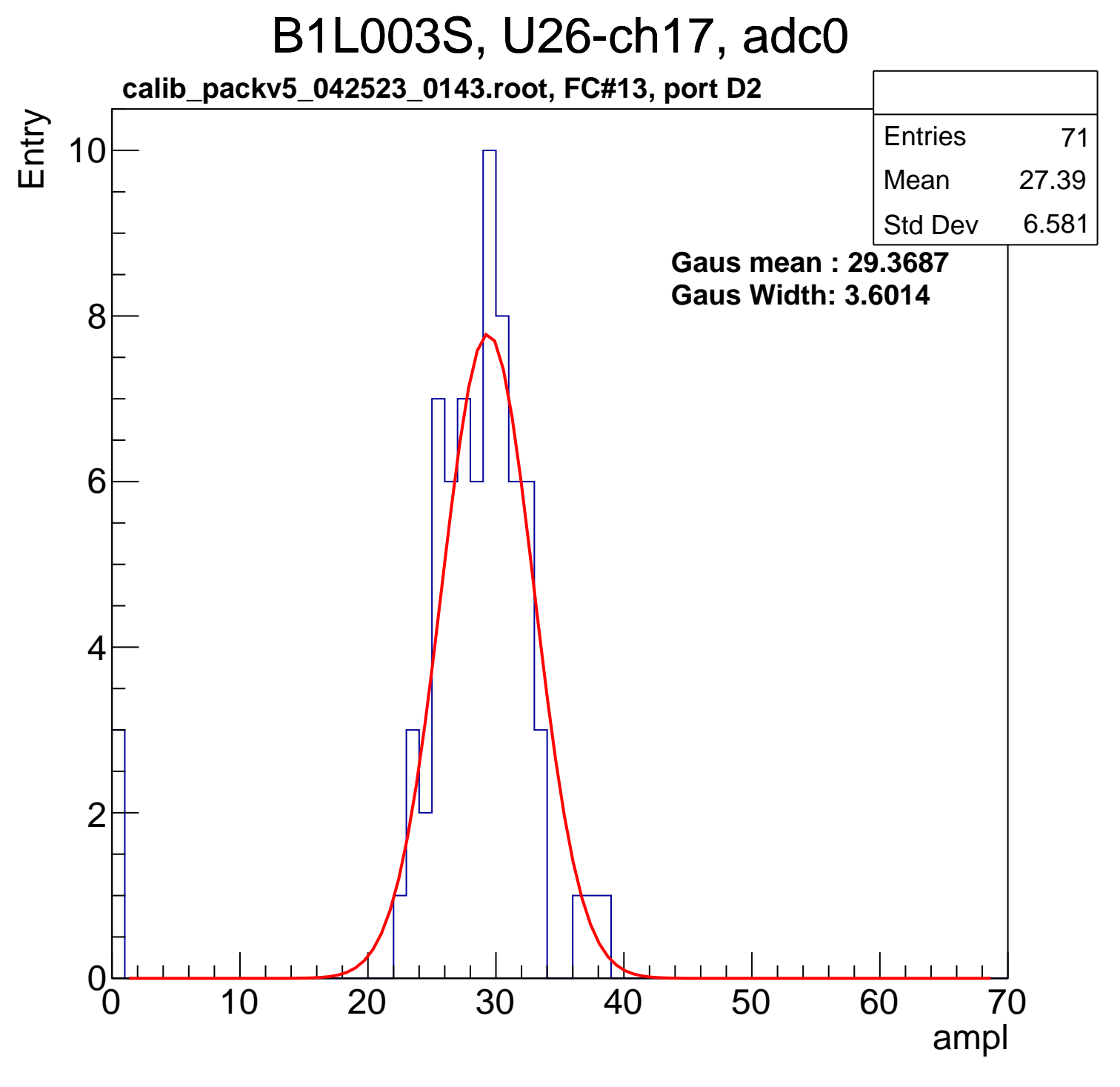
**Gaus Width: 3.6014**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



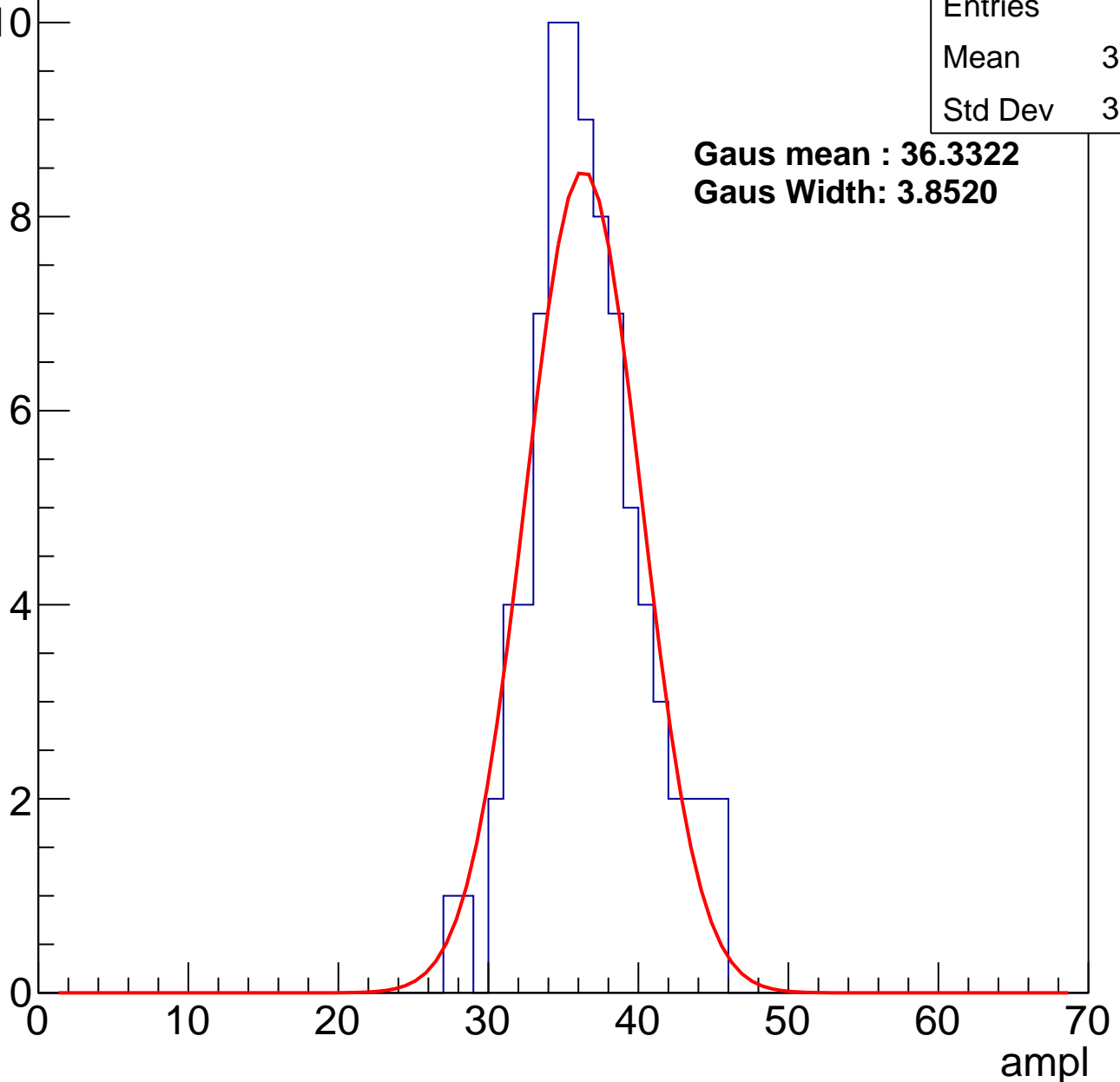
# B1L003S, U26-ch17, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	83
Mean	36.14
Std Dev	3.758

**Gaus mean : 36.3322**  
**Gaus Width: 3.8520**



# B1L003S, U26-ch17, adc2

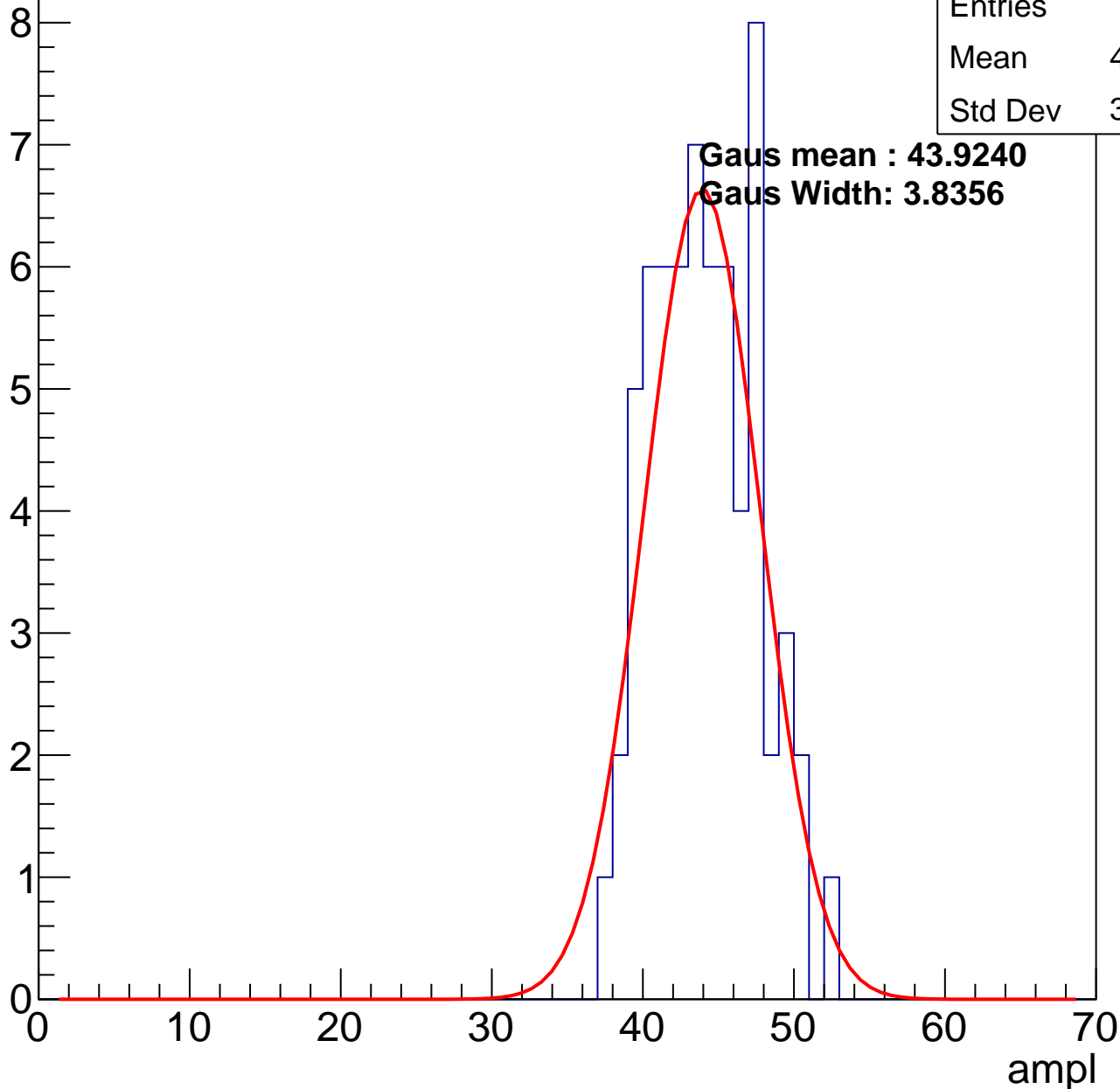
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	43.63
Std Dev	3.408

**Gaus mean : 43.9240**

**Gaus Width: 3.8356**

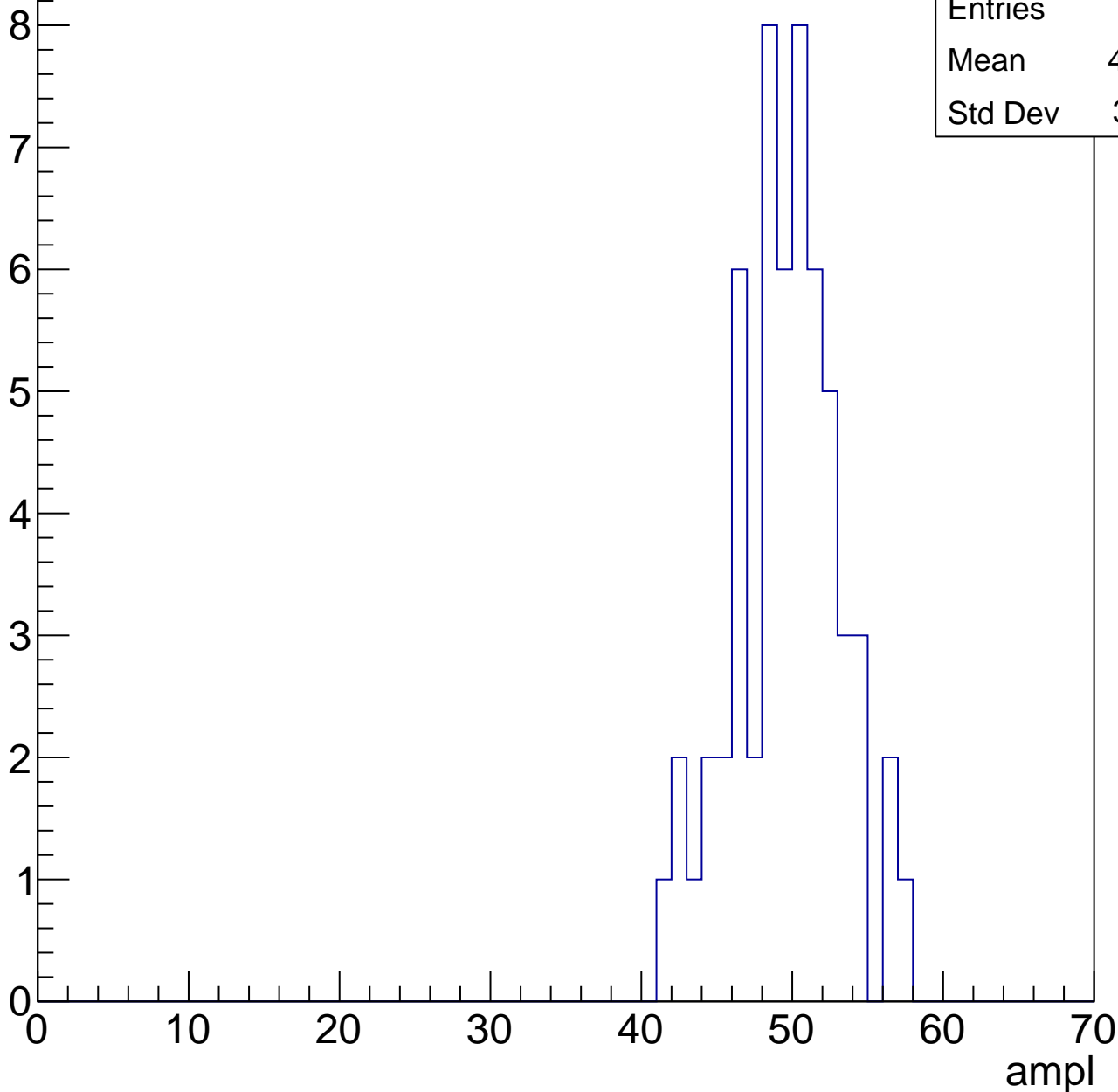


# B1L003S, U26-ch17, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	49.14
Std Dev	3.501

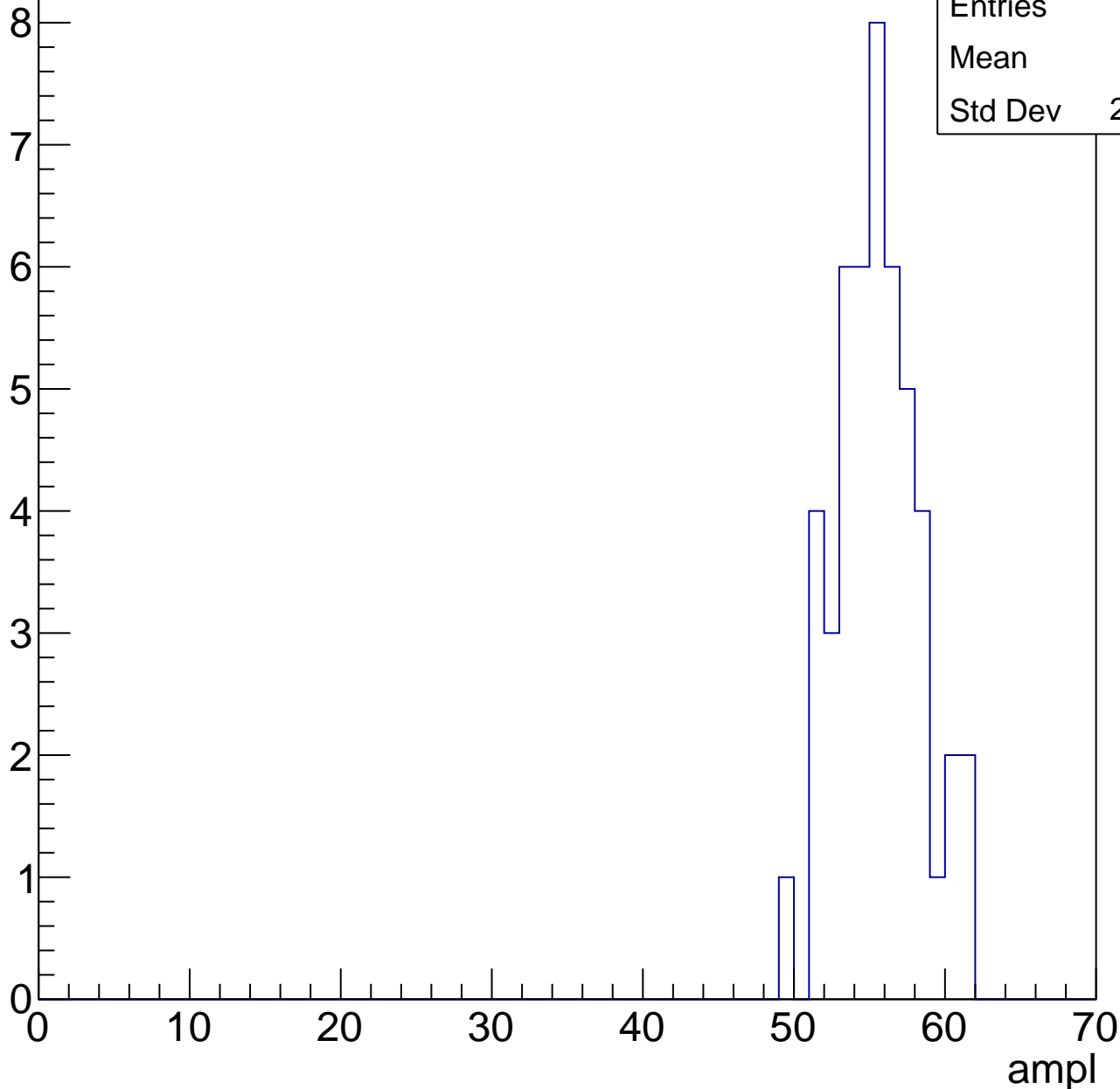


# B1L003S, U26-ch17, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	48
Mean	55.1
Std Dev	2.725



# B1L003S, U26-ch17, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

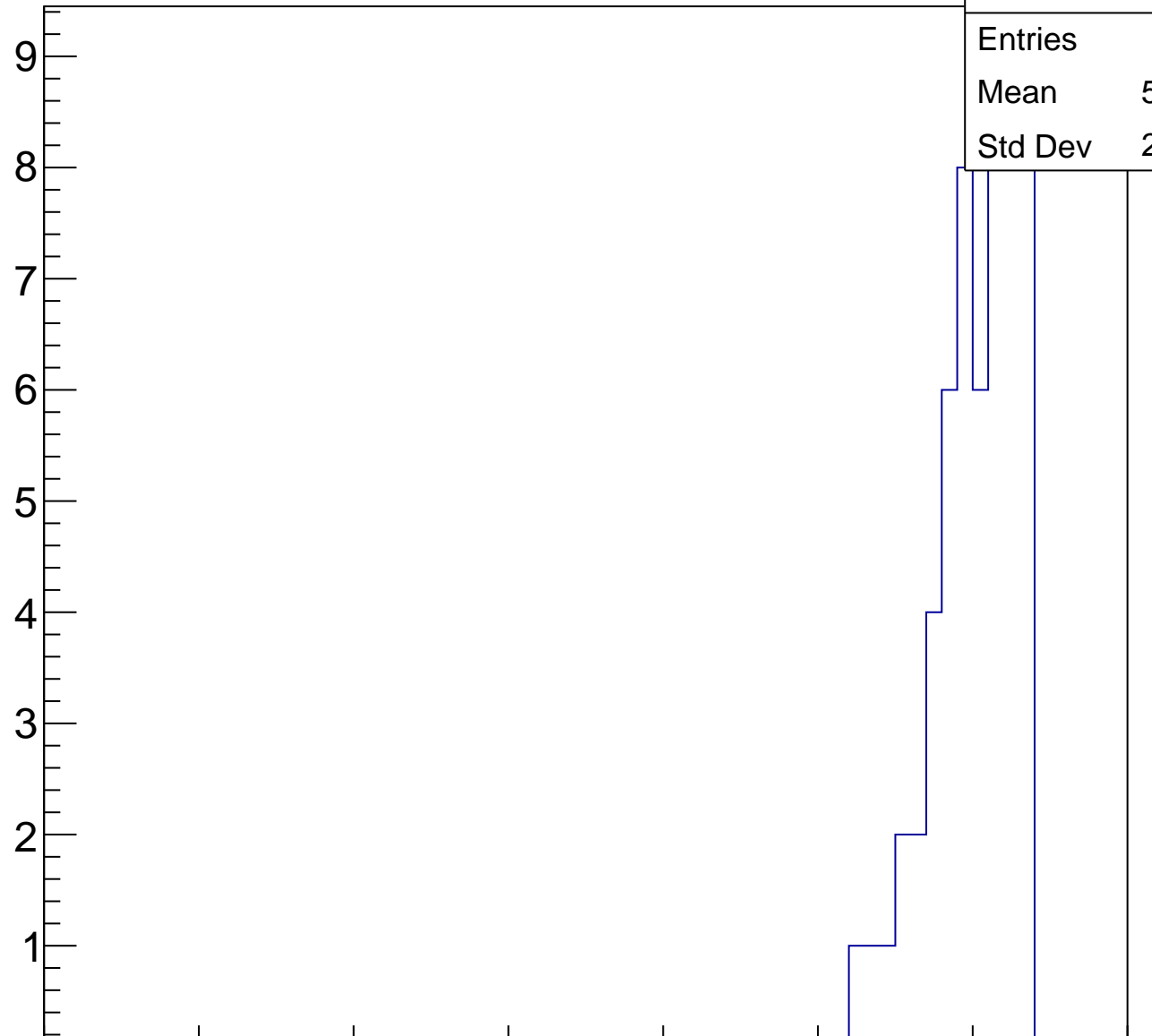
Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	56
Mean	59.64
Std Dev	2.715

ampl

0 10 20 30 40 50 60 70



# B1L003S, U26-ch17, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

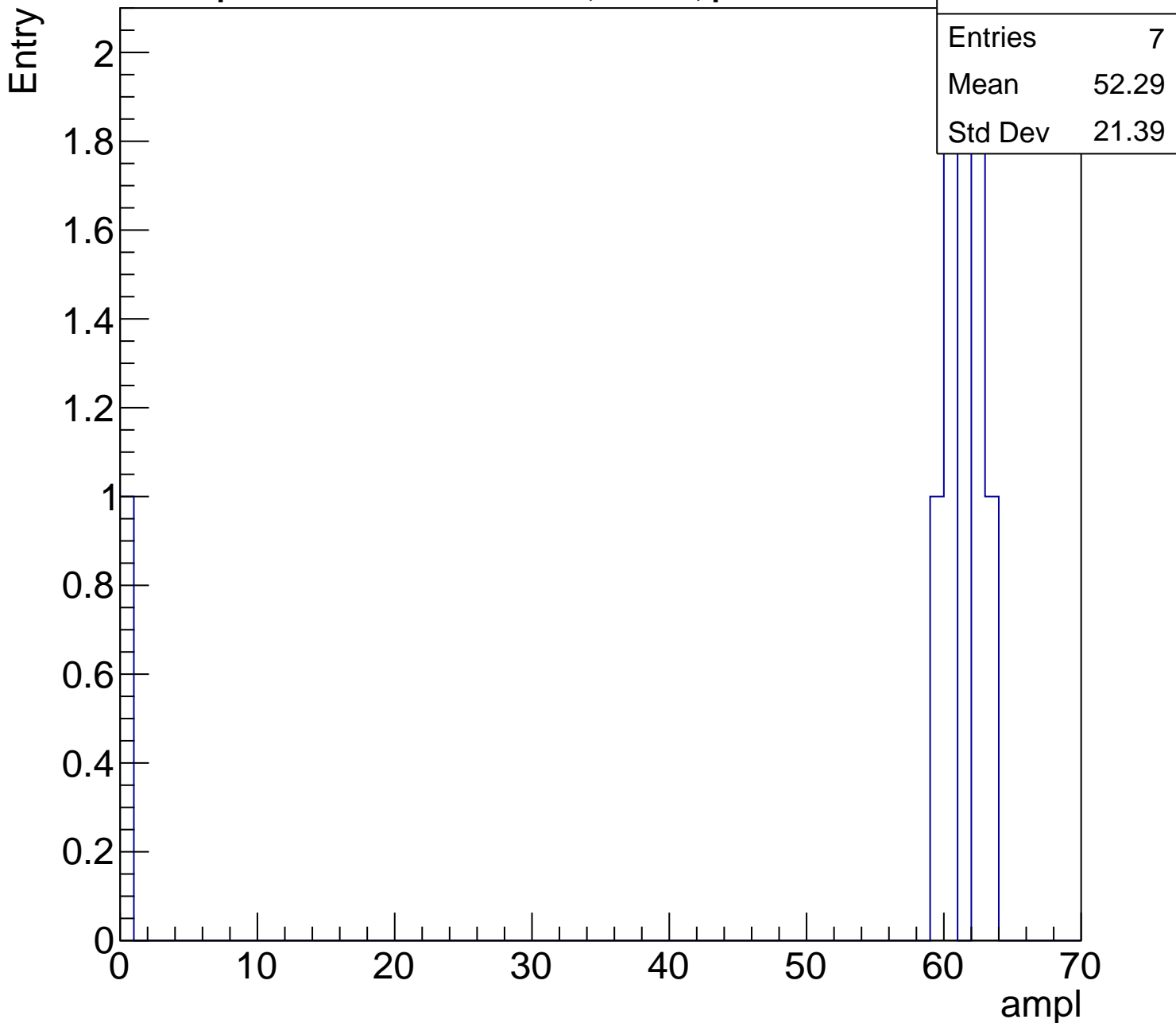
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	7
Mean	52.29
Std Dev	21.39

0 10 20 30 40 50 60 70

ampl





# B1L003S, U26-ch17, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L003S, U26-ch18, adc0

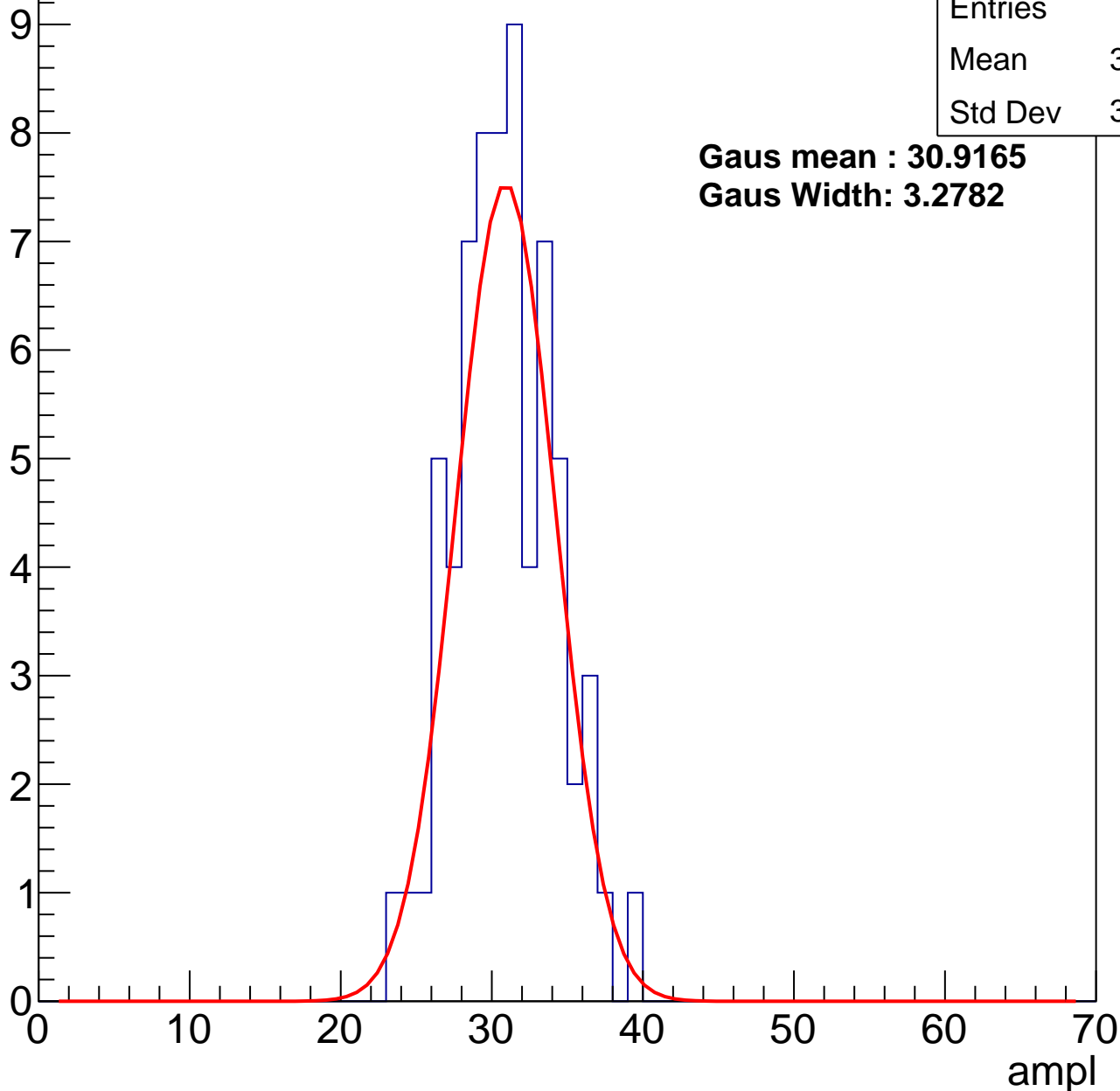
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	30.45
Std Dev	3.243

**Gaus mean : 30.9165**

**Gaus Width: 3.2782**



# B1L003S, U26-ch18, adc1

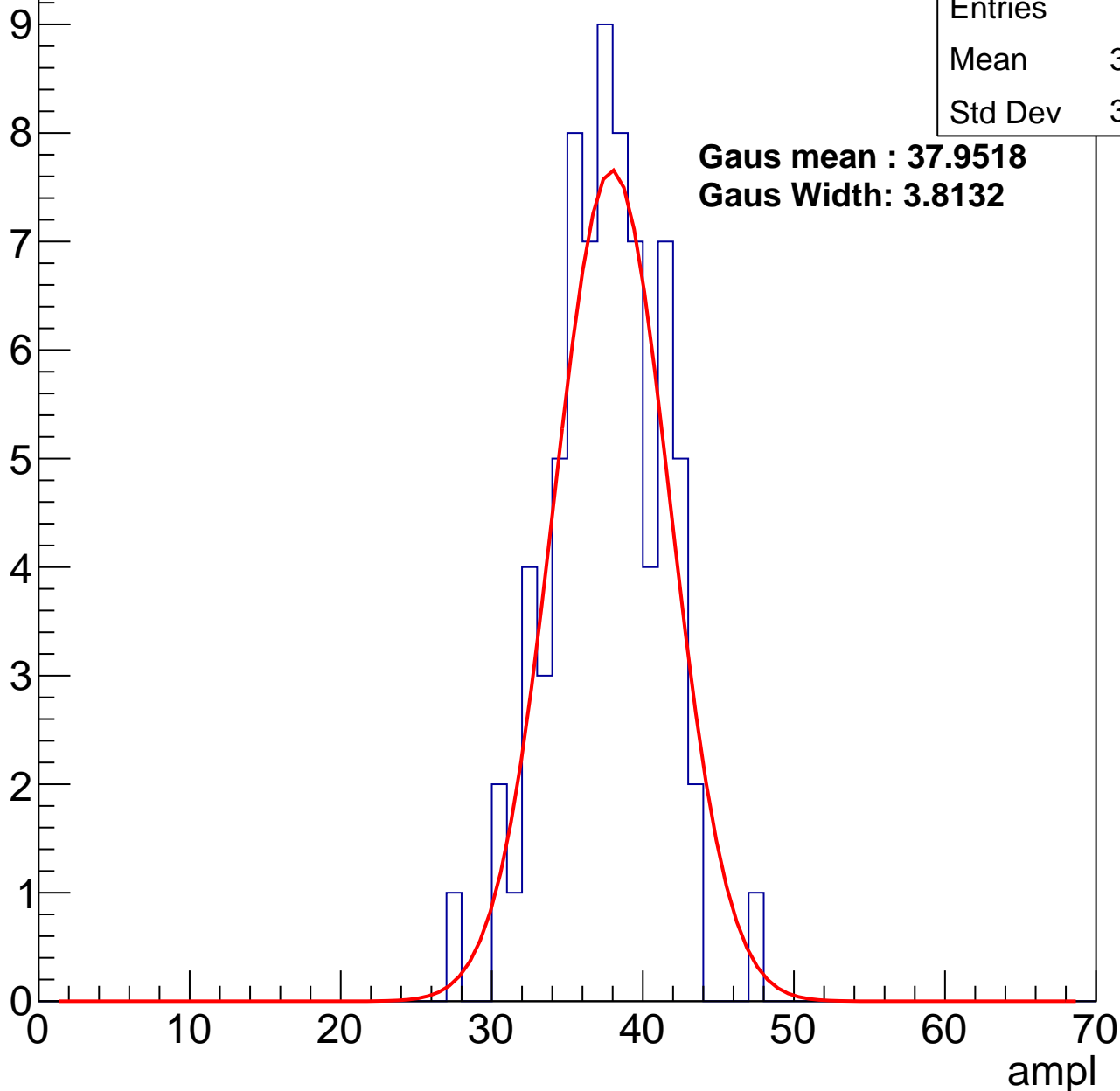
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	74
Mean	37.12
Std Dev	3.575

**Gaus mean : 37.9518**

**Gaus Width: 3.8132**



# B1L003S, U26-ch18, adc2

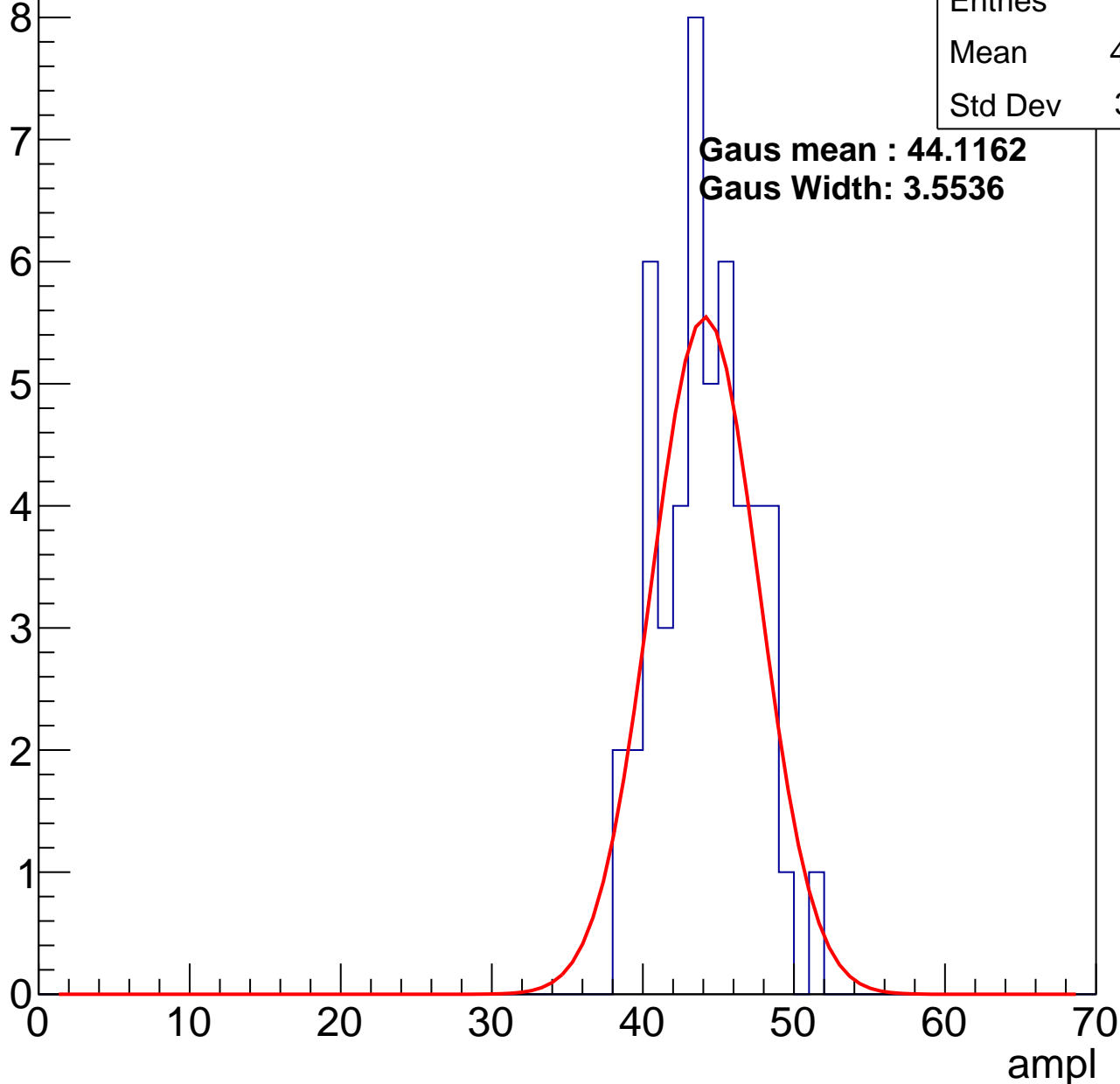
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	50
Mean	43.66
Std Dev	3.031

**Gaus mean : 44.1162**

**Gaus Width: 3.5536**

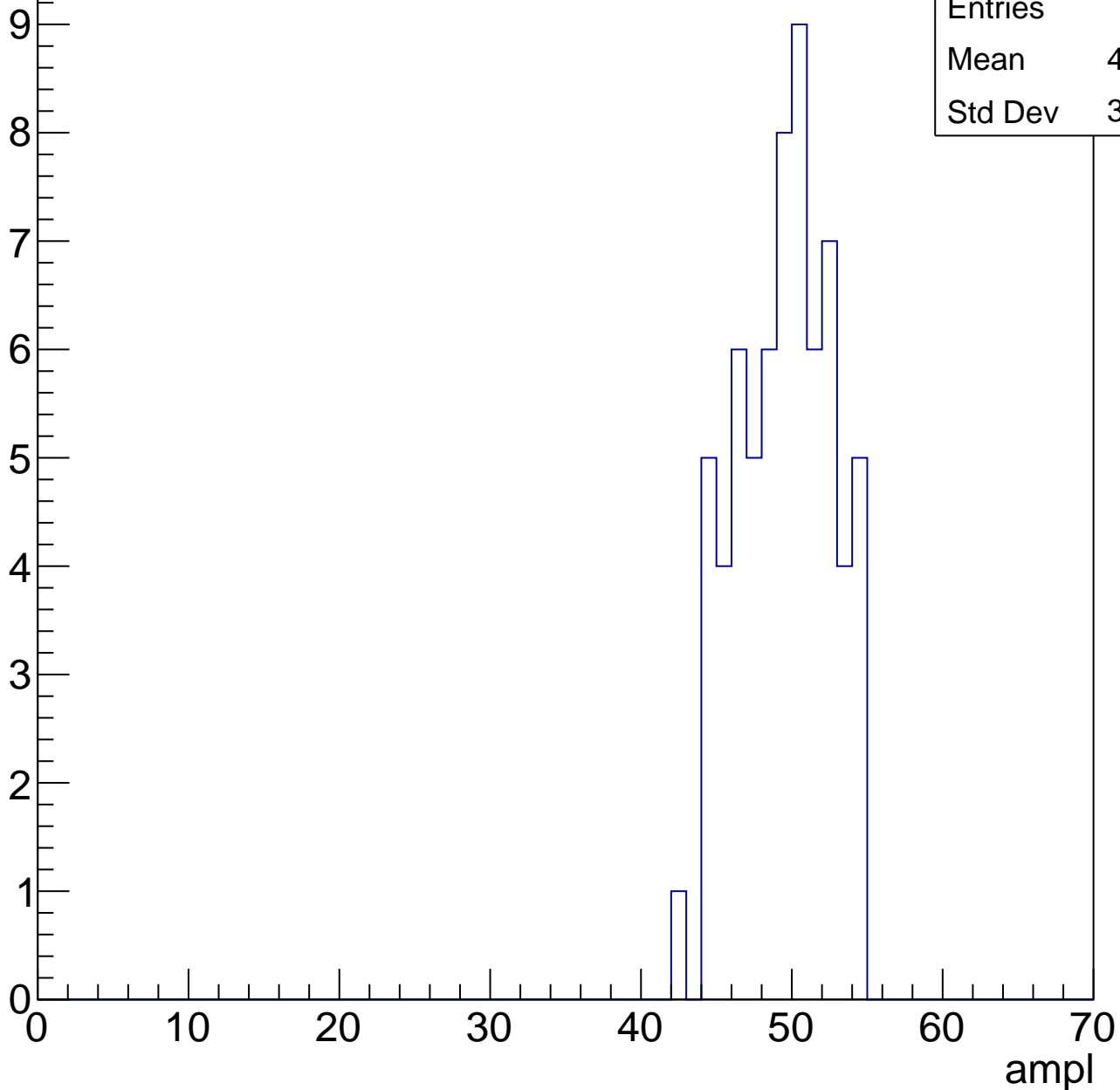


# B1L003S, U26-ch18, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	49.02
Std Dev	3.023



# B1L003S, U26-ch18, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	55
Mean	55.73
Std Dev	2.975

Entry

10

8

6

4

2

0

0

10

20

30

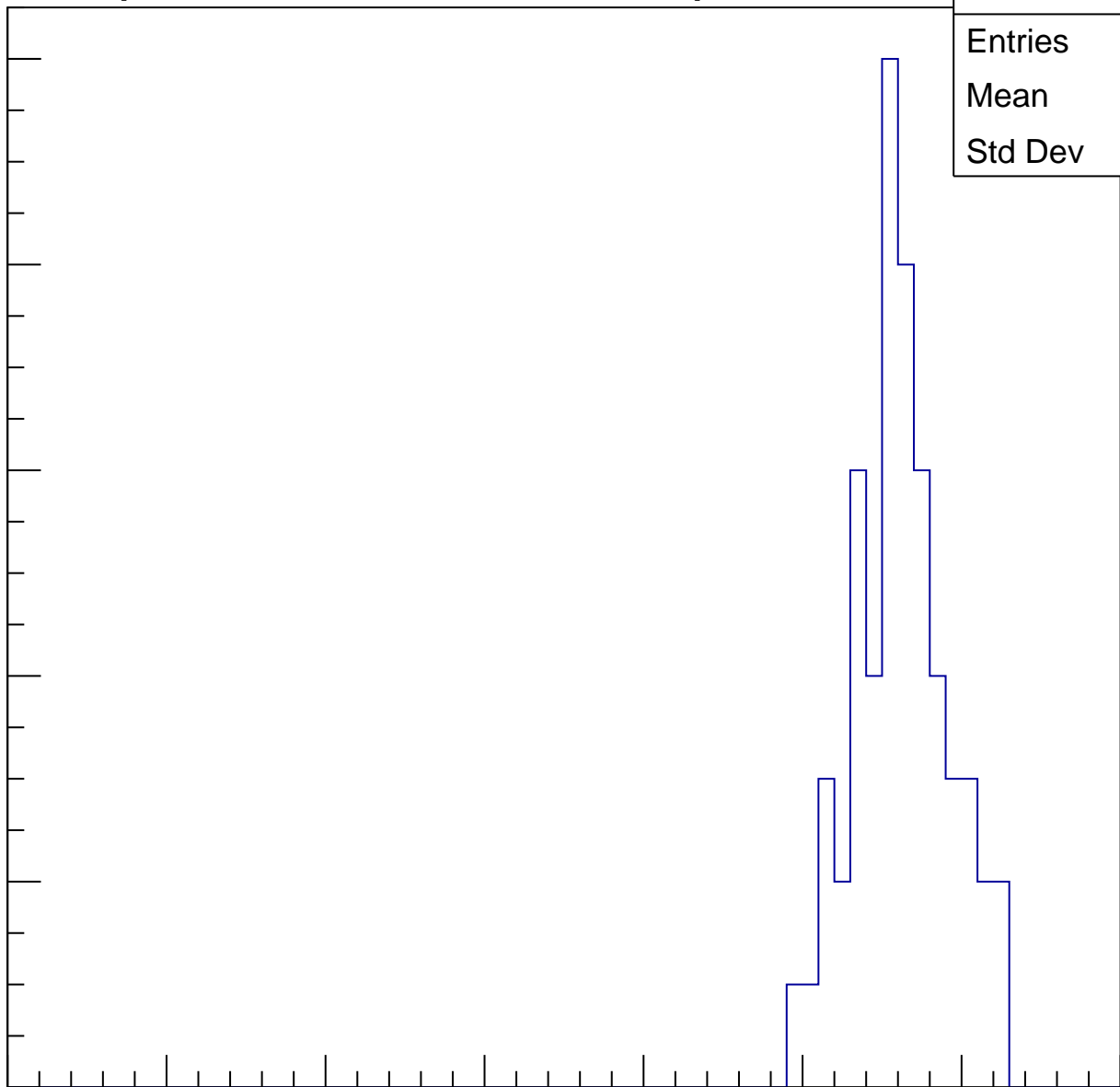
40

50

60

70

ampl

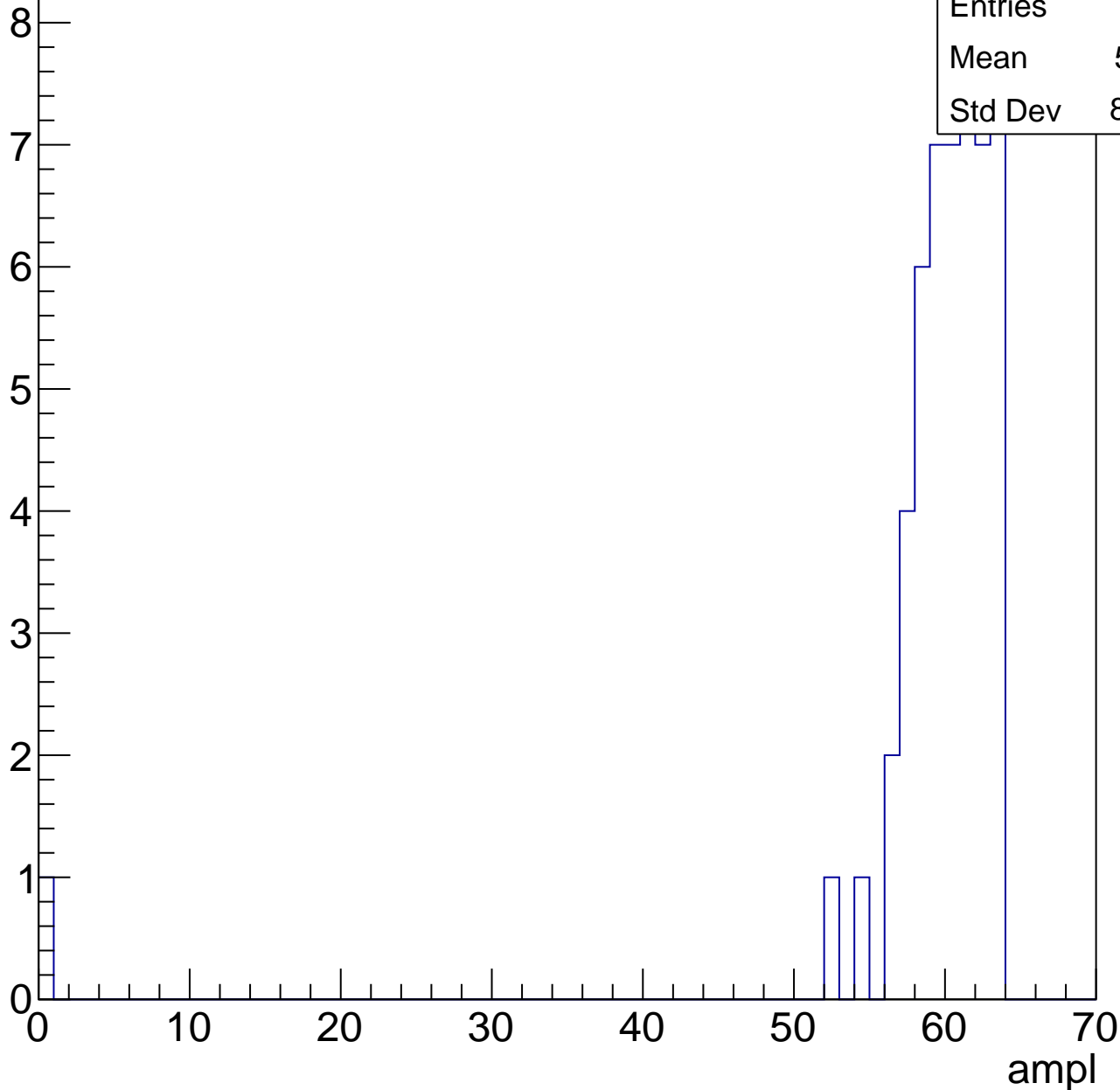


# B1L003S, U26-ch18, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	52
Mean	58.71
Std Dev	8.572



# B1L003S, U26-ch18, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch18, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U26-ch19, adc0

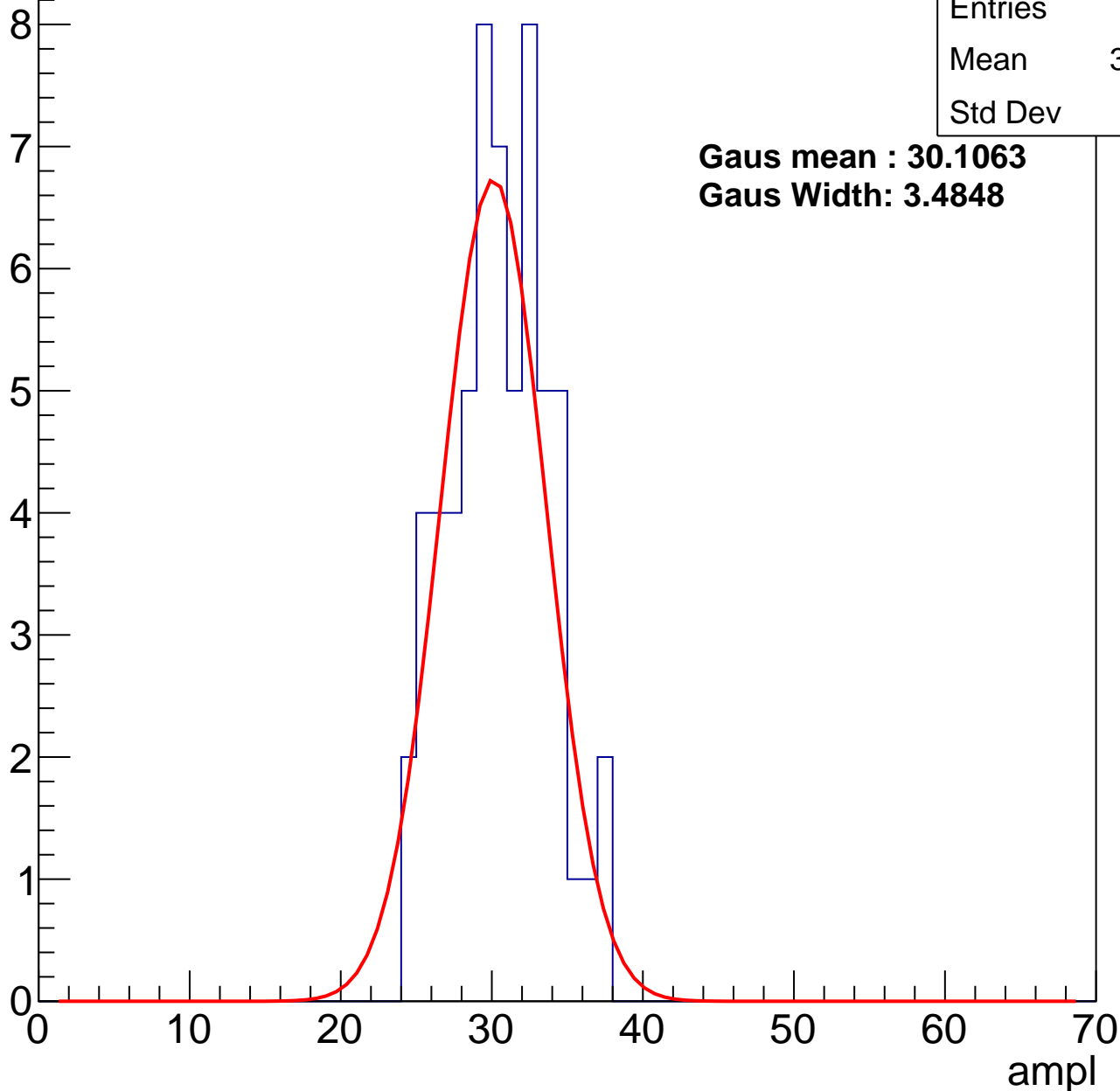
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	30.05
Std Dev	3.19

**Gaus mean : 30.1063**

**Gaus Width: 3.4848**



# B1L003S, U26-ch19, adc1

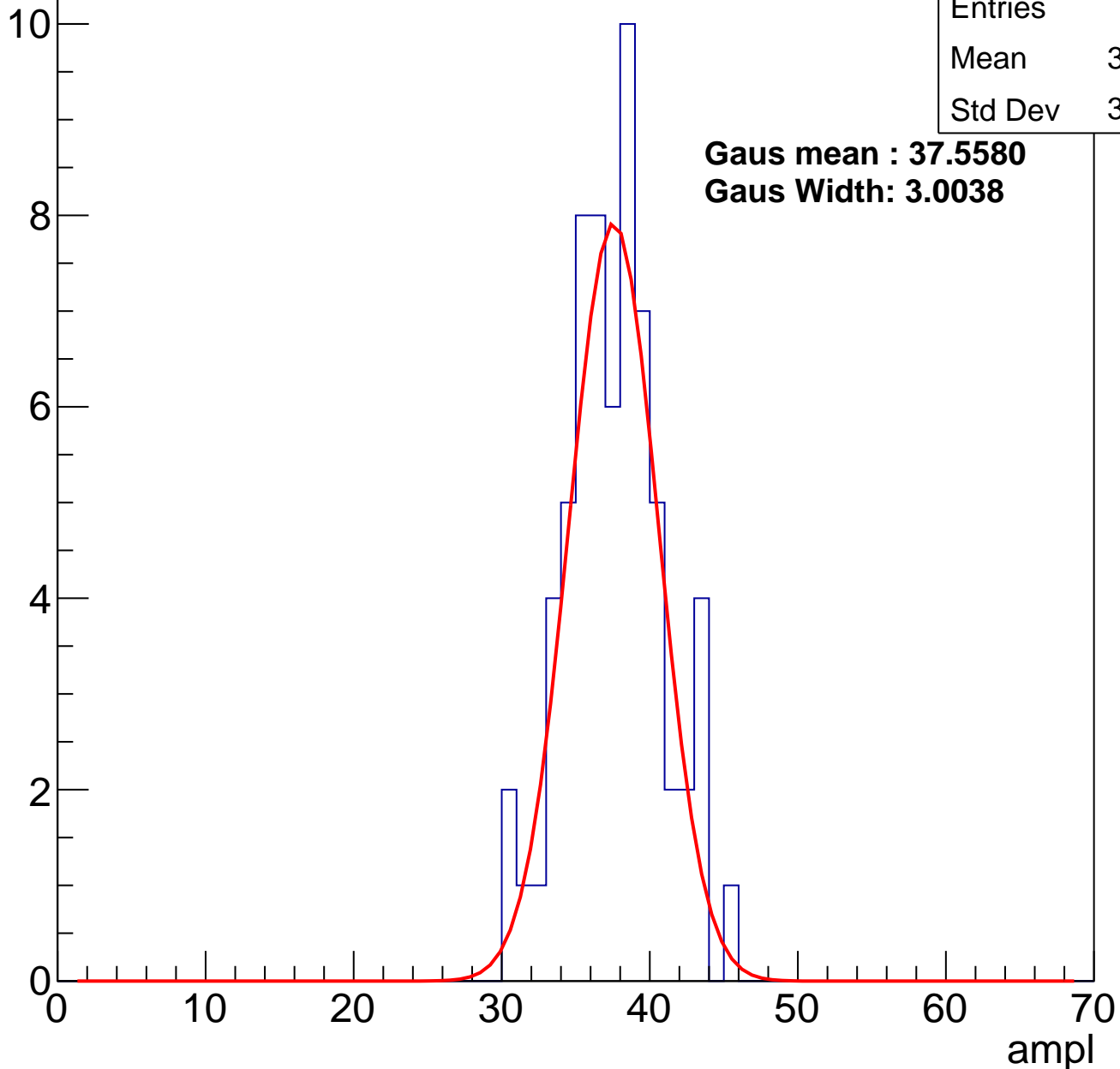
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	66
Mean	37.14
Std Dev	3.209

**Gaus mean : 37.5580**

**Gaus Width: 3.0038**

Entry



# B1L003S, U26-ch19, adc2

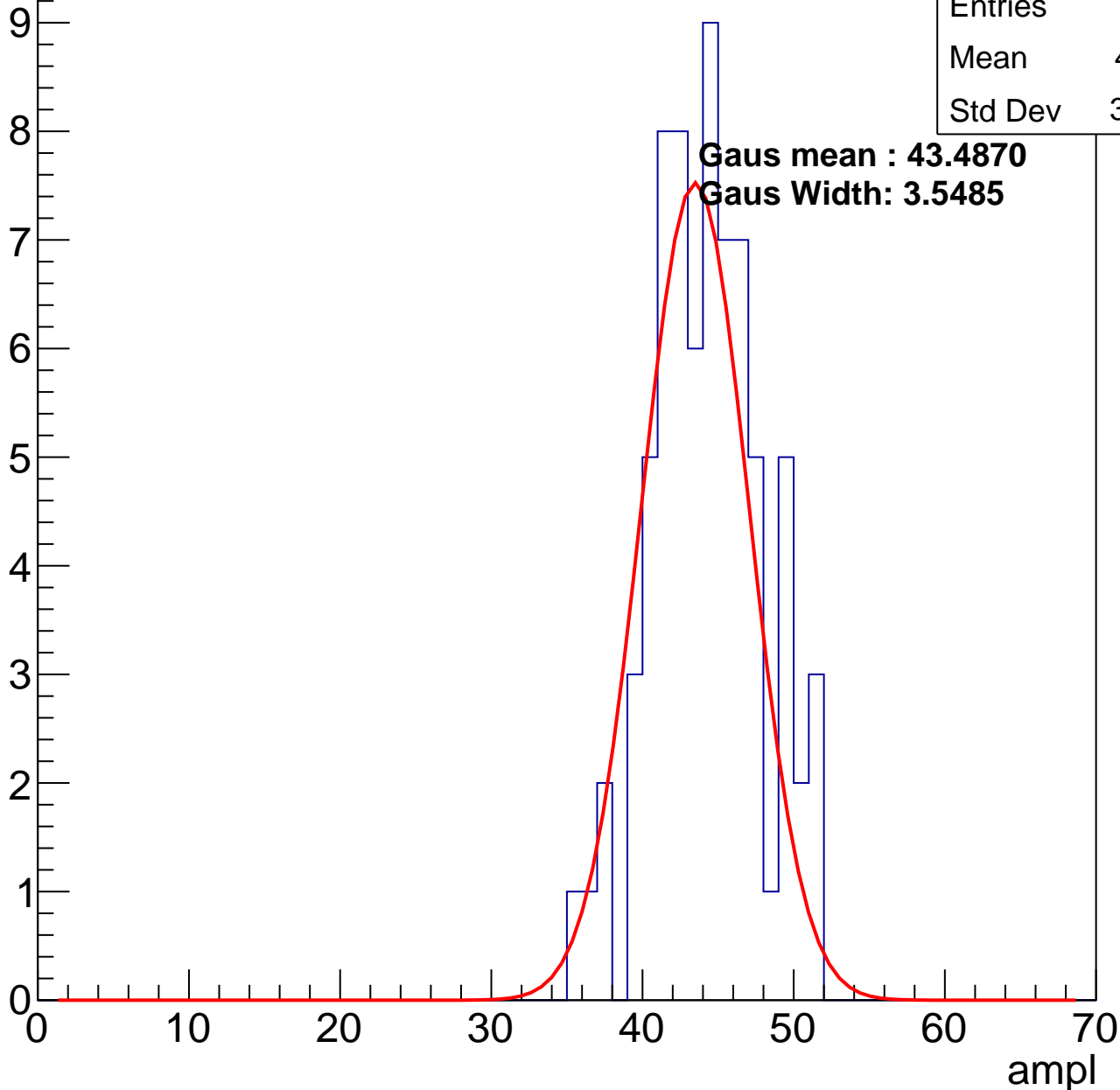
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	73
Mean	43.81
Std Dev	3.599

**Gaus mean : 43.4870**

**Gaus Width: 3.5485**

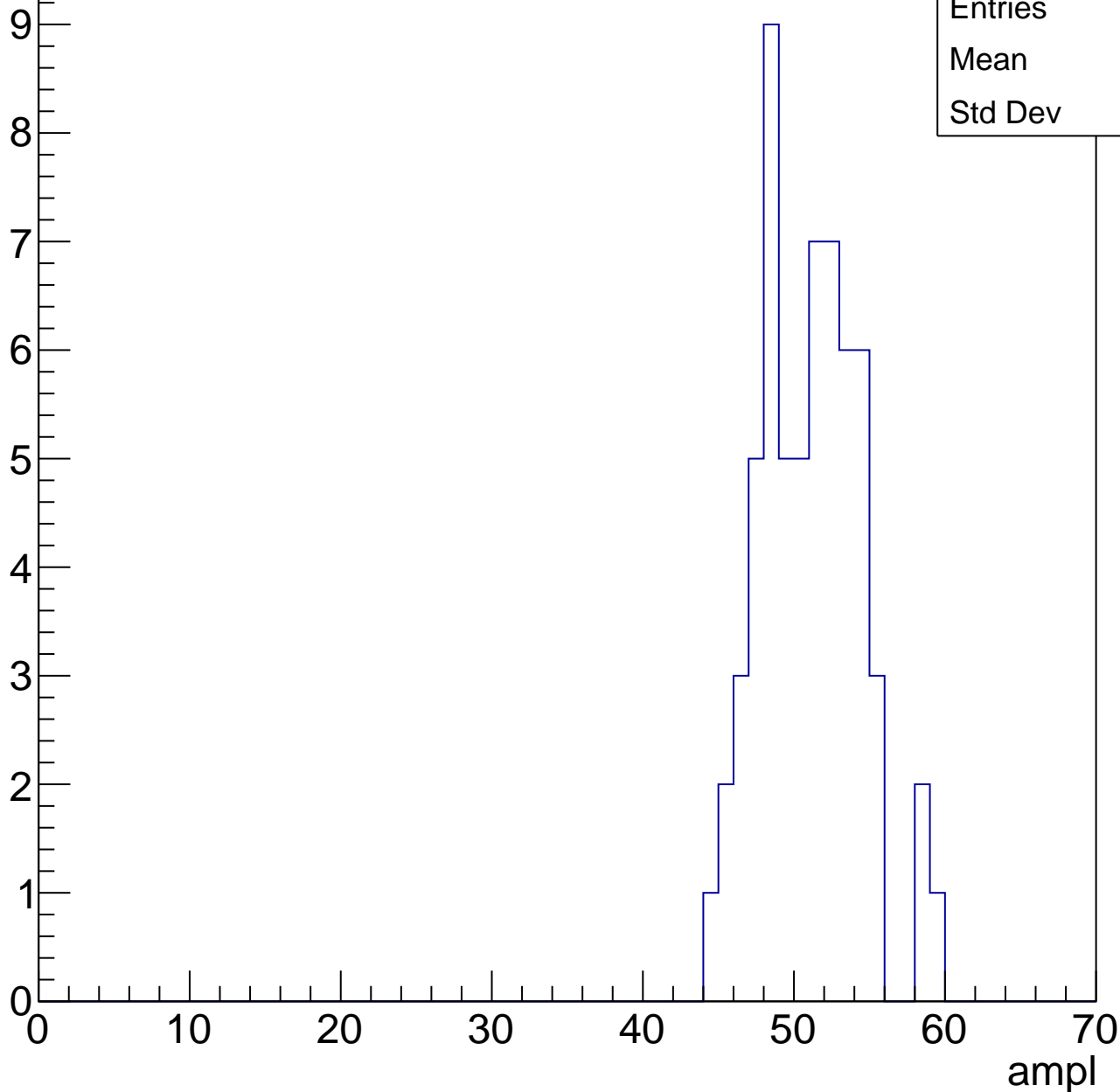


# B1L003S, U26-ch19, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	50.6
Std Dev	3.28

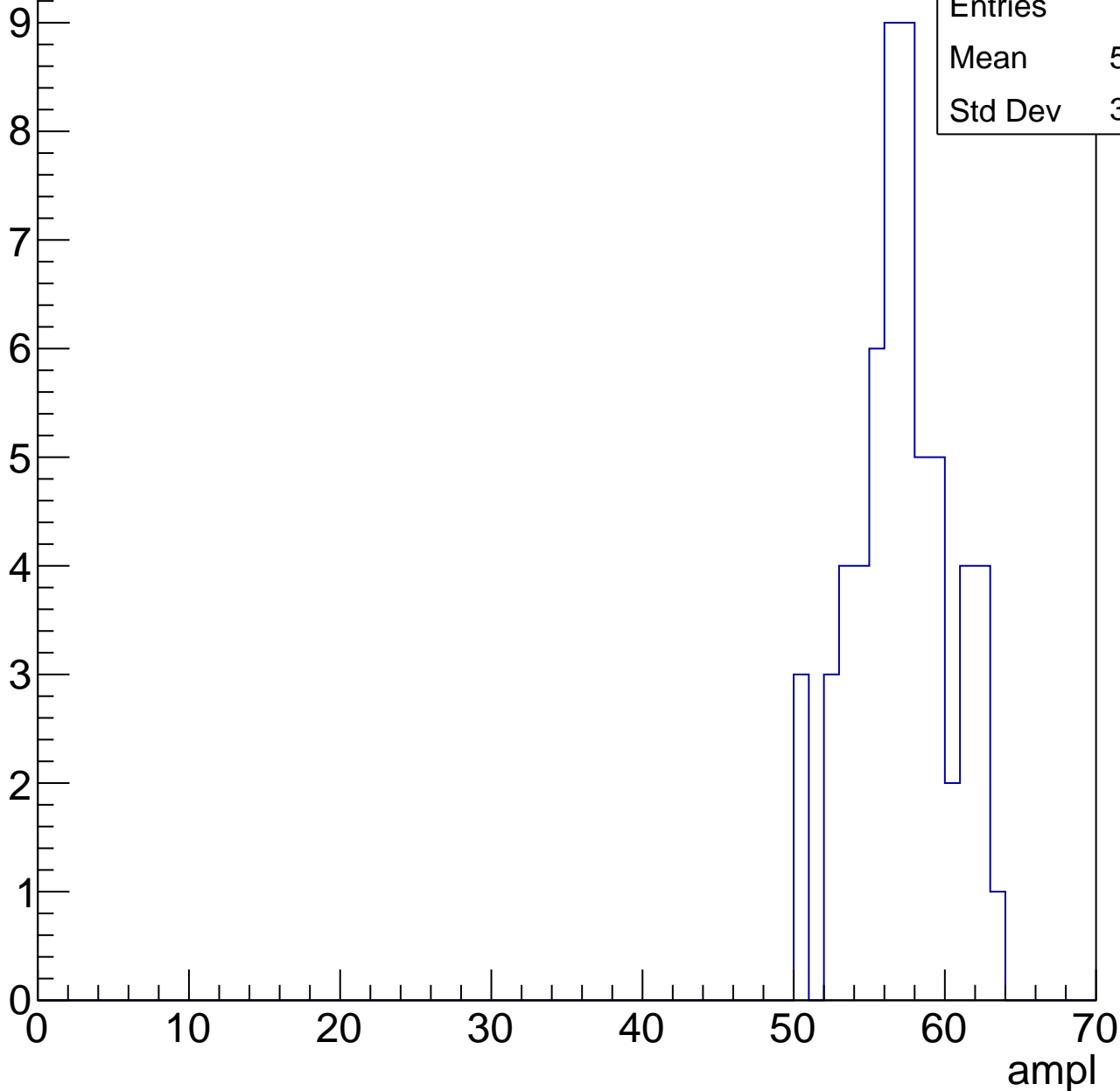


# B1L003S, U26-ch19, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	56.63
Std Dev	3.162

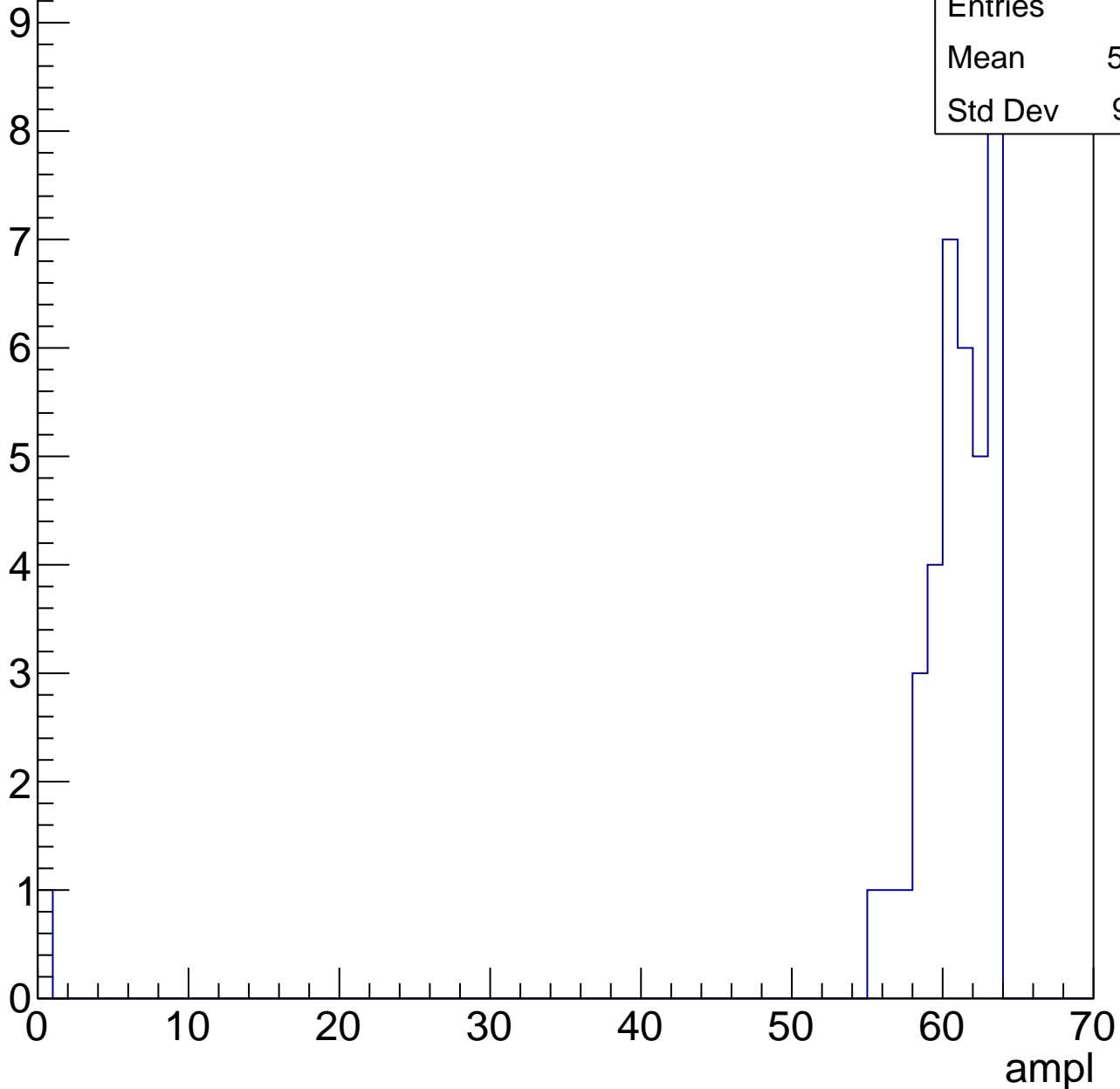


# B1L003S, U26-ch19, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	38
Mean	58.97
Std Dev	9.911



# B1L003S, U26-ch19, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch19, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U26-ch20, adc0

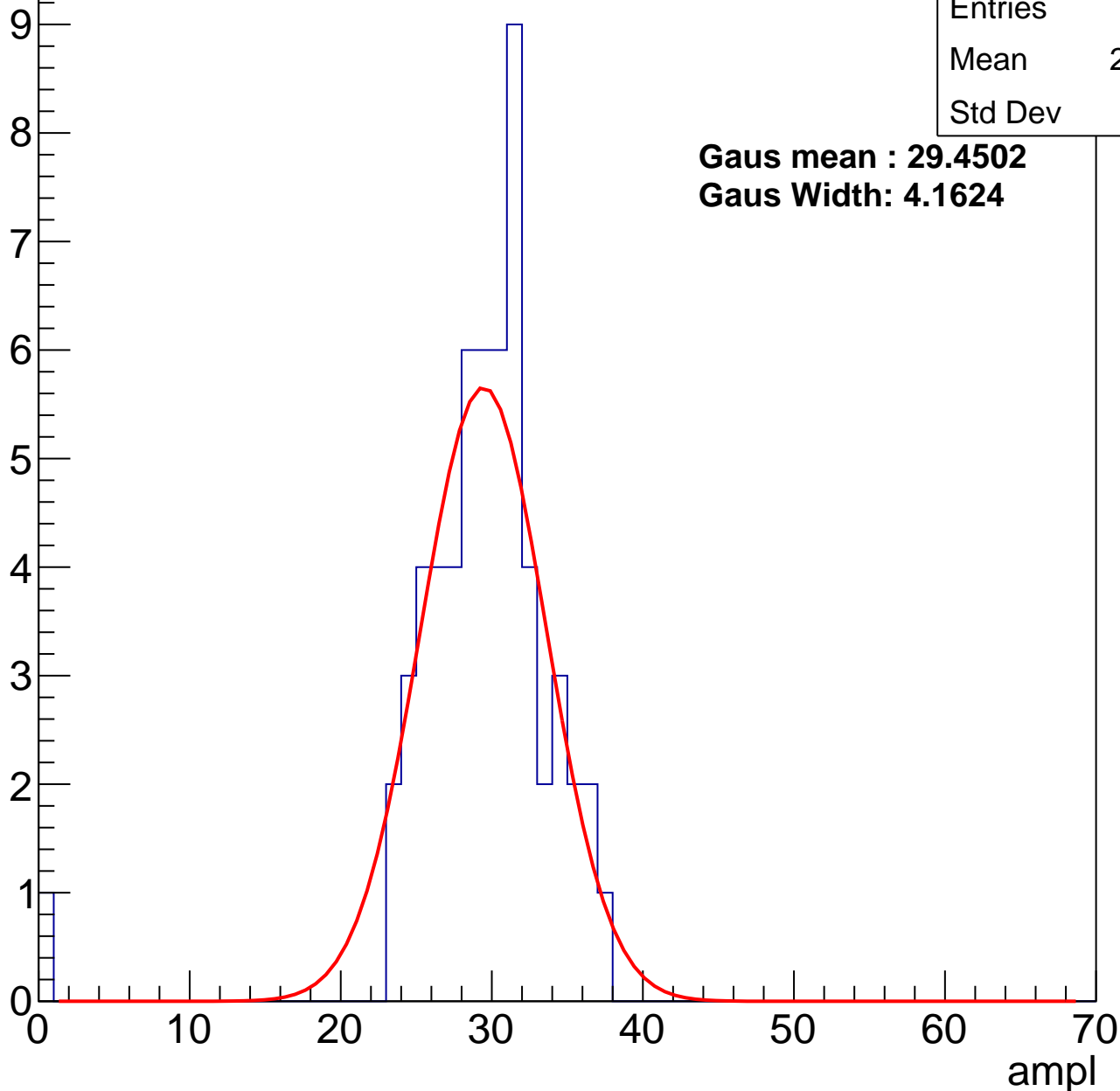
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	28.92
Std Dev	5.09

**Gaus mean : 29.4502**

**Gaus Width: 4.1624**



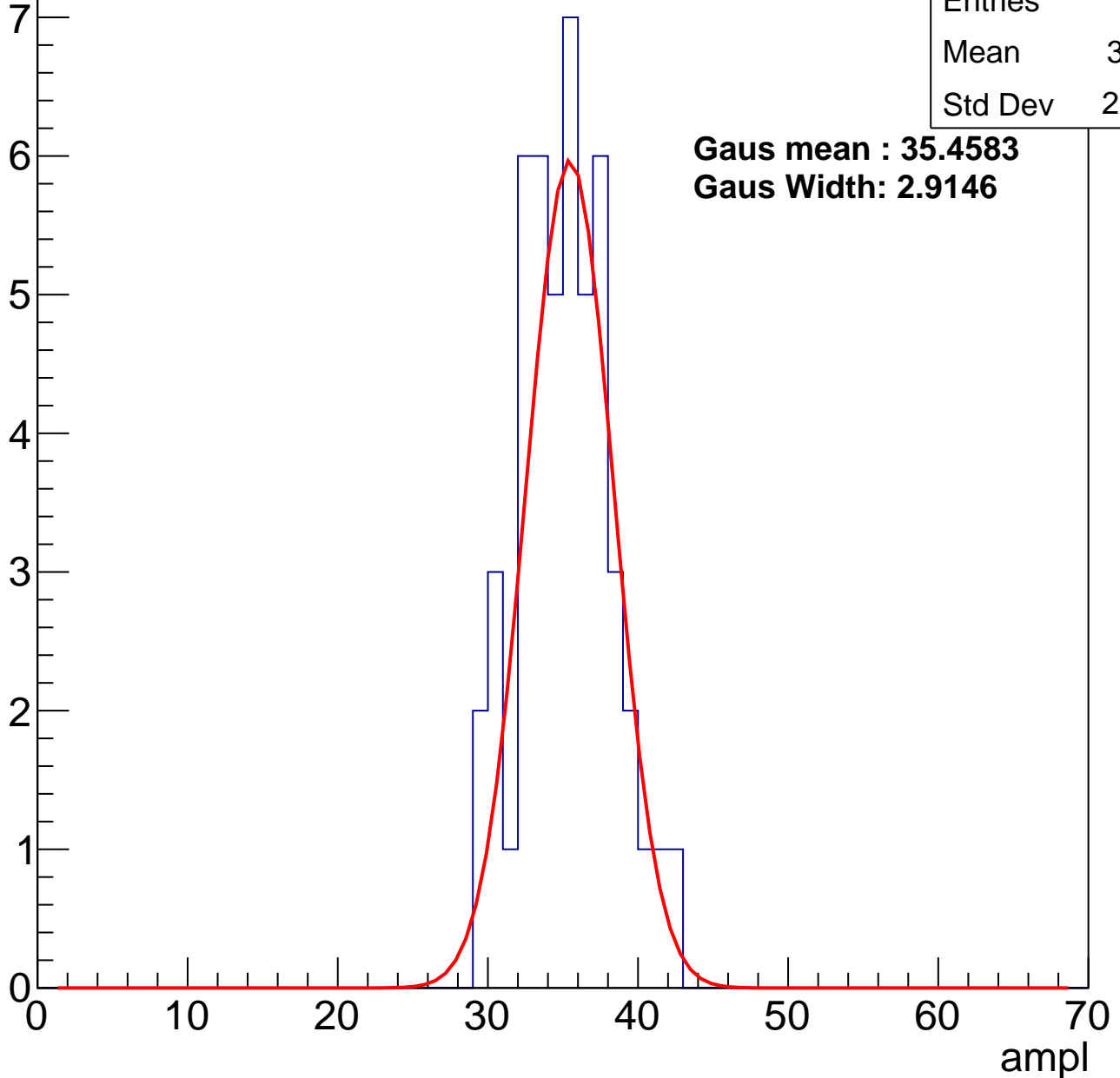
# B1L003S, U26-ch20, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

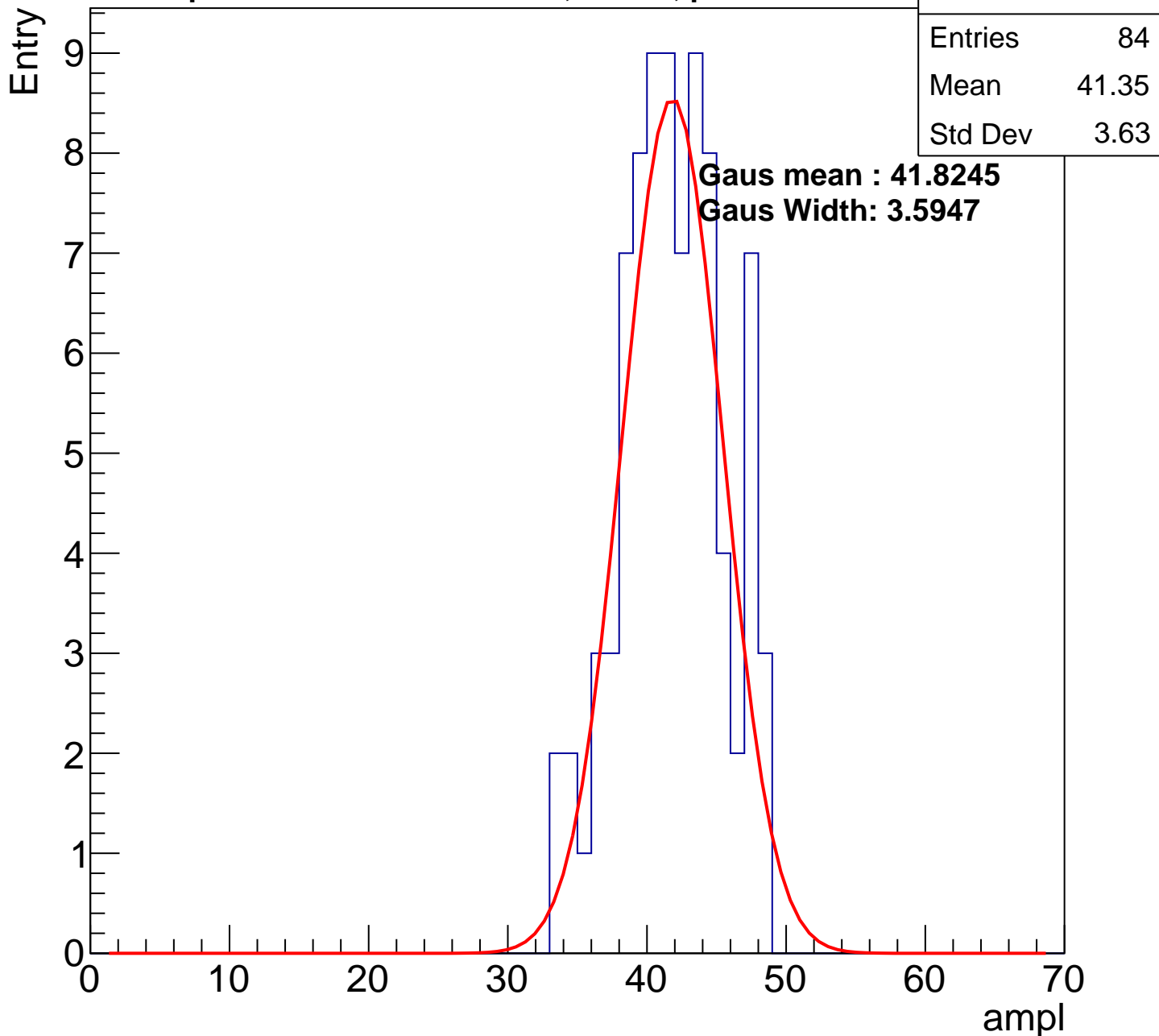
Entries	49
Mean	34.71
Std Dev	2.997

**Gaus mean : 35.4583**  
**Gaus Width: 2.9146**



# B1L003S, U26-ch20, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

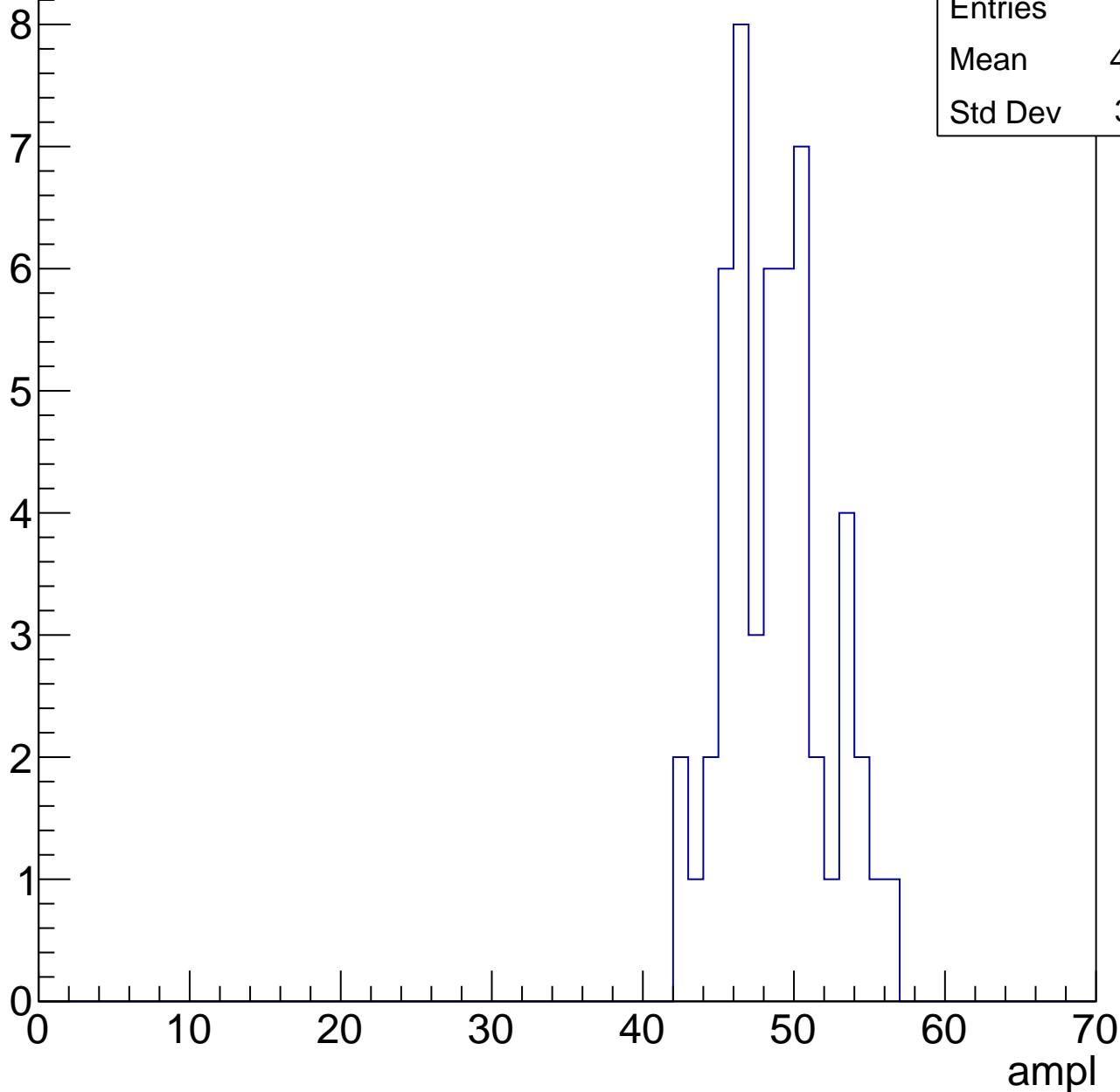


# B1L003S, U26-ch20, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

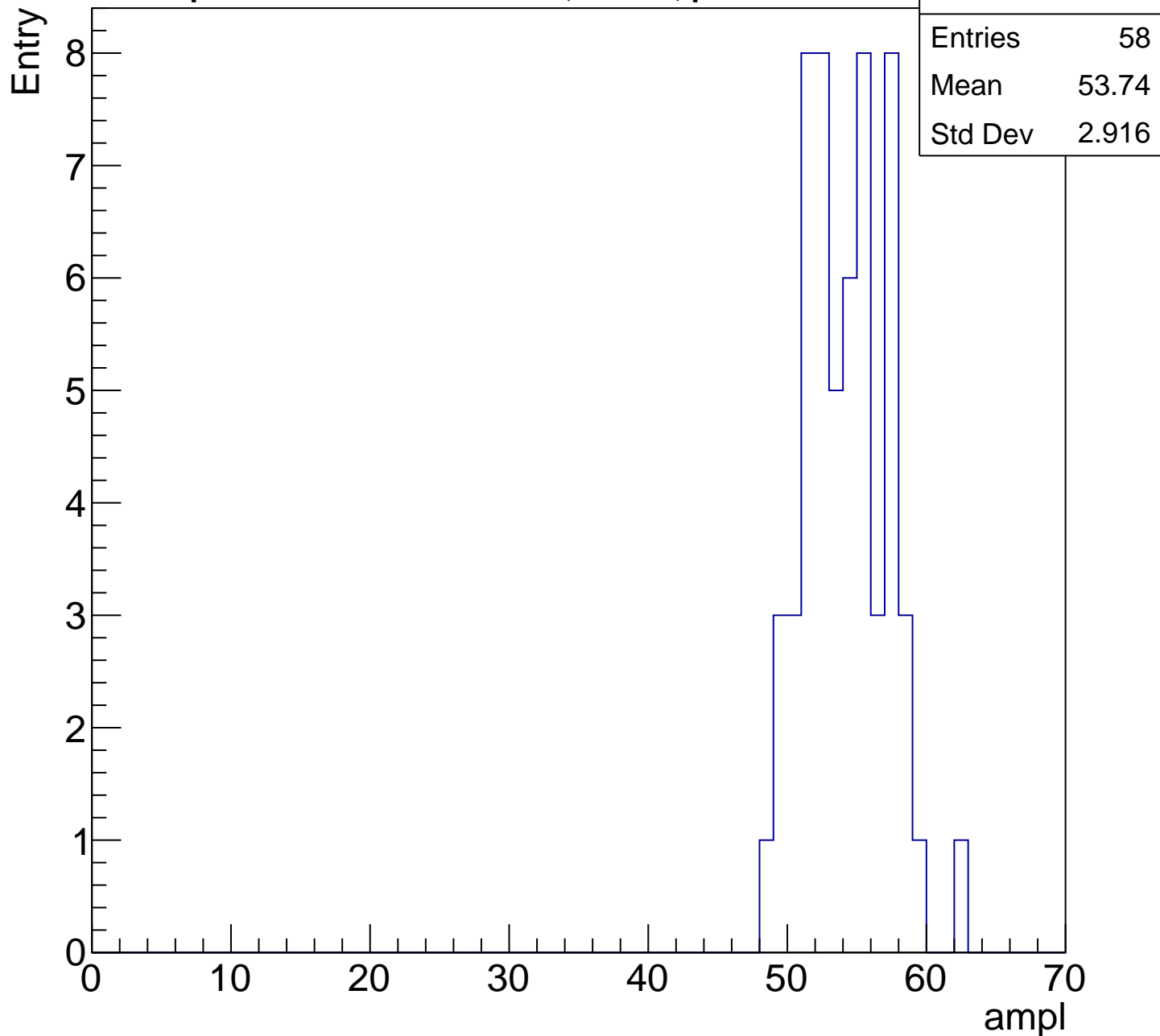
Entry

Entries	52
Mean	48.29
Std Dev	3.301



# B1L003S, U26-ch20, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

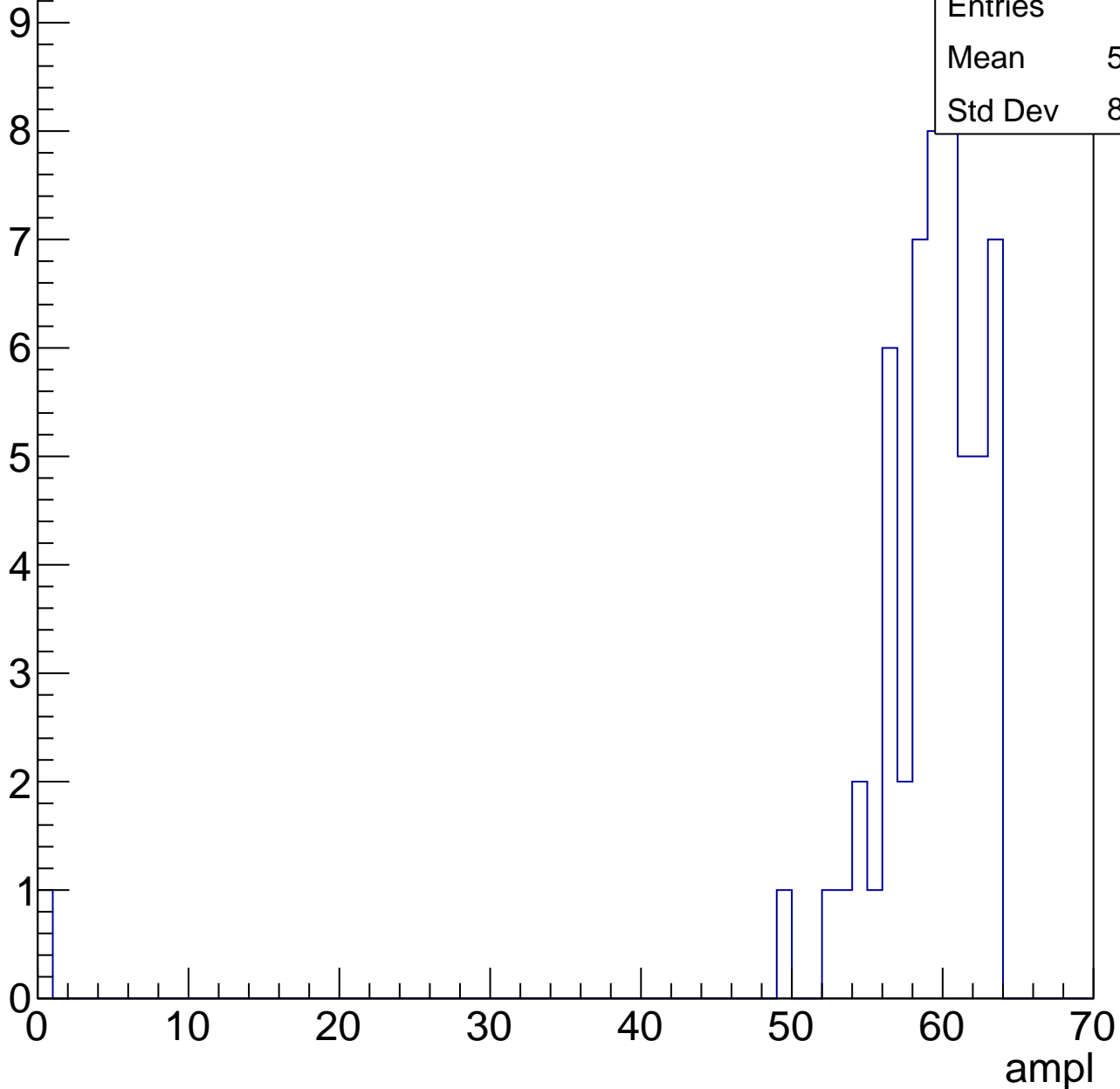


# B1L003S, U26-ch20, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	57.88
Std Dev	8.362

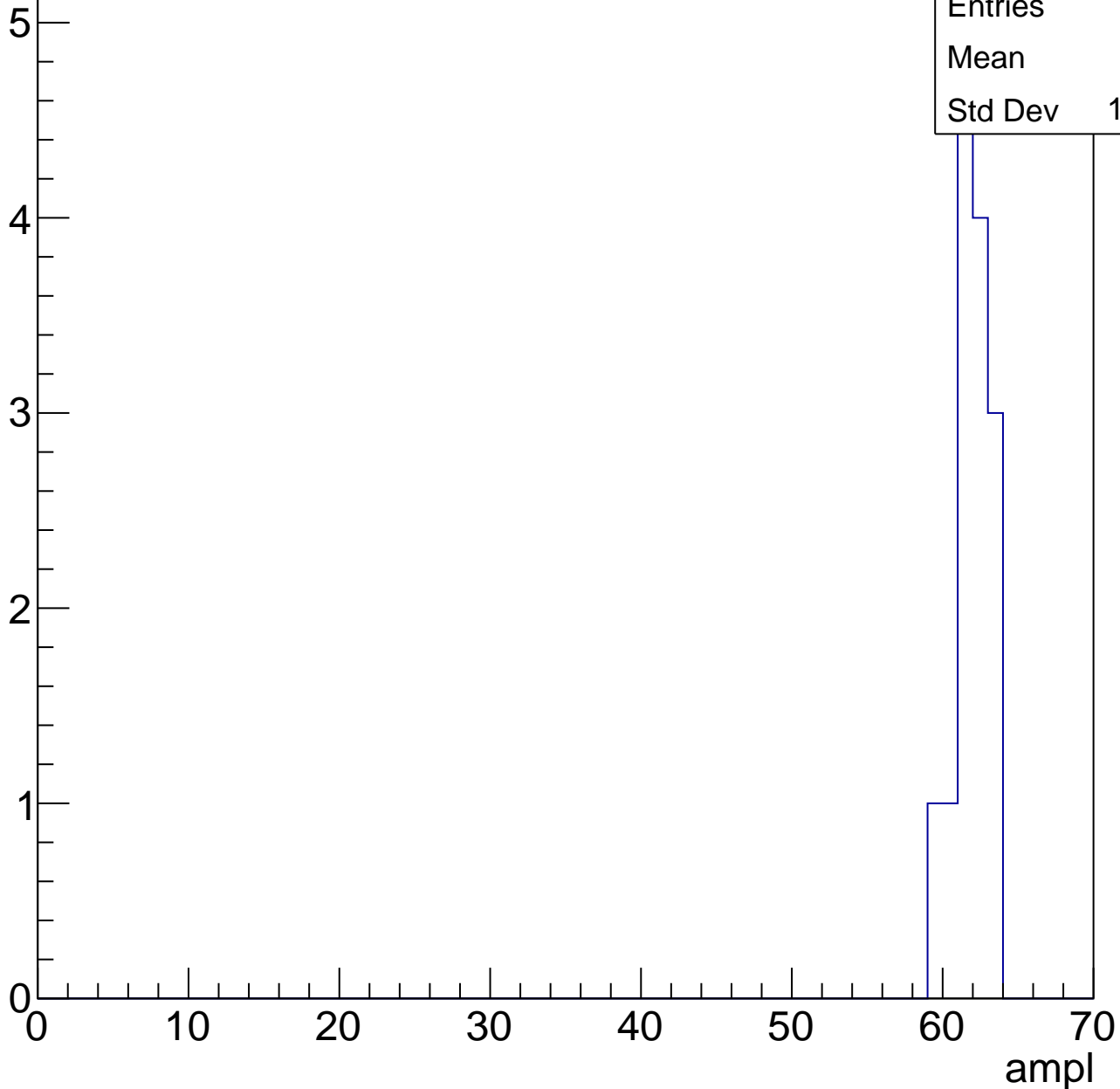


# B1L003S, U26-ch20, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	14
Mean	61.5
Std Dev	1.118





# B1L003S, U26-ch20, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L003S, U26-ch21, adc0

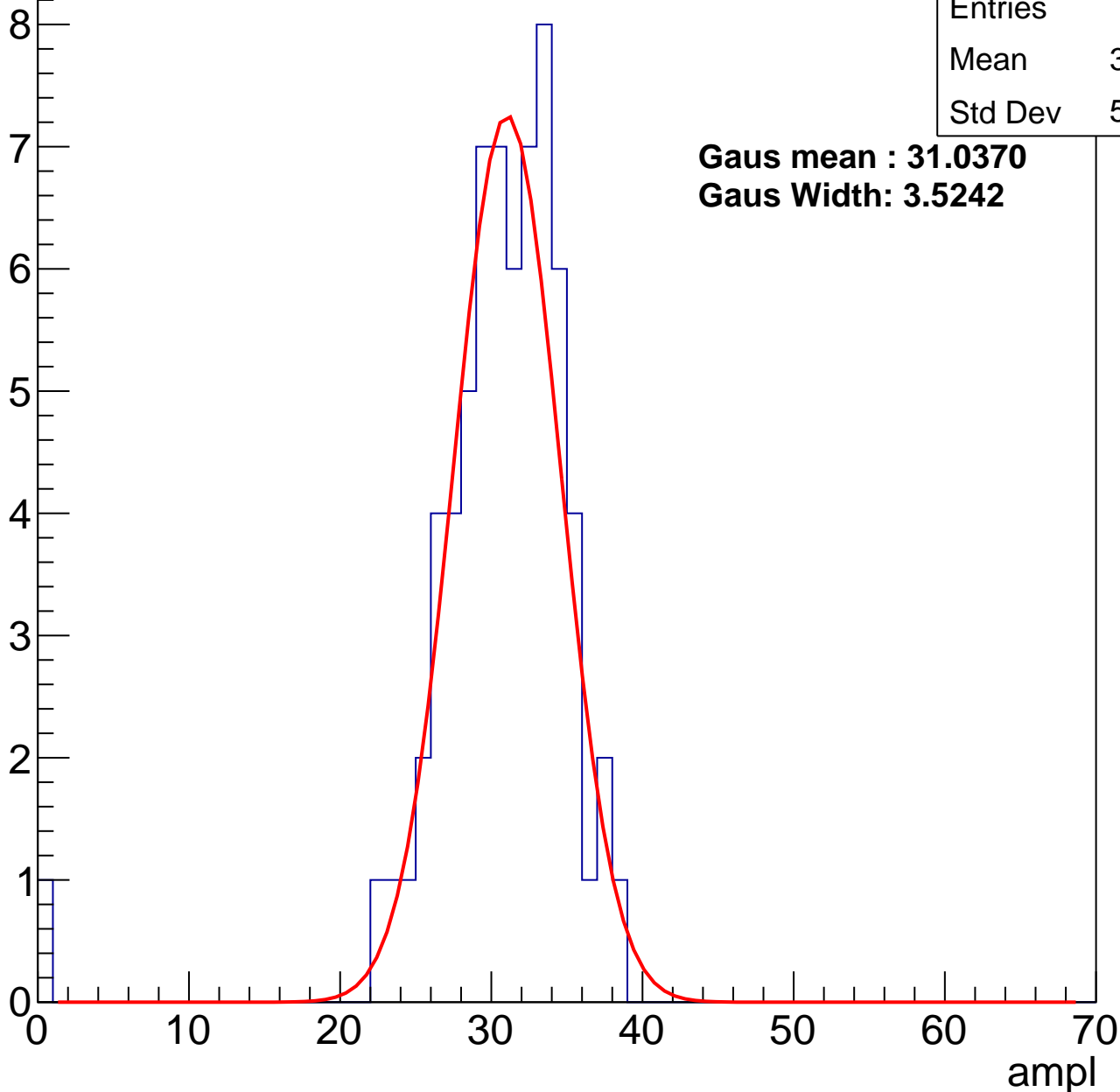
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	30.15
Std Dev	5.036

**Gaus mean : 31.0370**

**Gaus Width: 3.5242**



# B1L003S, U26-ch21, adc1

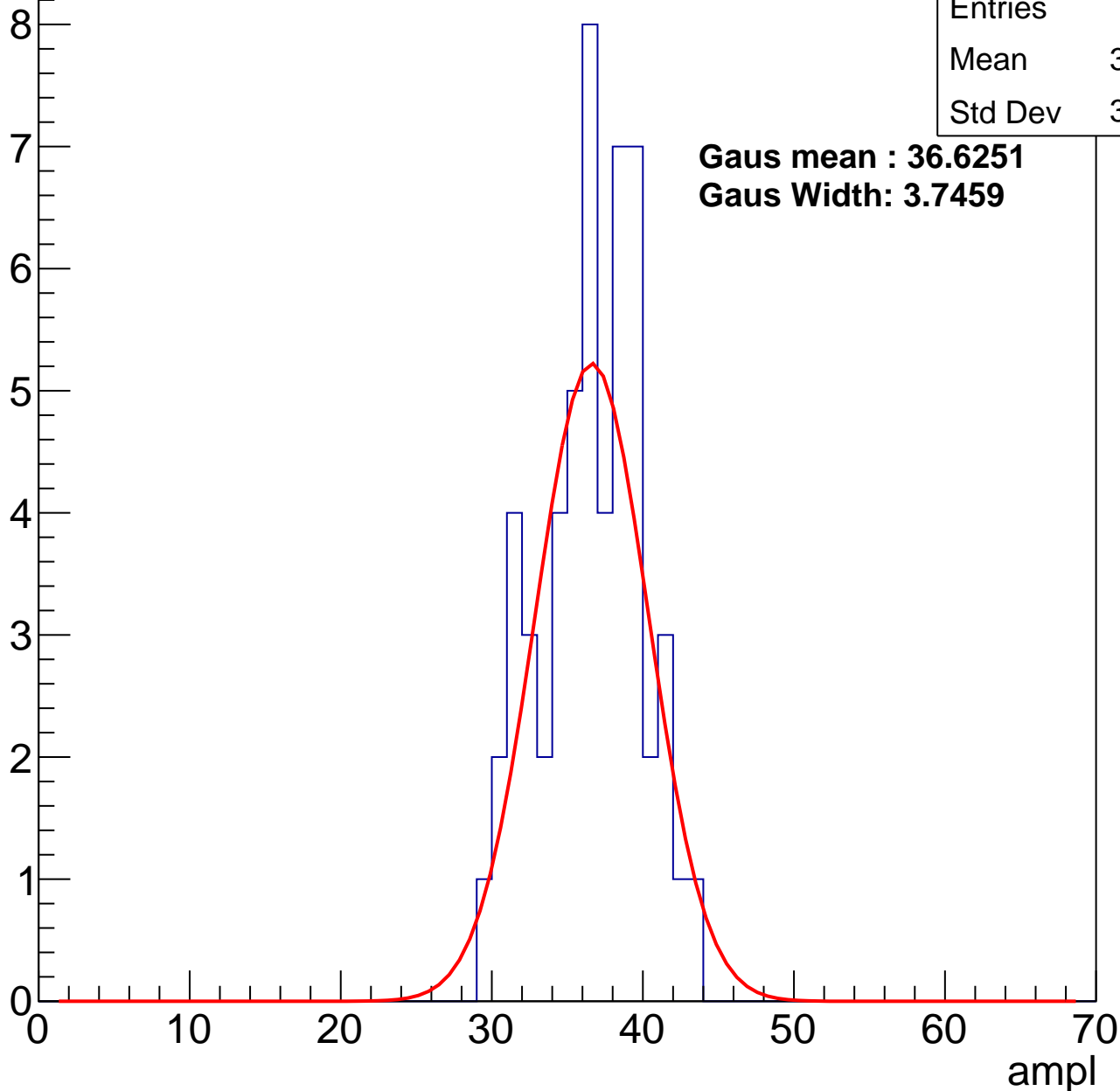
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	54
Mean	36.09
Std Dev	3.318

**Gaus mean : 36.6251**

**Gaus Width: 3.7459**



# B1L003S, U26-ch21, adc2

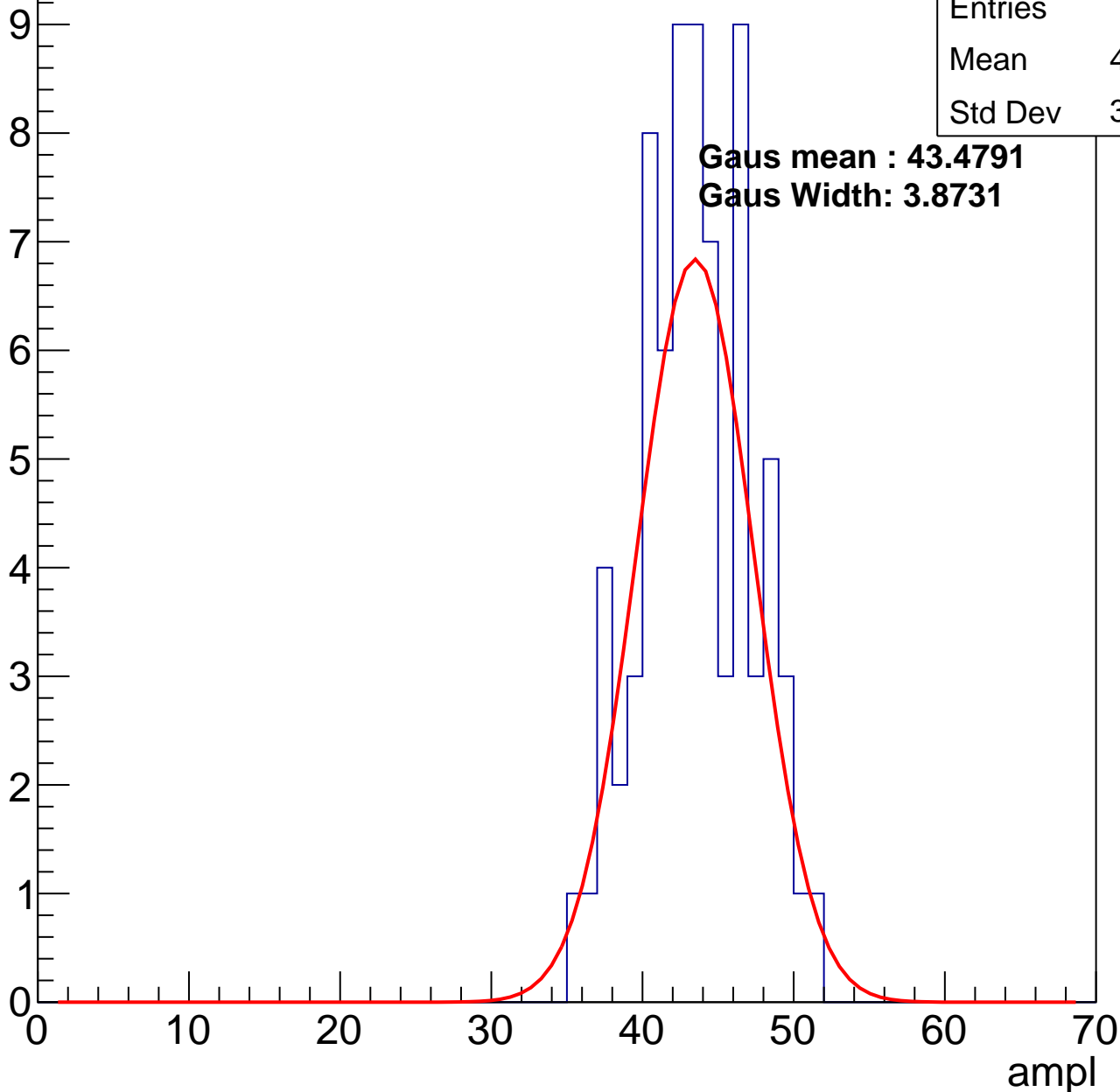
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	75
Mean	43.05
Std Dev	3.566

**Gaus mean : 43.4791**

**Gaus Width: 3.8731**

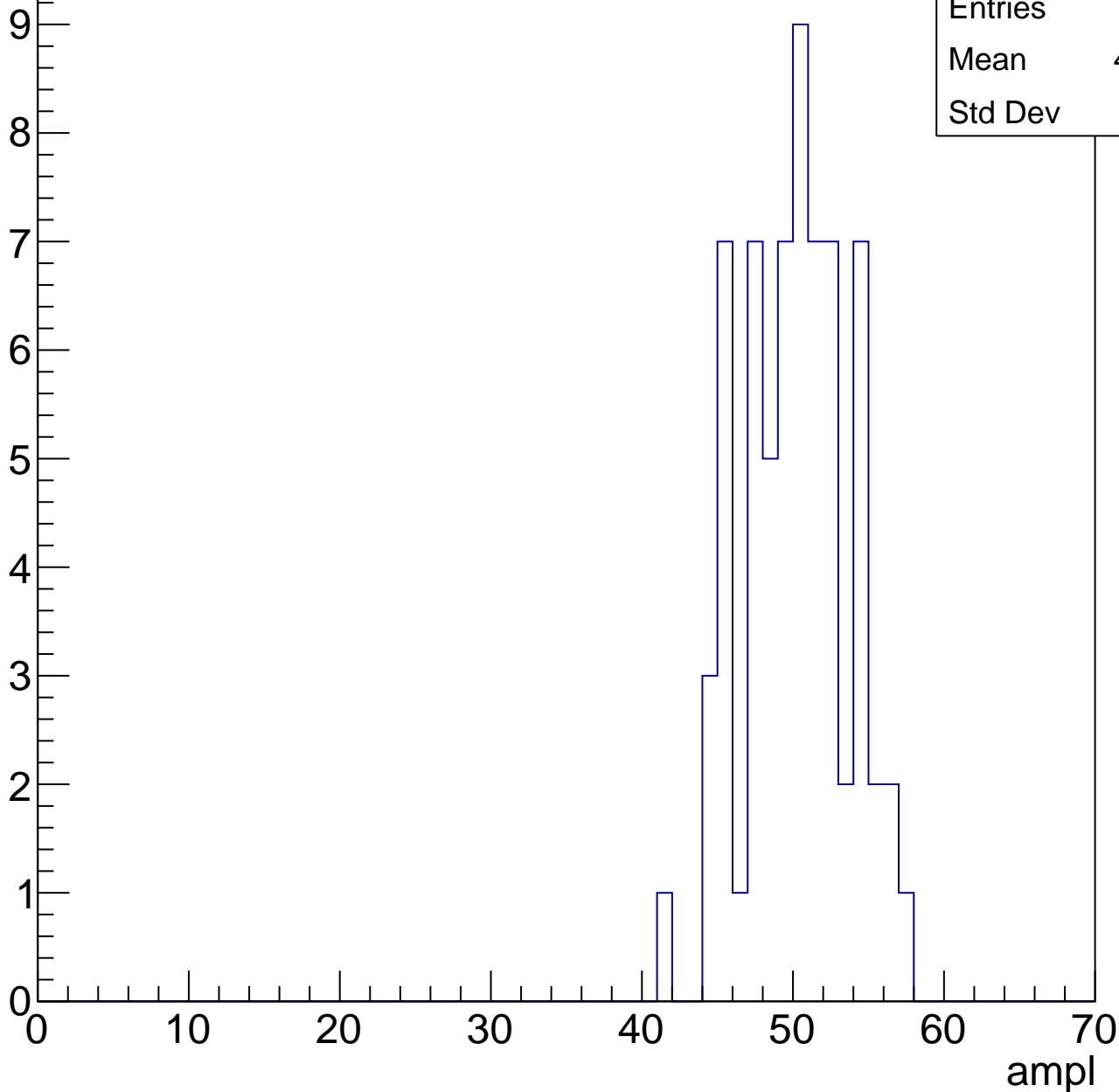


# B1L003S, U26-ch21, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	49.71
Std Dev	3.43

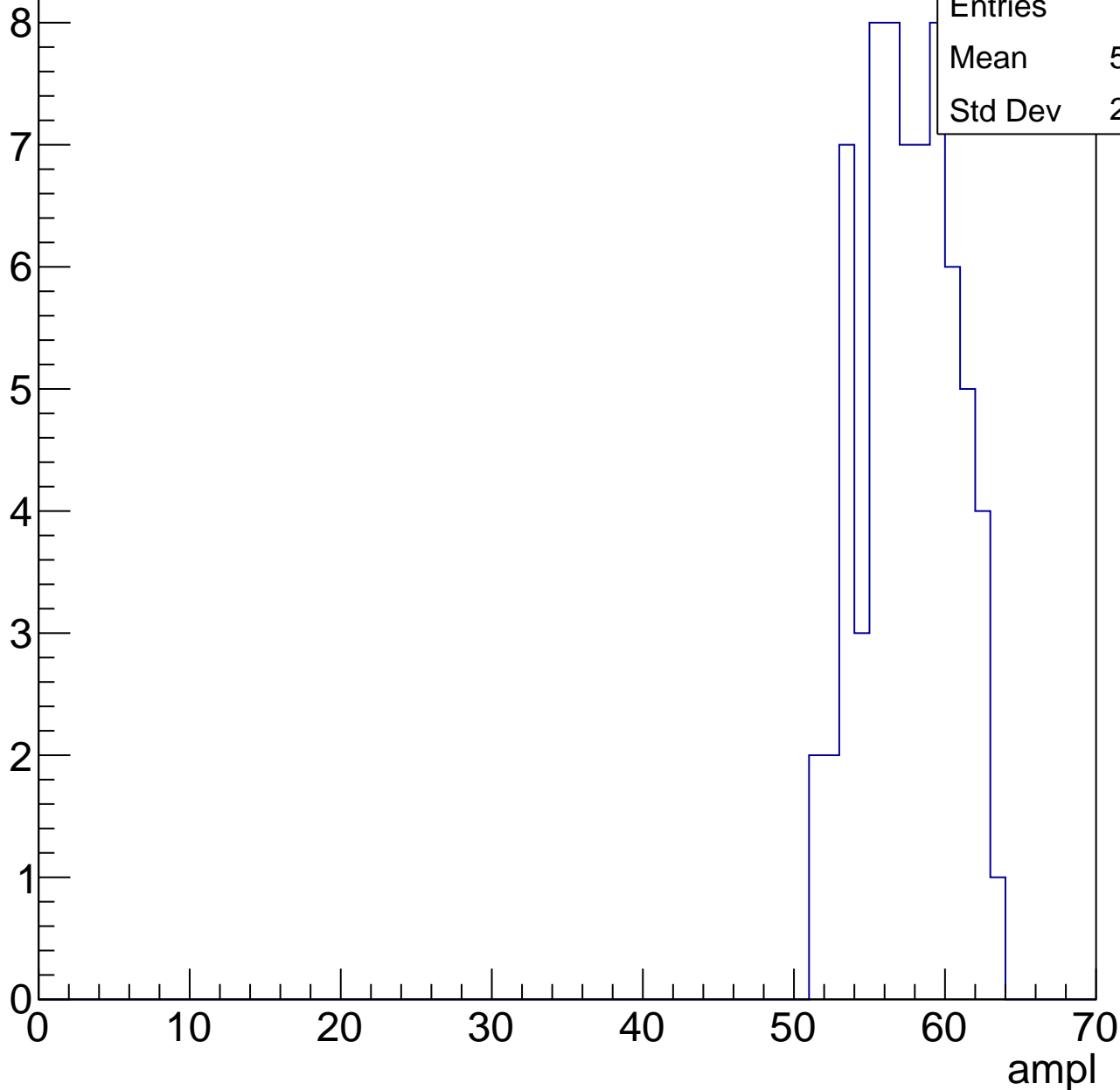


# B1L003S, U26-ch21, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	57.06
Std Dev	2.995

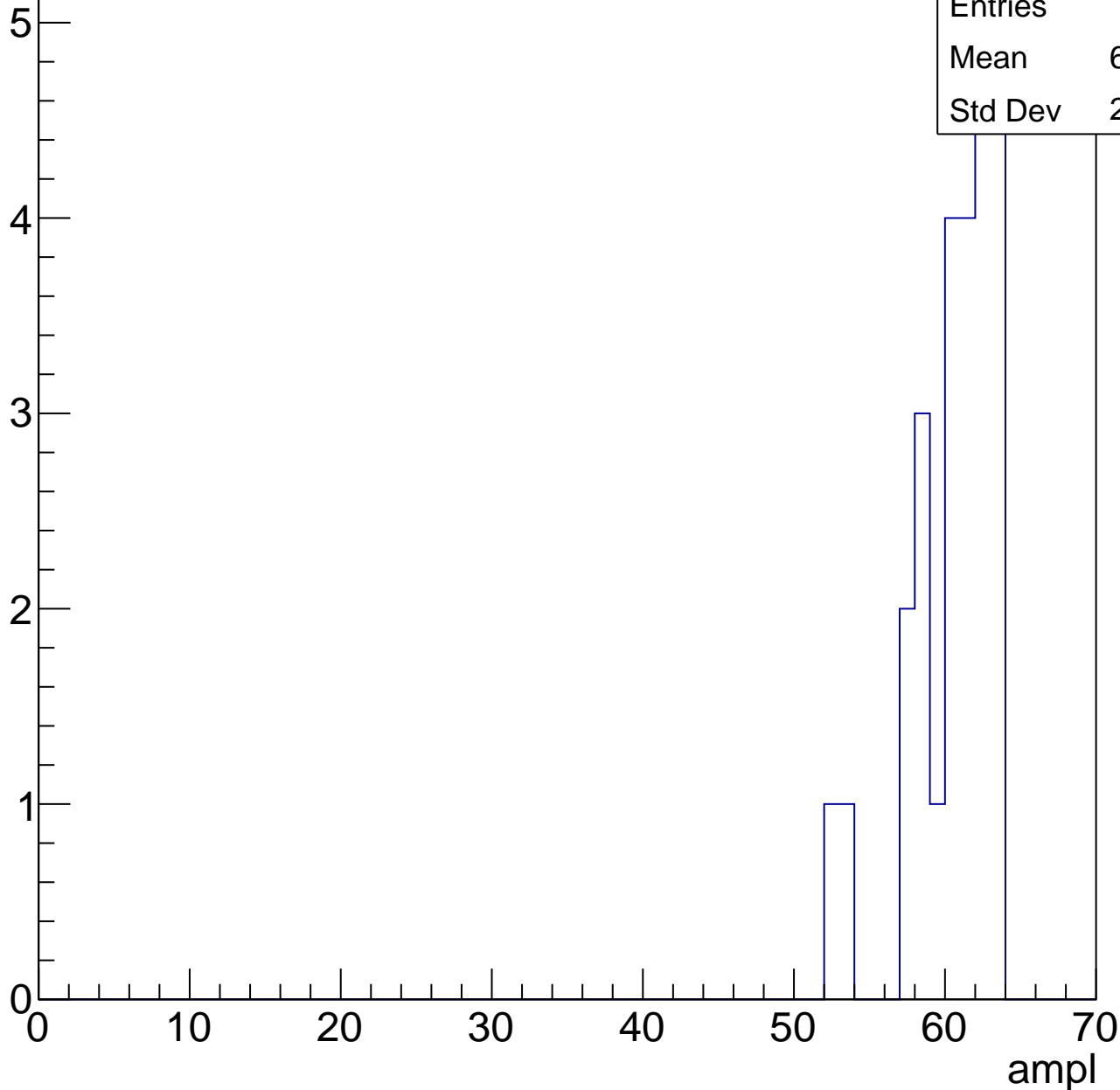


# B1L003S, U26-ch21, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

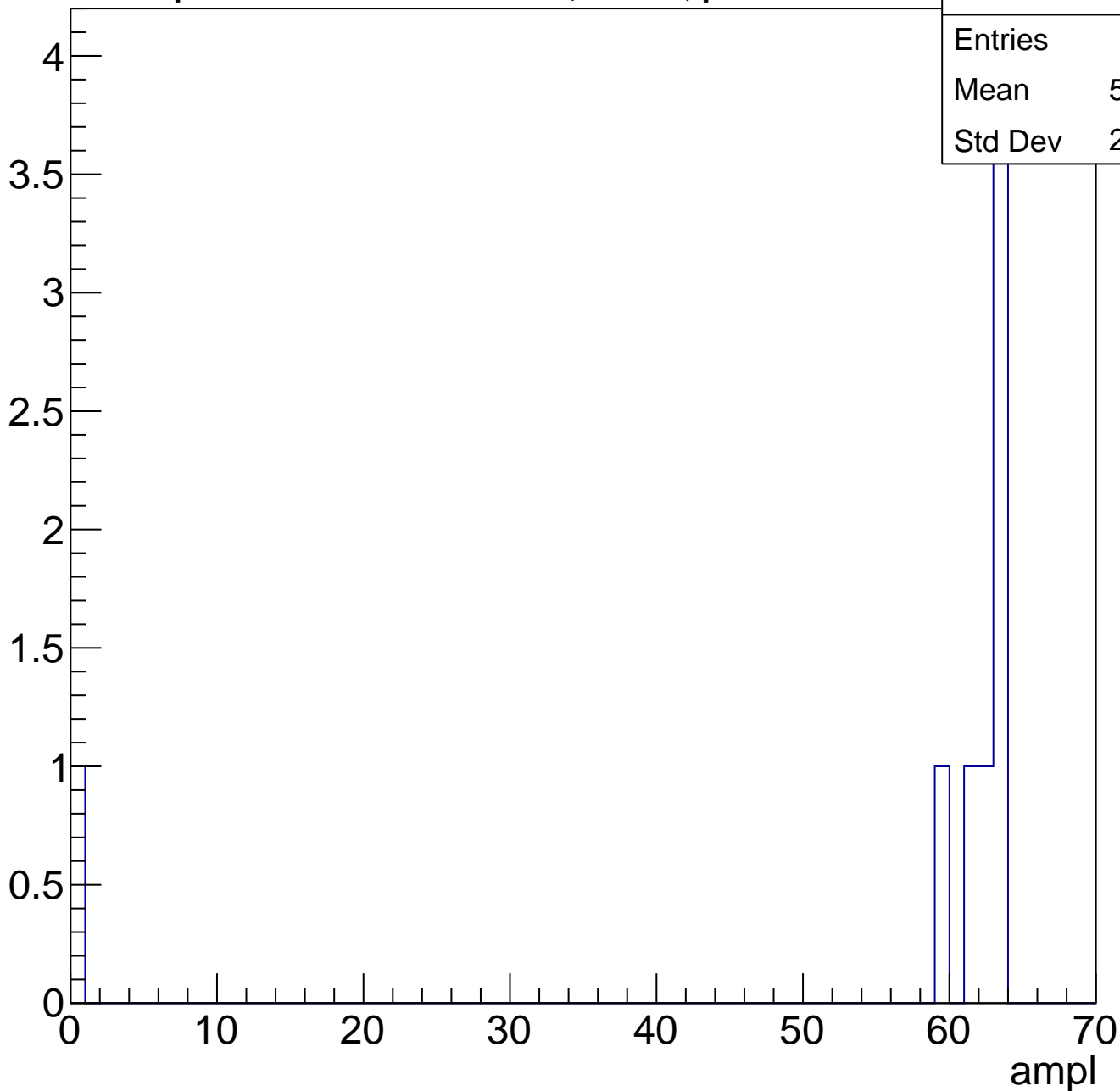
Entries	26
Mean	60.04
Std Dev	2.862



# B1L003S, U26-ch21, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch21, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L003S, U26-ch22, adc0

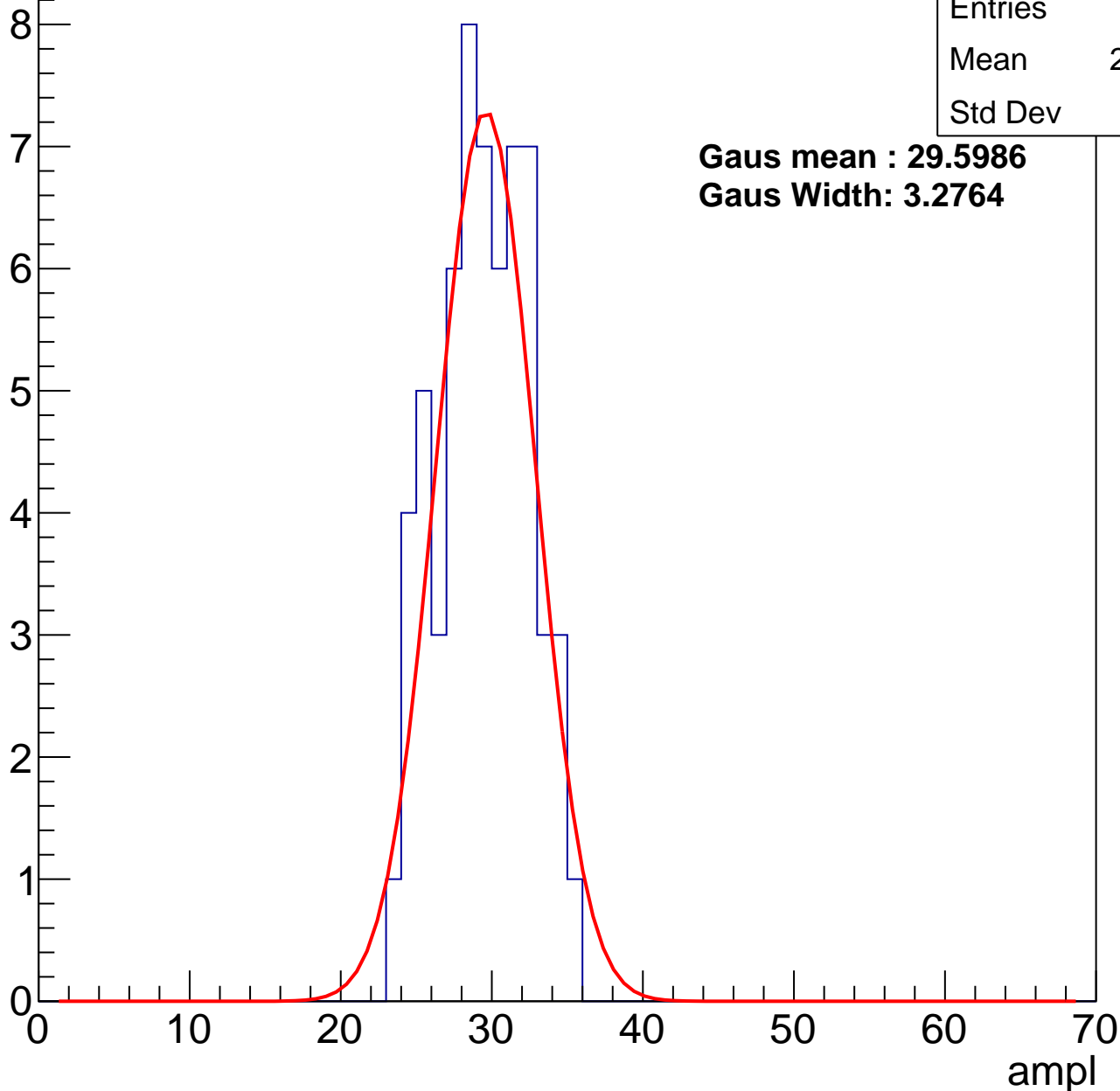
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	28.98
Std Dev	2.95

**Gaus mean : 29.5986**

**Gaus Width: 3.2764**



# B1L003S, U26-ch22, adc1

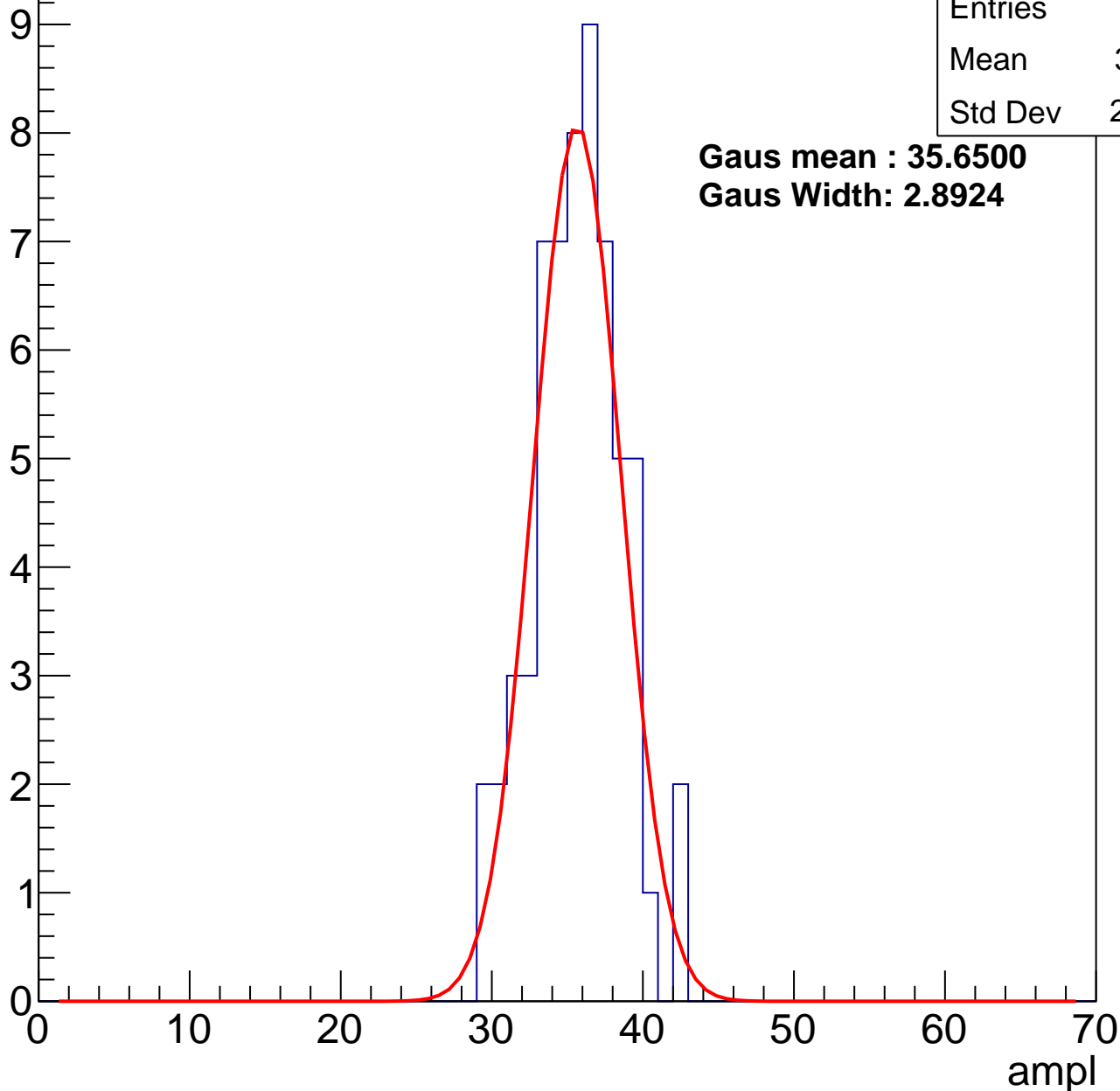
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	35.21
Std Dev	2.903

**Gaus mean : 35.6500**

**Gaus Width: 2.8924**



# B1L003S, U26-ch22, adc2

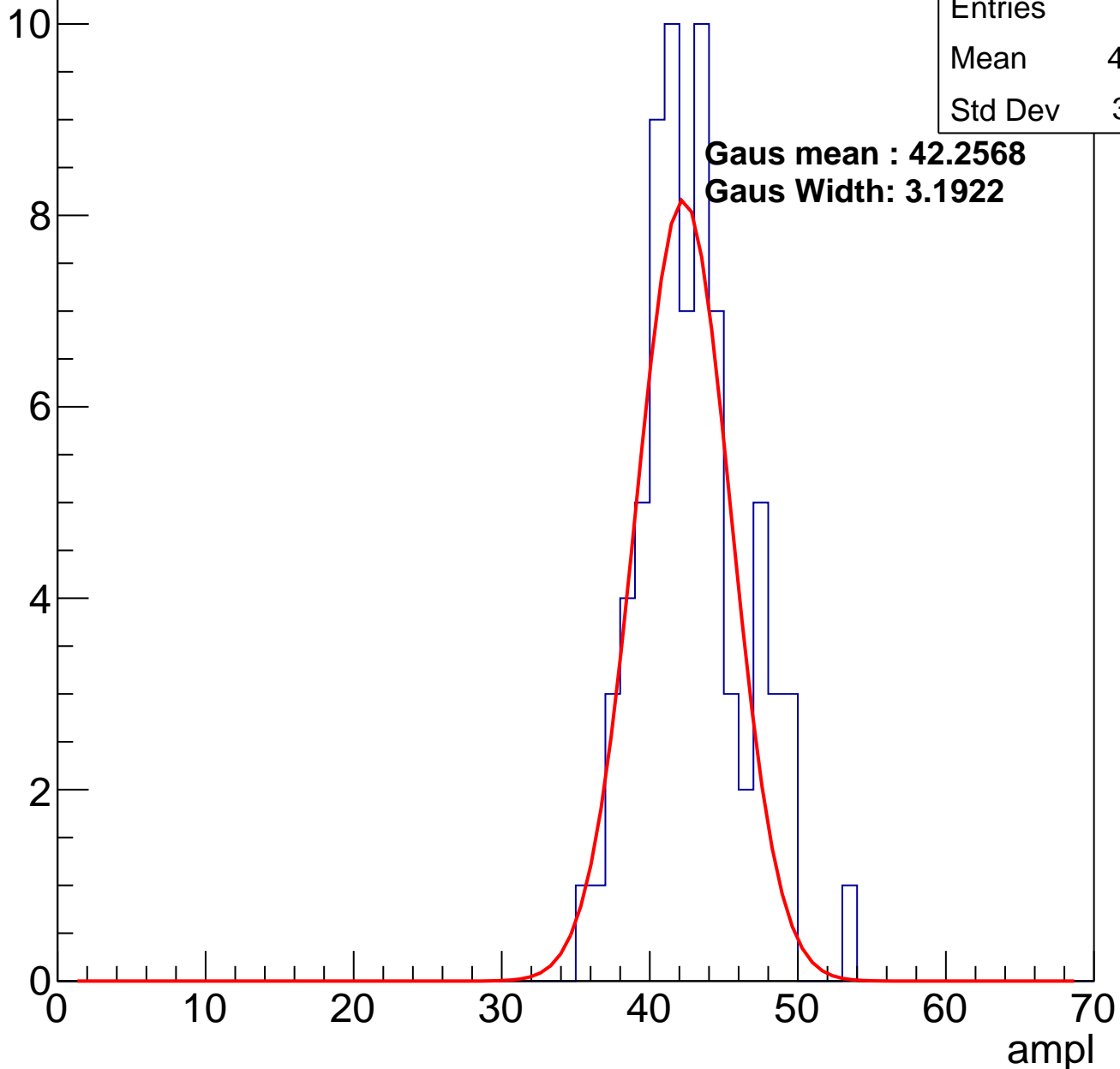
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	74
Mean	42.39
Std Dev	3.491

**Gaus mean : 42.2568**

**Gaus Width: 3.1922**

Entry

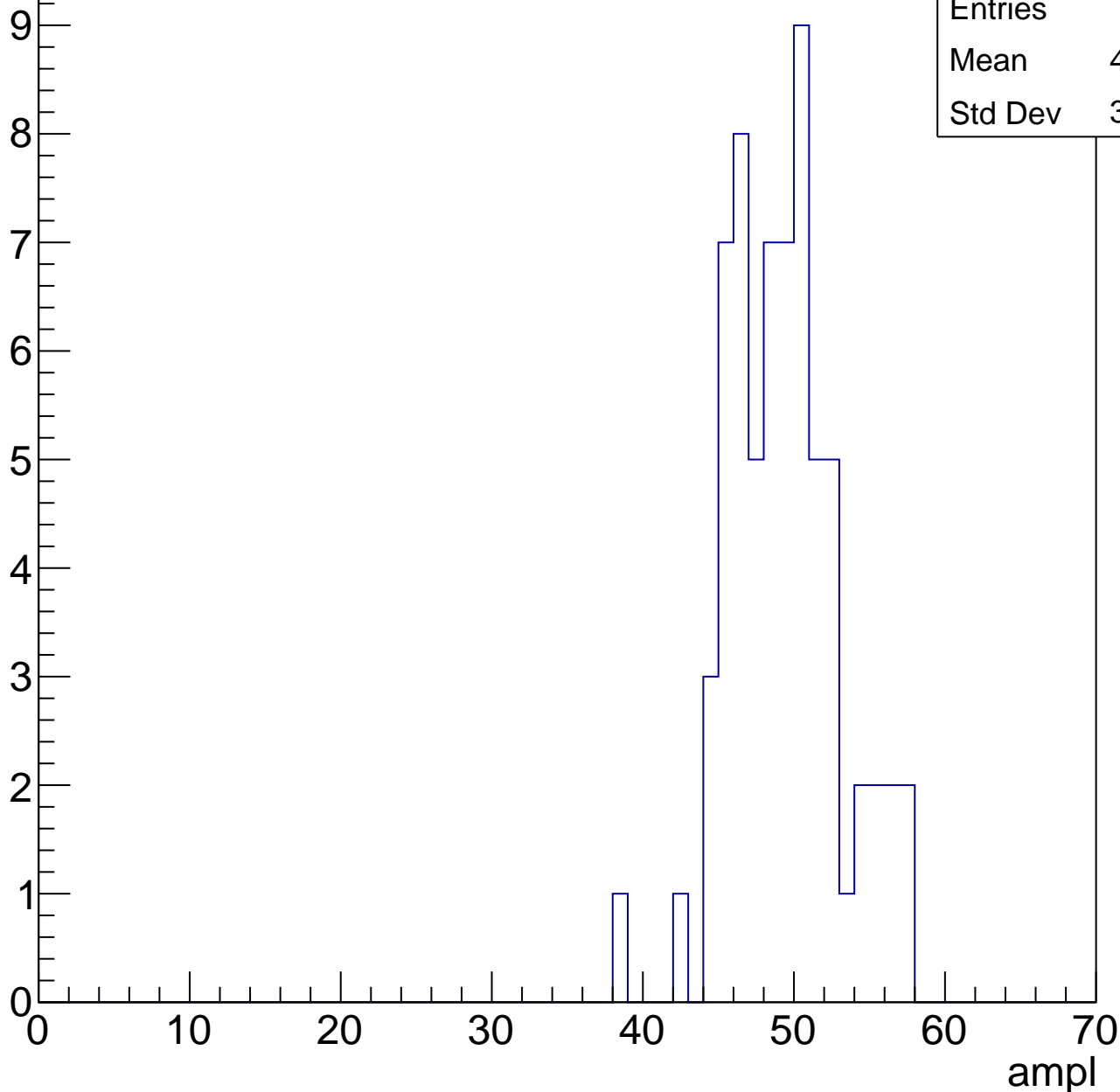


# B1L003S, U26-ch22, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	48.82
Std Dev	3.648



# B1L003S, U26-ch22, adc4

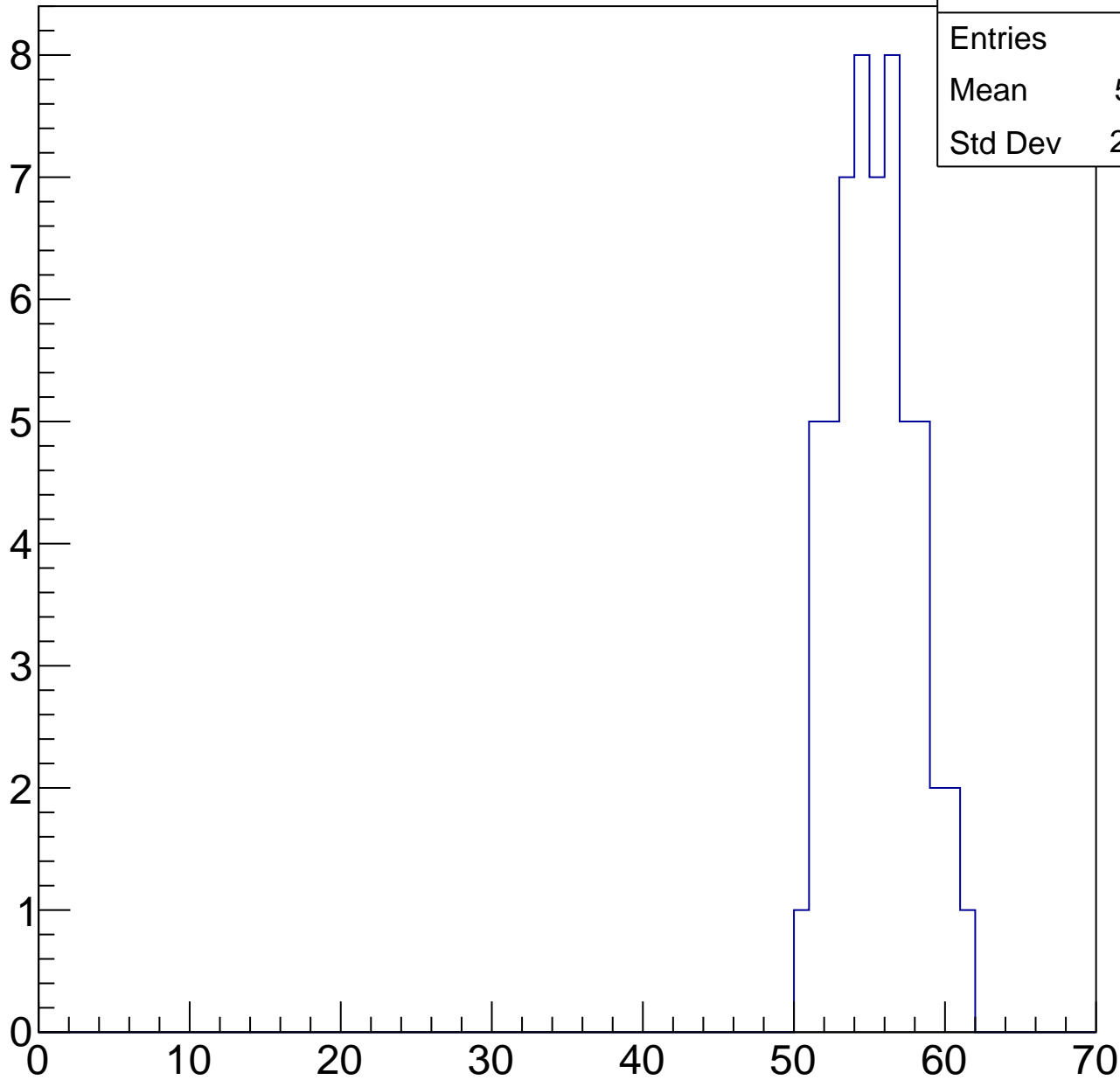
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	56
Mean	54.91
Std Dev	2.593

ampl

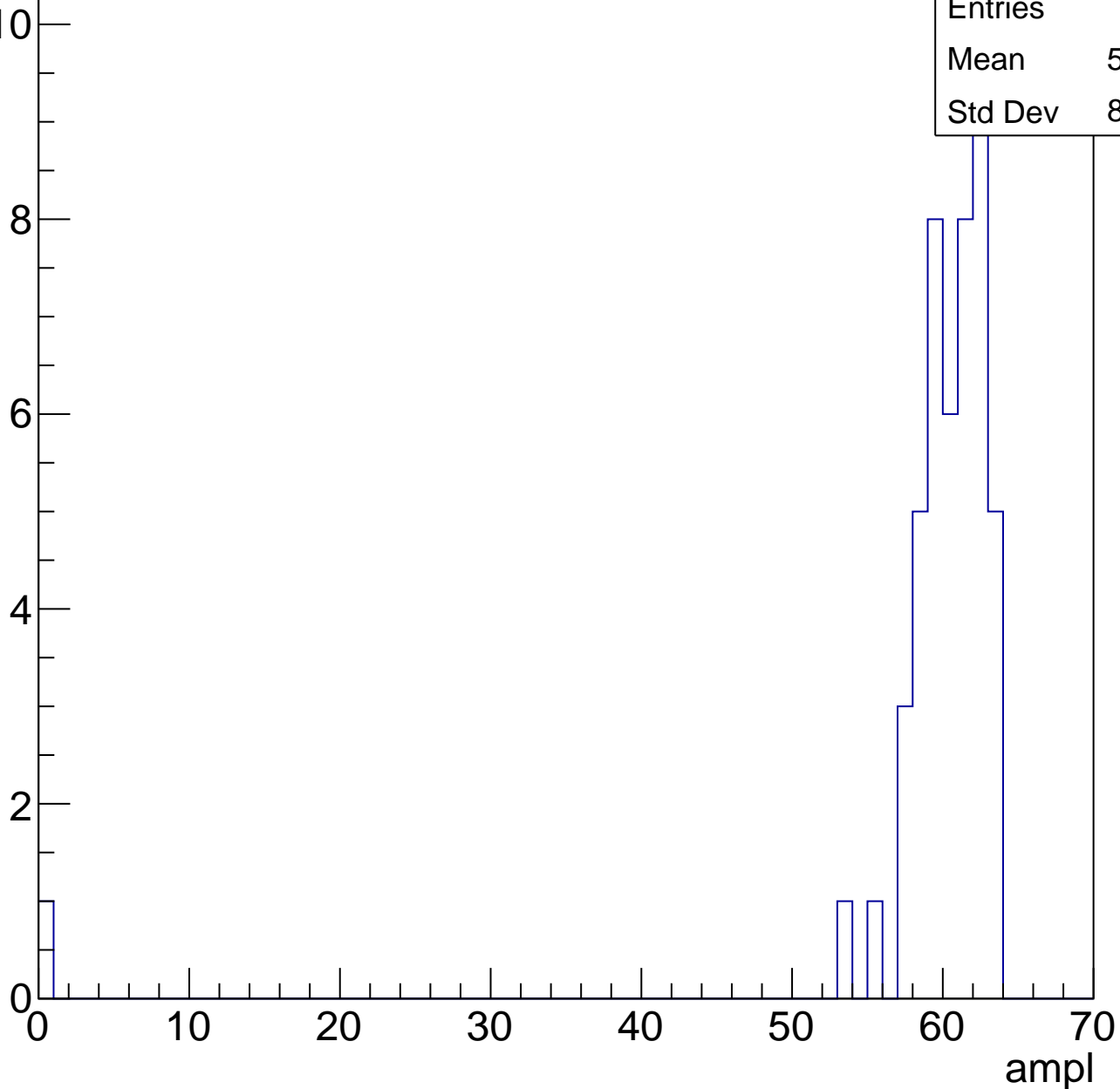


# B1L003S, U26-ch22, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	48
Mean	58.83
Std Dev	8.847

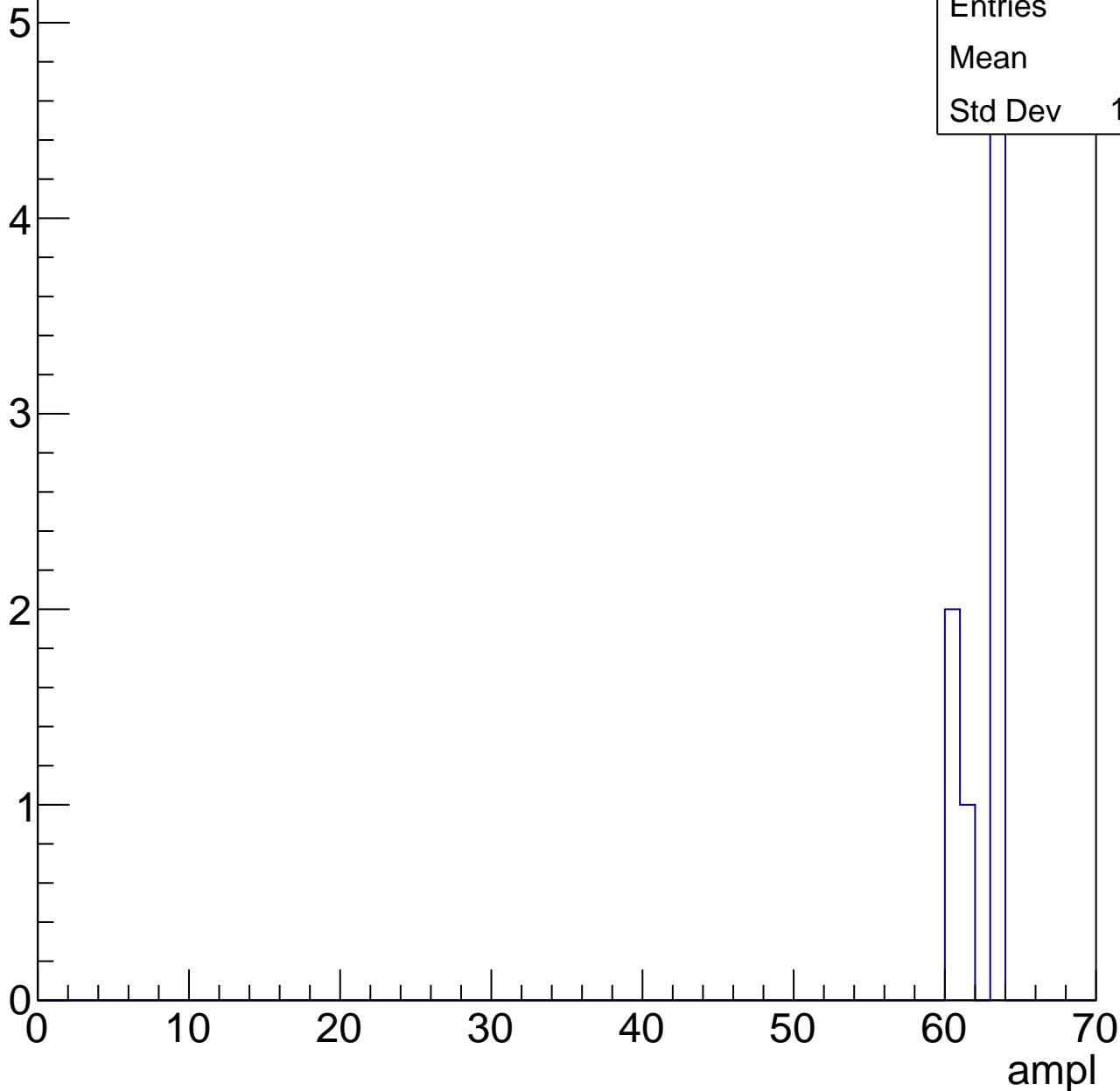


# B1L003S, U26-ch22, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	8
Mean	62
Std Dev	1.323





# B1L003S, U26-ch22, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U26-ch23, adc0

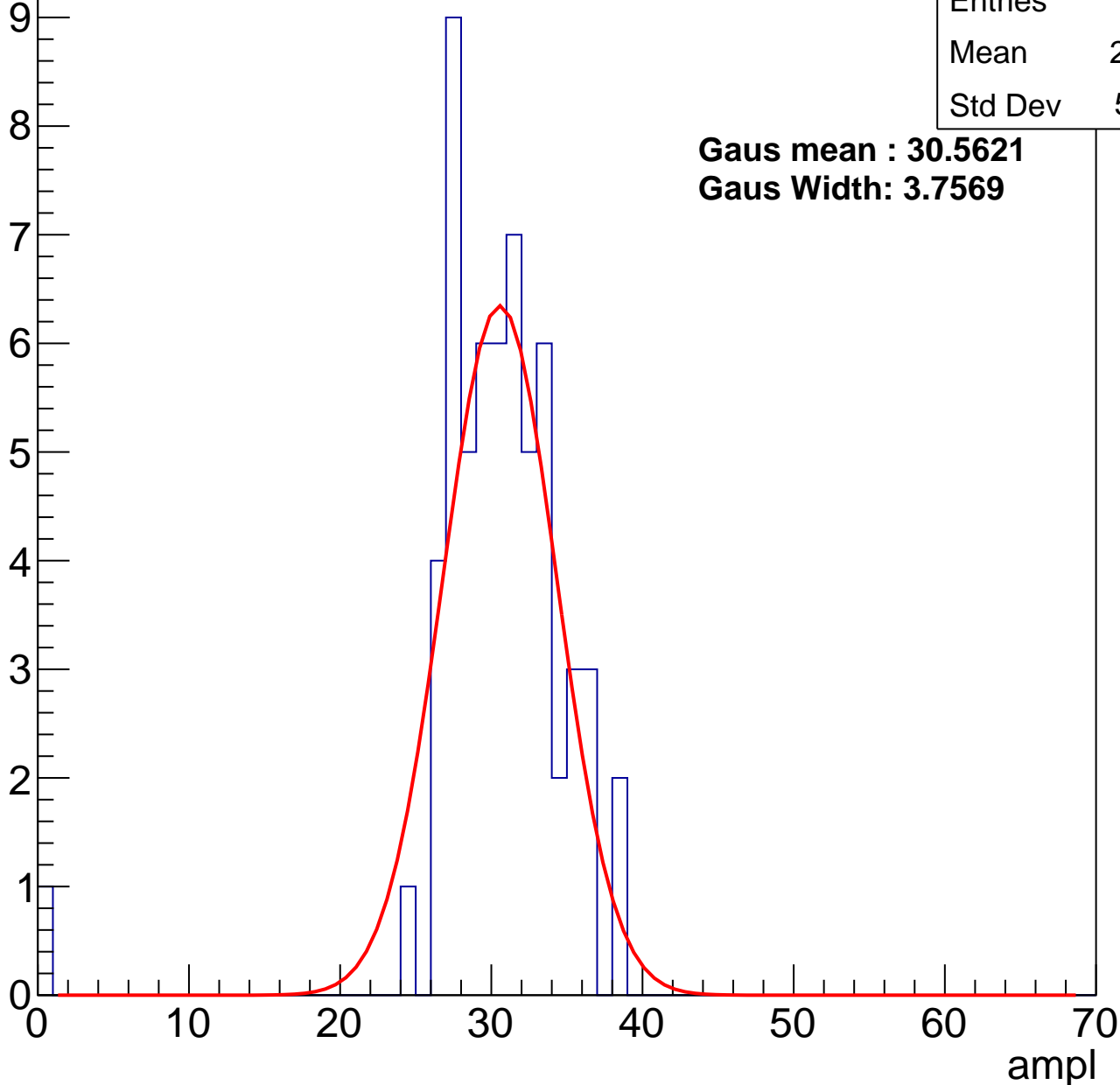
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	29.95
Std Dev	5.051

**Gaus mean : 30.5621**

**Gaus Width: 3.7569**



# B1L003S, U26-ch23, adc1

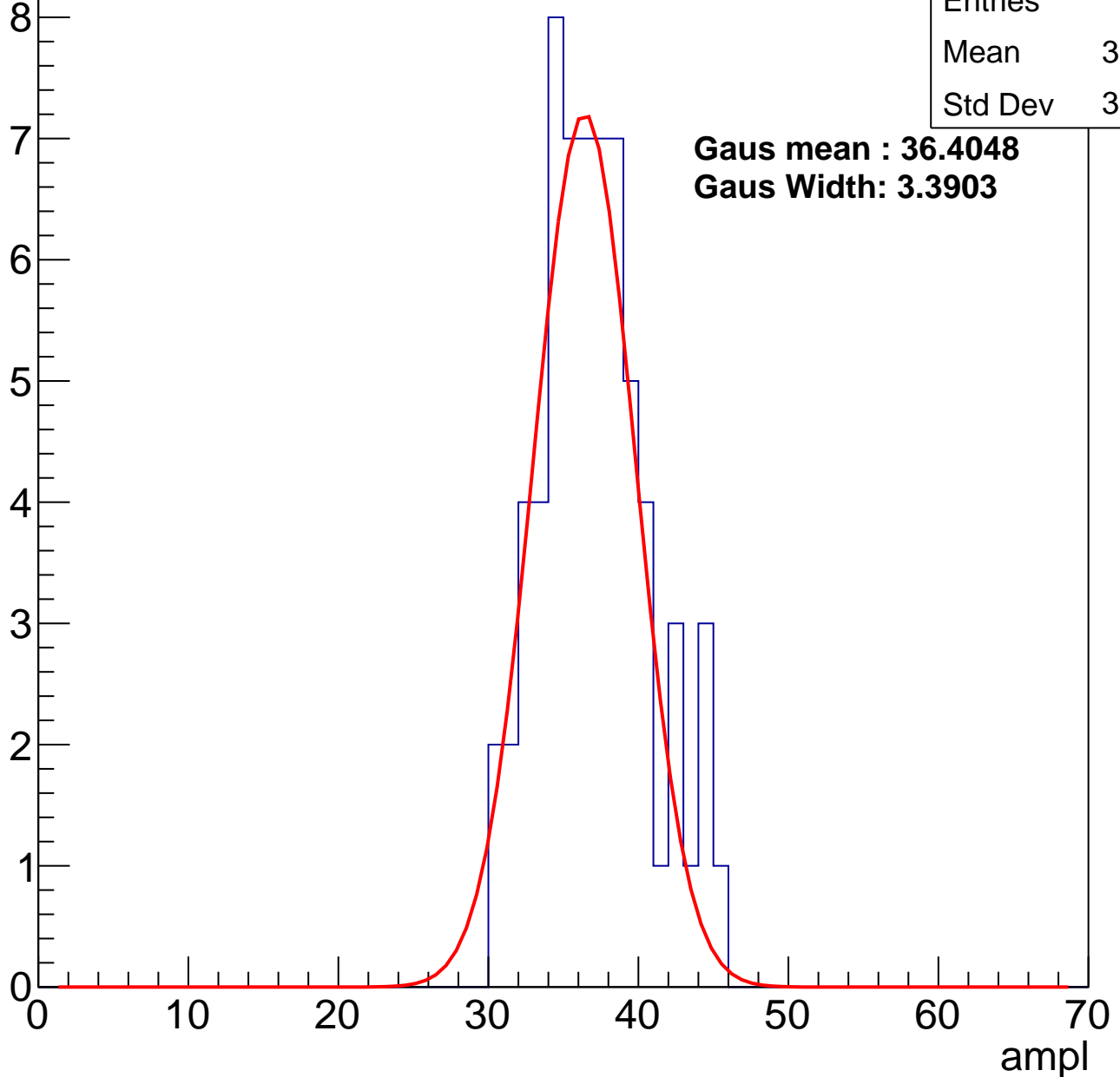
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	36.64
Std Dev	3.553

**Gaus mean : 36.4048**

**Gaus Width: 3.3903**



# B1L003S, U26-ch23, adc2

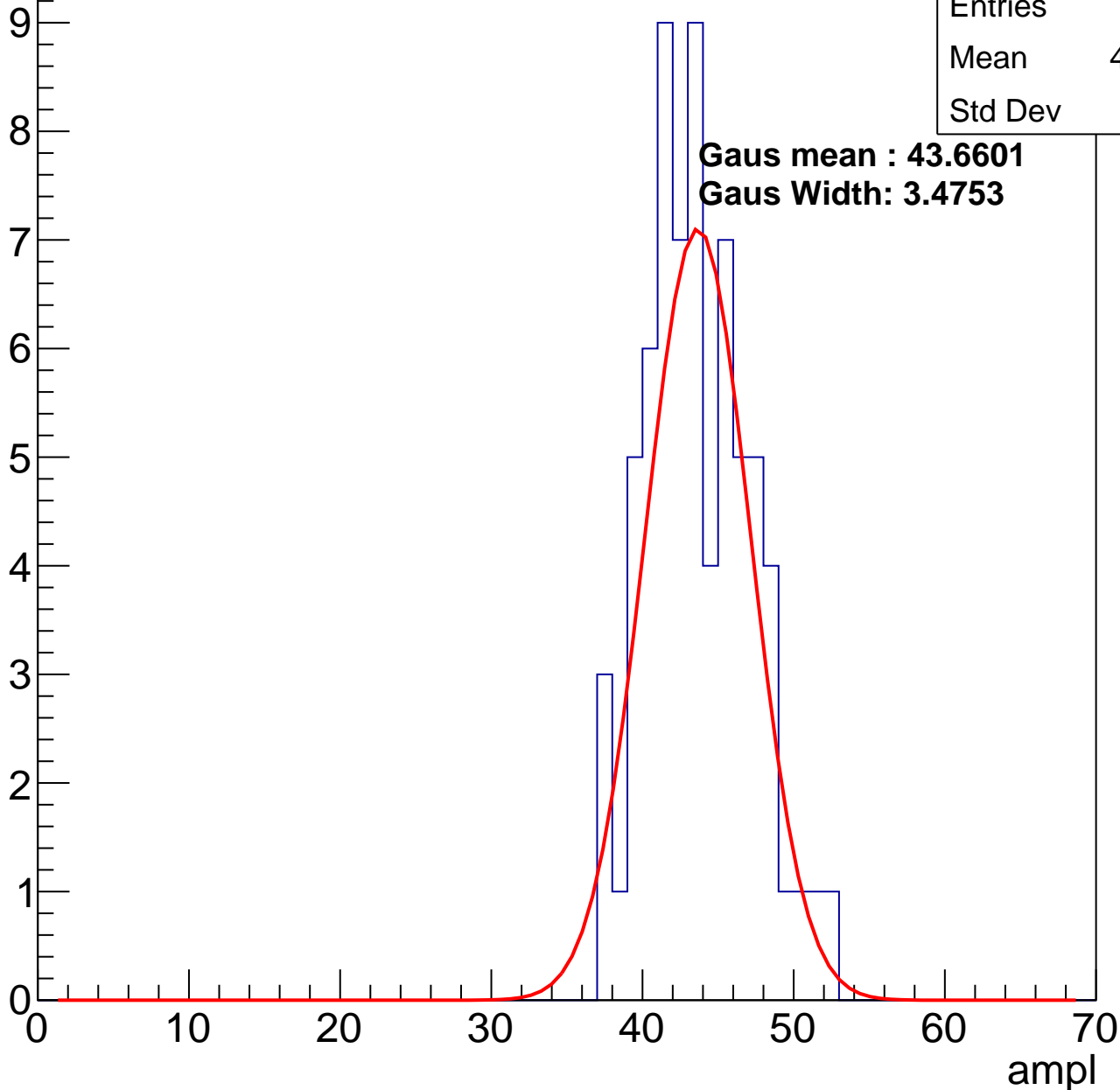
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	43.25
Std Dev	3.39

**Gaus mean : 43.6601**

**Gaus Width: 3.4753**

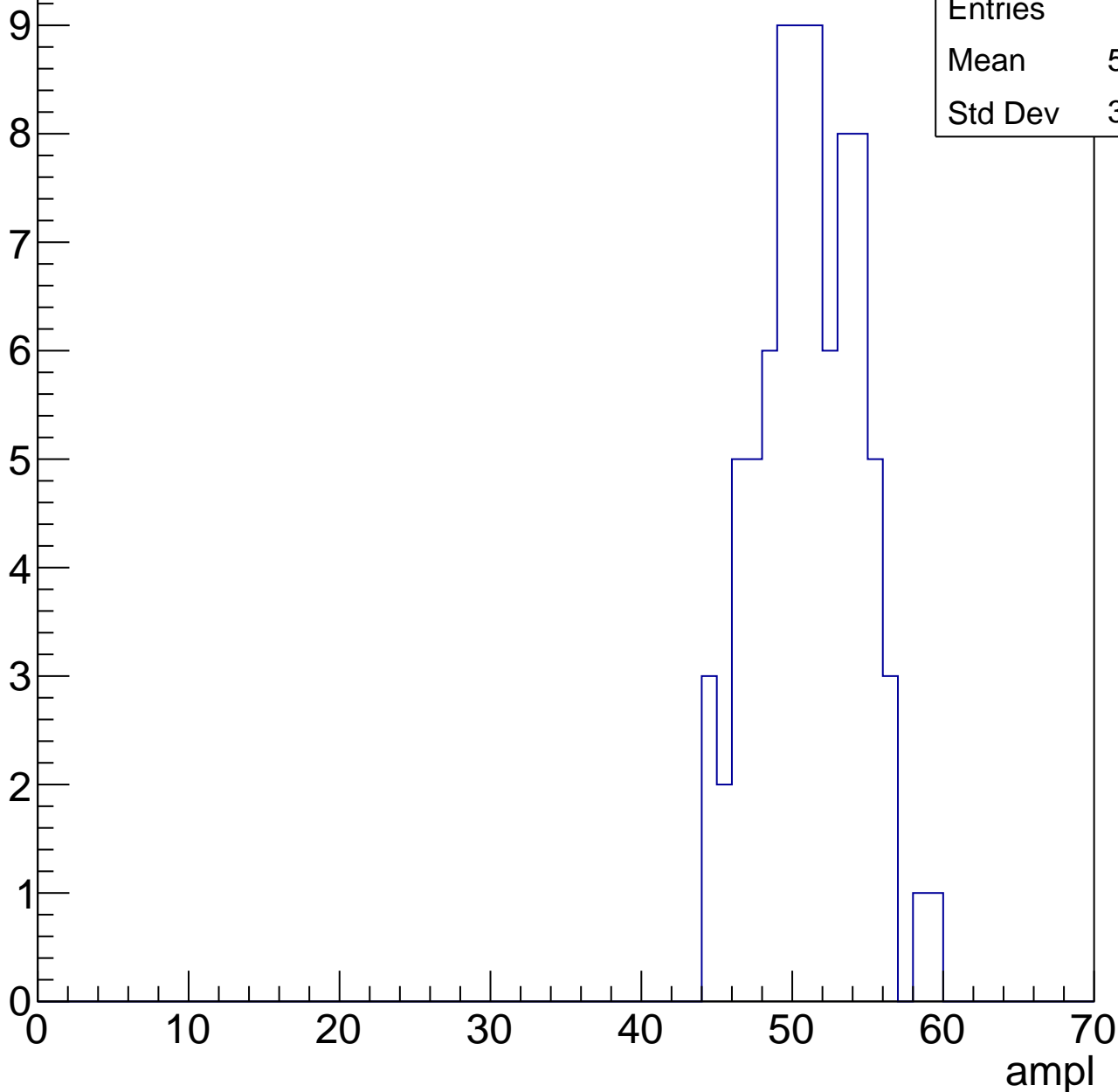


# B1L003S, U26-ch23, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

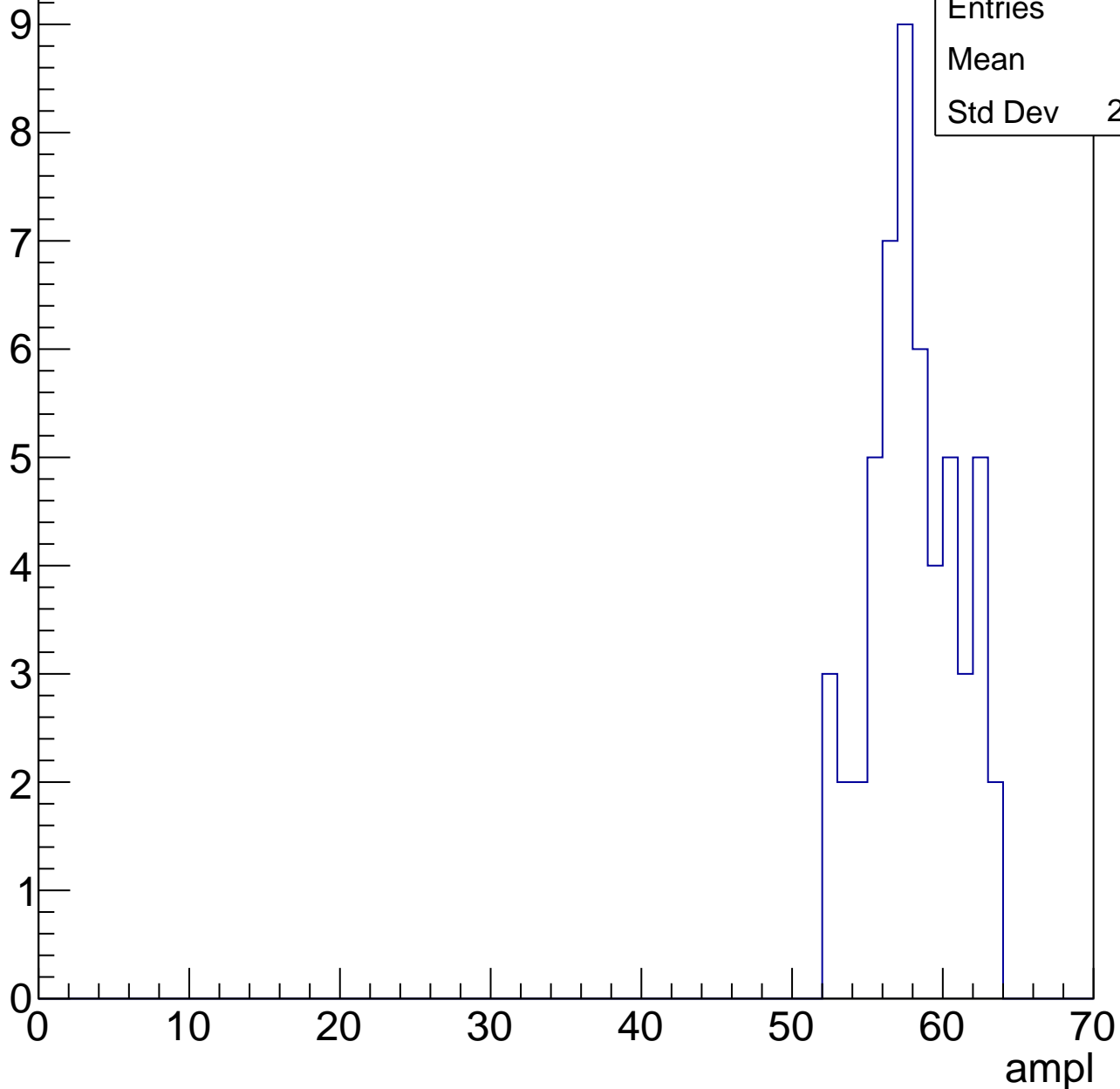
Entries	80
Mean	50.66
Std Dev	3.339



# B1L003S, U26-ch23, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

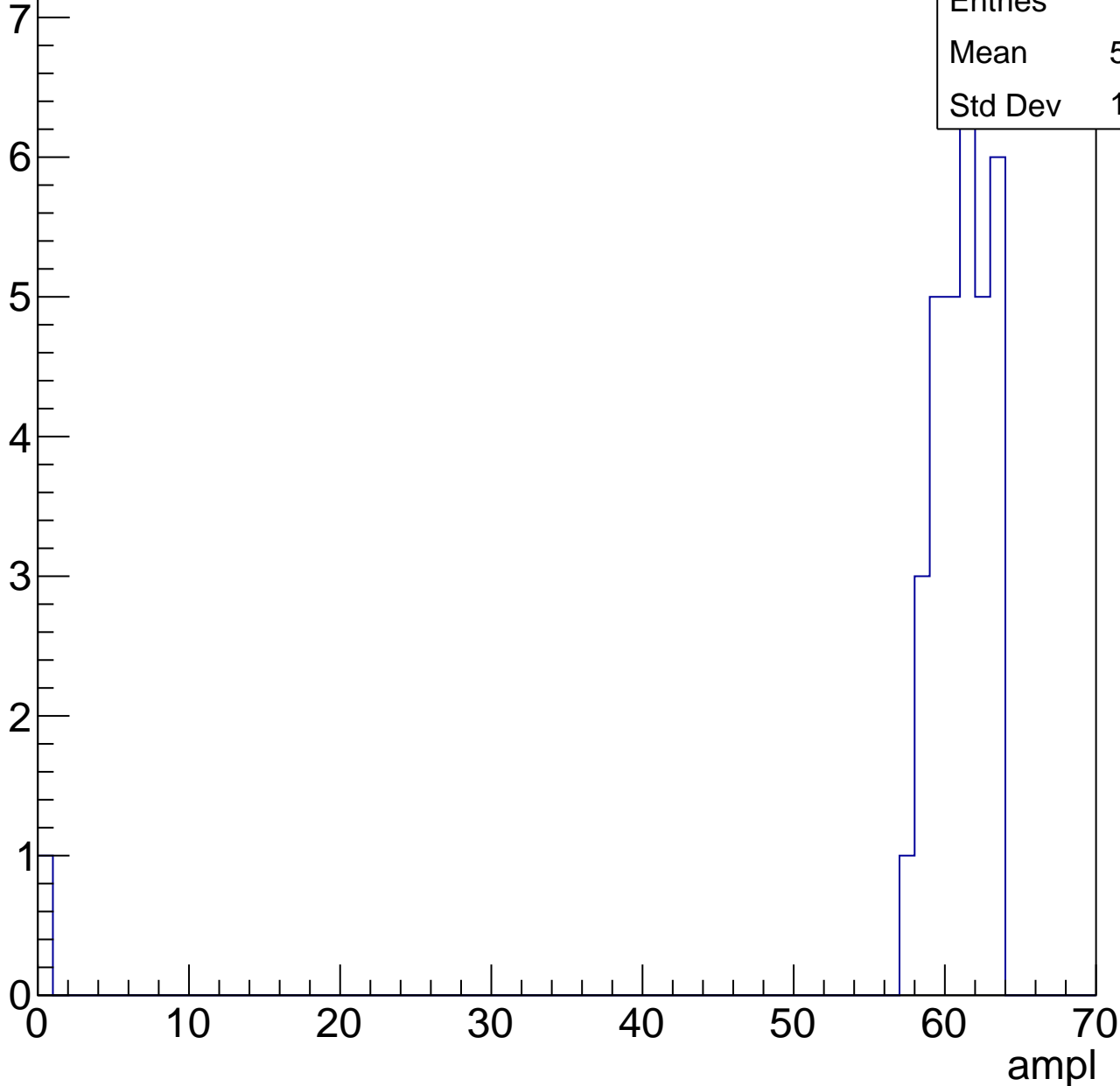


# B1L003S, U26-ch23, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	33
Mean	58.82
Std Dev	10.53



# B1L003S, U26-ch23, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	63
Std Dev	0

0 10 20 30 40 50 60 70

ampl



# B1L003S, U26-ch23, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U26-ch24, adc0

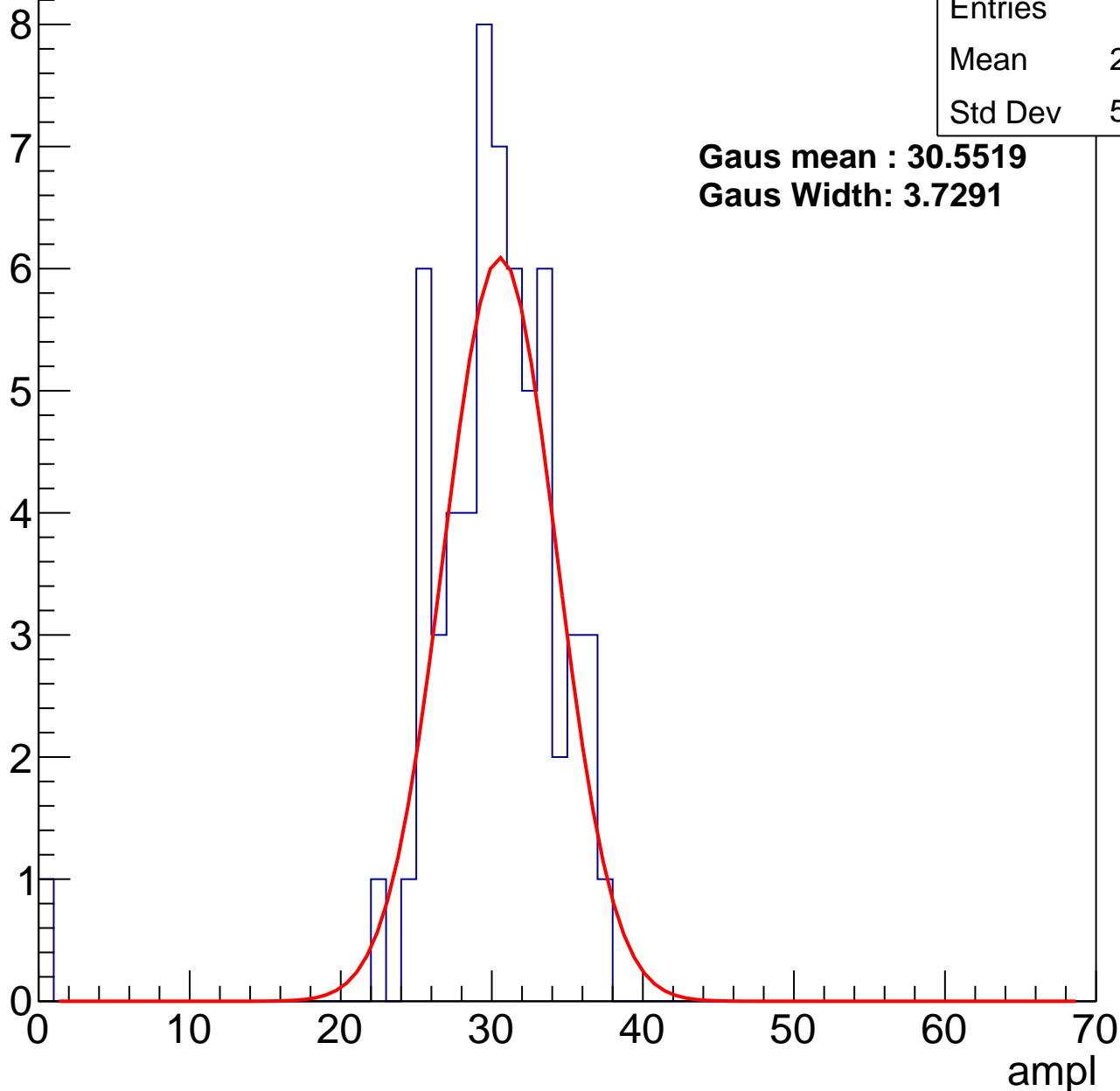
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	29.48
Std Dev	5.098

**Gaus mean : 30.5519**

**Gaus Width: 3.7291**



# B1L003S, U26-ch24, adc1

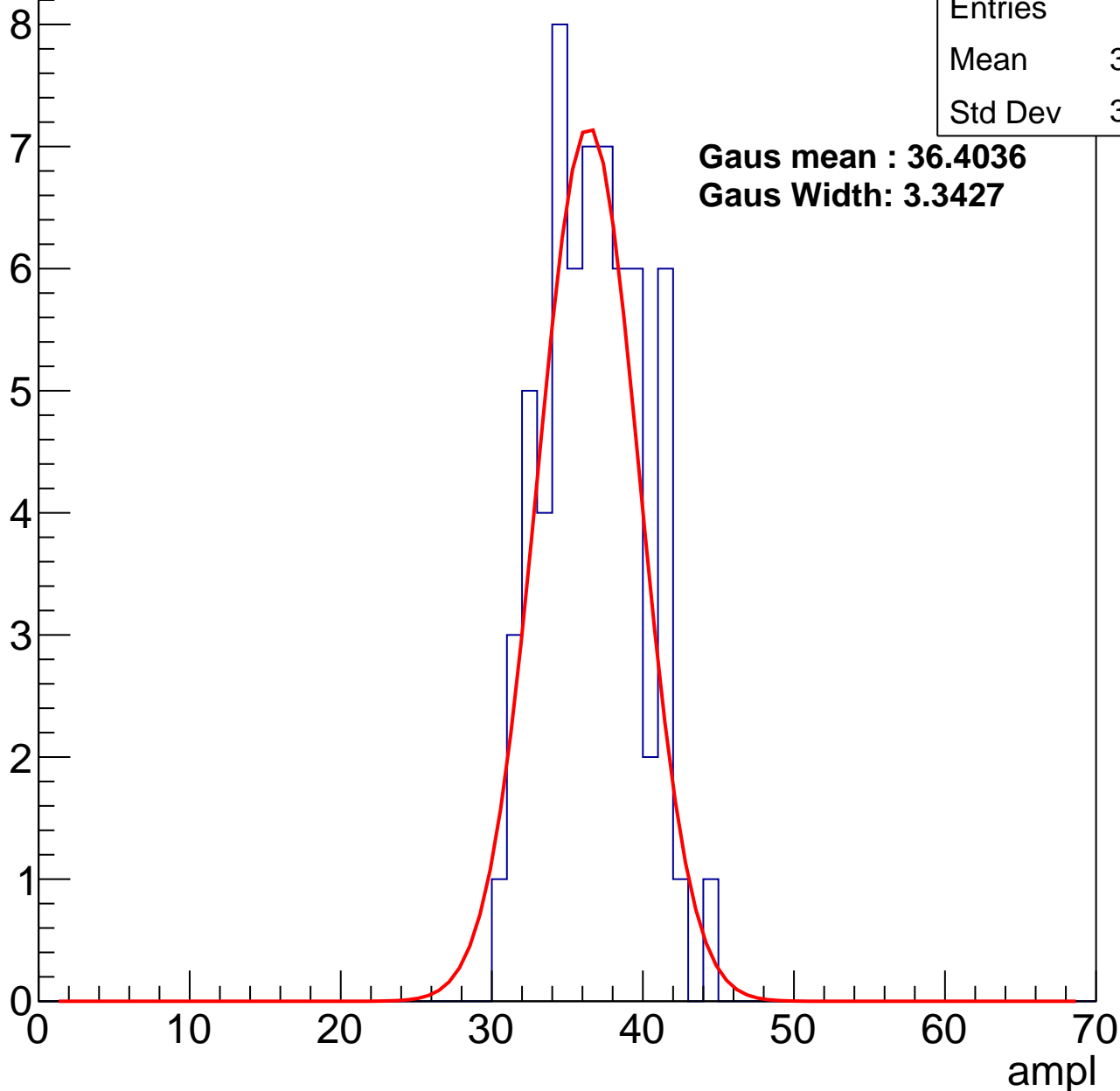
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	36.22
Std Dev	3.159

**Gaus mean : 36.4036**

**Gaus Width: 3.3427**



# B1L003S, U26-ch24, adc2

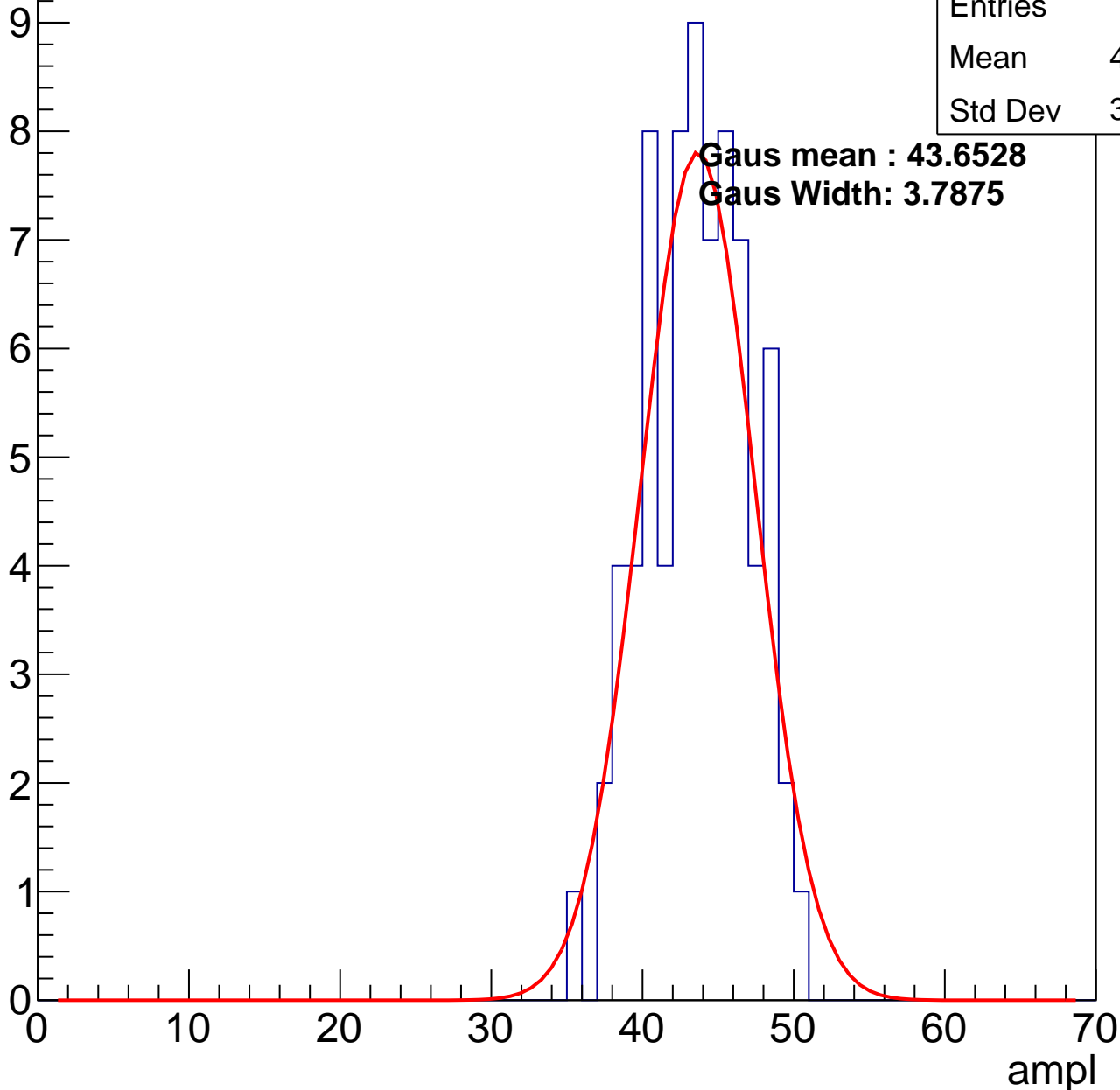
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	75
Mean	43.17
Std Dev	3.328

**Gaus mean : 43.6528**

**Gaus Width: 3.7875**

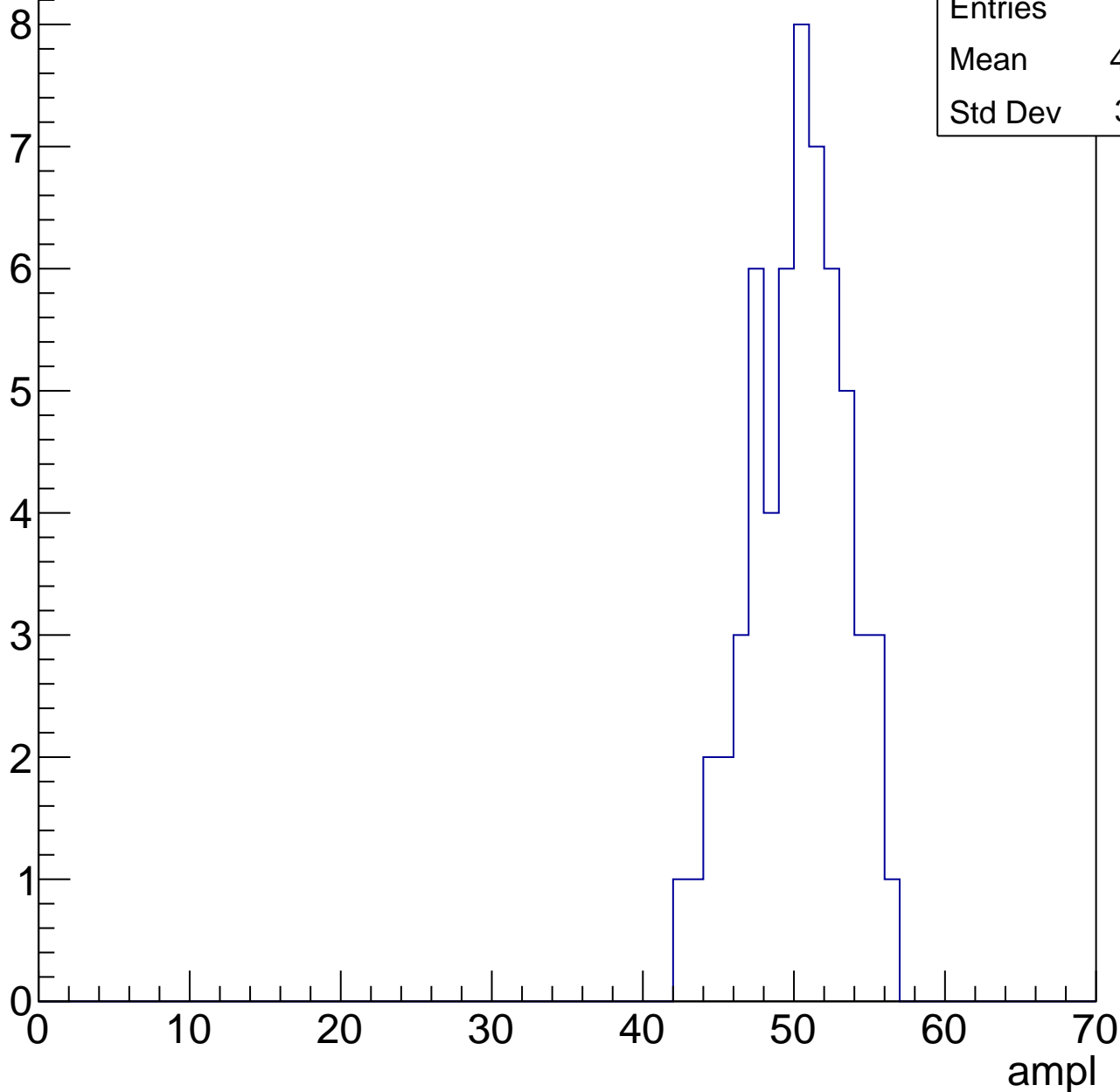


# B1L003S, U26-ch24, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

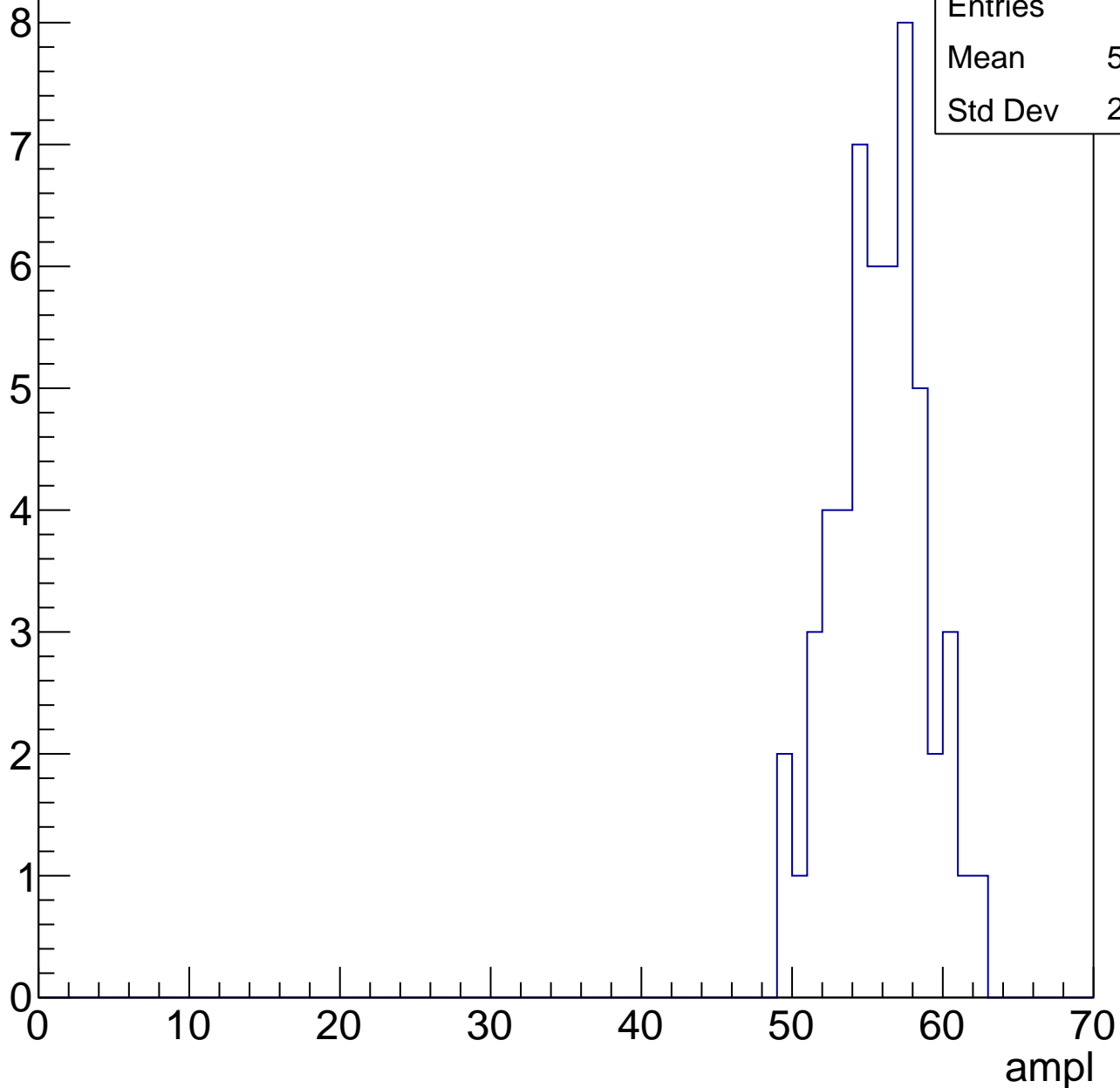
Entries	58
Mean	49.76
Std Dev	3.191



# B1L003S, U26-ch24, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U26-ch24, adc5

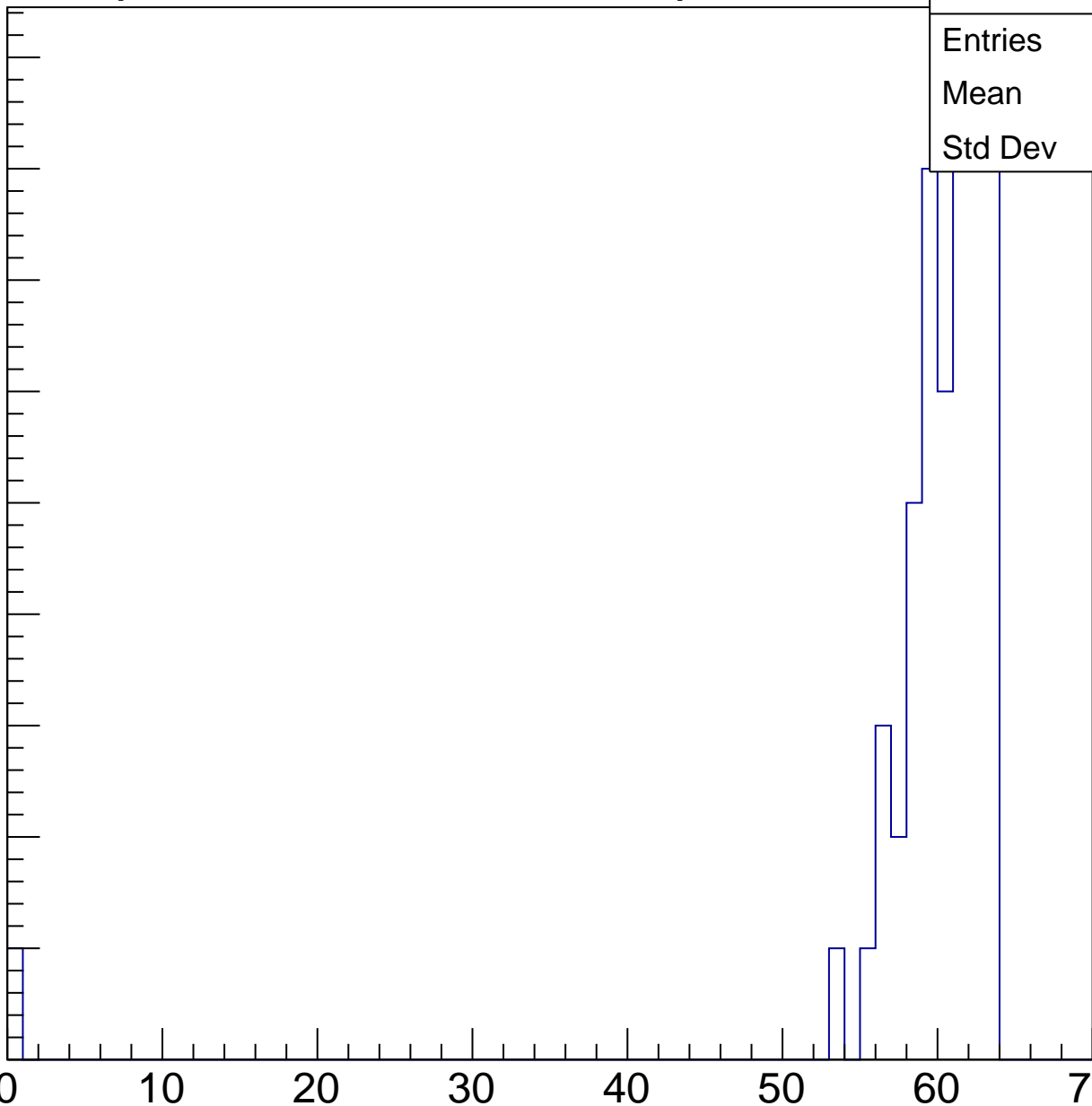
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	53
Mean	58.92
Std Dev	8.494

ampl



# B1L003S, U26-ch24, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	3
Mean	62
Std Dev	1.414



# B1L003S, U26-ch24, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L003S, U26-ch25, adc0

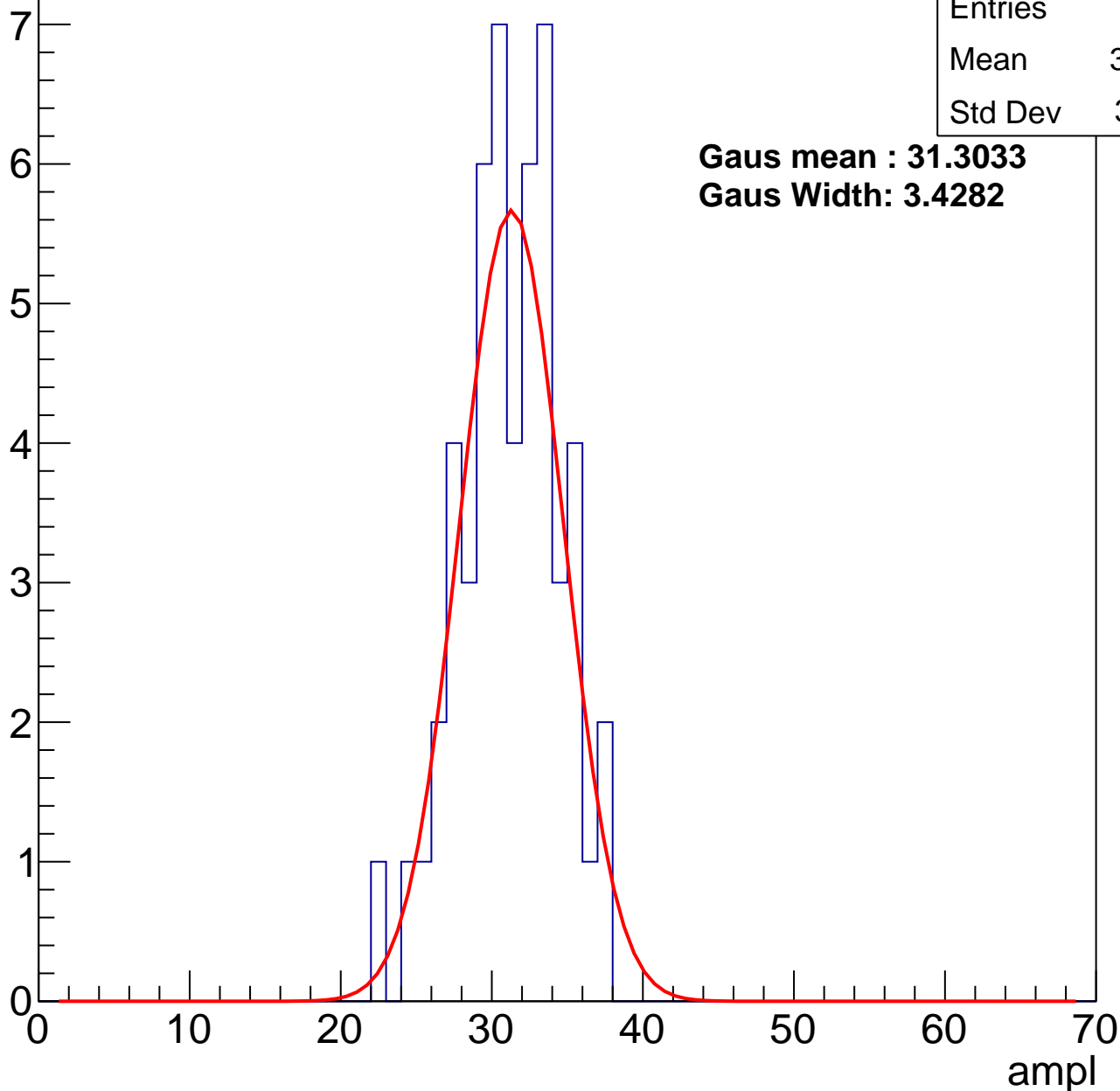
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	52
Mean	30.73
Std Dev	3.271

**Gaus mean : 31.3033**

**Gaus Width: 3.4282**



# B1L003S, U26-ch25, adc1

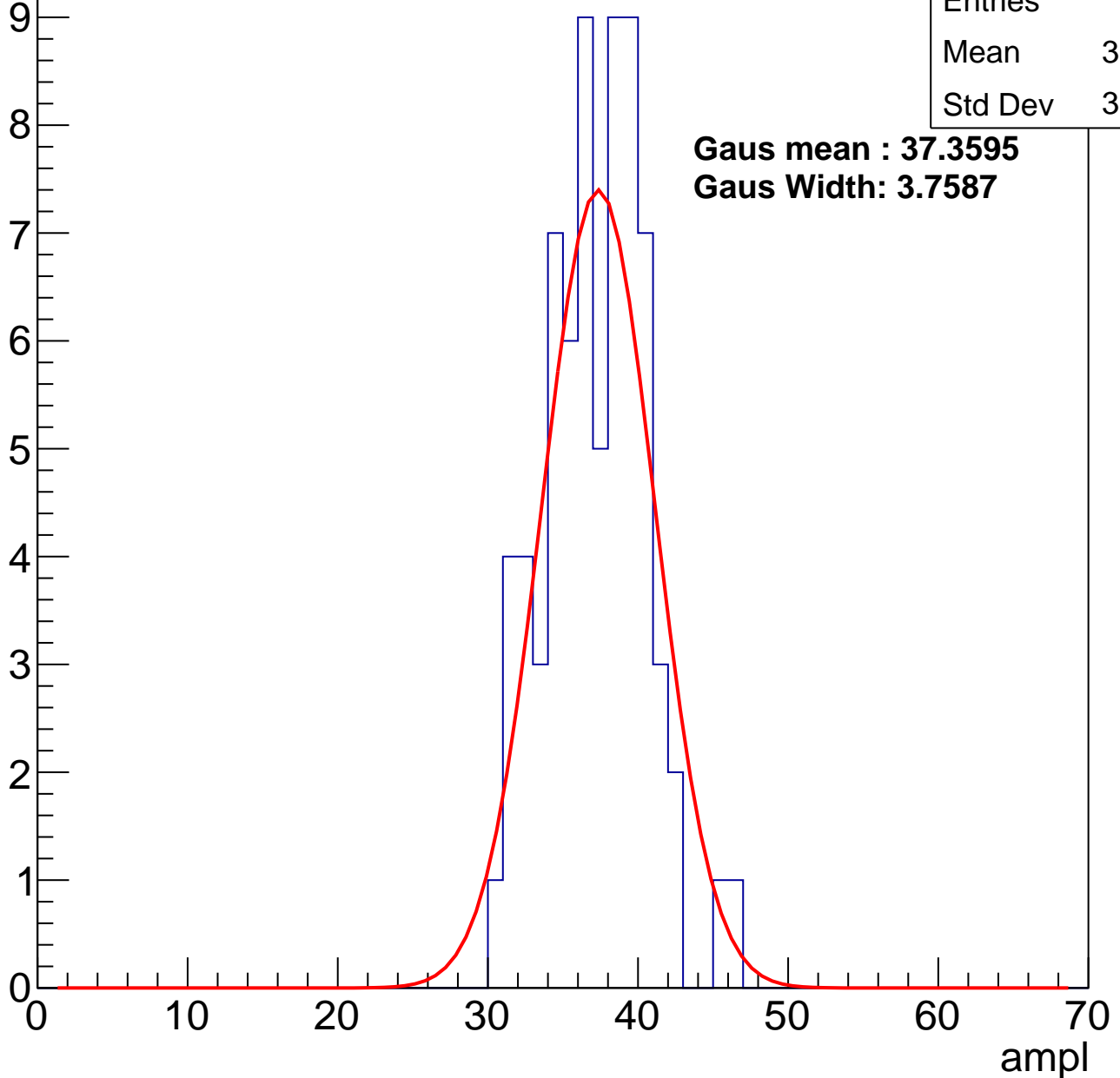
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	71
Mean	36.75
Std Dev	3.322

**Gaus mean : 37.3595**

**Gaus Width: 3.7587**



# B1L003S, U26-ch25, adc2

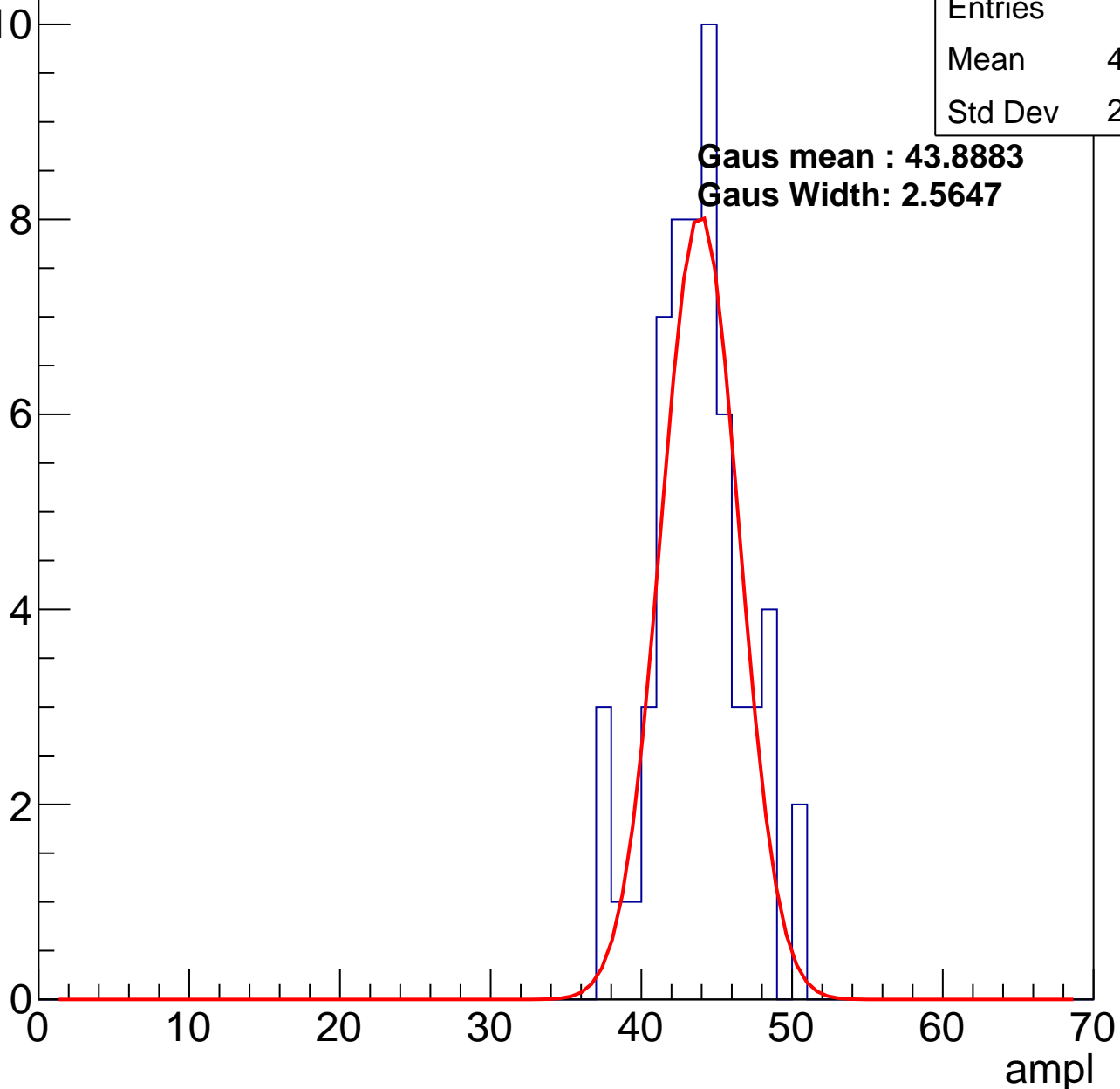
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	43.32
Std Dev	2.948

**Gaus mean : 43.8883**

**Gaus Width: 2.5647**

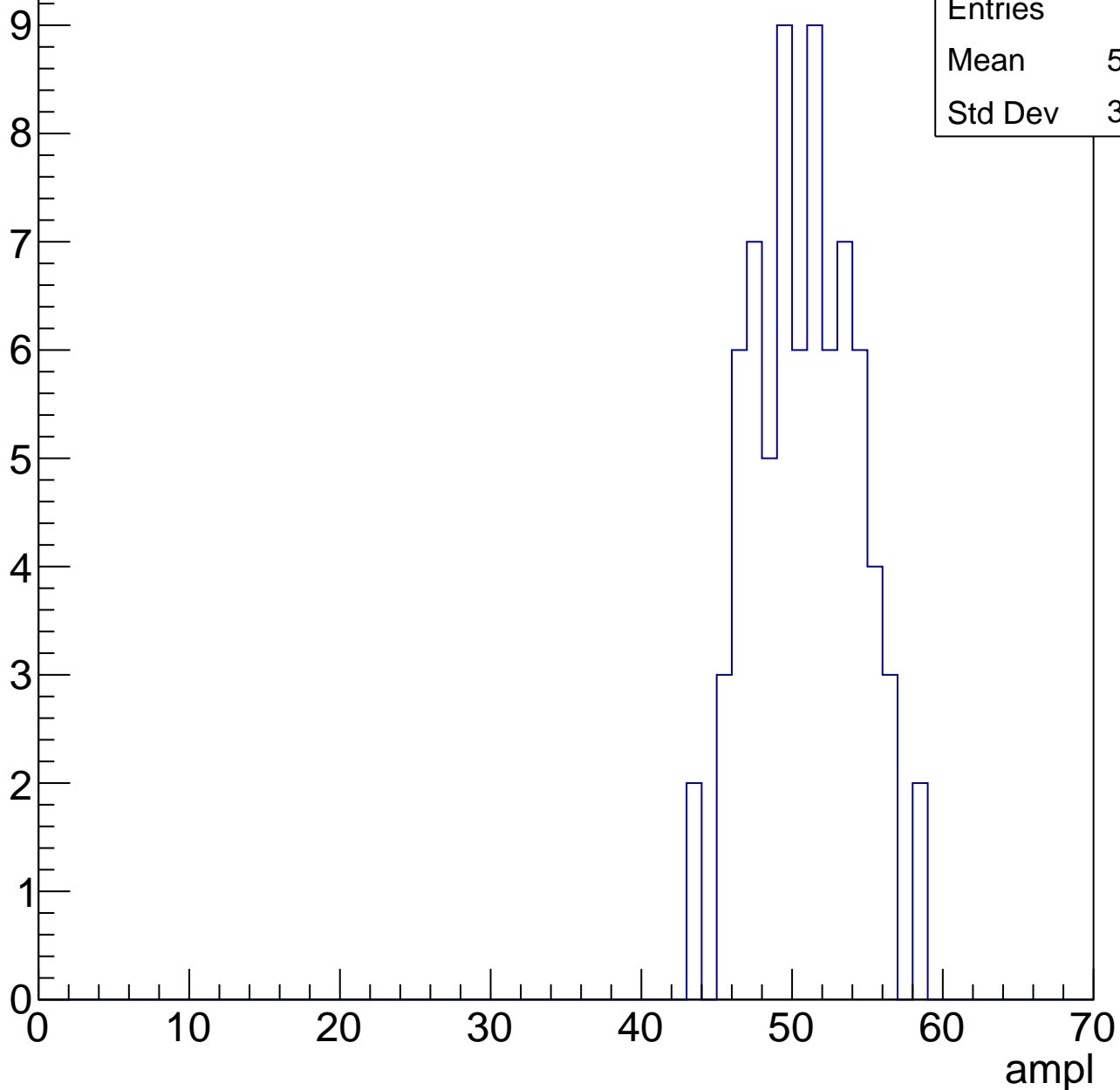


# B1L003S, U26-ch25, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	75
Mean	50.36
Std Dev	3.424



# B1L003S, U26-ch25, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	62
Mean	56.4
Std Dev	3.255

Entry

10

8

6

4

2

0

0

10

20

30

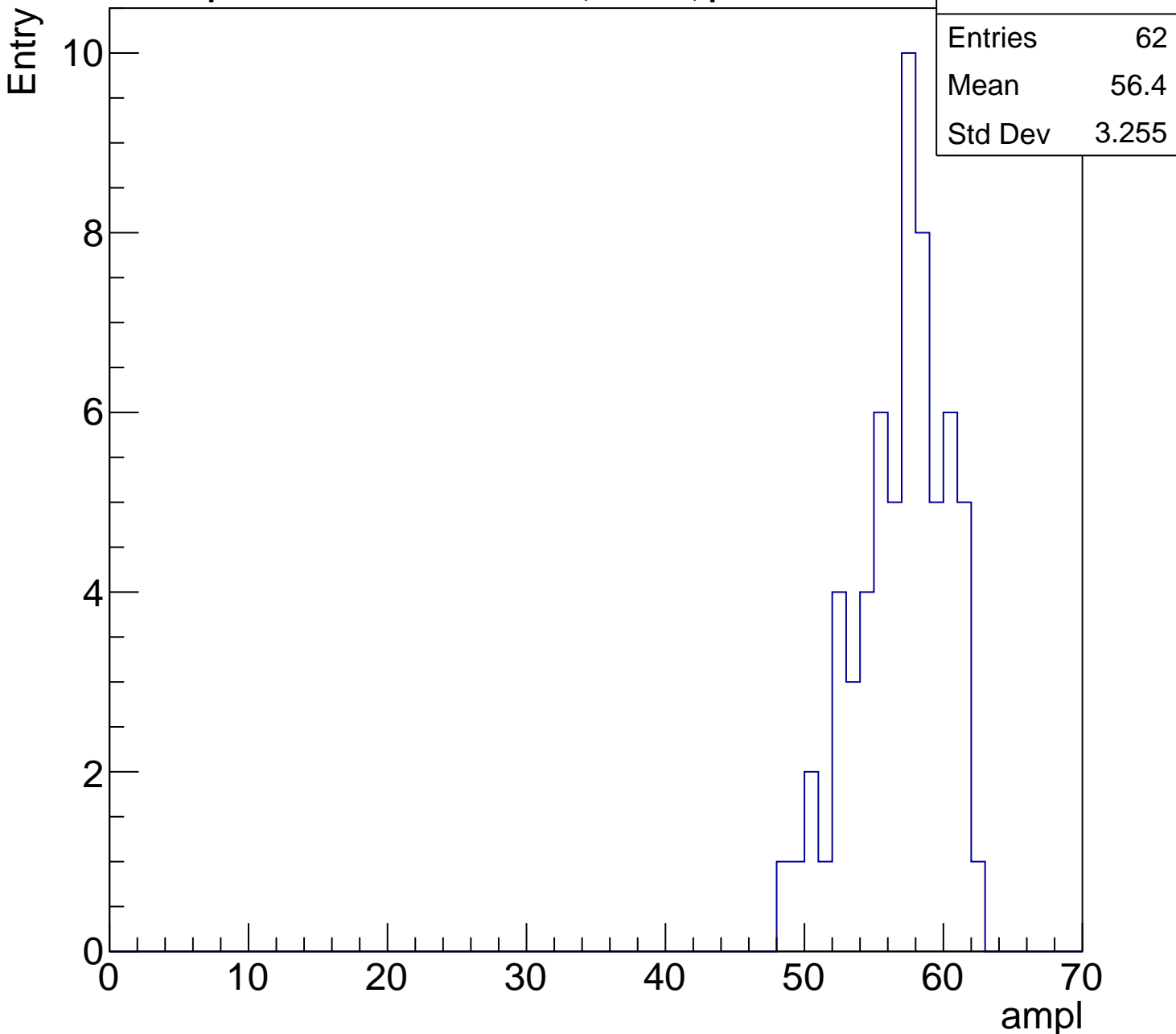
40

50

60

ampl

70

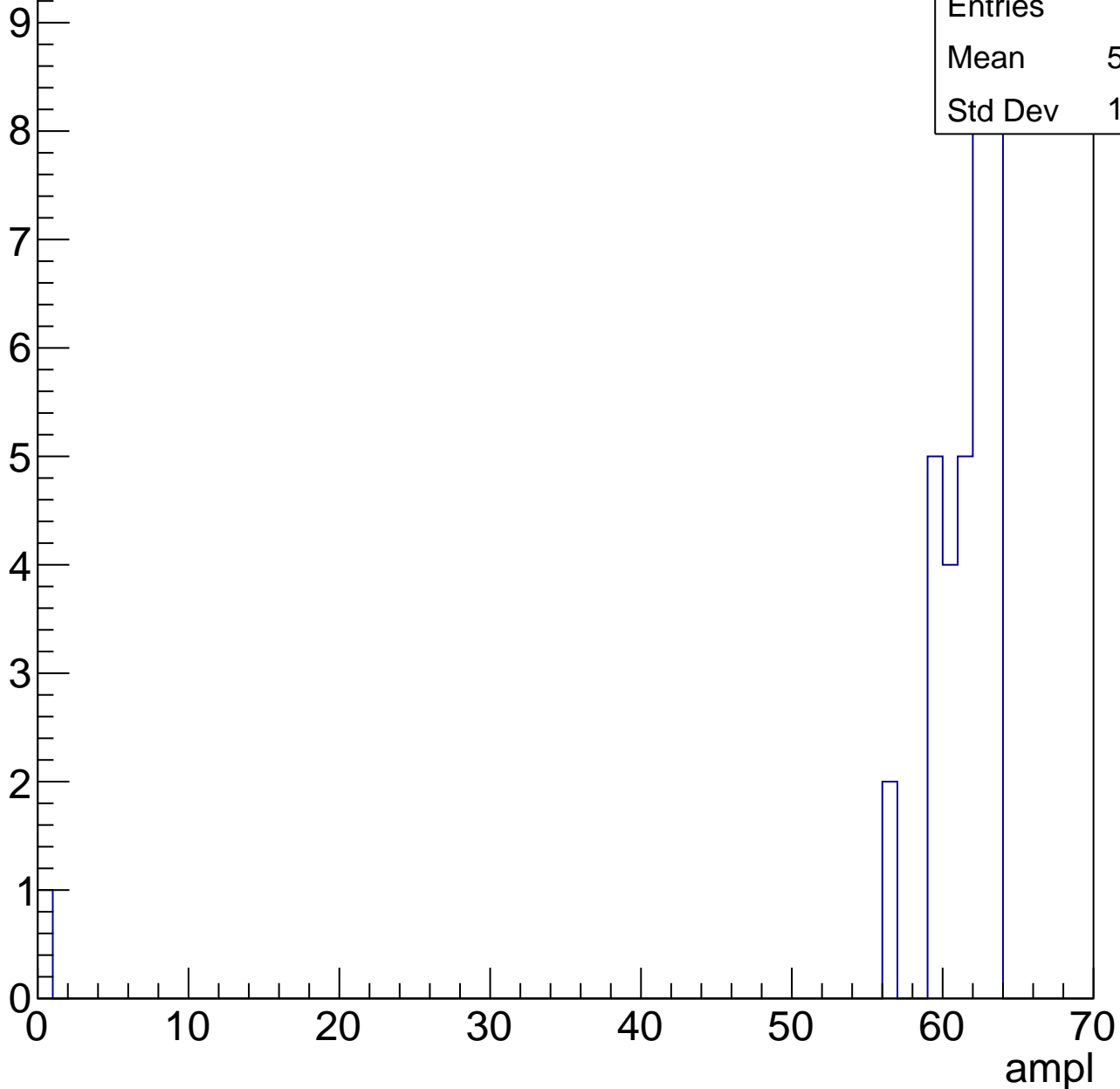


# B1L003S, U26-ch25, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	34
Mean	59.24
Std Dev	10.47



# B1L003S, U26-ch25, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch25, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U26-ch26, adc0

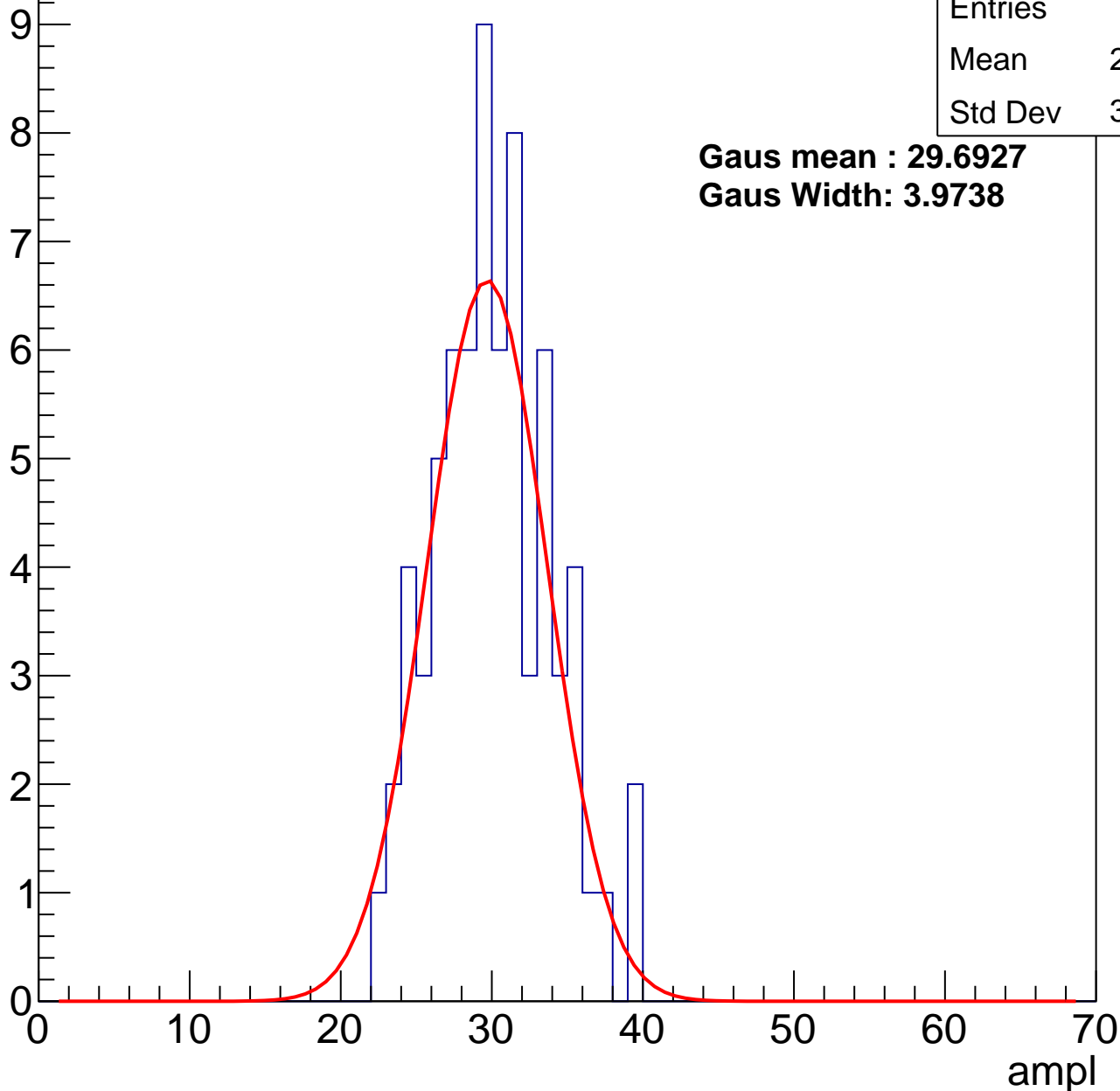
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	29.64
Std Dev	3.795

**Gaus mean : 29.6927**

**Gaus Width: 3.9738**



# B1L003S, U26-ch26, adc1

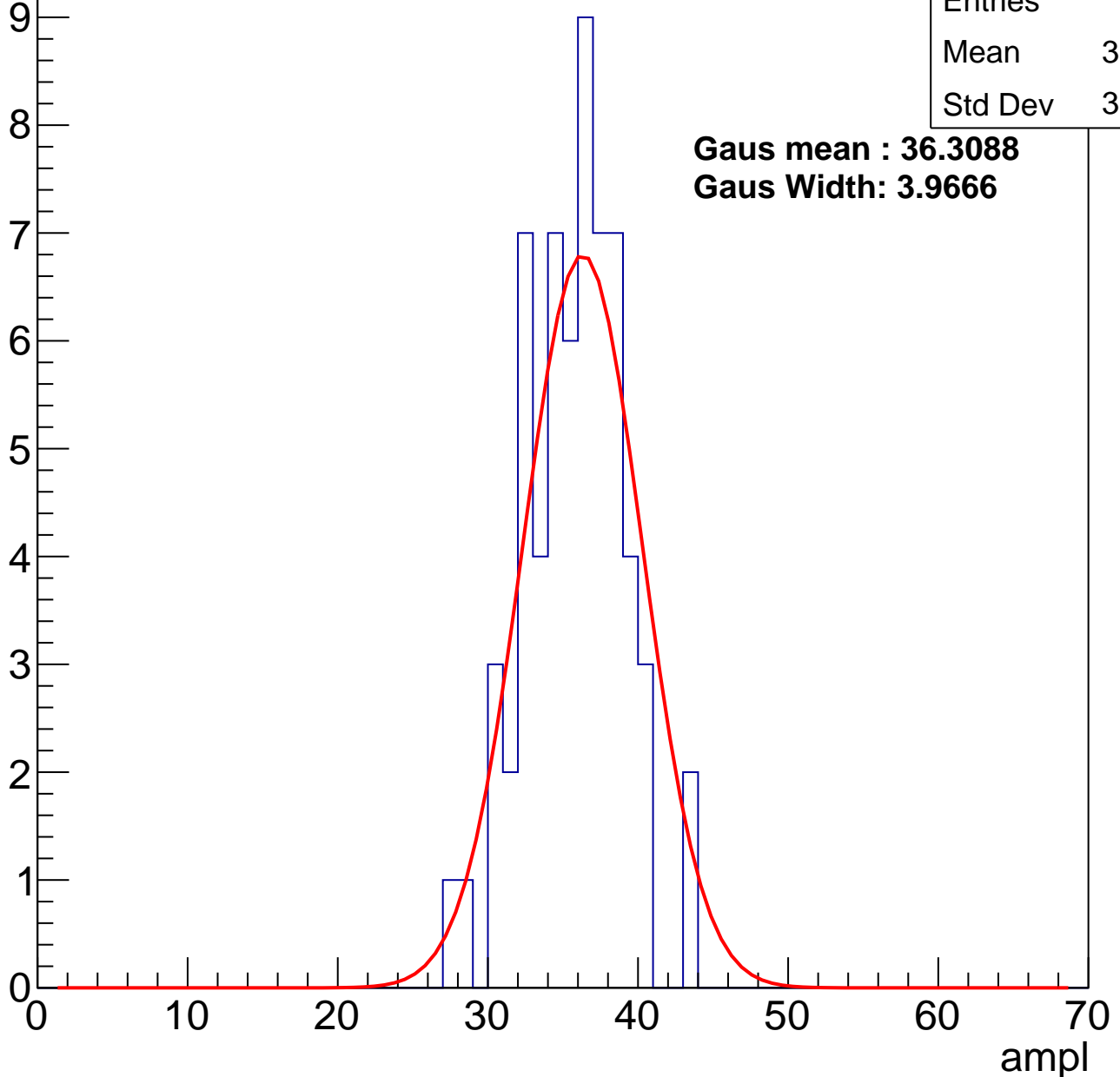
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	35.27
Std Dev	3.257

**Gaus mean : 36.3088**

**Gaus Width: 3.9666**



# B1L003S, U26-ch26, adc2

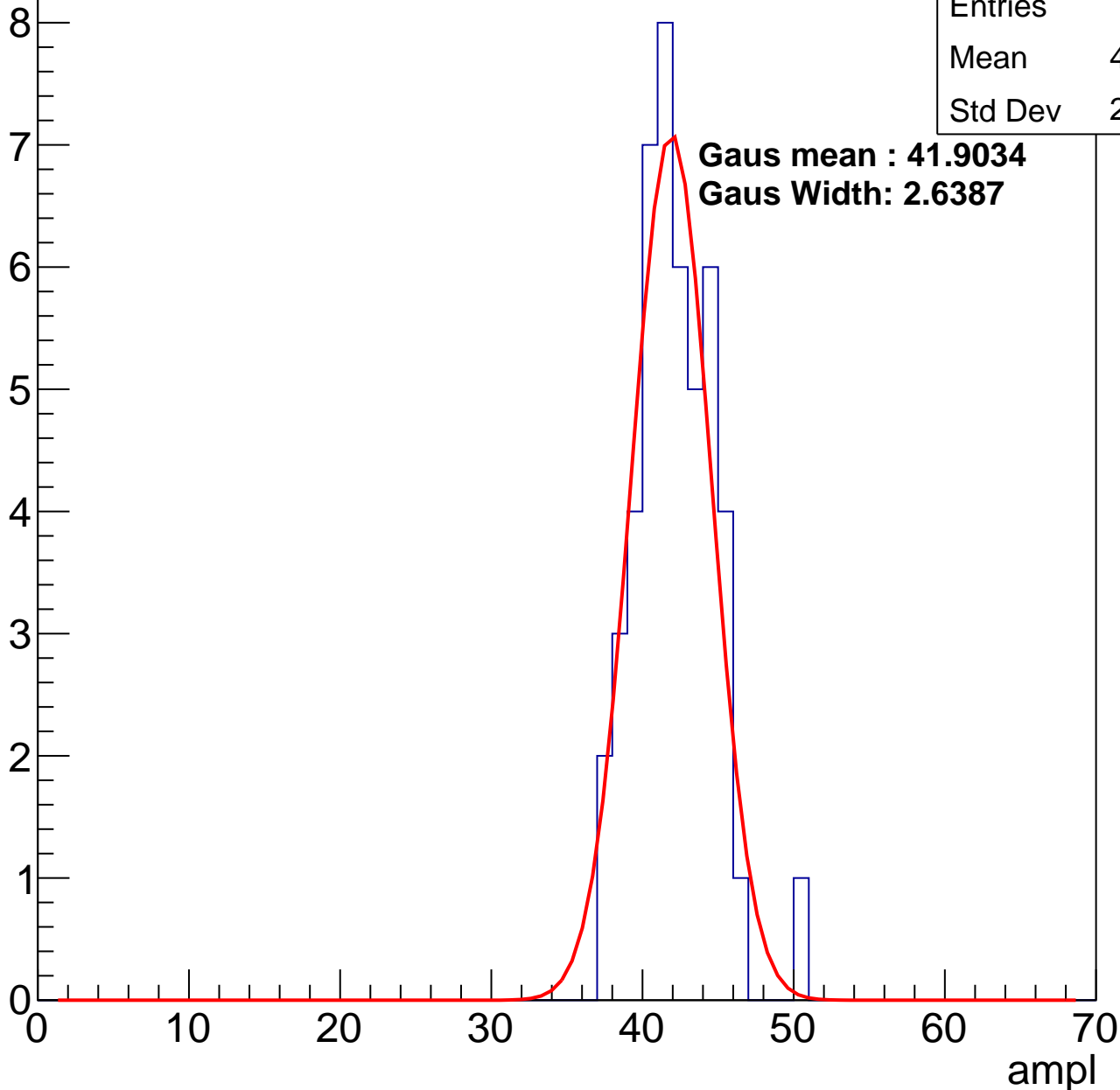
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	47
Mean	41.68
Std Dev	2.569

**Gaus mean : 41.9034**

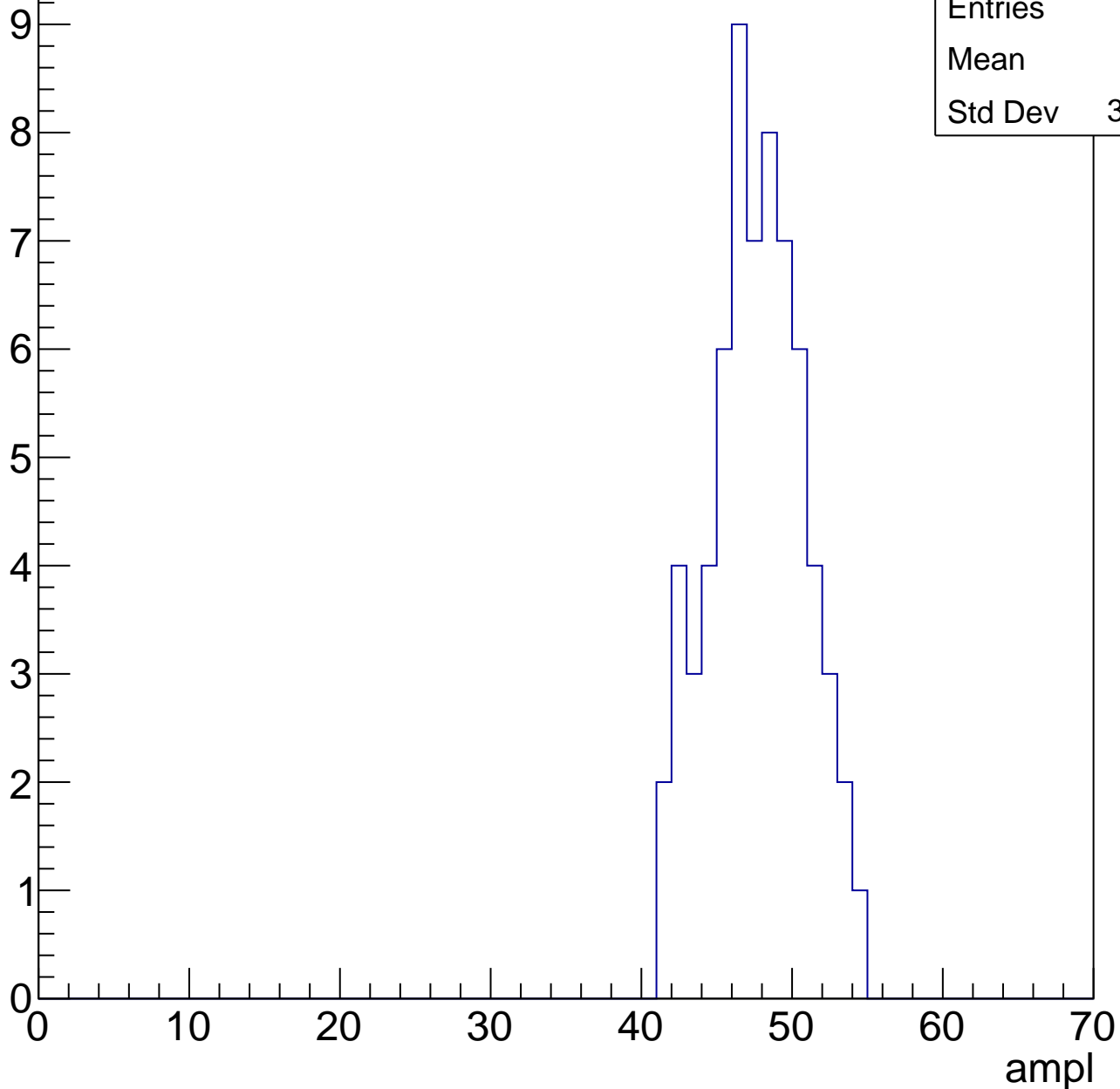
**Gaus Width: 2.6387**



# B1L003S, U26-ch26, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

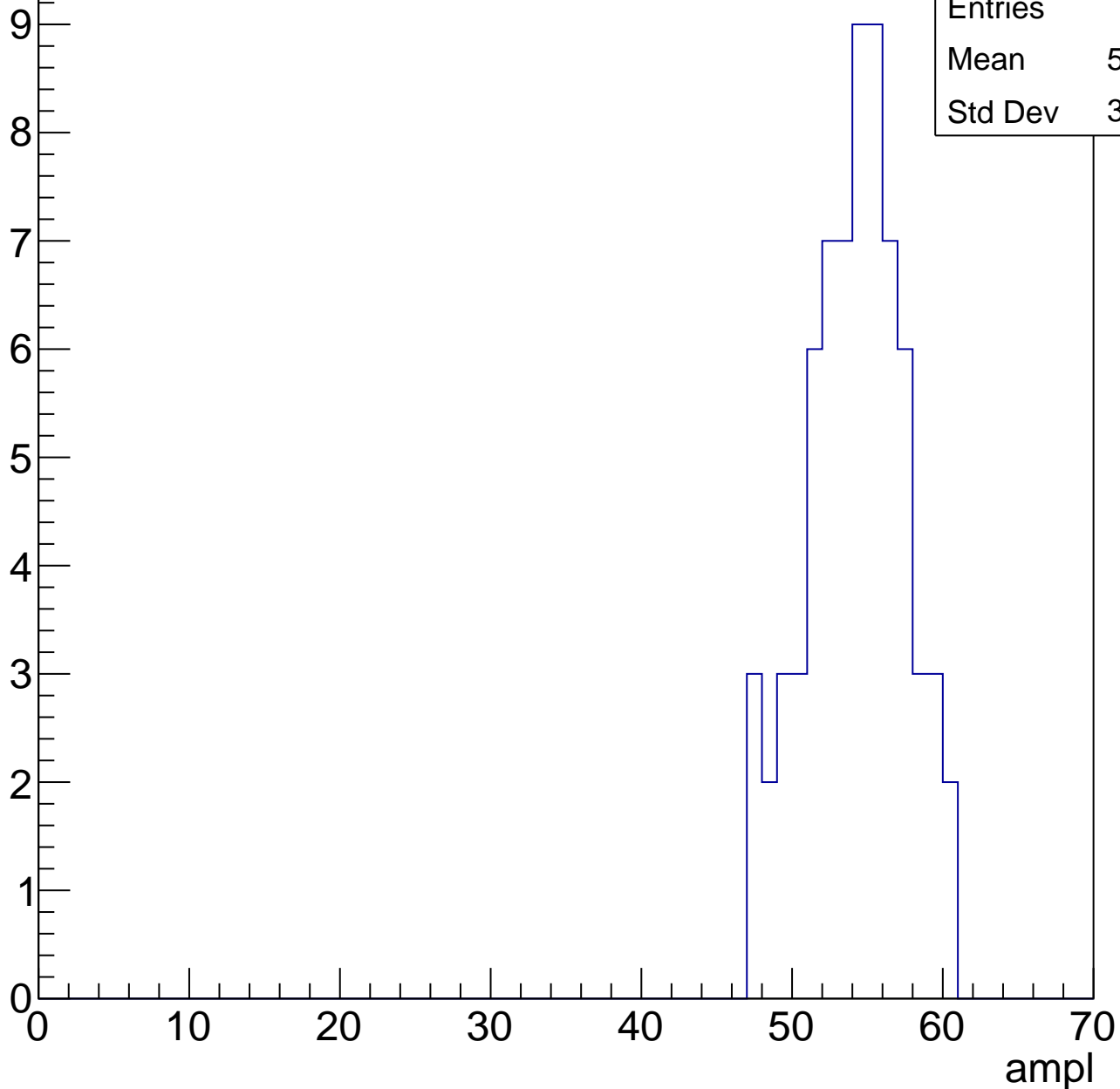
Entry



# B1L003S, U26-ch26, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

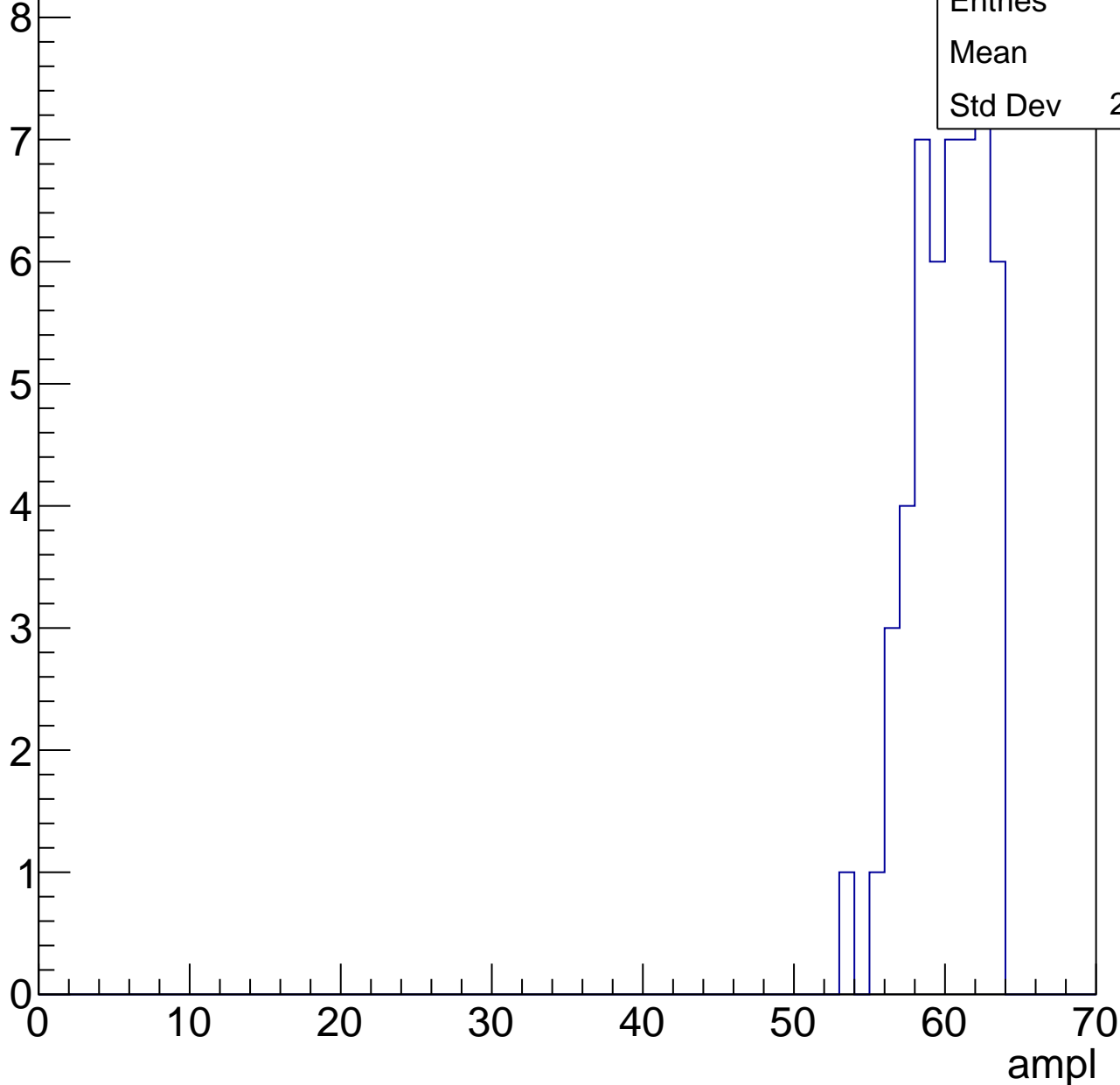


# B1L003S, U26-ch26, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

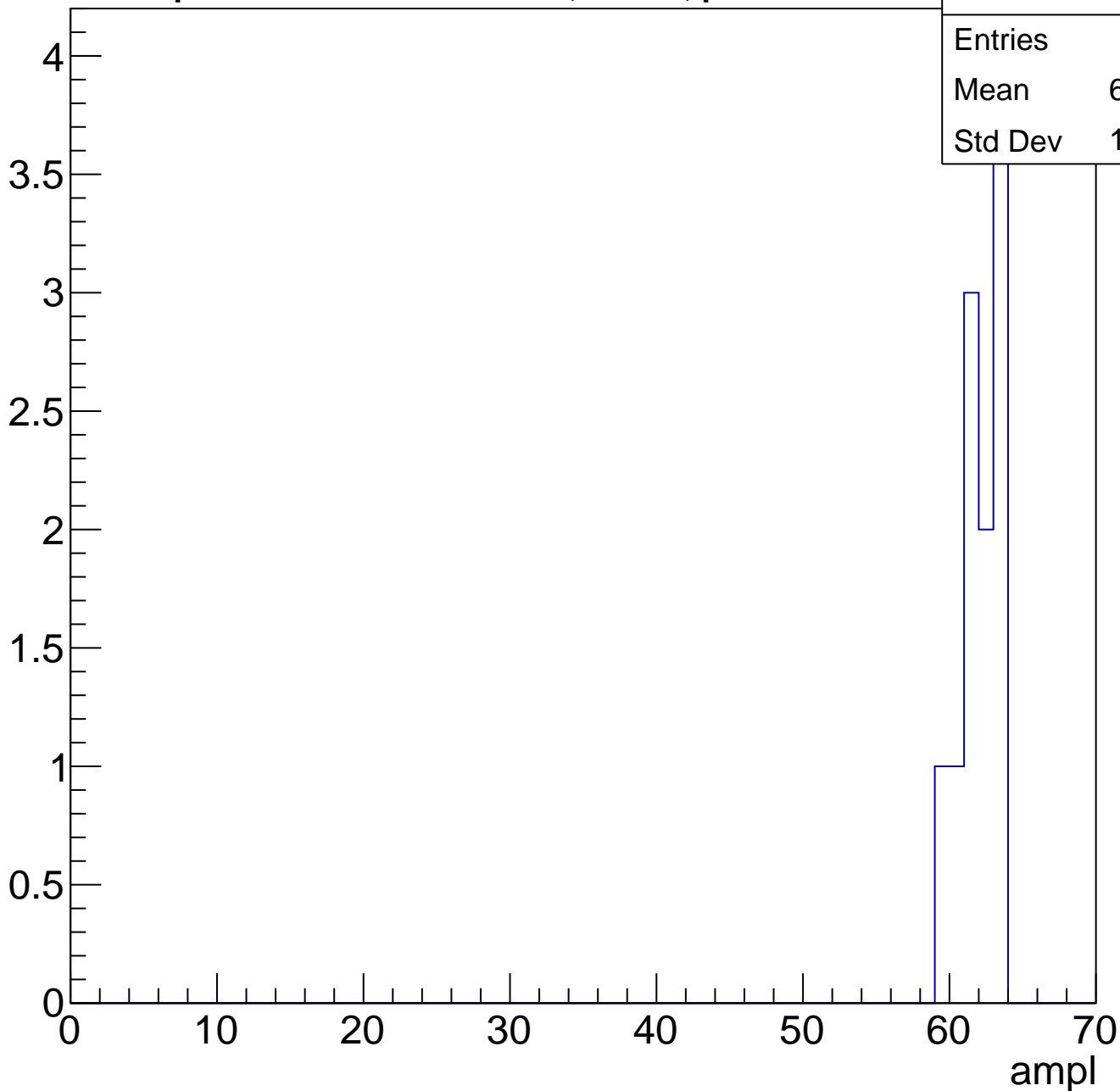
Entries	50
Mean	59.7
Std Dev	2.369



# B1L003S, U26-ch26, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch26, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L003S, U26-ch27, adc0

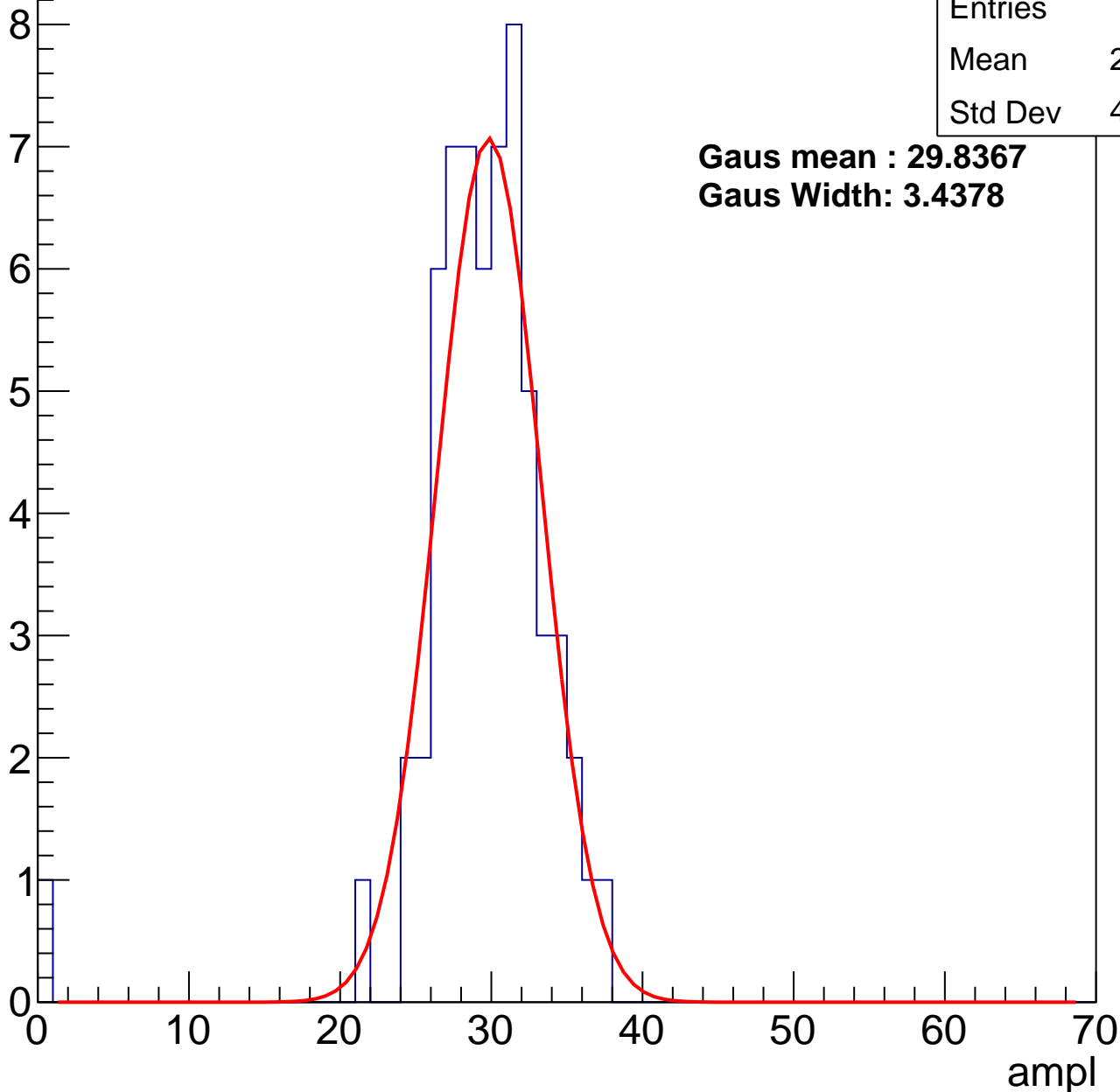
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	28.97
Std Dev	4.866

**Gaus mean : 29.8367**

**Gaus Width: 3.4378**



# B1L003S, U26-ch27, adc1

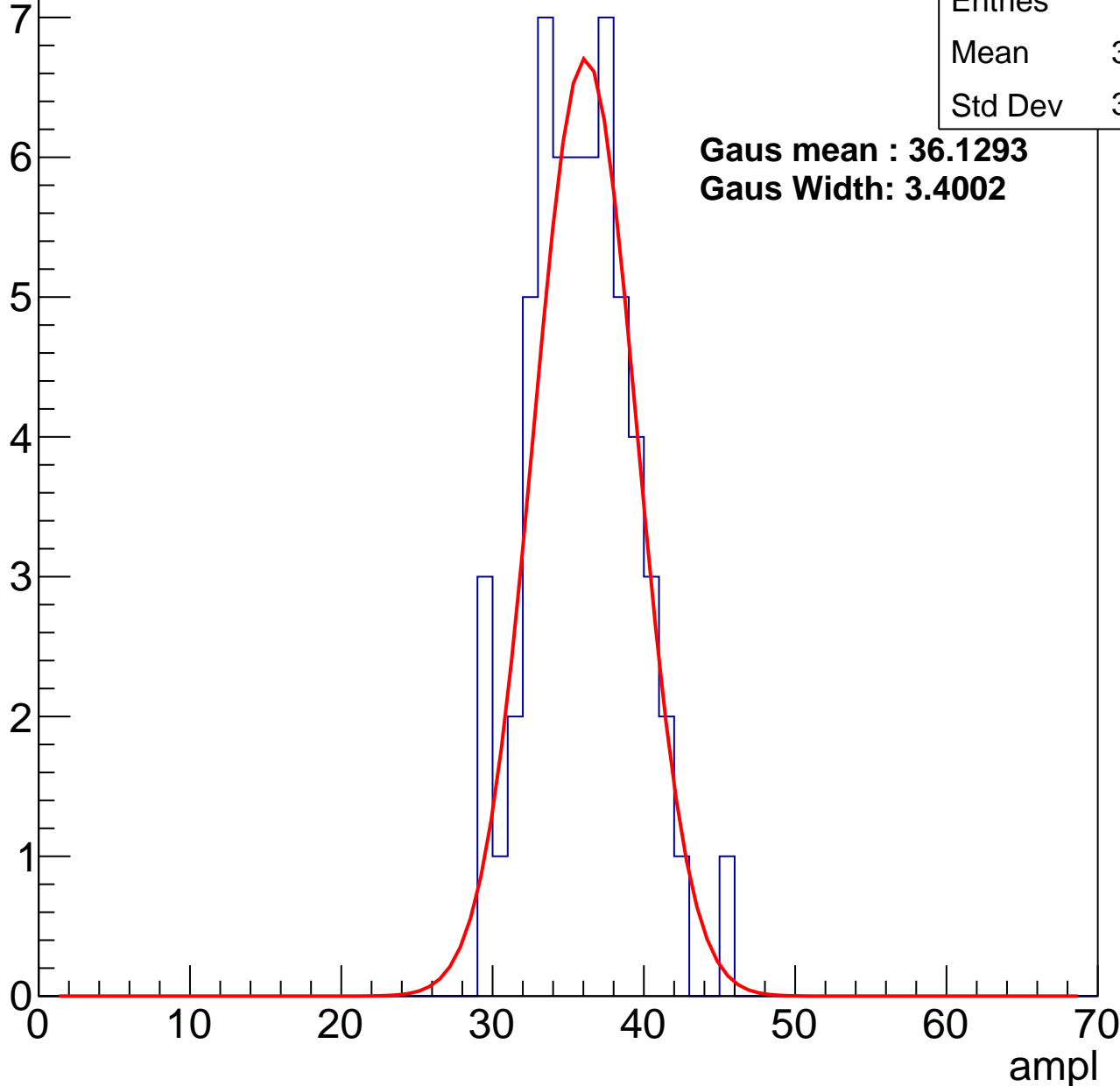
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	35.49
Std Dev	3.367

**Gaus mean : 36.1293**

**Gaus Width: 3.4002**



# B1L003S, U26-ch27, adc2

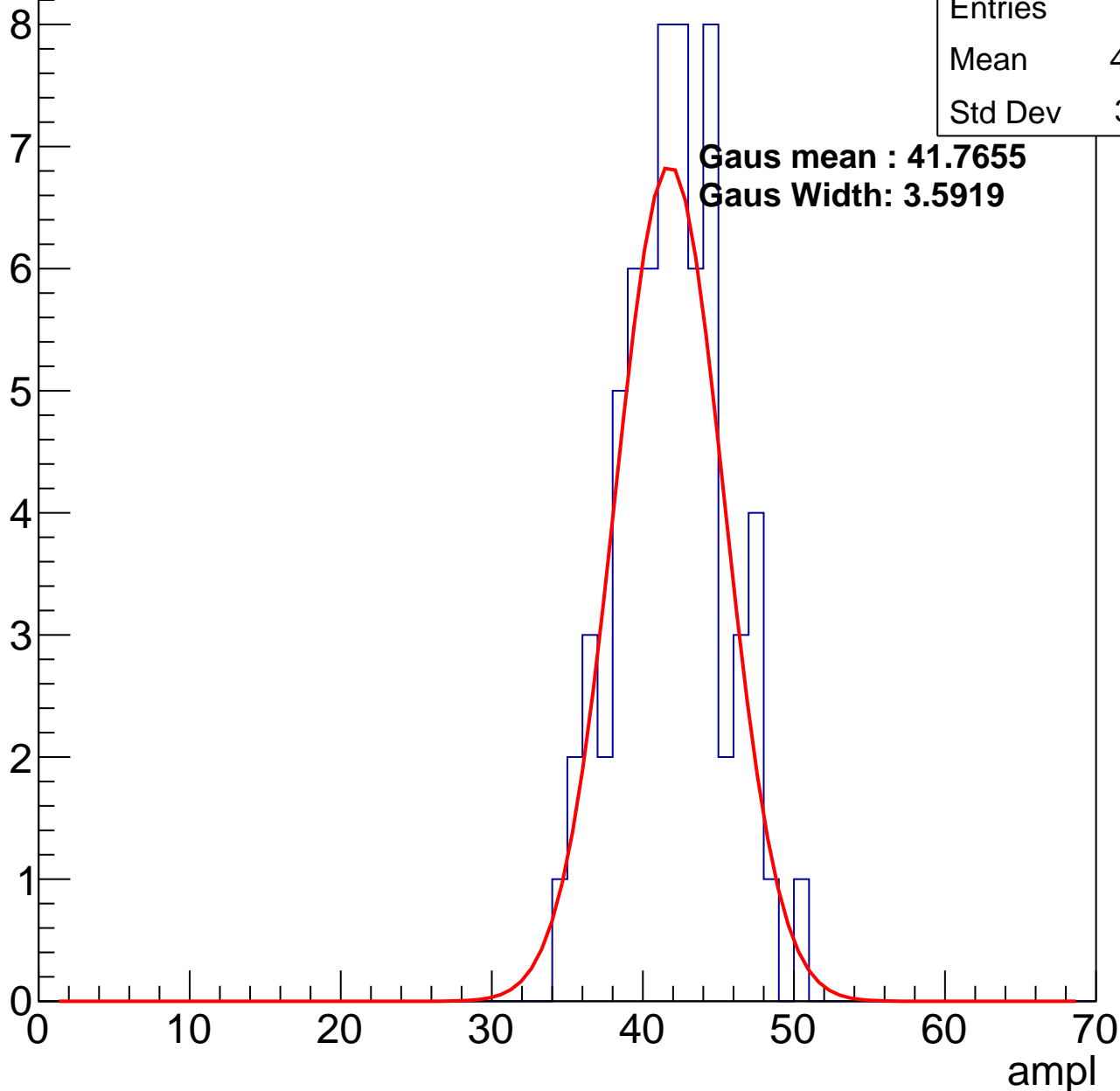
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	41.48
Std Dev	3.421

**Gaus mean : 41.7655**

**Gaus Width: 3.5919**



# B1L003S, U26-ch27, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

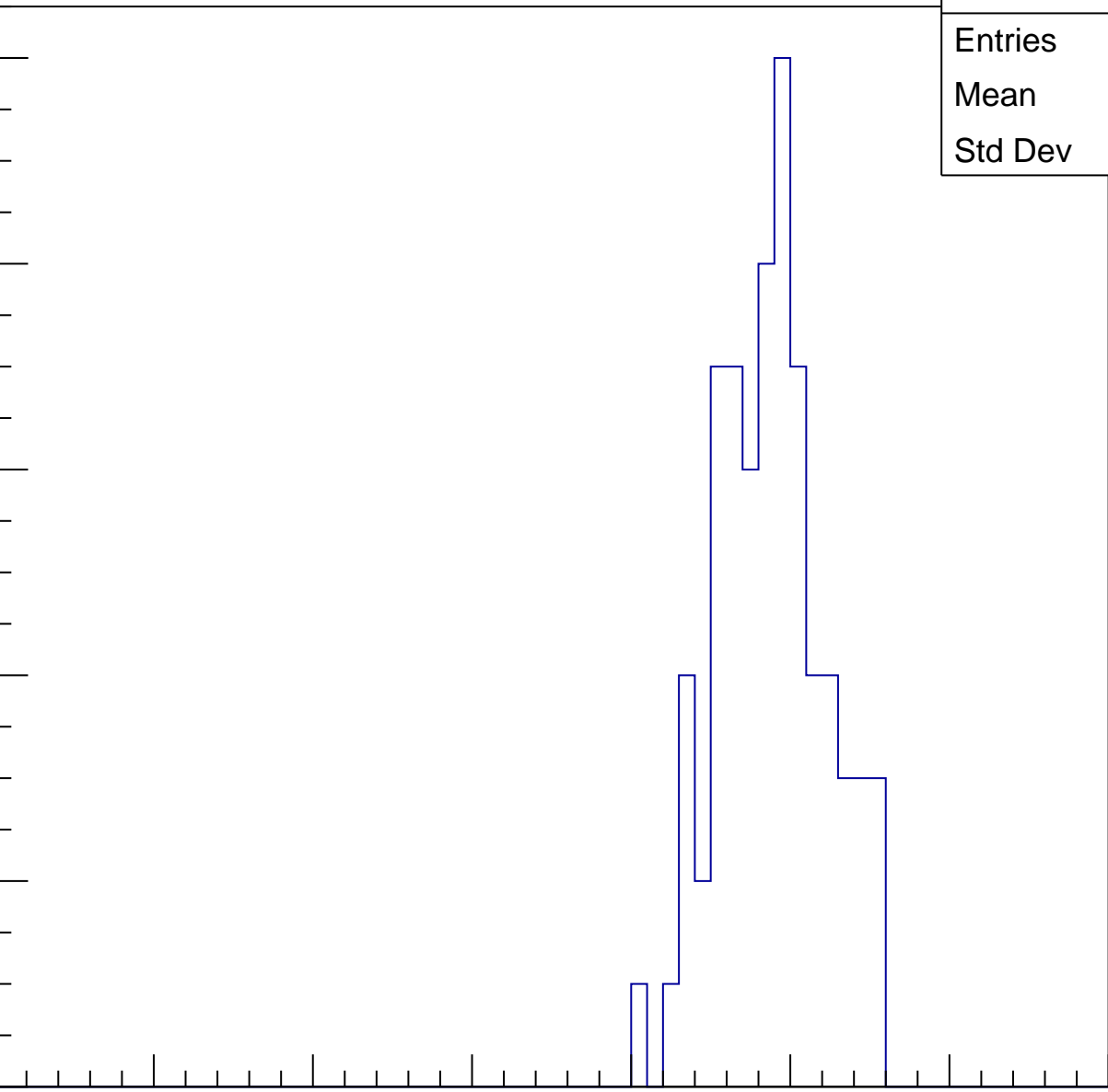
Entries	70
Mean	48.33
Std Dev	3.358

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

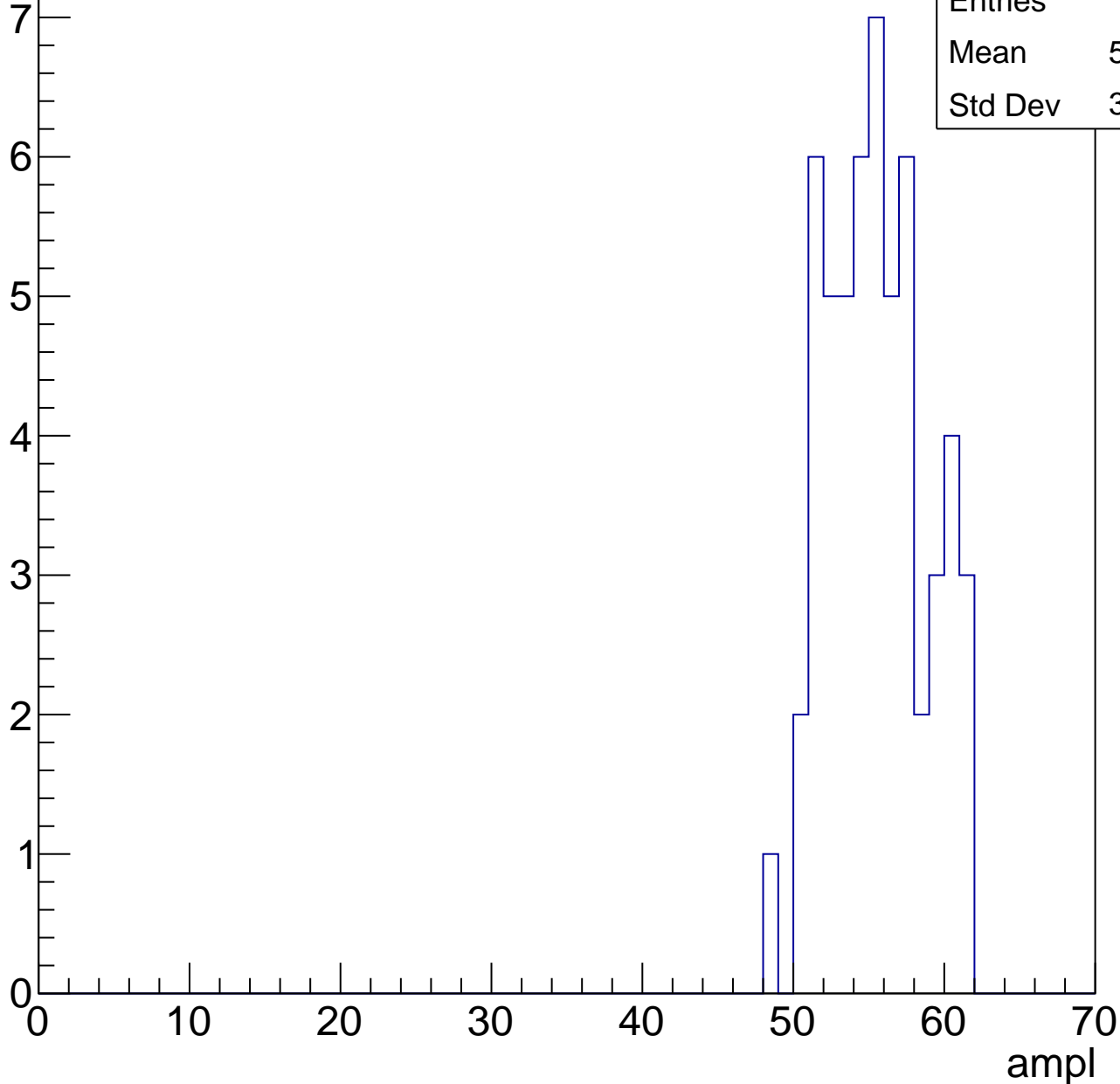


# B1L003S, U26-ch27, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	55.02
Std Dev	3.216

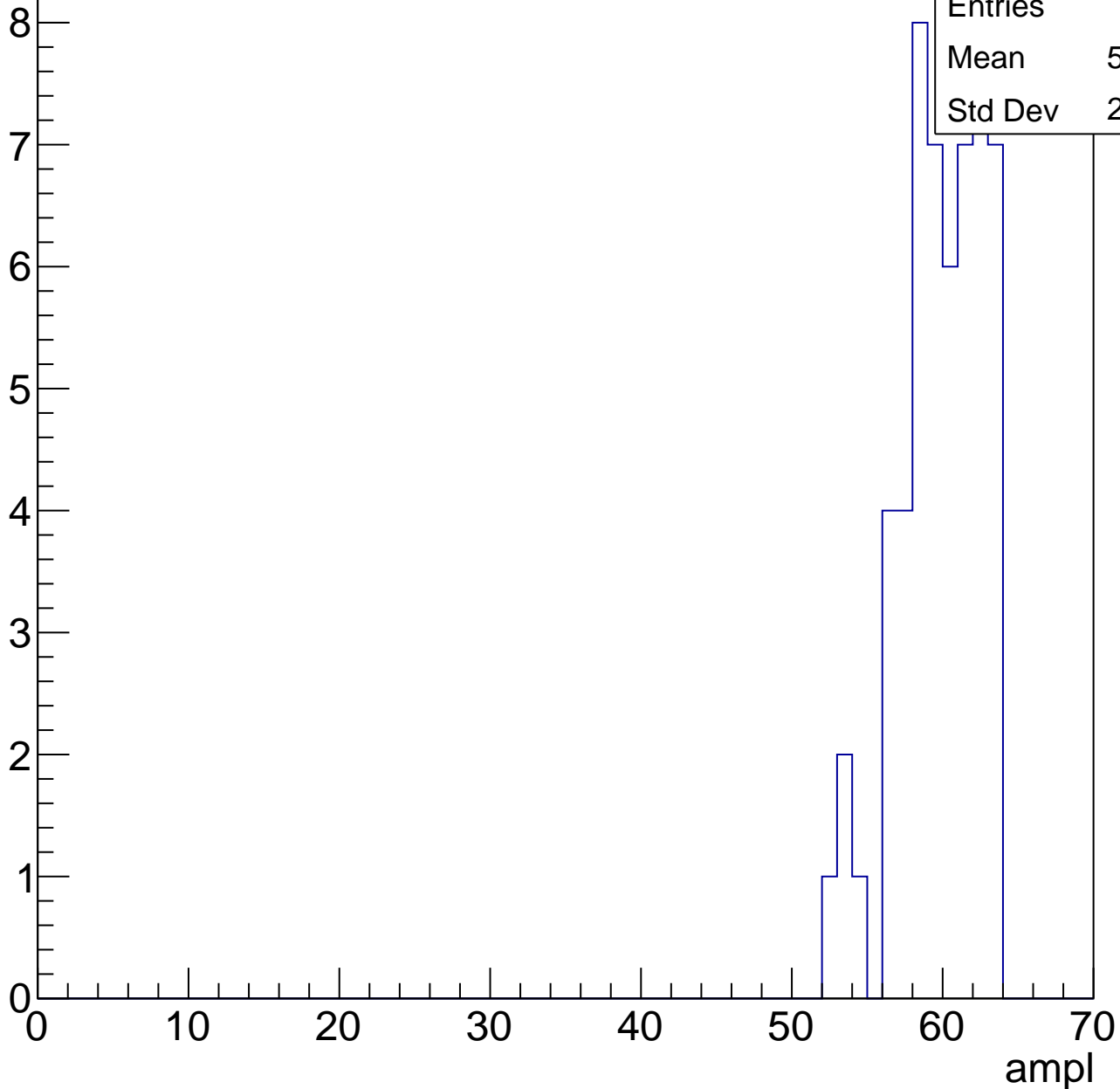


# B1L003S, U26-ch27, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

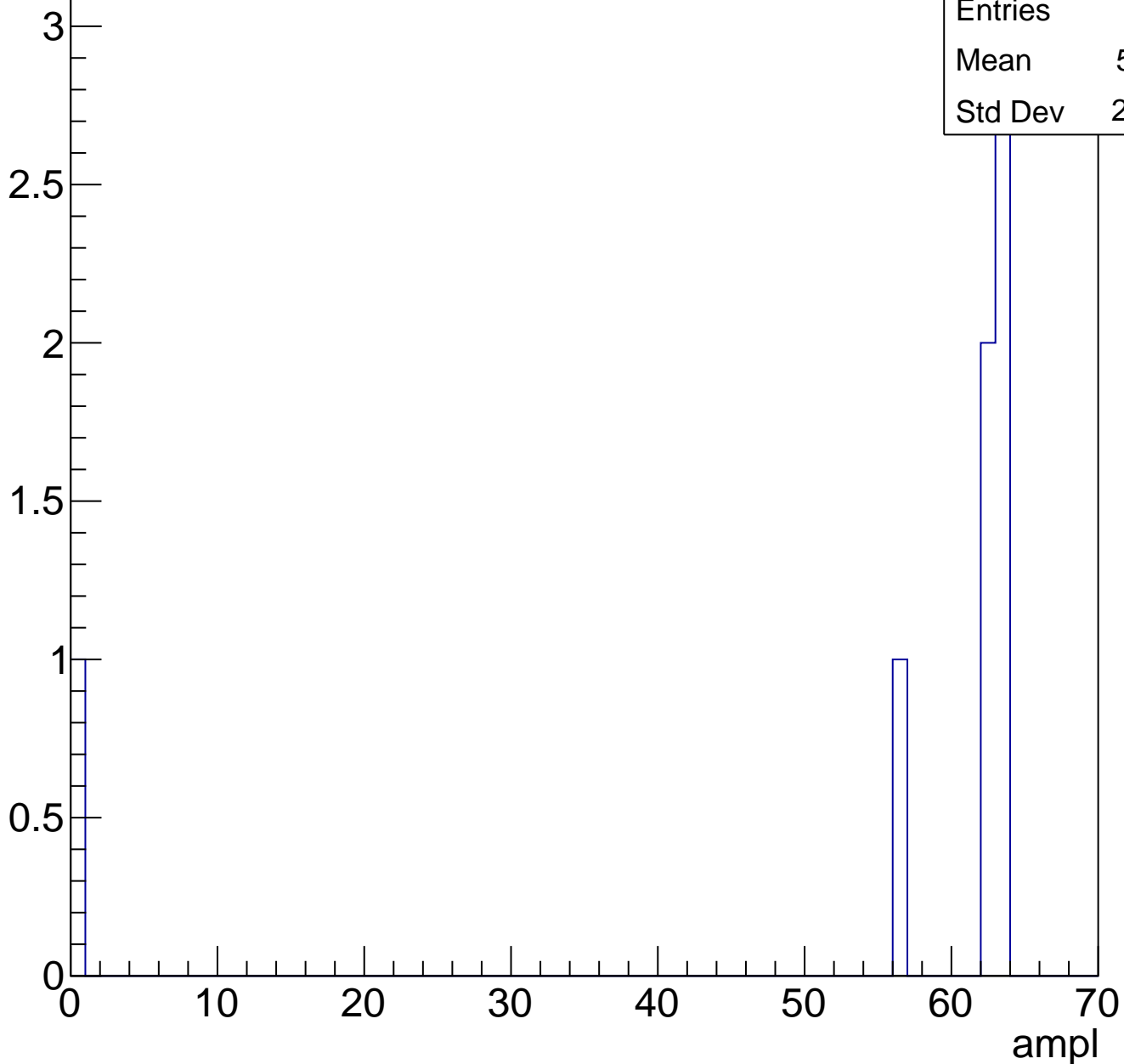
Entries	55
Mean	59.36
Std Dev	2.753



# B1L003S, U26-ch27, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch27, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U26-ch28, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	84
Mean	29.38
Std Dev	4.771

**Gaus mean : 30.8604**

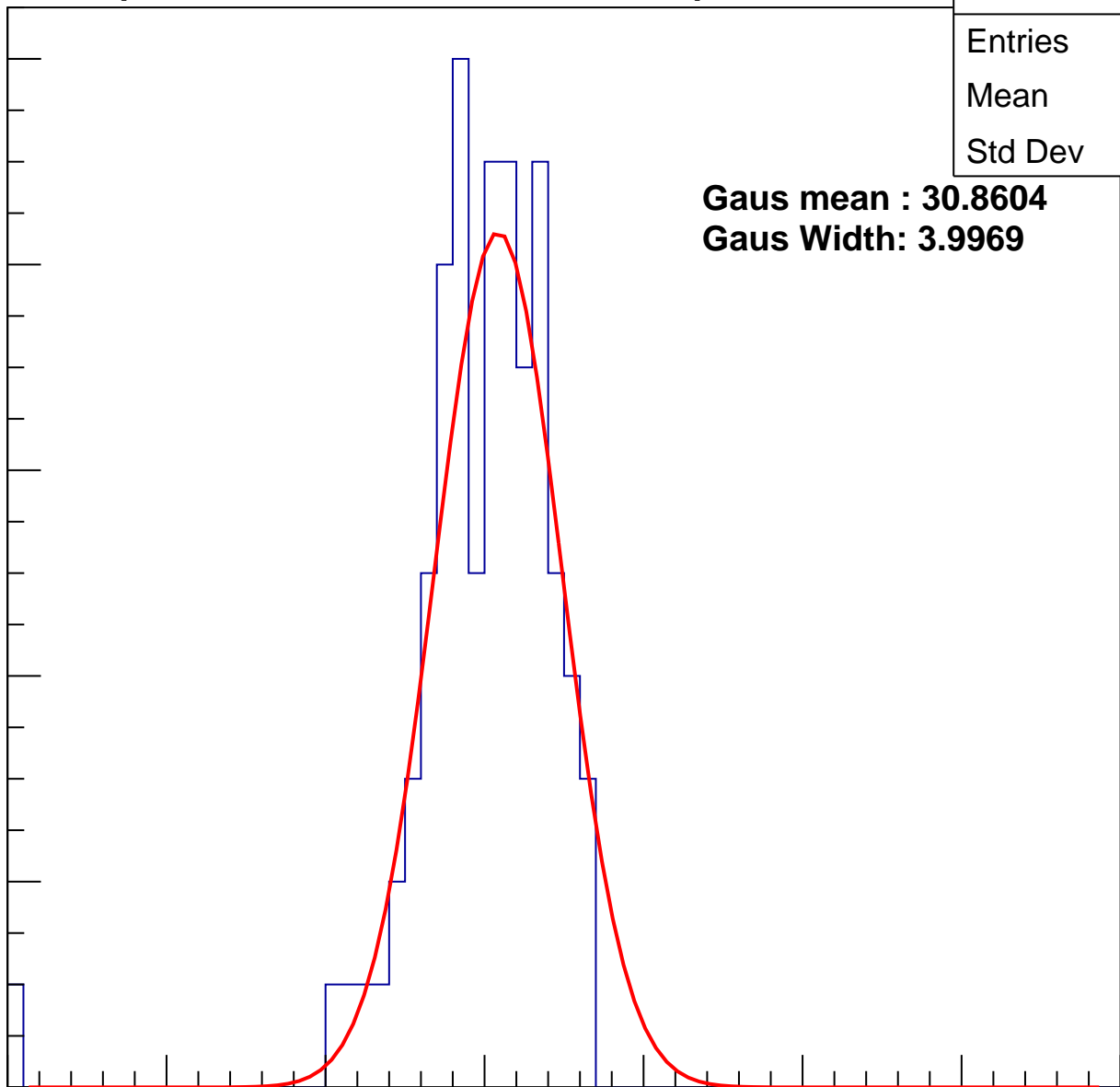
**Gaus Width: 3.9969**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

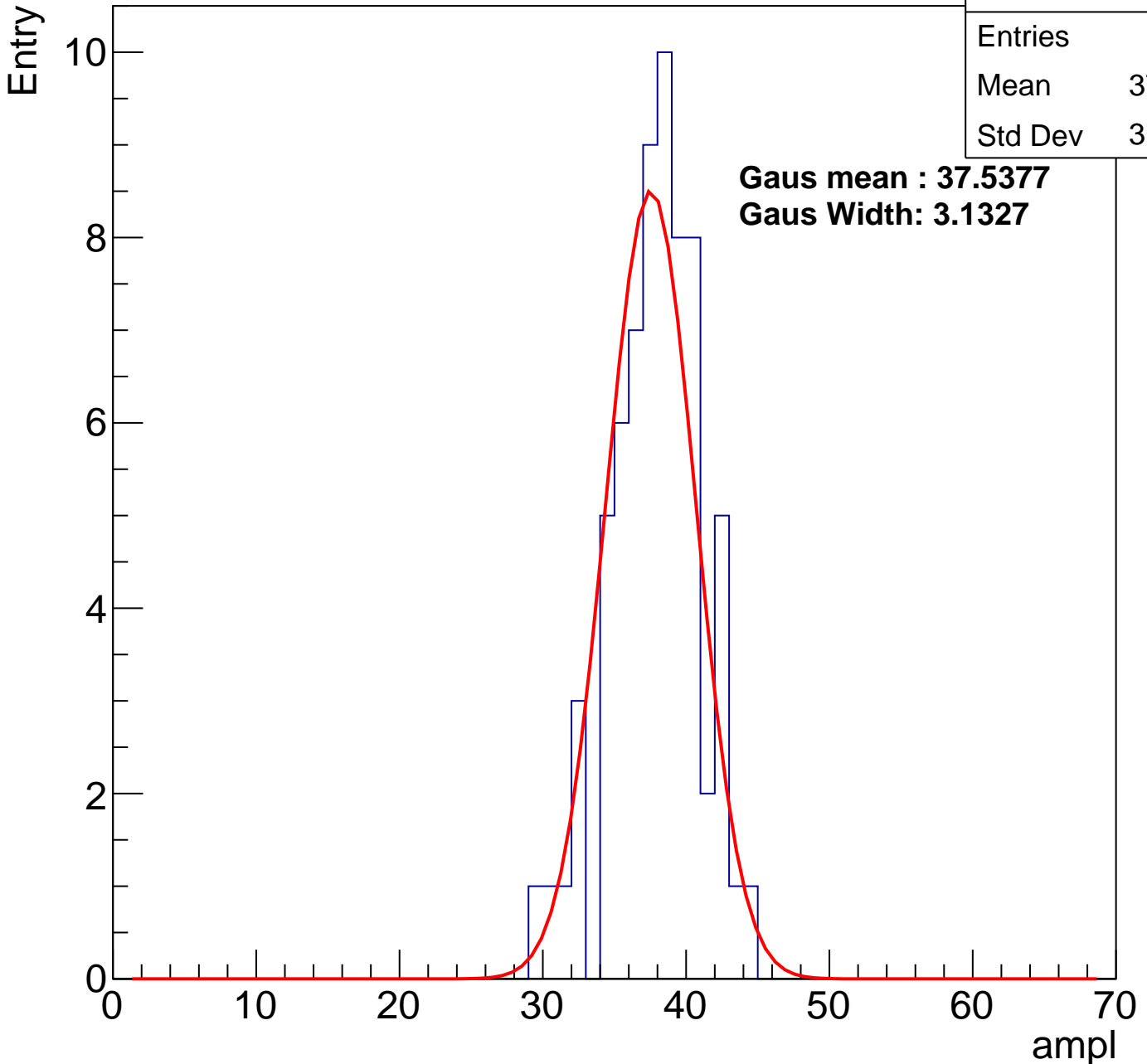


# B1L003S, U26-ch28, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	68
Mean	37.38
Std Dev	3.082

**Gaus mean : 37.5377**  
**Gaus Width: 3.1327**



# B1L003S, U26-ch28, adc2

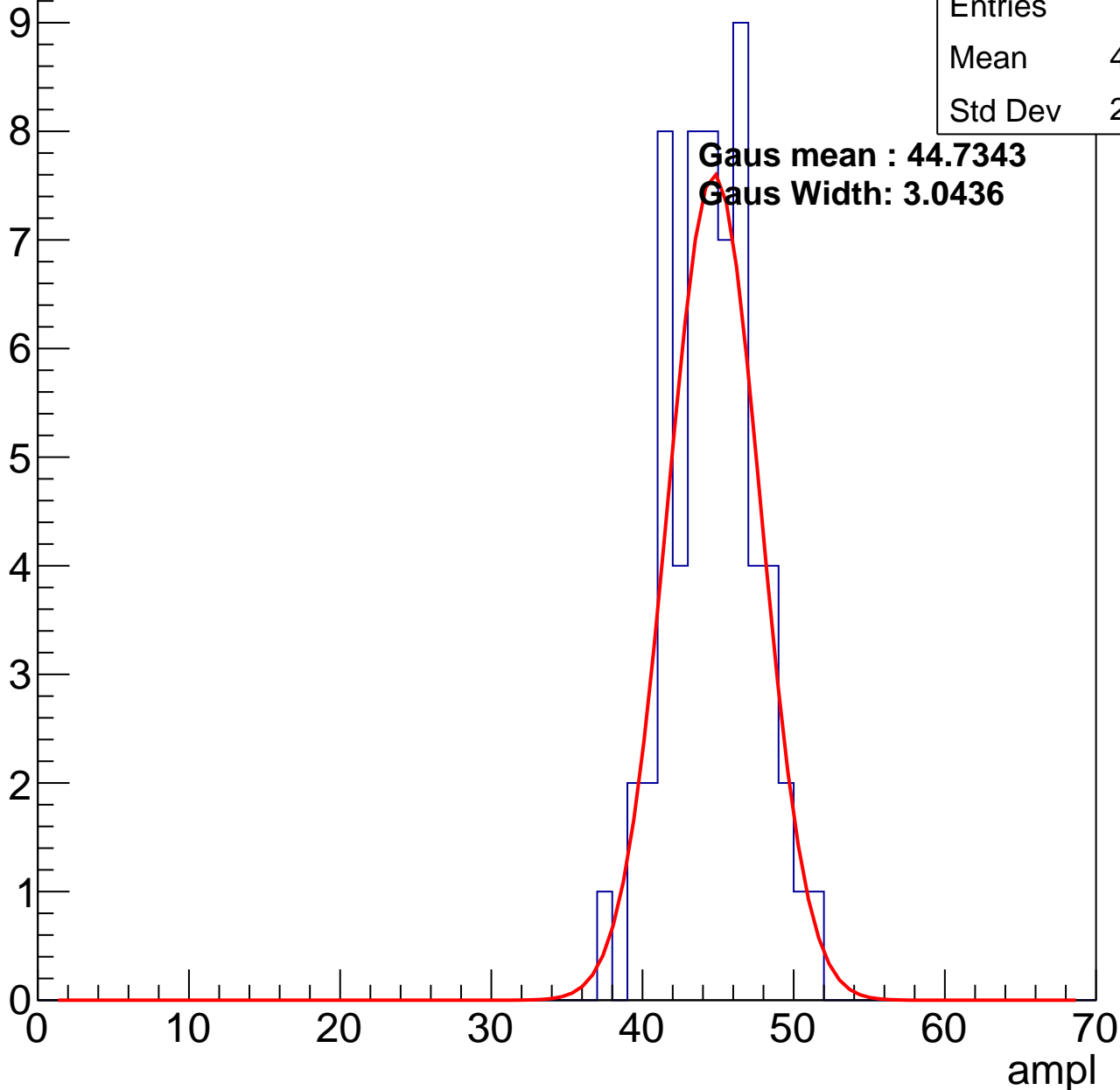
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	44.18
Std Dev	2.872

**Gaus mean : 44.7343**

**Gaus Width: 3.0436**

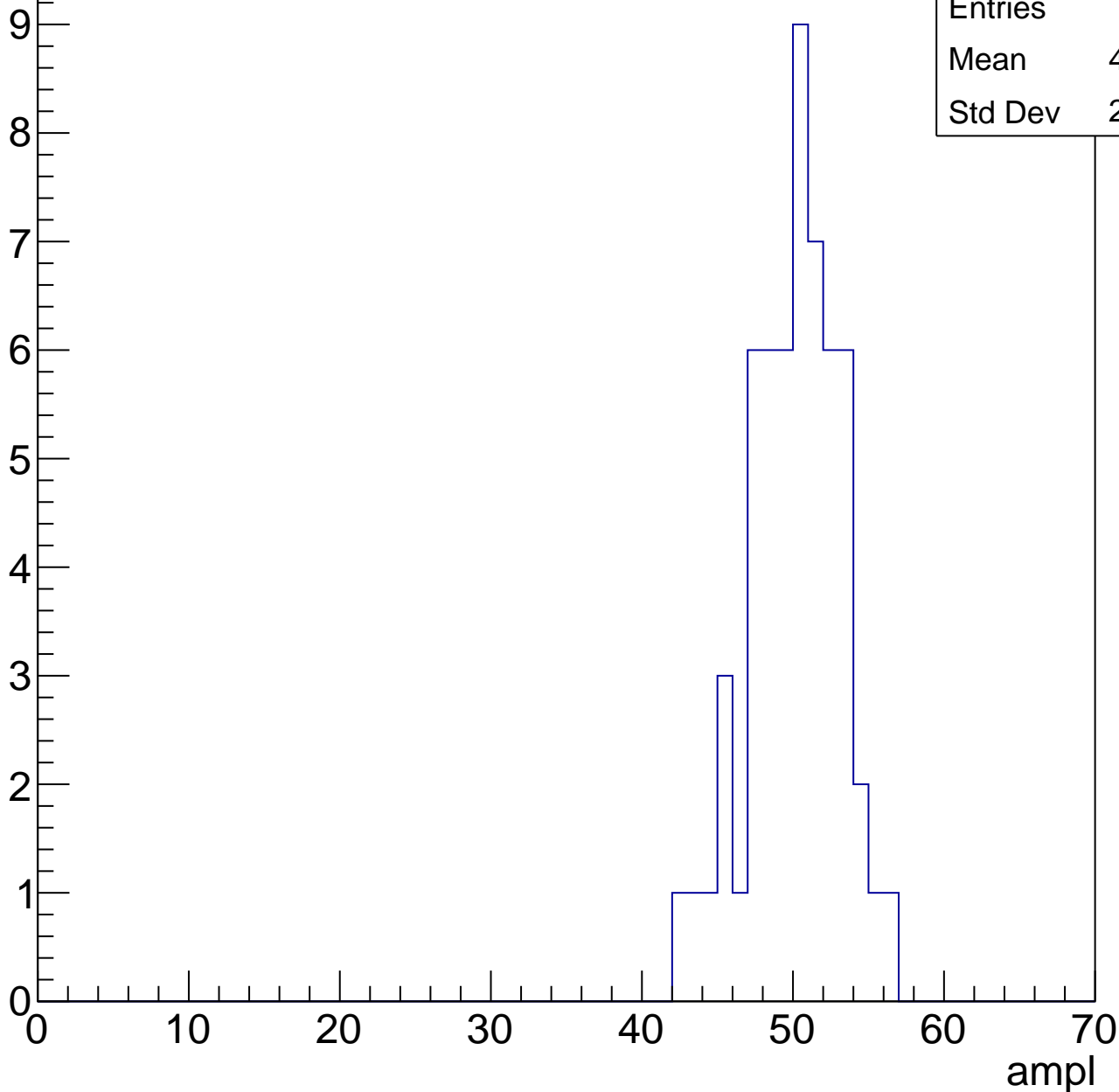


# B1L003S, U26-ch28, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	49.65
Std Dev	2.947

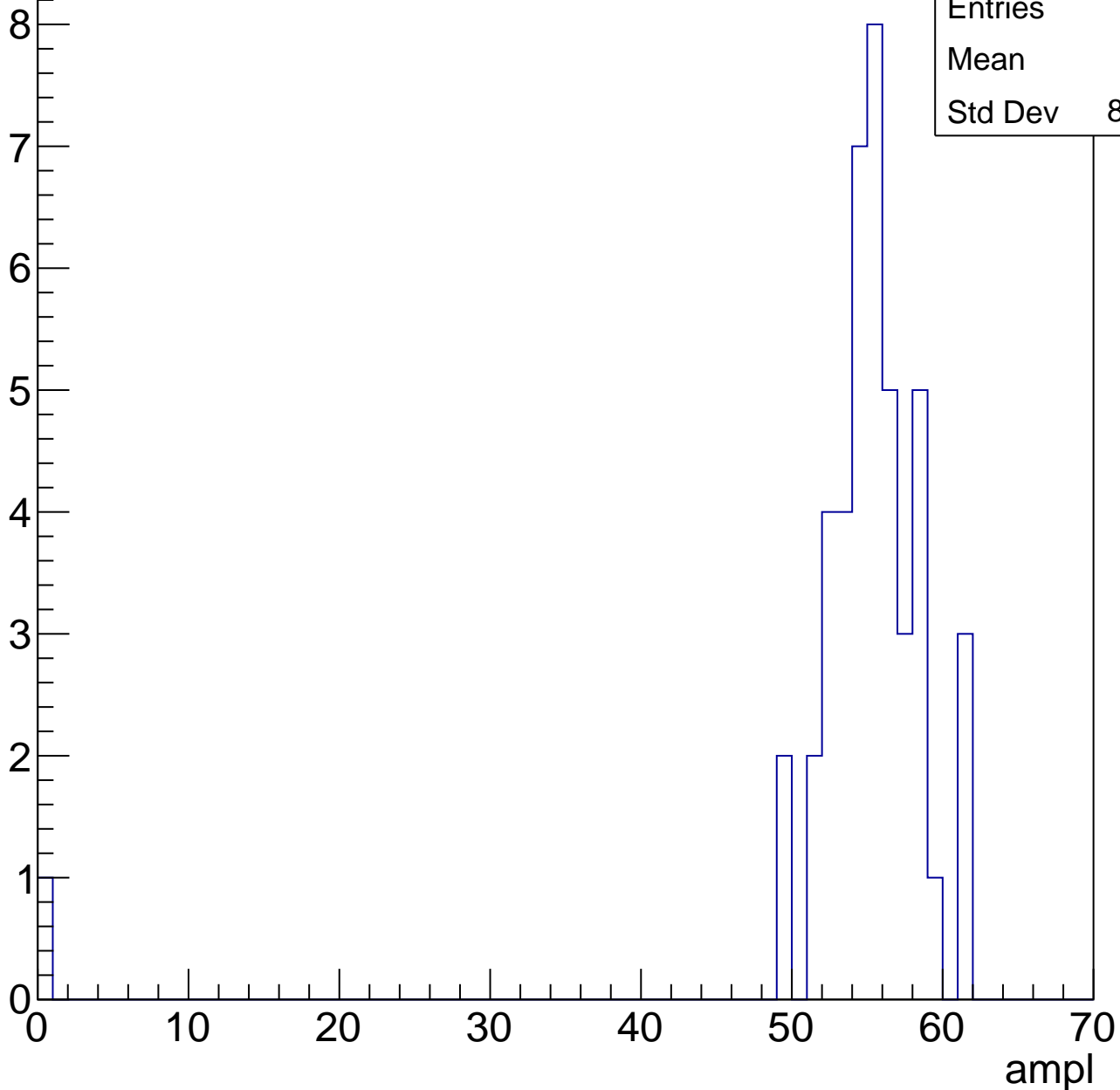


# B1L003S, U26-ch28, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	45
Mean	53.8
Std Dev	8.575

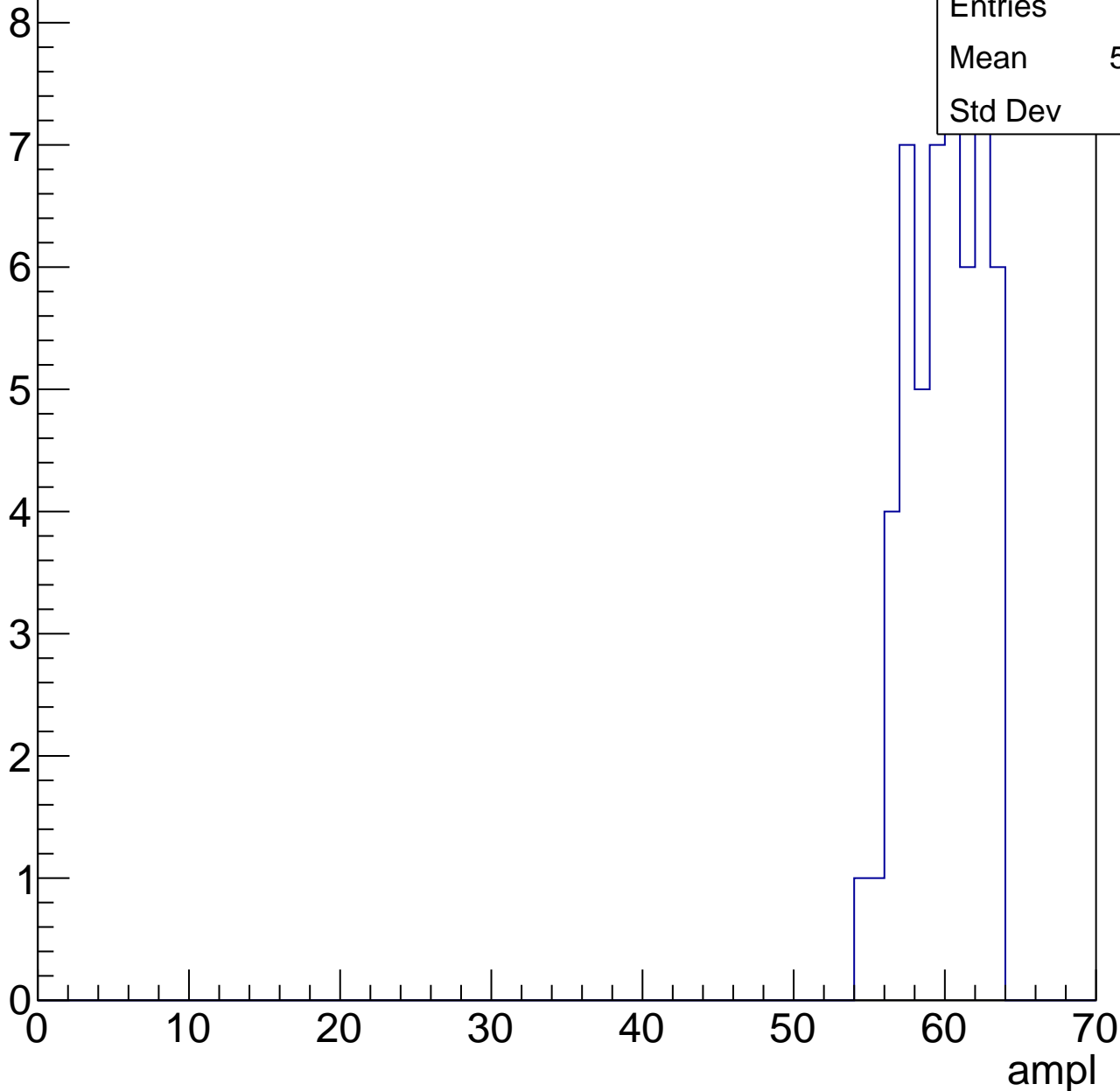


# B1L003S, U26-ch28, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

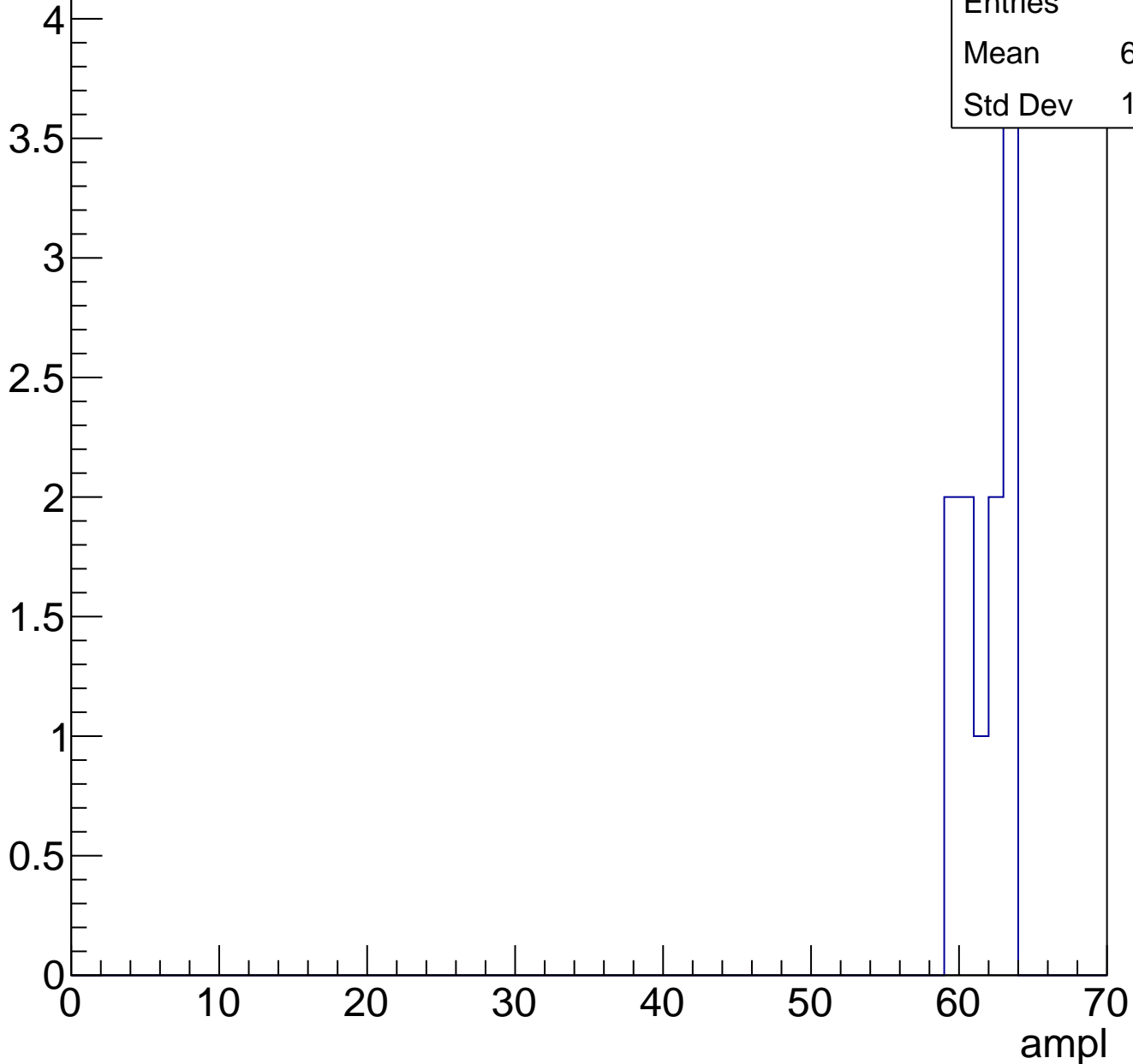
Entries	53
Mean	59.53
Std Dev	2.36



# B1L003S, U26-ch28, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch28, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U26-ch29, adc0

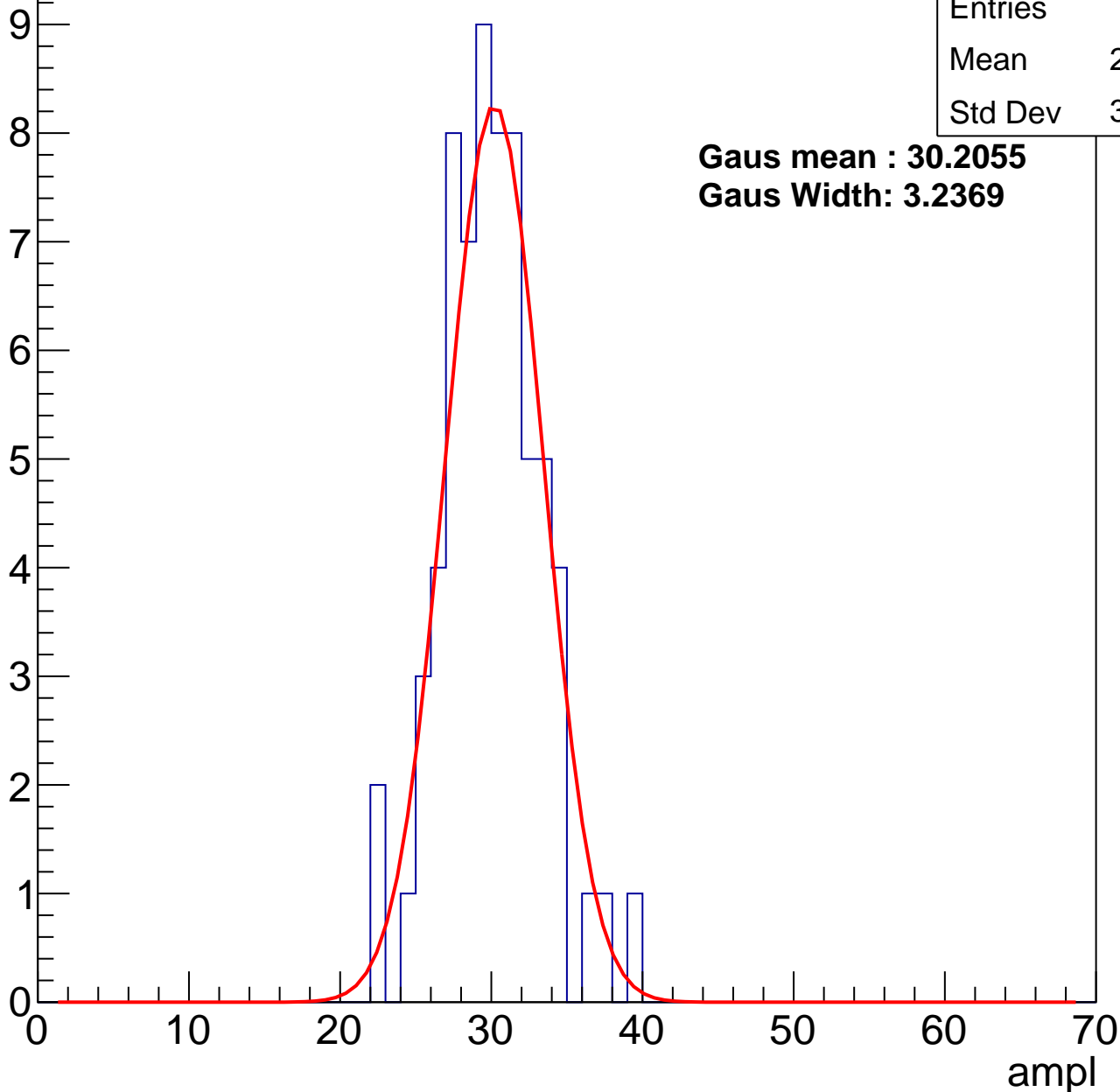
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	29.57
Std Dev	3.238

**Gaus mean : 30.2055**

**Gaus Width: 3.2369**



# B1L003S, U26-ch29, adc1

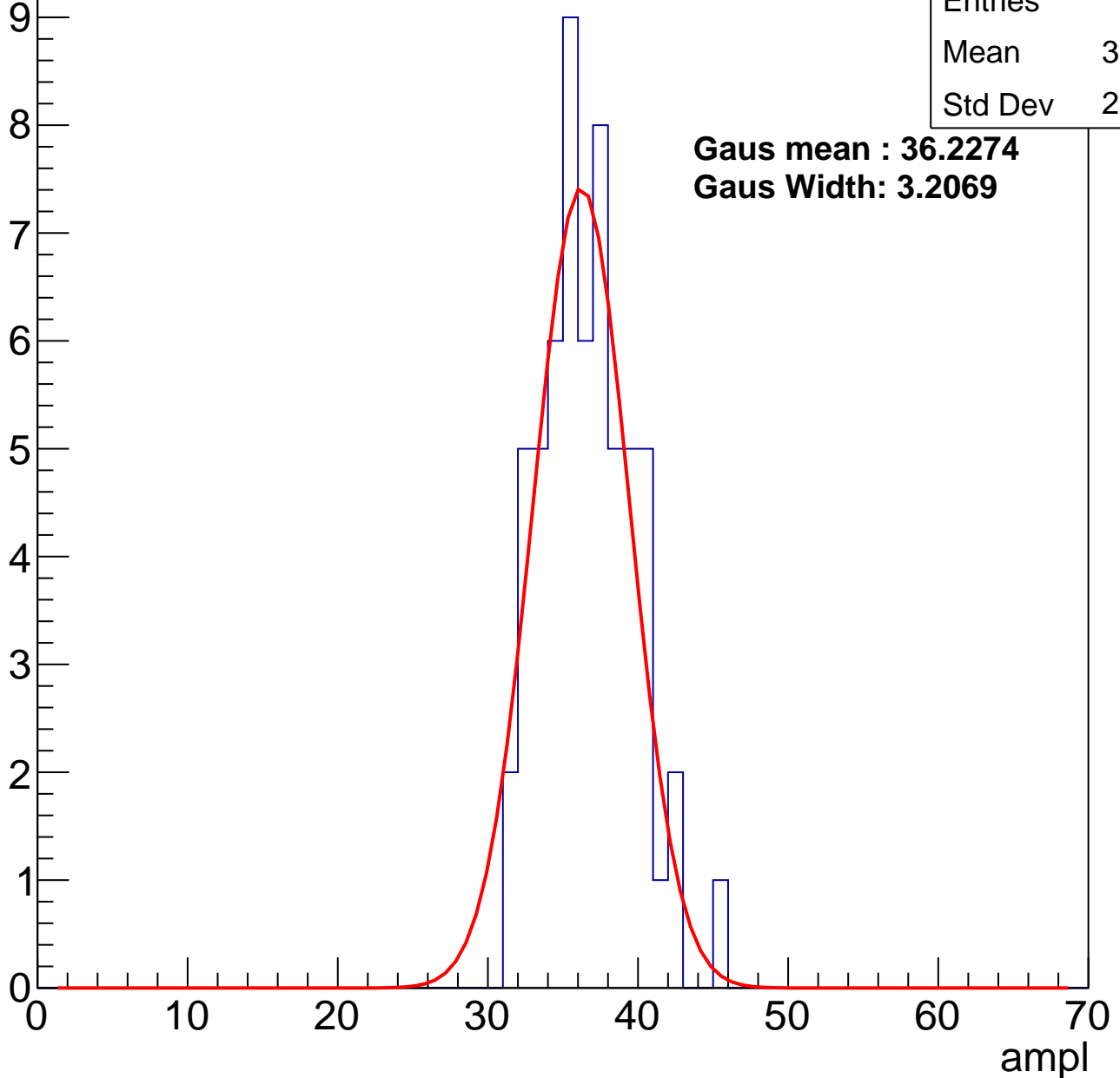
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	36.22
Std Dev	2.989

**Gaus mean : 36.2274**

**Gaus Width: 3.2069**



# B1L003S, U26-ch29, adc2

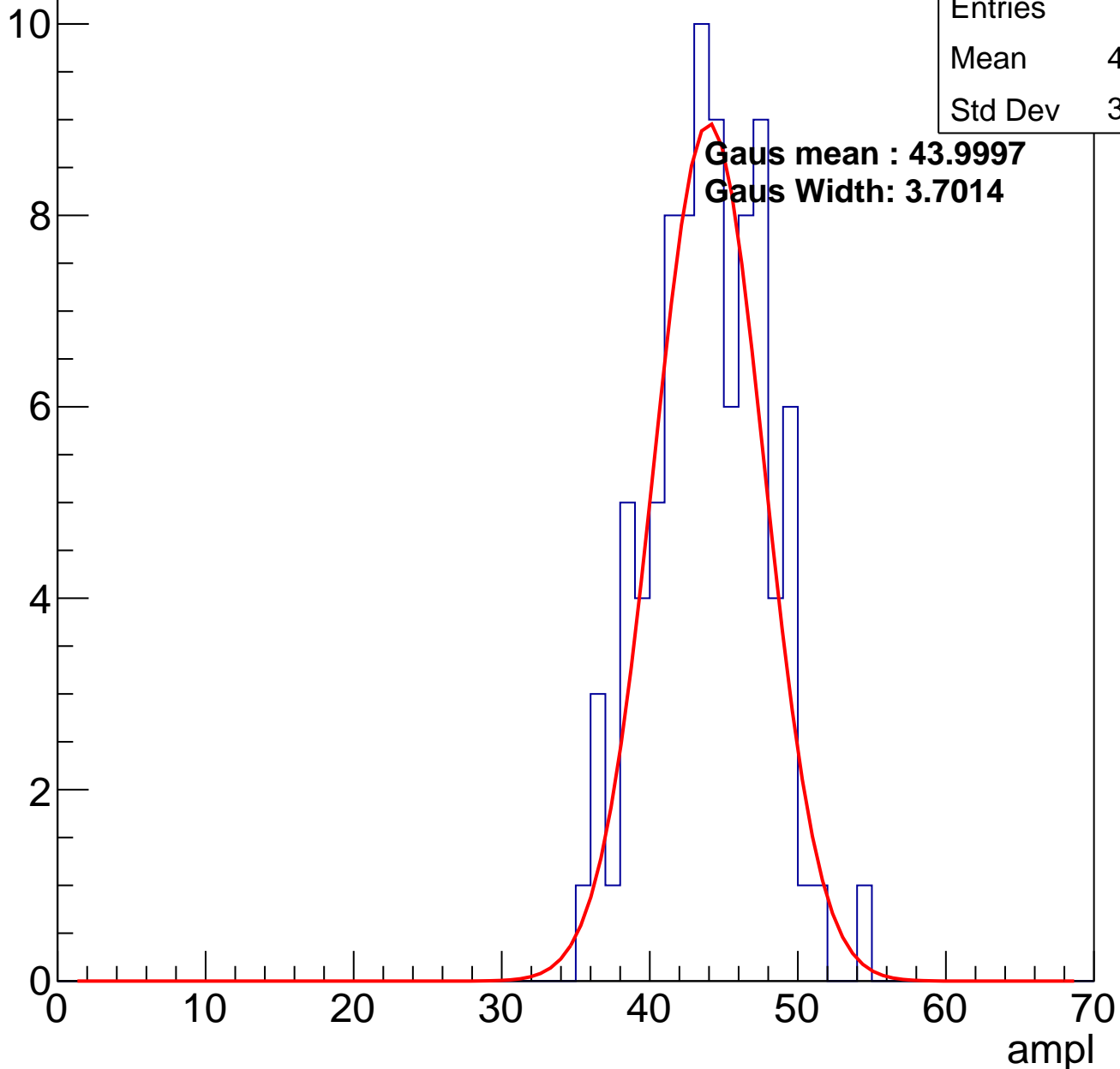
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	90
Mean	43.53
Std Dev	3.792

**Gaus mean : 43.9997**

**Gaus Width: 3.7014**

Entry

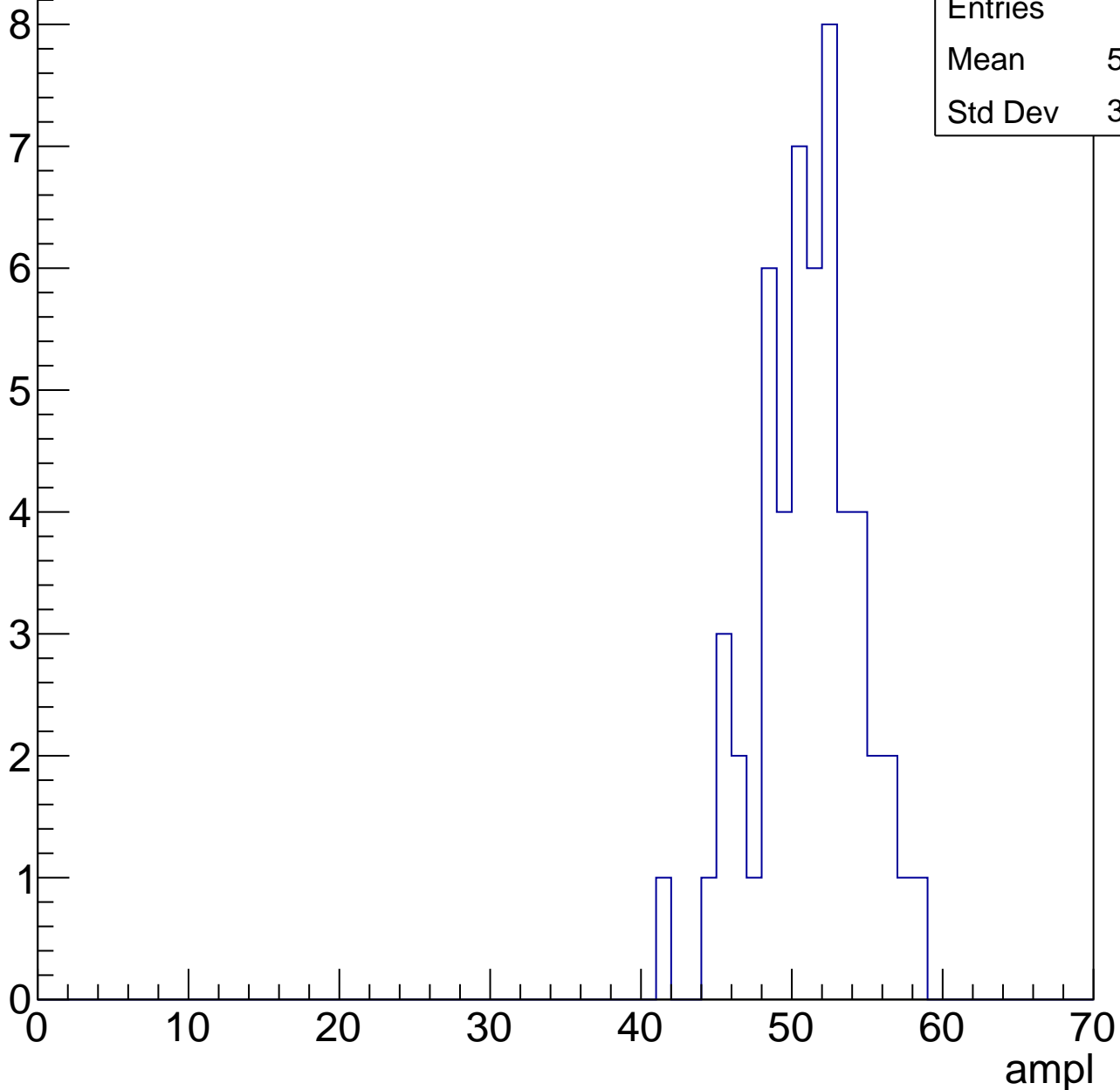


# B1L003S, U26-ch29, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	50.57
Std Dev	3.412

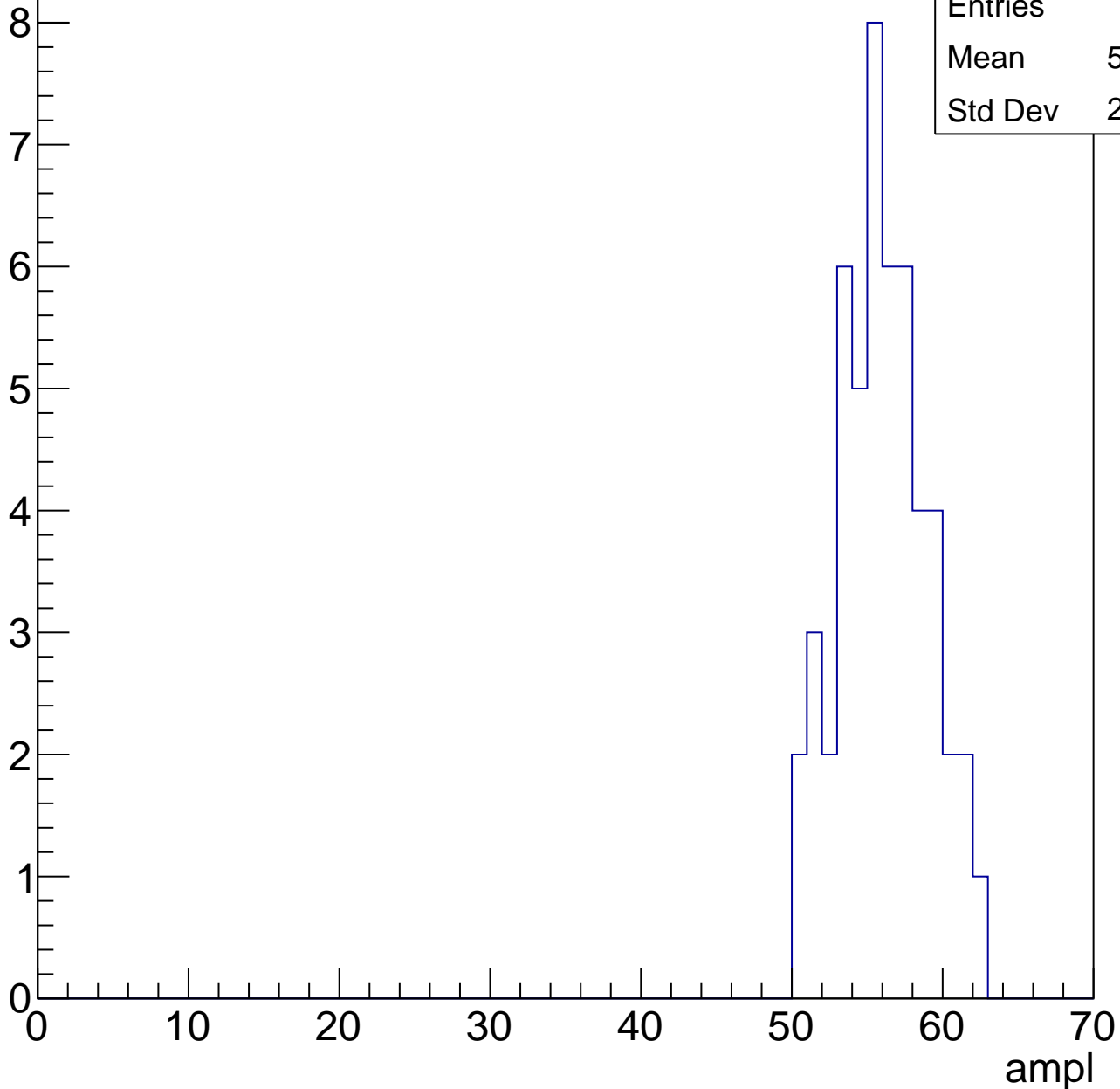


# B1L003S, U26-ch29, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	51
Mean	55.59
Std Dev	2.898

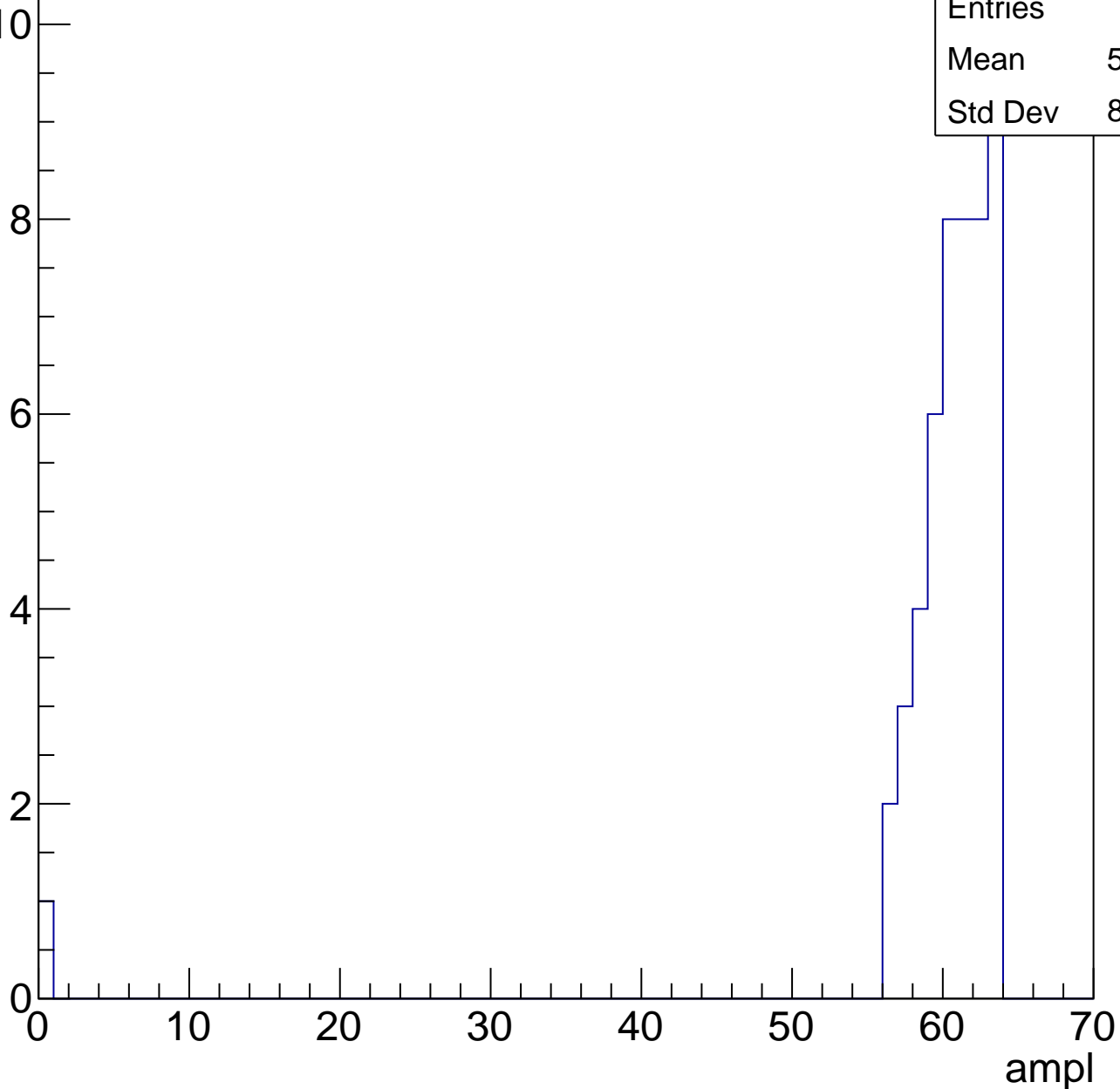


# B1L003S, U26-ch29, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	50
Mean	59.26
Std Dev	8.699



# B1L003S, U26-ch29, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

2

Mean

60

Std Dev

2



# B1L003S, U26-ch29, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U26-ch30, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	75
Mean	28.96
Std Dev	3.312

**Gaus mean : 29.6633**

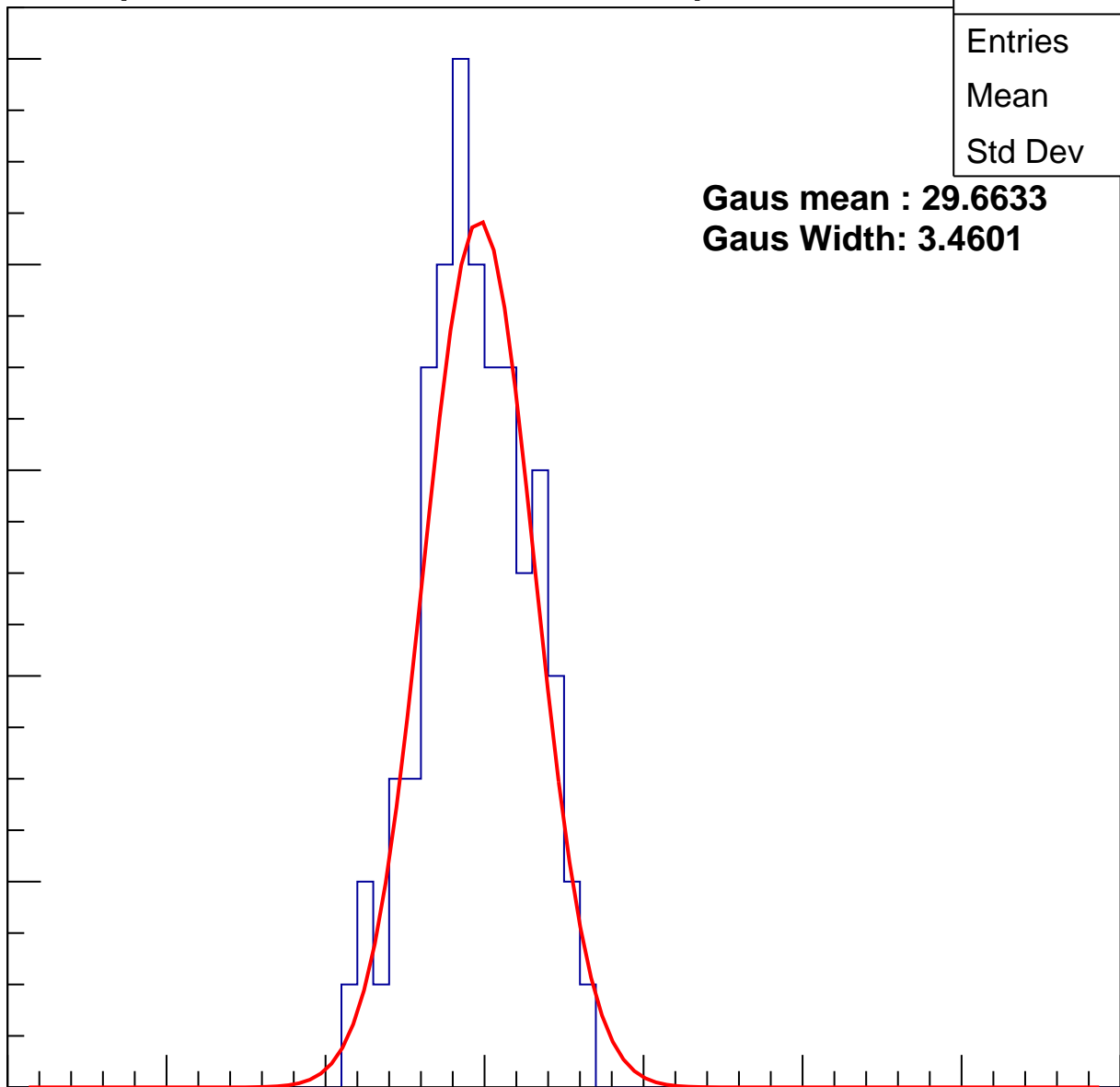
**Gaus Width: 3.4601**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U26-ch30, adc1

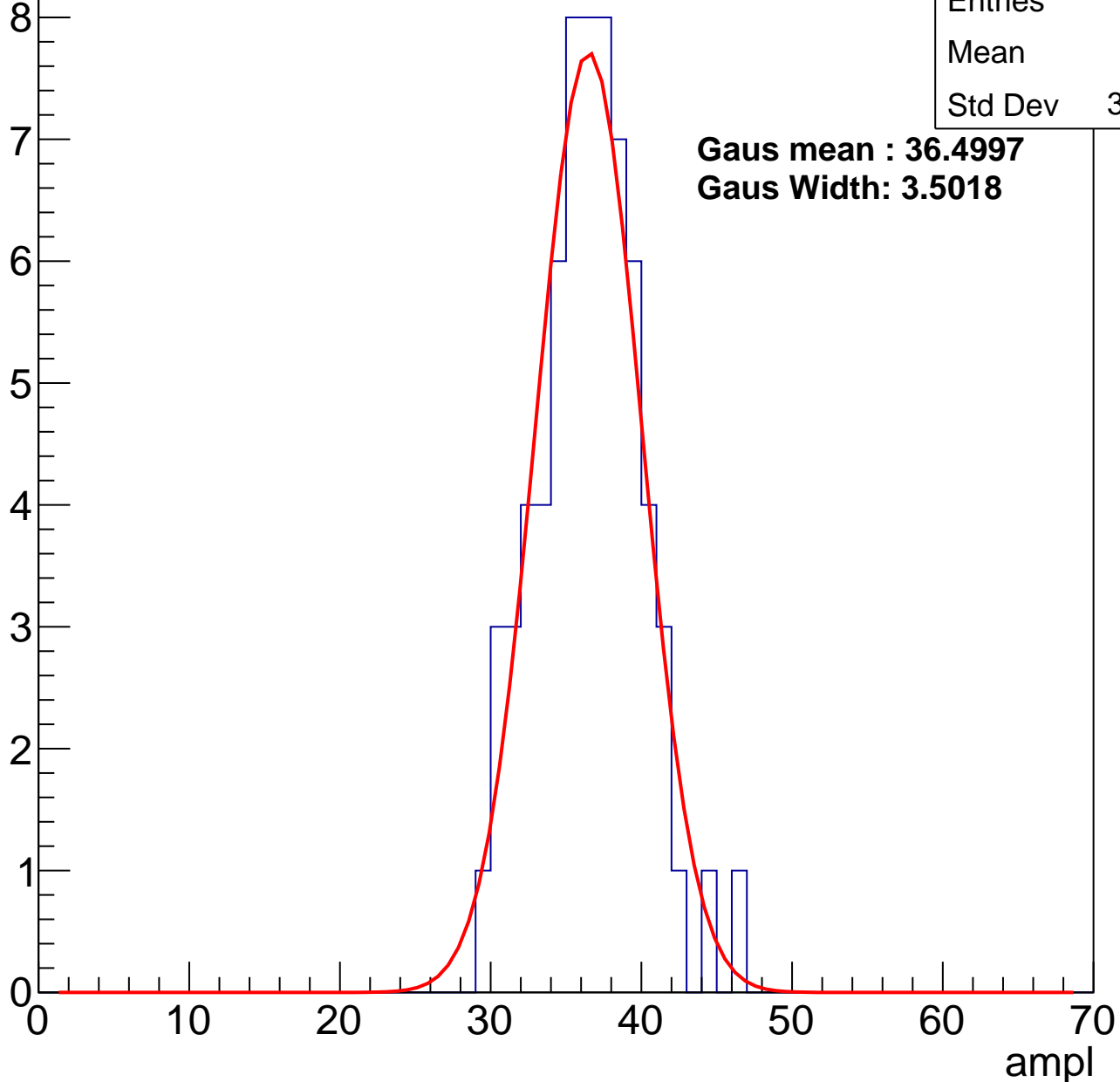
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	36.1
Std Dev	3.413

**Gaus mean : 36.4997**

**Gaus Width: 3.5018**



# B1L003S, U26-ch30, adc2

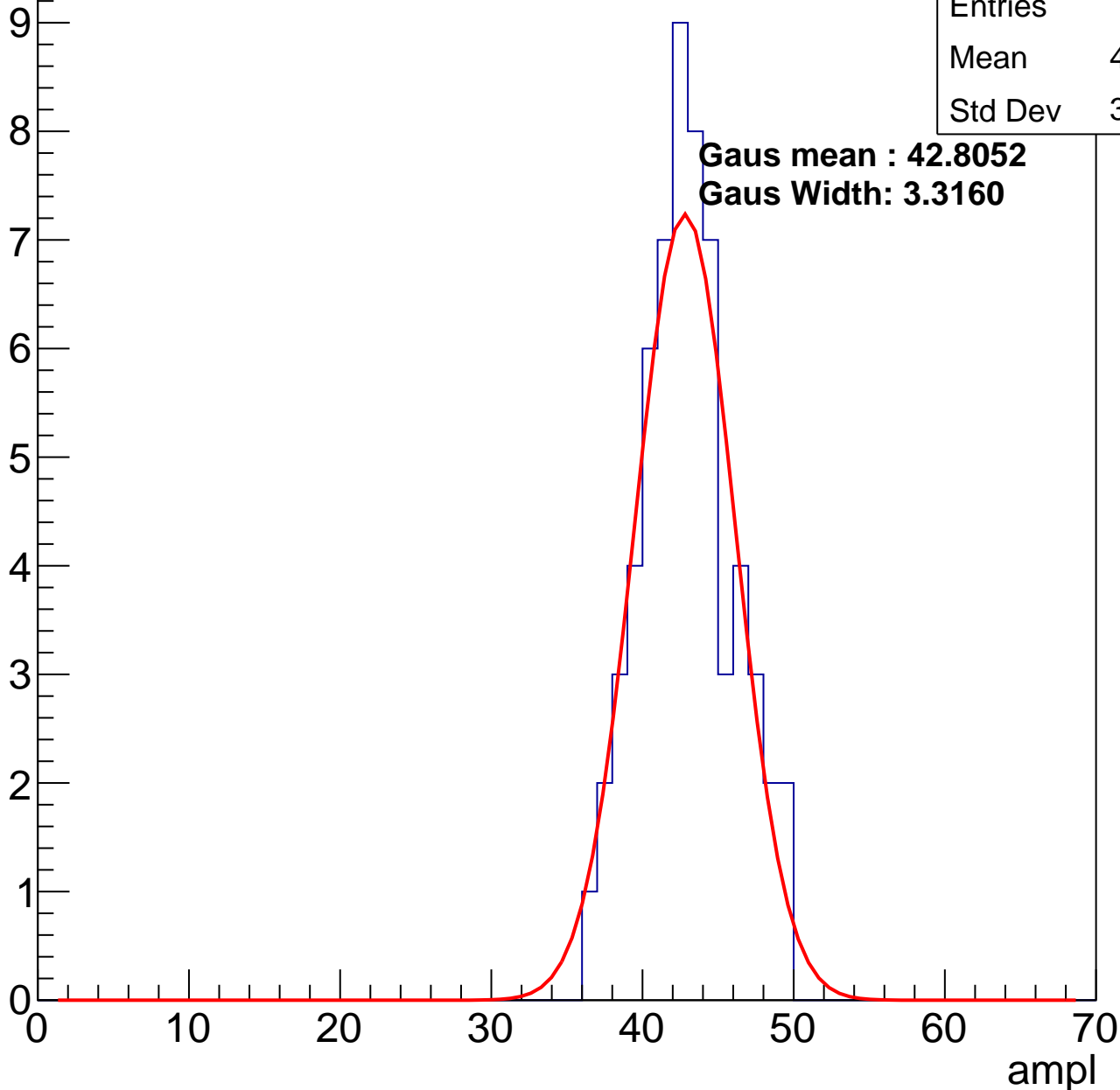
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	42.48
Std Dev	3.028

**Gaus mean : 42.8052**

**Gaus Width: 3.3160**

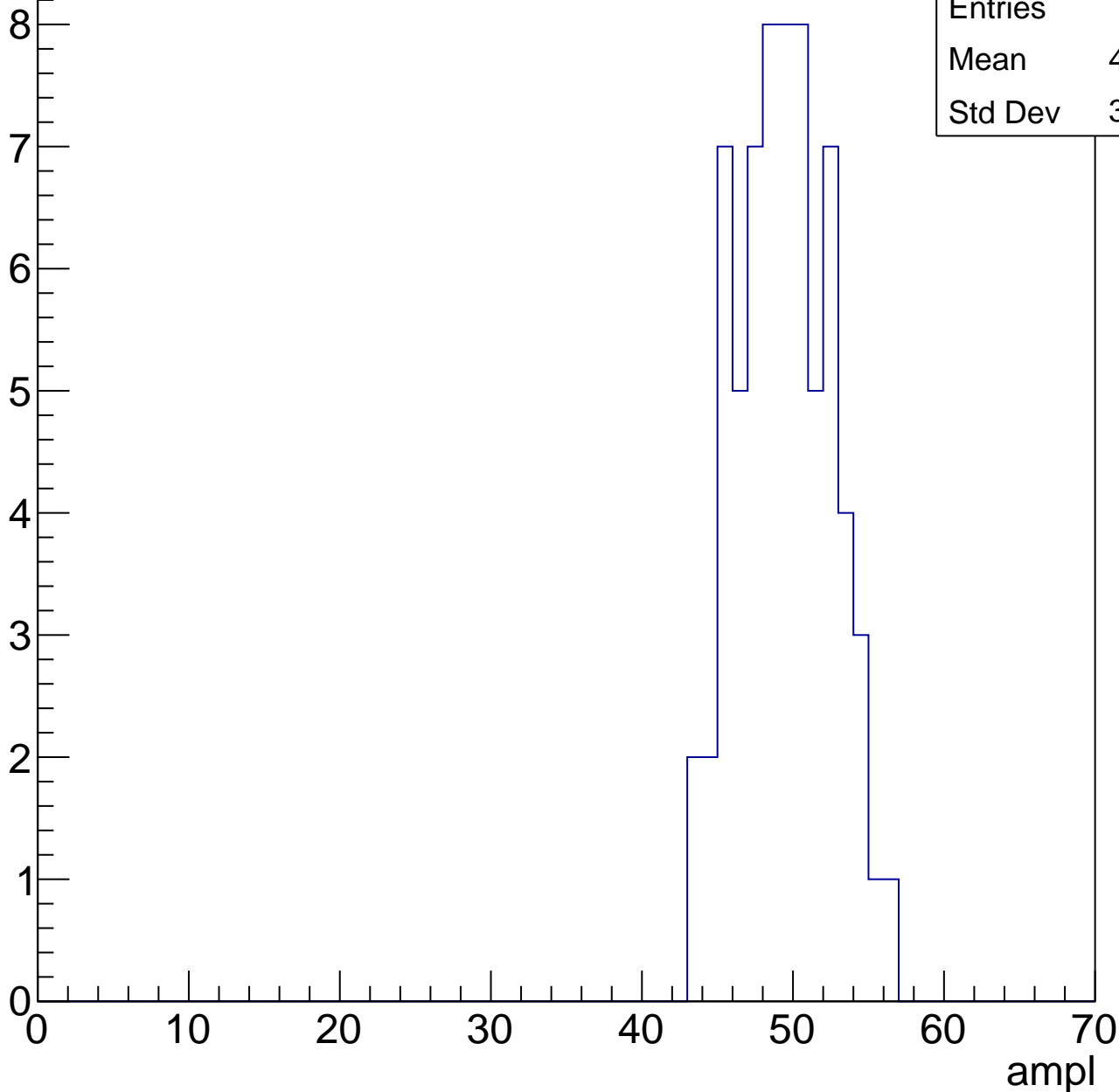


# B1L003S, U26-ch30, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	48.94
Std Dev	3.043

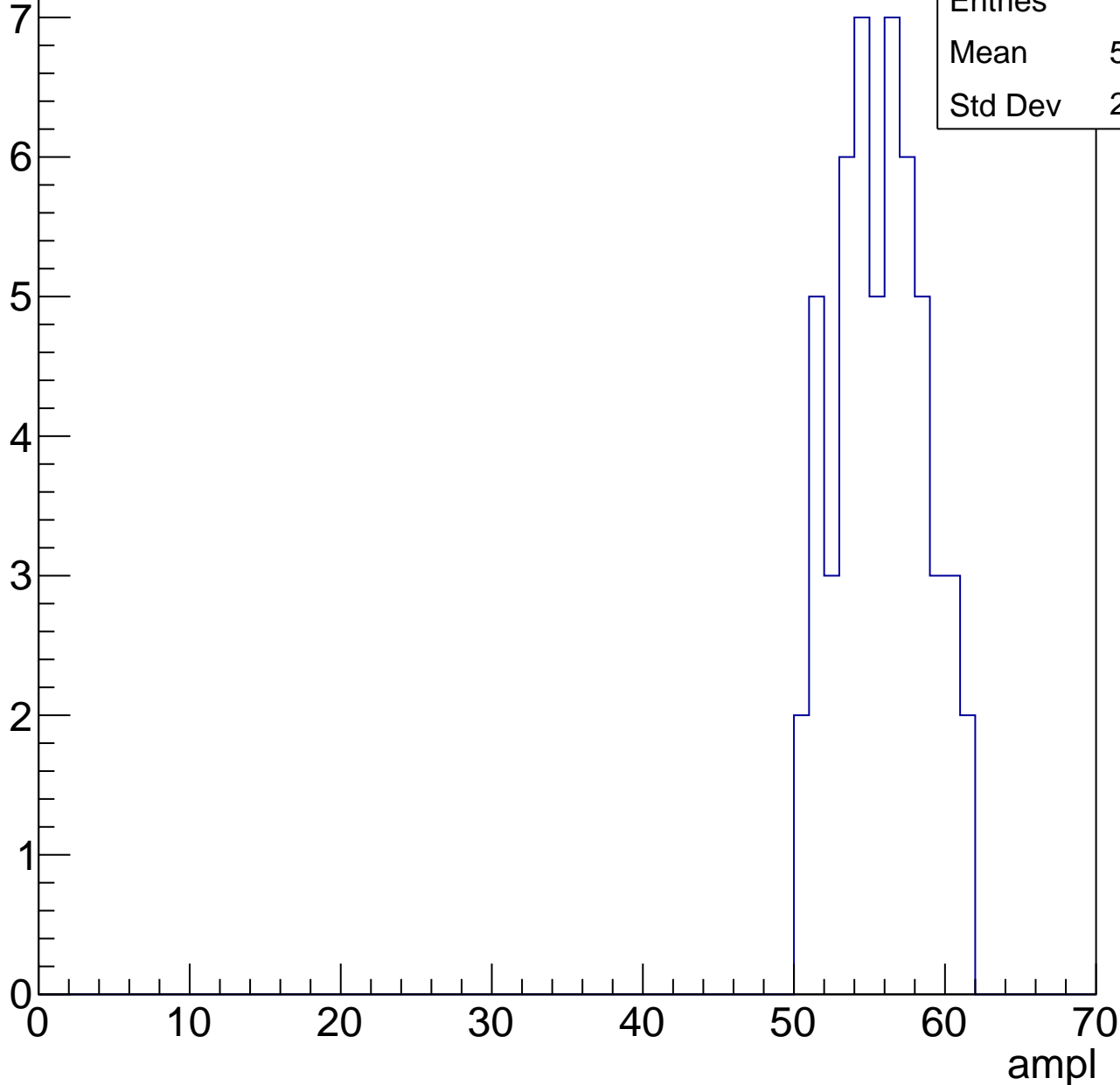


# B1L003S, U26-ch30, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	54
Mean	55.28
Std Dev	2.902

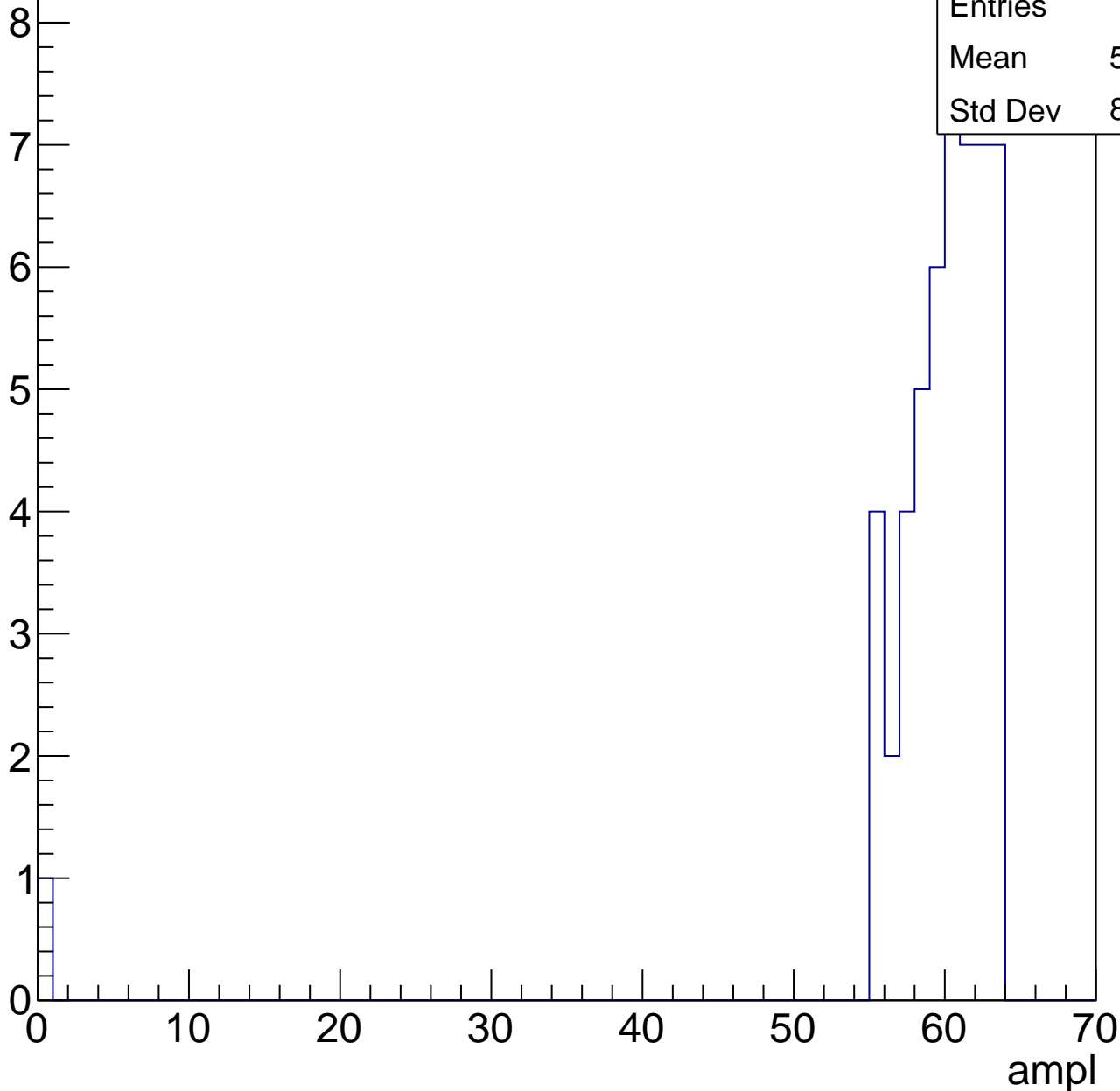


# B1L003S, U26-ch30, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

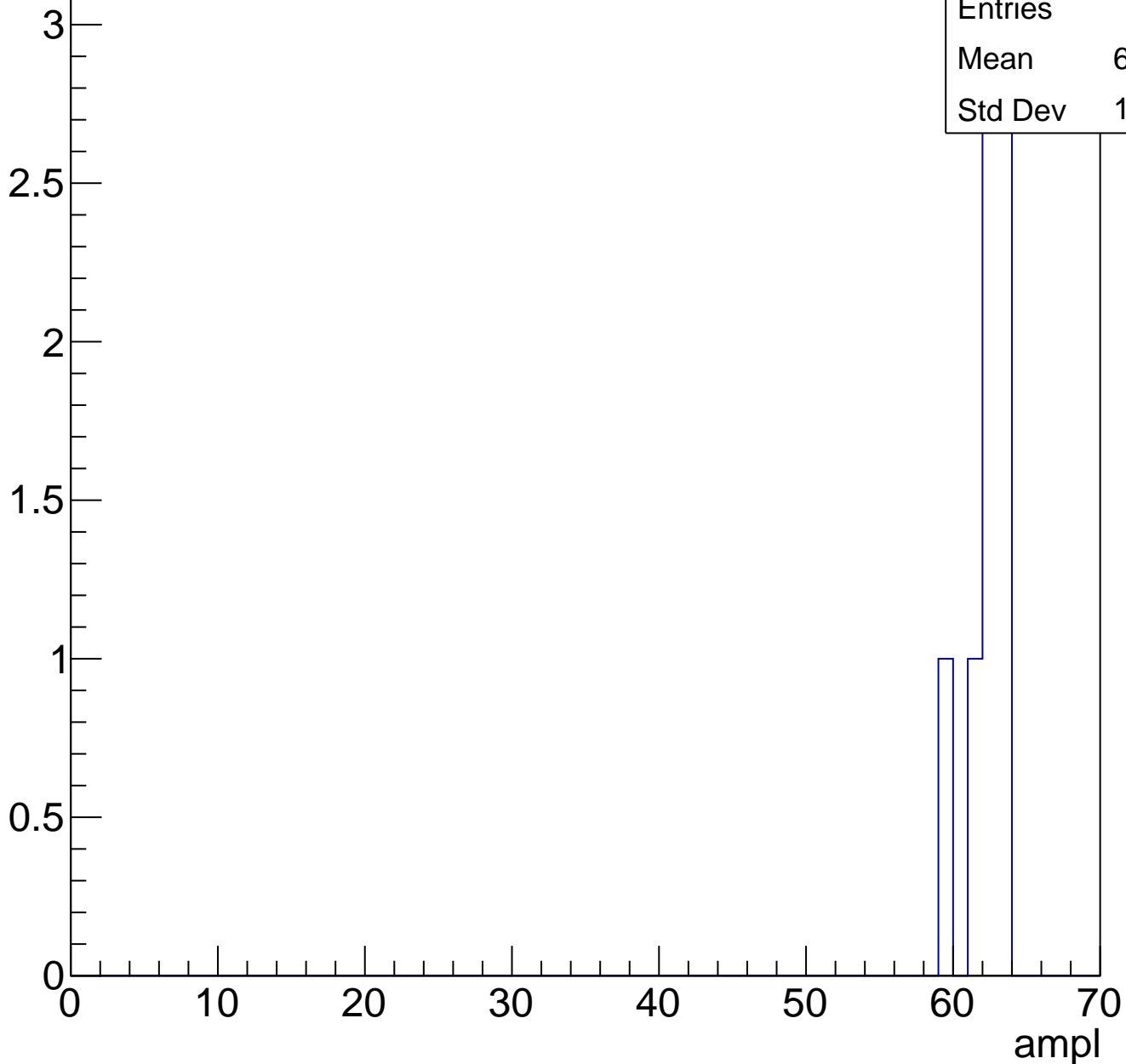
Entries	51
Mean	58.55
Std Dev	8.614



# B1L003S, U26-ch30, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch30, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U26-ch31, adc0

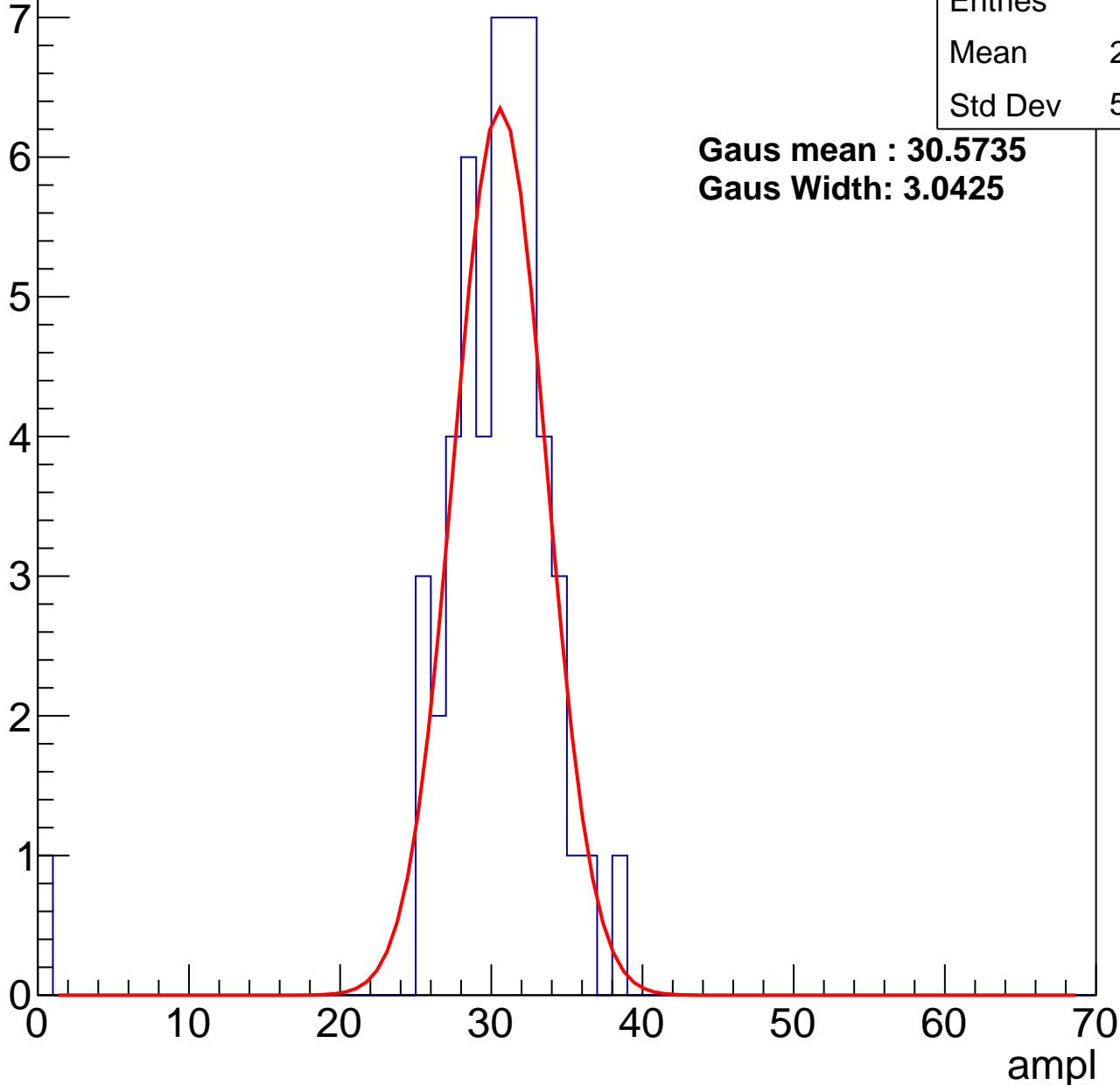
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	51
Mean	29.67
Std Dev	5.067

**Gaus mean : 30.5735**

**Gaus Width: 3.0425**



# B1L003S, U26-ch31, adc1

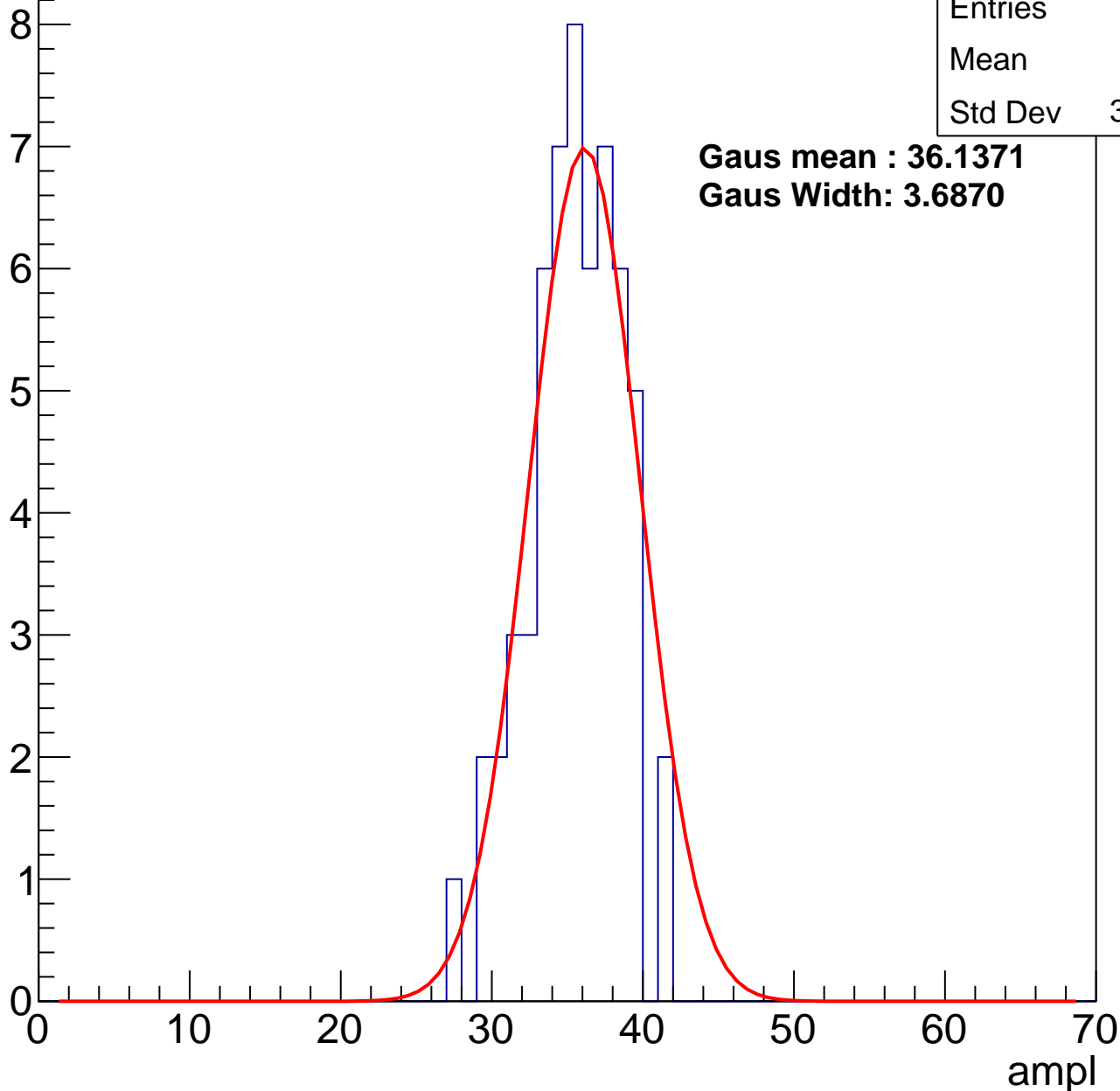
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	35
Std Dev	3.029

**Gaus mean : 36.1371**

**Gaus Width: 3.6870**



# B1L003S, U26-ch31, adc2

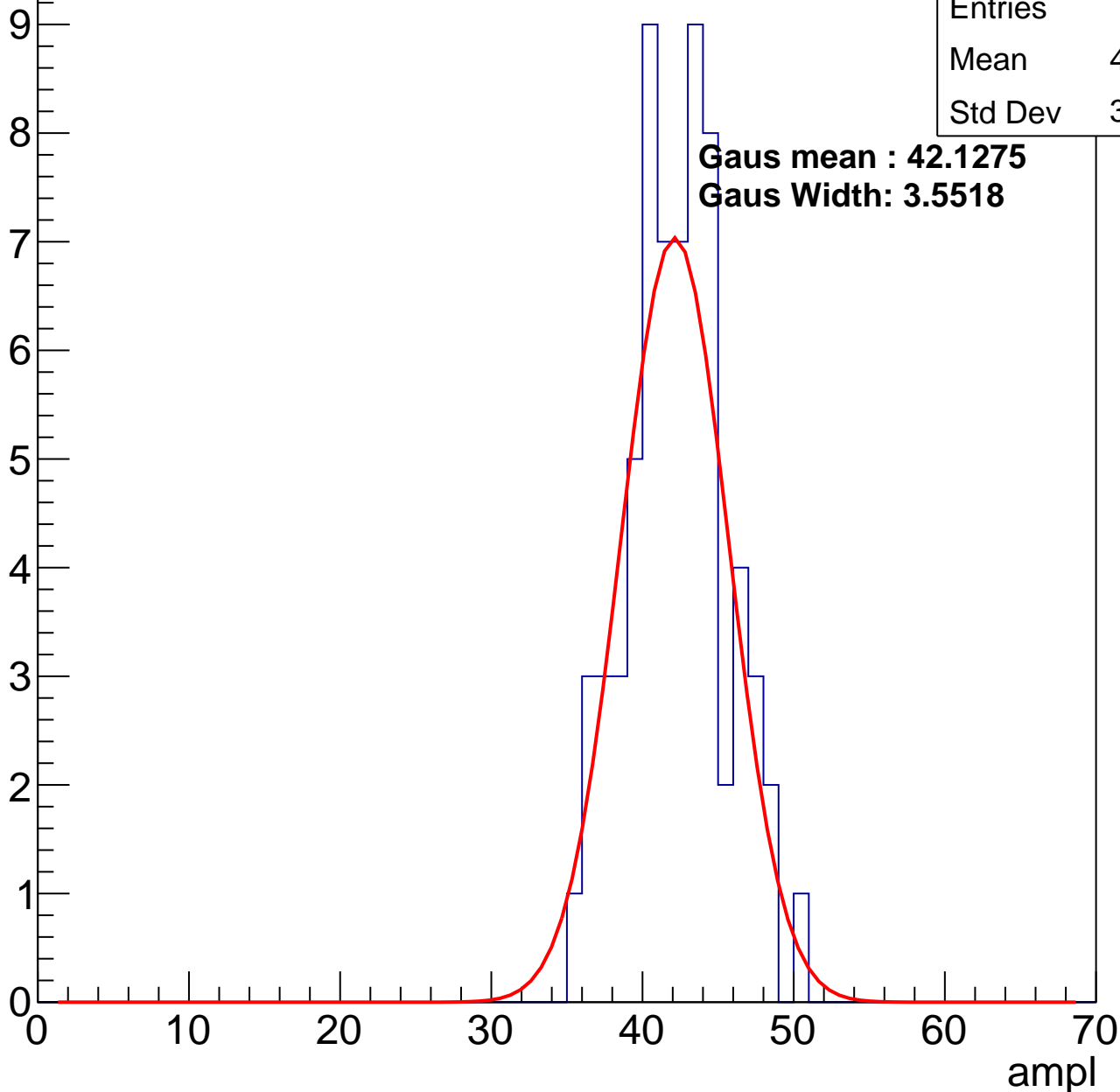
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	41.85
Std Dev	3.233

**Gaus mean : 42.1275**

**Gaus Width: 3.5518**

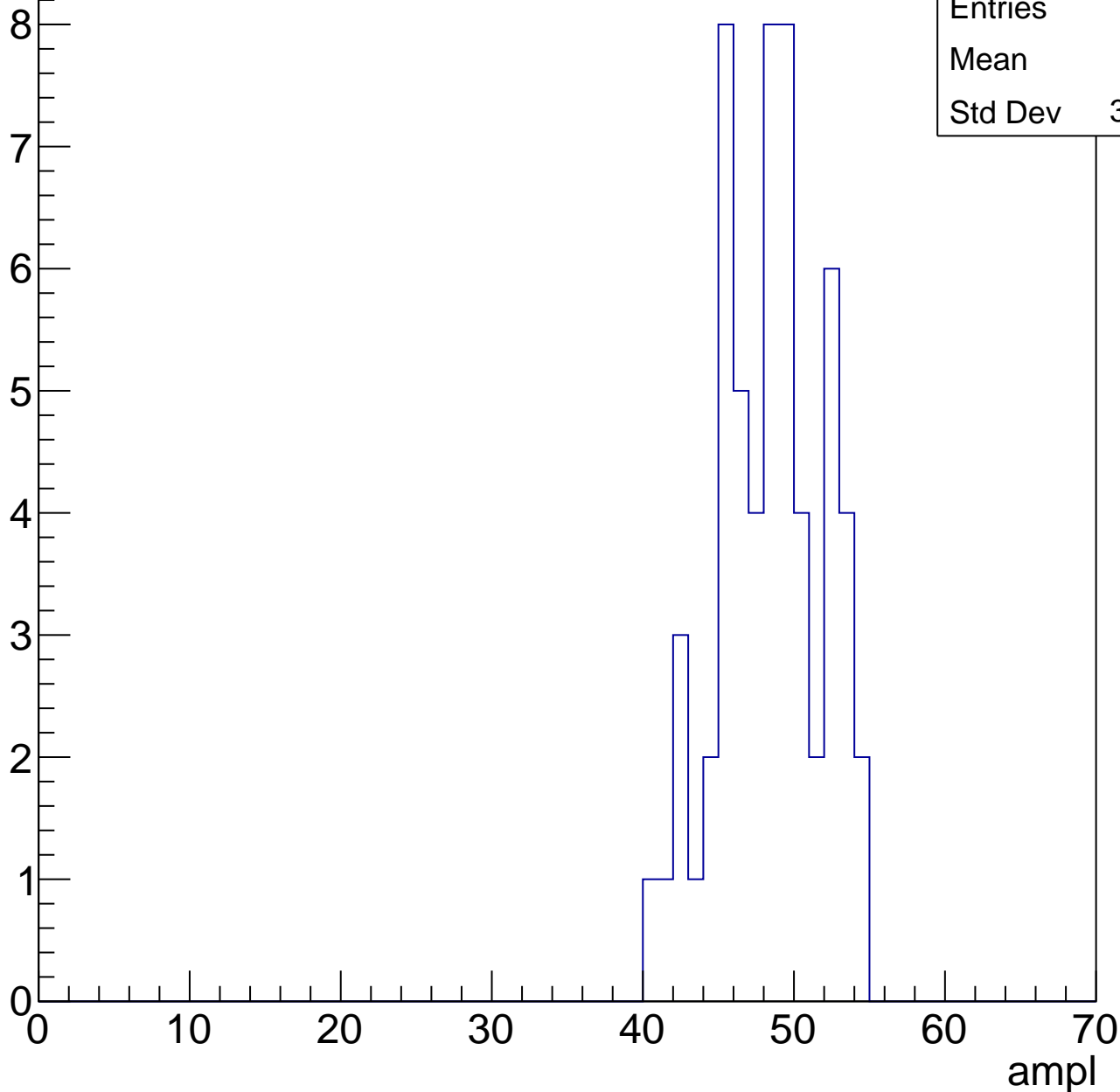


# B1L003S, U26-ch31, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	47.9
Std Dev	3.403

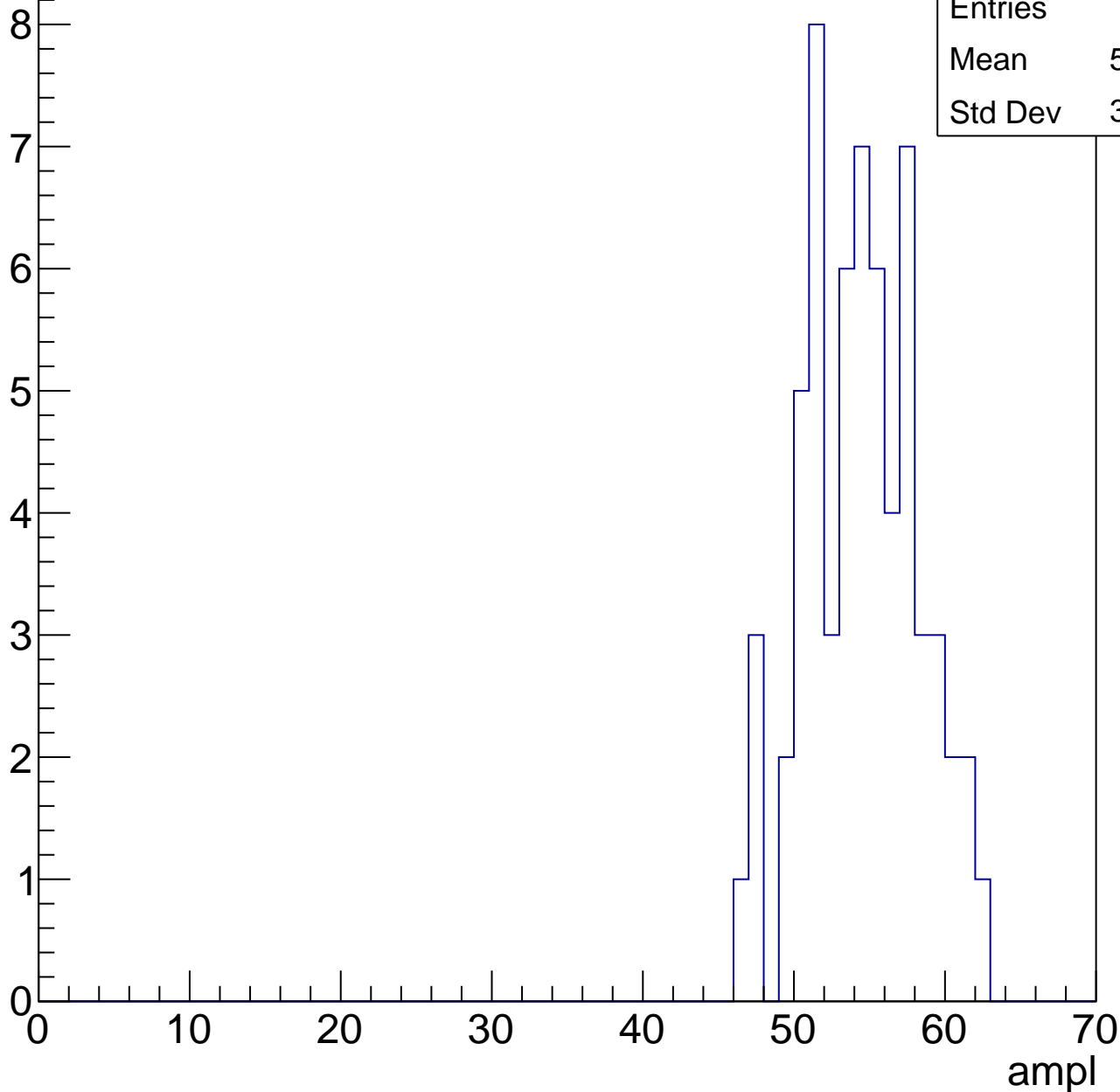


# B1L003S, U26-ch31, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

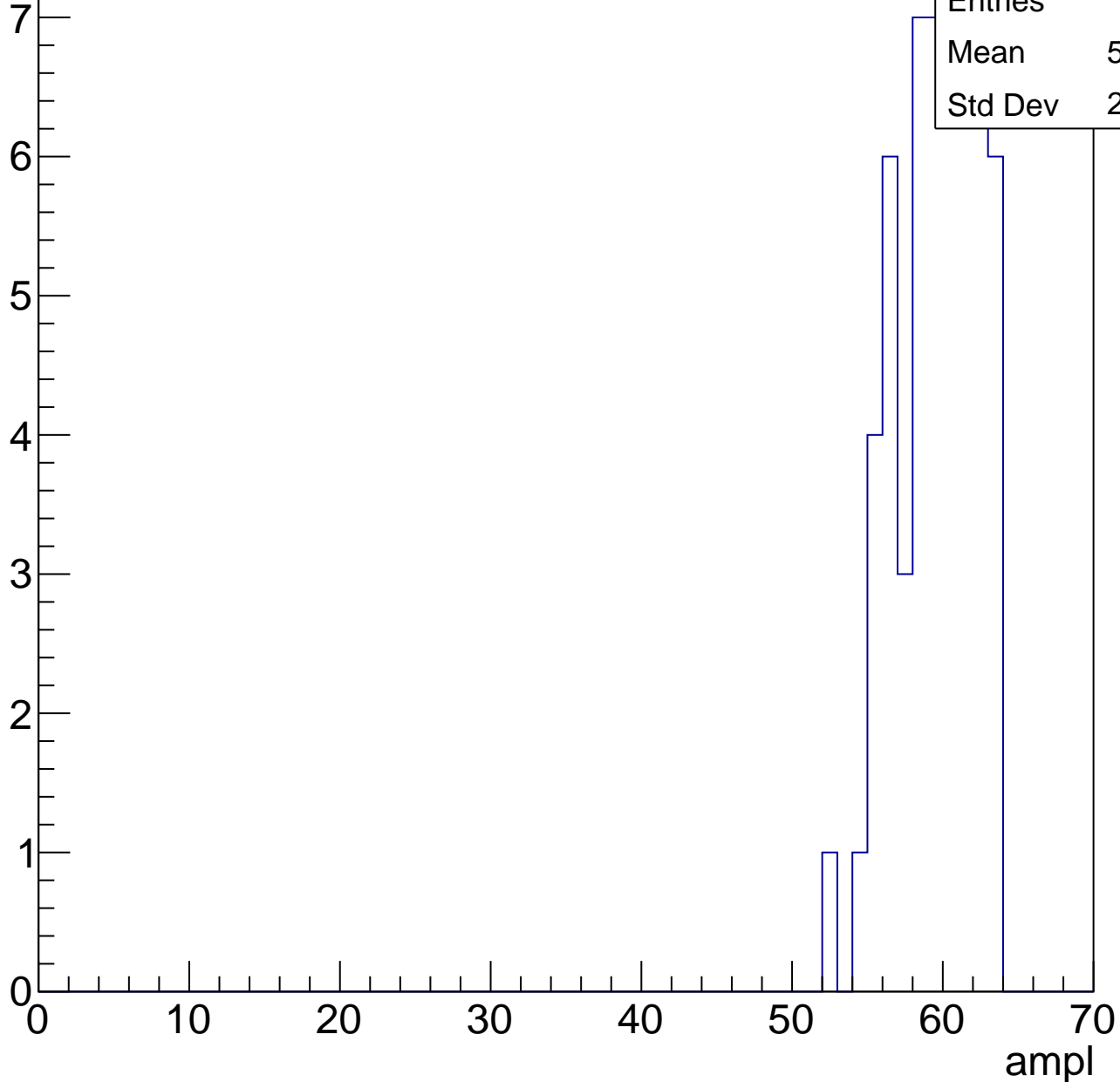
Entries	63
Mean	54.02
Std Dev	3.722



# B1L003S, U26-ch31, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

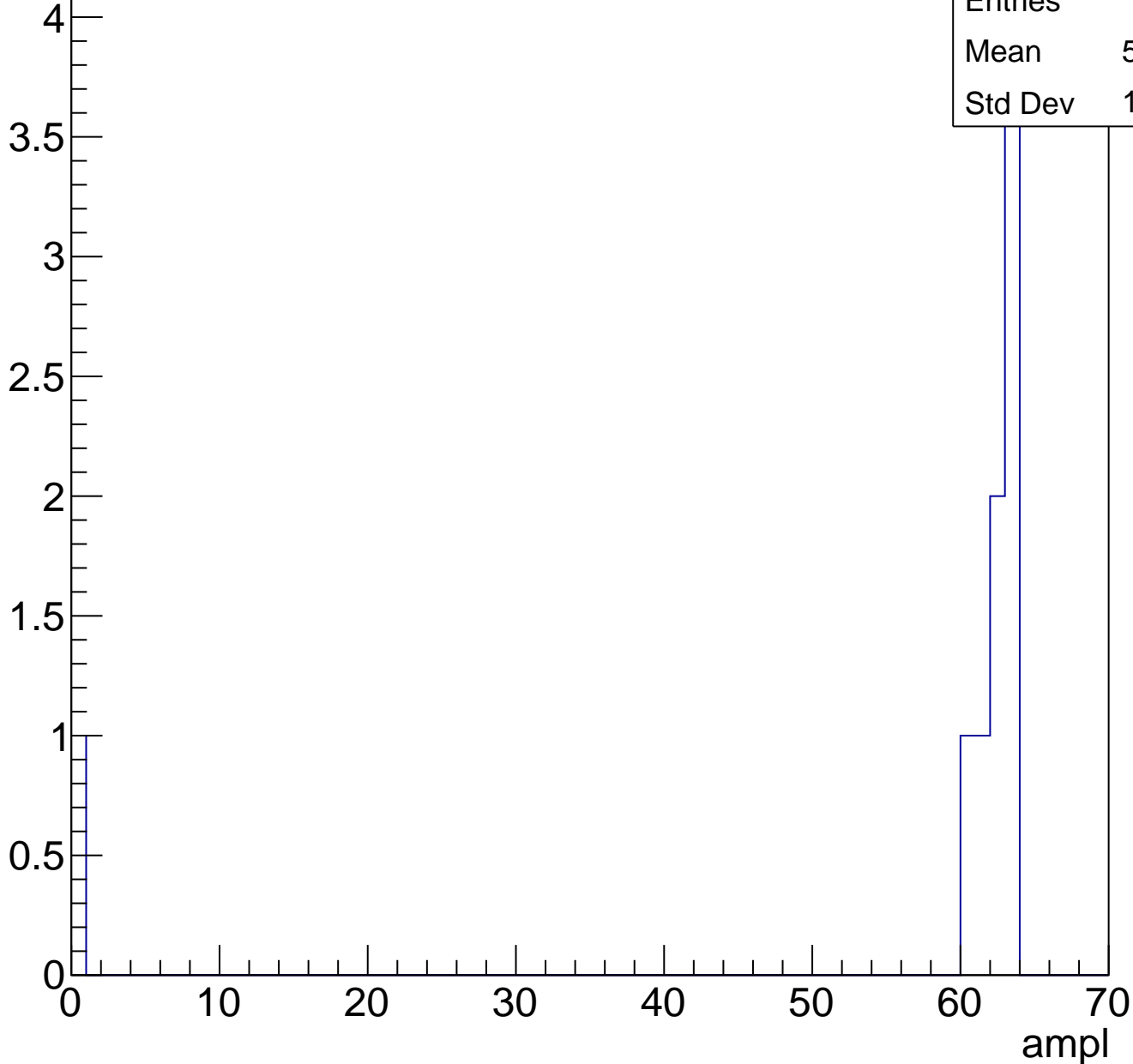
Entry



# B1L003S, U26-ch31, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

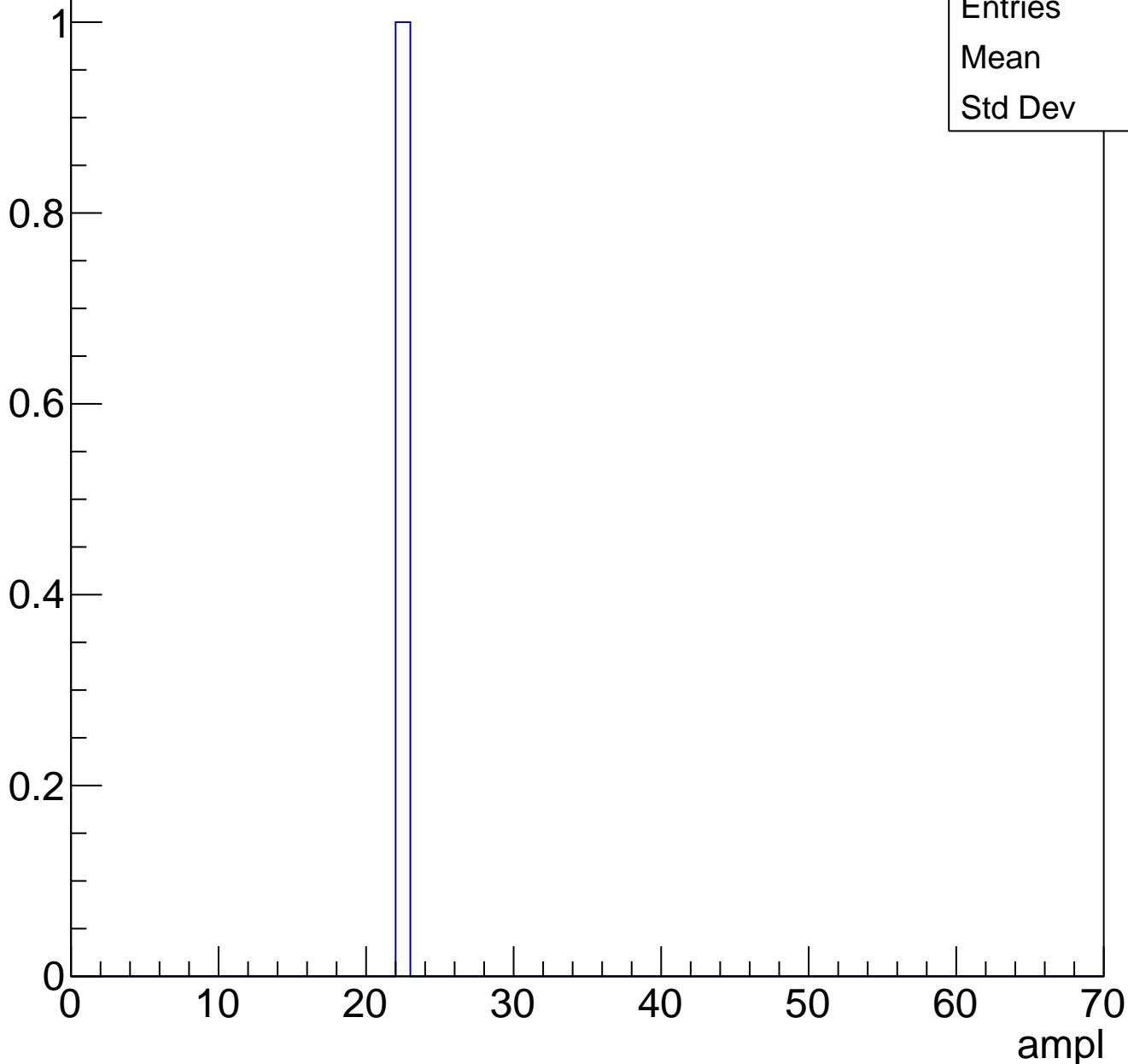




# B1L003S, U26-ch31, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U26-ch32, adc0

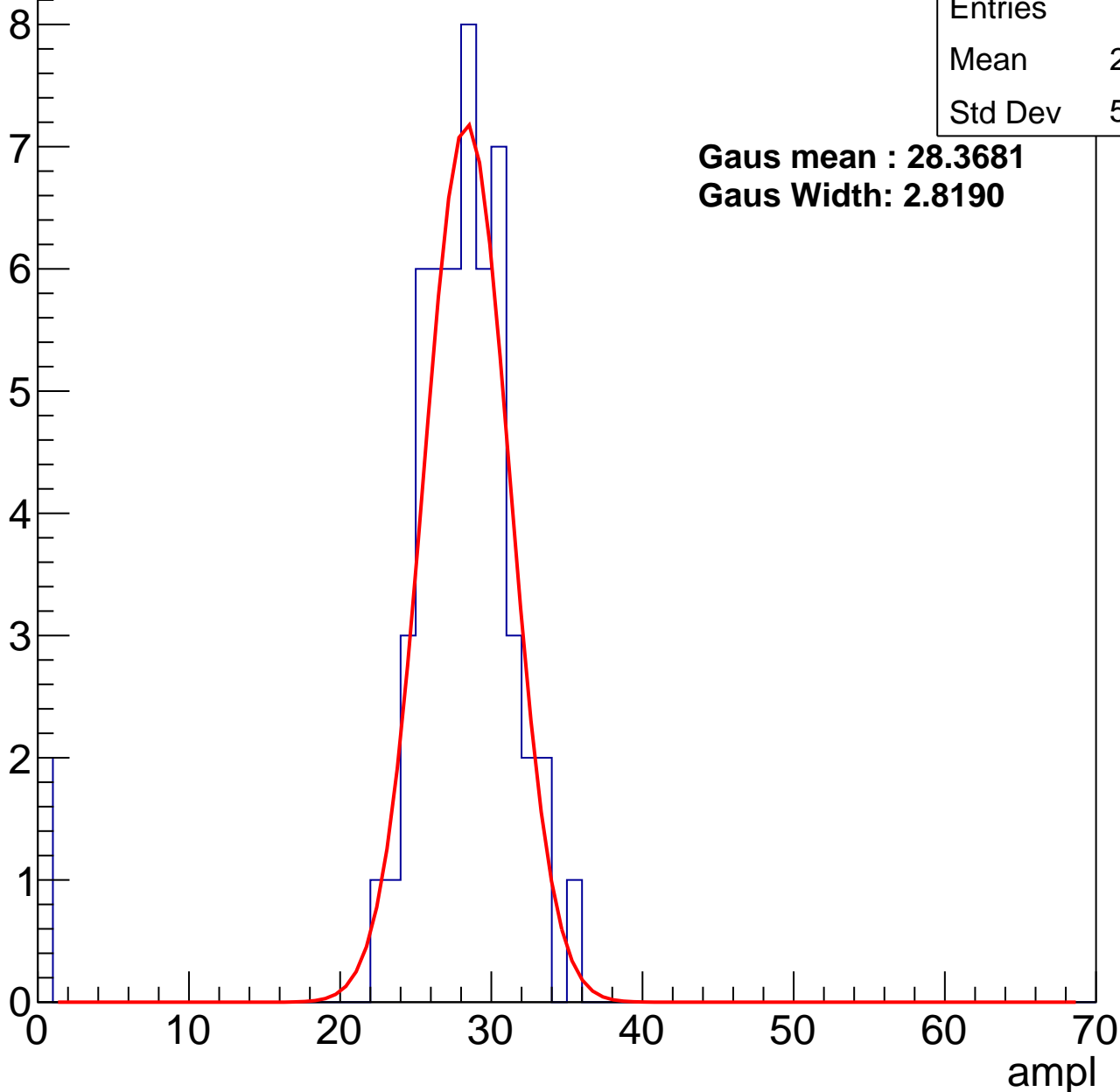
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	54
Mean	26.87
Std Dev	5.907

**Gaus mean : 28.3681**

**Gaus Width: 2.8190**



# B1L003S, U26-ch32, adc1

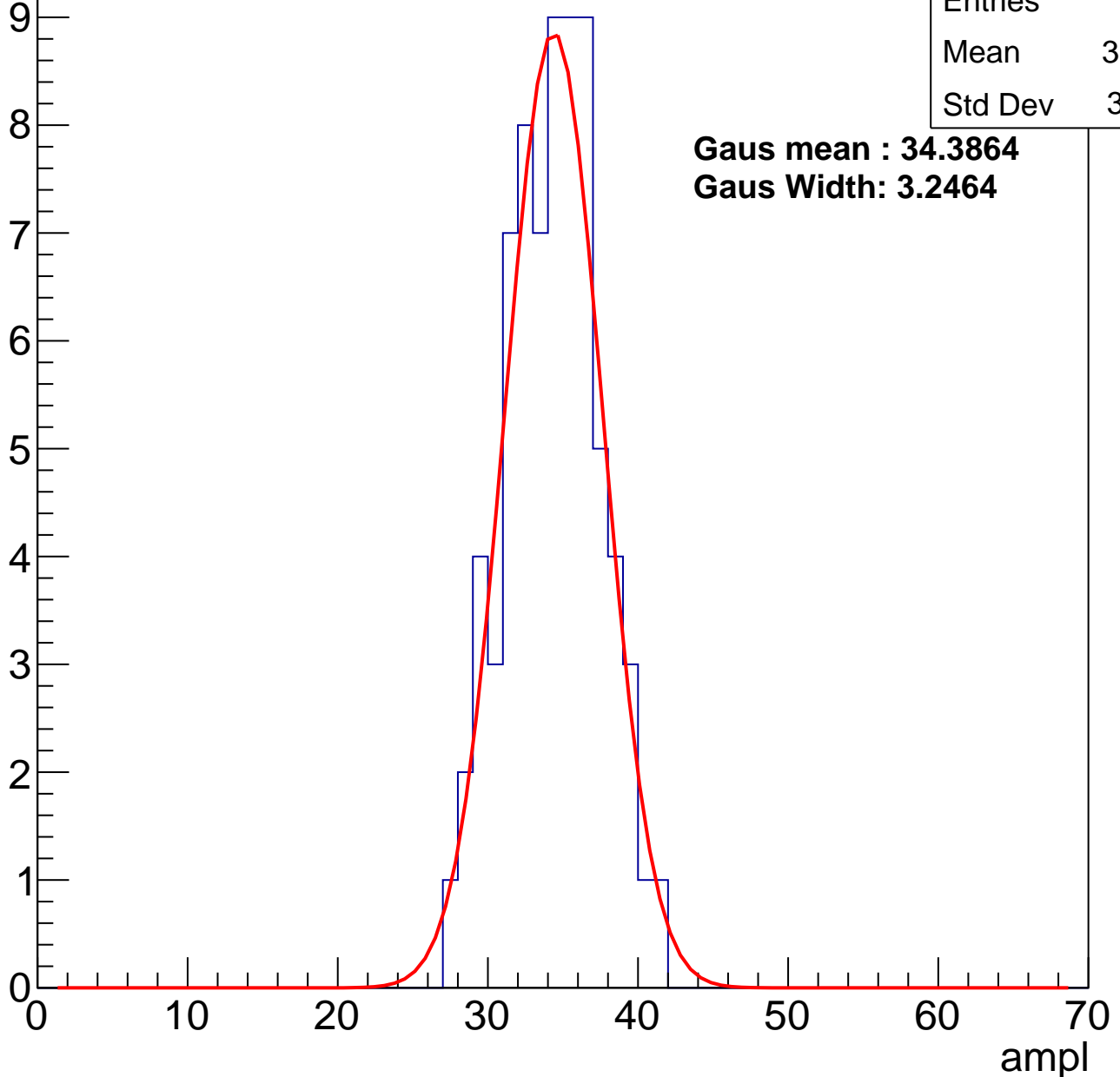
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	73
Mean	33.88
Std Dev	3.061

**Gaus mean : 34.3864**

**Gaus Width: 3.2464**



# B1L003S, U26-ch32, adc2

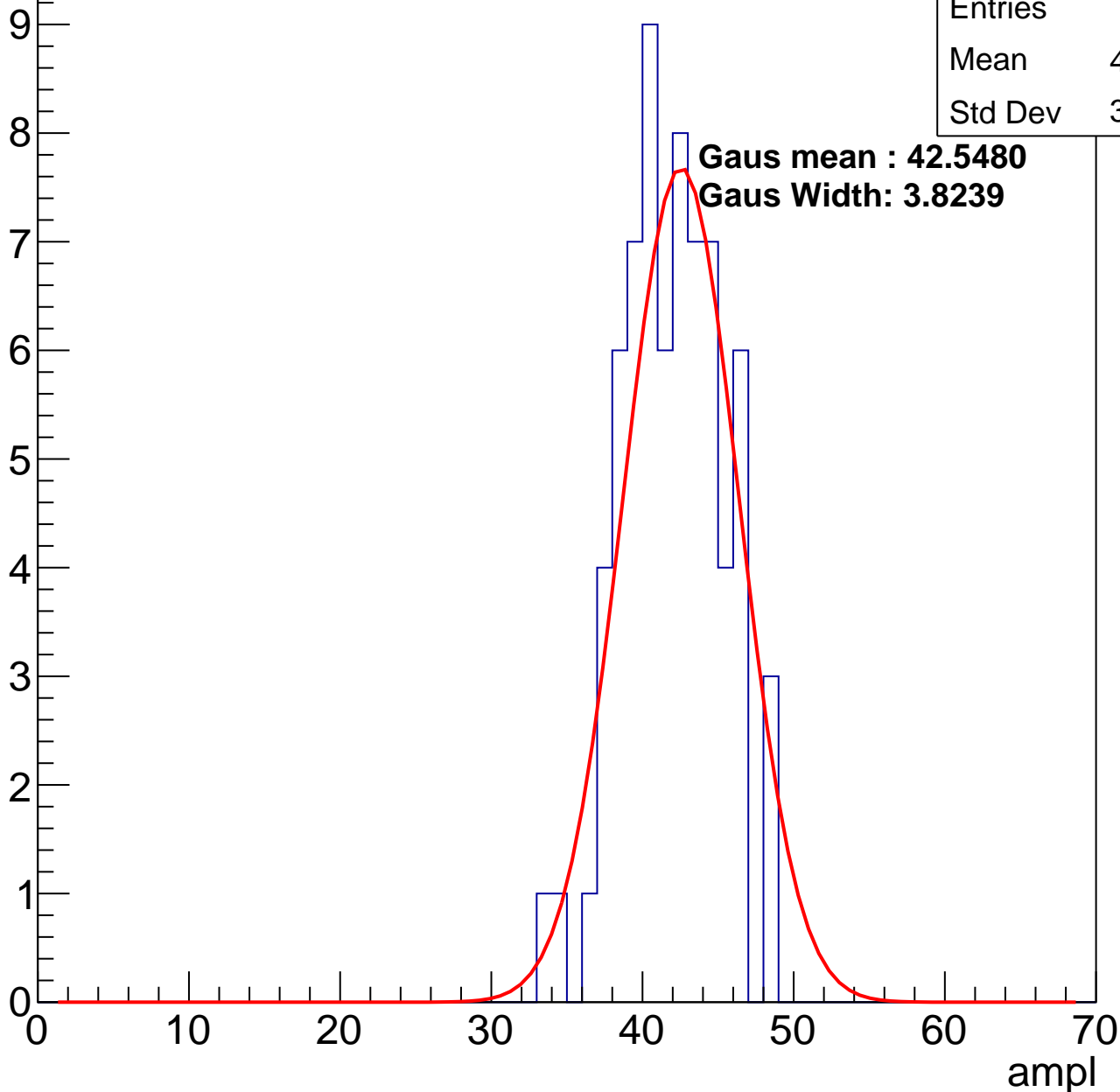
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	41.47
Std Dev	3.246

**Gaus mean : 42.5480**

**Gaus Width: 3.8239**

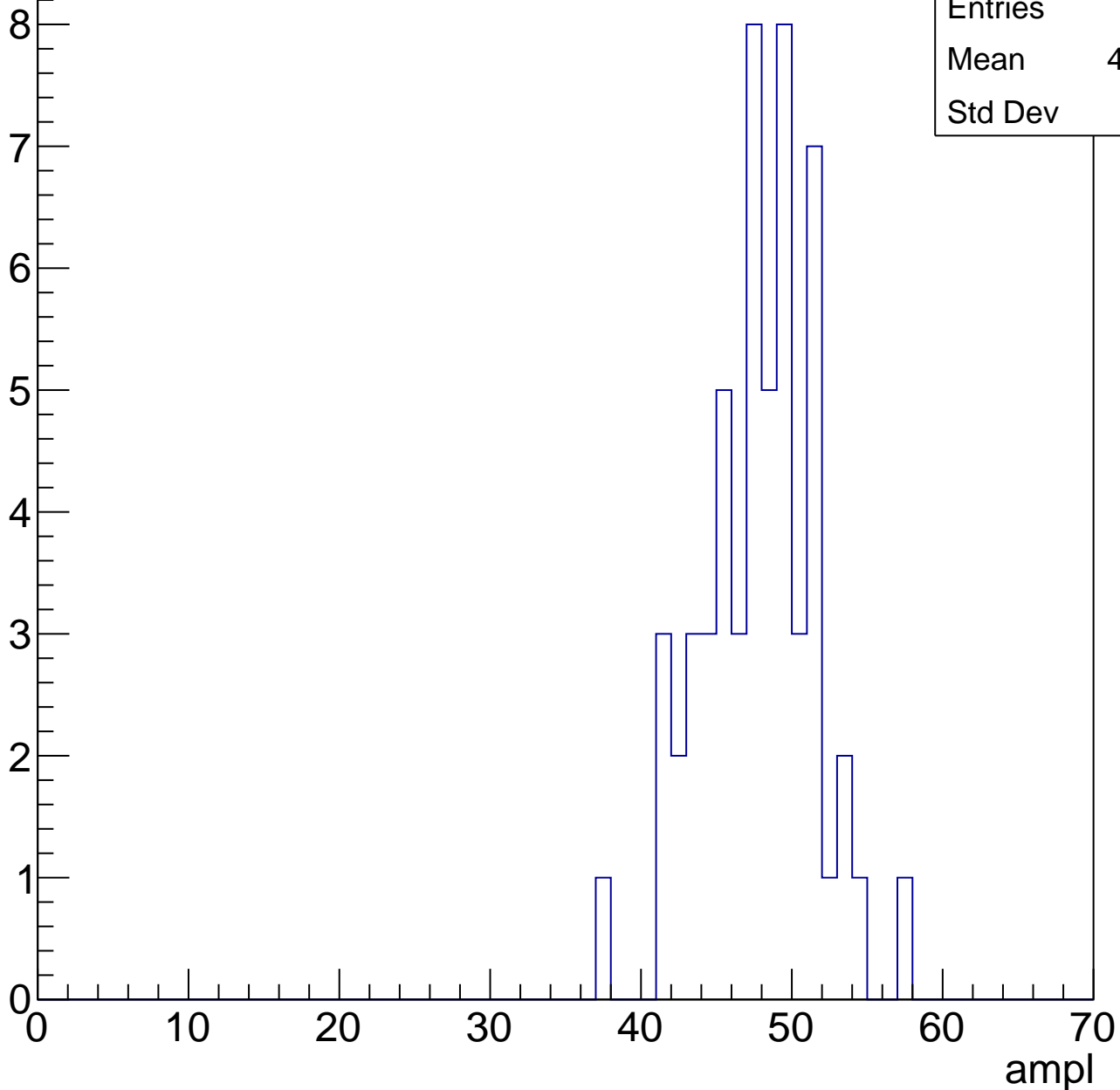


# B1L003S, U26-ch32, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	47.36
Std Dev	3.71

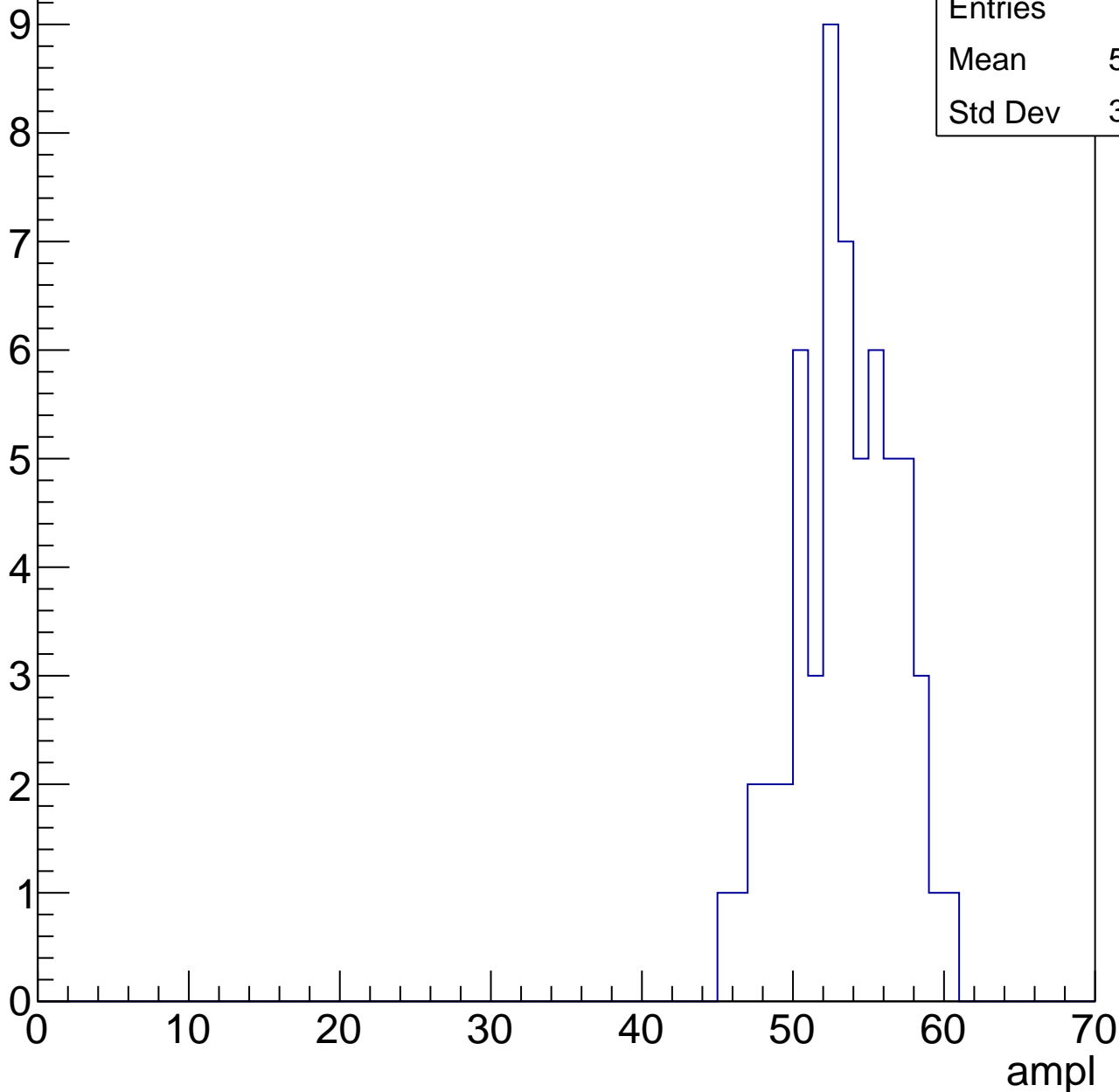


# B1L003S, U26-ch32, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	53.03
Std Dev	3.334



# B1L003S, U26-ch32, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

10

8

6

4

2

0

0

10

20

30

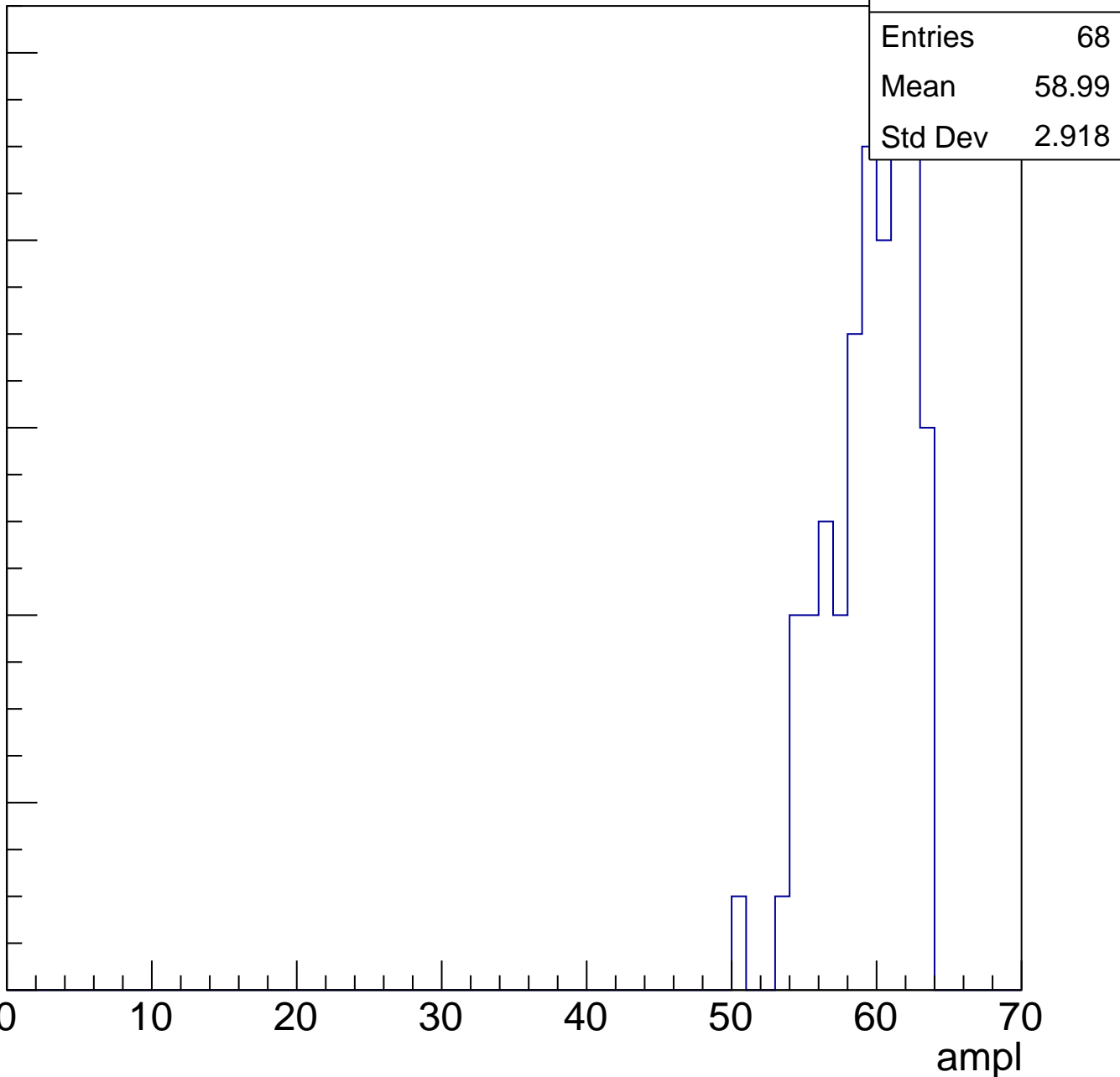
40

50

60

ampl

Entries	68
Mean	58.99
Std Dev	2.918



# B1L003S, U26-ch32, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch32, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	3
Mean	28.33
Std Dev	26.11

# B1L003S, U26-ch33, adc0

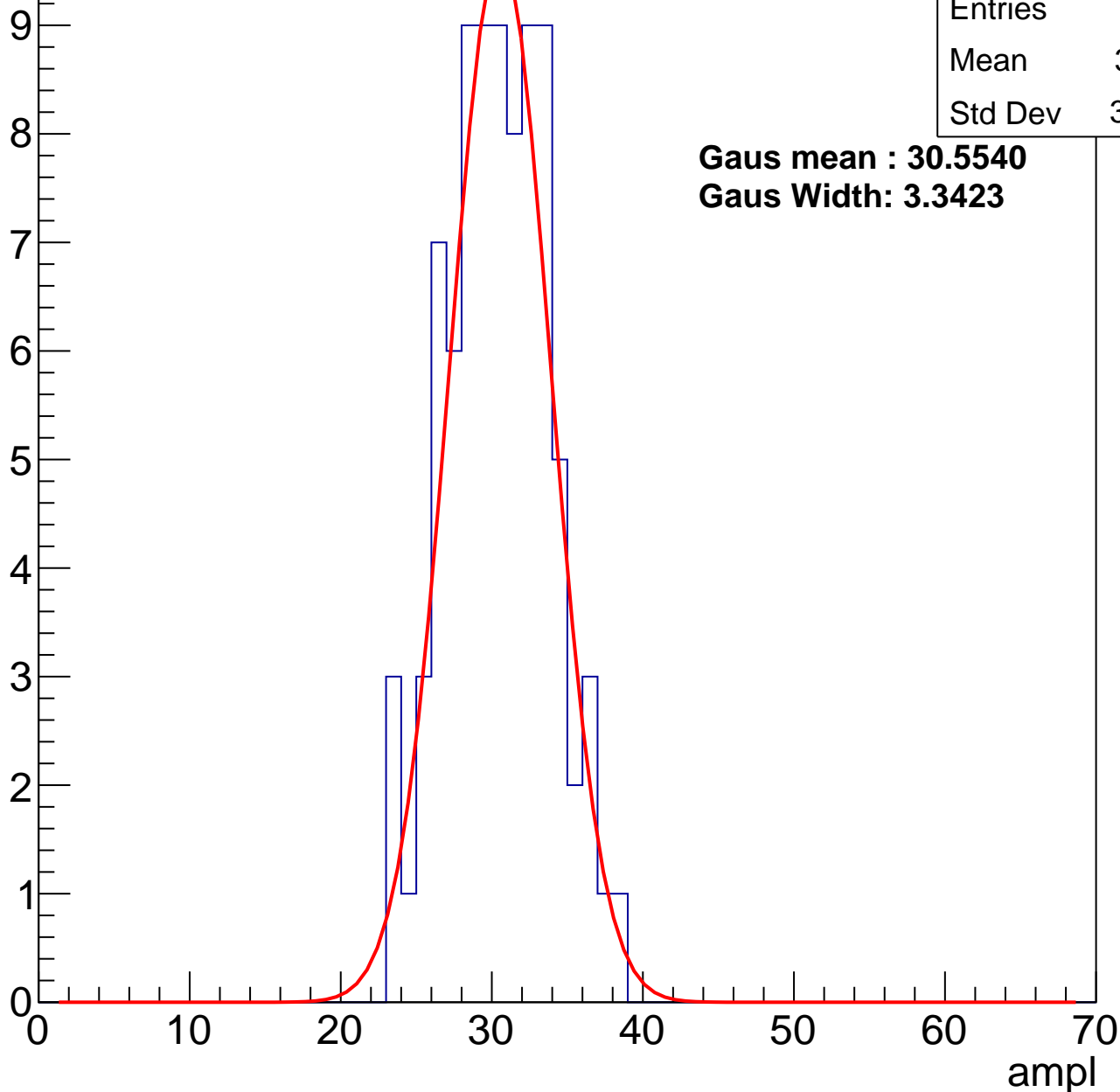
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	85
Mean	30.01
Std Dev	3.334

**Gaus mean : 30.5540**

**Gaus Width: 3.3423**



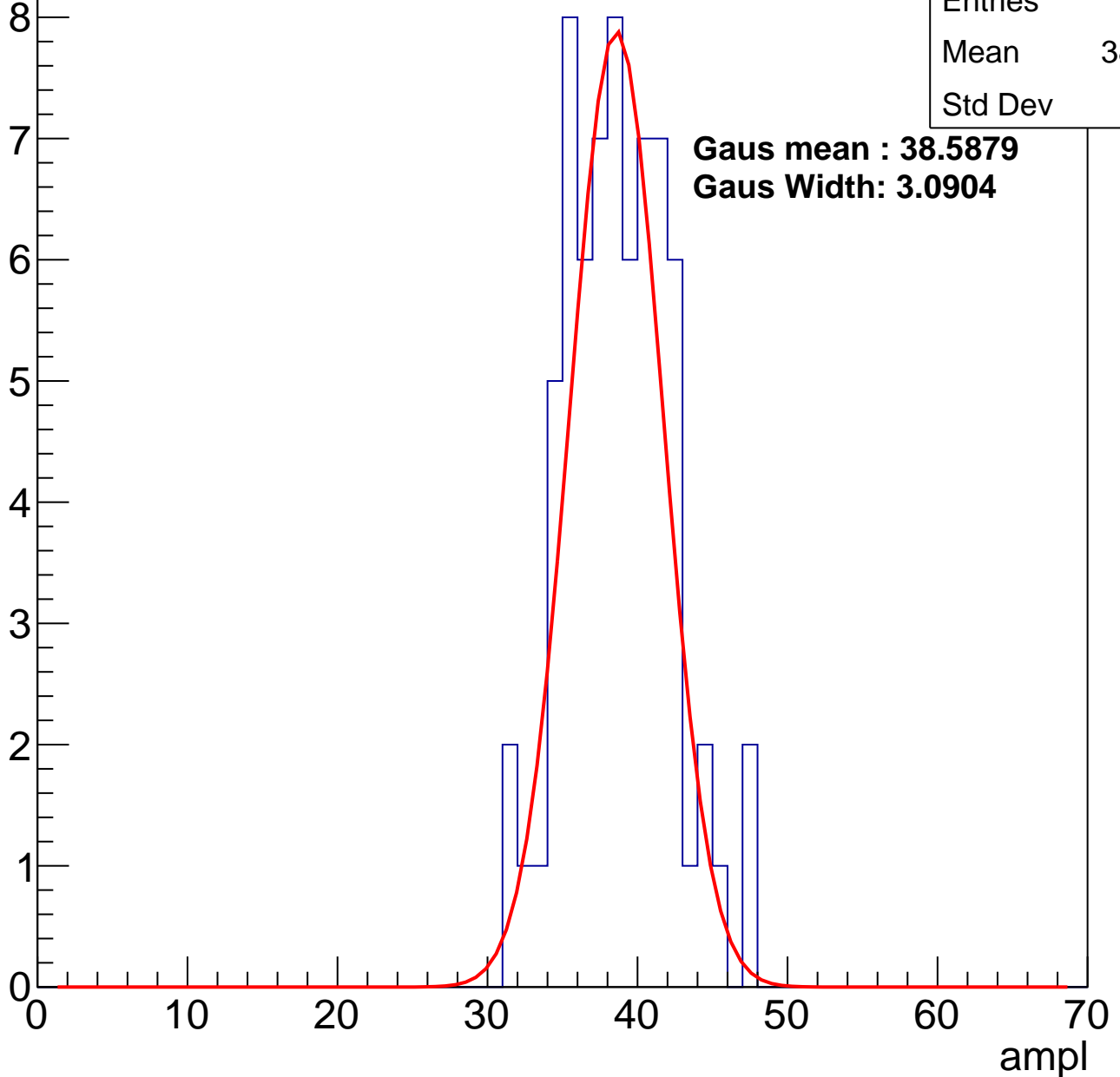
# B1L003S, U26-ch33, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	38.27
Std Dev	3.46

**Gaus mean : 38.5879**  
**Gaus Width: 3.0904**



# B1L003S, U26-ch33, adc2

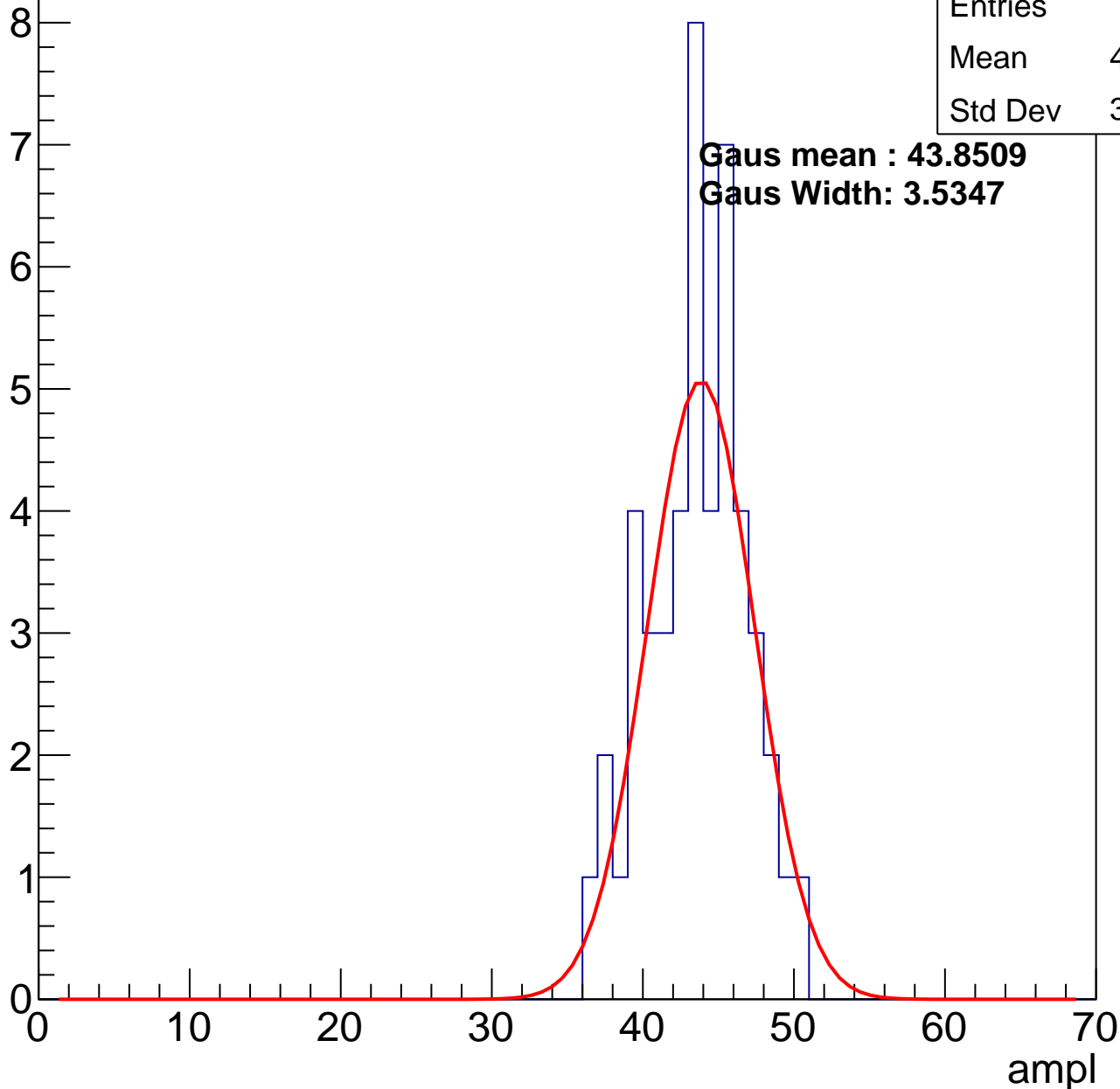
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	48
Mean	43.12
Std Dev	3.238

**Gaus mean : 43.8509**

**Gaus Width: 3.5347**



# B1L003S, U26-ch33, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

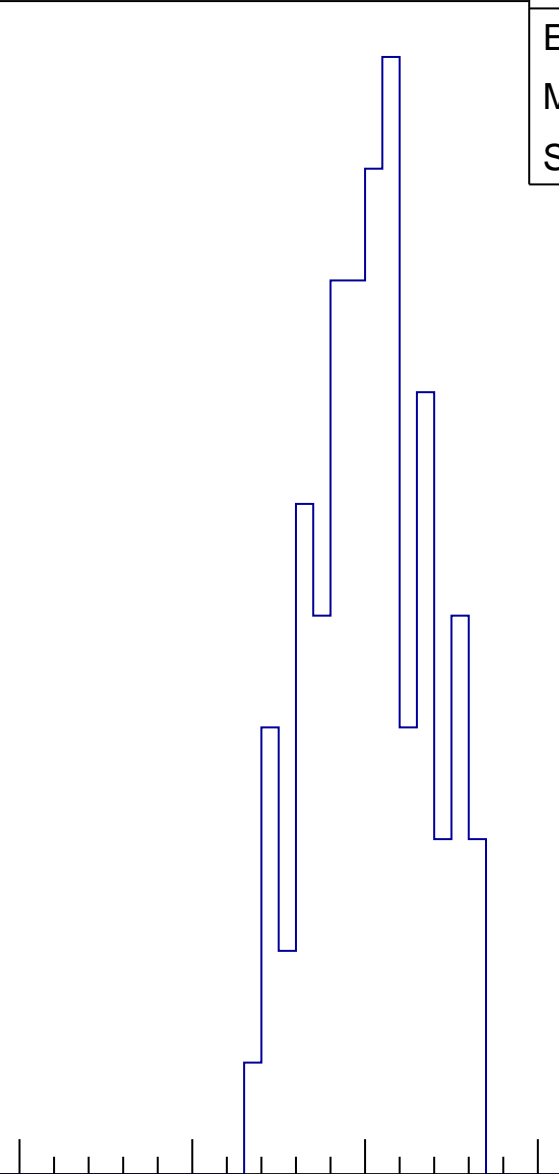
Entries	75
Mean	49.87
Std Dev	3.251

Entry

10  
8  
6  
4  
2  
0

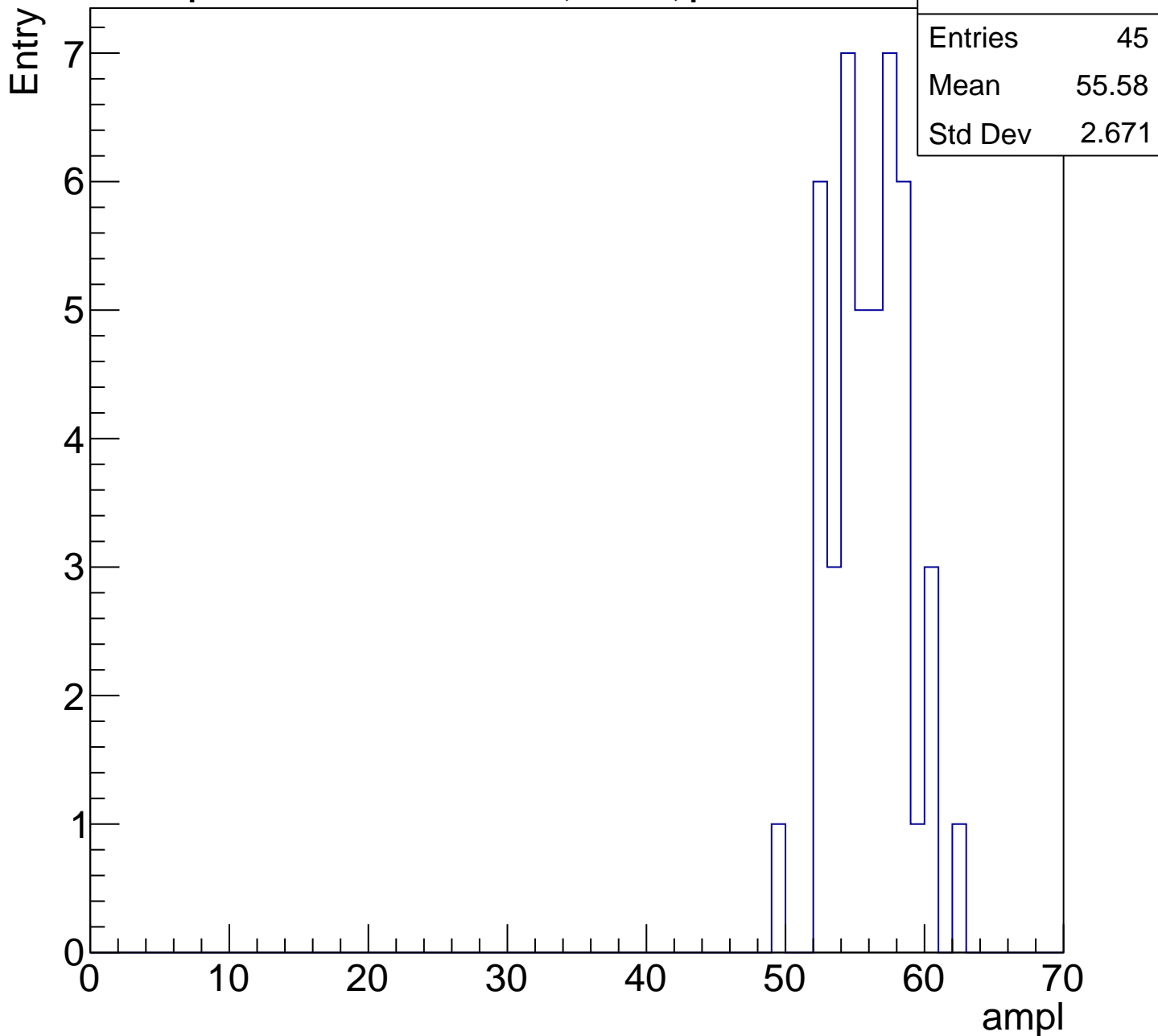
0 10 20 30 40 50 60 70

ampl



# B1L003S, U26-ch33, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

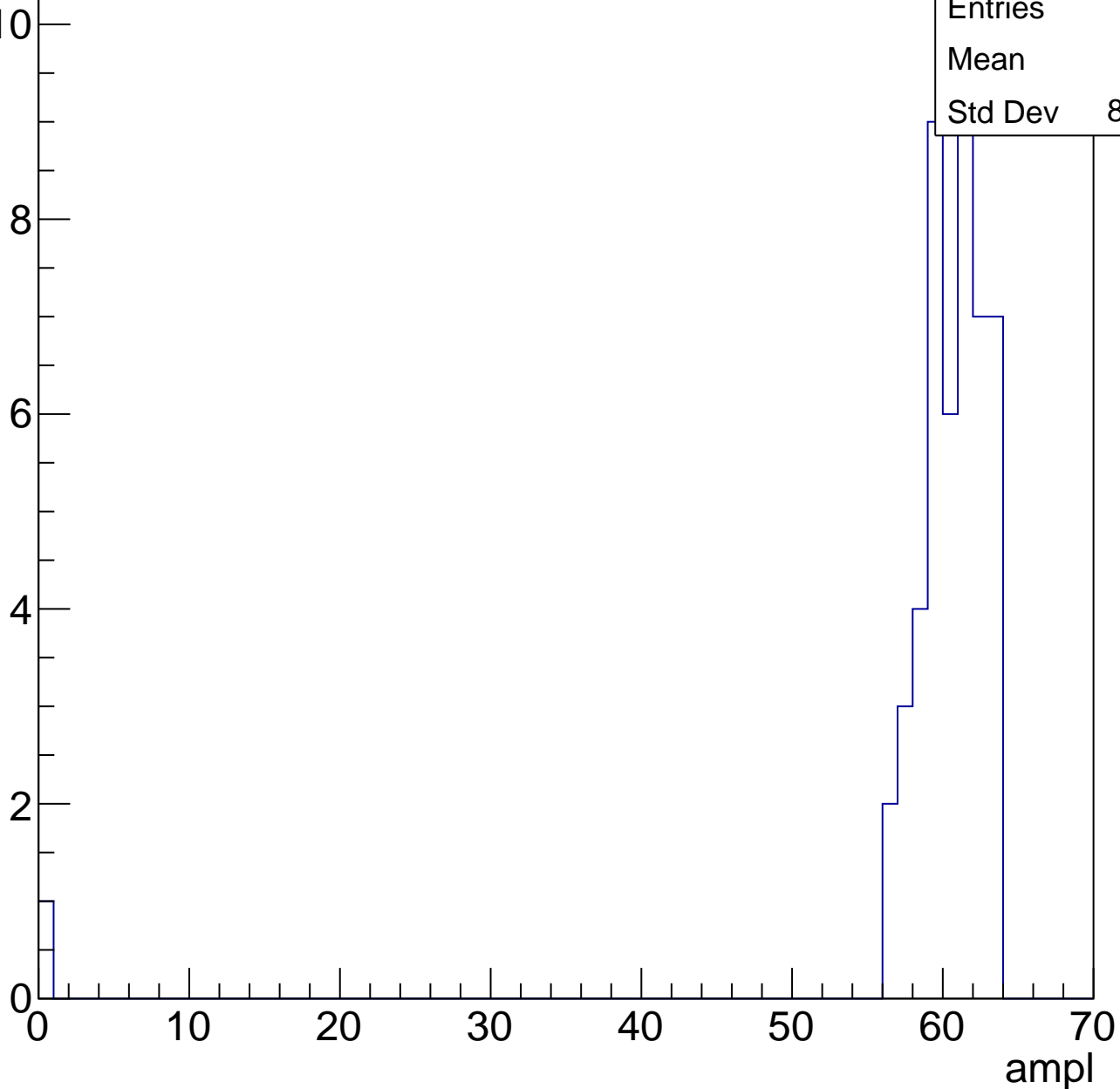


# B1L003S, U26-ch33, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

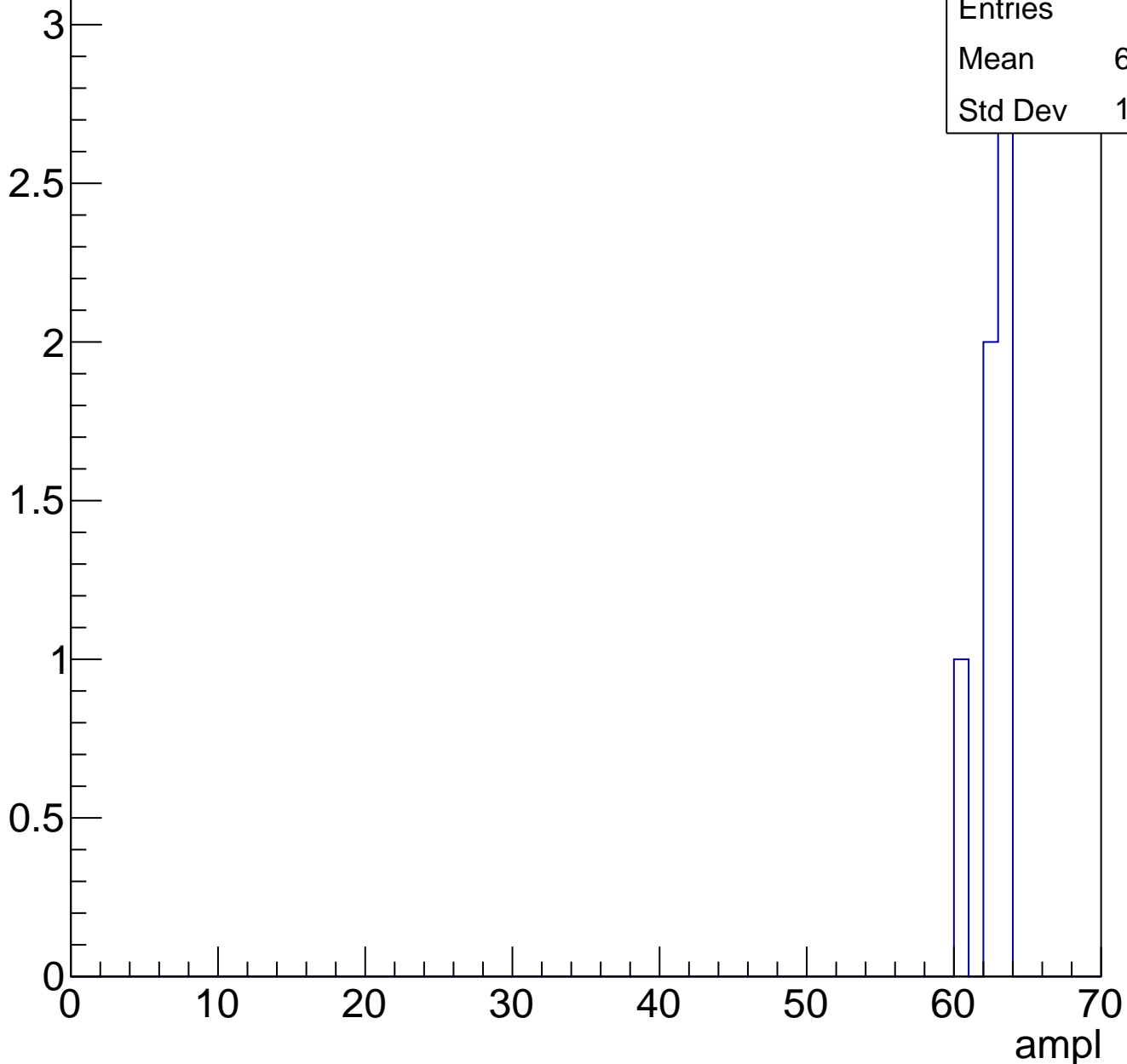
Entries	49
Mean	59
Std Dev	8.732



# B1L003S, U26-ch33, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

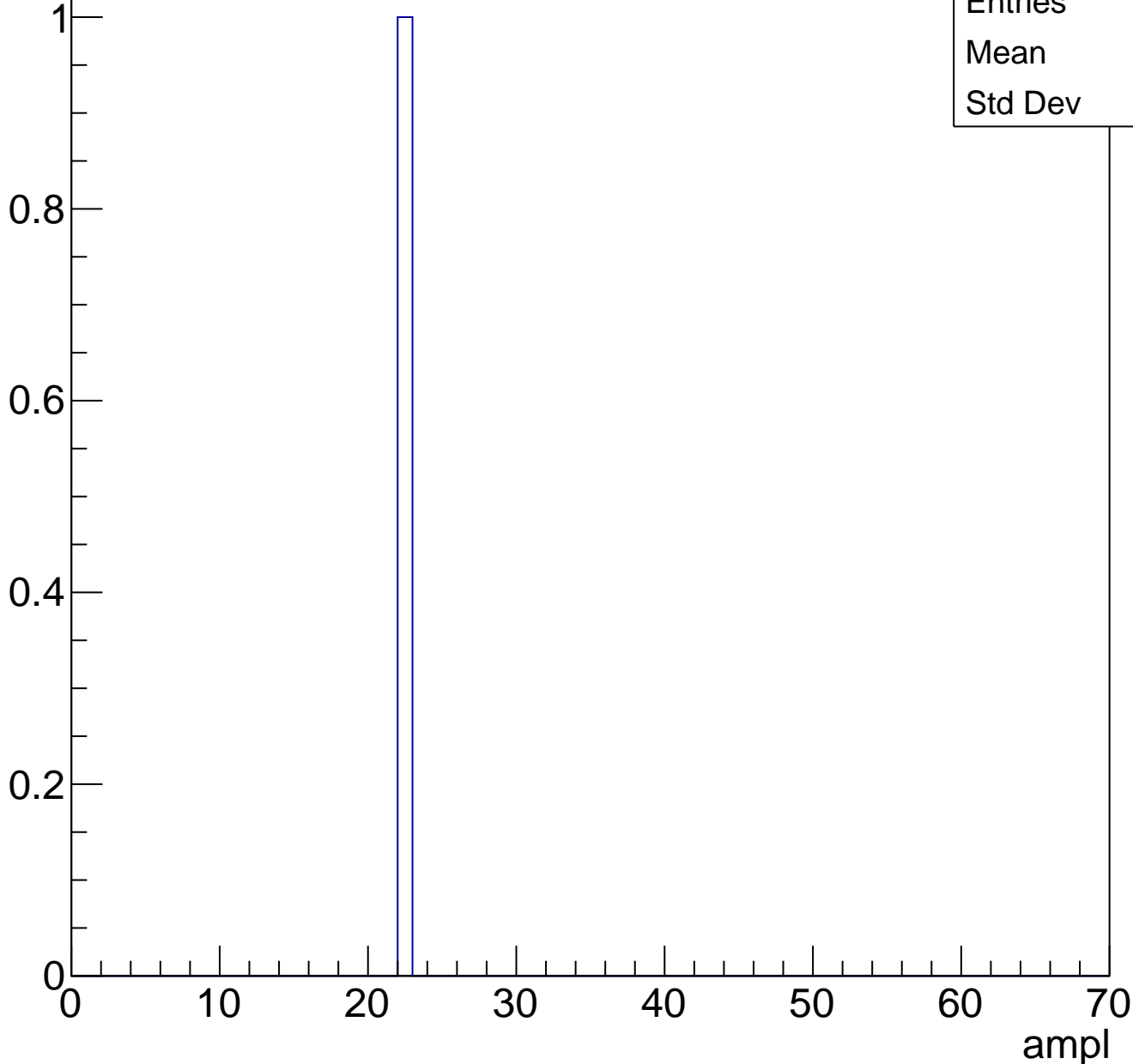




# B1L003S, U26-ch33, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	22
Std Dev	0

# B1L003S, U26-ch34, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	72
Mean	28.26
Std Dev	4.422

**Gaus mean : 29.1620**

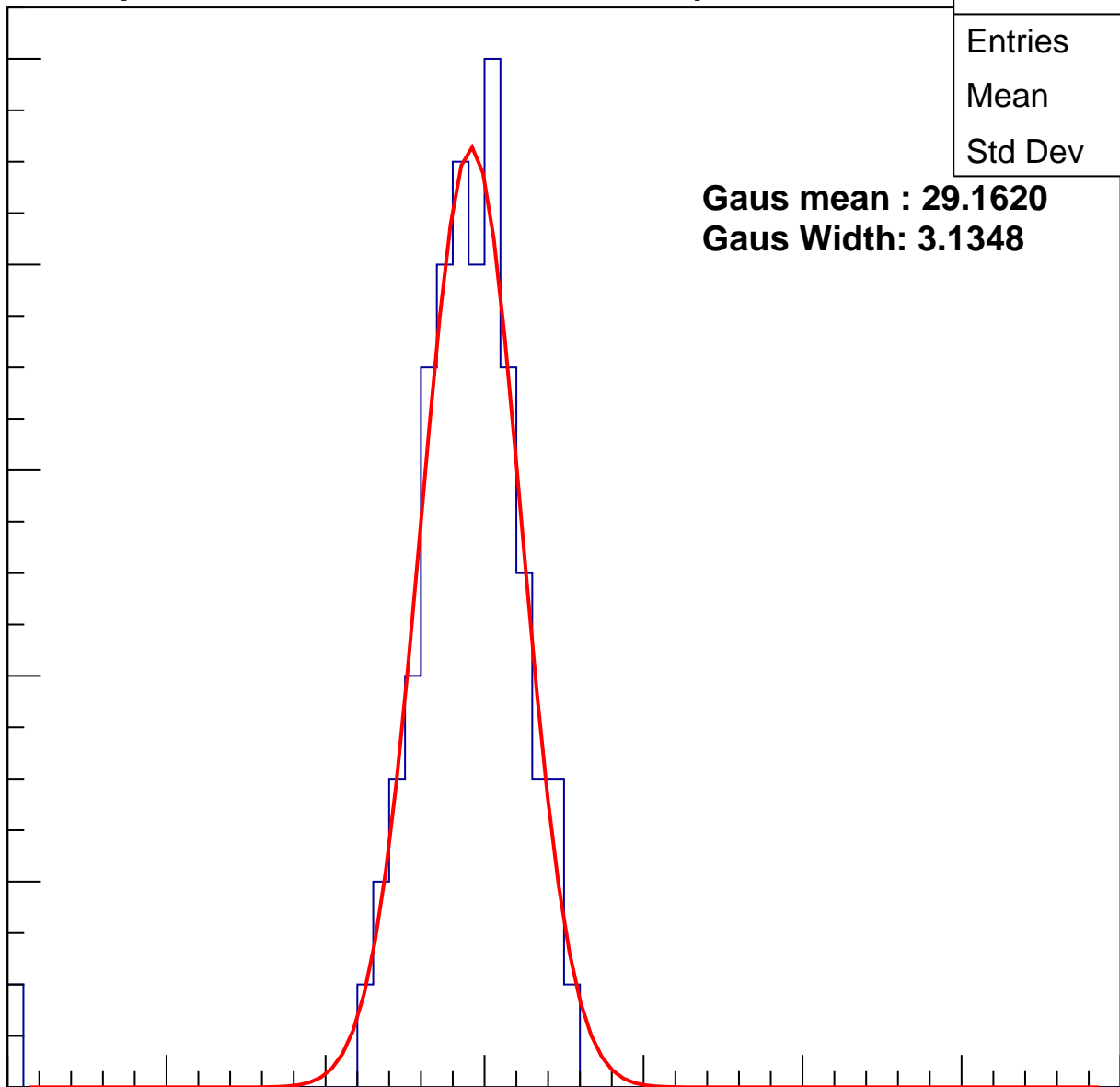
**Gaus Width: 3.1348**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U26-ch34, adc1

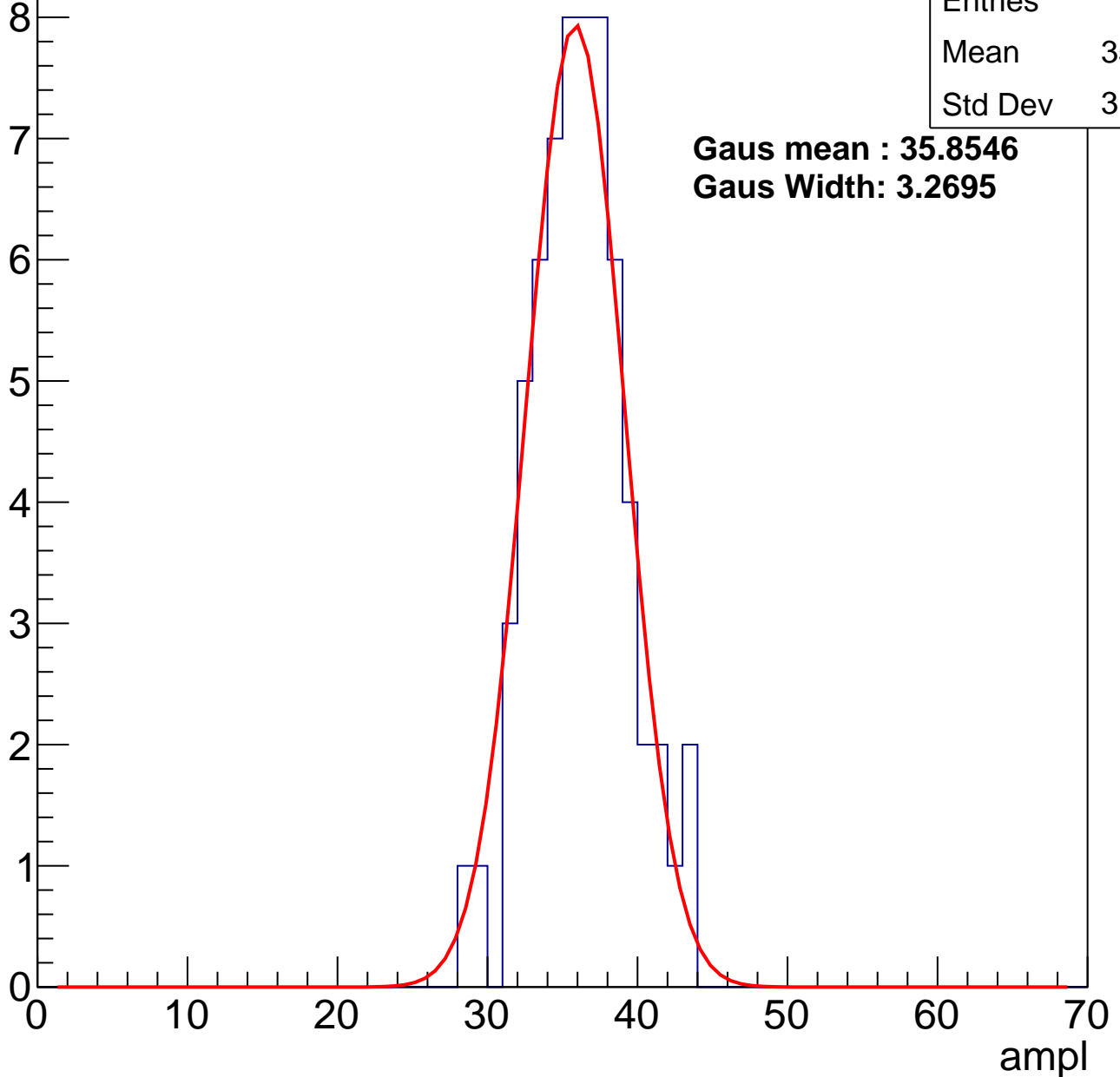
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	35.69
Std Dev	3.152

**Gaus mean : 35.8546**

**Gaus Width: 3.2695**



# B1L003S, U26-ch34, adc2

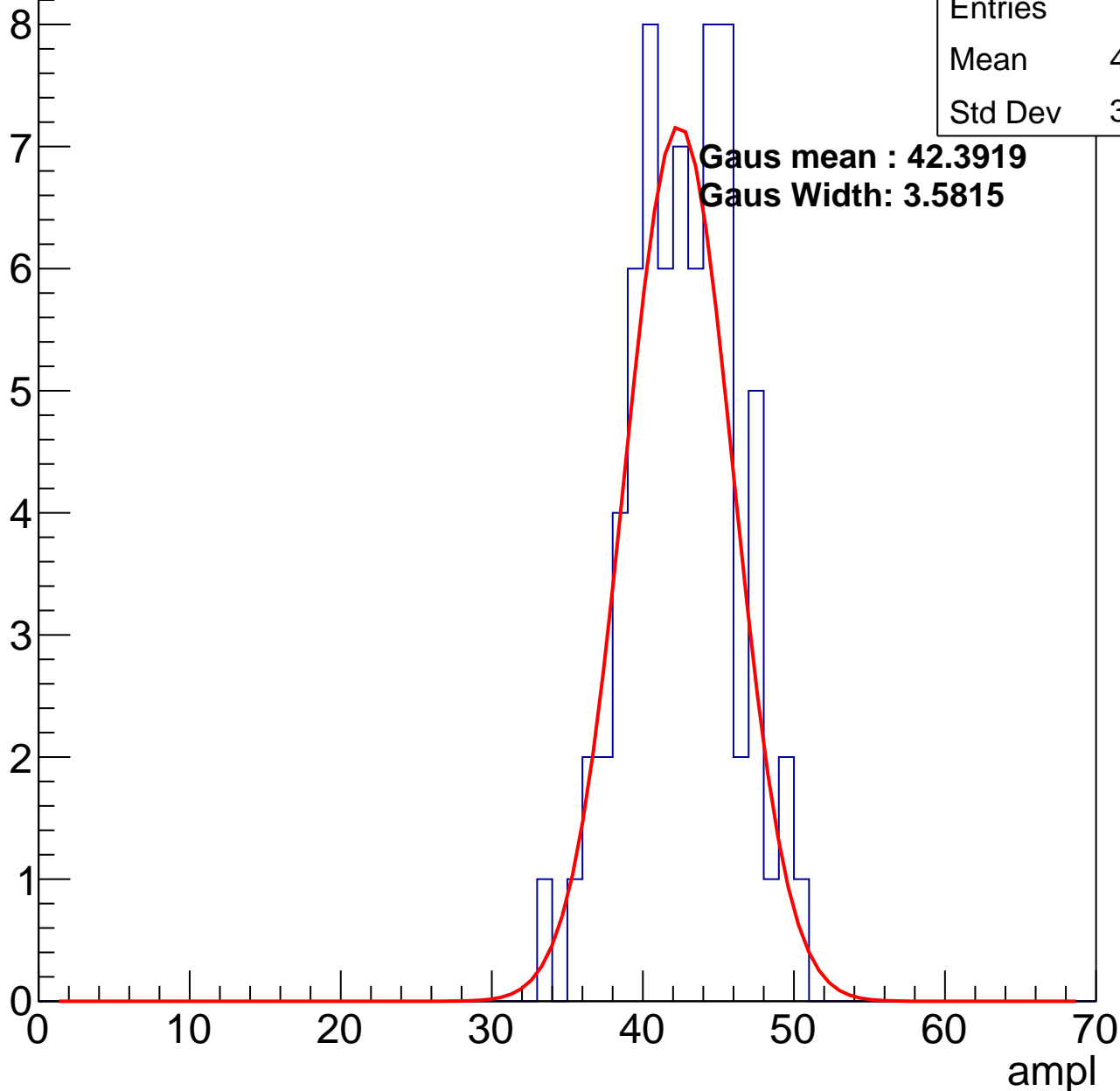
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	42.19
Std Dev	3.527

**Gaus mean : 42.3919**

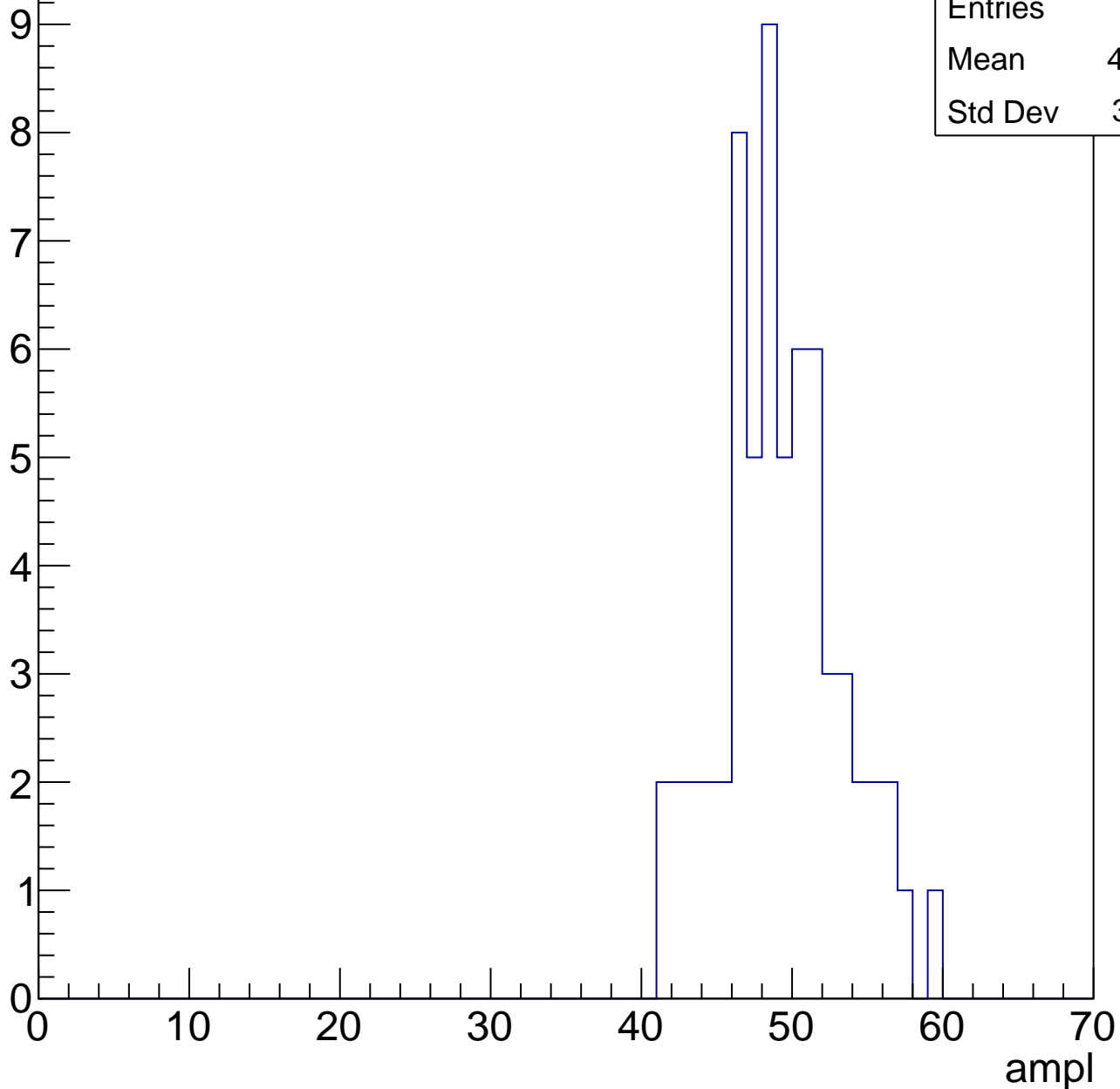
**Gaus Width: 3.5815**



# B1L003S, U26-ch34, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



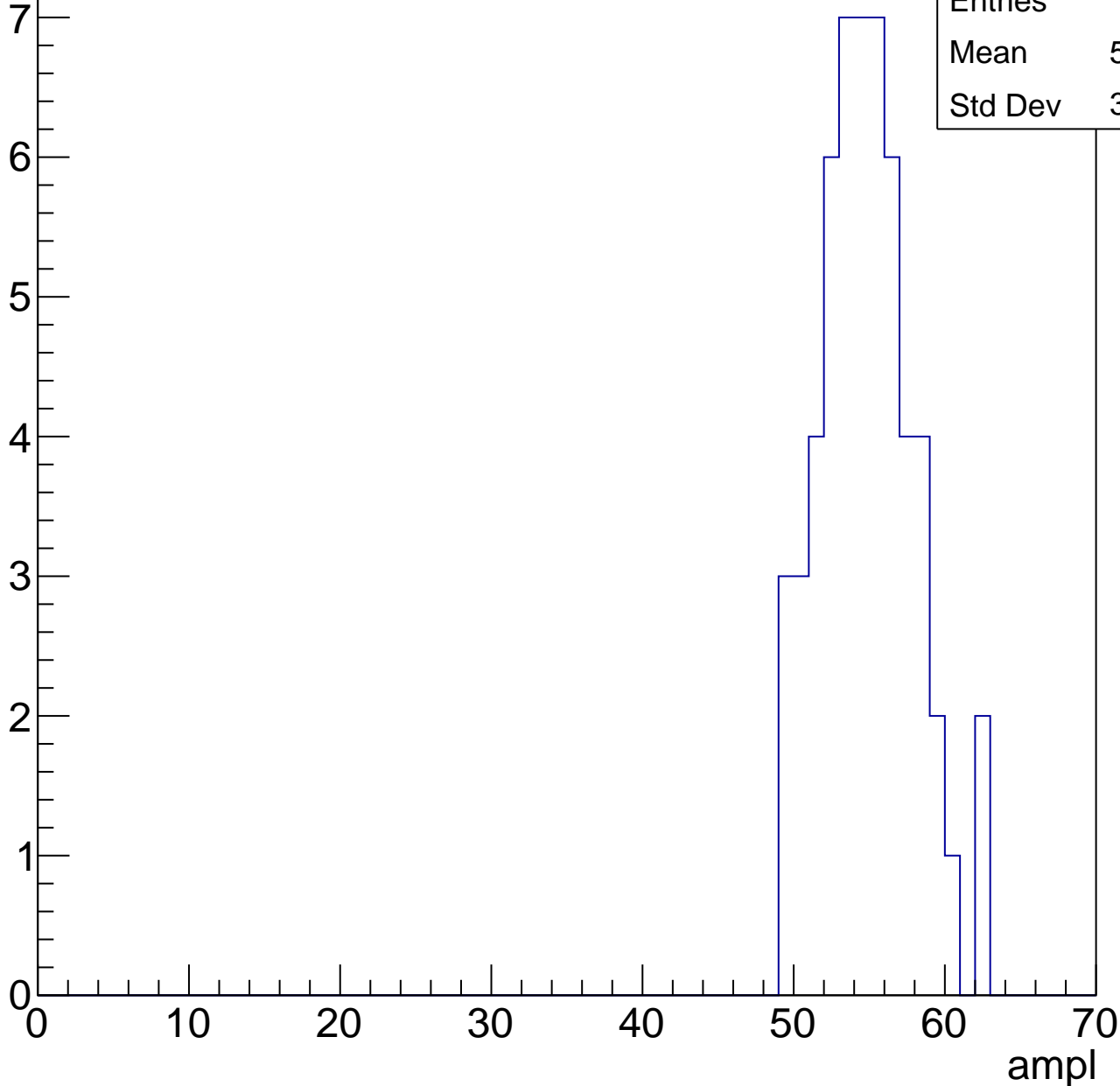
Entries	63
Mean	48.84
Std Dev	3.921

# B1L003S, U26-ch34, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	54.38
Std Dev	3.068



# B1L003S, U26-ch34, adc5

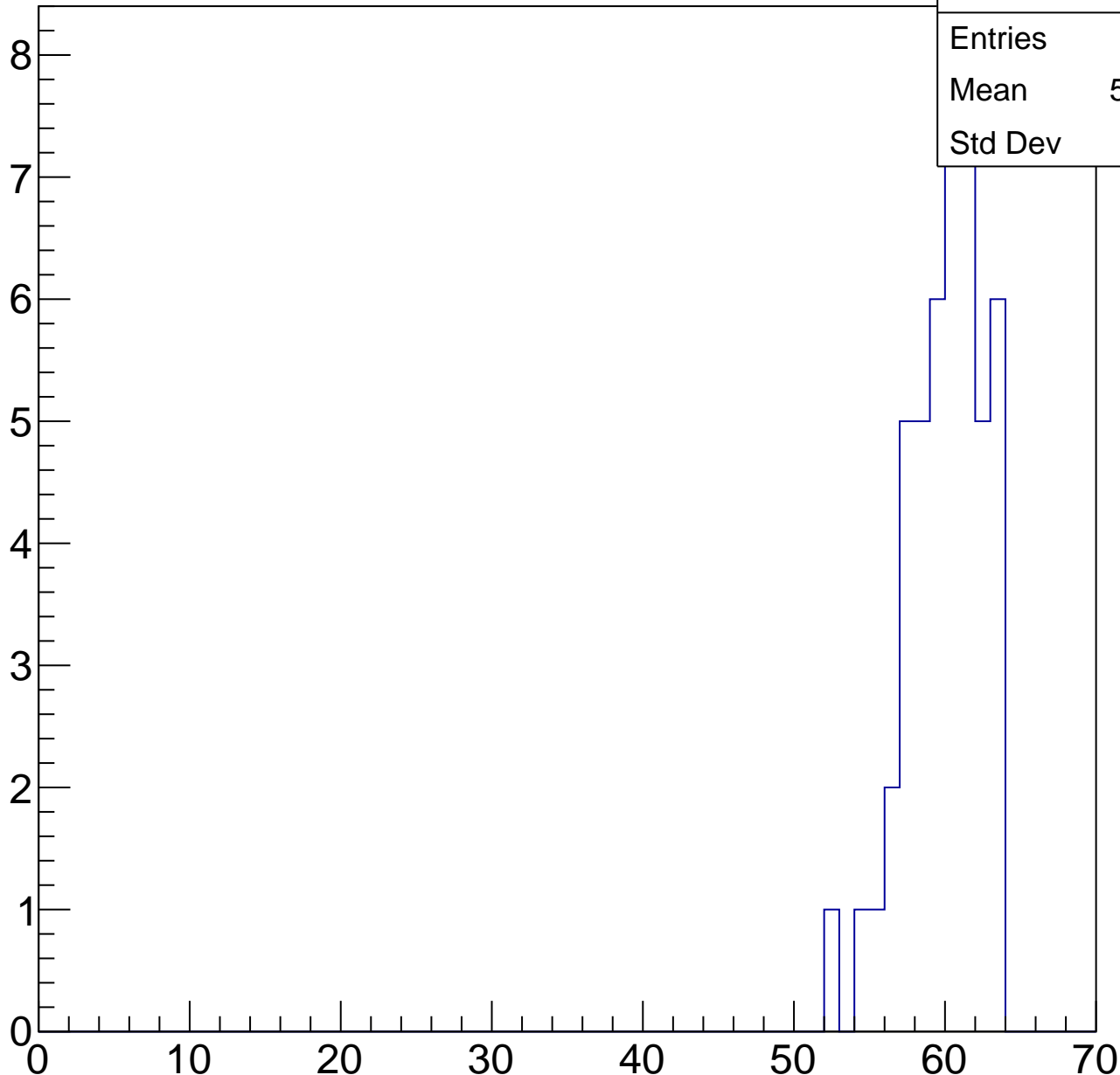
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	48
Mean	59.54
Std Dev	2.5

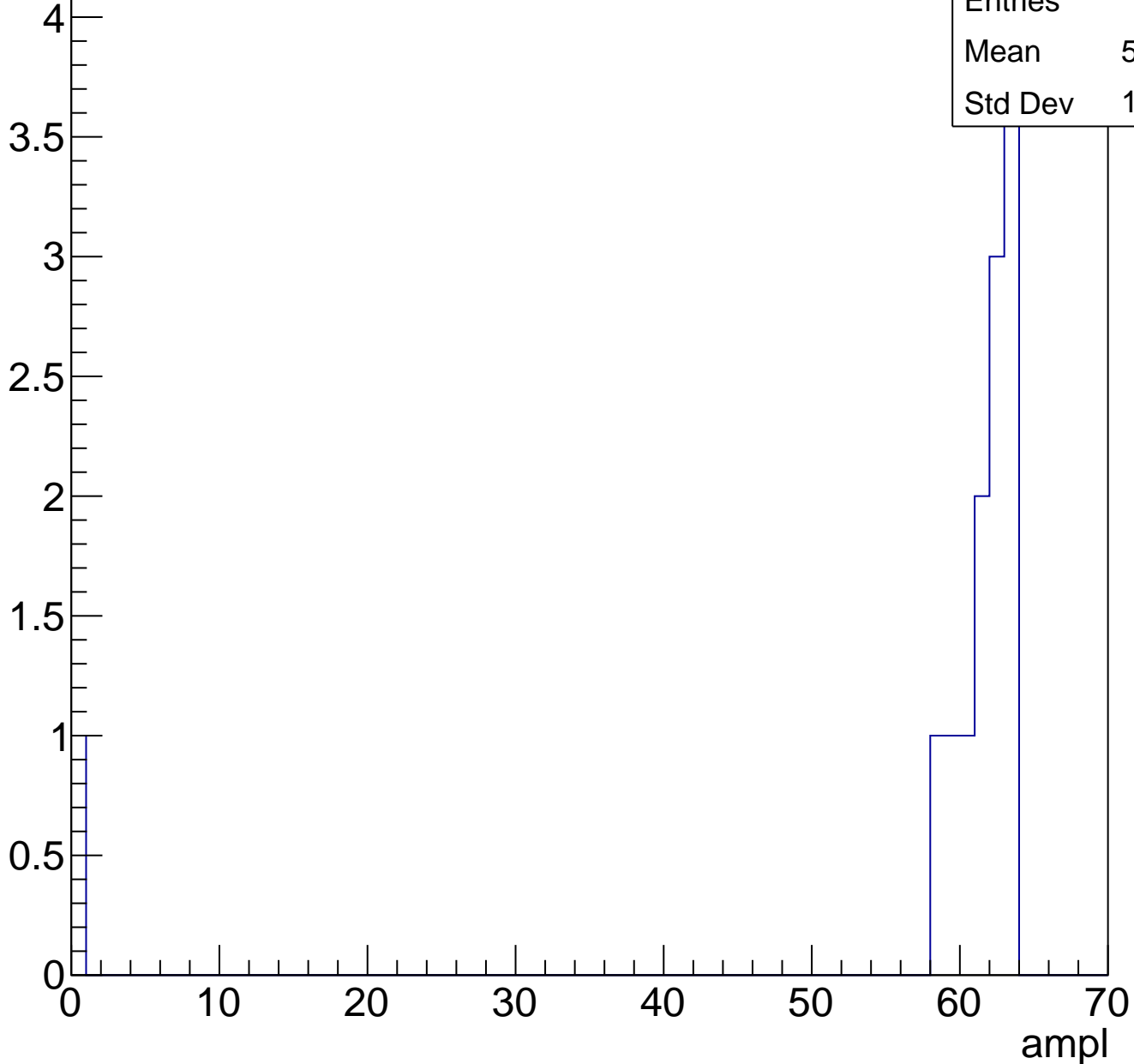
ampl



# B1L003S, U26-ch34, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch34, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U26-ch35, adc0

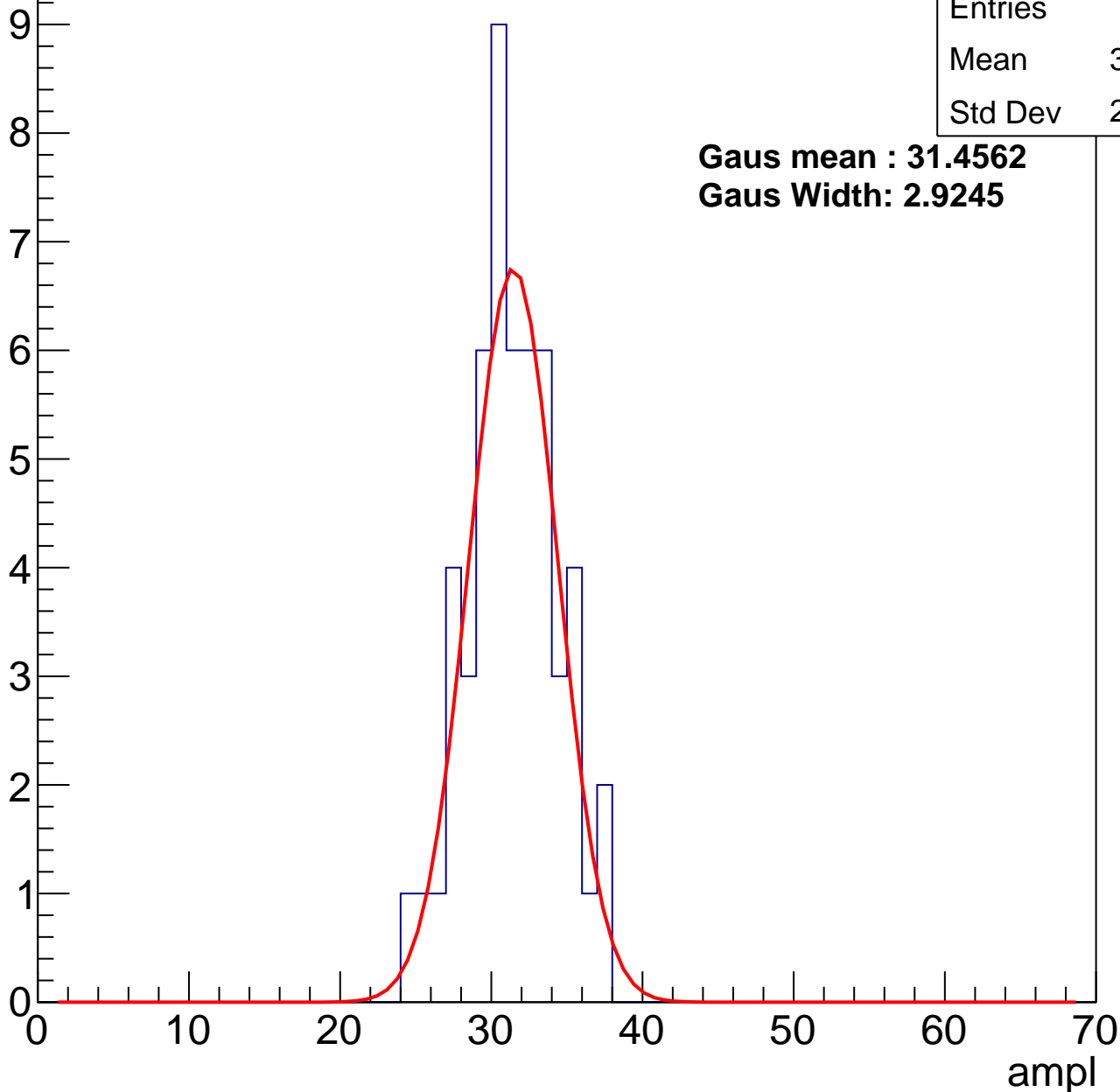
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	30.92
Std Dev	2.919

**Gaus mean : 31.4562**

**Gaus Width: 2.9245**



# B1L003S, U26-ch35, adc1

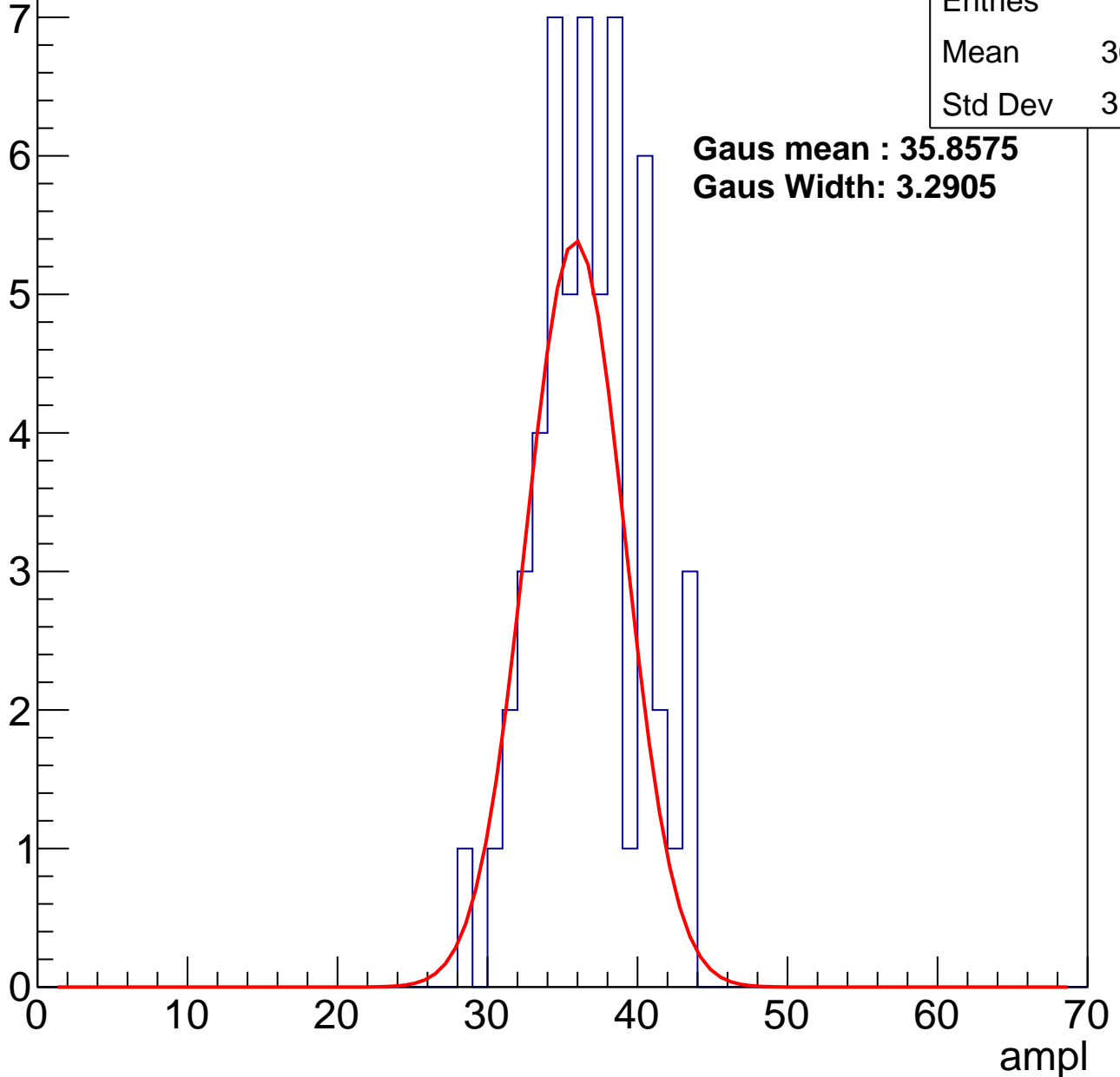
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	36.29
Std Dev	3.393

**Gaus mean : 35.8575**

**Gaus Width: 3.2905**



# B1L003S, U26-ch35, adc2

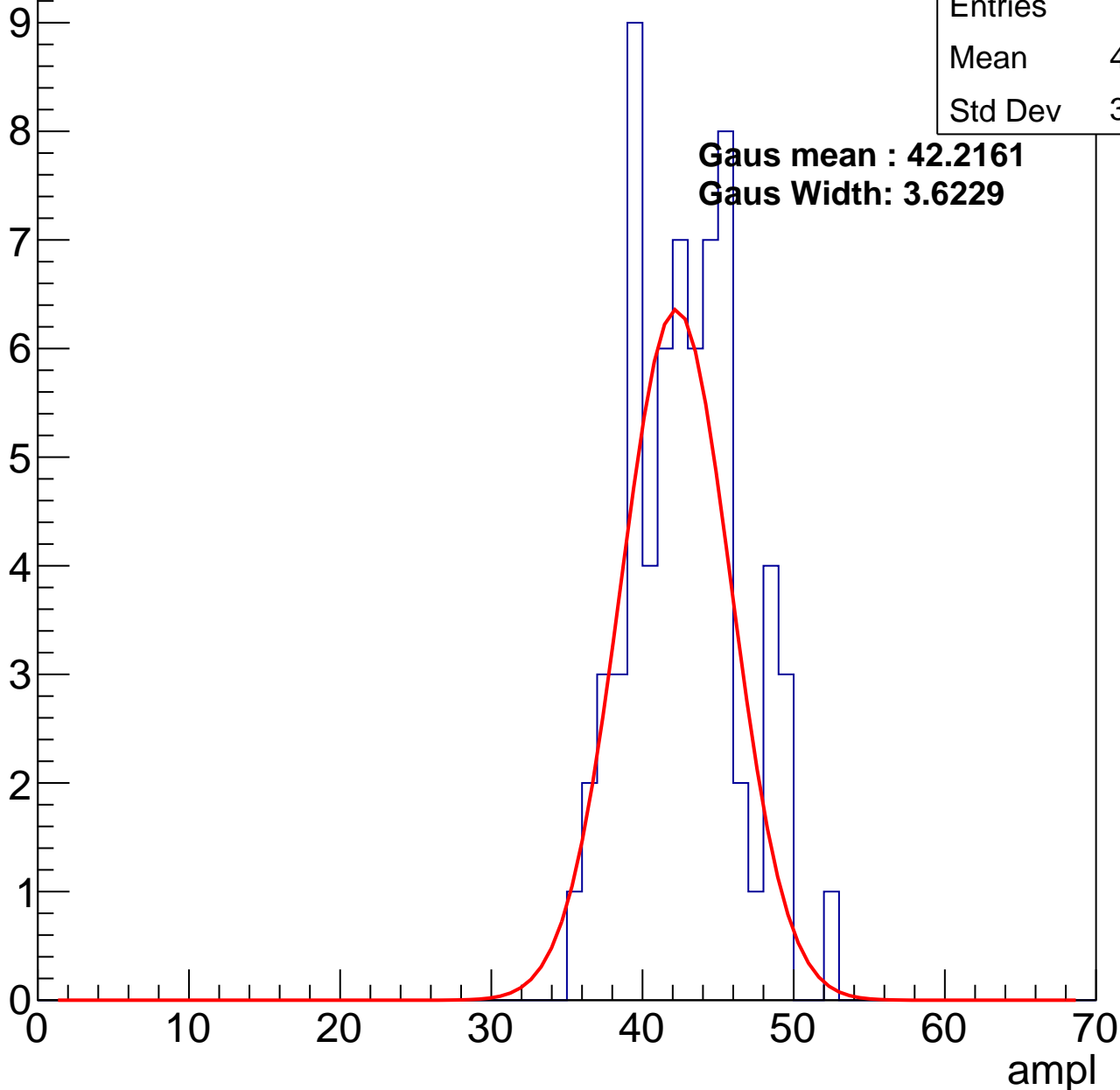
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	42.37
Std Dev	3.648

**Gaus mean : 42.2161**

**Gaus Width: 3.6229**

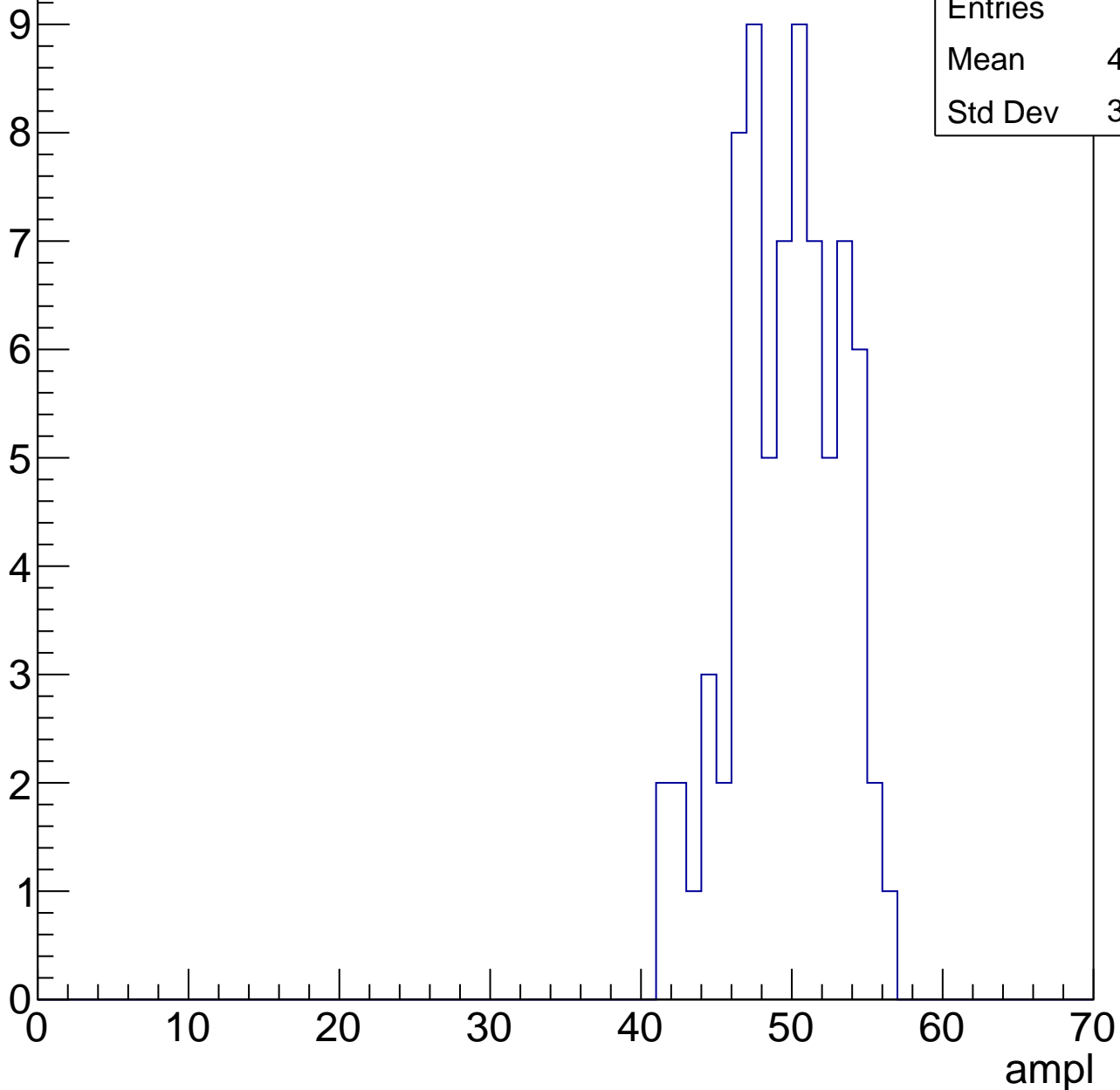


# B1L003S, U26-ch35, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

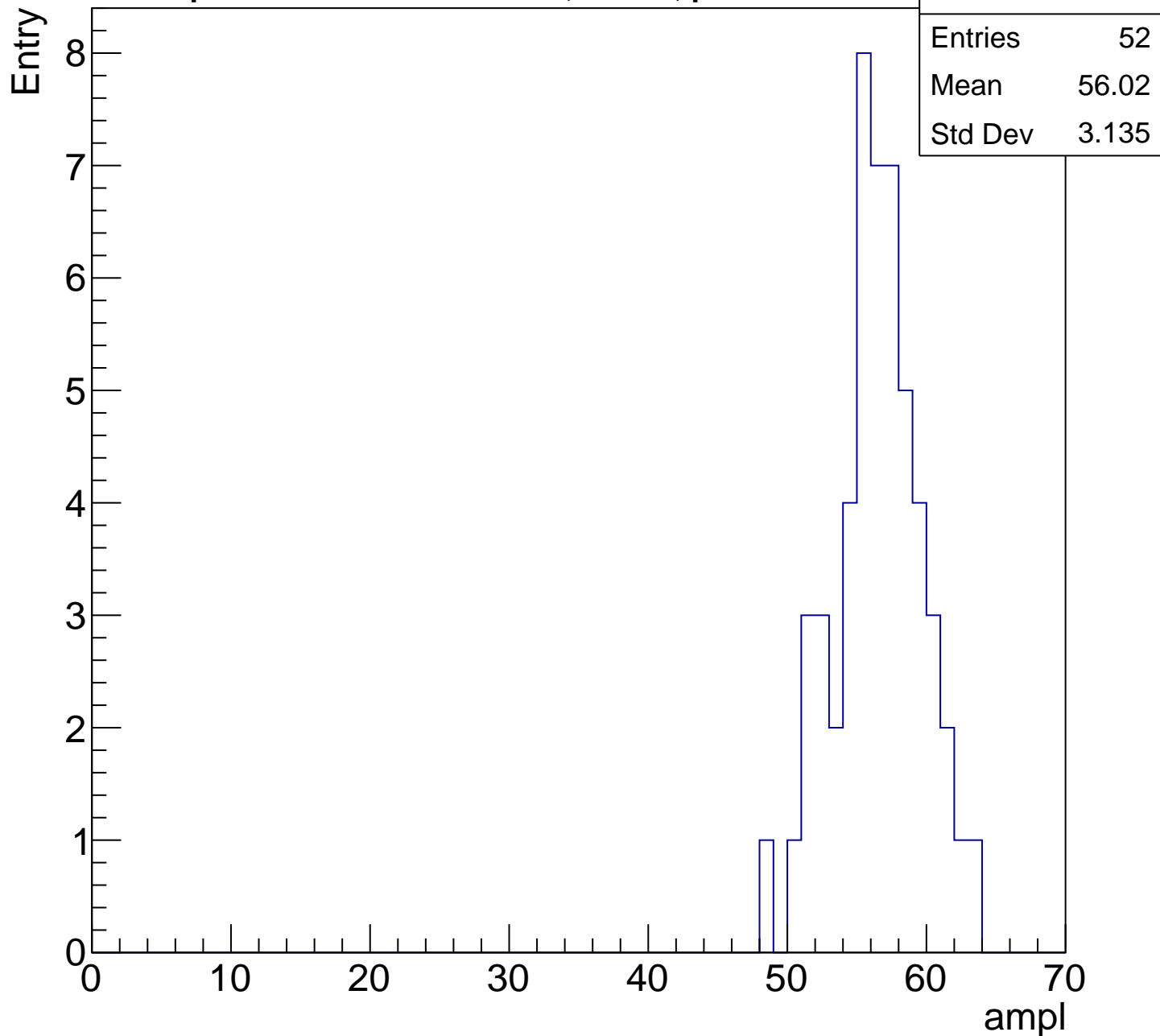
Entry

Entries	76
Mean	49.12
Std Dev	3.528



# B1L003S, U26-ch35, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2



# B1L003S, U26-ch35, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	45
Mean	59.98
Std Dev	2.534

ampl

0

10

20

30

40

50

60

70

1

2

3

4

5

6

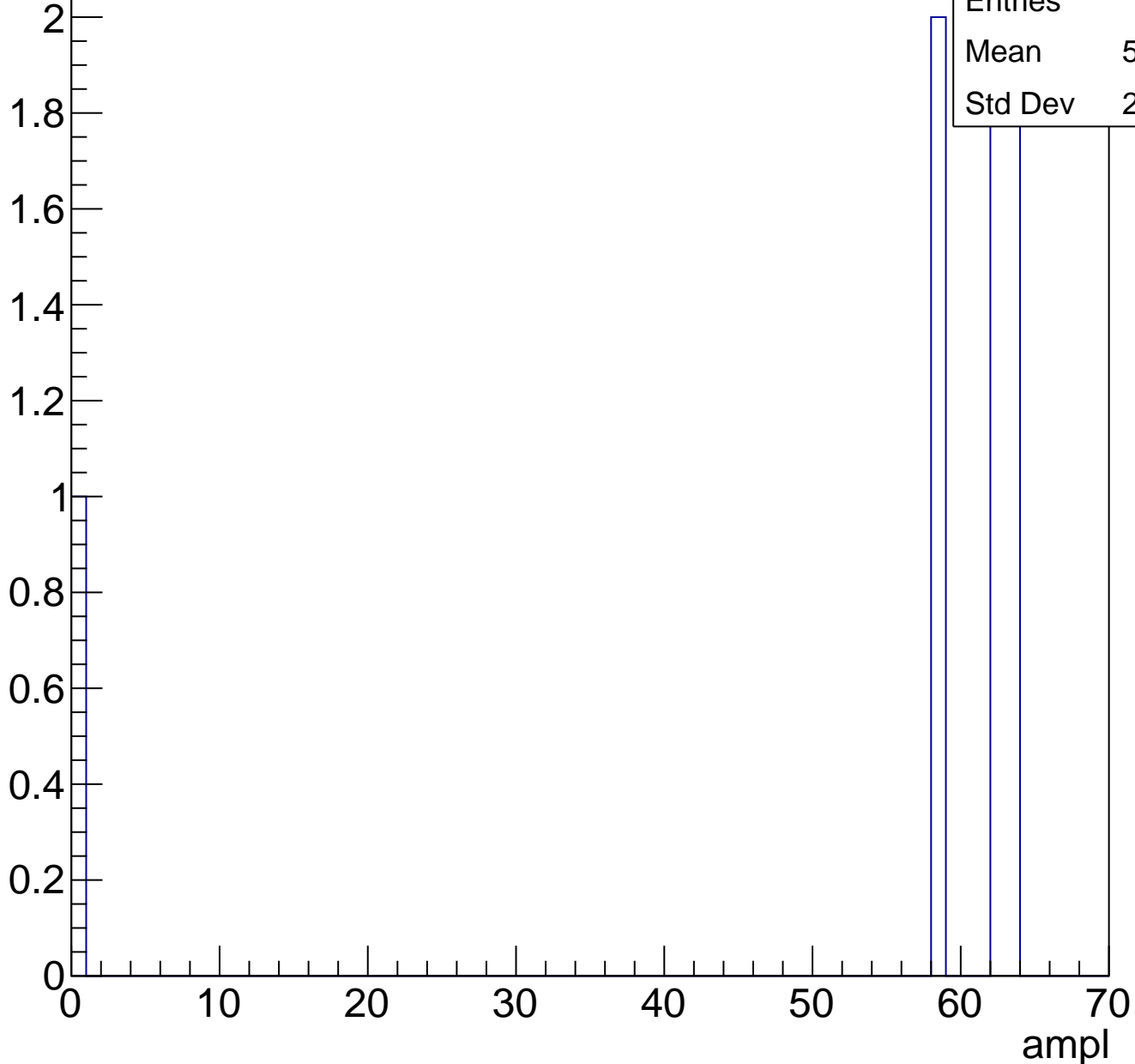
7

8

# B1L003S, U26-ch35, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch35, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L003S, U26-ch36, adc0

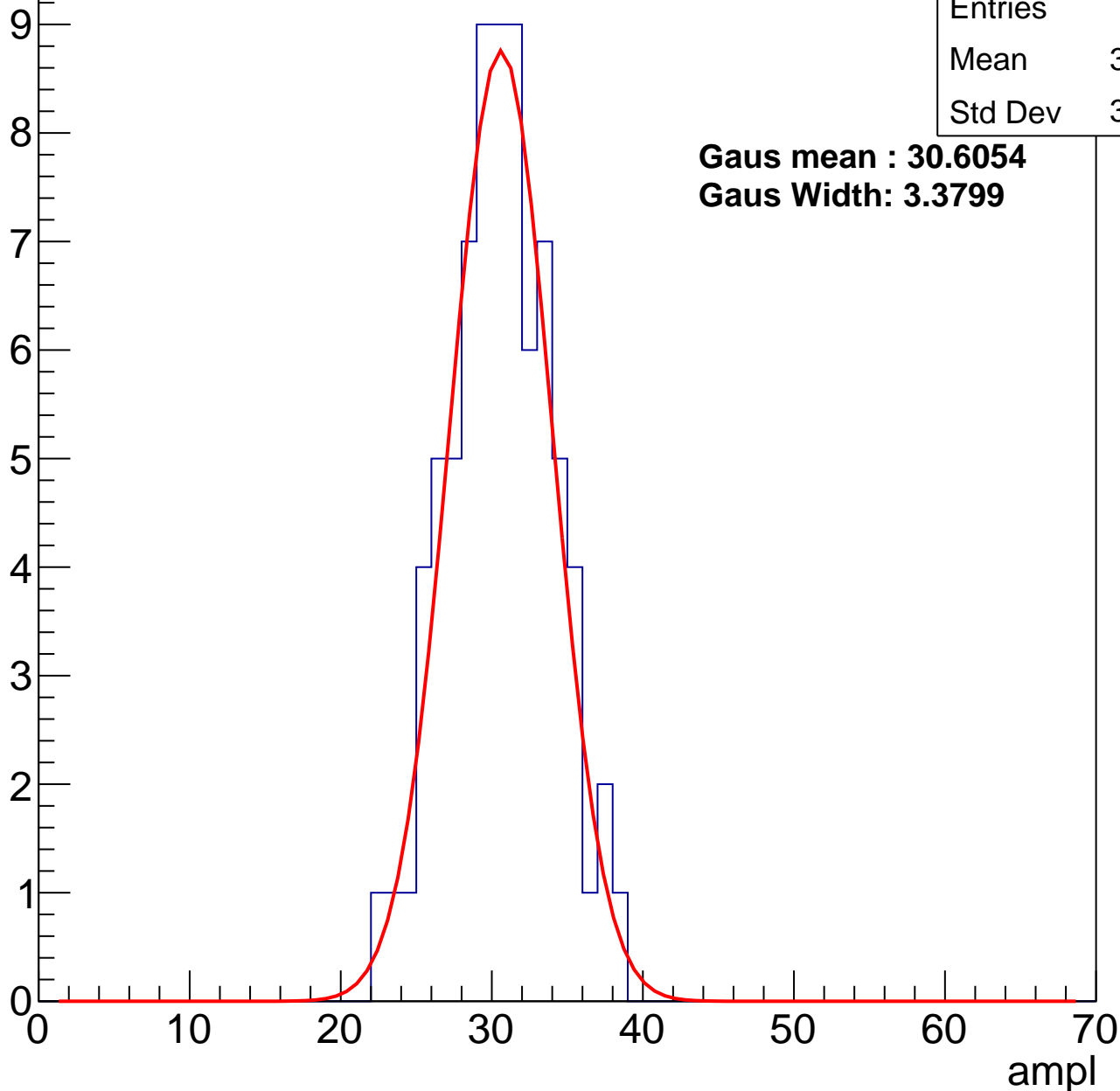
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	77
Mean	30.14
Std Dev	3.387

**Gaus mean : 30.6054**

**Gaus Width: 3.3799**



# B1L003S, U26-ch36, adc1

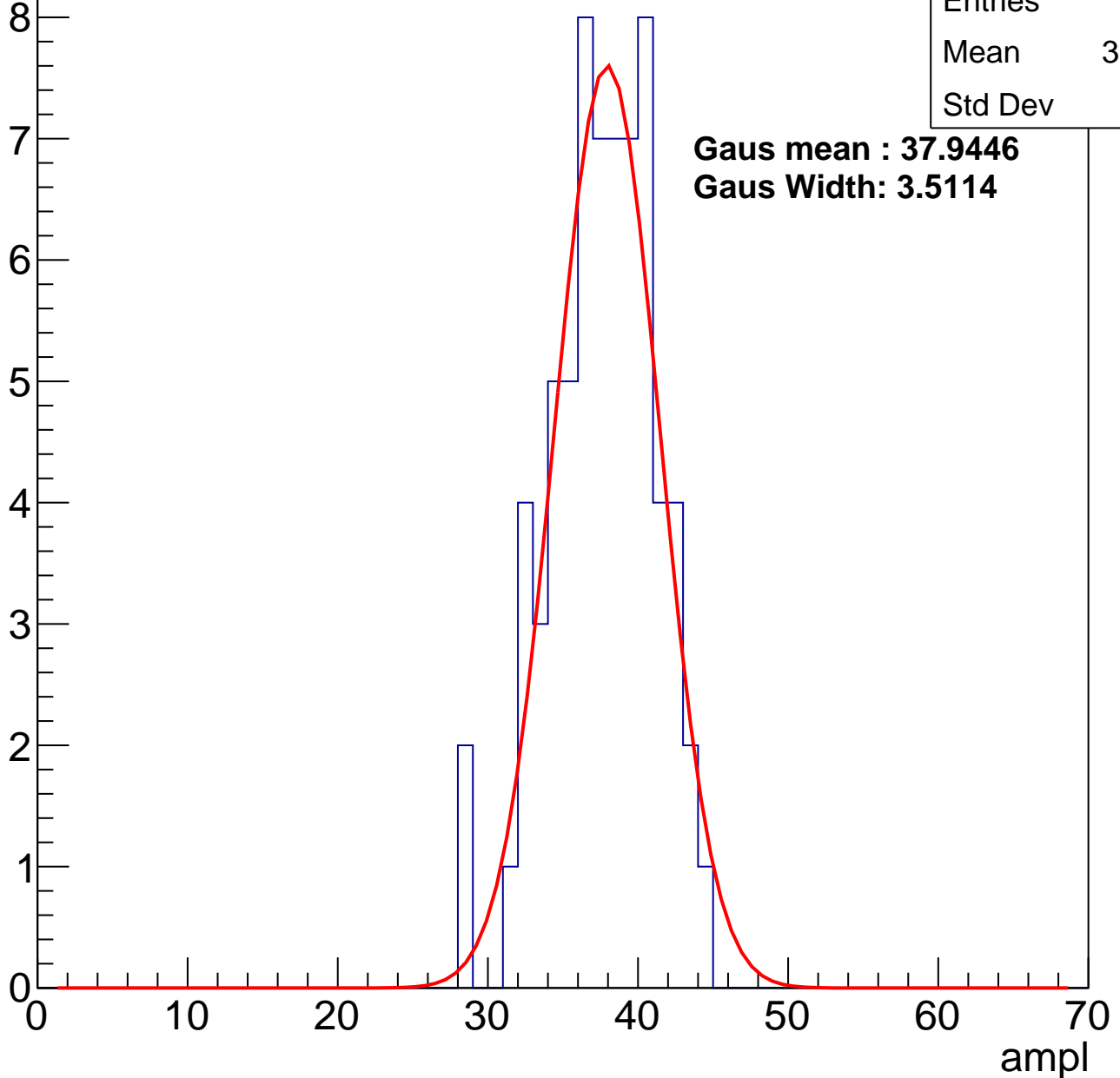
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	37.16
Std Dev	3.45

**Gaus mean : 37.9446**

**Gaus Width: 3.5114**

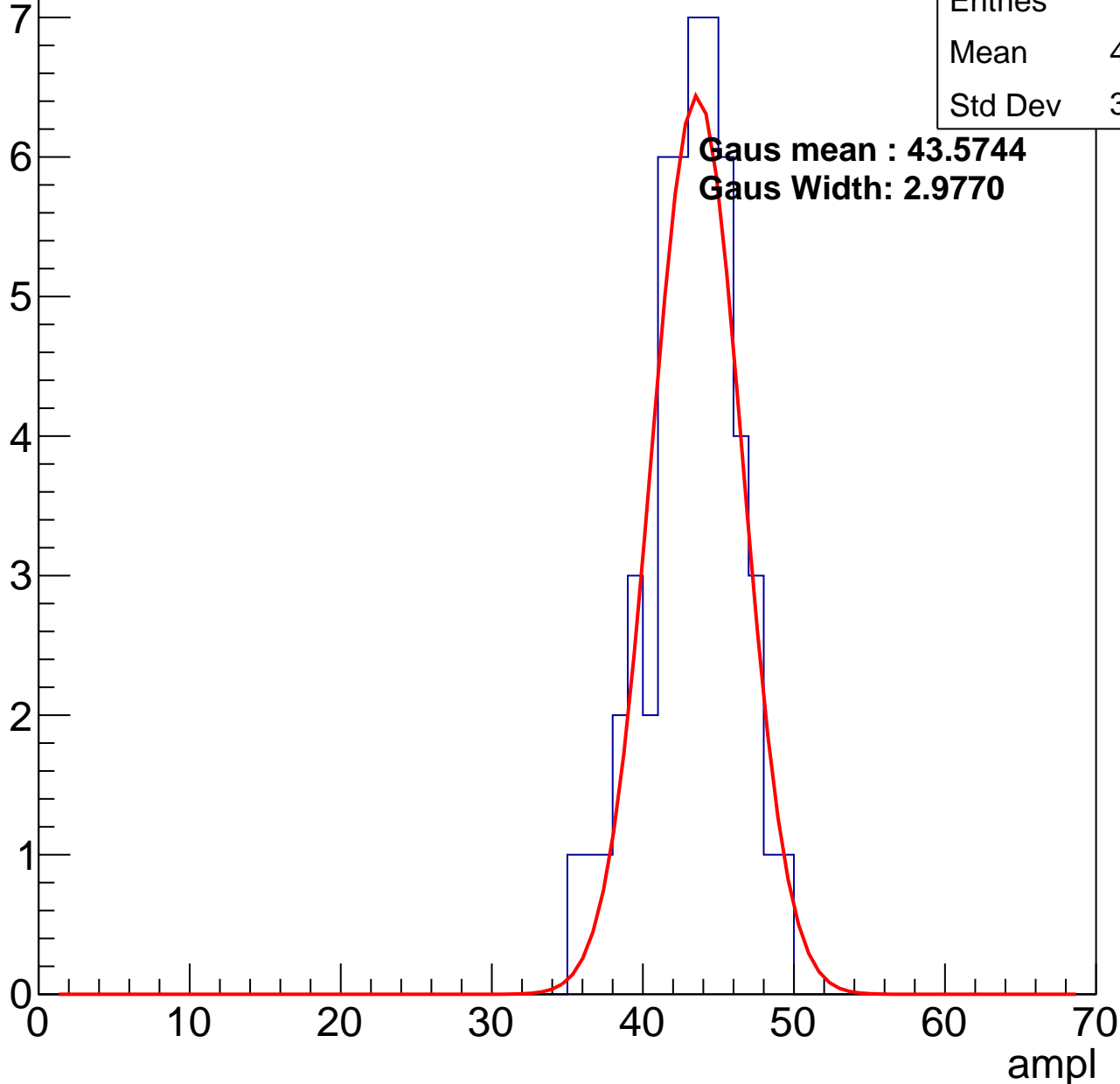


# B1L003S, U26-ch36, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	51
Mean	42.75
Std Dev	3.028

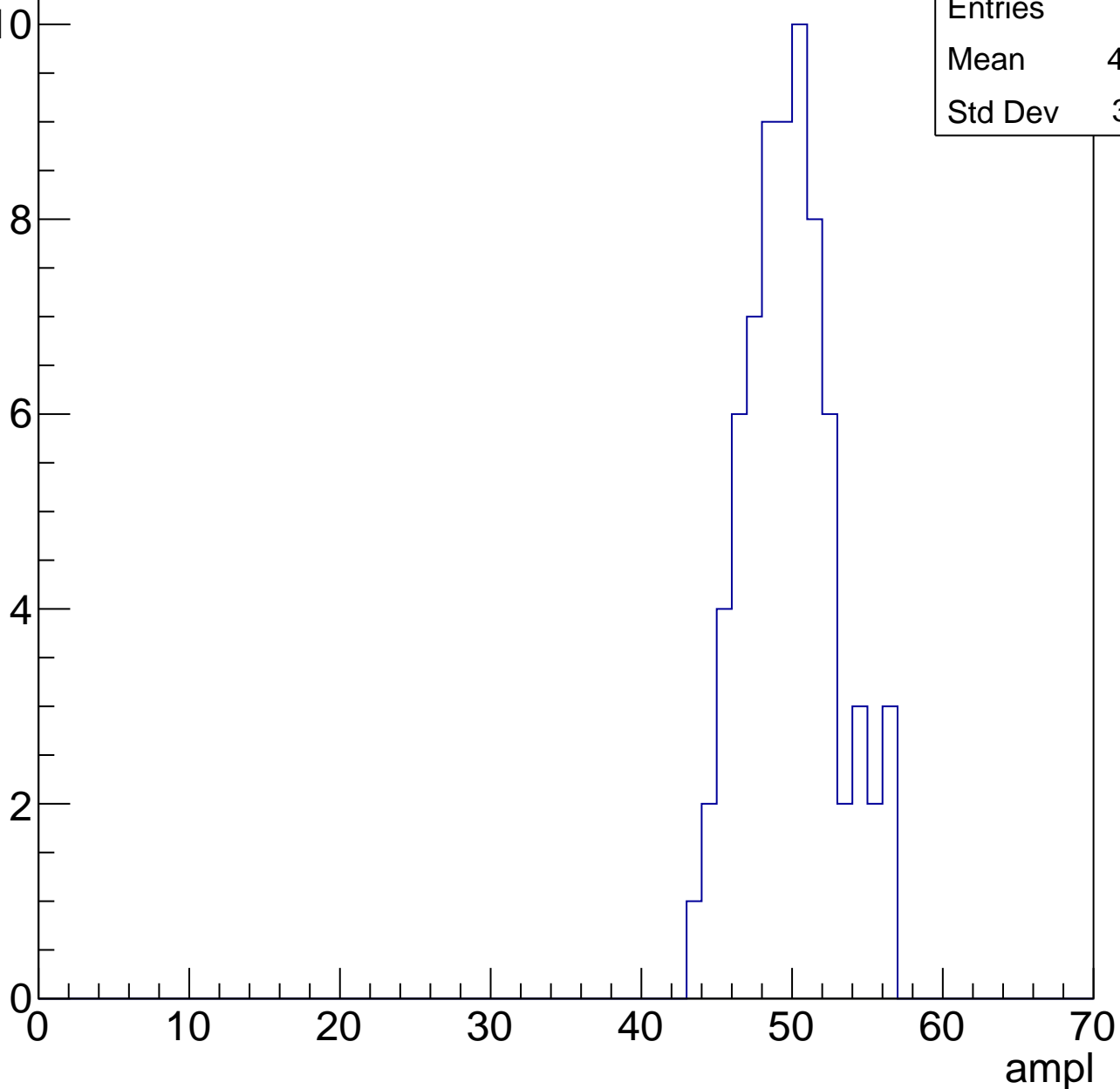


# B1L003S, U26-ch36, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	72
Mean	49.38
Std Dev	3.011

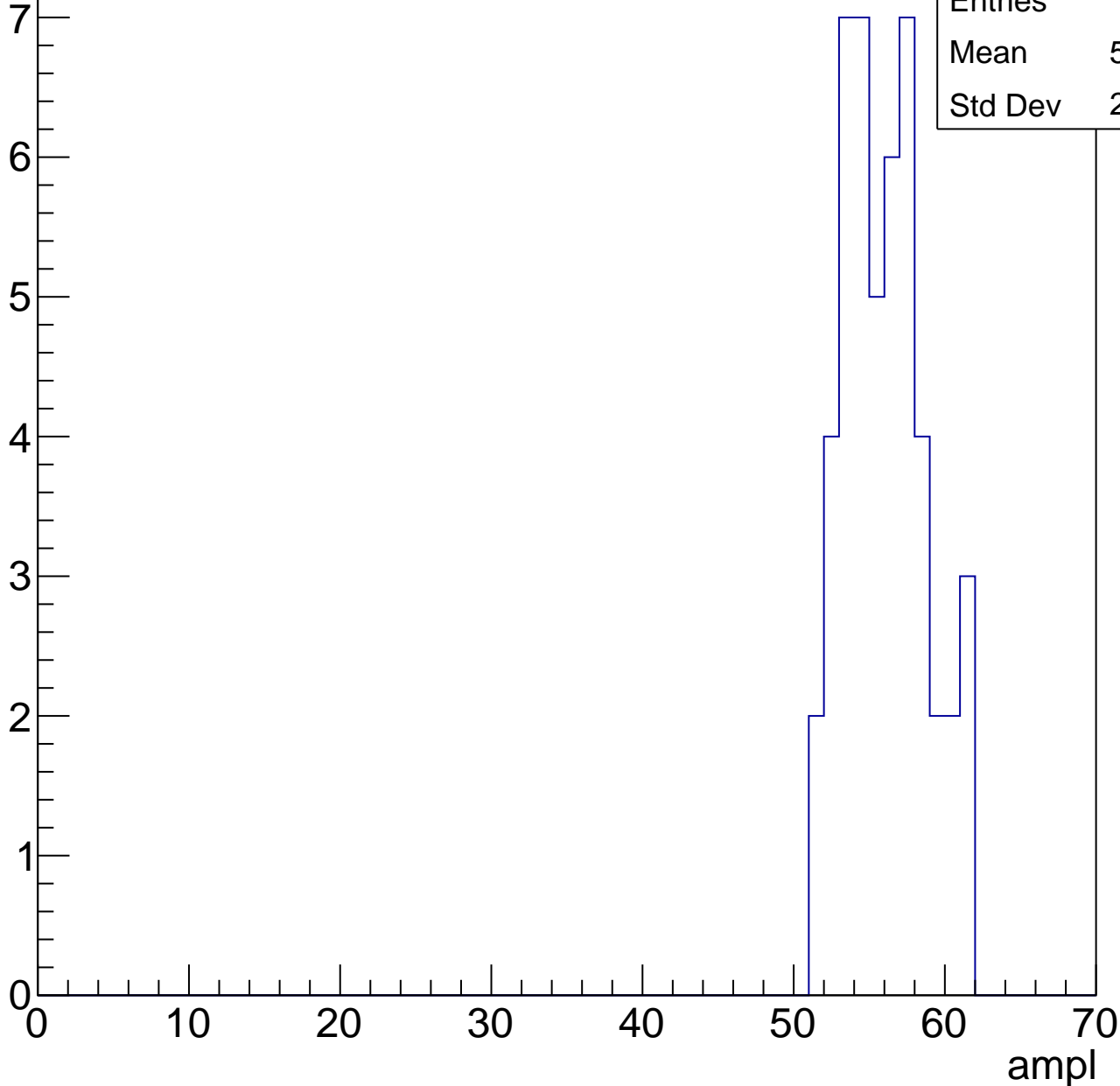


# B1L003S, U26-ch36, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

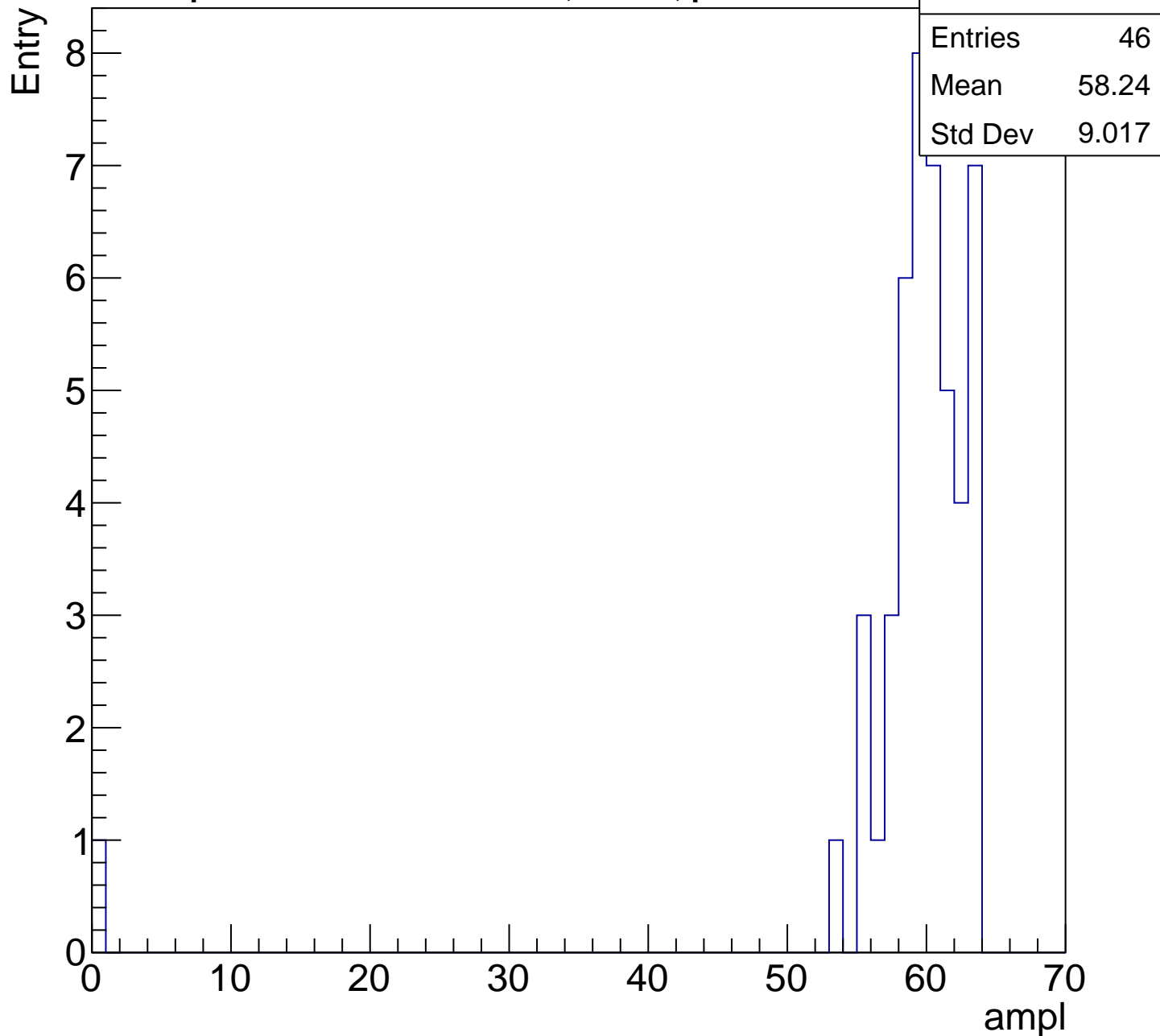
Entry

Entries	49
Mean	55.55
Std Dev	2.665



# B1L003S, U26-ch36, adc5

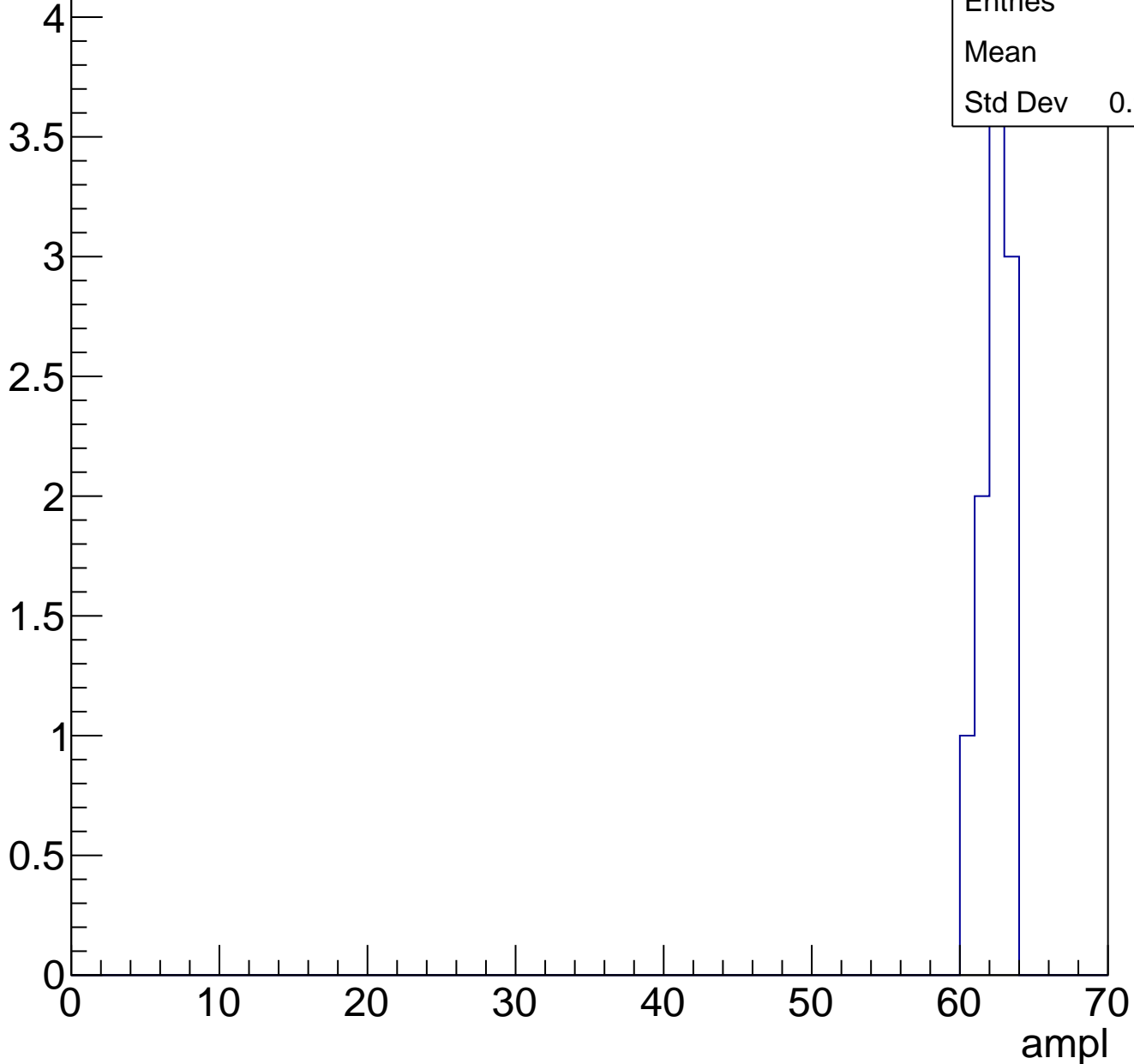
calib\_packv5\_042523\_0143.root, FC#13, port D2



# B1L003S, U26-ch36, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch36, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	48.67
Std Dev	18.86

0 10 20 30 40 50 60 70

ampl

22 62 63

# B1L003S, U26-ch37, adc0

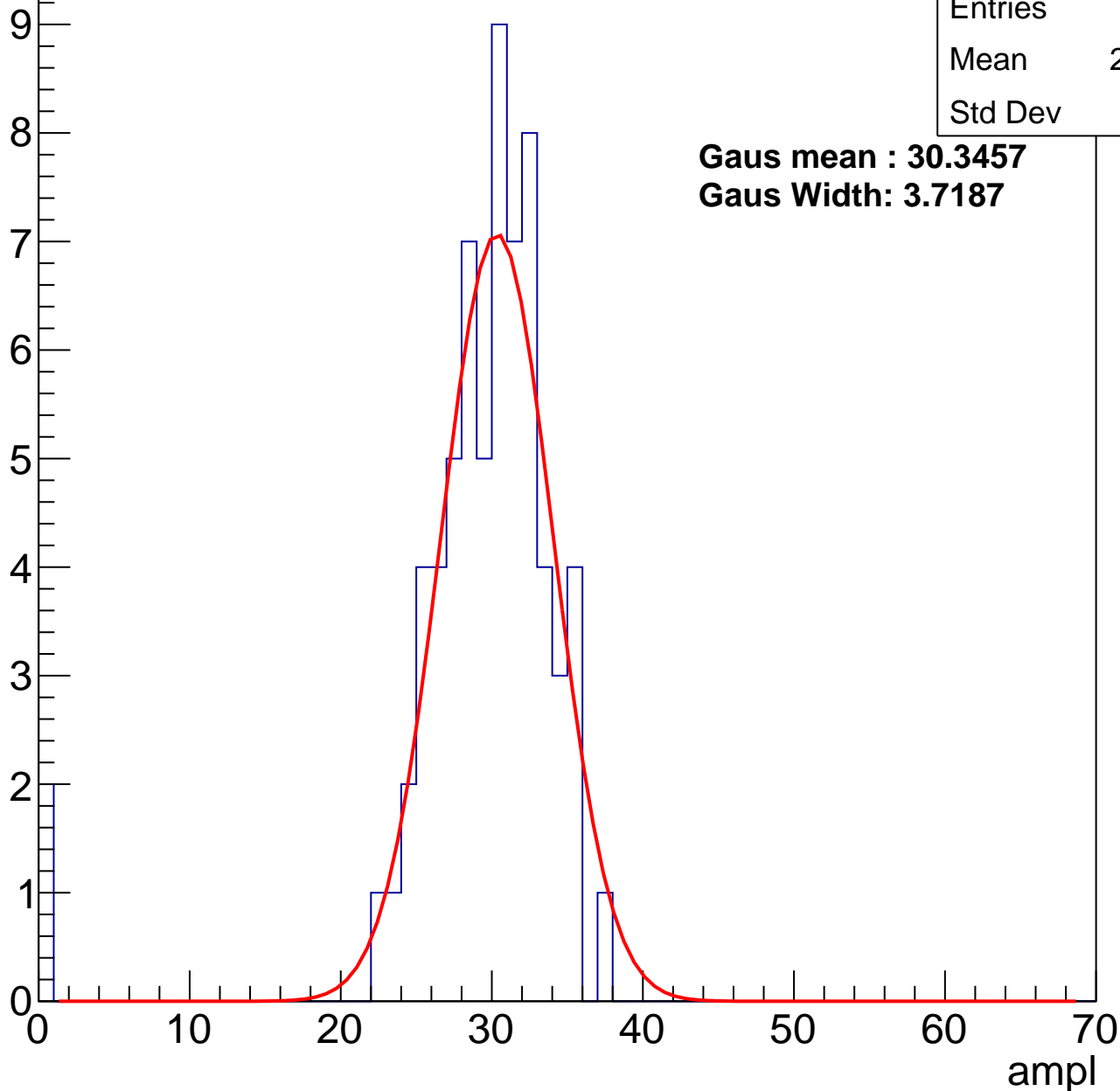
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	28.76
Std Dev	5.98

**Gaus mean : 30.3457**

**Gaus Width: 3.7187**



# B1L003S, U26-ch37, adc1

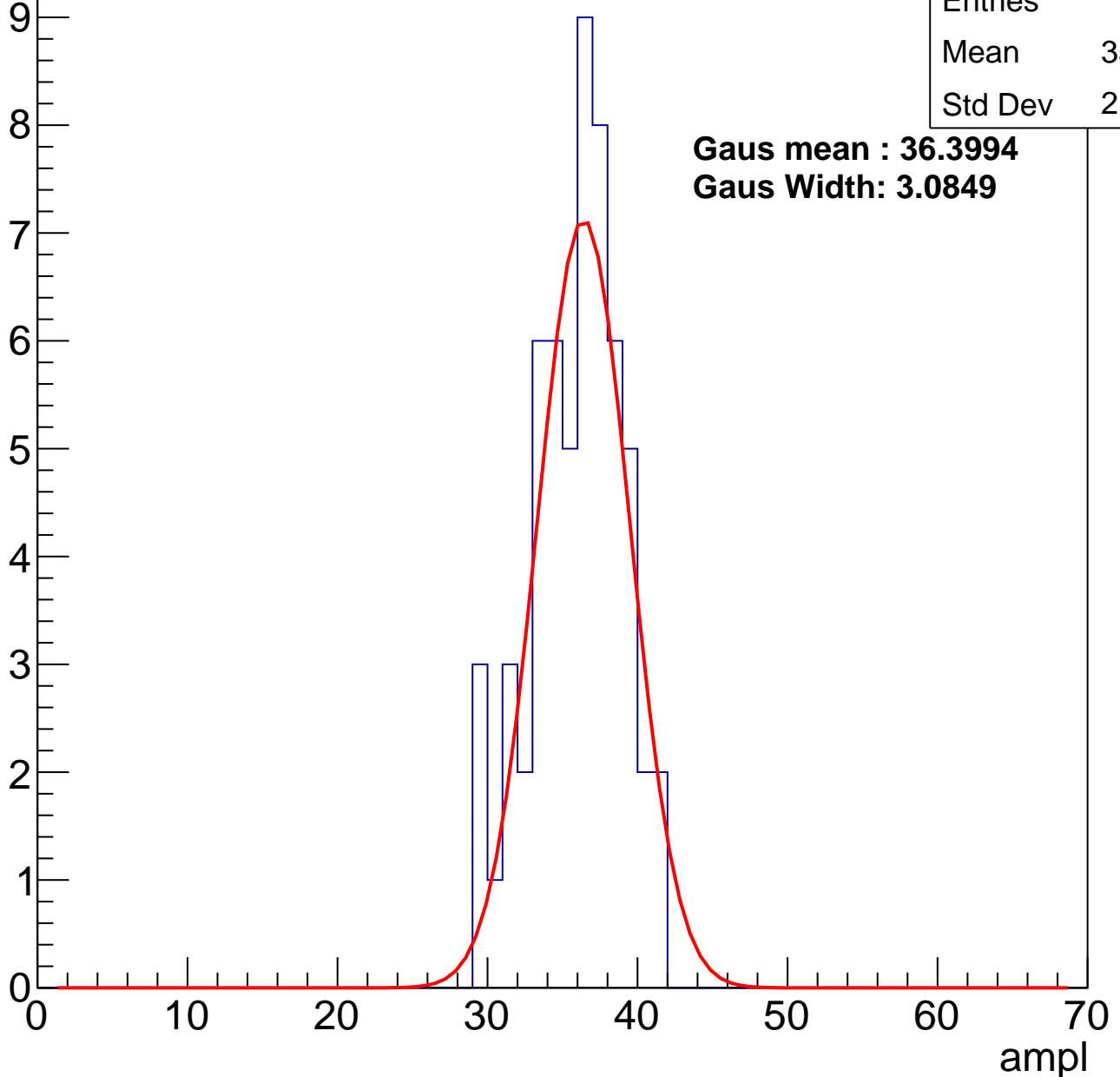
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	35.45
Std Dev	2.978

**Gaus mean : 36.3994**

**Gaus Width: 3.0849**



# B1L003S, U26-ch37, adc2

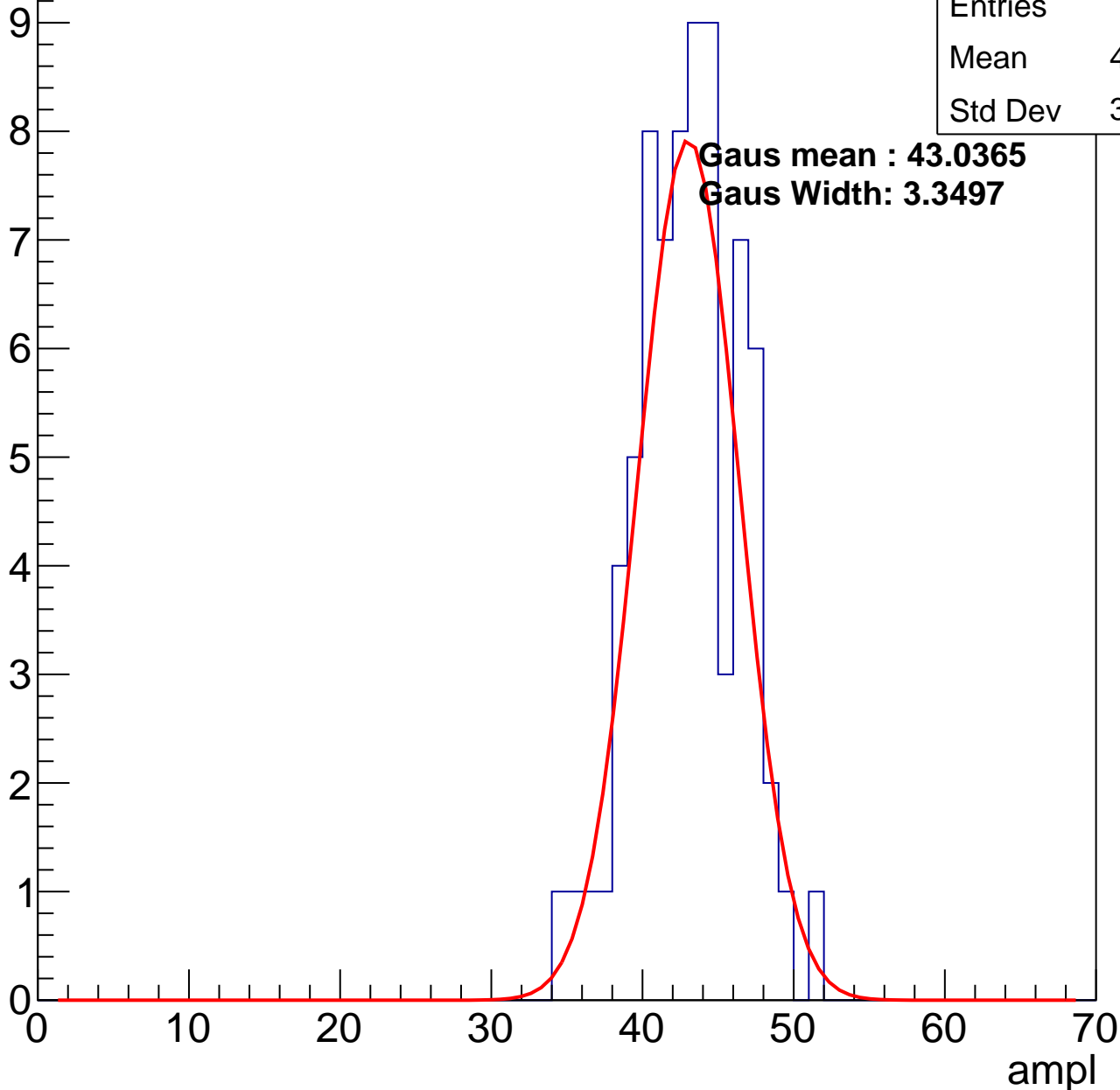
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	74
Mean	42.57
Std Dev	3.357

**Gaus mean : 43.0365**

**Gaus Width: 3.3497**

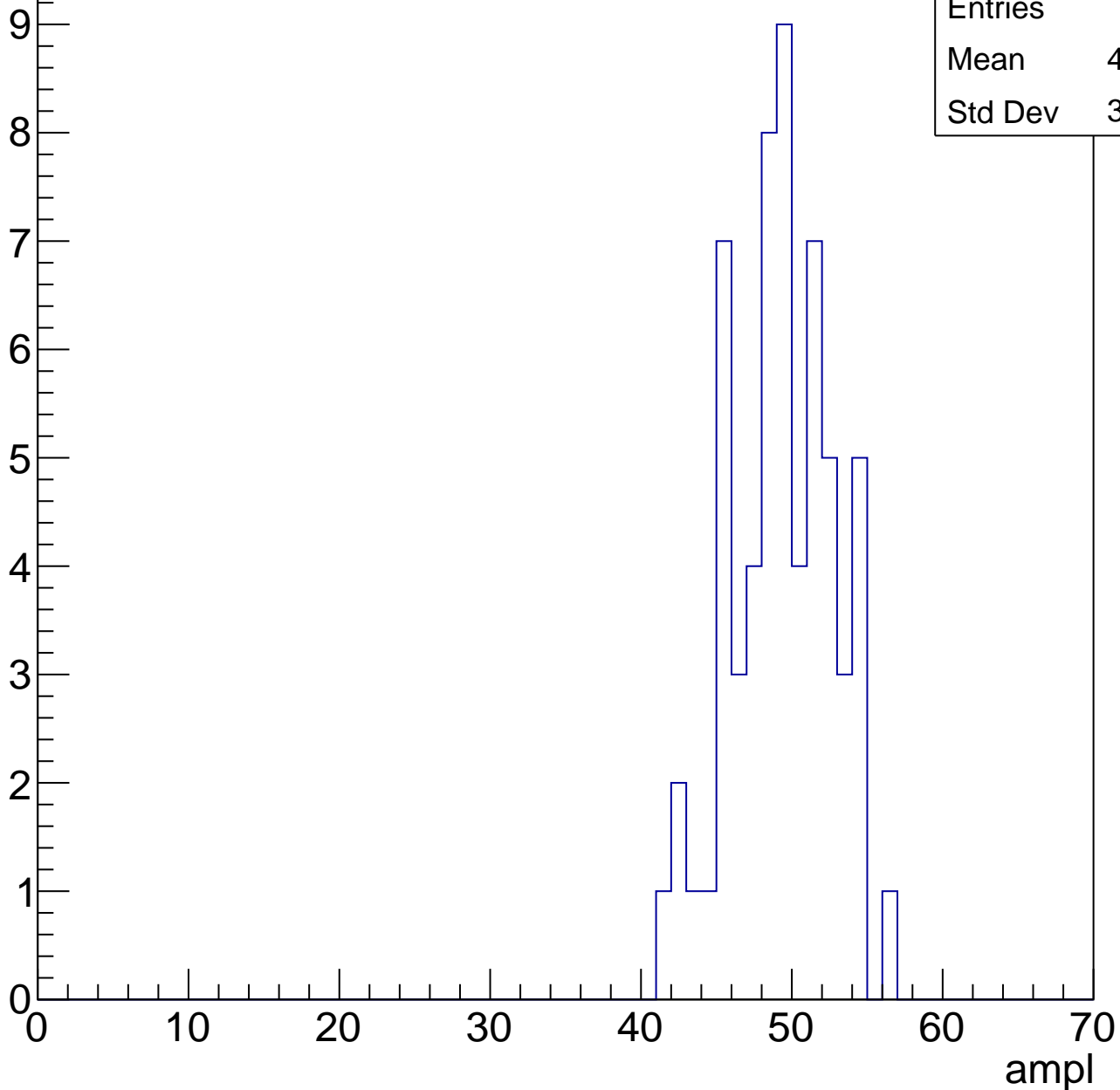


# B1L003S, U26-ch37, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	48.85
Std Dev	3.348

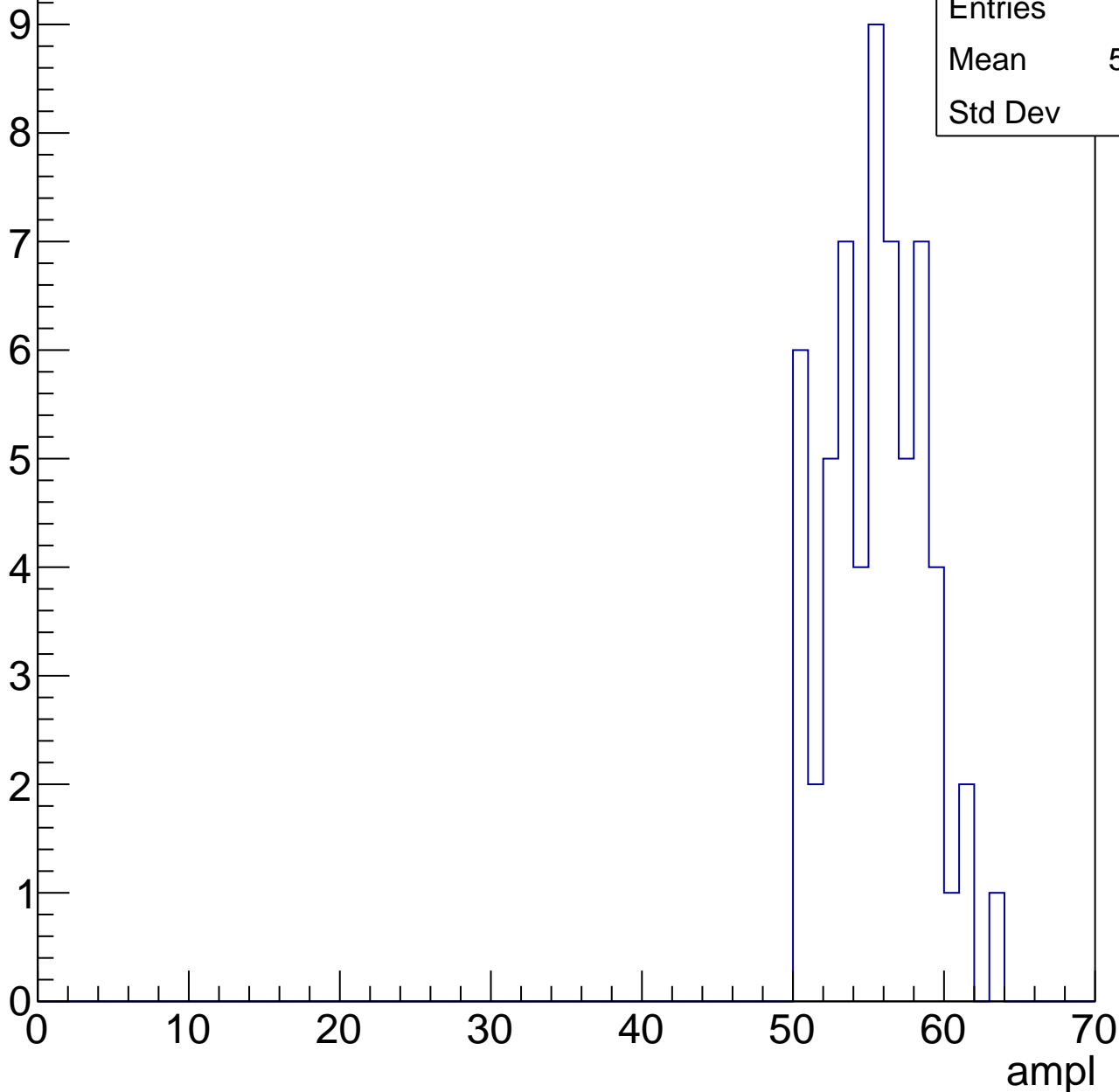


# B1L003S, U26-ch37, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	55.13
Std Dev	3.09



# B1L003S, U26-ch37, adc5

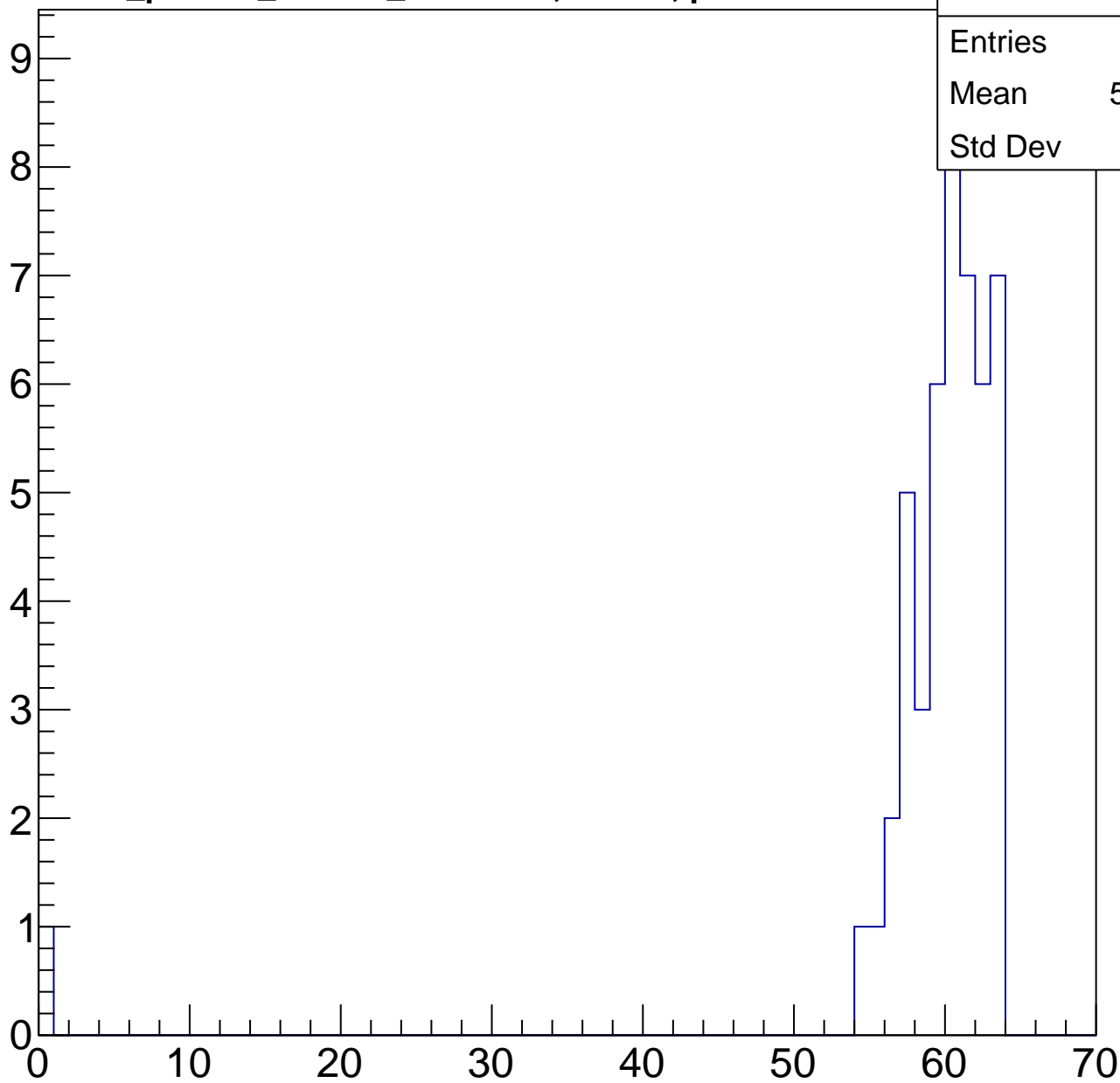
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	48
Mean	58.62
Std Dev	8.85

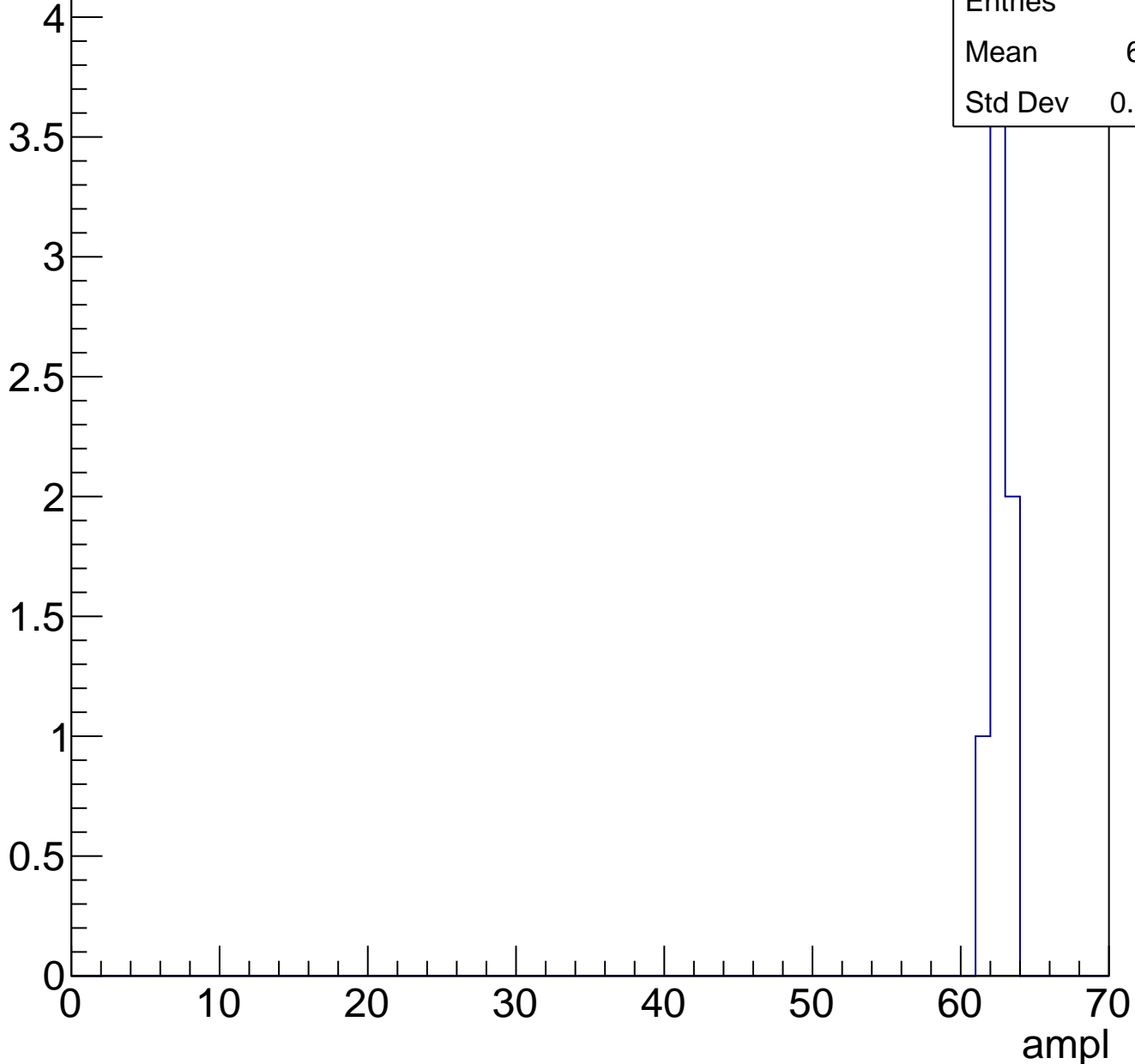
ampl



# B1L003S, U26-ch37, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch37, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U26-ch38, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	51
Mean	29.78
Std Dev	2.404

**Gaus mean : 29.9826**

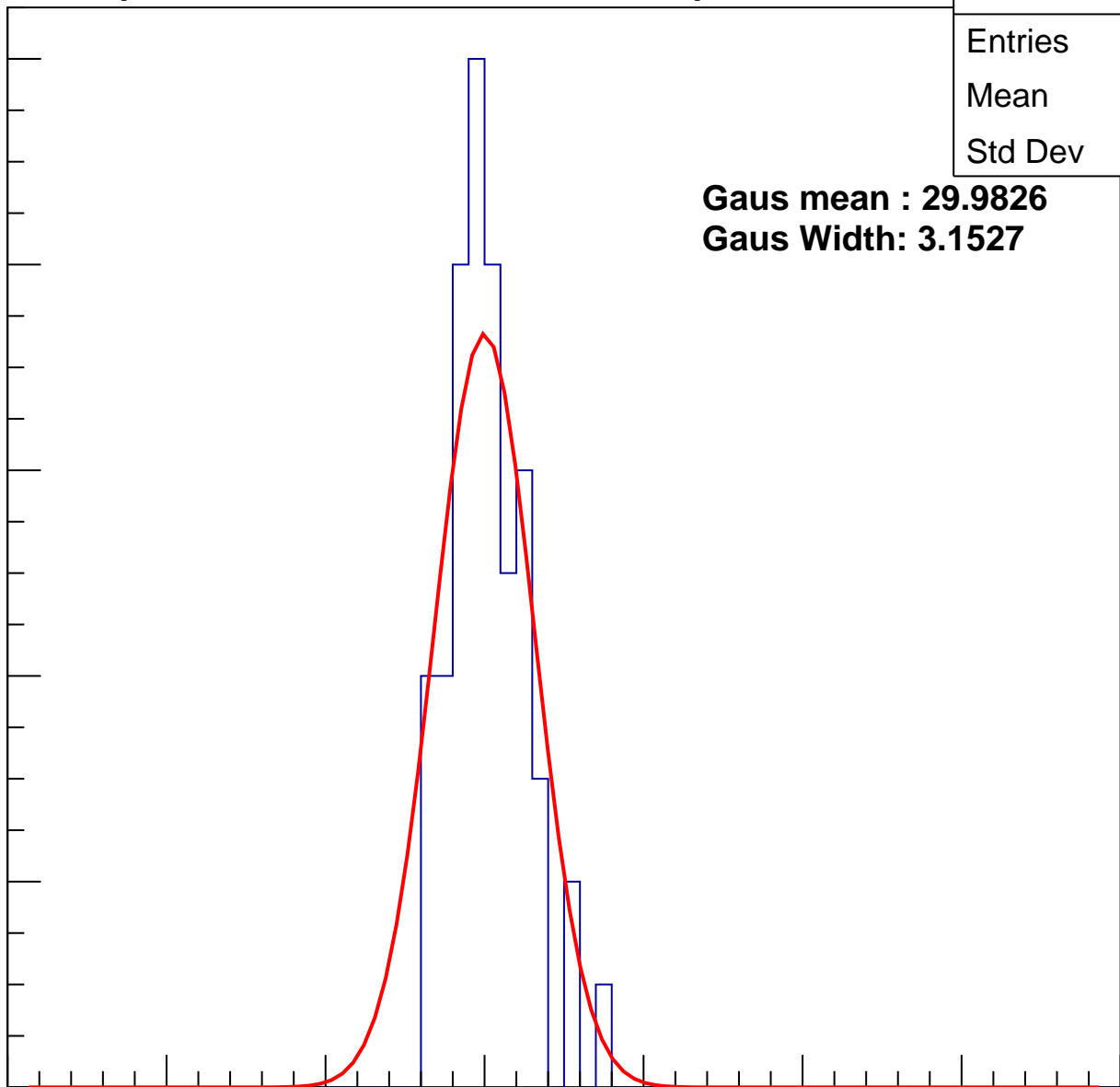
**Gaus Width: 3.1527**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



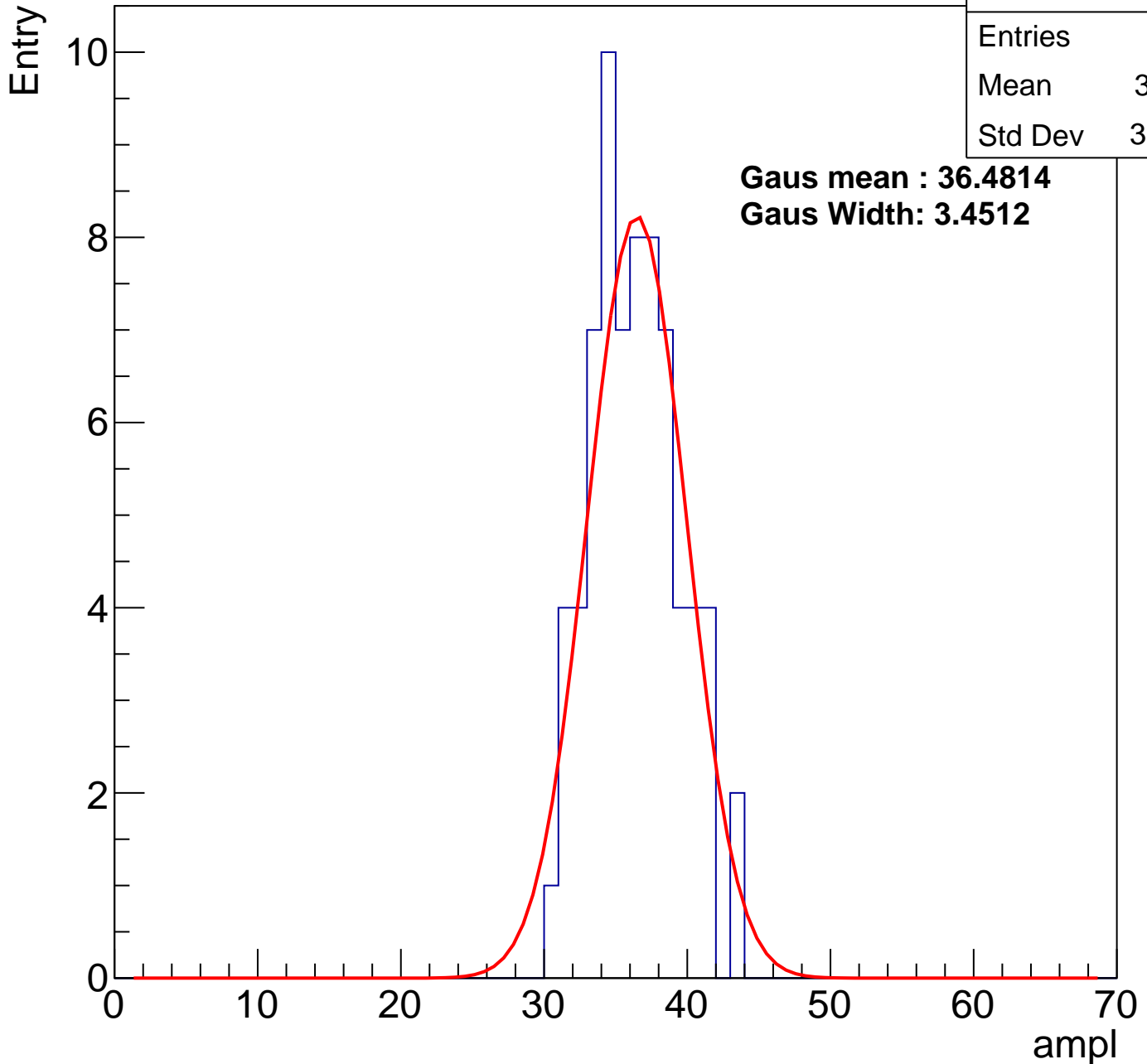
# B1L003S, U26-ch38, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	70
Mean	35.91
Std Dev	3.032

**Gaus mean : 36.4814**

**Gaus Width: 3.4512**

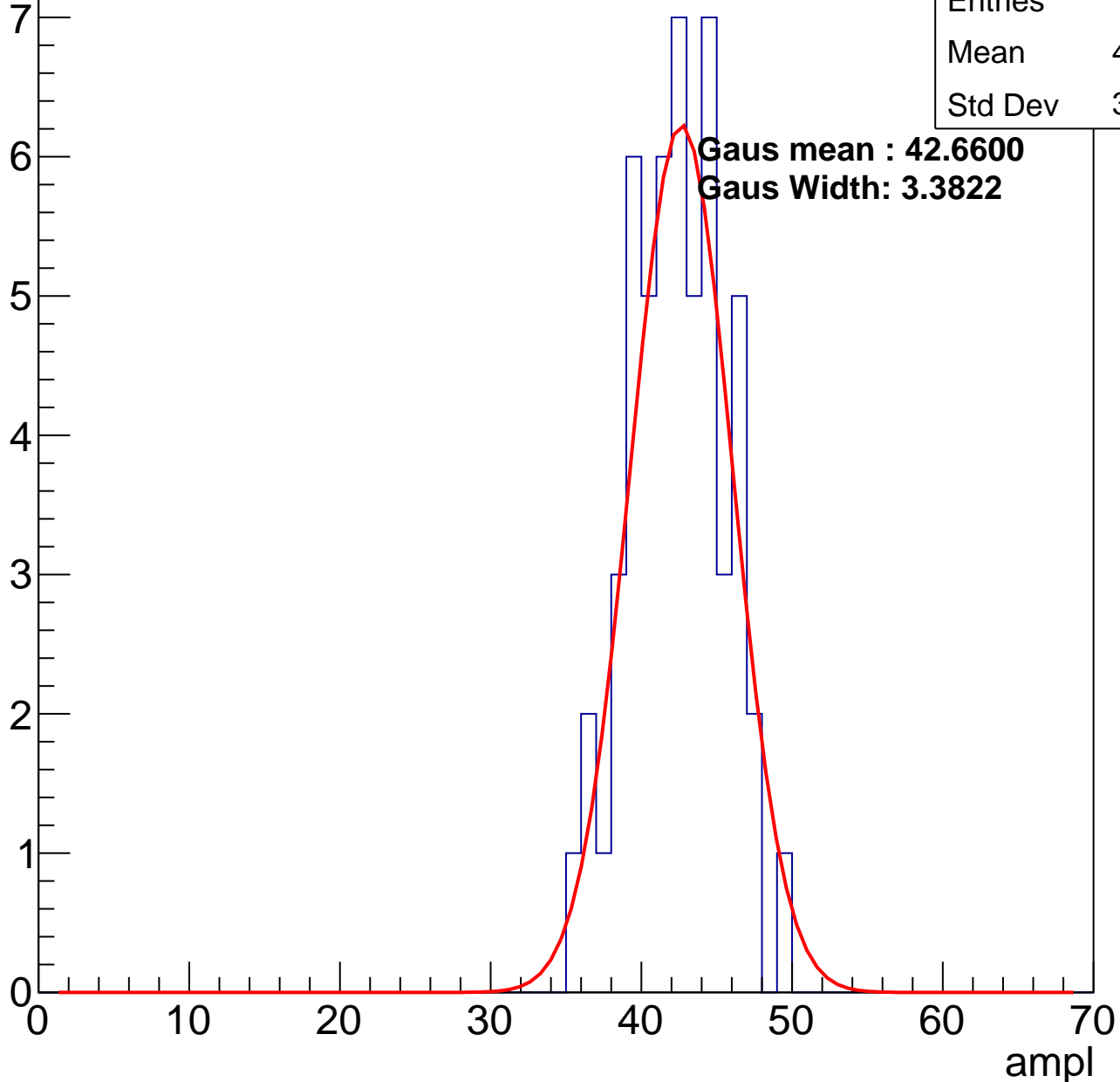


# B1L003S, U26-ch38, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	54
Mean	41.91
Std Dev	3.081

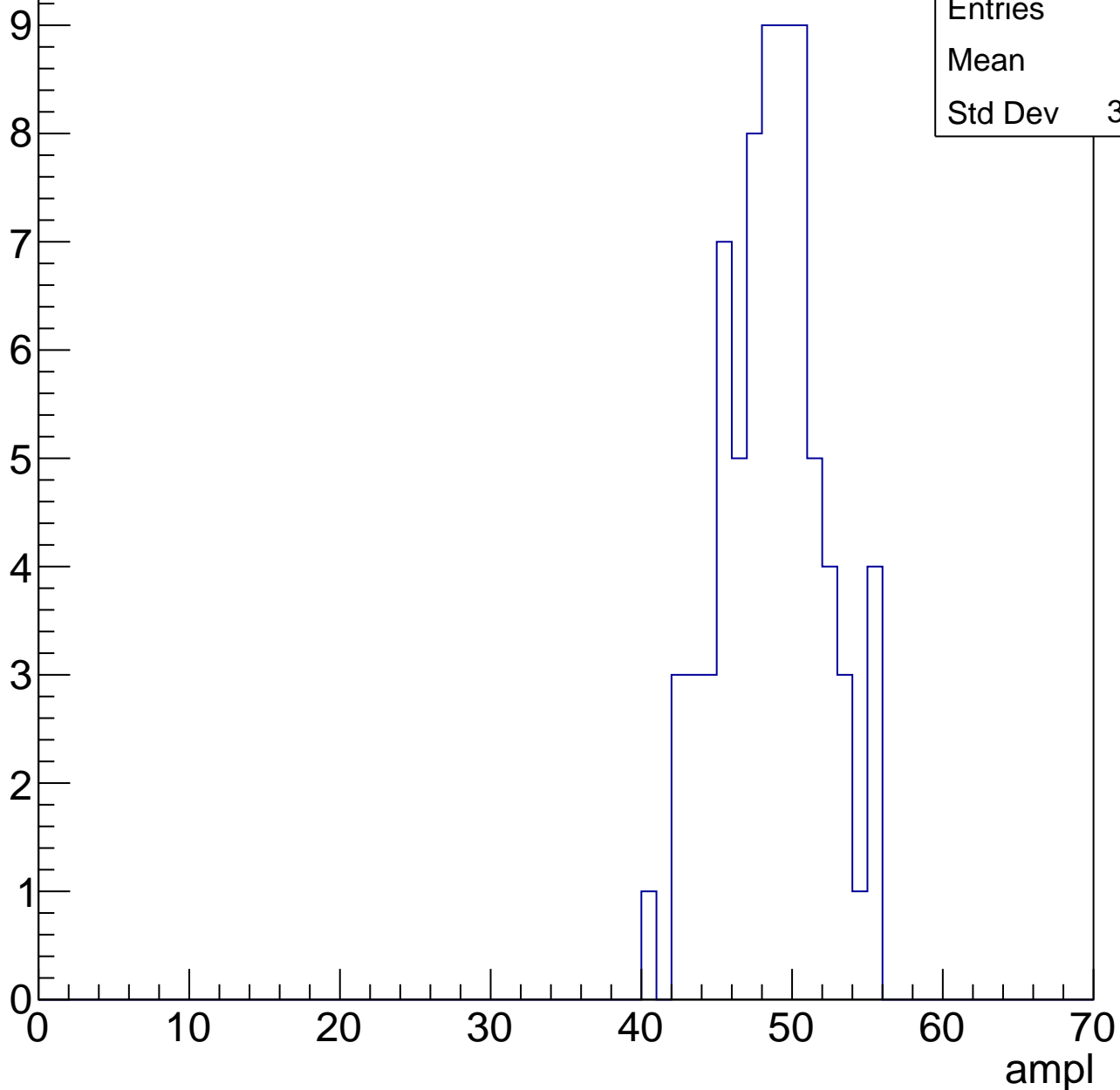


# B1L003S, U26-ch38, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

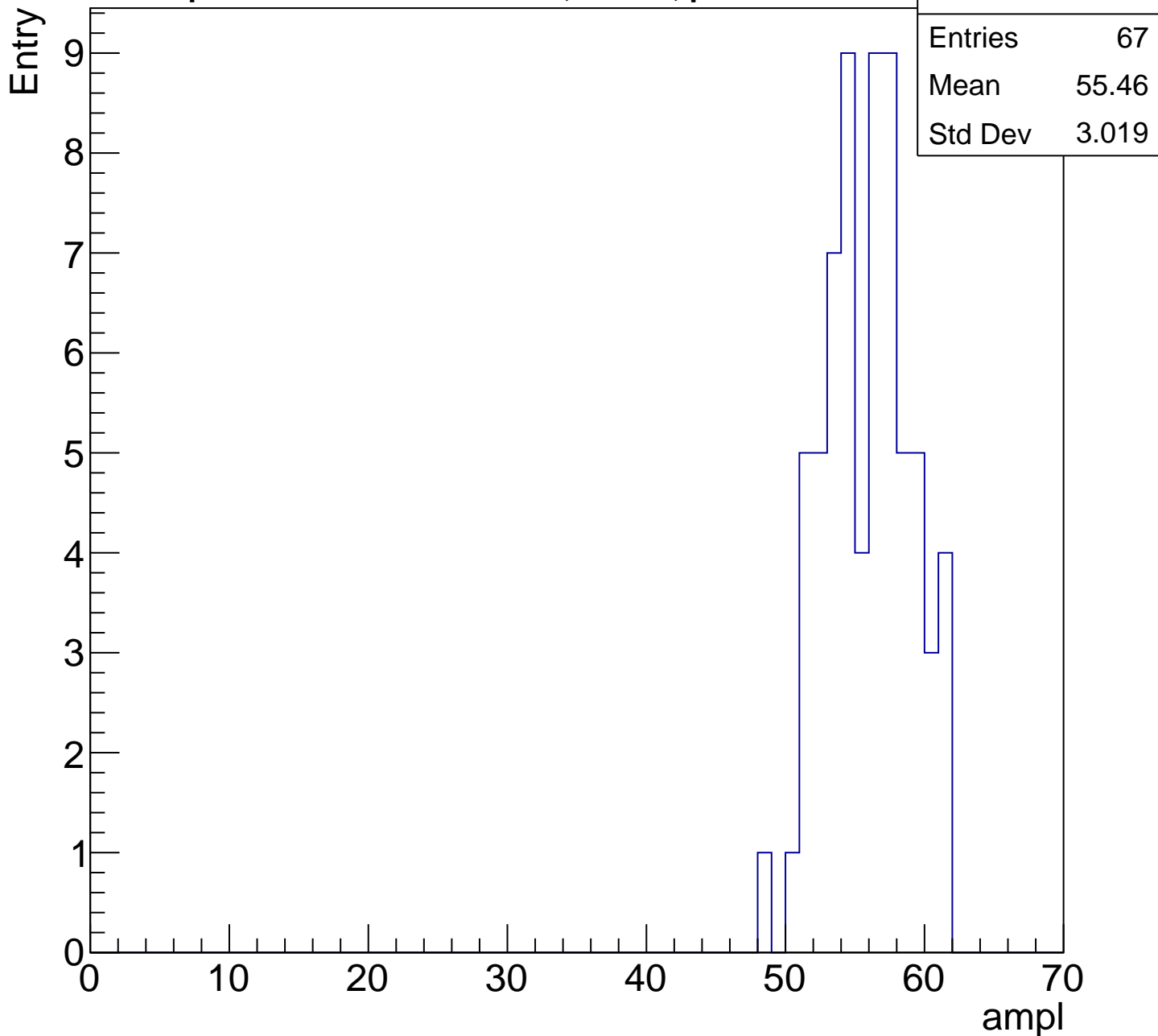
Entry

Entries	74
Mean	48.2
Std Dev	3.377



# B1L003S, U26-ch38, adc4

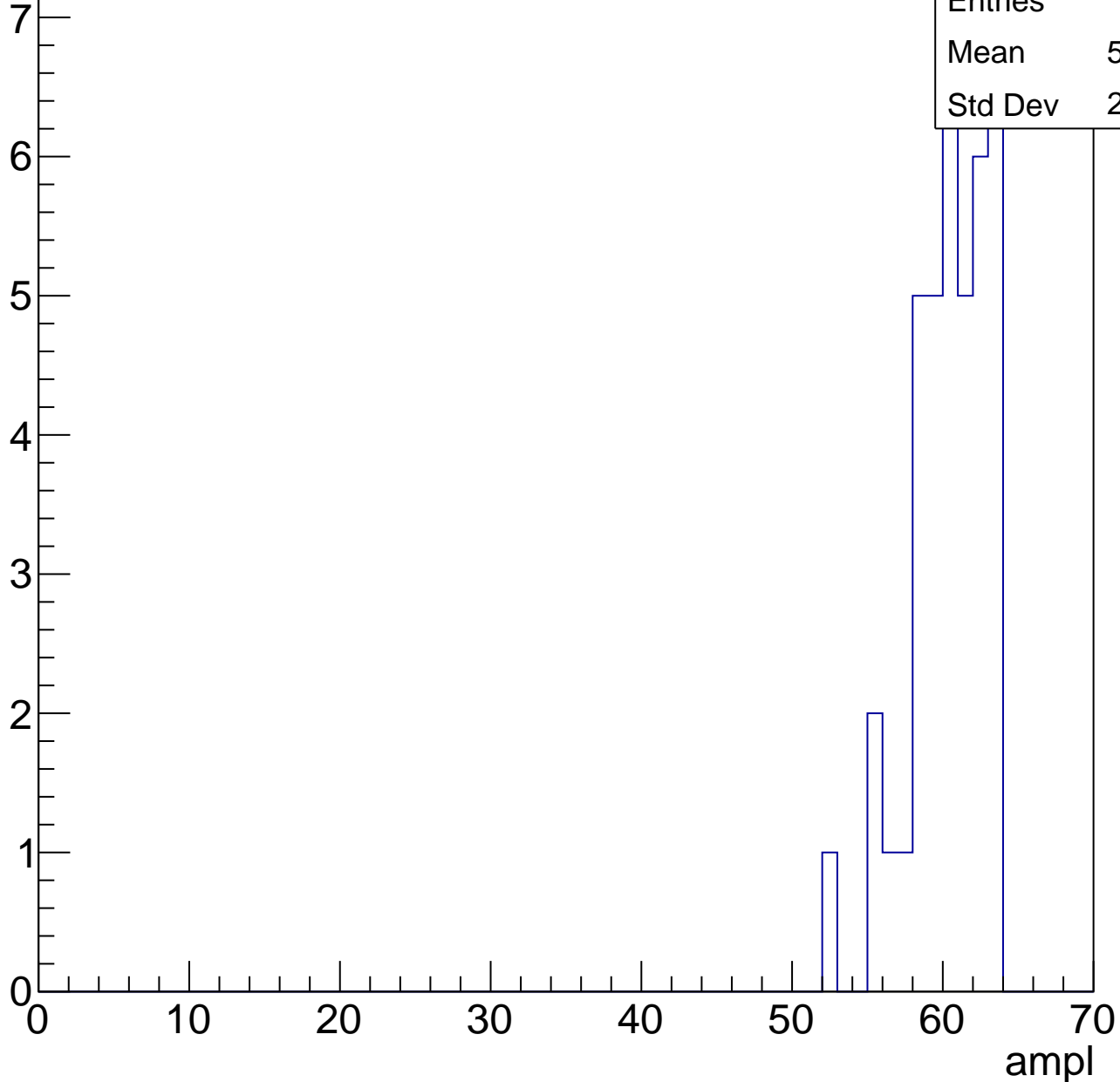
calib\_packv5\_042523\_0143.root, FC#13, port D2



# B1L003S, U26-ch38, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

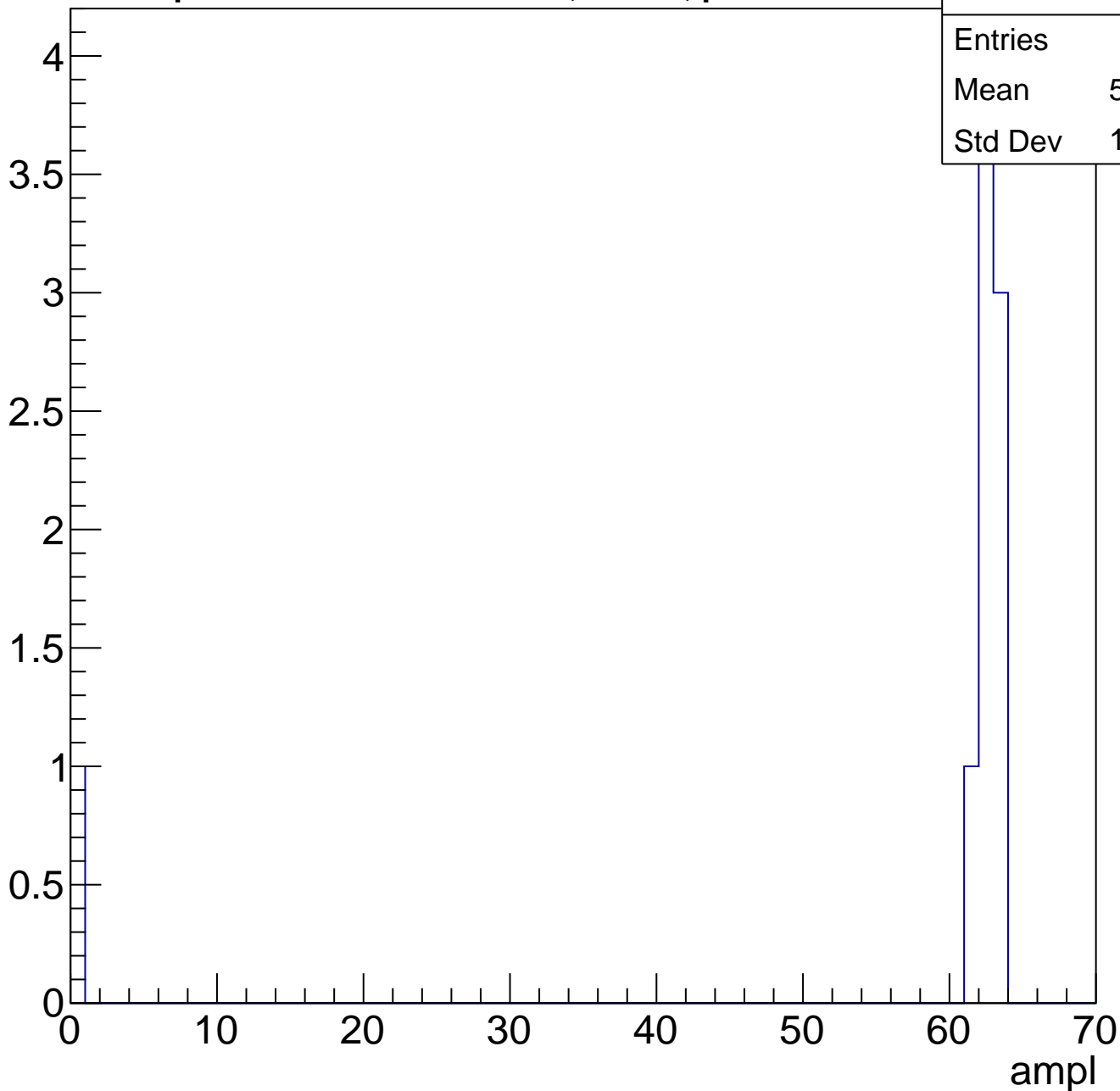
Entry



# B1L003S, U26-ch38, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

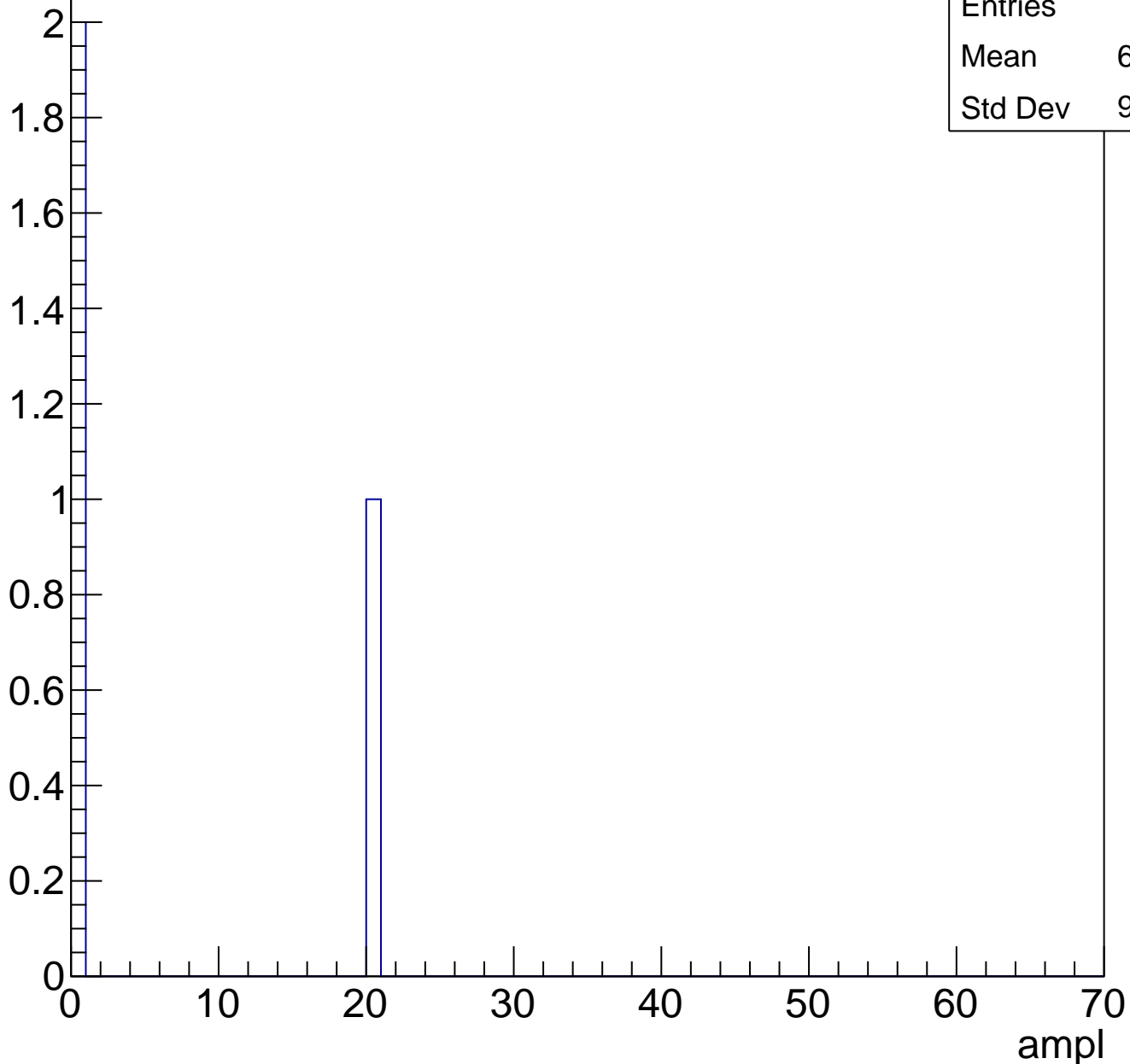




# B1L003S, U26-ch38, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	3
Mean	6.667
Std Dev	9.428

# B1L003S, U26-ch39, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	72
Mean	29.69
Std Dev	4.713

**Gaus mean : 30.8491**

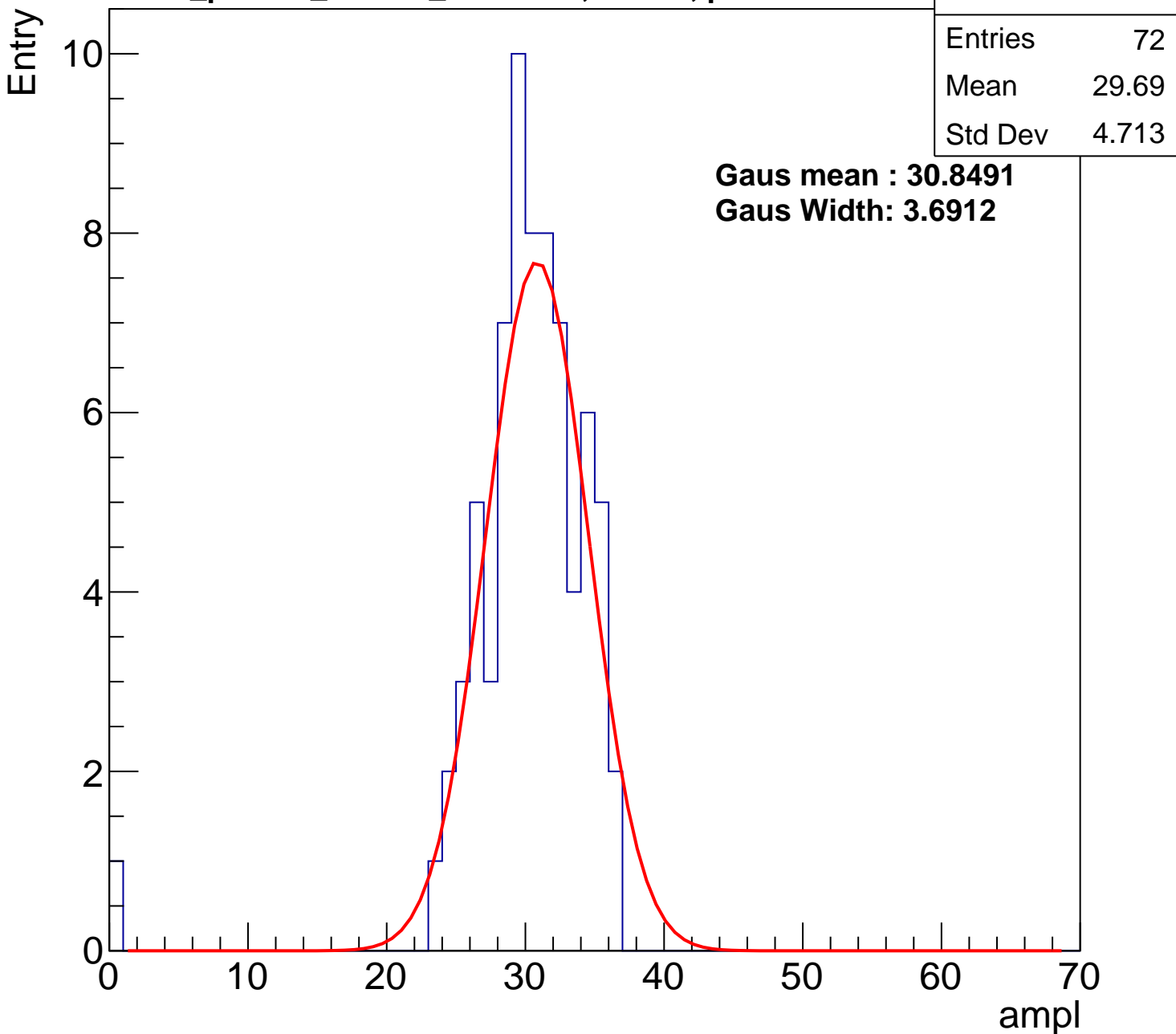
**Gaus Width: 3.6912**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U26-ch39, adc1

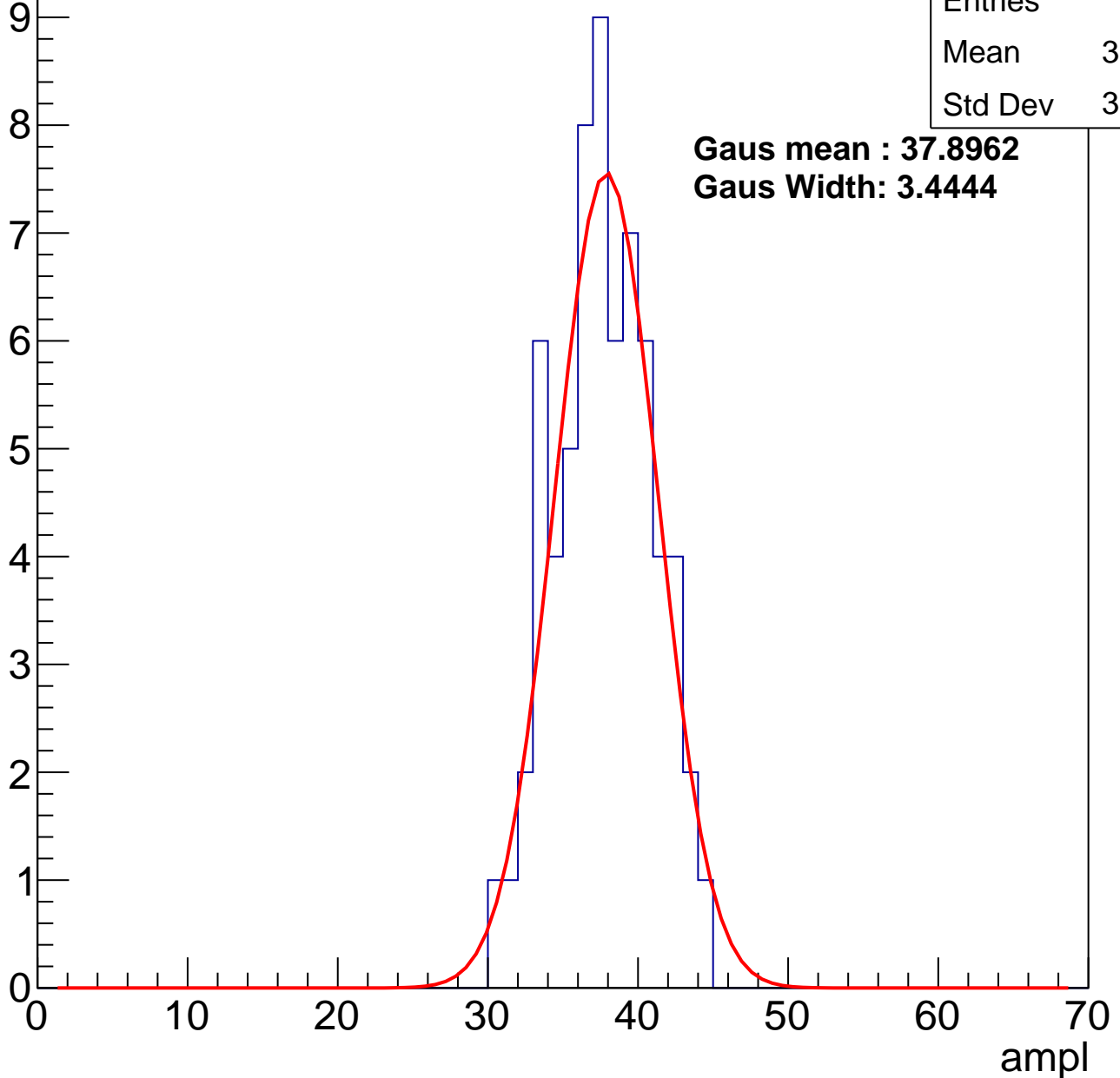
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	37.24
Std Dev	3.172

**Gaus mean : 37.8962**

**Gaus Width: 3.4444**



# B1L003S, U26-ch39, adc2

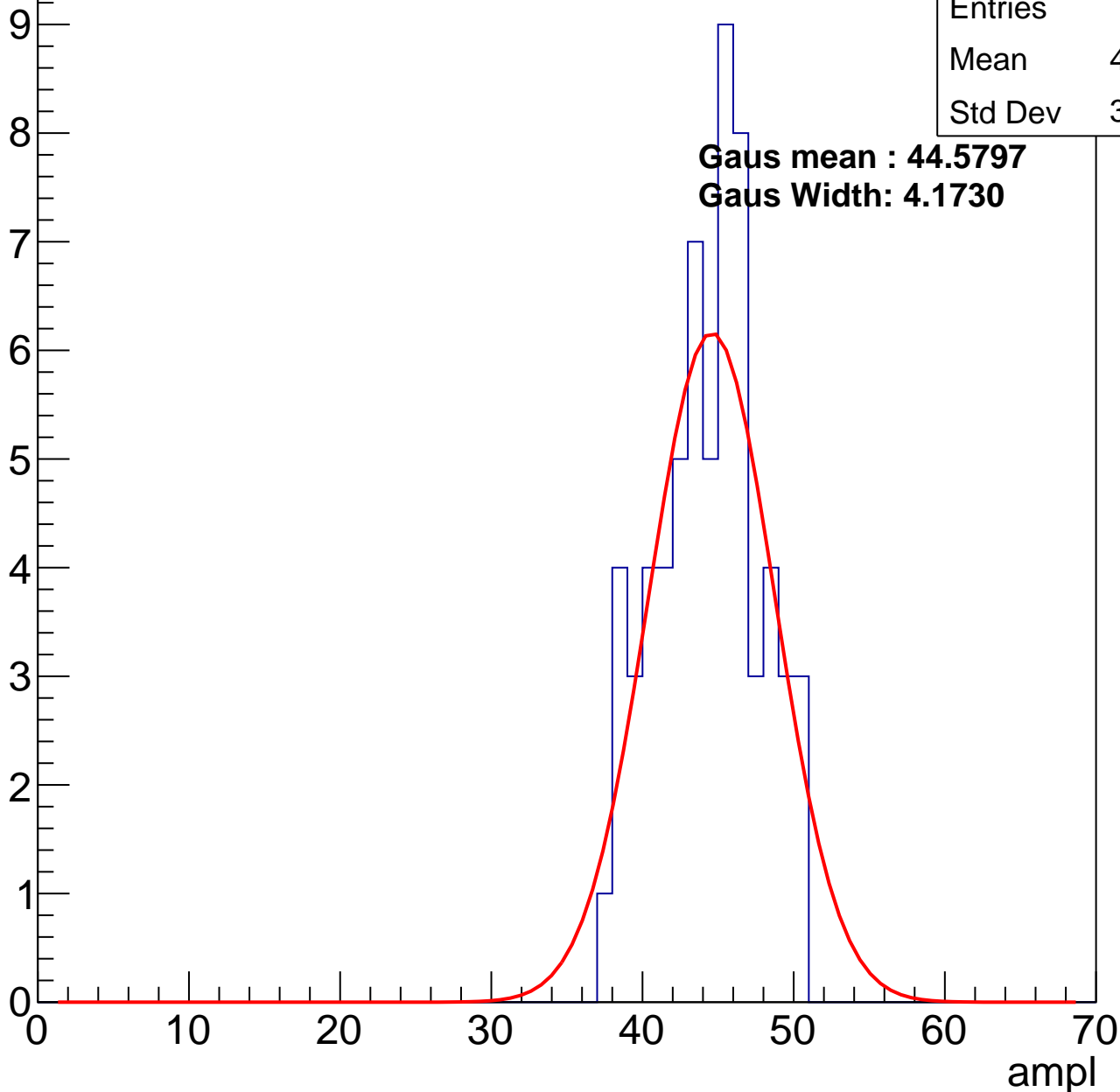
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	43.87
Std Dev	3.355

**Gaus mean : 44.5797**

**Gaus Width: 4.1730**

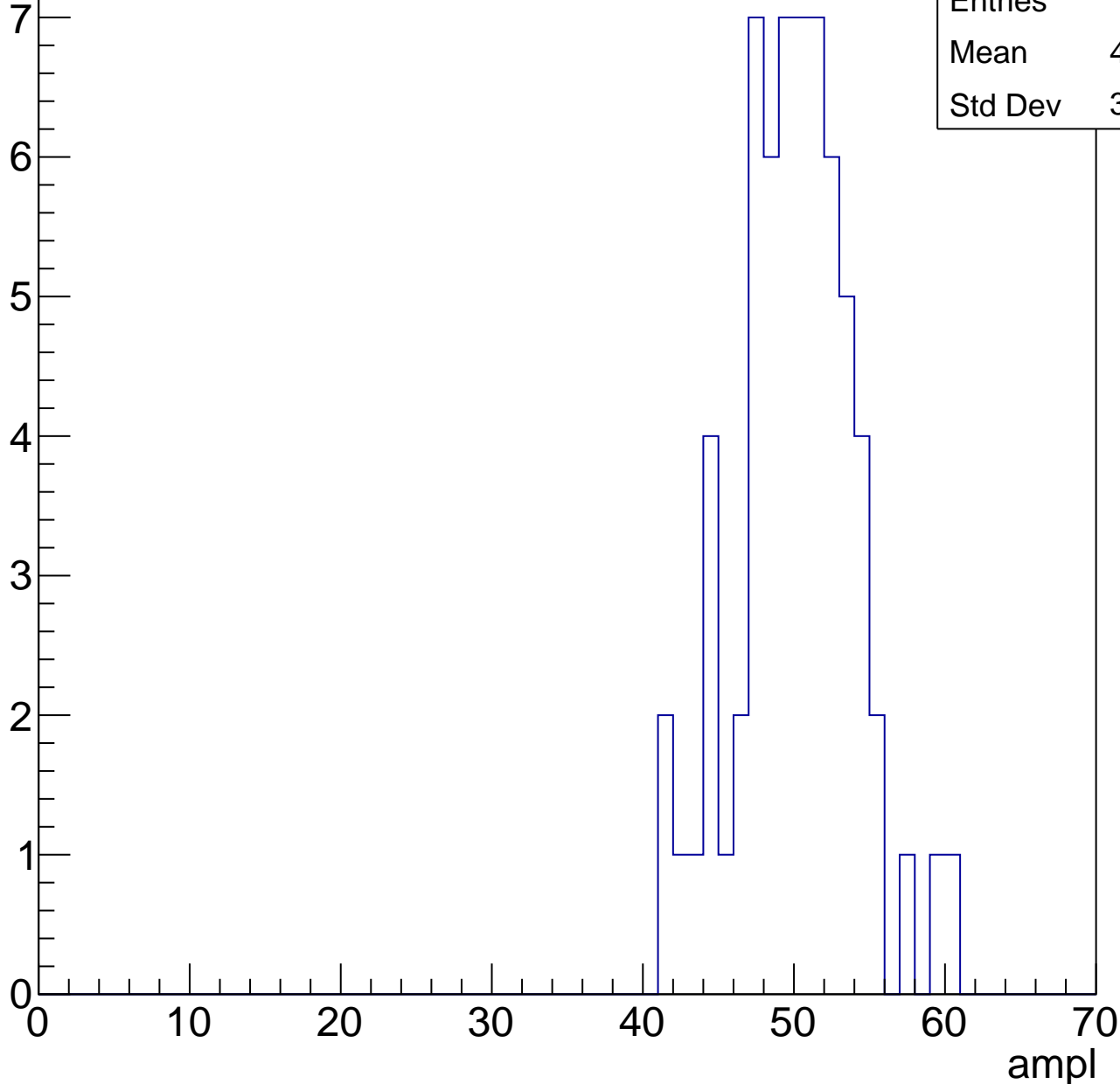


# B1L003S, U26-ch39, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	49.63
Std Dev	3.885

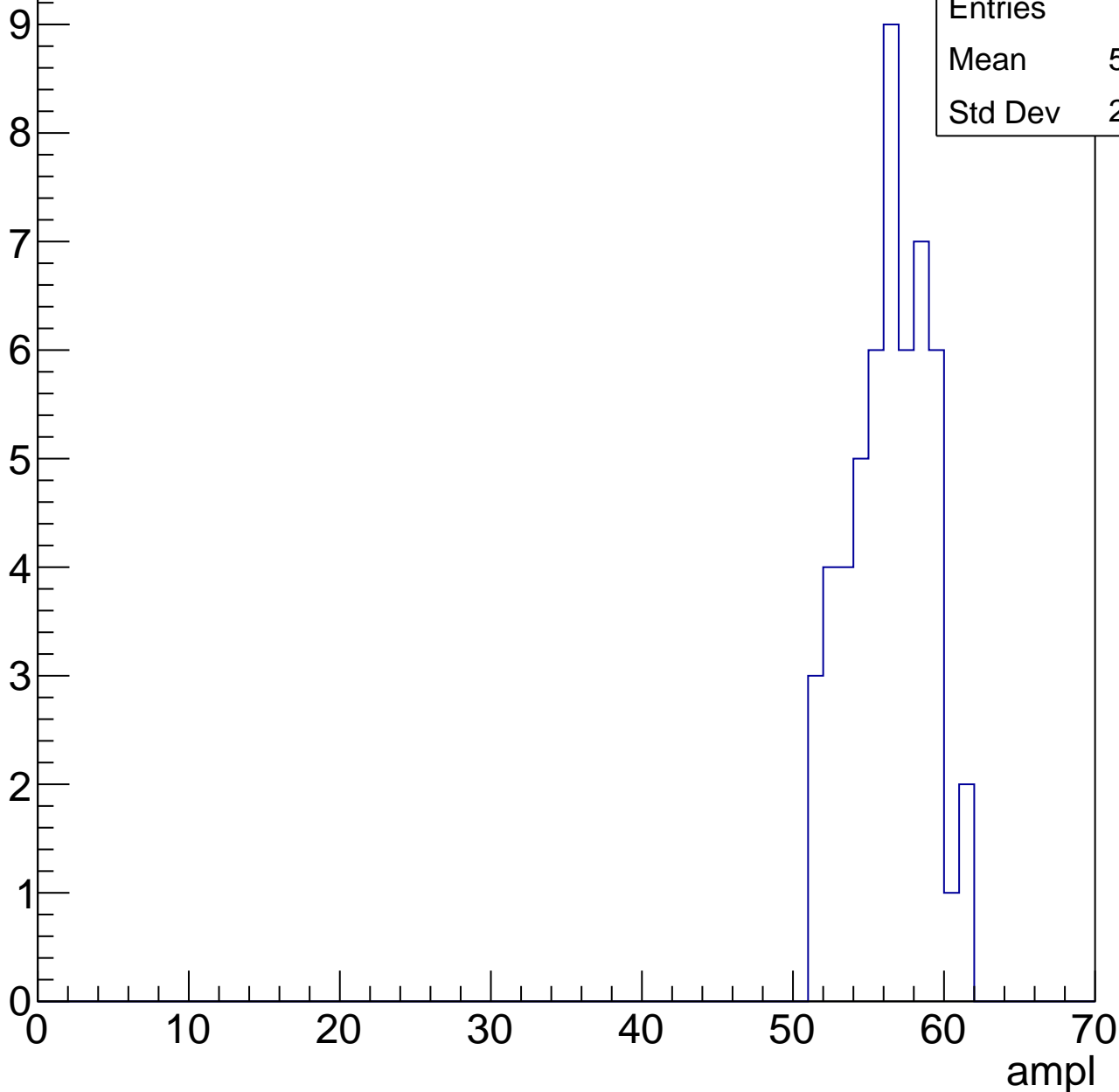


# B1L003S, U26-ch39, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	55.87
Std Dev	2.585

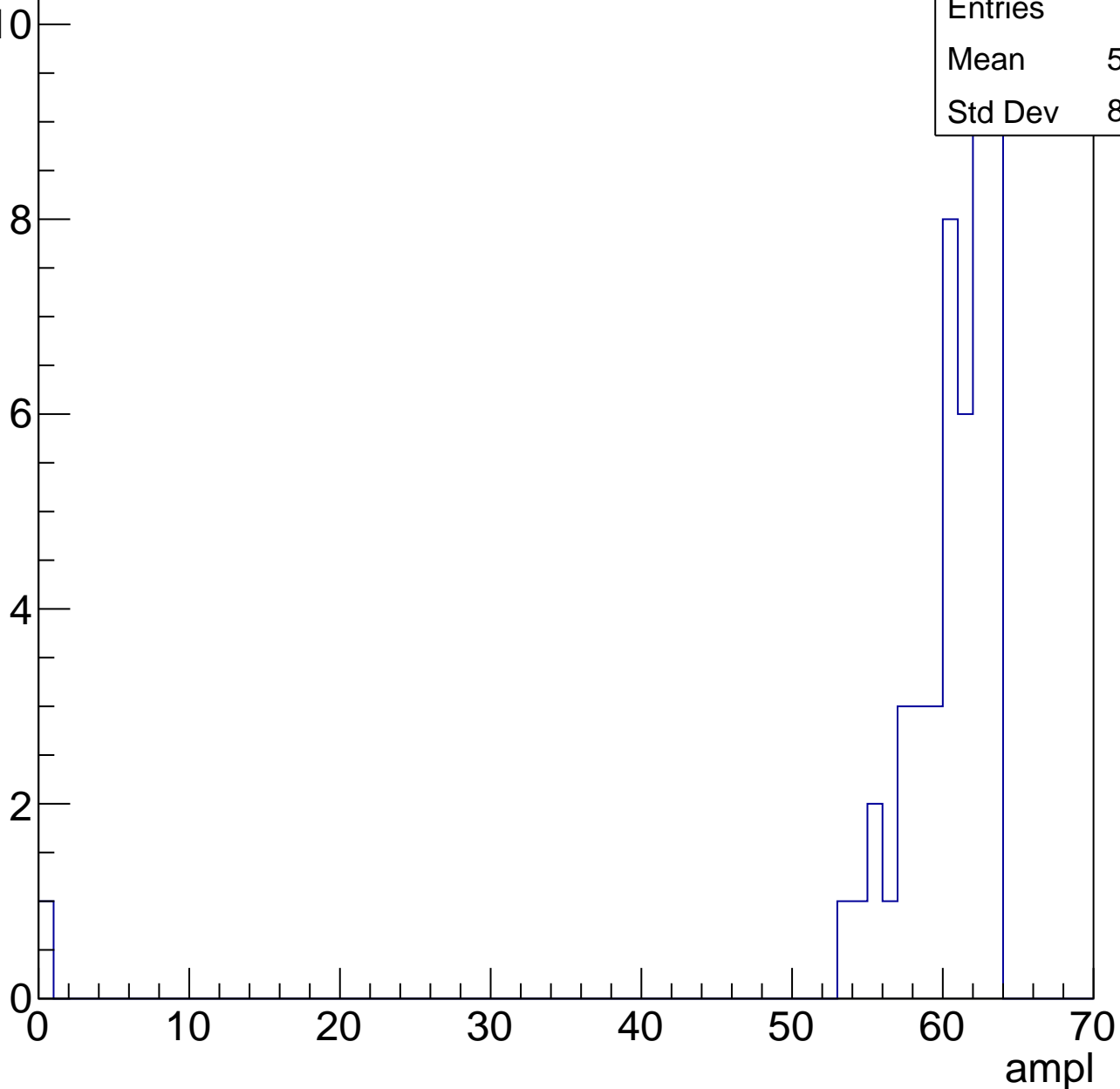


# B1L003S, U26-ch39, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	48
Mean	58.92
Std Dev	8.972



# B1L003S, U26-ch39, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch39, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

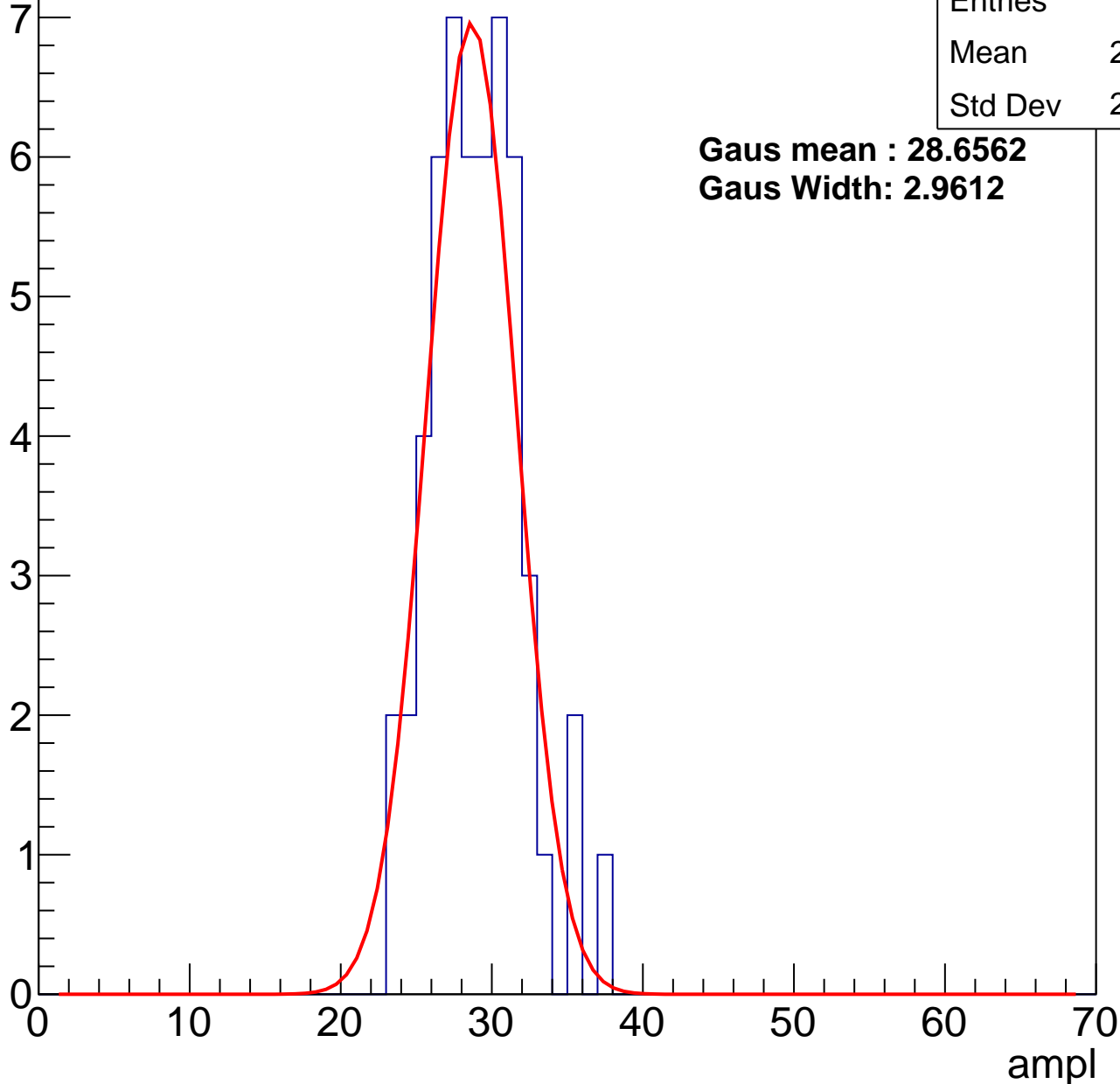


Entries	0
Mean	0
Std Dev	0

# B1L003S, U26-ch40, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U26-ch40, adc1

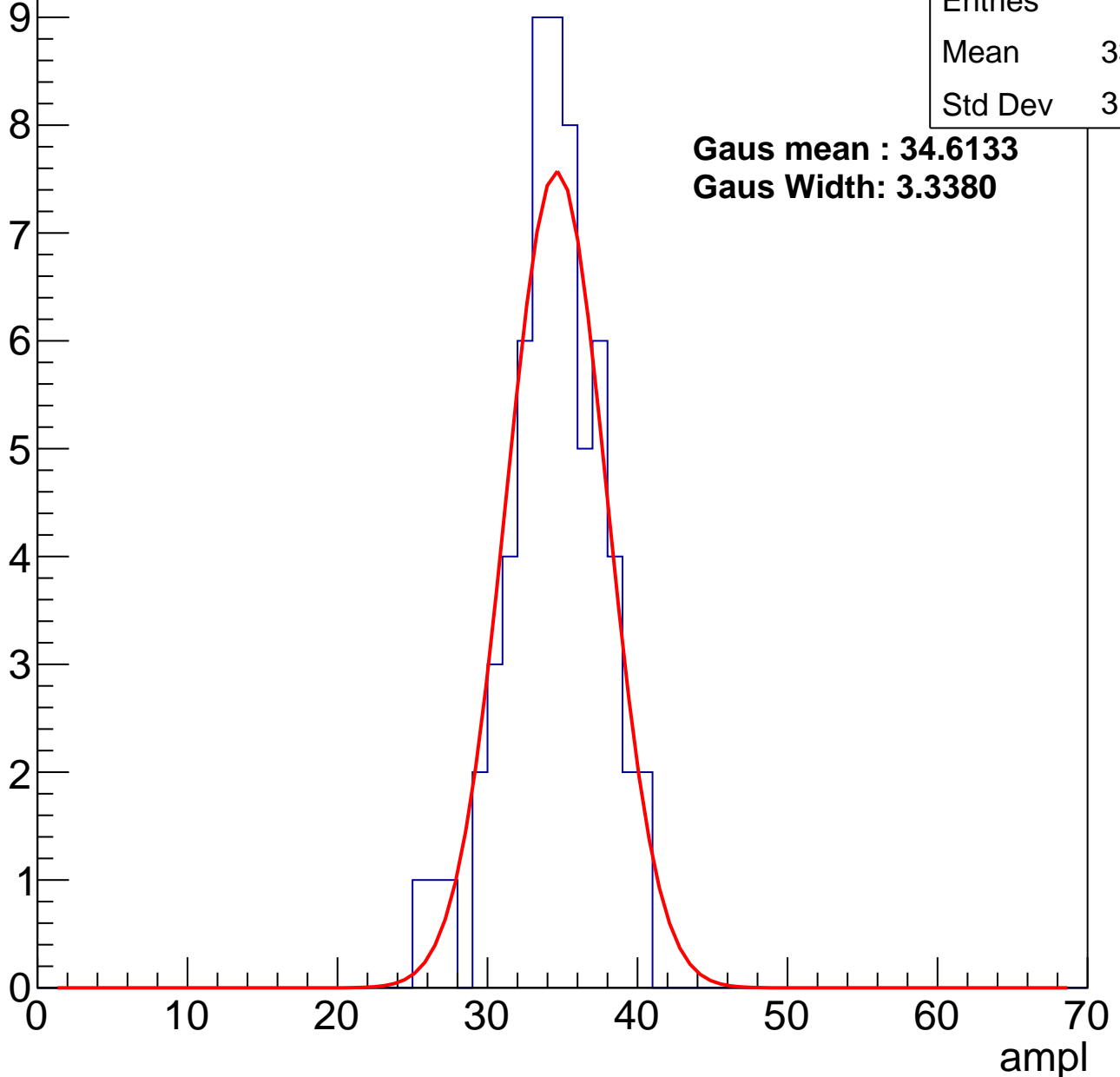
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	33.92
Std Dev	3.159

**Gaus mean : 34.6133**

**Gaus Width: 3.3380**



# B1L003S, U26-ch40, adc2

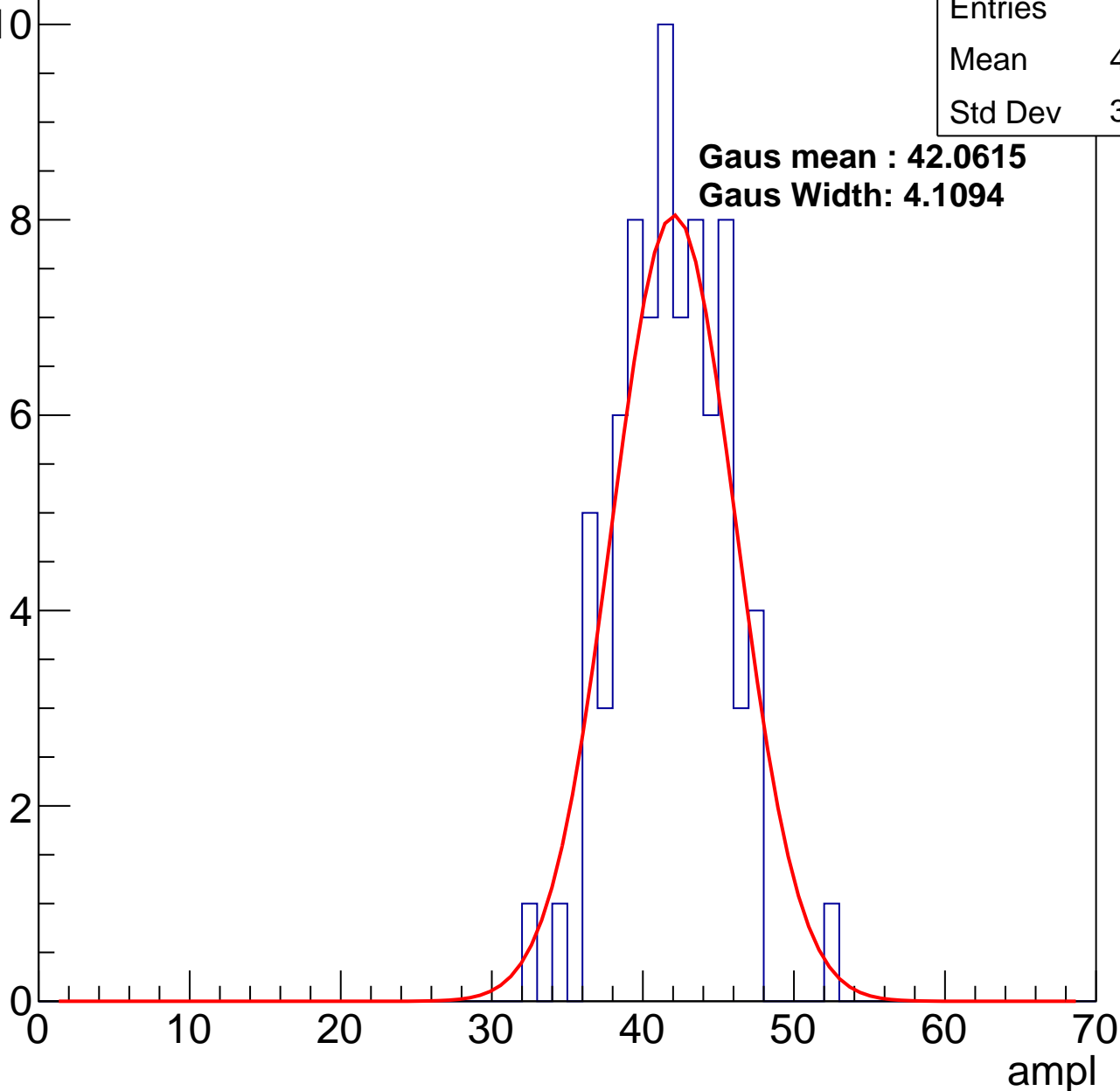
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	78
Mean	41.37
Std Dev	3.483

**Gaus mean : 42.0615**

**Gaus Width: 4.1094**

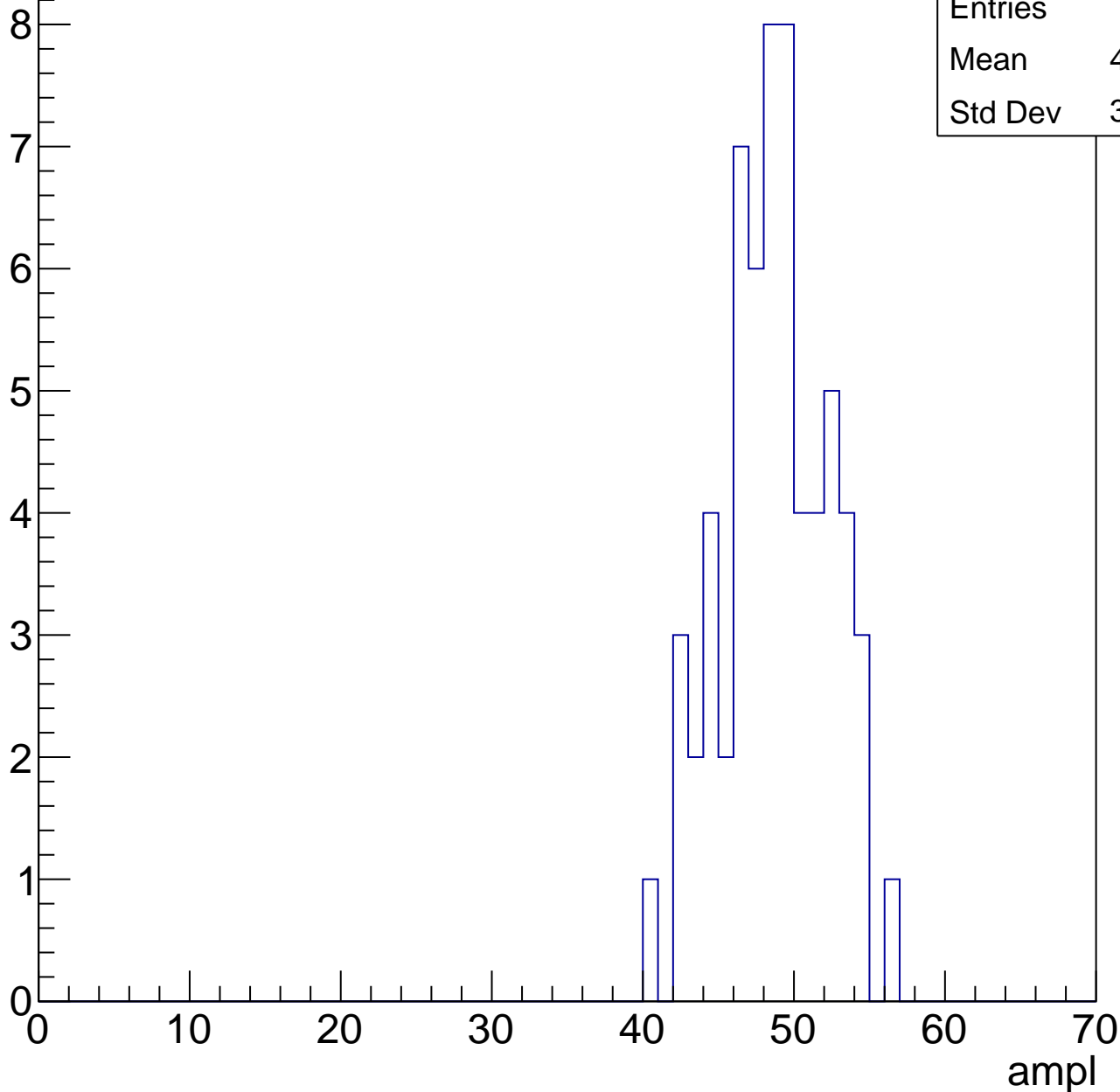


# B1L003S, U26-ch40, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	48.26
Std Dev	3.468

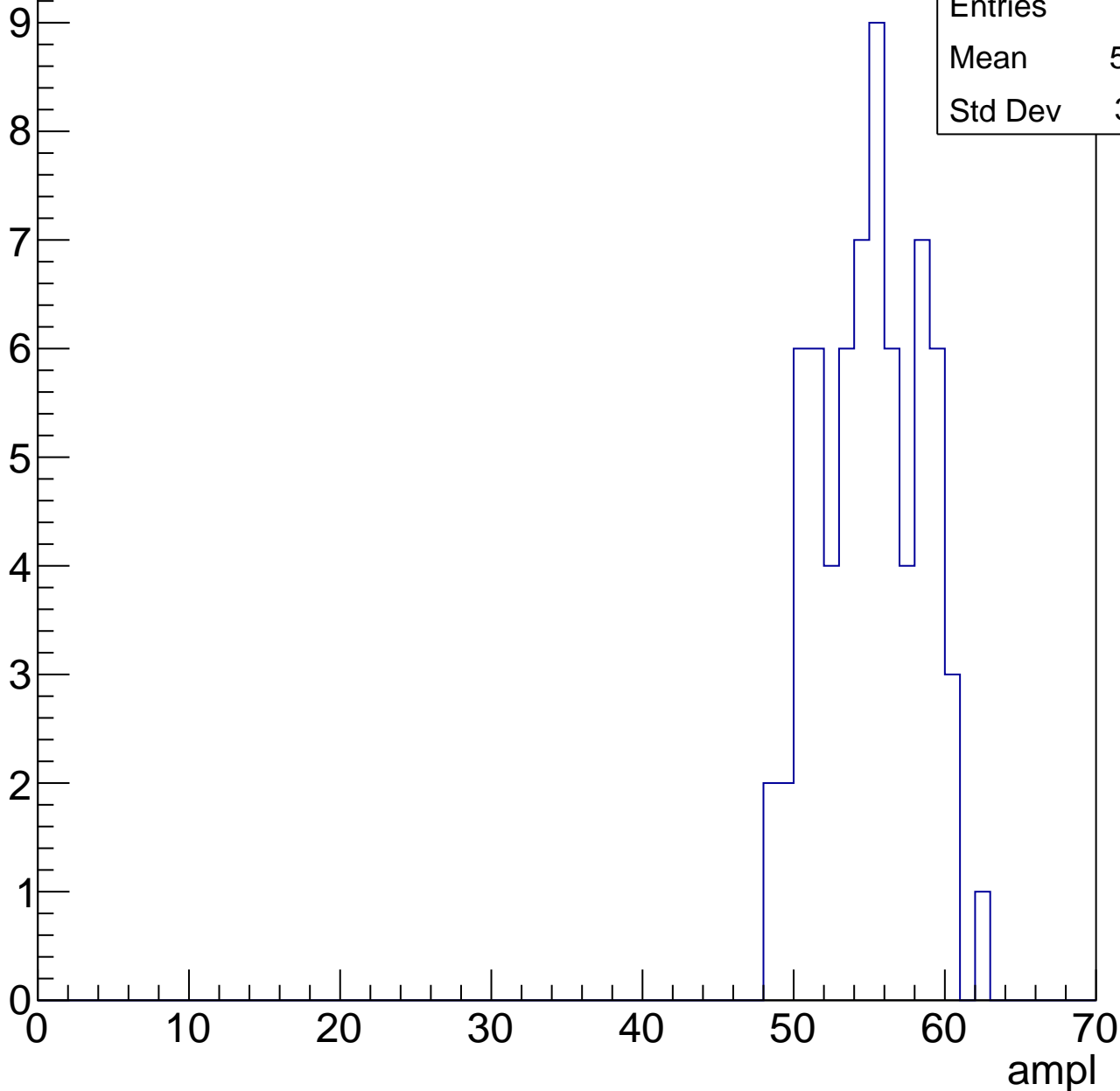


# B1L003S, U26-ch40, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	54.57
Std Dev	3.351

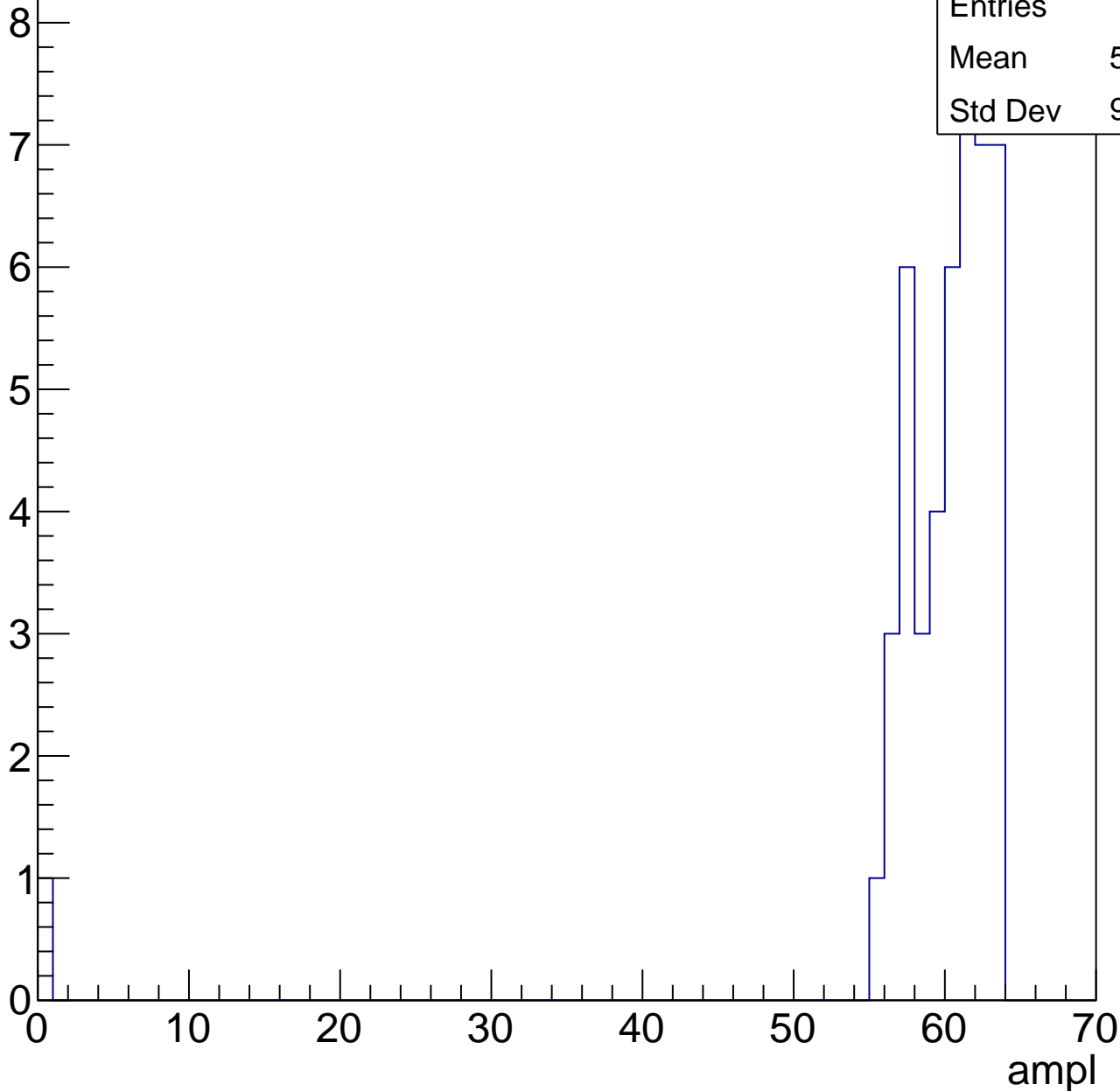


# B1L003S, U26-ch40, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	46
Mean	58.65
Std Dev	9.039



# B1L003S, U26-ch40, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch40, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U26-ch41, adc0

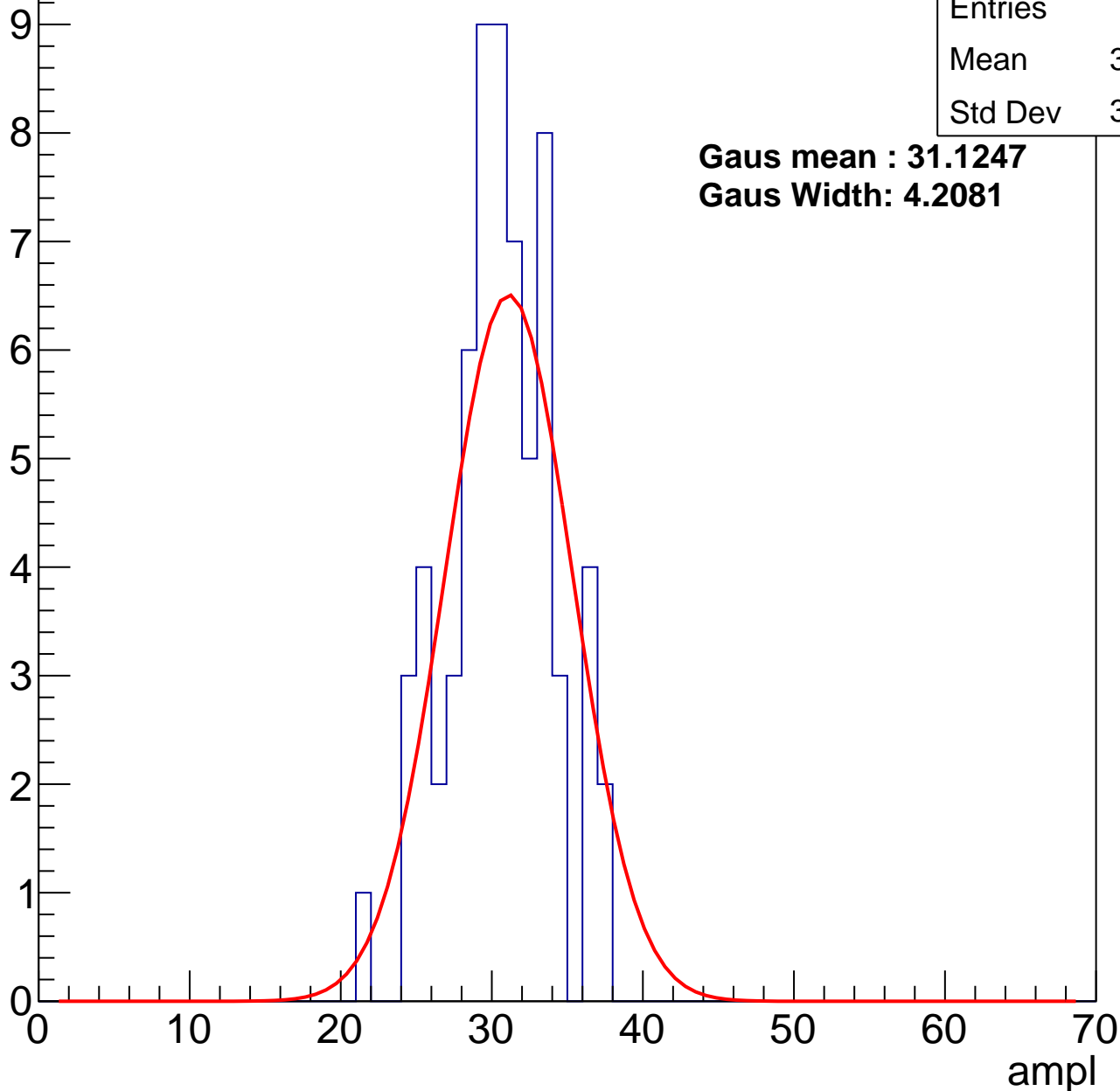
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	30.09
Std Dev	3.414

**Gaus mean : 31.1247**

**Gaus Width: 4.2081**



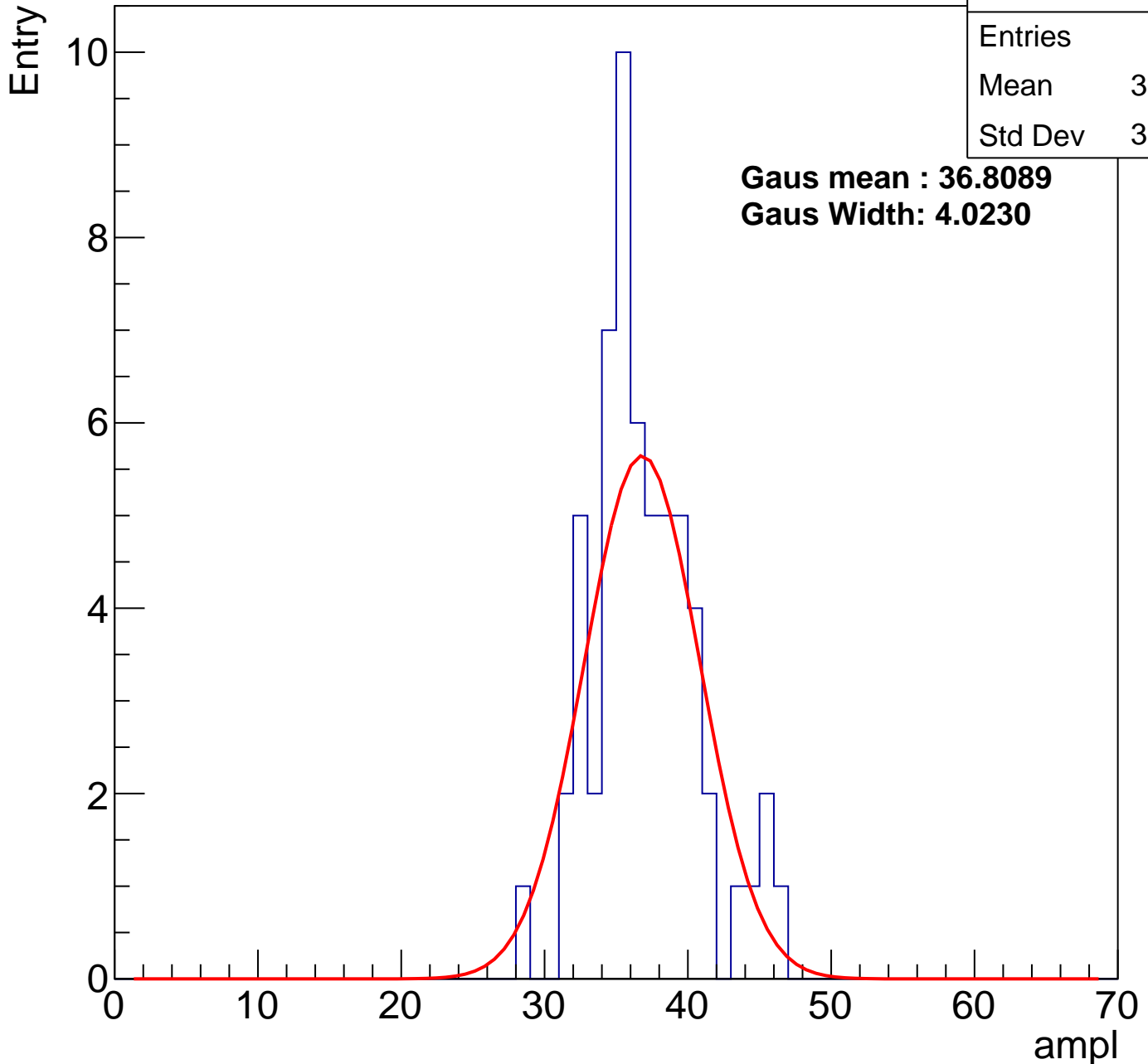
# B1L003S, U26-ch41, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	59
Mean	36.53
Std Dev	3.665

**Gaus mean : 36.8089**

**Gaus Width: 4.0230**



# B1L003S, U26-ch41, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	42.28
Std Dev	2.946

**Gaus mean : 42.3276**

**Gaus Width: 3.5601**

10

8

6

4

2

0

0

10

20

30

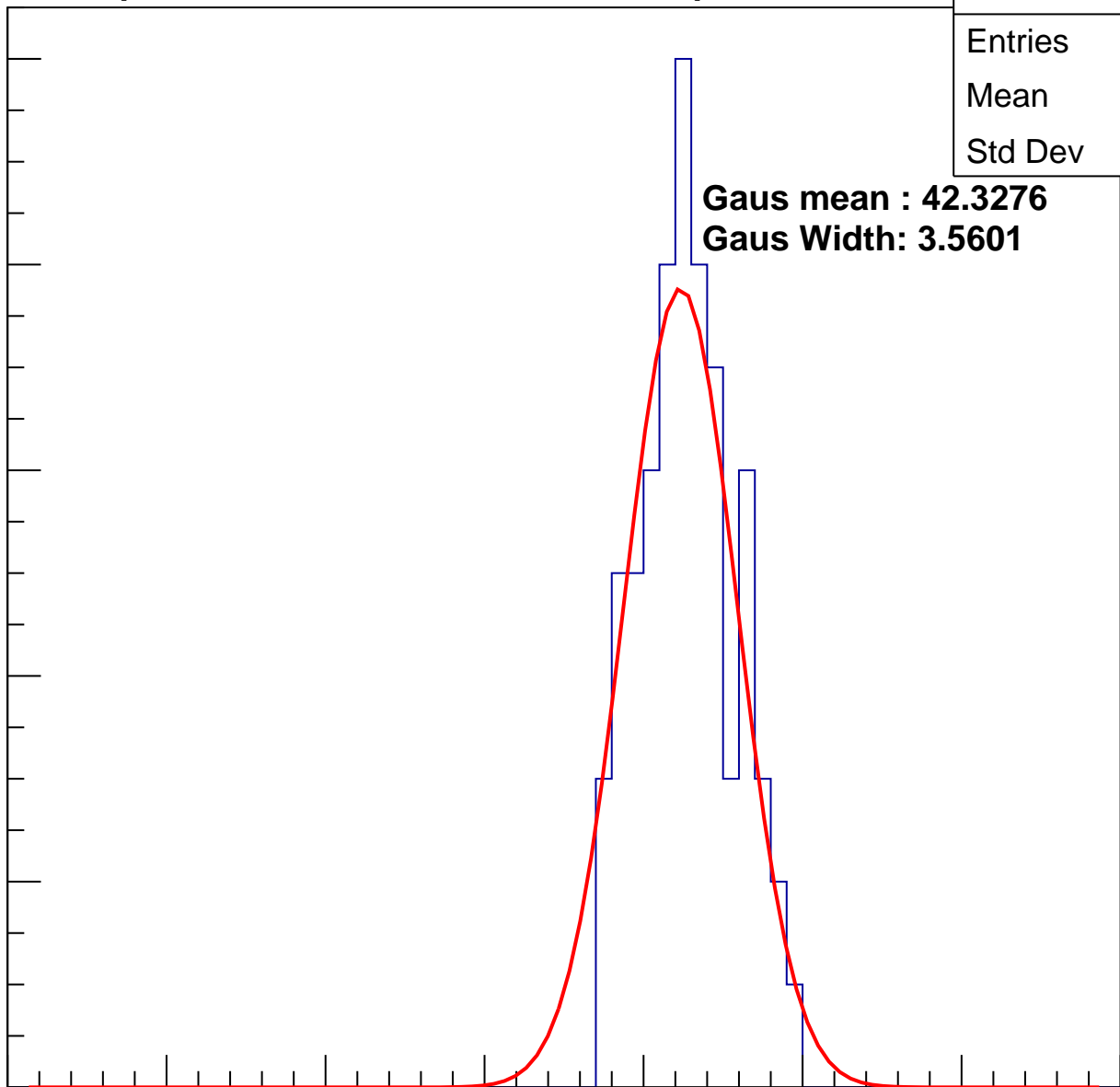
40

50

60

70

ampl

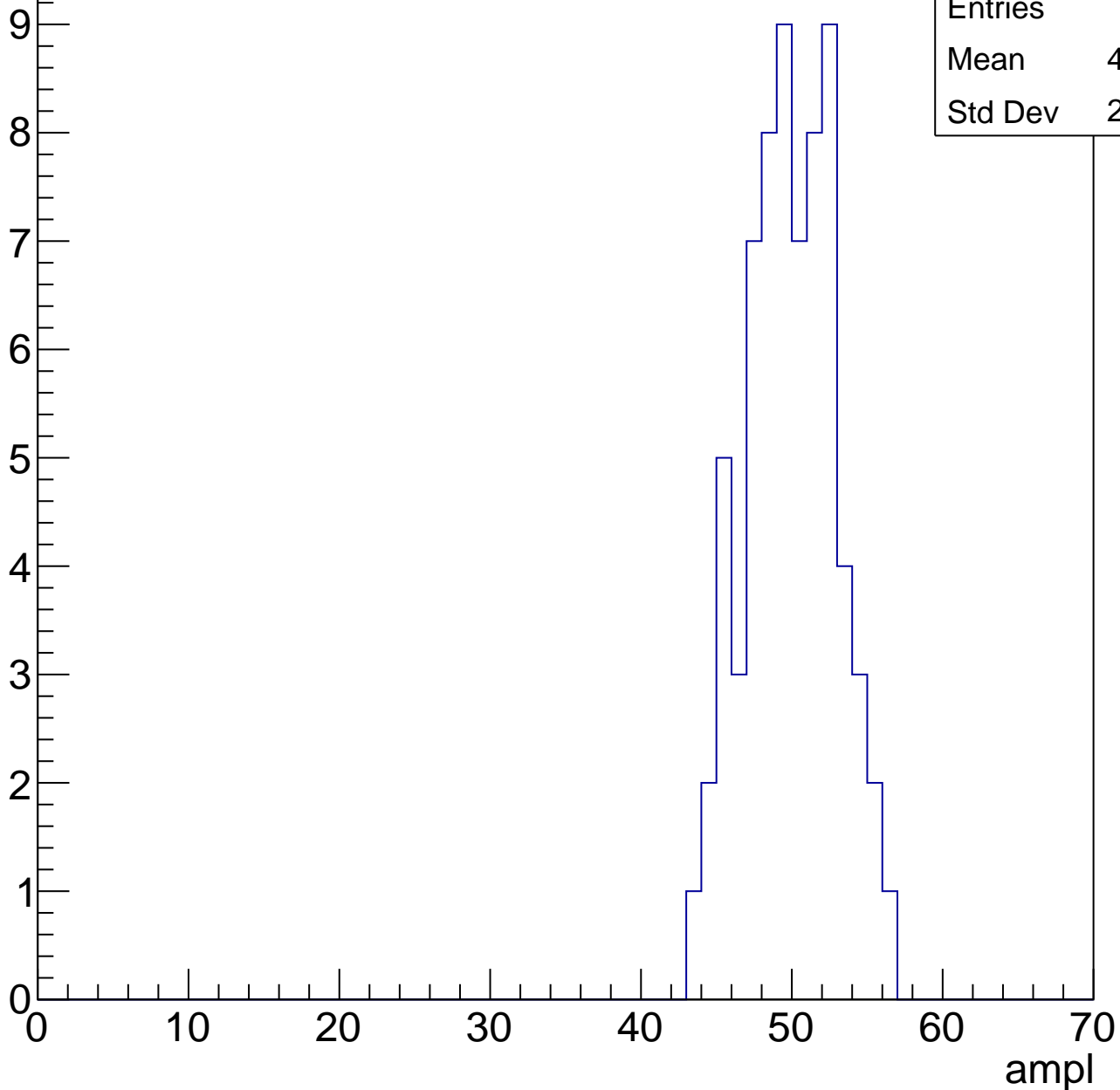


# B1L003S, U26-ch41, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	49.48
Std Dev	2.932

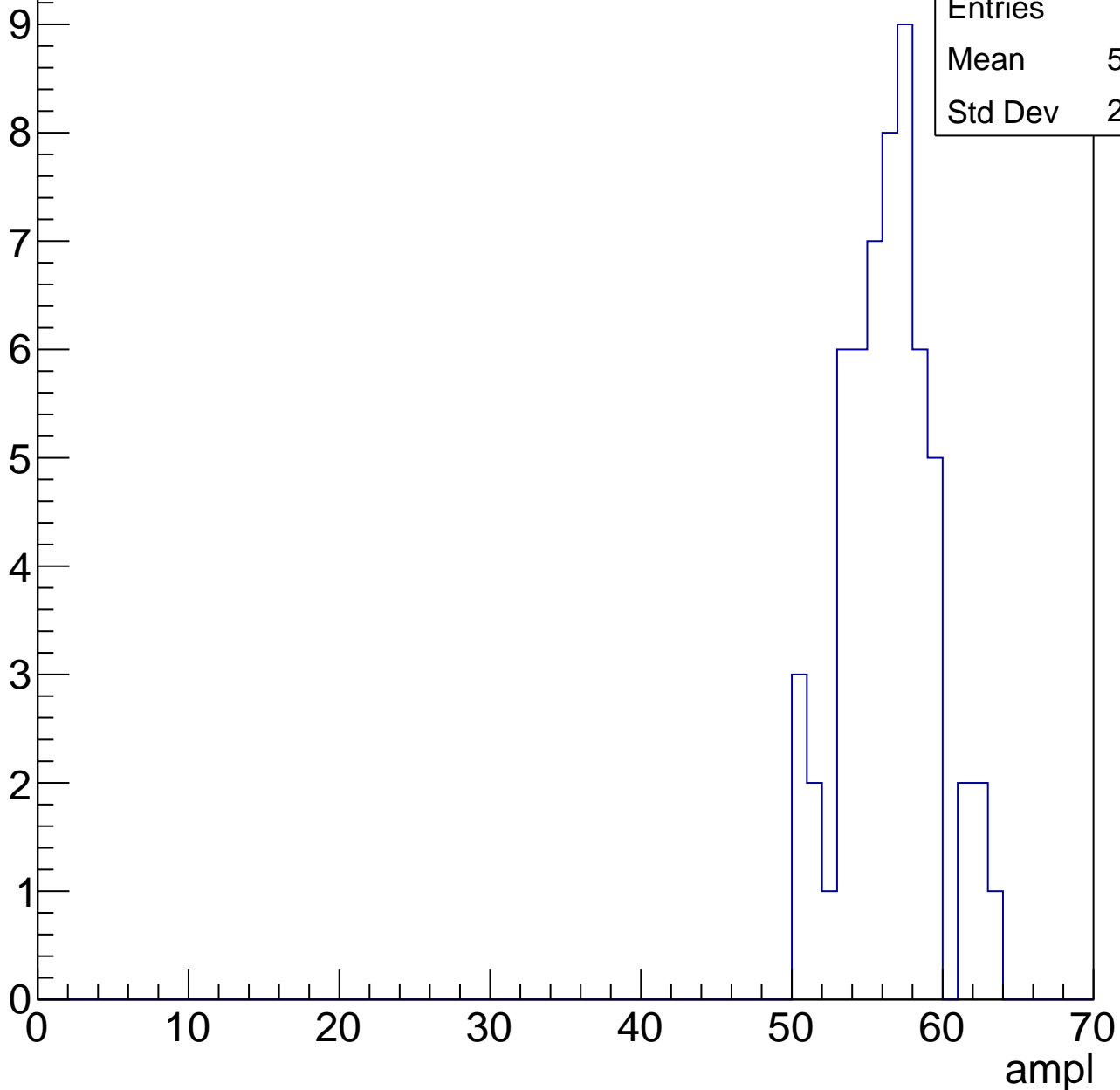


# B1L003S, U26-ch41, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	55.93
Std Dev	2.959

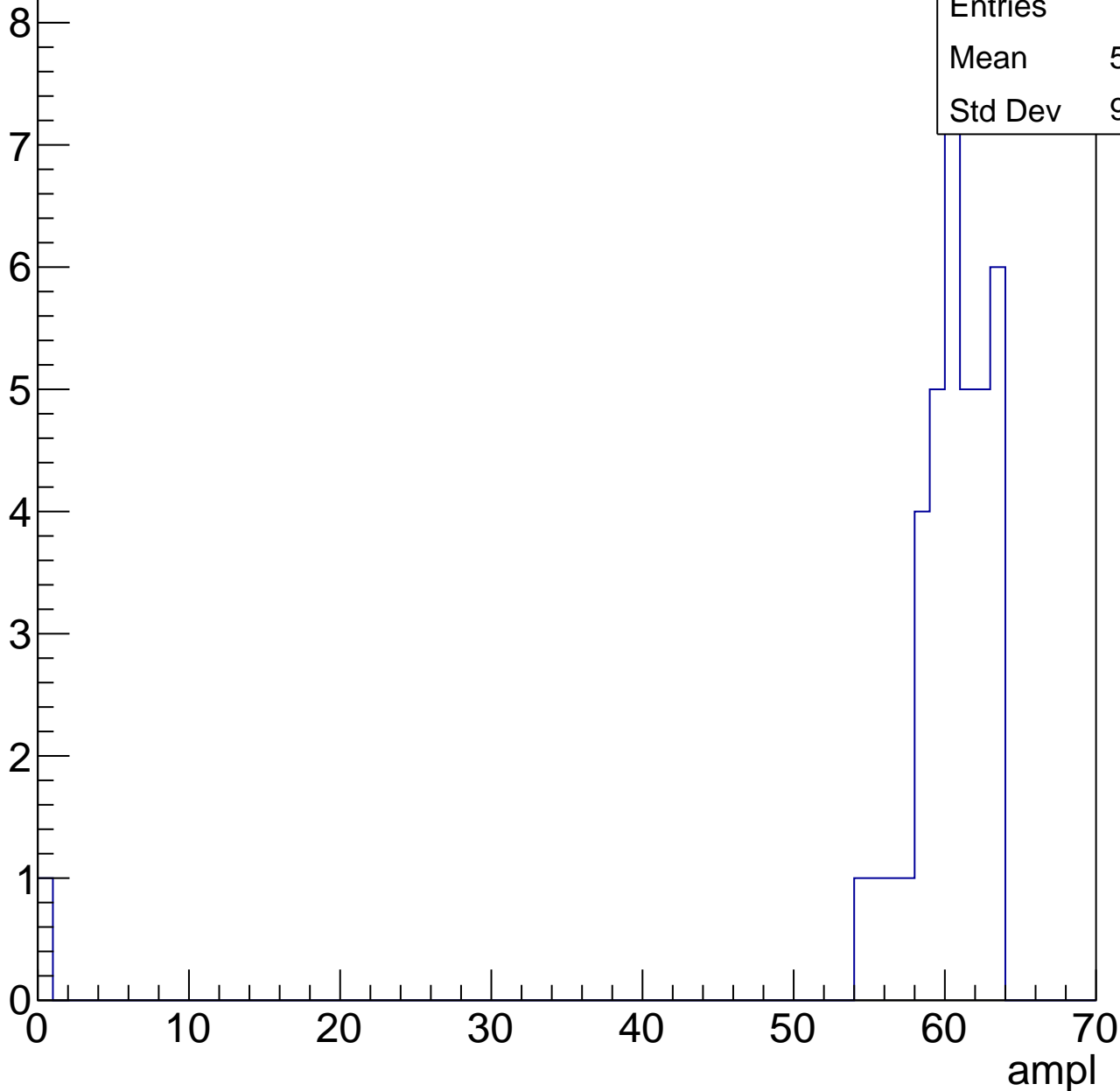


# B1L003S, U26-ch41, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	38
Mean	58.47
Std Dev	9.864



# B1L003S, U26-ch41, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries	11
Mean	61.64
Std Dev	1.068



# B1L003S, U26-ch41, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U26-ch42, adc0

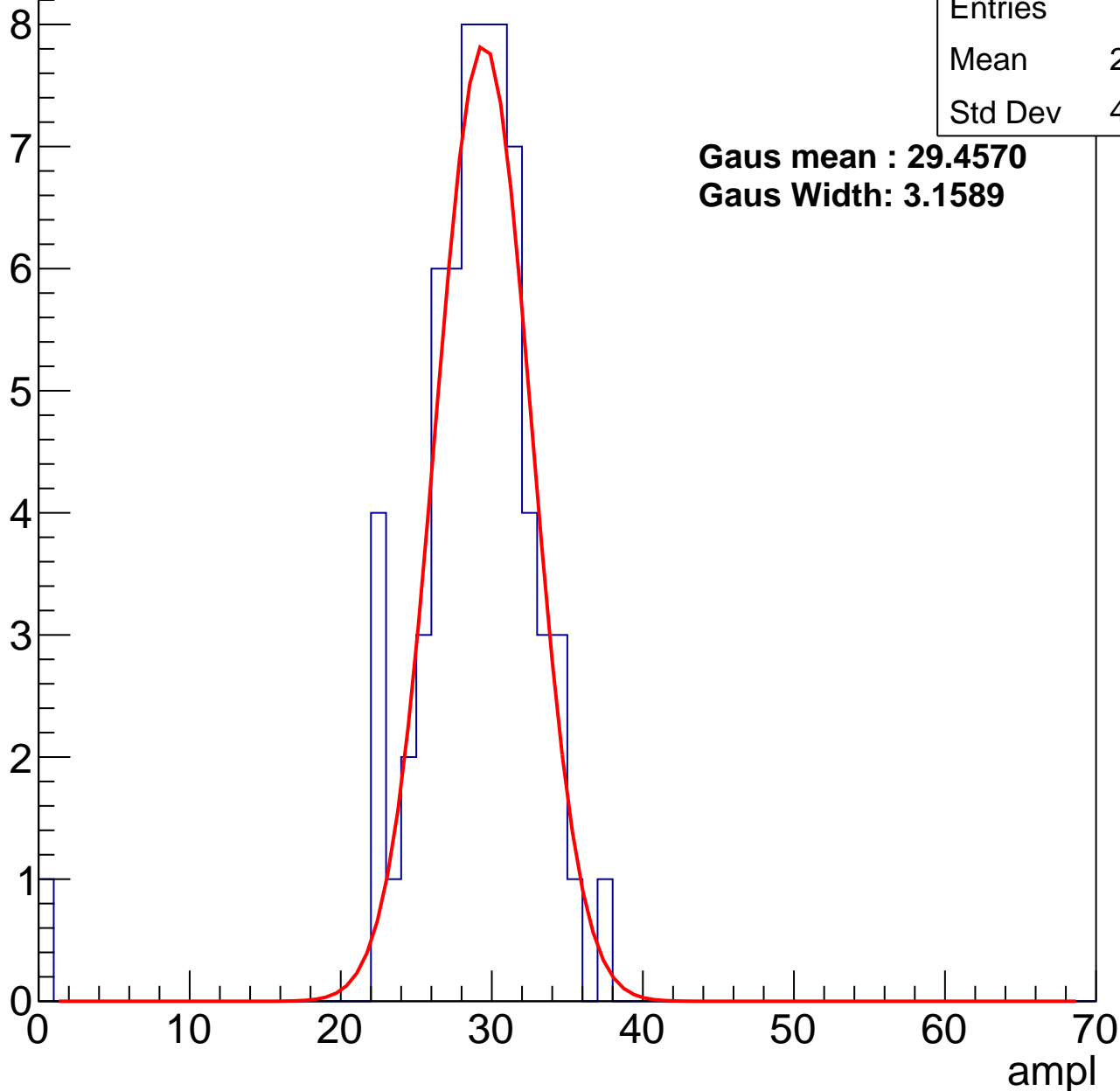
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	28.27
Std Dev	4.794

**Gaus mean : 29.4570**

**Gaus Width: 3.1589**



# B1L003S, U26-ch42, adc1

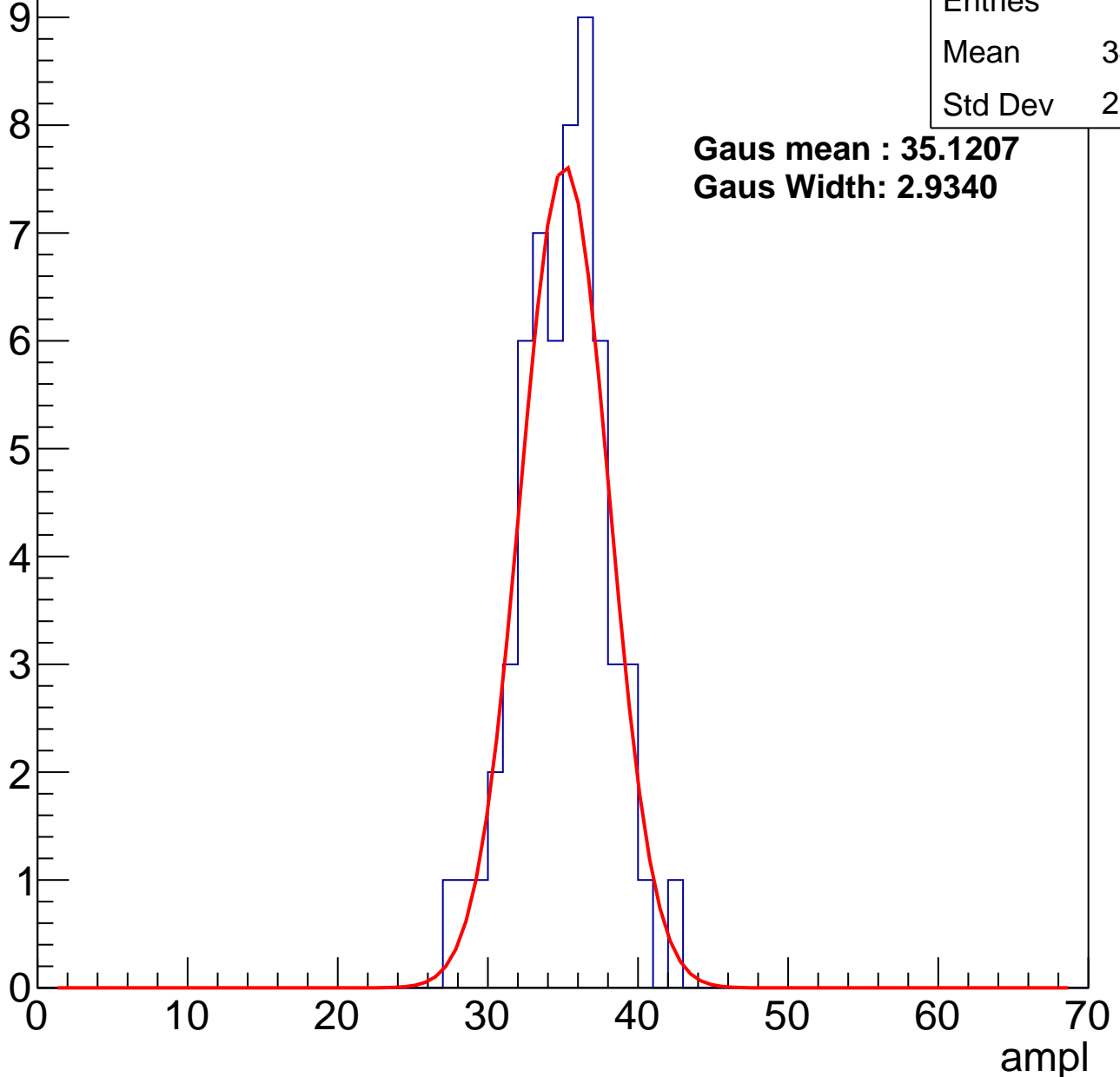
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	34.53
Std Dev	2.949

**Gaus mean : 35.1207**

**Gaus Width: 2.9340**



# B1L003S, U26-ch42, adc2

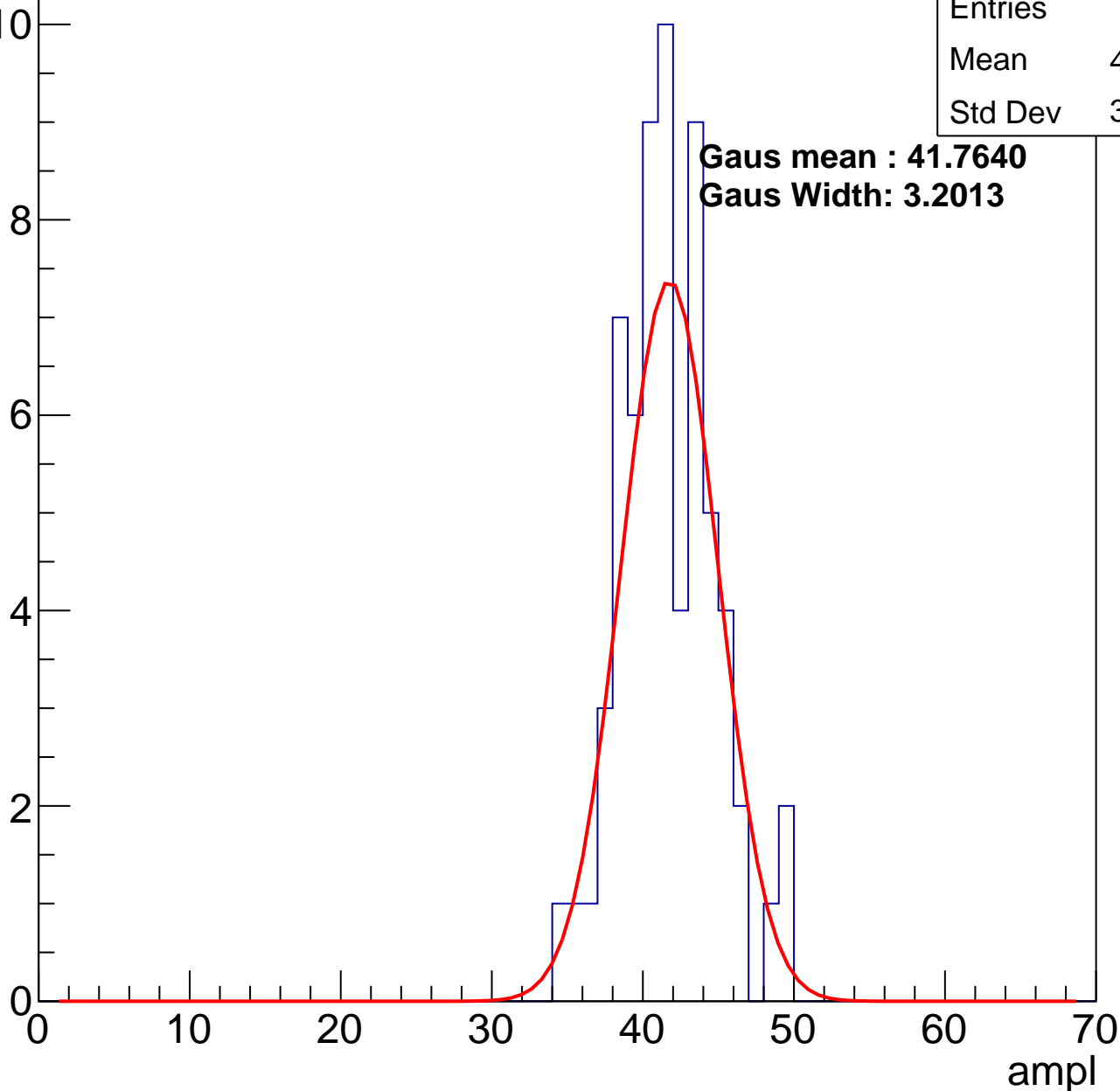
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	41.22
Std Dev	3.106

**Gaus mean : 41.7640**

**Gaus Width: 3.2013**

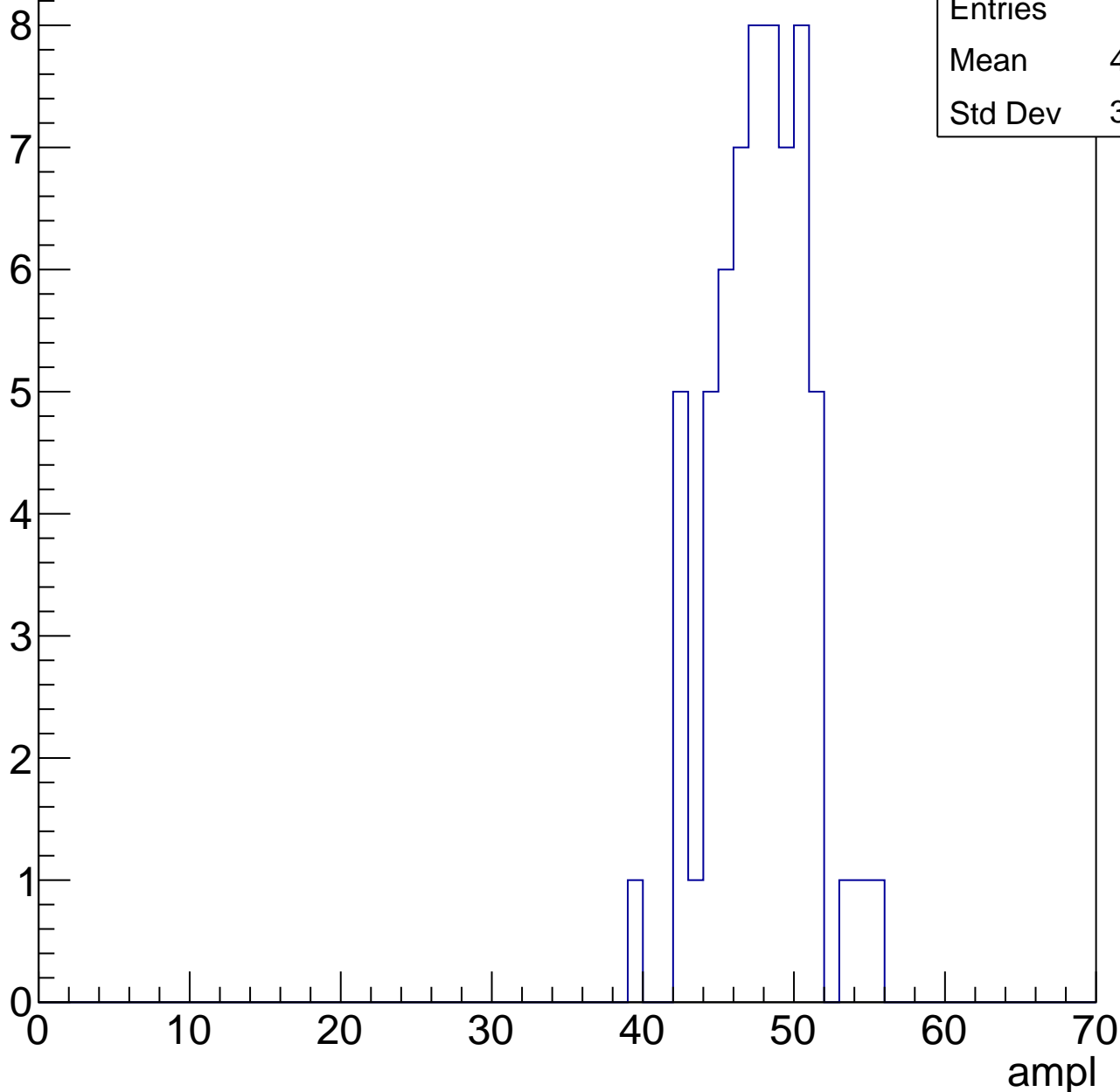


# B1L003S, U26-ch42, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	47.25
Std Dev	3.097

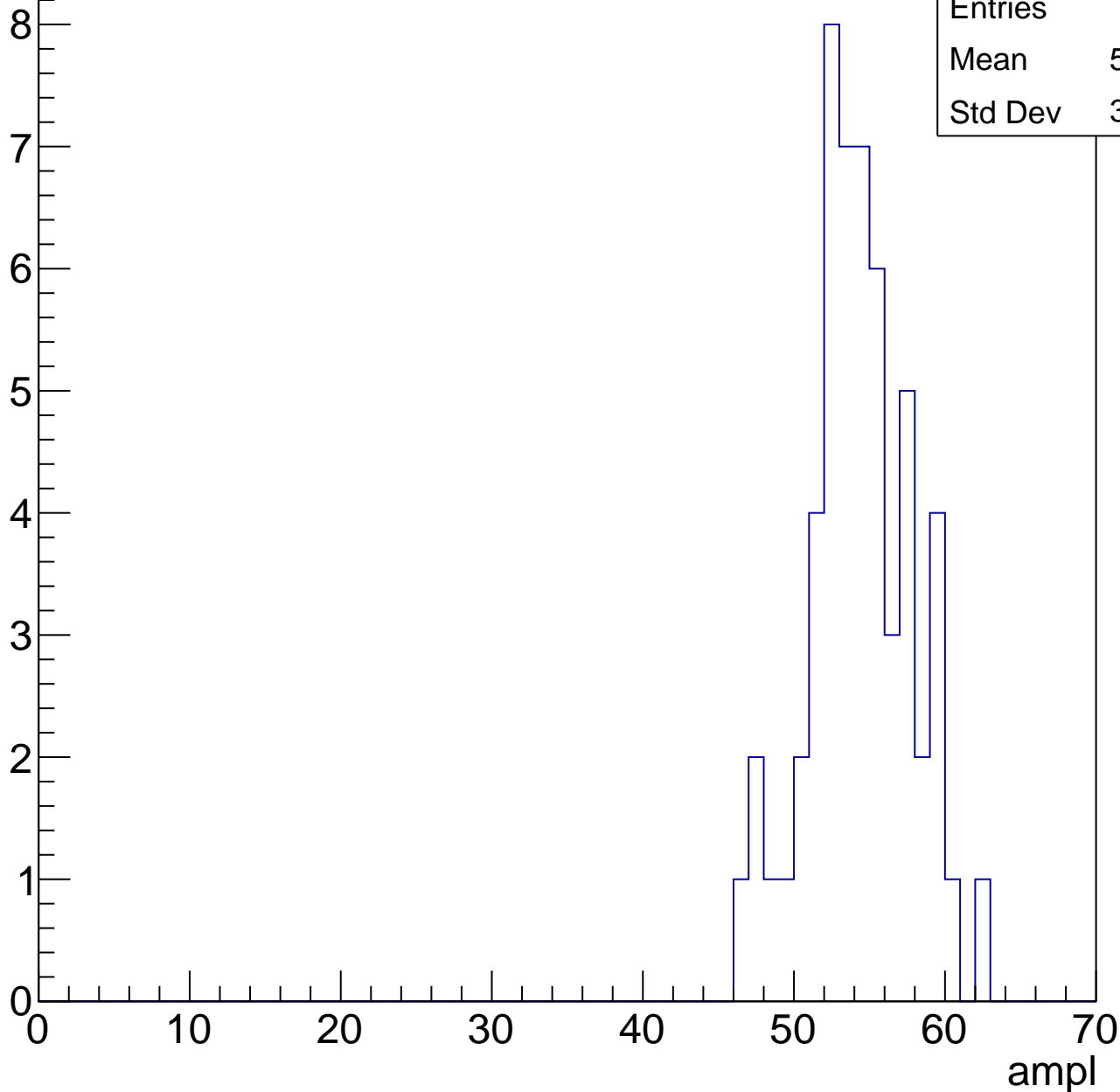


# B1L003S, U26-ch42, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	53.87
Std Dev	3.369

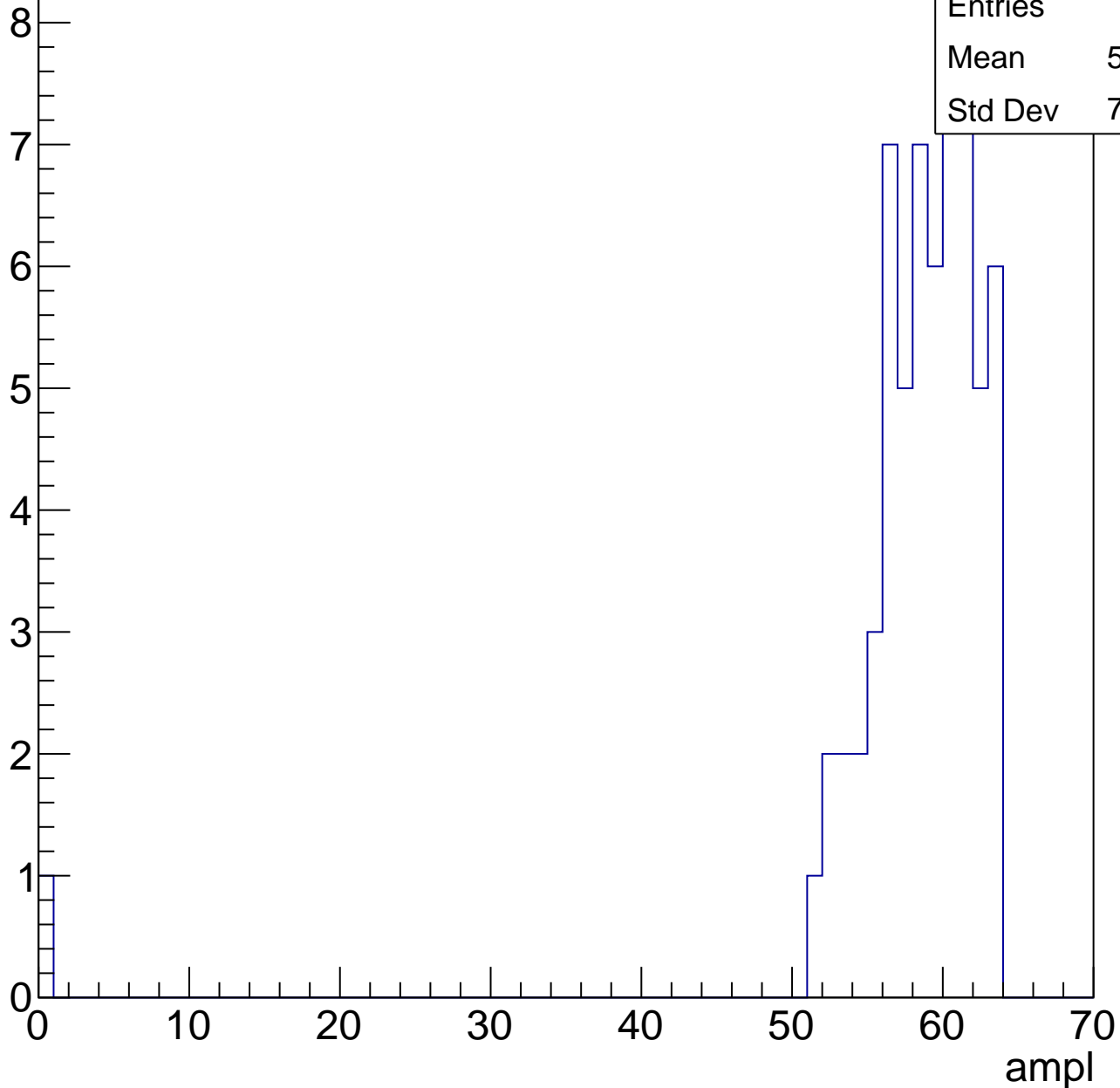


# B1L003S, U26-ch42, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

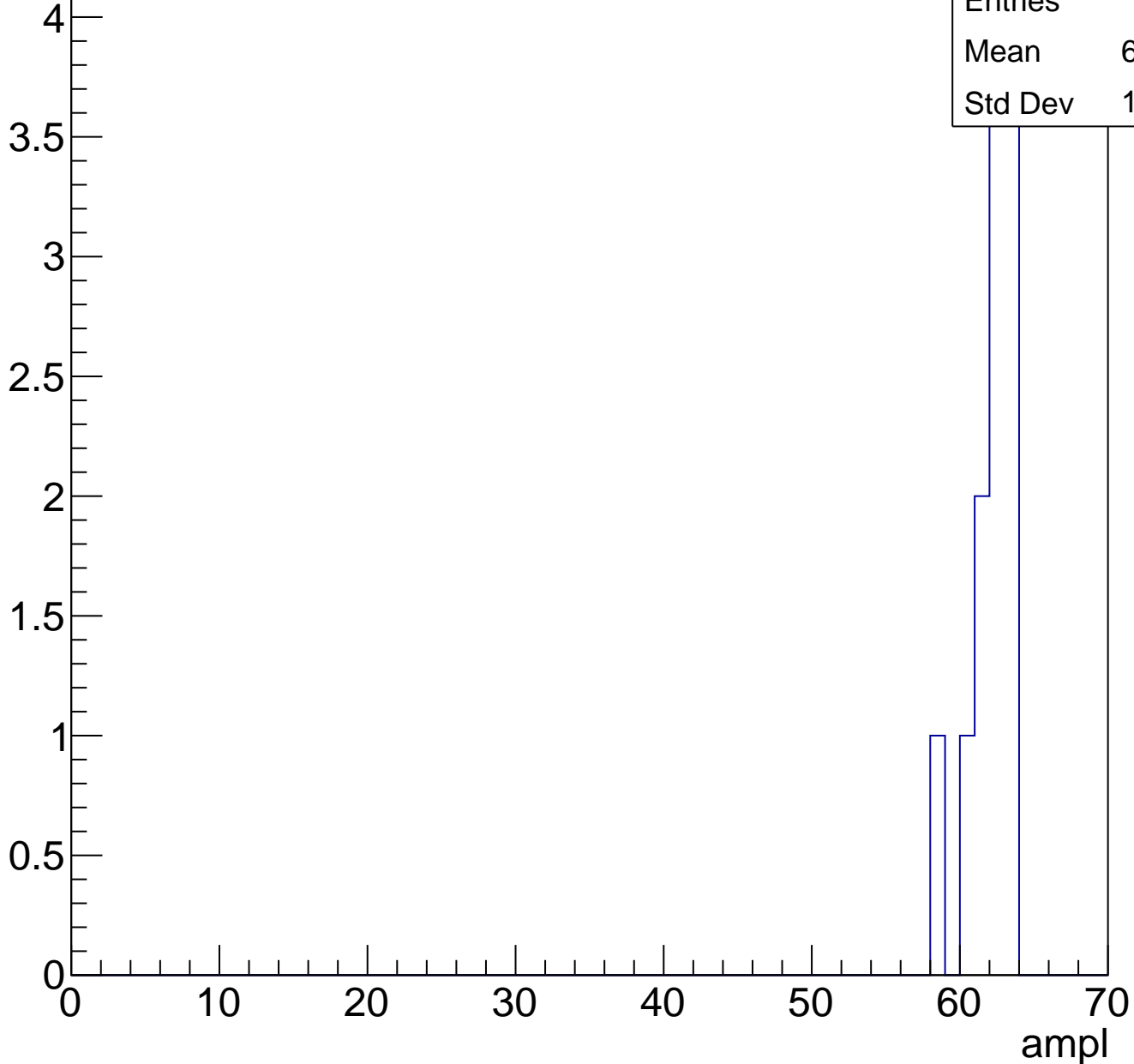
Entries	63
Mean	57.57
Std Dev	7.924



# B1L003S, U26-ch42, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch42, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U26-ch43, adc0

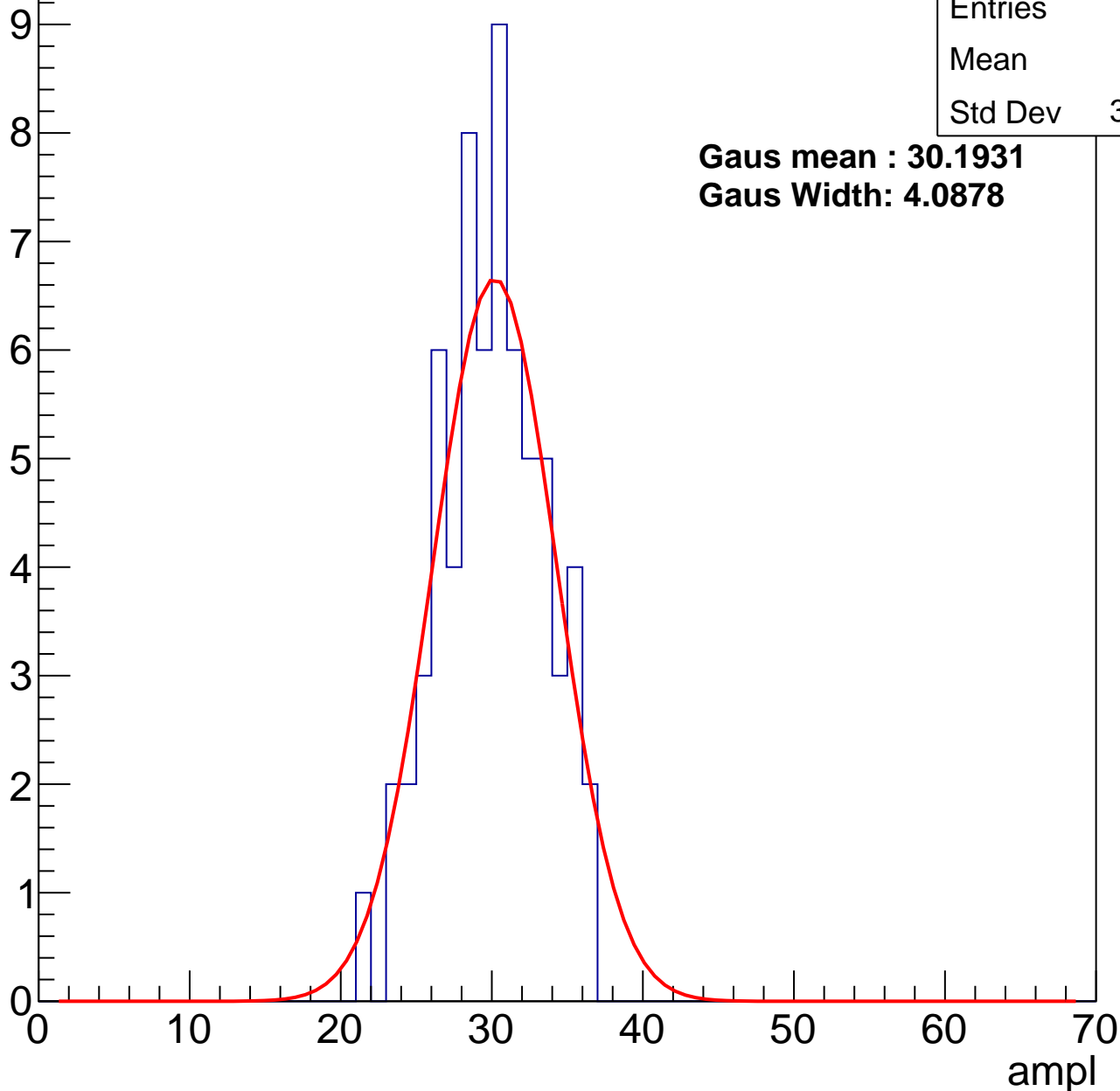
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	29.5
Std Dev	3.417

**Gaus mean : 30.1931**

**Gaus Width: 4.0878**



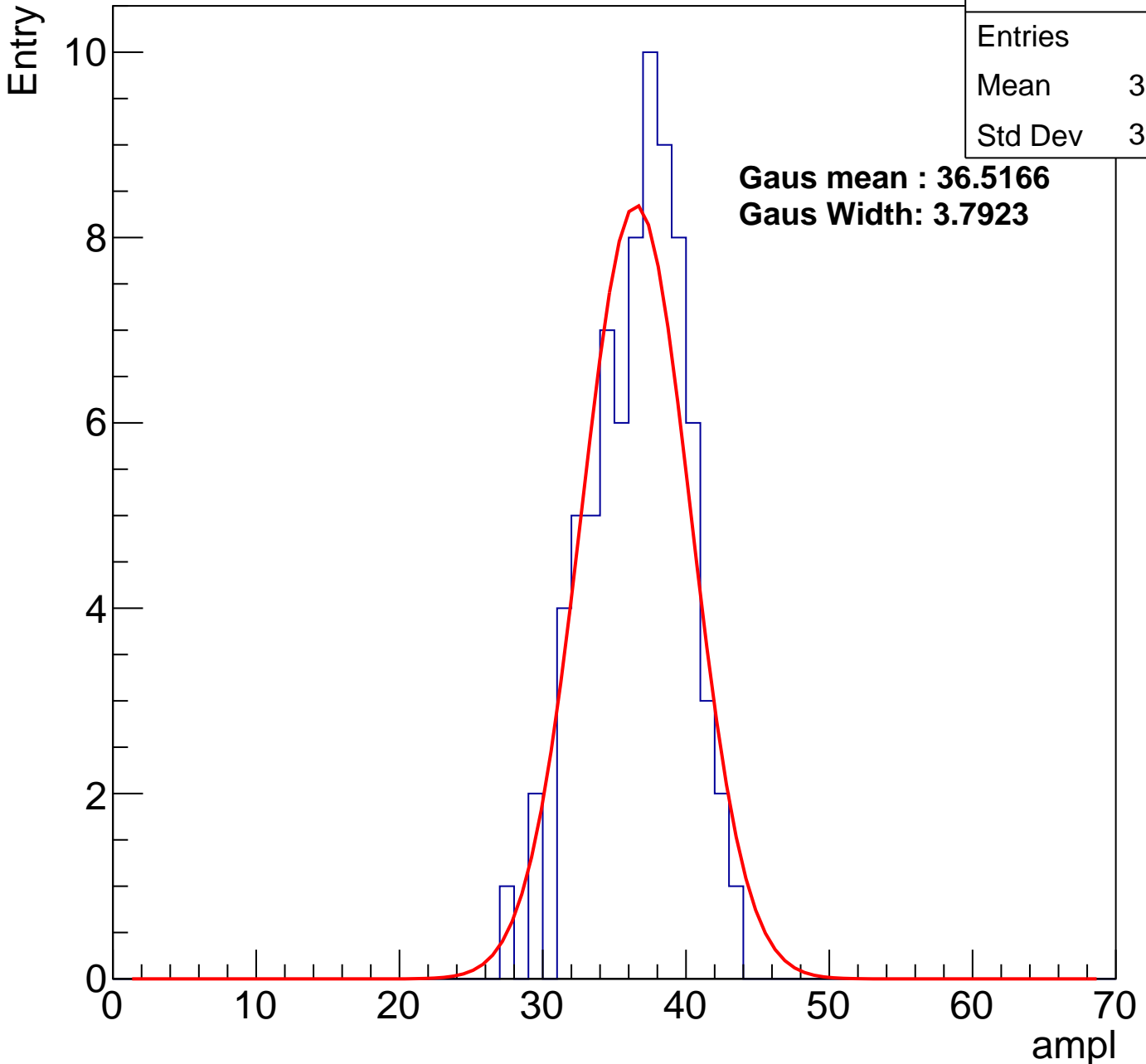
# B1L003S, U26-ch43, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	77
Mean	36.16
Std Dev	3.315

**Gaus mean : 36.5166**

**Gaus Width: 3.7923**

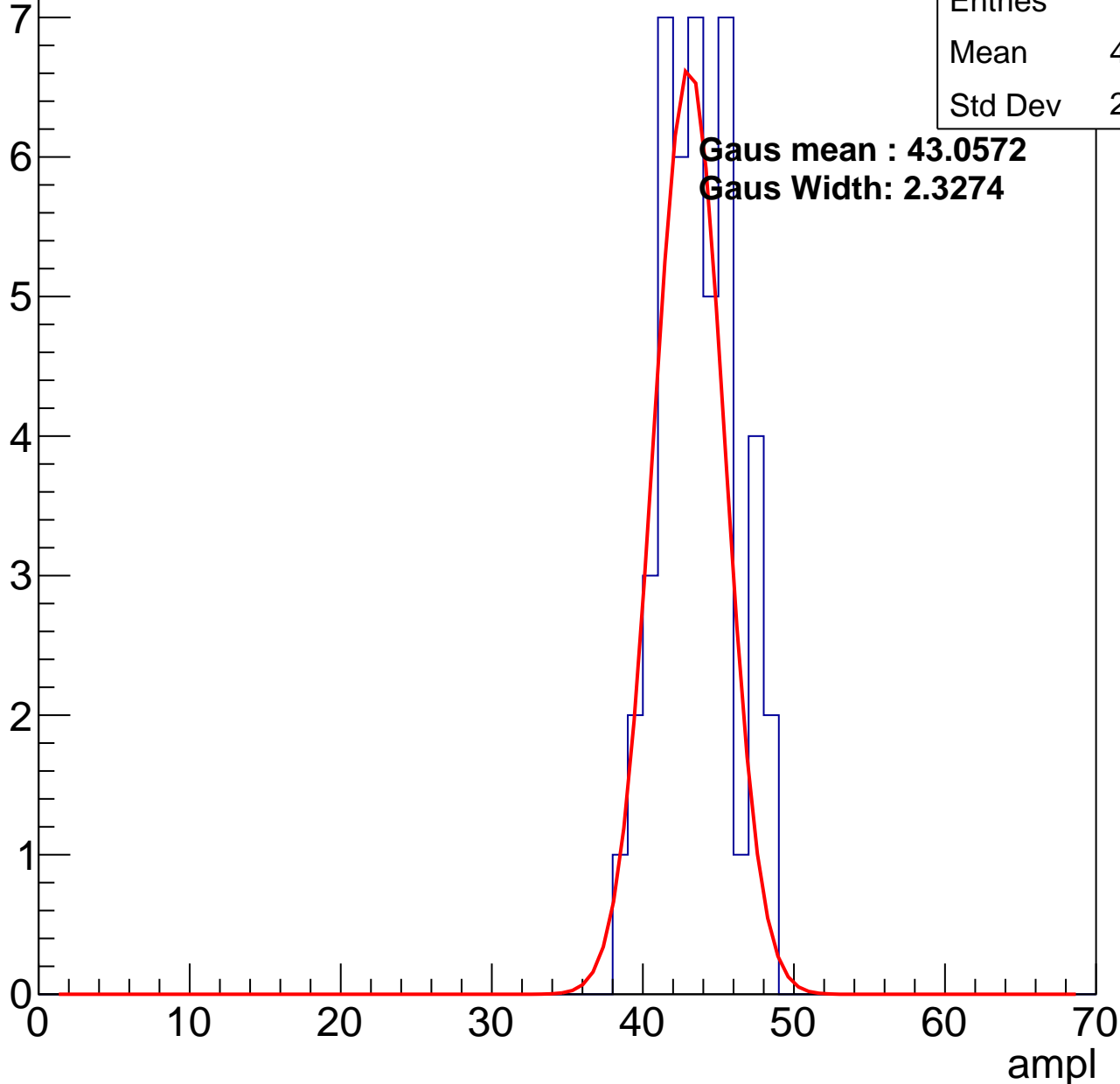


# B1L003S, U26-ch43, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	45
Mean	43.13
Std Dev	2.464

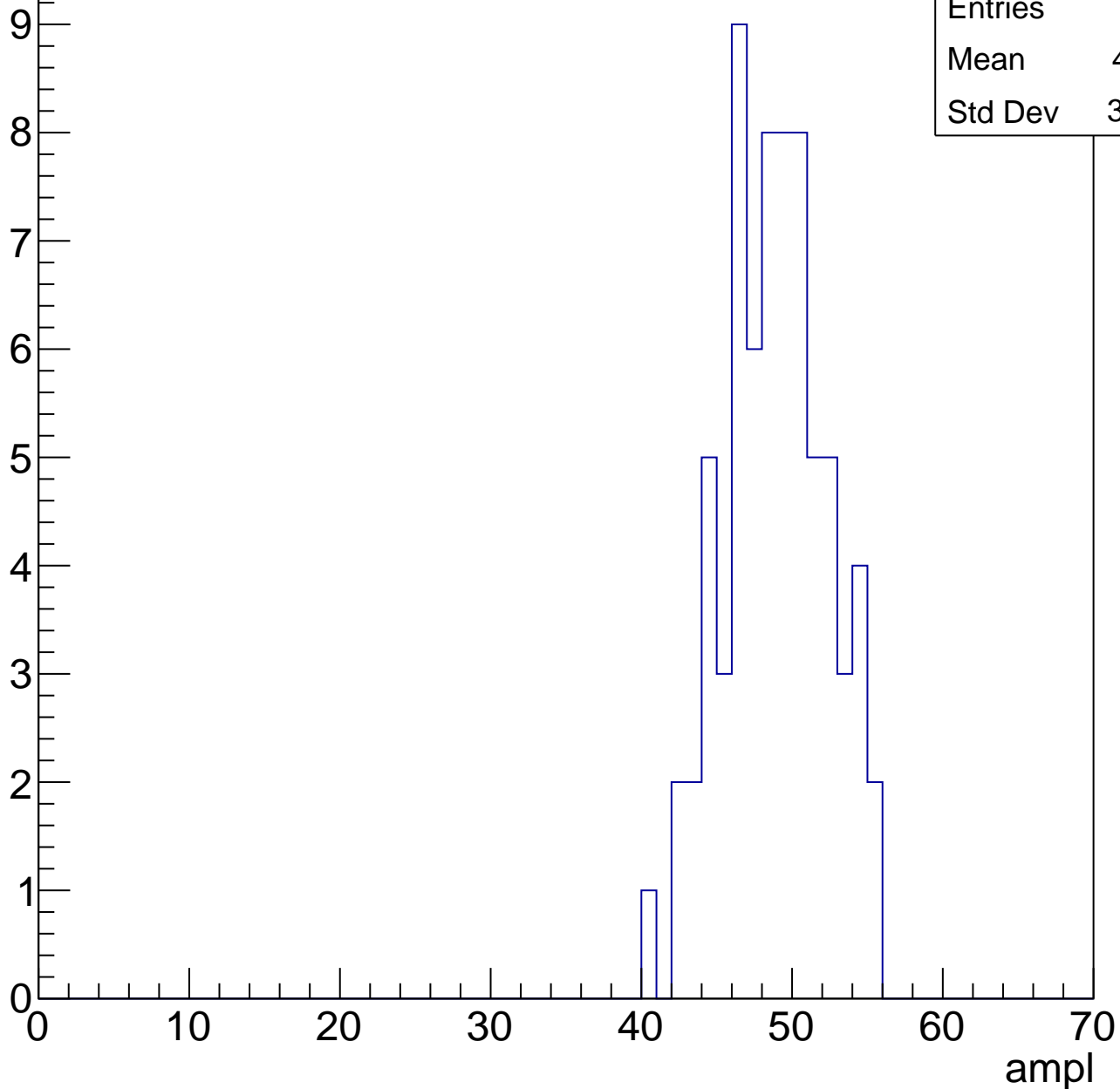


# B1L003S, U26-ch43, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	71
Mean	48.41
Std Dev	3.368

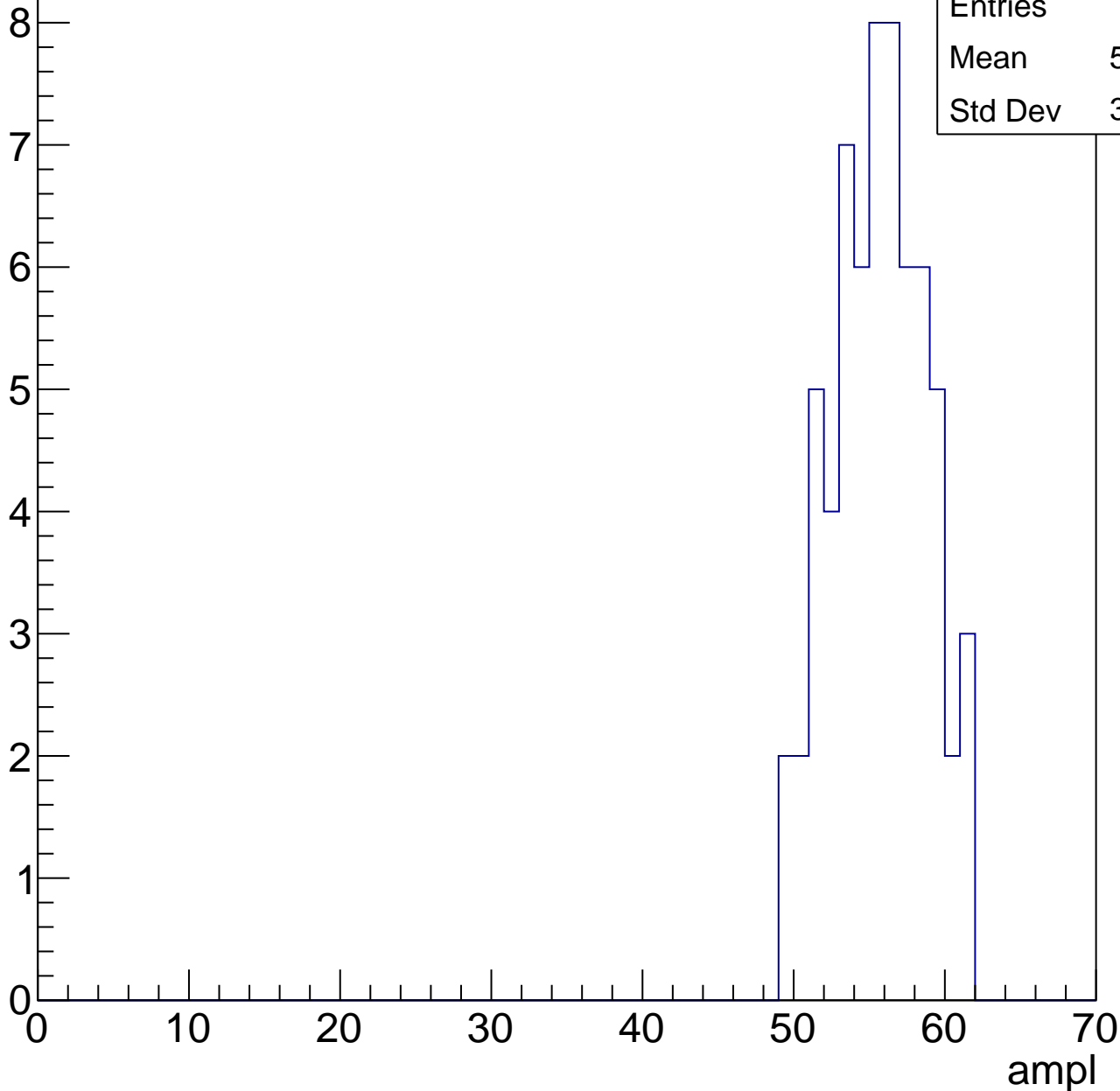


# B1L003S, U26-ch43, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	55.19
Std Dev	3.046



# B1L003S, U26-ch43, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	40
Mean	58.38
Std Dev	9.612

8  
7  
6  
5  
4  
3  
2  
1  
0

ampl

0

10

20

30

40

50

60

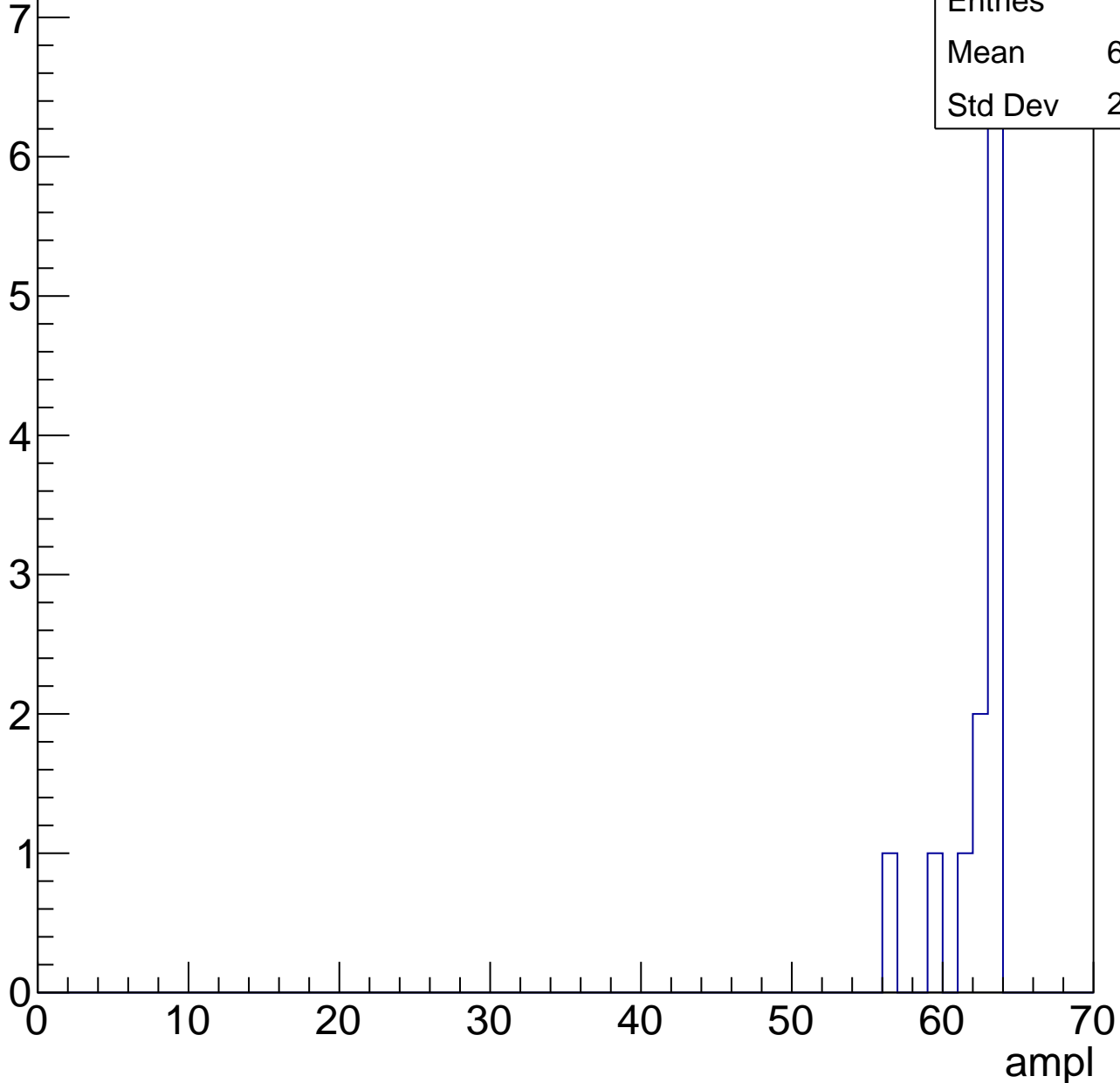
70

# B1L003S, U26-ch43, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	12
Mean	61.75
Std Dev	2.087





# B1L003S, U26-ch43, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U26-ch44, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	89
Mean	28.64
Std Dev	4.772

**Gaus mean : 29.3610**

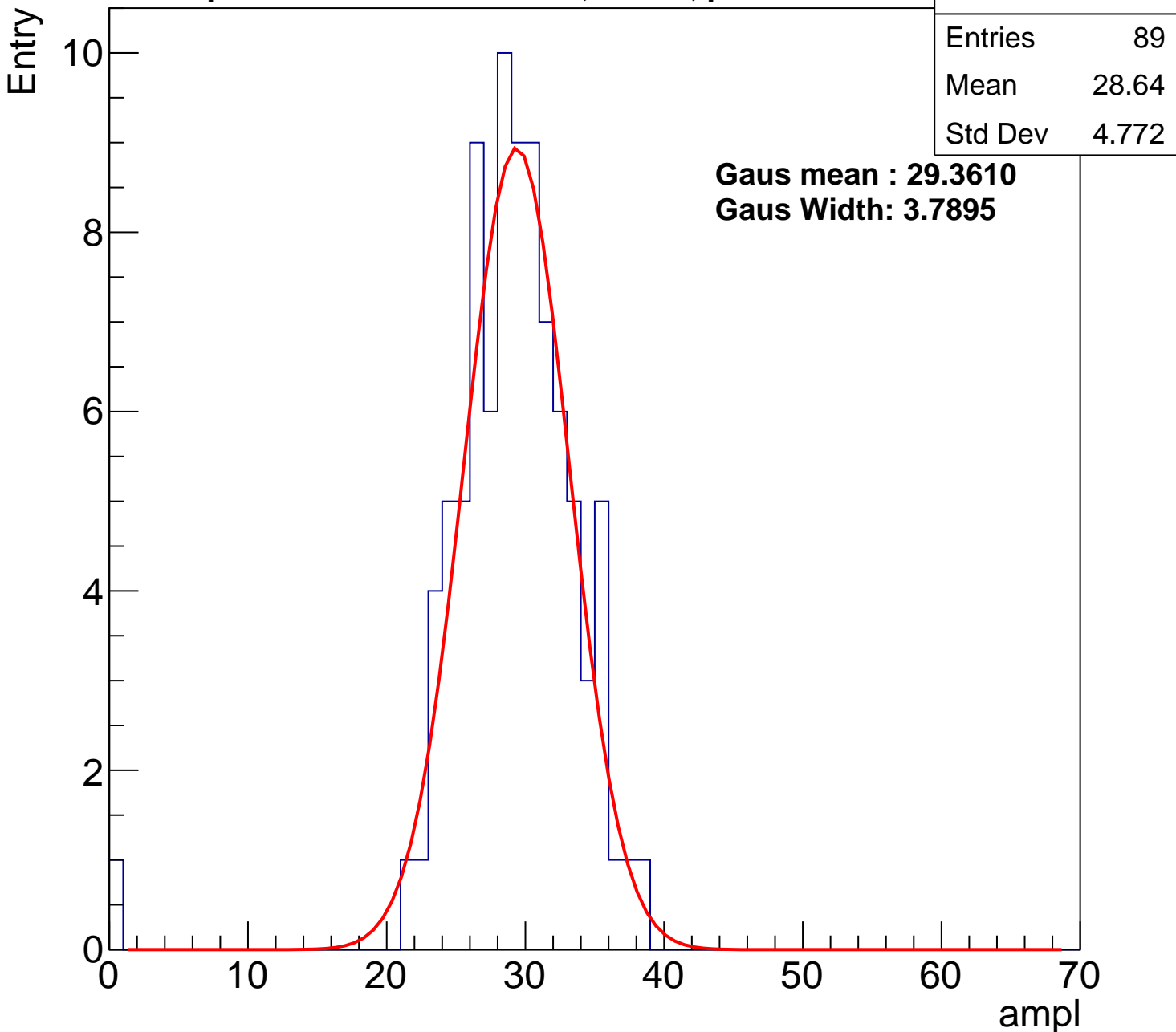
**Gaus Width: 3.7895**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U26-ch44, adc1

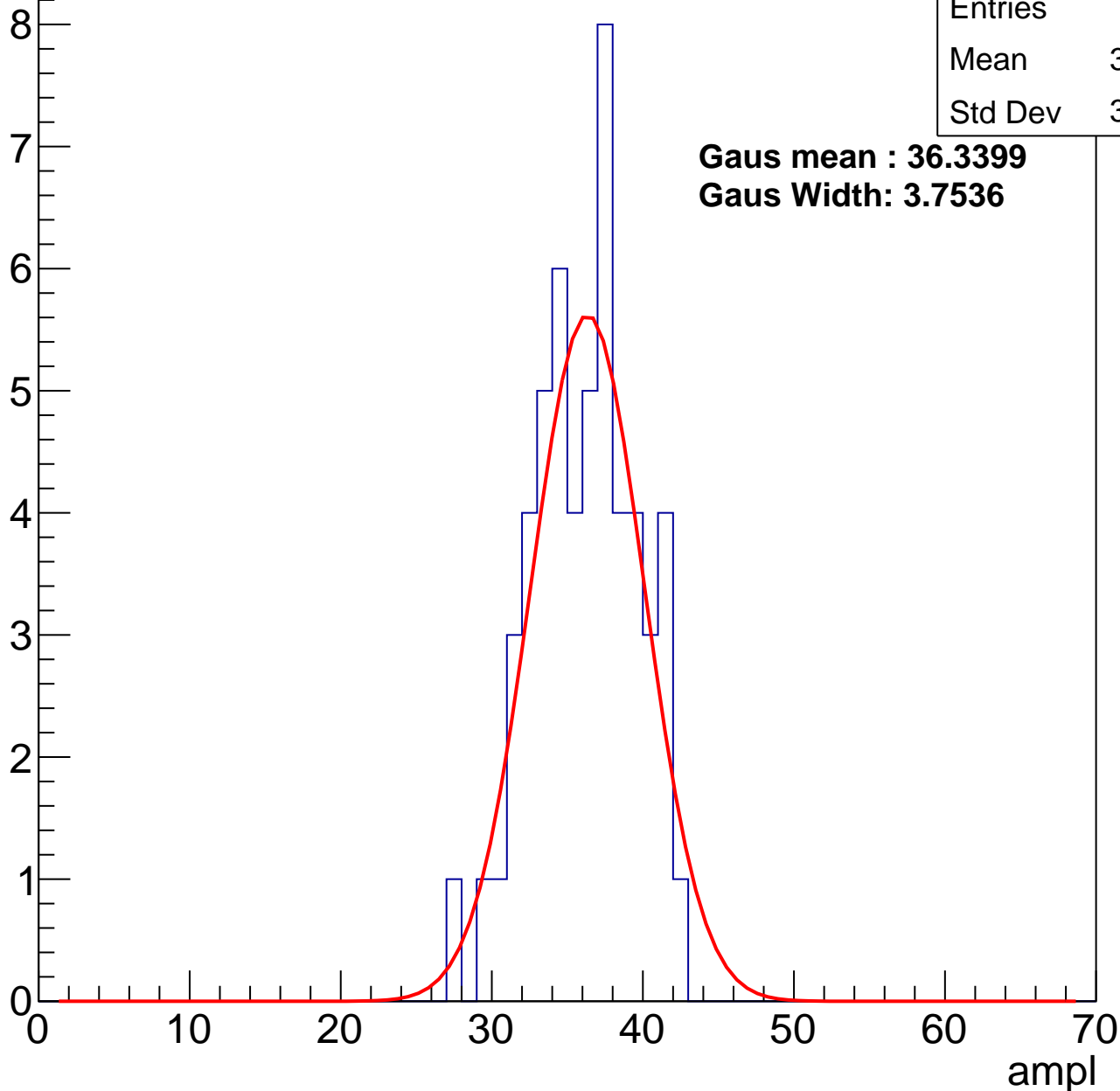
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	54
Mean	35.67
Std Dev	3.377

**Gaus mean : 36.3399**

**Gaus Width: 3.7536**



# B1L003S, U26-ch44, adc2

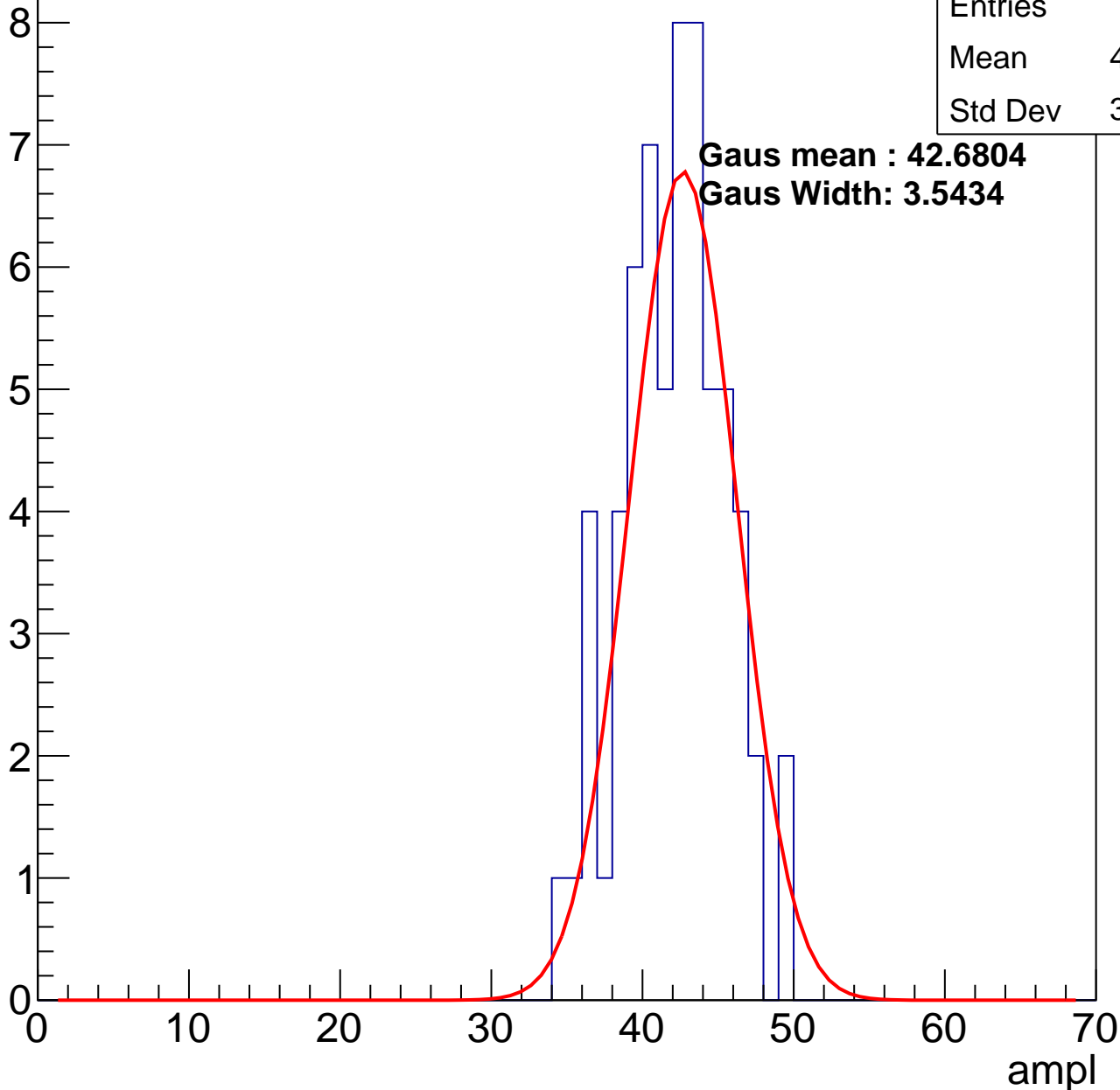
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	41.62
Std Dev	3.354

**Gaus mean : 42.6804**

**Gaus Width: 3.5434**



# B1L003S, U26-ch44, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

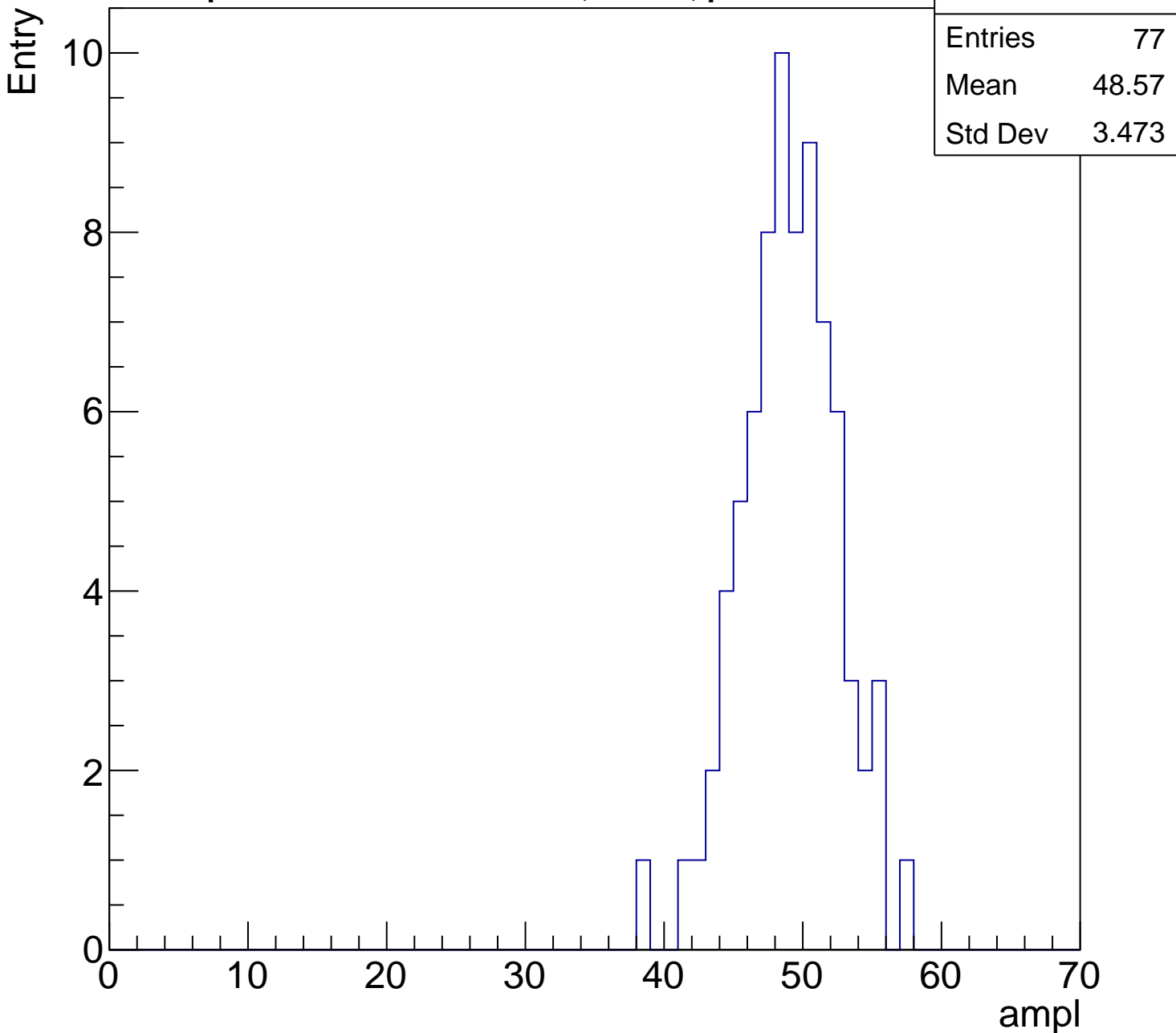
Entries	77
Mean	48.57
Std Dev	3.473

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

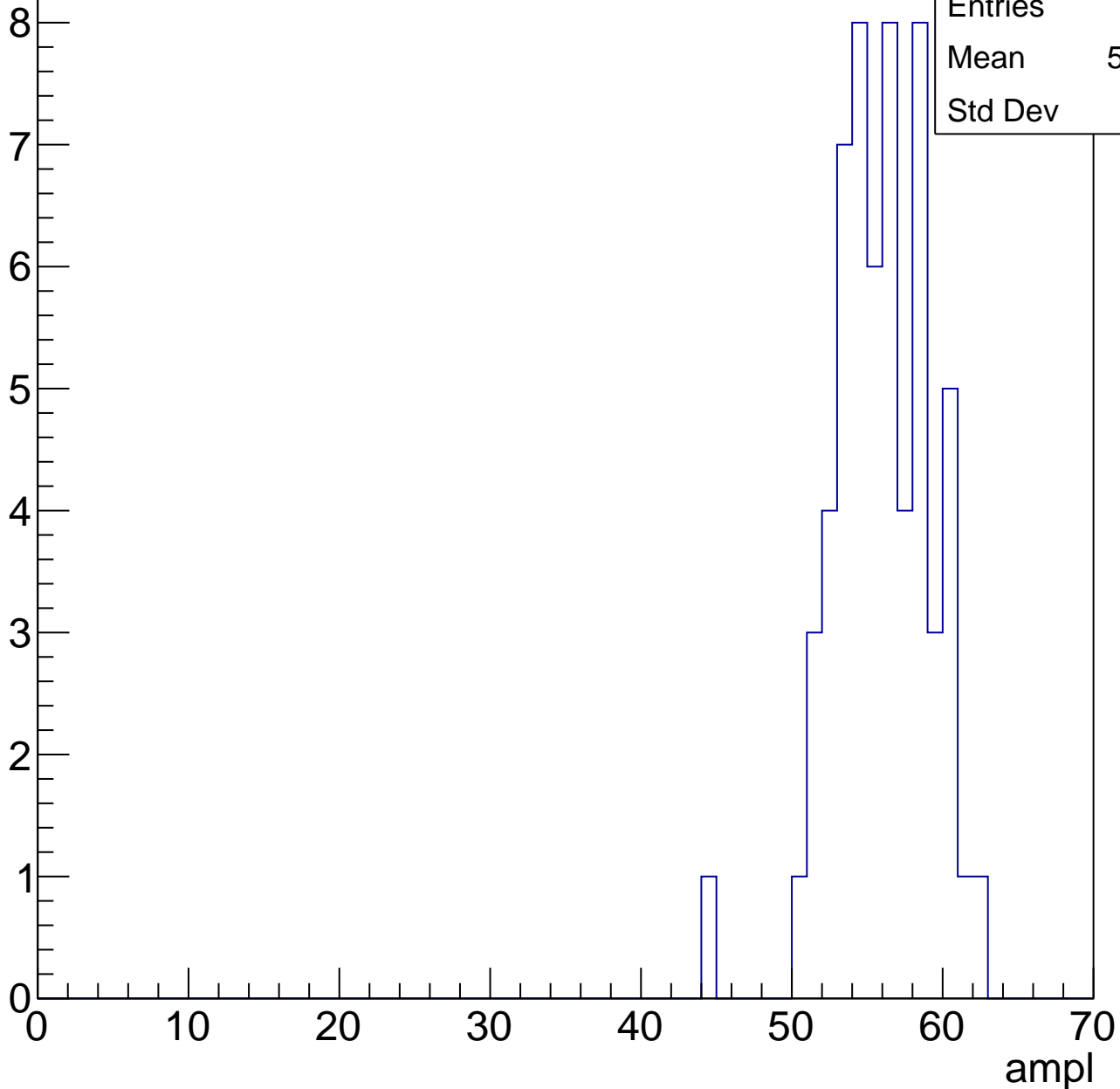


# B1L003S, U26-ch44, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	55.47
Std Dev	3.18



# B1L003S, U26-ch44, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

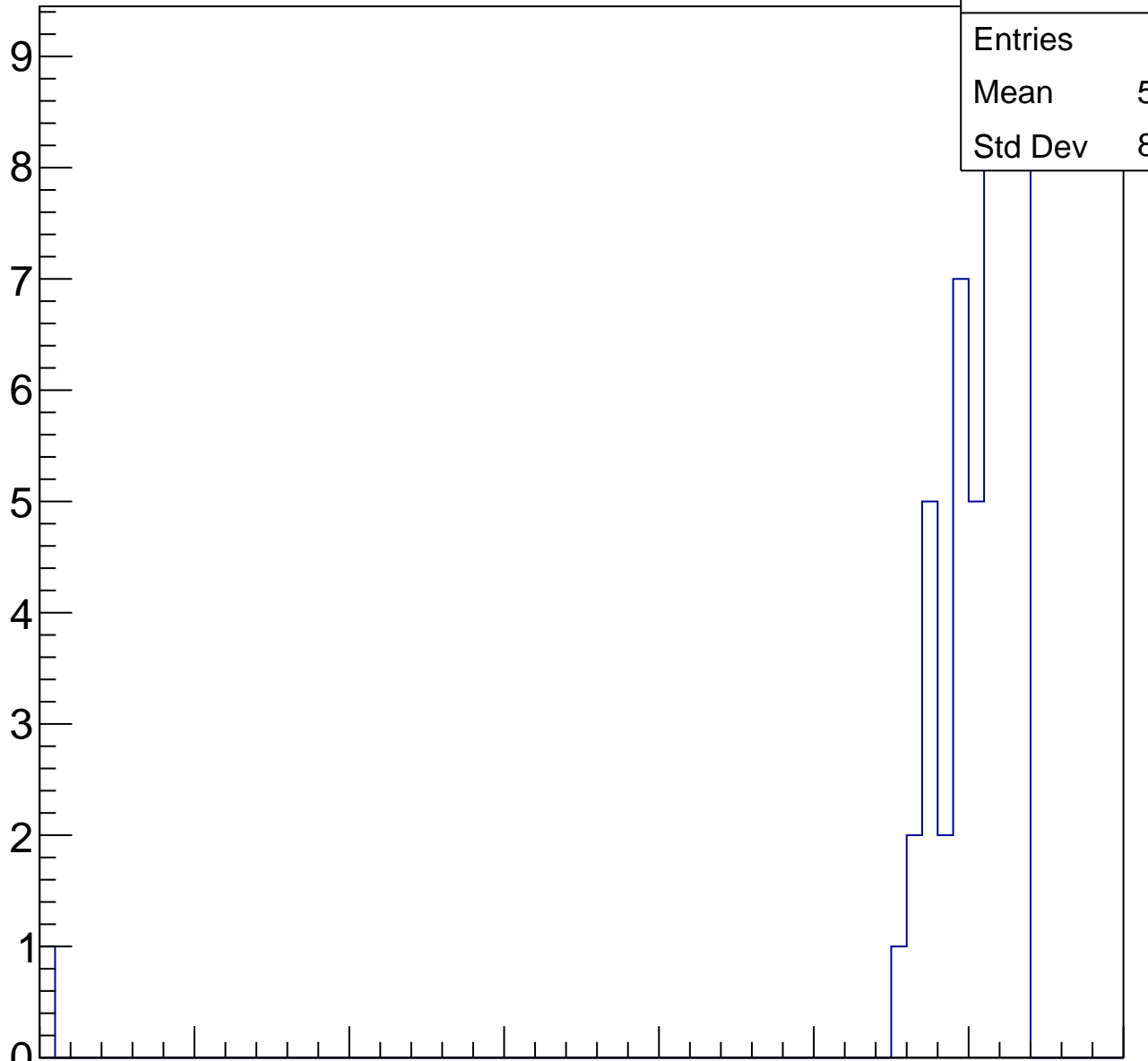
Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	49
Mean	59.04
Std Dev	8.799

ampl

0 10 20 30 40 50 60 70



# B1L003S, U26-ch44, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch44, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U26-ch45, adc0

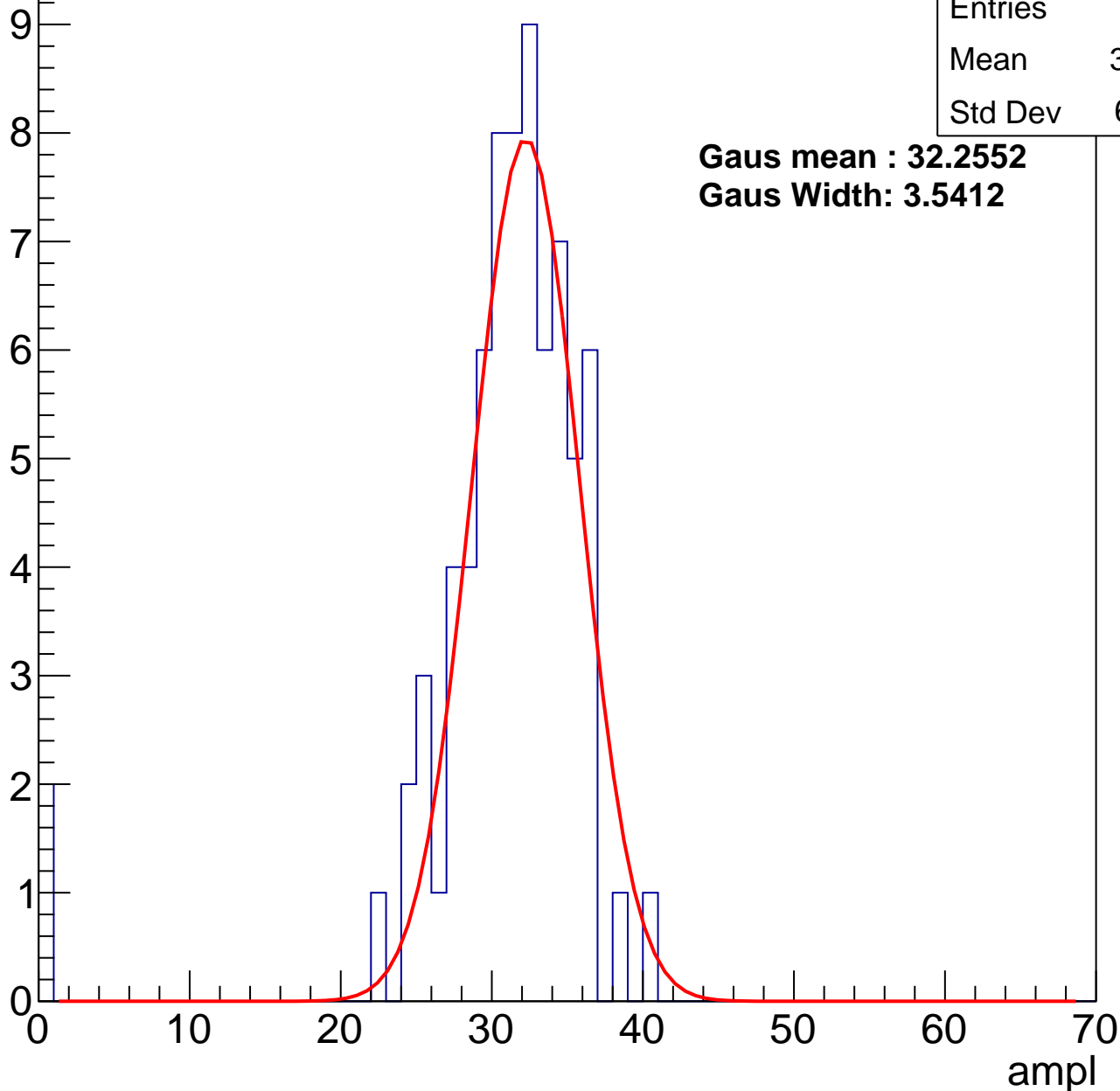
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	74
Mean	30.35
Std Dev	6.141

**Gaus mean : 32.2552**

**Gaus Width: 3.5412**



# B1L003S, U26-ch45, adc1

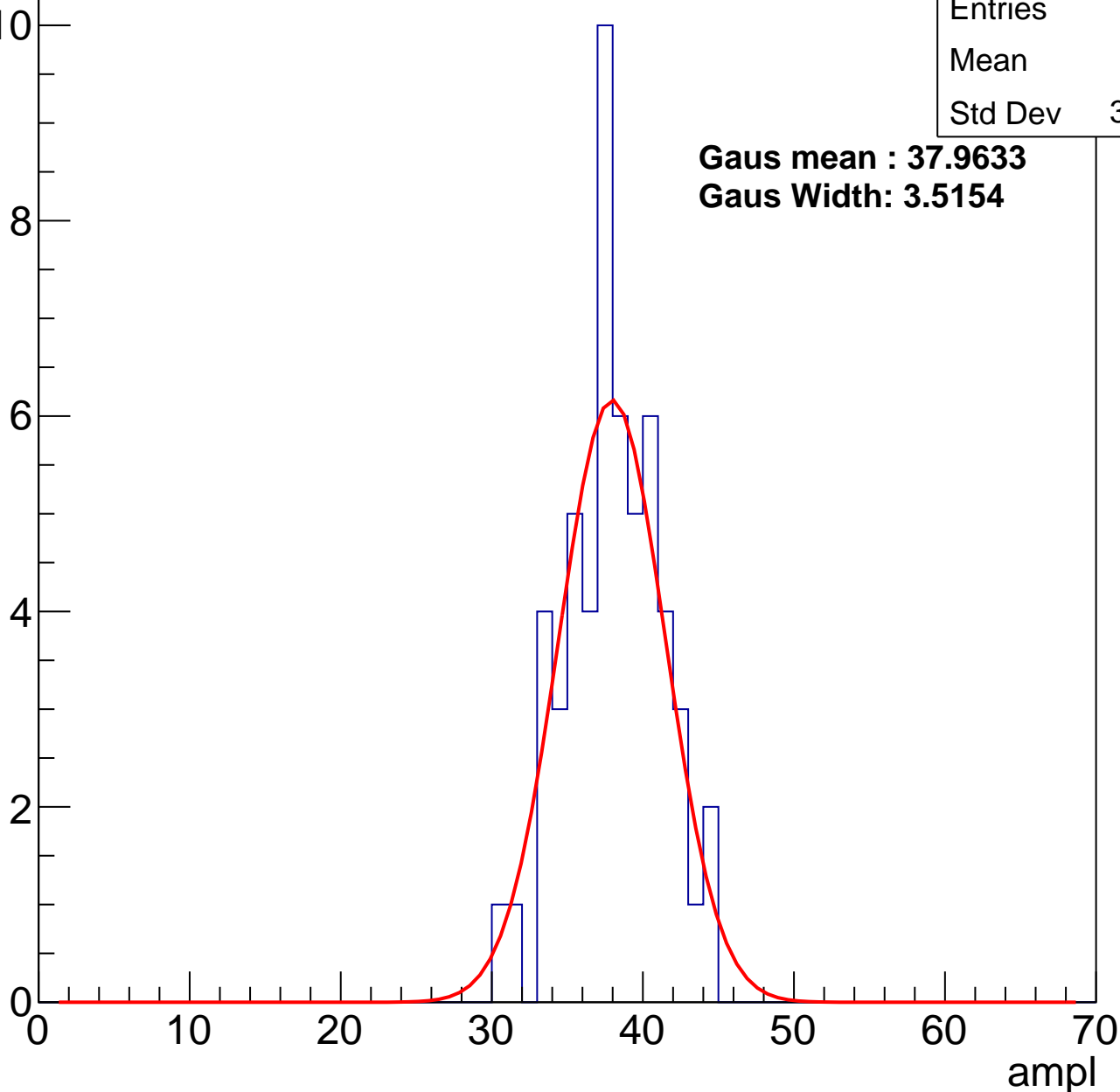
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	37.6
Std Dev	3.114

**Gaus mean : 37.9633**

**Gaus Width: 3.5154**



# B1L003S, U26-ch45, adc2

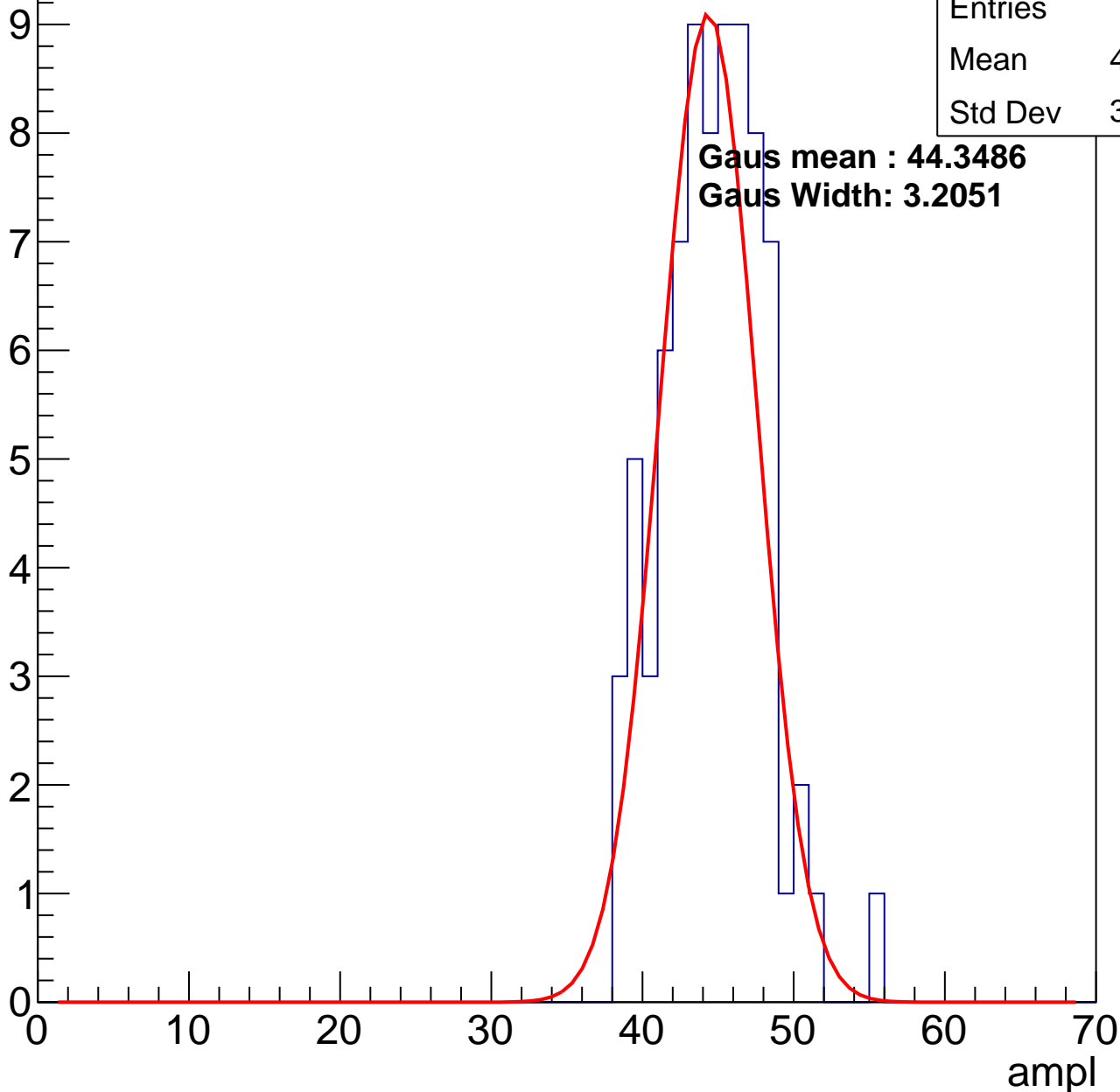
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	79
Mean	44.23
Std Dev	3.307

**Gaus mean : 44.3486**

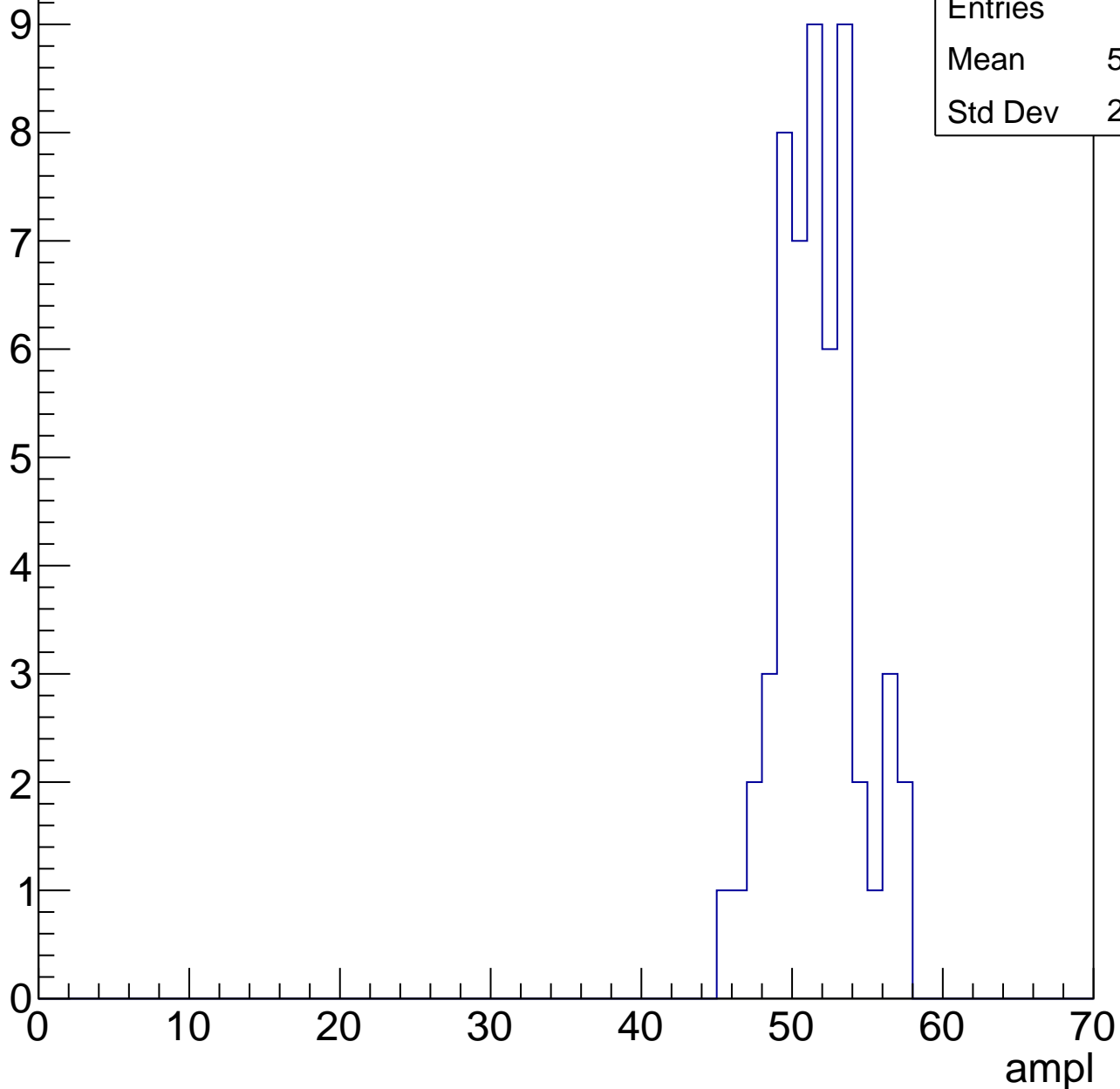
**Gaus Width: 3.2051**



# B1L003S, U26-ch45, adc3

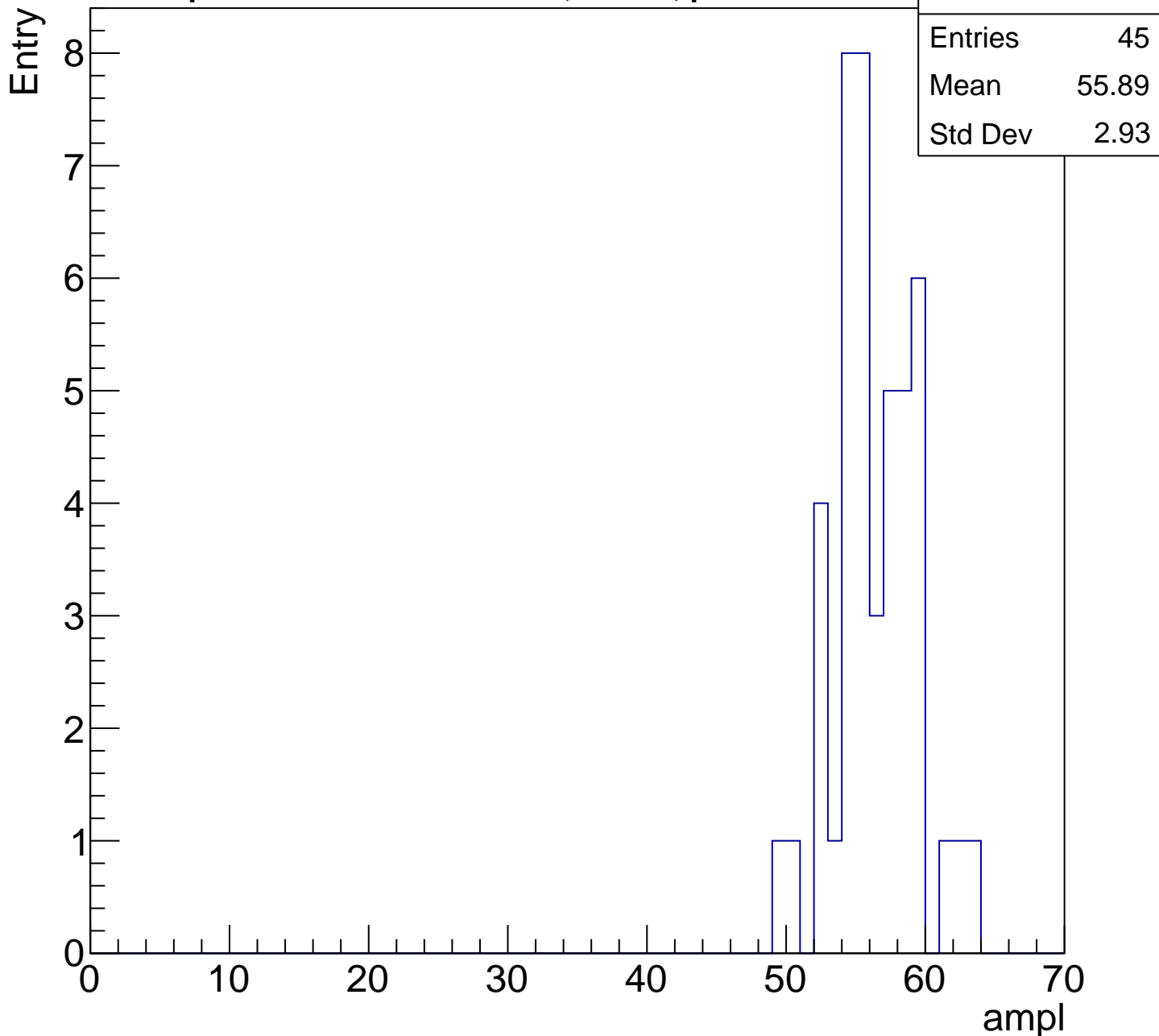
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U26-ch45, adc4

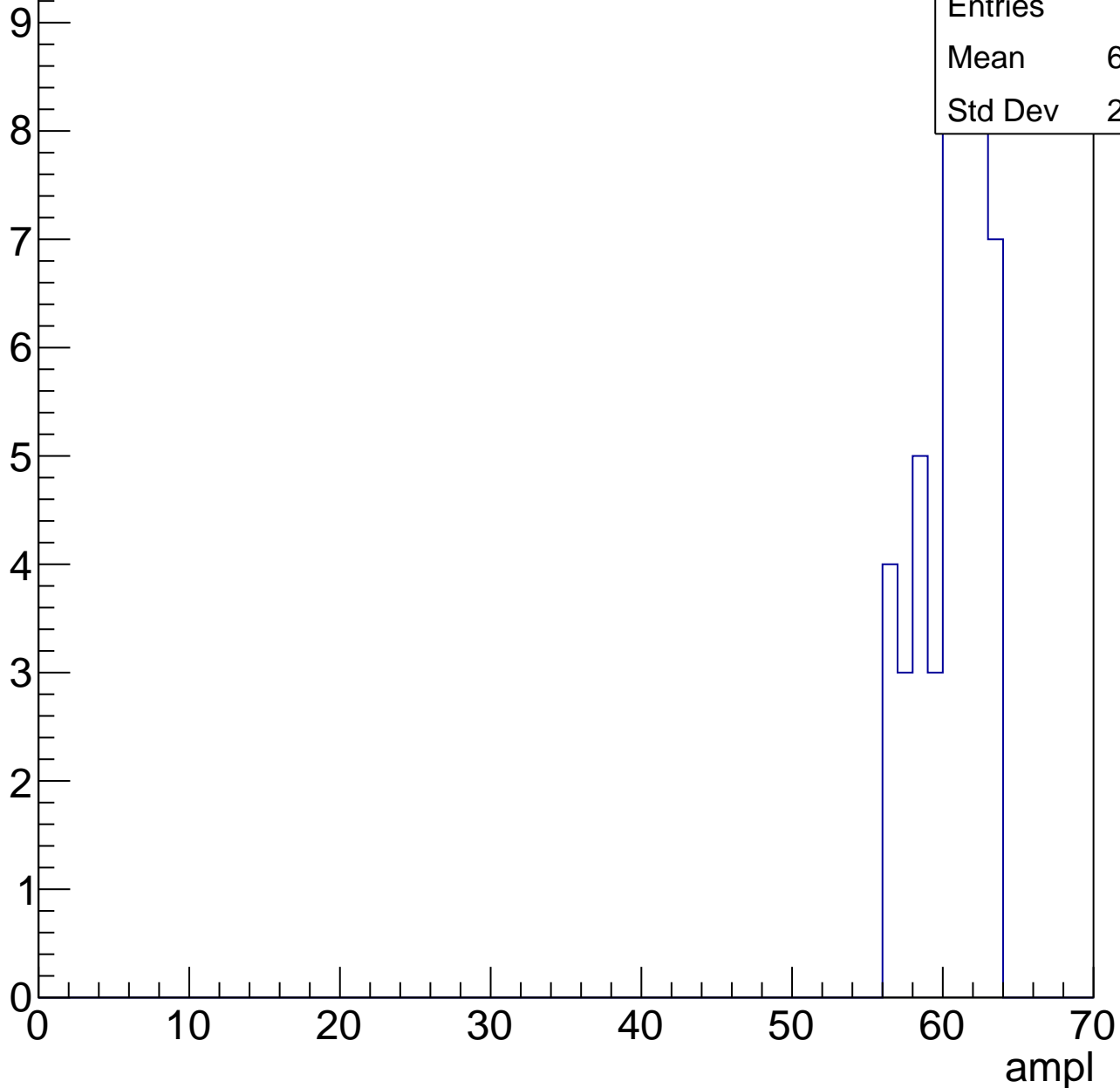
calib\_packv5\_042523\_0143.root, FC#13, port D2



# B1L003S, U26-ch45, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

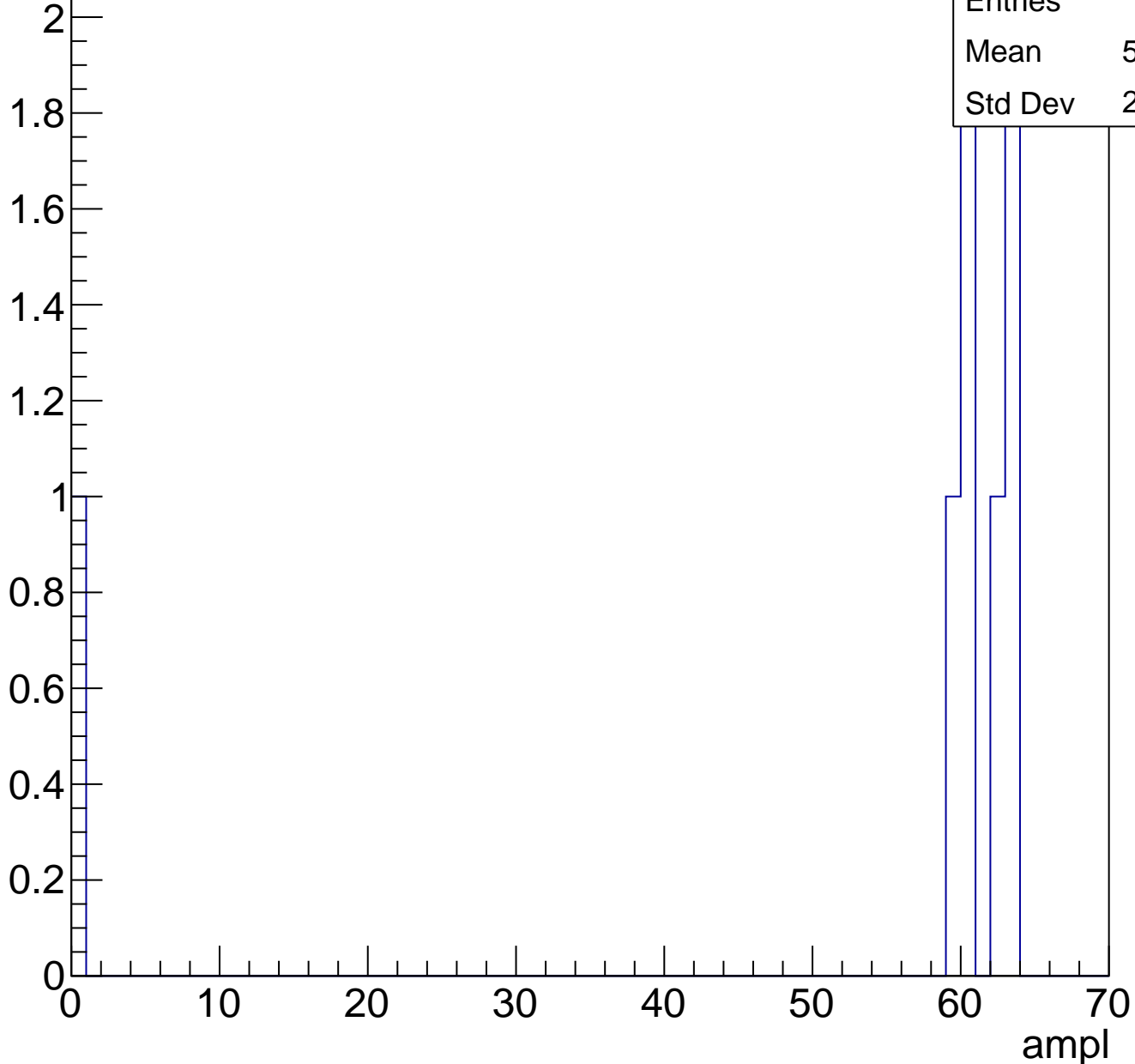


Entries	47
Mean	60.17
Std Dev	2.147

# B1L003S, U26-ch45, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	7
Mean	52.43
Std Dev	21.45



# B1L003S, U26-ch45, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U26-ch46, adc0

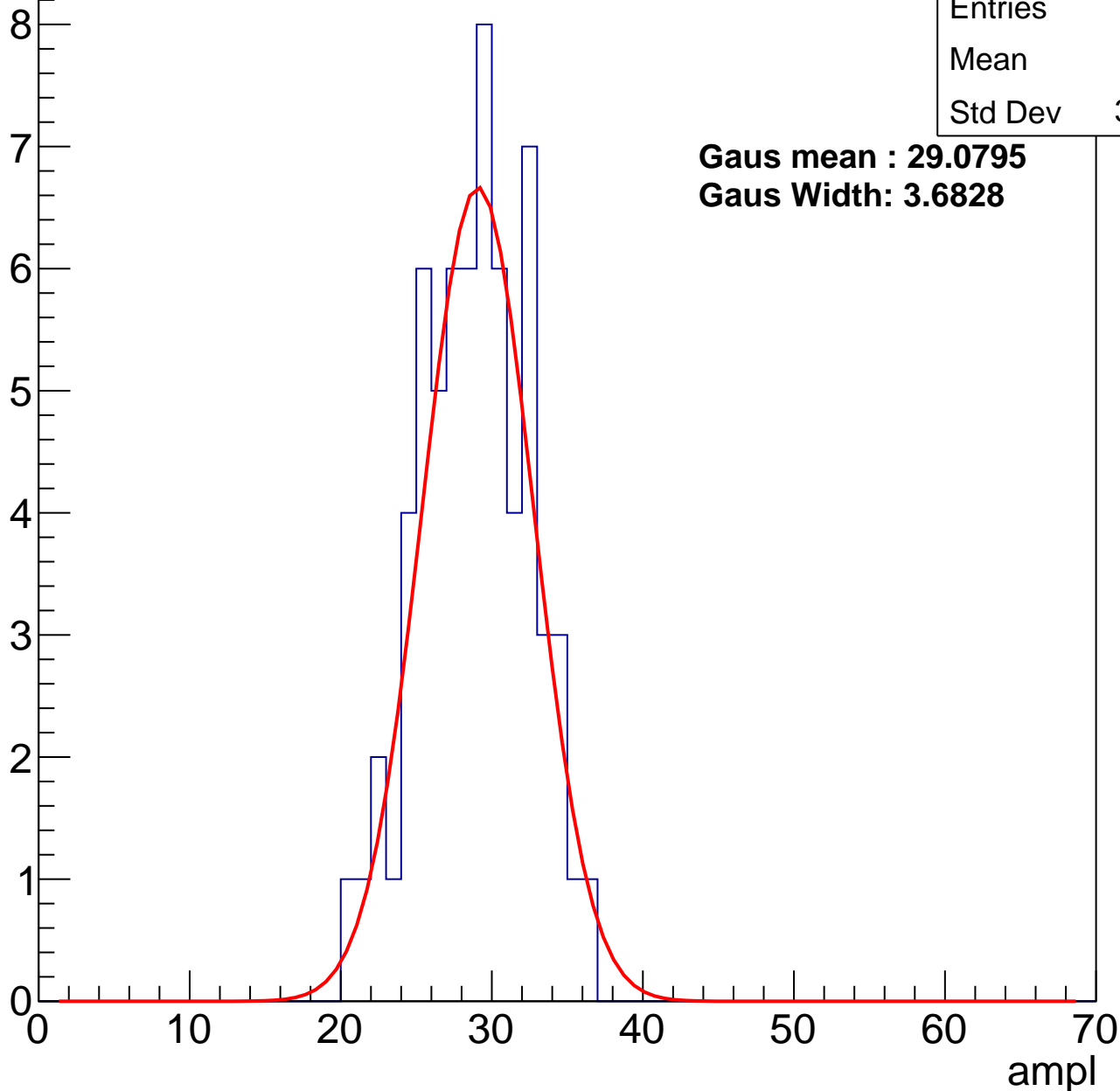
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	28.4
Std Dev	3.551

**Gaus mean : 29.0795**

**Gaus Width: 3.6828**



# B1L003S, U26-ch46, adc1

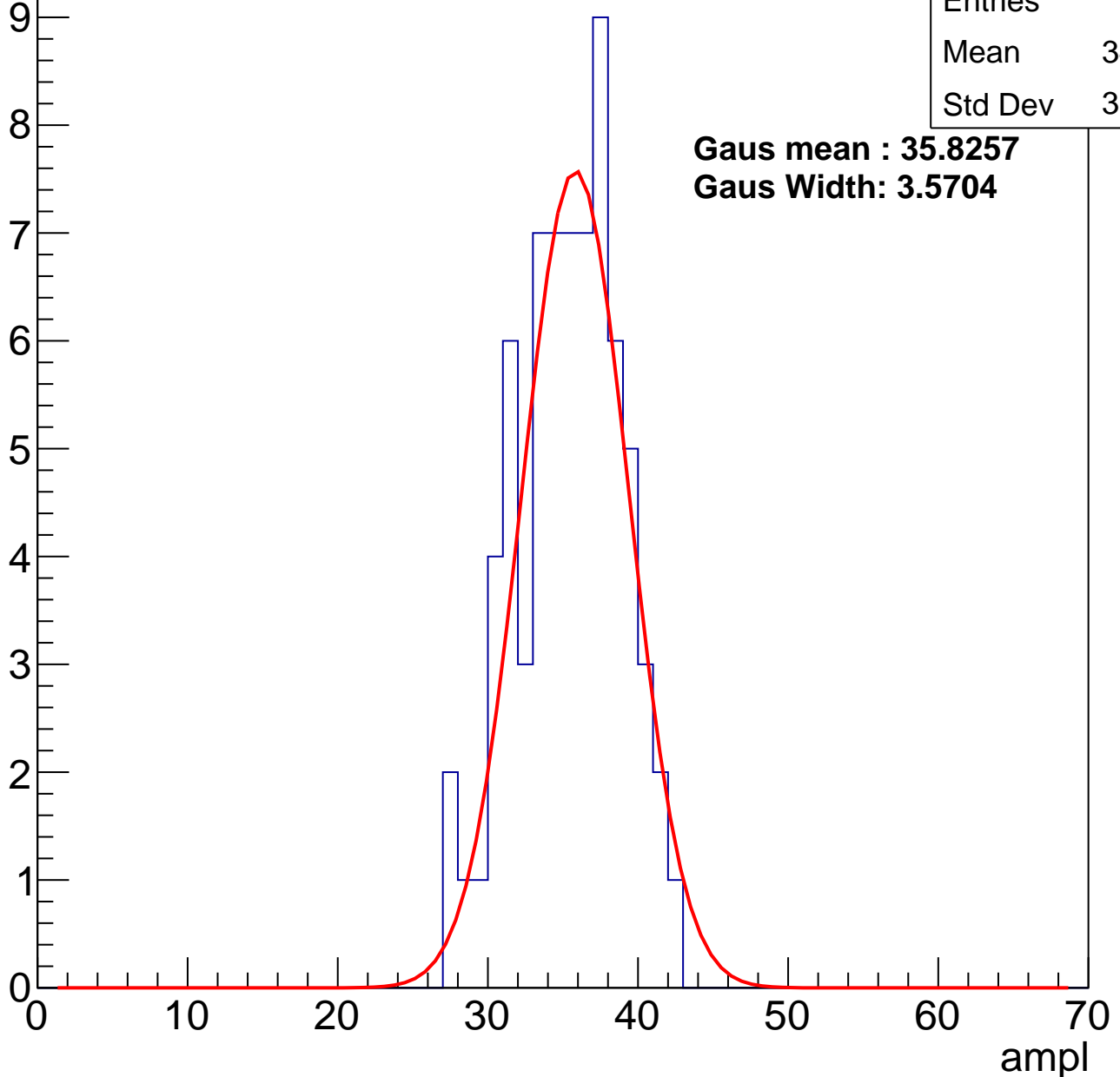
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	71
Mean	34.92
Std Dev	3.447

**Gaus mean : 35.8257**

**Gaus Width: 3.5704**



# B1L003S, U26-ch46, adc2

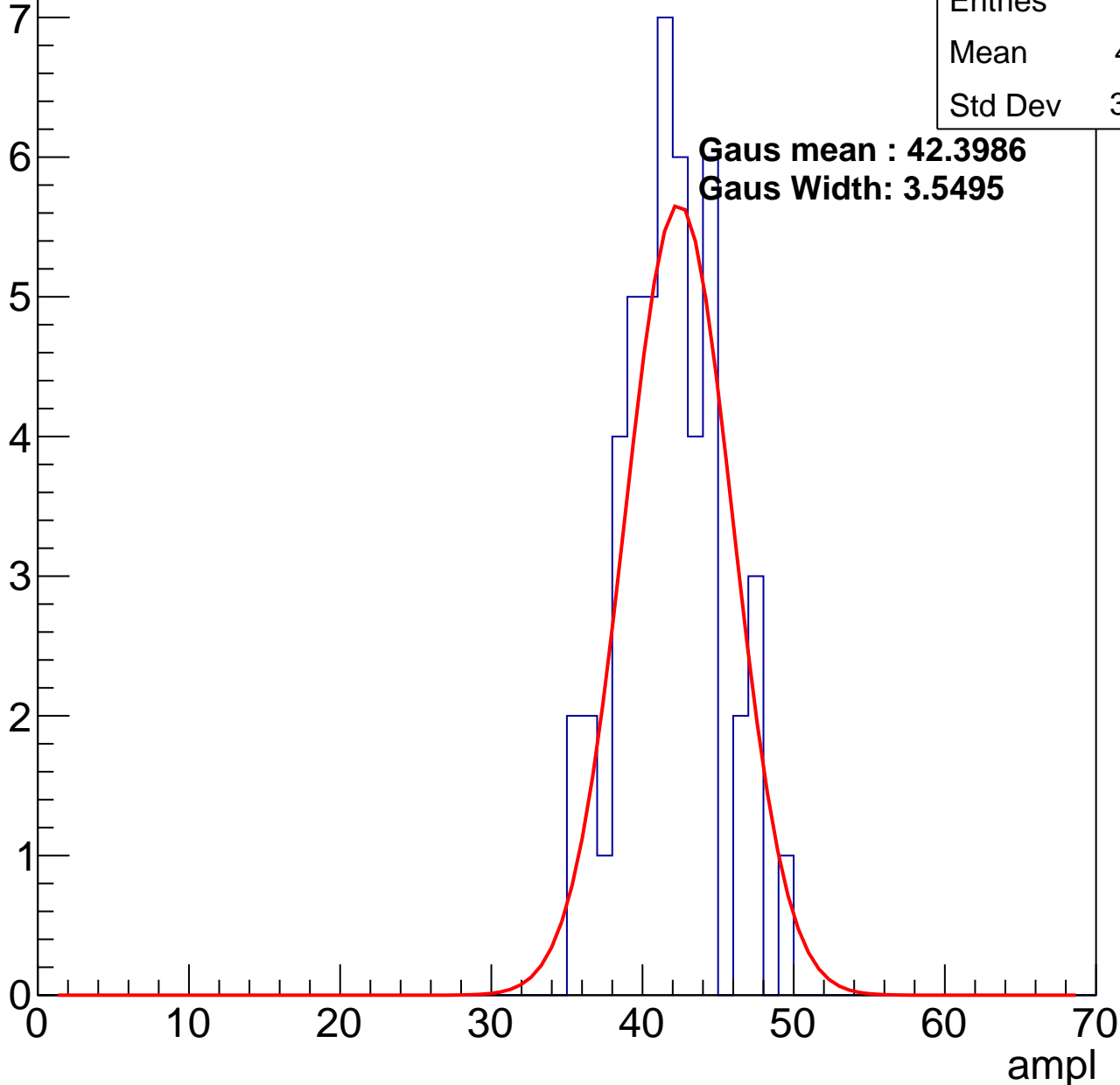
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	48
Mean	41.31
Std Dev	3.203

**Gaus mean : 42.3986**

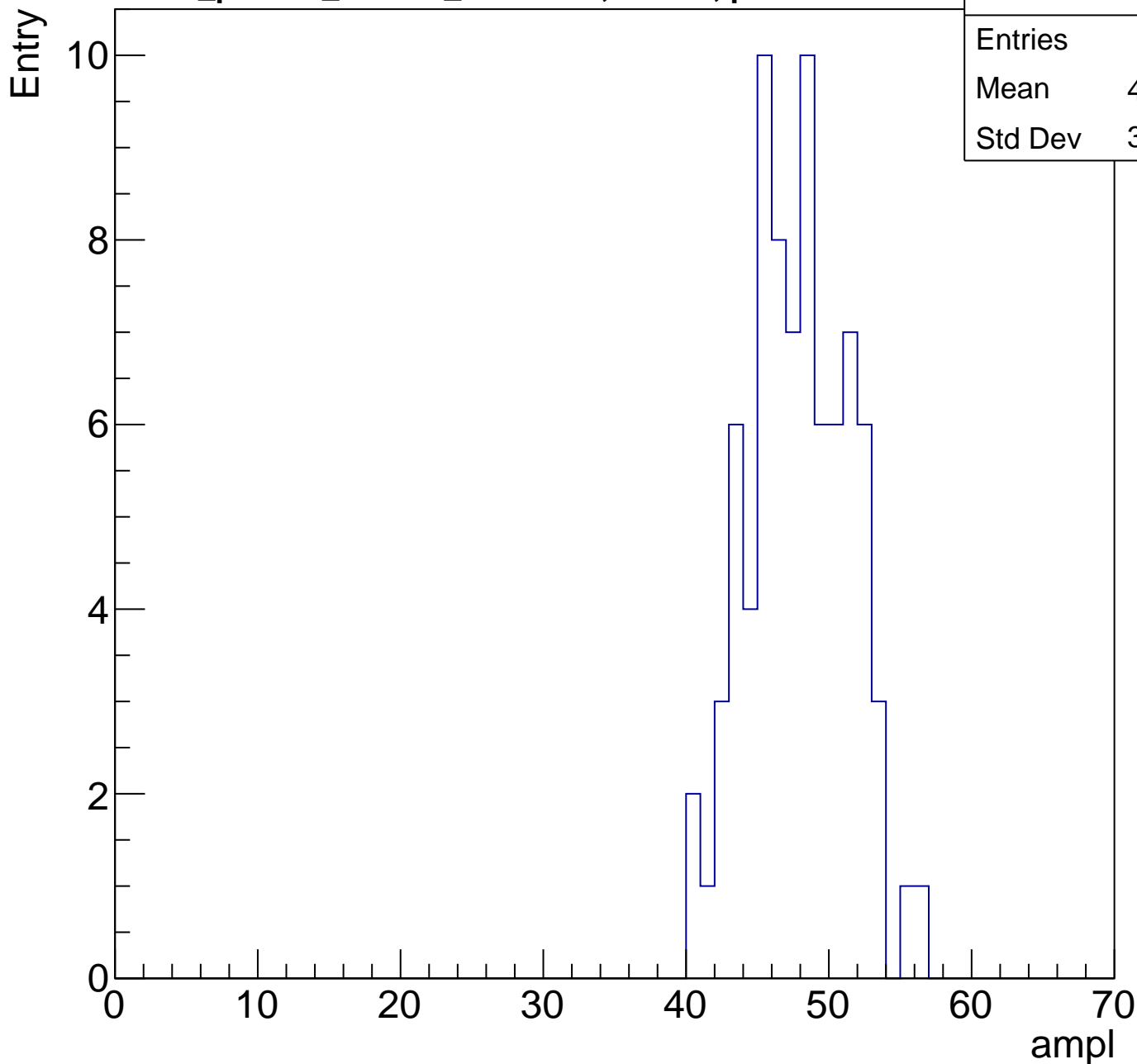
**Gaus Width: 3.5495**



# B1L003S, U26-ch46, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	81
Mean	47.42
Std Dev	3.474

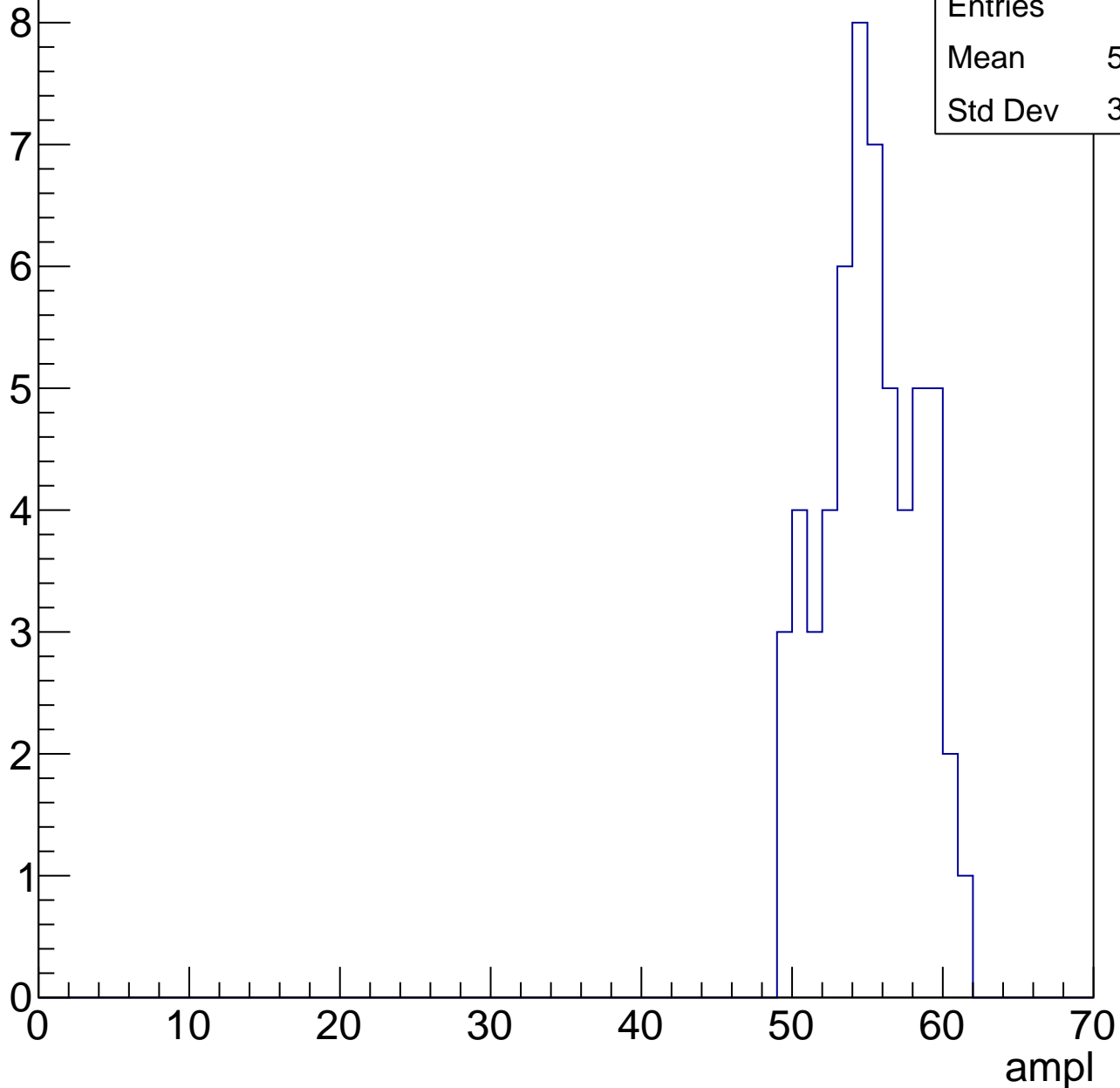


# B1L003S, U26-ch46, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	54.68
Std Dev	3.107

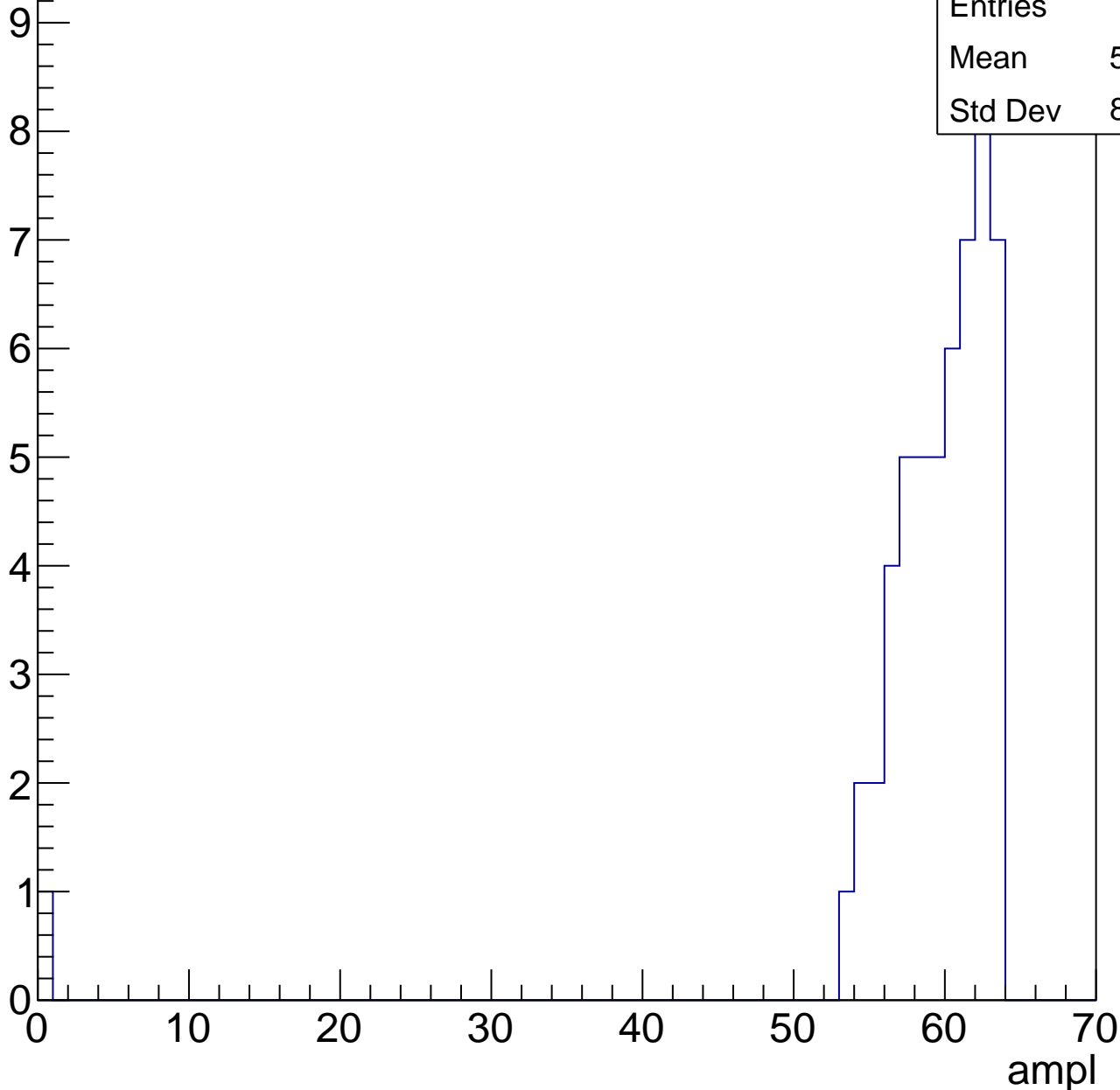


# B1L003S, U26-ch46, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	54
Mean	58.35
Std Dev	8.459



# B1L003S, U26-ch46, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

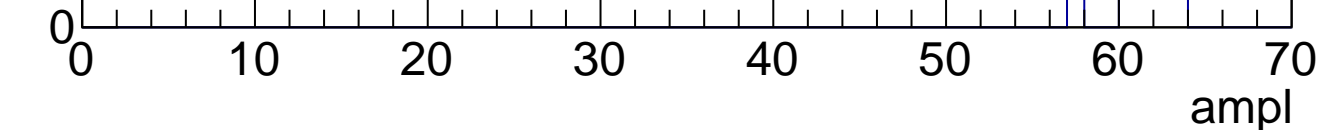
40

50

60

ampl

Entries	9
Mean	61.11
Std Dev	1.853





# B1L003S, U26-ch46, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U26-ch47, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	60
Mean	28.58
Std Dev	2.512

**Gaus mean : 29.0137**

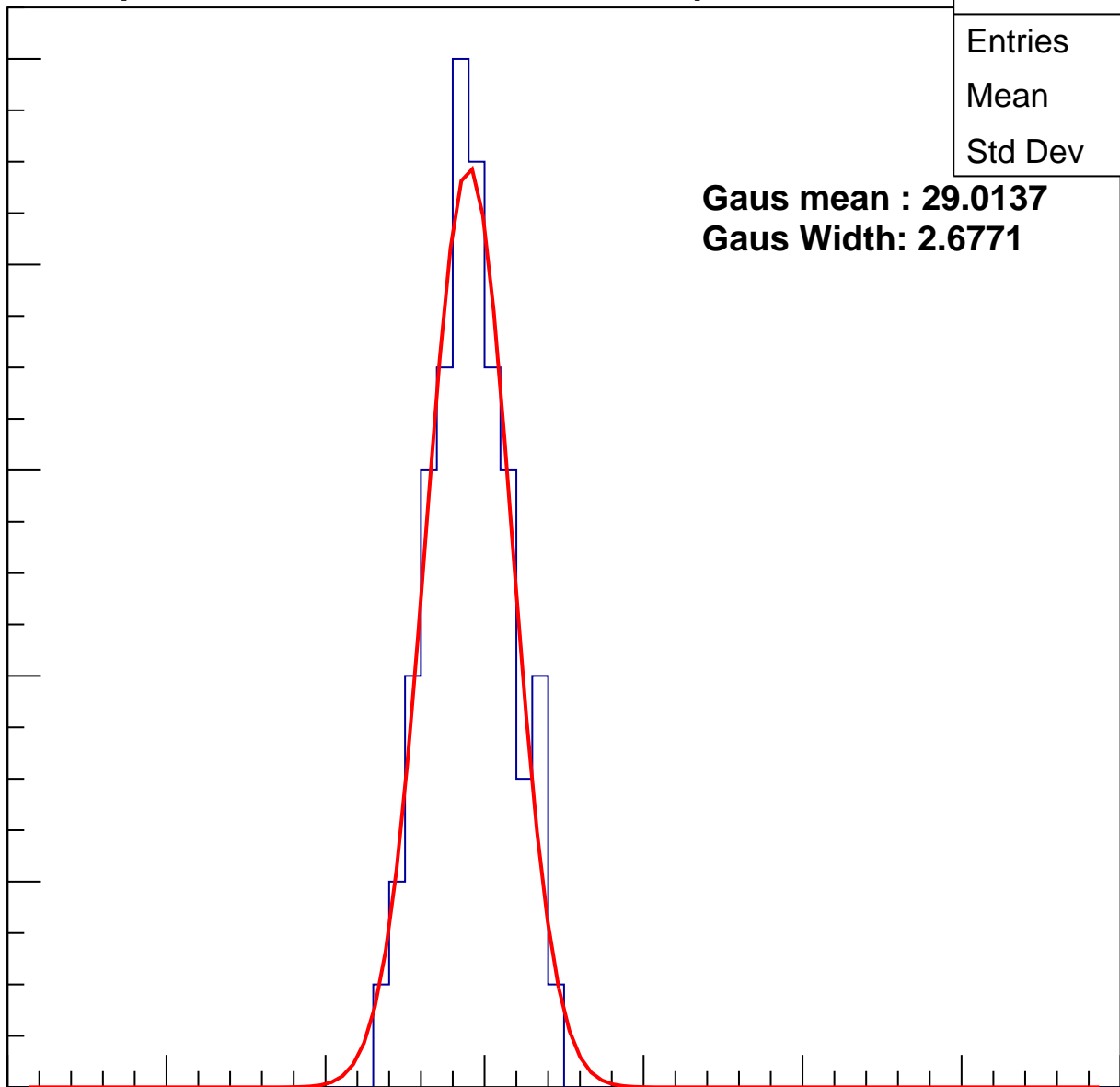
**Gaus Width: 2.6771**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U26-ch47, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	72
Mean	35.15
Std Dev	2.832

**Gaus mean : 35.6470**

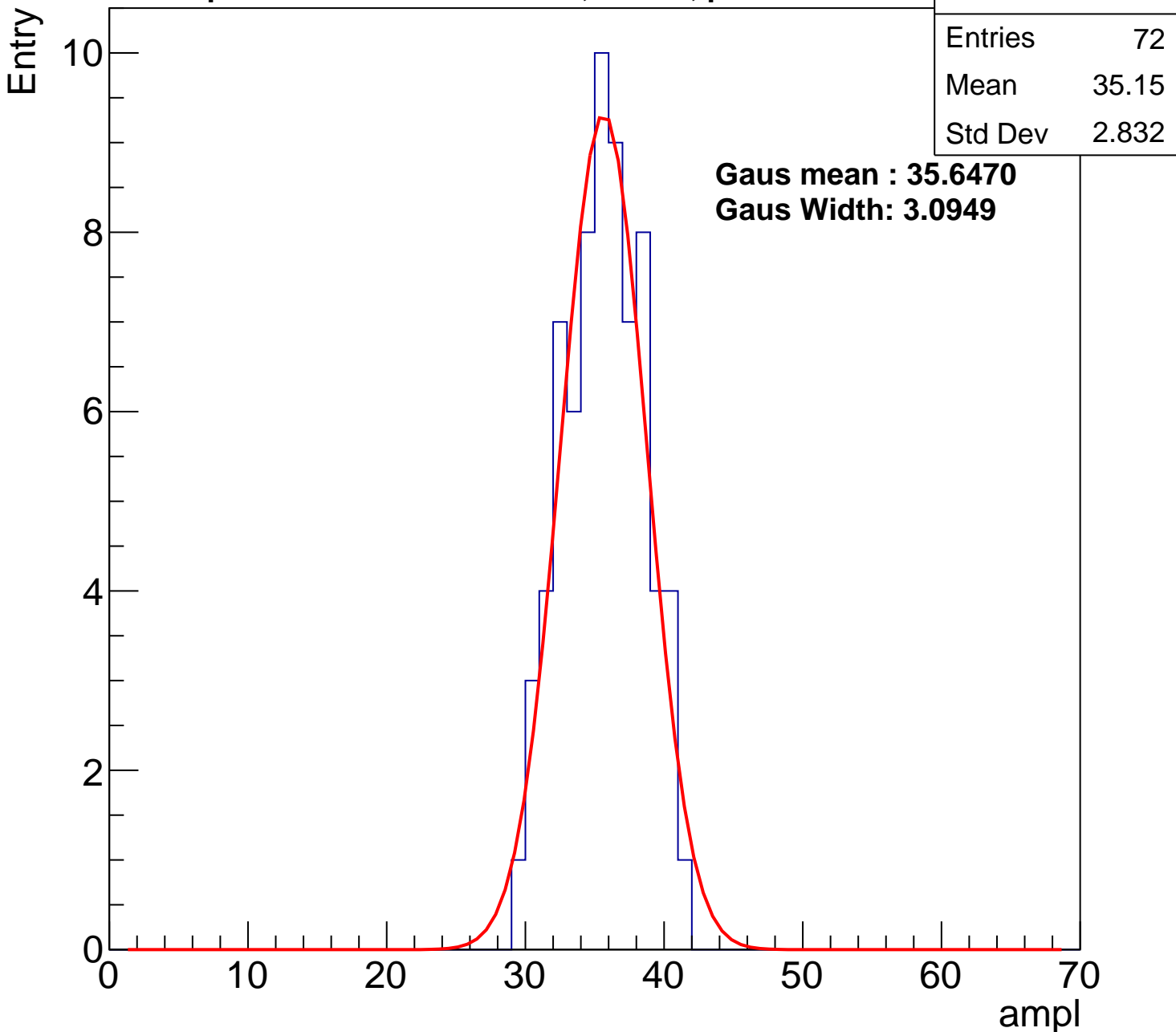
**Gaus Width: 3.0949**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U26-ch47, adc2

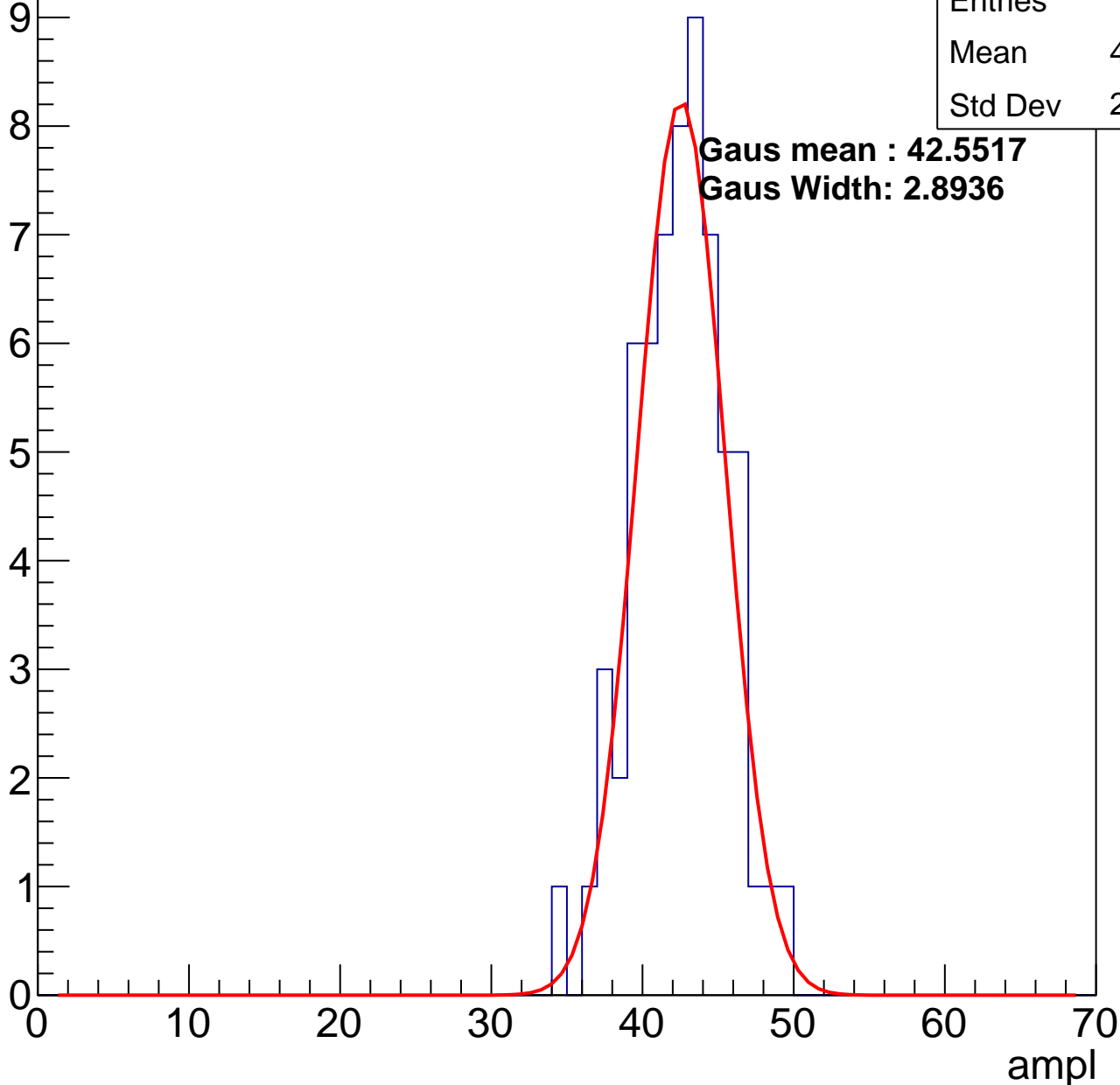
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	42.03
Std Dev	2.992

**Gaus mean : 42.5517**

**Gaus Width: 2.8936**

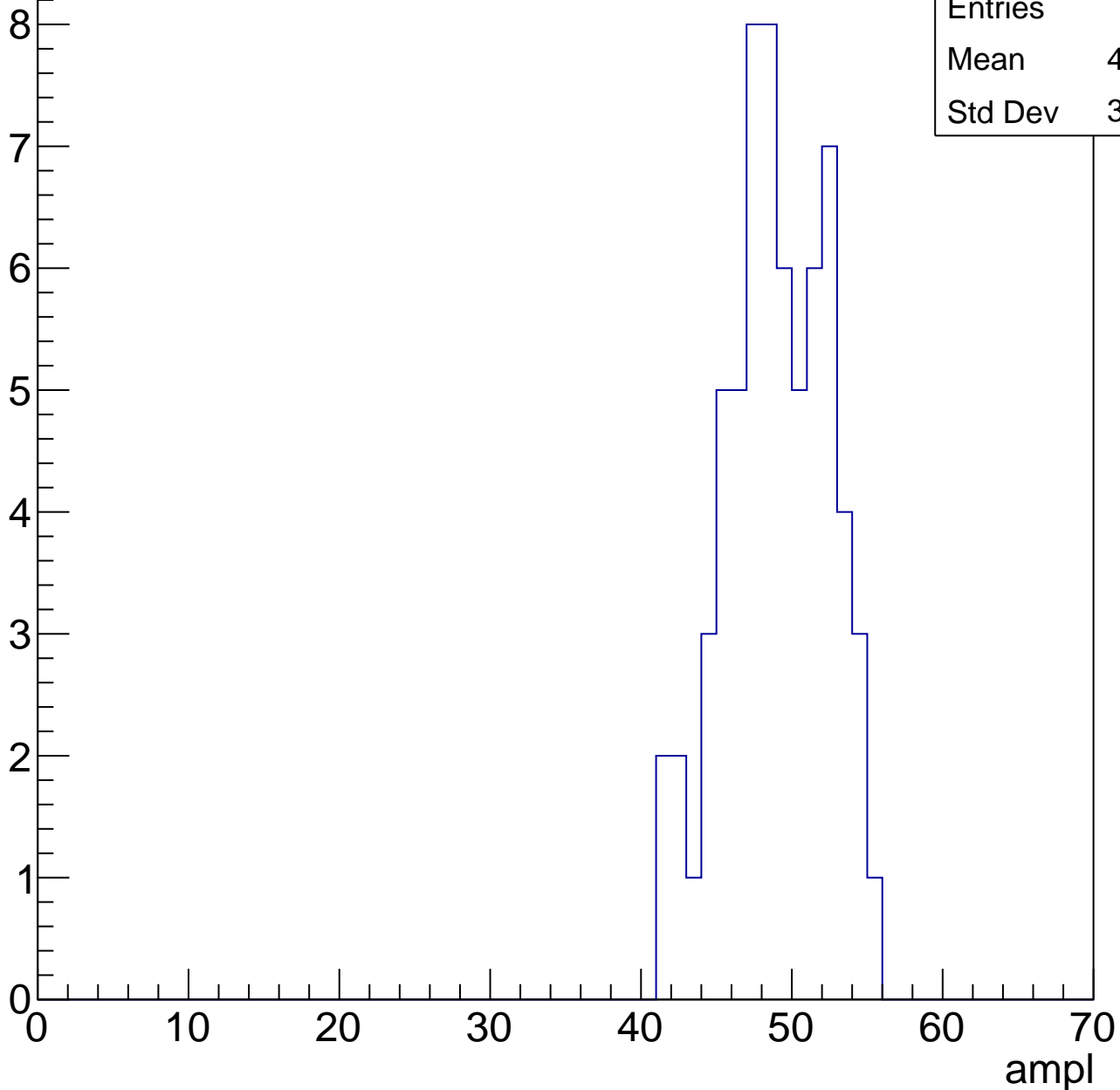


# B1L003S, U26-ch47, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	48.47
Std Dev	3.372

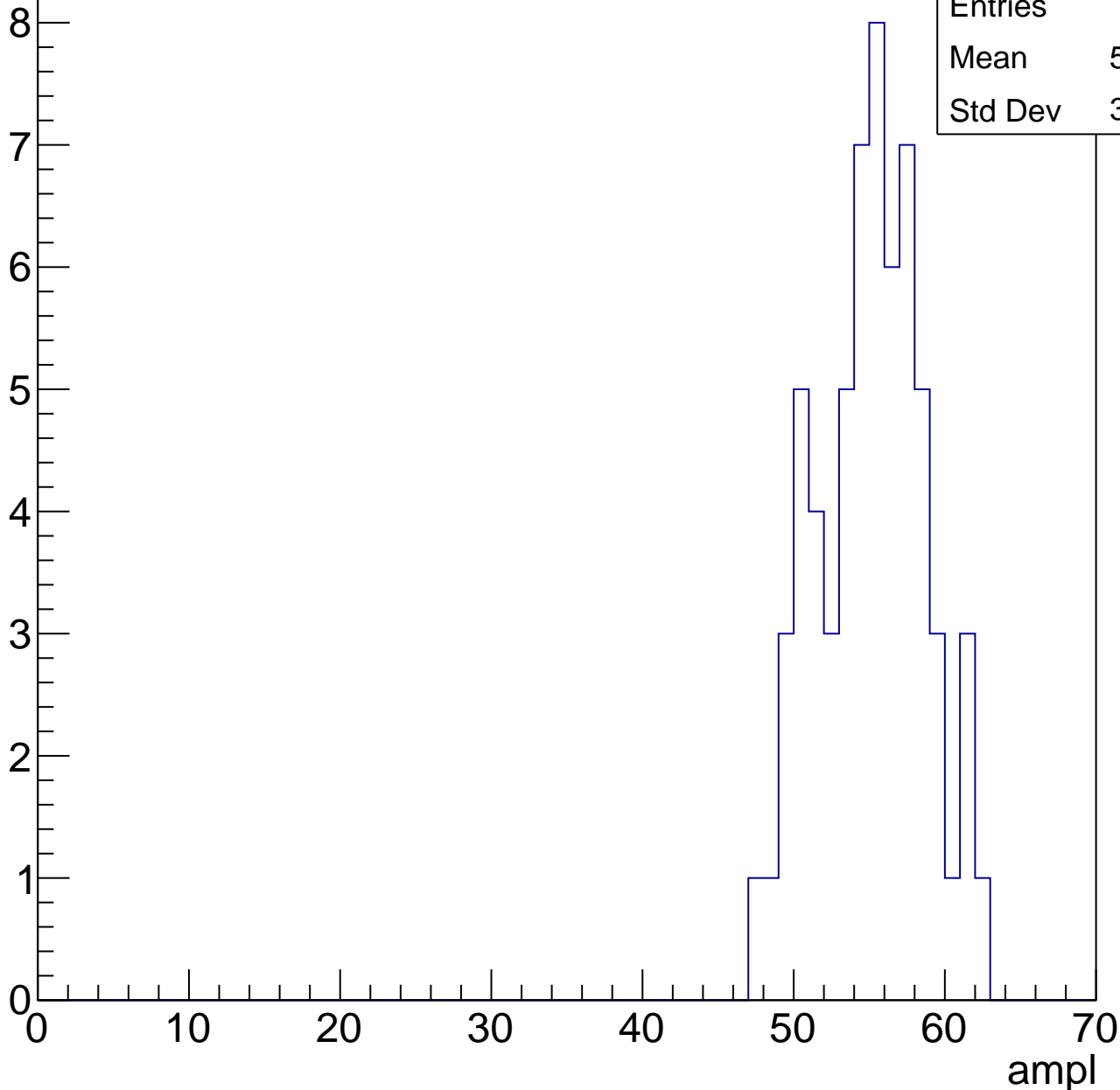


# B1L003S, U26-ch47, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	54.63
Std Dev	3.484

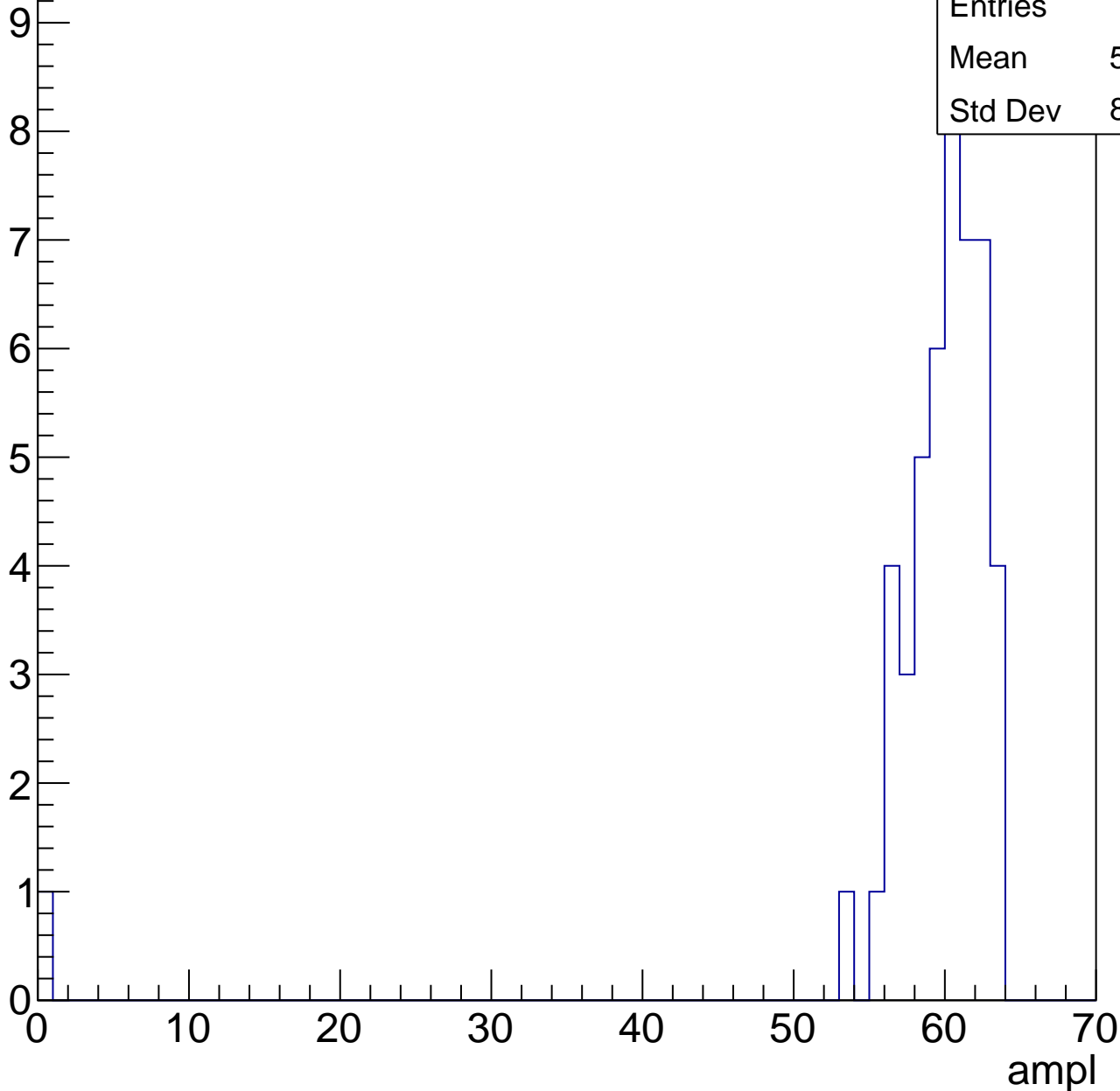


# B1L003S, U26-ch47, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	48
Mean	58.33
Std Dev	8.814

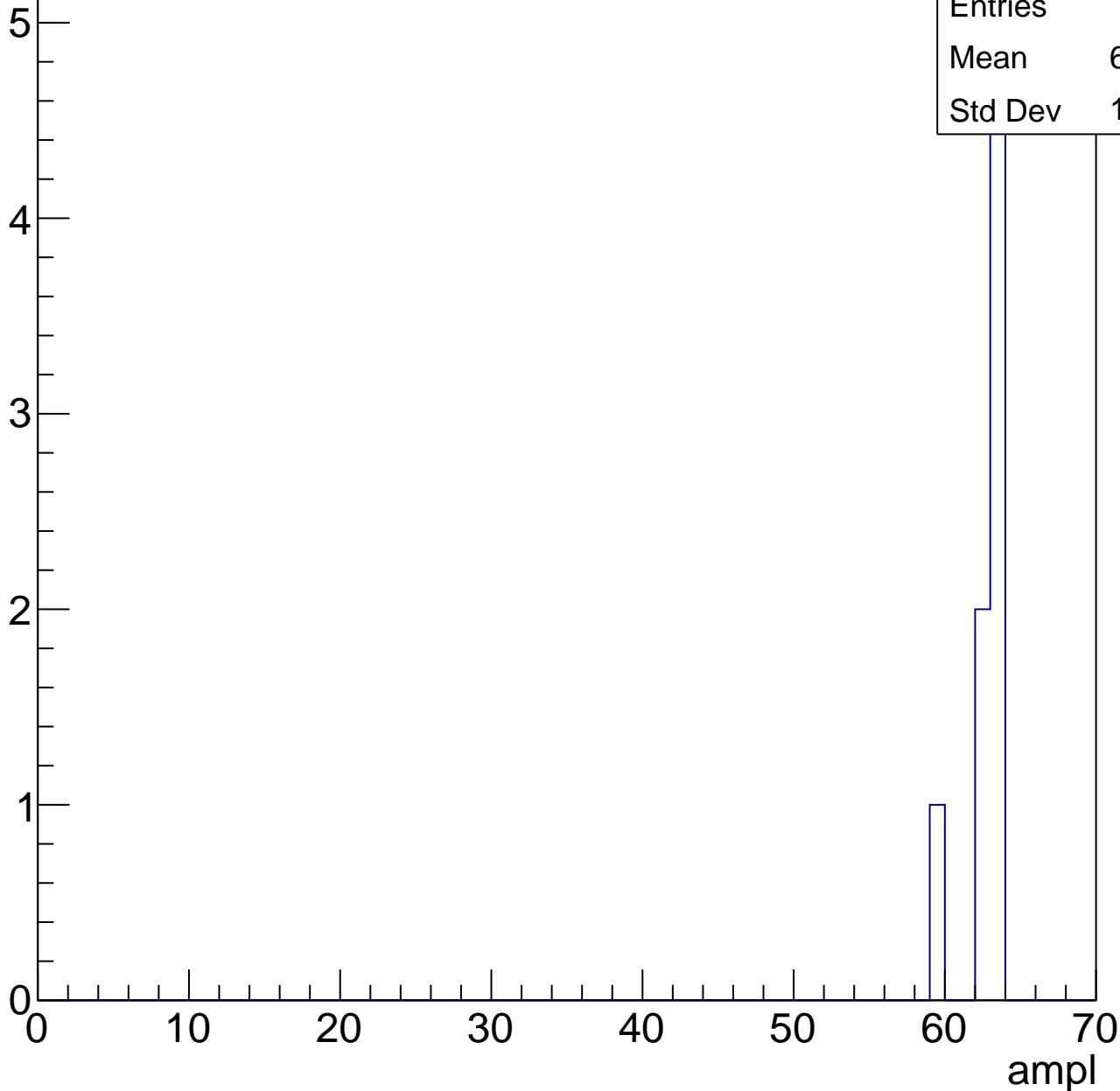


# B1L003S, U26-ch47, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	8
Mean	62.25
Std Dev	1.299





# B1L003S, U26-ch47, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	63
Std Dev	0

# B1L003S, U26-ch48, adc0

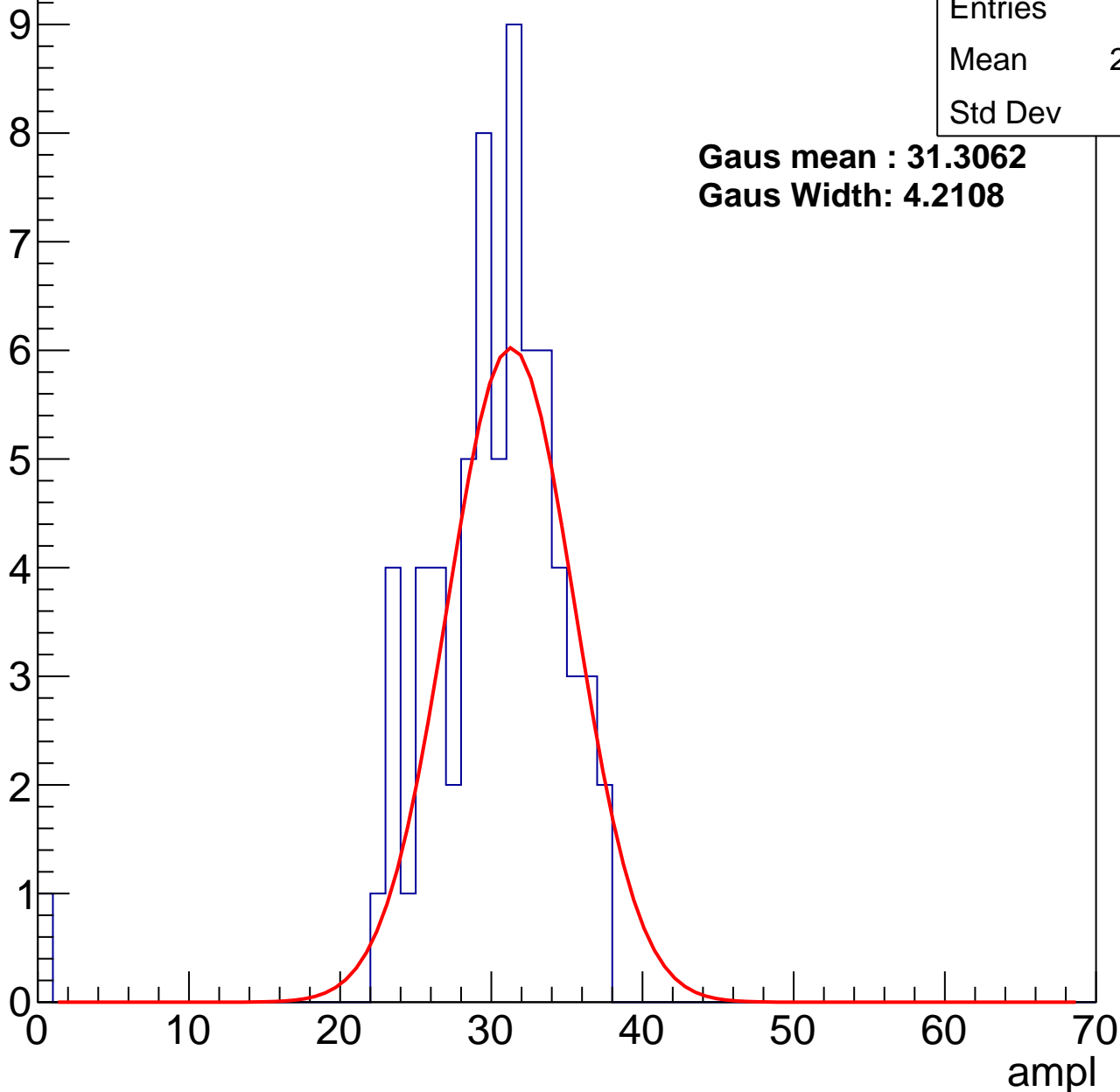
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	29.56
Std Dev	5.18

**Gaus mean : 31.3062**

**Gaus Width: 4.2108**



# B1L003S, U26-ch48, adc1

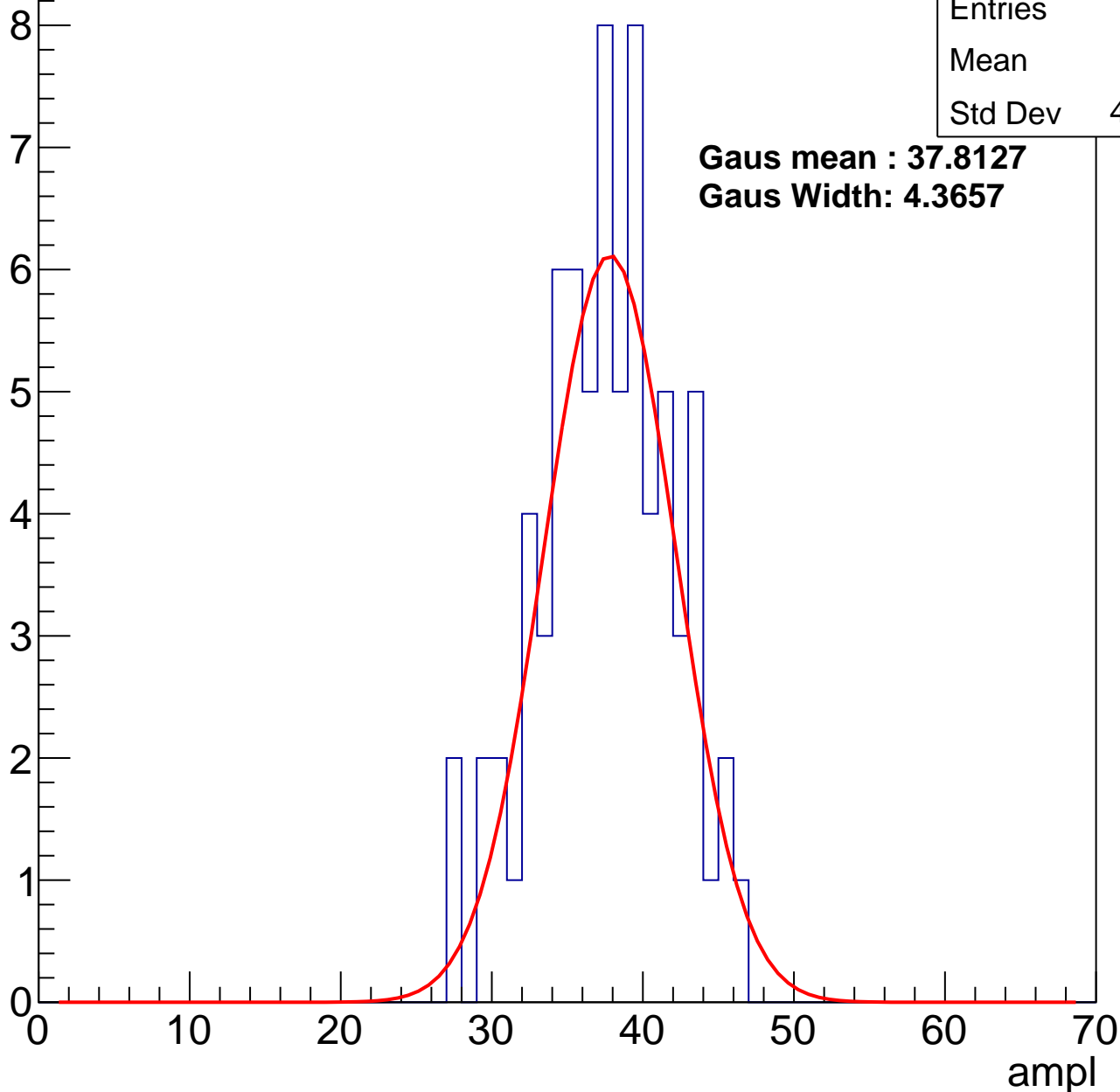
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	73
Mean	37.1
Std Dev	4.314

**Gaus mean : 37.8127**

**Gaus Width: 4.3657**



# B1L003S, U26-ch48, adc2

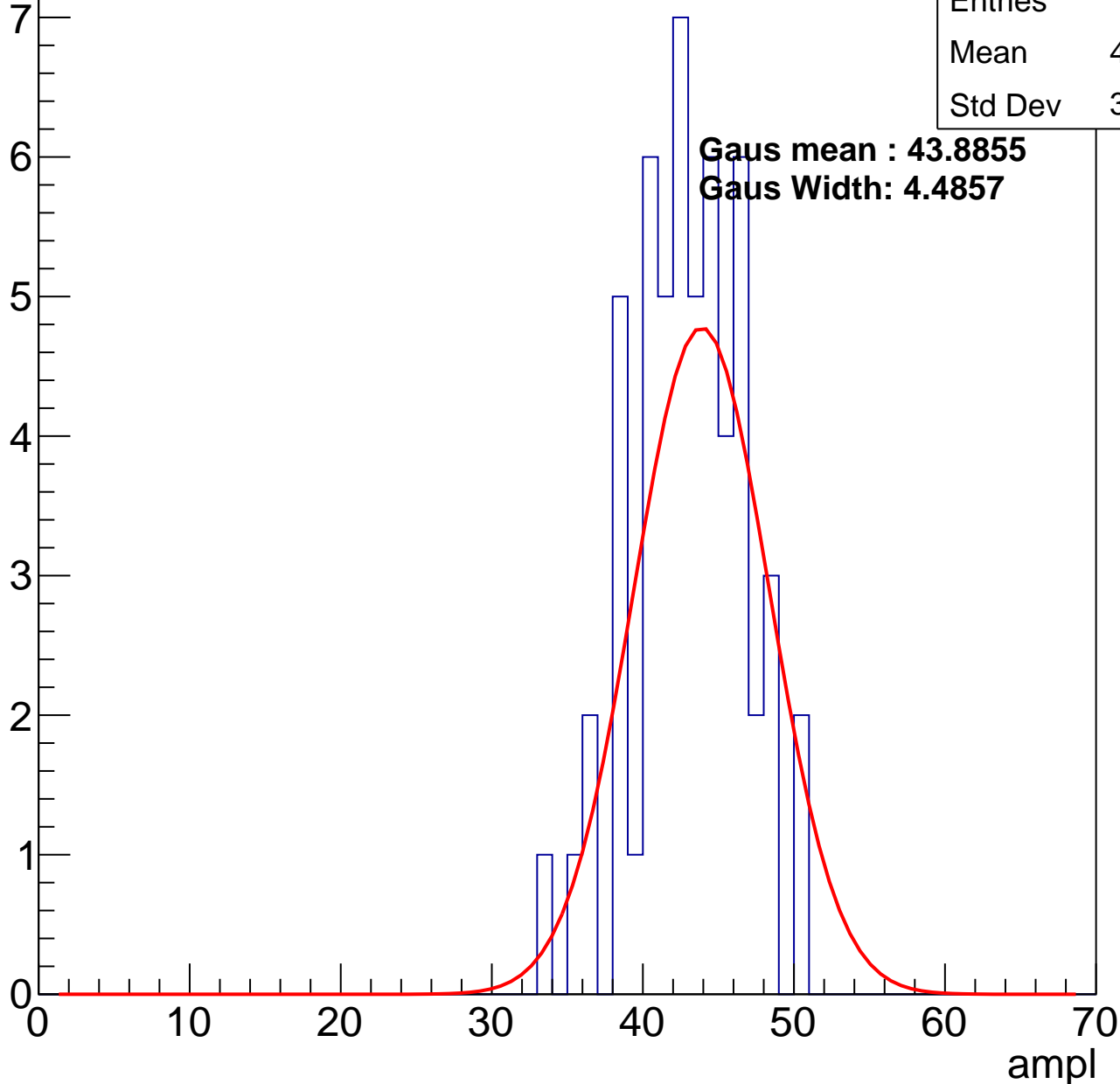
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	42.52
Std Dev	3.664

**Gaus mean : 43.8855**

**Gaus Width: 4.4857**

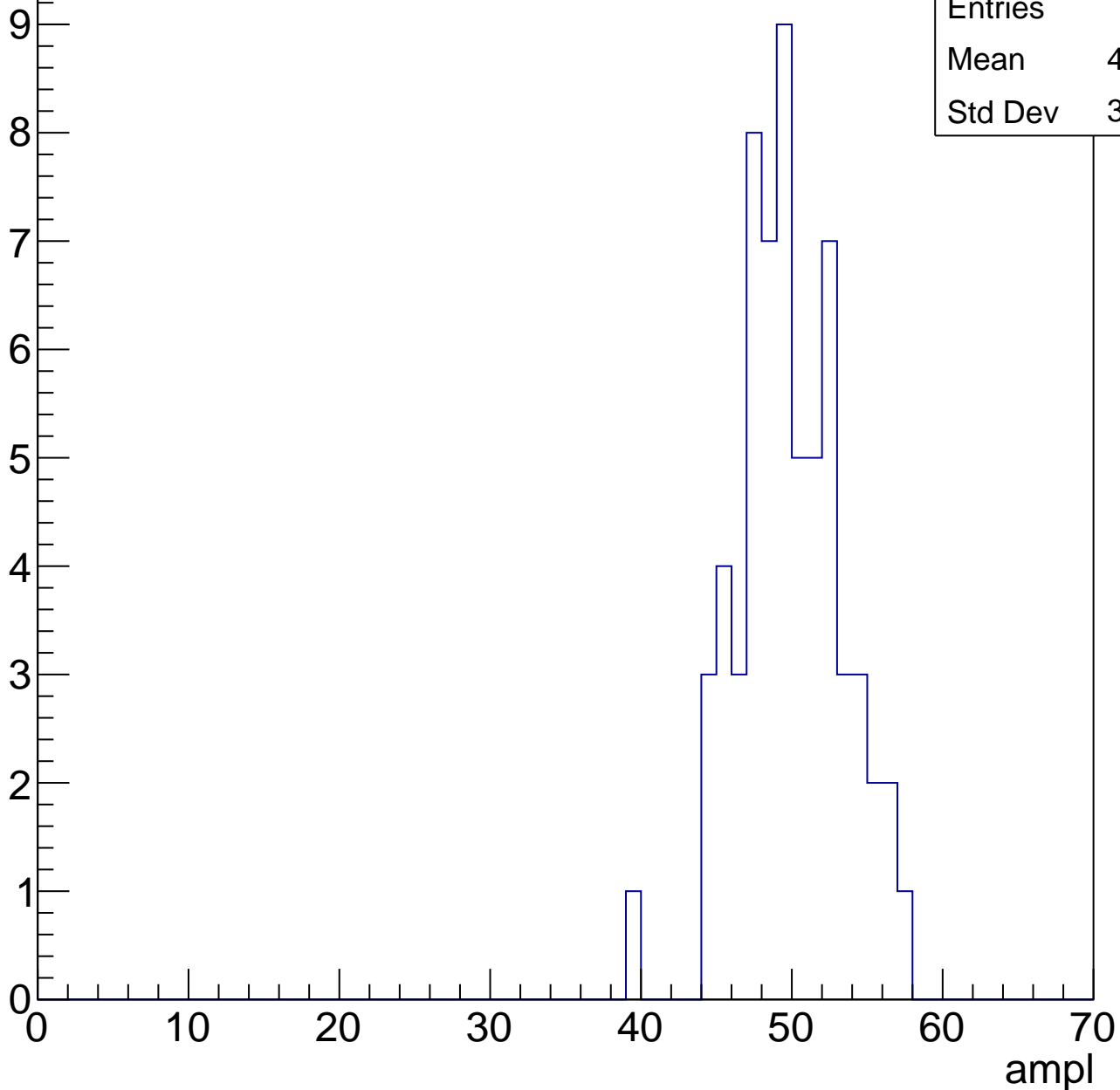


# B1L003S, U26-ch48, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	49.38
Std Dev	3.429

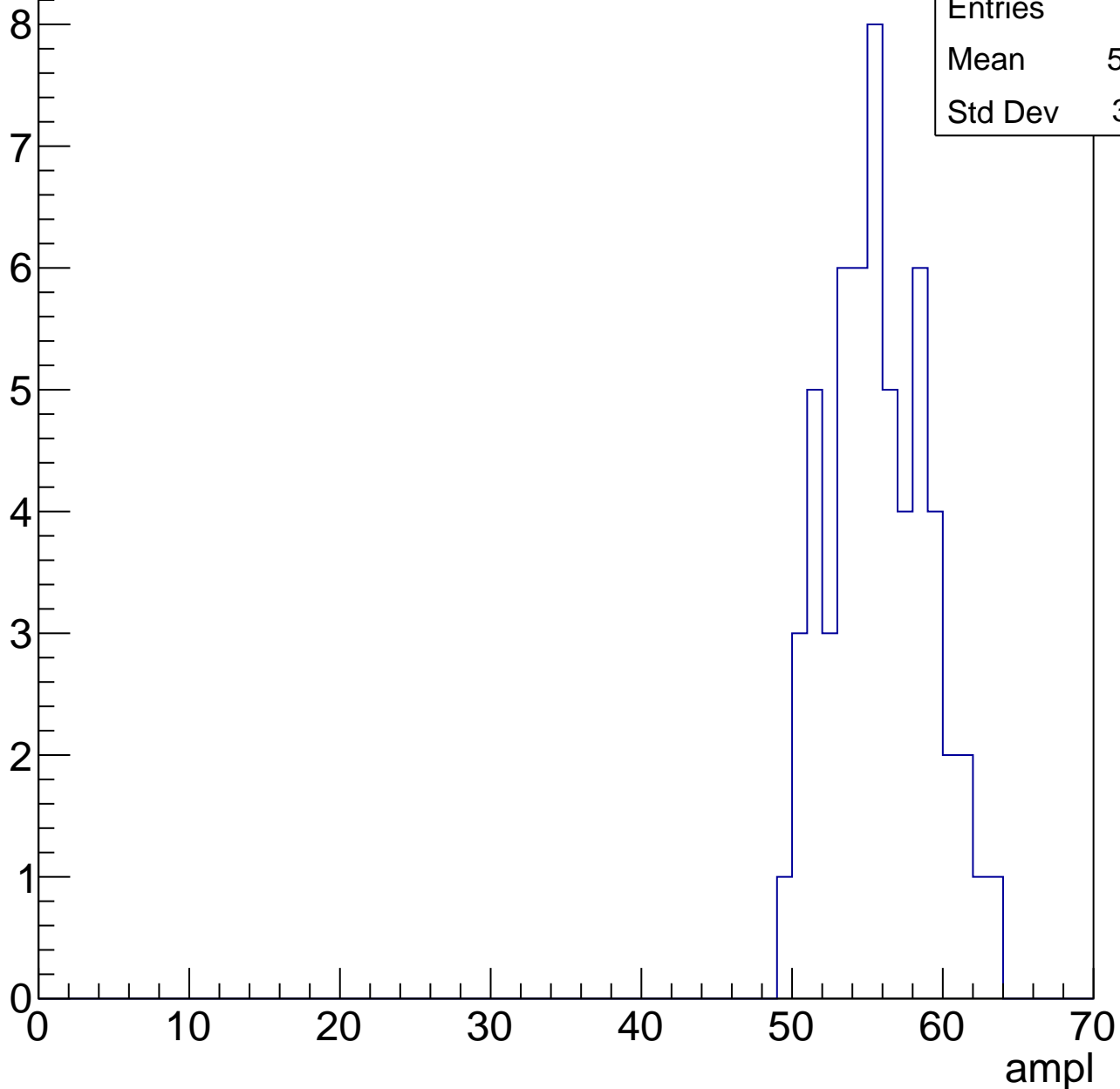


# B1L003S, U26-ch48, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	55.28
Std Dev	3.291

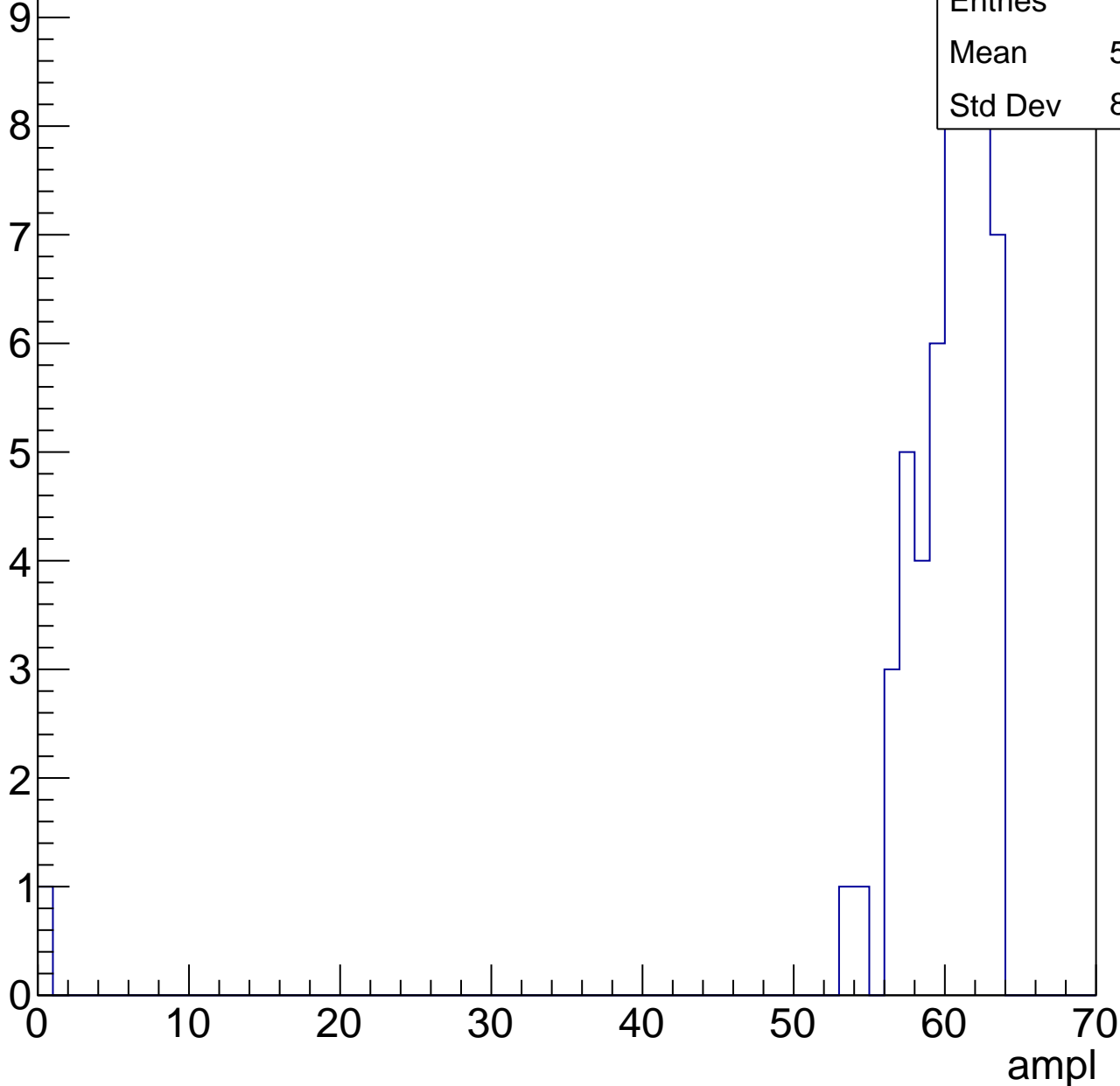


# B1L003S, U26-ch48, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	58.74
Std Dev	8.492



# B1L003S, U26-ch48, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch48, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U26-ch49, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	92
Mean	28.33
Std Dev	4.137

**Gaus mean : 29.0760**

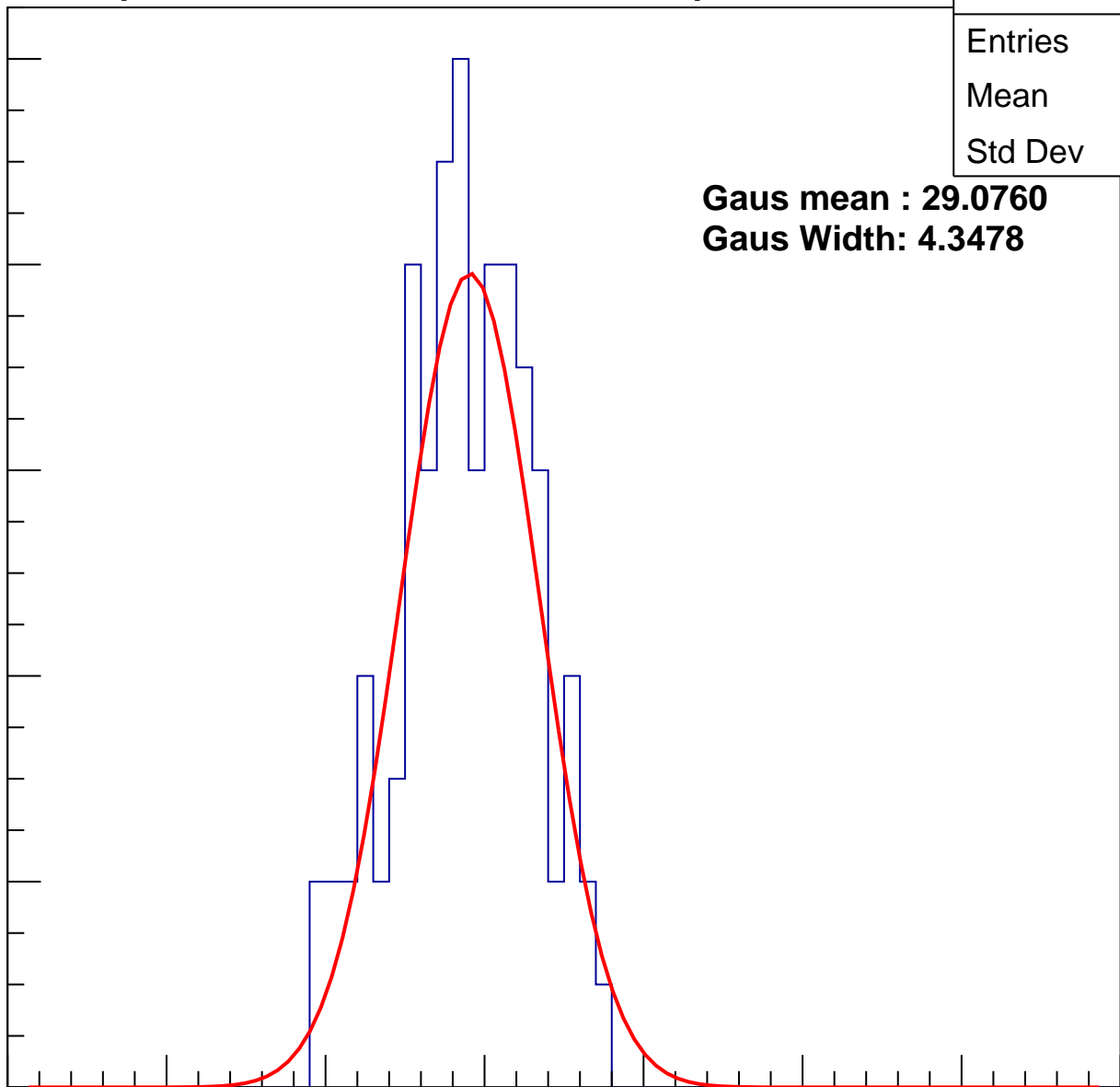
**Gaus Width: 4.3478**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U26-ch49, adc1

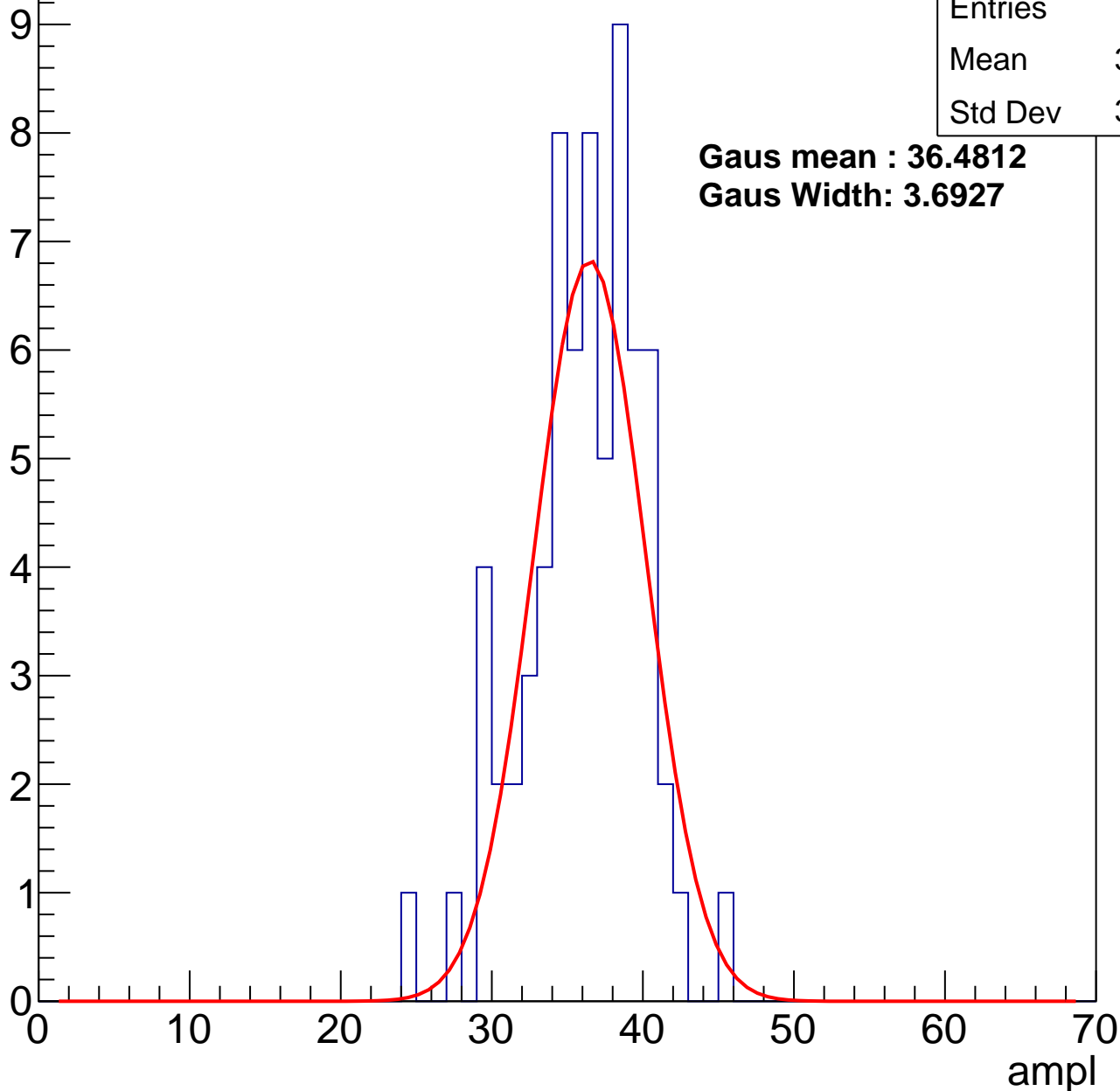
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	35.61
Std Dev	3.831

**Gaus mean : 36.4812**

**Gaus Width: 3.6927**



# B1L003S, U26-ch49, adc2

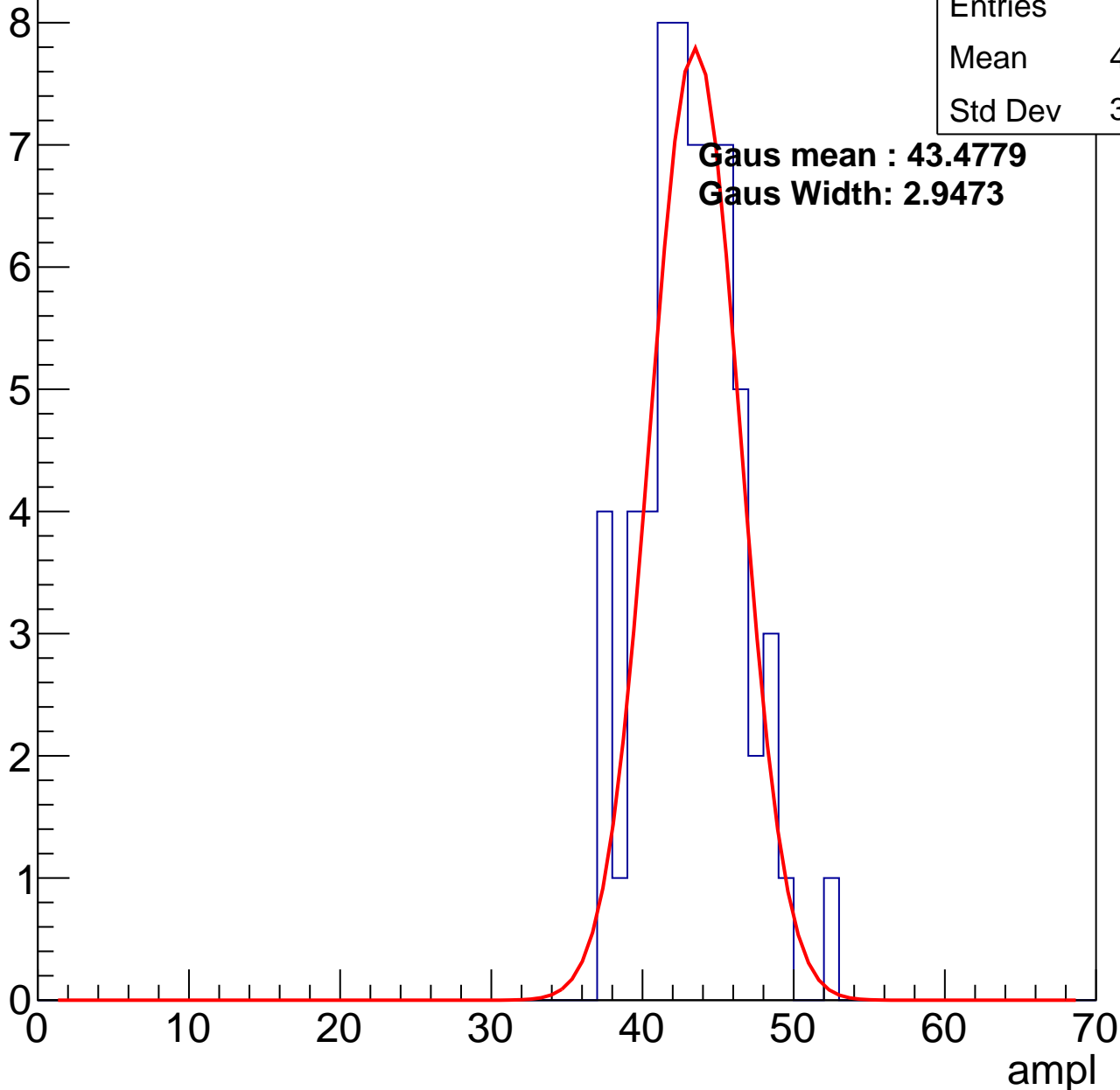
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	42.89
Std Dev	3.142

**Gaus mean : 43.4779**

**Gaus Width: 2.9473**

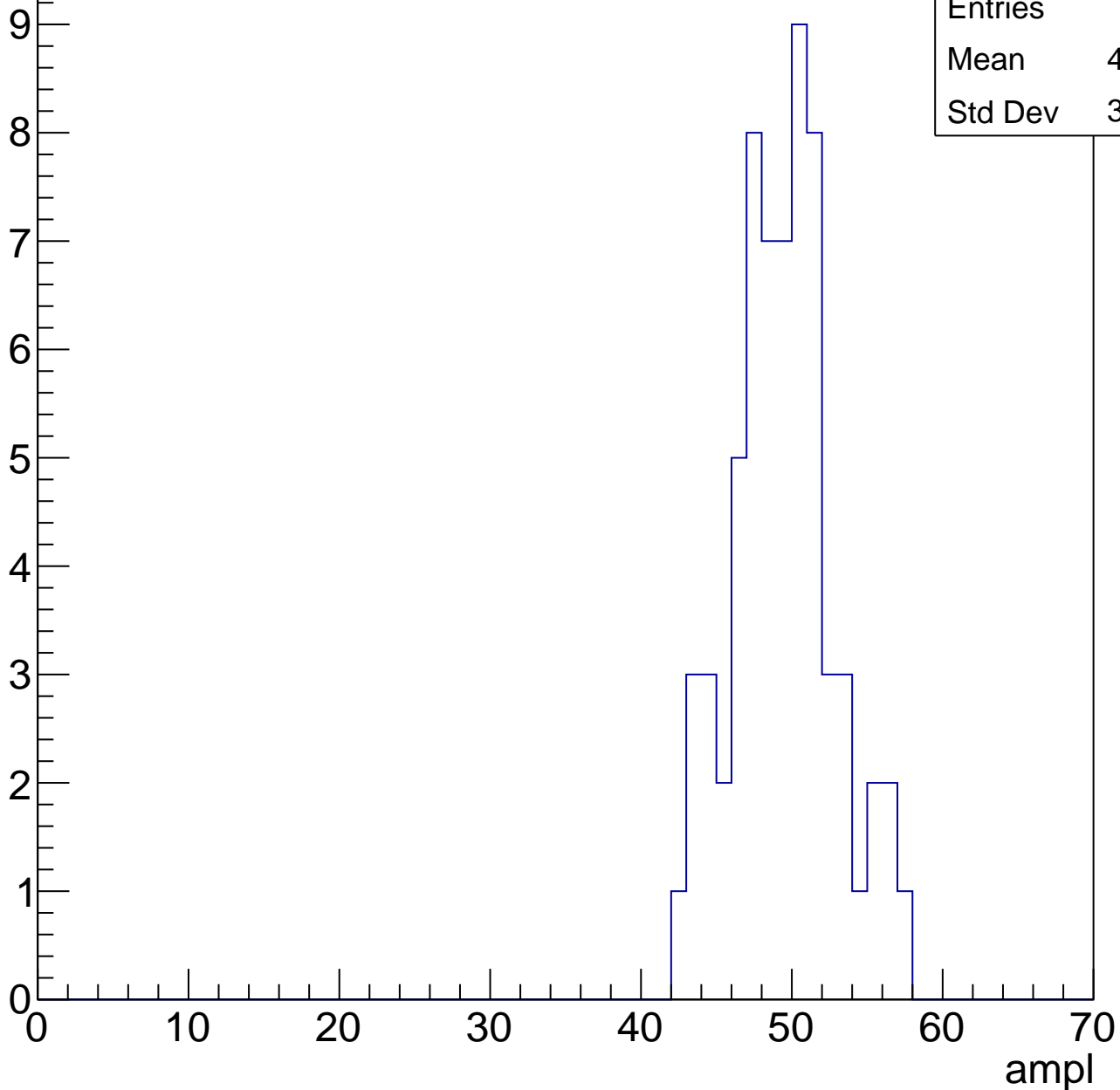


# B1L003S, U26-ch49, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	48.98
Std Dev	3.335

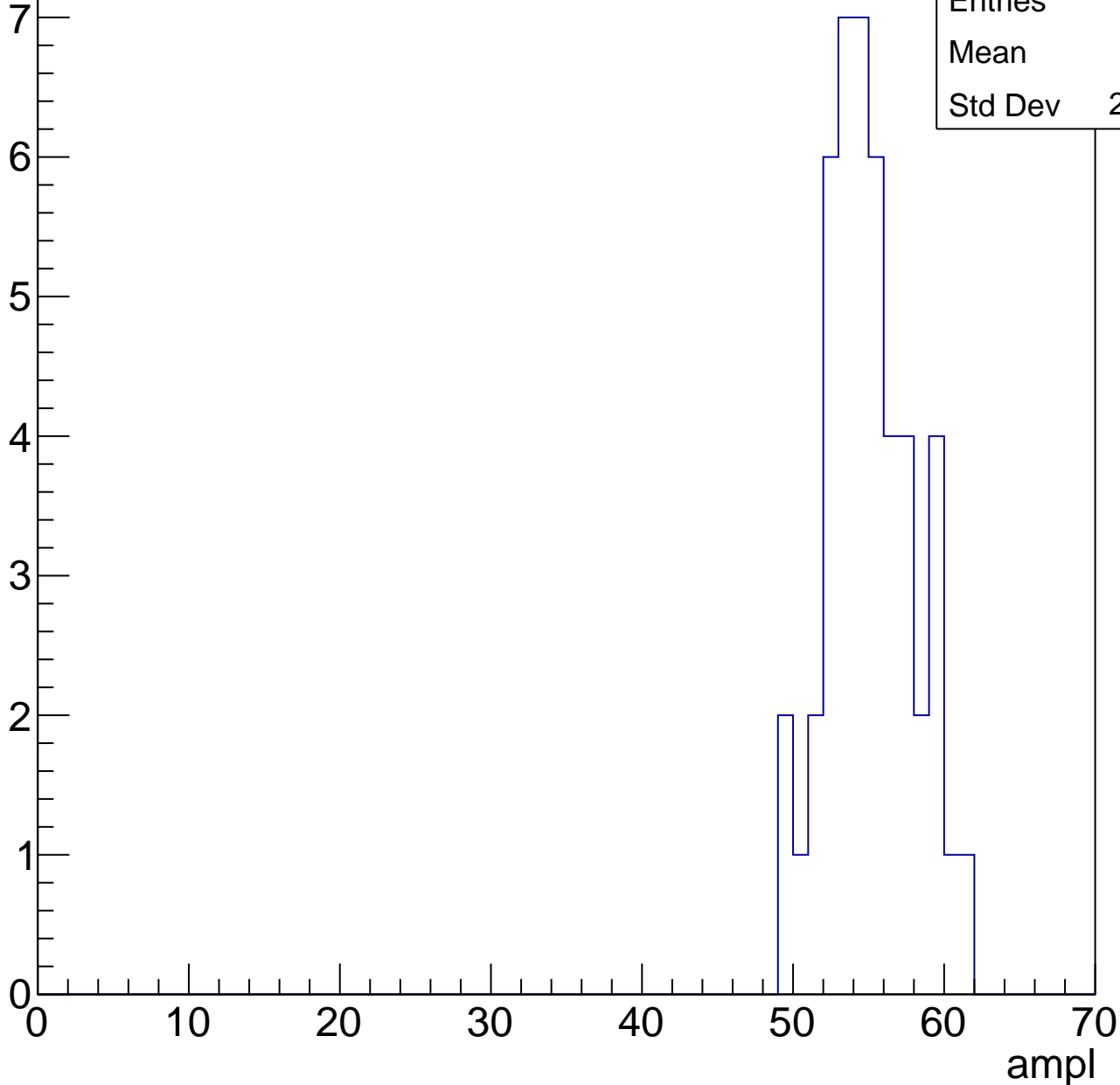


# B1L003S, U26-ch49, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	47
Mean	54.6
Std Dev	2.818



# B1L003S, U26-ch49, adc5

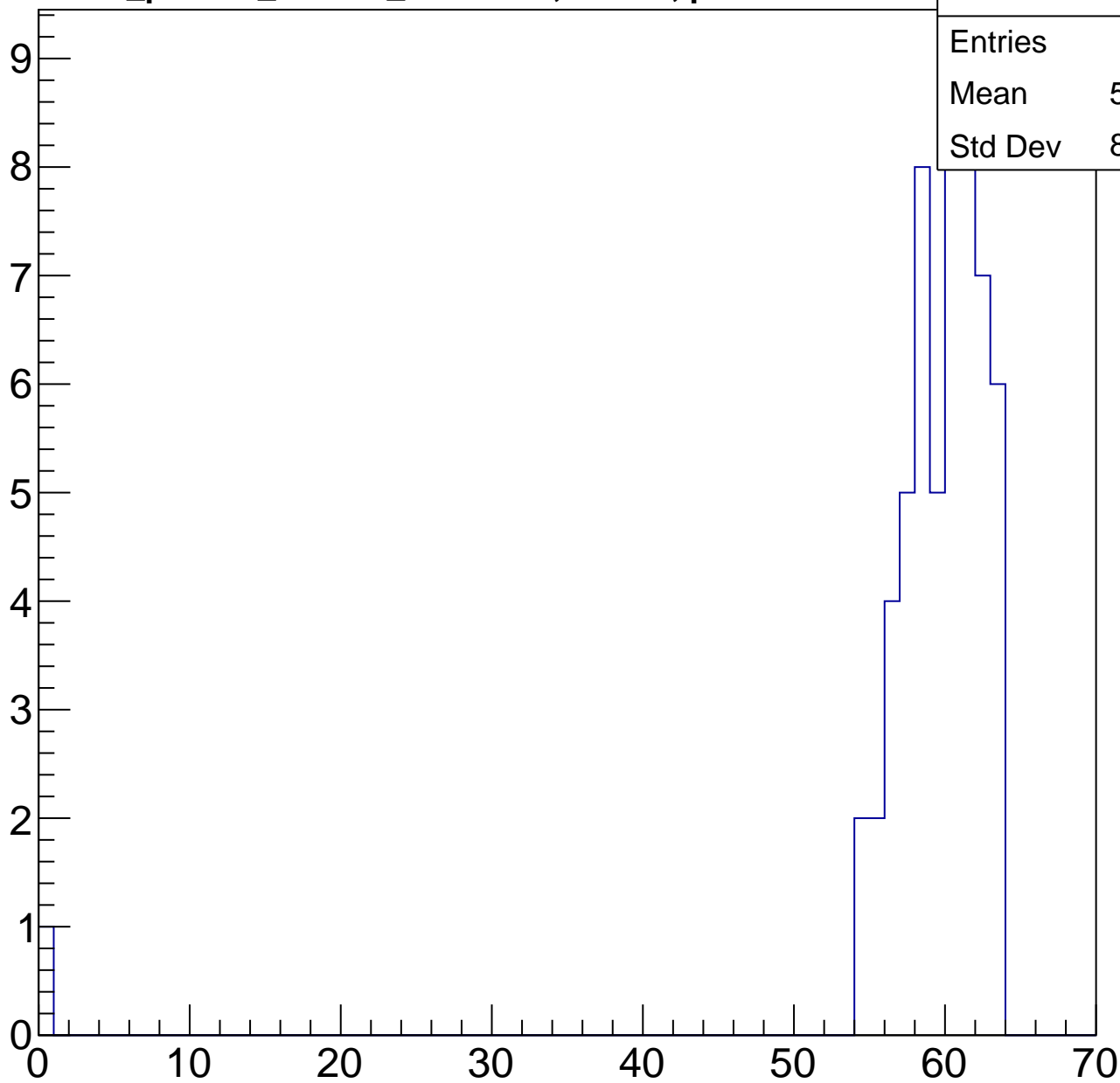
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	57
Mean	58.37
Std Dev	8.173

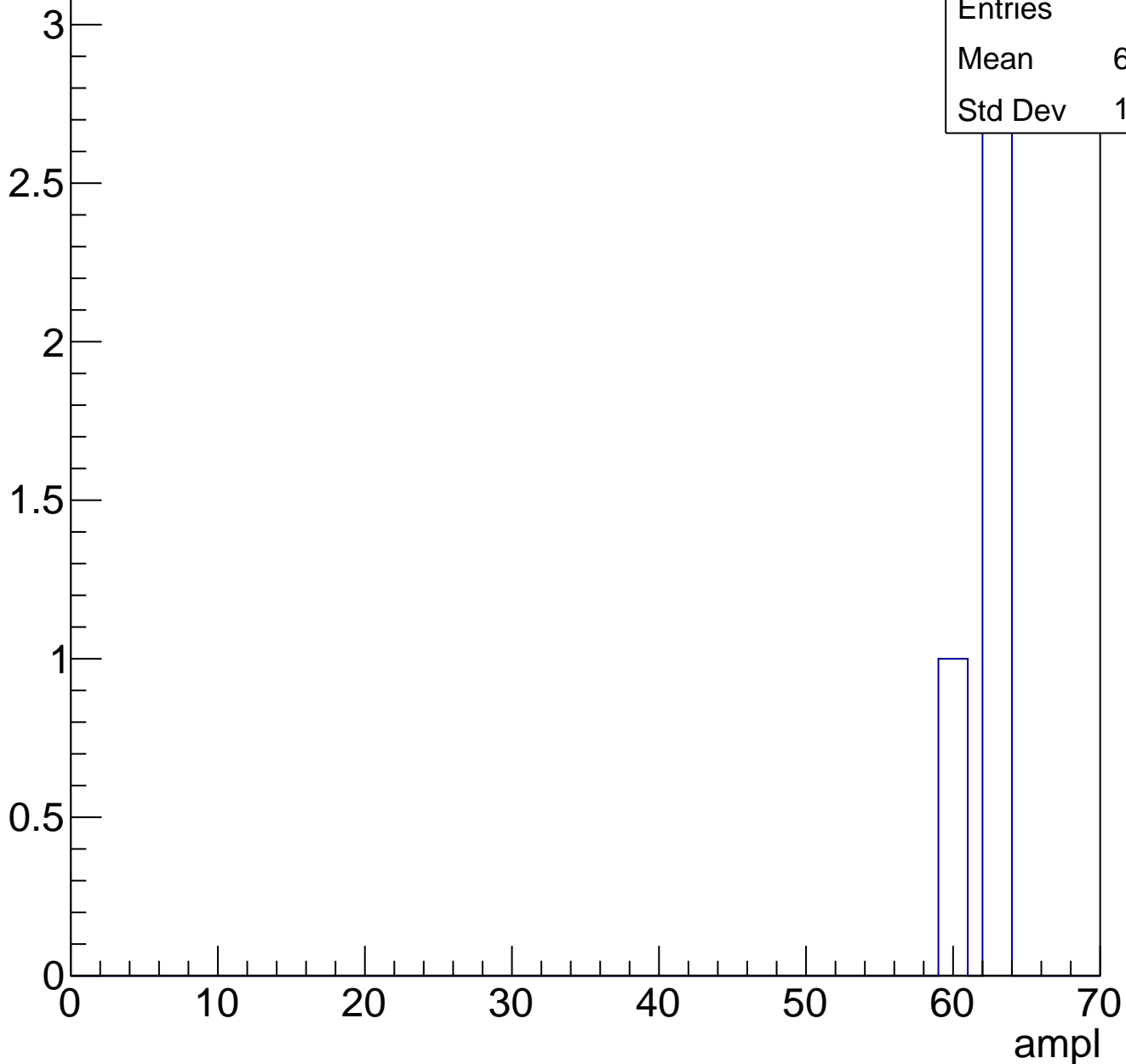
ampl



# B1L003S, U26-ch49, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch49, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U26-ch50, adc0

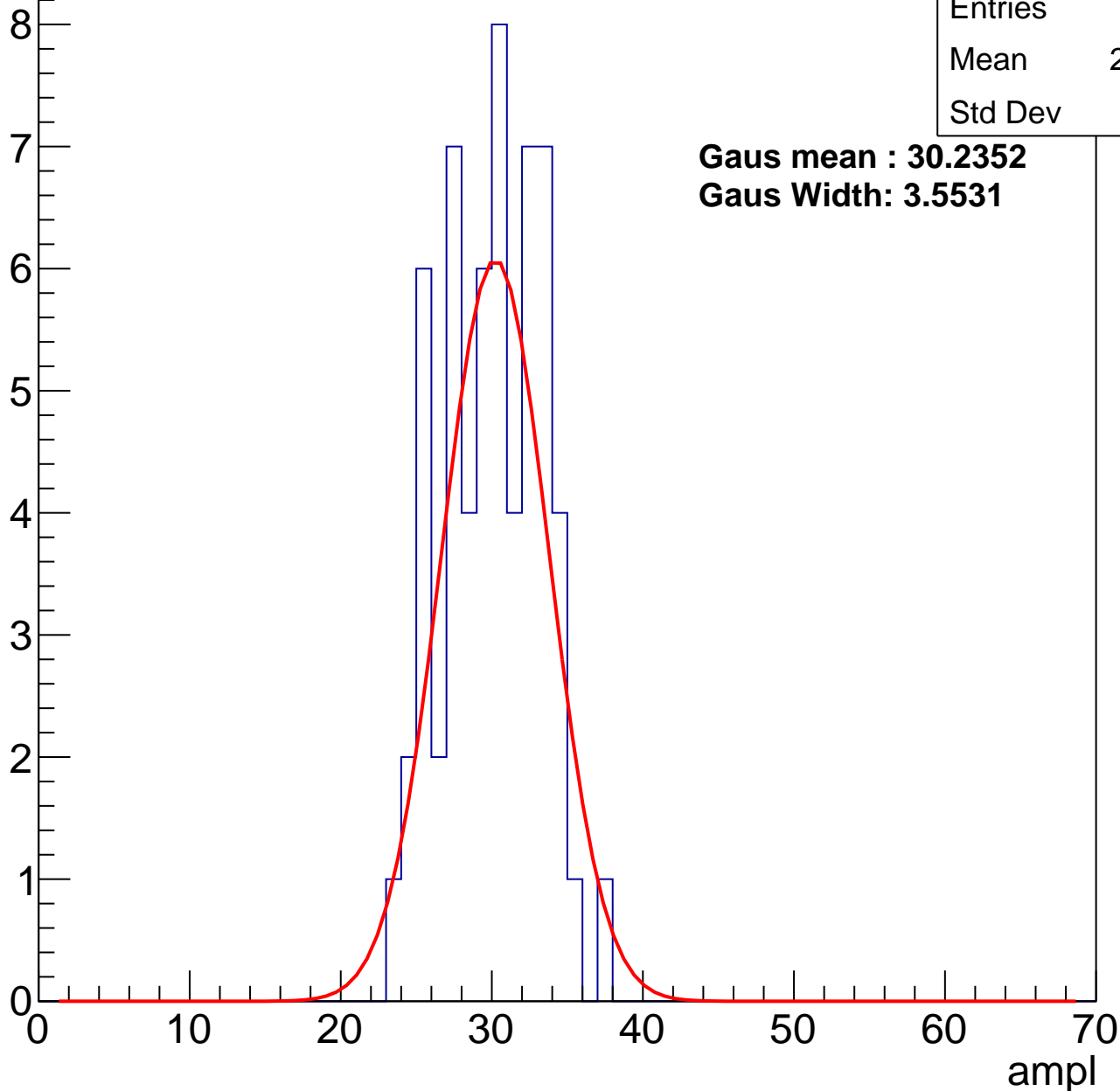
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	29.58
Std Dev	3.19

**Gaus mean : 30.2352**

**Gaus Width: 3.5531**



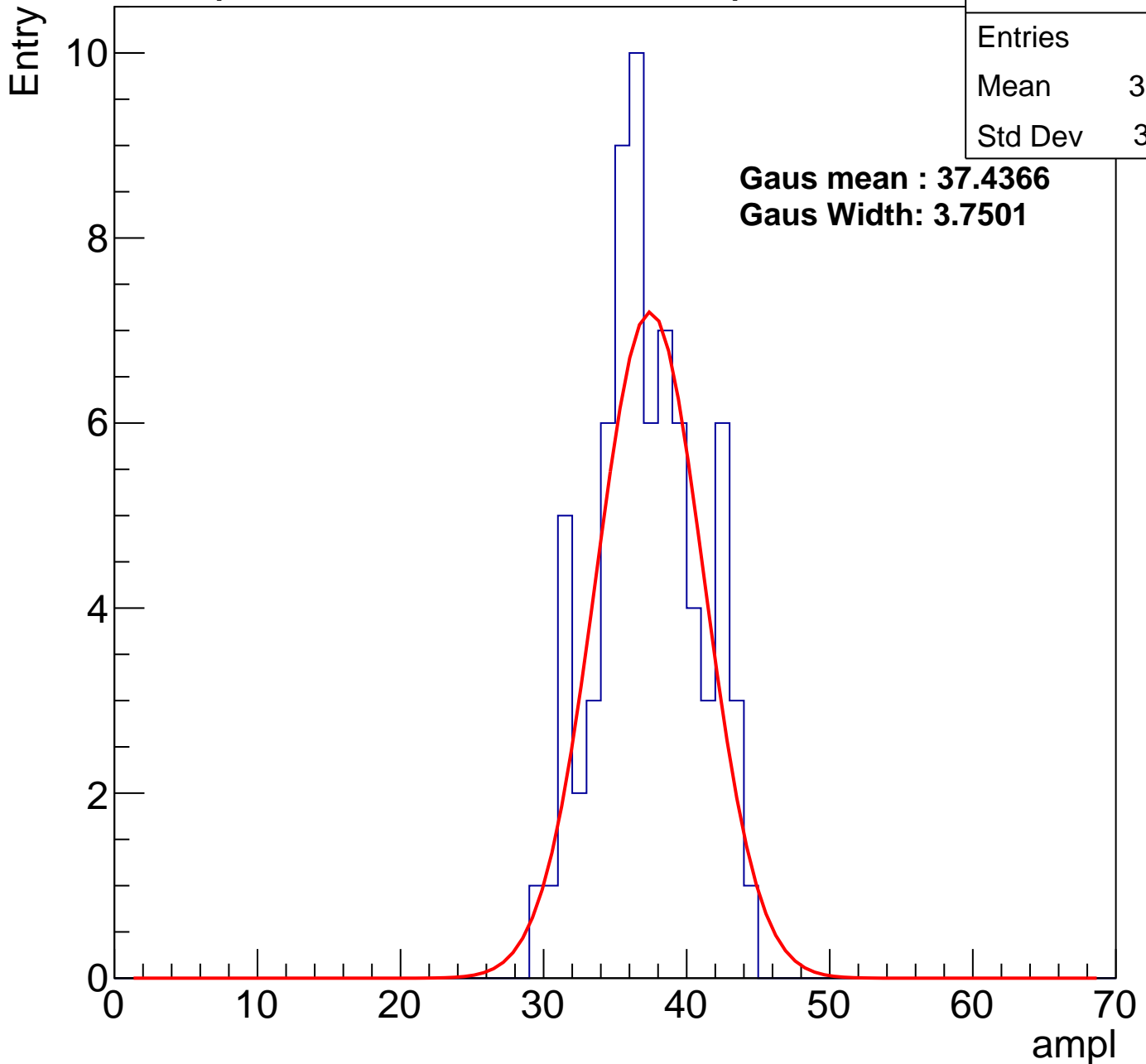
# B1L003S, U26-ch50, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	73
Mean	36.79
Std Dev	3.531

**Gaus mean : 37.4366**

**Gaus Width: 3.7501**



# B1L003S, U26-ch50, adc2

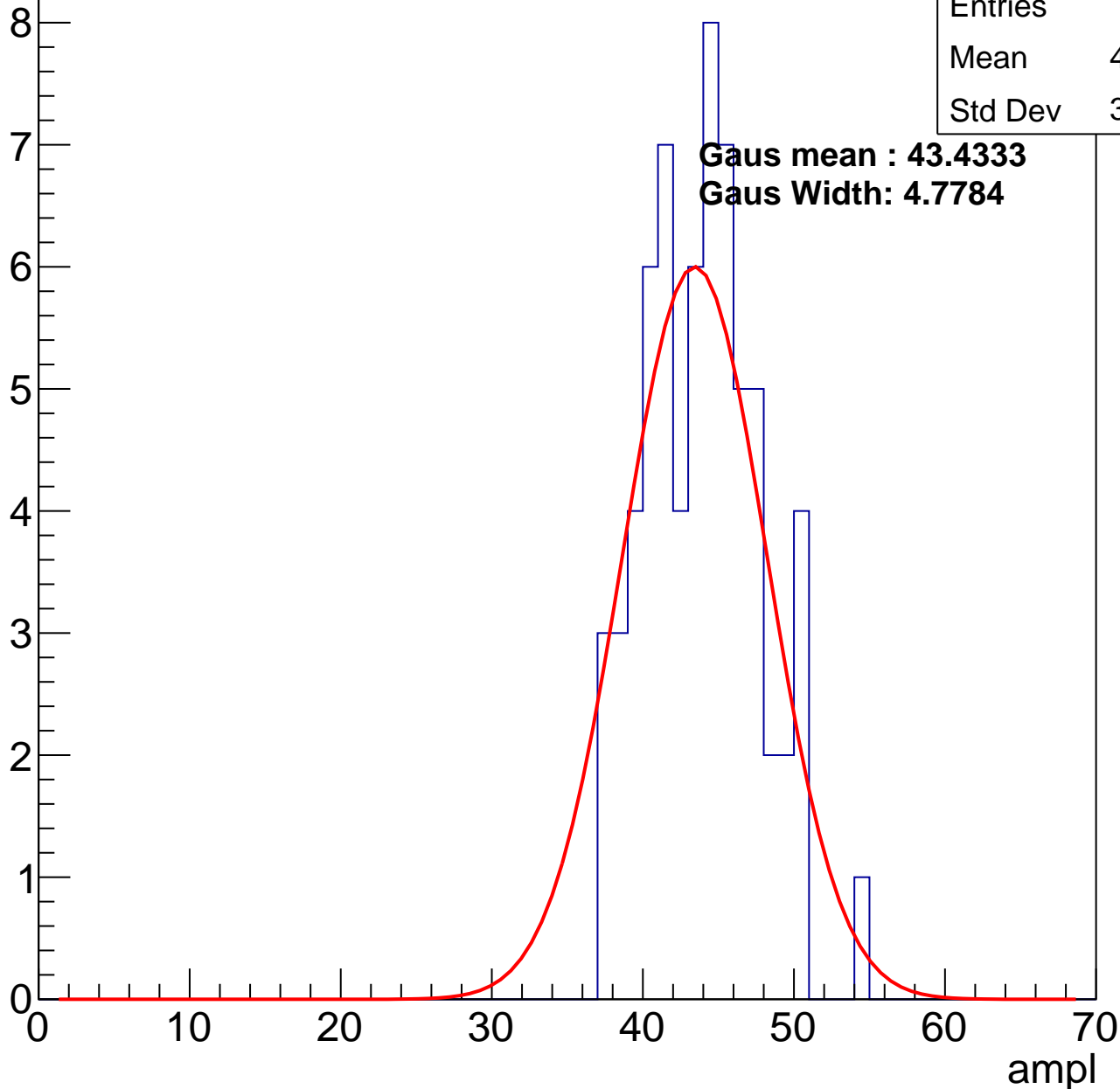
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	43.49
Std Dev	3.699

**Gaus mean : 43.4333**

**Gaus Width: 4.7784**

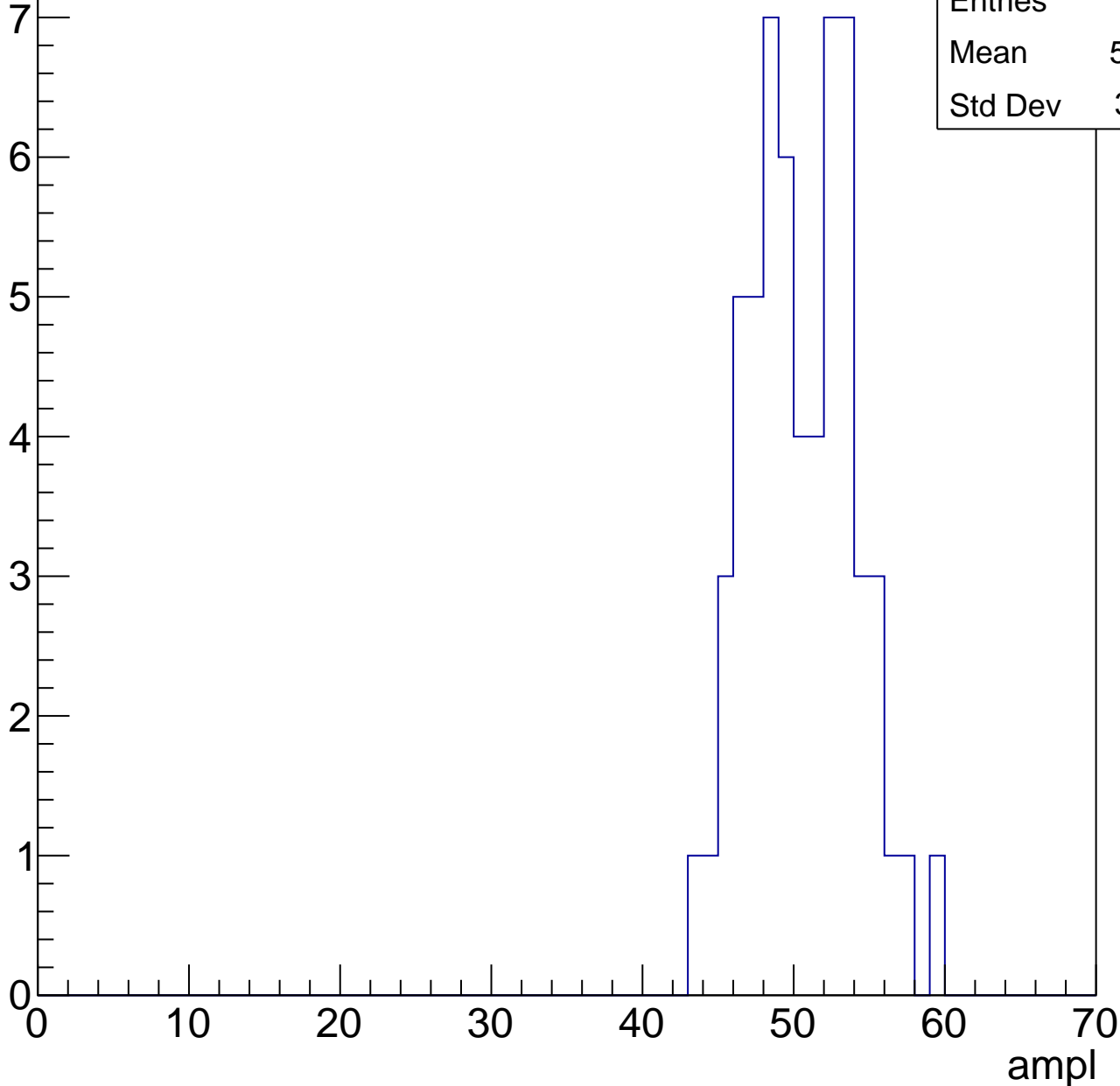


# B1L003S, U26-ch50, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	50.08
Std Dev	3.451

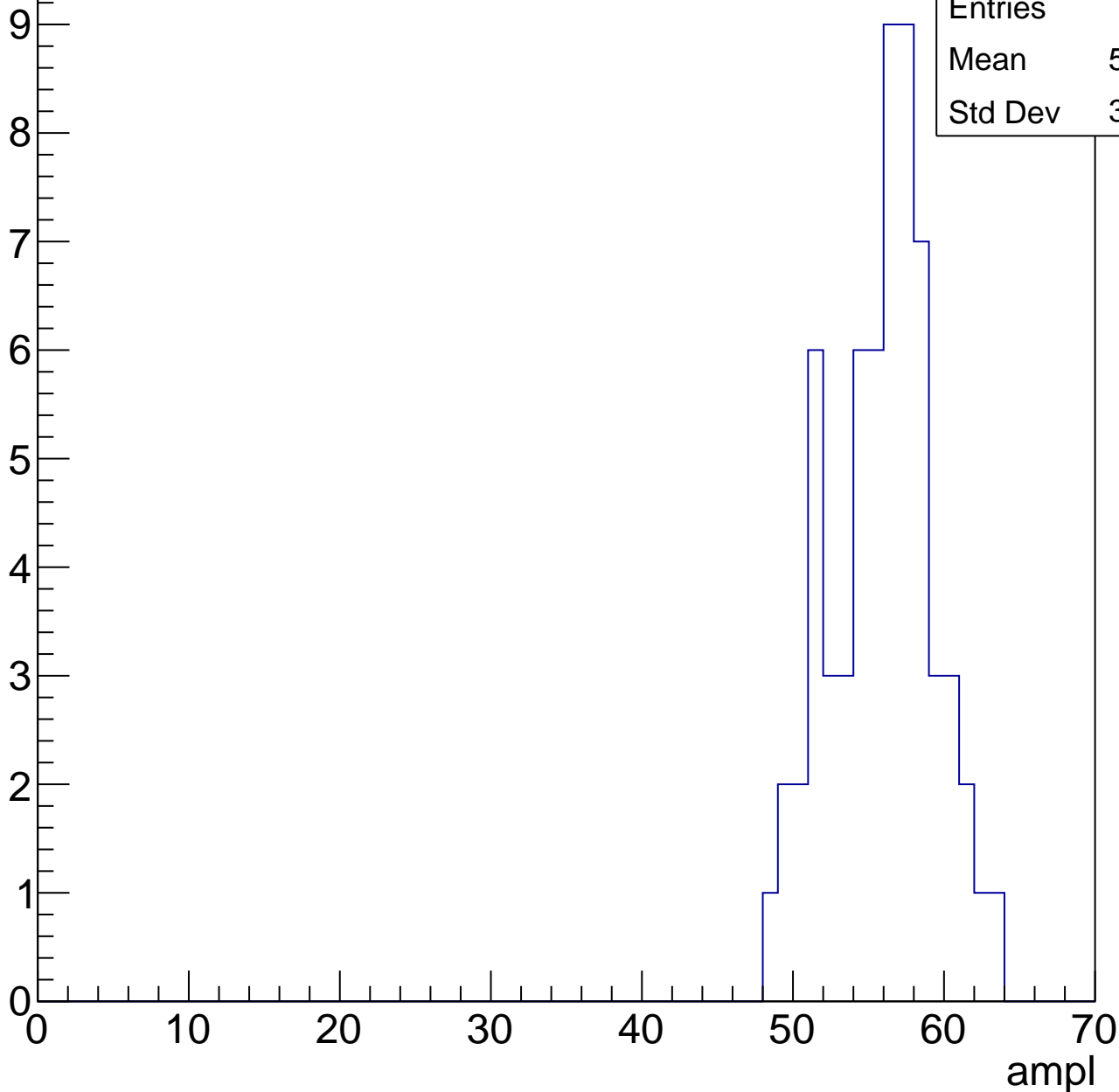


# B1L003S, U26-ch50, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	55.44
Std Dev	3.344

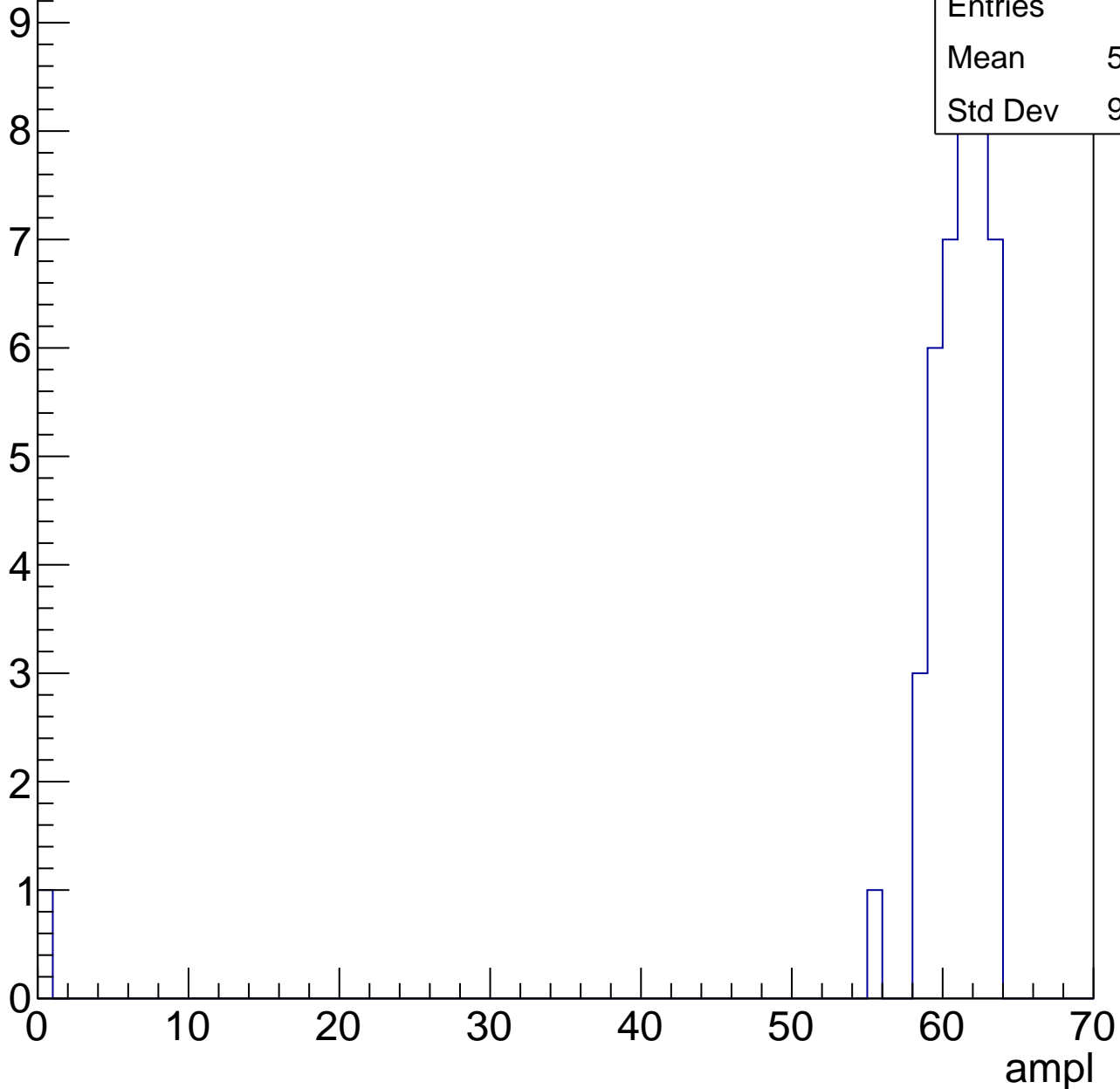


# B1L003S, U26-ch50, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	42
Mean	59.29
Std Dev	9.422



# B1L003S, U26-ch50, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	63
Std Dev	0

0 10 20 30 40 50 60 70

ampl



# B1L003S, U26-ch50, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L003S, U26-ch51, adc0

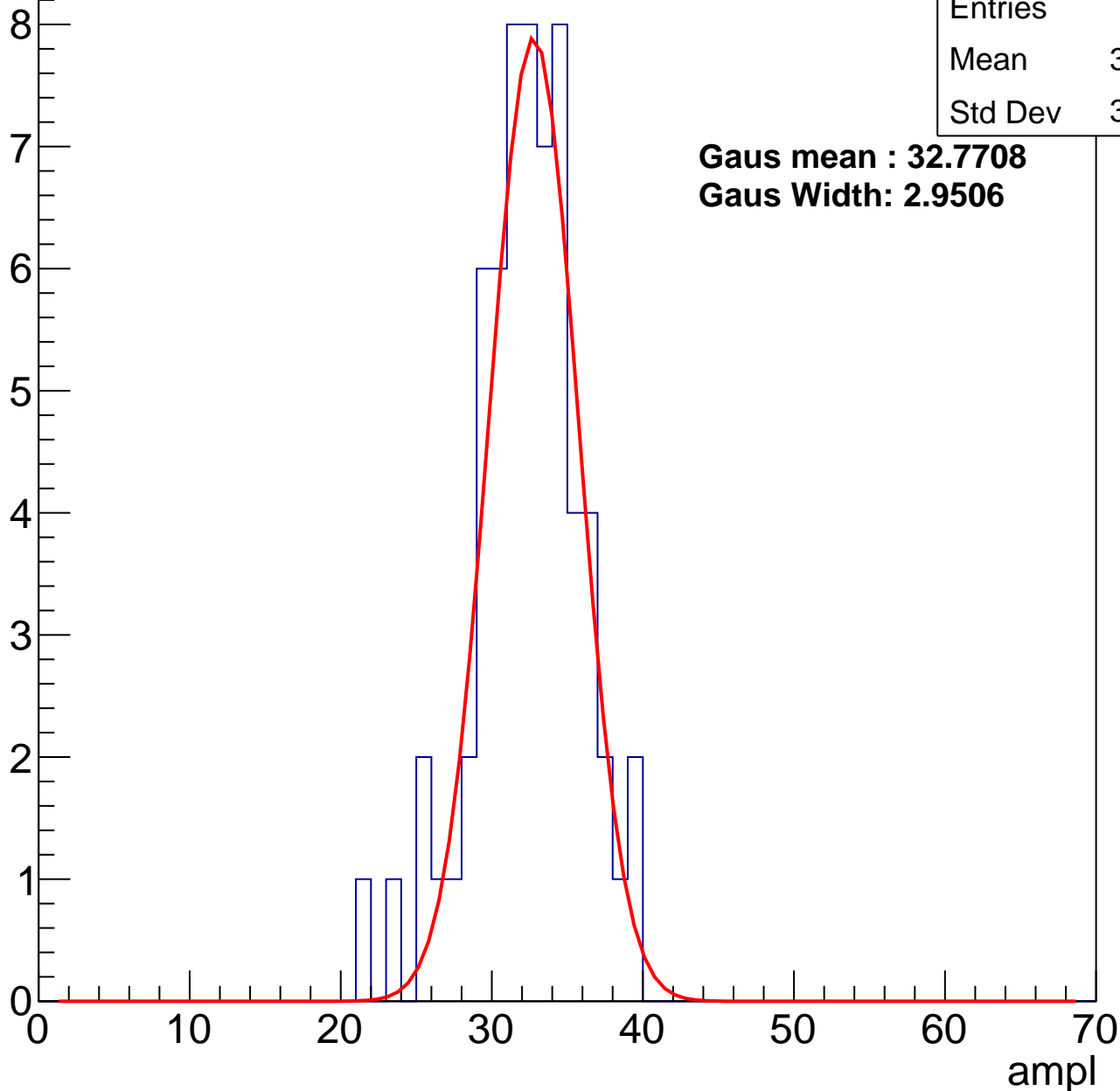
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	31.84
Std Dev	3.537

**Gaus mean : 32.7708**

**Gaus Width: 2.9506**



# B1L003S, U26-ch51, adc1

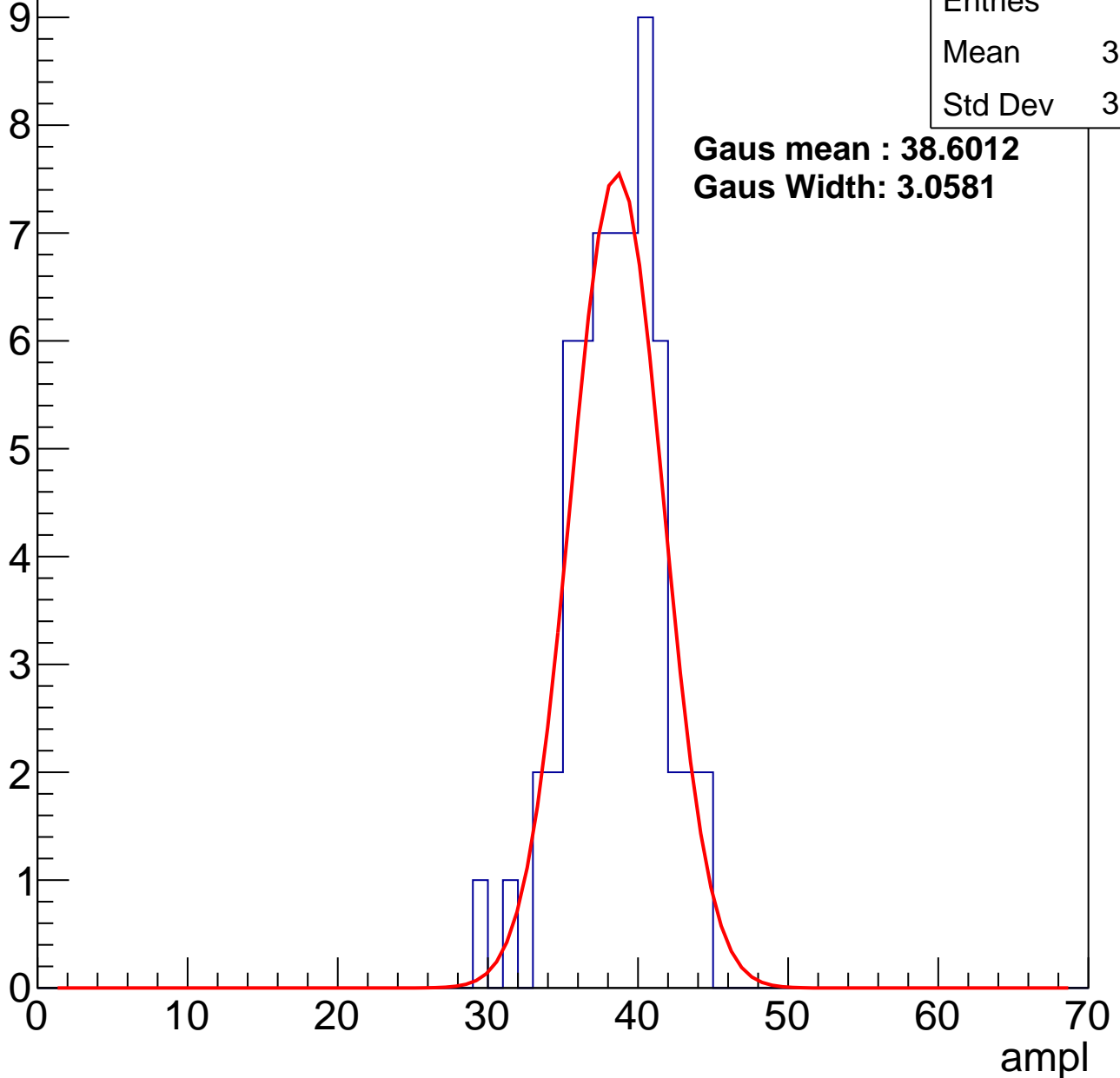
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	38.03
Std Dev	3.022

**Gaus mean : 38.6012**

**Gaus Width: 3.0581**



# B1L003S, U26-ch51, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	65
Mean	44.51
Std Dev	3.079

**Gaus mean : 44.7593**

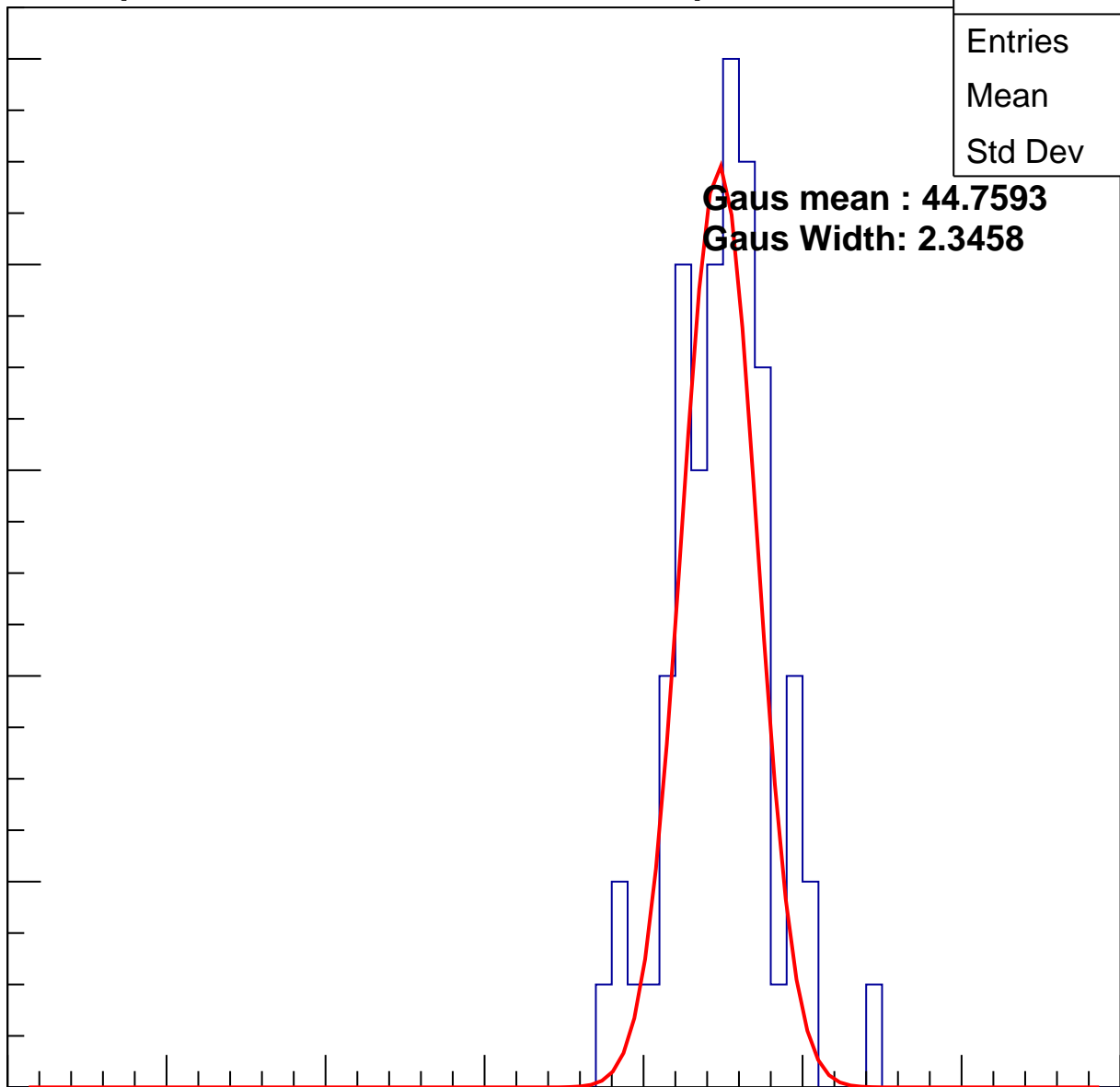
**Gaus Width: 2.3458**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

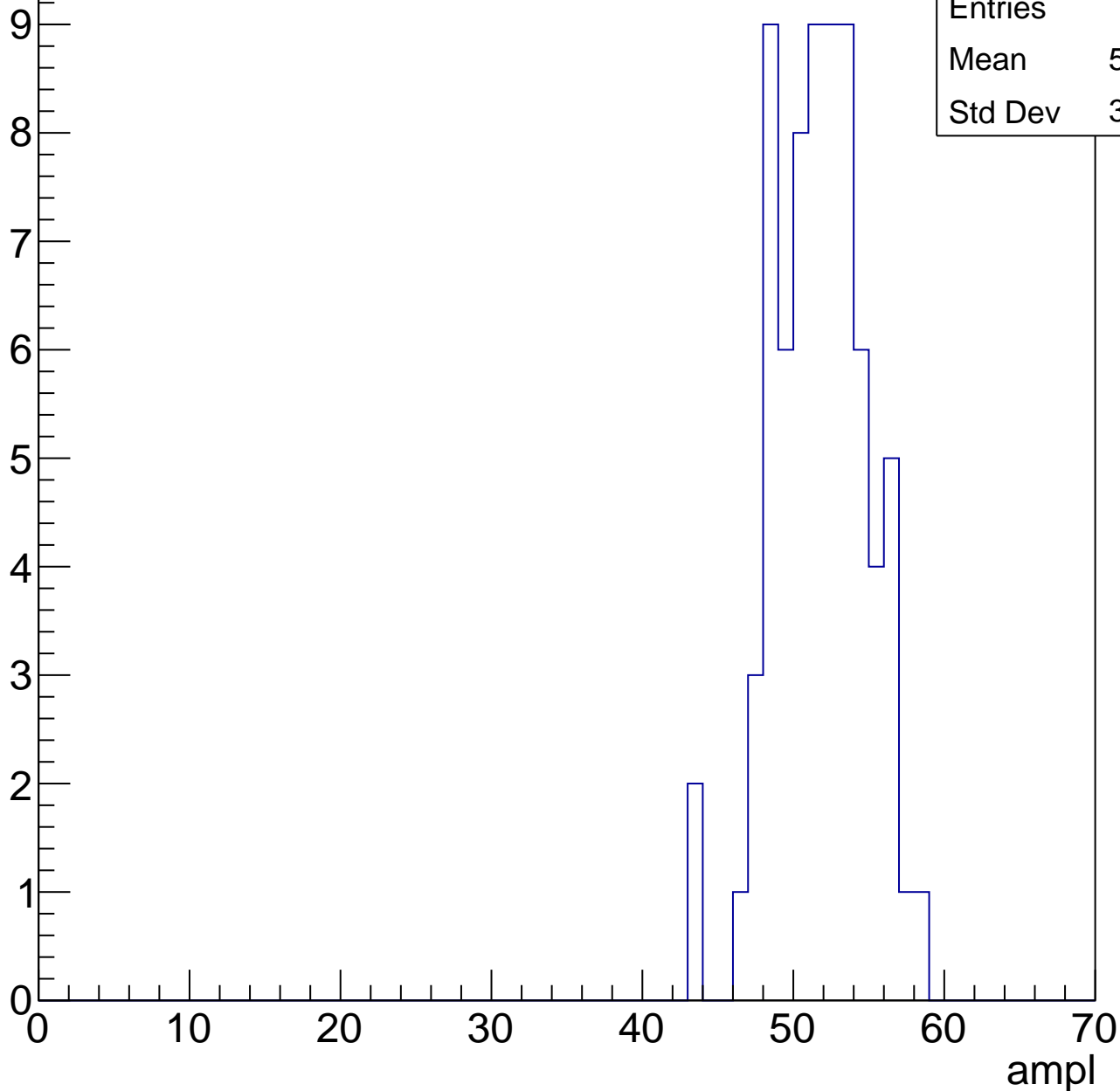


# B1L003S, U26-ch51, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	73
Mean	51.26
Std Dev	3.057

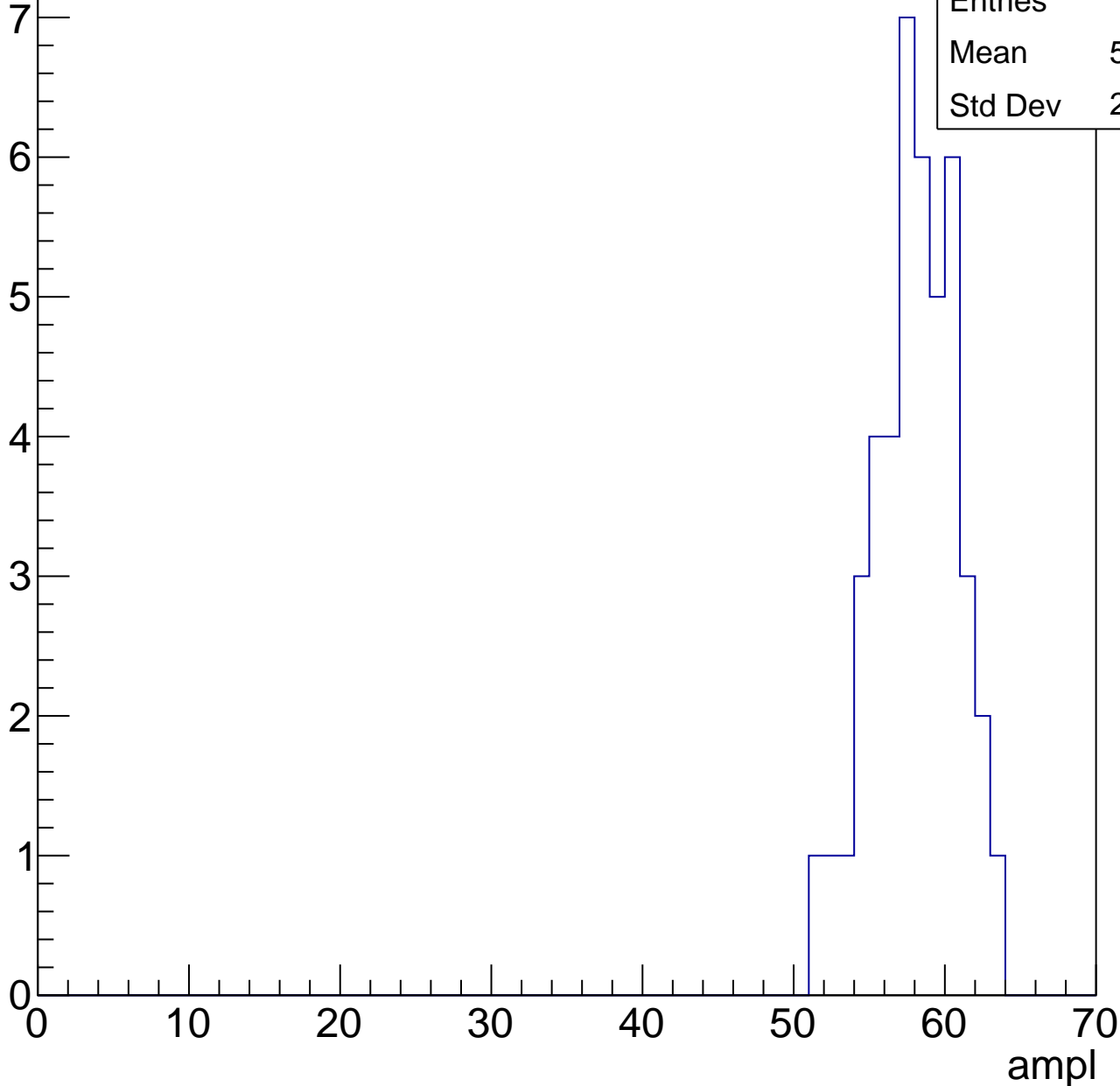


# B1L003S, U26-ch51, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	44
Mean	57.59
Std Dev	2.708

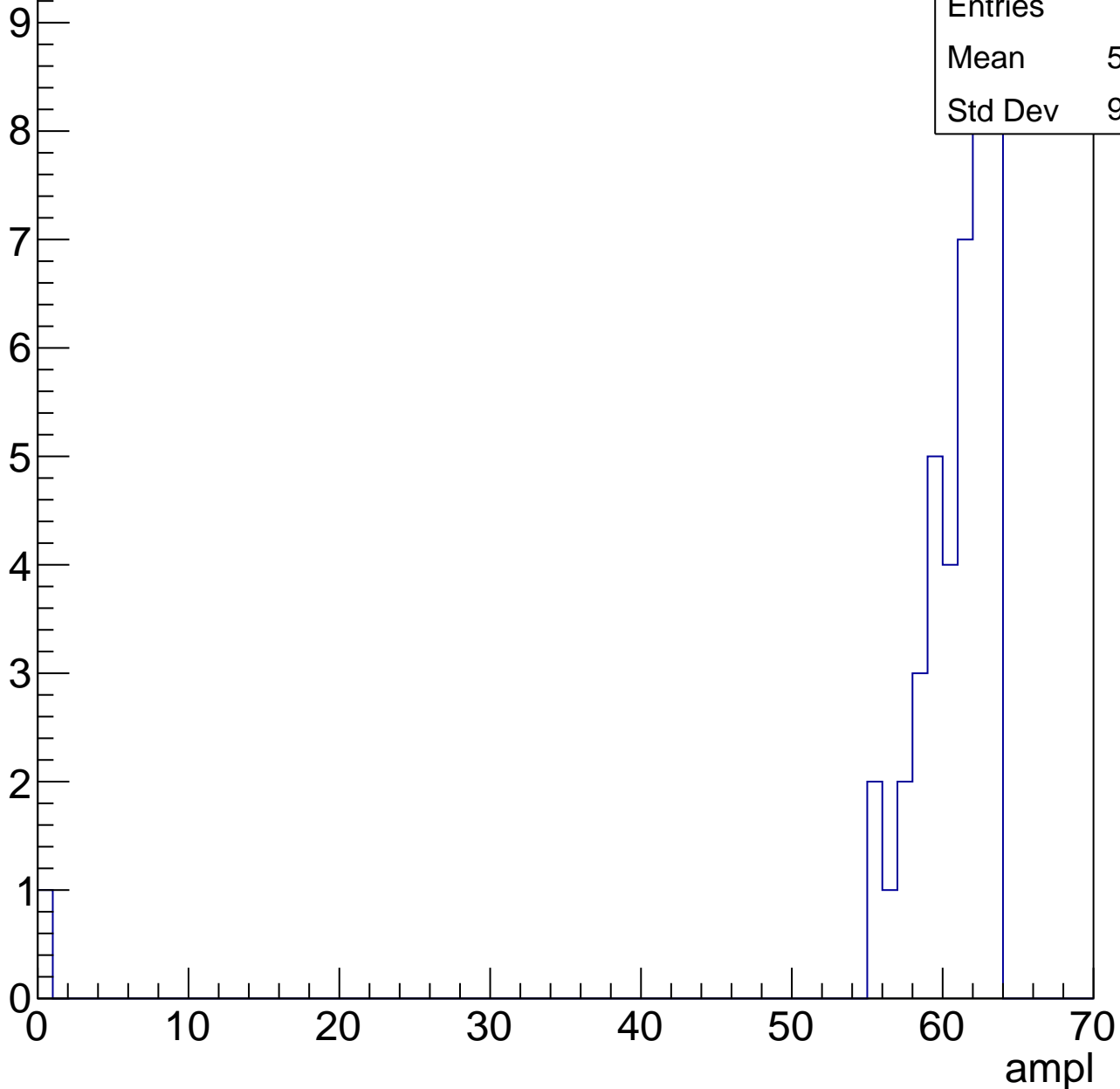


# B1L003S, U26-ch51, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	42
Mean	59.02
Std Dev	9.488



# B1L003S, U26-ch51, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L003S, U26-ch51, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U26-ch52, adc0

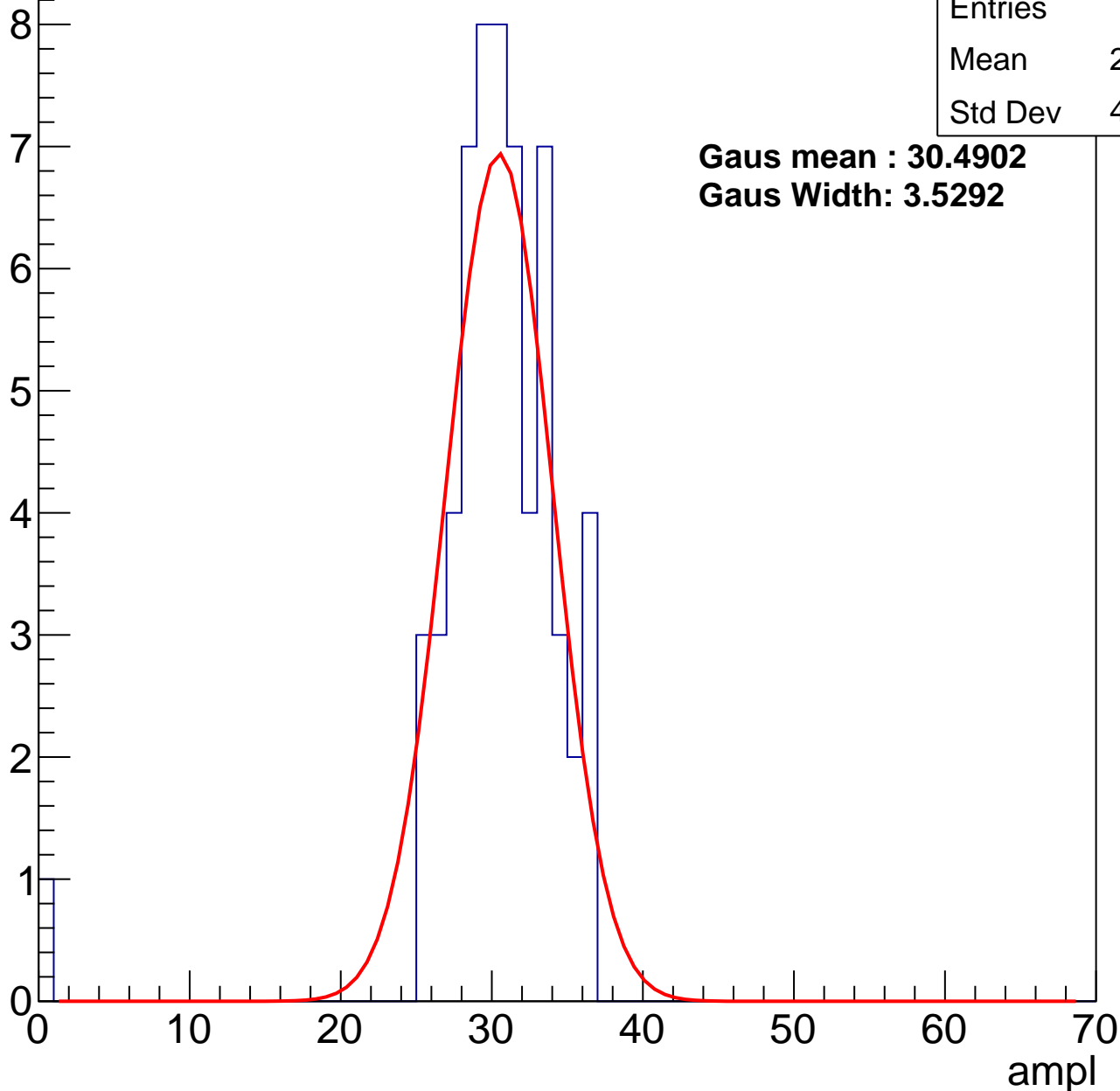
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	29.85
Std Dev	4.828

**Gaus mean : 30.4902**

**Gaus Width: 3.5292**



# B1L003S, U26-ch52, adc1

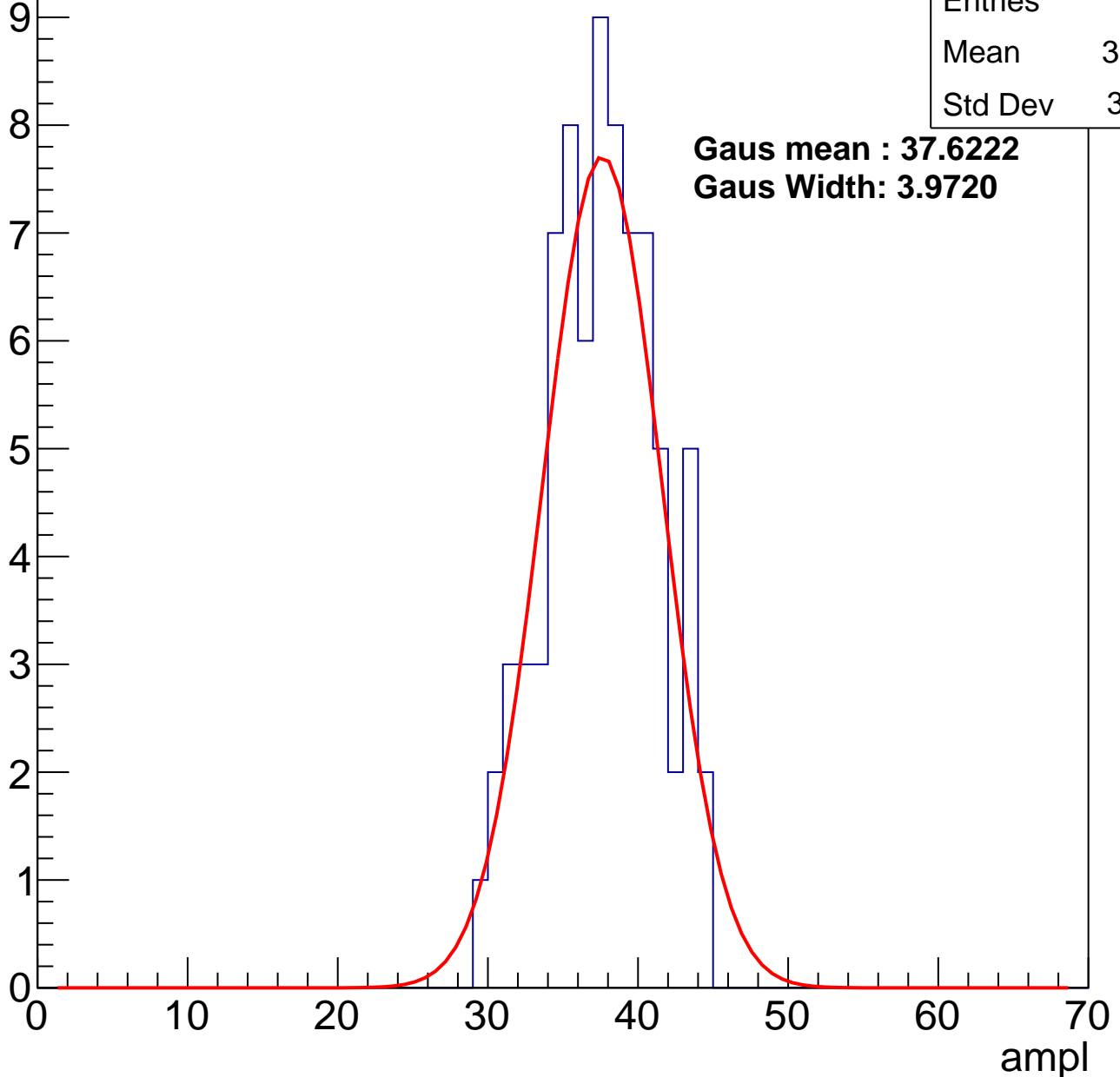
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	78
Mean	37.09
Std Dev	3.581

**Gaus mean : 37.6222**

**Gaus Width: 3.9720**



# B1L003S, U26-ch52, adc2

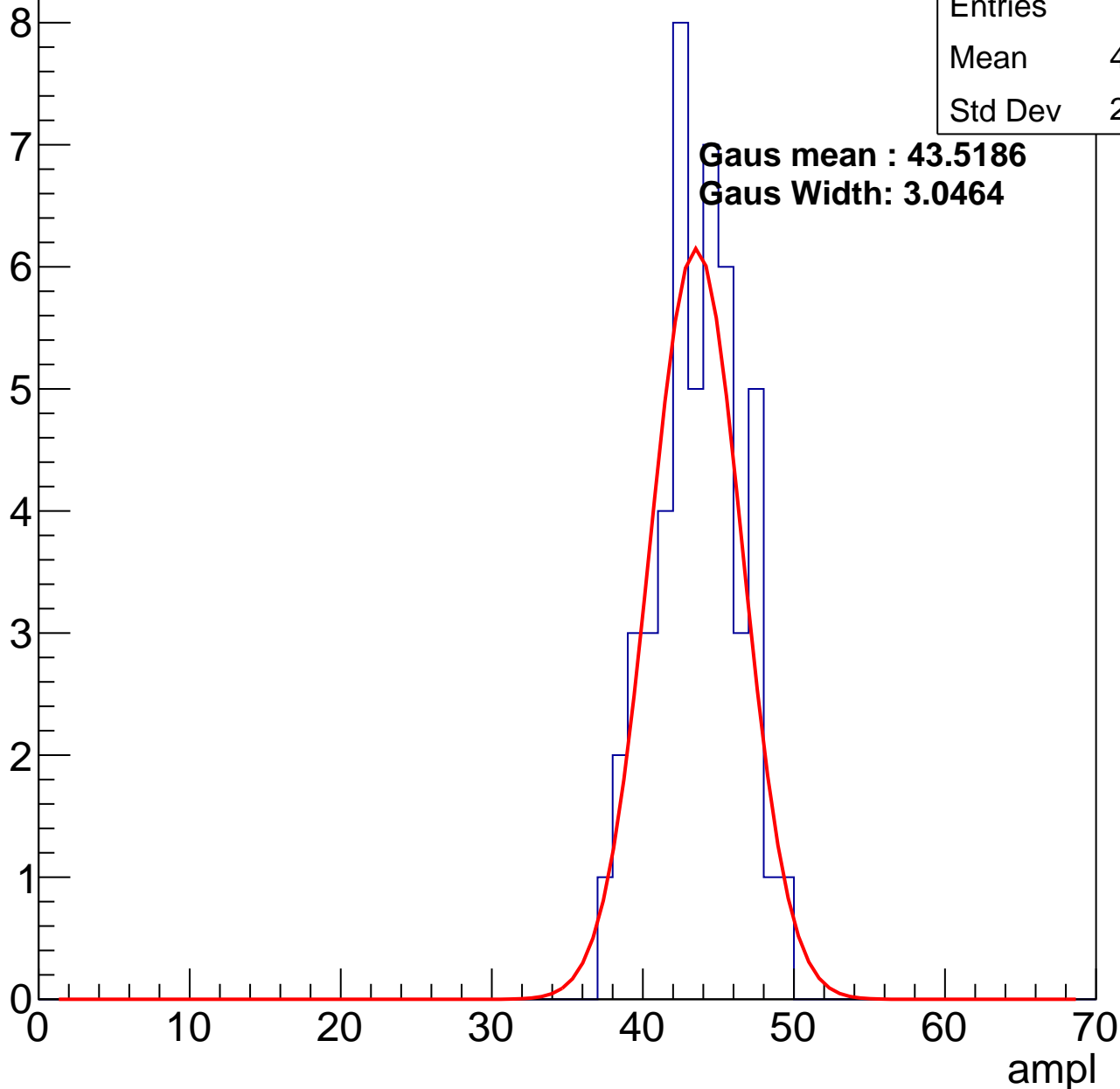
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	49
Mean	43.12
Std Dev	2.797

**Gaus mean : 43.5186**

**Gaus Width: 3.0464**

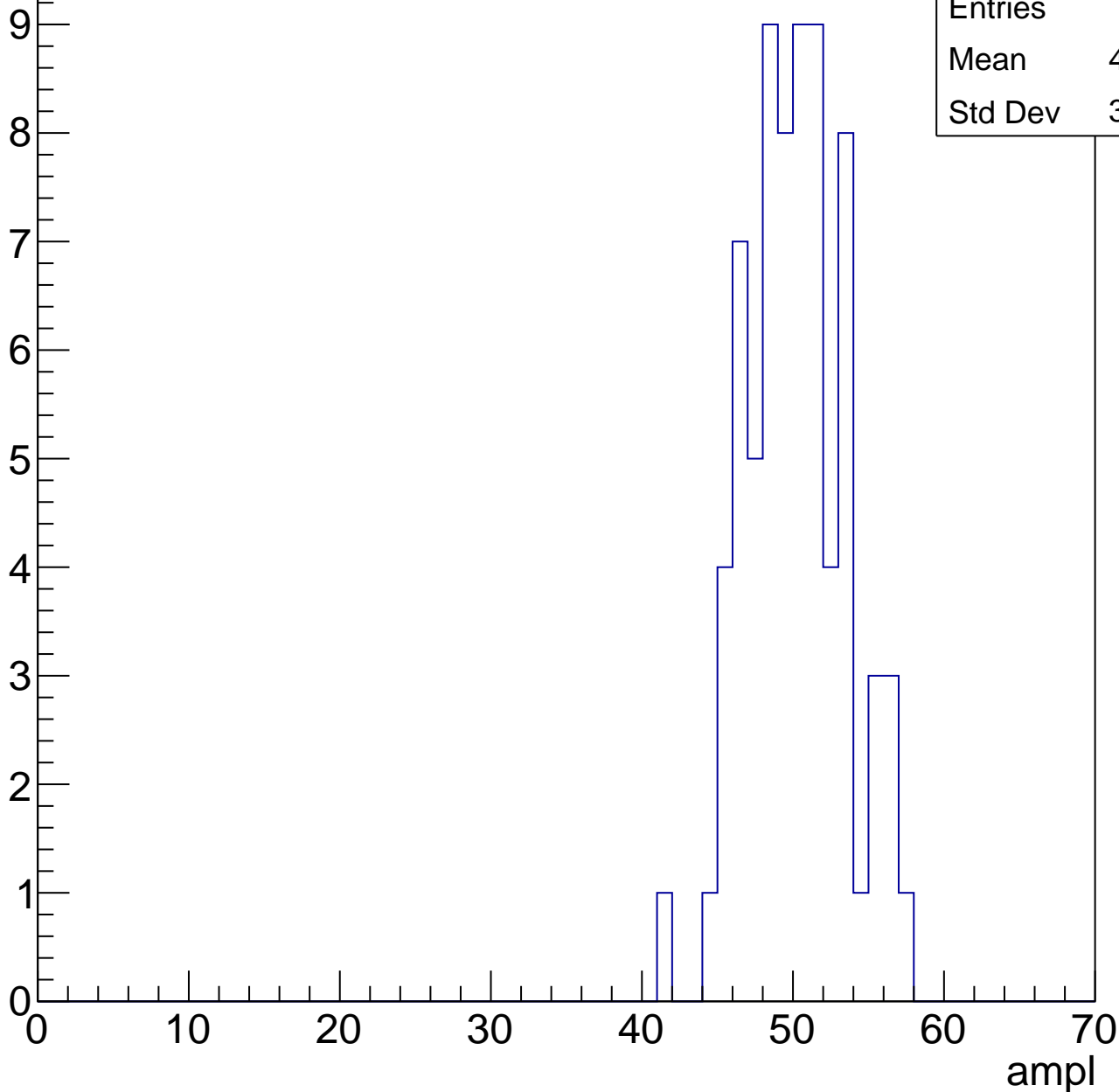


# B1L003S, U26-ch52, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

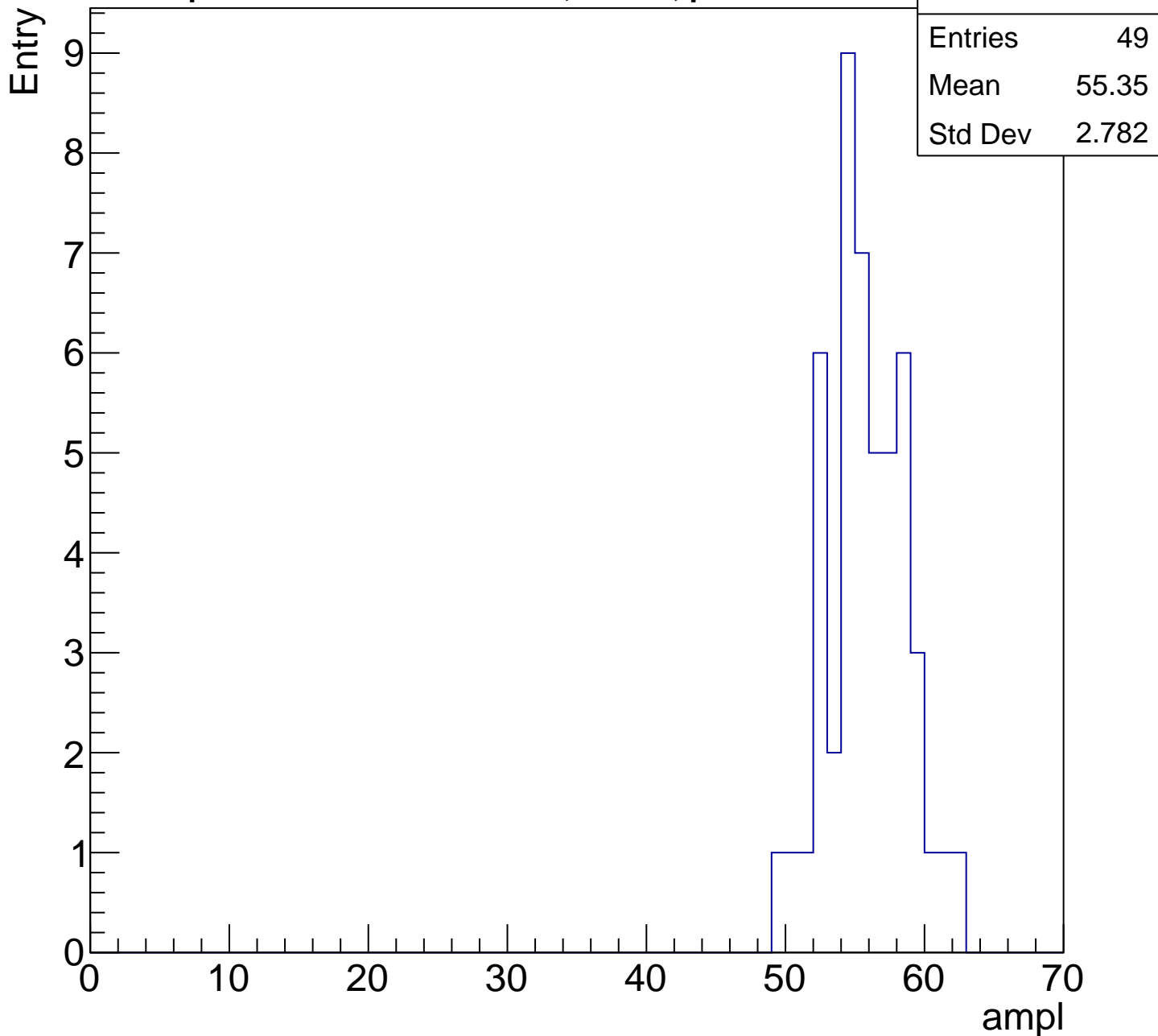
Entry

Entries	73
Mean	49.74
Std Dev	3.222



# B1L003S, U26-ch52, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2



# B1L003S, U26-ch52, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	51
Mean	59.06
Std Dev	8.58

ampl

0

10

20

30

40

50

60

70

# B1L003S, U26-ch52, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch52, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U26-ch53, adc0

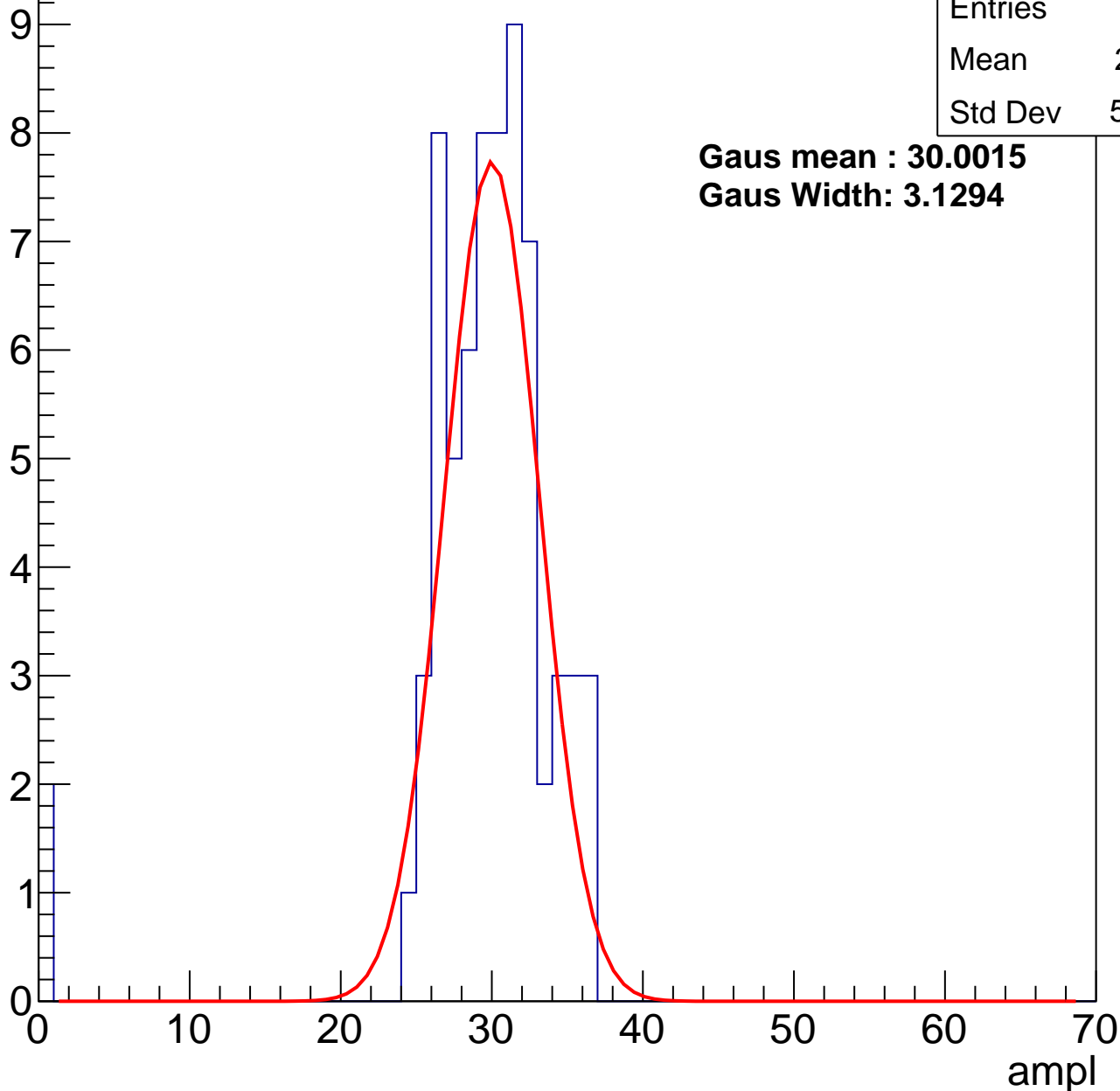
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	28.91
Std Dev	5.843

**Gaus mean : 30.0015**

**Gaus Width: 3.1294**



# B1L003S, U26-ch53, adc1

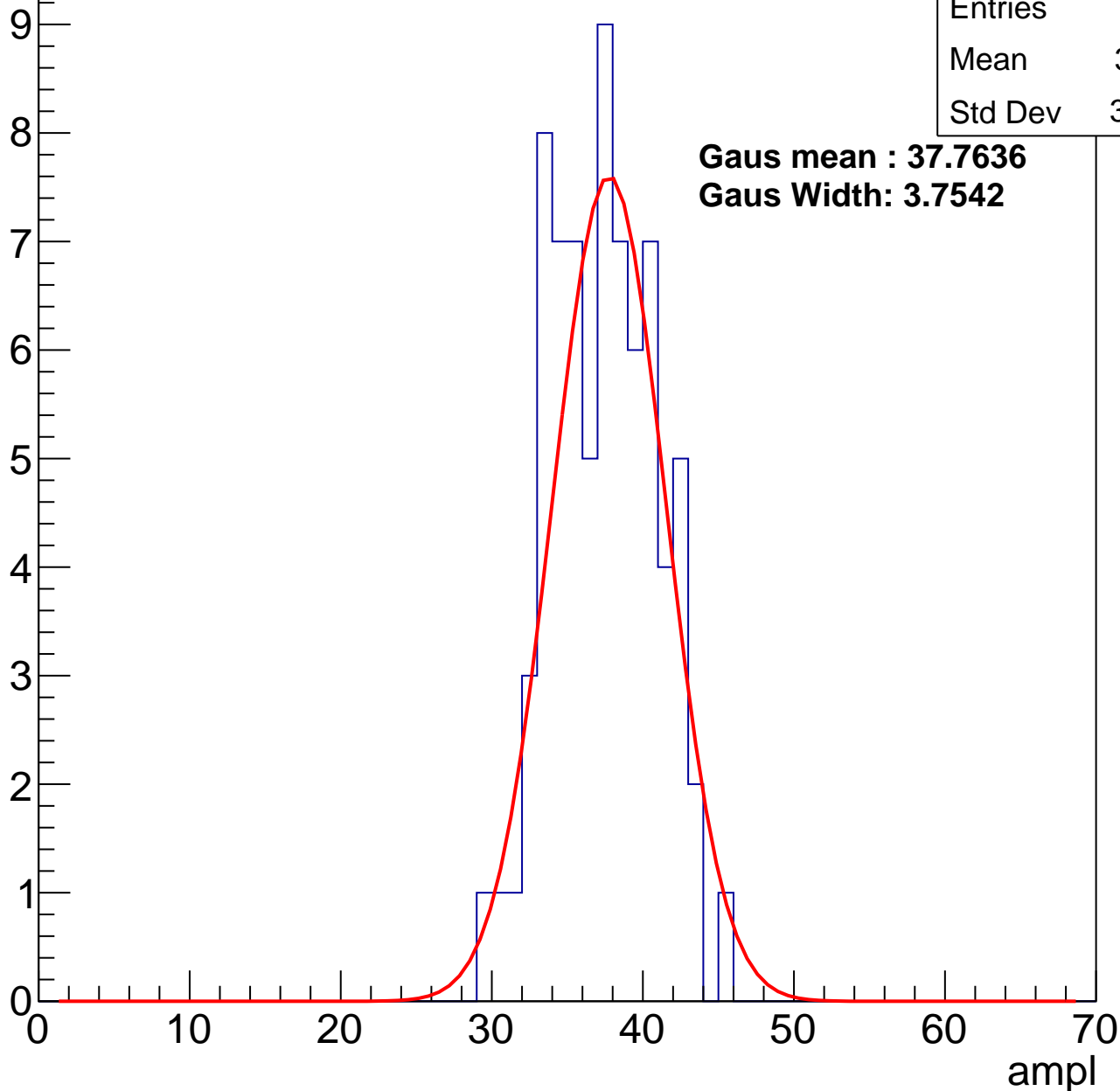
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	74
Mean	36.91
Std Dev	3.422

**Gaus mean : 37.7636**

**Gaus Width: 3.7542**



# B1L003S, U26-ch53, adc2

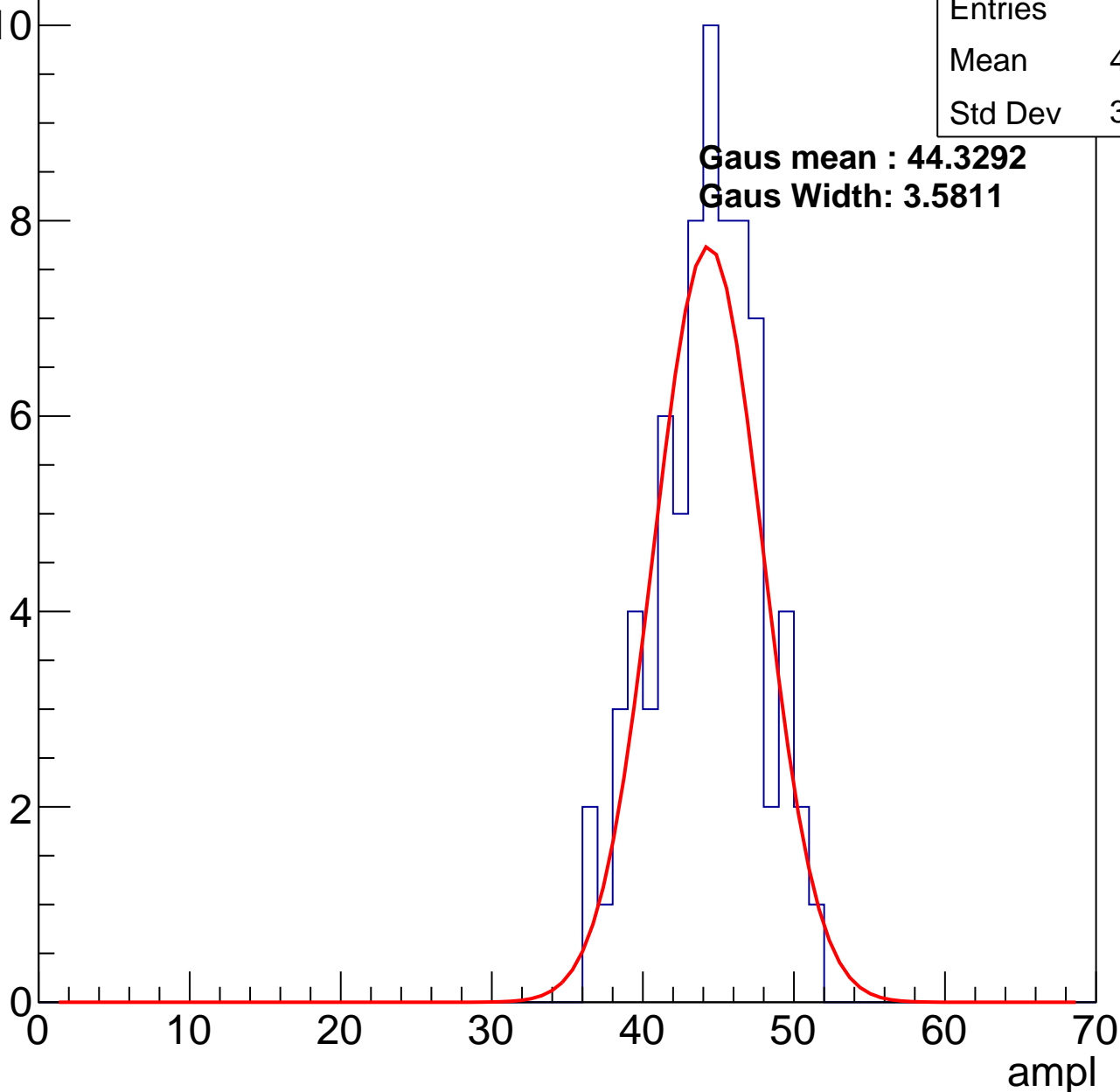
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	74
Mean	43.77
Std Dev	3.423

**Gaus mean : 44.3292**

**Gaus Width: 3.5811**

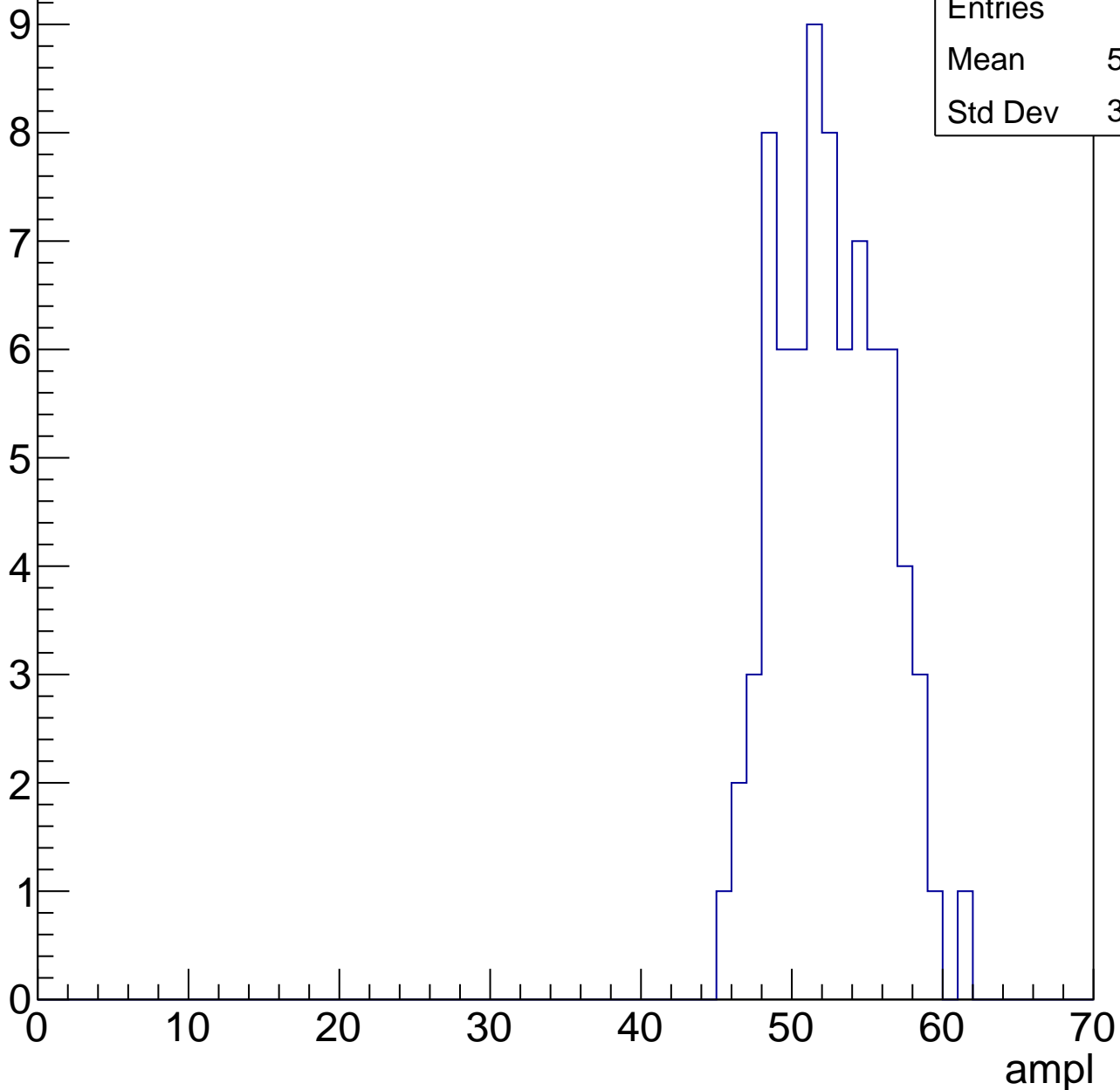


# B1L003S, U26-ch53, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	77
Mean	52.14
Std Dev	3.478

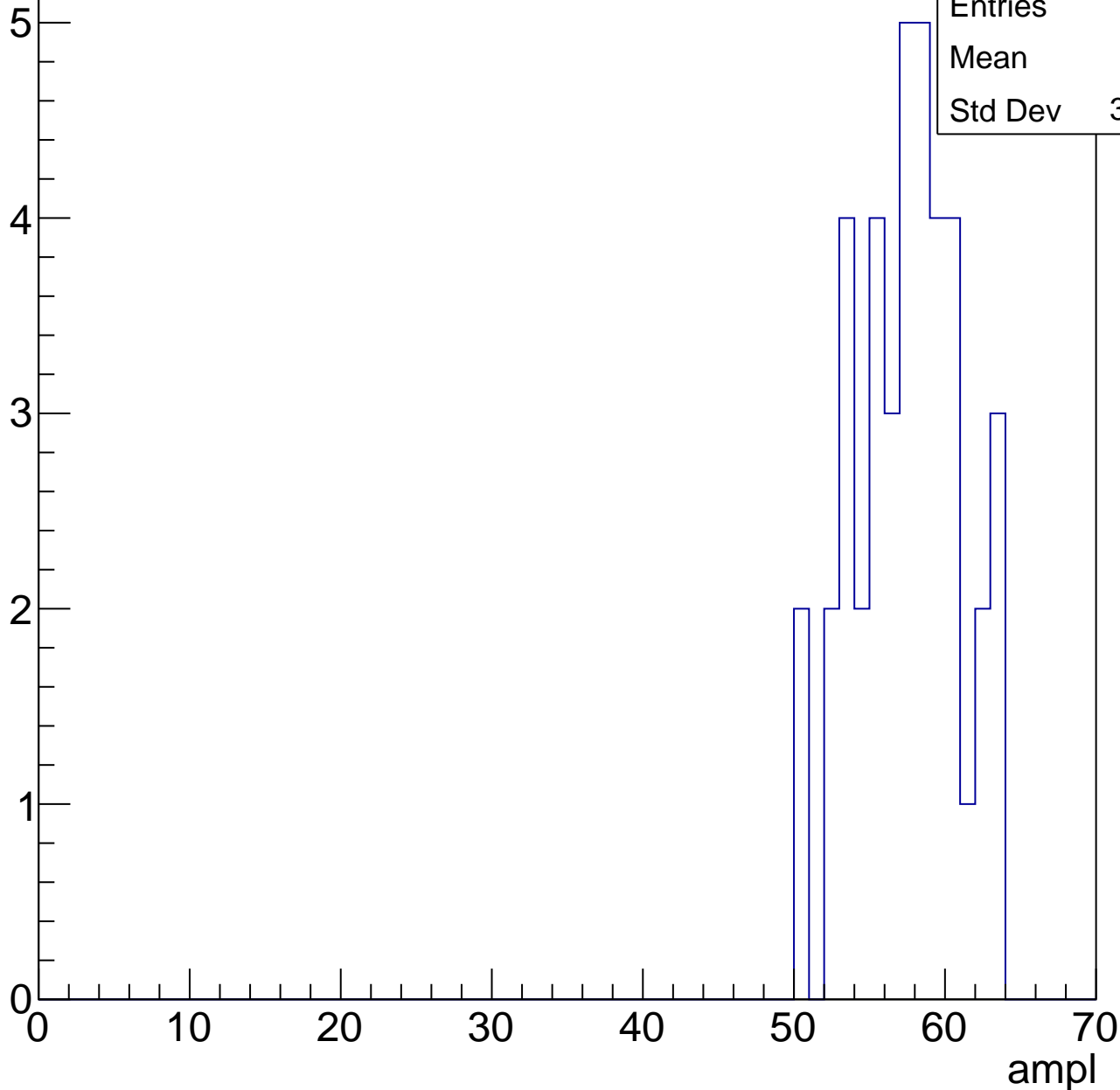


# B1L003S, U26-ch53, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	41
Mean	57
Std Dev	3.422

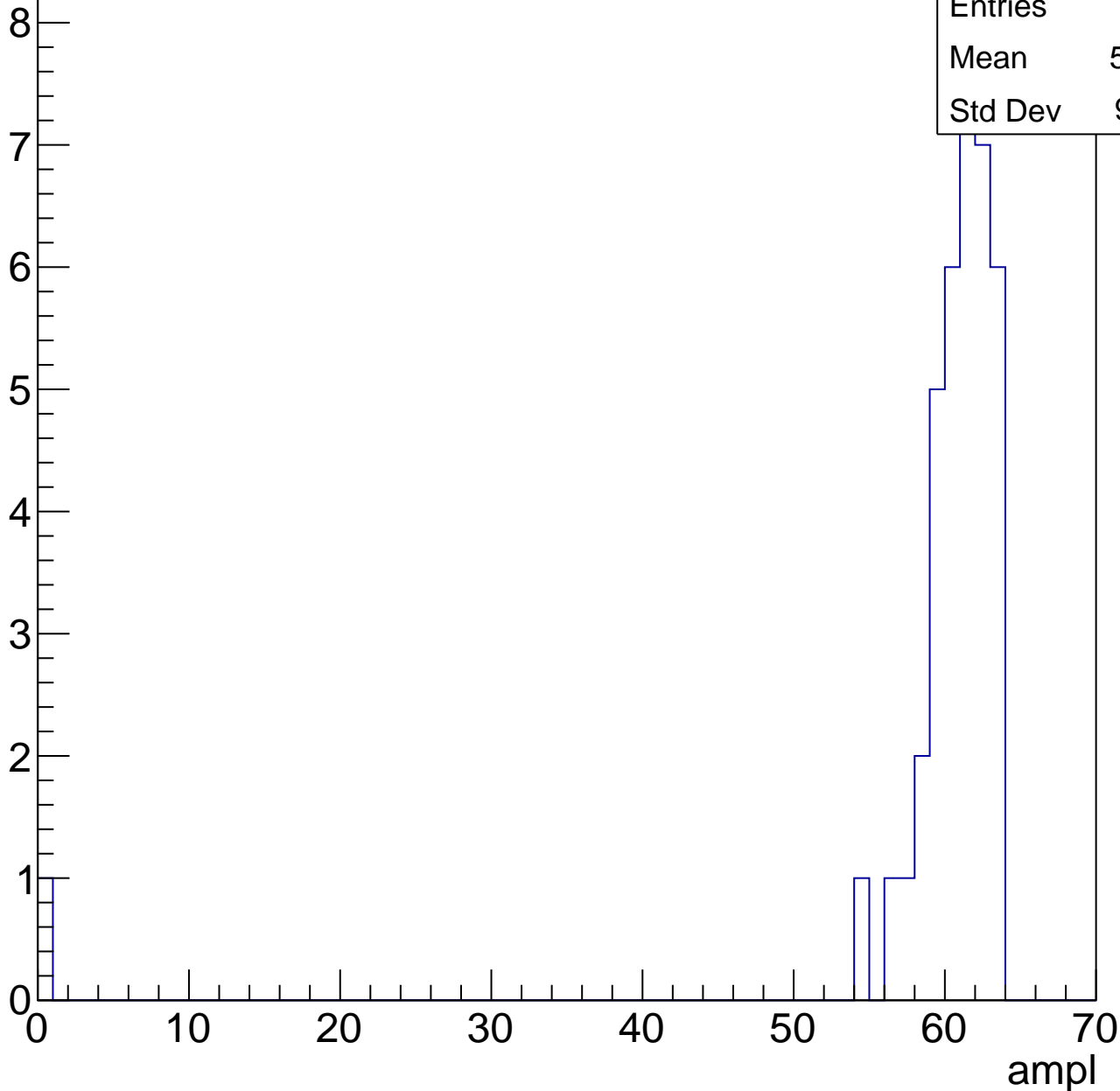


# B1L003S, U26-ch53, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	38
Mean	58.89
Std Dev	9.891



# B1L003S, U26-ch53, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch53, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	22
Std Dev	0

ampl

# B1L003S, U26-ch54, adc0

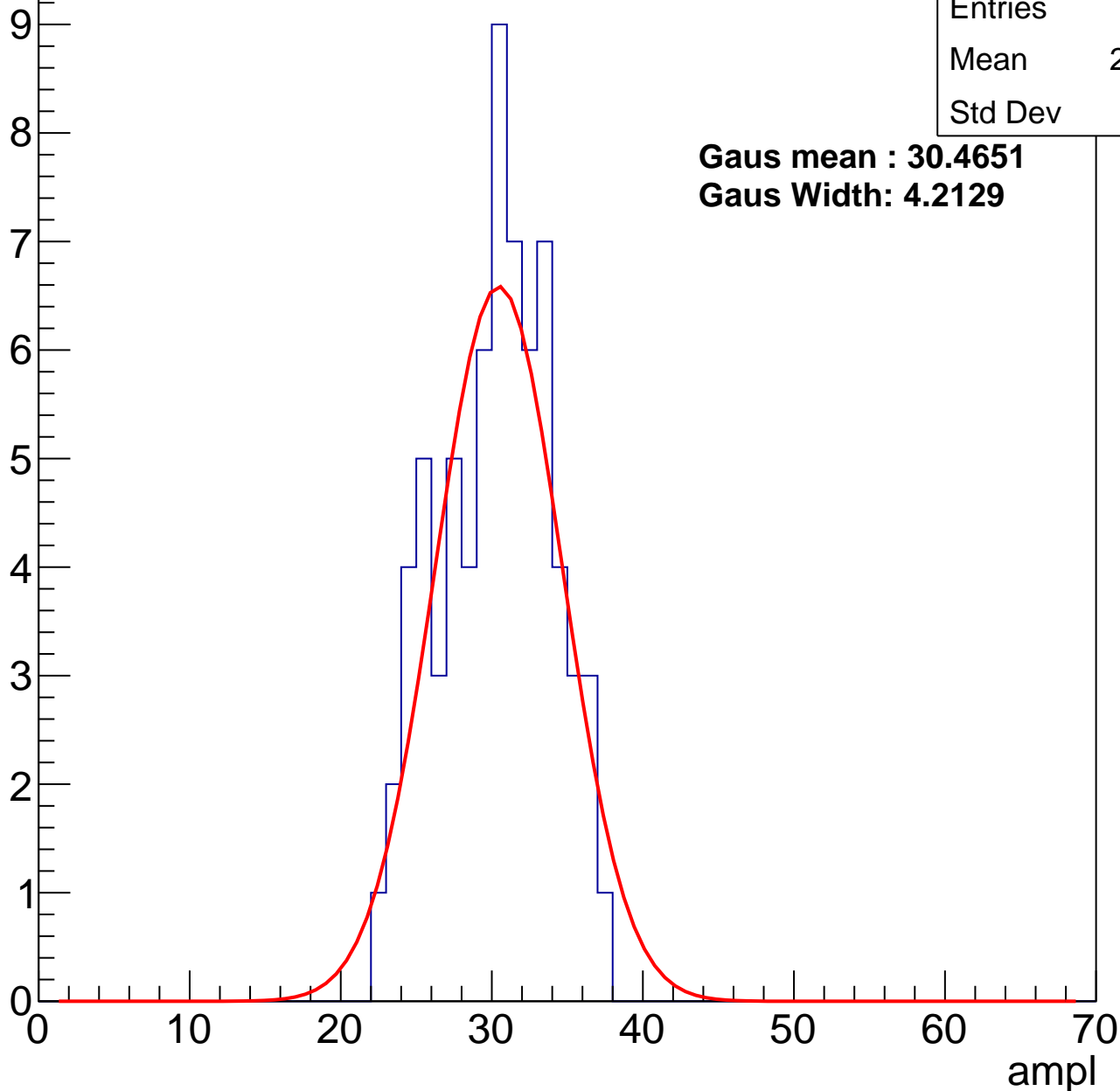
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	29.77
Std Dev	3.65

**Gaus mean : 30.4651**

**Gaus Width: 4.2129**



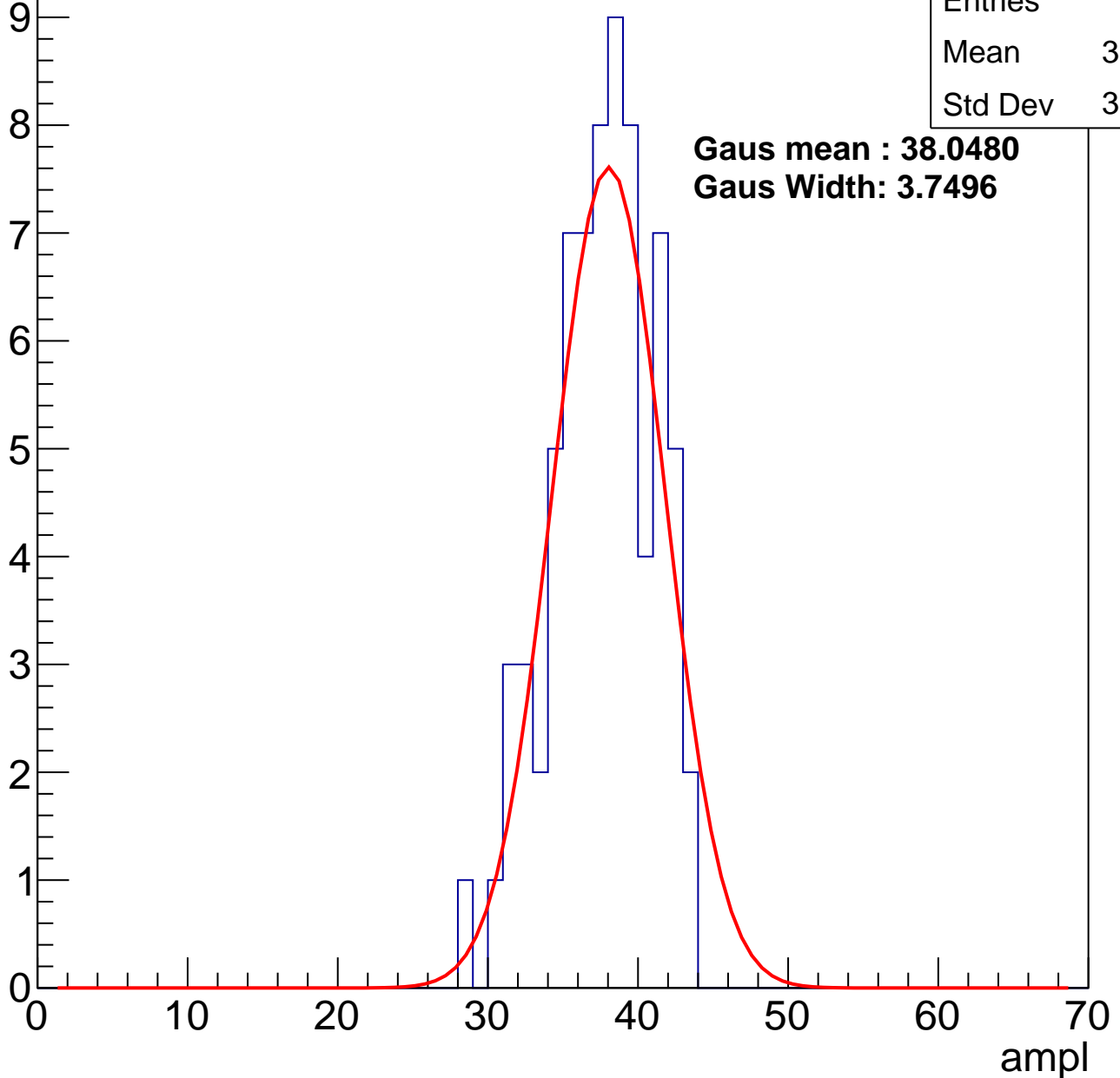
# B1L003S, U26-ch54, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	72
Mean	37.12
Std Dev	3.354

**Gaus mean : 38.0480**  
**Gaus Width: 3.7496**

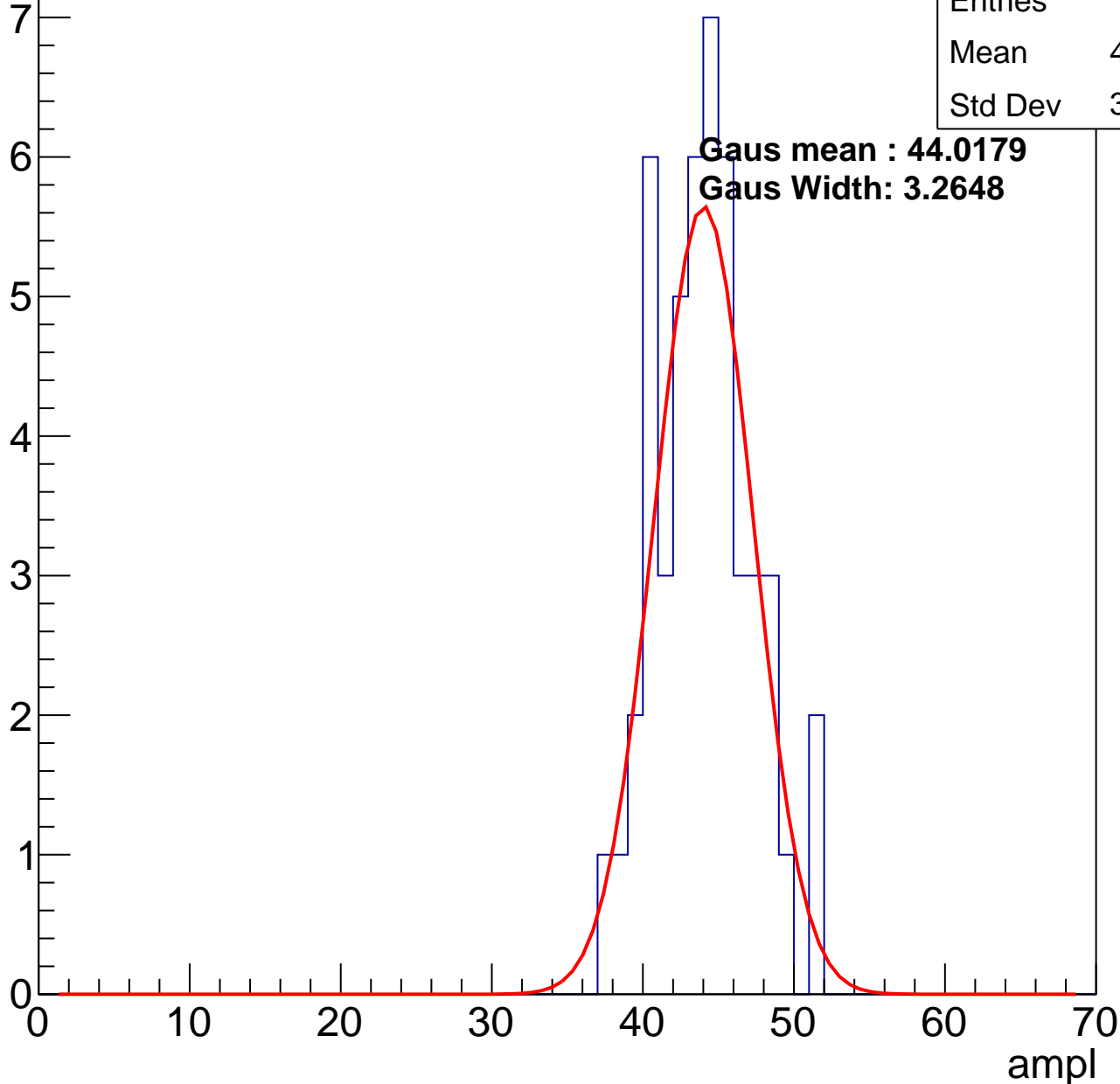


# B1L003S, U26-ch54, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

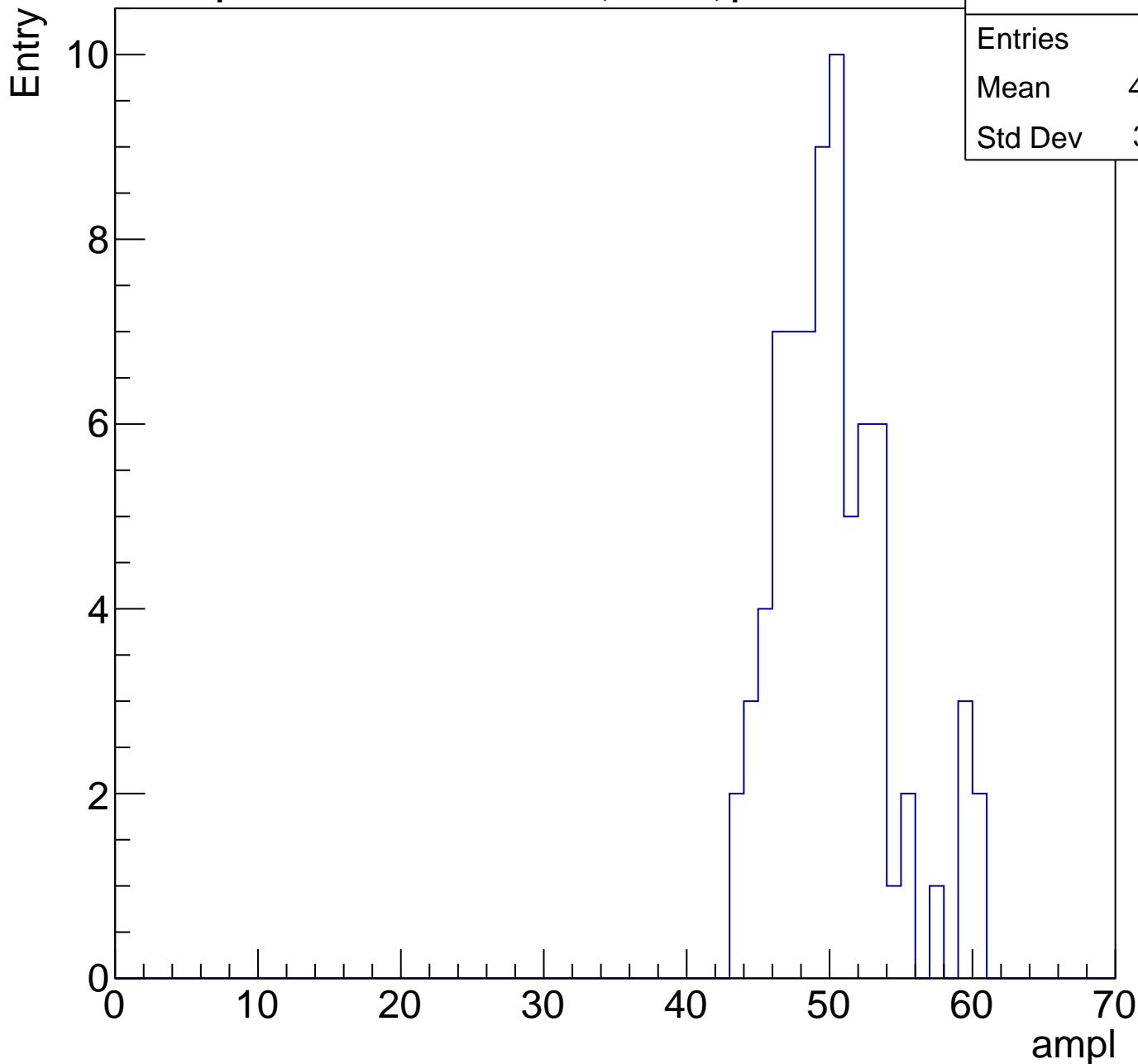
Entries	49
Mean	43.59
Std Dev	3.168



# B1L003S, U26-ch54, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	75
Mean	49.72
Std Dev	3.921

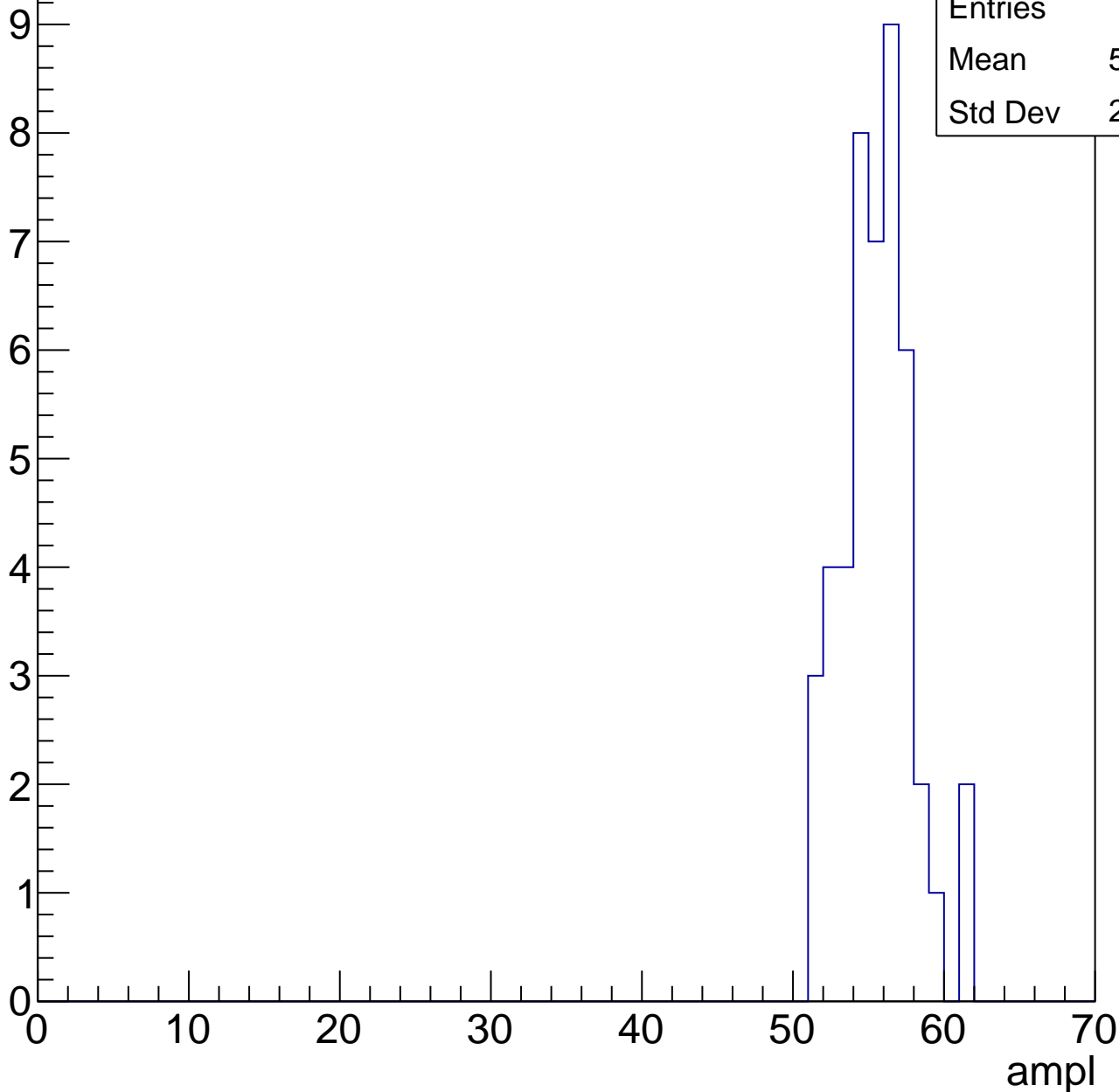


# B1L003S, U26-ch54, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

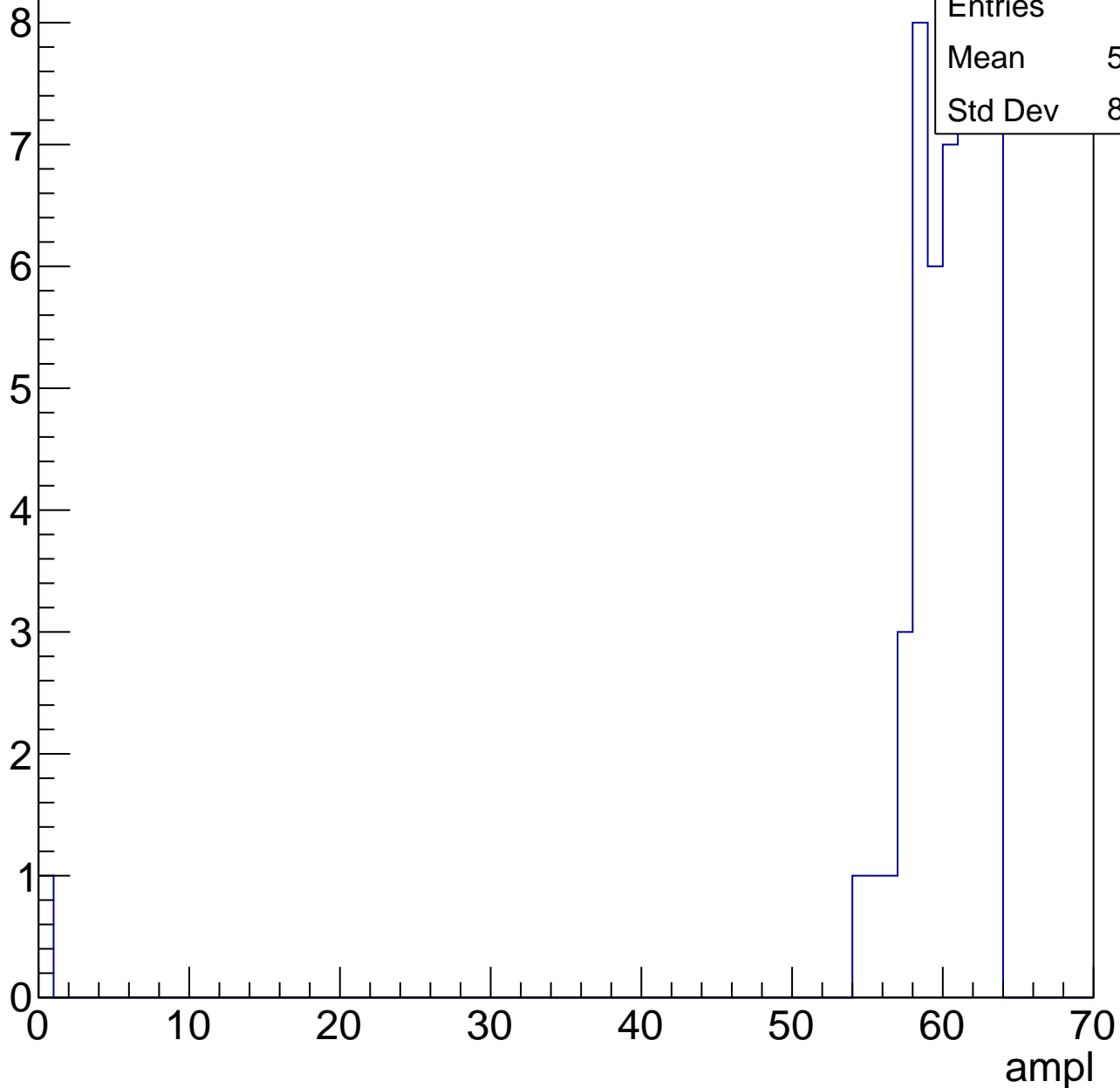
Entries	46
Mean	55.07
Std Dev	2.316



# B1L003S, U26-ch54, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U26-ch54, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch54, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U26-ch55, adc0

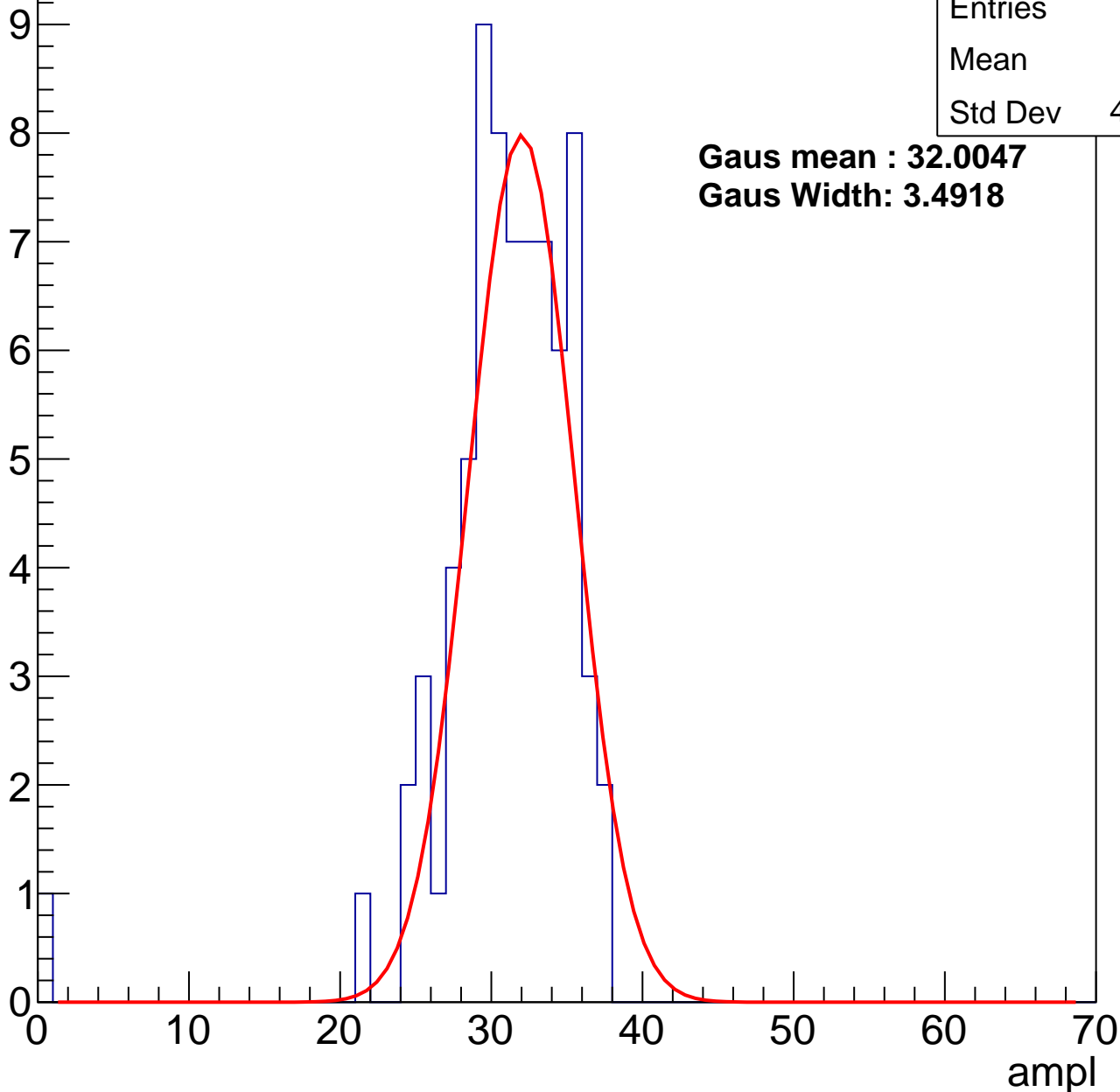
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	74
Mean	30.5
Std Dev	4.919

**Gaus mean : 32.0047**

**Gaus Width: 3.4918**



# B1L003S, U26-ch55, adc1

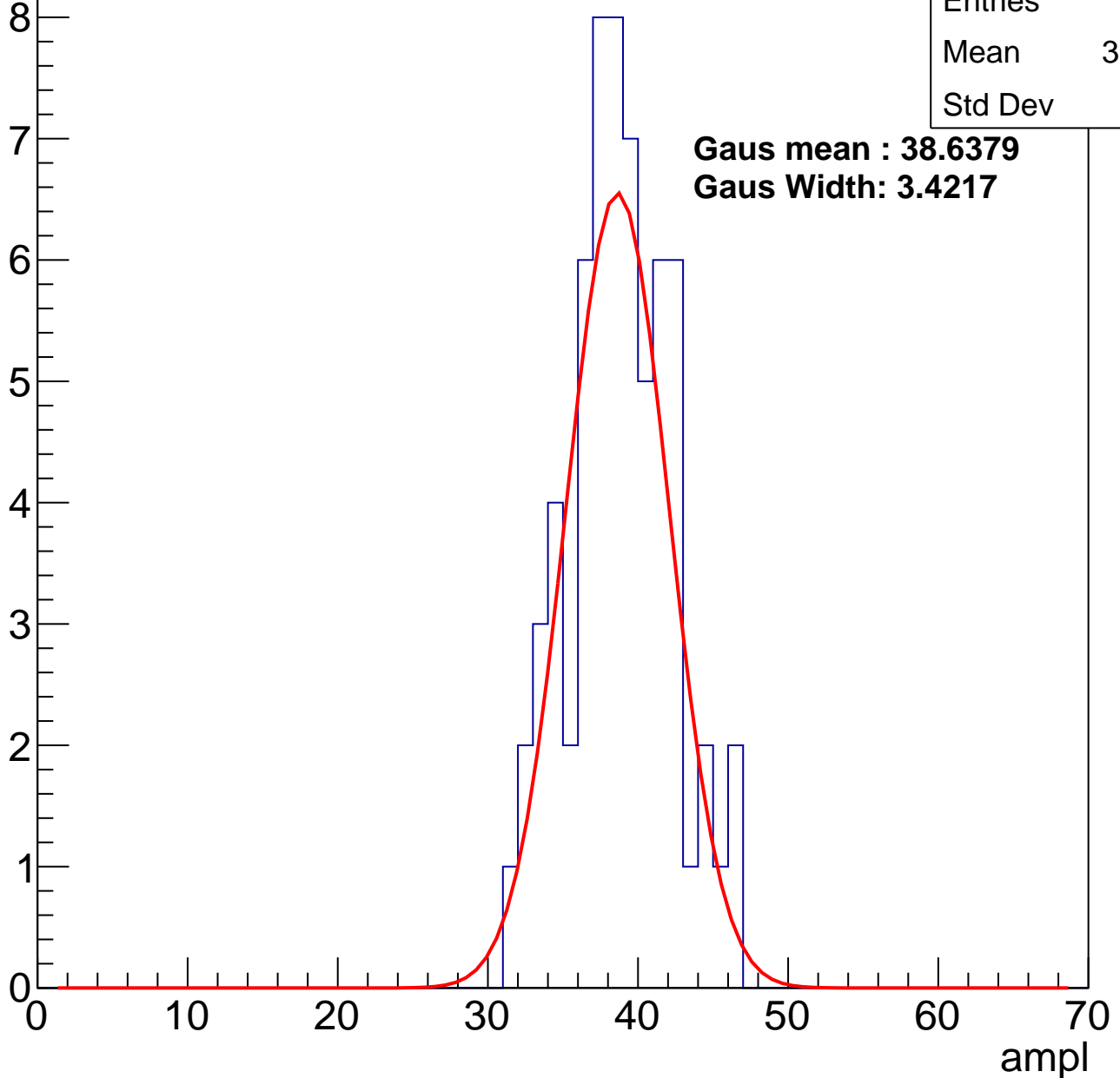
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	38.36
Std Dev	3.43

**Gaus mean : 38.6379**

**Gaus Width: 3.4217**



# B1L003S, U26-ch55, adc2

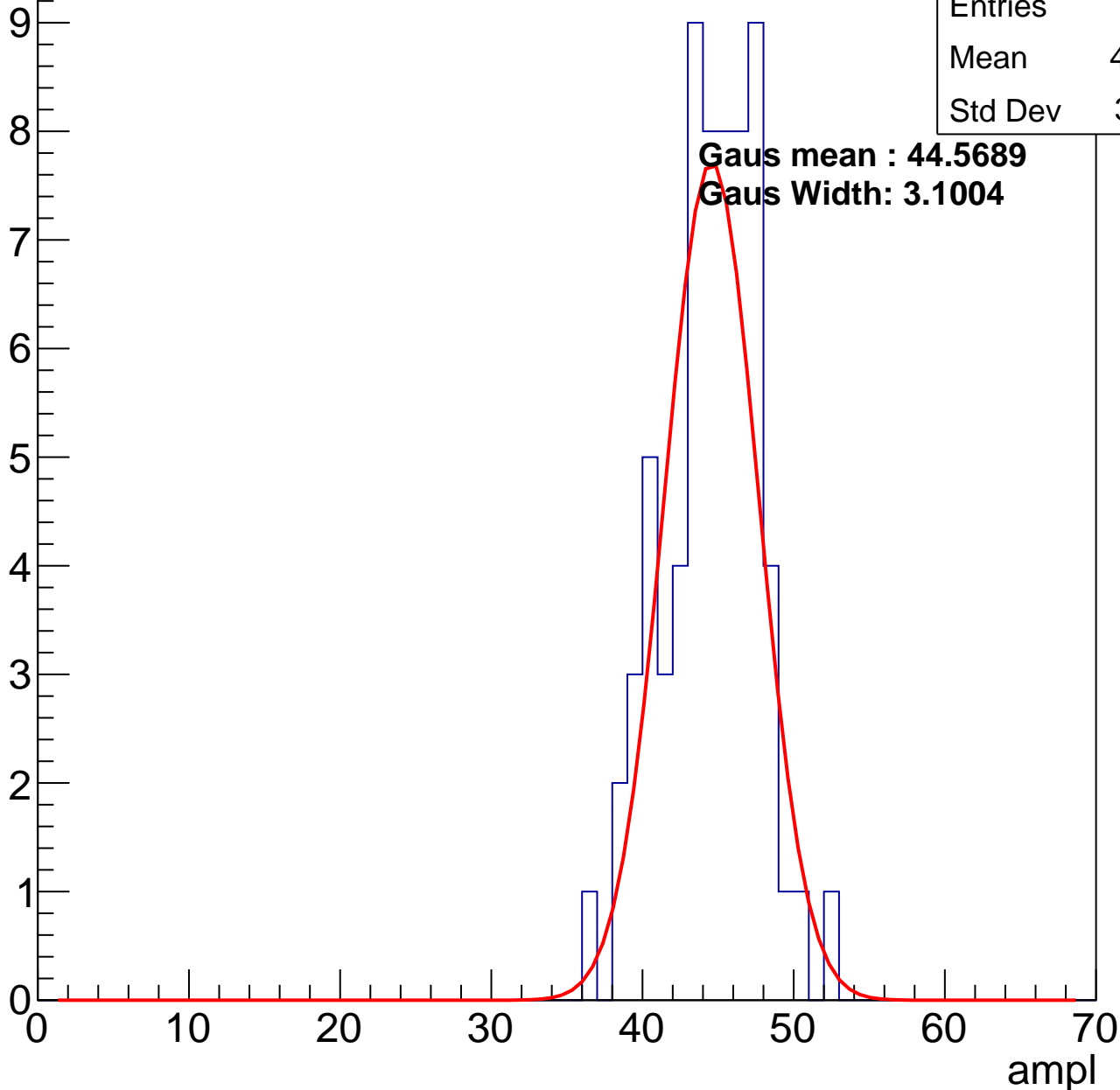
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	44.07
Std Dev	3.121

**Gaus mean : 44.5689**

**Gaus Width: 3.1004**



# B1L003S, U26-ch55, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

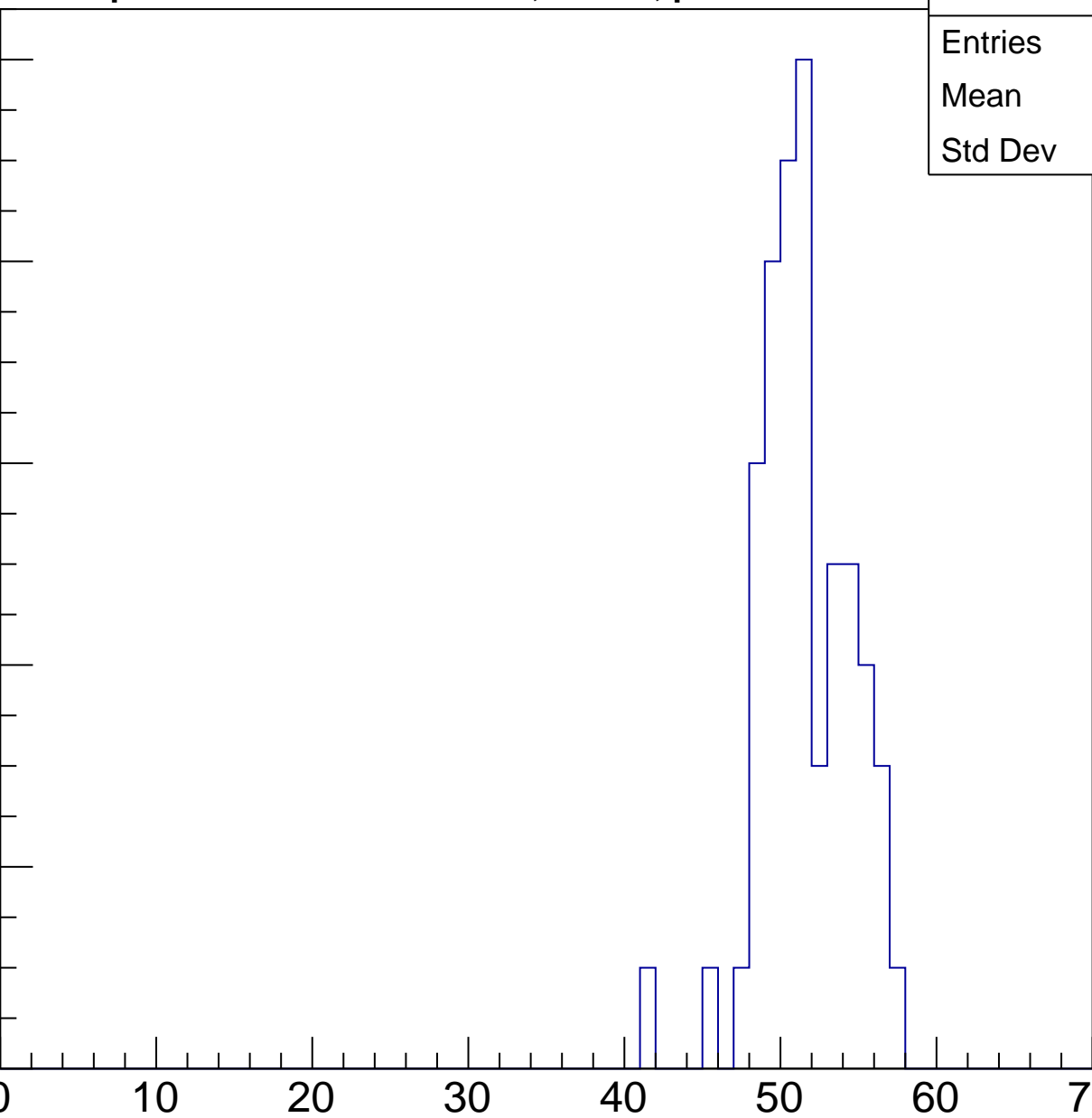
Entries	57
Mean	51.04
Std Dev	2.932

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

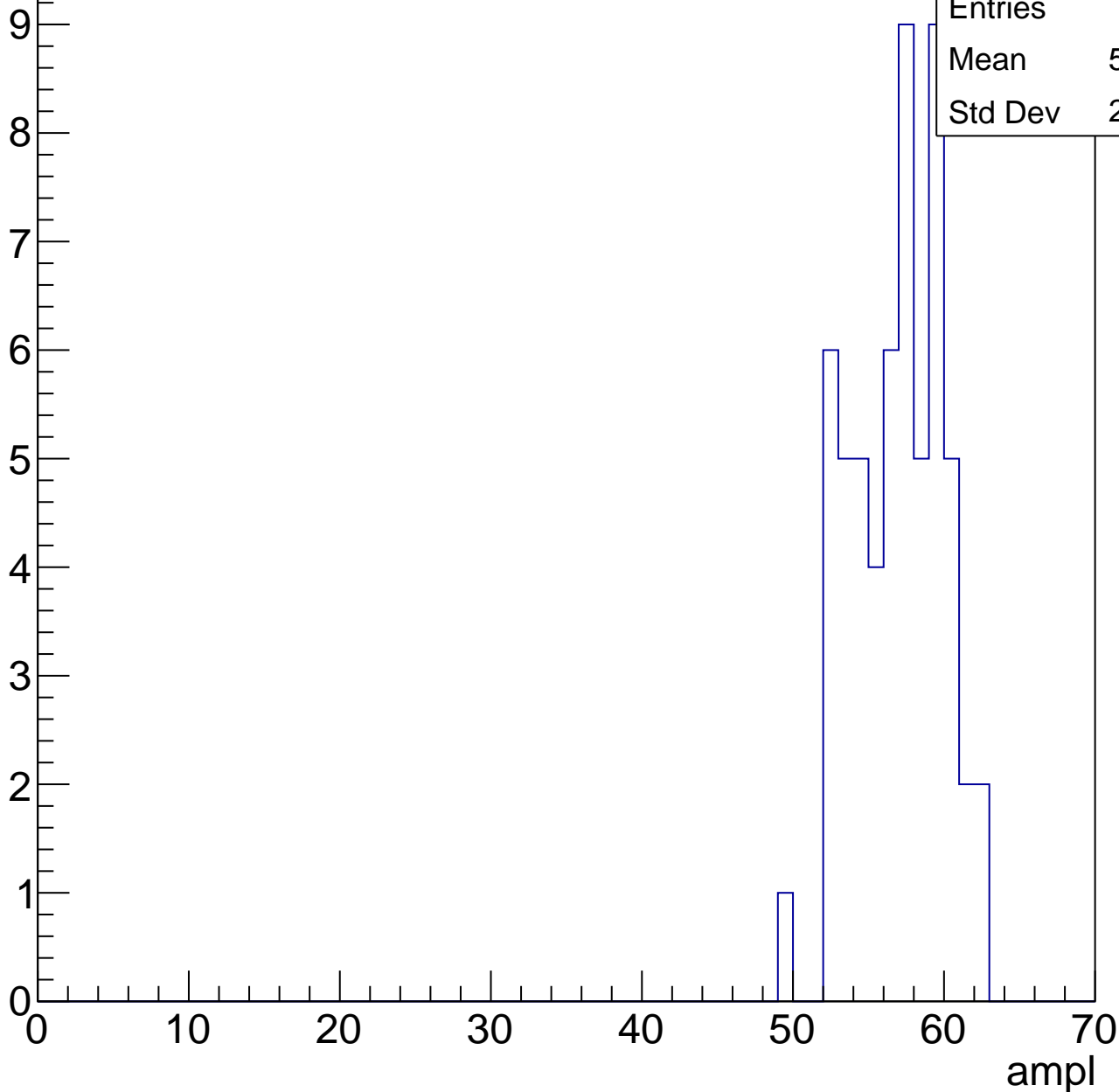


# B1L003S, U26-ch55, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	56.47
Std Dev	2.948

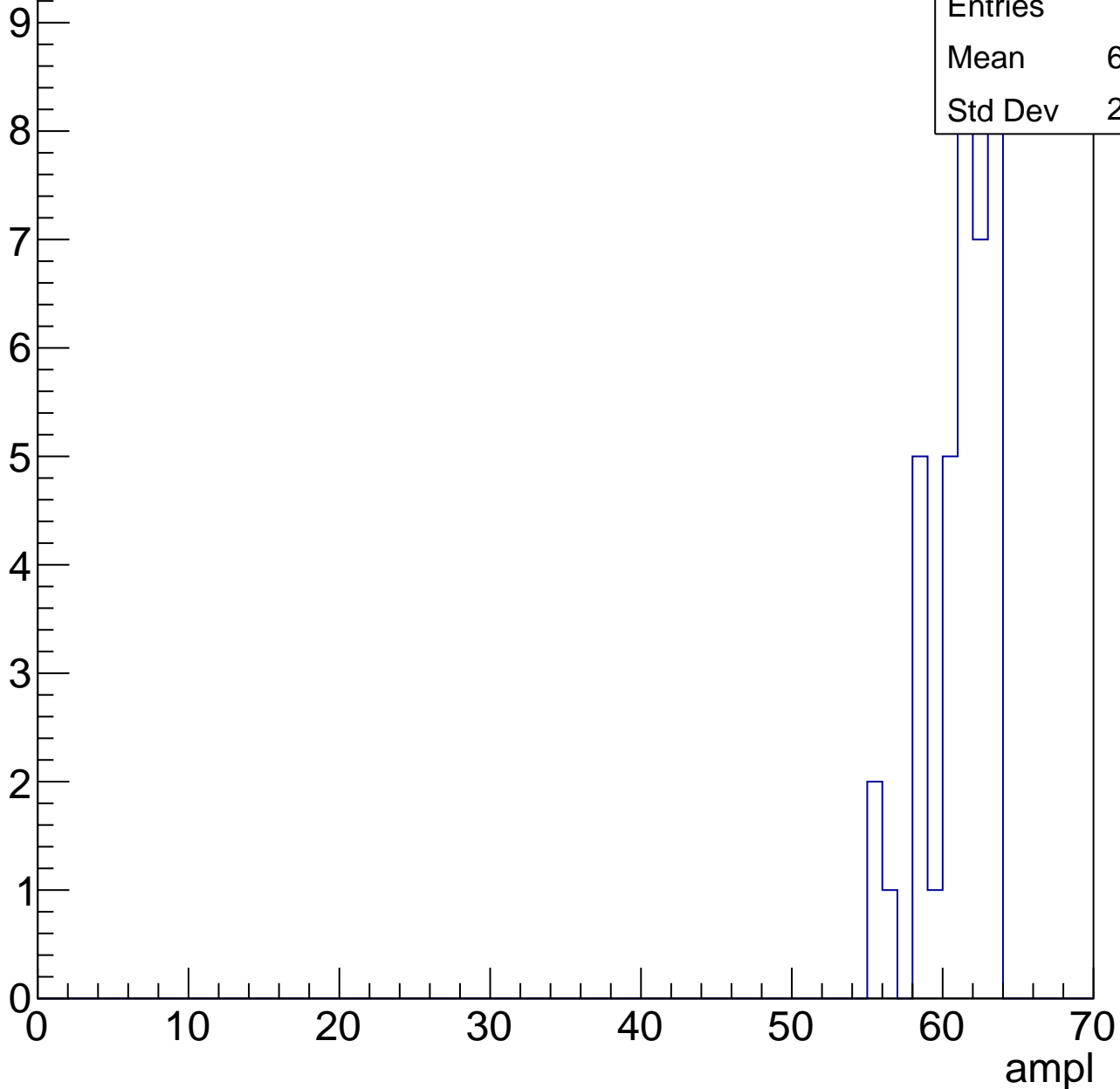


# B1L003S, U26-ch55, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	38
Mean	60.63
Std Dev	2.229



# B1L003S, U26-ch55, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch55, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U26-ch56, adc0

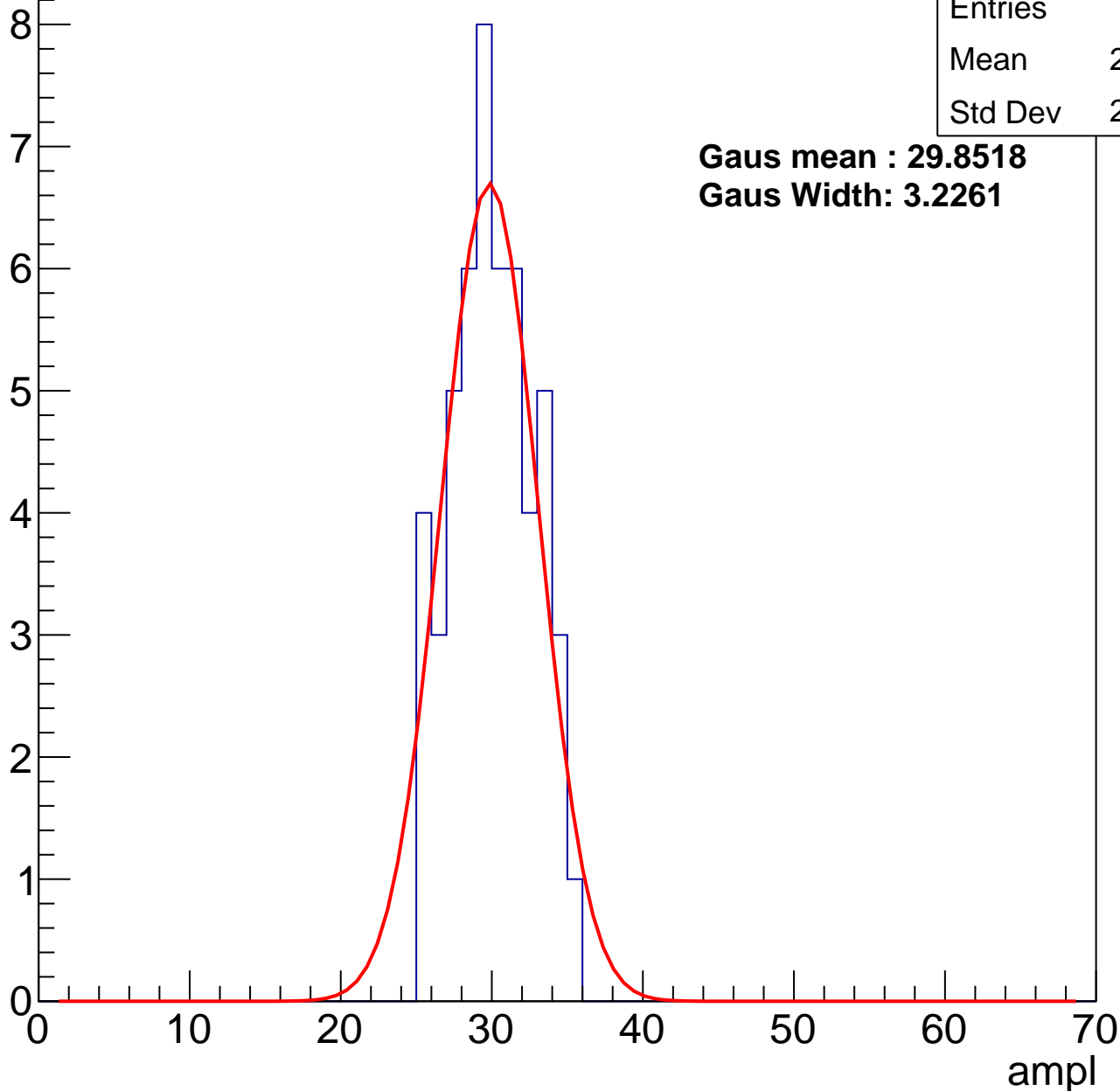
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	51
Mean	29.59
Std Dev	2.643

**Gaus mean : 29.8518**

**Gaus Width: 3.2261**



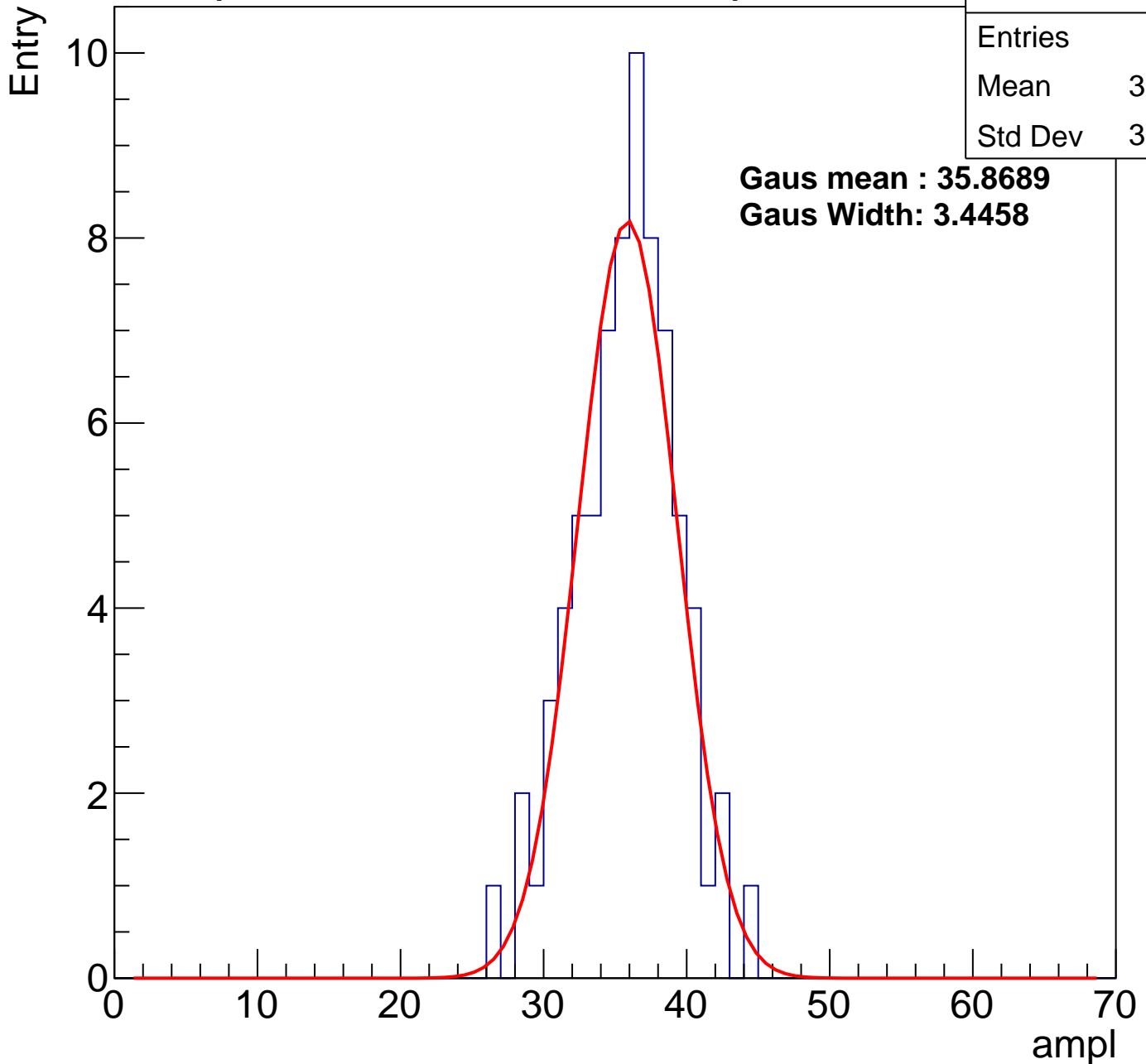
# B1L003S, U26-ch56, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	74
Mean	35.32
Std Dev	3.523

**Gaus mean : 35.8689**

**Gaus Width: 3.4458**



# B1L003S, U26-ch56, adc2

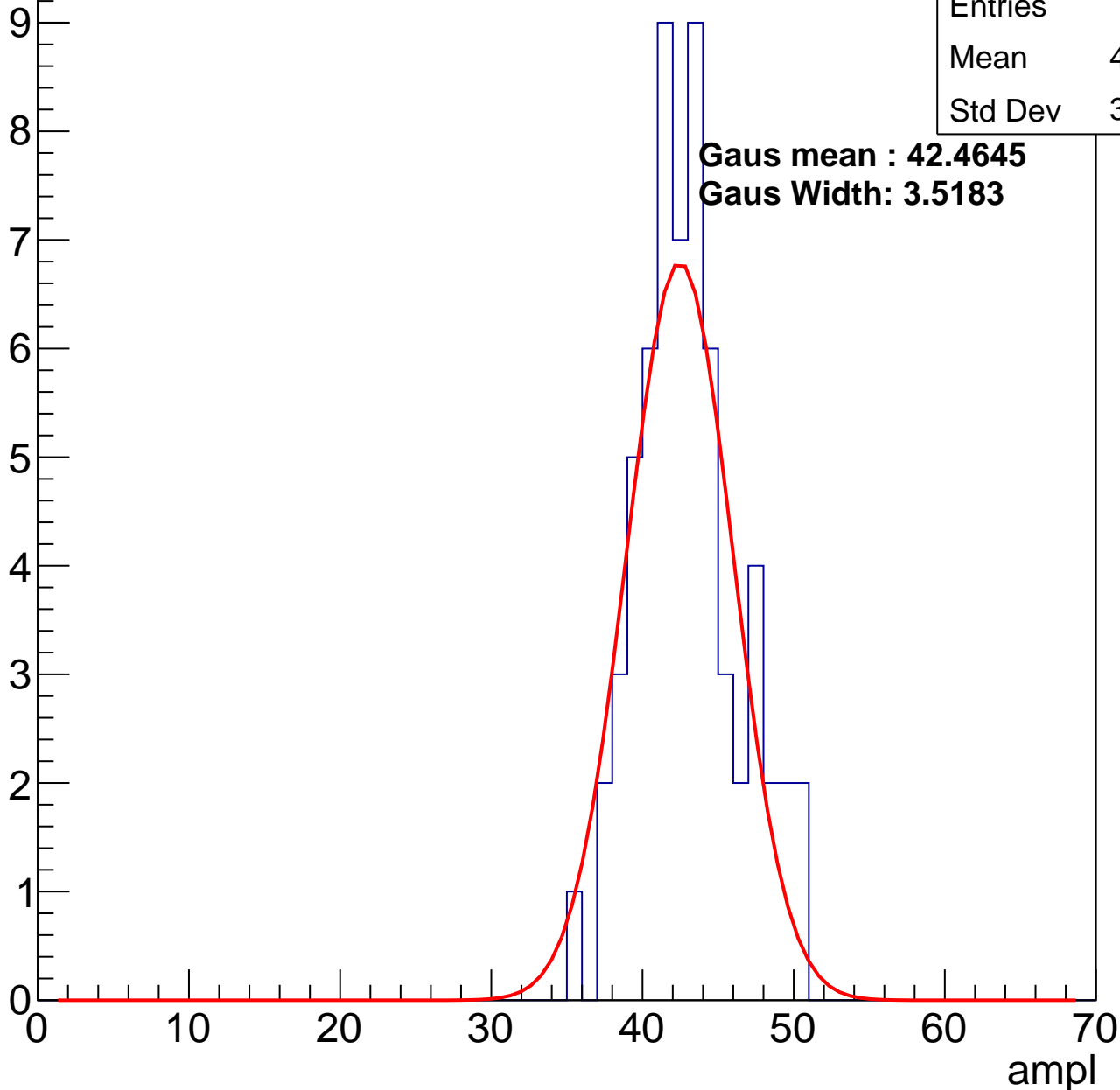
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	42.56
Std Dev	3.323

**Gaus mean : 42.4645**

**Gaus Width: 3.5183**

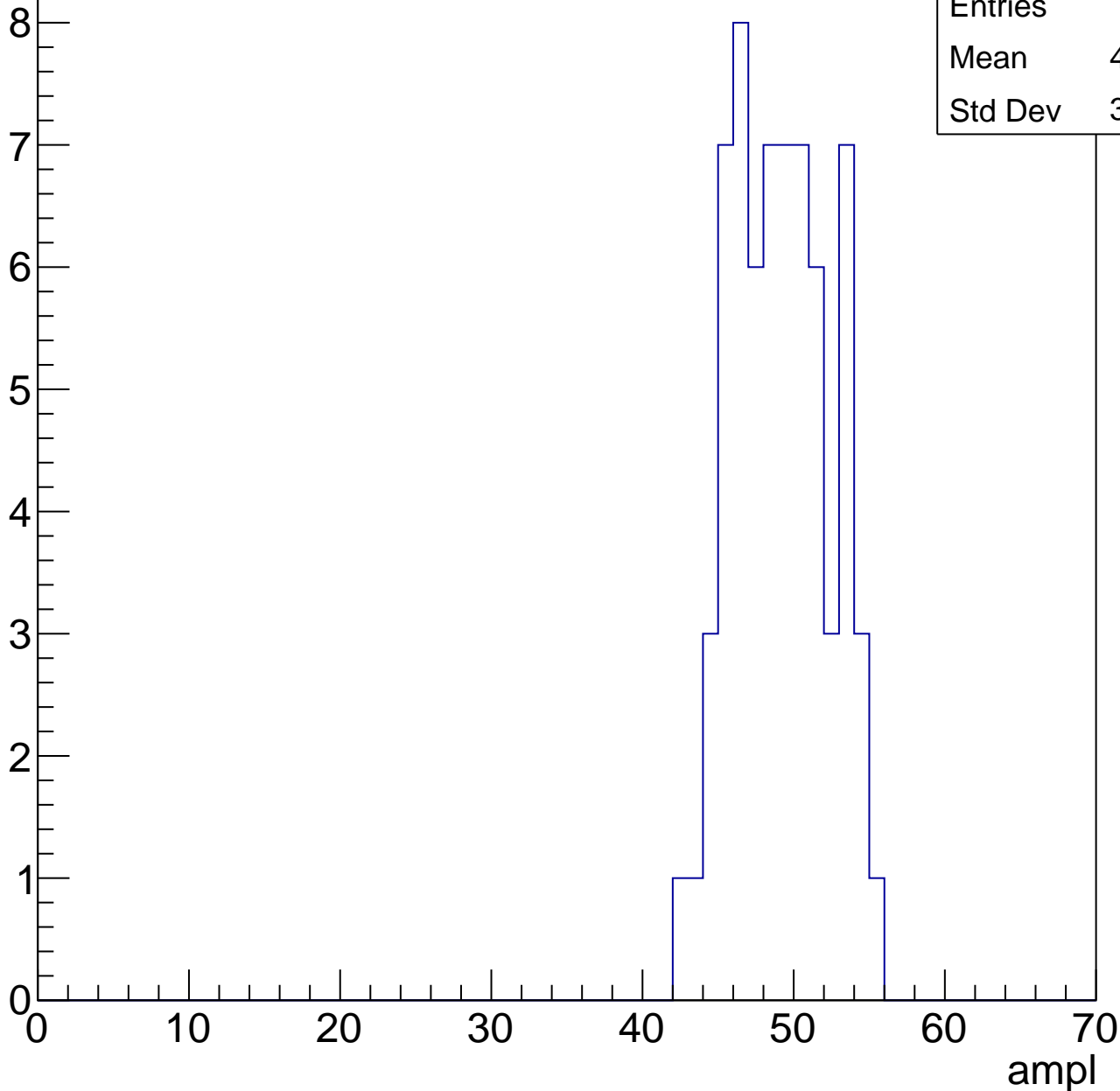


# B1L003S, U26-ch56, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

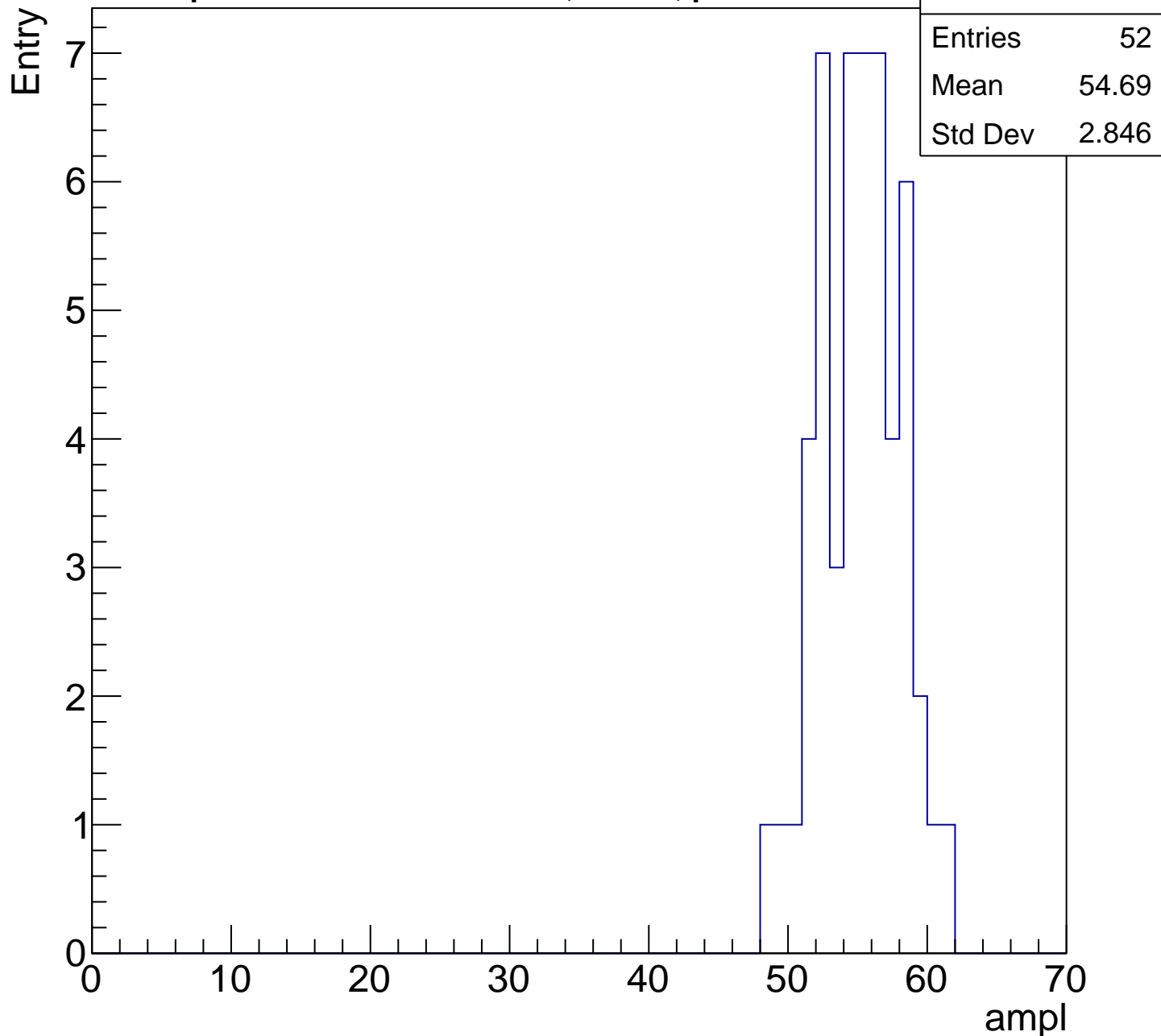
Entry

Entries	67
Mean	48.67
Std Dev	3.112



# B1L003S, U26-ch56, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2



# B1L003S, U26-ch56, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

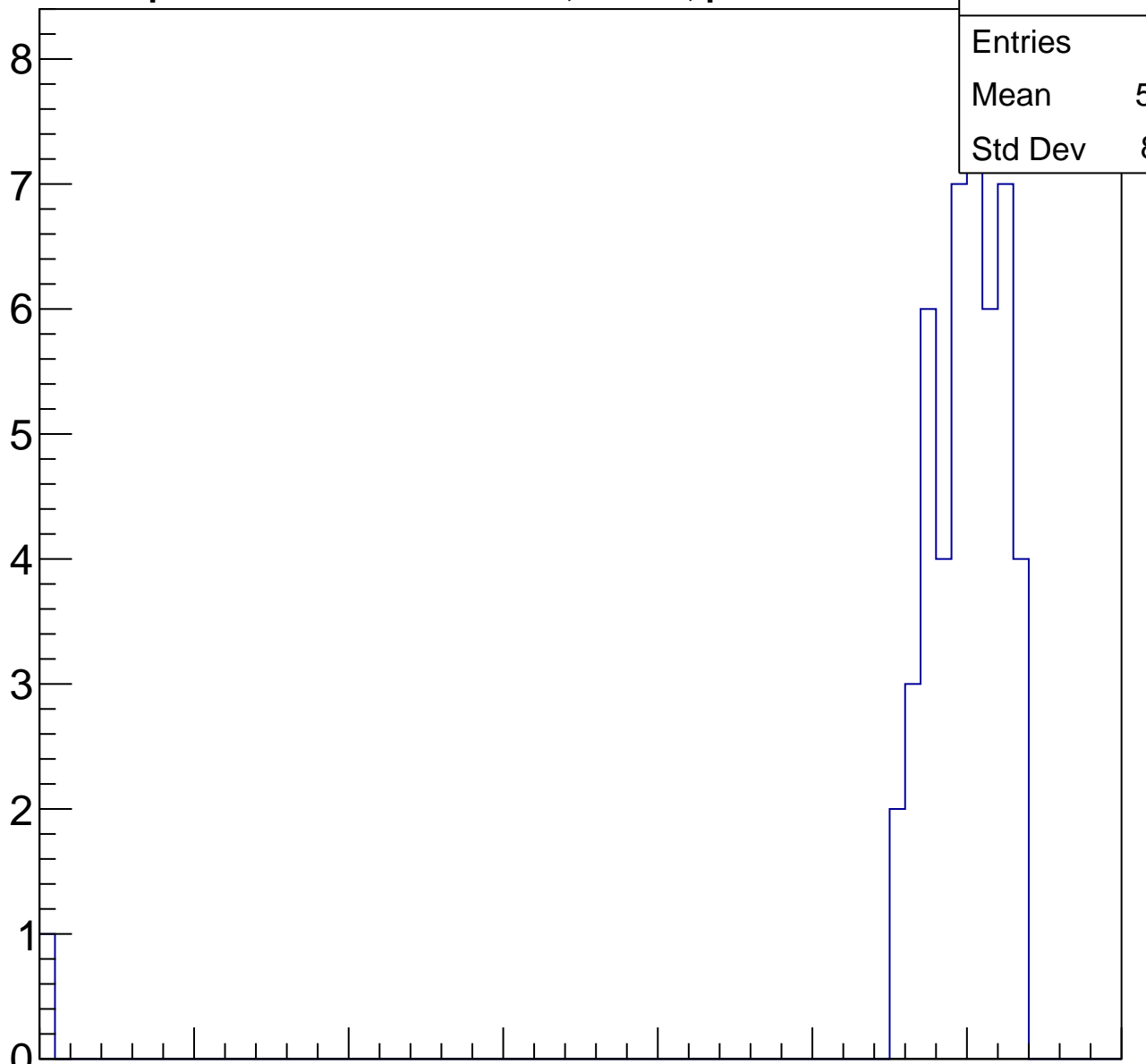
Entry

Entries	48
Mean	58.27
Std Dev	8.781

8  
7  
6  
5  
4  
3  
2  
1  
0

0 10 20 30 40 50 60 70

ampl

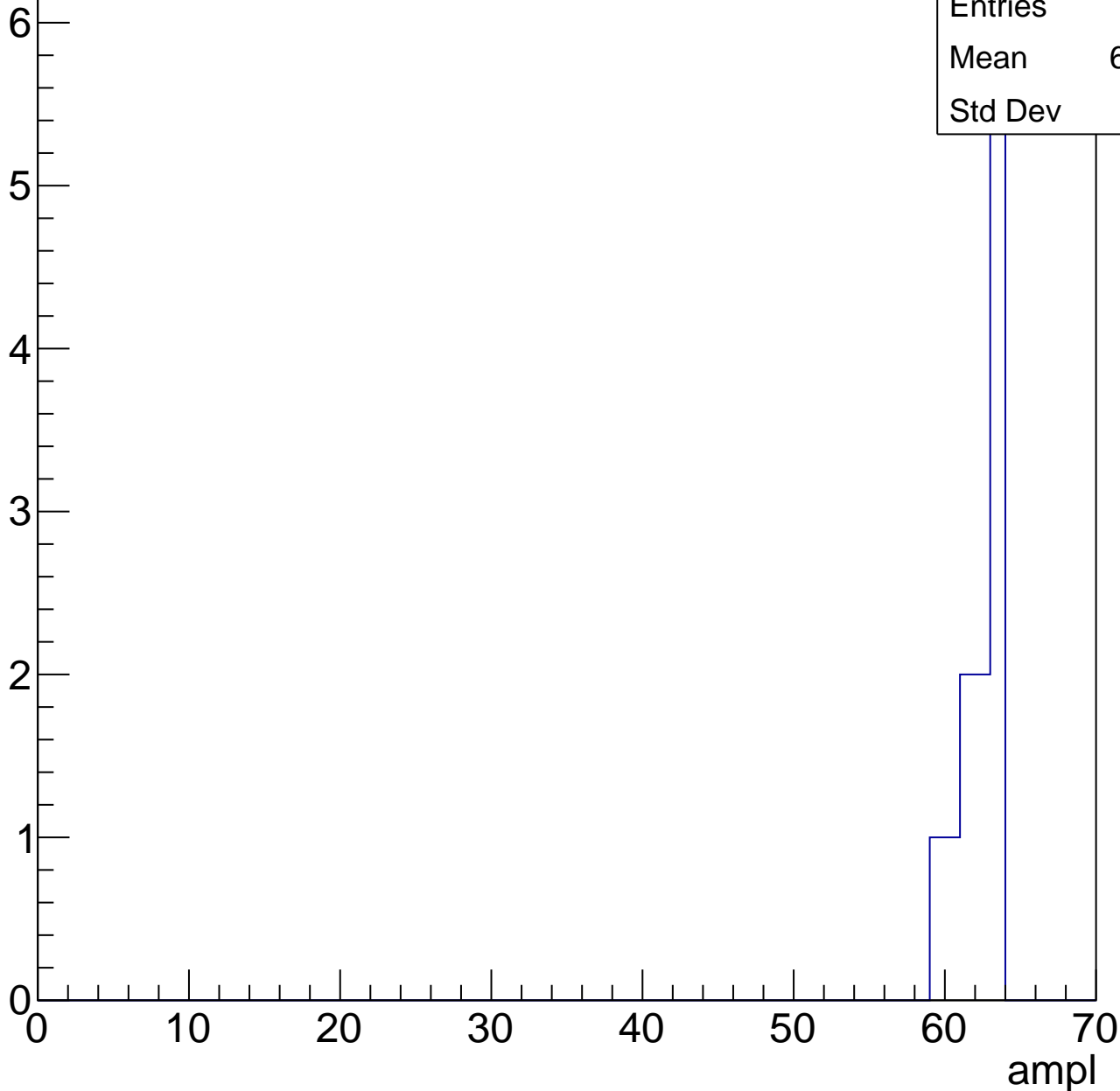


# B1L003S, U26-ch56, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	12
Mean	61.92
Std Dev	1.32

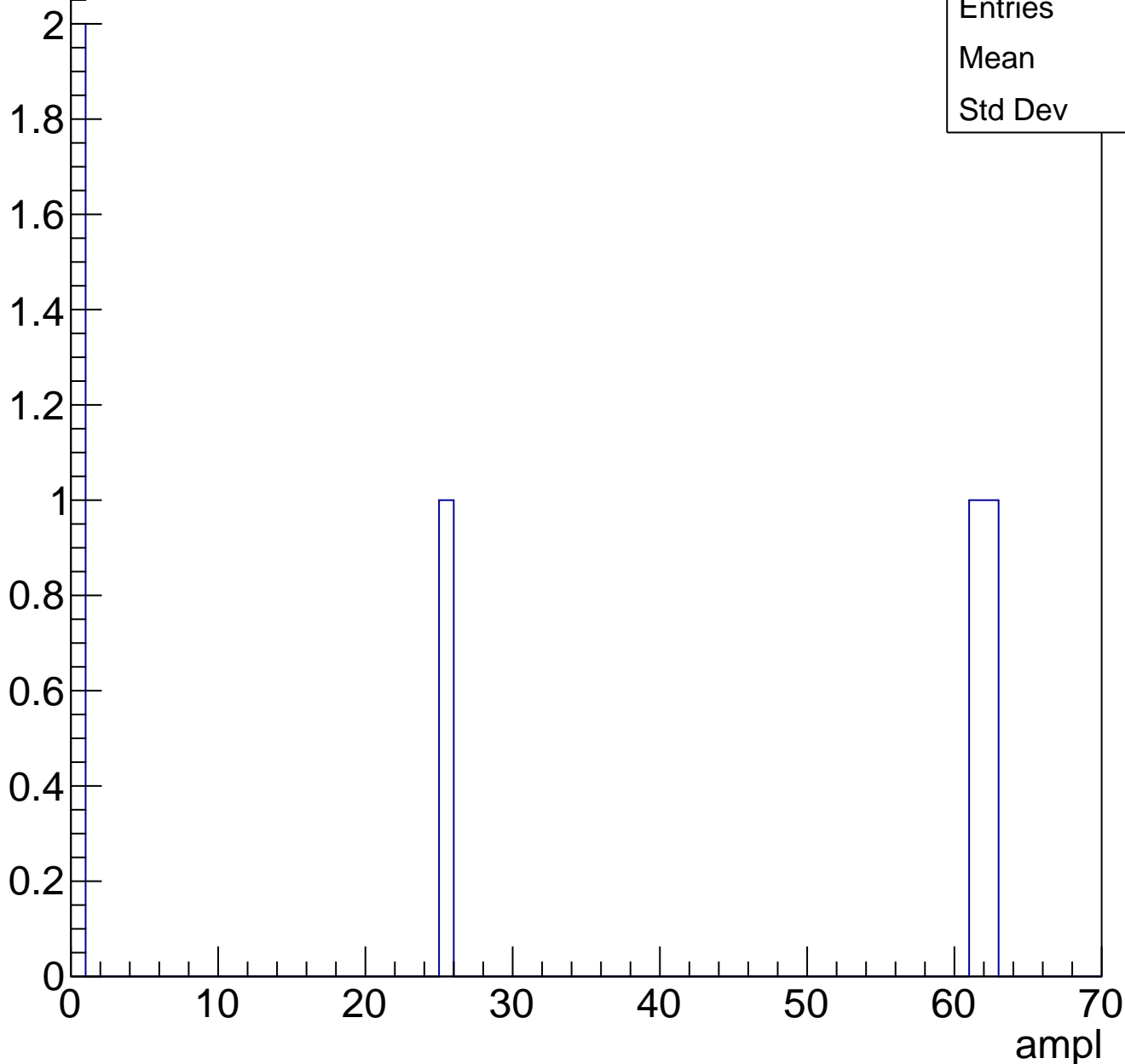




# B1L003S, U26-ch56, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	5
Mean	29.6
Std Dev	27.6

# B1L003S, U26-ch57, adc0

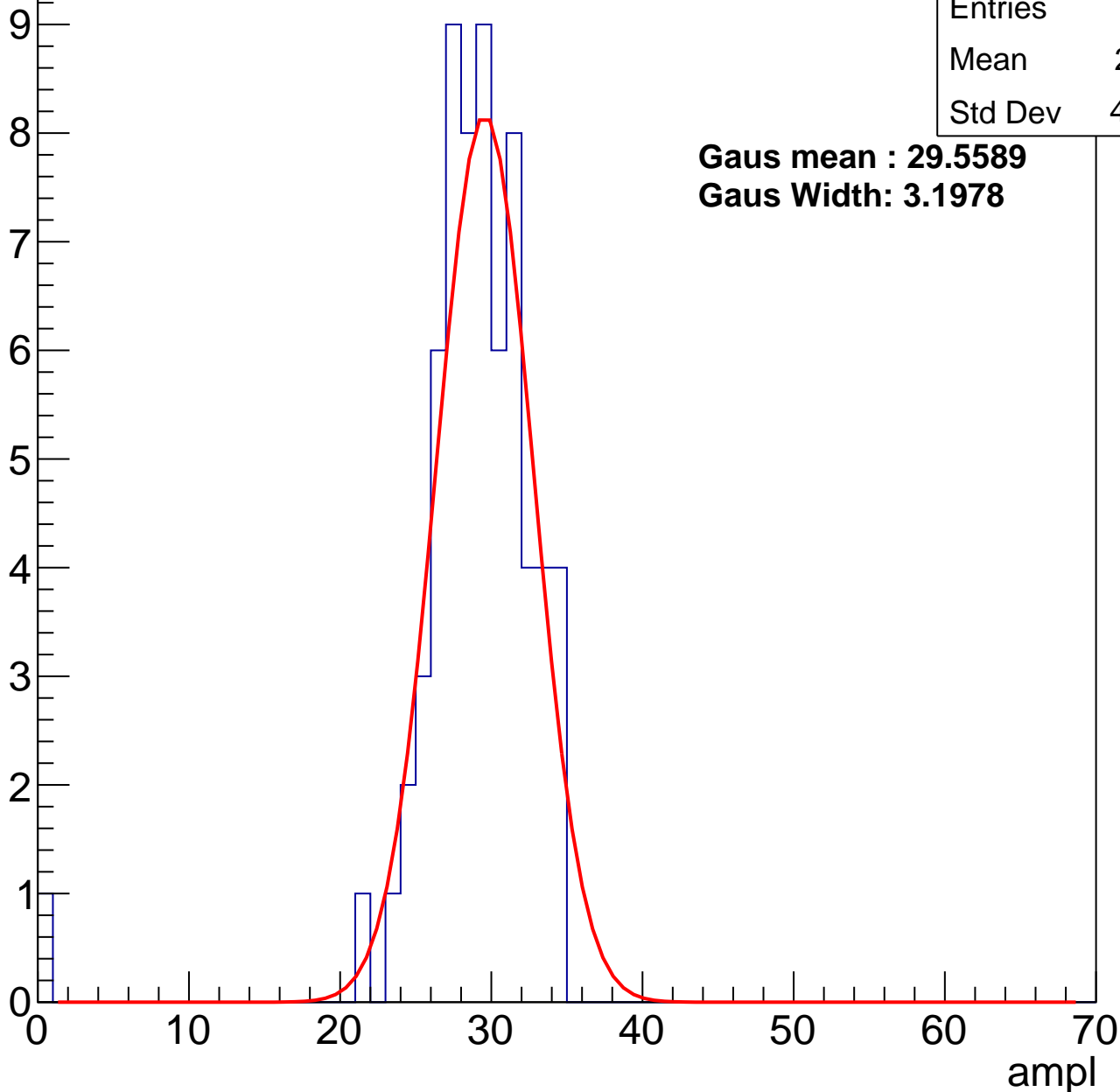
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	28.41
Std Dev	4.526

**Gaus mean : 29.5589**

**Gaus Width: 3.1978**



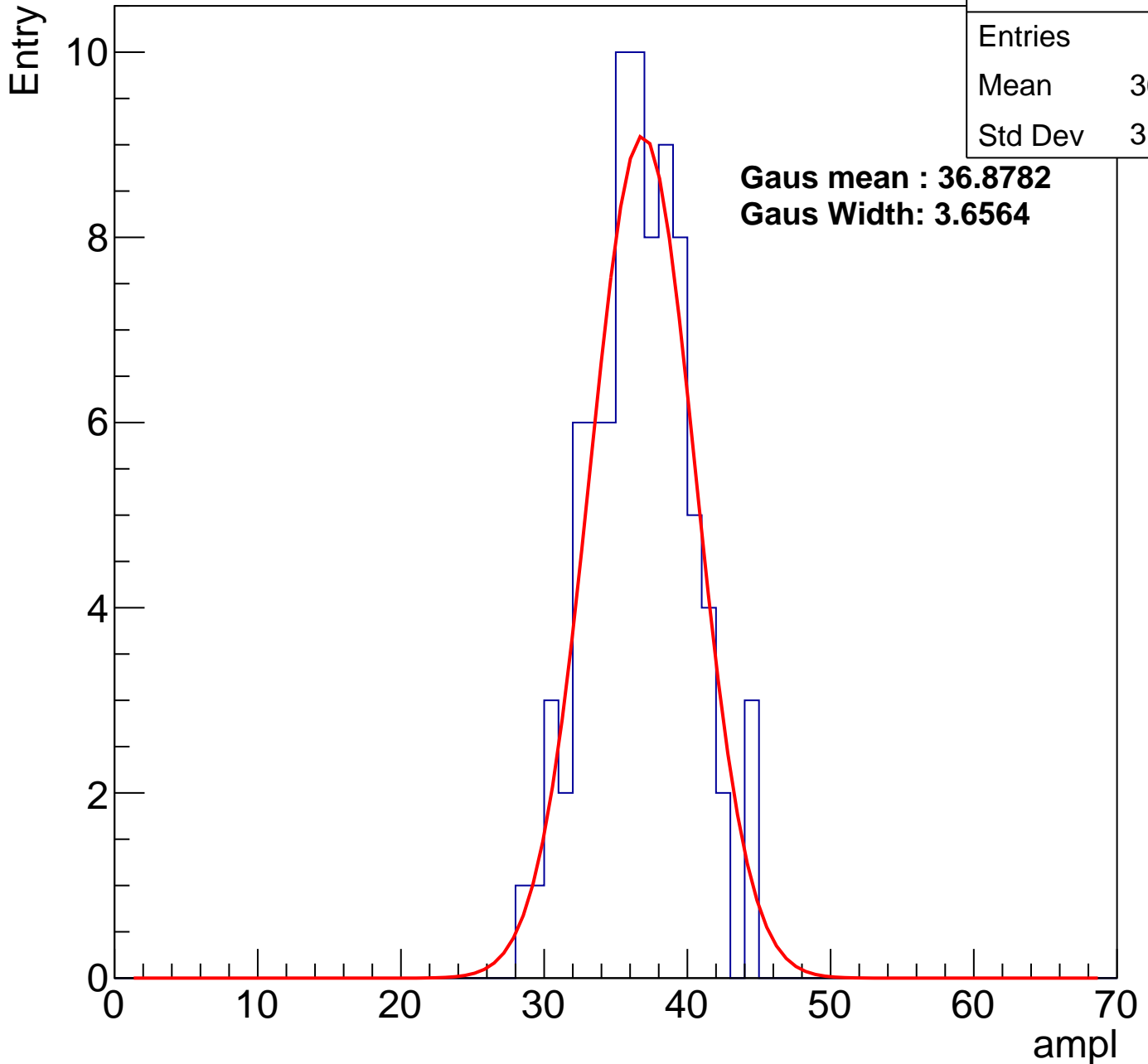
# B1L003S, U26-ch57, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	84
Mean	36.23
Std Dev	3.469

**Gaus mean : 36.8782**

**Gaus Width: 3.6564**



# B1L003S, U26-ch57, adc2

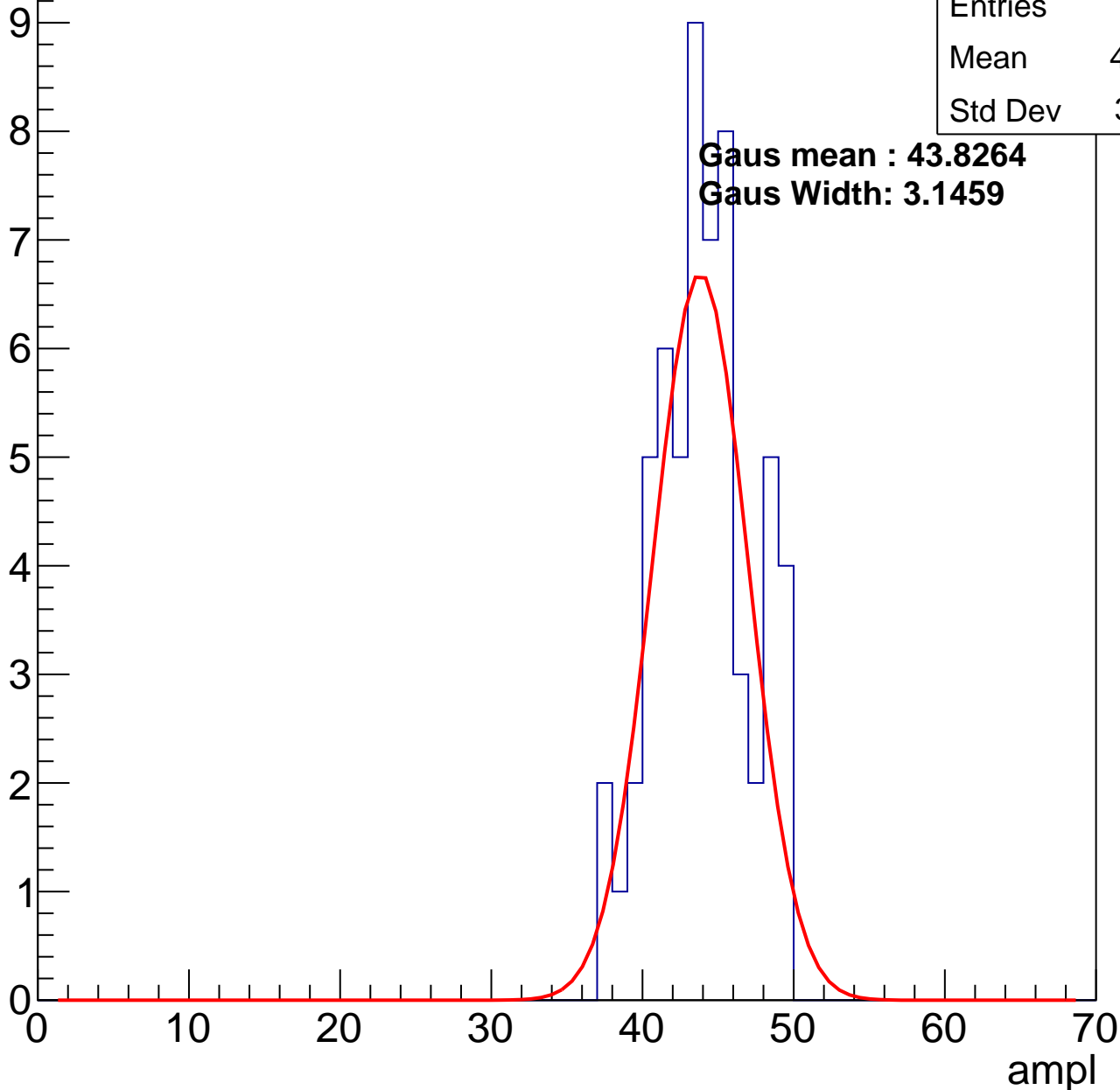
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	43.54
Std Dev	3.061

**Gaus mean : 43.8264**

**Gaus Width: 3.1459**

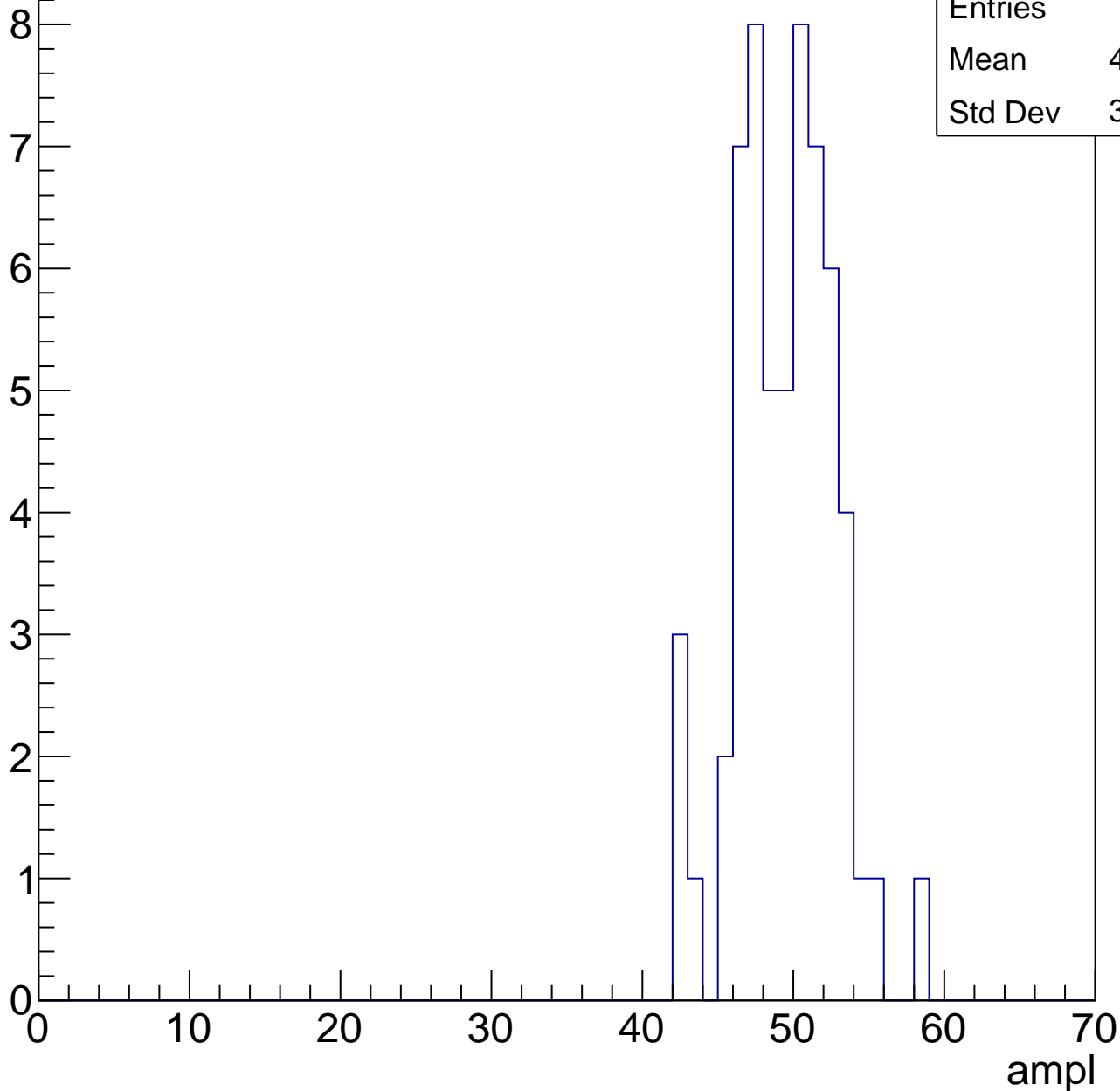


# B1L003S, U26-ch57, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

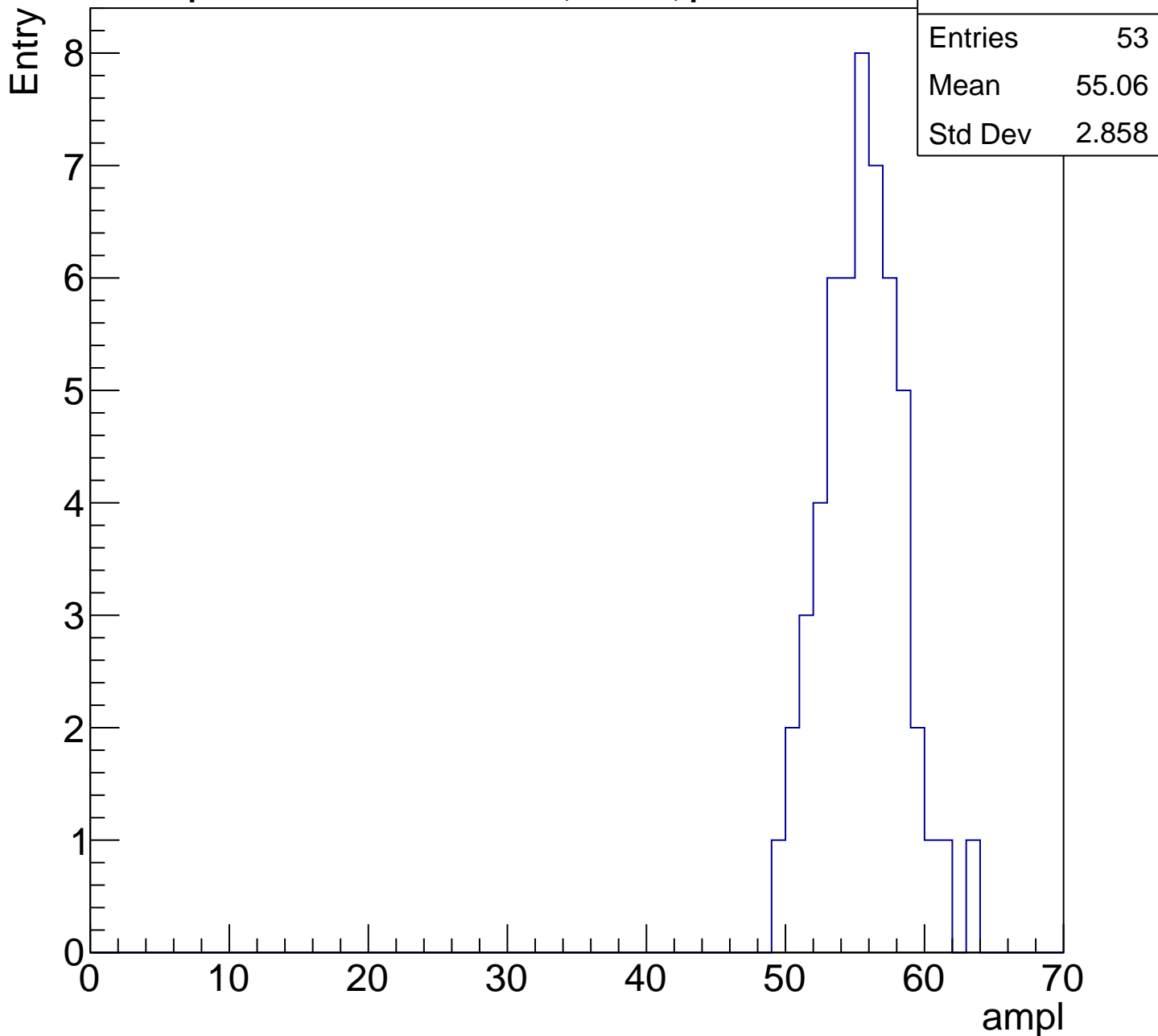
Entry

Entries	59
Mean	48.98
Std Dev	3.218



# B1L003S, U26-ch57, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2



# B1L003S, U26-ch57, adc5

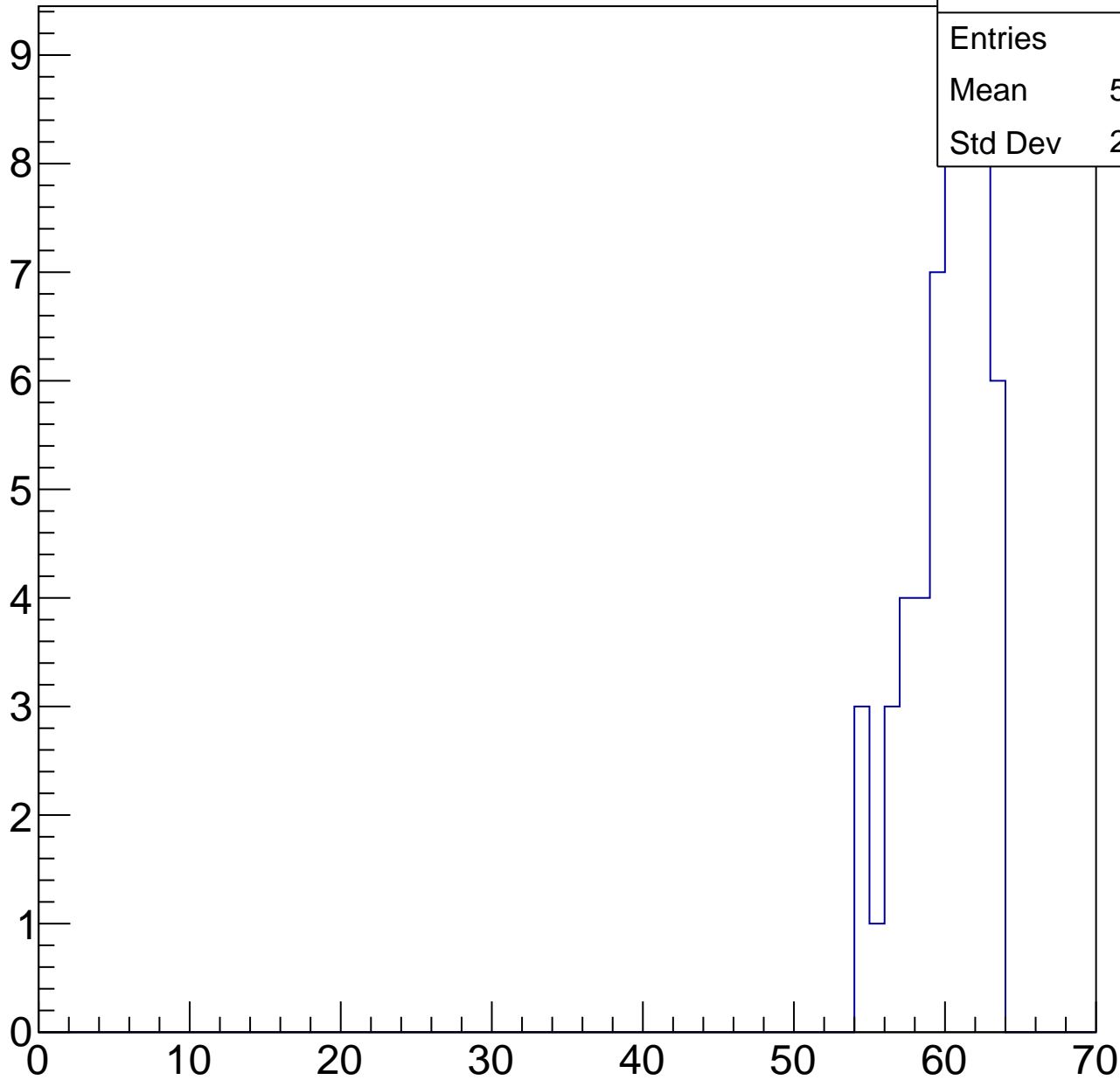
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	55
Mean	59.69
Std Dev	2.463

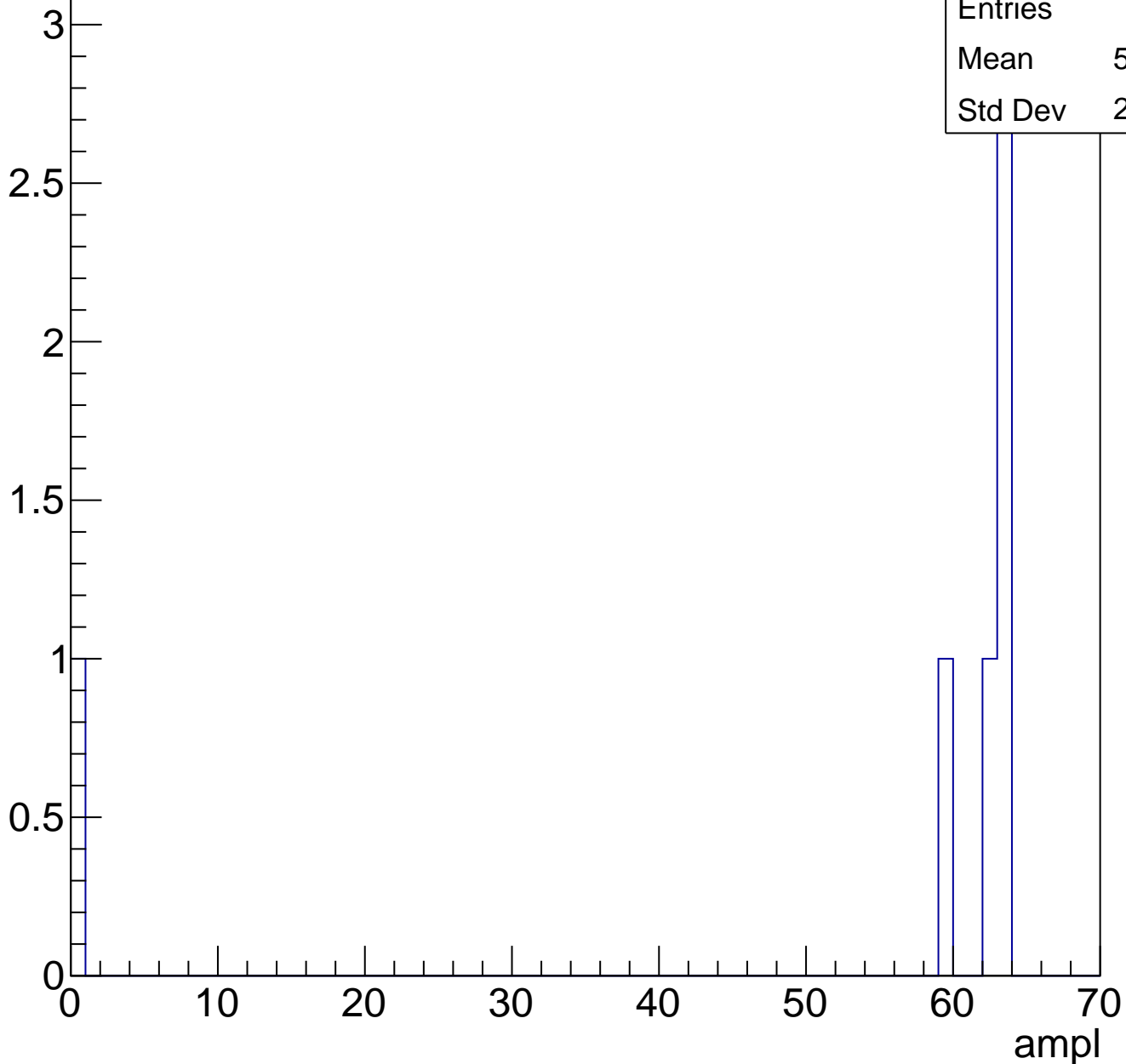
ampl



# B1L003S, U26-ch57, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch57, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	20
Std Dev	0

ampl

# B1L003S, U26-ch58, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	64
Mean	27.52
Std Dev	4.462

**Gaus mean : 28.3943**

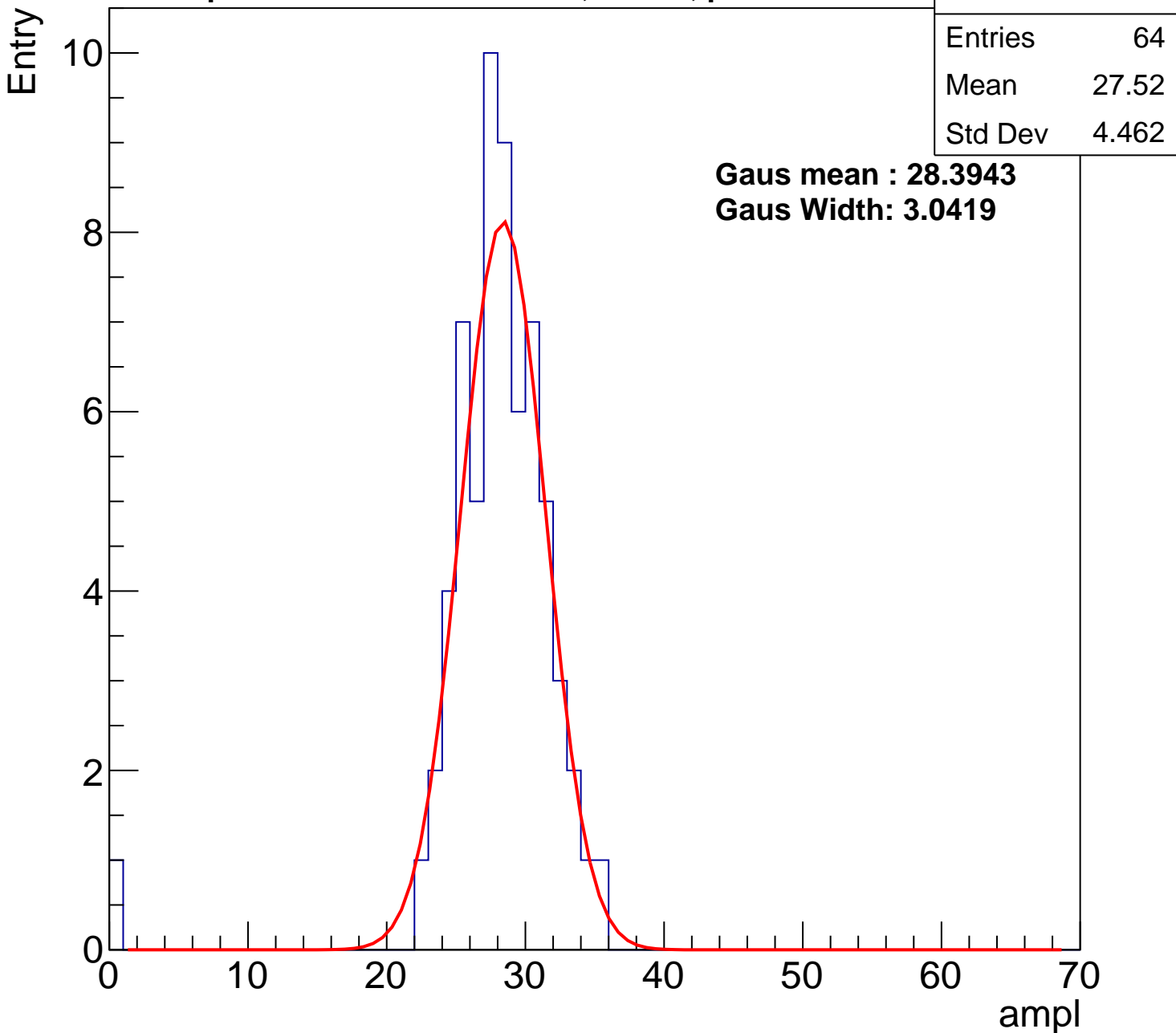
**Gaus Width: 3.0419**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U26-ch58, adc1

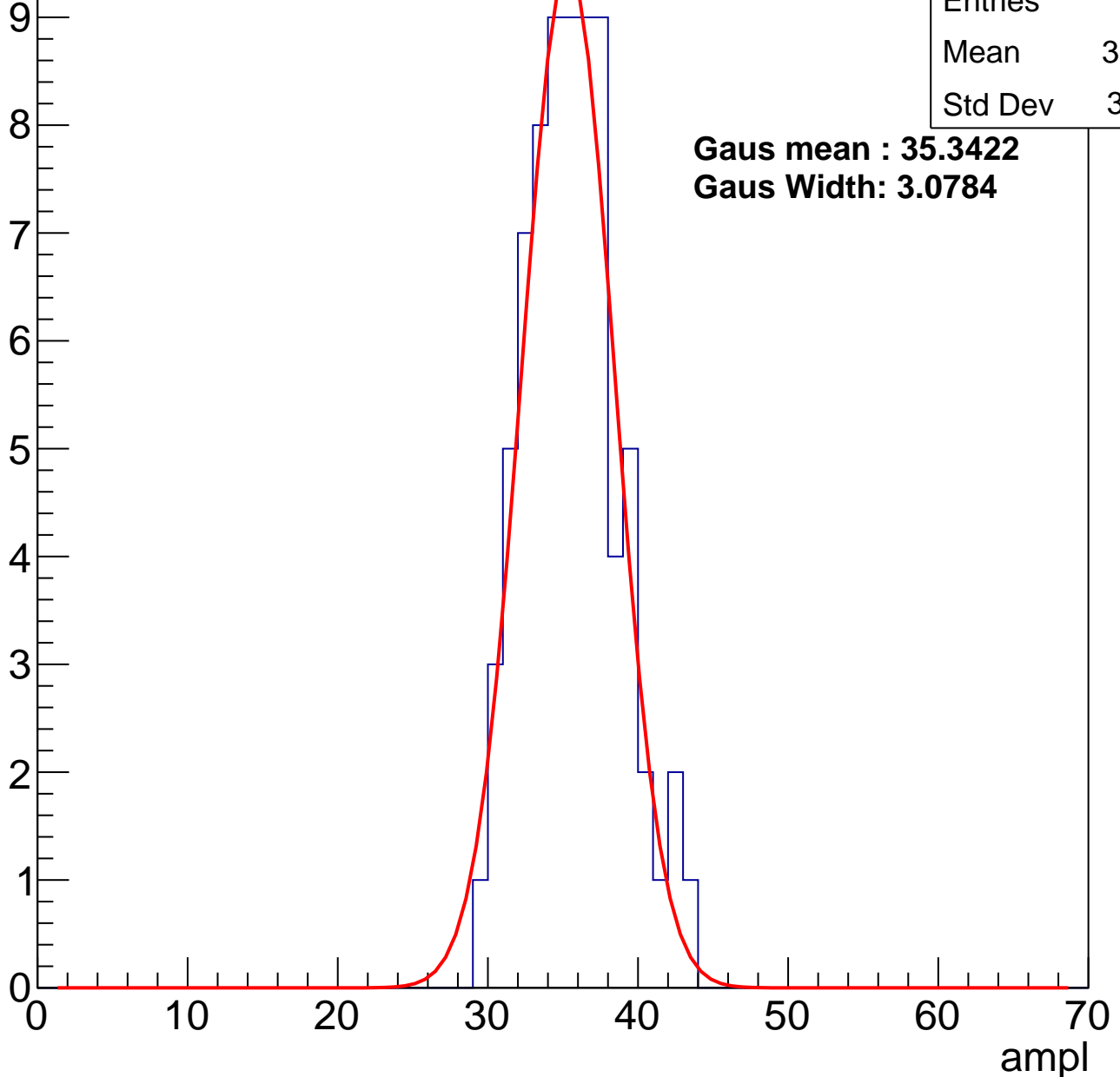
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	75
Mean	35.13
Std Dev	3.061

**Gaus mean : 35.3422**

**Gaus Width: 3.0784**



# B1L003S, U26-ch58, adc2

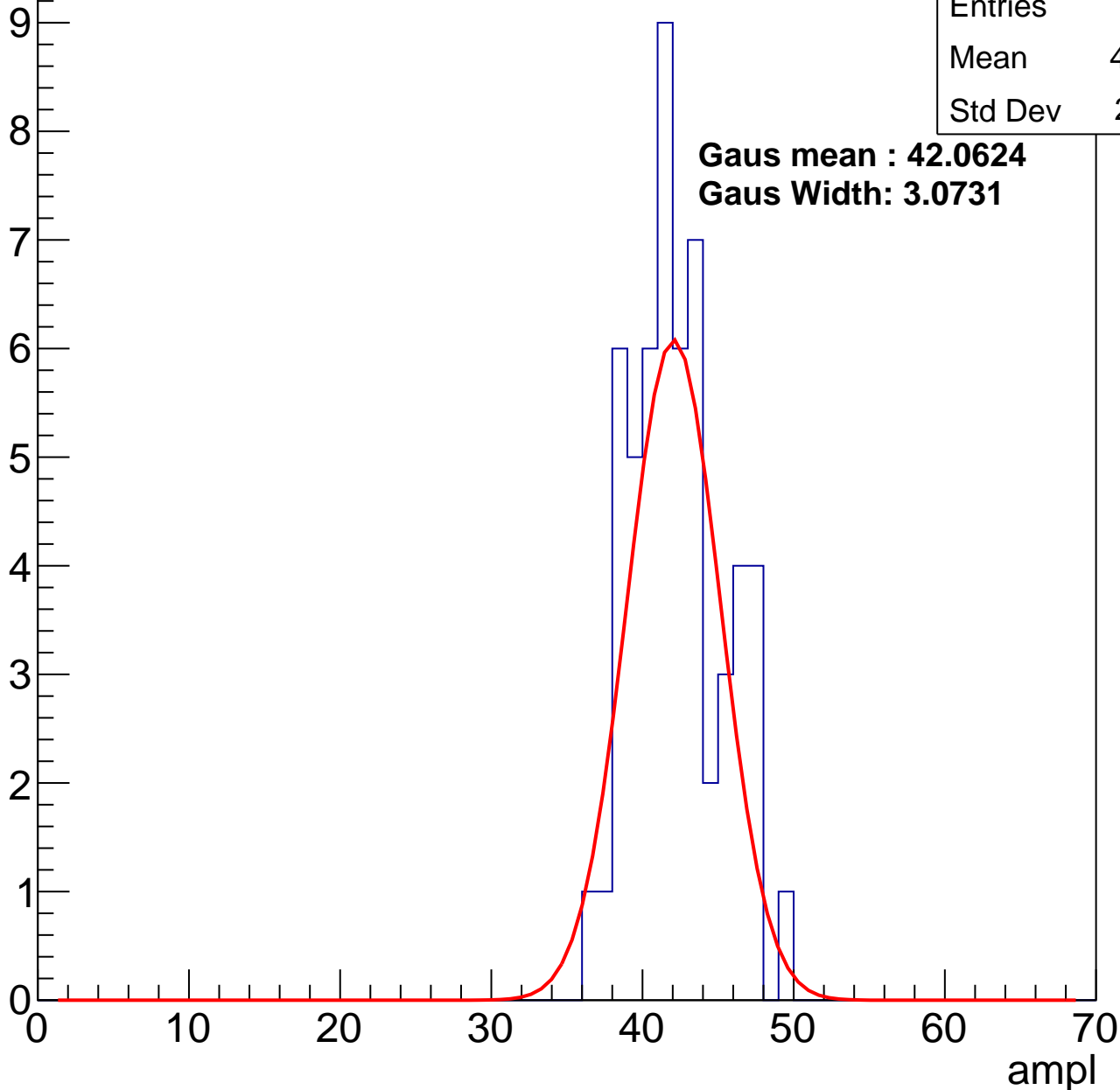
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	41.85
Std Dev	2.981

**Gaus mean : 42.0624**

**Gaus Width: 3.0731**



# B1L003S, U26-ch58, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

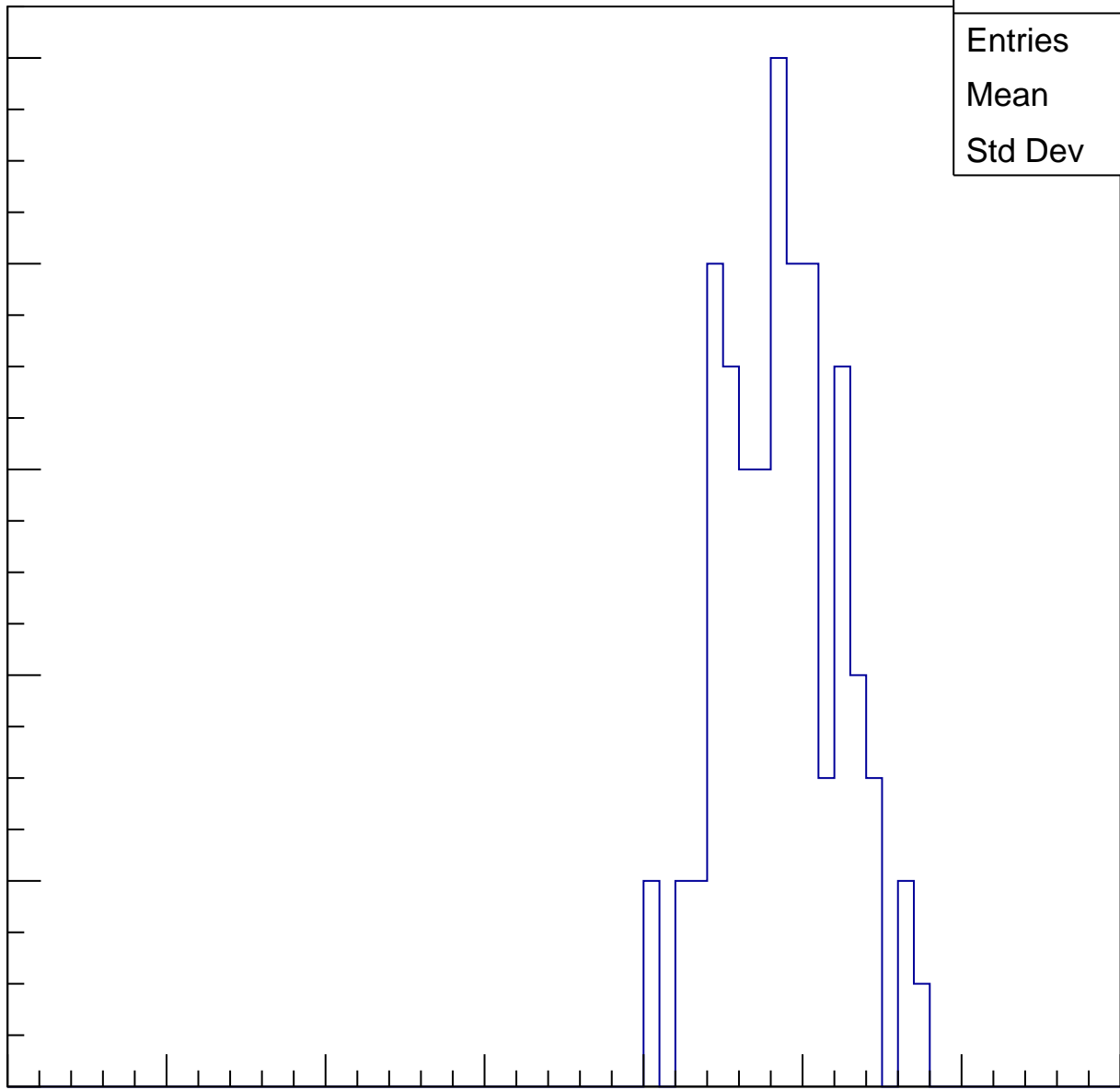
Entries	79
Mean	48.19
Std Dev	3.67

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

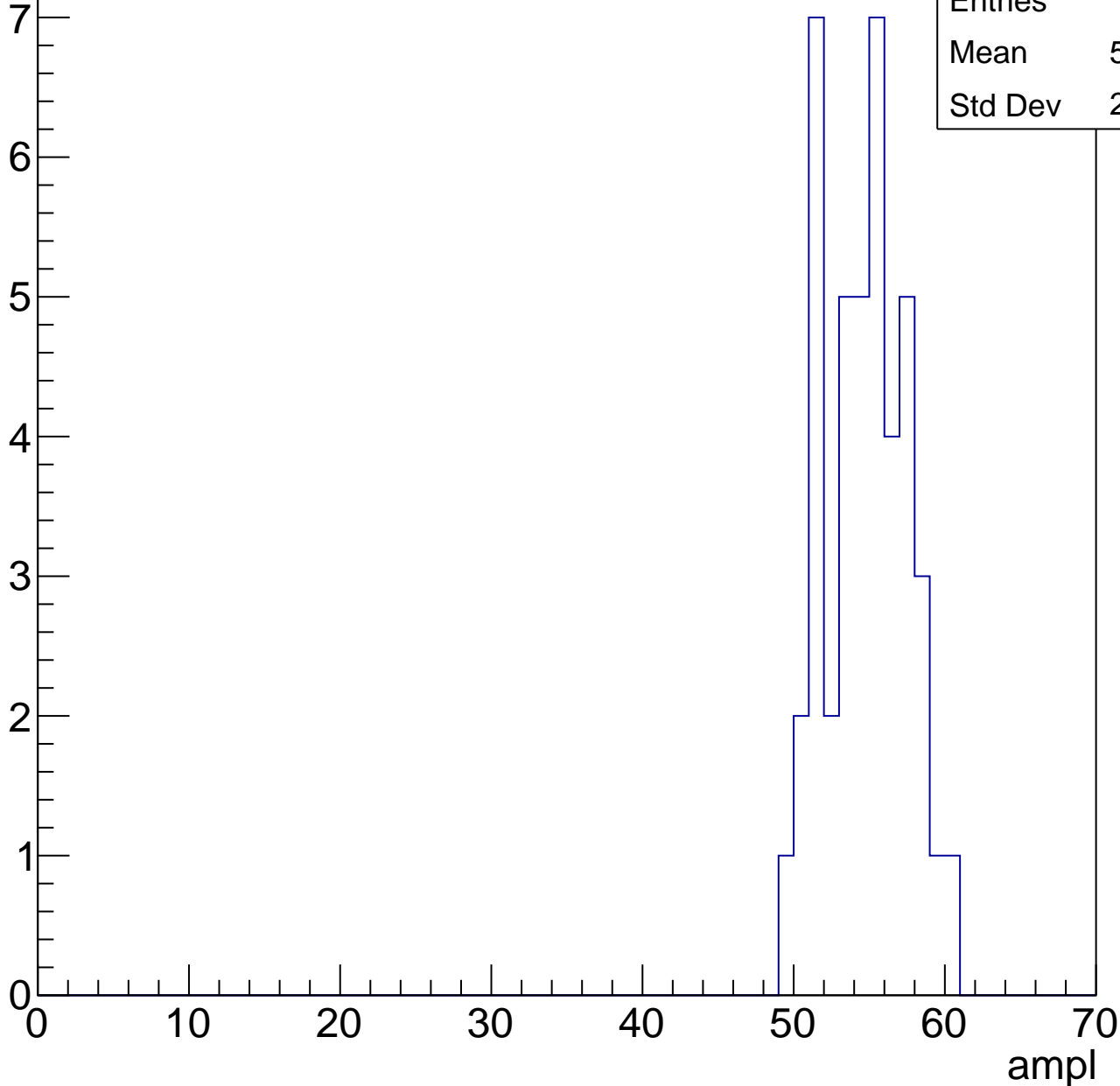


# B1L003S, U26-ch58, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	43
Mean	54.23
Std Dev	2.675



# B1L003S, U26-ch58, adc5

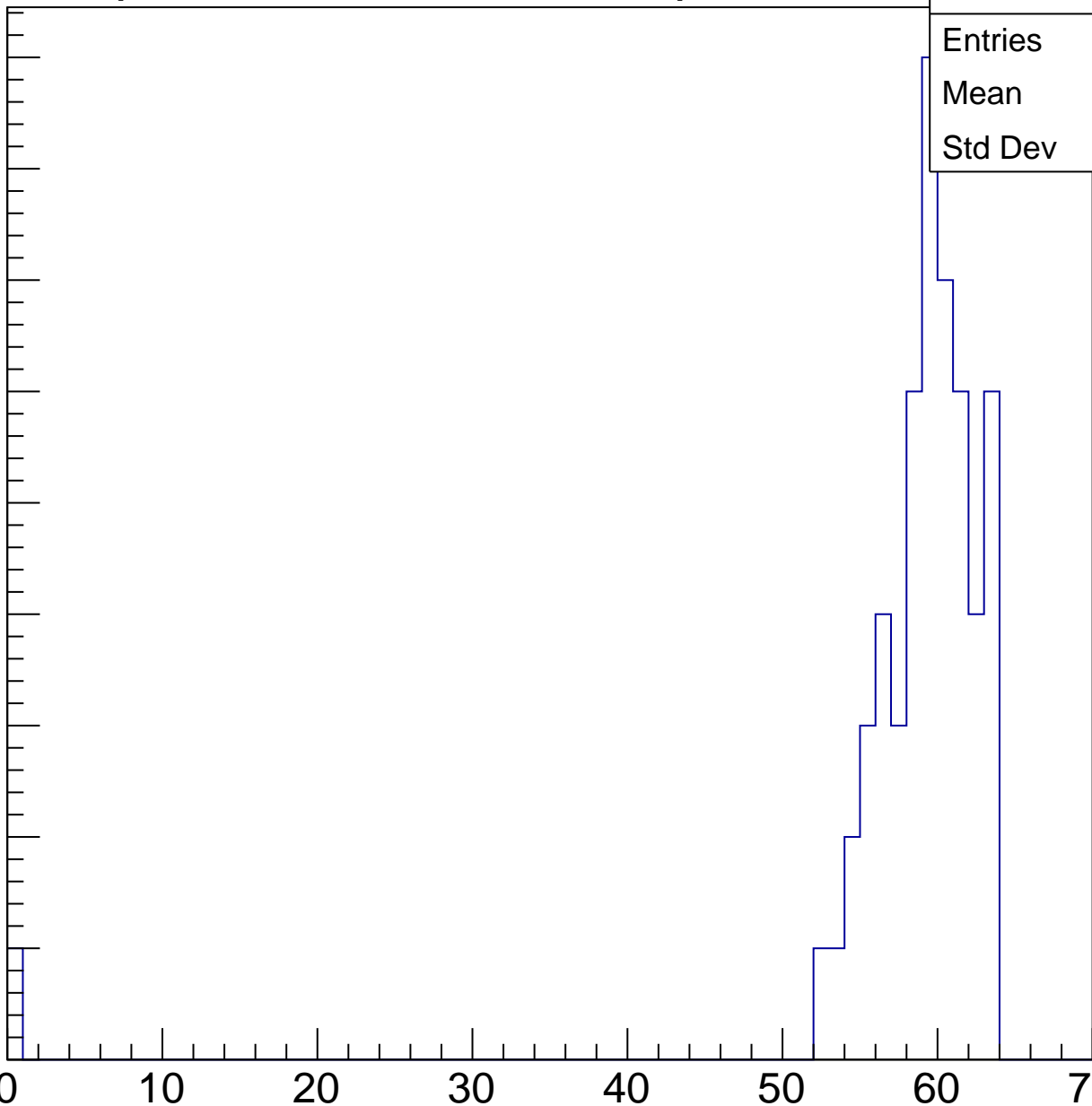
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	53
Mean	57.81
Std Dev	8.474

ampl

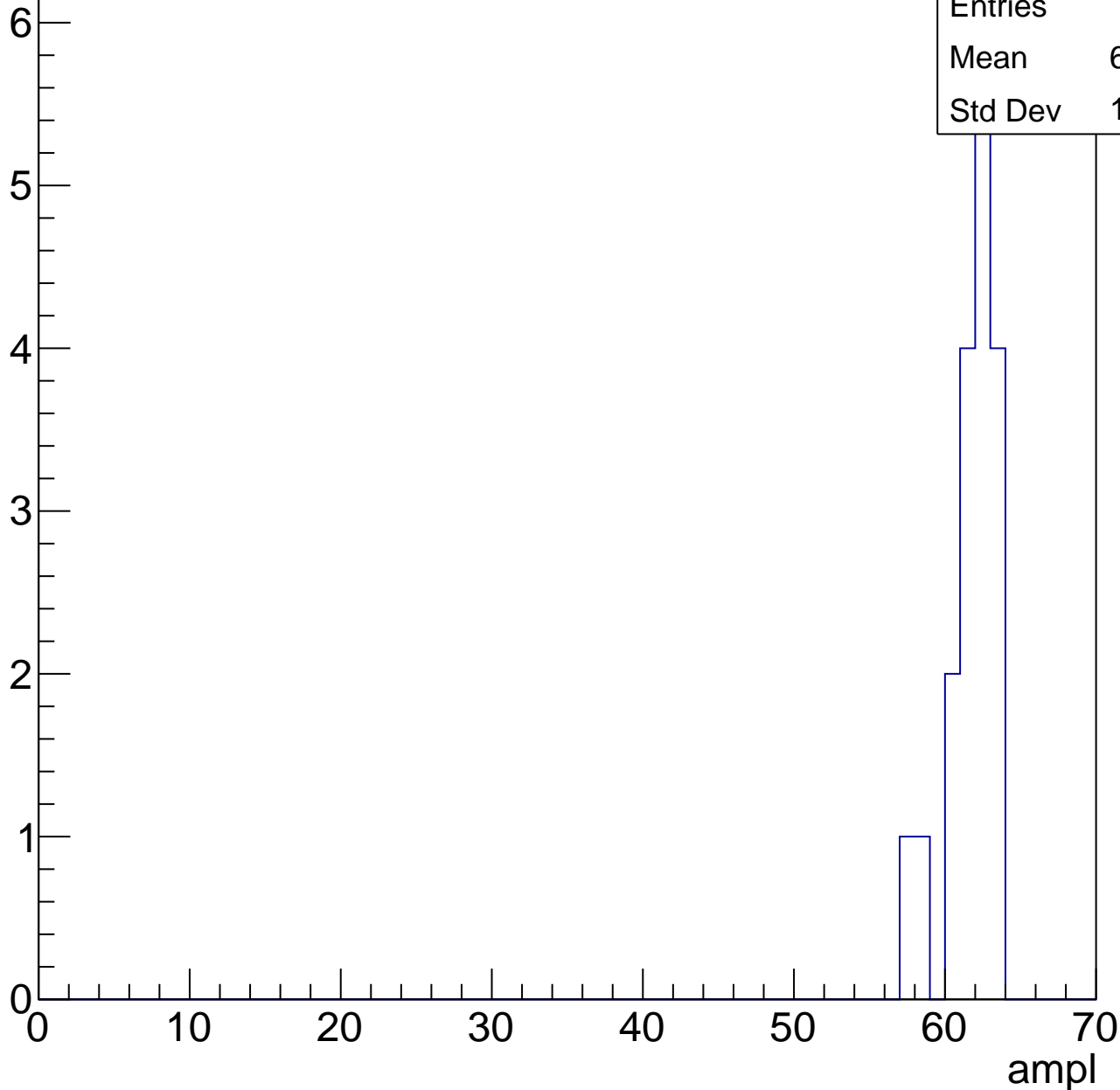


# B1L003S, U26-ch58, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	18
Mean	61.28
Std Dev	1.626





# B1L003S, U26-ch58, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U26-ch59, adc0

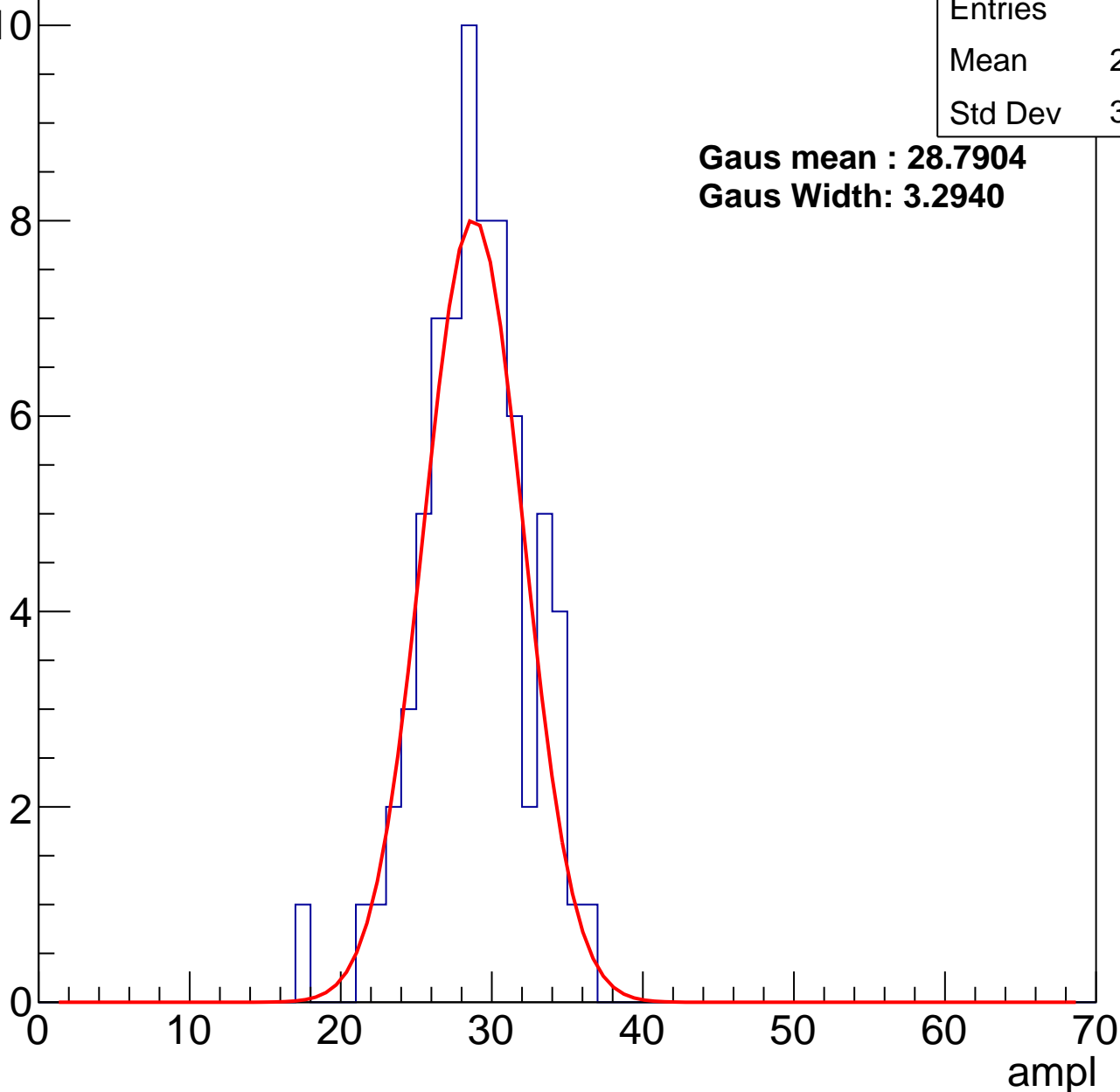
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	72
Mean	28.44
Std Dev	3.492

**Gaus mean : 28.7904**

**Gaus Width: 3.2940**



# B1L003S, U26-ch59, adc1

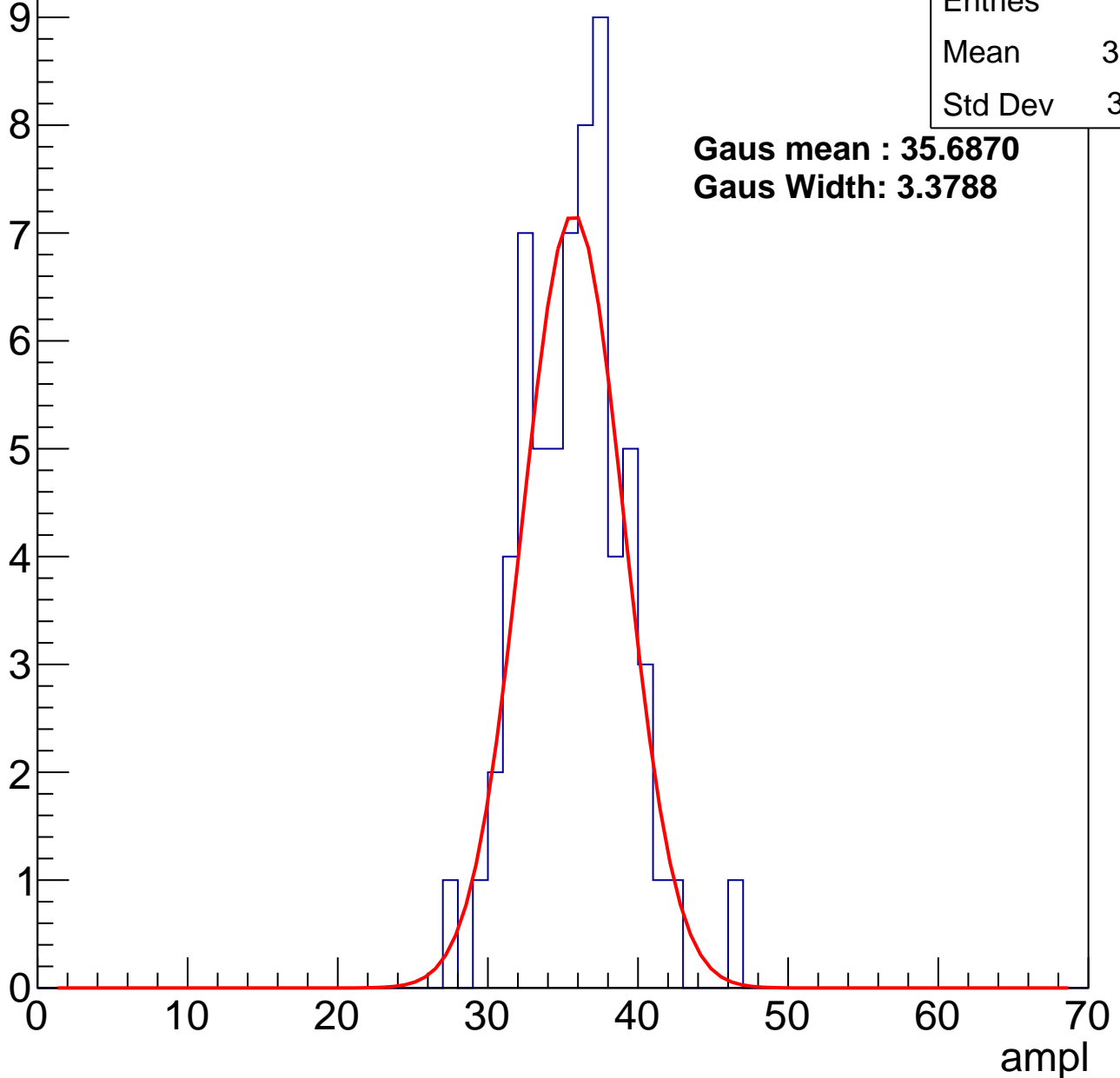
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	35.33
Std Dev	3.391

**Gaus mean : 35.6870**

**Gaus Width: 3.3788**



# B1L003S, U26-ch59, adc2

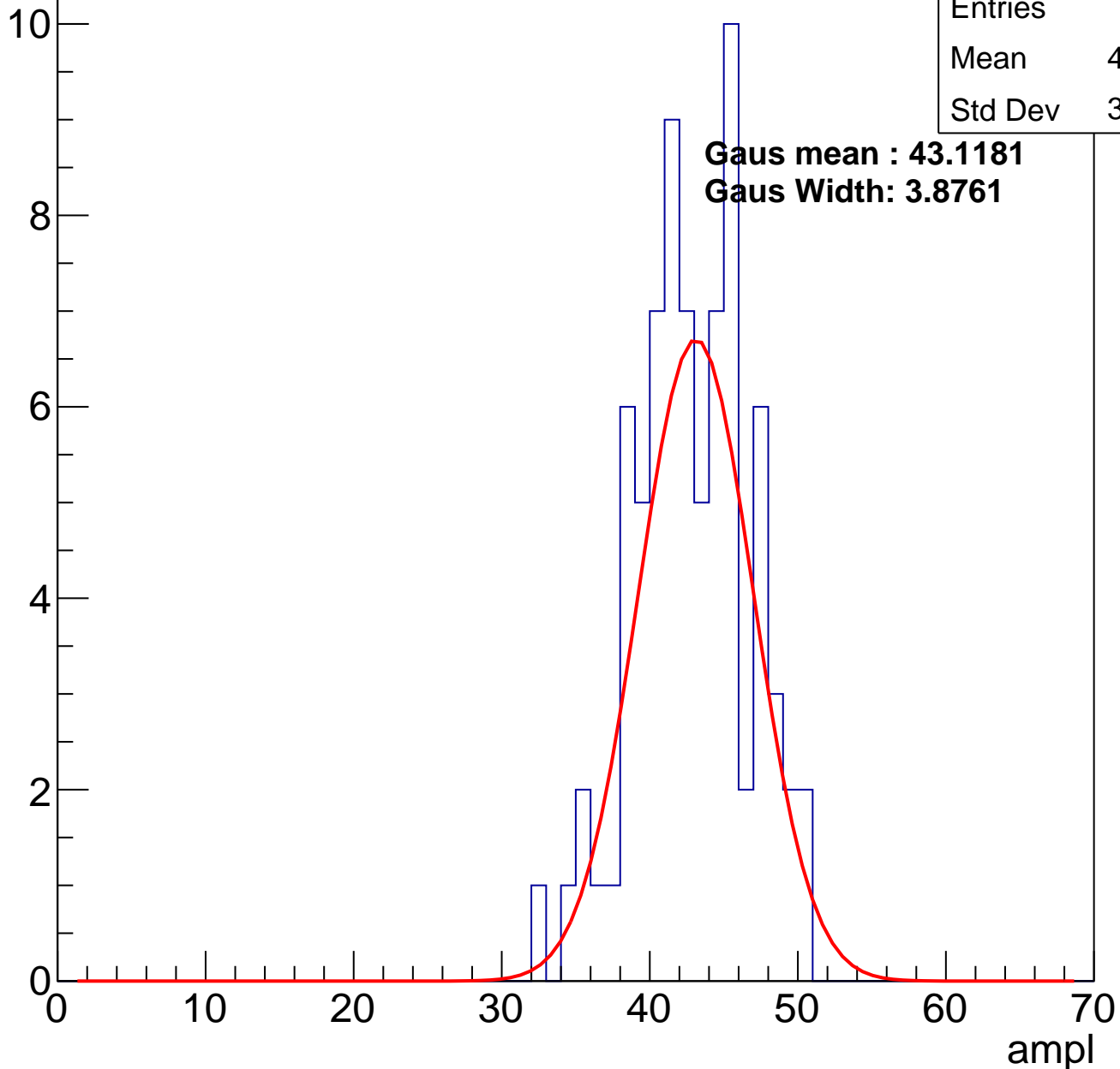
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	77
Mean	42.39
Std Dev	3.828

**Gaus mean : 43.1181**

**Gaus Width: 3.8761**

Entry

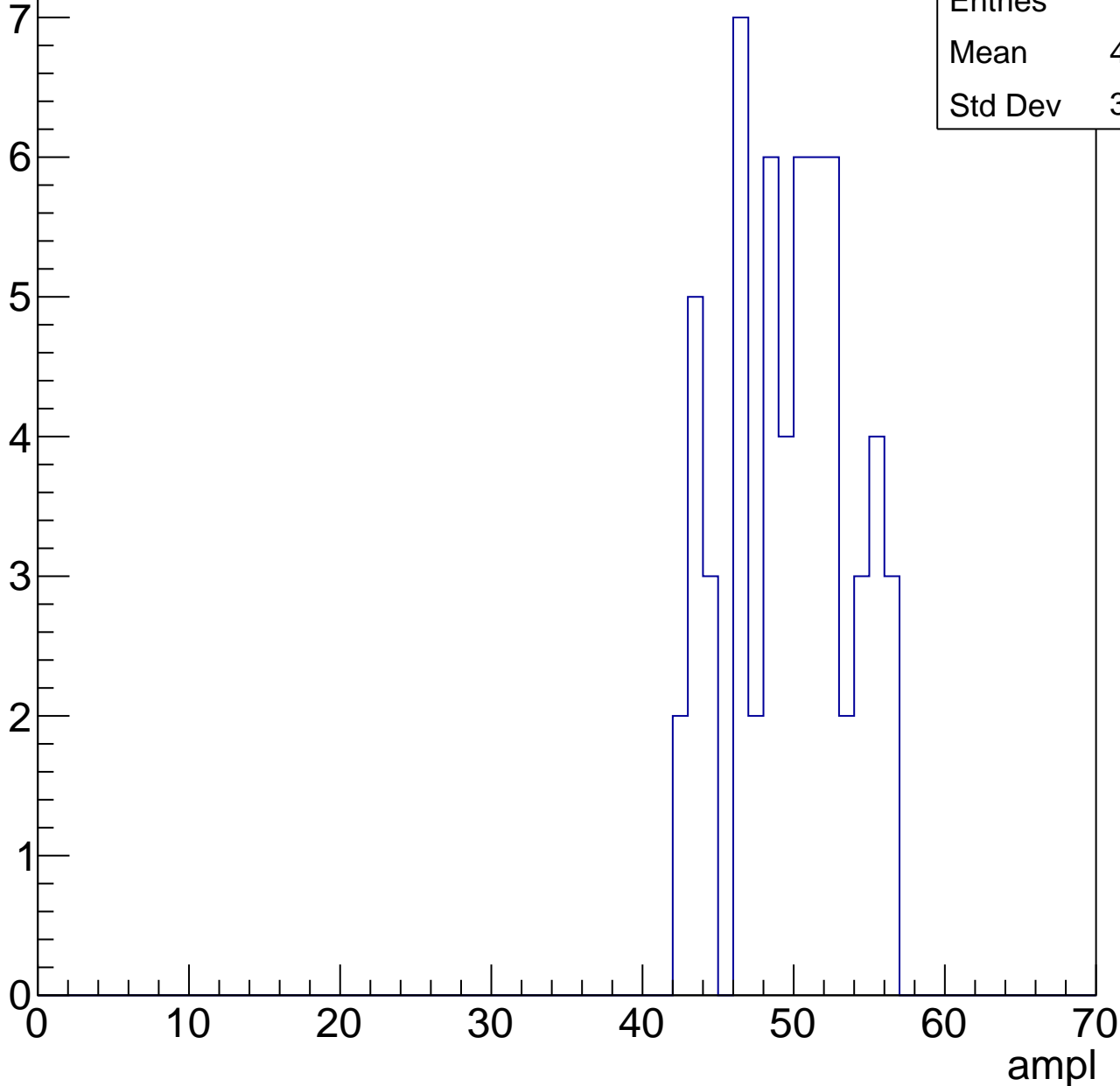


# B1L003S, U26-ch59, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	49.24
Std Dev	3.924

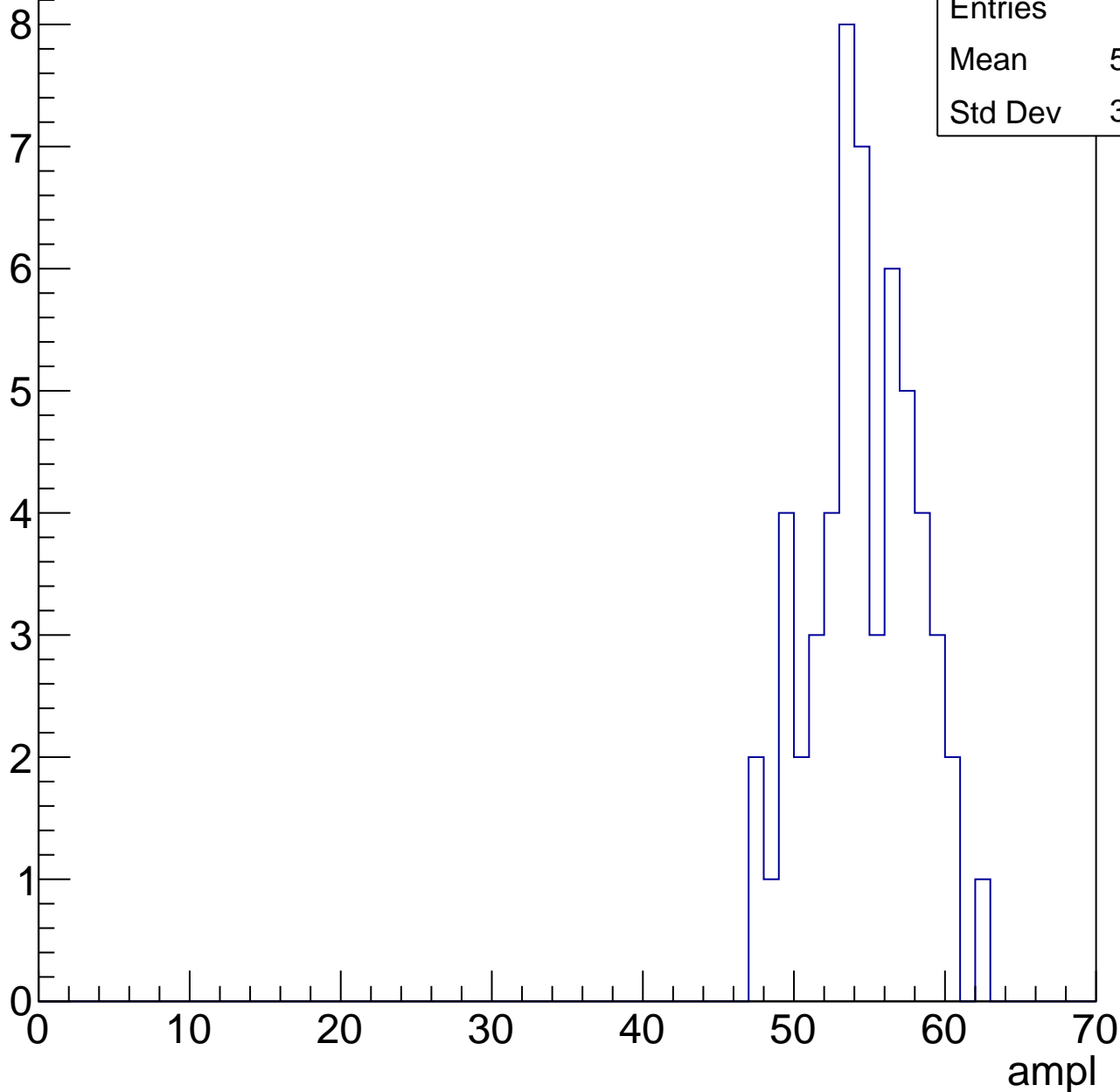


# B1L003S, U26-ch59, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	54.15
Std Dev	3.472



# B1L003S, U26-ch59, adc5

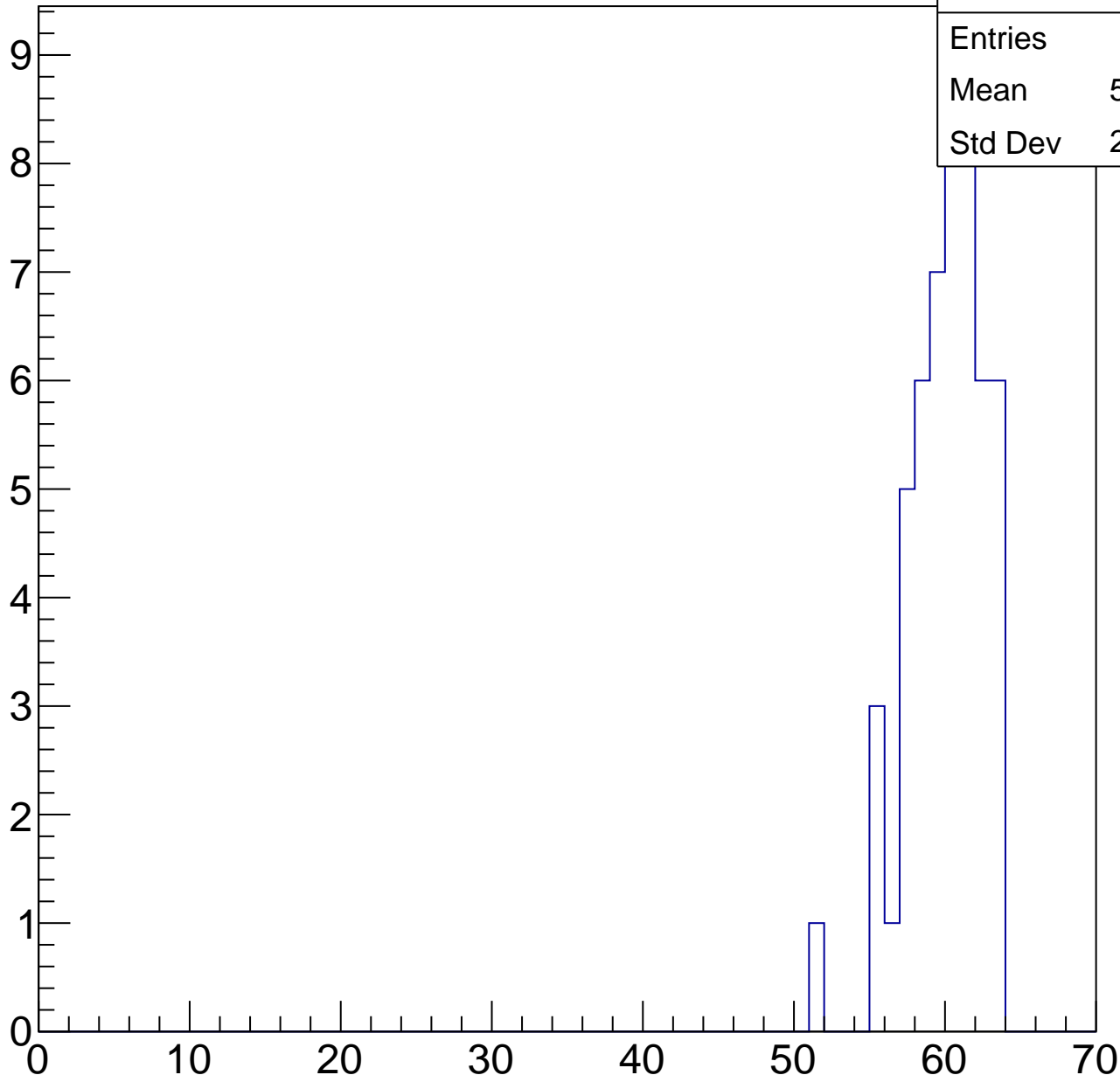
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	52
Mean	59.56
Std Dev	2.499

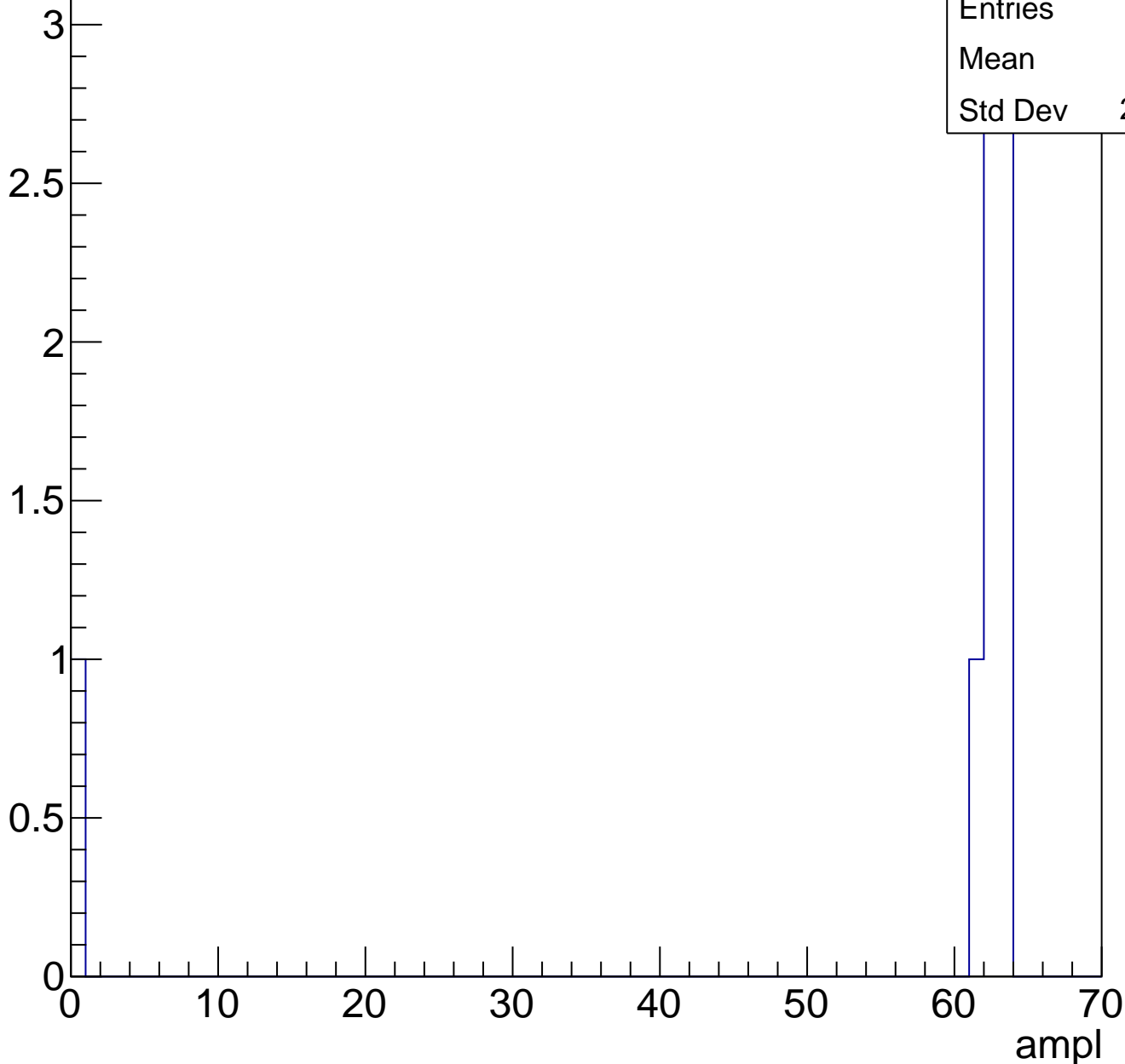
ampl



# B1L003S, U26-ch59, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch59, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U26-ch60, adc0

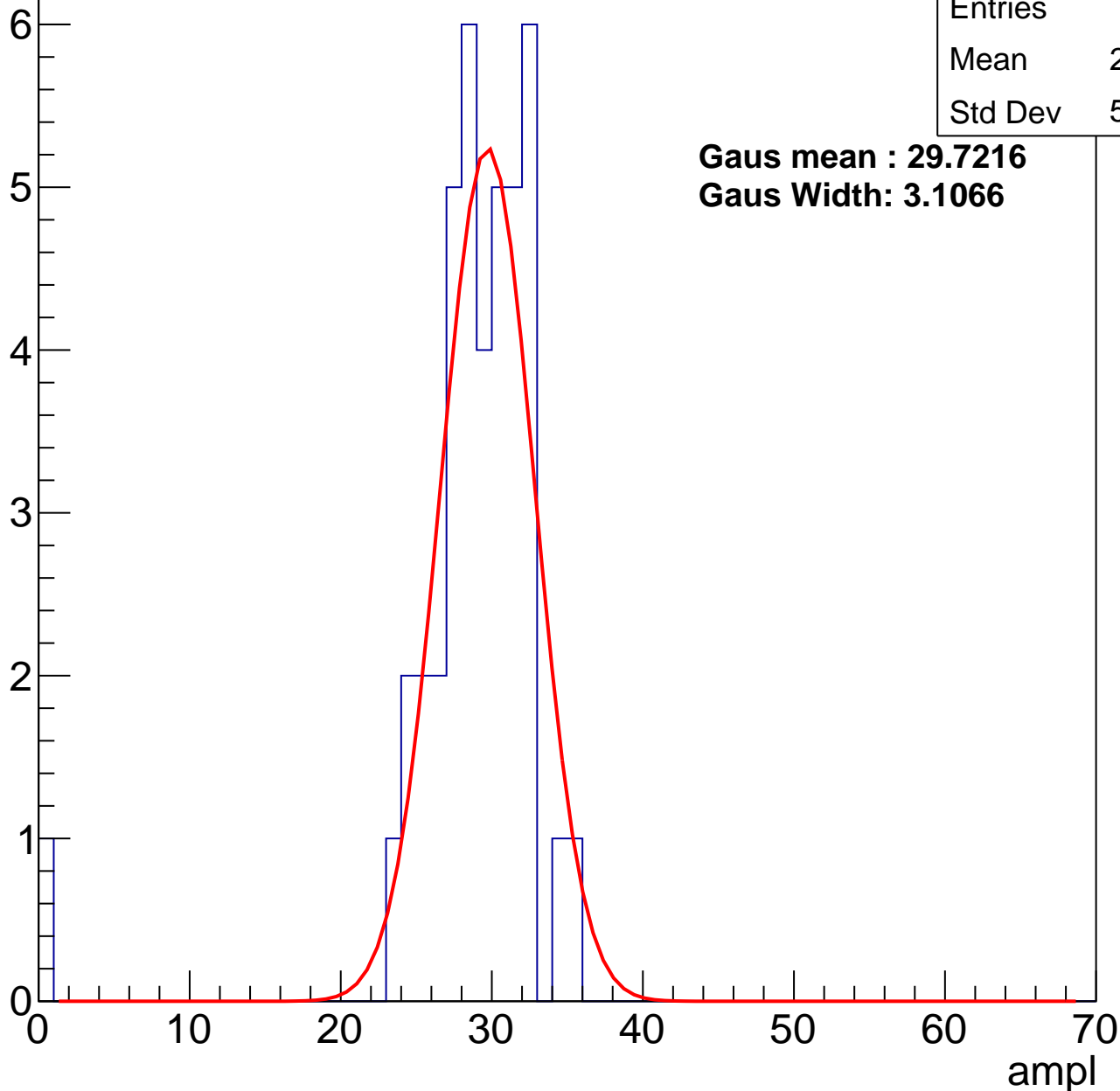
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	41
Mean	28.24
Std Dev	5.226

**Gaus mean : 29.7216**

**Gaus Width: 3.1066**



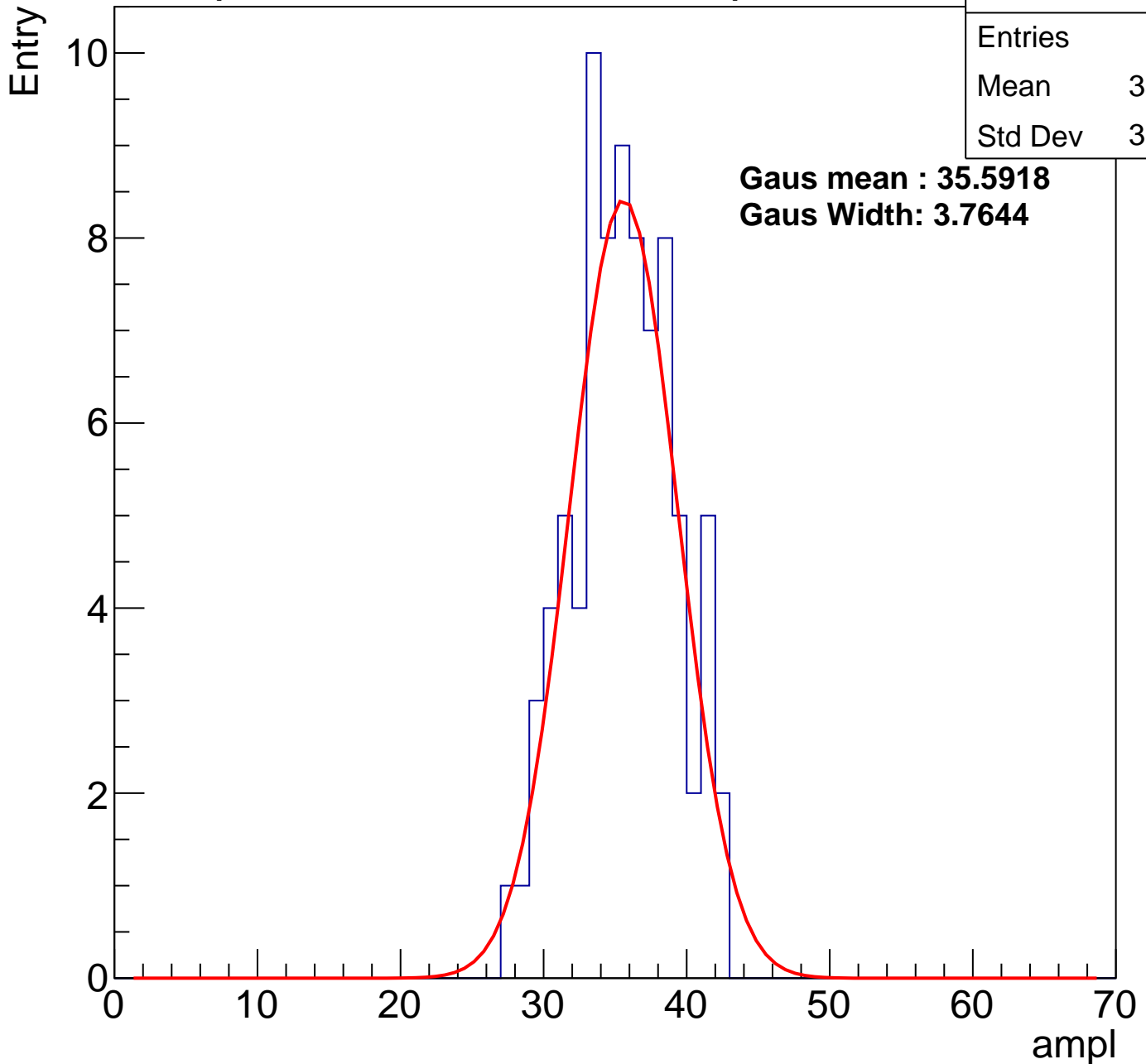
# B1L003S, U26-ch60, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	82
Mean	35.09
Std Dev	3.493

**Gaus mean : 35.5918**

**Gaus Width: 3.7644**



# B1L003S, U26-ch60, adc2

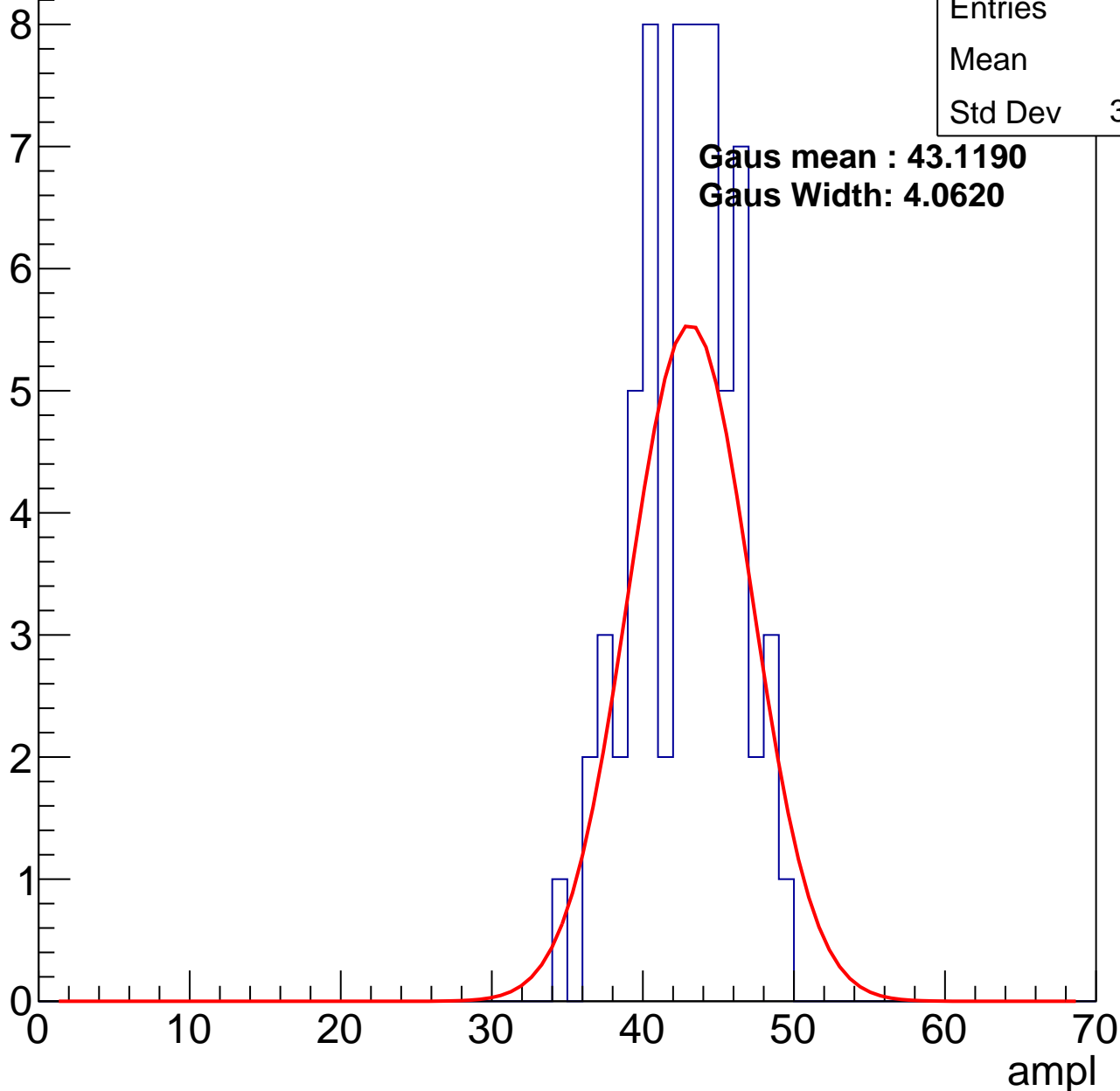
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	42.4
Std Dev	3.318

**Gaus mean : 43.1190**

**Gaus Width: 4.0620**

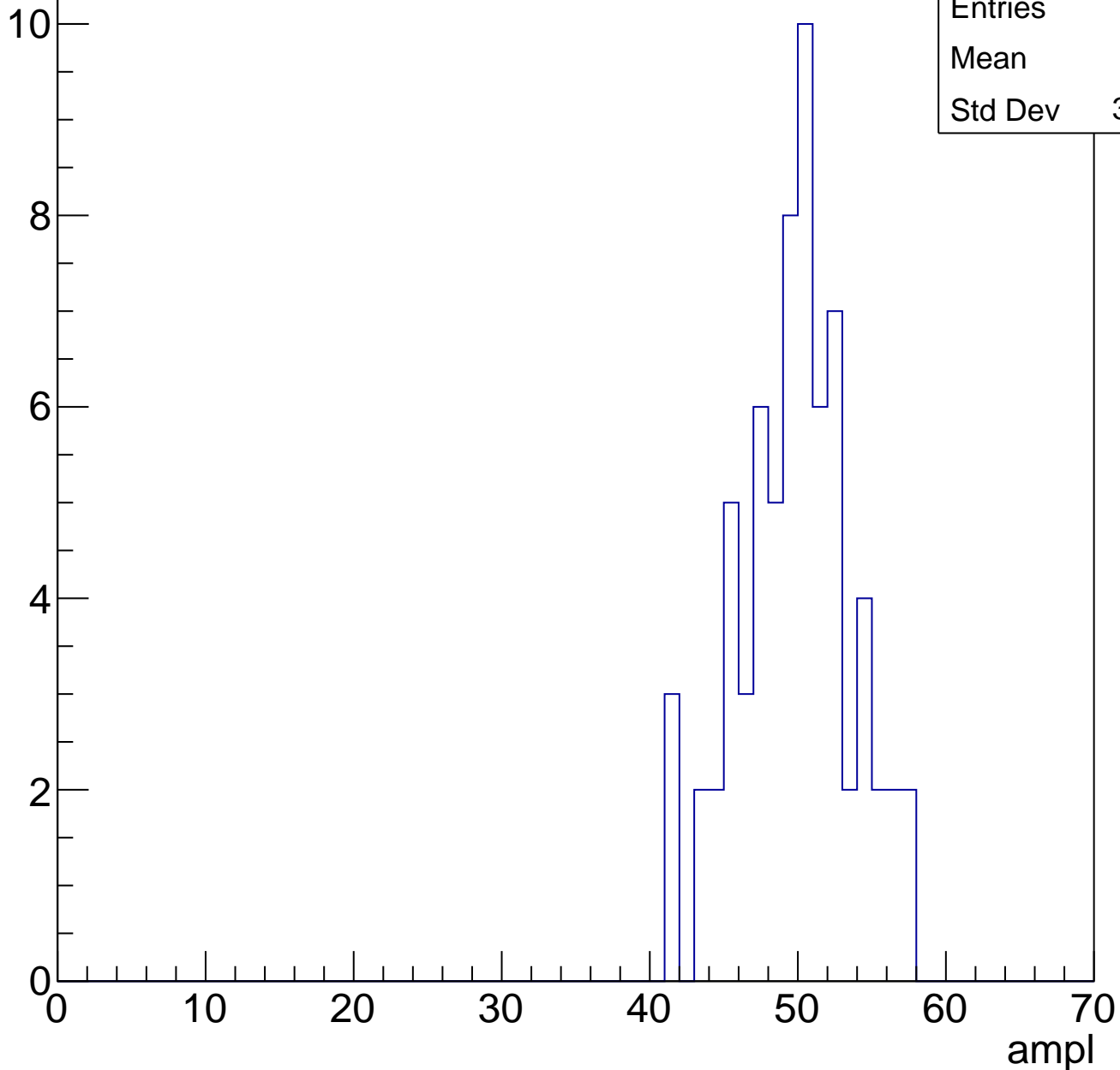


# B1L003S, U26-ch60, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

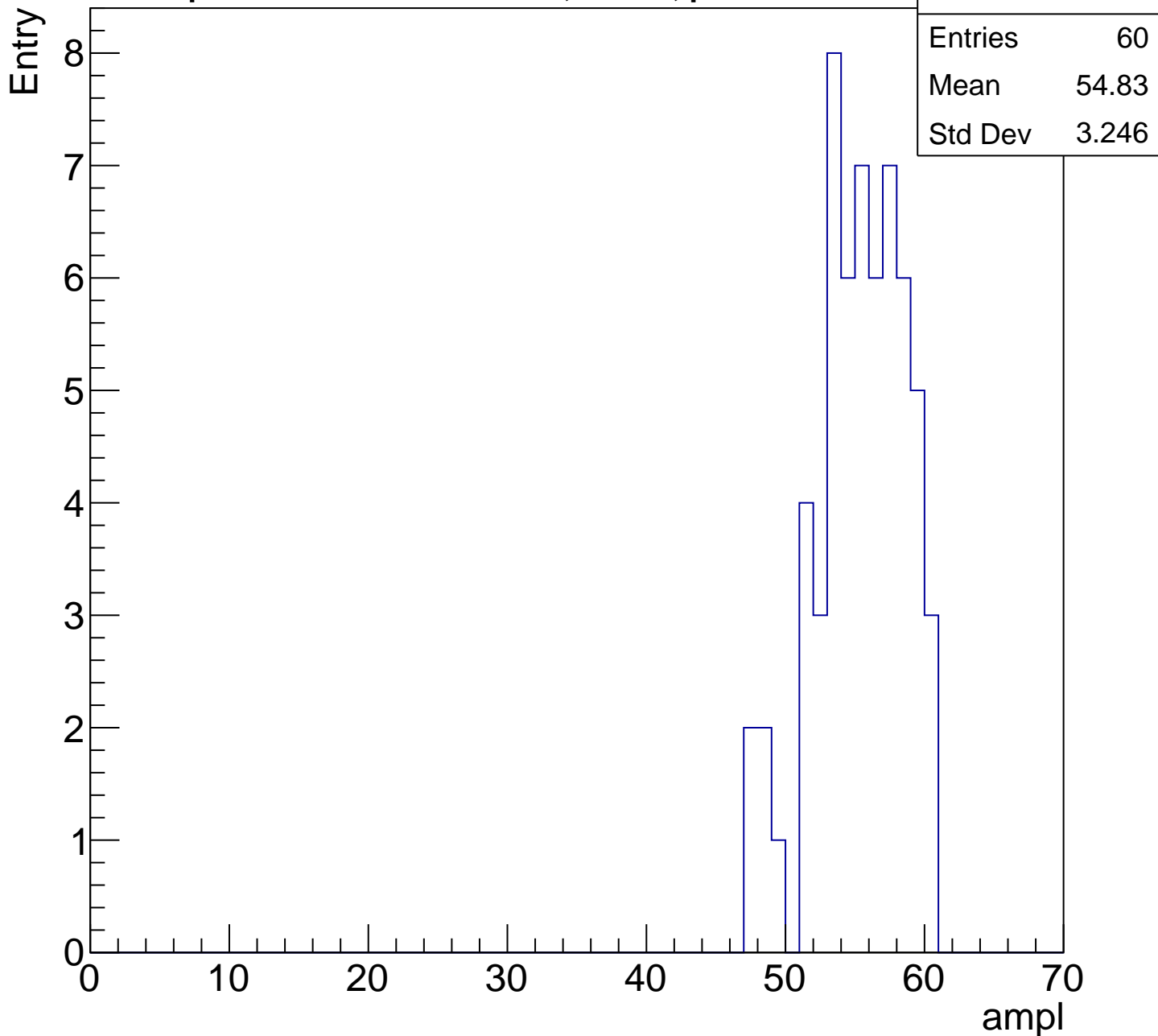
Entries	69
Mean	49.3
Std Dev	3.751

Entry



# B1L003S, U26-ch60, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

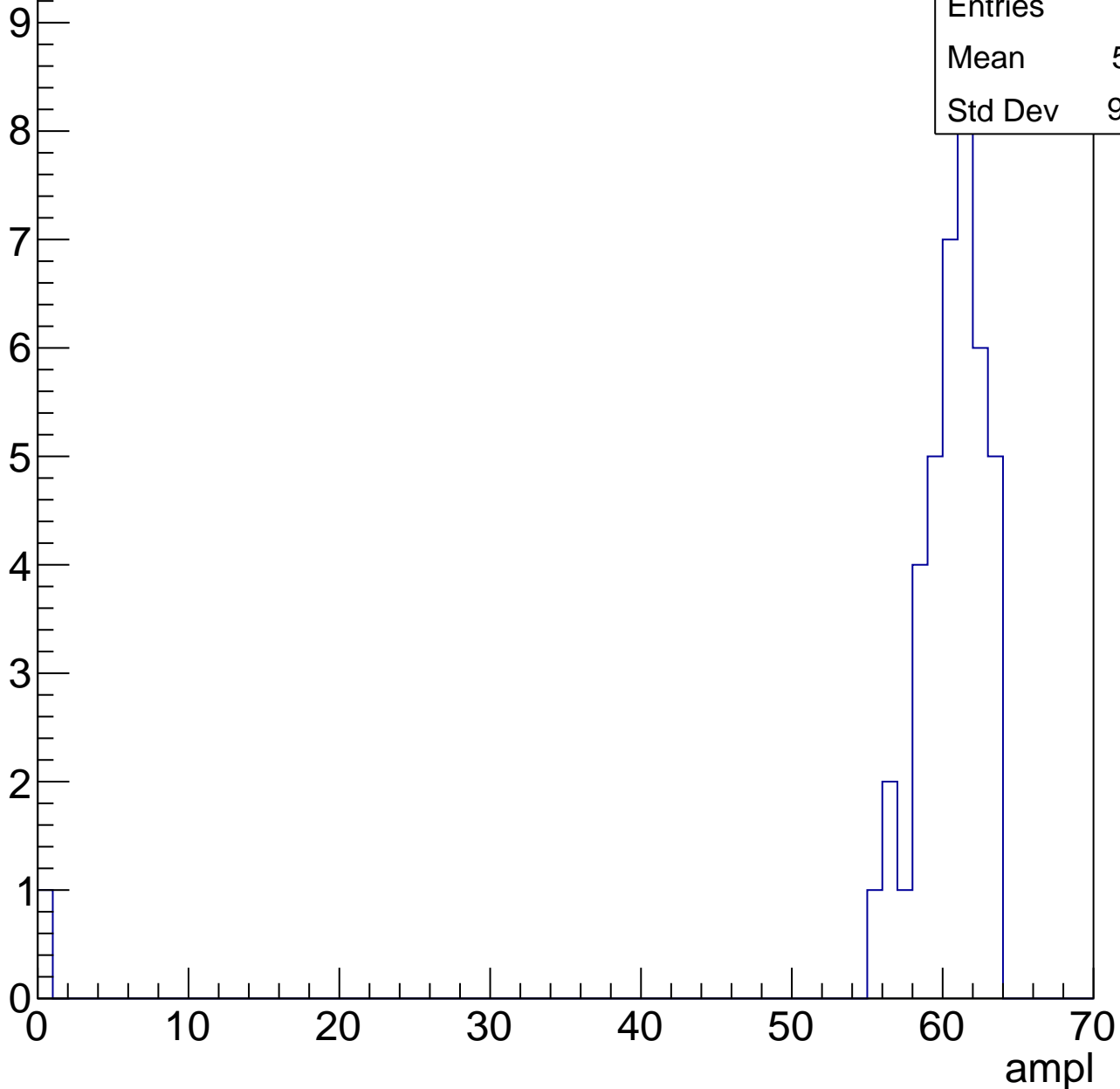


# B1L003S, U26-ch60, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

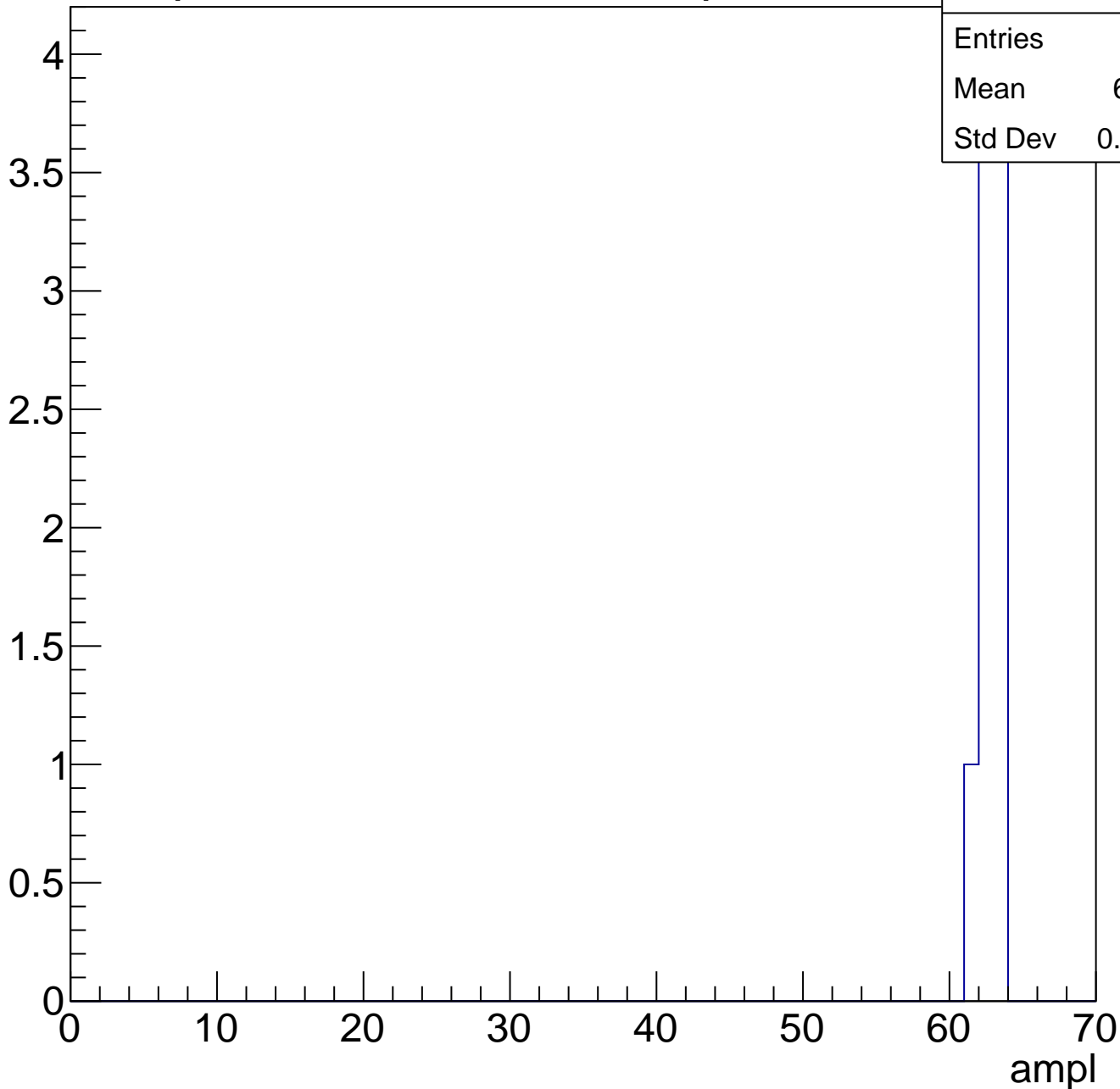
Entries	41
Mean	58.71
Std Dev	9.495



# B1L003S, U26-ch60, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

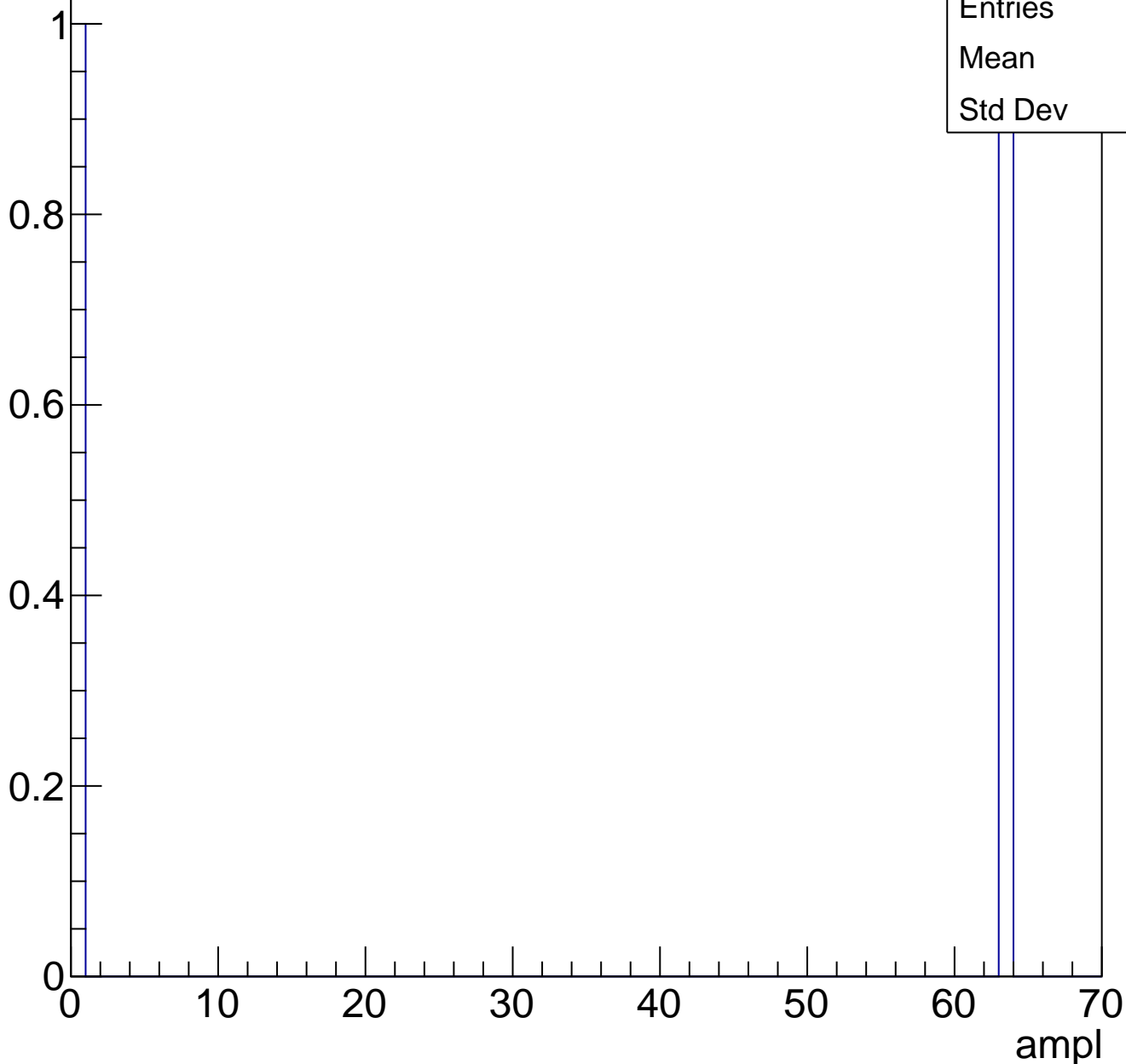




# B1L003S, U26-ch60, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U26-ch61, adc0

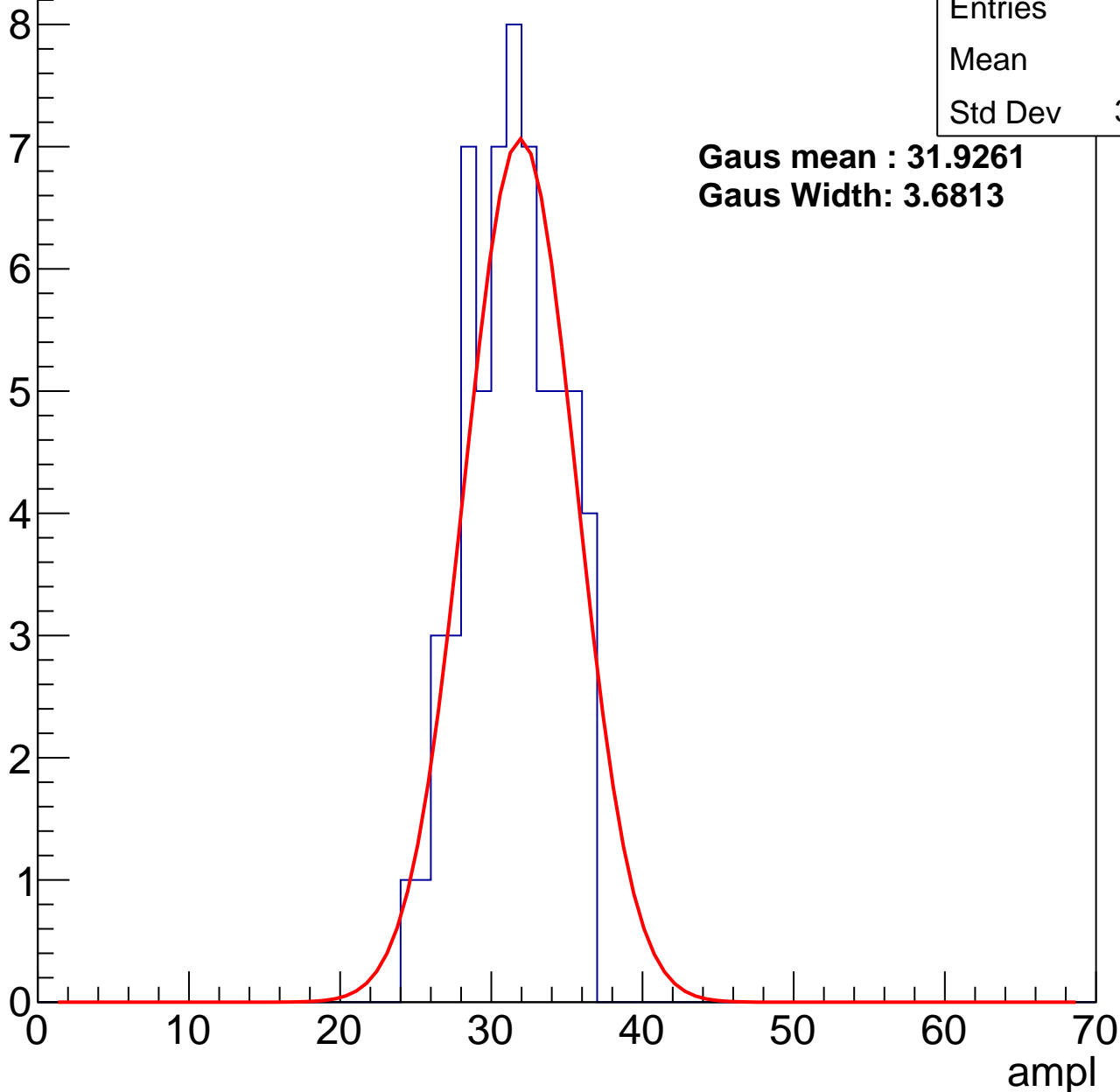
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	30.9
Std Dev	3.001

**Gaus mean : 31.9261**

**Gaus Width: 3.6813**



# B1L003S, U26-ch61, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	70
Mean	36.77
Std Dev	3.104

**Gaus mean : 37.7359**

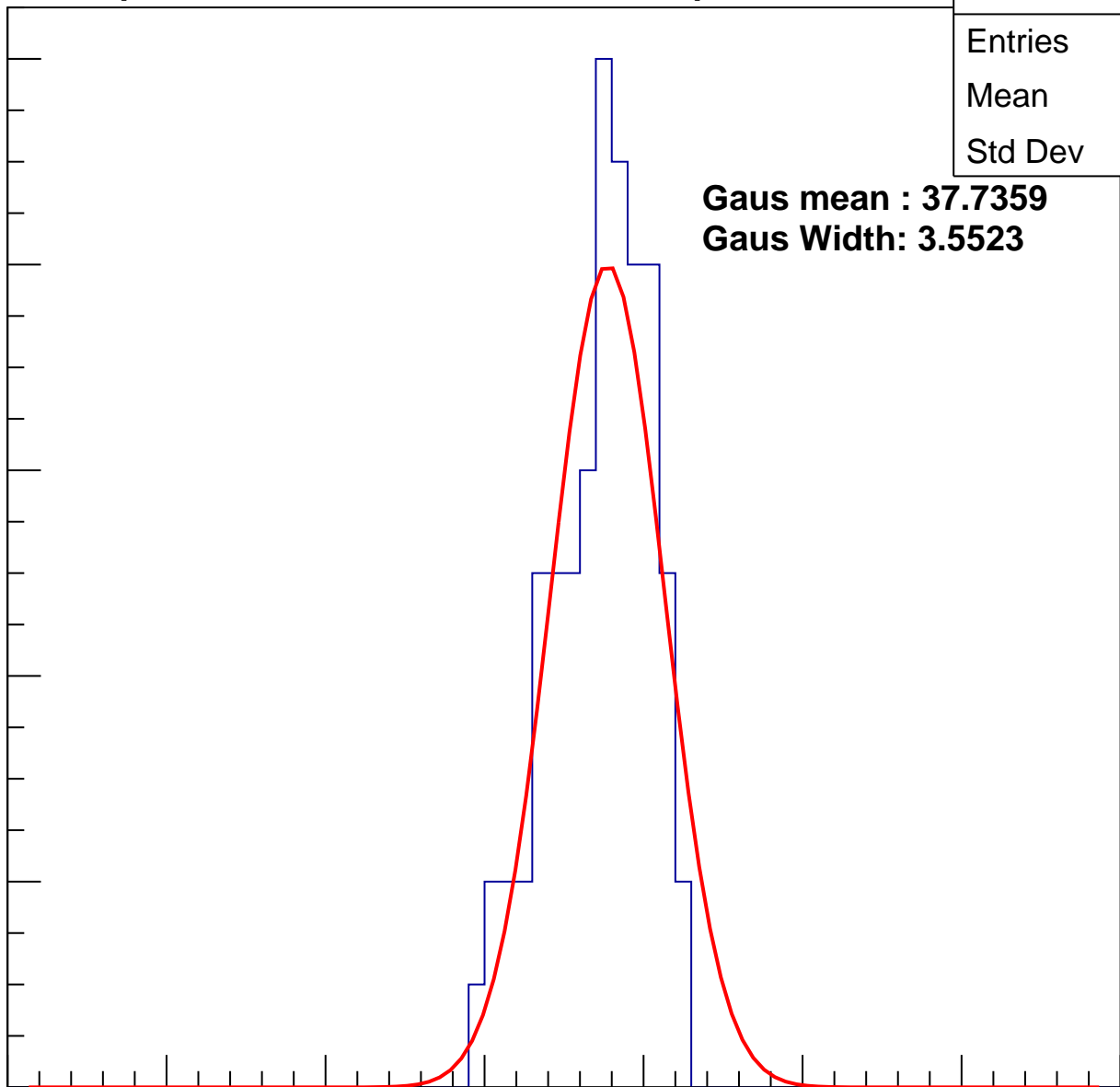
**Gaus Width: 3.5523**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U26-ch61, adc2

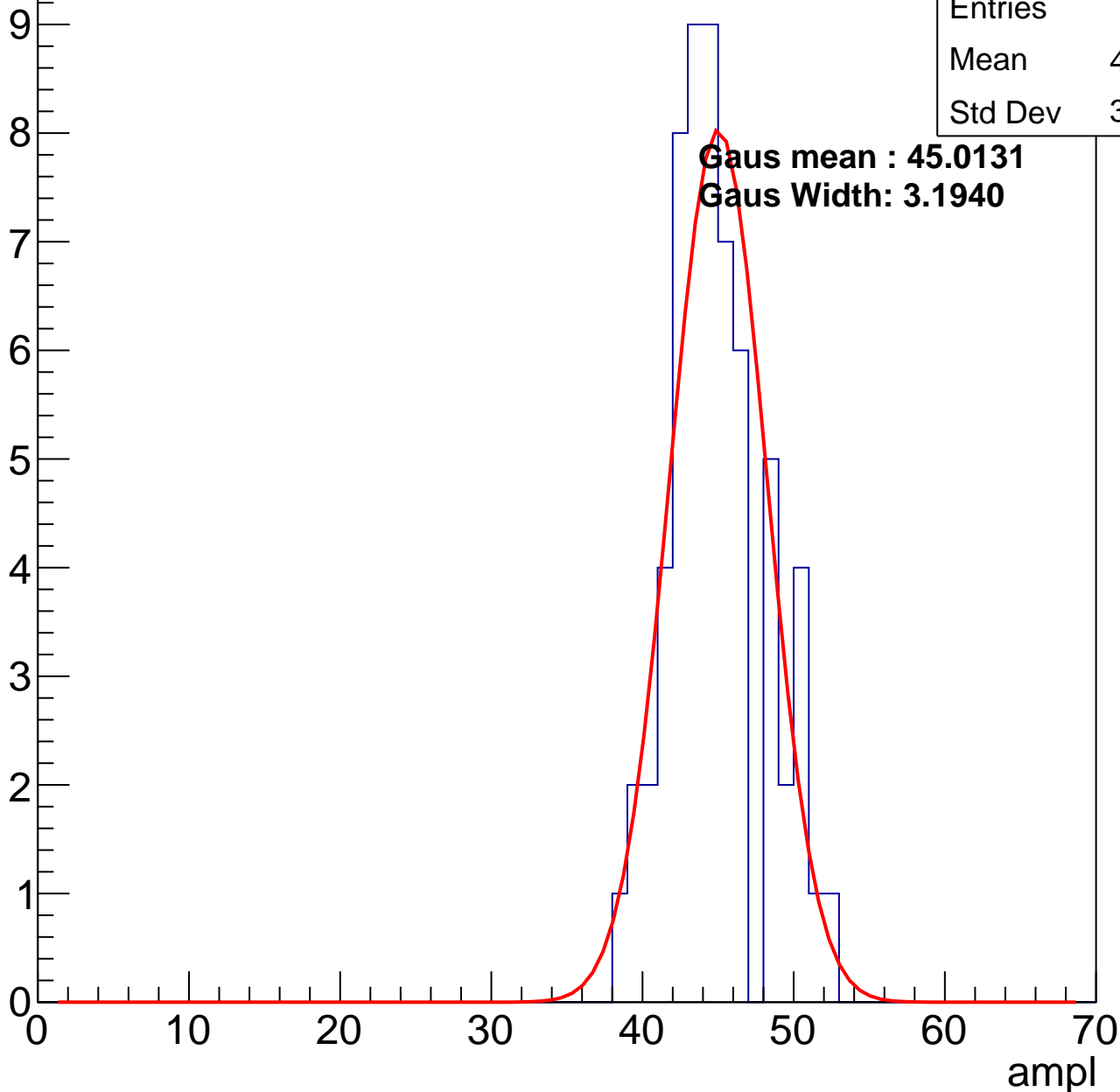
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	44.44
Std Dev	3.139

**Gaus mean : 45.0131**

**Gaus Width: 3.1940**

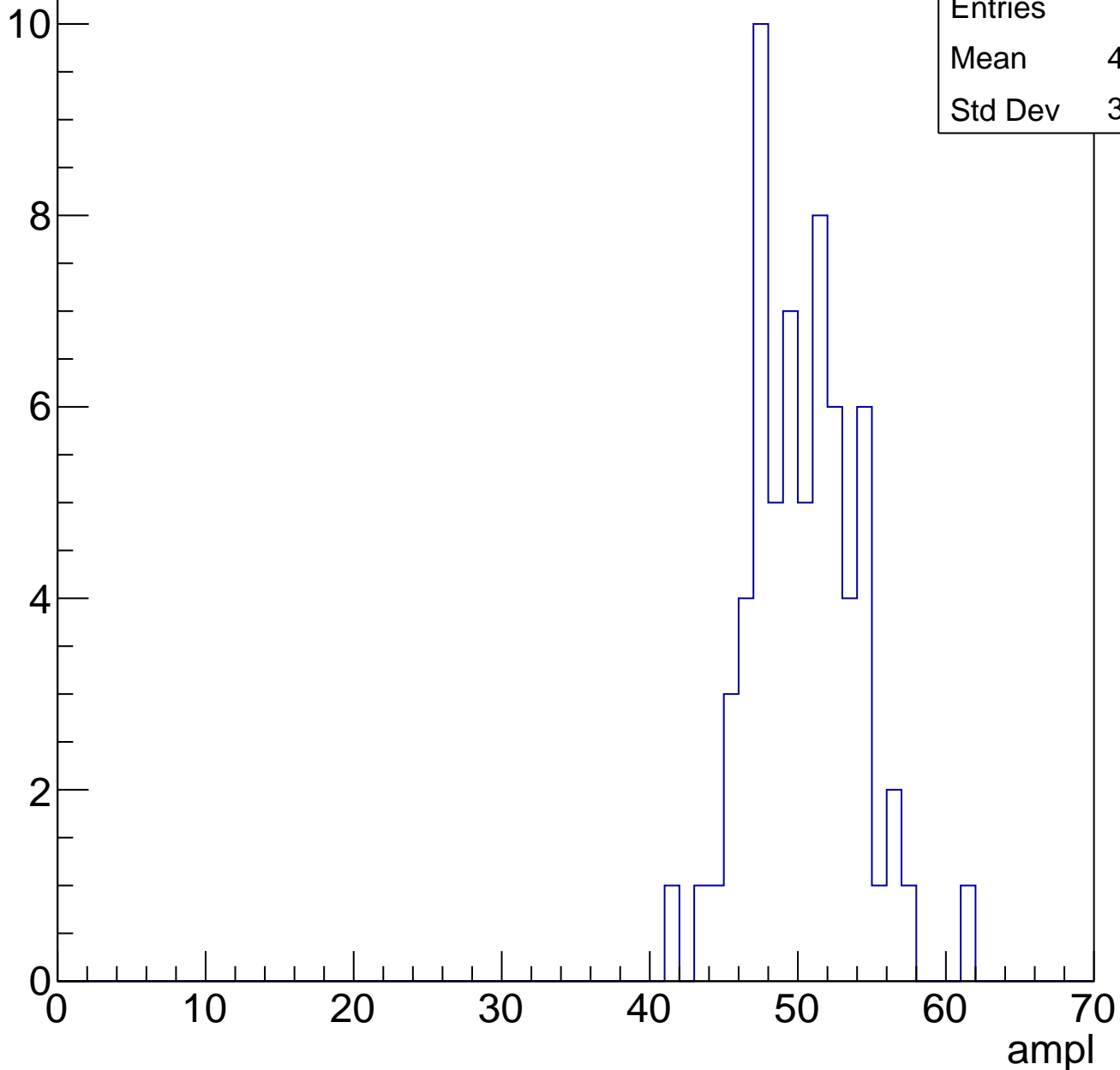


# B1L003S, U26-ch61, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	66
Mean	49.86
Std Dev	3.592

Entry



# B1L003S, U26-ch61, adc4

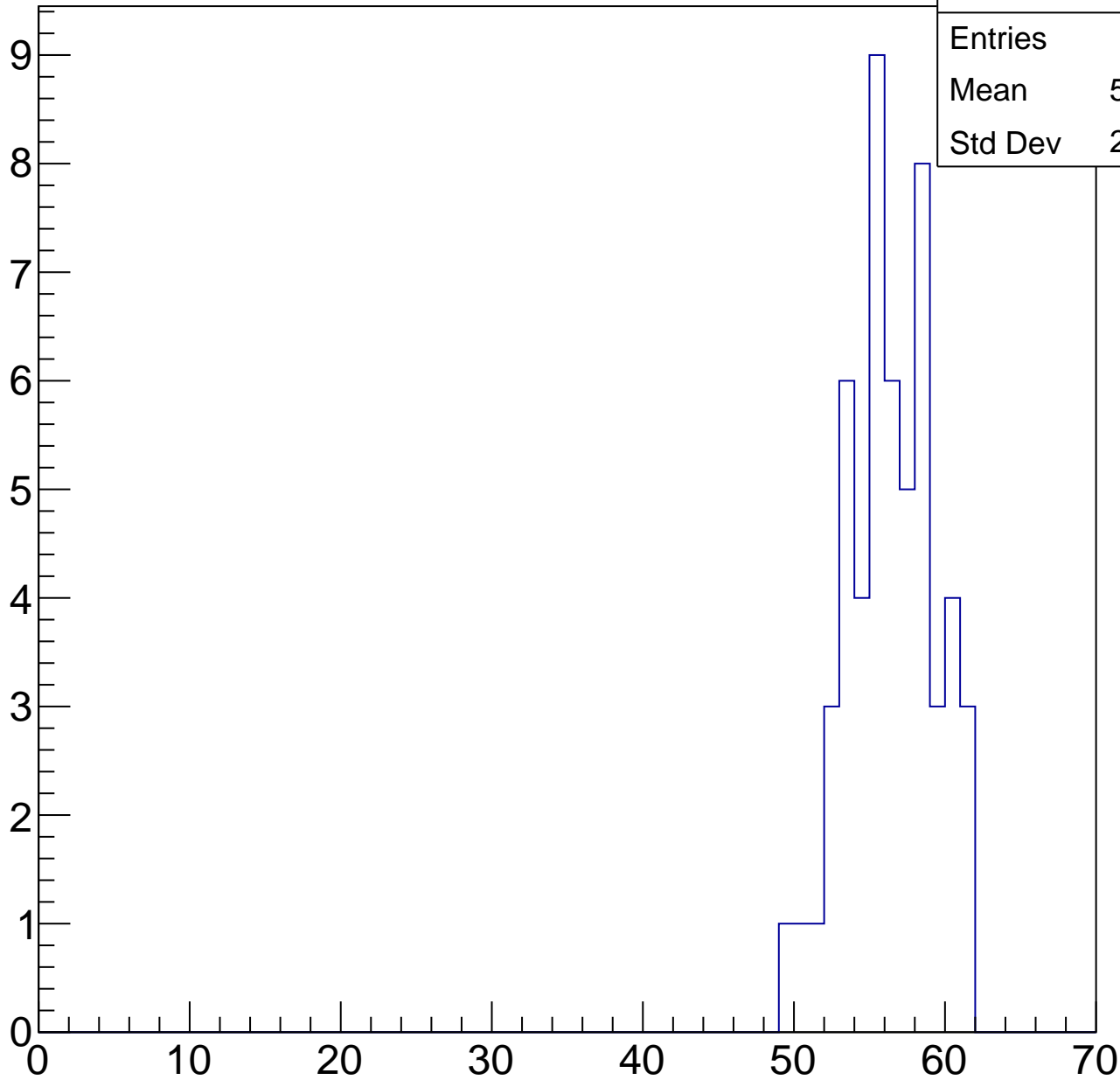
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	54
Mean	55.93
Std Dev	2.854

ampl

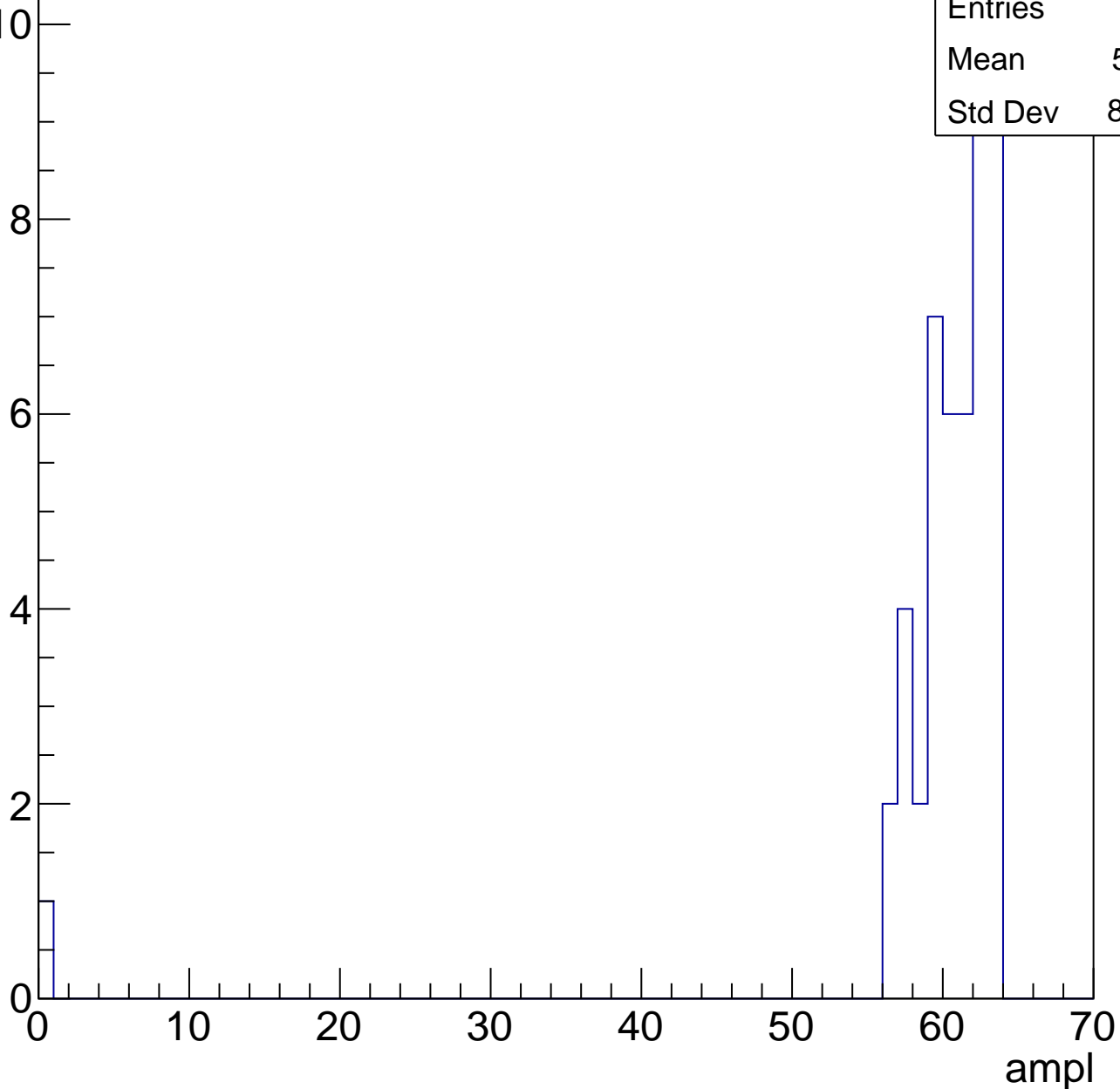


# B1L003S, U26-ch61, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	47
Mean	59.21
Std Dev	8.975



# B1L003S, U26-ch61, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch61, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U26-ch62, adc0

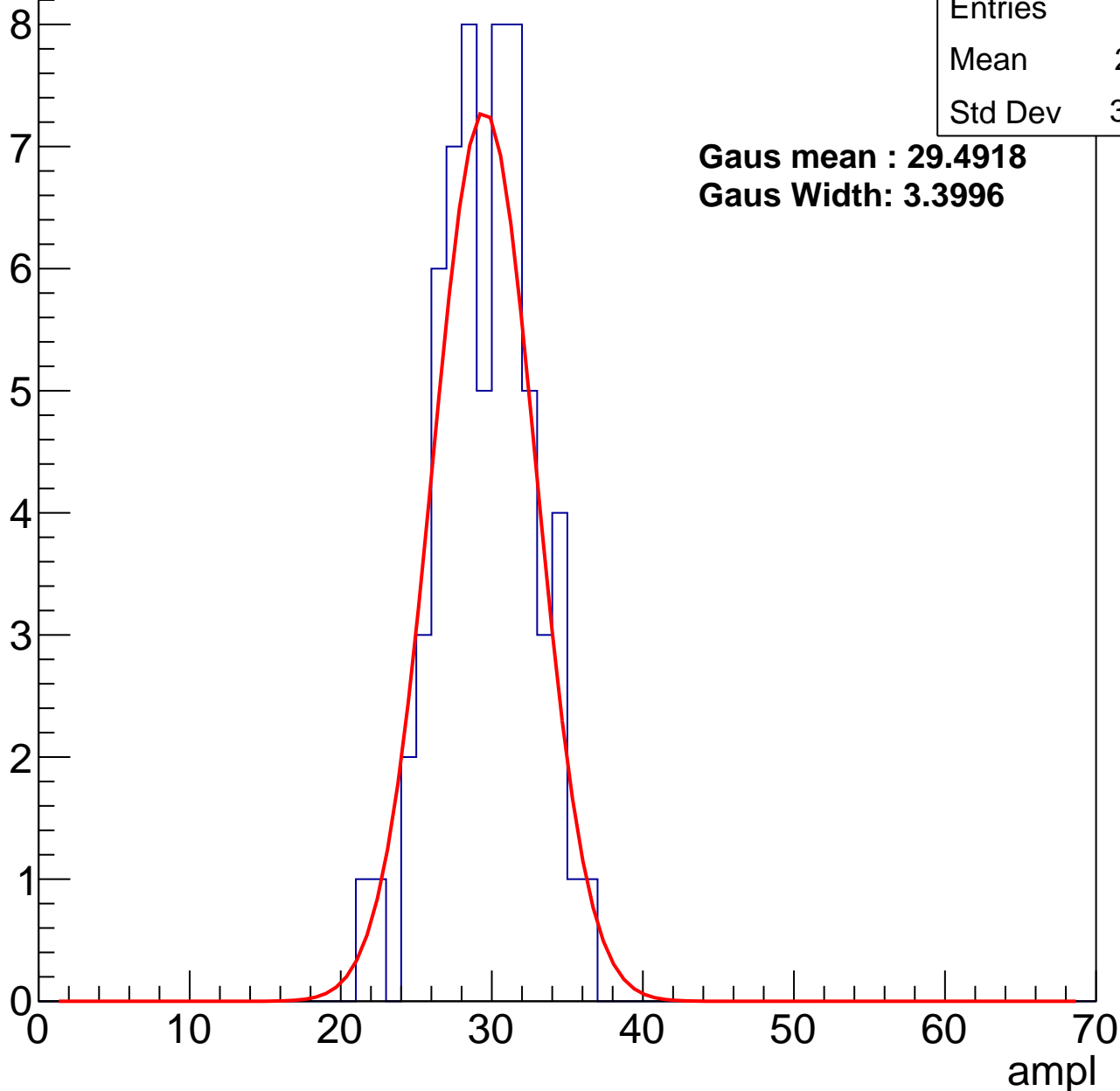
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	29.11
Std Dev	3.133

**Gaus mean : 29.4918**

**Gaus Width: 3.3996**



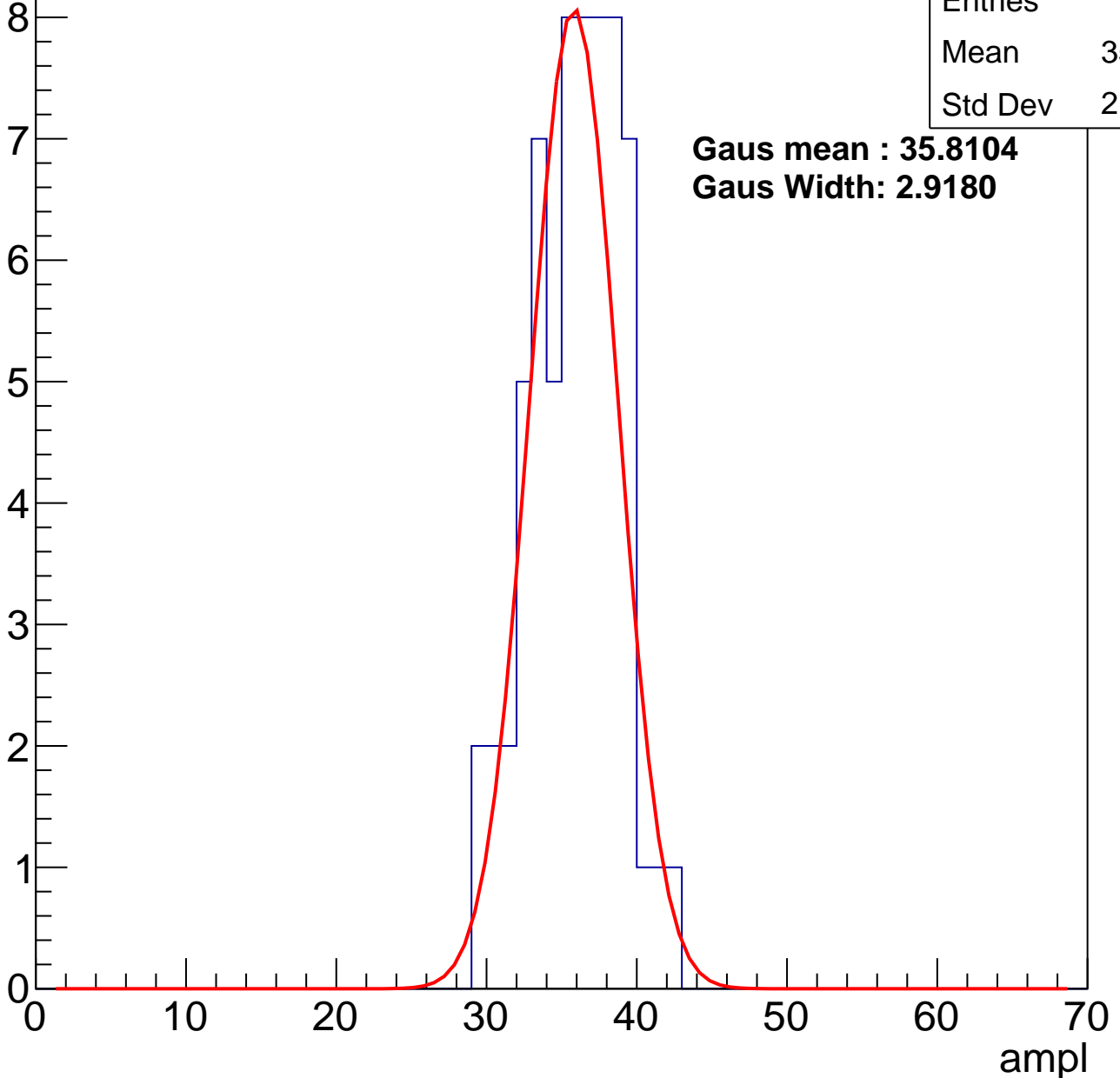
# B1L003S, U26-ch62, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	35.46
Std Dev	2.915

**Gaus mean : 35.8104**  
**Gaus Width: 2.9180**



# B1L003S, U26-ch62, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	42.67
Std Dev	3.315

**Gaus mean : 43.2956**

**Gaus Width: 3.4787**

10

8

6

4

2

0

ampl

0

10

20

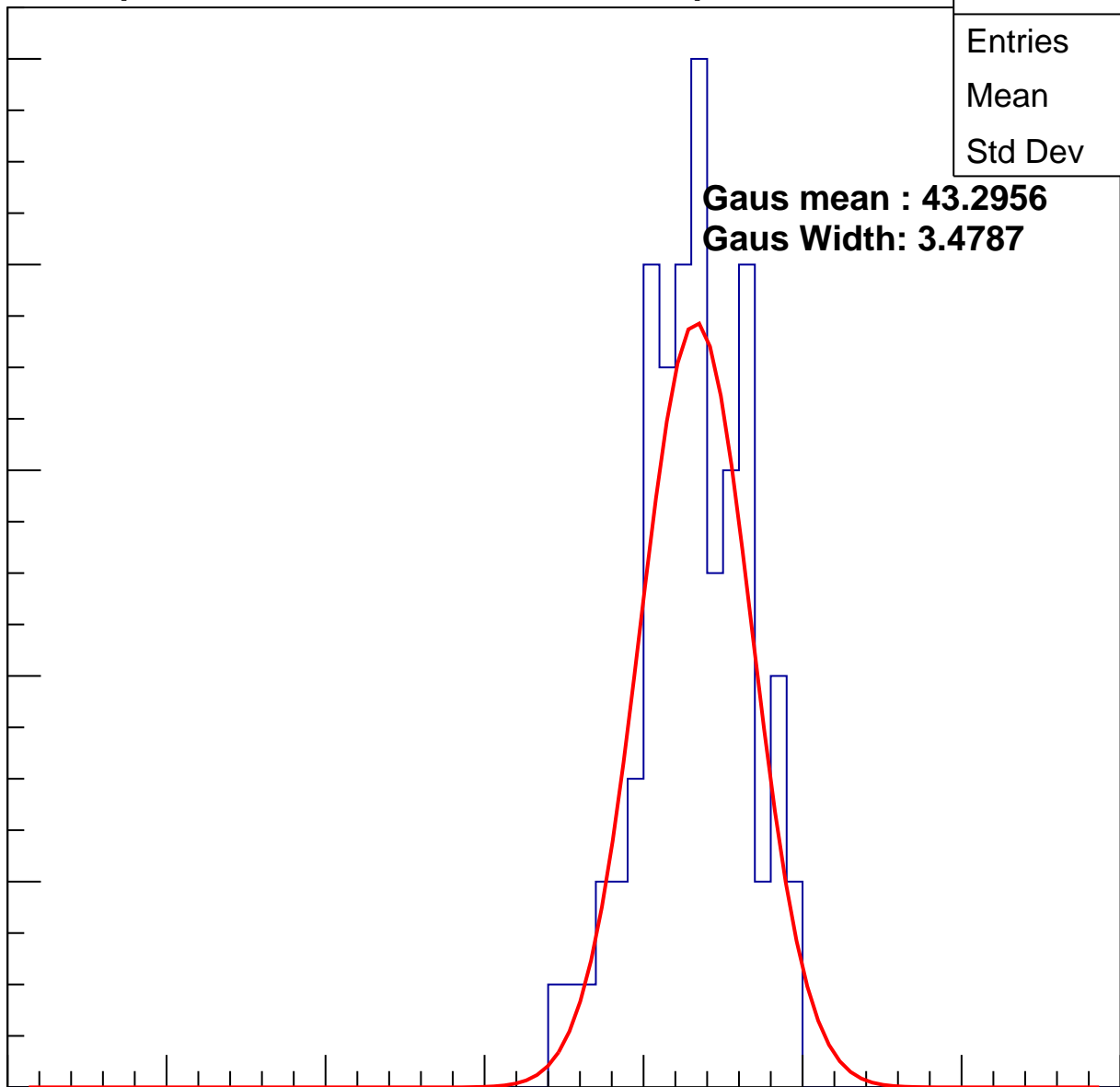
30

40

50

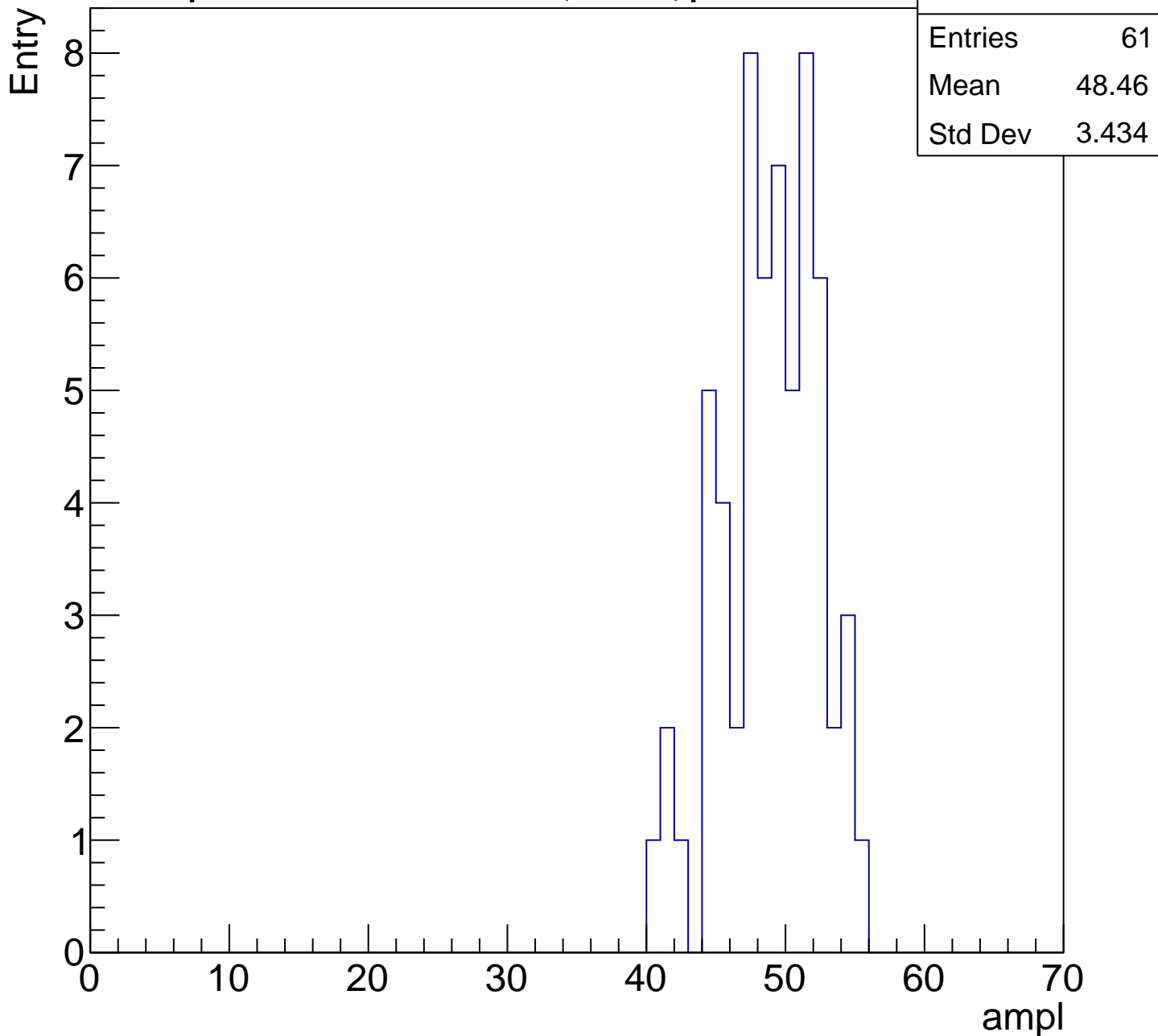
60

70



# B1L003S, U26-ch62, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

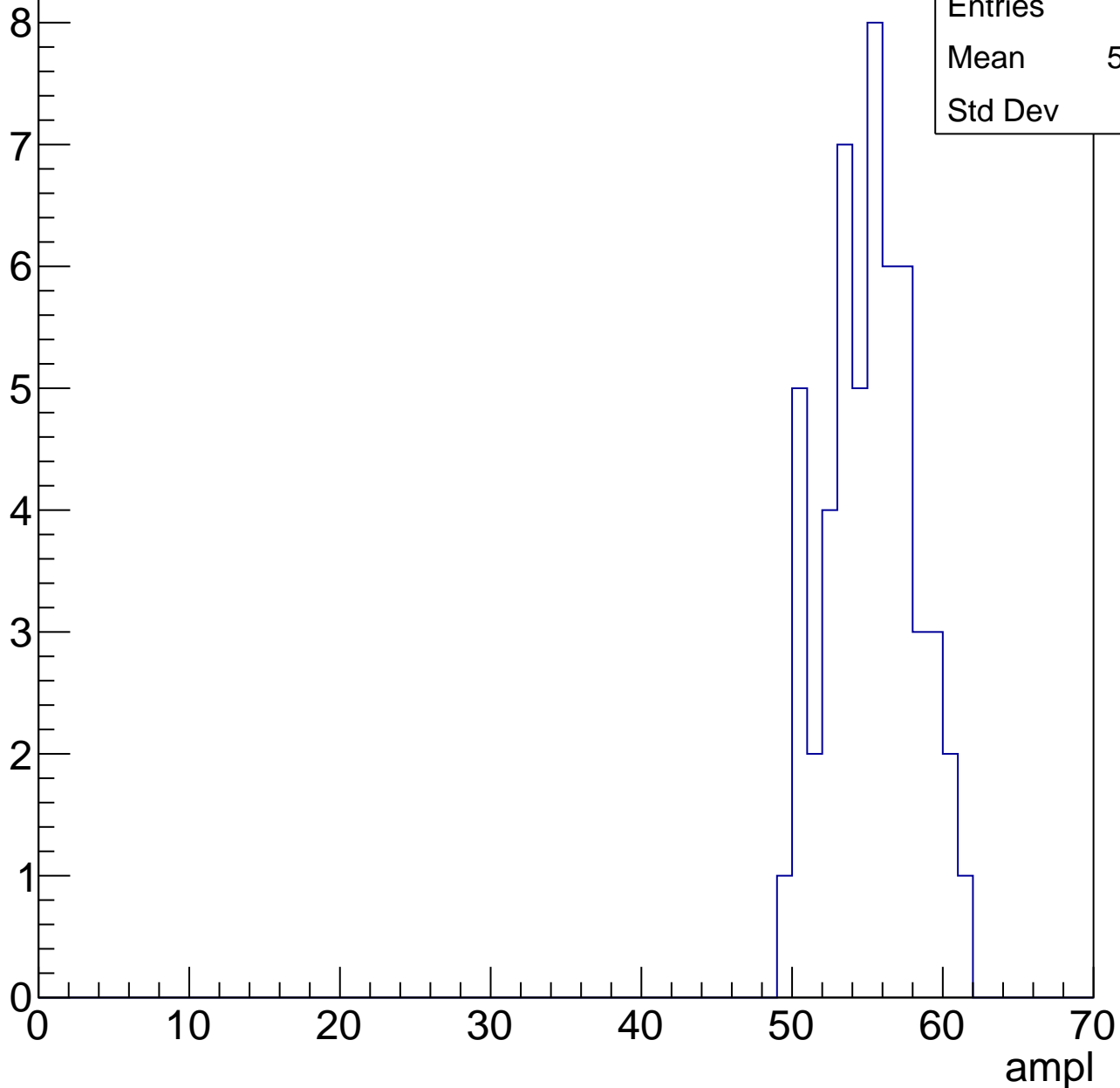


# B1L003S, U26-ch62, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	54.72
Std Dev	2.91

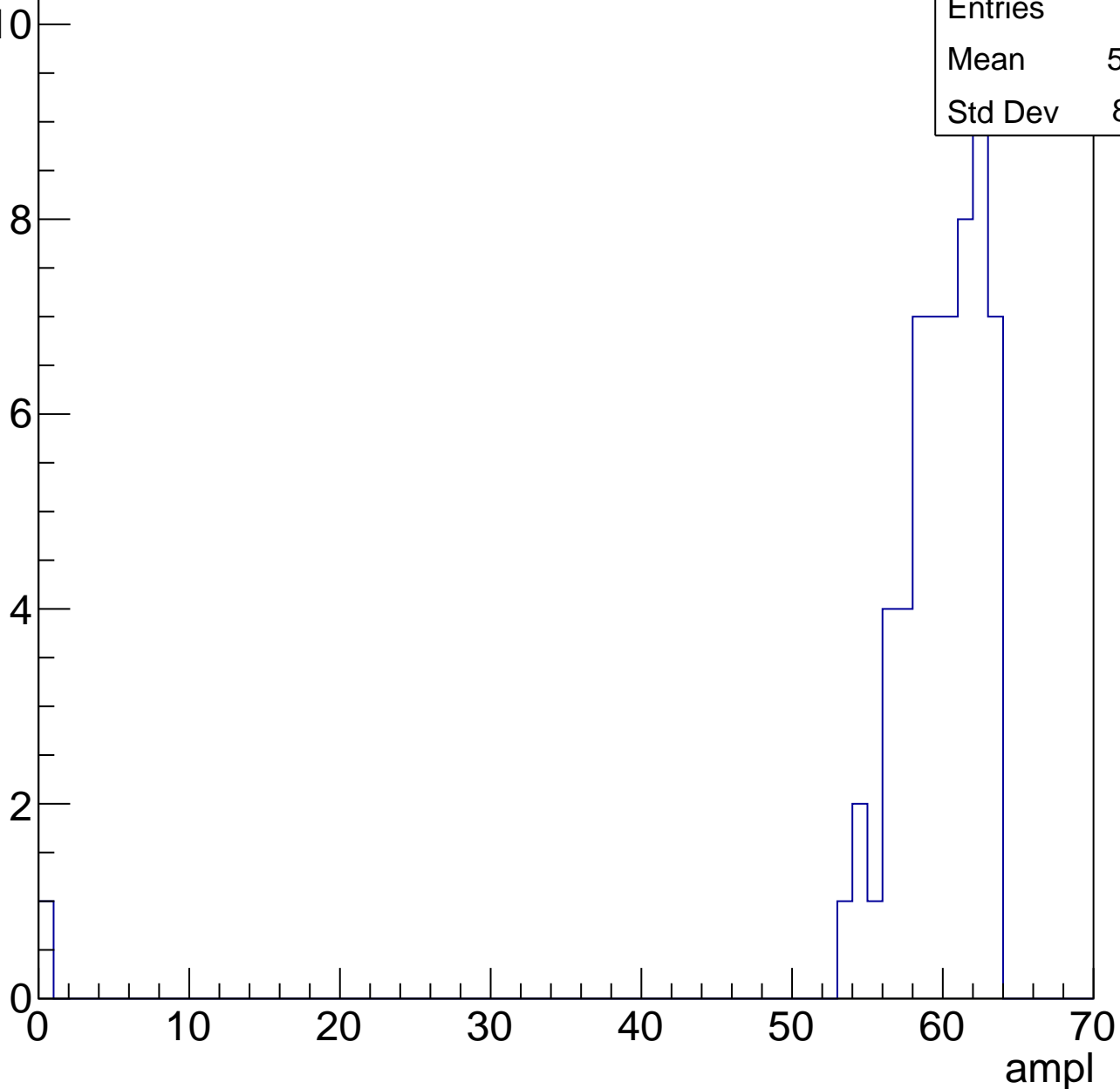


# B1L003S, U26-ch62, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

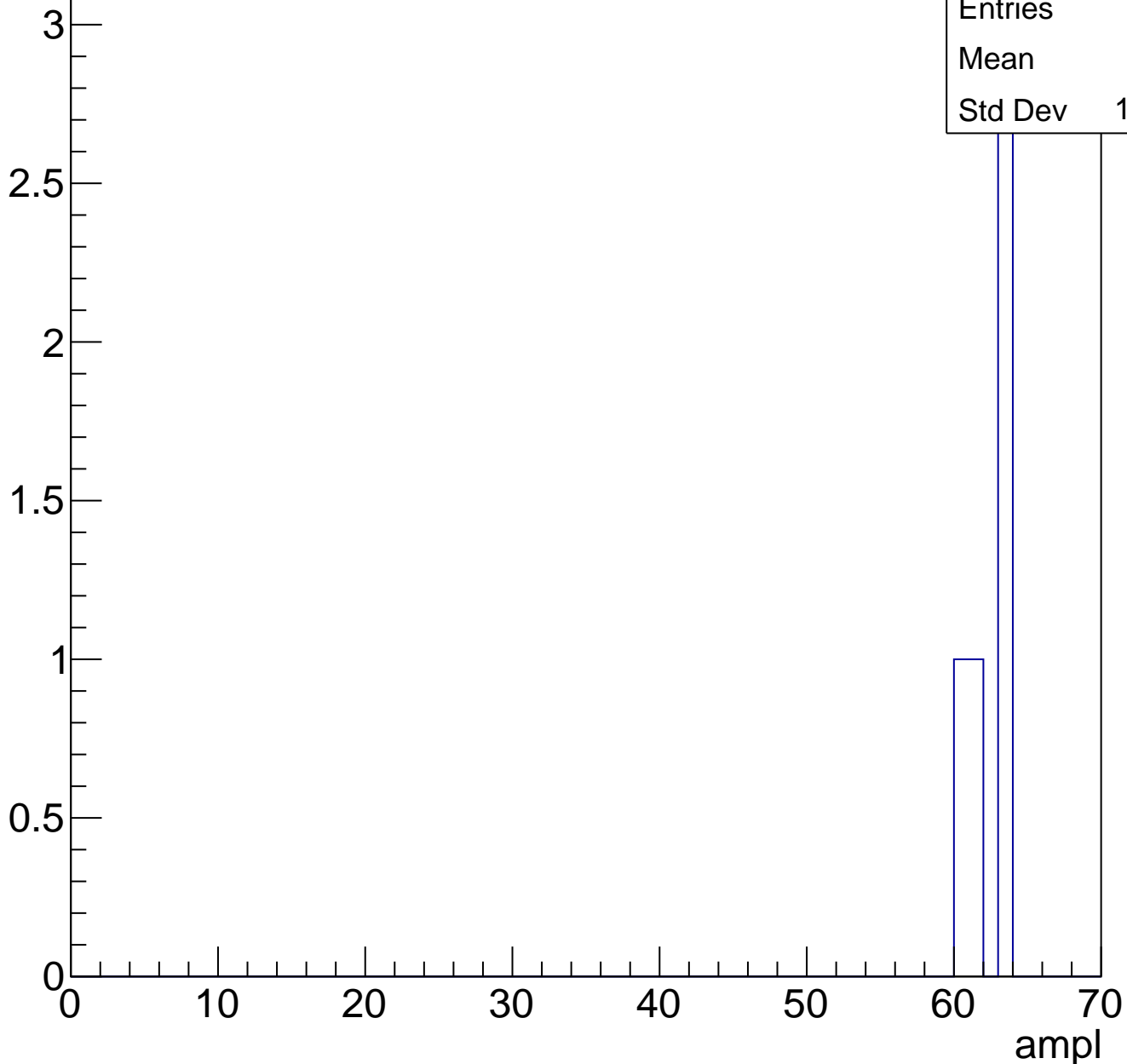
Entries	59
Mean	58.58
Std Dev	8.101



# B1L003S, U26-ch62, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch62, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L003S, U26-ch63, adc0

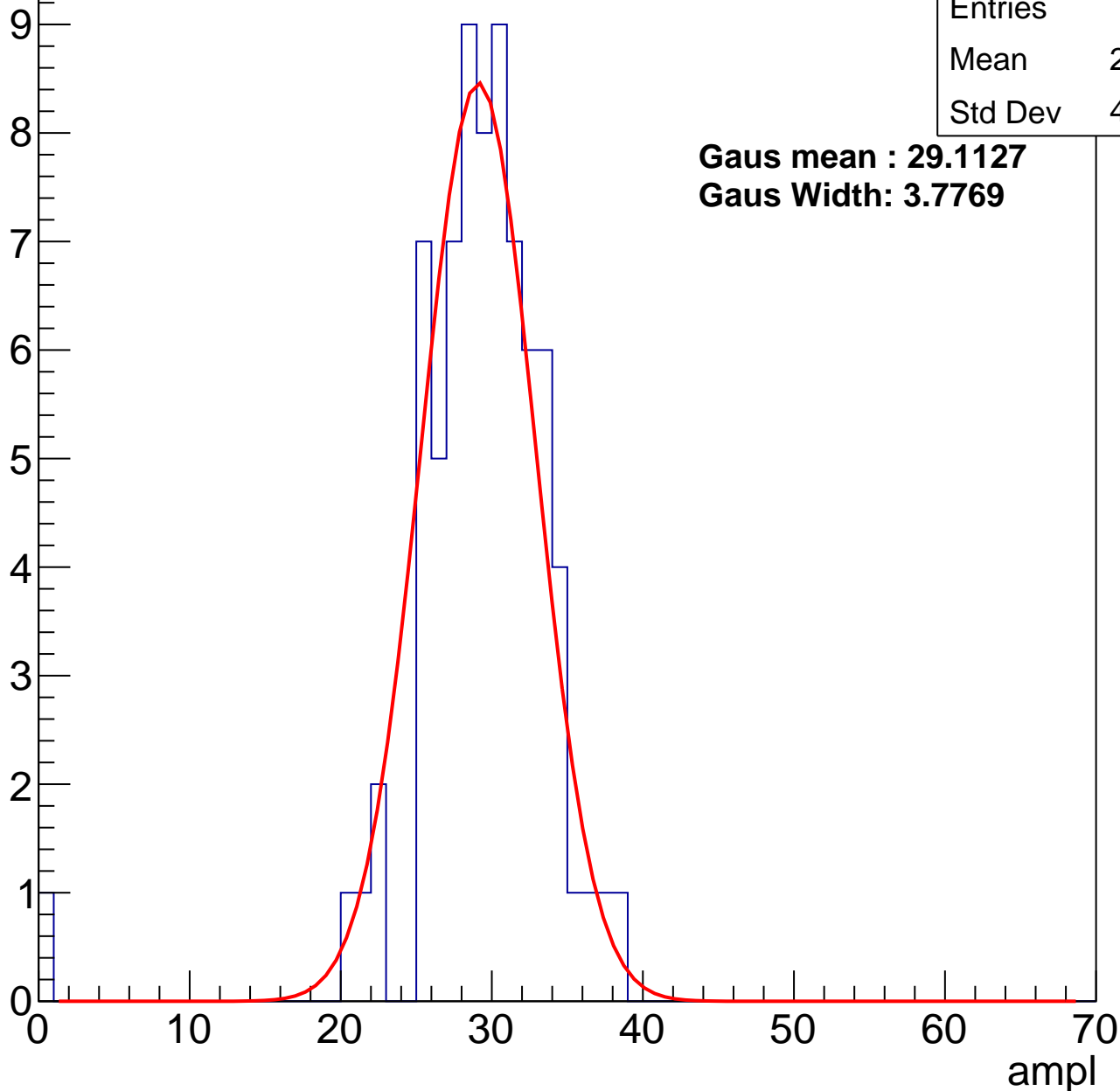
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	77
Mean	28.86
Std Dev	4.826

**Gaus mean : 29.1127**

**Gaus Width: 3.7769**



# B1L003S, U26-ch63, adc1

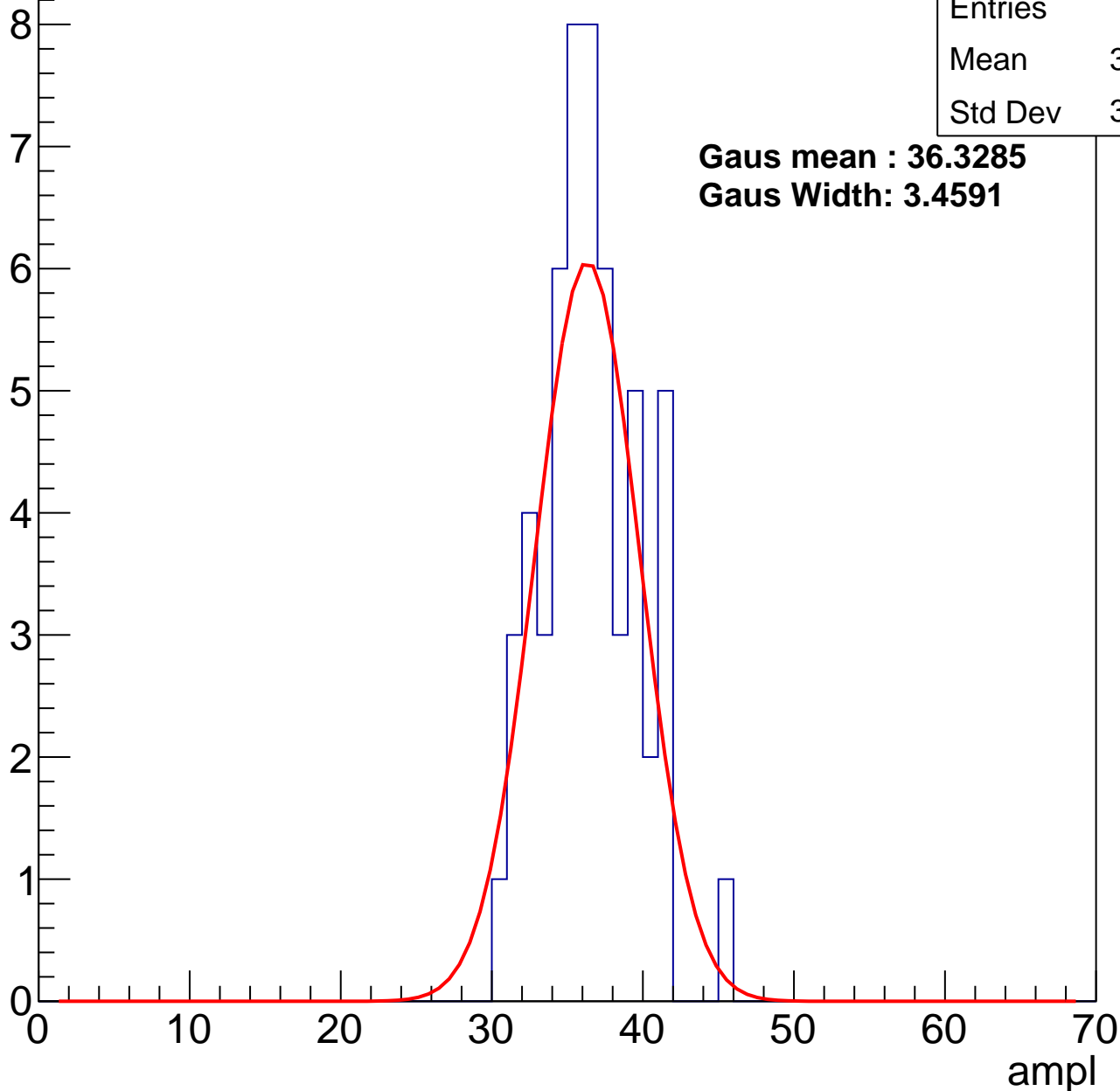
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	36.05
Std Dev	3.118

**Gaus mean : 36.3285**

**Gaus Width: 3.4591**



# B1L003S, U26-ch63, adc2

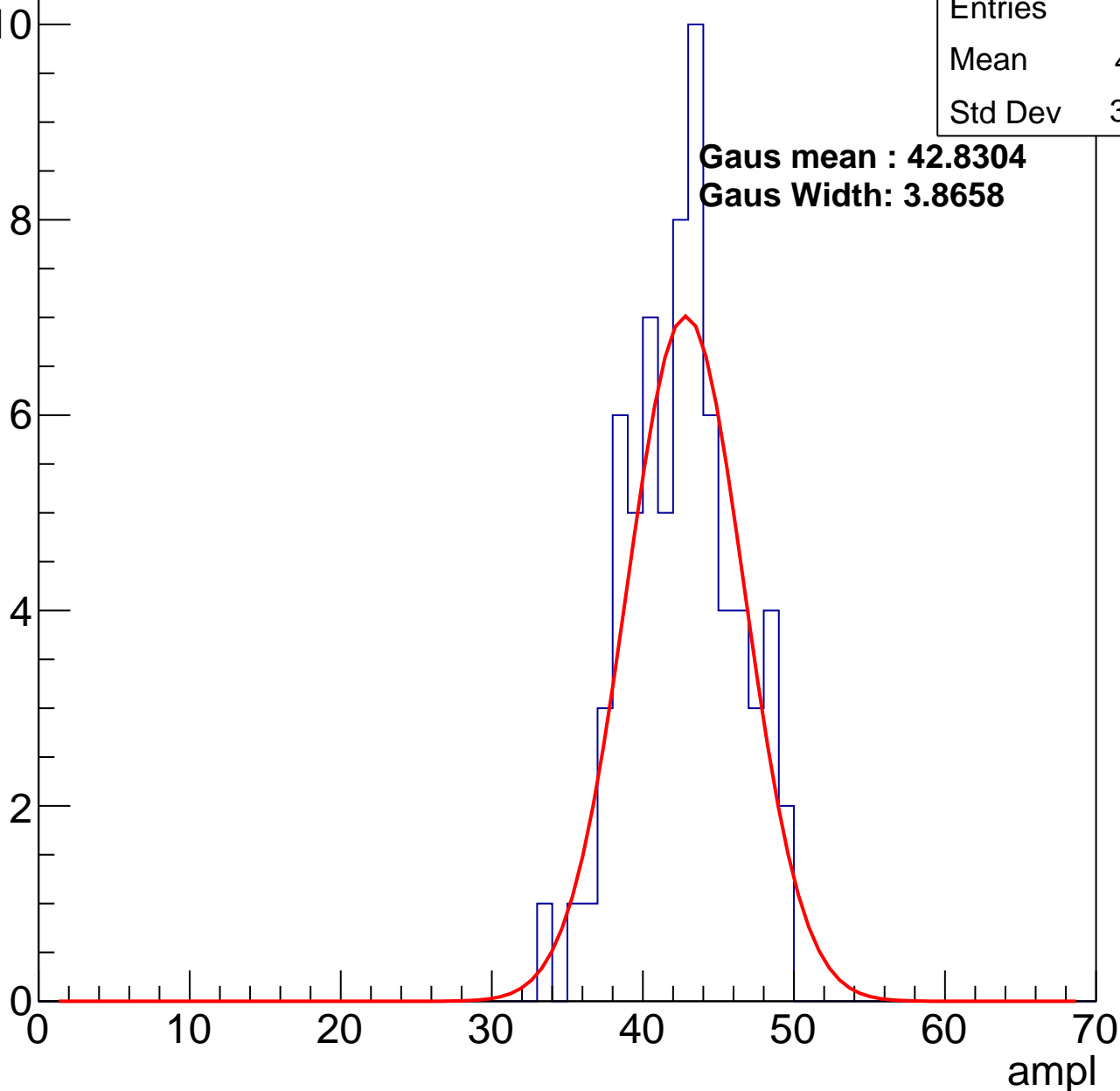
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	42.11
Std Dev	3.515

**Gaus mean : 42.8304**

**Gaus Width: 3.8658**

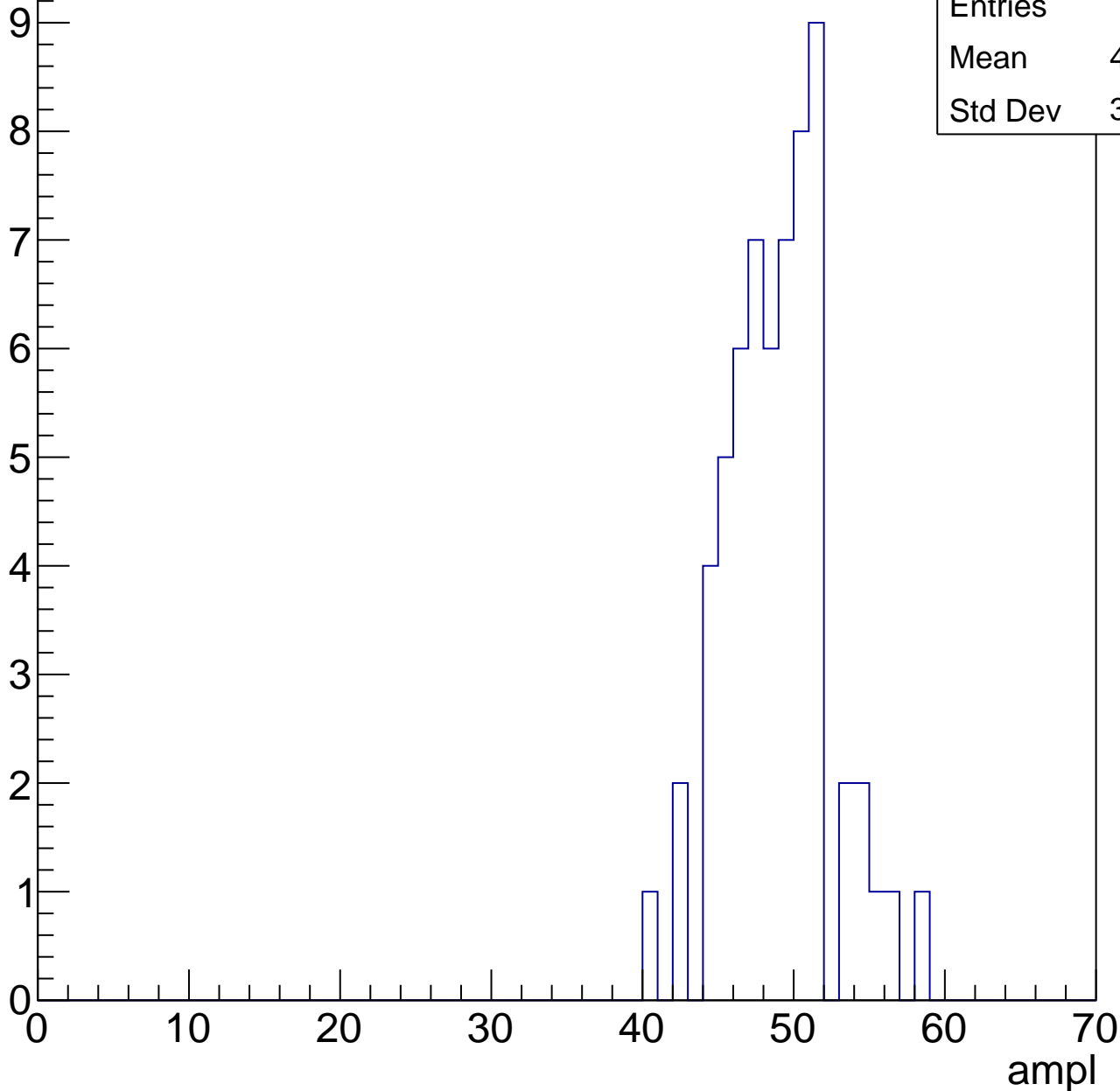


# B1L003S, U26-ch63, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	48.44
Std Dev	3.406

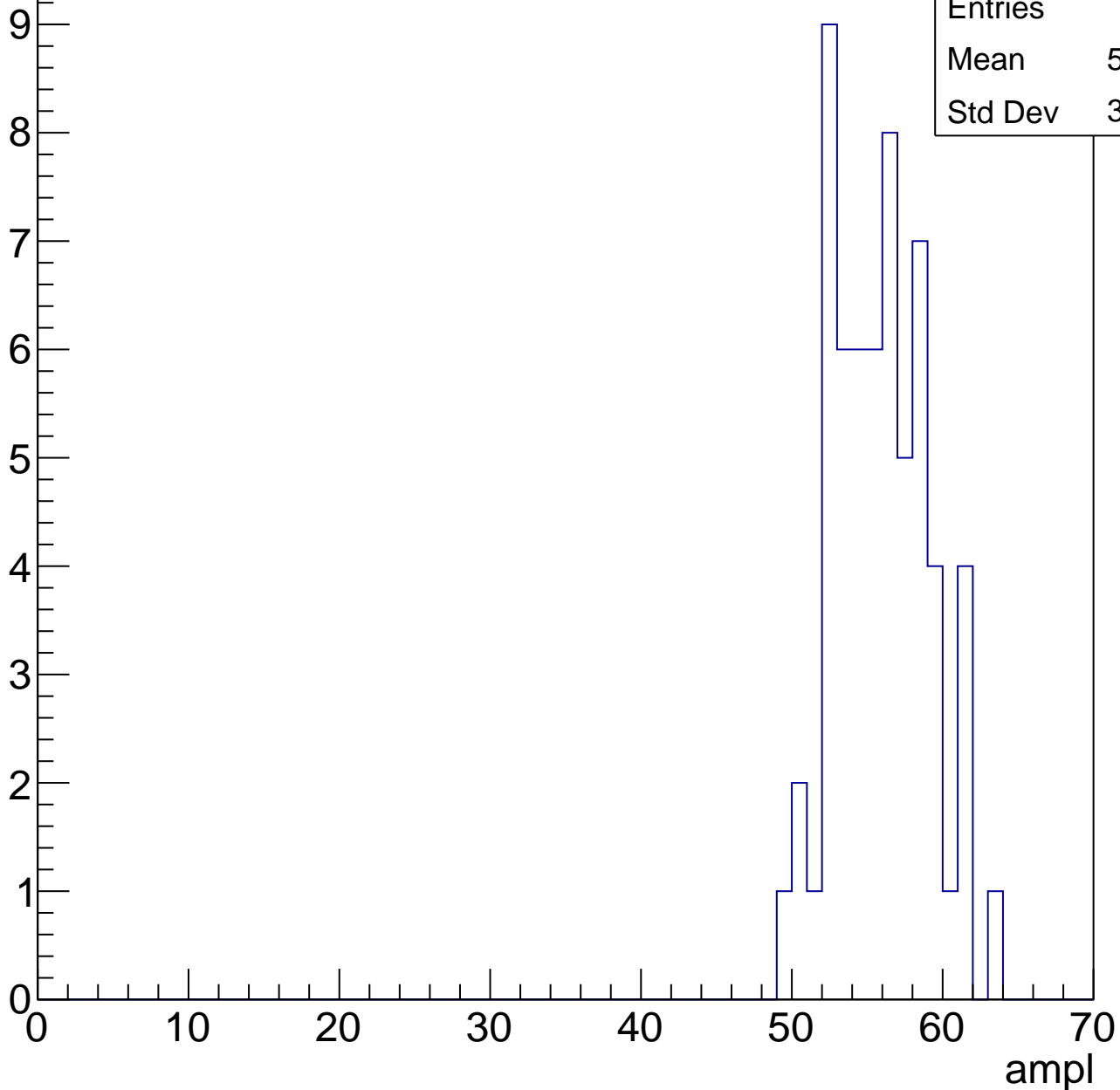


# B1L003S, U26-ch63, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	55.44
Std Dev	3.107

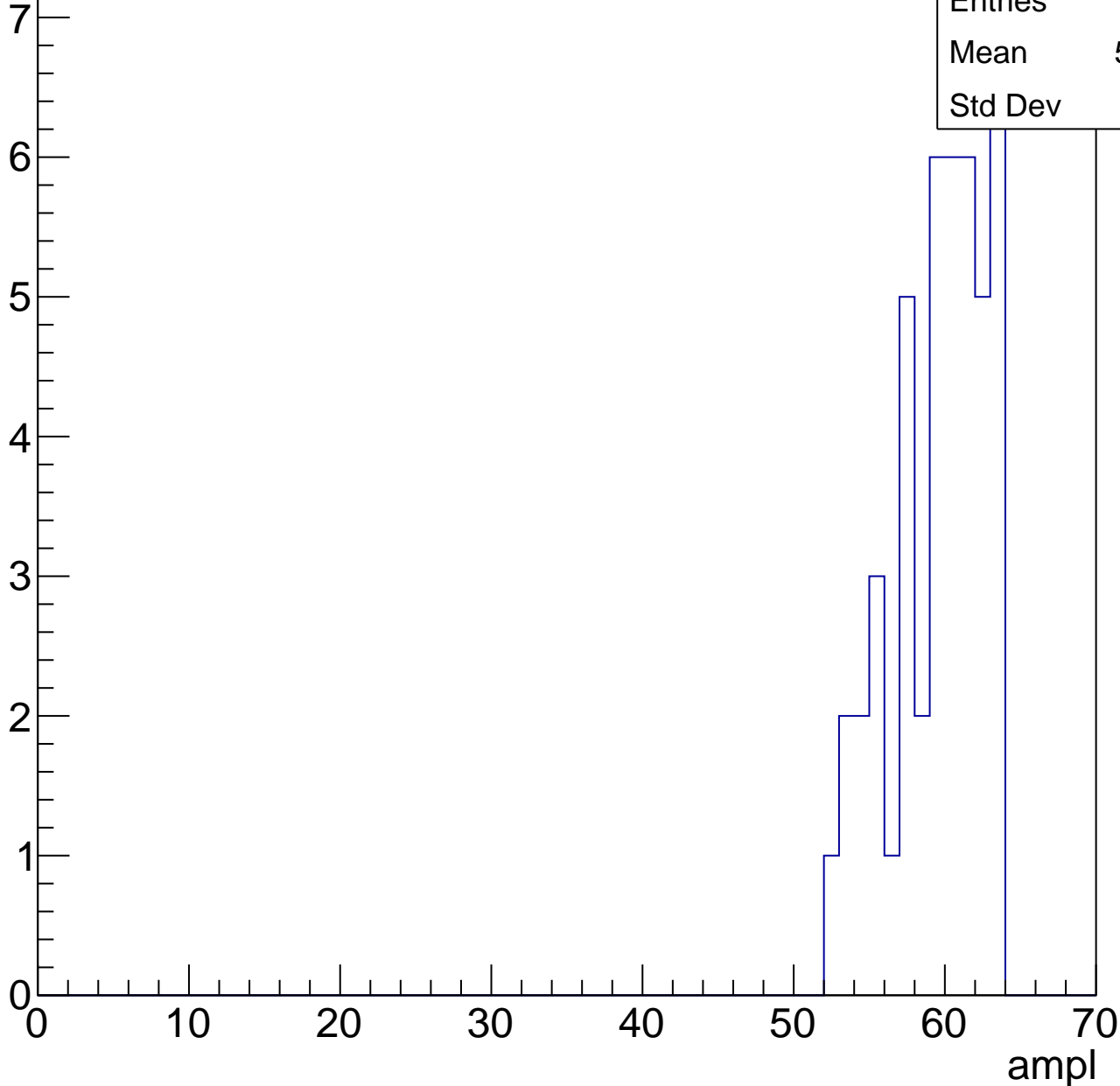


# B1L003S, U26-ch63, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	46
Mean	59.11
Std Dev	3.08

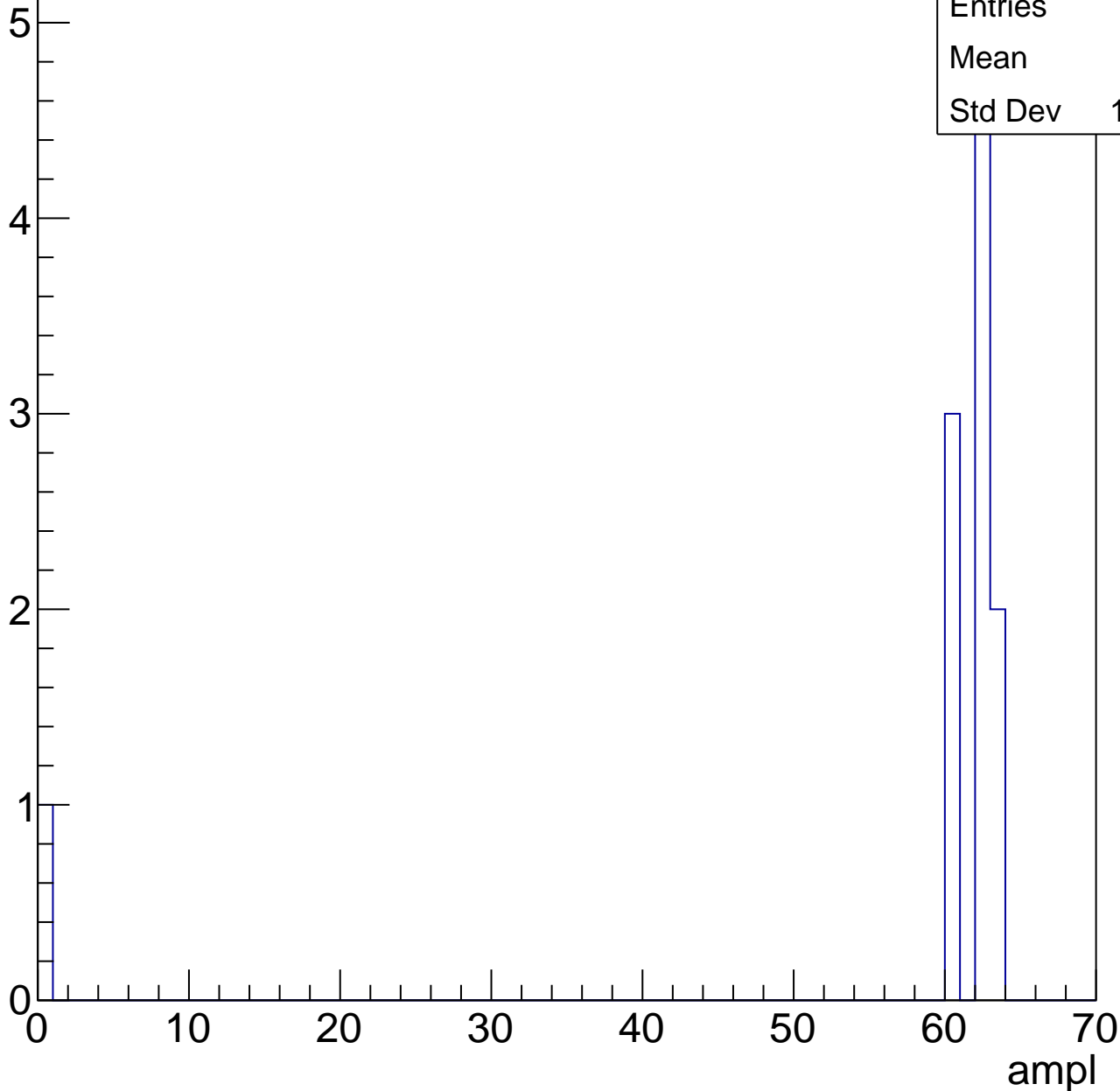


# B1L003S, U26-ch63, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	11
Mean	56
Std Dev	17.74





# B1L003S, U26-ch63, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U26-ch64, adc0

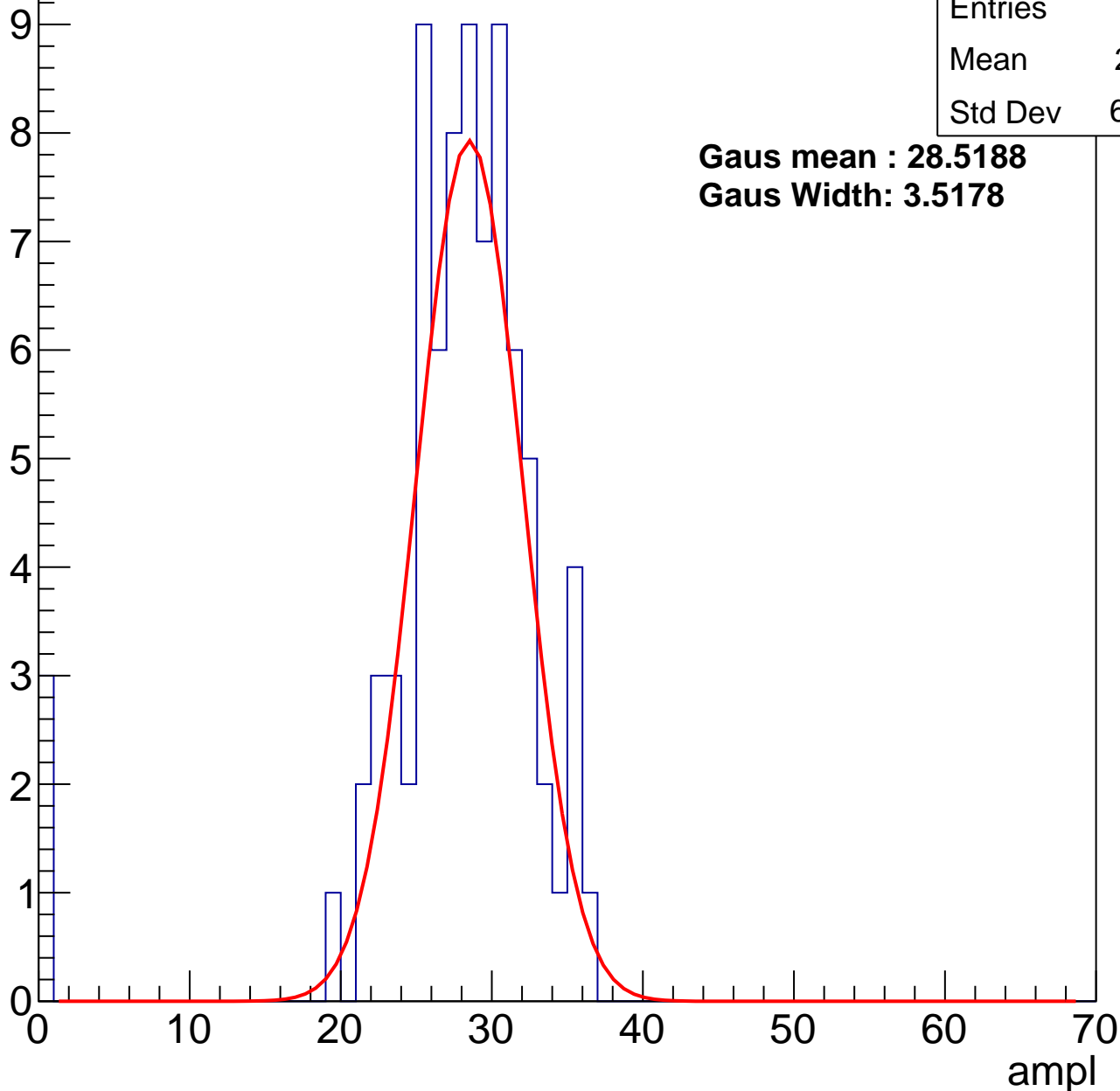
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	81
Mean	27.01
Std Dev	6.386

**Gaus mean : 28.5188**

**Gaus Width: 3.5178**



# B1L003S, U26-ch64, adc1

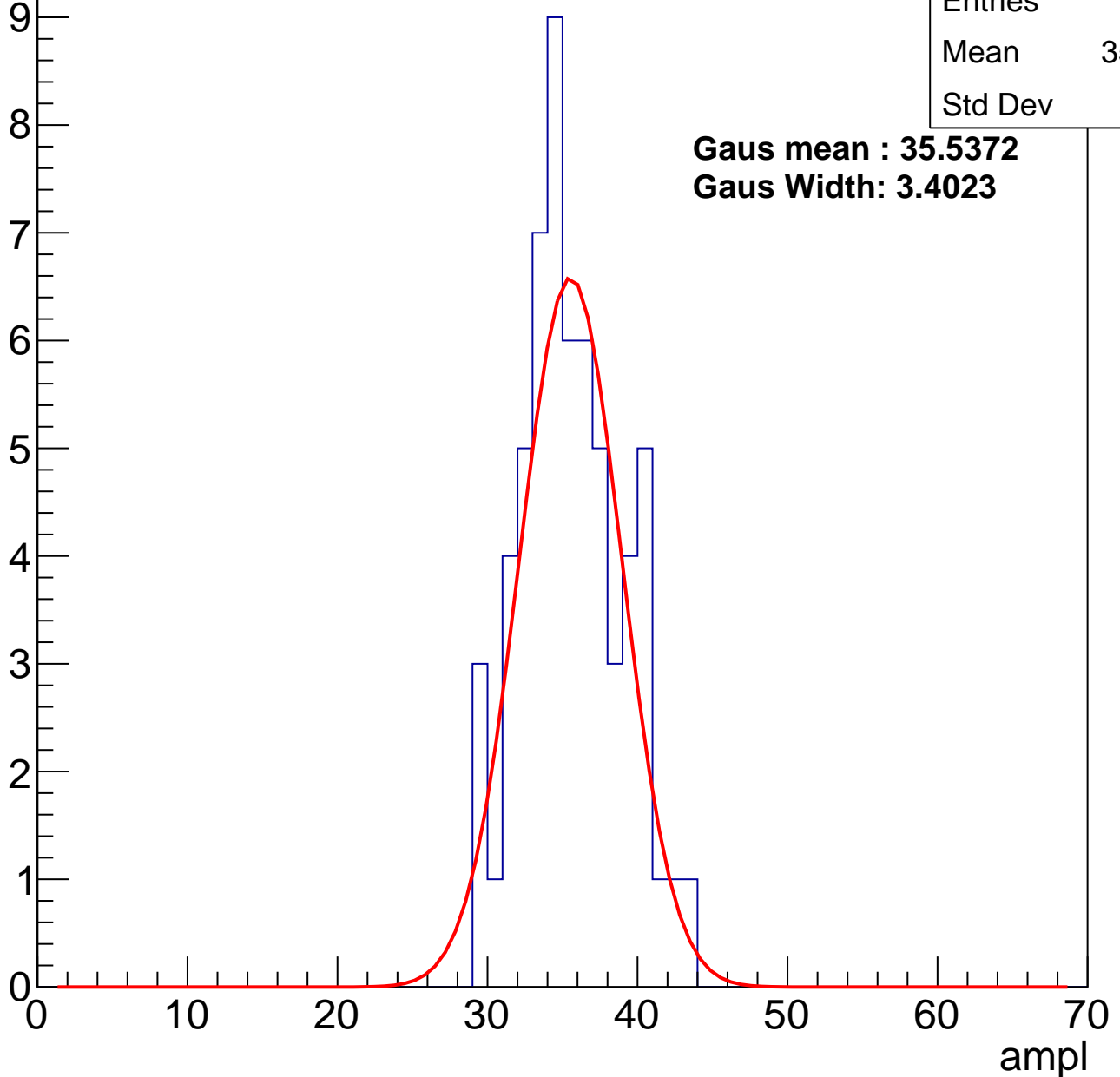
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	35.16
Std Dev	3.31

**Gaus mean : 35.5372**

**Gaus Width: 3.4023**



# B1L003S, U26-ch64, adc2

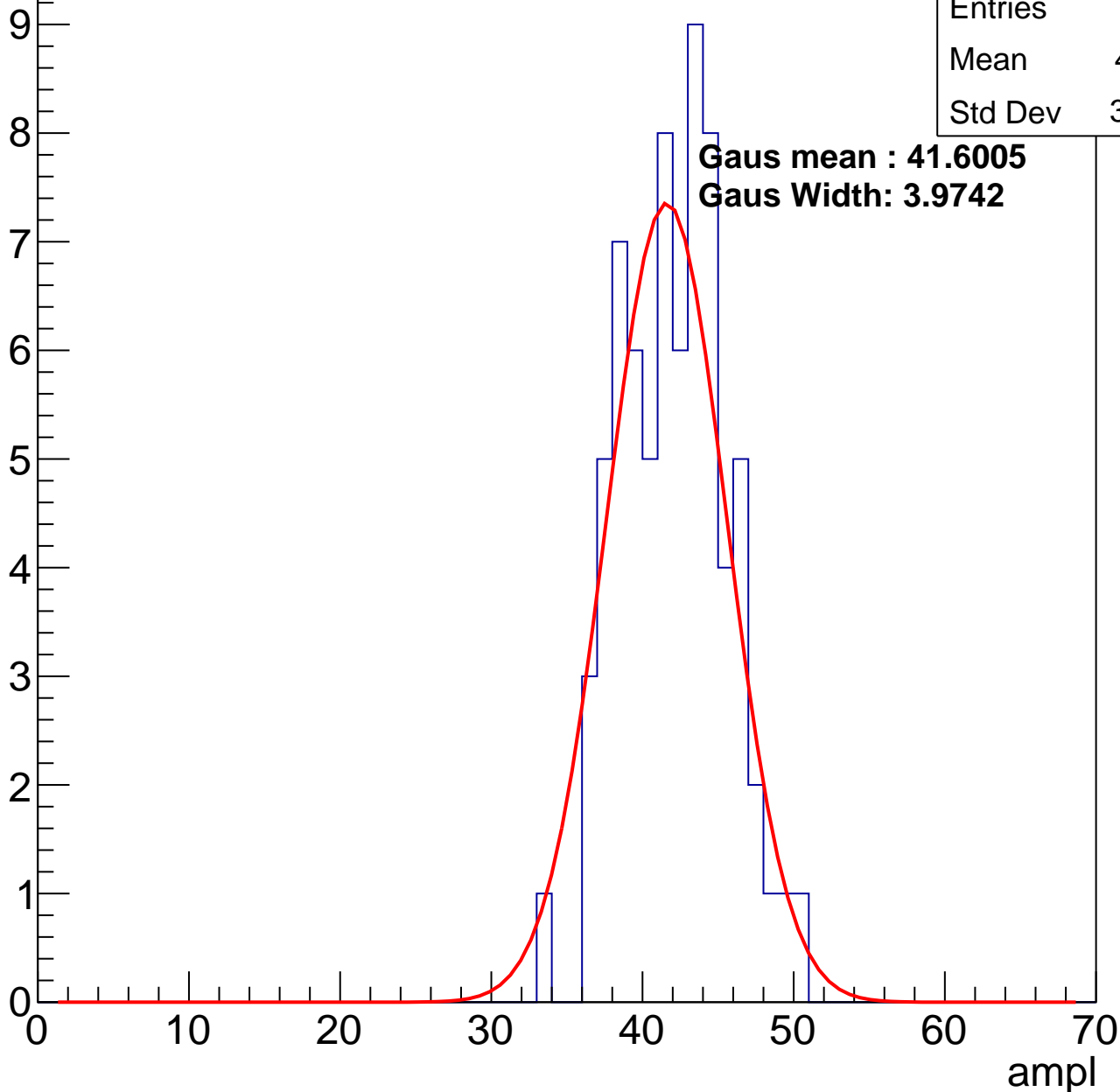
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	72
Mean	41.61
Std Dev	3.442

**Gaus mean : 41.6005**

**Gaus Width: 3.9742**

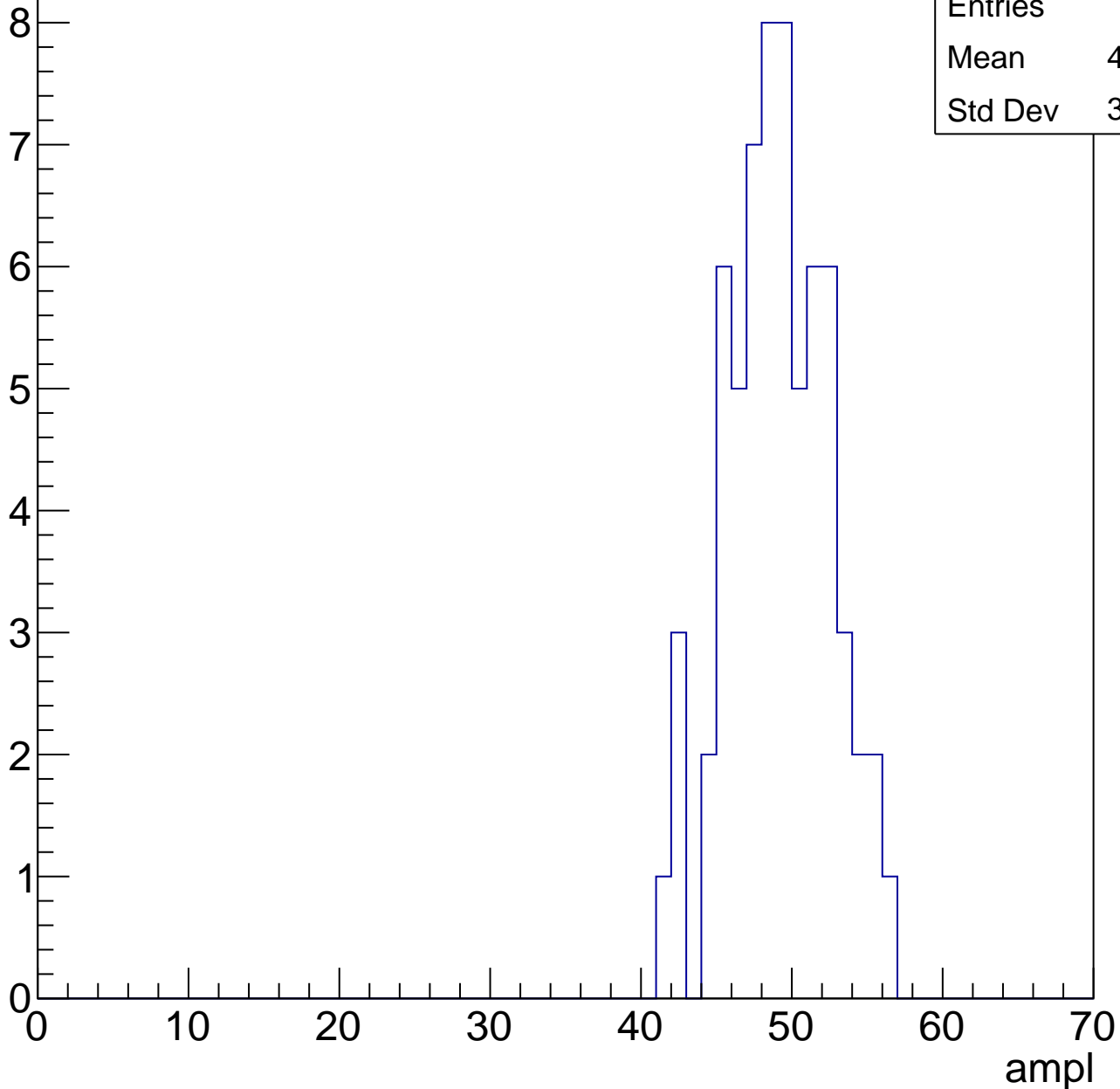


# B1L003S, U26-ch64, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	48.63
Std Dev	3.354

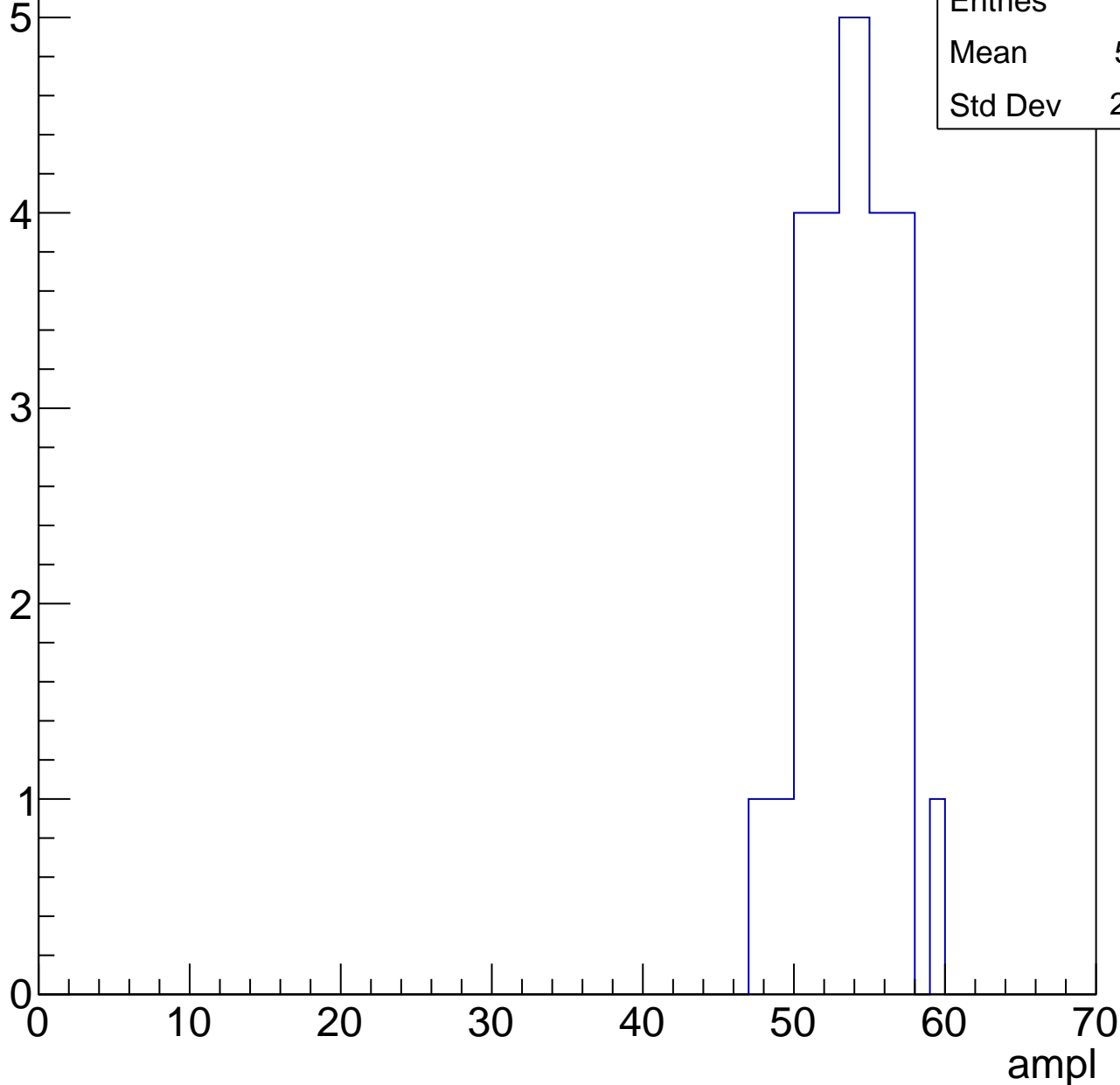


# B1L003S, U26-ch64, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	38
Mean	53.21
Std Dev	2.754



# B1L003S, U26-ch64, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

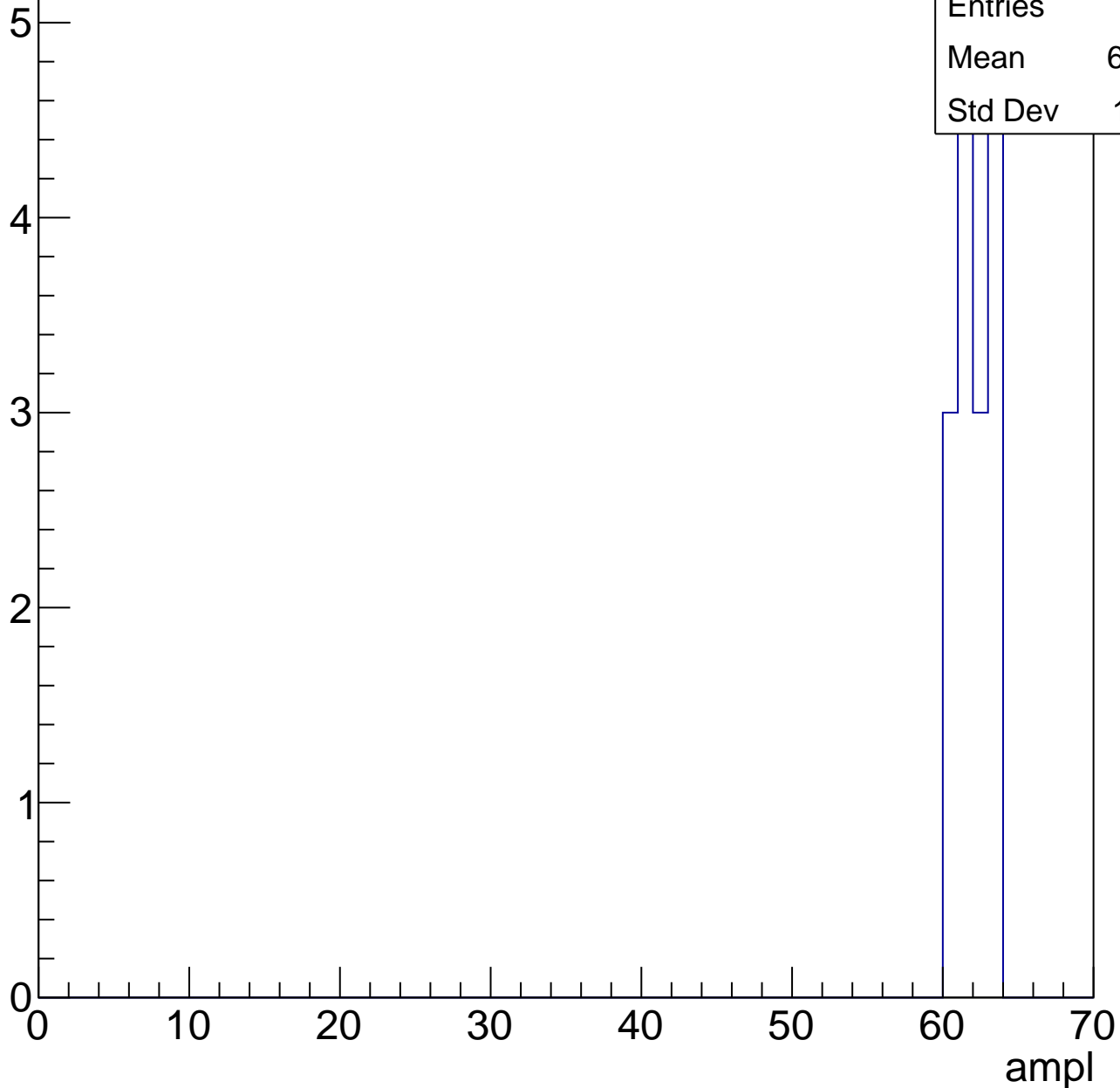
ampl

Entries	63
Mean	57.65
Std Dev	7.777

# B1L003S, U26-ch64, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch64, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U26-ch65, adc0

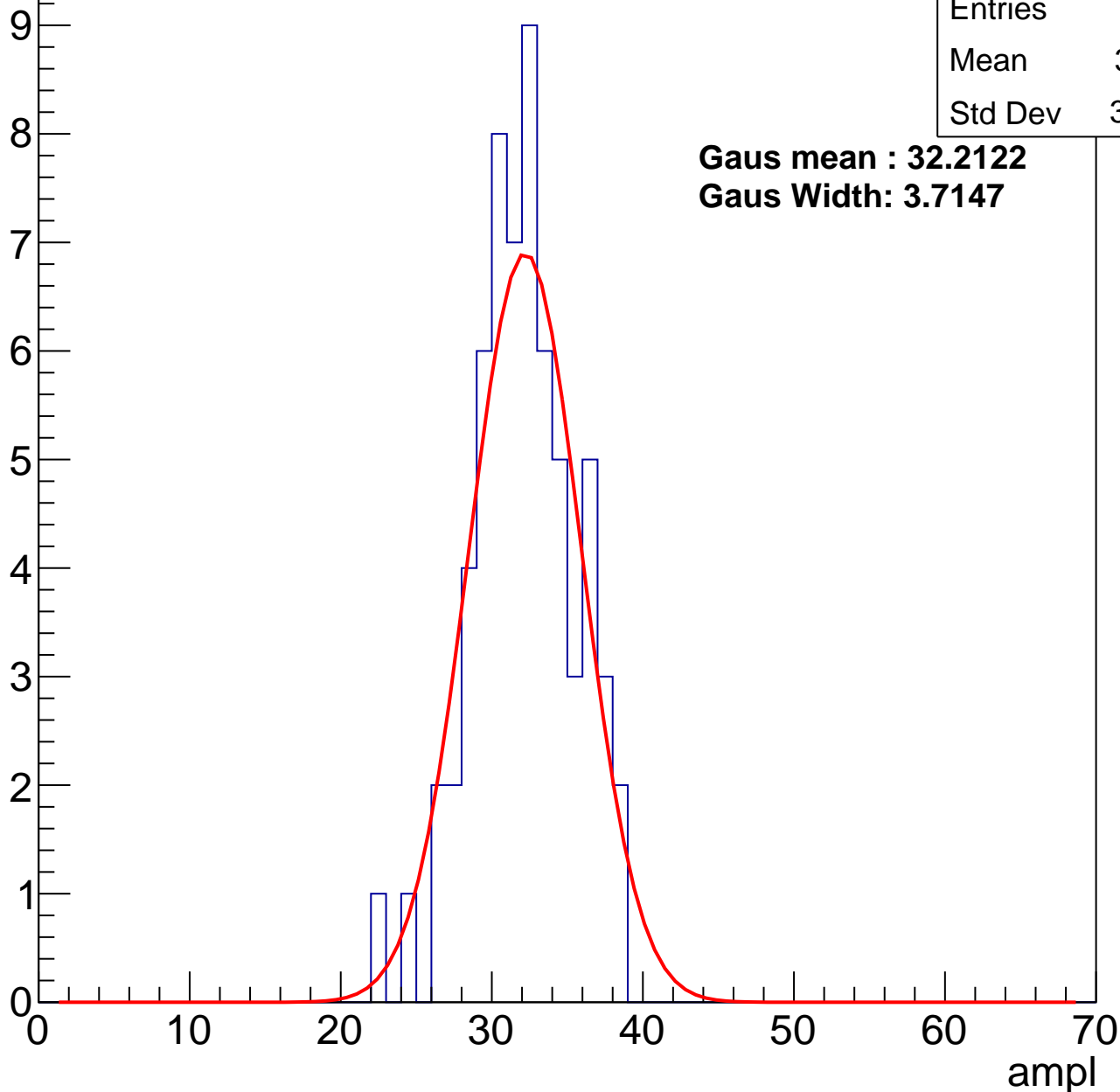
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	31.61
Std Dev	3.338

**Gaus mean : 32.2122**

**Gaus Width: 3.7147**



# B1L003S, U26-ch65, adc1

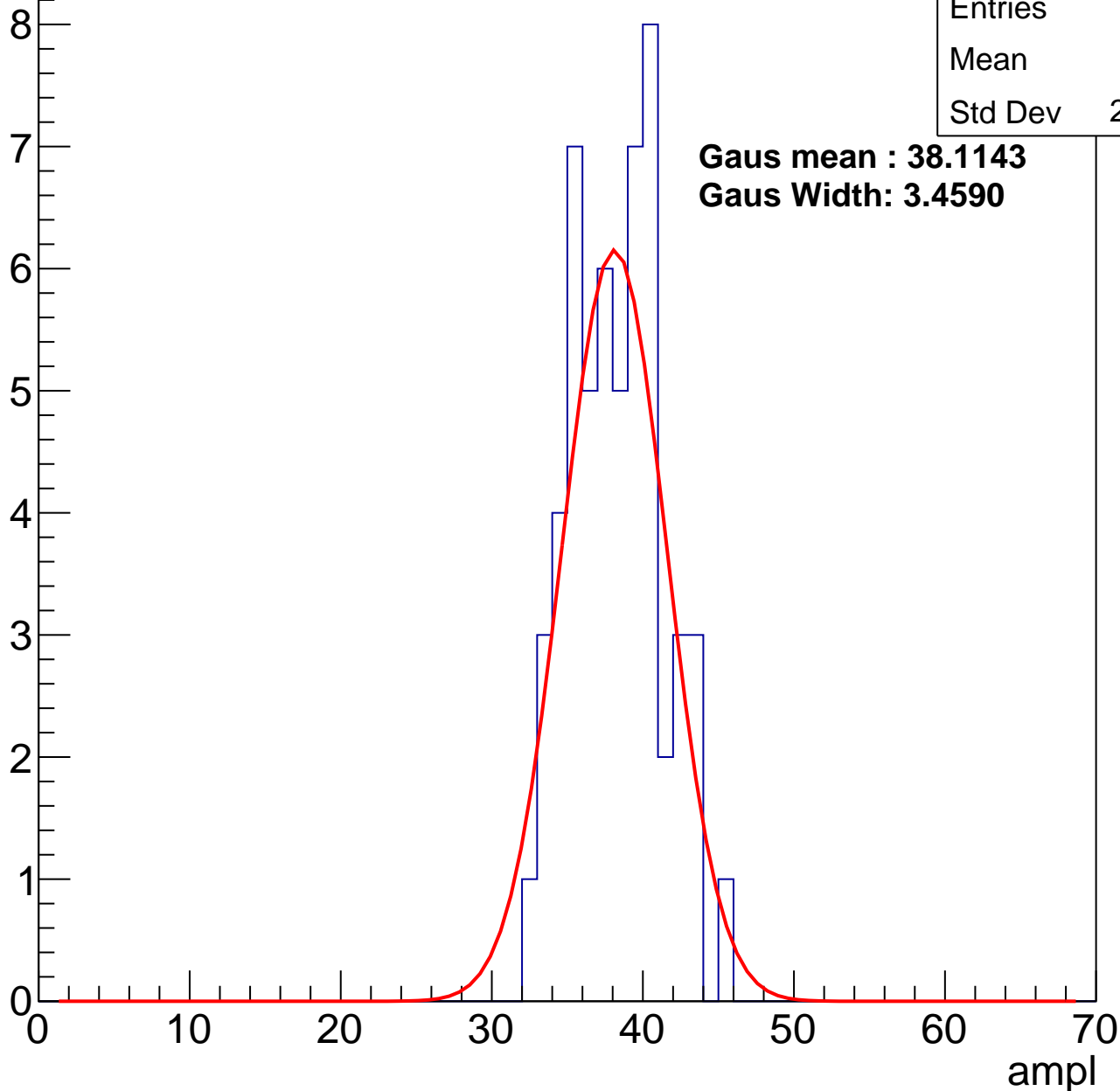
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	37.8
Std Dev	2.987

**Gaus mean : 38.1143**

**Gaus Width: 3.4590**



# B1L003S, U26-ch65, adc2

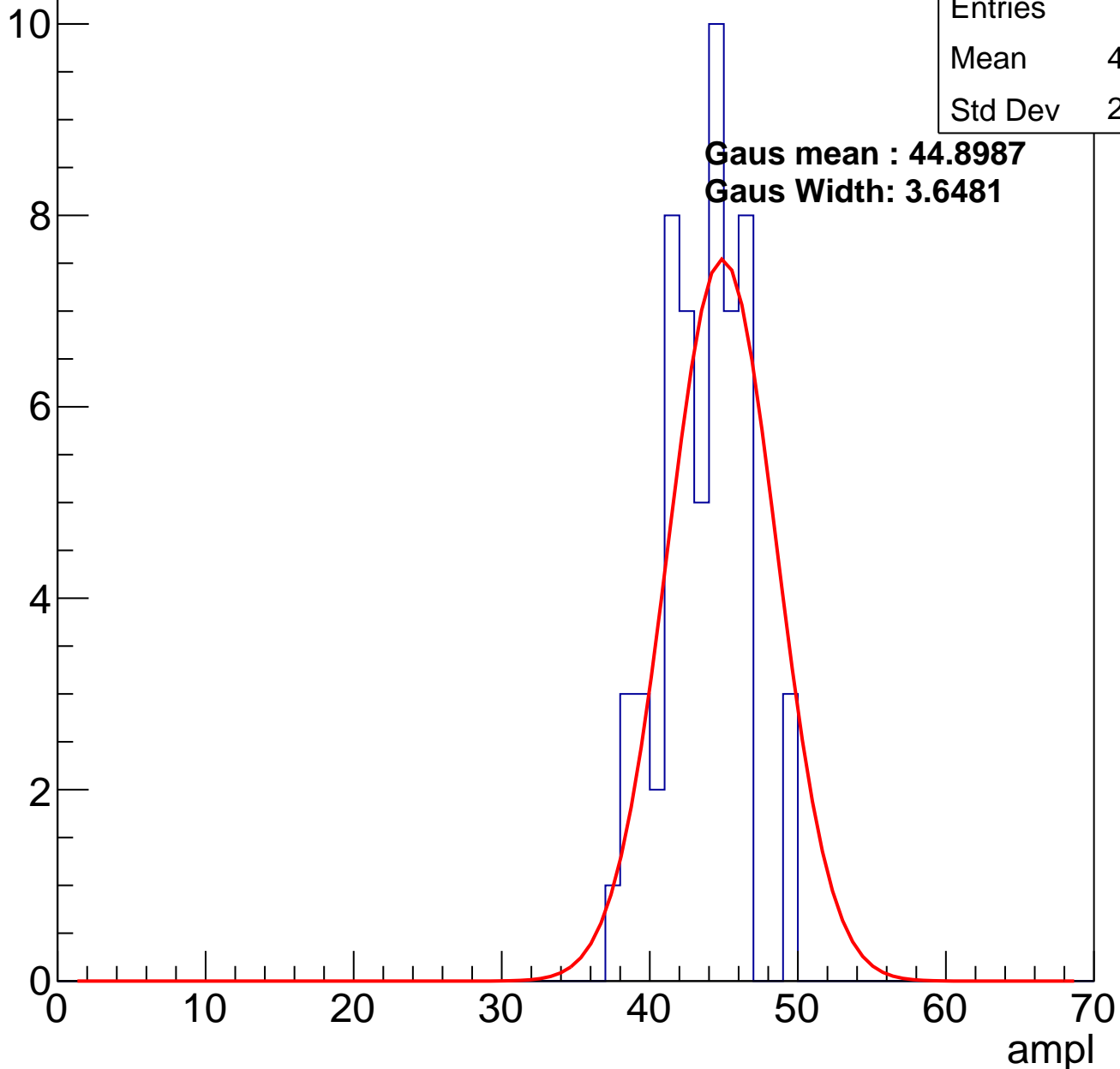
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	57
Mean	43.07
Std Dev	2.758

**Gaus mean : 44.8987**

**Gaus Width: 3.6481**

Entry



# B1L003S, U26-ch65, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

10

Entries 67

Mean 49.78

Std Dev 2.817

8

6

4

2

0

ampl

0

10

20

30

40

50

60

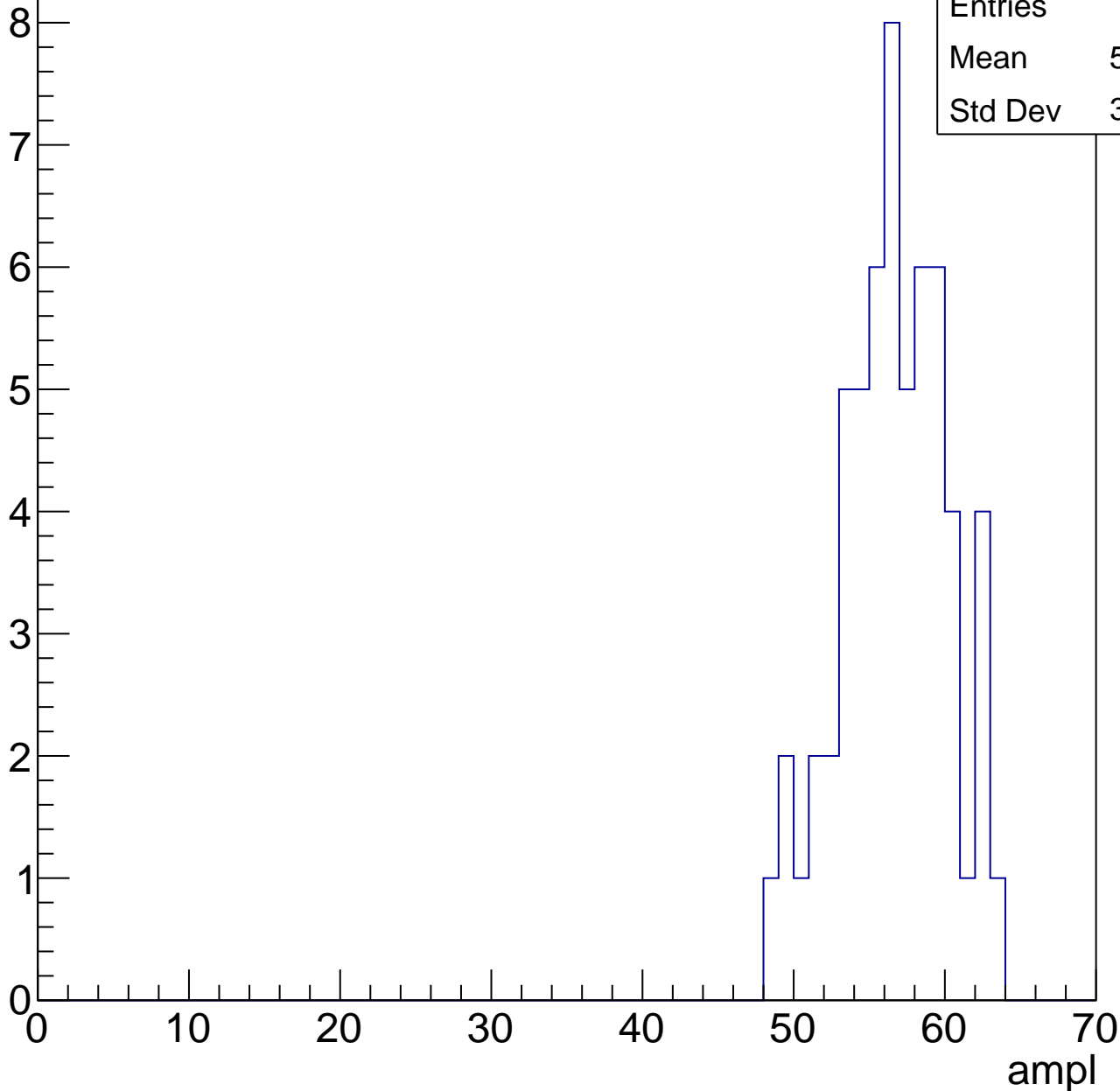
70

# B1L003S, U26-ch65, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	56.17
Std Dev	3.479



# B1L003S, U26-ch65, adc5

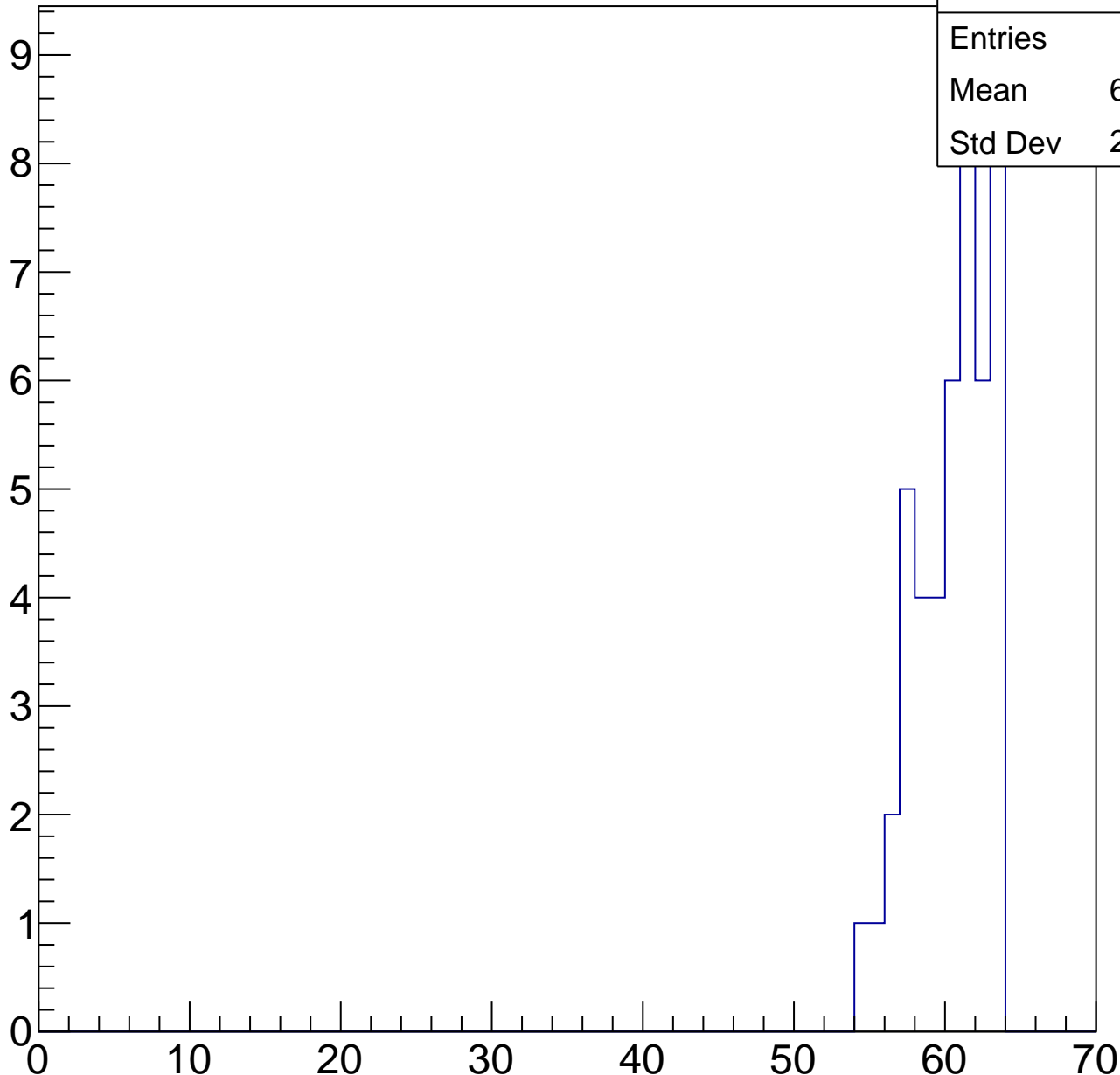
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	47
Mean	60.04
Std Dev	2.405

ampl



# B1L003S, U26-ch65, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0



# B1L003S, U26-ch65, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U26-ch66, adc0

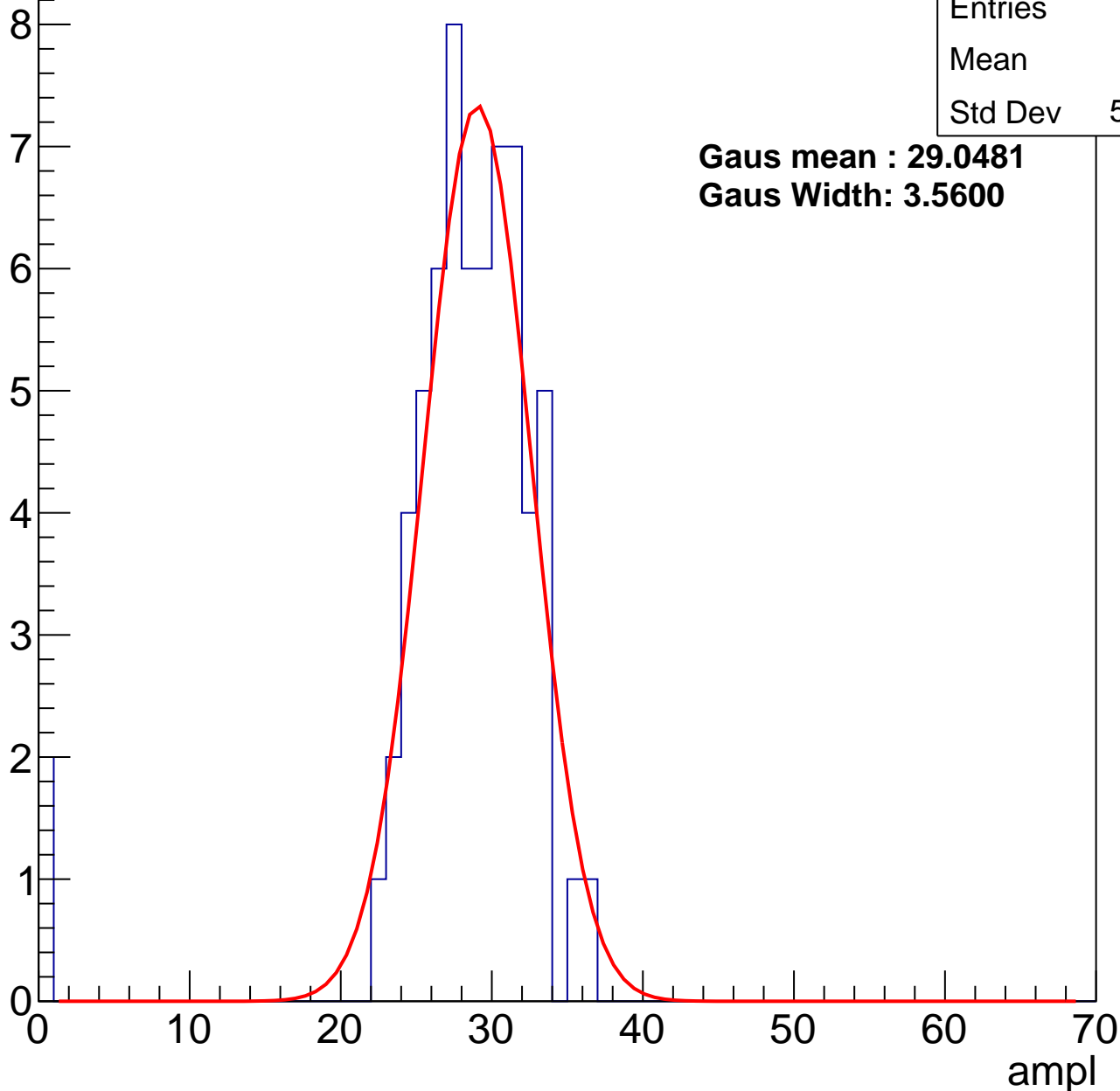
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	27.6
Std Dev	5.796

**Gaus mean : 29.0481**

**Gaus Width: 3.5600**



# B1L003S, U26-ch66, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	75
Mean	35.37
Std Dev	3.532

**Gaus mean : 35.7000**

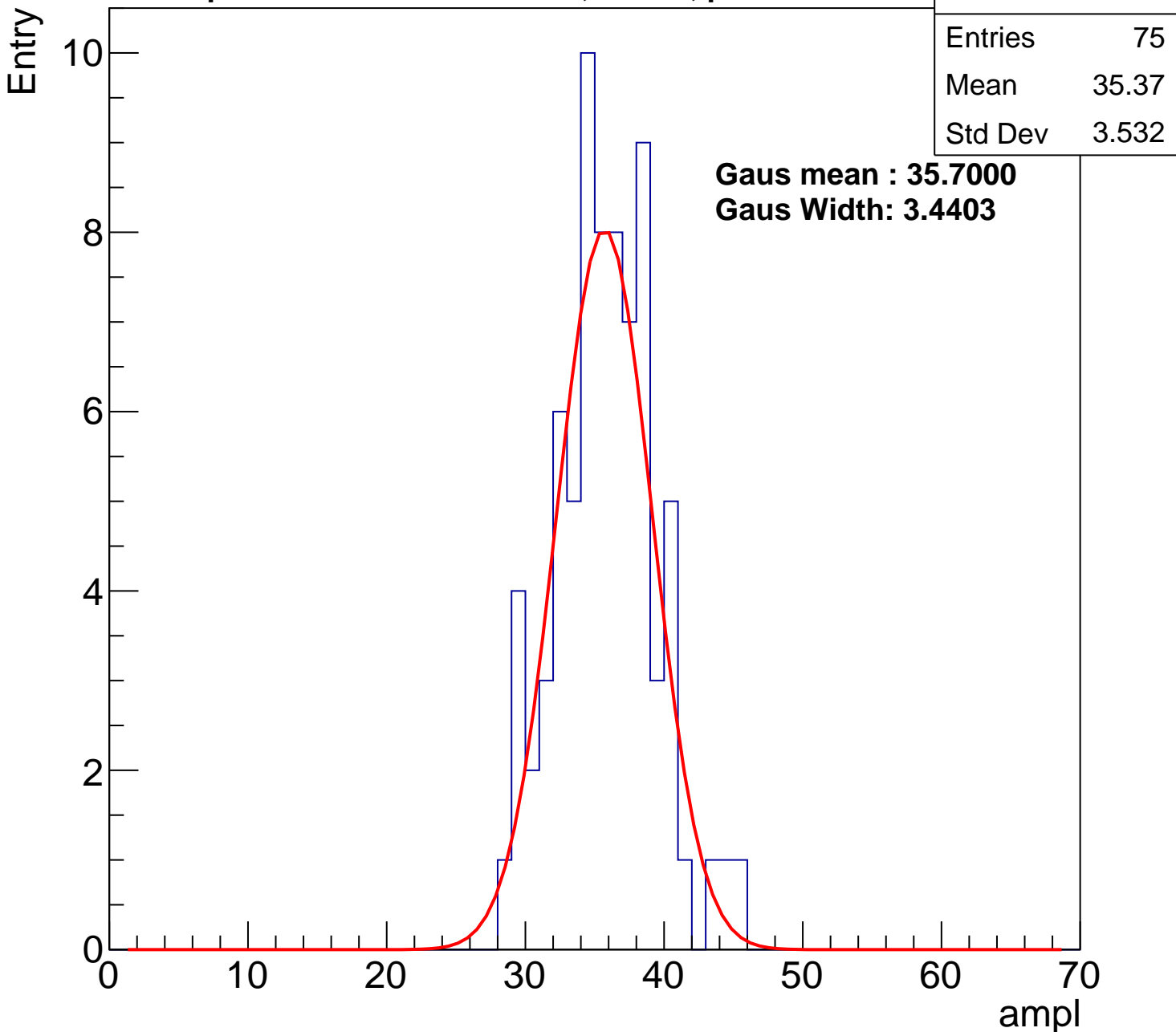
**Gaus Width: 3.4403**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L003S, U26-ch66, adc2

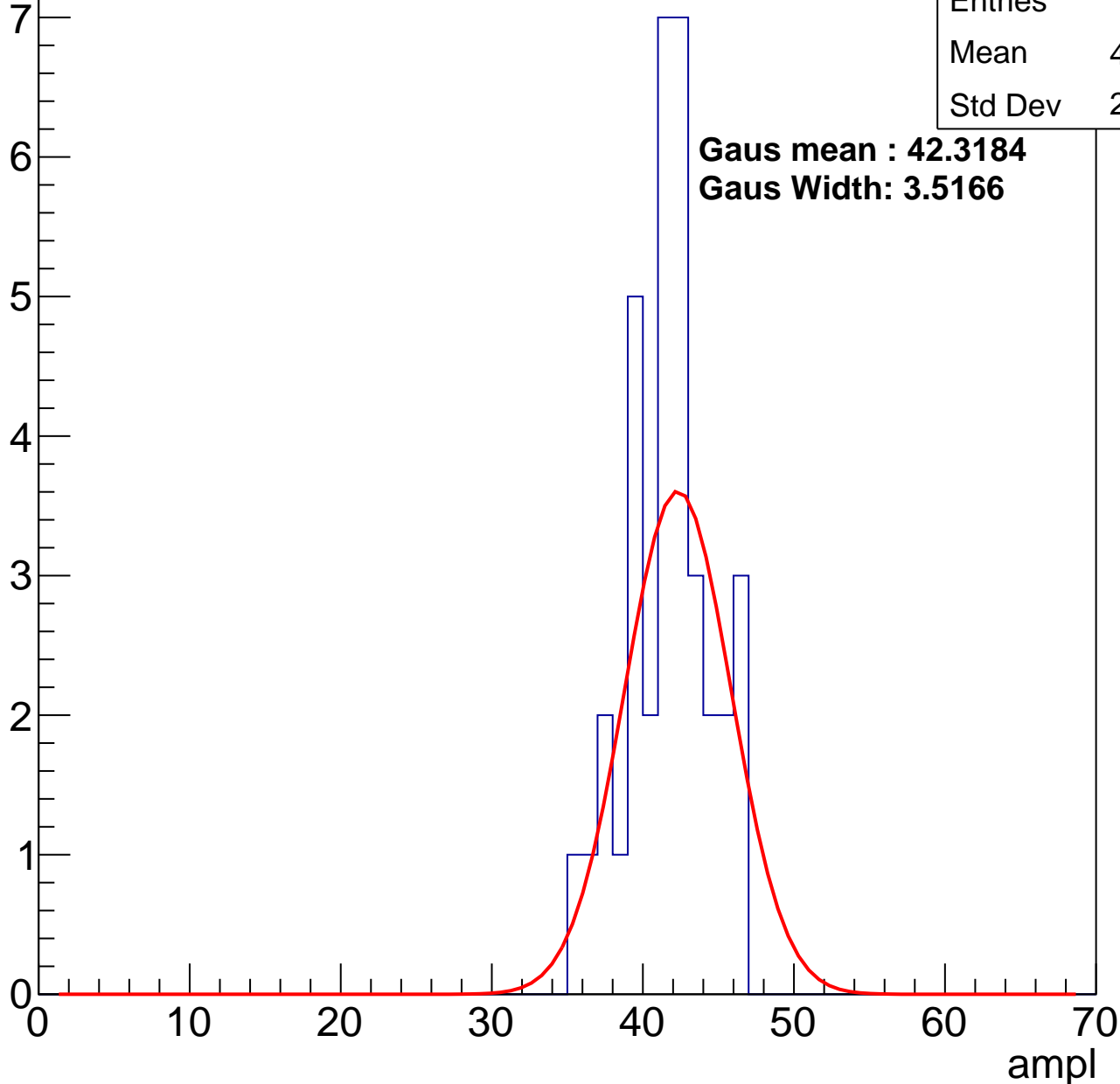
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	36
Mean	41.22
Std Dev	2.719

**Gaus mean : 42.3184**

**Gaus Width: 3.5166**



# B1L003S, U26-ch66, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

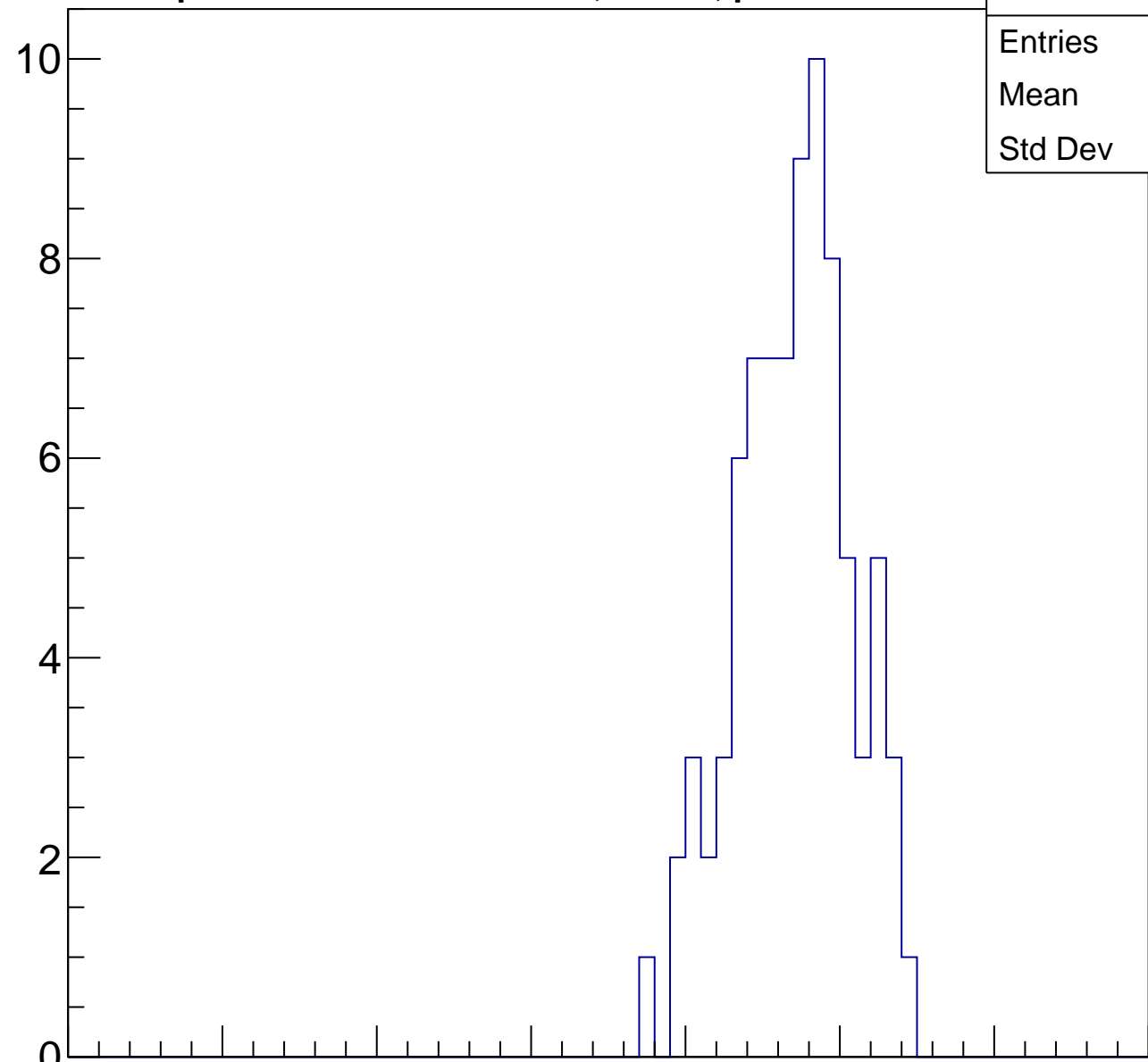
Entries	82
Mean	46.55
Std Dev	3.69

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

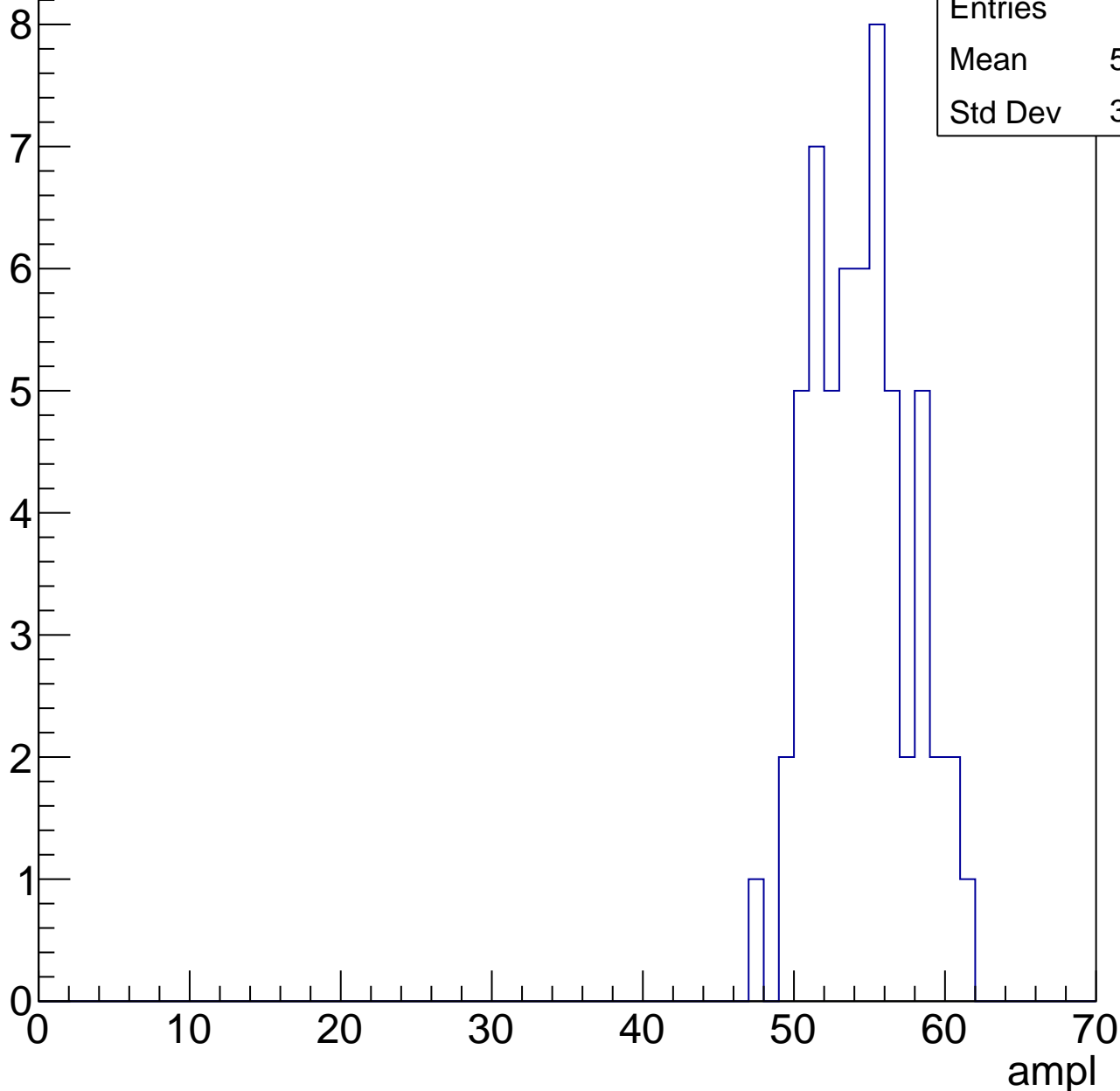


# B1L003S, U26-ch66, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

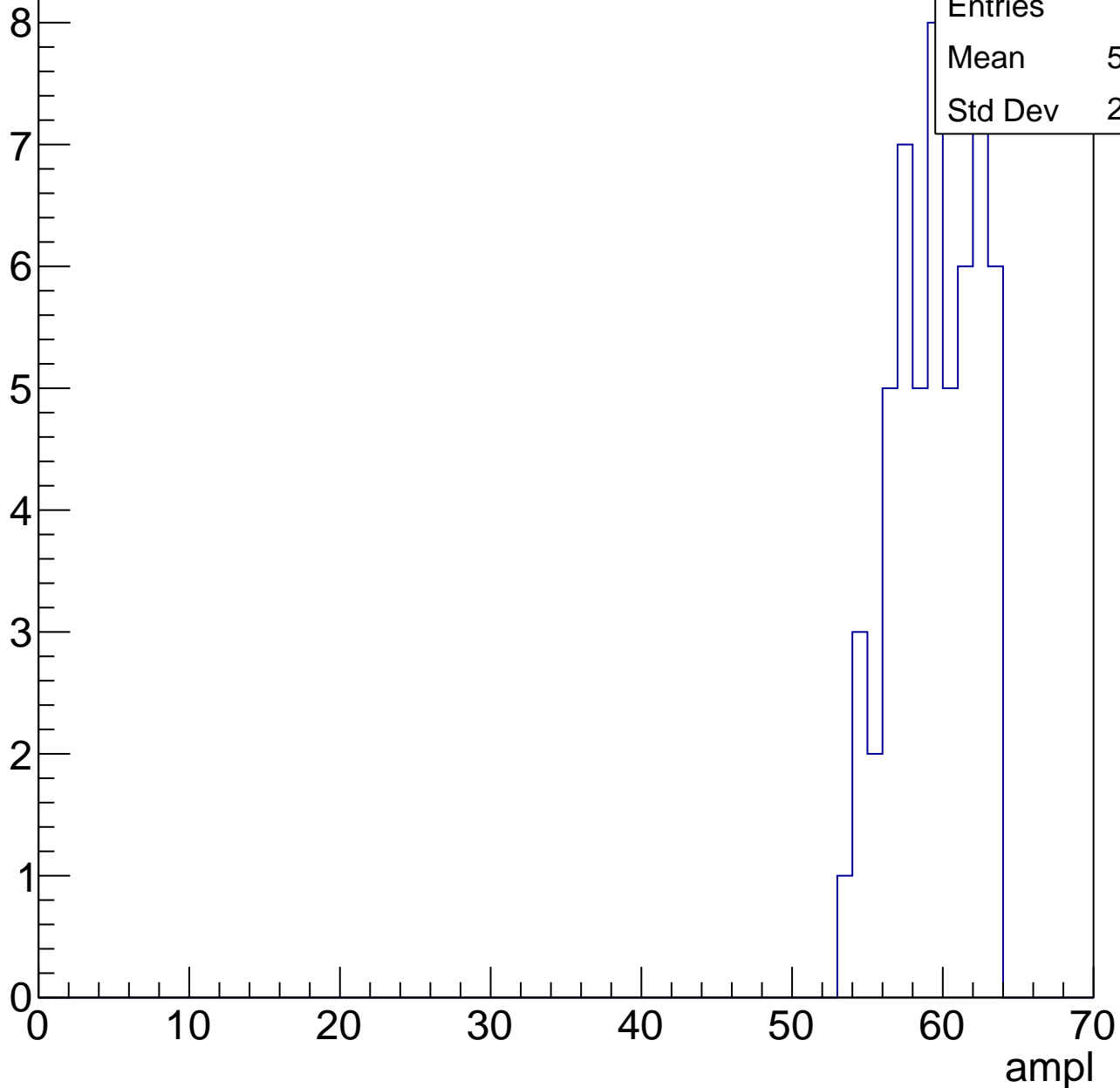
Entries	57
Mean	53.98
Std Dev	3.148



# B1L003S, U26-ch66, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

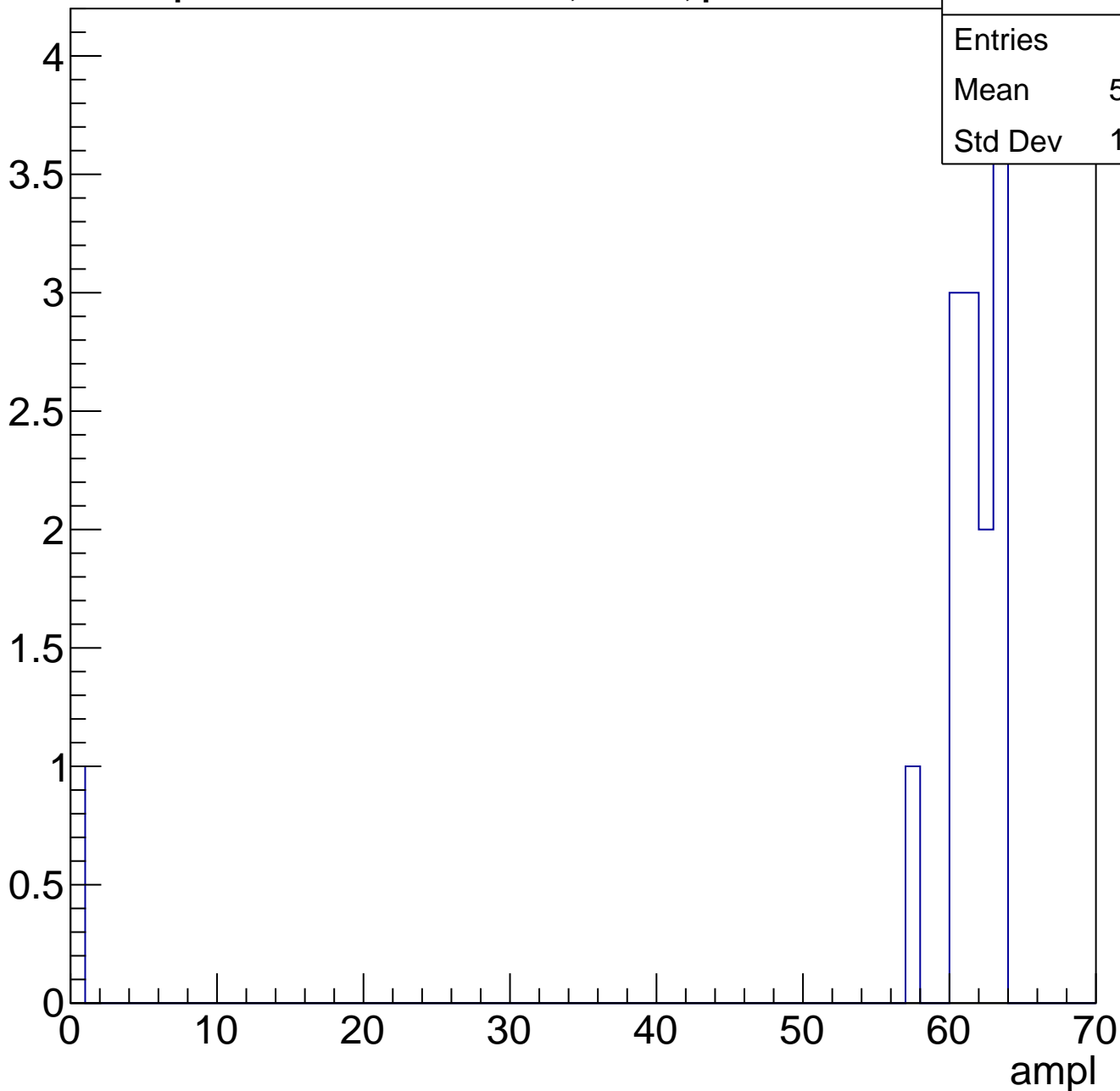
Entry



# B1L003S, U26-ch66, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	14
Mean	56.86
Std Dev	15.85



# B1L003S, U26-ch66, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	3
Mean	7.333
Std Dev	10.37

# B1L003S, U26-ch67, adc0

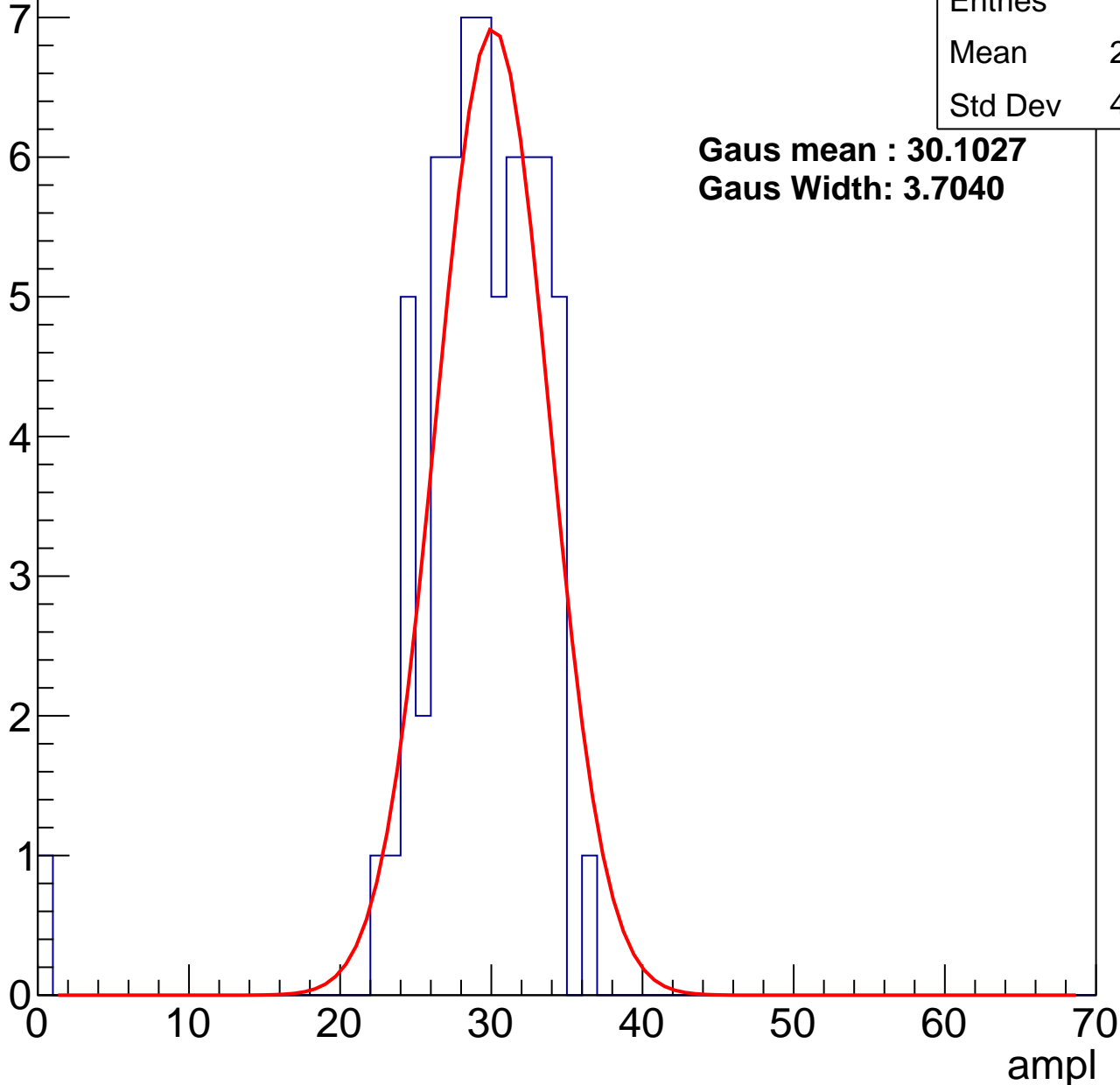
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	28.68
Std Dev	4.827

**Gaus mean : 30.1027**

**Gaus Width: 3.7040**



# B1L003S, U26-ch67, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	68
Mean	35.82
Std Dev	3.539

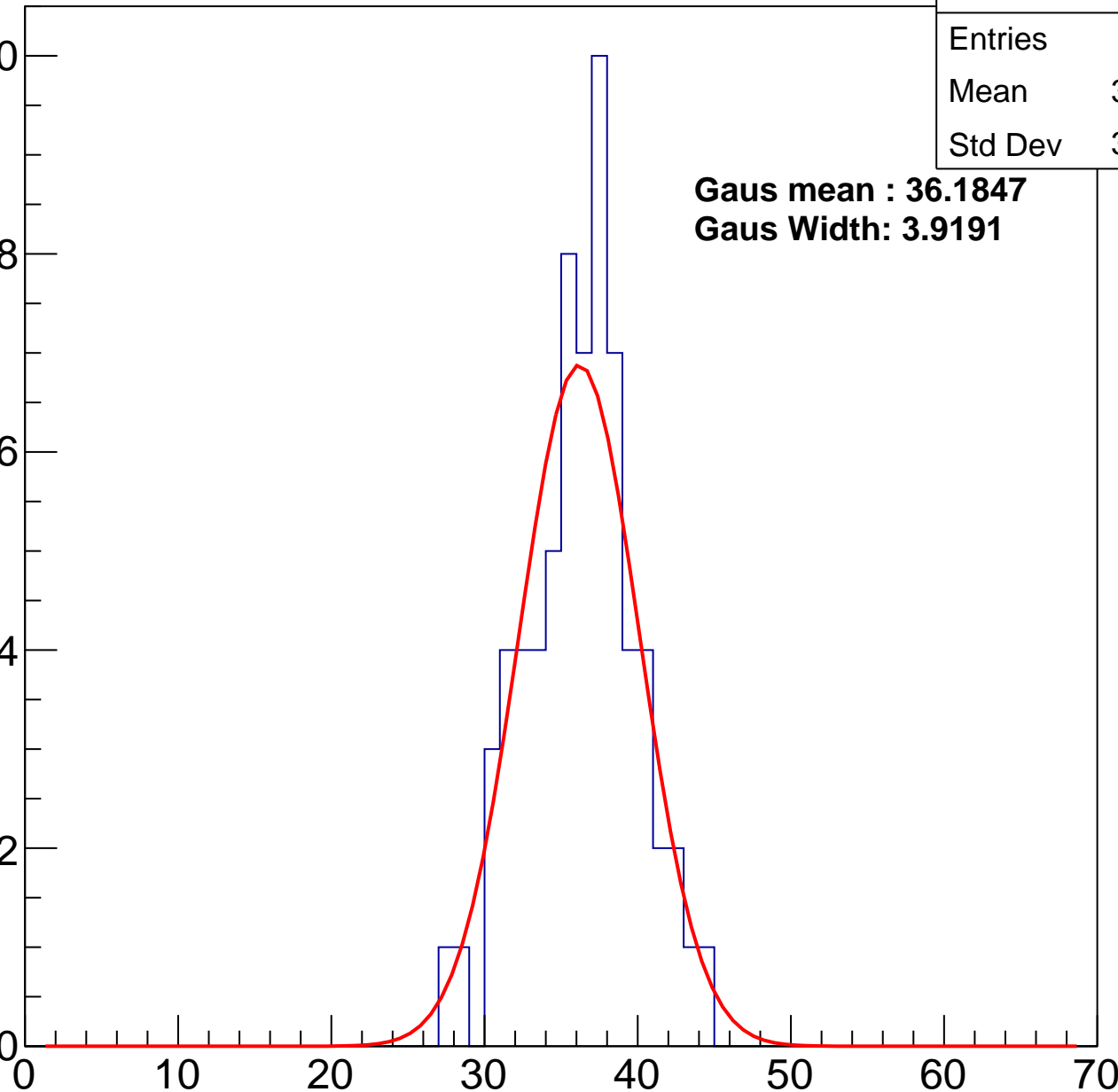
**Gaus mean : 36.1847**

**Gaus Width: 3.9191**

Entry

10  
8  
6  
4  
2  
0

ampl



# B1L003S, U26-ch67, adc2

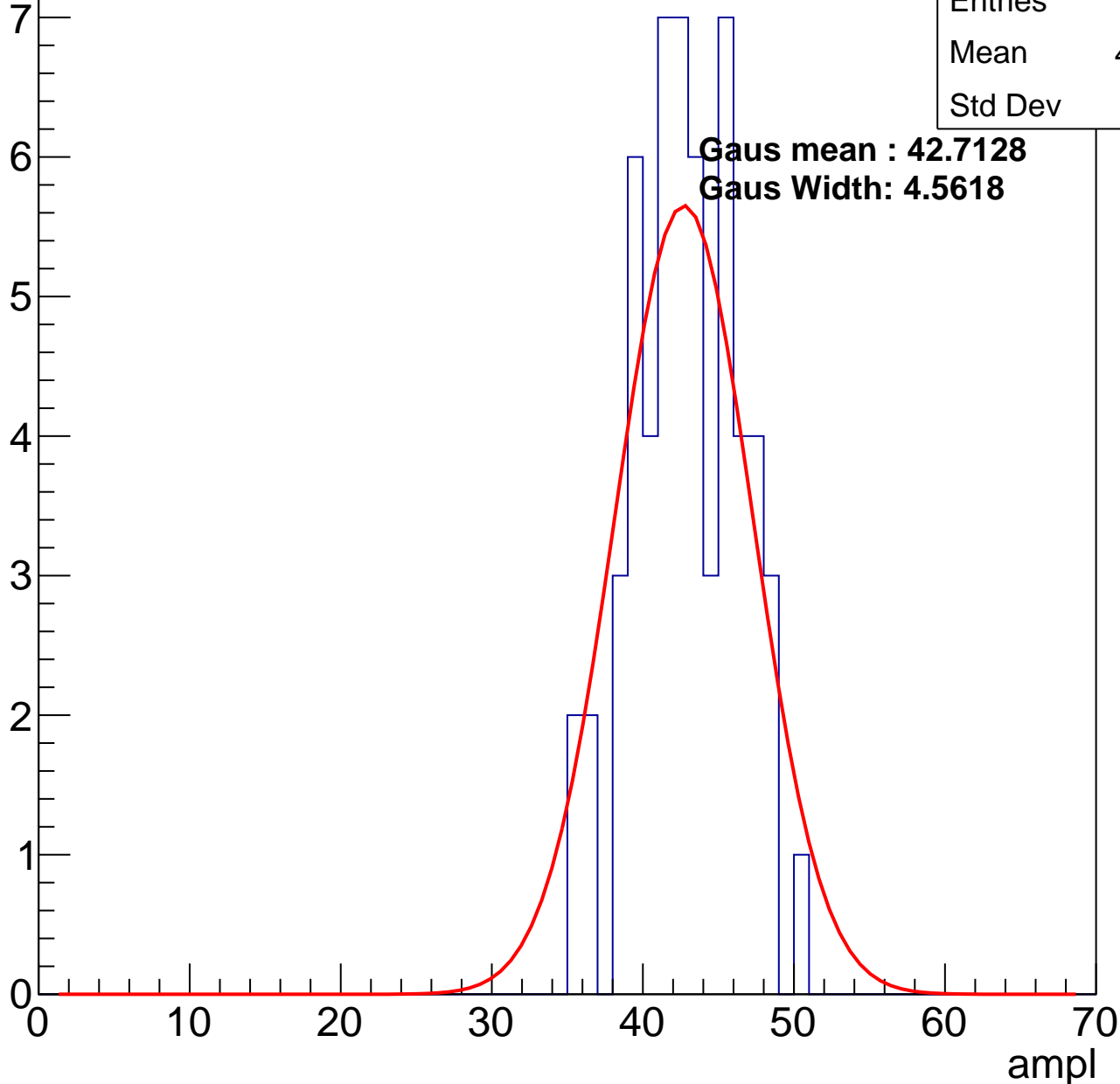
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	42.41
Std Dev	3.45

**Gaus mean : 42.7128**

**Gaus Width: 4.5618**

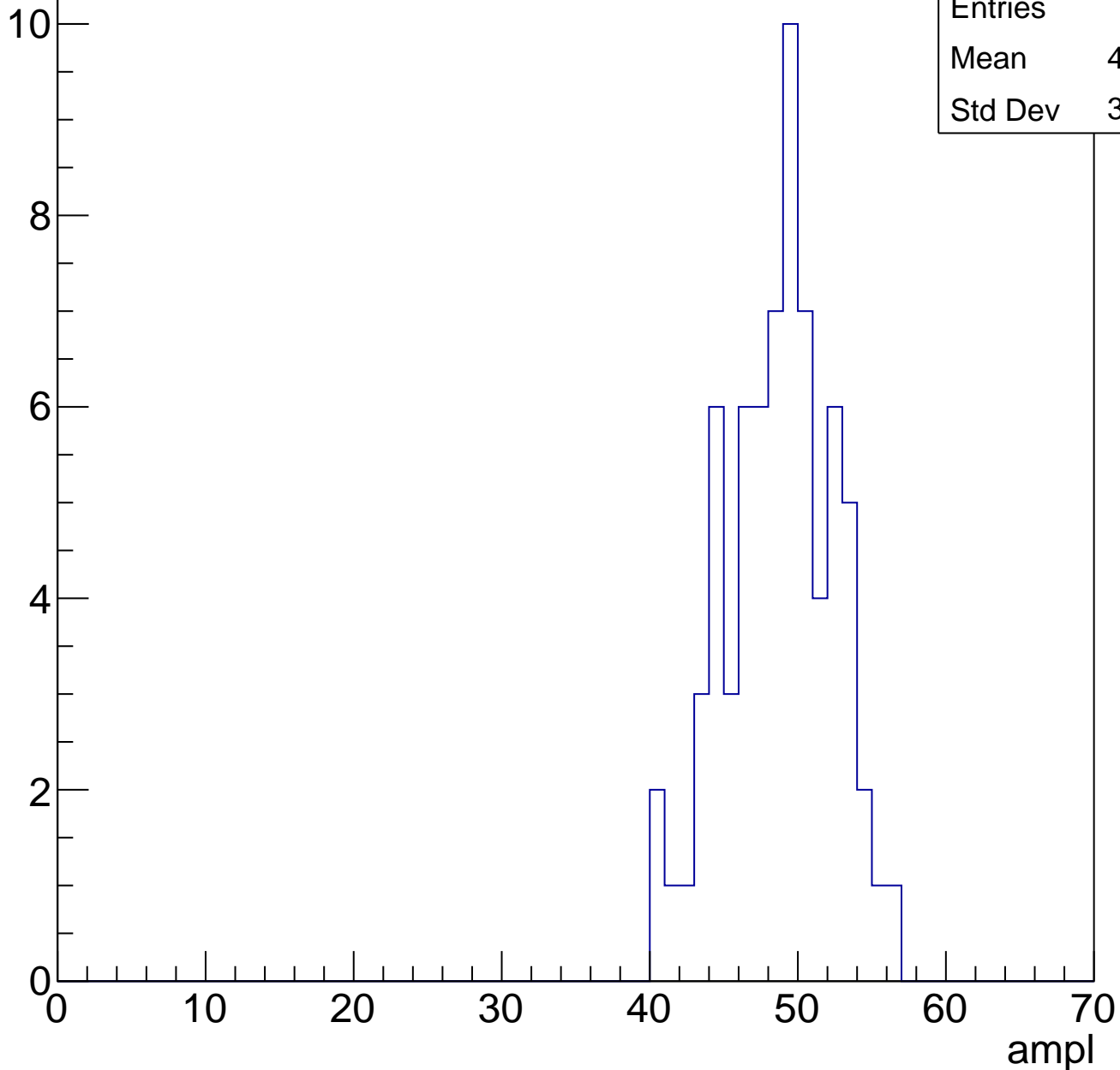


# B1L003S, U26-ch67, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	71
Mean	48.24
Std Dev	3.594

Entry



# B1L003S, U26-ch67, adc4

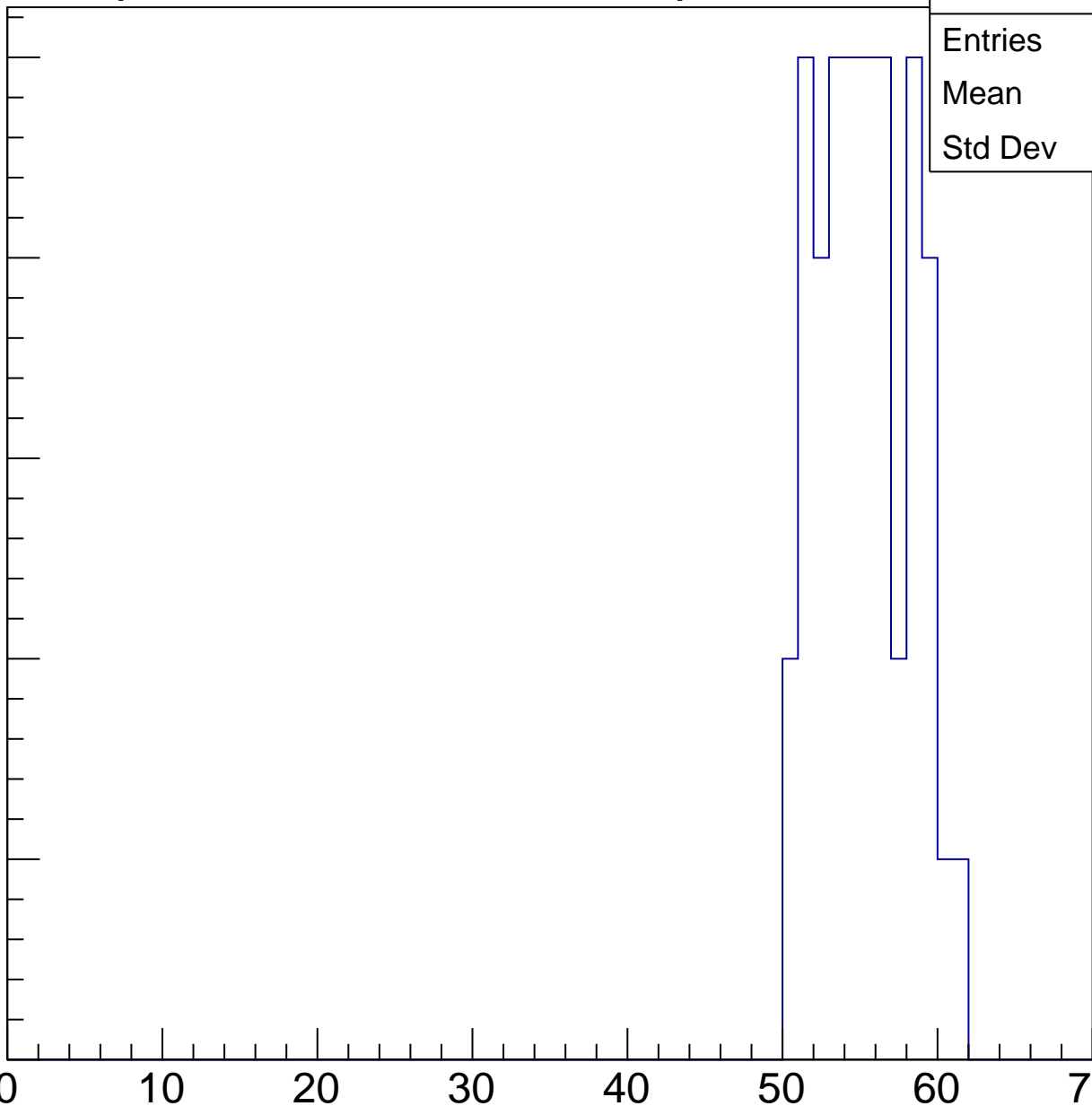
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

5  
4  
3  
2  
1  
0

Entries	44
Mean	54.86
Std Dev	2.912

ampl

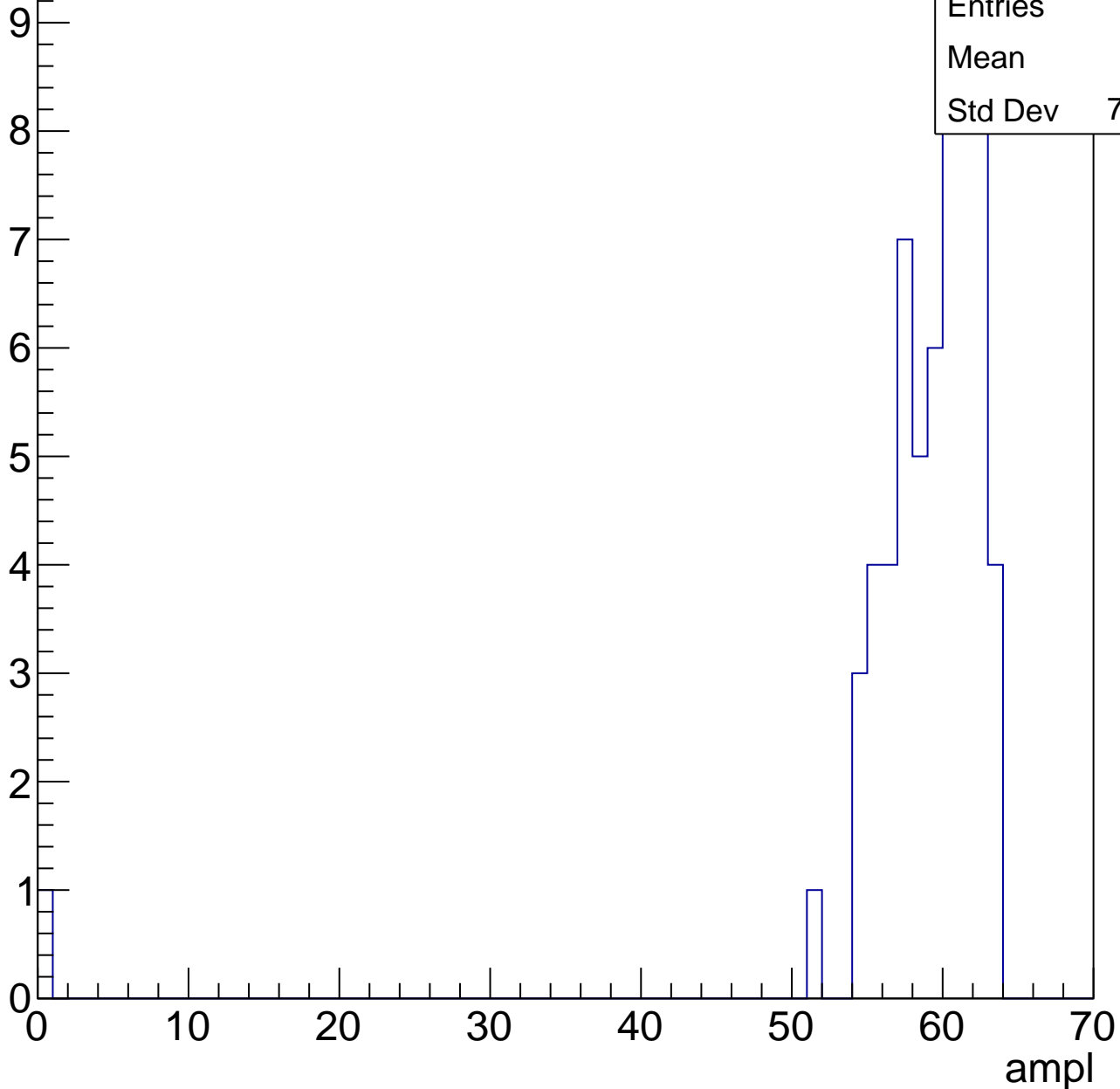


# B1L003S, U26-ch67, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	58
Std Dev	7.973

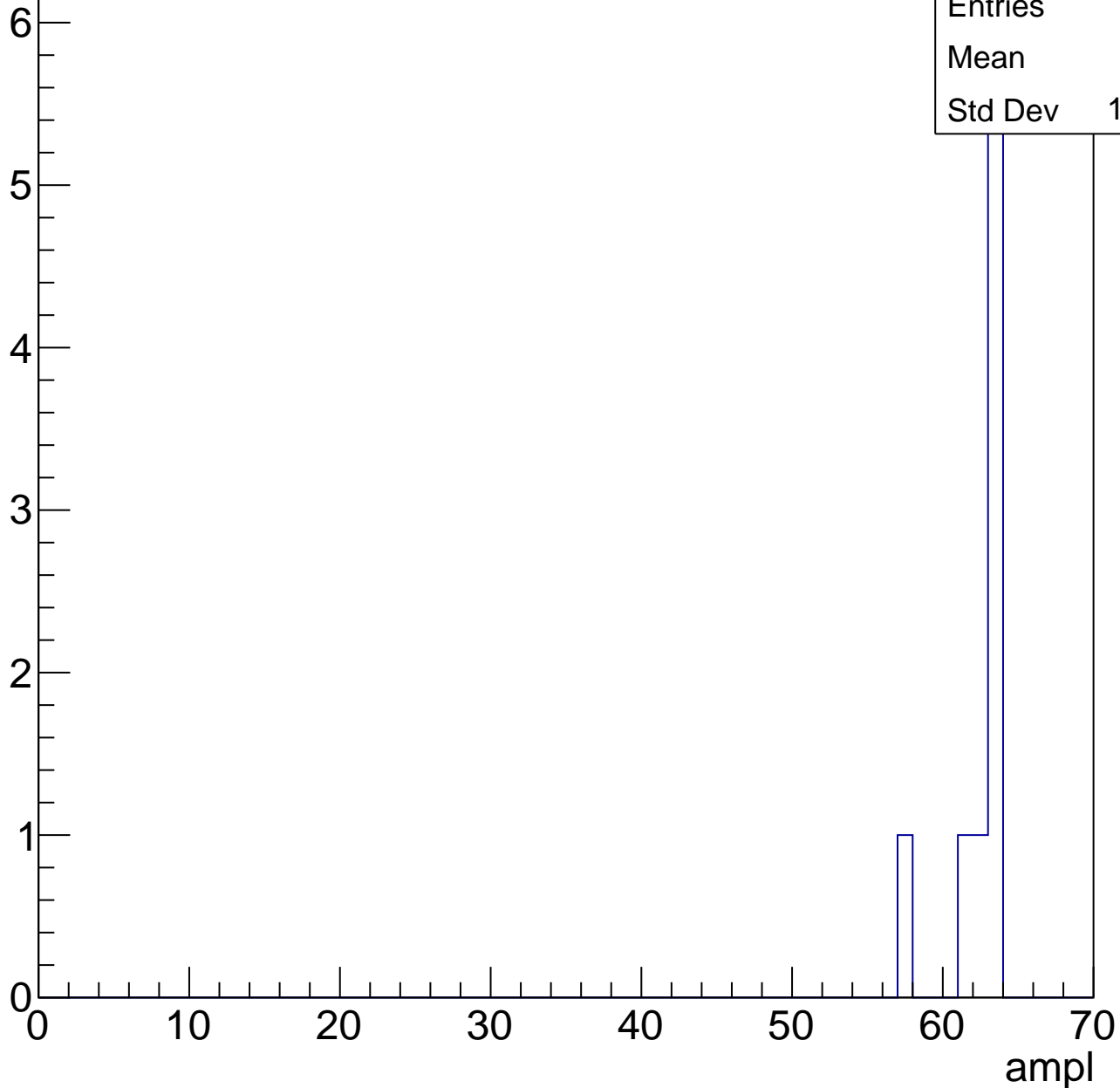


# B1L003S, U26-ch67, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	9
Mean	62
Std Dev	1.886





# B1L003S, U26-ch67, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	22
Std Dev	0

ampl

# B1L003S, U26-ch68, adc0

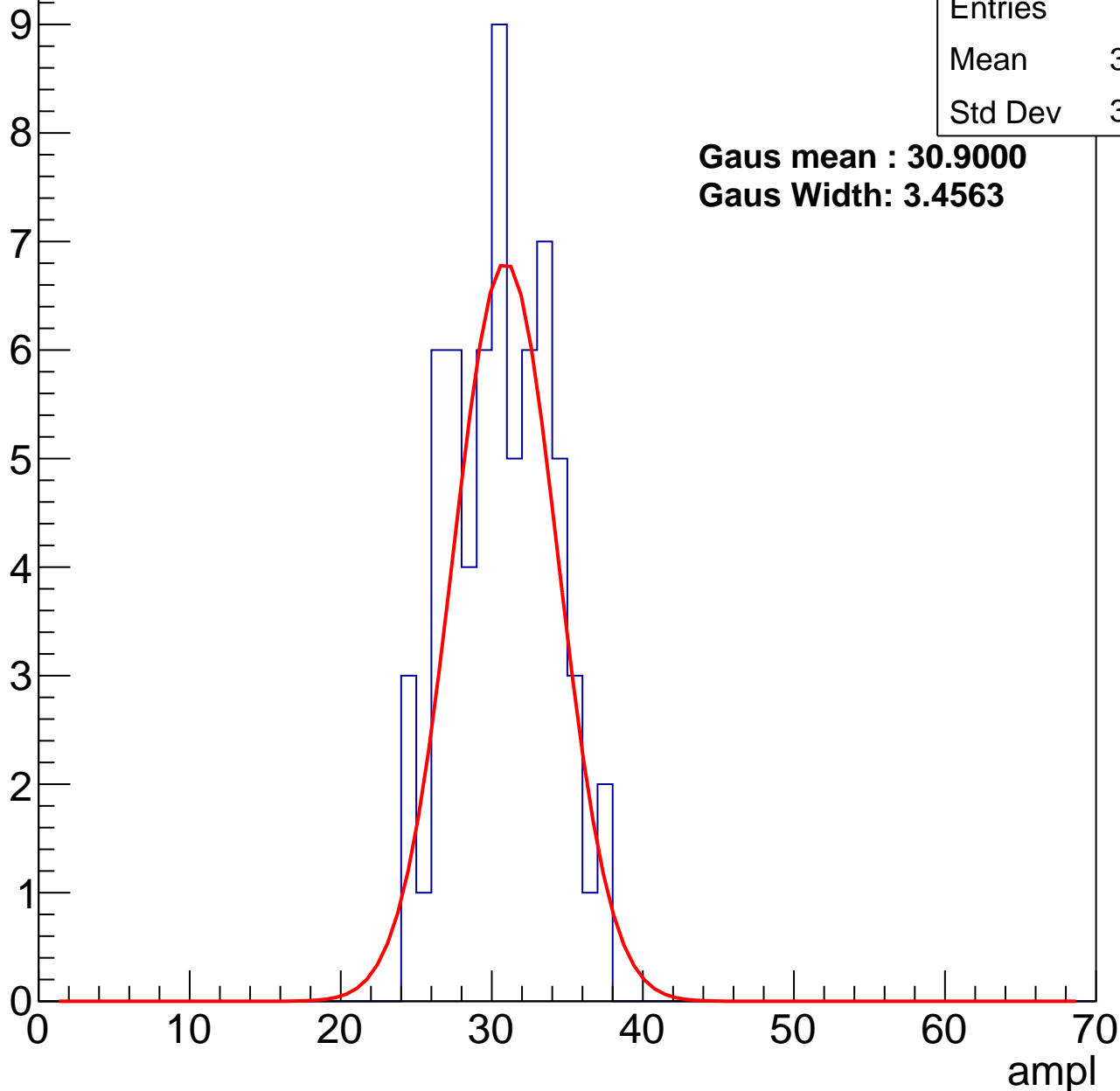
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	30.22
Std Dev	3.267

**Gaus mean : 30.9000**

**Gaus Width: 3.4563**



# B1L003S, U26-ch68, adc1

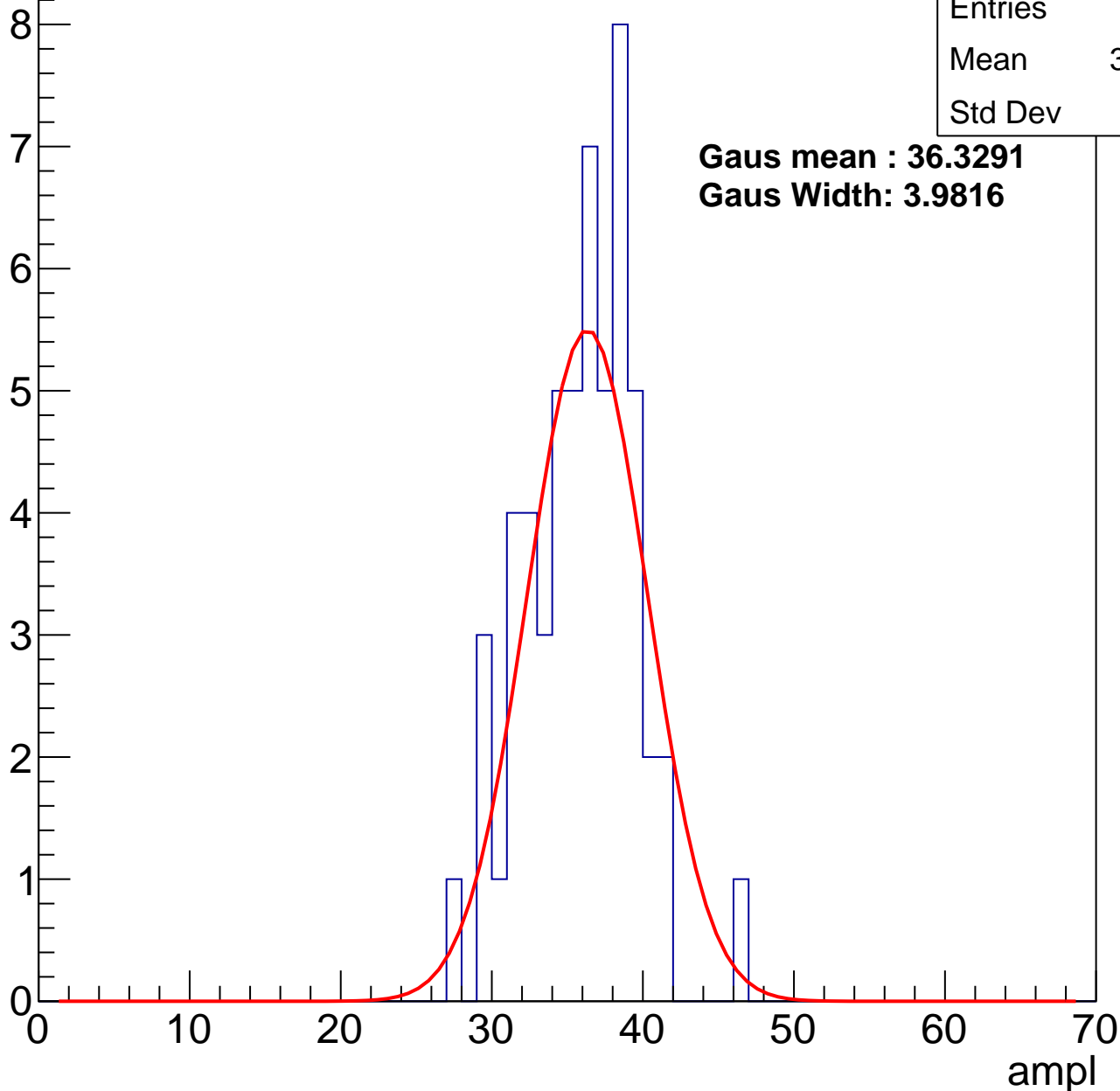
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	35.43
Std Dev	3.6

**Gaus mean : 36.3291**

**Gaus Width: 3.9816**



# B1L003S, U26-ch68, adc2

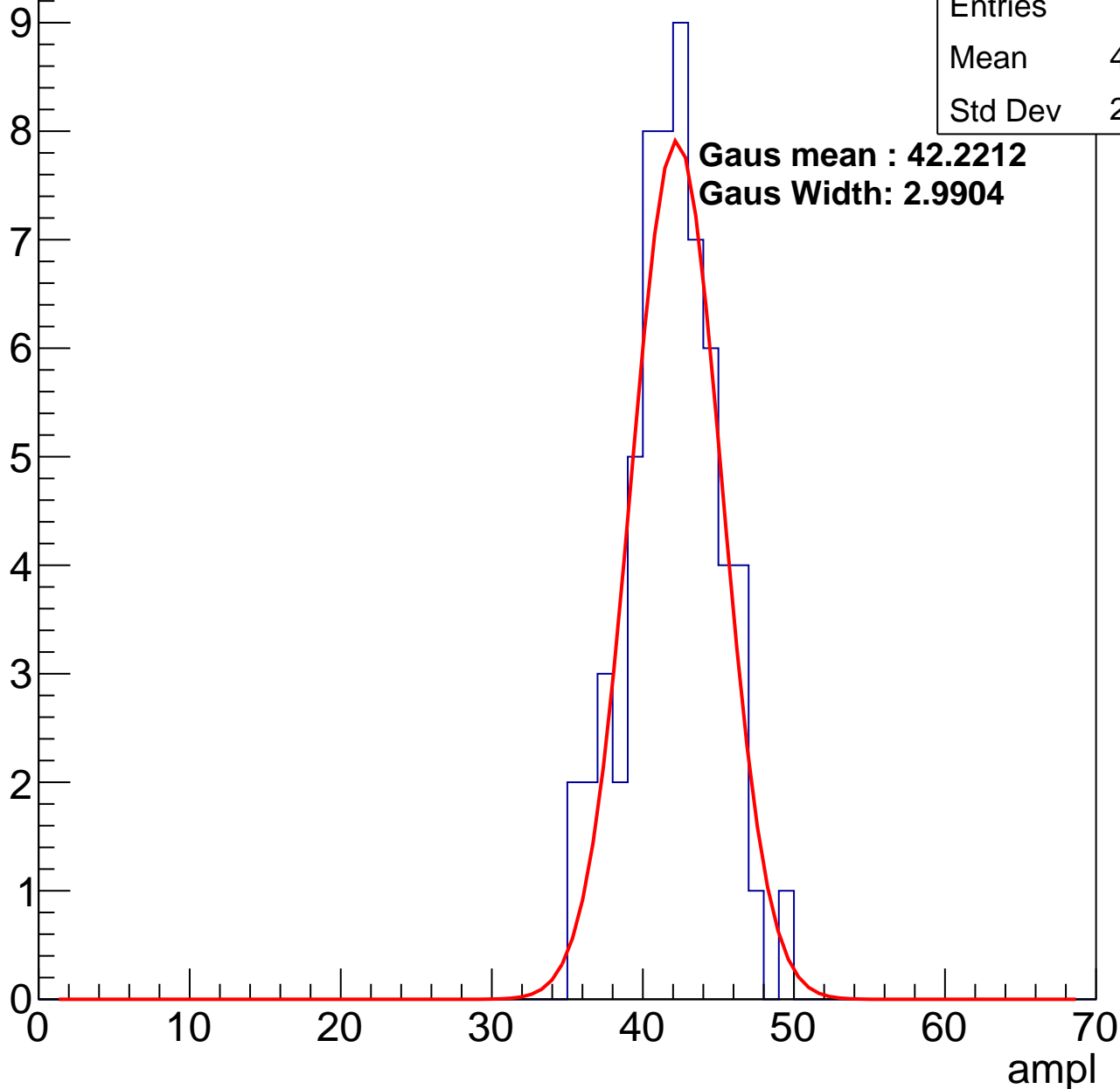
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	41.53
Std Dev	2.988

**Gaus mean : 42.2212**

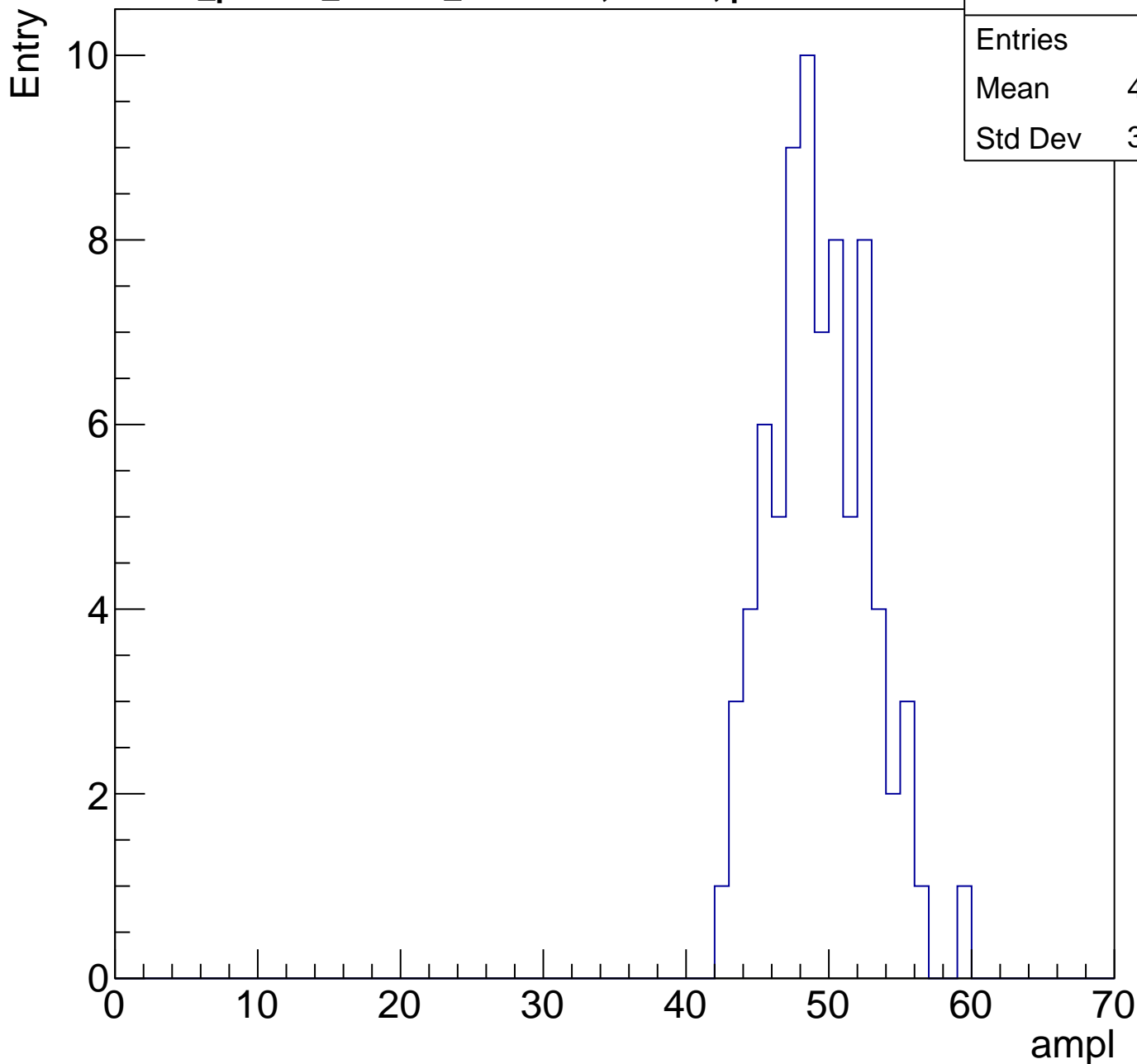
**Gaus Width: 2.9904**



# B1L003S, U26-ch68, adc3

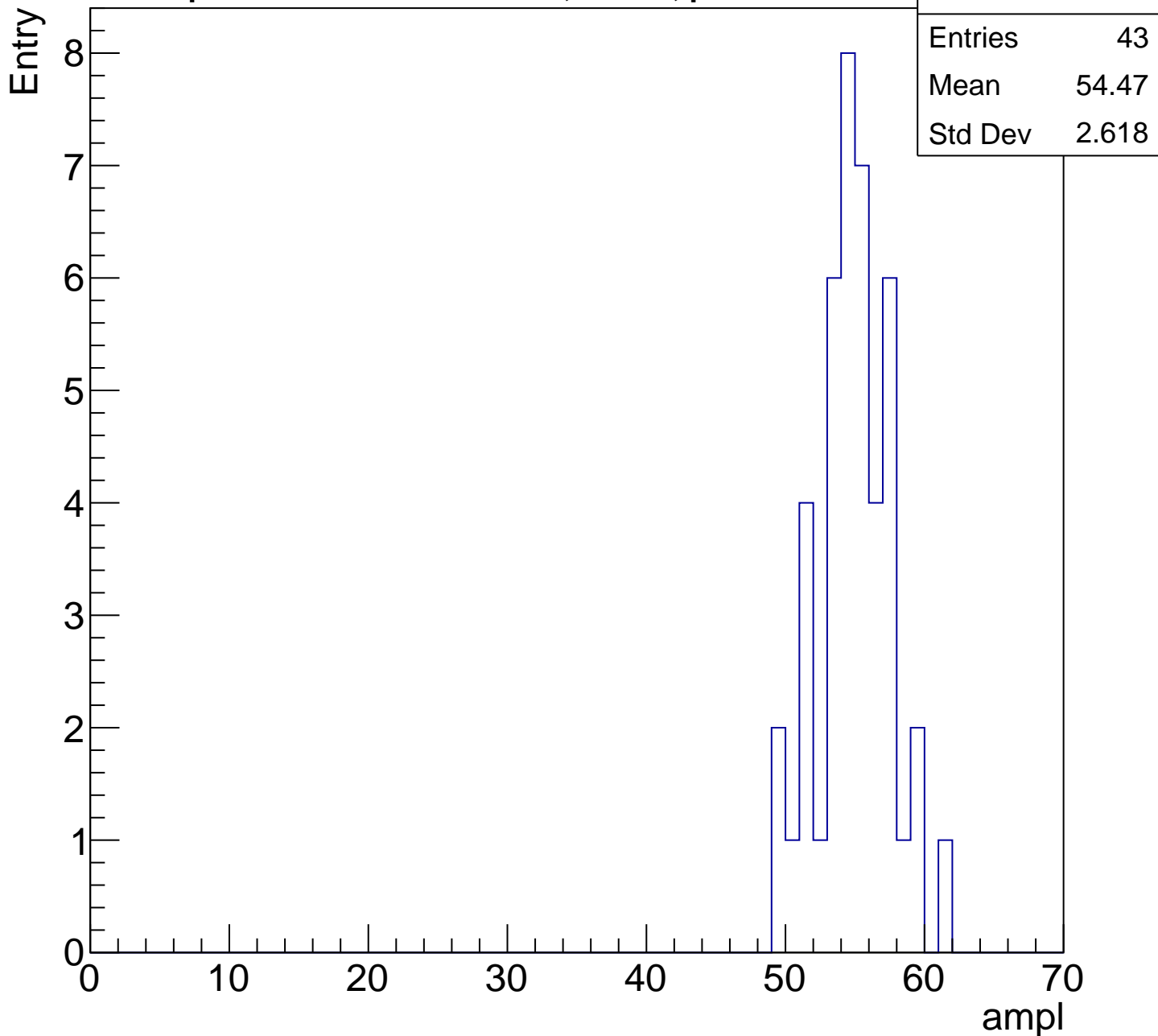
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	77
Mean	48.88
Std Dev	3.445



# B1L003S, U26-ch68, adc4

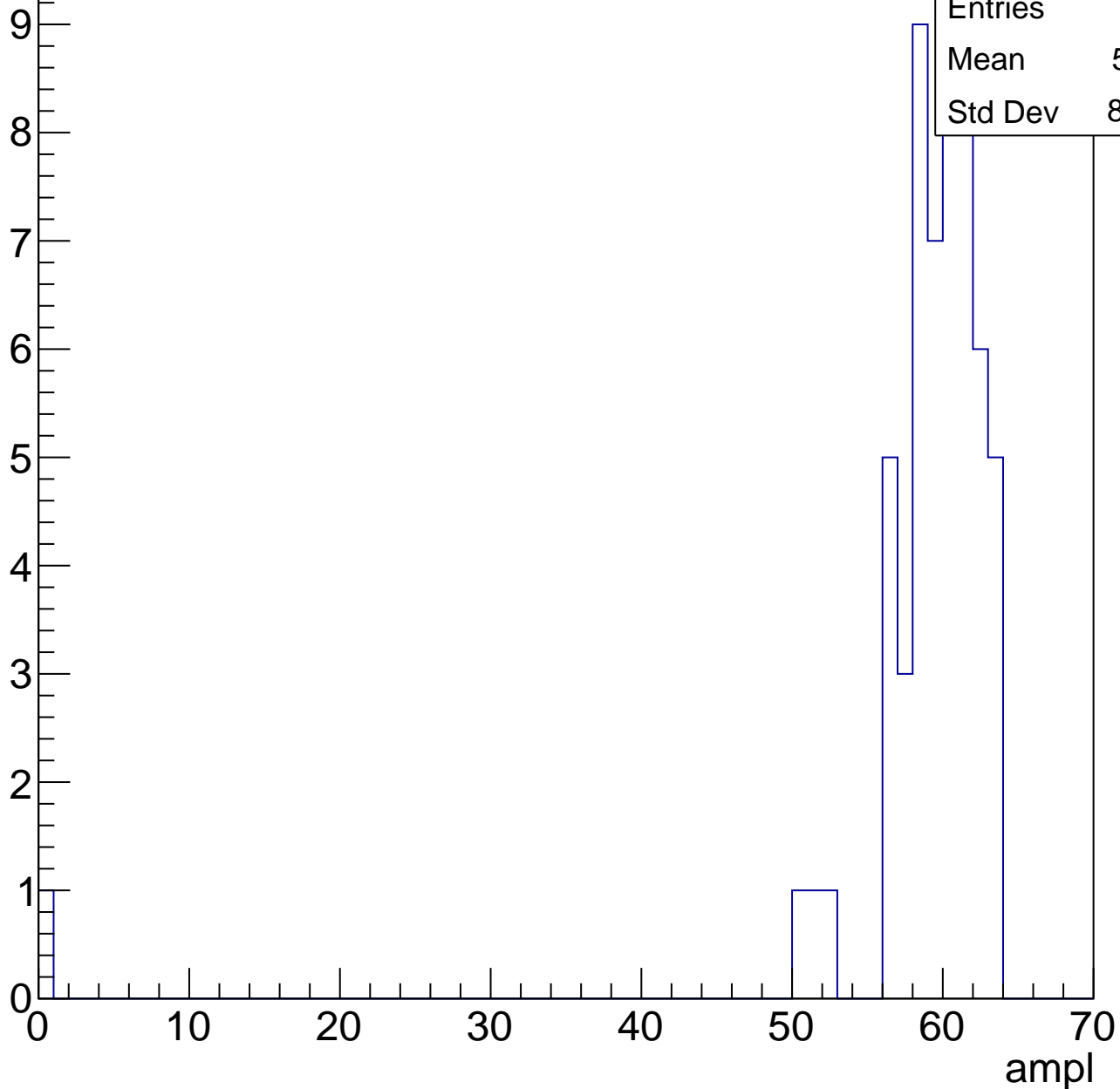
calib\_packv5\_042523\_0143.root, FC#13, port D2



# B1L003S, U26-ch68, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

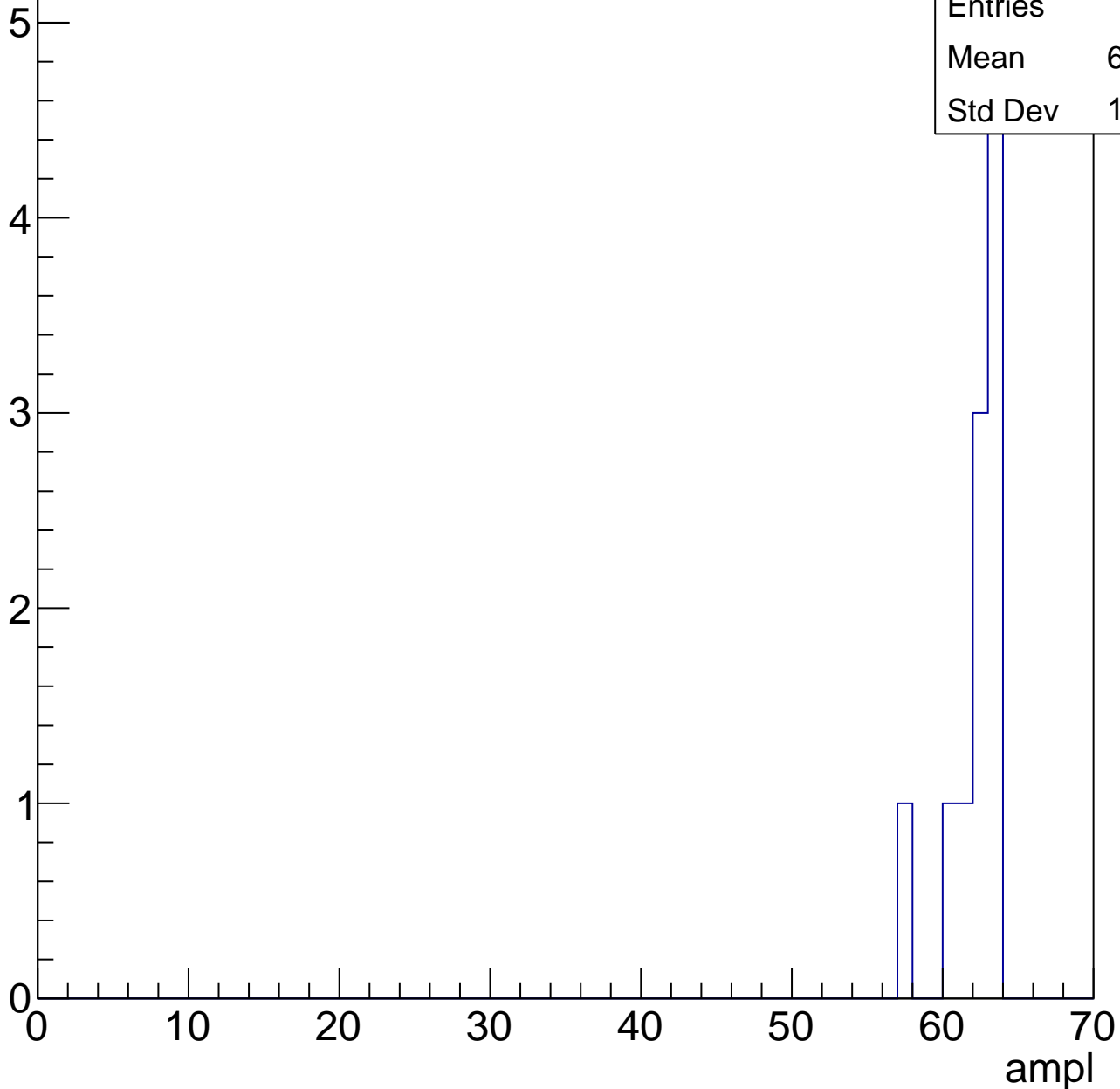


# B1L003S, U26-ch68, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	11
Mean	61.73
Std Dev	1.763





# B1L003S, U26-ch68, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	43
Std Dev	19

ampl

0 10 20 30 40 50 60 70

# B1L003S, U26-ch69, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	73
Mean	29.26
Std Dev	4.623

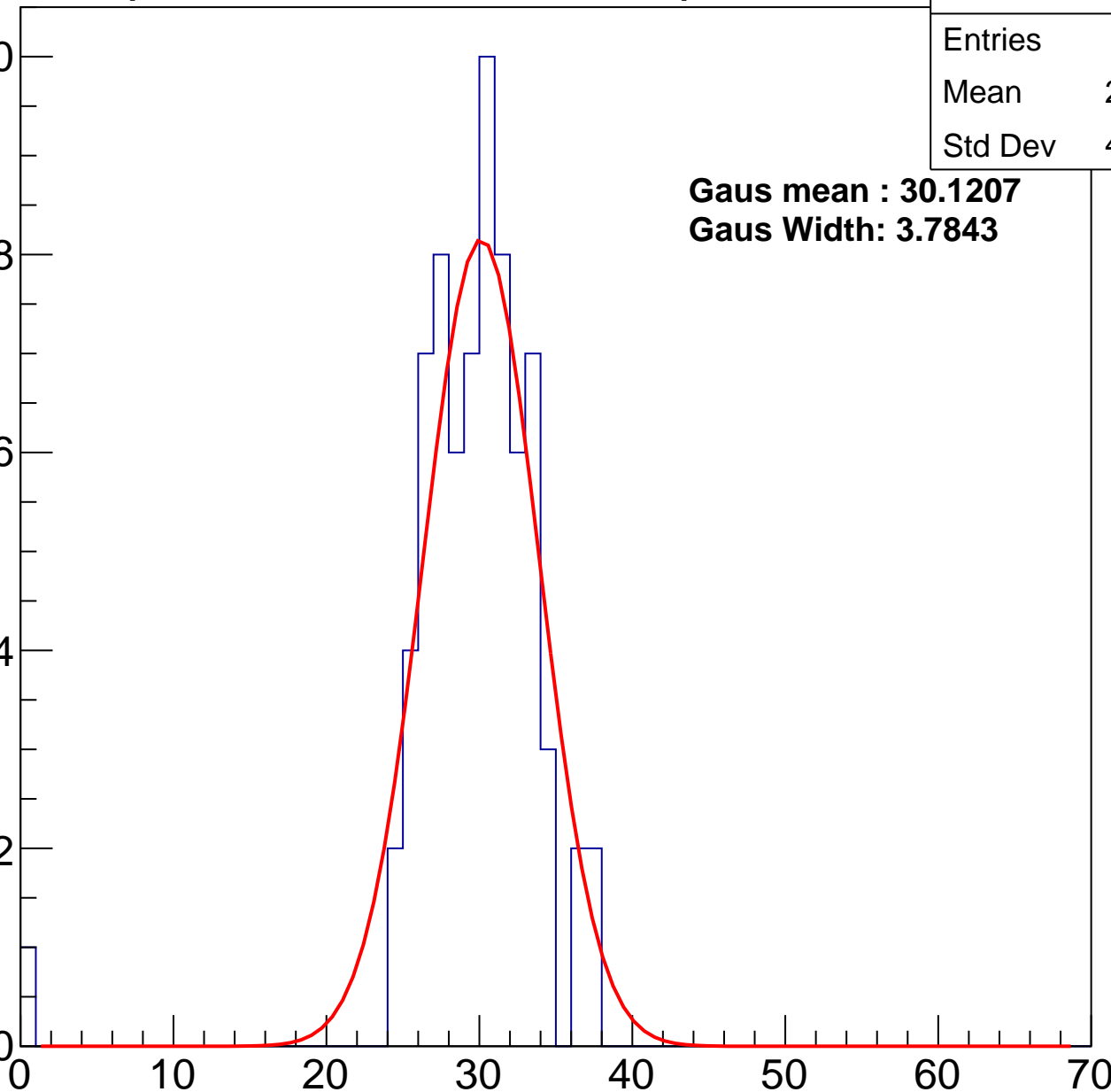
**Gaus mean : 30.1207**

**Gaus Width: 3.7843**

Entry

10  
8  
6  
4  
2  
0

ampl



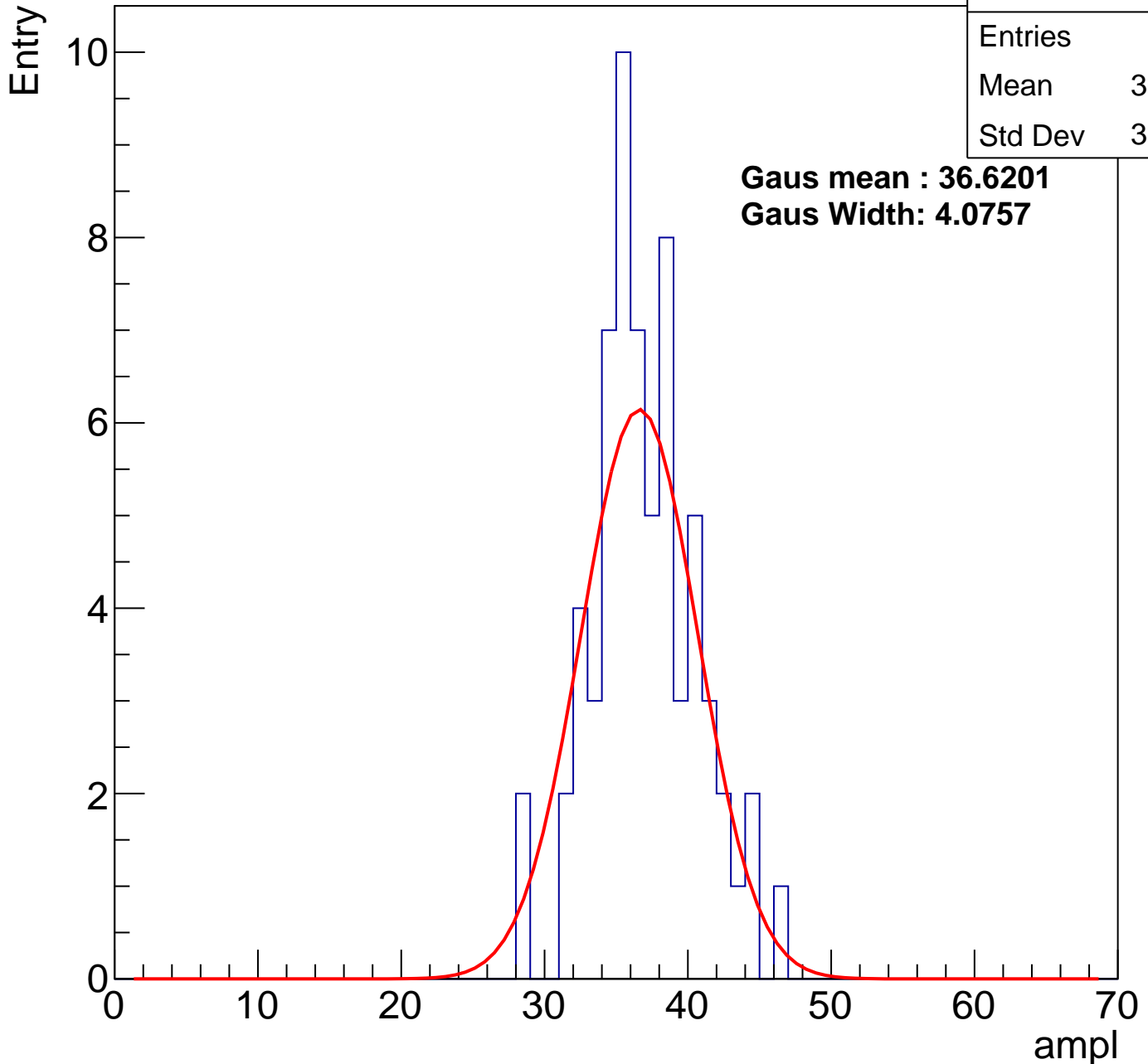
# B1L003S, U26-ch69, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	65
Mean	36.54
Std Dev	3.629

**Gaus mean : 36.6201**

**Gaus Width: 4.0757**

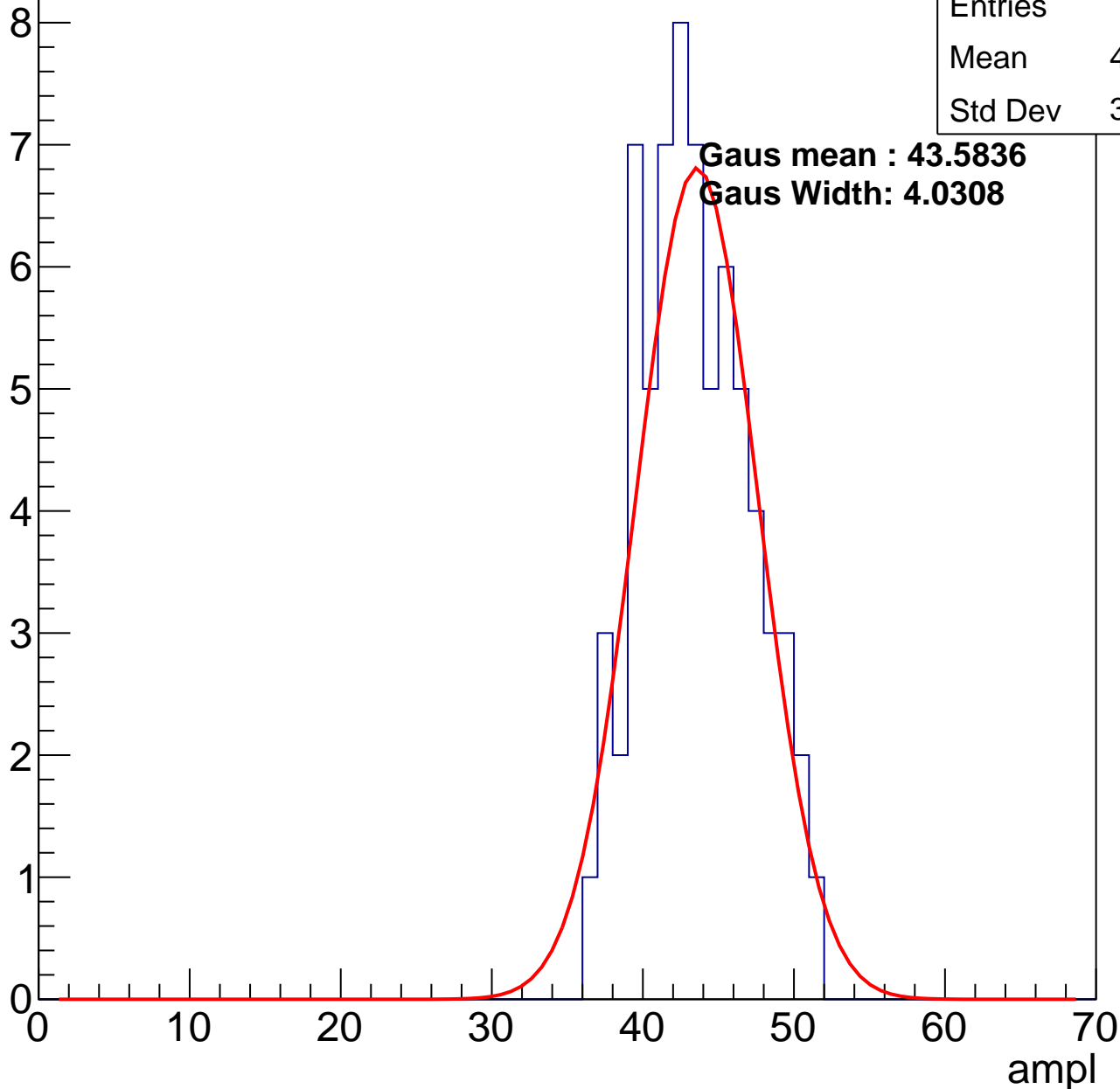


# B1L003S, U26-ch69, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	43.04
Std Dev	3.577

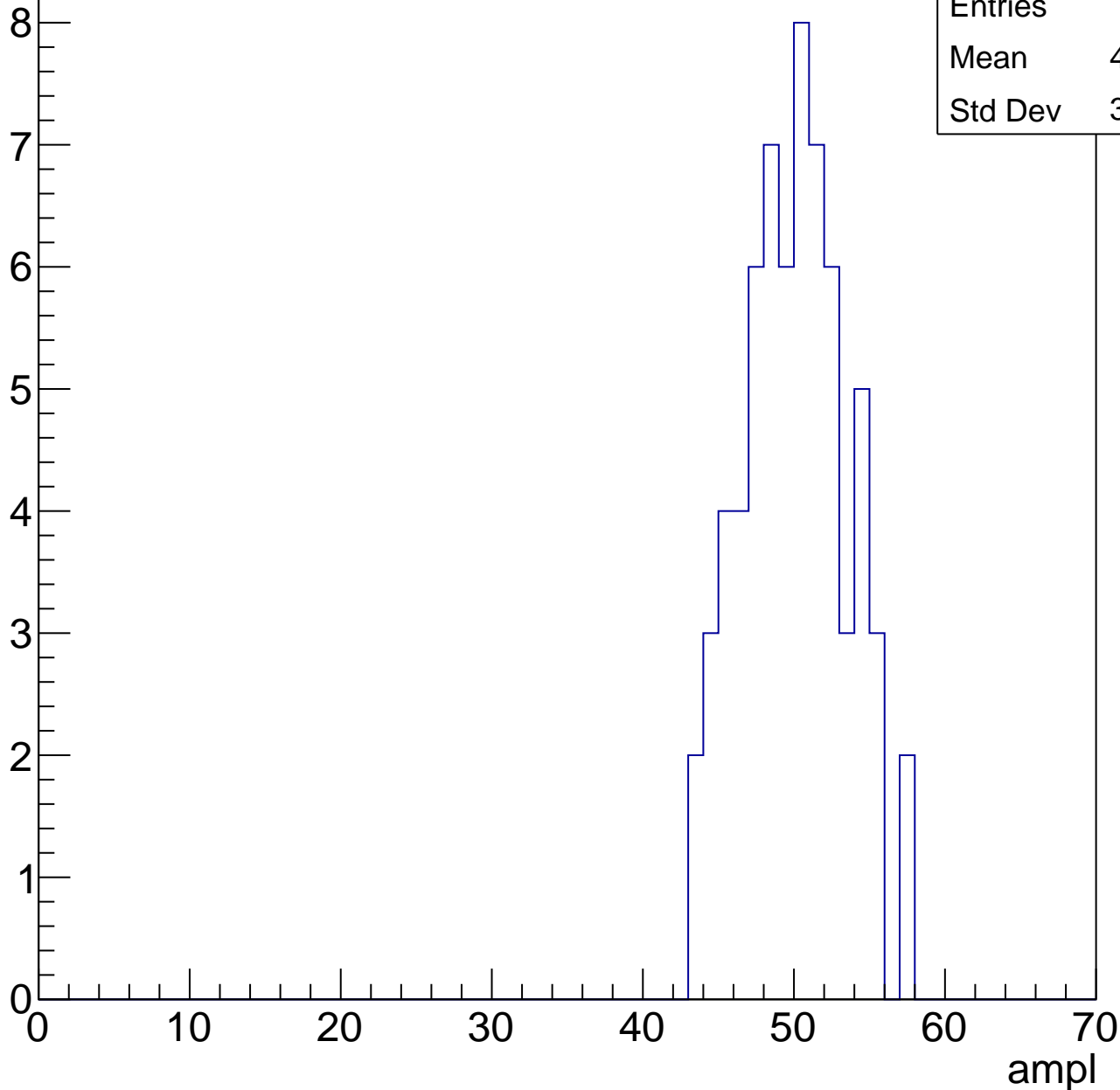


# B1L003S, U26-ch69, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

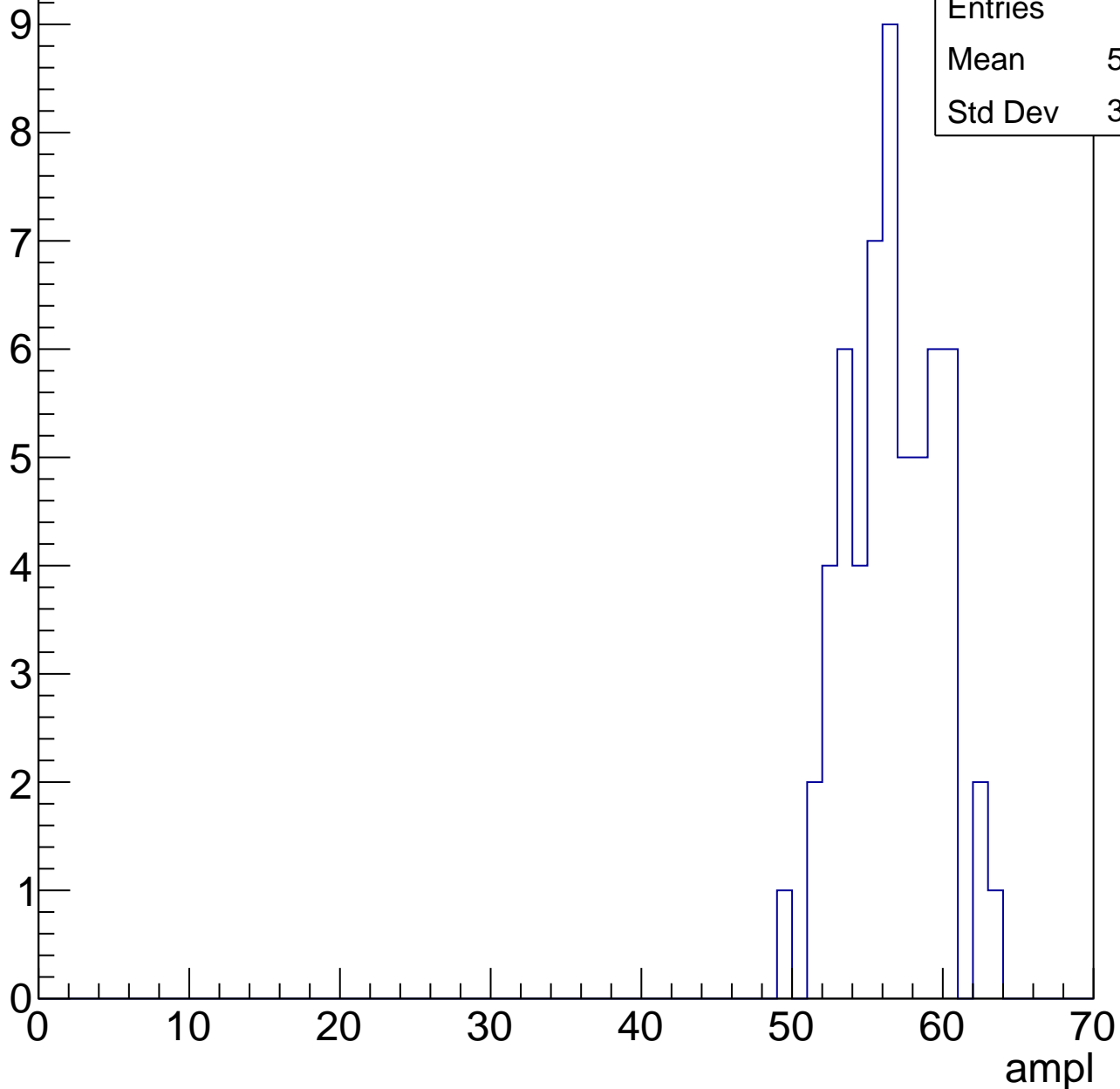
Entries	66
Mean	49.56
Std Dev	3.385



# B1L003S, U26-ch69, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



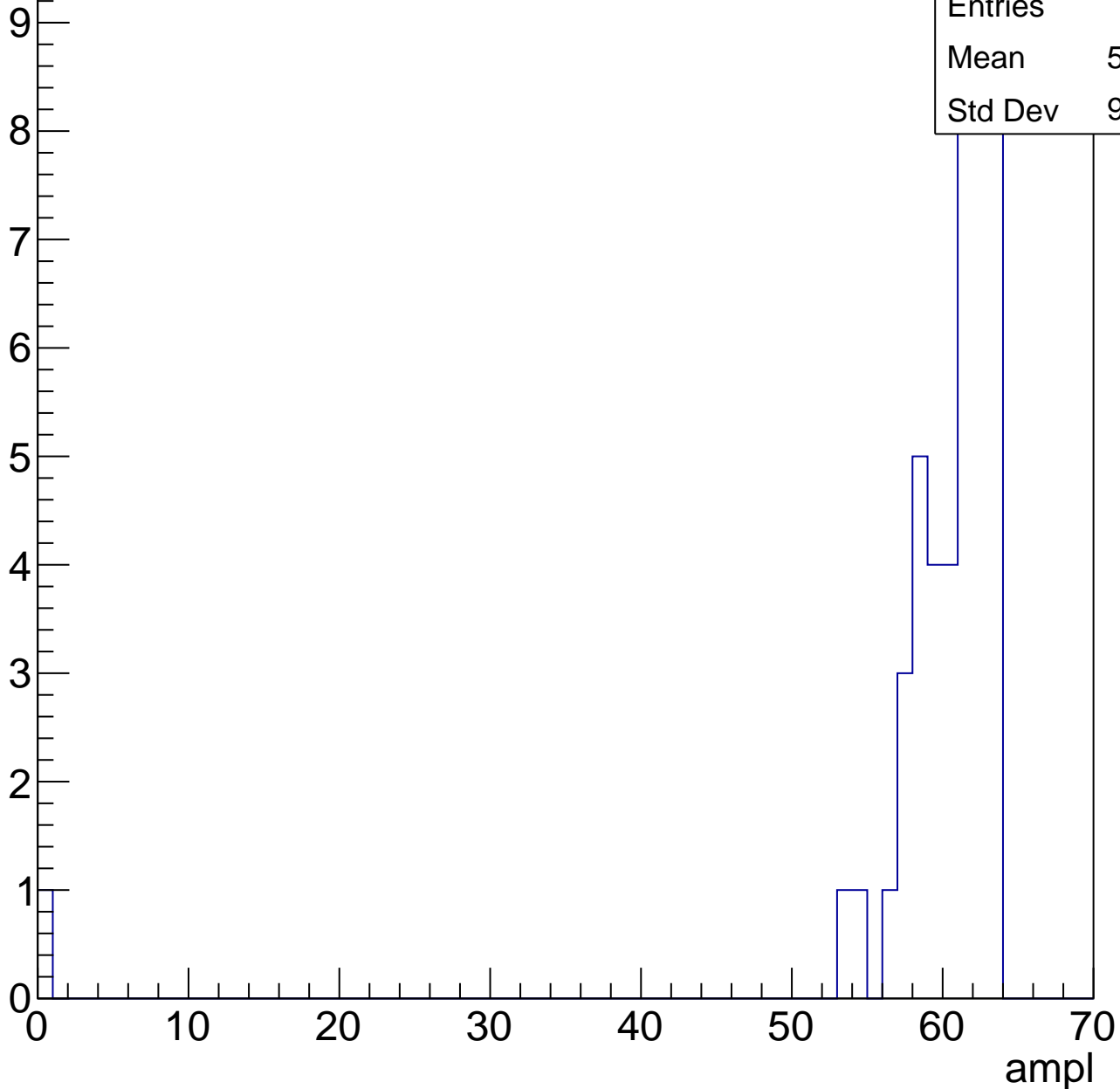
Entries	58
Mean	56.17
Std Dev	3.035

# B1L003S, U26-ch69, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	45
Mean	58.87
Std Dev	9.198



# B1L003S, U26-ch69, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch69, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U26-ch70, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	77
Mean	28.16
Std Dev	3.35

**Gaus mean : 28.2046**

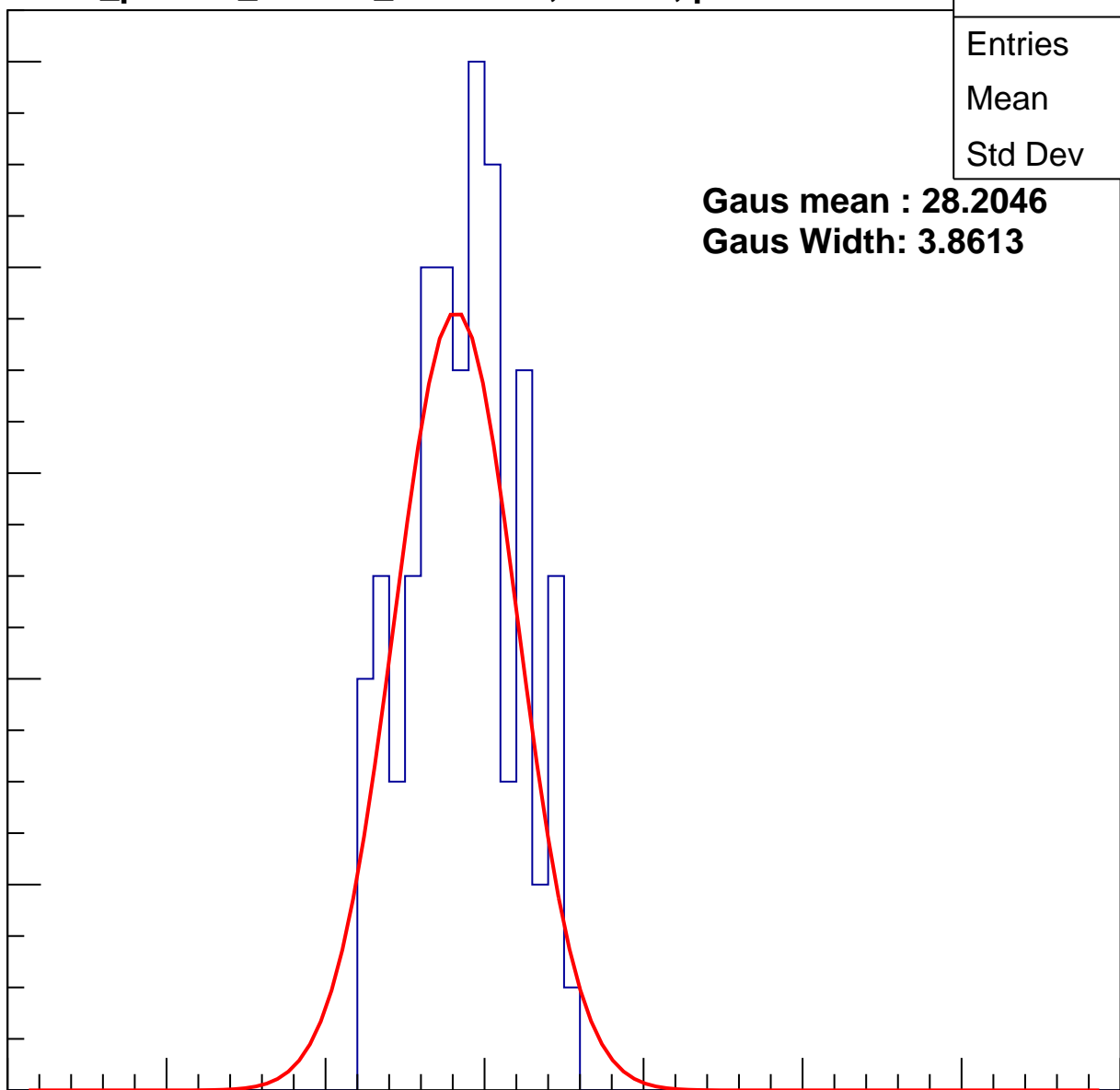
**Gaus Width: 3.8613**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U26-ch70, adc1

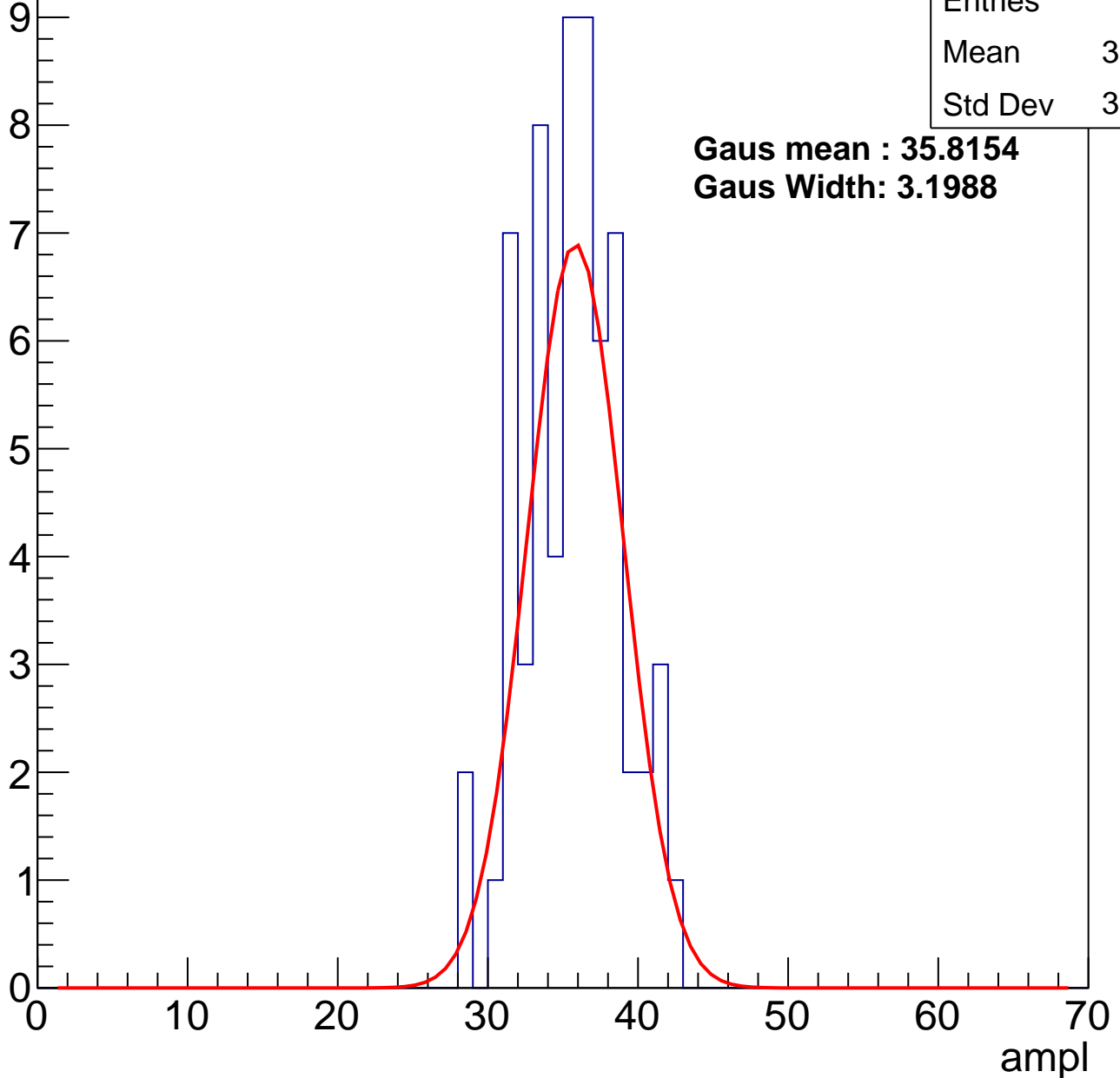
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	35.14
Std Dev	3.142

**Gaus mean : 35.8154**

**Gaus Width: 3.1988**



# B1L003S, U26-ch70, adc2

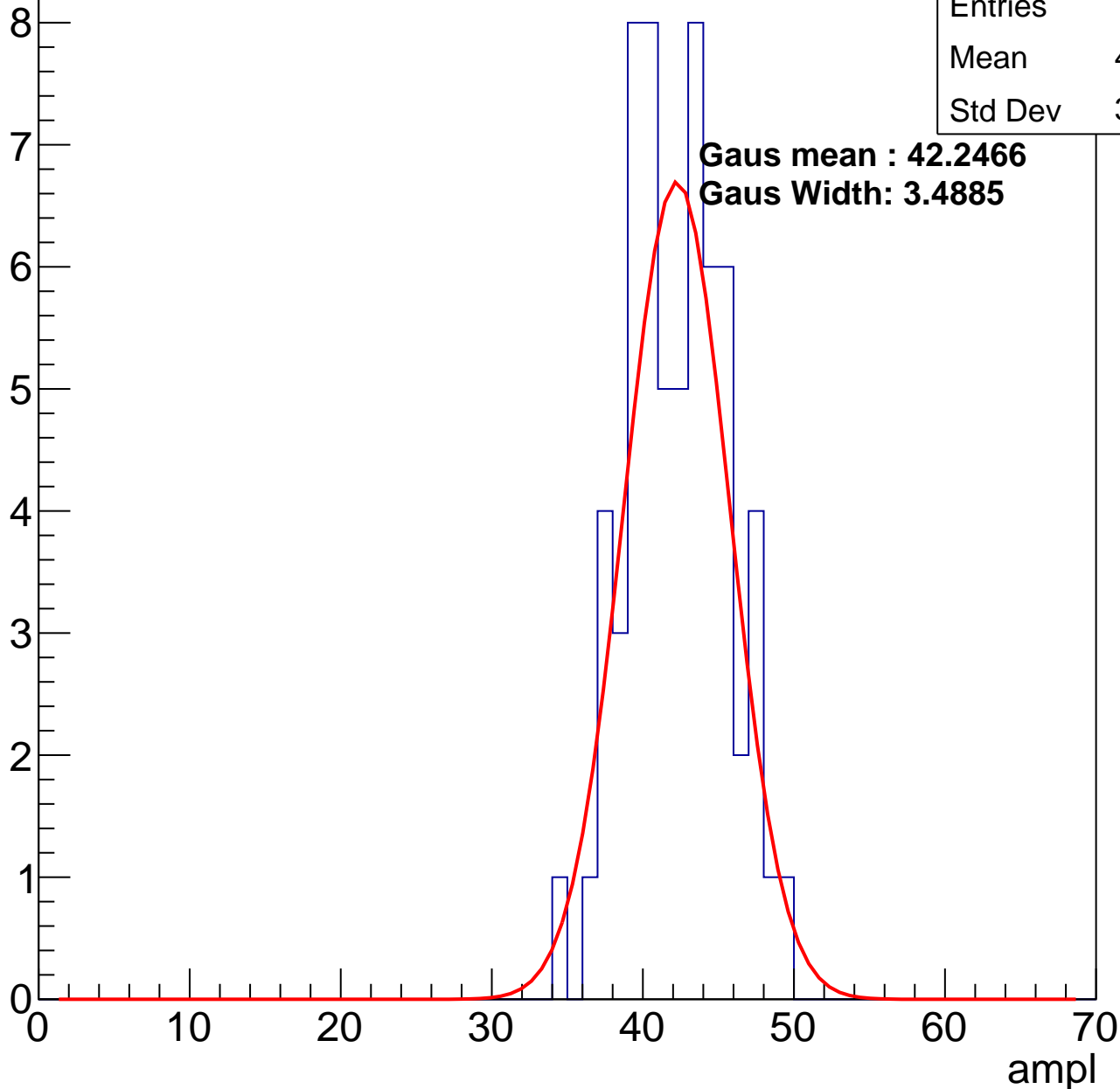
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	41.81
Std Dev	3.231

**Gaus mean : 42.2466**

**Gaus Width: 3.4885**

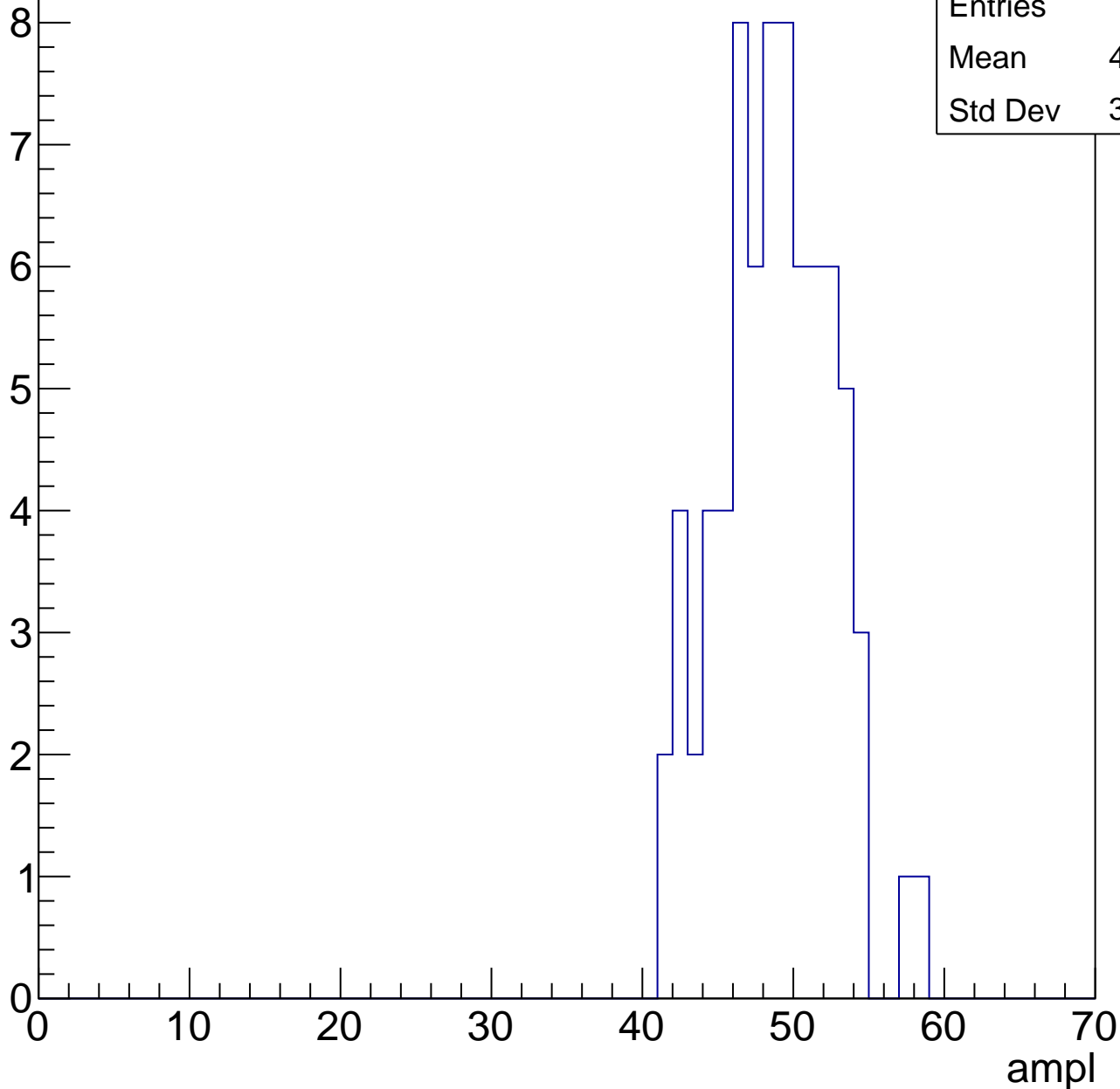


# B1L003S, U26-ch70, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	74
Mean	48.35
Std Dev	3.707

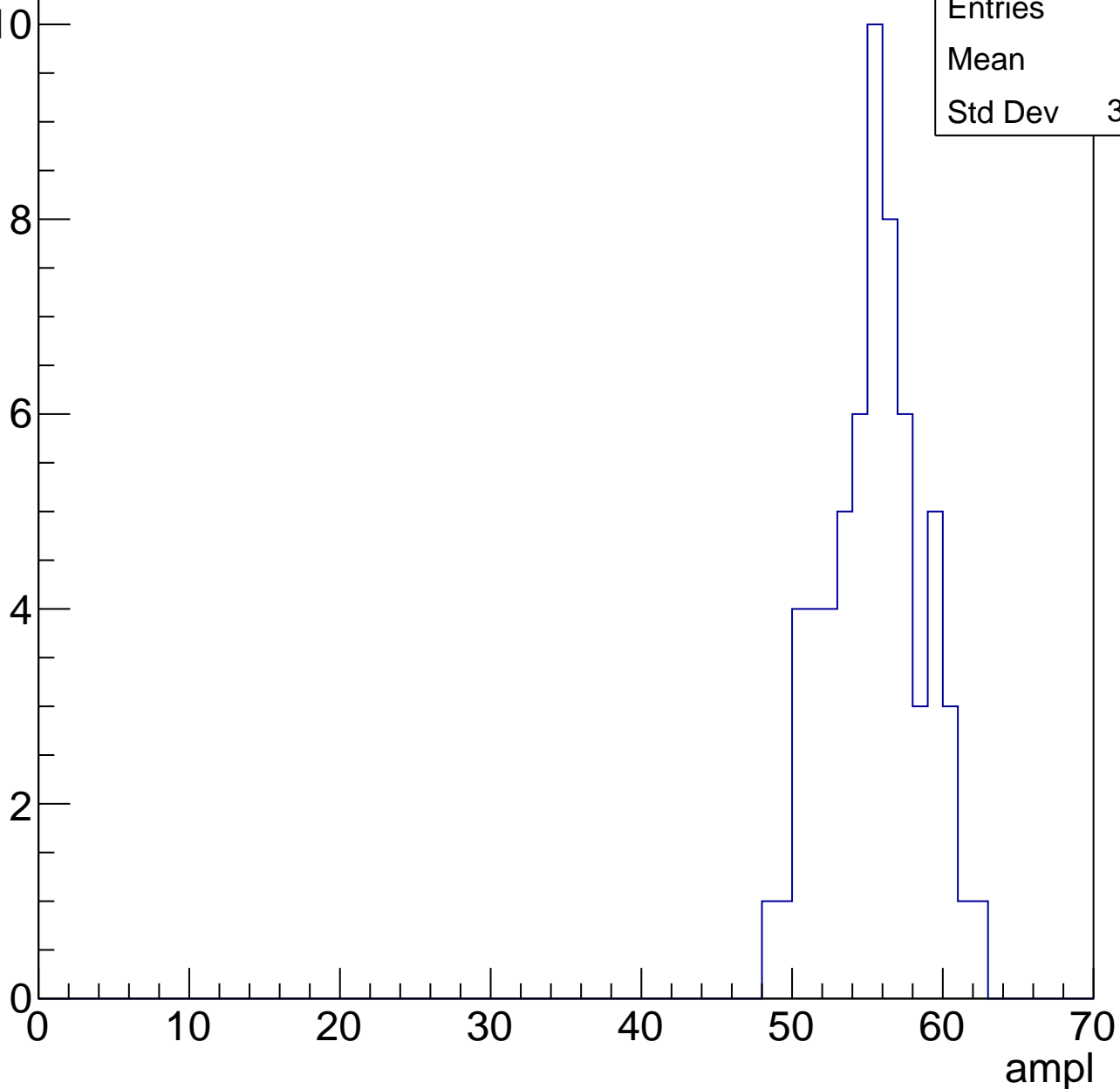


# B1L003S, U26-ch70, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	55
Std Dev	3.137

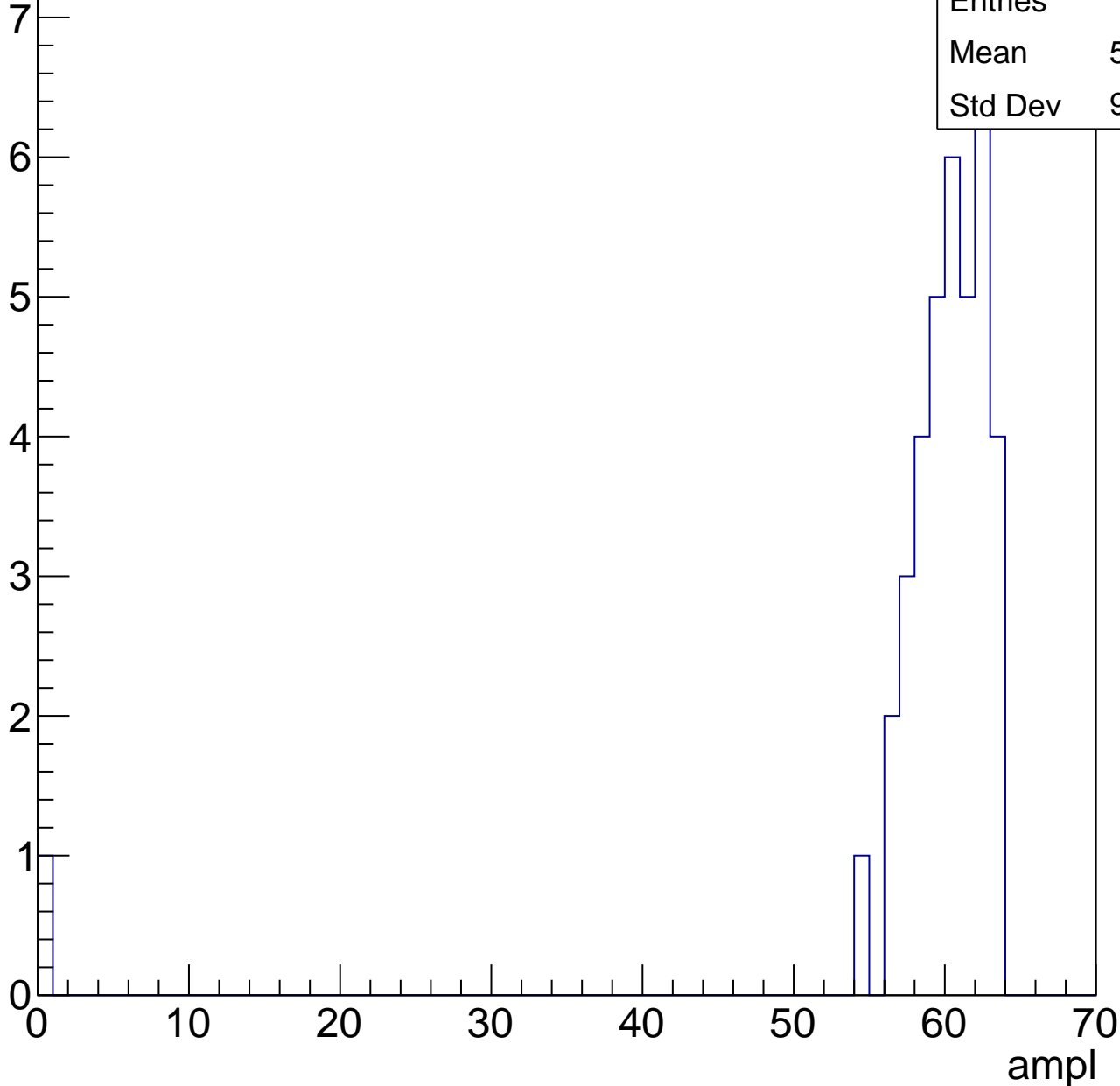


# B1L003S, U26-ch70, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	38
Mean	58.29
Std Dev	9.833

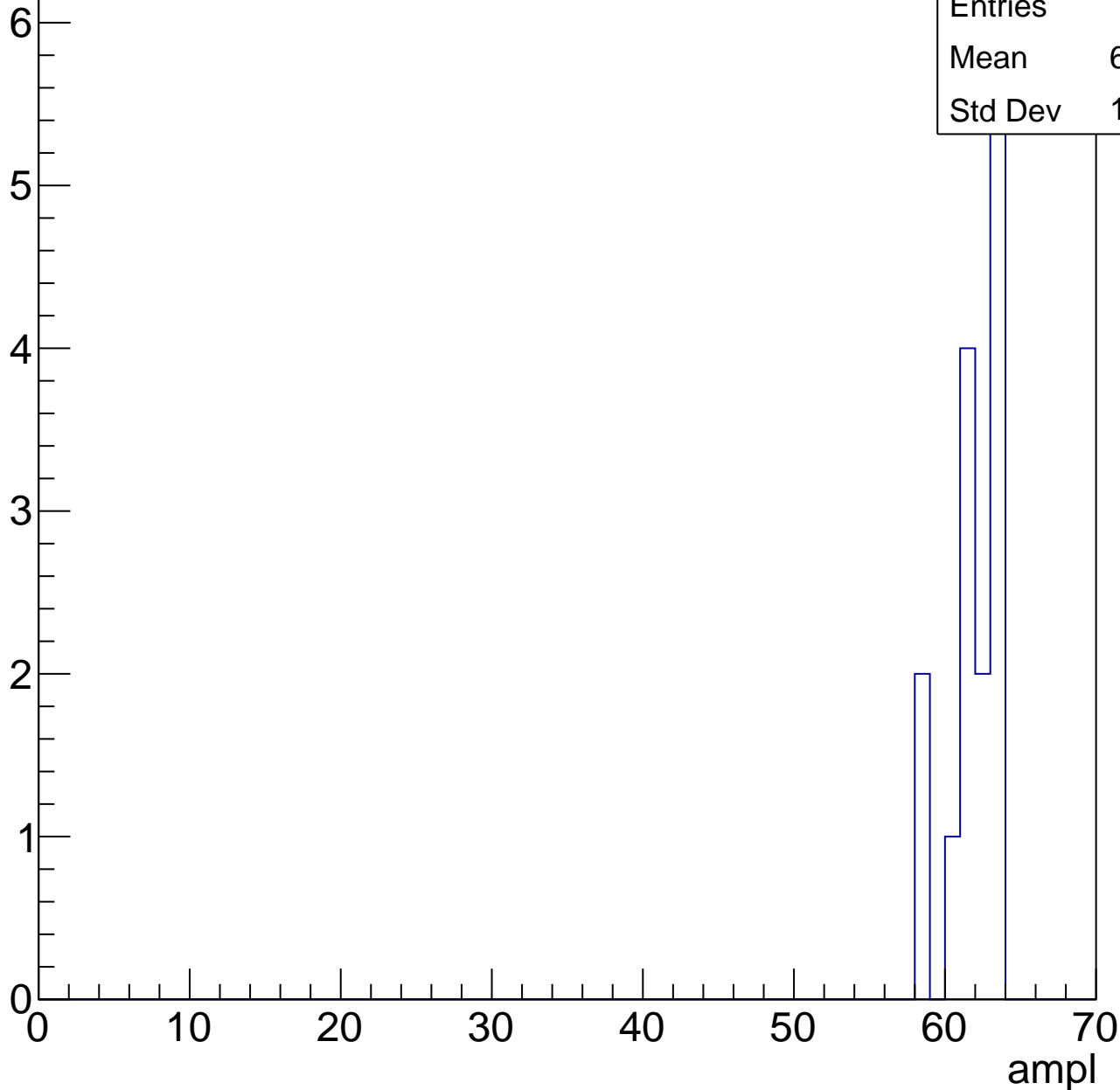


# B1L003S, U26-ch70, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	15
Mean	61.47
Std Dev	1.668





# B1L003S, U26-ch70, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	20
Std Dev	0

ampl

# B1L003S, U26-ch71, adc0

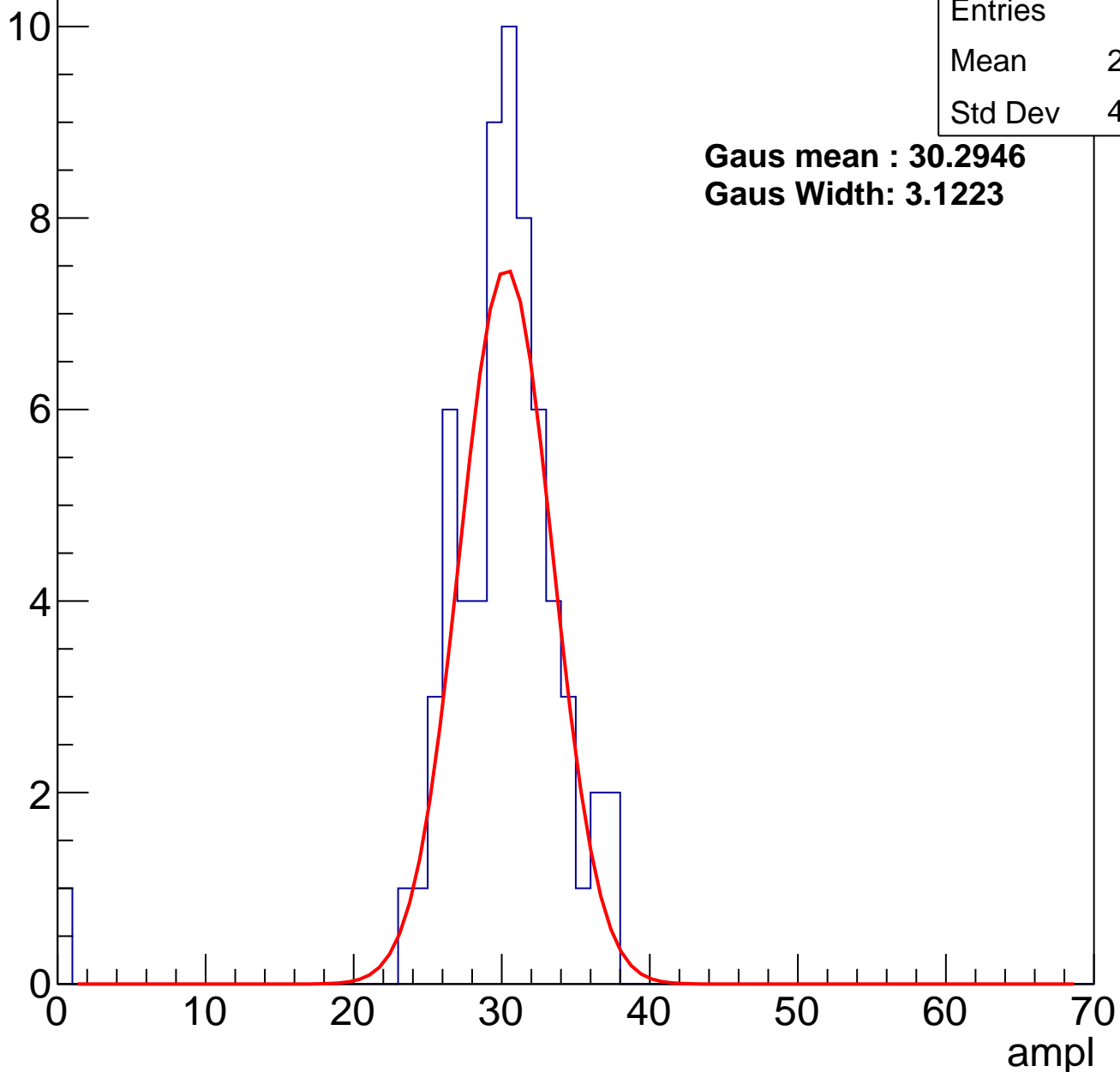
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	65
Mean	29.45
Std Dev	4.817

**Gaus mean : 30.2946**

**Gaus Width: 3.1223**

Entry



# B1L003S, U26-ch71, adc1

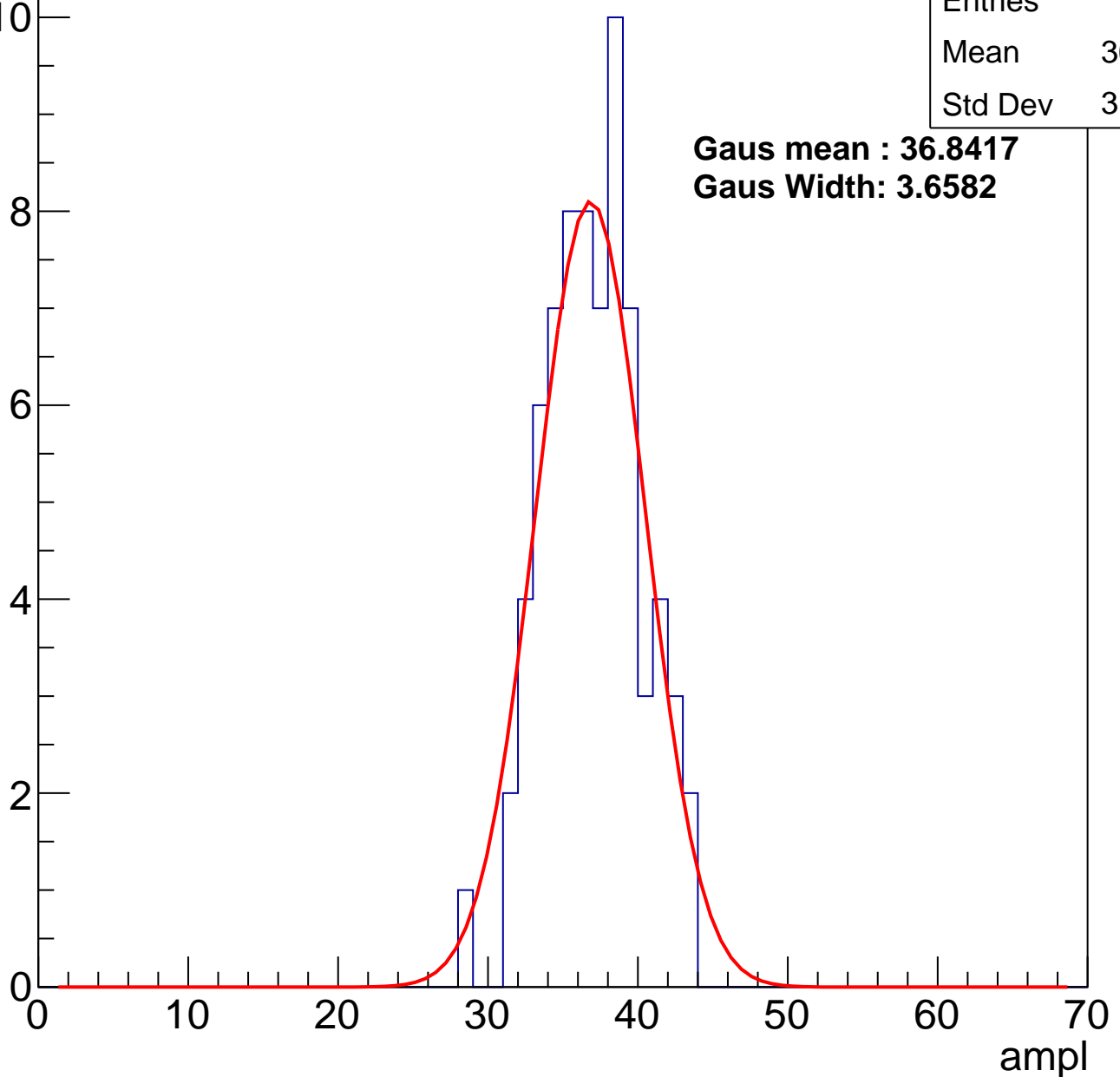
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	72
Mean	36.53
Std Dev	3.145

**Gaus mean : 36.8417**

**Gaus Width: 3.6582**



# B1L003S, U26-ch71, adc2

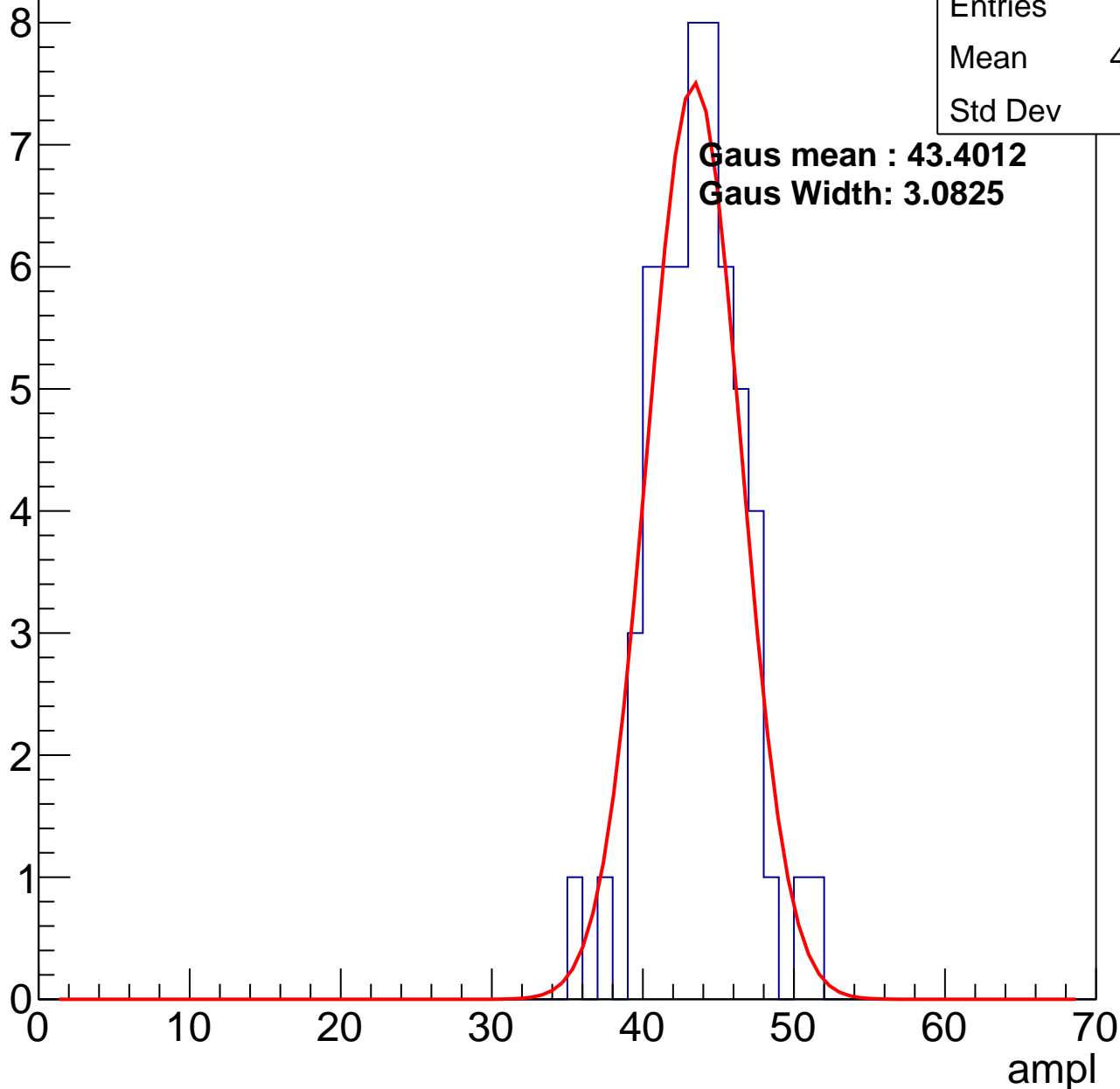
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	43.16
Std Dev	2.99

**Gaus mean : 43.4012**

**Gaus Width: 3.0825**

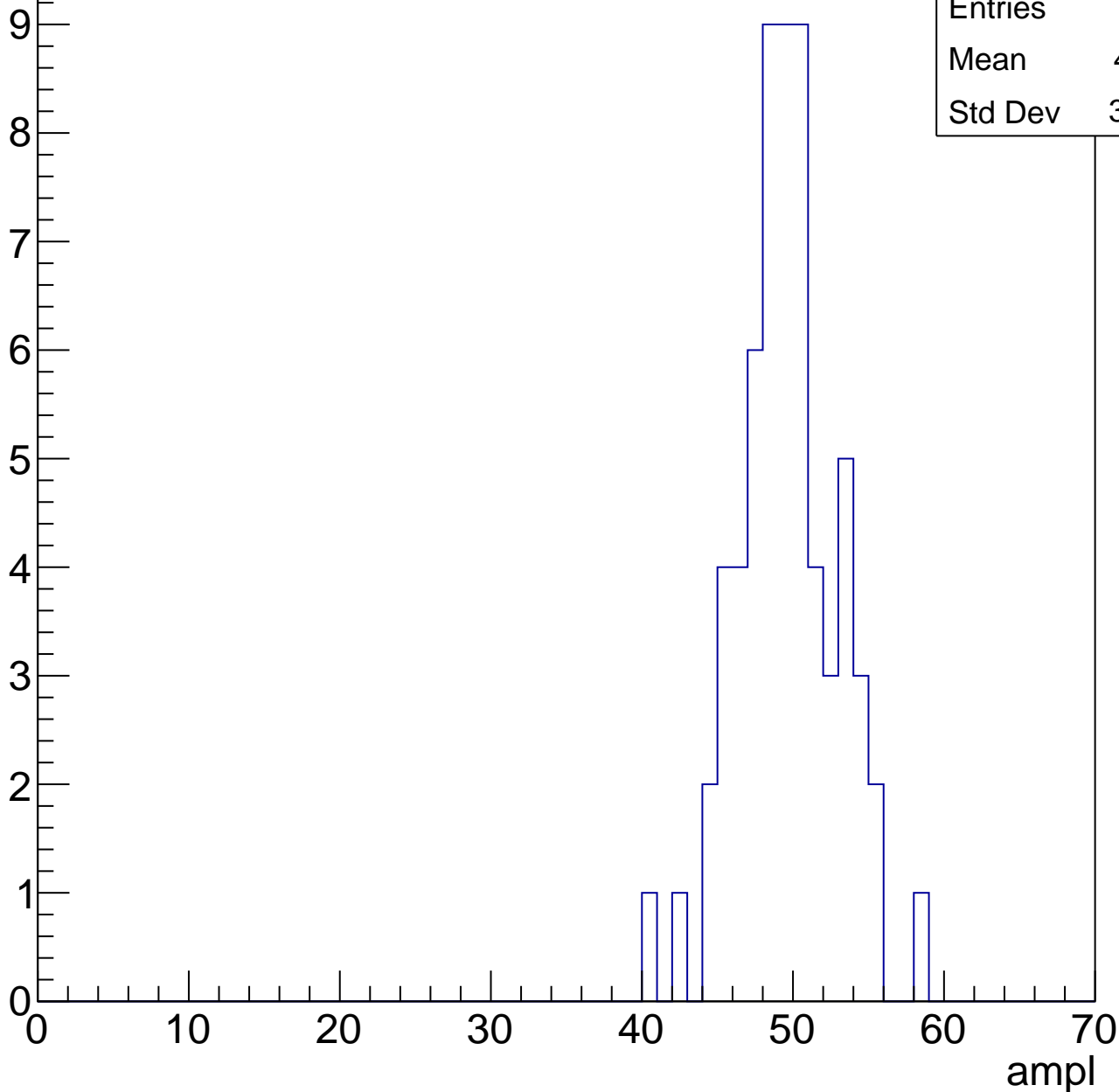


# B1L003S, U26-ch71, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	49.11
Std Dev	3.267

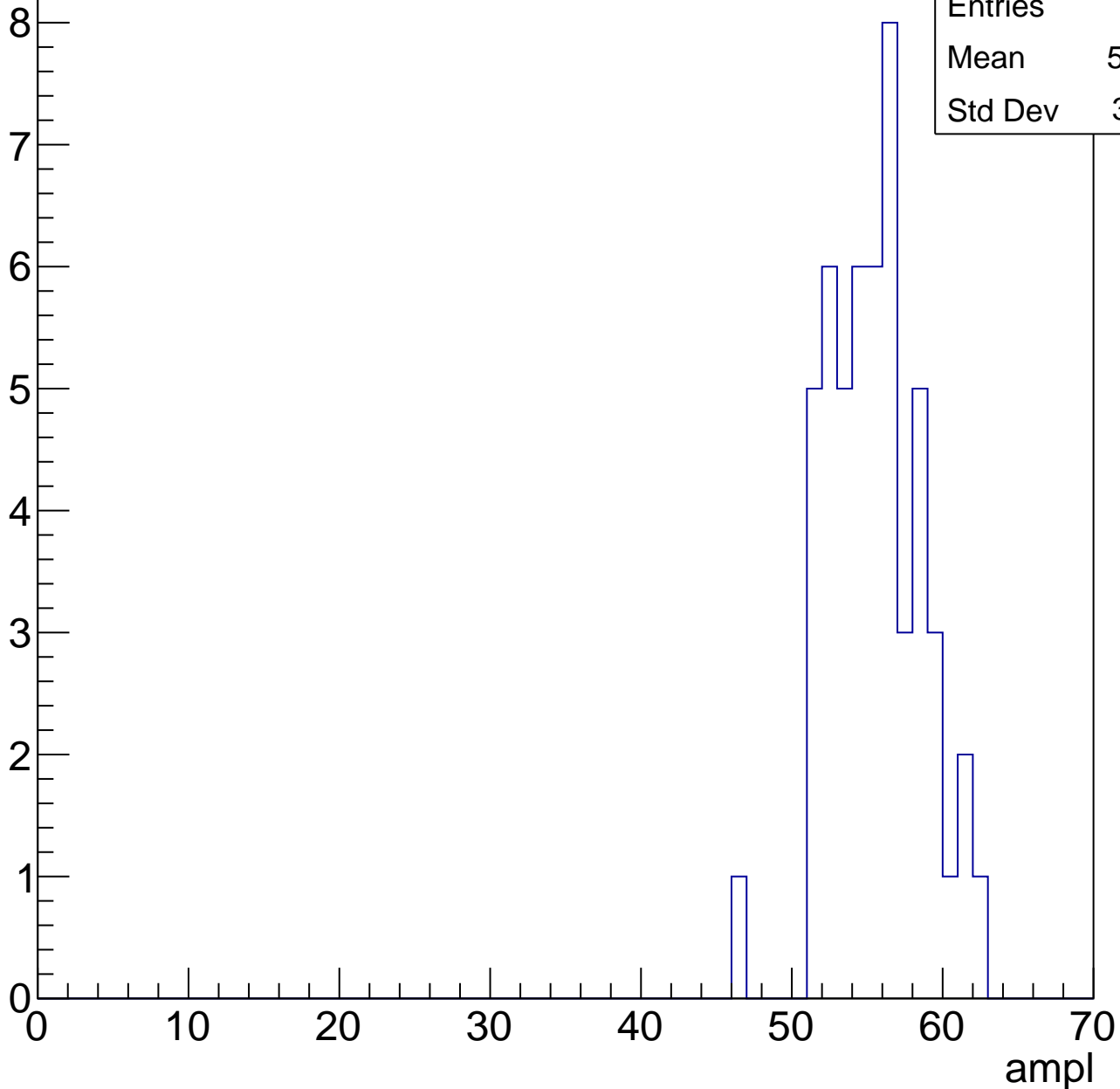


# B1L003S, U26-ch71, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	52
Mean	55.04
Std Dev	3.101

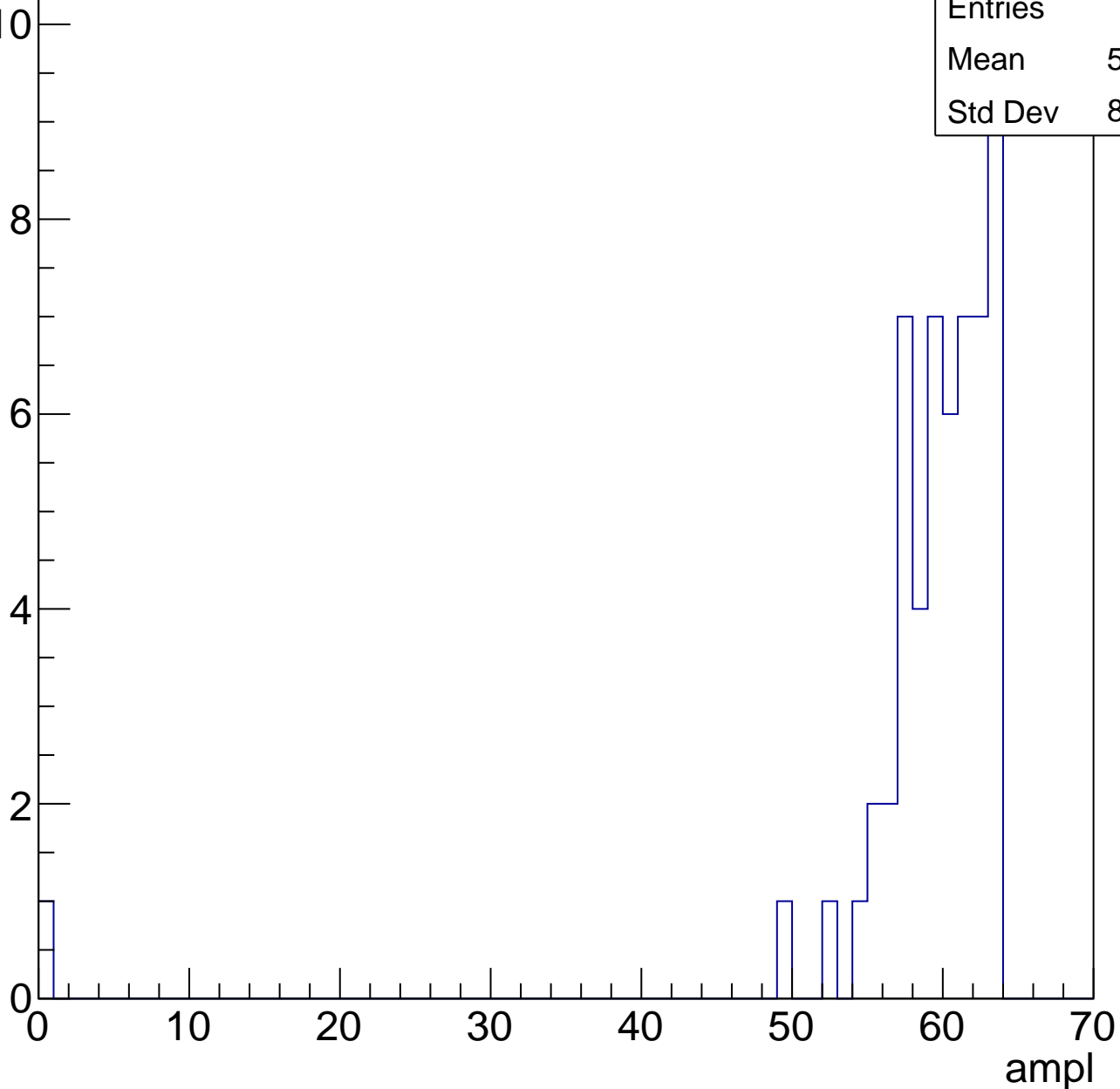


# B1L003S, U26-ch71, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

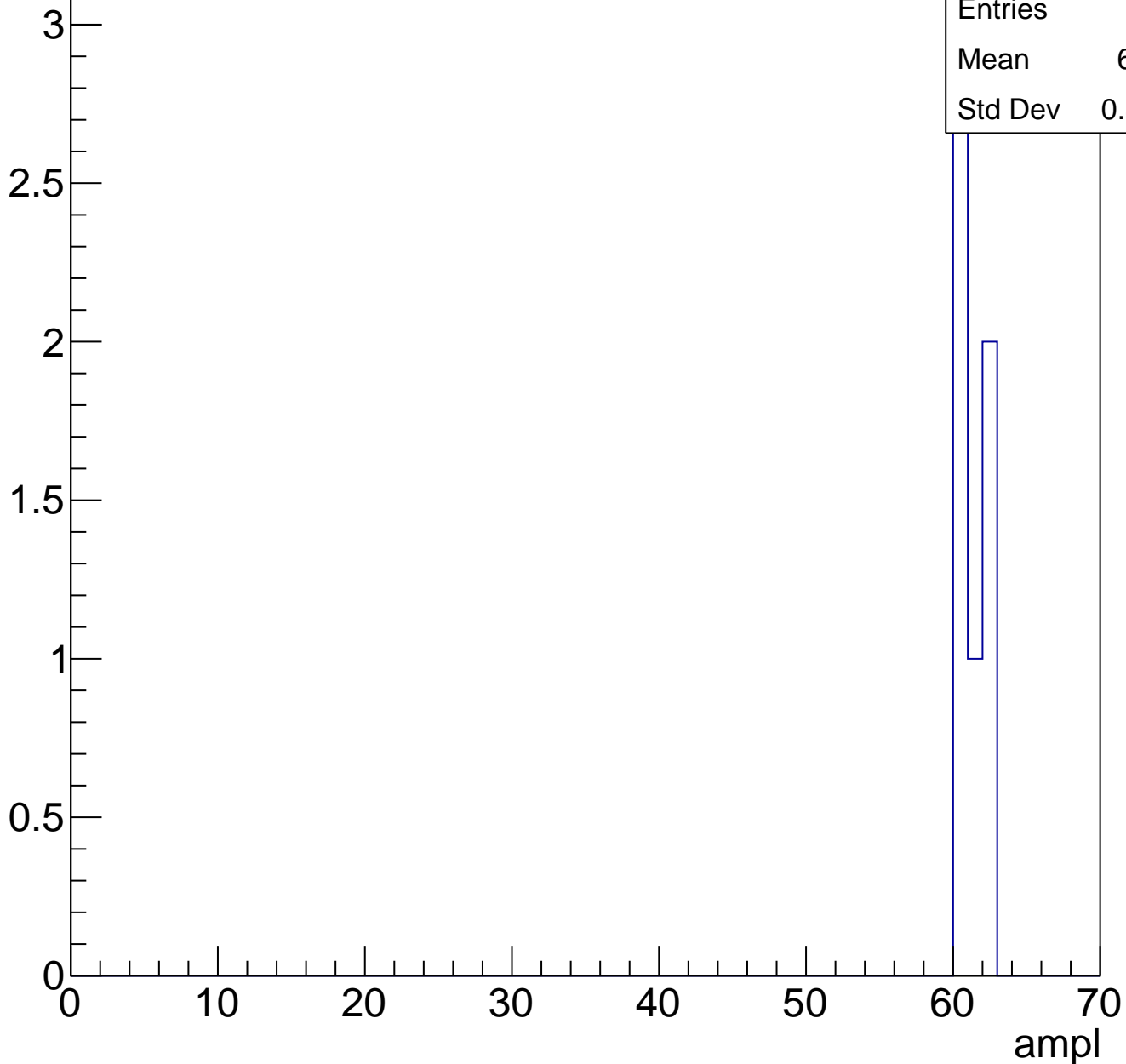
Entries	56
Mean	58.43
Std Dev	8.426



# B1L003S, U26-ch71, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



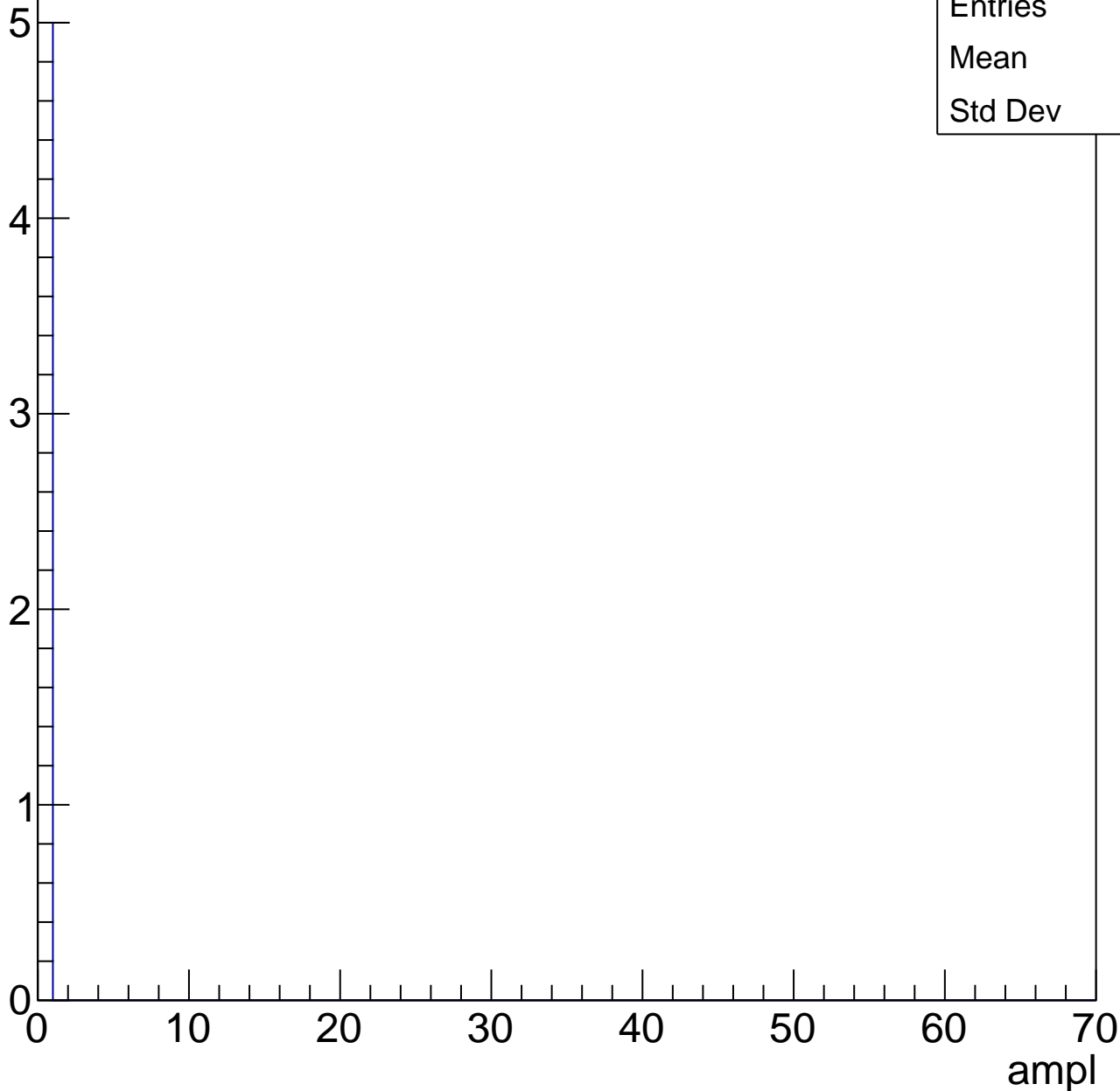


# B1L003S, U26-ch71, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	5
Mean	0
Std Dev	0



# B1L003S, U26-ch72, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	77
Mean	29.65
Std Dev	3.17

**Gaus mean : 30.1709**

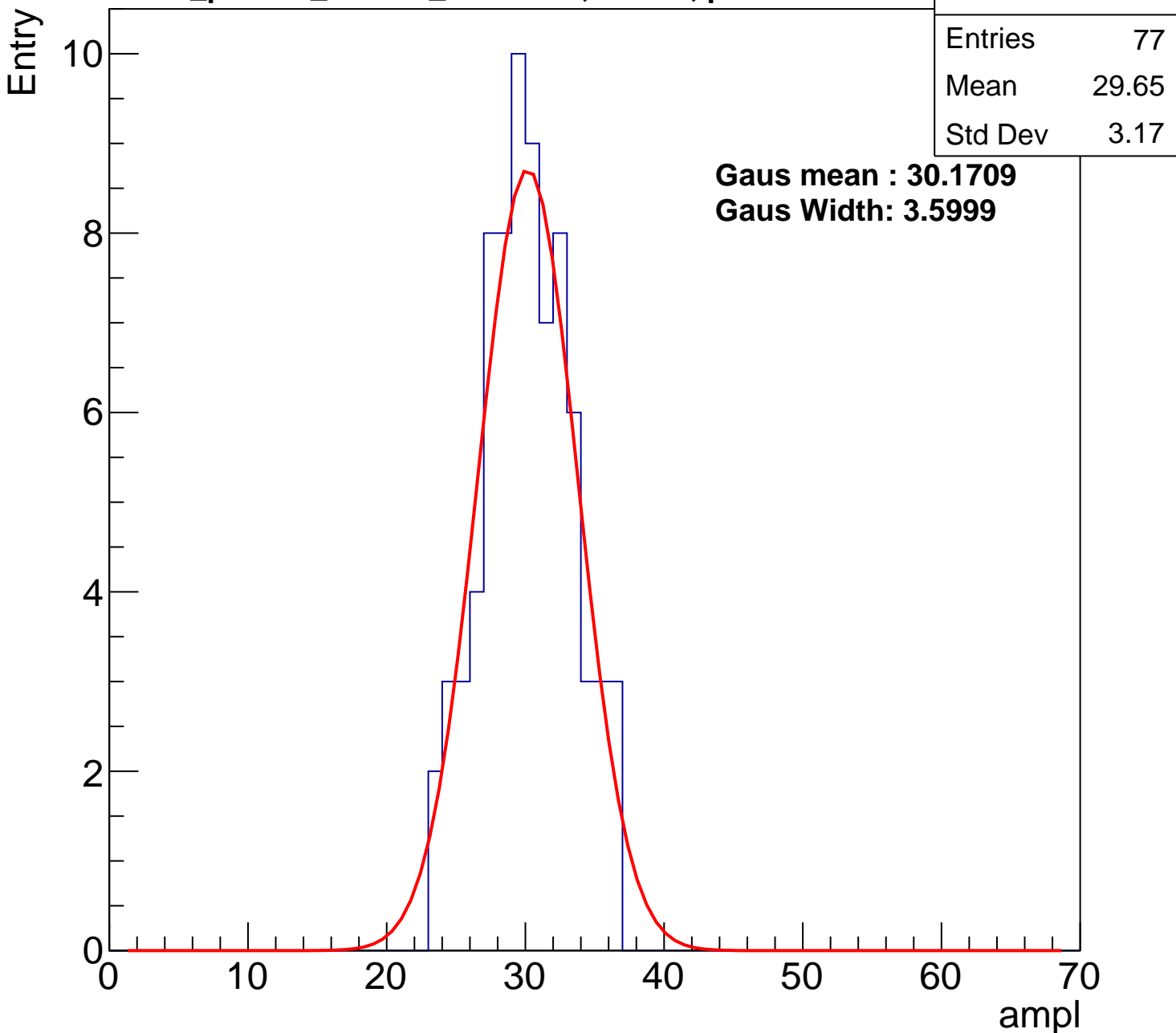
**Gaus Width: 3.5999**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U26-ch72, adc1

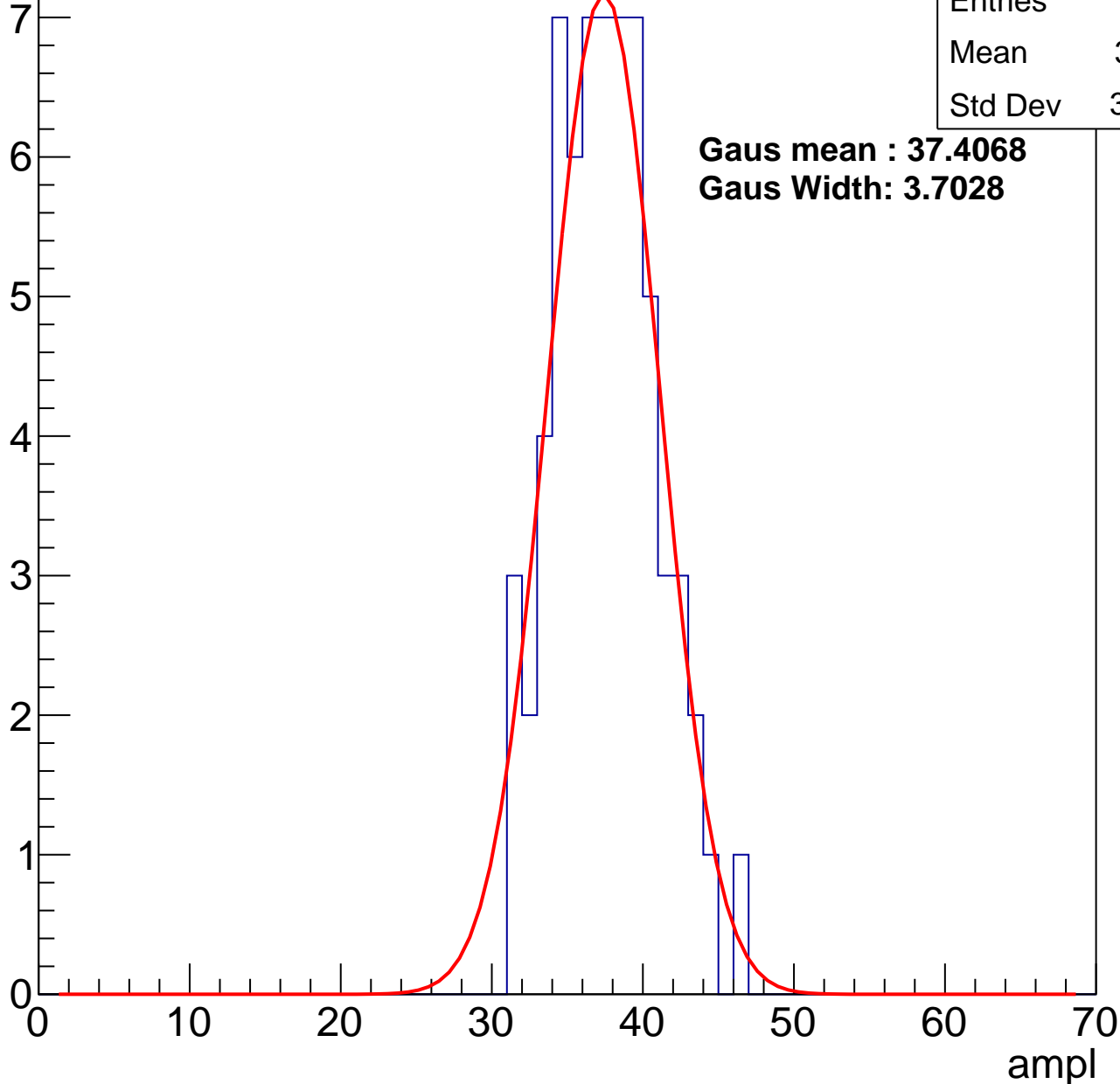
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	37.11
Std Dev	3.329

**Gaus mean : 37.4068**

**Gaus Width: 3.7028**

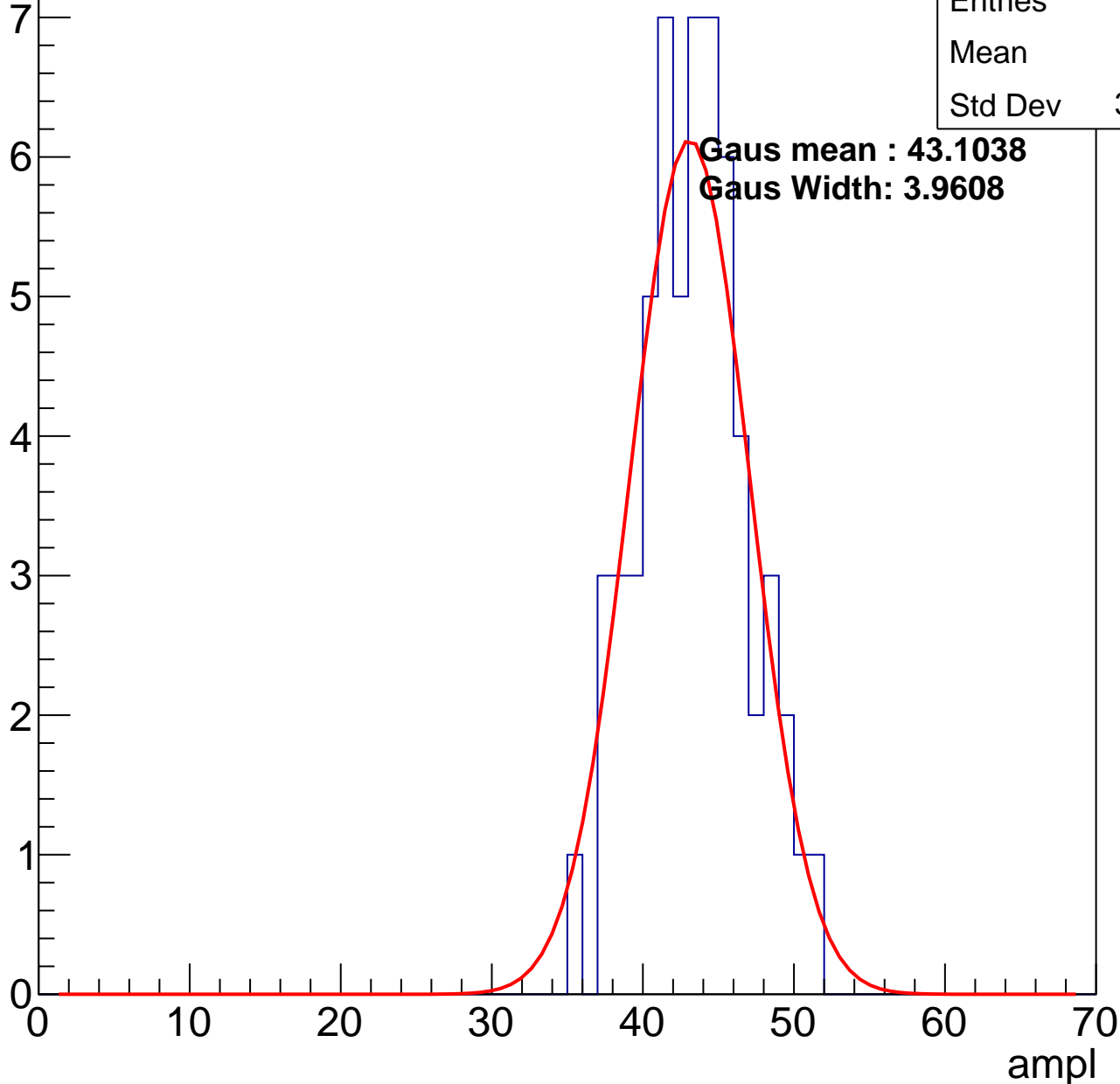


# B1L003S, U26-ch72, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	42.9
Std Dev	3.491

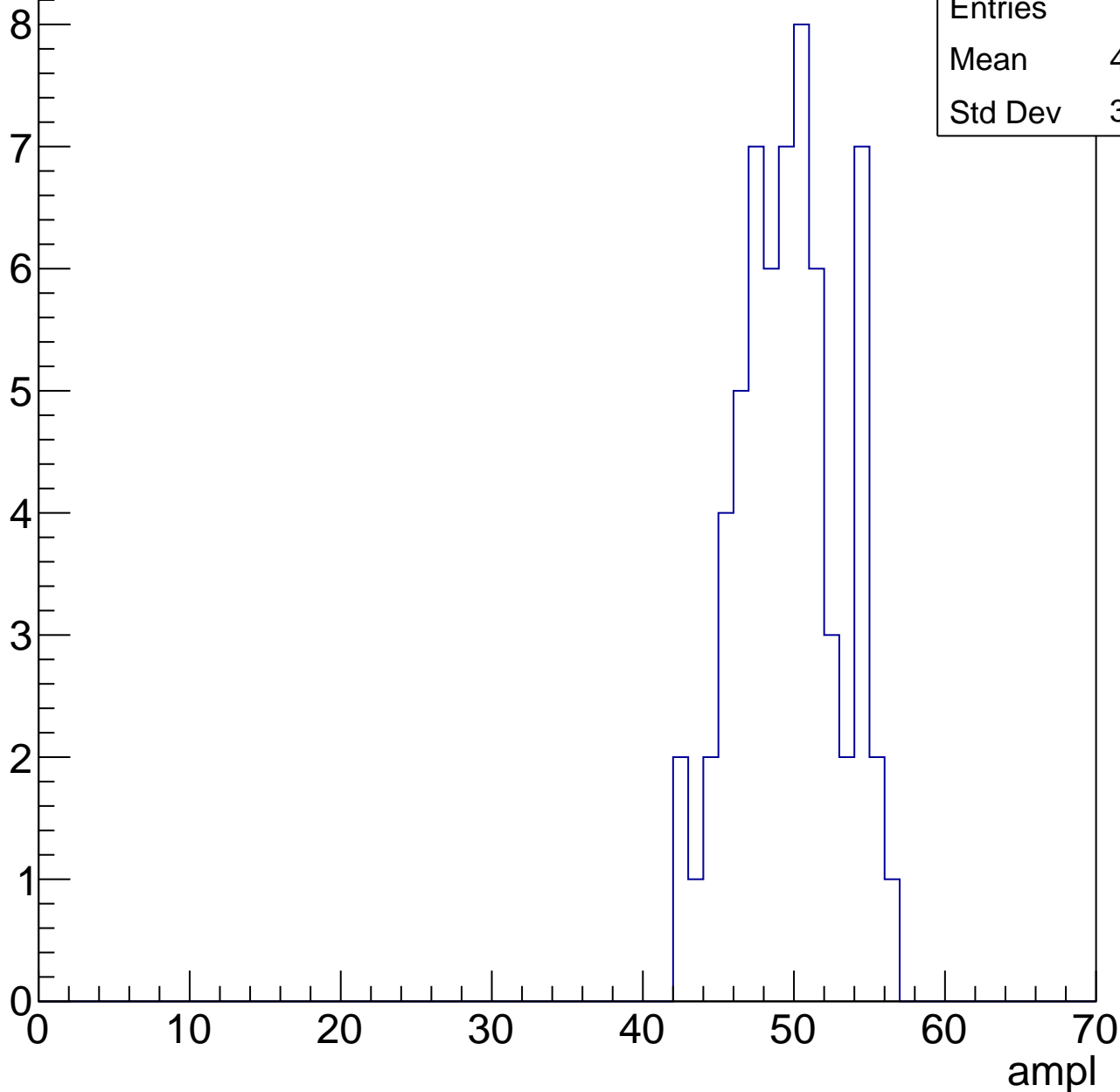


# B1L003S, U26-ch72, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	49.16
Std Dev	3.363

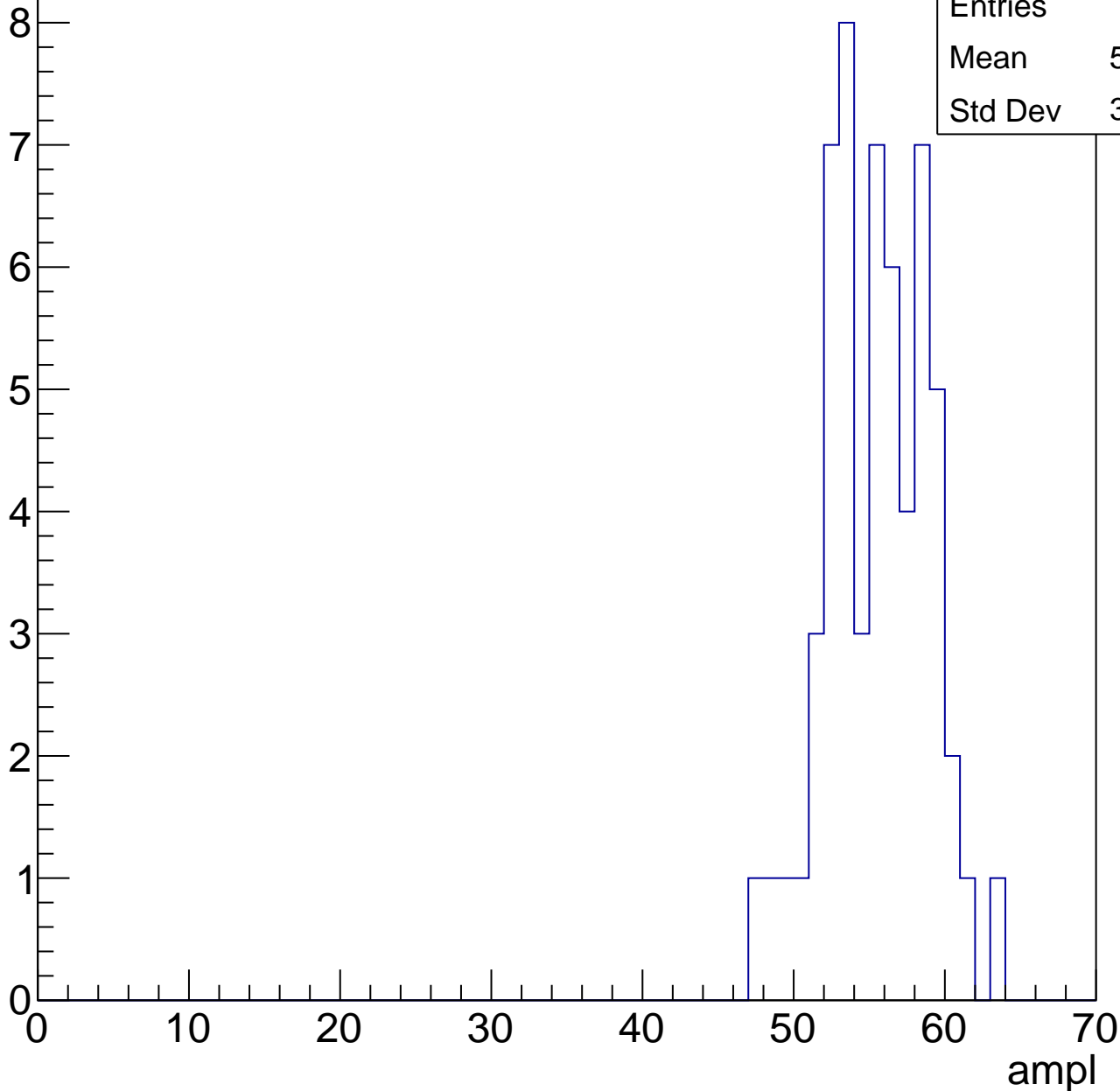


# B1L003S, U26-ch72, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	55.02
Std Dev	3.309

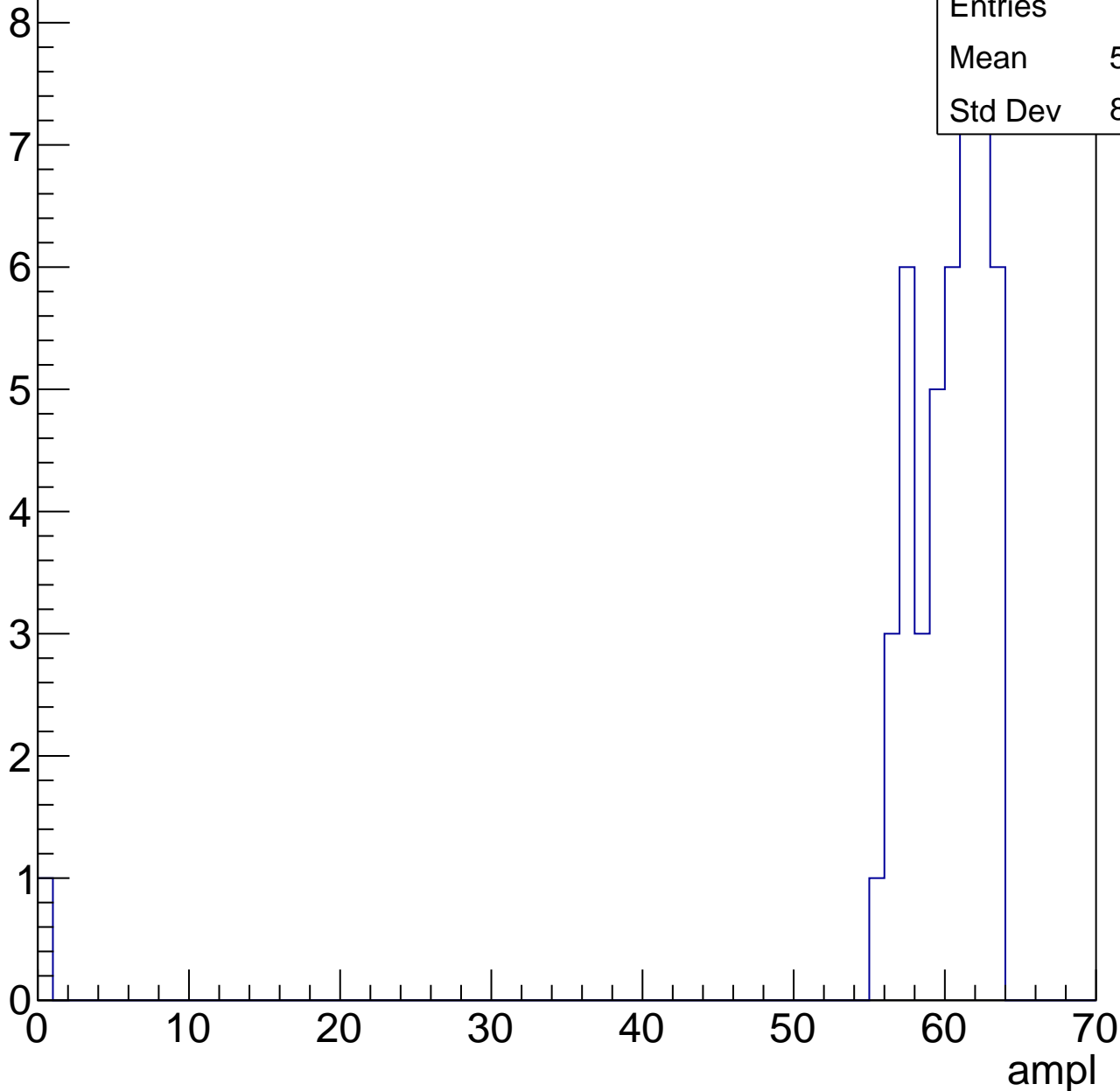


# B1L003S, U26-ch72, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	47
Mean	58.64
Std Dev	8.933



# B1L003S, U26-ch72, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	7
Mean	61.57
Std Dev	1.178

0 10 20 30 40 50 60 70

ampl



# B1L003S, U26-ch72, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U26-ch73, adc0

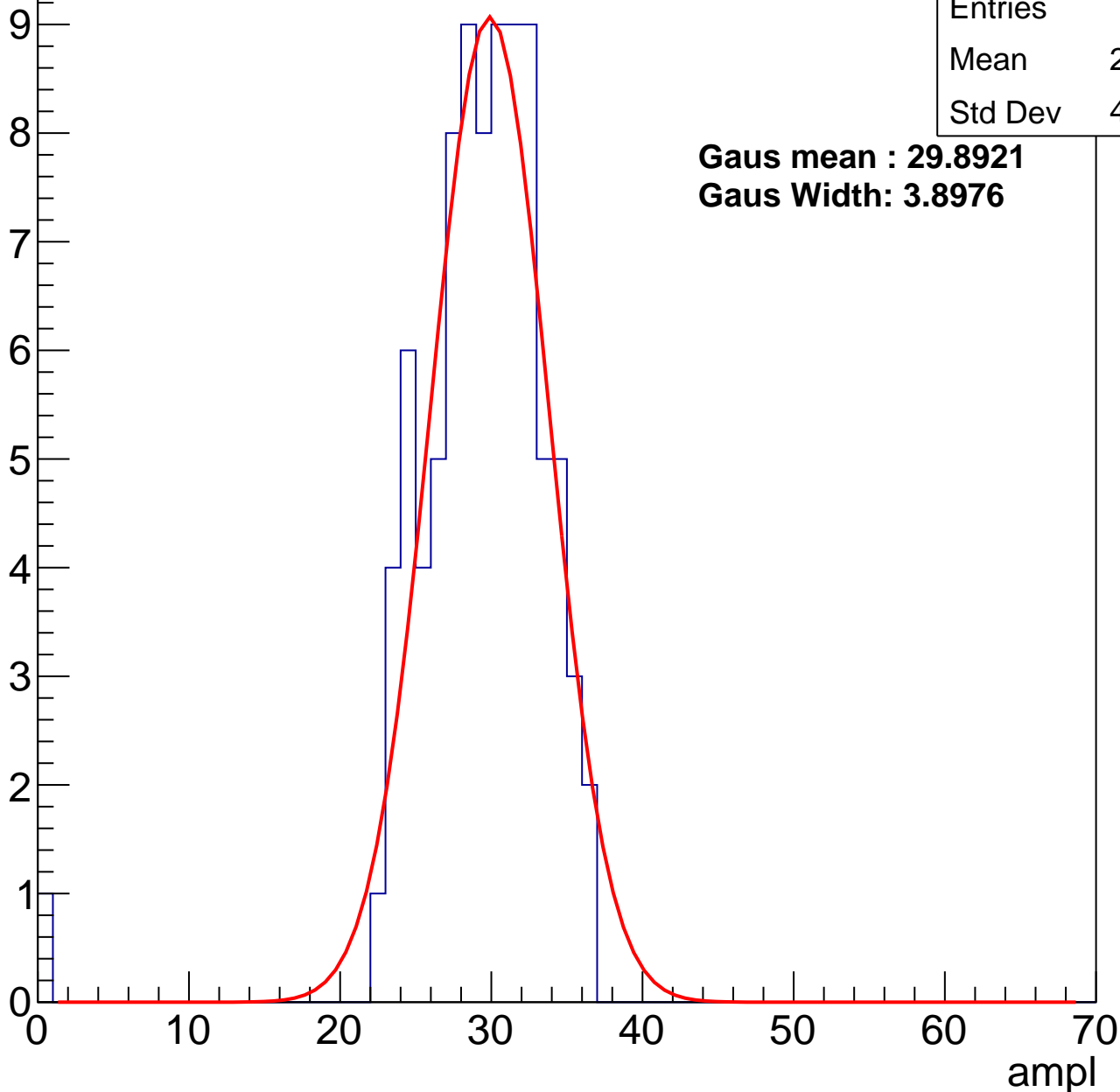
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	88
Mean	28.83
Std Dev	4.608

**Gaus mean : 29.8921**

**Gaus Width: 3.8976**

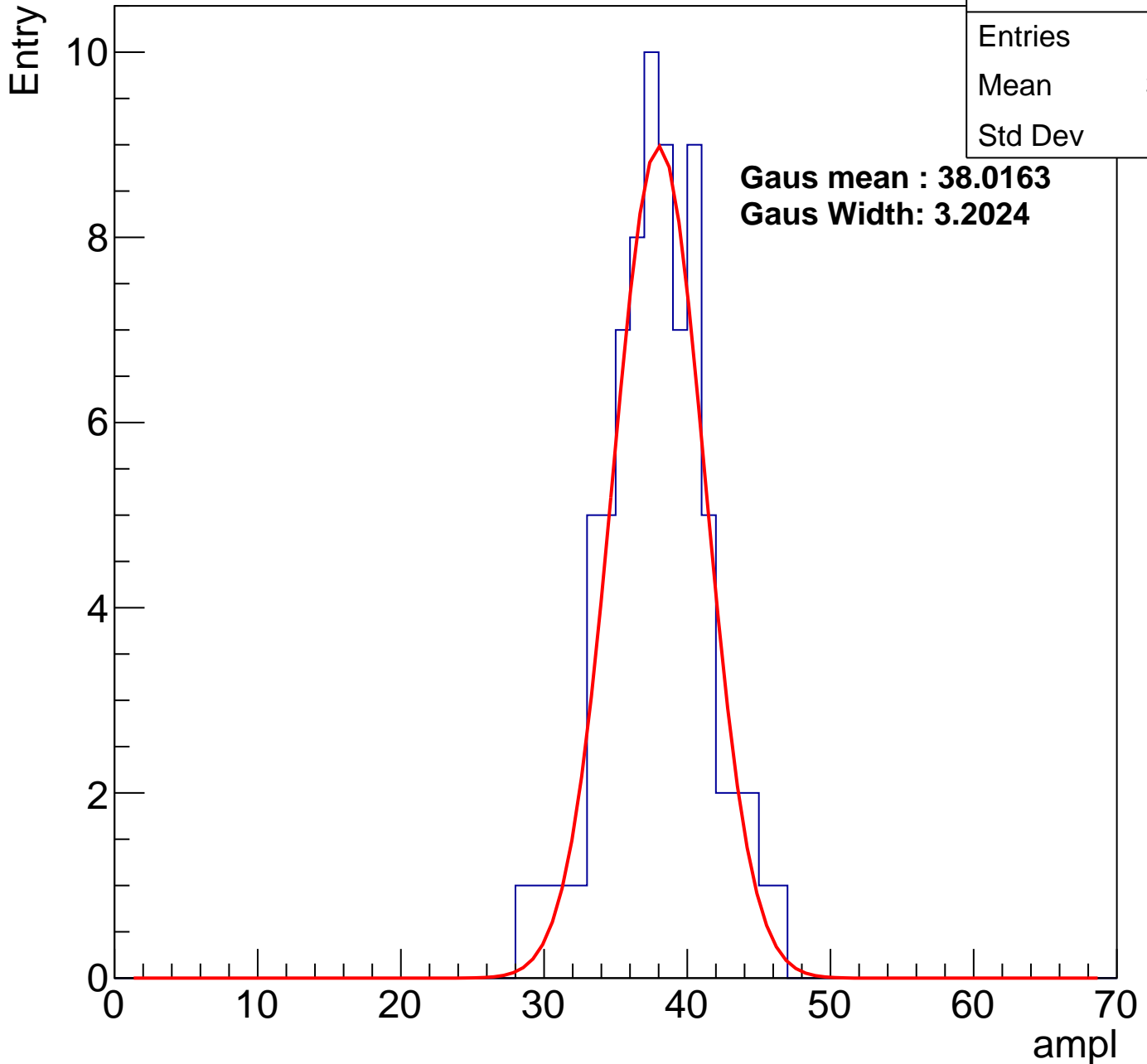


# B1L003S, U26-ch73, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	78
Mean	37.4
Std Dev	3.52

**Gaus mean : 38.0163**  
**Gaus Width: 3.2024**



# B1L003S, U26-ch73, adc2

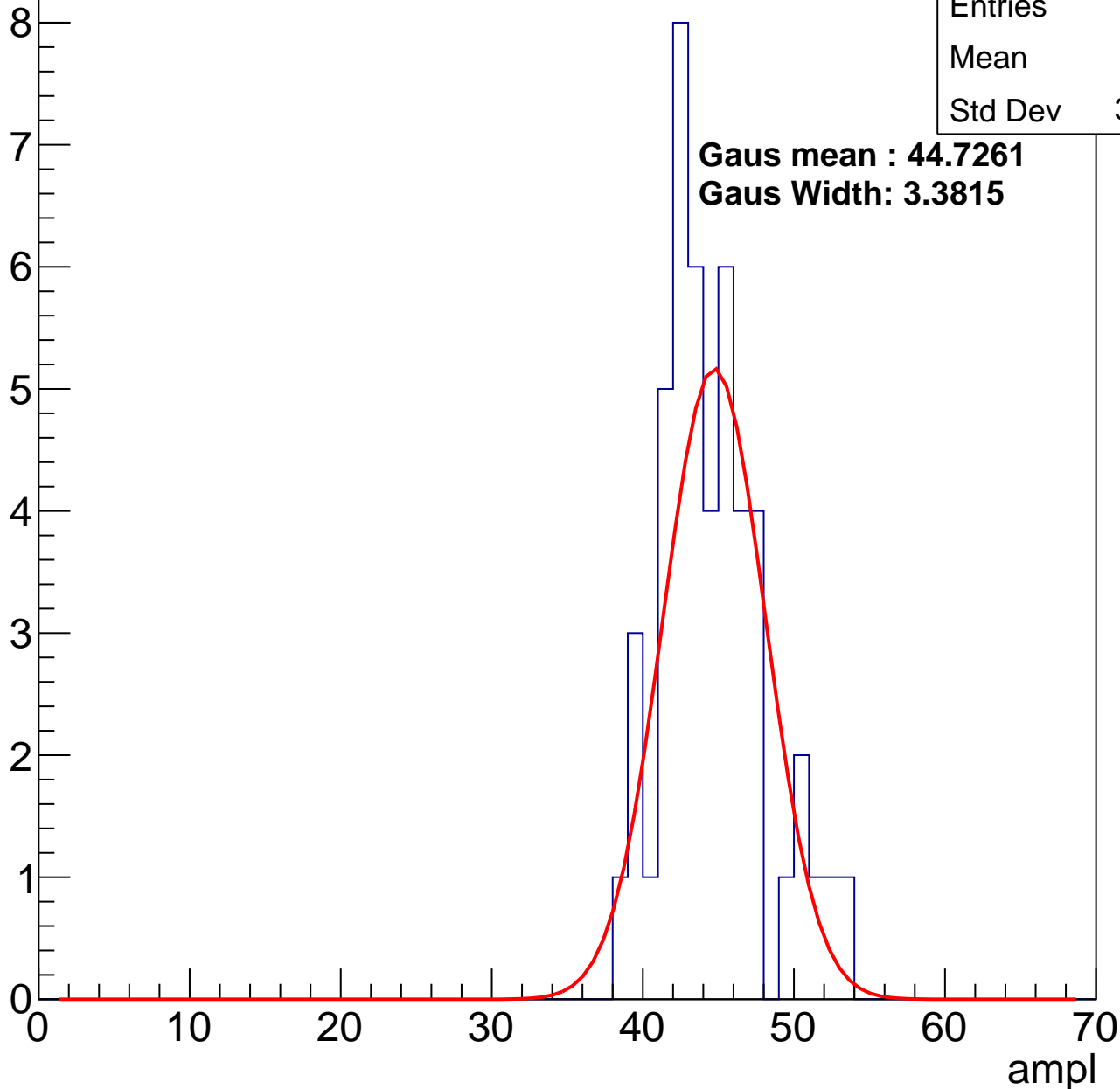
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	48
Mean	44.1
Std Dev	3.411

**Gaus mean : 44.7261**

**Gaus Width: 3.3815**



# B1L003S, U26-ch73, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

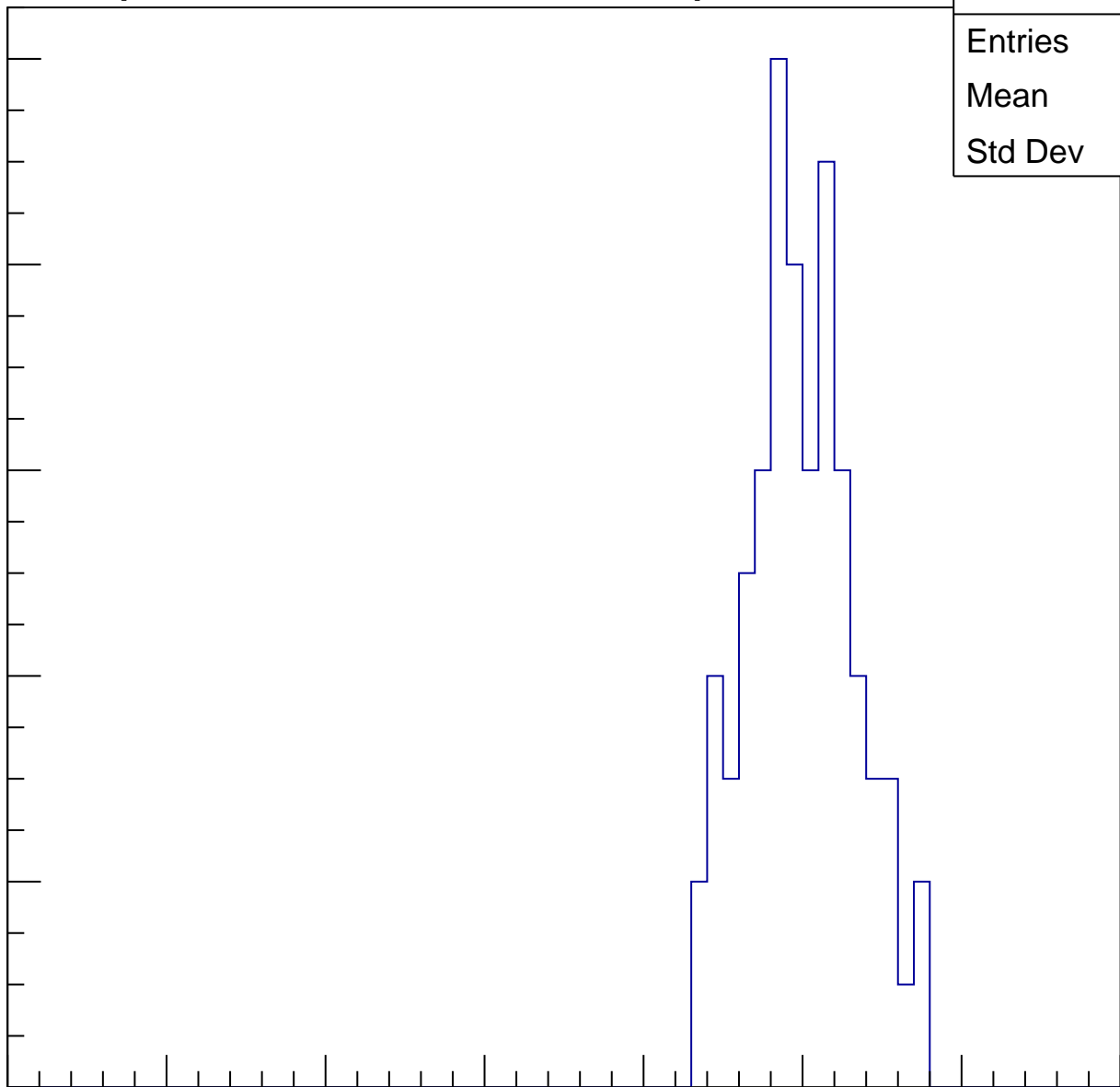
Entries	72
Mean	49.46
Std Dev	3.341

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

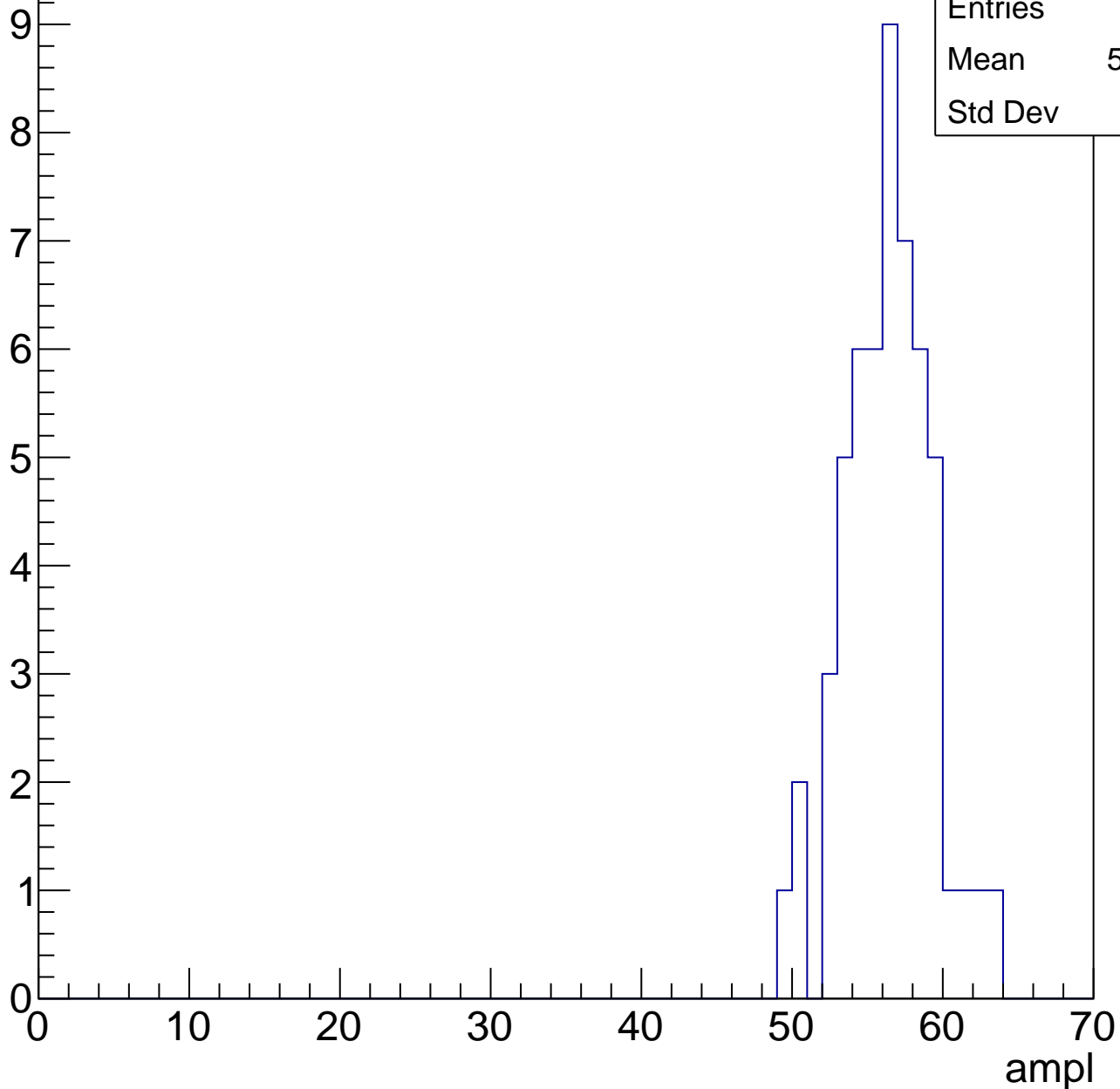
ampl



# B1L003S, U26-ch73, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



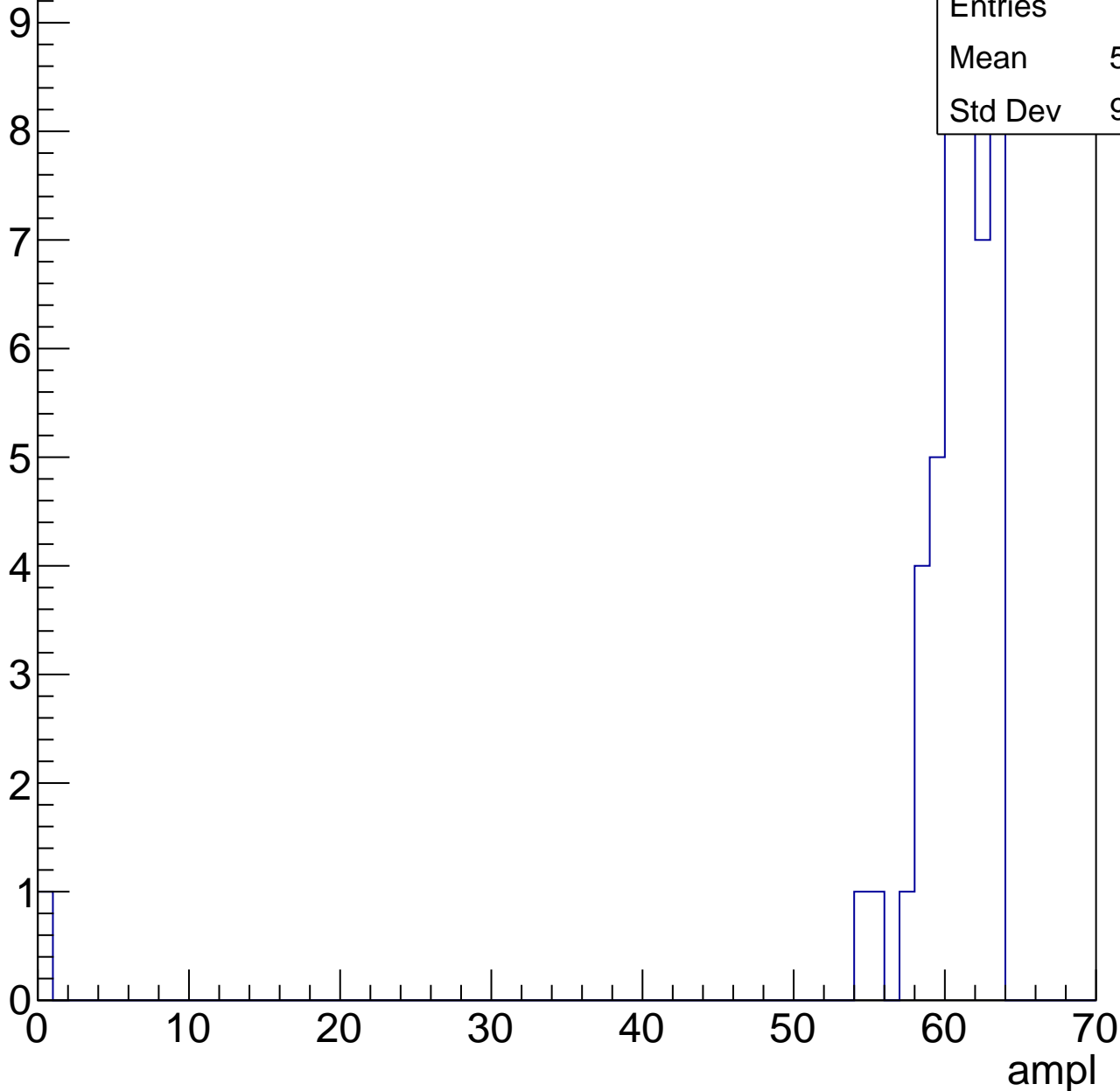
Entries	54
Mean	55.85
Std Dev	2.87

# B1L003S, U26-ch73, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	45
Mean	59.09
Std Dev	9.143



# B1L003S, U26-ch73, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	62
Std Dev	0.7071

ampl

0 10 20 30 40 50 60 70



# B1L003S, U26-ch73, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	21
Std Dev	0

ampl

# B1L003S, U26-ch74, adc0

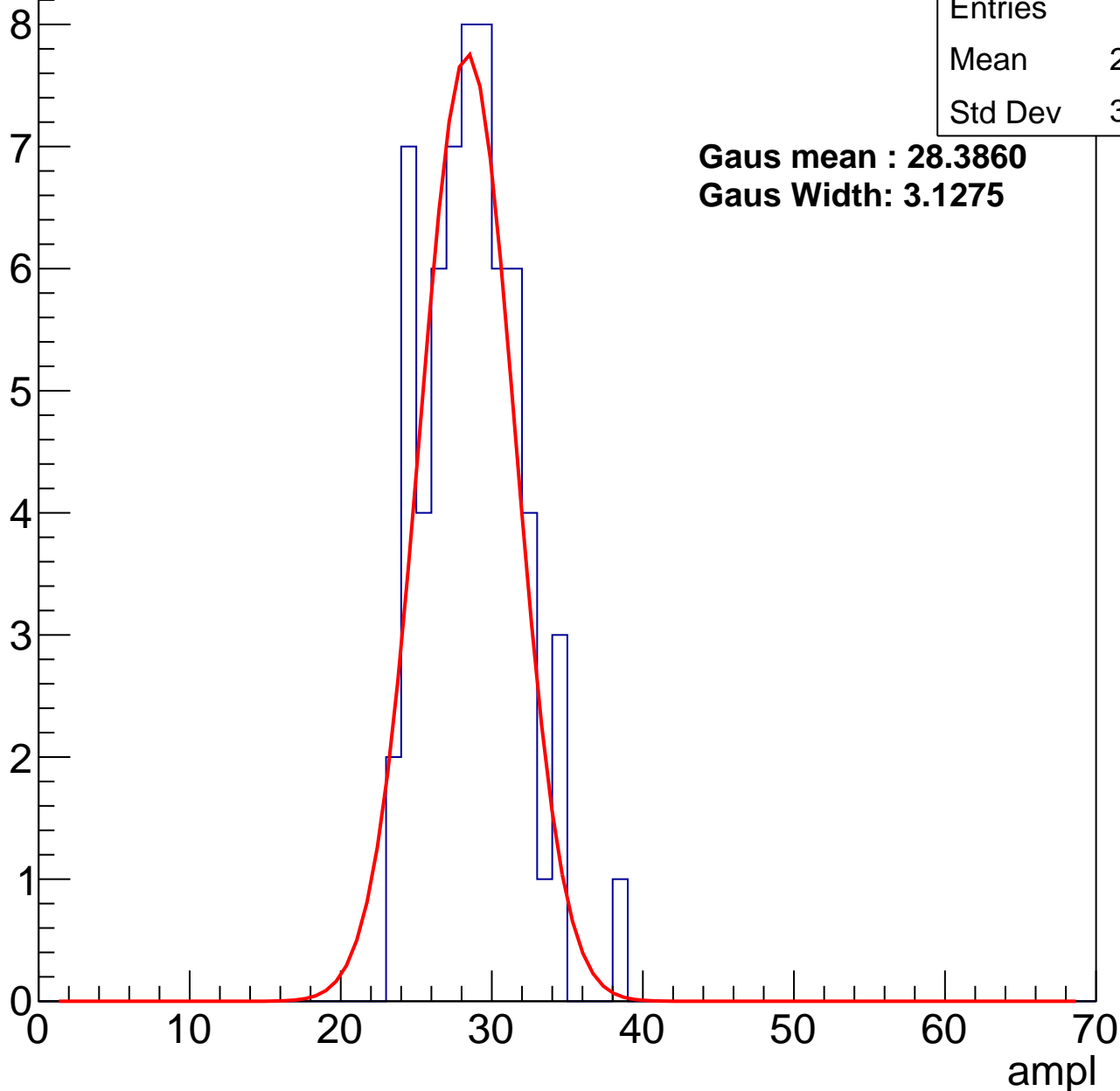
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	28.29
Std Dev	3.104

**Gaus mean : 28.3860**

**Gaus Width: 3.1275**



# B1L003S, U26-ch74, adc1

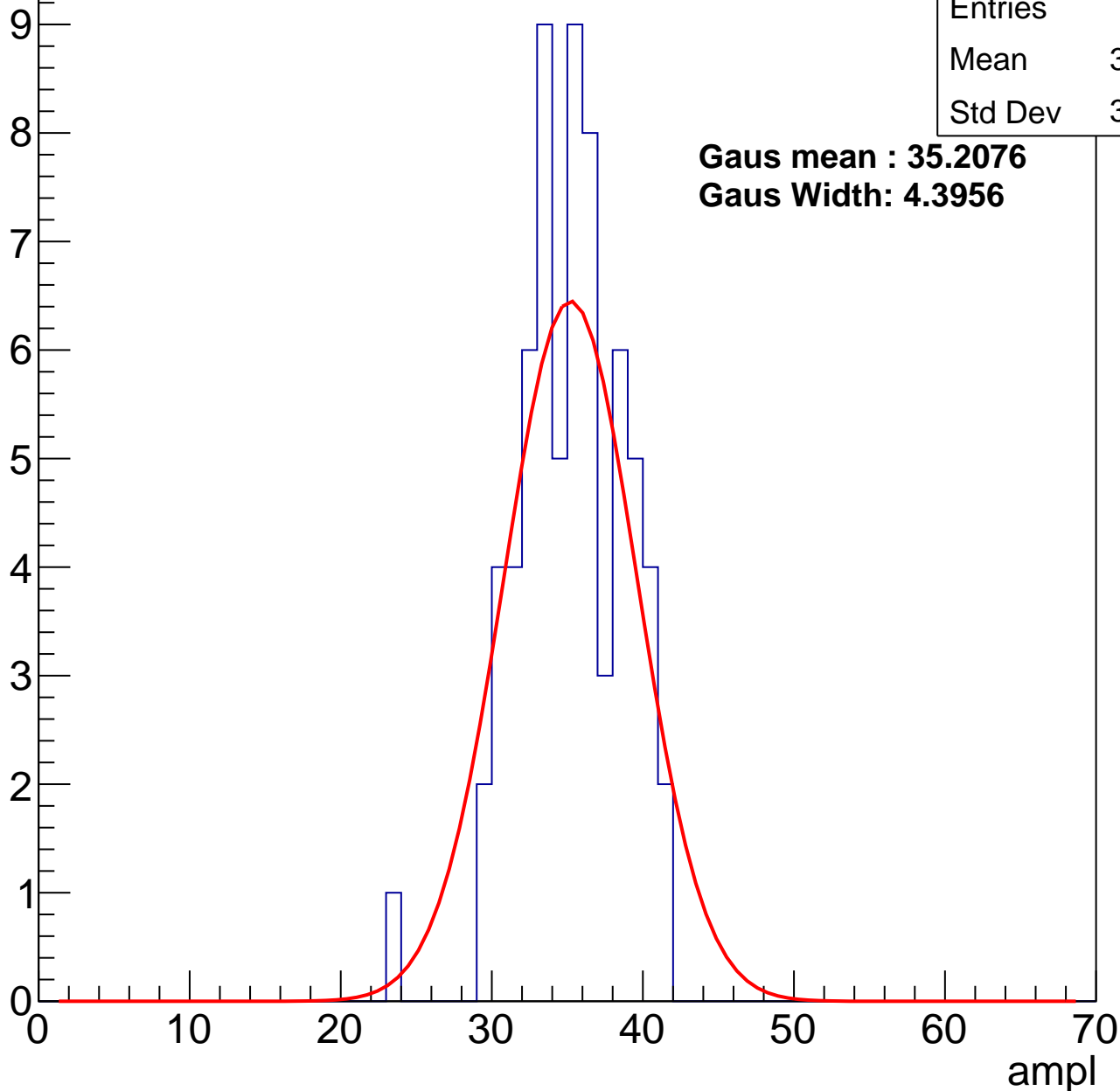
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	34.75
Std Dev	3.423

**Gaus mean : 35.2076**

**Gaus Width: 4.3956**



# B1L003S, U26-ch74, adc2

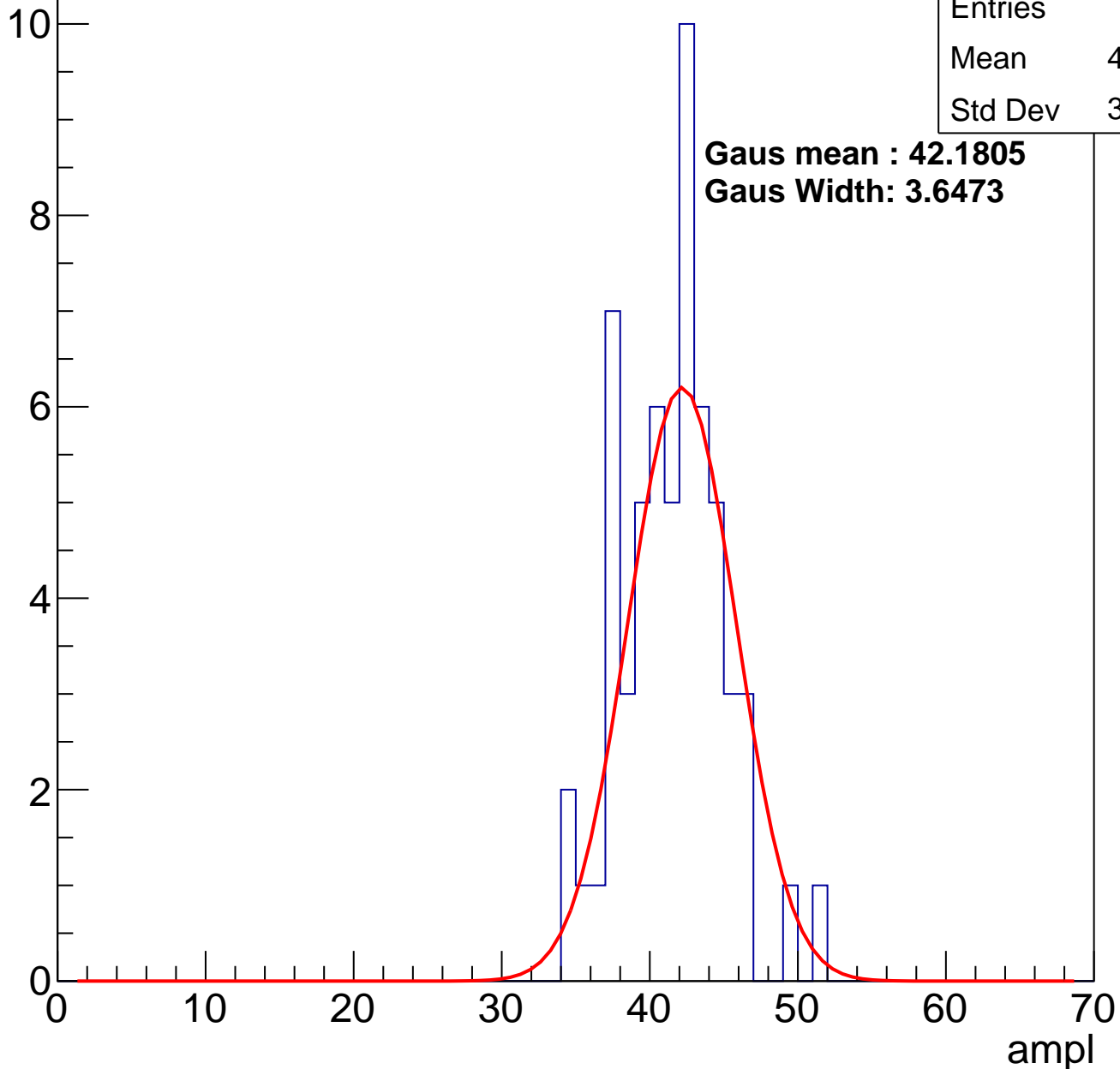
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	59
Mean	41.07
Std Dev	3.419

**Gaus mean : 42.1805**

**Gaus Width: 3.6473**

Entry

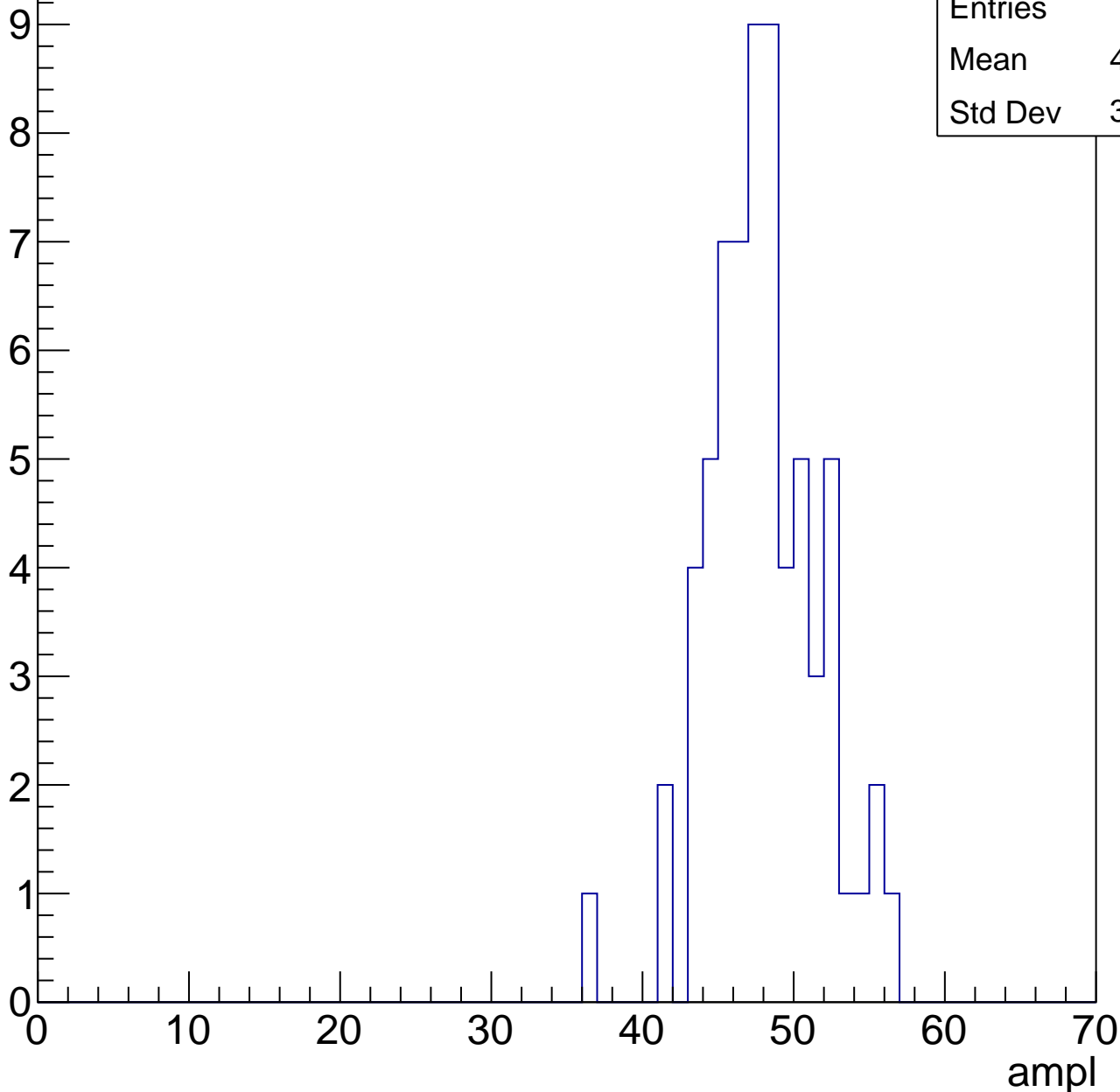


# B1L003S, U26-ch74, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	47.48
Std Dev	3.607

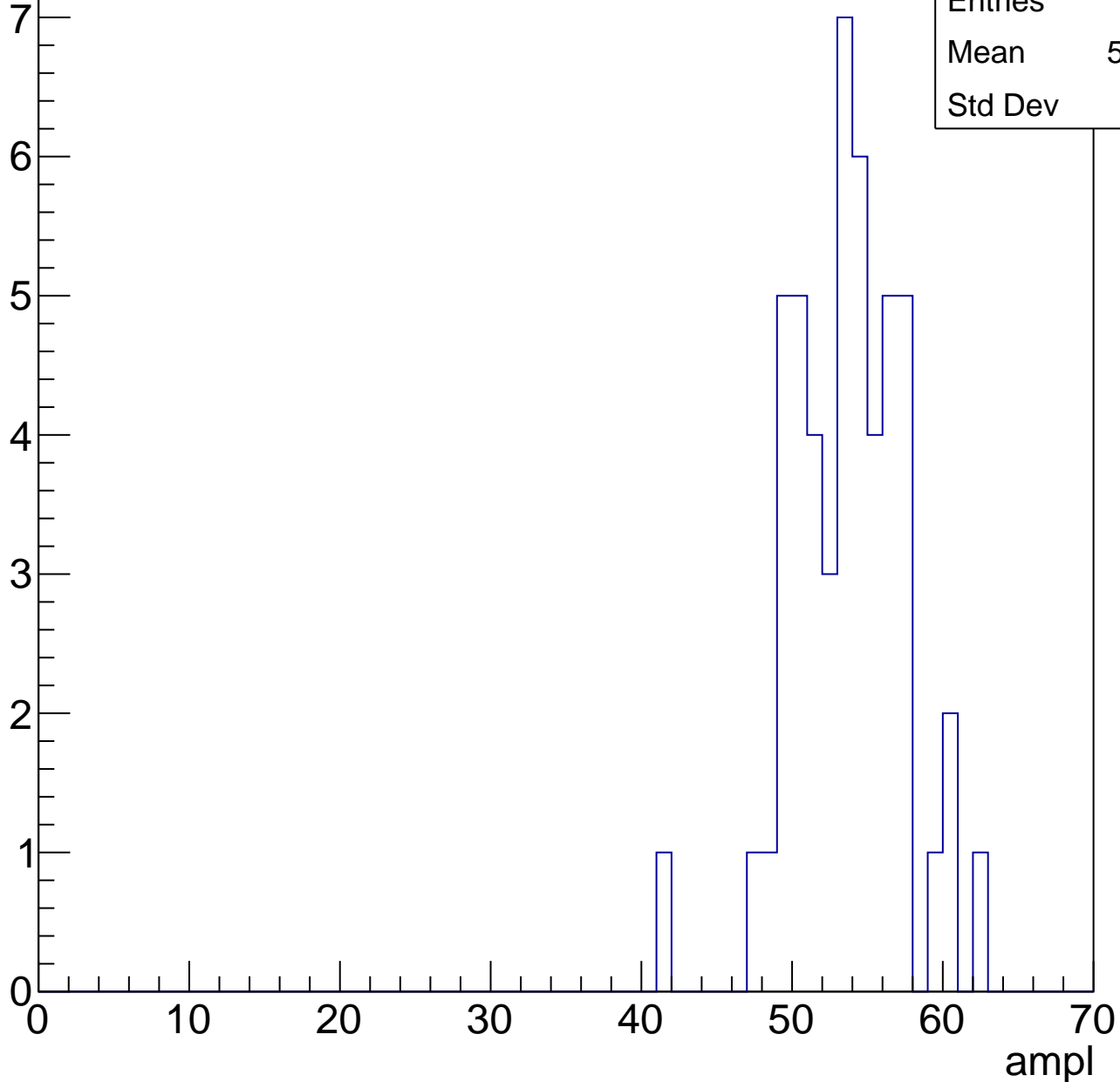


# B1L003S, U26-ch74, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	51
Mean	53.18
Std Dev	3.73



# B1L003S, U26-ch74, adc5

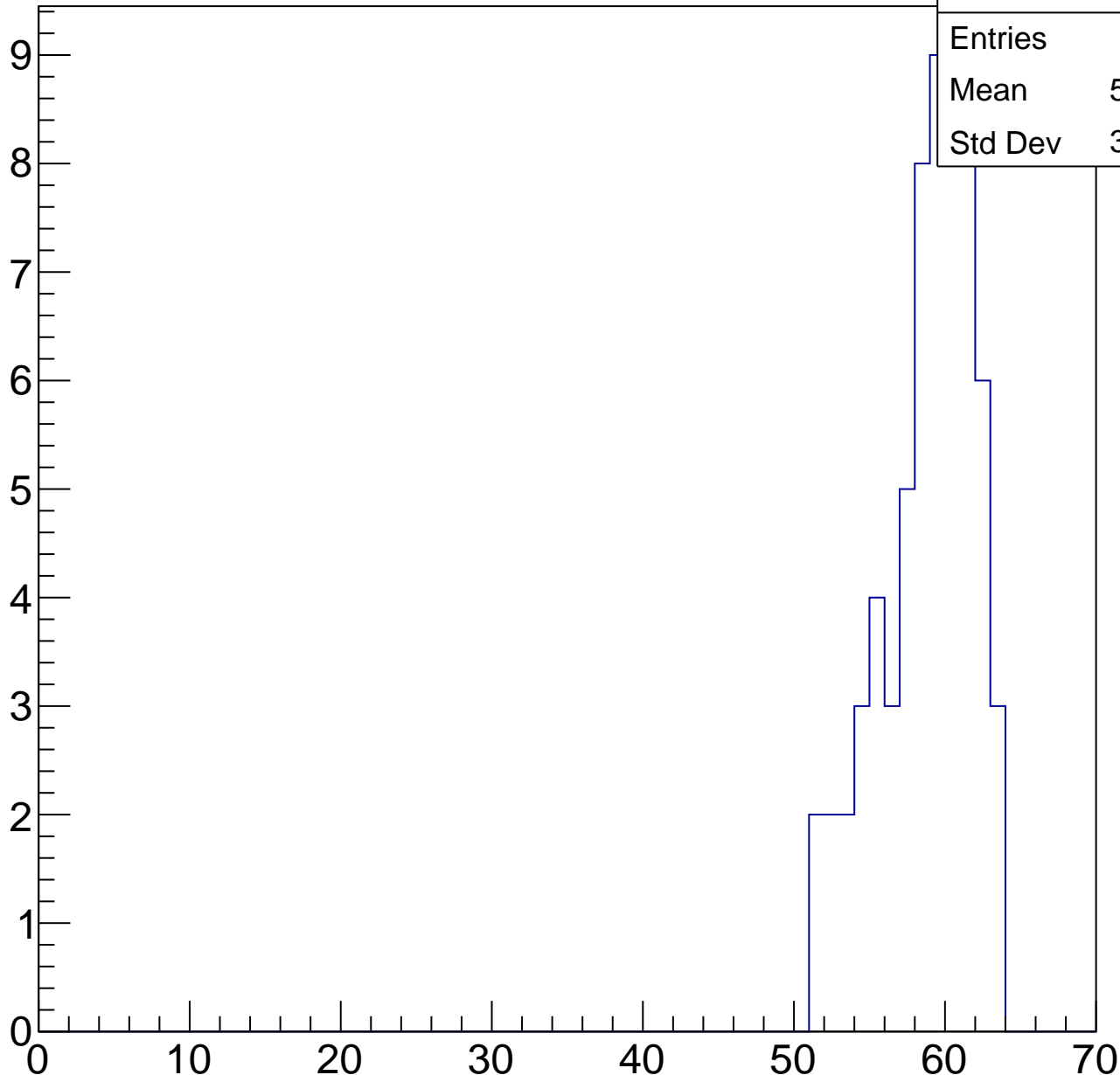
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	63
Mean	58.27
Std Dev	3.087

ampl

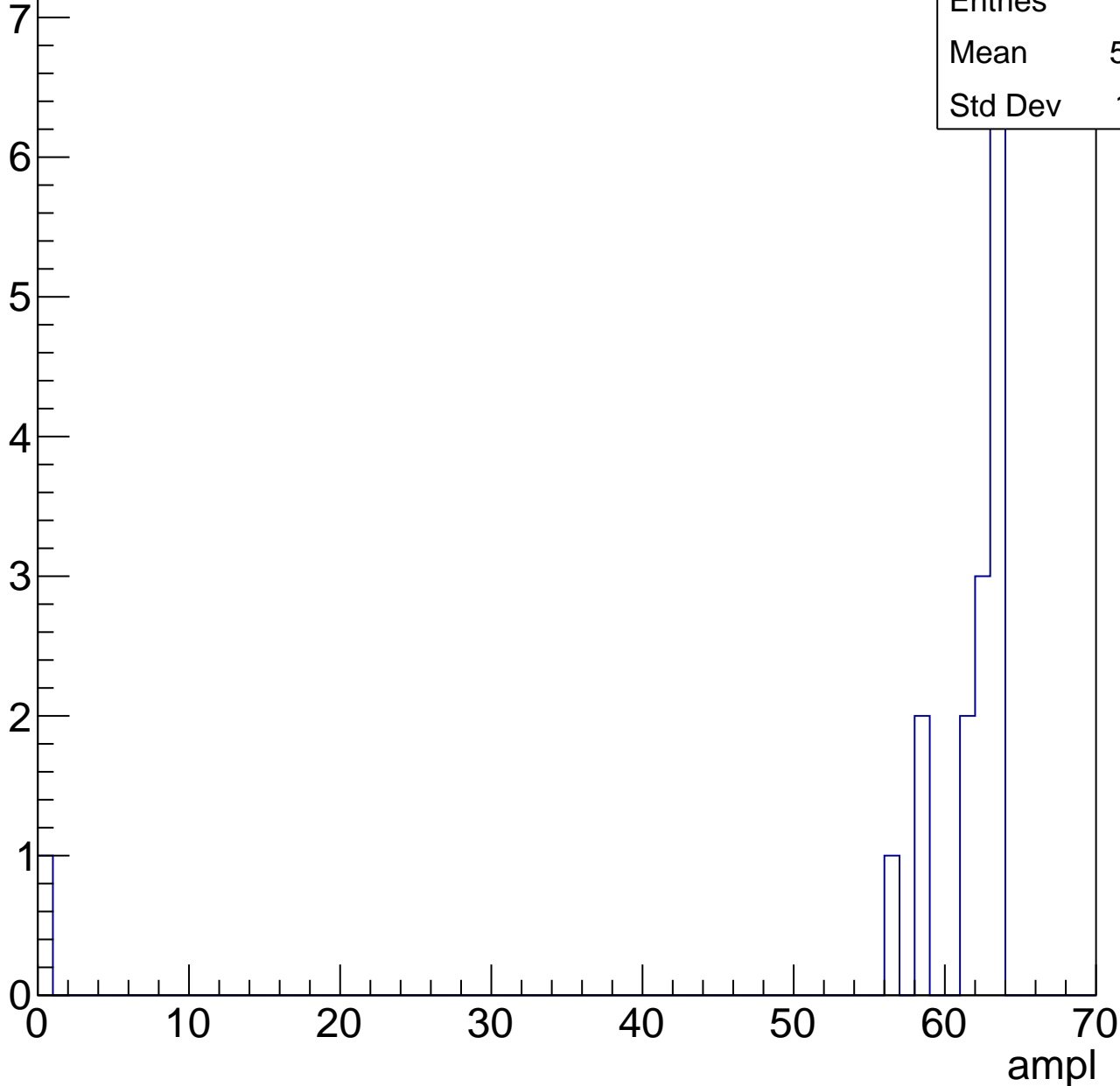


# B1L003S, U26-ch74, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	16
Mean	57.56
Std Dev	15.01

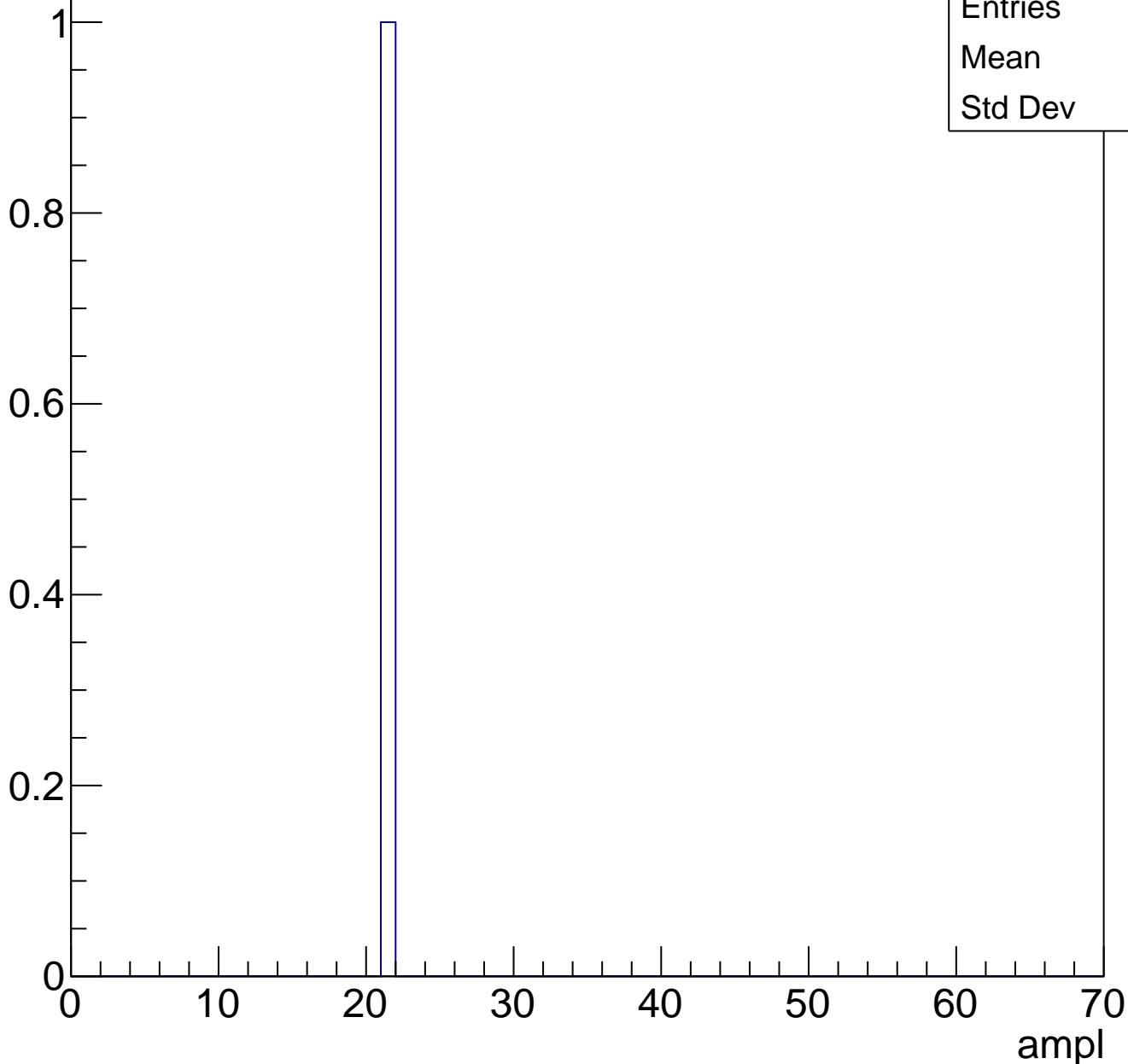




# B1L003S, U26-ch74, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U26-ch75, adc0

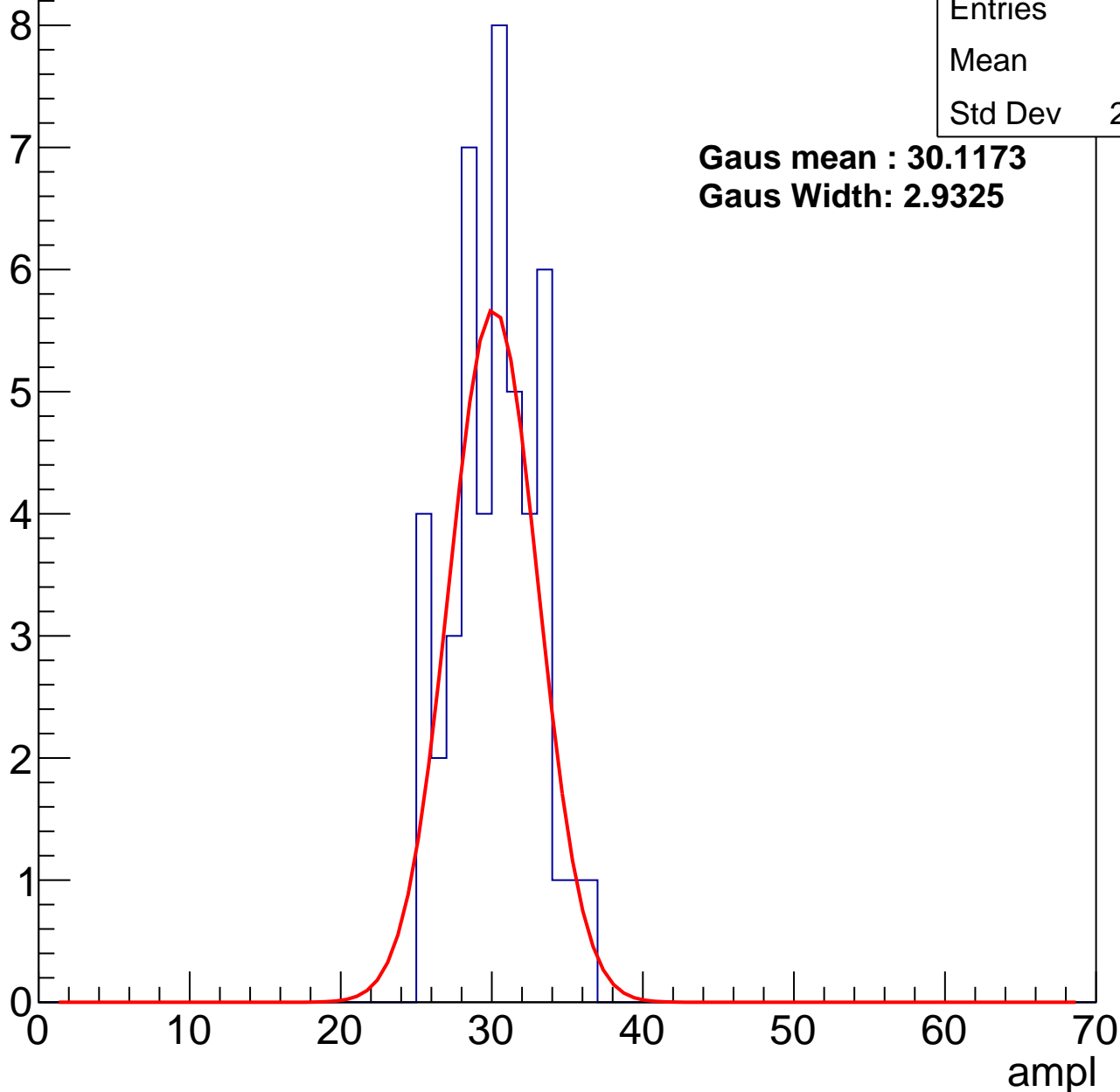
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	46
Mean	29.8
Std Dev	2.724

**Gaus mean : 30.1173**

**Gaus Width: 2.9325**



# B1L003S, U26-ch75, adc1

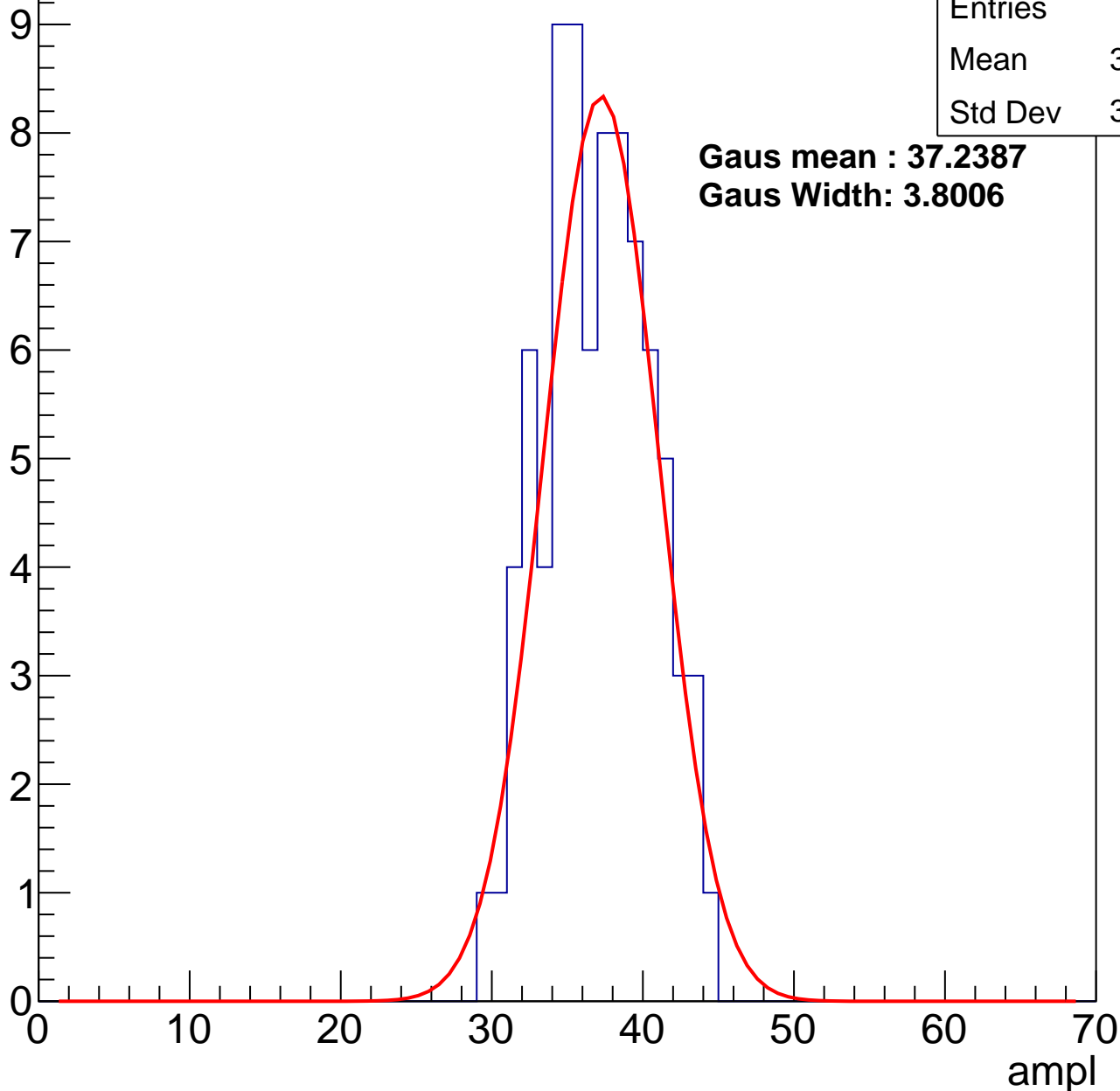
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	81
Mean	36.56
Std Dev	3.478

**Gaus mean : 37.2387**

**Gaus Width: 3.8006**



# B1L003S, U26-ch75, adc2

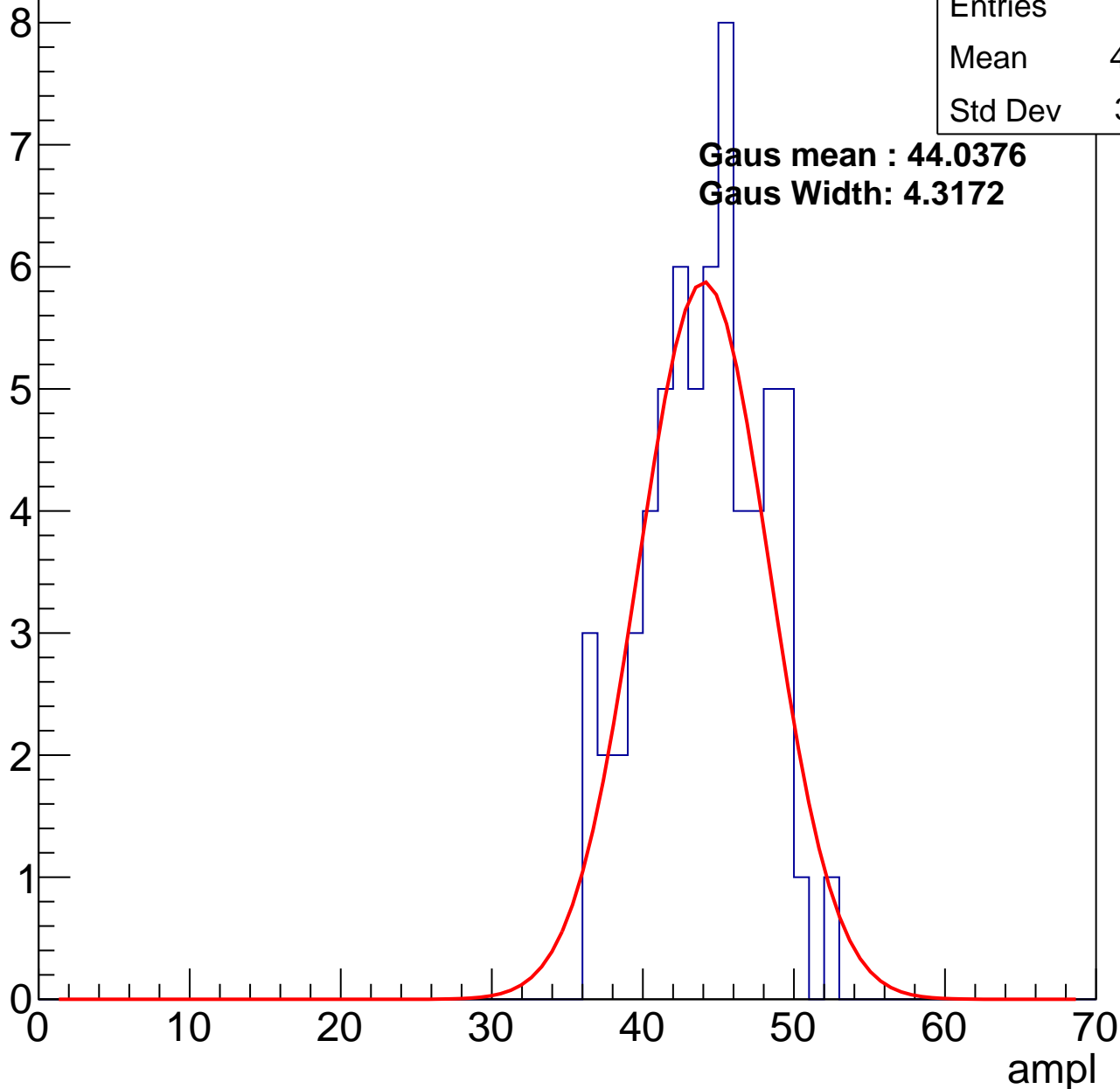
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	43.59
Std Dev	3.811

**Gaus mean : 44.0376**

**Gaus Width: 4.3172**

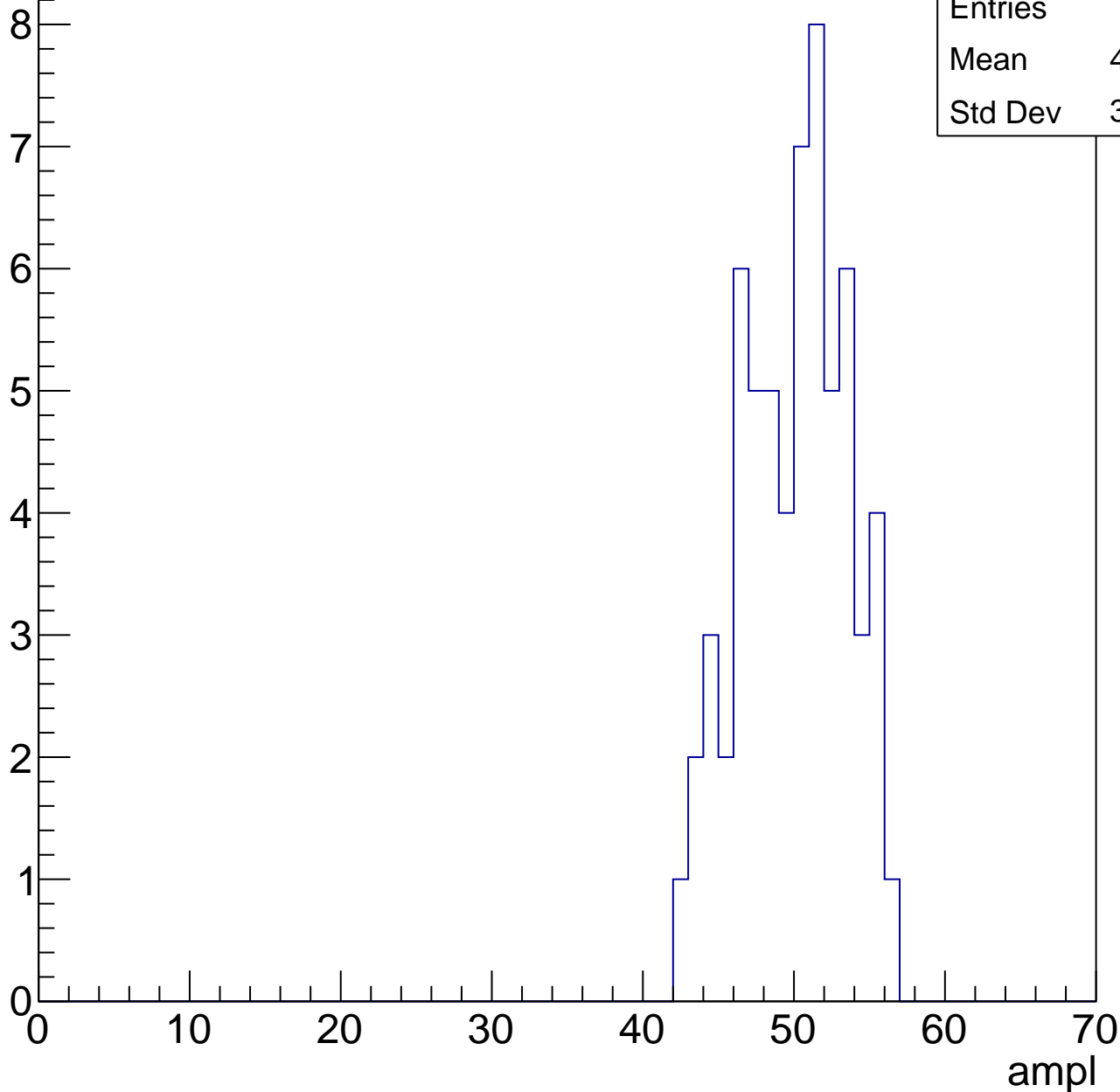


# B1L003S, U26-ch75, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	49.53
Std Dev	3.449

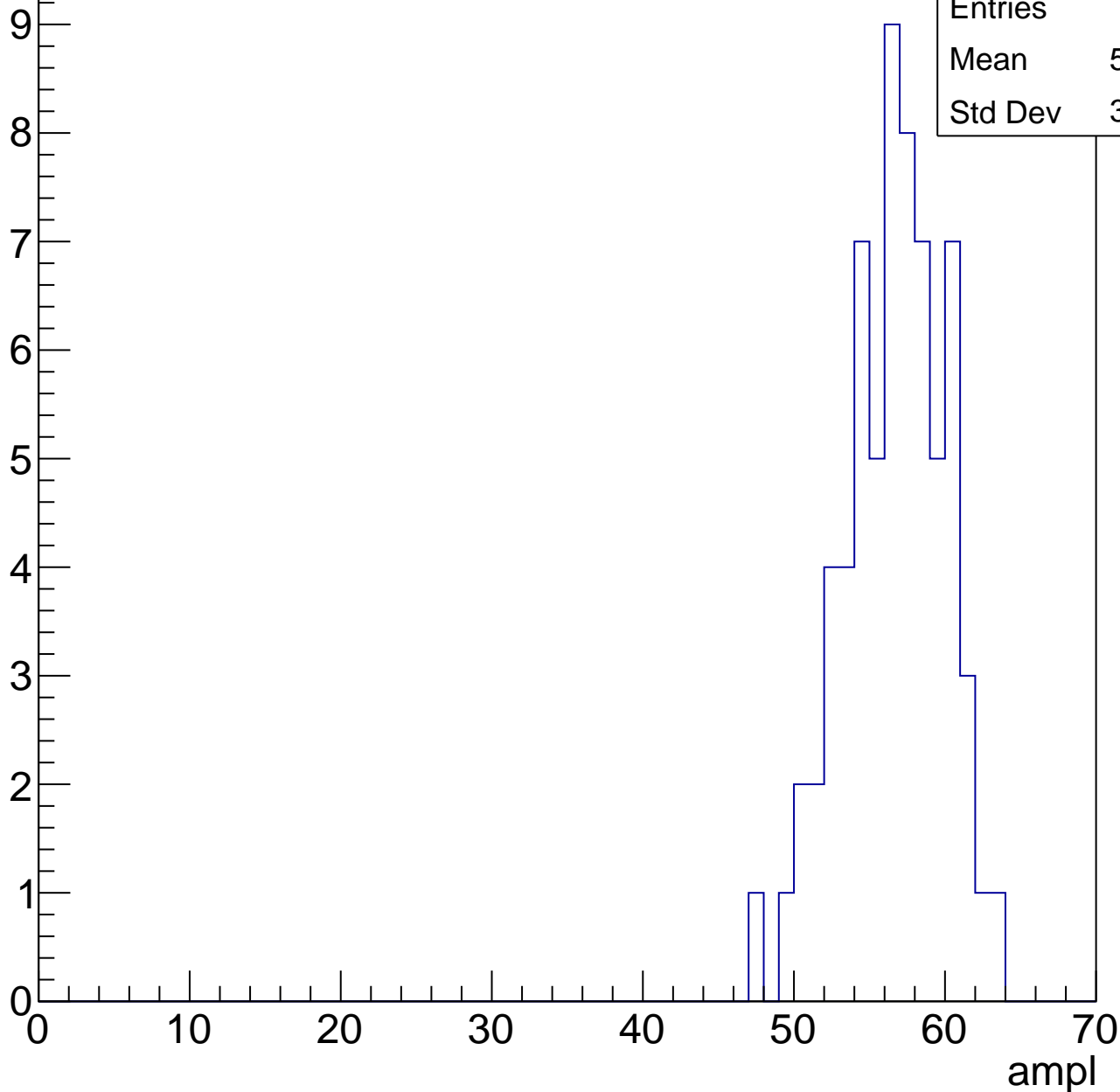


# B1L003S, U26-ch75, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	56.12
Std Dev	3.317

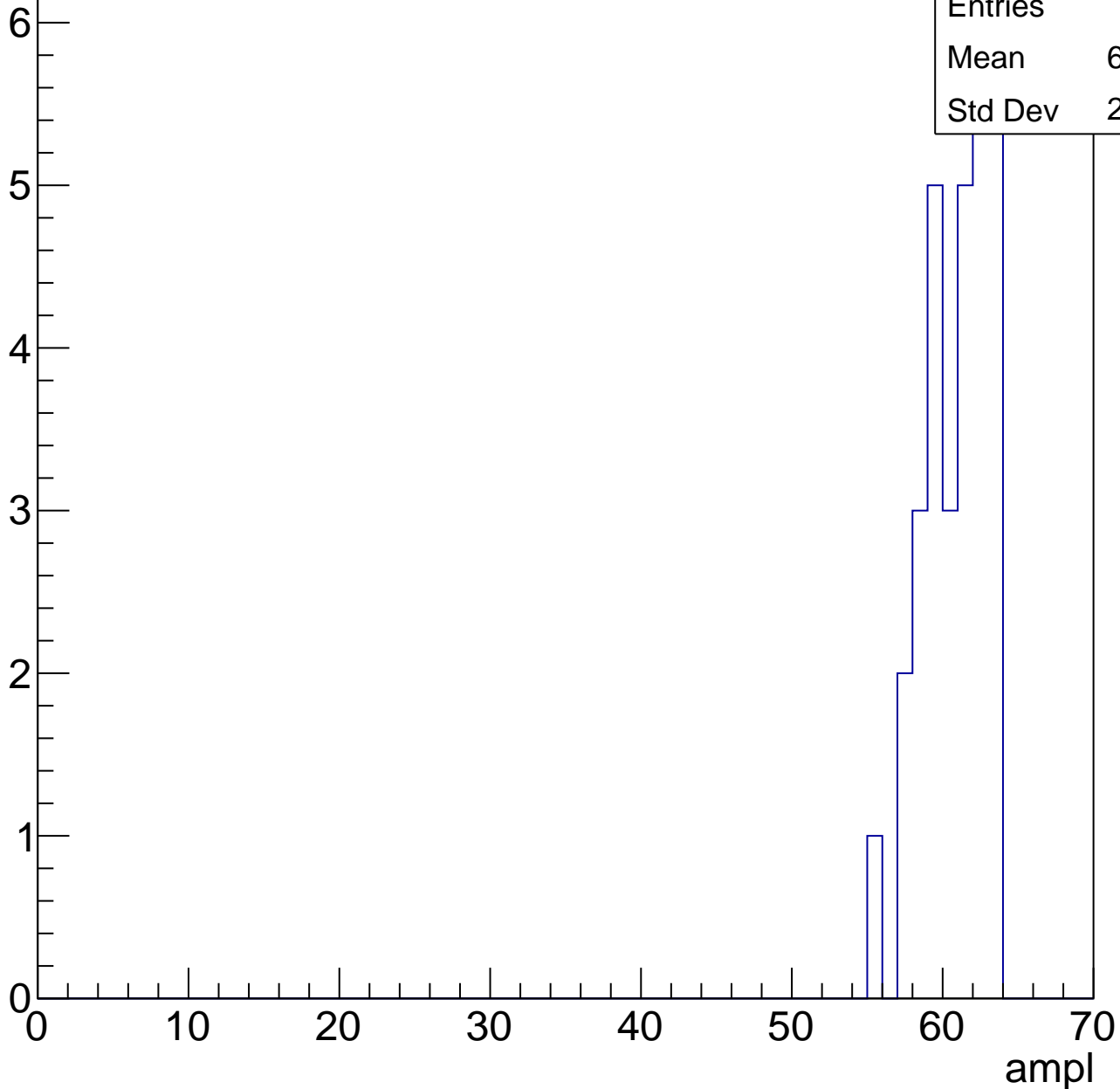


# B1L003S, U26-ch75, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	31
Mean	60.42
Std Dev	2.106



# B1L003S, U26-ch75, adc6

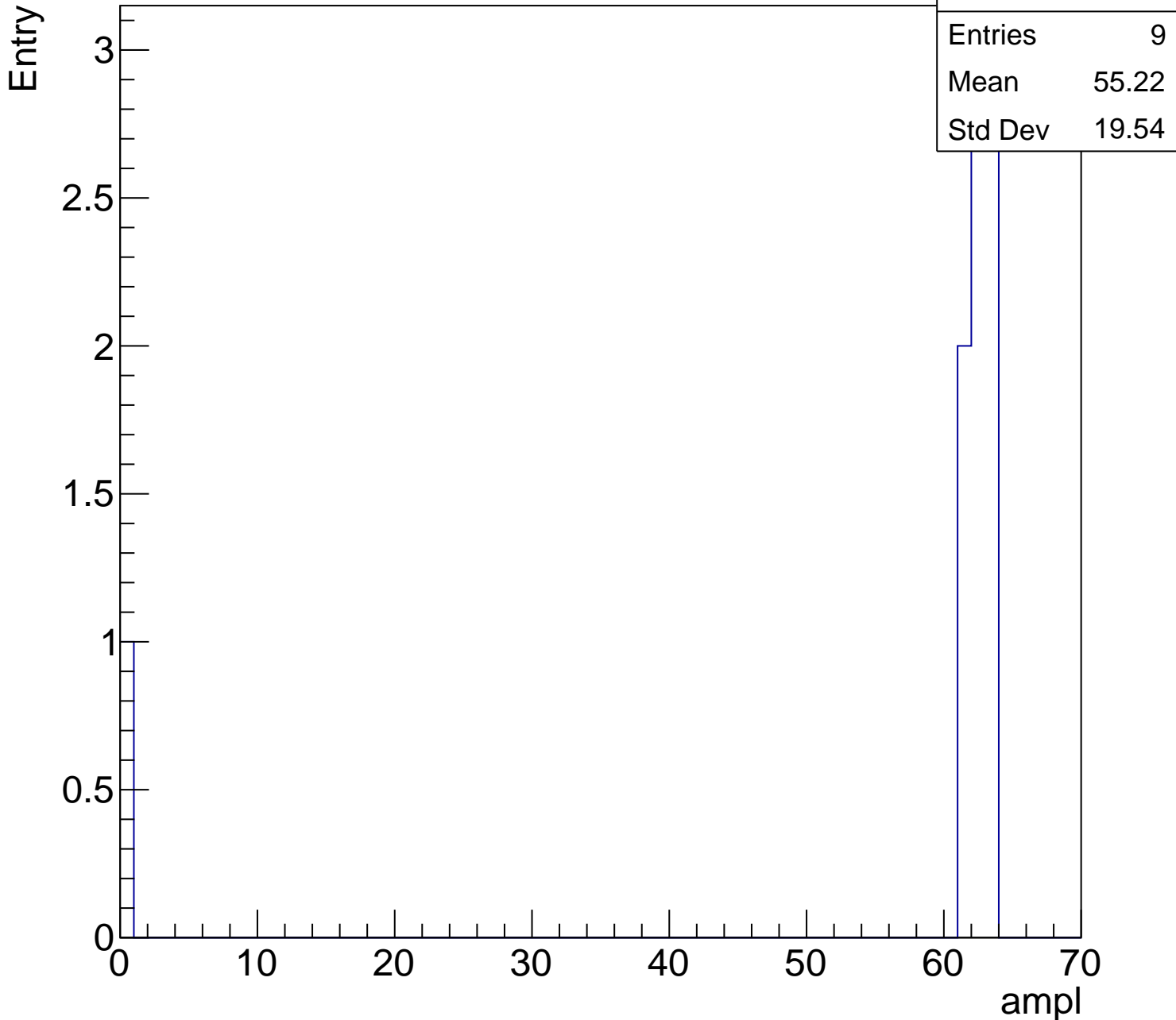
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

3  
2.5  
2  
1.5  
1  
0.5  
0

Entries	9
Mean	55.22
Std Dev	19.54

ampl





# B1L003S, U26-ch75, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	12
Std Dev	12

# B1L003S, U26-ch76, adc0

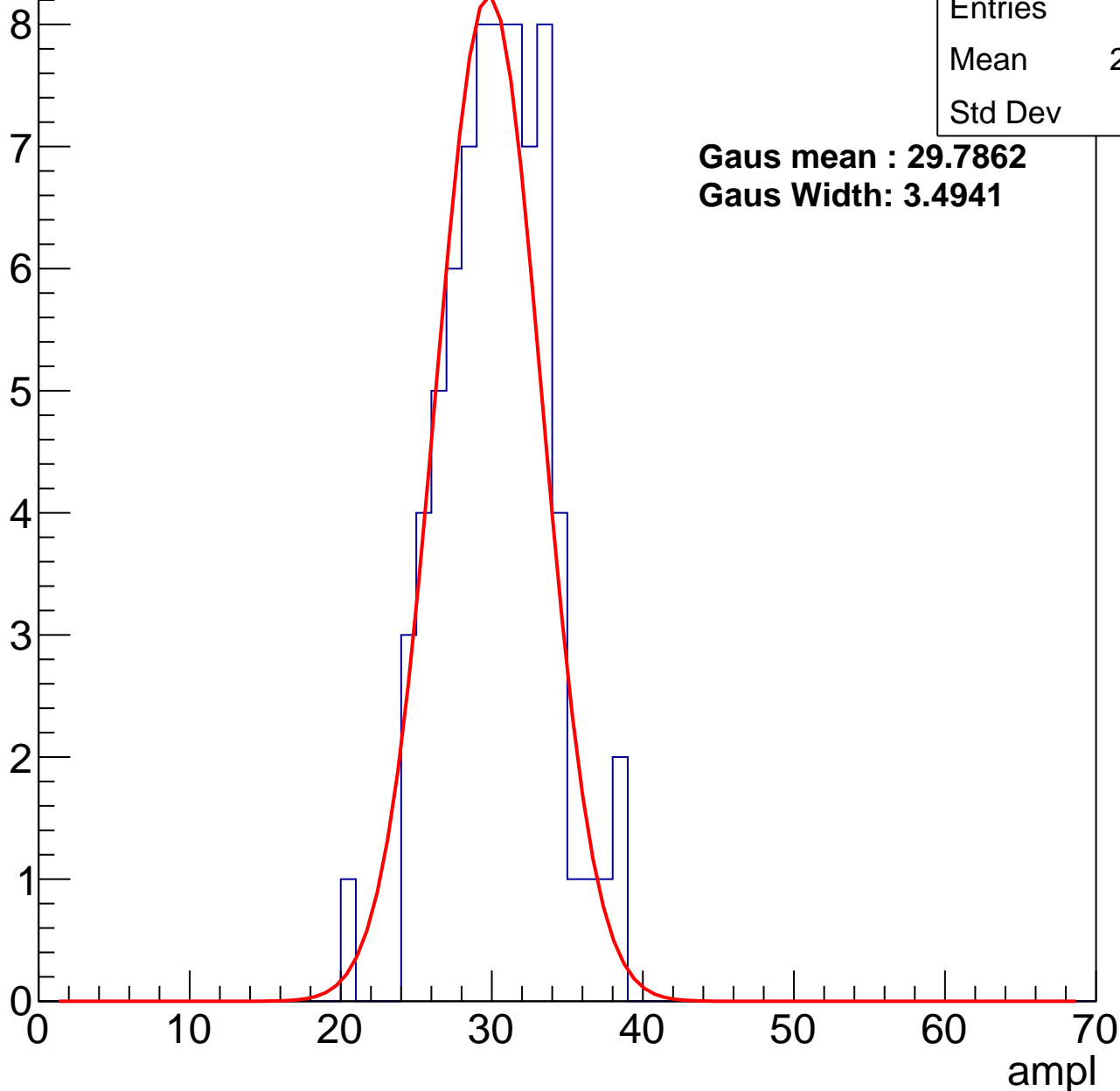
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	74
Mean	29.84
Std Dev	3.46

**Gaus mean : 29.7862**

**Gaus Width: 3.4941**



# B1L003S, U26-ch76, adc1

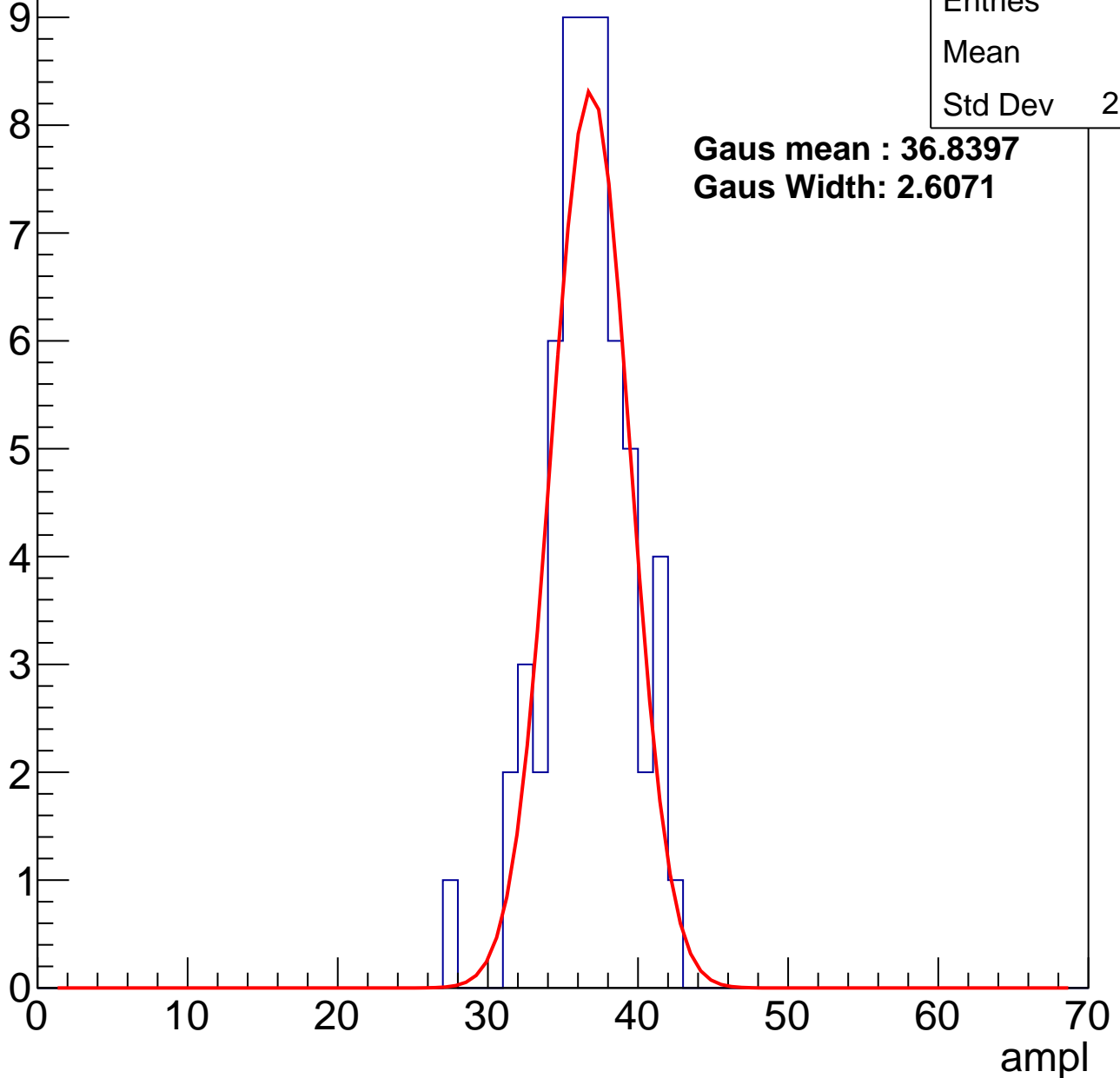
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	36.2
Std Dev	2.833

**Gaus mean : 36.8397**

**Gaus Width: 2.6071**



# B1L003S, U26-ch76, adc2

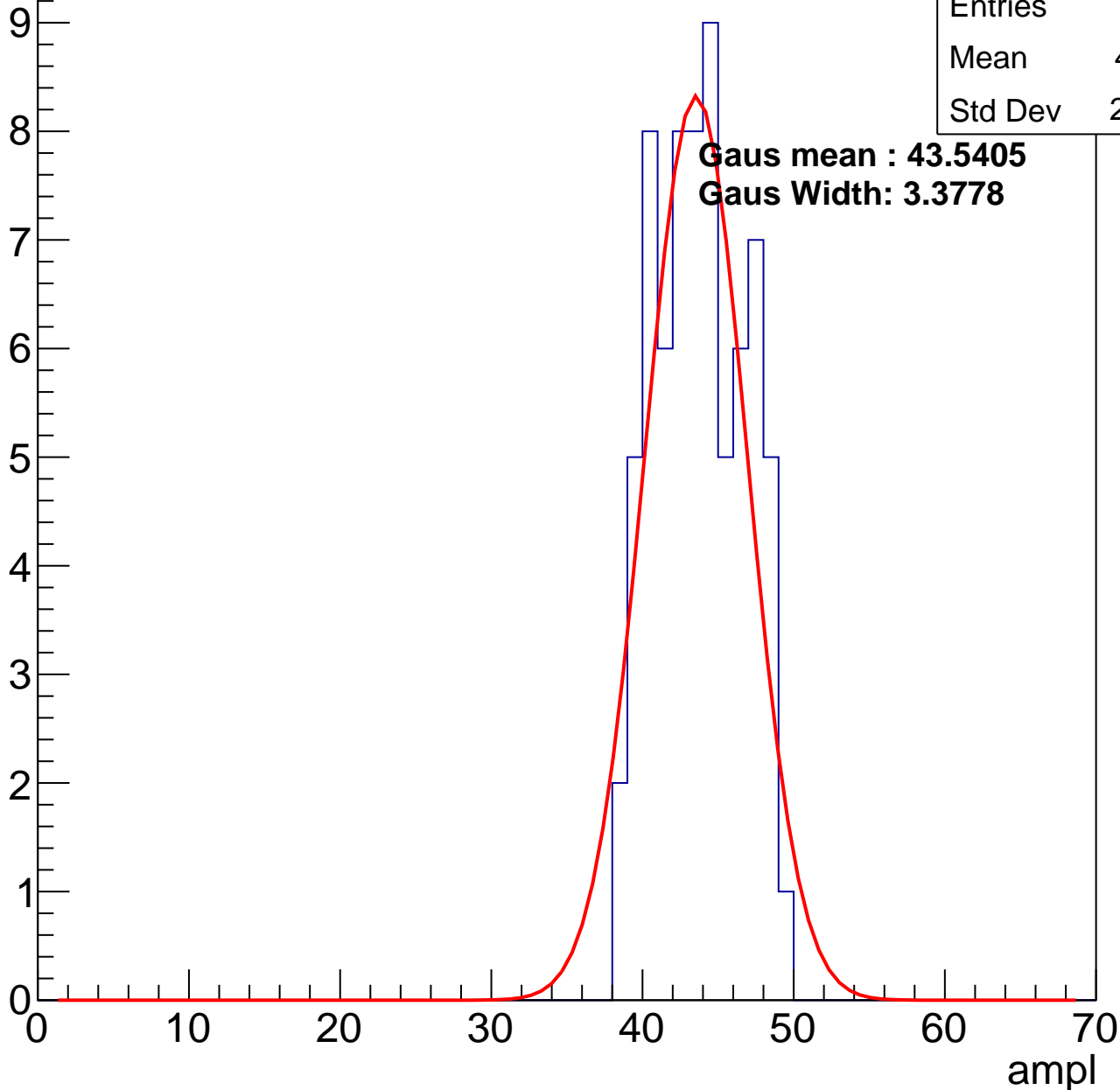
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	43.31
Std Dev	2.886

**Gaus mean : 43.5405**

**Gaus Width: 3.3778**

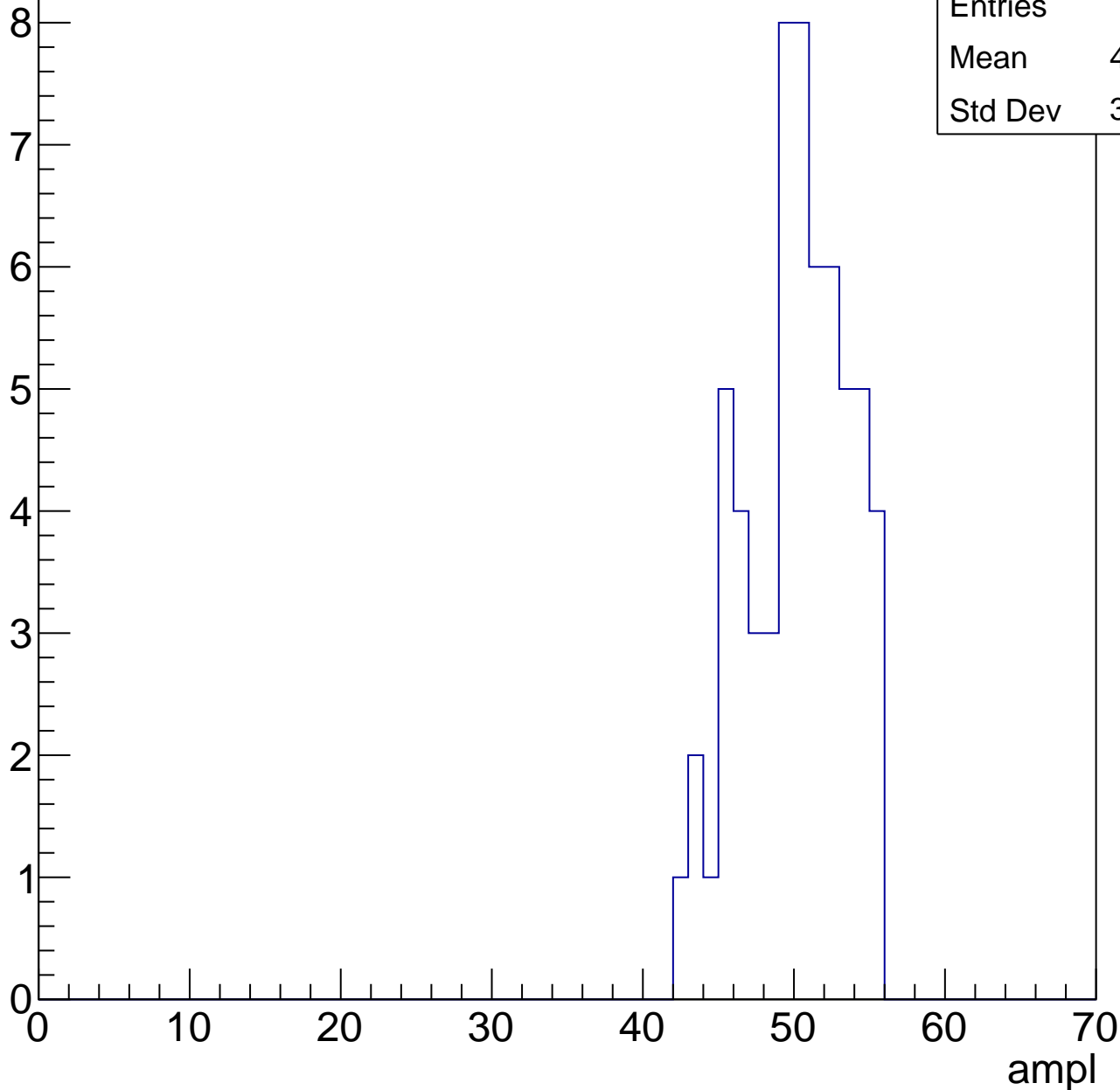


# B1L003S, U26-ch76, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	49.69
Std Dev	3.346

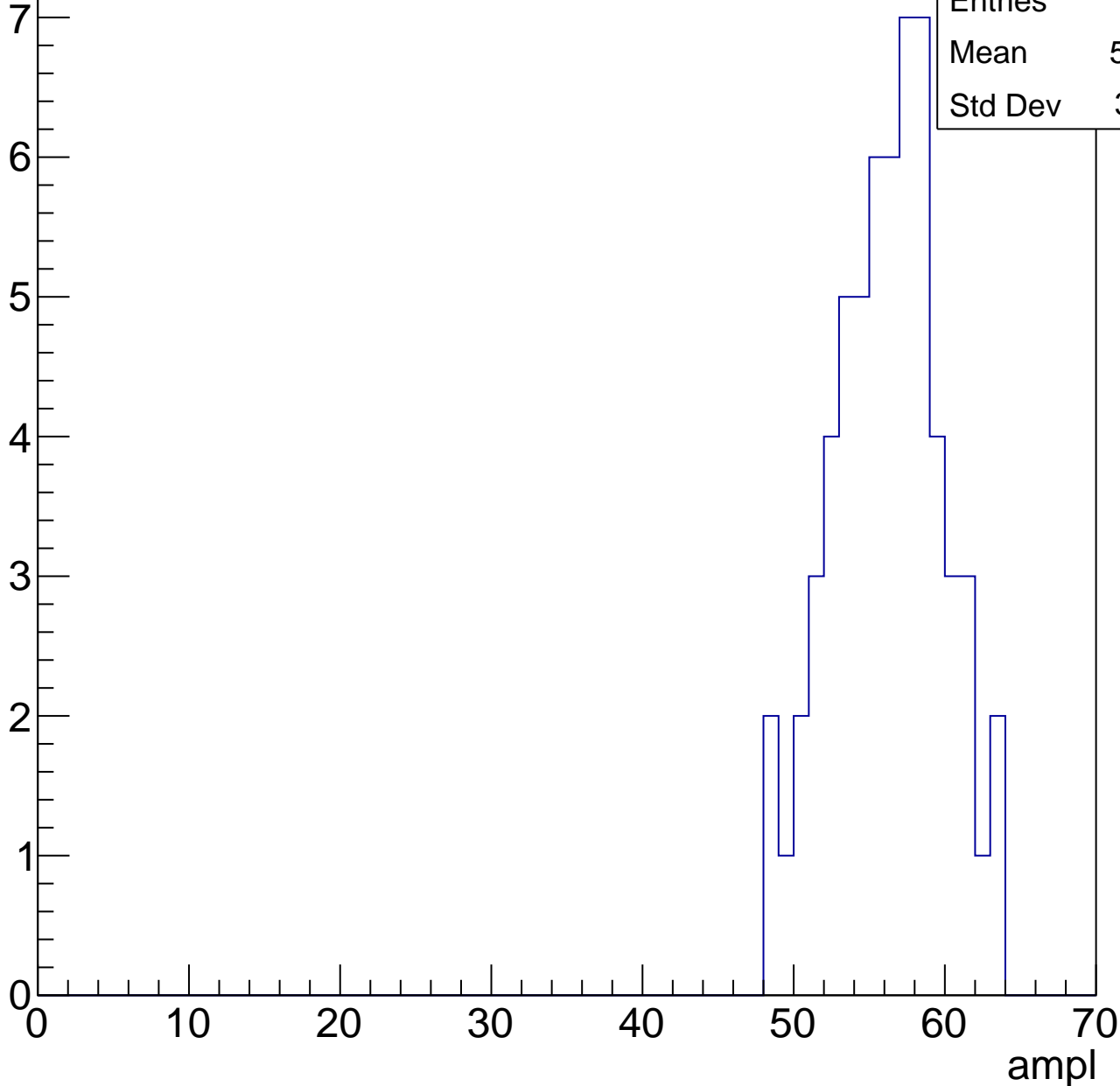


# B1L003S, U26-ch76, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	55.72
Std Dev	3.581



# B1L003S, U26-ch76, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

7

6

5

4

3

2

1

0

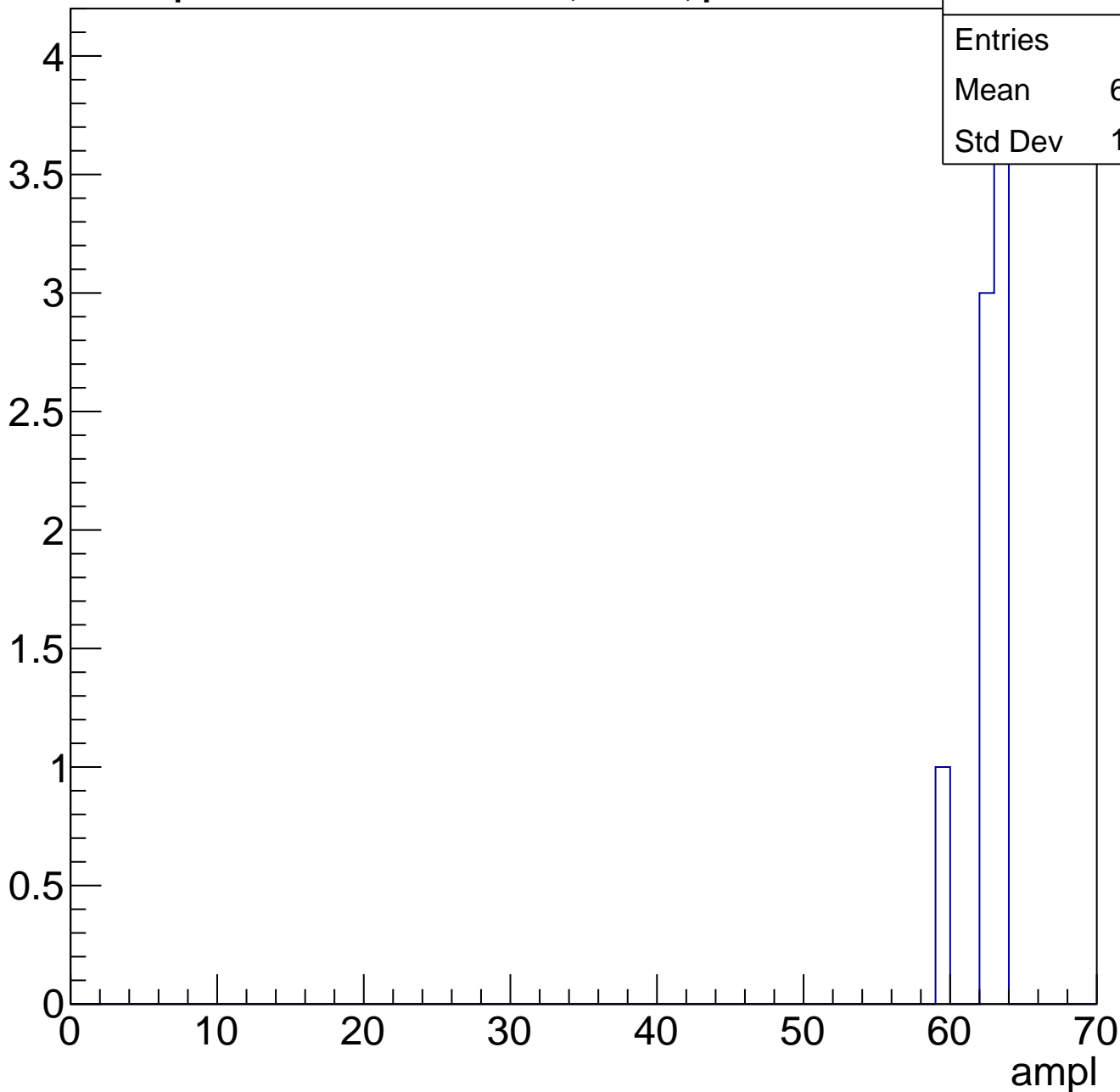
Entries	41
Mean	58.2
Std Dev	9.528

ampl

# B1L003S, U26-ch76, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch76, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L003S, U26-ch77, adc0

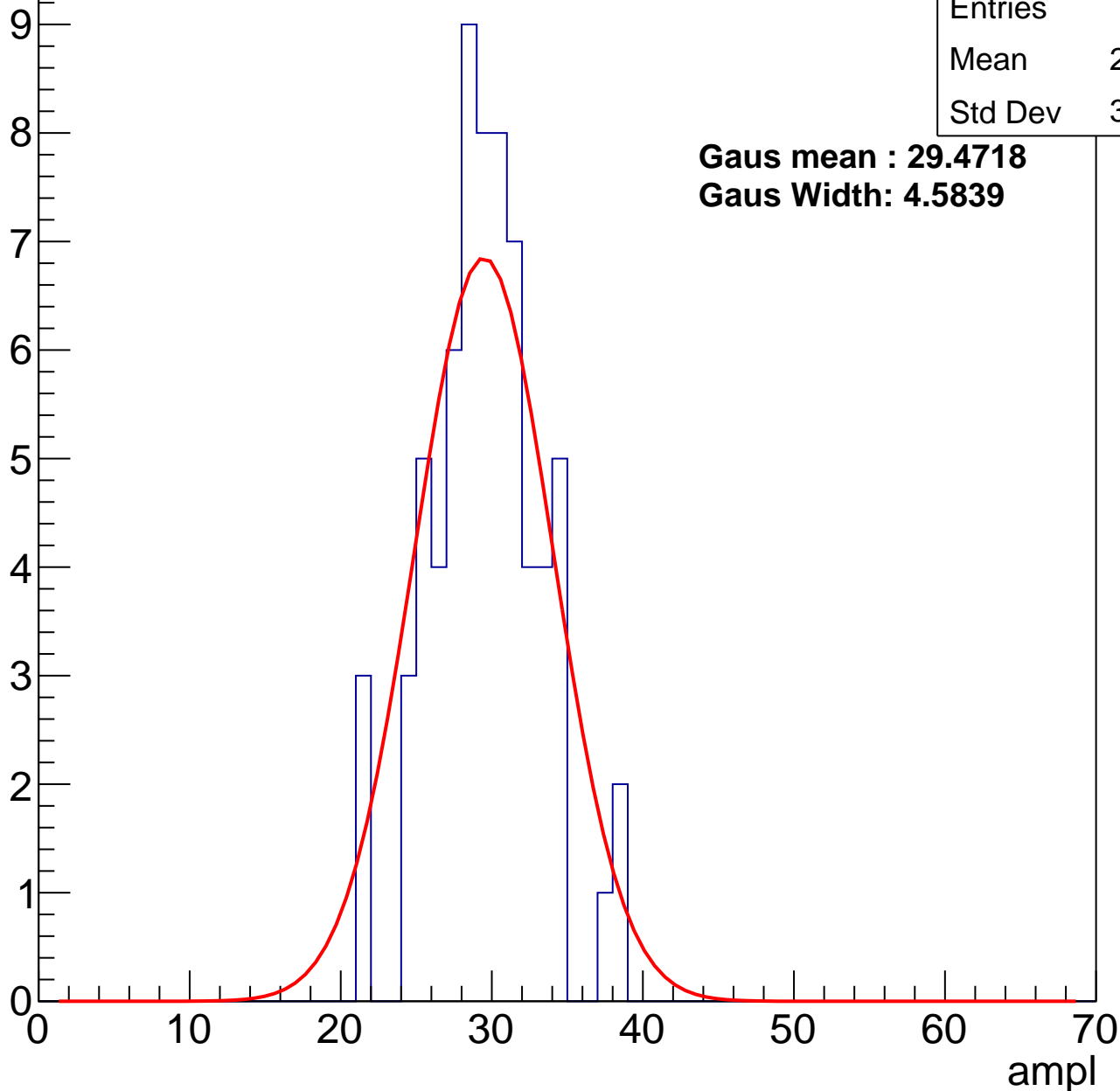
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	29.13
Std Dev	3.615

**Gaus mean : 29.4718**

**Gaus Width: 4.5839**



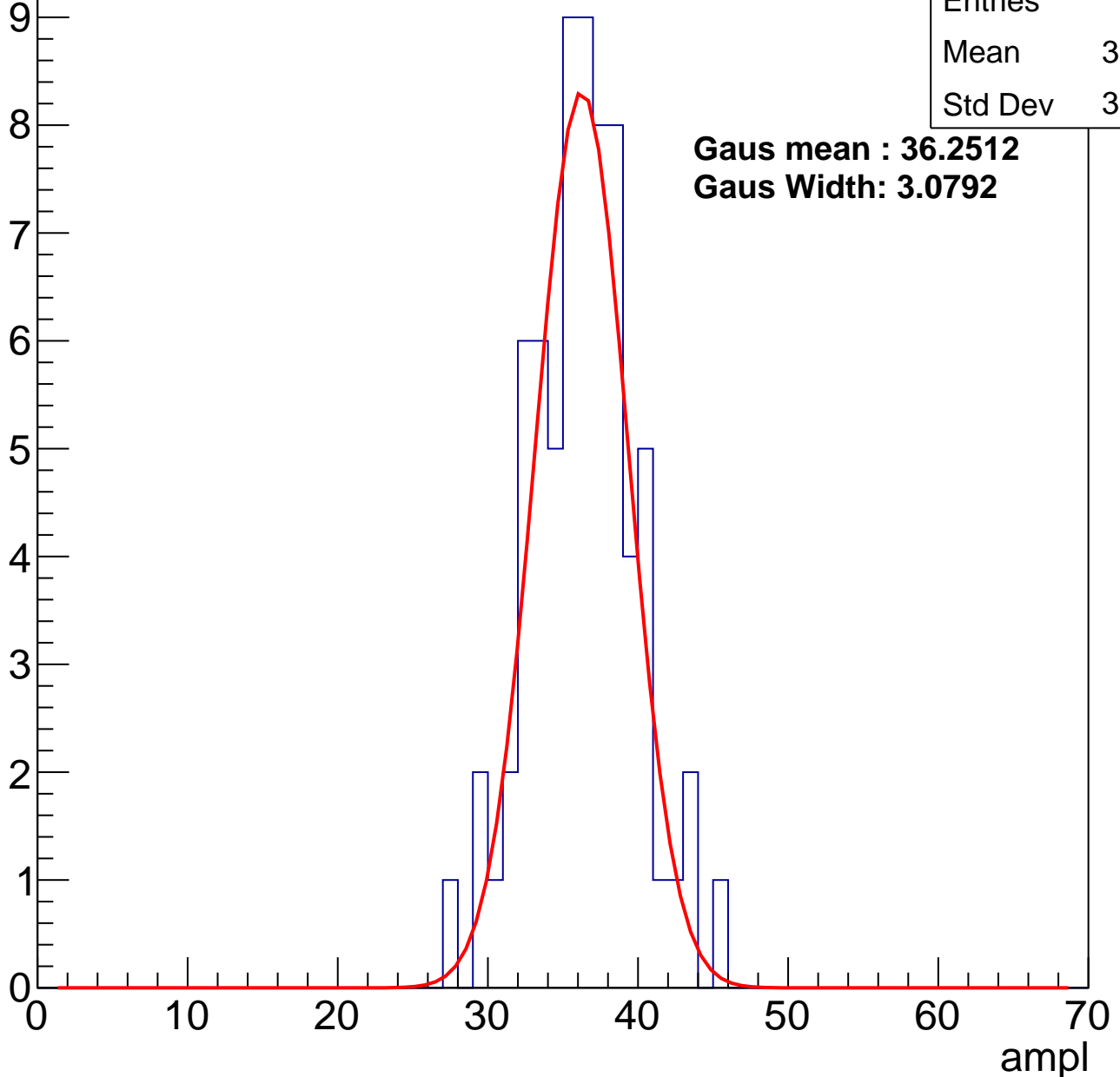
# B1L003S, U26-ch77, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	71
Mean	35.86
Std Dev	3.437

**Gaus mean : 36.2512**  
**Gaus Width: 3.0792**



# B1L003S, U26-ch77, adc2

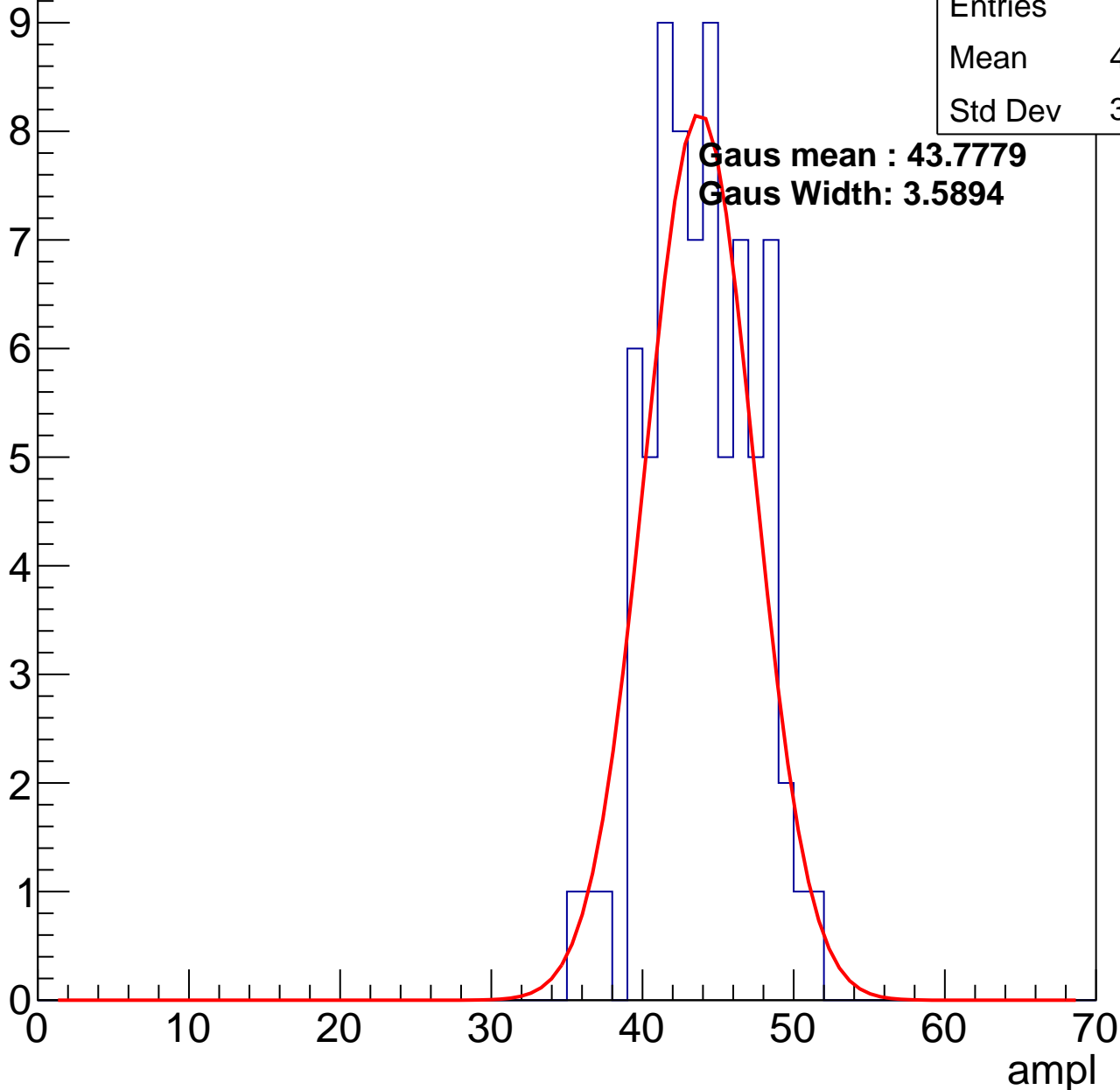
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	75
Mean	43.48
Std Dev	3.364

**Gaus mean : 43.7779**

**Gaus Width: 3.5894**

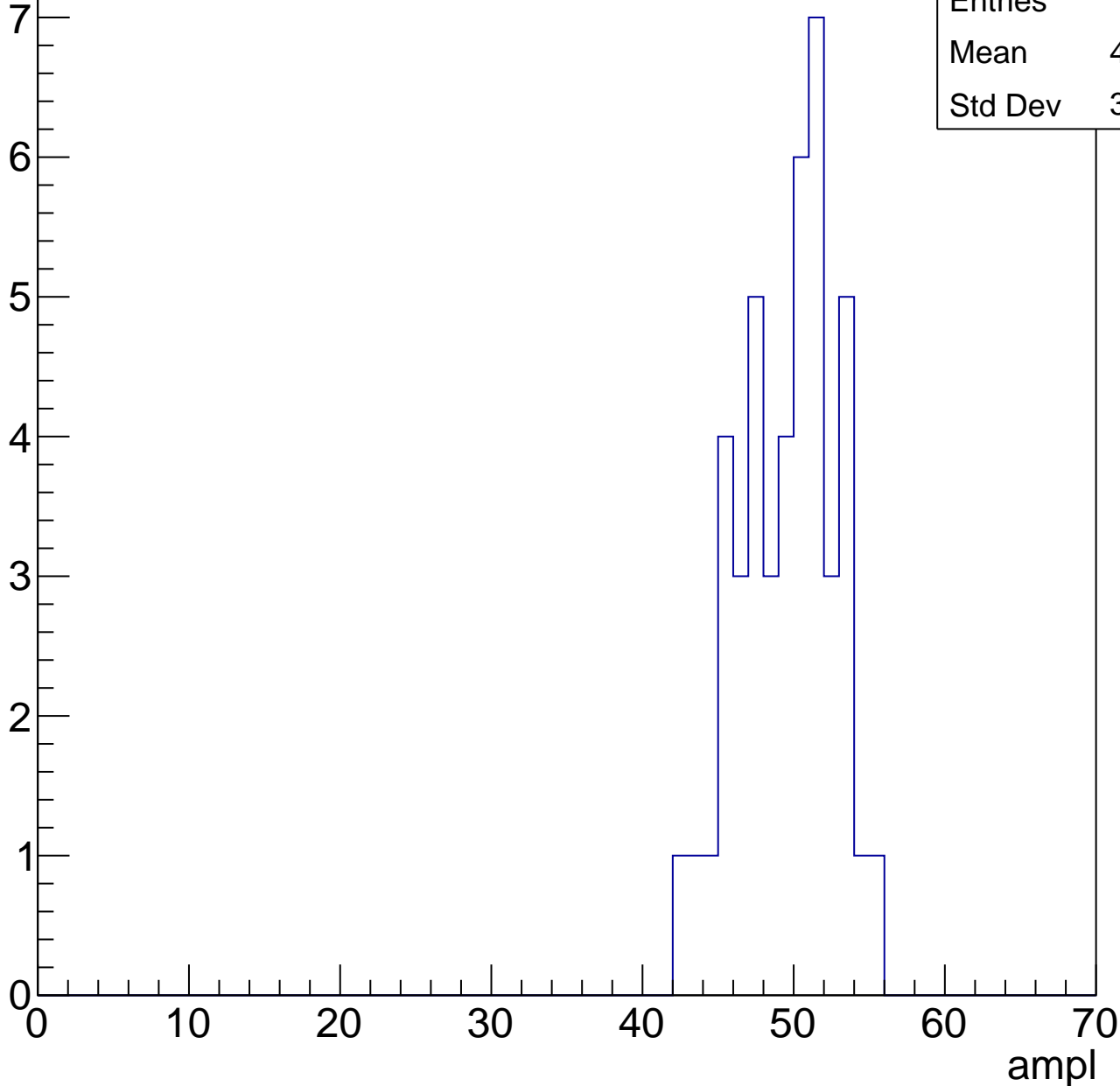


# B1L003S, U26-ch77, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	45
Mean	49.09
Std Dev	3.076

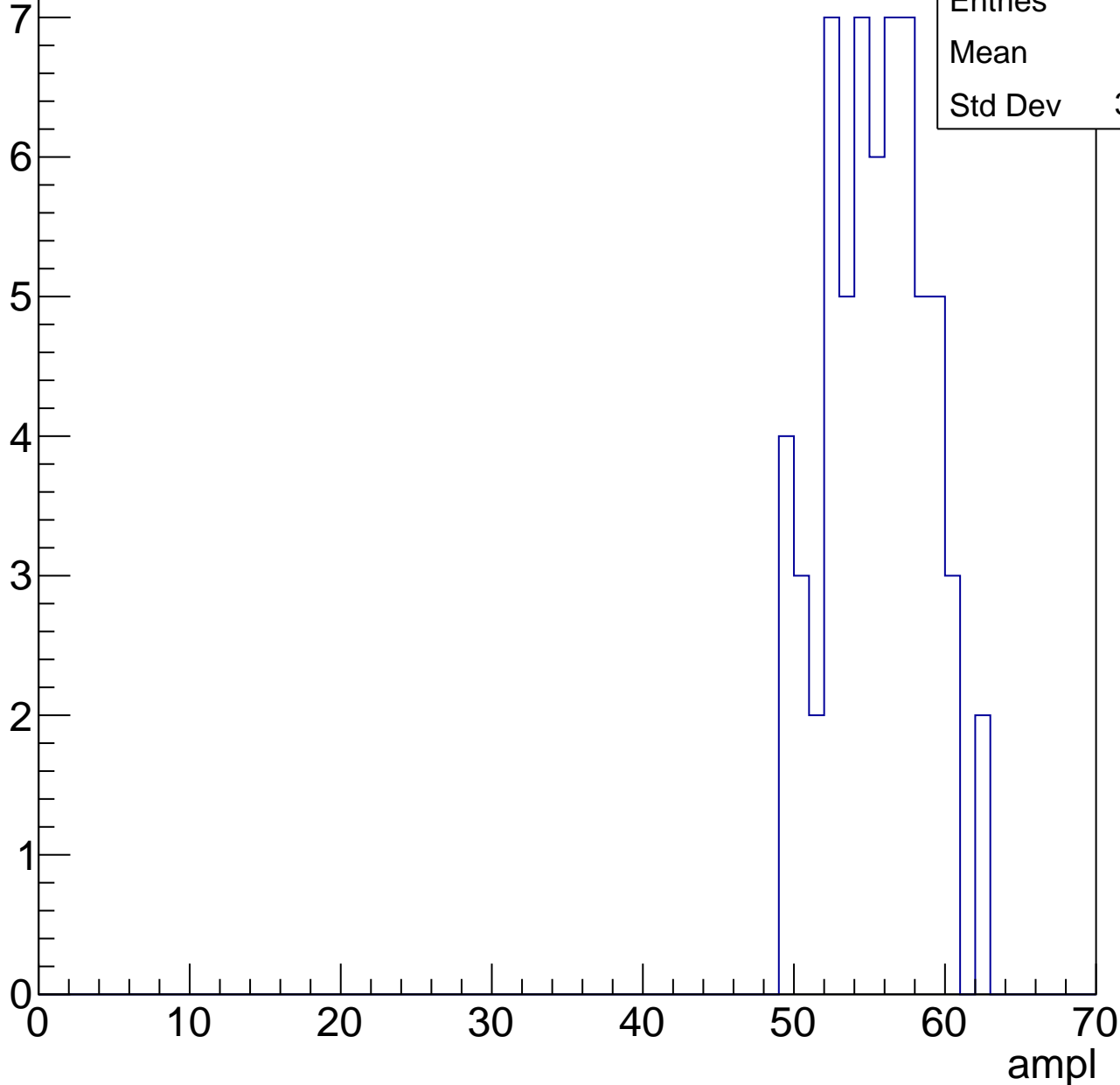


# B1L003S, U26-ch77, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	55
Std Dev	3.271

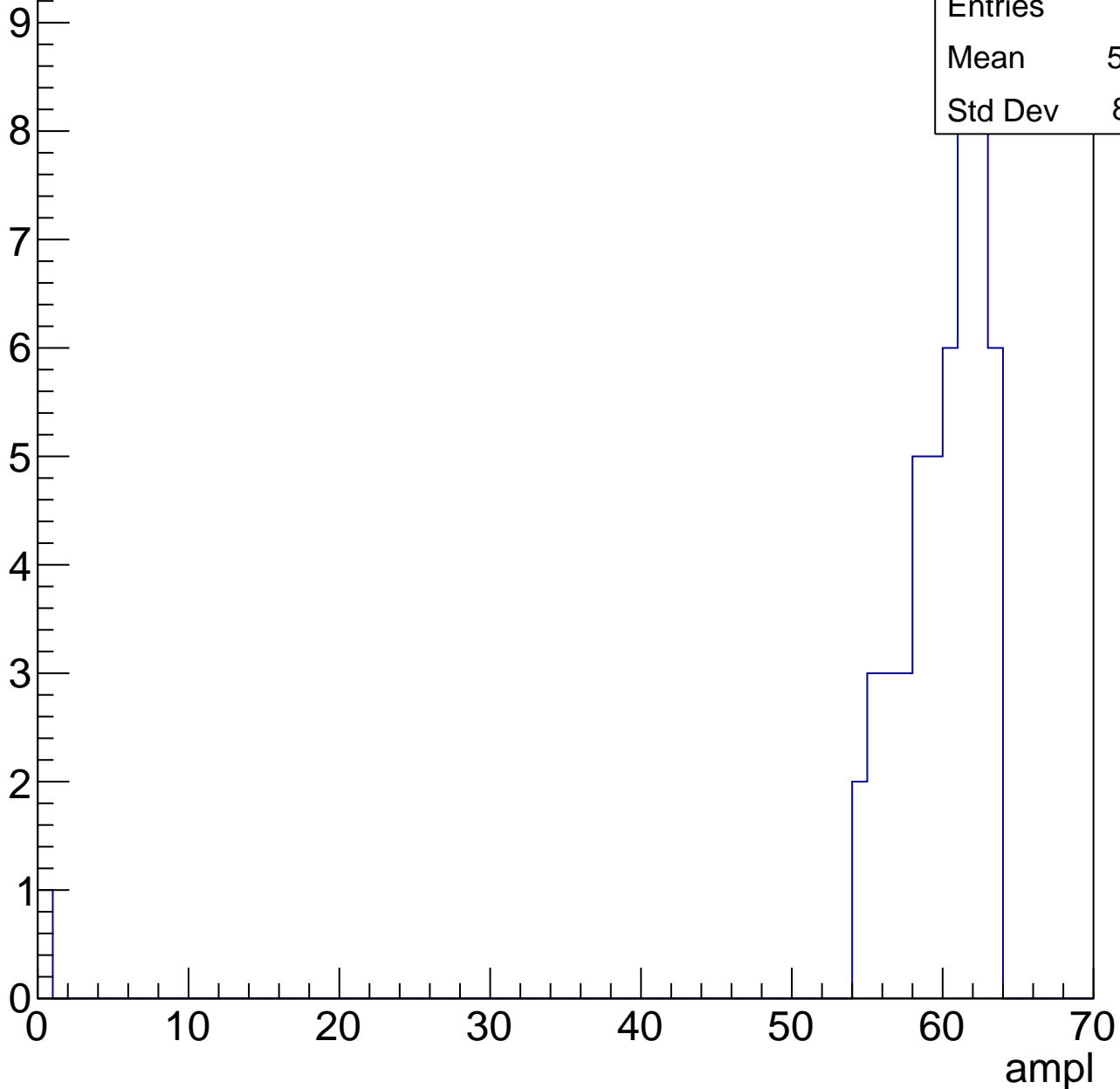


# B1L003S, U26-ch77, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

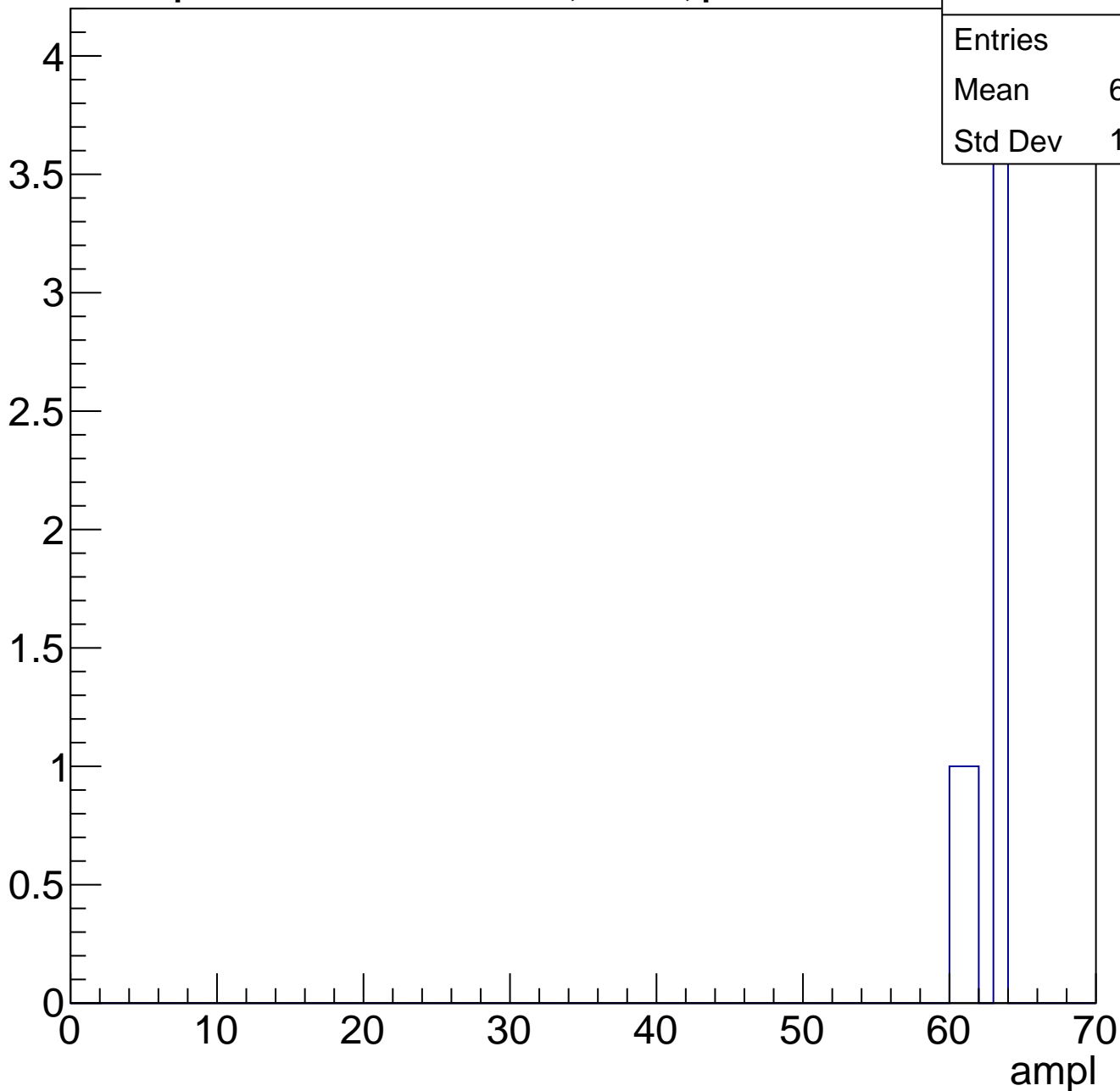
Entries	51
Mean	58.43
Std Dev	8.651



# B1L003S, U26-ch77, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch77, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U26-ch78, adc0

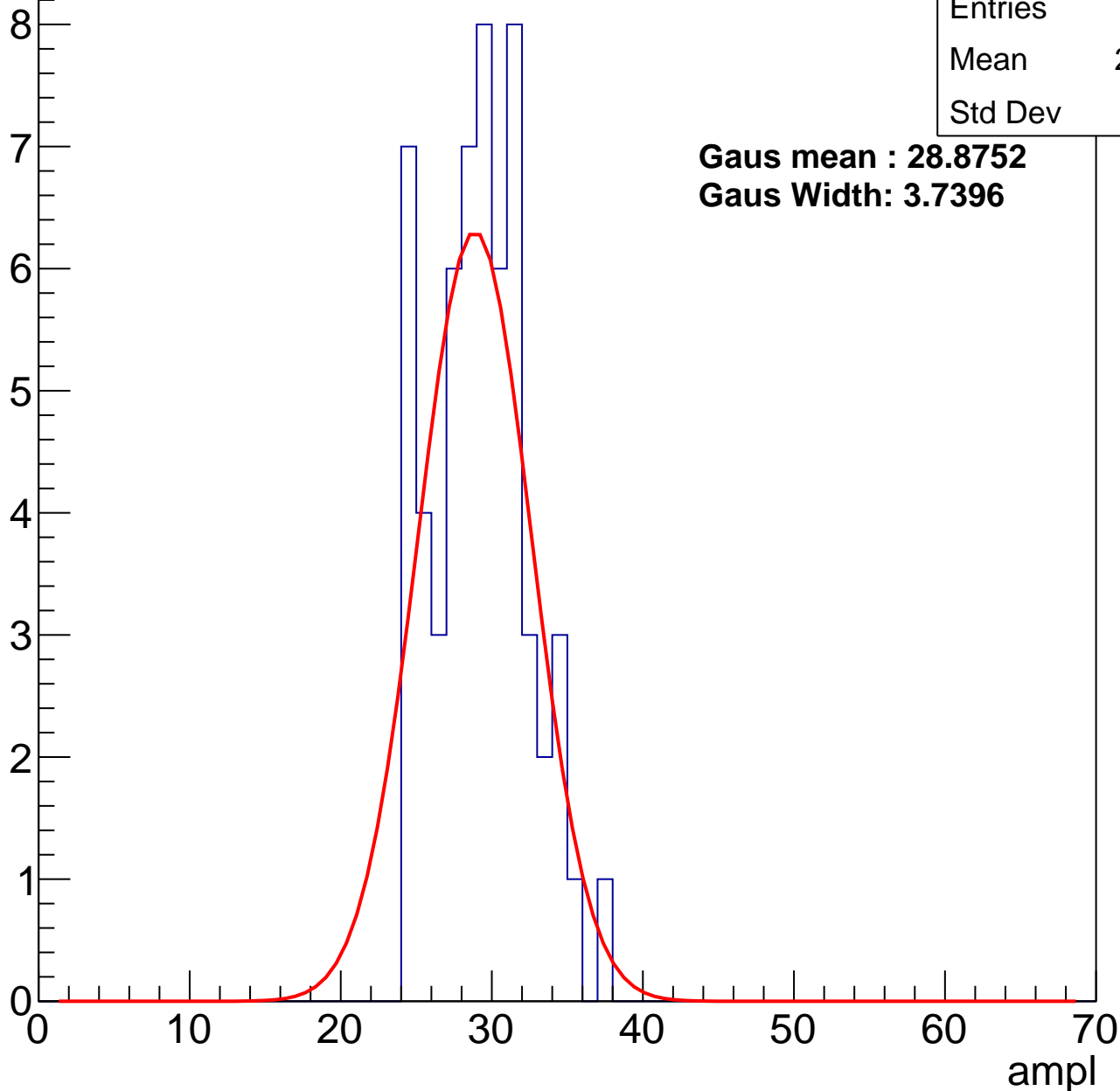
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	28.81
Std Dev	3.1

**Gaus mean : 28.8752**

**Gaus Width: 3.7396**



# B1L003S, U26-ch78, adc1

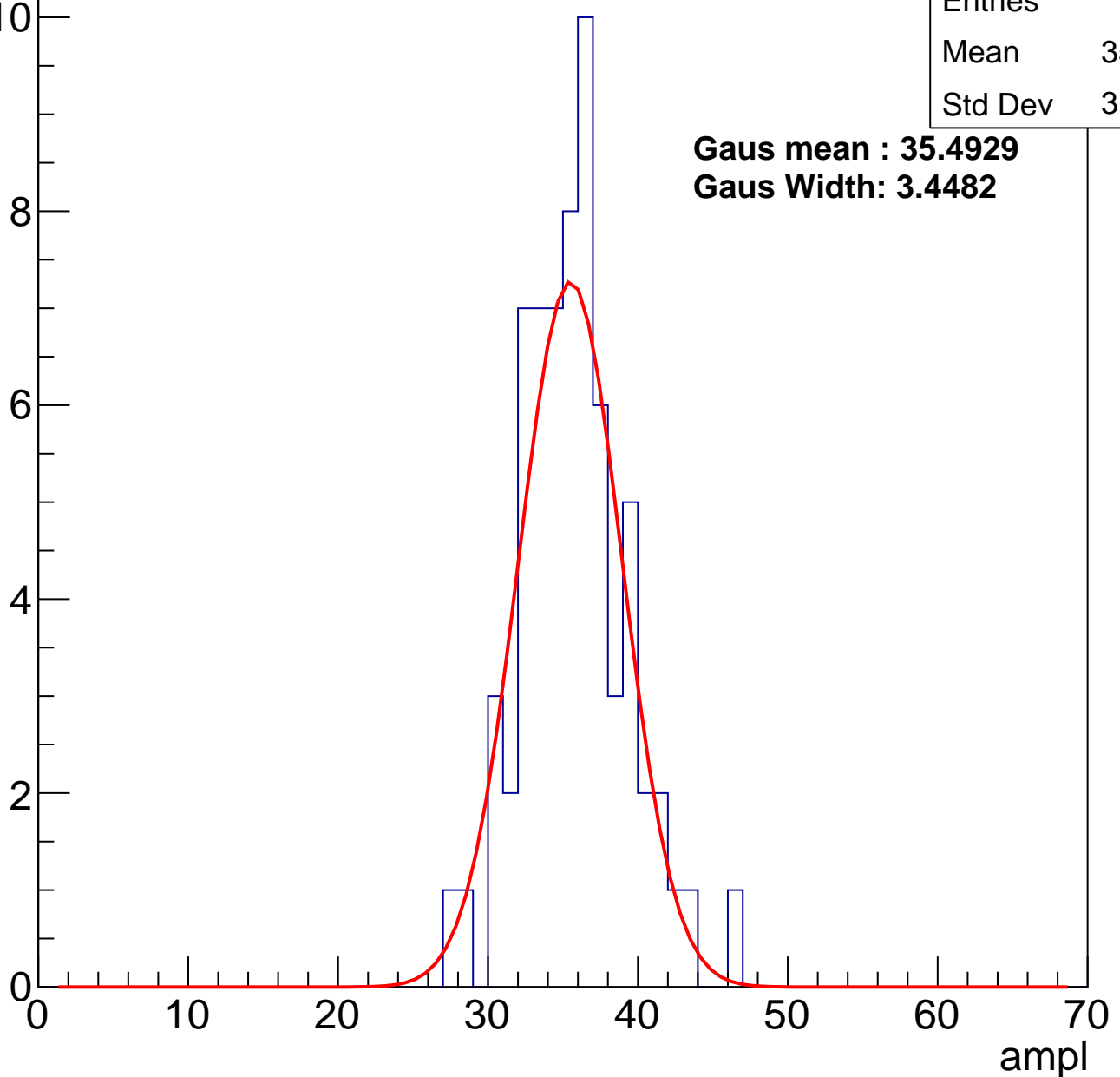
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	35.28
Std Dev	3.476

**Gaus mean : 35.4929**

**Gaus Width: 3.4482**



# B1L003S, U26-ch78, adc2

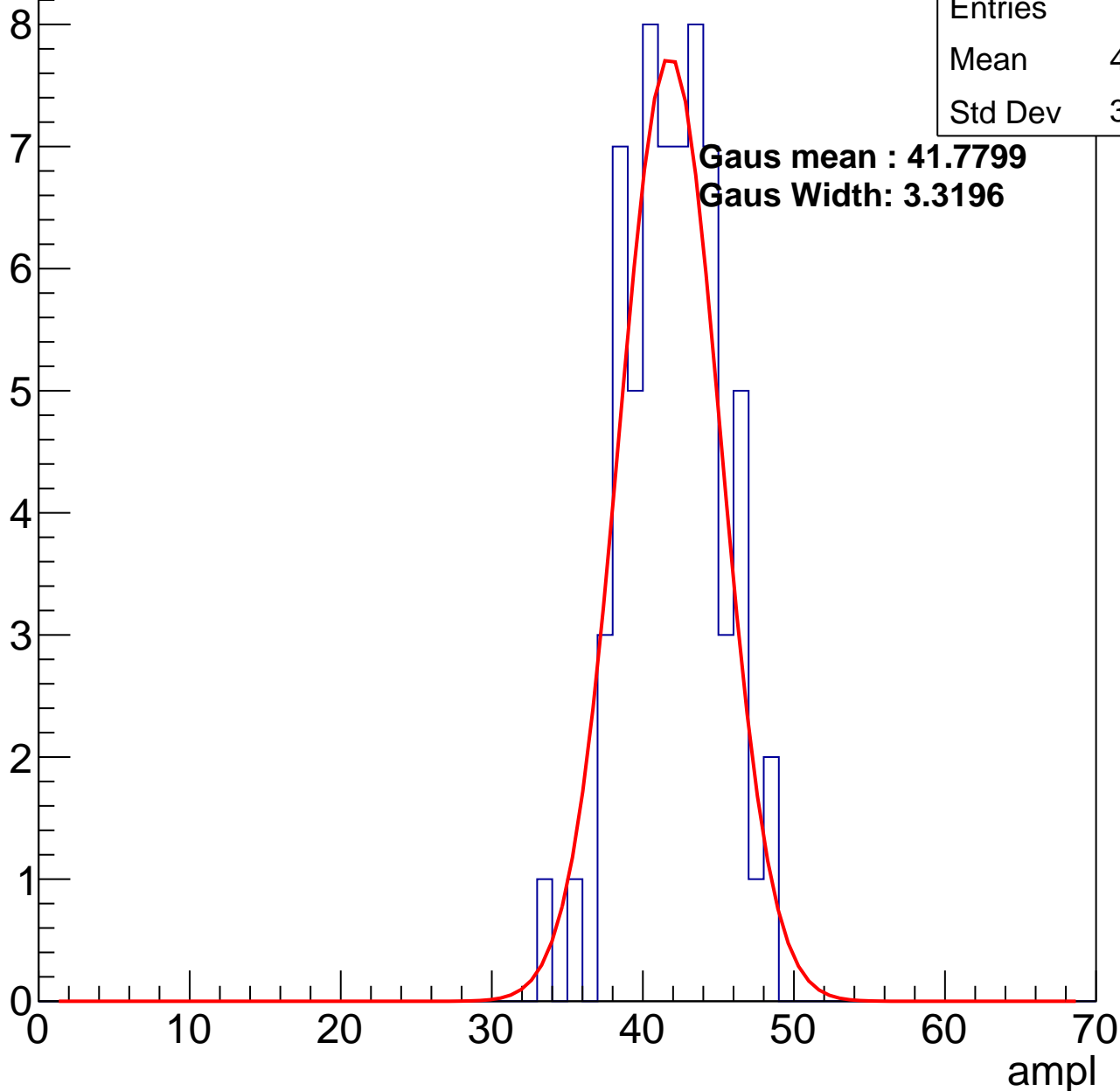
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	41.55
Std Dev	3.108

**Gaus mean : 41.7799**

**Gaus Width: 3.3196**

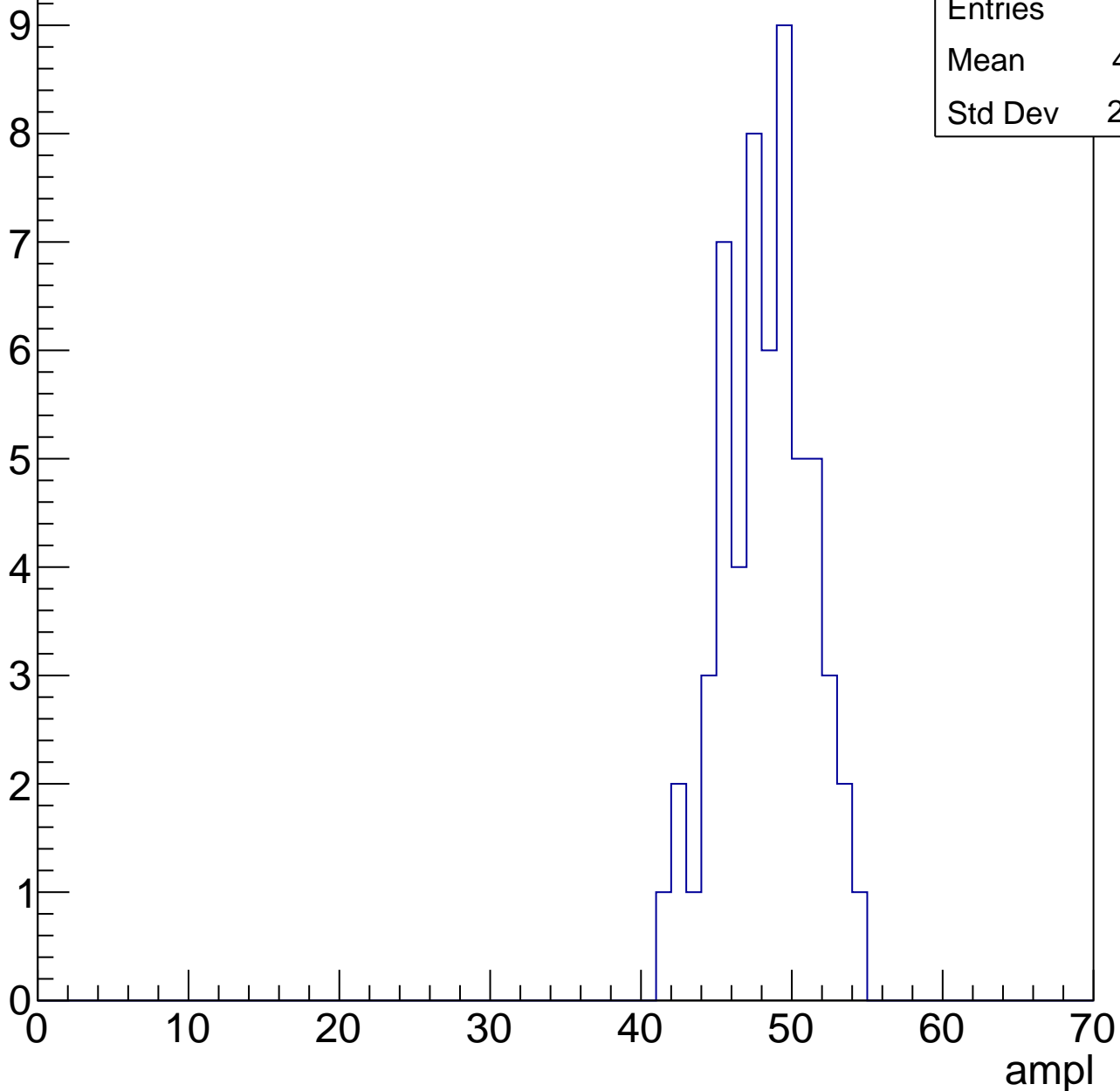


# B1L003S, U26-ch78, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	47.81
Std Dev	2.923

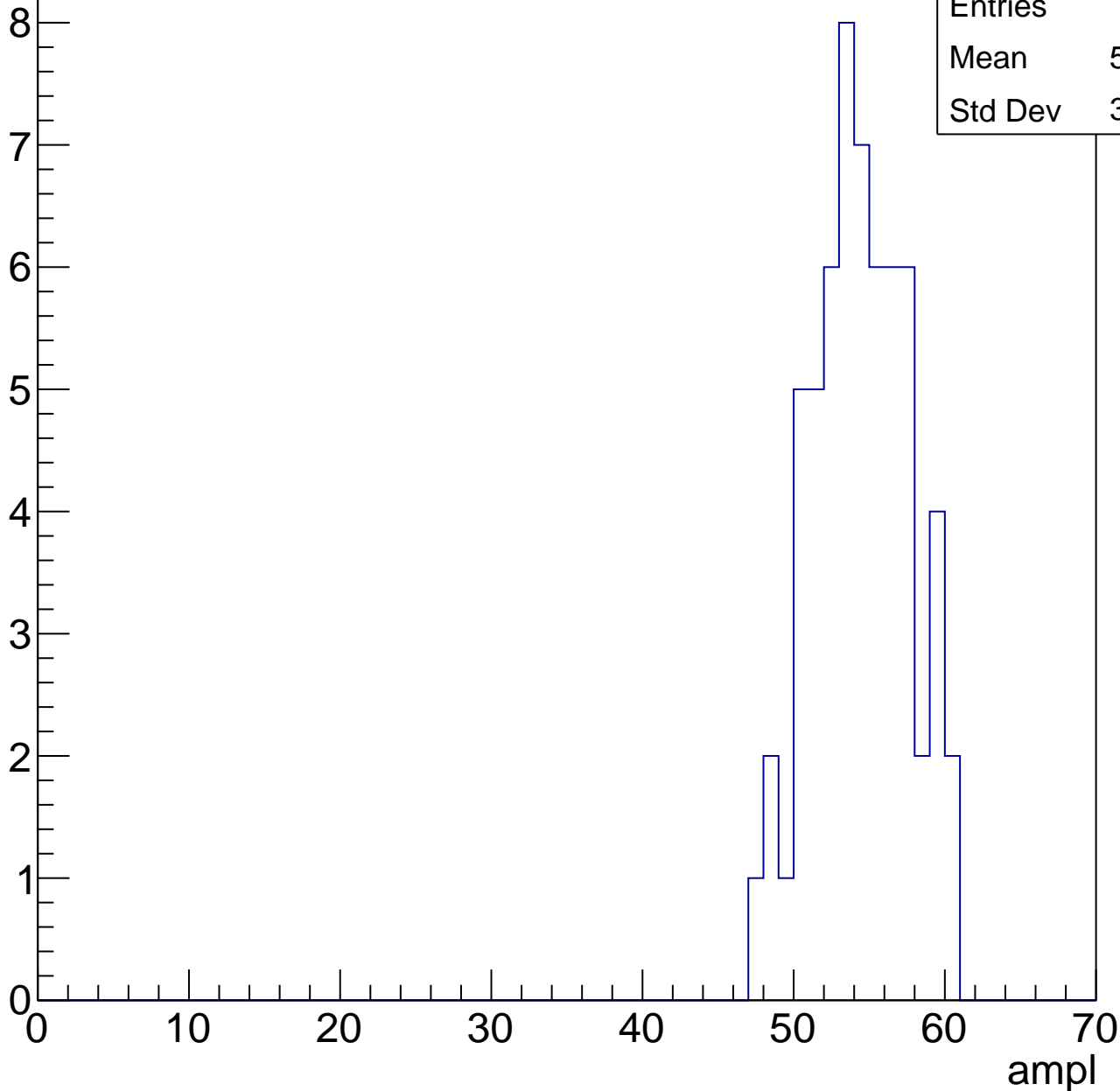


# B1L003S, U26-ch78, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	53.95
Std Dev	3.112

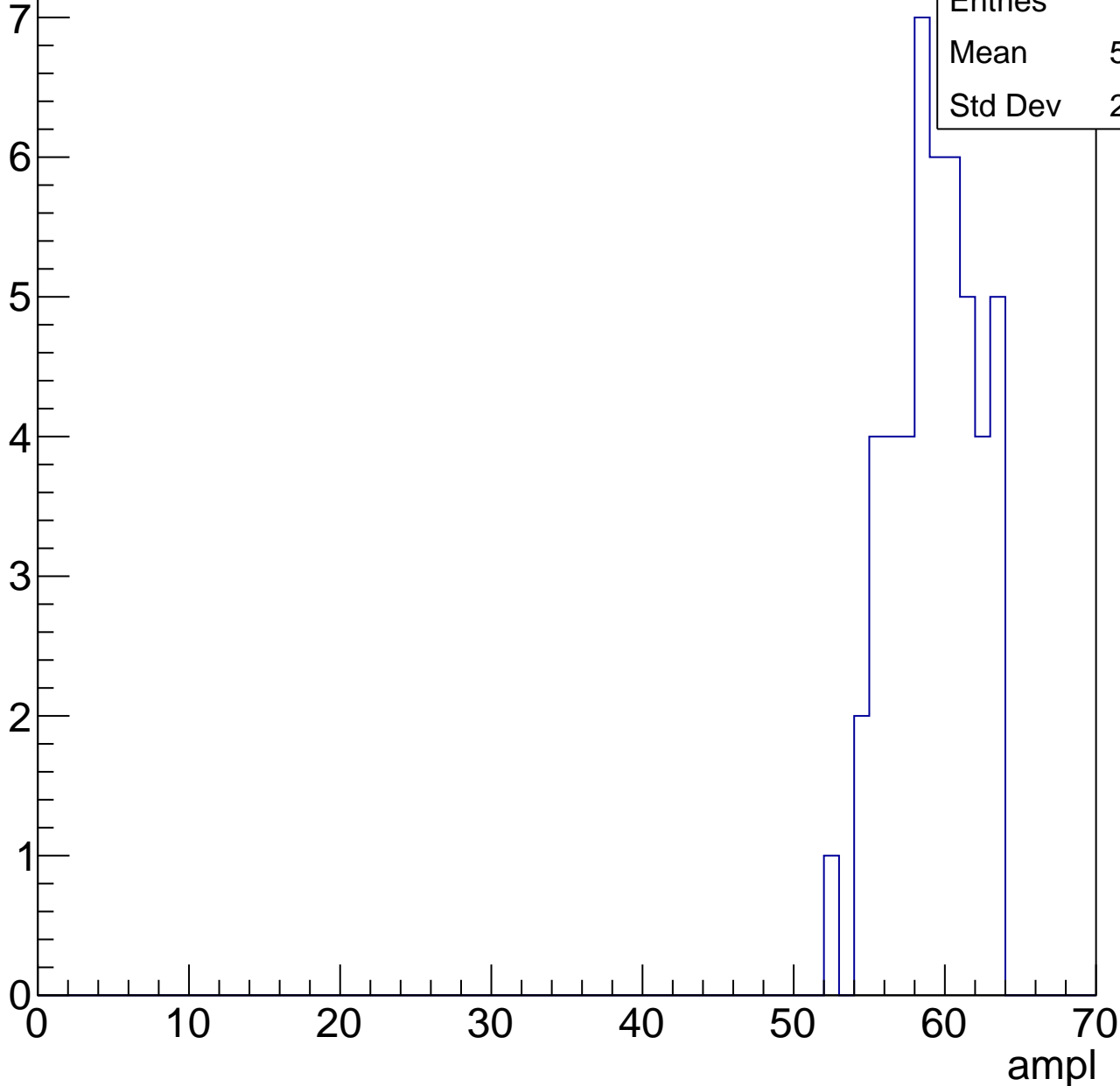


# B1L003S, U26-ch78, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	48
Mean	58.75
Std Dev	2.742

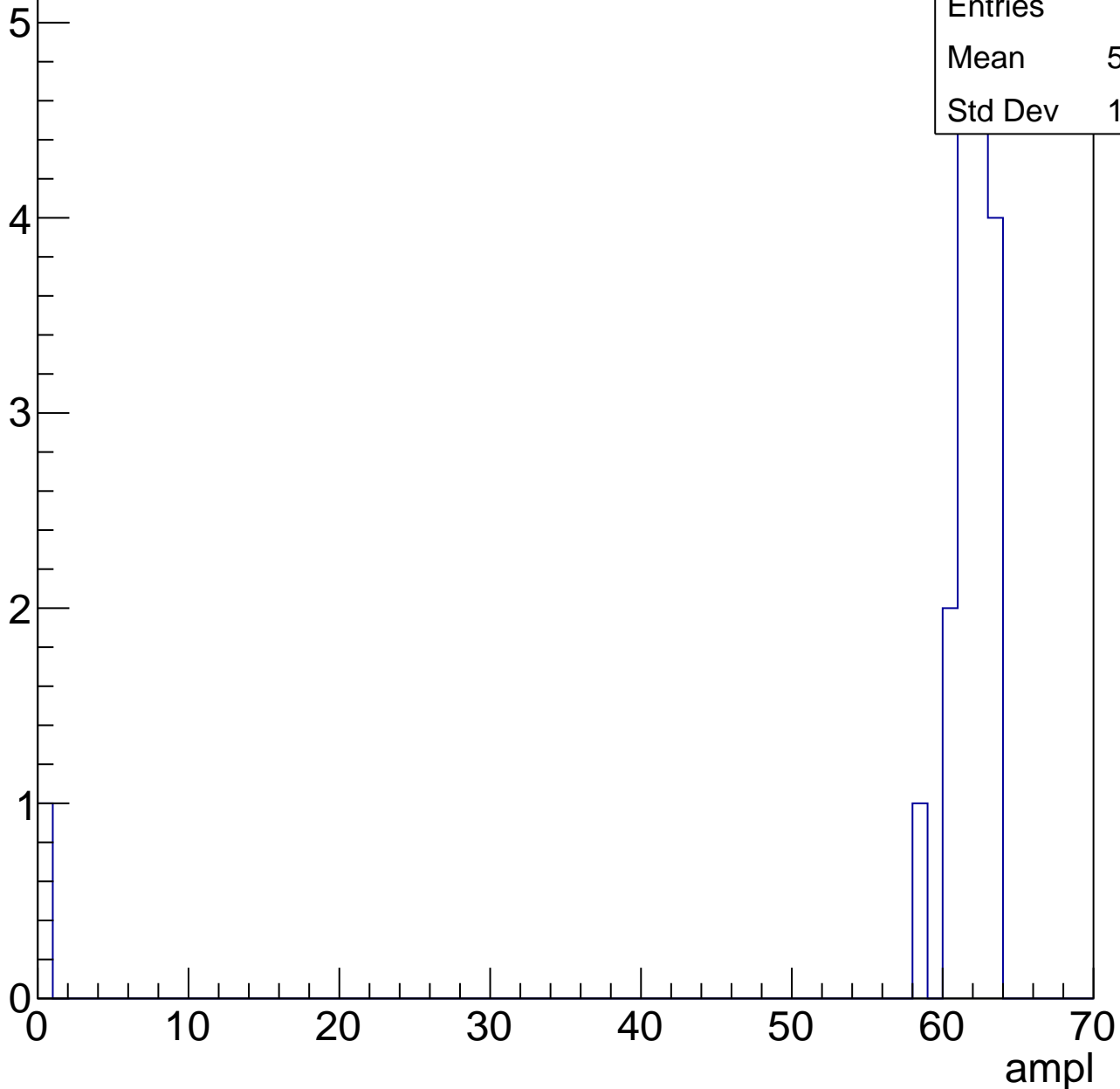


# B1L003S, U26-ch78, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	18
Mean	58.06
Std Dev	14.14

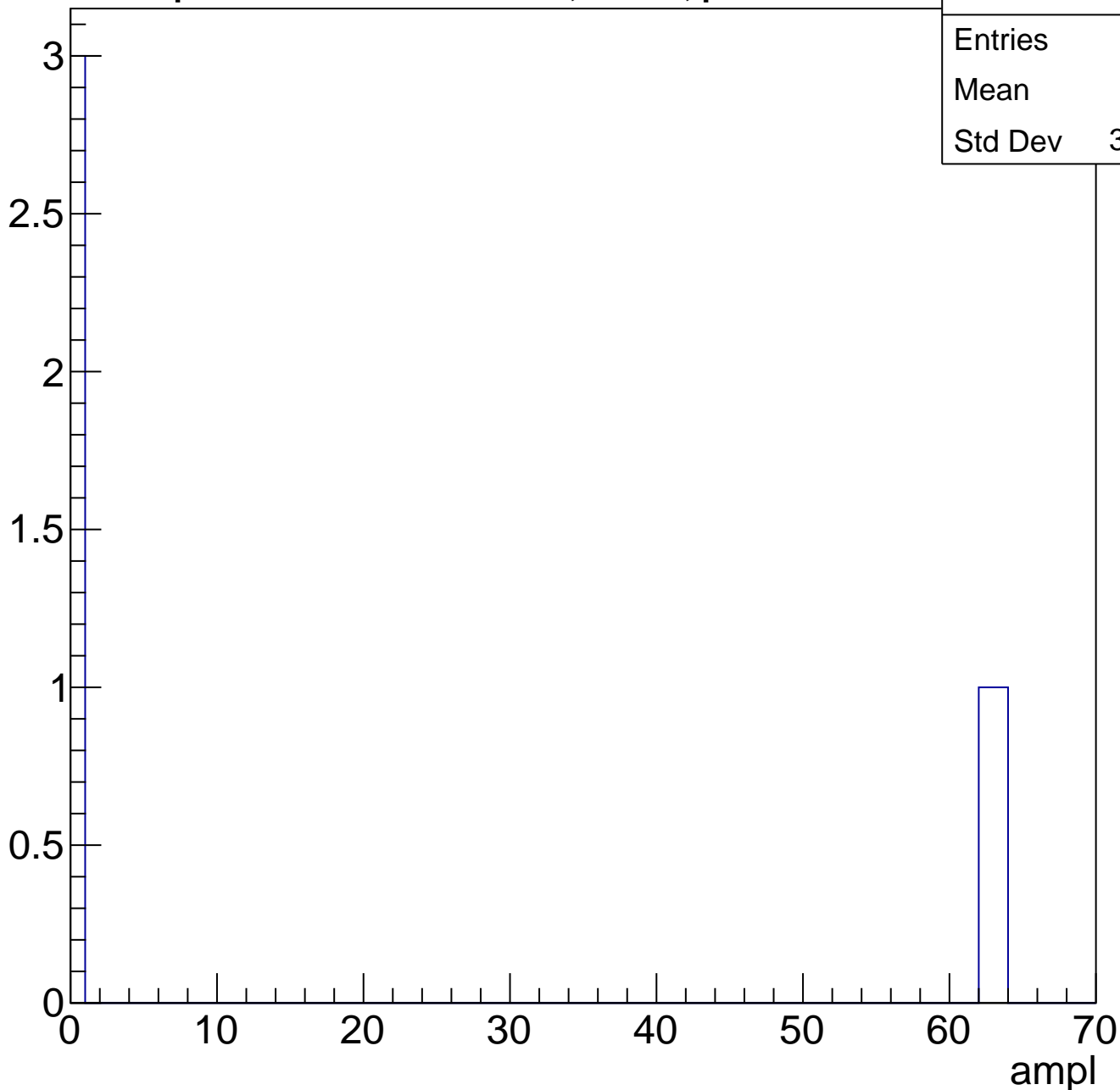




# B1L003S, U26-ch78, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	5
Mean	25
Std Dev	30.62

# B1L003S, U26-ch79, adc0

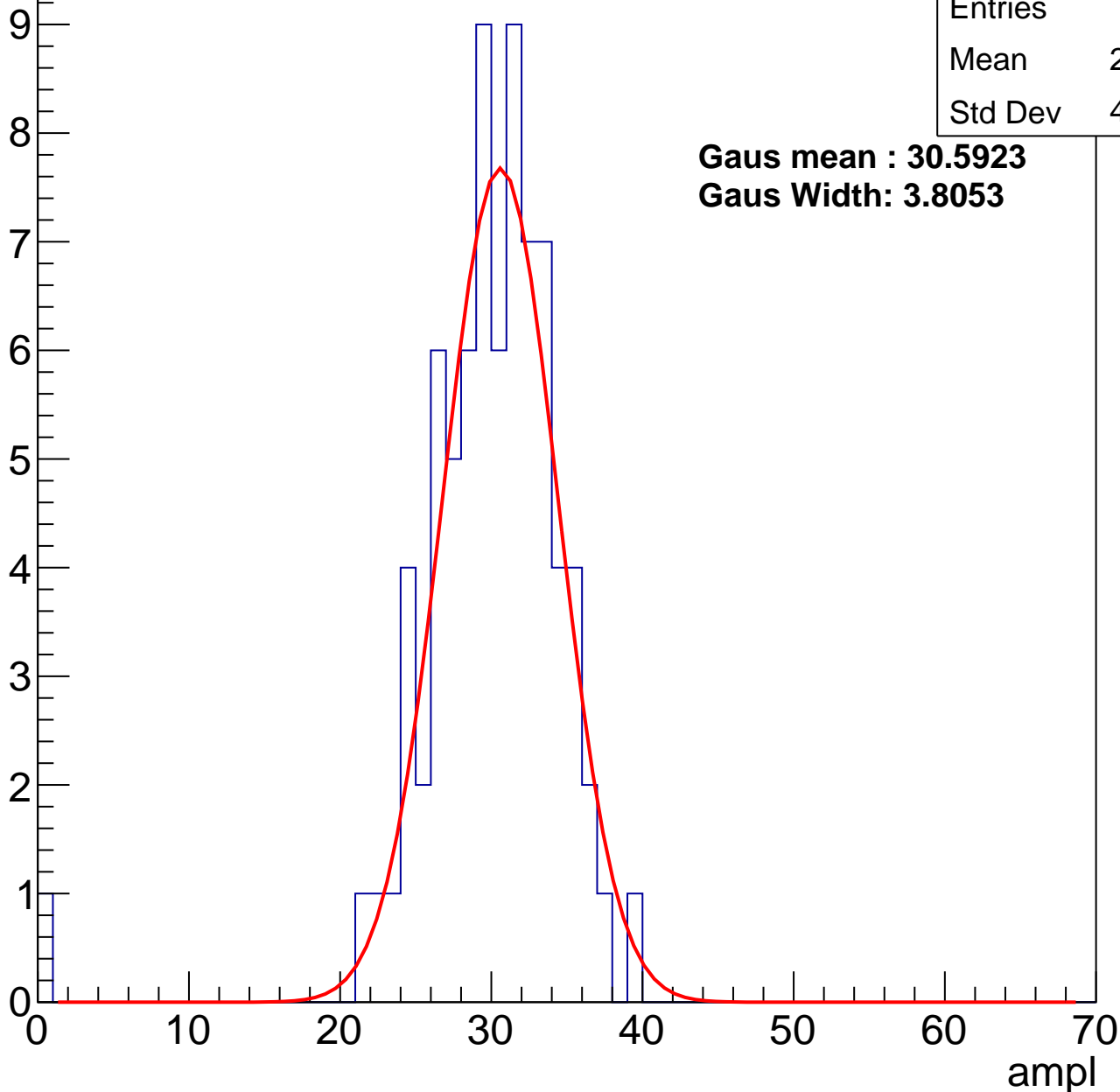
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	77
Mean	29.48
Std Dev	4.977

**Gaus mean : 30.5923**

**Gaus Width: 3.8053**



# B1L003S, U26-ch79, adc1

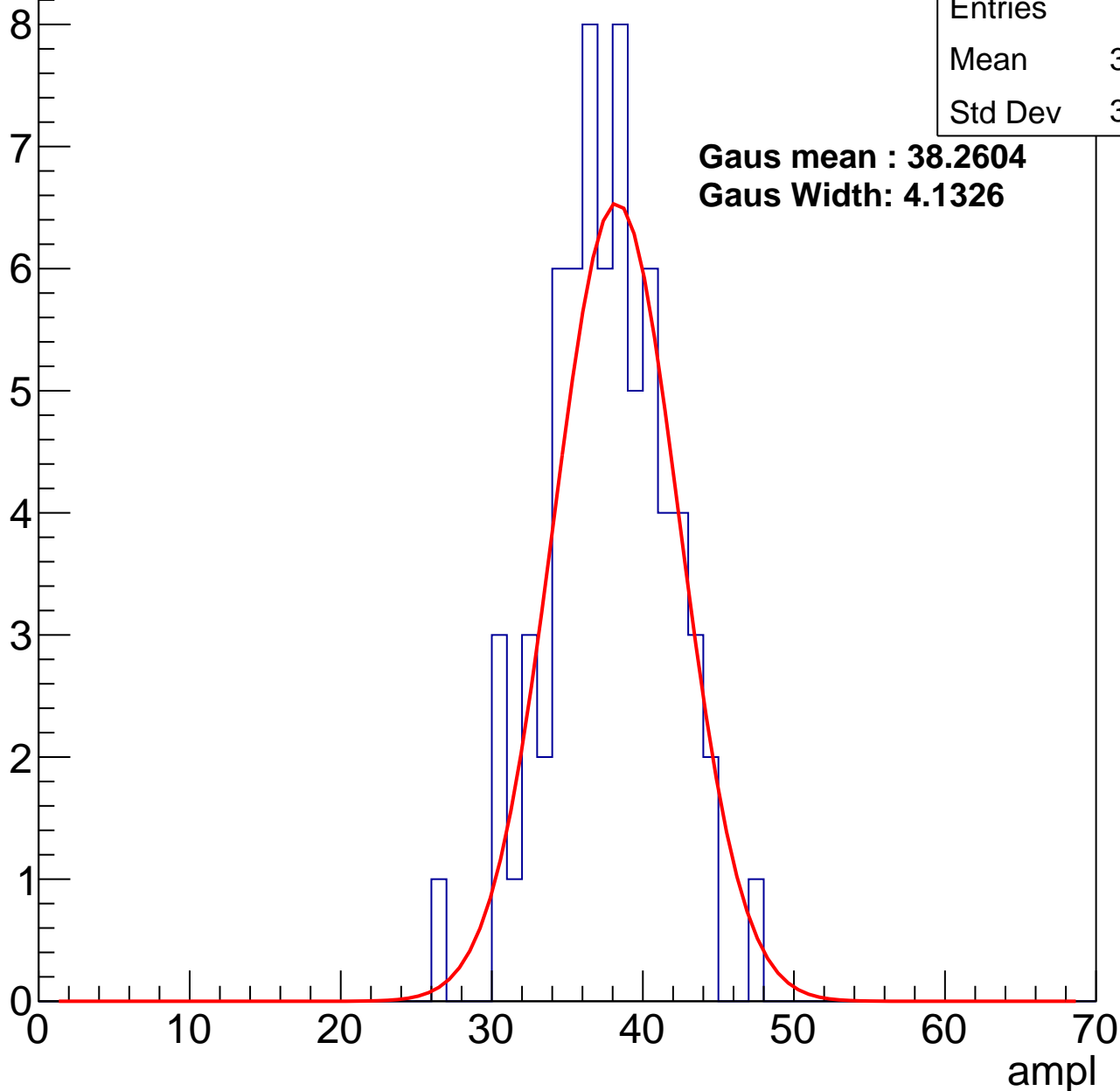
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	37.22
Std Dev	3.893

**Gaus mean : 38.2604**

**Gaus Width: 4.1326**



# B1L003S, U26-ch79, adc2

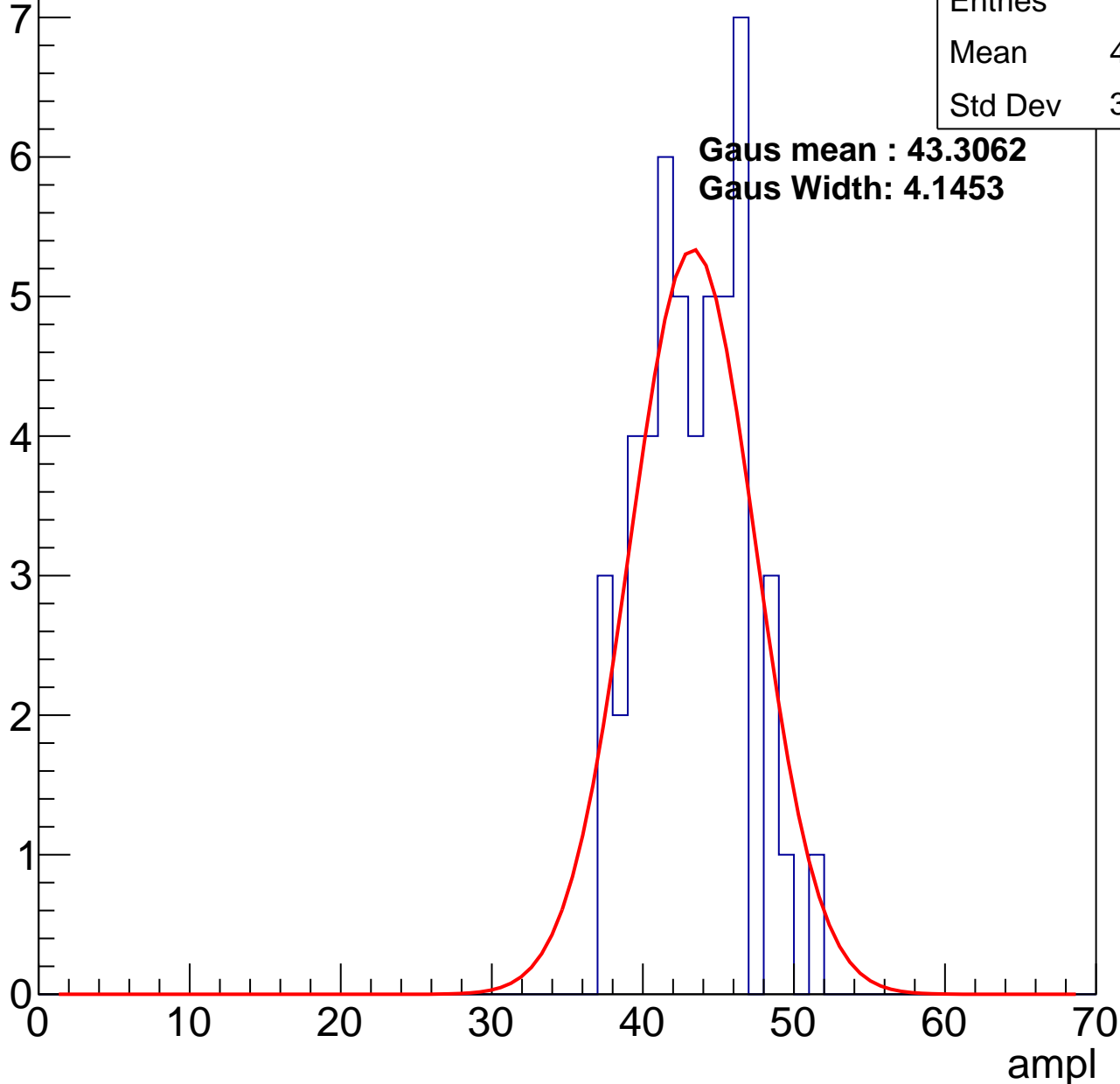
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	50
Mean	42.84
Std Dev	3.313

**Gaus mean : 43.3062**

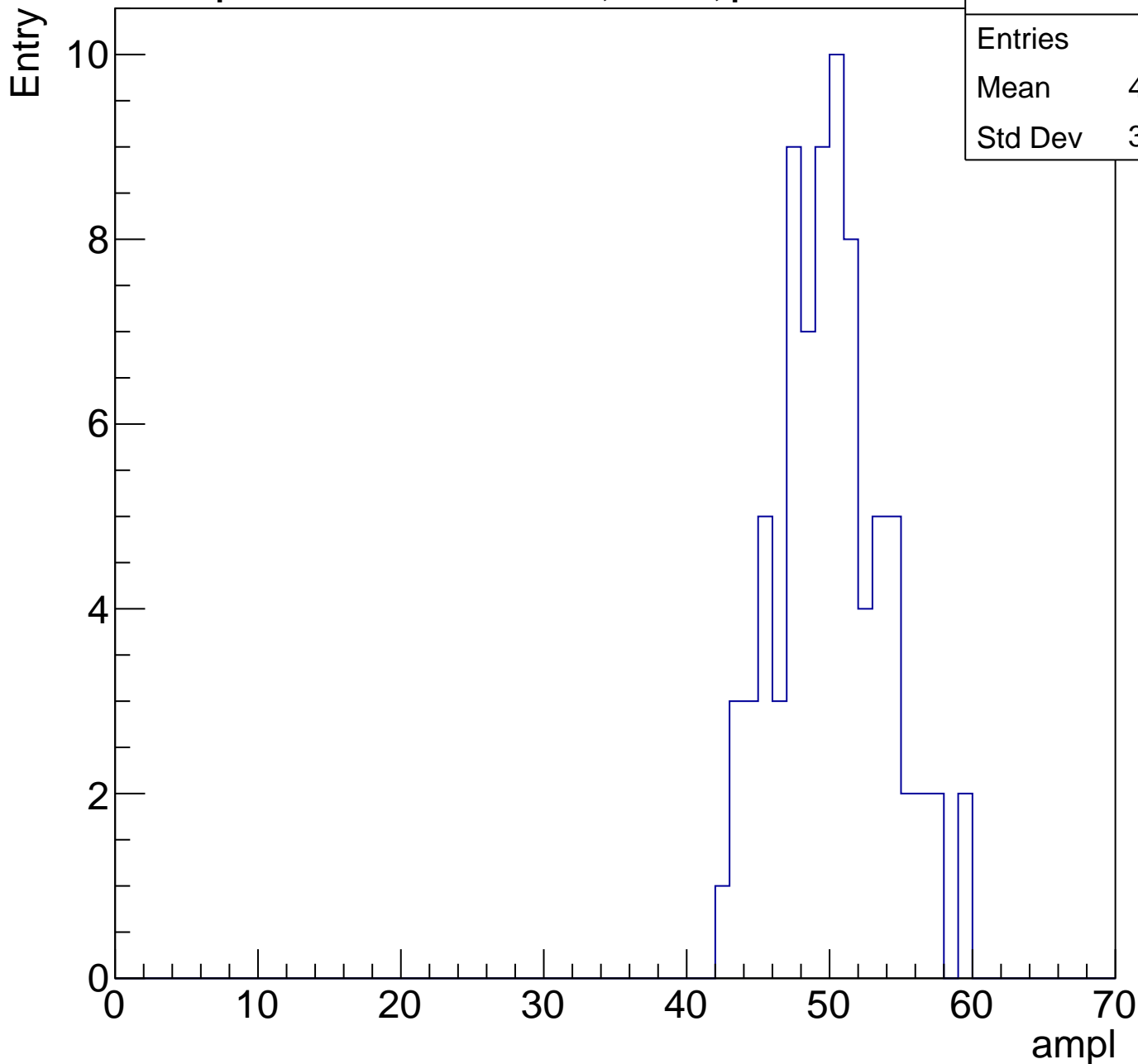
**Gaus Width: 4.1453**



# B1L003S, U26-ch79, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	80
Mean	49.64
Std Dev	3.759

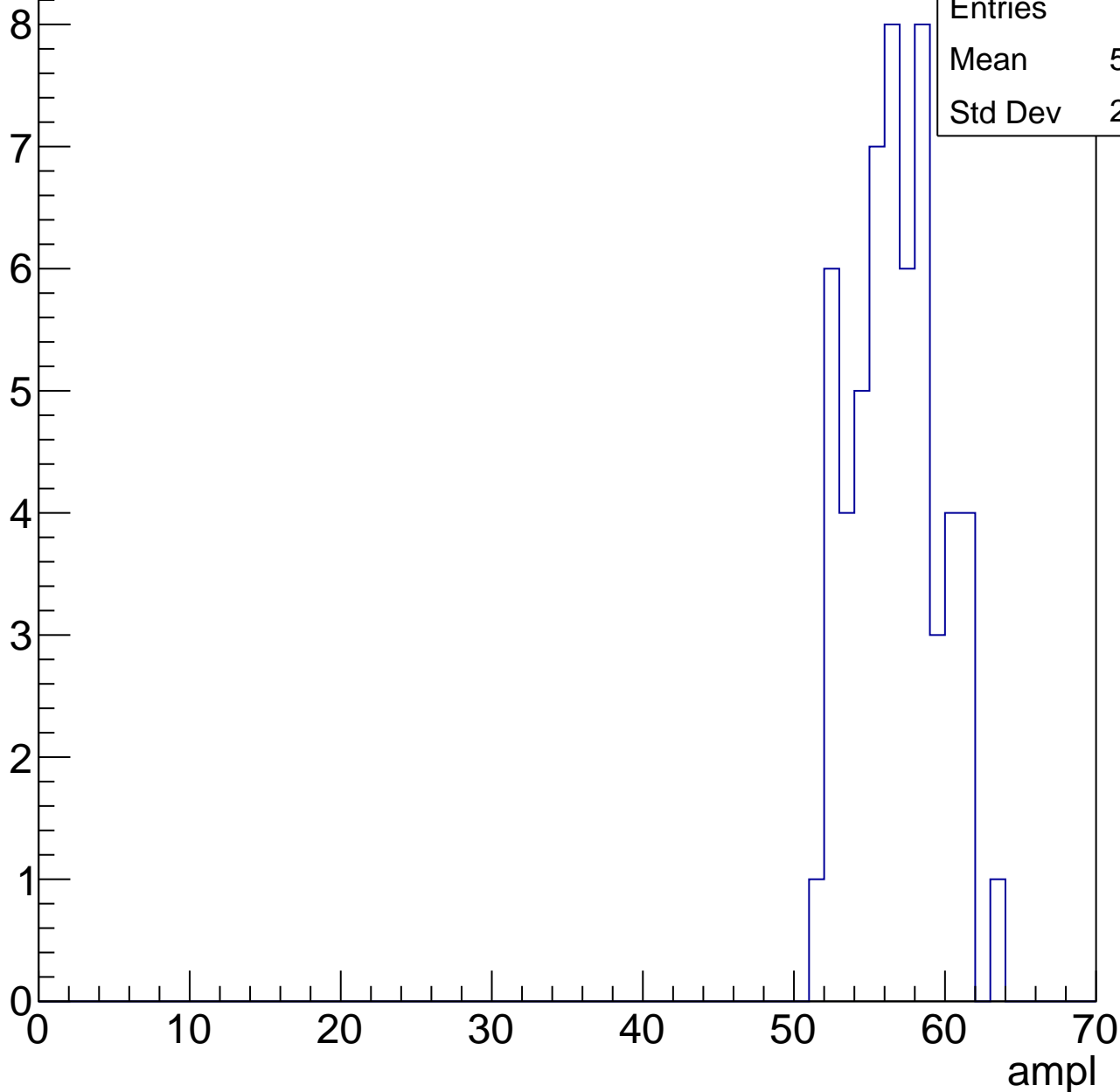


# B1L003S, U26-ch79, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	56.28
Std Dev	2.833

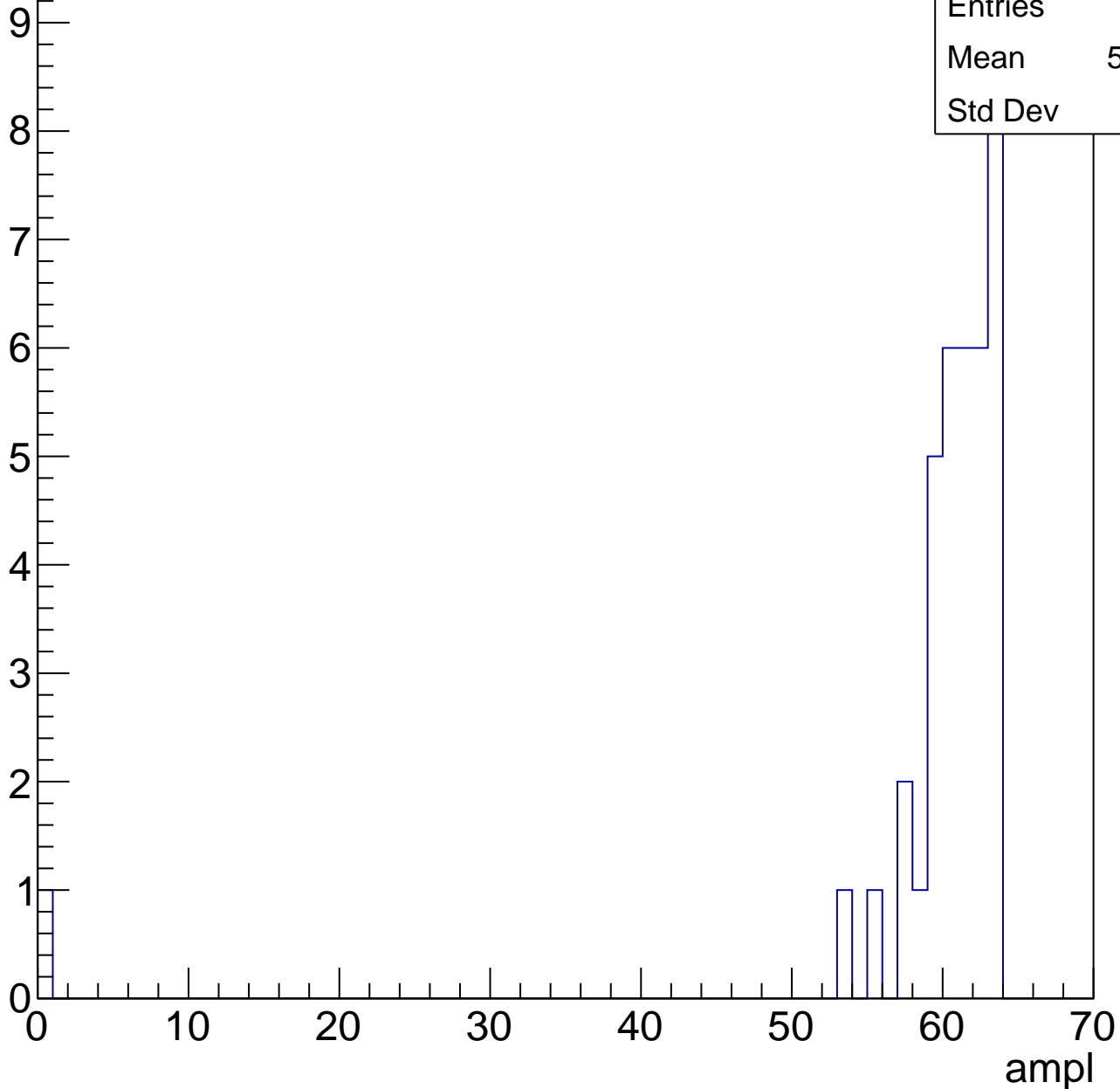


# B1L003S, U26-ch79, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

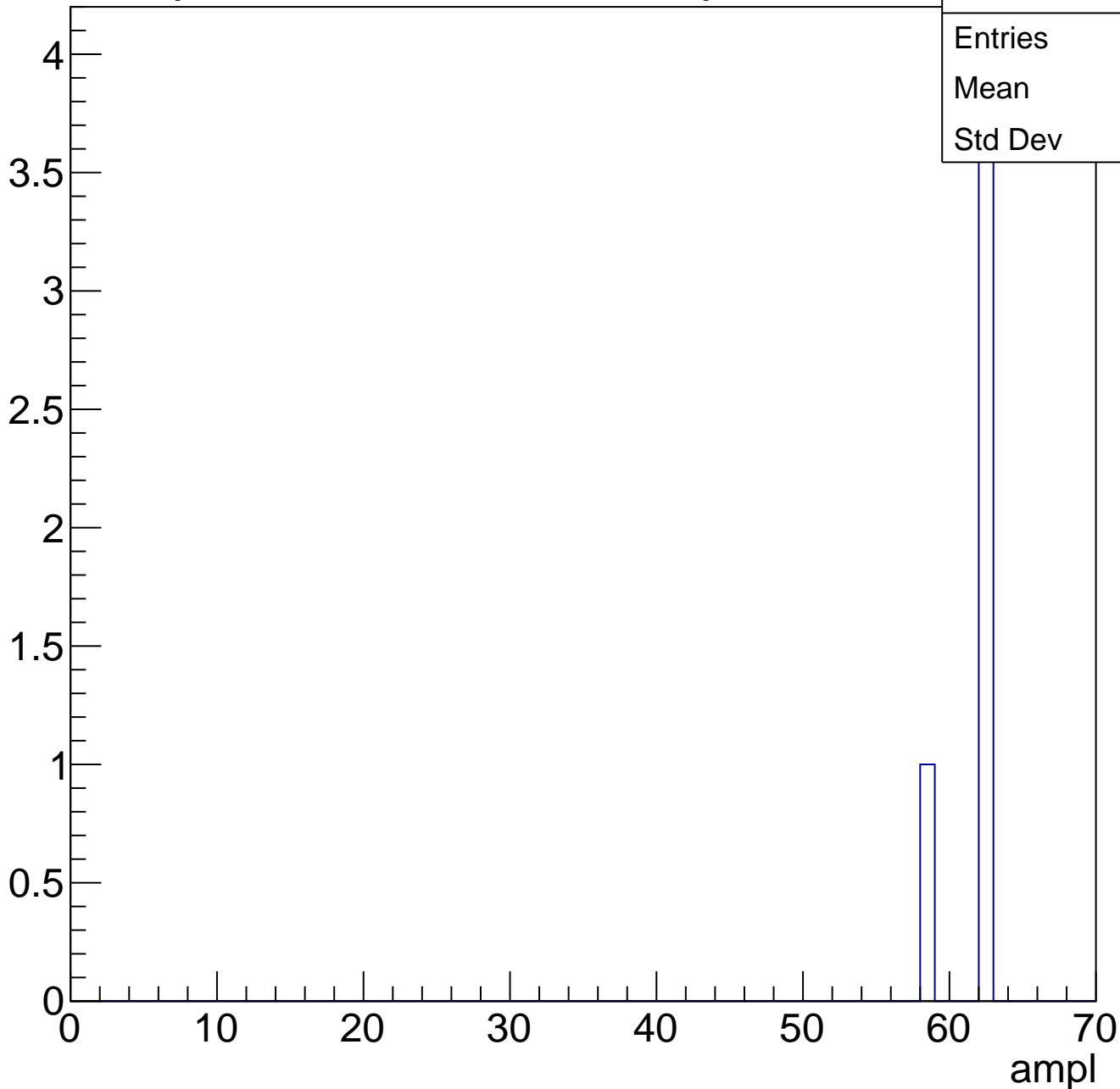
Entries	38
Mean	58.95
Std Dev	9.96



# B1L003S, U26-ch79, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch79, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U26-ch80, adc0

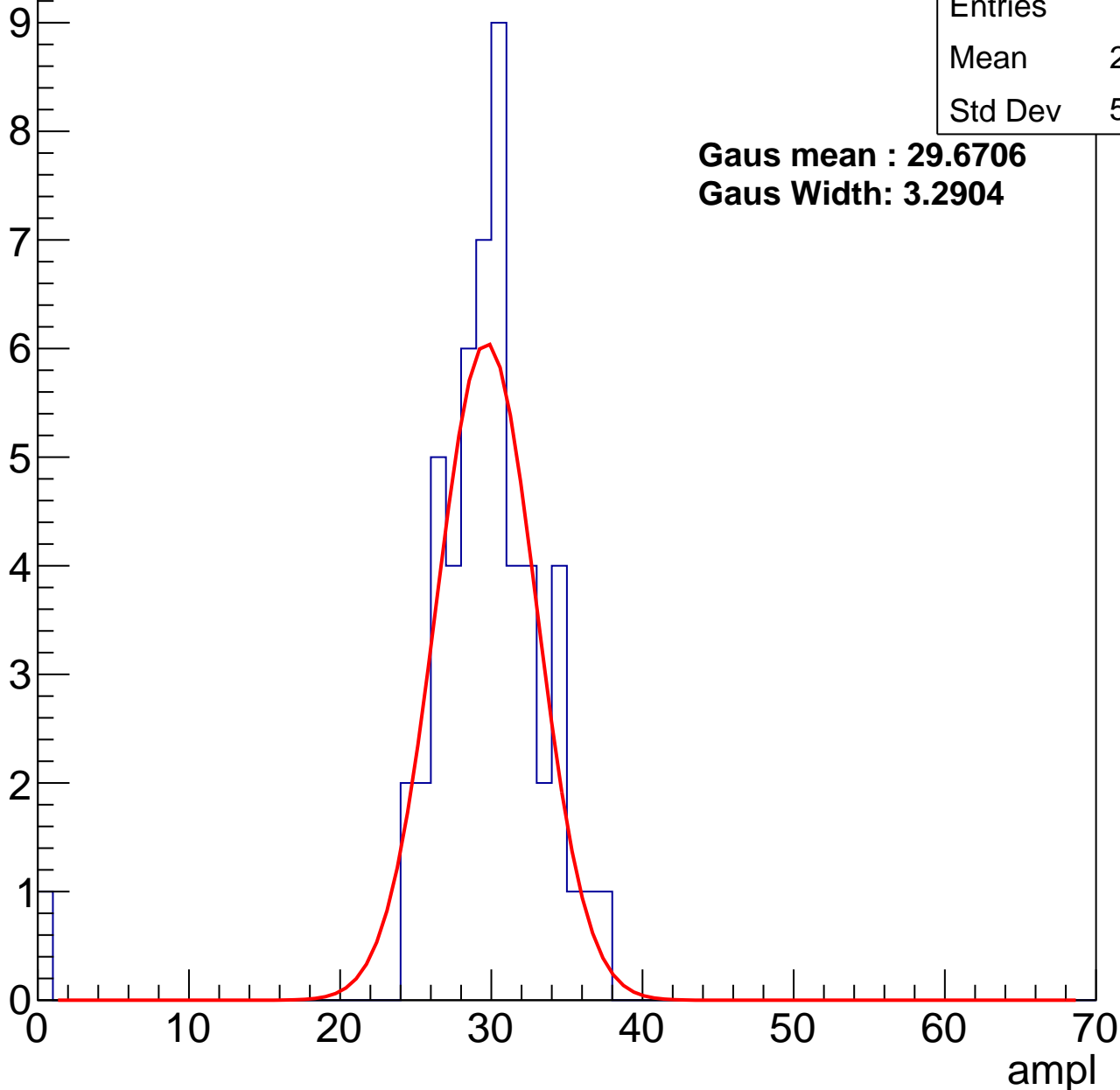
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	29.04
Std Dev	5.013

**Gaus mean : 29.6706**

**Gaus Width: 3.2904**



# B1L003S, U26-ch80, adc1

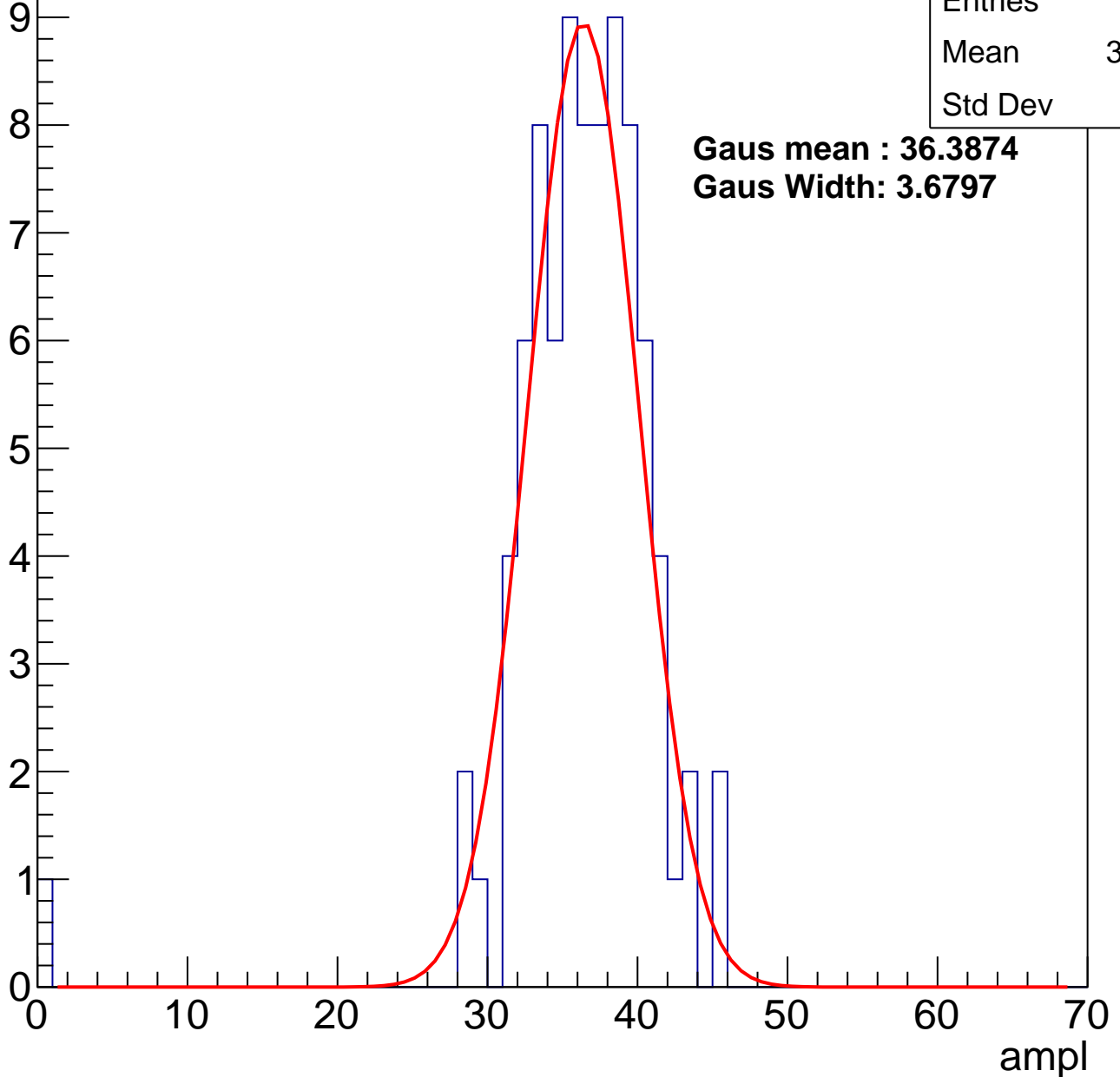
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	85
Mean	35.81
Std Dev	5.29

**Gaus mean : 36.3874**

**Gaus Width: 3.6797**



# B1L003S, U26-ch80, adc2

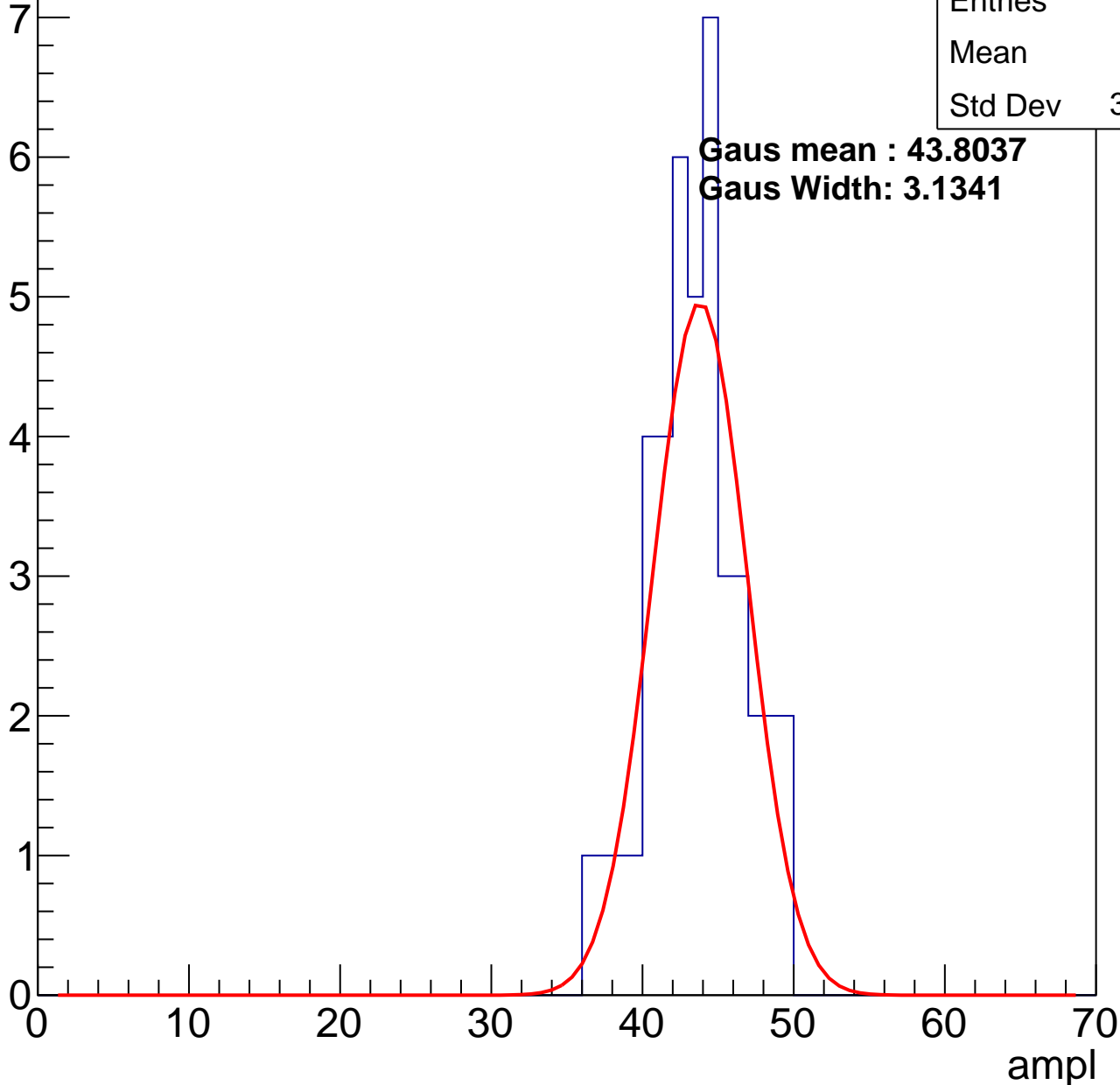
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	42
Mean	43.1
Std Dev	3.022

**Gaus mean : 43.8037**

**Gaus Width: 3.1341**

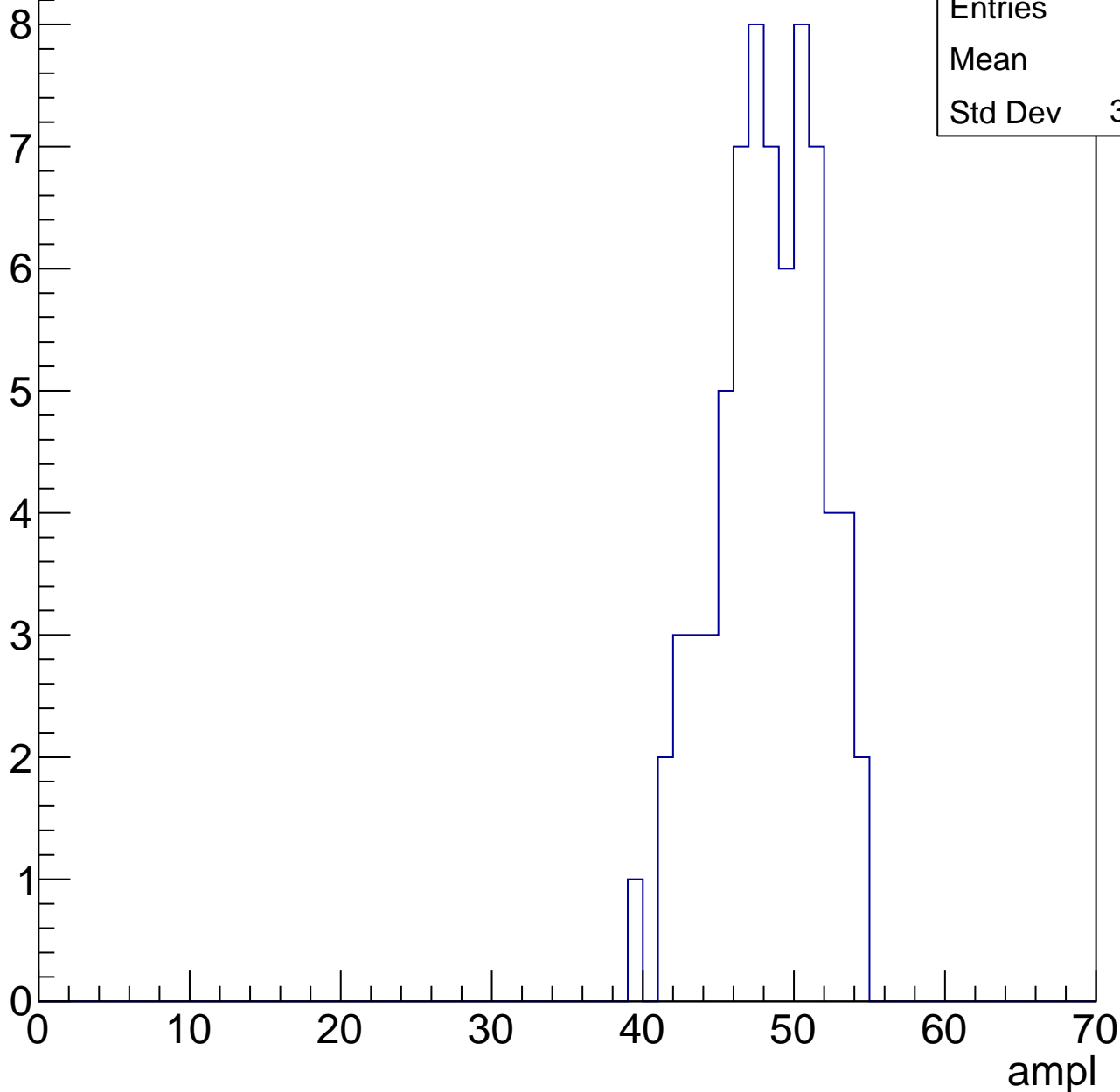


# B1L003S, U26-ch80, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	47.8
Std Dev	3.433

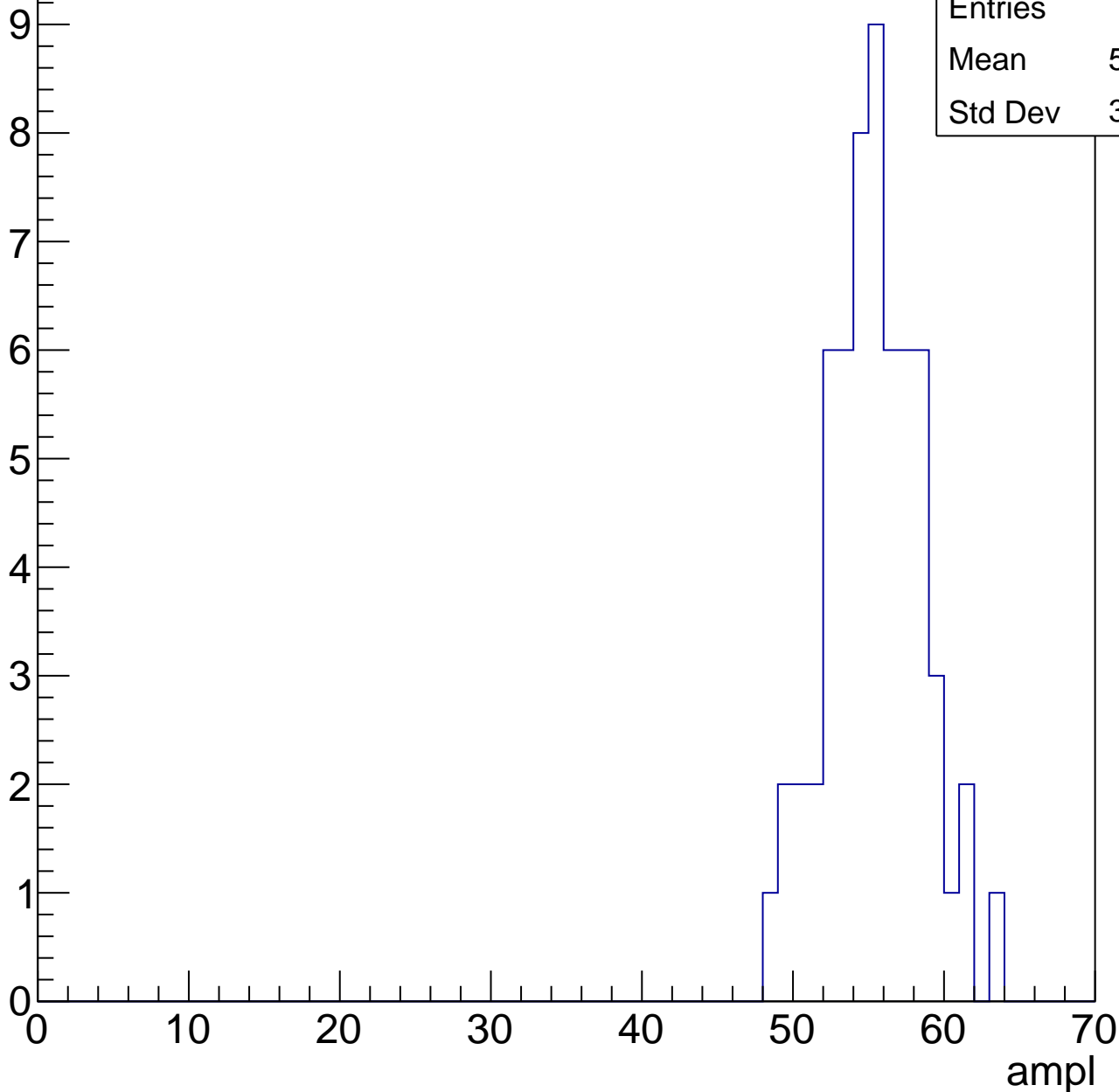


# B1L003S, U26-ch80, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	54.97
Std Dev	3.089

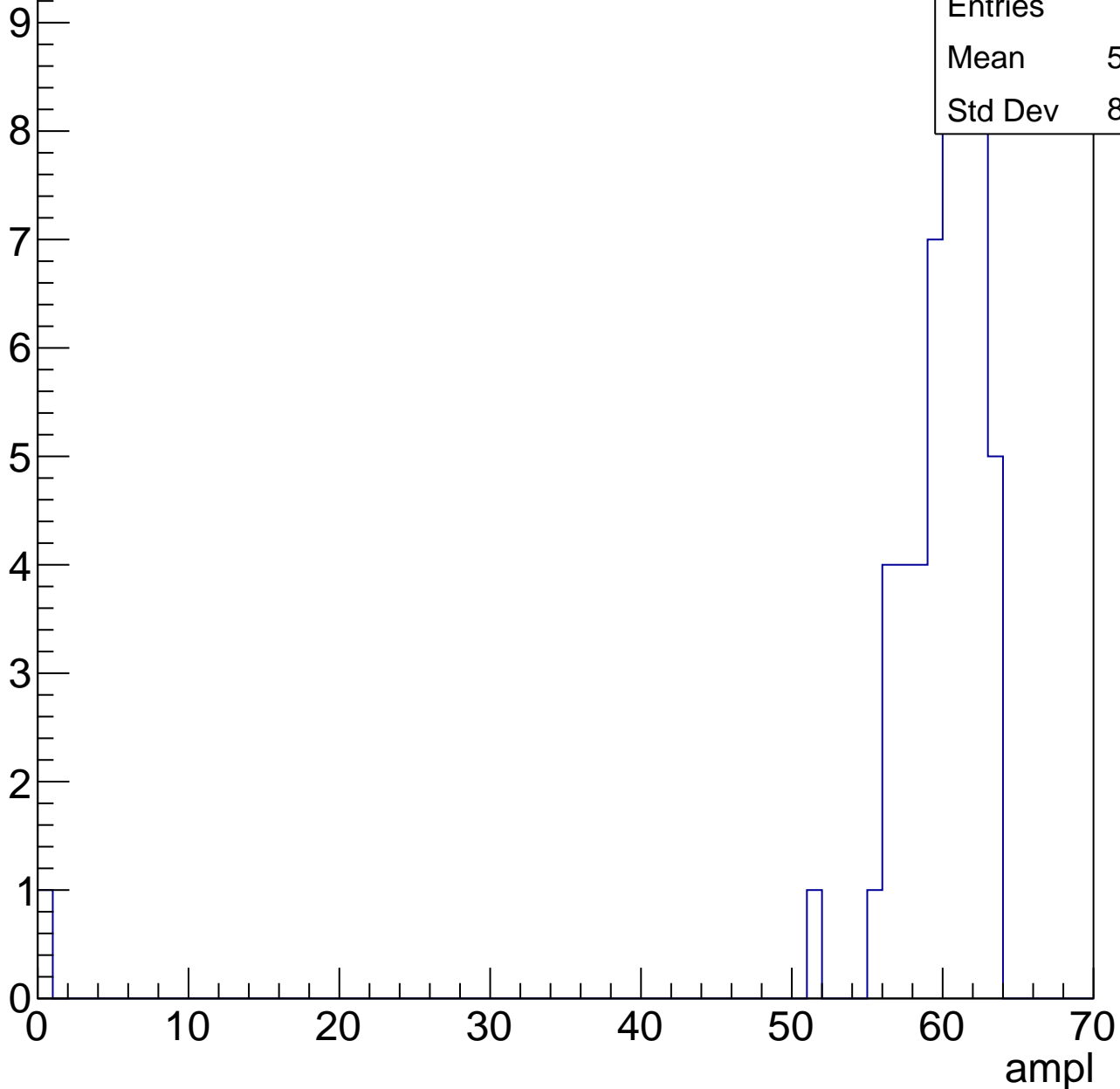


# B1L003S, U26-ch80, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	58.57
Std Dev	8.478



# B1L003S, U26-ch80, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch80, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

1

Mean

63

Std Dev

0

# B1L003S, U26-ch81, adc0

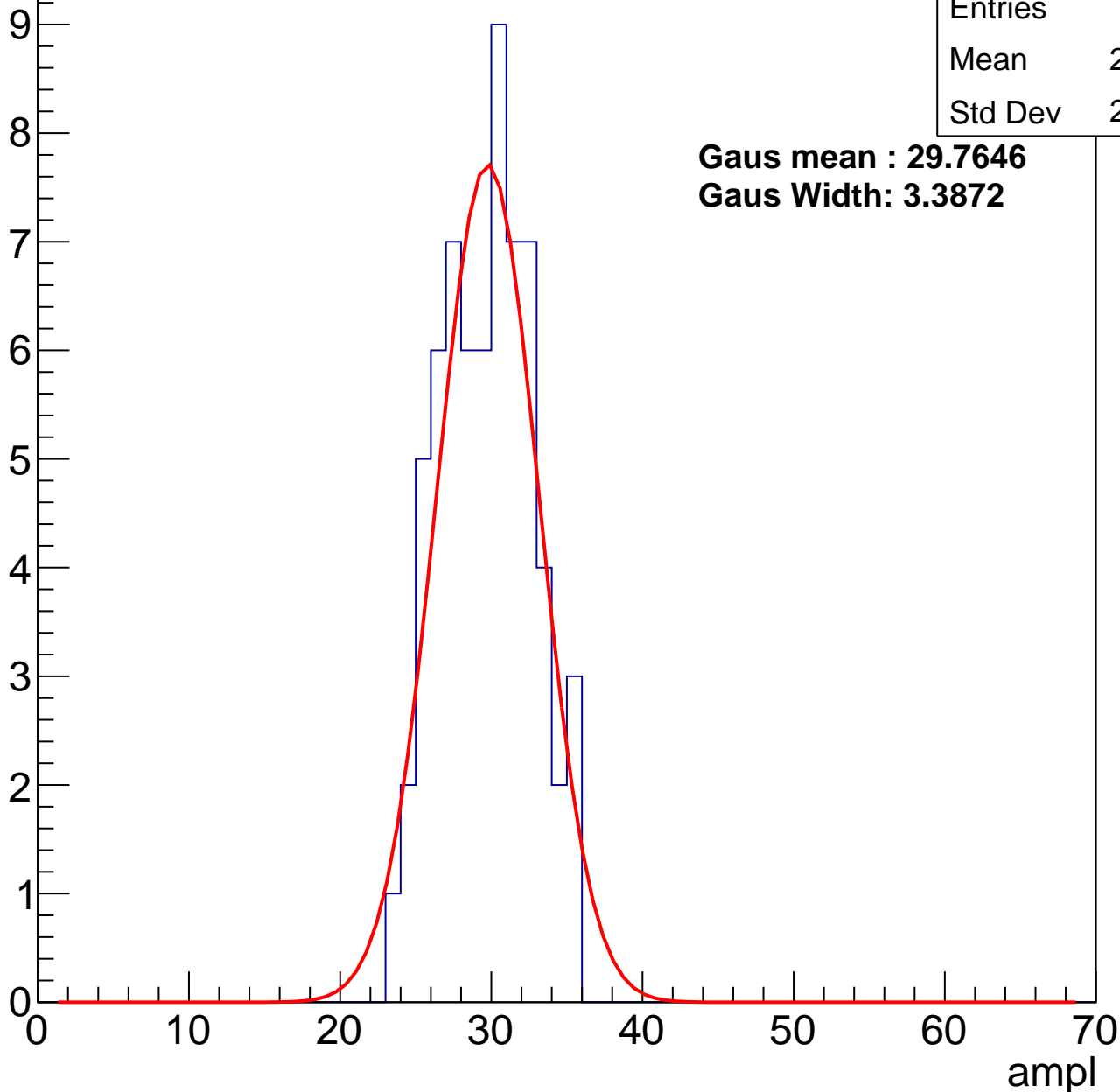
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	29.22
Std Dev	2.969

**Gaus mean : 29.7646**

**Gaus Width: 3.3872**



# B1L003S, U26-ch81, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	70
Mean	36.19
Std Dev	3.077

**Gaus mean : 36.6649**

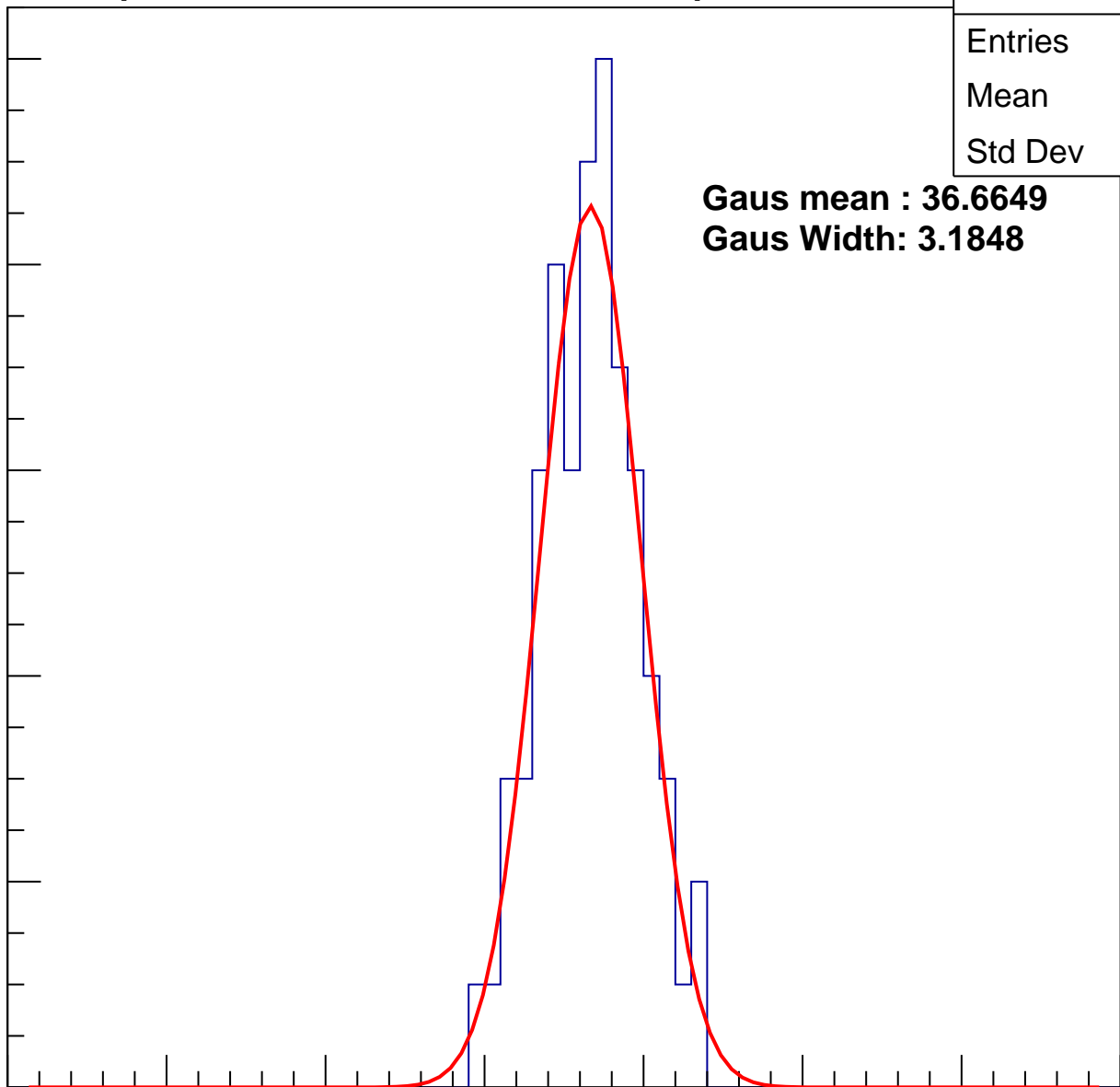
**Gaus Width: 3.1848**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U26-ch81, adc2

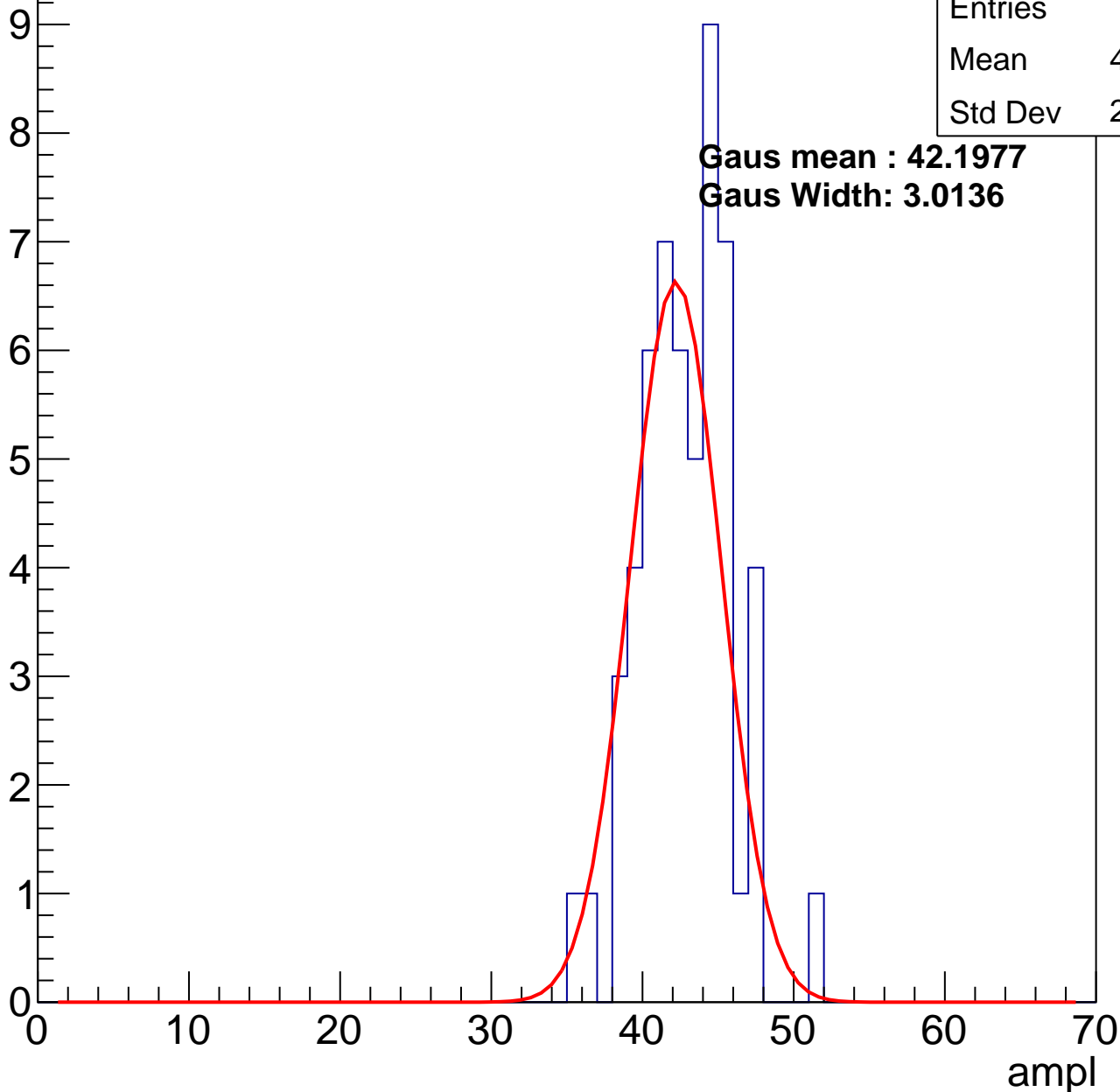
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	42.38
Std Dev	2.994

**Gaus mean : 42.1977**

**Gaus Width: 3.0136**

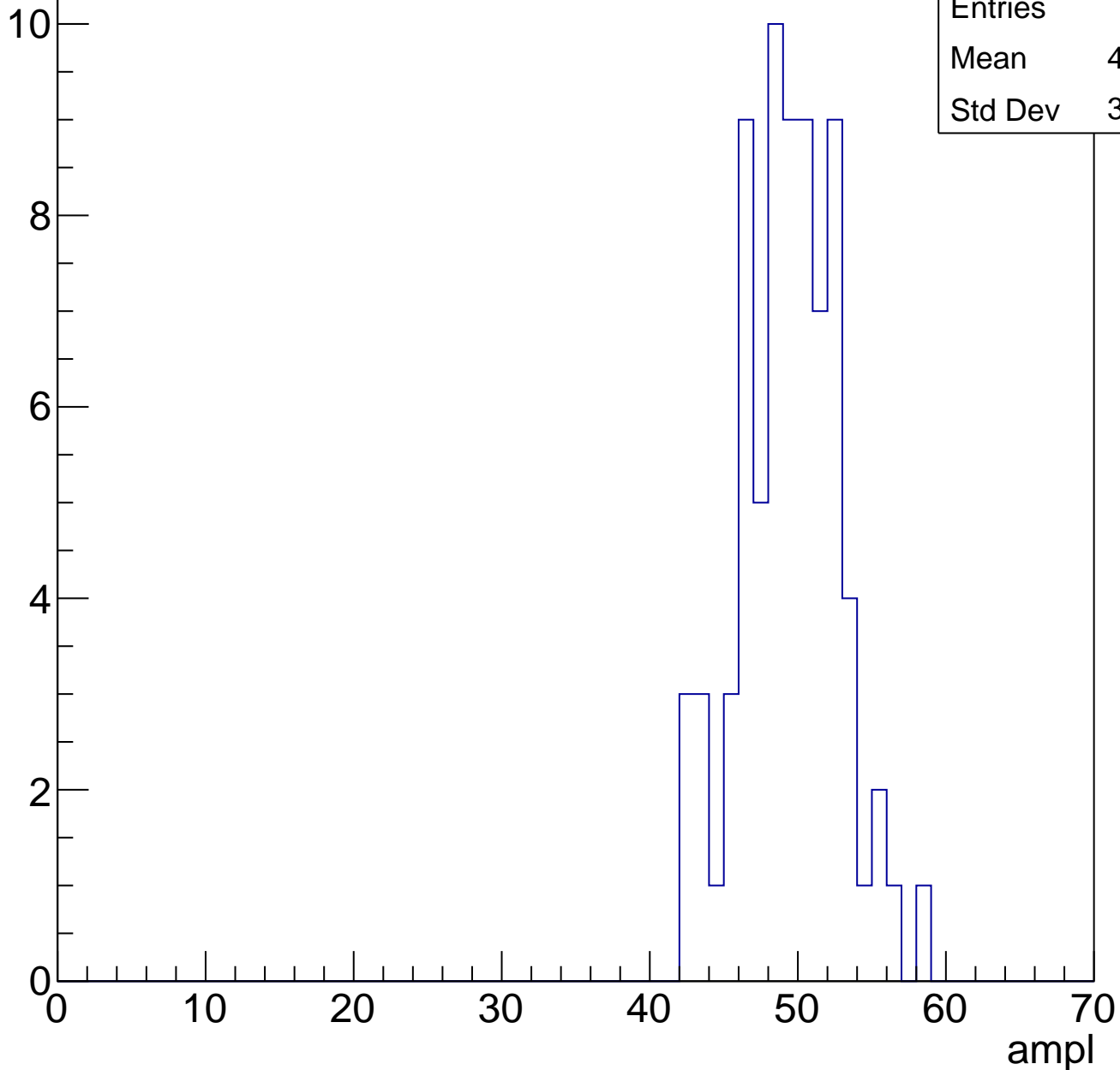


# B1L003S, U26-ch81, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	77
Mean	48.95
Std Dev	3.318

Entry

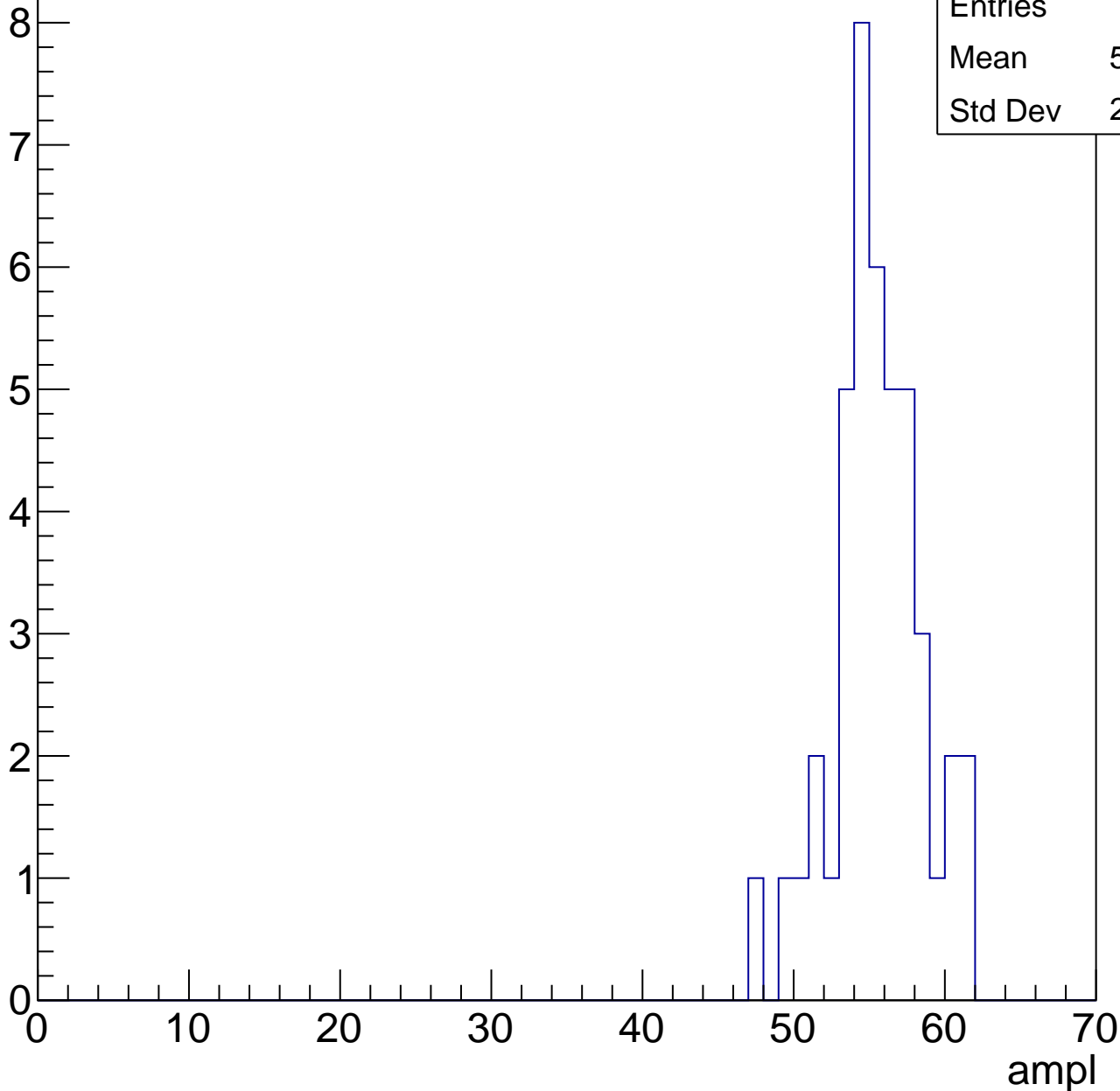


# B1L003S, U26-ch81, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	43
Mean	55.05
Std Dev	2.988

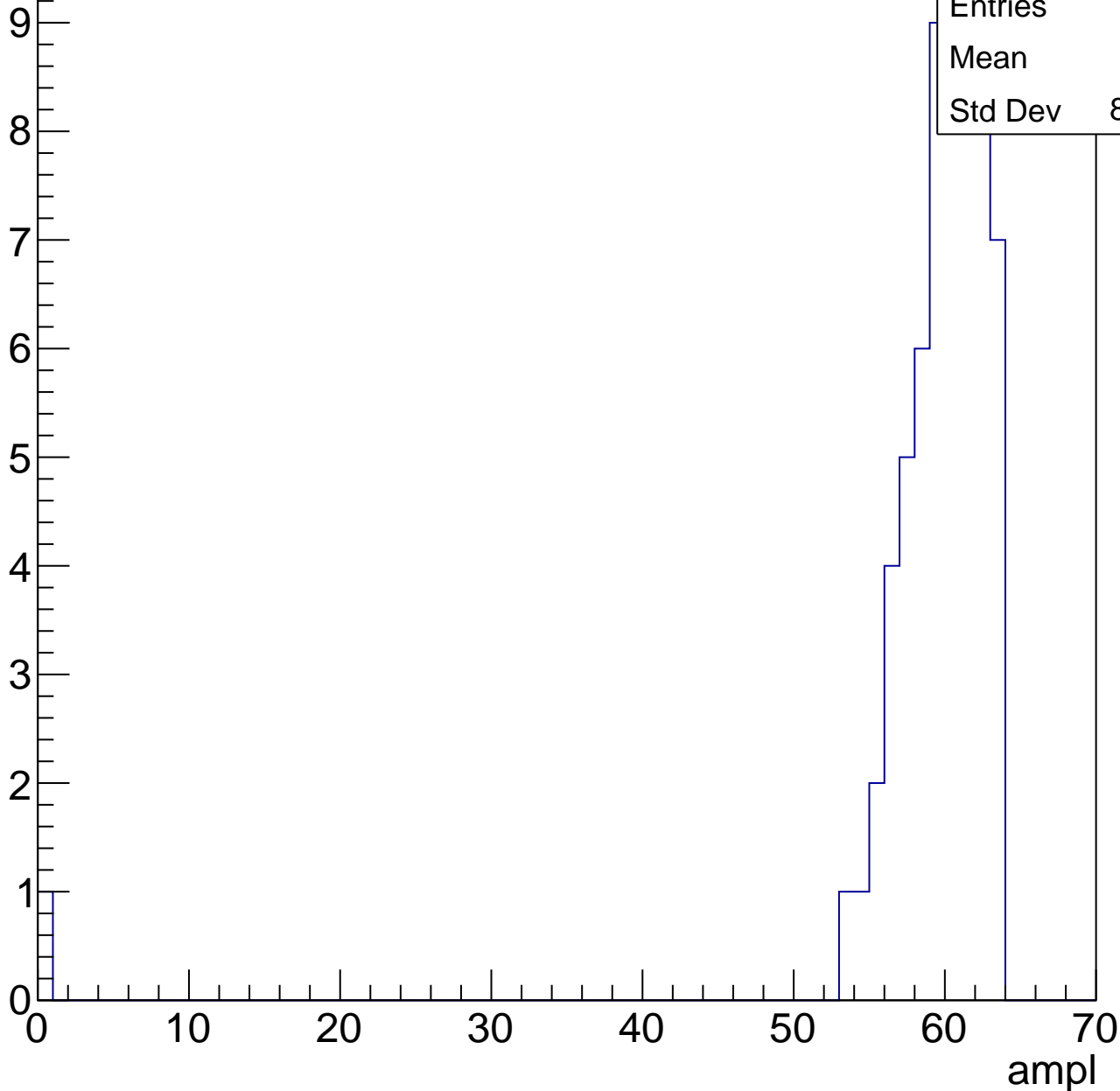


# B1L003S, U26-ch81, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	58.5
Std Dev	8.005



# B1L003S, U26-ch81, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch81, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U26-ch82, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	77
Mean	30.25
Std Dev	5.079

**Gaus mean : 30.9883**

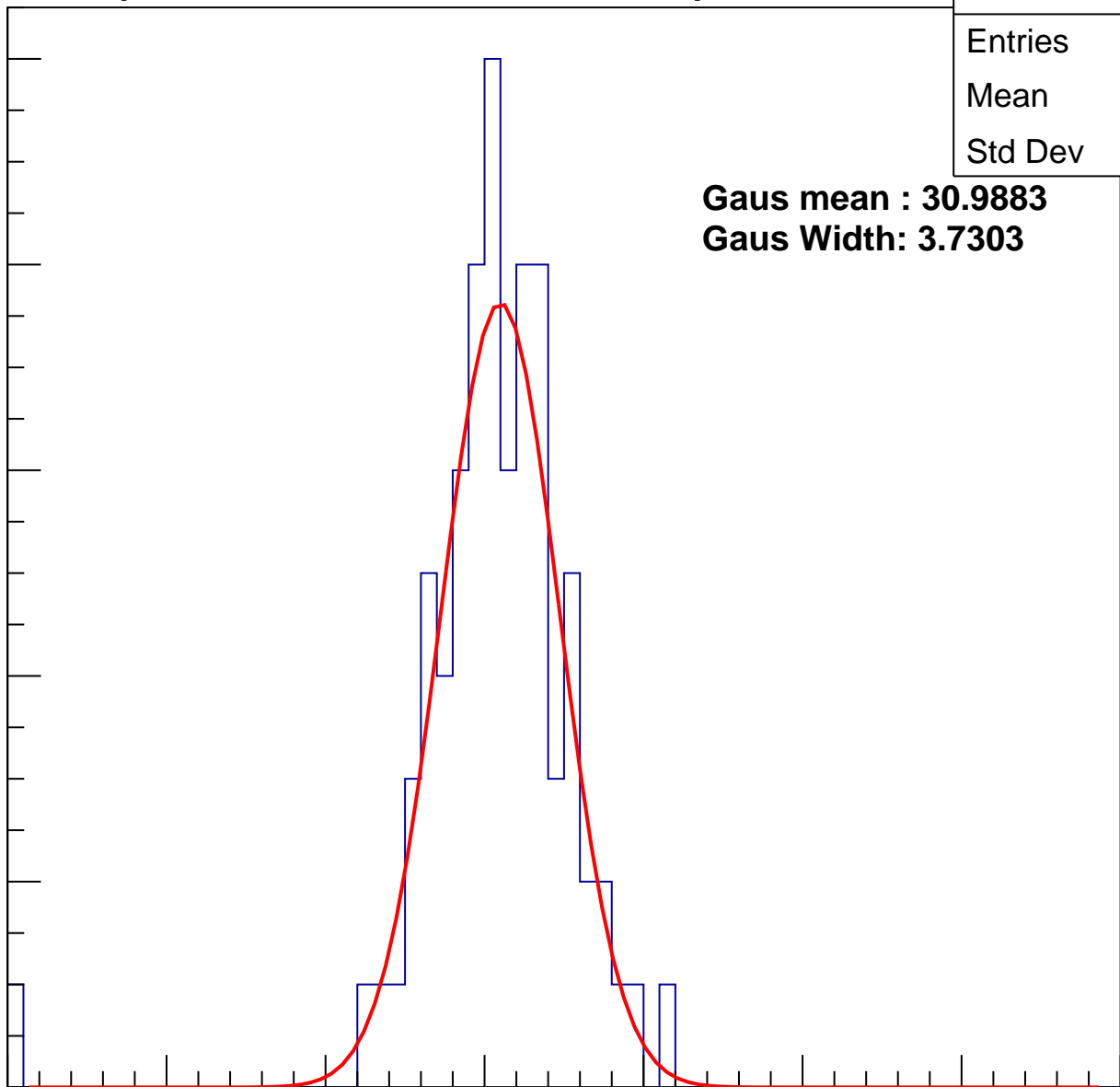
**Gaus Width: 3.7303**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U26-ch82, adc1

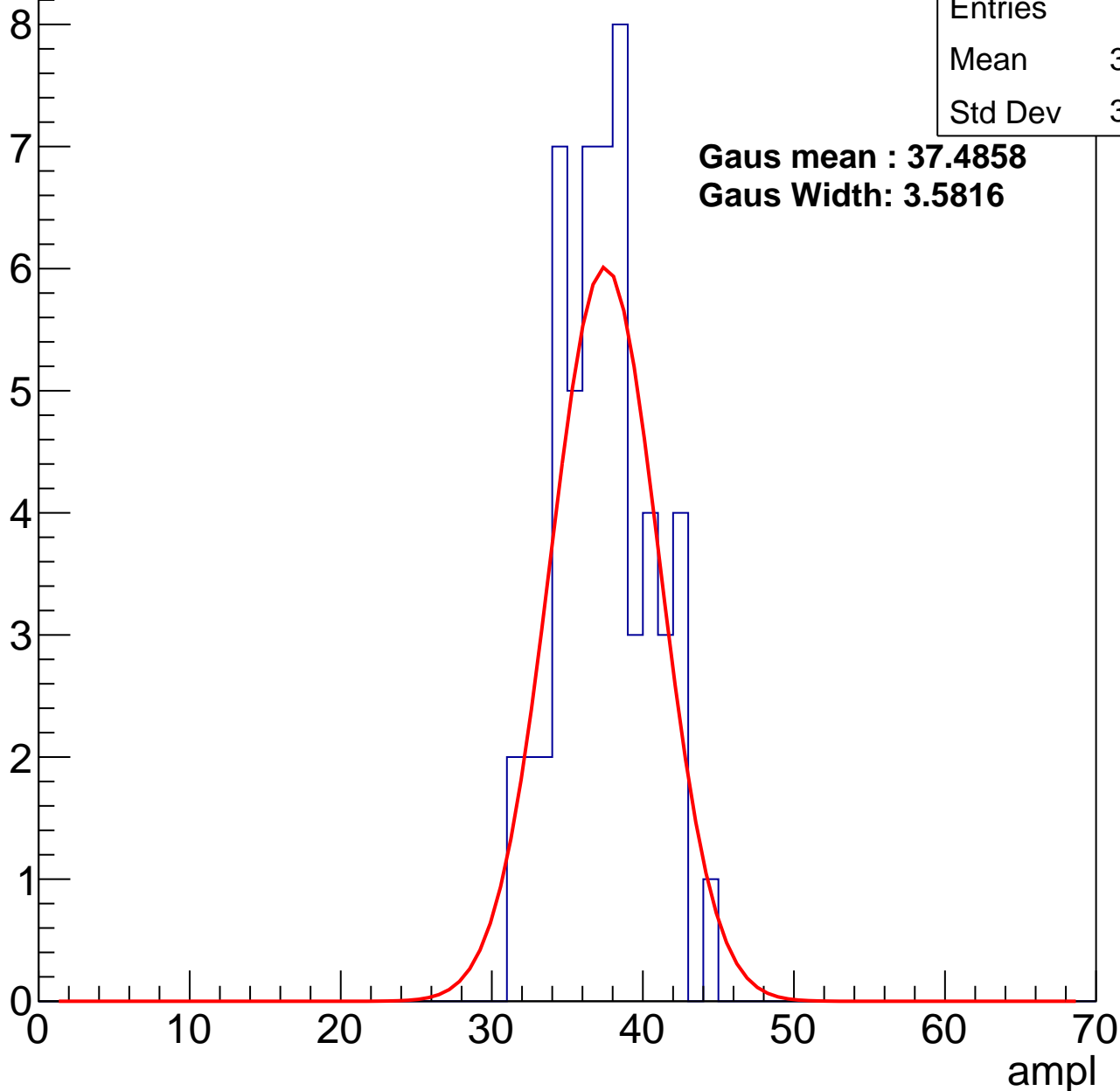
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	36.95
Std Dev	3.006

**Gaus mean : 37.4858**

**Gaus Width: 3.5816**



# B1L003S, U26-ch82, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	77
Mean	43.92
Std Dev	3.588

**Gaus mean : 44.2346**

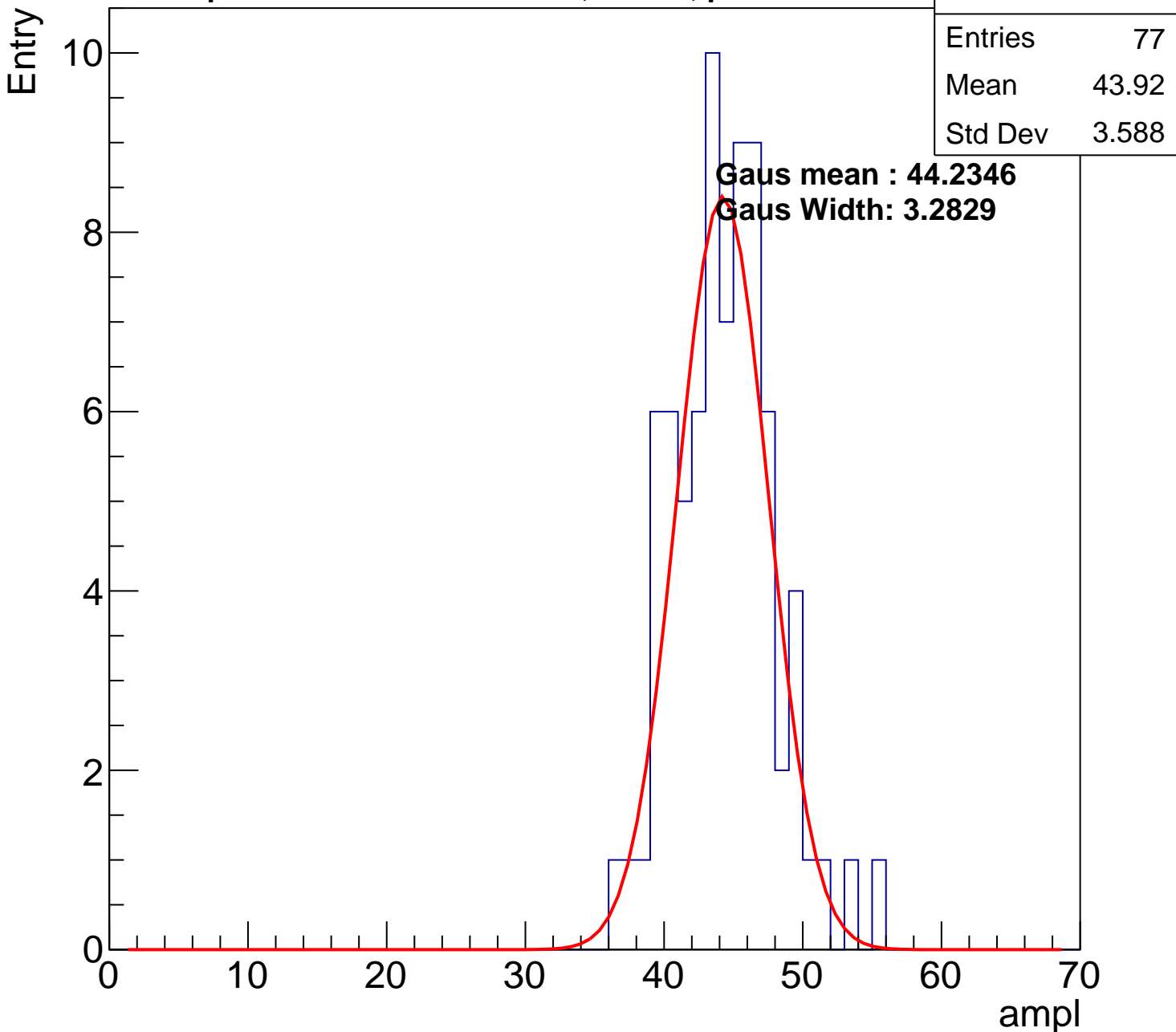
**Gaus Width: 3.2829**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

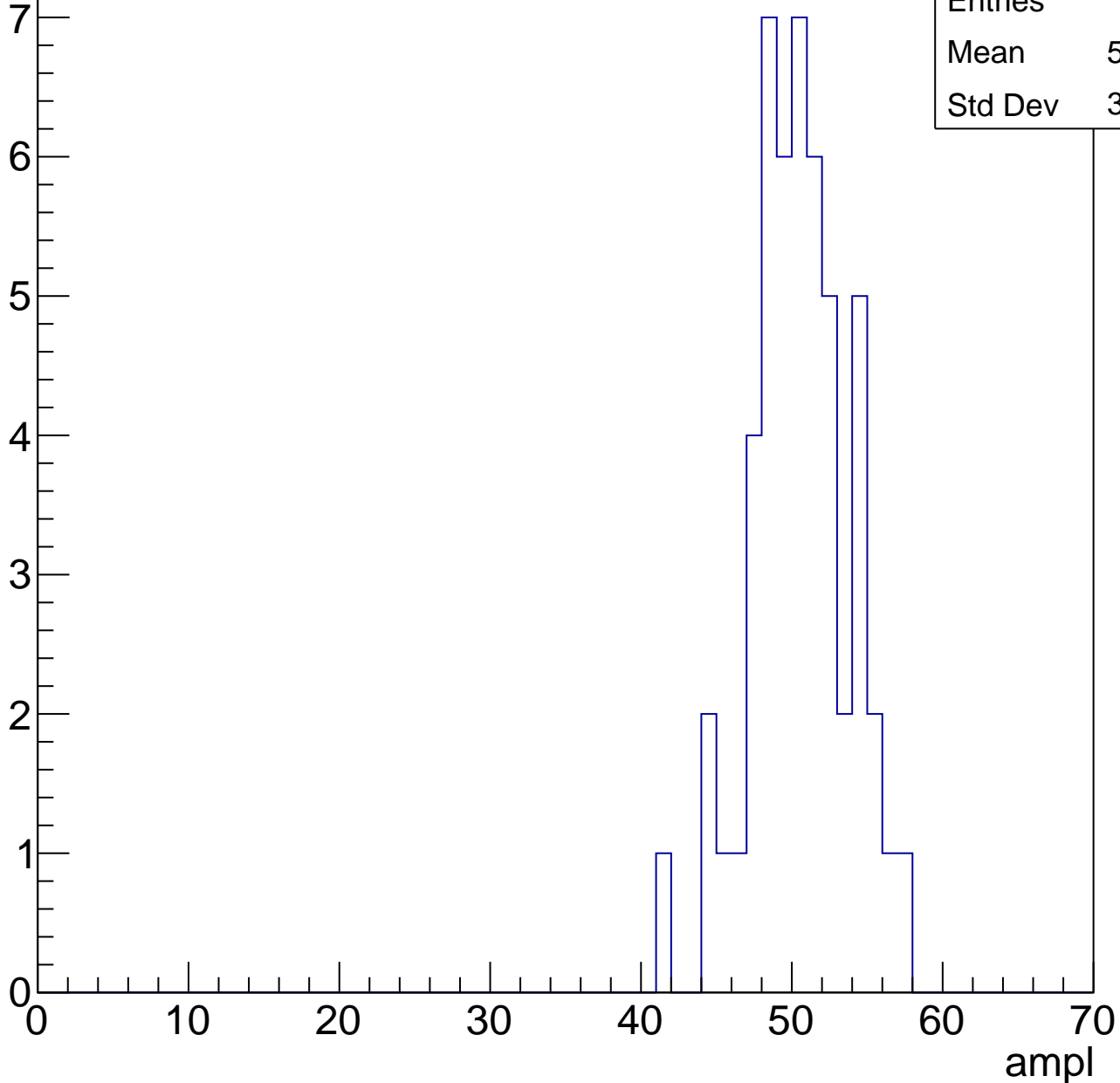


# B1L003S, U26-ch82, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	51
Mean	50.06
Std Dev	3.202

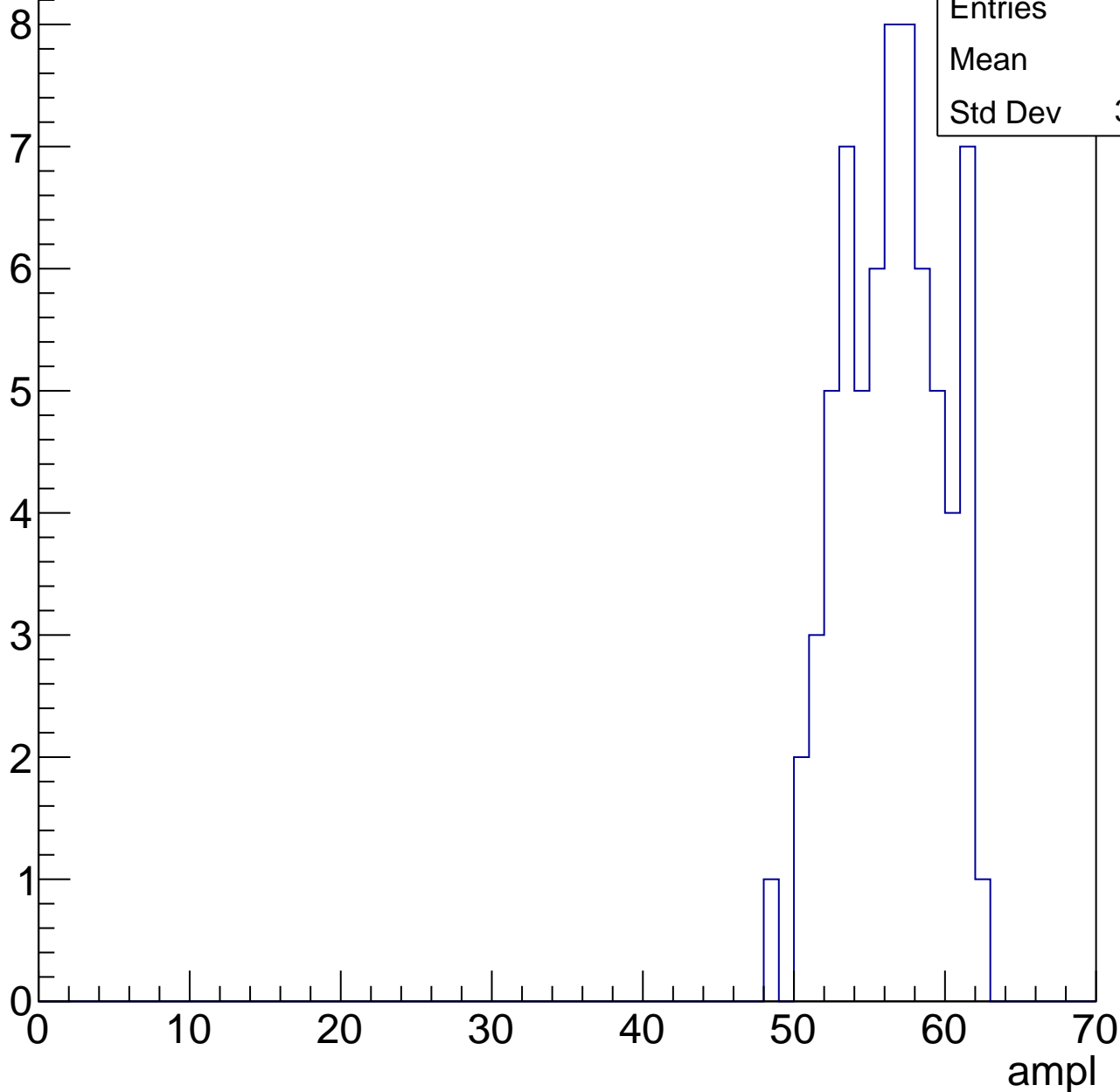


# B1L003S, U26-ch82, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	56
Std Dev	3.281

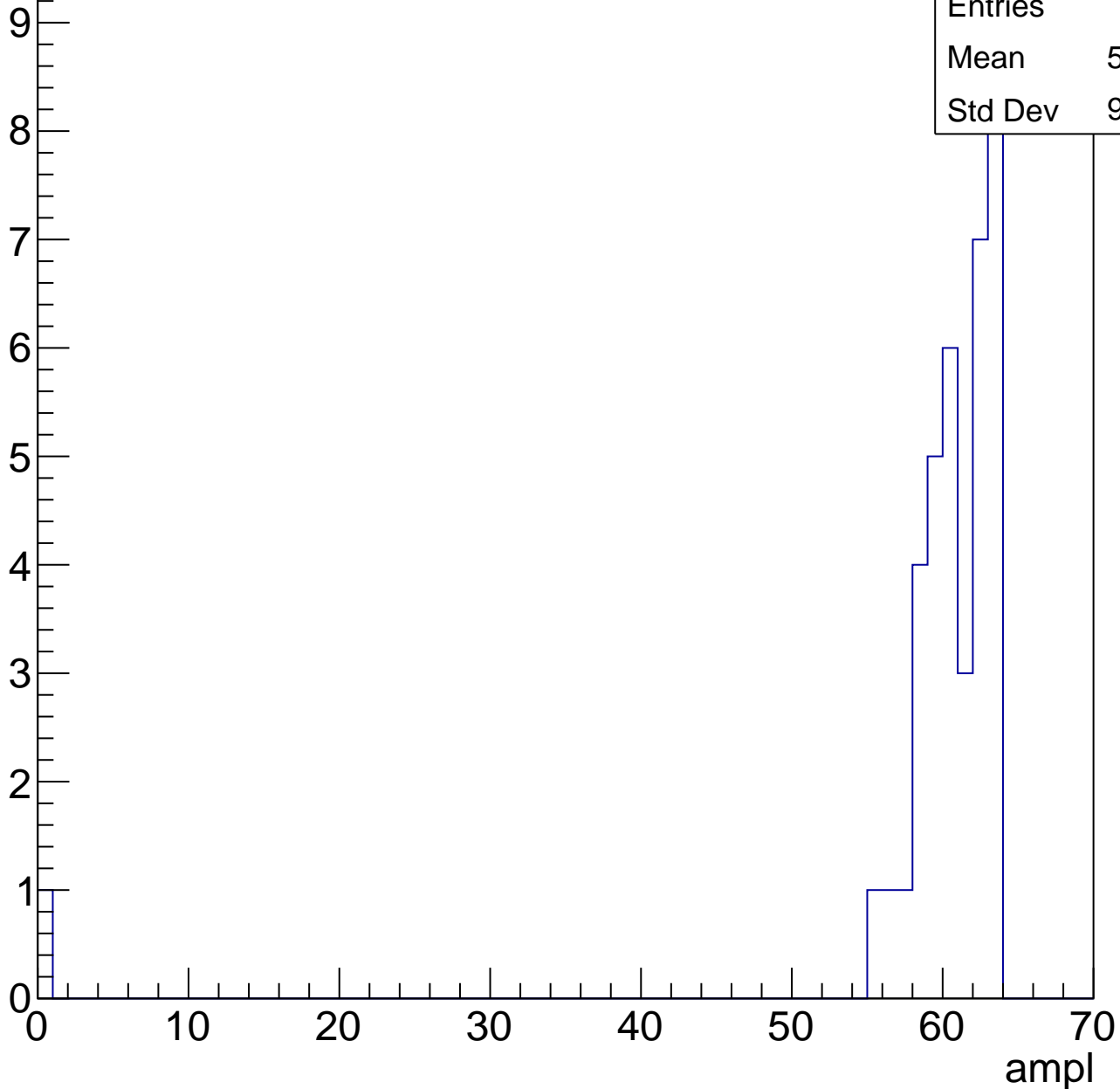


# B1L003S, U26-ch82, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	38
Mean	58.92
Std Dev	9.919



# B1L003S, U26-ch82, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch82, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L003S, U26-ch83, adc0

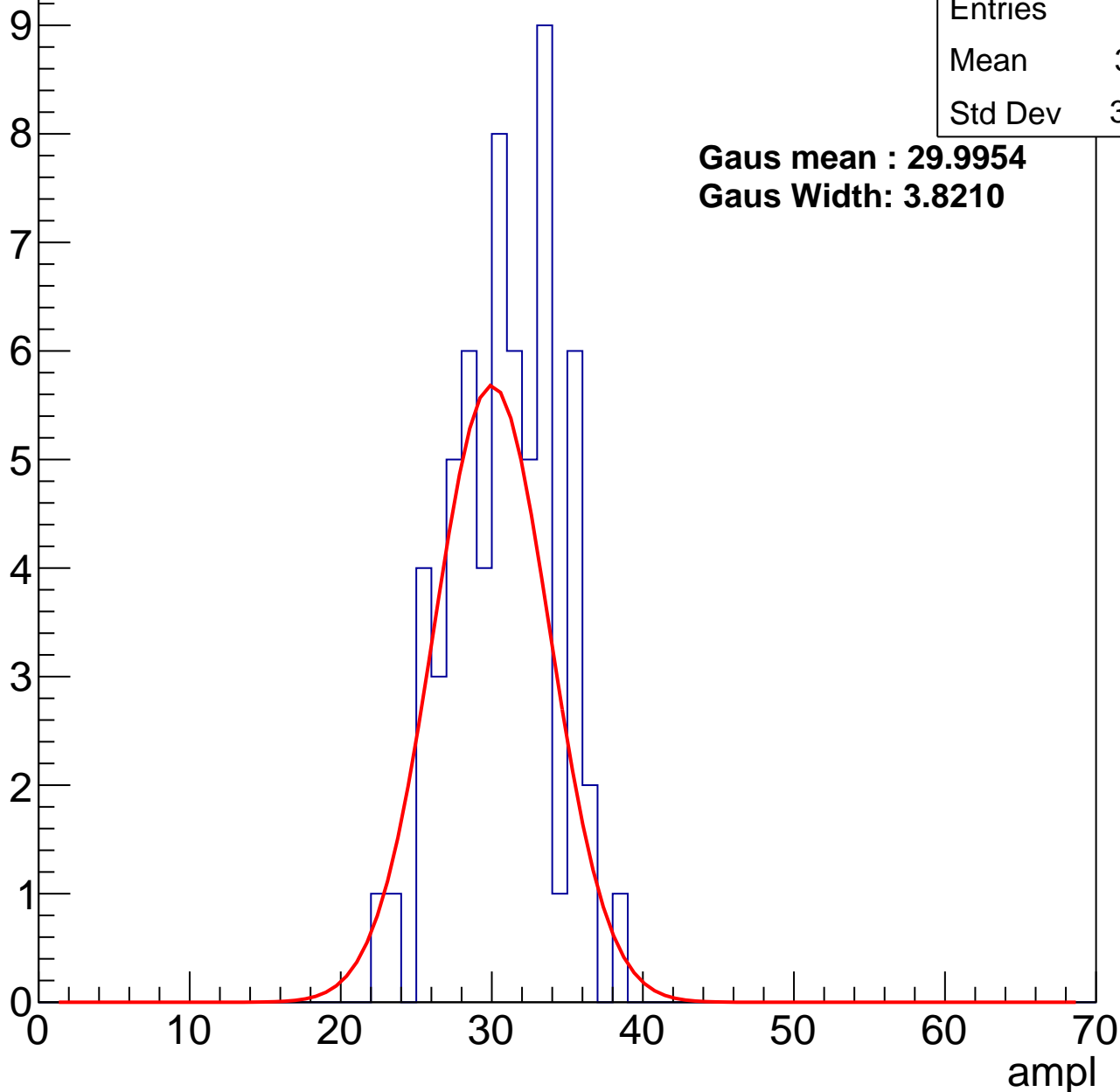
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	30.31
Std Dev	3.448

**Gaus mean : 29.9954**

**Gaus Width: 3.8210**



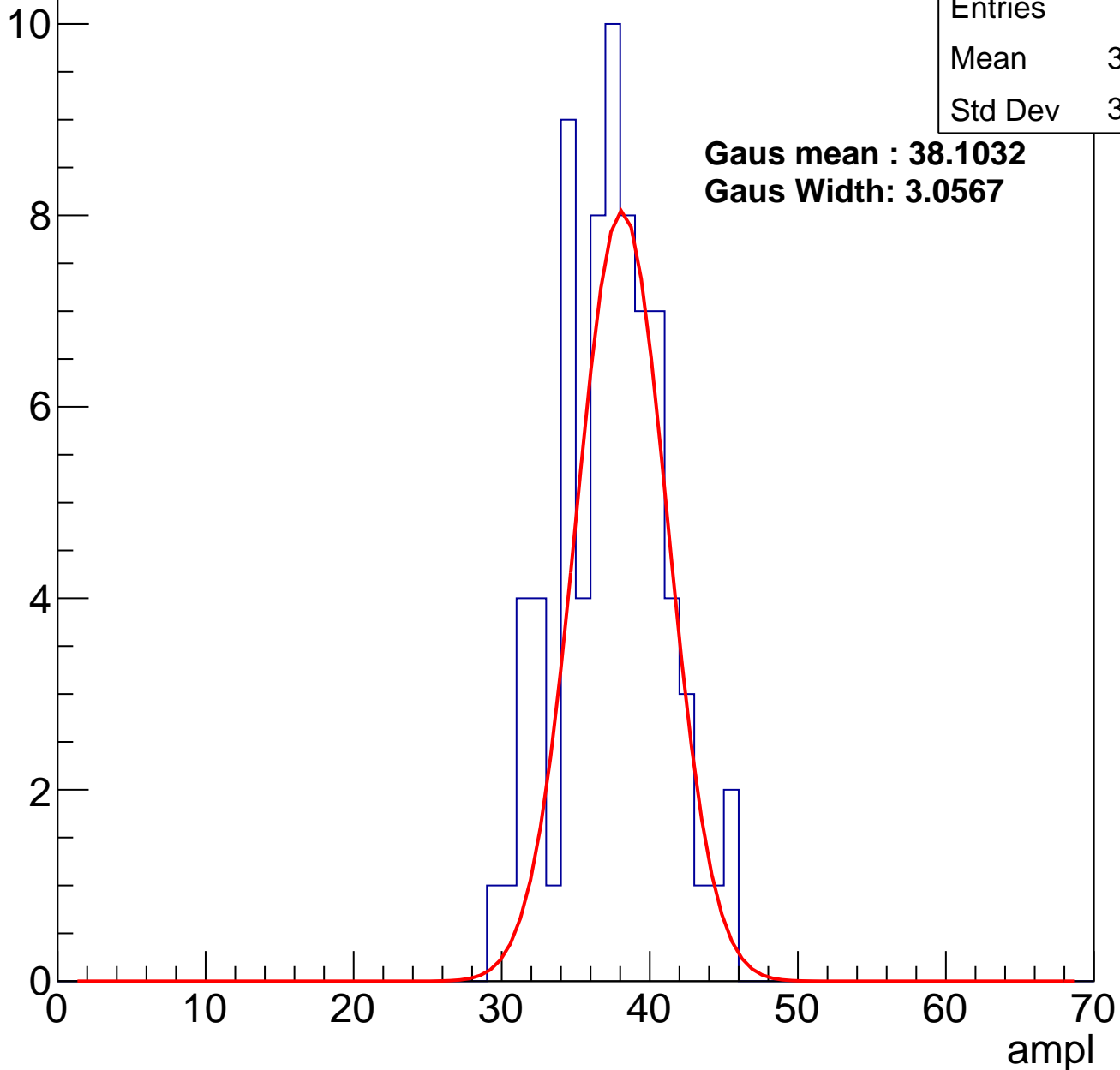
# B1L003S, U26-ch83, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	75
Mean	36.96
Std Dev	3.519

**Gaus mean : 38.1032**  
**Gaus Width: 3.0567**

Entry



# B1L003S, U26-ch83, adc2

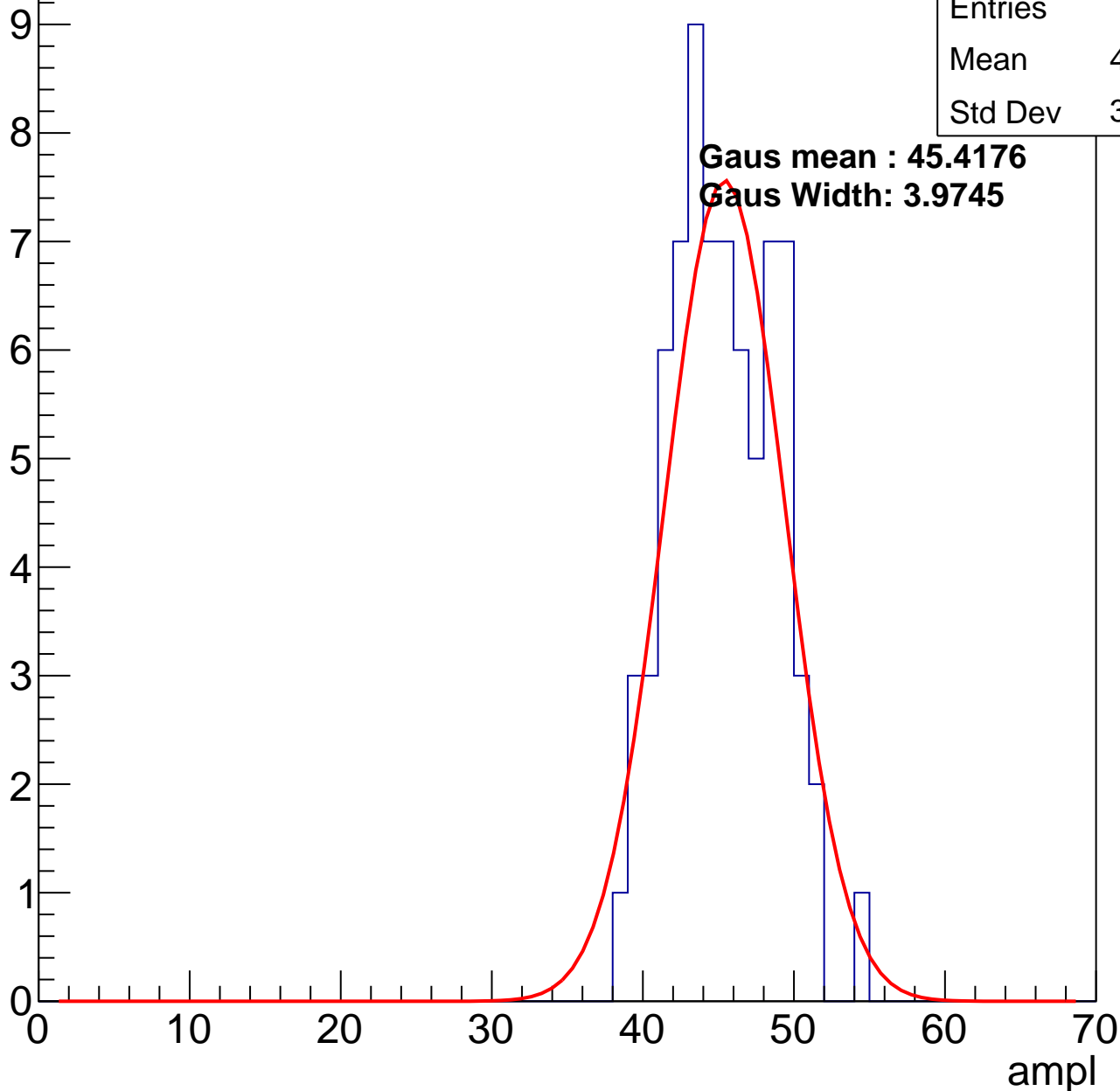
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	74
Mean	44.88
Std Dev	3.413

**Gaus mean : 45.4176**

**Gaus Width: 3.9745**

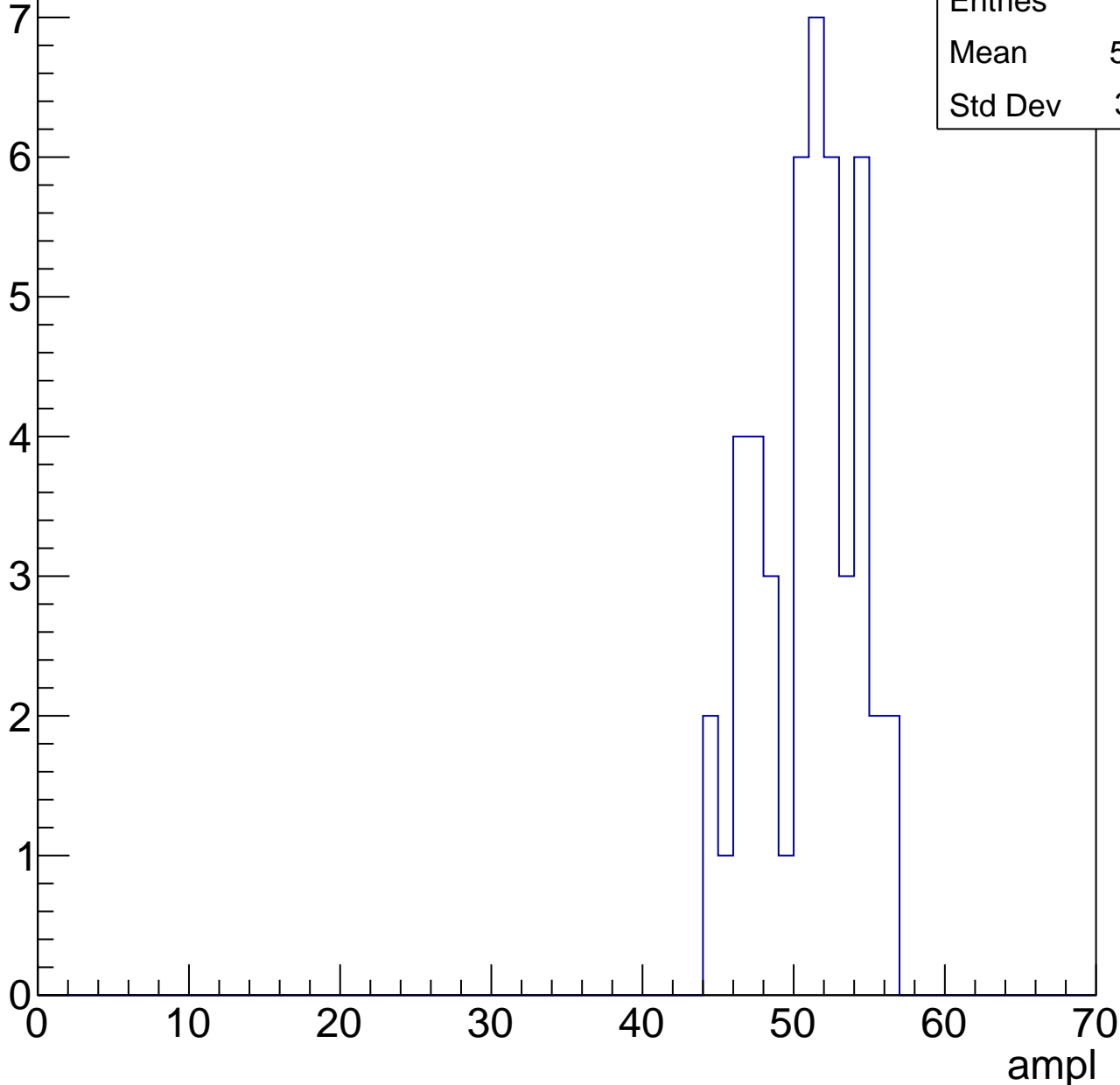


# B1L003S, U26-ch83, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	47
Mean	50.47
Std Dev	3.181

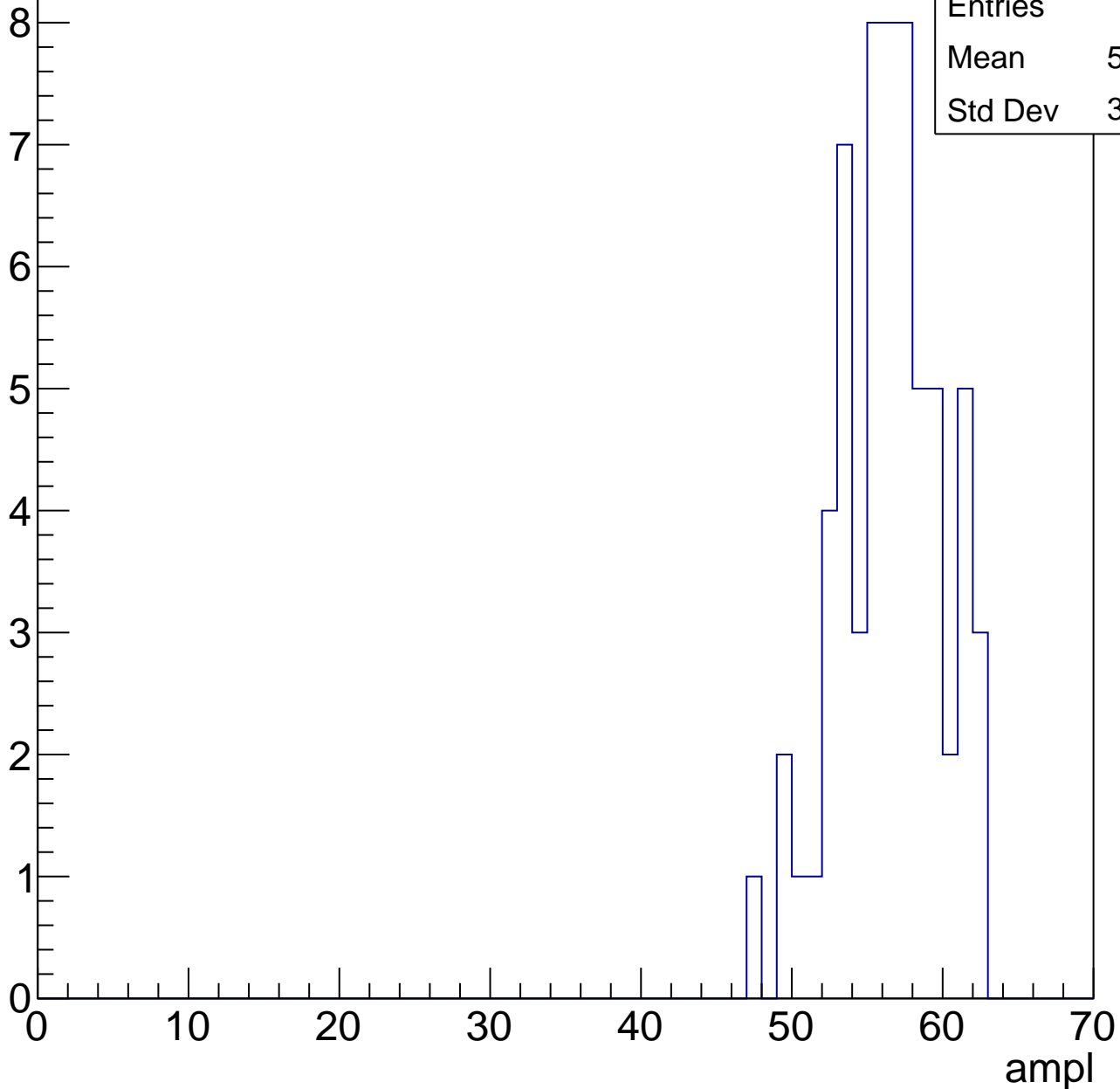


# B1L003S, U26-ch83, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	55.98
Std Dev	3.392

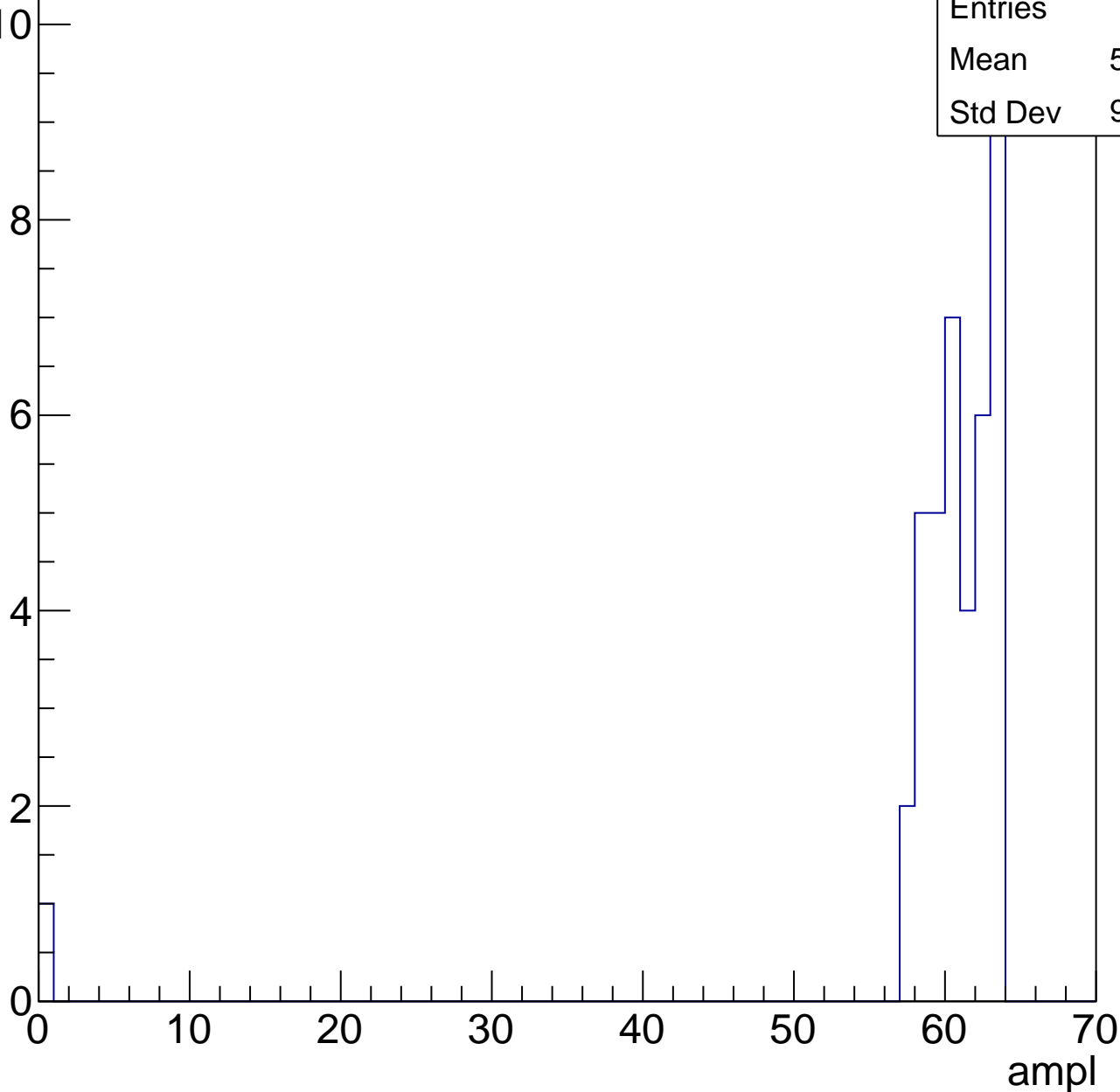


# B1L003S, U26-ch83, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	40
Mean	59.12
Std Dev	9.657



# B1L003S, U26-ch83, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch83, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U26-ch84, adc0

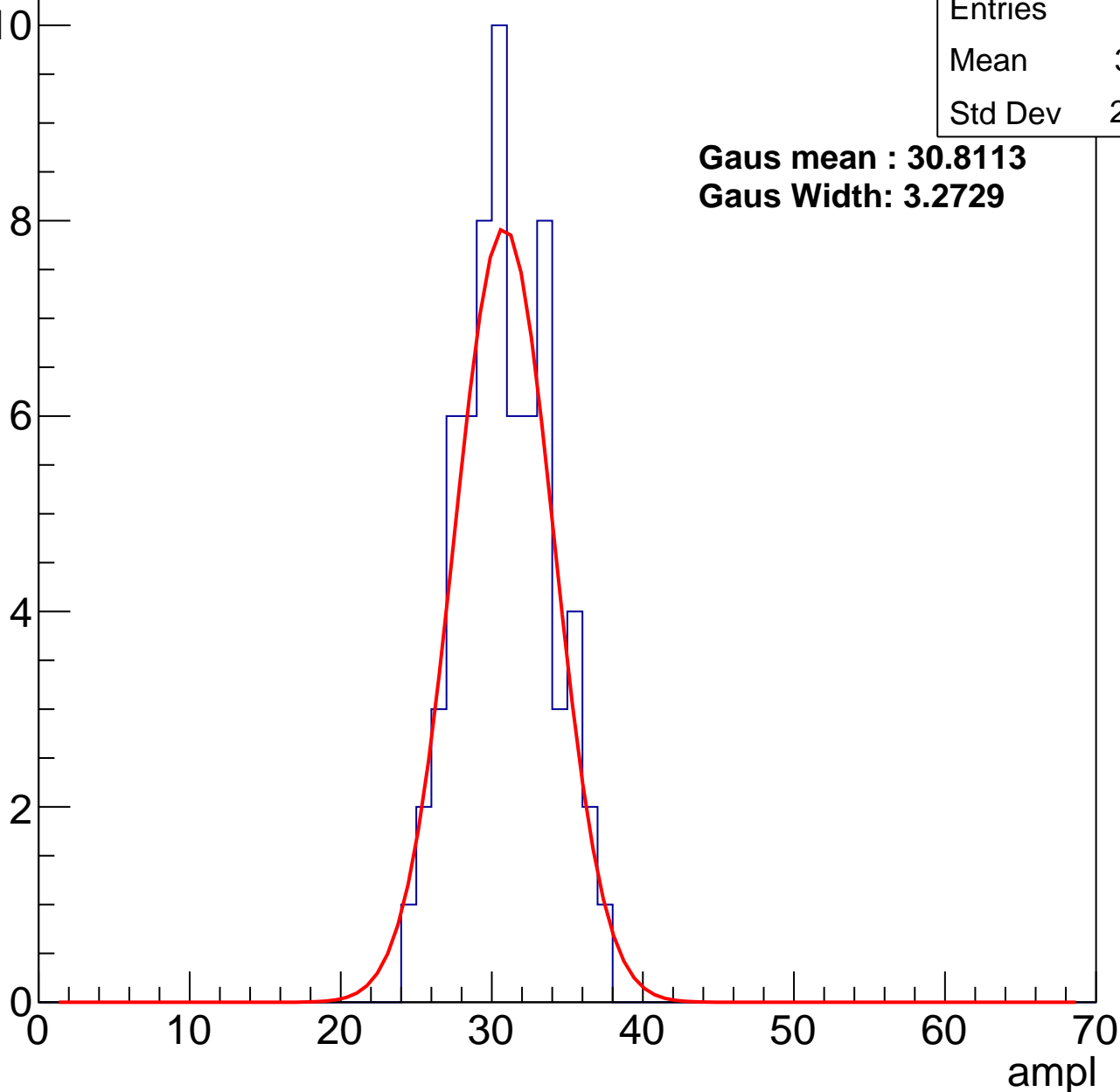
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	30.41
Std Dev	2.964

**Gaus mean : 30.8113**

**Gaus Width: 3.2729**



# B1L003S, U26-ch84, adc1

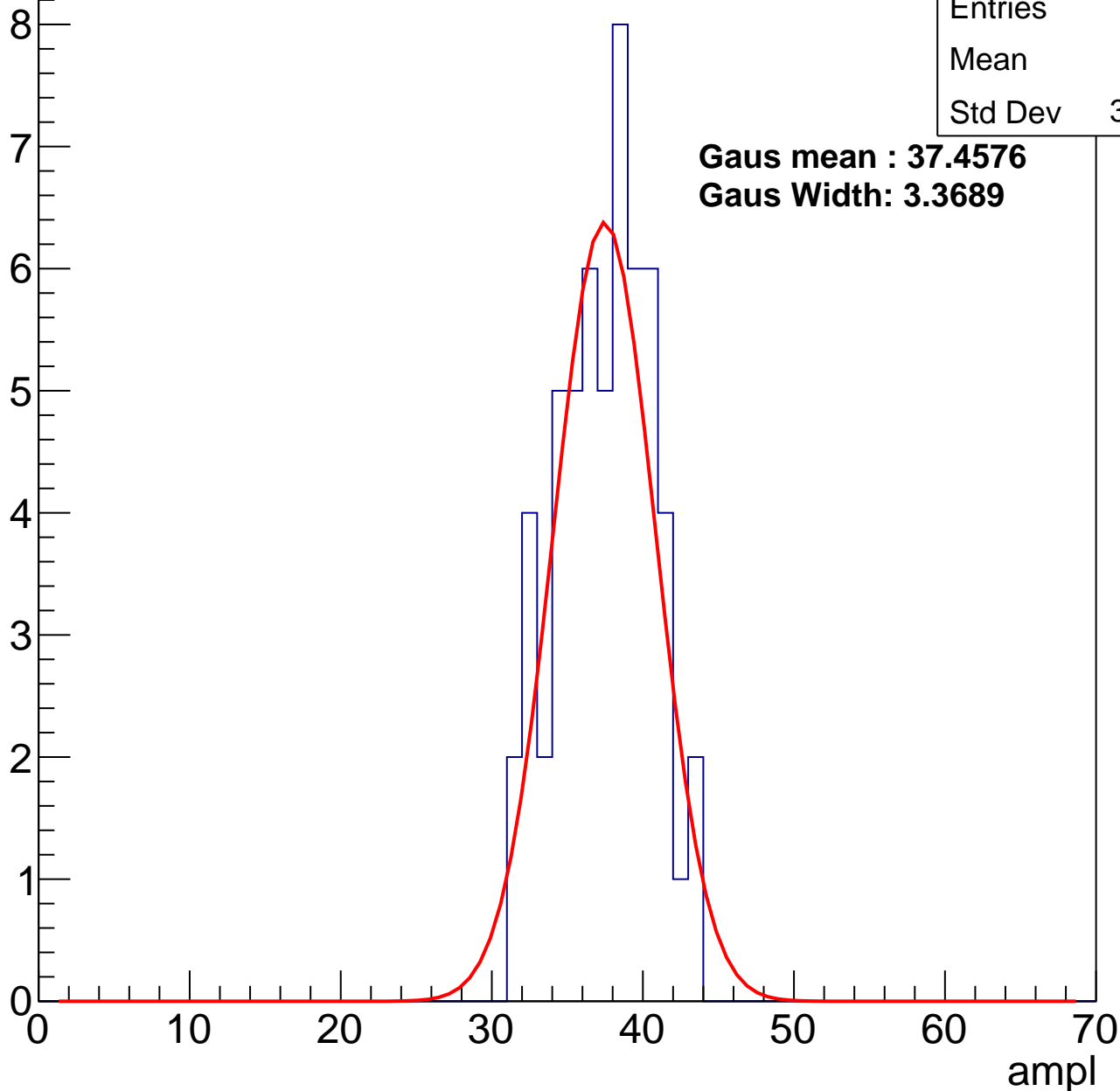
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	37
Std Dev	3.053

**Gaus mean : 37.4576**

**Gaus Width: 3.3689**



# B1L003S, U26-ch84, adc2

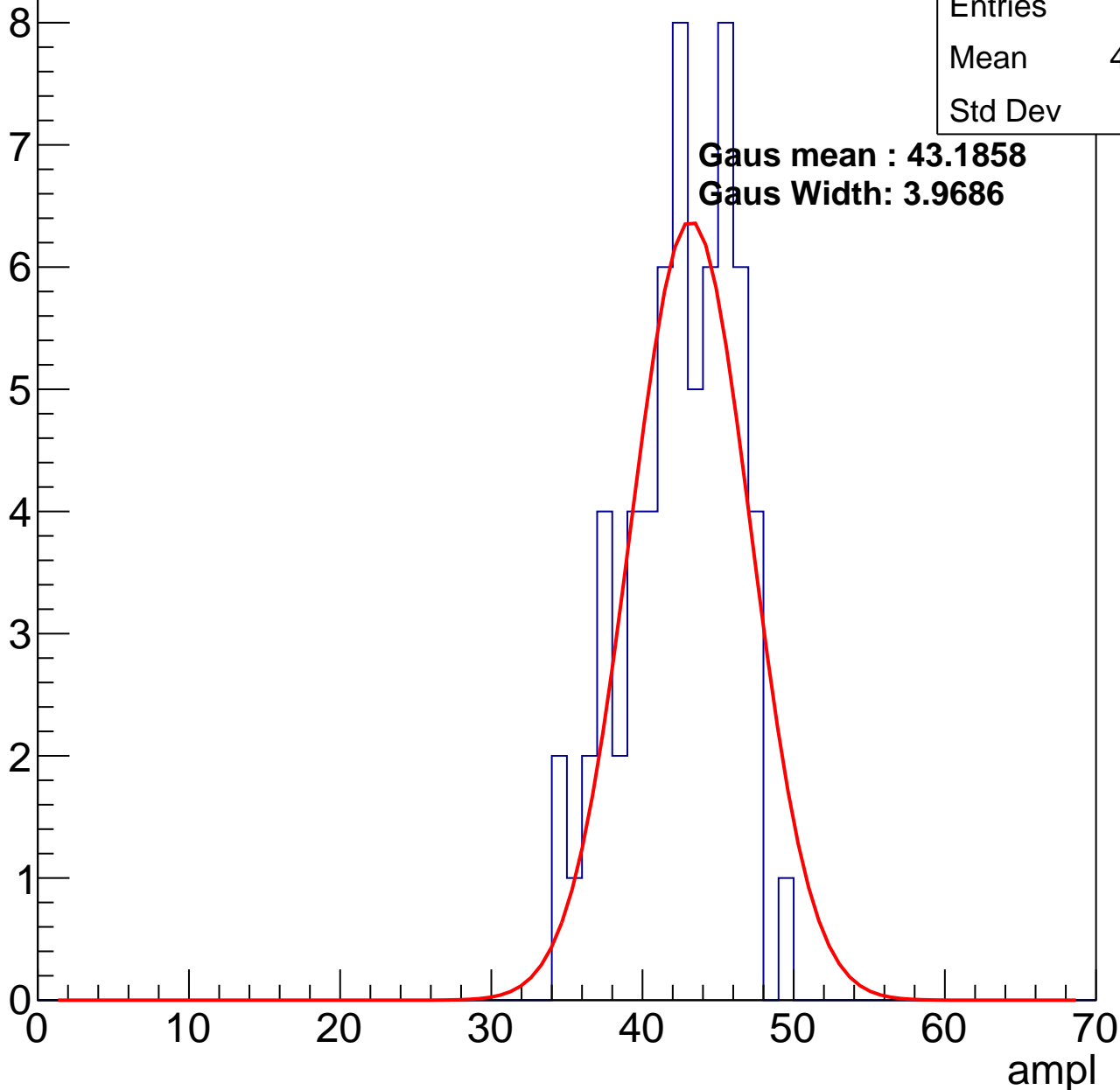
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	42.05
Std Dev	3.53

**Gaus mean : 43.1858**

**Gaus Width: 3.9686**



# B1L003S, U26-ch84, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	75
Mean	49.61
Std Dev	3.54

Entry

10

8

6

4

2

0

0

10

20

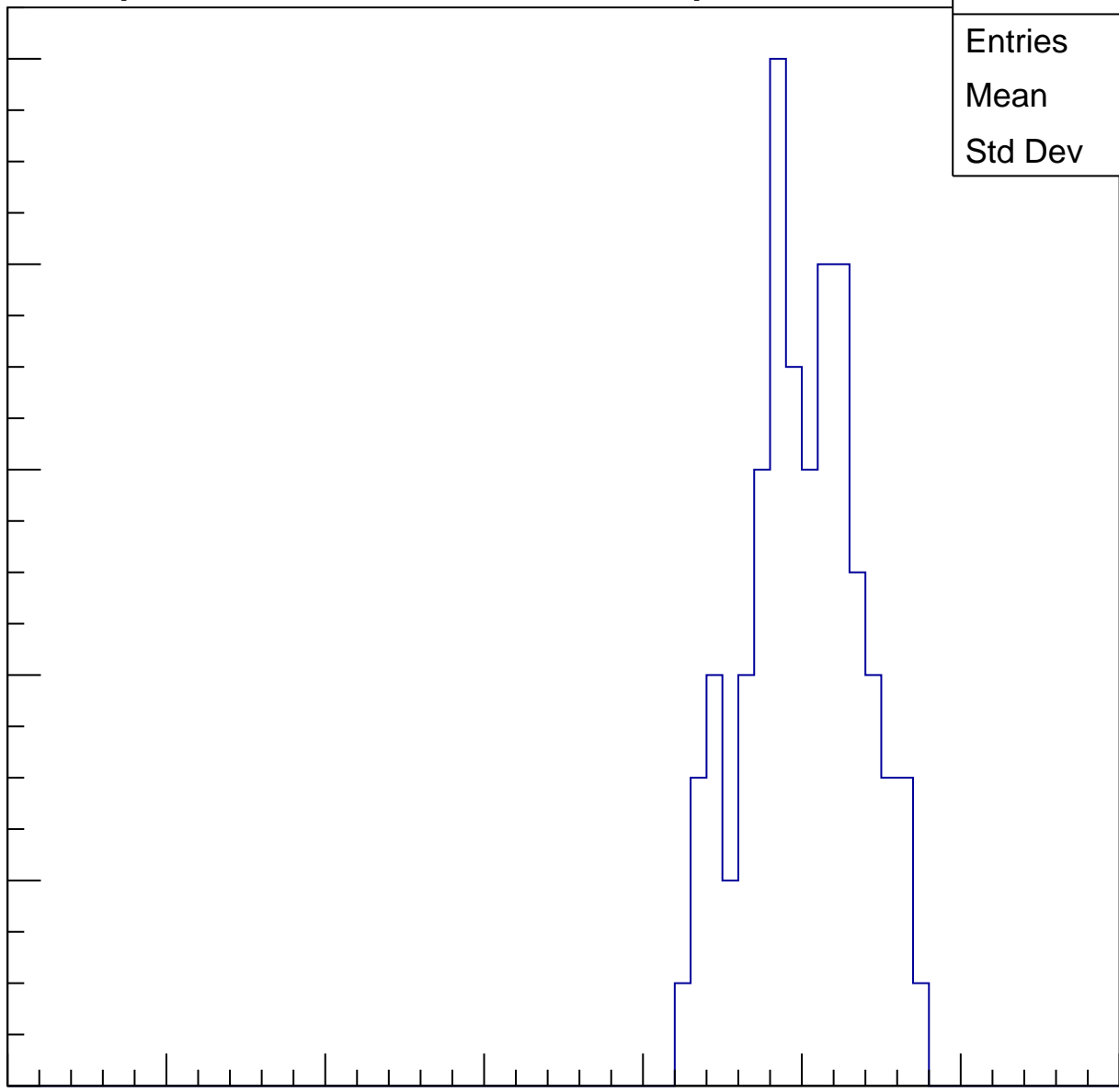
30

40

50

60

ampl

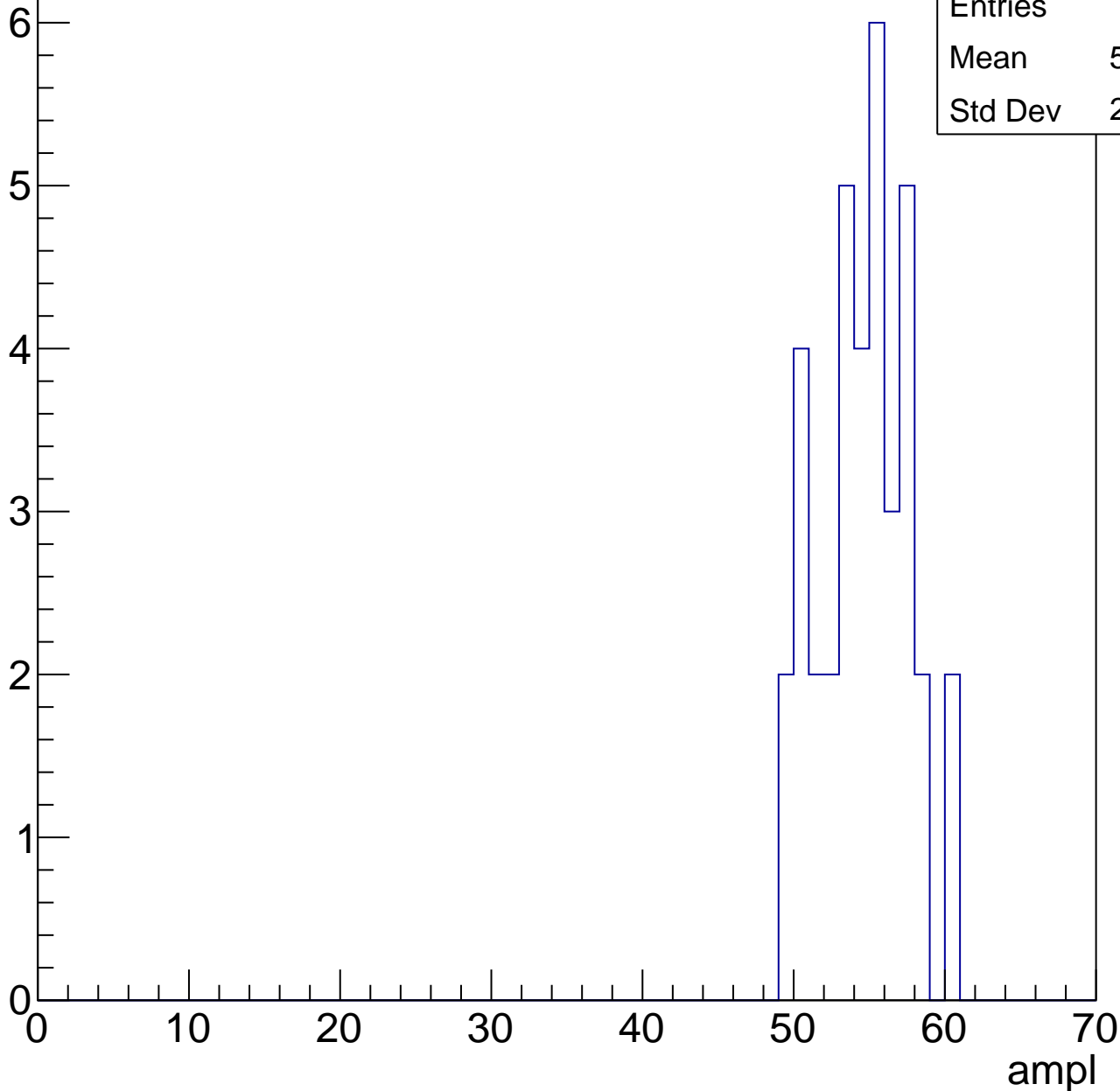


# B1L003S, U26-ch84, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

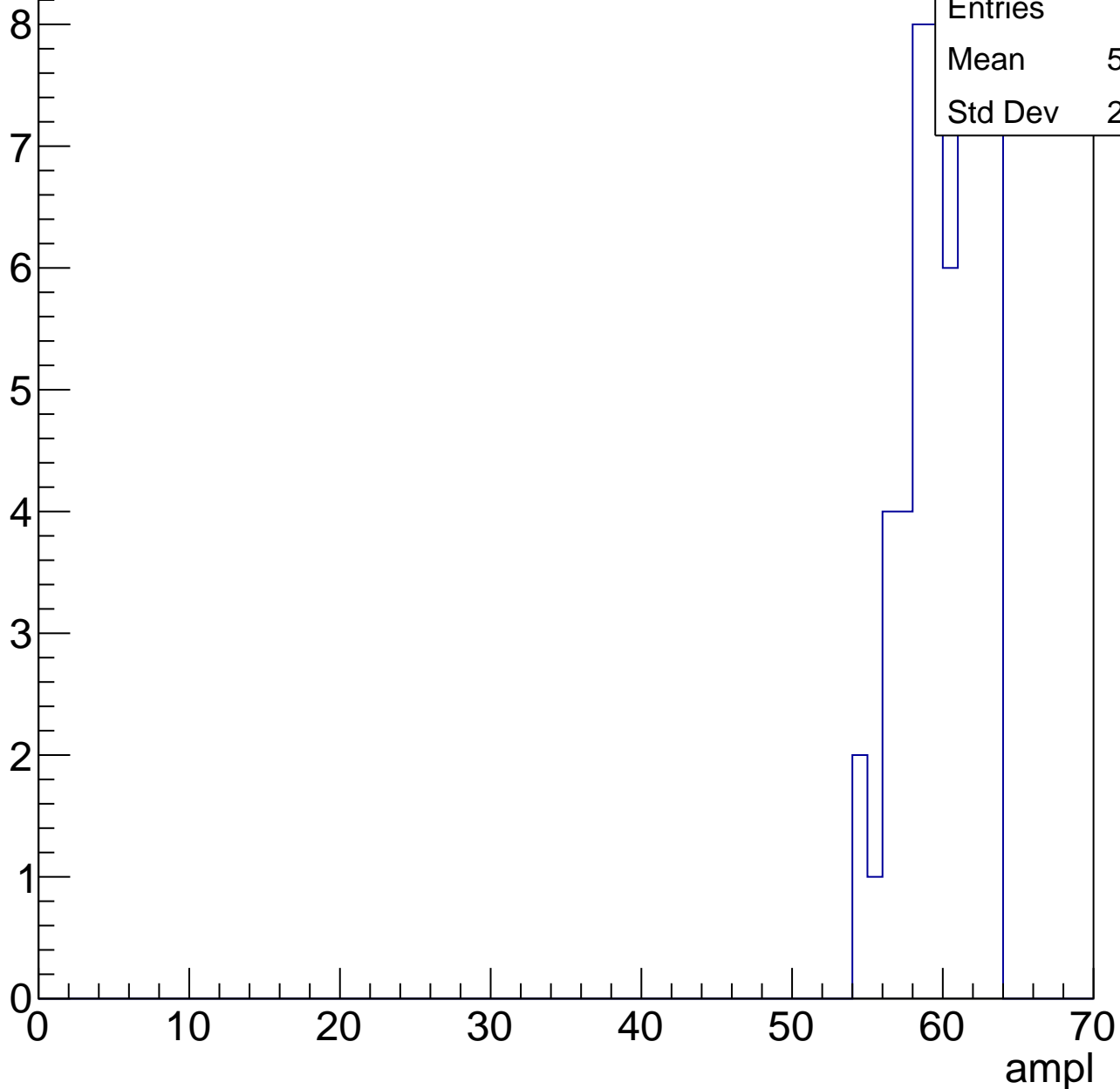
Entries	37
Mean	54.16
Std Dev	2.899



# B1L003S, U26-ch84, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U26-ch84, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	10
Mean	54.8
Std Dev	18.32

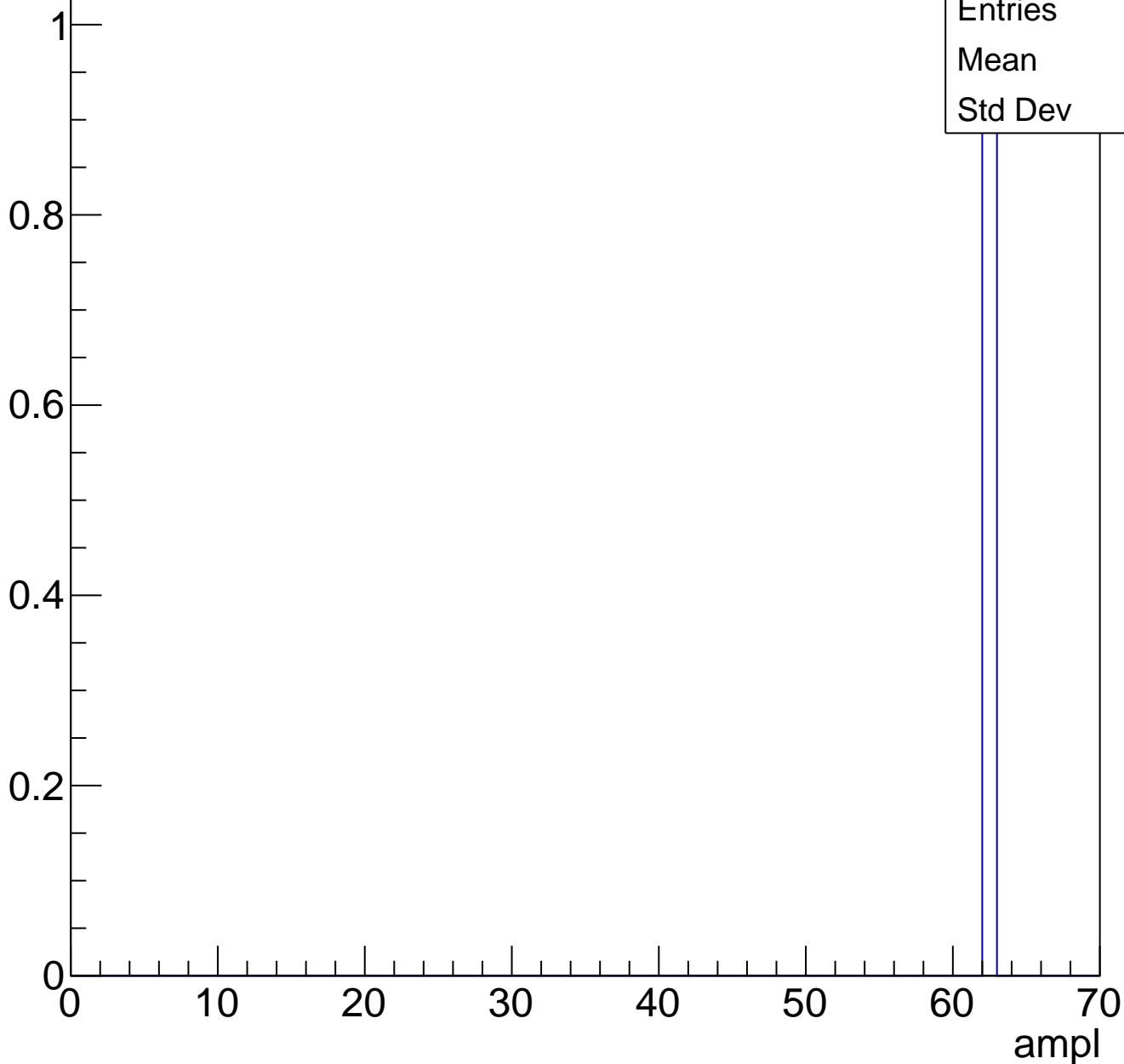
ampl



# B1L003S, U26-ch84, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	62
Std Dev	0

# B1L003S, U26-ch85, adc0

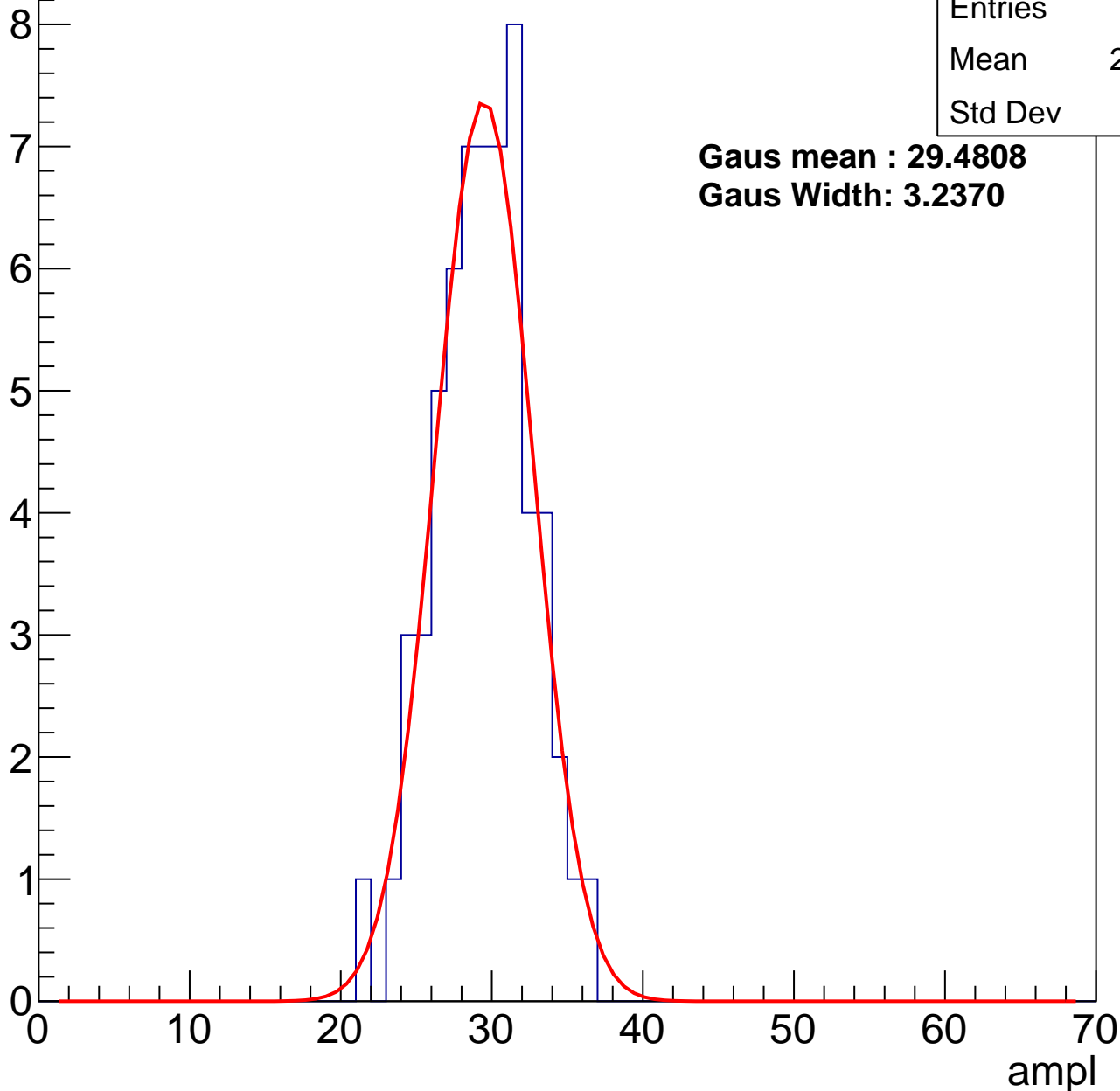
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	28.98
Std Dev	3.09

**Gaus mean : 29.4808**

**Gaus Width: 3.2370**



# B1L003S, U26-ch85, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	87
Mean	36.78
Std Dev	3.449

**Gaus mean : 37.4544**

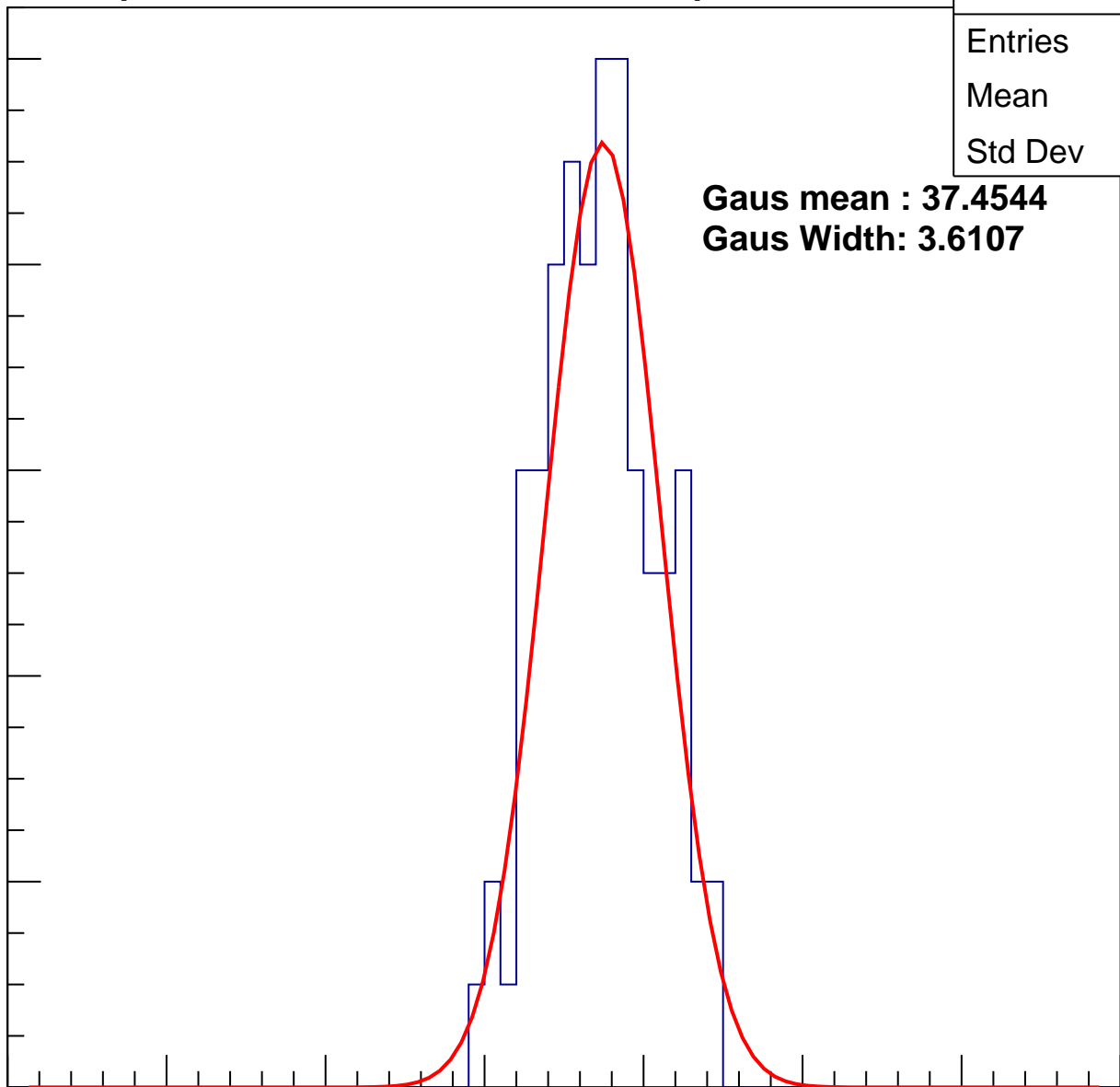
**Gaus Width: 3.6107**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U26-ch85, adc2

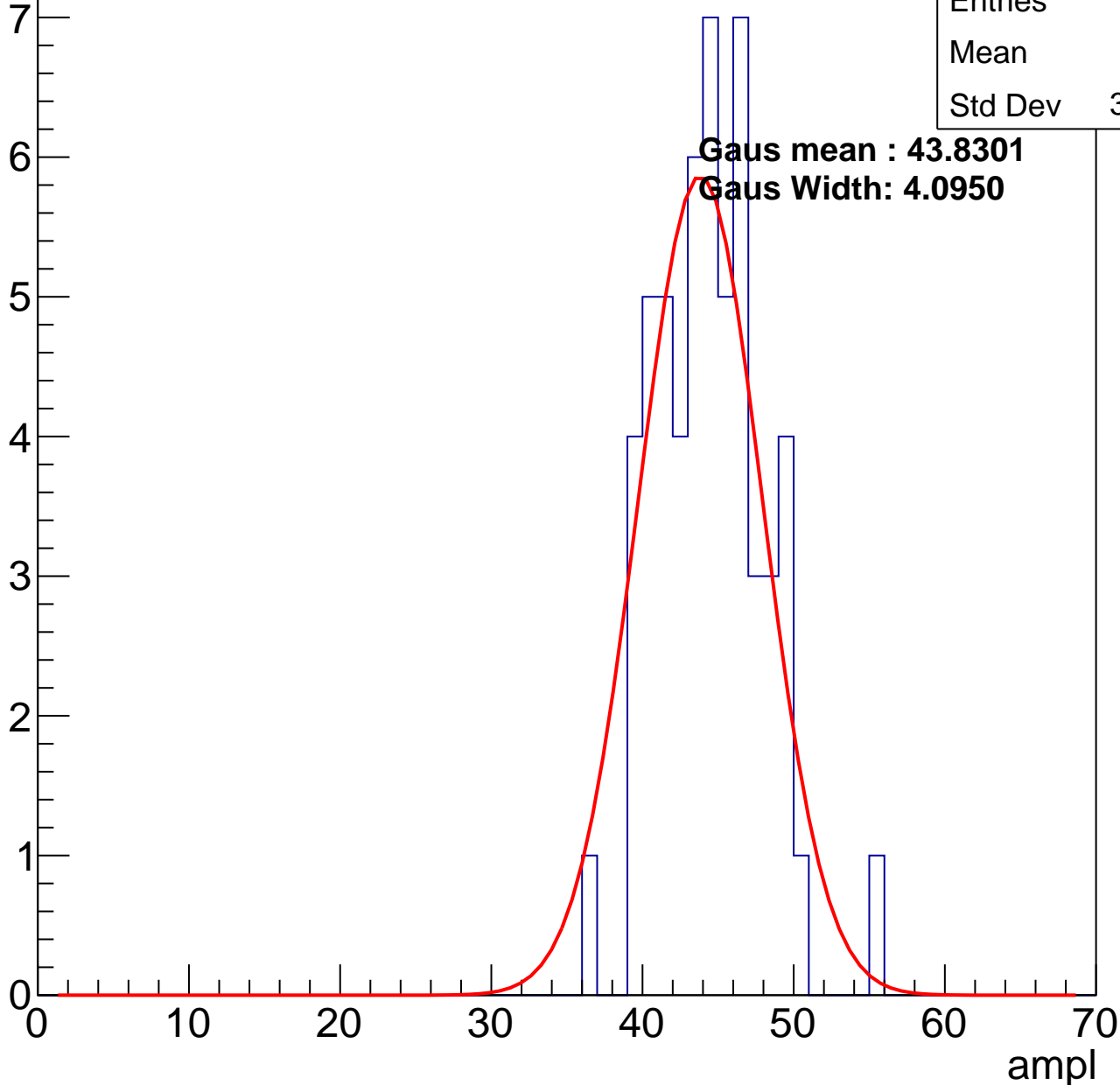
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	44
Std Dev	3.474

**Gaus mean : 43.8301**

**Gaus Width: 4.0950**

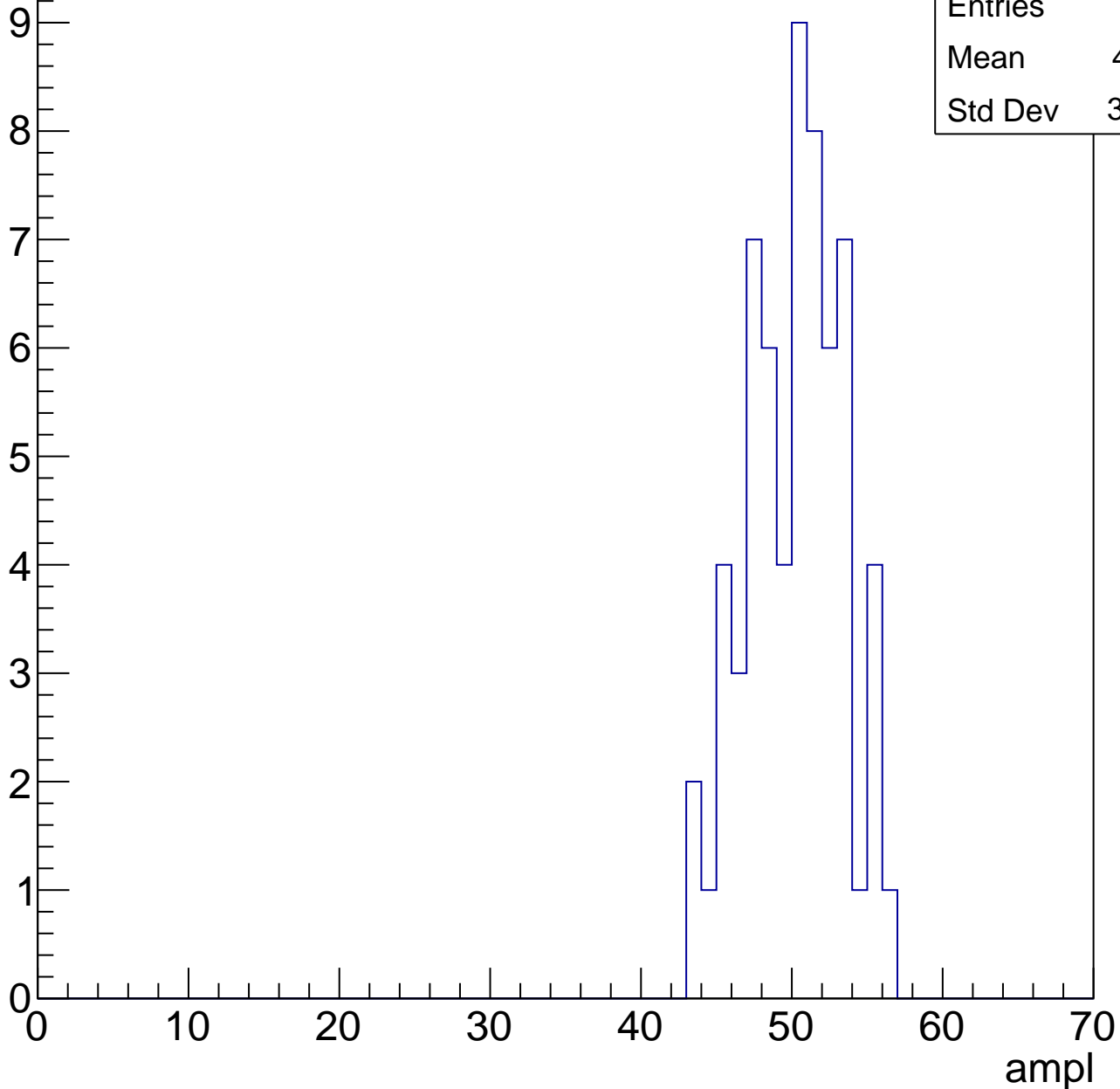


# B1L003S, U26-ch85, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	49.71
Std Dev	3.124

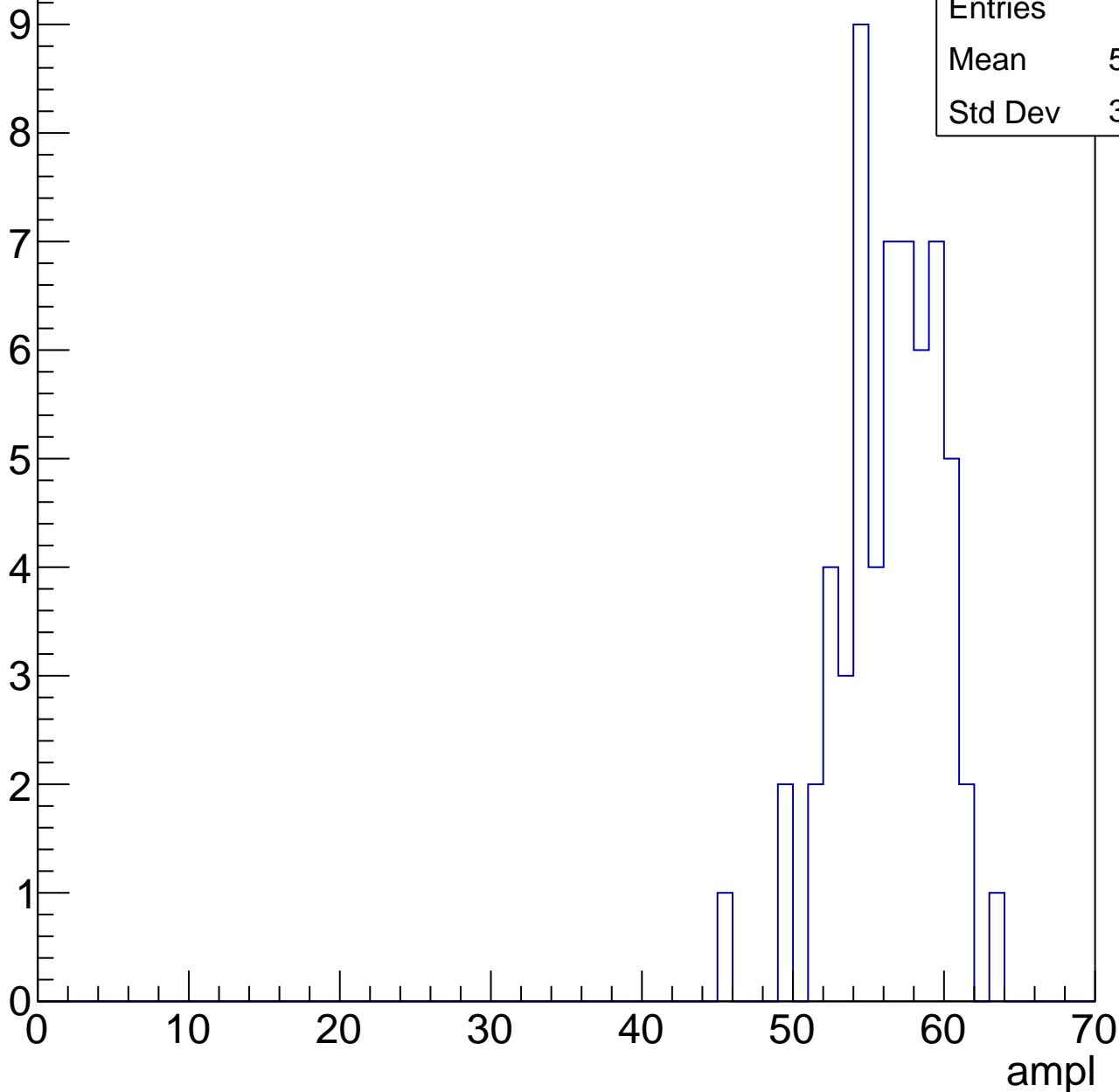


# B1L003S, U26-ch85, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	55.92
Std Dev	3.348



# B1L003S, U26-ch85, adc5

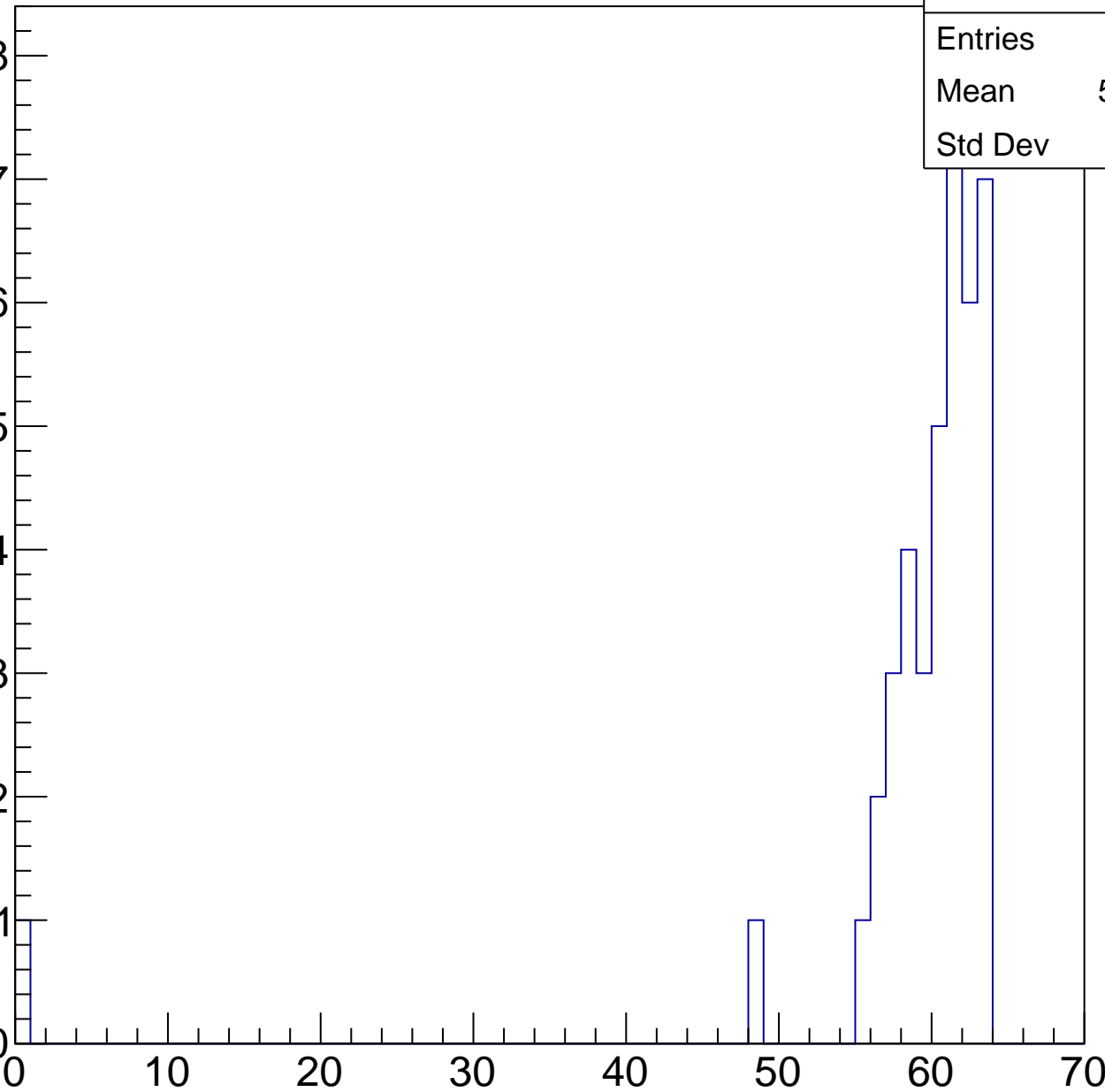
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	41
Mean	58.44
Std Dev	9.68

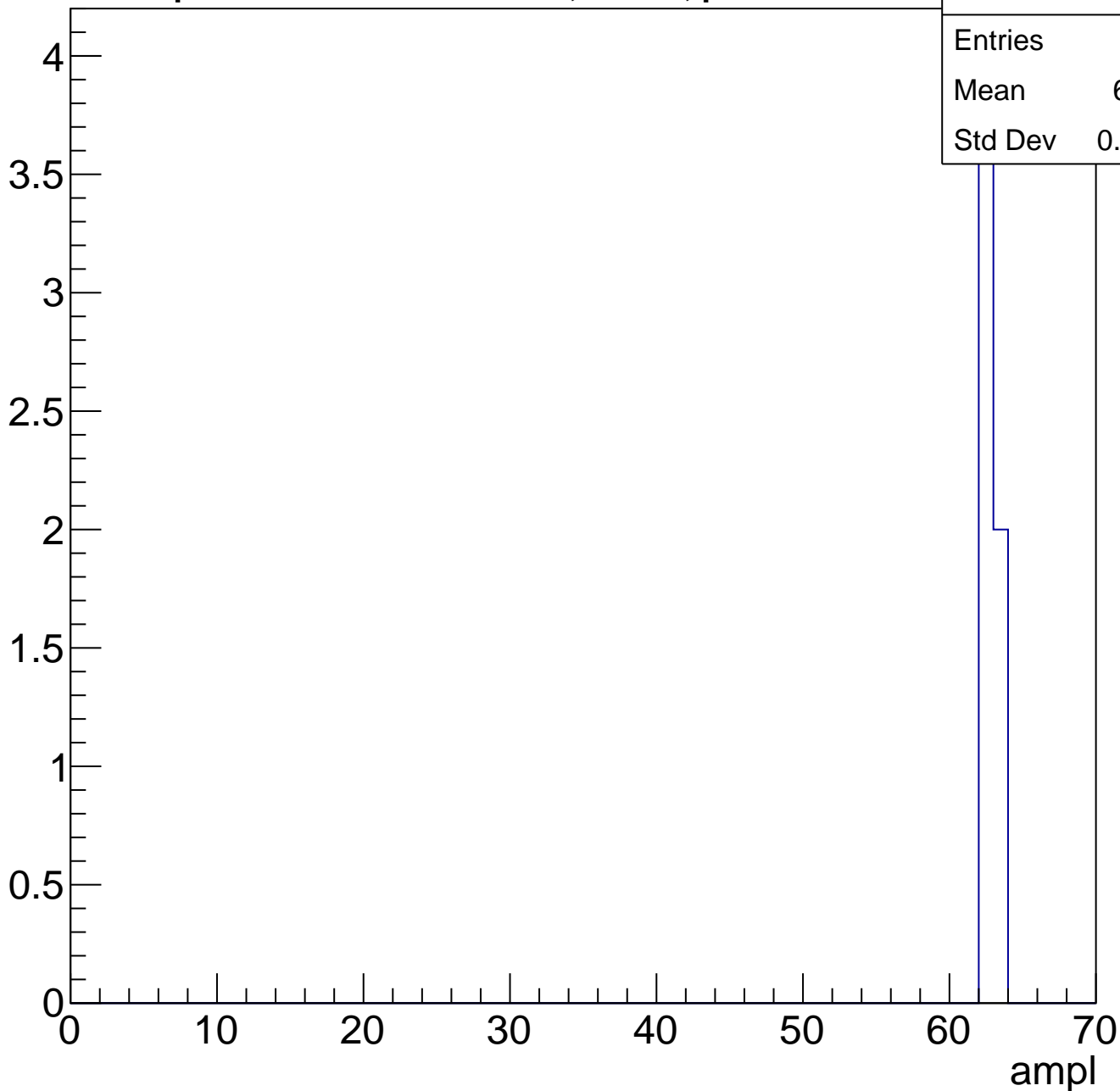
ampl



# B1L003S, U26-ch85, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch85, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	20
Std Dev	0

ampl

# B1L003S, U26-ch86, adc0

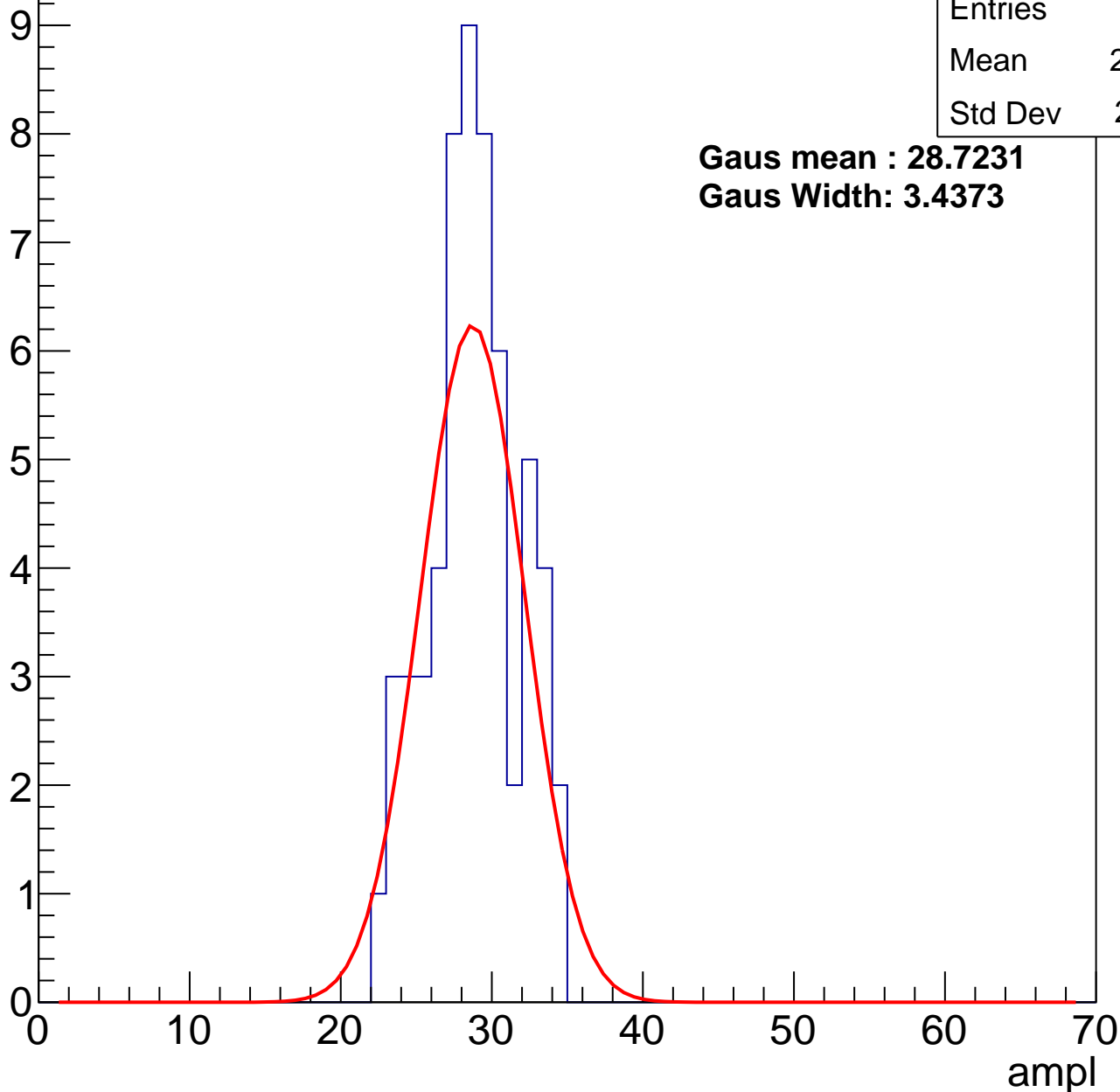
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	28.34
Std Dev	2.951

**Gaus mean : 28.7231**

**Gaus Width: 3.4373**



# B1L003S, U26-ch86, adc1

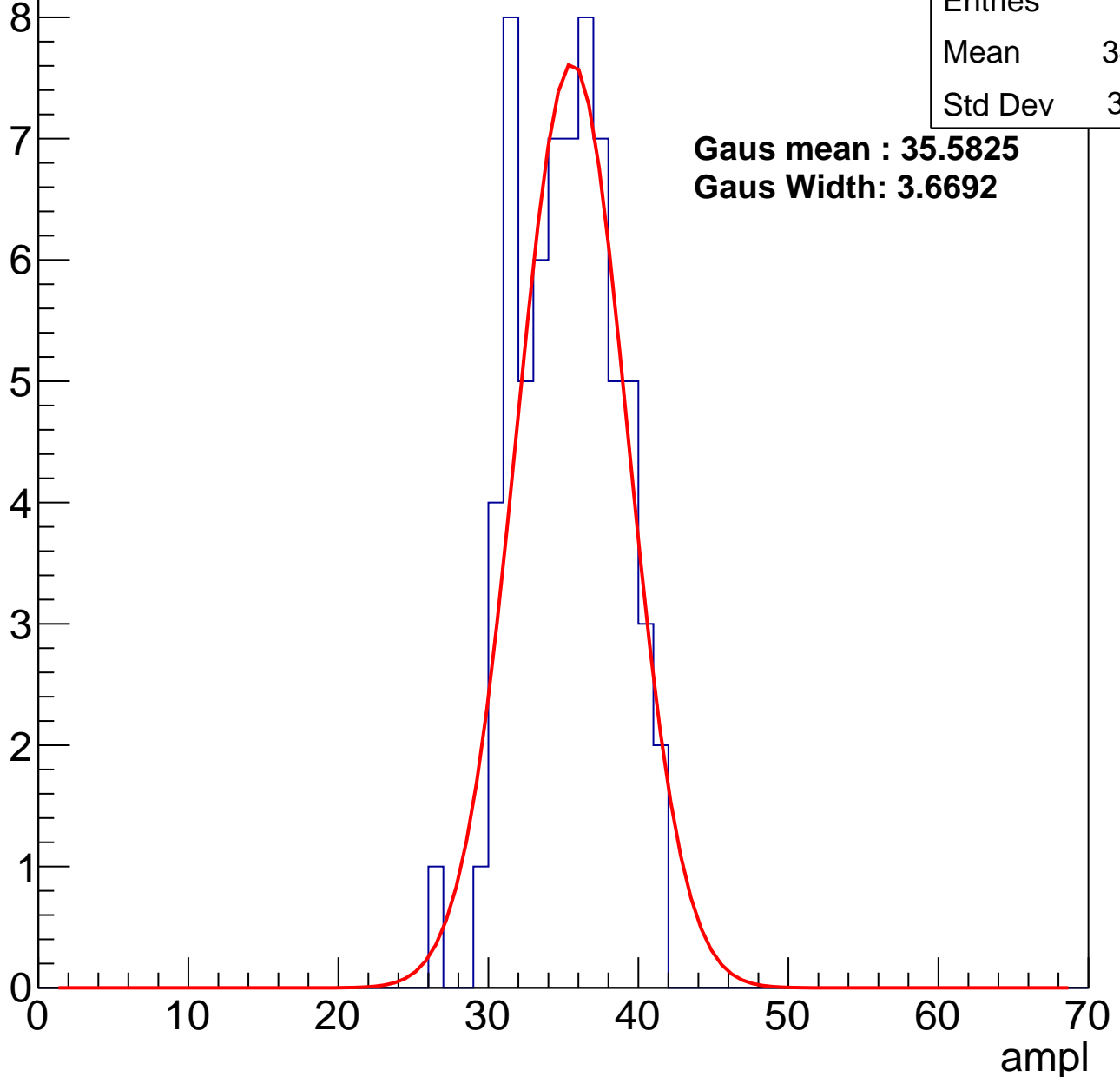
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	34.75
Std Dev	3.241

**Gaus mean : 35.5825**

**Gaus Width: 3.6692**



# B1L003S, U26-ch86, adc2

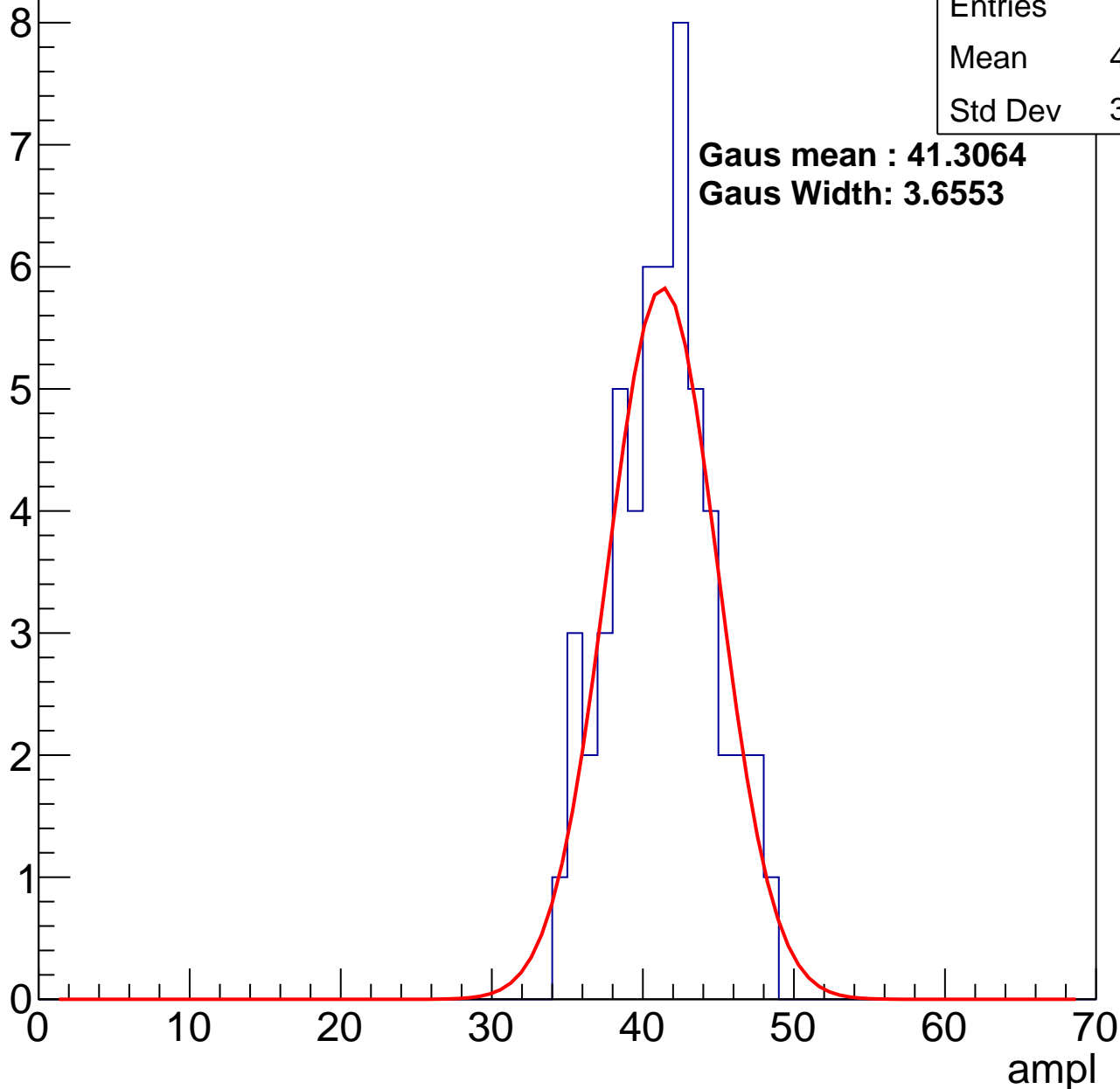
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	54
Mean	40.83
Std Dev	3.298

**Gaus mean : 41.3064**

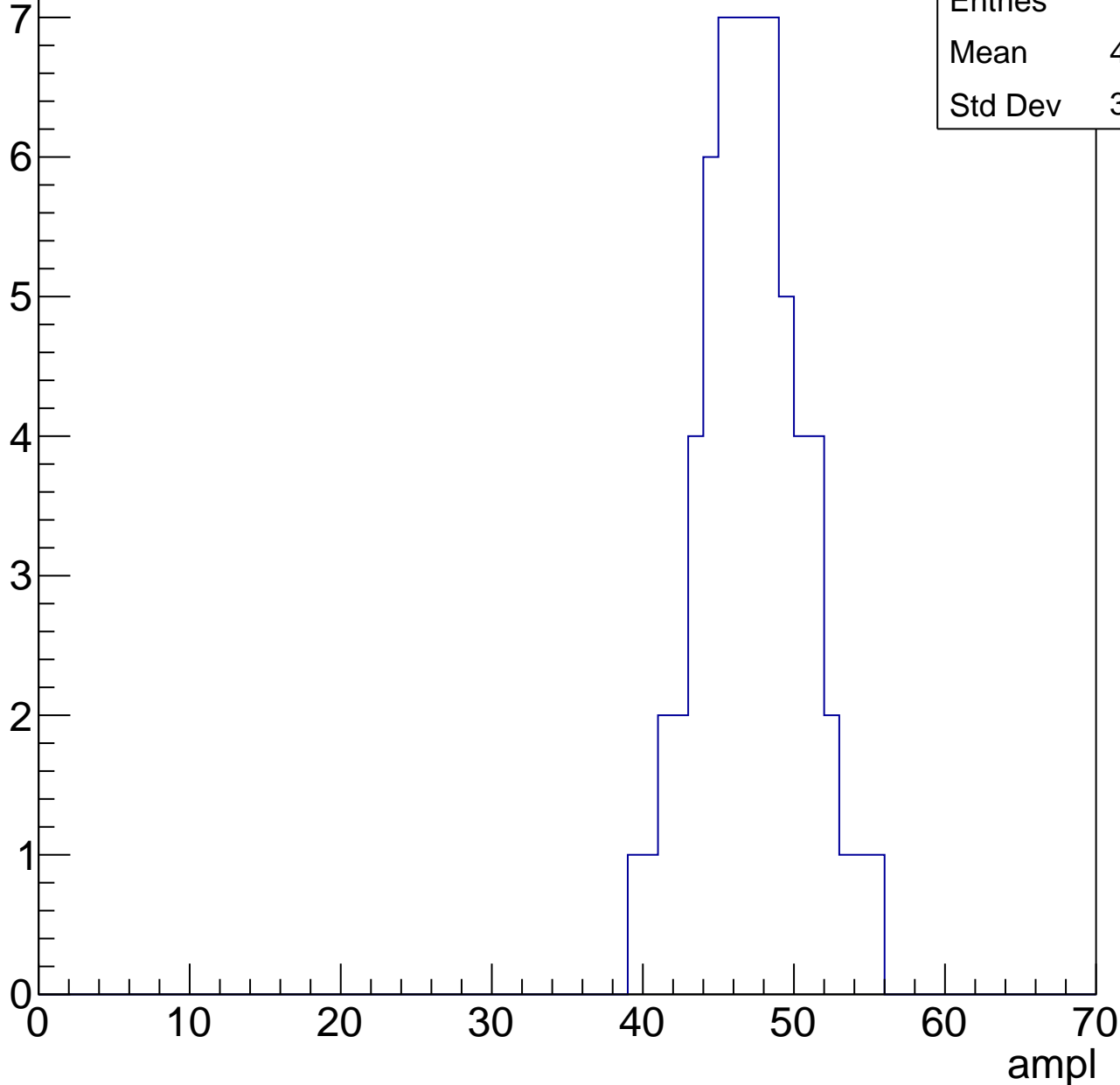
**Gaus Width: 3.6553**



# B1L003S, U26-ch86, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

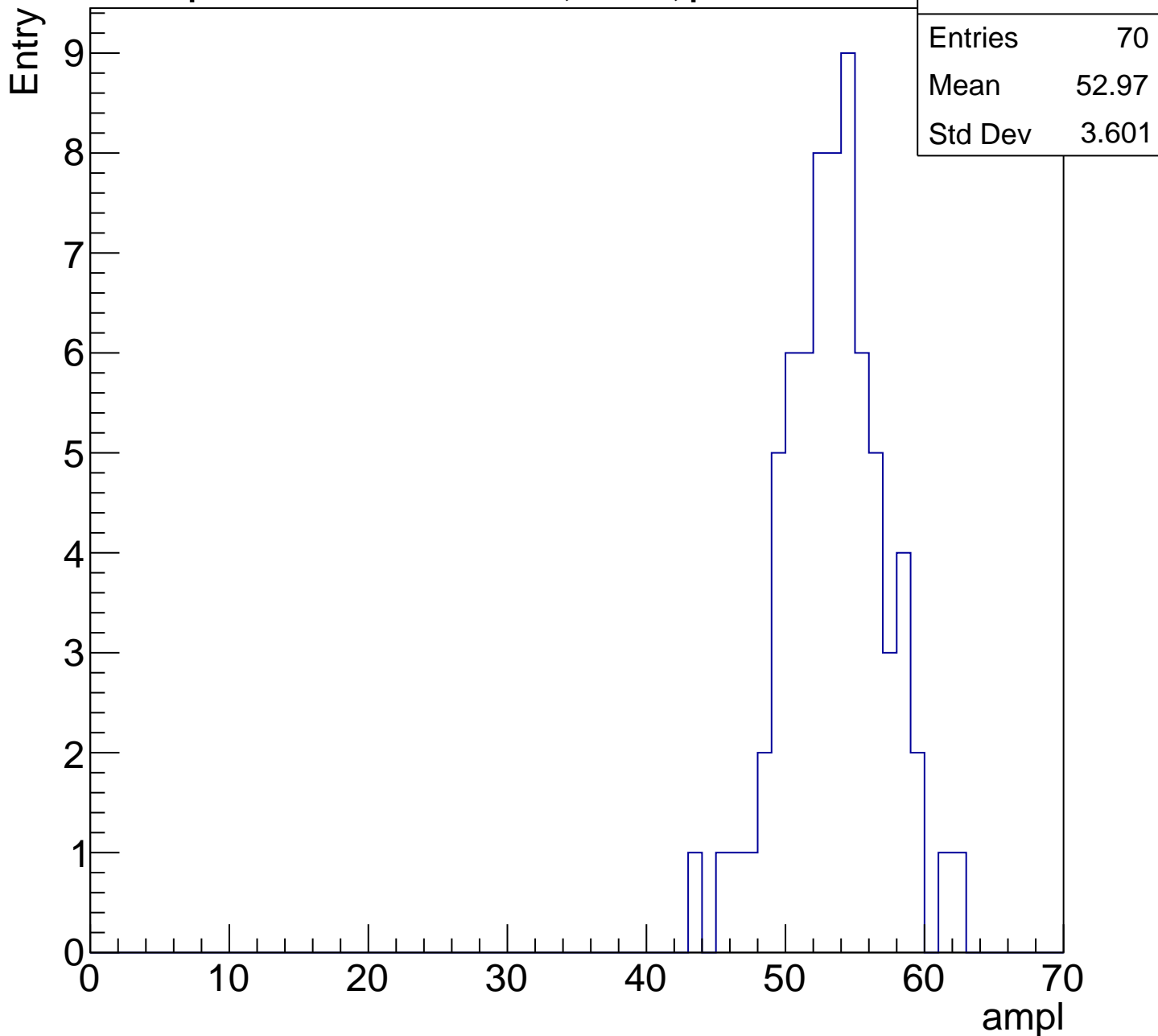
Entry



Entries	62
Mean	46.74
Std Dev	3.384

# B1L003S, U26-ch86, adc4

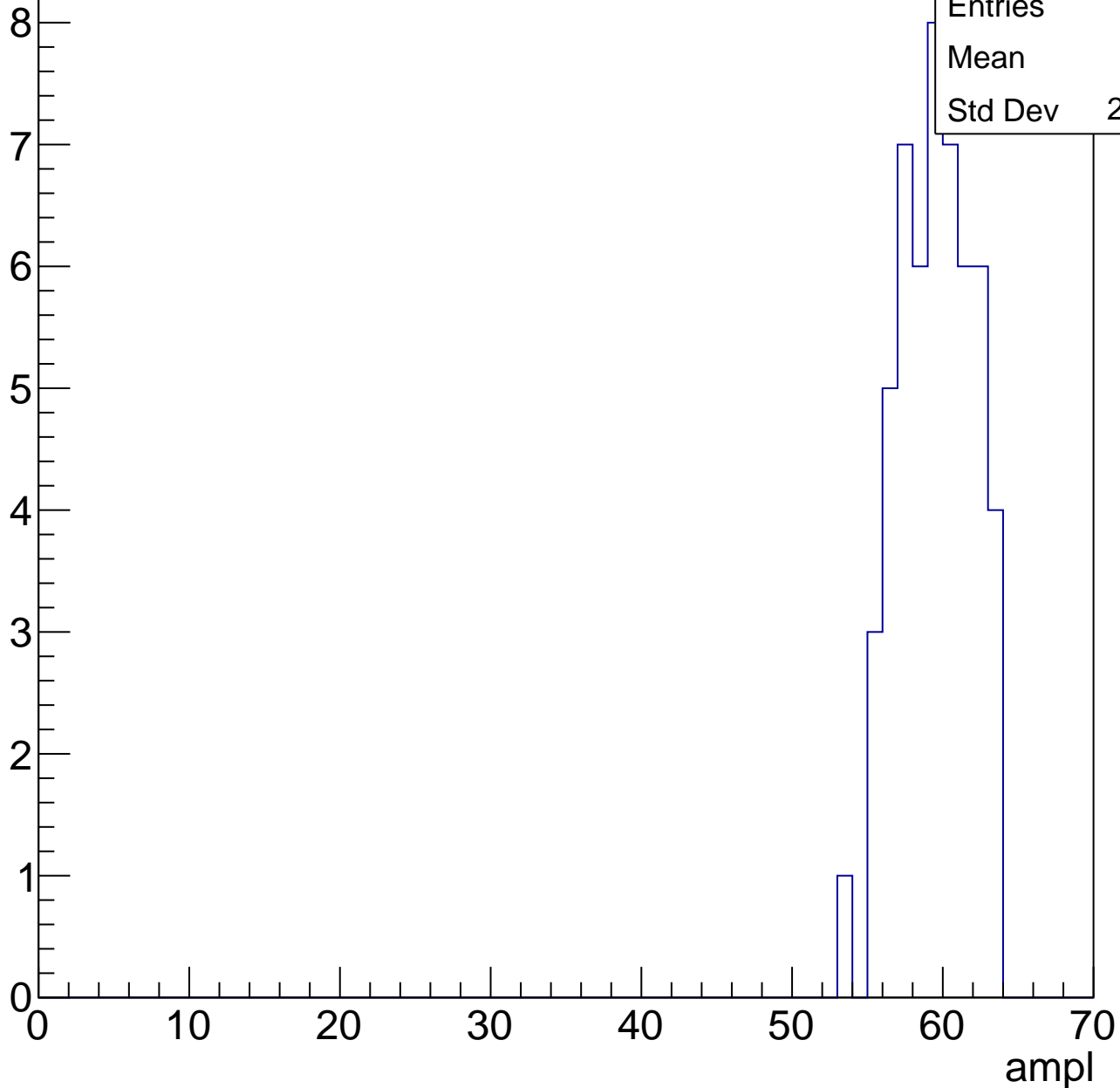
calib\_packv5\_042523\_0143.root, FC#13, port D2



# B1L003S, U26-ch86, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

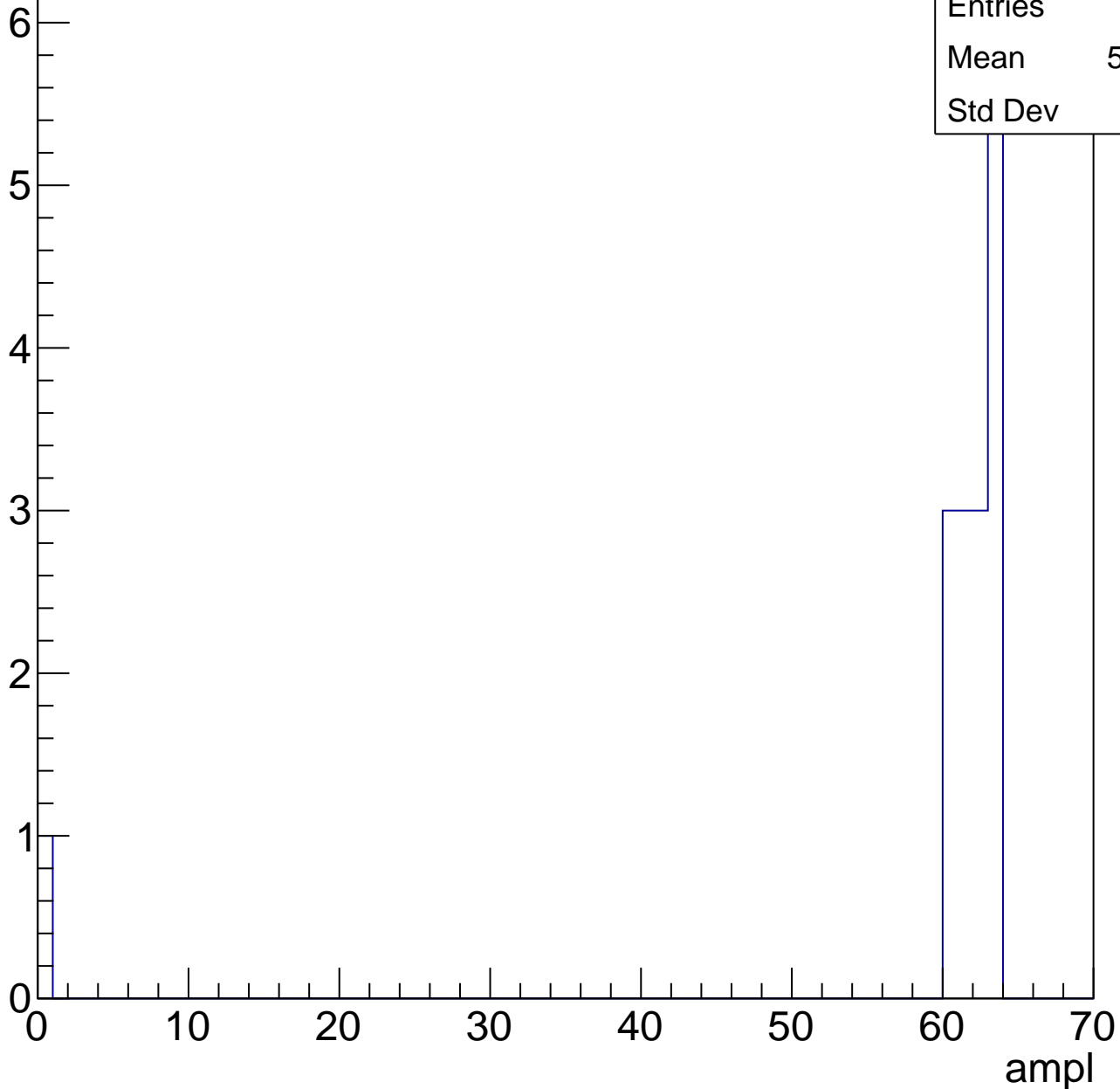


# B1L003S, U26-ch86, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	16
Mean	57.94
Std Dev	15





# B1L003S, U26-ch86, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	11
Std Dev	11

# B1L003S, U26-ch87, adc0

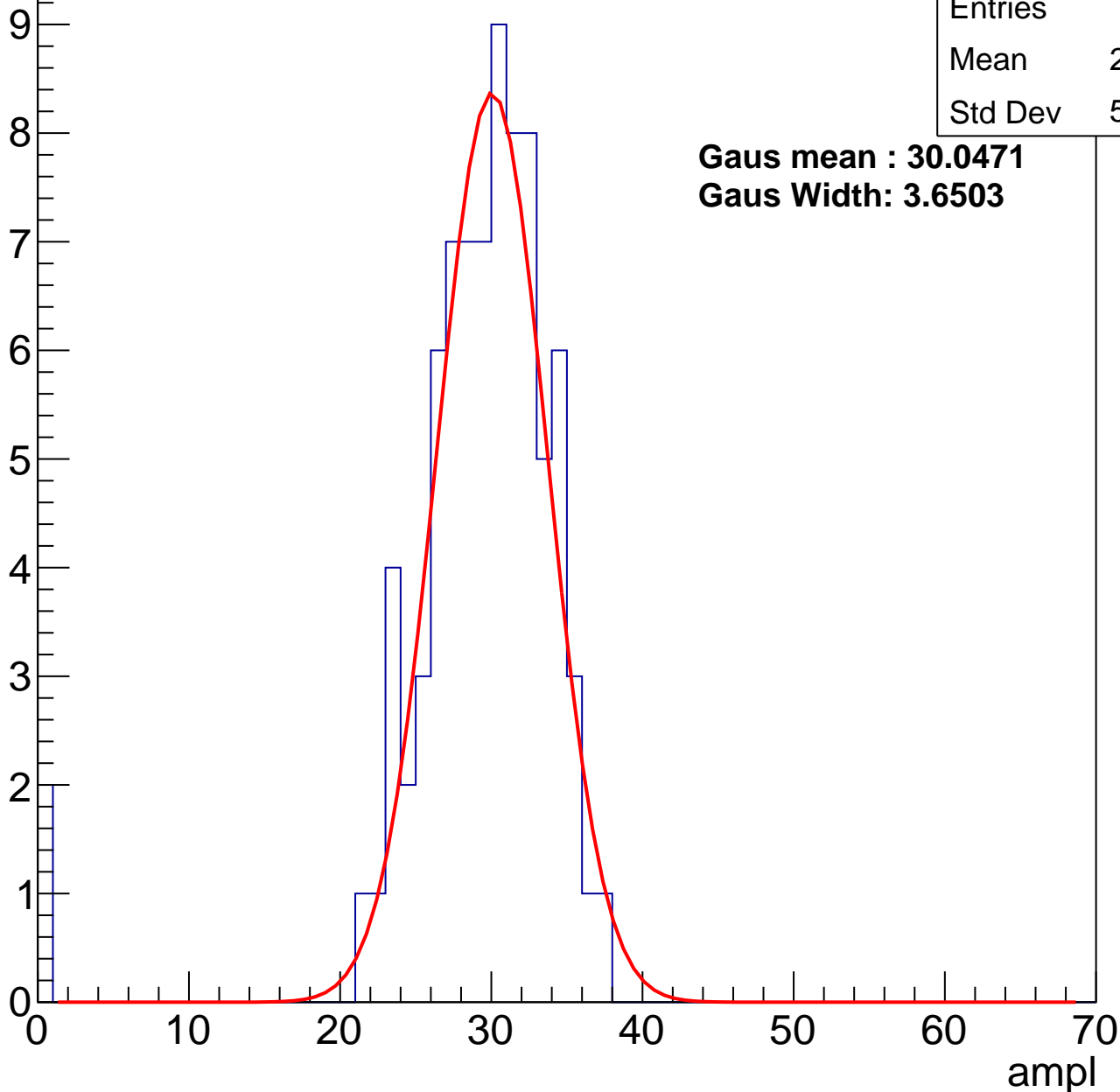
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	81
Mean	28.68
Std Dev	5.754

**Gaus mean : 30.0471**

**Gaus Width: 3.6503**



# B1L003S, U26-ch87, adc1

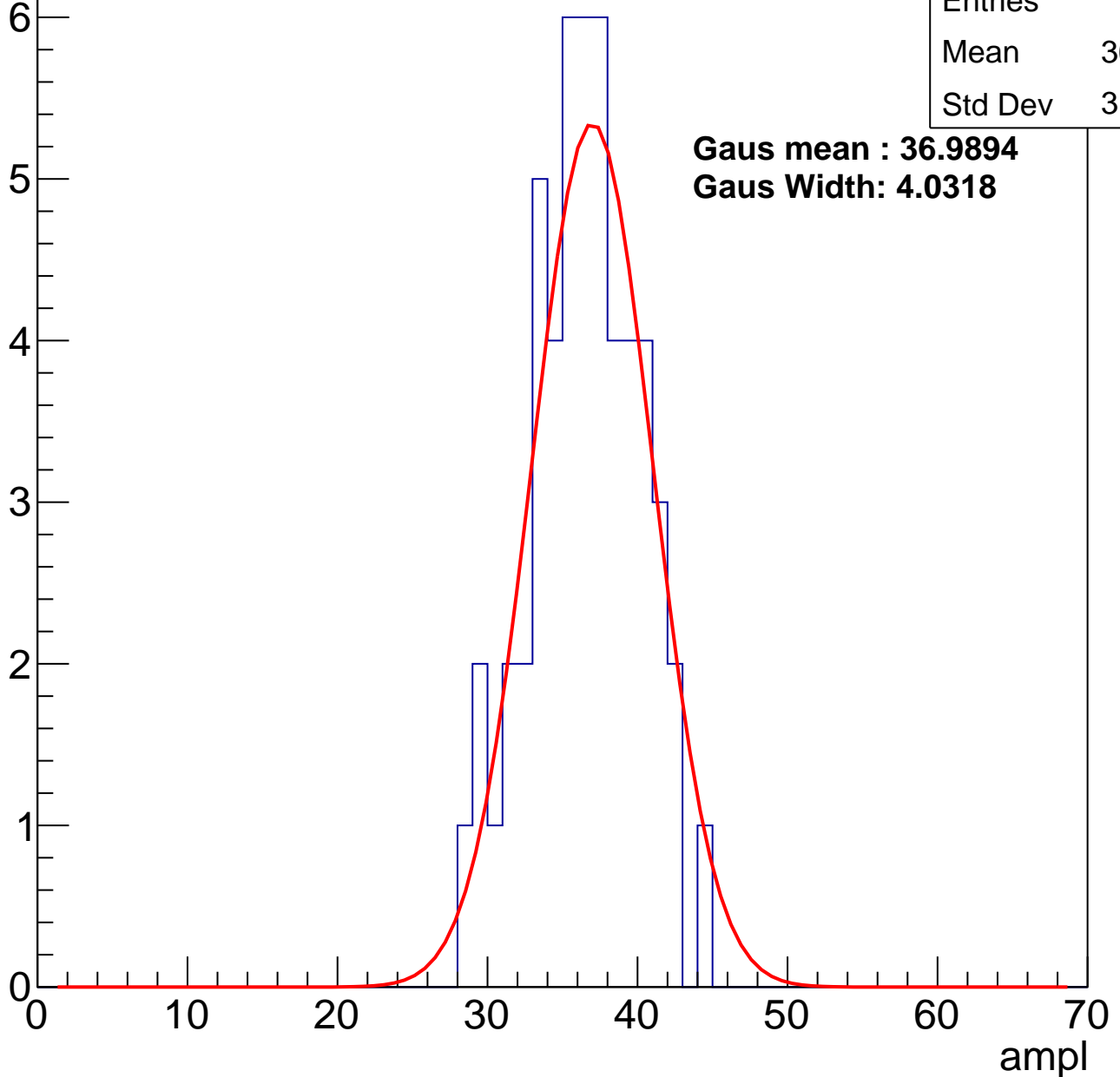
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	36.04
Std Dev	3.582

**Gaus mean : 36.9894**

**Gaus Width: 4.0318**



# B1L003S, U26-ch87, adc2

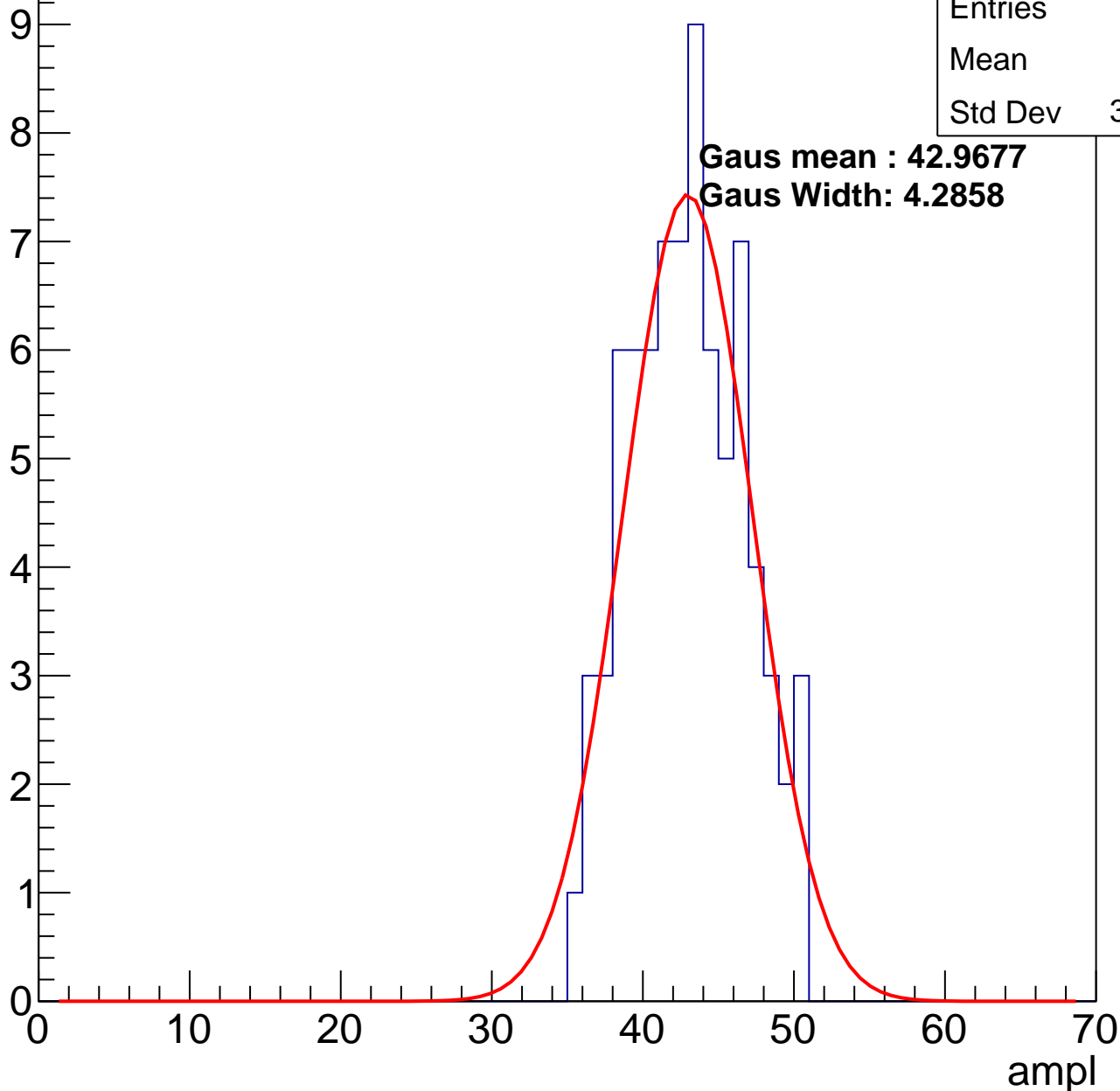
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	78
Mean	42.5
Std Dev	3.724

**Gaus mean : 42.9677**

**Gaus Width: 4.2858**

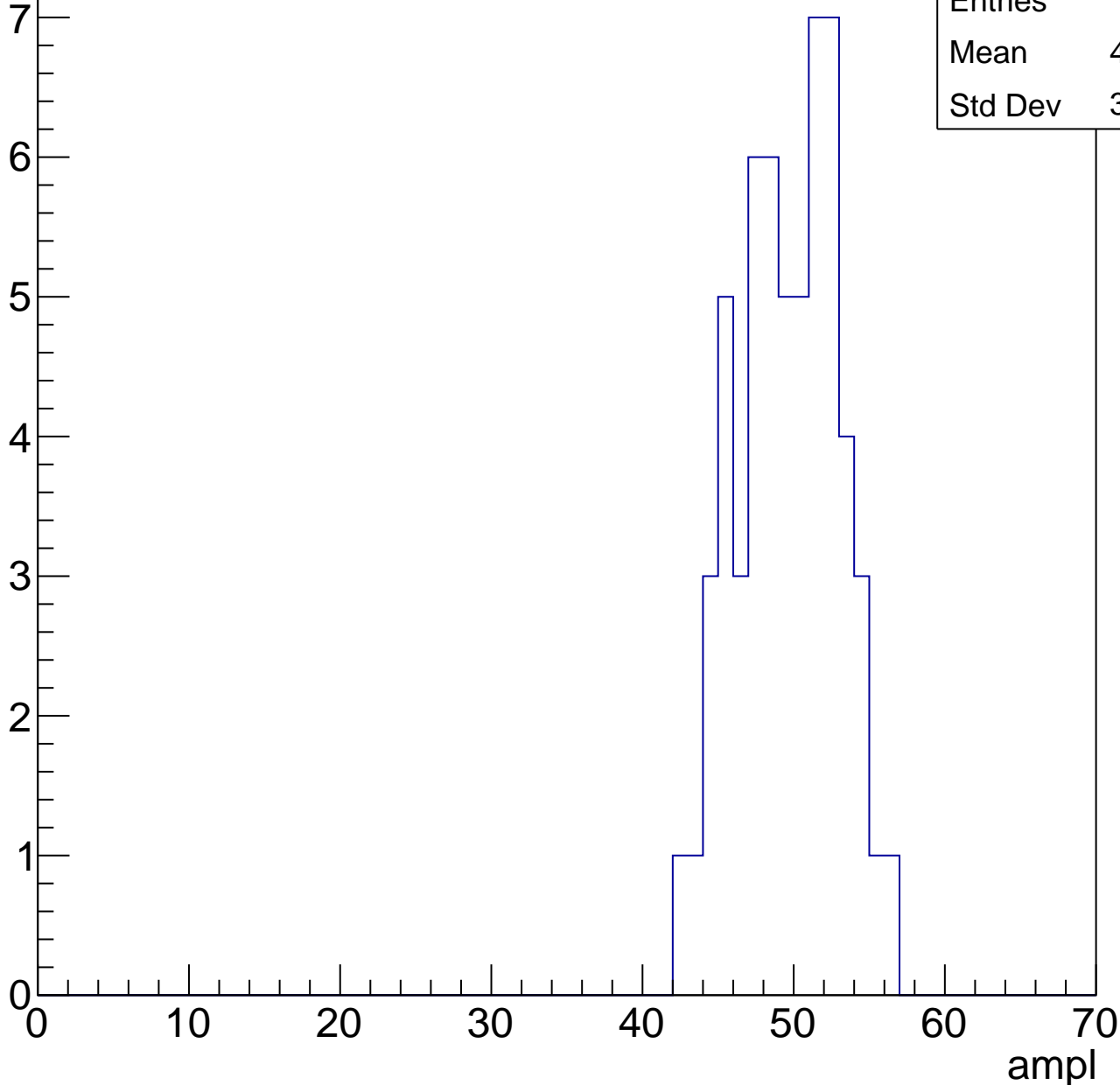


# B1L003S, U26-ch87, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	49.16
Std Dev	3.258

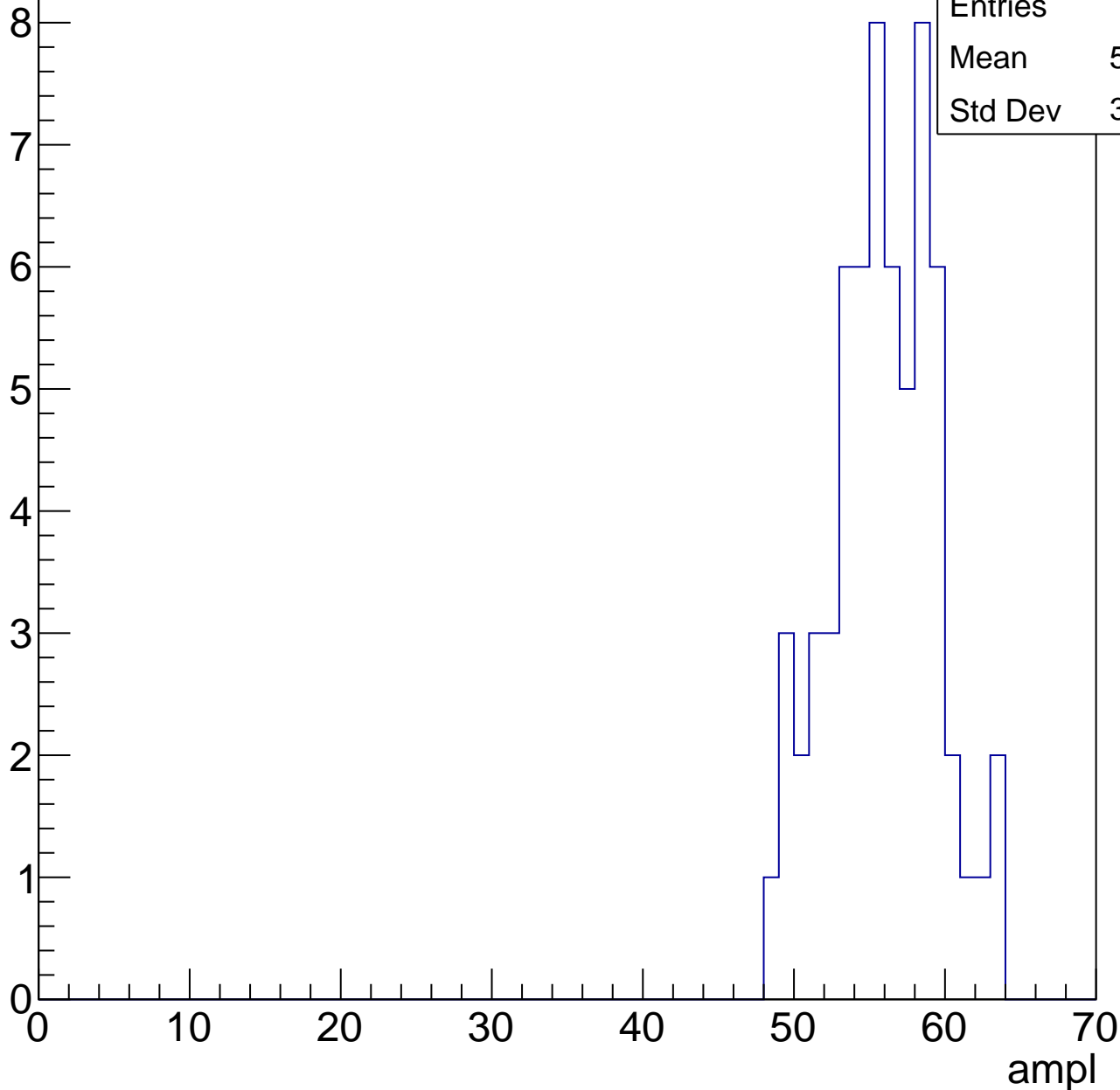


# B1L003S, U26-ch87, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	55.46
Std Dev	3.463

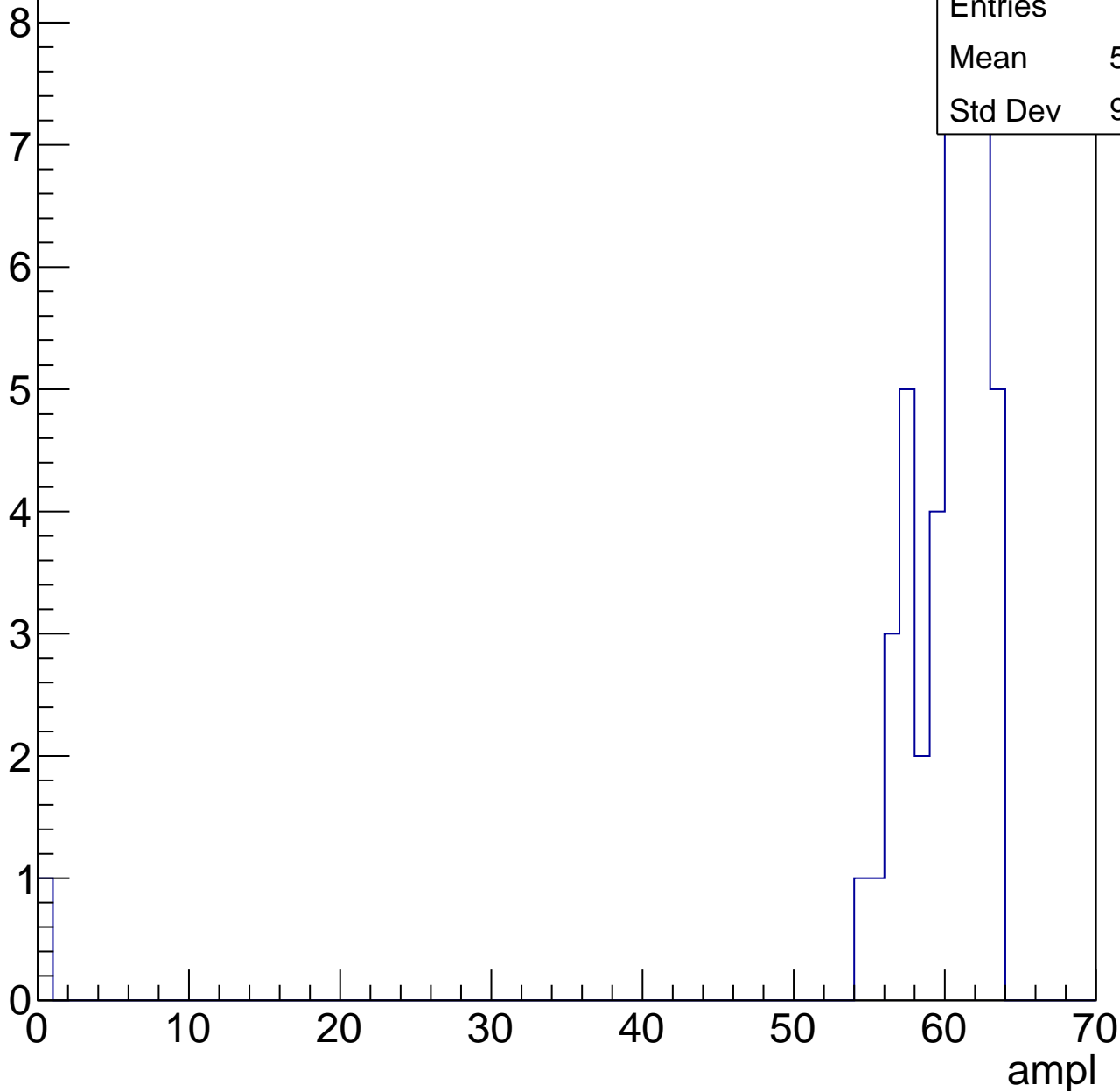


# B1L003S, U26-ch87, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	46
Mean	58.54
Std Dev	9.033



# B1L003S, U26-ch87, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch87, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L003S, U26-ch88, adc0

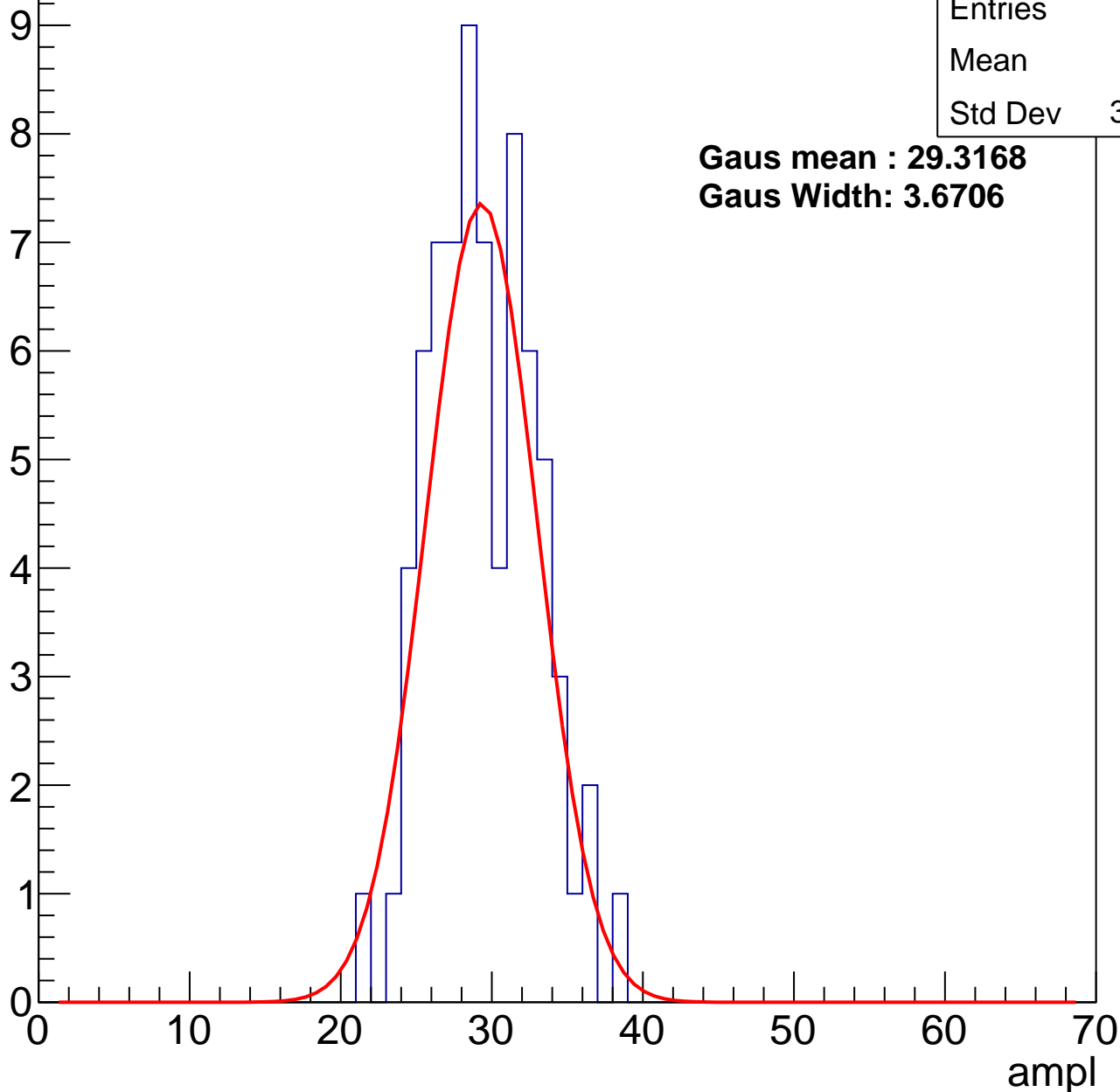
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	72
Mean	29
Std Dev	3.448

**Gaus mean : 29.3168**

**Gaus Width: 3.6706**



# B1L003S, U26-ch88, adc1

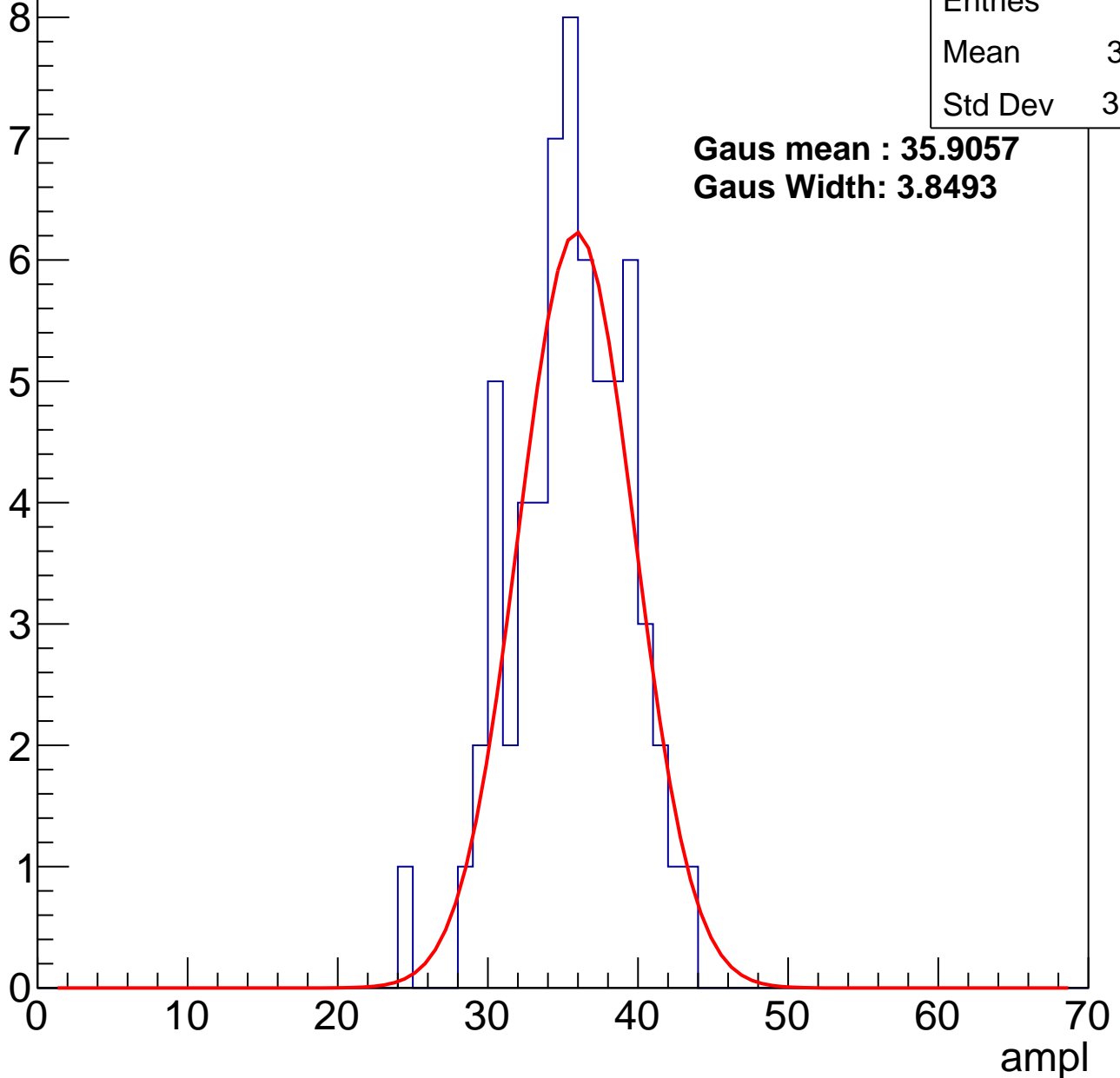
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	35.11
Std Dev	3.746

**Gaus mean : 35.9057**

**Gaus Width: 3.8493**



# B1L003S, U26-ch88, adc2

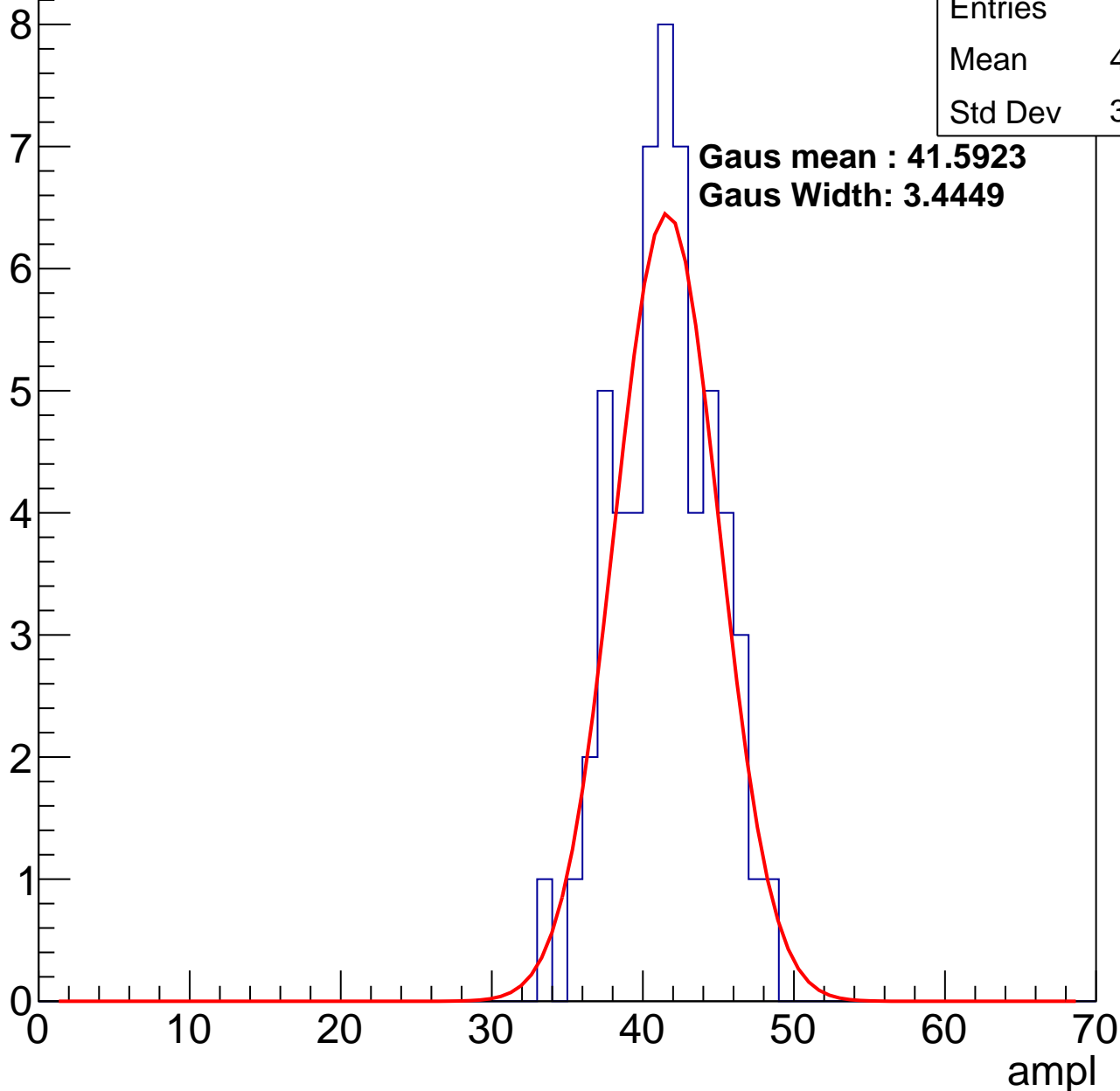
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	41.05
Std Dev	3.192

**Gaus mean : 41.5923**

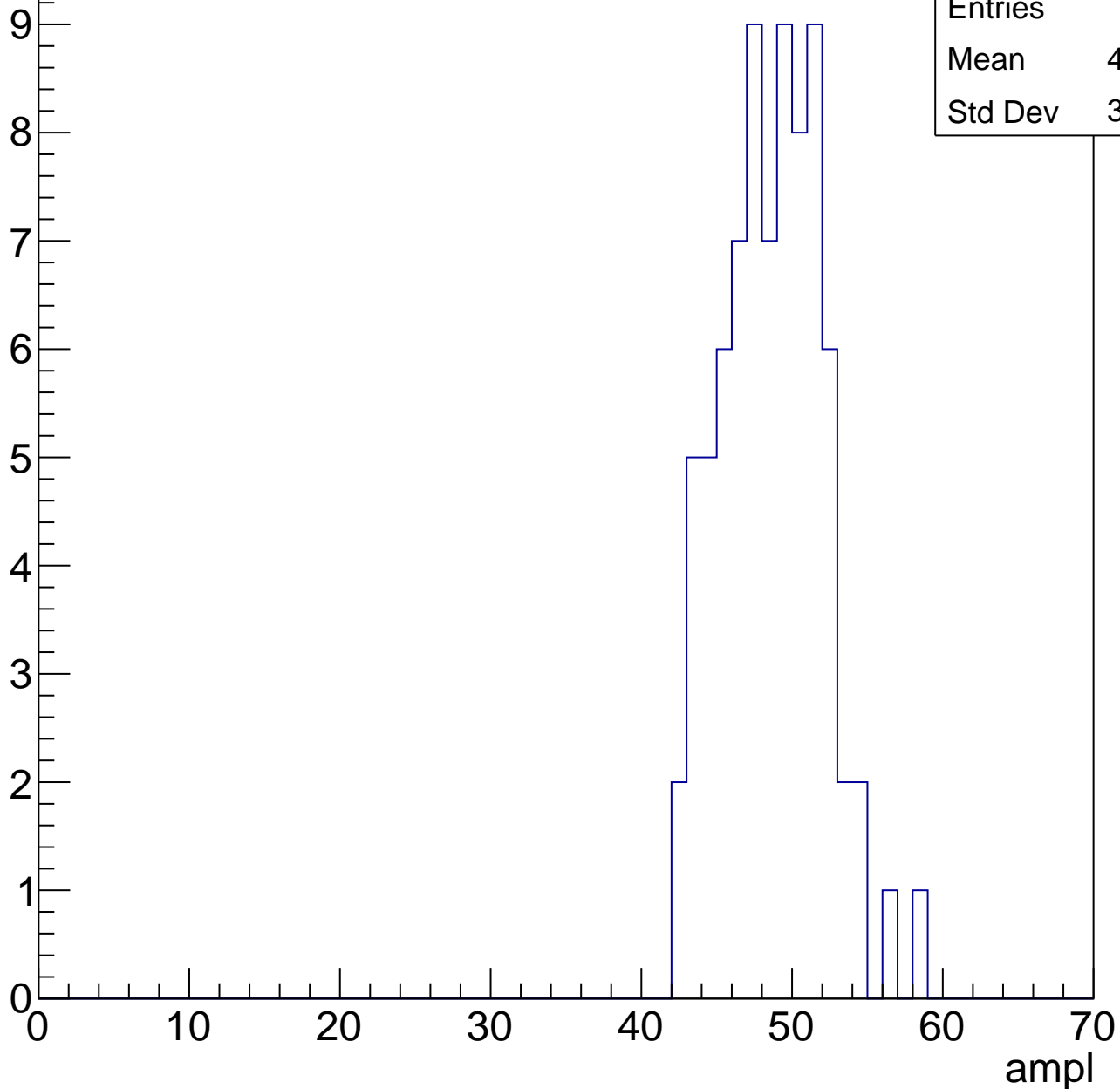
**Gaus Width: 3.4449**



# B1L003S, U26-ch88, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

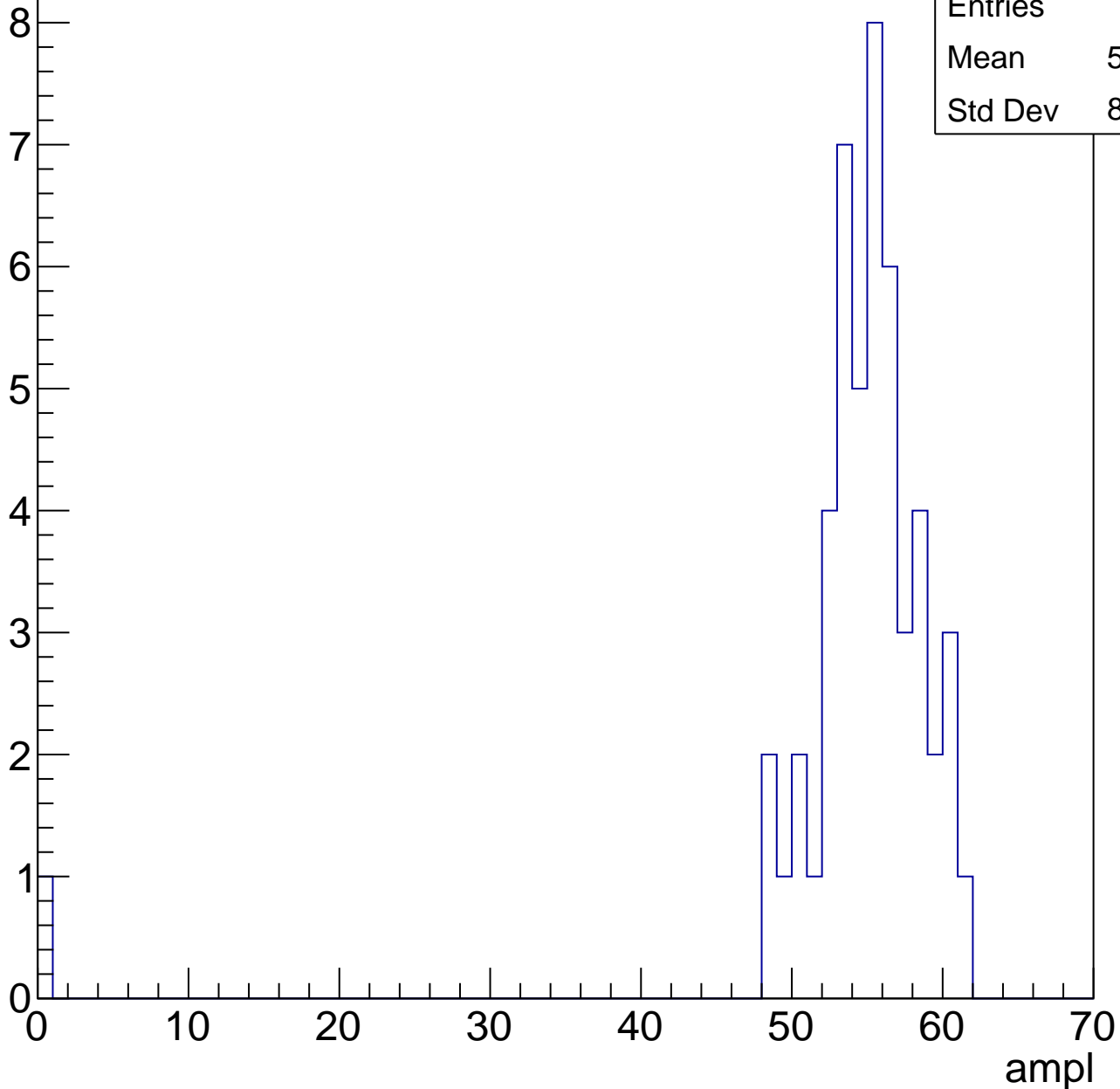


# B1L003S, U26-ch88, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

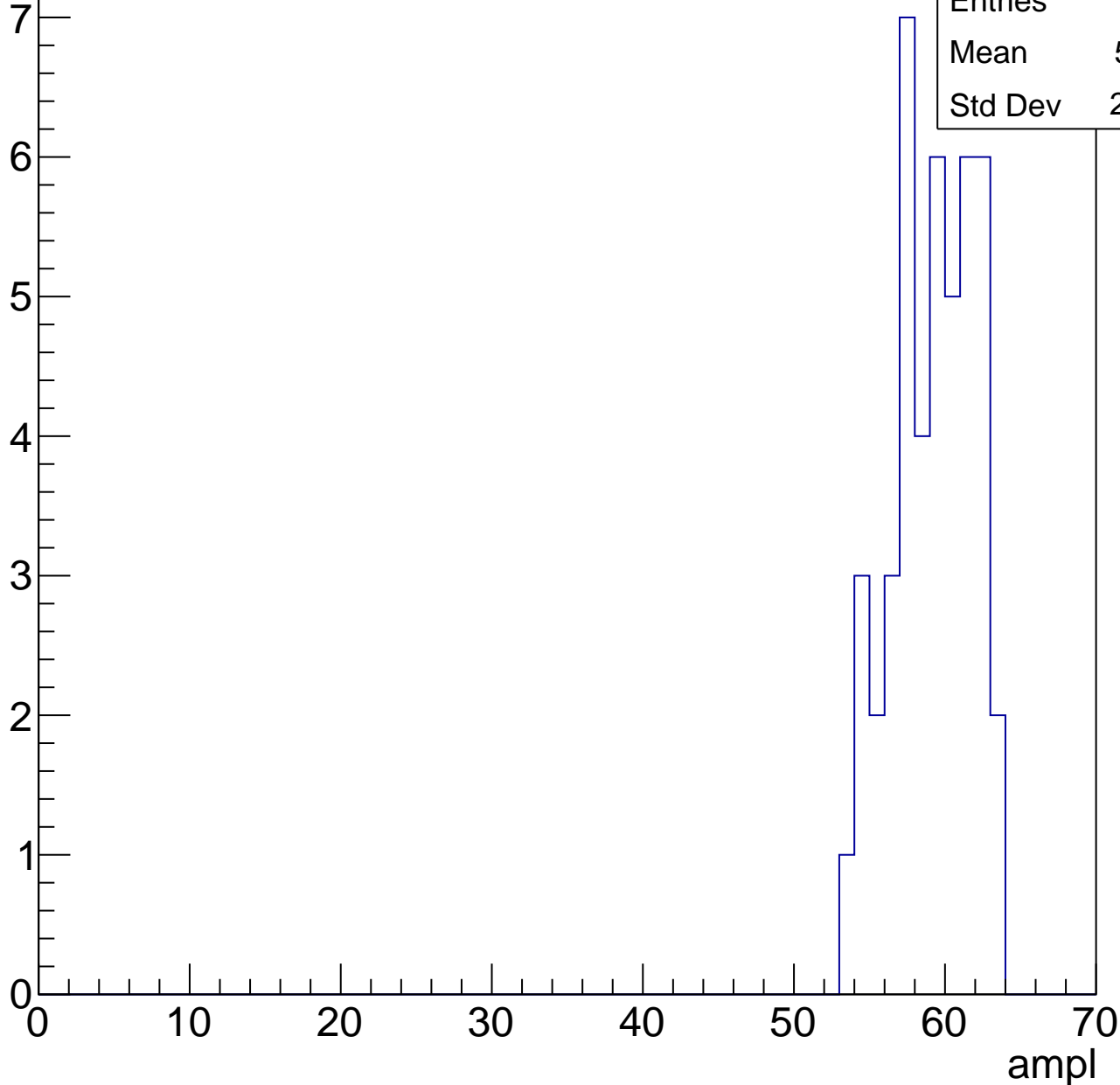
Entries	50
Mean	53.66
Std Dev	8.248



# B1L003S, U26-ch88, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



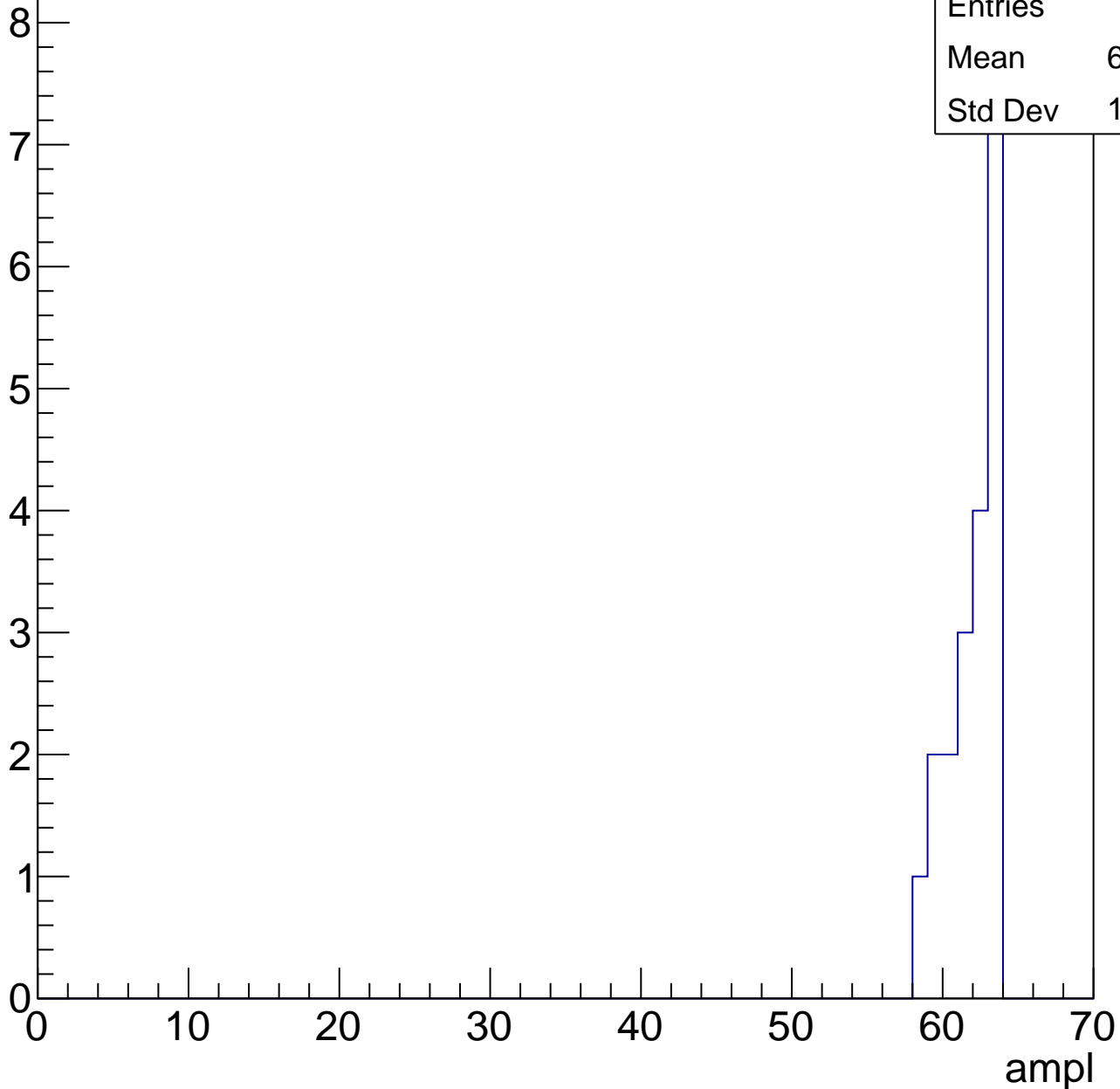
Entries	45
Mean	58.71
Std Dev	2.638

# B1L003S, U26-ch88, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	20
Mean	61.55
Std Dev	1.564





# B1L003S, U26-ch88, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U26-ch89, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	73
Mean	29.51
Std Dev	5.732

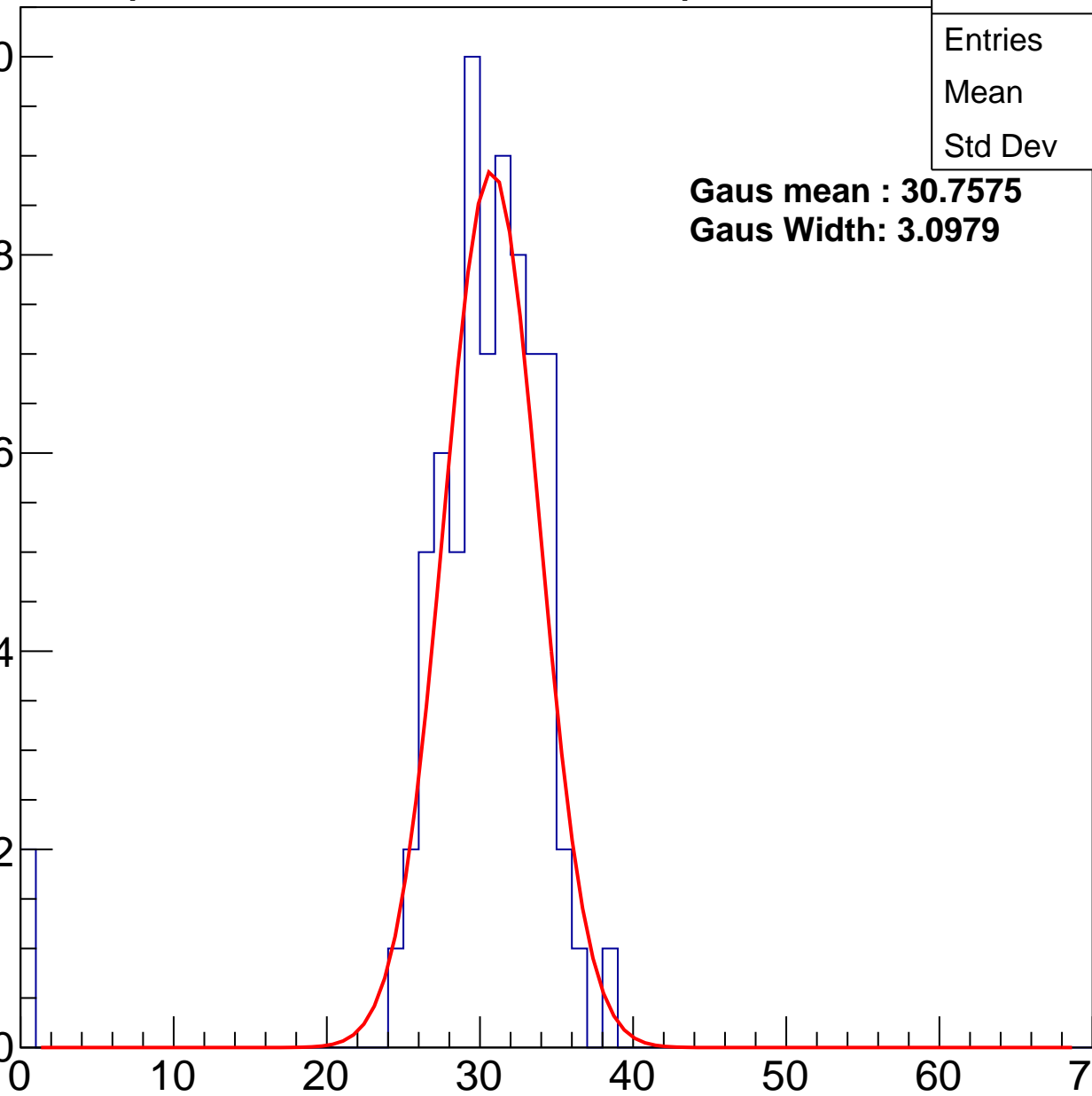
**Gaus mean : 30.7575**

**Gaus Width: 3.0979**

Entry

10  
8  
6  
4  
2  
0

ampl



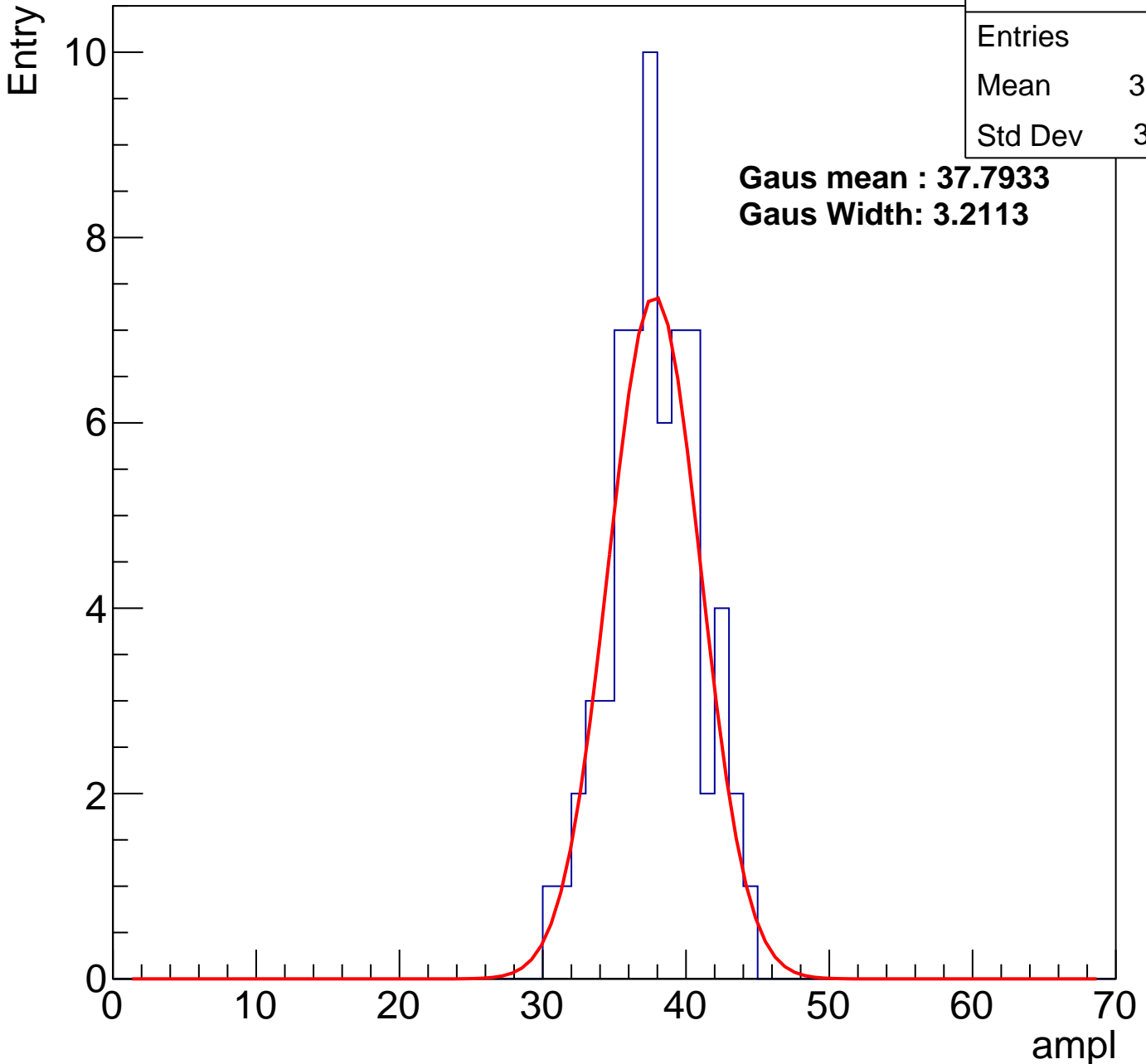
# B1L003S, U26-ch89, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	63
Mean	37.37
Std Dev	3.051

**Gaus mean : 37.7933**

**Gaus Width: 3.2113**



# B1L003S, U26-ch89, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	76
Mean	44.08
Std Dev	3.645

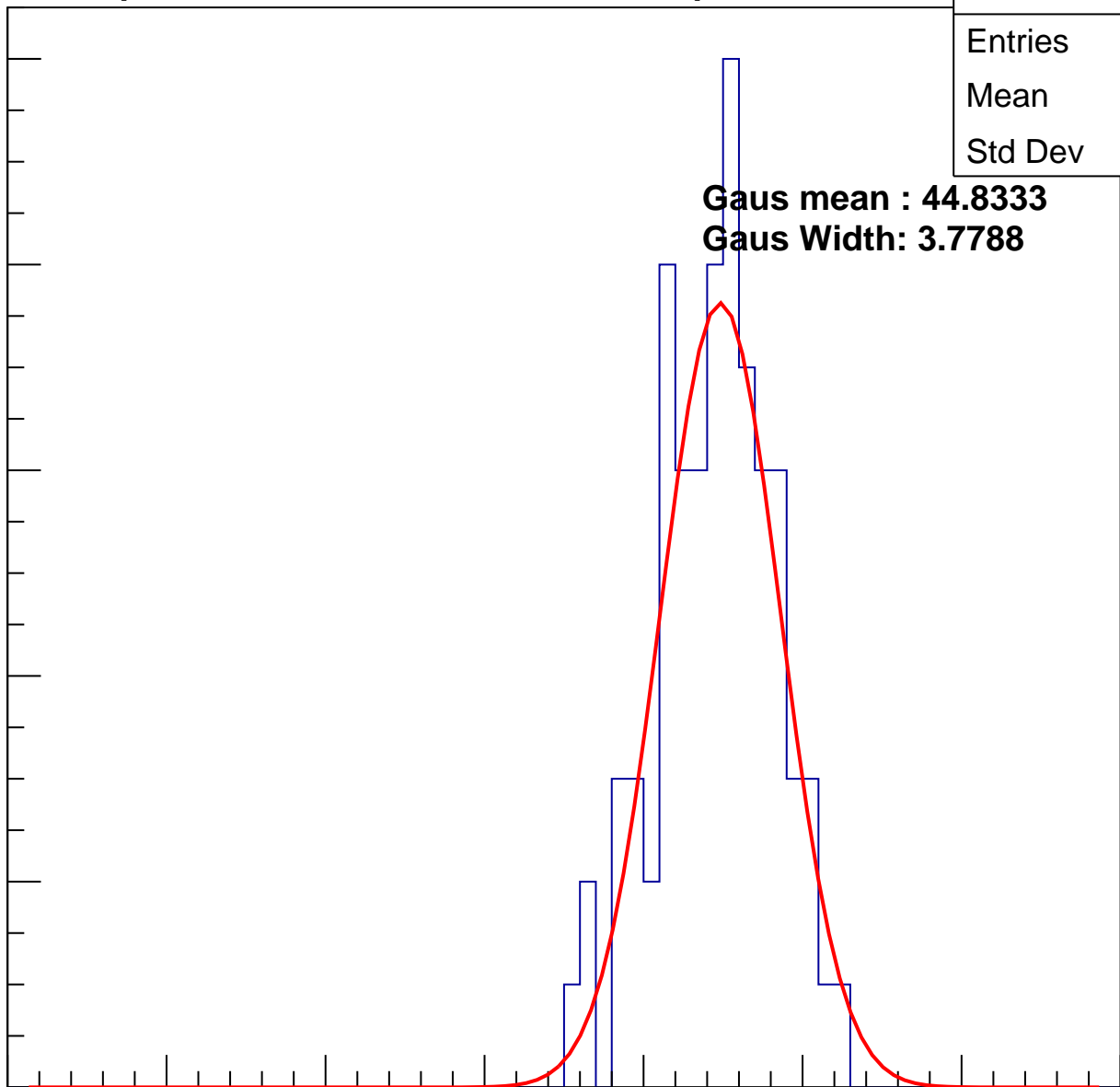
**Gaus mean : 44.8333**

**Gaus Width: 3.7788**

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

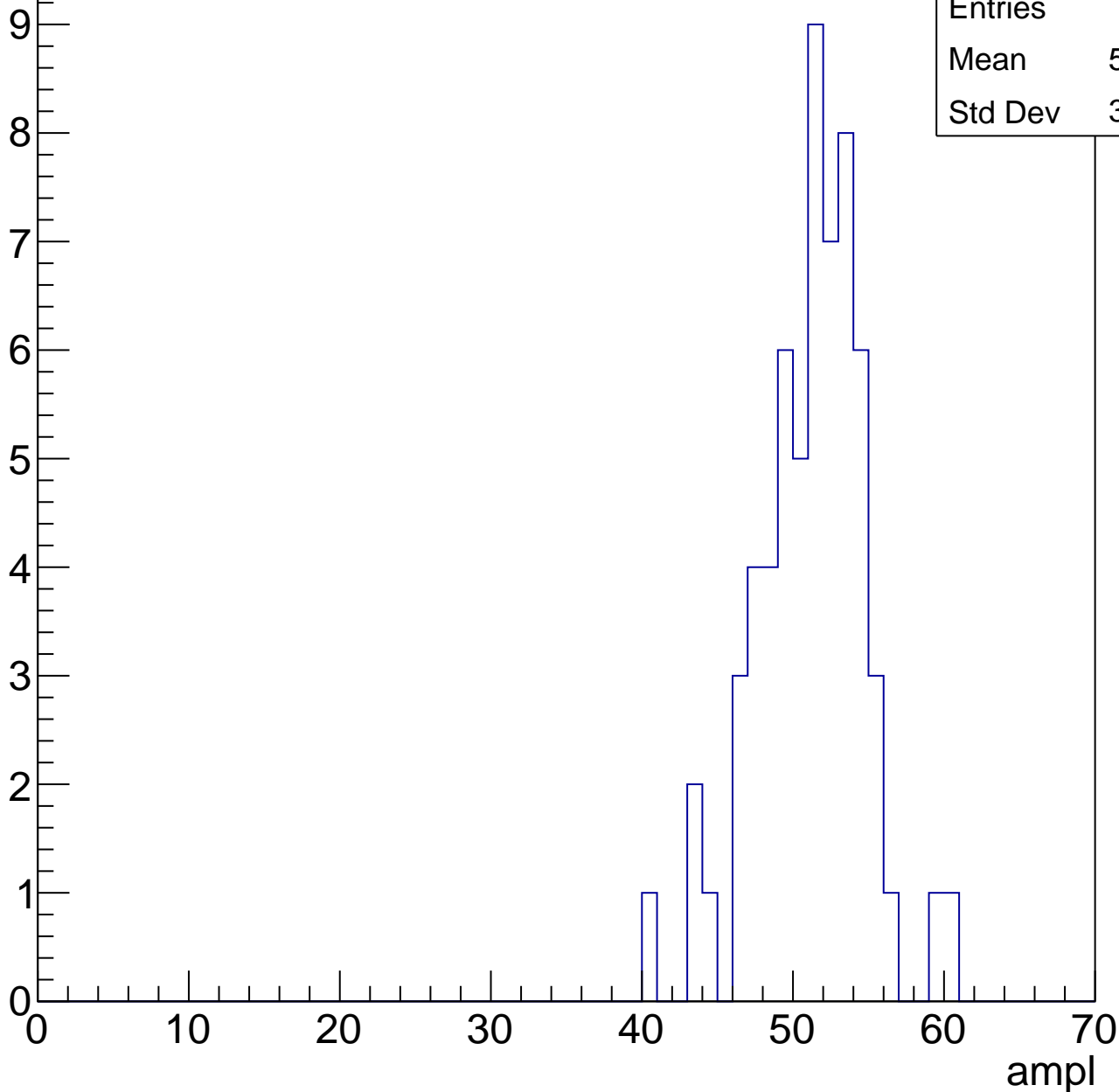


# B1L003S, U26-ch89, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	50.69
Std Dev	3.608

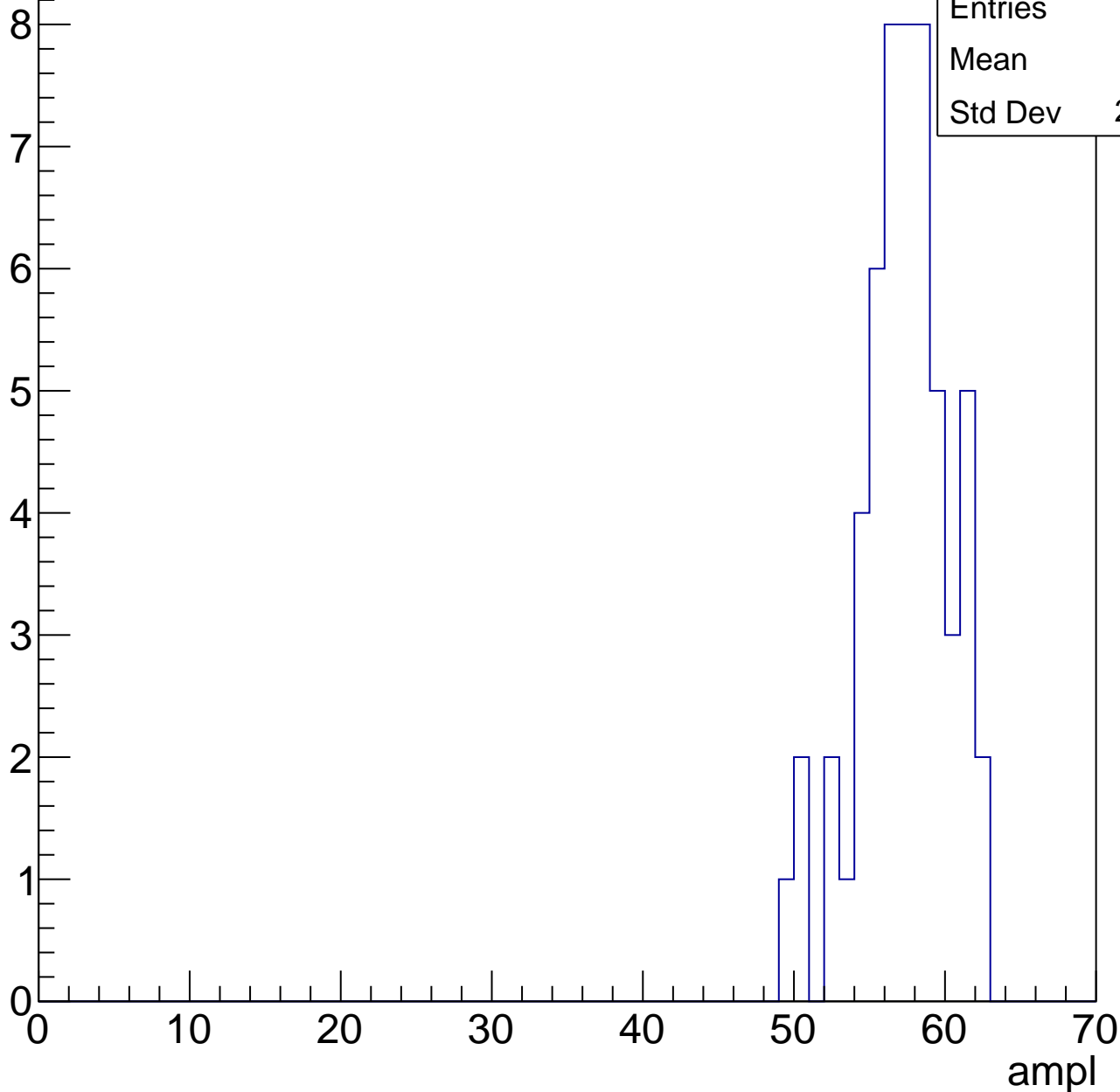


# B1L003S, U26-ch89, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	56.8
Std Dev	2.951

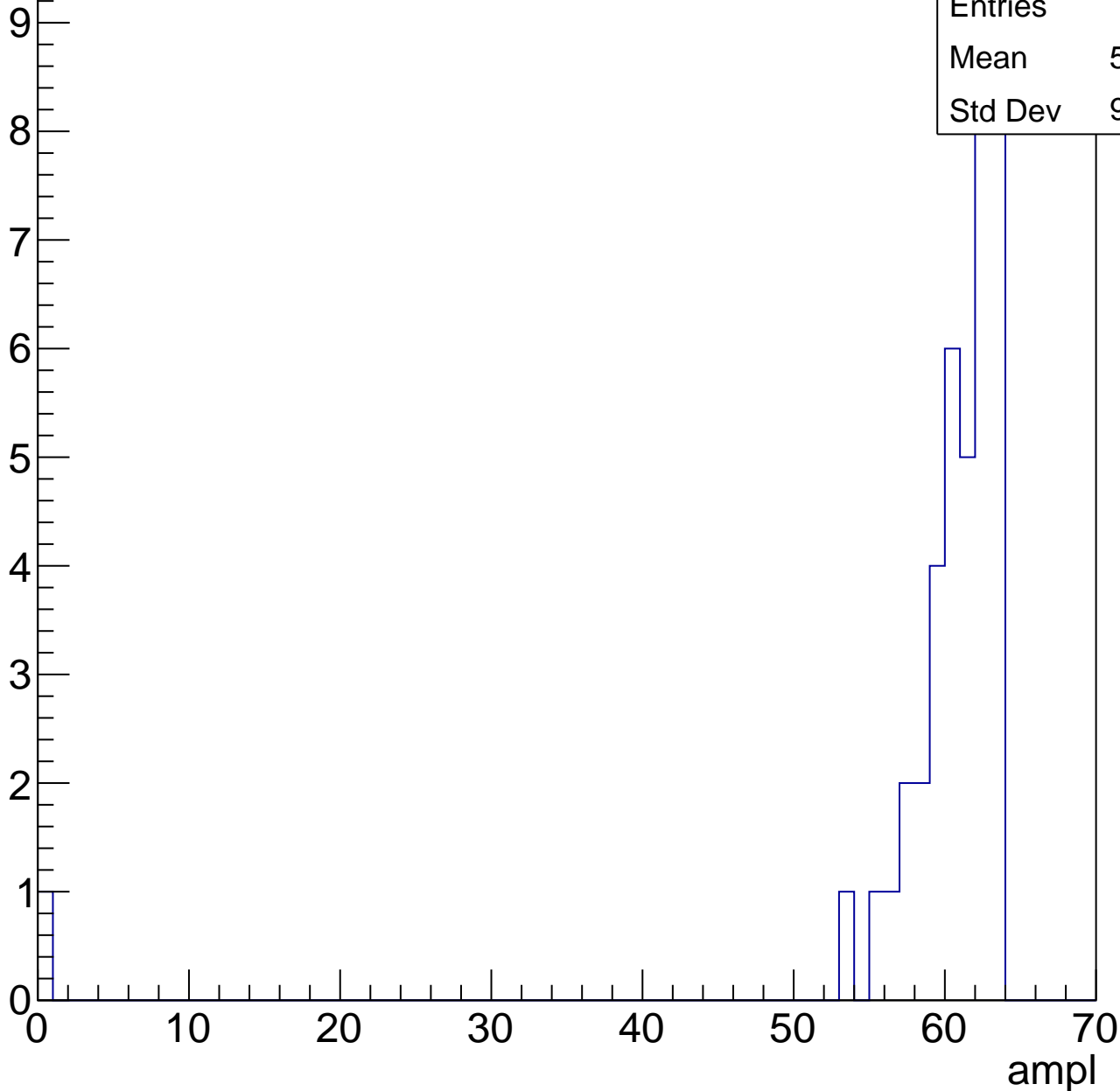


# B1L003S, U26-ch89, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	40
Mean	58.95
Std Dev	9.739



# B1L003S, U26-ch89, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch89, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U26-ch90, adc0

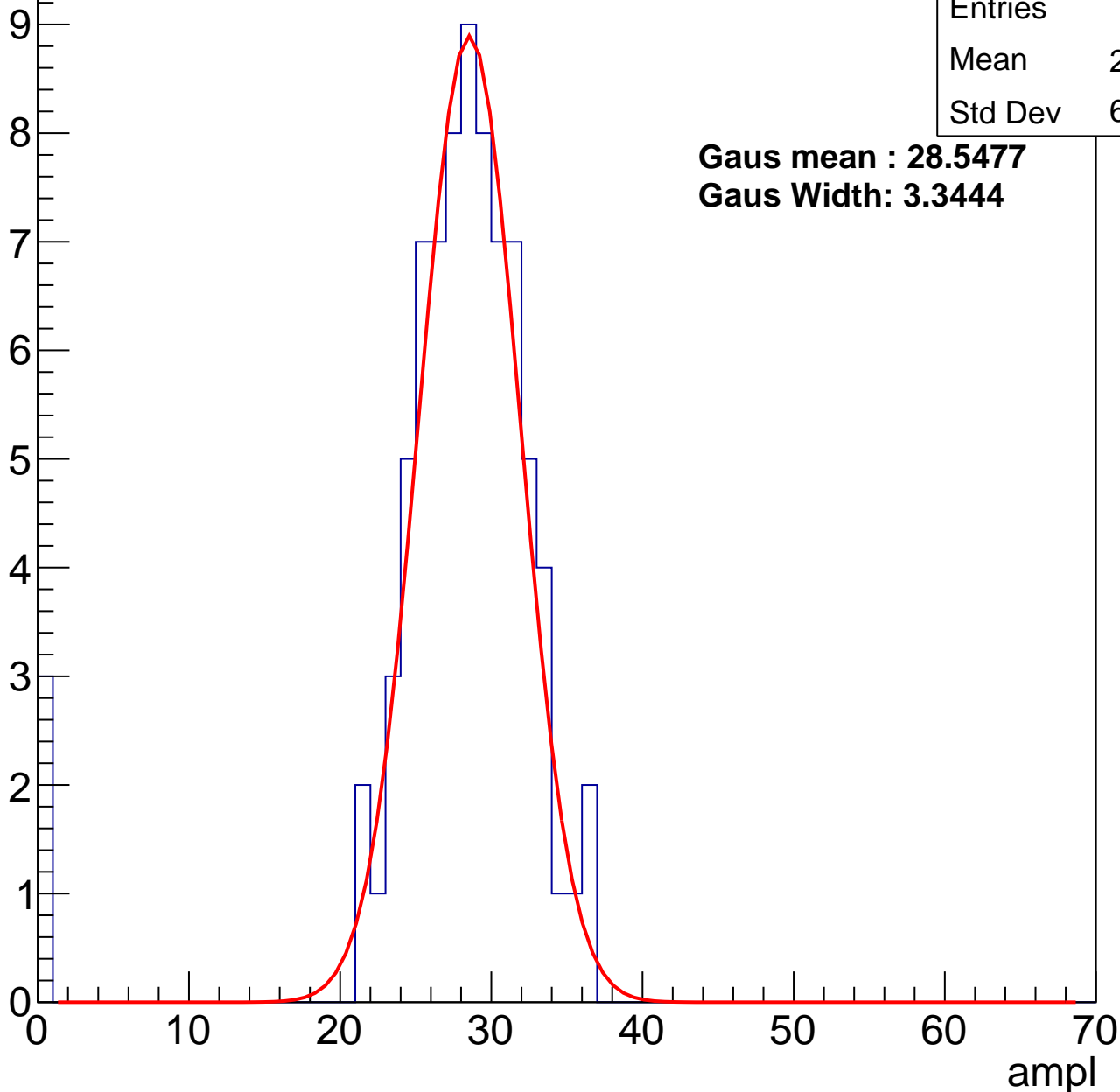
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	80
Mean	27.12
Std Dev	6.296

**Gaus mean : 28.5477**

**Gaus Width: 3.3444**



# B1L003S, U26-ch90, adc1

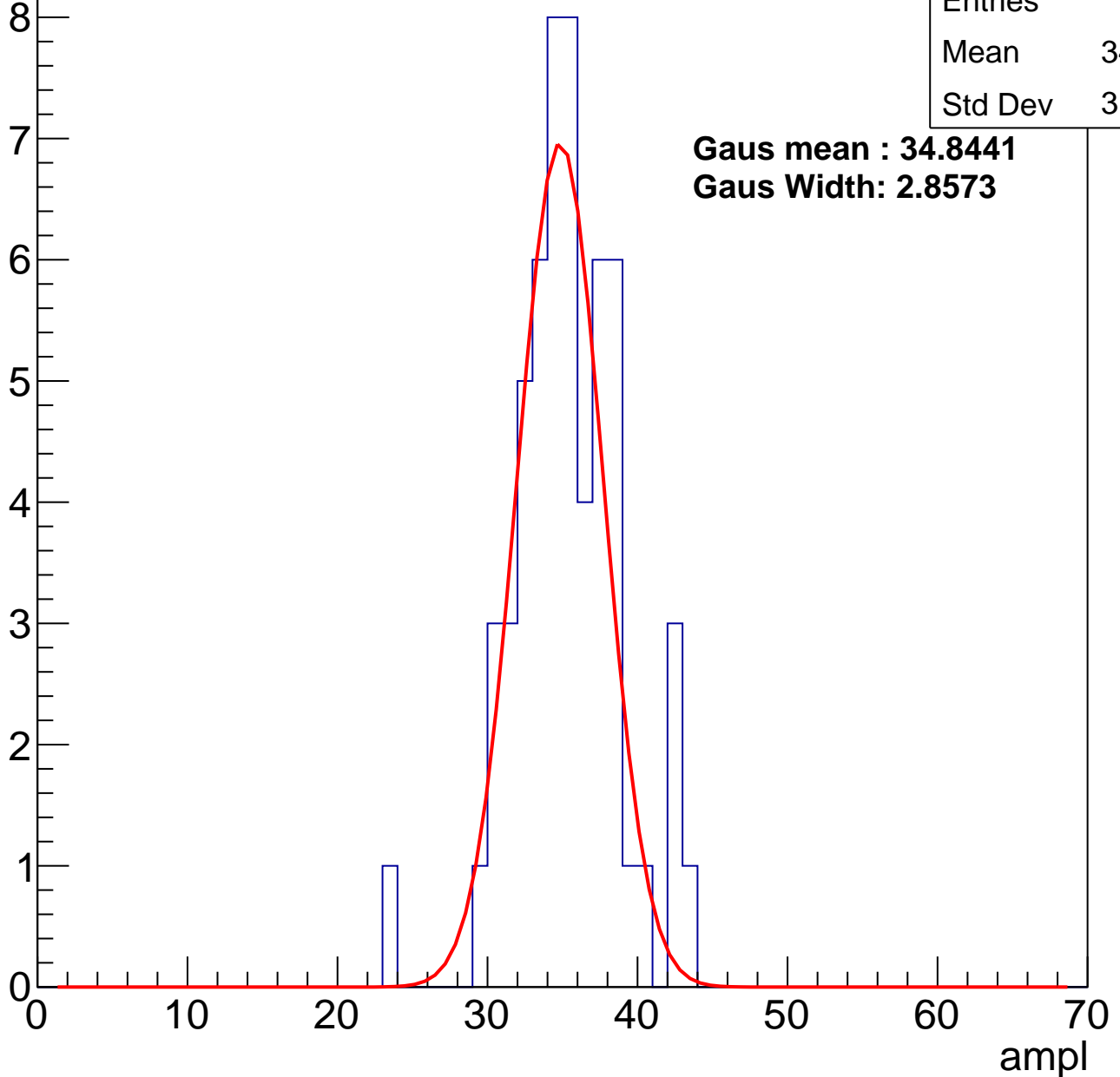
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	34.86
Std Dev	3.536

**Gaus mean : 34.8441**

**Gaus Width: 2.8573**



# B1L003S, U26-ch90, adc2

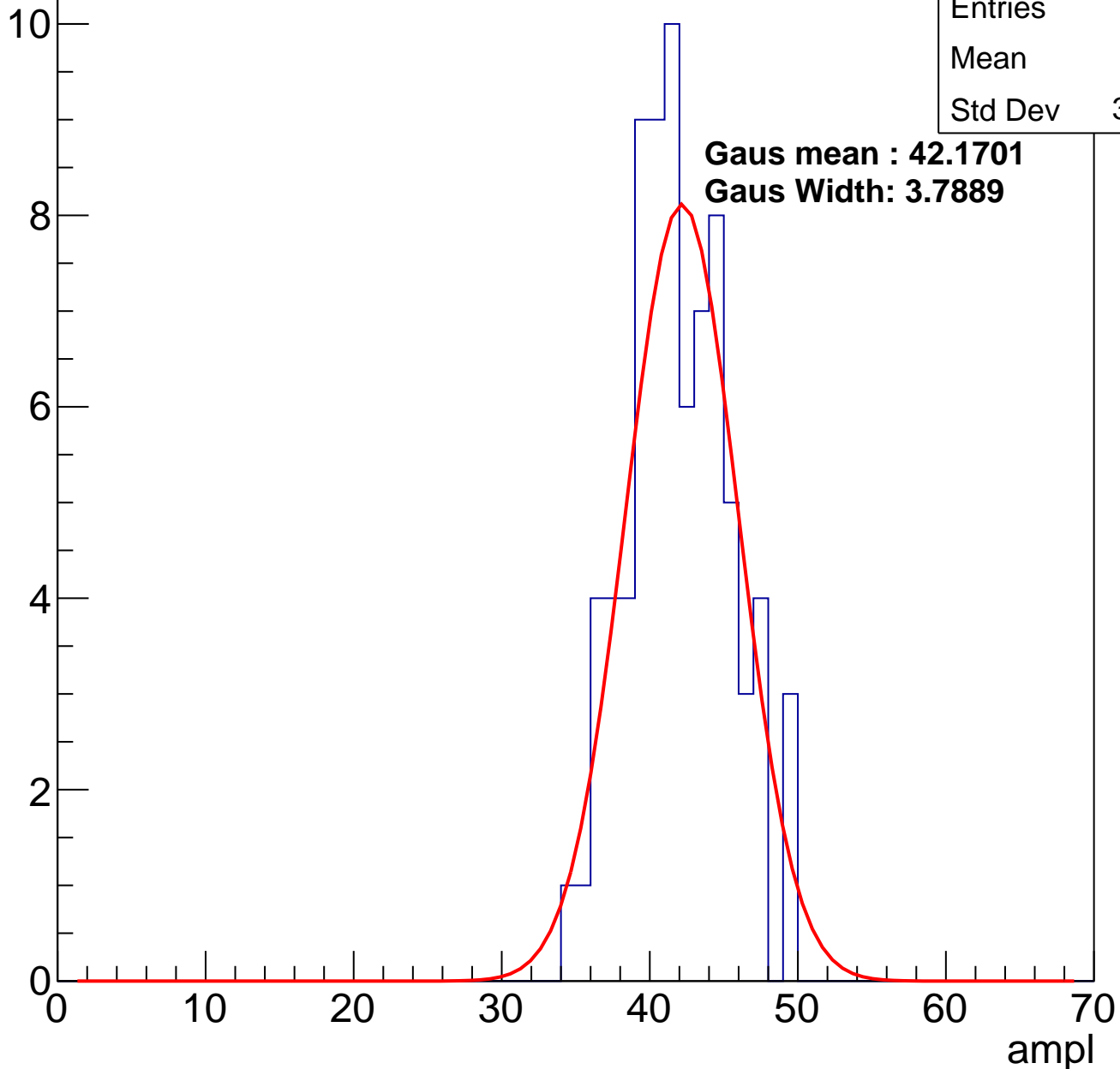
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	78
Mean	41.5
Std Dev	3.411

**Gaus mean : 42.1701**

**Gaus Width: 3.7889**

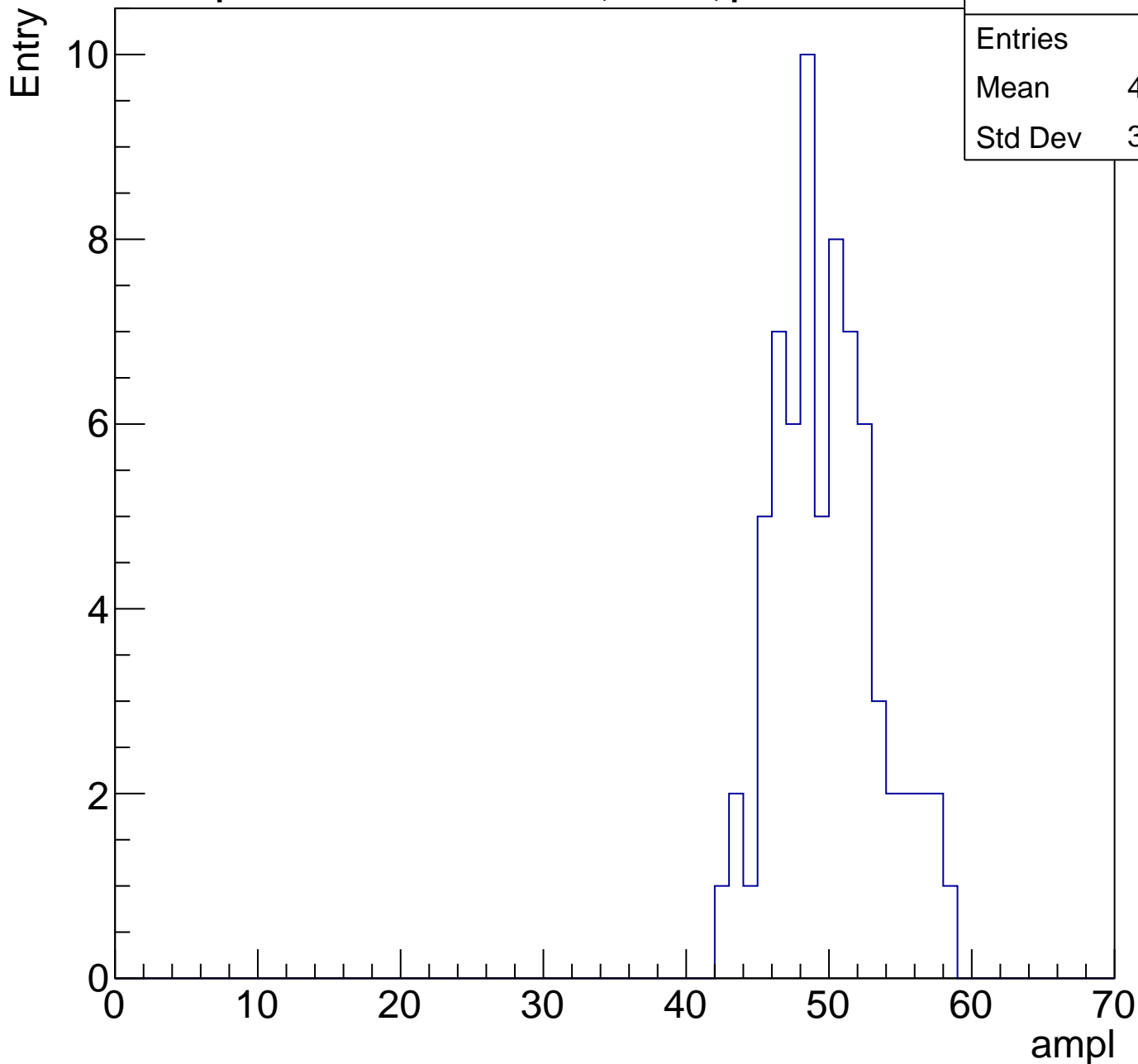
Entry



# B1L003S, U26-ch90, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	70
Mean	49.37
Std Dev	3.546

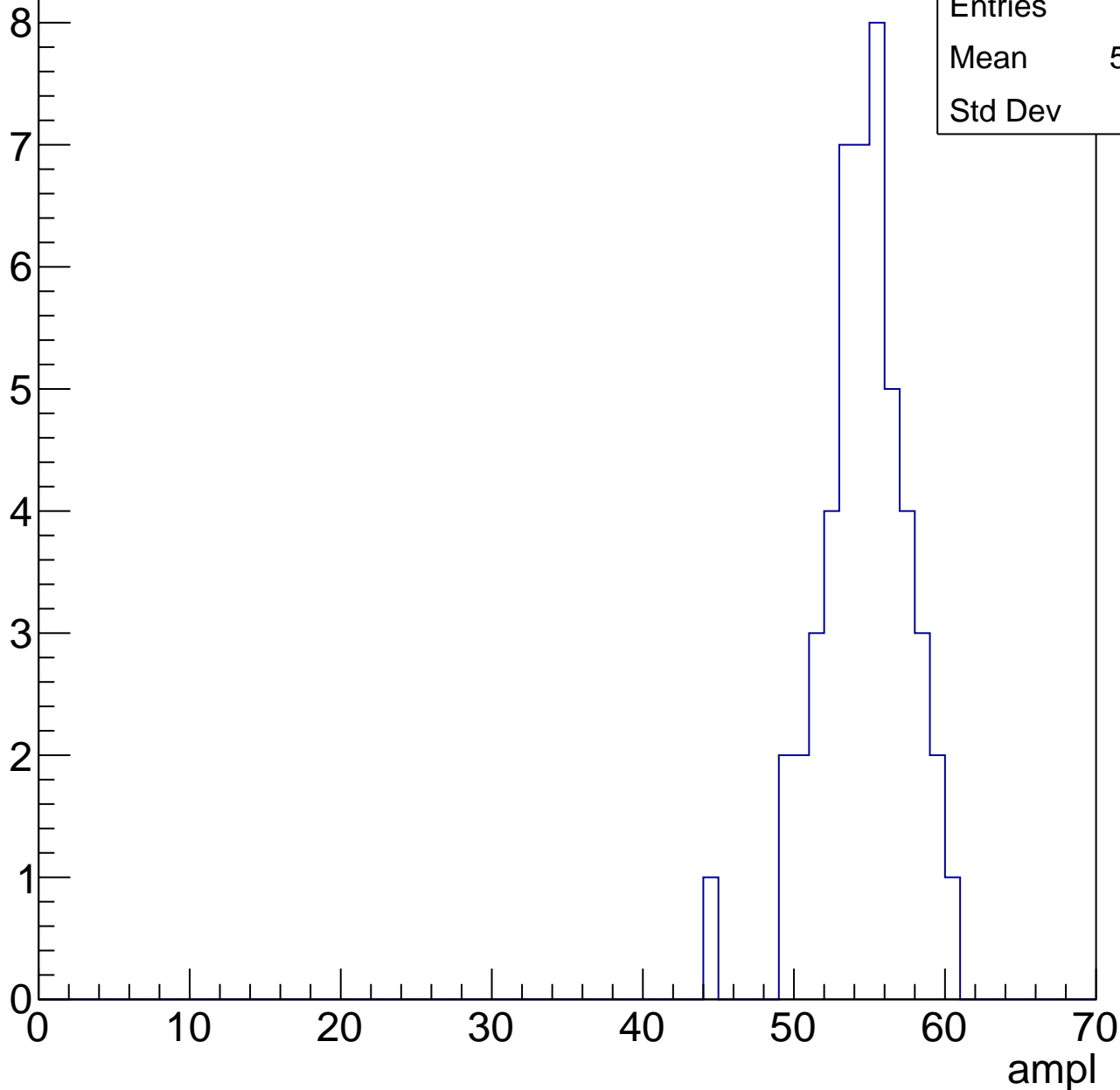


# B1L003S, U26-ch90, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	49
Mean	54.12
Std Dev	2.96

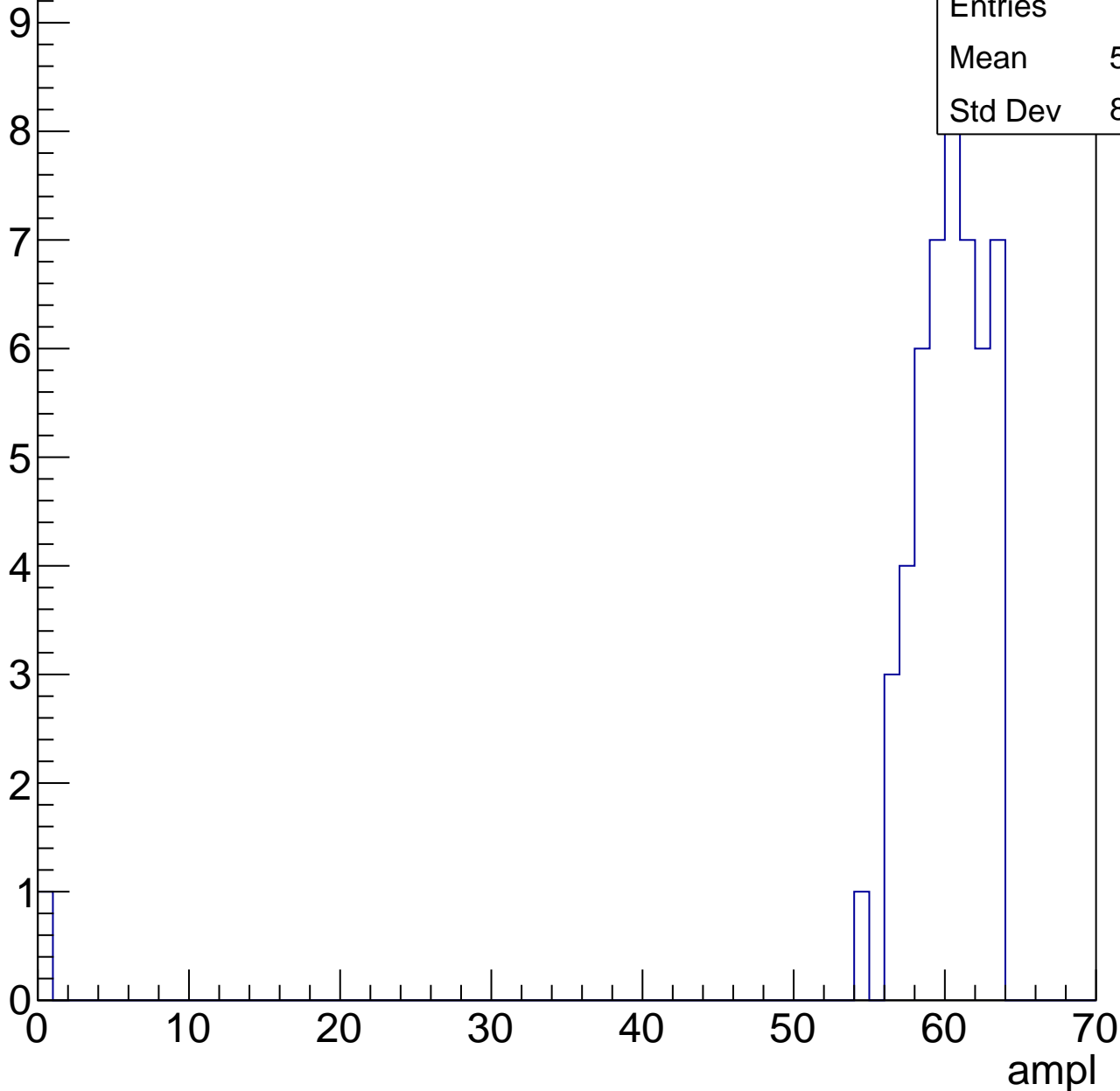


# B1L003S, U26-ch90, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

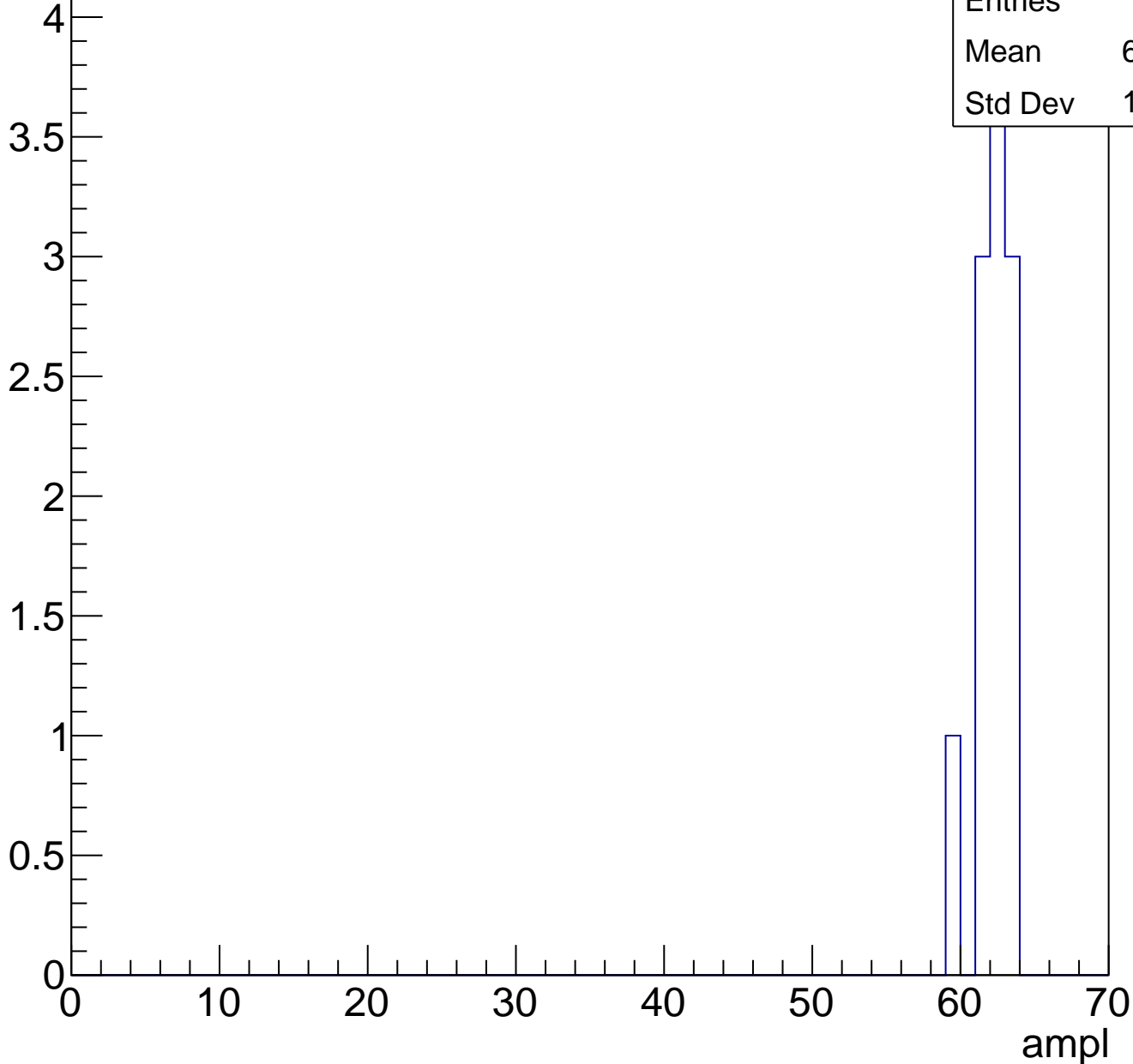
Entries	51
Mean	58.65
Std Dev	8.577



# B1L003S, U26-ch90, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch90, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U26-ch91, adc0

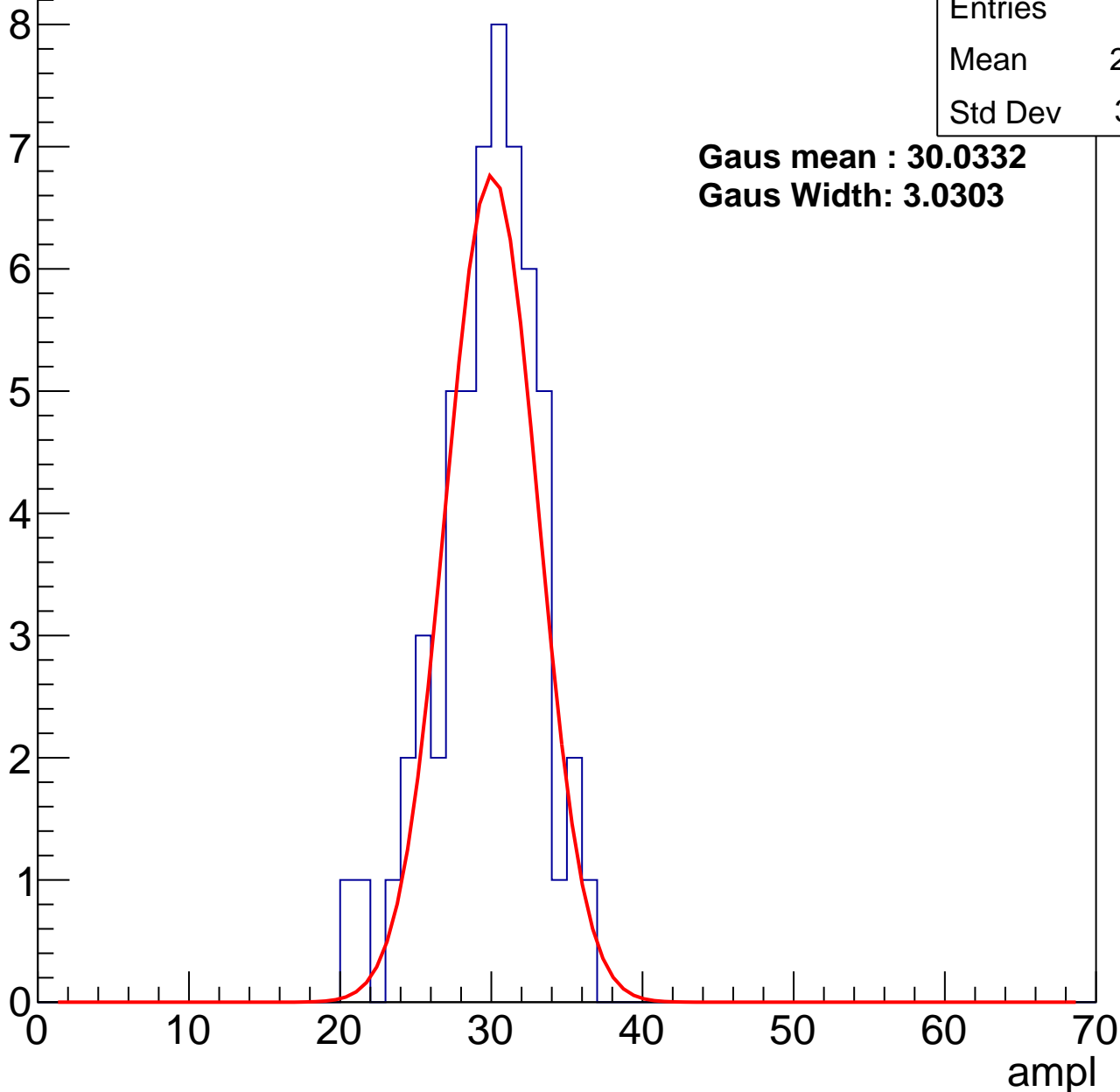
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	29.32
Std Dev	3.331

**Gaus mean : 30.0332**

**Gaus Width: 3.0303**



# B1L003S, U26-ch91, adc1

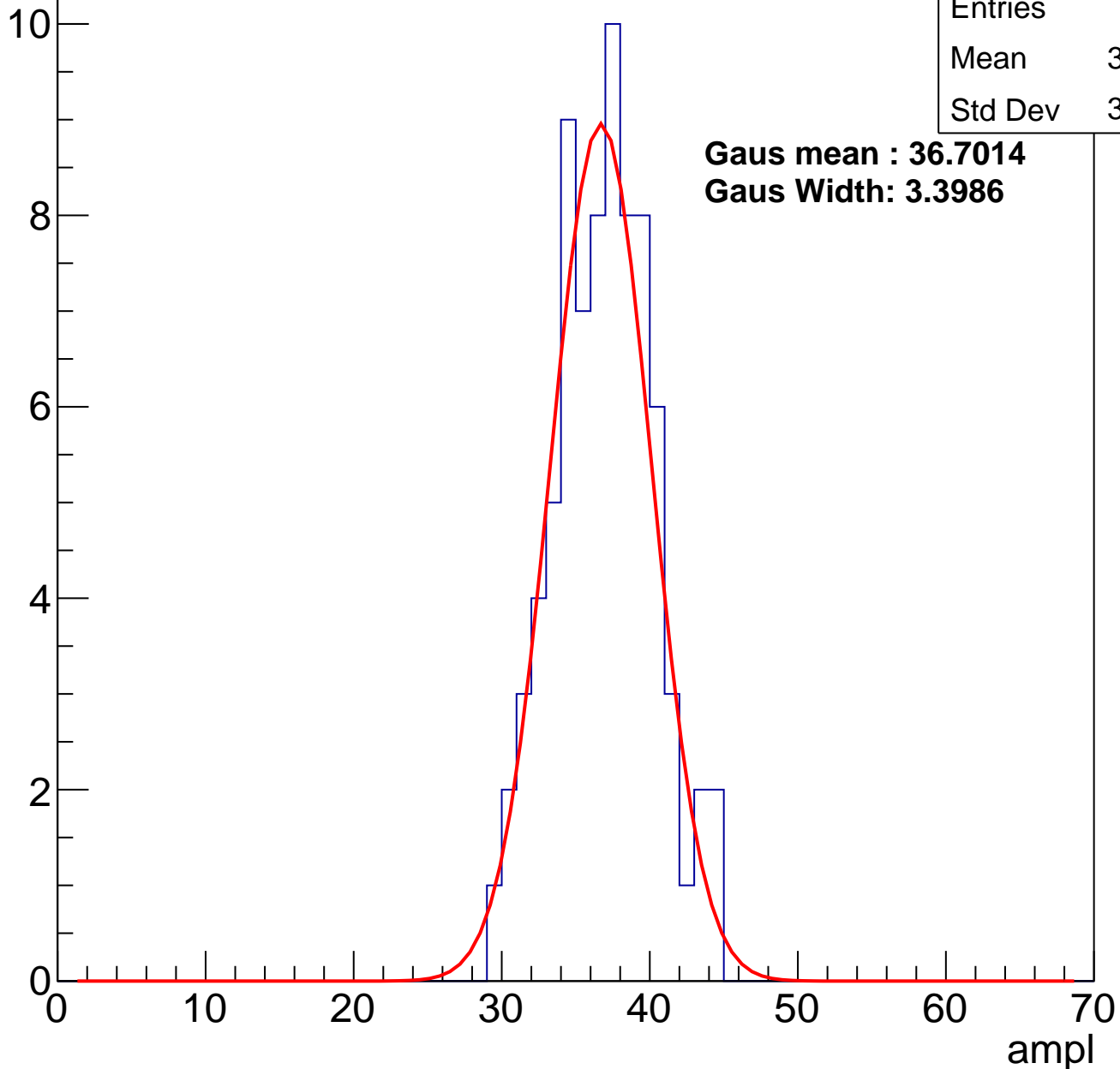
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	79
Mean	36.44
Std Dev	3.337

**Gaus mean : 36.7014**

**Gaus Width: 3.3986**

Entry



# B1L003S, U26-ch91, adc2

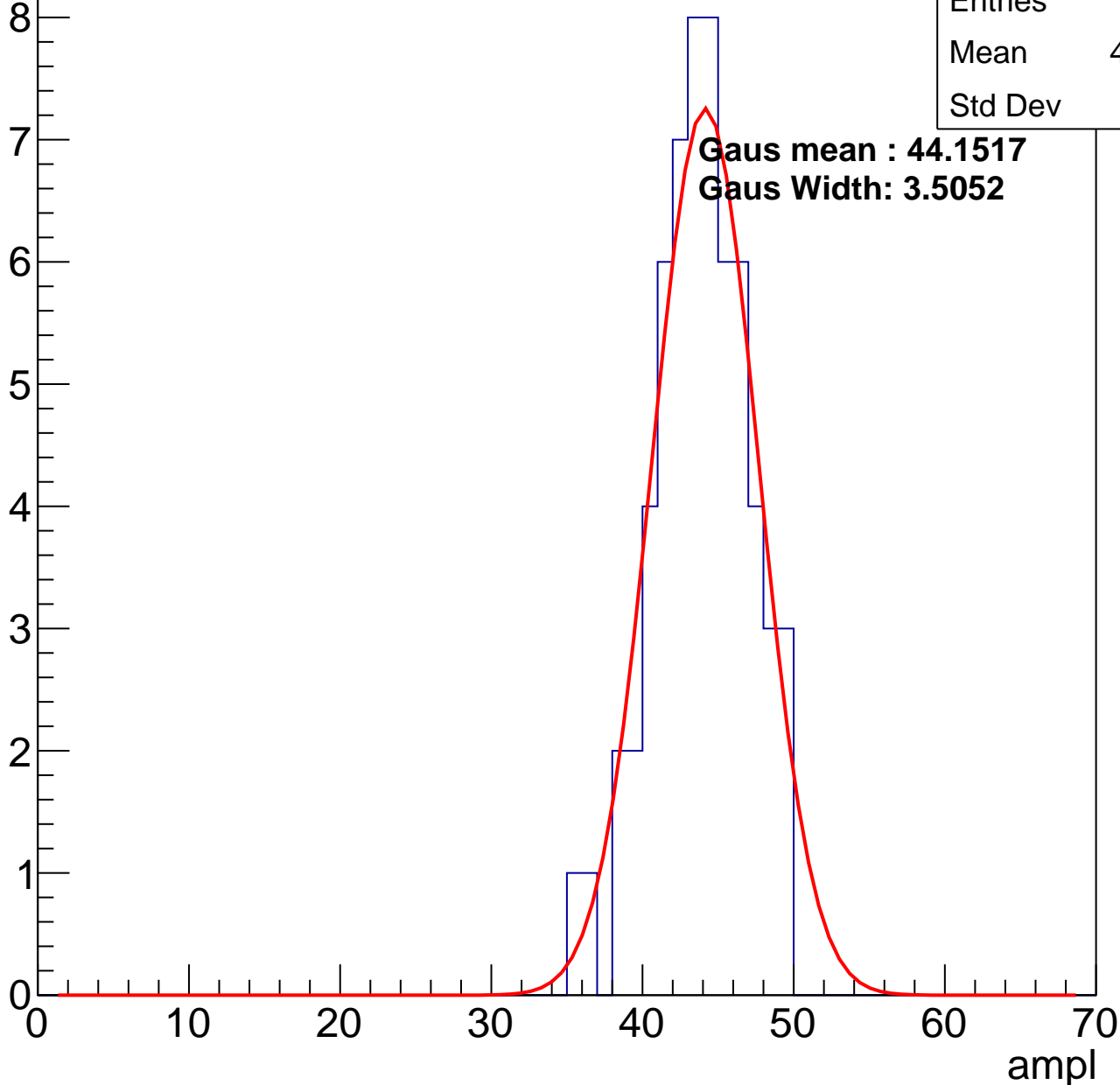
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	43.38
Std Dev	3.1

**Gaus mean : 44.1517**

**Gaus Width: 3.5052**

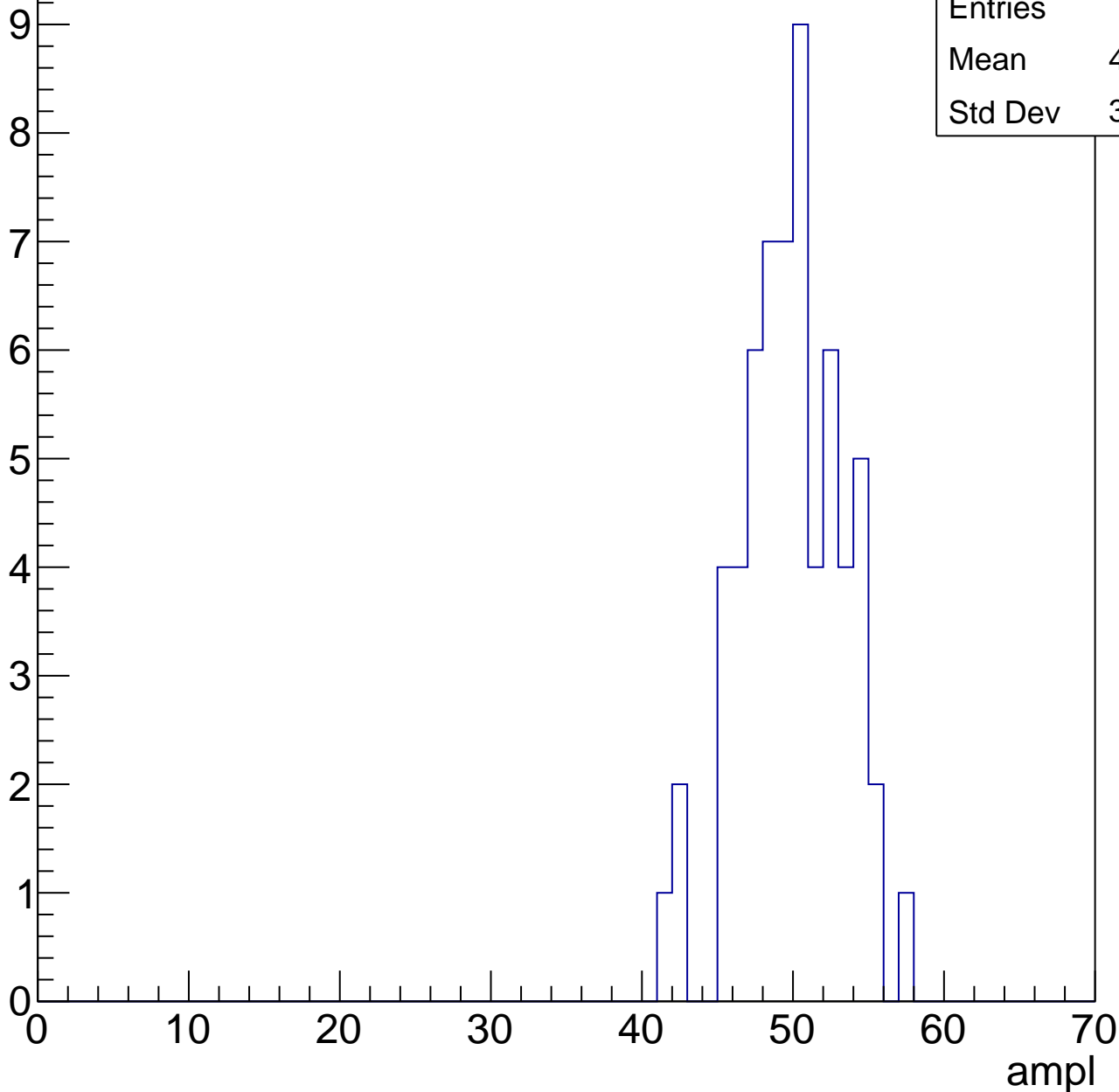


# B1L003S, U26-ch91, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

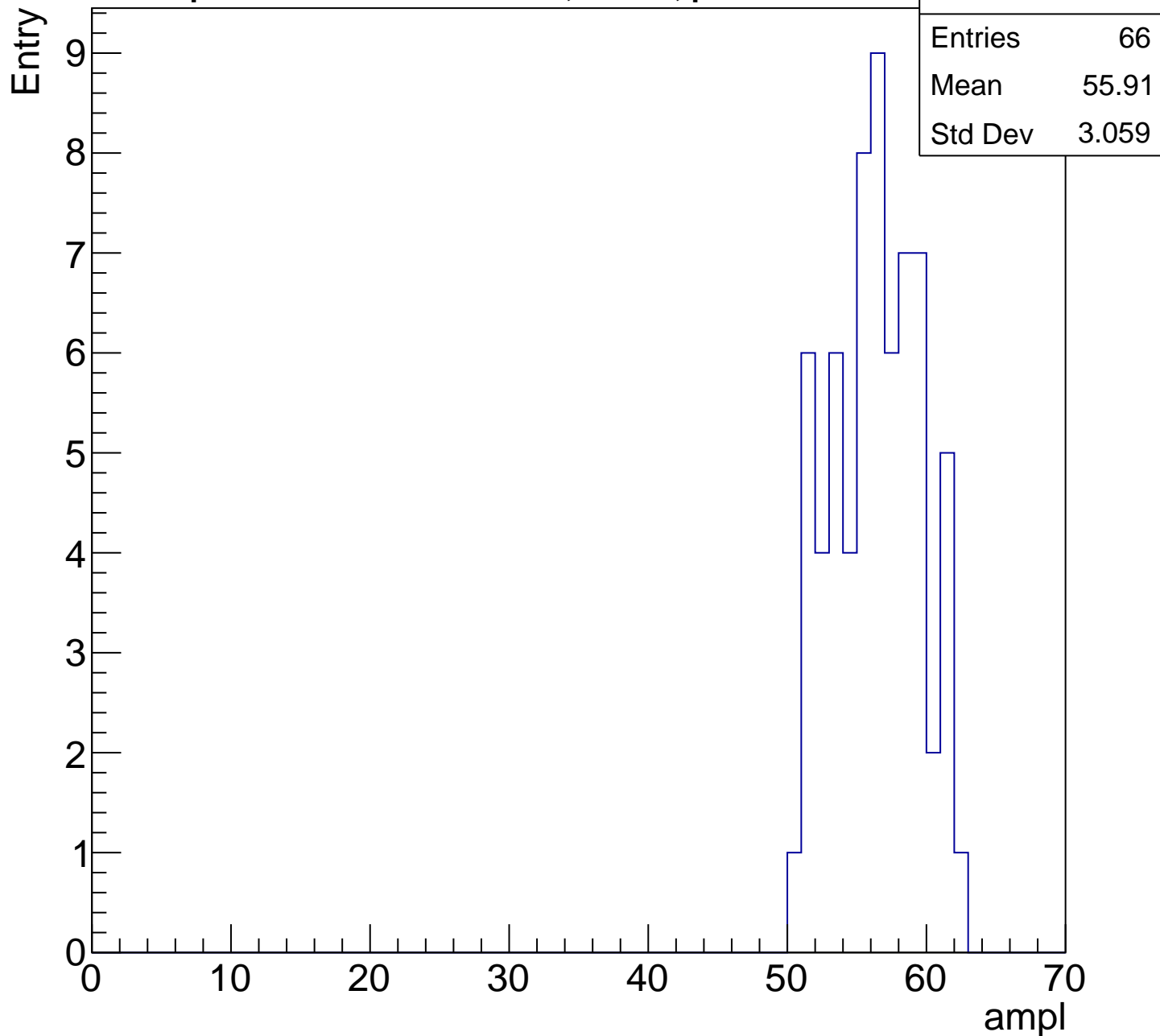
Entry

Entries	62
Mean	49.44
Std Dev	3.324



# B1L003S, U26-ch91, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

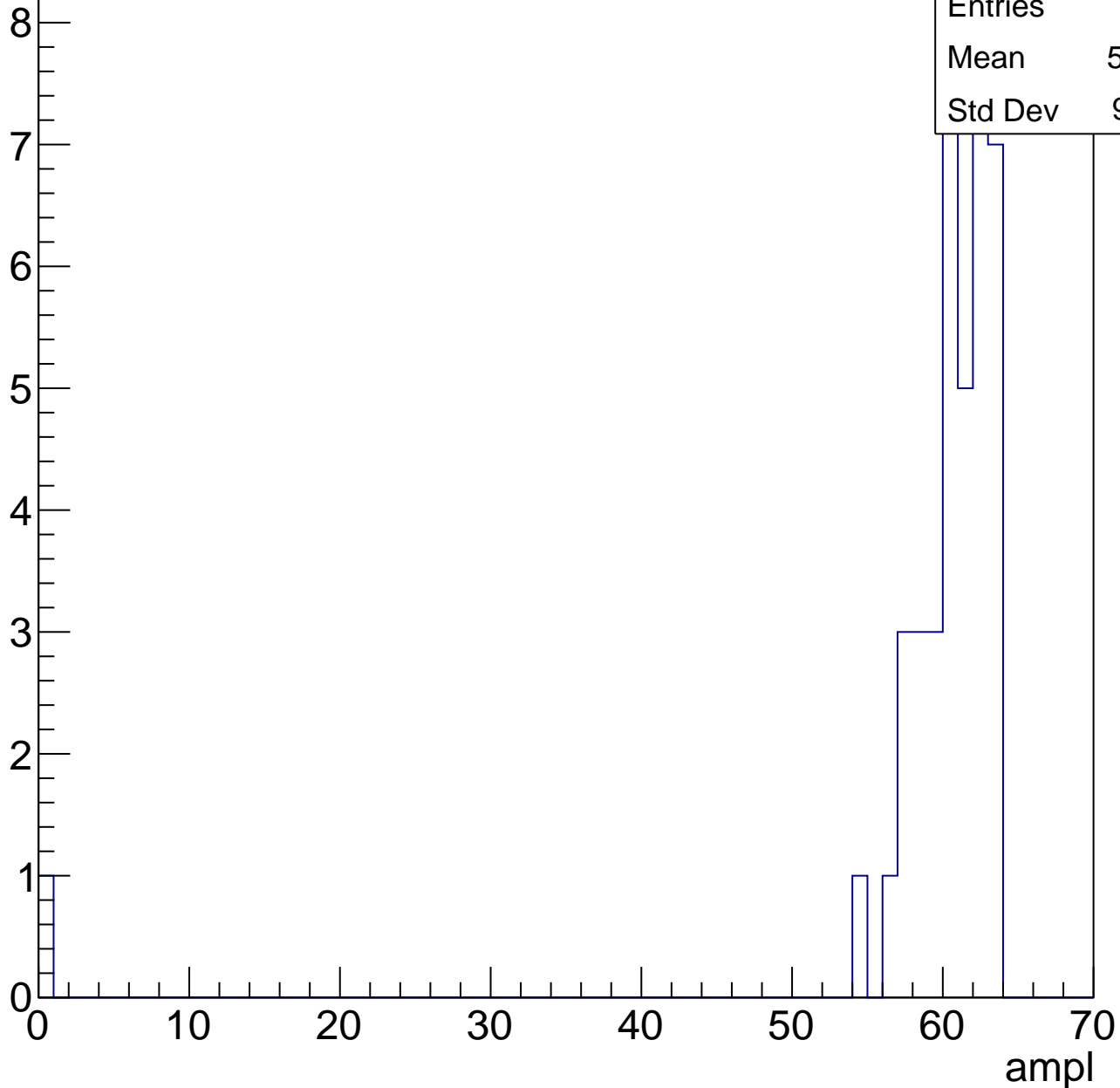


# B1L003S, U26-ch91, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	40
Mean	58.85
Std Dev	9.671



# B1L003S, U26-ch91, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch91, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U26-ch92, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	52
Mean	29.12
Std Dev	3.093

**Gaus mean : 29.3646**

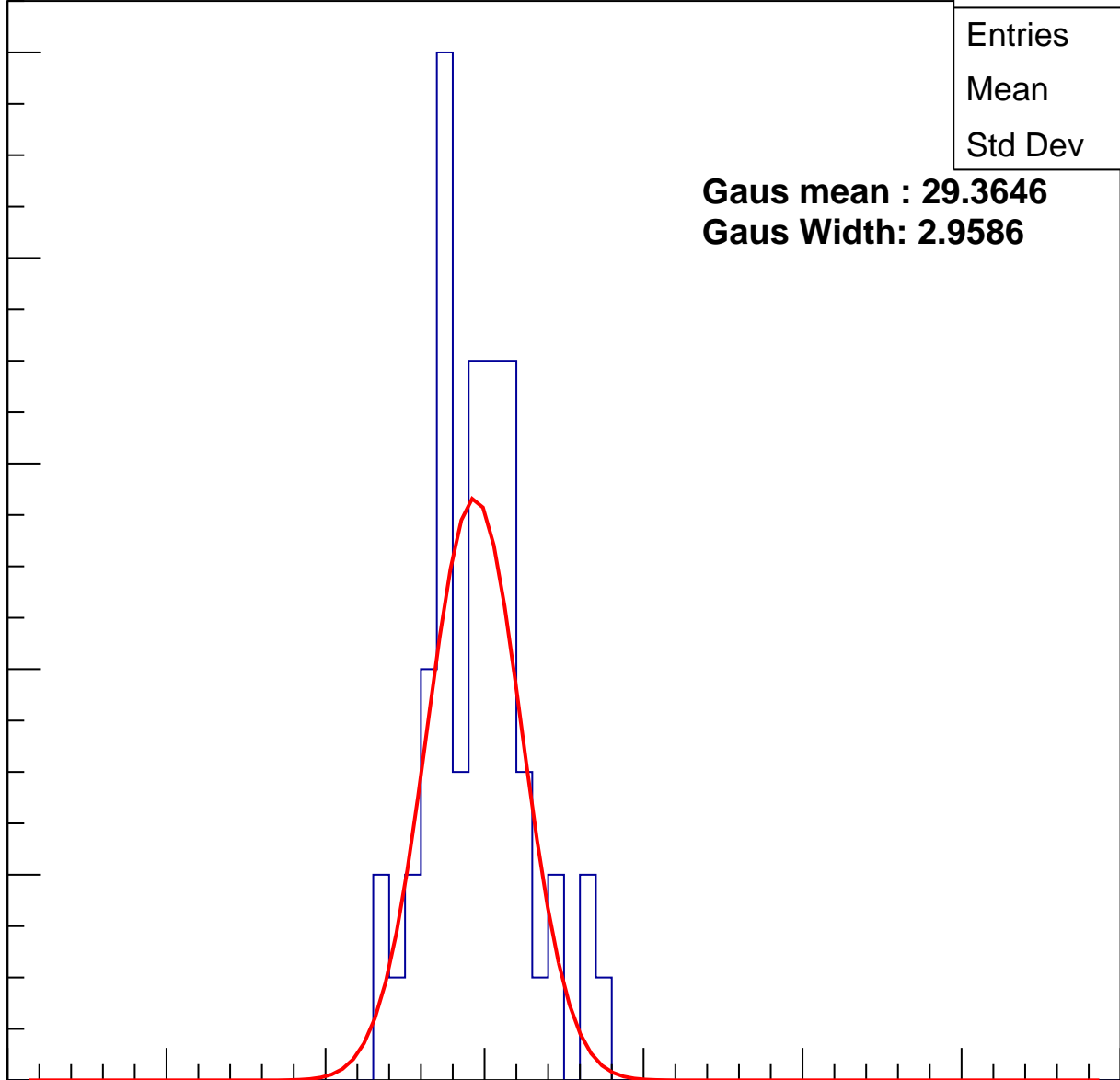
**Gaus Width: 2.9586**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



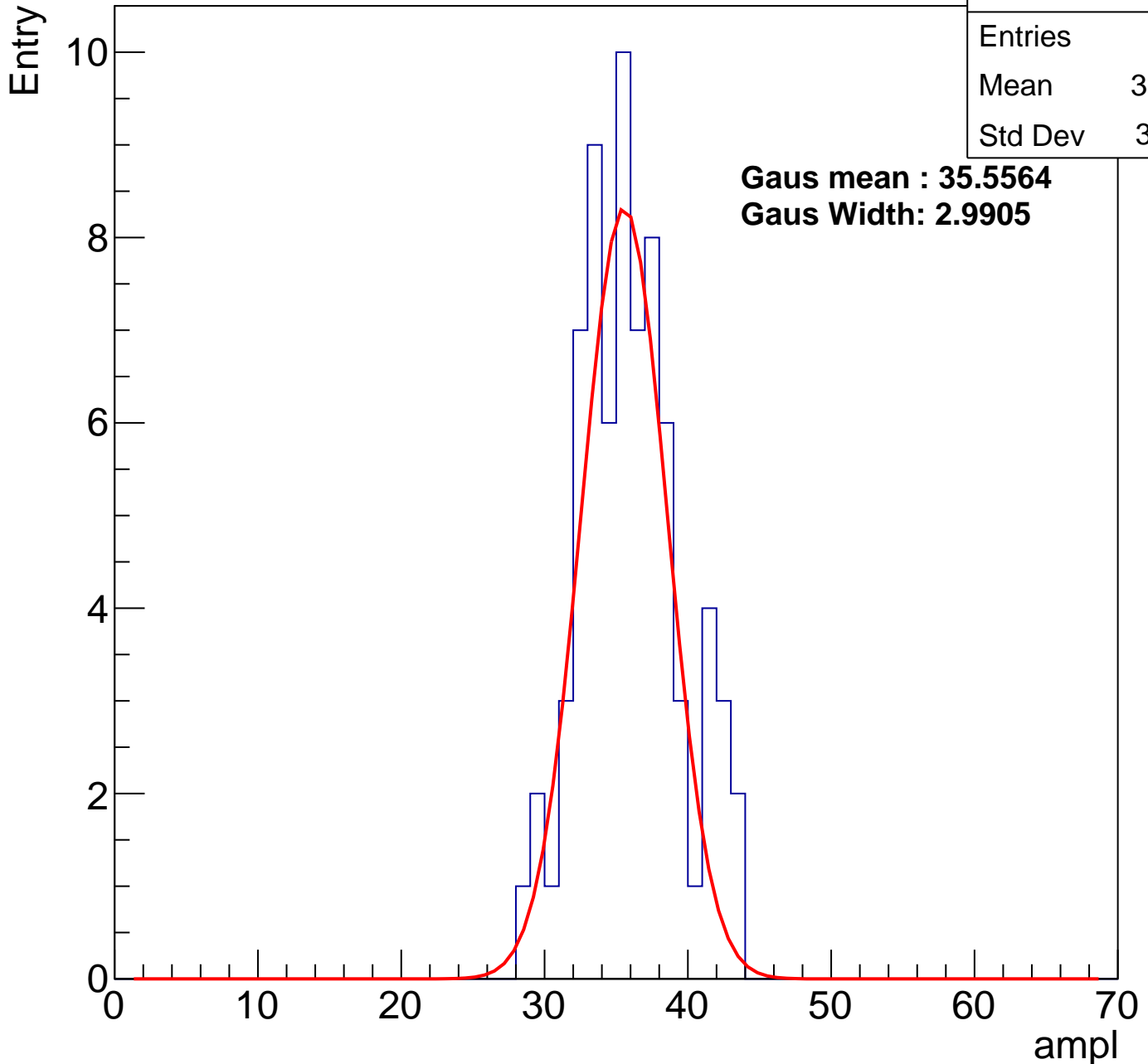
# B1L003S, U26-ch92, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	73
Mean	35.52
Std Dev	3.441

**Gaus mean : 35.5564**

**Gaus Width: 2.9905**



# B1L003S, U26-ch92, adc2

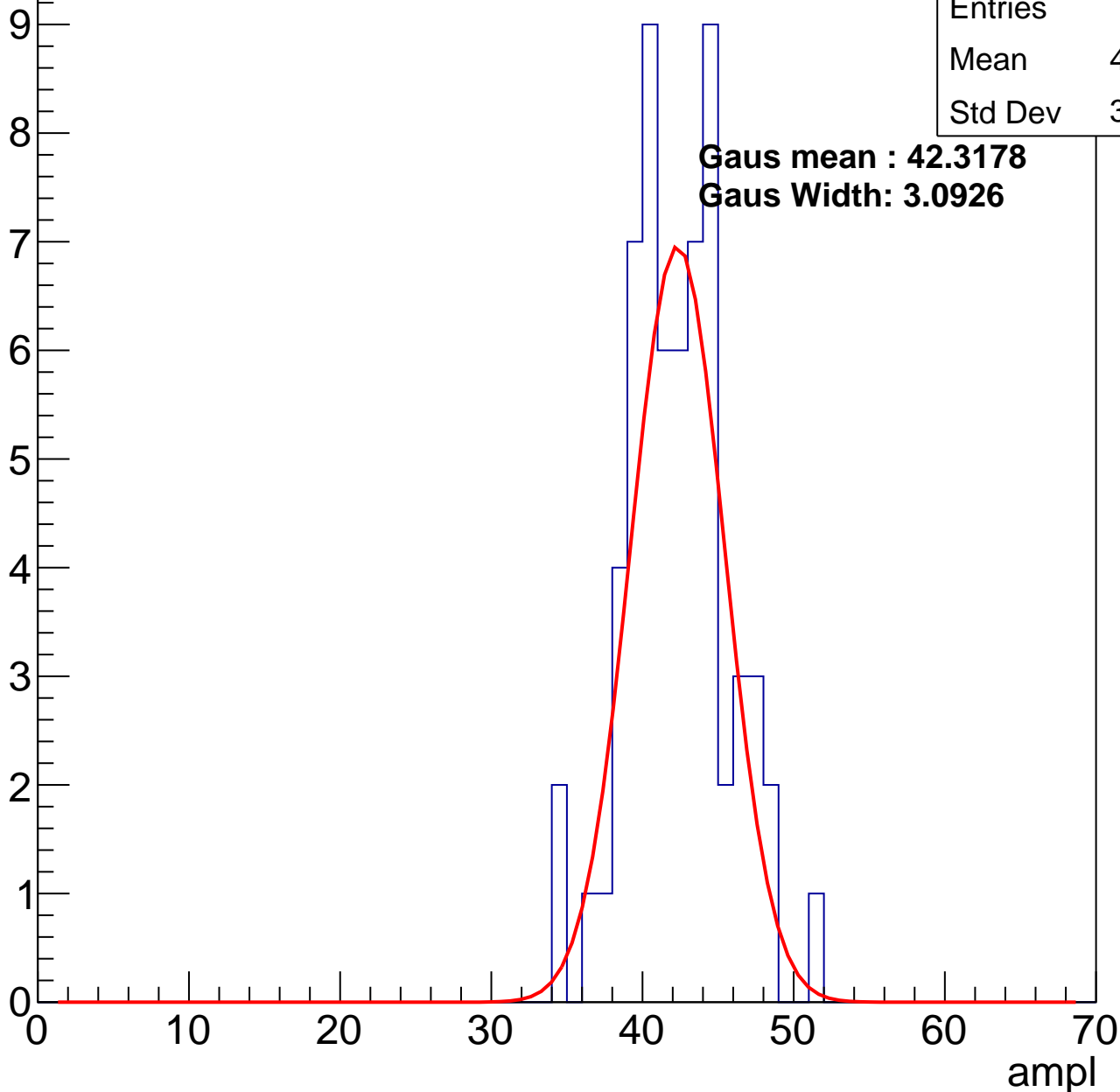
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	41.86
Std Dev	3.318

**Gaus mean : 42.3178**

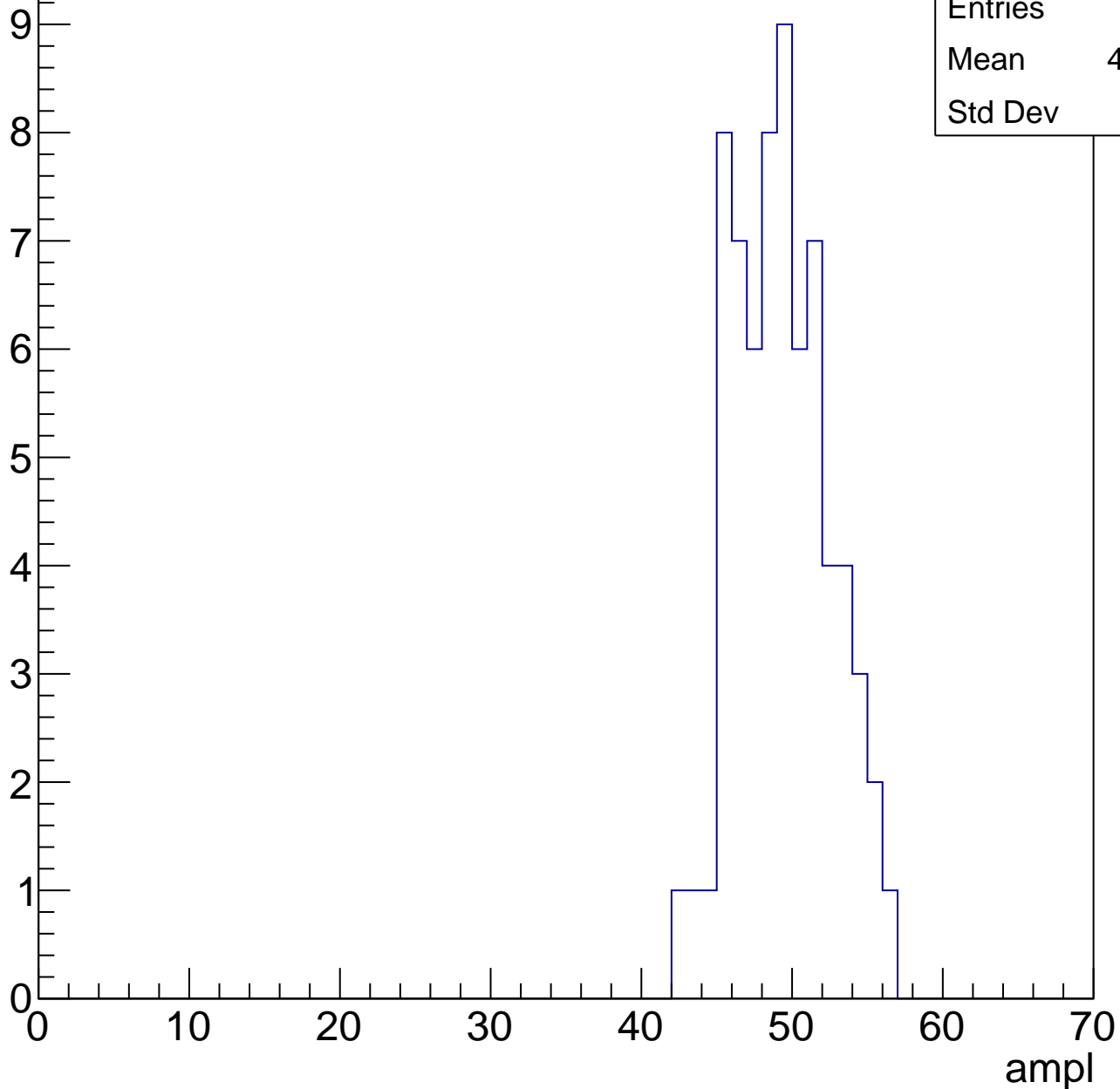
**Gaus Width: 3.0926**



# B1L003S, U26-ch92, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

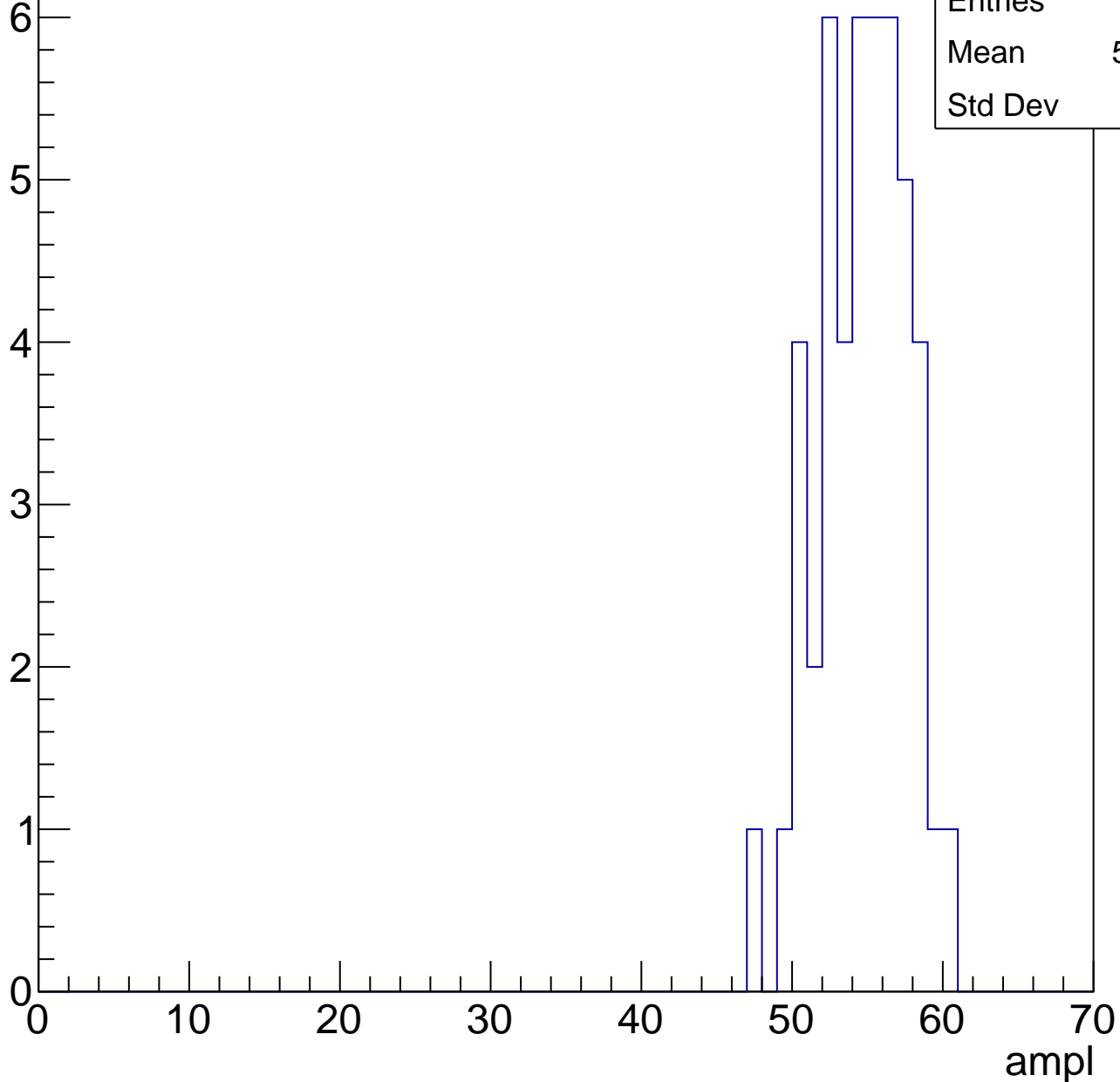


Entries	68
Mean	48.87
Std Dev	3.12

# B1L003S, U26-ch92, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

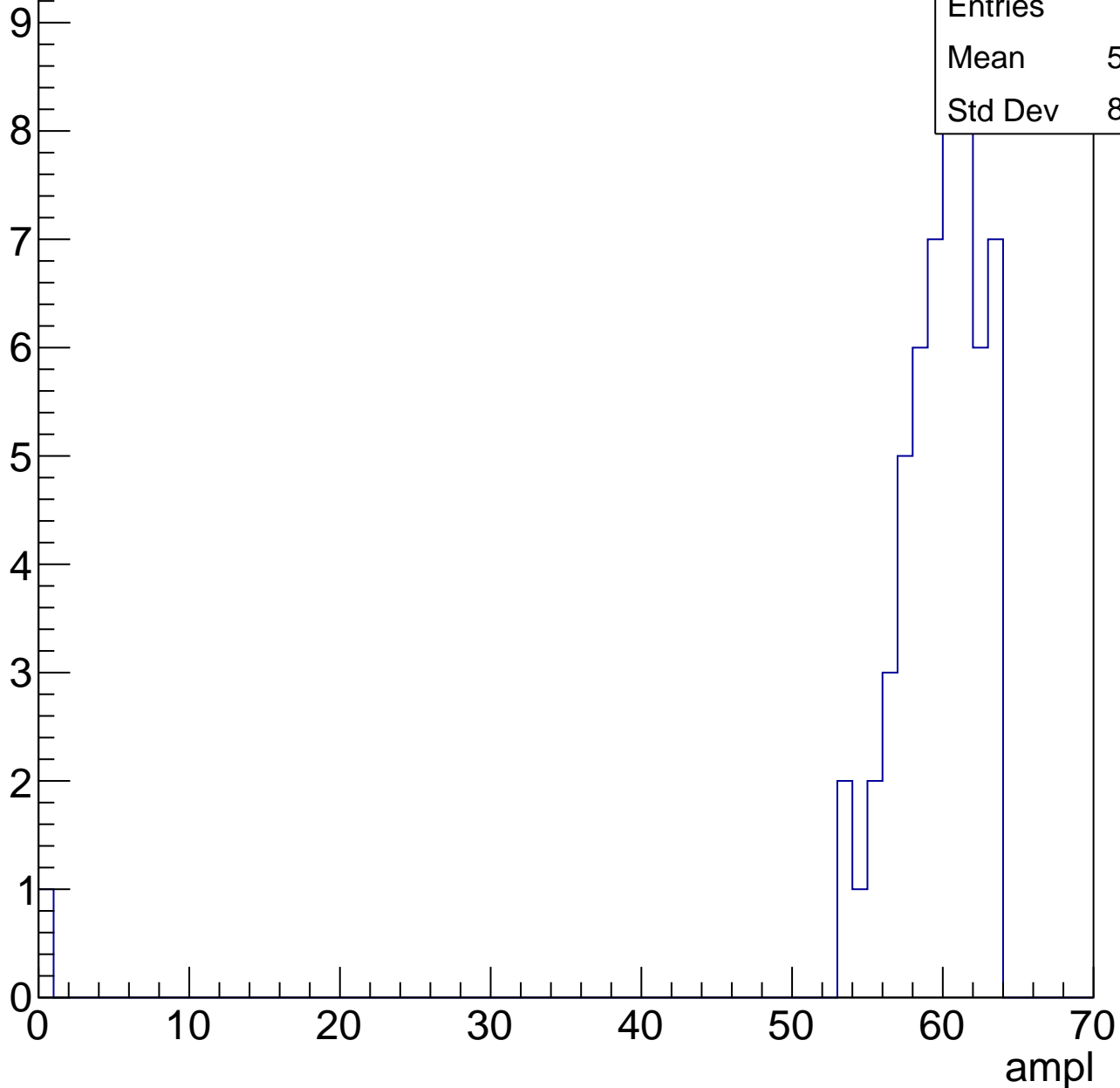


Entries	47
Mean	54.21
Std Dev	2.85

# B1L003S, U26-ch92, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

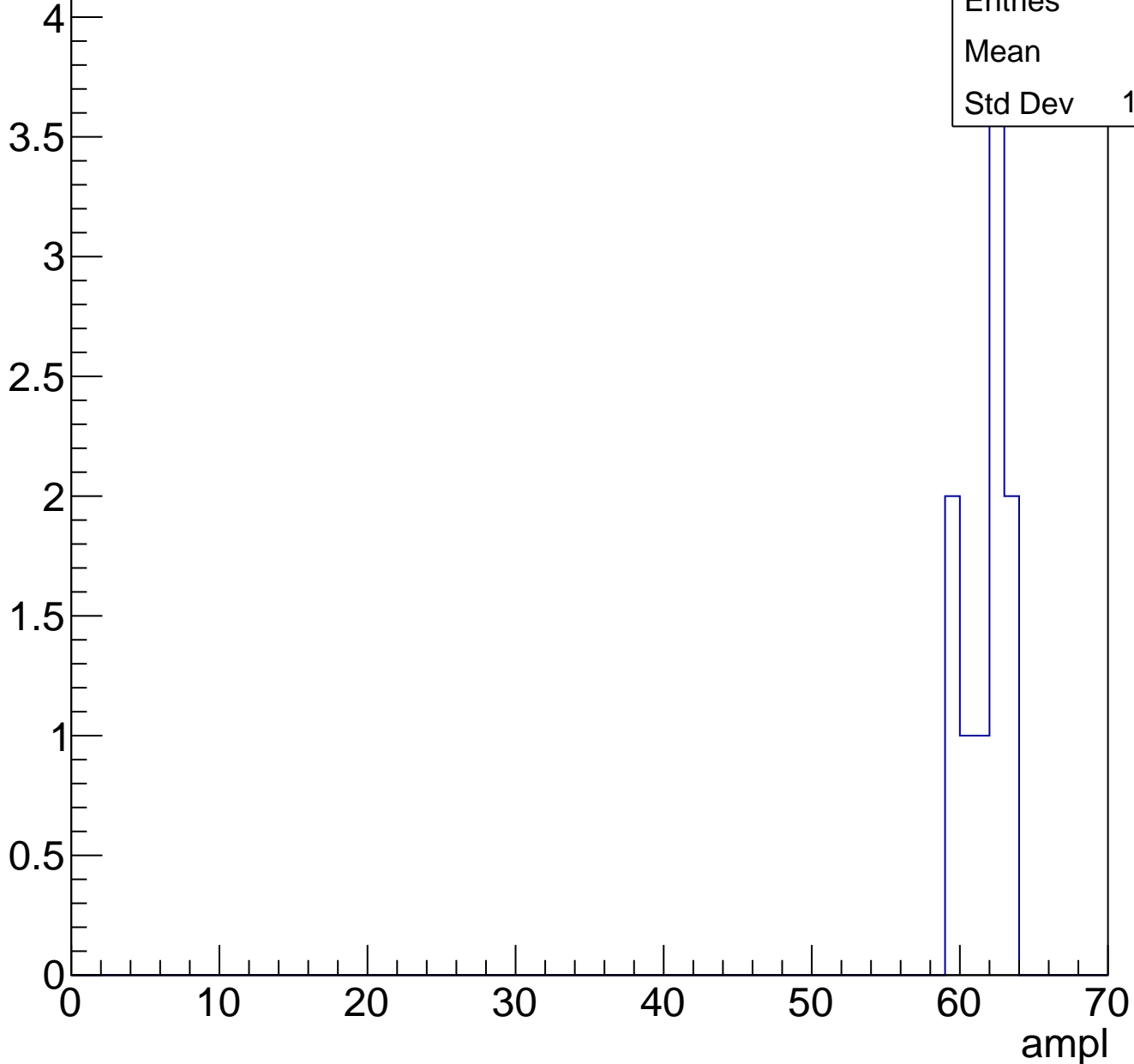
Entry



# B1L003S, U26-ch92, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	10
Mean	61.3
Std Dev	1.418



# B1L003S, U26-ch92, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U26-ch93, adc0

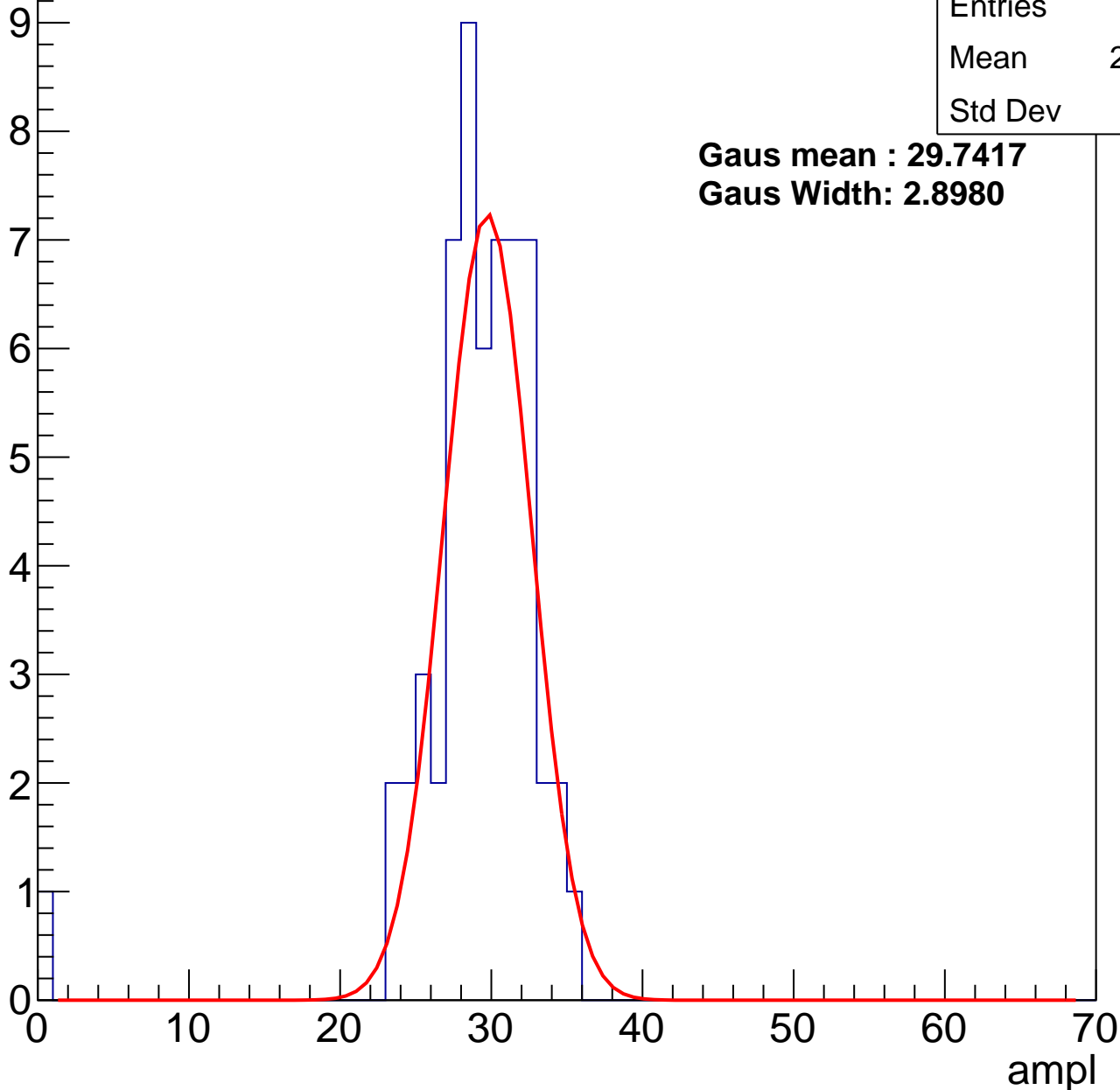
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	28.55
Std Dev	4.68

**Gaus mean : 29.7417**

**Gaus Width: 2.8980**



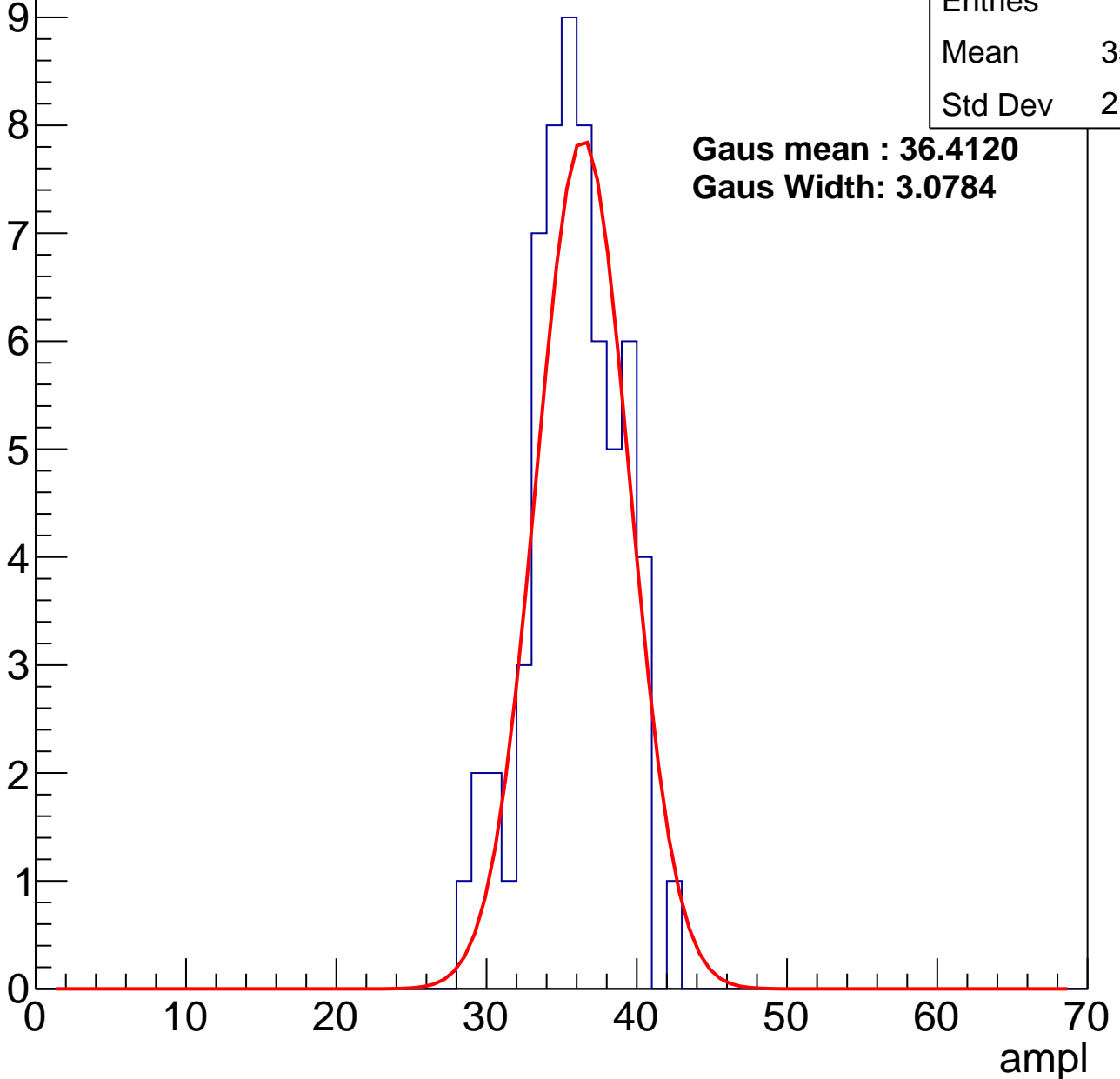
# B1L003S, U26-ch93, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	35.35
Std Dev	2.993

**Gaus mean : 36.4120**  
**Gaus Width: 3.0784**



# B1L003S, U26-ch93, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	80
Mean	42.4
Std Dev	3.488

**Gaus mean : 42.9010**

**Gaus Width: 3.8570**

10

8

6

4

2

0

0

10

20

30

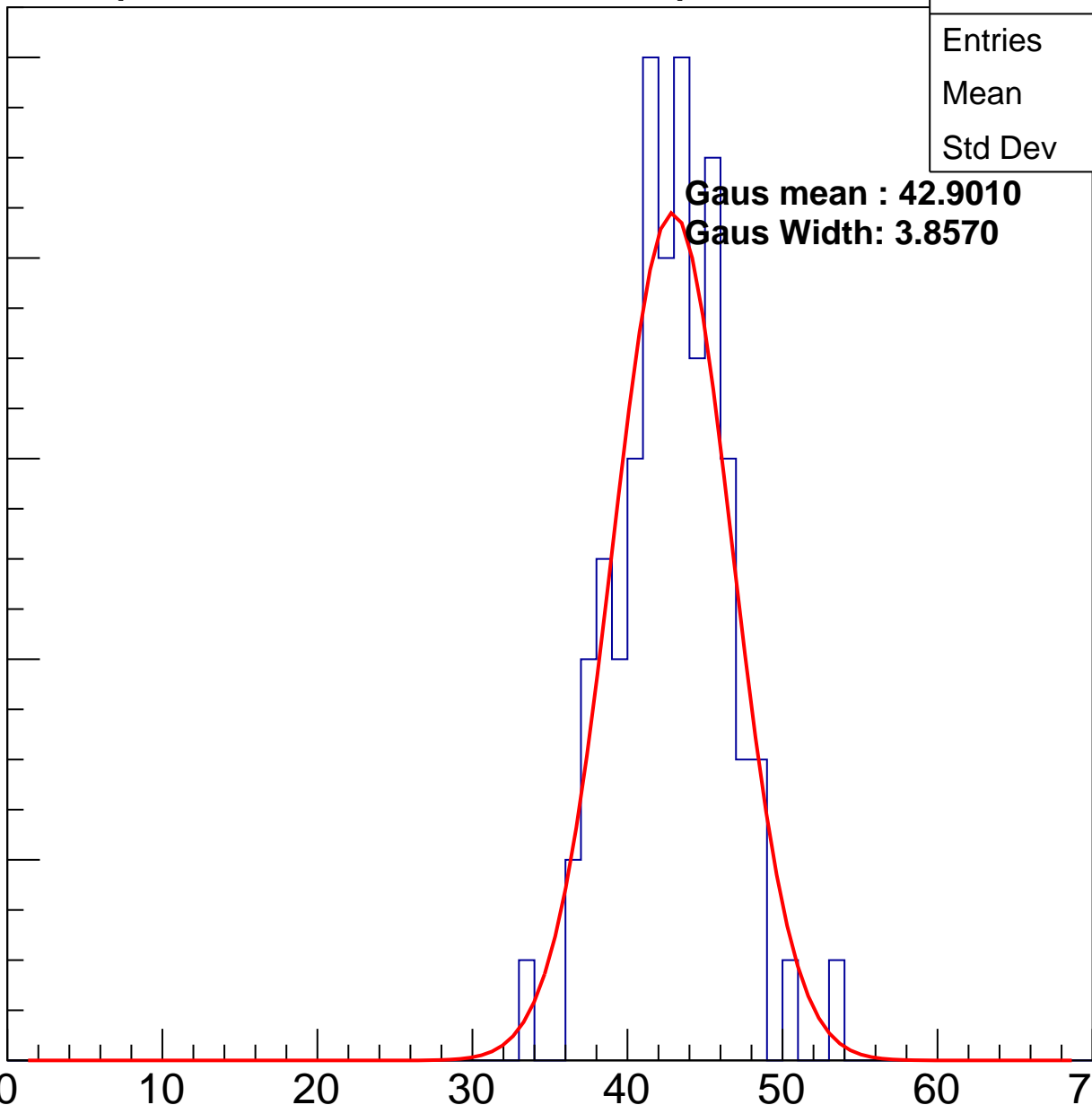
40

50

60

70

ampl

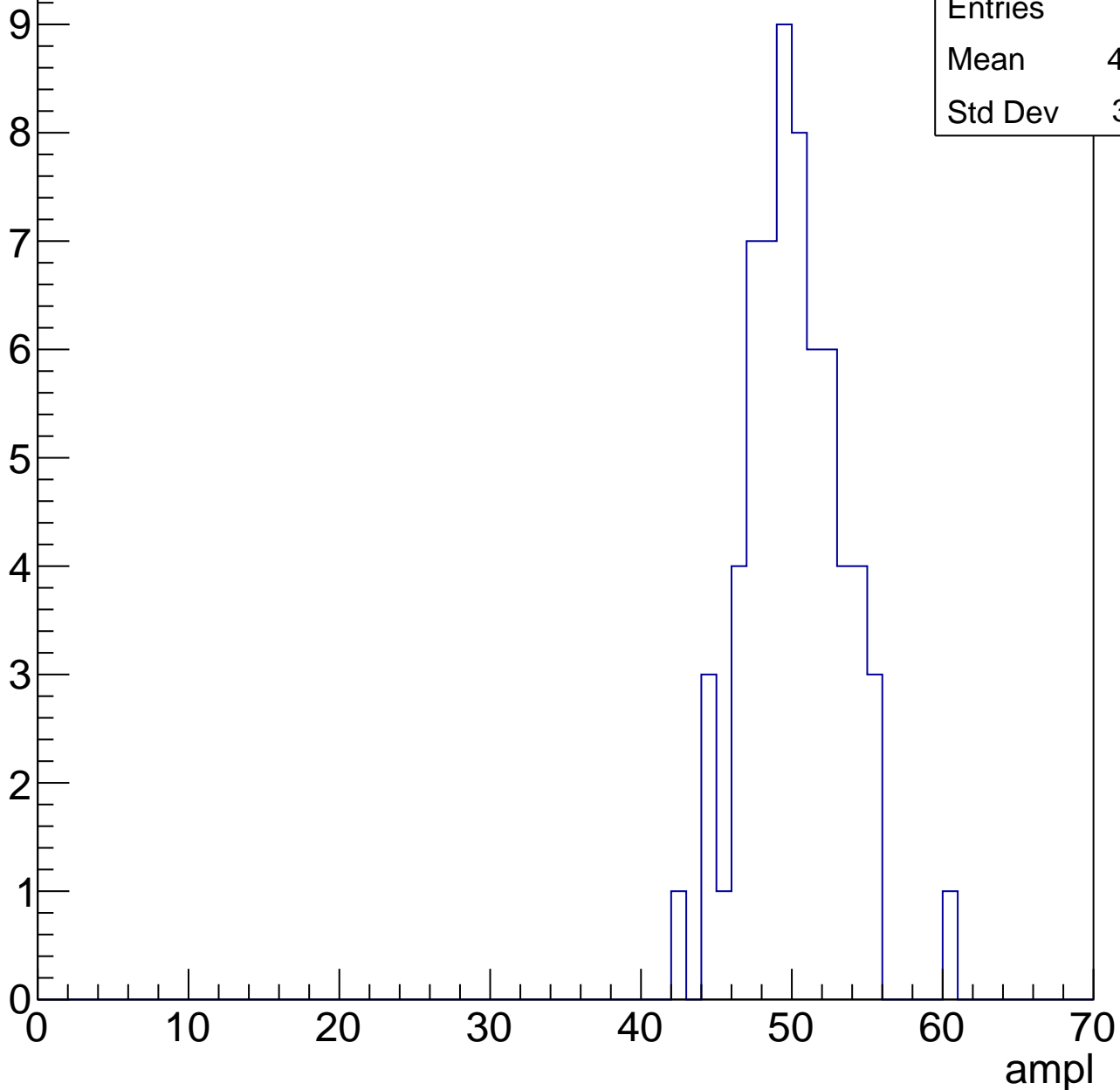


# B1L003S, U26-ch93, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	49.69
Std Dev	3.211

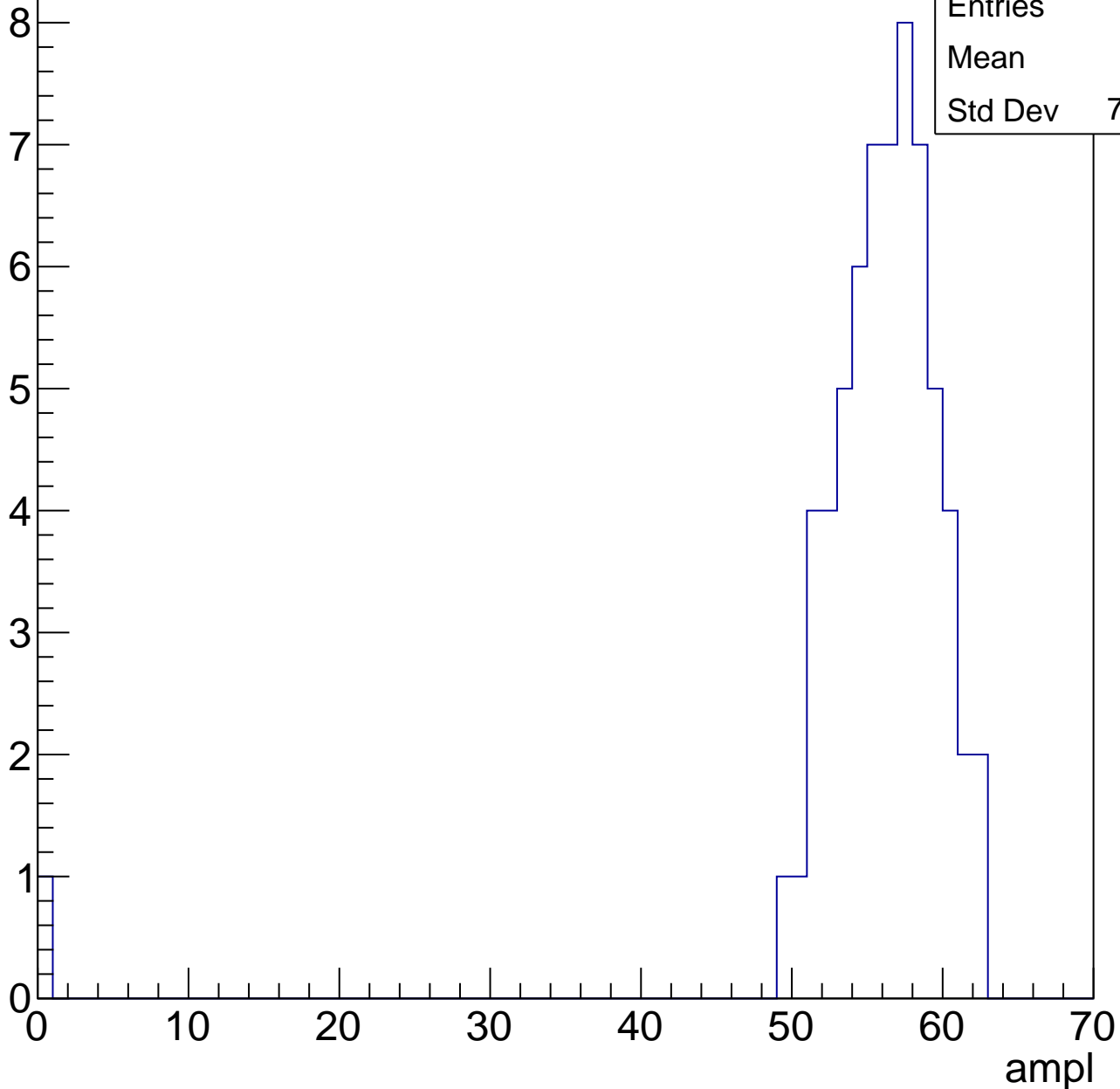


# B1L003S, U26-ch93, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	55
Std Dev	7.566

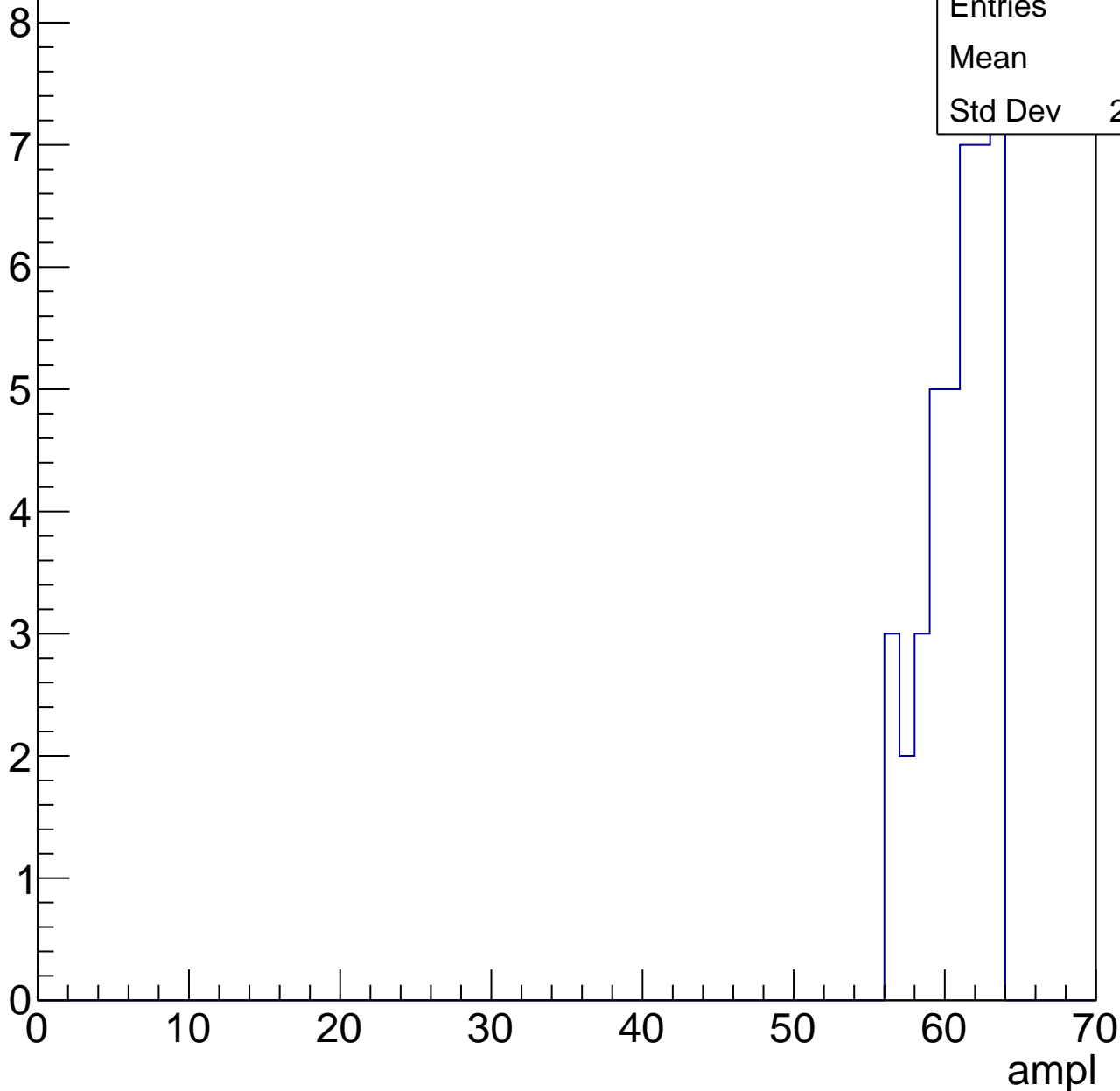


# B1L003S, U26-ch93, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	40
Mean	60.4
Std Dev	2.142



# B1L003S, U26-ch93, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	62.25
Std Dev	0.8292

ampl

0 10 20 30 40 50 60 70



# B1L003S, U26-ch93, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U26-ch94, adc0

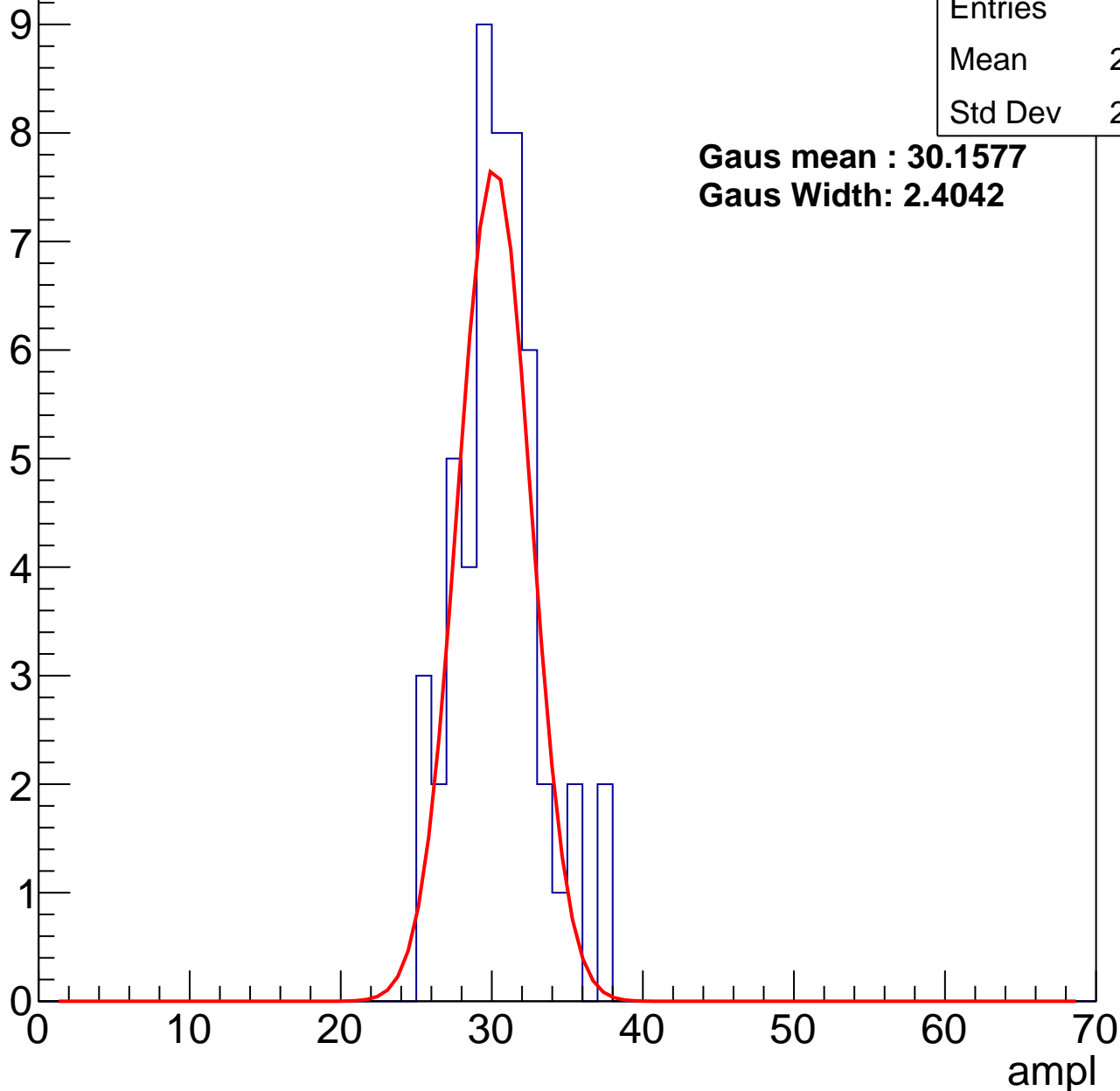
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	52
Mean	29.98
Std Dev	2.742

**Gaus mean : 30.1577**

**Gaus Width: 2.4042**



# B1L003S, U26-ch94, adc1

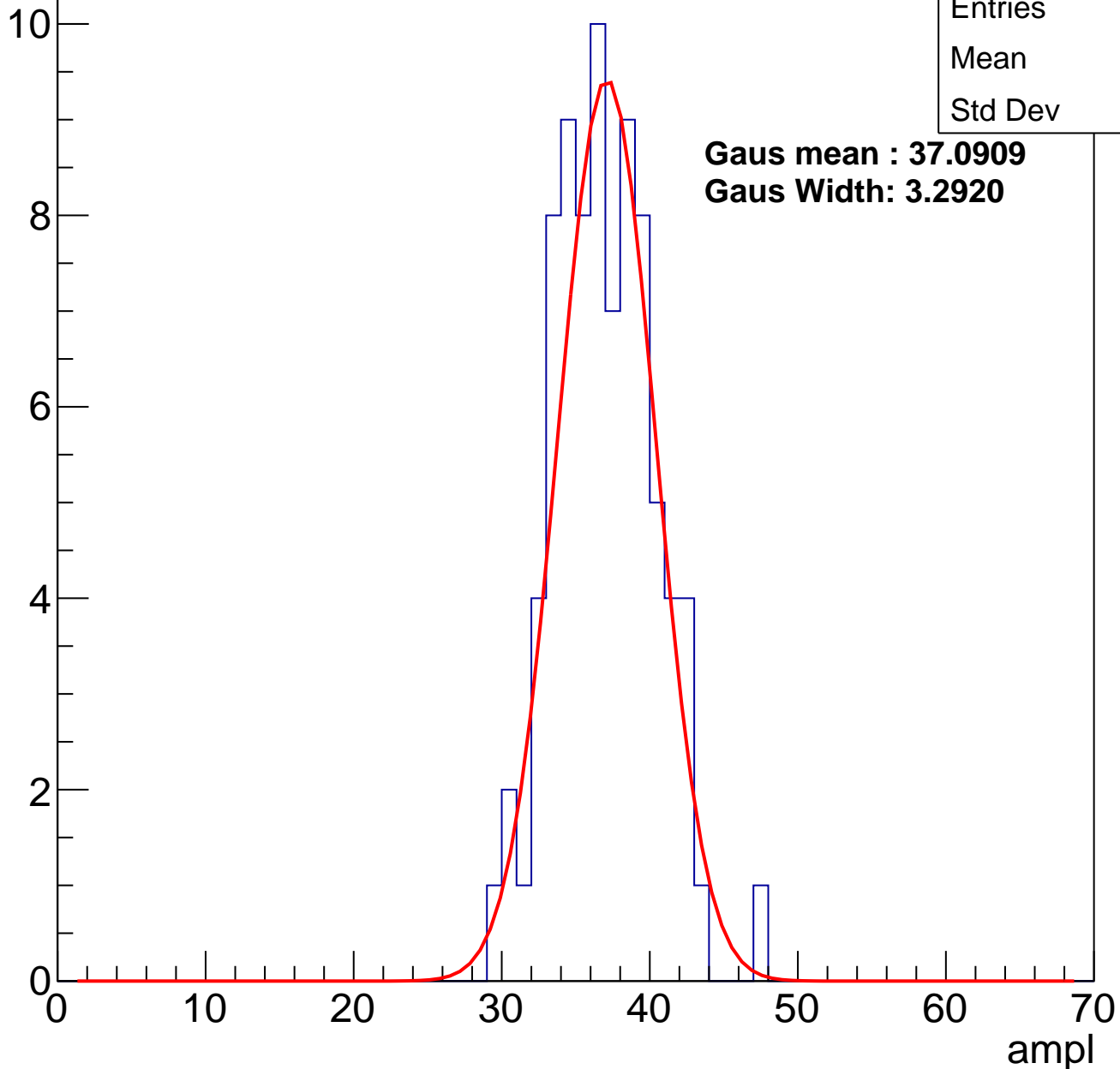
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	82
Mean	36.5
Std Dev	3.34

**Gaus mean : 37.0909**

**Gaus Width: 3.2920**

Entry



# B1L003S, U26-ch94, adc2

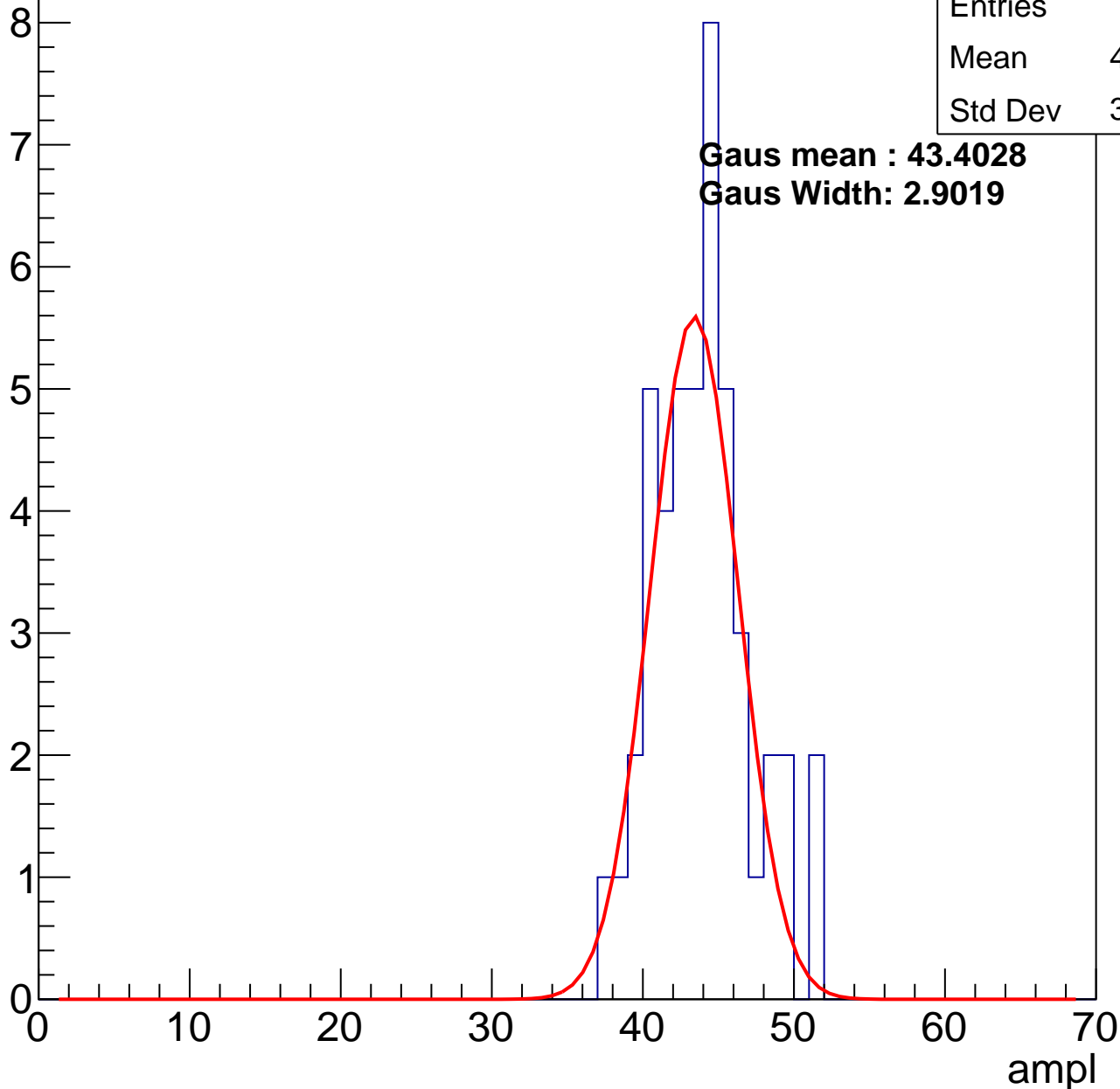
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	46
Mean	43.48
Std Dev	3.195

**Gaus mean : 43.4028**

**Gaus Width: 2.9019**

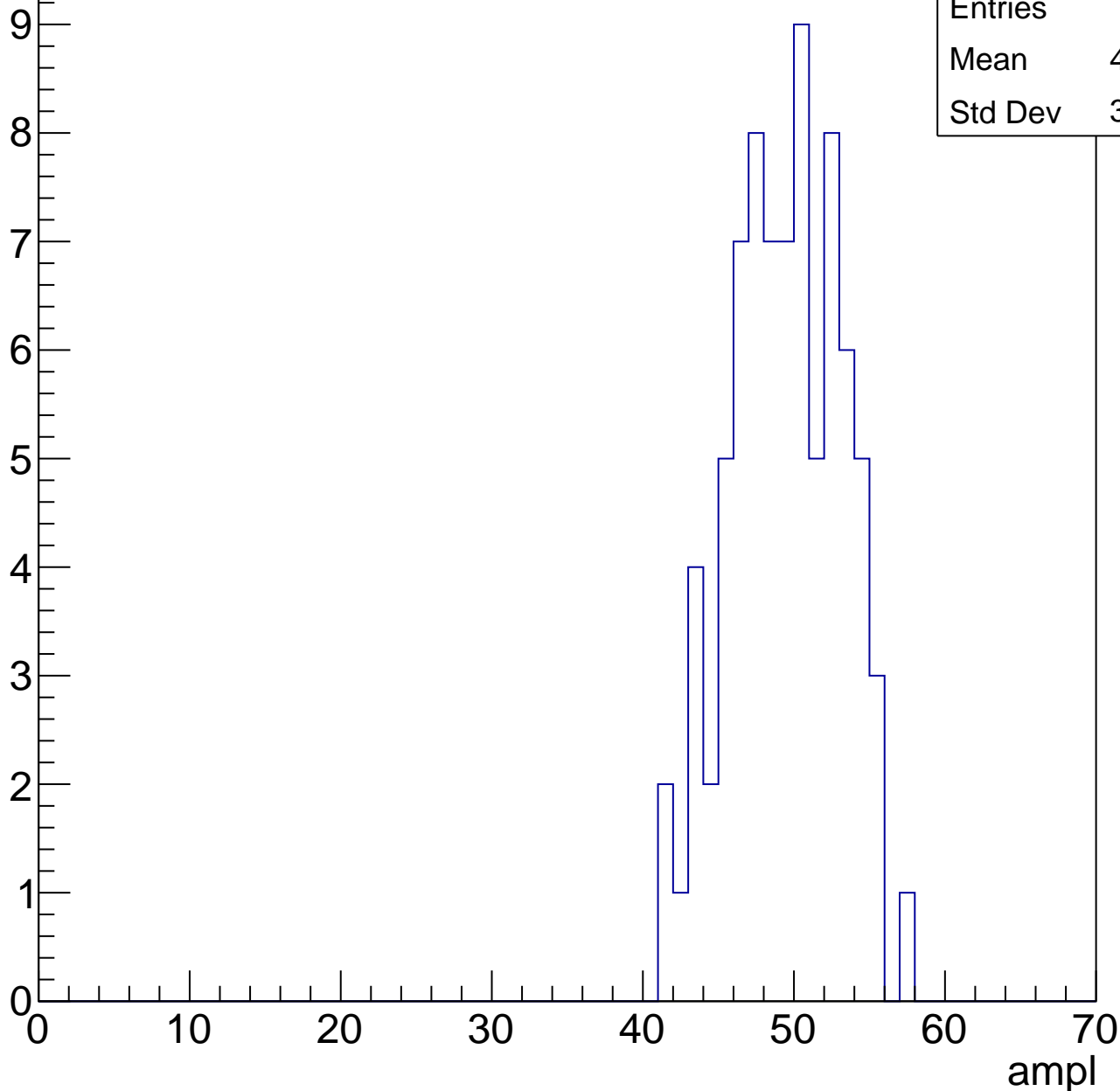


# B1L003S, U26-ch94, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	80
Mean	48.96
Std Dev	3.617

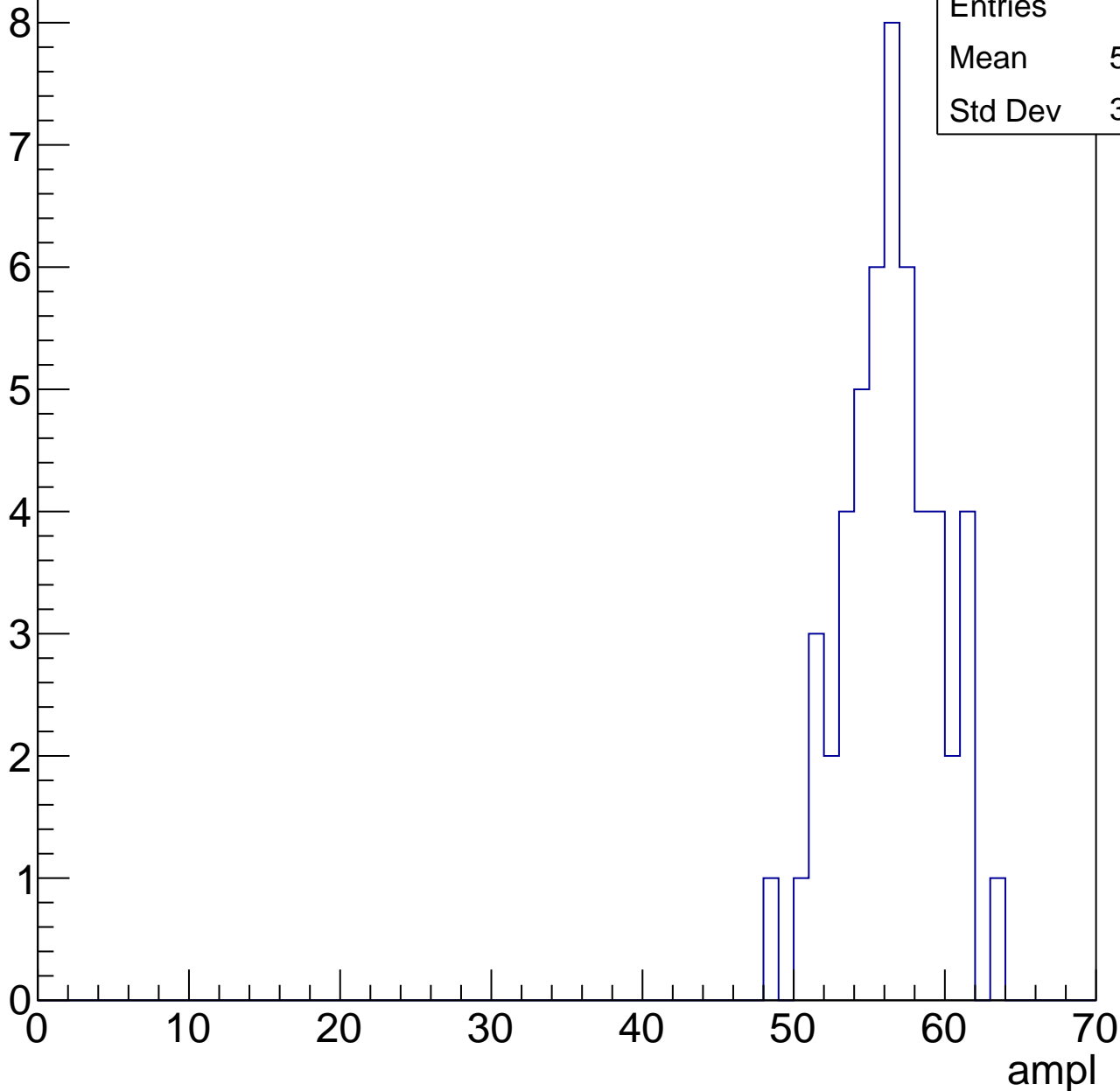


# B1L003S, U26-ch94, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

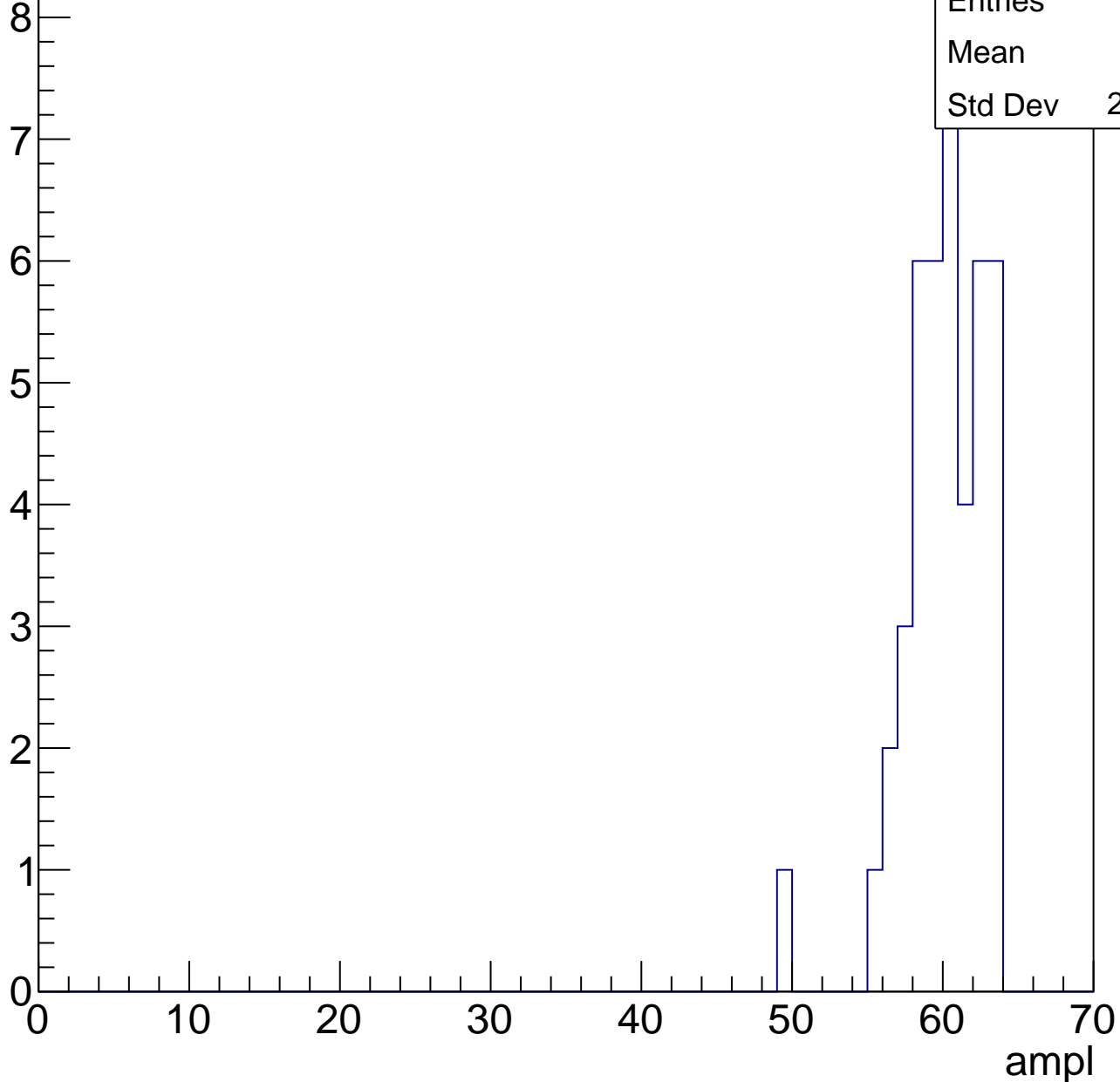
Entries	51
Mean	55.92
Std Dev	3.155



# B1L003S, U26-ch94, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

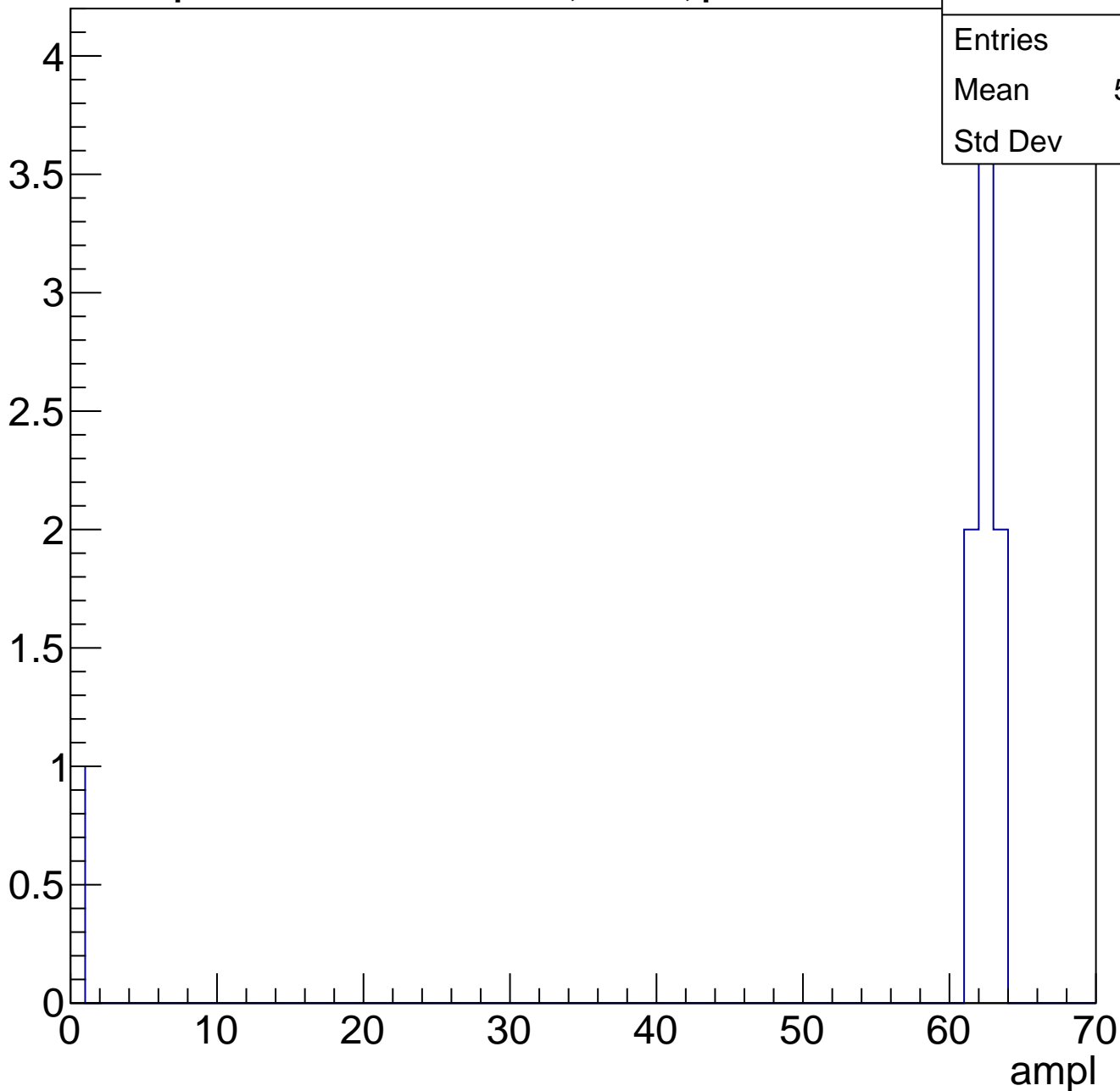
Entry



# B1L003S, U26-ch94, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch94, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U26-ch95, adc0

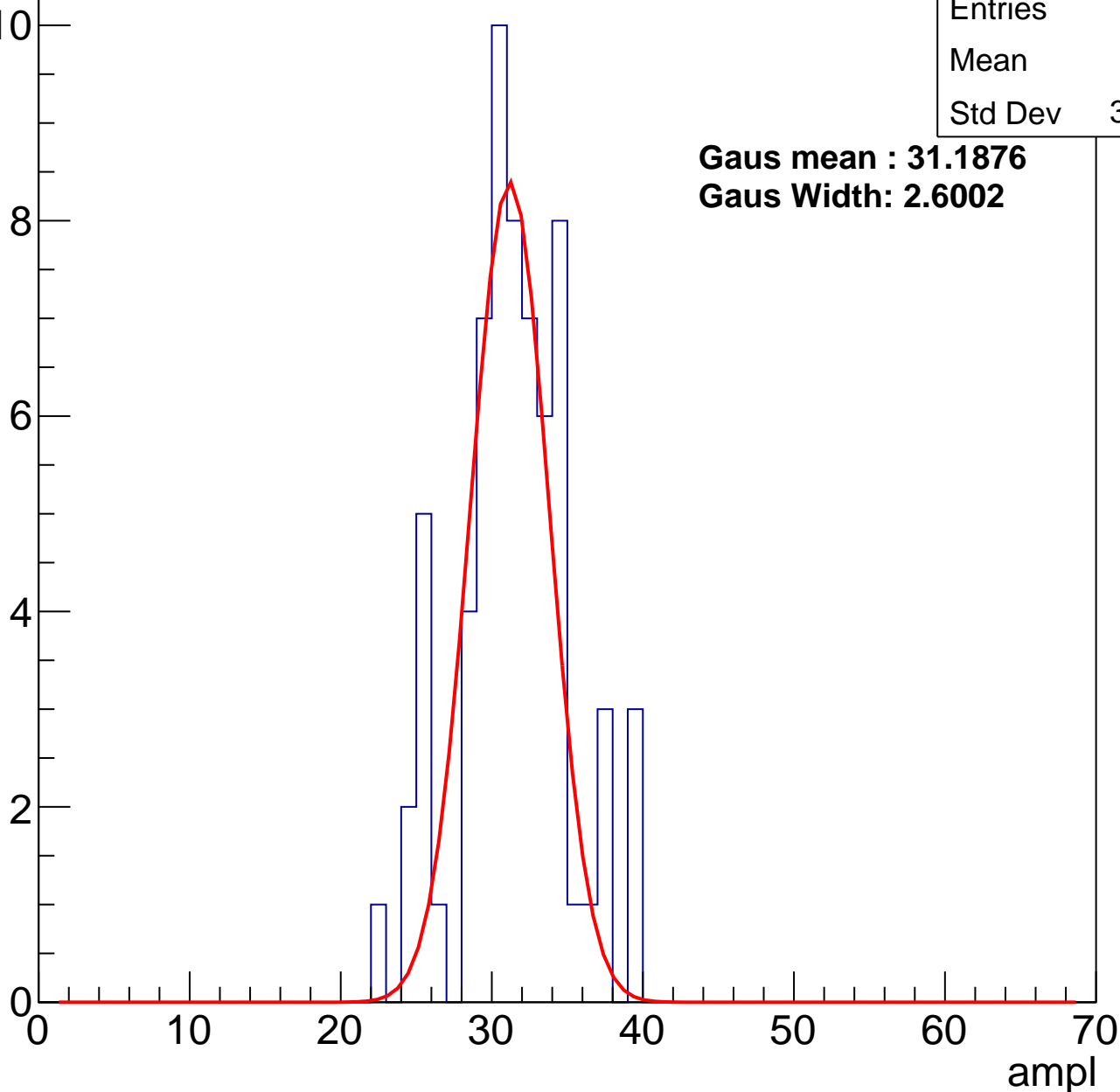
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	31
Std Dev	3.669

**Gaus mean : 31.1876**

**Gaus Width: 2.6002**



# B1L003S, U26-ch95, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	62
Mean	37.26
Std Dev	2.862

**Gaus mean : 37.8025**

**Gaus Width: 2.9909**

Entry

10

8

6

4

2

0

0

10

20

30

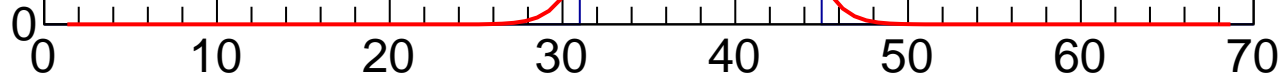
40

50

60

70

ampl



# B1L003S, U26-ch95, adc2

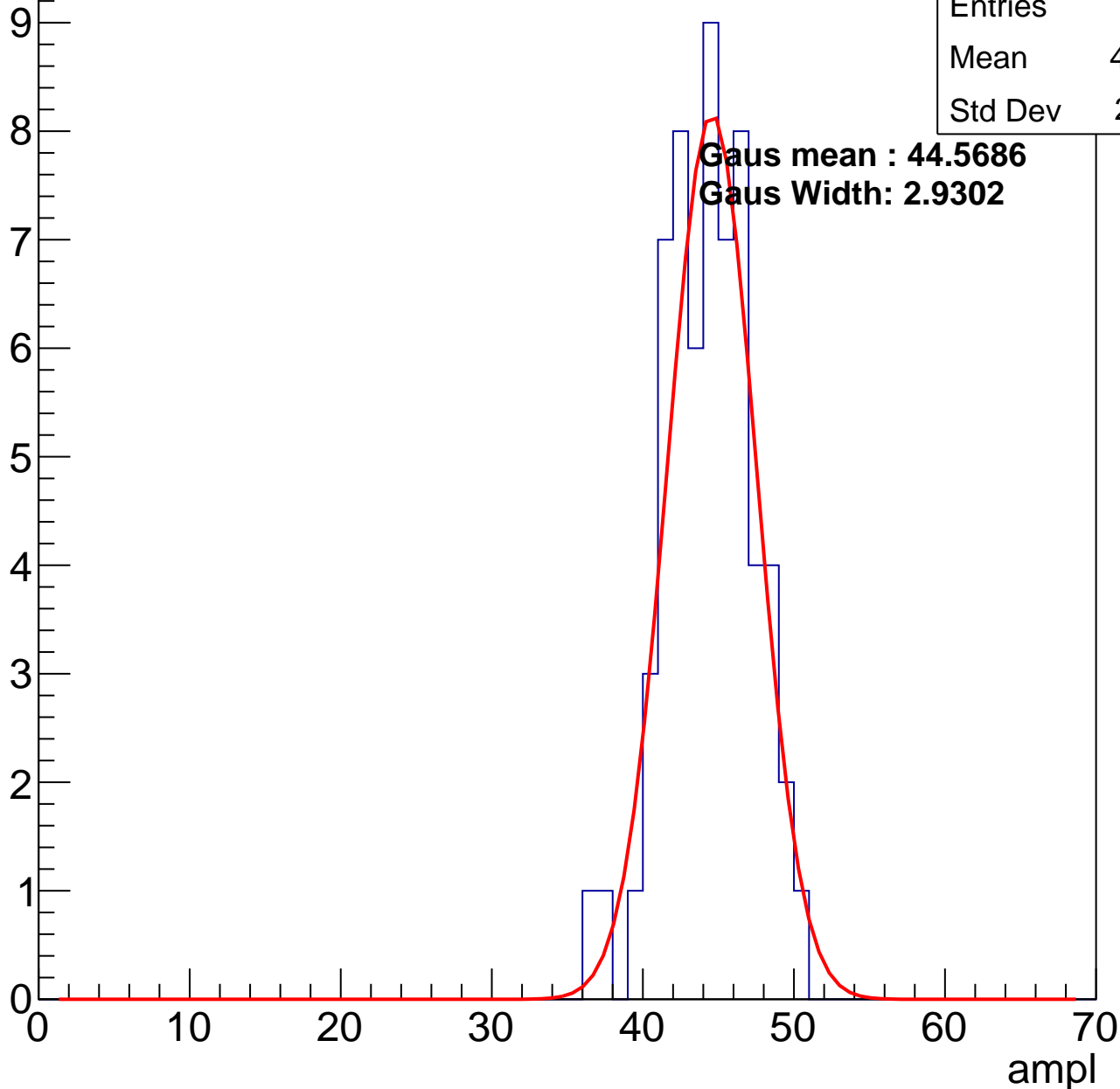
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	43.87
Std Dev	2.871

**Gaus mean : 44.5686**

**Gaus Width: 2.9302**

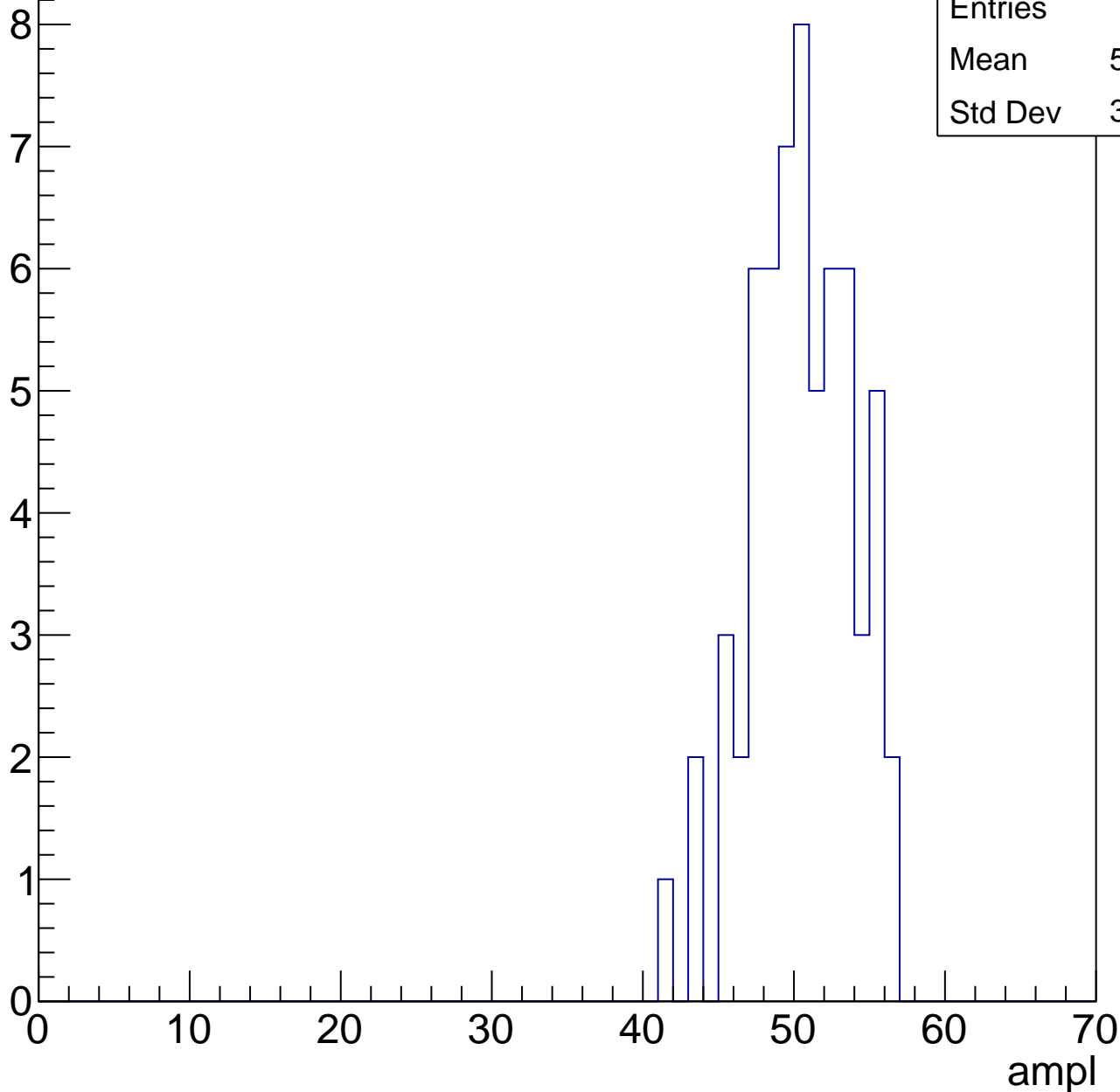


# B1L003S, U26-ch95, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	50.02
Std Dev	3.358

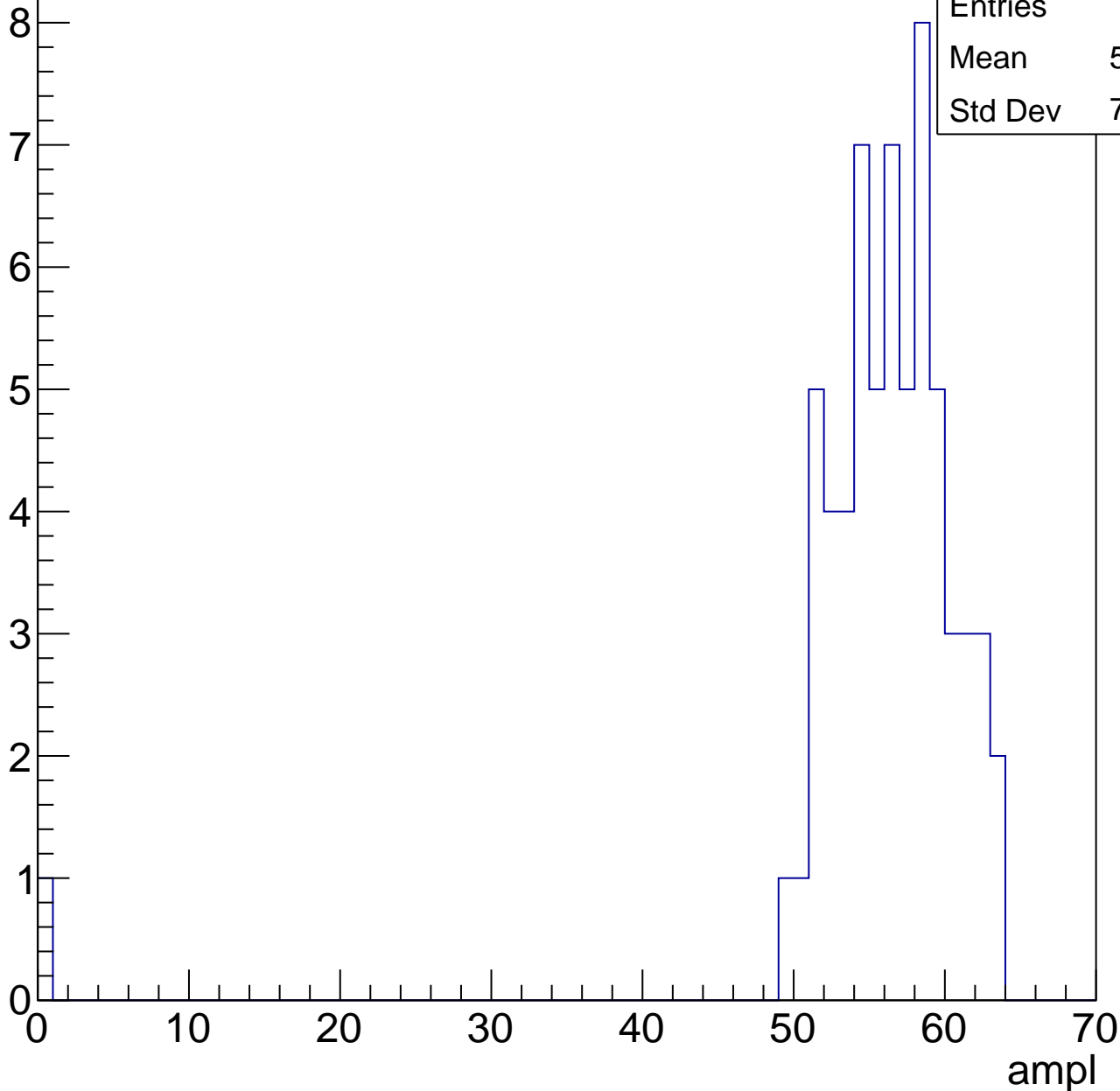


# B1L003S, U26-ch95, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	55.28
Std Dev	7.763



# B1L003S, U26-ch95, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

7  
6  
5  
4  
3  
2  
1  
0

Entries	41
Mean	60.34
Std Dev	2.02

ampl

0 10 20 30 40 50 60 70

0

1

2

3

4

5

6

7

# B1L003S, U26-ch95, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L003S, U26-ch95, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	63
Std Dev	0

# B1L003S, U26-ch96, adc0

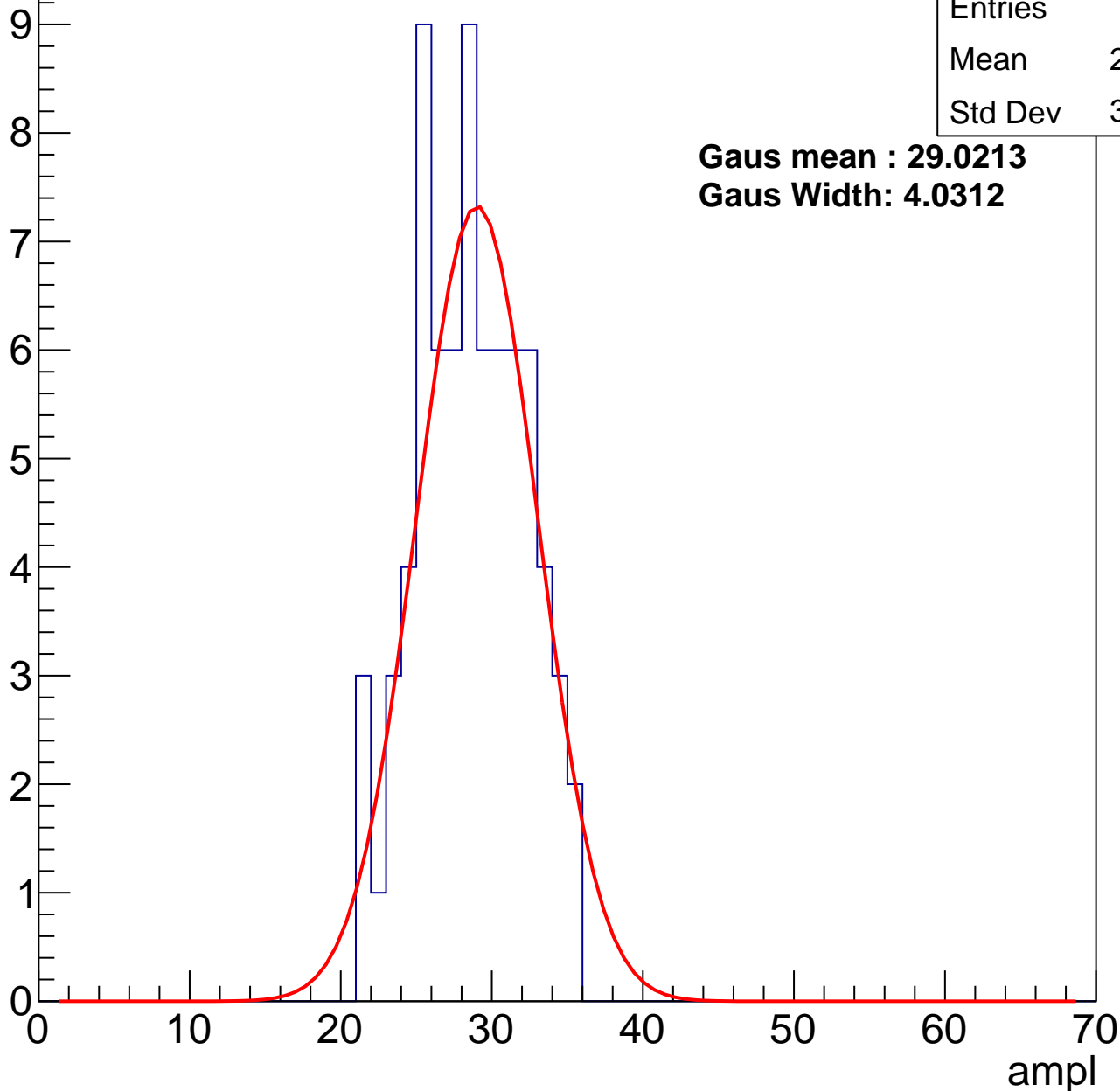
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	74
Mean	28.12
Std Dev	3.522

**Gaus mean : 29.0213**

**Gaus Width: 4.0312**



# B1L003S, U26-ch96, adc1

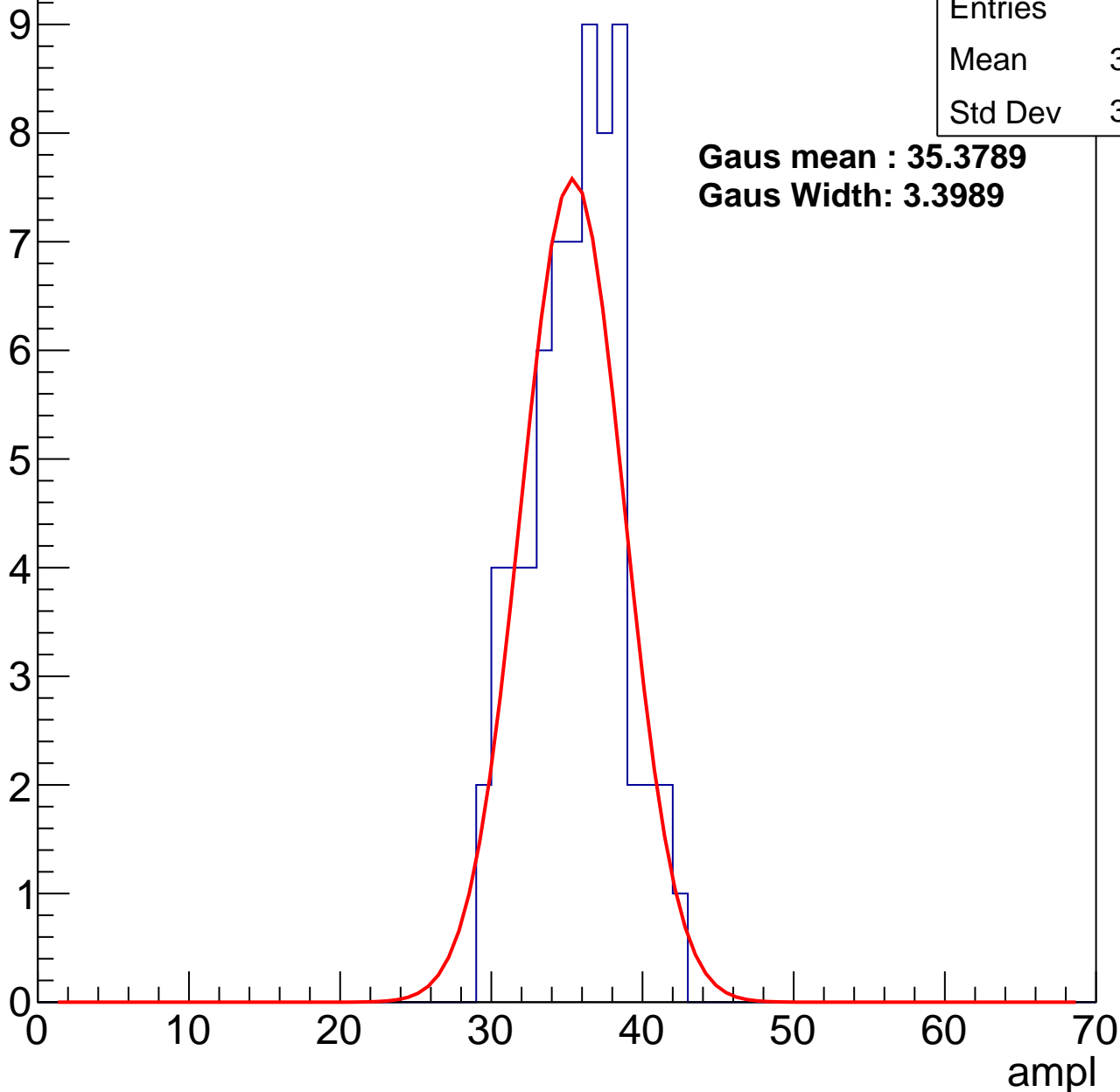
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	35.15
Std Dev	3.058

**Gaus mean : 35.3789**

**Gaus Width: 3.3989**



# B1L003S, U26-ch96, adc2

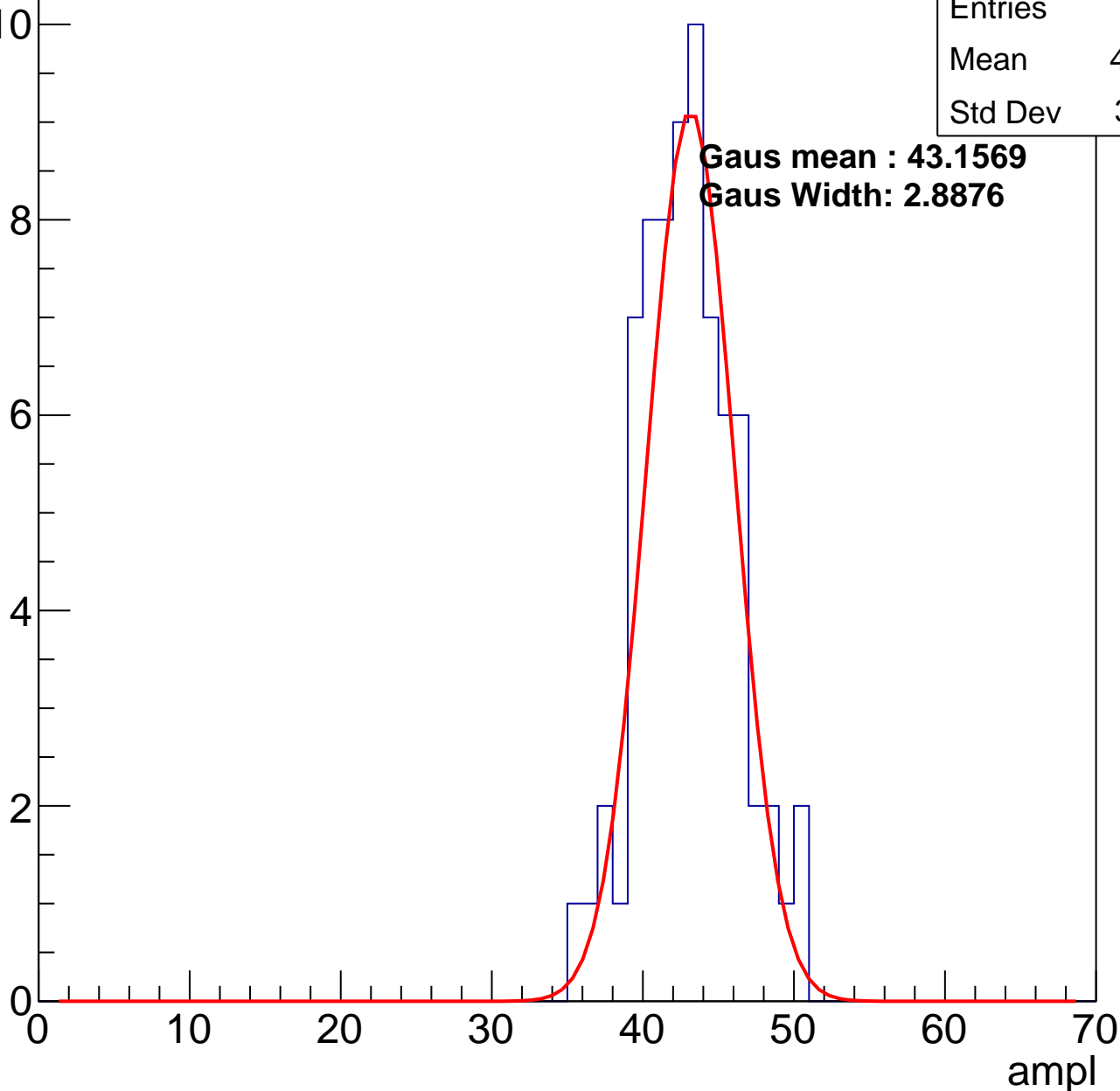
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	73
Mean	42.53
Std Dev	3.141

**Gaus mean : 43.1569**

**Gaus Width: 2.8876**

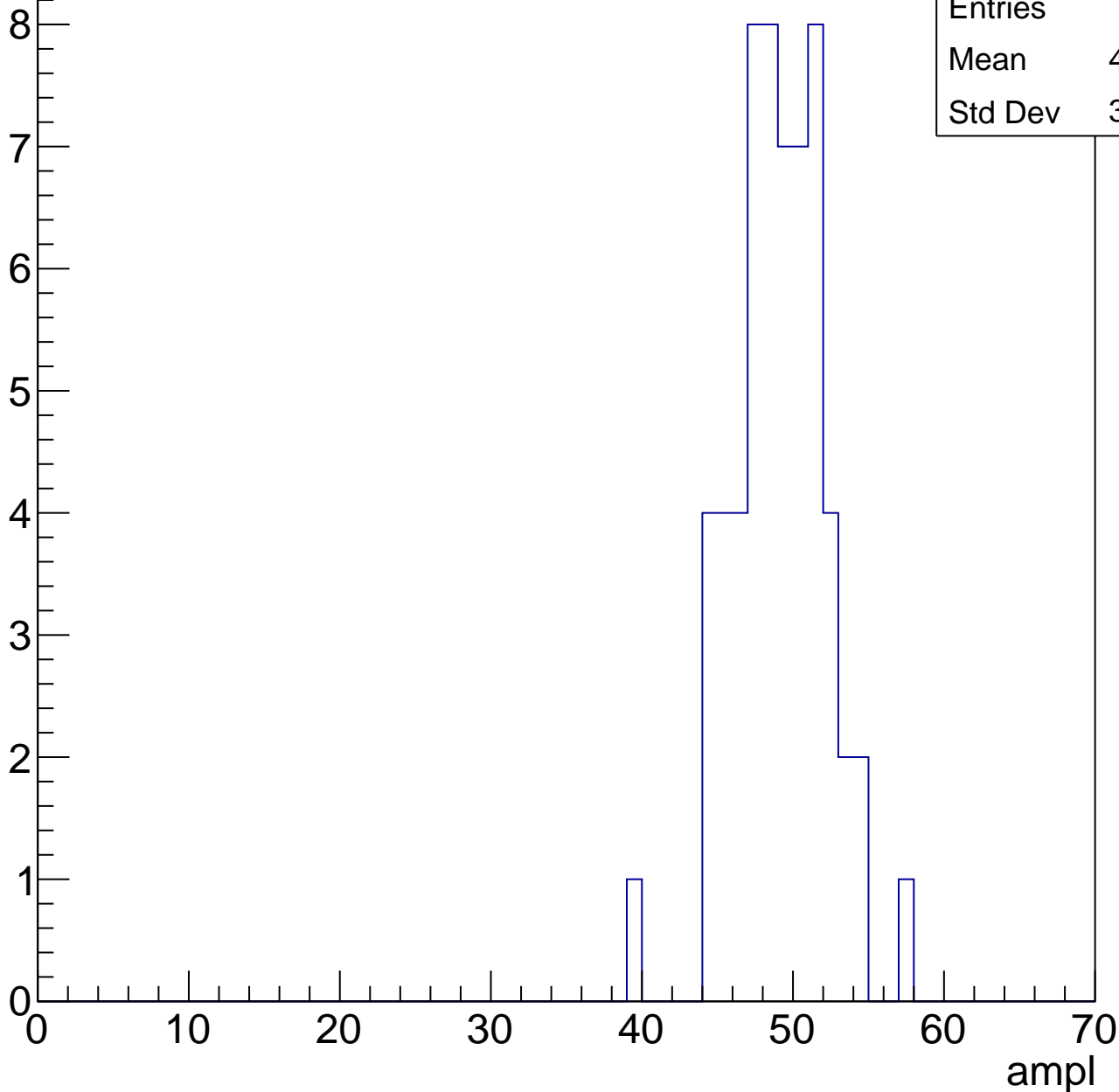


# B1L003S, U26-ch96, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

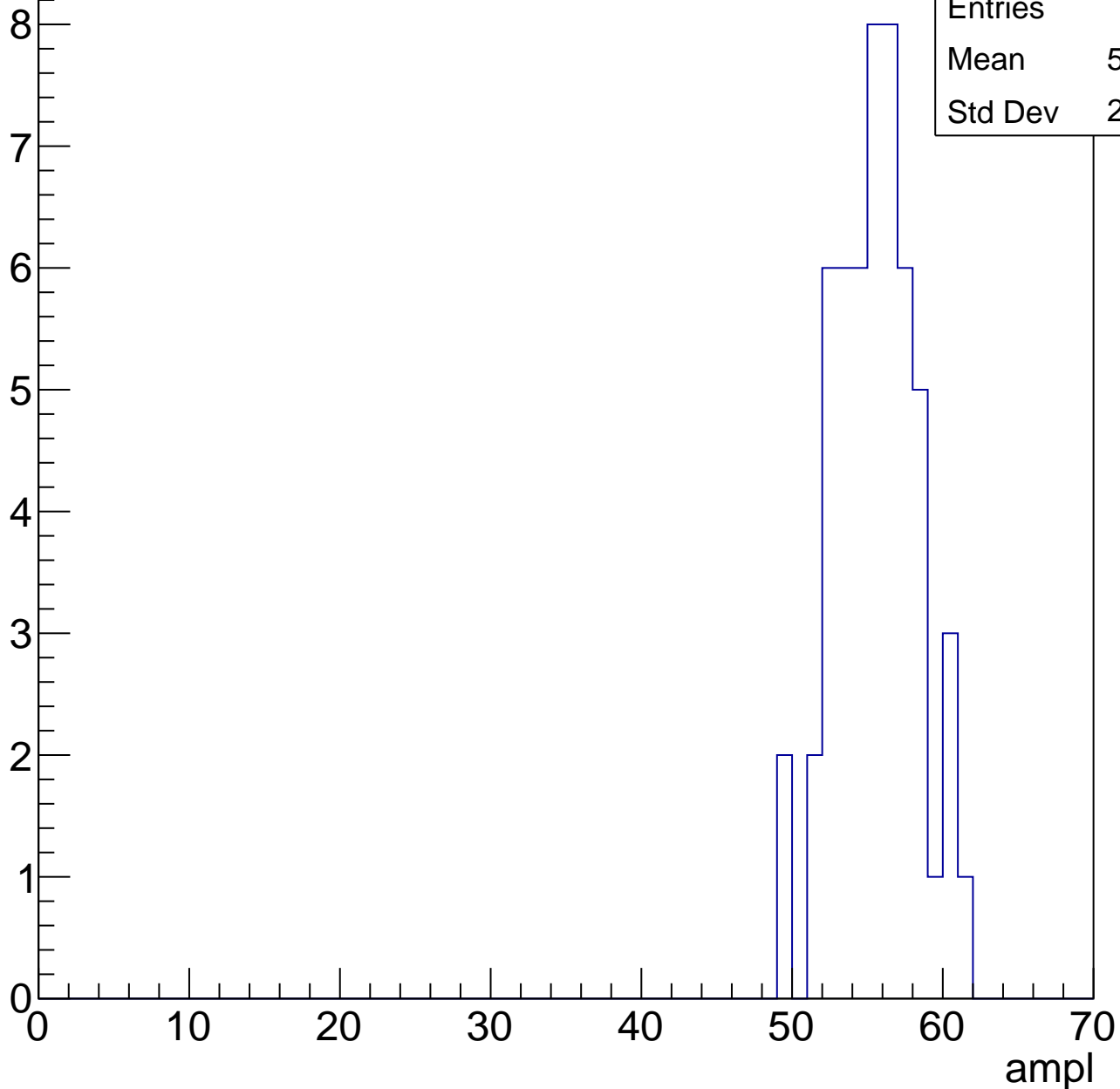
Entries	60
Mean	48.65
Std Dev	3.038



# B1L003S, U26-ch96, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

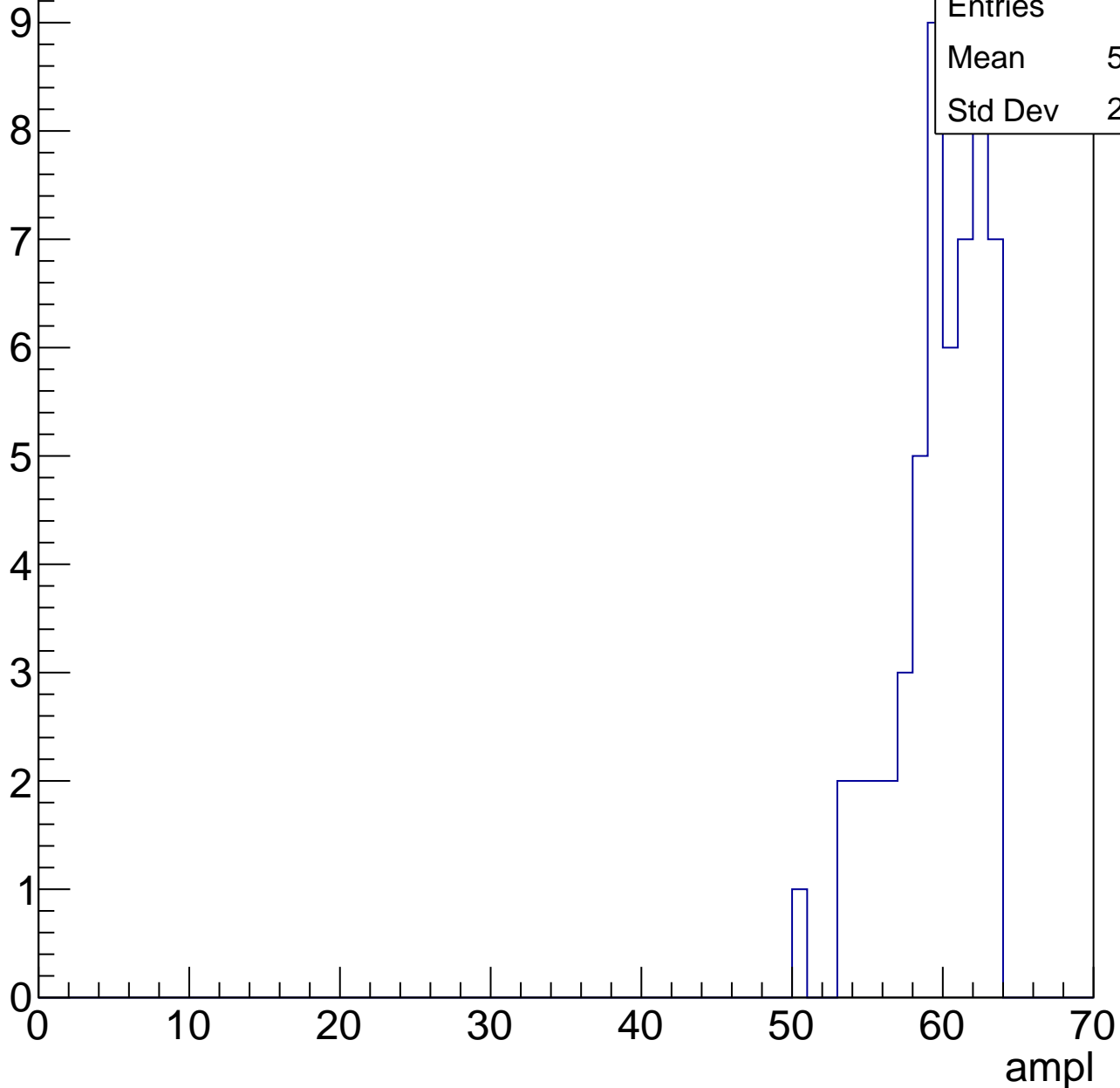


Entries	54
Mean	55.07
Std Dev	2.693

# B1L003S, U26-ch96, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U26-ch96, adc6

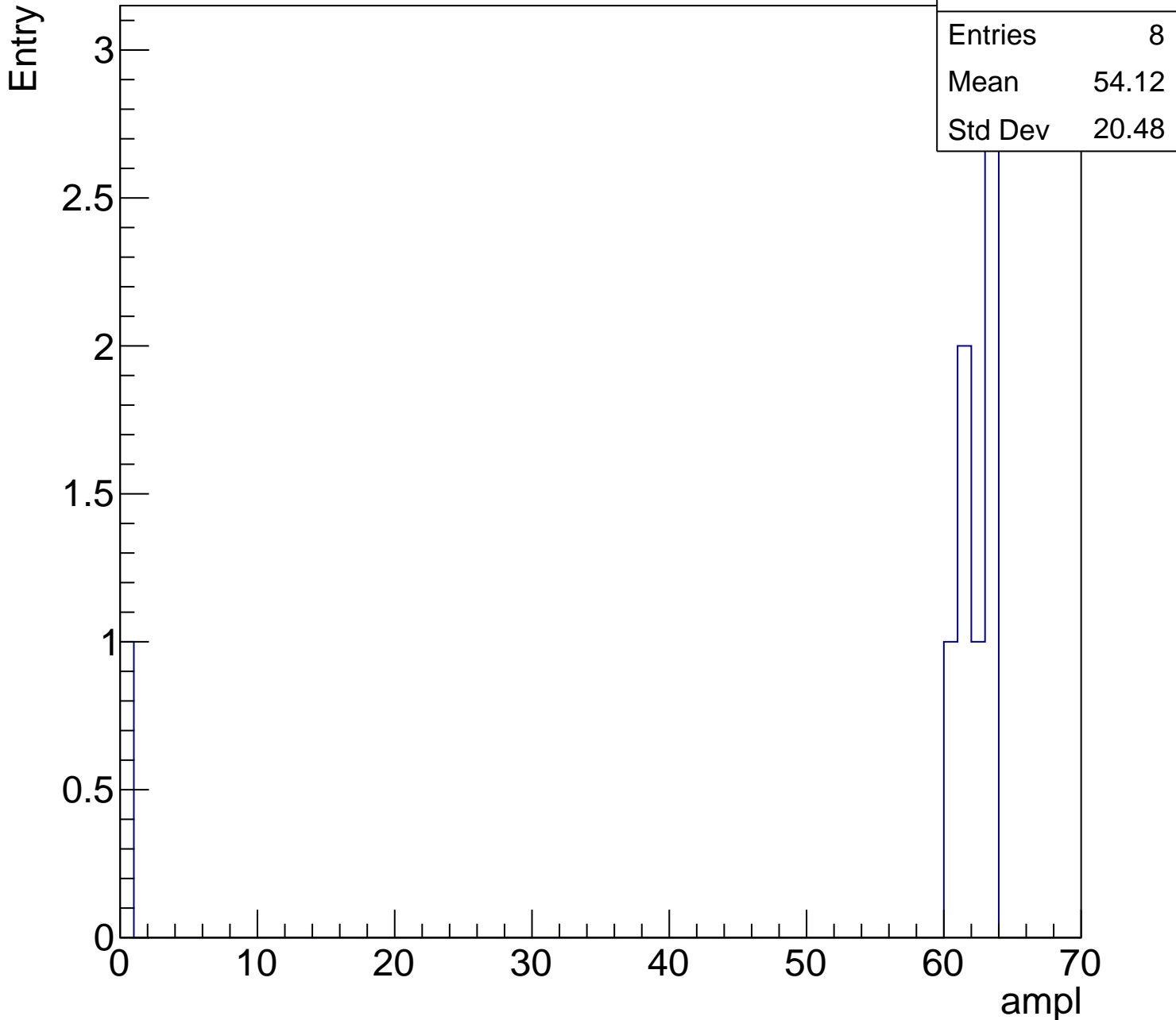
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

3  
2.5  
2  
1.5  
1  
0.5  
0

Entries	8
Mean	54.12
Std Dev	20.48

ampl





# B1L003S, U26-ch96, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U26-ch97, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	84
Mean	29.54
Std Dev	3.587

**Gaus mean : 29.7608**

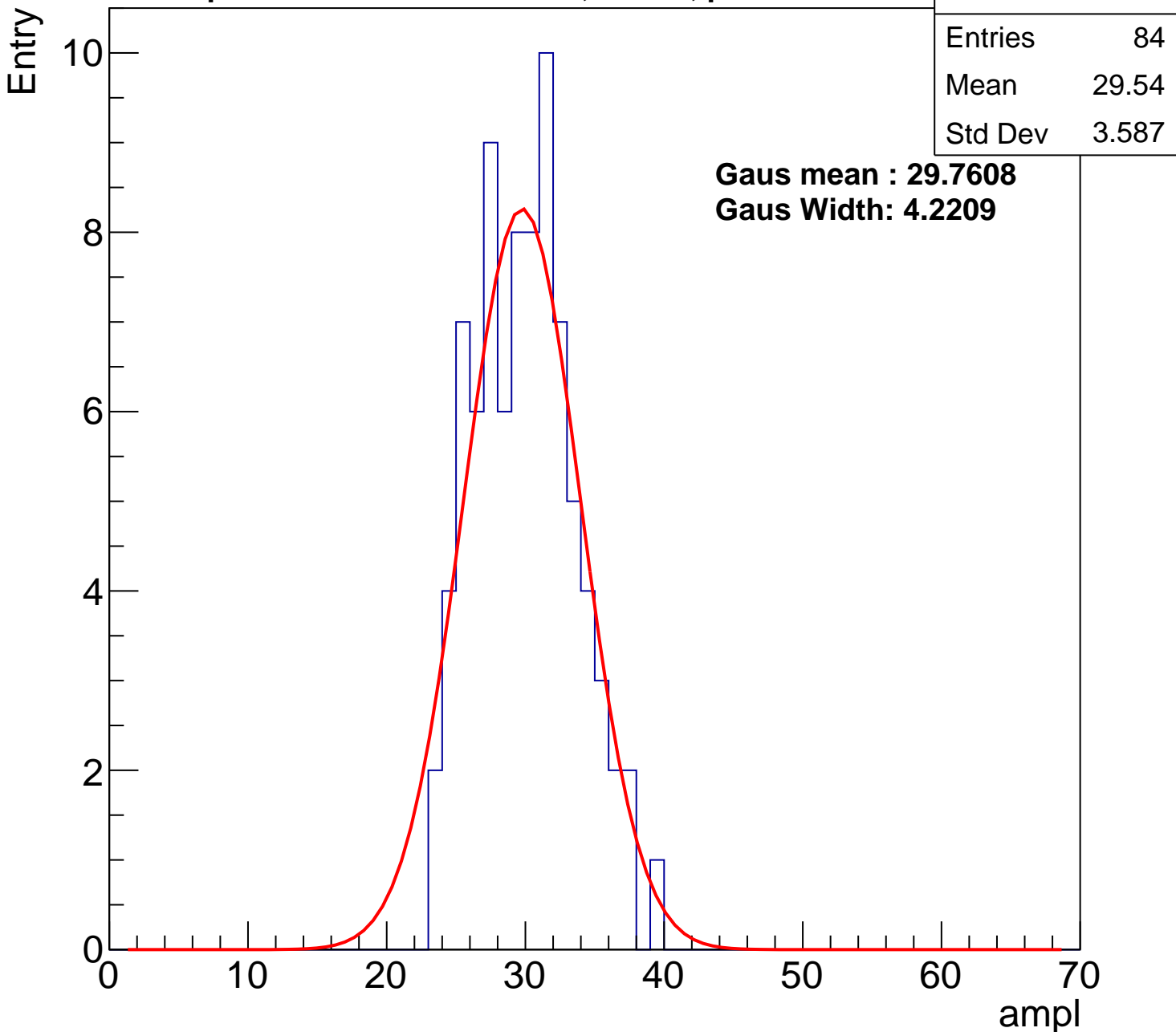
**Gaus Width: 4.2209**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U26-ch97, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	58
Mean	36.47
Std Dev	3.169

**Gaus mean : 36.1830**

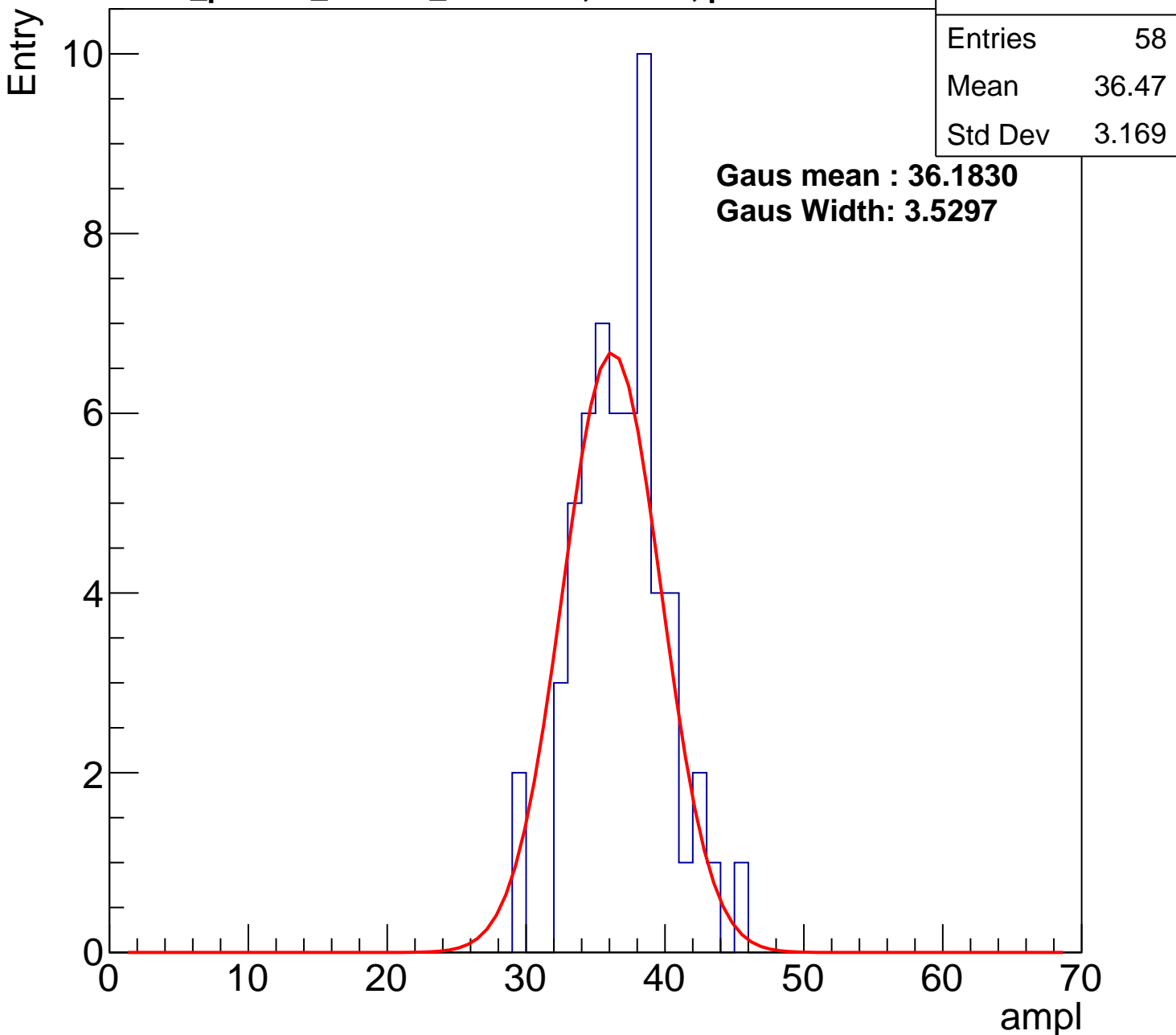
**Gaus Width: 3.5297**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U26-ch97, adc2

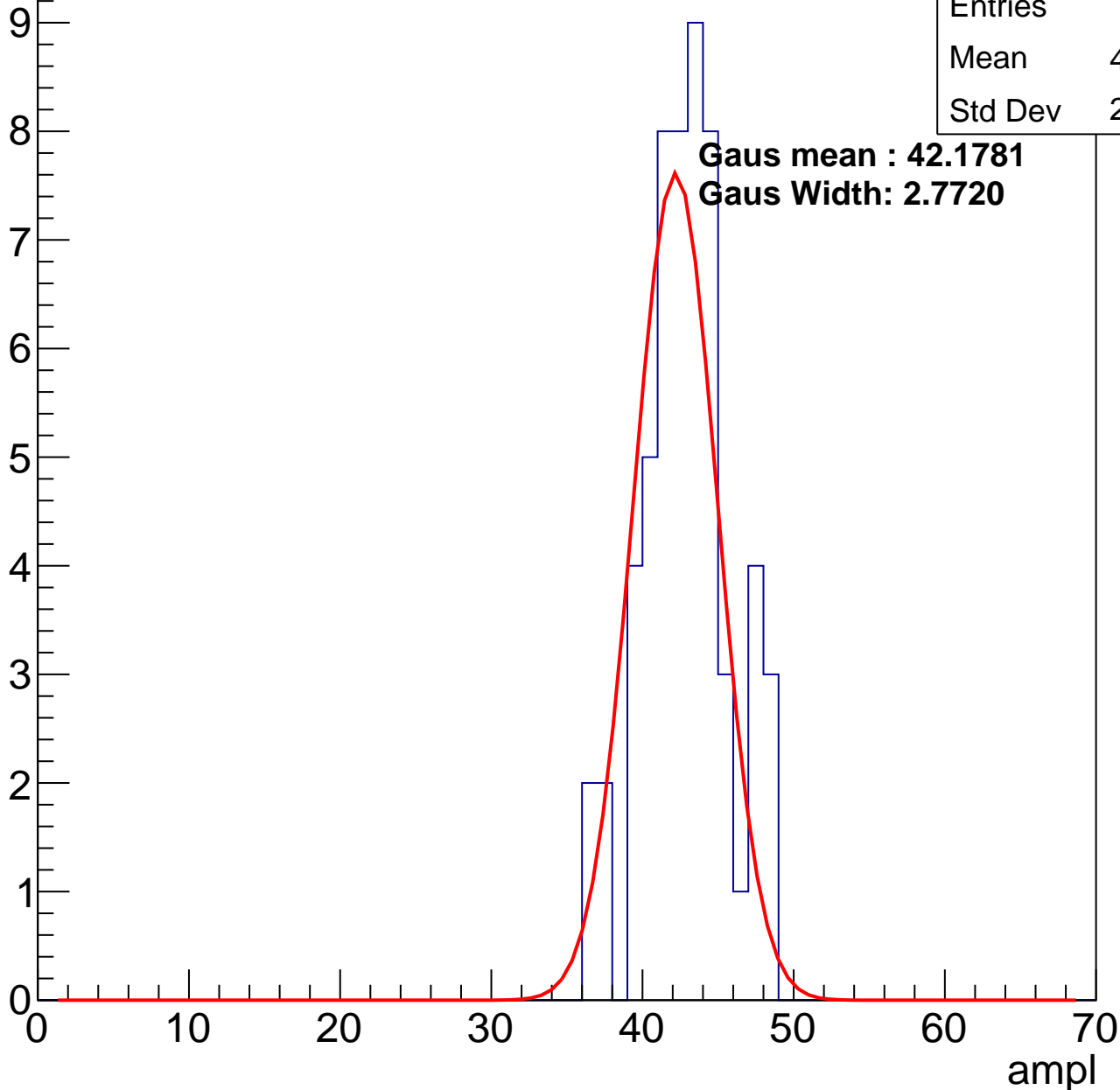
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	42.42
Std Dev	2.865

**Gaus mean : 42.1781**

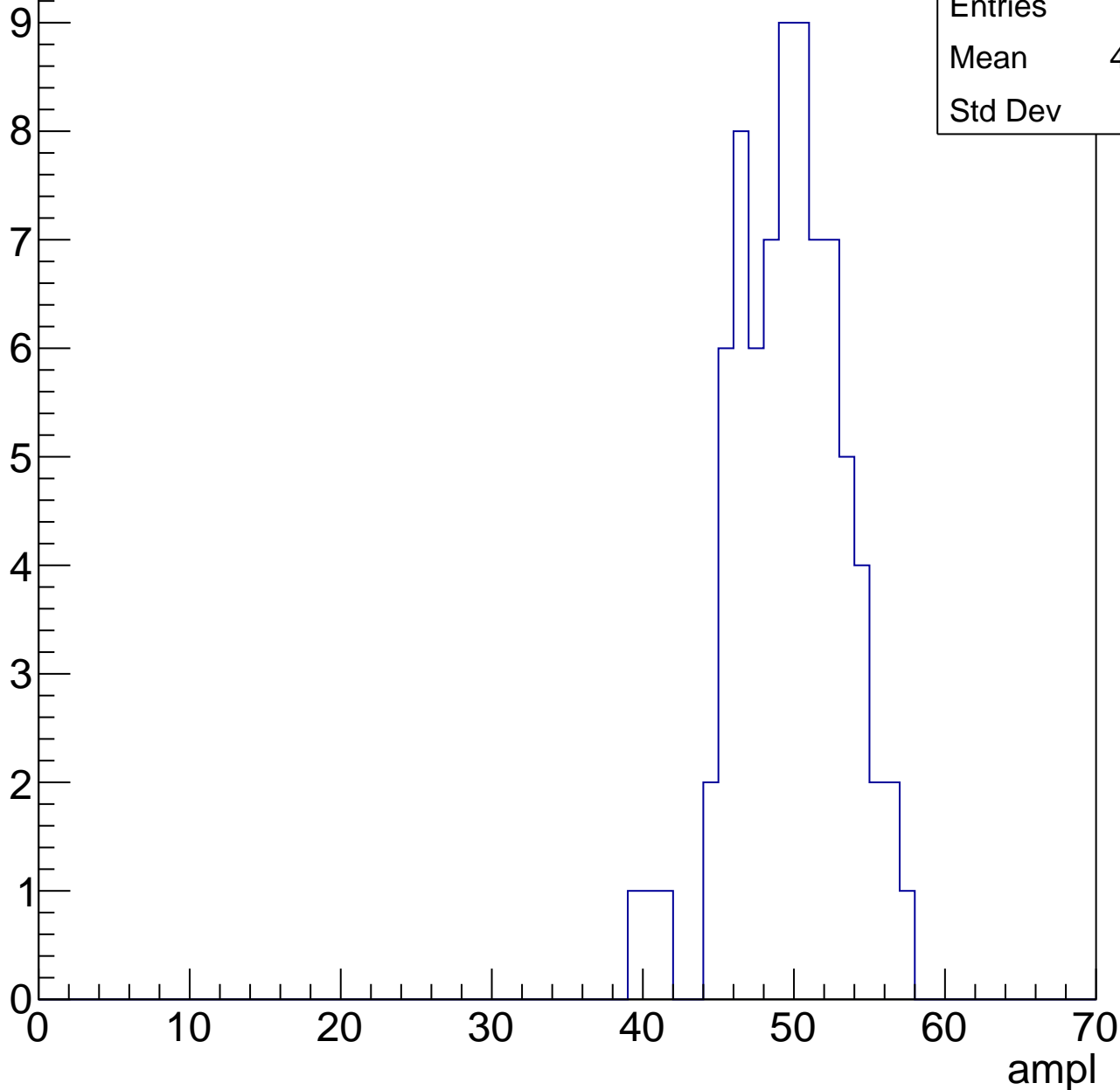
**Gaus Width: 2.7720**



# B1L003S, U26-ch97, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

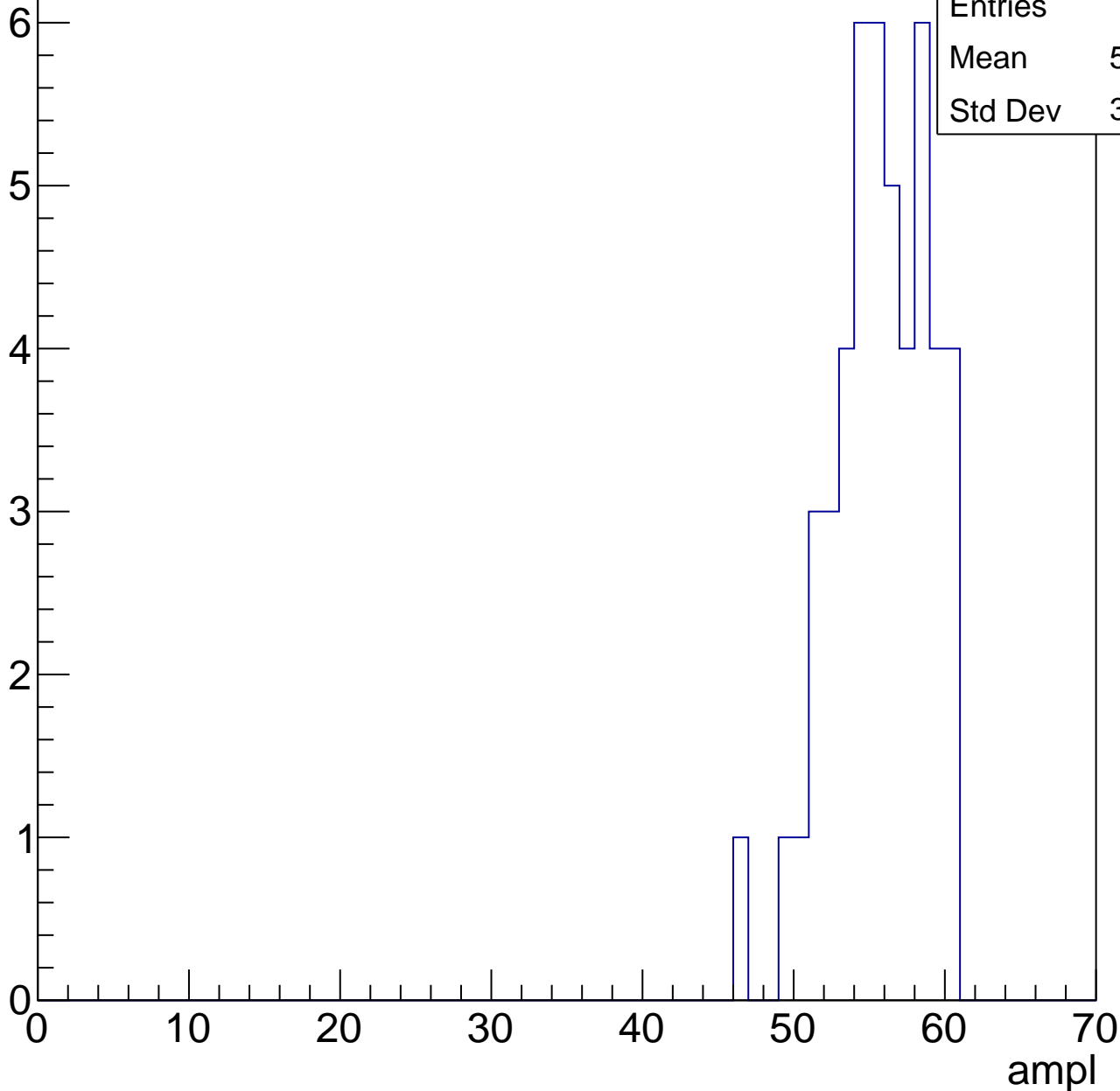


# B1L003S, U26-ch97, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	48
Mean	55.25
Std Dev	3.146



# B1L003S, U26-ch97, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

10

8

6

4

2

0

0

10

20

30

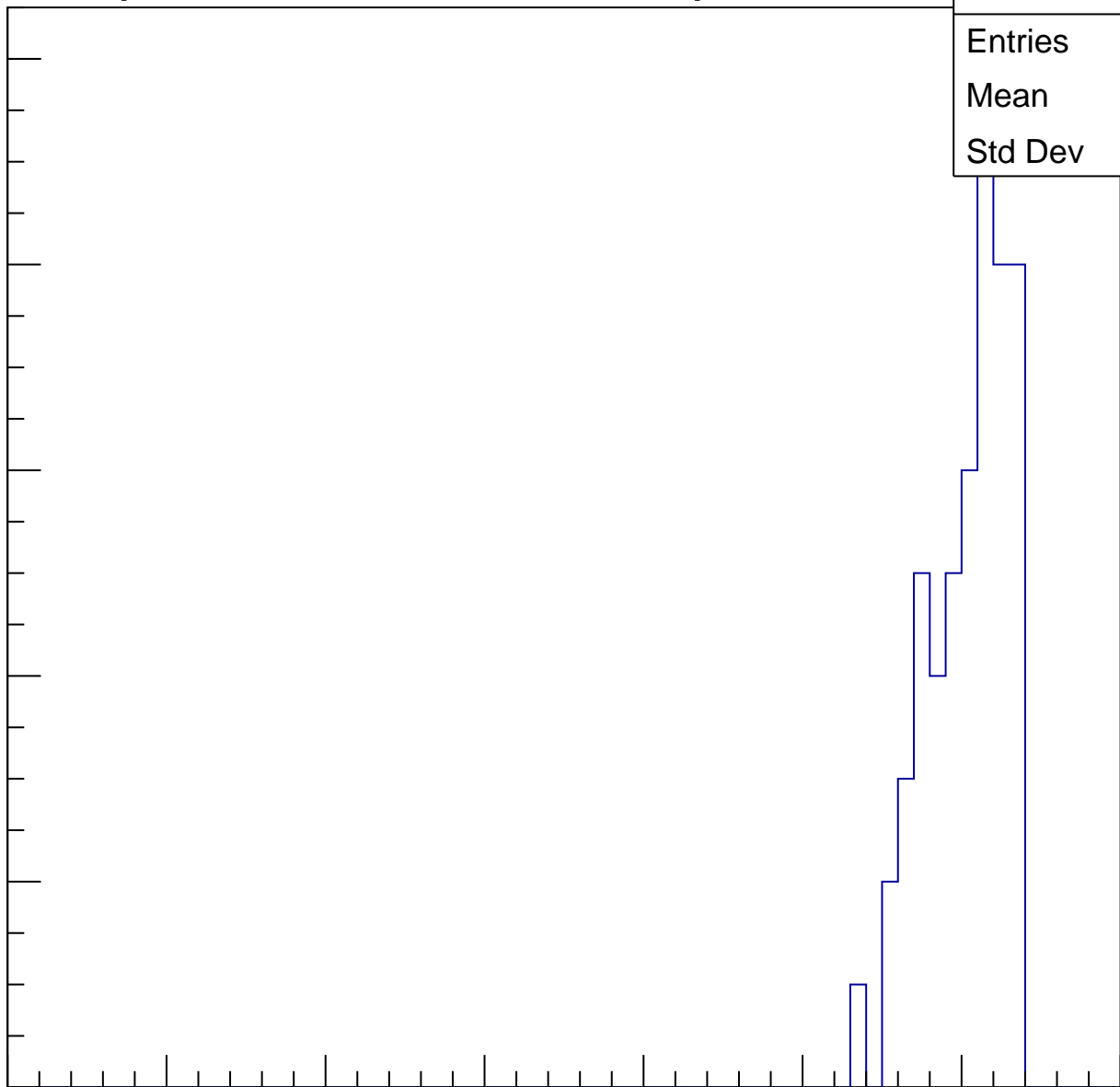
40

50

60

ampl

Entries	52
Mean	59.87
Std Dev	2.504



# B1L003S, U26-ch97, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

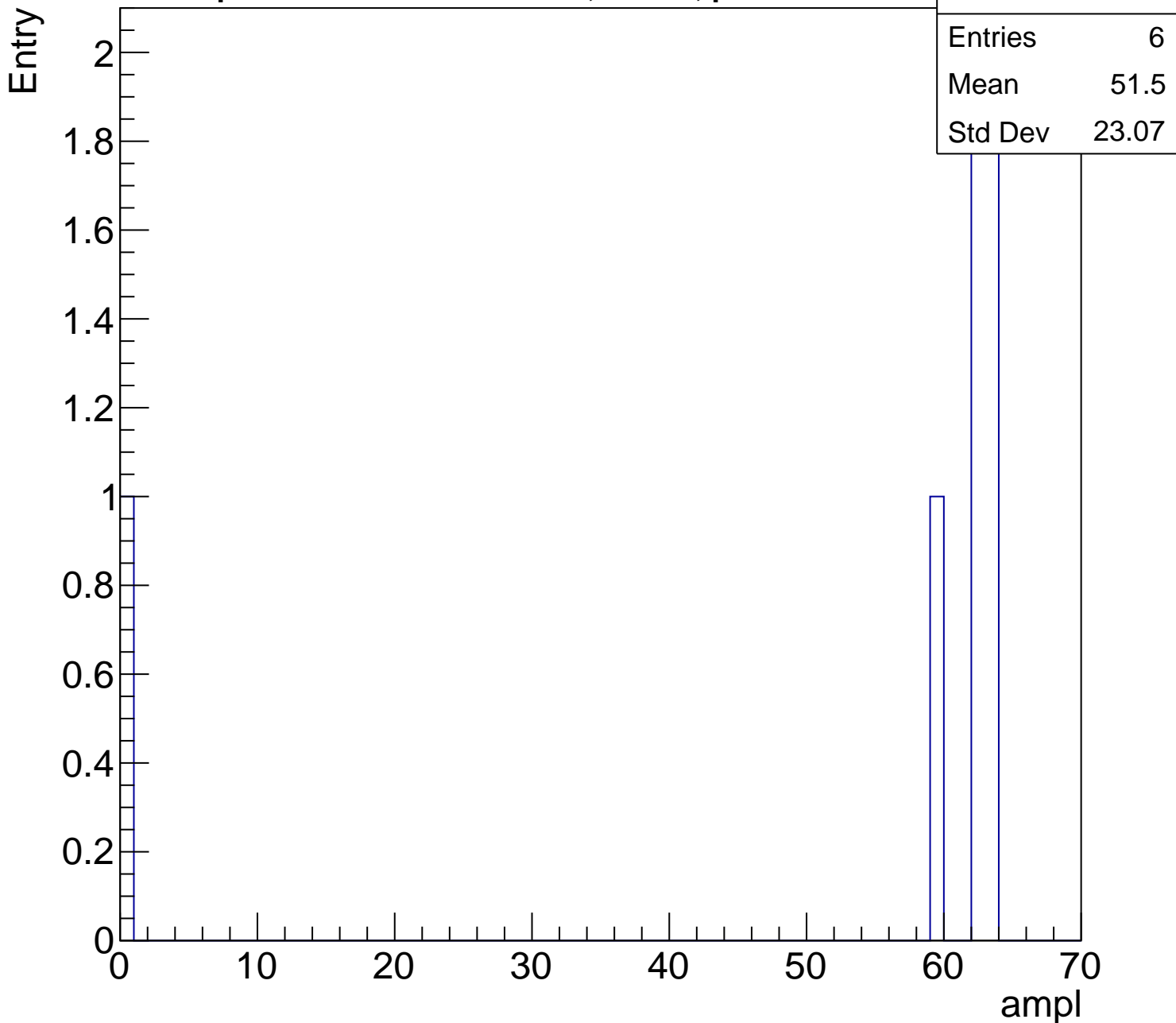
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	51.5
Std Dev	23.07

0 10 20 30 40 50 60 70

ampl





# B1L003S, U26-ch97, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	23
Std Dev	0

ampl

# B1L003S, U26-ch98, adc0

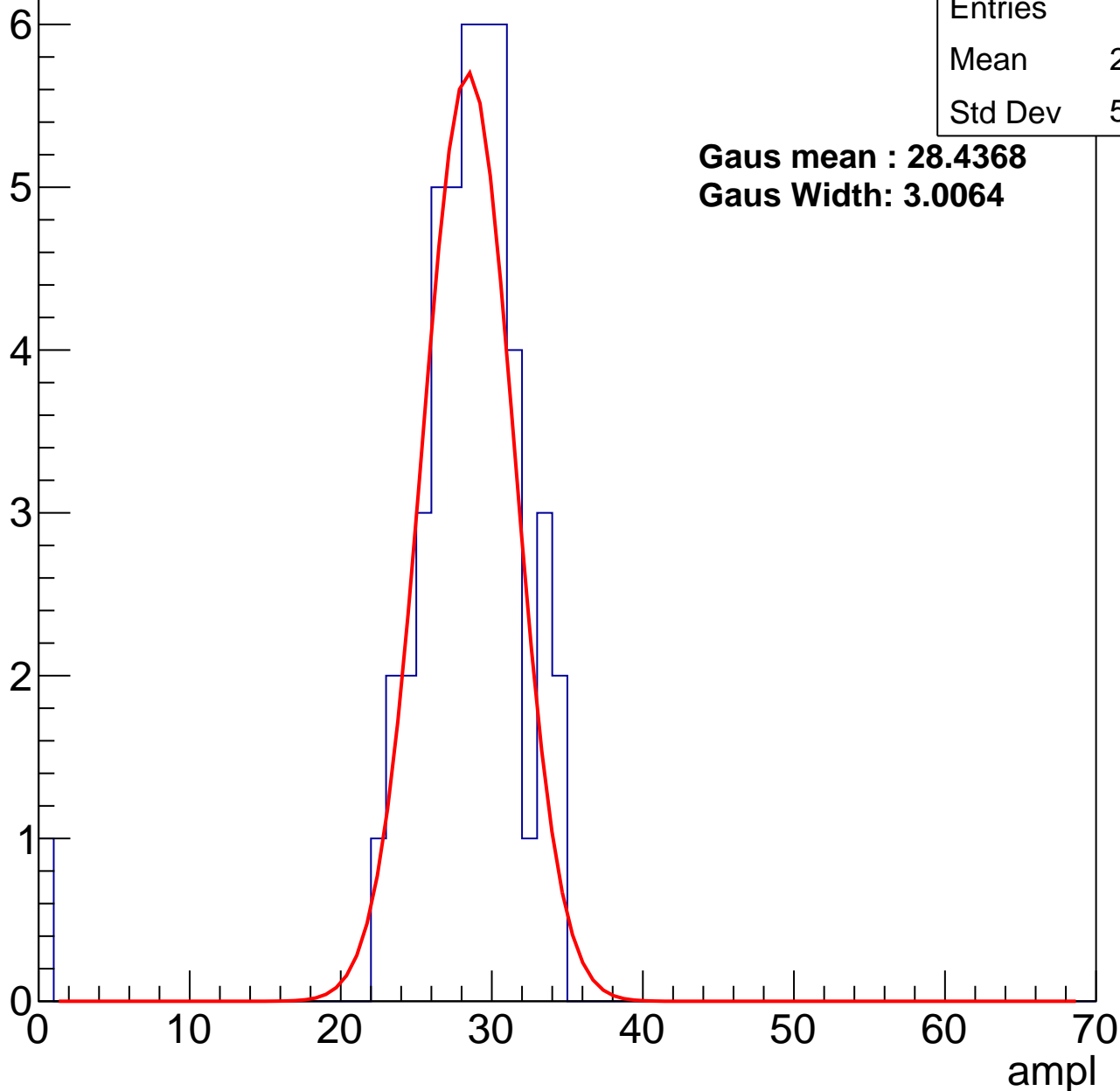
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	47
Mean	27.68
Std Dev	5.007

**Gaus mean : 28.4368**

**Gaus Width: 3.0064**



# B1L003S, U26-ch98, adc1

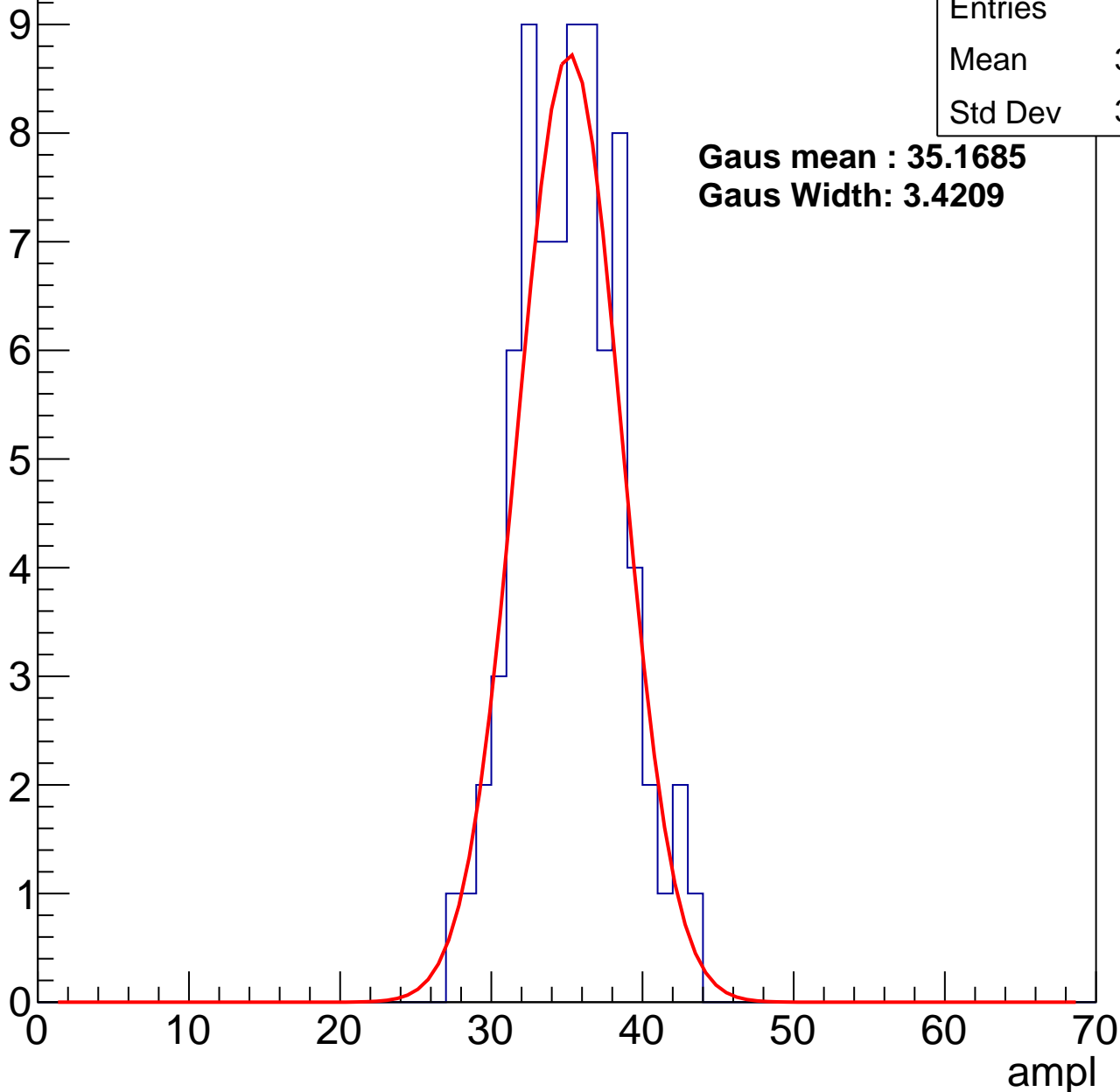
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	78
Mean	34.81
Std Dev	3.371

**Gaus mean : 35.1685**

**Gaus Width: 3.4209**



# B1L003S, U26-ch98, adc2

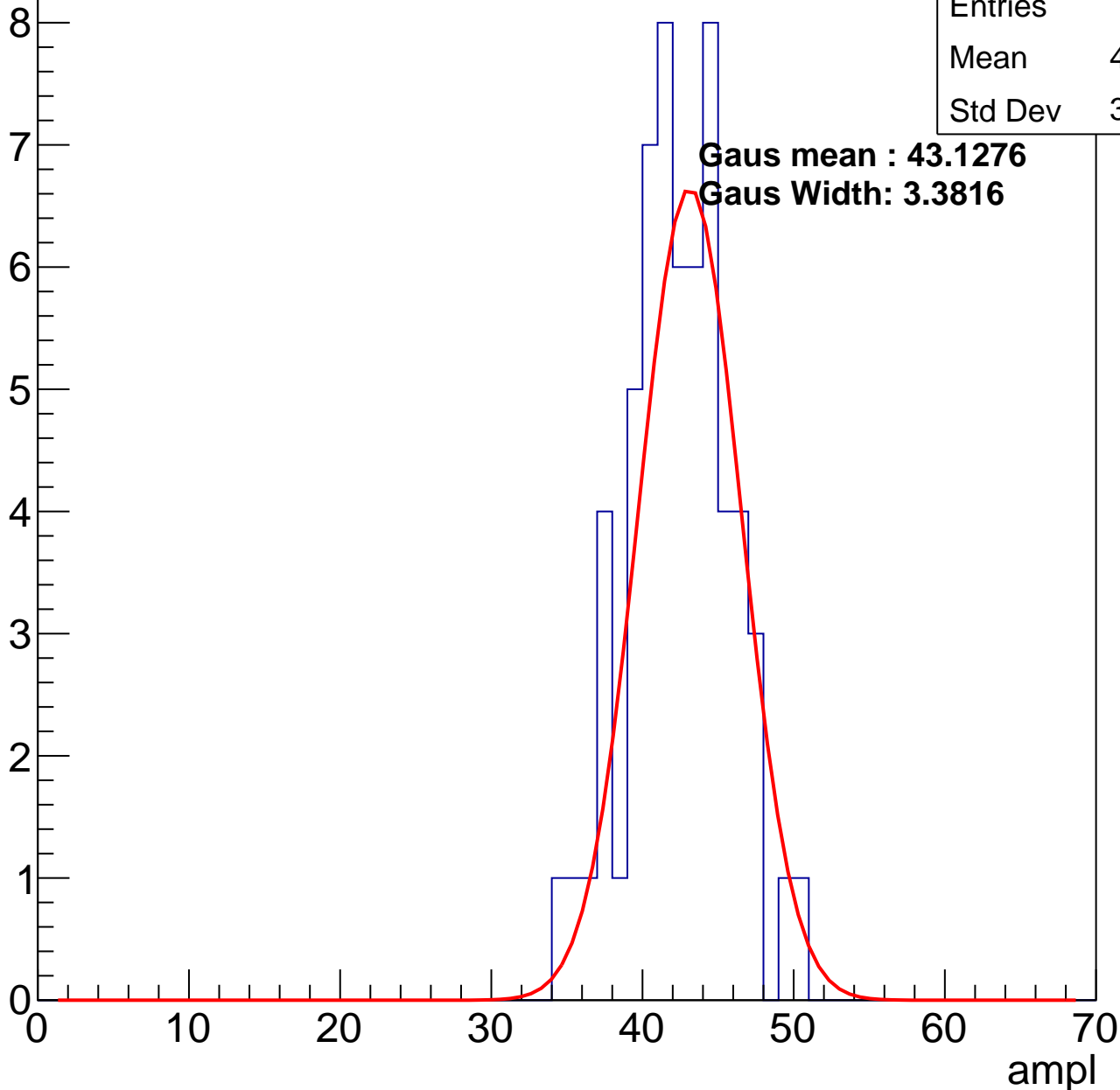
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	41.97
Std Dev	3.319

**Gaus mean : 43.1276**

**Gaus Width: 3.3816**

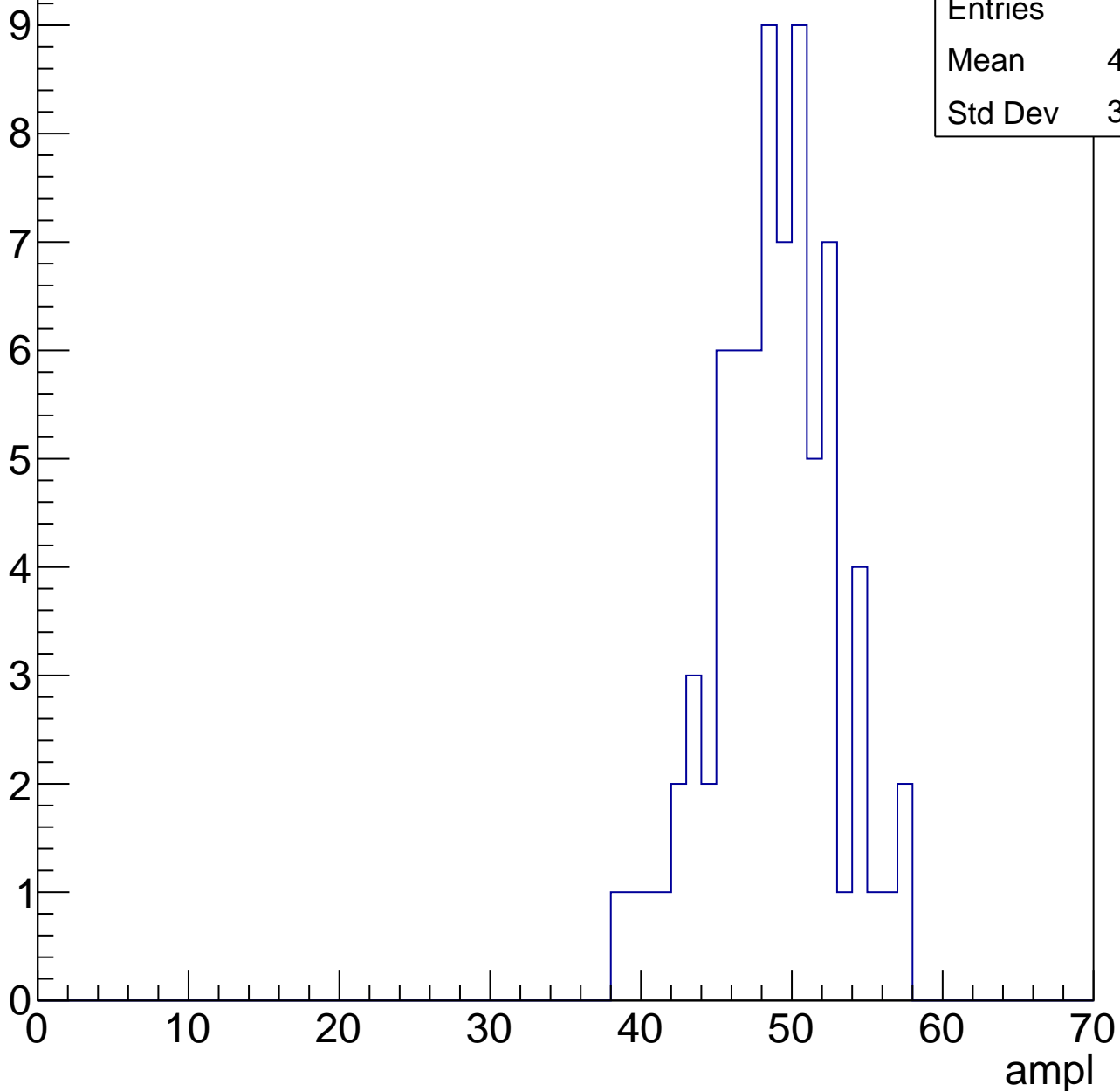


# B1L003S, U26-ch98, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	75
Mean	48.33
Std Dev	3.988

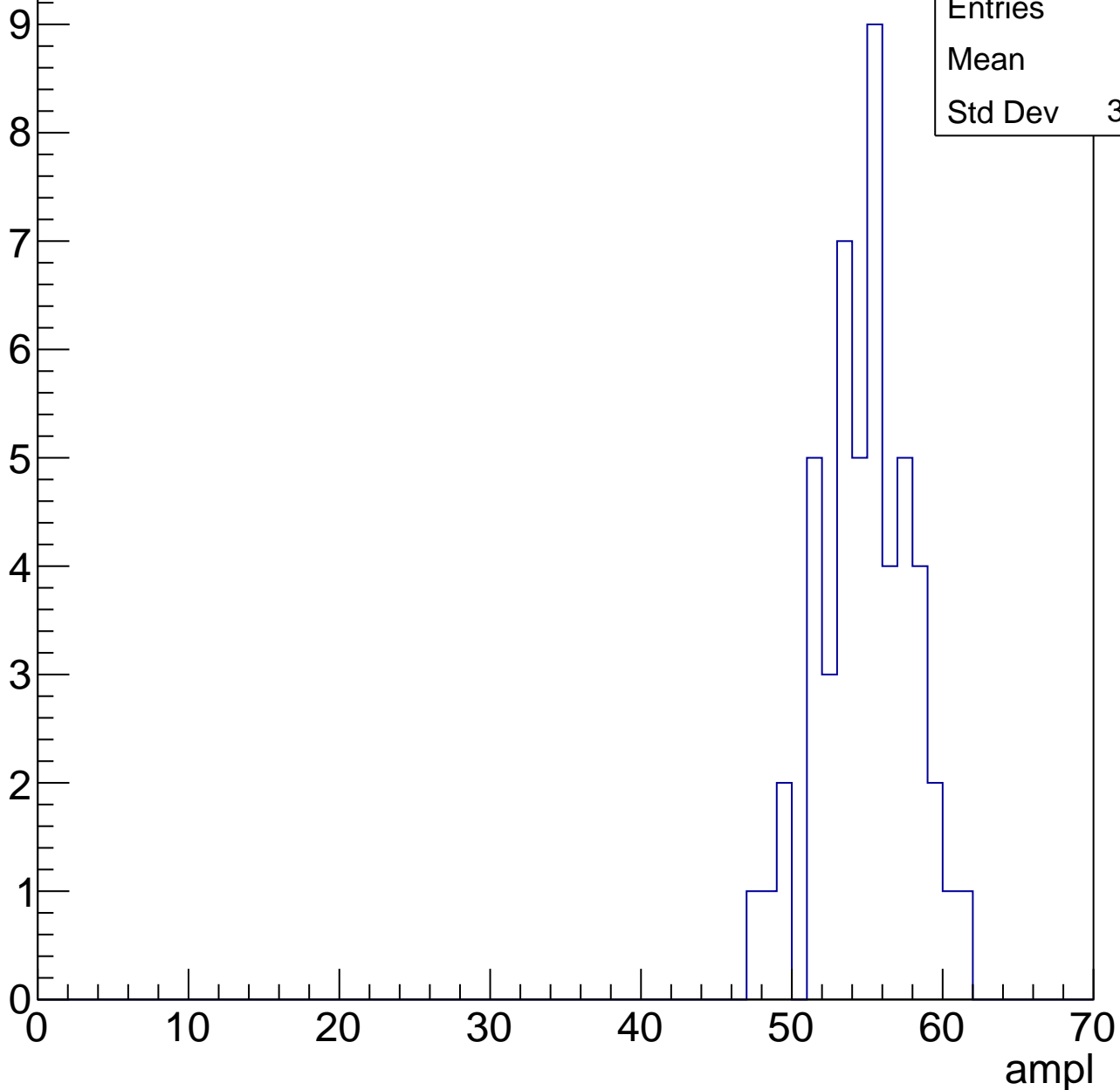


# B1L003S, U26-ch98, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

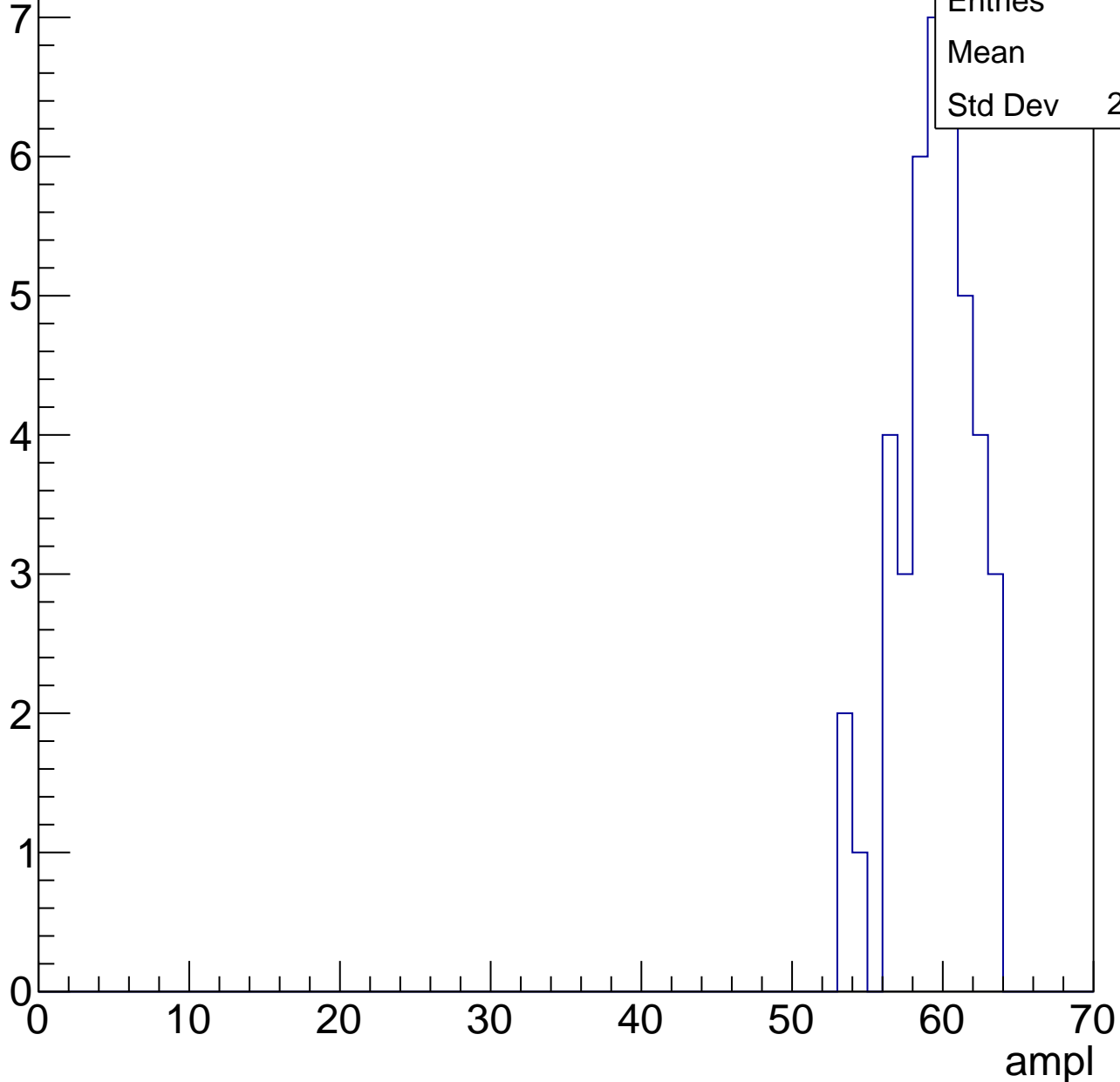
Entries	50
Mean	54.4
Std Dev	3.033



# B1L003S, U26-ch98, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

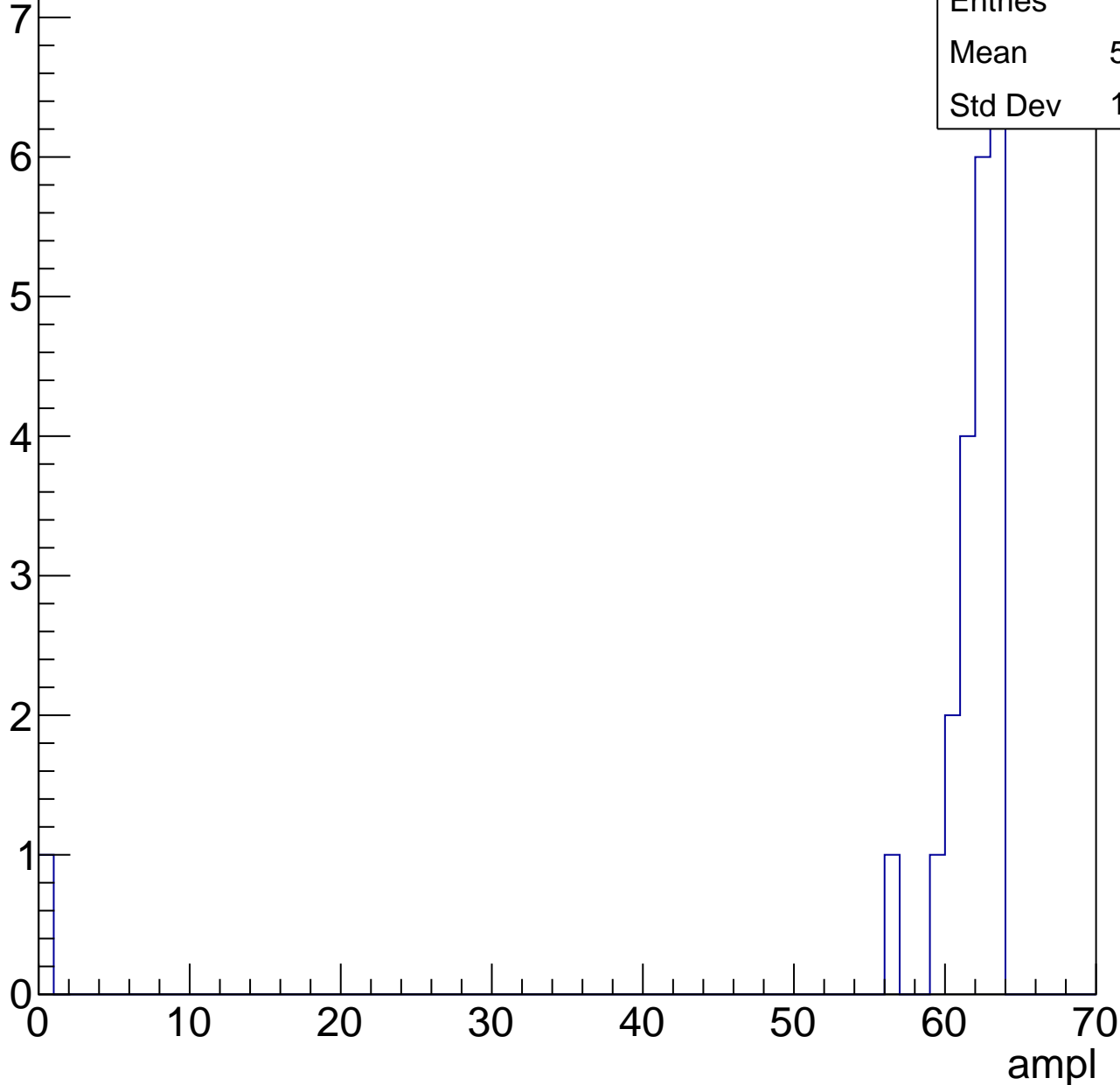


# B1L003S, U26-ch98, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	22
Mean	58.73
Std Dev	12.92





# B1L003S, U26-ch98, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U26-ch99, adc0

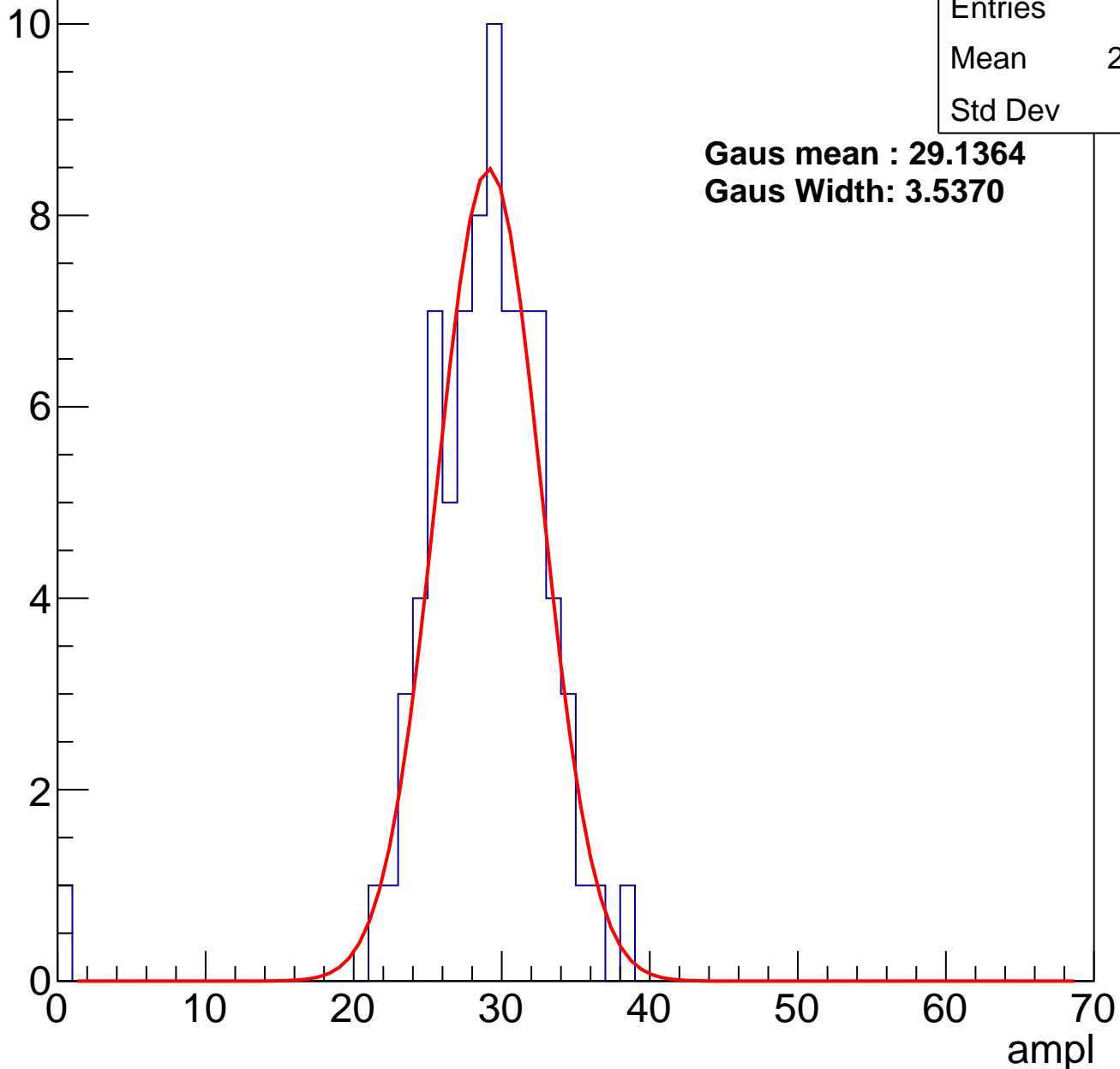
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	78
Mean	28.33
Std Dev	4.7

**Gaus mean : 29.1364**

**Gaus Width: 3.5370**

Entry



# B1L003S, U26-ch99, adc1

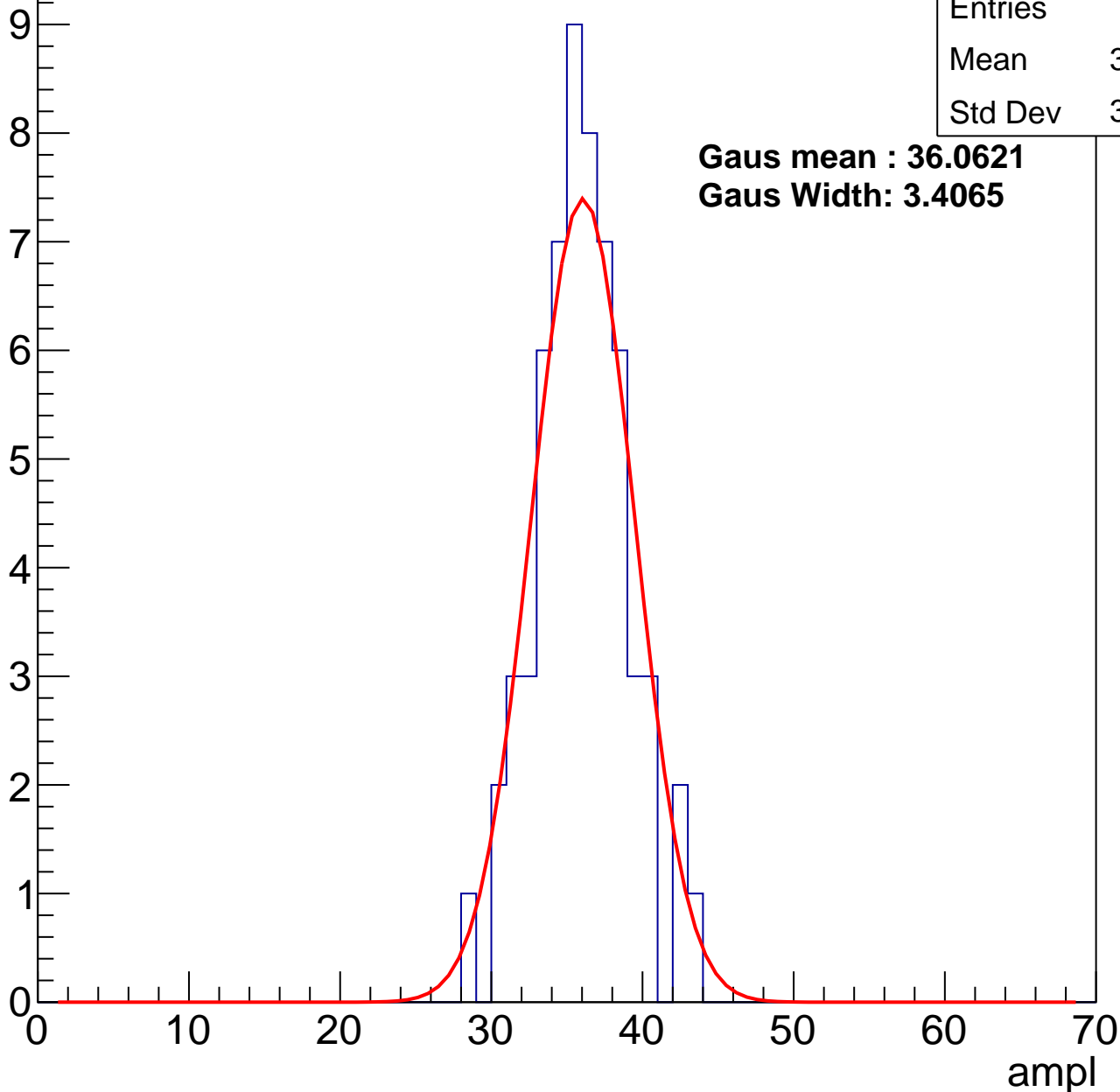
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	35.52
Std Dev	3.039

**Gaus mean : 36.0621**

**Gaus Width: 3.4065**



# B1L003S, U26-ch99, adc2

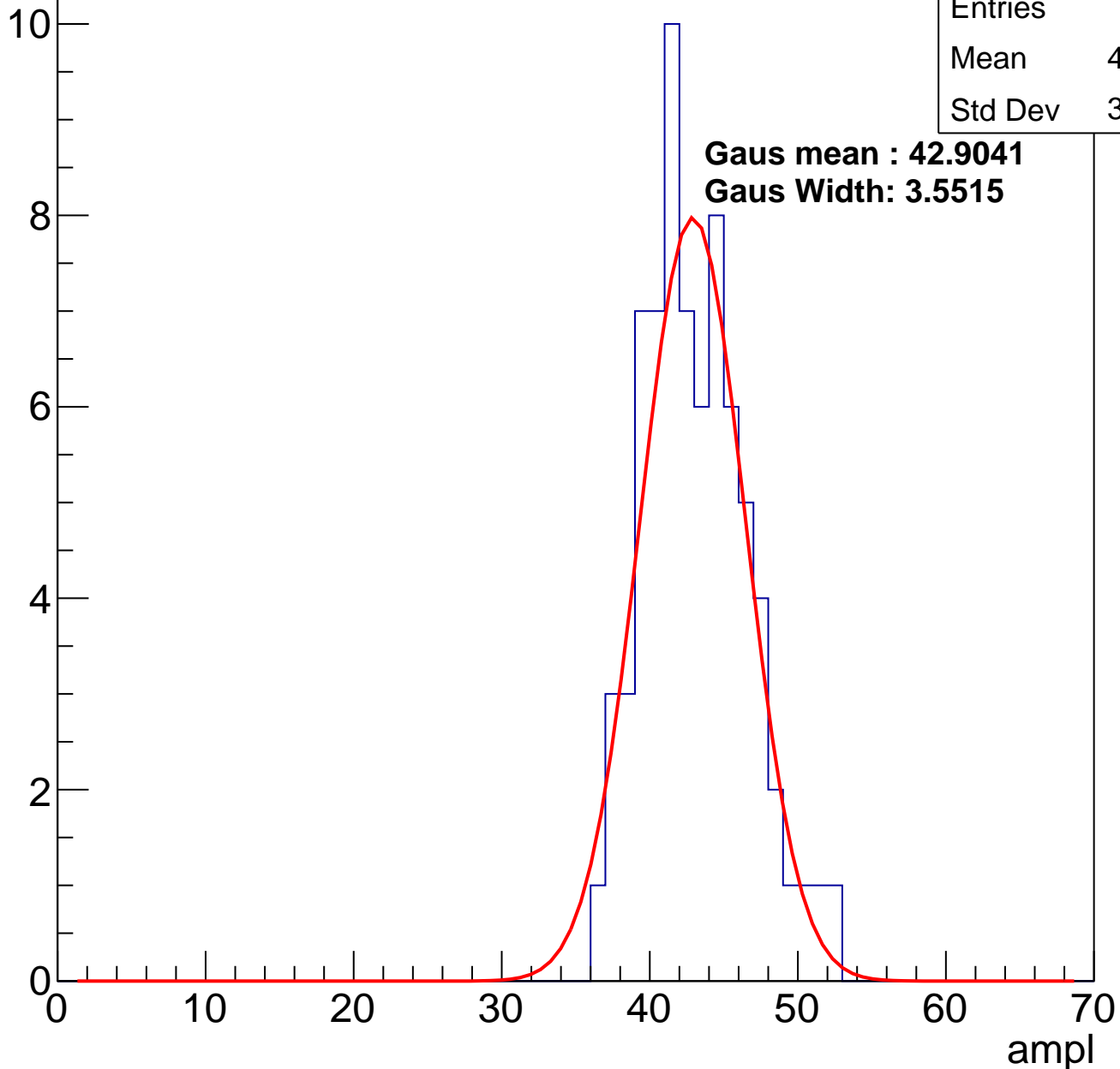
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	73
Mean	42.66
Std Dev	3.445

**Gaus mean : 42.9041**

**Gaus Width: 3.5515**

Entry

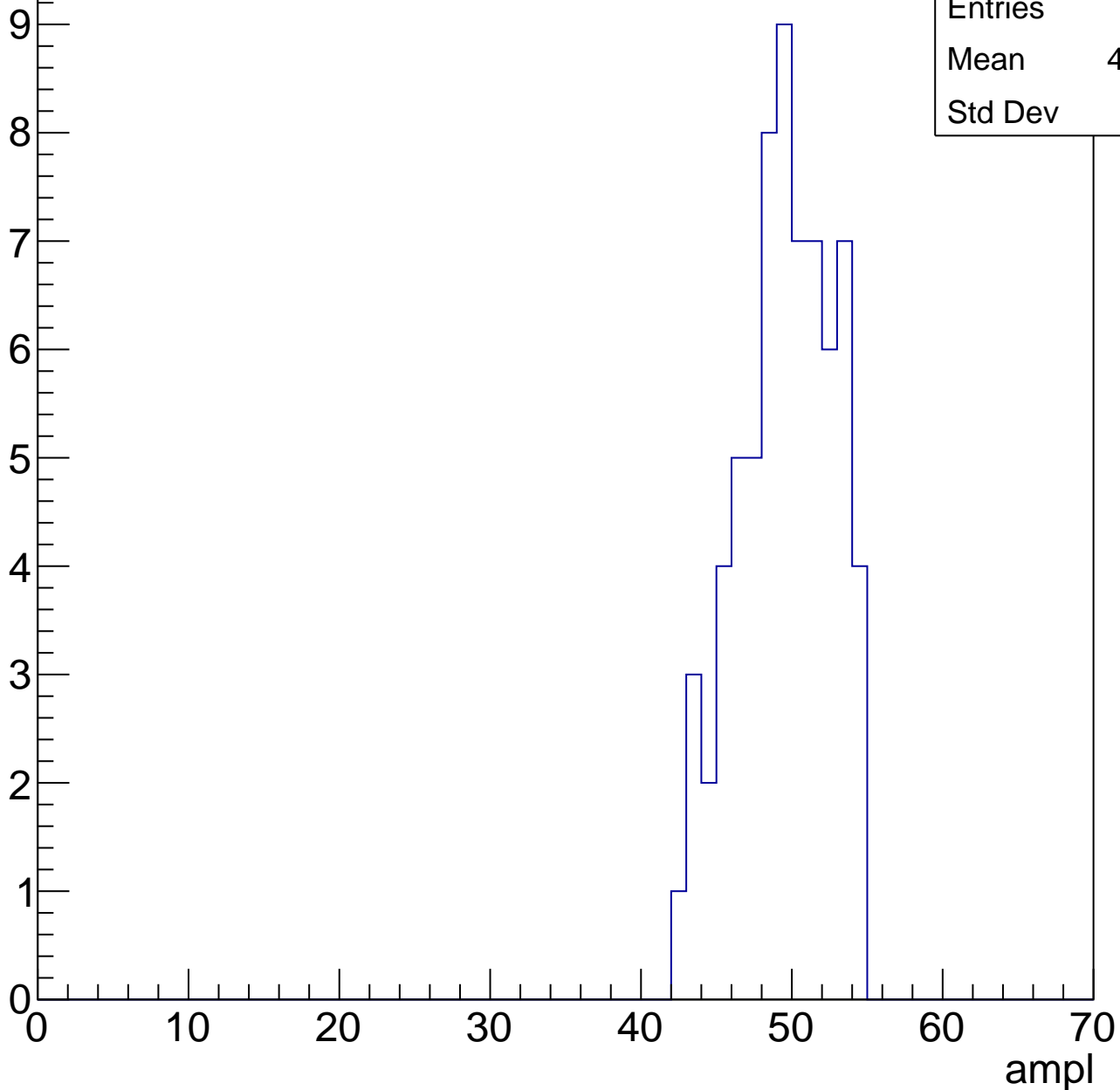


# B1L003S, U26-ch99, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	49.04
Std Dev	3.08

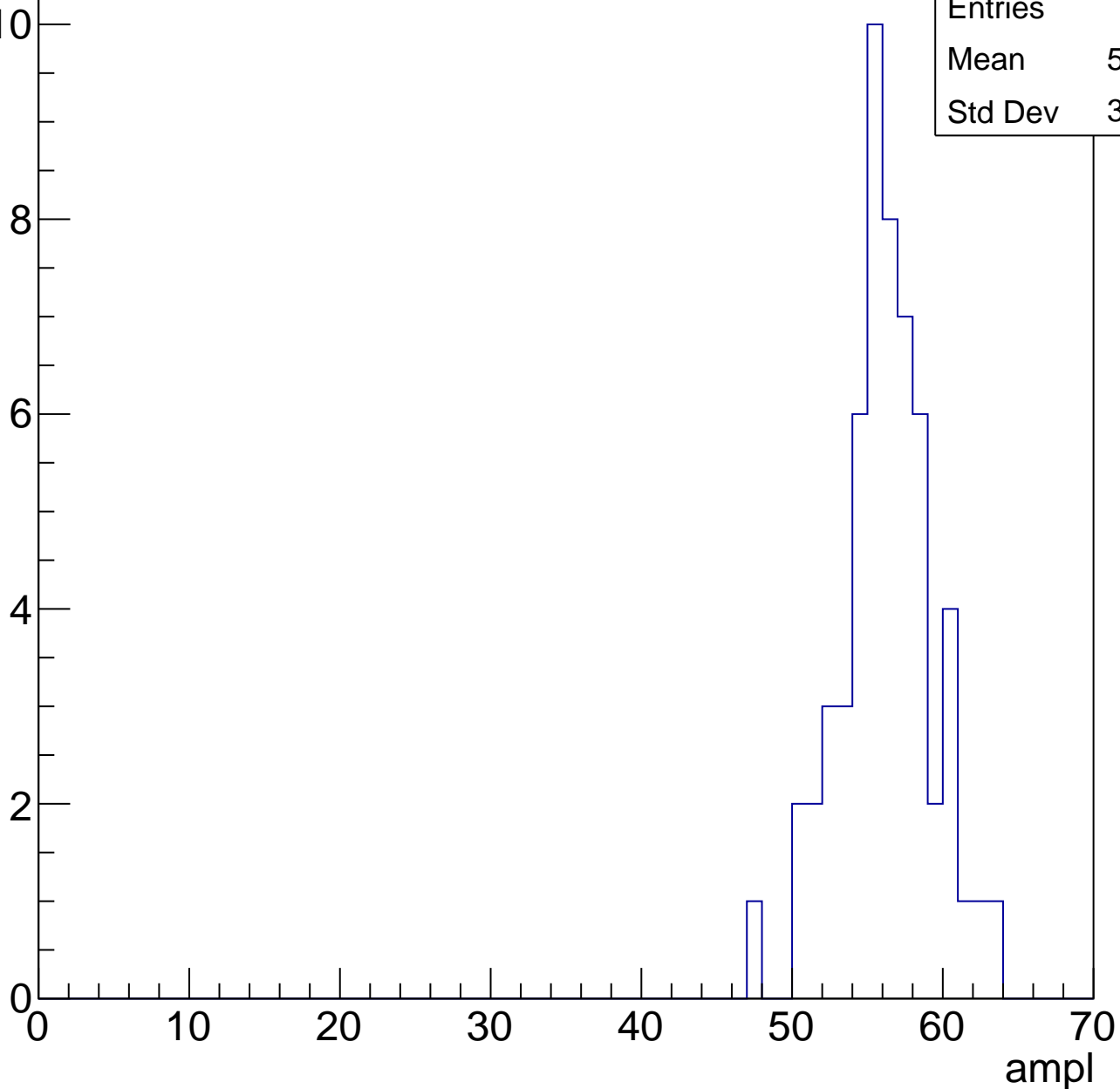


# B1L003S, U26-ch99, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

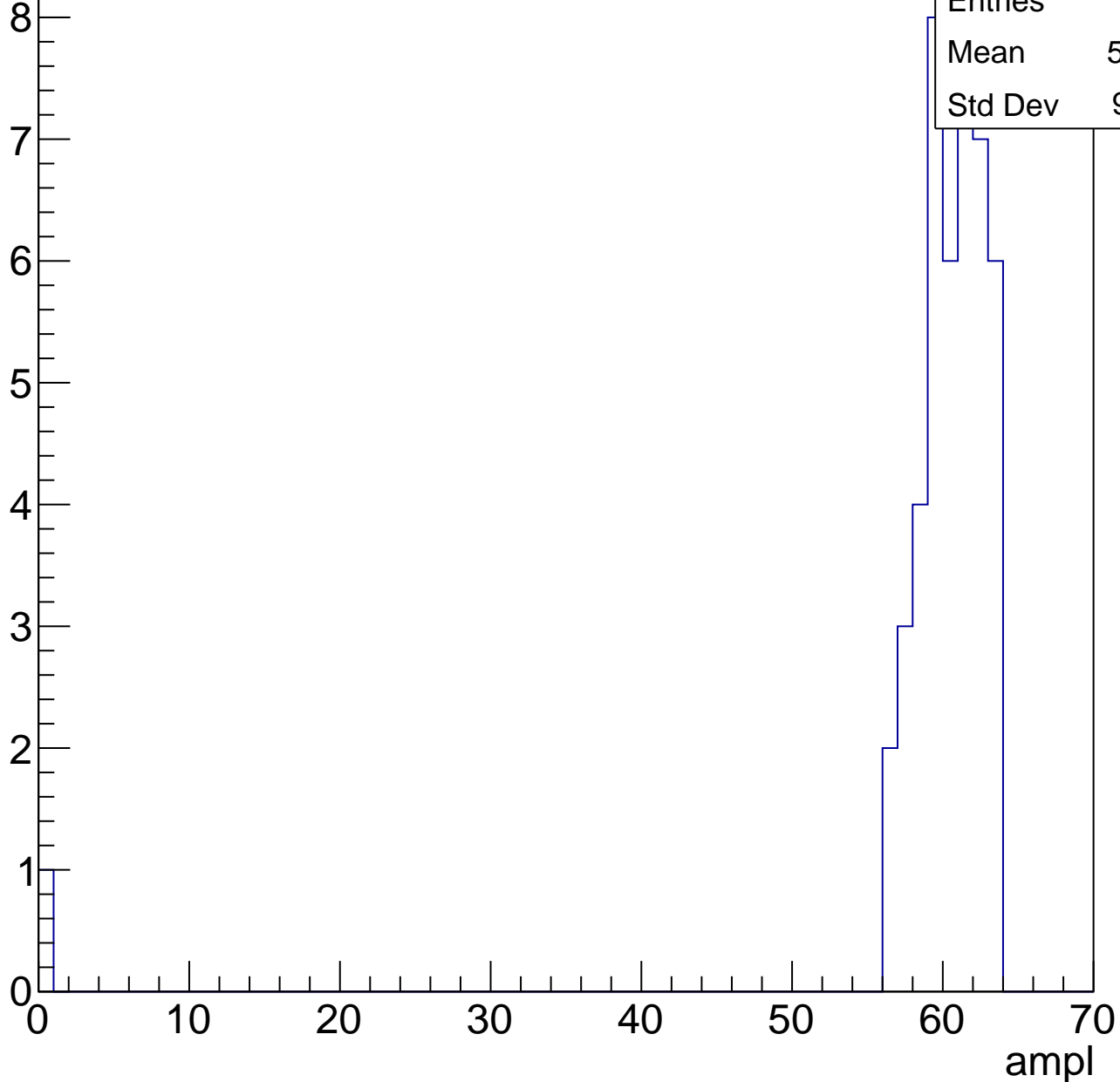
Entries	57
Mean	55.74
Std Dev	3.052



# B1L003S, U26-ch99, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

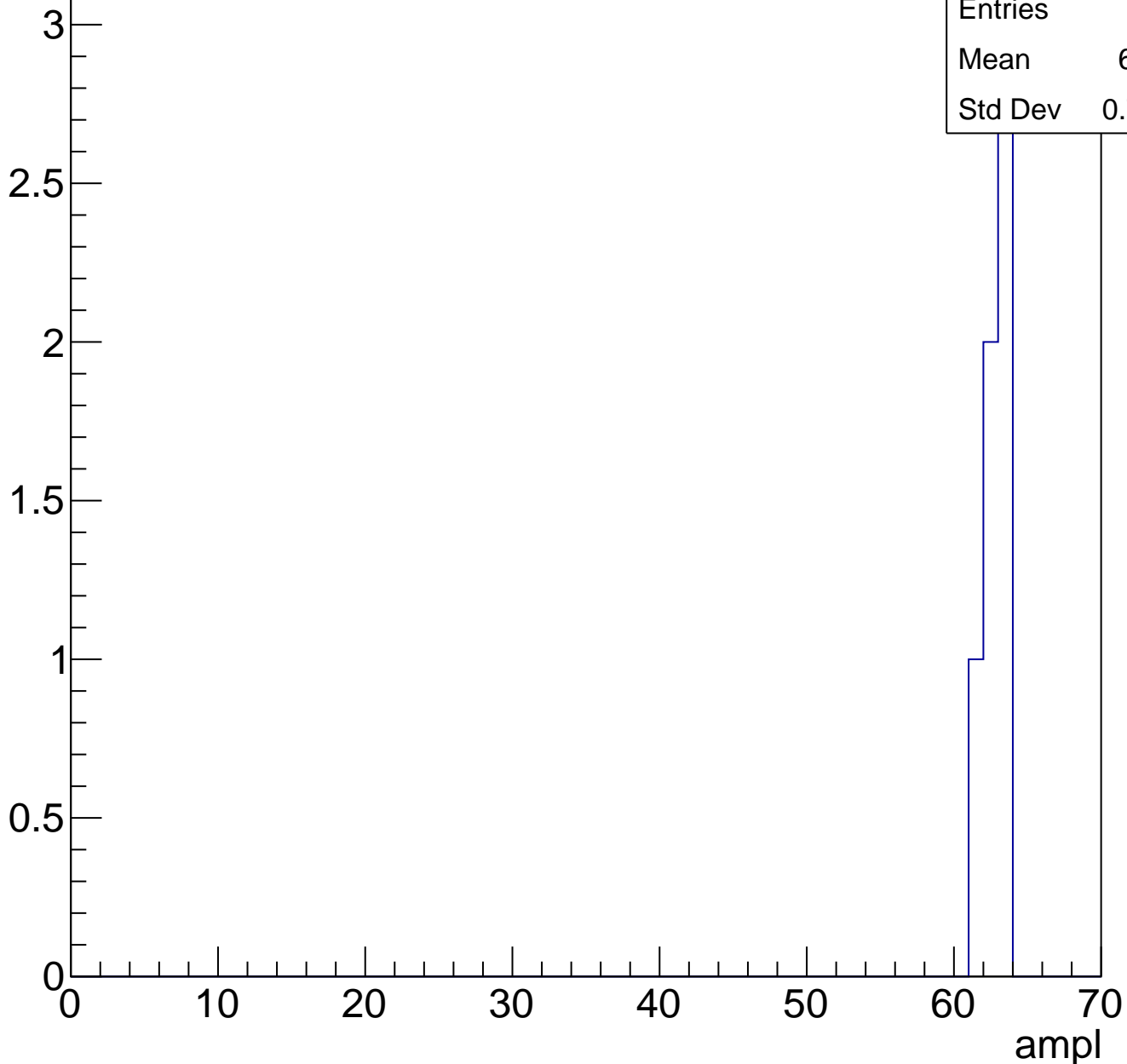
Entry



# B1L003S, U26-ch99, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch99, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U26-ch100, adc0

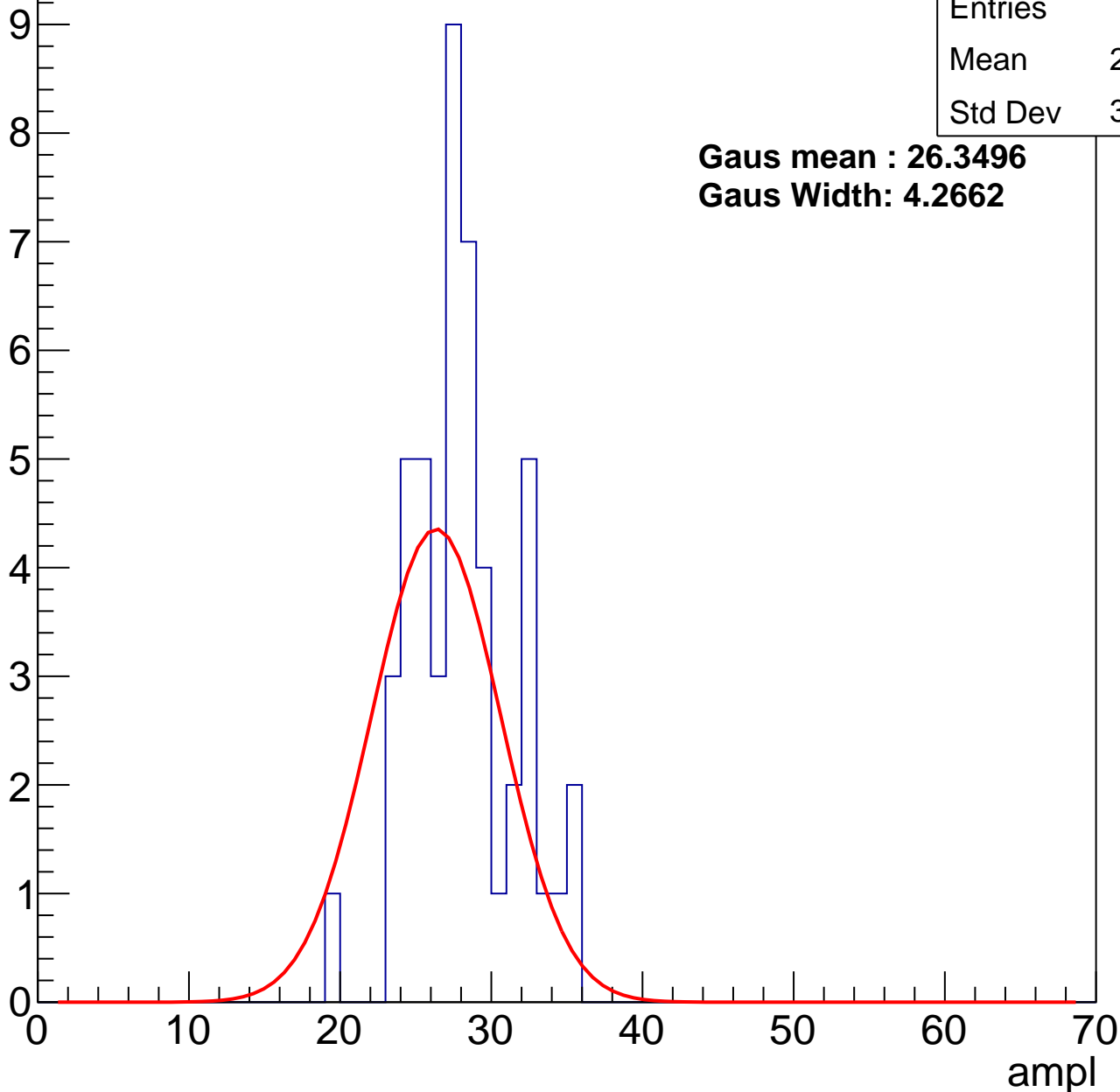
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	49
Mean	27.65
Std Dev	3.384

**Gaus mean : 26.3496**

**Gaus Width: 4.2662**



# B1L003S, U26-ch100, adc1

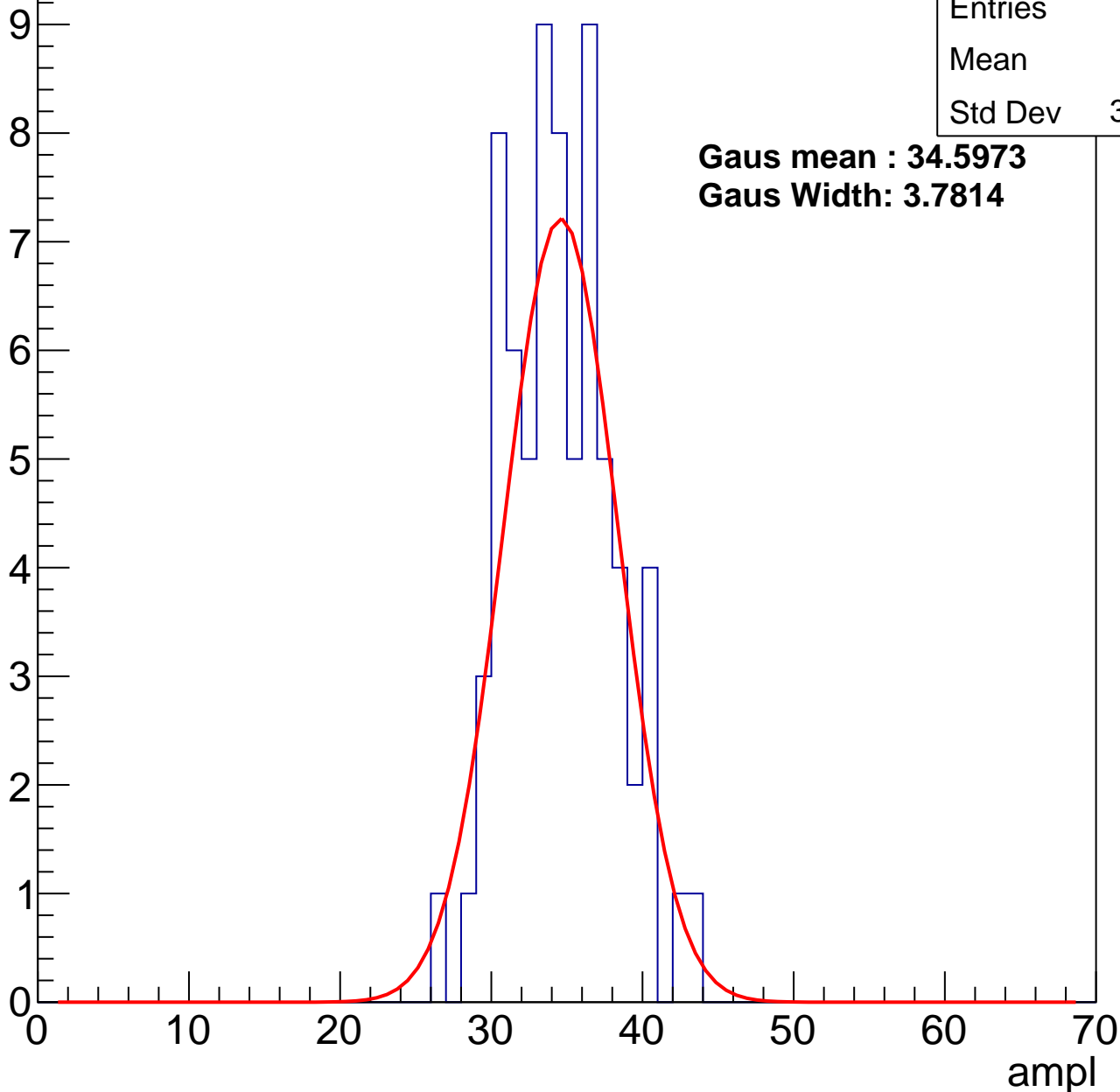
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	72
Mean	34.1
Std Dev	3.485

**Gaus mean : 34.5973**

**Gaus Width: 3.7814**



# B1L003S, U26-ch100, adc2

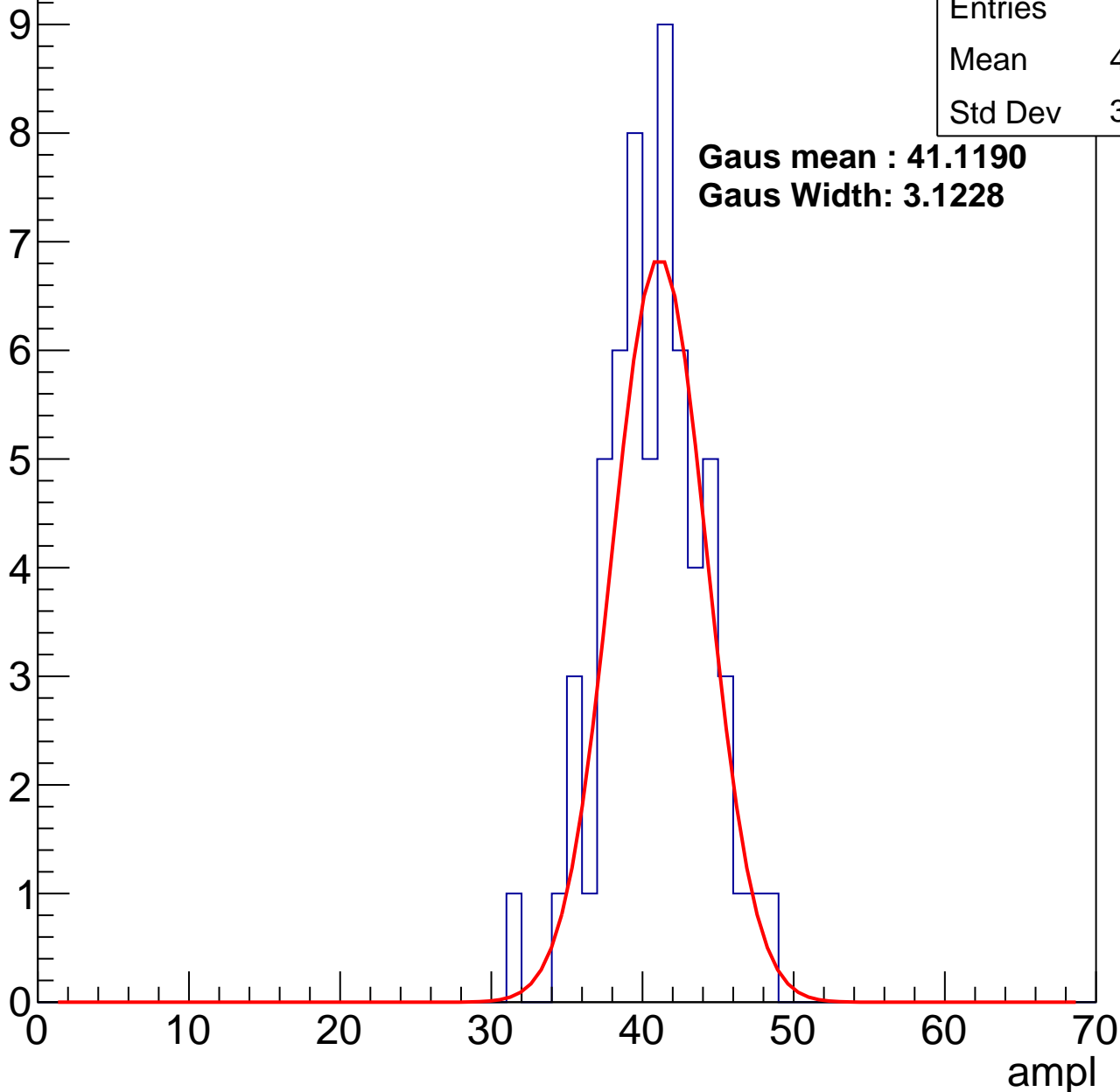
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	40.33
Std Dev	3.295

**Gaus mean : 41.1190**

**Gaus Width: 3.1228**

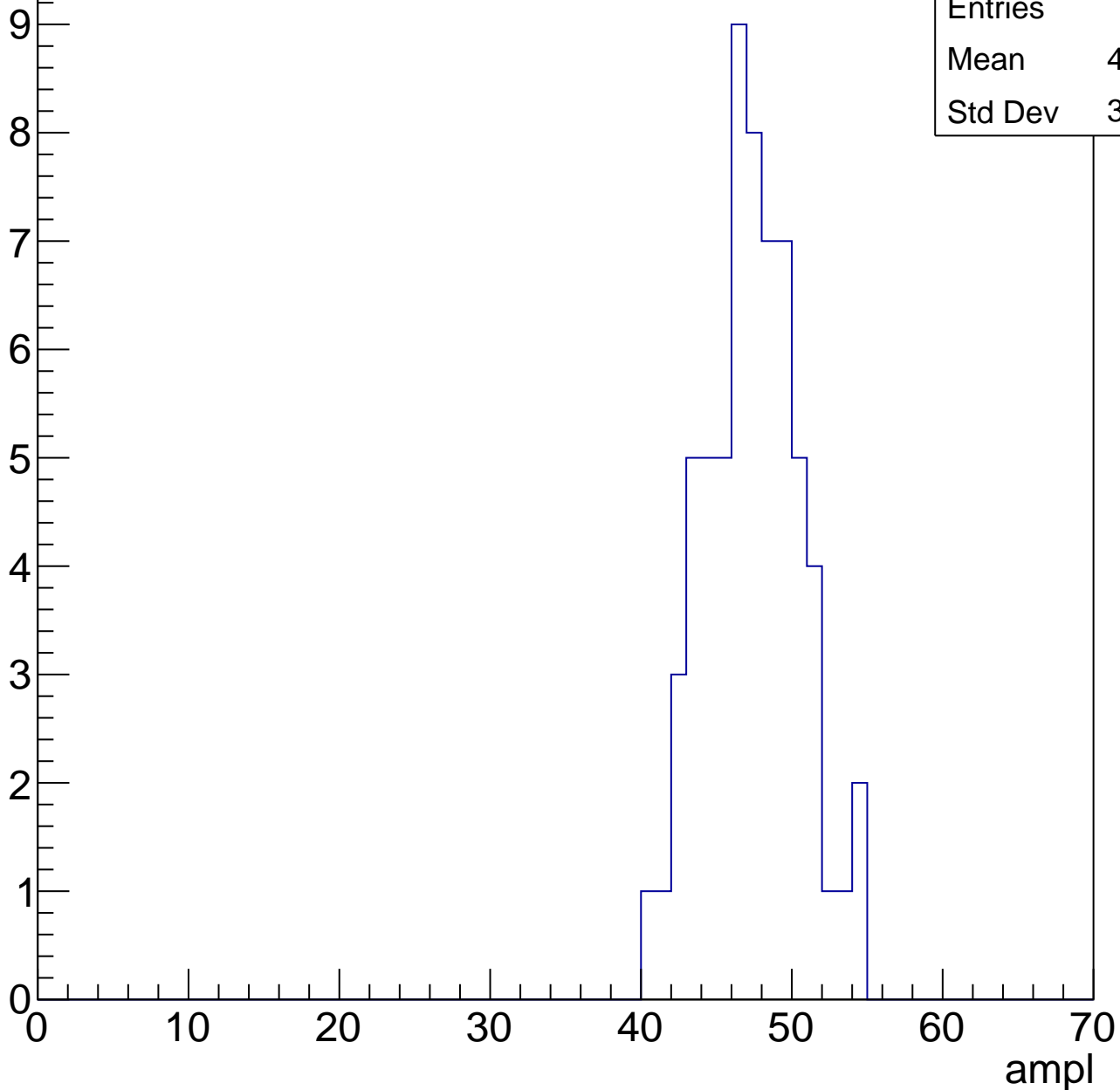


# B1L003S, U26-ch100, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	46.92
Std Dev	3.104

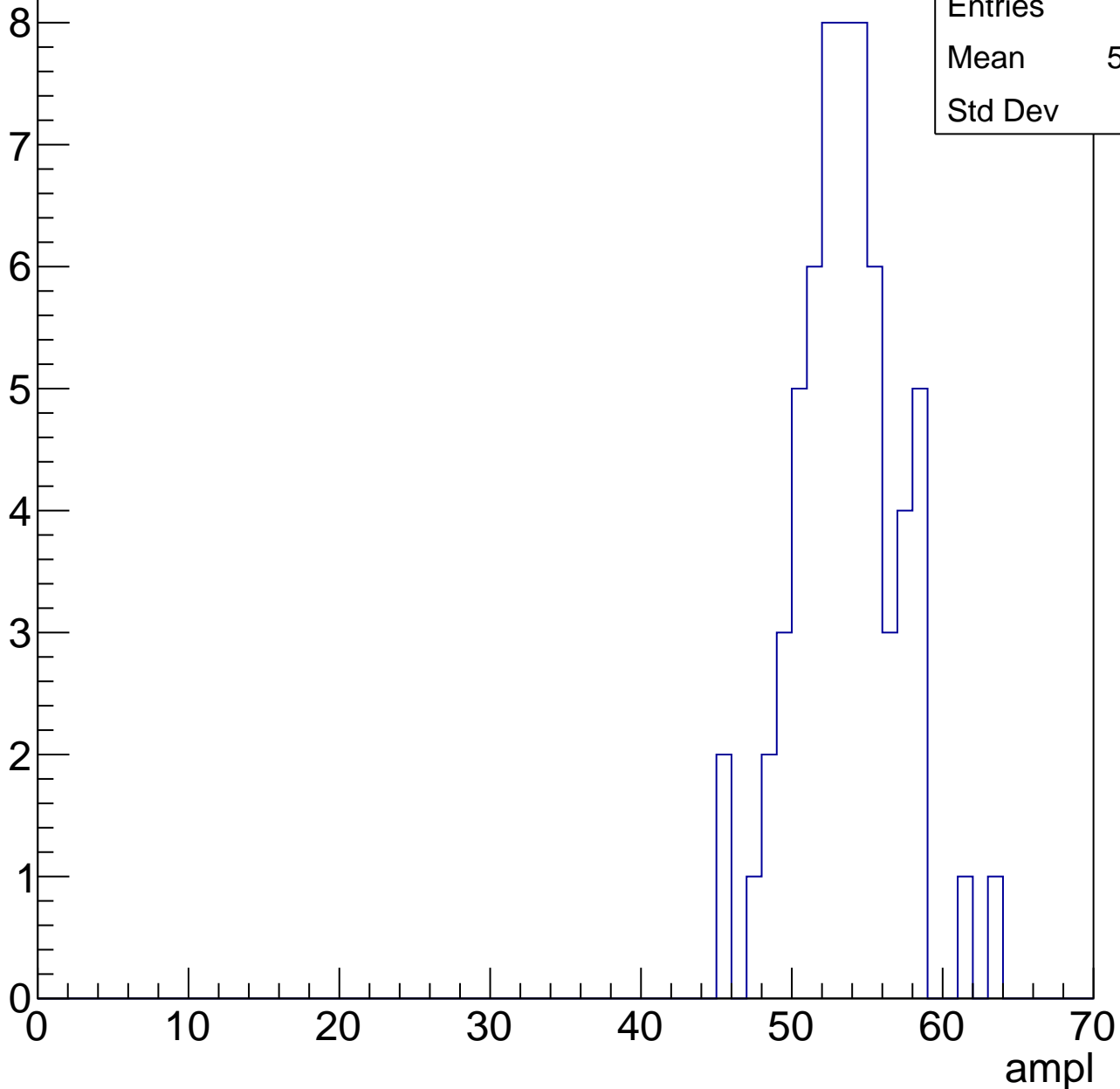


# B1L003S, U26-ch100, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	53.14
Std Dev	3.45

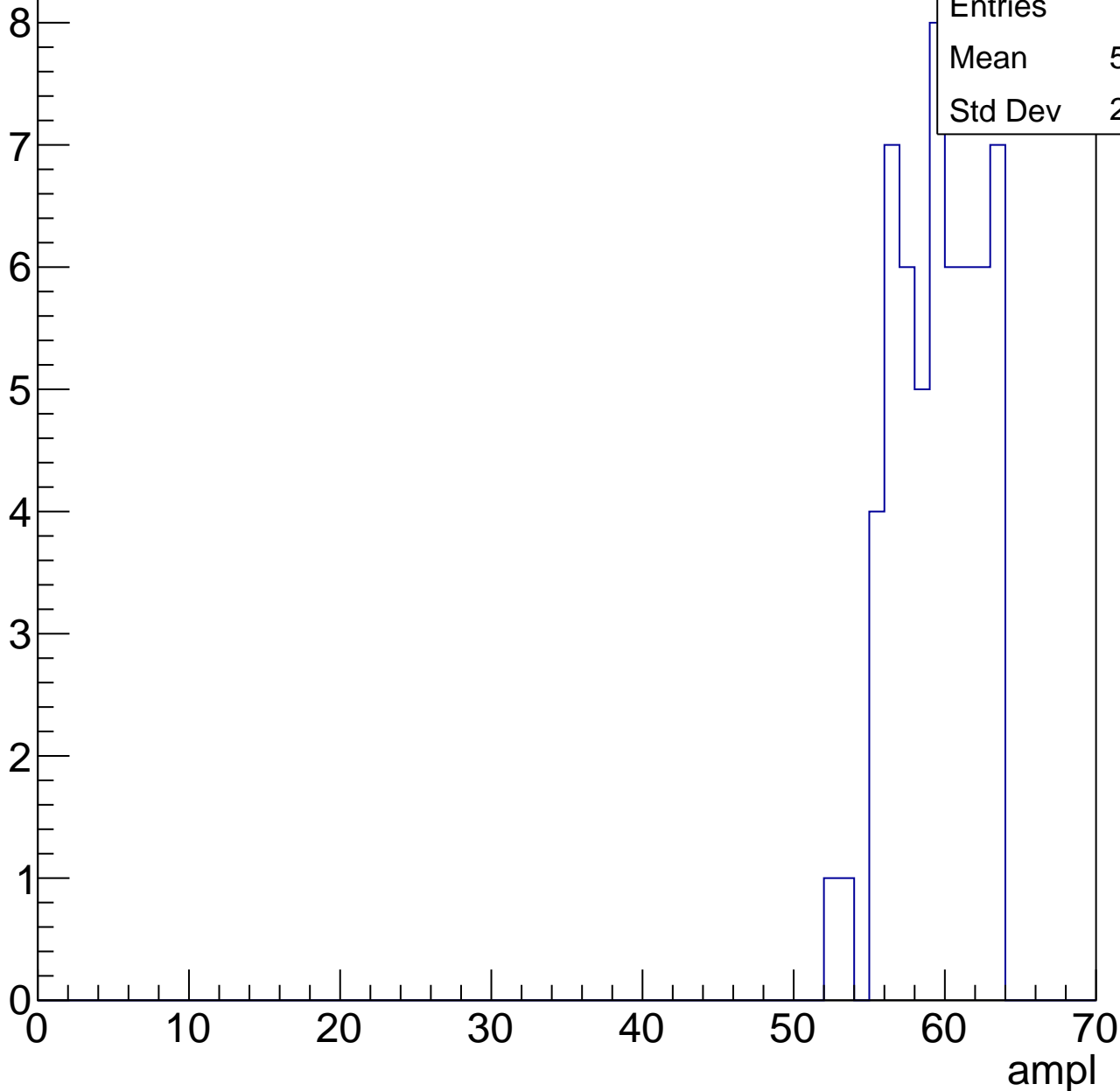


# B1L003S, U26-ch100, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

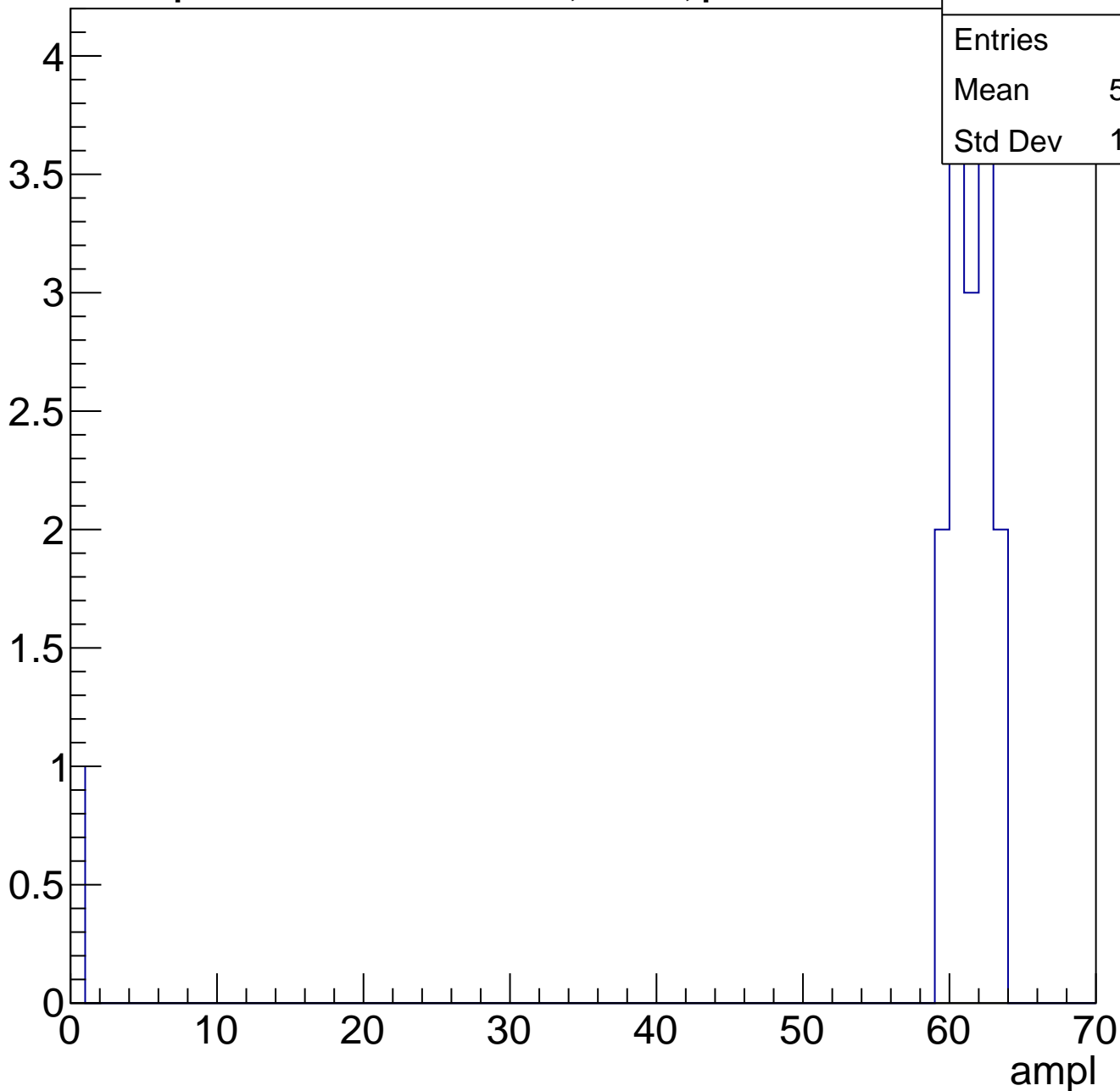
Entries	57
Mean	58.95
Std Dev	2.768



# B1L003S, U26-ch100, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch100, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U26-ch101, adc0

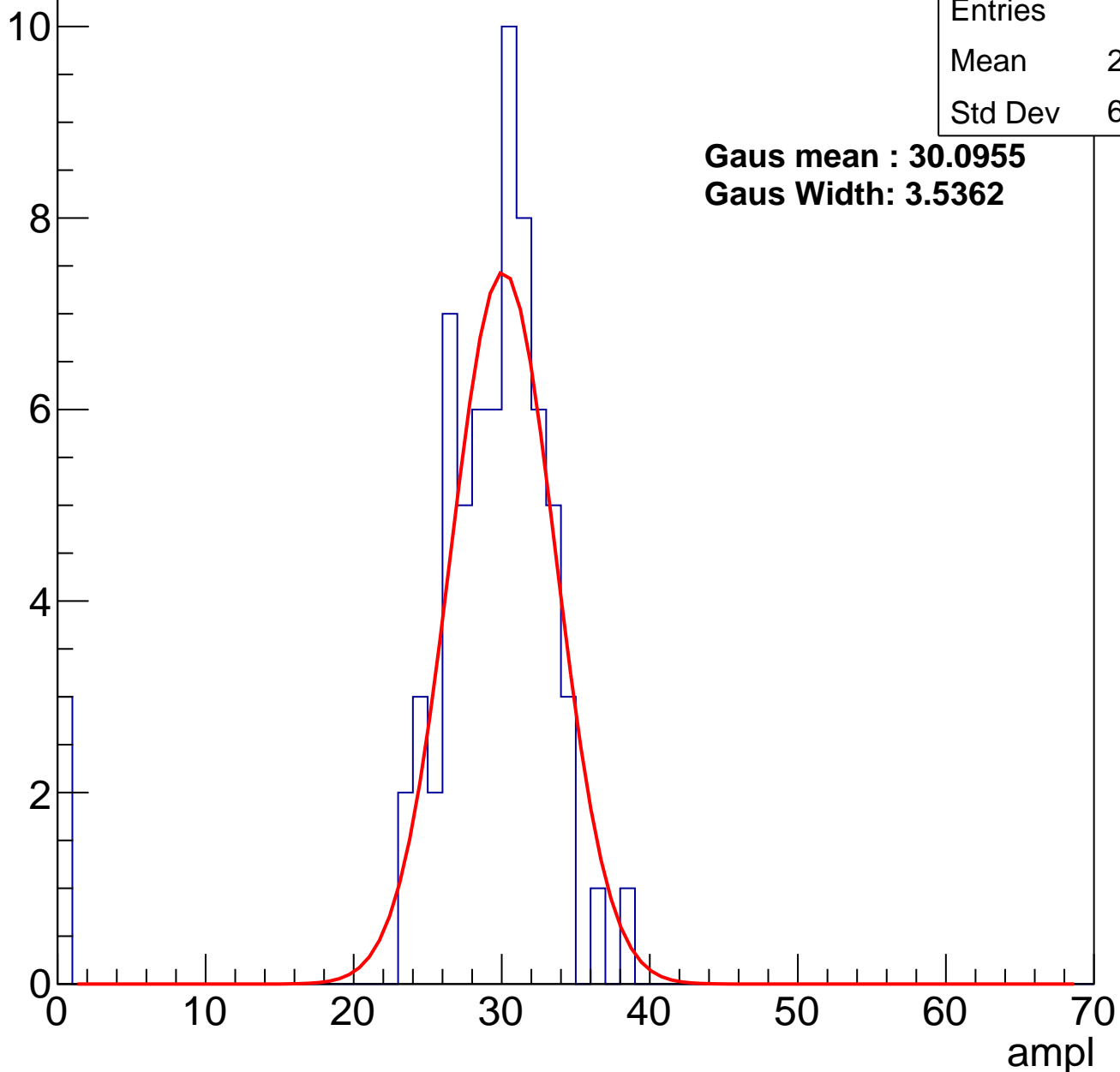
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	68
Mean	28.06
Std Dev	6.765

**Gaus mean : 30.0955**

**Gaus Width: 3.5362**

Entry



# B1L003S, U26-ch101, adc1

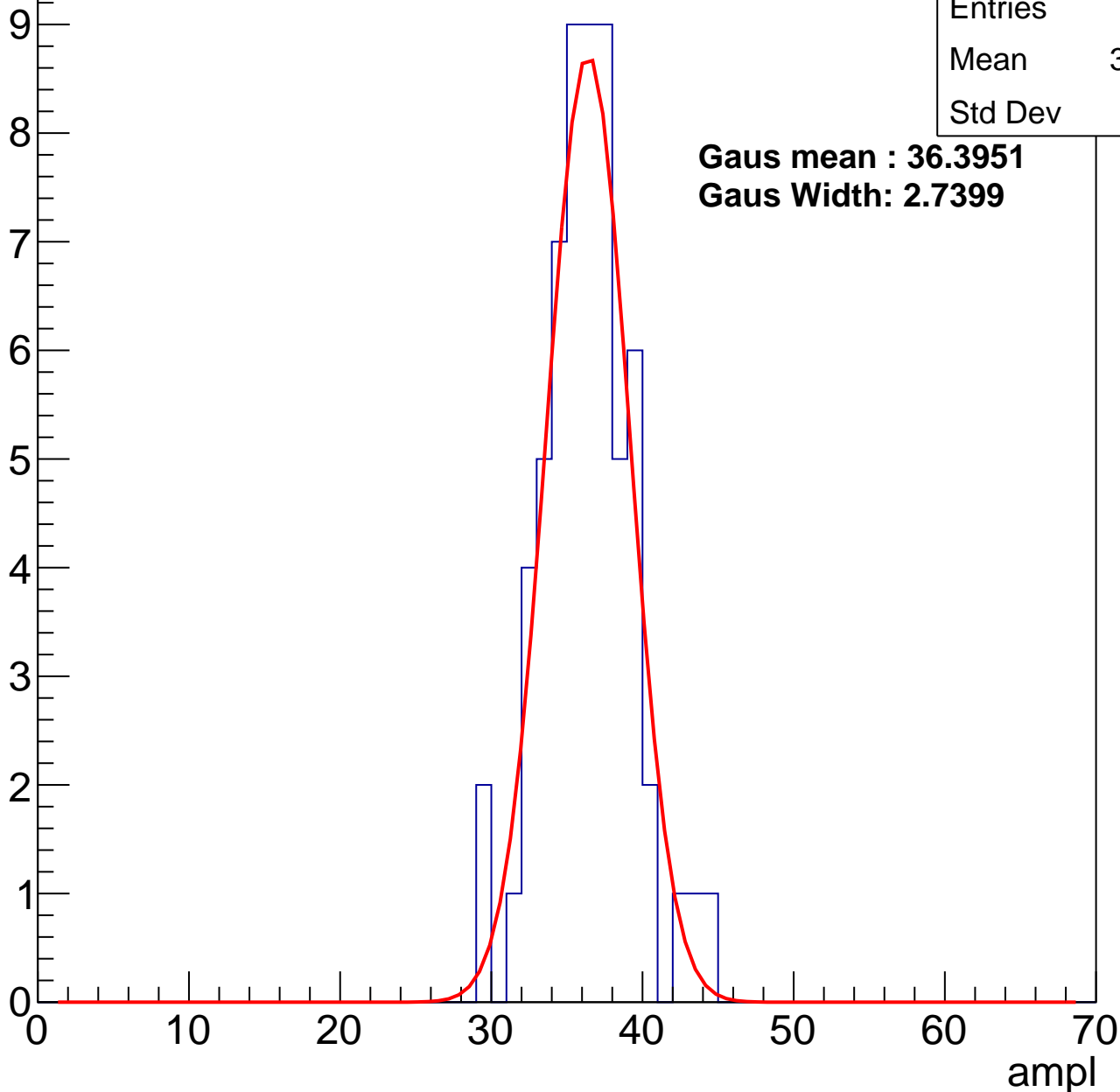
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	35.89
Std Dev	2.93

**Gaus mean : 36.3951**

**Gaus Width: 2.7399**



# B1L003S, U26-ch101, adc2

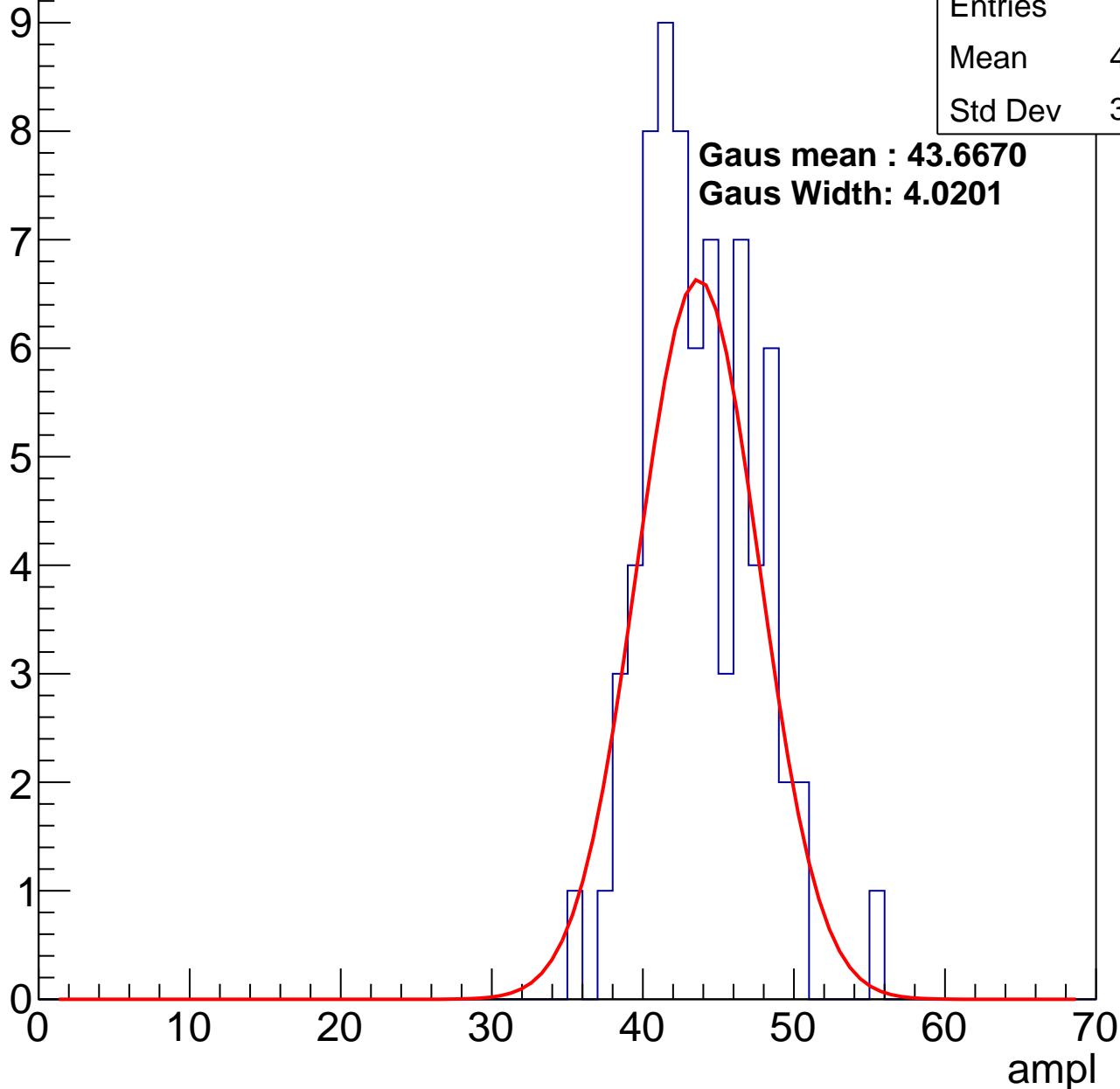
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	72
Mean	43.32
Std Dev	3.647

**Gaus mean : 43.6670**

**Gaus Width: 4.0201**

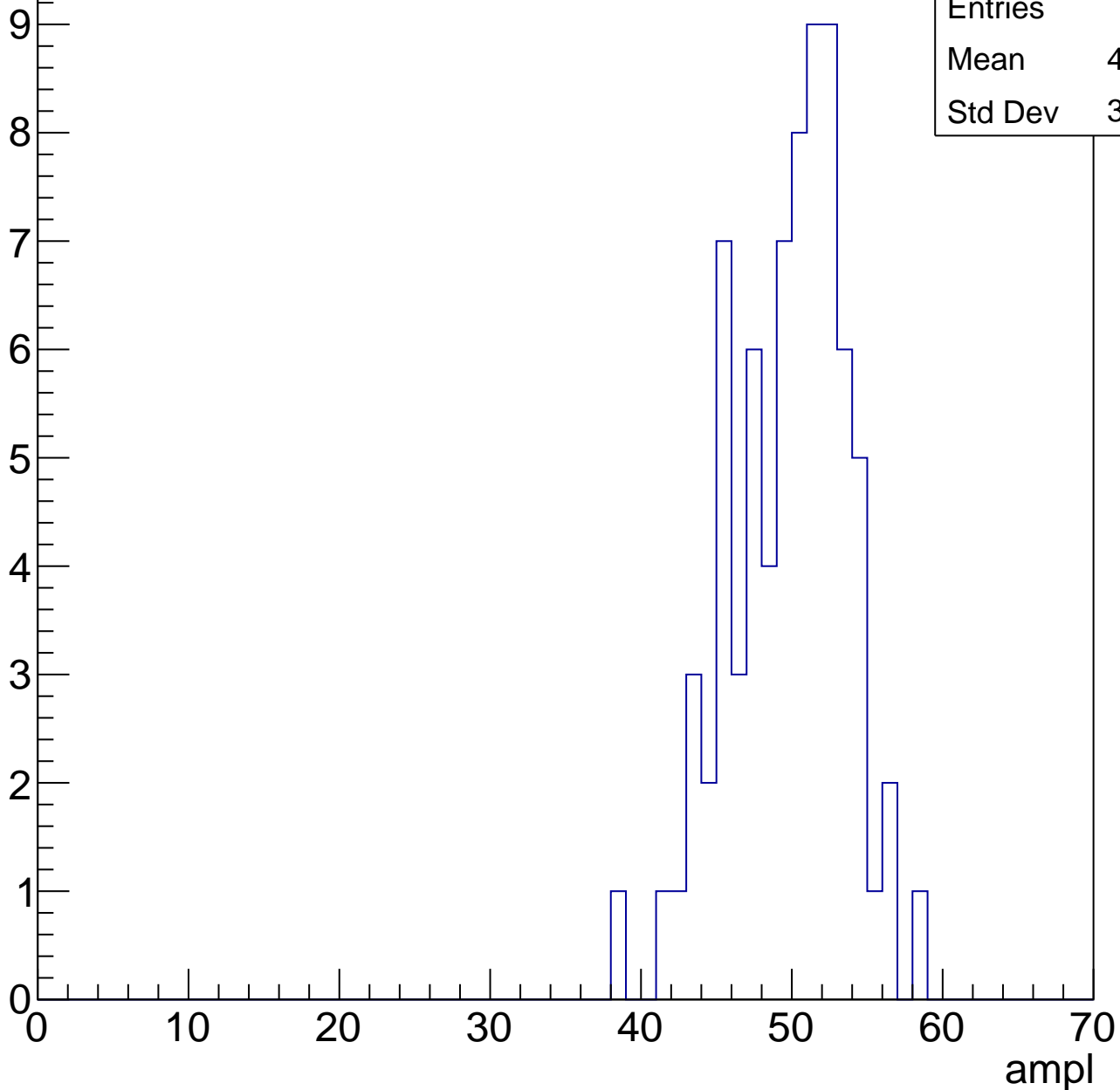


# B1L003S, U26-ch101, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	76
Mean	49.32
Std Dev	3.826

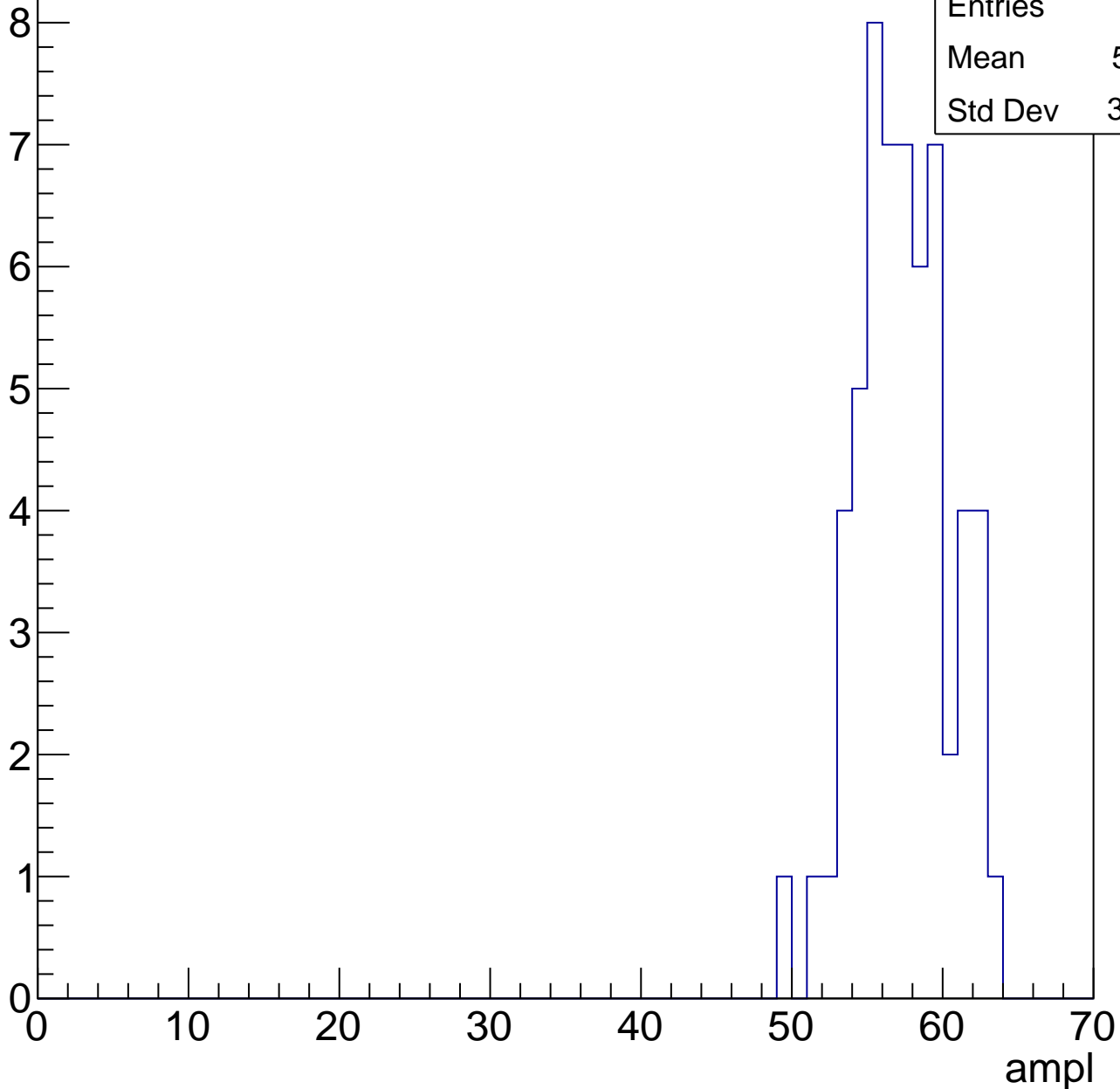


# B1L003S, U26-ch101, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	56.91
Std Dev	3.007



# B1L003S, U26-ch101, adc5

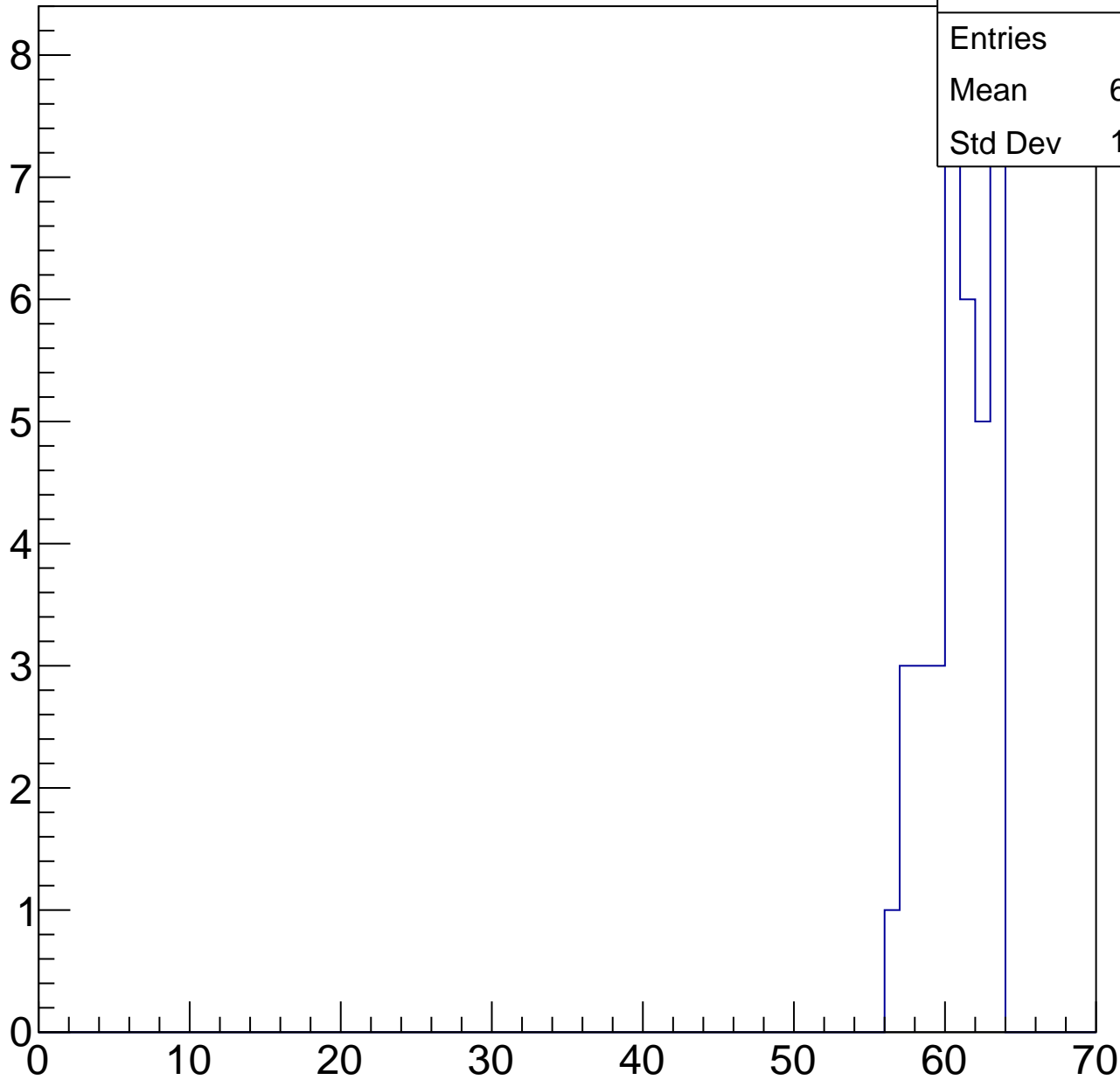
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	37
Mean	60.49
Std Dev	1.995

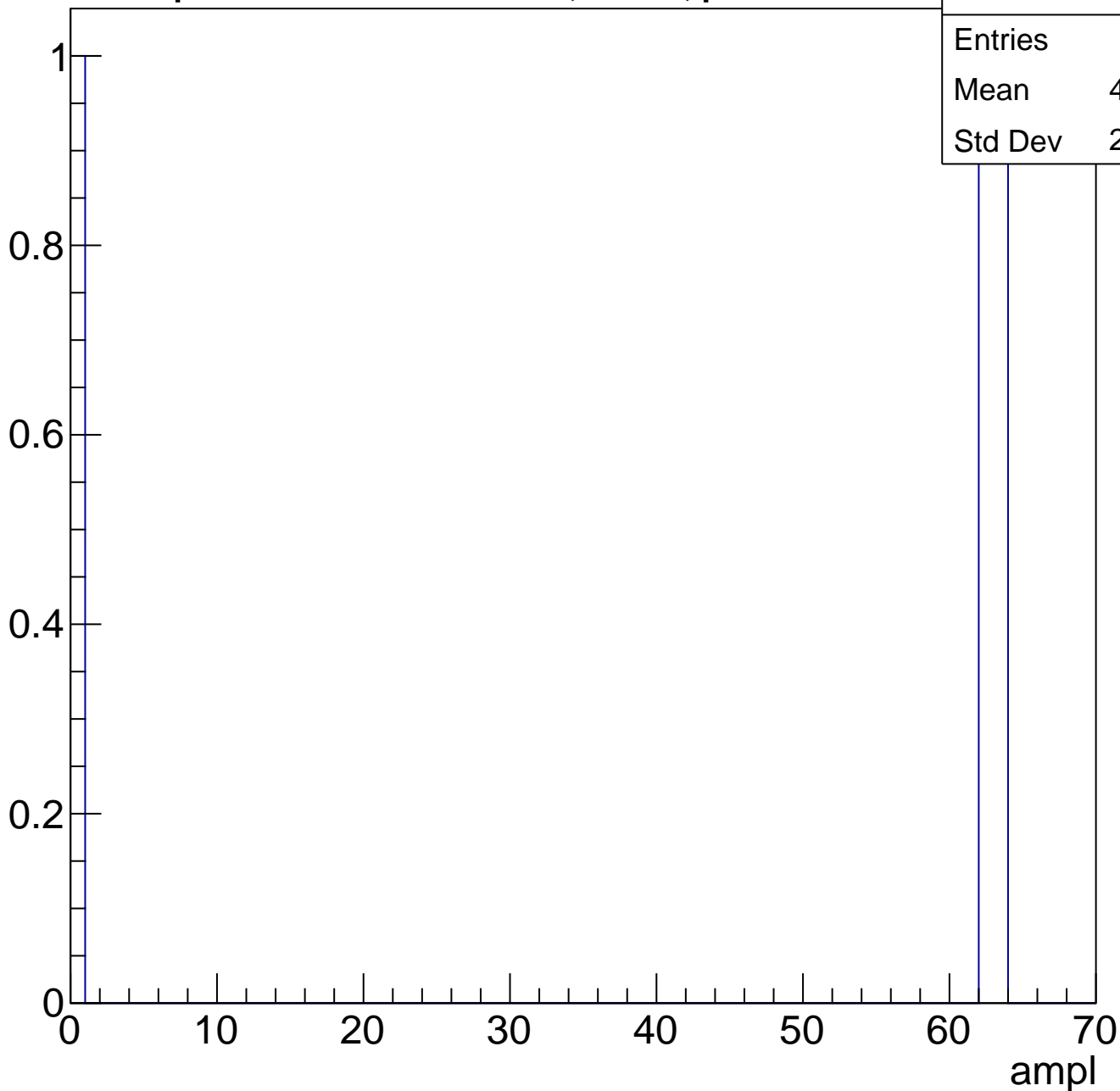
ampl



# B1L003S, U26-ch101, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch101, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U26-ch102, adc0

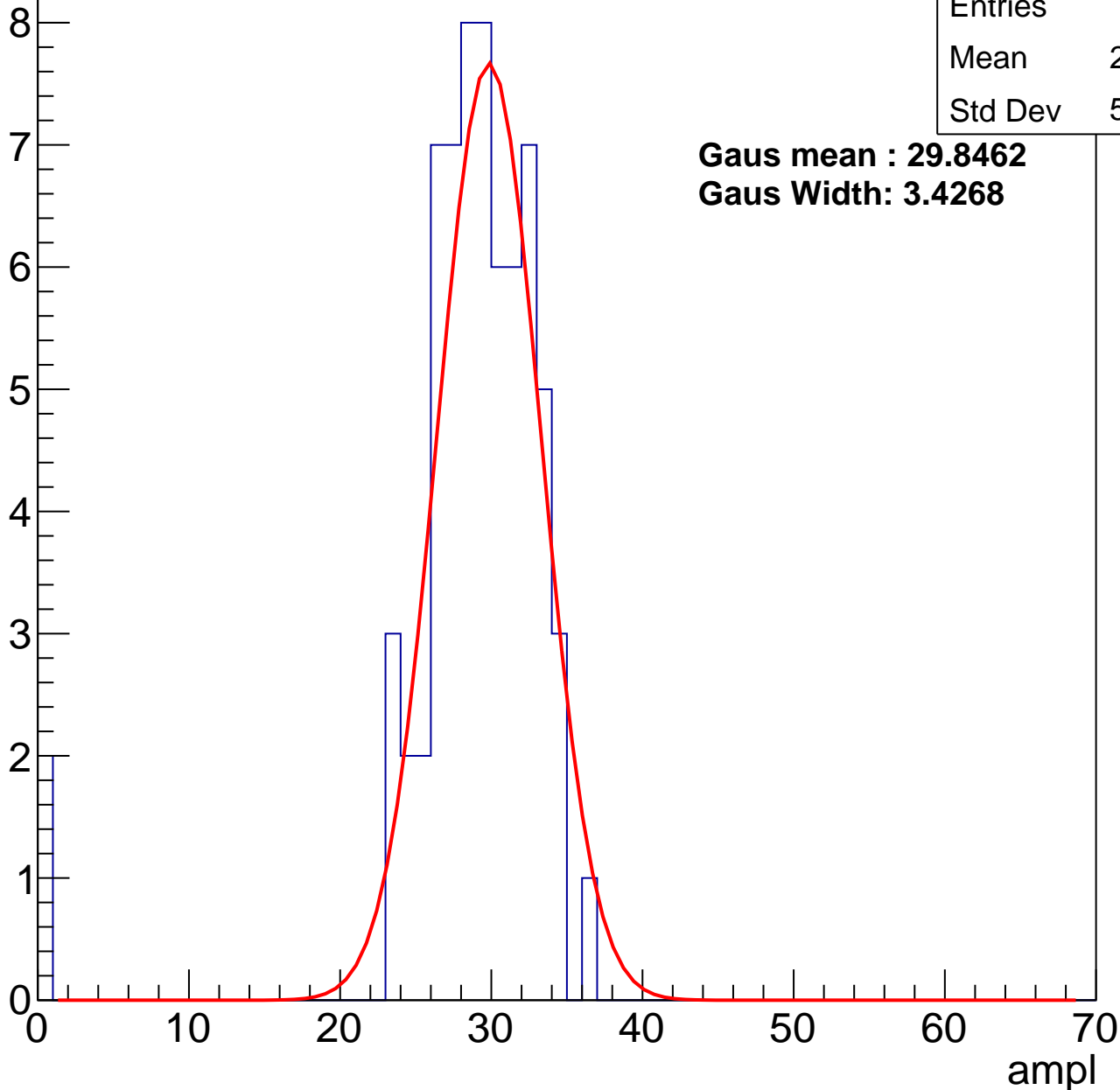
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	28.16
Std Dev	5.758

**Gaus mean : 29.8462**

**Gaus Width: 3.4268**



# B1L003S, U26-ch102, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	65
Mean	35.91
Std Dev	3.45

**Gaus mean : 36.1366**

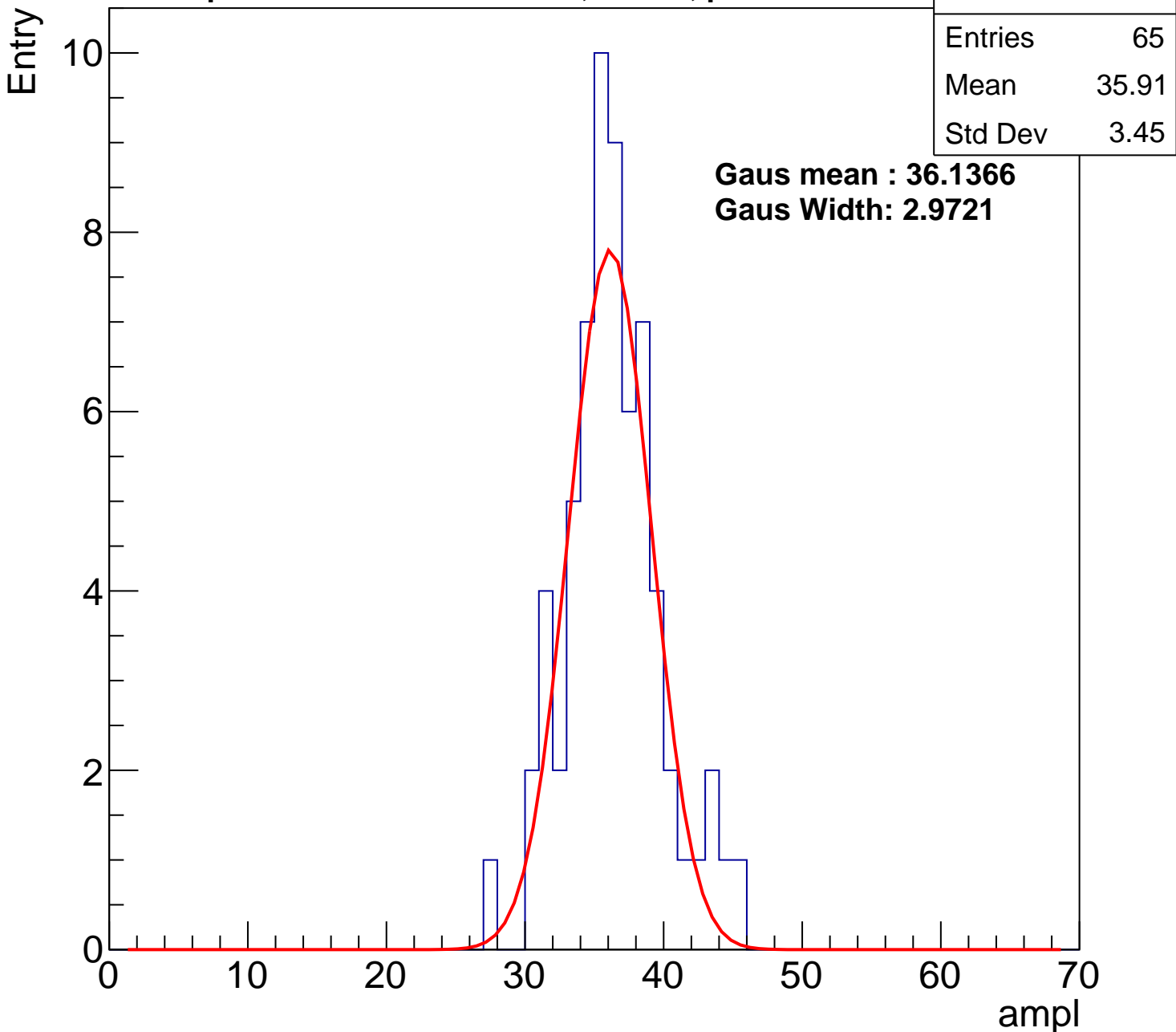
**Gaus Width: 2.9721**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U26-ch102, adc2

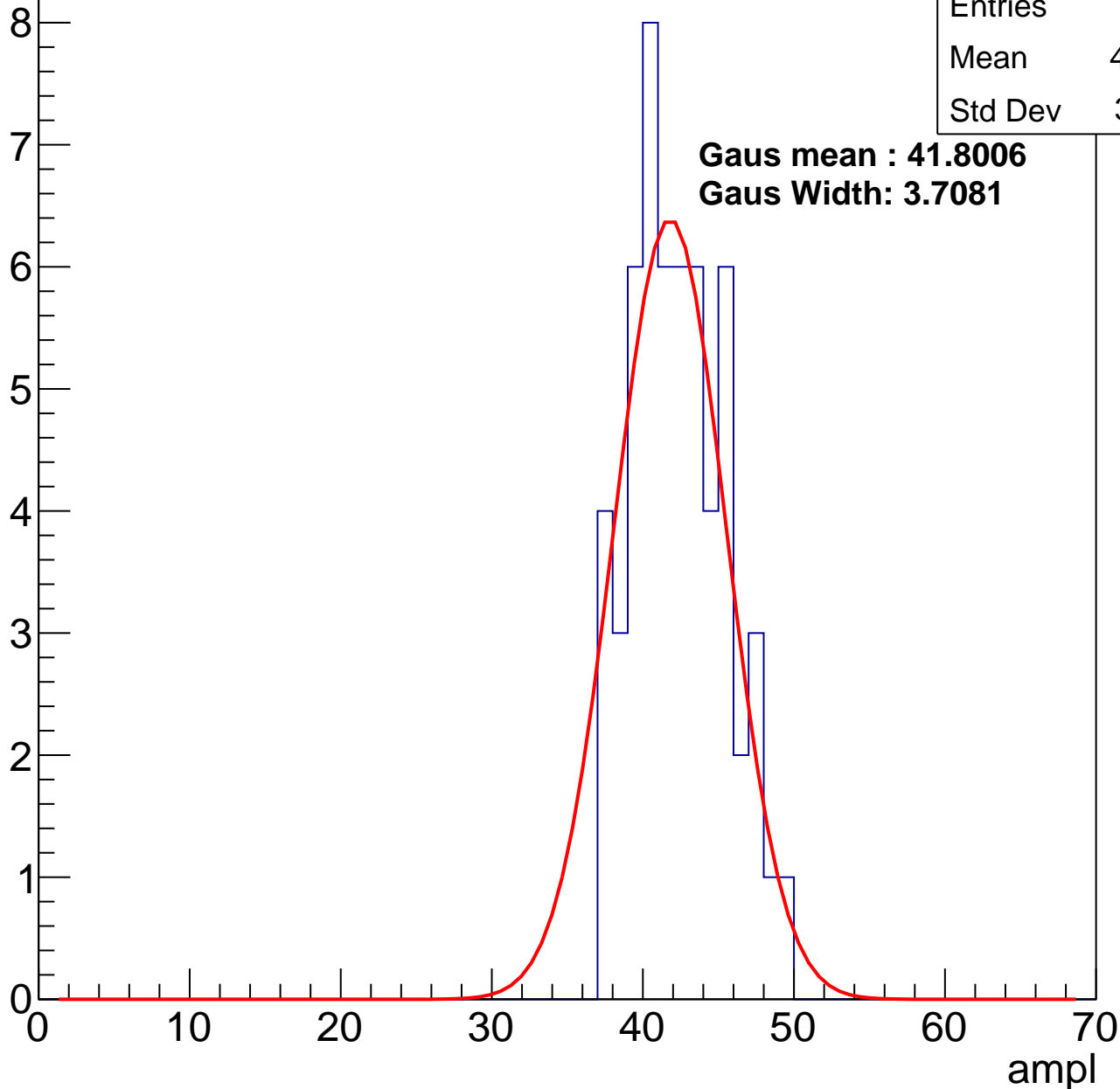
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	41.93
Std Dev	3.011

**Gaus mean : 41.8006**

**Gaus Width: 3.7081**

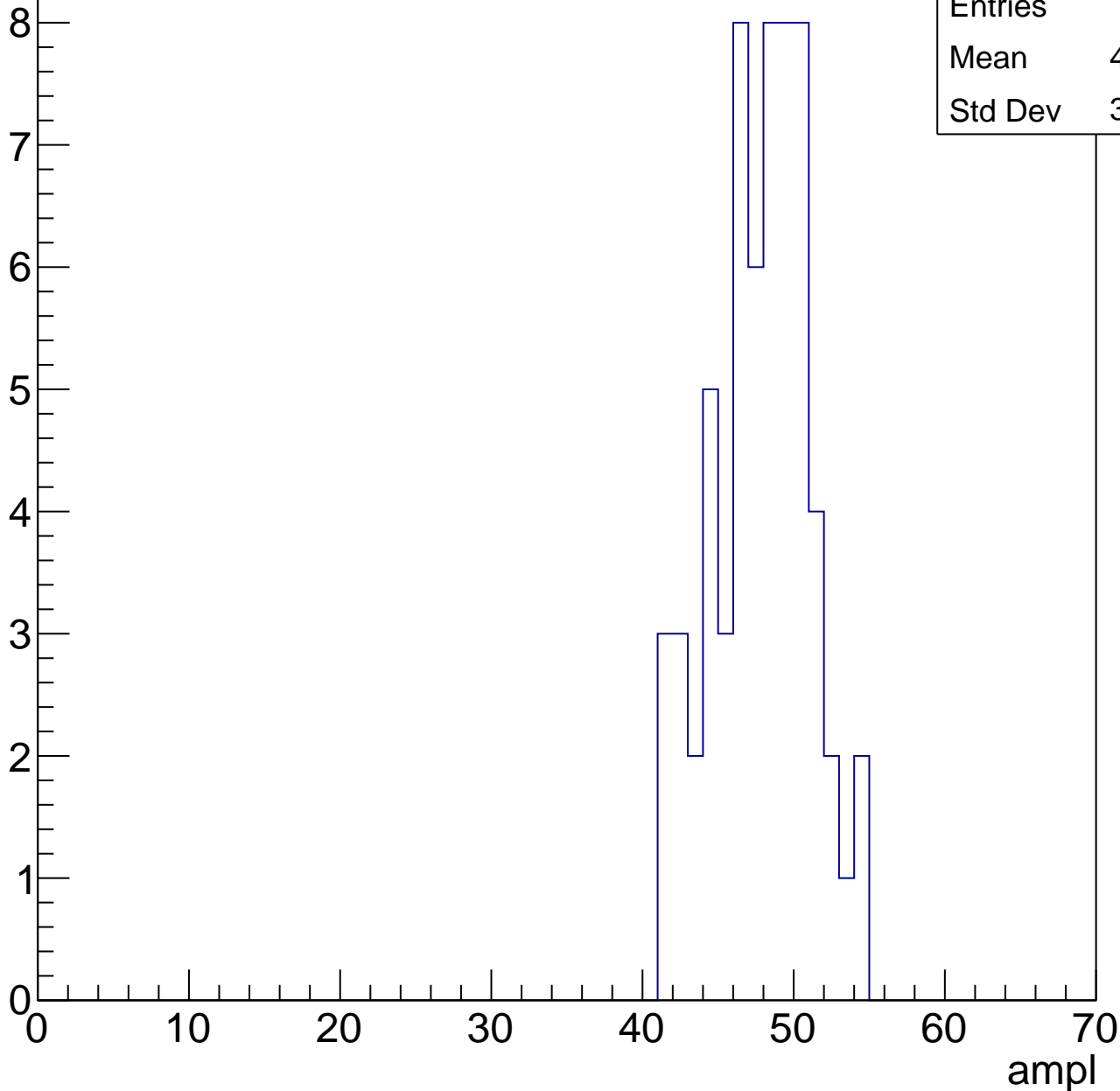


# B1L003S, U26-ch102, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	47.38
Std Dev	3.164

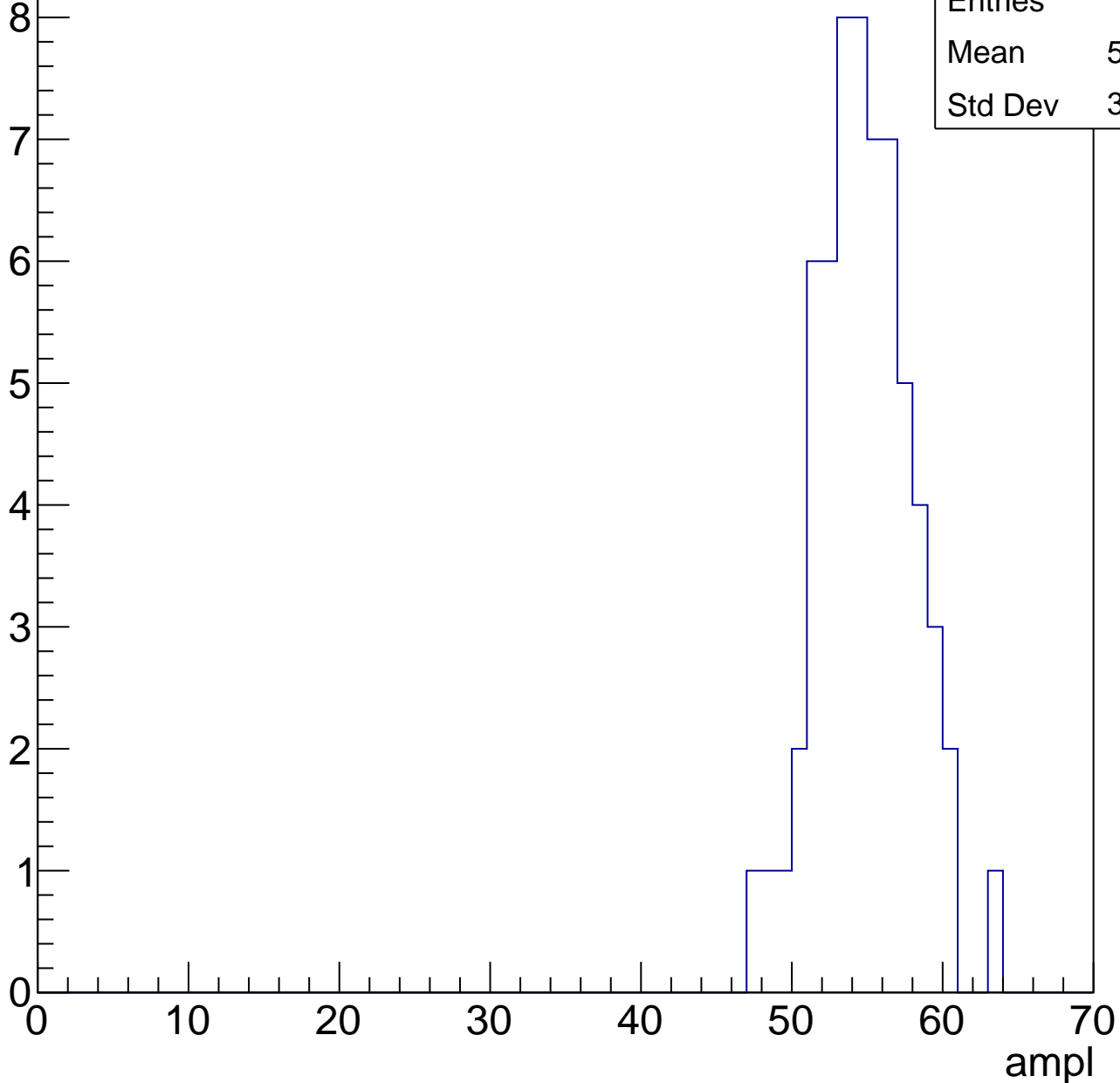


# B1L003S, U26-ch102, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	54.39
Std Dev	3.087

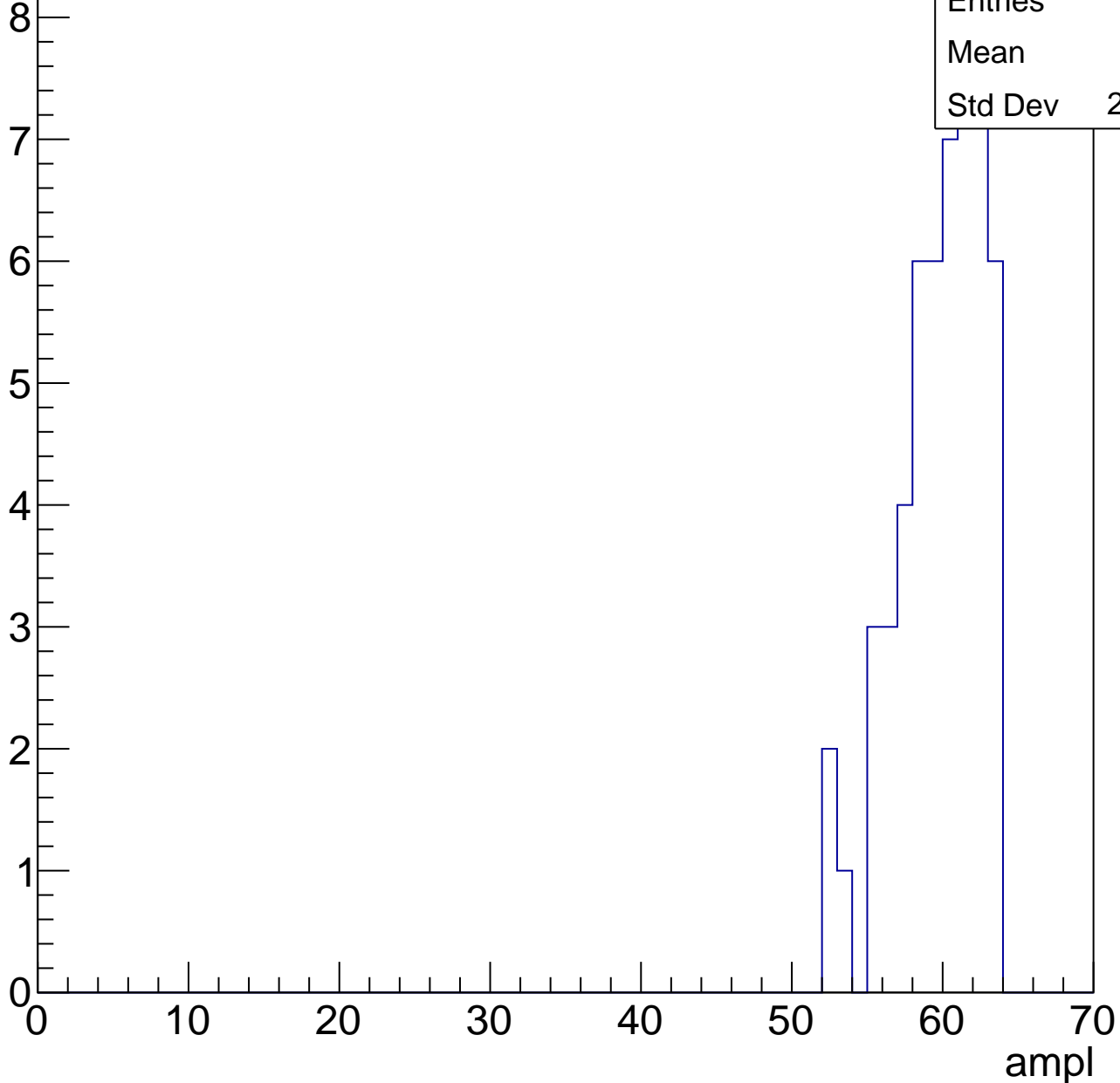


# B1L003S, U26-ch102, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	54
Mean	59.3
Std Dev	2.833



# B1L003S, U26-ch102, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

3

2.5

2

1.5

1

0.5

0

Entries

11

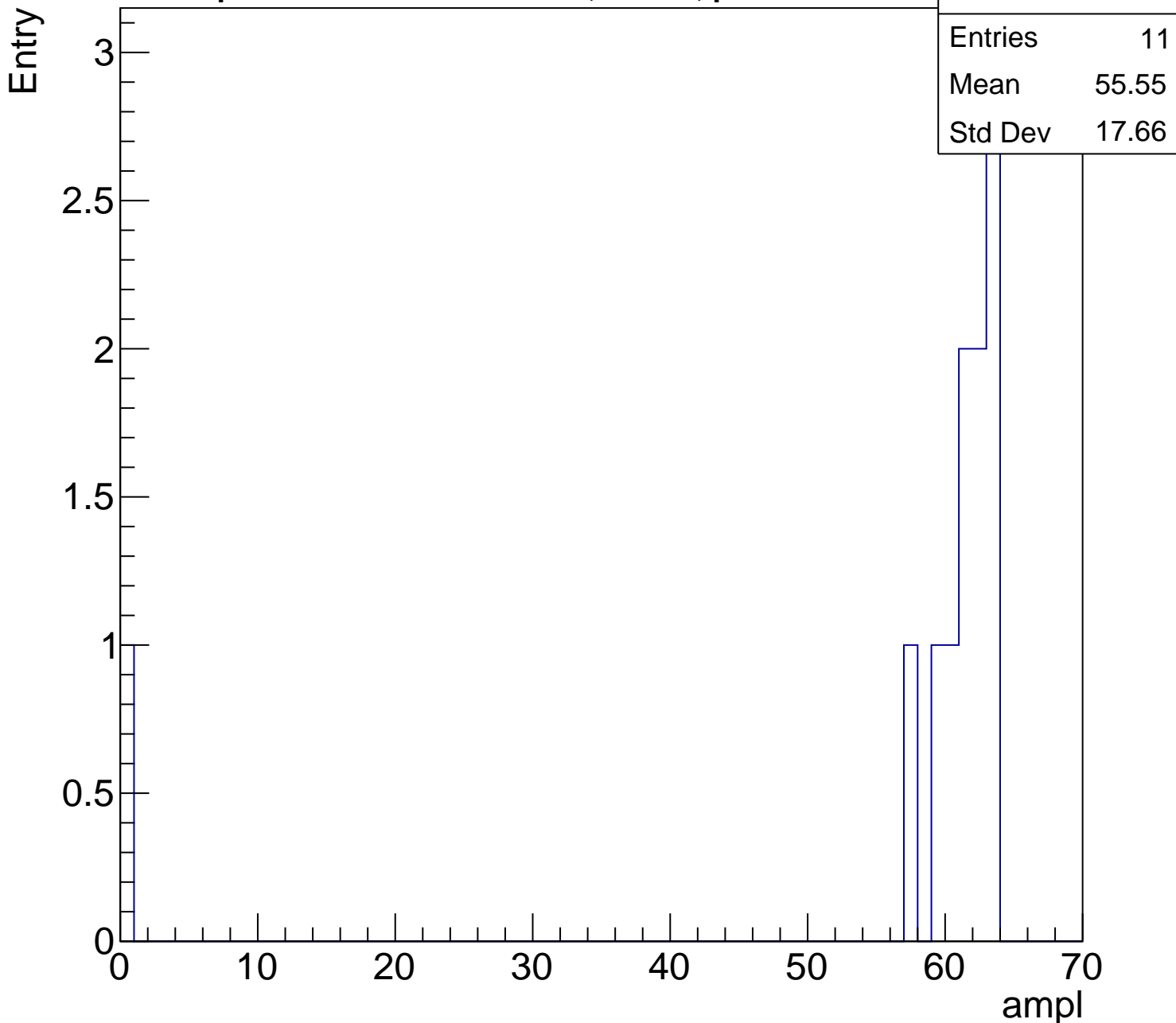
Mean

55.55

Std Dev

17.66

ampl





# B1L003S, U26-ch102, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

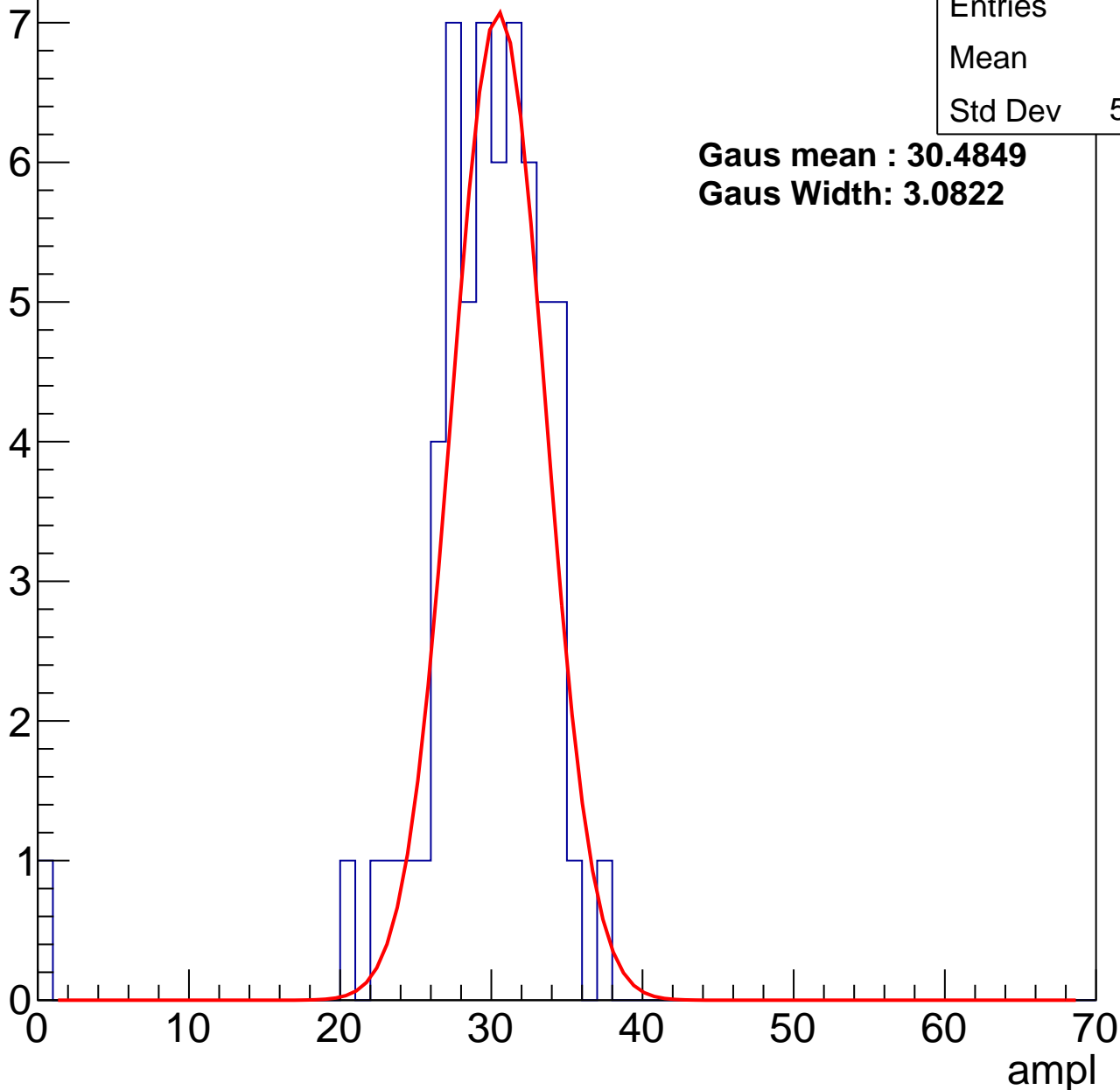
# B1L003S, U26-ch103, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	29.1
Std Dev	5.016

**Gaus mean : 30.4849**  
**Gaus Width: 3.0822**



# B1L003S, U26-ch103, adc1

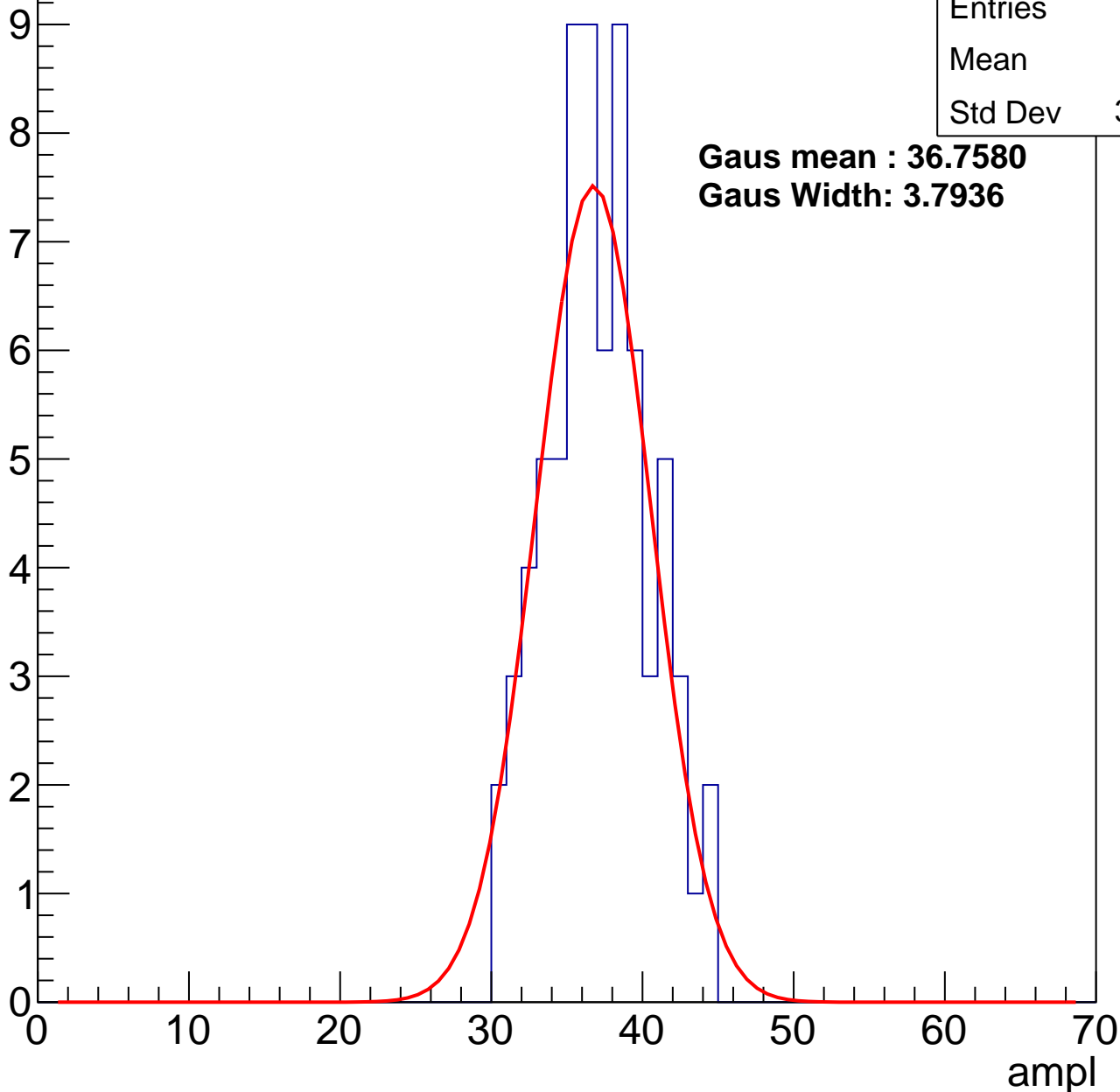
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	72
Mean	36.6
Std Dev	3.361

**Gaus mean : 36.7580**

**Gaus Width: 3.7936**



# B1L003S, U26-ch103, adc2

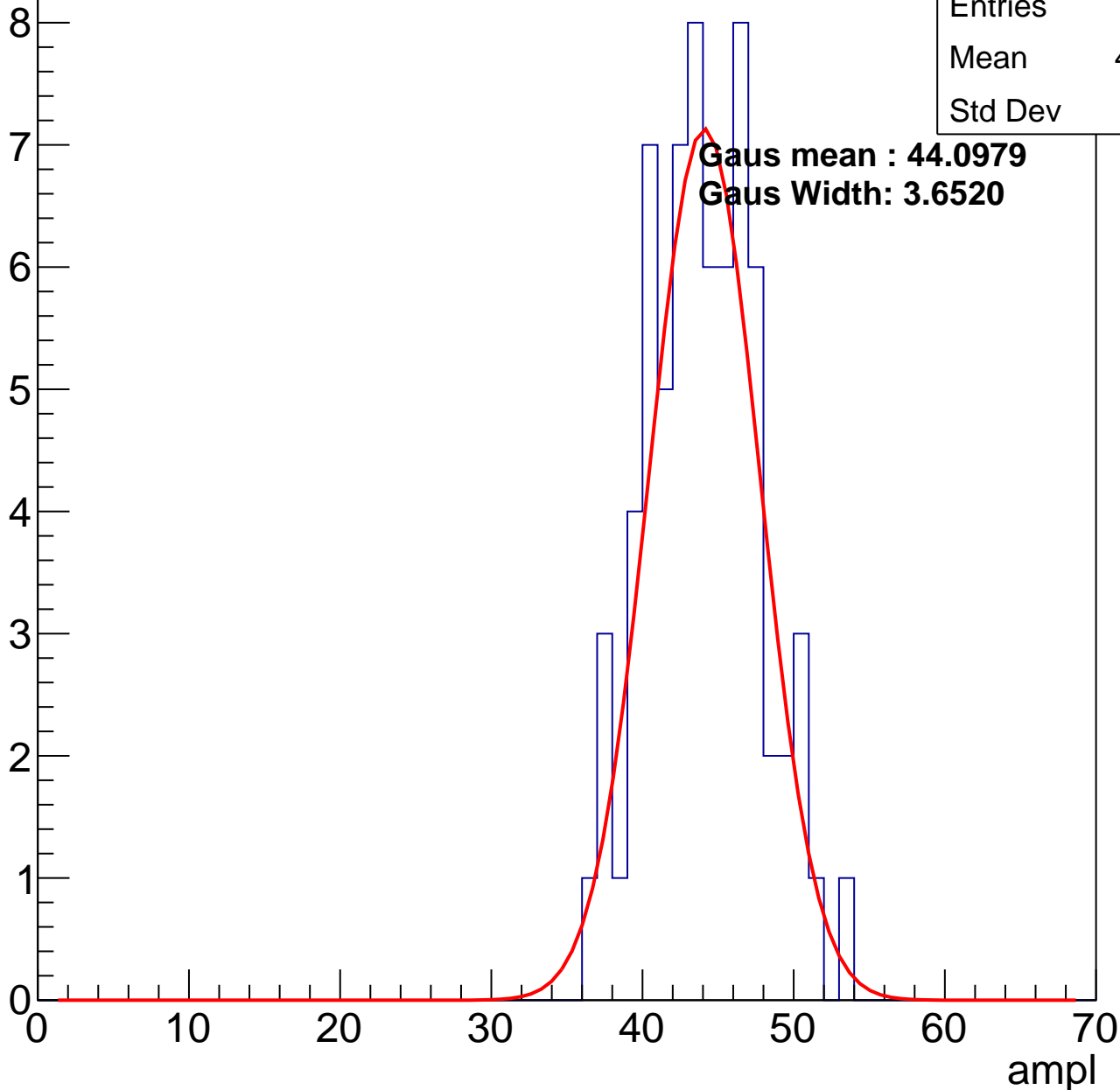
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	71
Mean	43.61
Std Dev	3.64

**Gaus mean : 44.0979**

**Gaus Width: 3.6520**

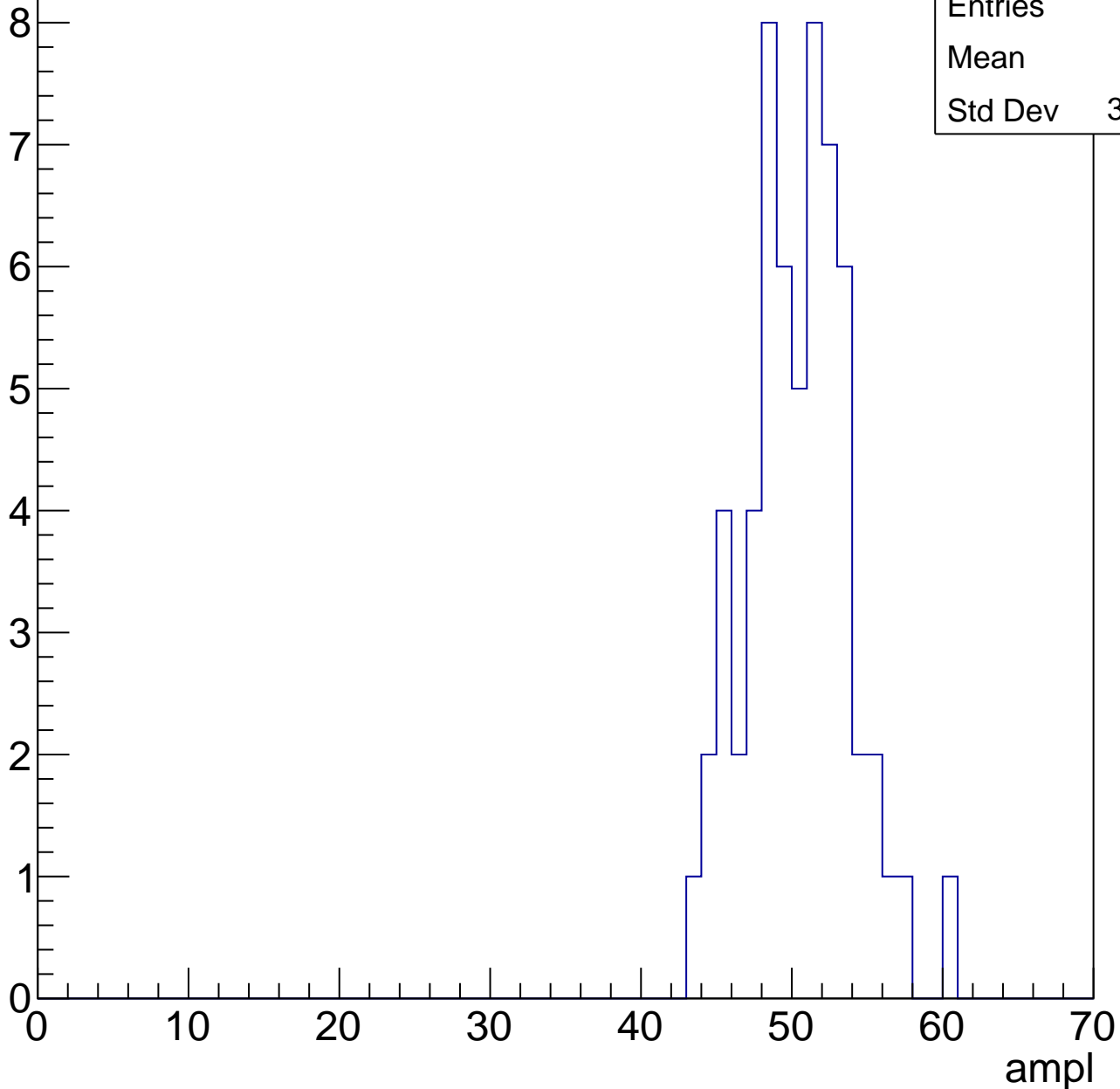


# B1L003S, U26-ch103, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	50
Std Dev	3.376

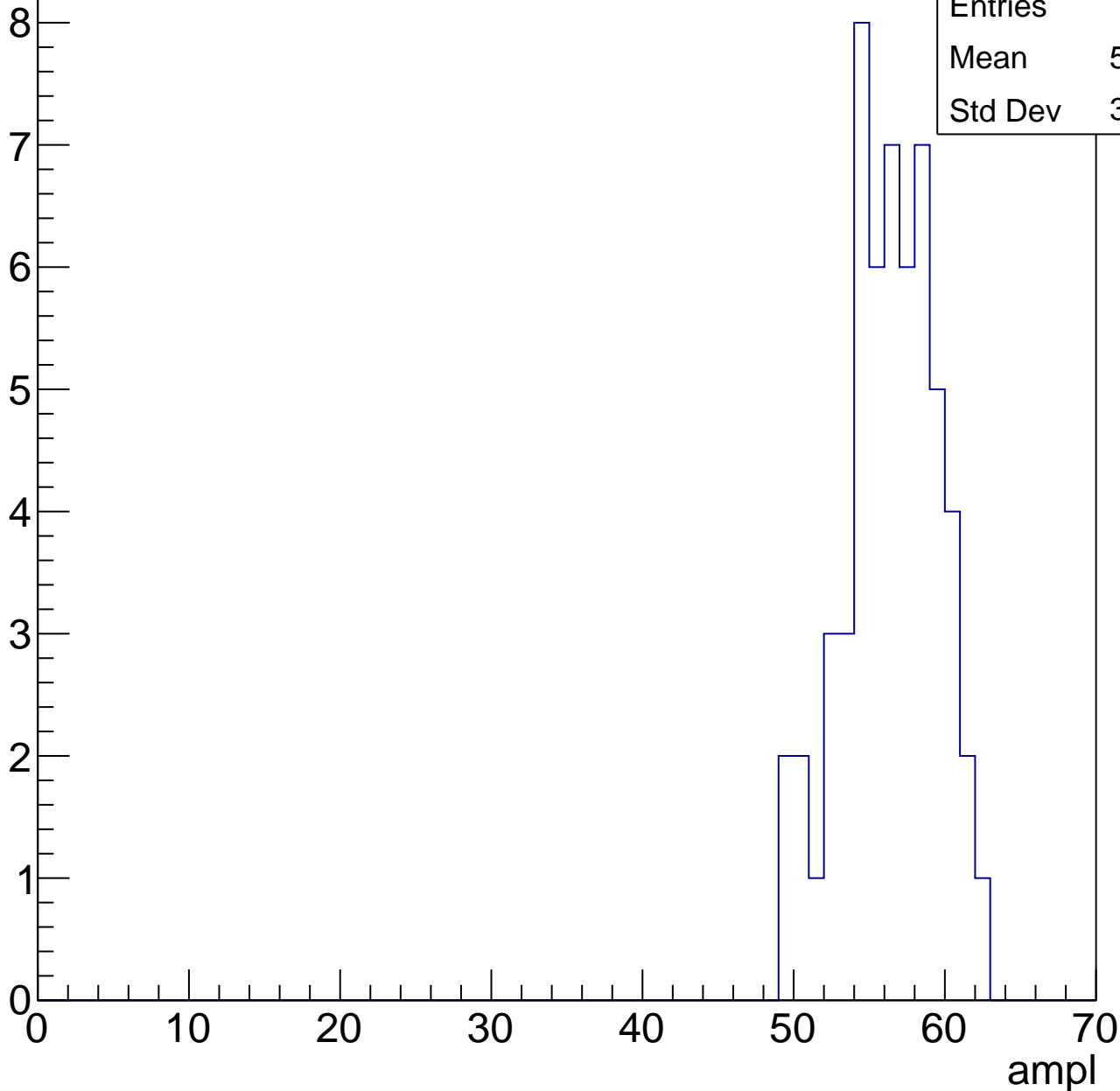


# B1L003S, U26-ch103, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	55.88
Std Dev	3.067

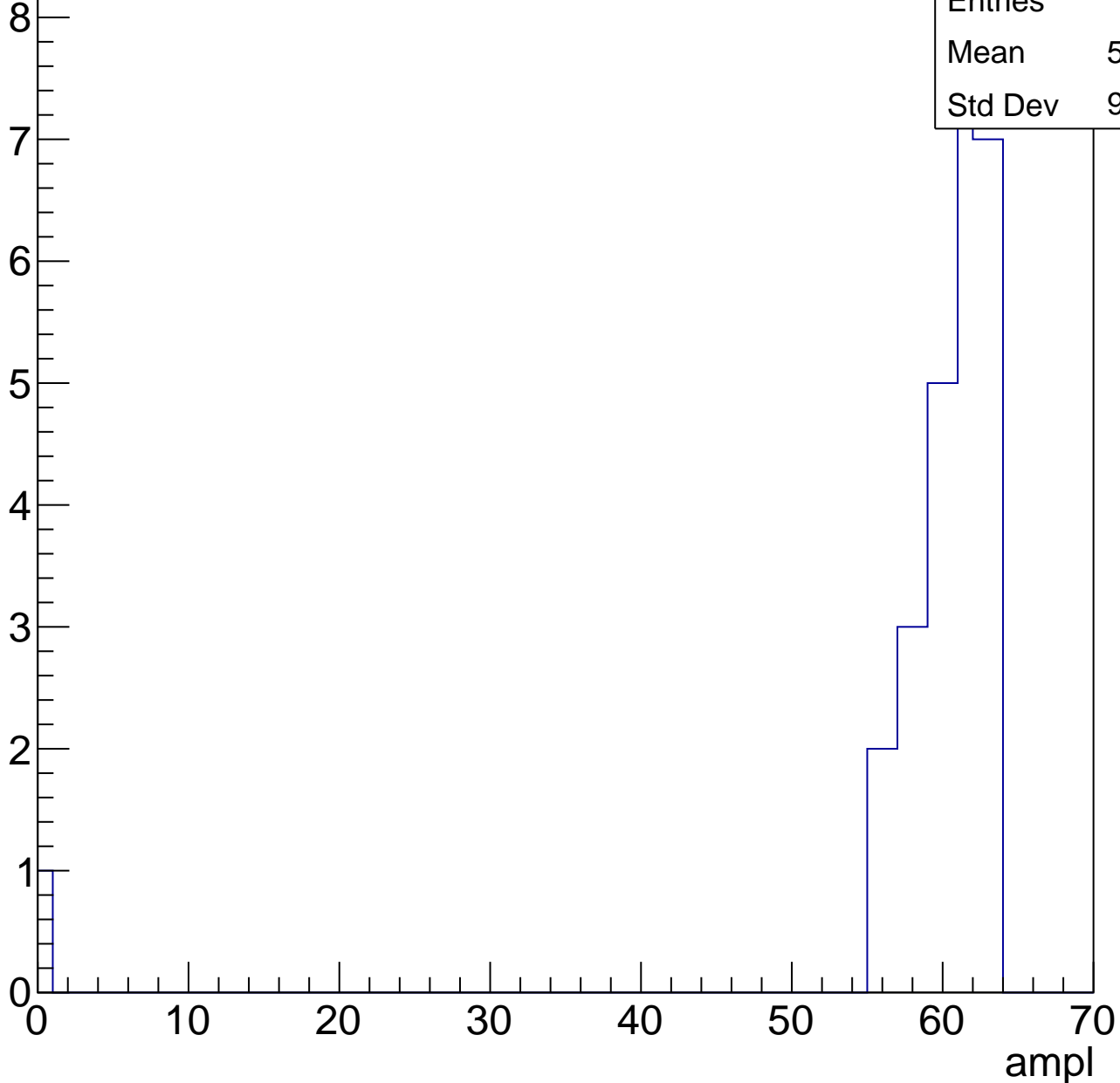


# B1L003S, U26-ch103, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

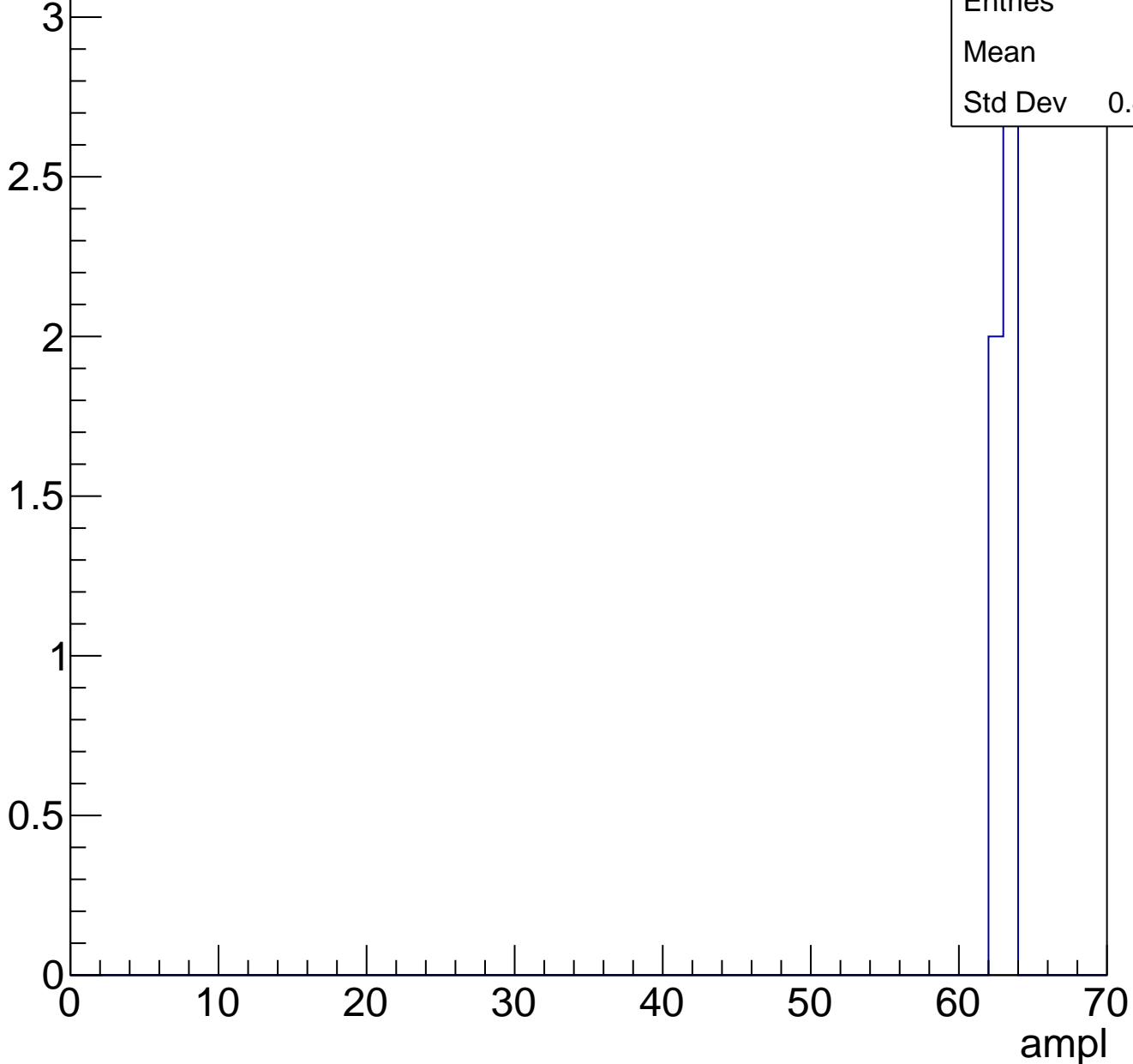
Entries	43
Mean	58.72
Std Dev	9.344



# B1L003S, U26-ch103, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch103, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U26-ch104, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	67
Mean	27.78
Std Dev	5.646

**Gaus mean : 29.3163**

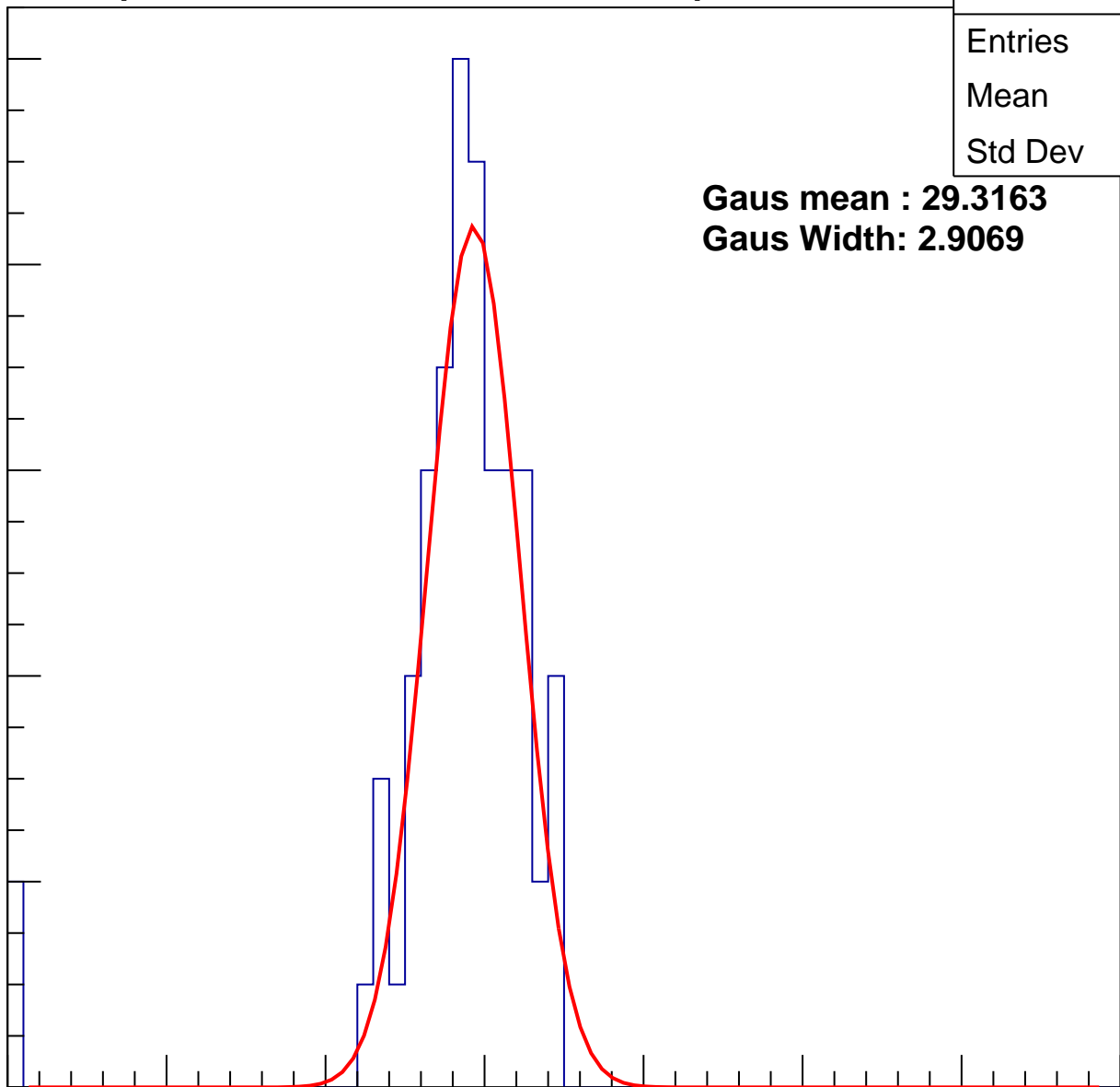
**Gaus Width: 2.9069**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U26-ch104, adc1

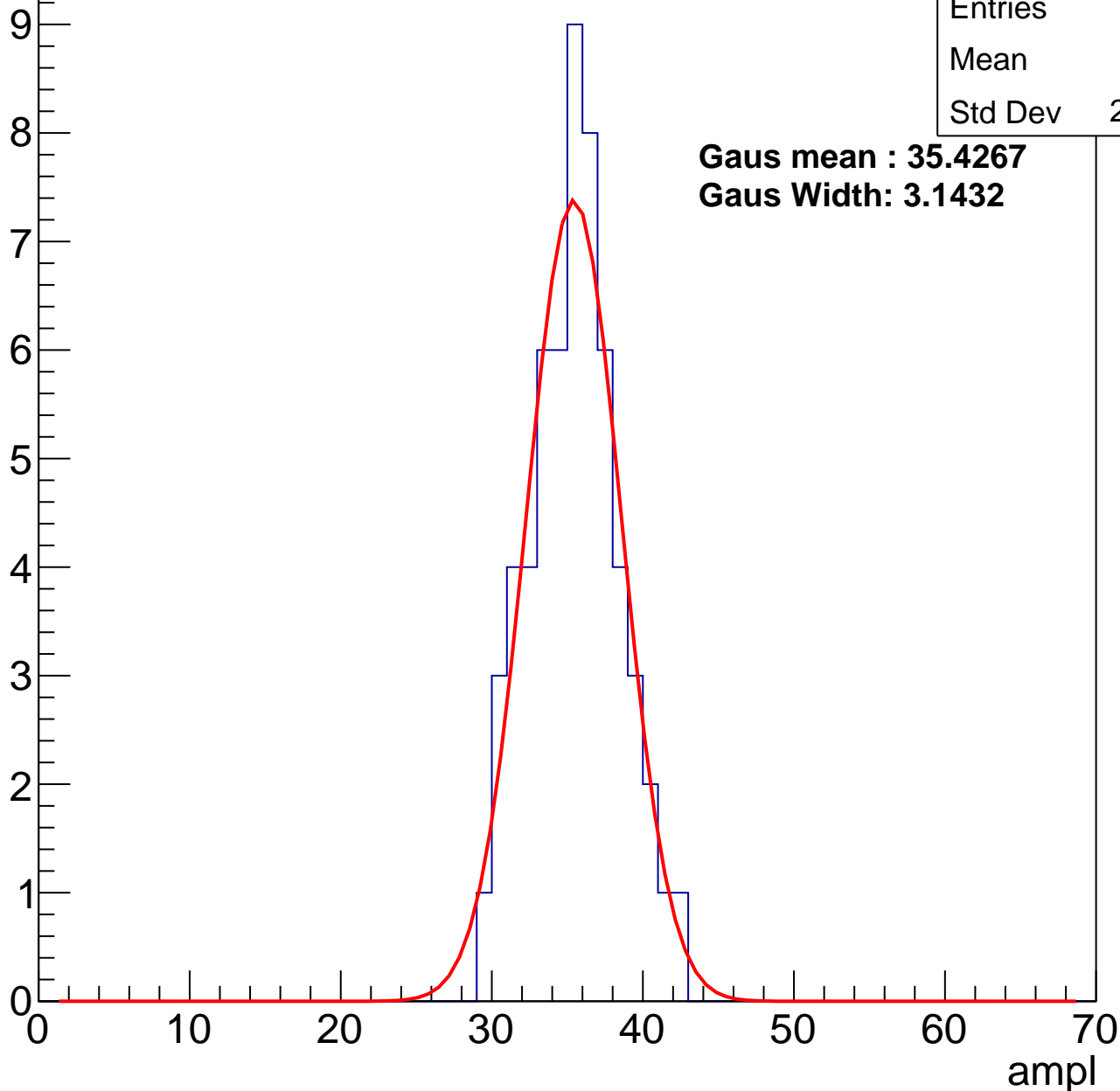
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	35
Std Dev	2.913

**Gaus mean : 35.4267**

**Gaus Width: 3.1432**



# B1L003S, U26-ch104, adc2

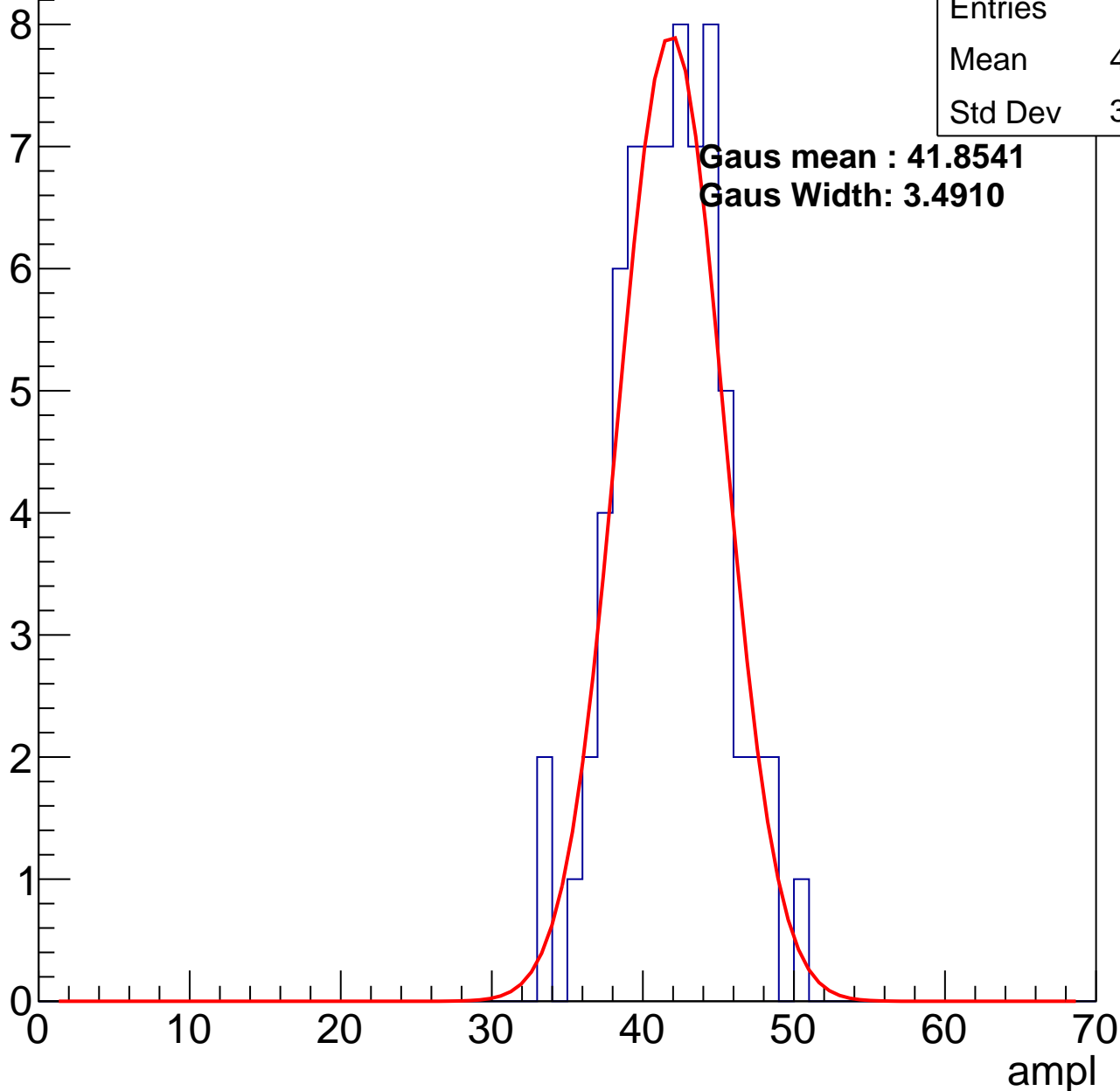
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	71
Mean	41.34
Std Dev	3.456

**Gaus mean : 41.8541**

**Gaus Width: 3.4910**

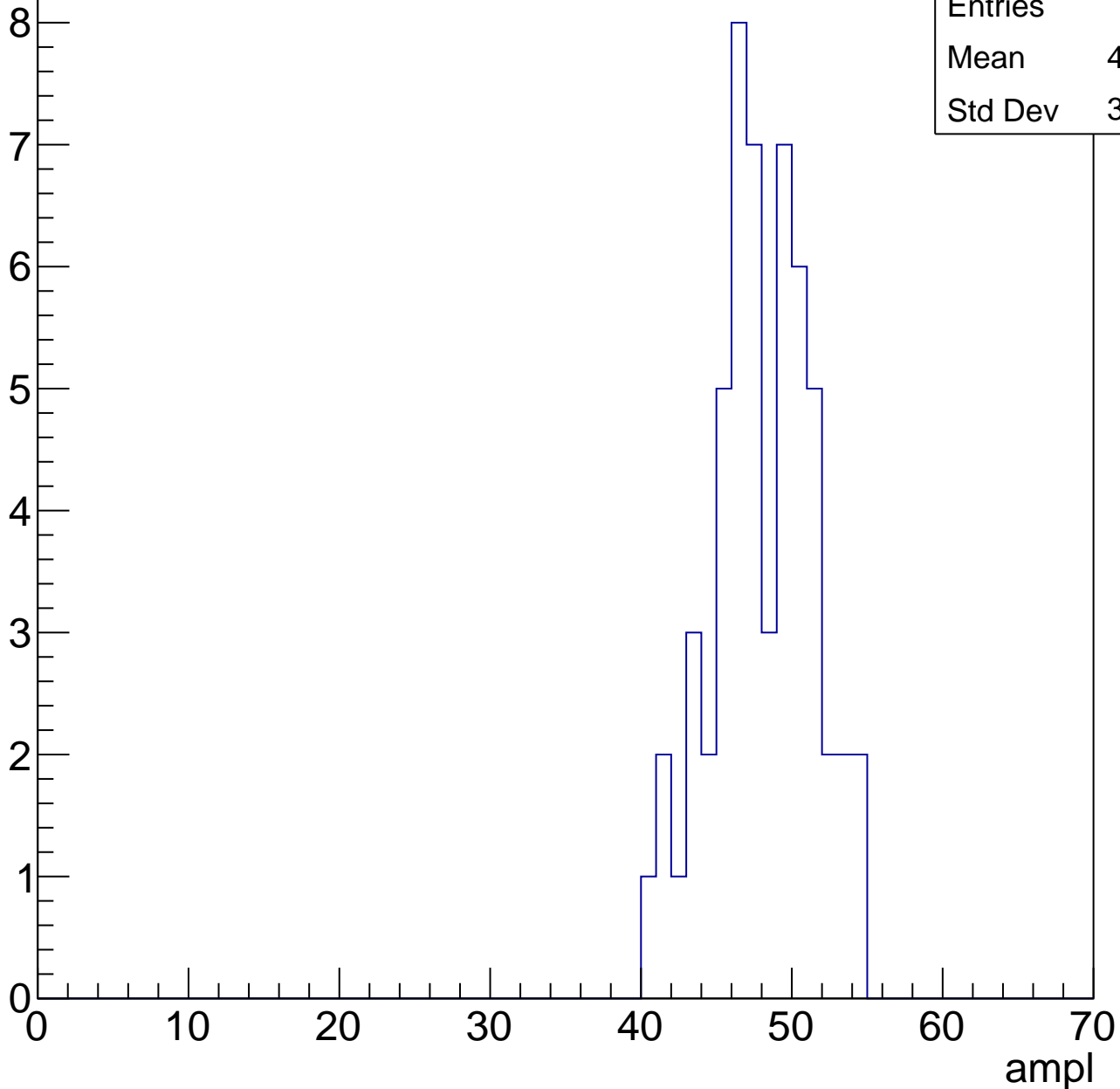


# B1L003S, U26-ch104, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

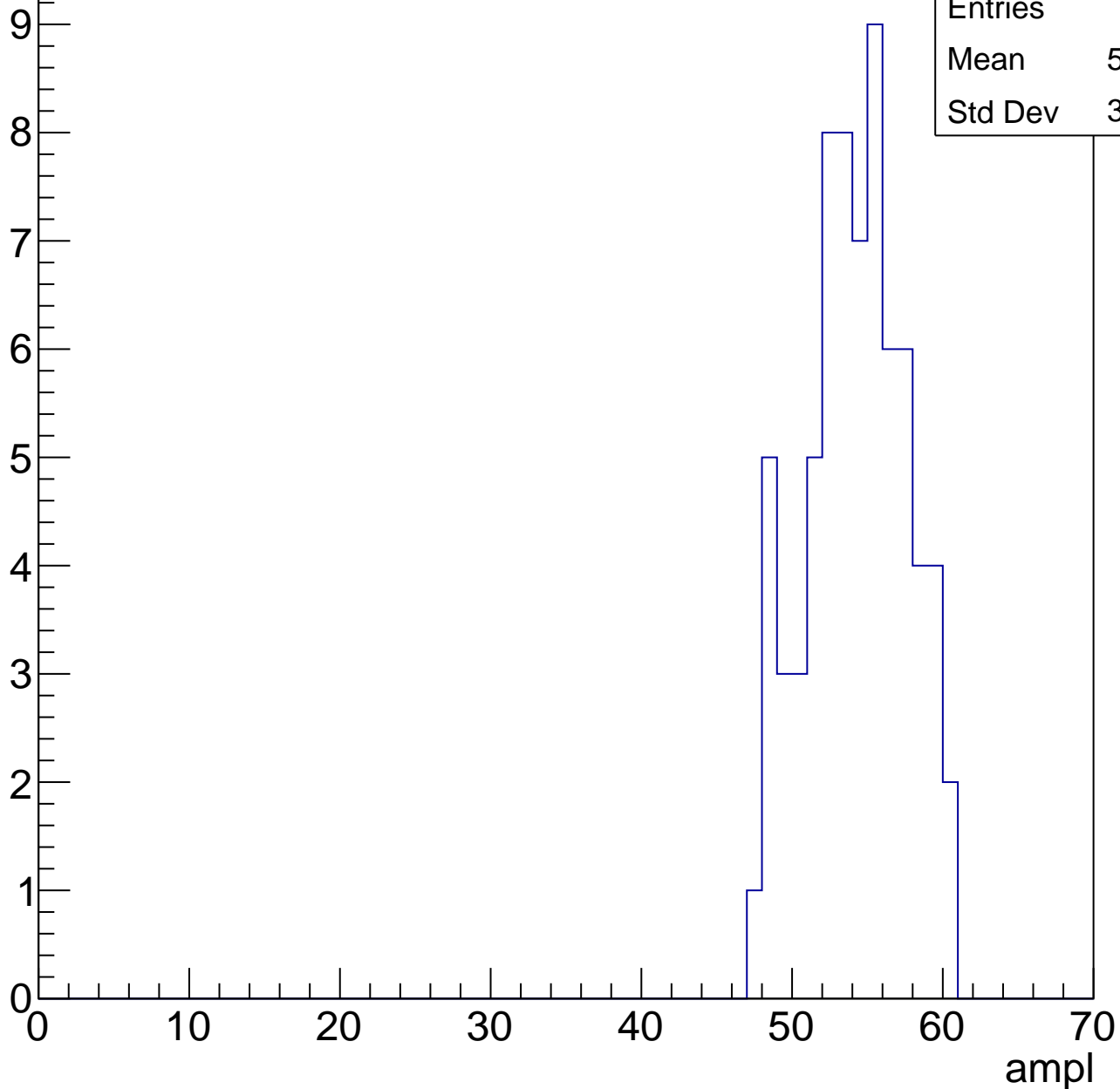
Entries	56
Mean	47.55
Std Dev	3.295



# B1L003S, U26-ch104, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



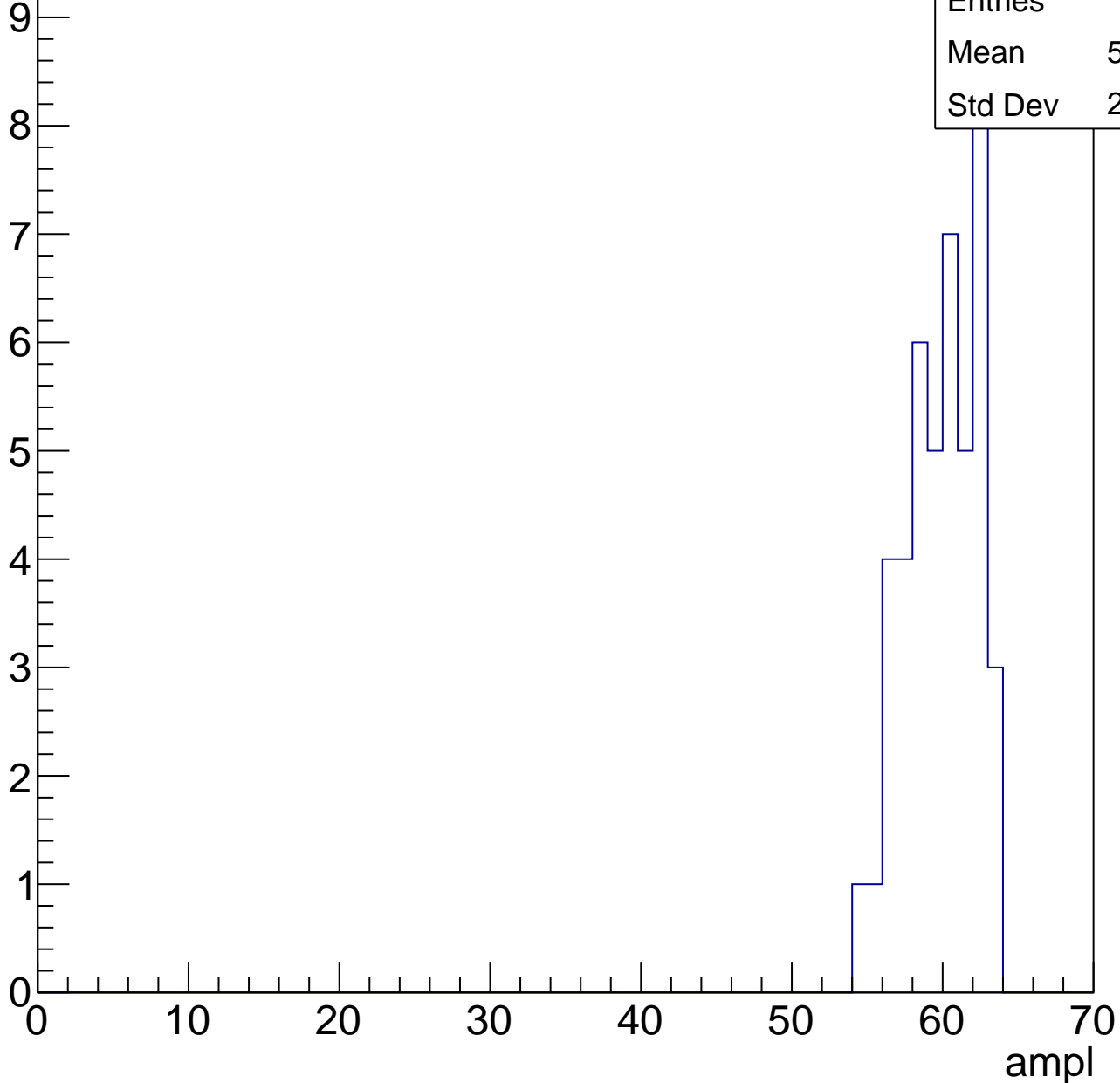
Entries	71
Mean	53.77
Std Dev	3.264

# B1L003S, U26-ch104, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	45
Mean	59.47
Std Dev	2.334

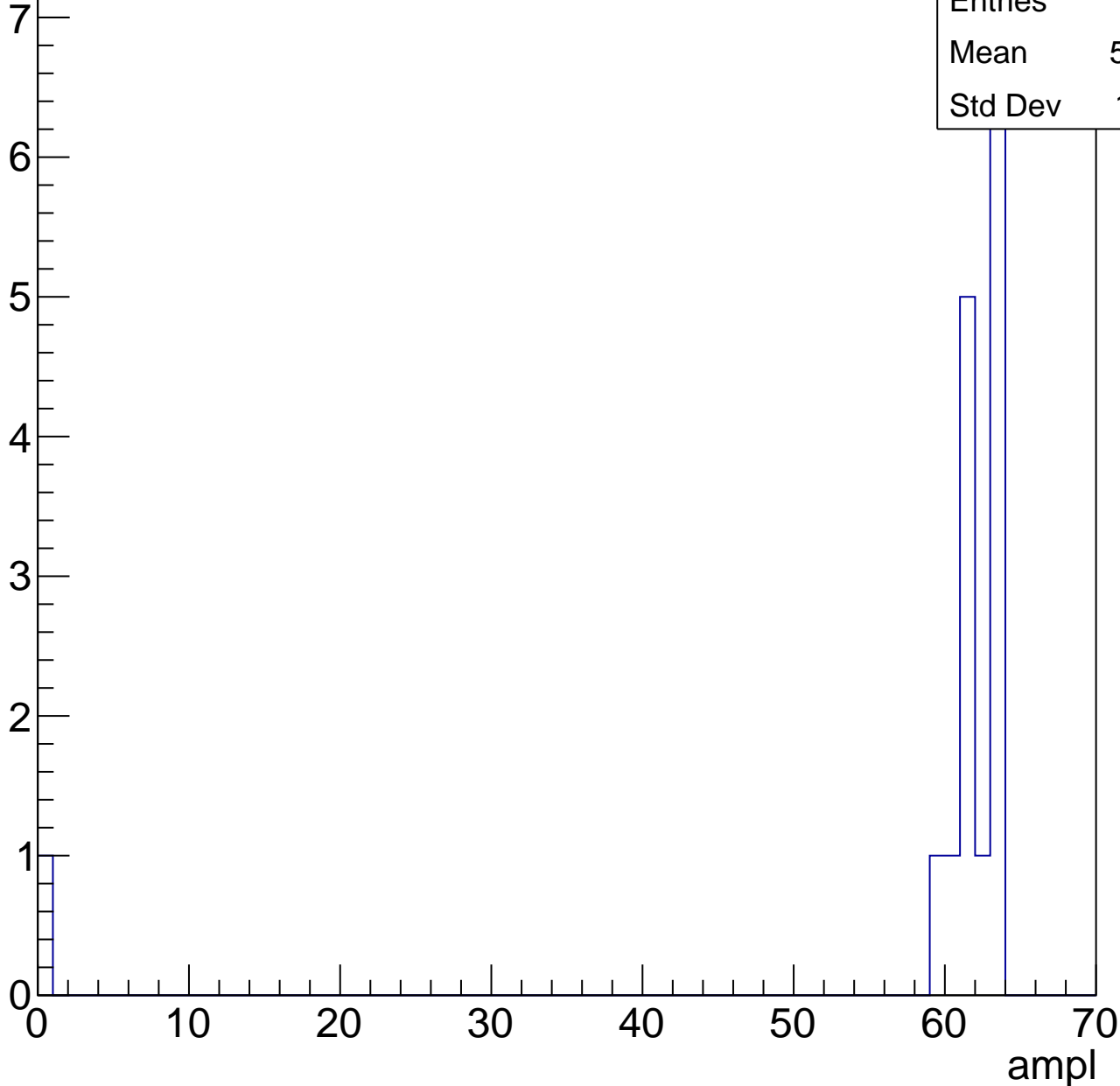


# B1L003S, U26-ch104, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	16
Mean	57.94
Std Dev	15.01





# B1L003S, U26-ch104, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U26-ch105, adc0

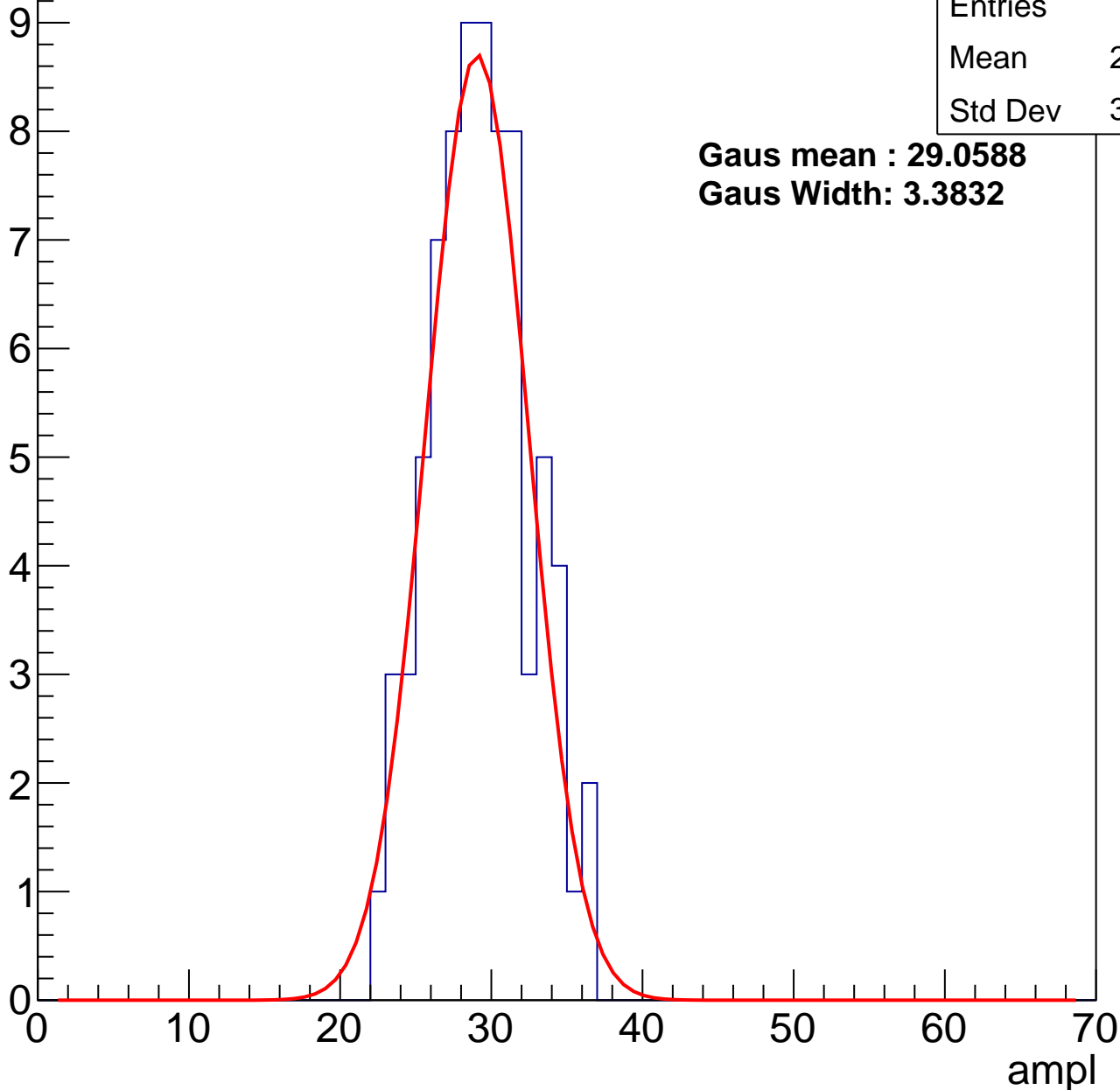
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	76
Mean	28.83
Std Dev	3.234

**Gaus mean : 29.0588**

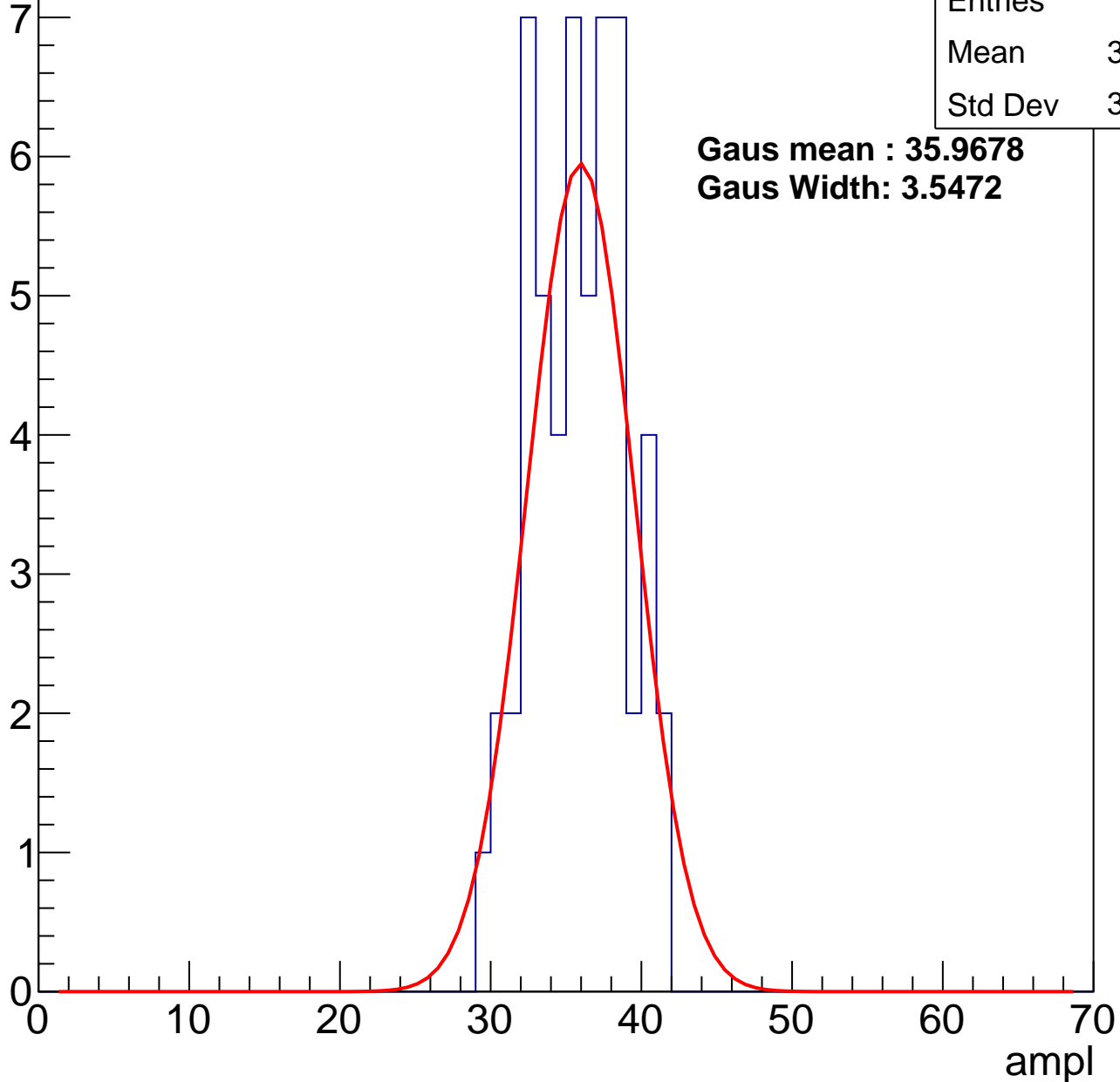
**Gaus Width: 3.3832**



# B1L003S, U26-ch105, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U26-ch105, adc2

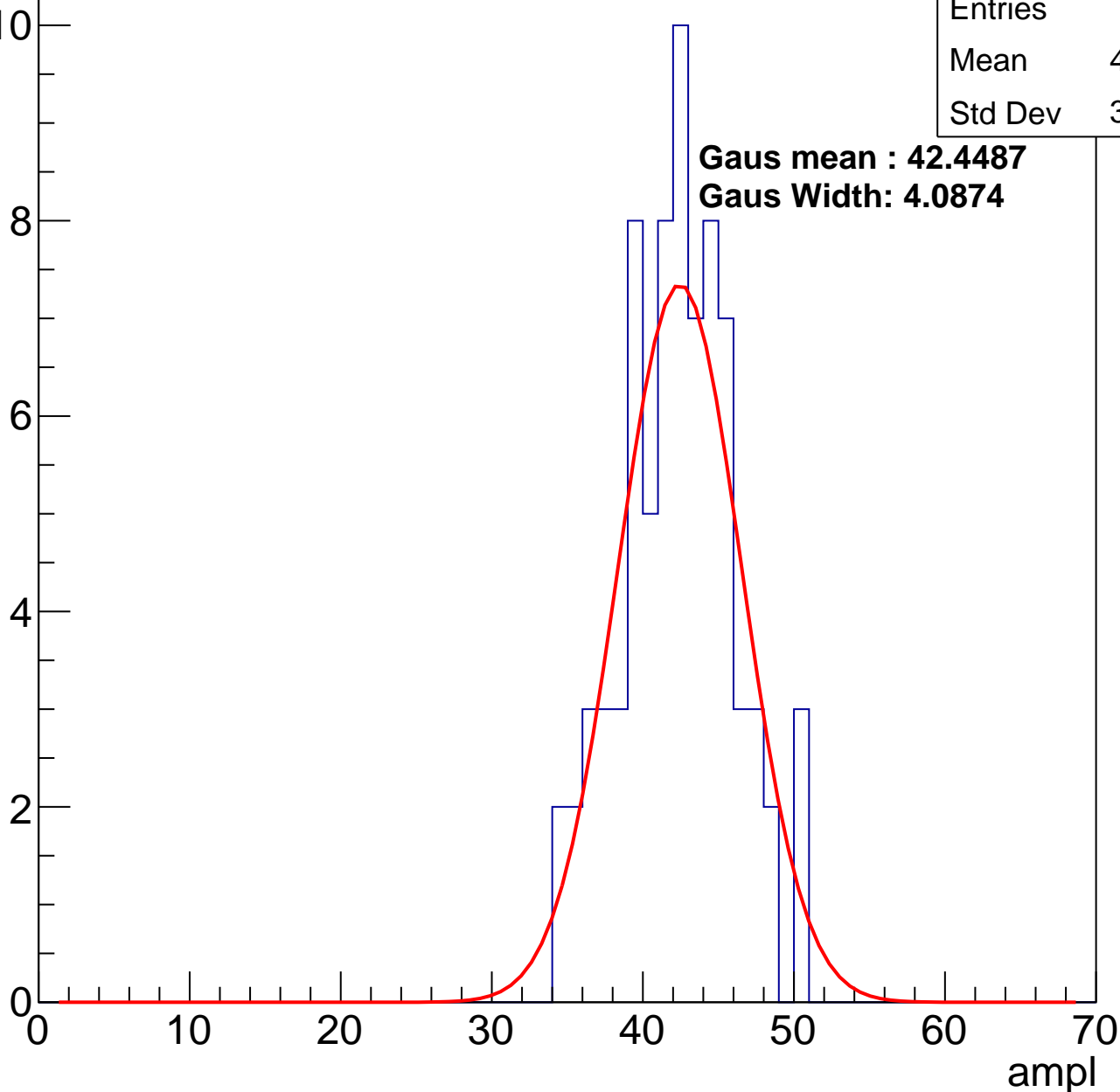
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	77
Mean	41.87
Std Dev	3.683

**Gaus mean : 42.4487**

**Gaus Width: 4.0874**

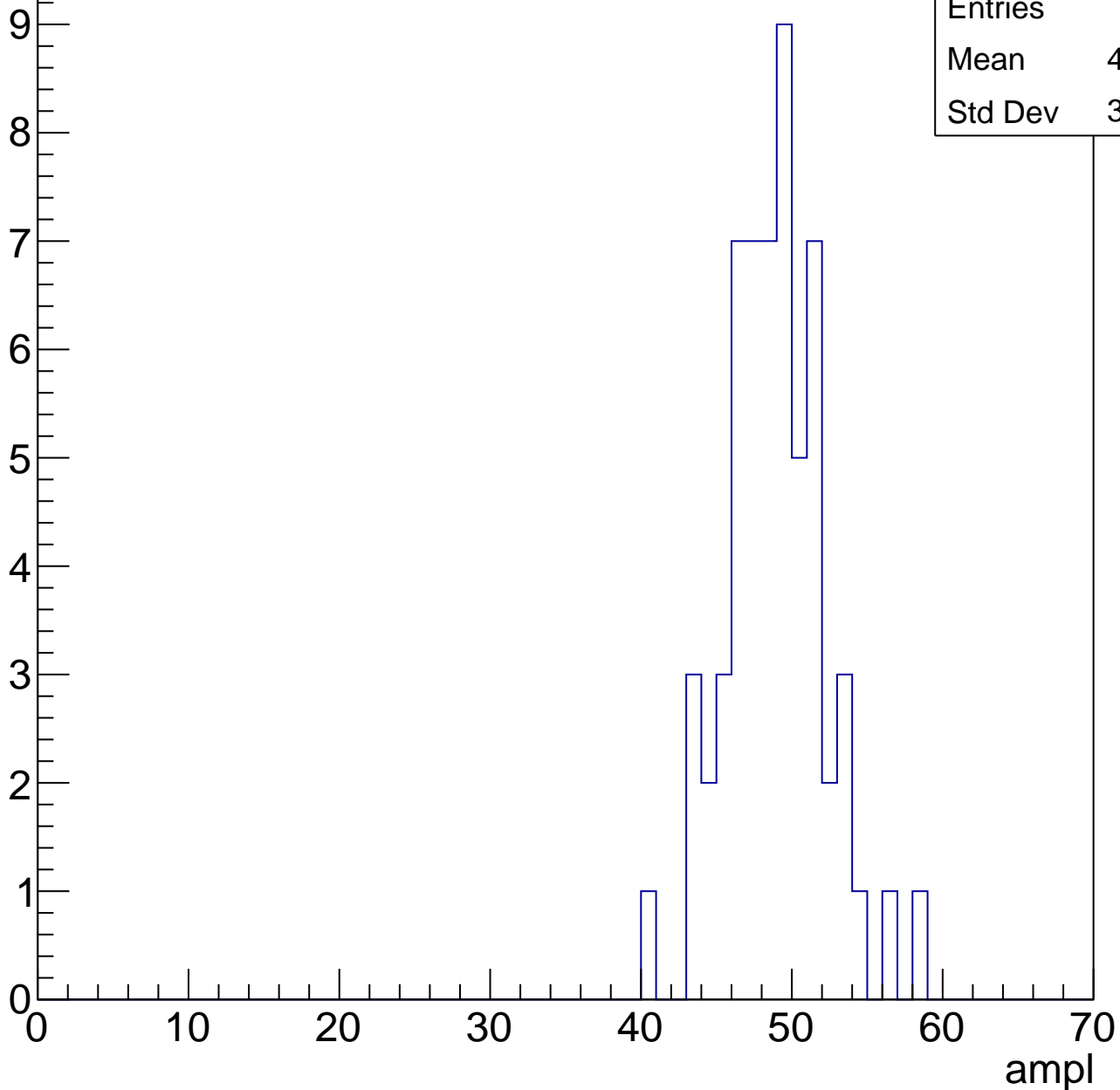


# B1L003S, U26-ch105, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	48.44
Std Dev	3.243

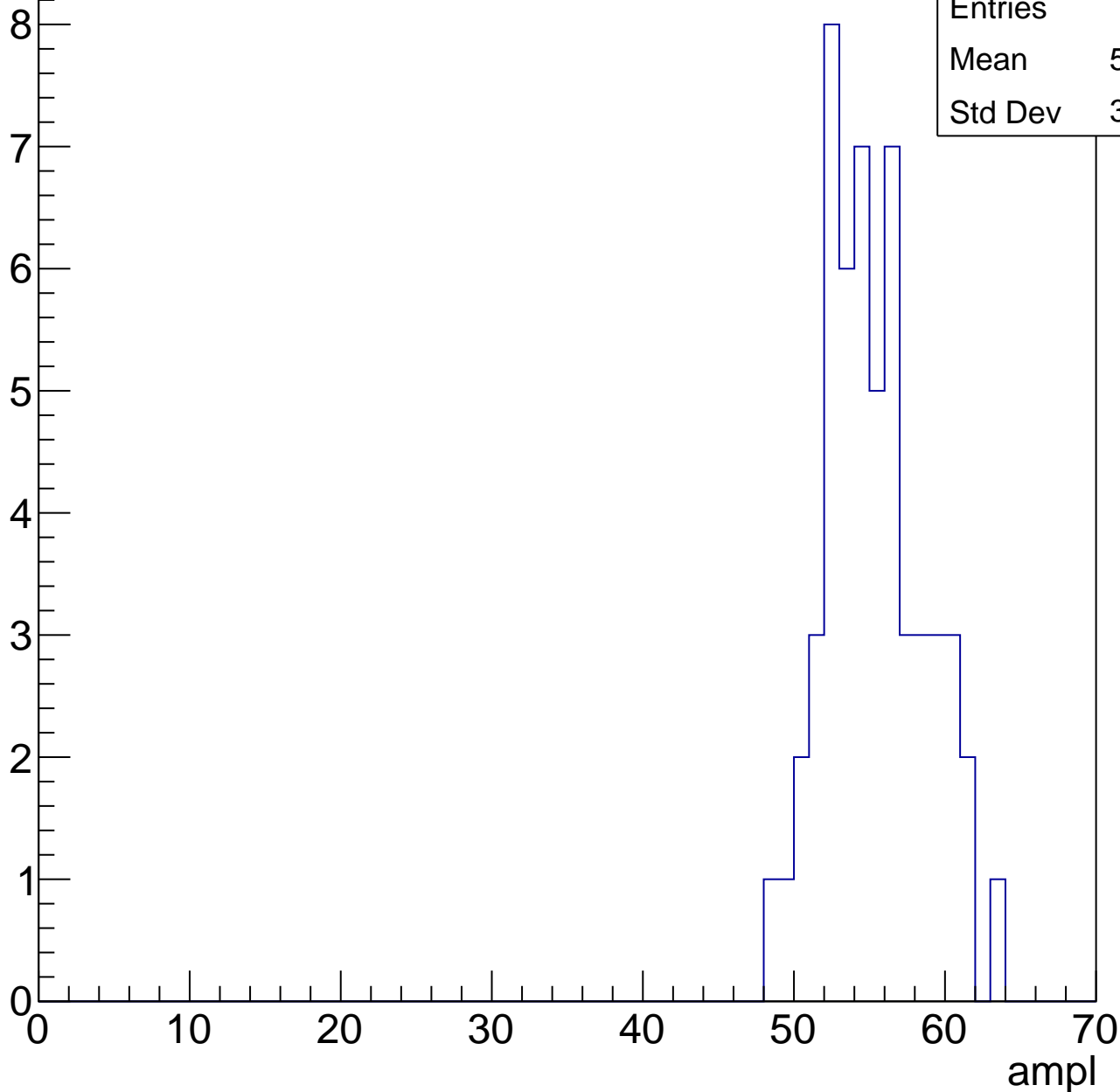


# B1L003S, U26-ch105, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	54.84
Std Dev	3.274

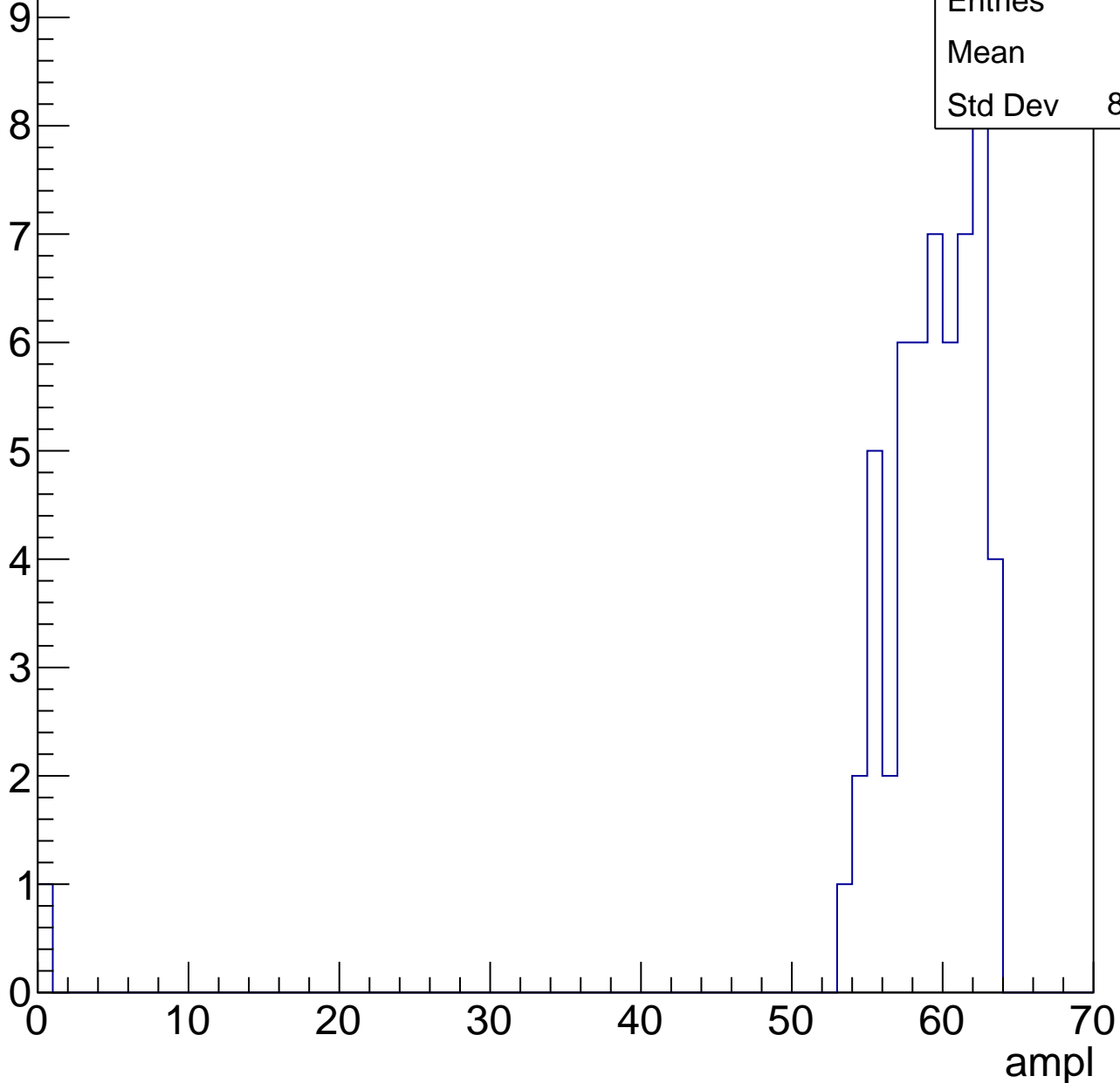


# B1L003S, U26-ch105, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	58
Std Dev	8.257

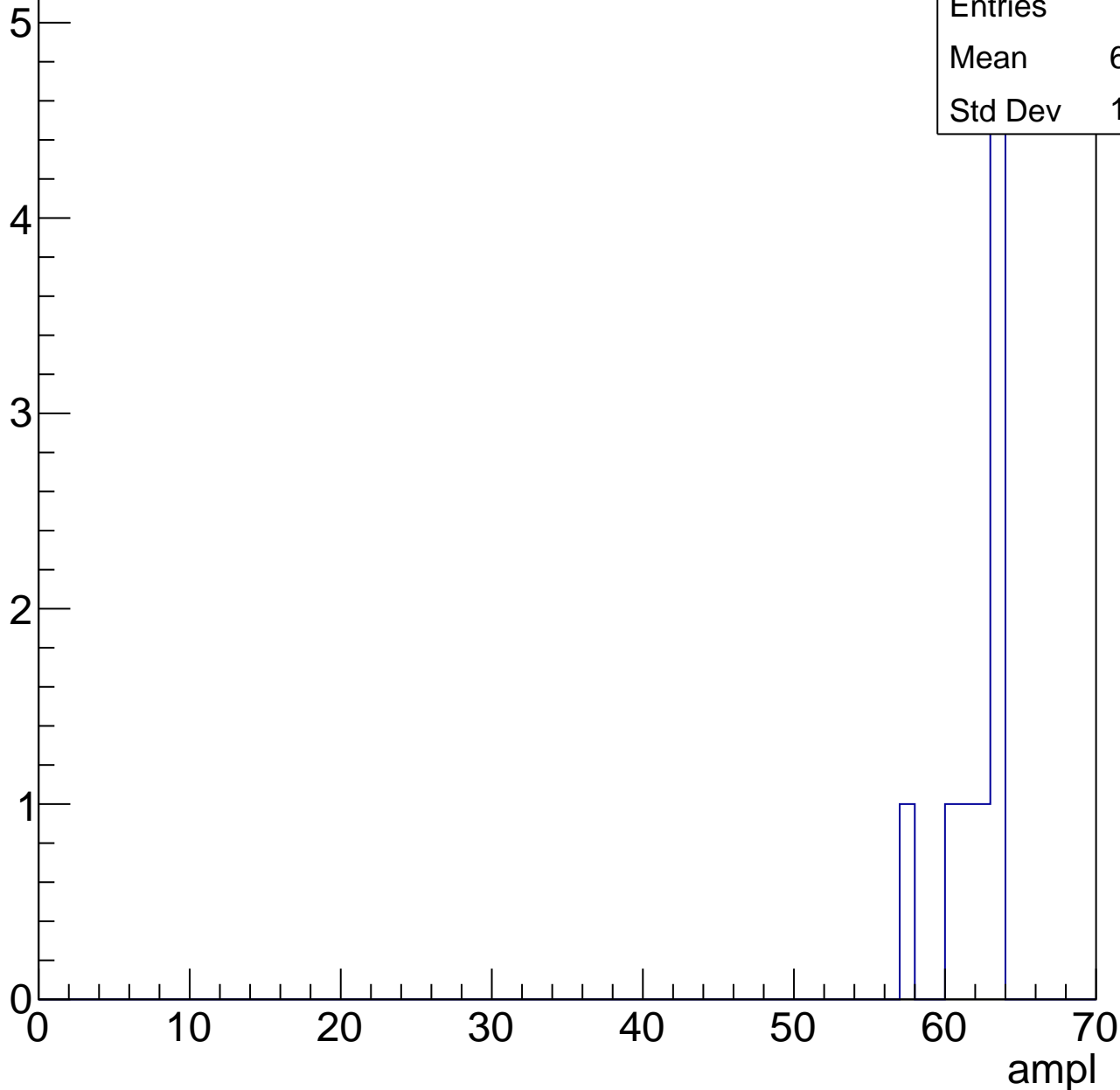


# B1L003S, U26-ch105, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	9
Mean	61.67
Std Dev	1.944

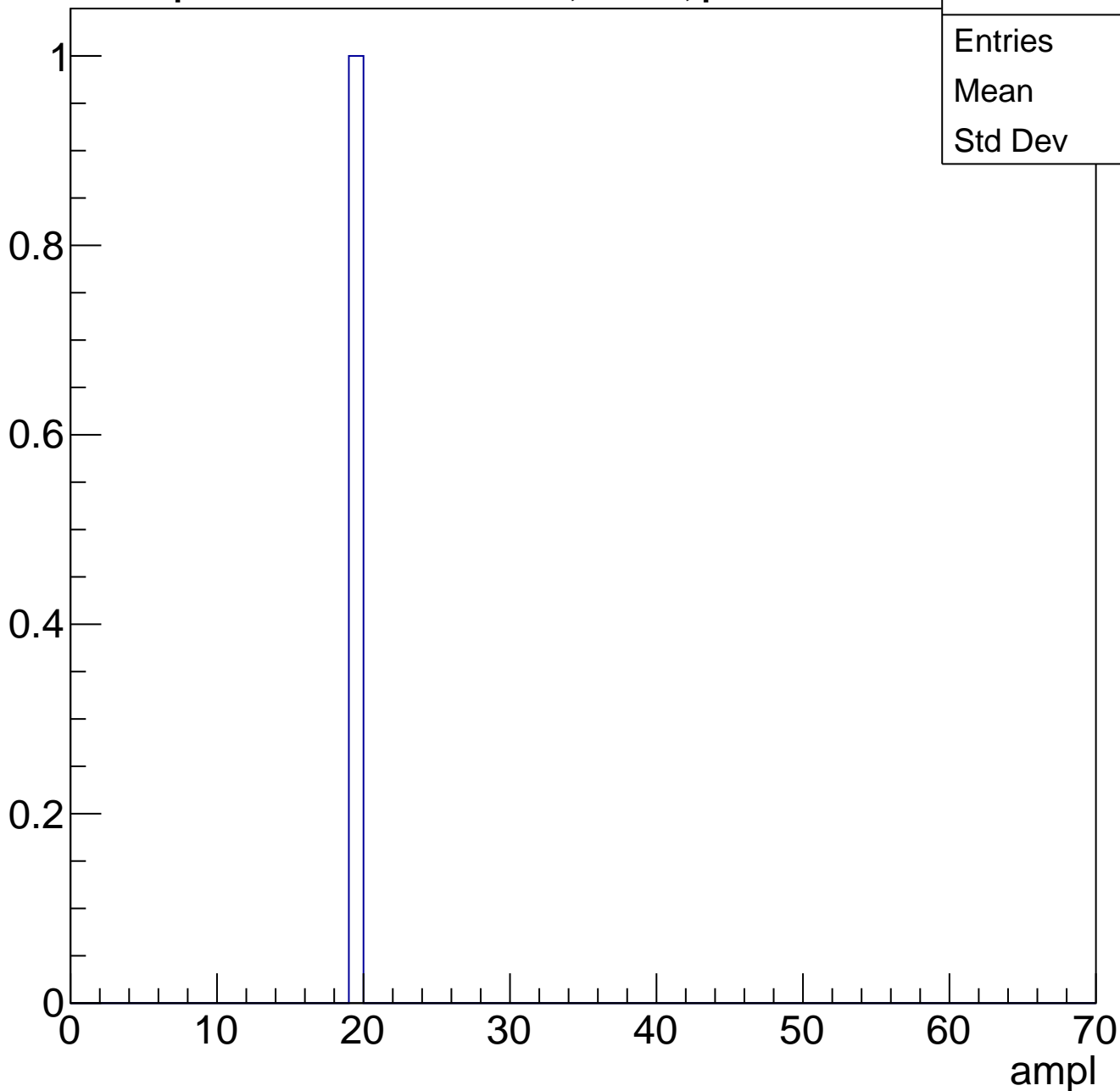




# B1L003S, U26-ch105, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U26-ch106, adc0

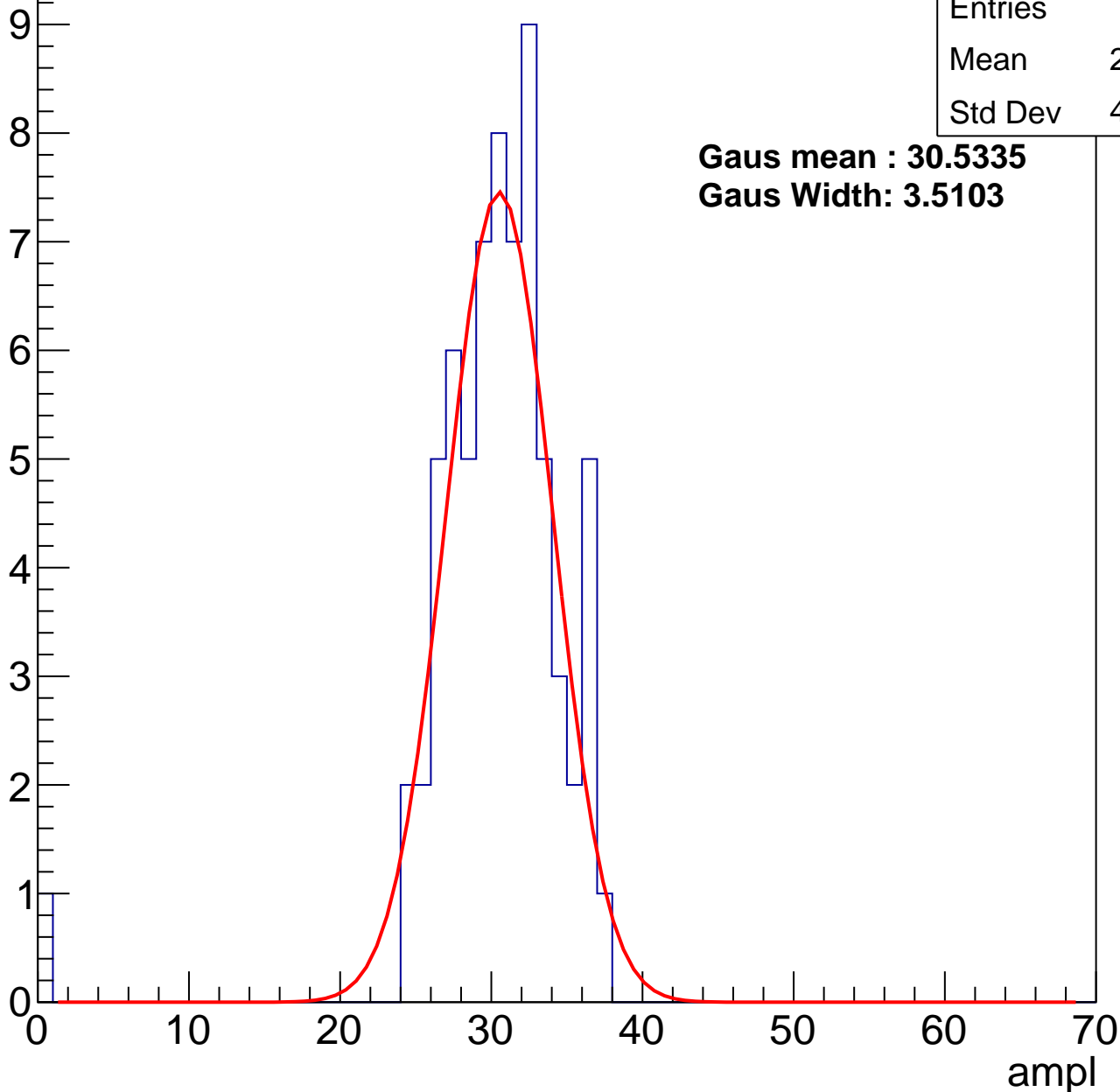
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	29.88
Std Dev	4.846

**Gaus mean : 30.5335**

**Gaus Width: 3.5103**



# B1L003S, U26-ch106, adc1

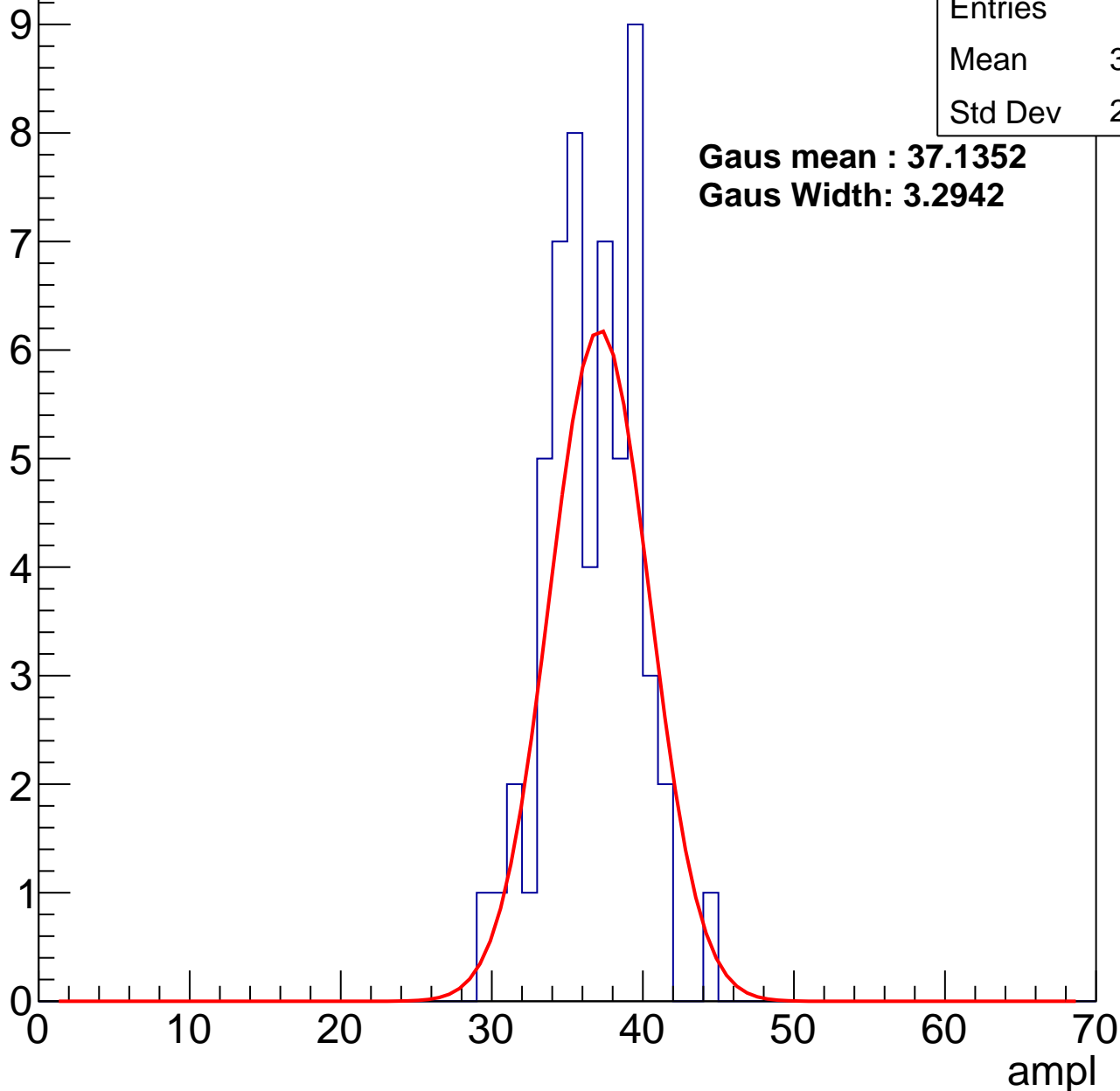
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	36.18
Std Dev	2.989

**Gaus mean : 37.1352**

**Gaus Width: 3.2942**



# B1L003S, U26-ch106, adc2

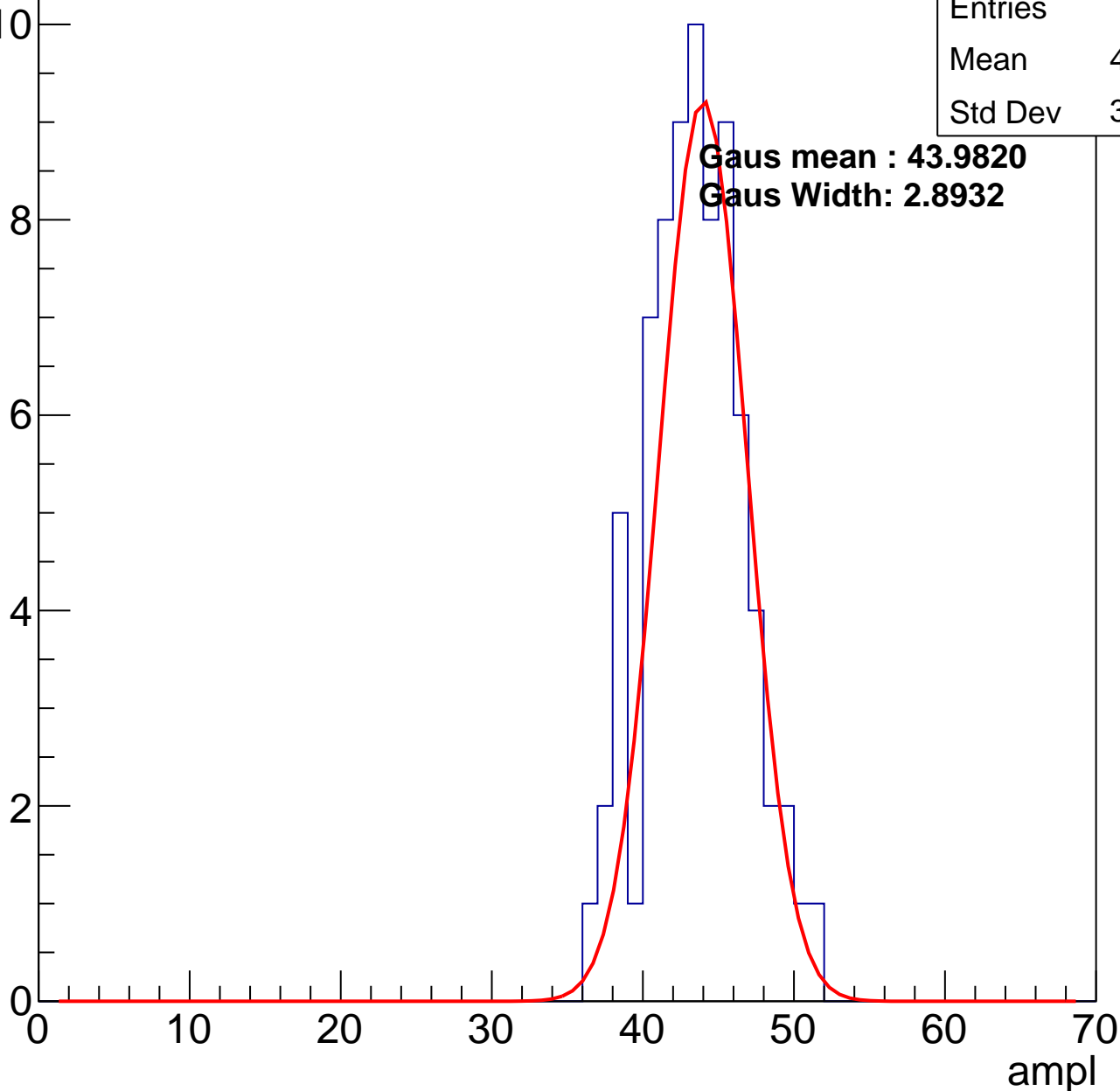
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	76
Mean	43.04
Std Dev	3.168

**Gaus mean : 43.9820**

**Gaus Width: 2.8932**

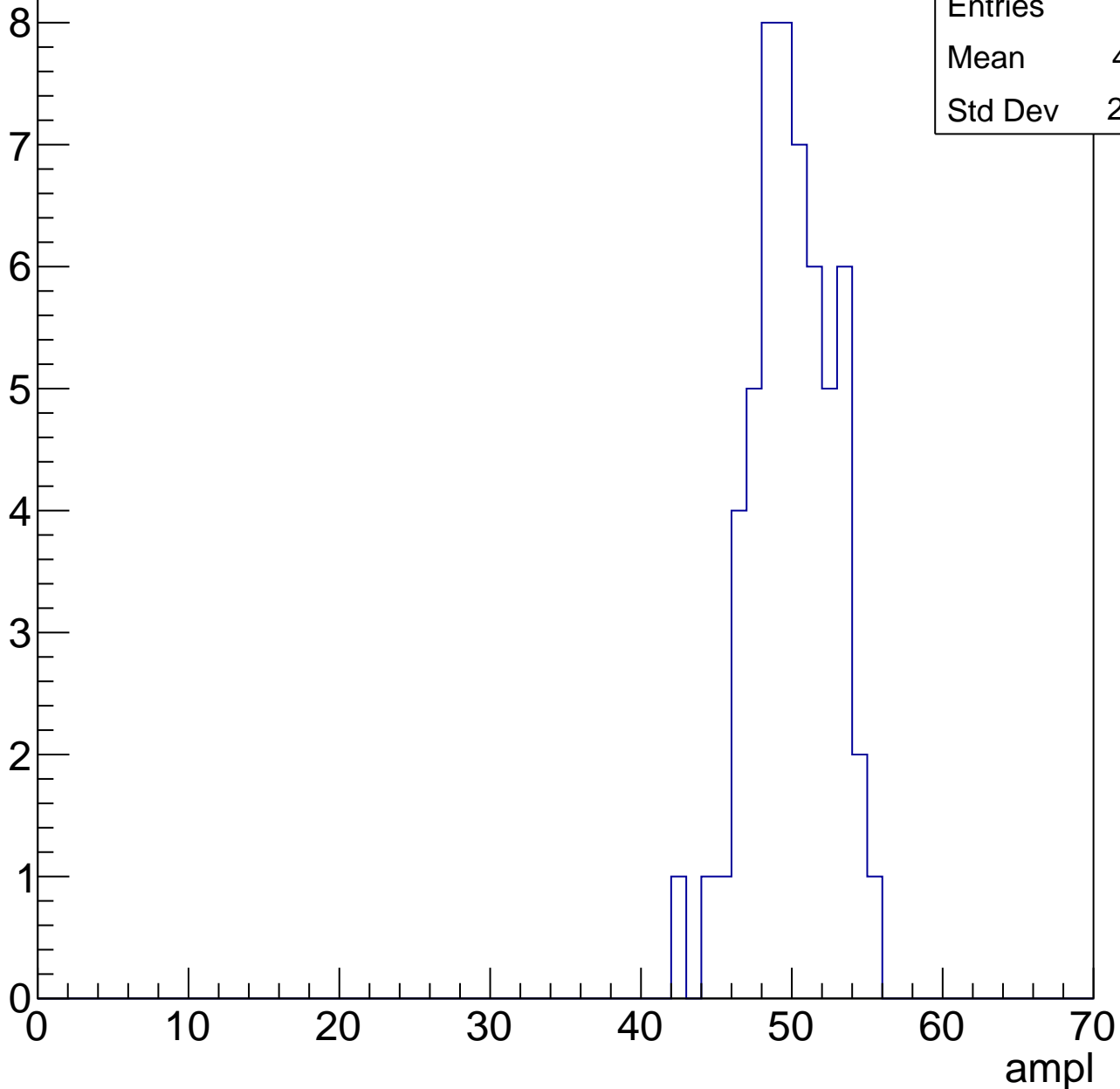


# B1L003S, U26-ch106, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	49.51
Std Dev	2.689

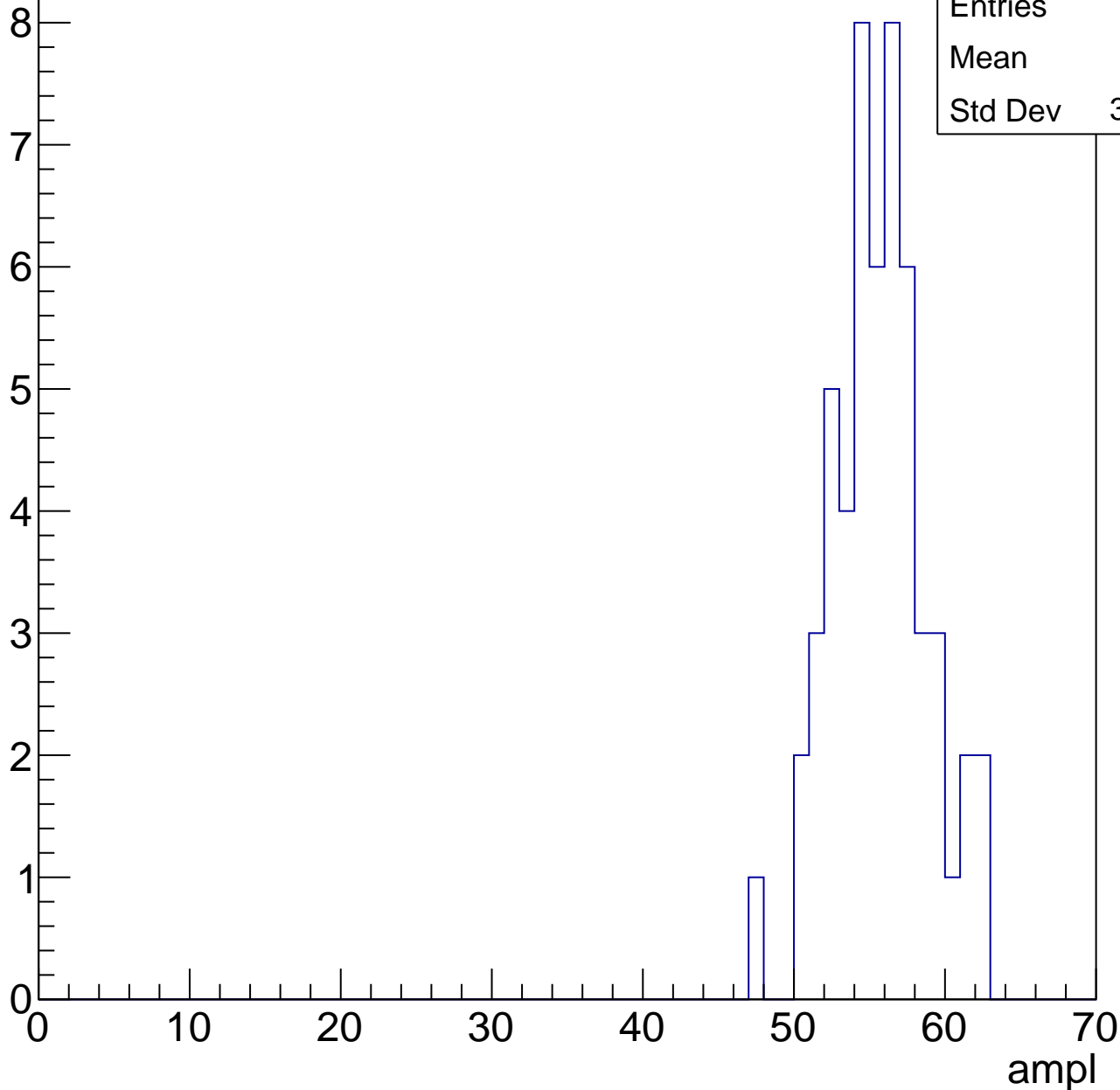


# B1L003S, U26-ch106, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	54
Mean	55.2
Std Dev	3.135

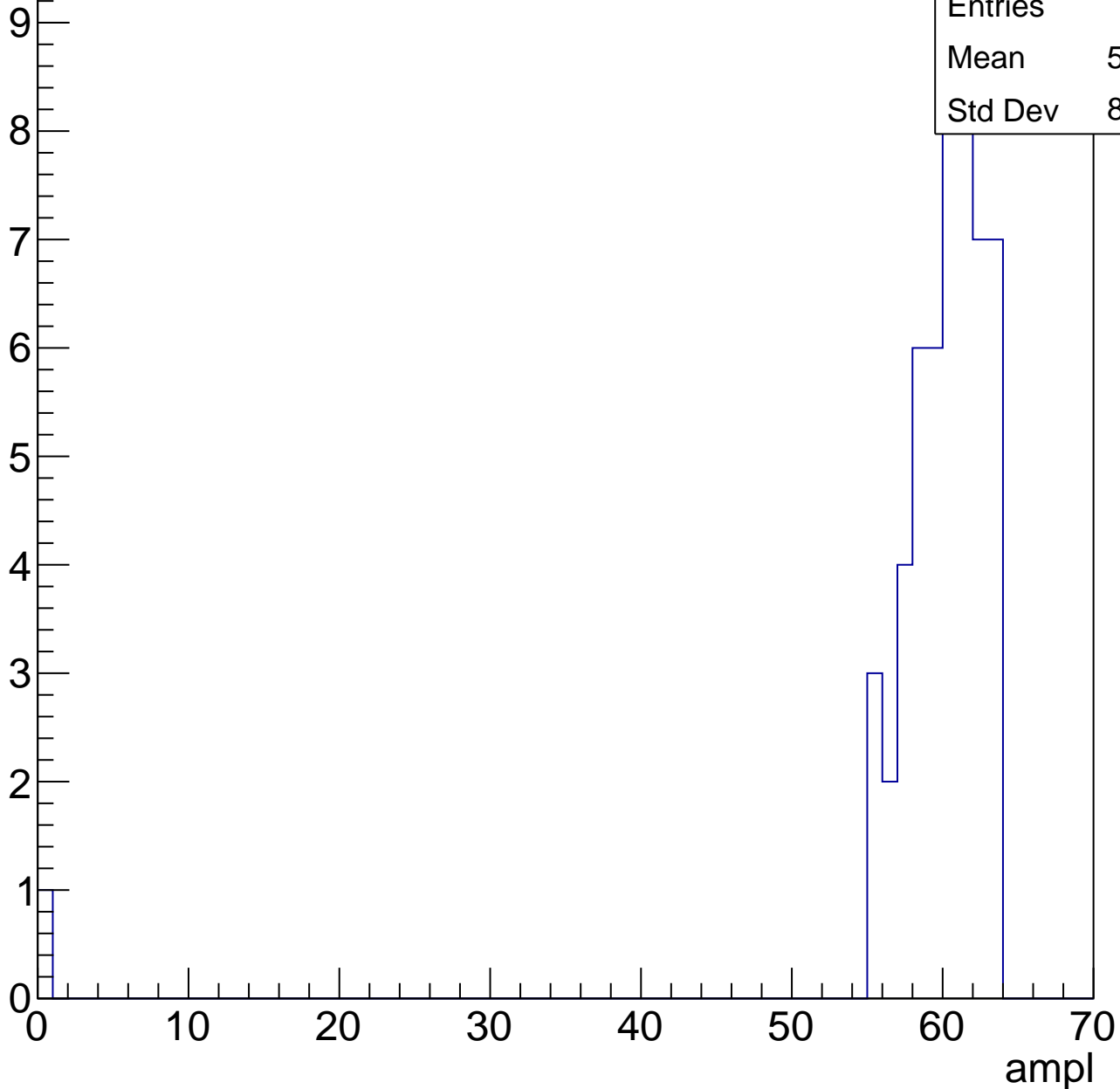


# B1L003S, U26-ch106, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

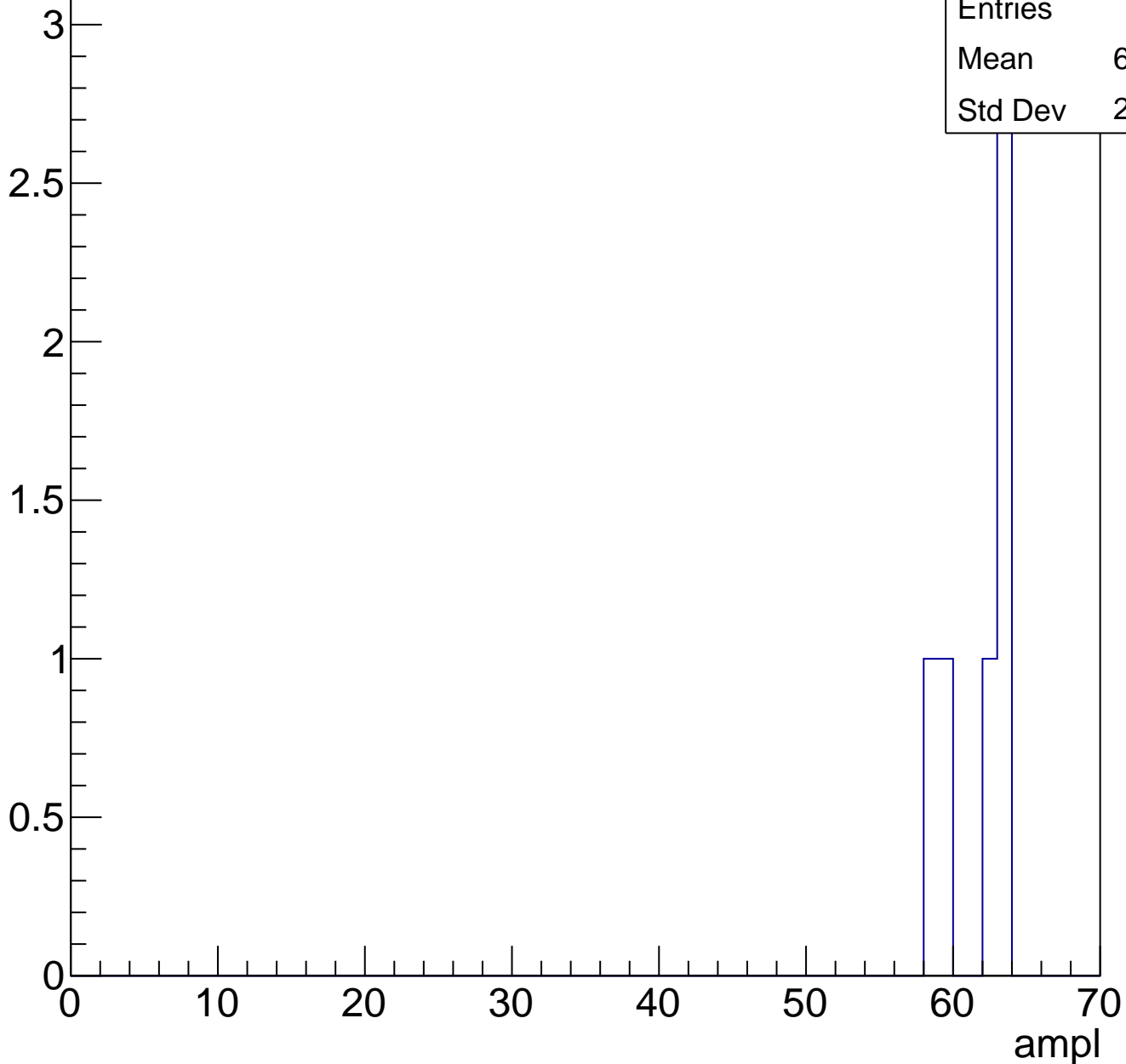
Entries	53
Mean	58.68
Std Dev	8.445



# B1L003S, U26-ch106, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch106, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U26-ch107, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	68
Mean	29.66
Std Dev	4.913

**Gaus mean : 30.5747**

**Gaus Width: 3.5961**

Entry

10  
8  
6  
4  
2  
0

ampl

0

10

20

30

40

50

60

70

# B1L003S, U26-ch107, adc1

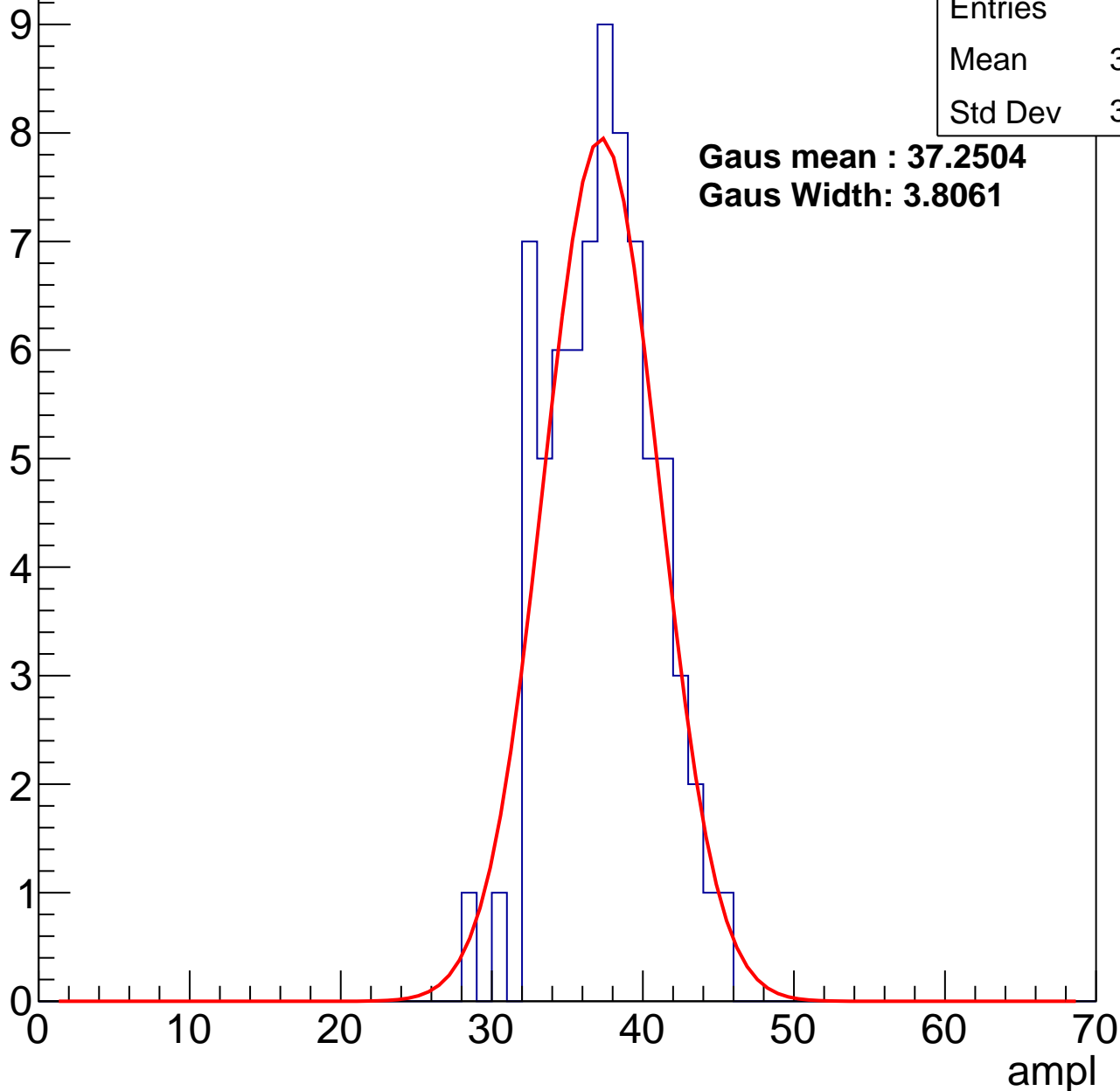
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	74
Mean	36.88
Std Dev	3.468

**Gaus mean : 37.2504**

**Gaus Width: 3.8061**



# B1L003S, U26-ch107, adc2

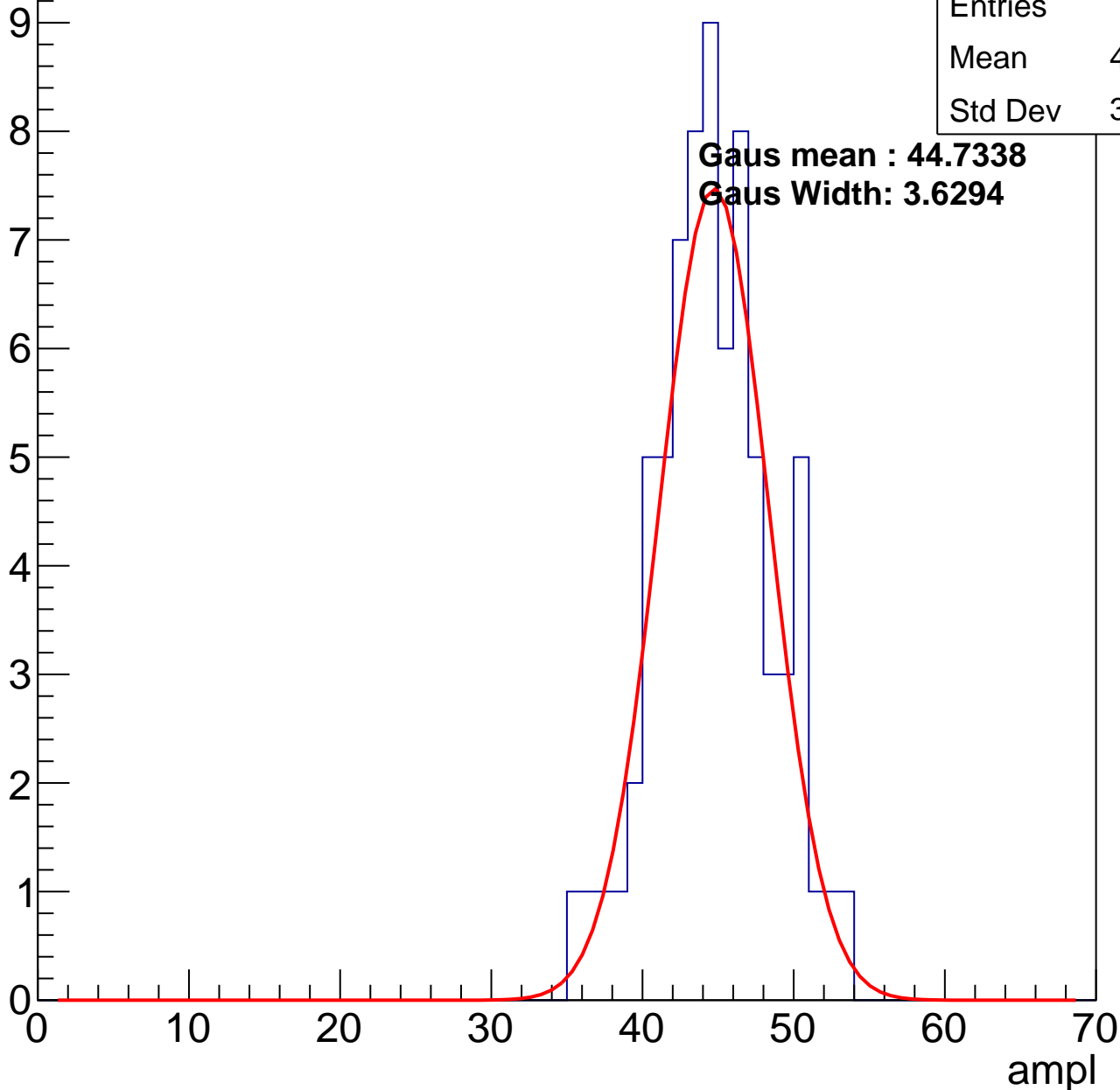
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	73
Mean	44.29
Std Dev	3.729

**Gaus mean : 44.7338**

**Gaus Width: 3.6294**

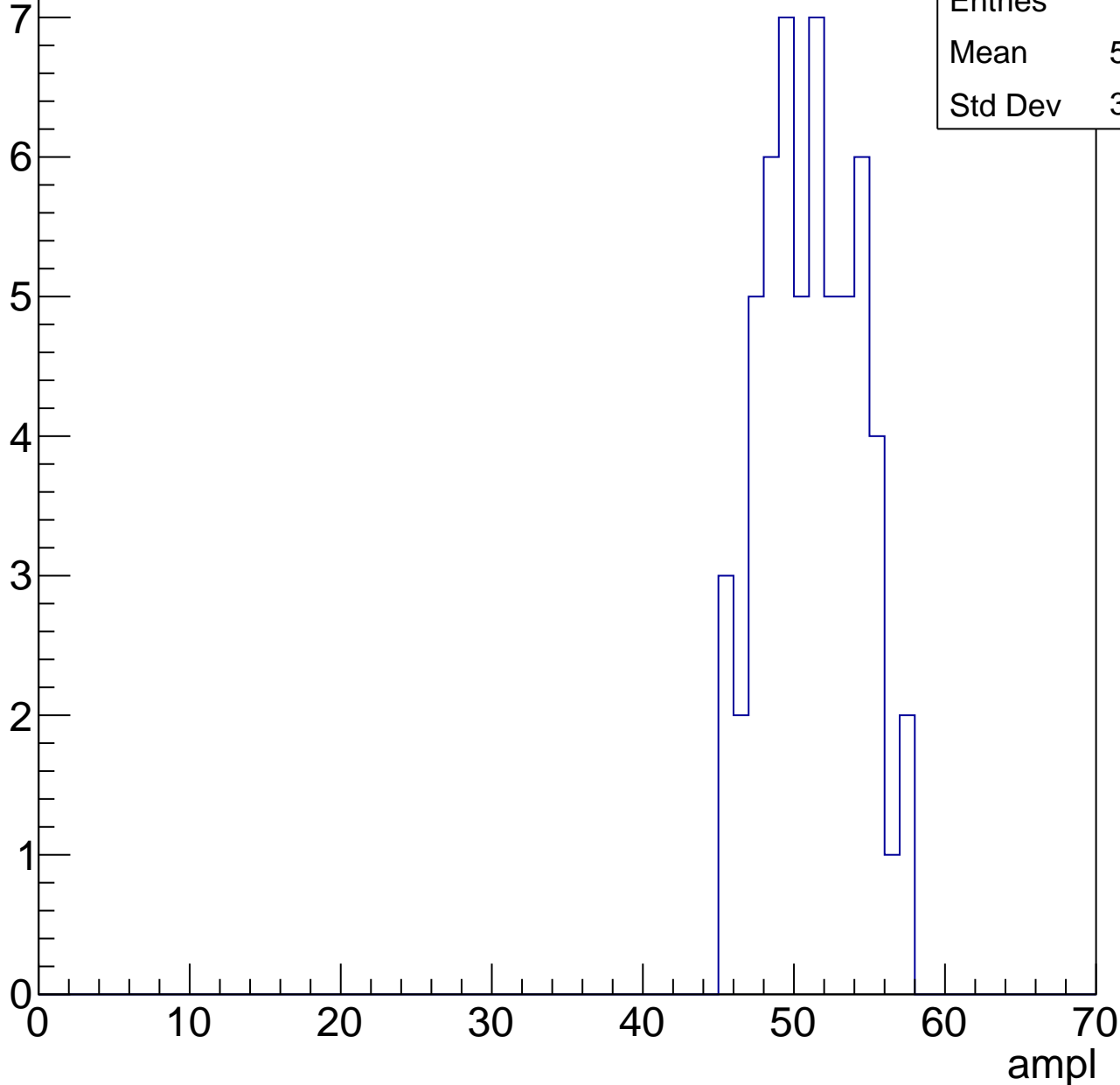


# B1L003S, U26-ch107, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	50.67
Std Dev	3.104

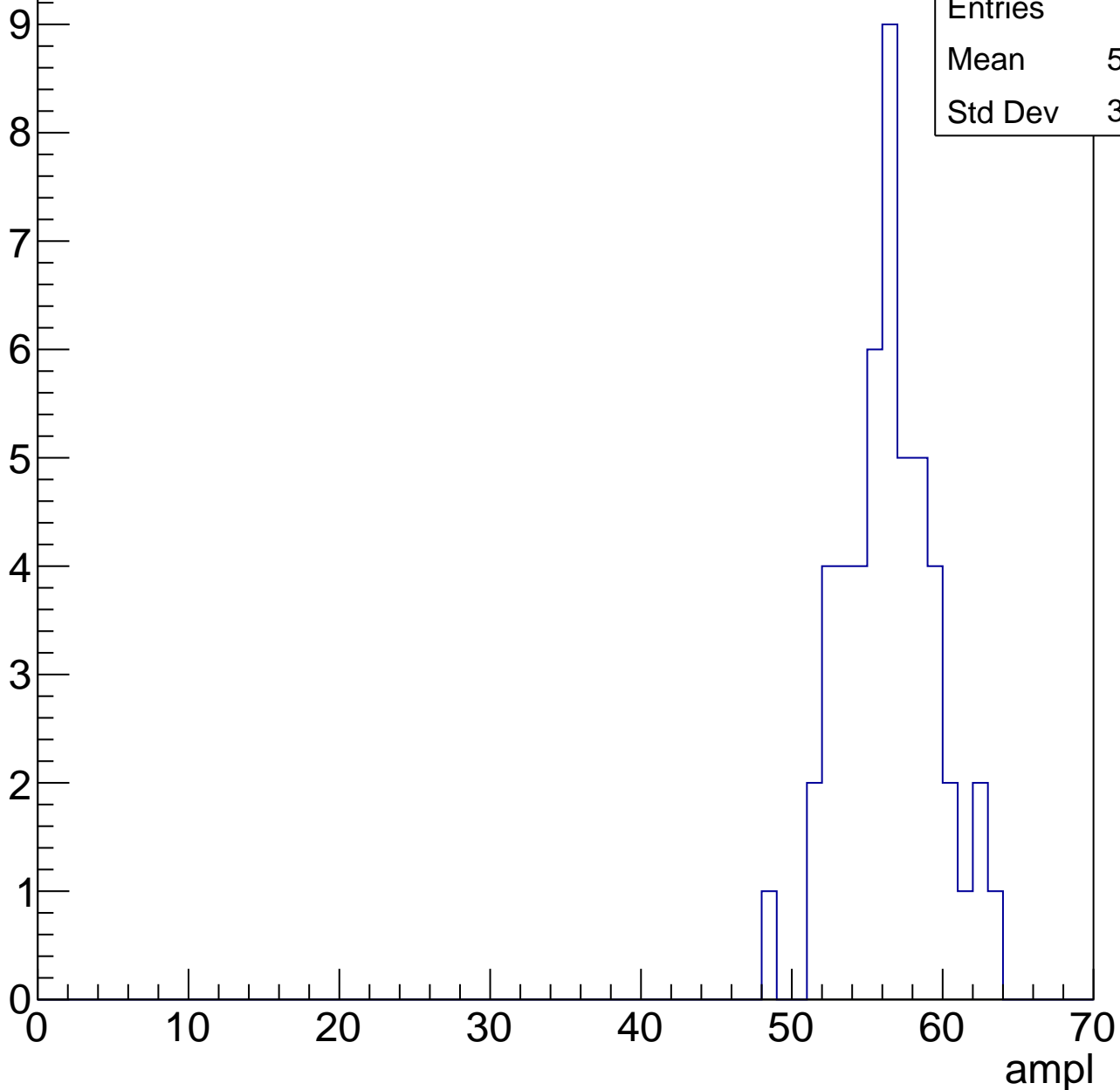


# B1L003S, U26-ch107, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	50
Mean	55.98
Std Dev	3.082

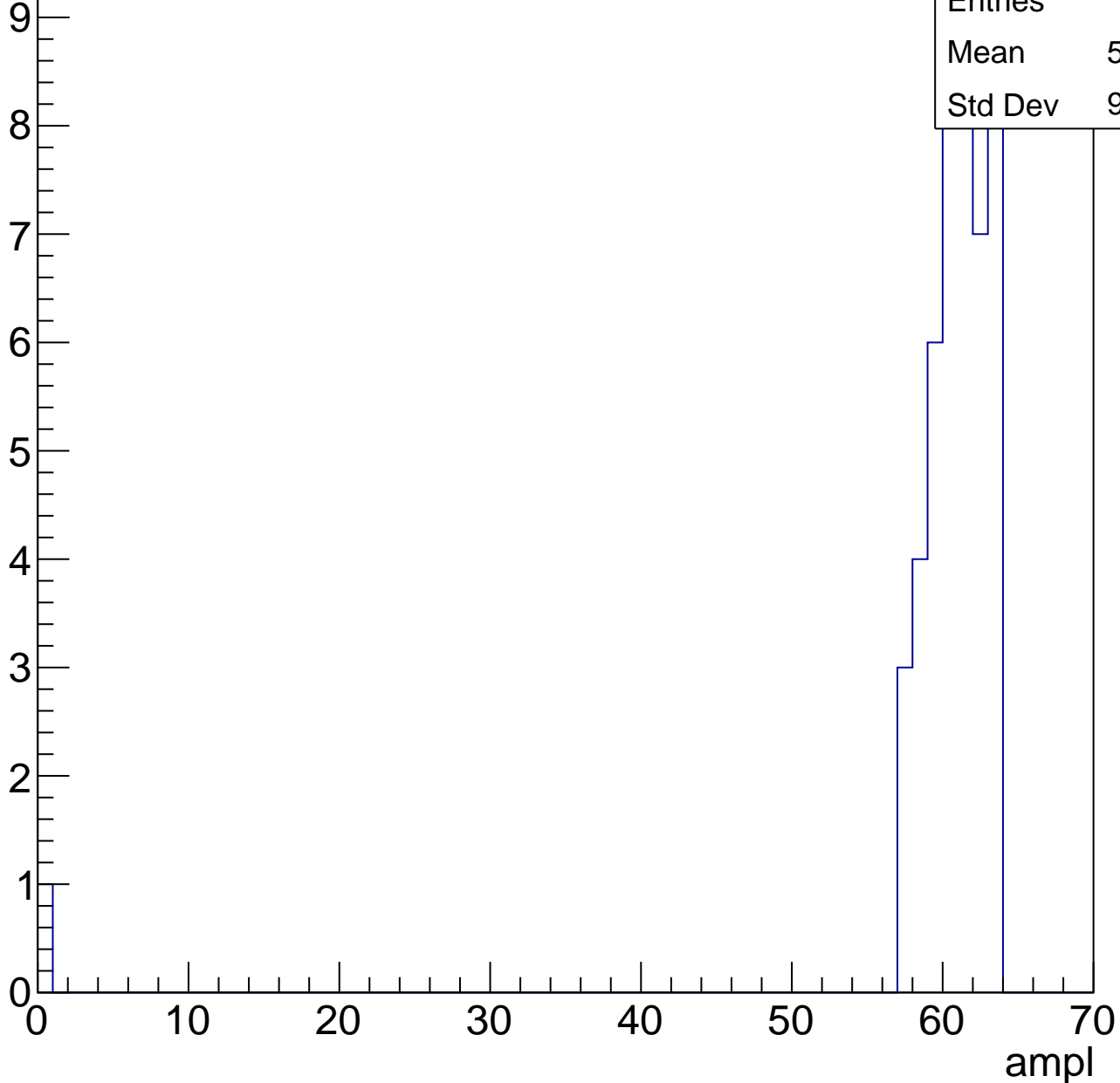


# B1L003S, U26-ch107, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

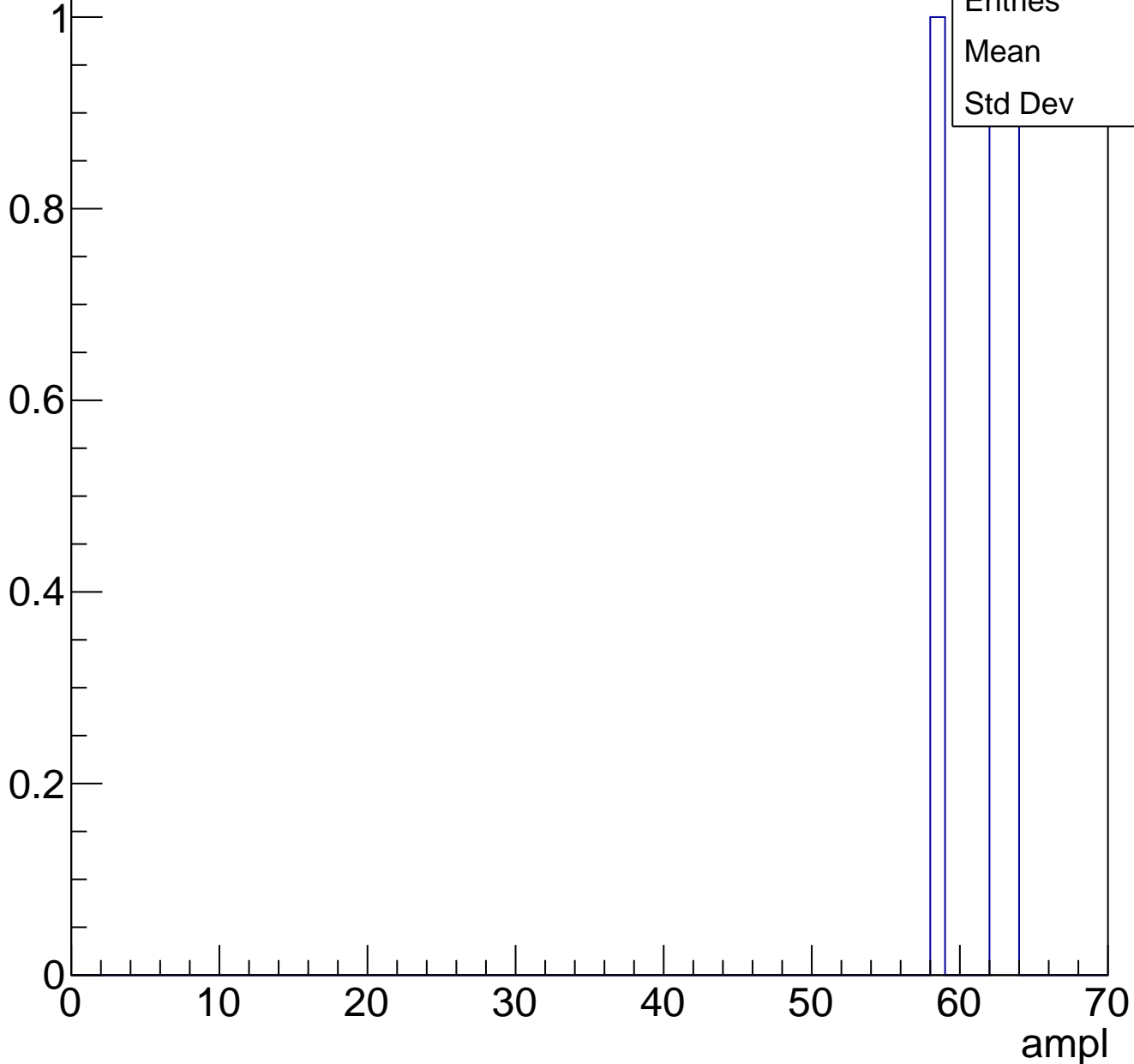
Entries	46
Mean	59.22
Std Dev	9.005



# B1L003S, U26-ch107, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch107, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U26-ch108, adc0

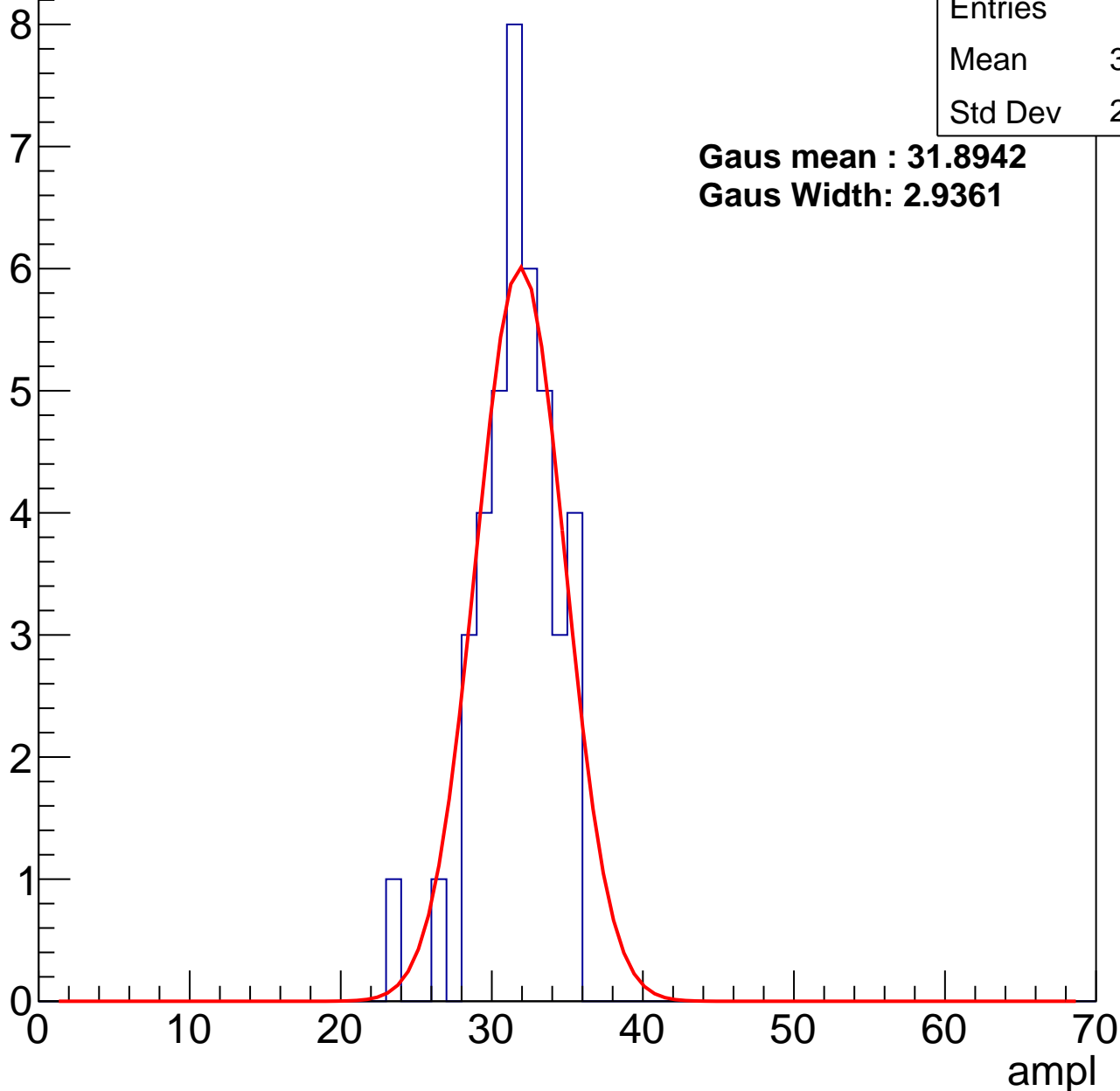
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	40
Mean	31.15
Std Dev	2.515

**Gaus mean : 31.8942**

**Gaus Width: 2.9361**



# B1L003S, U26-ch108, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	69
Mean	36.58
Std Dev	2.831

**Gaus mean : 37.1958**

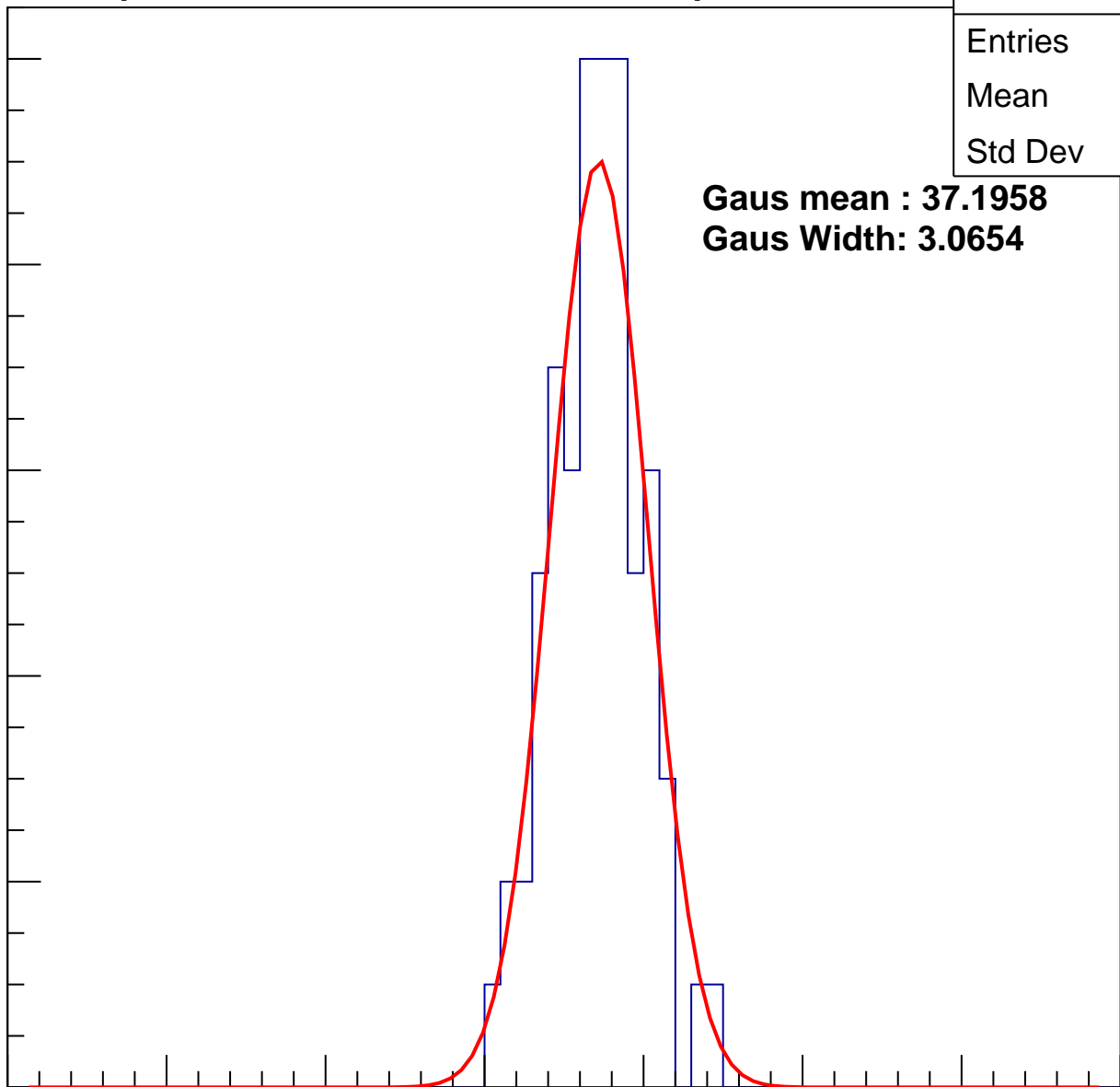
**Gaus Width: 3.0654**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L003S, U26-ch108, adc2

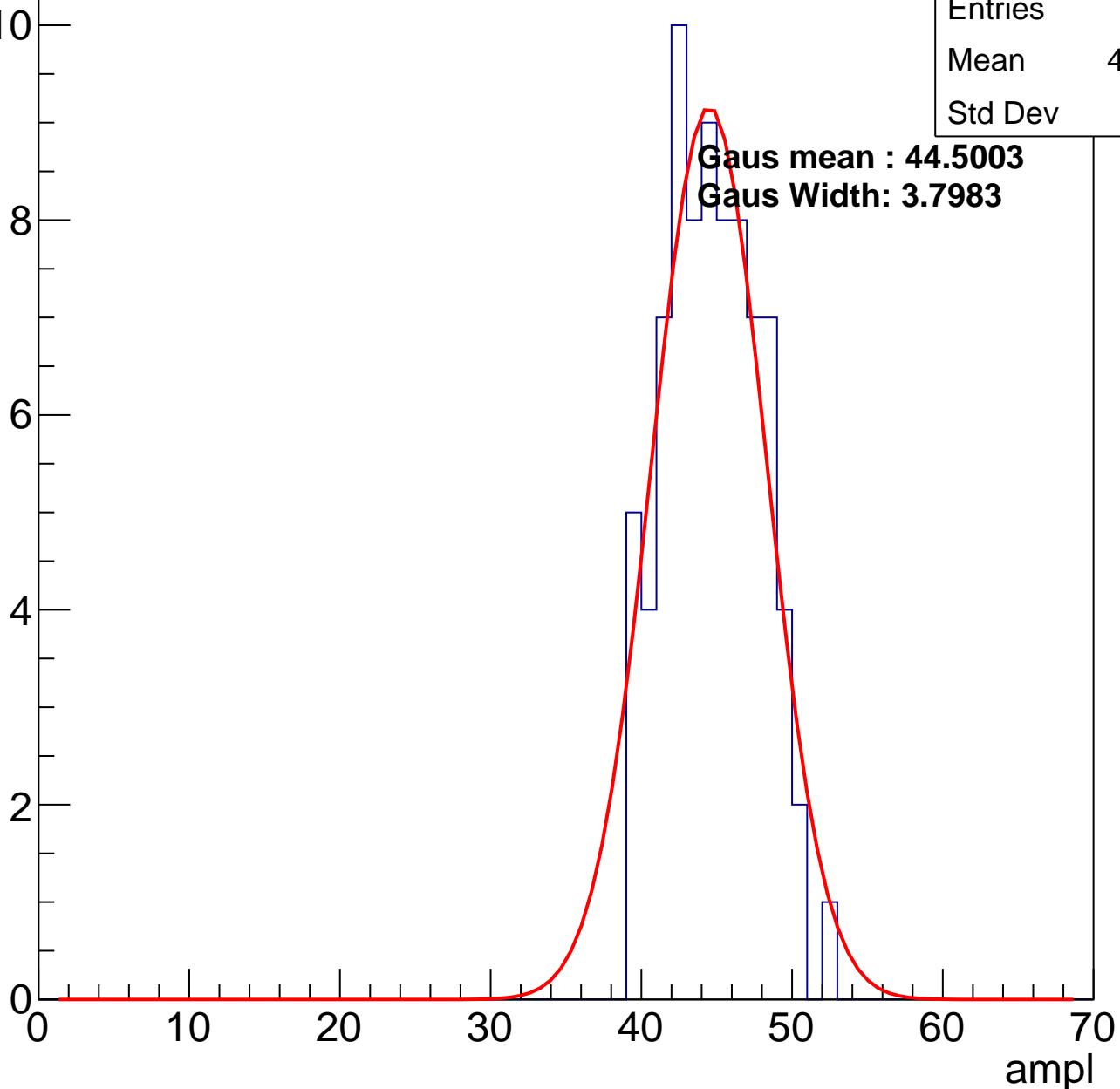
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	80
Mean	44.29
Std Dev	3.05

**Gaus mean : 44.5003**

**Gaus Width: 3.7983**

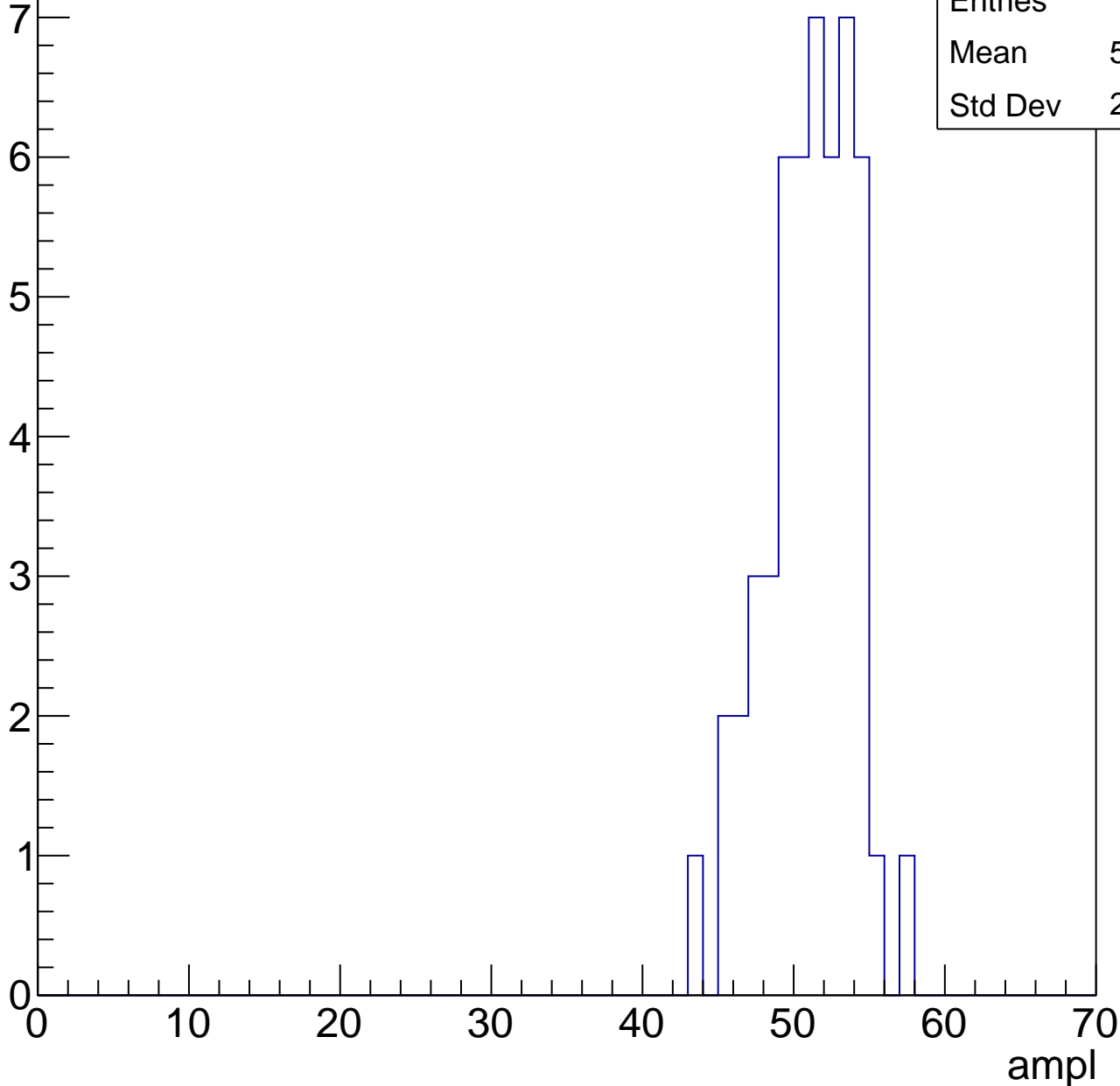


# B1L003S, U26-ch108, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

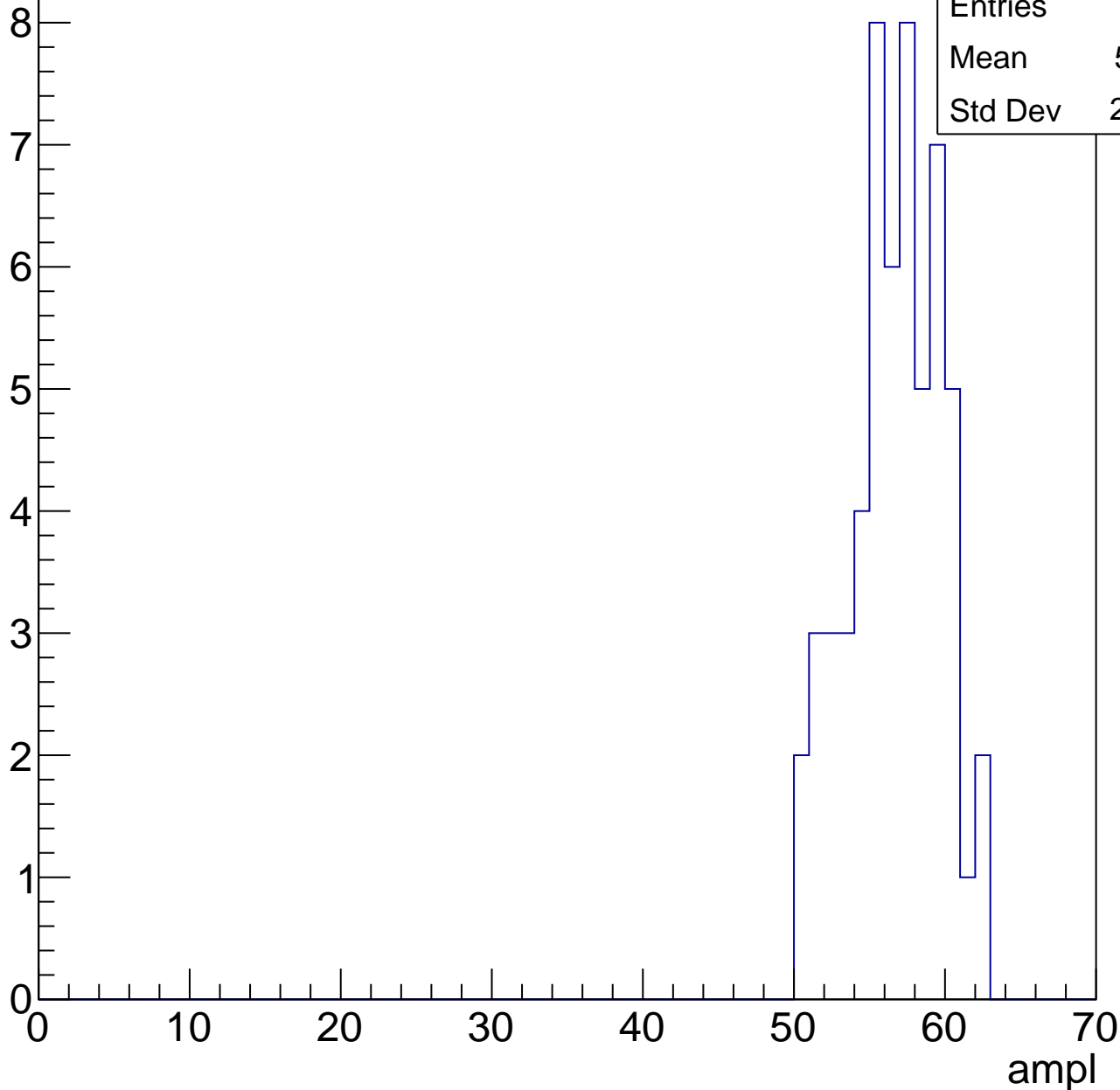
Entries	51
Mean	50.59
Std Dev	2.878



# B1L003S, U26-ch108, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



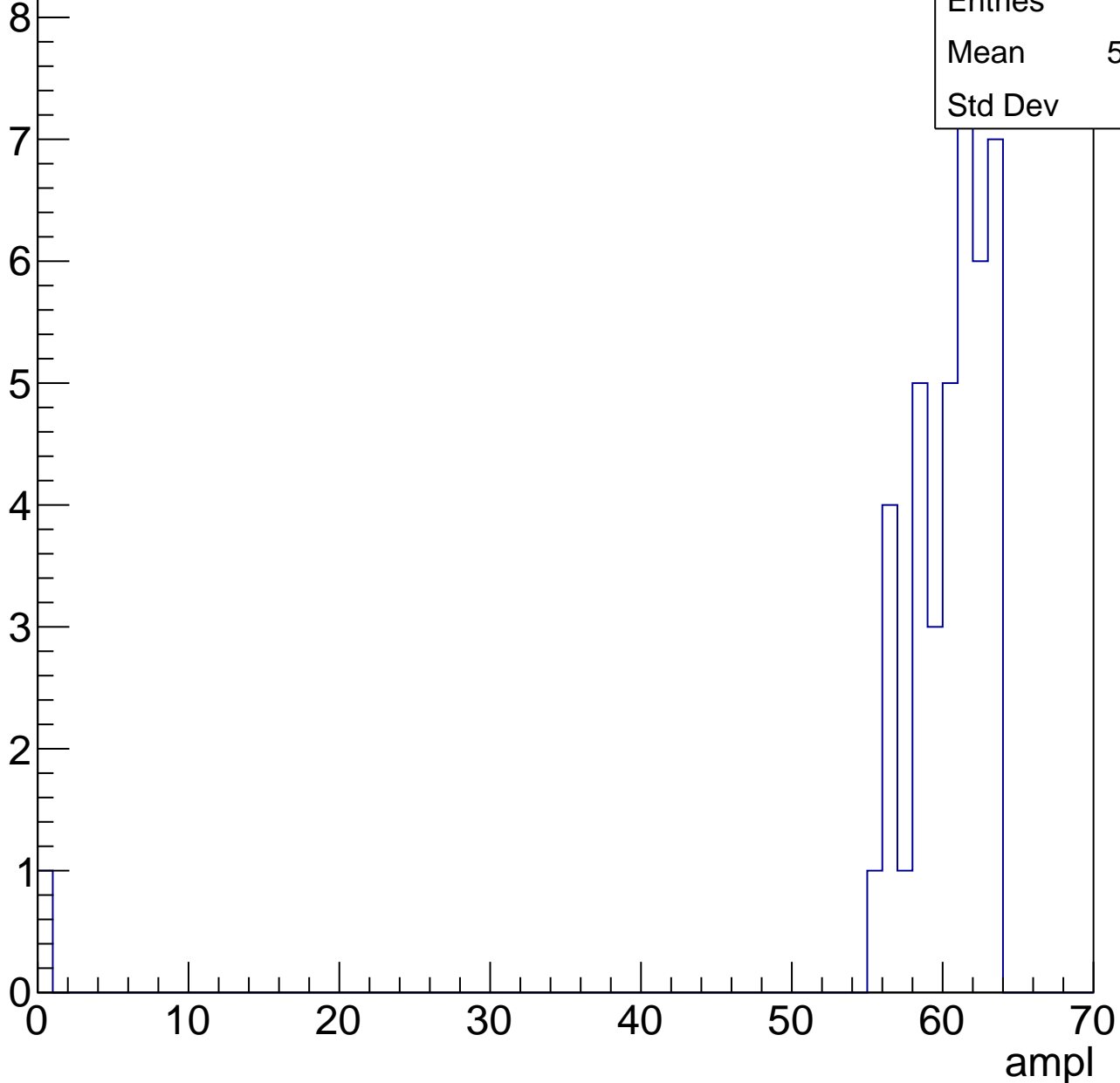
Entries	57
Mean	56.21
Std Dev	2.996

# B1L003S, U26-ch108, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	41
Mean	58.63
Std Dev	9.55



# B1L003S, U26-ch108, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch108, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U26-ch109, adc0

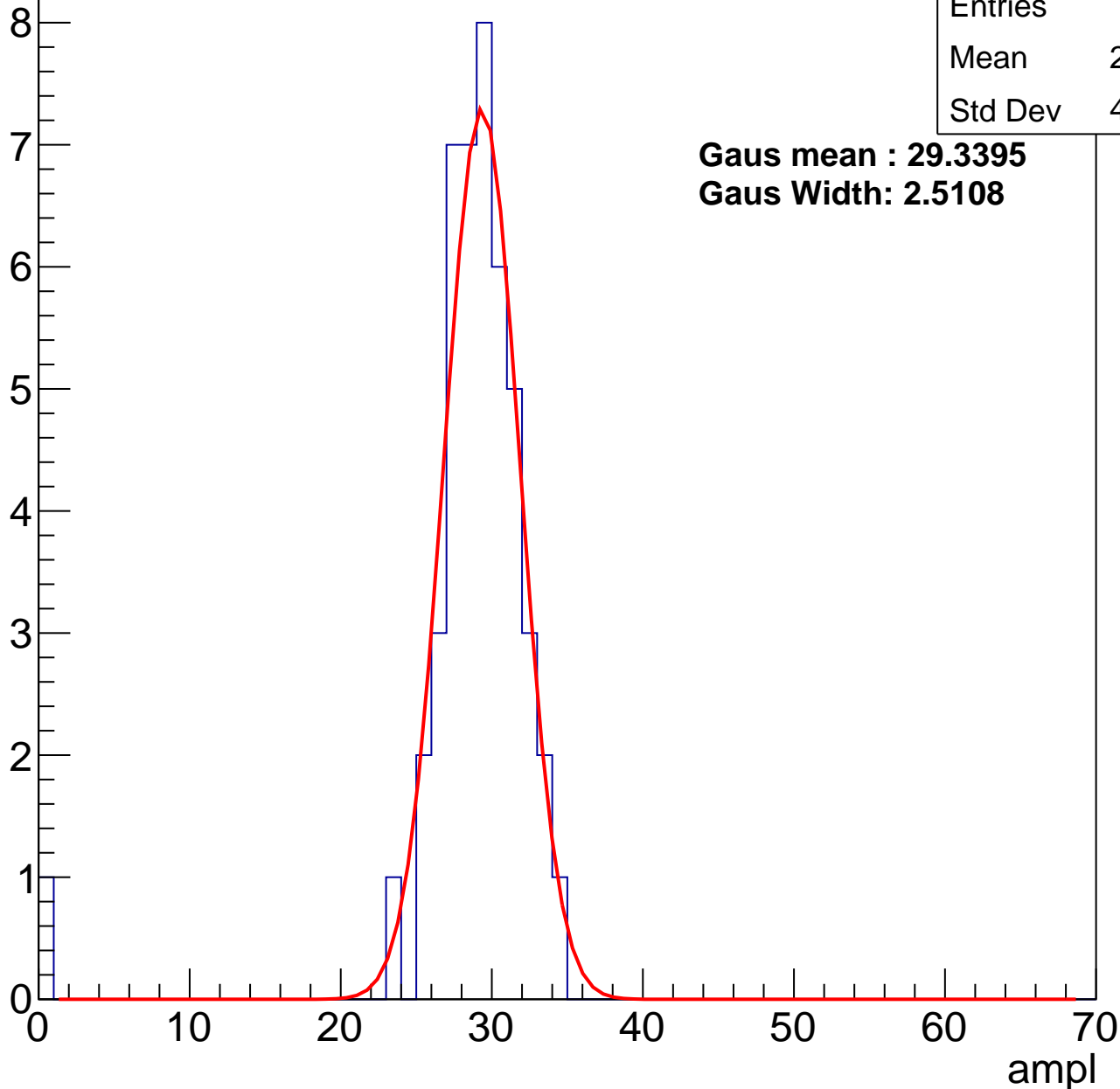
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	46
Mean	28.24
Std Dev	4.788

**Gaus mean : 29.3395**

**Gaus Width: 2.5108**



# B1L003S, U26-ch109, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	90
Mean	35.51
Std Dev	3.658

**Gaus mean : 35.6071**

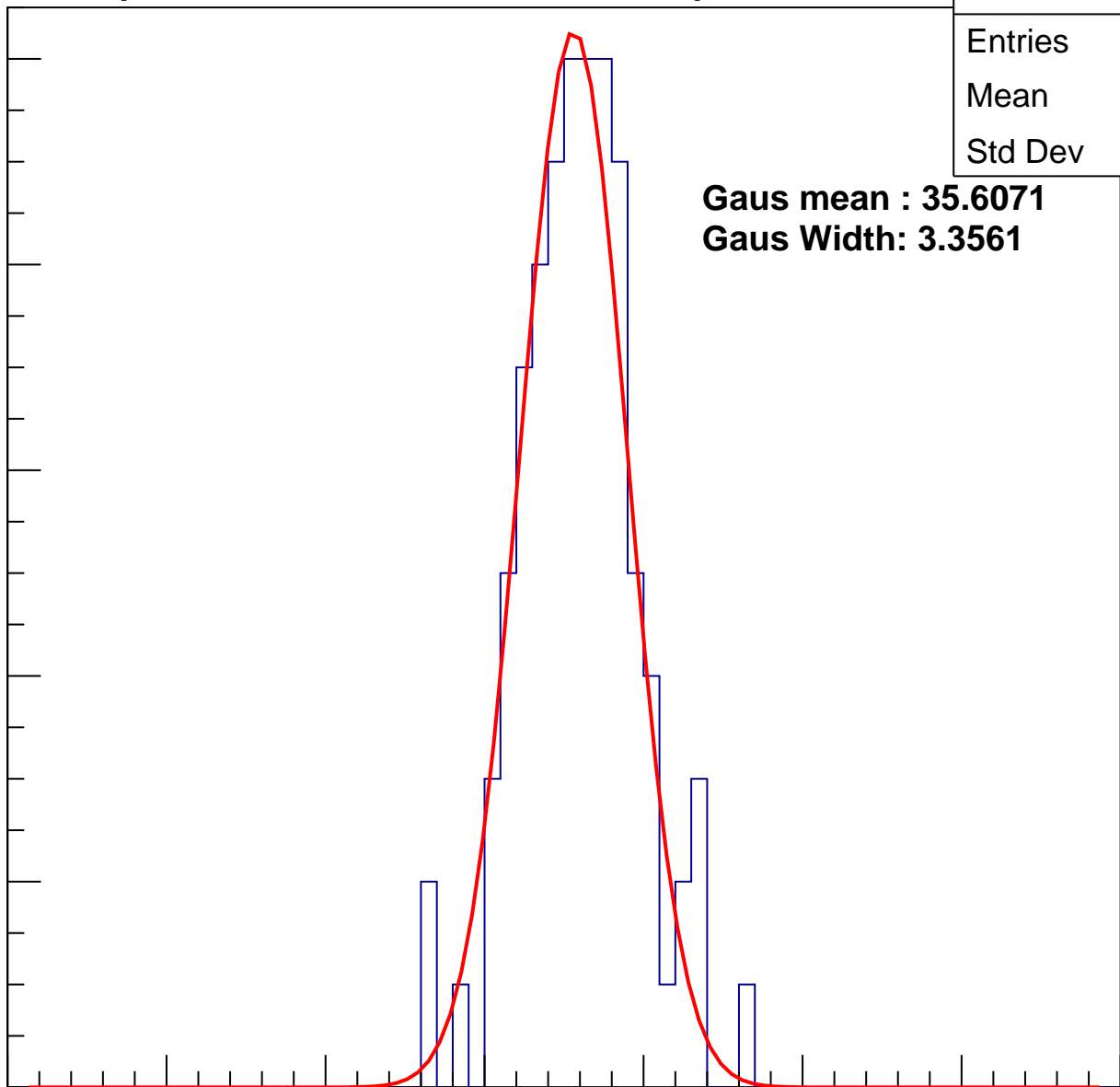
**Gaus Width: 3.3561**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U26-ch109, adc2

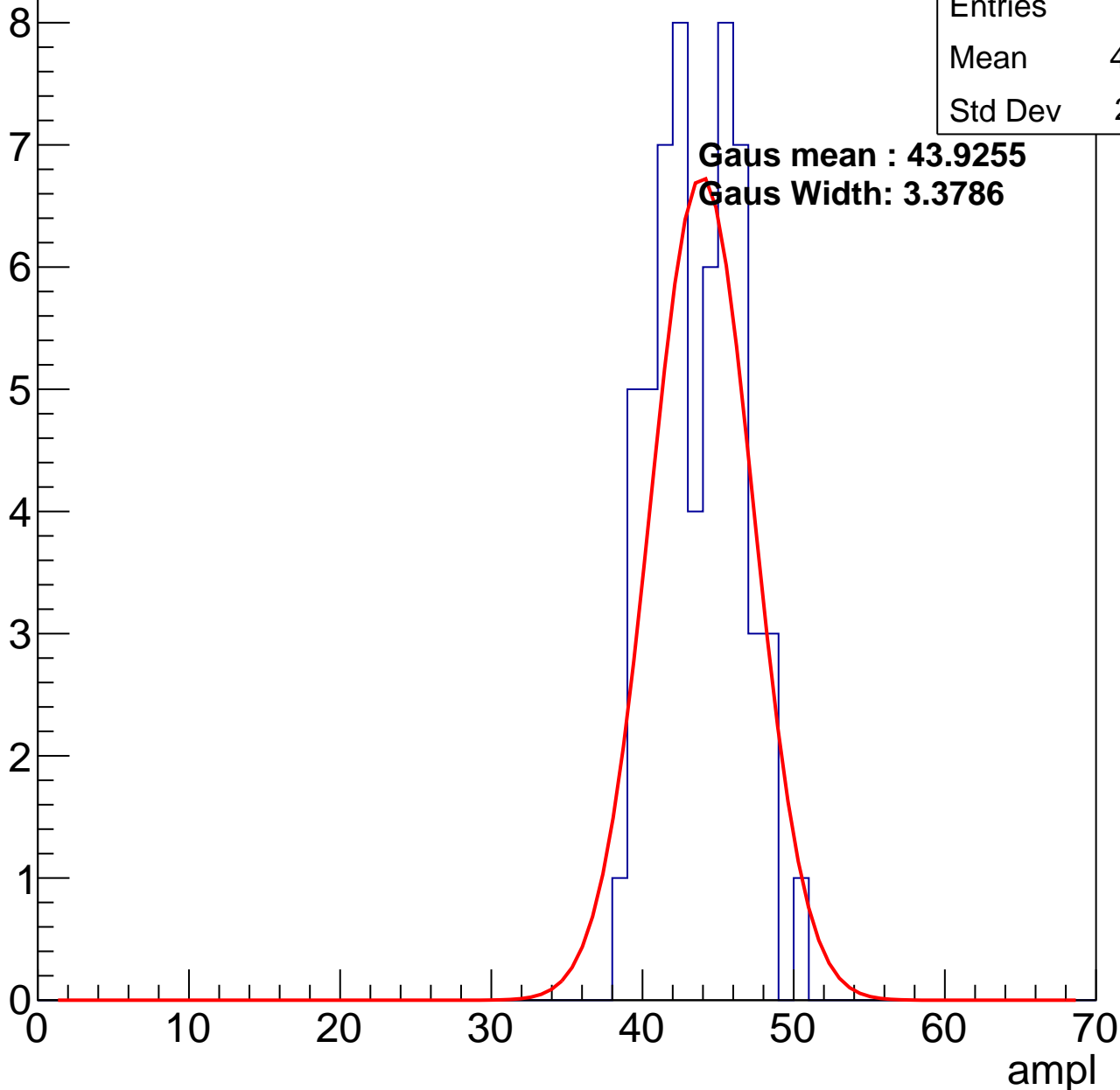
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	43.26
Std Dev	2.801

**Gaus mean : 43.9255**

**Gaus Width: 3.3786**

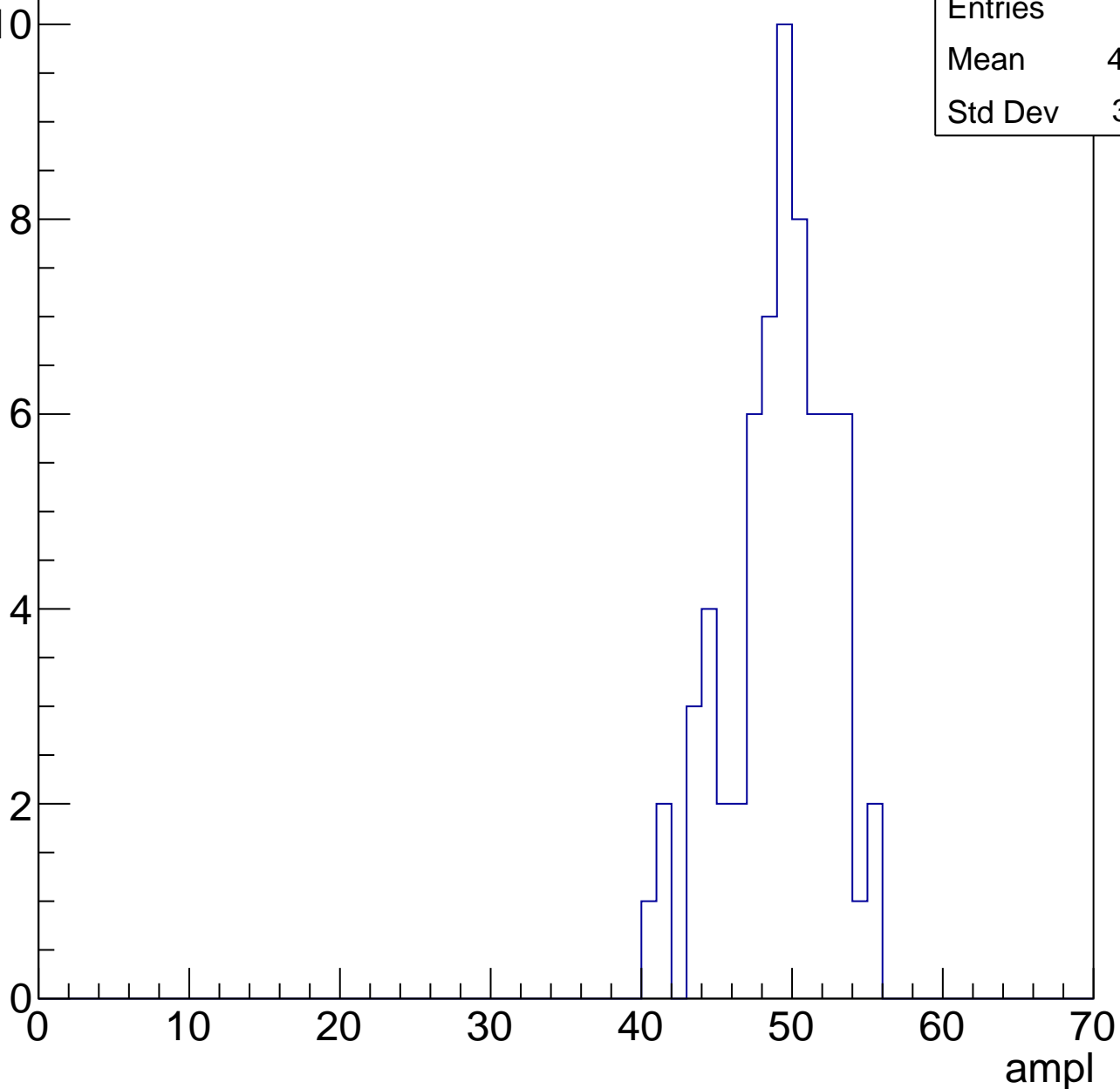


# B1L003S, U26-ch109, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	48.74
Std Dev	3.421

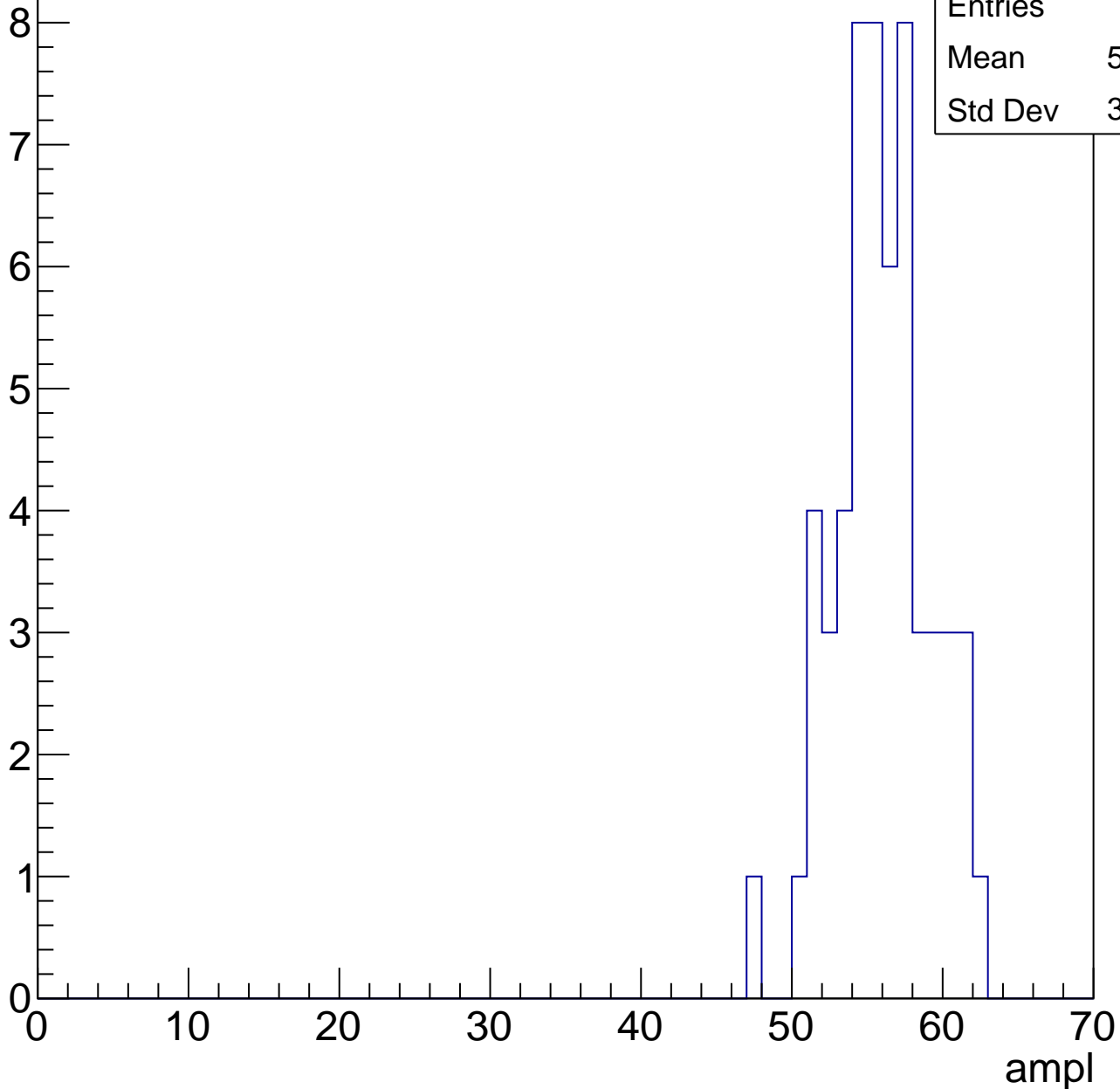


# B1L003S, U26-ch109, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	55.52
Std Dev	3.088

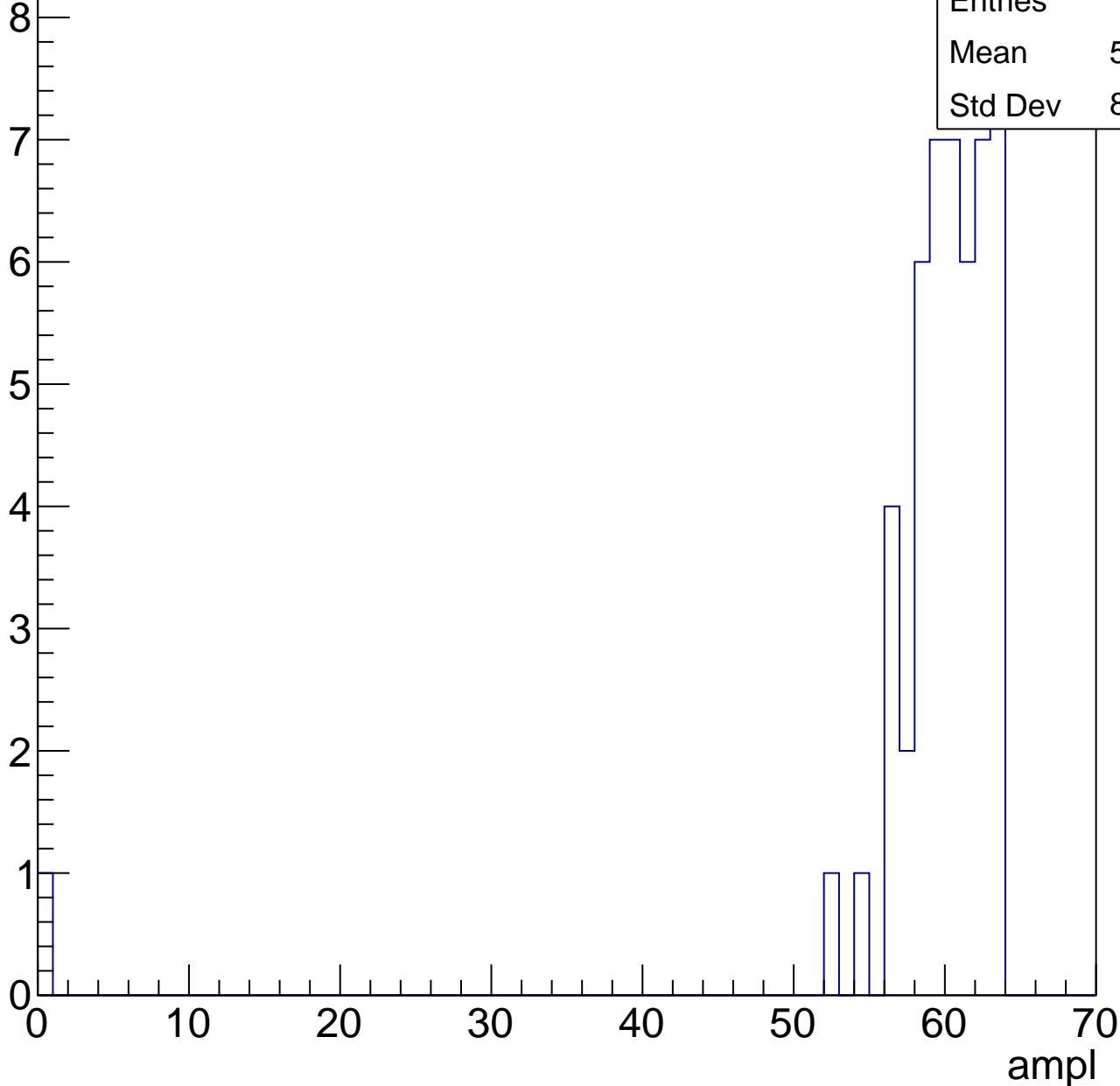


# B1L003S, U26-ch109, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	50
Mean	58.58
Std Dev	8.739



# B1L003S, U26-ch109, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

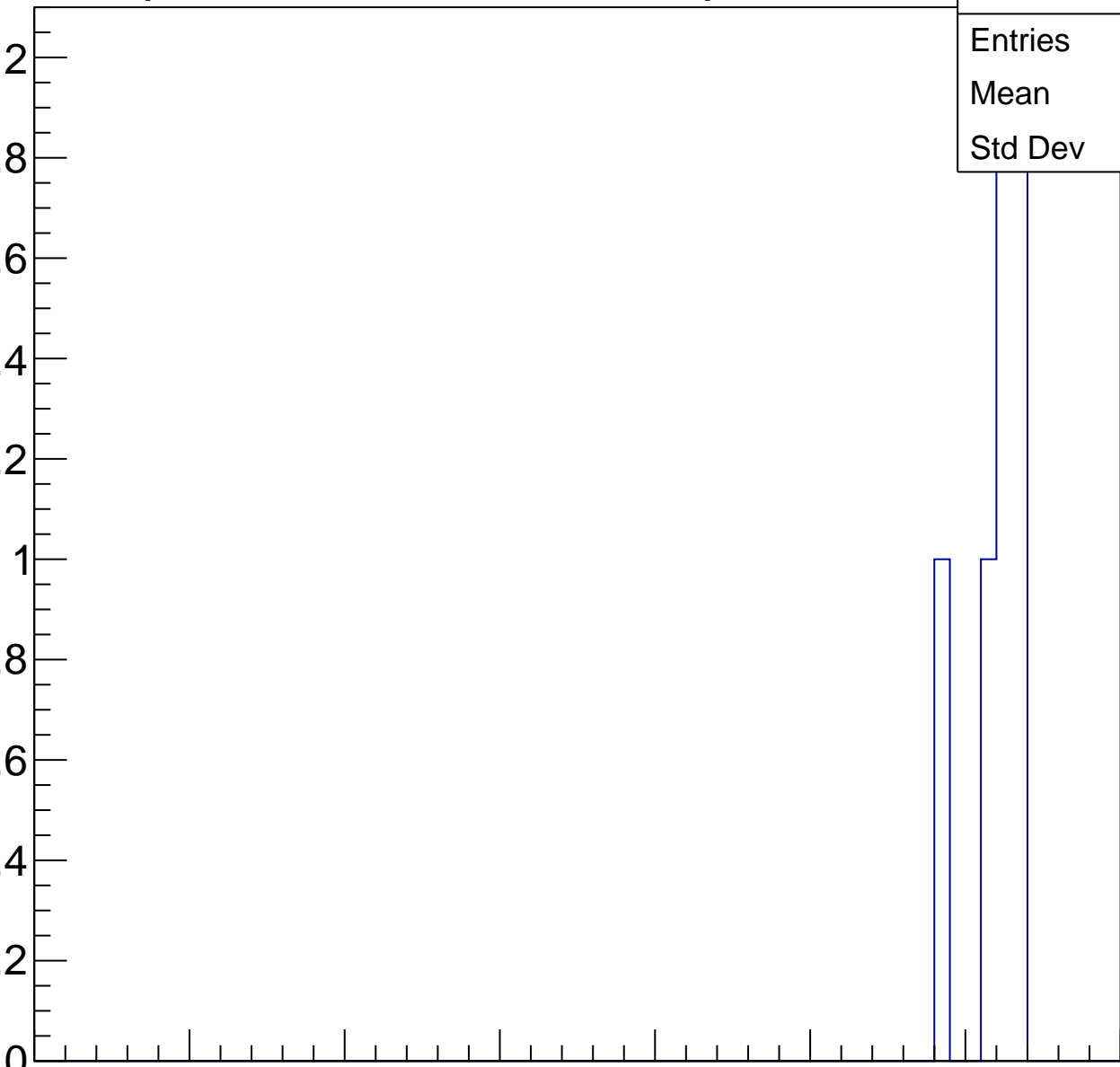
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	61.5
Std Dev	1.708

0 10 20 30 40 50 60 70

ampl





# B1L003S, U26-ch109, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U26-ch110, adc0

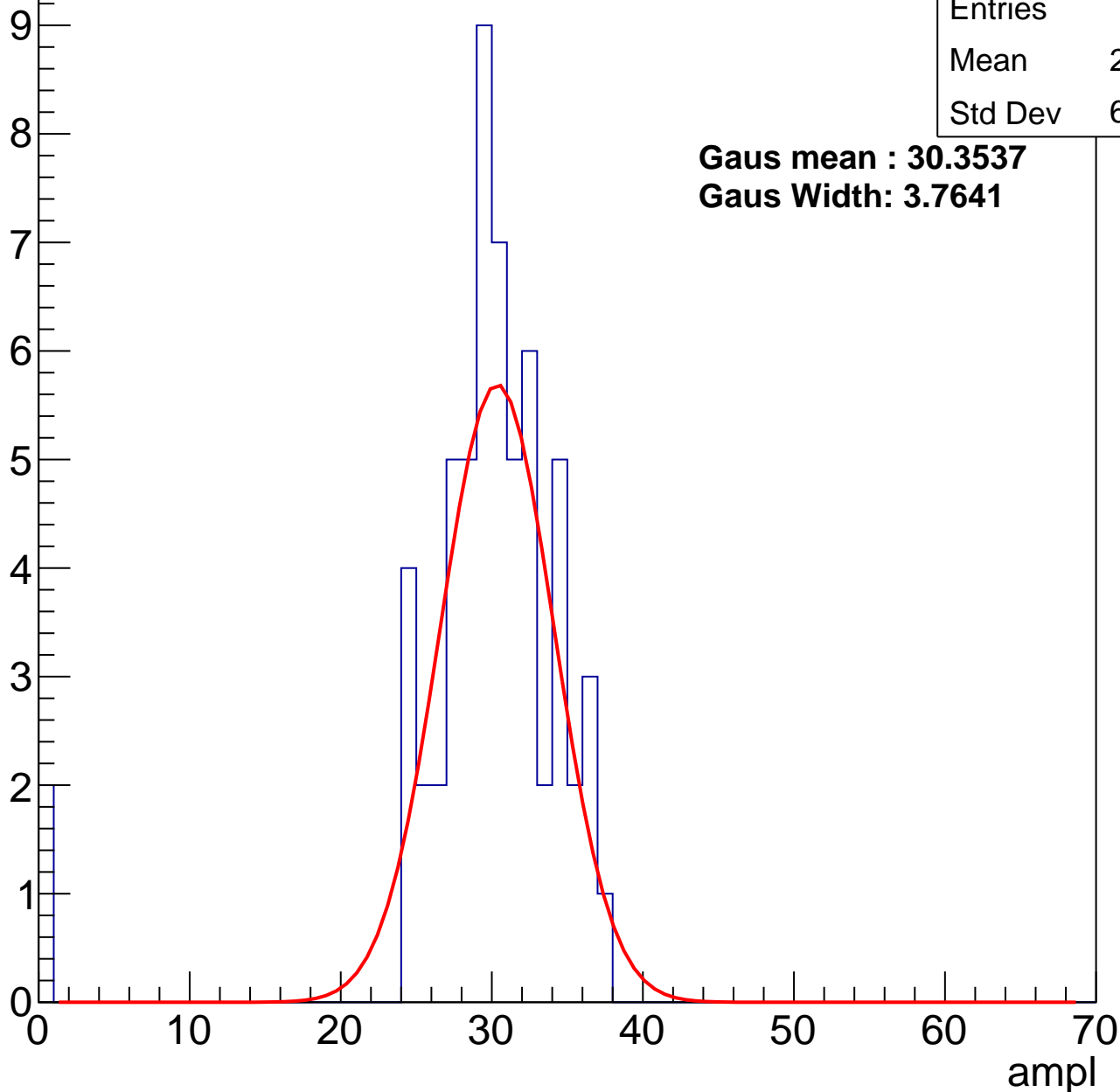
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	29.03
Std Dev	6.295

**Gaus mean : 30.3537**

**Gaus Width: 3.7641**



# B1L003S, U26-ch110, adc1

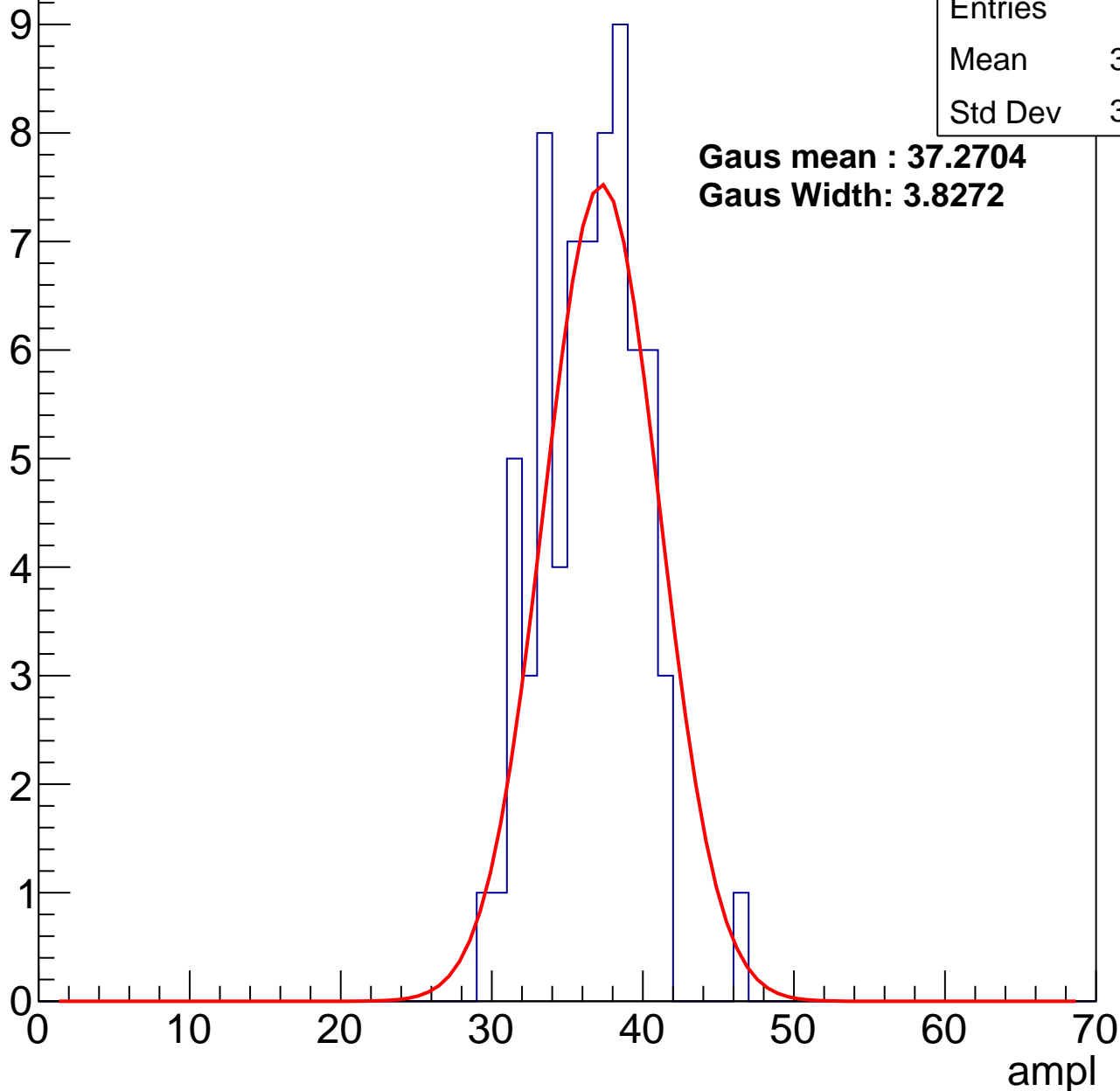
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	36.06
Std Dev	3.234

**Gaus mean : 37.2704**

**Gaus Width: 3.8272**



# B1L003S, U26-ch110, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	42.91
Std Dev	3.476

**Gaus mean : 43.7700**

**Gaus Width: 2.9677**

10

8

6

4

2

0

0

10

20

30

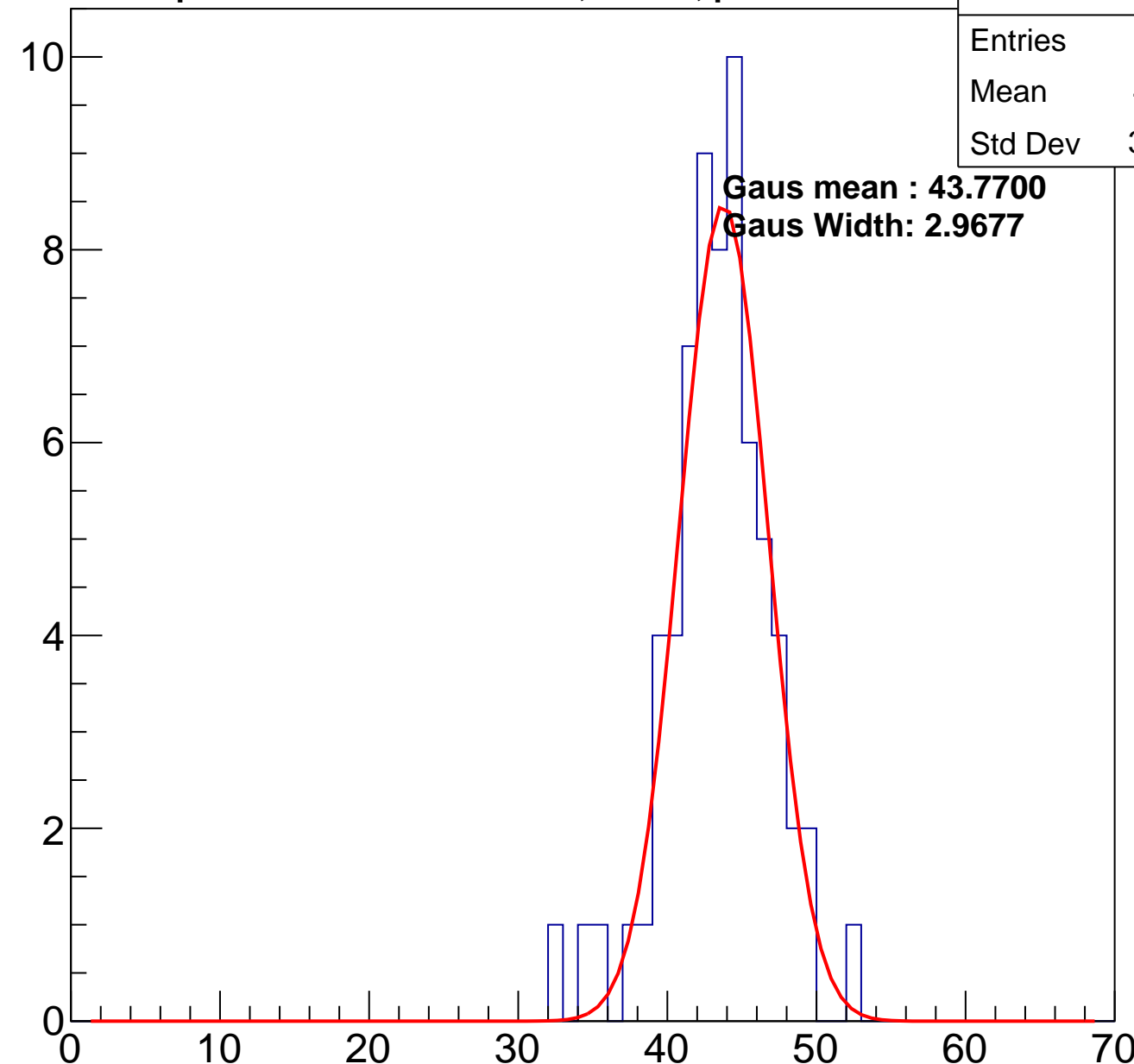
40

50

60

70

ampl

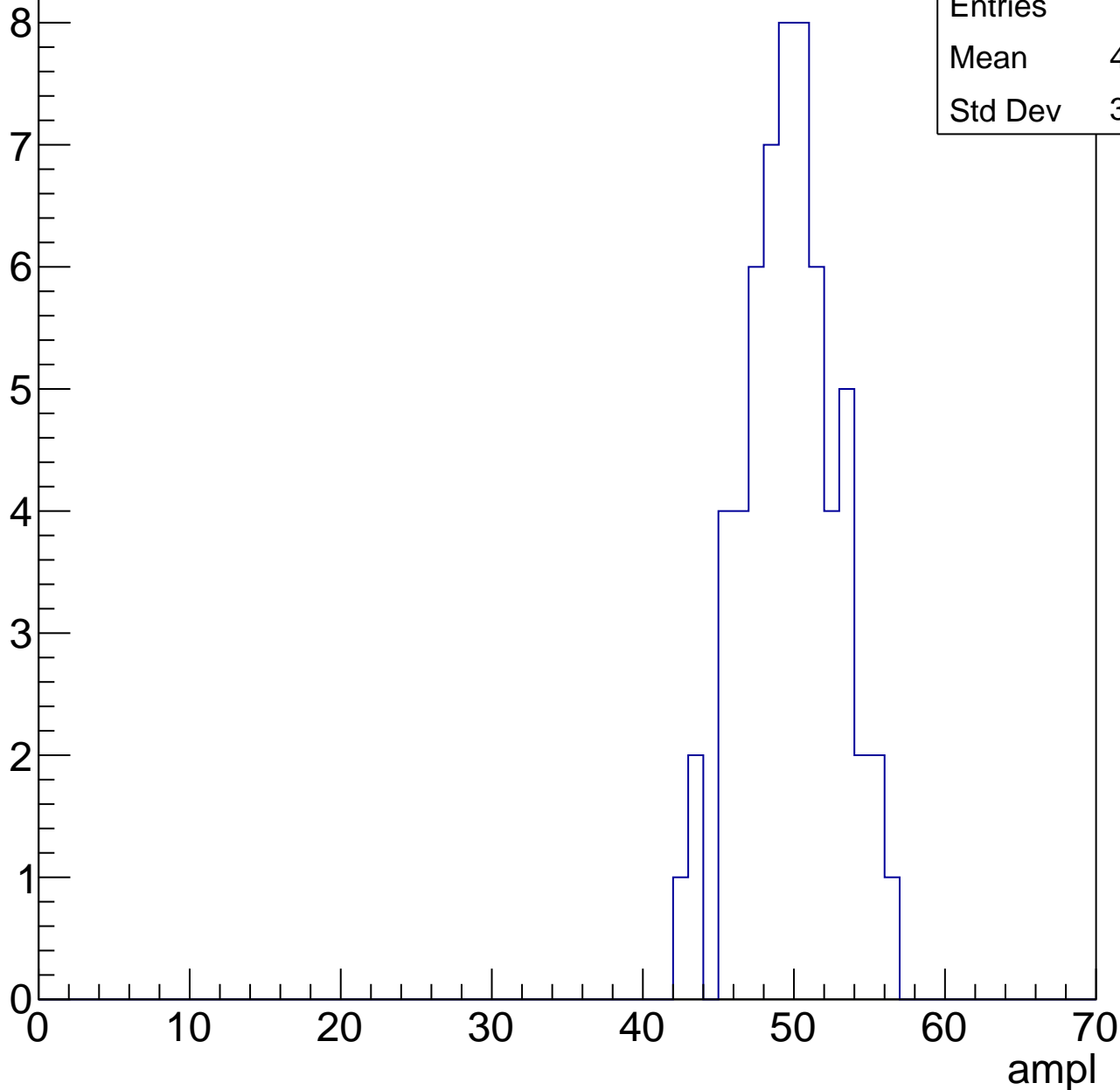


# B1L003S, U26-ch110, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	49.25
Std Dev	3.075

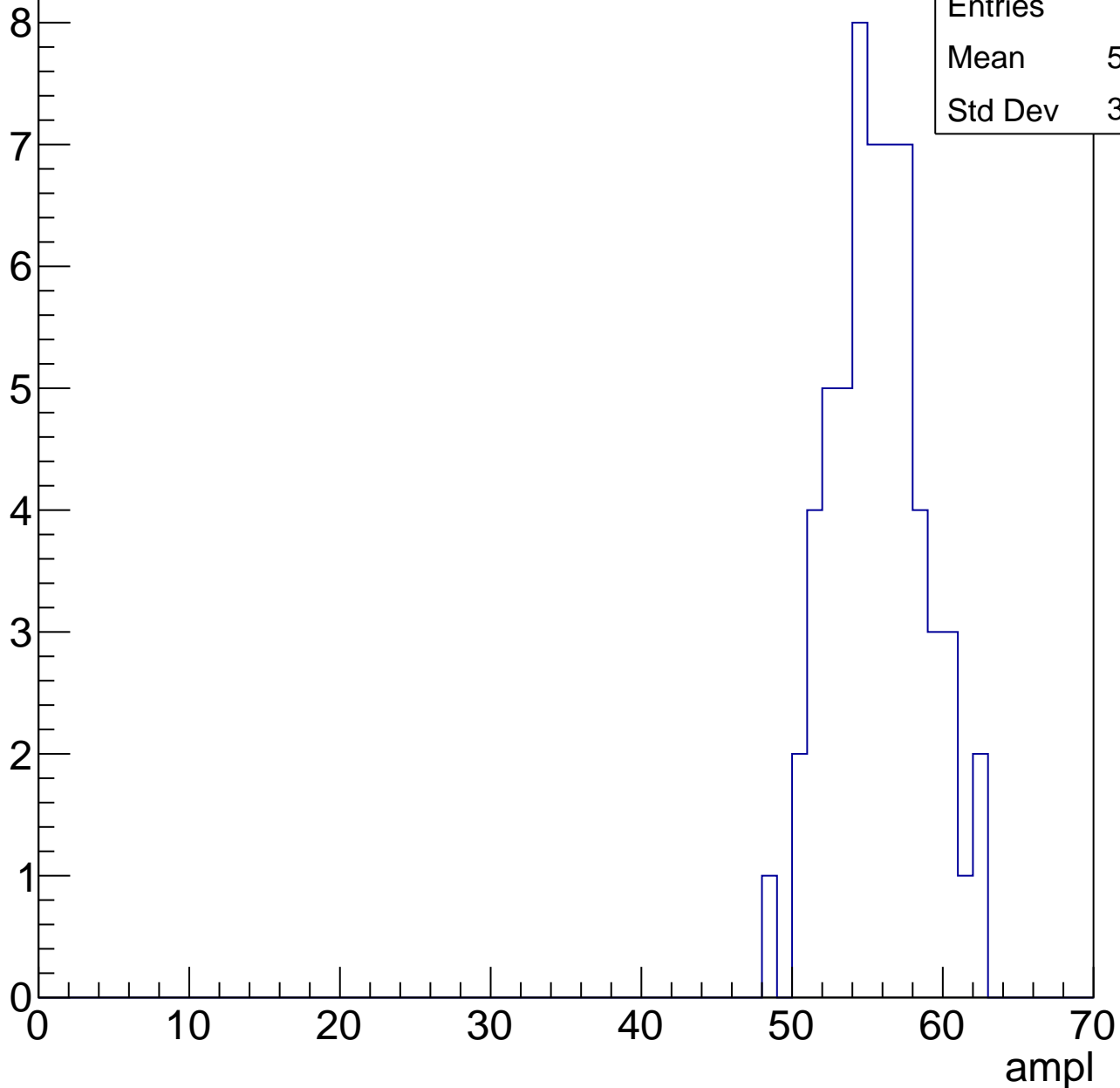


# B1L003S, U26-ch110, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	55.24
Std Dev	3.083

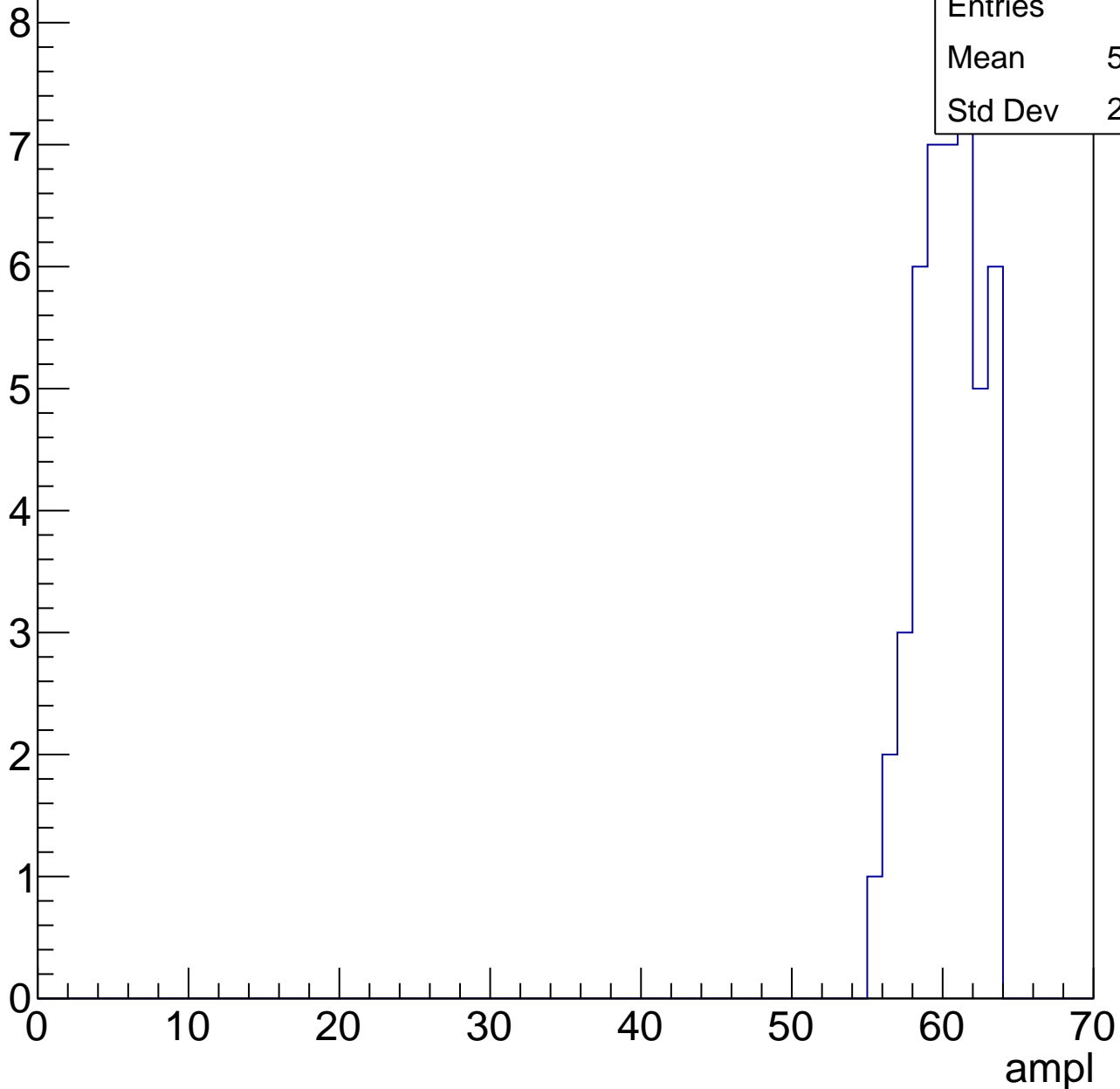


# B1L003S, U26-ch110, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

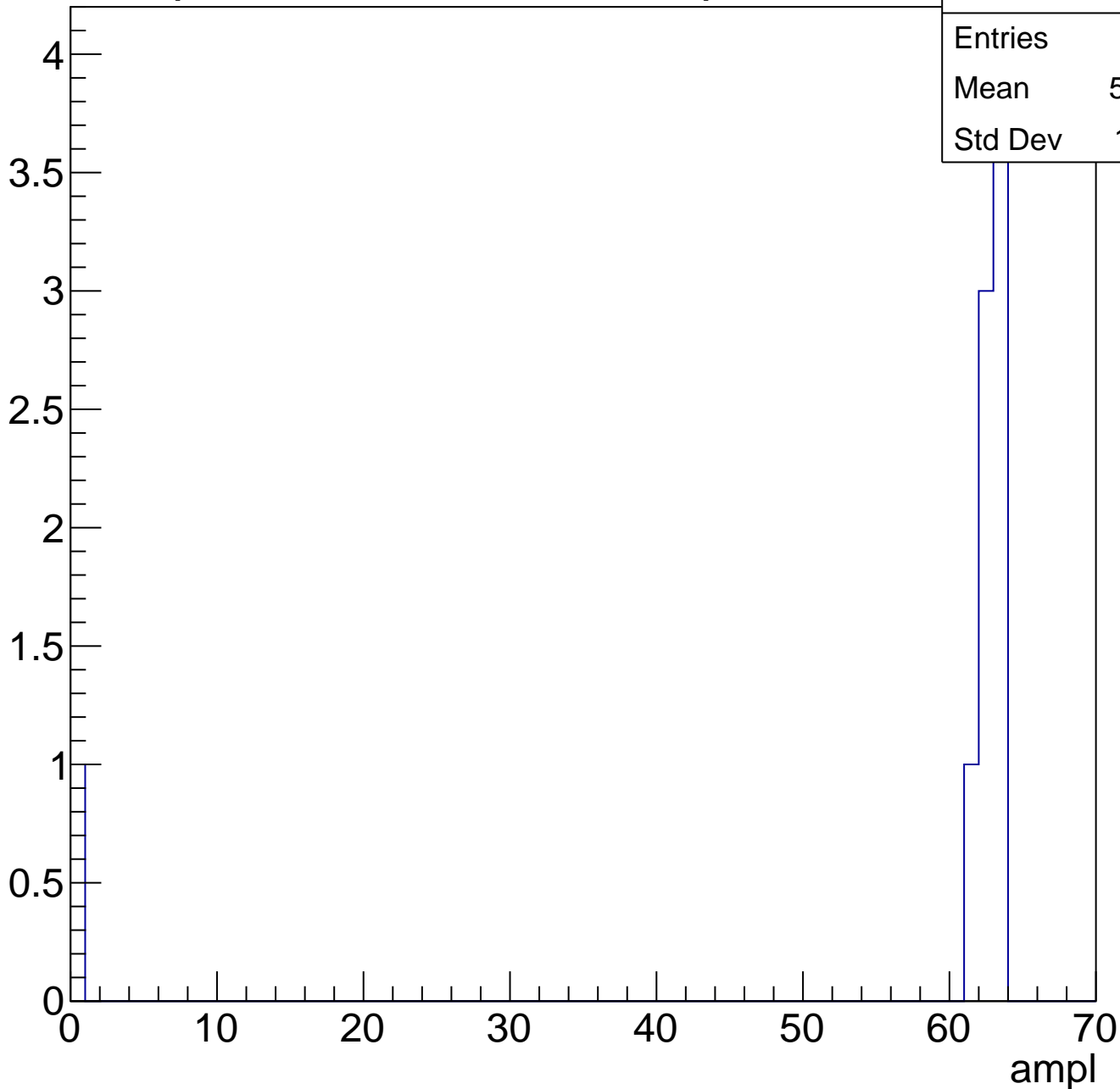
Entries	45
Mean	59.89
Std Dev	2.089



# B1L003S, U26-ch110, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch110, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U26-ch111, adc0

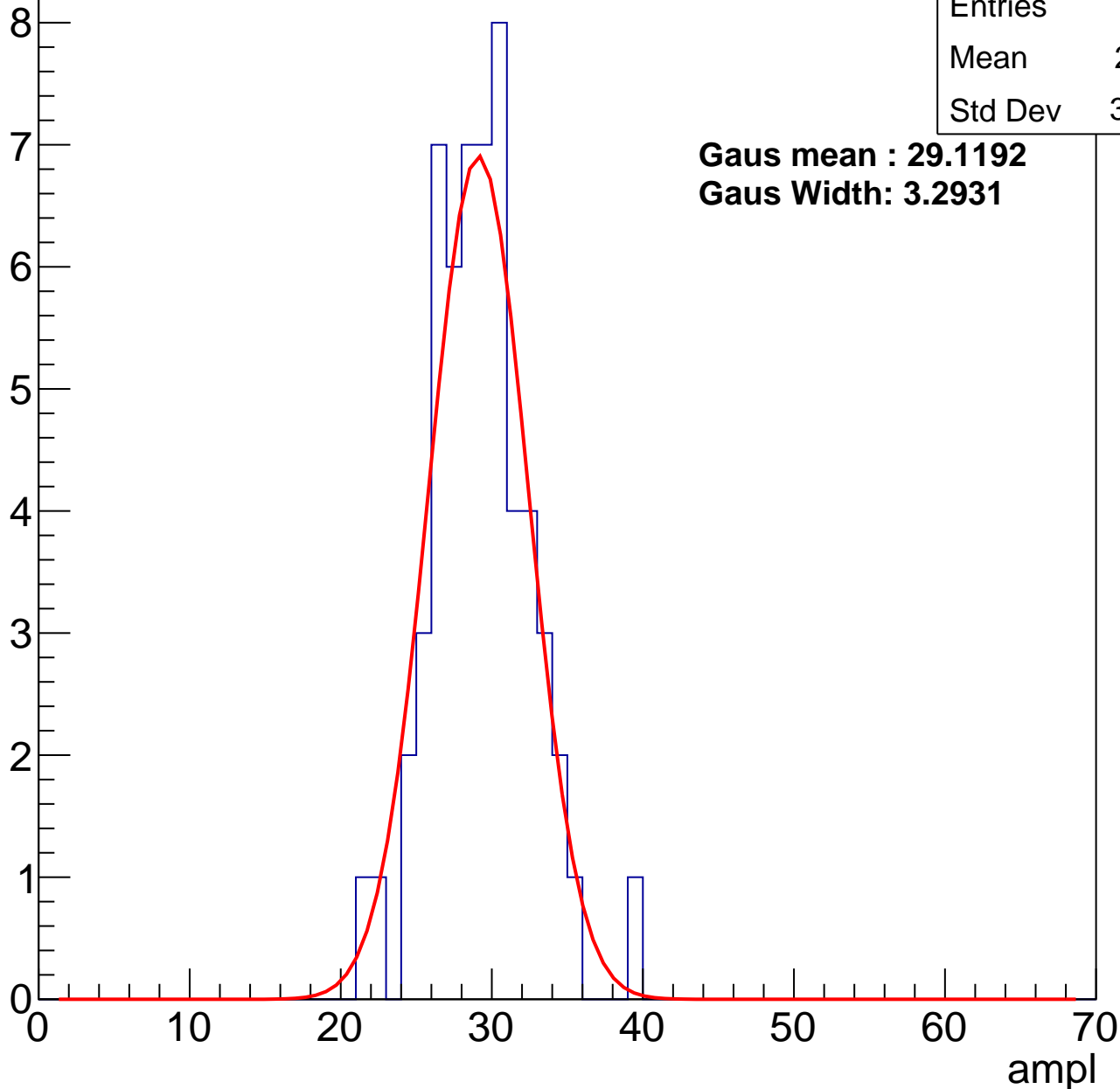
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	28.81
Std Dev	3.236

**Gaus mean : 29.1192**

**Gaus Width: 3.2931**



# B1L003S, U26-ch111, adc1

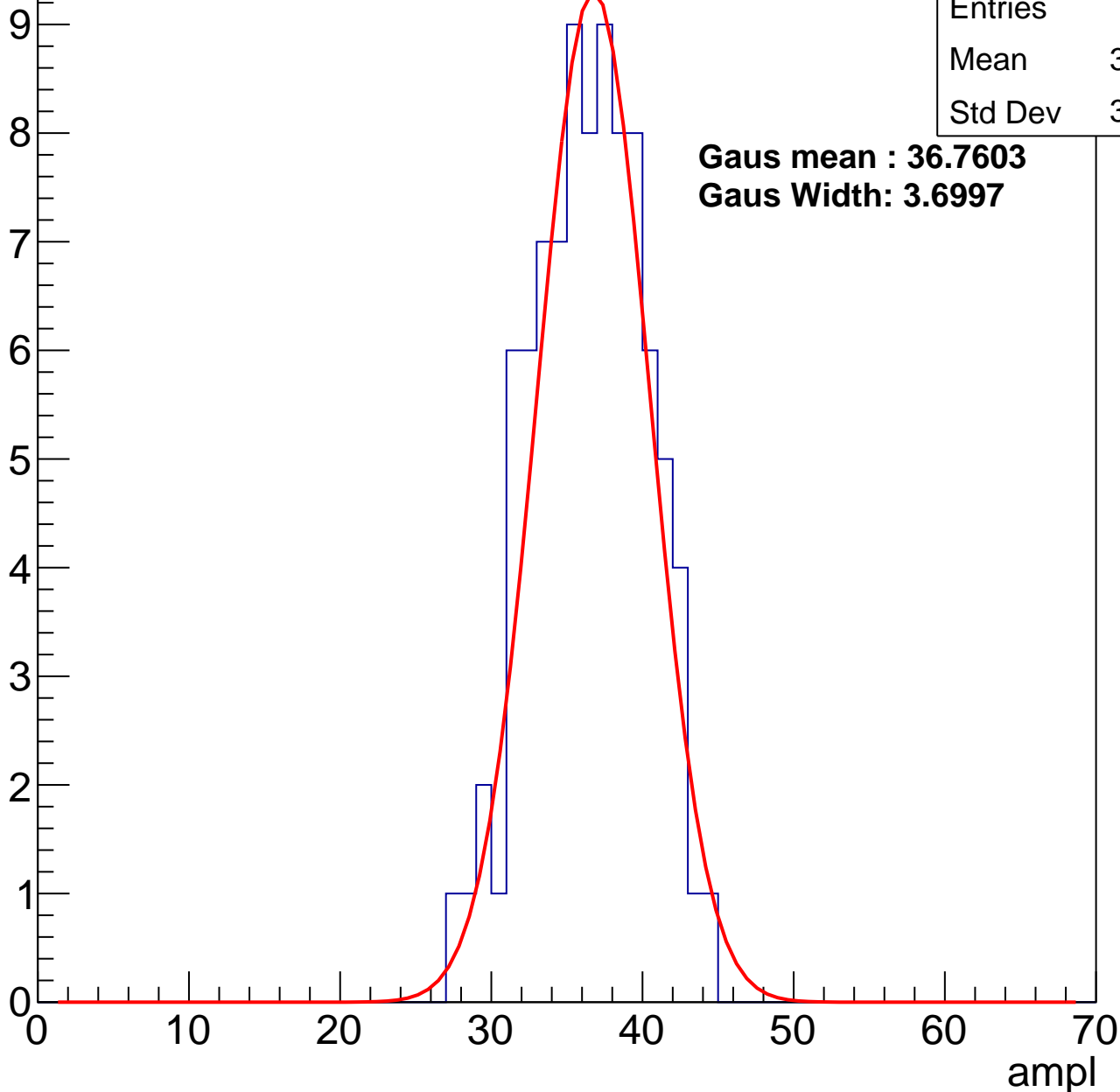
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	90
Mean	36.02
Std Dev	3.676

**Gaus mean : 36.7603**

**Gaus Width: 3.6997**



# B1L003S, U26-ch111, adc2

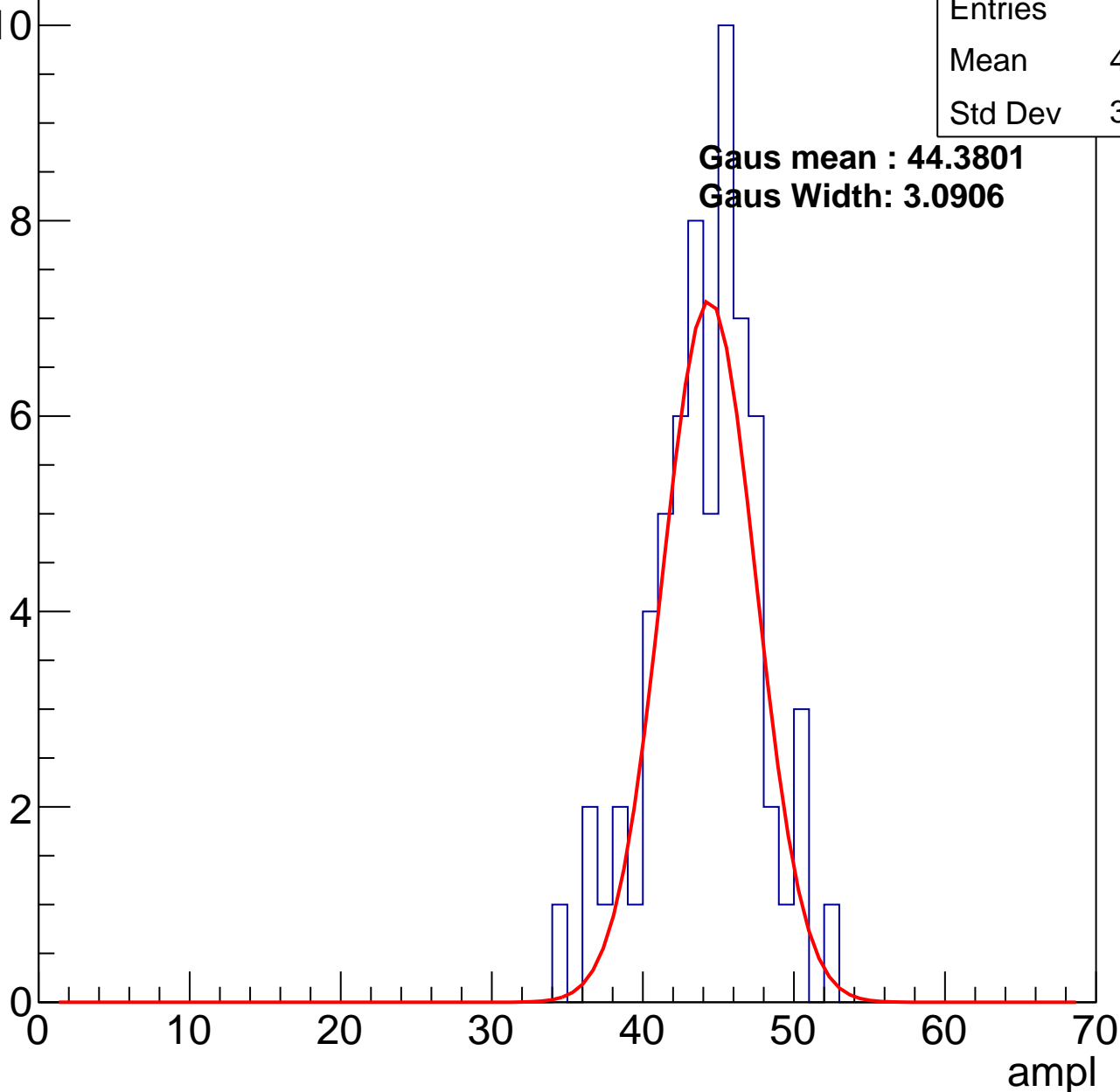
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	43.69
Std Dev	3.573

**Gaus mean : 44.3801**

**Gaus Width: 3.0906**

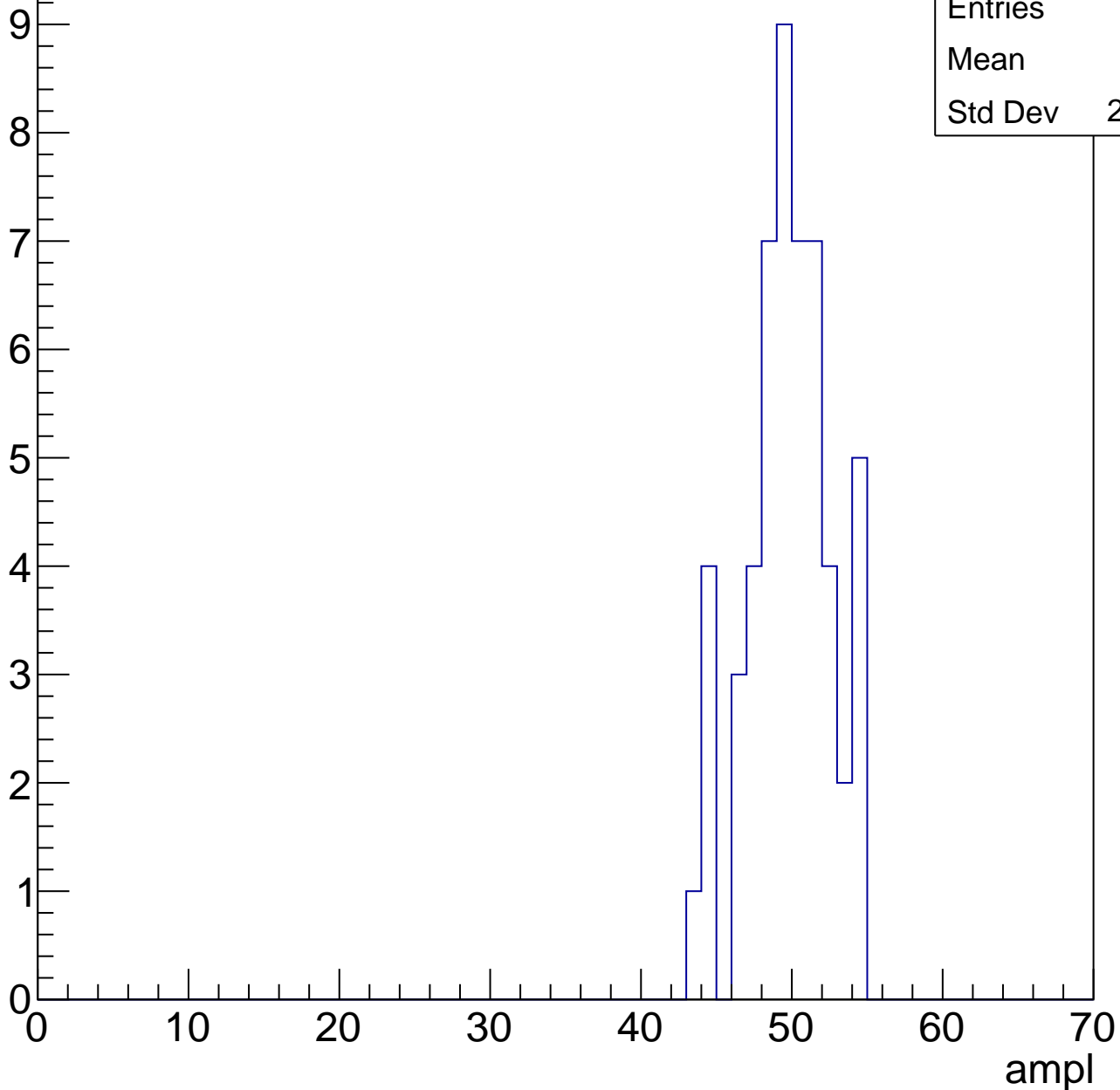


# B1L003S, U26-ch111, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	49.3
Std Dev	2.779

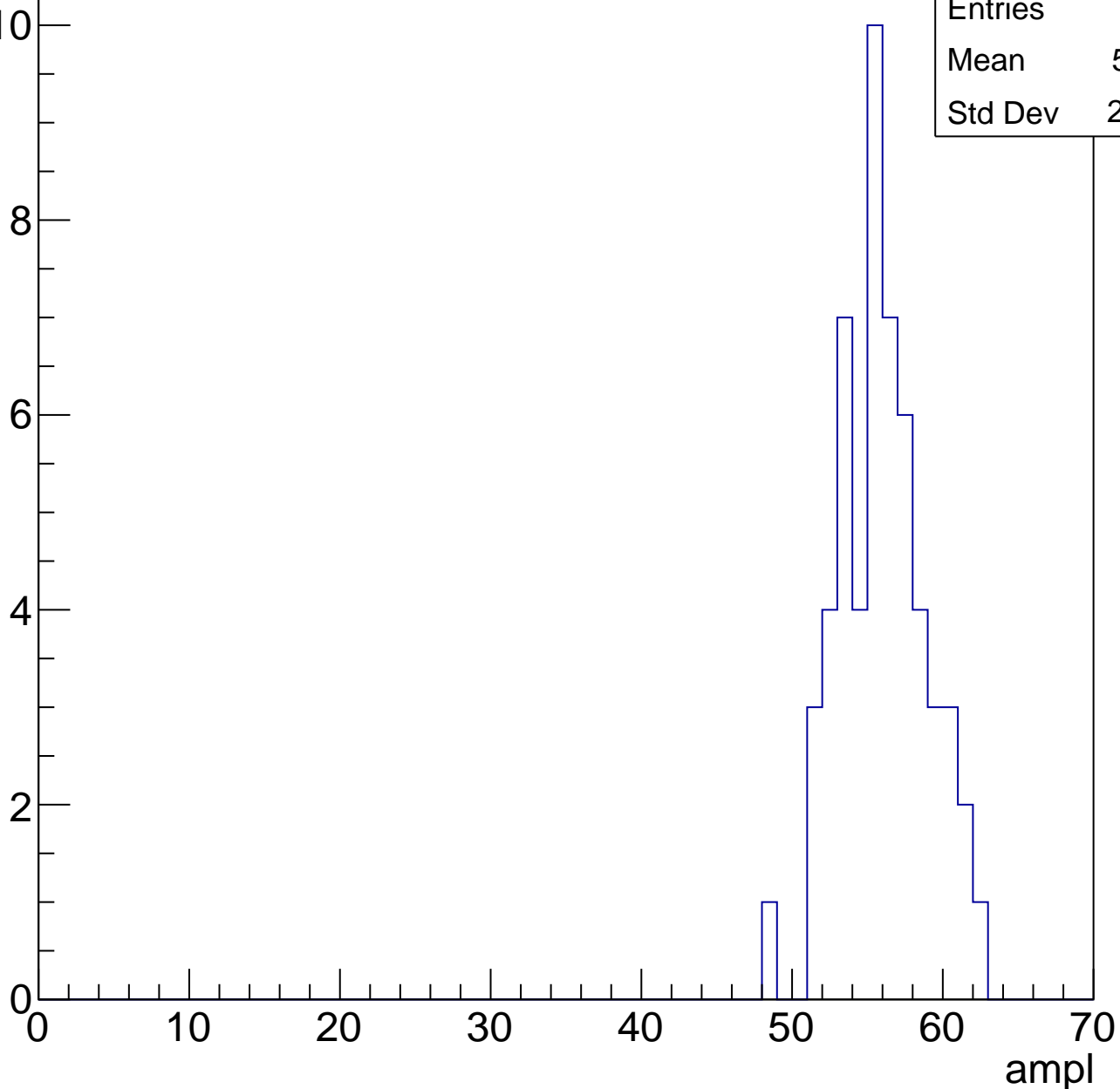


# B1L003S, U26-ch111, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	55.51
Std Dev	2.897

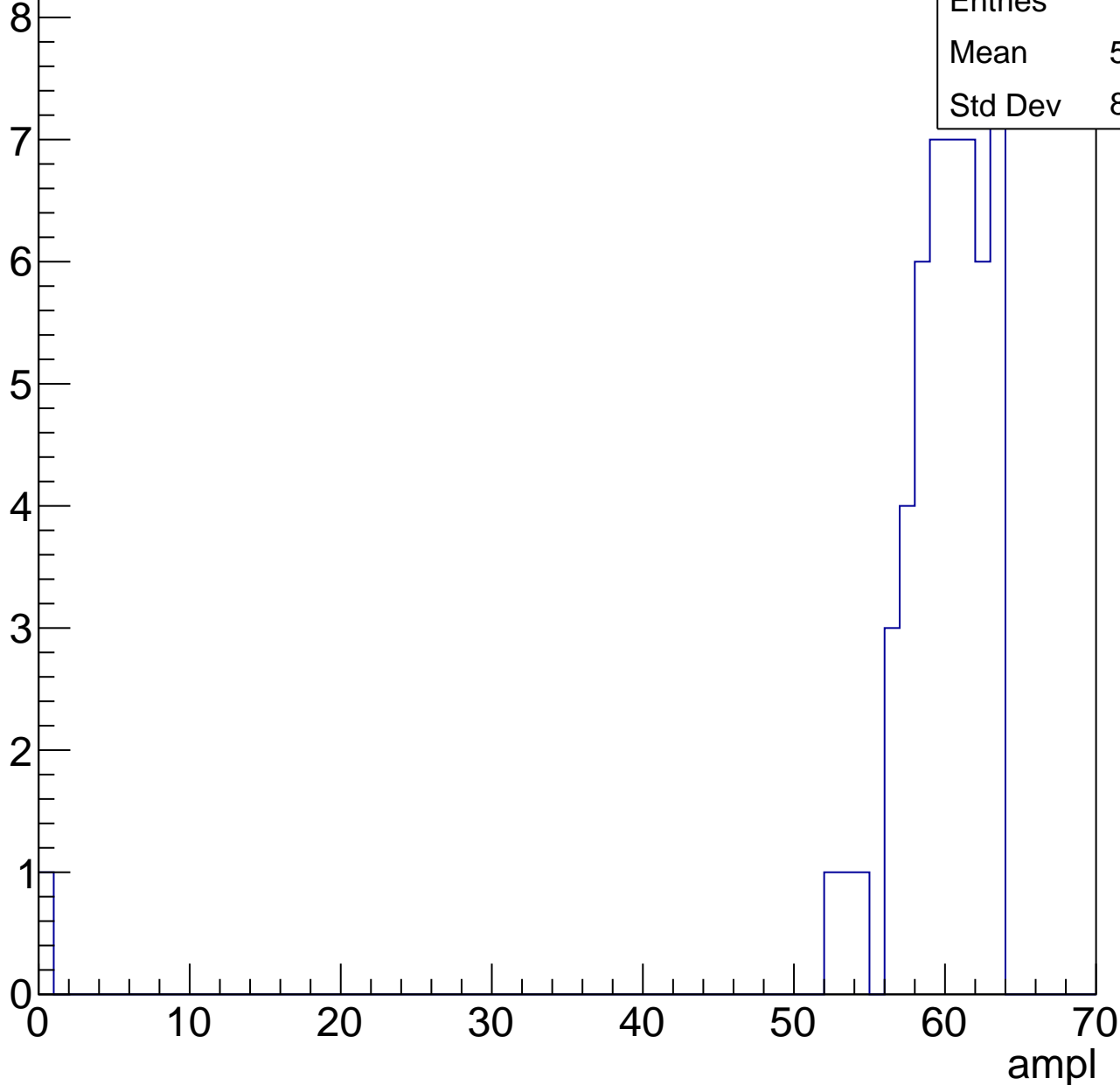


# B1L003S, U26-ch111, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

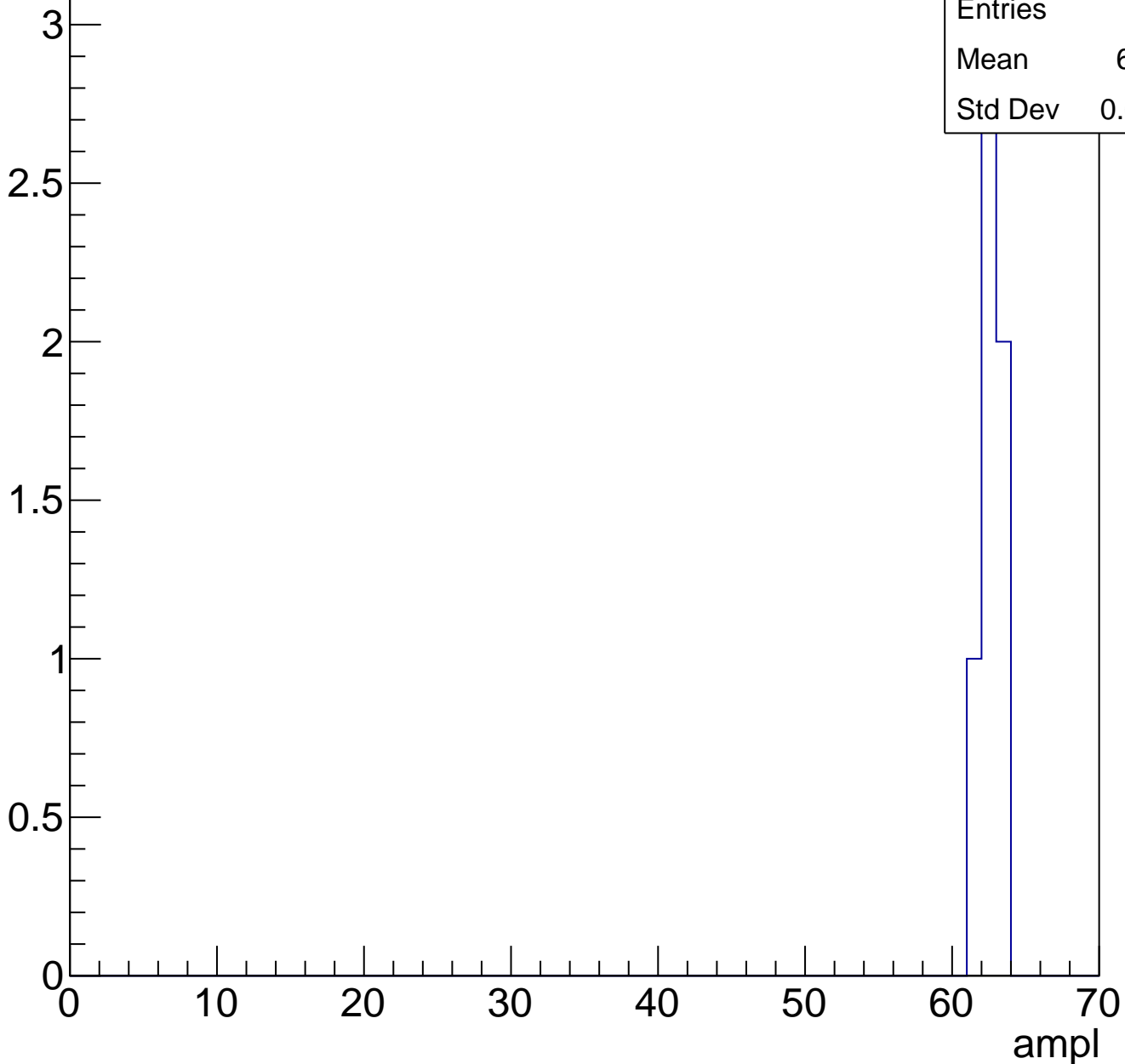
Entries	52
Mean	58.44
Std Dev	8.594



# B1L003S, U26-ch111, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch111, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U26-ch112, adc0

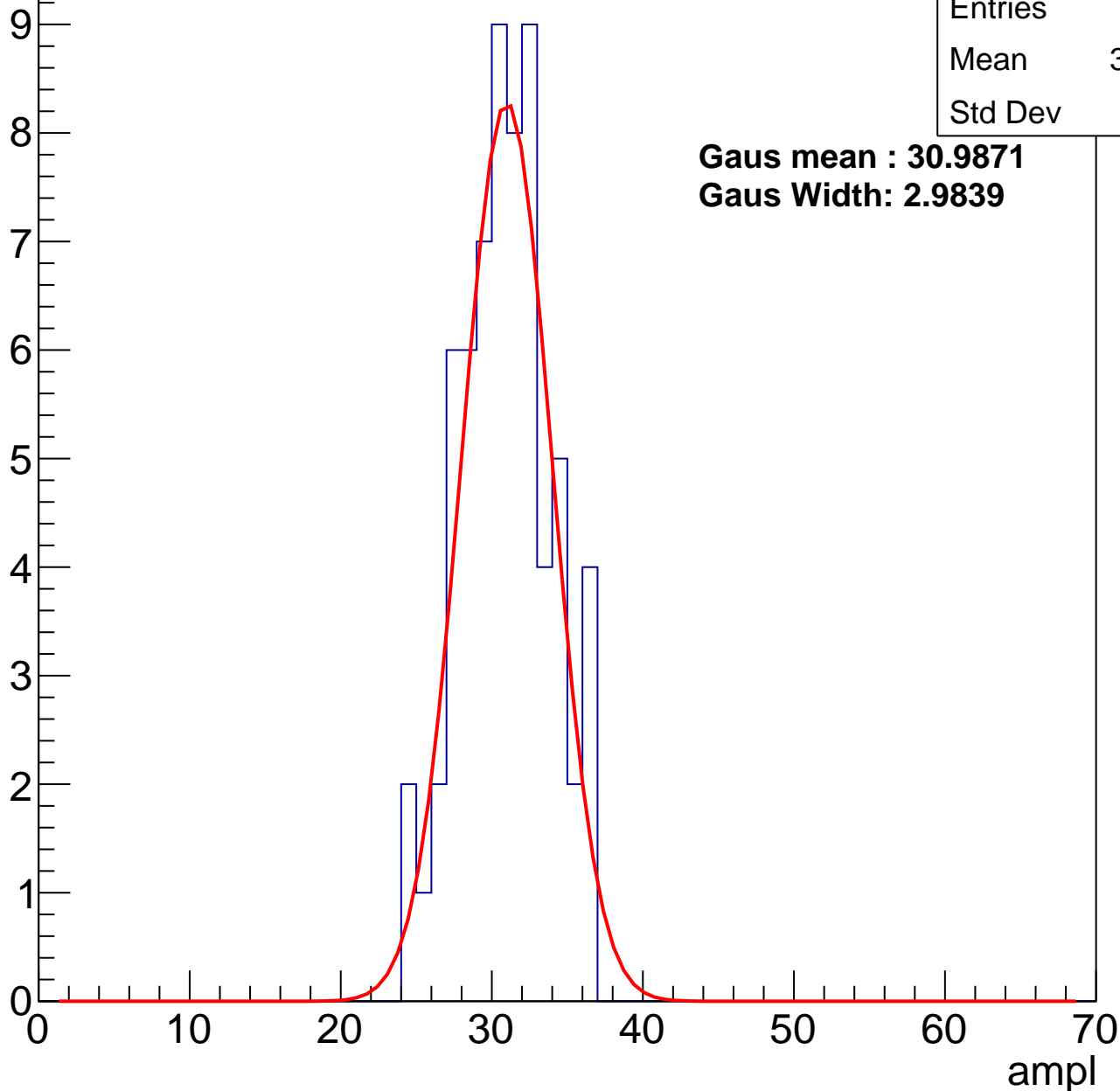
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	30.46
Std Dev	2.92

**Gaus mean : 30.9871**

**Gaus Width: 2.9839**



# B1L003S, U26-ch112, adc1

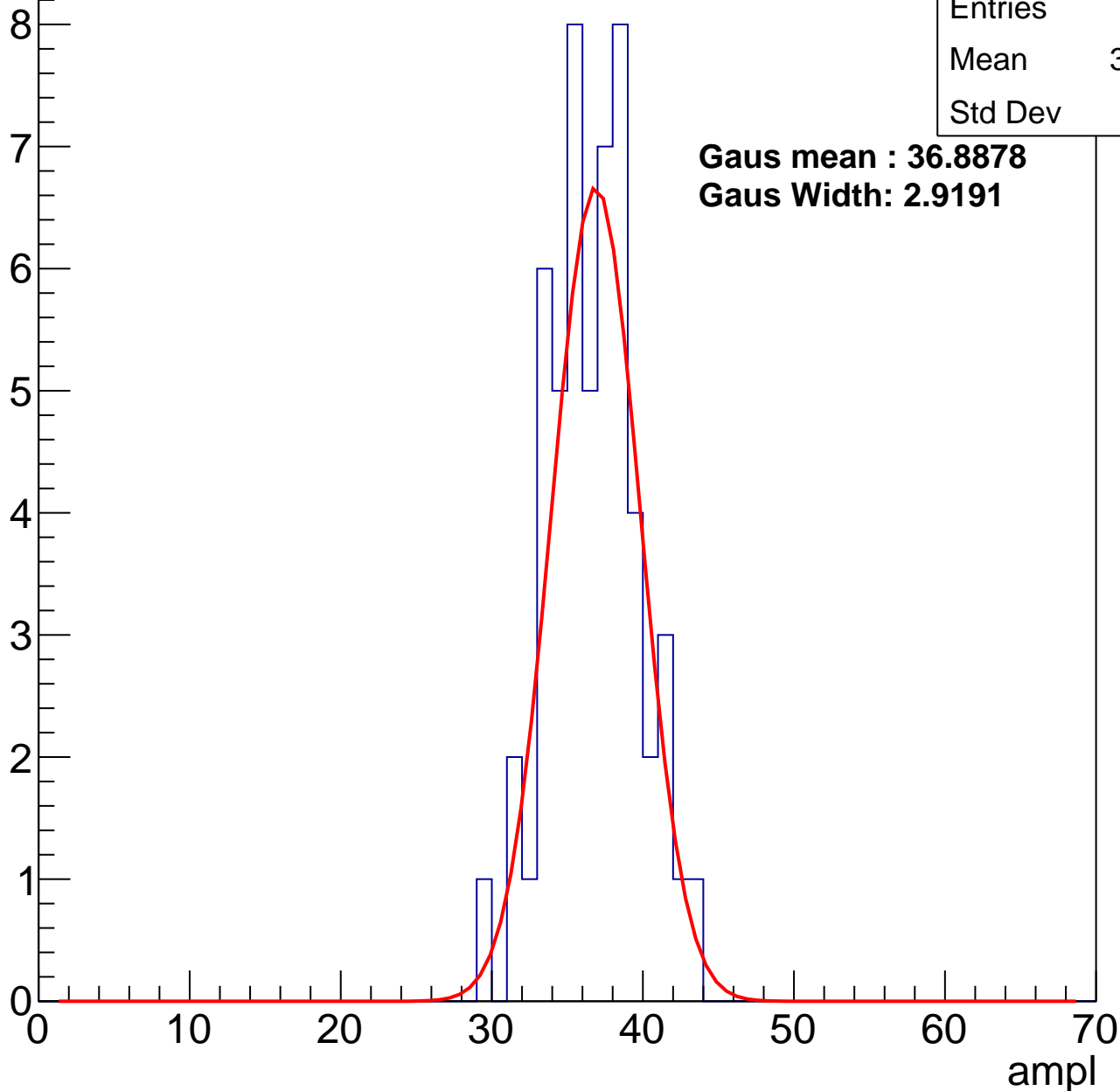
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	54
Mean	36.26
Std Dev	2.92

**Gaus mean : 36.8878**

**Gaus Width: 2.9191**



# B1L003S, U26-ch112, adc2

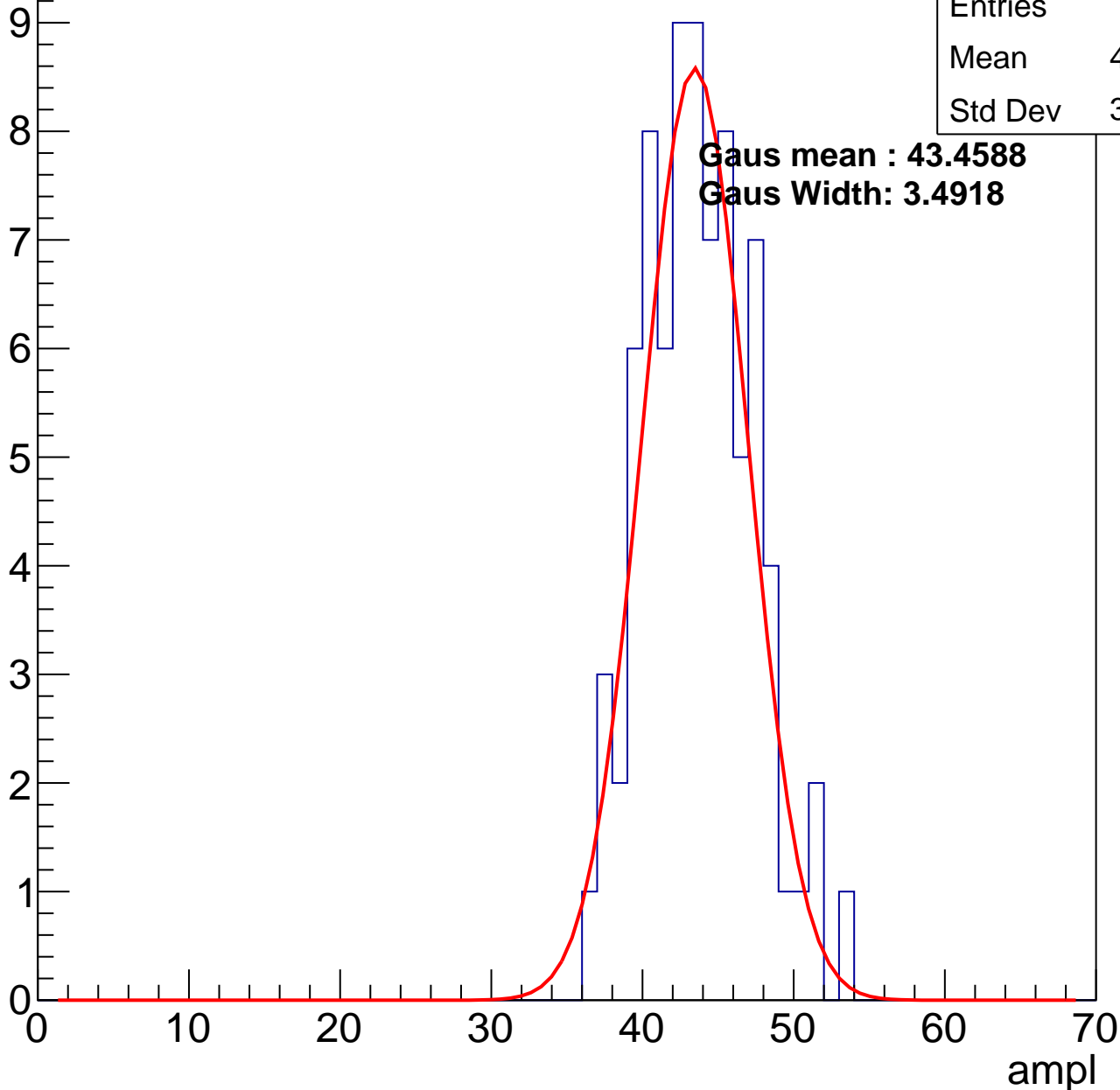
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	80
Mean	43.26
Std Dev	3.556

**Gaus mean : 43.4588**

**Gaus Width: 3.4918**

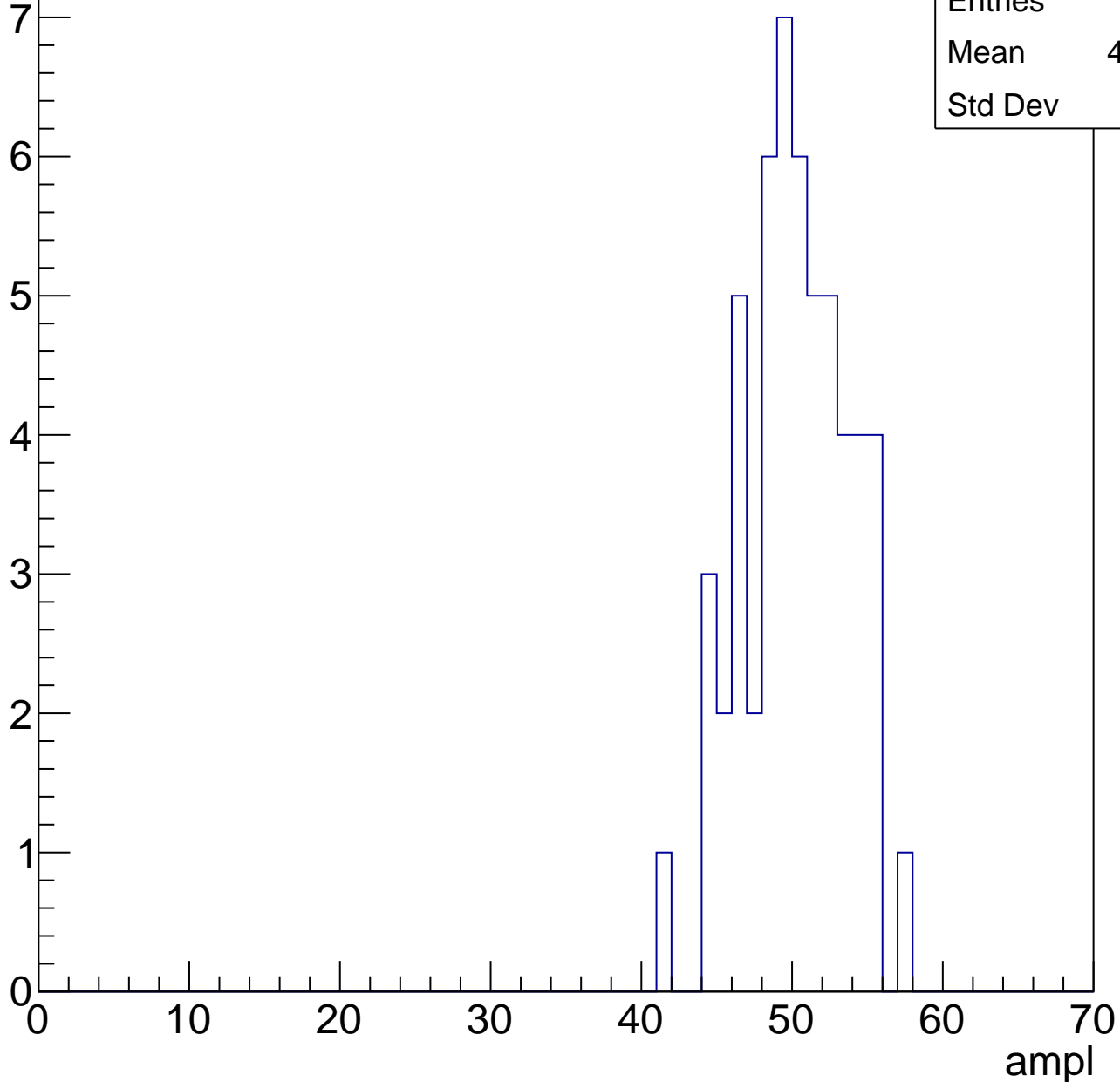


# B1L003S, U26-ch112, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	49.78
Std Dev	3.41

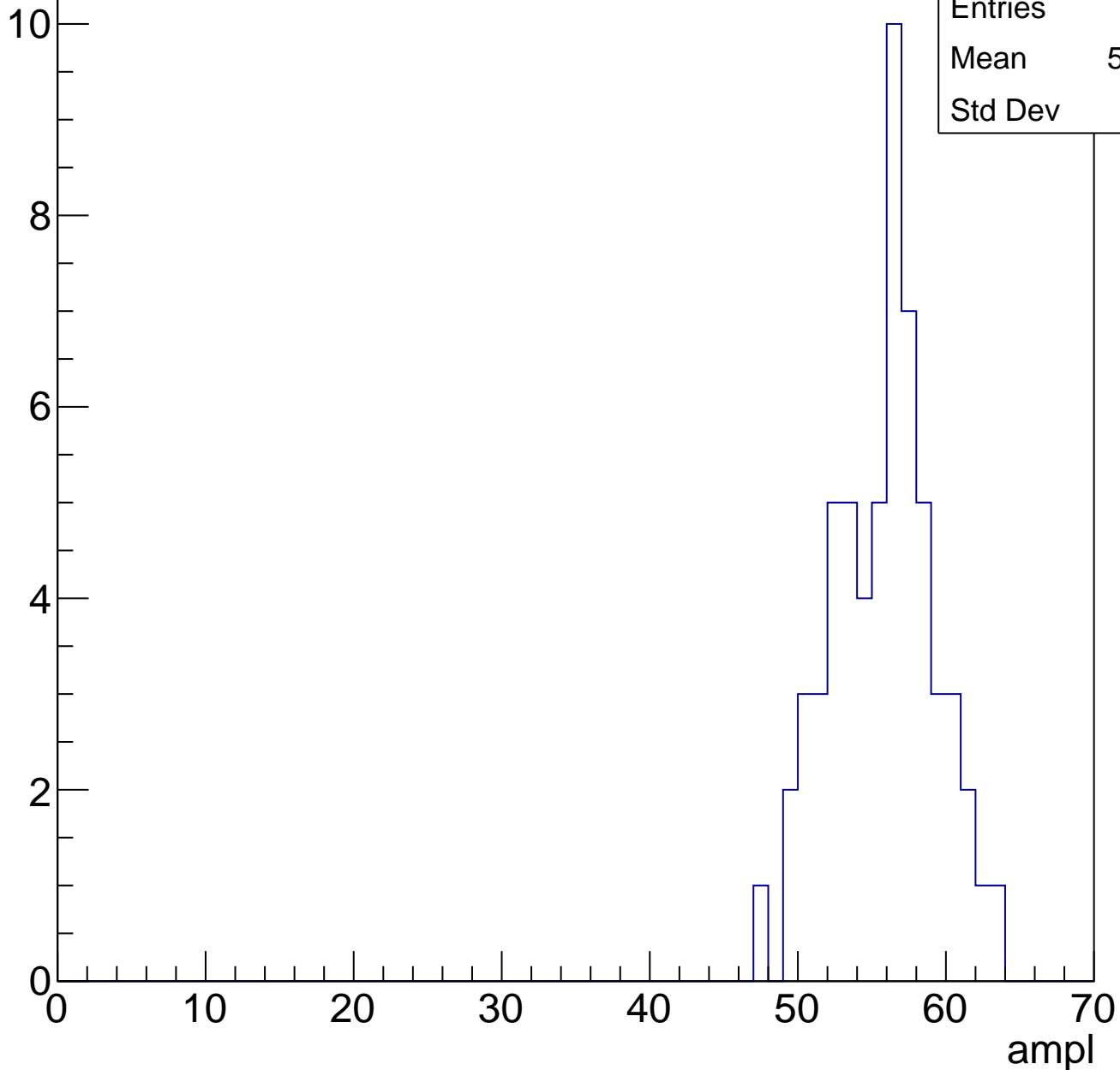


# B1L003S, U26-ch112, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	60
Mean	55.28
Std Dev	3.45

Entry

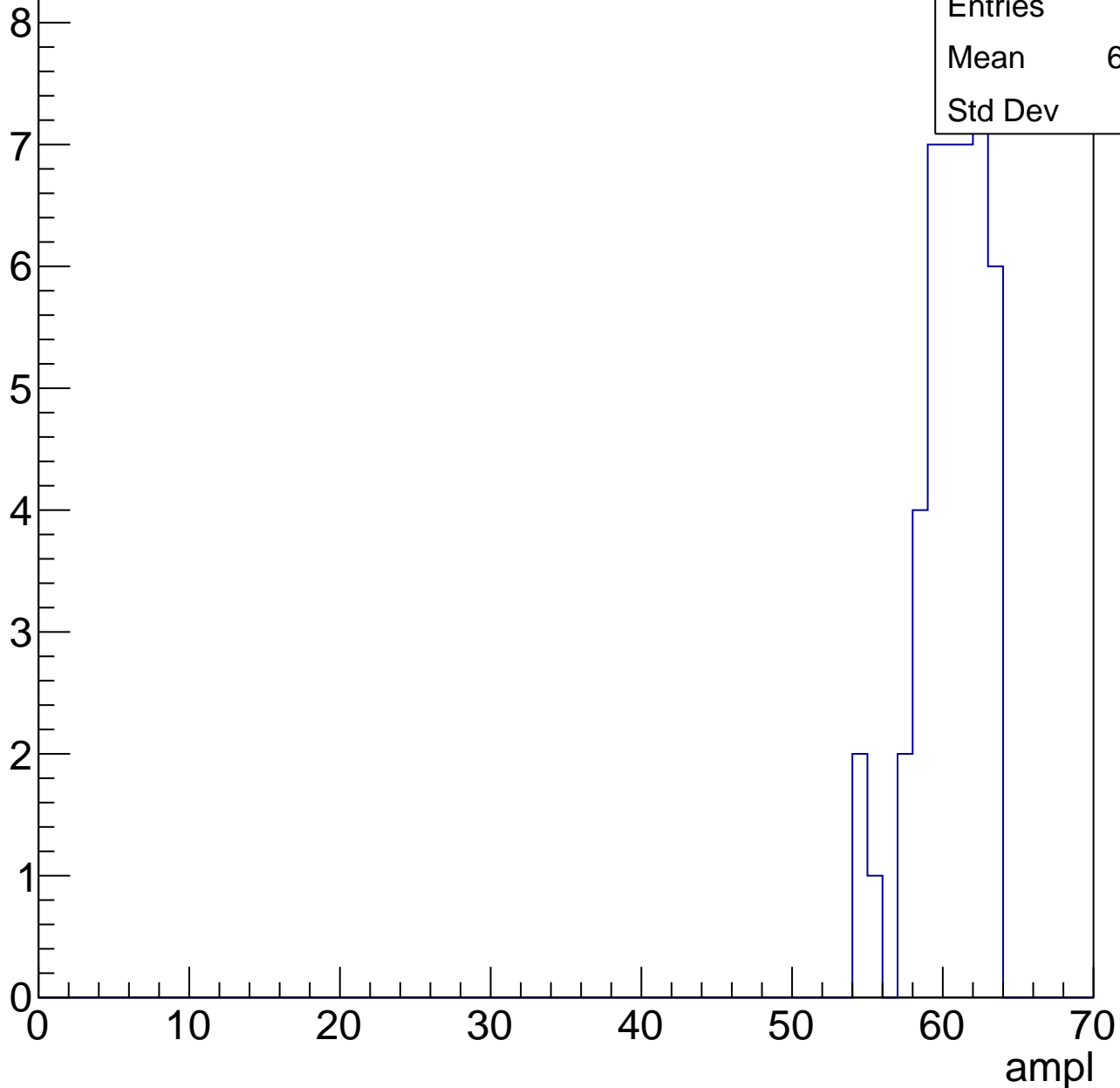


# B1L003S, U26-ch112, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

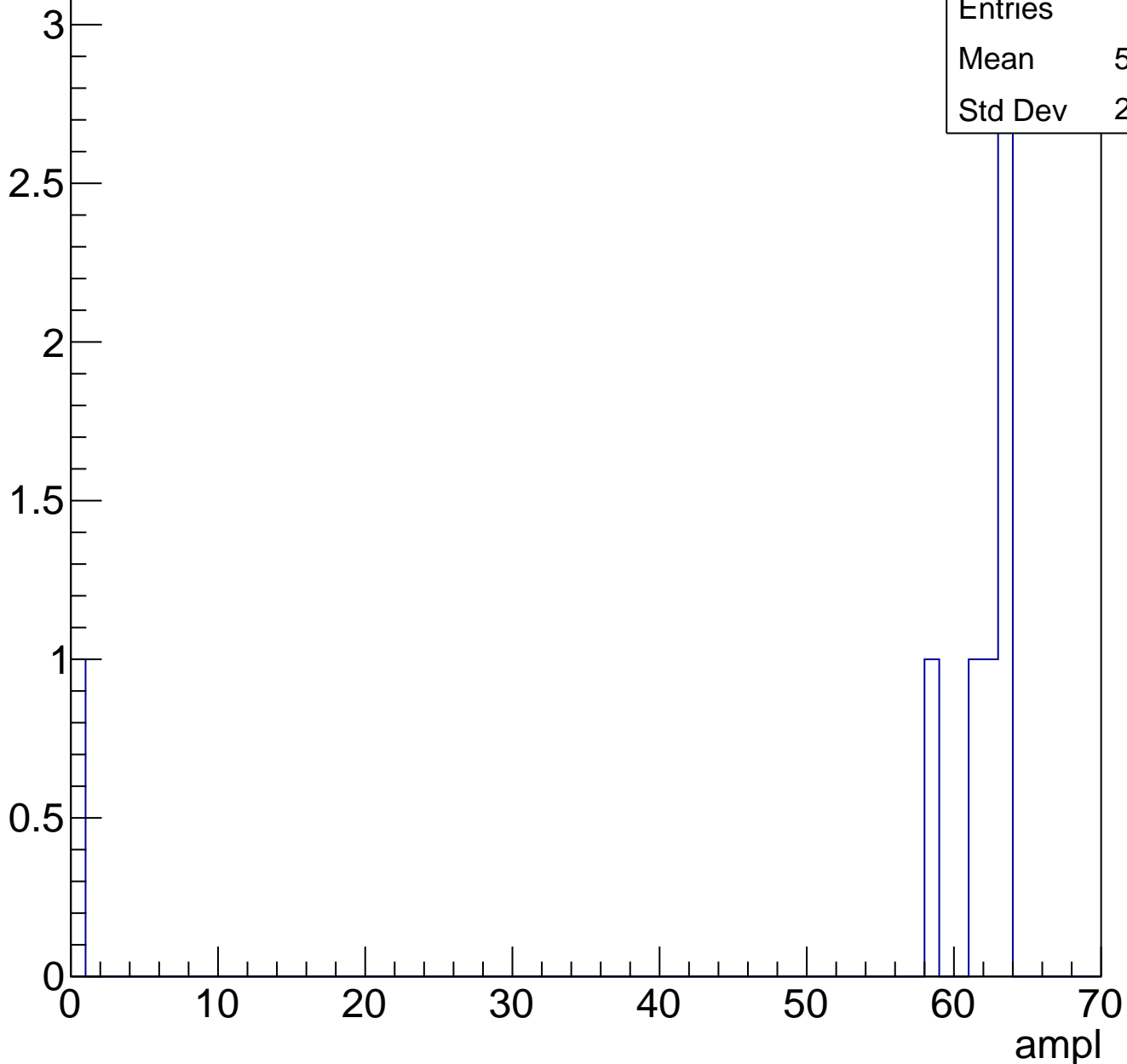
Entries	44
Mean	60.07
Std Dev	2.29



# B1L003S, U26-ch112, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch112, adc7

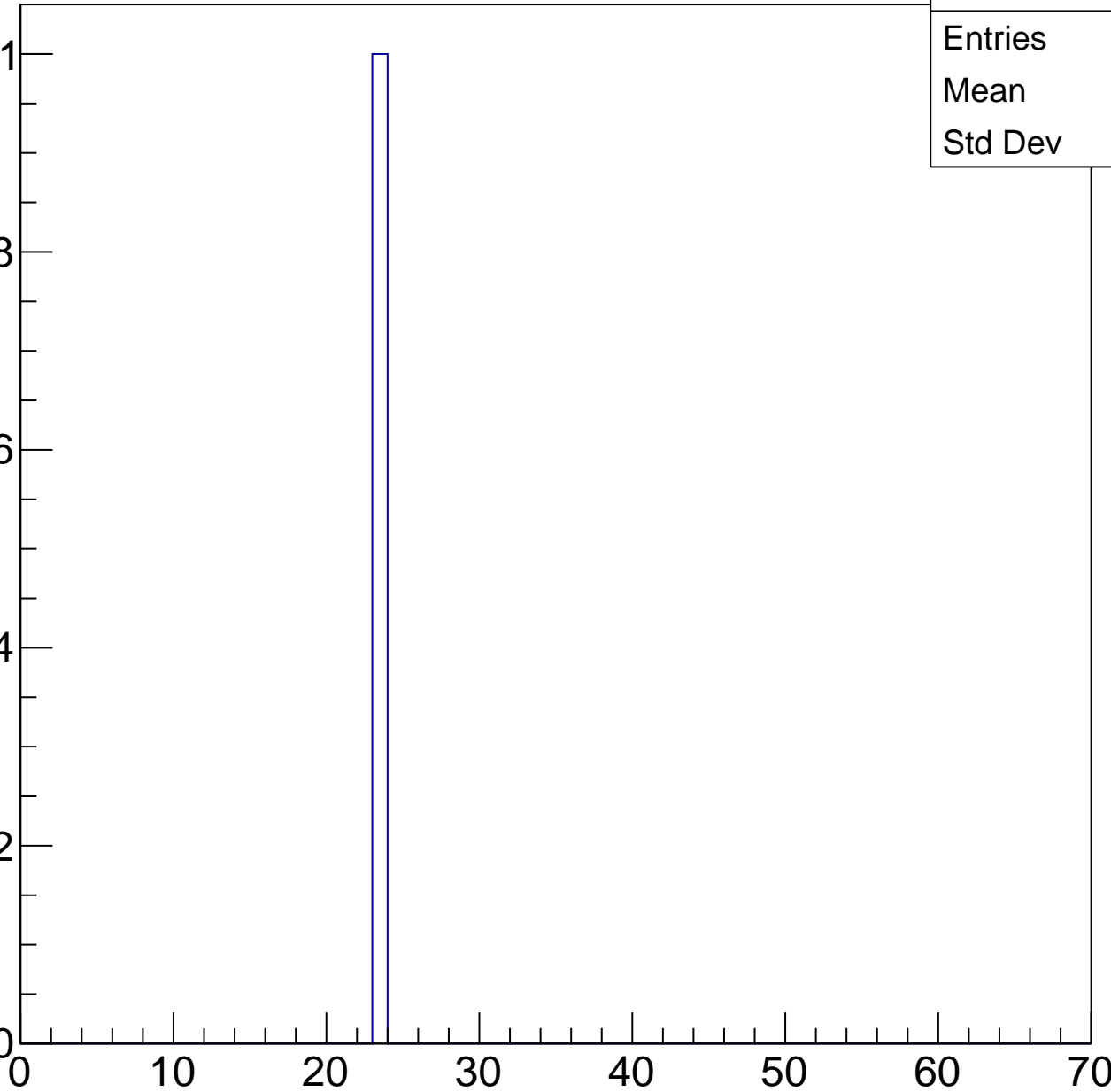
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	23
Std Dev	0

ampl



# B1L003S, U26-ch113, adc0

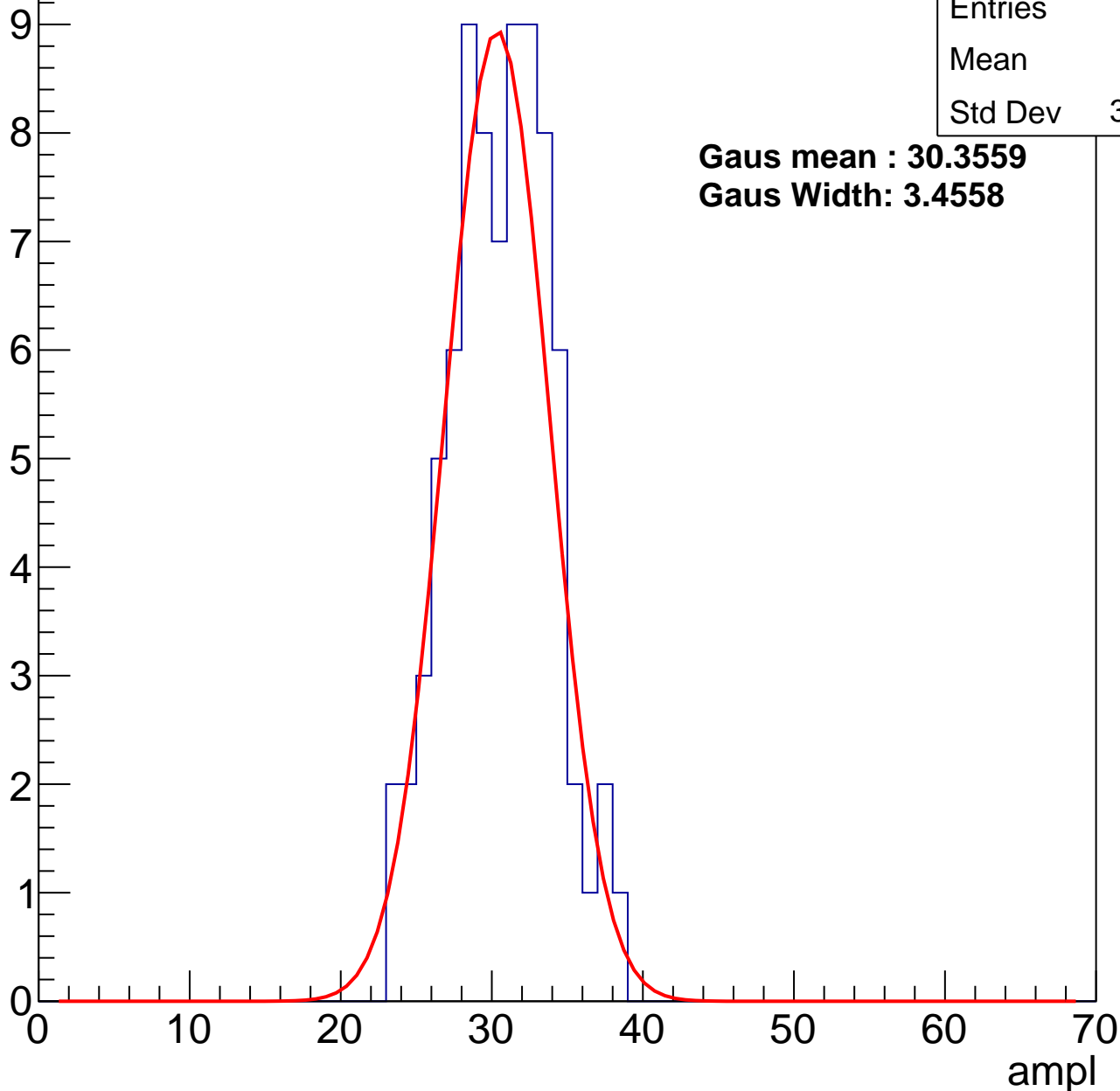
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	80
Mean	30.1
Std Dev	3.323

**Gaus mean : 30.3559**

**Gaus Width: 3.4558**



# B1L003S, U26-ch113, adc1

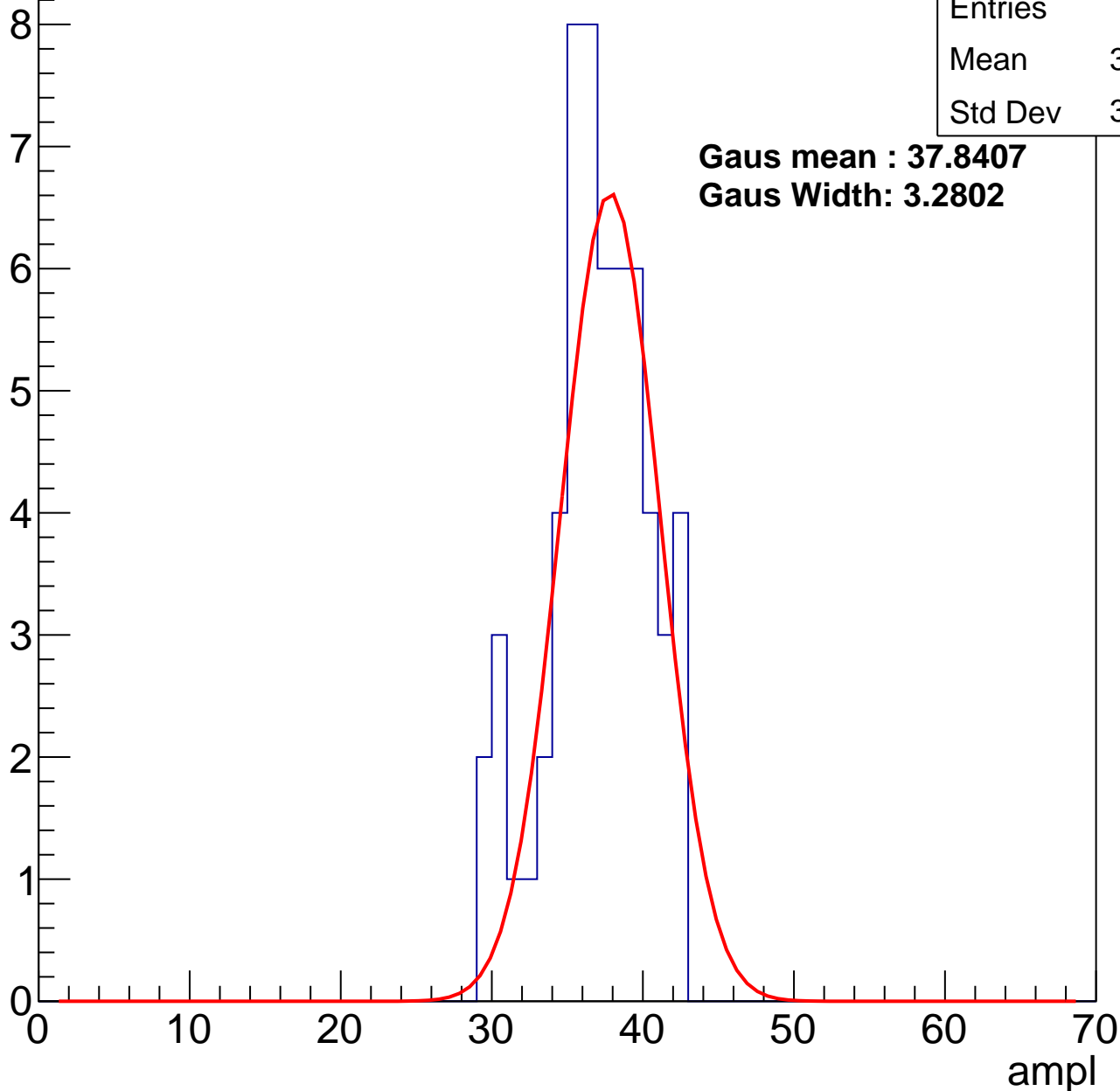
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	36.48
Std Dev	3.328

**Gaus mean : 37.8407**

**Gaus Width: 3.2802**



# B1L003S, U26-ch113, adc2

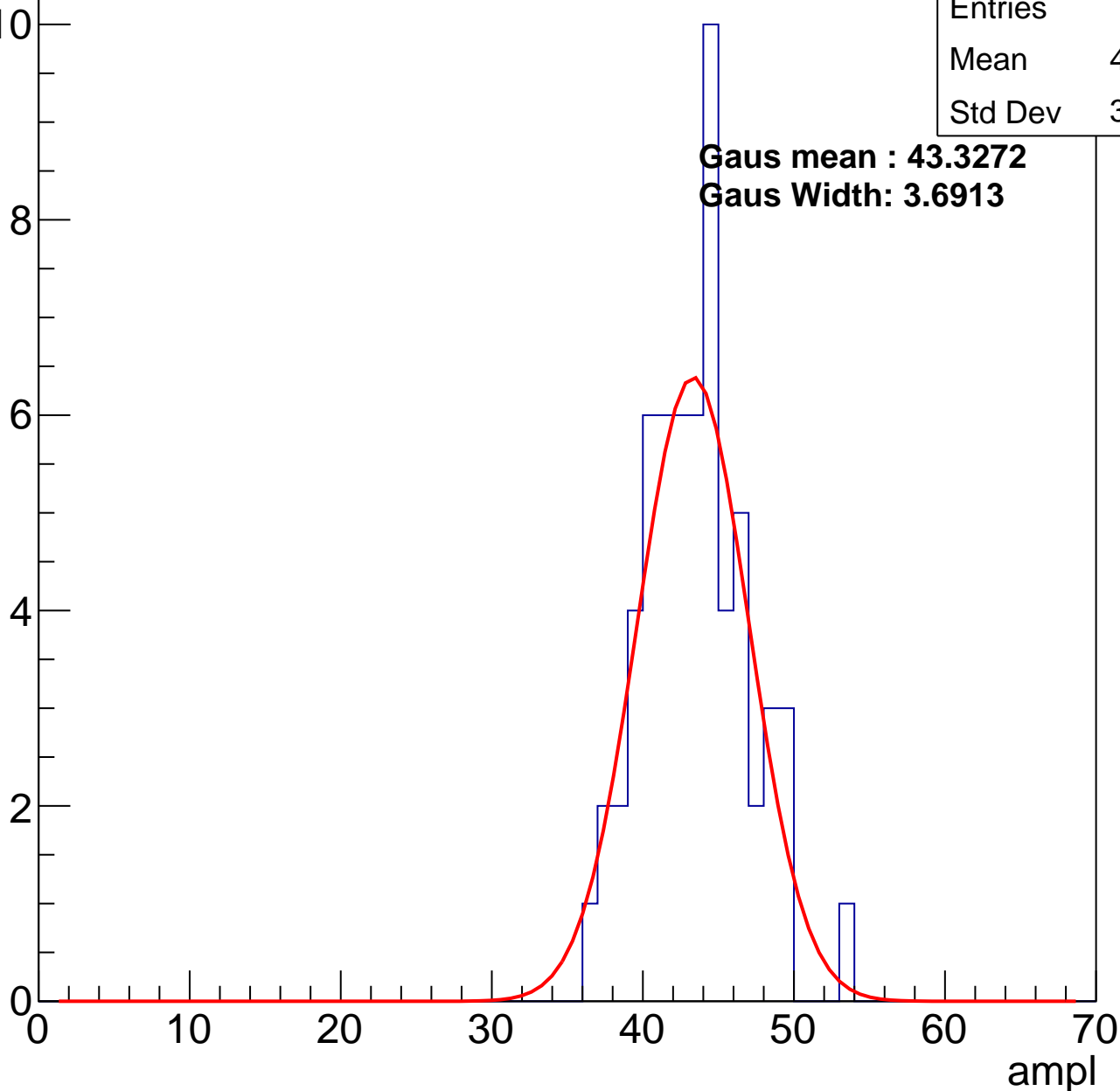
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	43.05
Std Dev	3.399

**Gaus mean : 43.3272**

**Gaus Width: 3.6913**

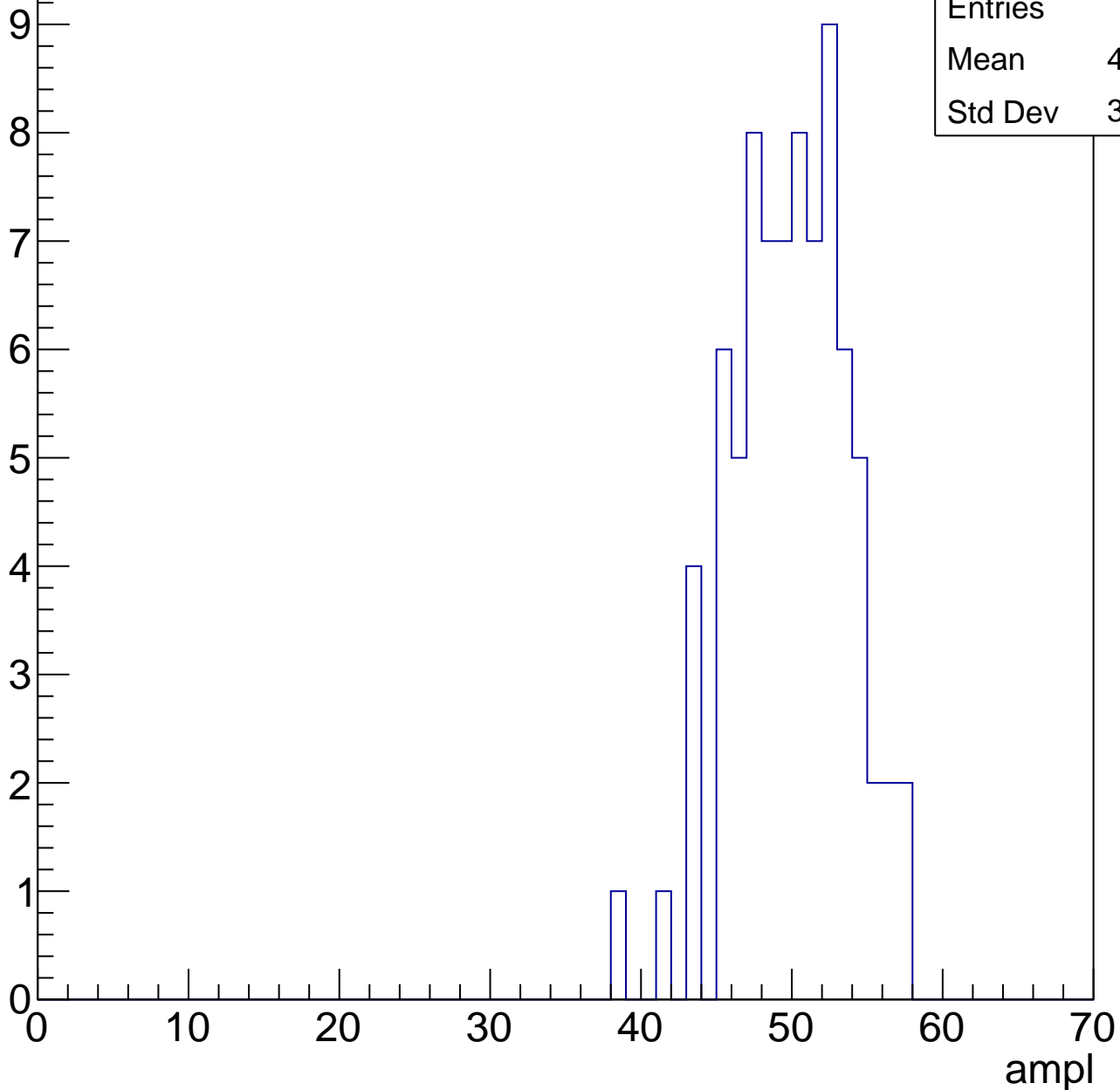


# B1L003S, U26-ch113, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

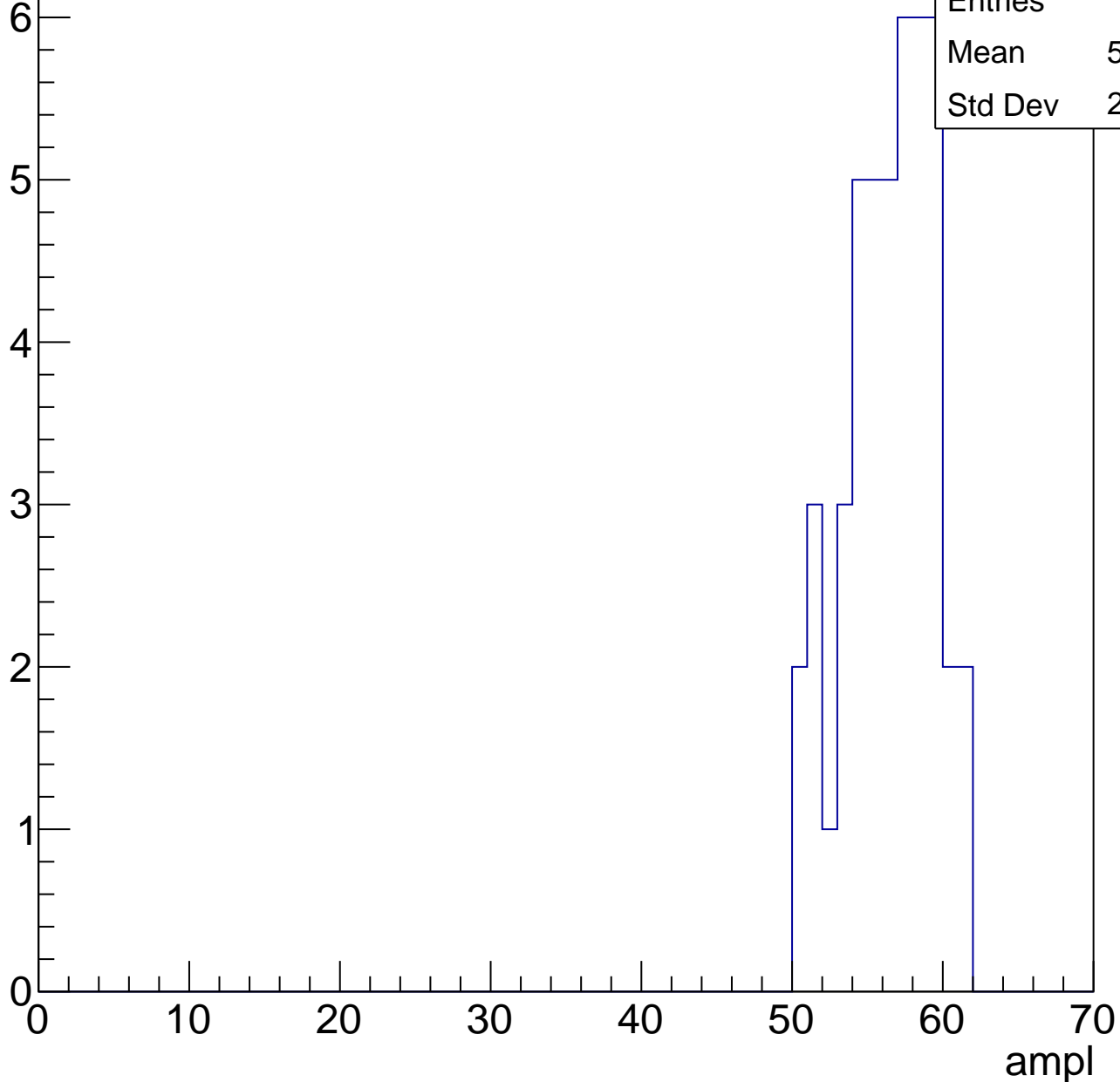
Entries	80
Mean	49.44
Std Dev	3.758



# B1L003S, U26-ch113, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



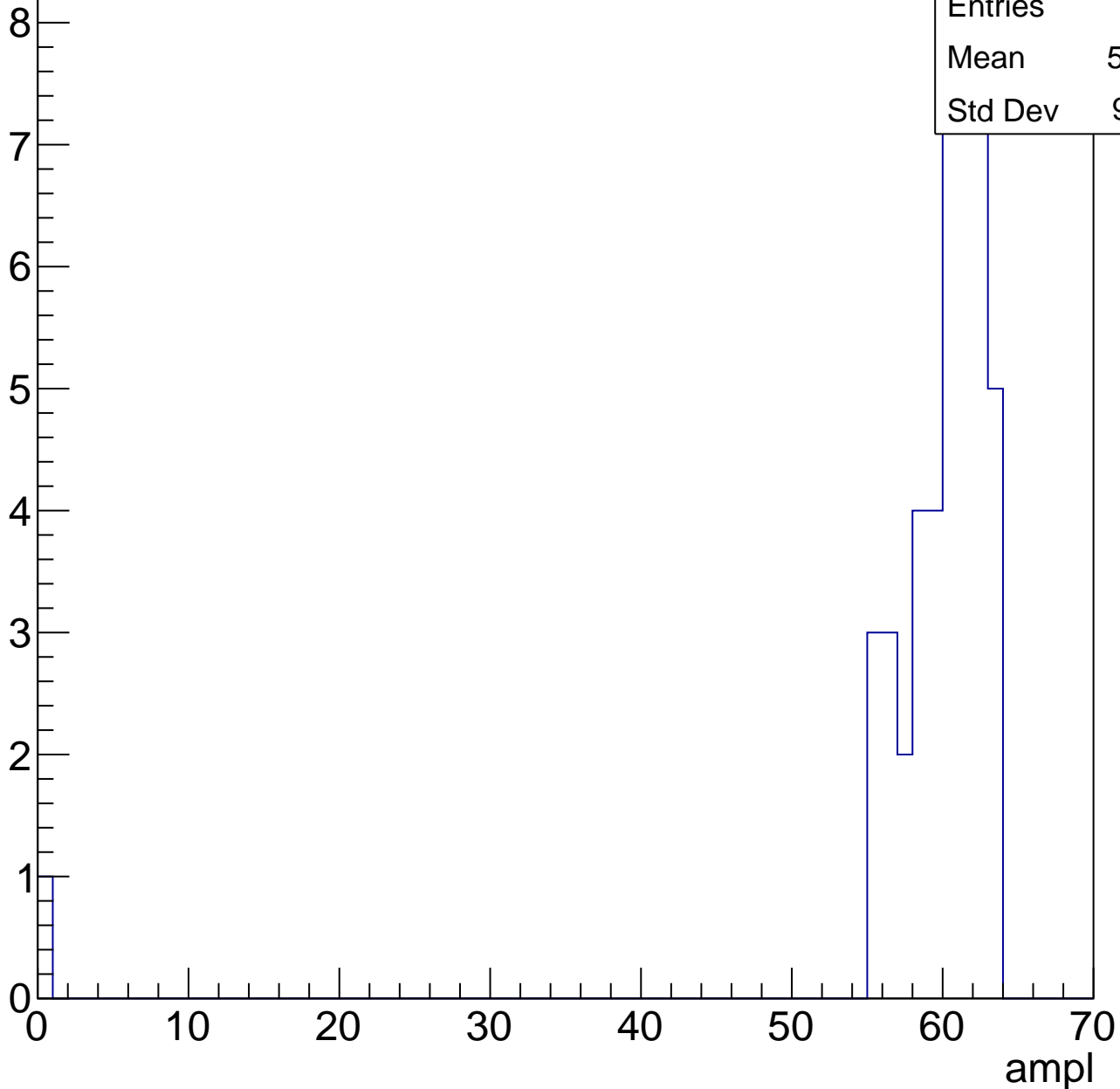
Entries	46
Mean	55.98
Std Dev	2.878

# B1L003S, U26-ch113, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	46
Mean	58.57
Std Dev	9.031

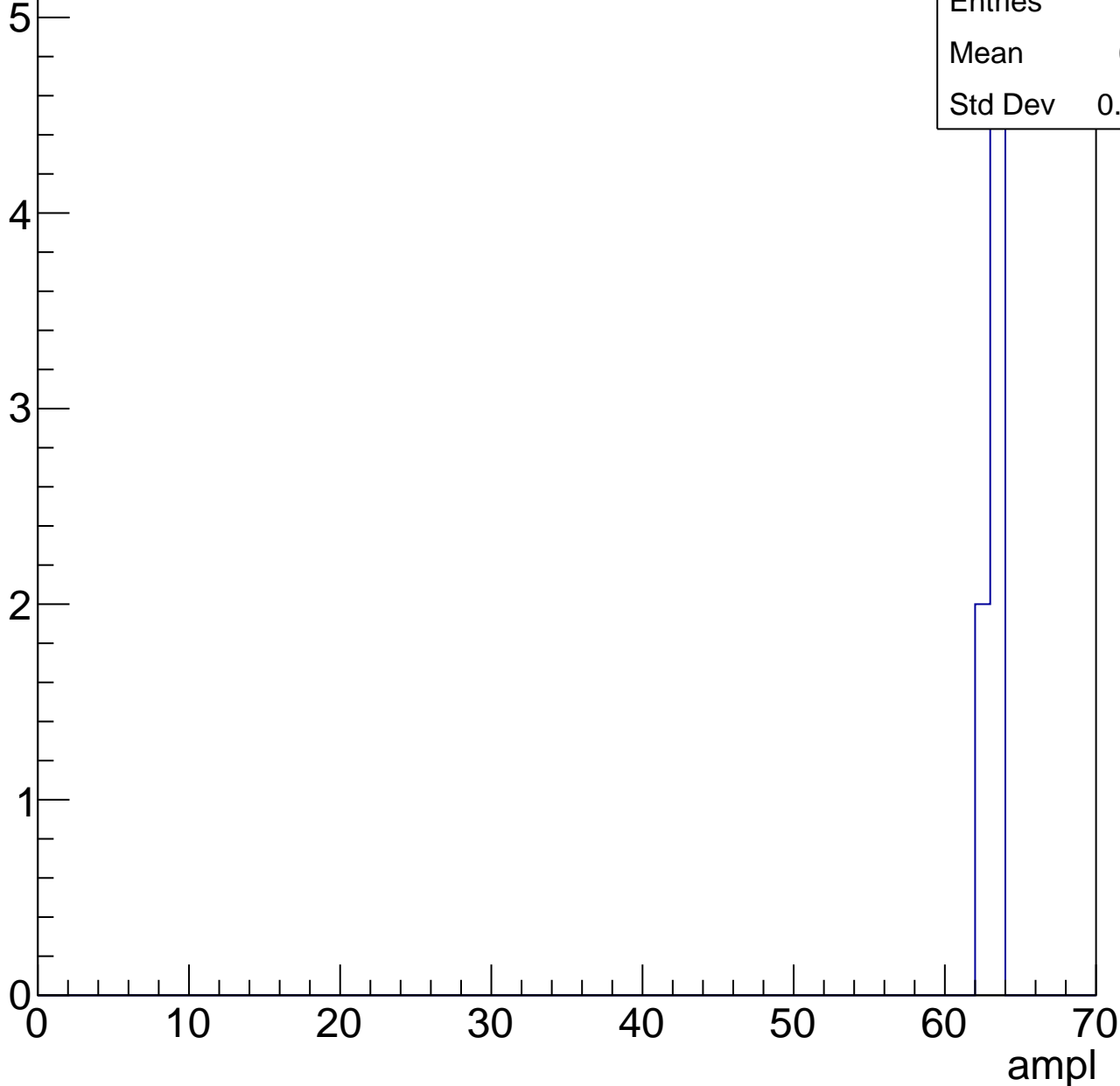


# B1L003S, U26-ch113, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	7
Mean	62.71
Std Dev	0.4518





# B1L003S, U26-ch113, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	22
Std Dev	0

ampl

# B1L003S, U26-ch114, adc0

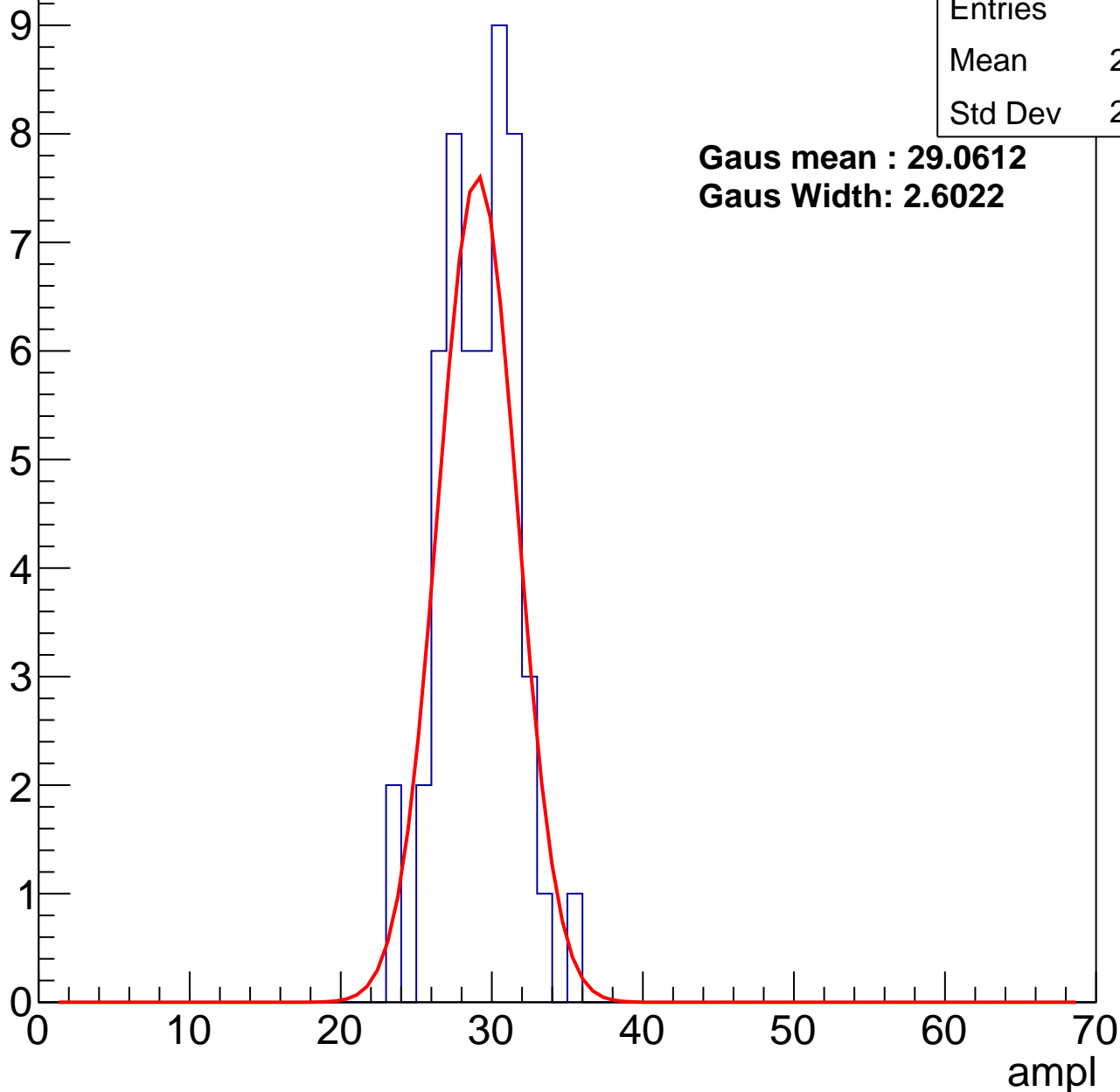
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	52
Mean	28.69
Std Dev	2.446

**Gaus mean : 29.0612**

**Gaus Width: 2.6022**



# B1L003S, U26-ch114, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	72
Mean	35.38
Std Dev	2.884

**Gaus mean : 35.6920**

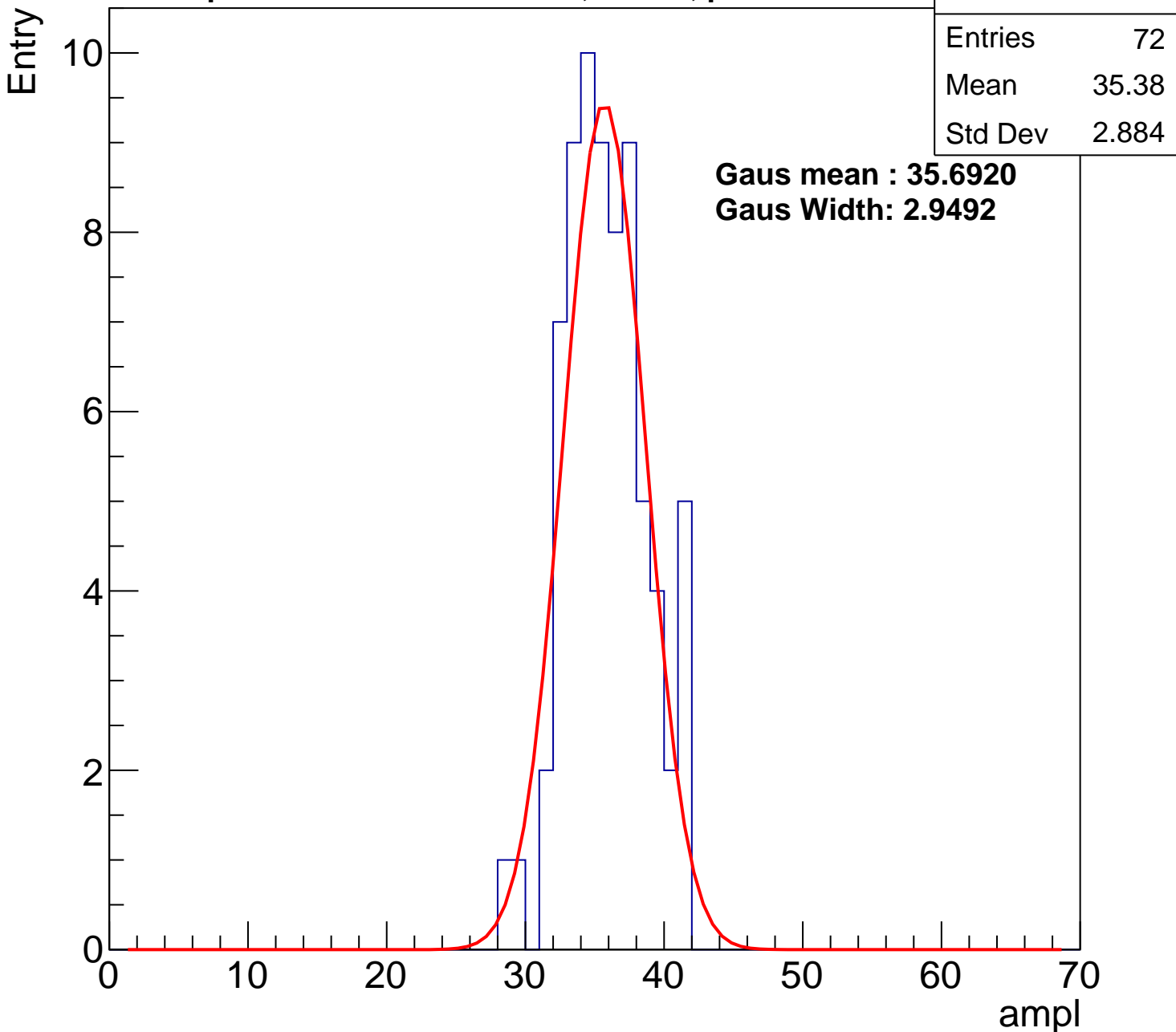
**Gaus Width: 2.9492**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L003S, U26-ch114, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	62
Mean	41.94
Std Dev	2.839

**Gaus mean : 42.7519**

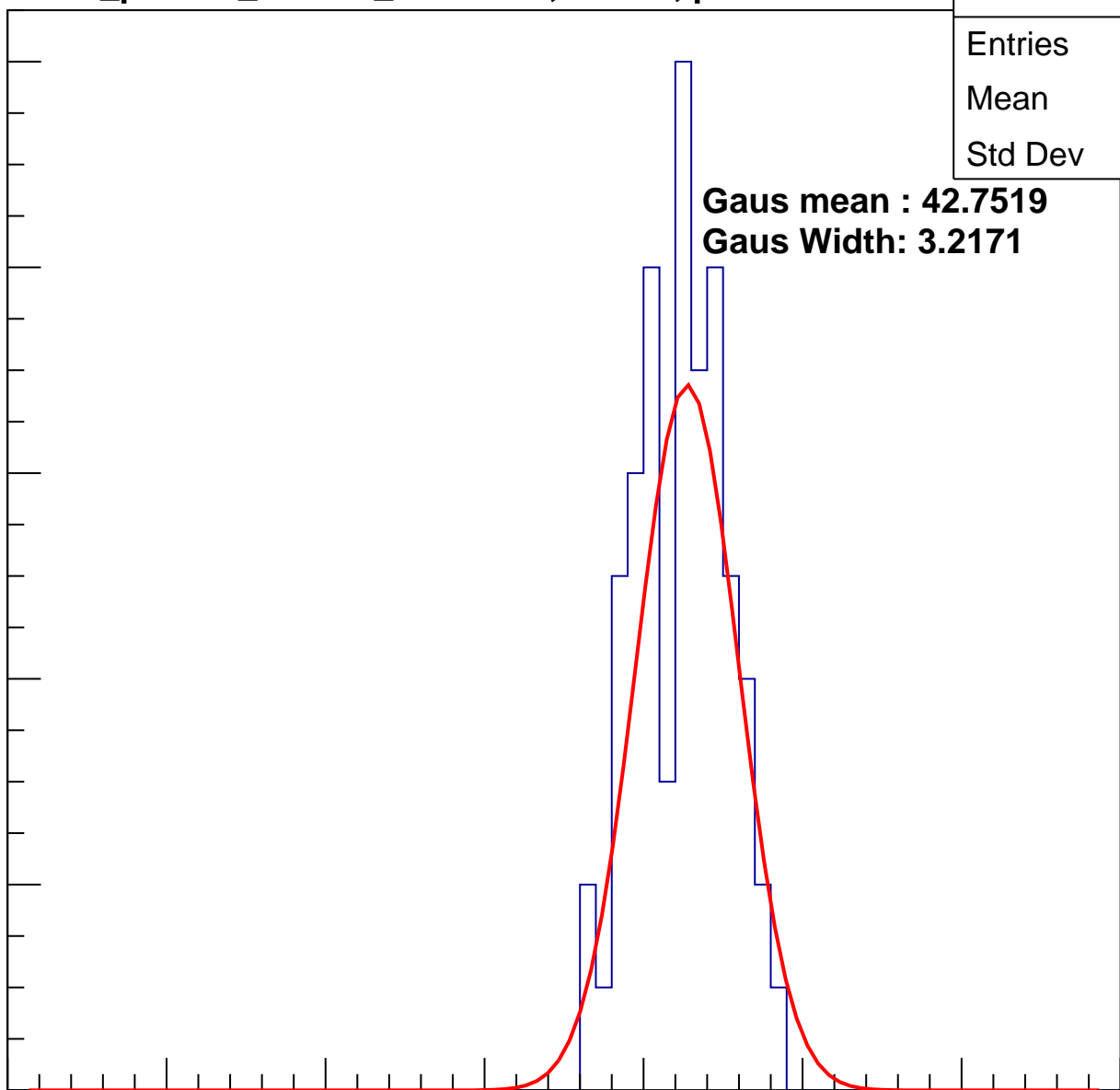
**Gaus Width: 3.2171**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

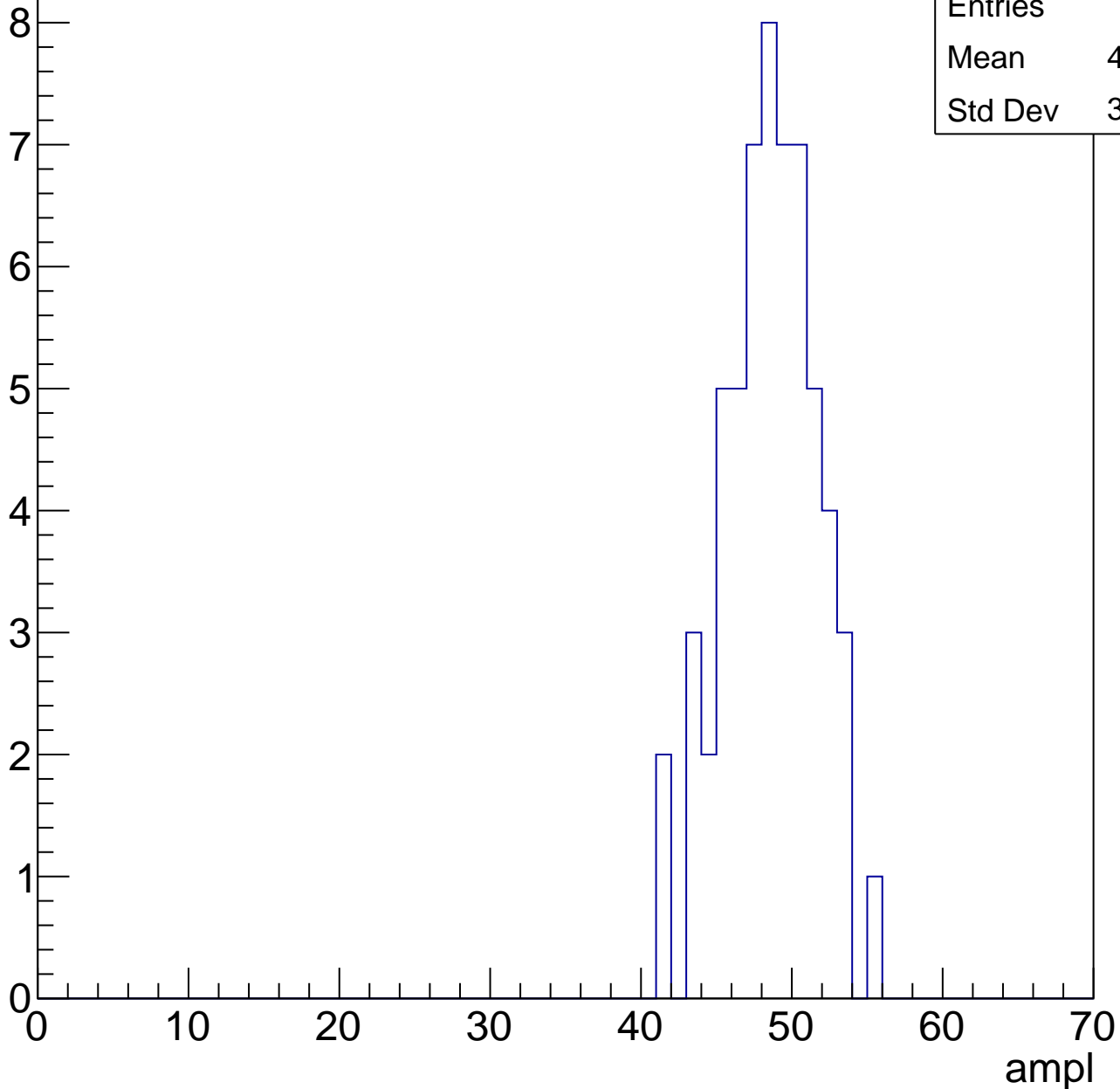


# B1L003S, U26-ch114, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	48.08
Std Dev	3.038

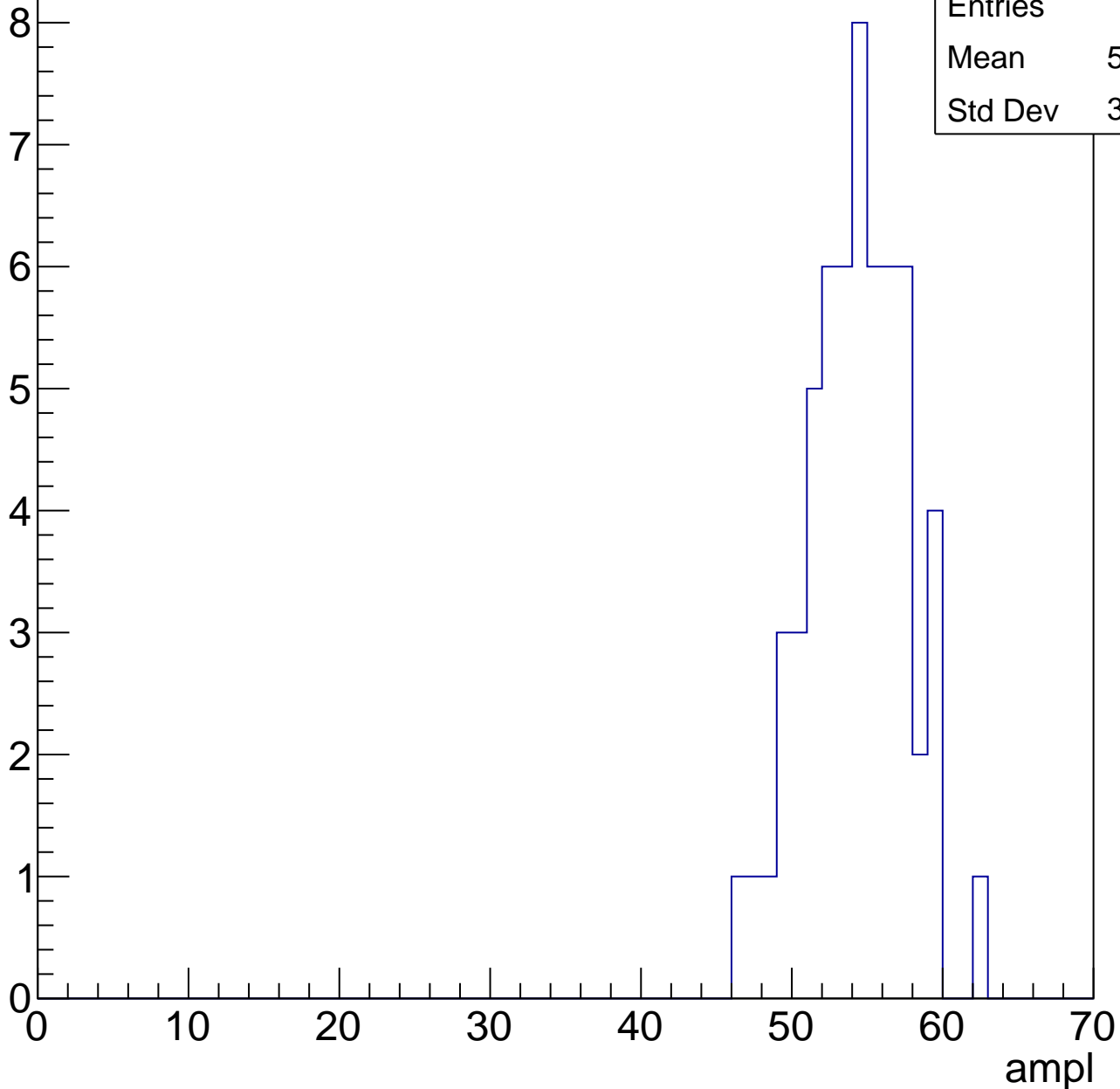


# B1L003S, U26-ch114, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	53.85
Std Dev	3.256

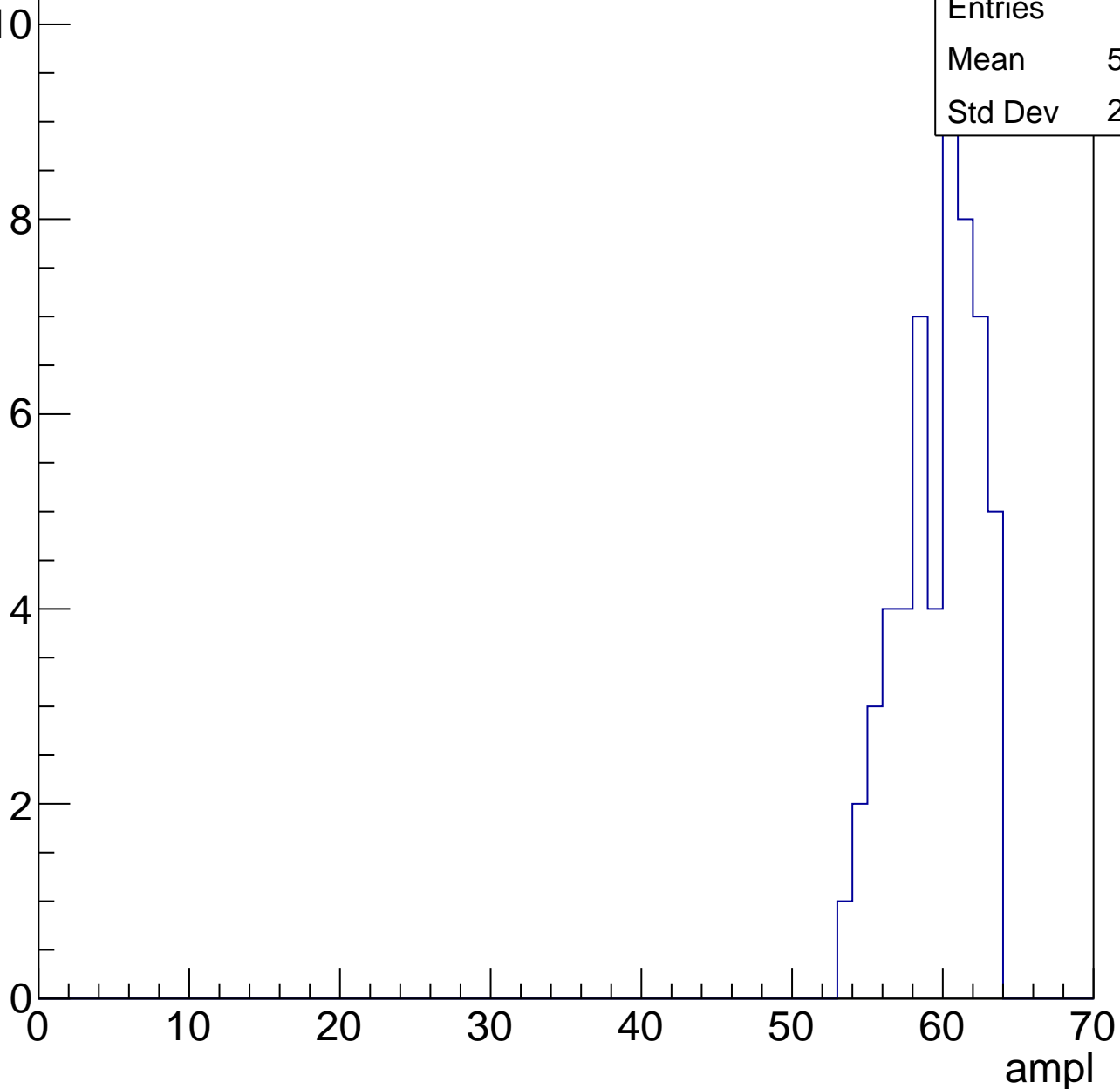


# B1L003S, U26-ch114, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	59.22
Std Dev	2.612

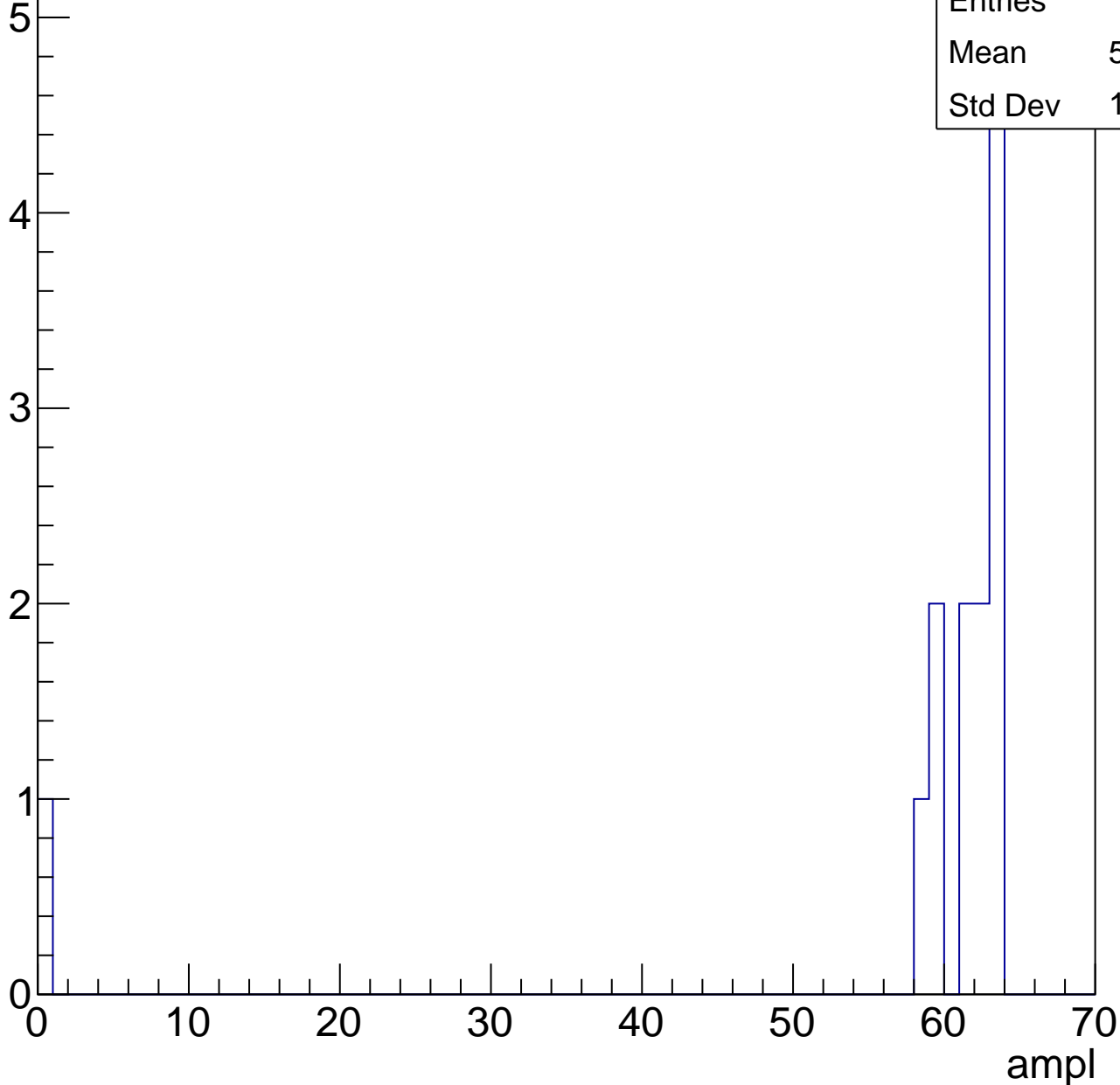


# B1L003S, U26-ch114, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	13
Mean	56.69
Std Dev	16.45





# B1L003S, U26-ch114, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U26-ch115, adc0

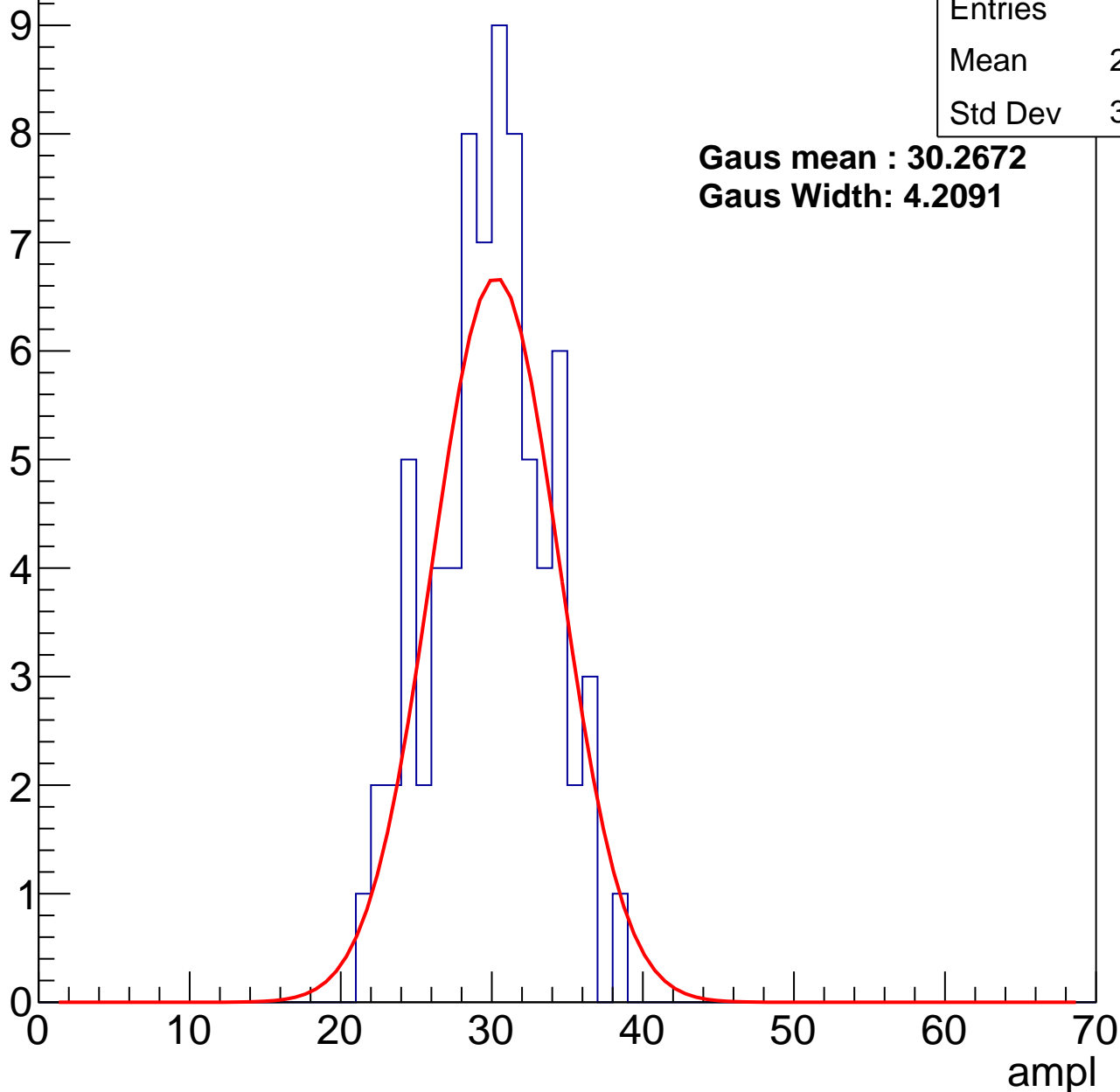
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	73
Mean	29.45
Std Dev	3.767

**Gaus mean : 30.2672**

**Gaus Width: 4.2091**



# B1L003S, U26-ch115, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	70
Mean	36.67
Std Dev	3.289

**Gaus mean : 36.8014**

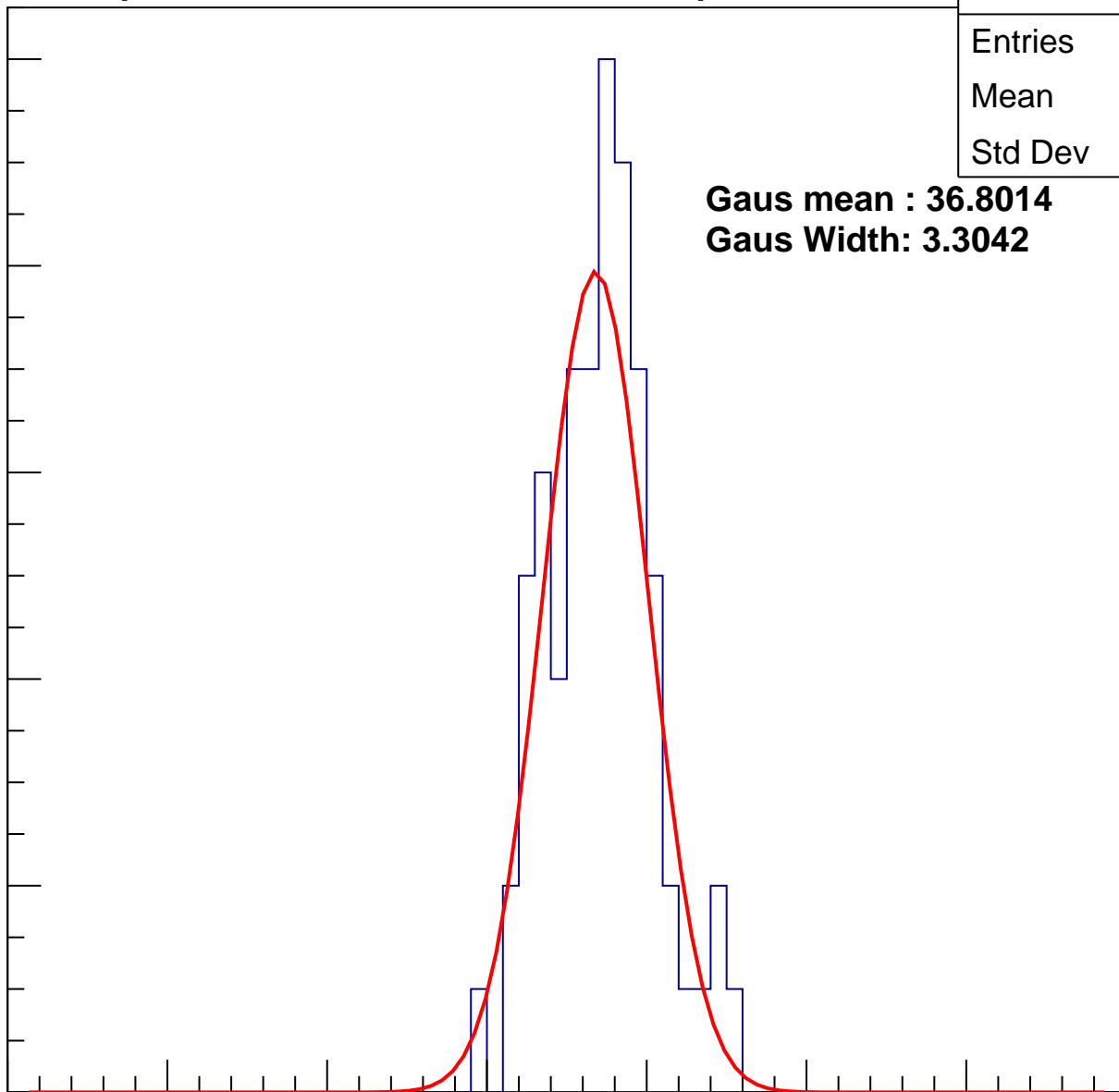
**Gaus Width: 3.3042**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L003S, U26-ch115, adc2

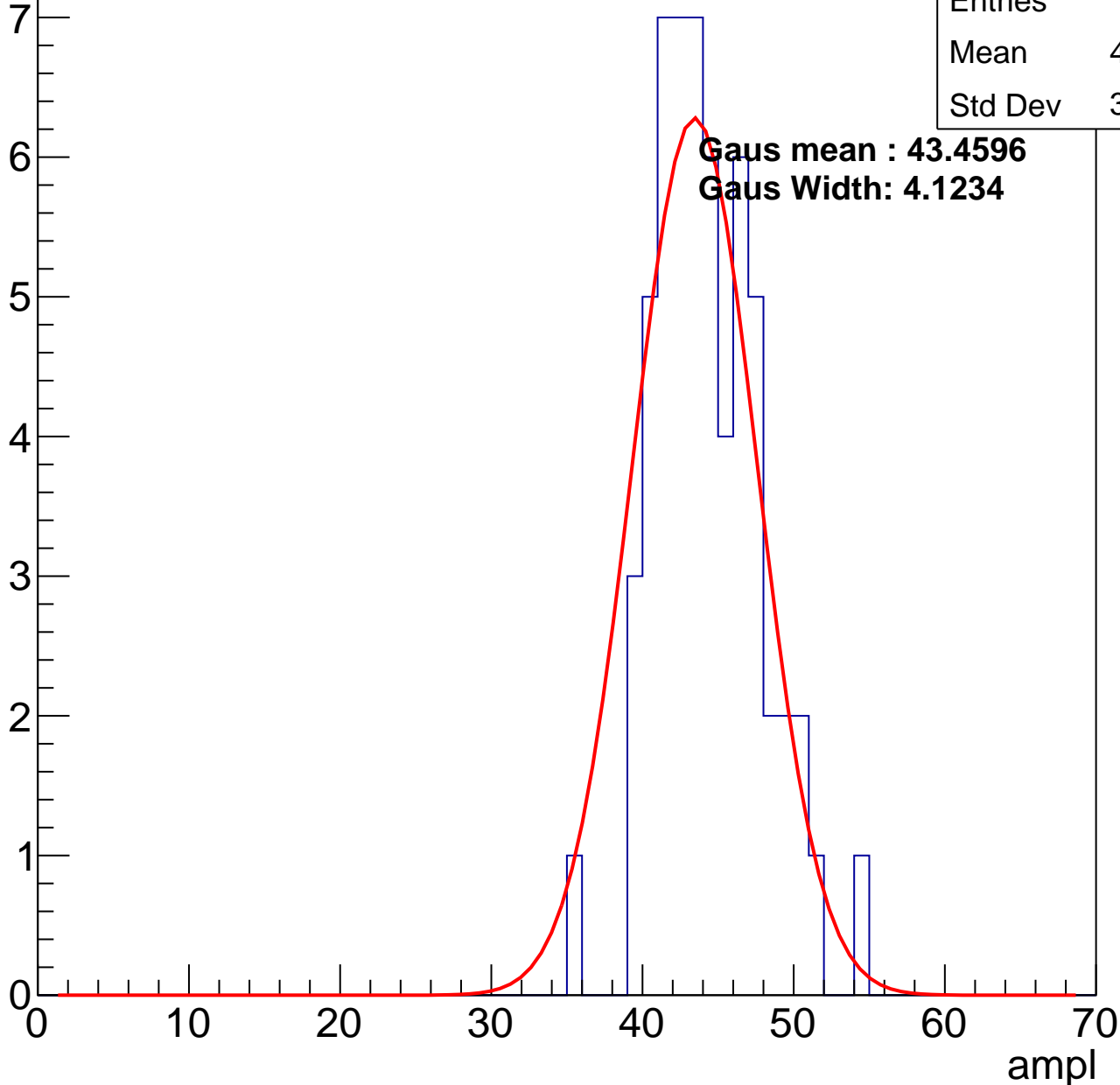
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	43.86
Std Dev	3.466

**Gaus mean : 43.4596**

**Gaus Width: 4.1234**

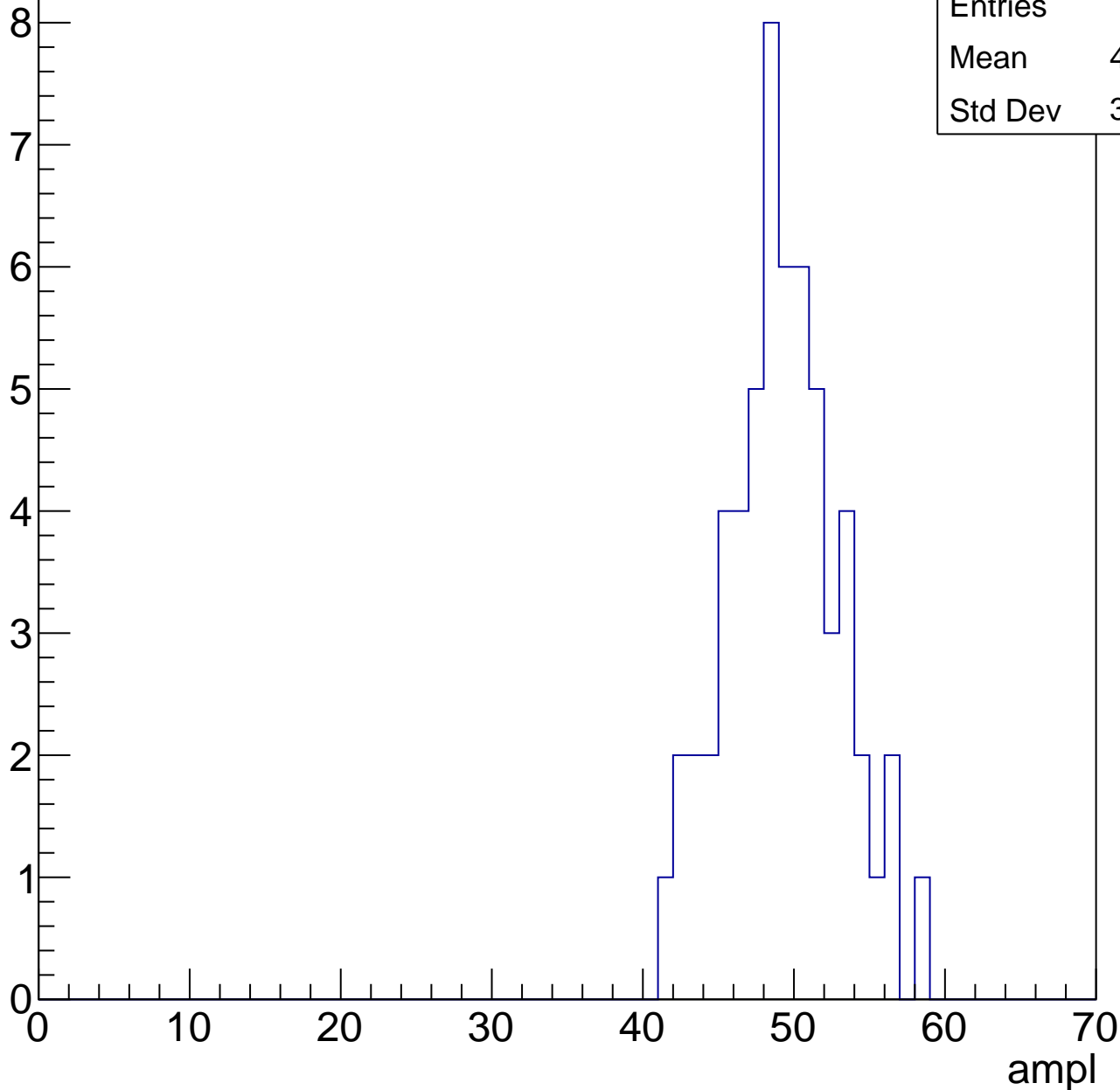


# B1L003S, U26-ch115, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	48.83
Std Dev	3.696

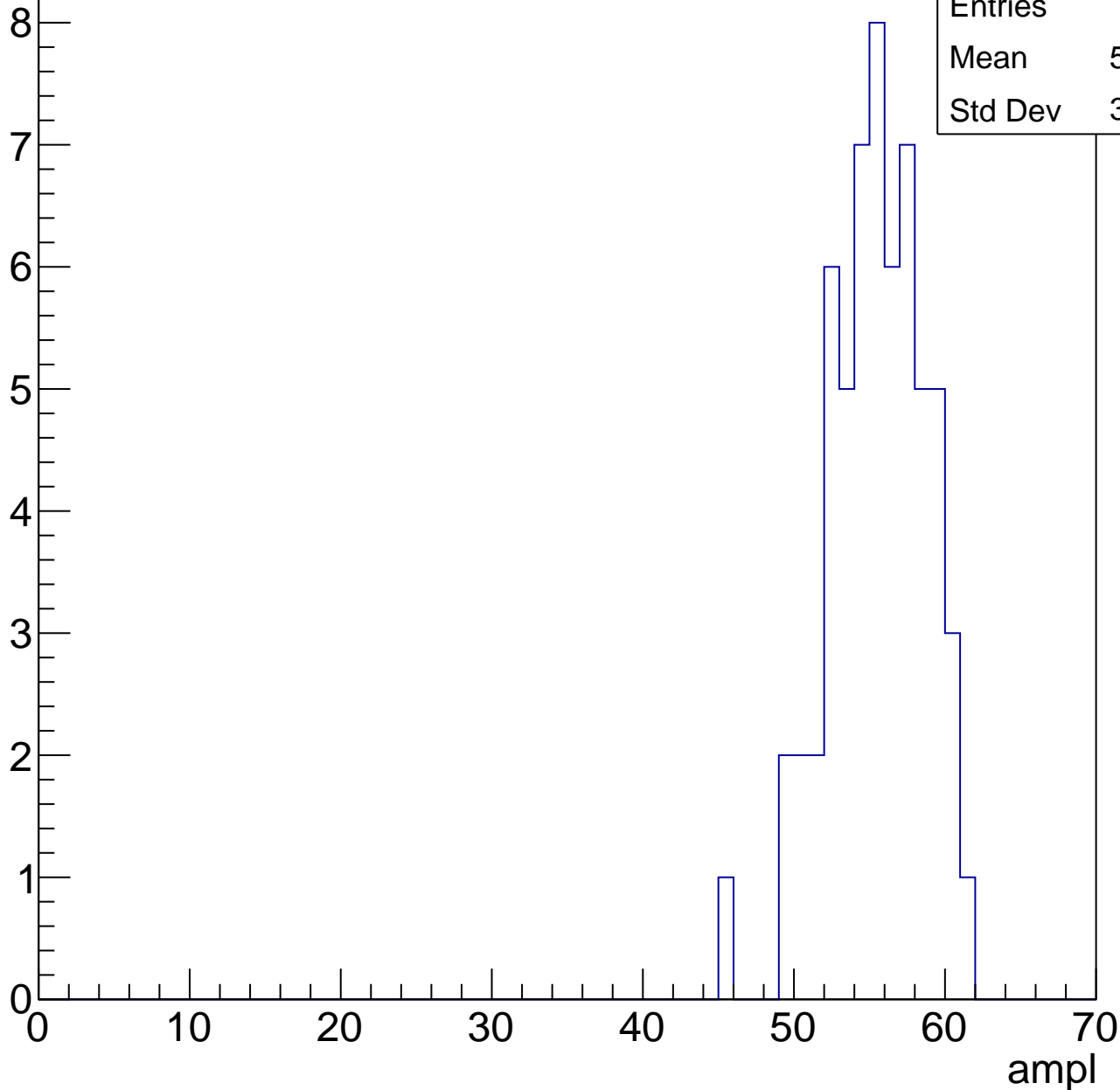


# B1L003S, U26-ch115, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	55.02
Std Dev	3.175

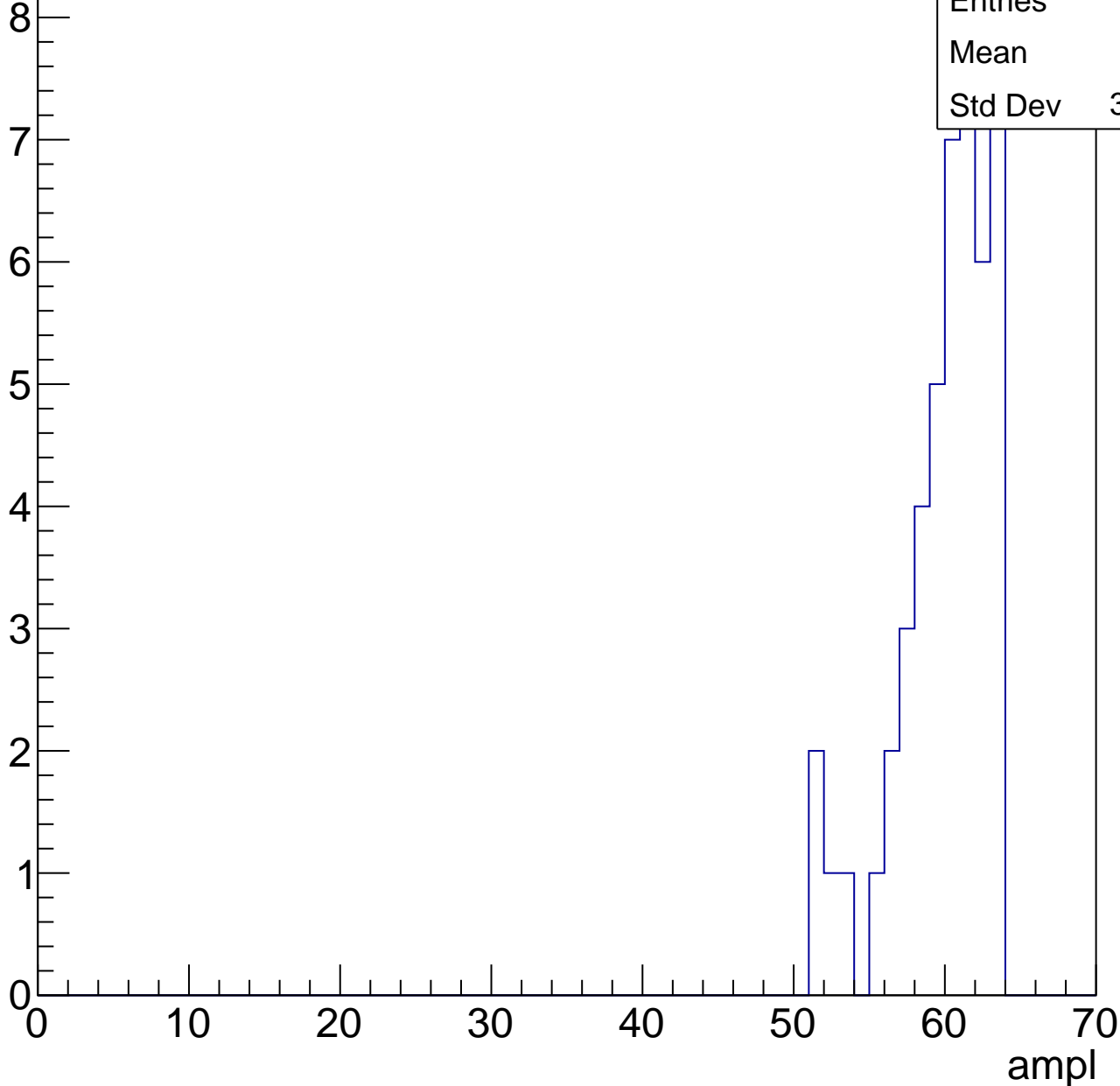


# B1L003S, U26-ch115, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

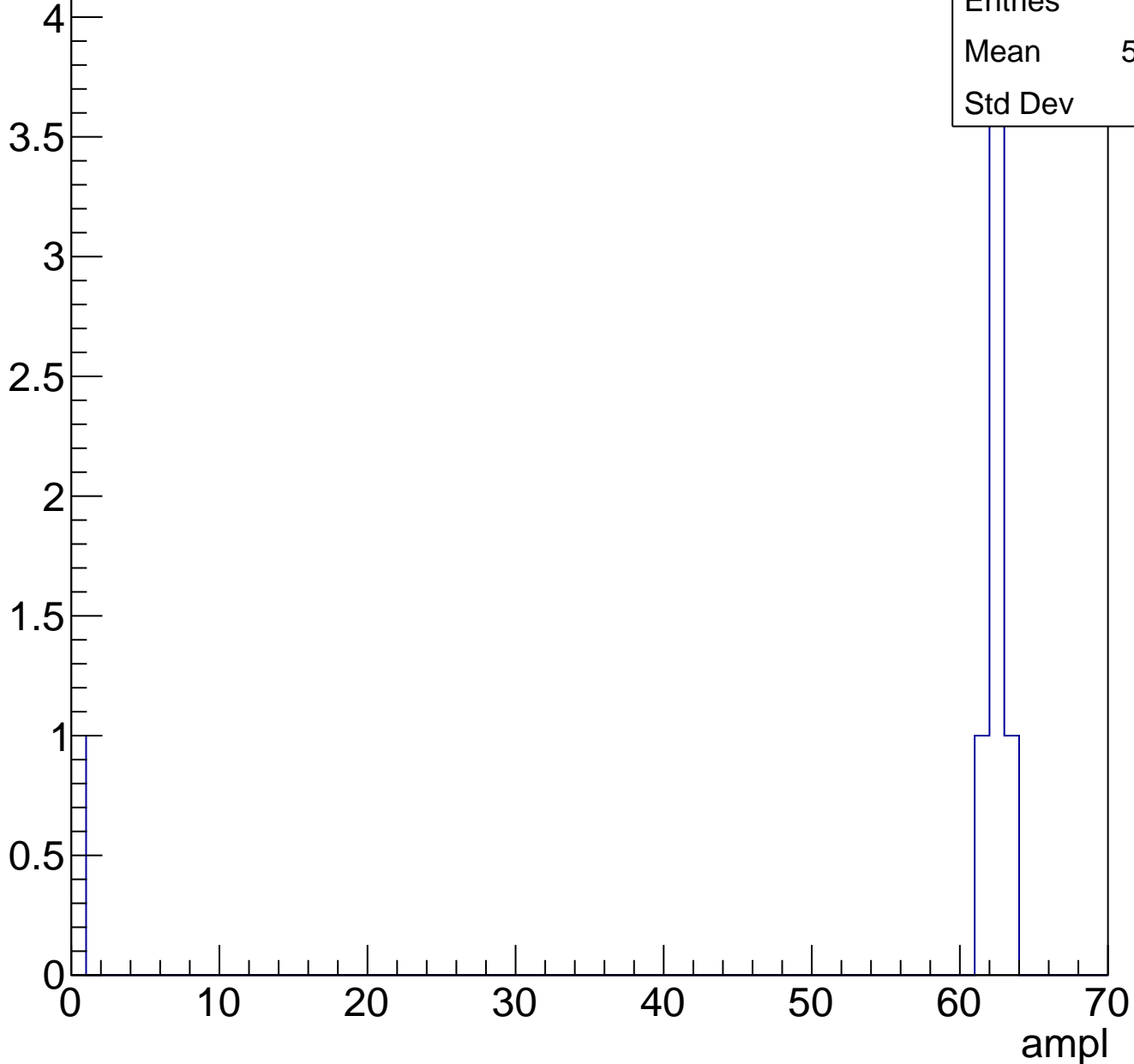
Entries	48
Mean	59.5
Std Dev	3.136



# B1L003S, U26-ch115, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch115, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U26-ch116, adc0

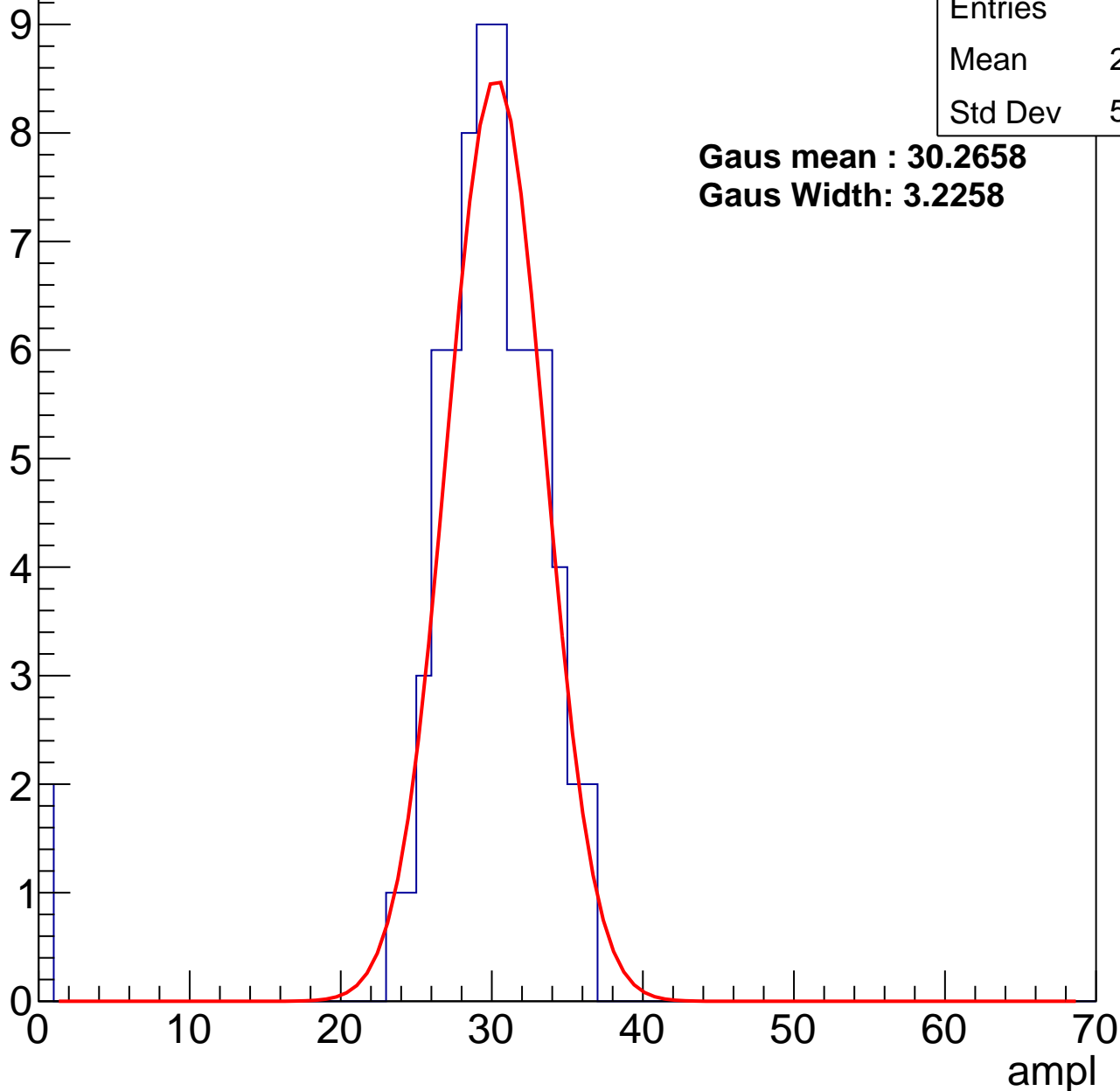
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	71
Mean	28.86
Std Dev	5.727

**Gaus mean : 30.2658**

**Gaus Width: 3.2258**



# B1L003S, U26-ch116, adc1

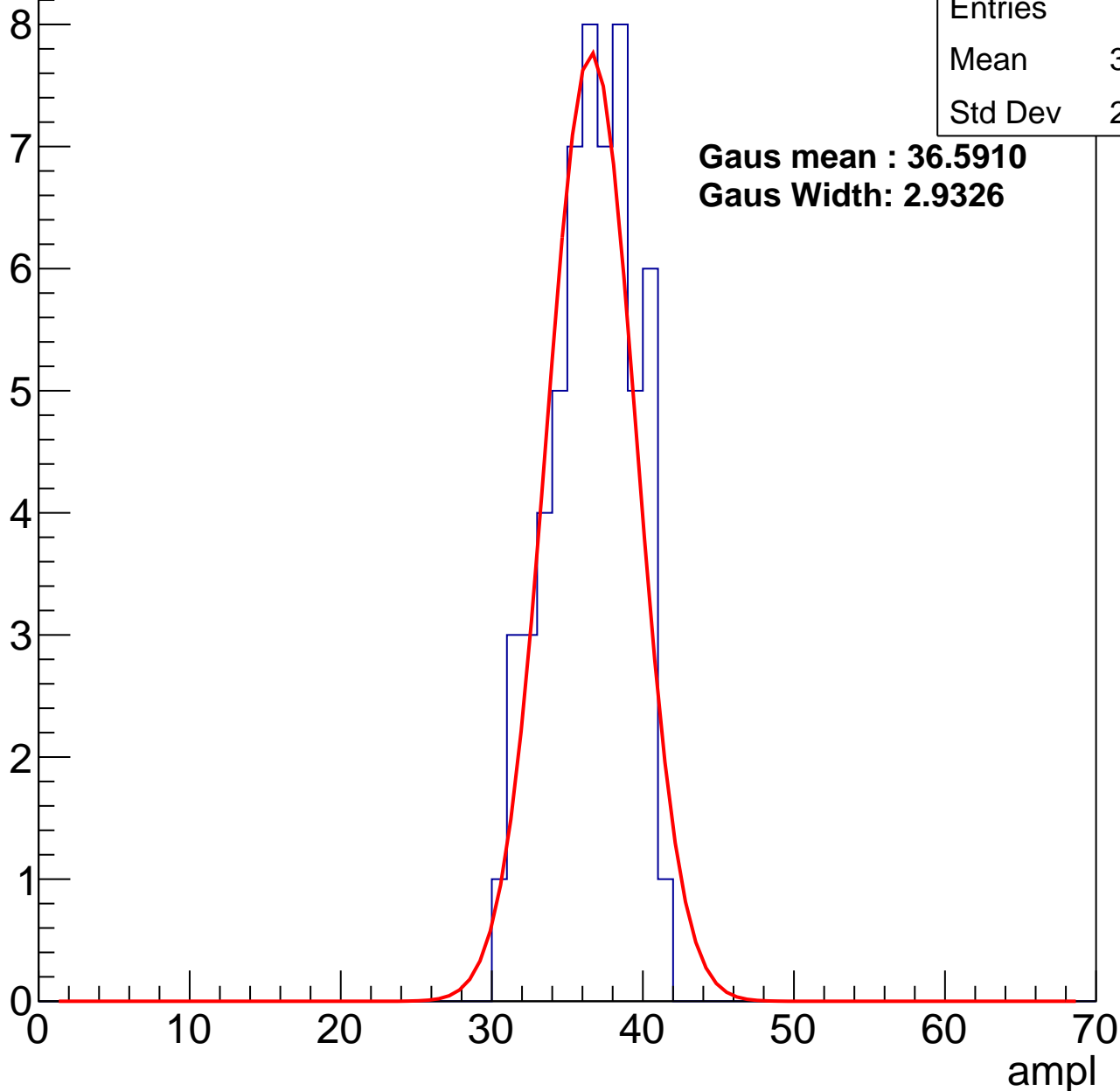
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	36.09
Std Dev	2.712

**Gaus mean : 36.5910**

**Gaus Width: 2.9326**



# B1L003S, U26-ch116, adc2

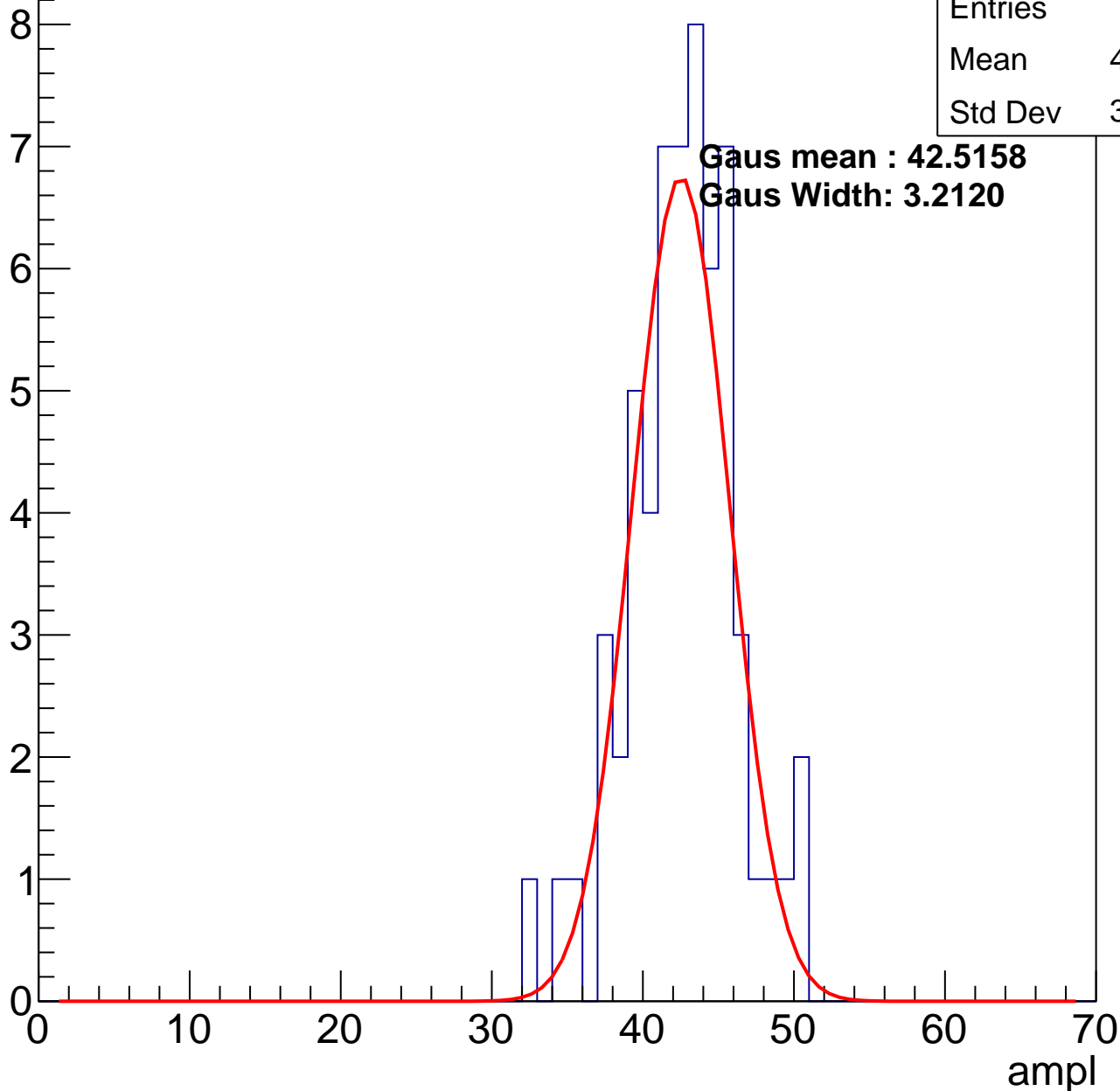
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	42.15
Std Dev	3.577

**Gaus mean : 42.5158**

**Gaus Width: 3.2120**

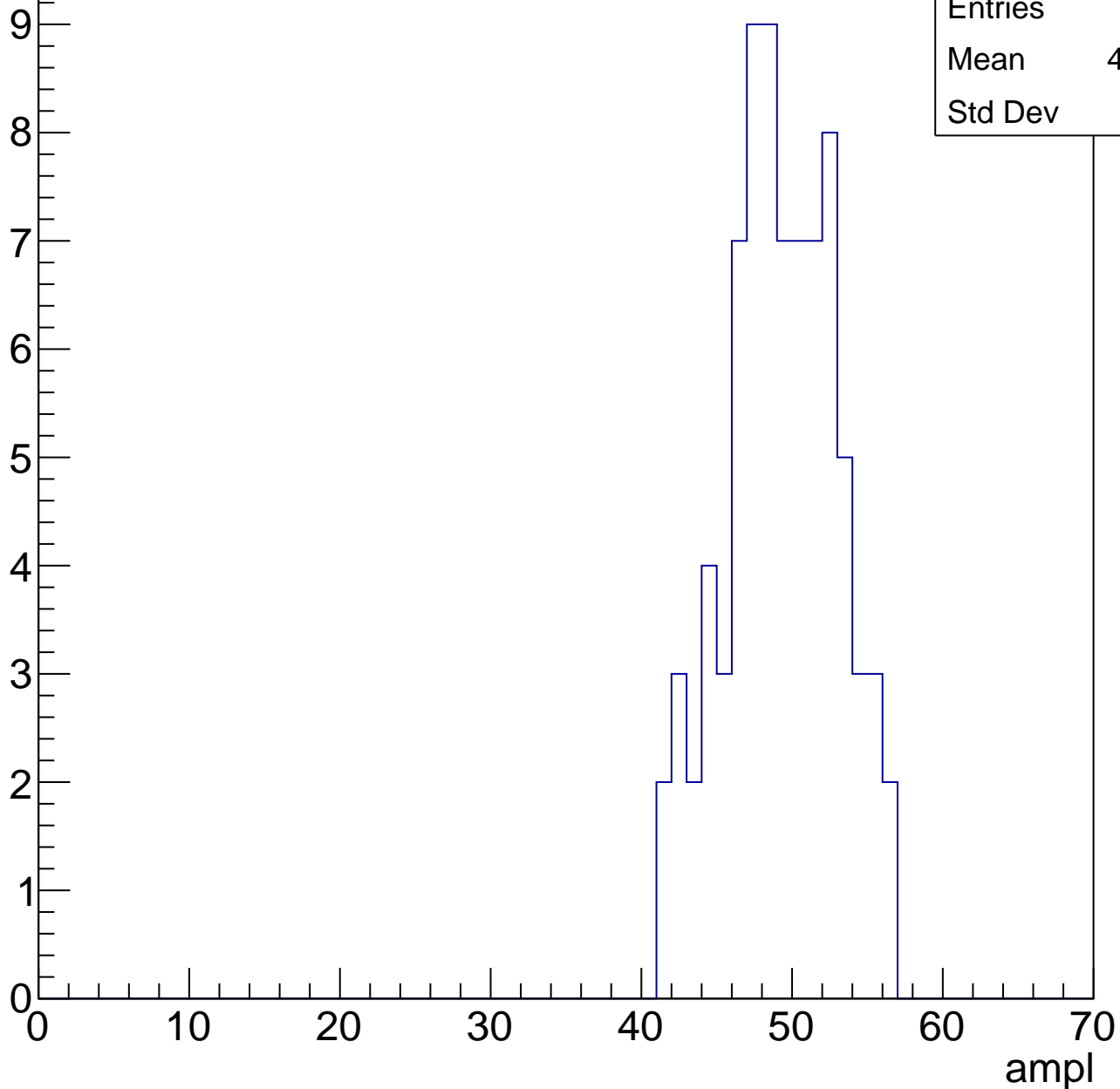


# B1L003S, U26-ch116, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	81
Mean	48.79
Std Dev	3.63

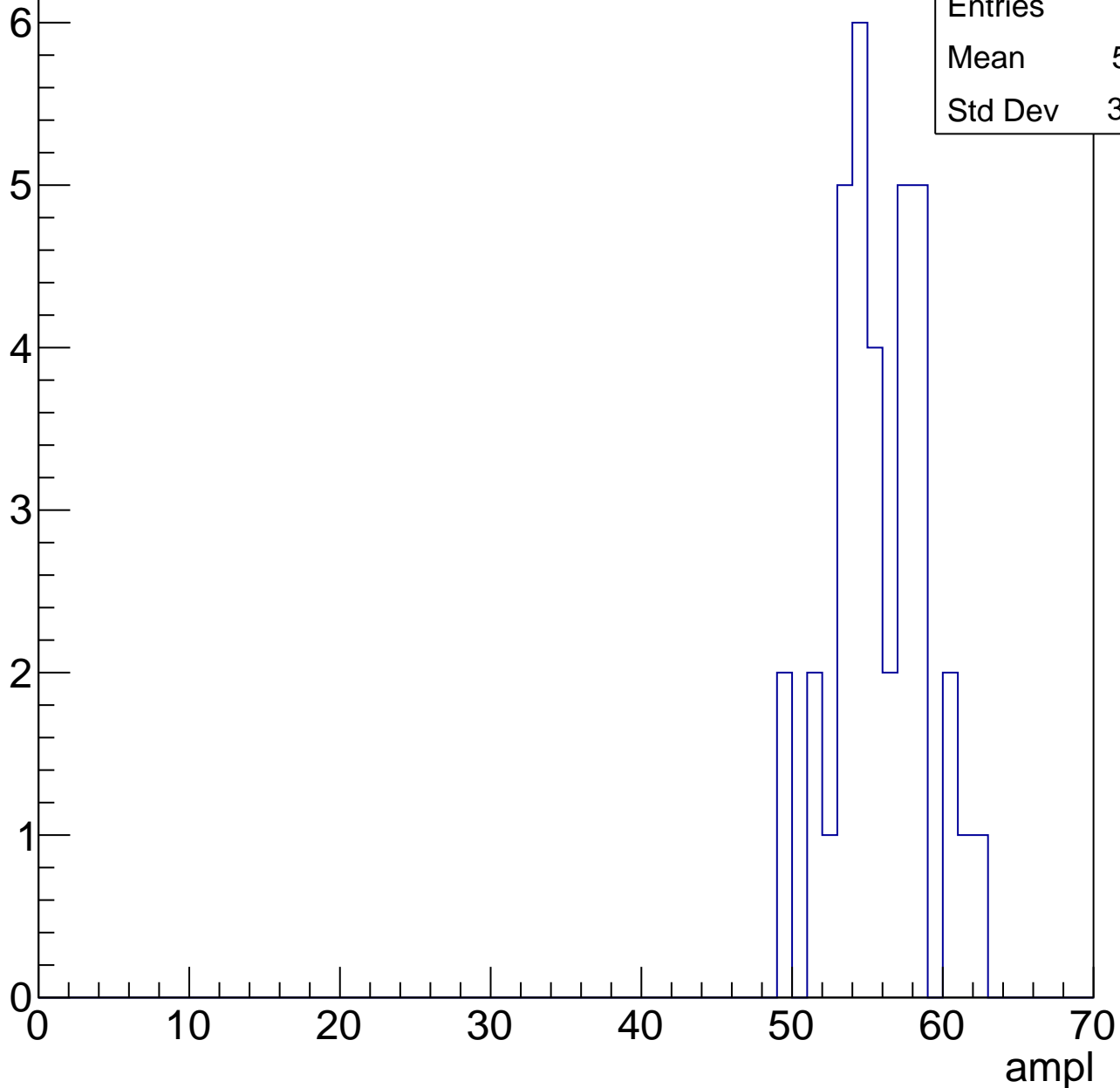


# B1L003S, U26-ch116, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	36
Mean	55.31
Std Dev	3.062

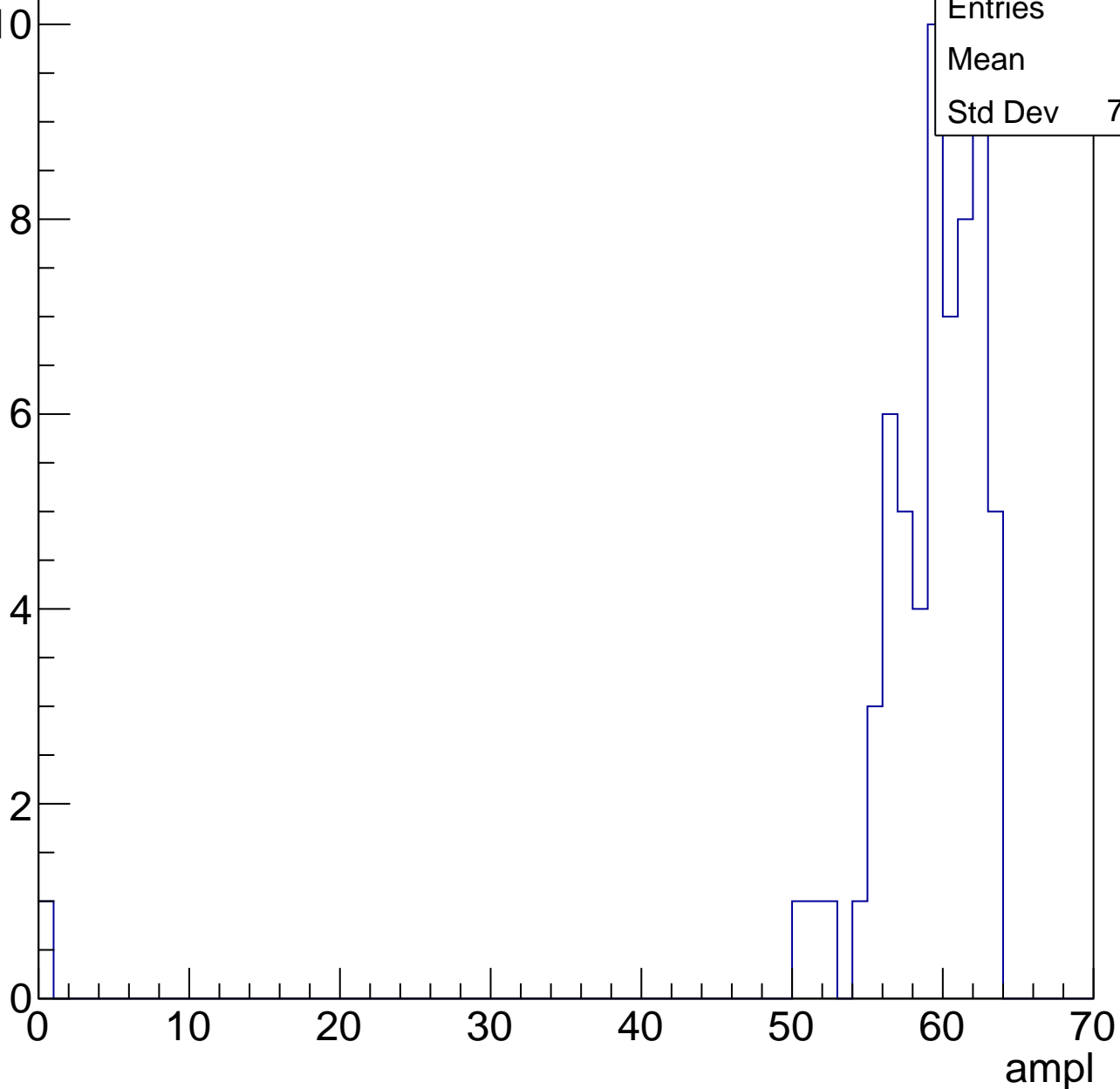


# B1L003S, U26-ch116, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	58
Std Dev	7.996

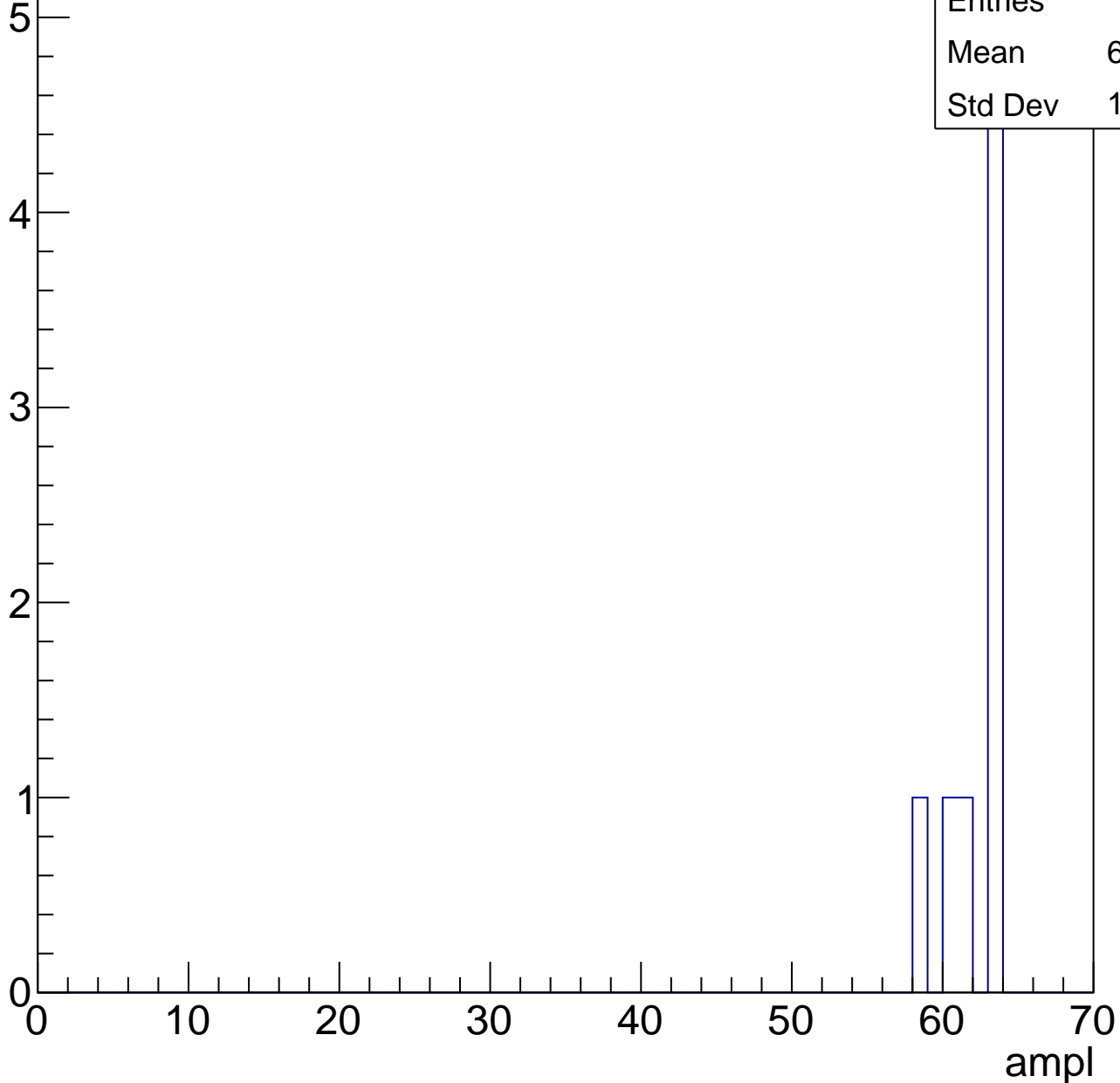


# B1L003S, U26-ch116, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	8
Mean	61.75
Std Dev	1.785

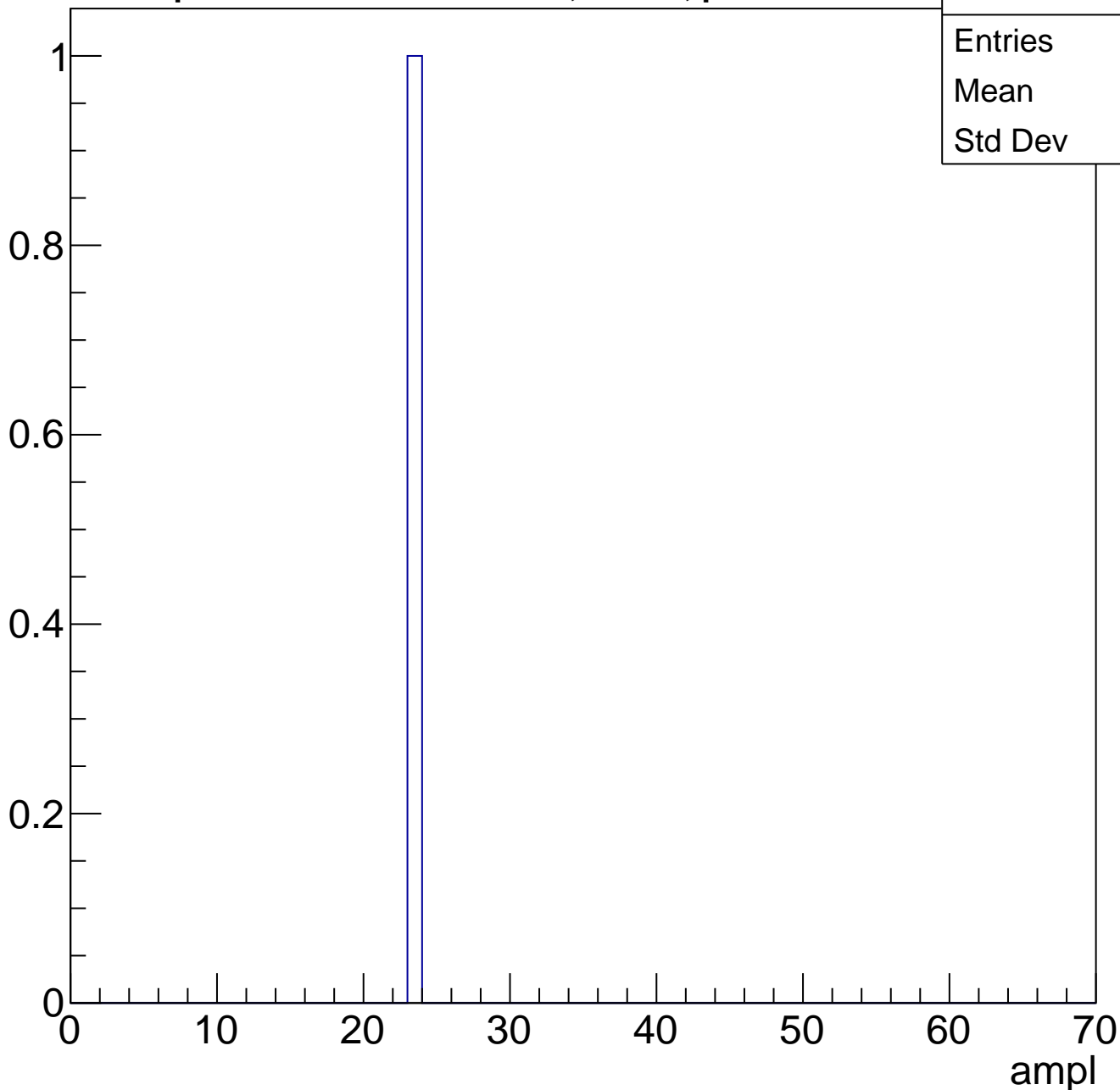




# B1L003S, U26-ch116, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	23
Std Dev	0

# B1L003S, U26-ch117, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	70
Mean	28.39
Std Dev	4.897

**Gaus mean : 29.4194**

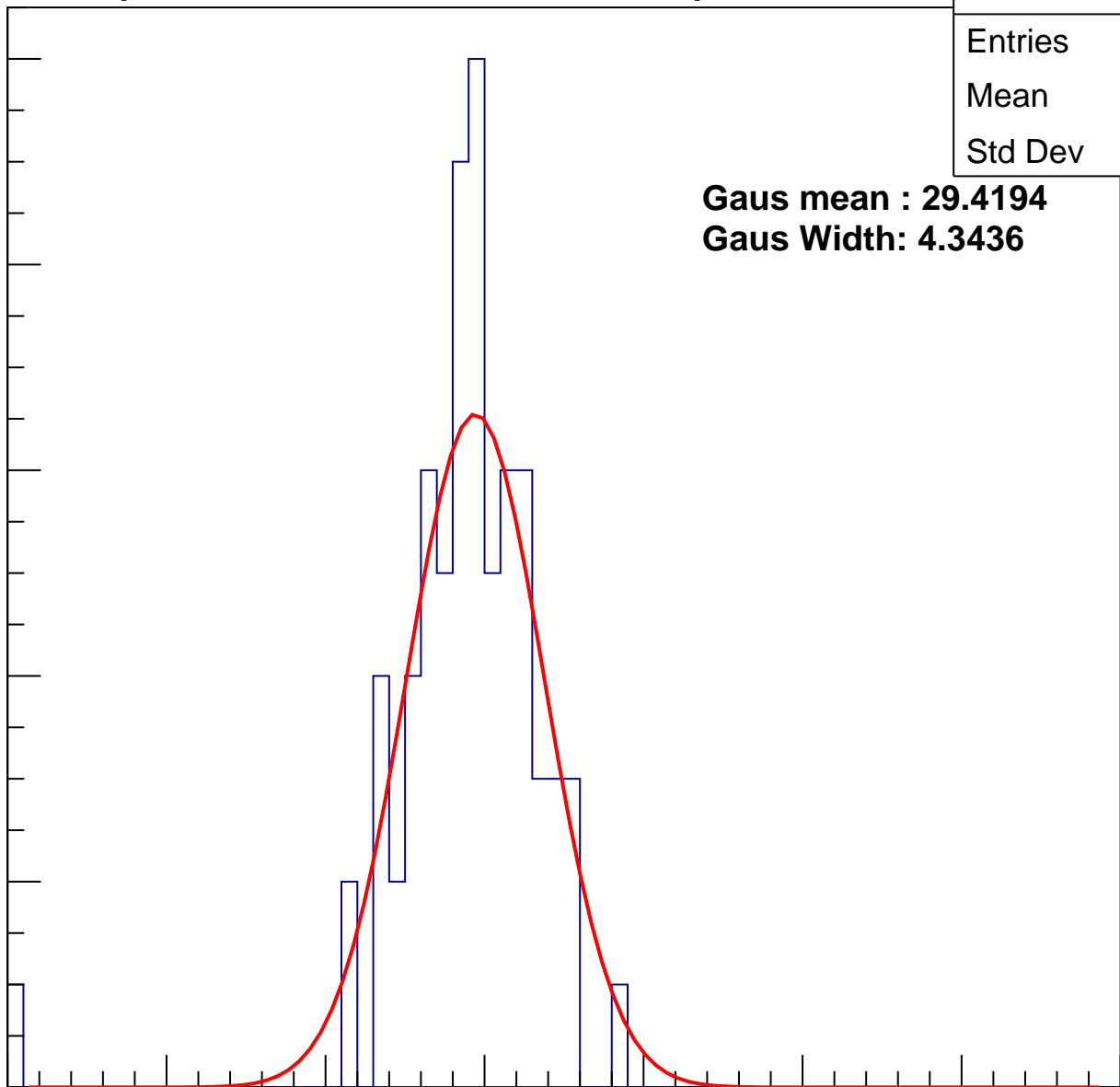
**Gaus Width: 4.3436**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U26-ch117, adc1

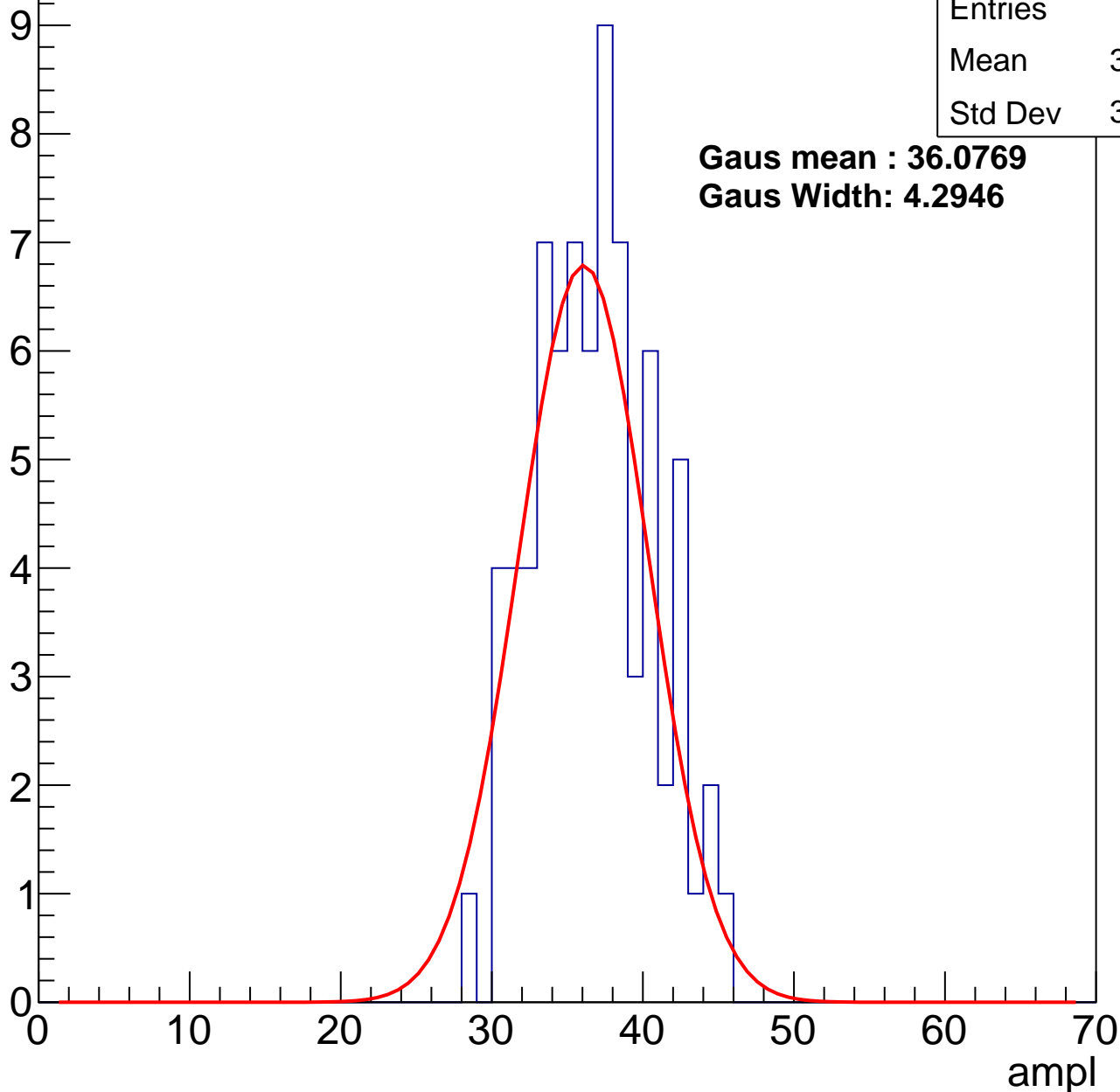
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	75
Mean	36.27
Std Dev	3.845

**Gaus mean : 36.0769**

**Gaus Width: 4.2946**



# B1L003S, U26-ch117, adc2

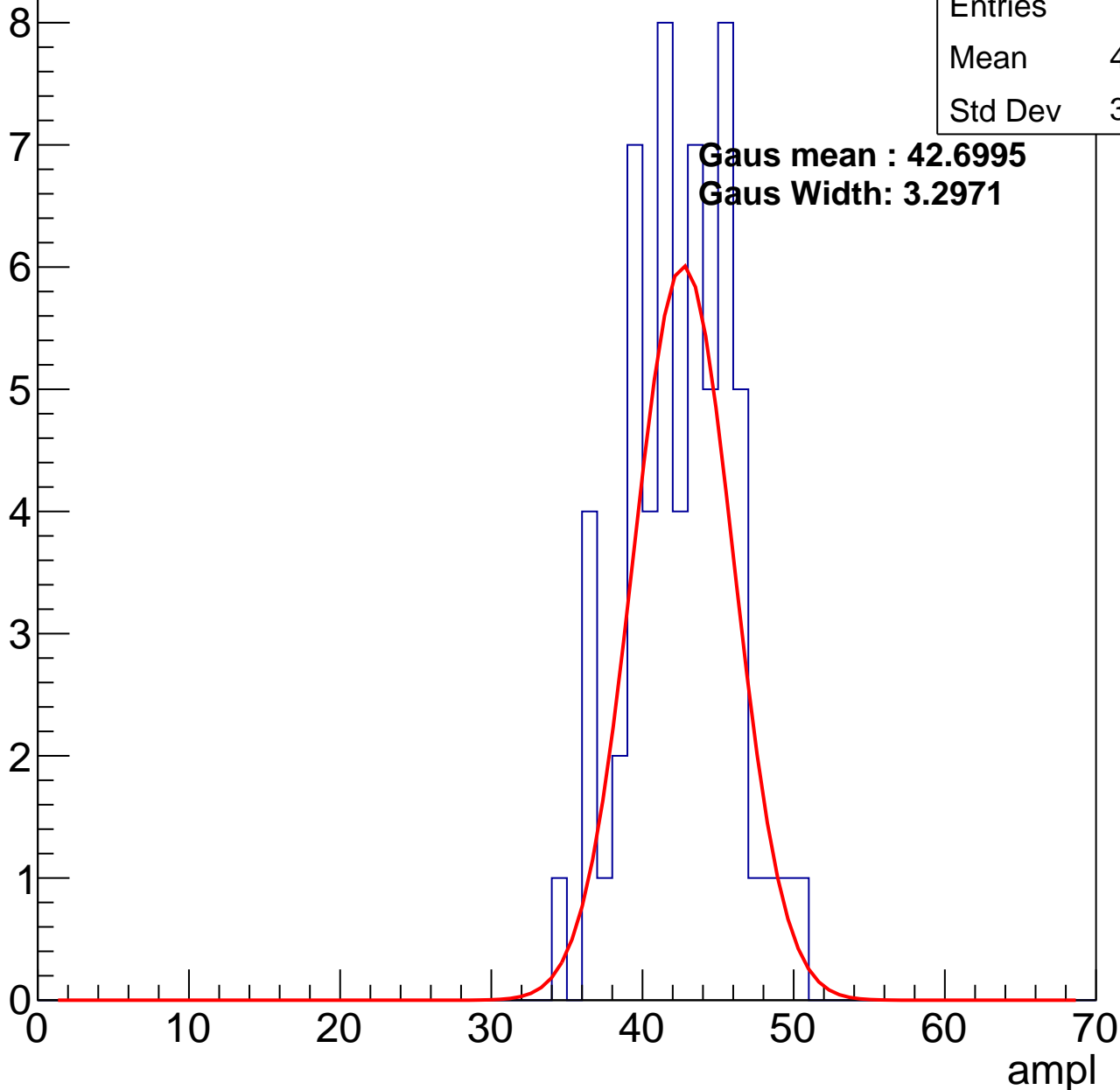
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	42.08
Std Dev	3.427

**Gaus mean : 42.6995**

**Gaus Width: 3.2971**

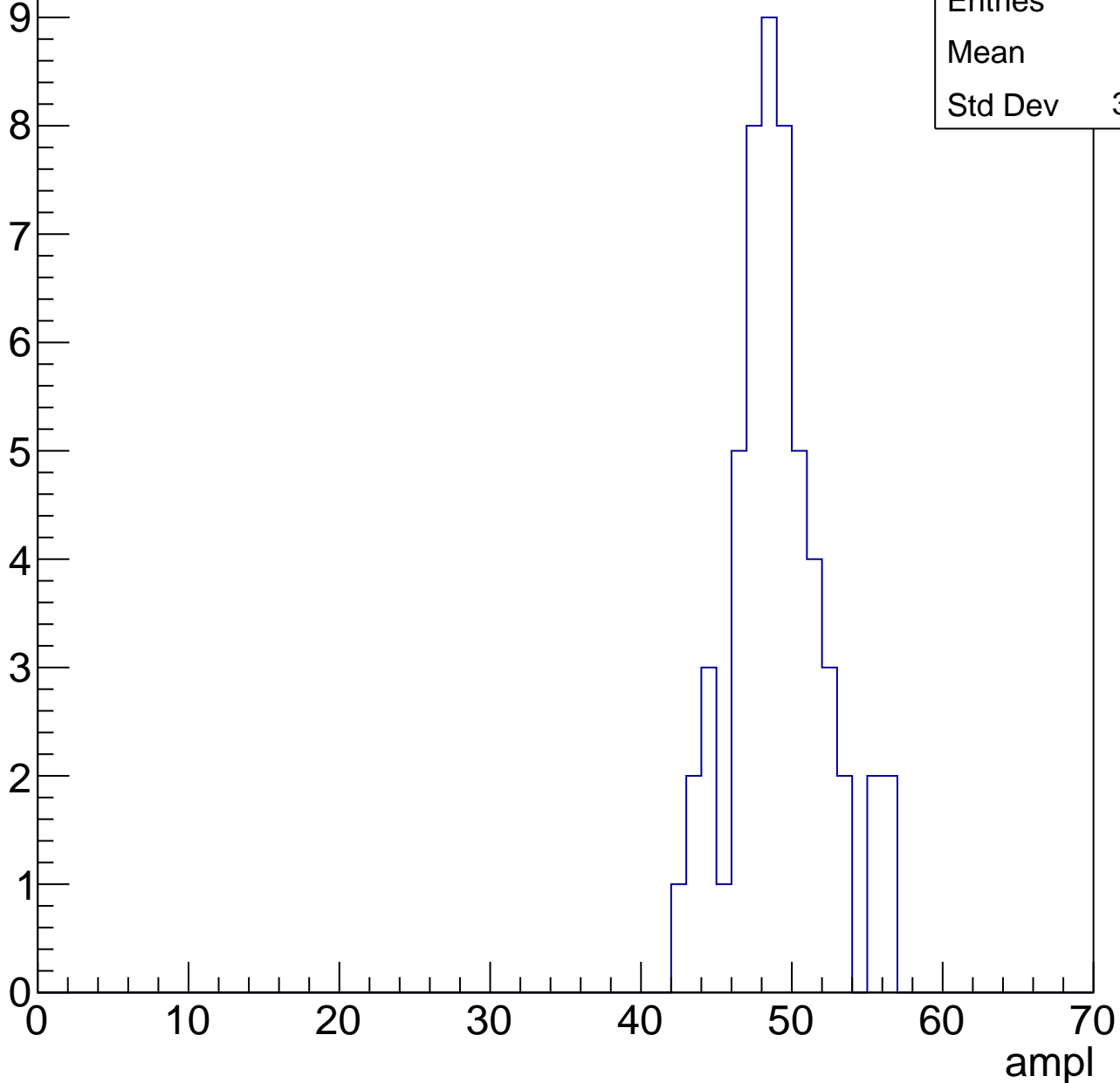


# B1L003S, U26-ch117, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	48.6
Std Dev	3.131

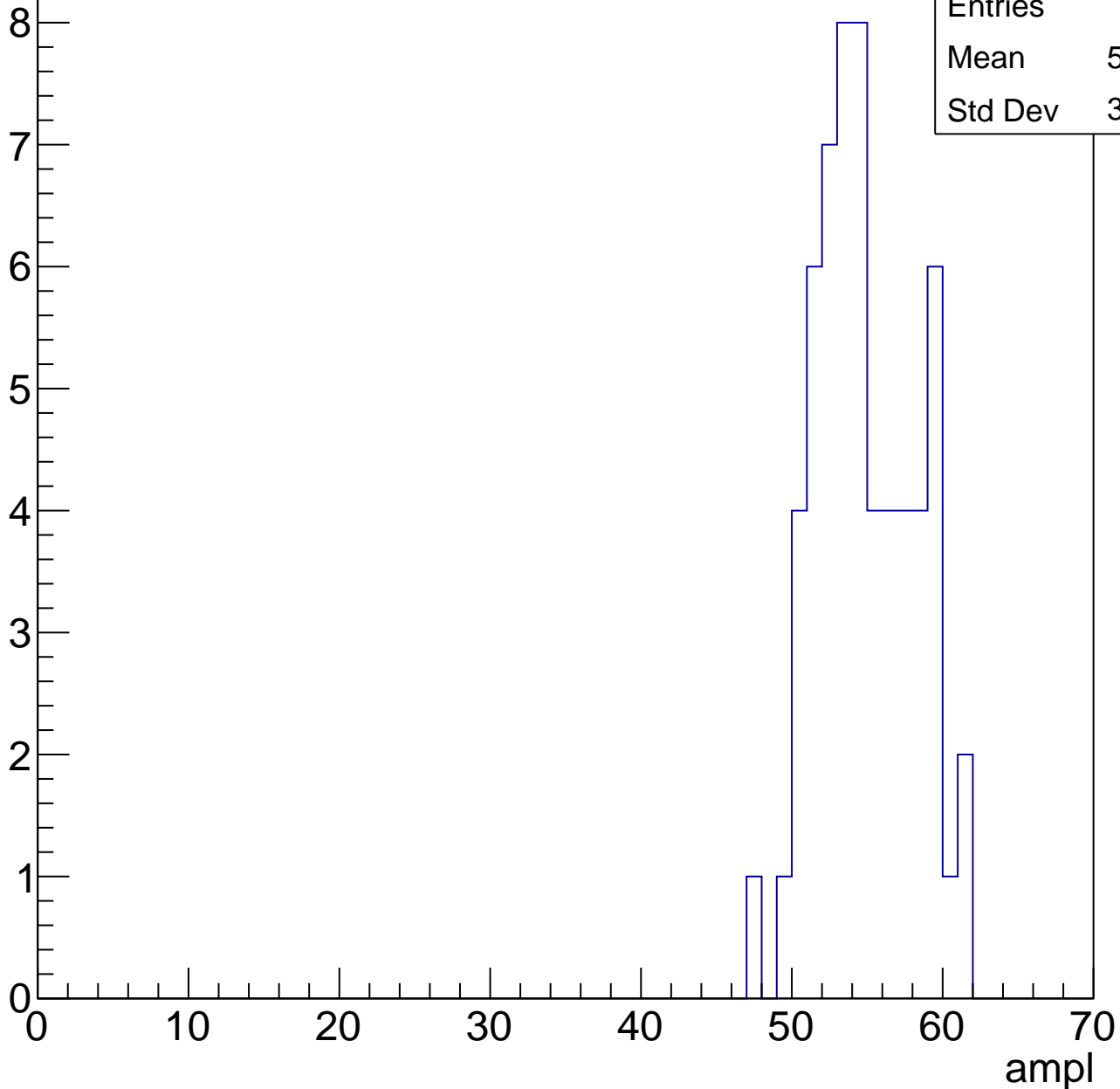


# B1L003S, U26-ch117, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	54.37
Std Dev	3.225



# B1L003S, U26-ch117, adc5

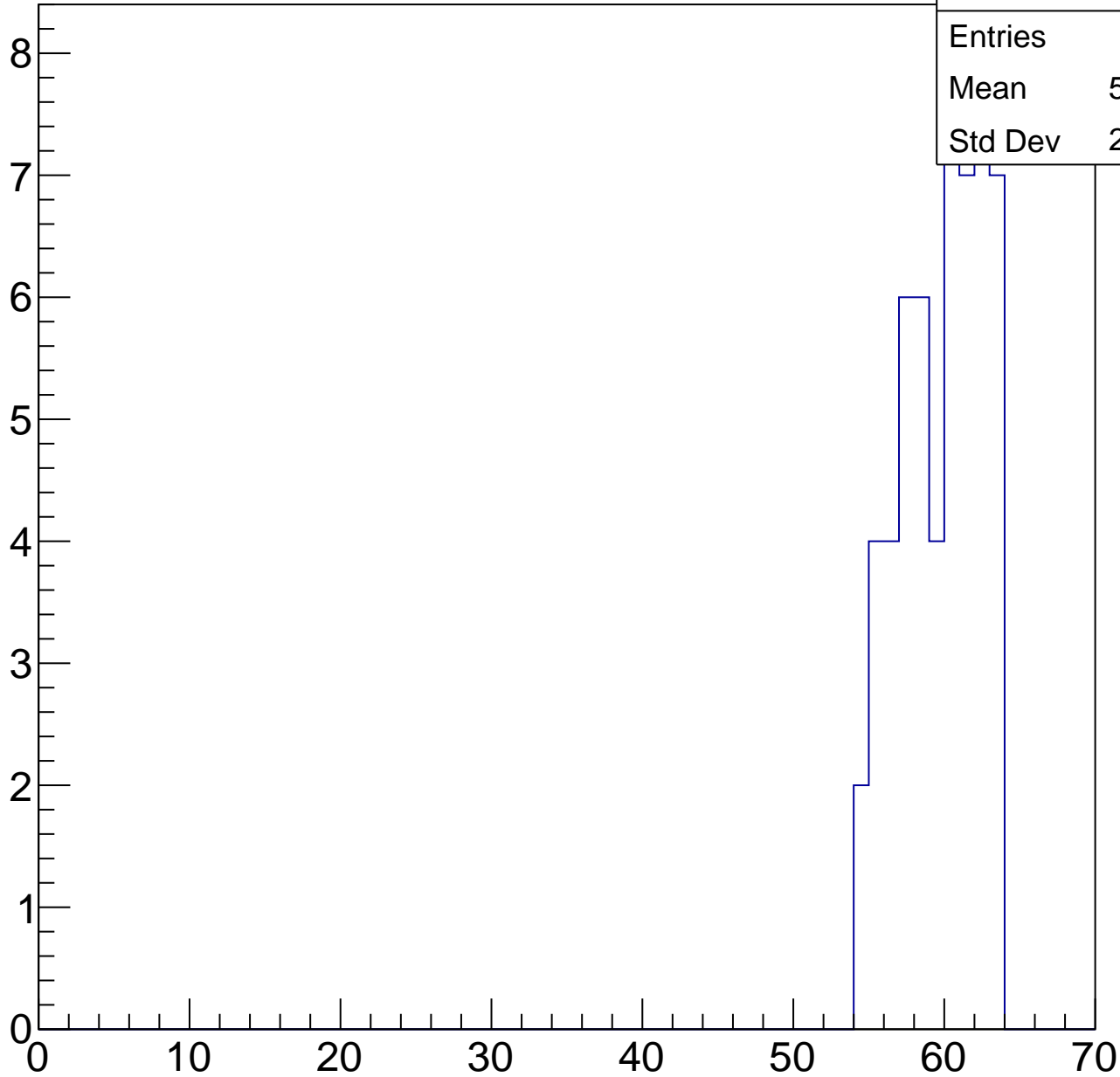
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	56
Mean	59.32
Std Dev	2.653

ampl



# B1L003S, U26-ch117, adc6

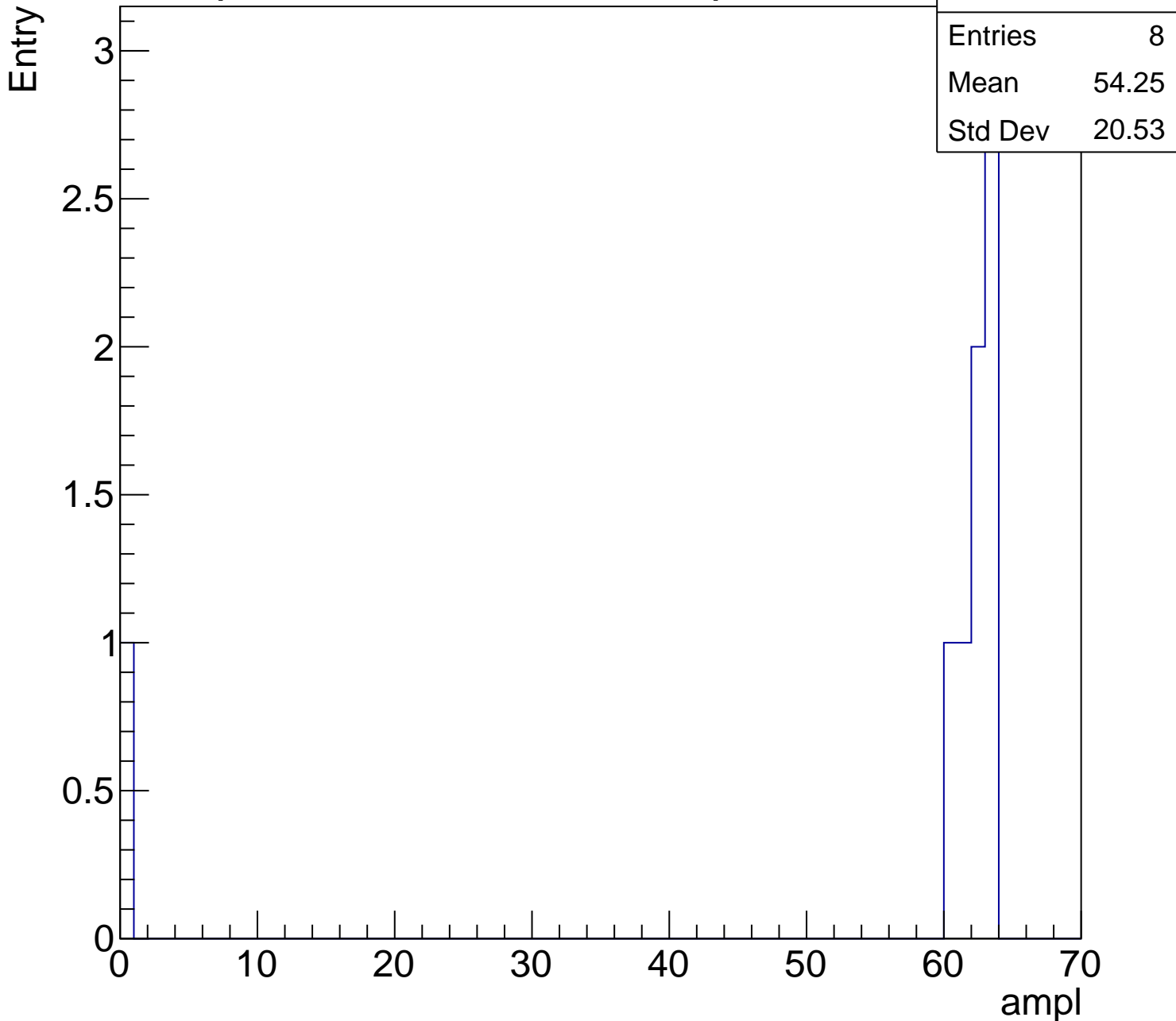
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

3  
2.5  
2  
1.5  
1  
0.5  
0

Entries	8
Mean	54.25
Std Dev	20.53

ampl





# B1L003S, U26-ch117, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U26-ch118, adc0

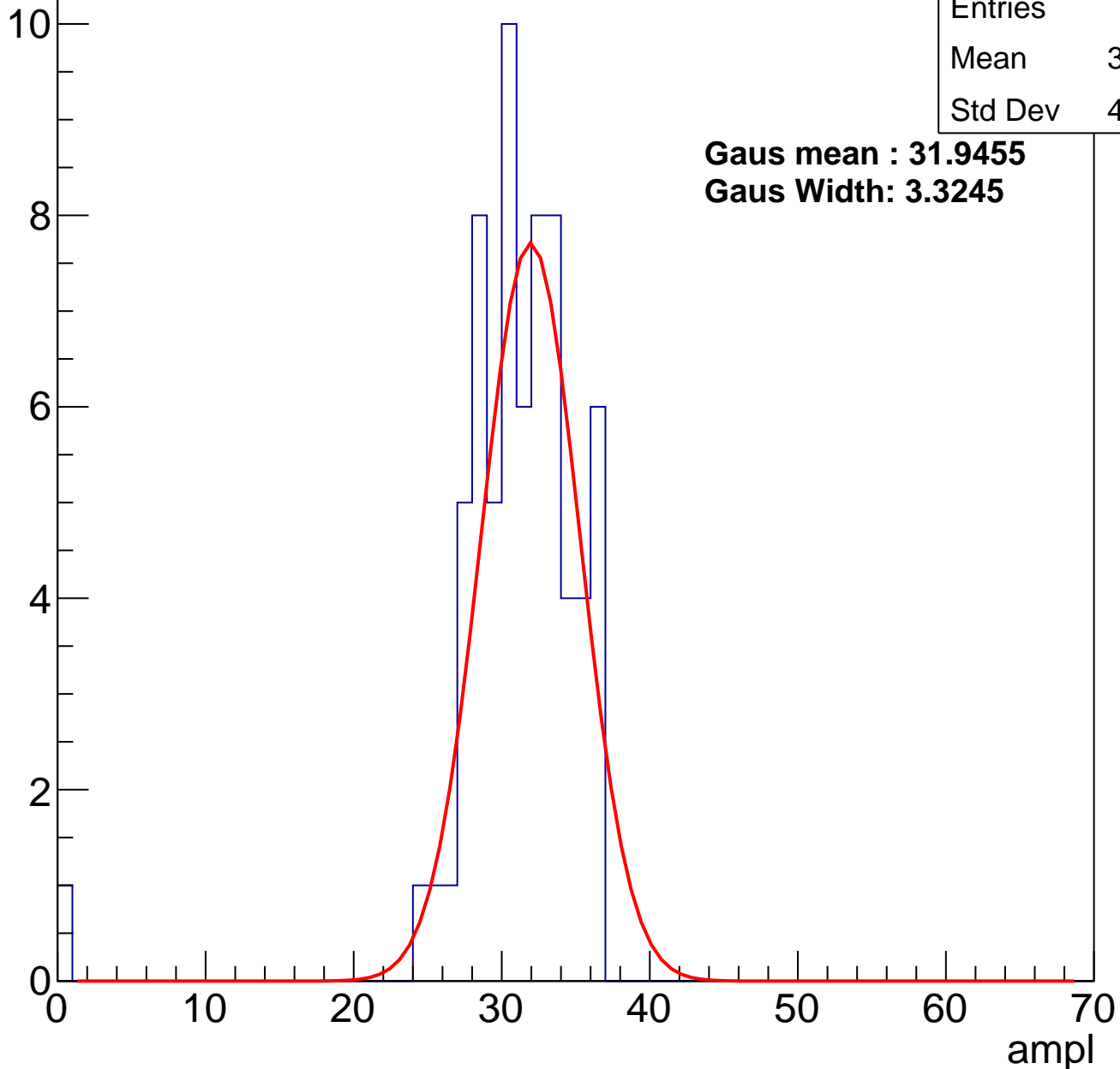
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	68
Mean	30.54
Std Dev	4.742

**Gaus mean : 31.9455**

**Gaus Width: 3.3245**

Entry



# B1L003S, U26-ch118, adc1

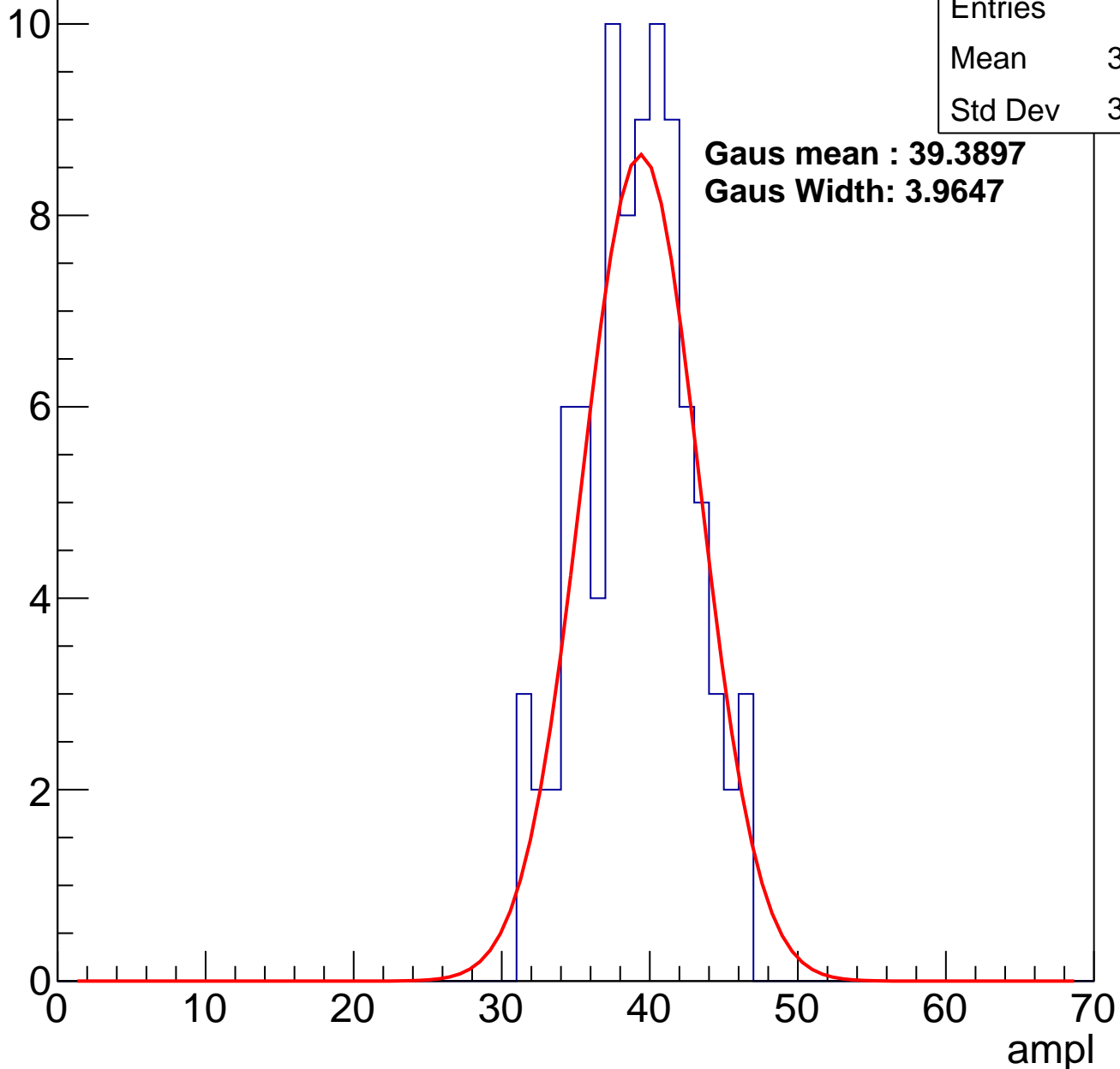
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	88
Mean	38.66
Std Dev	3.624

**Gaus mean : 39.3897**

**Gaus Width: 3.9647**

Entry



# B1L003S, U26-ch118, adc2

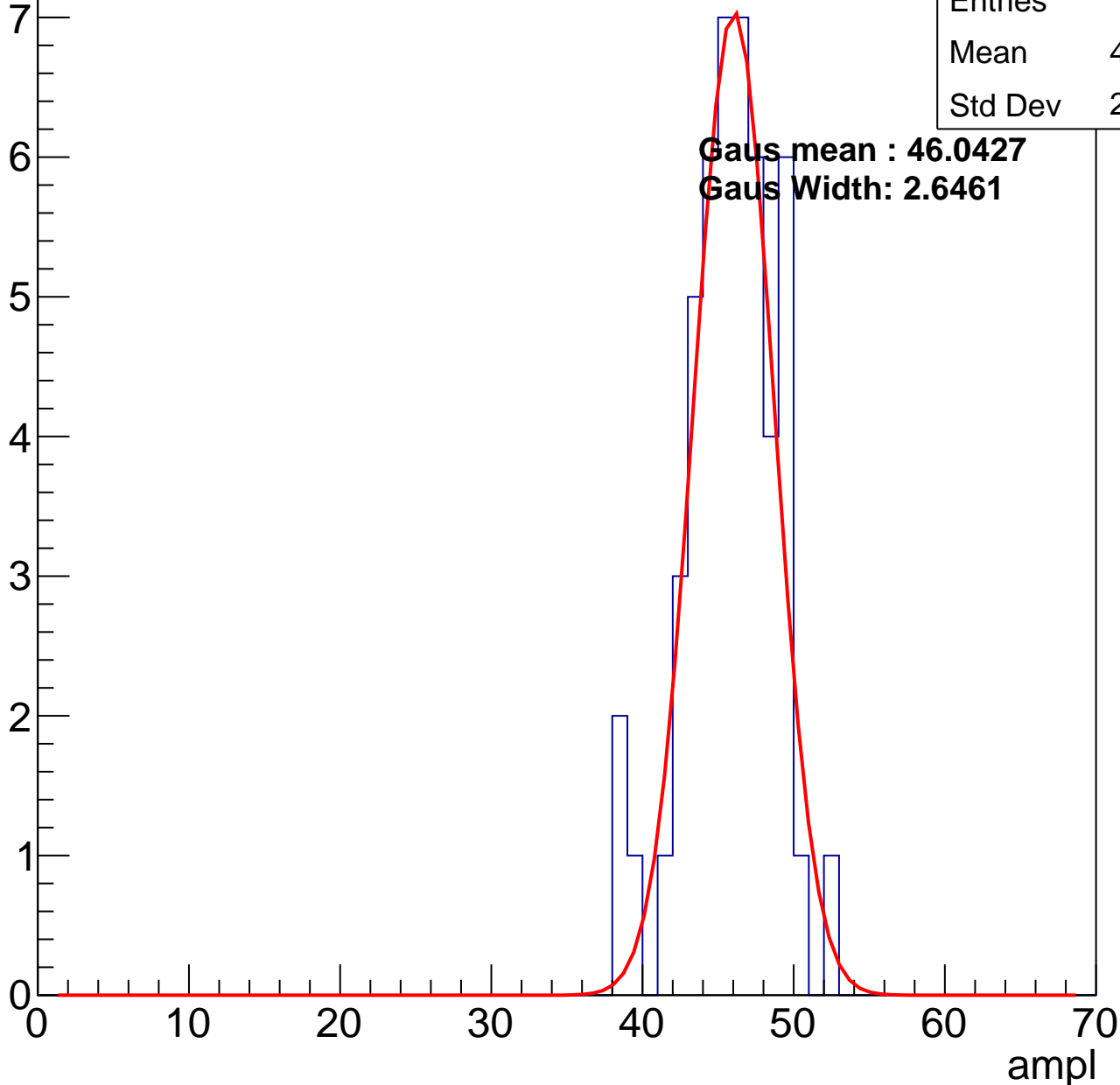
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	50
Mean	45.36
Std Dev	2.945

**Gaus mean : 46.0427**

**Gaus Width: 2.6461**

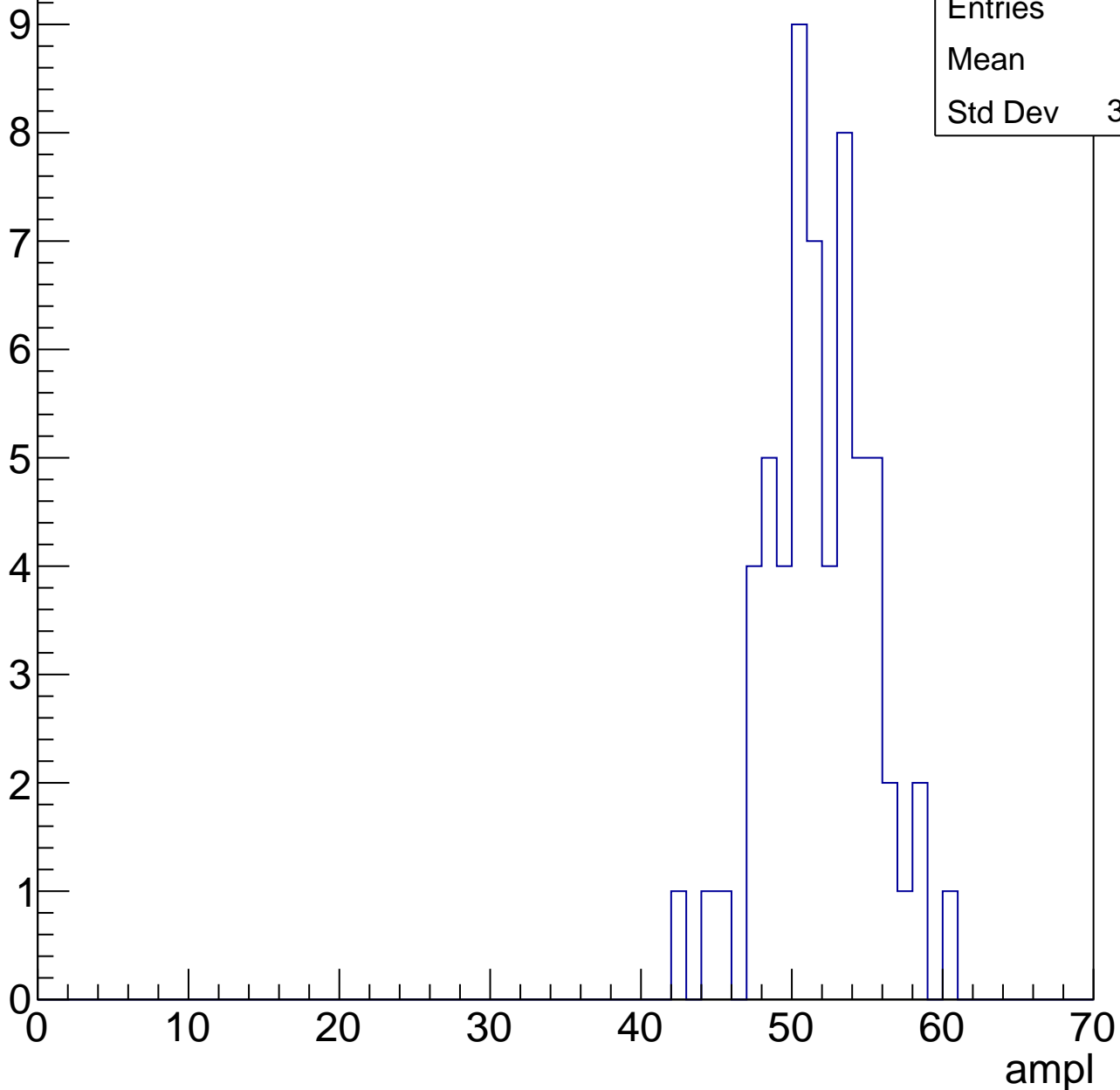


# B1L003S, U26-ch118, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	51.4
Std Dev	3.455

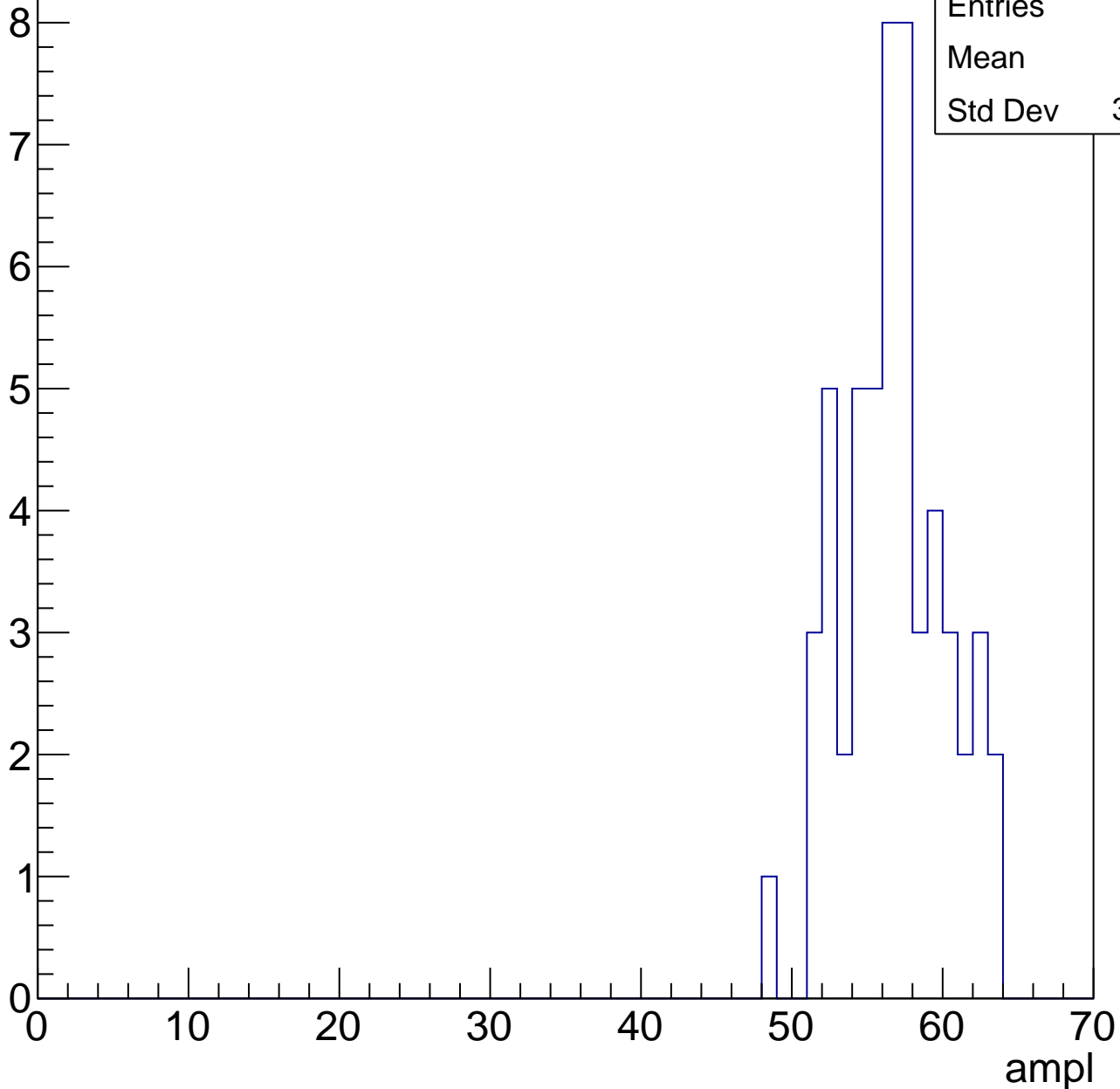


# B1L003S, U26-ch118, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

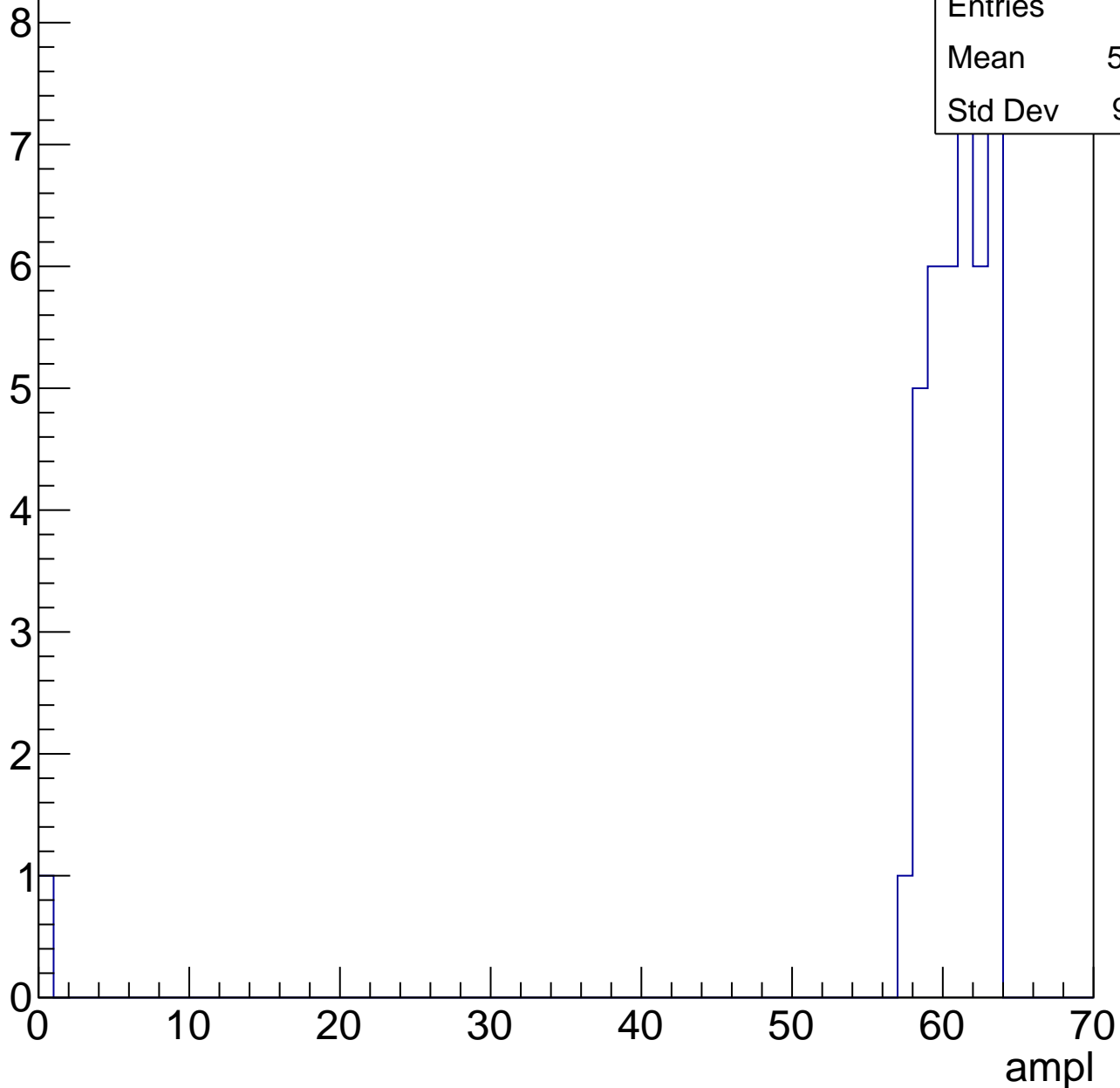
Entries	54
Mean	56.3
Std Dev	3.381



# B1L003S, U26-ch118, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U26-ch118, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch118, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	23
Std Dev	0

ampl

# B1L003S, U26-ch119, adc0

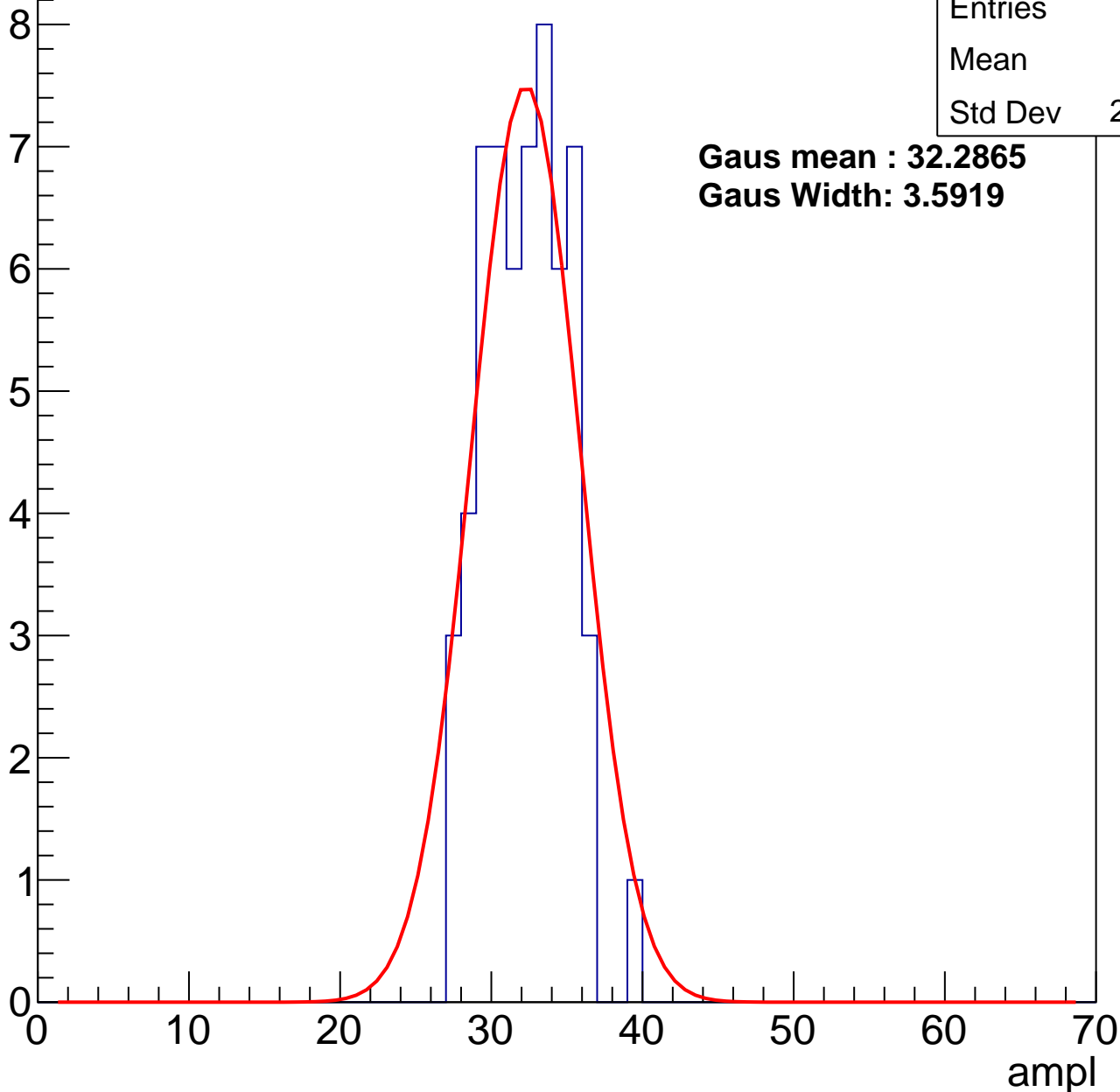
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	31.8
Std Dev	2.686

**Gaus mean : 32.2865**

**Gaus Width: 3.5919**



# B1L003S, U26-ch119, adc1

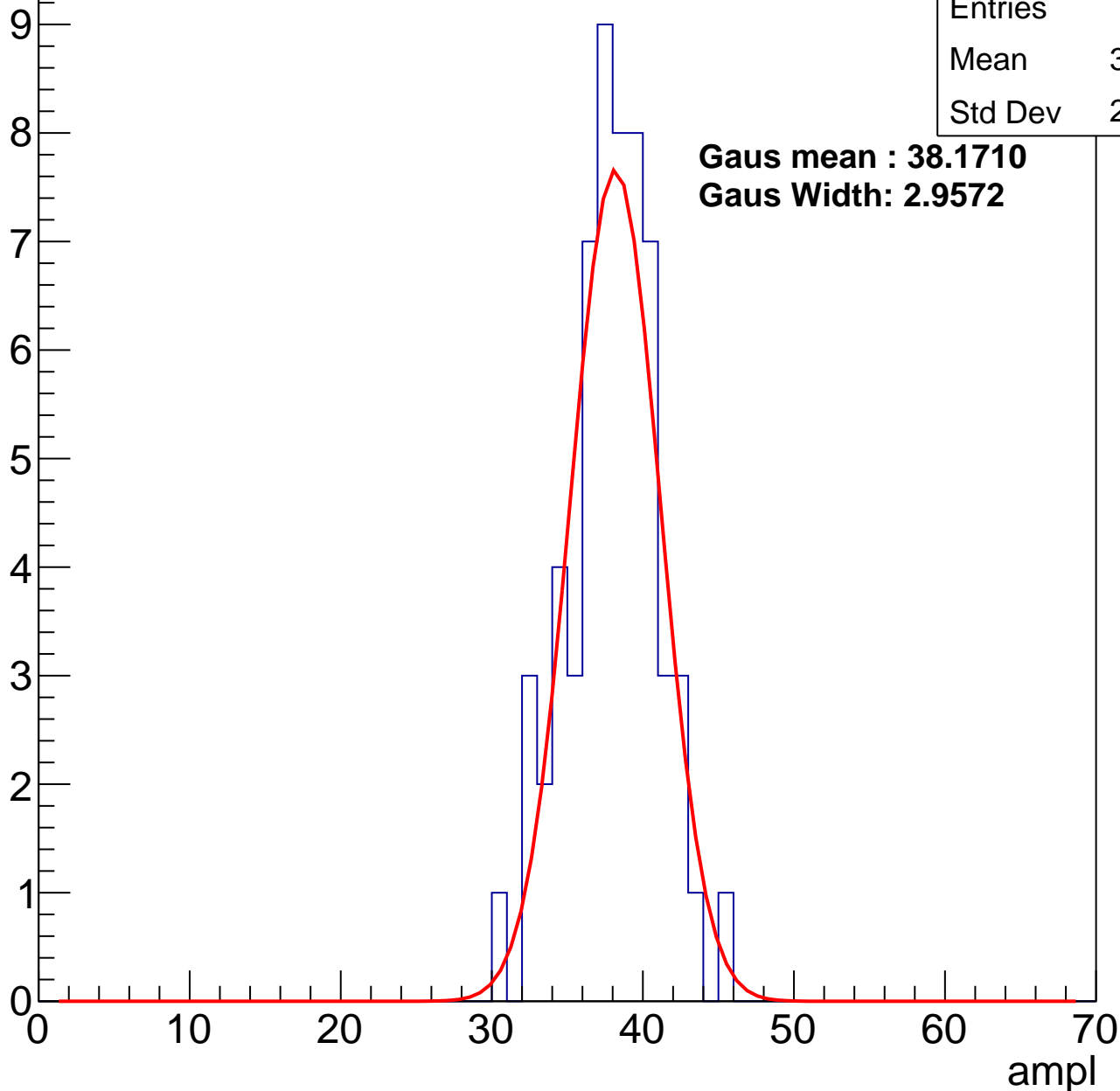
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	37.52
Std Dev	2.947

**Gaus mean : 38.1710**

**Gaus Width: 2.9572**



# B1L003S, U26-ch119, adc2

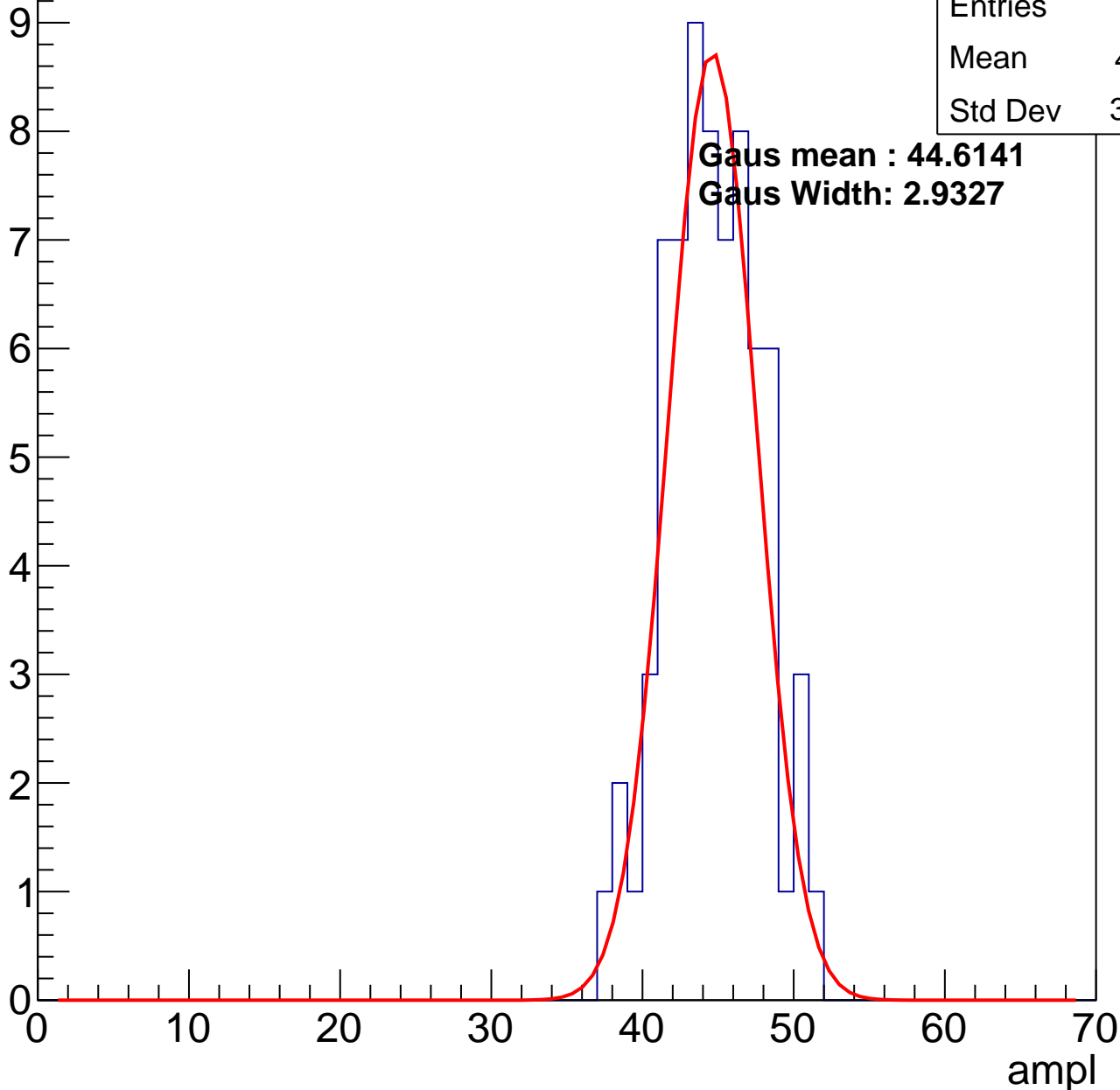
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	44.21
Std Dev	3.075

**Gaus mean : 44.6141**

**Gaus Width: 2.9327**

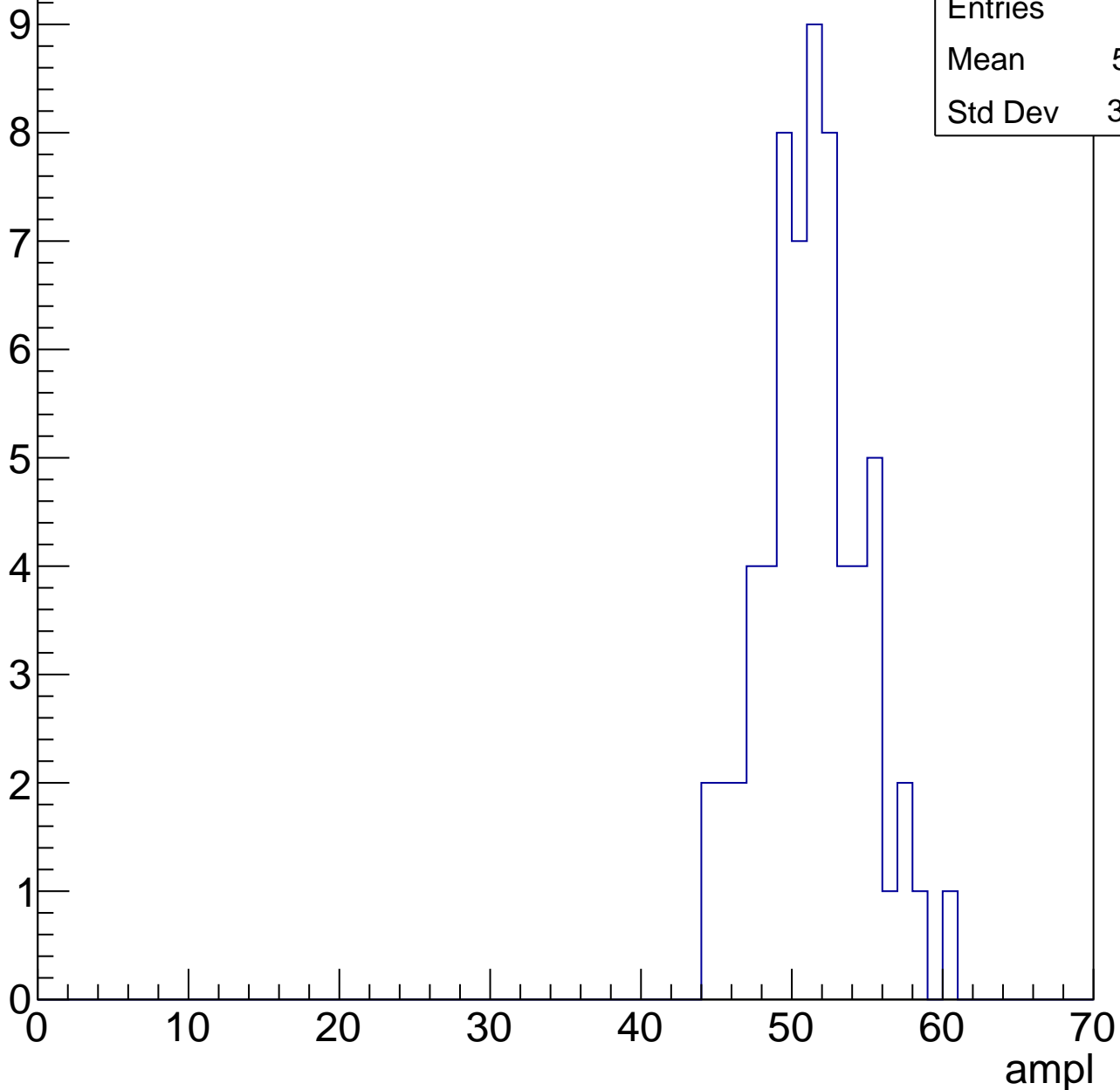


# B1L003S, U26-ch119, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

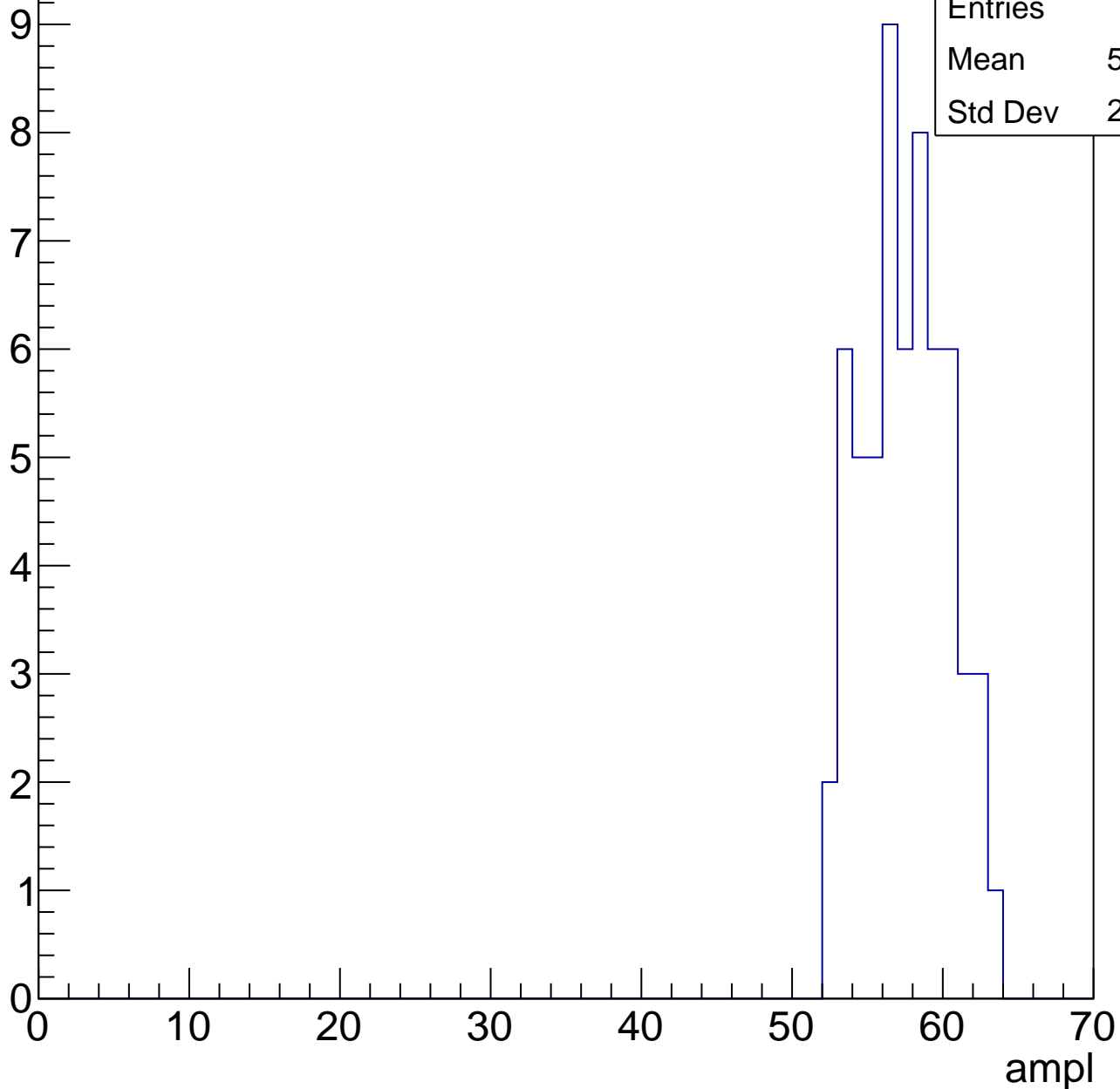
Entries	64
Mean	50.91
Std Dev	3.367



# B1L003S, U26-ch119, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



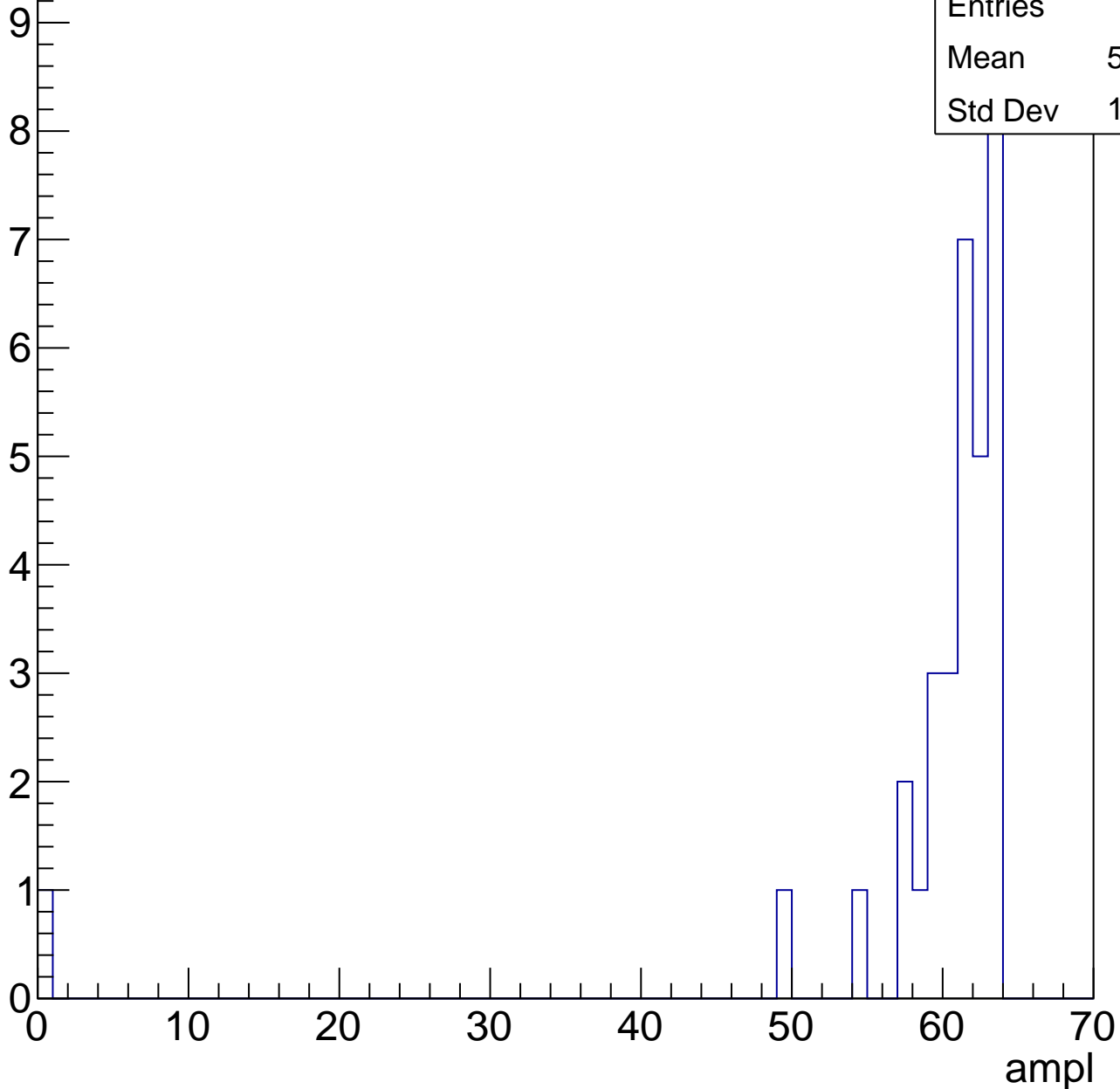
Entries	60
Mean	57.05
Std Dev	2.783

# B1L003S, U26-ch119, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	33
Mean	58.67
Std Dev	10.78



# B1L003S, U26-ch119, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	61
Std Dev	1.414

ampl

0 10 20 30 40 50 60 70

0 0.2 0.4 0.6 0.8 1 1.2 1.4 1.6 1.8 2

0 10 20 30 40 50 60 70

0 10 20 30 40 50 60 70

0 10 20 30 40 50 60 70

0 10 20 30 40 50 60 70

0 10 20 30 40 50 60 70

0 10 20 30 40 50 60 70

0 10 20 30 40 50 60 70

0 10 20 30 40 50 60 70

0 10 20 30 40 50 60 70

0 10 20 30 40 50 60 70

0 10 20 30 40 50 60 70

0 10 20 30 40 50 60 70

0 10 20 30 40 50 60 70

0 10 20 30 40 50 60 70

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0 10 20 30 40 50 60 70

0 10 20 30 40 50 60 70

0 10 20 30 40 50 60 70

0 10 20 30 40 50 60 70

0 10 20 30 40 50 60 70

0 10 20 30 40 50 60 70

0 10 20 30 40 50 60 70



# B1L003S, U26-ch119, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	12.5
Std Dev	12.5

# B1L003S, U26-ch120, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	79
Mean	30.25
Std Dev	3.706

**Gaus mean : 31.3606**

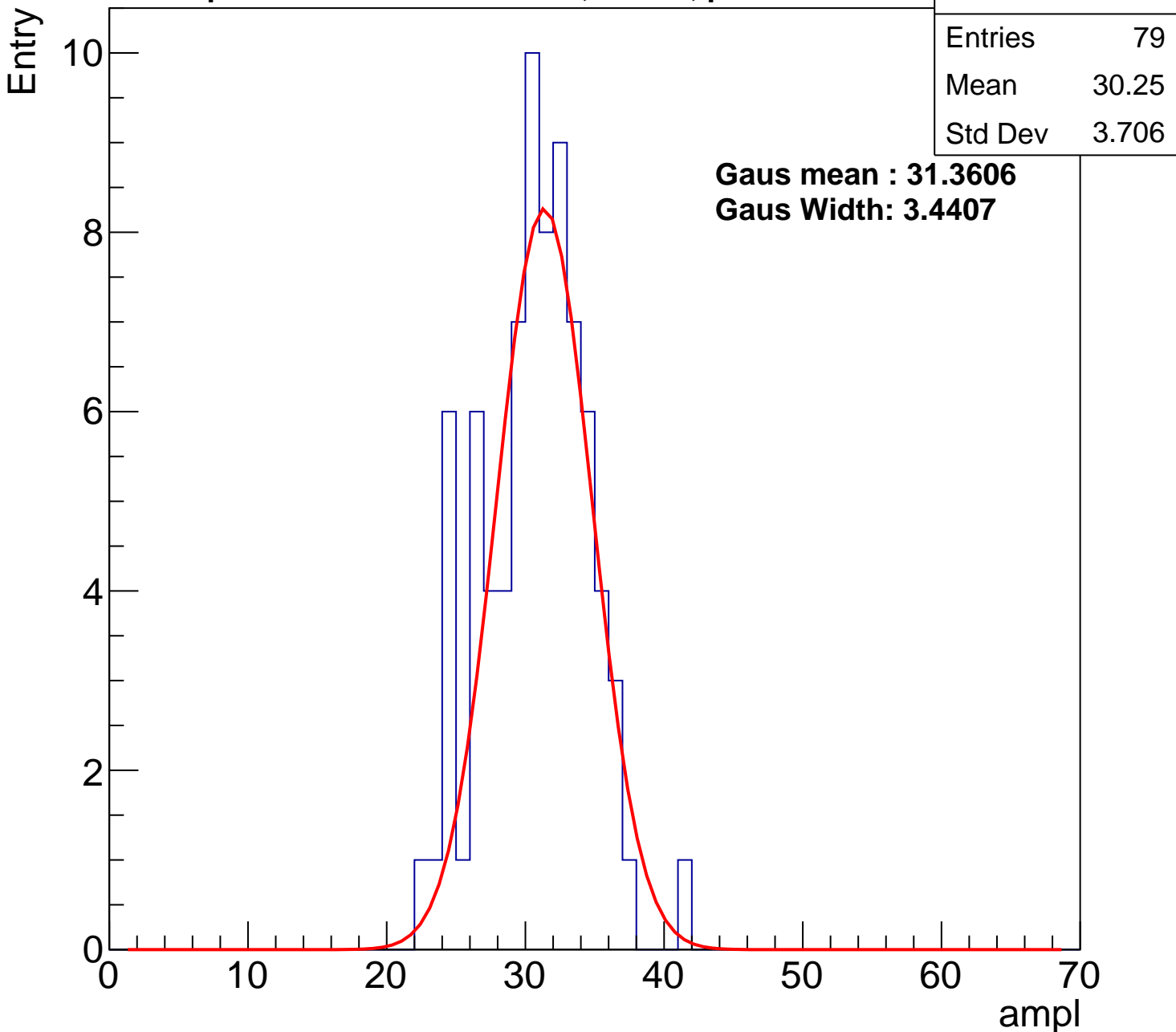
**Gaus Width: 3.4407**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U26-ch120, adc1

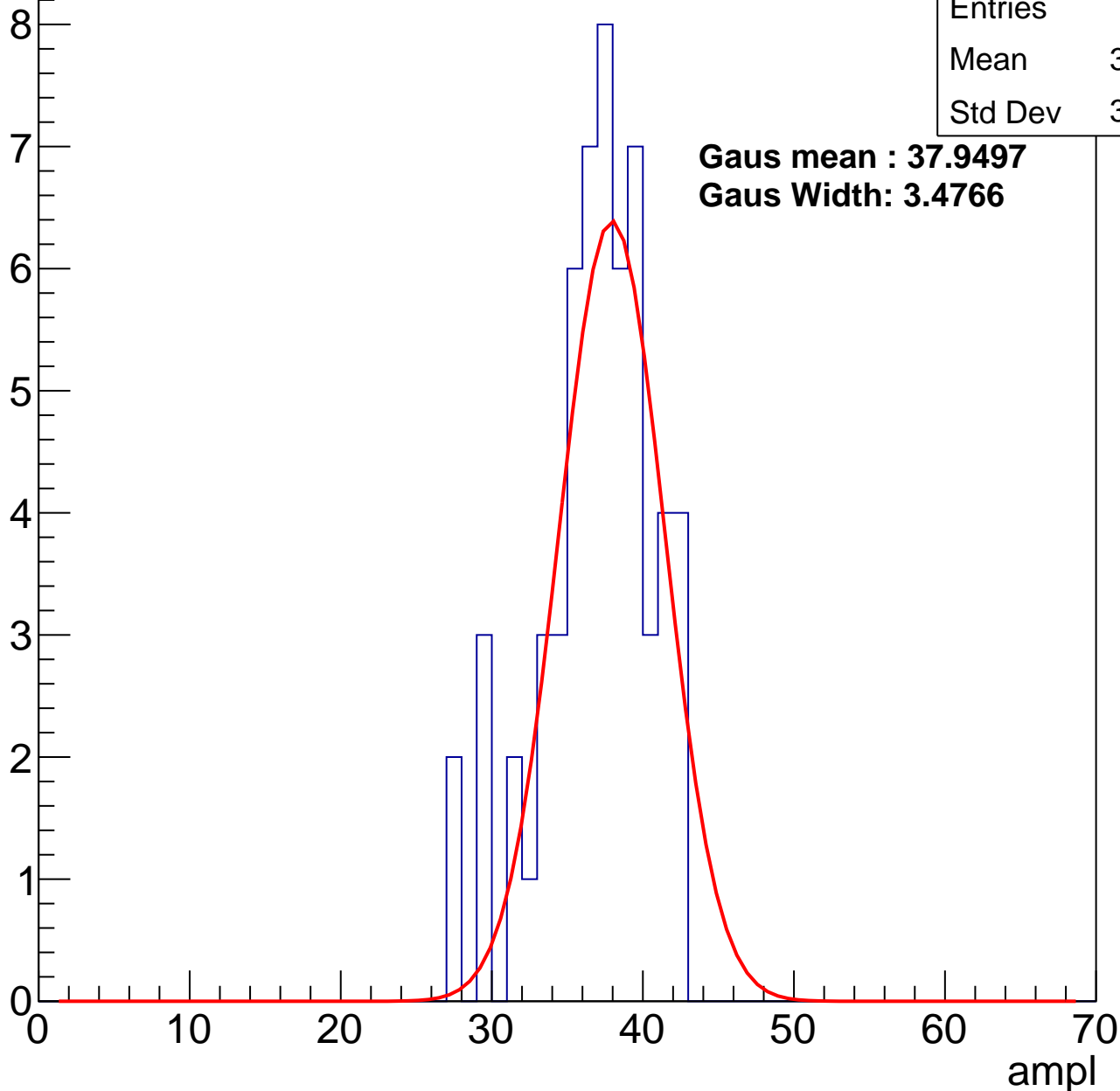
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	36.39
Std Dev	3.678

**Gaus mean : 37.9497**

**Gaus Width: 3.4766**



# B1L003S, U26-ch120, adc2

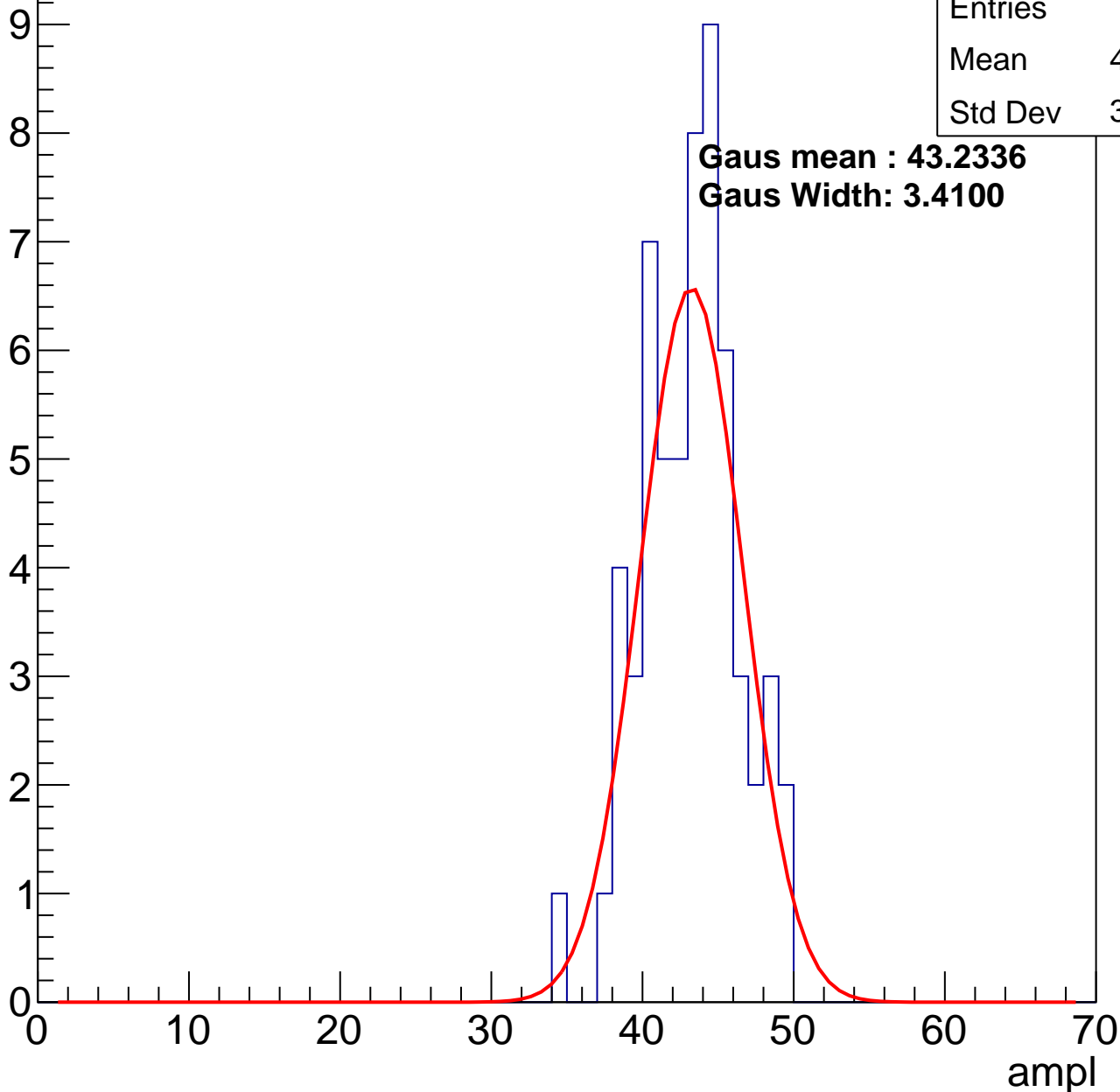
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	42.69
Std Dev	3.153

**Gaus mean : 43.2336**

**Gaus Width: 3.4100**

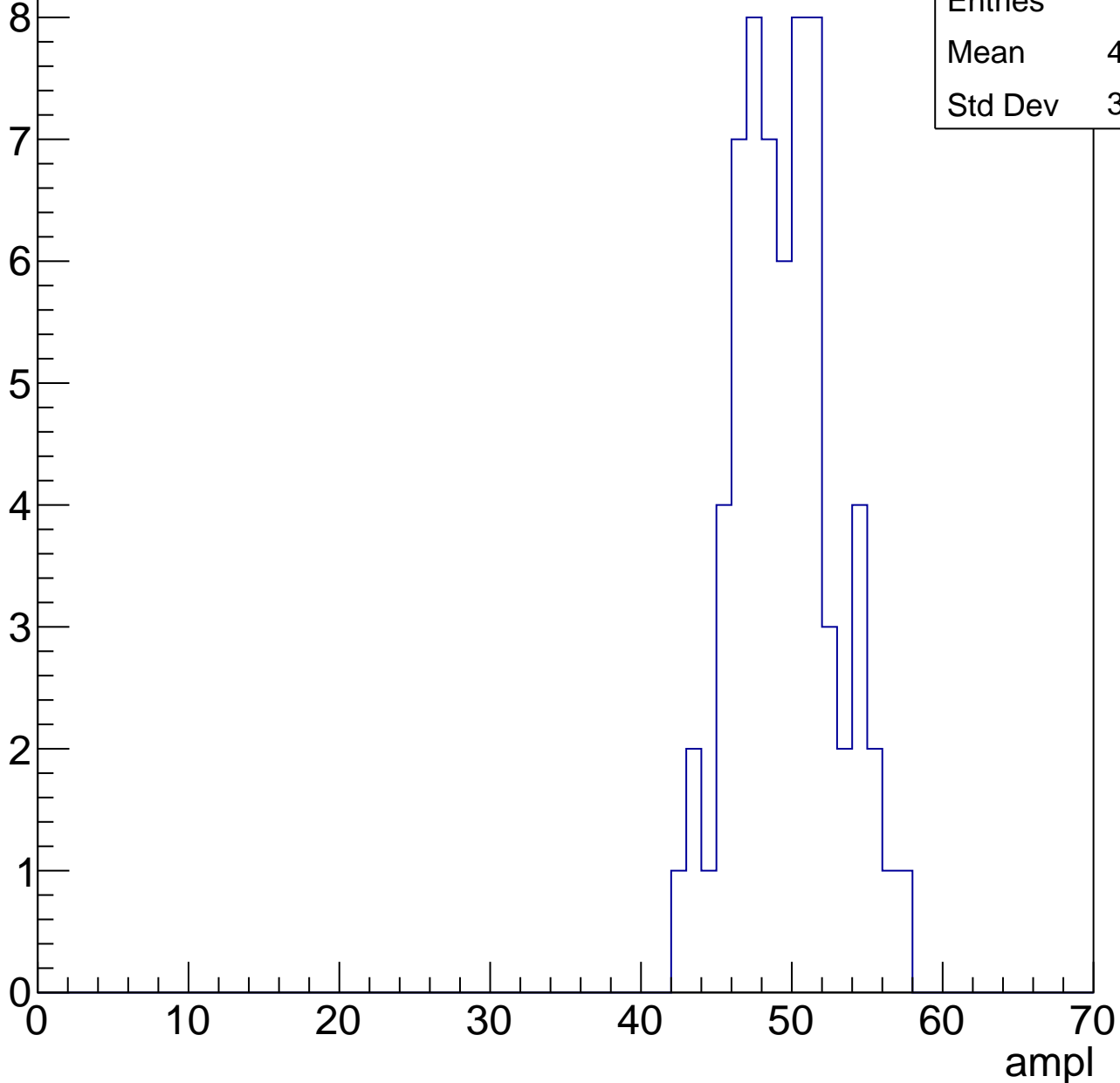


# B1L003S, U26-ch120, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	49.06
Std Dev	3.272

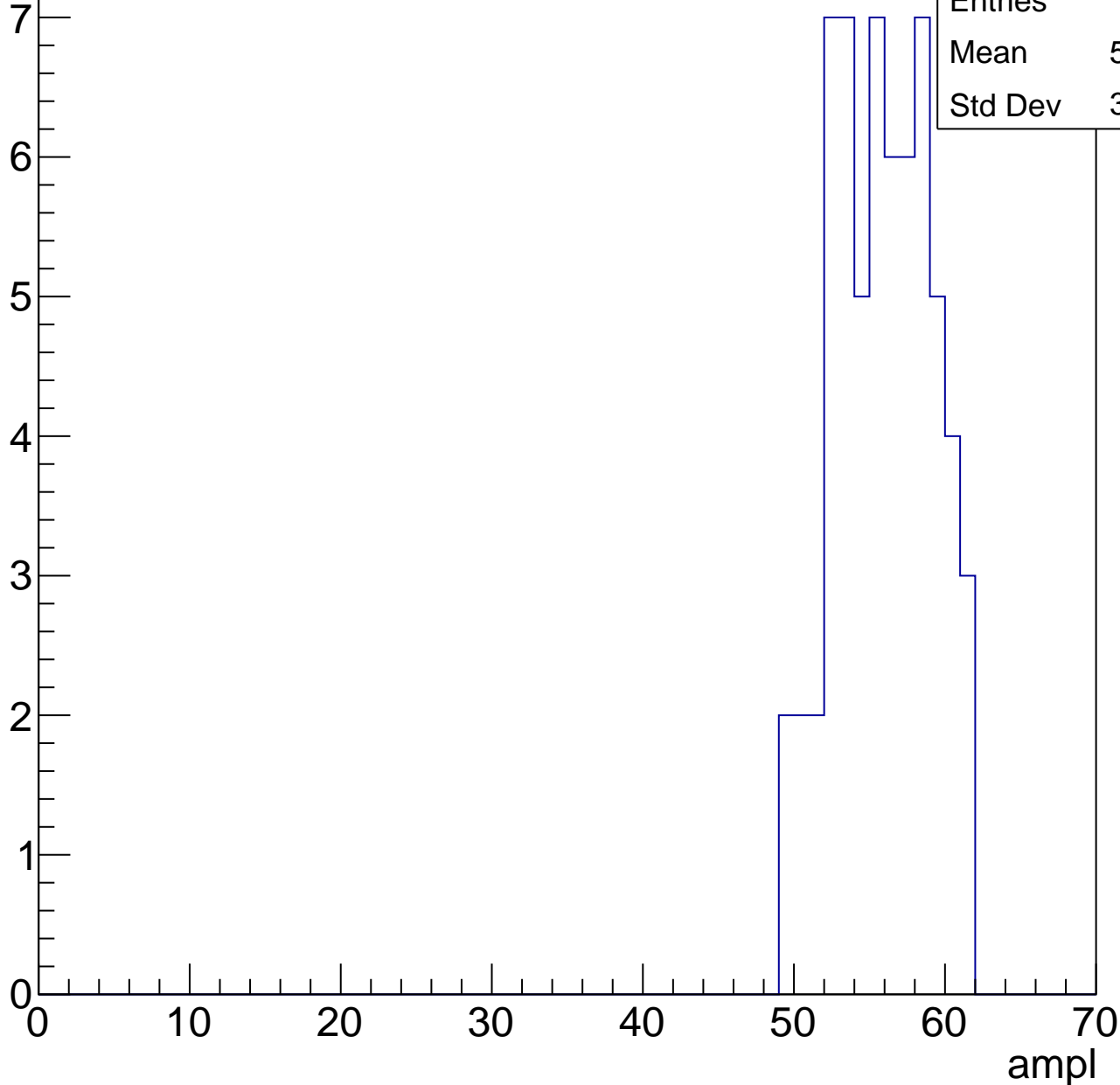


# B1L003S, U26-ch120, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	55.43
Std Dev	3.136

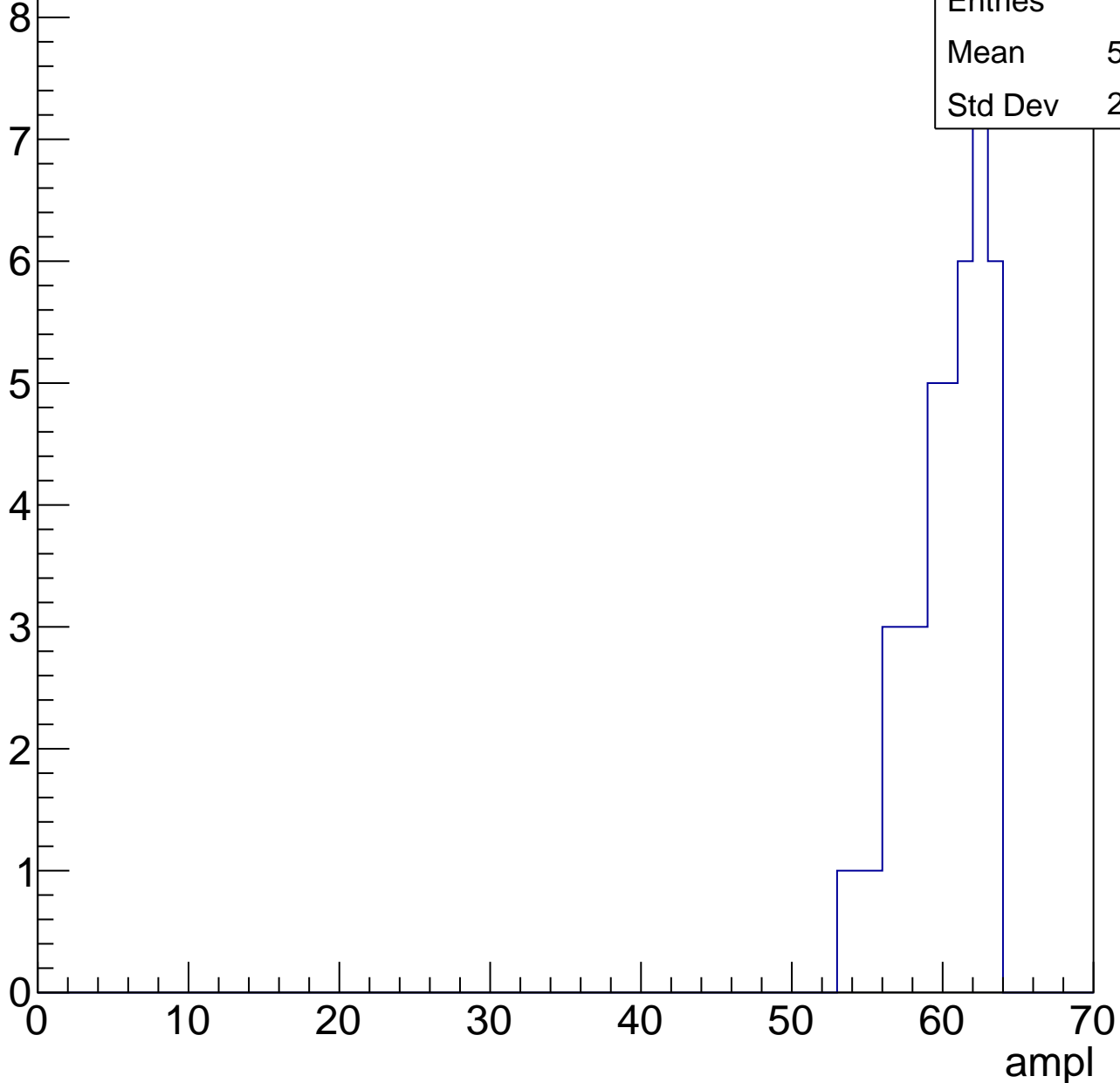


# B1L003S, U26-ch120, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

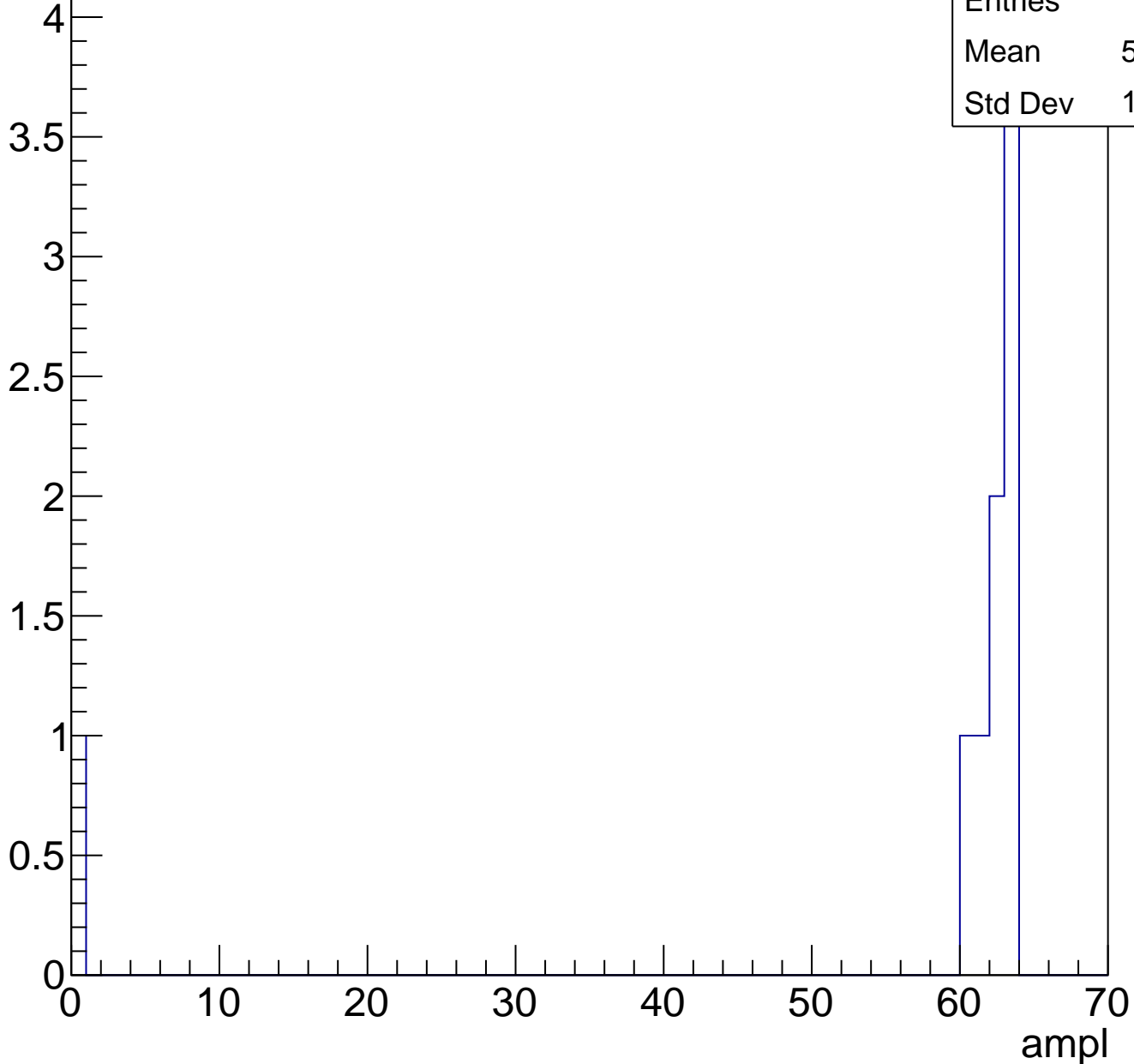
Entries	42
Mean	59.76
Std Dev	2.635



# B1L003S, U26-ch120, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch120, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U26-ch121, adc0

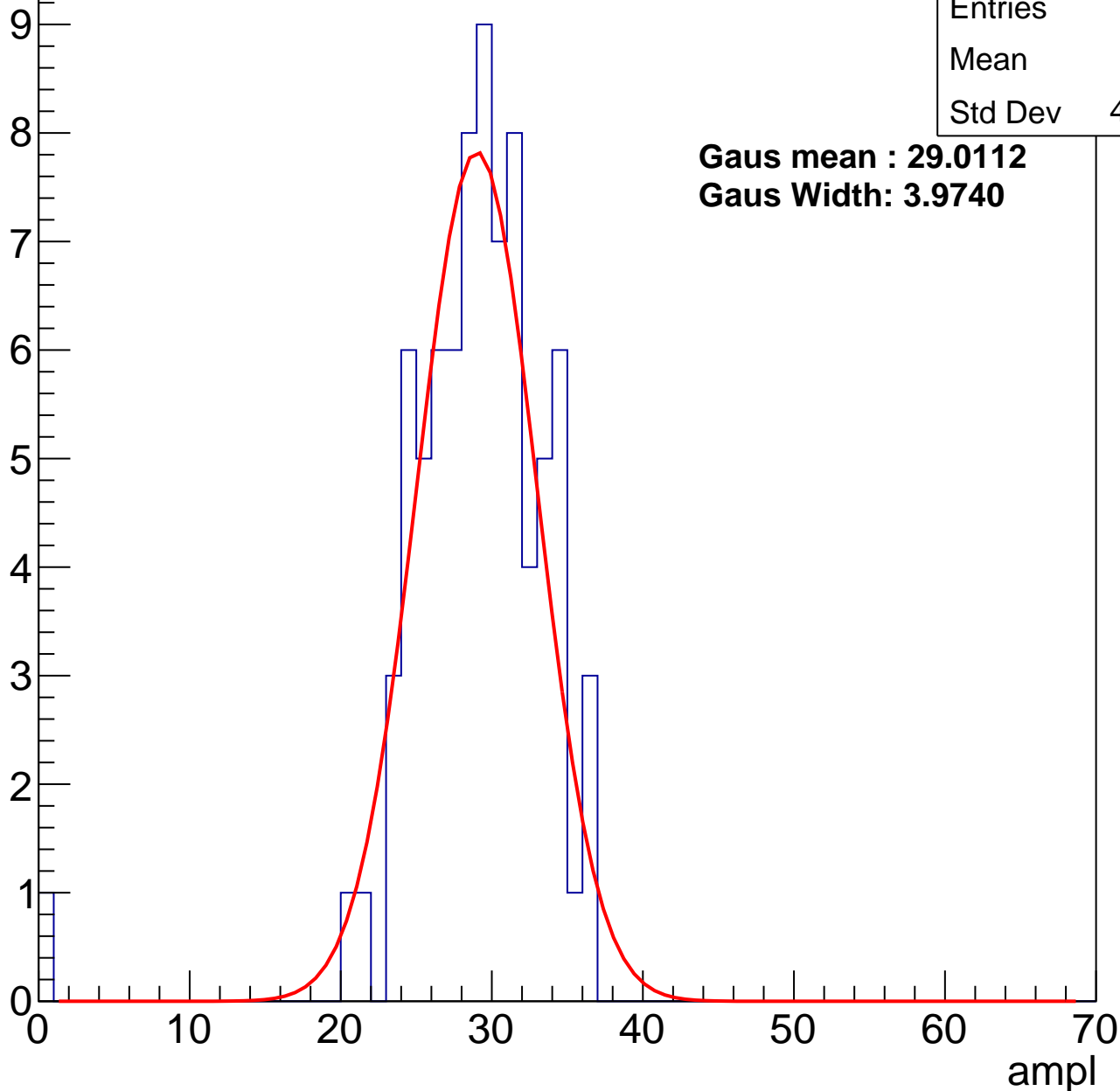
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	80
Mean	28.5
Std Dev	4.845

**Gaus mean : 29.0112**

**Gaus Width: 3.9740**



# B1L003S, U26-ch121, adc1

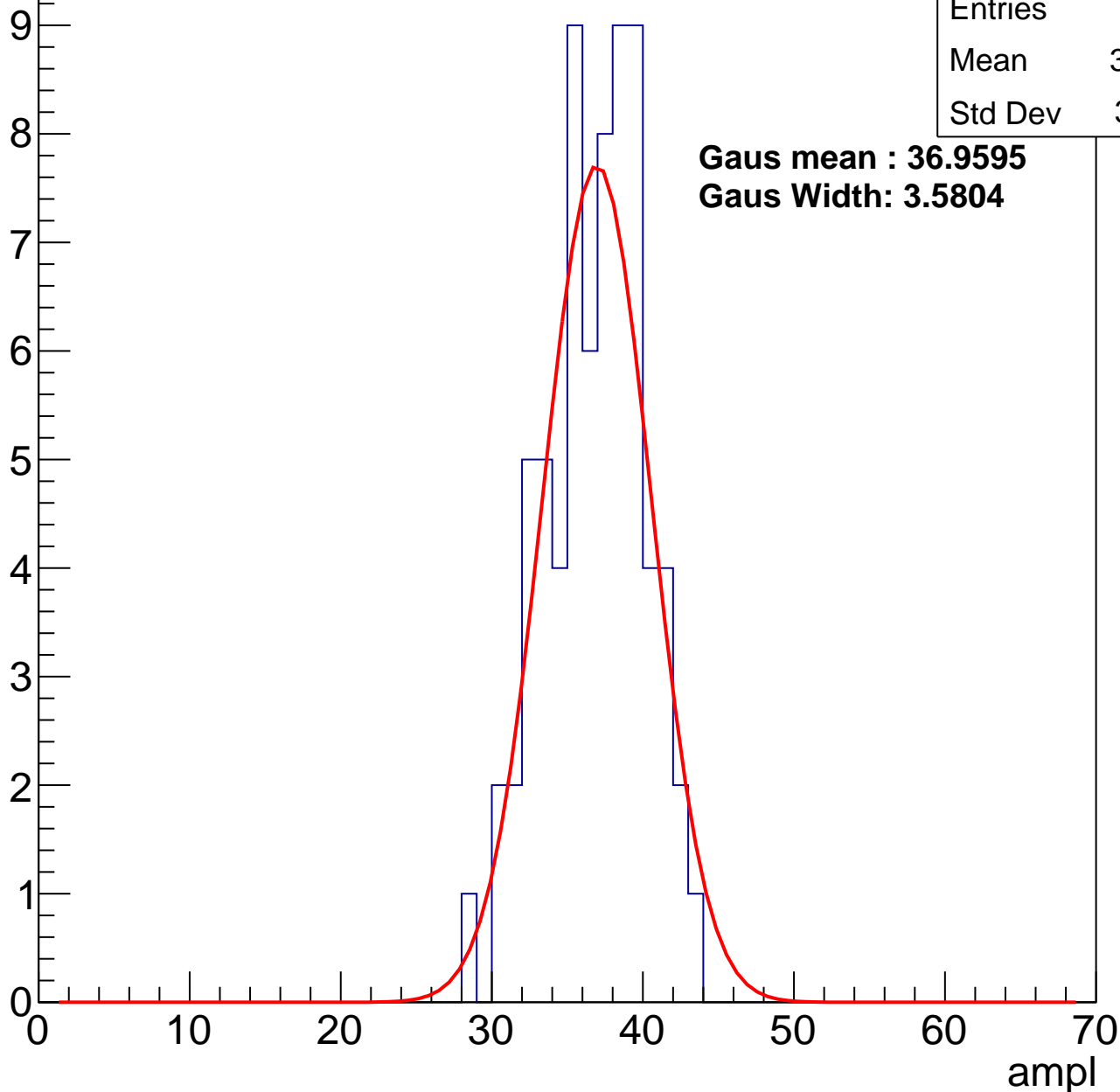
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	71
Mean	36.37
Std Dev	3.221

**Gaus mean : 36.9595**

**Gaus Width: 3.5804**



# B1L003S, U26-ch121, adc2

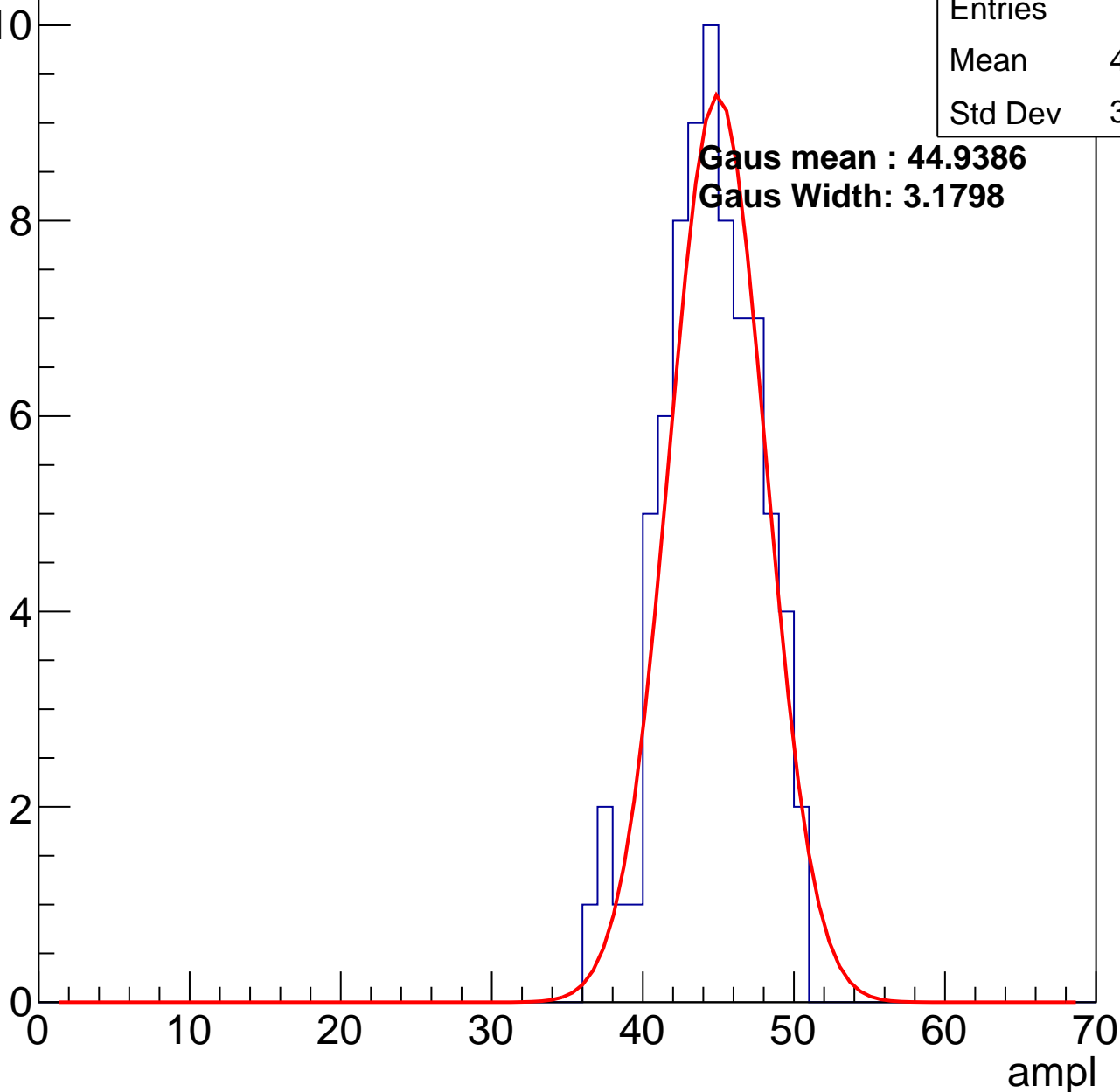
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	76
Mean	43.99
Std Dev	3.139

**Gaus mean : 44.9386**

**Gaus Width: 3.1798**



# B1L003S, U26-ch121, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

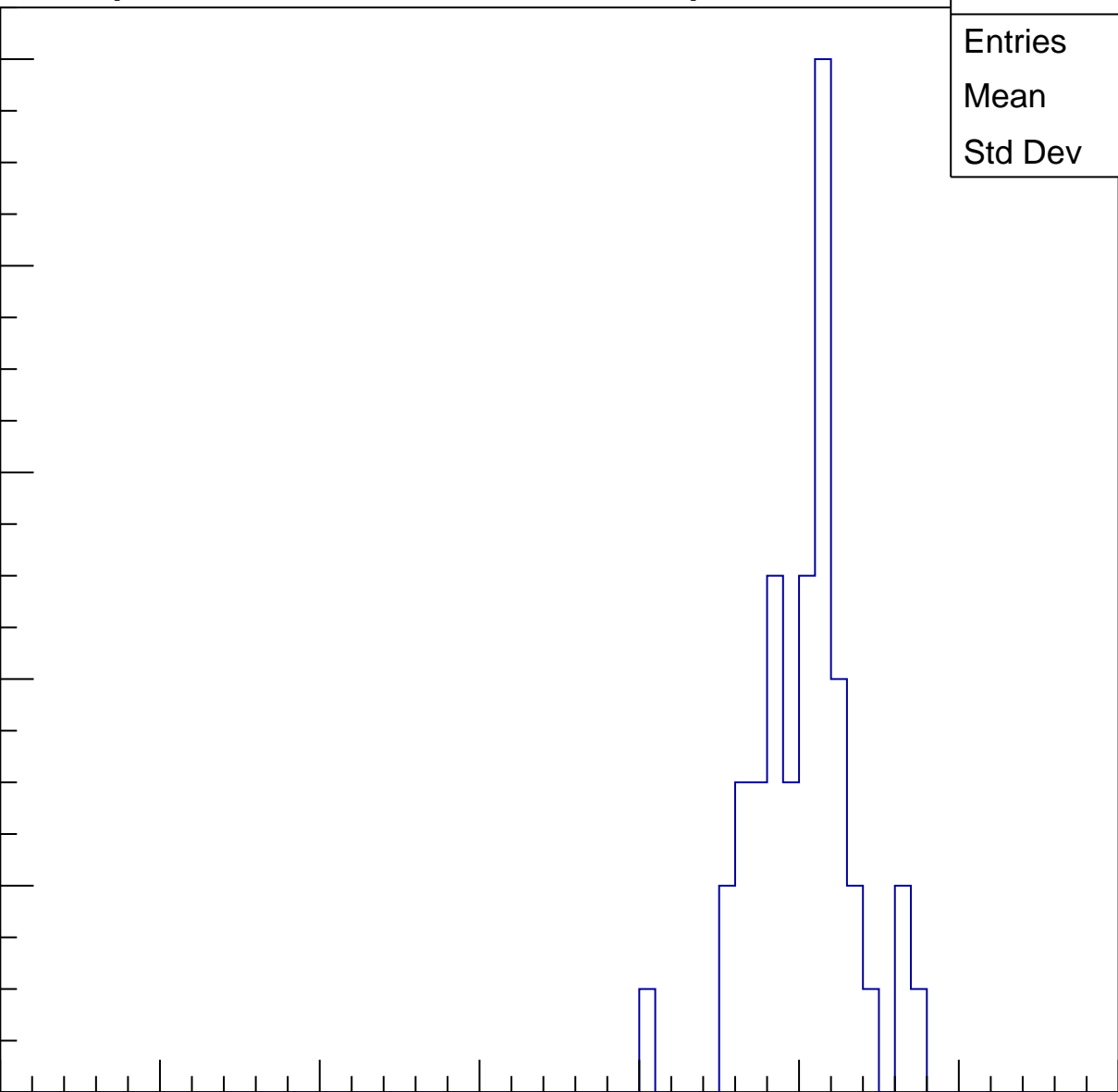
Entries	42
Mean	49.83
Std Dev	3.192

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

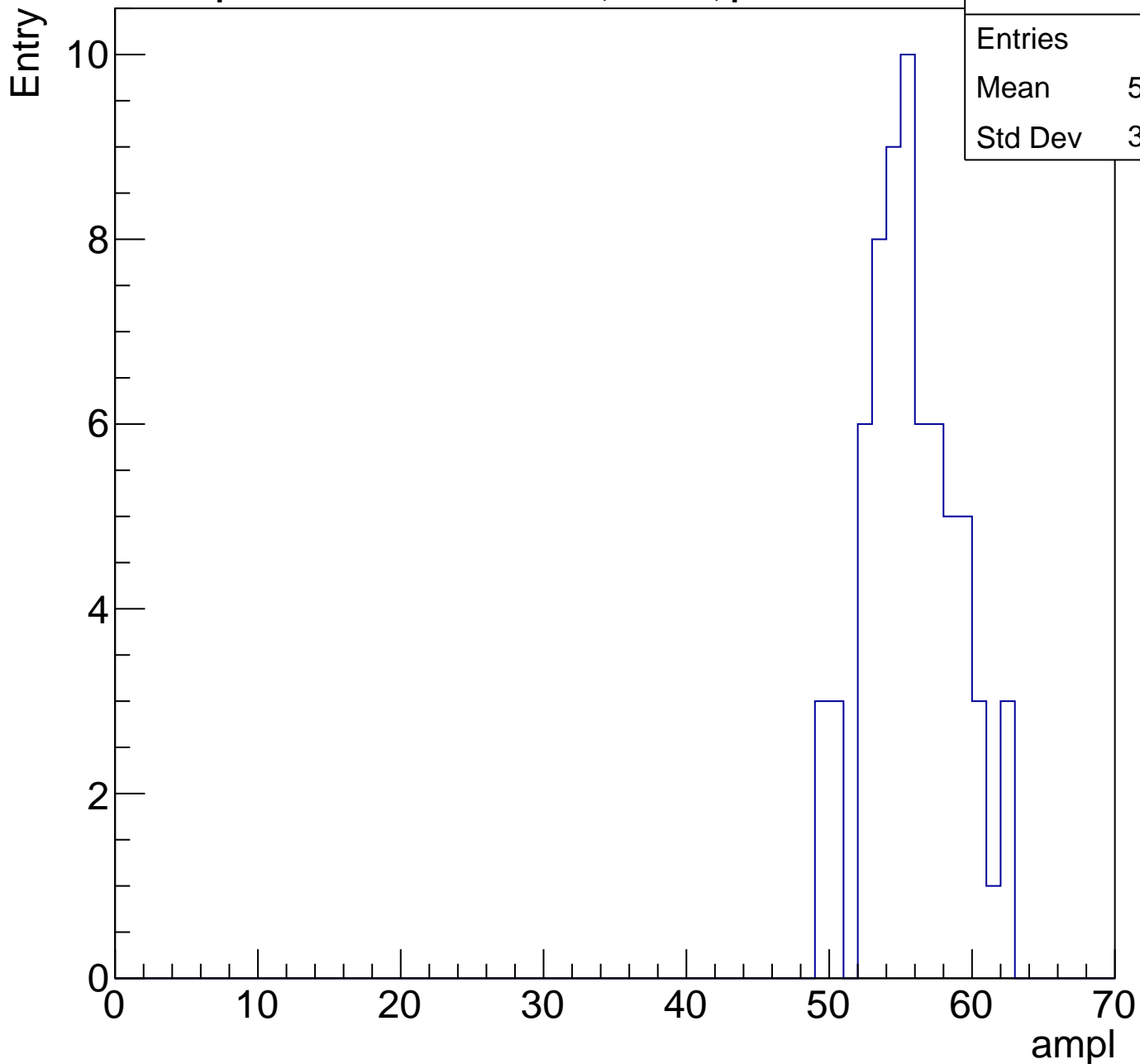
ampl



# B1L003S, U26-ch121, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	68
Mean	55.28
Std Dev	3.175

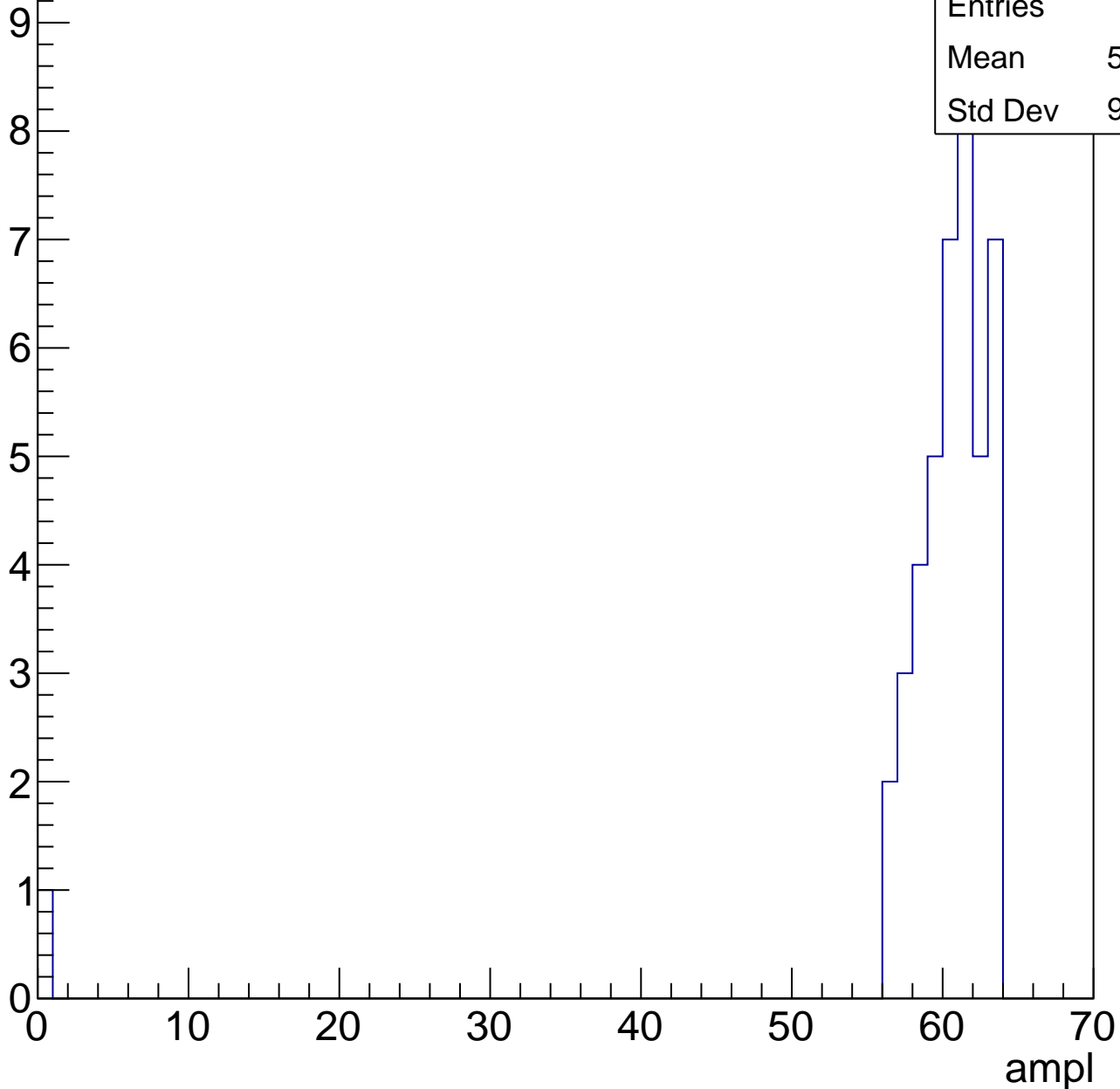


# B1L003S, U26-ch121, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

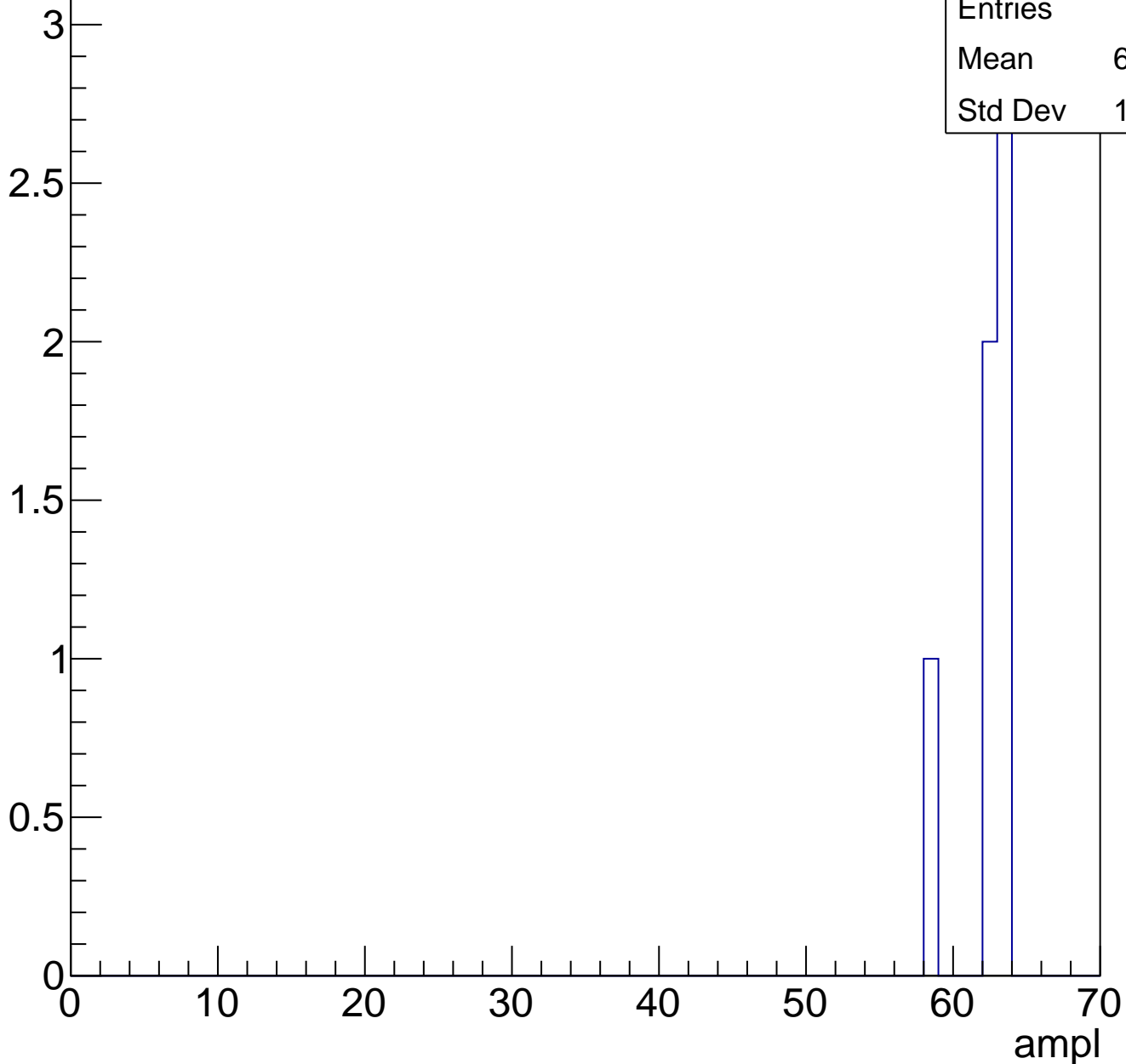
Entries	43
Mean	58.84
Std Dev	9.293



# B1L003S, U26-ch121, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch121, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L003S, U26-ch122, adc0

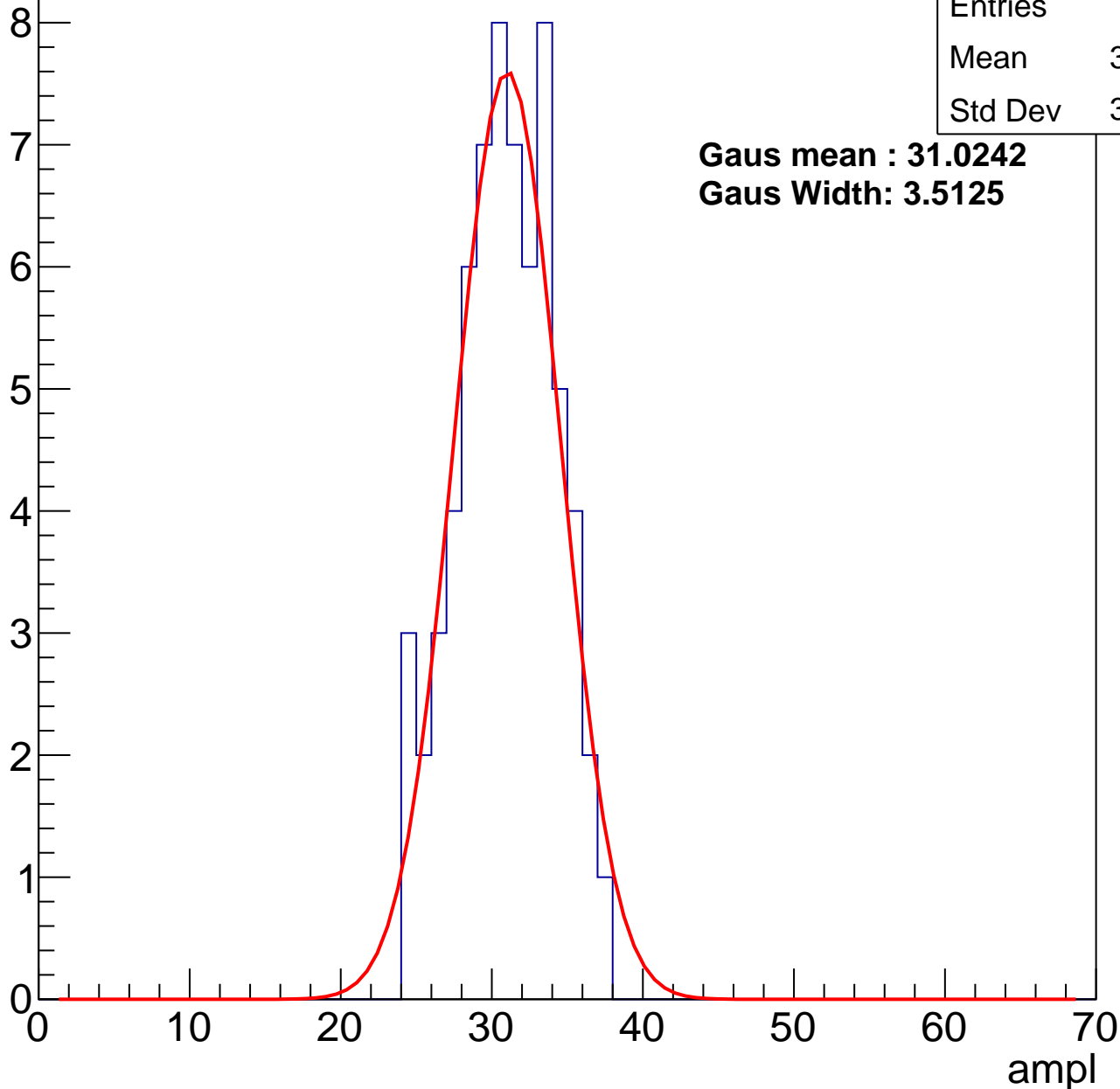
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	30.47
Std Dev	3.168

**Gaus mean : 31.0242**

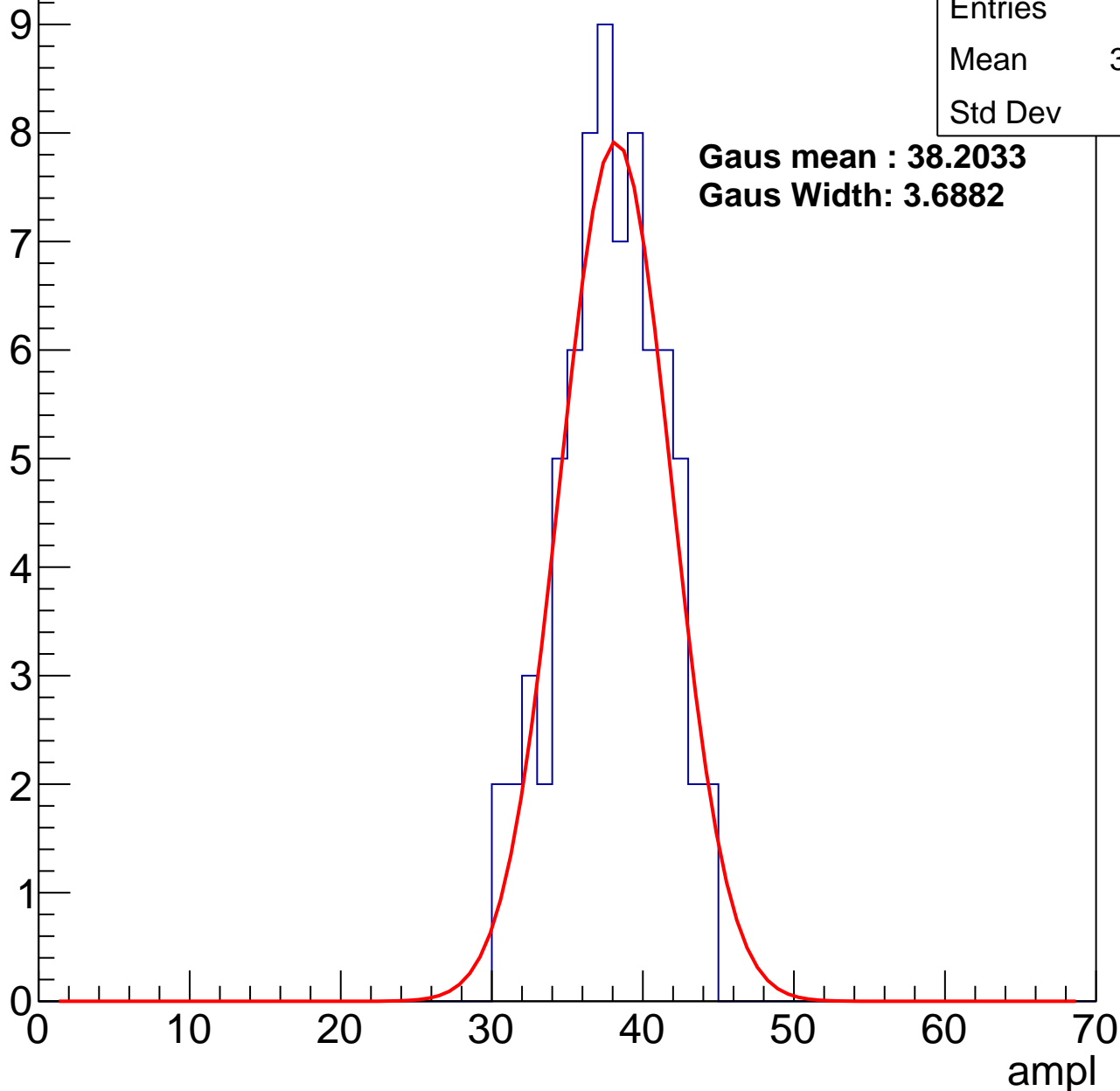
**Gaus Width: 3.5125**



# B1L003S, U26-ch122, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U26-ch122, adc2

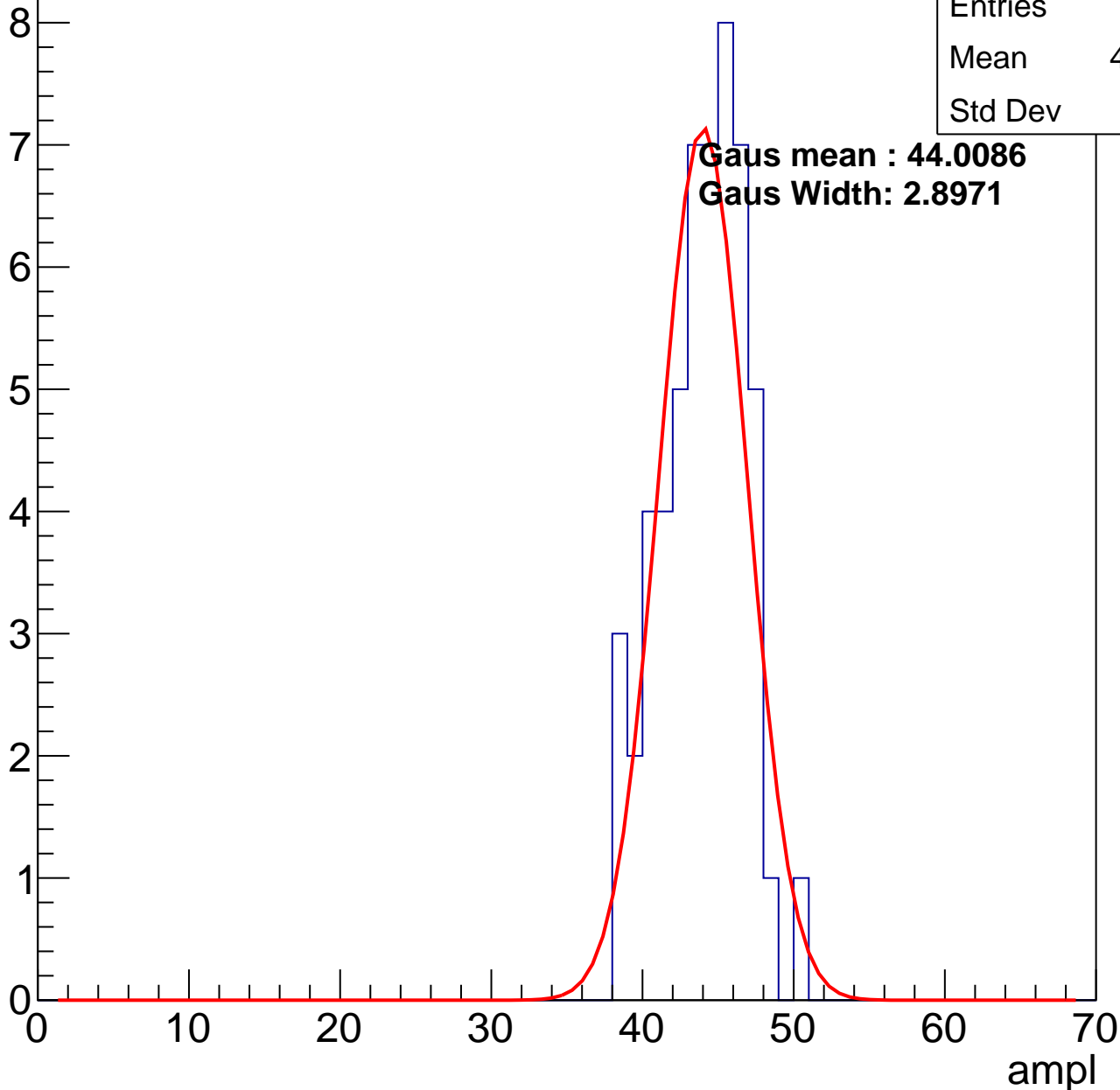
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	54
Mean	43.52
Std Dev	2.74

**Gaus mean : 44.0086**

**Gaus Width: 2.8971**

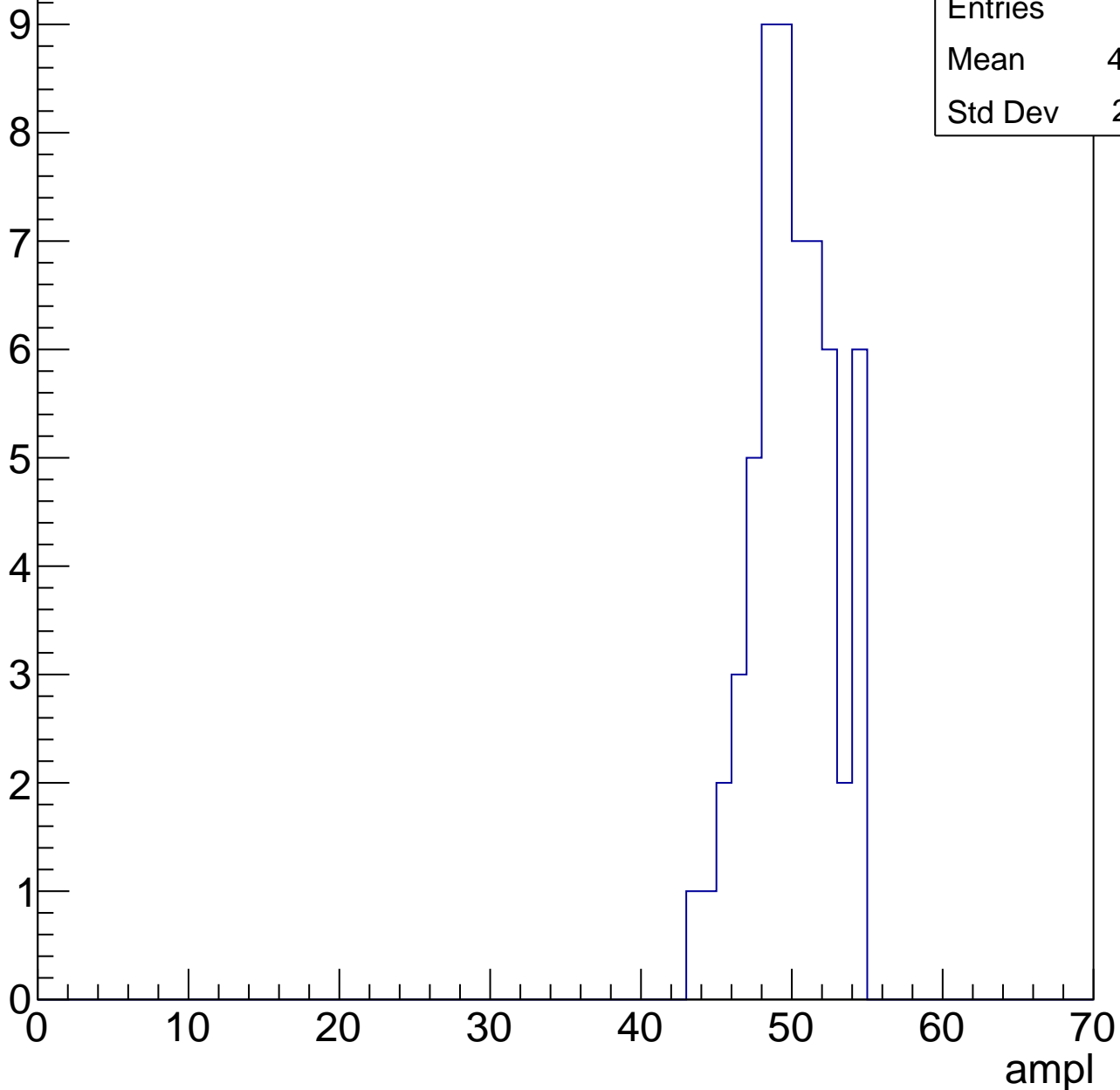


# B1L003S, U26-ch122, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	49.52
Std Dev	2.641

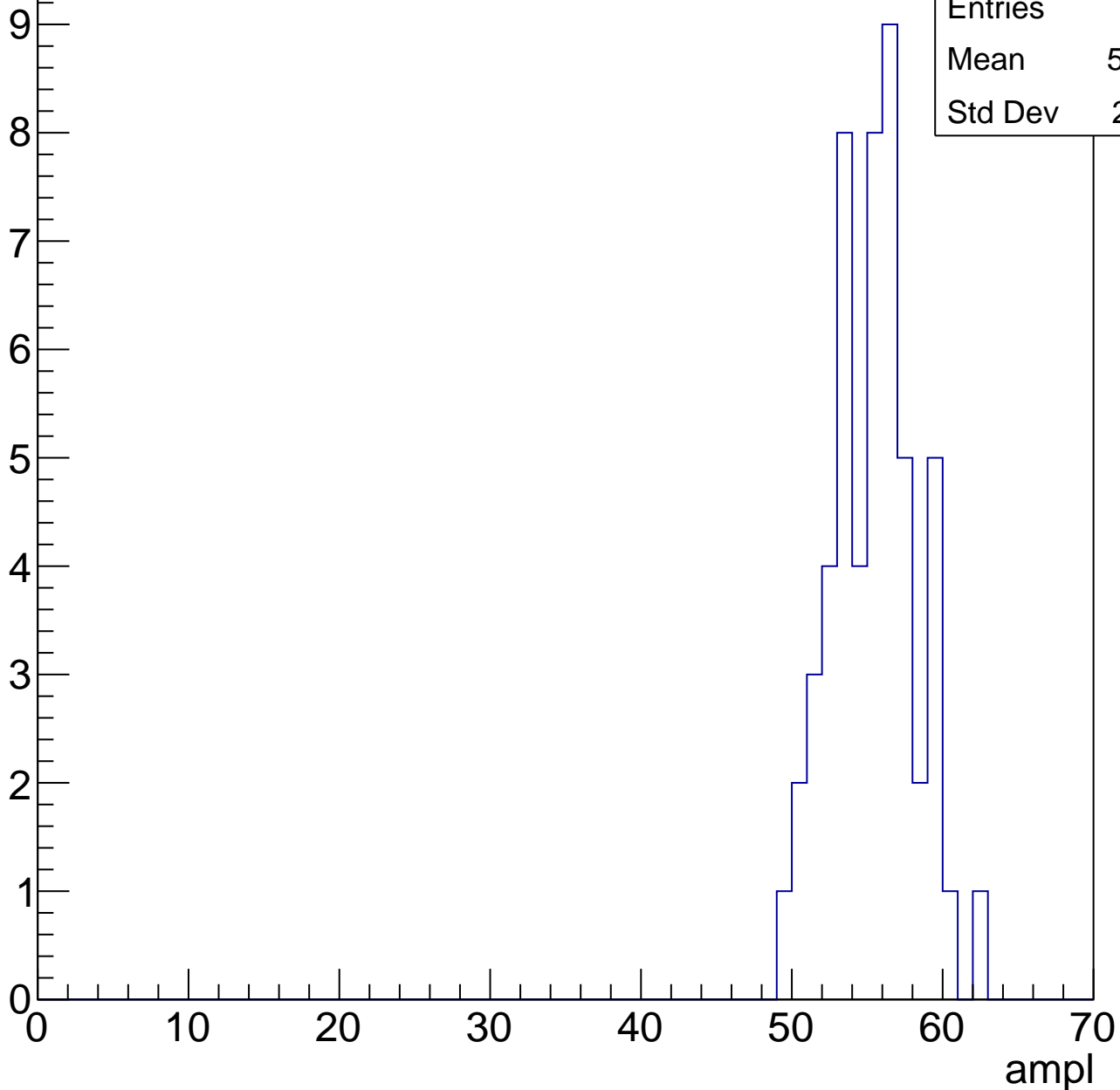


# B1L003S, U26-ch122, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	54.94
Std Dev	2.771



# B1L003S, U26-ch122, adc5

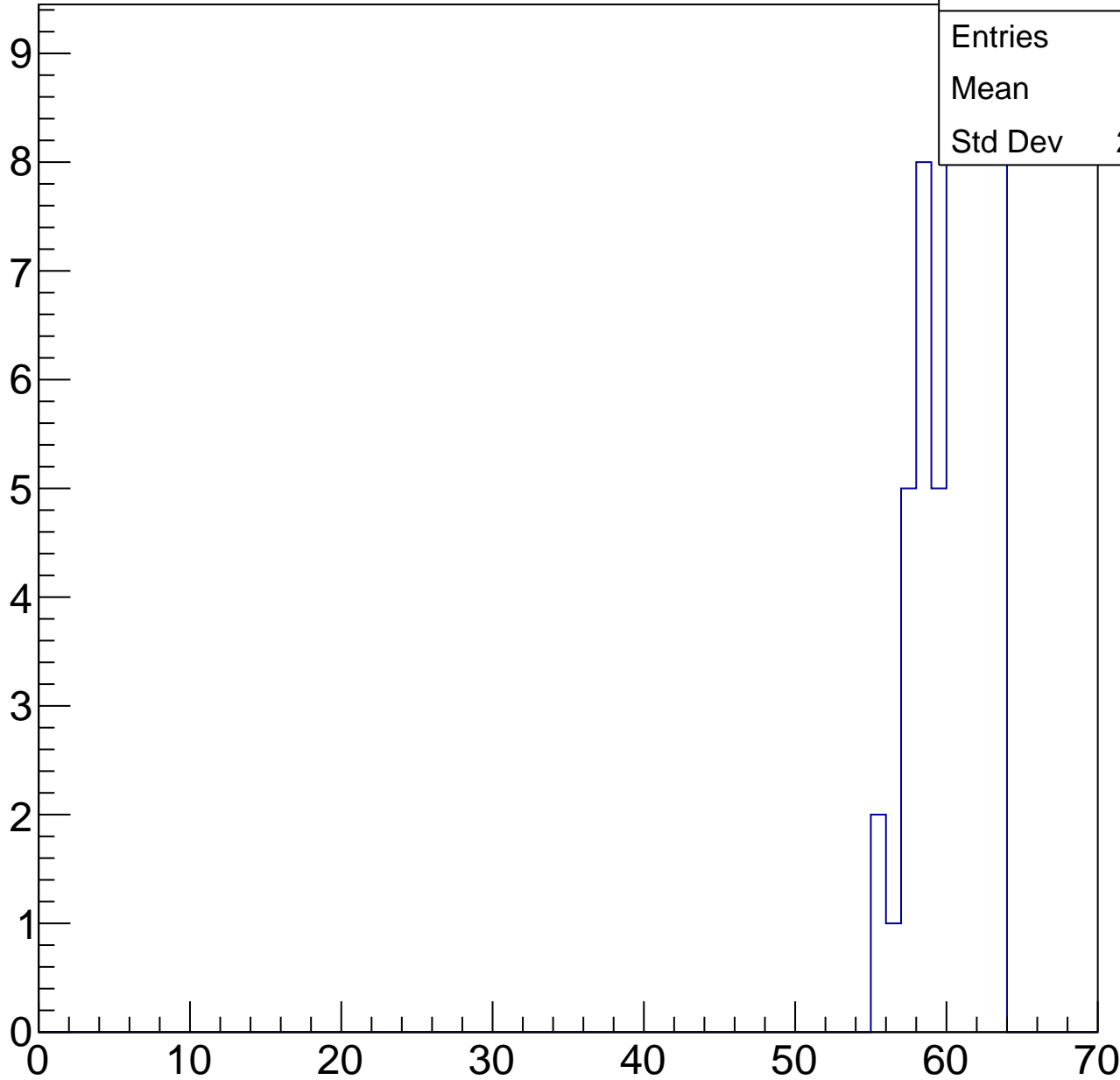
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	54
Mean	60
Std Dev	2.211

ampl



# B1L003S, U26-ch122, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

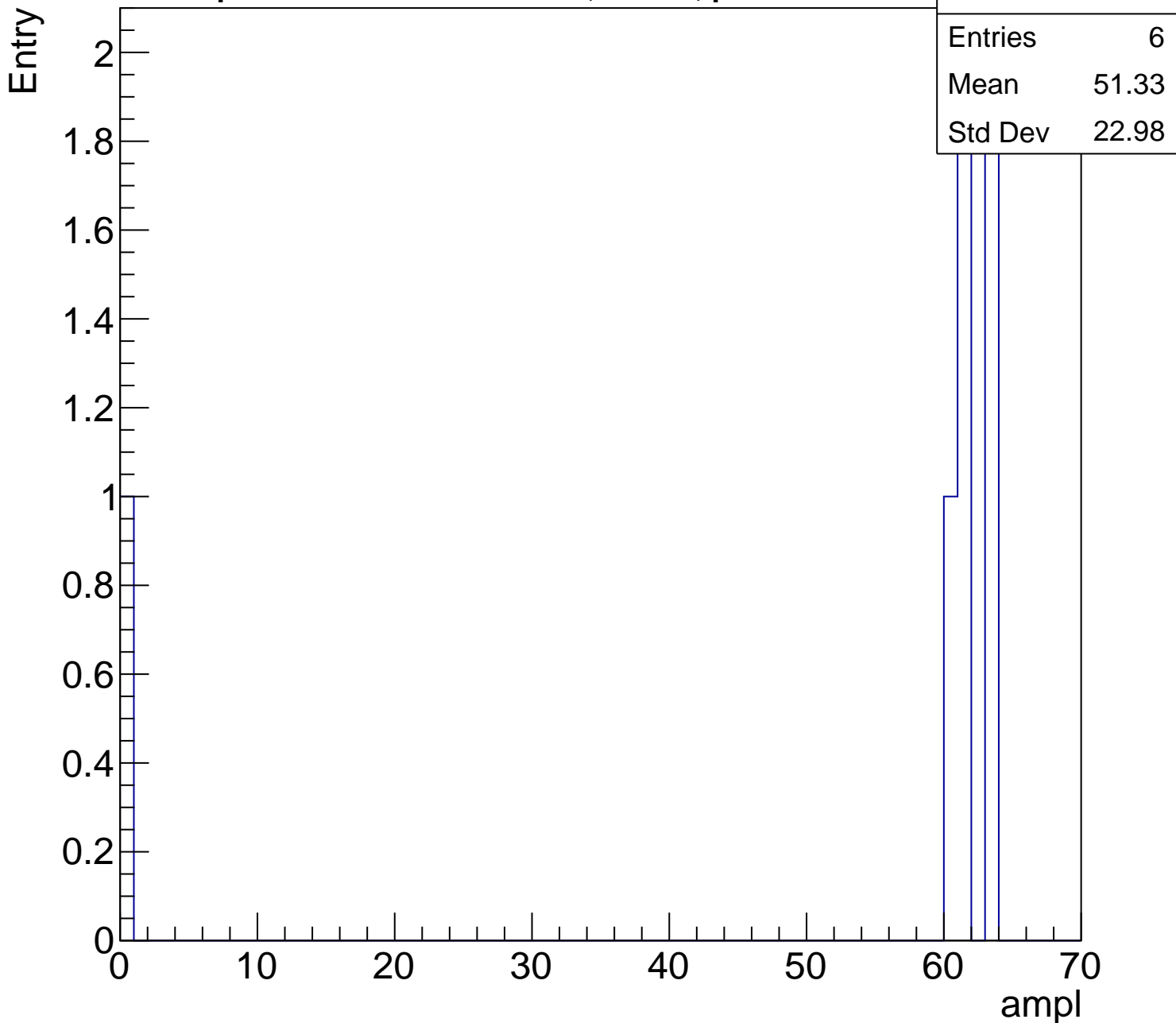
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	51.33
Std Dev	22.98

0 10 20 30 40 50 60 70

ampl





# B1L003S, U26-ch122, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U26-ch123, adc0

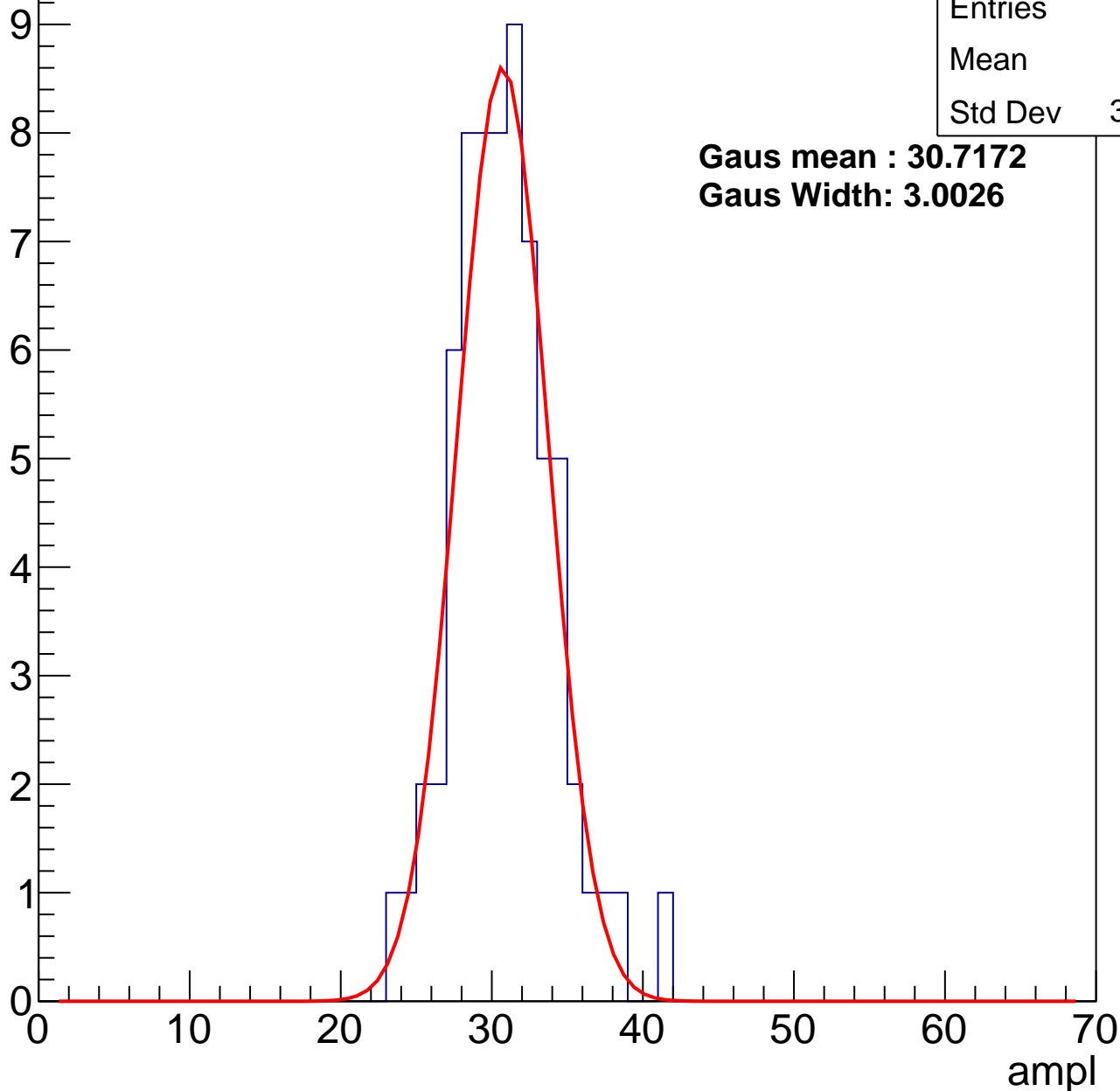
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	30.4
Std Dev	3.282

**Gaus mean : 30.7172**

**Gaus Width: 3.0026**



# B1L003S, U26-ch123, adc1

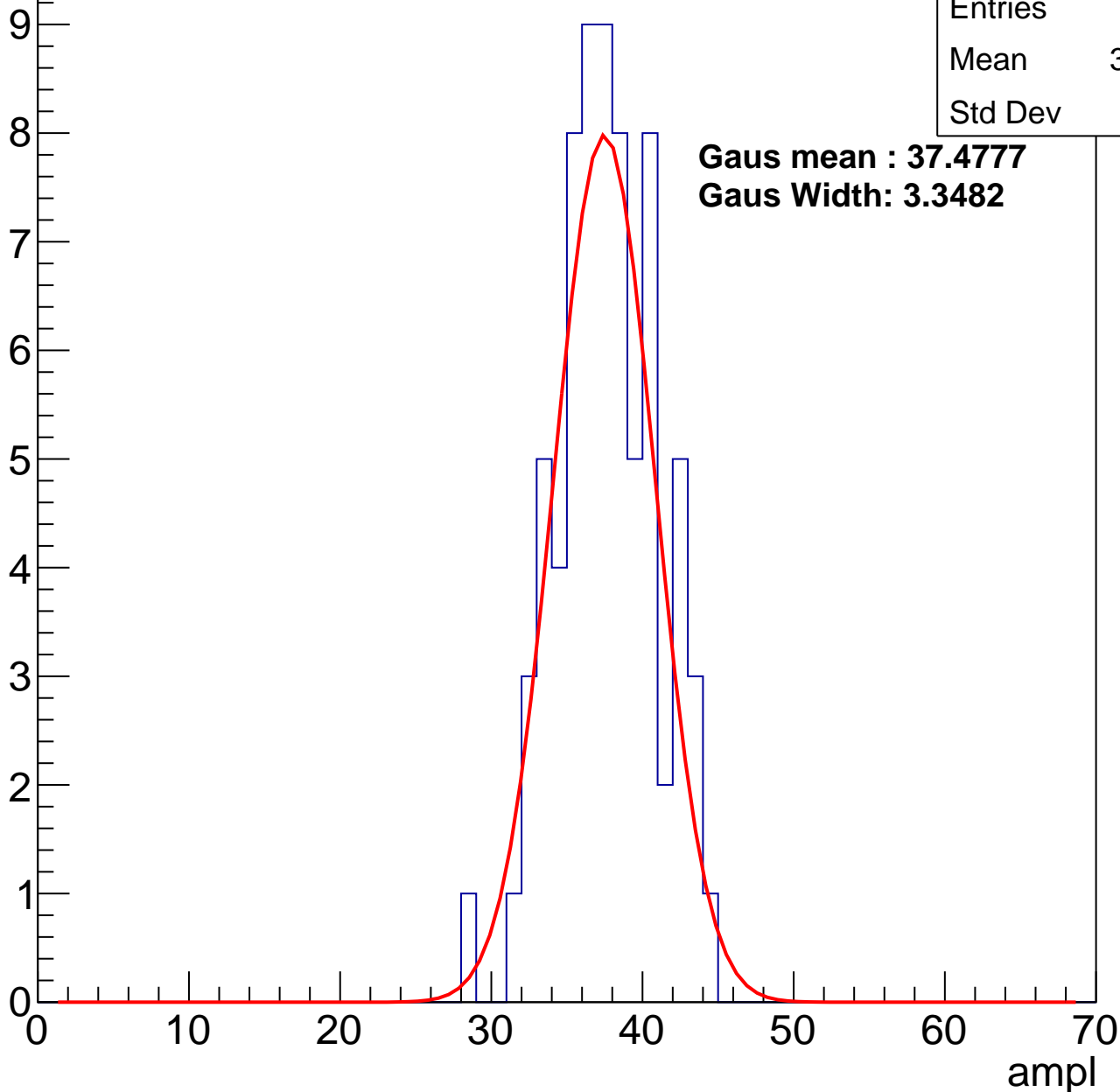
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	72
Mean	37.18
Std Dev	3.25

**Gaus mean : 37.4777**

**Gaus Width: 3.3482**



# B1L003S, U26-ch123, adc2

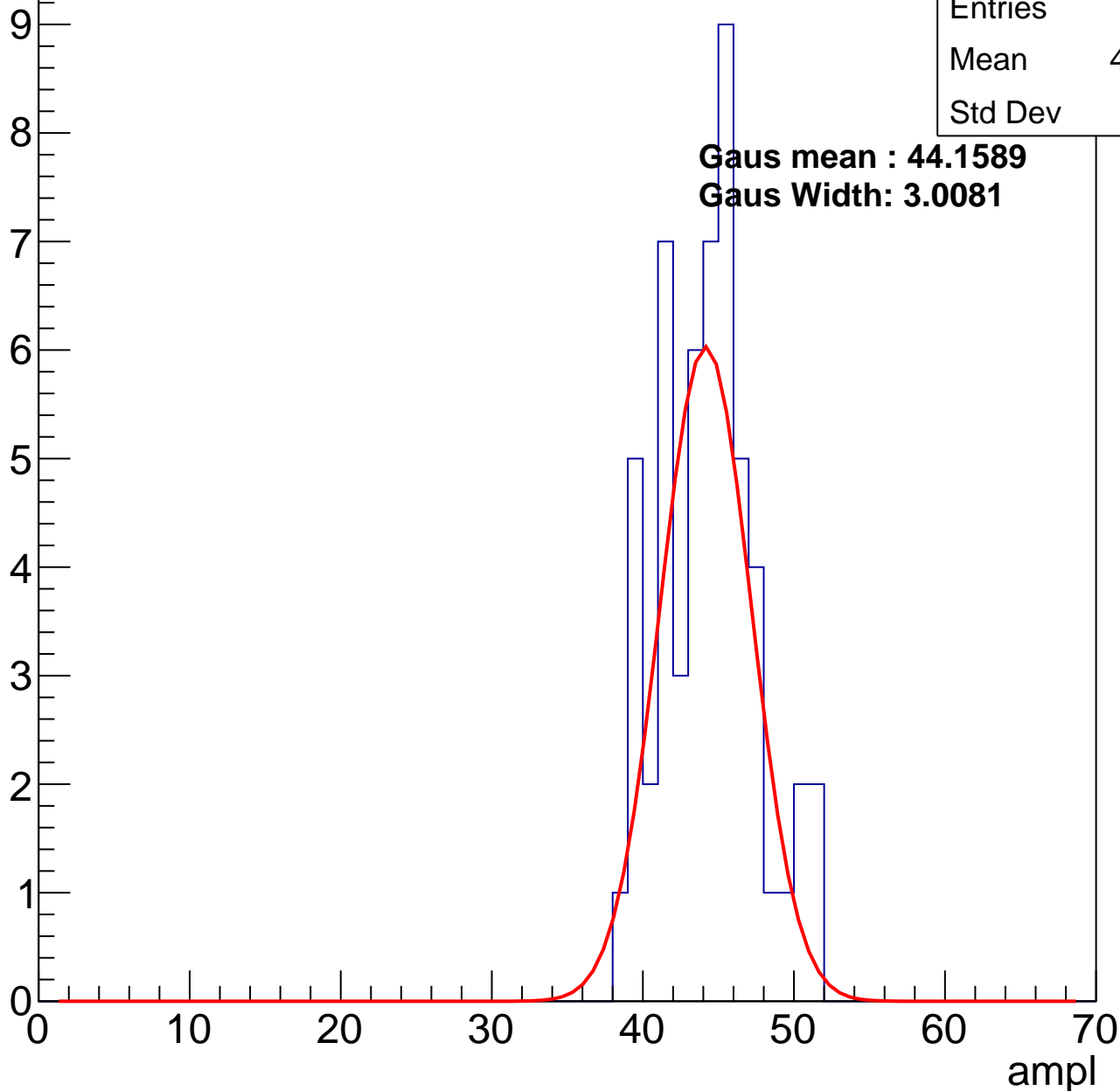
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	43.89
Std Dev	3.16

**Gaus mean : 44.1589**

**Gaus Width: 3.0081**

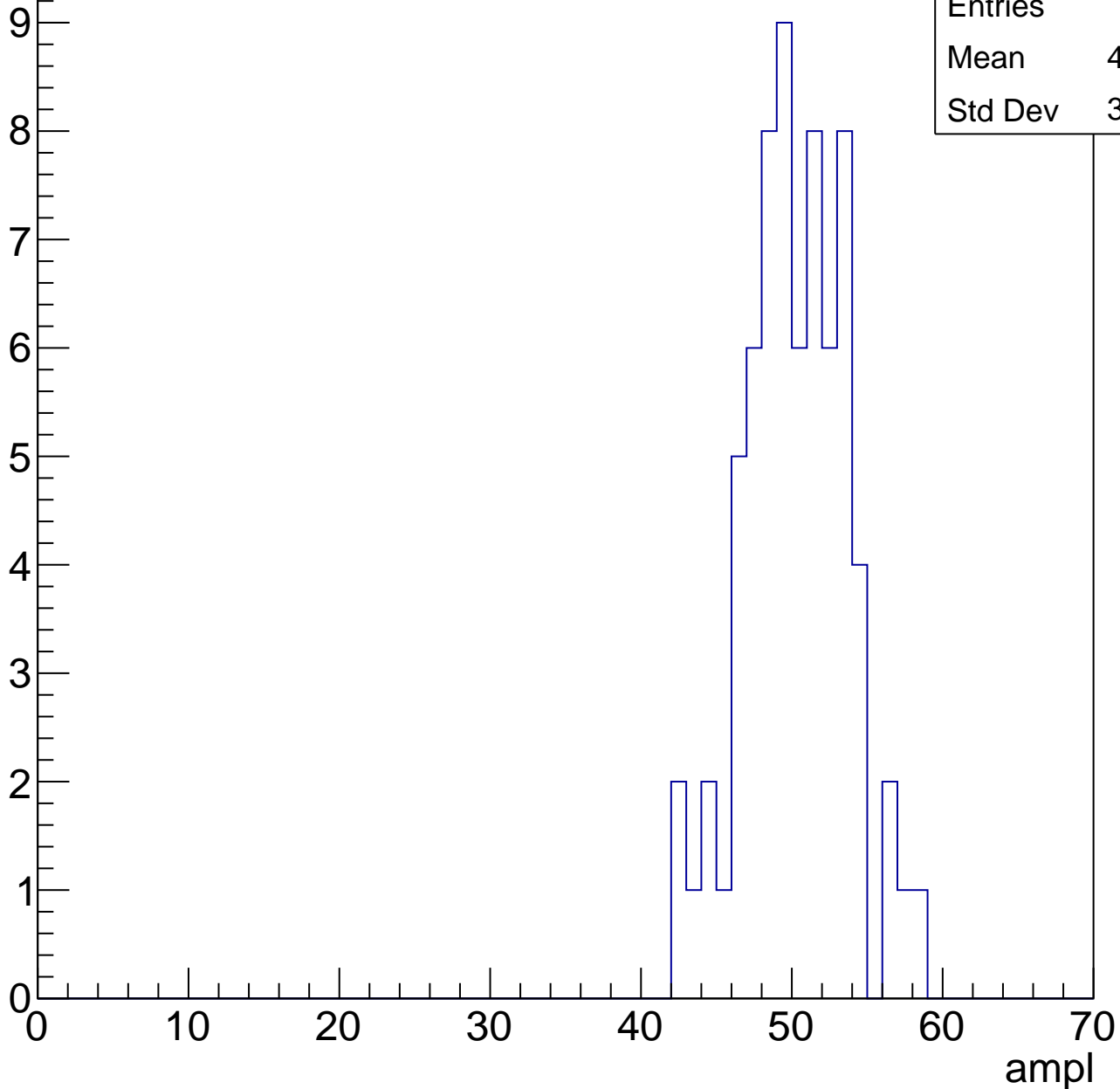


# B1L003S, U26-ch123, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	49.77
Std Dev	3.377

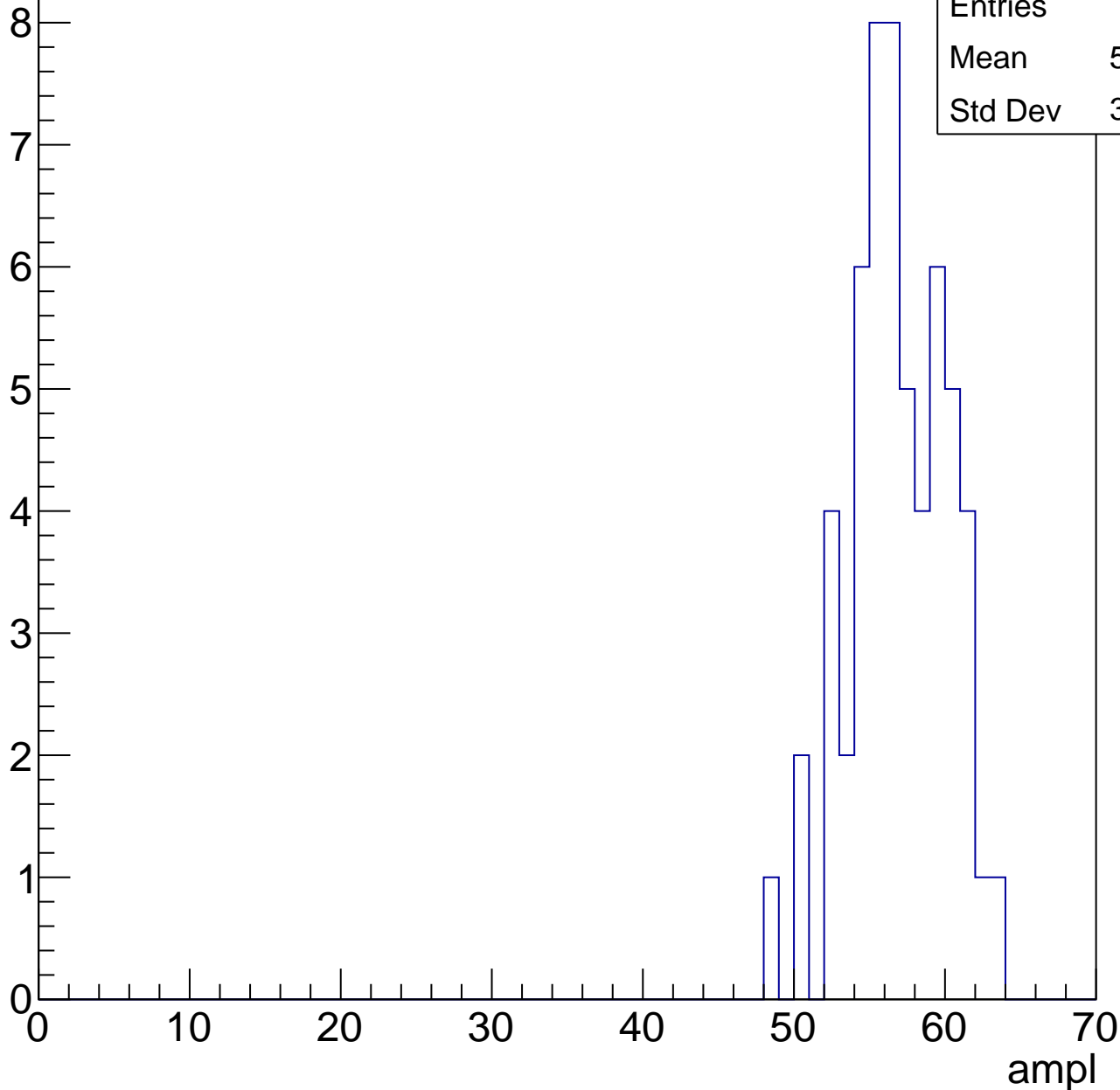


# B1L003S, U26-ch123, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	56.39
Std Dev	3.194

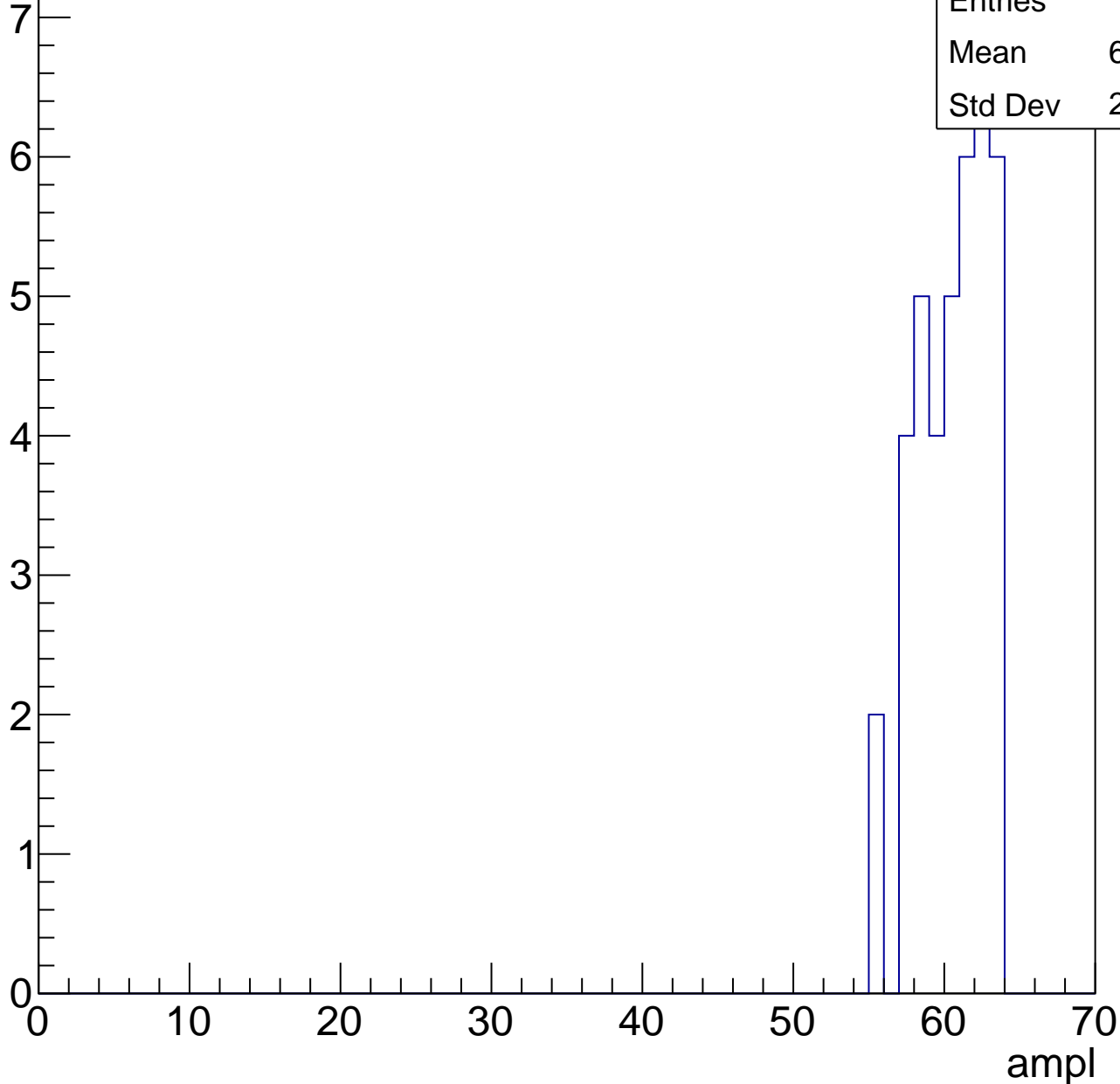


# B1L003S, U26-ch123, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

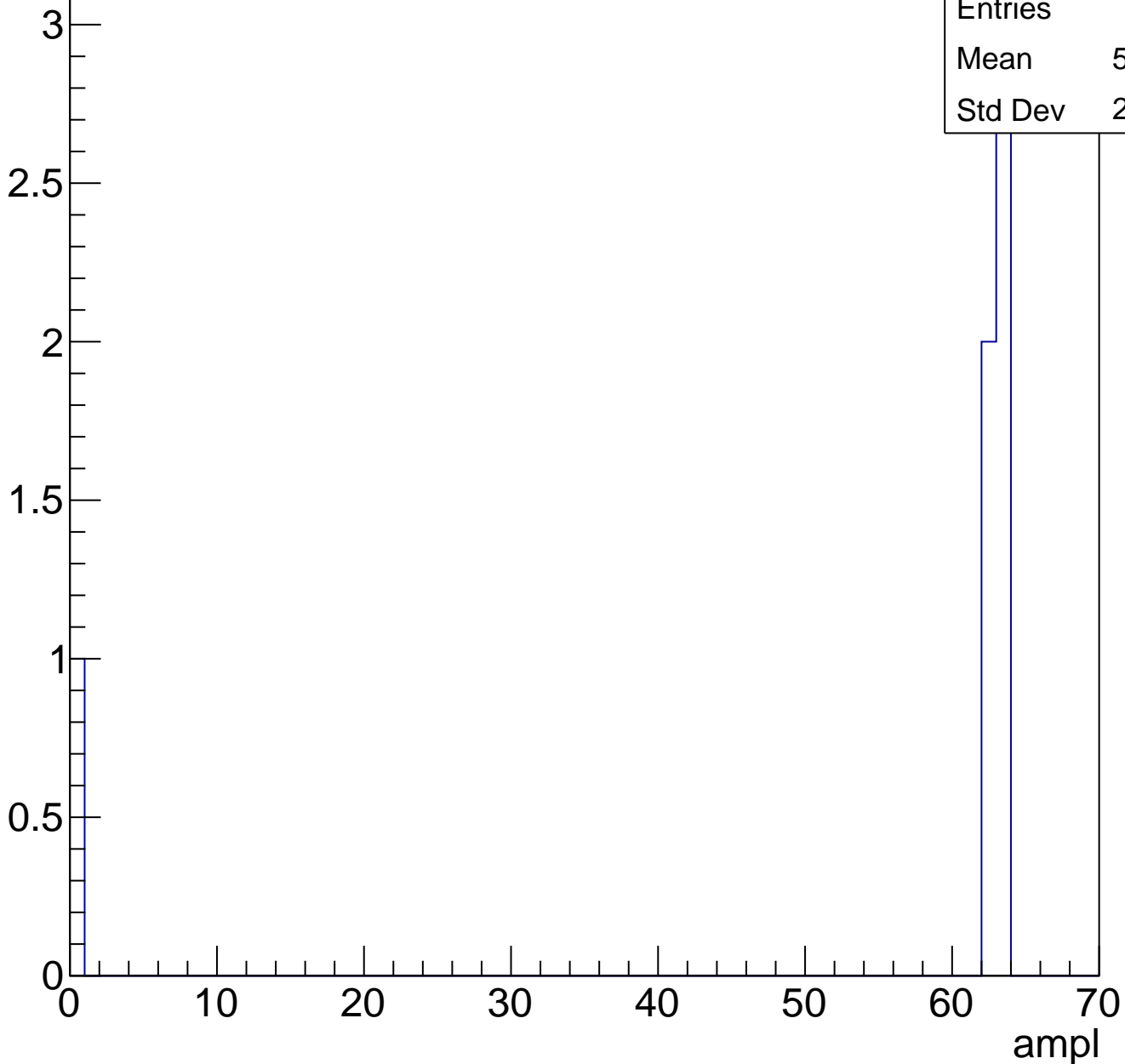
Entries	39
Mean	60.05
Std Dev	2.253



# B1L003S, U26-ch123, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch123, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L003S, U26-ch124, adc0

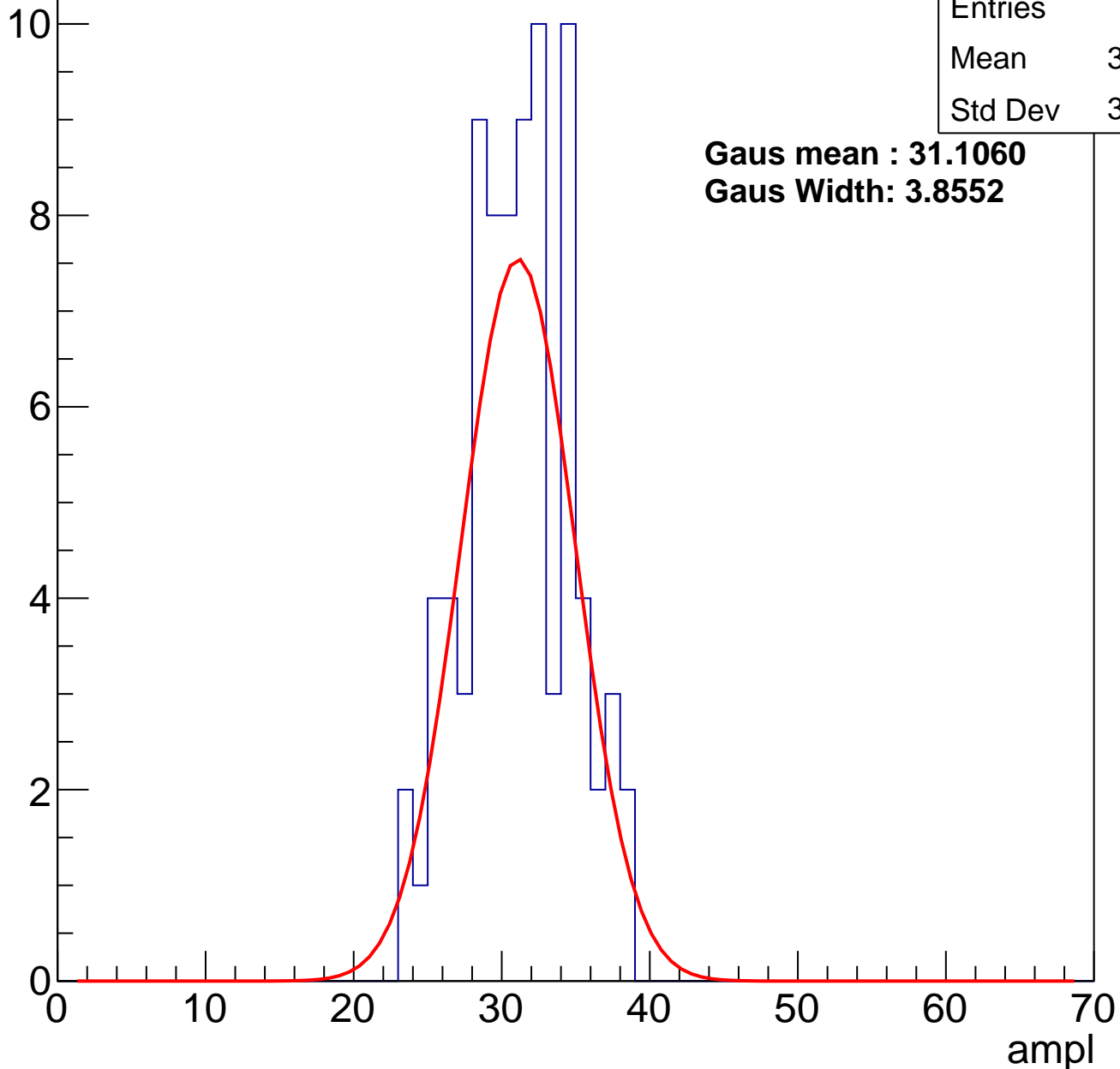
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	82
Mean	30.68
Std Dev	3.516

**Gaus mean : 31.1060**

**Gaus Width: 3.8552**

Entry



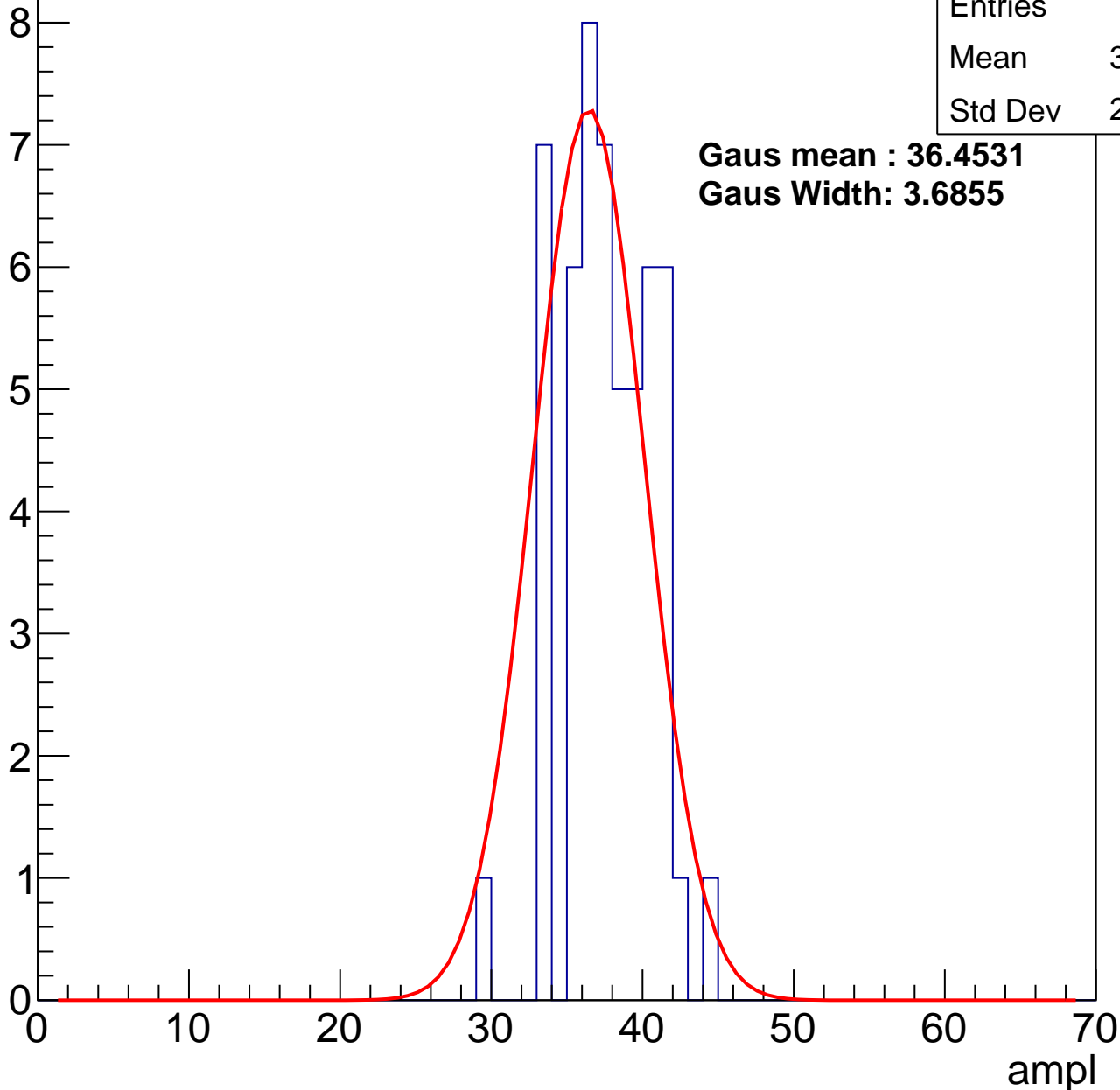
# B1L003S, U26-ch124, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	37.25
Std Dev	2.926

**Gaus mean : 36.4531**  
**Gaus Width: 3.6855**



# B1L003S, U26-ch124, adc2

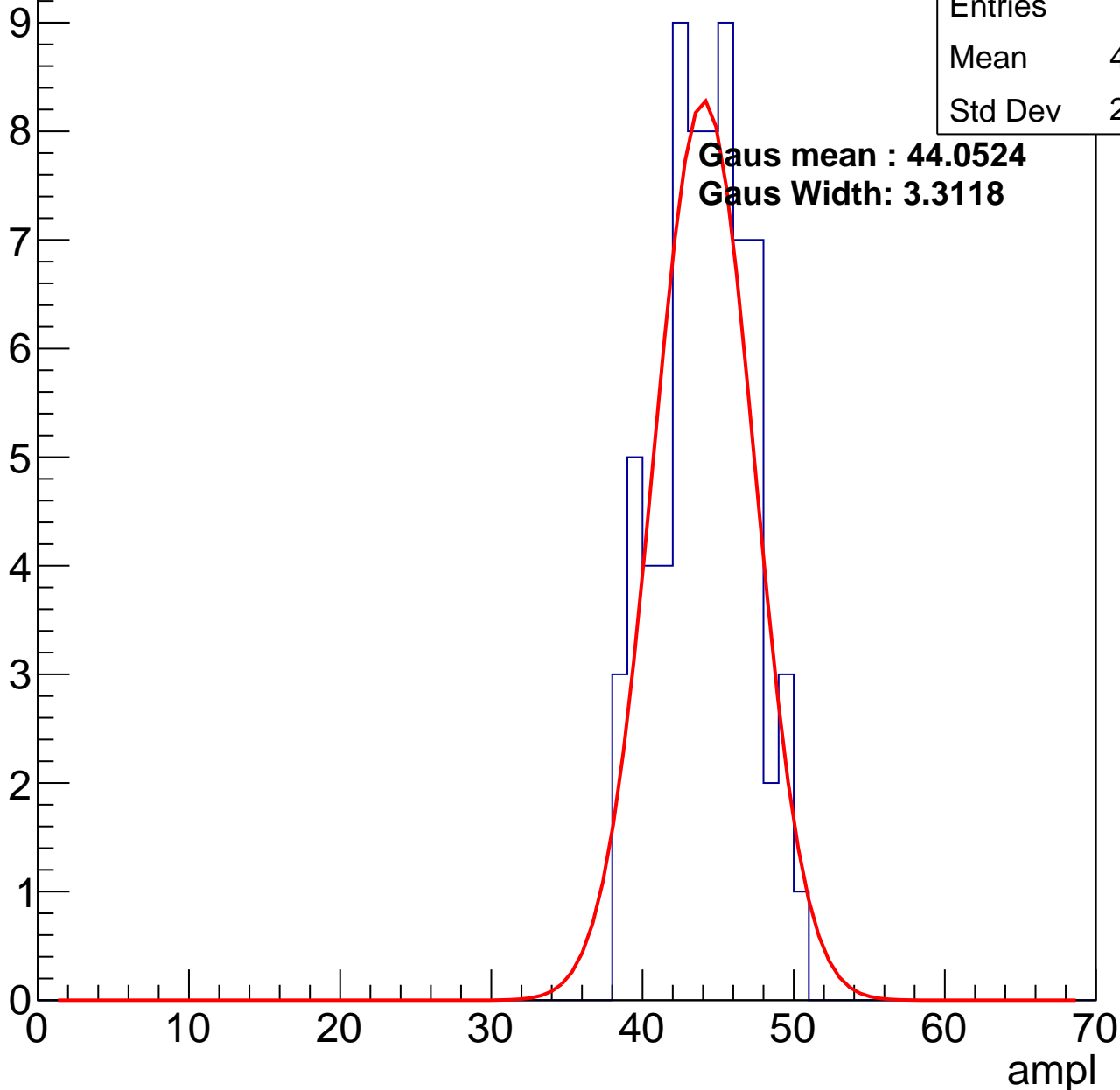
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	43.66
Std Dev	2.956

**Gaus mean : 44.0524**

**Gaus Width: 3.3118**

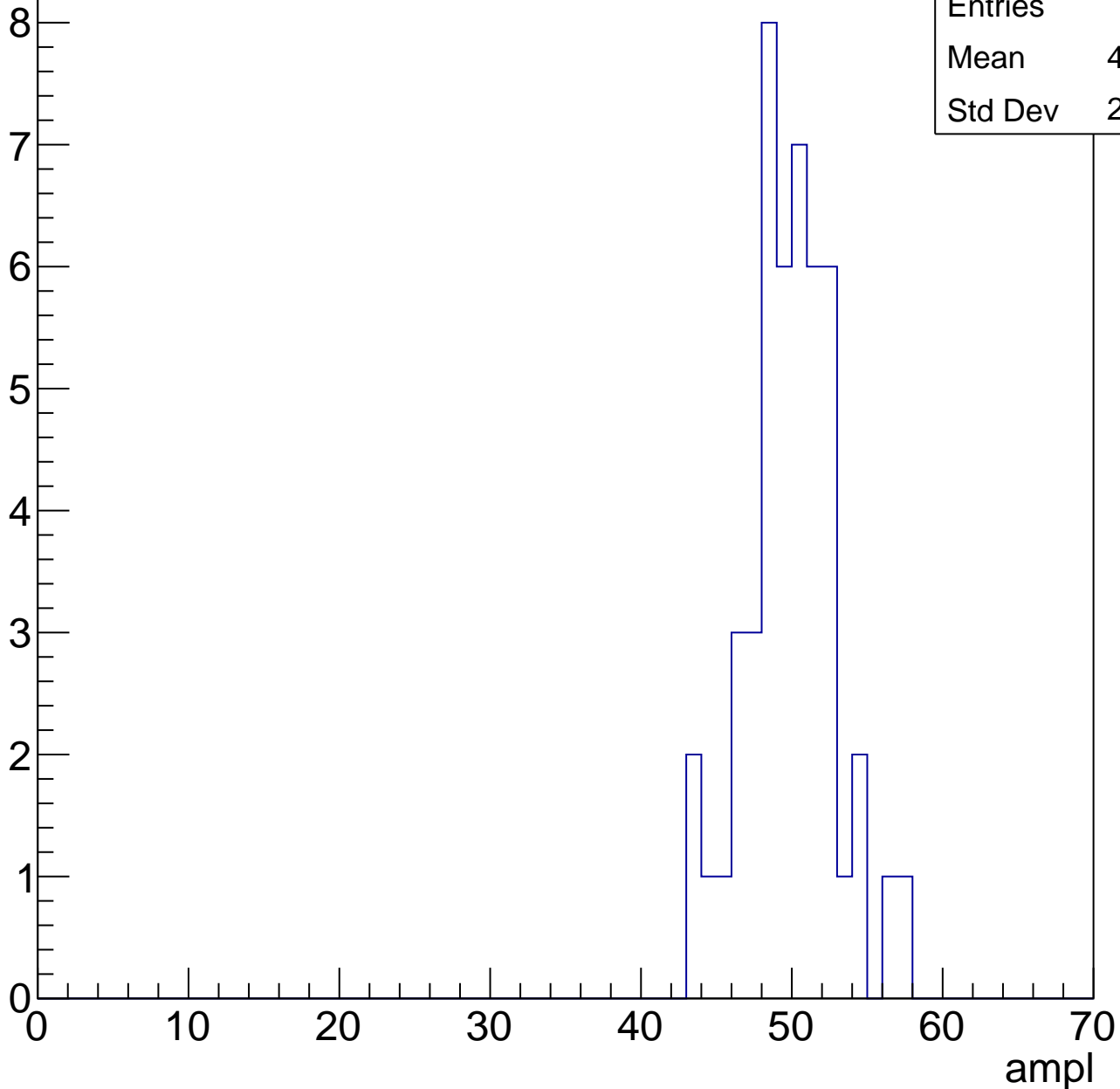


# B1L003S, U26-ch124, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	48
Mean	49.46
Std Dev	2.937

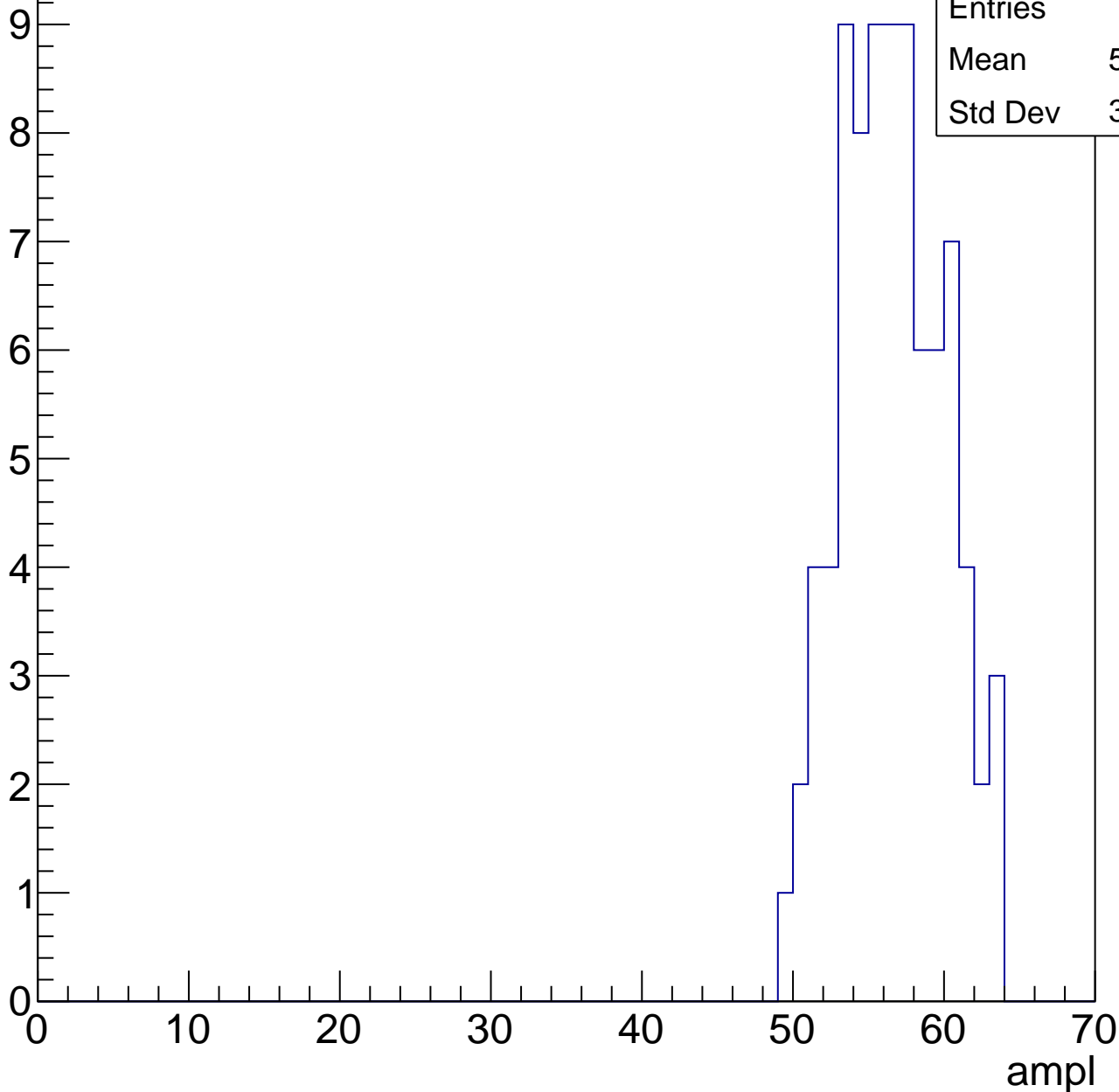


# B1L003S, U26-ch124, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	83
Mean	56.16
Std Dev	3.335

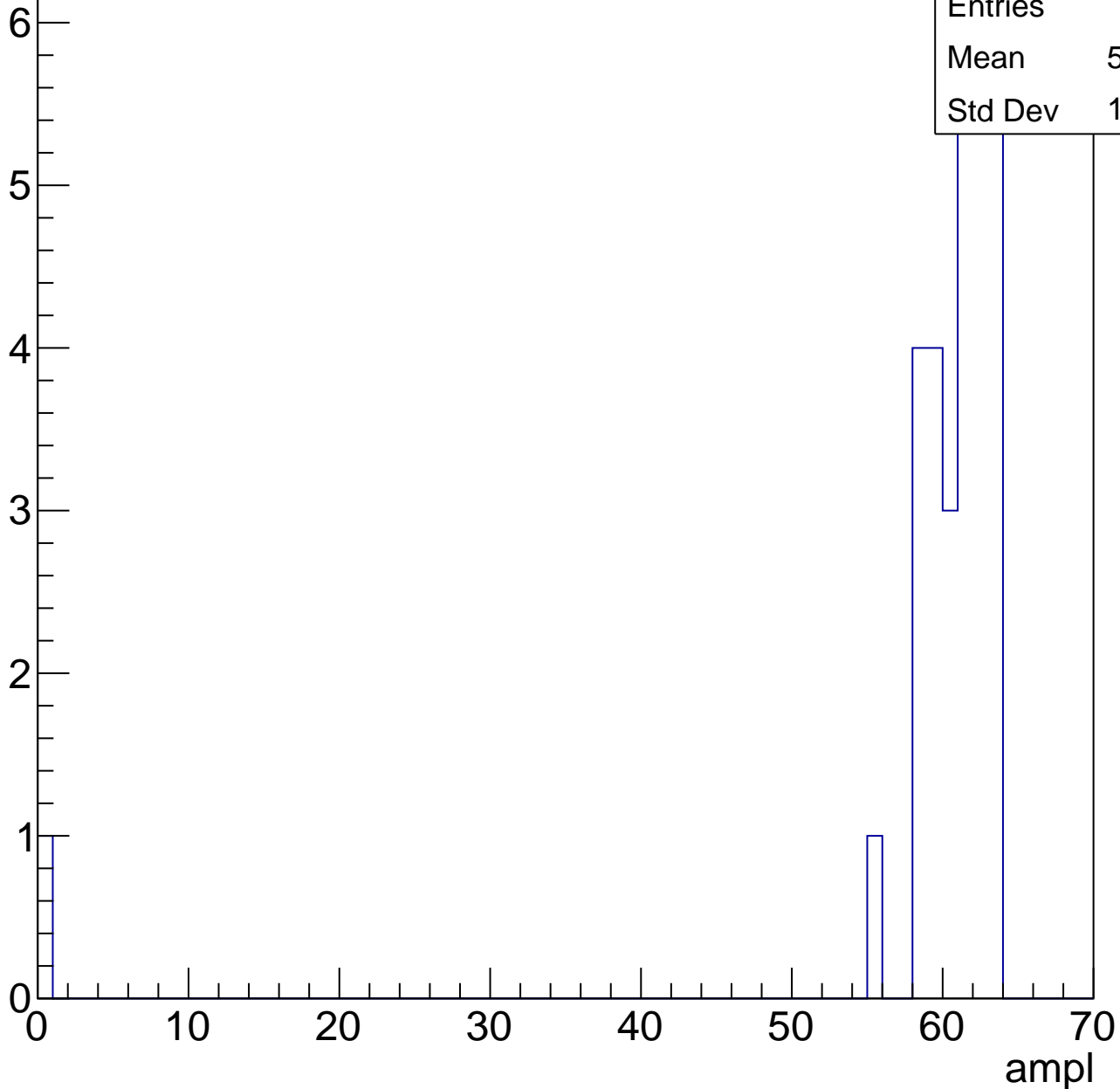


# B1L003S, U26-ch124, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	31
Mean	58.68
Std Dev	10.89



# B1L003S, U26-ch124, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.33
Std Dev	0.4714

ampl



# B1L003S, U26-ch124, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U26-ch125, adc0

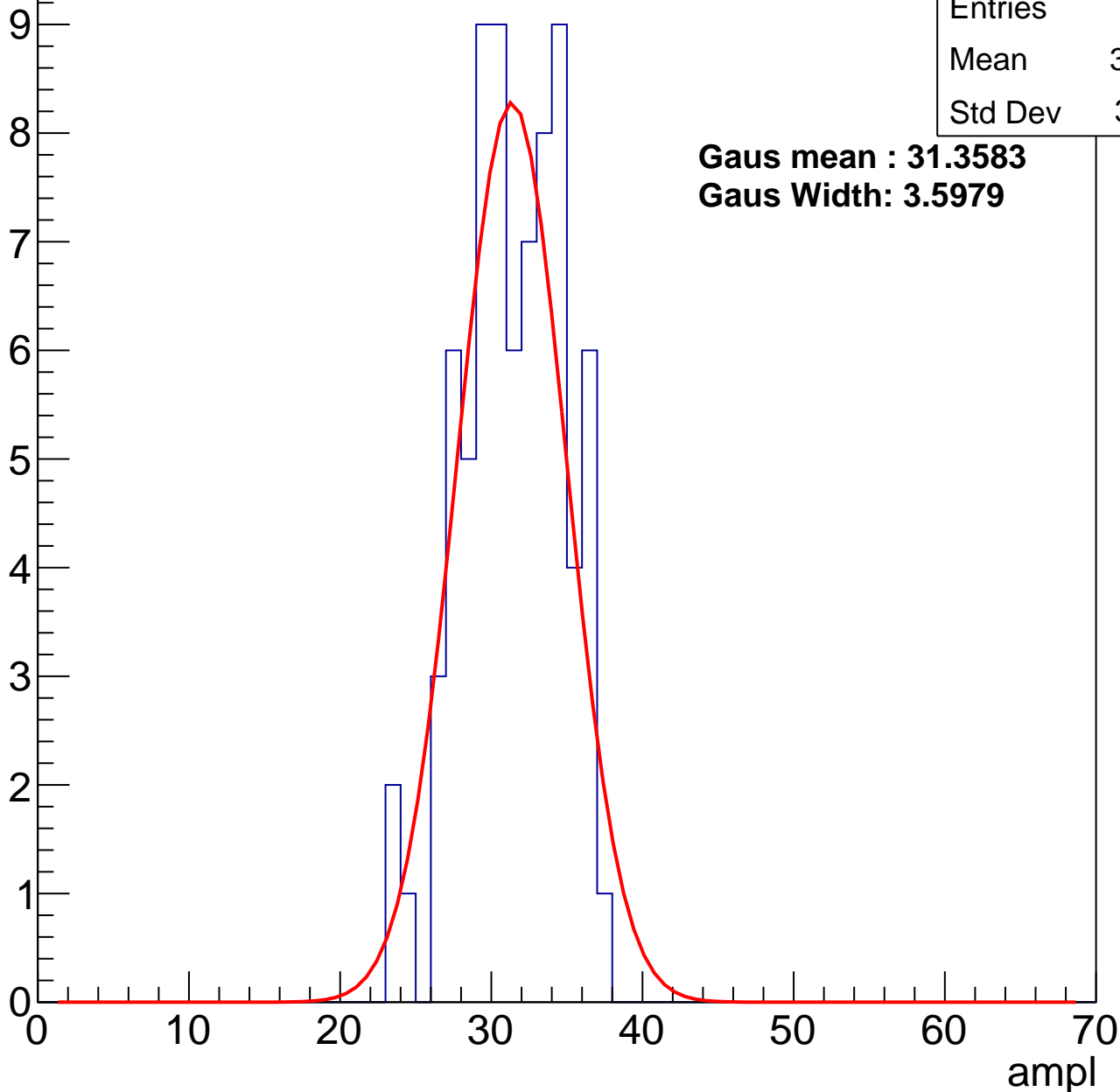
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	76
Mean	30.97
Std Dev	3.261

**Gaus mean : 31.3583**

**Gaus Width: 3.5979**



# B1L003S, U26-ch125, adc1

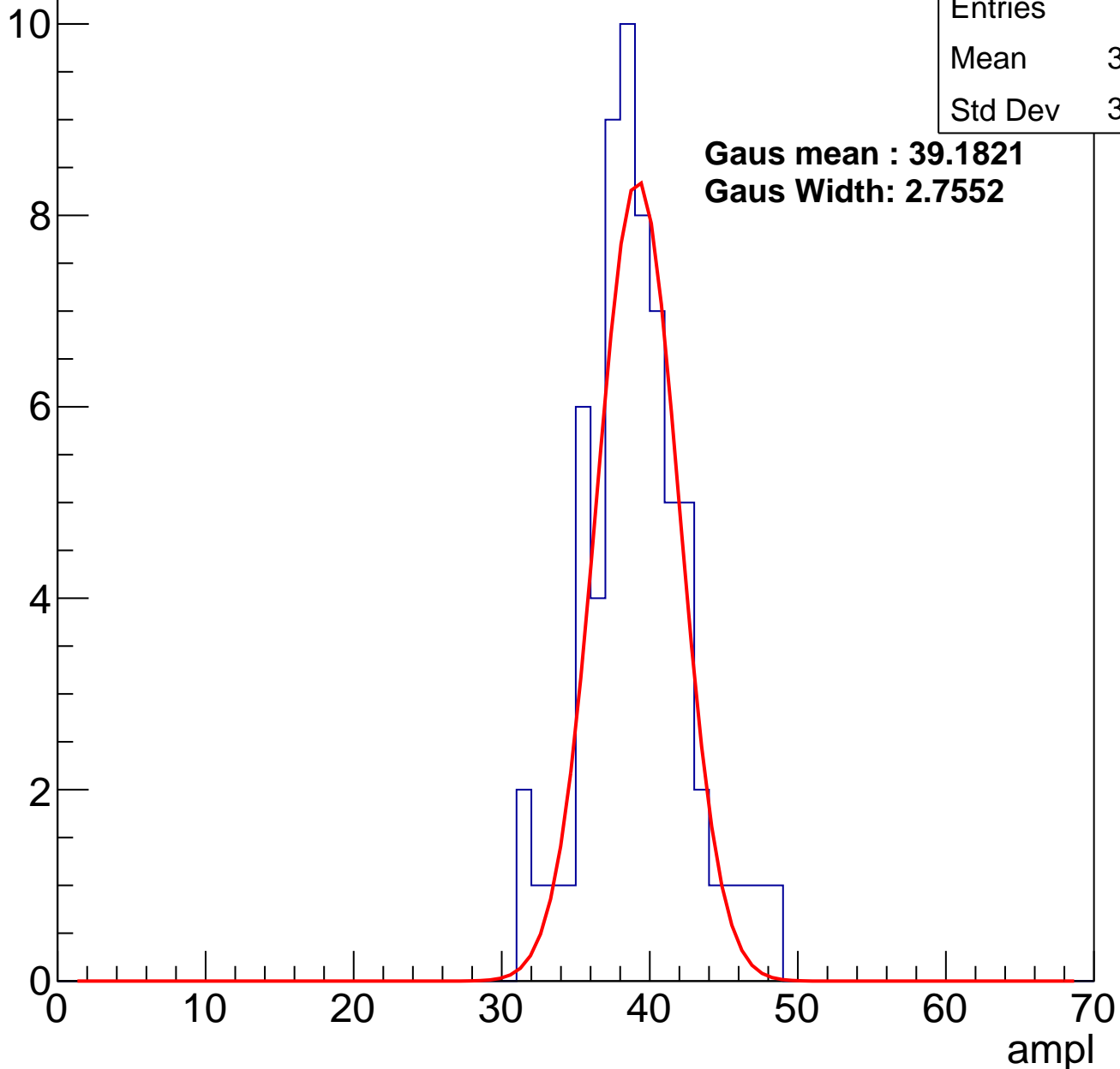
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	66
Mean	38.65
Std Dev	3.409

**Gaus mean : 39.1821**

**Gaus Width: 2.7552**

Entry



# B1L003S, U26-ch125, adc2

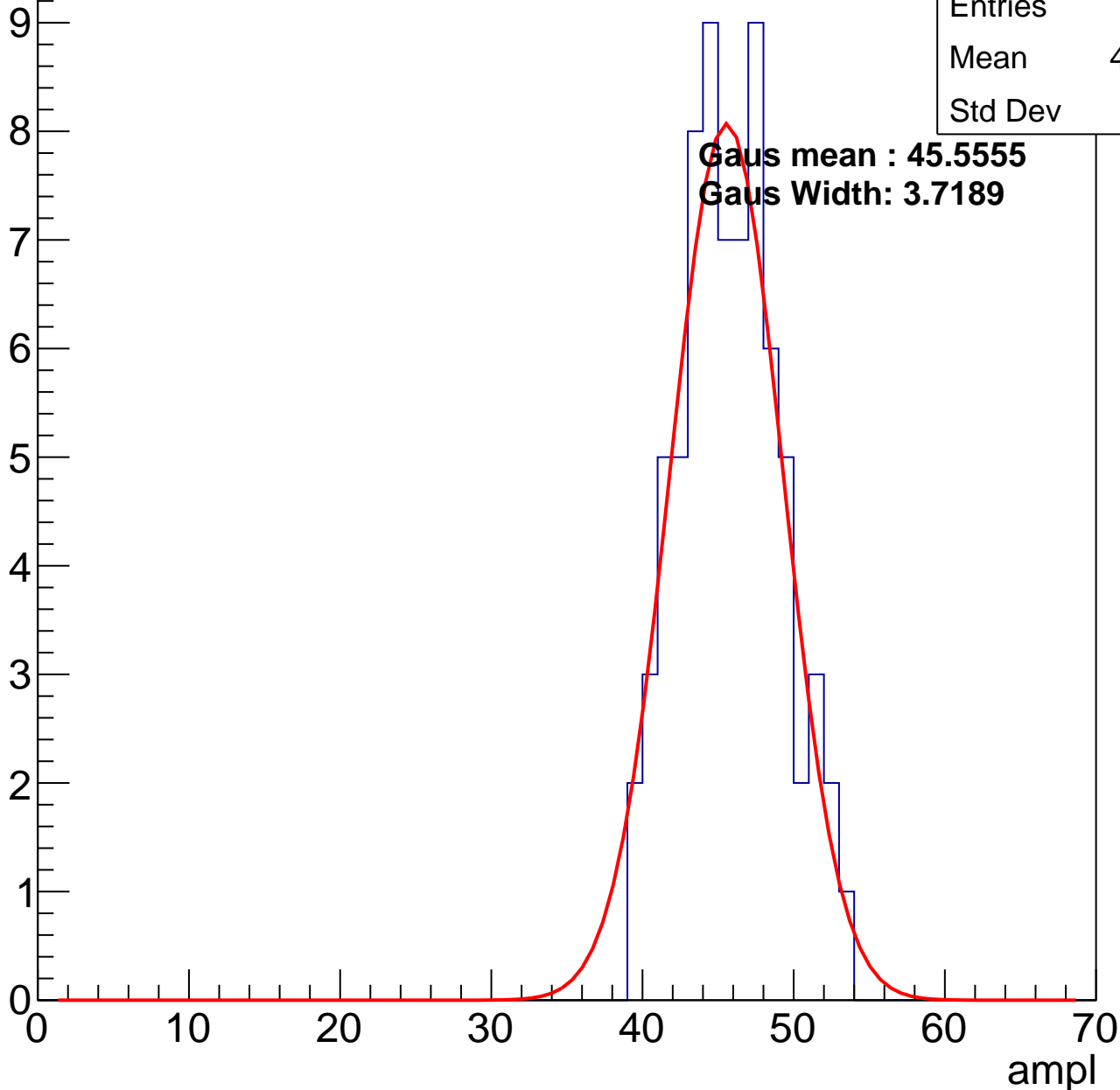
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	74
Mean	45.35
Std Dev	3.29

**Gaus mean : 45.5555**

**Gaus Width: 3.7189**

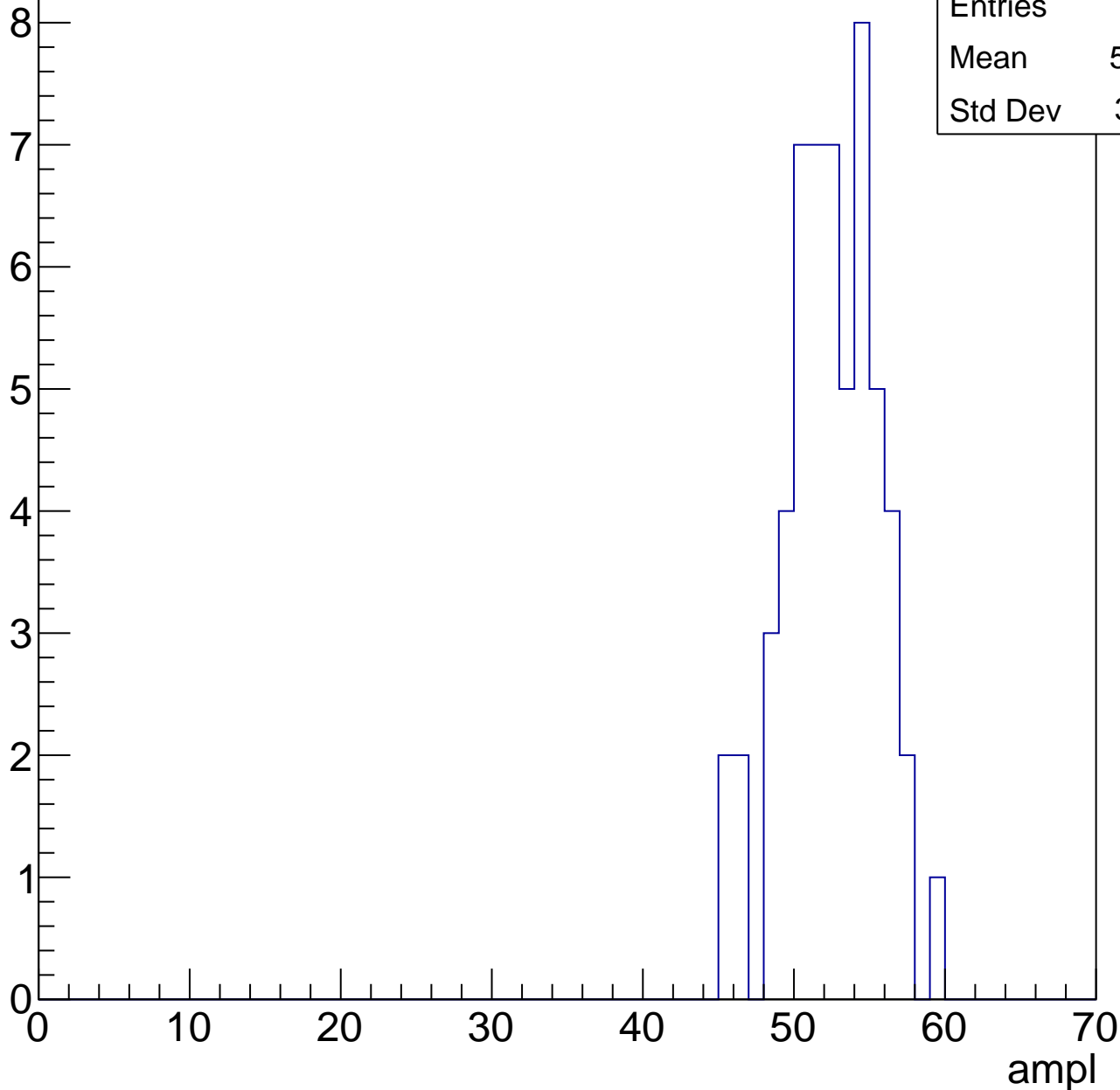


# B1L003S, U26-ch125, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

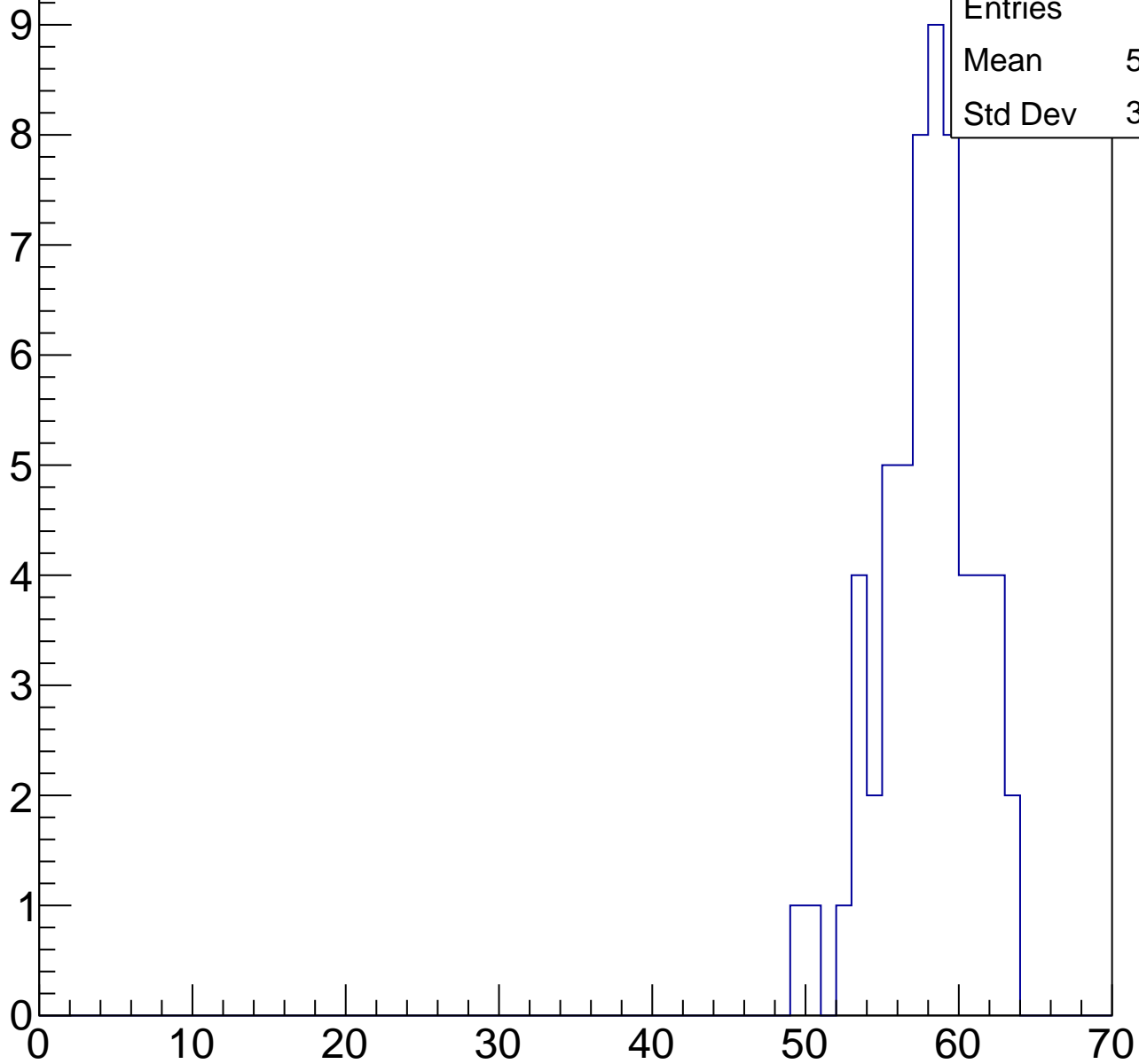
Entries	57
Mean	51.96
Std Dev	3.061



# B1L003S, U26-ch125, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	58
Mean	57.48
Std Dev	3.064

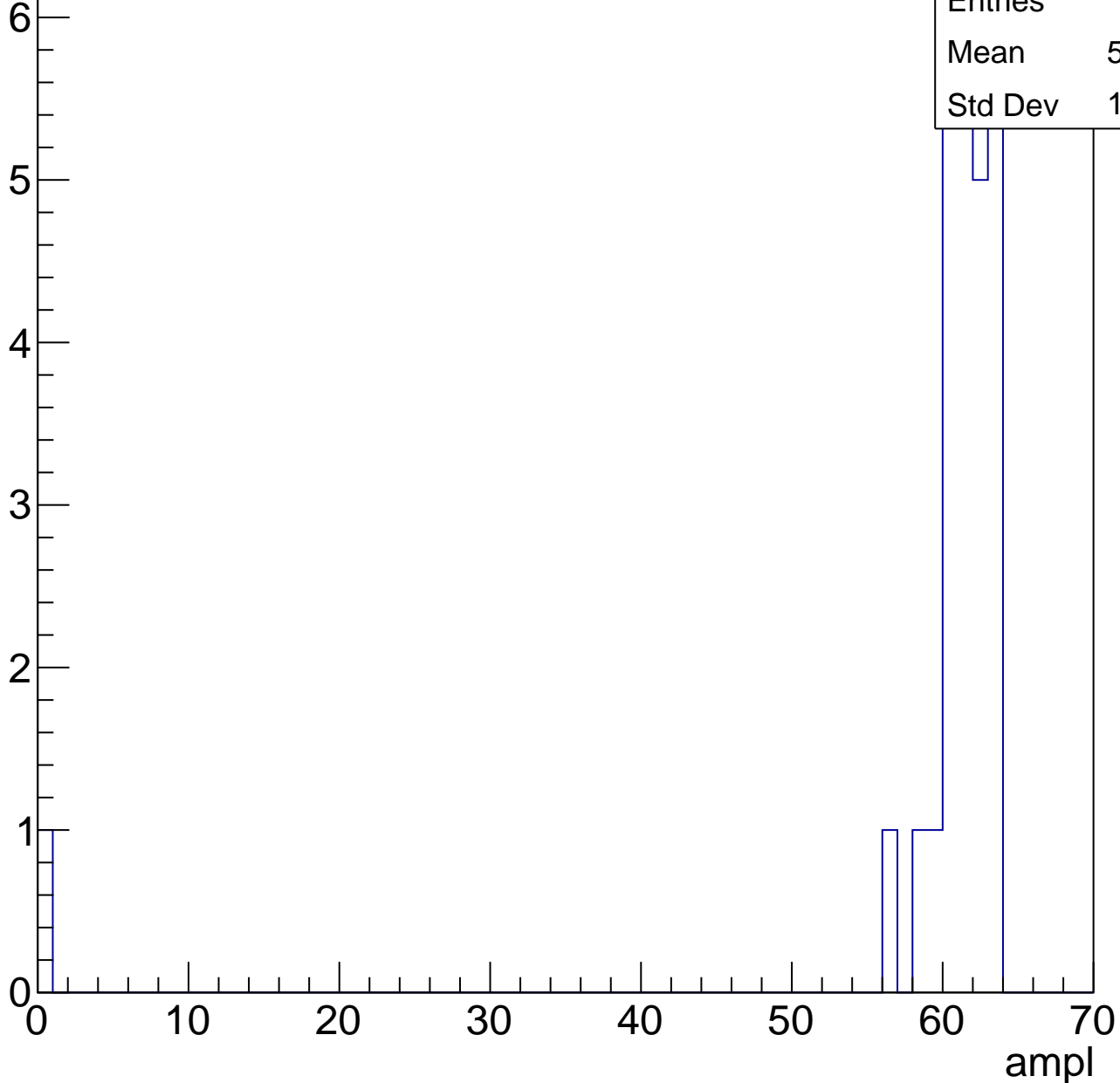
ampl

# B1L003S, U26-ch125, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	27
Mean	58.78
Std Dev	11.64



# B1L003S, U26-ch125, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch125, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U26-ch126, adc0

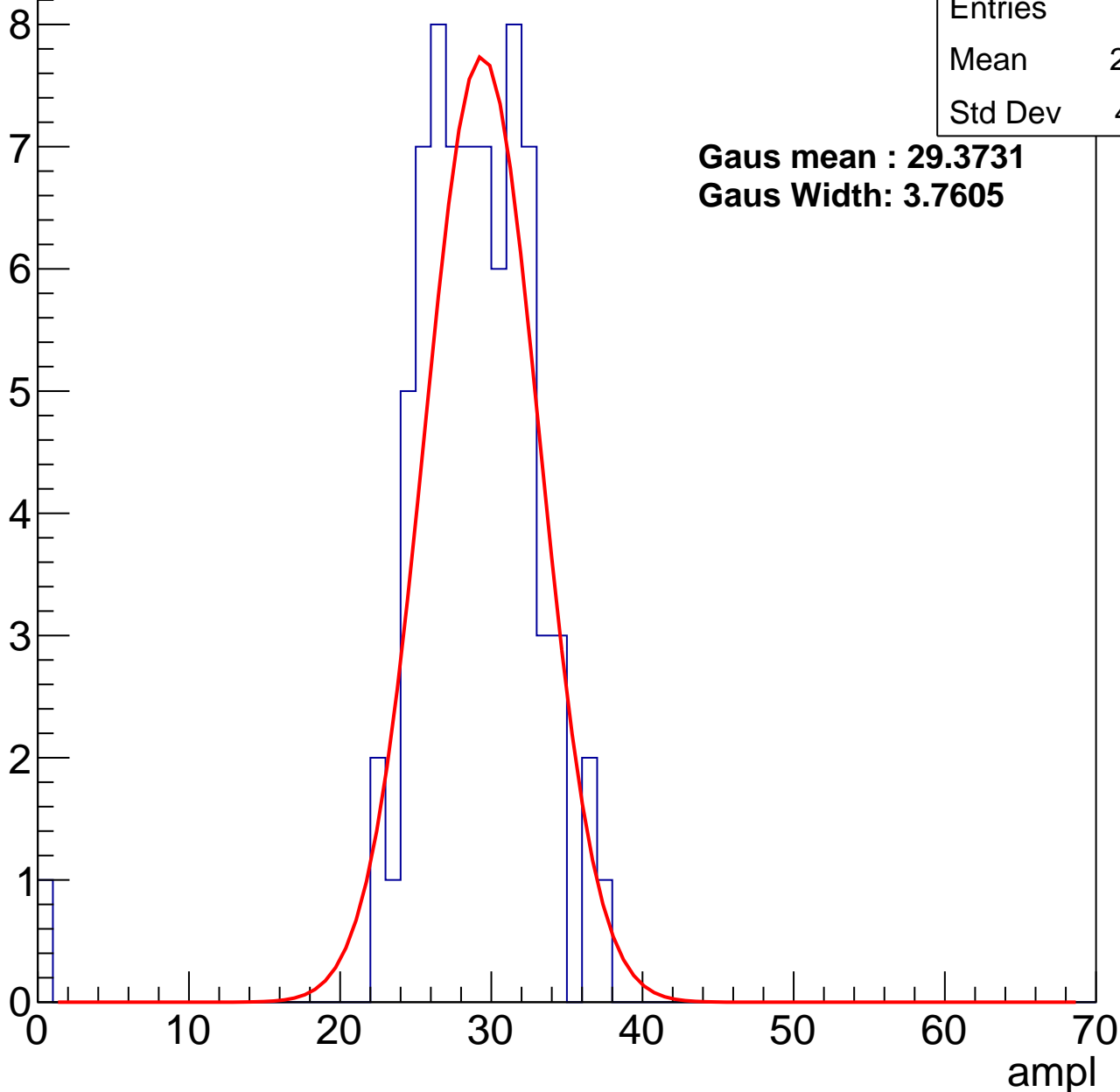
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	75
Mean	28.27
Std Dev	4.711

**Gaus mean : 29.3731**

**Gaus Width: 3.7605**



# B1L003S, U26-ch126, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	53
Mean	34.96
Std Dev	3.308

**Gaus mean : 35.2577**

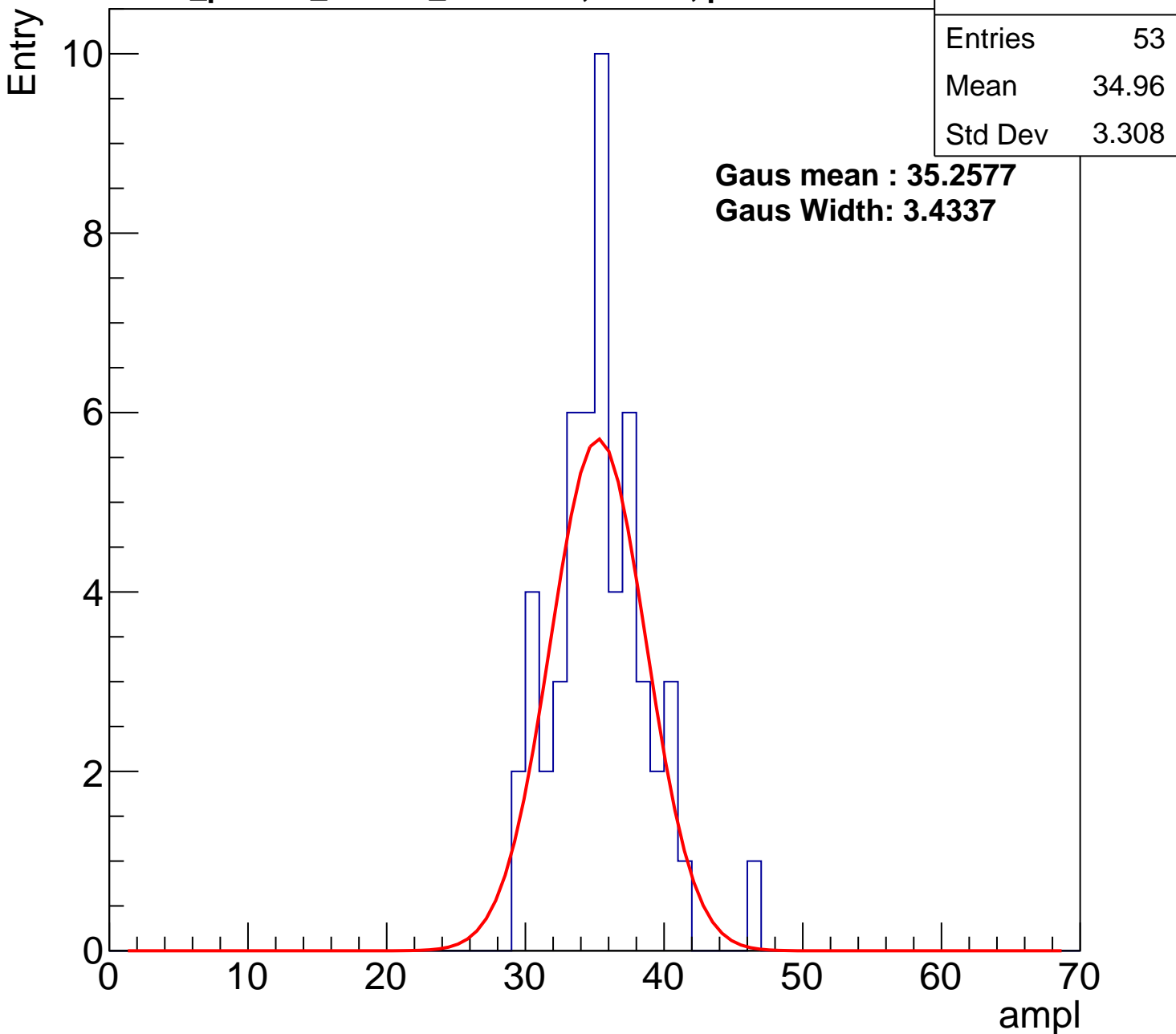
**Gaus Width: 3.4337**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U26-ch126, adc2

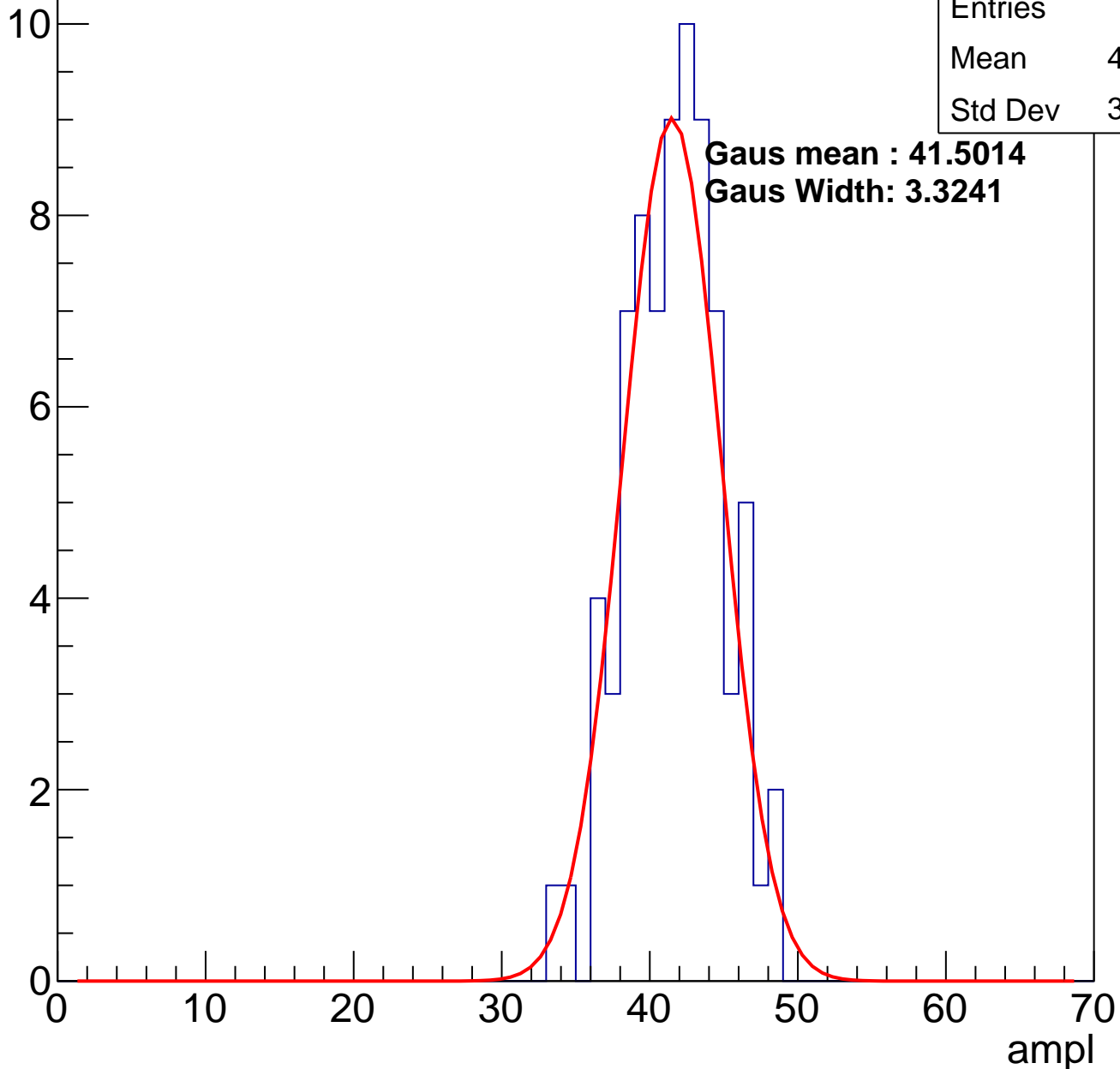
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	77
Mean	41.19
Std Dev	3.175

**Gaus mean : 41.5014**

**Gaus Width: 3.3241**

Entry

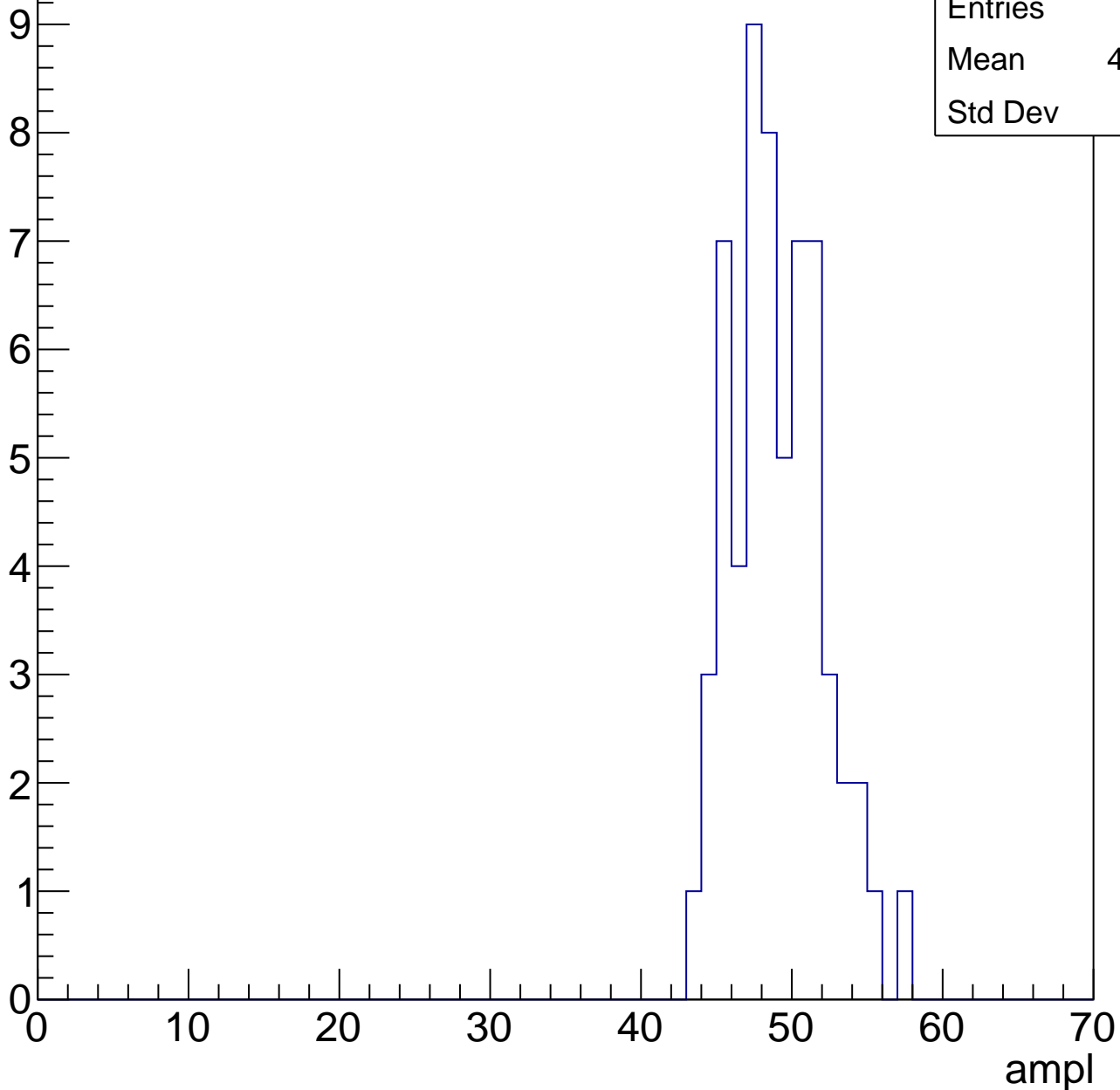


# B1L003S, U26-ch126, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	48.58
Std Dev	2.99

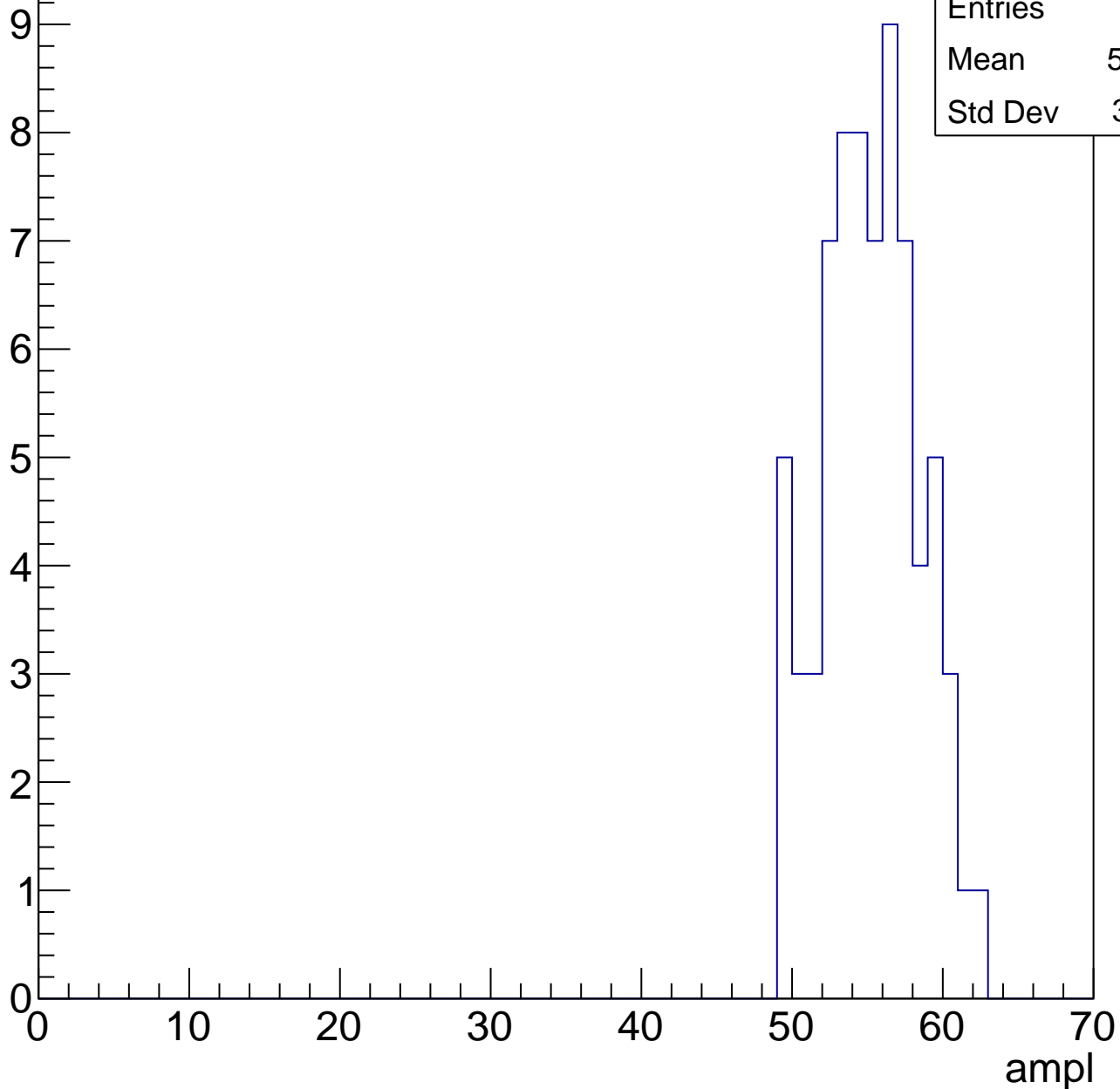


# B1L003S, U26-ch126, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	71
Mean	54.73
Std Dev	3.171

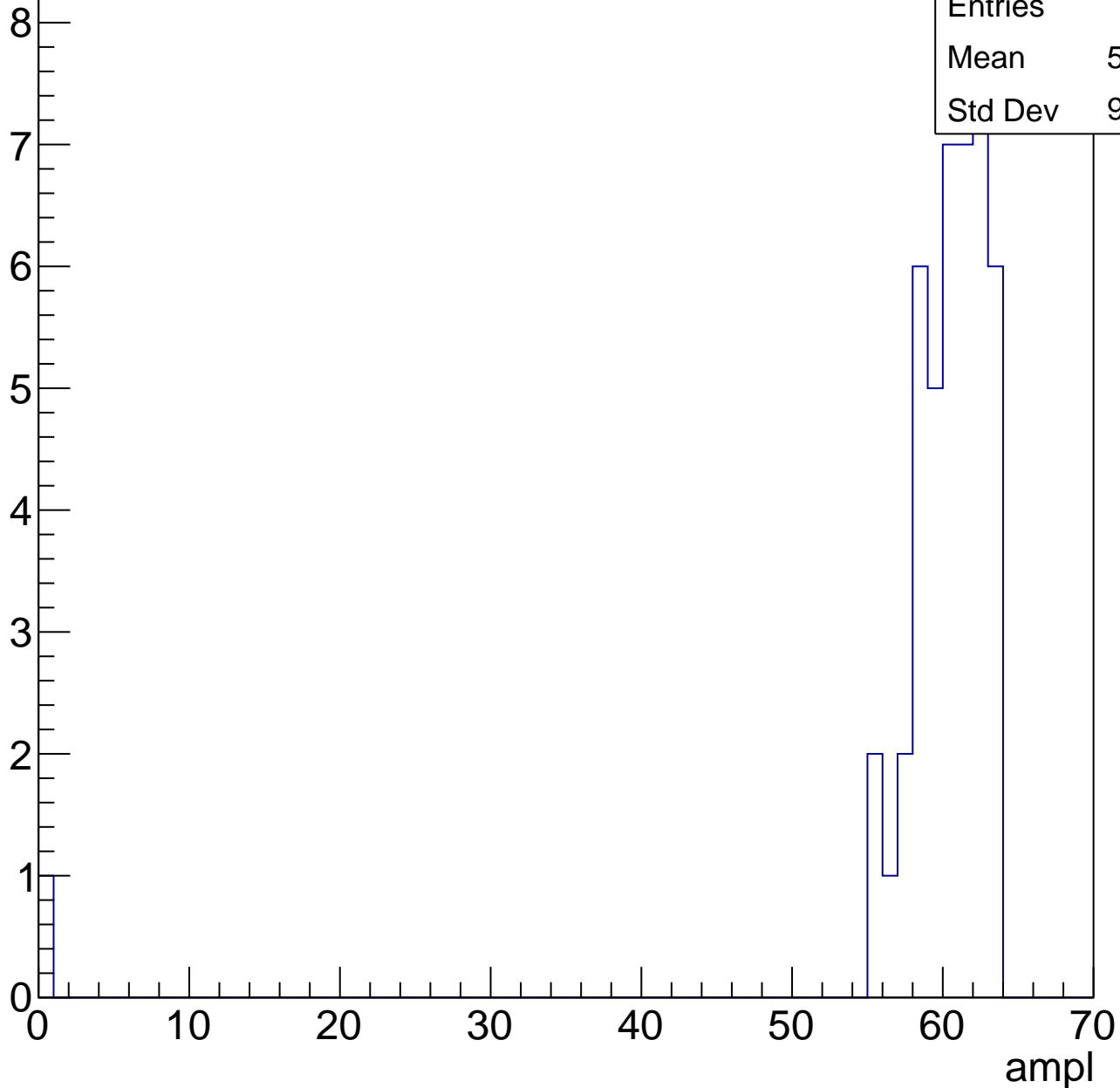


# B1L003S, U26-ch126, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	45
Mean	58.76
Std Dev	9.112



# B1L003S, U26-ch126, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

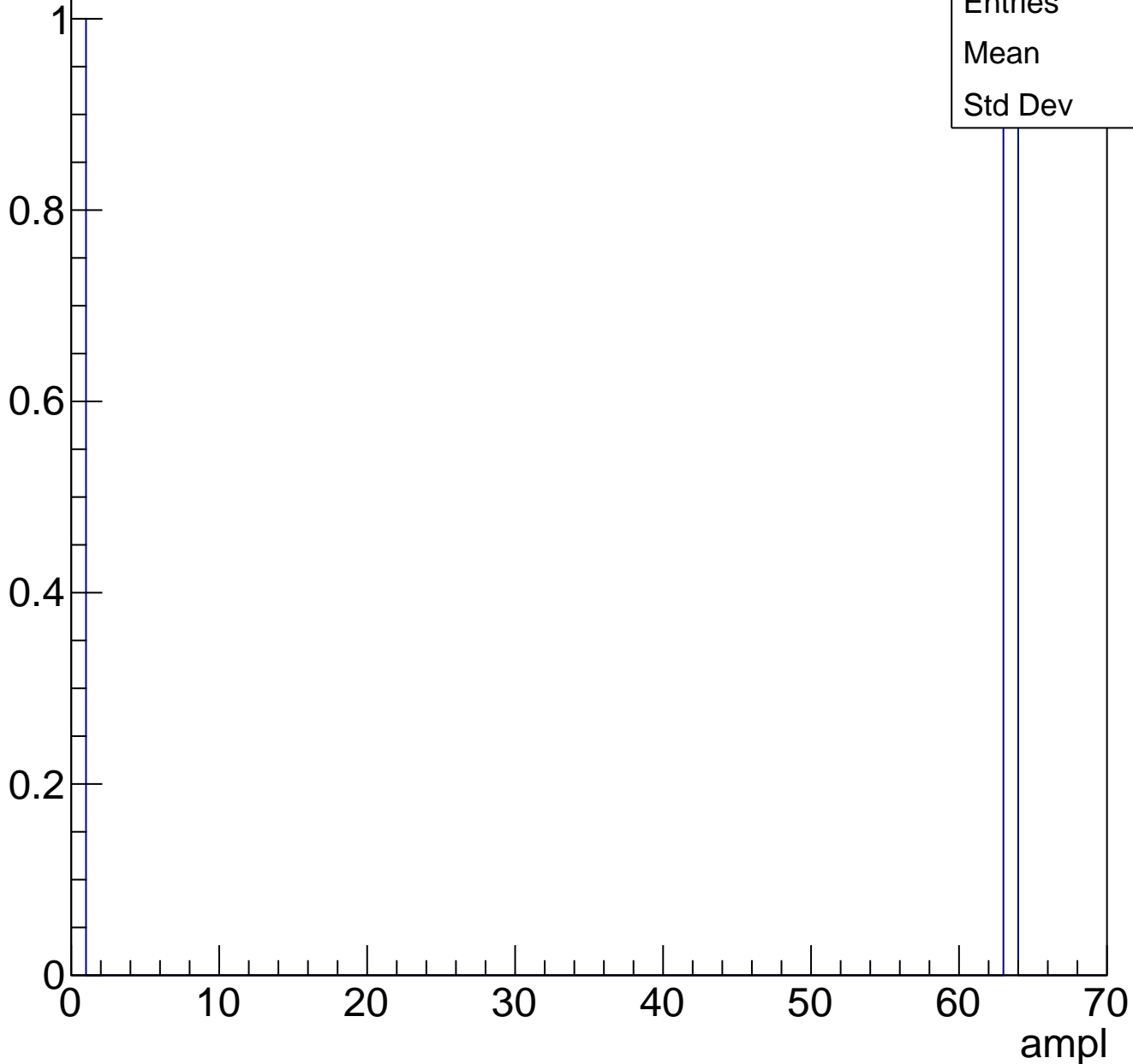




# B1L003S, U26-ch126, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U26-ch127, adc0

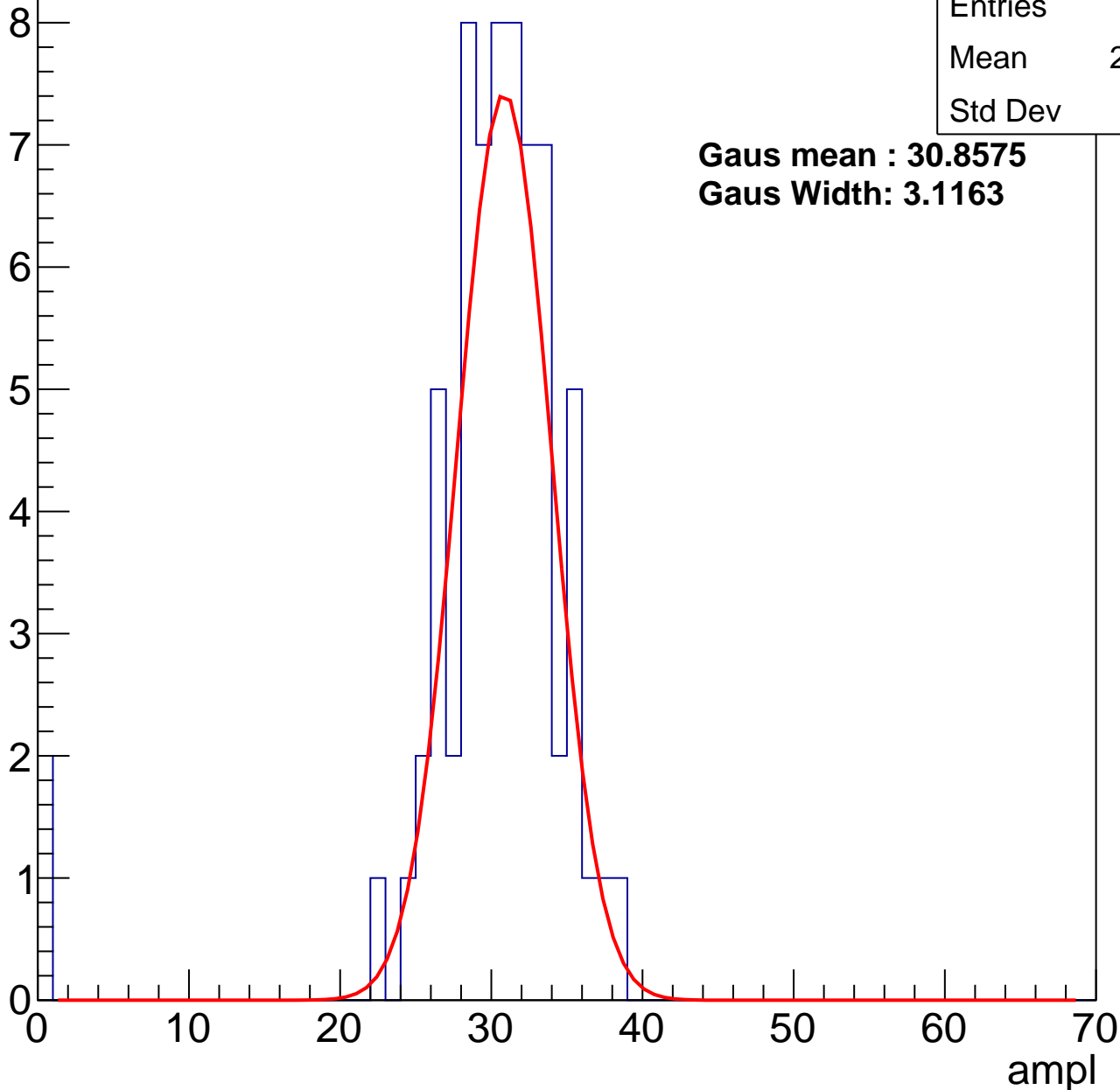
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	29.47
Std Dev	6.03

**Gaus mean : 30.8575**

**Gaus Width: 3.1163**



# B1L003S, U26-ch127, adc1

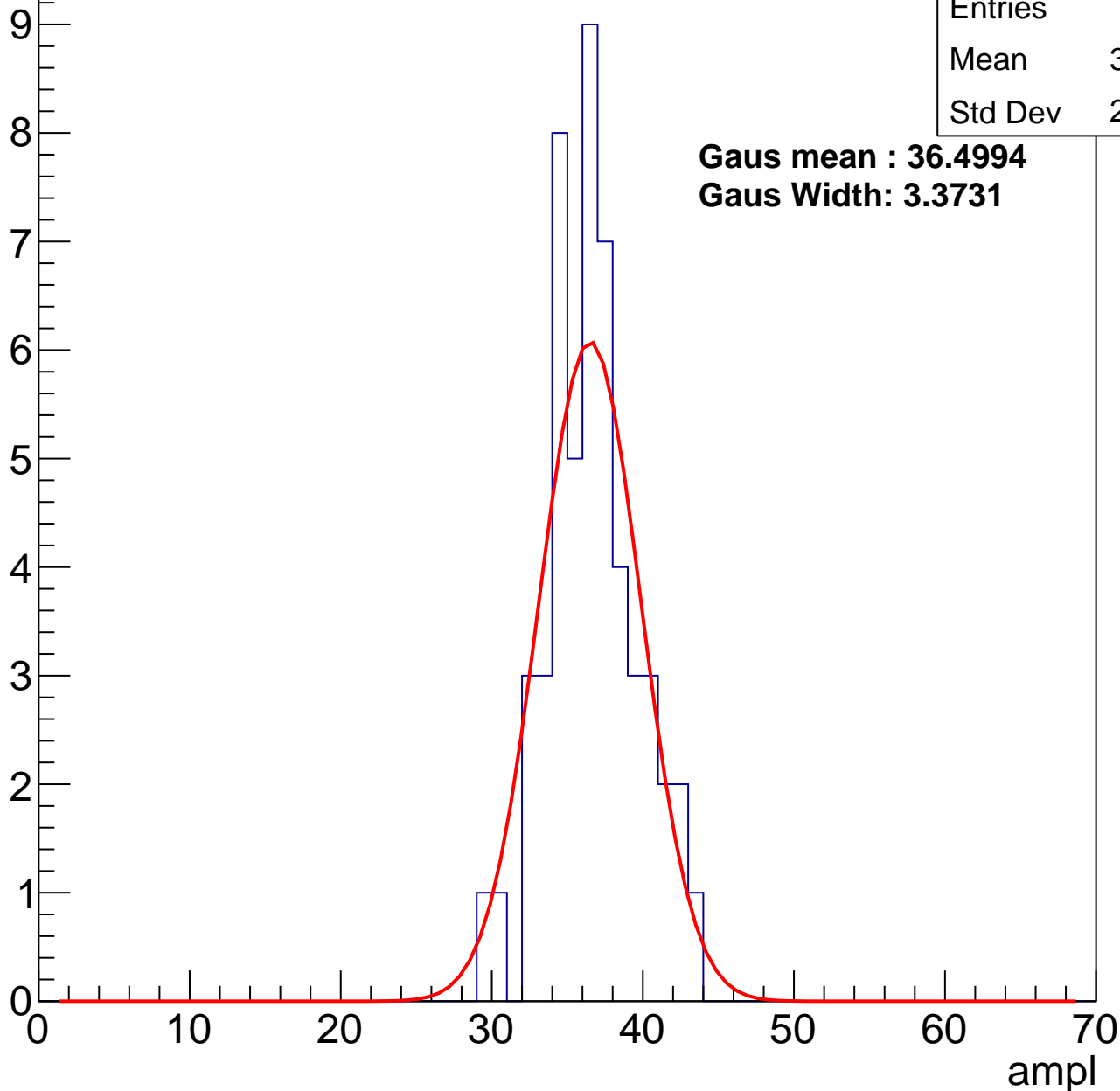
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	52
Mean	36.19
Std Dev	2.987

**Gaus mean : 36.4994**

**Gaus Width: 3.3731**



# B1L003S, U26-ch127, adc2

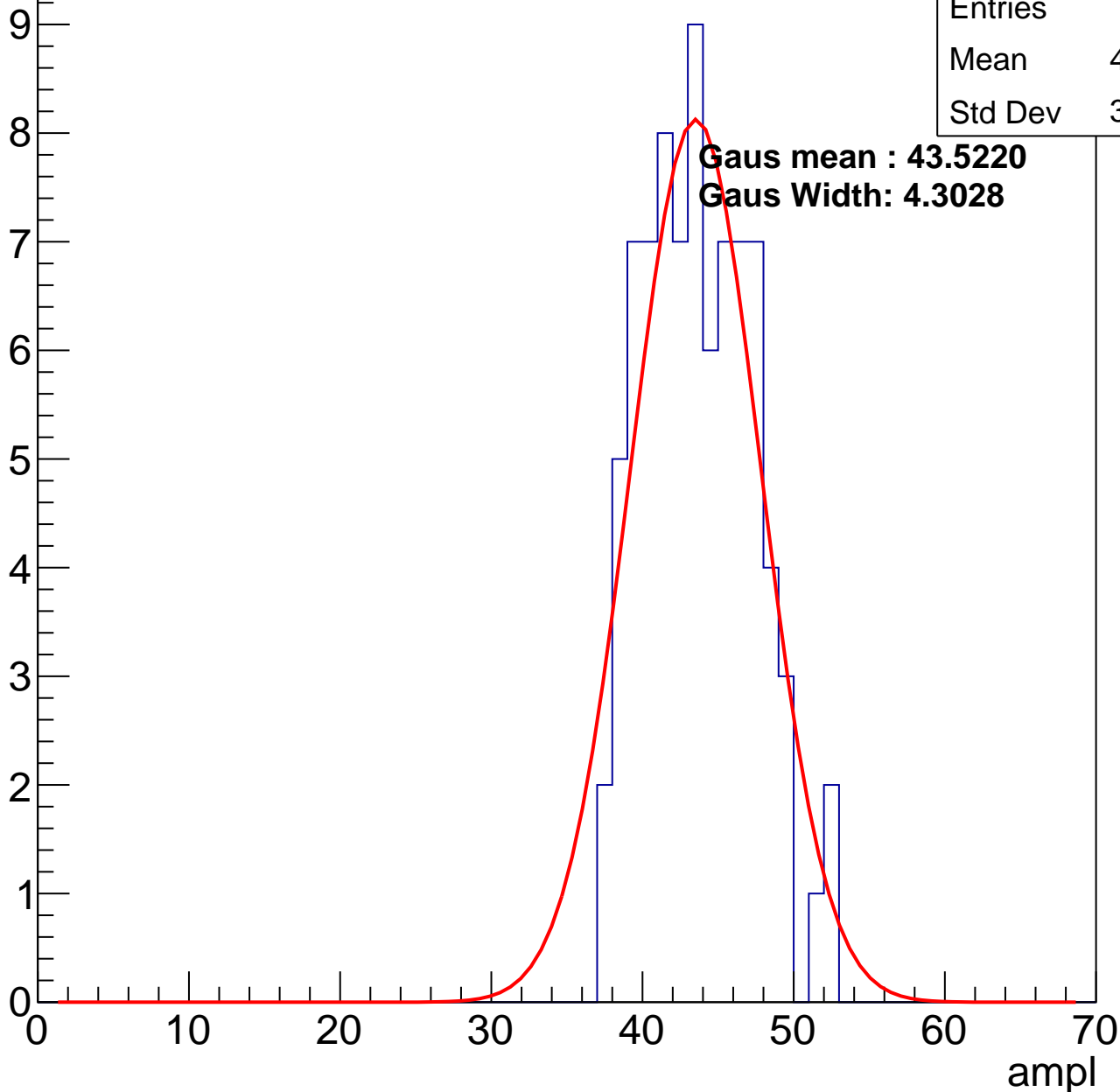
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	82
Mean	43.29
Std Dev	3.573

**Gaus mean : 43.5220**

**Gaus Width: 4.3028**

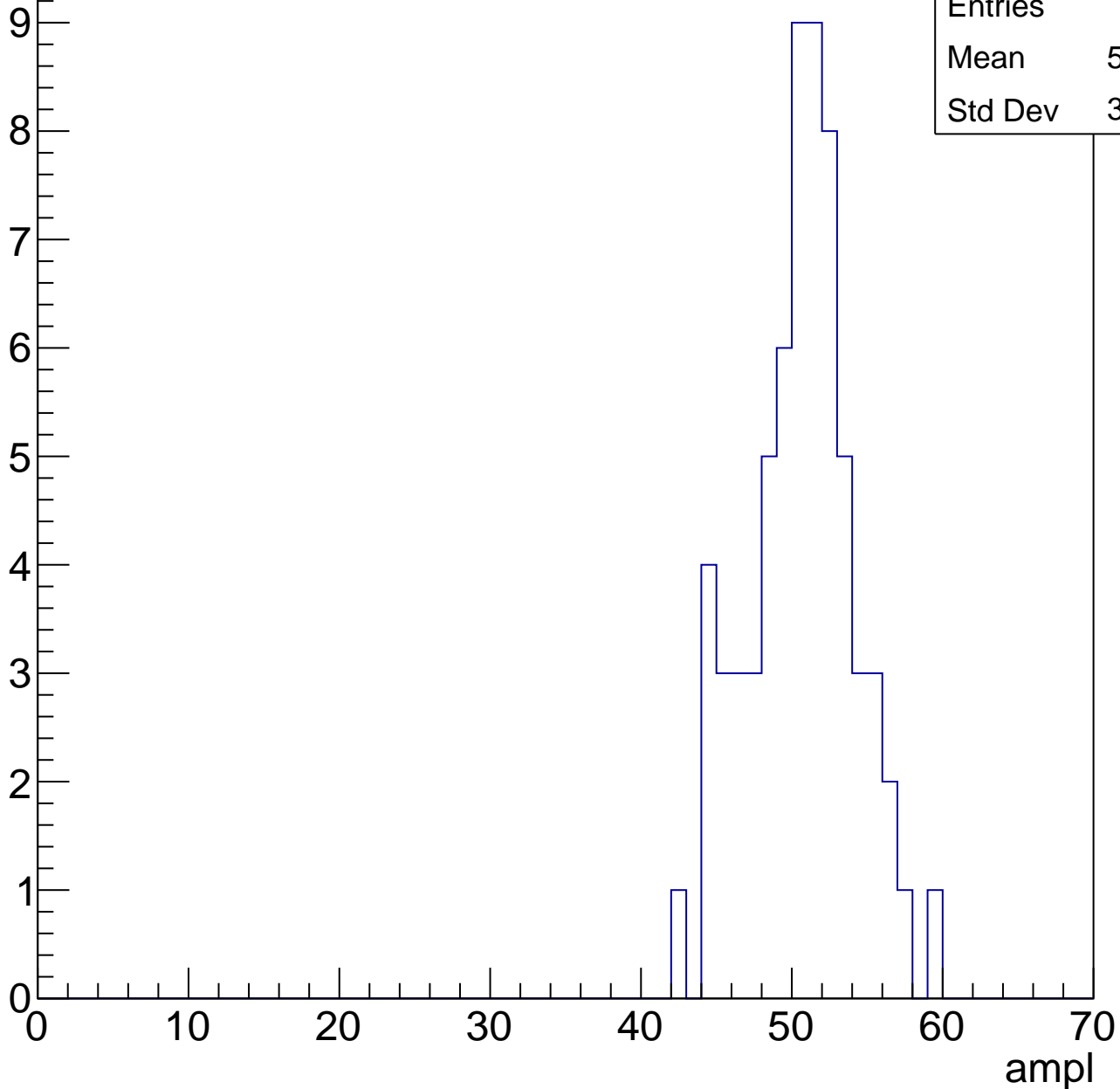


# B1L003S, U26-ch127, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	50.17
Std Dev	3.467

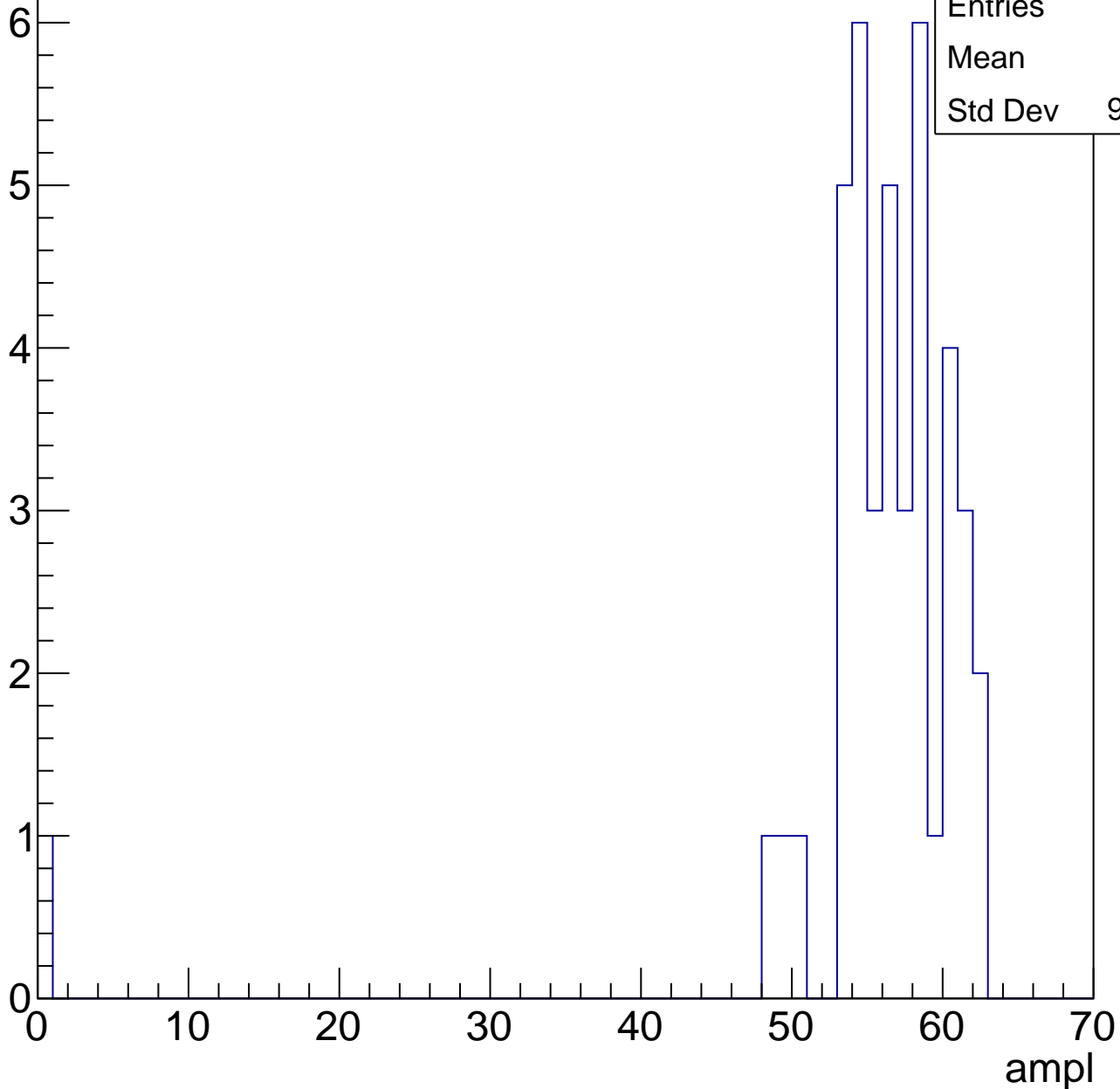


# B1L003S, U26-ch127, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

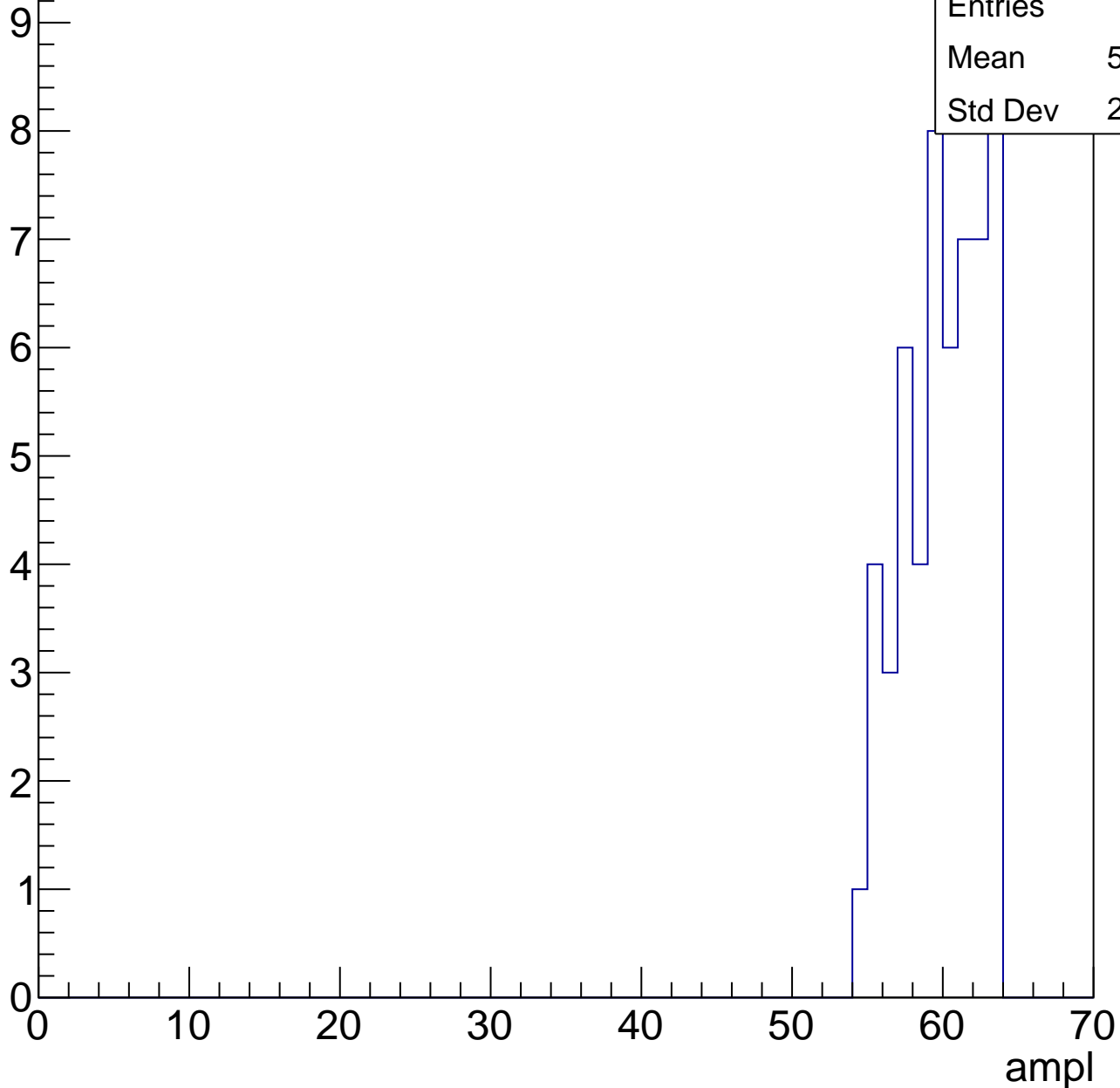
Entries	42
Mean	54.9
Std Dev	9.198



# B1L003S, U26-ch127, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U26-ch127, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U26-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

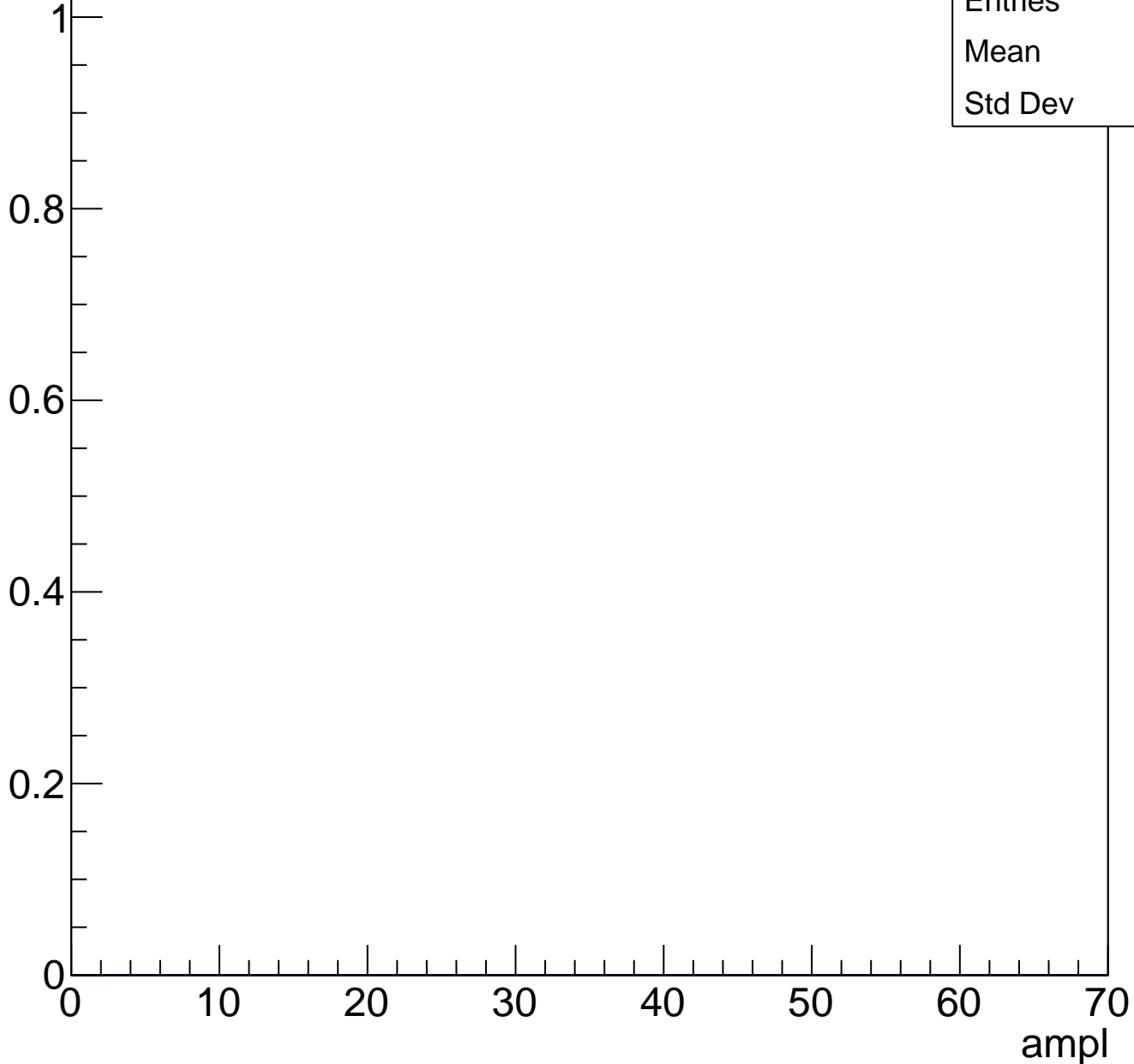


Entries	0
Mean	0
Std Dev	0

# B1L003S, U26-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0