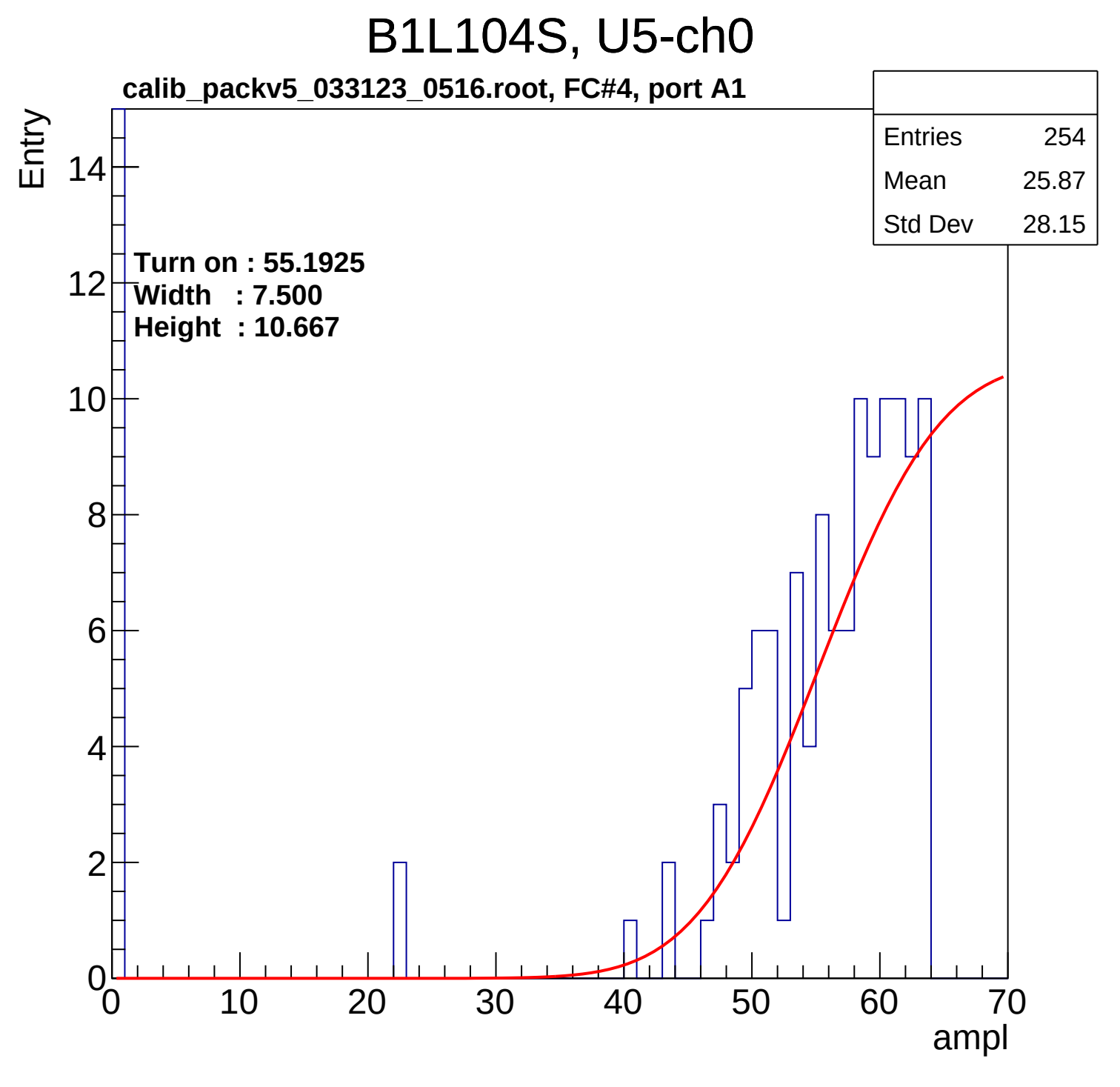
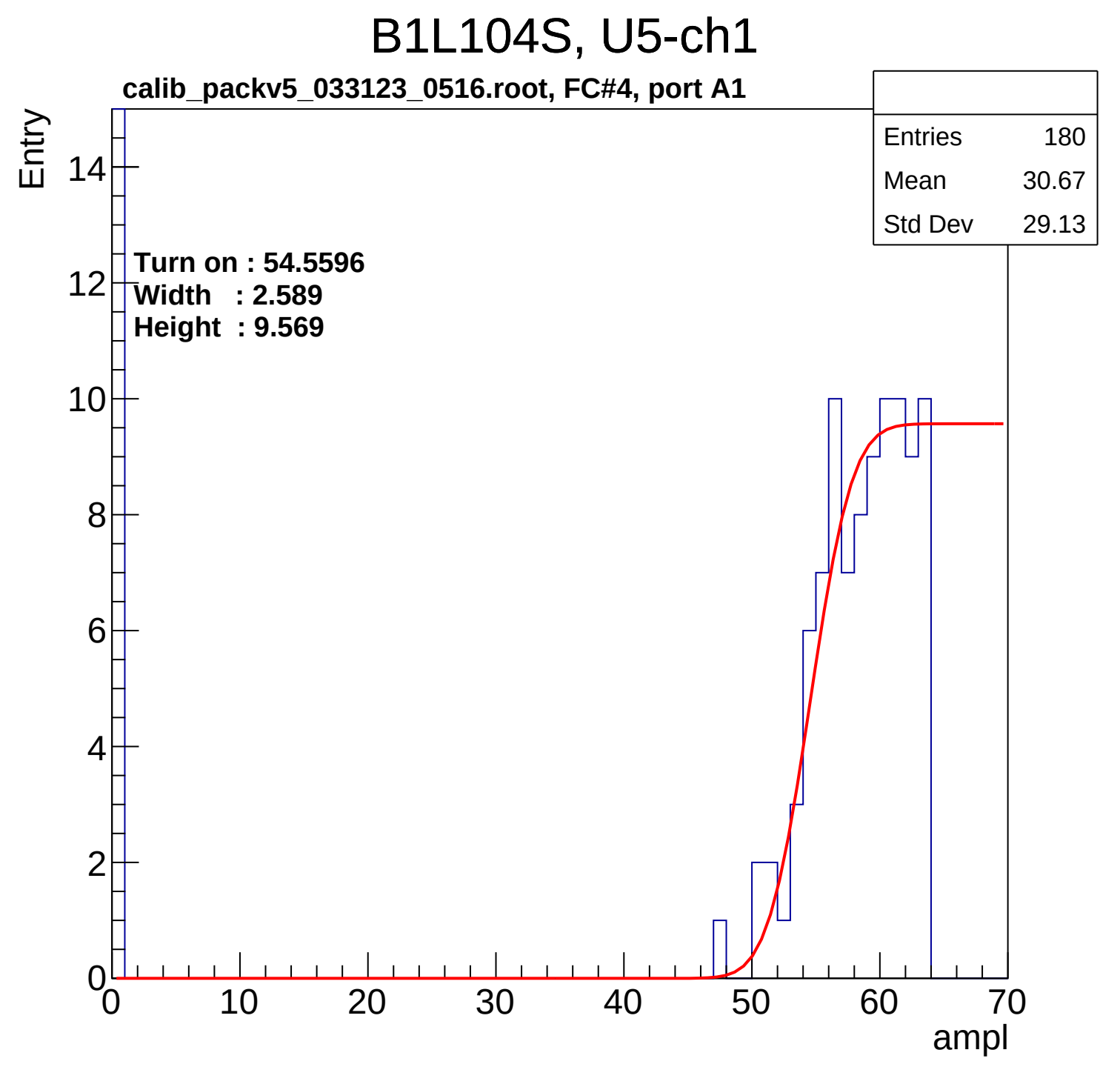
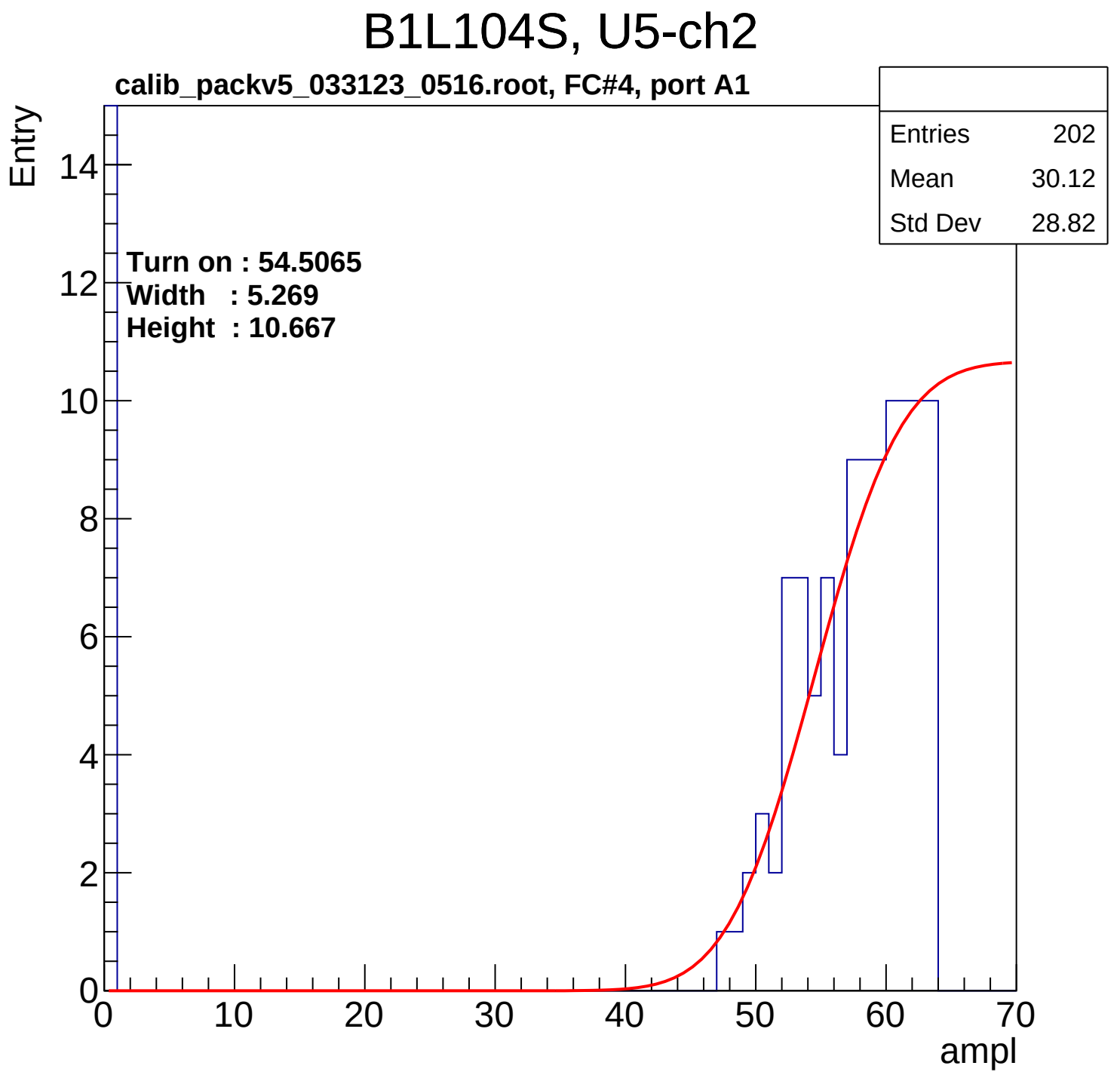
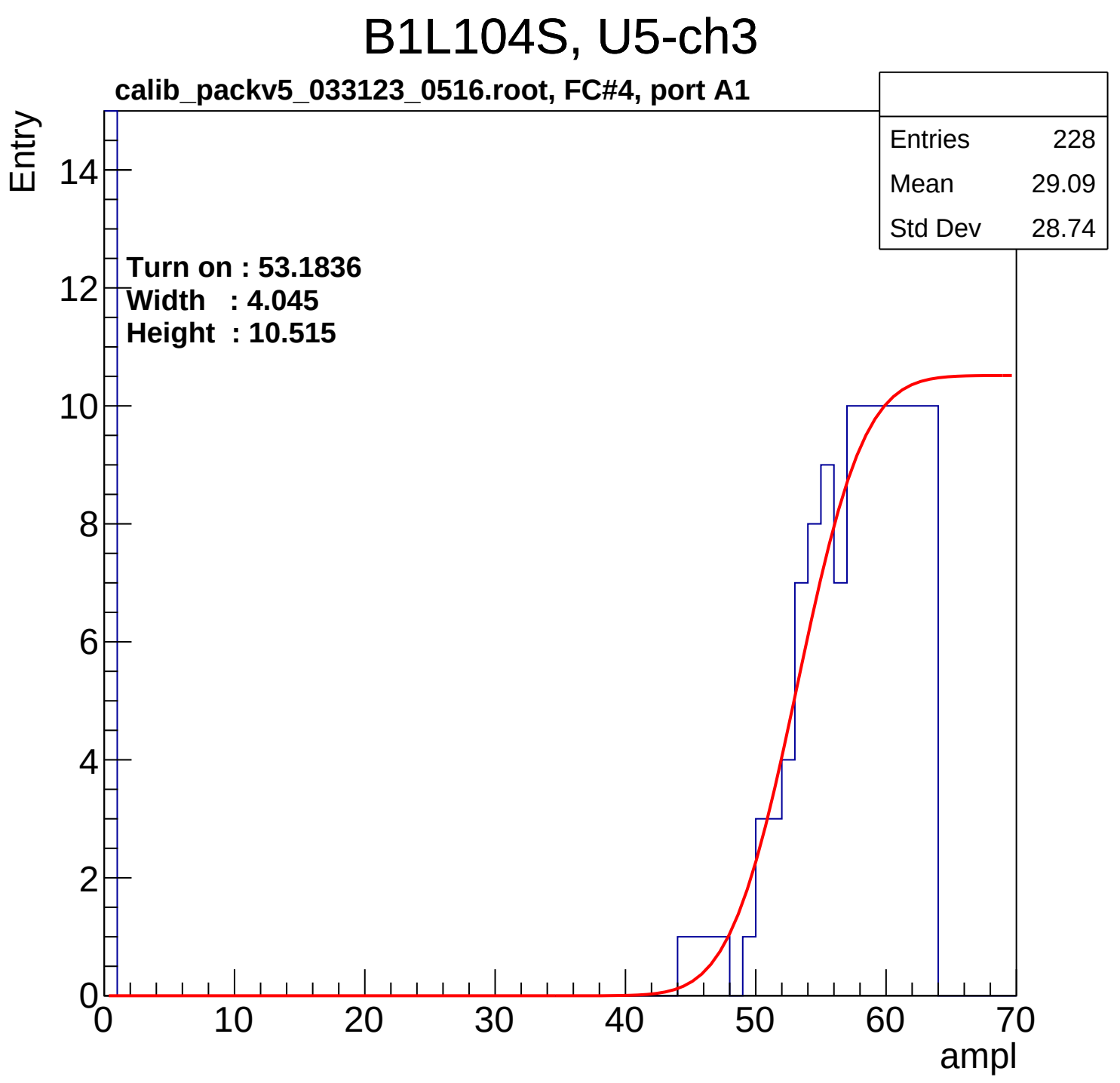
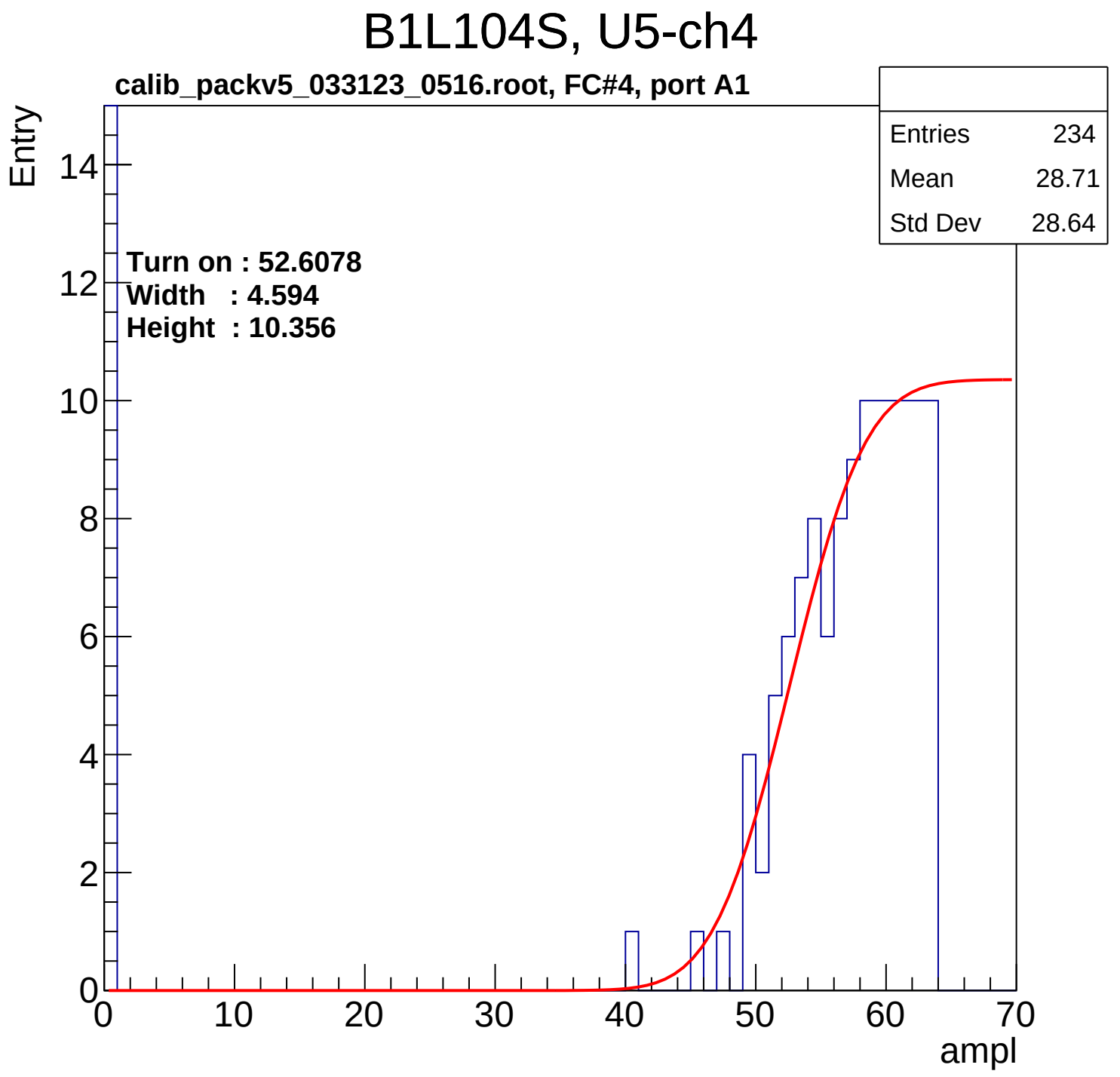
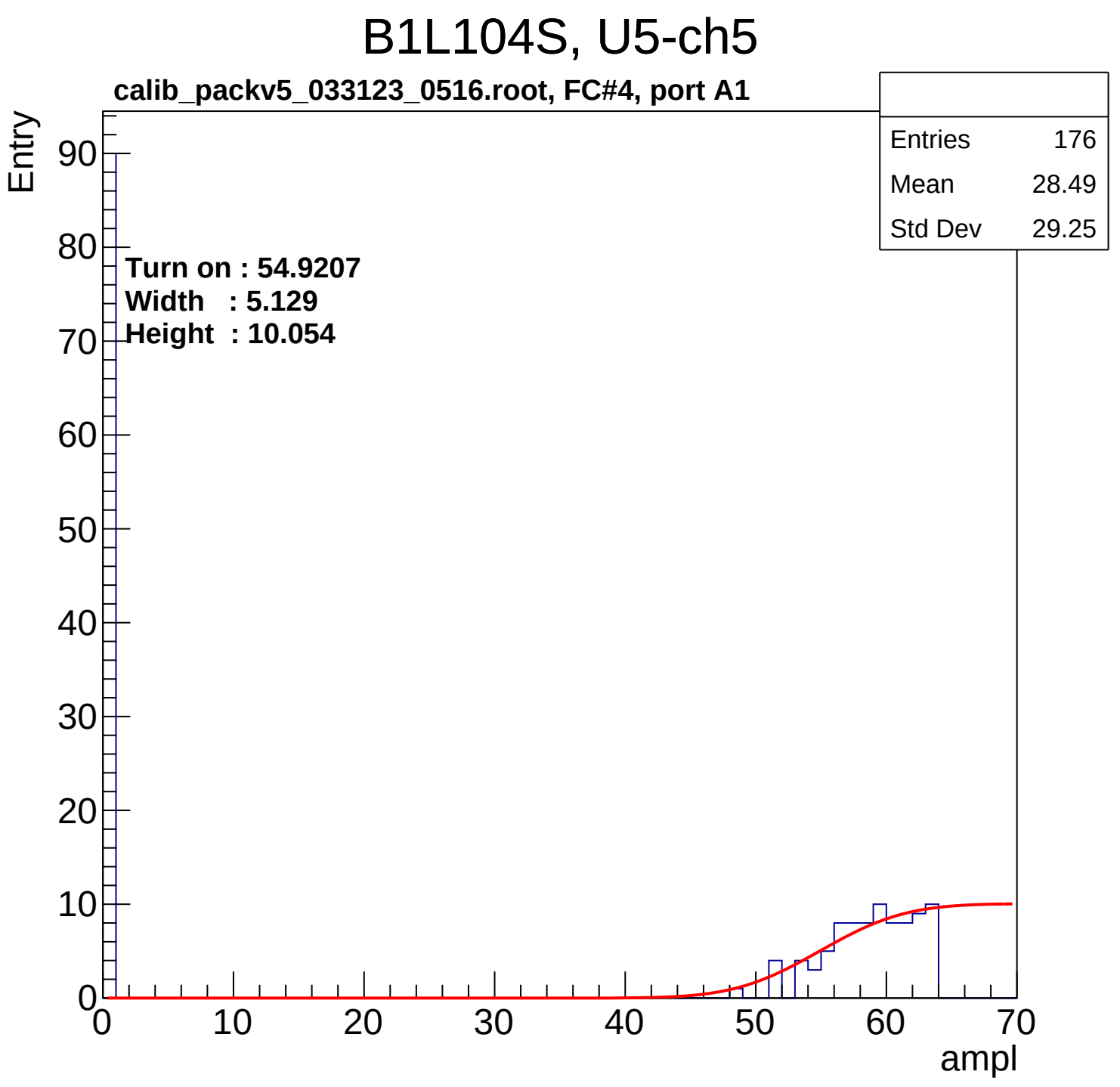

B1L104S, U5-ch0
calib_packv5_033123_0516.root, FC#4, port A1
Entries 254
Mean 25.87
Std Dev 28.15
Turn on : 55.1925
Width : 7.500
Height : 10.667
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

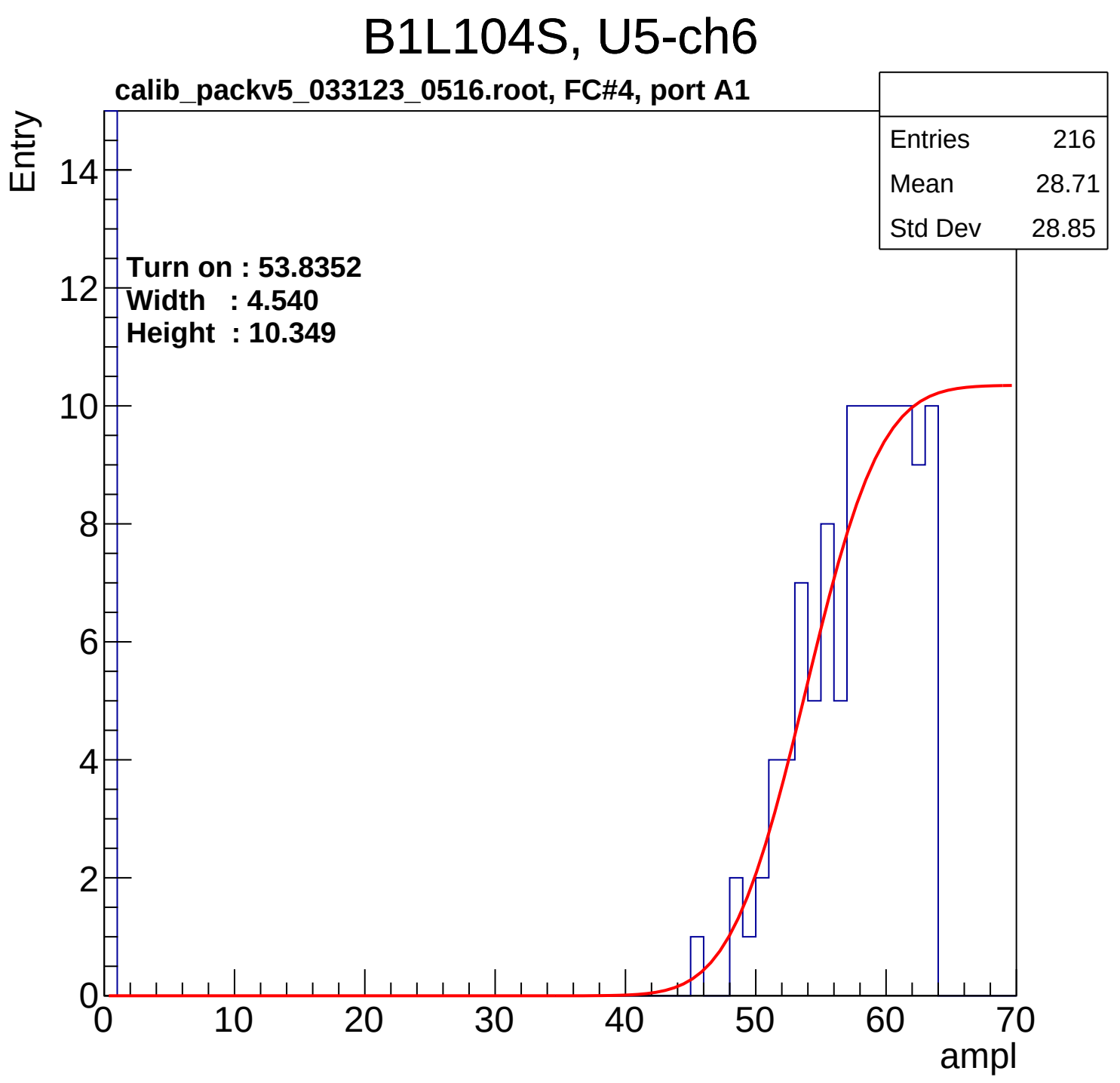

B1L104S, U5-ch1
calib_packv5_033123_0516.root, FC#4, port A1
Entries 180
Mean 30.67
Std Dev 29.13
Turn on : 54.5596
Width : 2.589
Height : 9.569
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

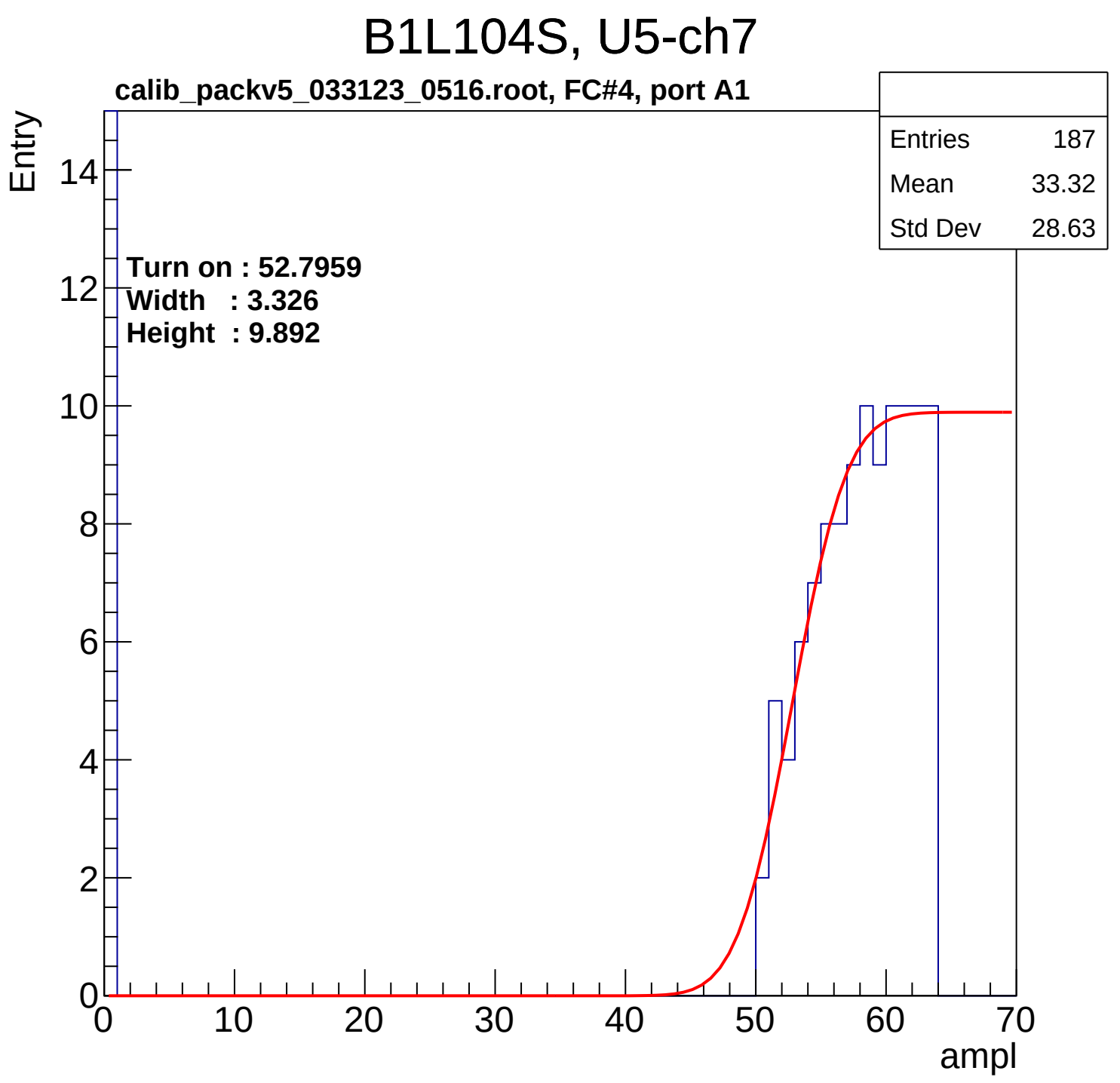

B1L104S, U5-ch2
calib_packv5_033123_0516.root, FC#4, port A1
Entries 202
Mean 30.12
Std Dev 28.82
Turn on : 54.5065
Width : 5.269
Height : 10.667
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

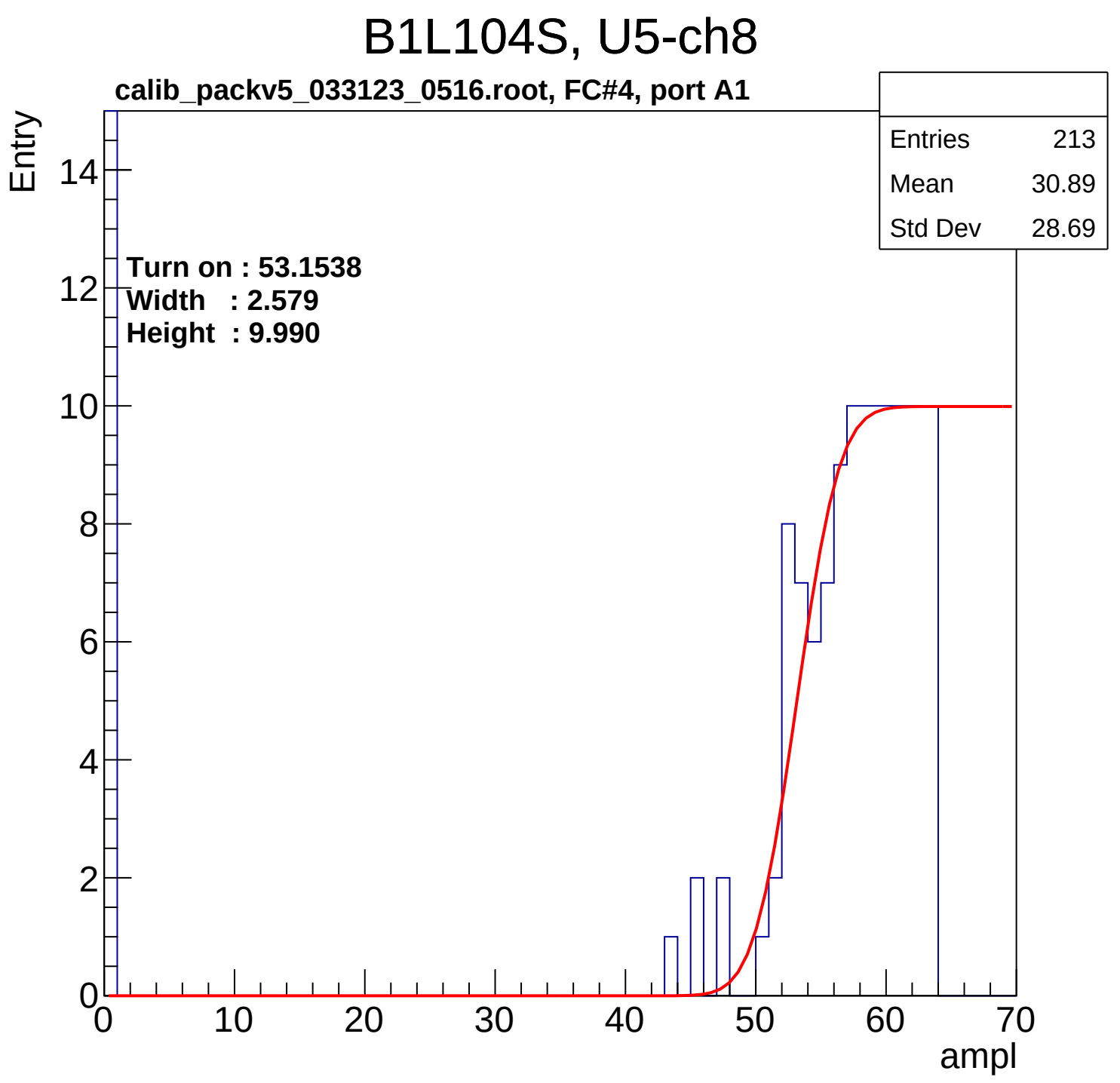

B1L104S, U5-ch3
calib_packv5_033123_0516.root, FC#4, port A1
Entries 228
Mean 29.09
Std Dev 28.74
Turn on : 53.1836
Width : 4.045
Height : 10.515
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

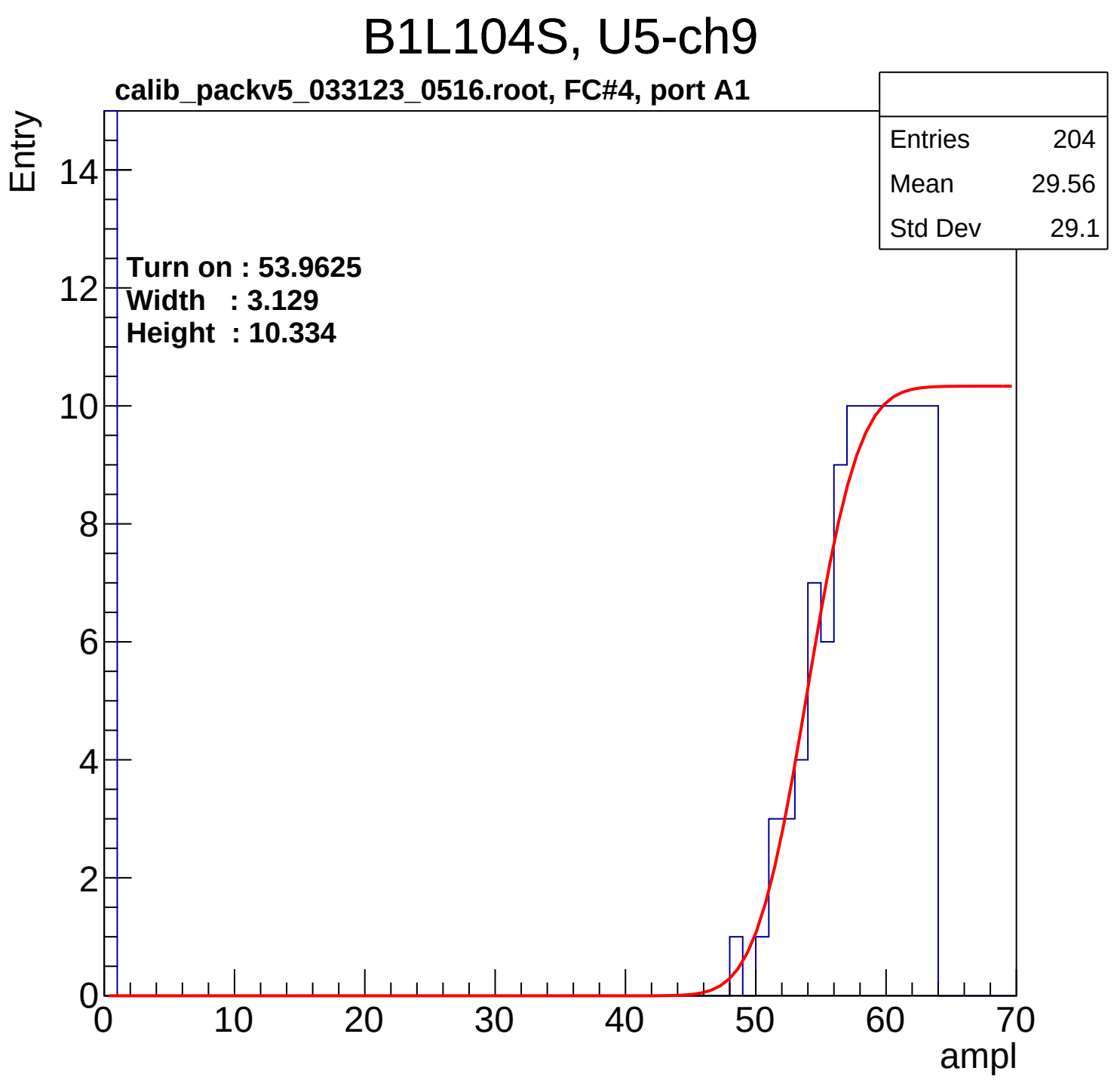

B1L104S, U5-ch4
calib_packv5_033123_0516.root, FC#4, port A1
Entries 234
Mean 28.71
Std Dev 28.64
Turn on : 52.6078
Width : 4.594
Height : 10.356
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

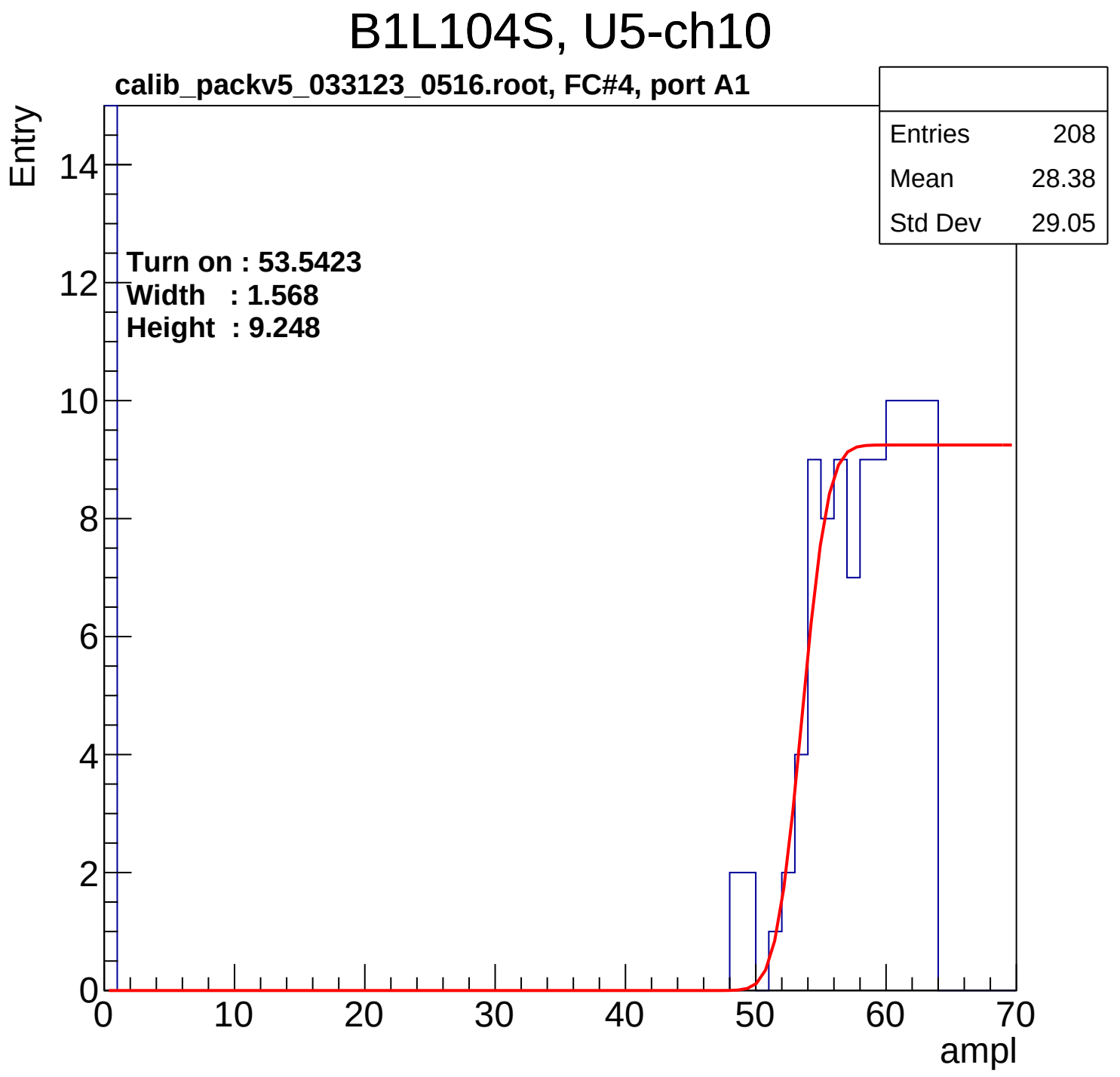

B1L104S, U5-ch5
calib_packv5_033123_0516.root, FC#4, port A1
Entries 176
Mean 28.49
Std Dev 29.25
Turn on : 54.9207
Width : 5.129
Height : 10.054
Entry
ampl
0
10
20
30
40
50
60
70
80
90

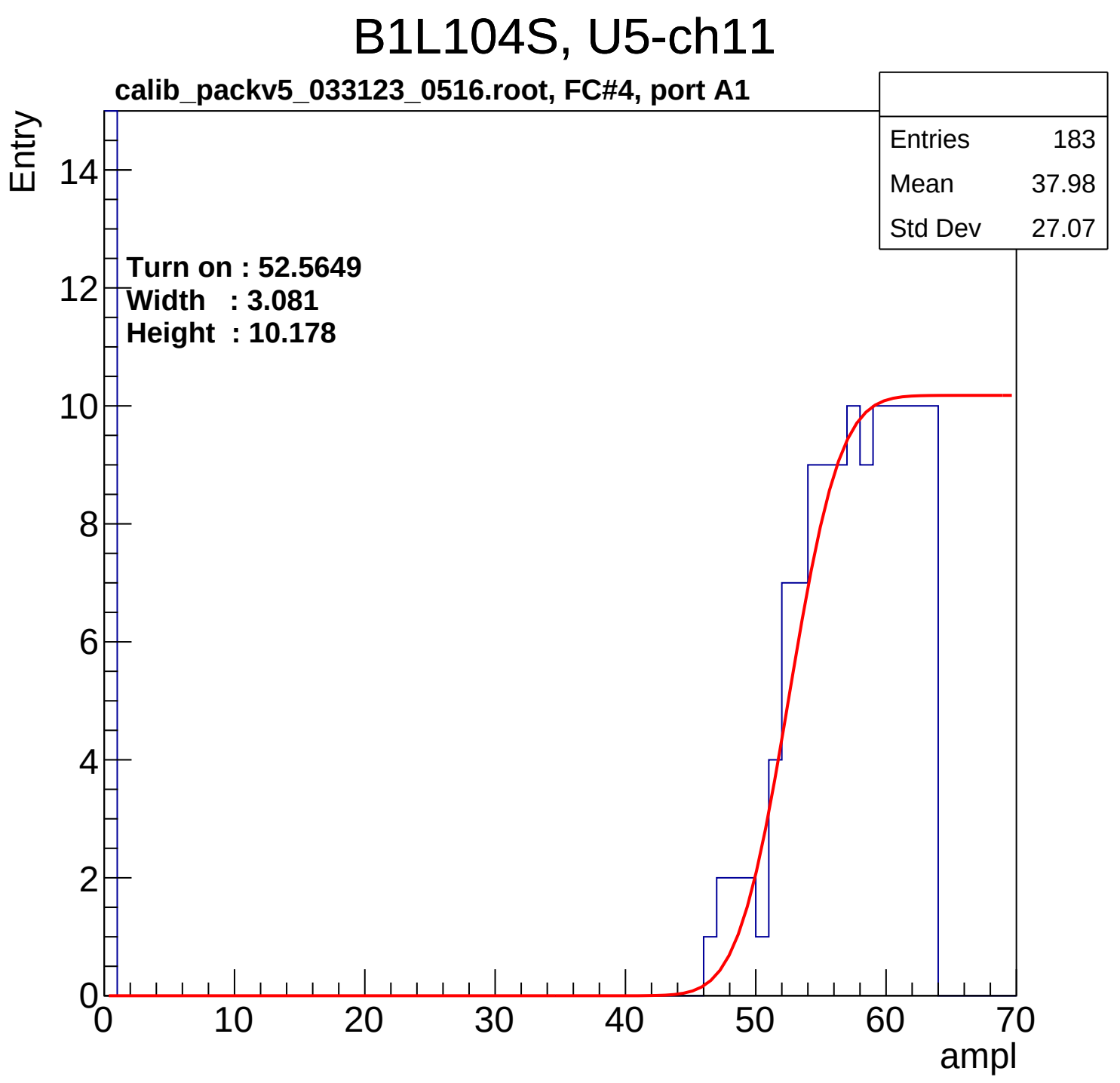

B1L104S, U5-ch6
calib_packv5_033123_0516.root, FC#4, port A1
Entries 216
Mean 28.71
Std Dev 28.85
Turn on : 53.8352
Width : 4.540
Height : 10.349
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

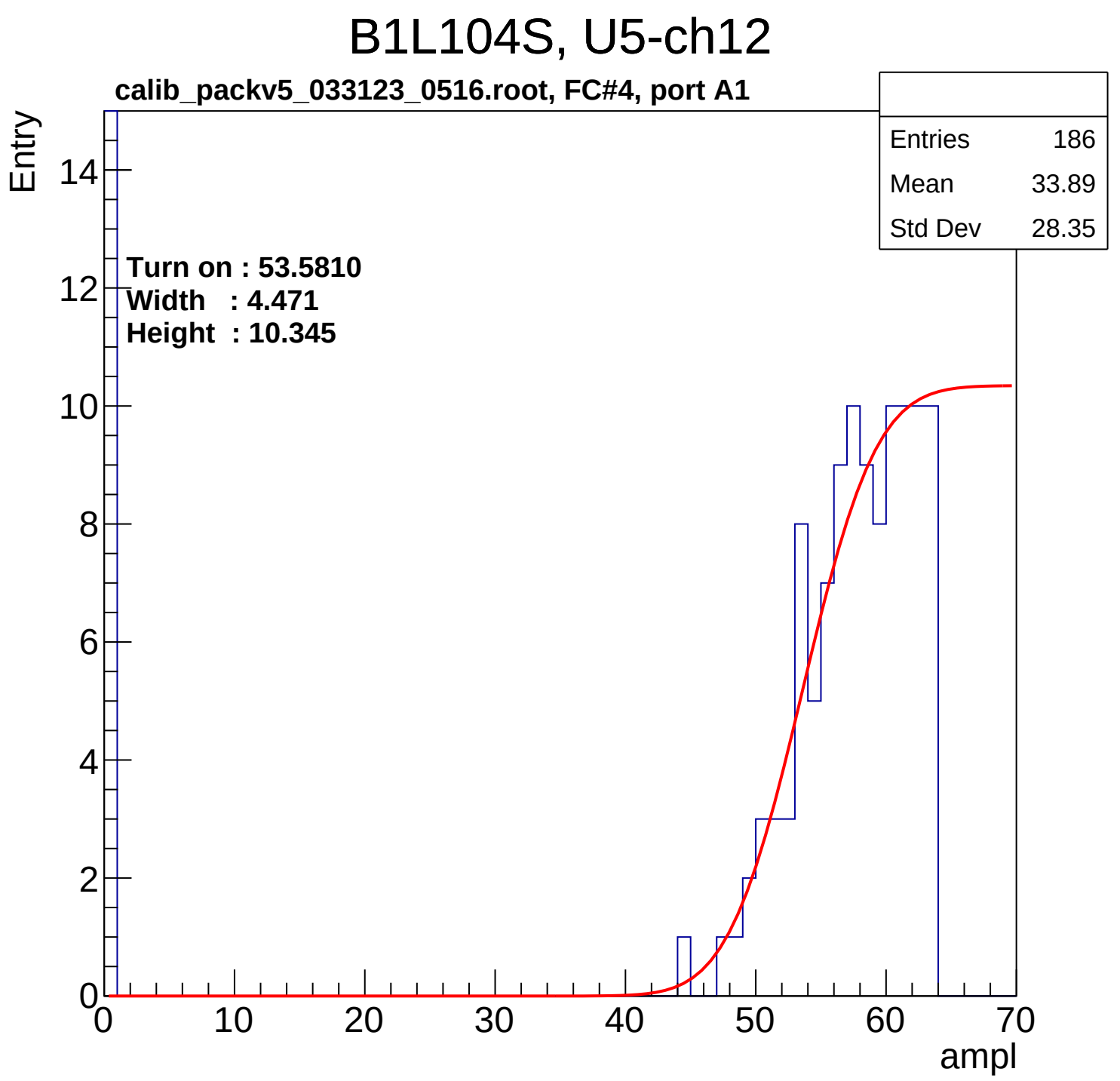

B1L104S, U5-ch7
calib_packv5_033123_0516.root, FC#4, port A1
Entries 187
Mean 33.32
Std Dev 28.63
Turn on : 52.7959
Width : 3.326
Height : 9.892
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

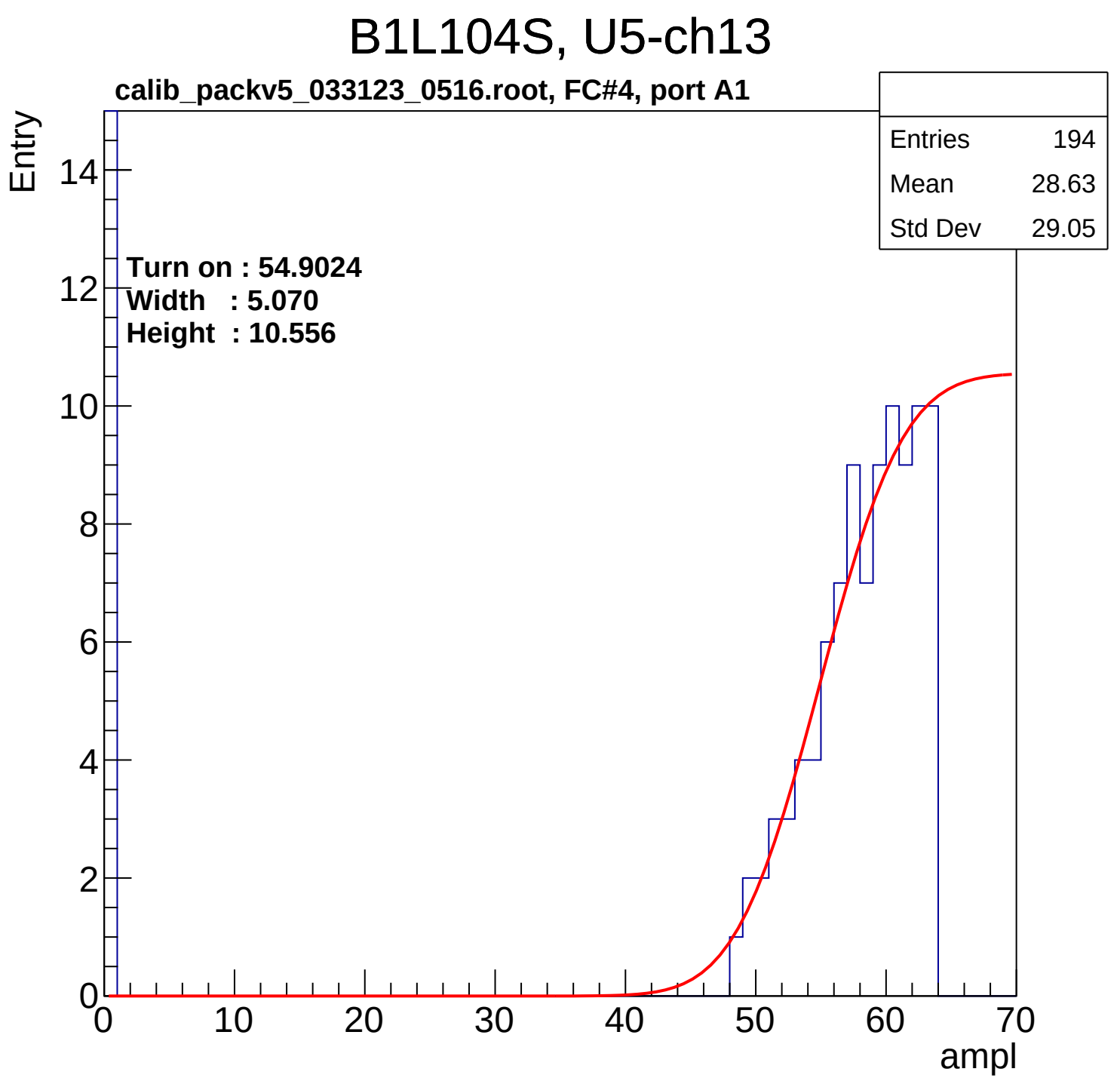

B1L104S, U5-ch8
calib_packv5_033123_0516.root, FC#4, port A1
Entries 213
Mean 30.89
Std Dev 28.69
Turn on : 53.1538
Width : 2.579
Height : 9.990
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

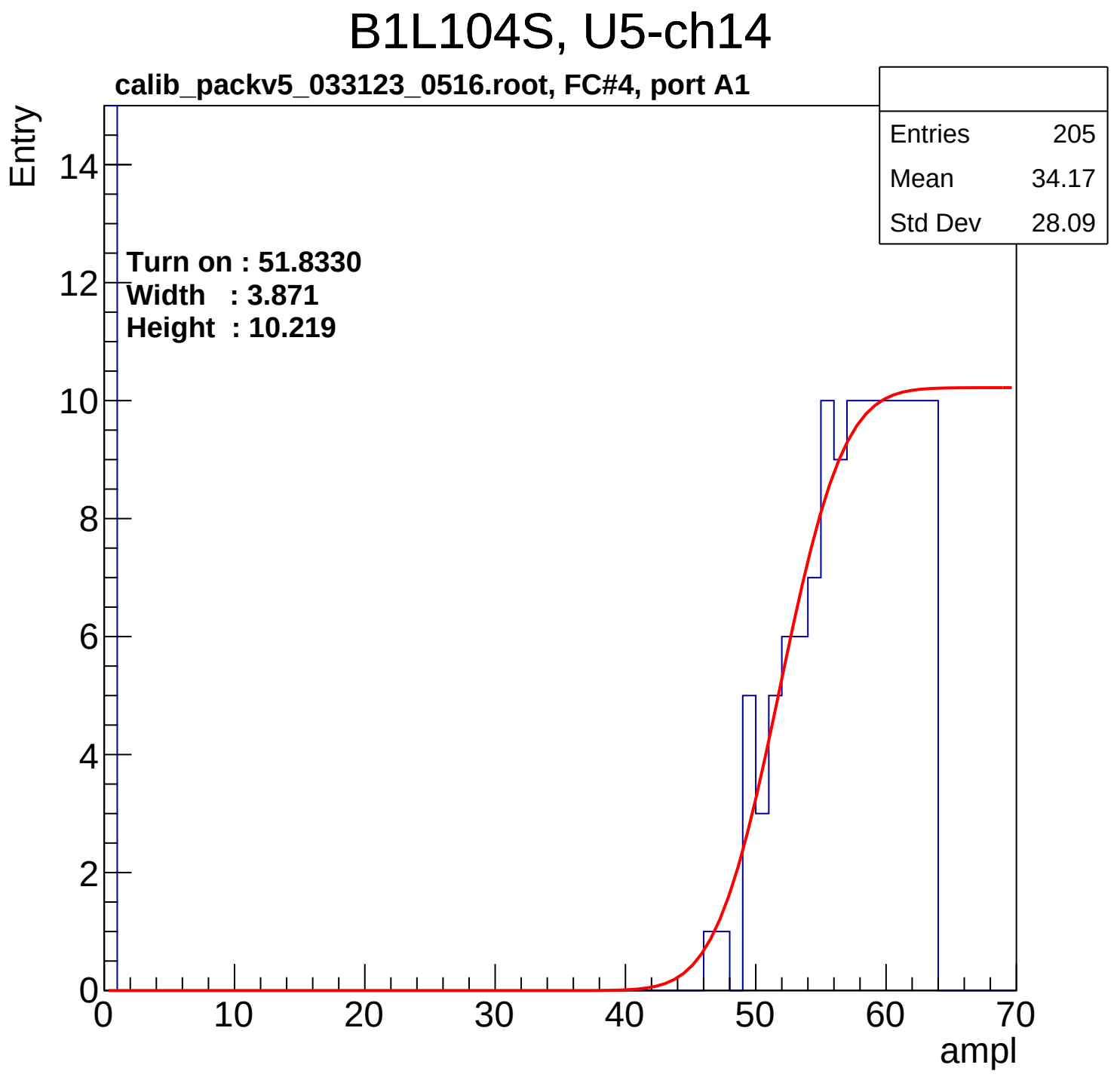

B1L104S, U5-ch9
calib_packv5_033123_0516.root, FC#4, port A1
Entries 204
Mean 29.56
Std Dev 29.1
Turn on : 53.9625
Width : 3.129
Height : 10.334
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

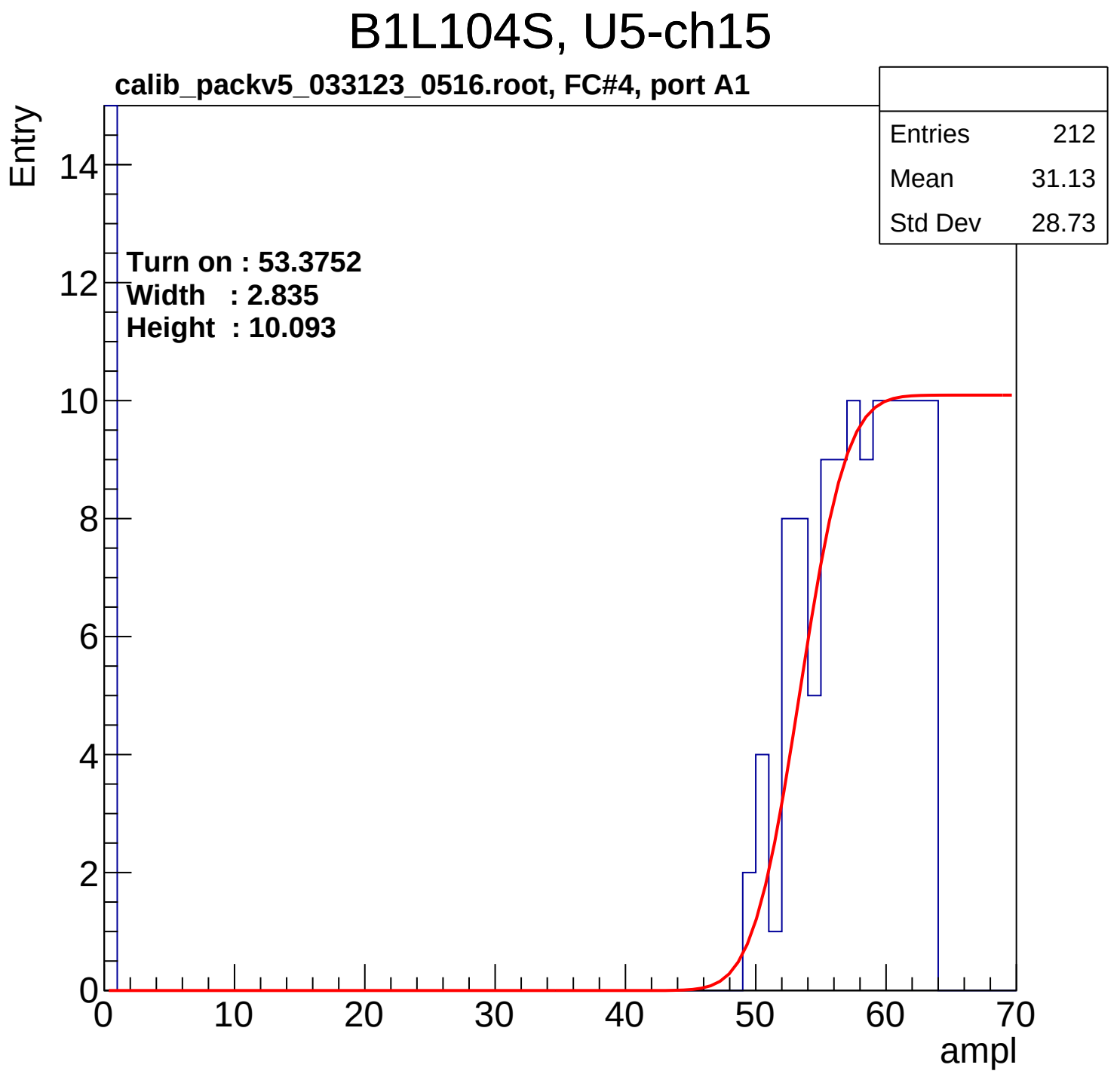

B1L104S, U5-ch10
calib_packv5_033123_0516.root, FC#4, port A1
Entries 208
Mean 28.38
Std Dev 29.05
Turn on : 53.5423
Width : 1.568
Height : 9.248
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

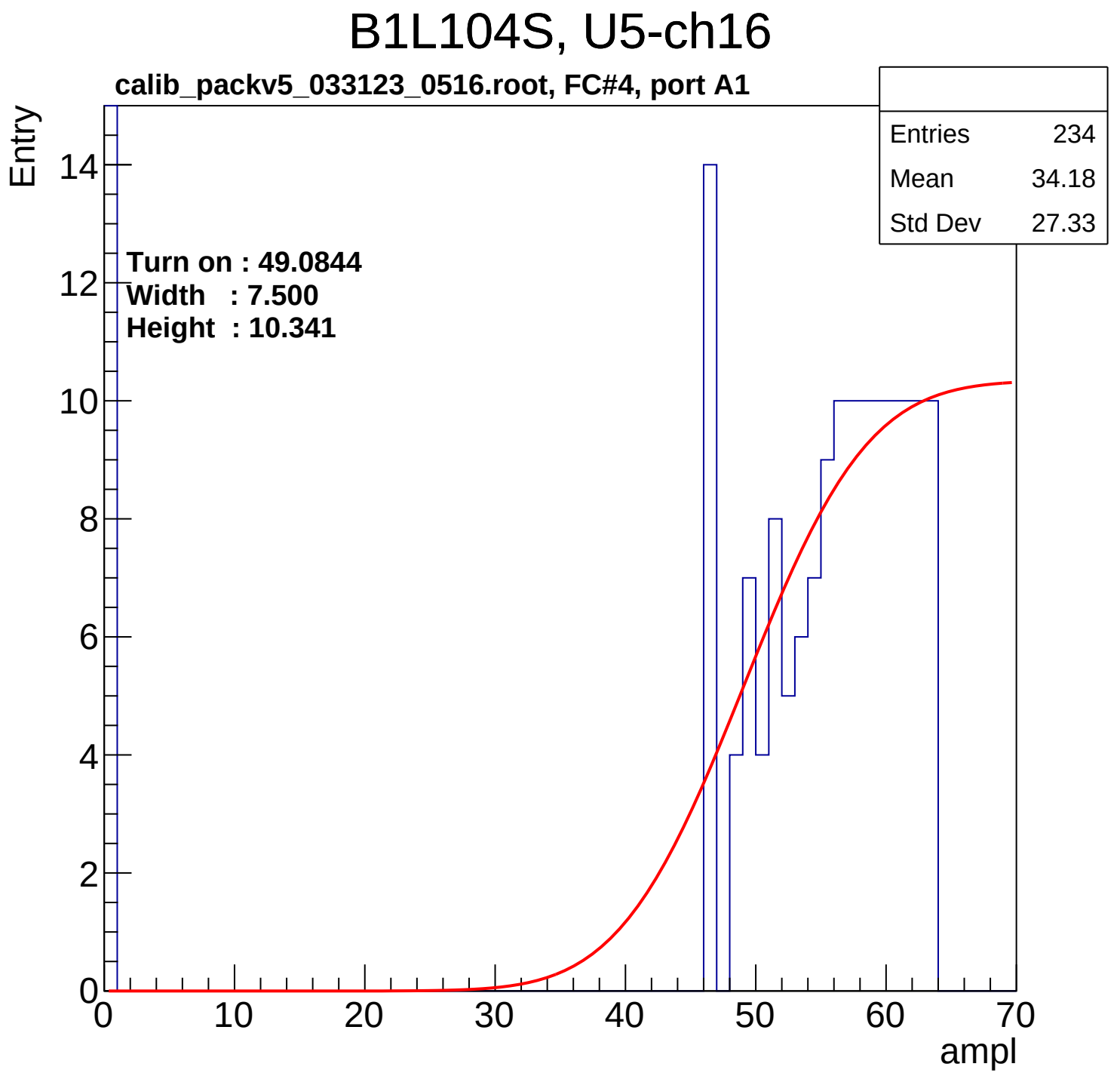

B1L104S, U5-ch11
calib_packv5_033123_0516.root, FC#4, port A1
Entries 183
Mean 37.98
Std Dev 27.07
Turn on : 52.5649
Width : 3.081
Height : 10.178
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

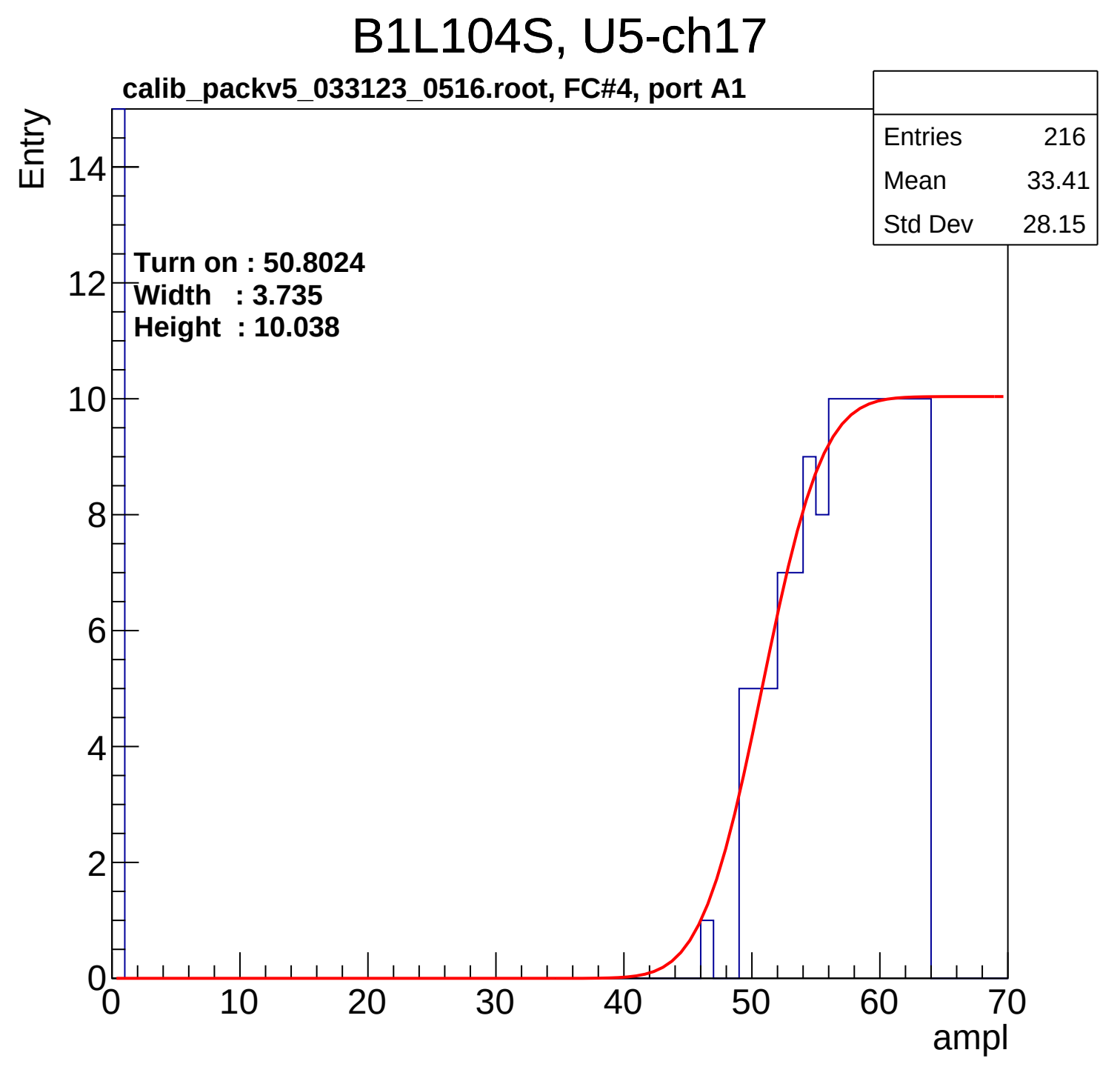

B1L104S, U5-ch12
calib_packv5_033123_0516.root, FC#4, port A1
Entries 186
Mean 33.89
Std Dev 28.35
Turn on : 53.5810
Width : 4.471
Height : 10.345
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

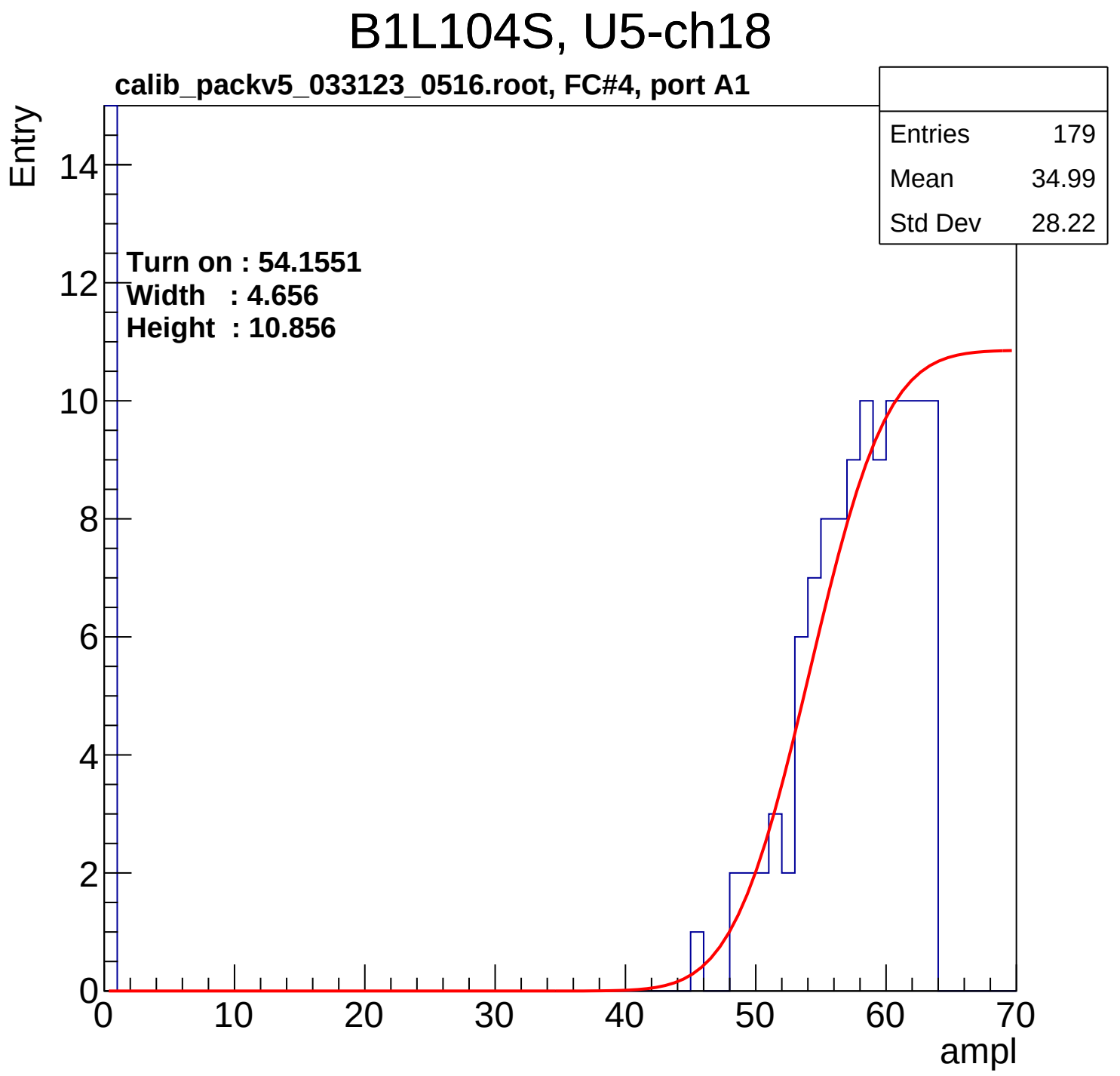

B1L104S, U5-ch13
calib_packv5_033123_0516.root, FC#4, port A1
Entries 194
Mean 28.63
Std Dev 29.05
Turn on : 54.9024
Width : 5.070
Height : 10.556
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

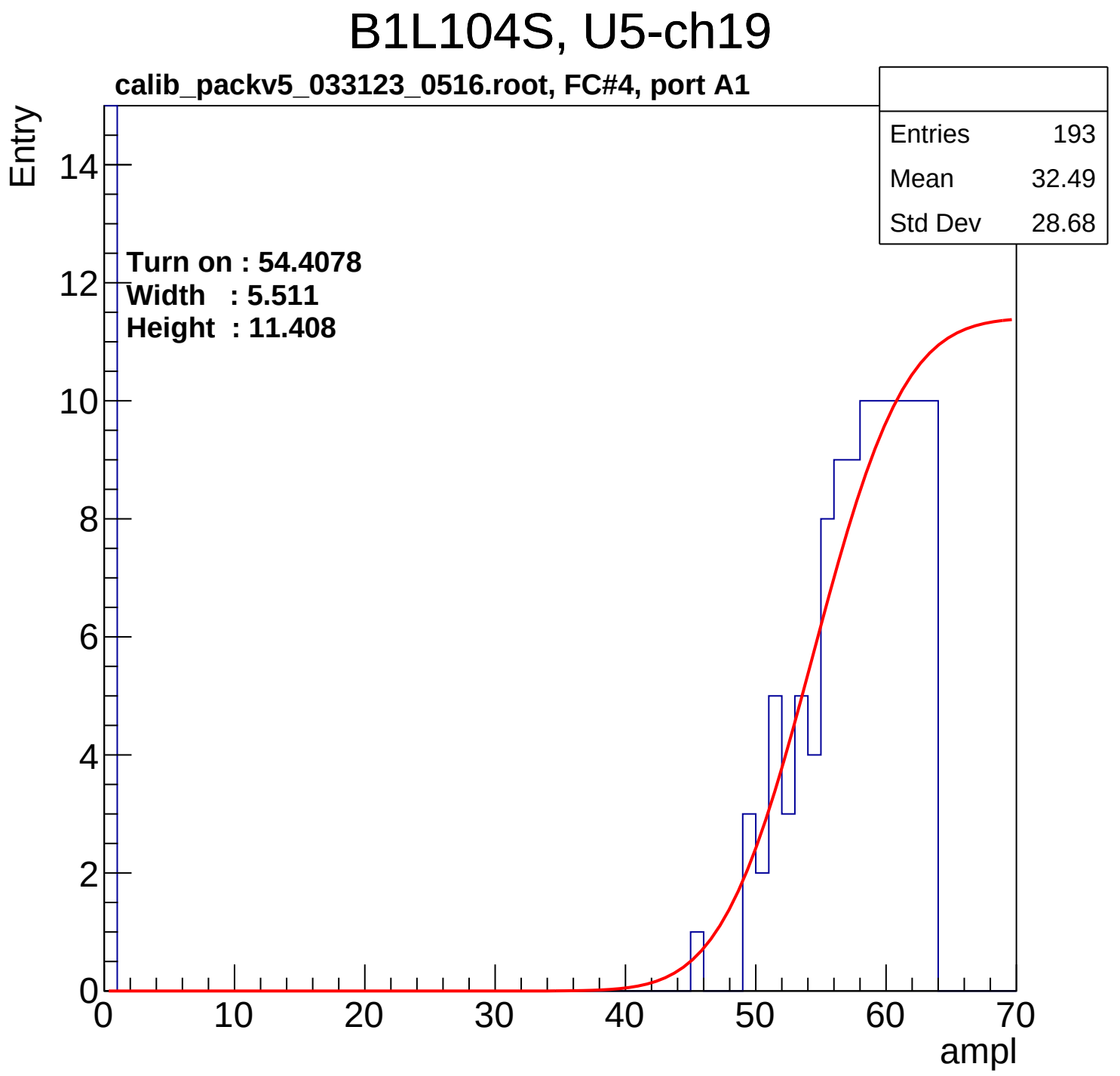

B1L104S, U5-ch14
calib_packv5_033123_0516.root, FC#4, port A1
Entries 205
Mean 34.17
Std Dev 28.09
Turn on : 51.8330
Width : 3.871
Height : 10.219
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

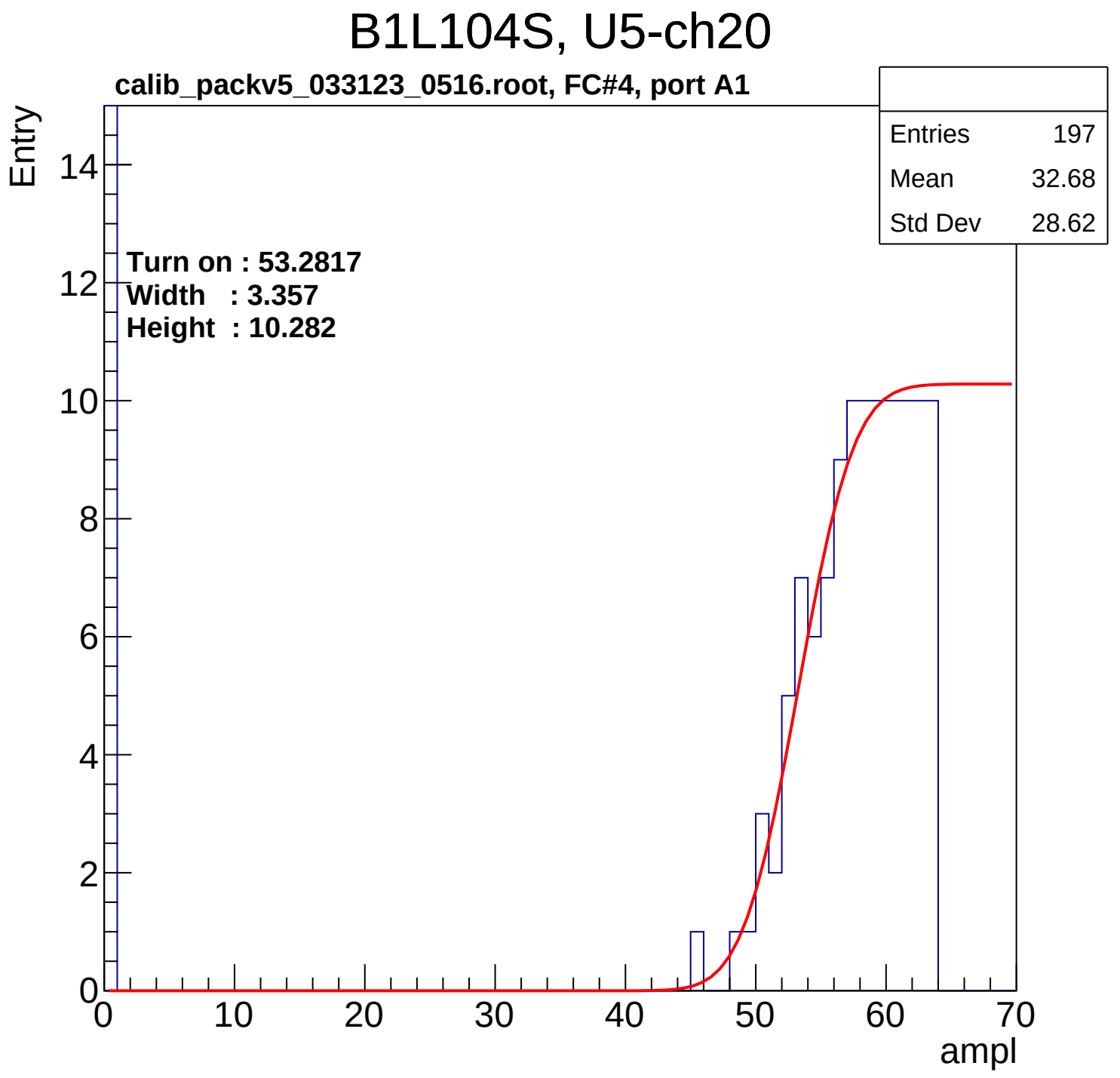

B1L104S, U5-ch15
calib_packv5_033123_0516.root, FC#4, port A1
Entries 212
Mean 31.13
Std Dev 28.73
Turn on : 53.3752
Width : 2.835
Height : 10.093
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

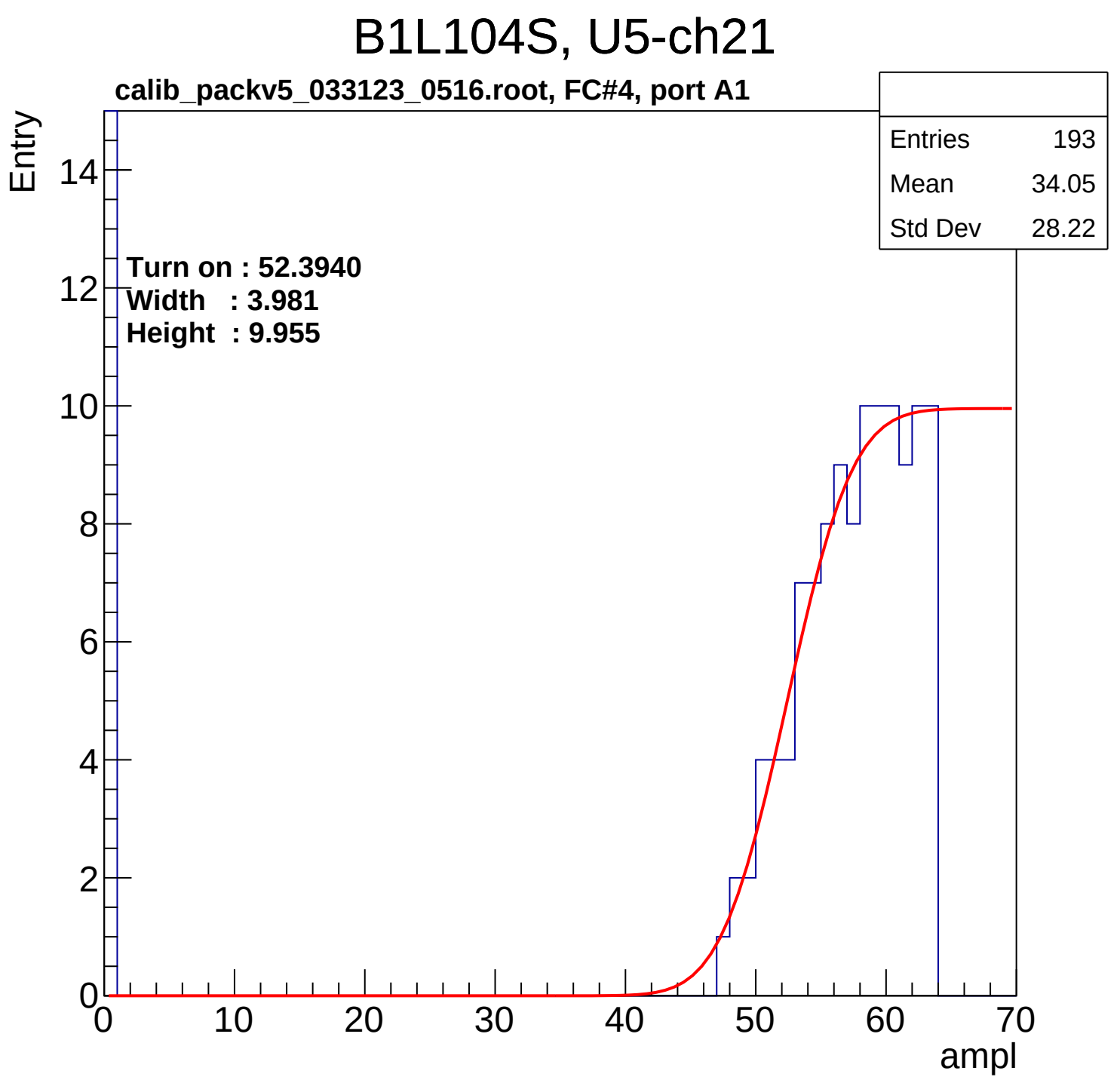

B1L104S, U5-ch16
calib_packv5_033123_0516.root, FC#4, port A1
Entries 234
Mean 34.18
Std Dev 27.33
Turn on : 49.0844
Width : 7.500
Height : 10.341
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

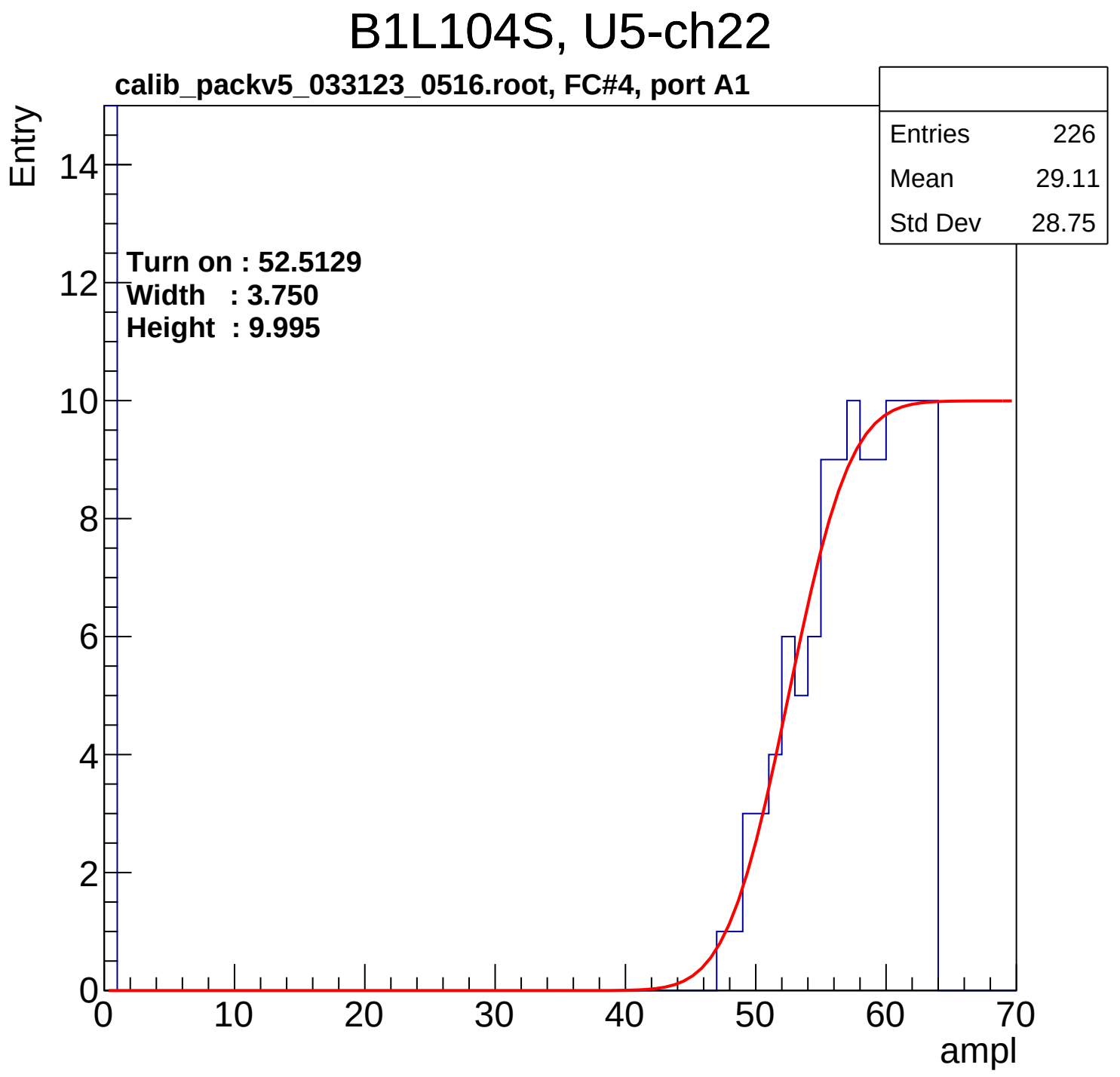

B1L104S, U5-ch17
calib_packv5_033123_0516.root, FC#4, port A1
Entries 216
Mean 33.41
Std Dev 28.15
Turn on : 50.8024
Width : 3.735
Height : 10.038
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

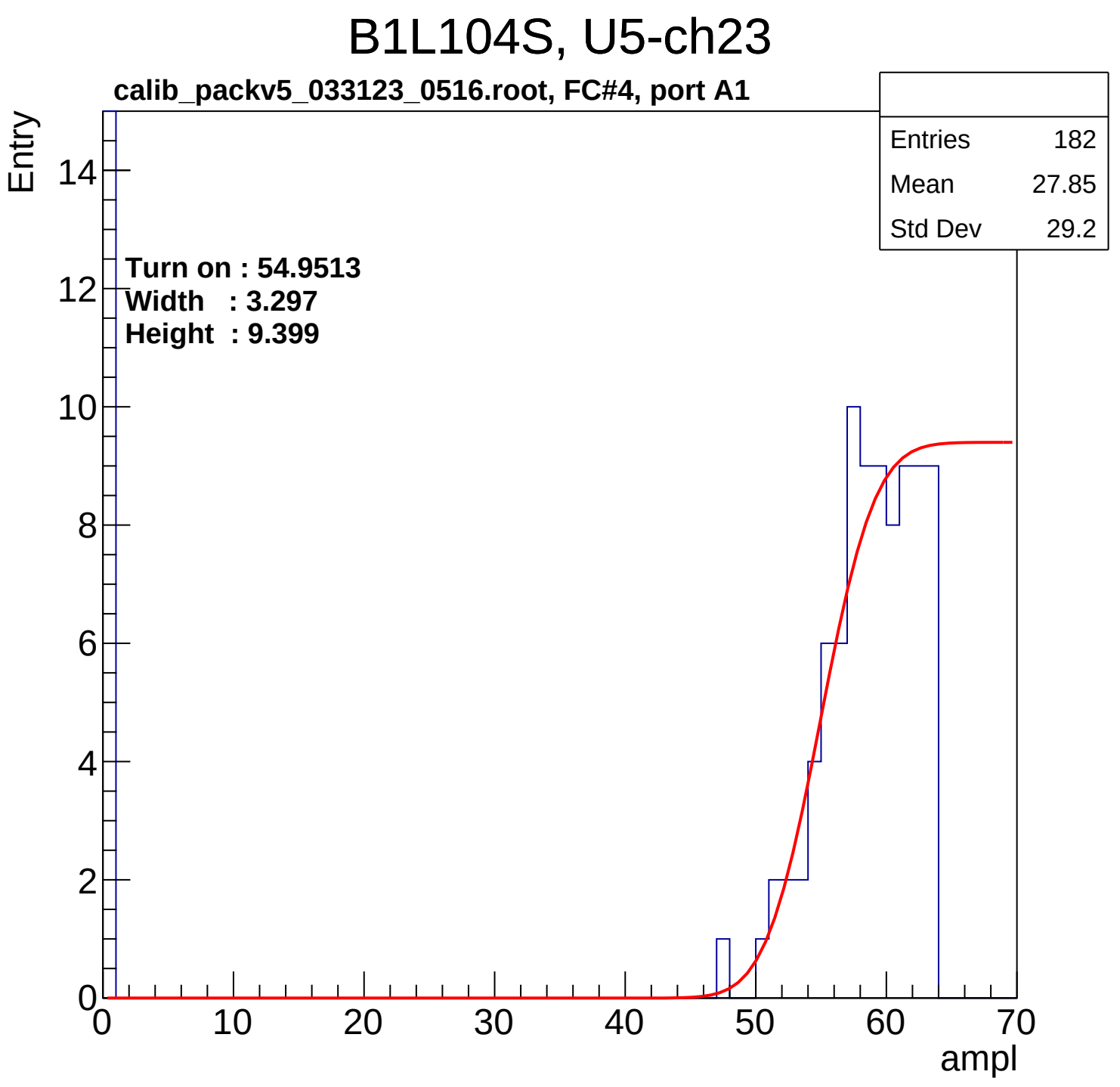

B1L104S, U5-ch18
calib_packv5_033123_0516.root, FC#4, port A1
Entries 179
Mean 34.99
Std Dev 28.22
Turn on : 54.1551
Width : 4.656
Height : 10.856
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

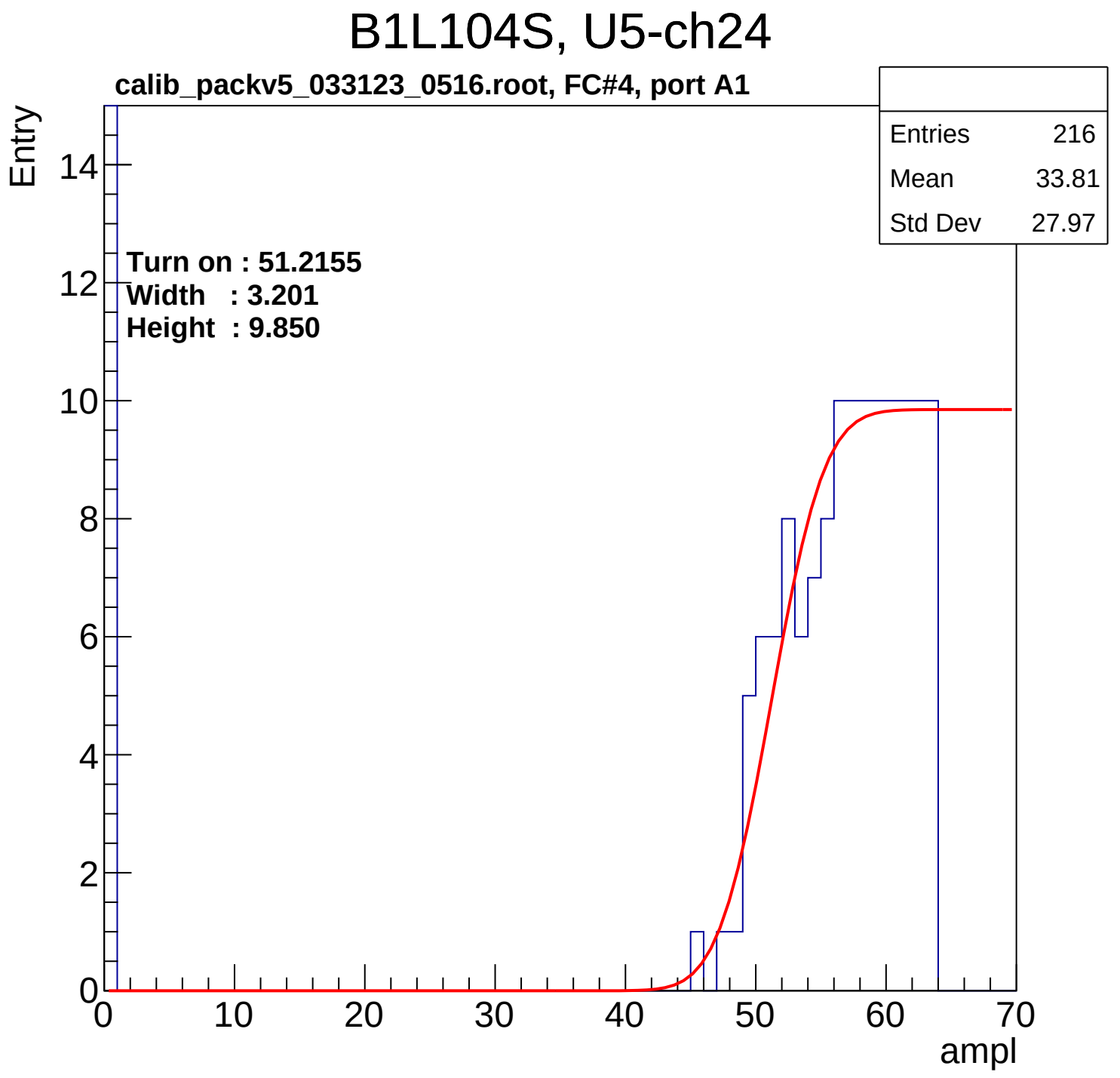

B1L104S, U5-ch19
calib_packv5_033123_0516.root, FC#4, port A1
Entries 193
Mean 32.49
Std Dev 28.68
Turn on : 54.4078
Width : 5.511
Height : 11.408
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

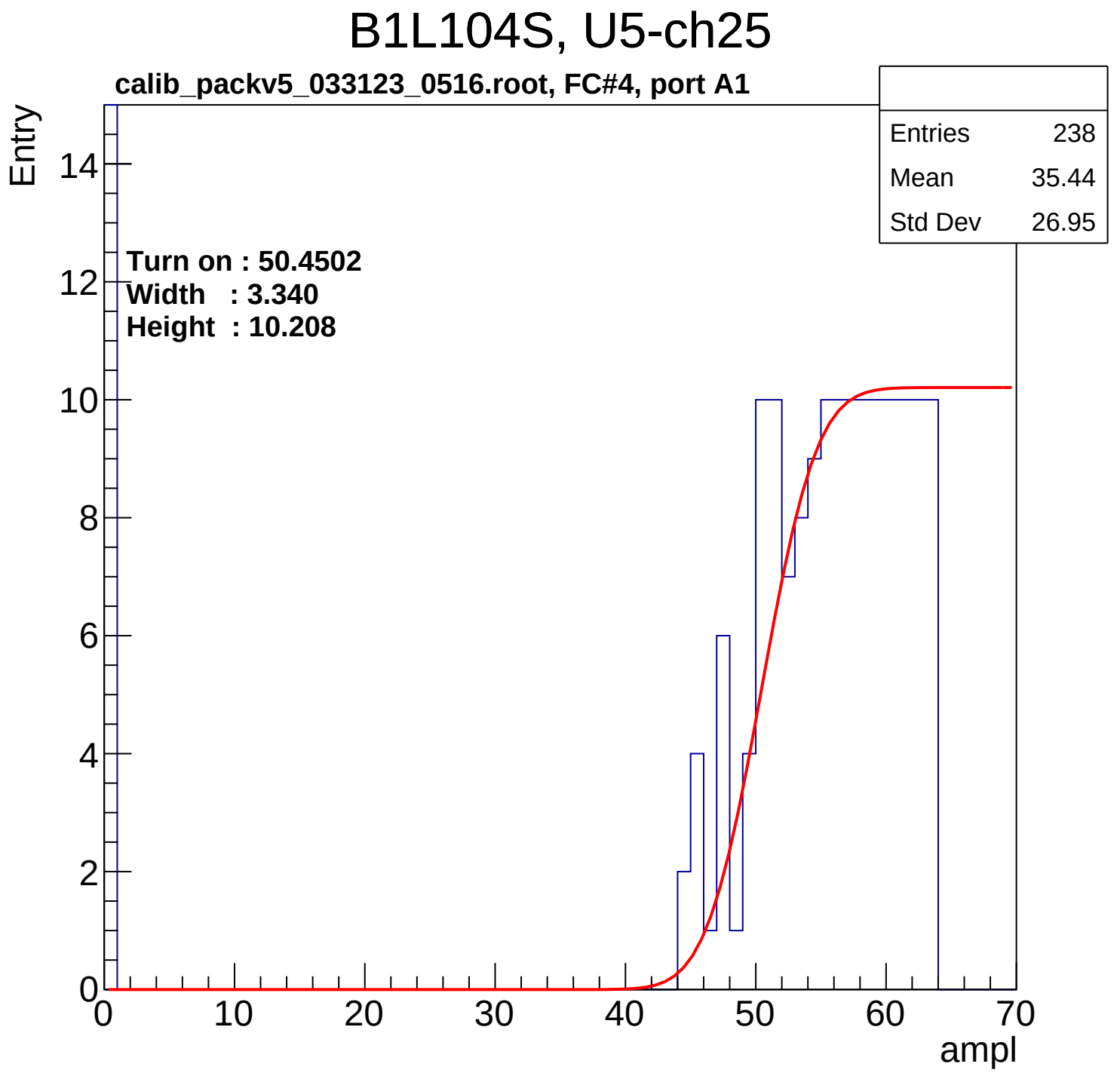

B1L104S, U5-ch20
calib_packv5_033123_0516.root, FC#4, port A1
Entries 197
Mean 32.68
Std Dev 28.62
Turn on : 53.2817
Width : 3.357
Height : 10.282
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

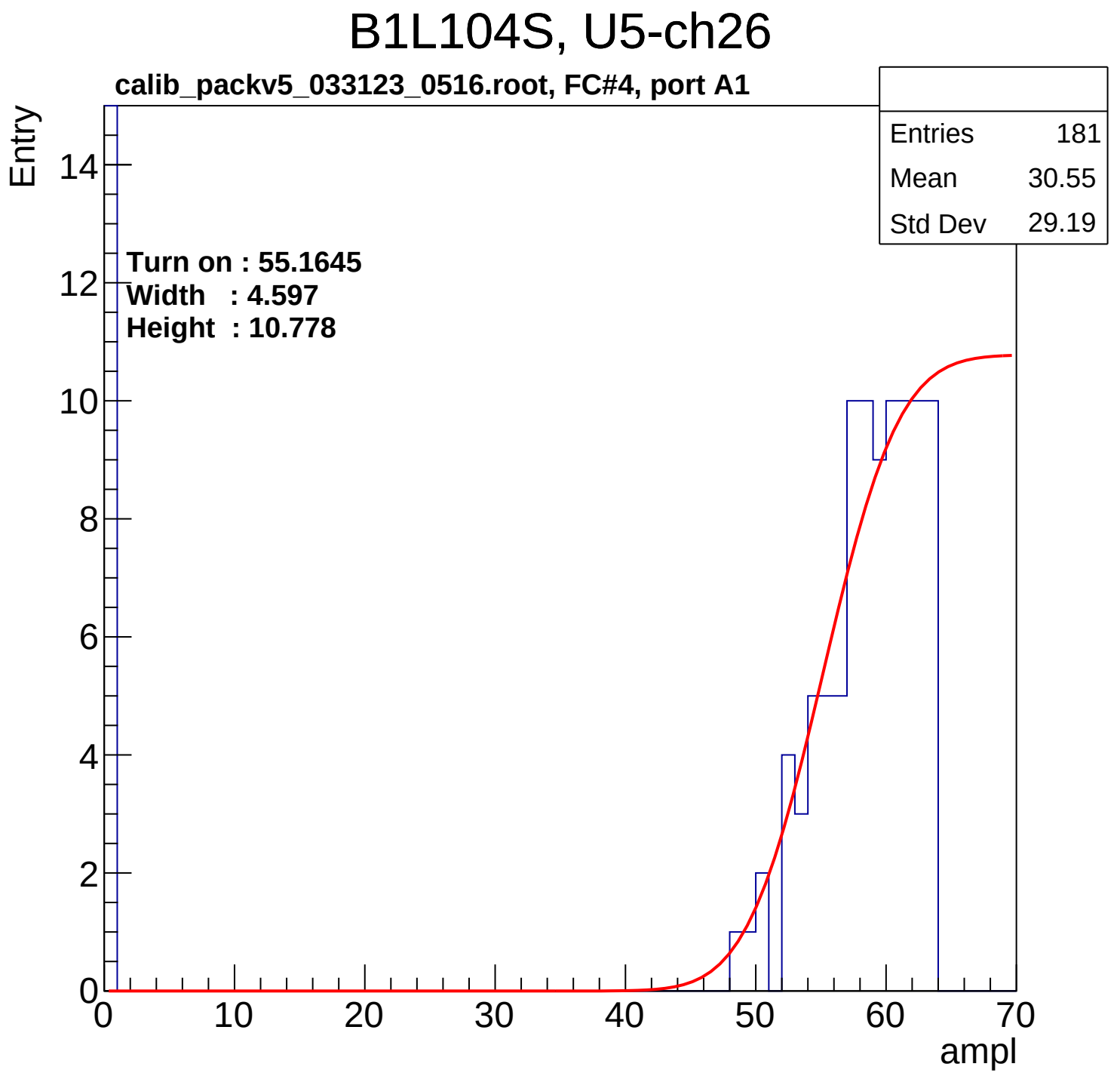

B1L104S, U5-ch21
calib_packv5_033123_0516.root, FC#4, port A1
Entries 193
Mean 34.05
Std Dev 28.22
Turn on : 52.3940
Width : 3.981
Height : 9.955
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

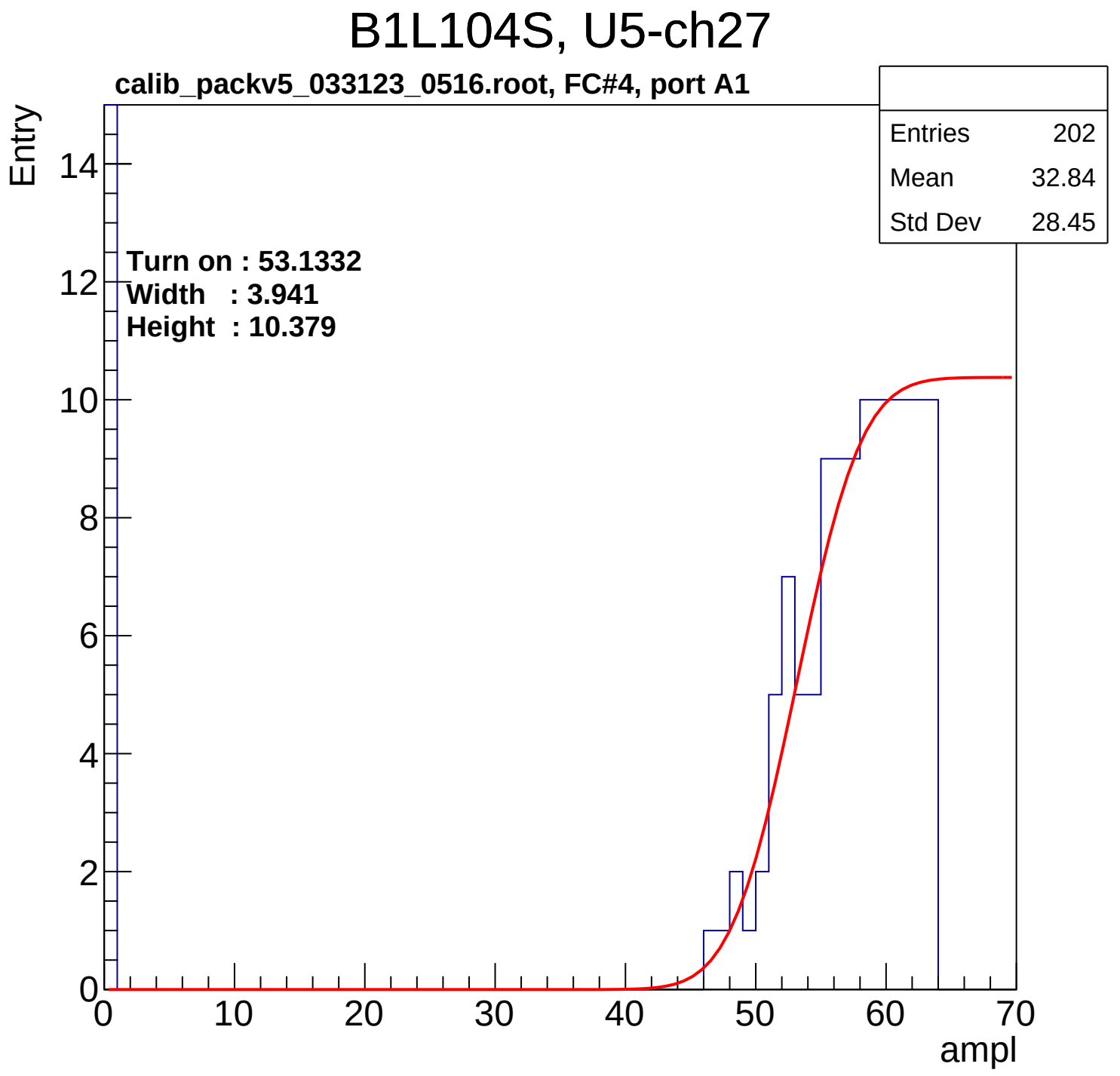

B1L104S, U5-ch22
calib_packv5_033123_0516.root, FC#4, port A1
Entries 226
Mean 29.11
Std Dev 28.75
Turn on : 52.5129
Width : 3.750
Height : 9.995
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

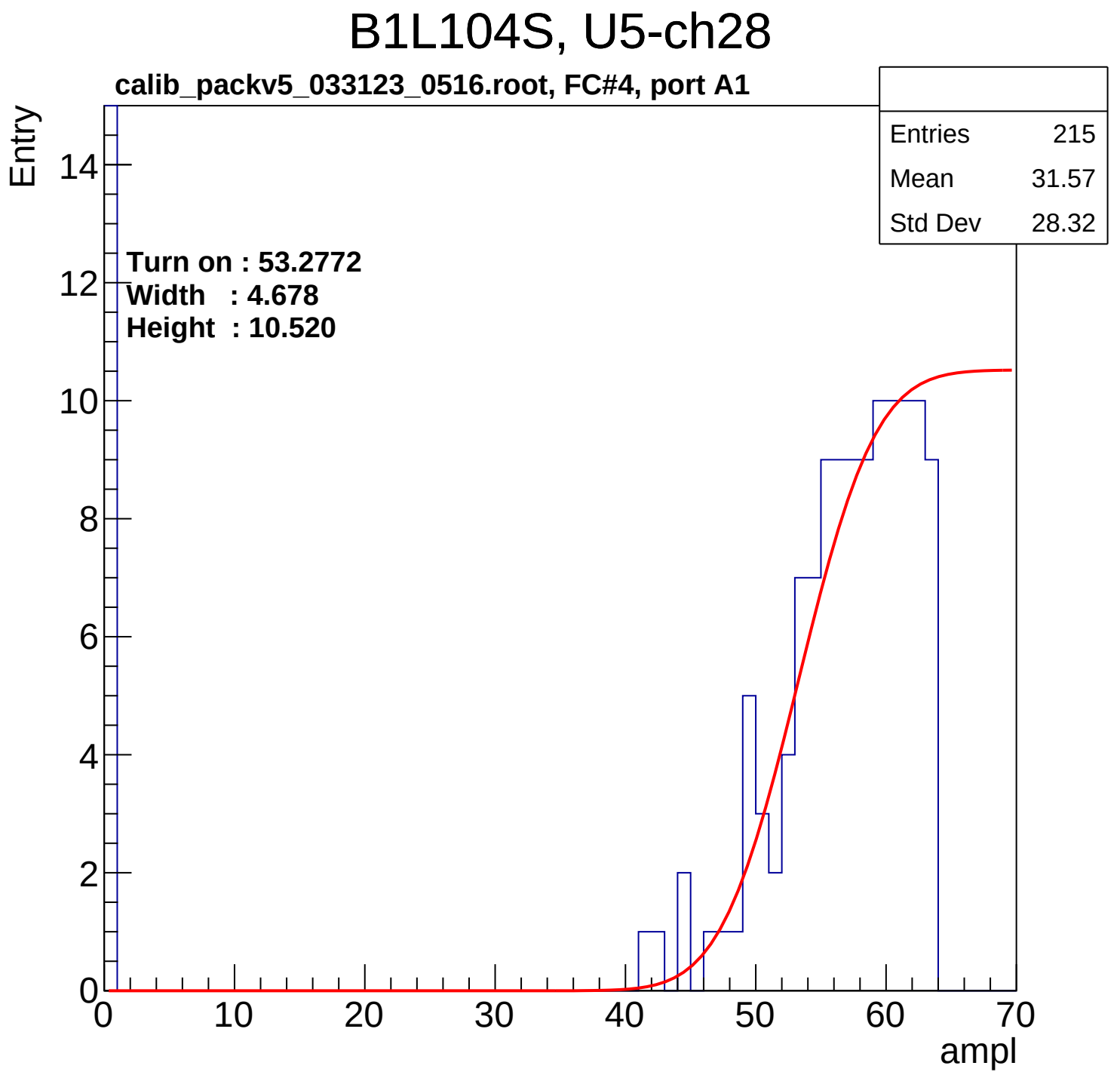

B1L104S, U5-ch23
calib_packv5_033123_0516.root, FC#4, port A1
Entries 182
Mean 27.85
Std Dev 29.2
Turn on : 54.9513
Width : 3.297
Height : 9.399
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

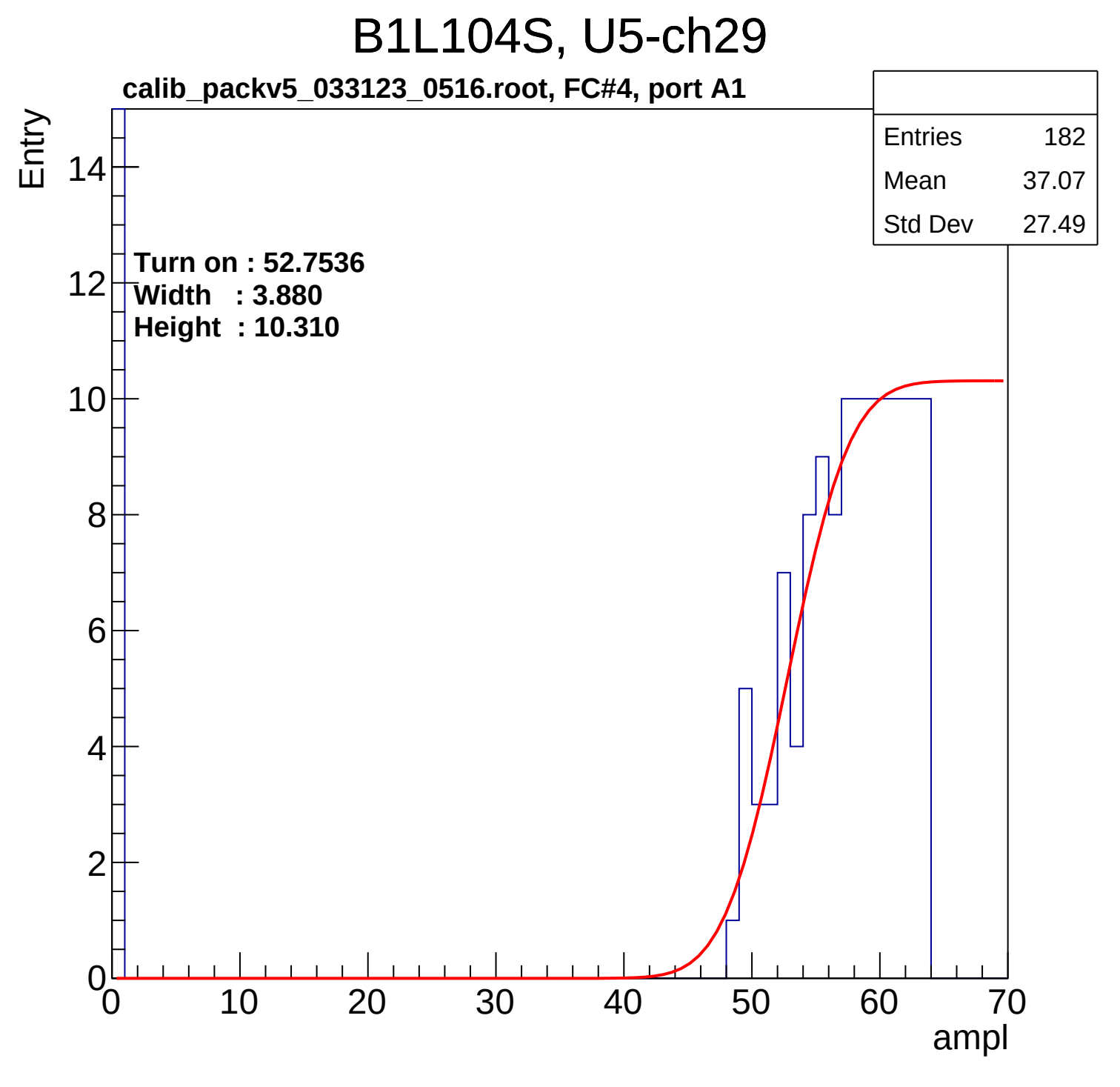

B1L104S, U5-ch24
calib_packv5_033123_0516.root, FC#4, port A1
Entries 216
Mean 33.81
Std Dev 27.97
Turn on : 51.2155
Width : 3.201
Height : 9.850
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

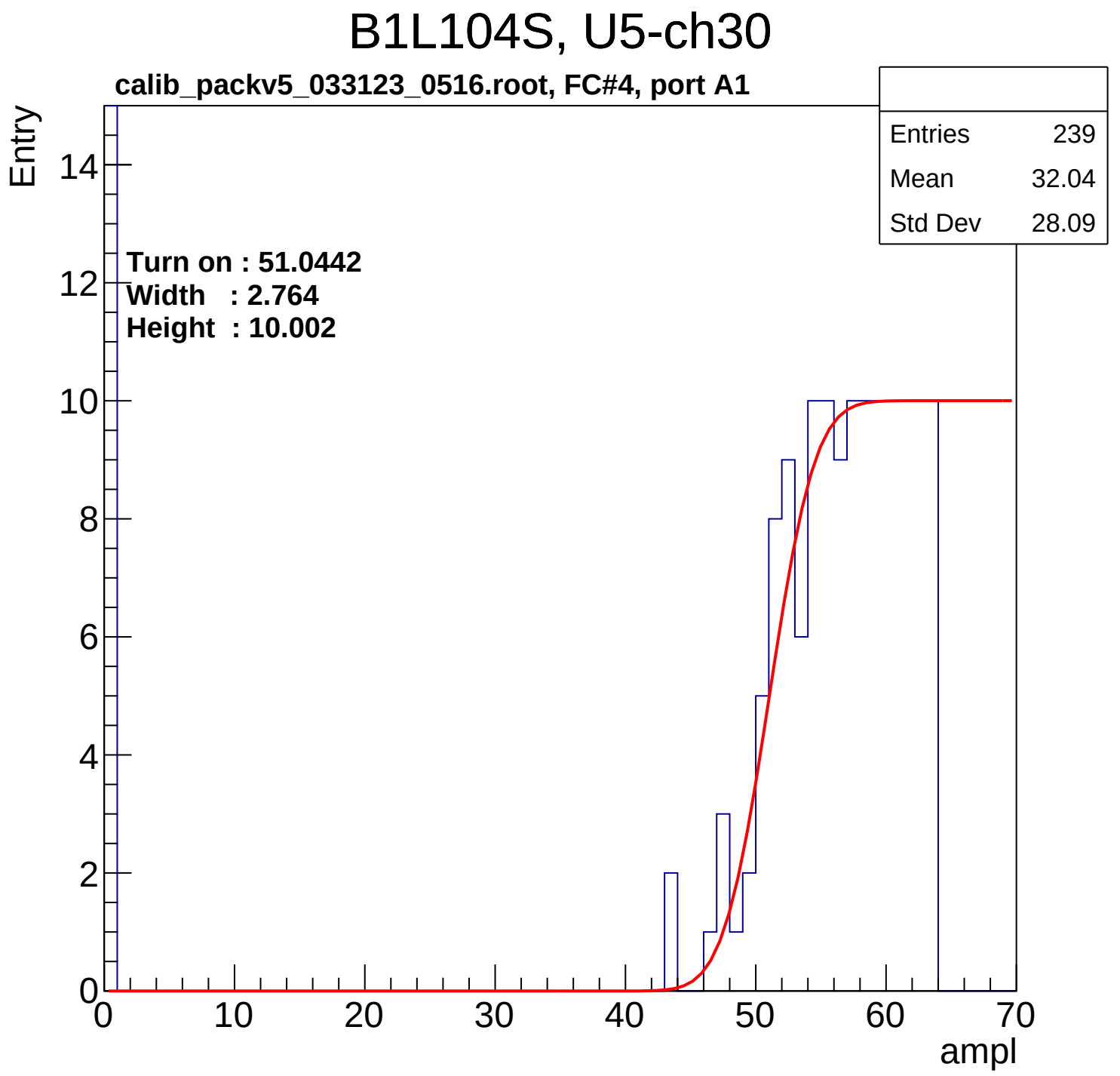

B1L104S, U5-ch25
calib_packv5_033123_0516.root, FC#4, port A1
Entries 238
Mean 35.44
Std Dev 26.95
Turn on : 50.4502
Width : 3.340
Height : 10.208
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

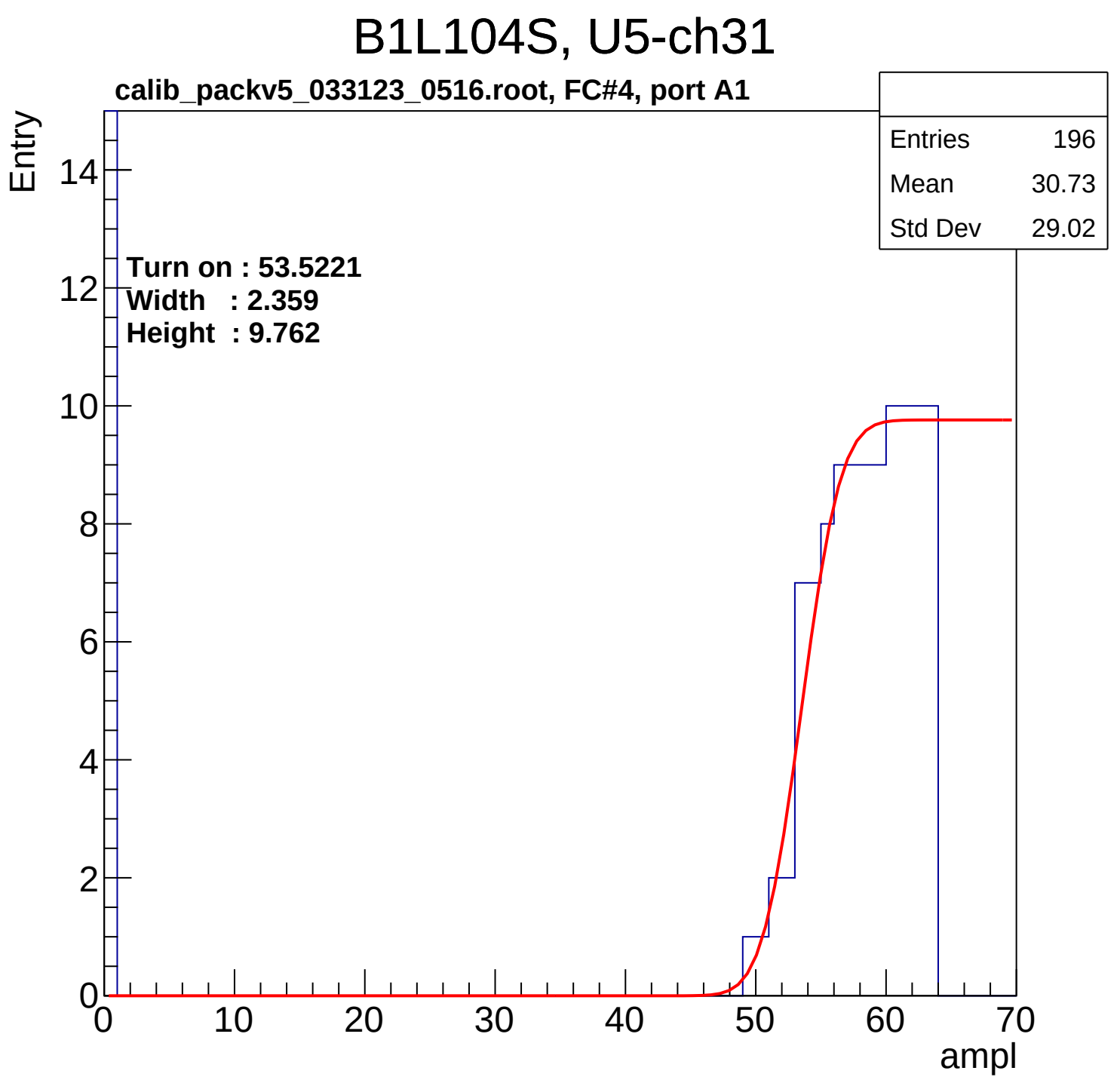

B1L104S, U5-ch26
calib_packv5_033123_0516.root, FC#4, port A1
Entries 181
Mean 30.55
Std Dev 29.19
Turn on : 55.1645
Width : 4.597
Height : 10.778
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

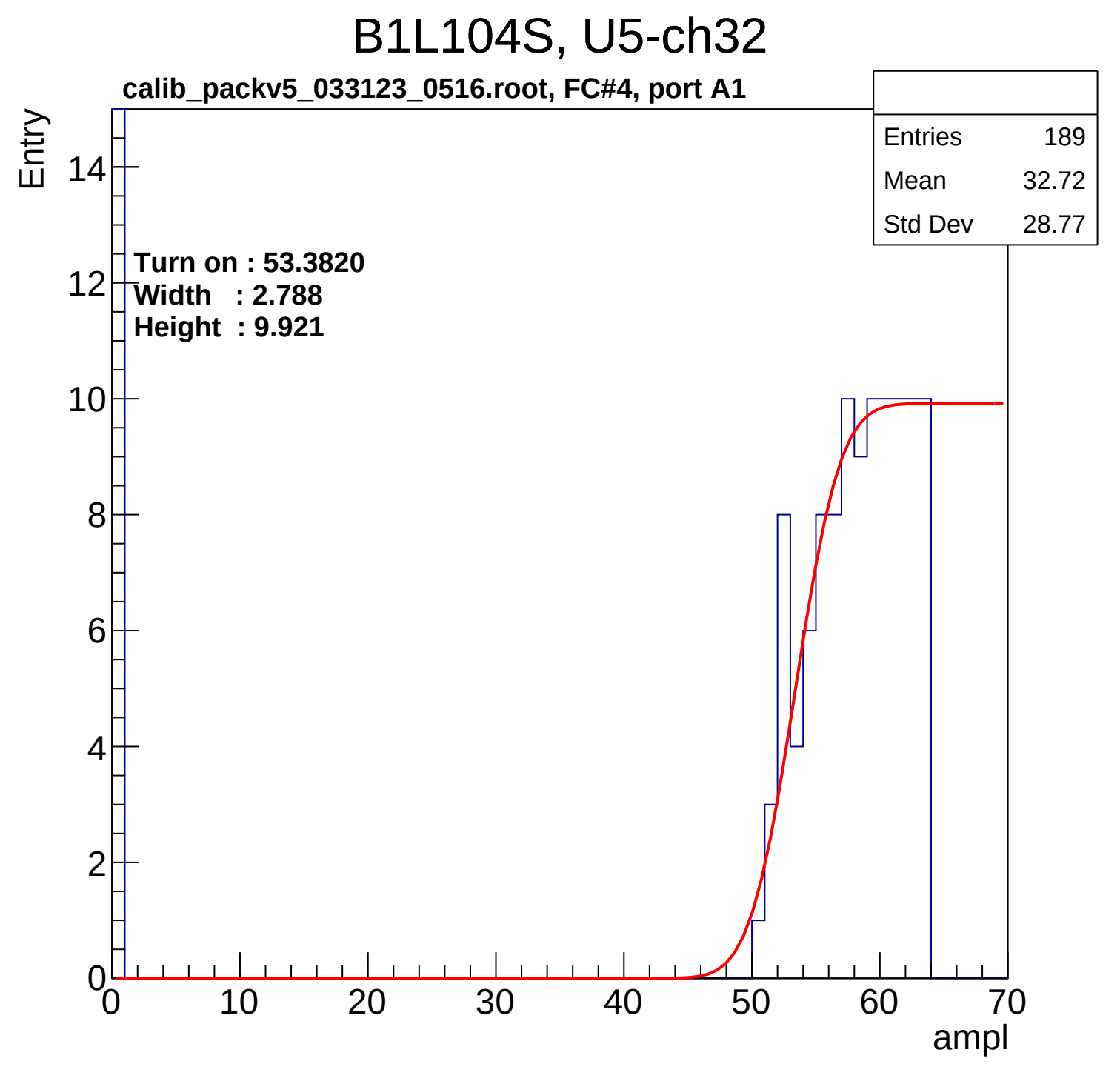

B1L104S, U5-ch27
calib_packv5_033123_0516.root, FC#4, port A1
Entries 202
Mean 32.84
Std Dev 28.45
Turn on : 53.1332
Width : 3.941
Height : 10.379
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

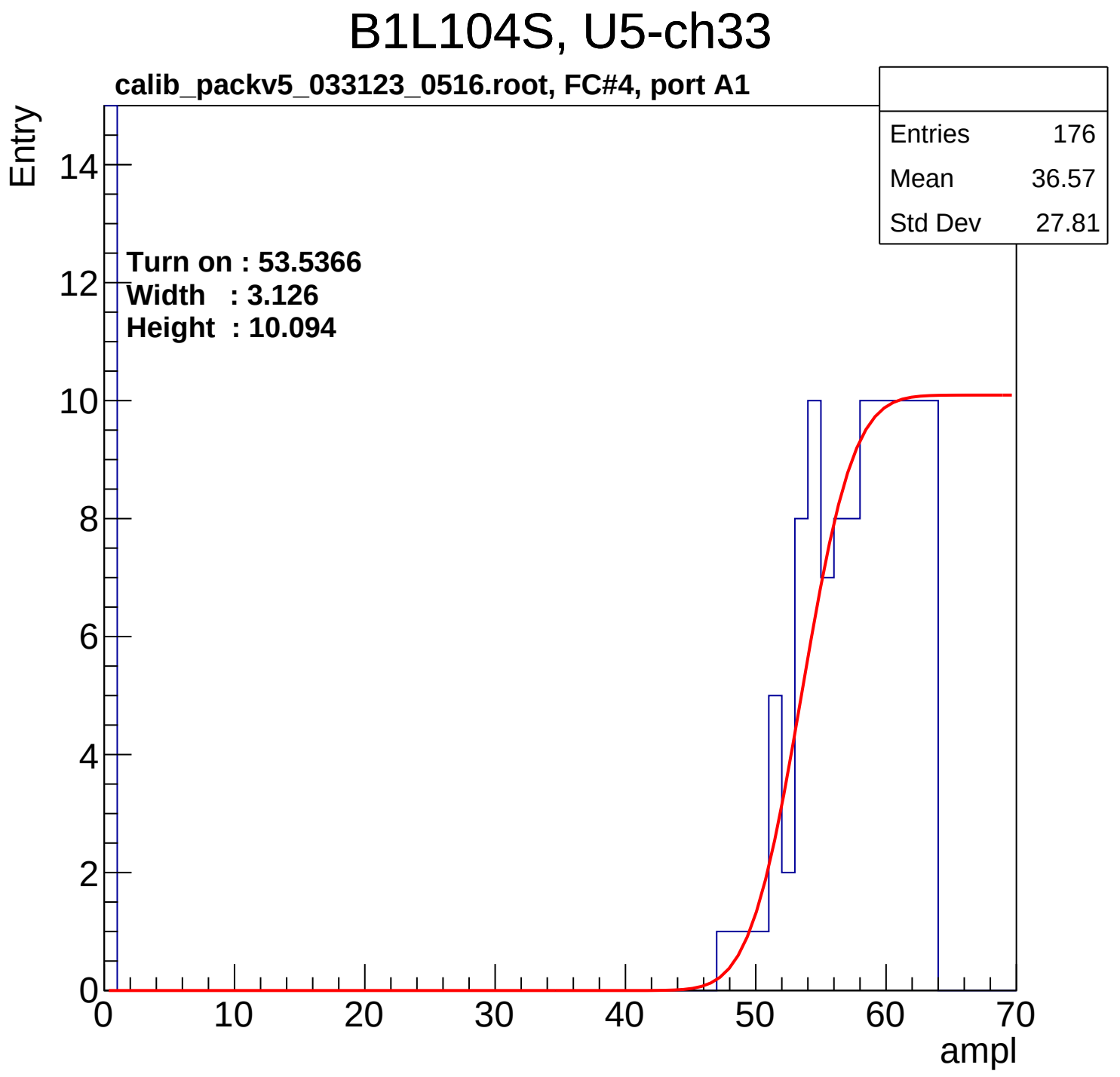

B1L104S, U5-ch28
calib_packv5_033123_0516.root, FC#4, port A1
Entries 215
Mean 31.57
Std Dev 28.32
Turn on : 53.2772
Width : 4.678
Height : 10.520
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

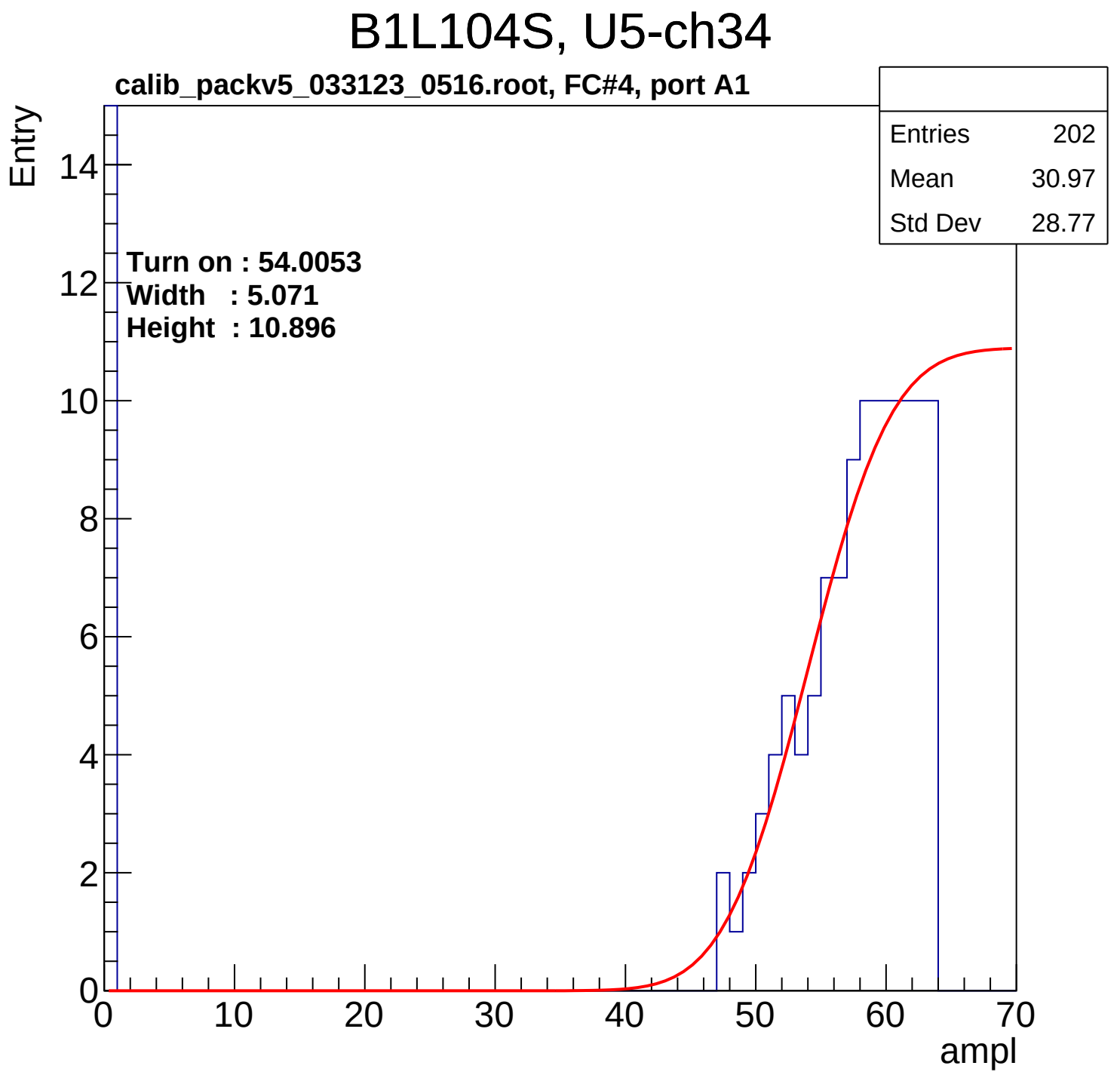

B1L104S, U5-ch29
calib_packv5_033123_0516.root, FC#4, port A1
Entries 182
Mean 37.07
Std Dev 27.49
Turn on : 52.7536
Width : 3.880
Height : 10.310
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

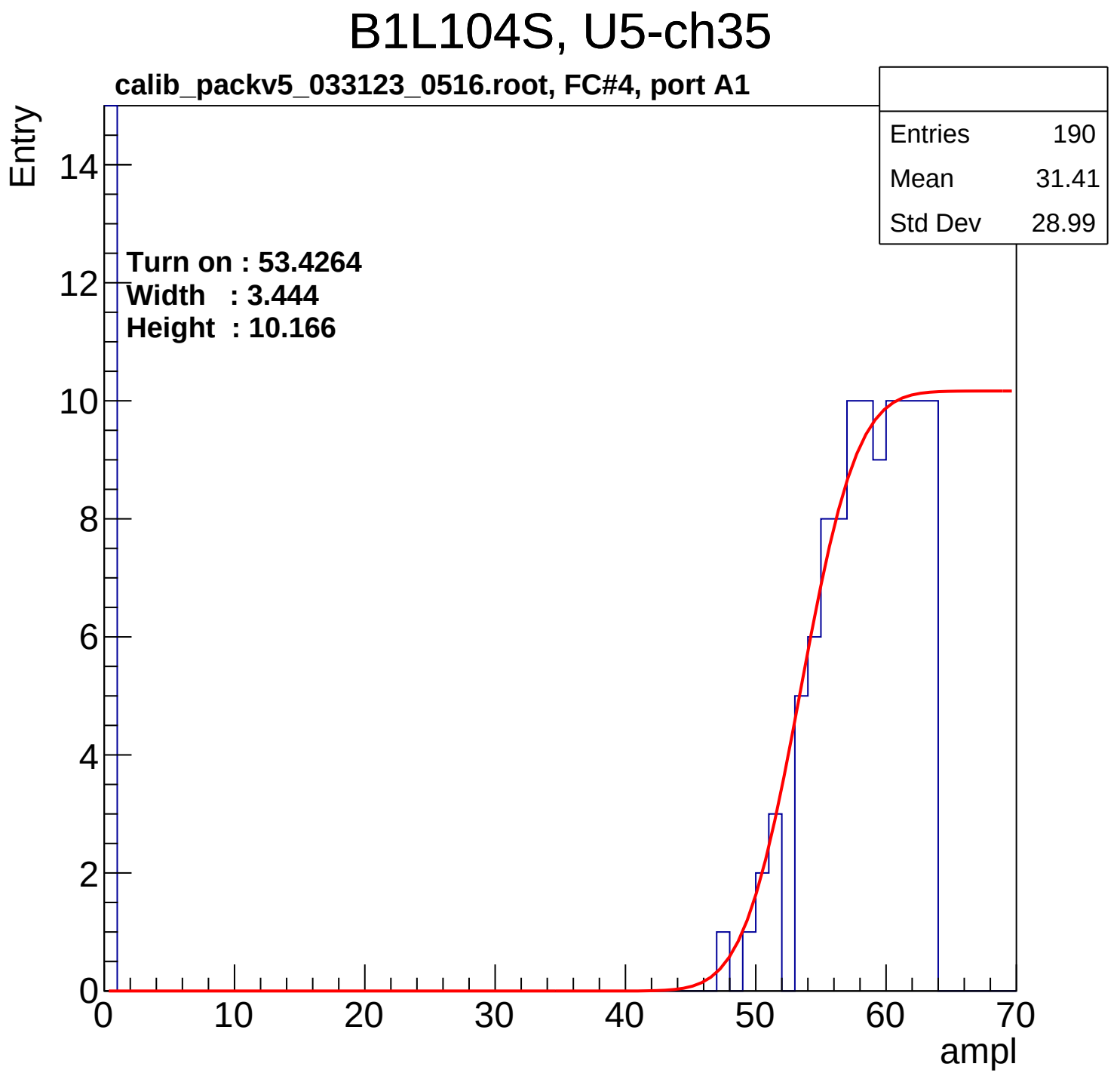

B1L104S, U5-ch30
calib_packv5_033123_0516.root, FC#4, port A1
Entries 239
Mean 32.04
Std Dev 28.09
Turn on : 51.0442
Width : 2.764
Height : 10.002
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

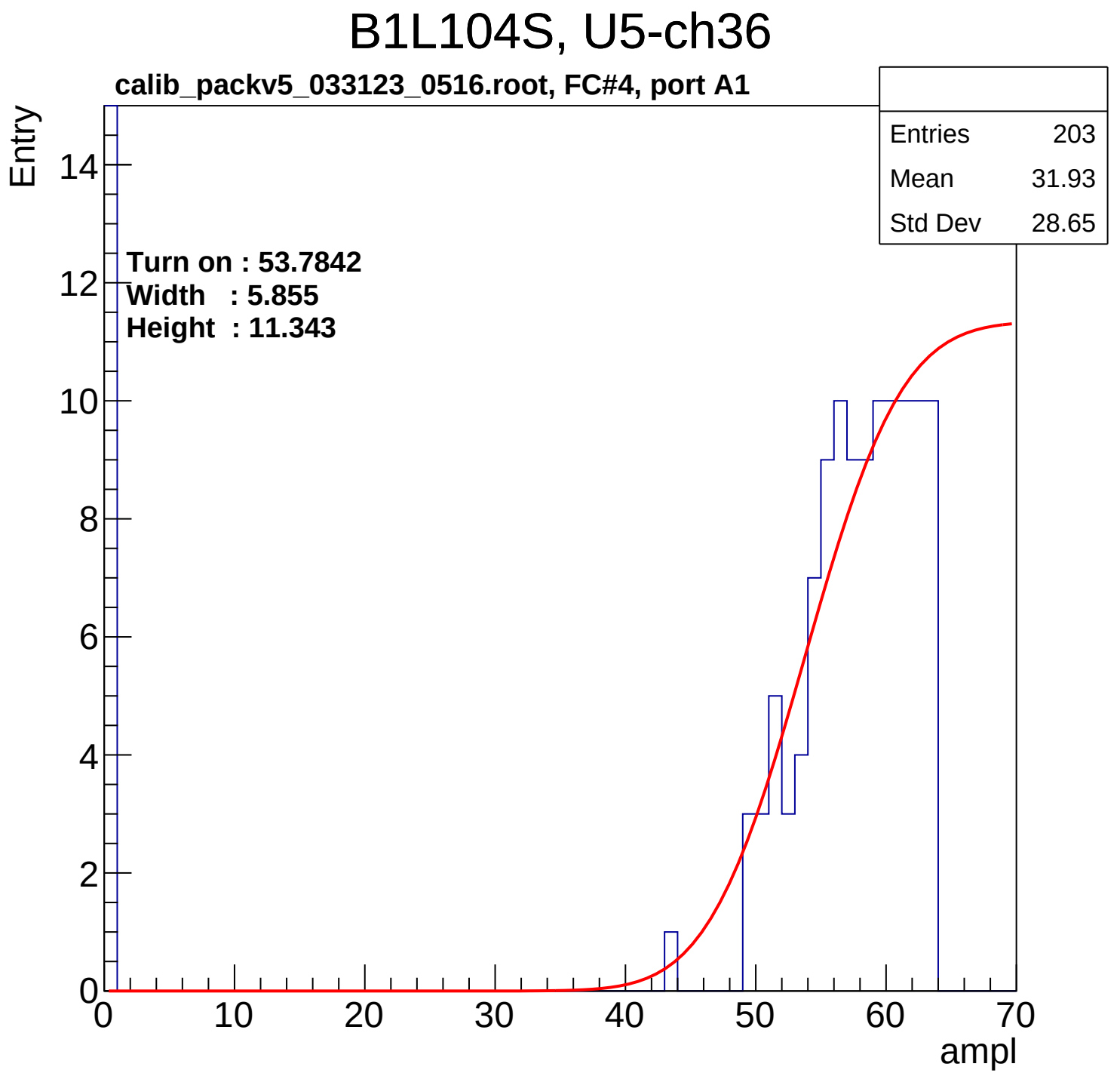

B1L104S, U5-ch31
calib_packv5_033123_0516.root, FC#4, port A1
Entries 196
Mean 30.73
Std Dev 29.02
Turn on : 53.5221
Width : 2.359
Height : 9.762
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

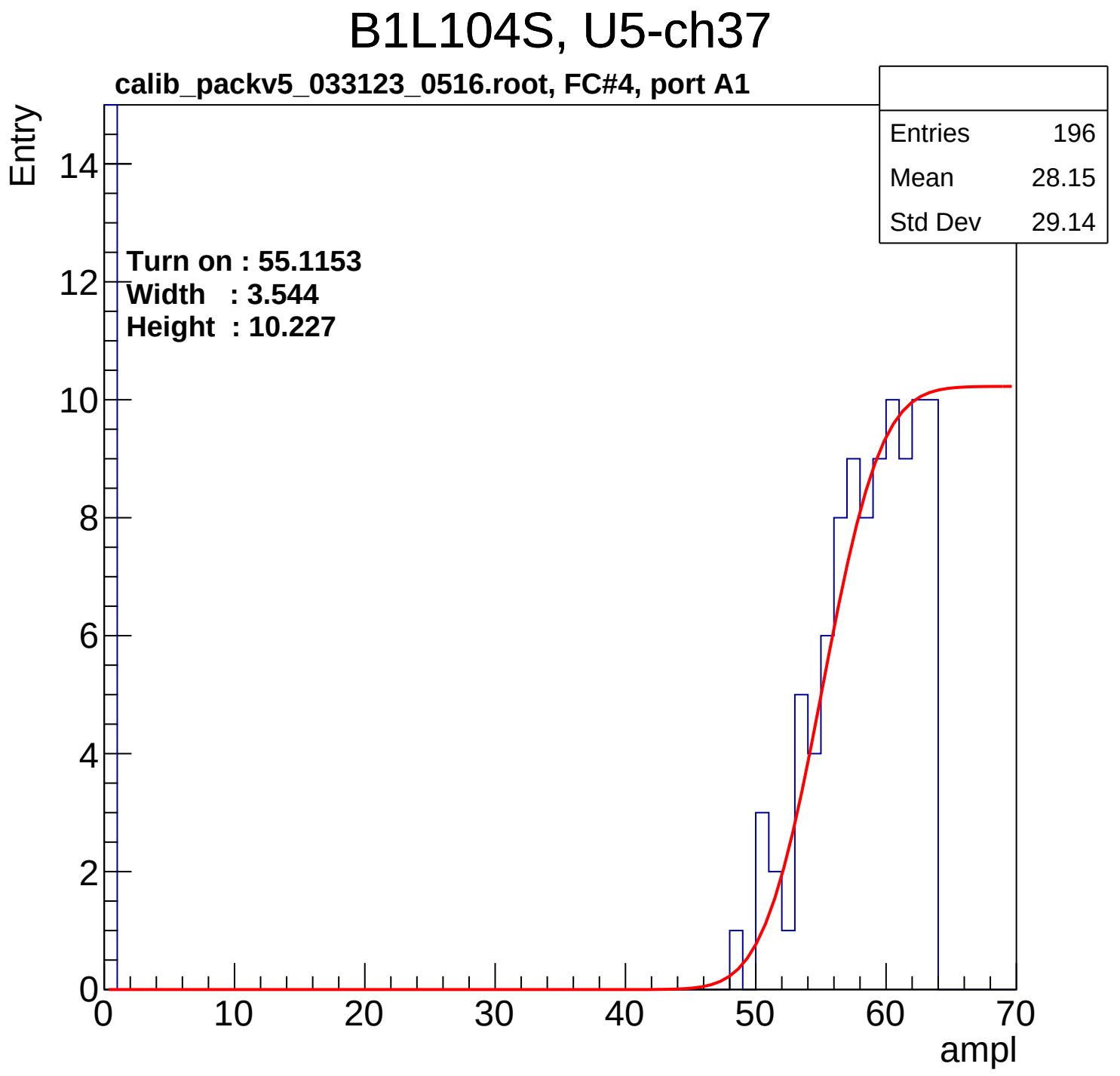

B1L104S, U5-ch32
calib_packv5_033123_0516.root, FC#4, port A1
Entries 189
Mean 32.72
Std Dev 28.77
Turn on : 53.3820
Width : 2.788
Height : 9.921
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

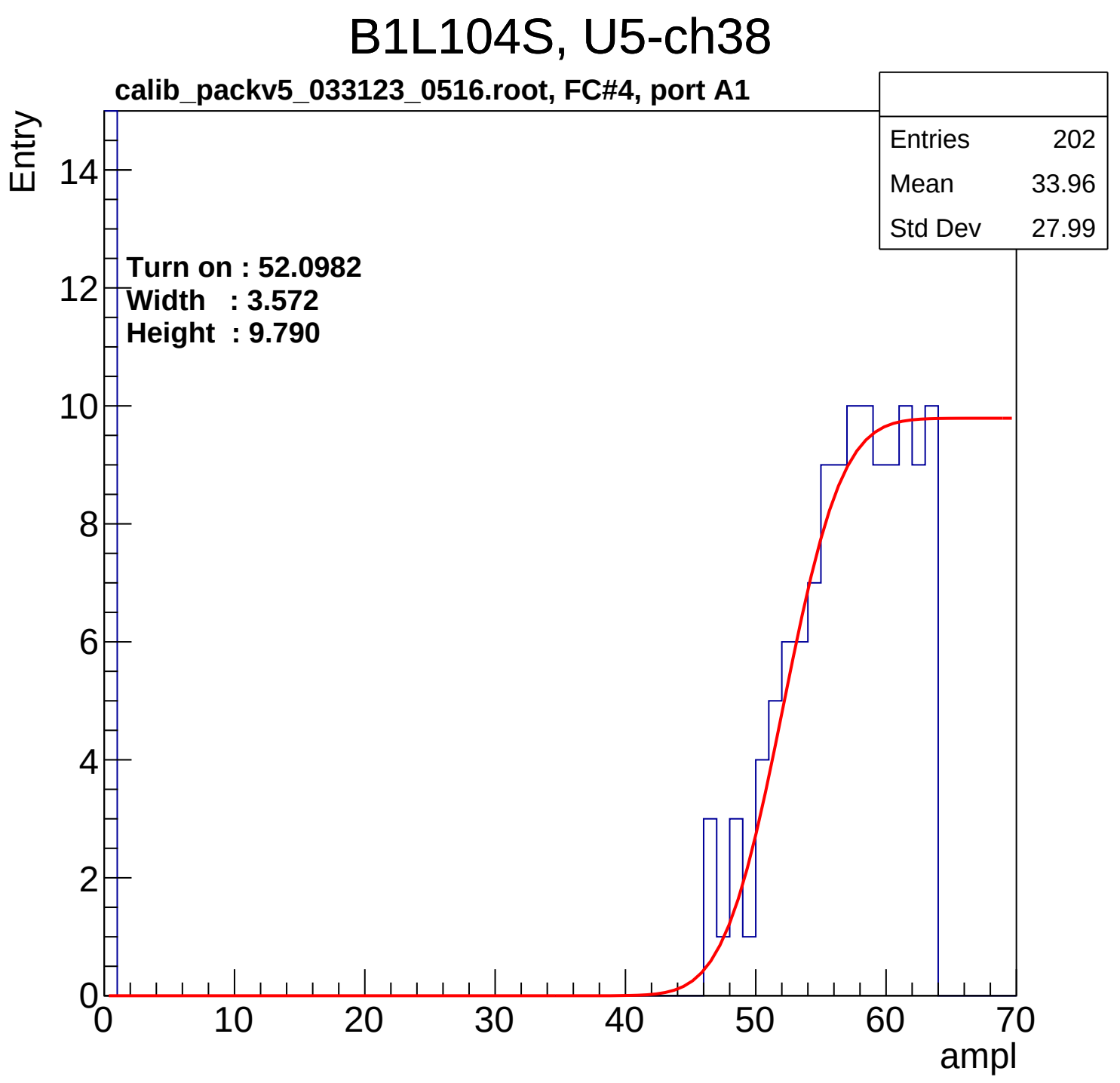

B1L104S, U5-ch33
calib_packv5_033123_0516.root, FC#4, port A1
Entries 176
Mean 36.57
Std Dev 27.81
Turn on : 53.5366
Width : 3.126
Height : 10.094
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

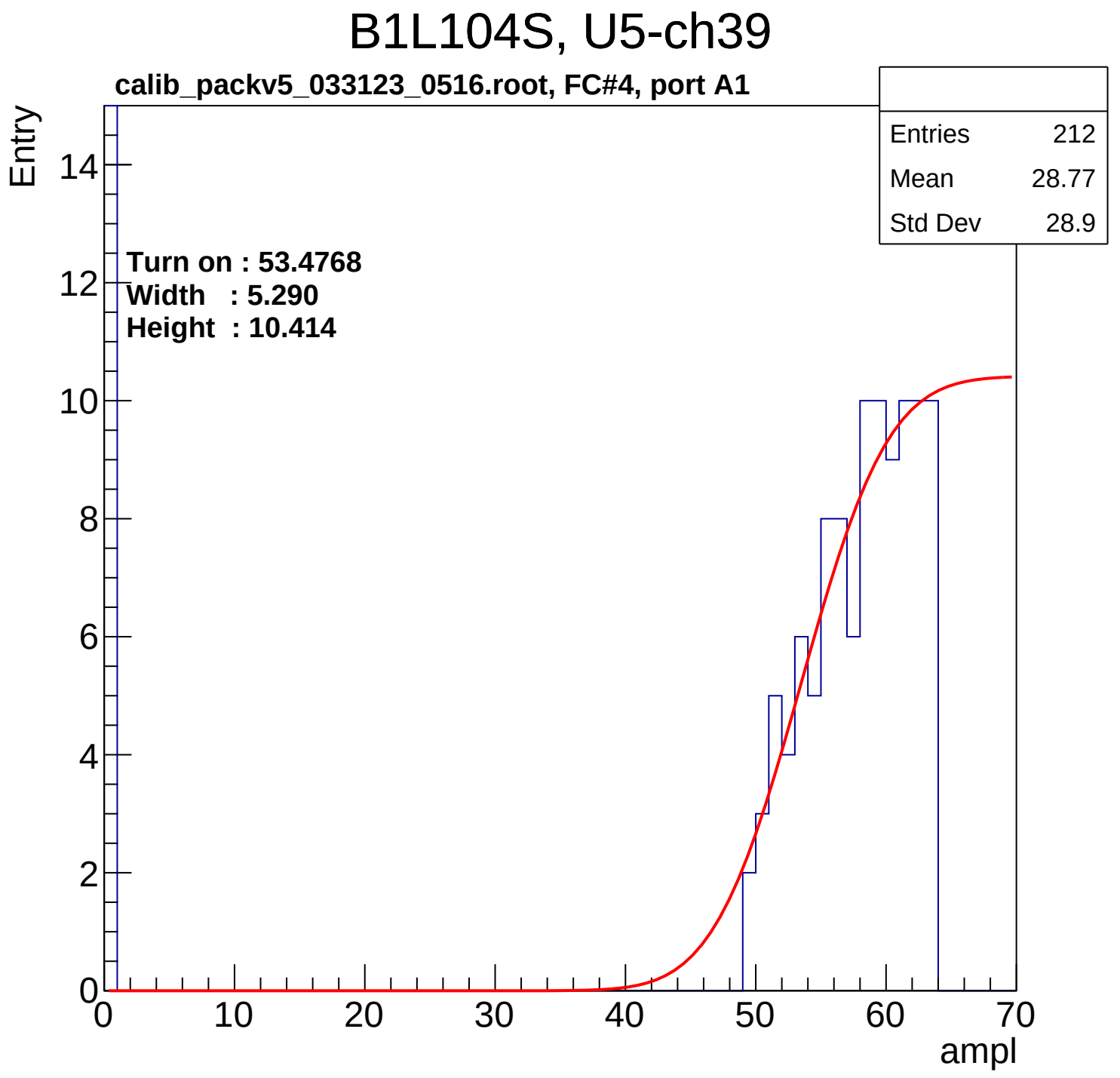

B1L104S, U5-ch34
calib_packv5_033123_0516.root, FC#4, port A1
Entries 202
Mean 30.97
Std Dev 28.77
Turn on : 54.0053
Width : 5.071
Height : 10.896
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

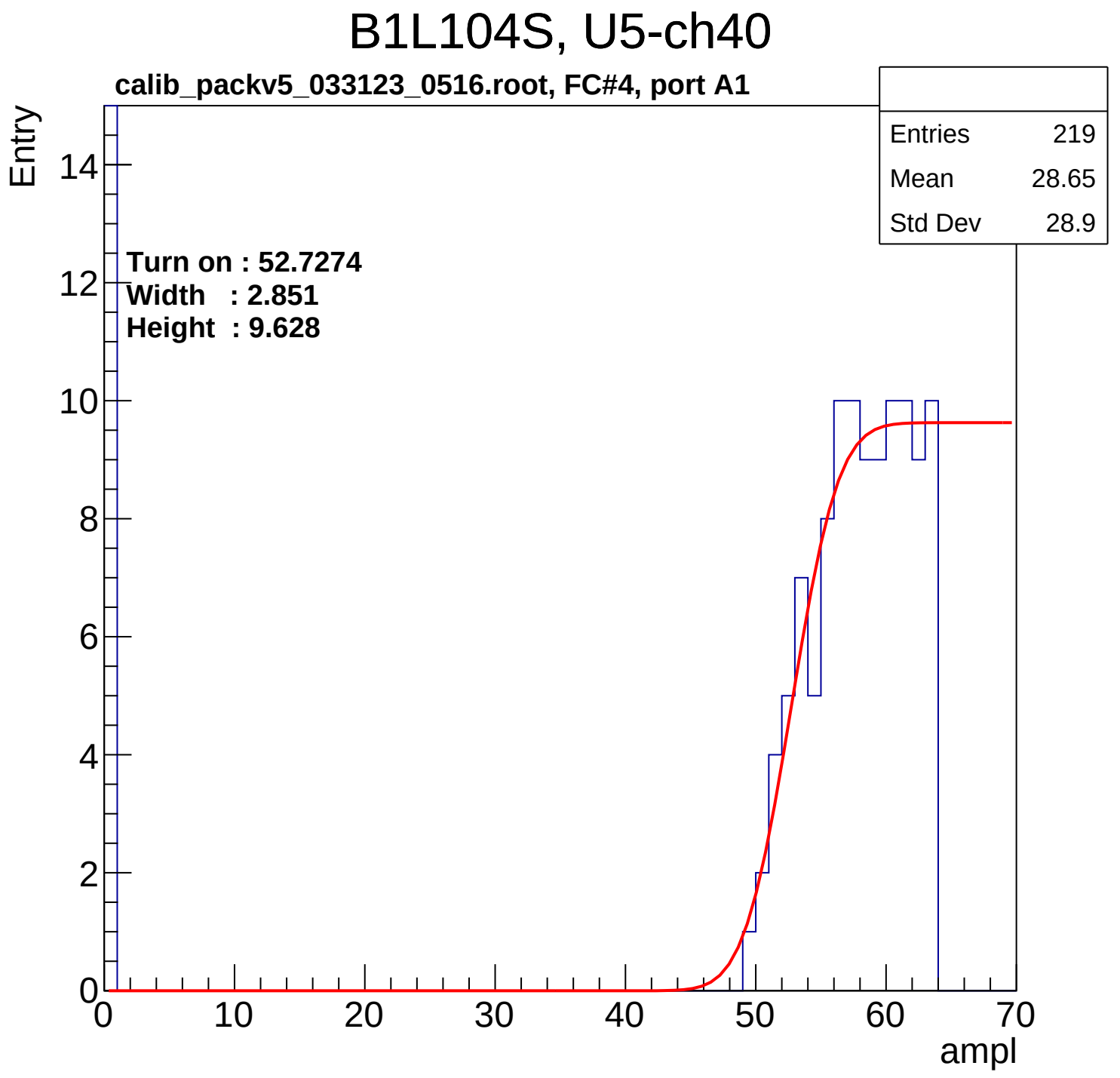

B1L104S, U5-ch35
calib_packv5_033123_0516.root, FC#4, port A1
Entries 190
Mean 31.41
Std Dev 28.99
Turn on : 53.4264
Width : 3.444
Height : 10.166
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

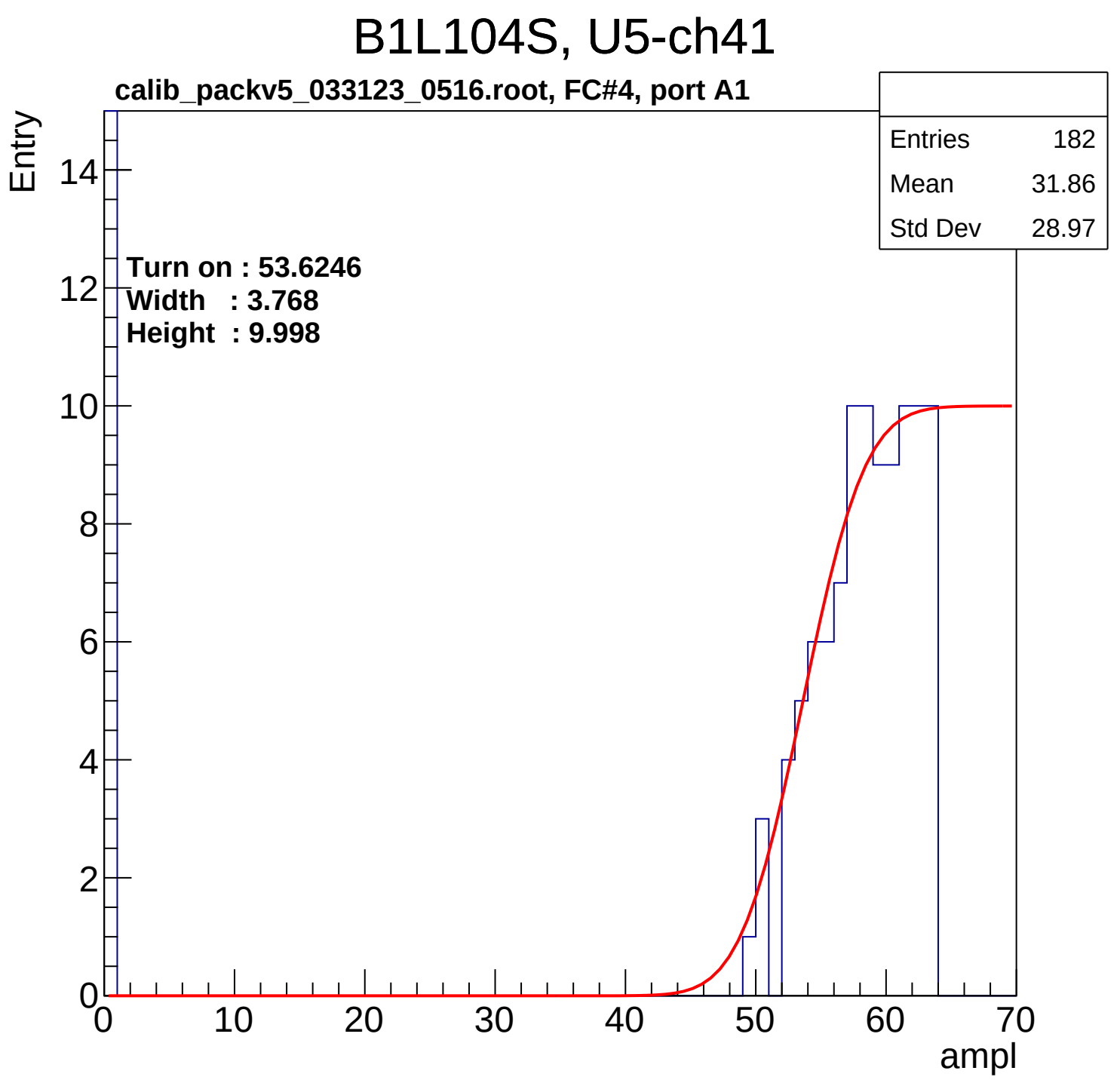

B1L104S, U5-ch36
calib_packv5_033123_0516.root, FC#4, port A1
Entries 203
Mean 31.93
Std Dev 28.65
Turn on : 53.7842
Width : 5.855
Height : 11.343
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

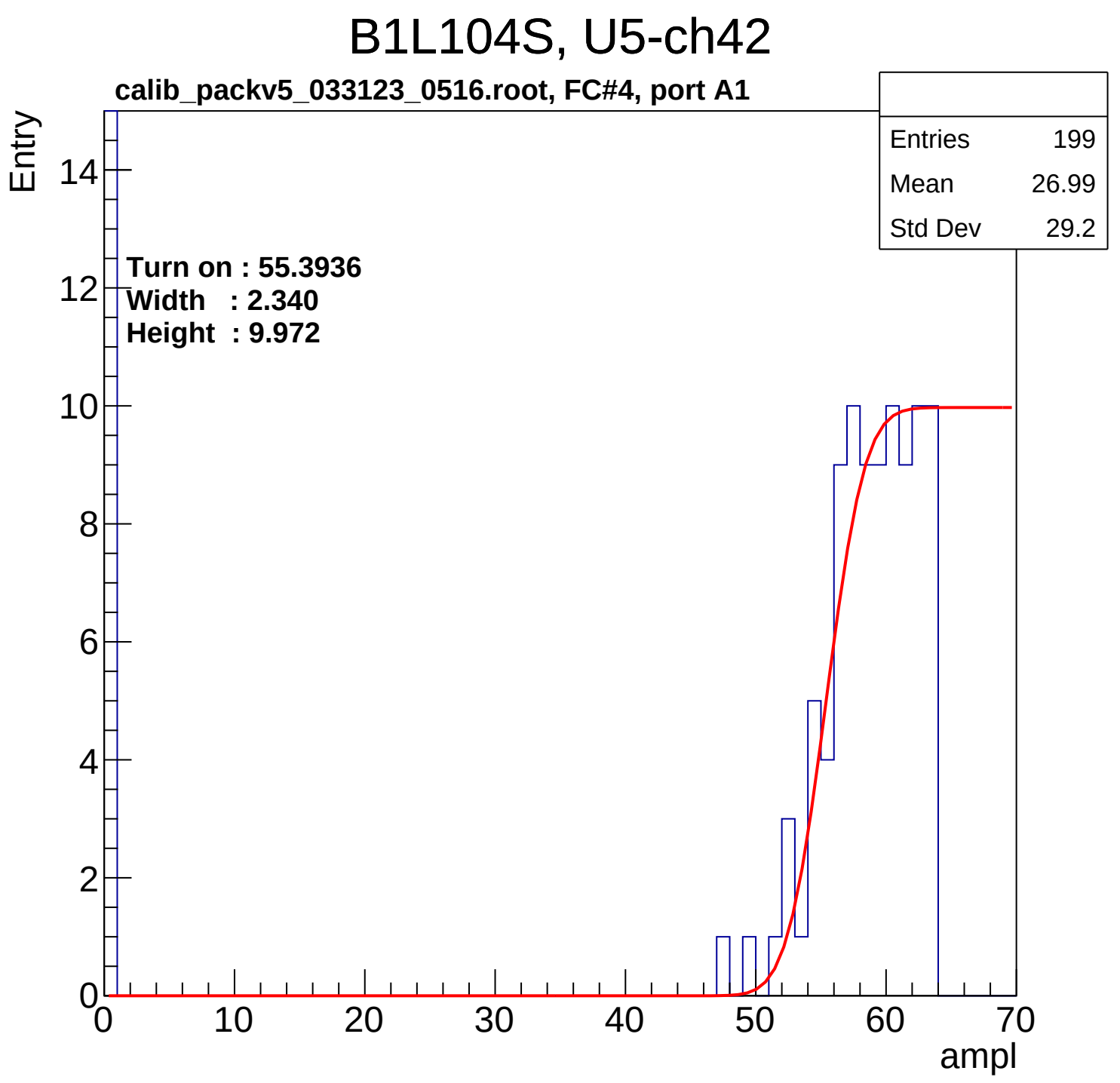

B1L104S, U5-ch37
calib_packv5_033123_0516.root, FC#4, port A1
Entries 196
Mean 28.15
Std Dev 29.14
Turn on : 55.1153
Width : 3.544
Height : 10.227
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

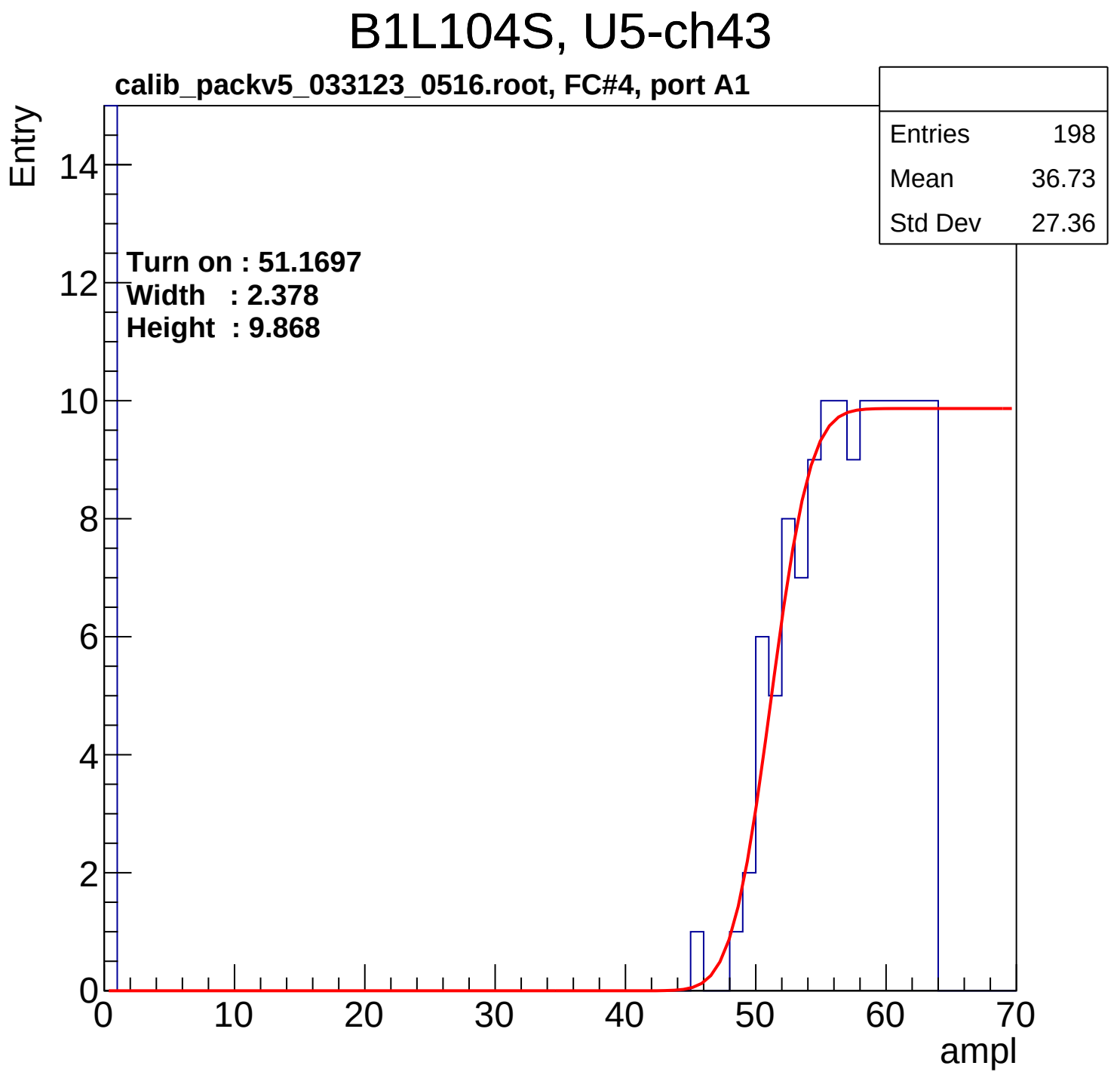

B1L104S, U5-ch38
calib_packv5_033123_0516.root, FC#4, port A1
Entries 202
Mean 33.96
Std Dev 27.99
Turn on : 52.0982
Width : 3.572
Height : 9.790
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

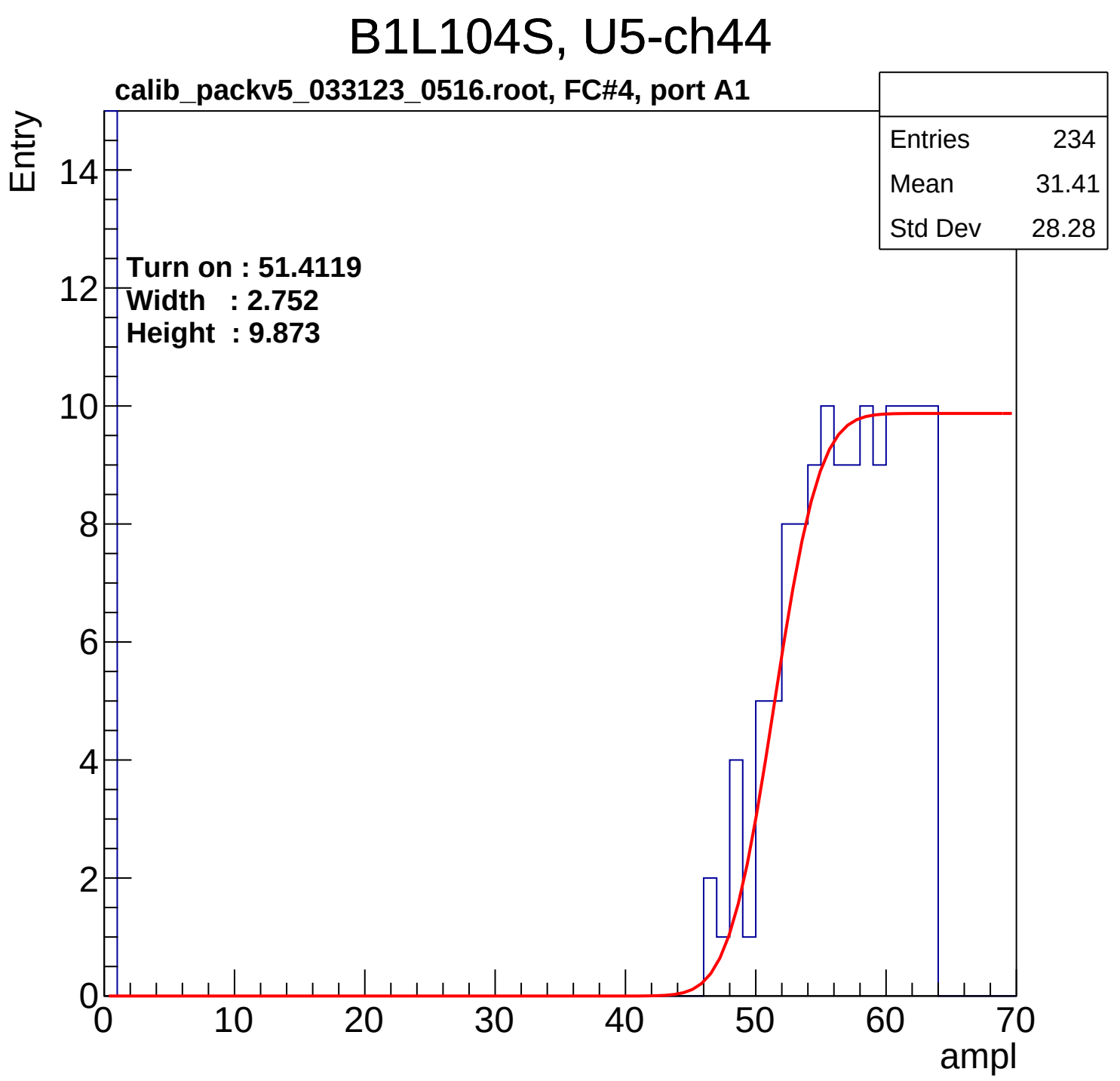

B1L104S, U5-ch39
calib_packv5_033123_0516.root, FC#4, port A1
Entries 212
Mean 28.77
Std Dev 28.9
Turn on : 53.4768
Width : 5.290
Height : 10.414
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

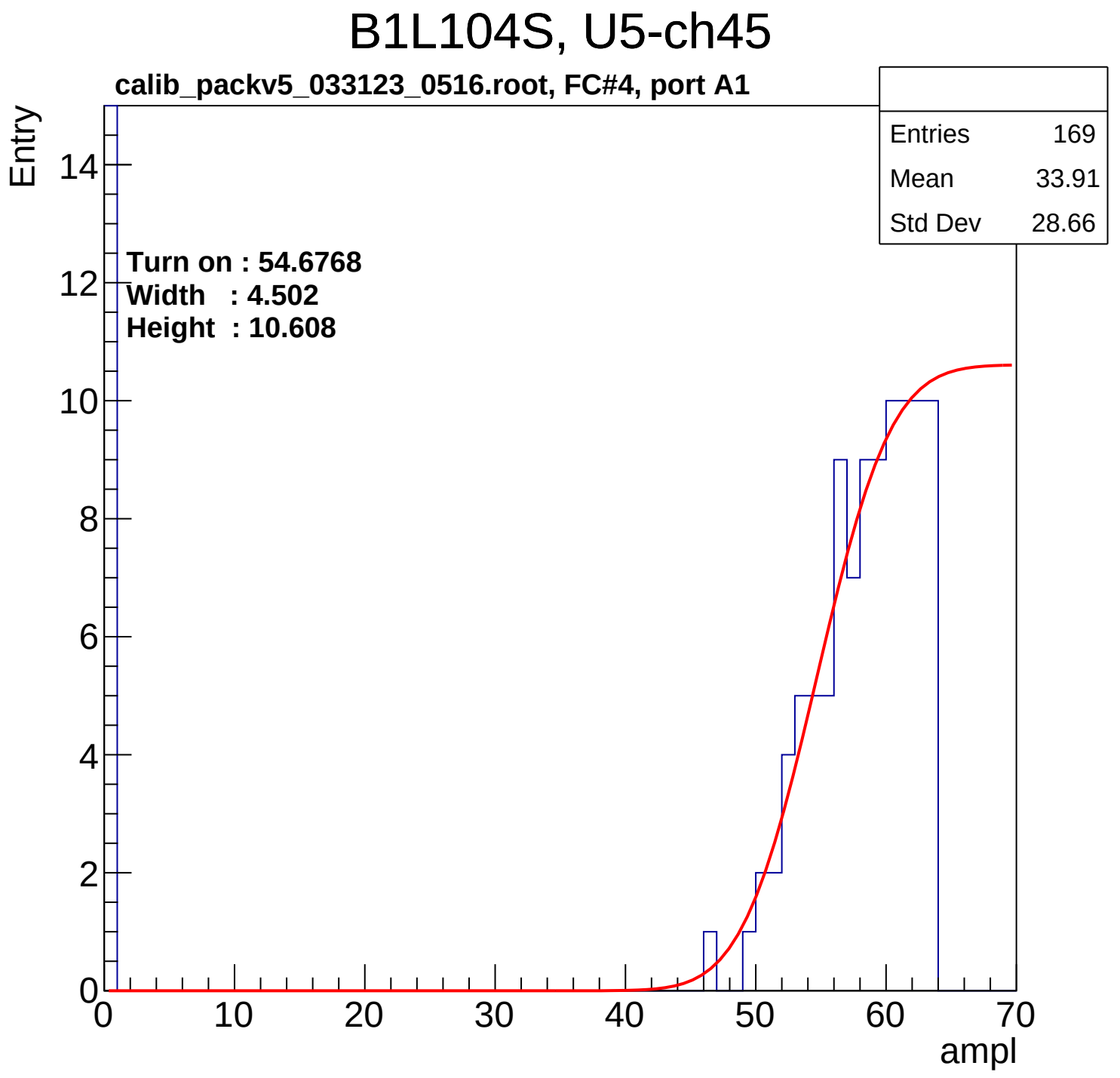

B1L104S, U5-ch40
calib_packv5_033123_0516.root, FC#4, port A1
Entries 219
Mean 28.65
Std Dev 28.9
Turn on : 52.7274
Width : 2.851
Height : 9.628
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

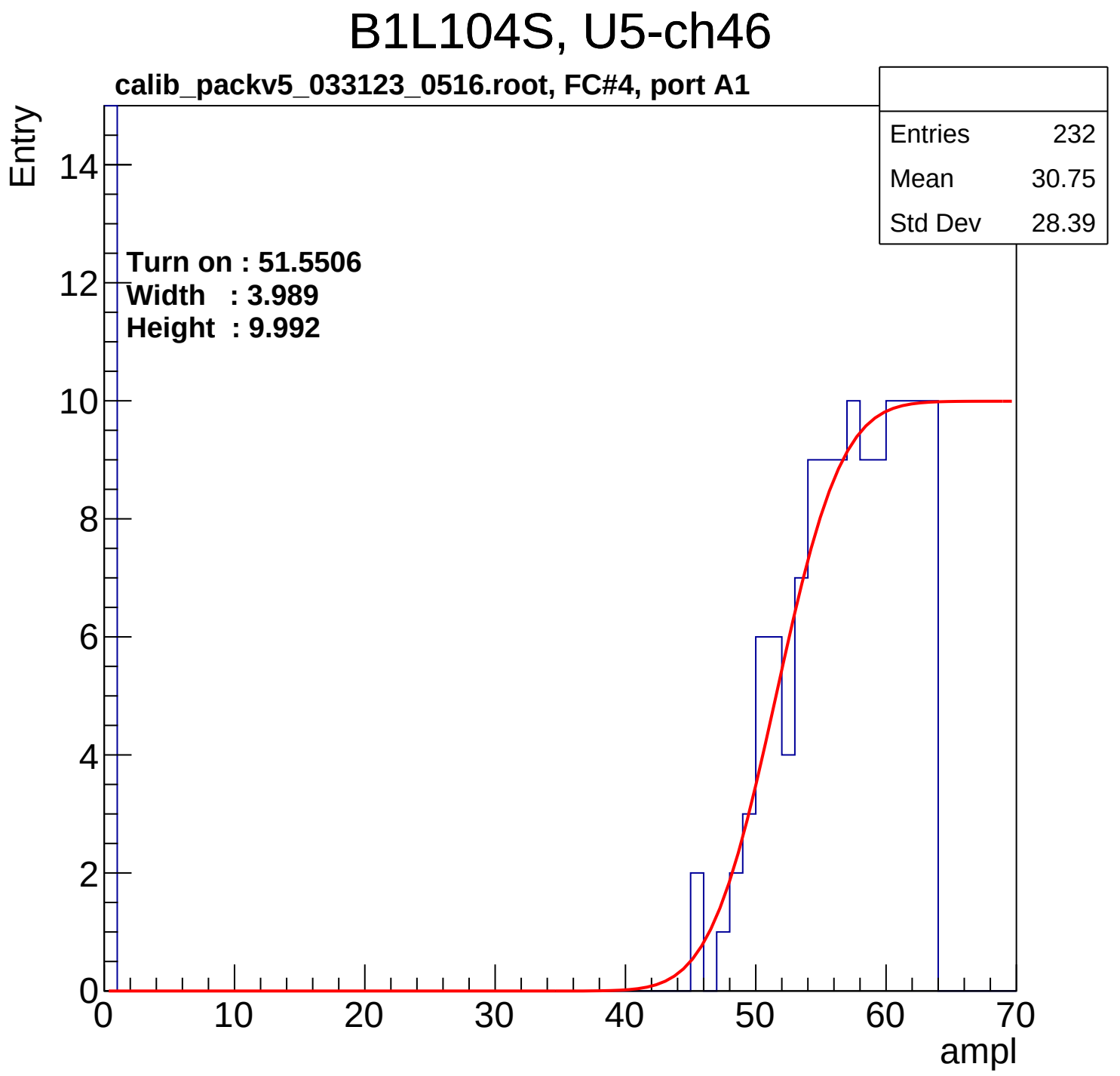

B1L104S, U5-ch41
calib_packv5_033123_0516.root, FC#4, port A1
Entries 182
Mean 31.86
Std Dev 28.97
Turn on : 53.6246
Width : 3.768
Height : 9.998
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

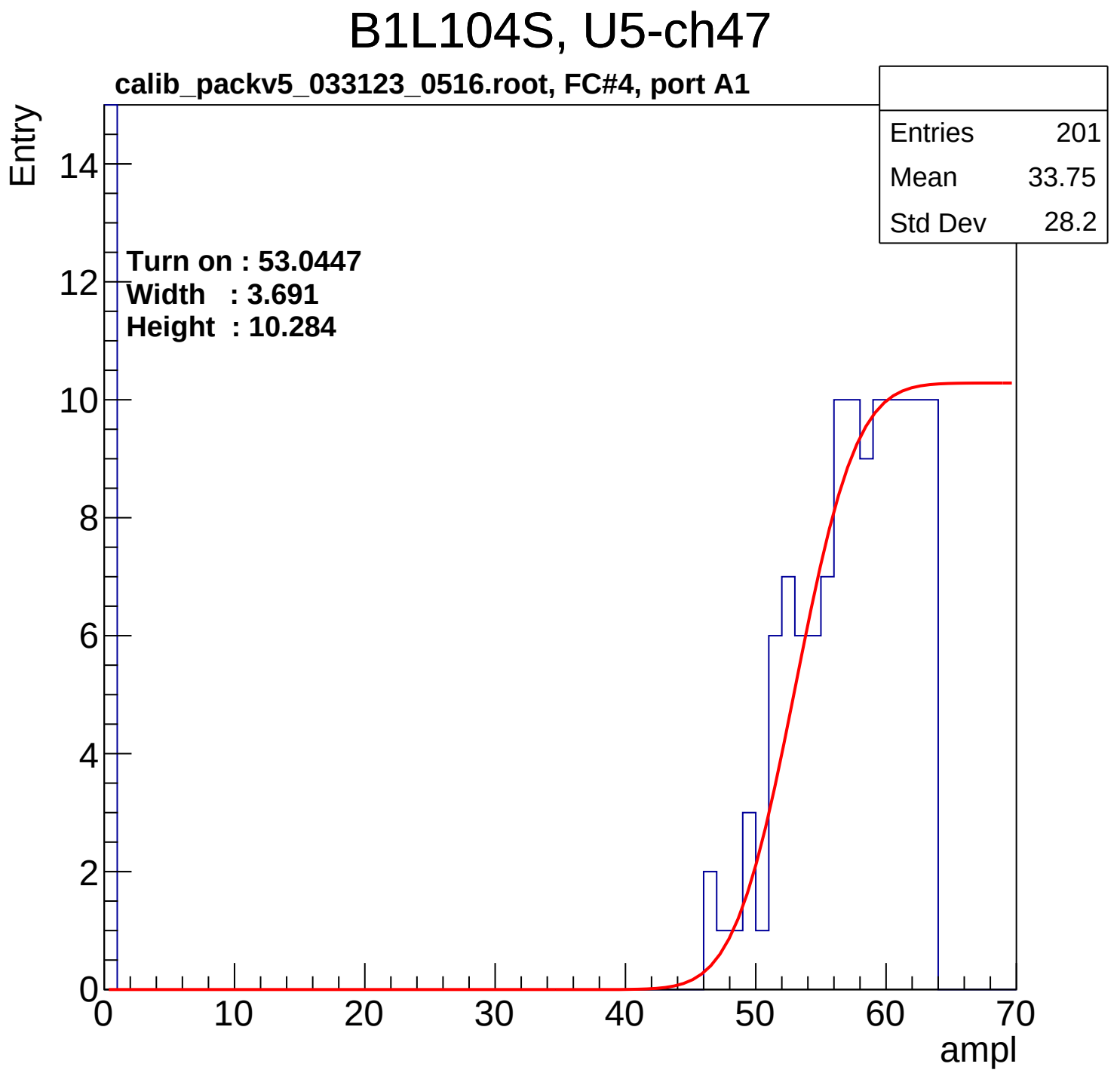

B1L104S, U5-ch42
calib_packv5_033123_0516.root, FC#4, port A1
Entries 199
Mean 26.99
Std Dev 29.2
Turn on : 55.3936
Width : 2.340
Height : 9.972
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

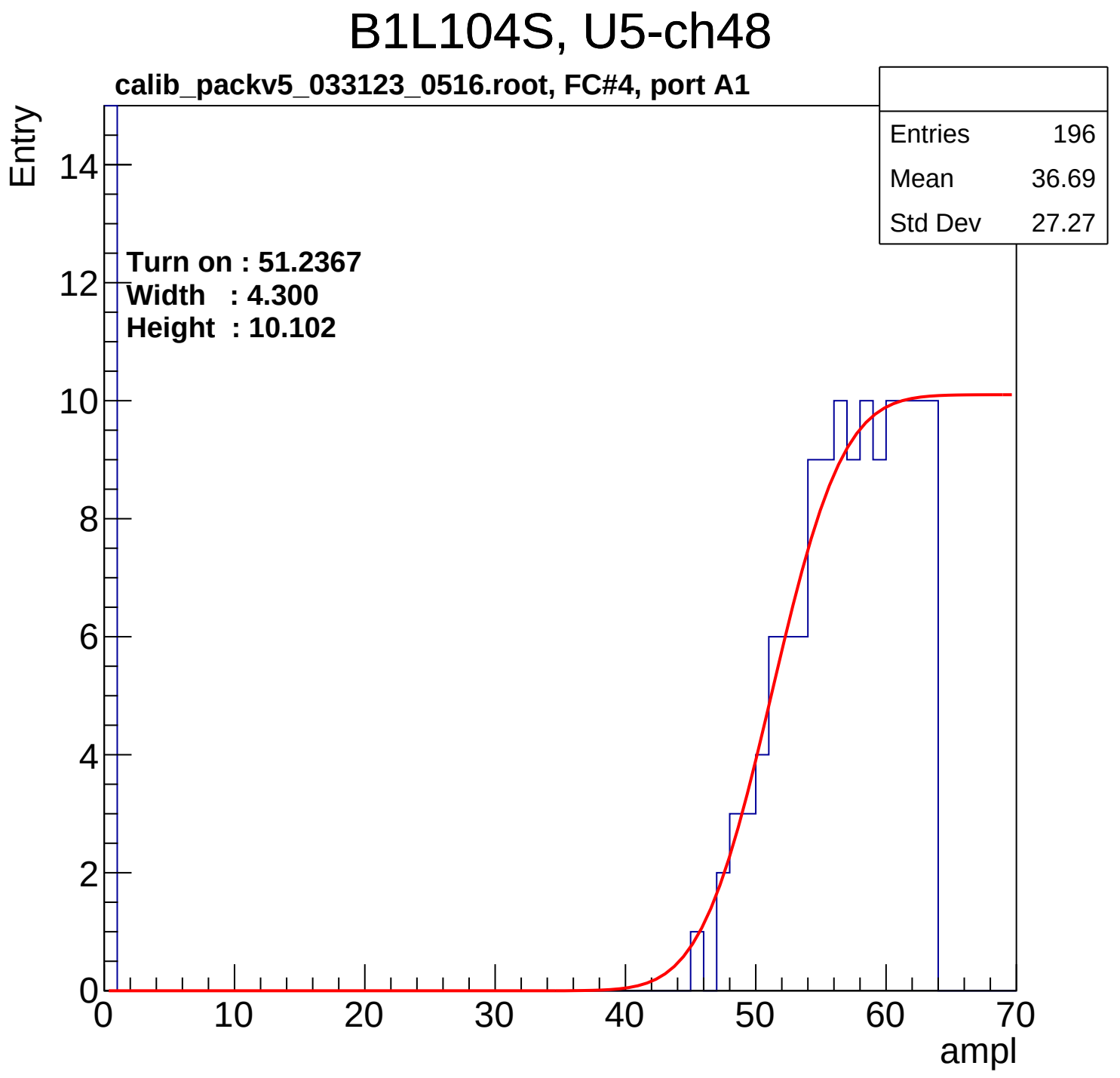

B1L104S, U5-ch43
calib_packv5_033123_0516.root, FC#4, port A1
Entries 198
Mean 36.73
Std Dev 27.36
Turn on : 51.1697
Width : 2.378
Height : 9.868
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

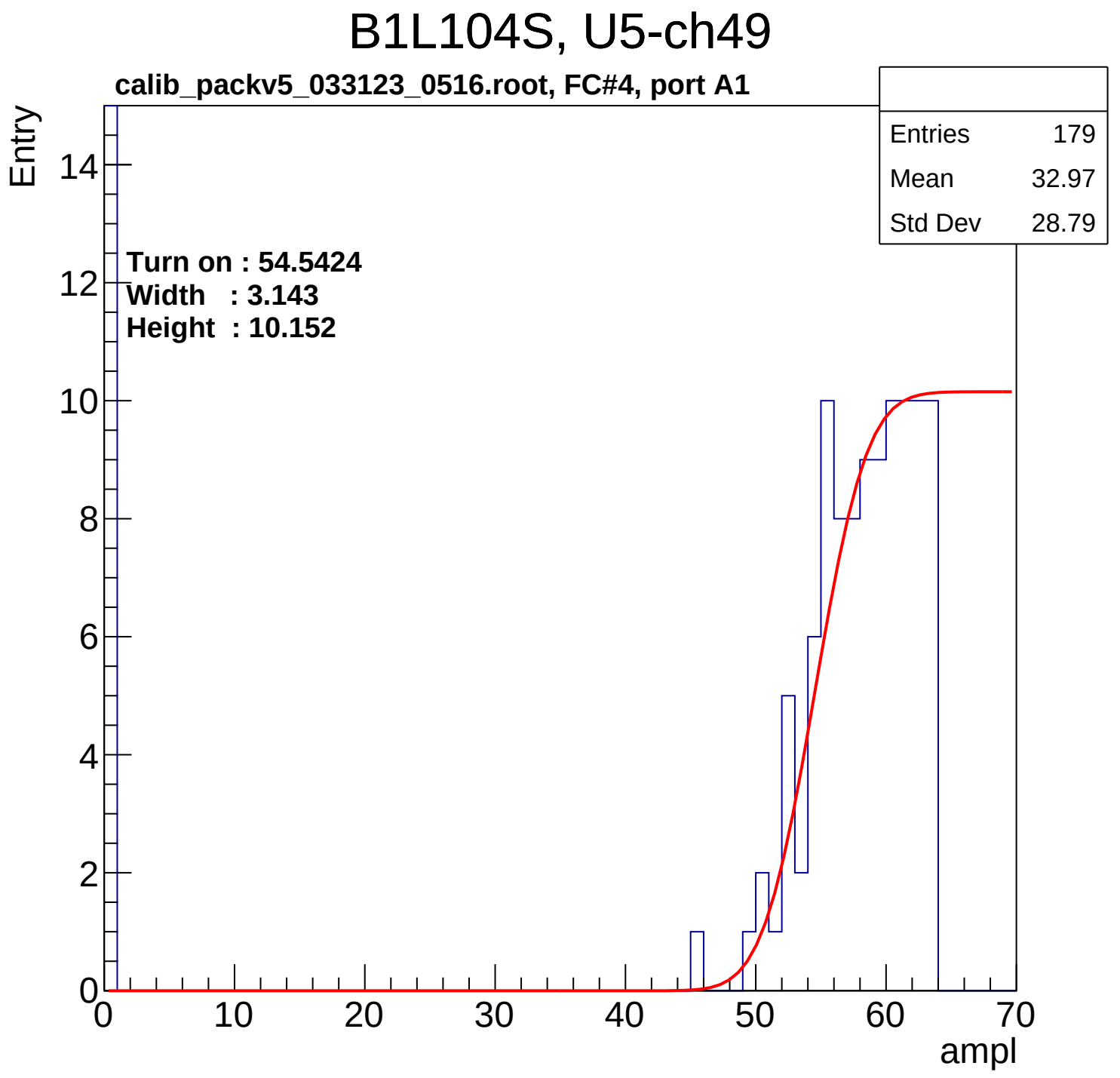

B1L104S, U5-ch44
calib_packv5_033123_0516.root, FC#4, port A1
Entries 234
Mean 31.41
Std Dev 28.28
Turn on : 51.4119
Width : 2.752
Height : 9.873
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

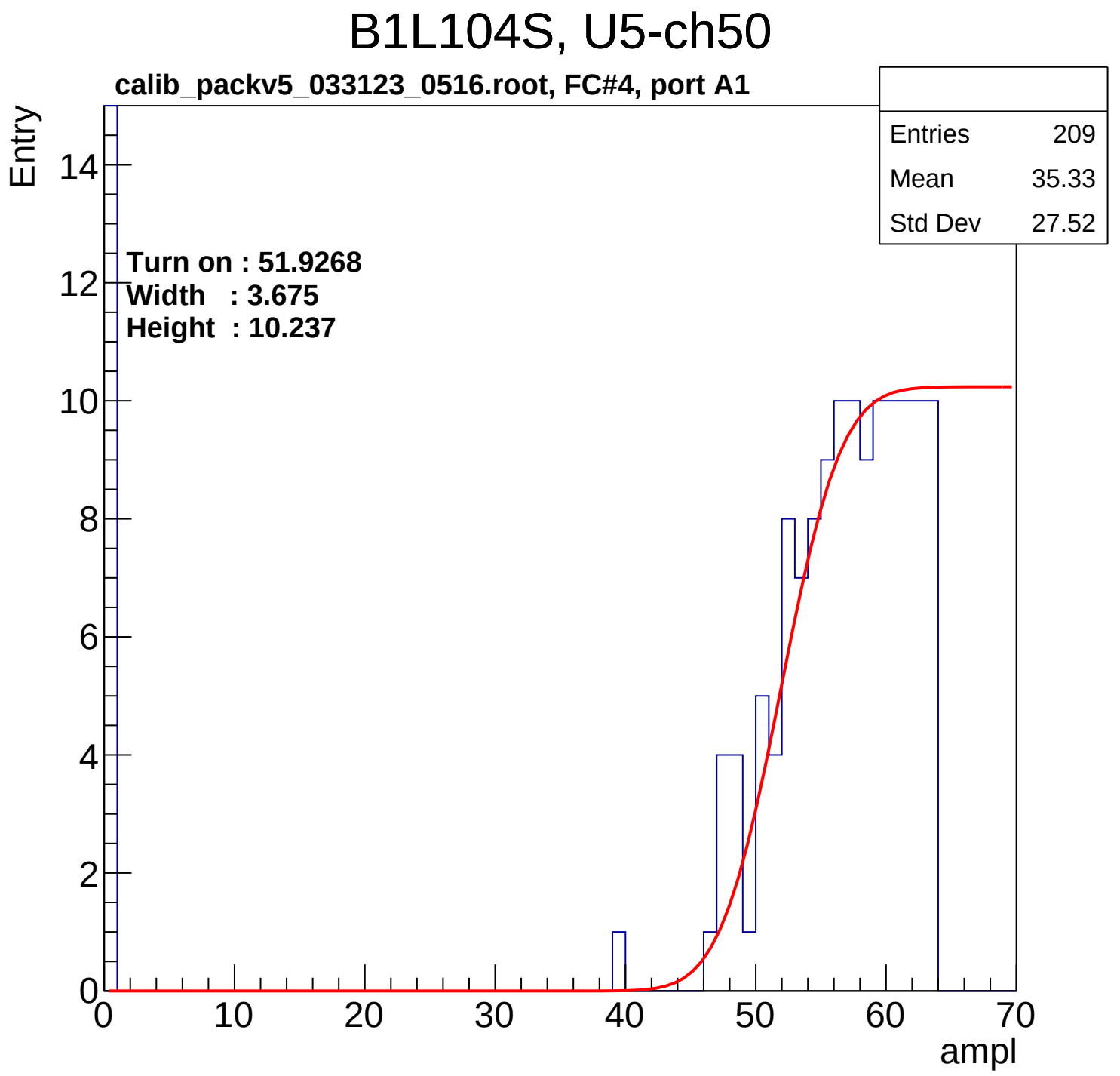

B1L104S, U5-ch45
calib_packv5_033123_0516.root, FC#4, port A1
Entries 169
Mean 33.91
Std Dev 28.66
Turn on : 54.6768
Width : 4.502
Height : 10.608
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

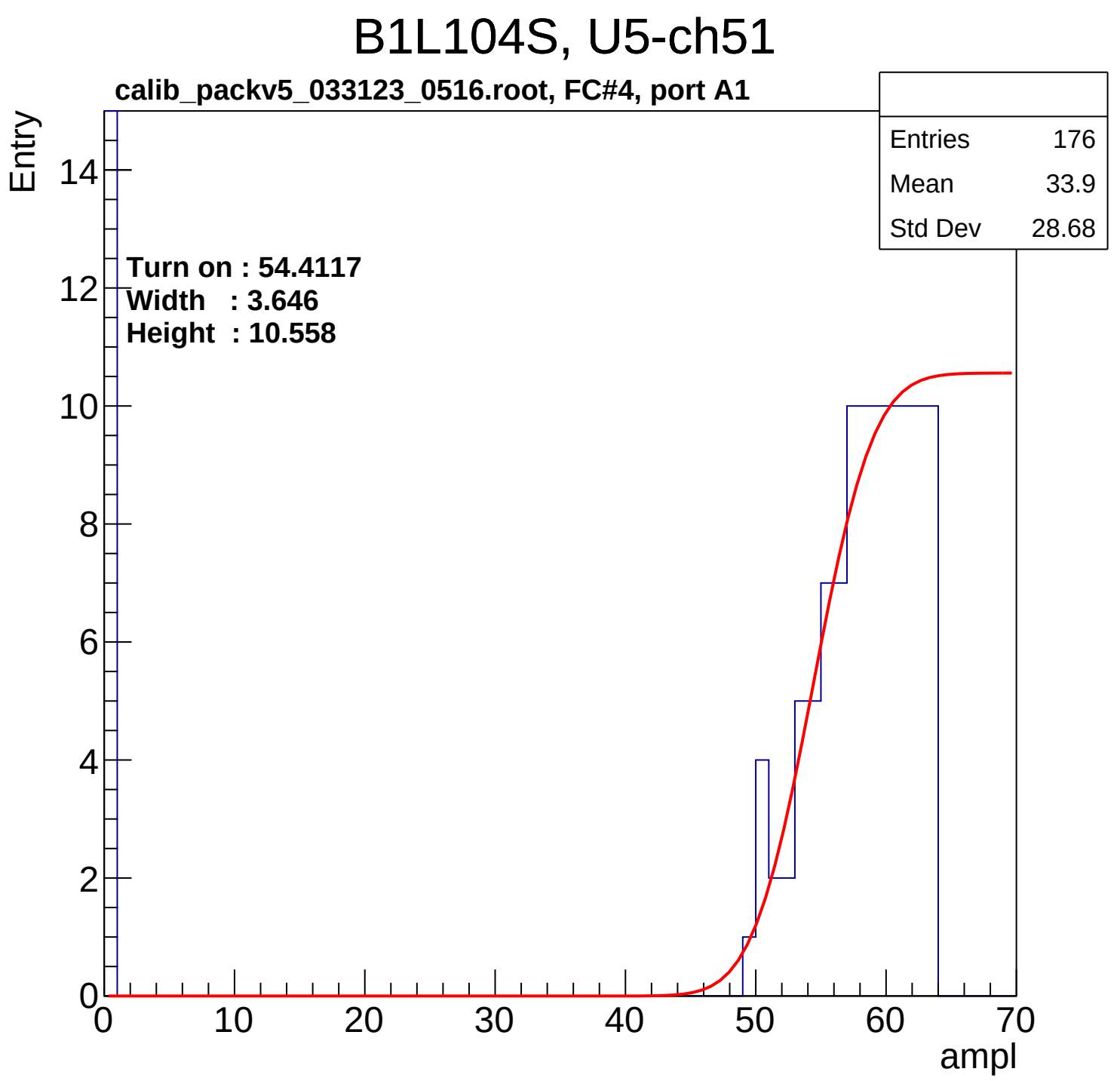

B1L104S, U5-ch46
calib_packv5_033123_0516.root, FC#4, port A1
Entries 232
Mean 30.75
Std Dev 28.39
Turn on : 51.5506
Width : 3.989
Height : 9.992
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

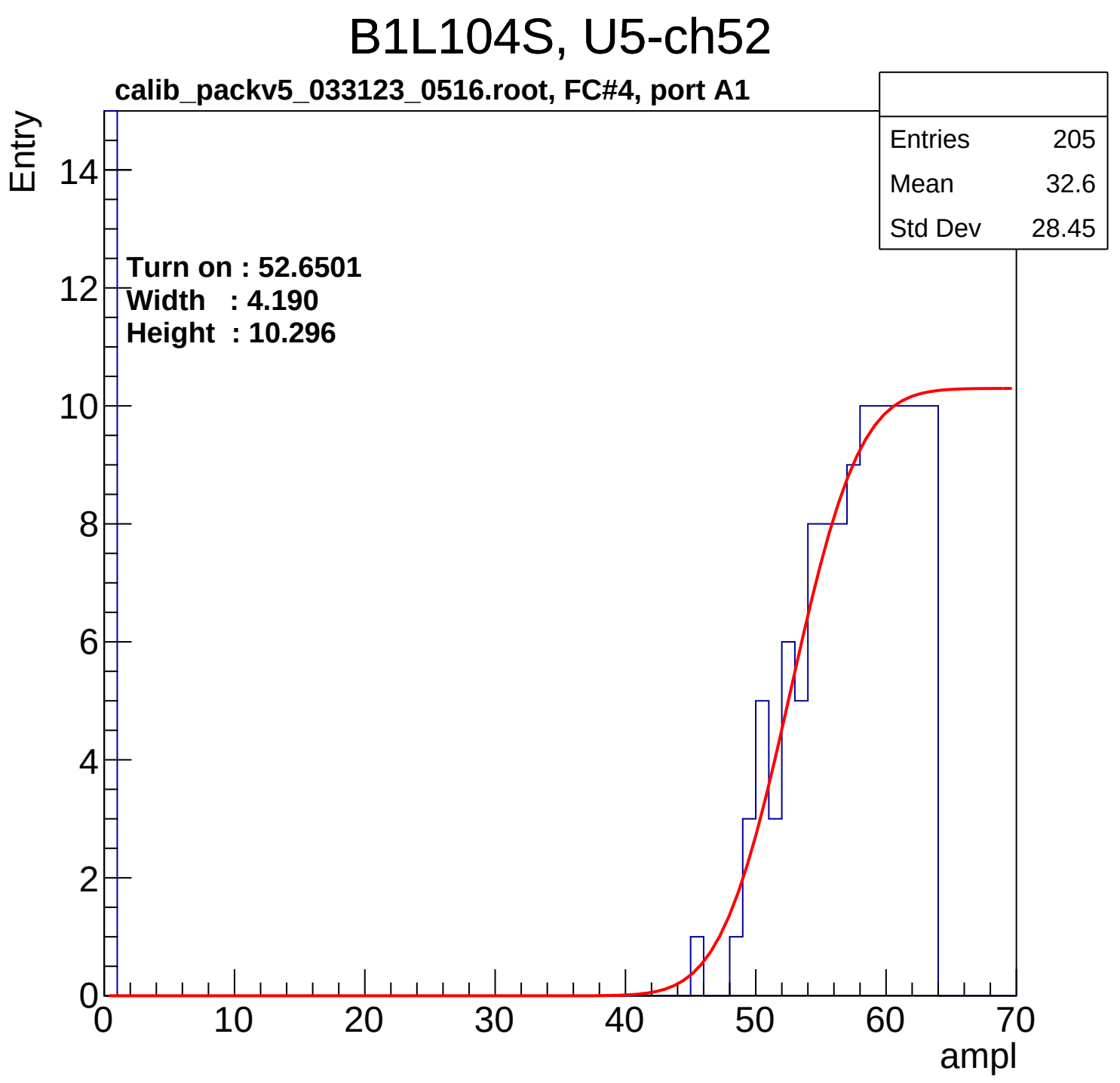

B1L104S, U5-ch47
calib_packv5_033123_0516.root, FC#4, port A1
Entries 201
Mean 33.75
Std Dev 28.2
Turn on : 53.0447
Width : 3.691
Height : 10.284
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

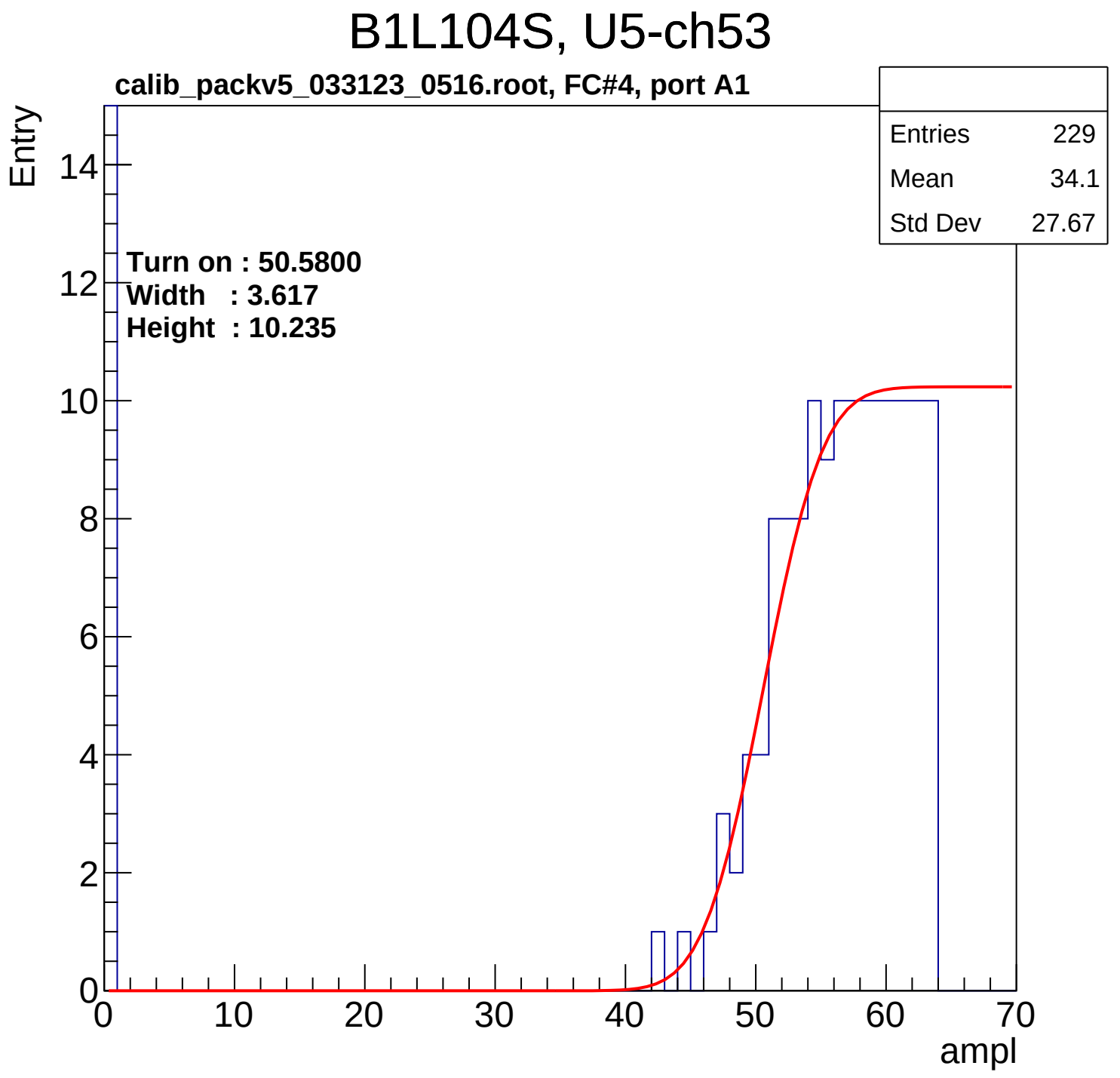

B1L104S, U5-ch48
calib_packv5_033123_0516.root, FC#4, port A1
Entries 196
Mean 36.69
Std Dev 27.27
Turn on : 51.2367
Width : 4.300
Height : 10.102
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

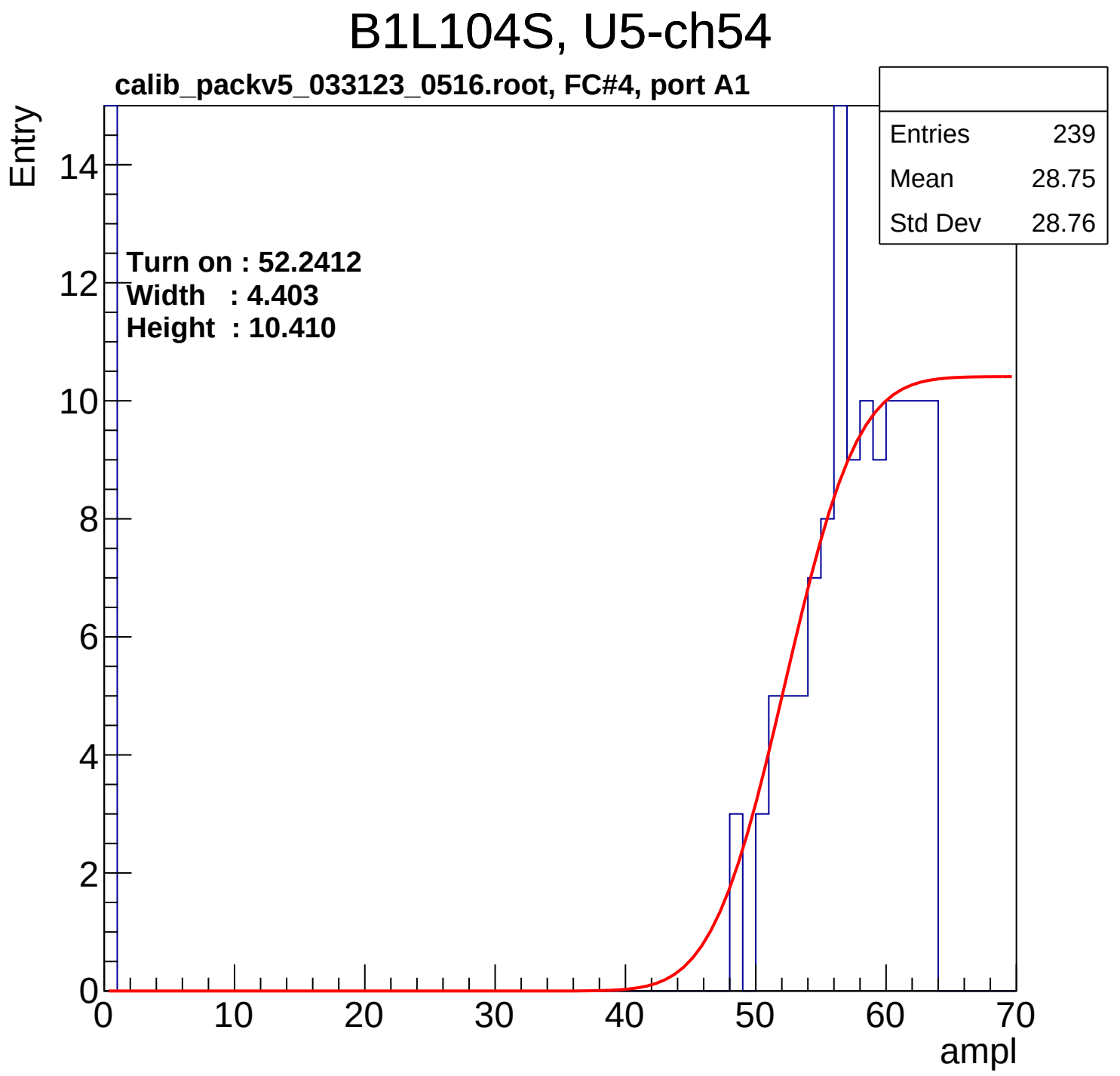

B1L104S, U5-ch49
calib_packv5_033123_0516.root, FC#4, port A1
Entries 179
Mean 32.97
Std Dev 28.79
Turn on : 54.5424
Width : 3.143
Height : 10.152
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

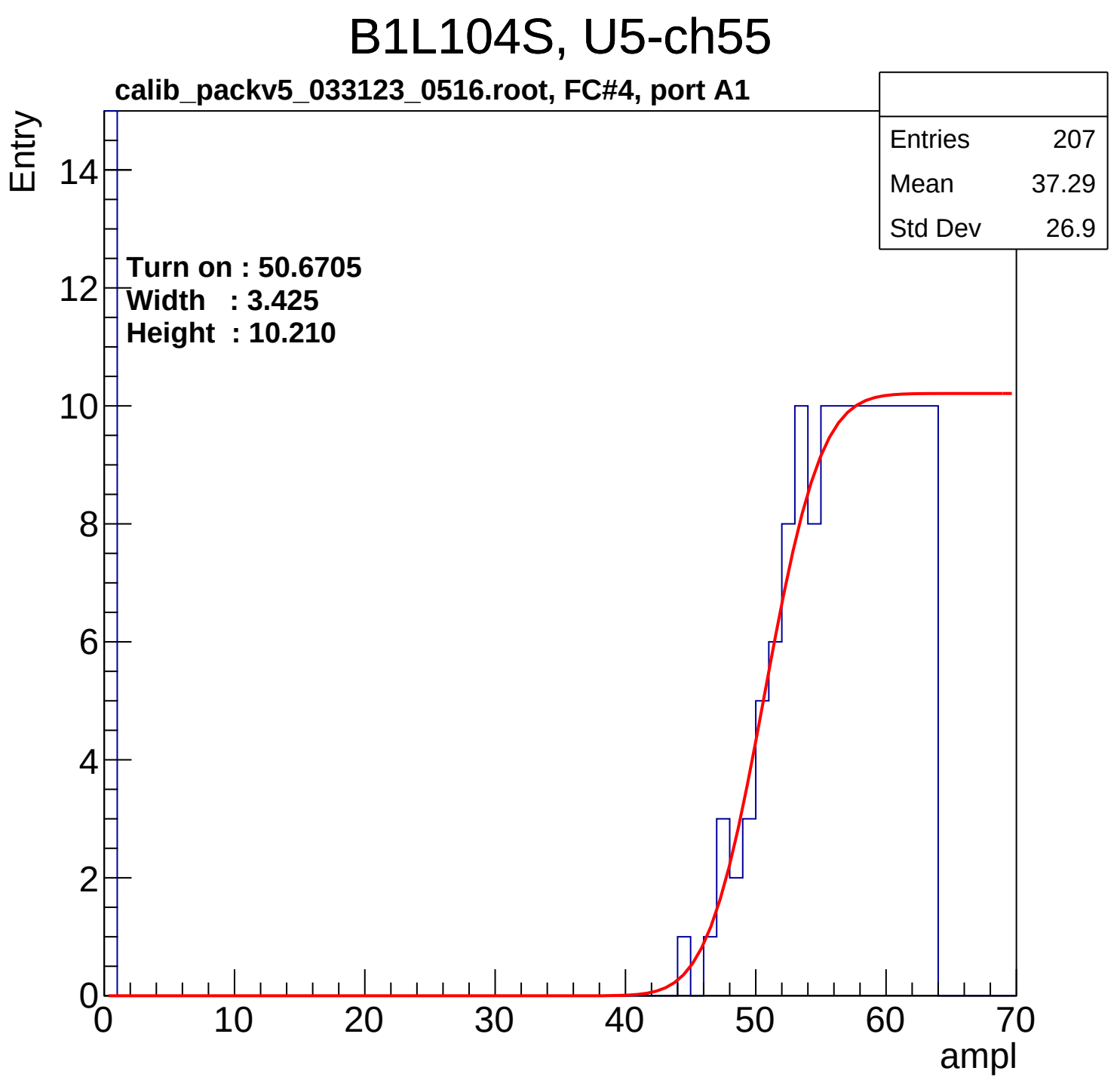

B1L104S, U5-ch50
calib_packv5_033123_0516.root, FC#4, port A1
Entries 209
Mean 35.33
Std Dev 27.52
Turn on : 51.9268
Width : 3.675
Height : 10.237
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

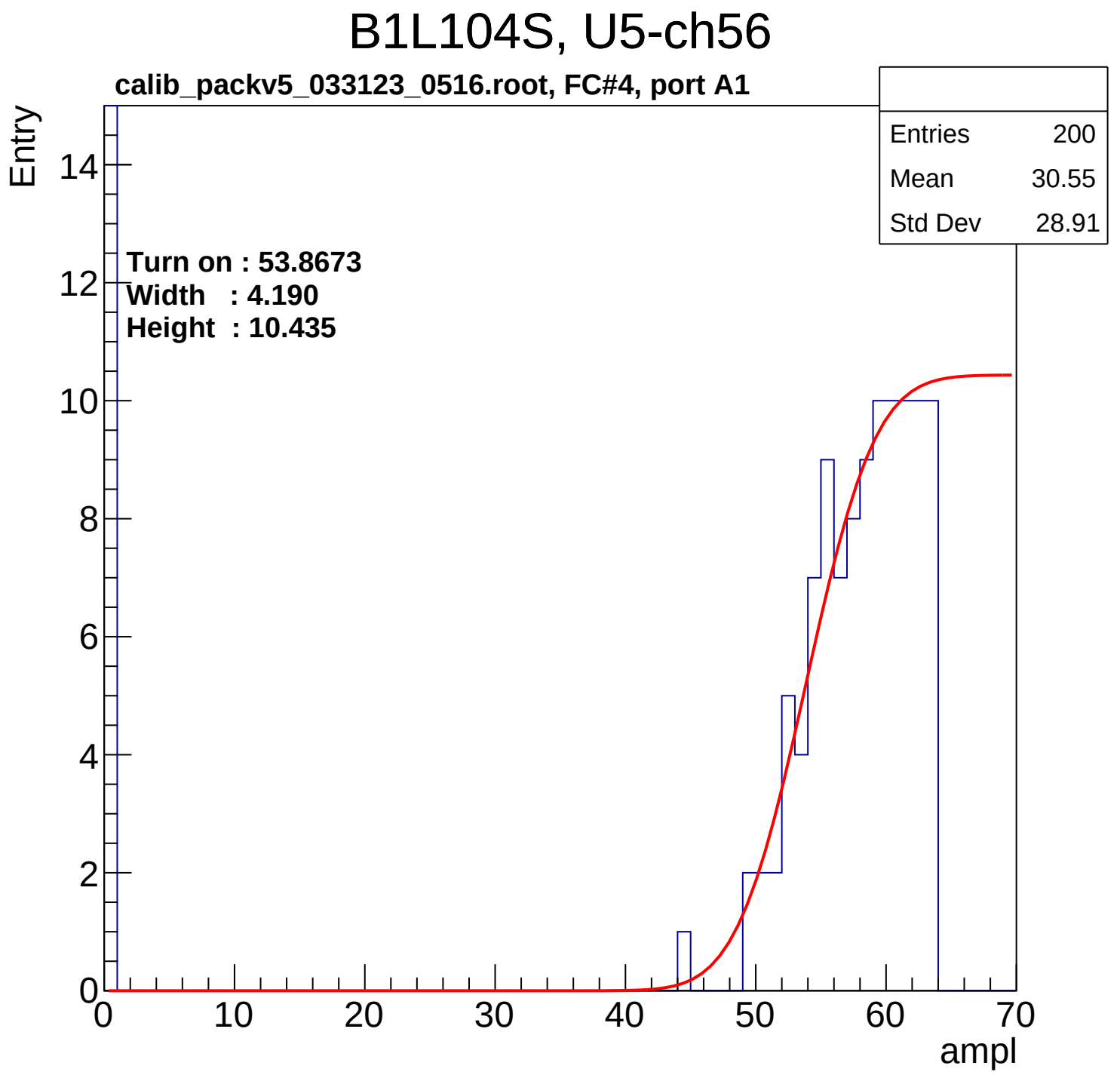

B1L104S, U5-ch51
calib_packv5_033123_0516.root, FC#4, port A1
Entries 176
Mean 33.9
Std Dev 28.68
Turn on : 54.4117
Width : 3.646
Height : 10.558
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

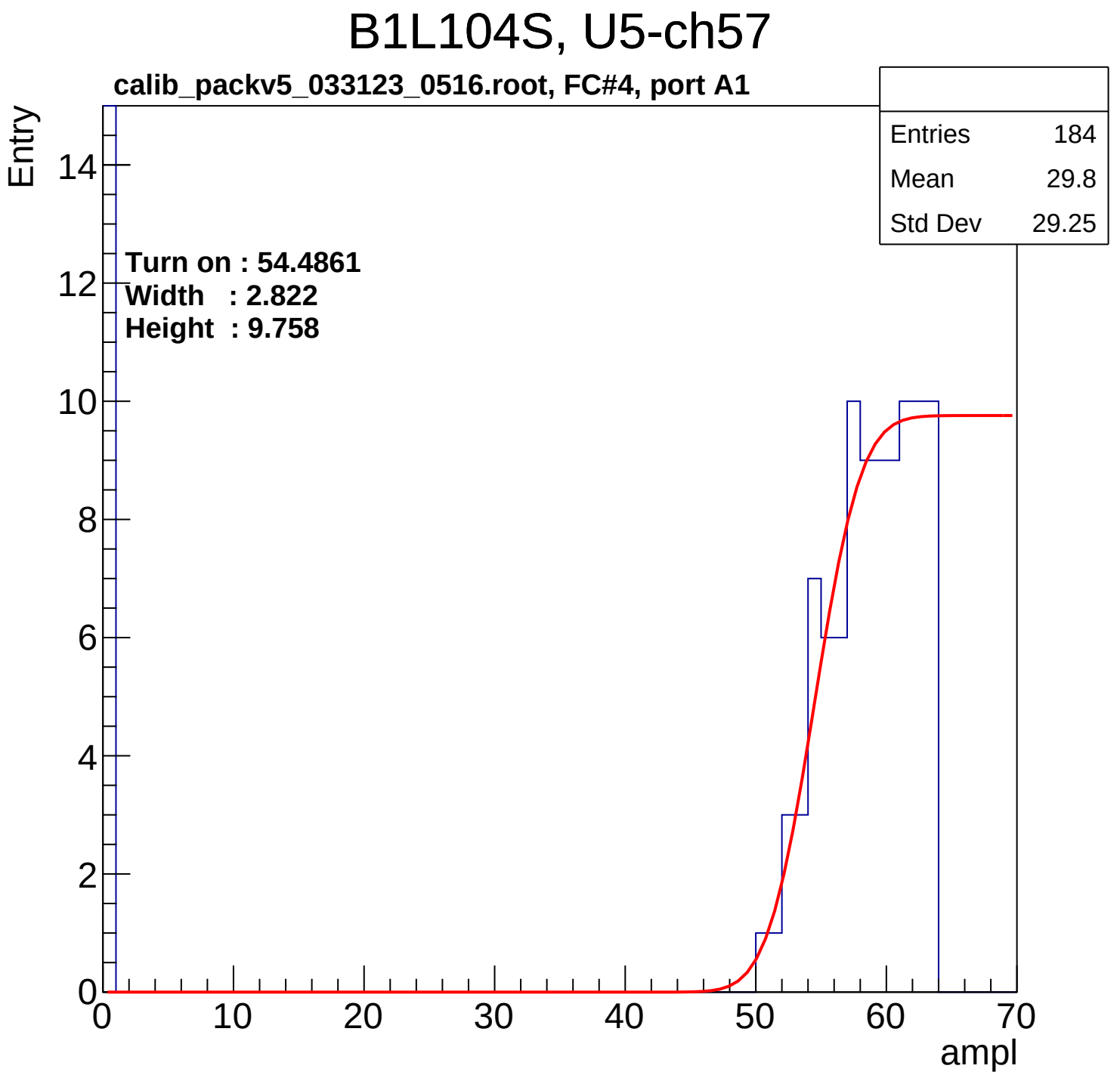

B1L104S, U5-ch52
calib_packv5_033123_0516.root, FC#4, port A1
Entries 205
Mean 32.6
Std Dev 28.45
Turn on : 52.6501
Width : 4.190
Height : 10.296
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

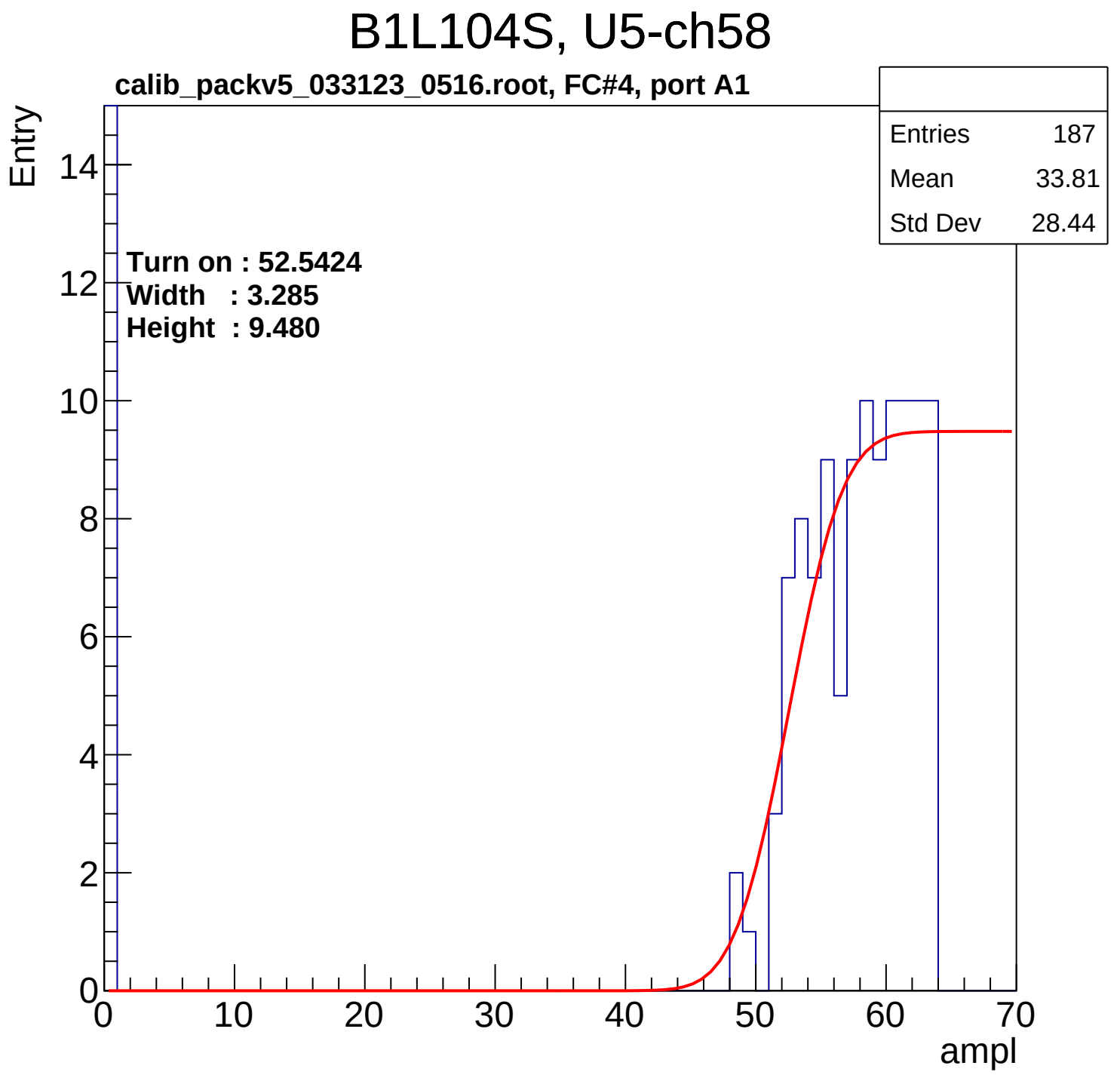

B1L104S, U5-ch53
calib_packv5_033123_0516.root, FC#4, port A1
Entries 229
Mean 34.1
Std Dev 27.67
Turn on : 50.5800
Width : 3.617
Height : 10.235
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

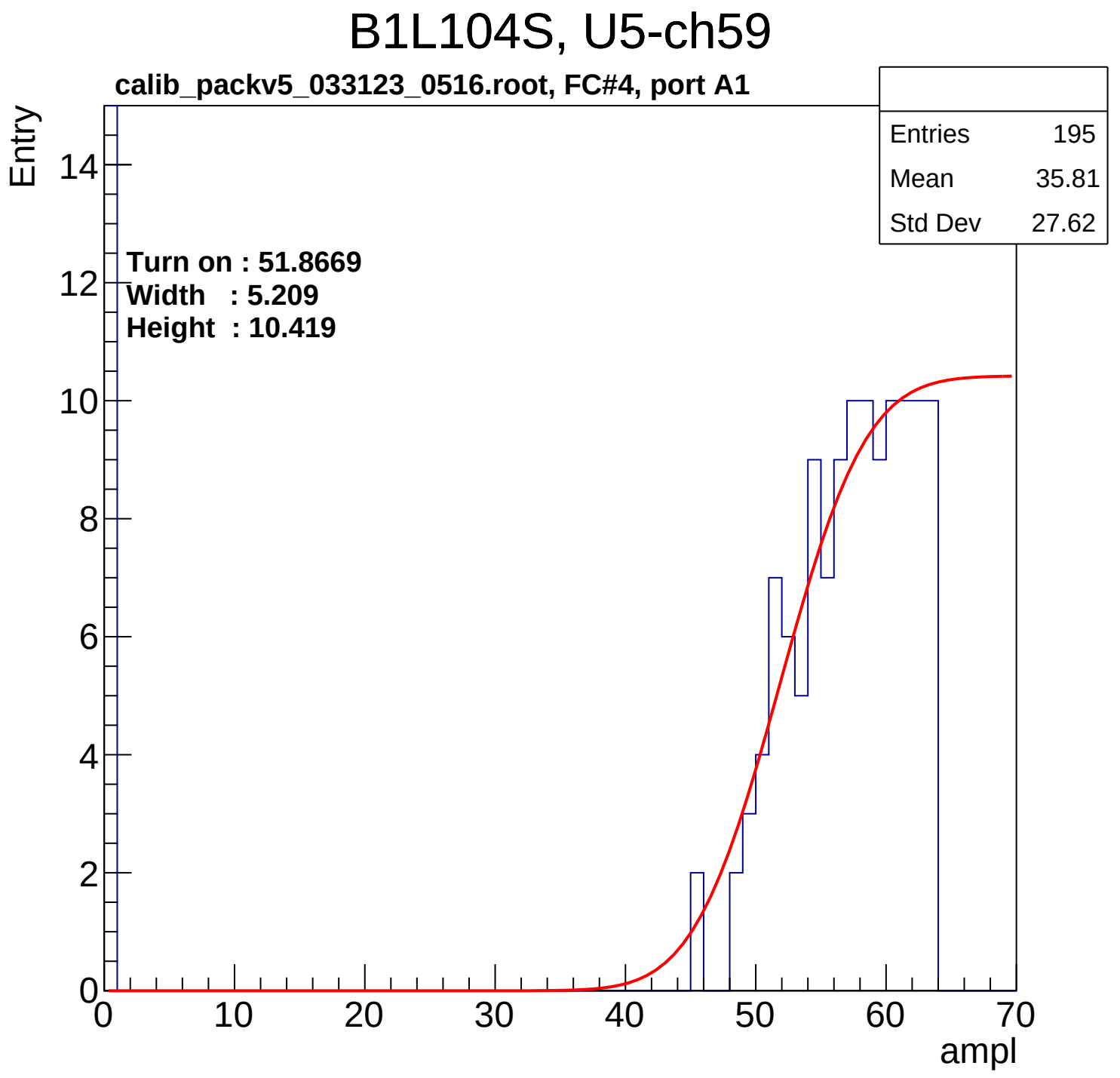

B1L104S, U5-ch54
calib_packv5_033123_0516.root, FC#4, port A1
Entries 239
Mean 28.75
Std Dev 28.76
Turn on : 52.2412
Width : 4.403
Height : 10.410
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

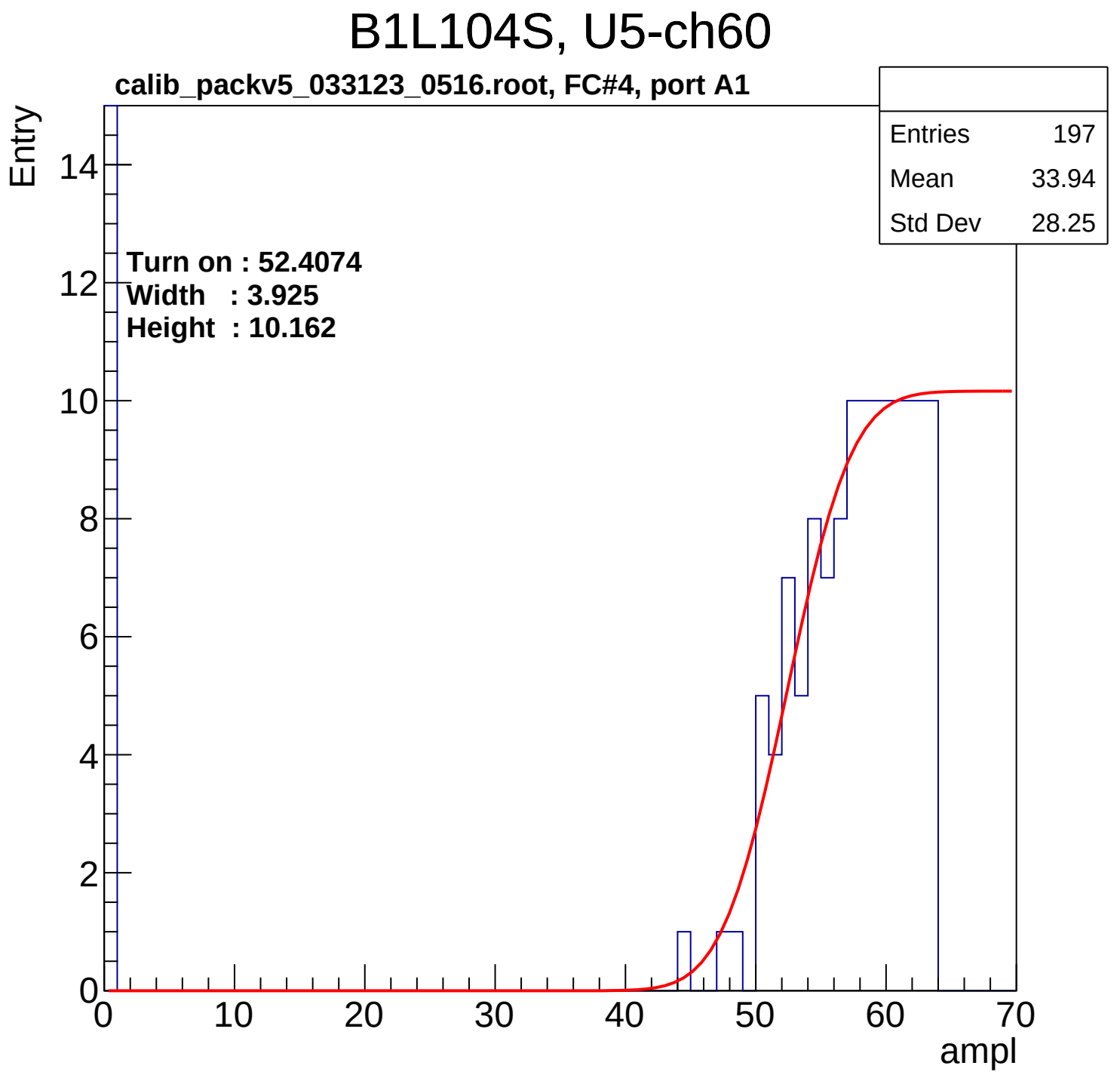

B1L104S, U5-ch55
calib_packv5_033123_0516.root, FC#4, port A1
Entries 207
Mean 37.29
Std Dev 26.9
Turn on : 50.6705
Width : 3.425
Height : 10.210
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

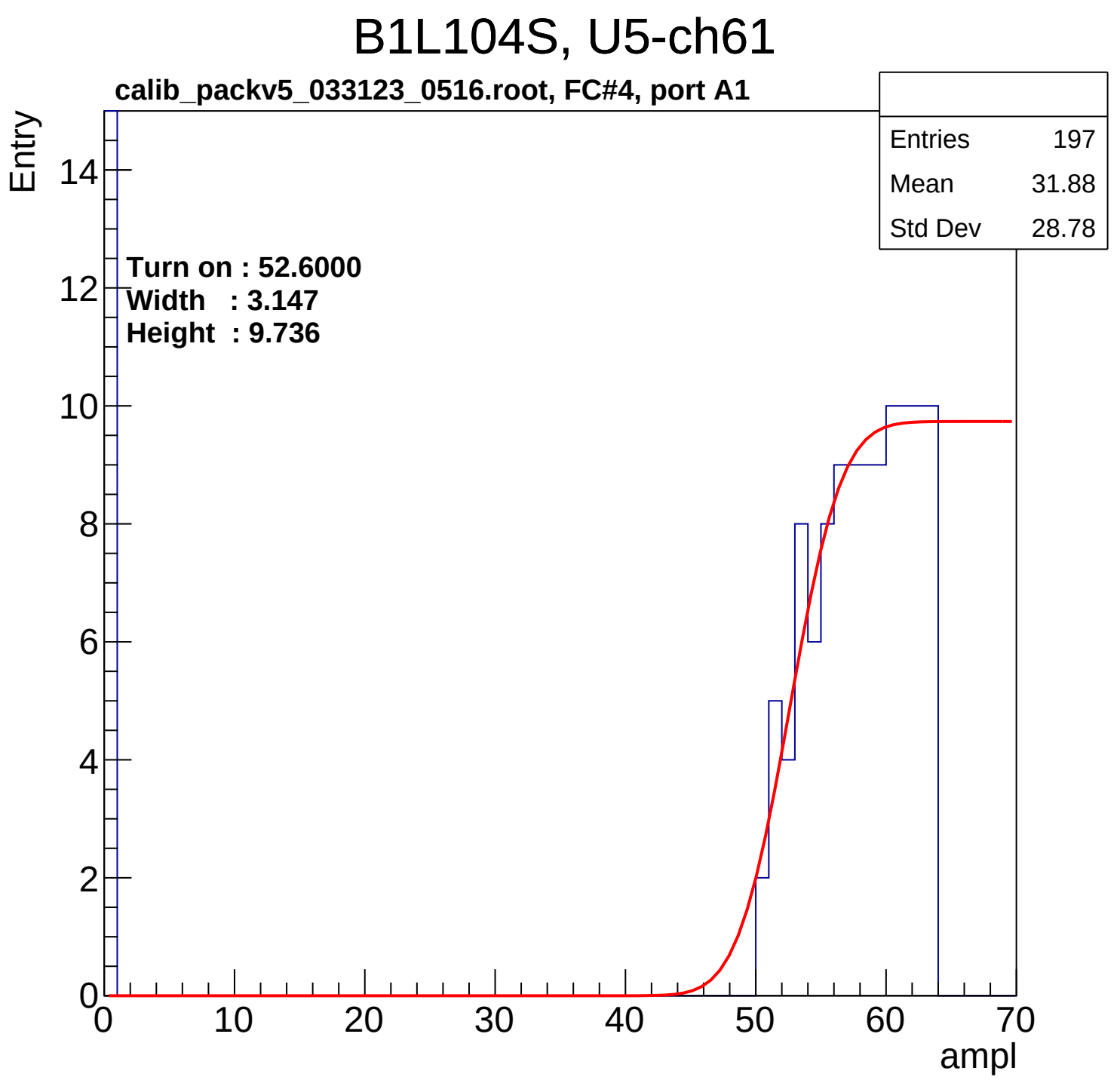

B1L104S, U5-ch56
calib_packv5_033123_0516.root, FC#4, port A1
Entries 200
Mean 30.55
Std Dev 28.91
Turn on : 53.8673
Width : 4.190
Height : 10.435
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

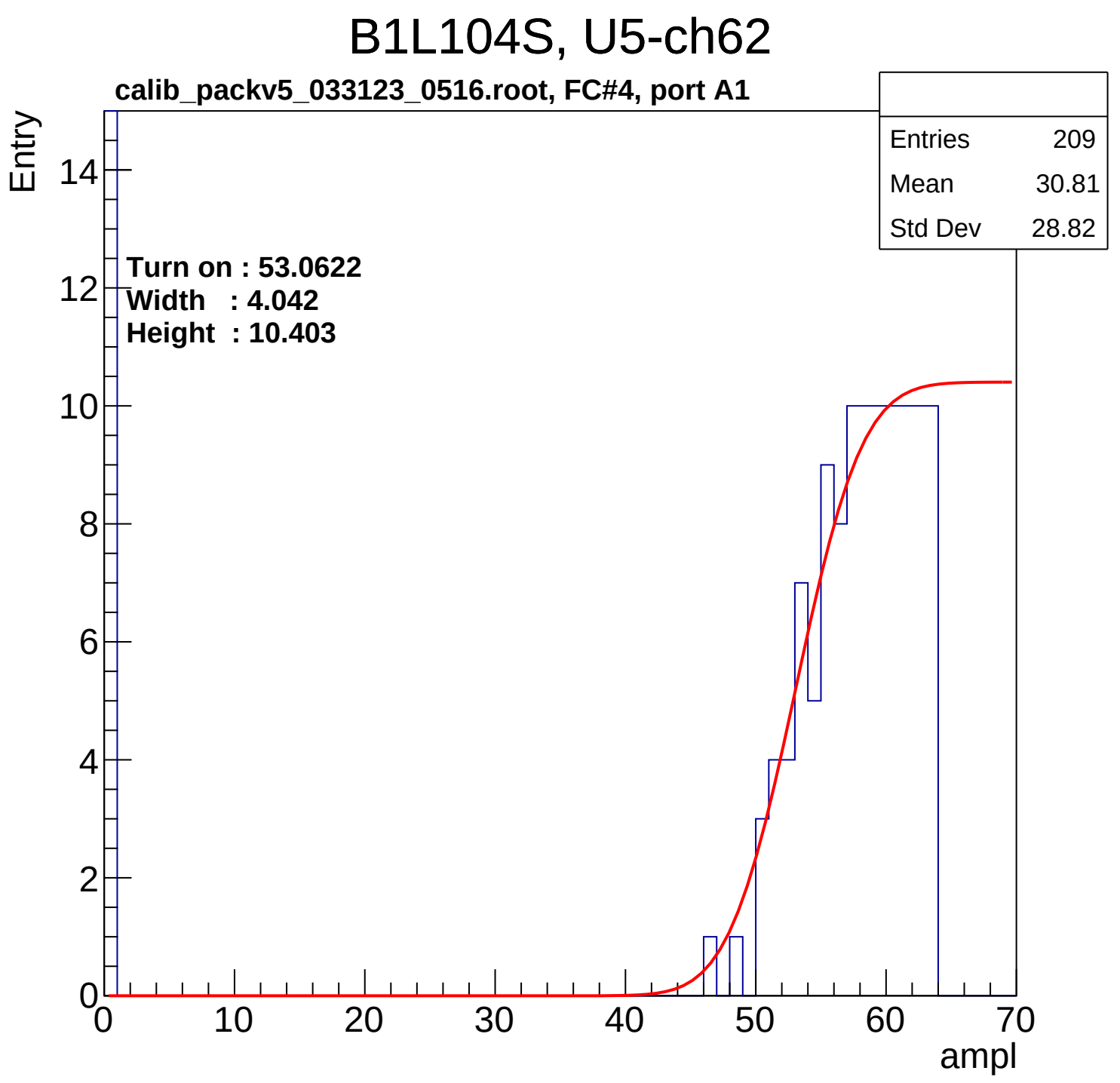

B1L104S, U5-ch57
calib_packv5_033123_0516.root, FC#4, port A1
Entries 184
Mean 29.8
Std Dev 29.25
Turn on : 54.4861
Width : 2.822
Height : 9.758
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

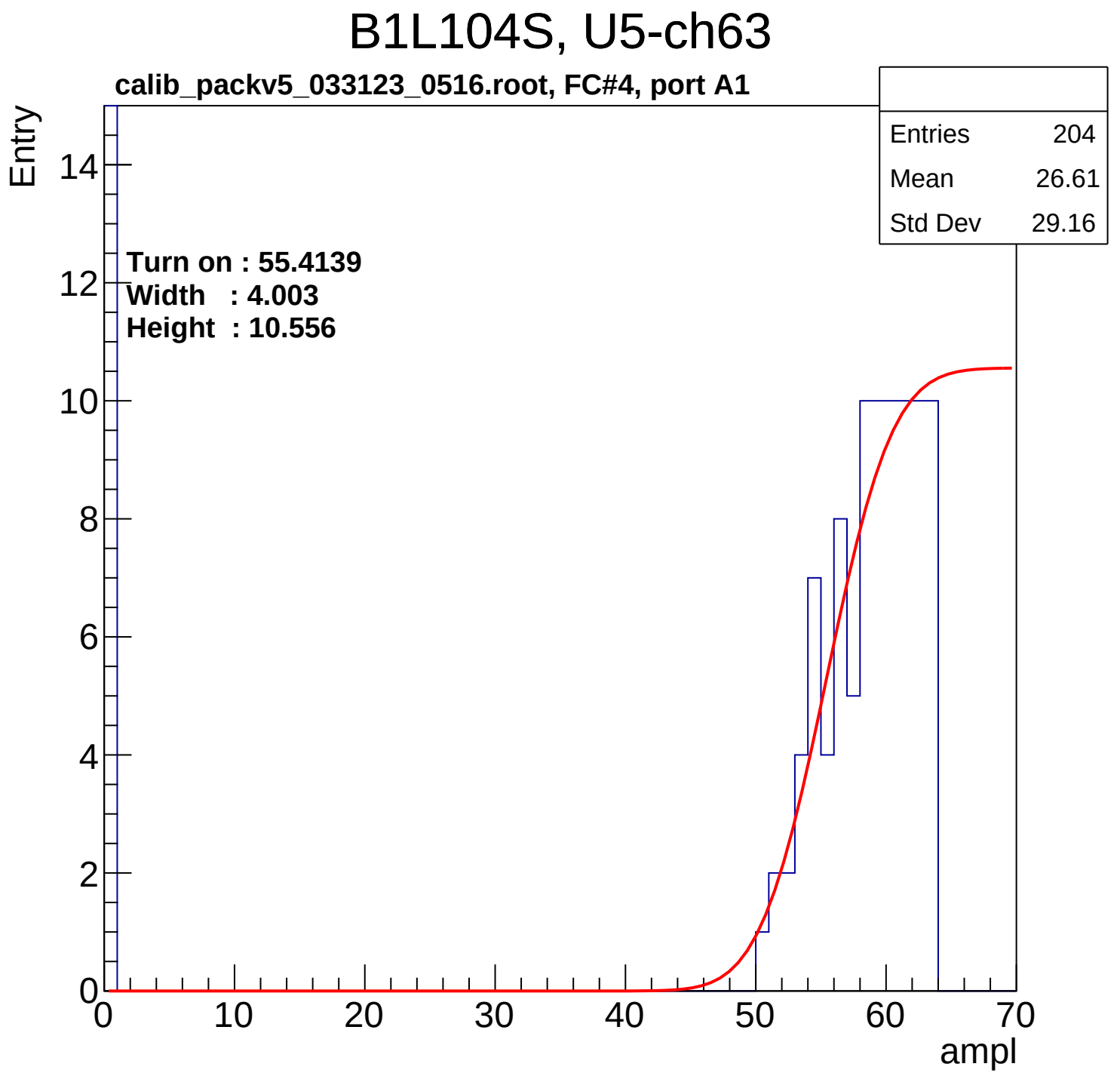

B1L104S, U5-ch58
calib_packv5_033123_0516.root, FC#4, port A1
Entries 187
Mean 33.81
Std Dev 28.44
Turn on : 52.5424
Width : 3.285
Height : 9.480
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

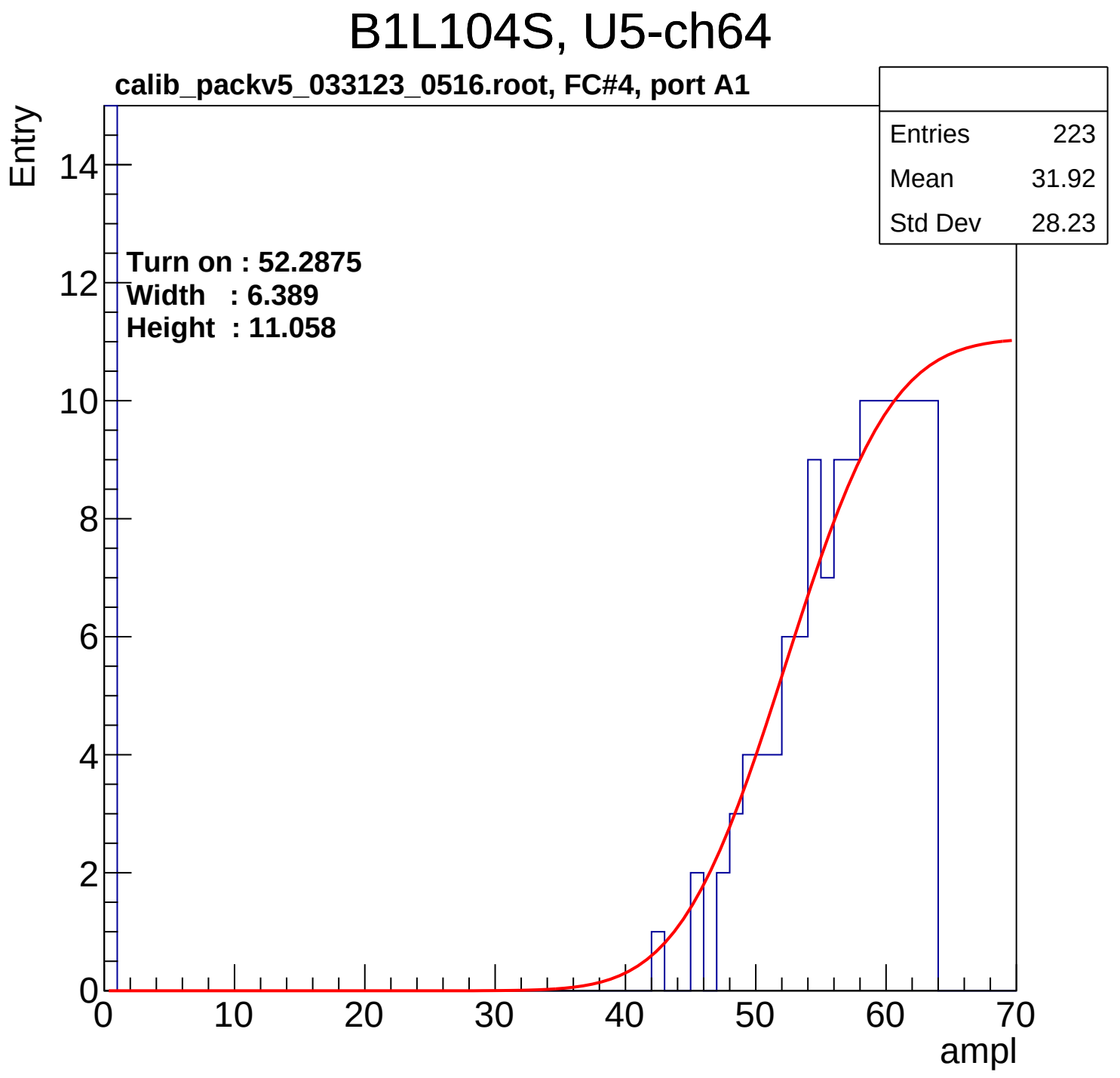

B1L104S, U5-ch59
calib_packv5_033123_0516.root, FC#4, port A1
Entries 195
Mean 35.81
Std Dev 27.62
Turn on : 51.8669
Width : 5.209
Height : 10.419
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

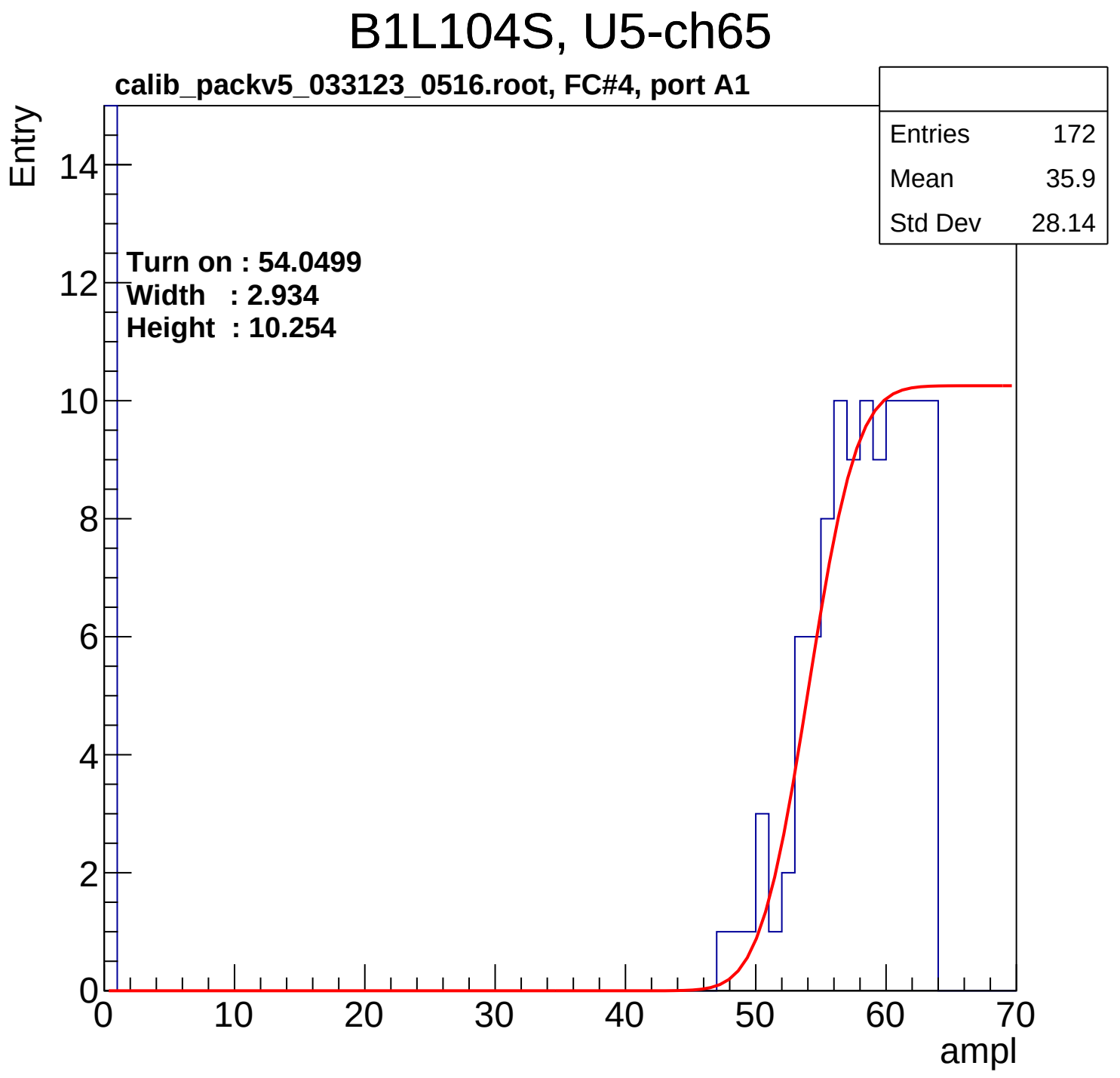

B1L104S, U5-ch60
calib_packv5_033123_0516.root, FC#4, port A1
Entries 197
Mean 33.94
Std Dev 28.25
Turn on : 52.4074
Width : 3.925
Height : 10.162
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

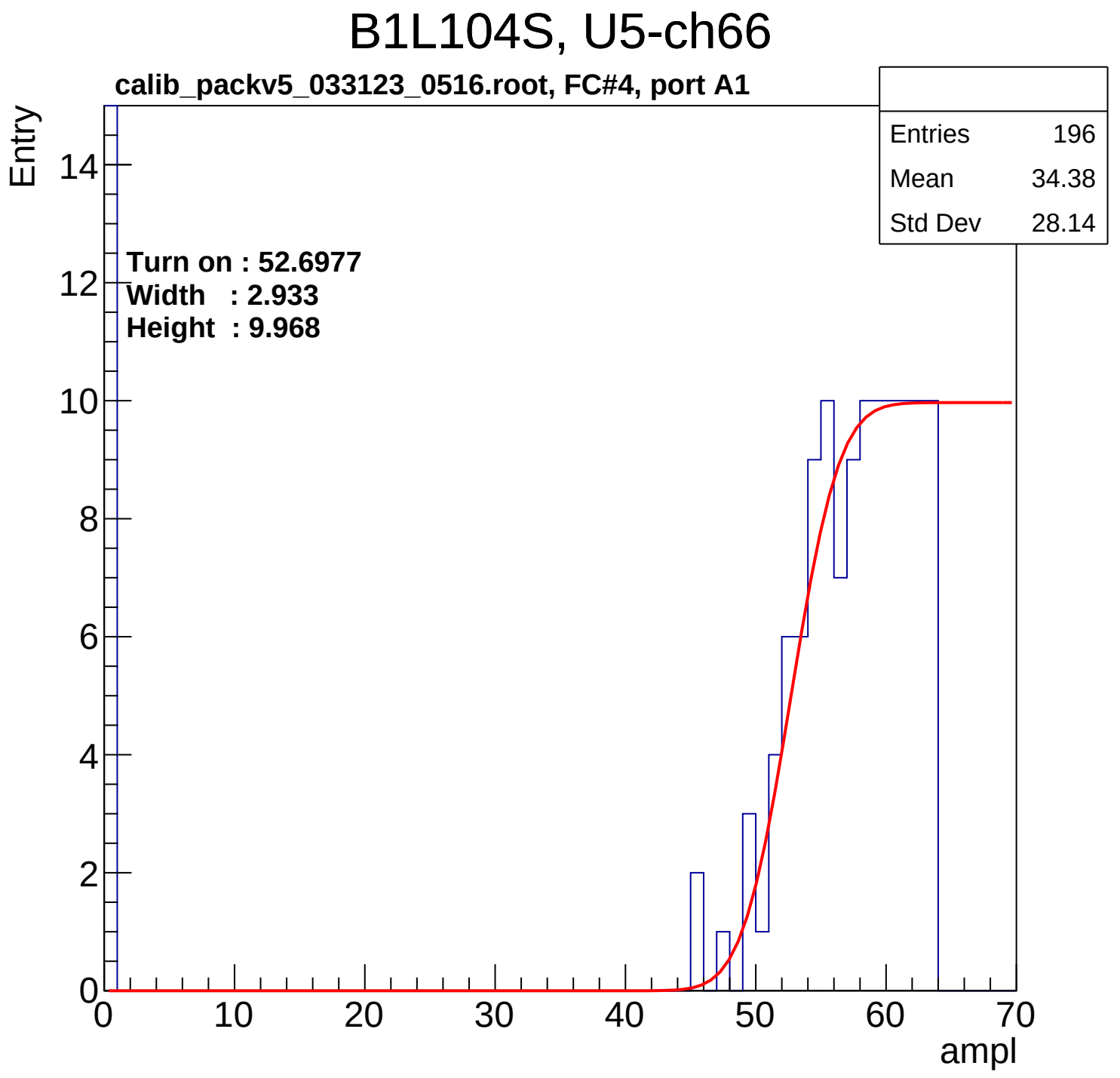

B1L104S, U5-ch61
calib_packv5_033123_0516.root, FC#4, port A1
Entries 197
Mean 31.88
Std Dev 28.78
Turn on : 52.6000
Width : 3.147
Height : 9.736
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

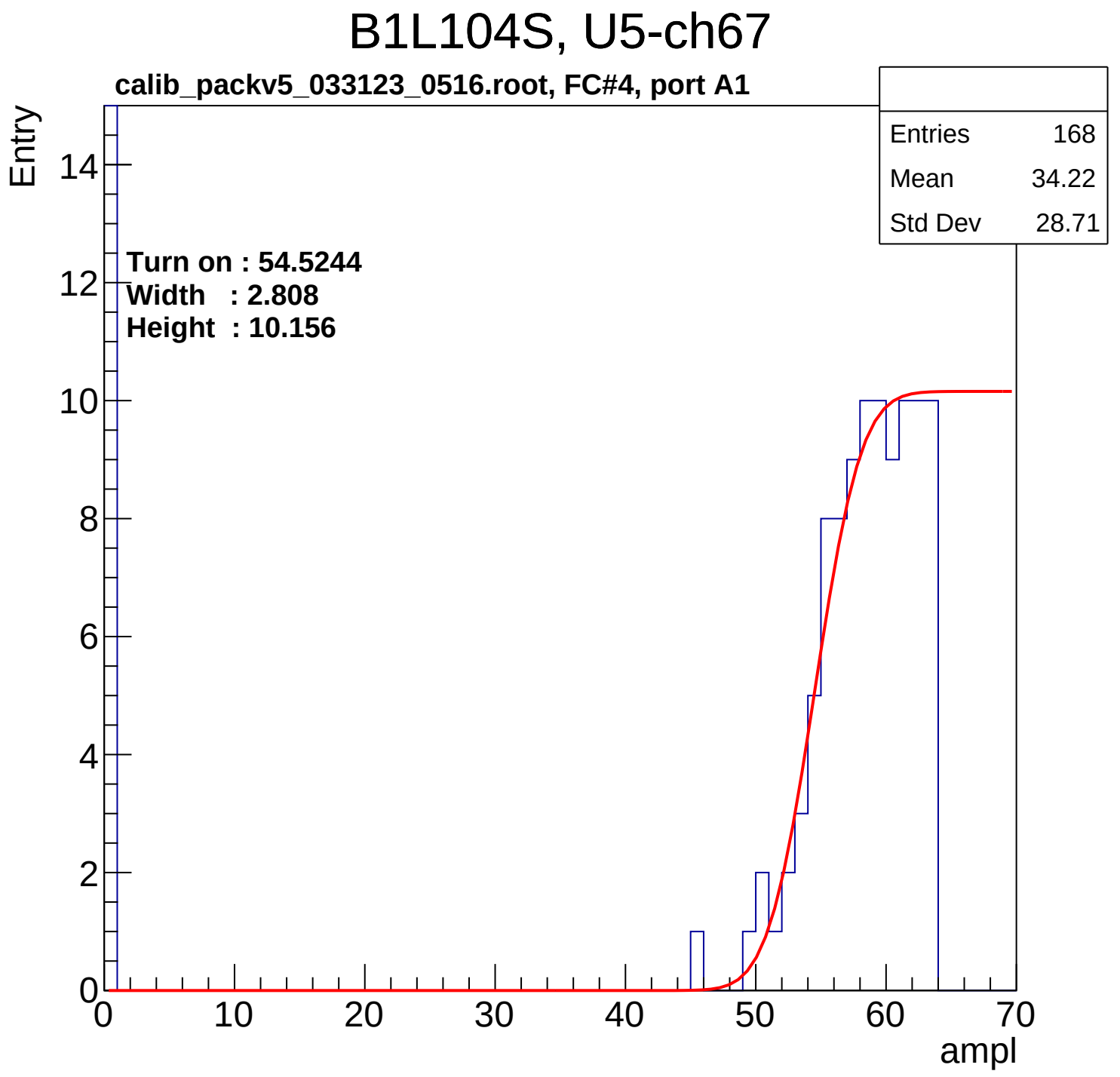

B1L104S, U5-ch62
calib_packv5_033123_0516.root, FC#4, port A1
Entries 209
Mean 30.81
Std Dev 28.82
Turn on : 53.0622
Width : 4.042
Height : 10.403
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

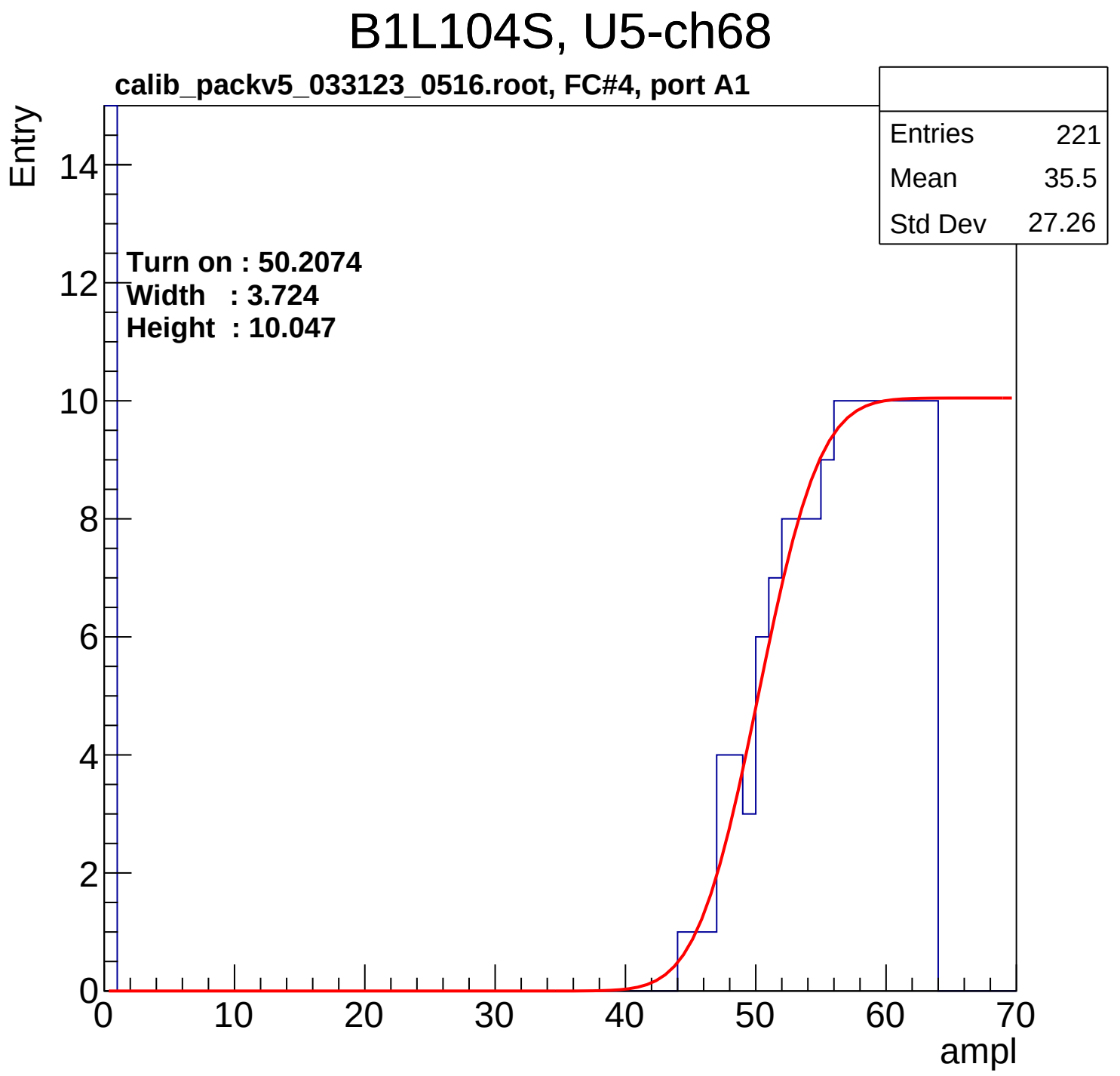

B1L104S, U5-ch63
calib_packv5_033123_0516.root, FC#4, port A1
Entries 204
Mean 26.61
Std Dev 29.16
Turn on : 55.4139
Width : 4.003
Height : 10.556
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

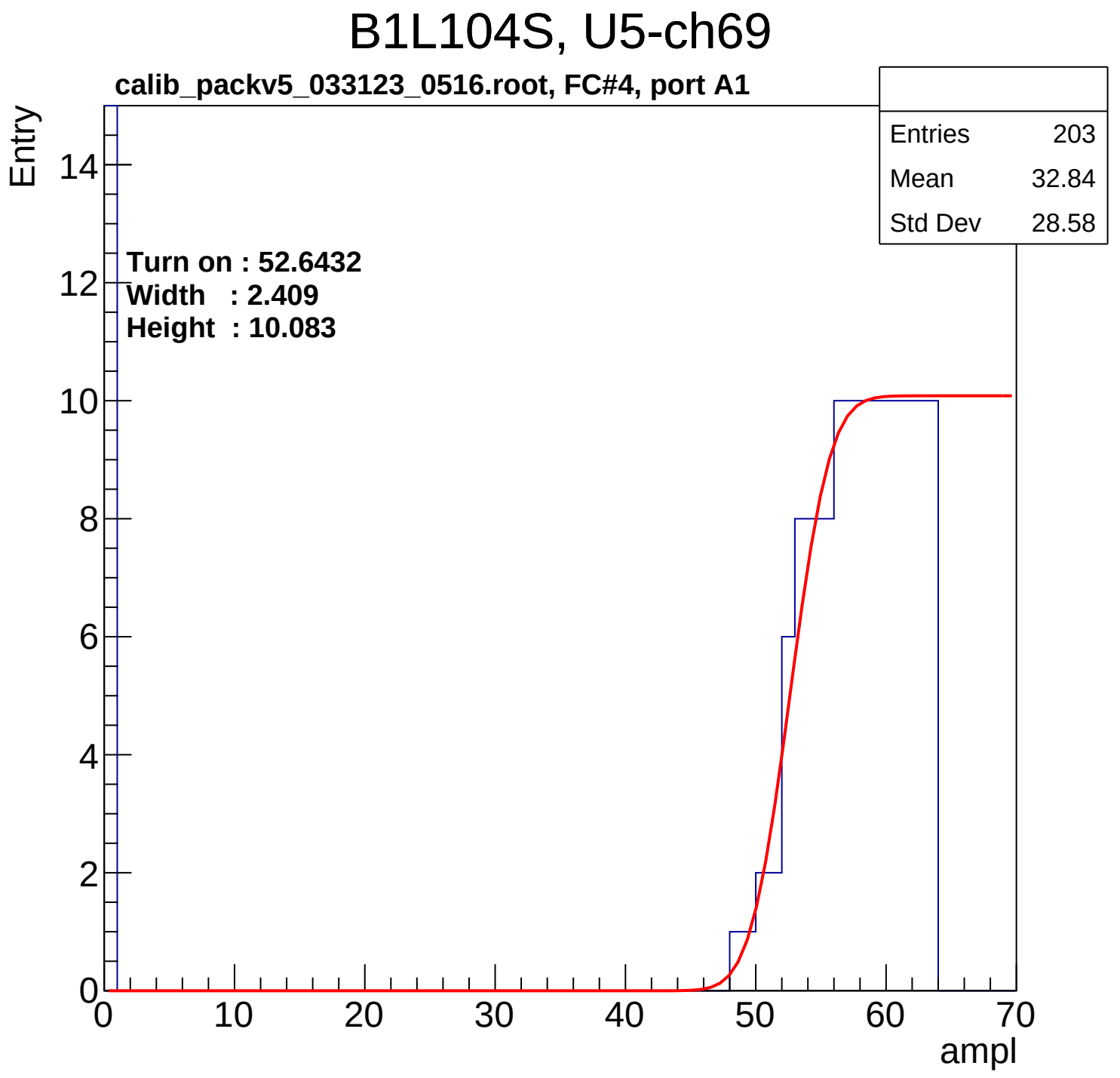

B1L104S, U5-ch64
calib_packv5_033123_0516.root, FC#4, port A1
Entries 223
Mean 31.92
Std Dev 28.23
Turn on : 52.2875
Width : 6.389
Height : 11.058
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

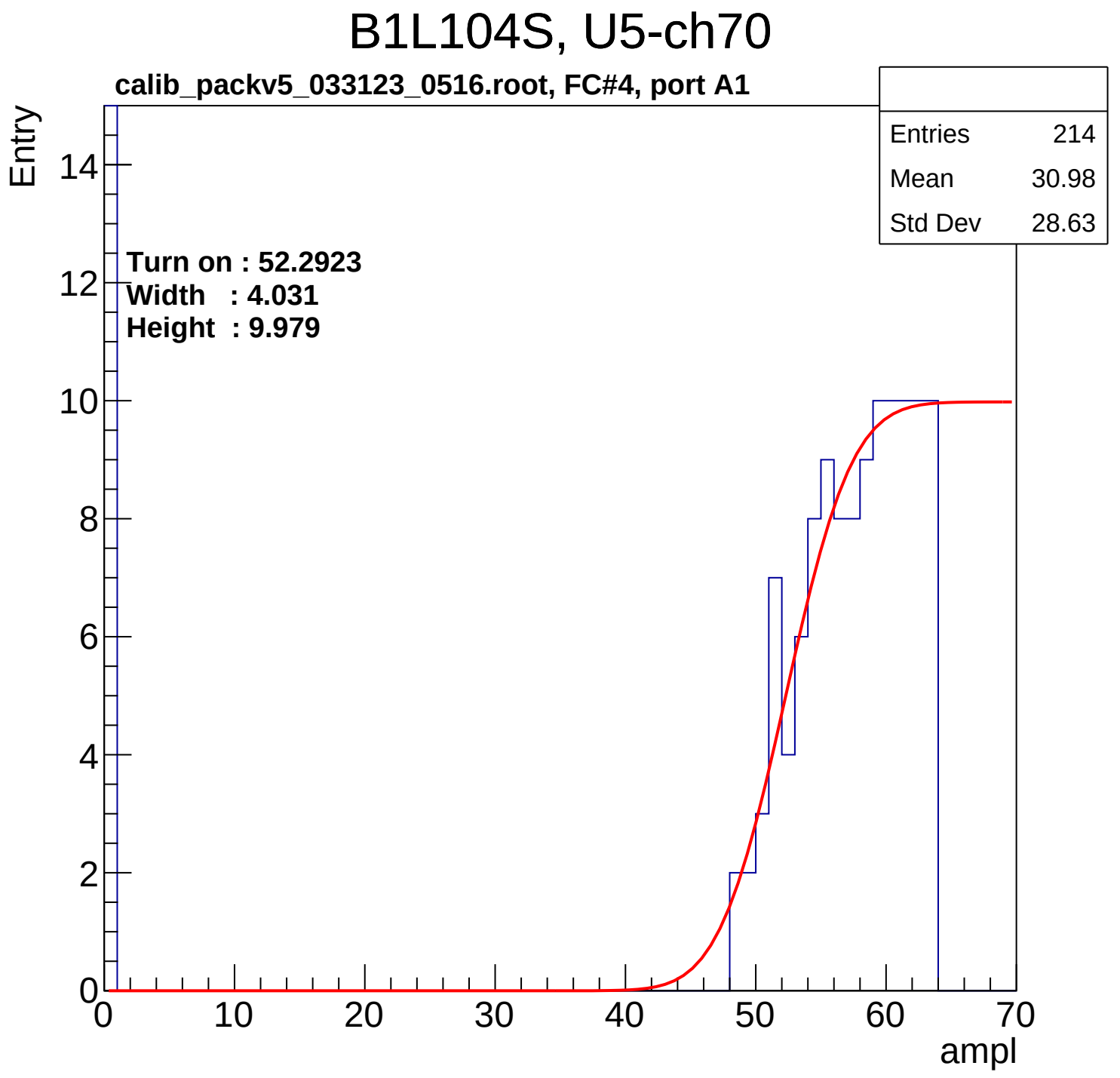

B1L104S, U5-ch65
calib_packv5_033123_0516.root, FC#4, port A1
Entries 172
Mean 35.9
Std Dev 28.14
Turn on : 54.0499
Width : 2.934
Height : 10.254
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

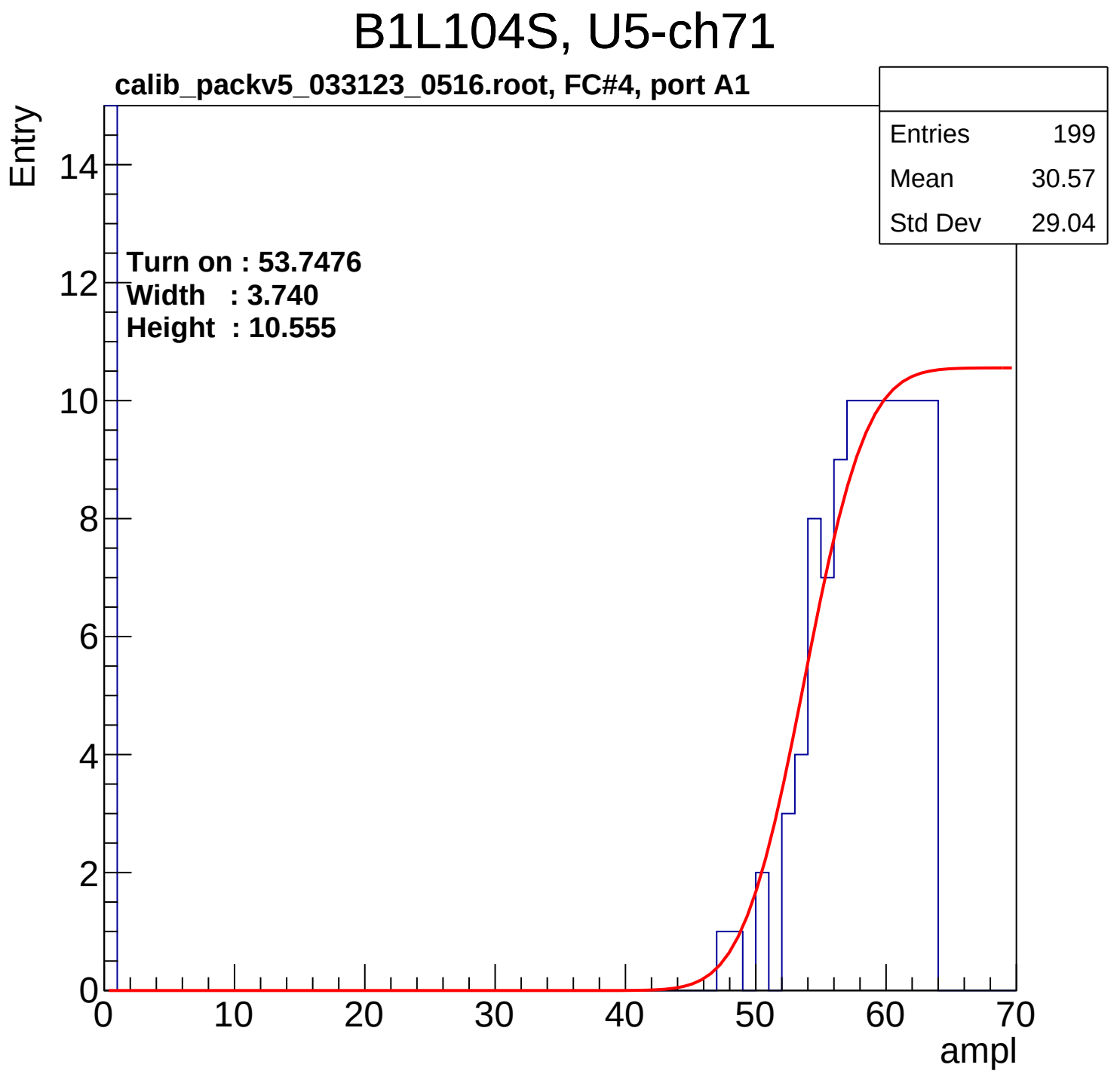

B1L104S, U5-ch66
calib_packv5_033123_0516.root, FC#4, port A1
Entries 196
Mean 34.38
Std Dev 28.14
Turn on : 52.6977
Width : 2.933
Height : 9.968
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

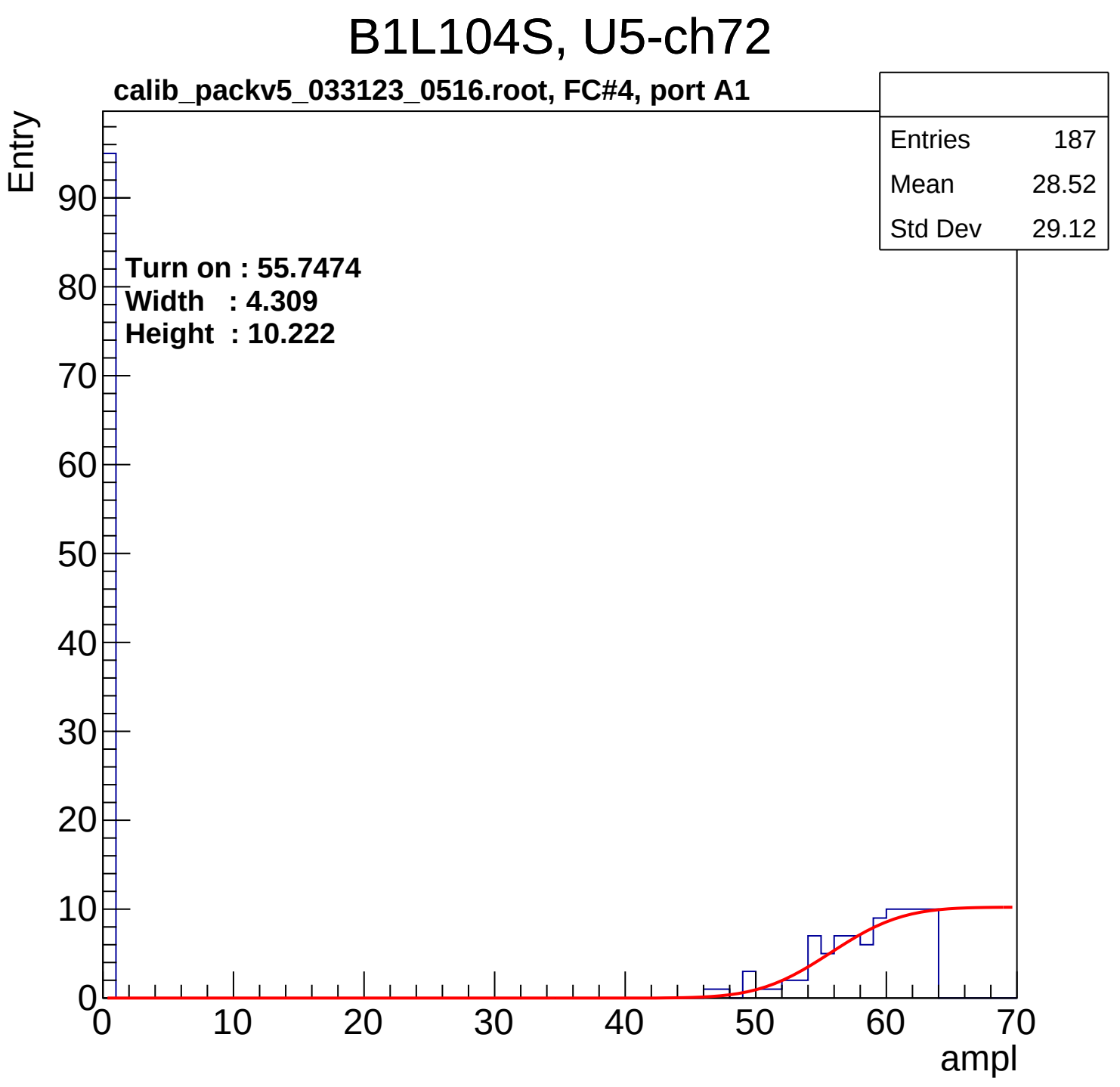

B1L104S, U5-ch67
calib_packv5_033123_0516.root, FC#4, port A1
Entries 168
Mean 34.22
Std Dev 28.71
Turn on : 54.5244
Width : 2.808
Height : 10.156
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

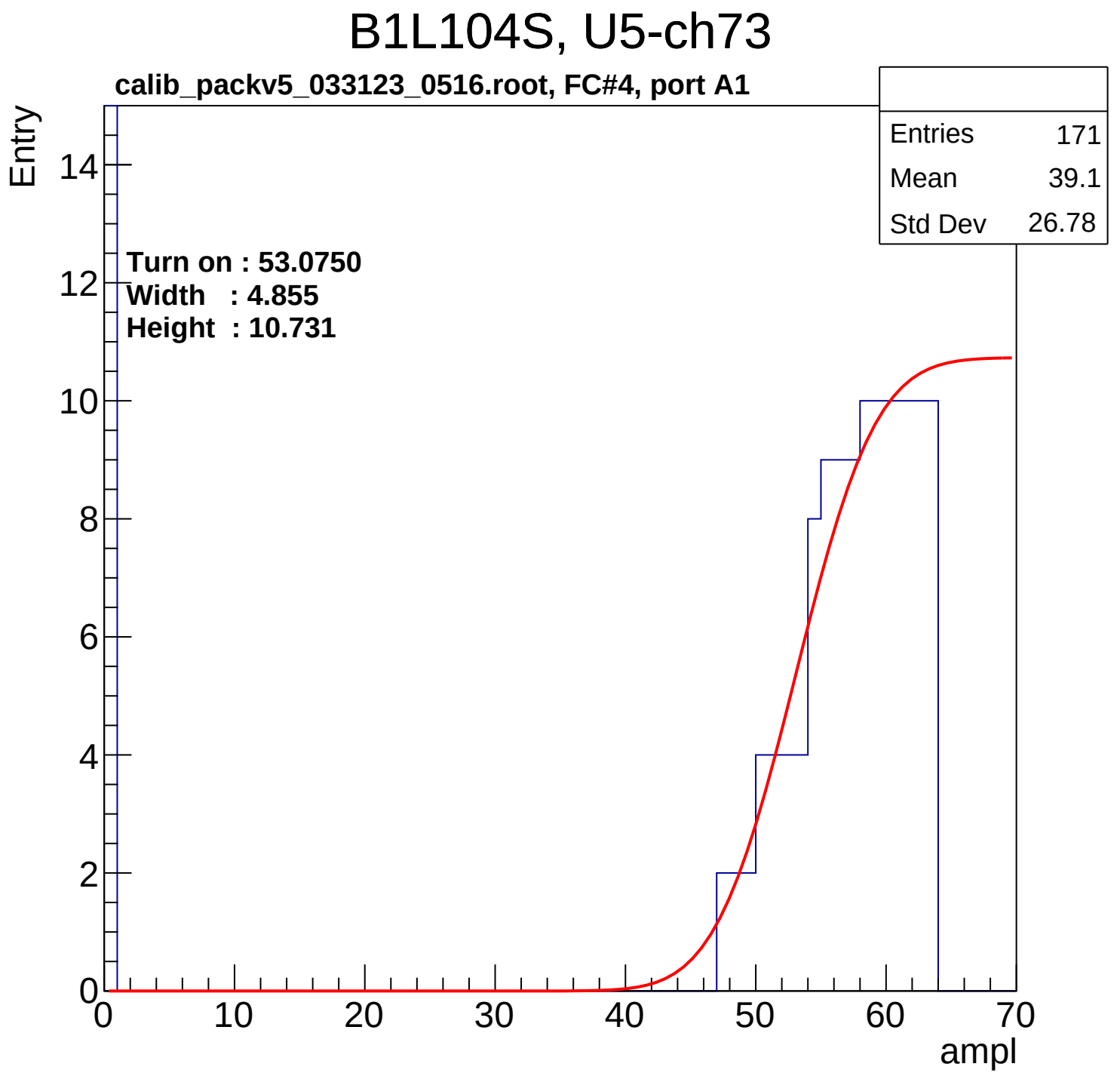

B1L104S, U5-ch68
calib_packv5_033123_0516.root, FC#4, port A1
Entries 221
Mean 35.5
Std Dev 27.26
Turn on : 50.2074
Width : 3.724
Height : 10.047
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

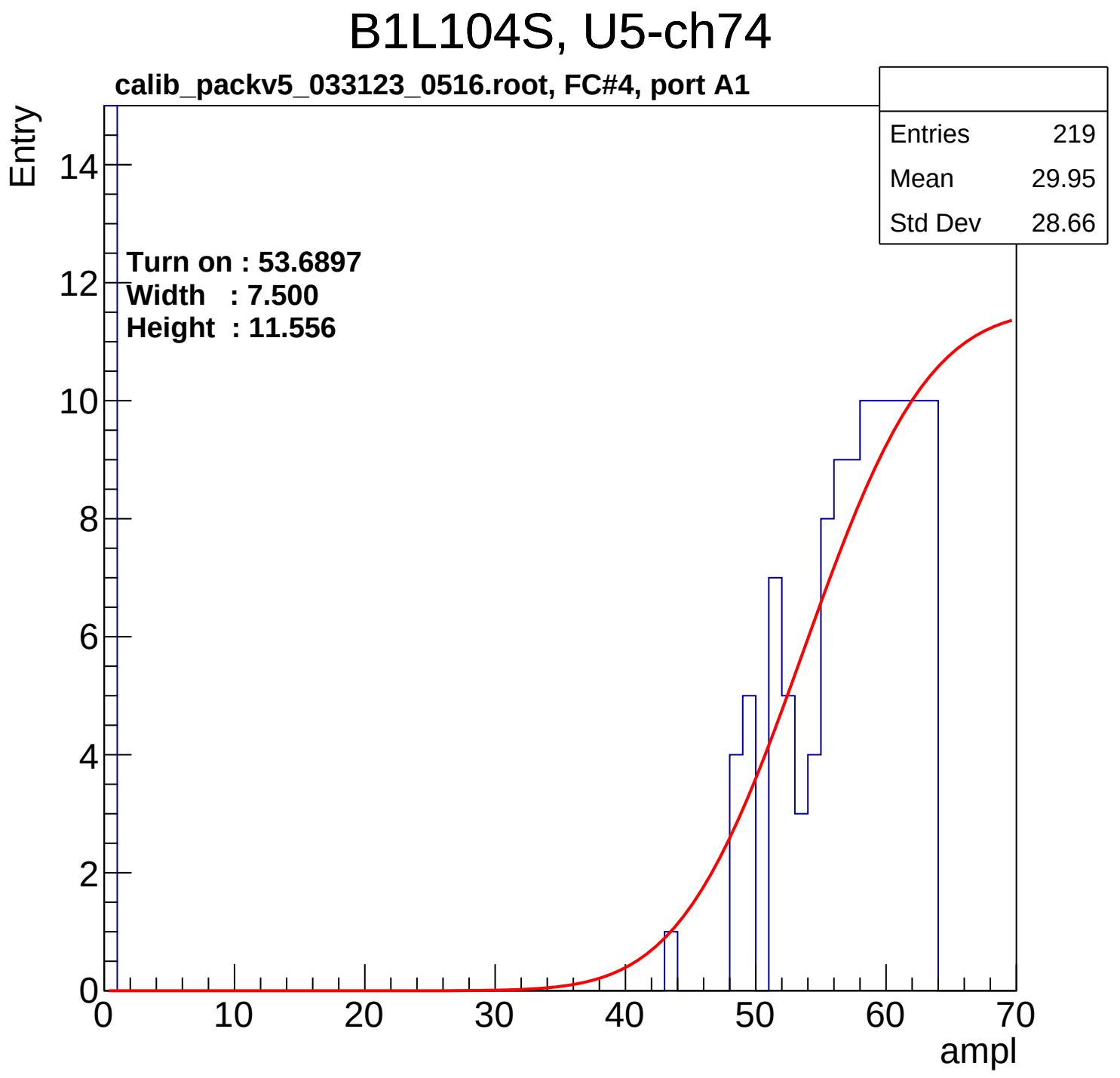

B1L104S, U5-ch69
calib_packv5_033123_0516.root, FC#4, port A1
Entries 203
Mean 32.84
Std Dev 28.58
Turn on : 52.6432
Width : 2.409
Height : 10.083
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

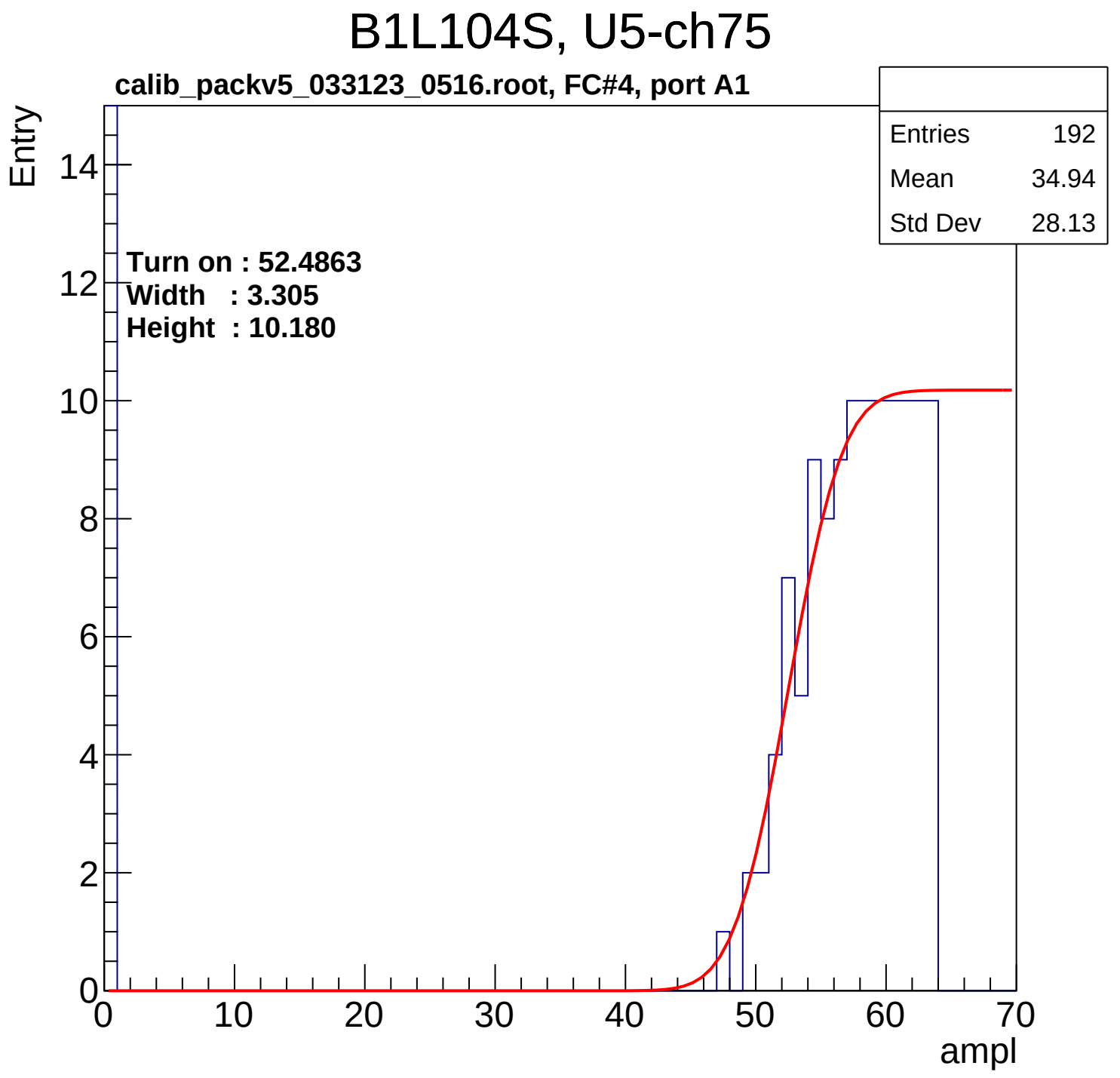

B1L104S, U5-ch70
calib_packv5_033123_0516.root, FC#4, port A1
Entries 214
Mean 30.98
Std Dev 28.63
Turn on : 52.2923
Width : 4.031
Height : 9.979
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

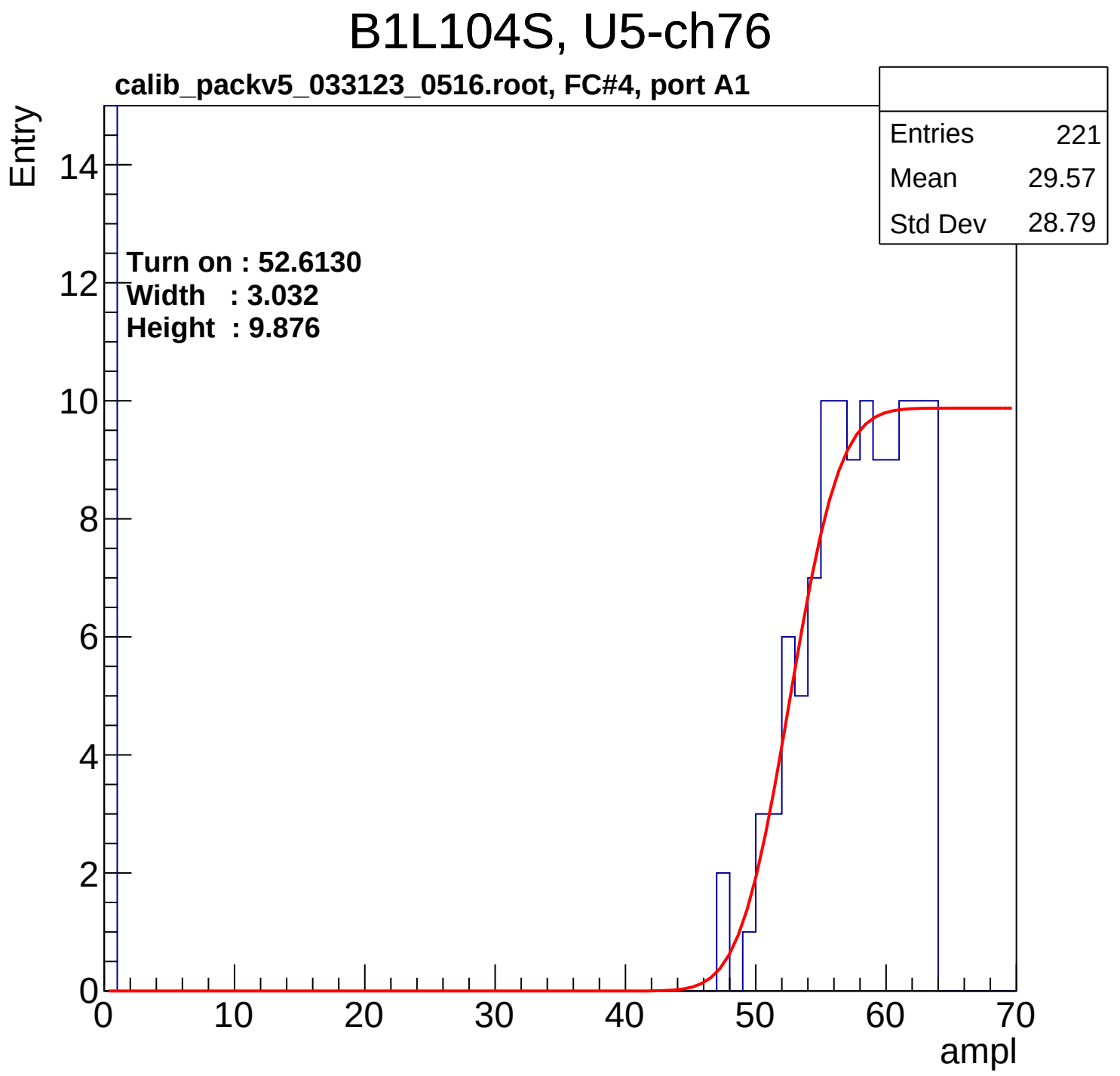

B1L104S, U5-ch71
calib_packv5_033123_0516.root, FC#4, port A1
Entries 199
Mean 30.57
Std Dev 29.04
Turn on : 53.7476
Width : 3.740
Height : 10.555
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

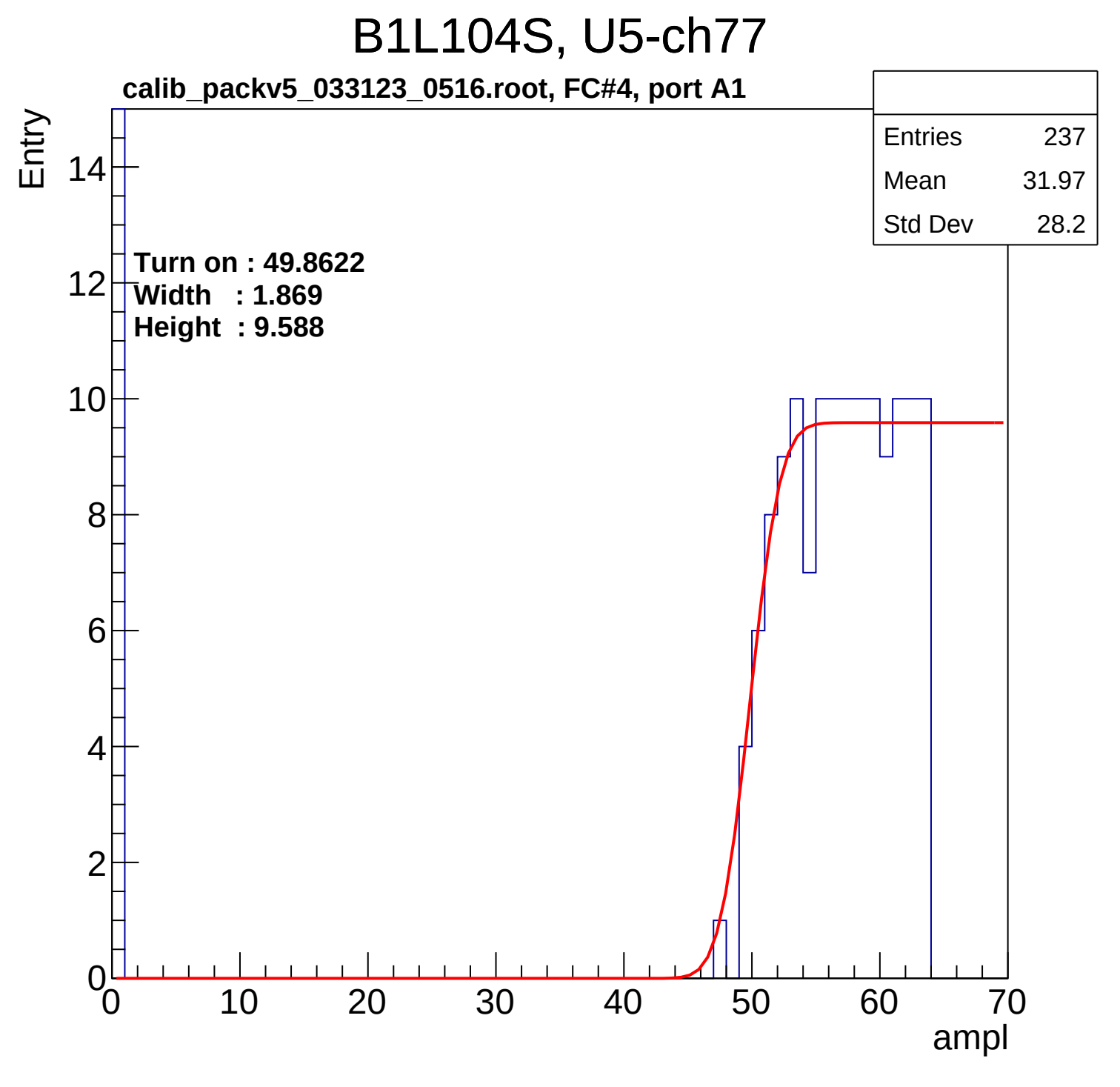

B1L104S, U5-ch72
calib_packv5_033123_0516.root, FC#4, port A1
Entries 187
Mean 28.52
Std Dev 29.12
Turn on : 55.7474
Width : 4.309
Height : 10.222
Entry
ampl
0
10
20
30
40
50
60
70
80
90

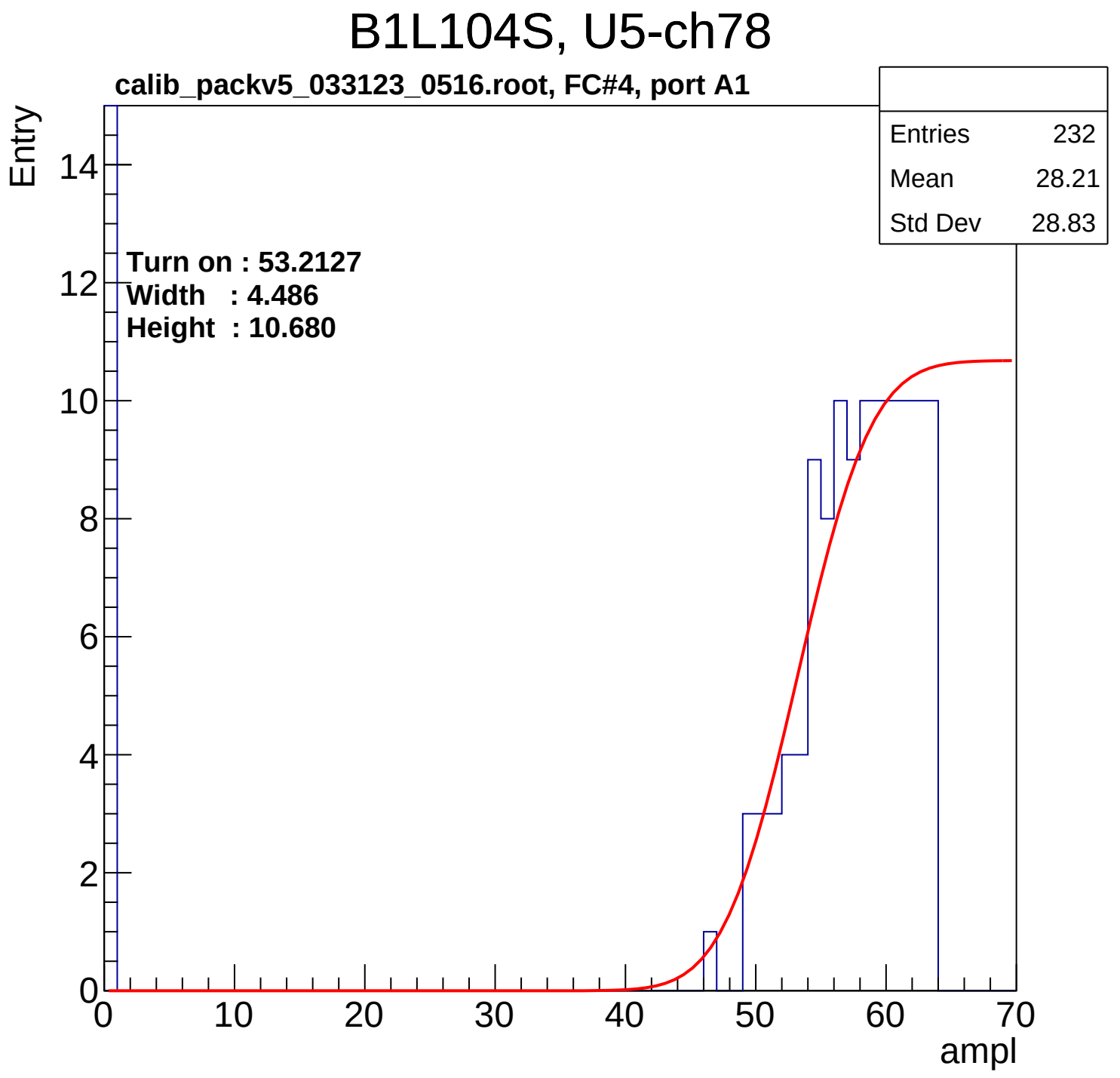

B1L104S, U5-ch73
calib_packv5_033123_0516.root, FC#4, port A1
Entries 171
Mean 39.1
Std Dev 26.78
Turn on : 53.0750
Width : 4.855
Height : 10.731
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

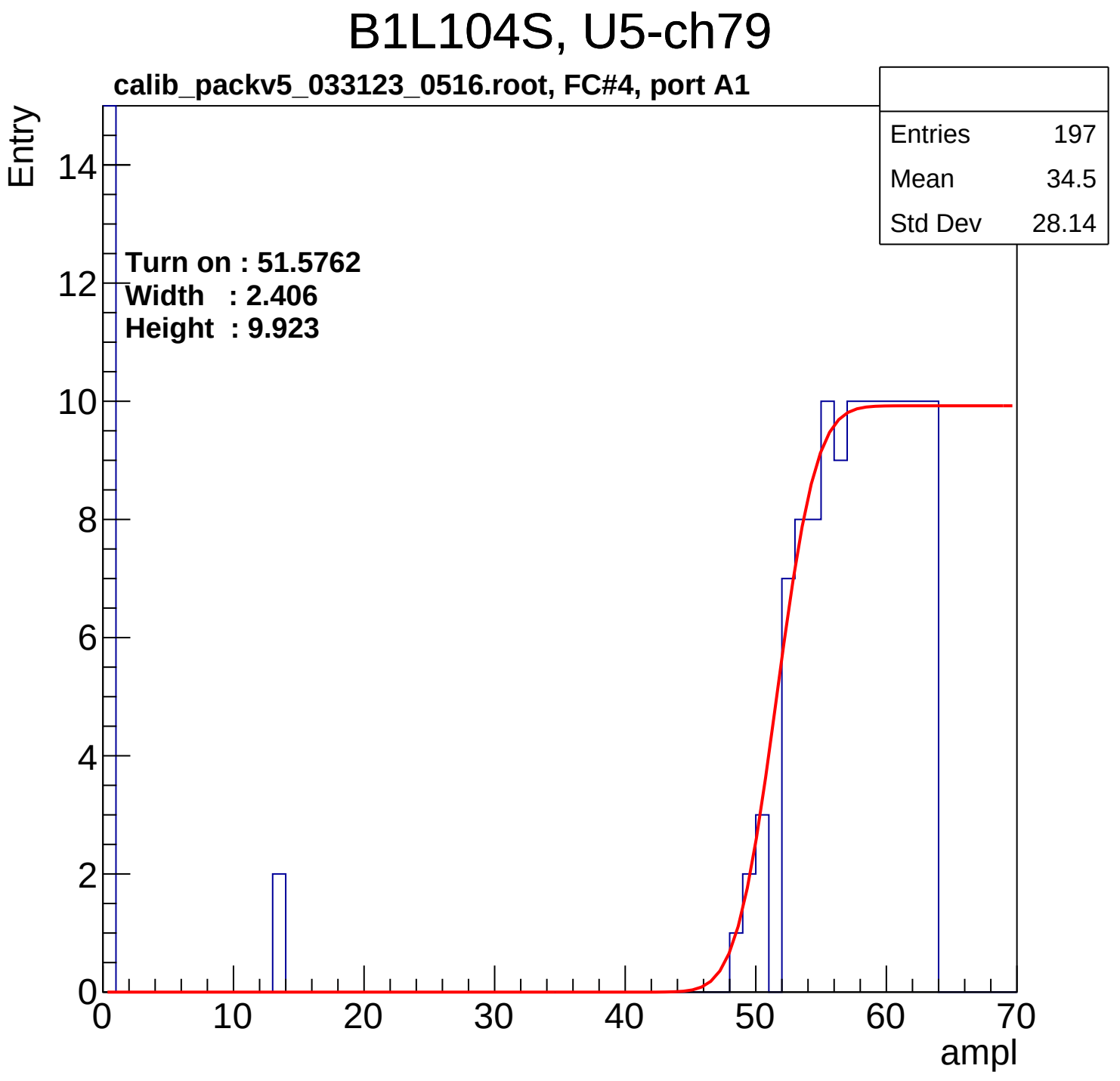

B1L104S, U5-ch74
calib_packv5_033123_0516.root, FC#4, port A1
Entries 219
Mean 29.95
Std Dev 28.66
Turn on : 53.6897
Width : 7.500
Height : 11.556
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

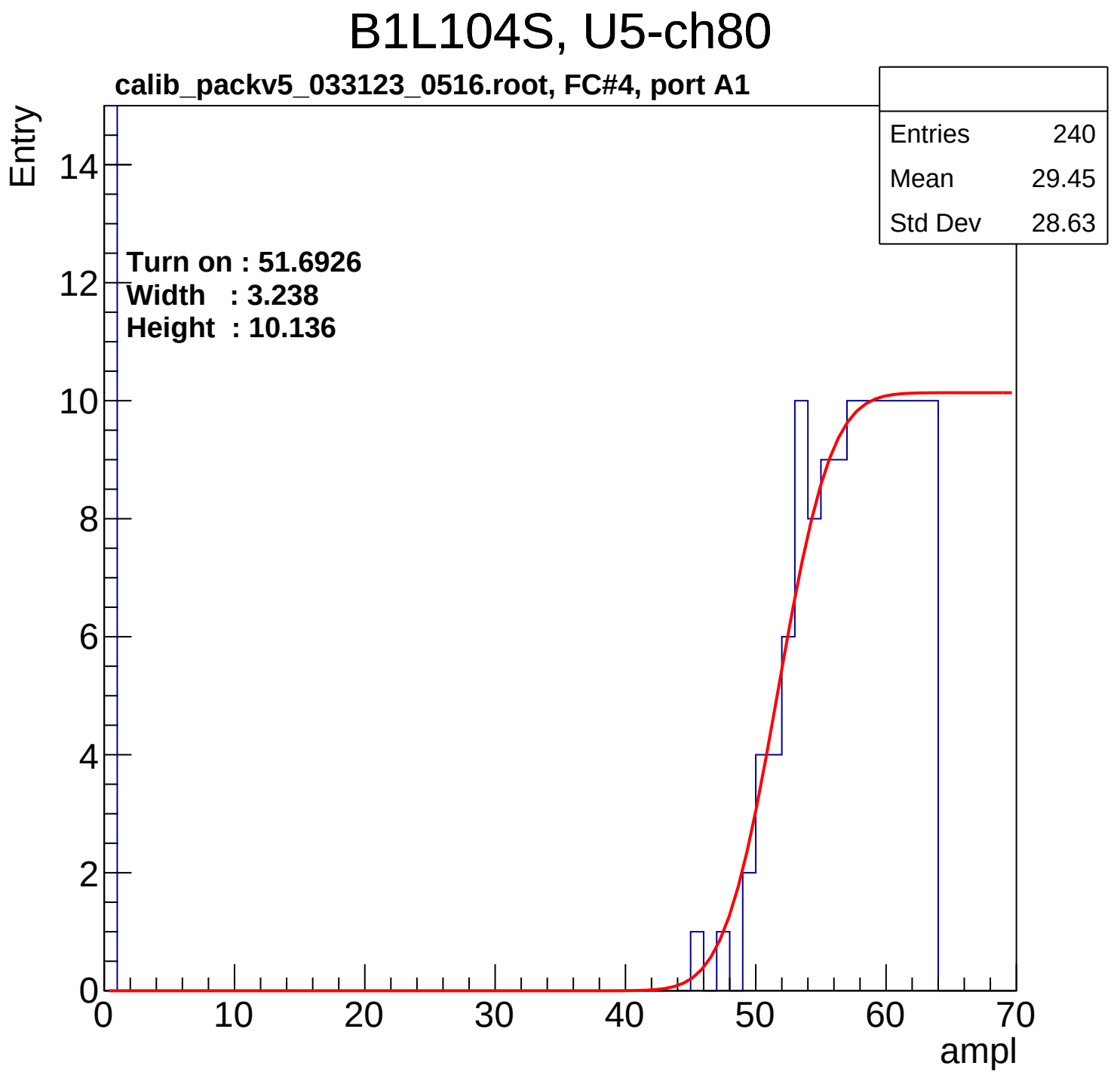

B1L104S, U5-ch75
calib_packv5_033123_0516.root, FC#4, port A1
Entries 192
Mean 34.94
Std Dev 28.13
Turn on : 52.4863
Width : 3.305
Height : 10.180
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

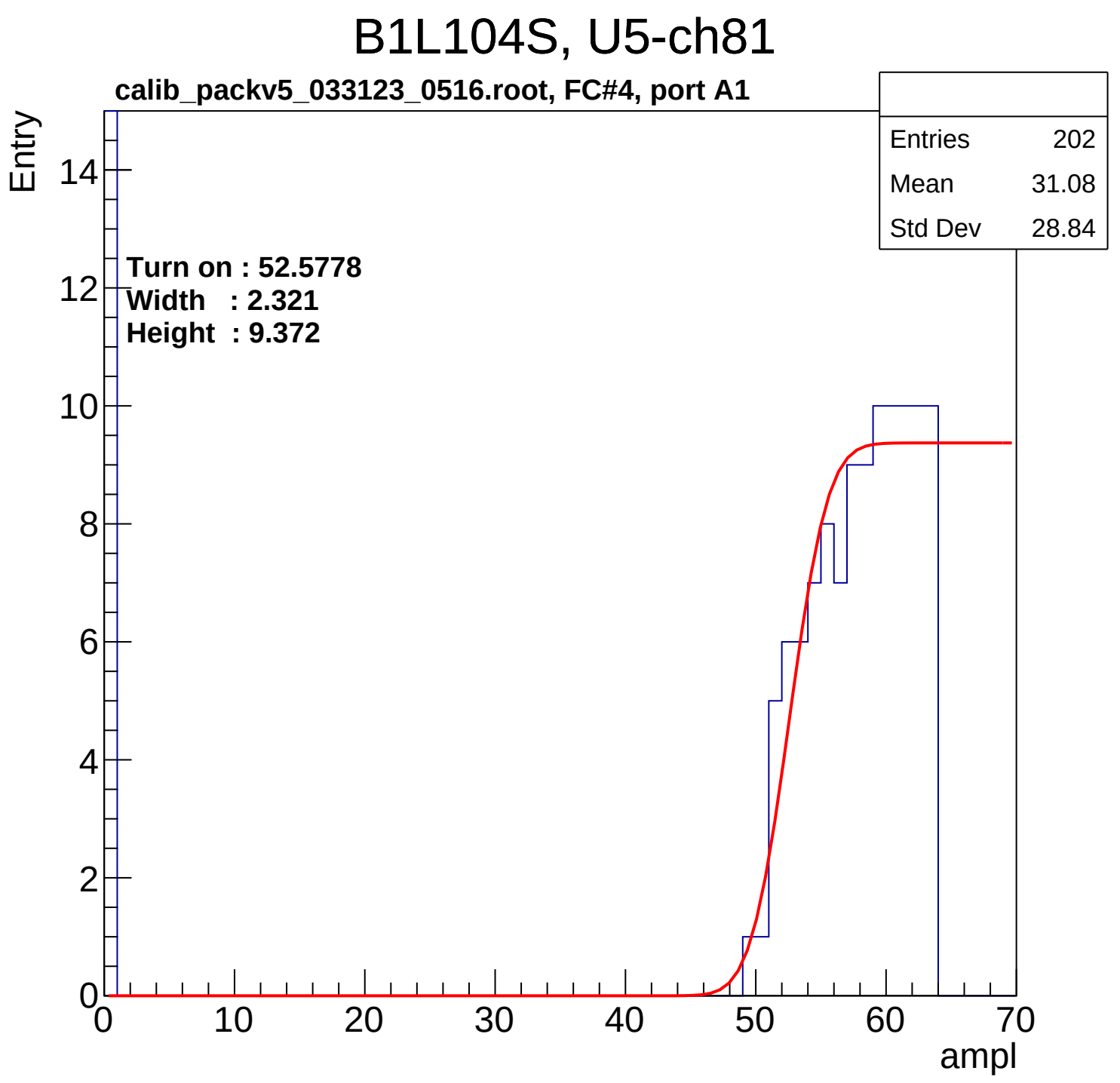

B1L104S, U5-ch76
calib_packv5_033123_0516.root, FC#4, port A1
Entries 221
Mean 29.57
Std Dev 28.79
Turn on : 52.6130
Width : 3.032
Height : 9.876
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

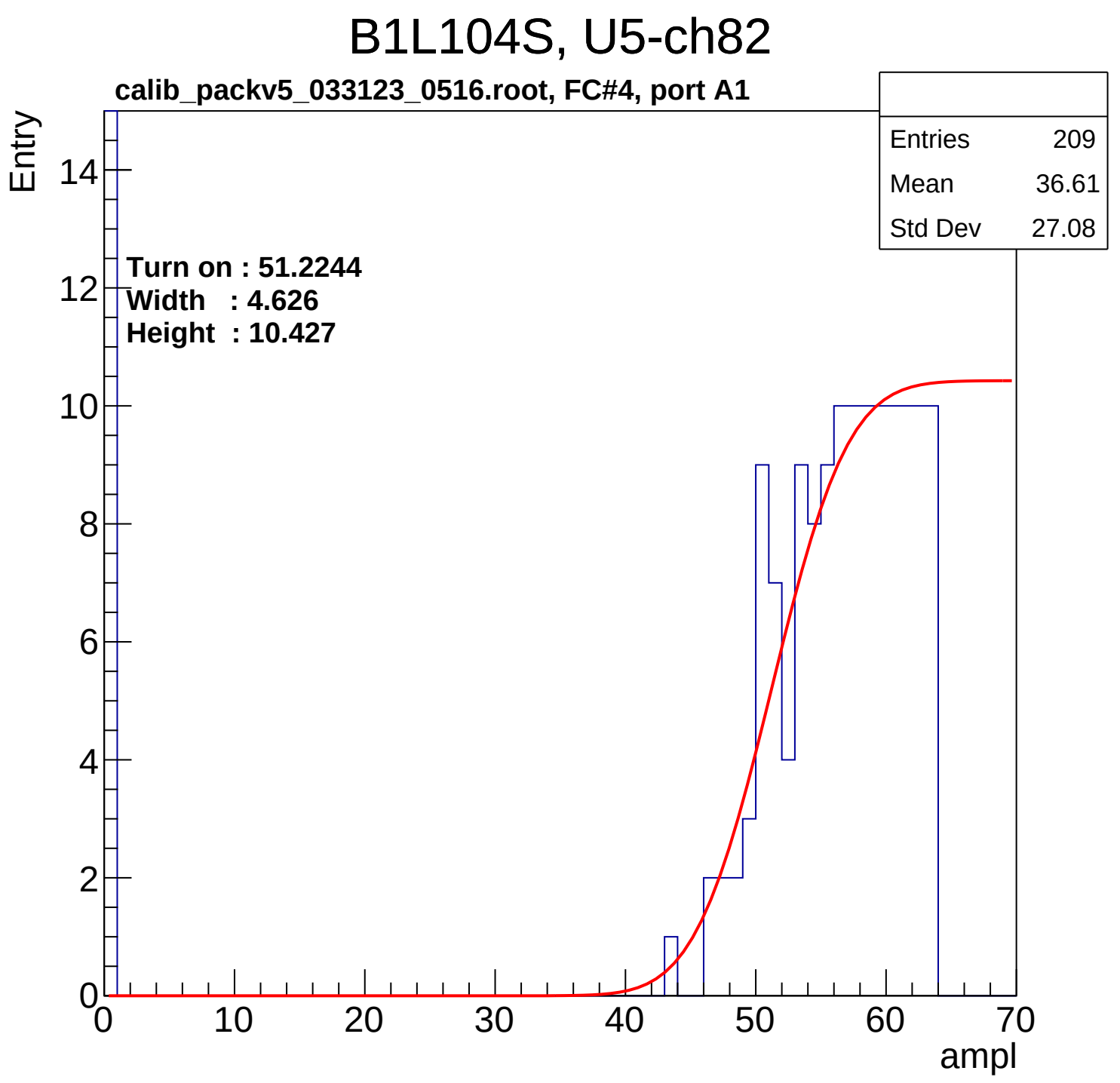

B1L104S, U5-ch77
calib_packv5_033123_0516.root, FC#4, port A1
Entries 237
Mean 31.97
Std Dev 28.2
Turn on : 49.8622
Width : 1.869
Height : 9.588
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

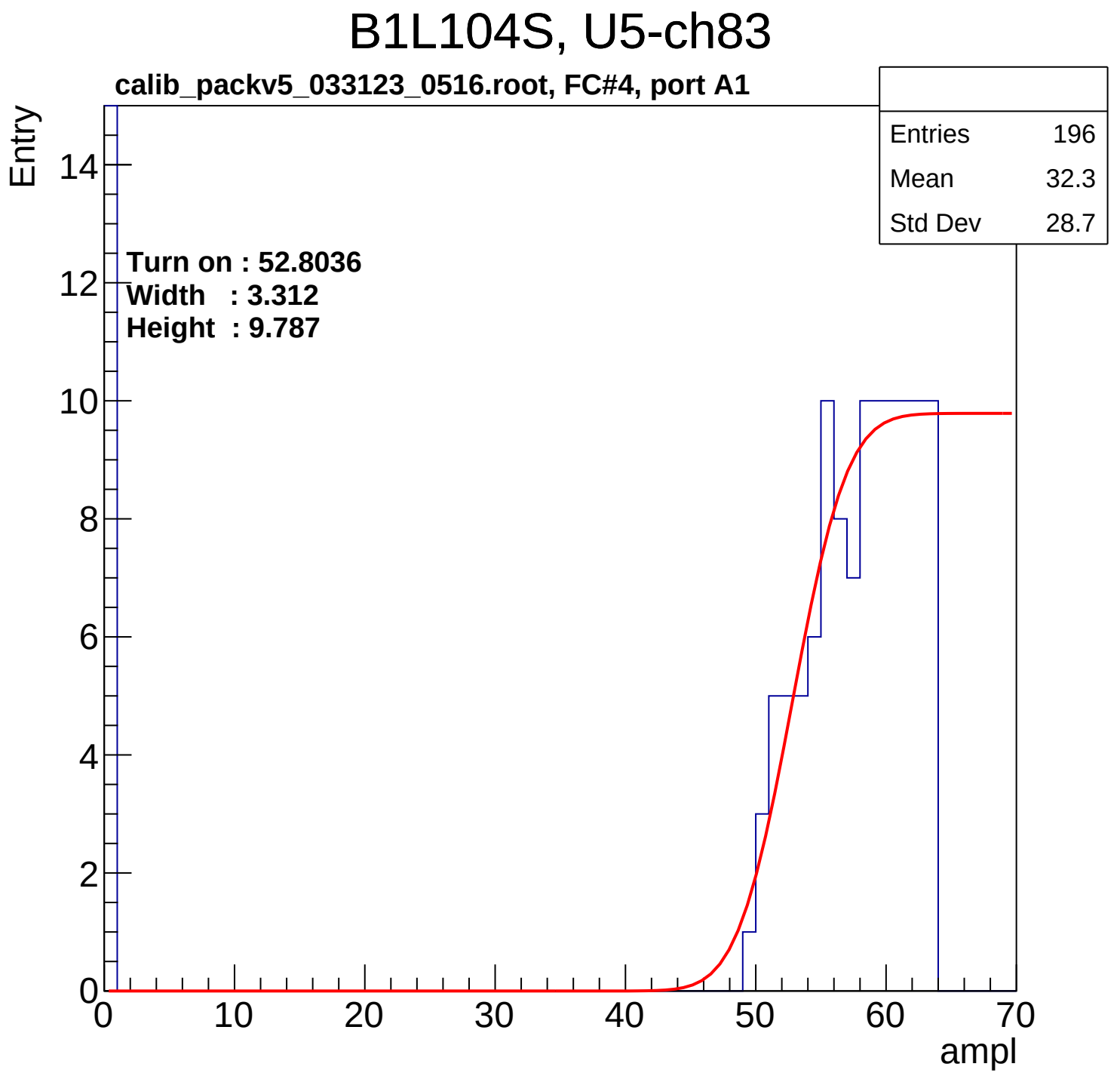

B1L104S, U5-ch78
calib_packv5_033123_0516.root, FC#4, port A1
Entries 232
Mean 28.21
Std Dev 28.83
Turn on : 53.2127
Width : 4.486
Height : 10.680
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

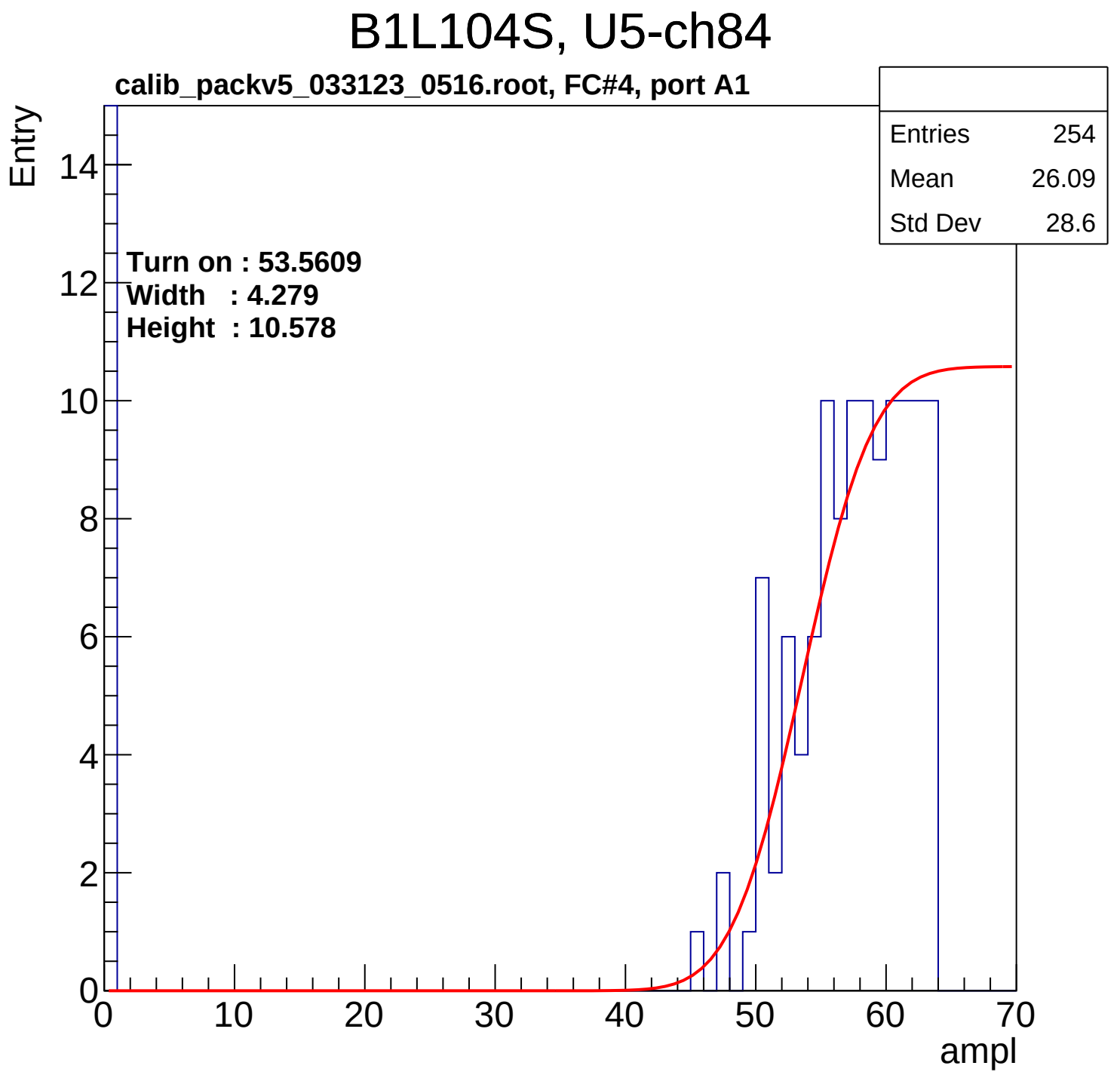

B1L104S, U5-ch79
calib_packv5_033123_0516.root, FC#4, port A1
Entries 197
Mean 34.5
Std Dev 28.14
Turn on : 51.5762
Width : 2.406
Height : 9.923
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

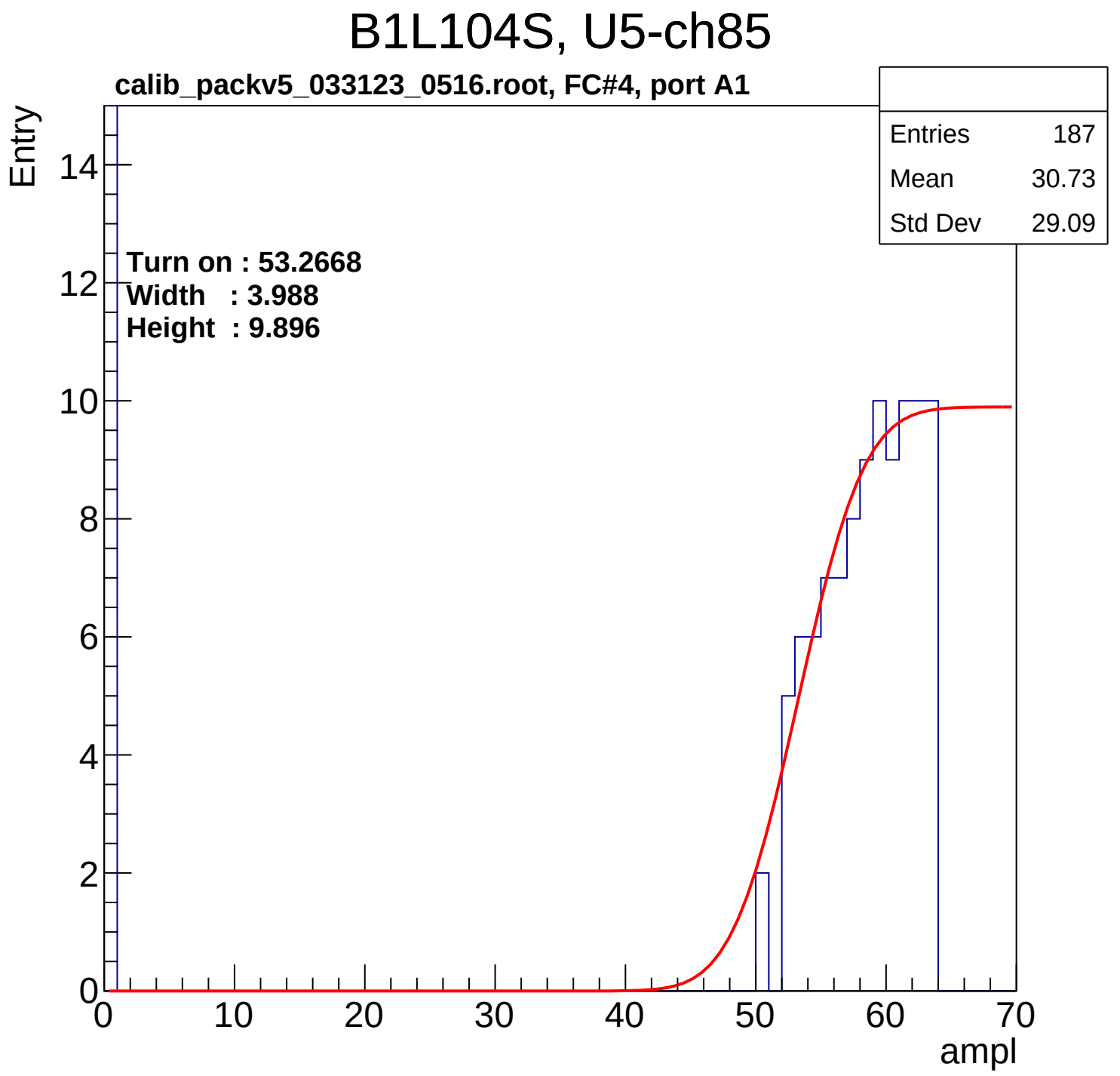

B1L104S, U5-ch80
calib_packv5_033123_0516.root, FC#4, port A1
Entries 240
Mean 29.45
Std Dev 28.63
Turn on : 51.6926
Width : 3.238
Height : 10.136
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

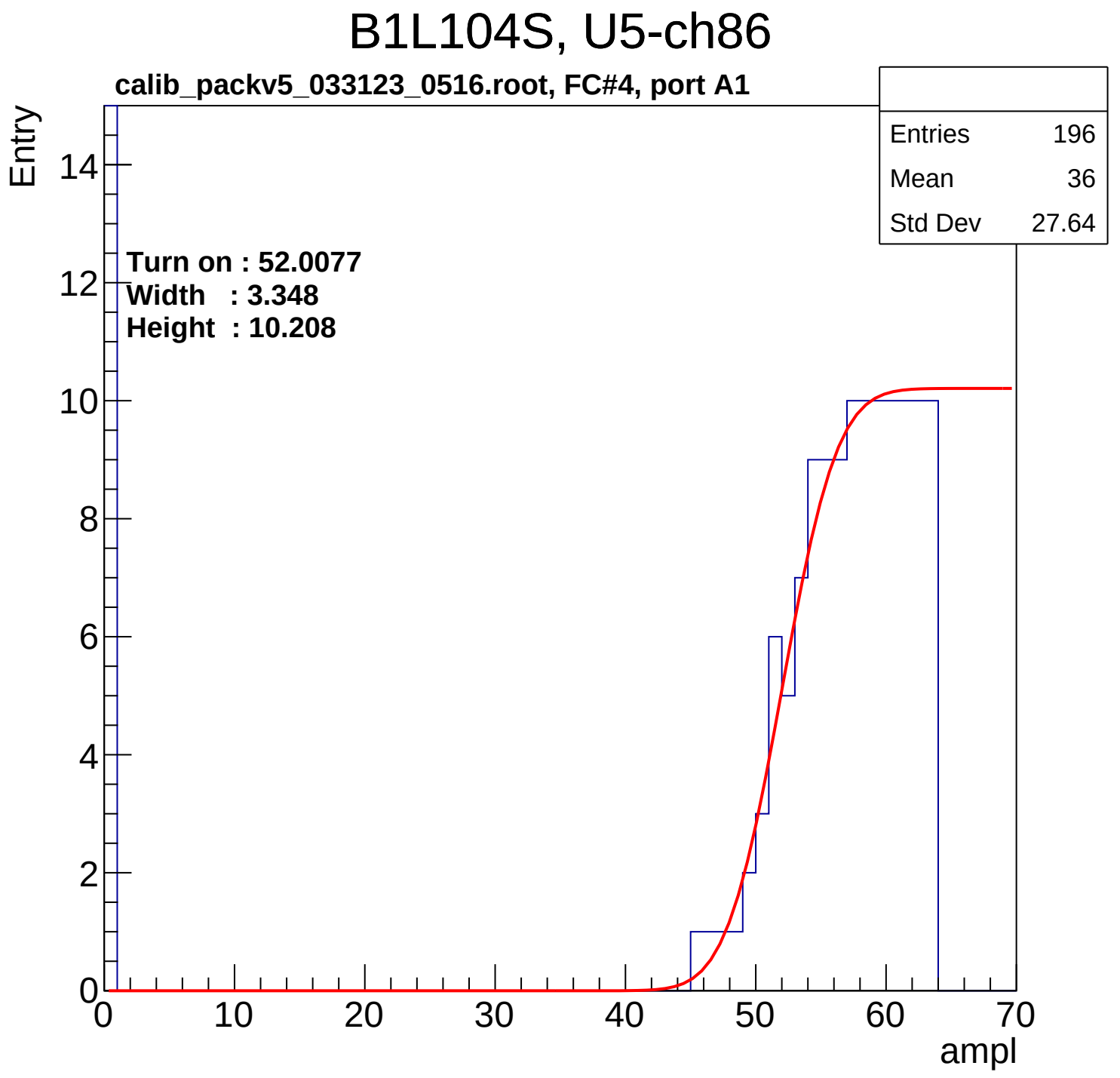

B1L104S, U5-ch81
calib_packv5_033123_0516.root, FC#4, port A1
Entries 202
Mean 31.08
Std Dev 28.84
Turn on : 52.5778
Width : 2.321
Height : 9.372
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

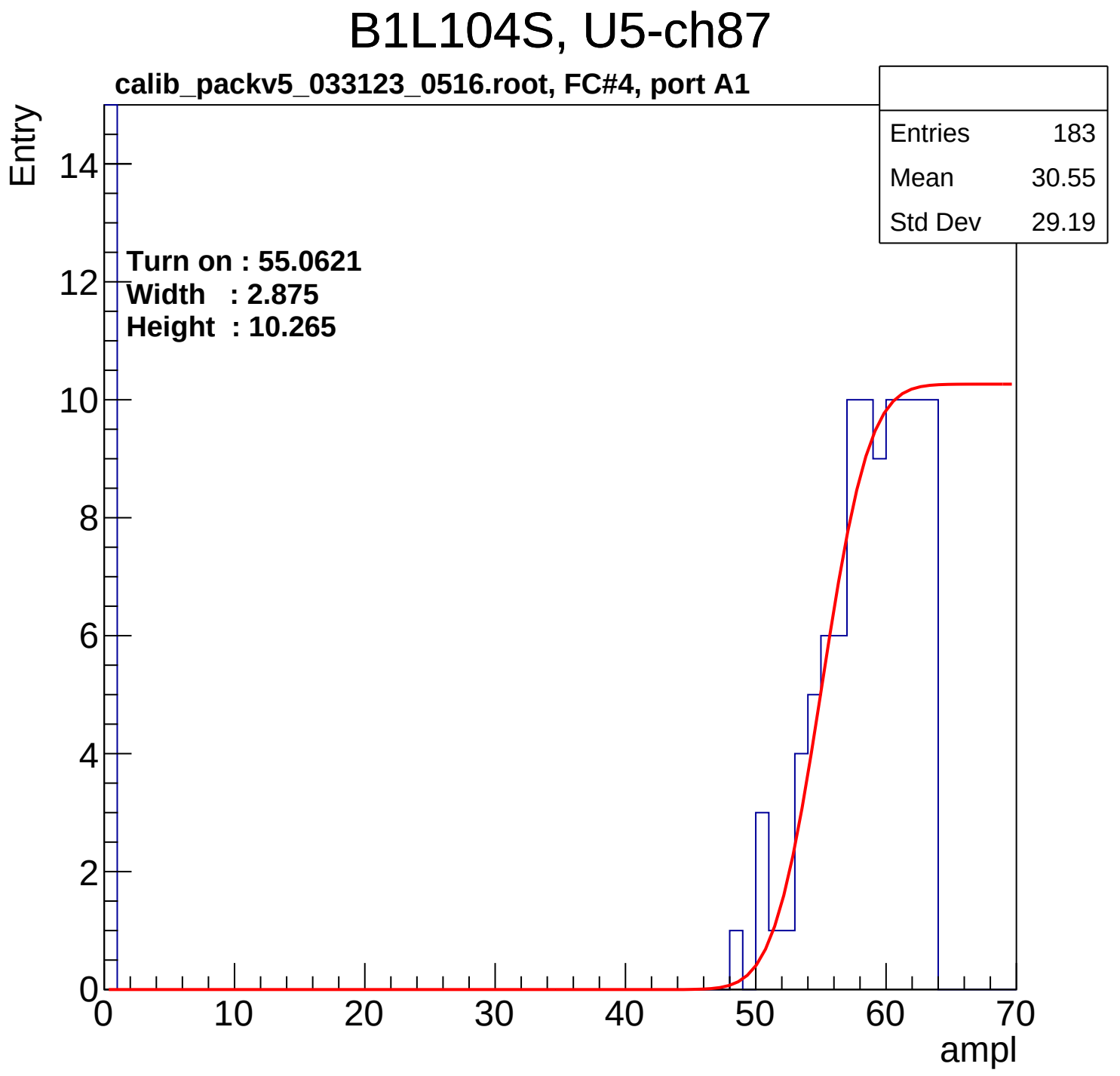

B1L104S, U5-ch82
calib_packv5_033123_0516.root, FC#4, port A1
Entries 209
Mean 36.61
Std Dev 27.08
Turn on : 51.2244
Width : 4.626
Height : 10.427
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

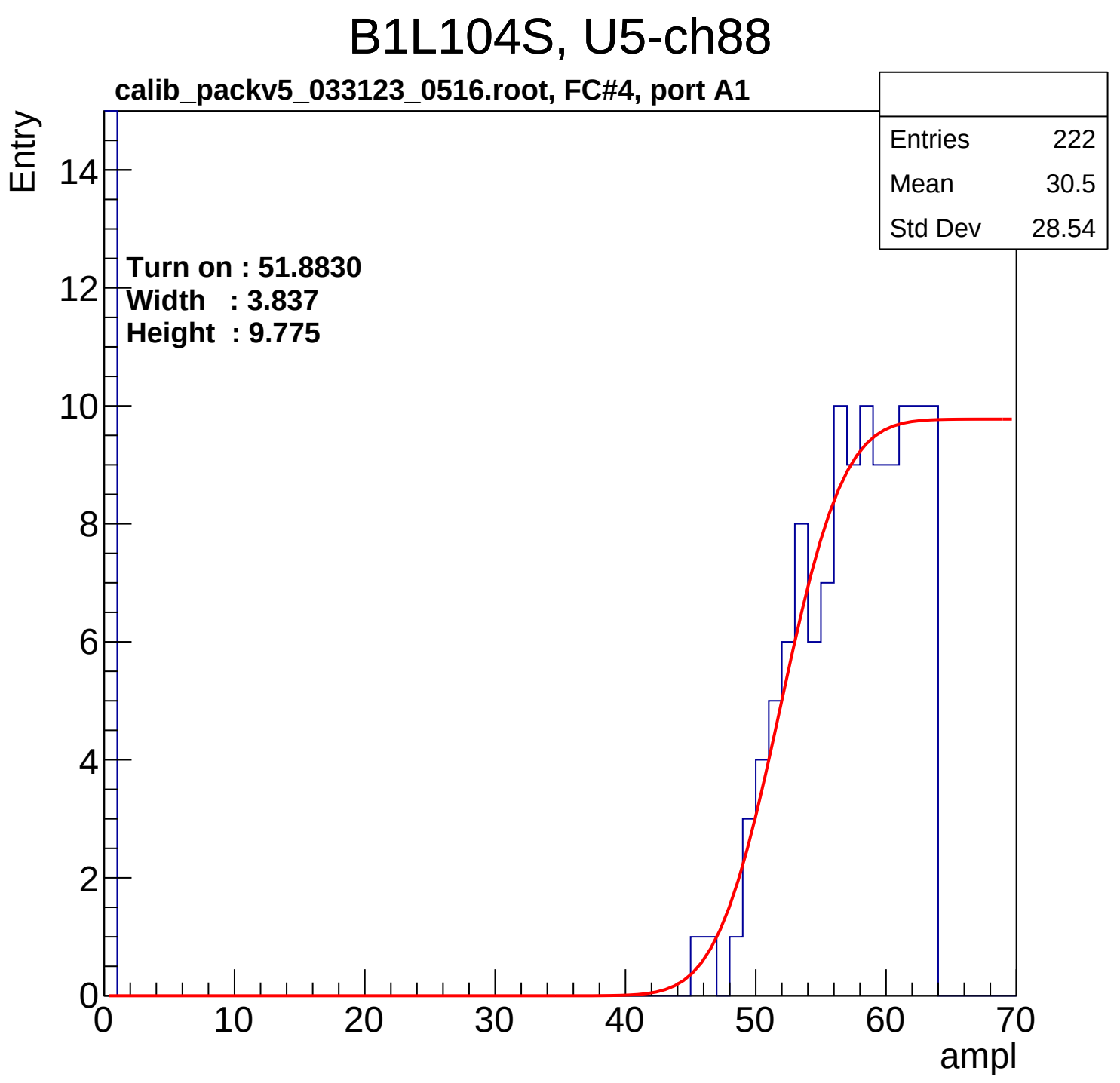

B1L104S, U5-ch83
calib_packv5_033123_0516.root, FC#4, port A1
Entries 196
Mean 32.3
Std Dev 28.7
Turn on : 52.8036
Width : 3.312
Height : 9.787
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

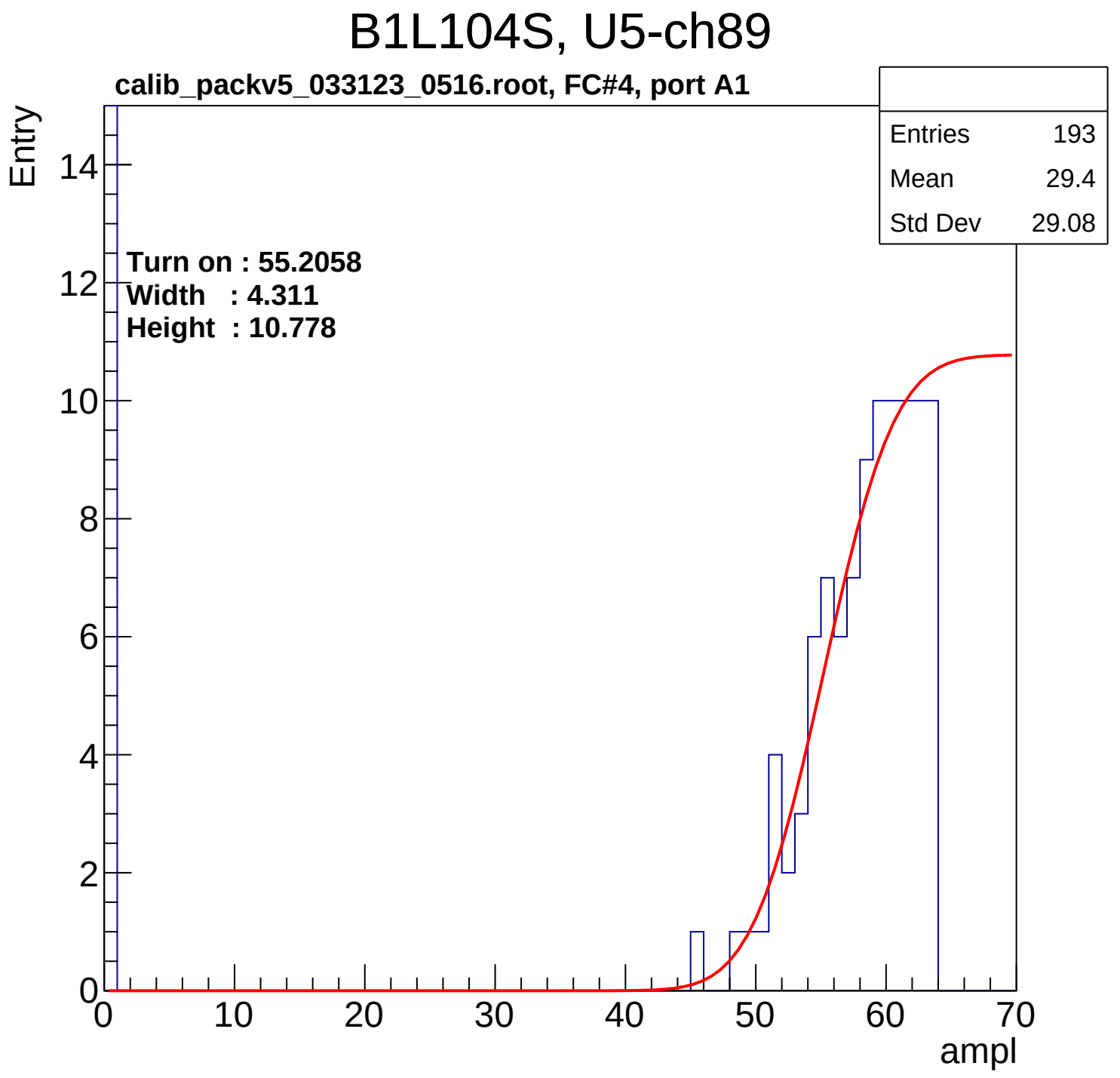

B1L104S, U5-ch84
calib_packv5_033123_0516.root, FC#4, port A1
Entries 254
Mean 26.09
Std Dev 28.6
Turn on : 53.5609
Width : 4.279
Height : 10.578
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

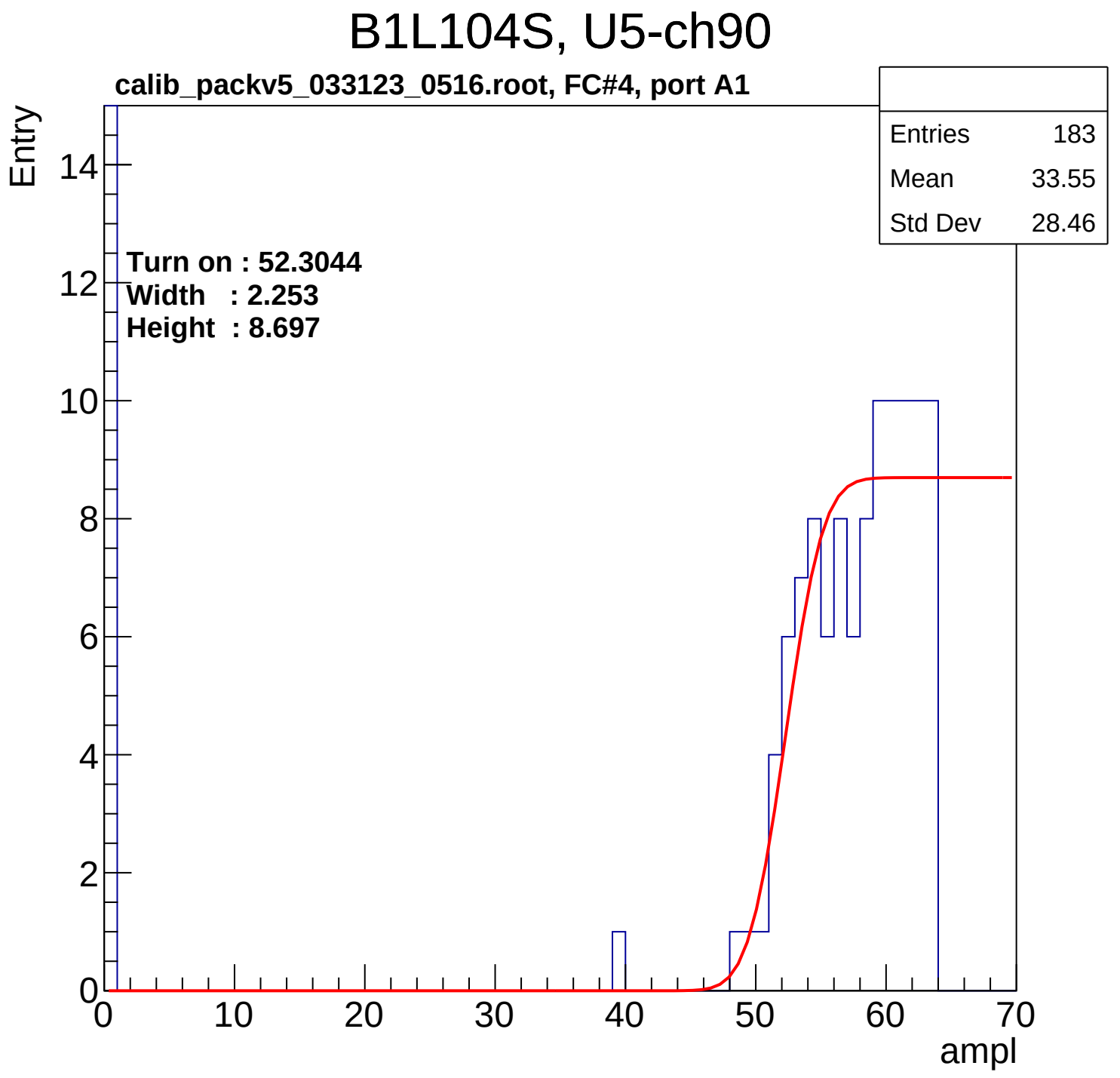

B1L104S, U5-ch85
calib_packv5_033123_0516.root, FC#4, port A1
Entries 187
Mean 30.73
Std Dev 29.09
Turn on : 53.2668
Width : 3.988
Height : 9.896
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

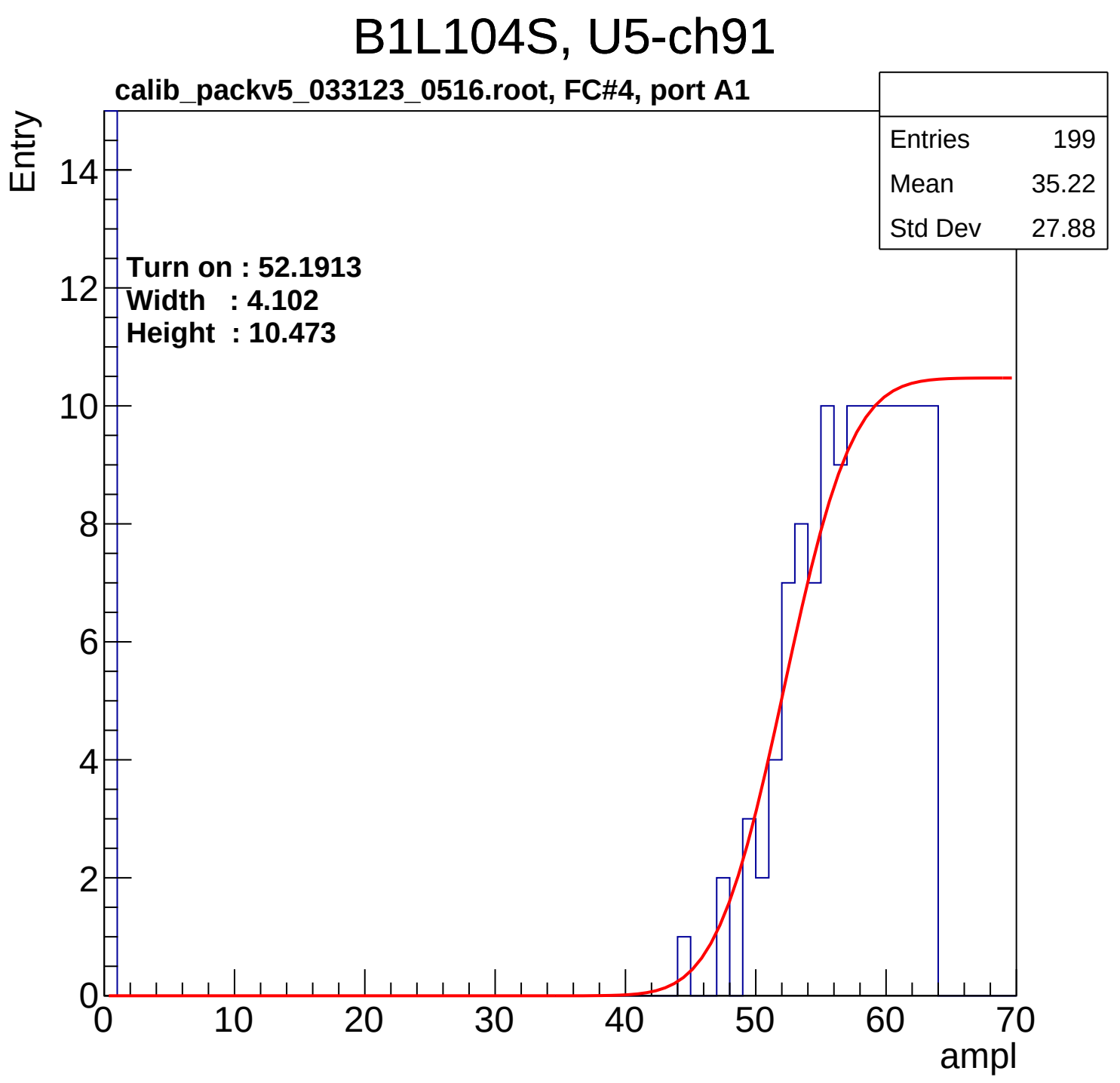

B1L104S, U5-ch86
calib_packv5_033123_0516.root, FC#4, port A1
Entries 196
Mean 36
Std Dev 27.64
Turn on : 52.0077
Width : 3.348
Height : 10.208
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

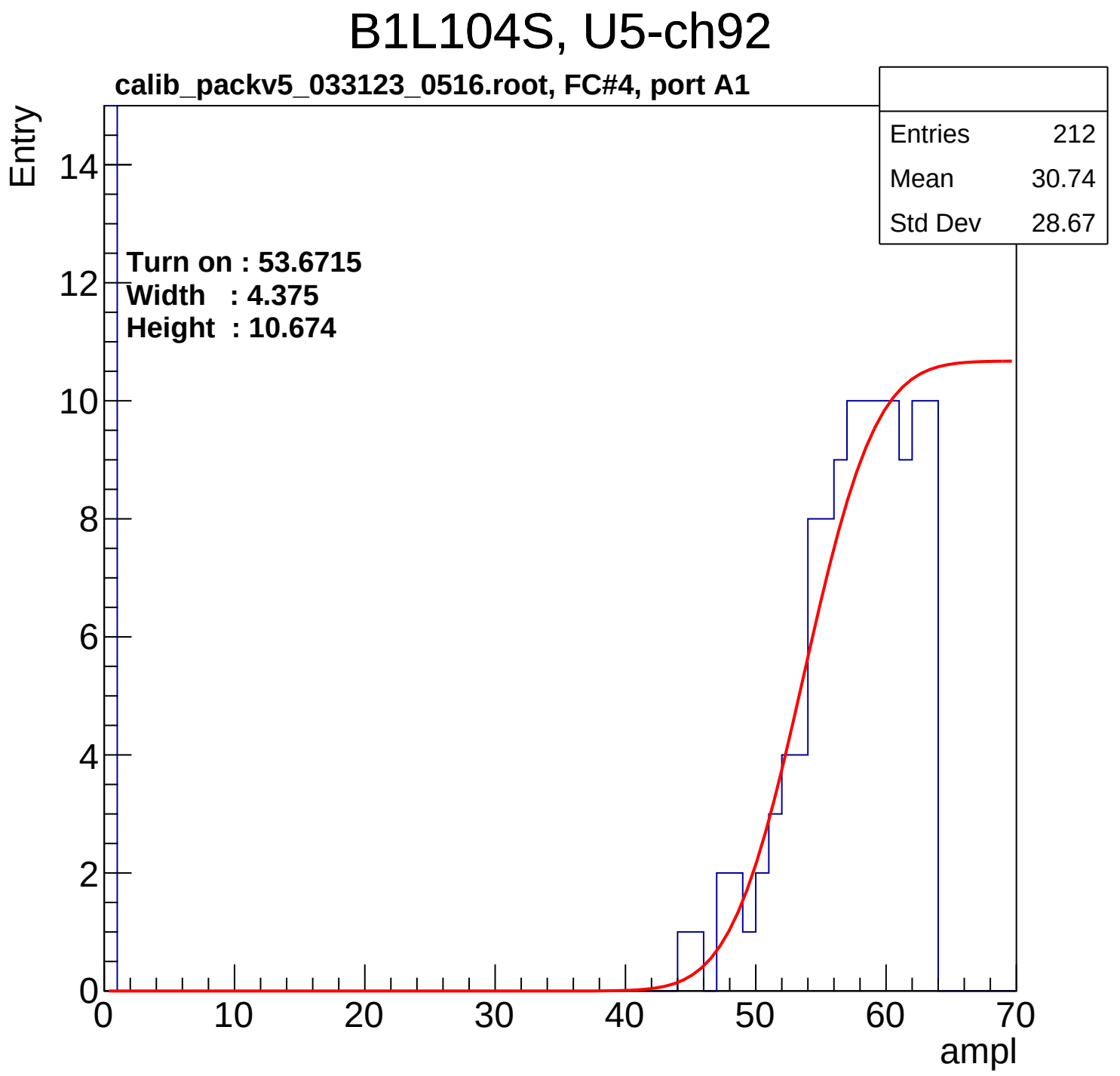

B1L104S, U5-ch87
calib_packv5_033123_0516.root, FC#4, port A1
Entries 183
Mean 30.55
Std Dev 29.19
Turn on : 55.0621
Width : 2.875
Height : 10.265
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

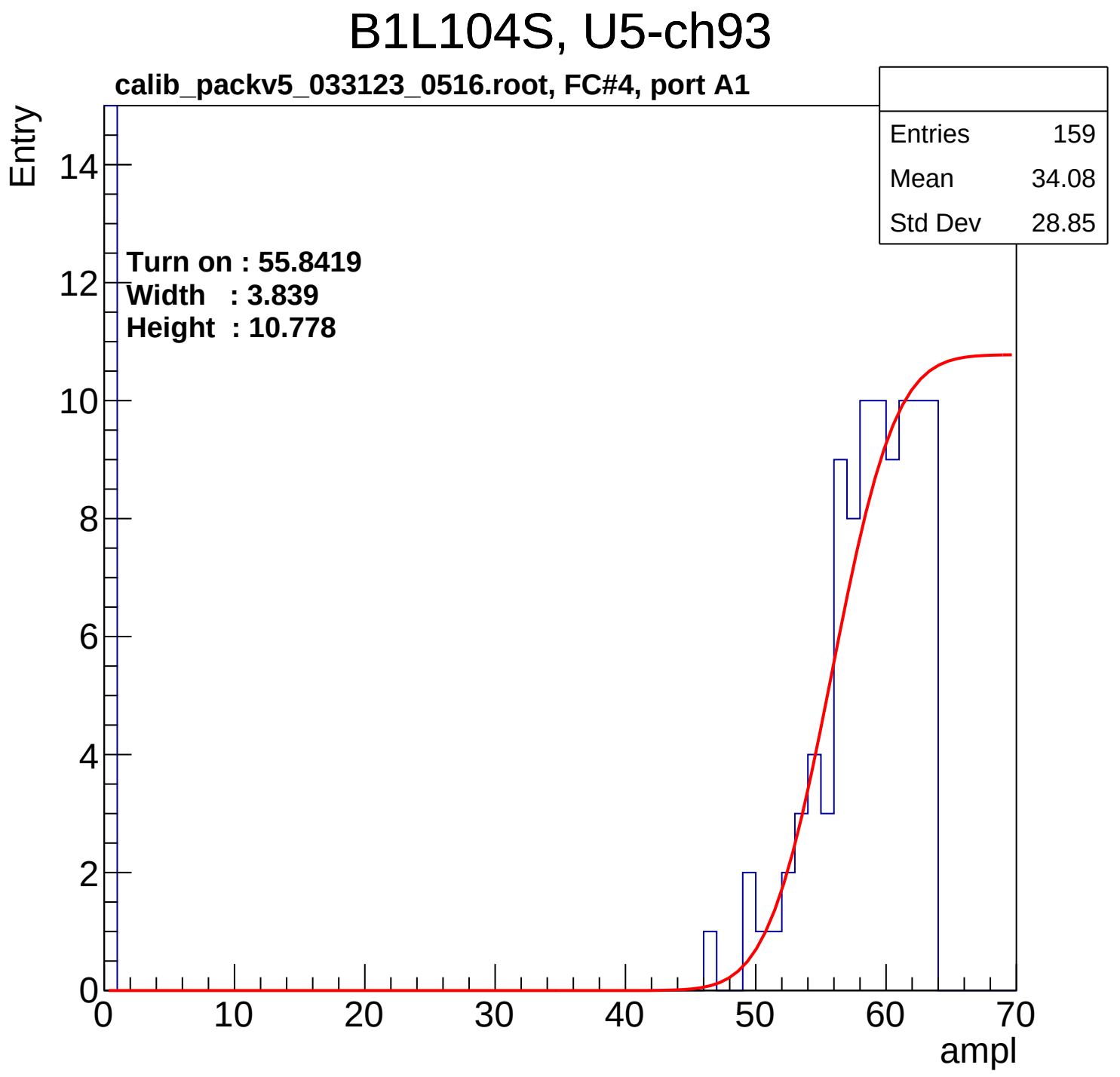

B1L104S, U5-ch88
calib_packv5_033123_0516.root, FC#4, port A1
Entries 222
Mean 30.5
Std Dev 28.54
Turn on : 51.8830
Width : 3.837
Height : 9.775
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

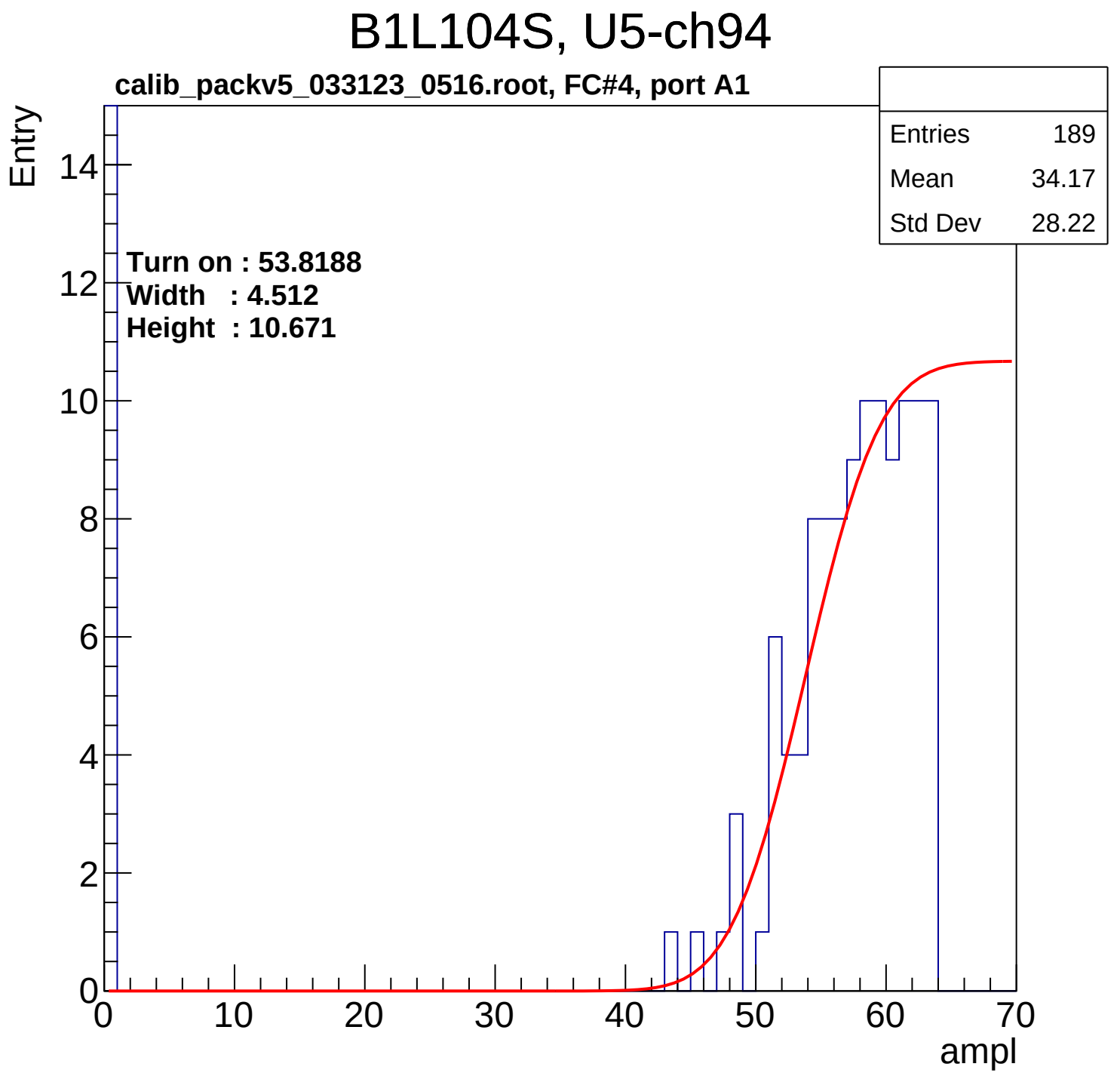

B1L104S, U5-ch89
calib_packv5_033123_0516.root, FC#4, port A1
Entries 193
Mean 29.4
Std Dev 29.08
Turn on : 55.2058
Width : 4.311
Height : 10.778
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

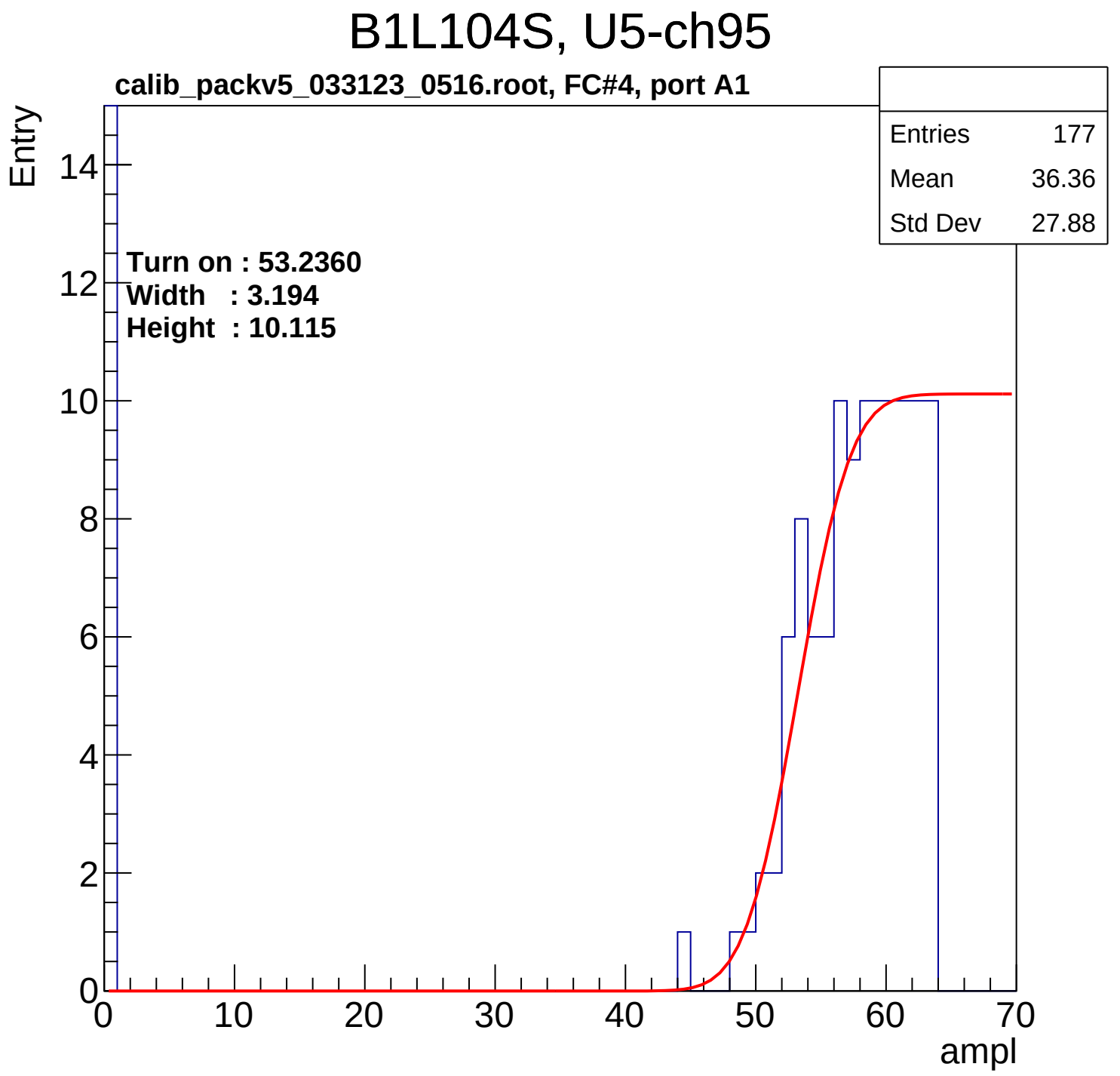

B1L104S, U5-ch90
calib_packv5_033123_0516.root, FC#4, port A1
Entries 183
Mean 33.55
Std Dev 28.46
Turn on : 52.3044
Width : 2.253
Height : 8.697
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

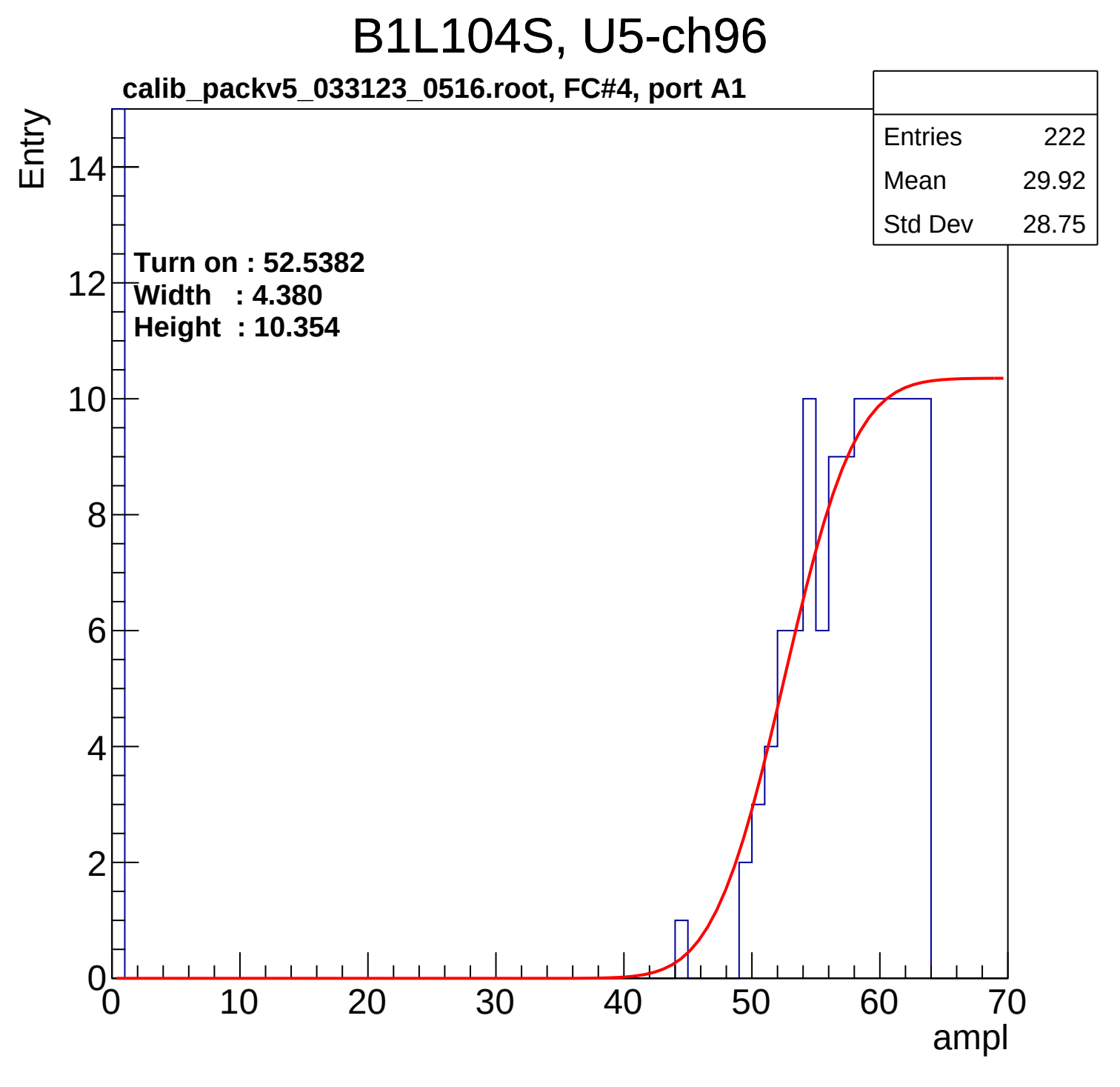

B1L104S, U5-ch91
calib_packv5_033123_0516.root, FC#4, port A1
Entries 199
Mean 35.22
Std Dev 27.88
Turn on : 52.1913
Width : 4.102
Height : 10.473
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

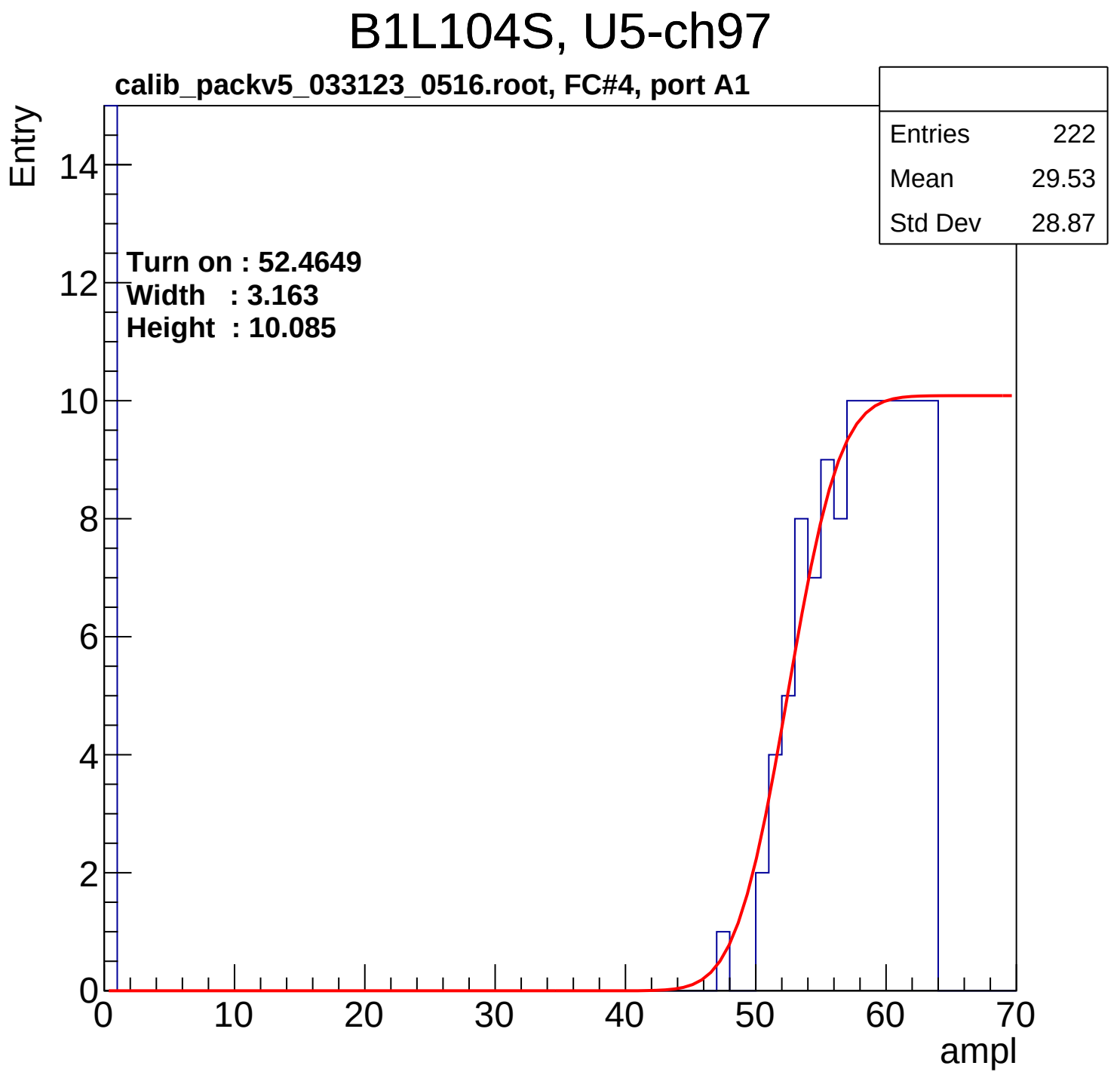

B1L104S, U5-ch92
calib_packv5_033123_0516.root, FC#4, port A1
Entries 212
Mean 30.74
Std Dev 28.67
Turn on : 53.6715
Width : 4.375
Height : 10.674
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

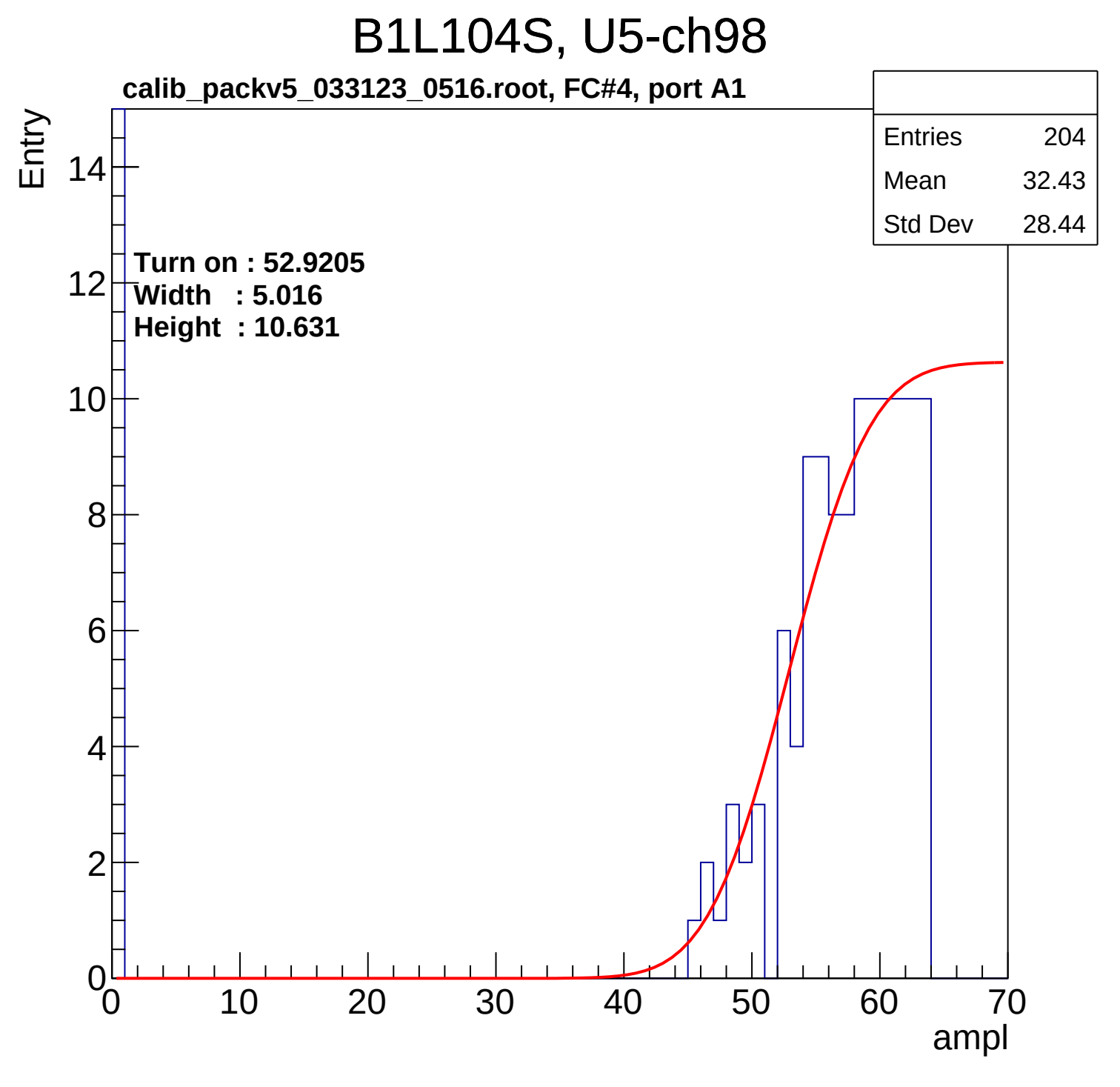

B1L104S, U5-ch93
calib_packv5_033123_0516.root, FC#4, port A1
Entries 159
Mean 34.08
Std Dev 28.85
Turn on : 55.8419
Width : 3.839
Height : 10.778
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

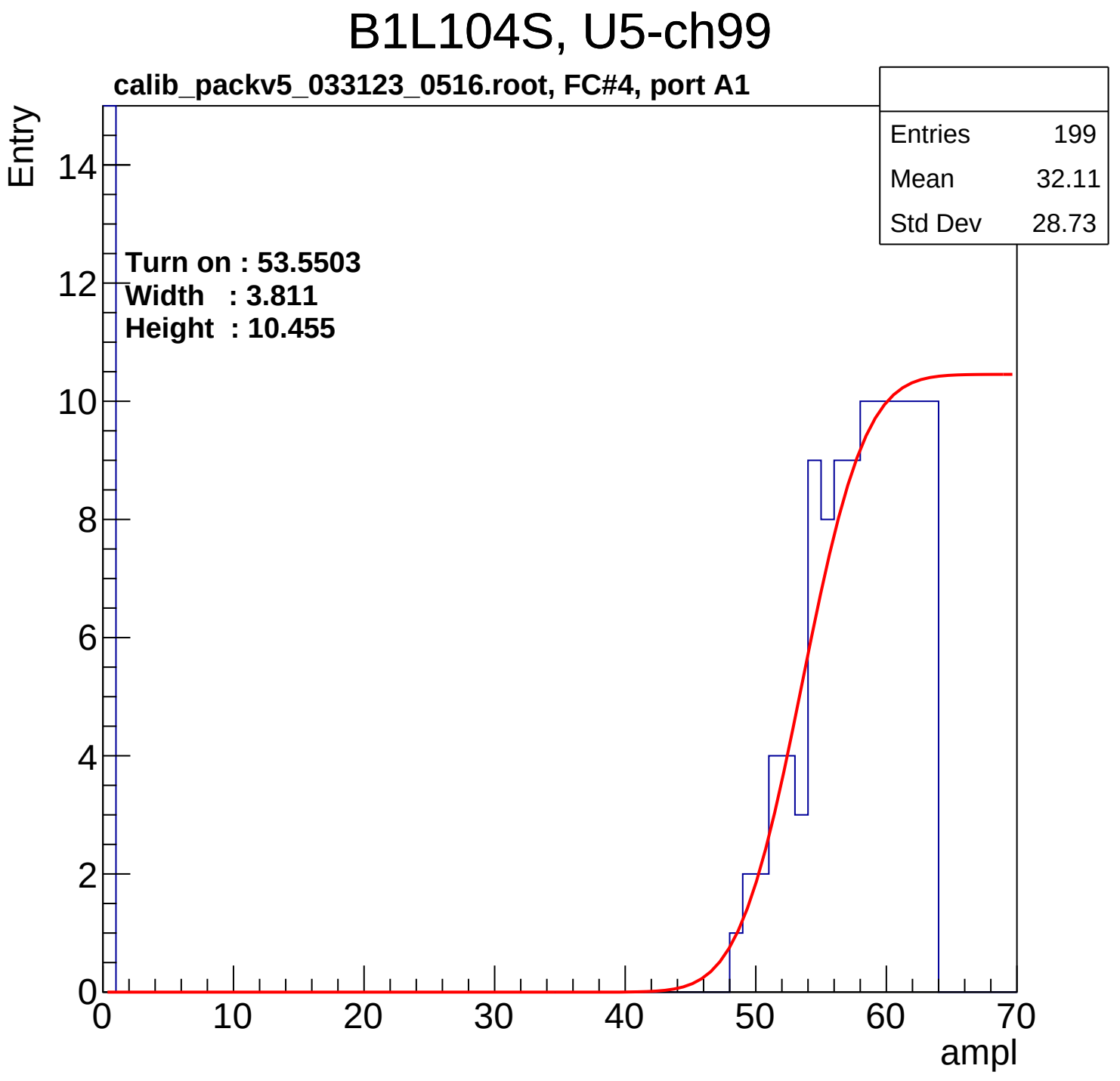

B1L104S, U5-ch94
calib_packv5_033123_0516.root, FC#4, port A1
Entries 189
Mean 34.17
Std Dev 28.22
Turn on : 53.8188
Width : 4.512
Height : 10.671
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

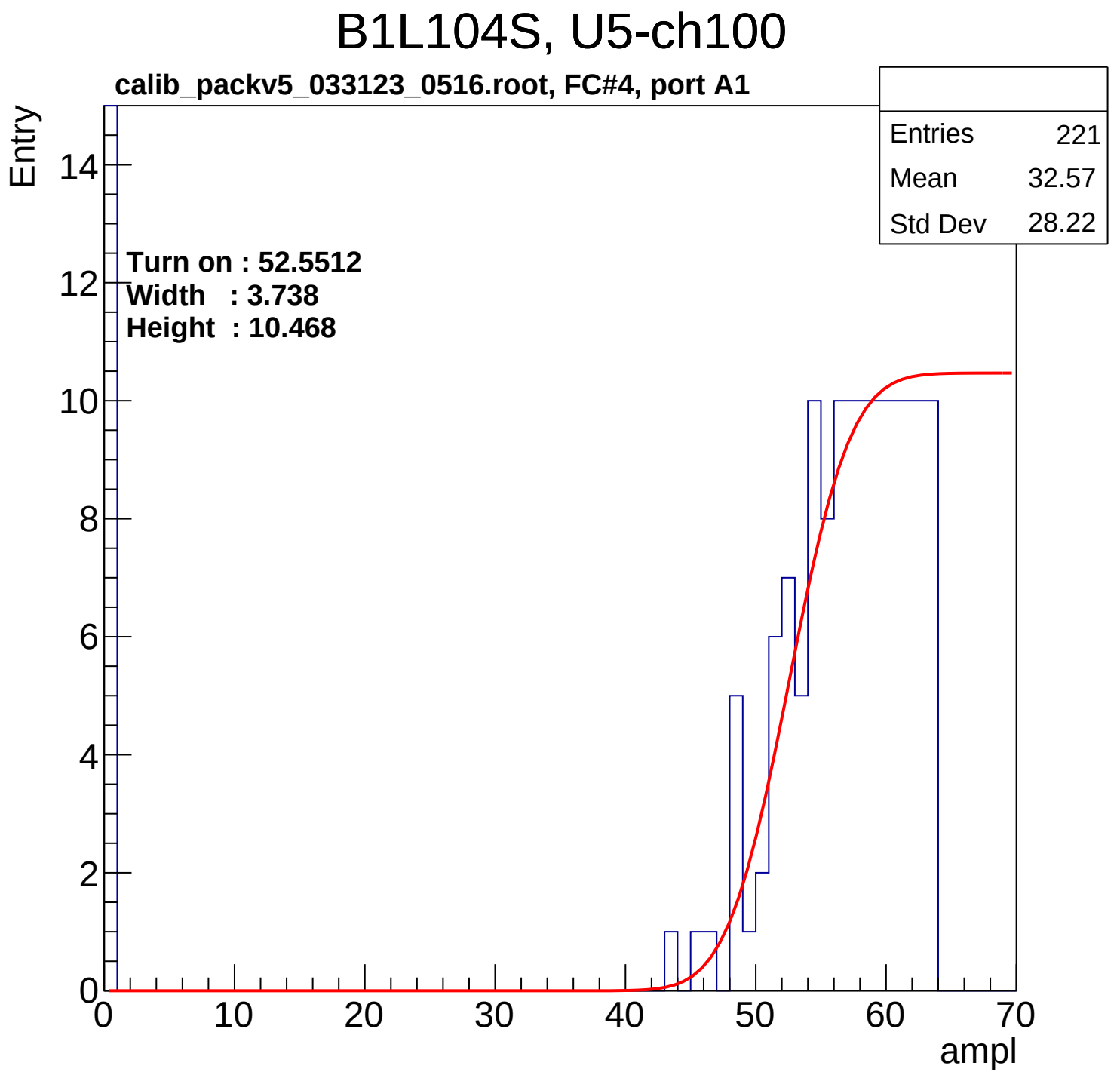

B1L104S, U5-ch95
calib_packv5_033123_0516.root, FC#4, port A1
Entries 177
Mean 36.36
Std Dev 27.88
Turn on : 53.2360
Width : 3.194
Height : 10.115
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

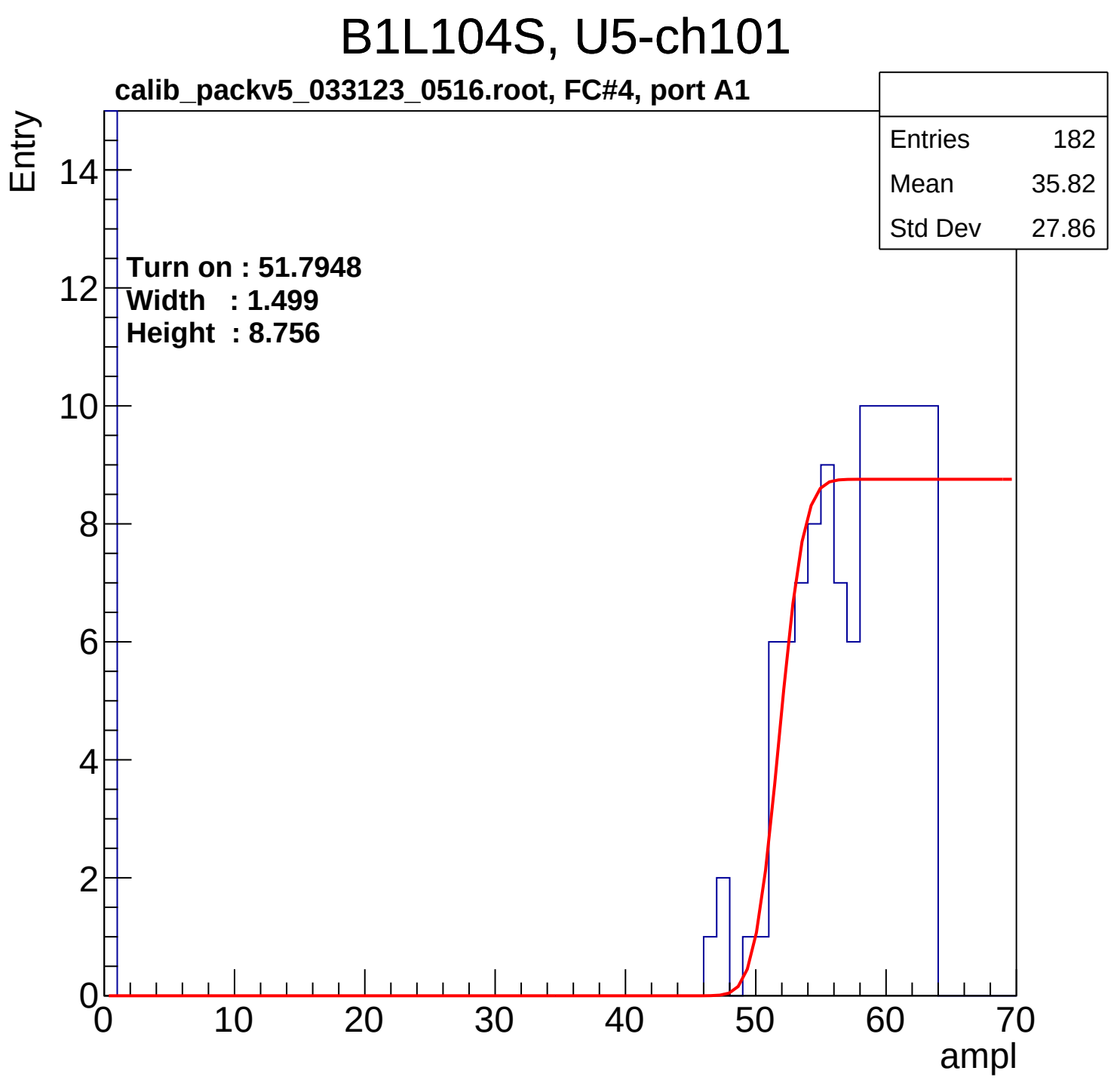

B1L104S, U5-ch96
calib_packv5_033123_0516.root, FC#4, port A1
Entries 222
Mean 29.92
Std Dev 28.75
Turn on : 52.5382
Width : 4.380
Height : 10.354
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

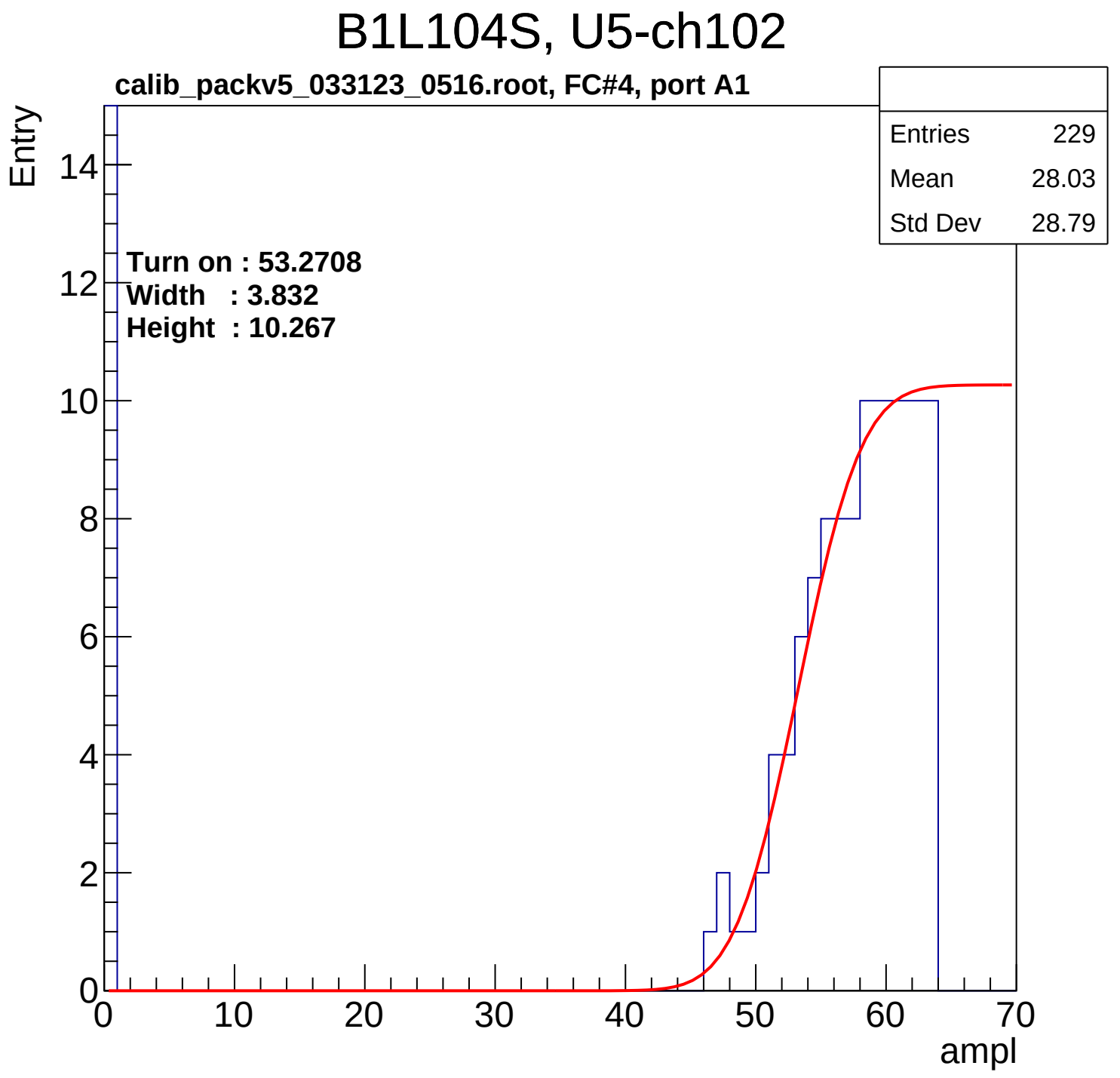

B1L104S, U5-ch97
calib_packv5_033123_0516.root, FC#4, port A1
Entries 222
Mean 29.53
Std Dev 28.87
Turn on : 52.4649
Width : 3.163
Height : 10.085
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

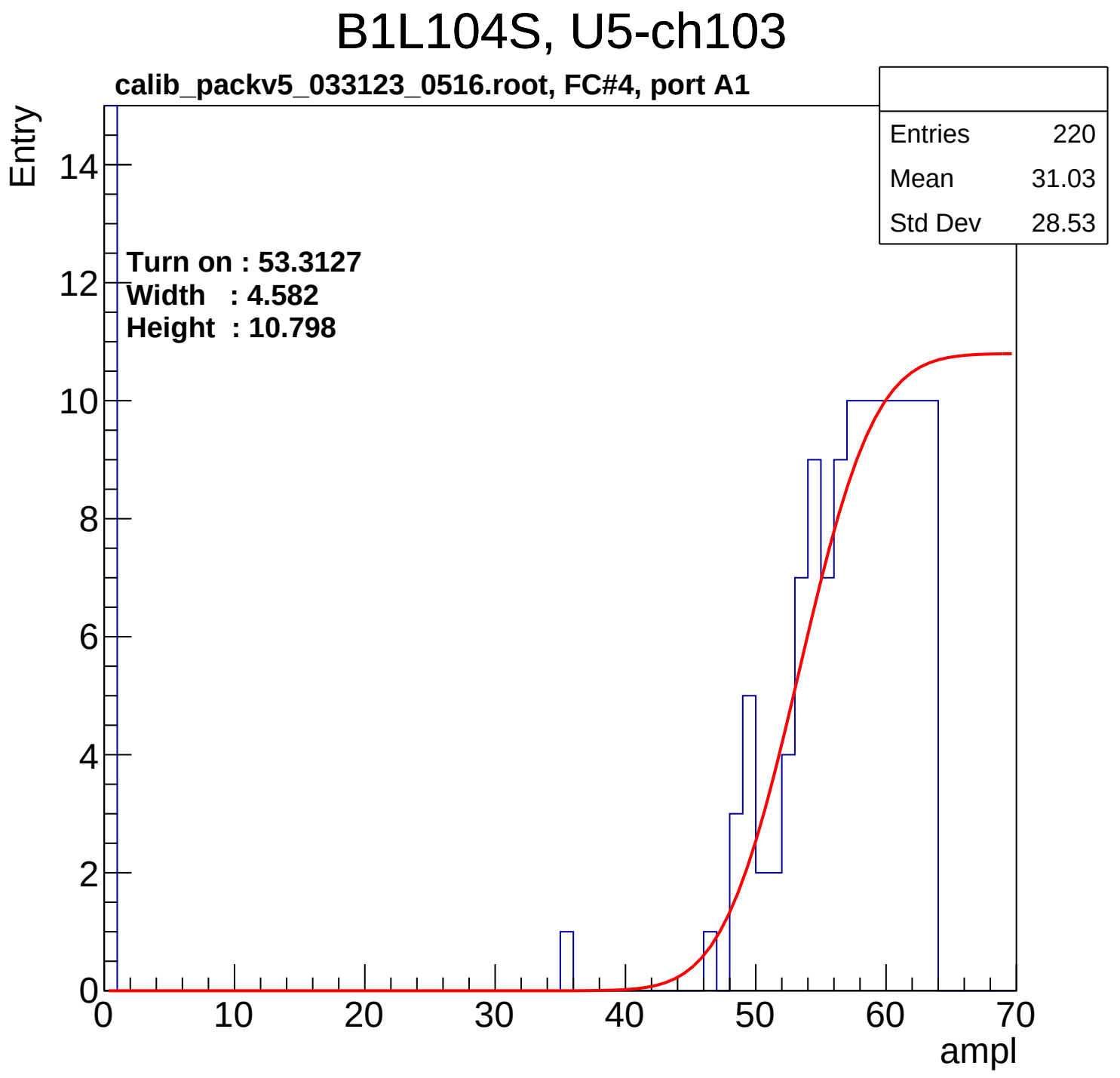

B1L104S, U5-ch98
calib_packv5_033123_0516.root, FC#4, port A1
Entries 204
Mean 32.43
Std Dev 28.44
Turn on : 52.9205
Width : 5.016
Height : 10.631
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

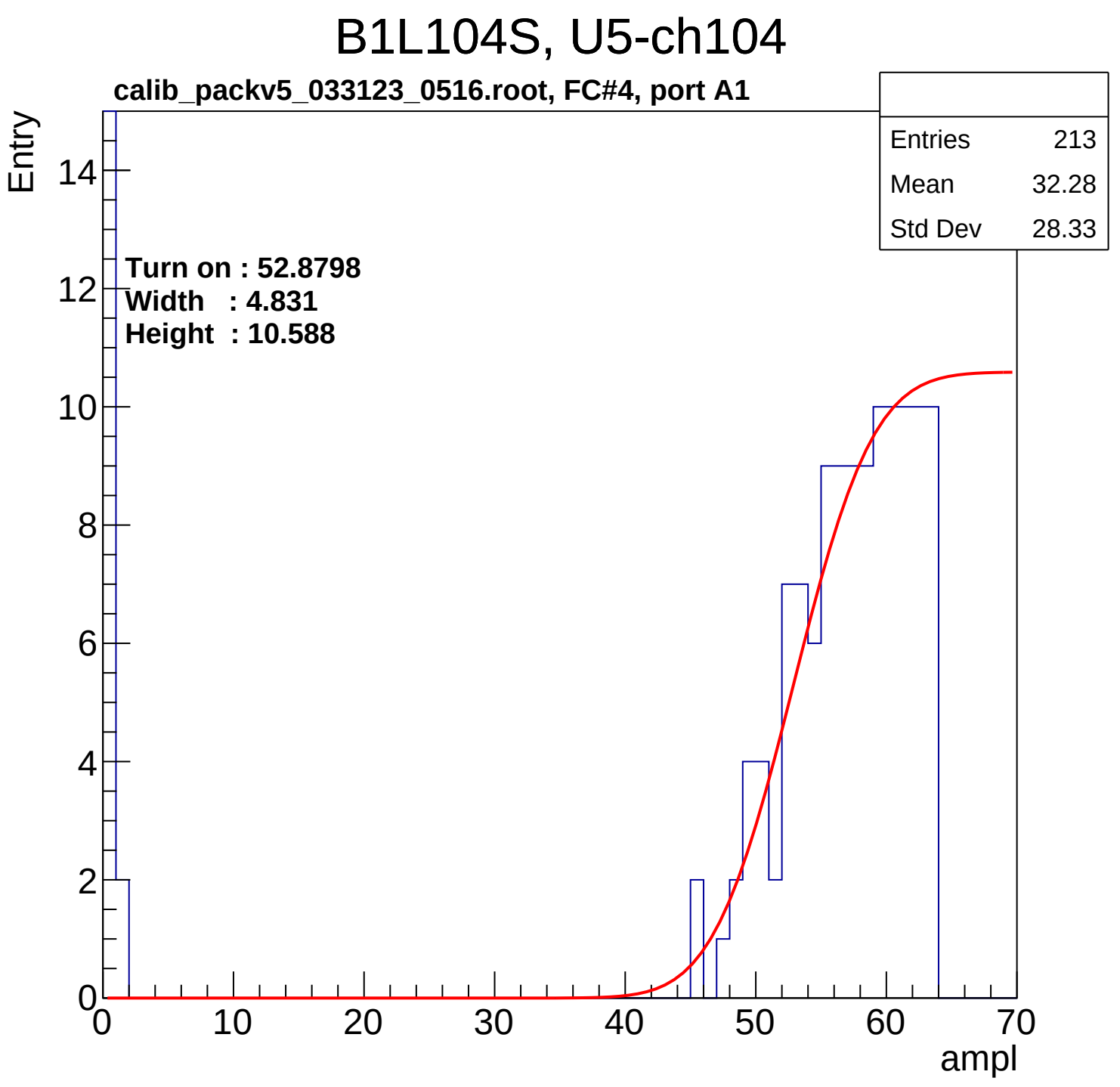

B1L104S, U5-ch99
calib_packv5_033123_0516.root, FC#4, port A1
Entries 199
Mean 32.11
Std Dev 28.73
Turn on : 53.5503
Width : 3.811
Height : 10.455
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

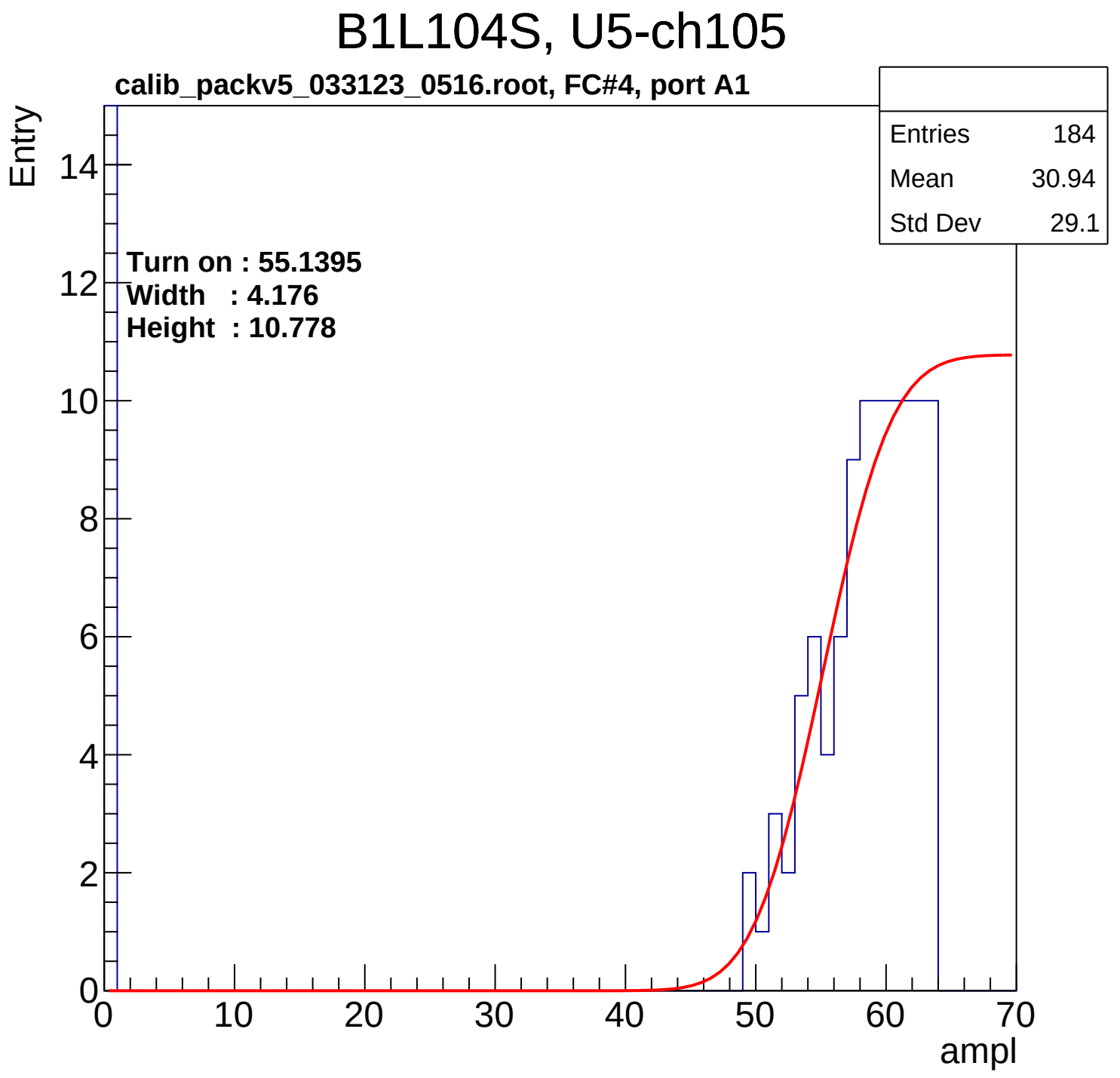

B1L104S, U5-ch100
calib_packv5_033123_0516.root, FC#4, port A1
Entries 221
Mean 32.57
Std Dev 28.22
Turn on : 52.5512
Width : 3.738
Height : 10.468
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

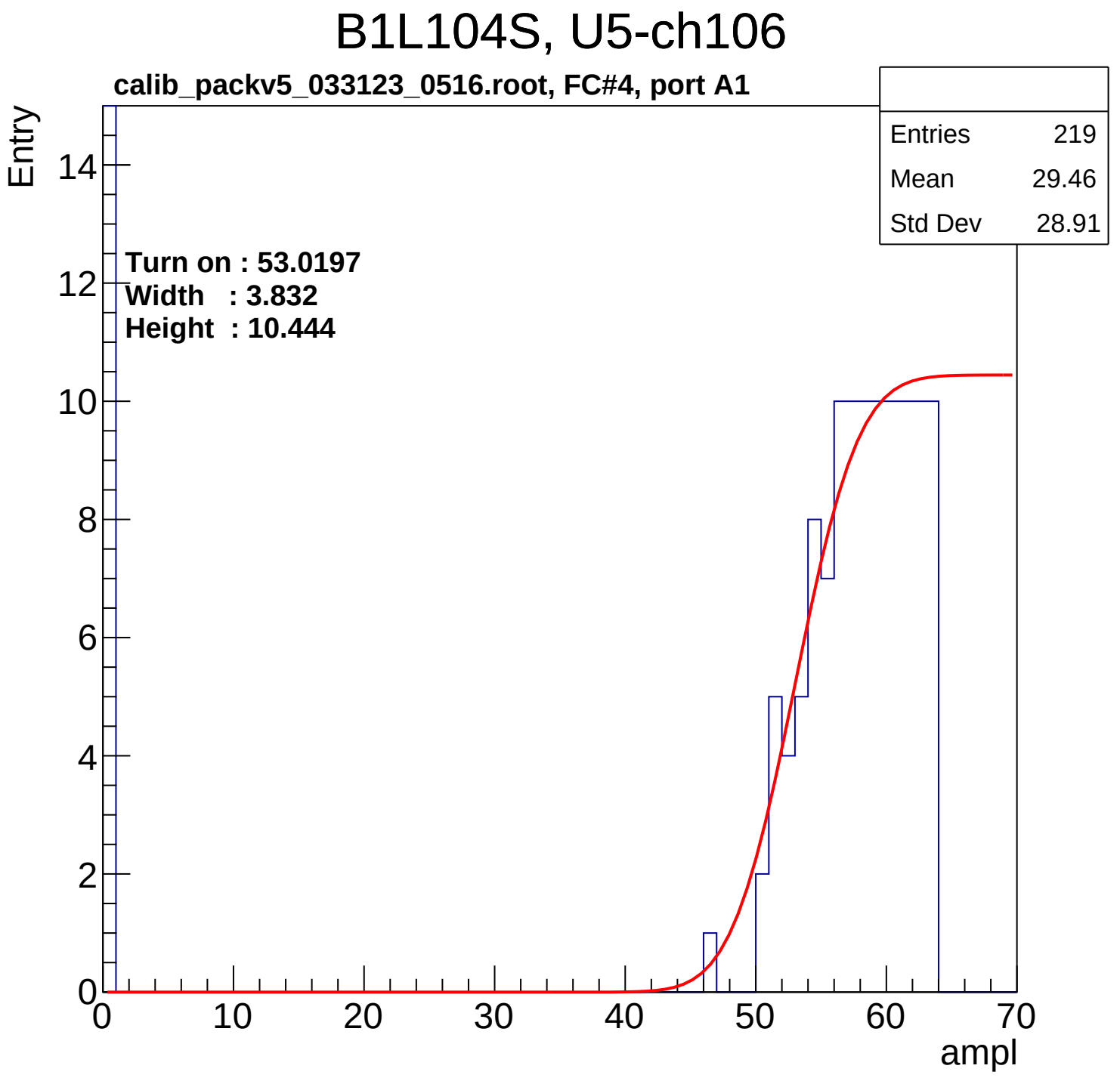

B1L104S, U5-ch101
calib_packv5_033123_0516.root, FC#4, port A1
Entries 182
Mean 35.82
Std Dev 27.86
Turn on : 51.7948
Width : 1.499
Height : 8.756
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

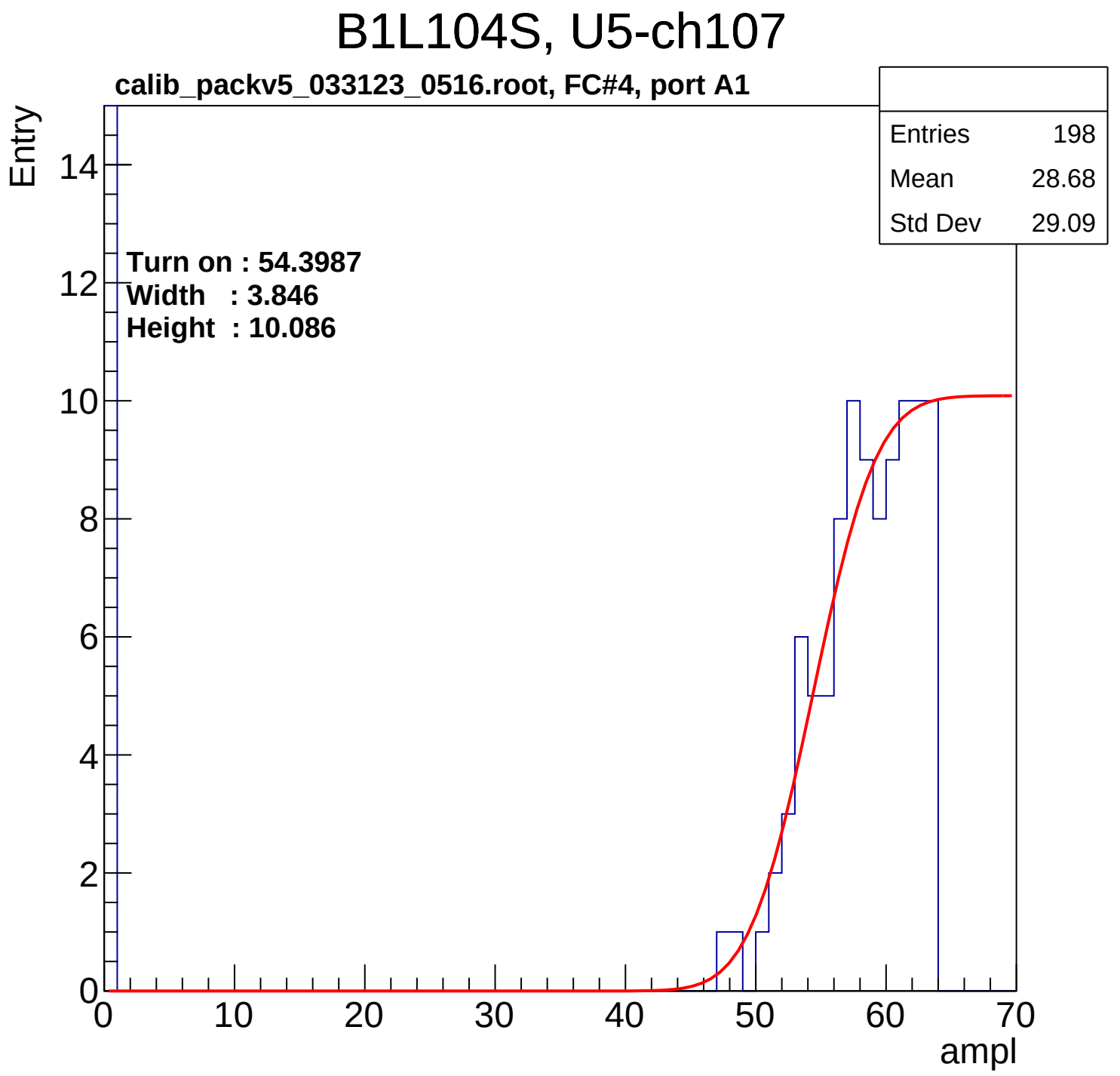

B1L104S, U5-ch102
calib_packv5_033123_0516.root, FC#4, port A1
Entries 229
Mean 28.03
Std Dev 28.79
Turn on : 53.2708
Width : 3.832
Height : 10.267
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

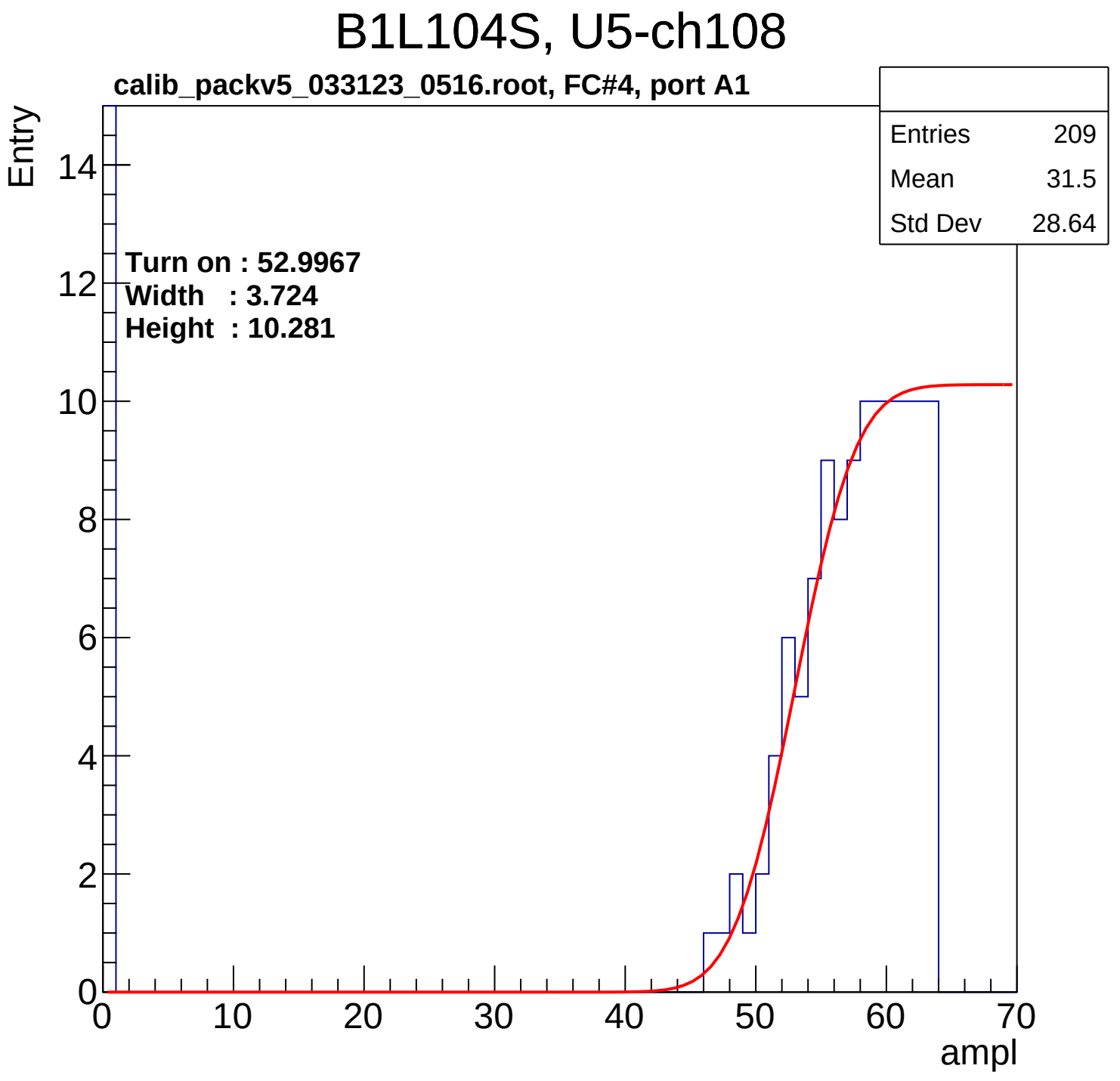

B1L104S, U5-ch103
calib_packv5_033123_0516.root, FC#4, port A1
Entries 220
Mean 31.03
Std Dev 28.53
Turn on : 53.3127
Width : 4.582
Height : 10.798
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

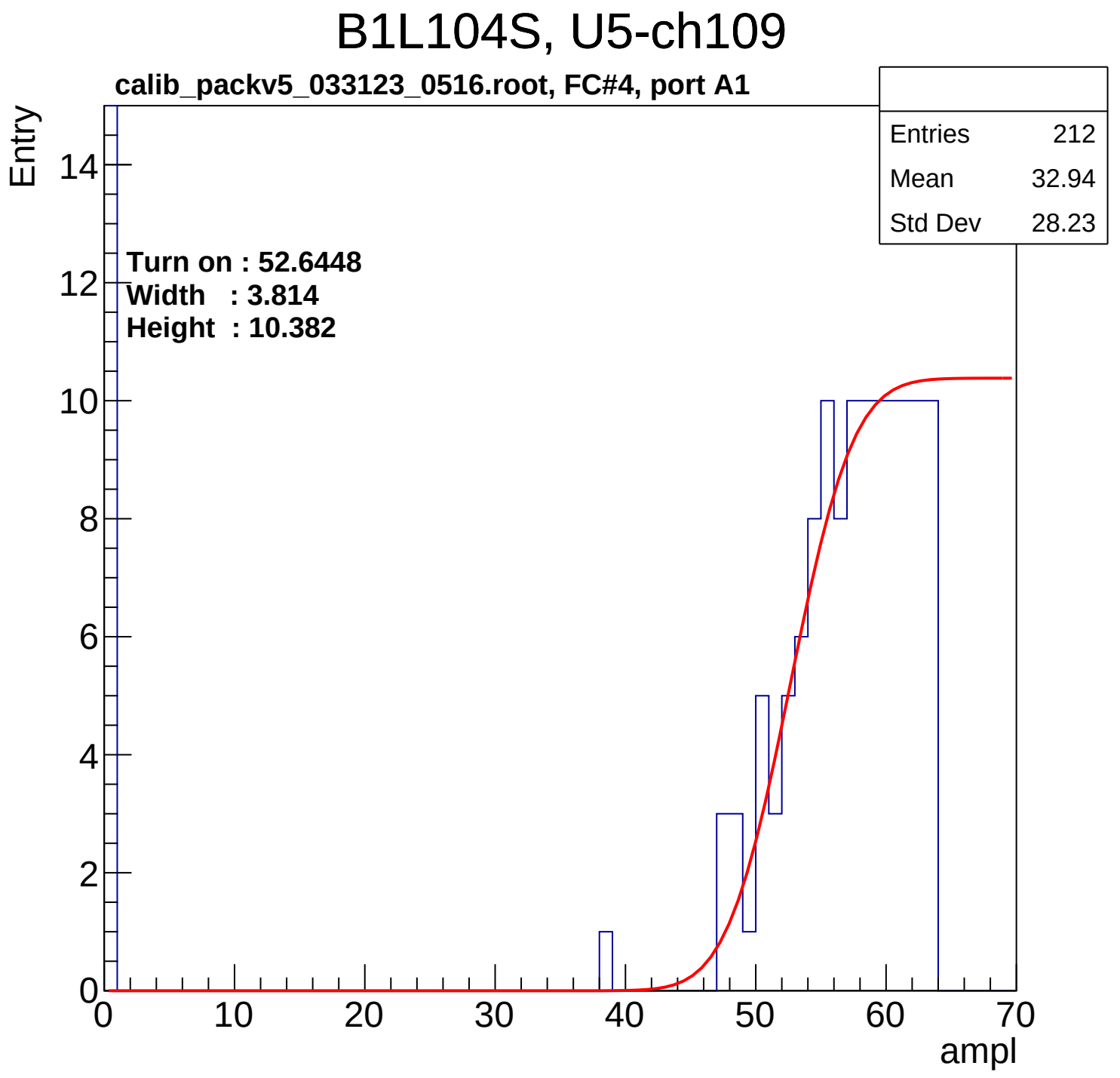

B1L104S, U5-ch104
calib_packv5_033123_0516.root, FC#4, port A1
Entries 213
Mean 32.28
Std Dev 28.33
Turn on : 52.8798
Width : 4.831
Height : 10.588
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

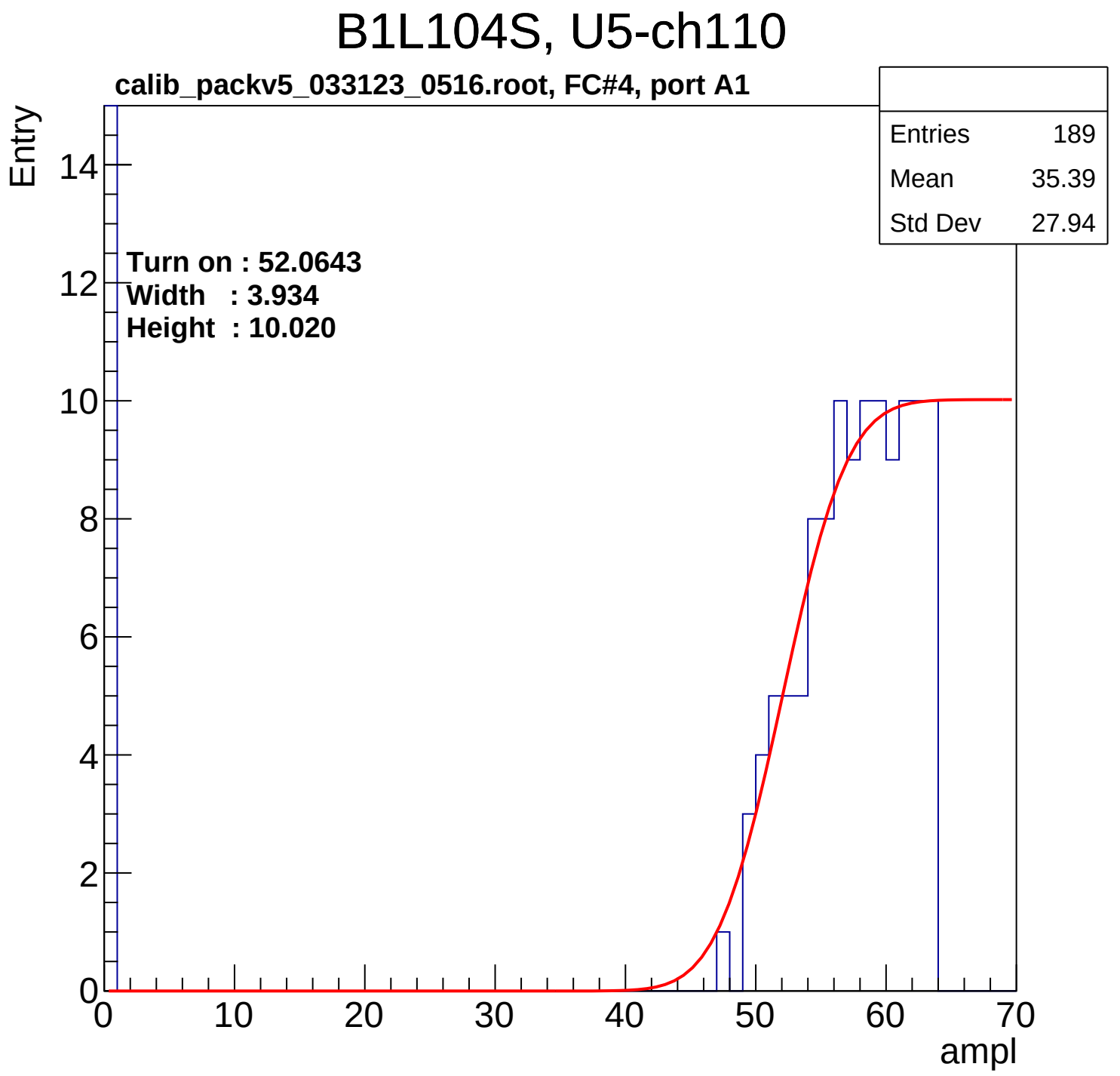

B1L104S, U5-ch105
calib_packv5_033123_0516.root, FC#4, port A1
Entries 184
Mean 30.94
Std Dev 29.1
Turn on : 55.1395
Width : 4.176
Height : 10.778
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

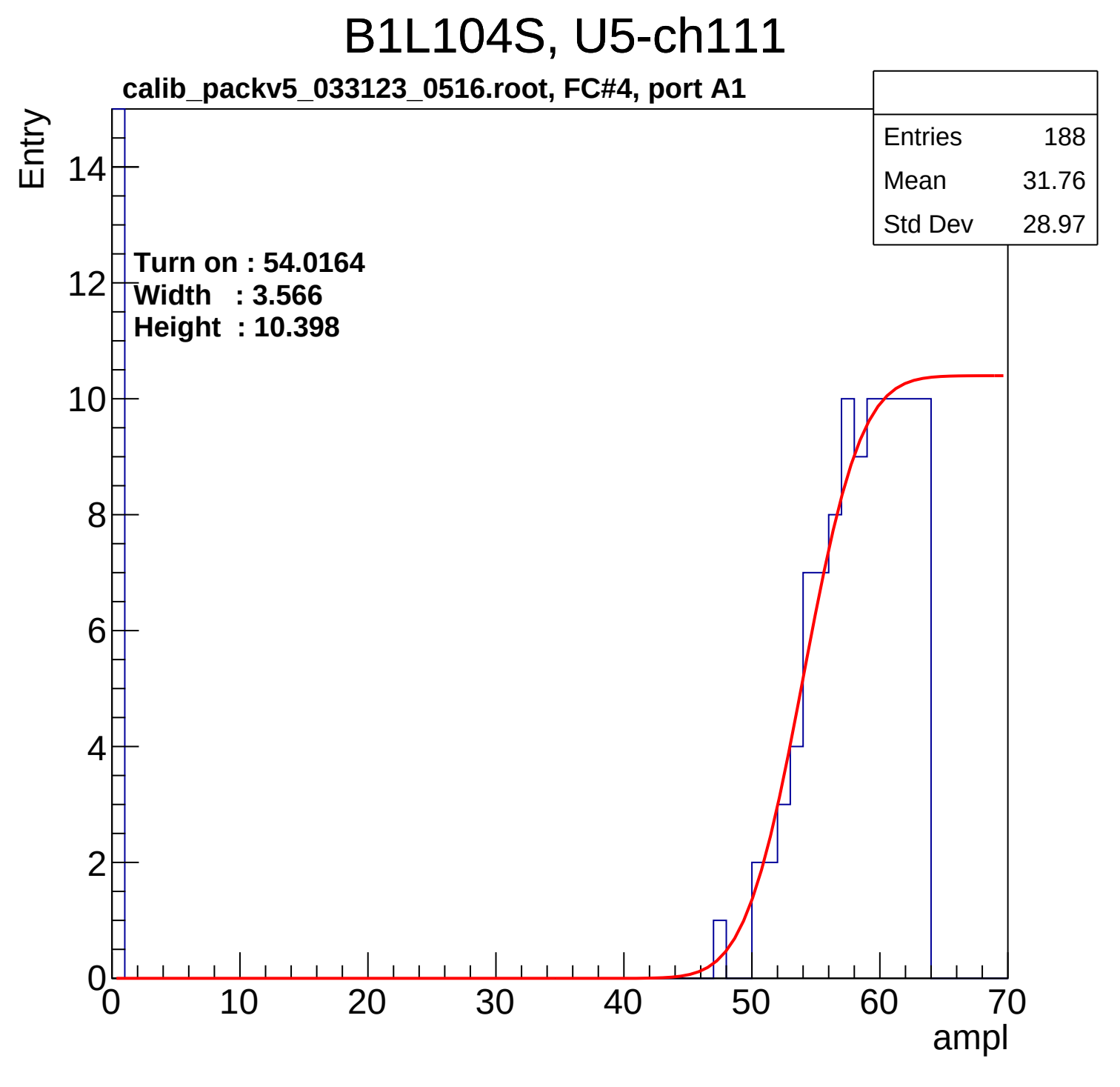

B1L104S, U5-ch106
calib_packv5_033123_0516.root, FC#4, port A1
Entries 219
Mean 29.46
Std Dev 28.91
Turn on : 53.0197
Width : 3.832
Height : 10.444
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

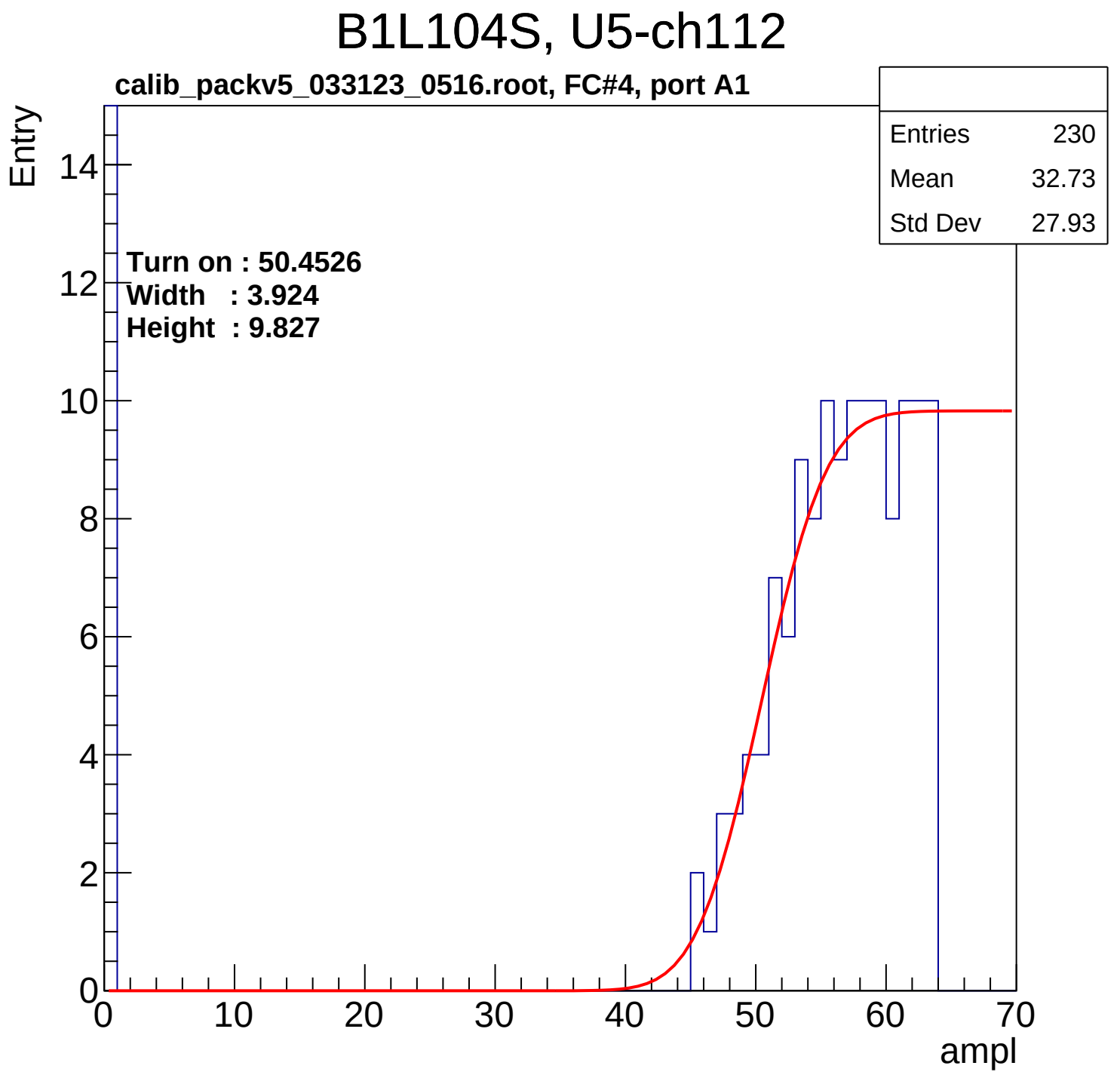

B1L104S, U5-ch107
calib_packv5_033123_0516.root, FC#4, port A1
Entries 198
Mean 28.68
Std Dev 29.09
Turn on : 54.3987
Width : 3.846
Height : 10.086
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

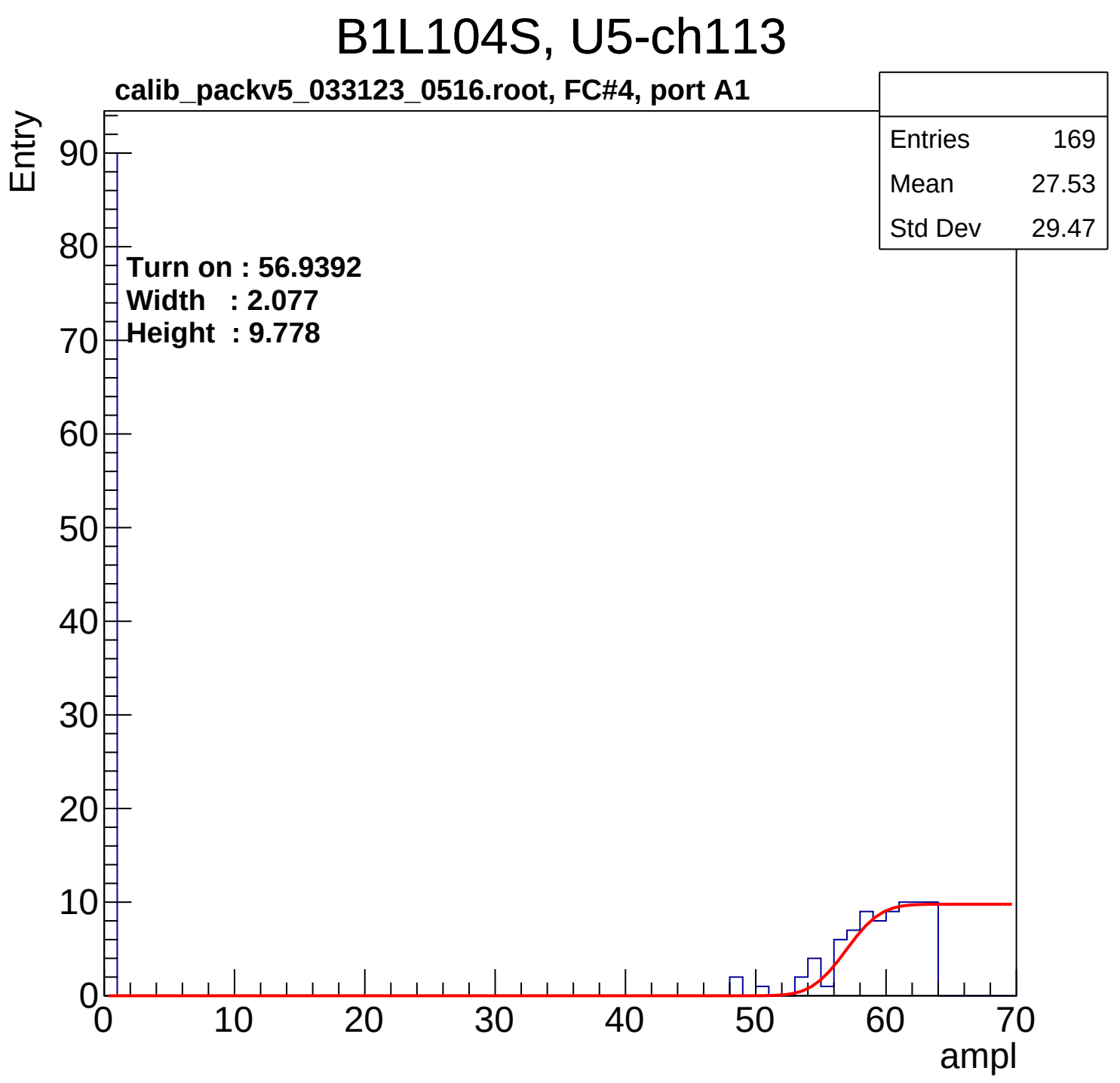

B1L104S, U5-ch108
calib_packv5_033123_0516.root, FC#4, port A1
Entries 209
Mean 31.5
Std Dev 28.64
Turn on : 52.9967
Width : 3.724
Height : 10.281
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

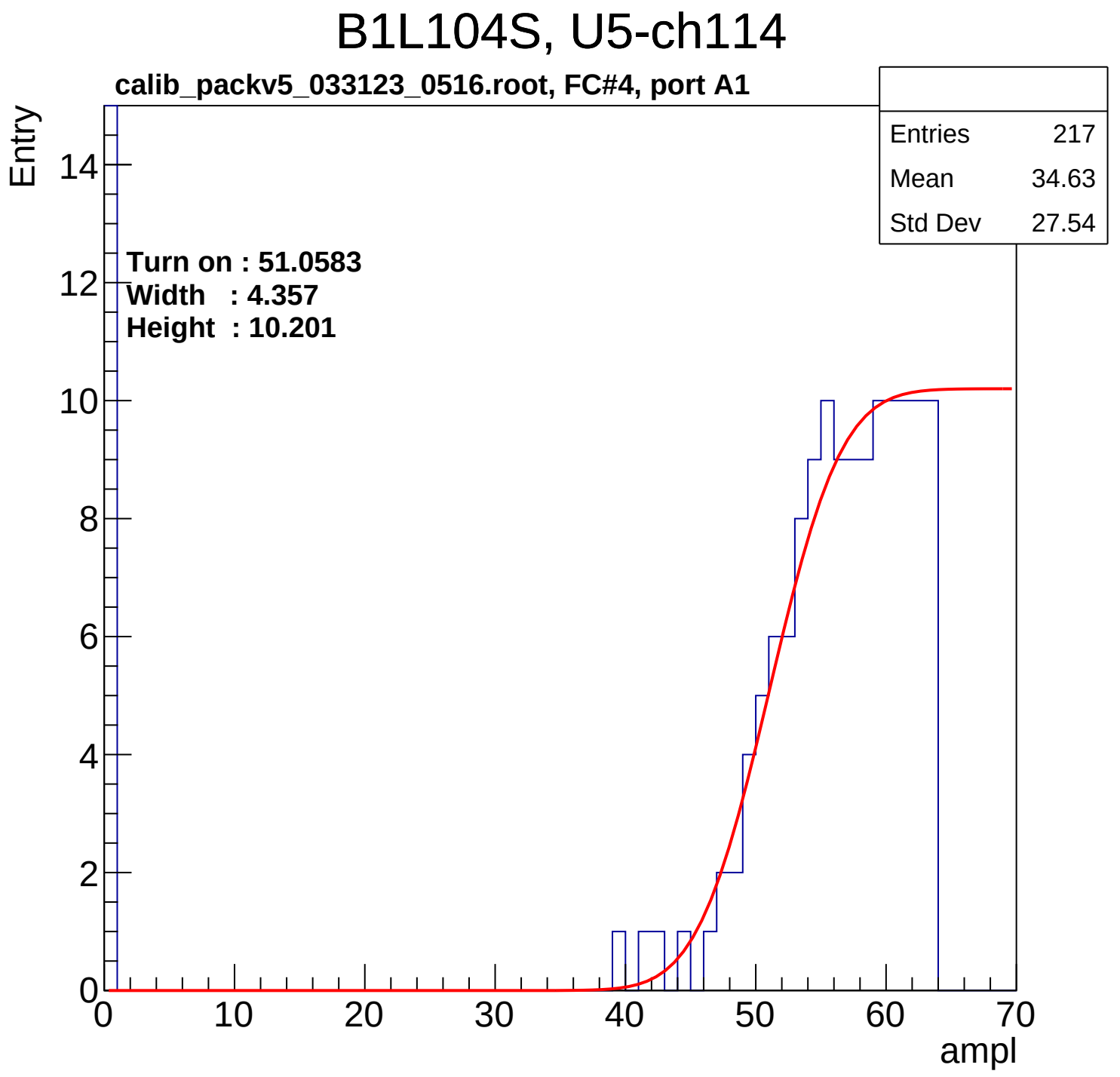

B1L104S, U5-ch109
calib_packv5_033123_0516.root, FC#4, port A1
Entries 212
Mean 32.94
Std Dev 28.23
Turn on : 52.6448
Width : 3.814
Height : 10.382
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

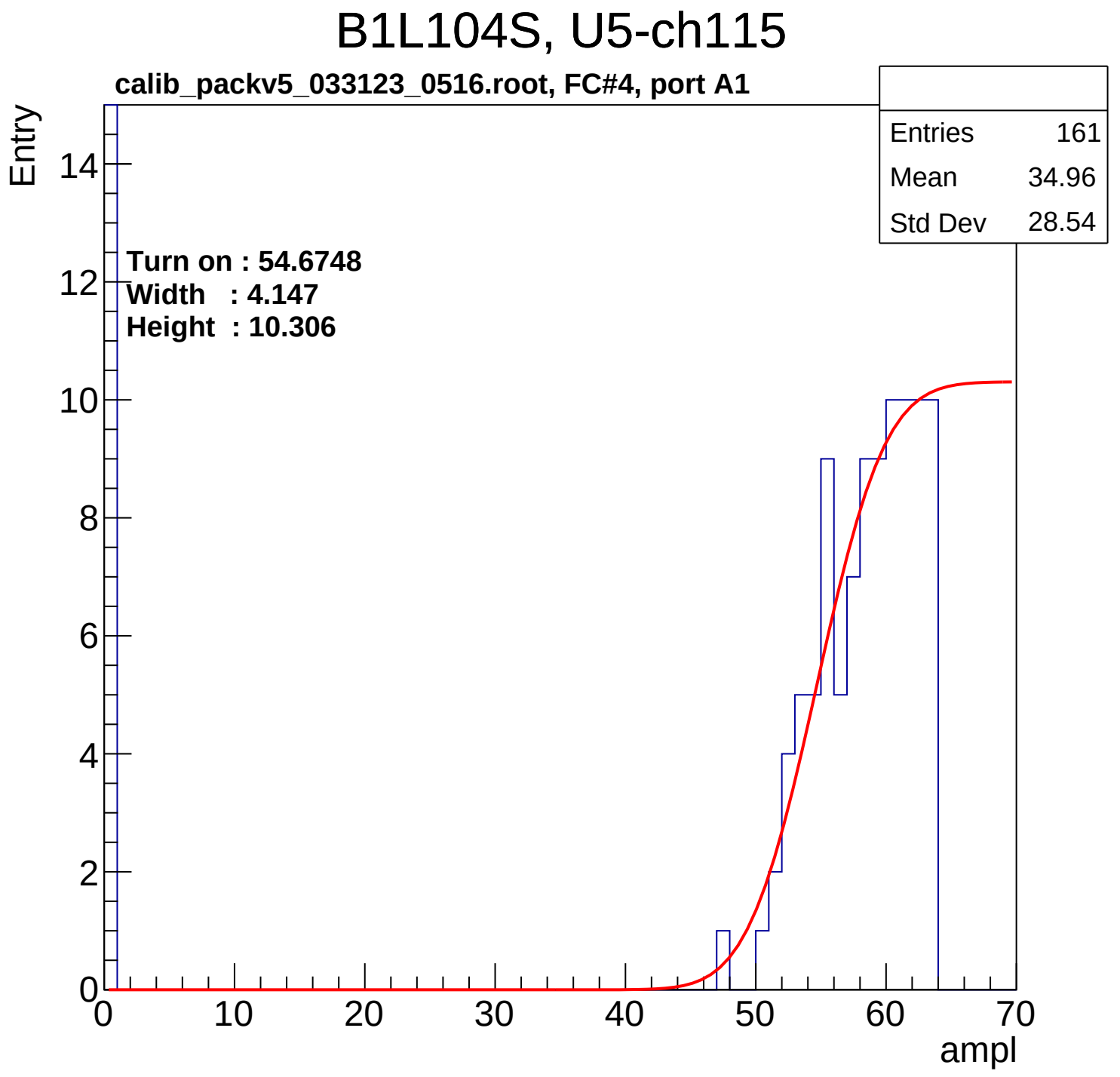

B1L104S, U5-ch110
calib_packv5_033123_0516.root, FC#4, port A1
Entries 189
Mean 35.39
Std Dev 27.94
Turn on : 52.0643
Width : 3.934
Height : 10.020
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

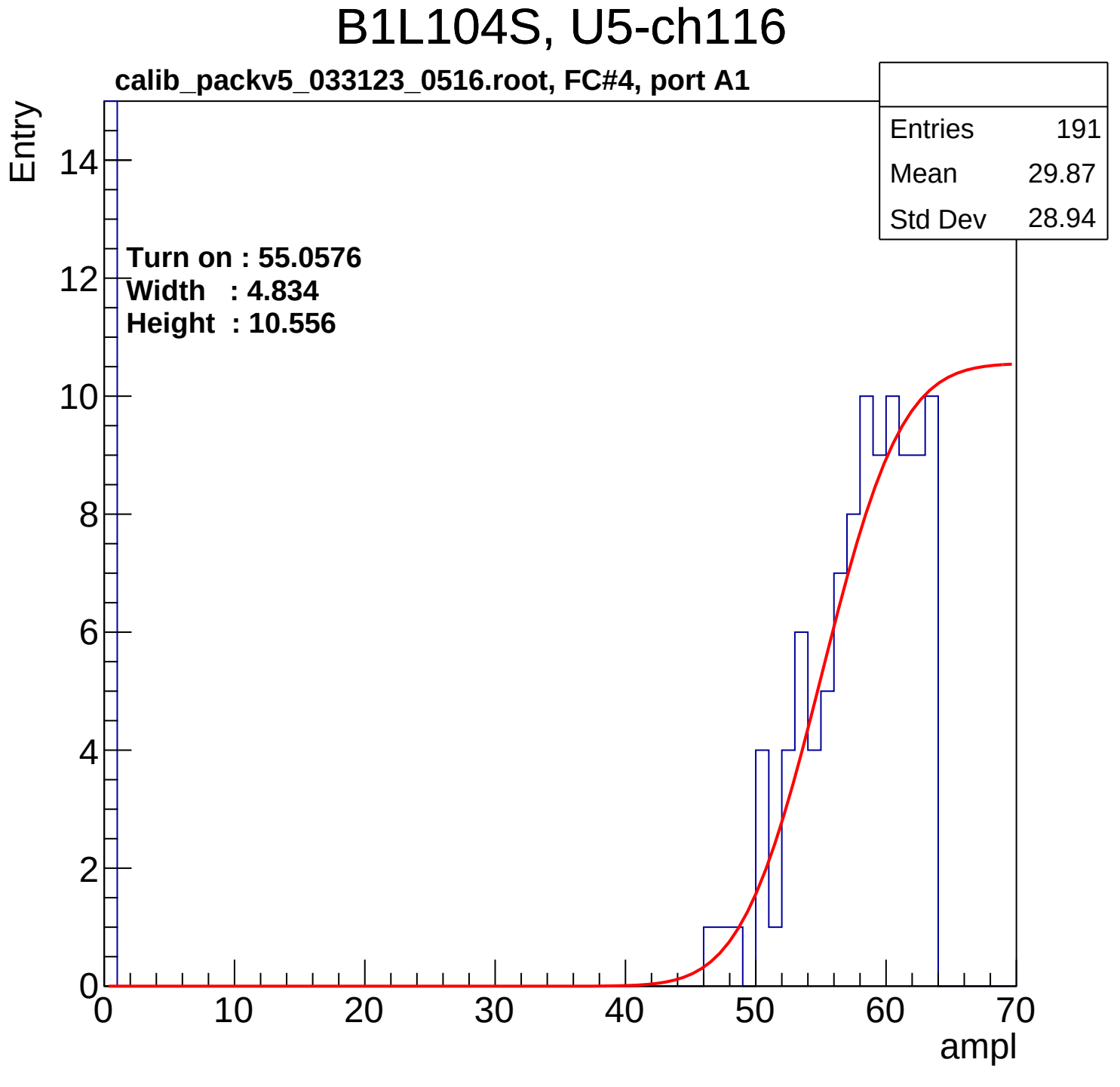

B1L104S, U5-ch111
calib_packv5_033123_0516.root, FC#4, port A1
Entries 188
Mean 31.76
Std Dev 28.97
Turn on : 54.0164
Width : 3.566
Height : 10.398
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

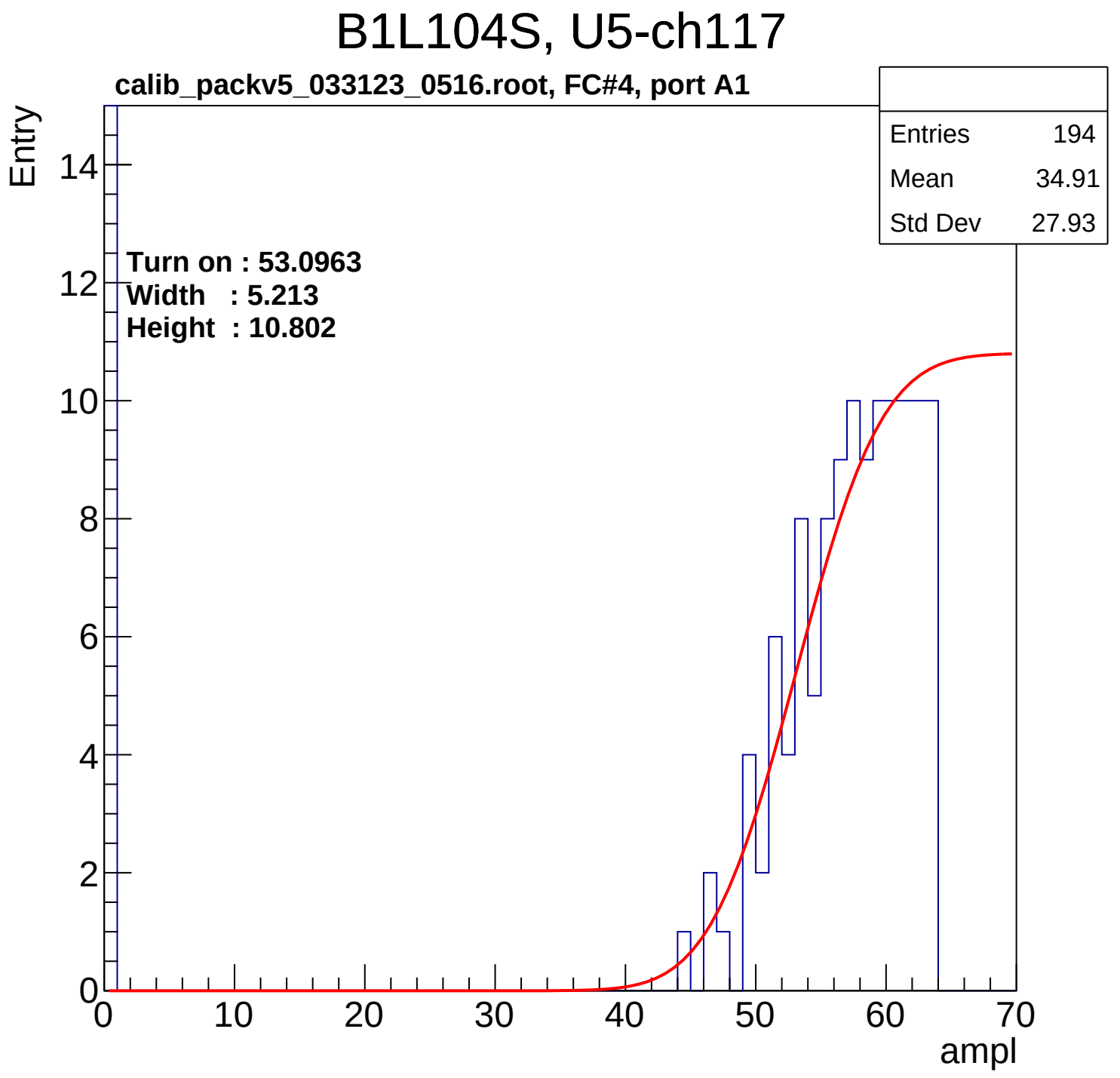

B1L104S, U5-ch112
calib_packv5_033123_0516.root, FC#4, port A1
Entries 230
Mean 32.73
Std Dev 27.93
Turn on : 50.4526
Width : 3.924
Height : 9.827
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

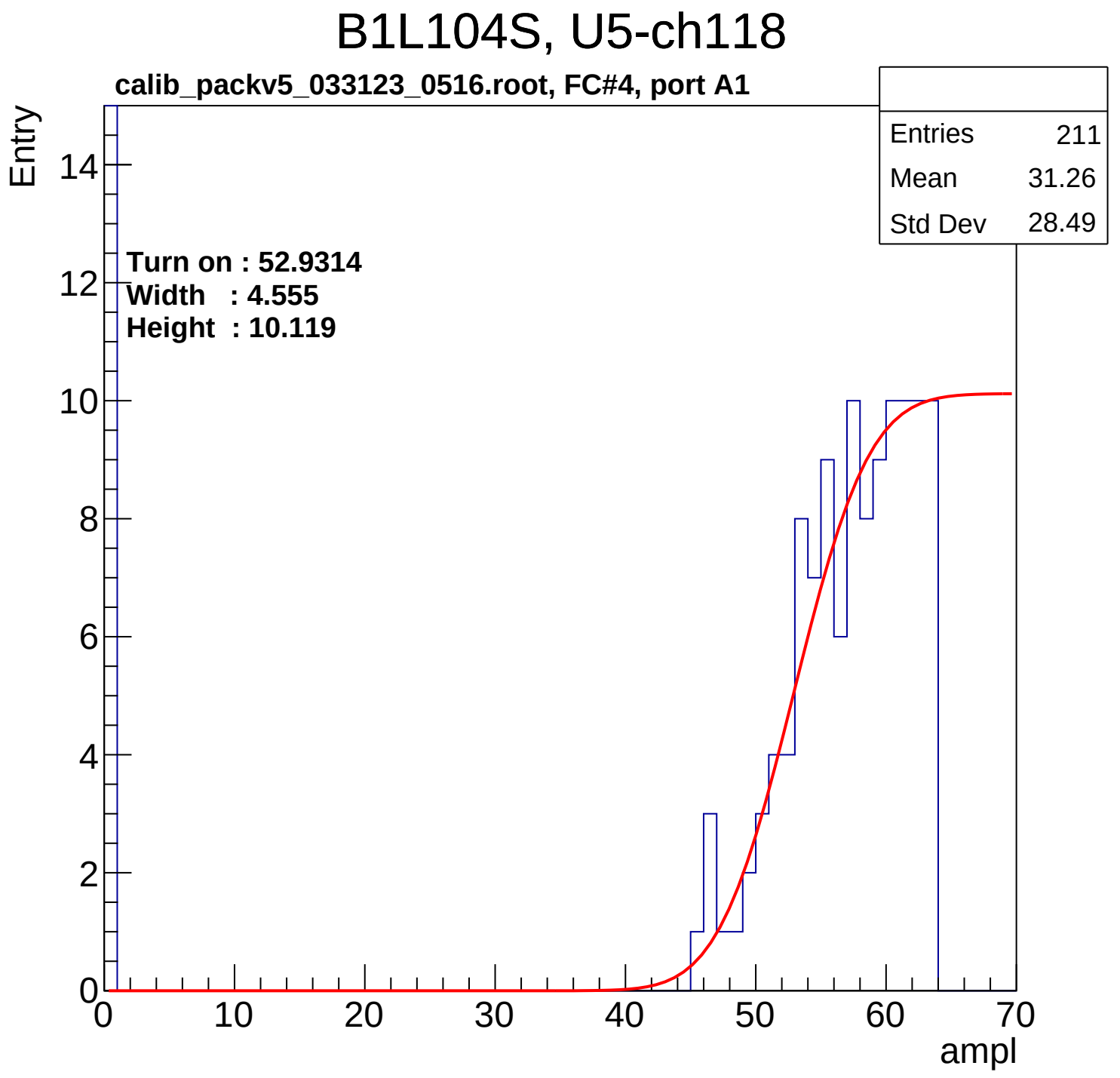

B1L104S, U5-ch113
calib_packv5_033123_0516.root, FC#4, port A1
Entries 169
Mean 27.53
Std Dev 29.47
Turn on : 56.9392
Width : 2.077
Height : 9.778
Entry
ampl
0
10
20
30
40
50
60
70
80
90

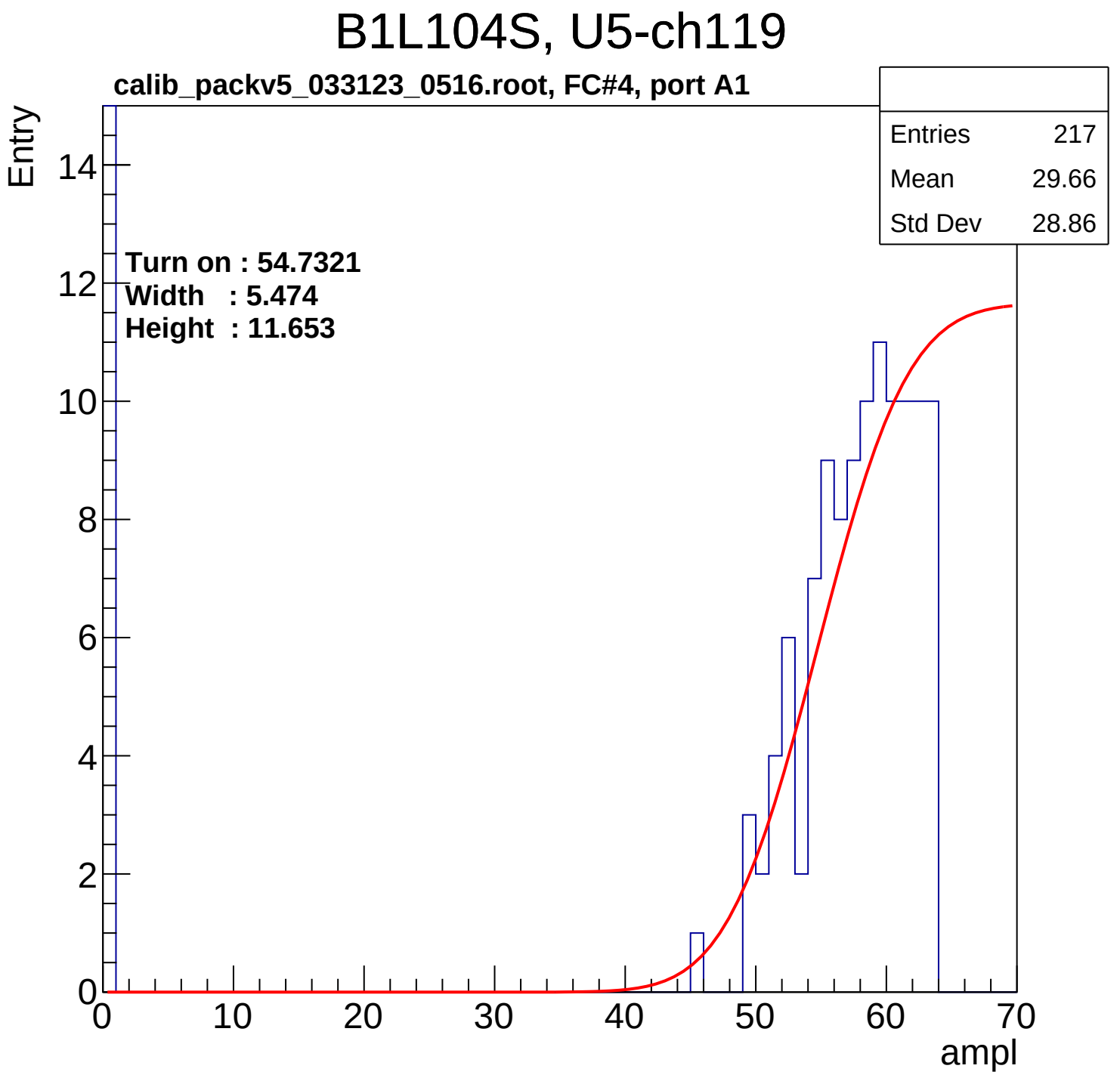

B1L104S, U5-ch114
calib_packv5_033123_0516.root, FC#4, port A1
Entries 217
Mean 34.63
Std Dev 27.54
Turn on : 51.0583
Width : 4.357
Height : 10.201
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

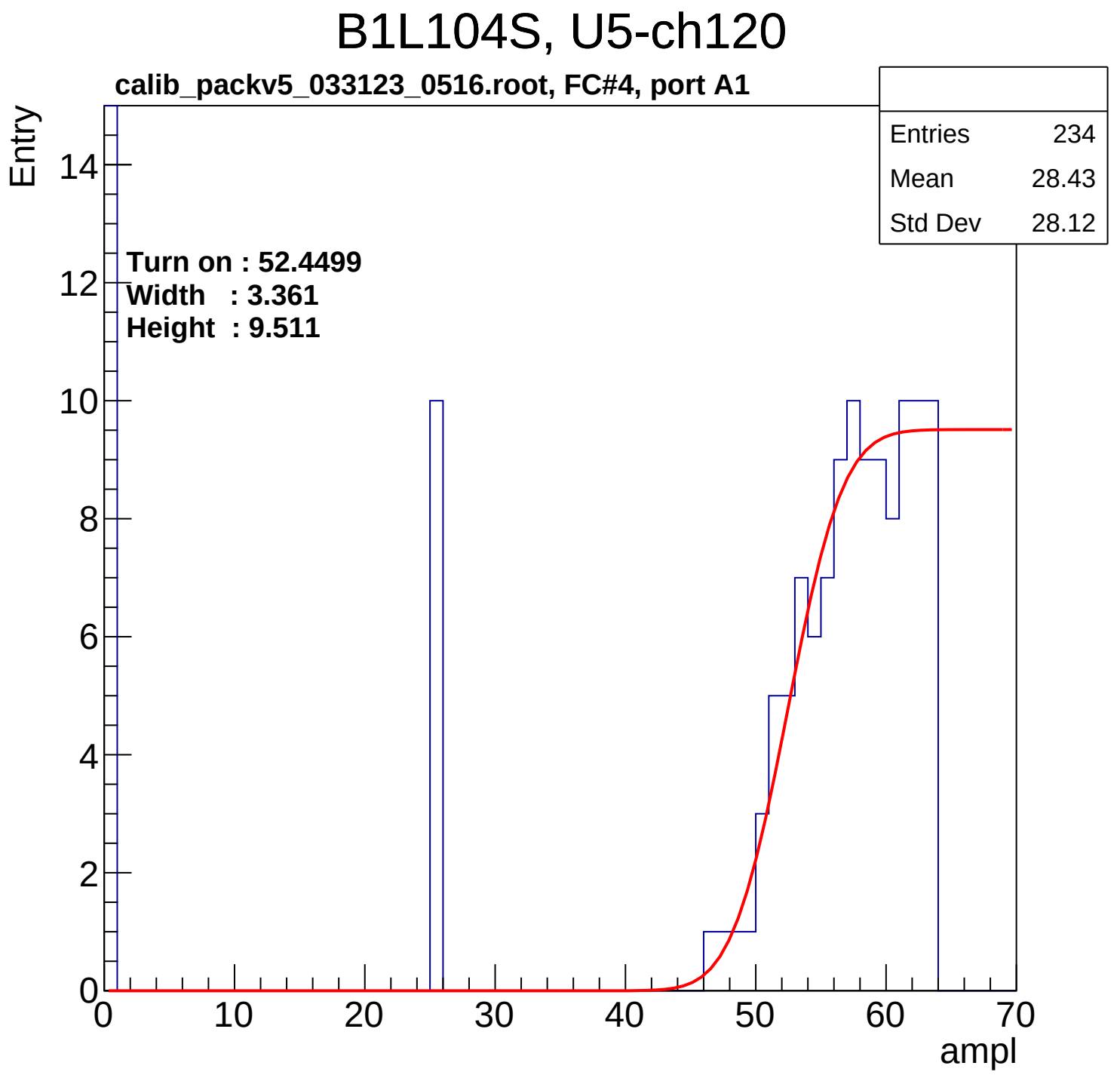

B1L104S, U5-ch115
calib_packv5_033123_0516.root, FC#4, port A1
Entries 161
Mean 34.96
Std Dev 28.54
Turn on : 54.6748
Width : 4.147
Height : 10.306
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

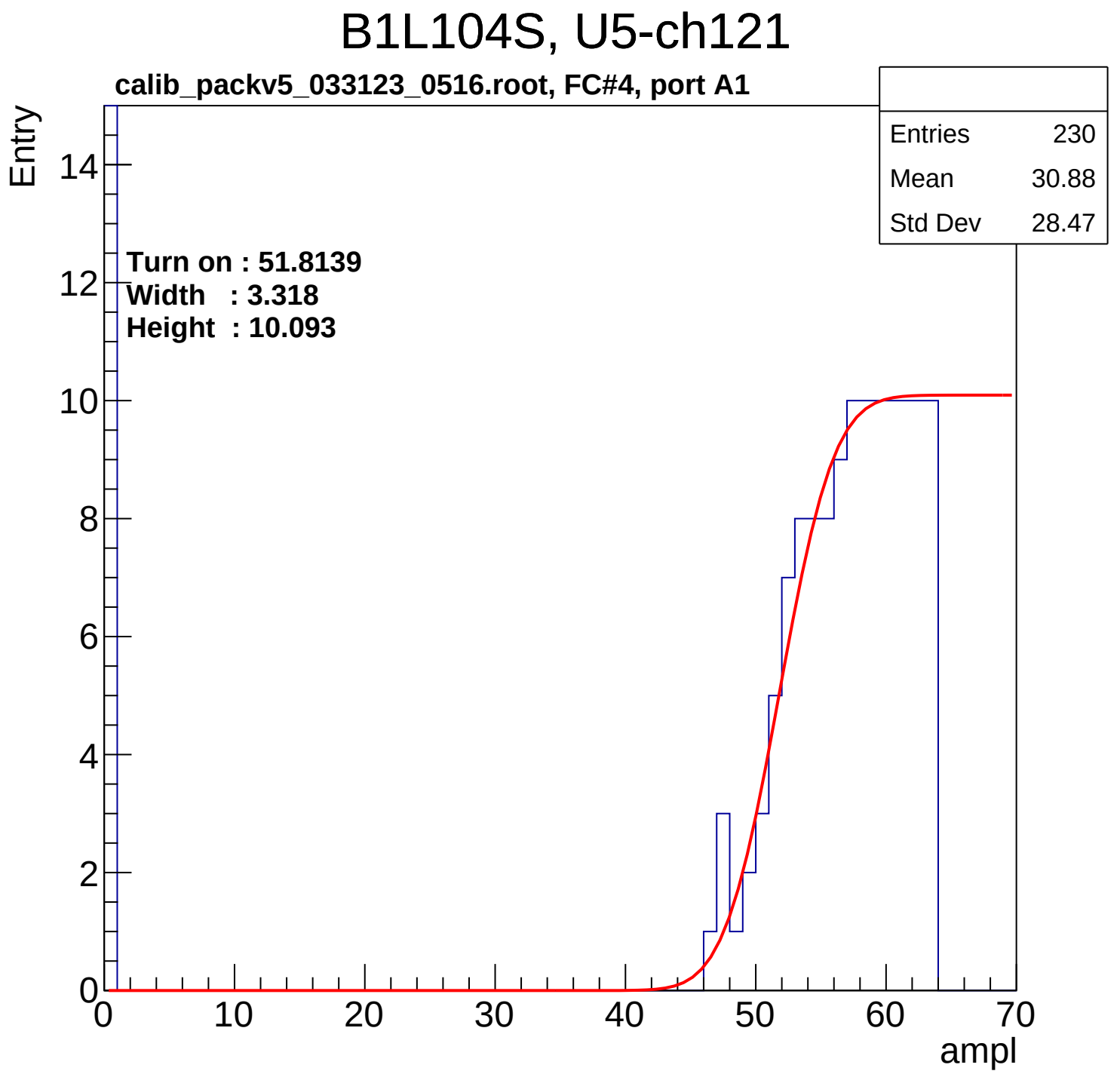

B1L104S, U5-ch116
calib_packv5_033123_0516.root, FC#4, port A1
Entries 191
Mean 29.87
Std Dev 28.94
Turn on : 55.0576
Width : 4.834
Height : 10.556
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

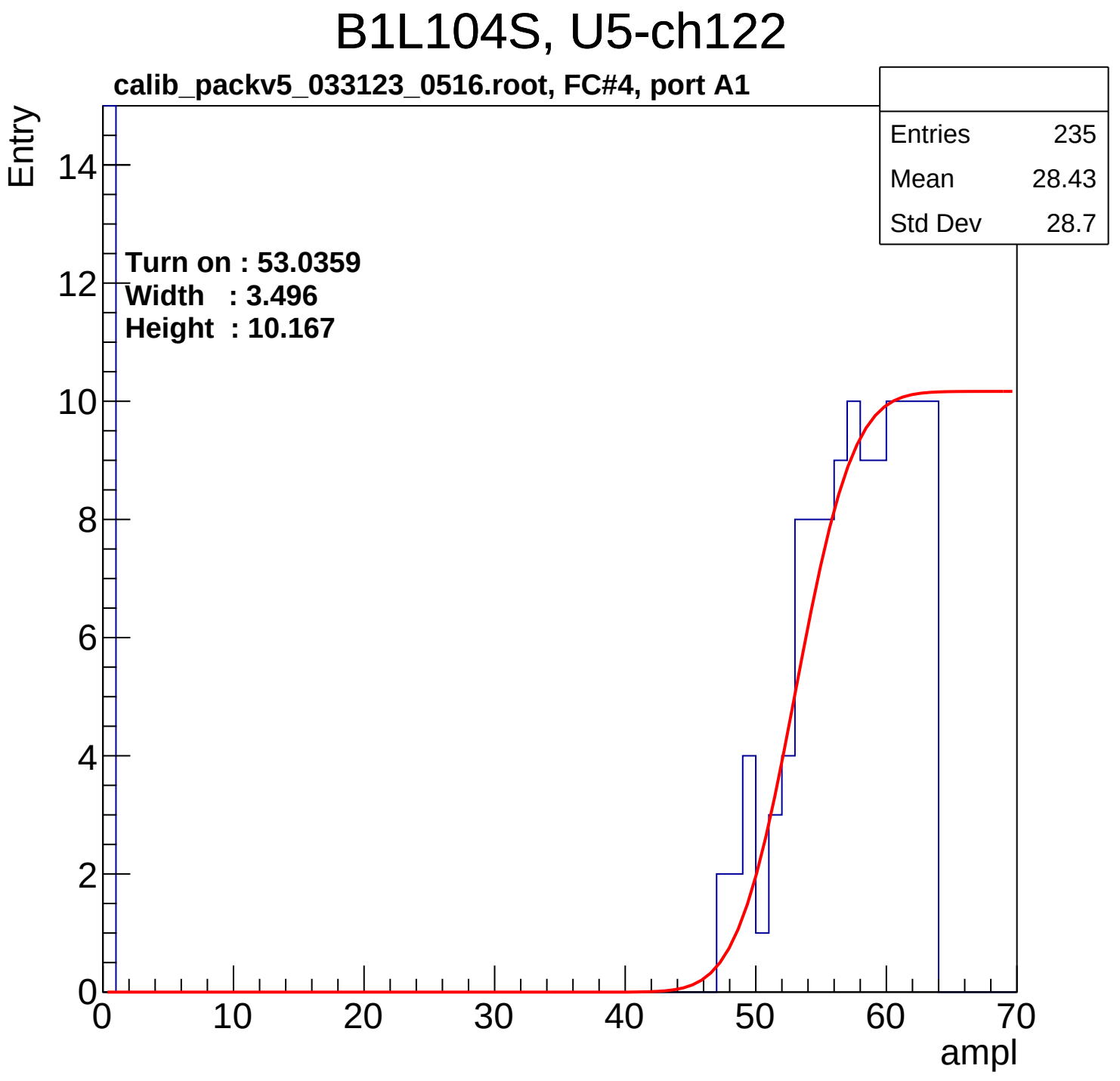

B1L104S, U5-ch117
calib_packv5_033123_0516.root, FC#4, port A1
Entries 194
Mean 34.91
Std Dev 27.93
Turn on : 53.0963
Width : 5.213
Height : 10.802
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

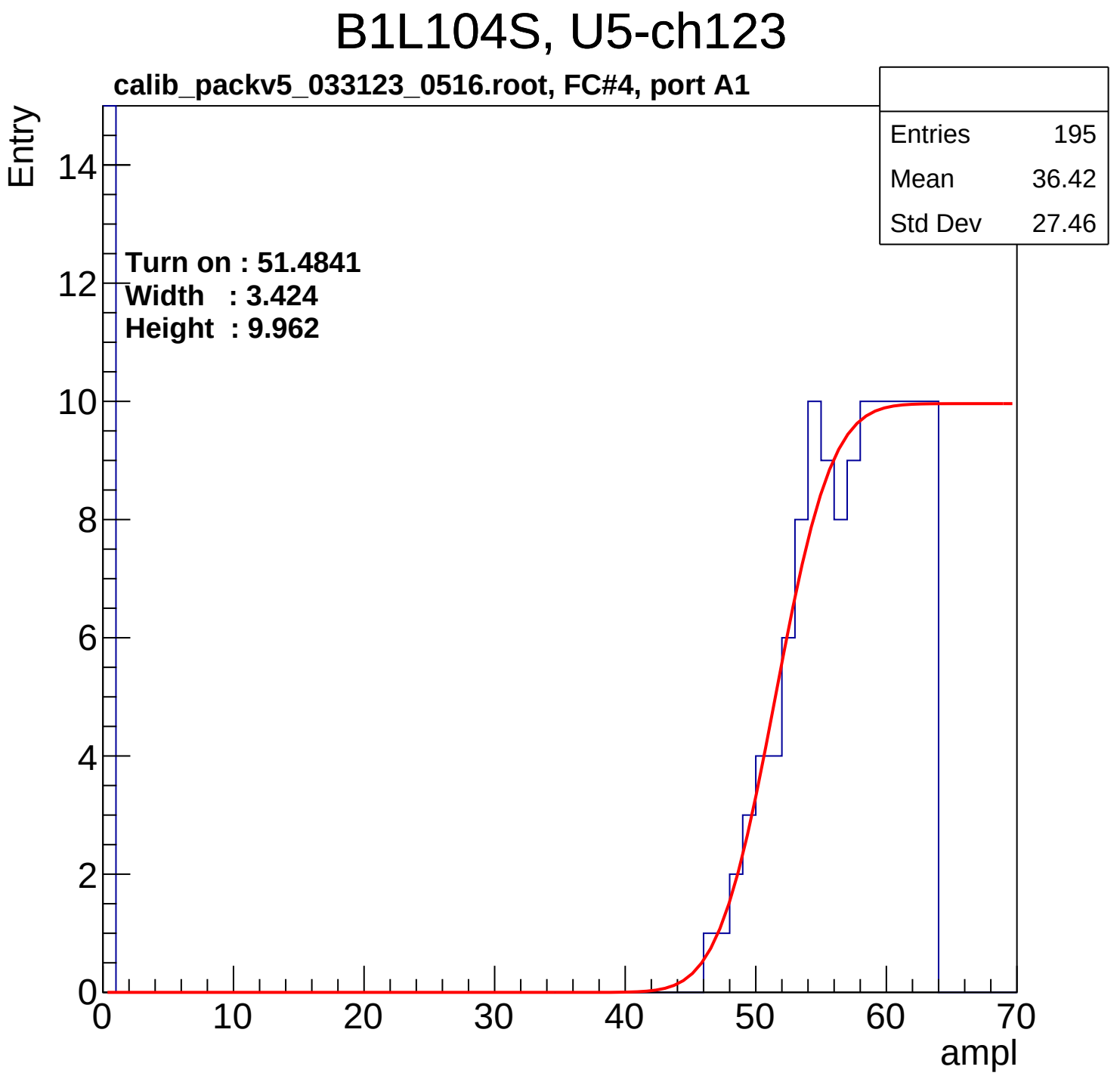

B1L104S, U5-ch118
calib_packv5_033123_0516.root, FC#4, port A1
Entries 211
Mean 31.26
Std Dev 28.49
Turn on : 52.9314
Width : 4.555
Height : 10.119
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

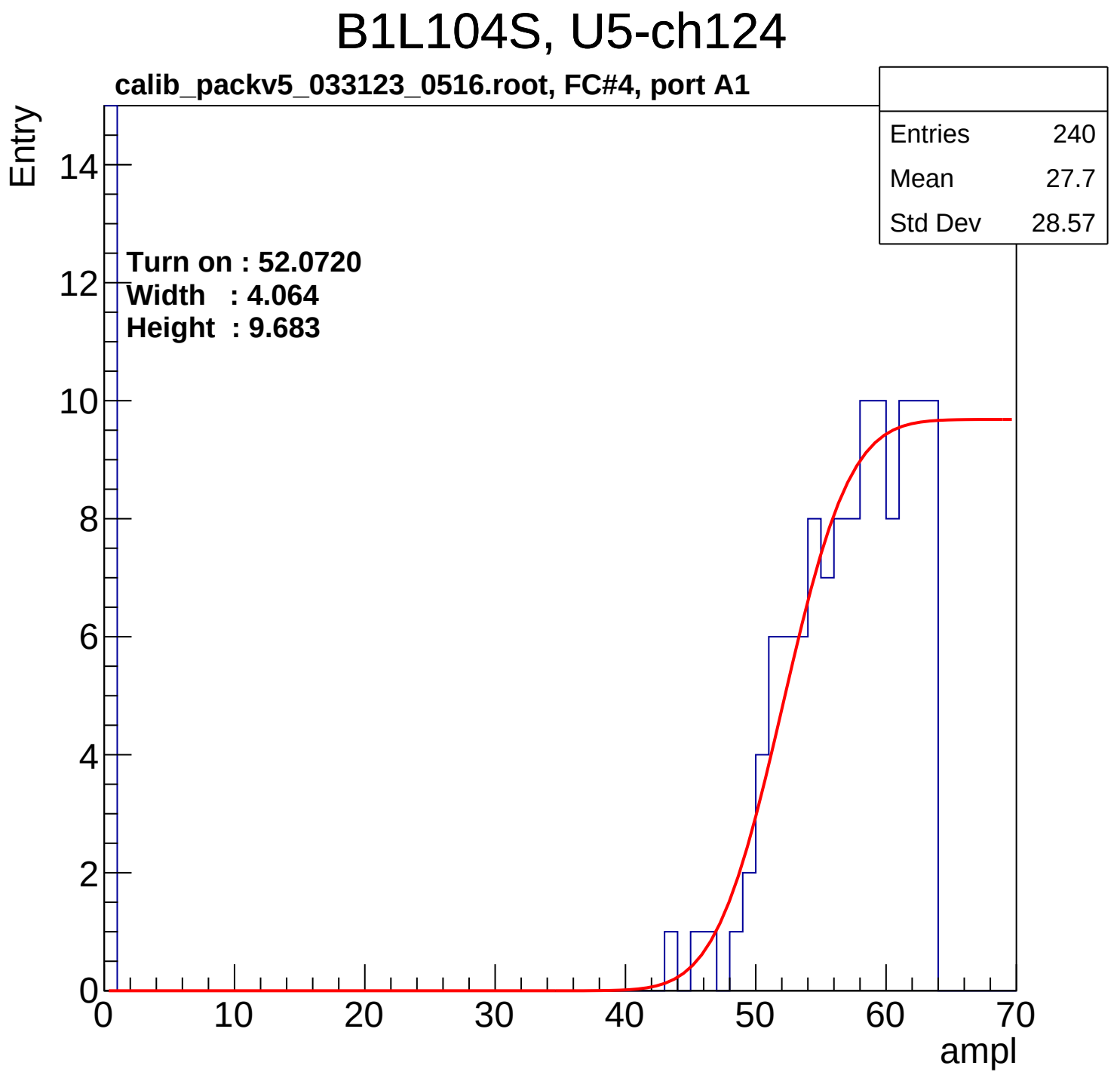

B1L104S, U5-ch119
calib_packv5_033123_0516.root, FC#4, port A1
Entries 217
Mean 29.66
Std Dev 28.86
Turn on : 54.7321
Width : 5.474
Height : 11.653
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

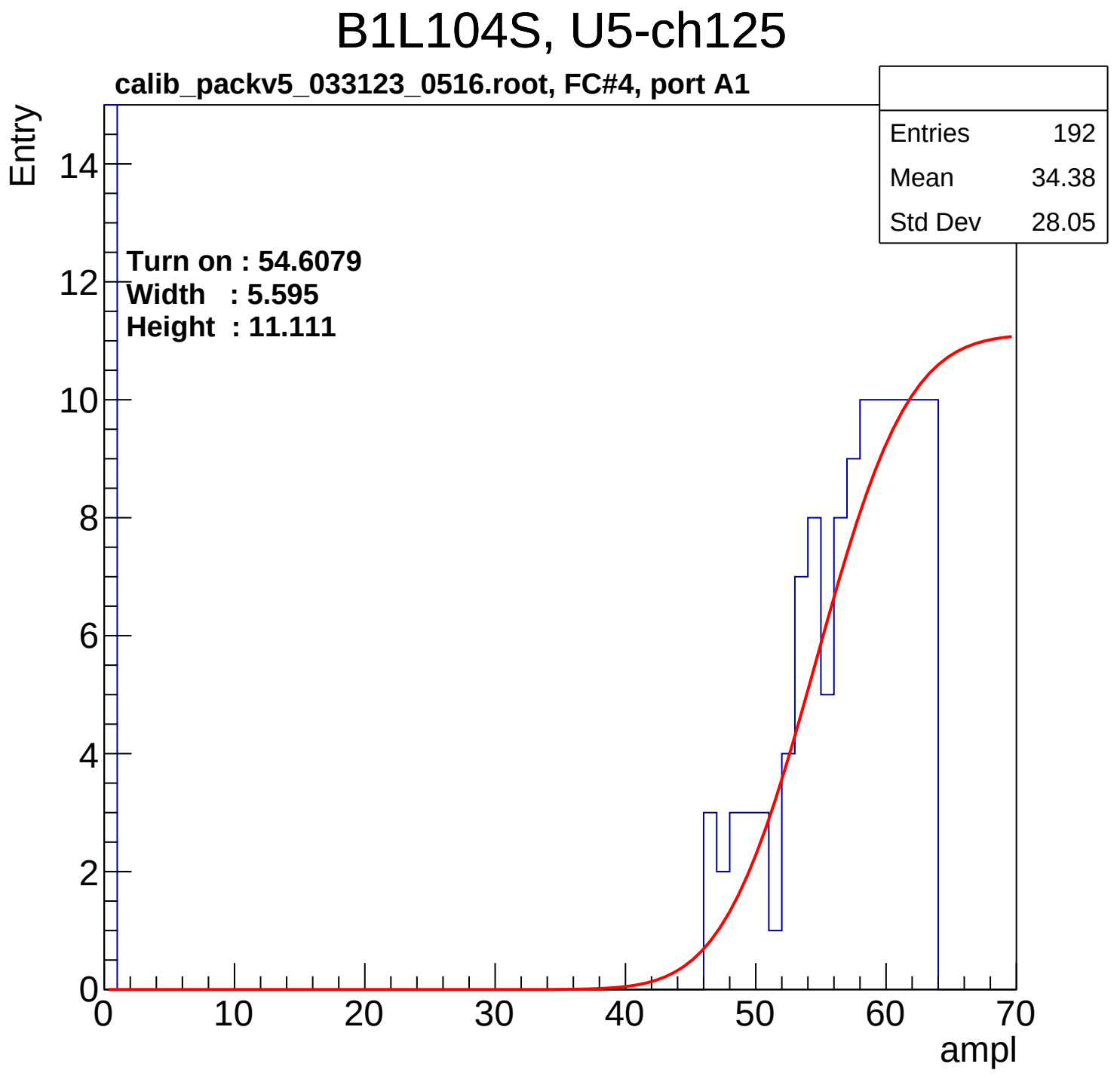

B1L104S, U5-ch120
calib_packv5_033123_0516.root, FC#4, port A1
Entries 234
Mean 28.43
Std Dev 28.12
Turn on : 52.4499
Width : 3.361
Height : 9.511
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

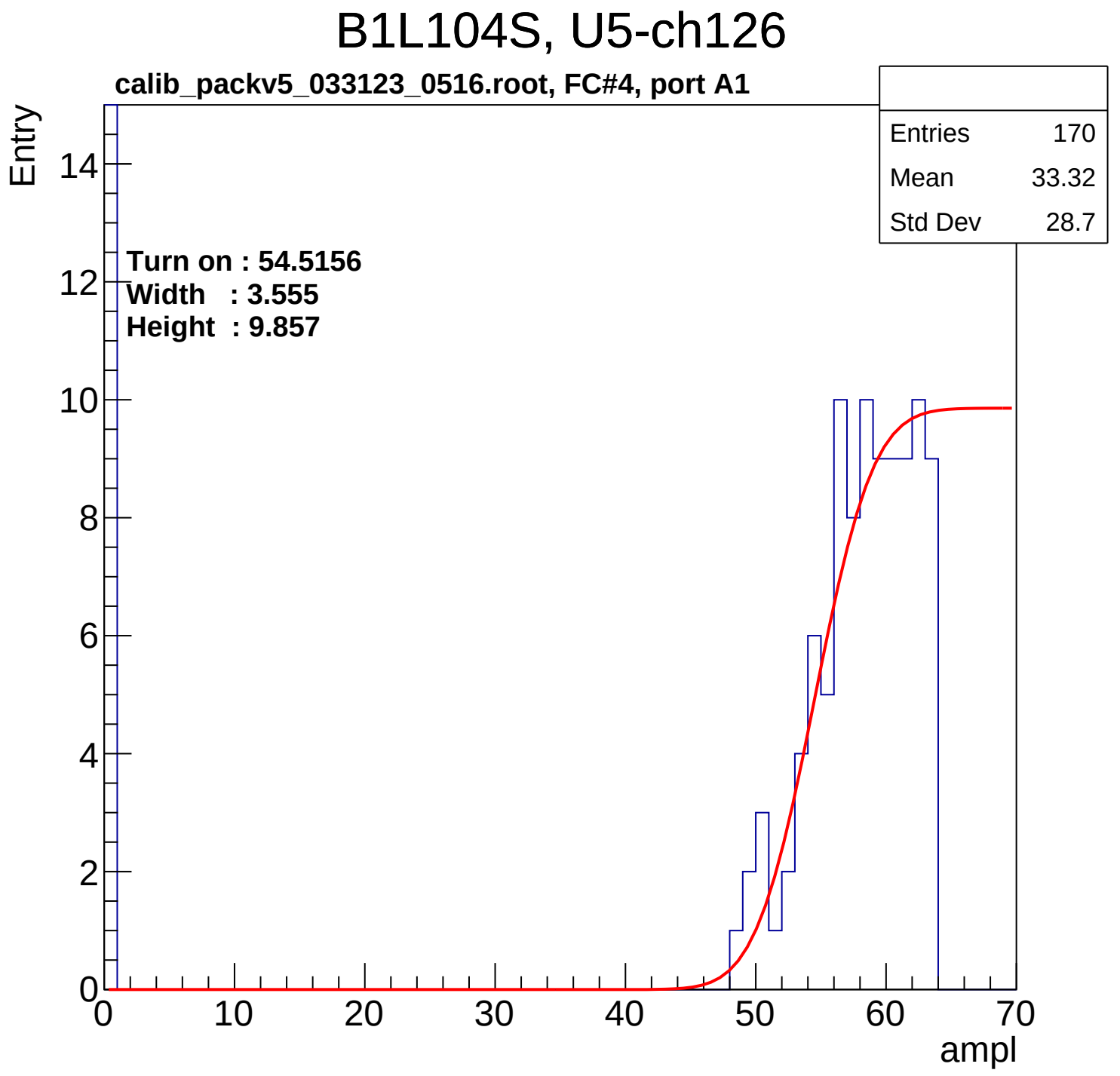

B1L104S, U5-ch121
calib_packv5_033123_0516.root, FC#4, port A1
Entries 230
Mean 30.88
Std Dev 28.47
Turn on : 51.8139
Width : 3.318
Height : 10.093
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

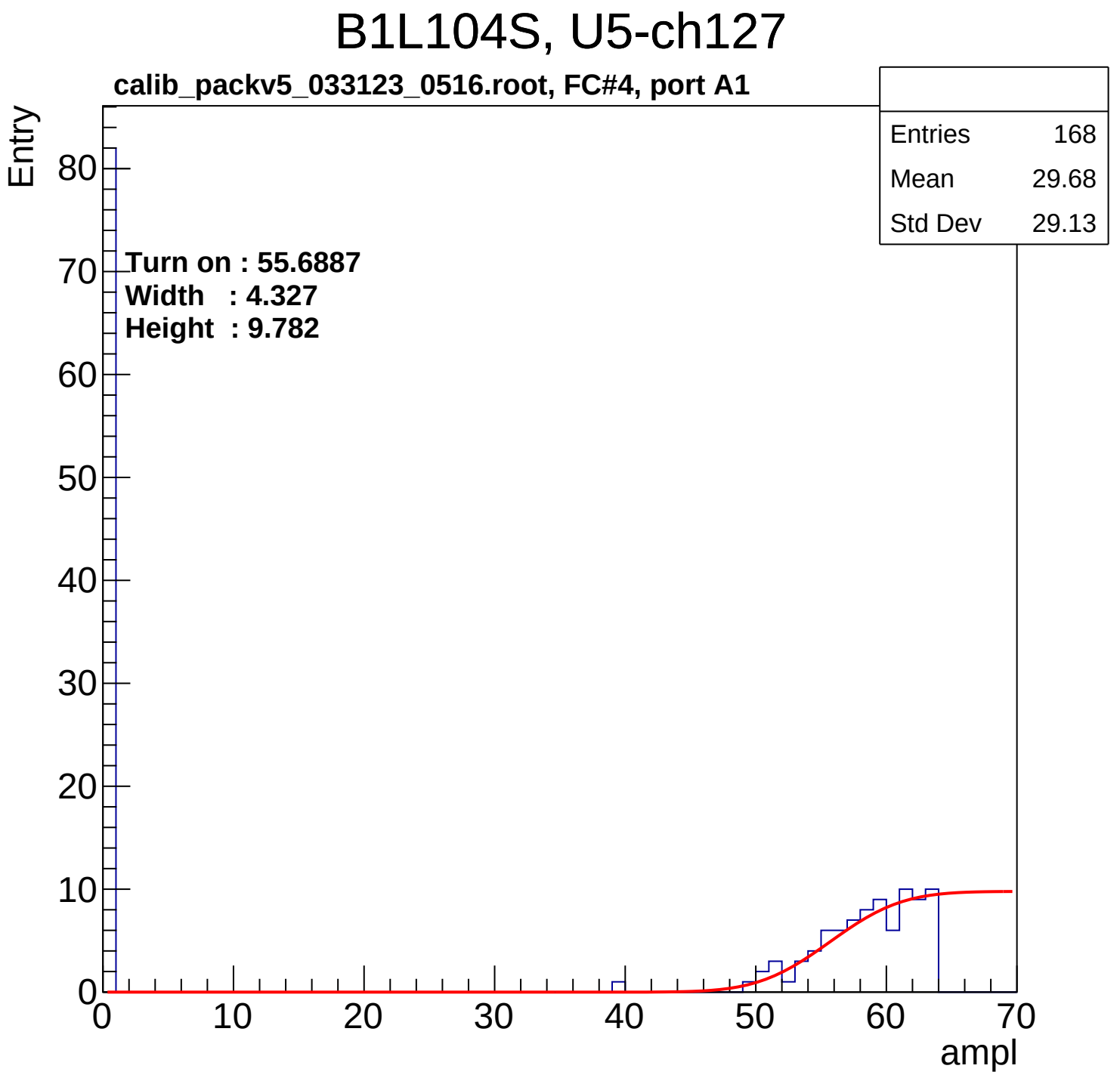

B1L104S, U5-ch122
calib_packv5_033123_0516.root, FC#4, port A1
Entries 235
Mean 28.43
Std Dev 28.7
Turn on : 53.0359
Width : 3.496
Height : 10.167
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

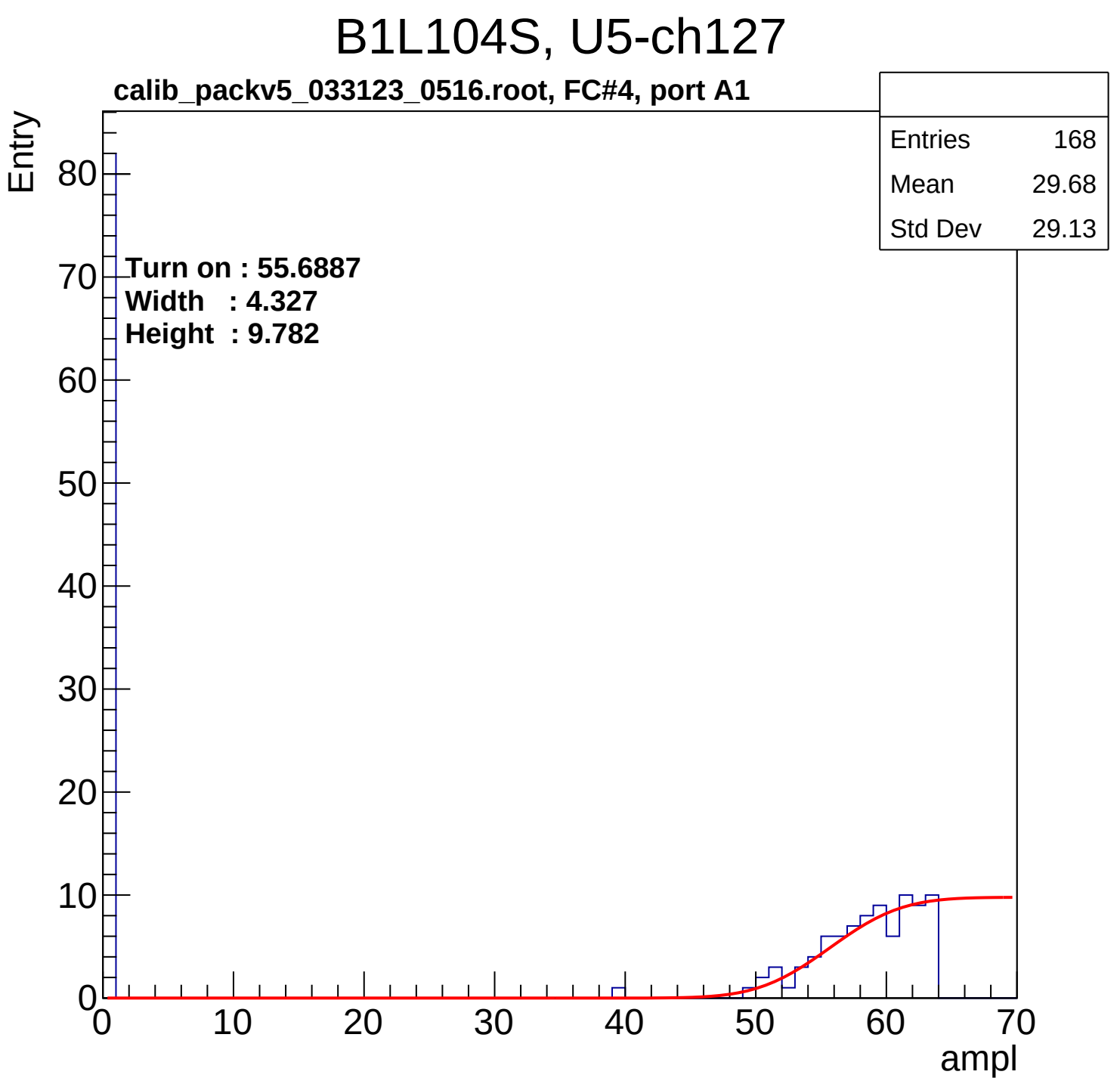

B1L104S, U5-ch123
calib_packv5_033123_0516.root, FC#4, port A1
Entries 195
Mean 36.42
Std Dev 27.46
Turn on : 51.4841
Width : 3.424
Height : 9.962
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L104S, U5-ch124
calib_packv5_033123_0516.root, FC#4, port A1
Entries 240
Mean 27.7
Std Dev 28.57
Turn on : 52.0720
Width : 4.064
Height : 9.683
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L104S, U5-ch125
calib_packv5_033123_0516.root, FC#4, port A1
Entries 192
Mean 34.38
Std Dev 28.05
Turn on : 54.6079
Width : 5.595
Height : 11.111
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L104S, U5-ch126
calib_packv5_033123_0516.root, FC#4, port A1
Entries 170
Mean 33.32
Std Dev 28.7
Turn on : 54.5156
Width : 3.555
Height : 9.857
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L104S, U5-ch127
calib_packv5_033123_0516.root, FC#4, port A1
Entries 168
Mean 29.68
Std Dev 29.13
Turn on : 55.6887
Width : 4.327
Height : 9.782
Entry
ampl
0
10
20
30
40
50
60
70
80


B1L104S, U5-ch127
calib_packv5_033123_0516.root, FC#4, port A1
Entries 168
Mean 29.68
Std Dev 29.13
Turn on : 55.6887
Width : 4.327
Height : 9.782
Entry
ampl
0
10
20
30
40
50
60
70
80