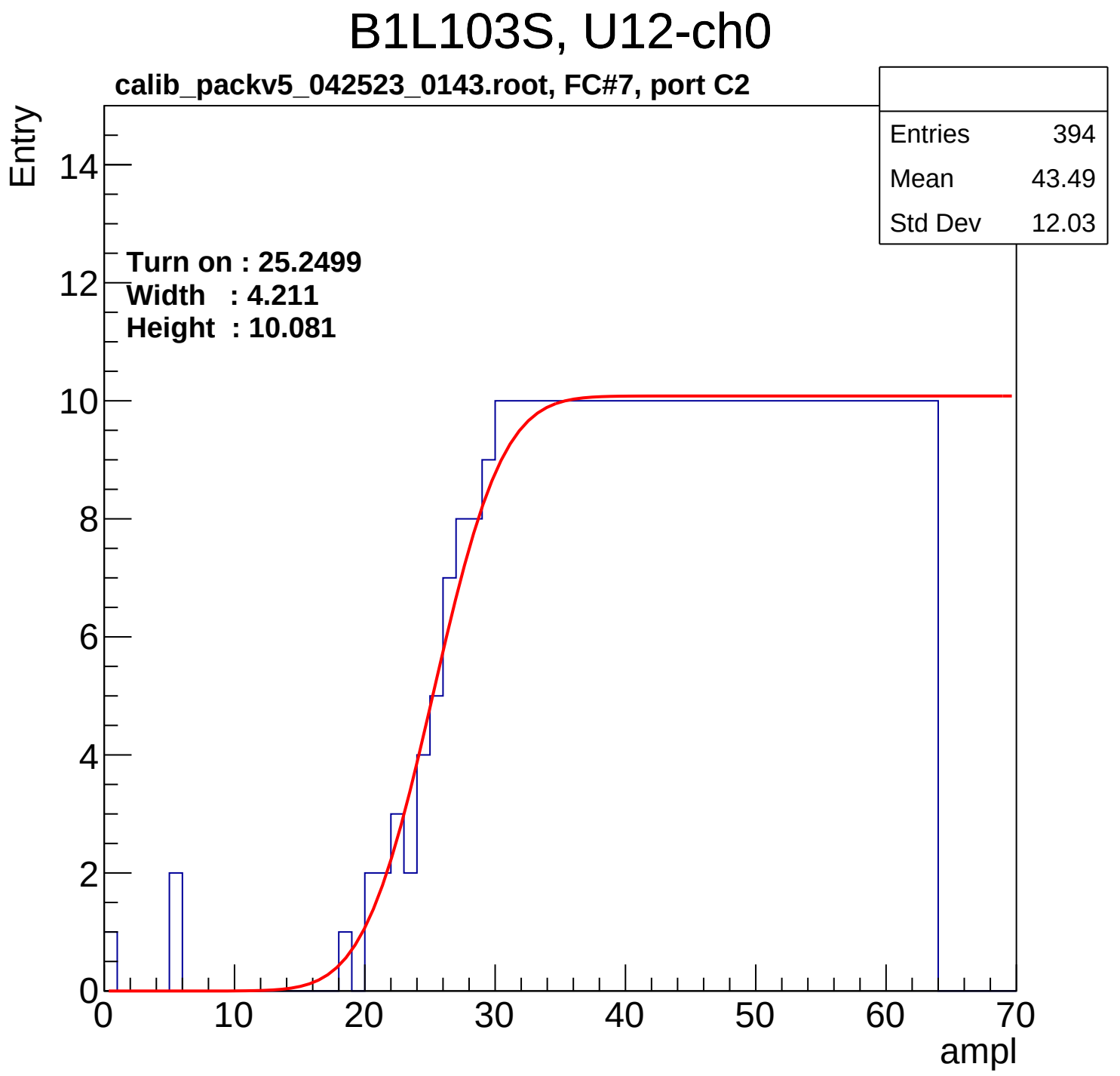
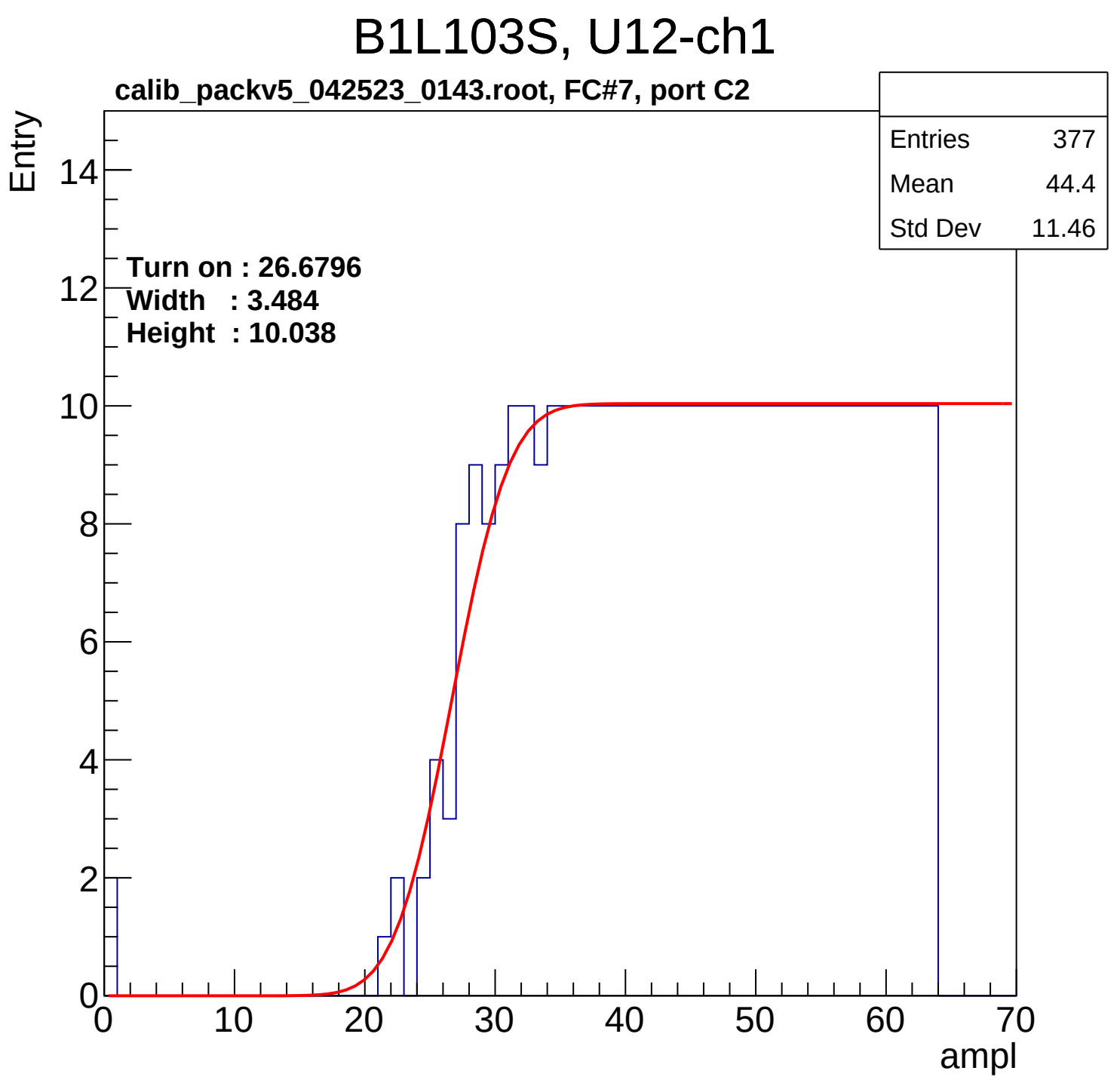
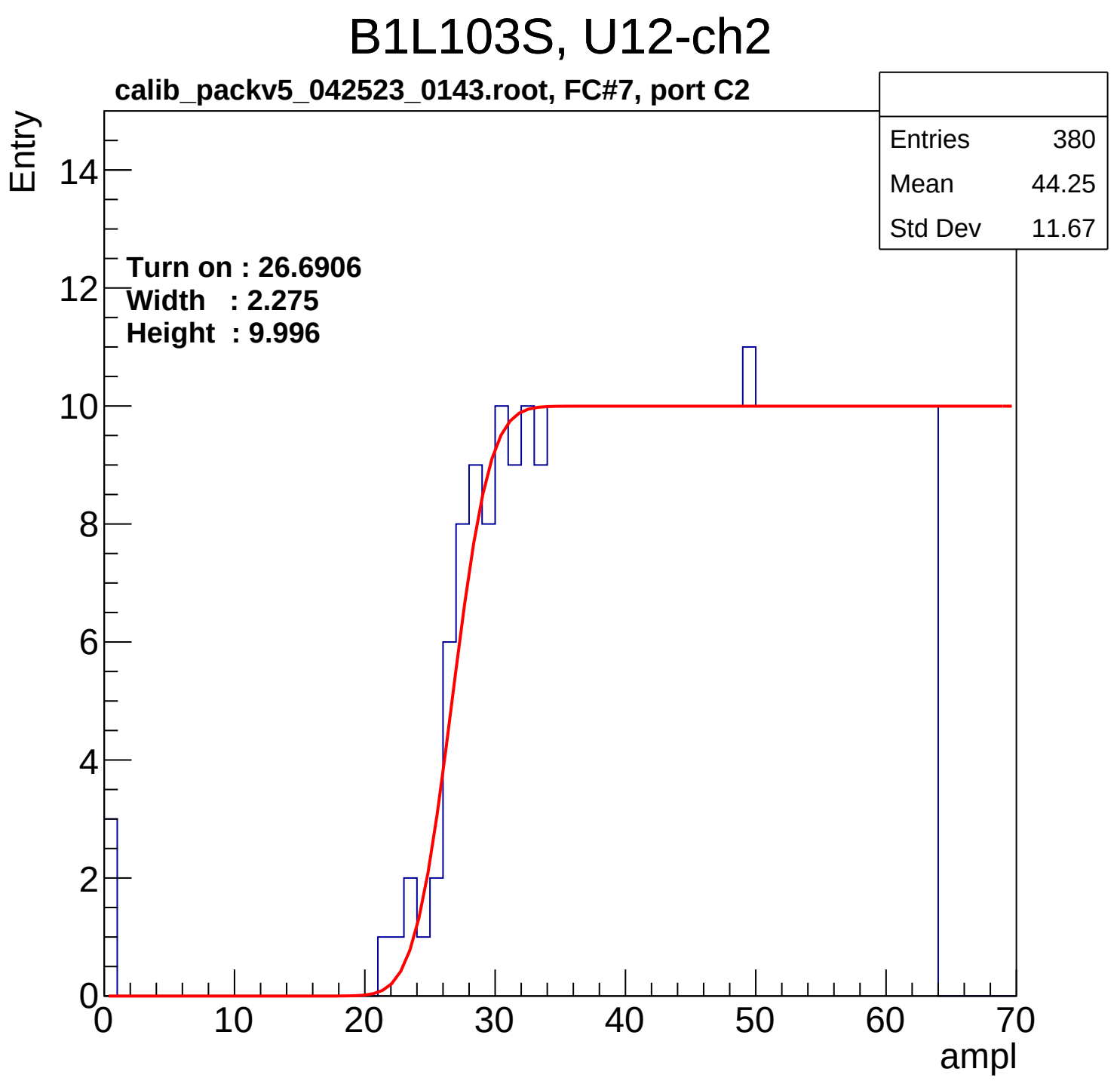
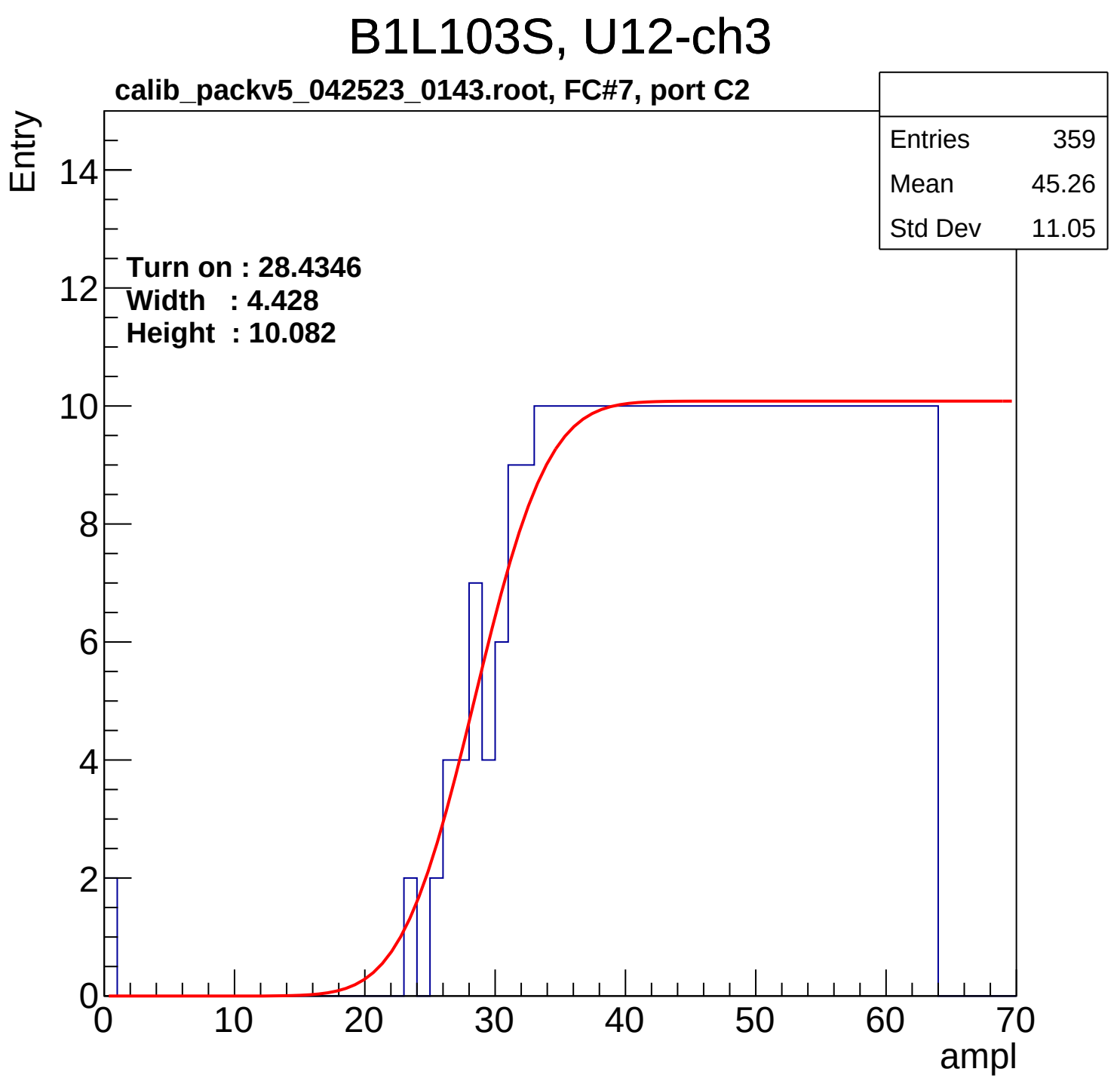
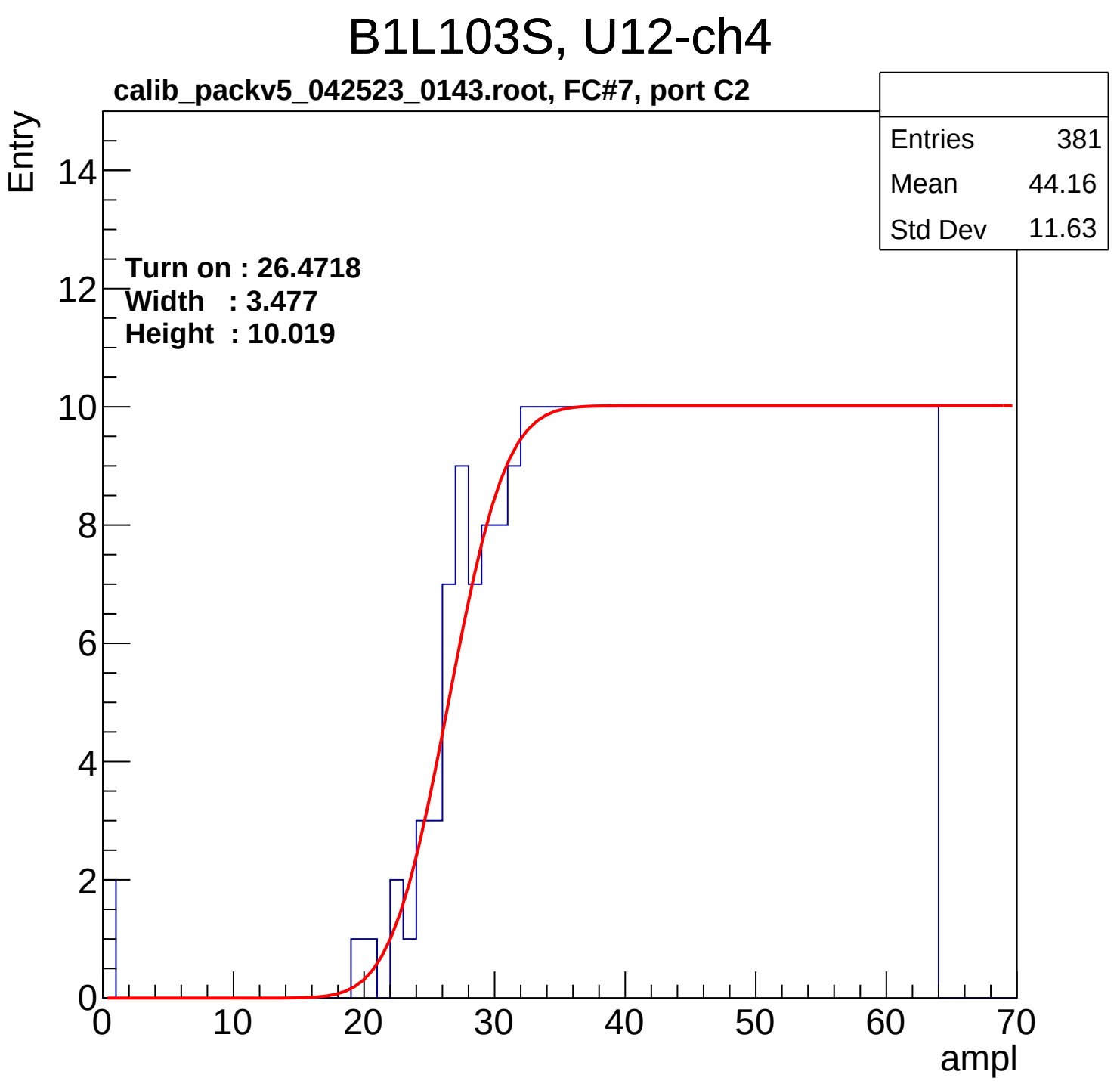
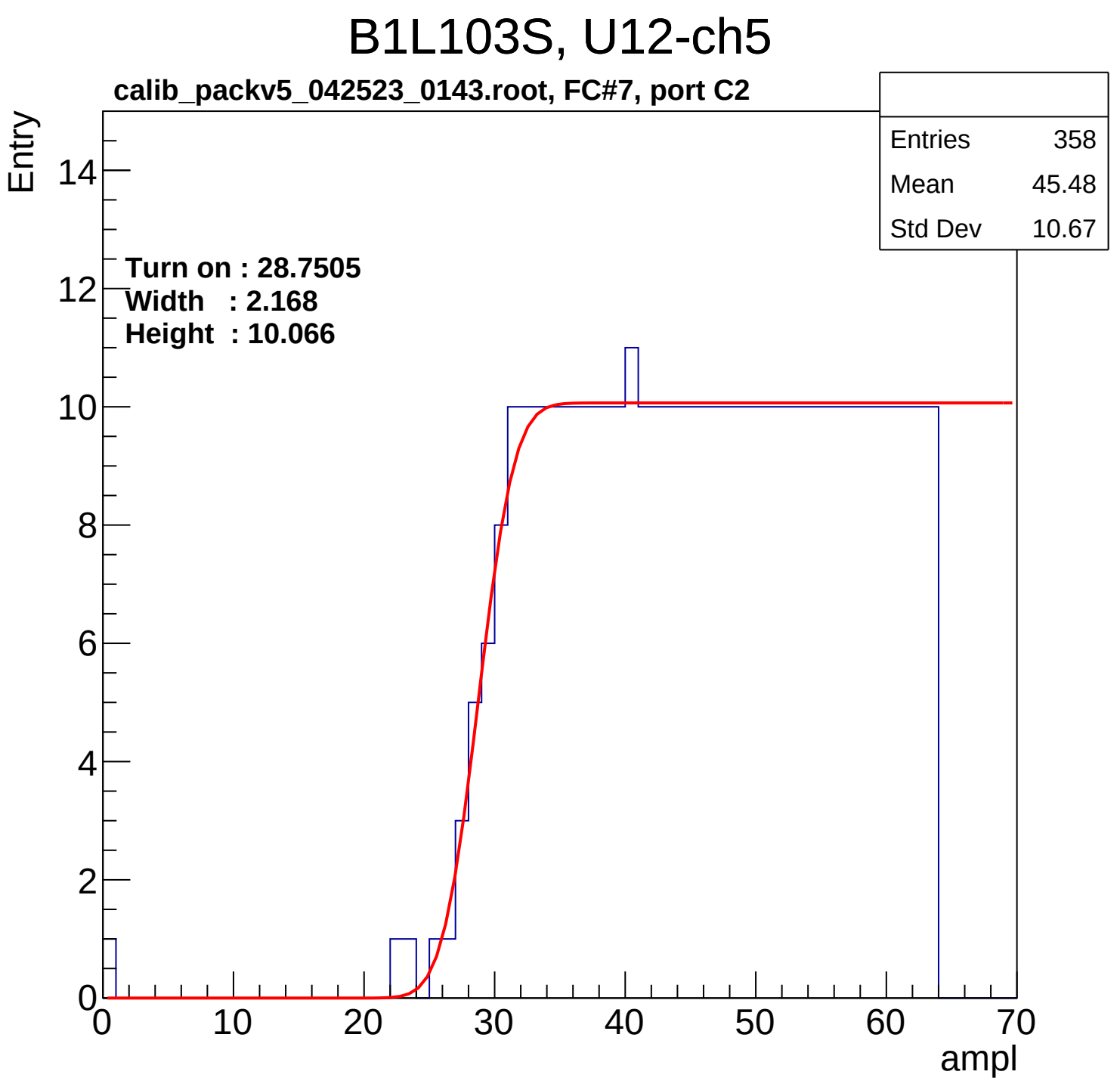

B1L103S, U12-ch0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 394
Mean 43.49
Std Dev 12.03
Turn on : 25.2499
Width : 4.211
Height : 10.081
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

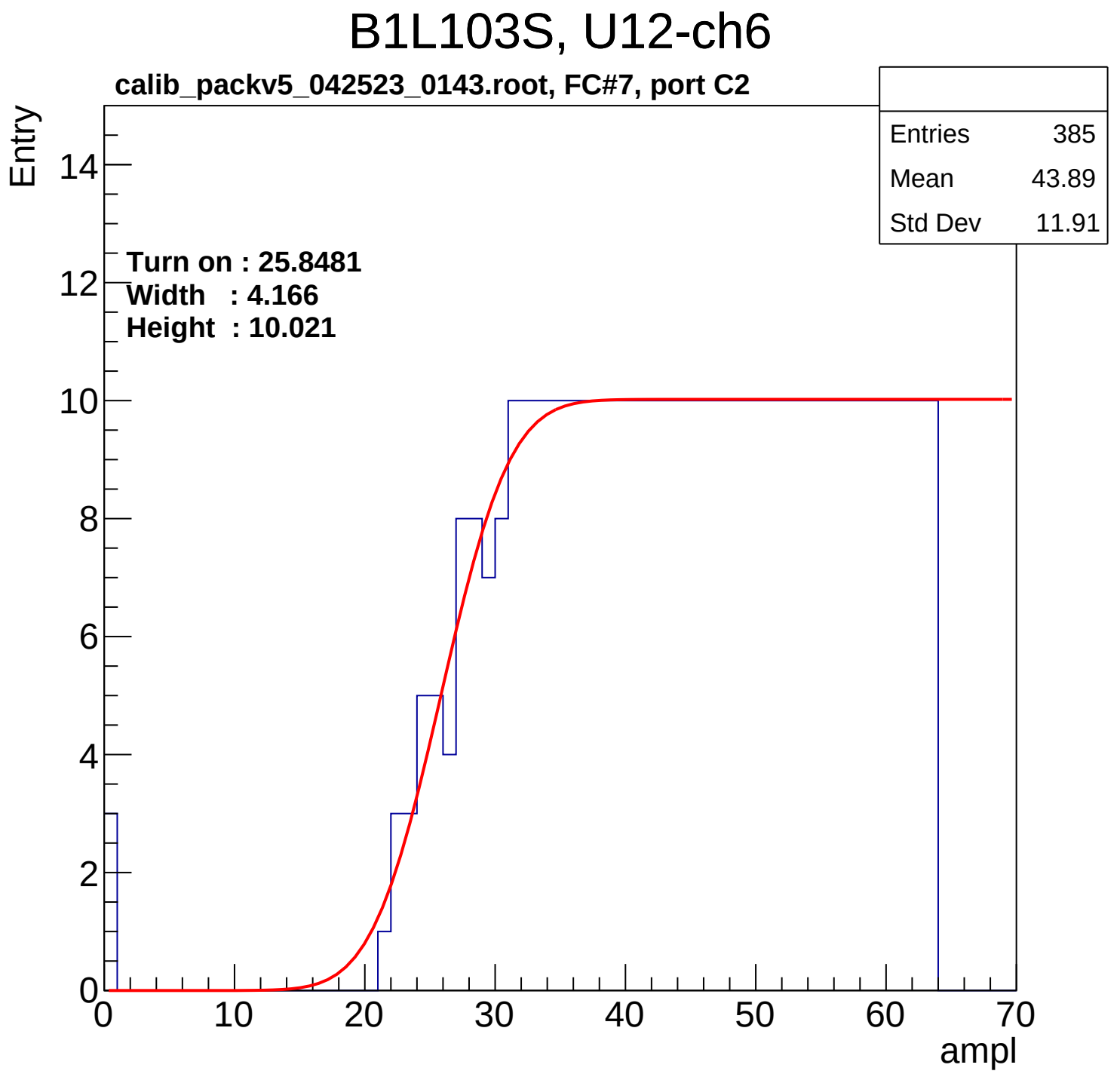

B1L103S, U12-ch1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 377
Mean 44.4
Std Dev 11.46
Turn on : 26.6796
Width : 3.484
Height : 10.038
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

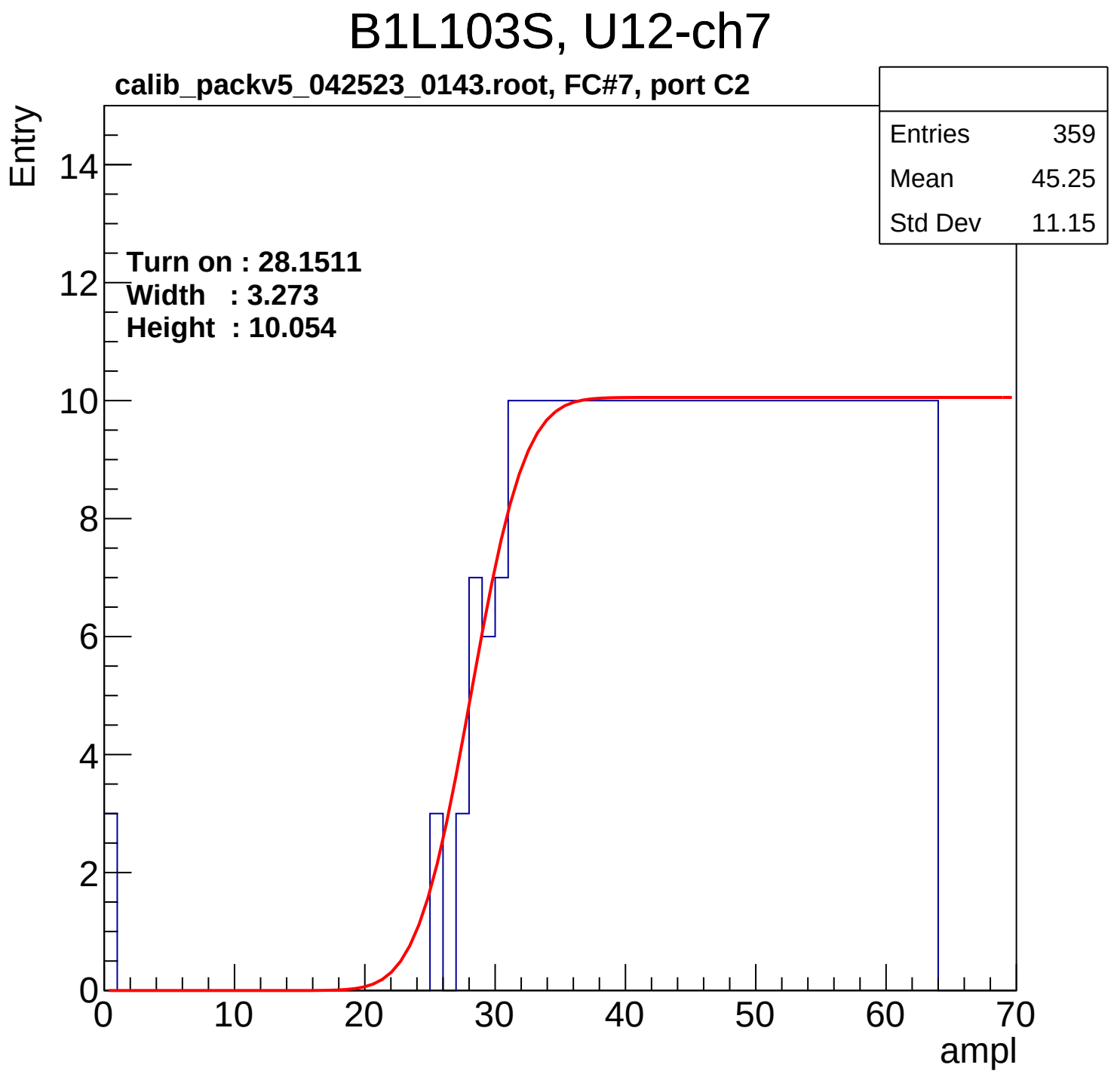

B1L103S, U12-ch2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 380
Mean 44.25
Std Dev 11.67
Turn on : 26.6906
Width : 2.275
Height : 9.996
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

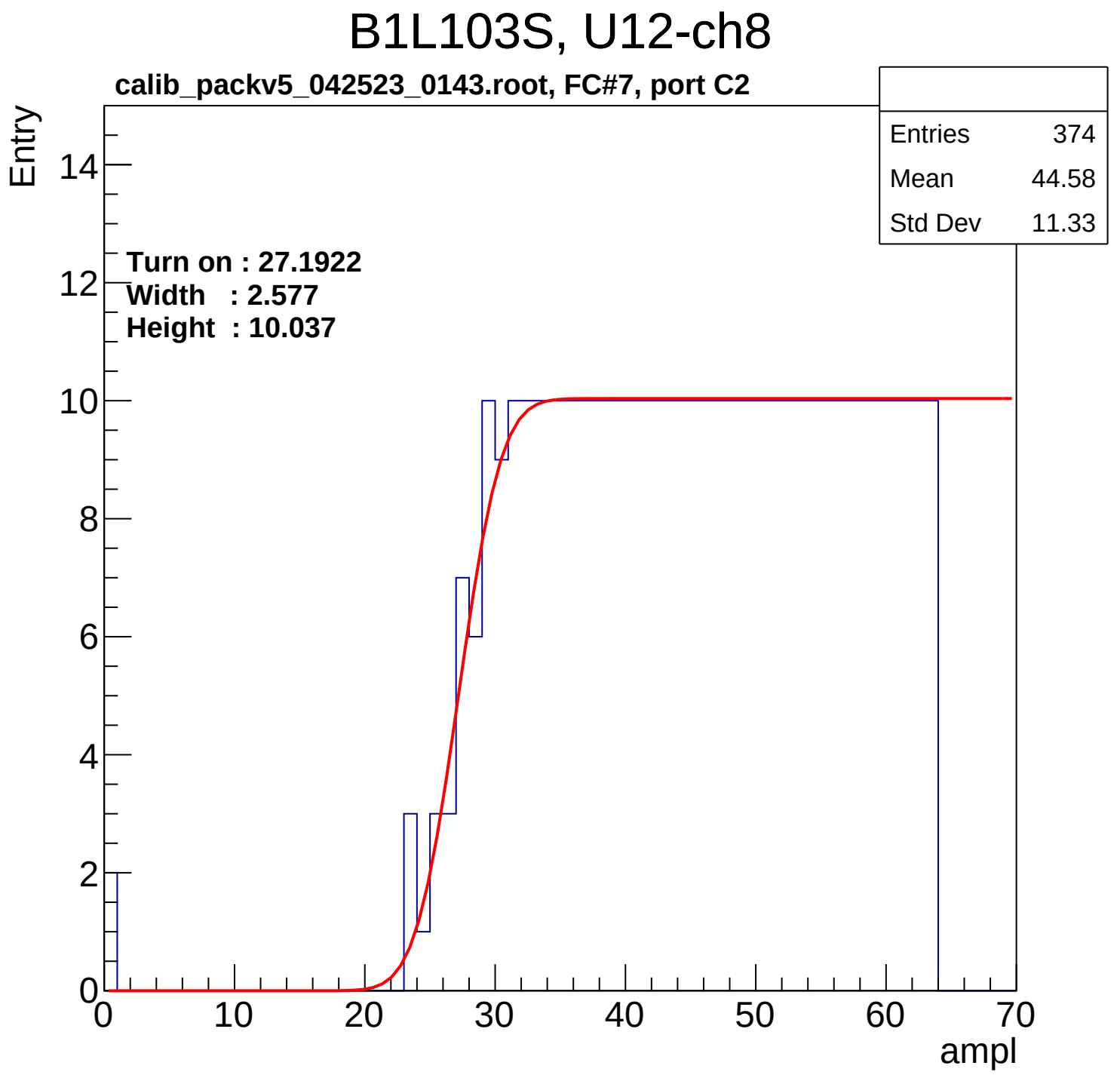

B1L103S, U12-ch3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 359
Mean 45.26
Std Dev 11.05
Turn on : 28.4346
Width : 4.428
Height : 10.082
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

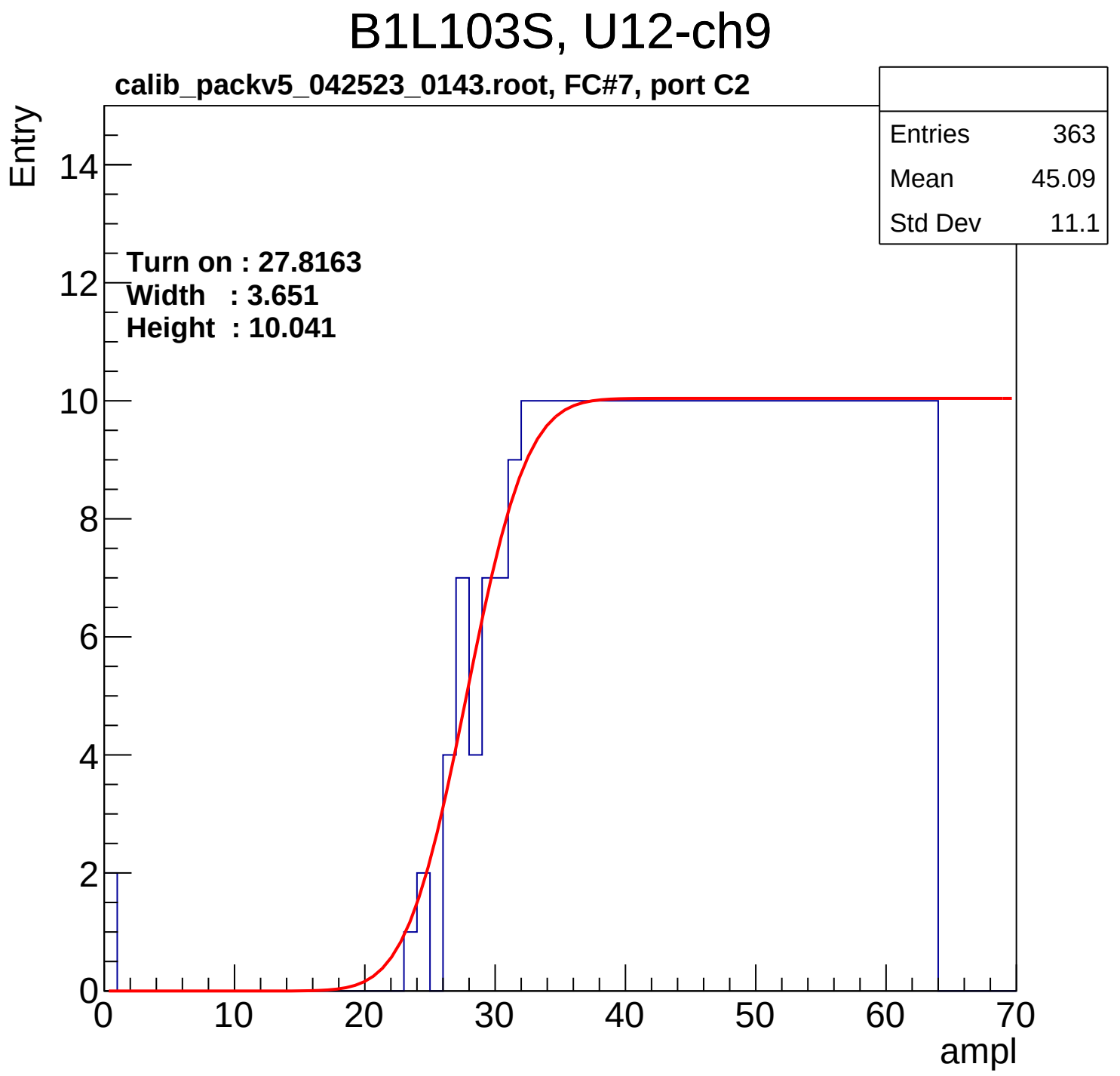

B1L103S, U12-ch4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 381
Mean 44.16
Std Dev 11.63
Turn on : 26.4718
Width : 3.477
Height : 10.019
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

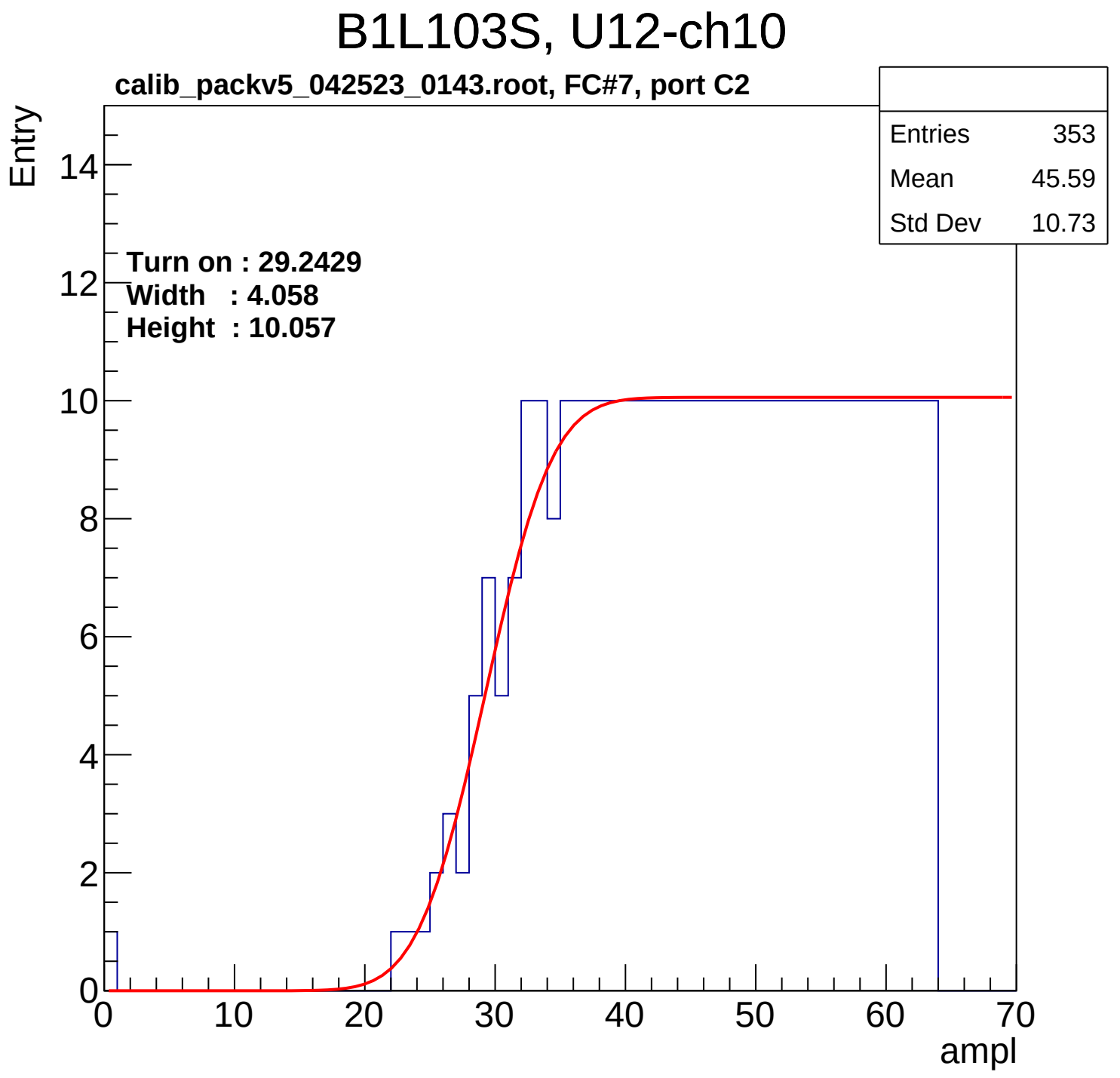

B1L103S, U12-ch5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 358
Mean 45.48
Std Dev 10.67
Turn on : 28.7505
Width : 2.168
Height : 10.066
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

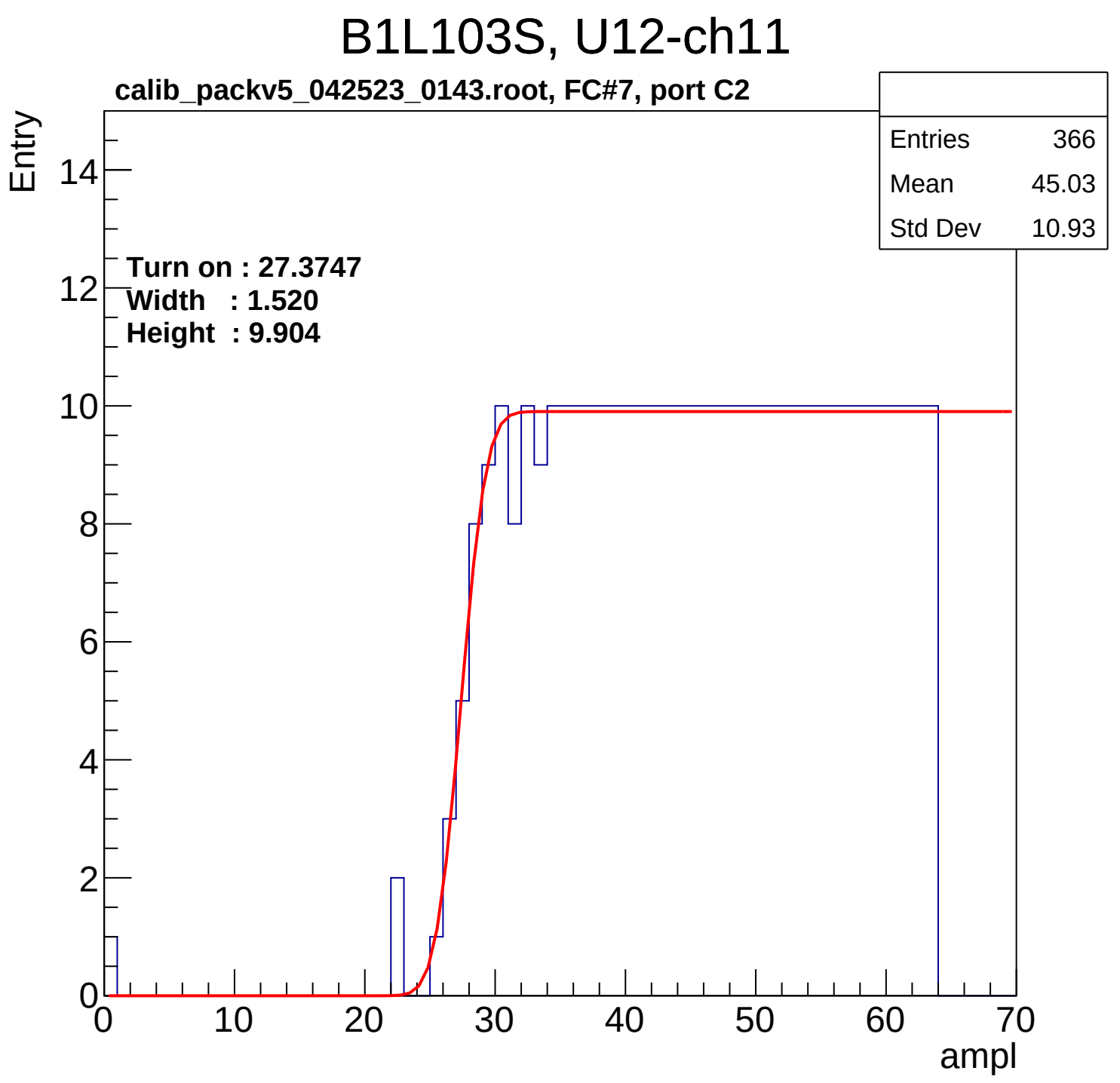

B1L103S, U12-ch6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 385
Mean 43.89
Std Dev 11.91
Turn on : 25.8481
Width : 4.166
Height : 10.021
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

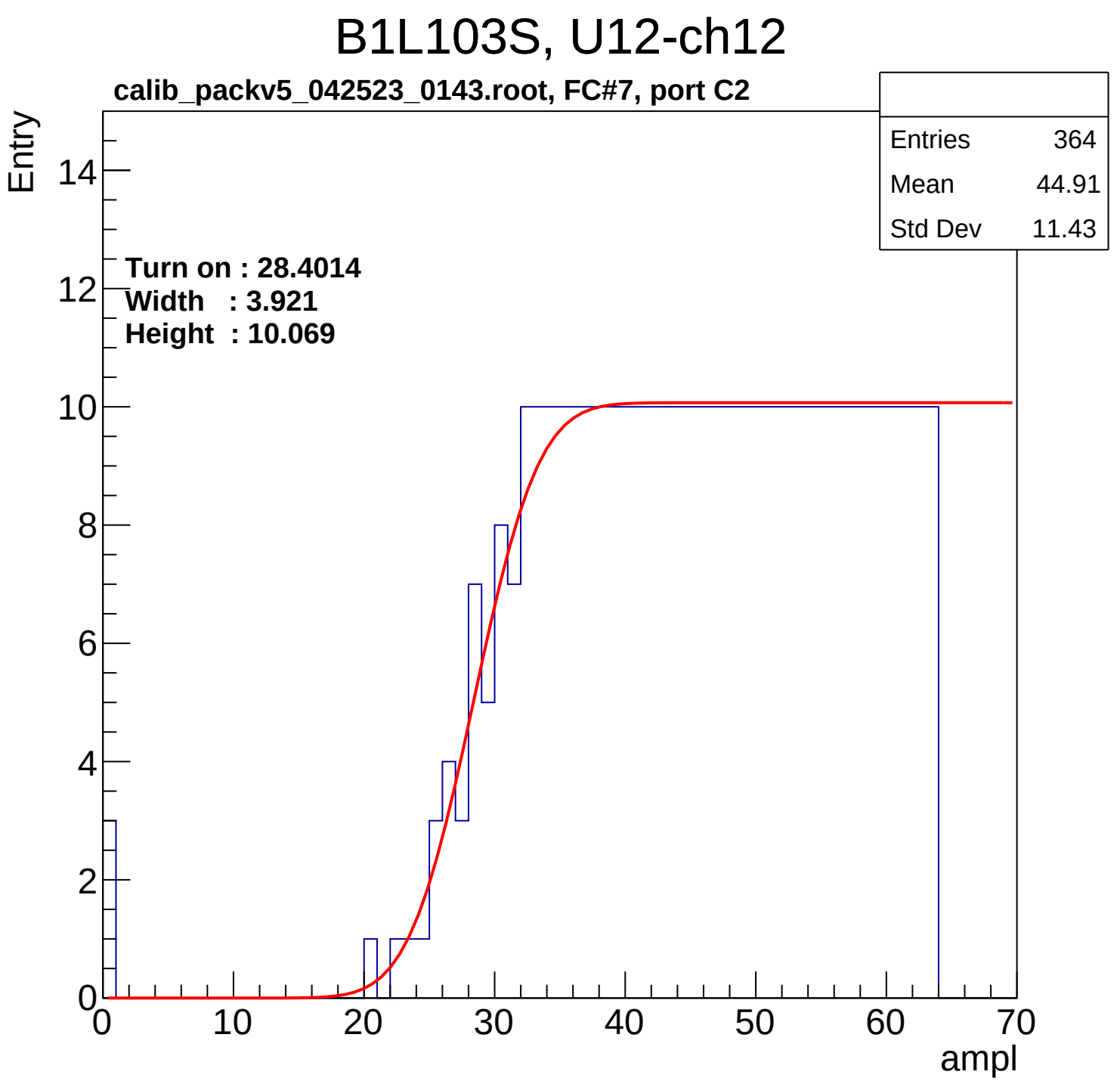

B1L103S, U12-ch7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 359
Mean 45.25
Std Dev 11.15
Turn on : 28.1511
Width : 3.273
Height : 10.054
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

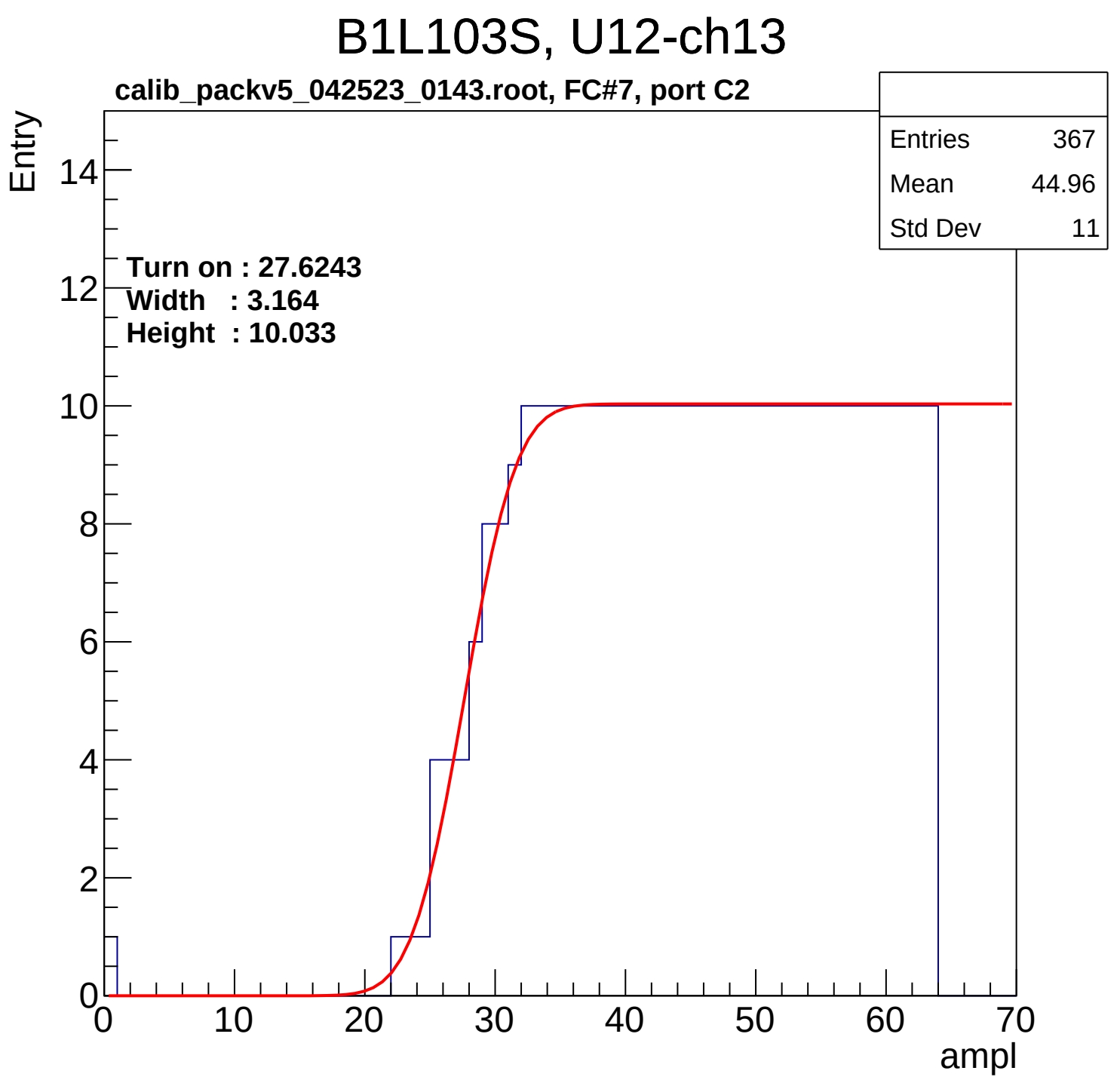

B1L103S, U12-ch8
calib_packv5_042523_0143.root, FC#7, port C2
Entries 374
Mean 44.58
Std Dev 11.33
Turn on : 27.1922
Width : 2.577
Height : 10.037
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

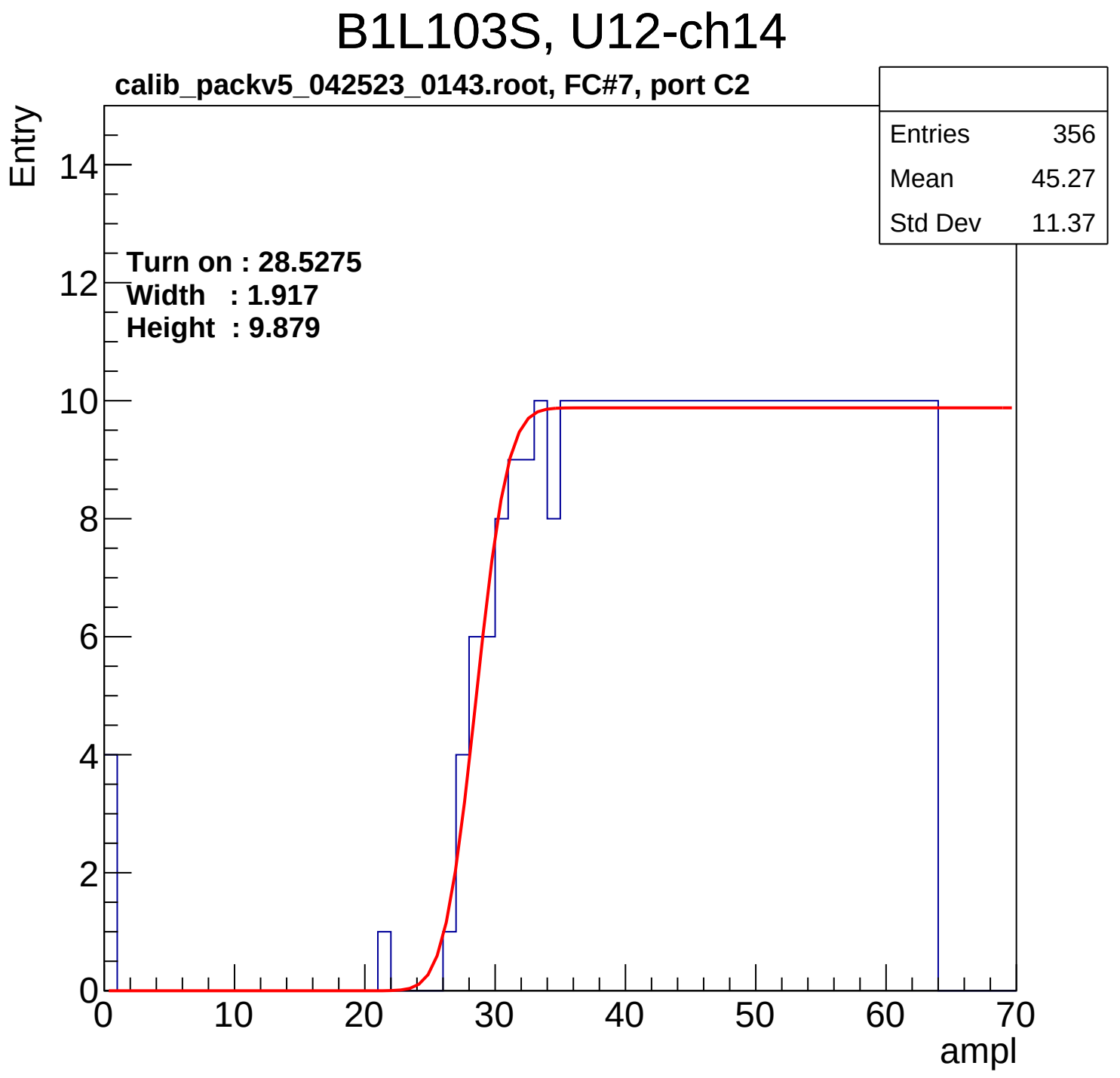

B1L103S, U12-ch9
calib_packv5_042523_0143.root, FC#7, port C2
Entries 363
Mean 45.09
Std Dev 11.1
Turn on : 27.8163
Width : 3.651
Height : 10.041
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

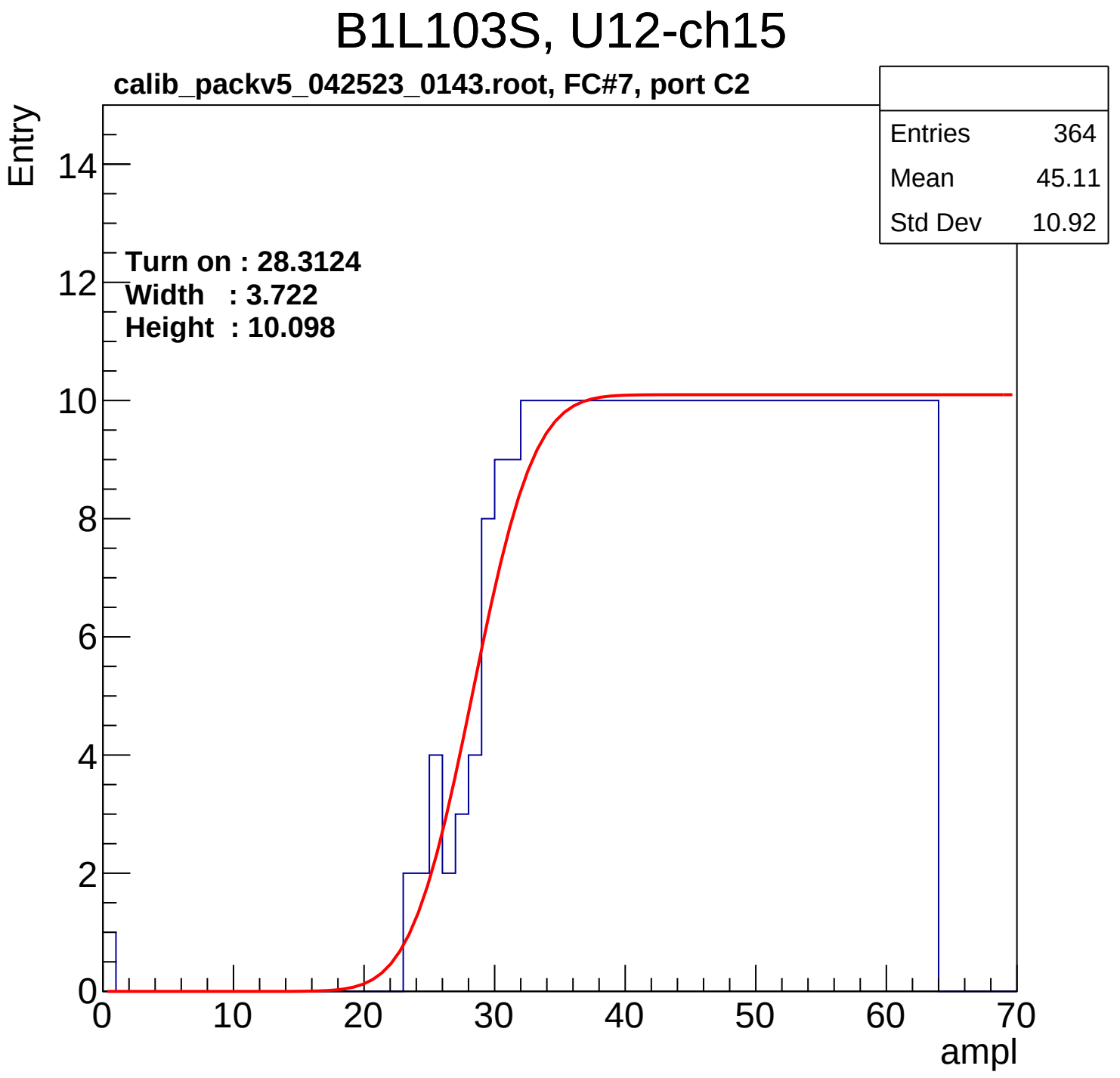

B1L103S, U12-ch10
calib_packv5_042523_0143.root, FC#7, port C2
Entries 353
Mean 45.59
Std Dev 10.73
Turn on : 29.2429
Width : 4.058
Height : 10.057
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

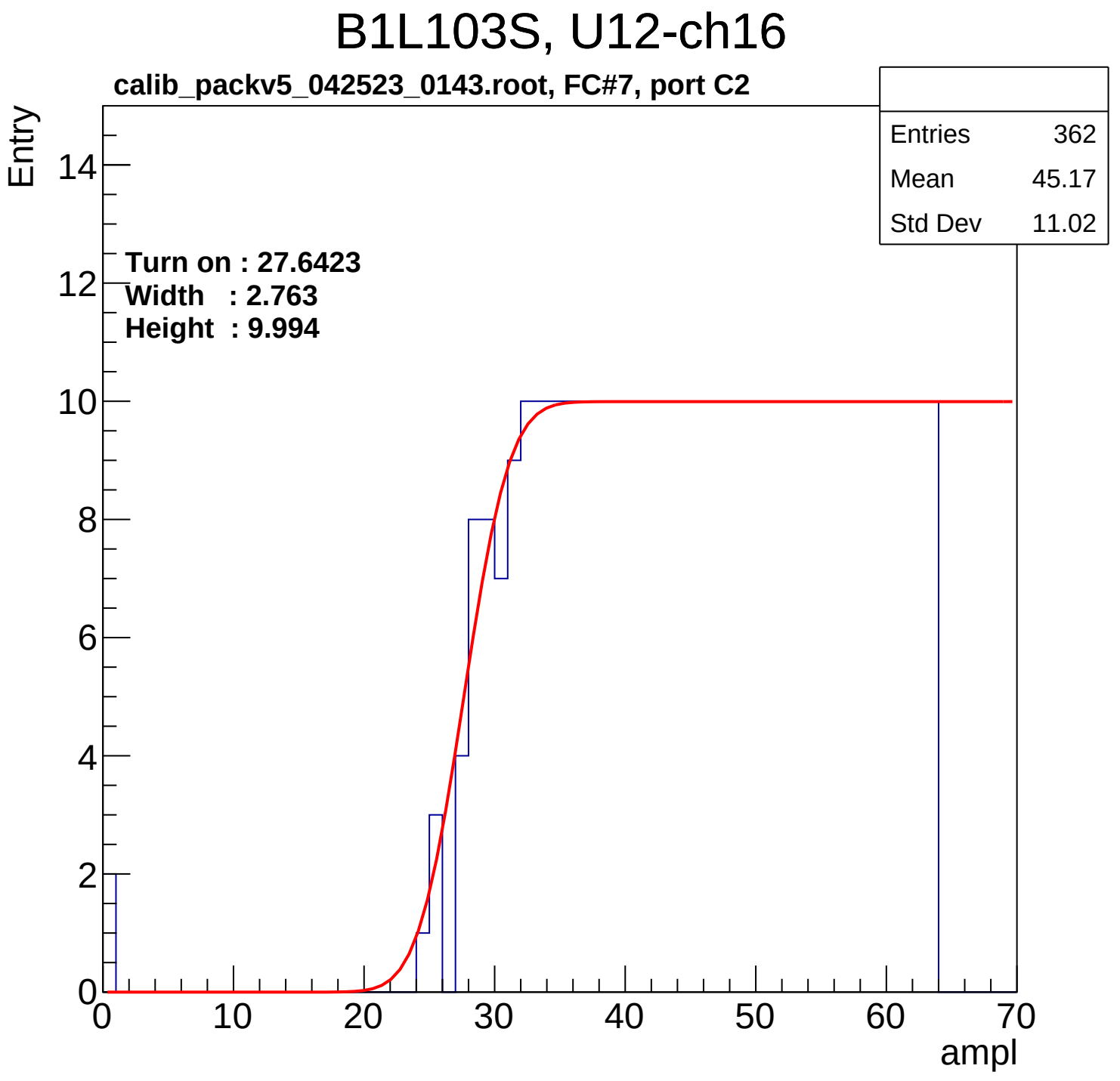

B1L103S, U12-ch11
calib_packv5_042523_0143.root, FC#7, port C2
Entries 366
Mean 45.03
Std Dev 10.93
Turn on : 27.3747
Width : 1.520
Height : 9.904
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

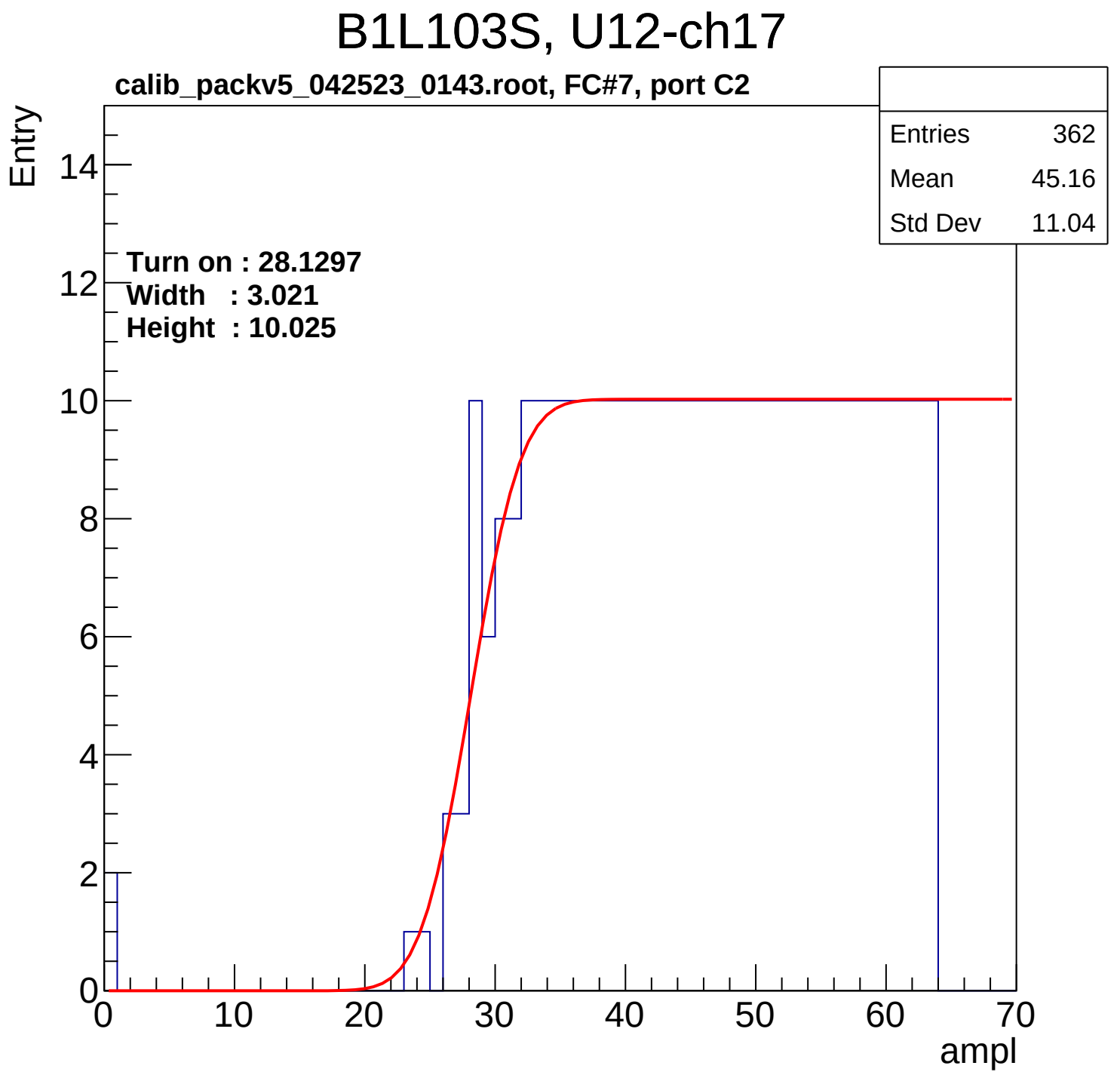

B1L103S, U12-ch12
calib_packv5_042523_0143.root, FC#7, port C2
Entries 364
Mean 44.91
Std Dev 11.43
Turn on : 28.4014
Width : 3.921
Height : 10.069
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

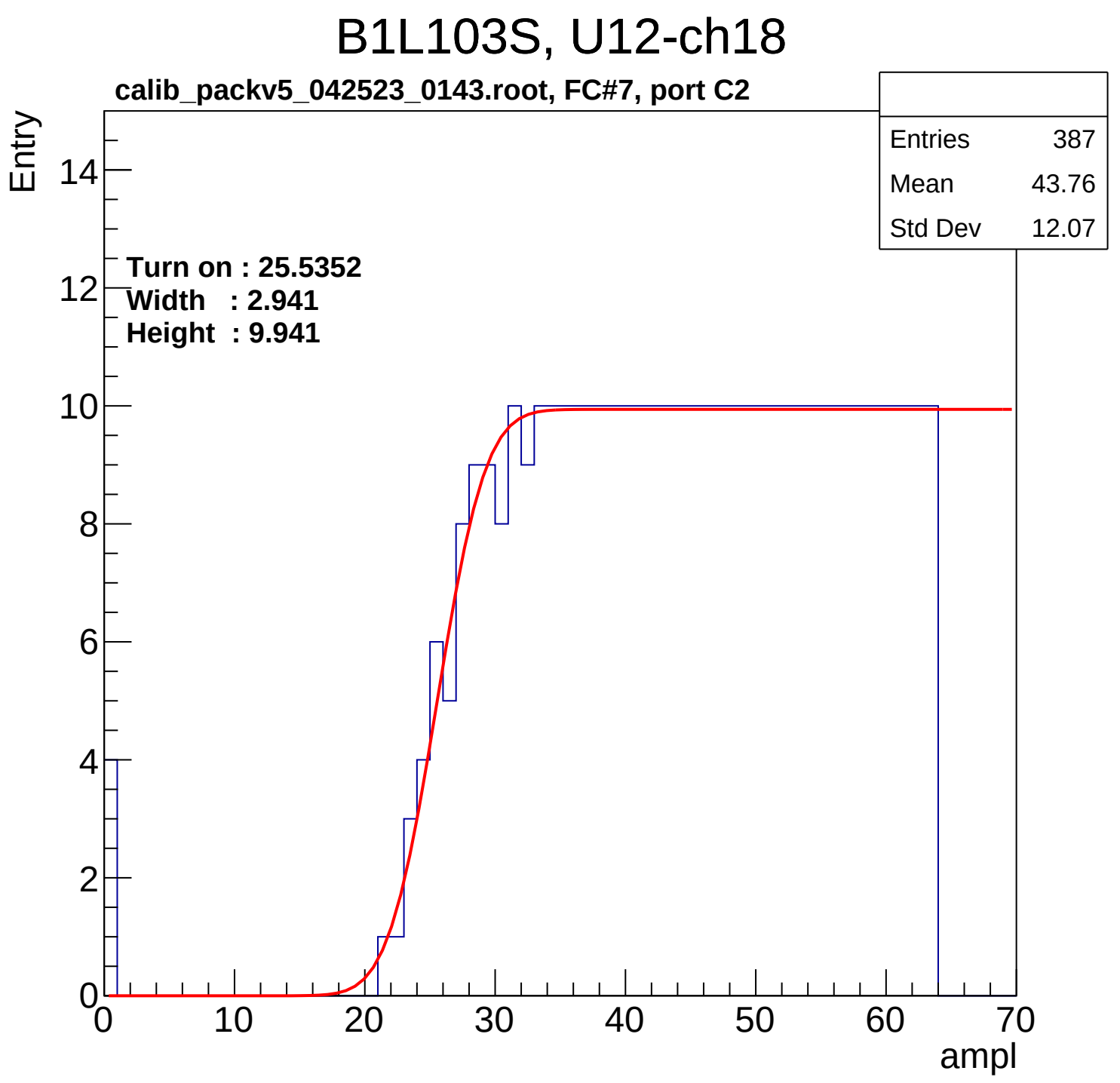

B1L103S, U12-ch13
calib_packv5_042523_0143.root, FC#7, port C2
Entries 367
Mean 44.96
Std Dev 11
Turn on : 27.6243
Width : 3.164
Height : 10.033
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

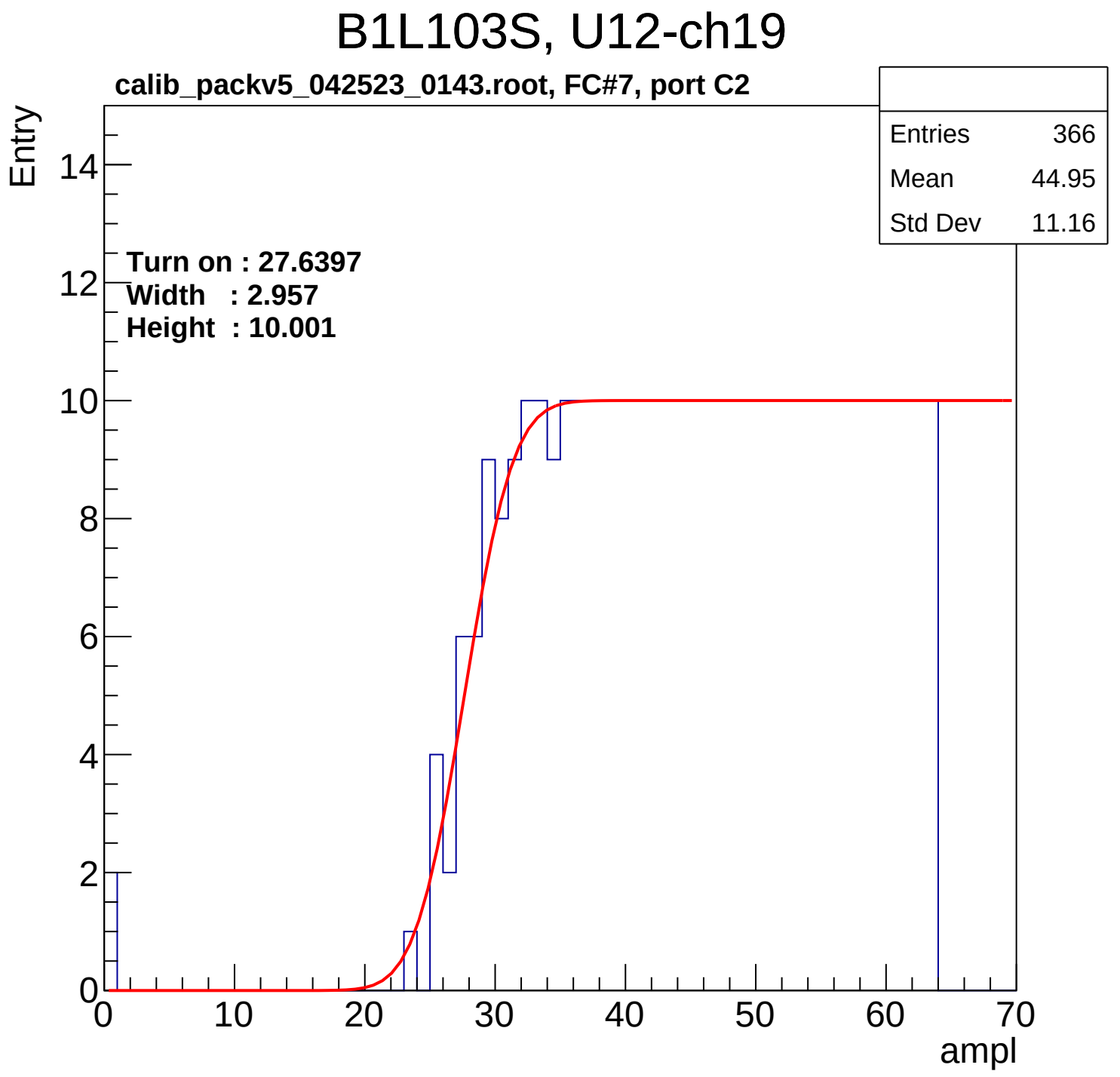

B1L103S, U12-ch14
calib_packv5_042523_0143.root, FC#7, port C2
Entries 356
Mean 45.27
Std Dev 11.37
Turn on : 28.5275
Width : 1.917
Height : 9.879
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

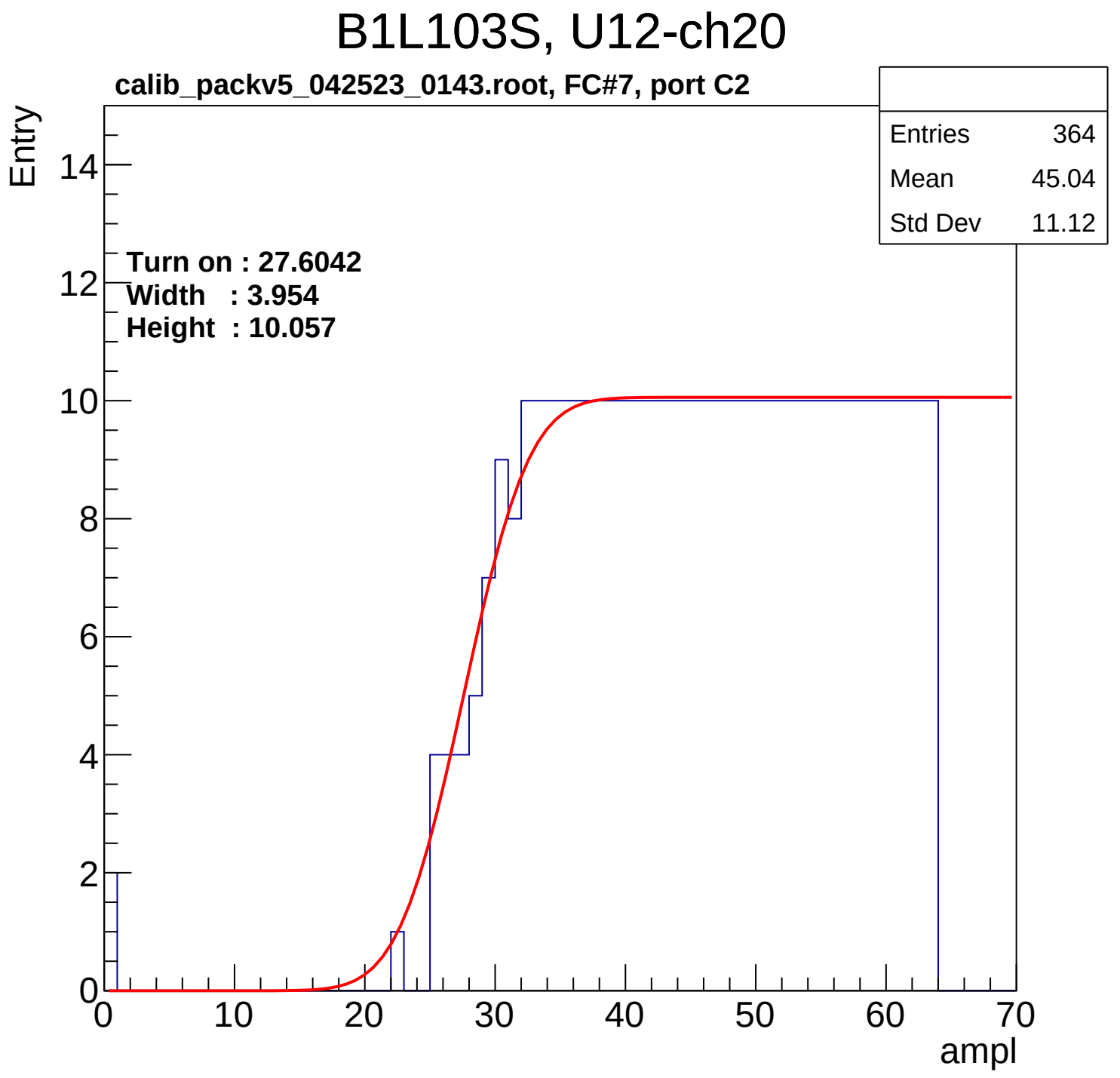

B1L103S, U12-ch15
calib_packv5_042523_0143.root, FC#7, port C2
Entries 364
Mean 45.11
Std Dev 10.92
Turn on : 28.3124
Width : 3.722
Height : 10.098
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

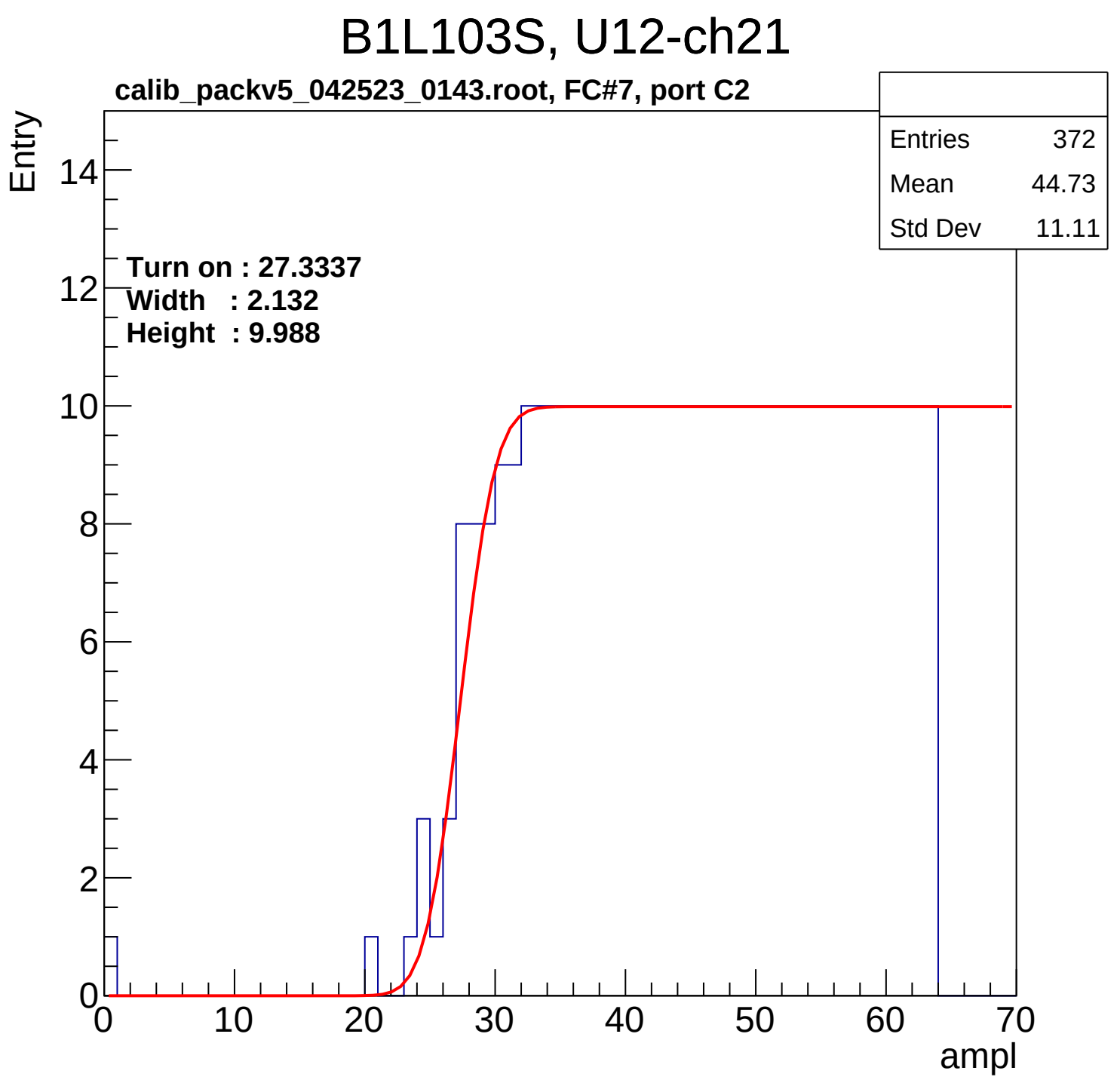

B1L103S, U12-ch16
calib_packv5_042523_0143.root, FC#7, port C2
Entries 362
Mean 45.17
Std Dev 11.02
Turn on : 27.6423
Width : 2.763
Height : 9.994
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

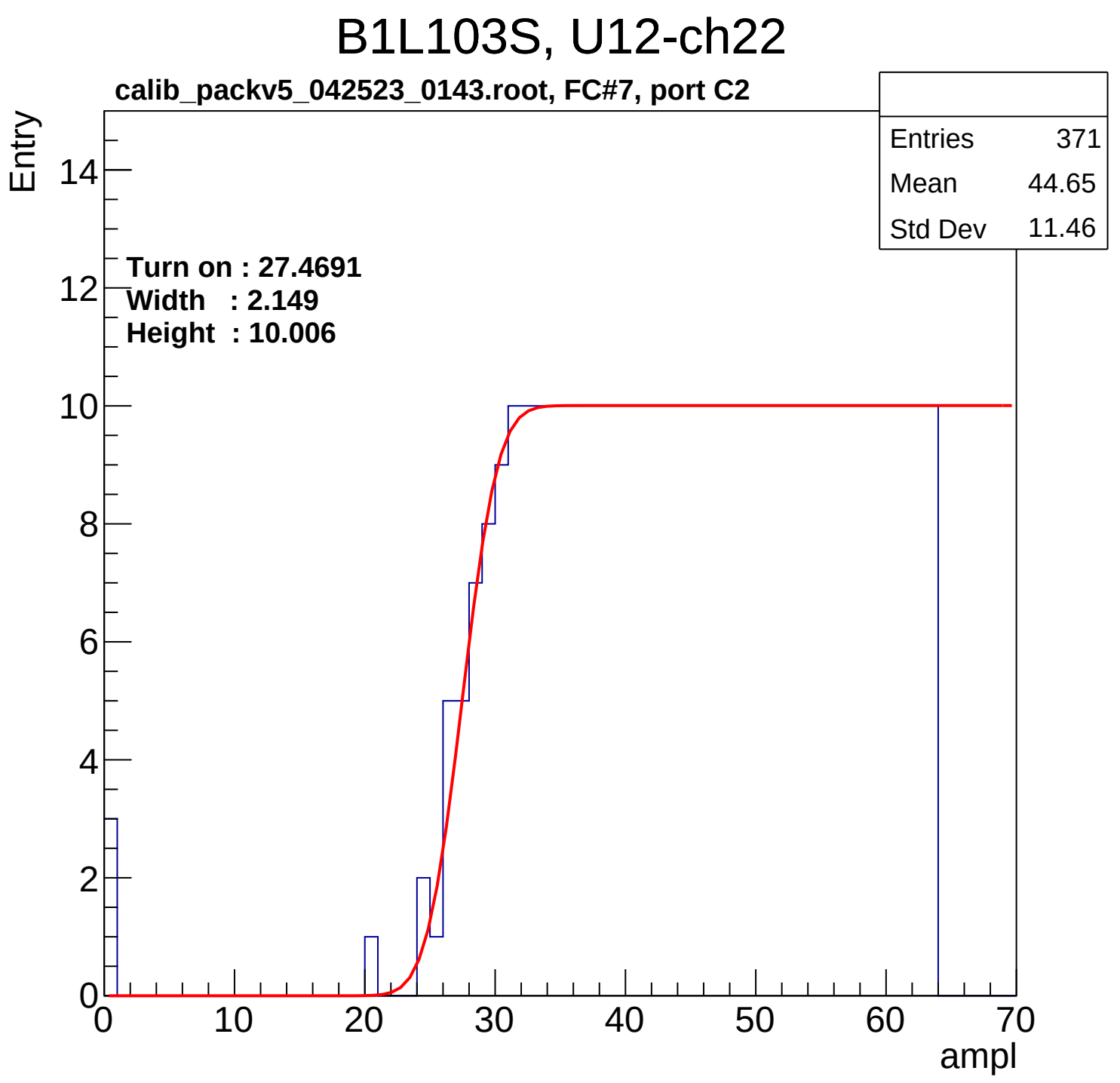

B1L103S, U12-ch17
calib_packv5_042523_0143.root, FC#7, port C2
Entries 362
Mean 45.16
Std Dev 11.04
Turn on : 28.1297
Width : 3.021
Height : 10.025
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

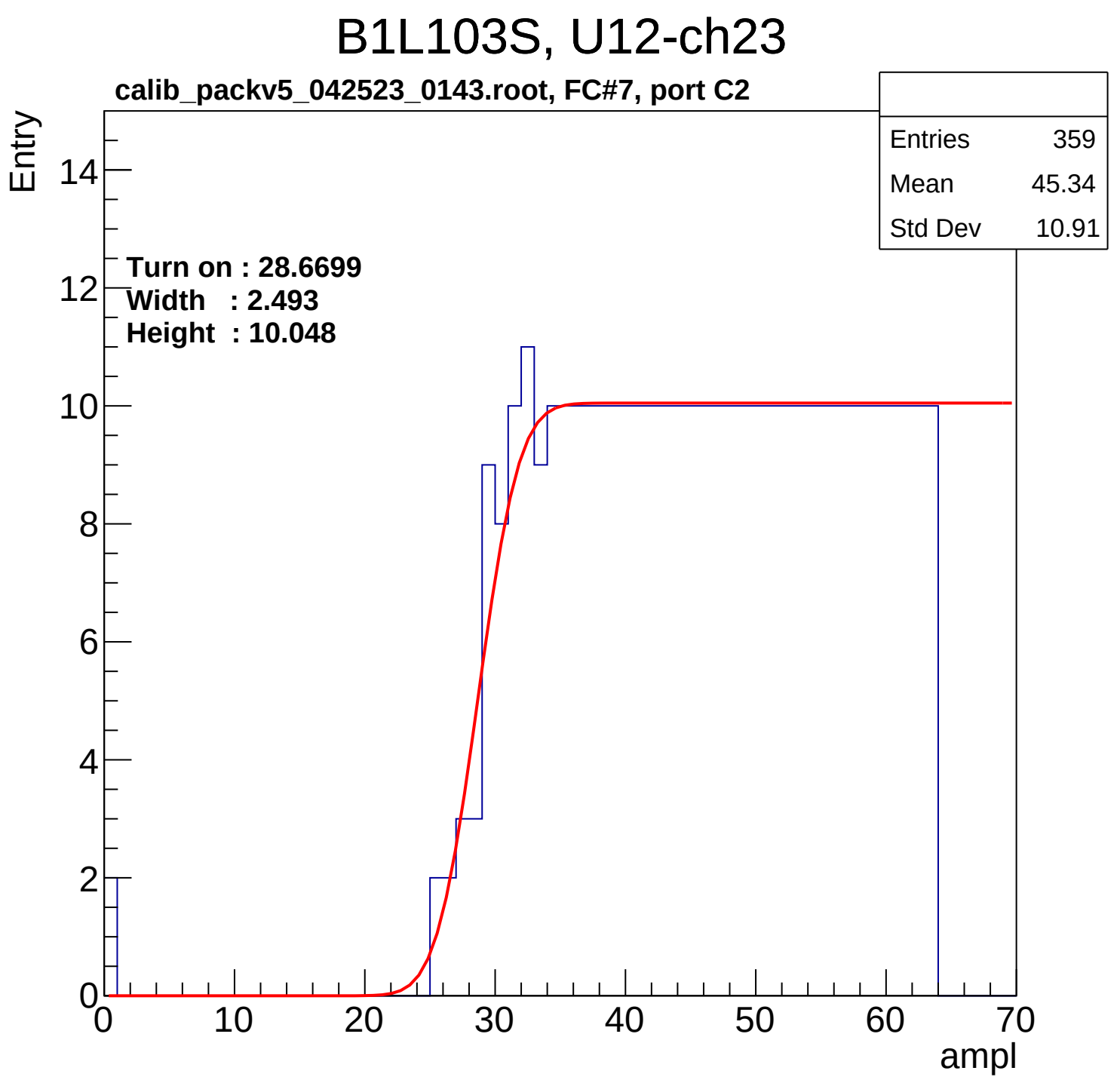

B1L103S, U12-ch18
calib_packv5_042523_0143.root, FC#7, port C2
Entries 387
Mean 43.76
Std Dev 12.07
Turn on : 25.5352
Width : 2.941
Height : 9.941
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

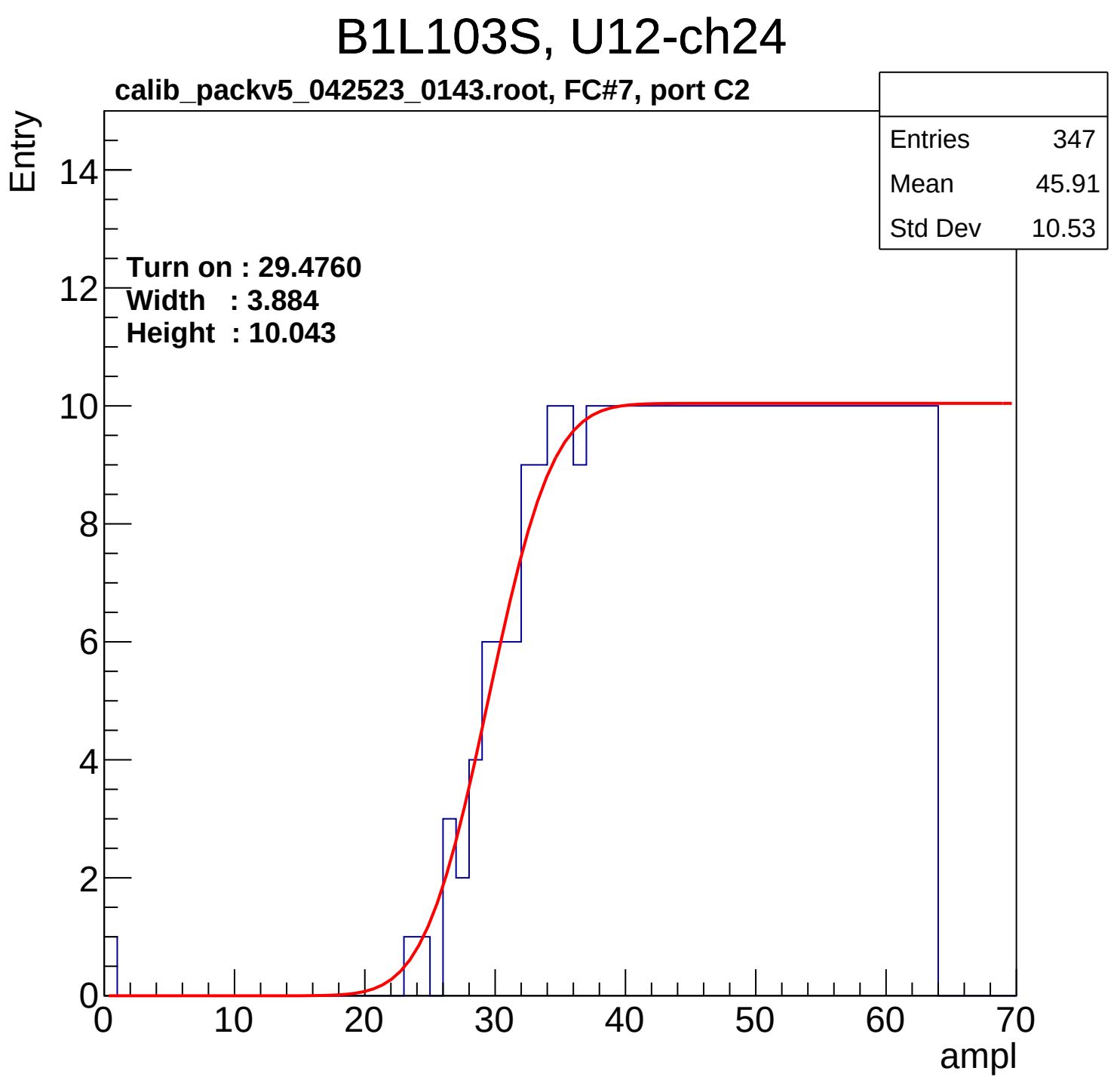

B1L103S, U12-ch19
calib_packv5_042523_0143.root, FC#7, port C2
Entries 366
Mean 44.95
Std Dev 11.16
Turn on : 27.6397
Width : 2.957
Height : 10.001
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

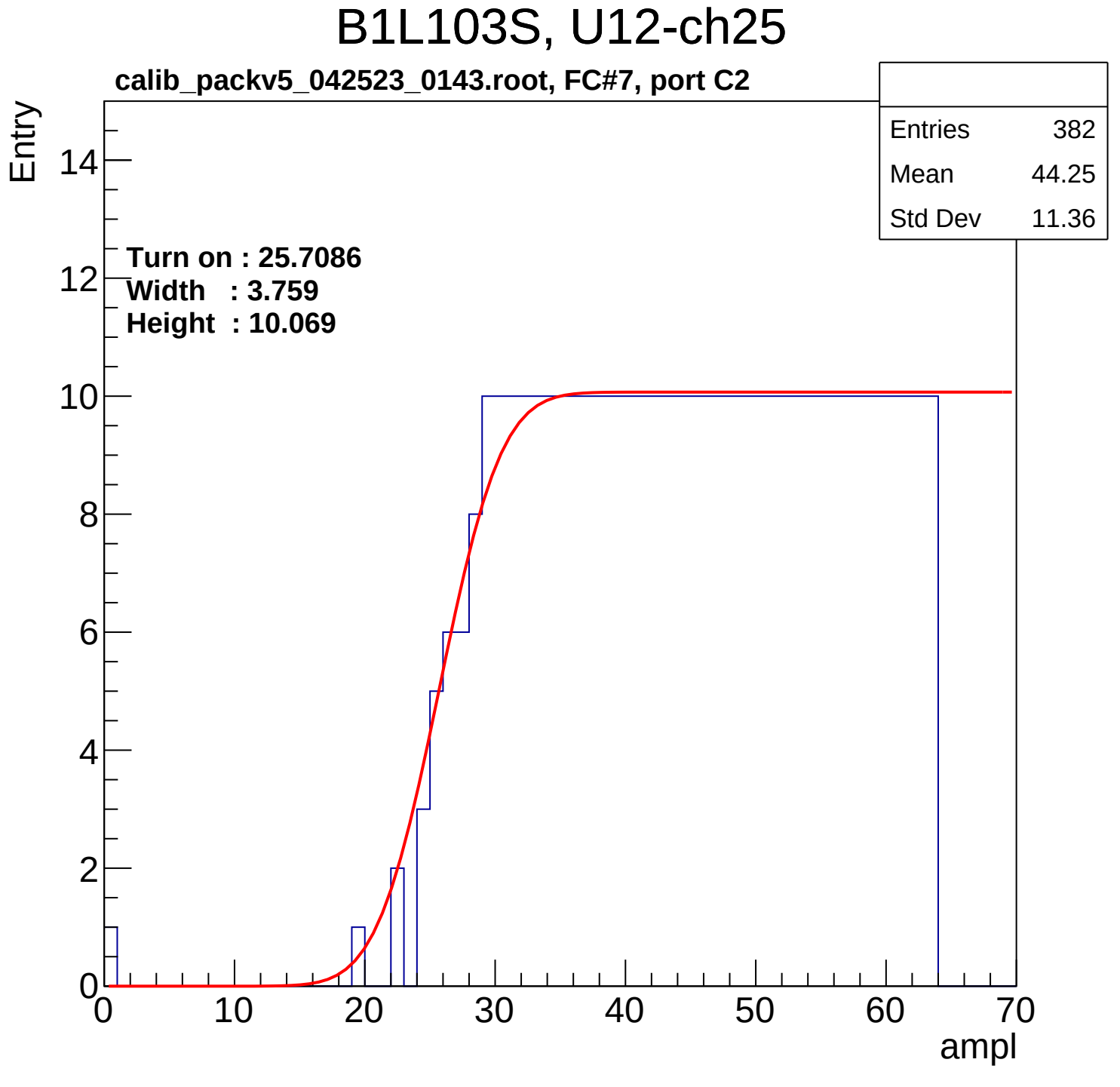

B1L103S, U12-ch20
calib_packv5_042523_0143.root, FC#7, port C2
Entries 364
Mean 45.04
Std Dev 11.12
Turn on : 27.6042
Width : 3.954
Height : 10.057
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

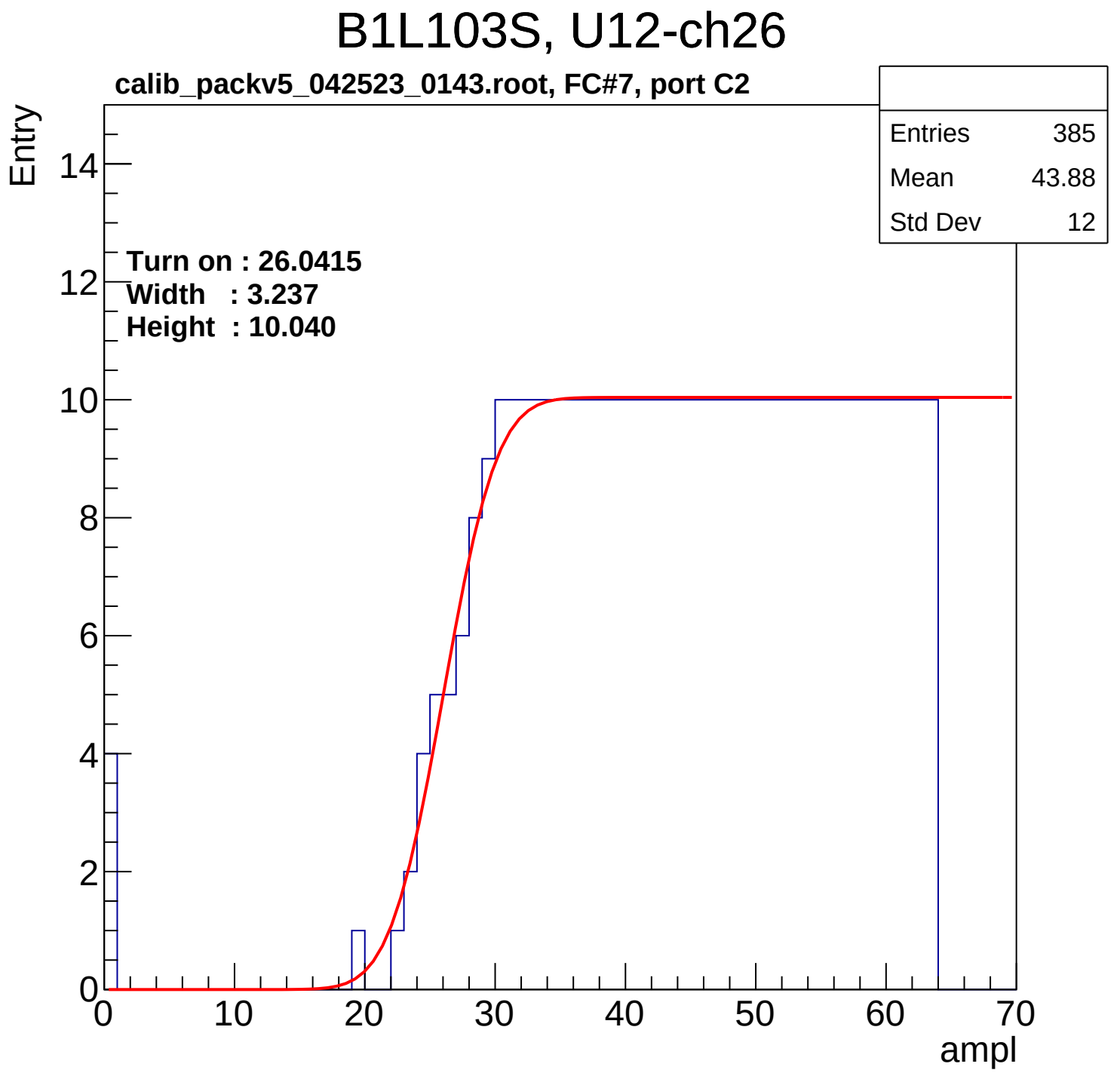

B1L103S, U12-ch21
calib_packv5_042523_0143.root, FC#7, port C2
Entries 372
Mean 44.73
Std Dev 11.11
Turn on : 27.3337
Width : 2.132
Height : 9.988
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

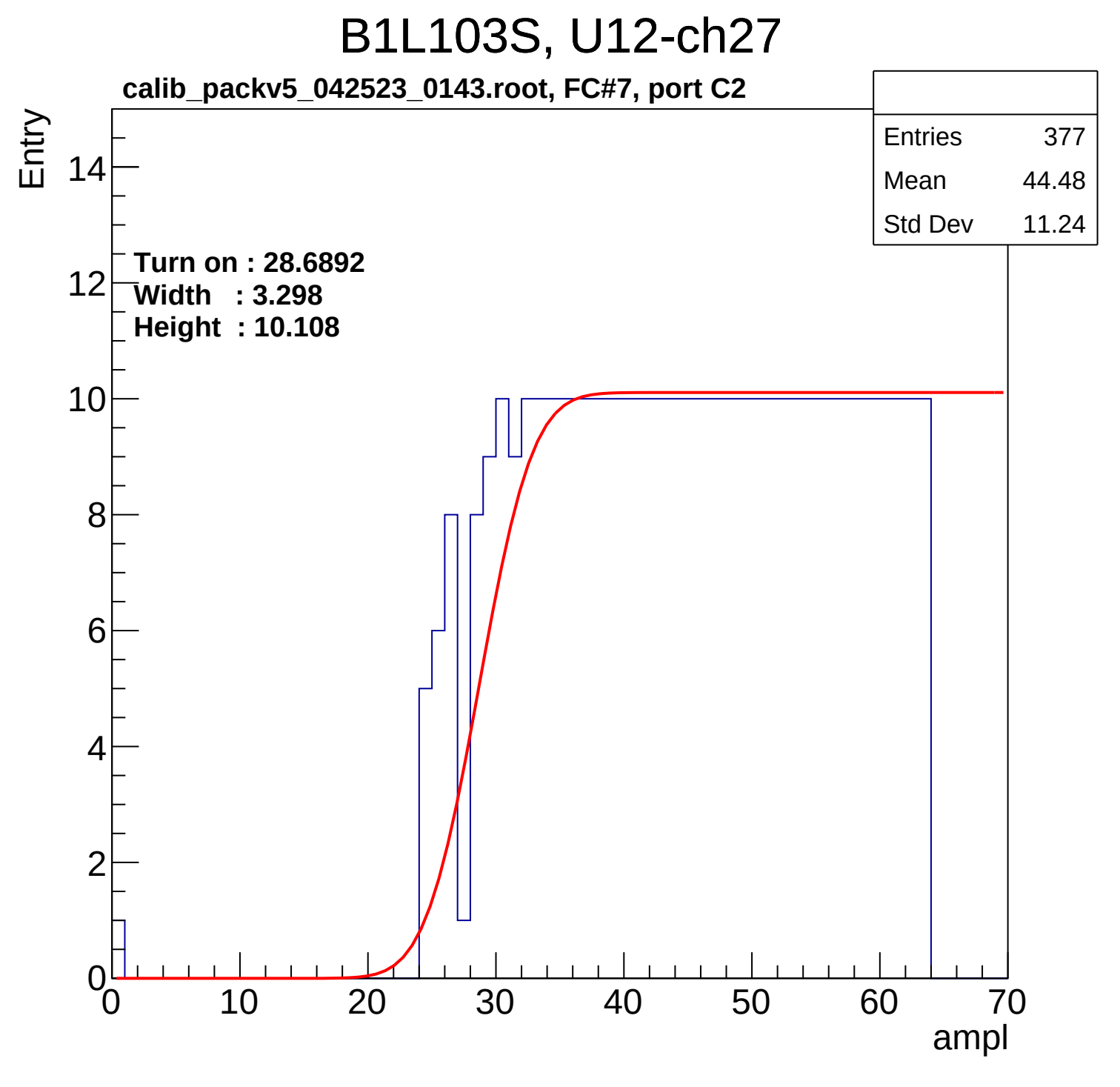

B1L103S, U12-ch22
calib_packv5_042523_0143.root, FC#7, port C2
Entries 371
Mean 44.65
Std Dev 11.46
Turn on : 27.4691
Width : 2.149
Height : 10.006
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

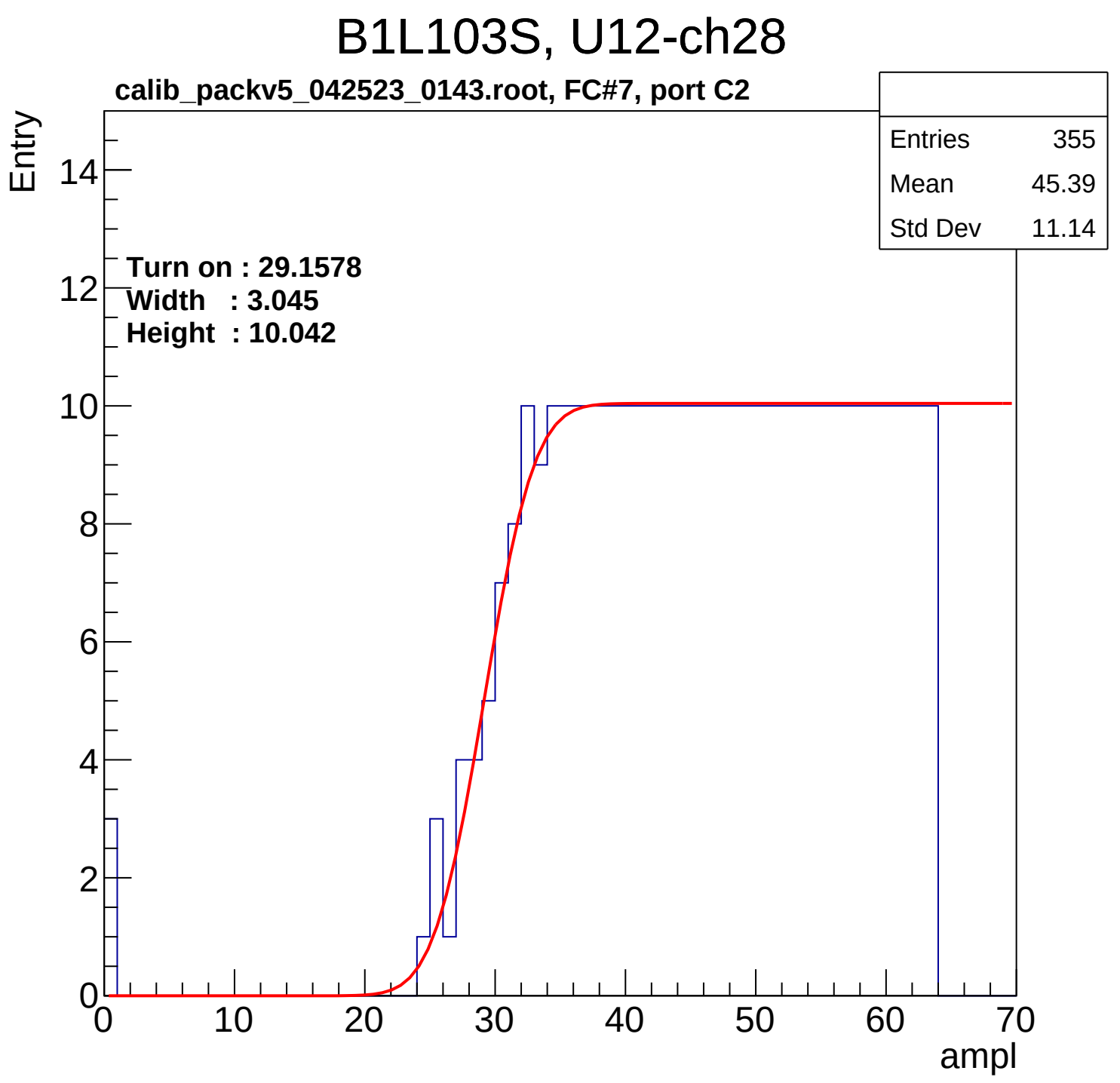

B1L103S, U12-ch23
calib_packv5_042523_0143.root, FC#7, port C2
Entries 359
Mean 45.34
Std Dev 10.91
Turn on : 28.6699
Width : 2.493
Height : 10.048
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

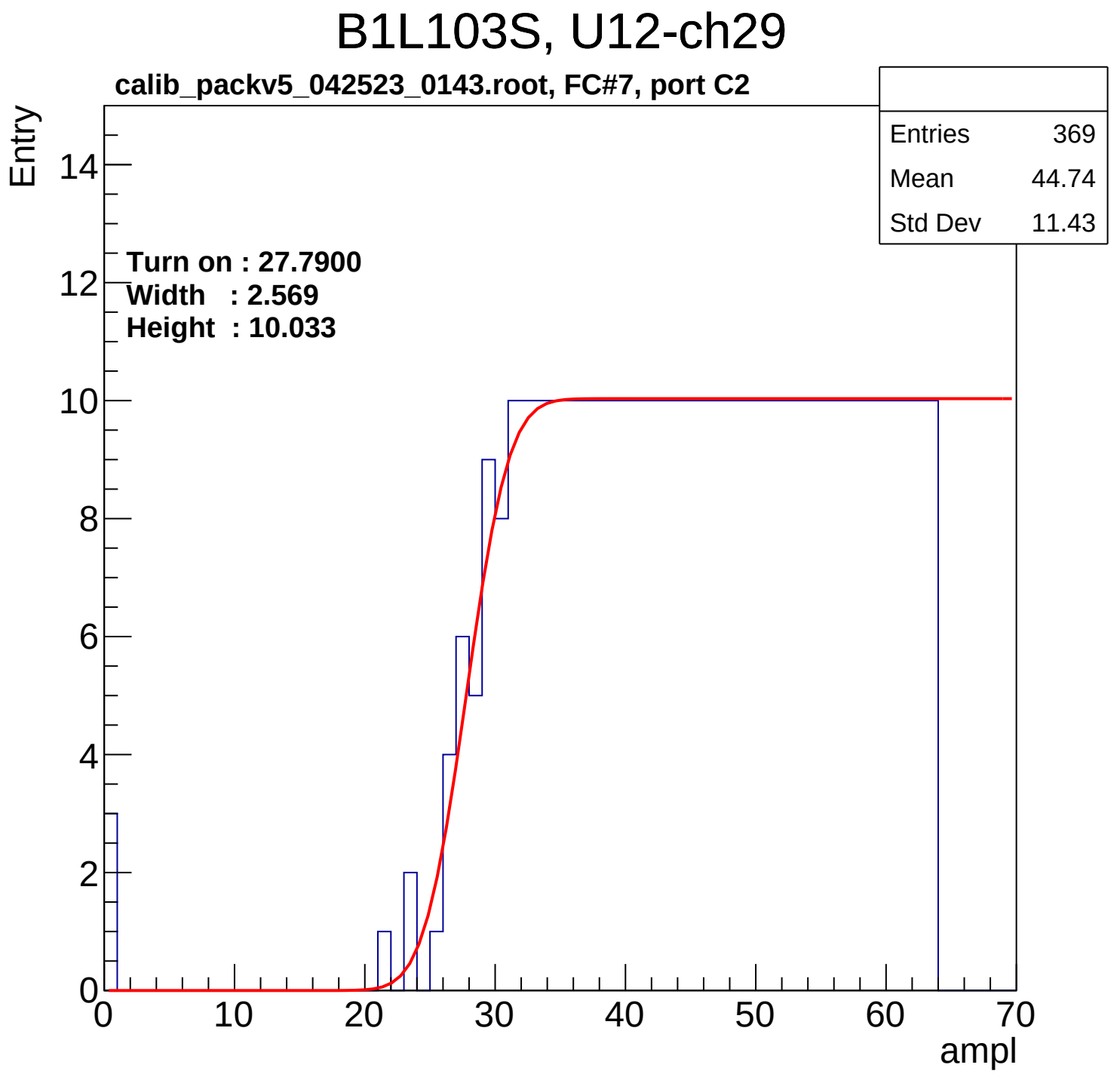

B1L103S, U12-ch24
calib_packv5_042523_0143.root, FC#7, port C2
Entries 347
Mean 45.91
Std Dev 10.53
Turn on : 29.4760
Width : 3.884
Height : 10.043
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

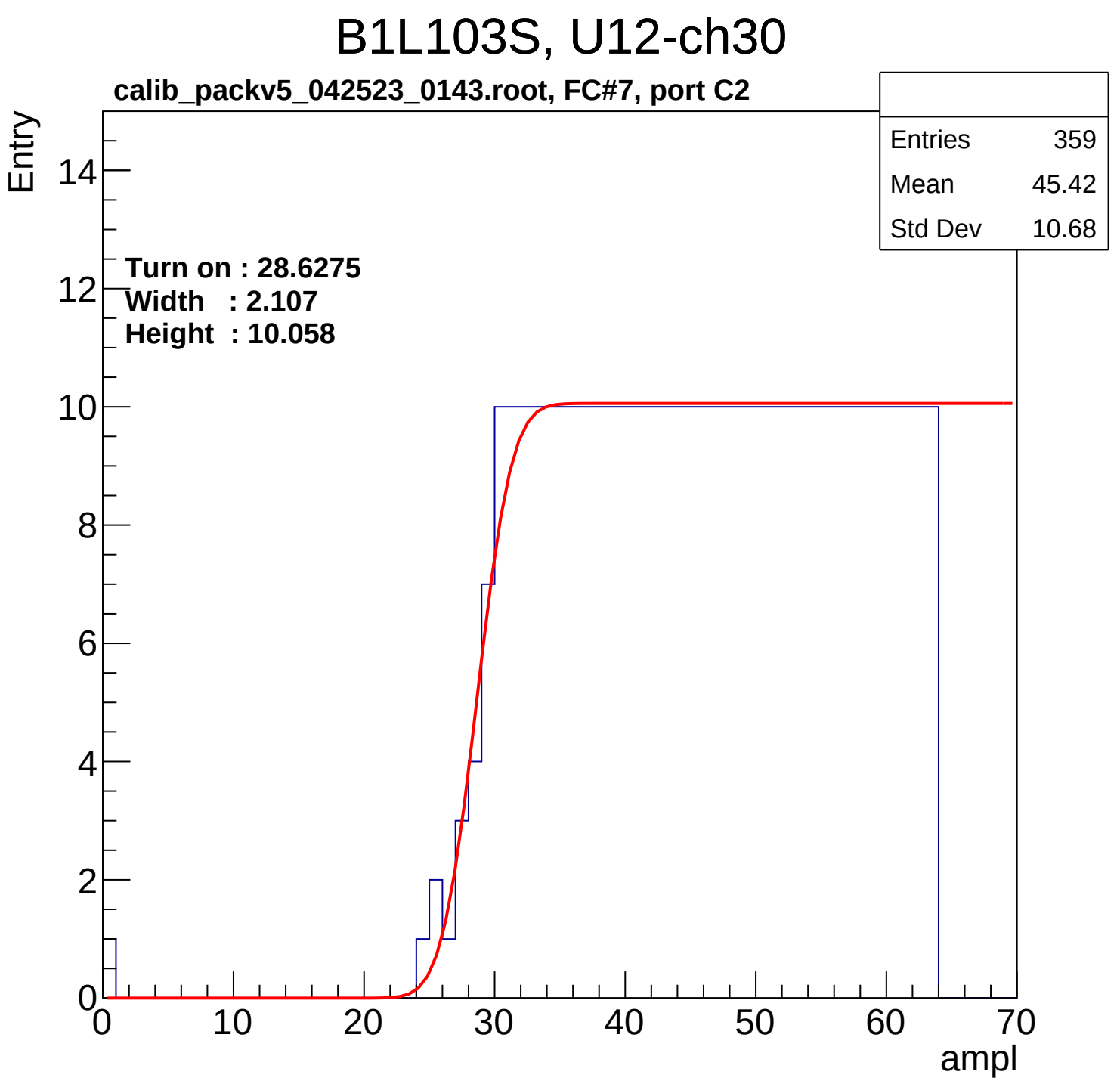

B1L103S, U12-ch25
calib_packv5_042523_0143.root, FC#7, port C2
Entries 382
Mean 44.25
Std Dev 11.36
Turn on : 25.7086
Width : 3.759
Height : 10.069
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

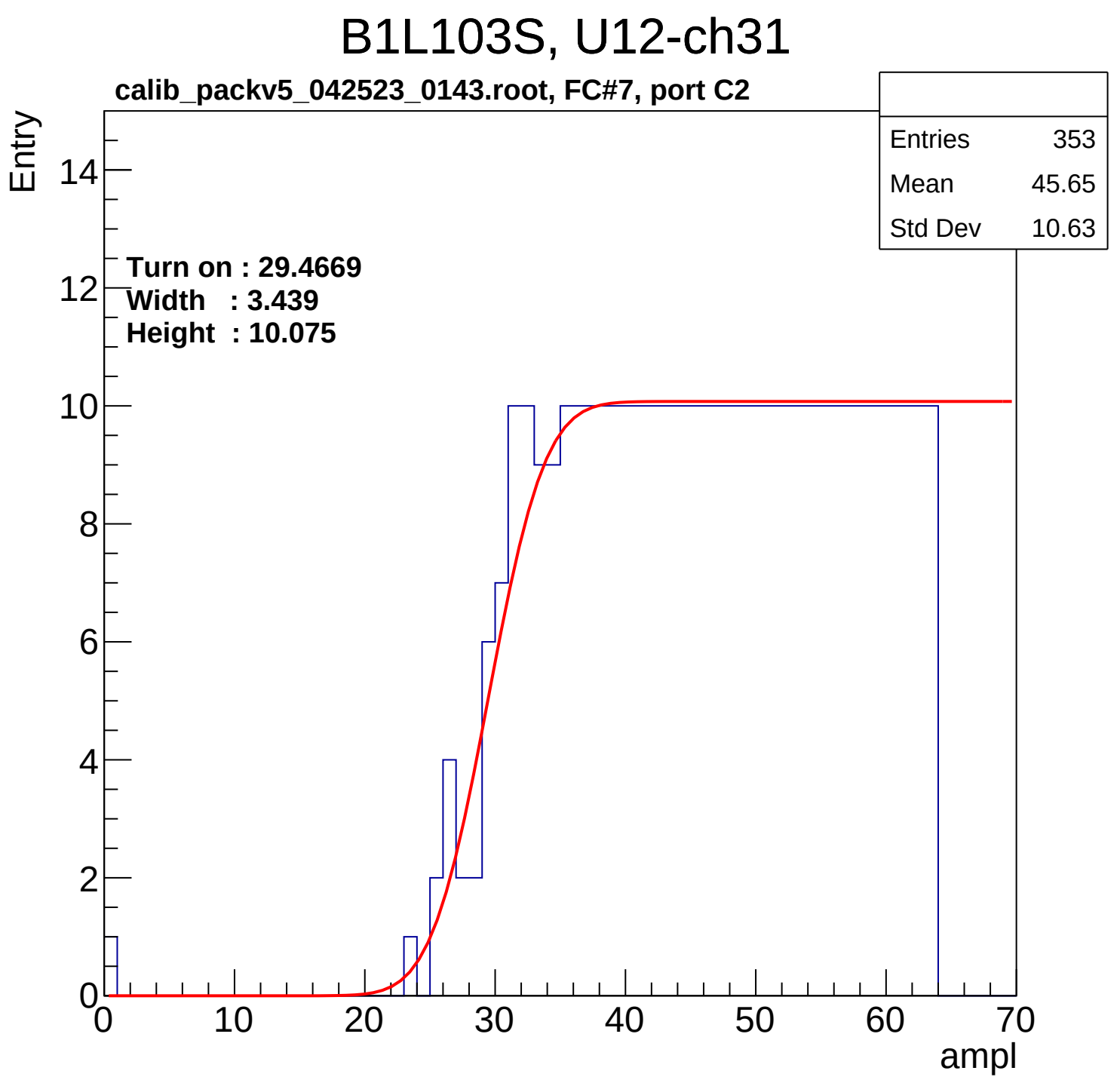

B1L103S, U12-ch26
calib_packv5_042523_0143.root, FC#7, port C2
Entries 385
Mean 43.88
Std Dev 12
Turn on : 26.0415
Width : 3.237
Height : 10.040
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

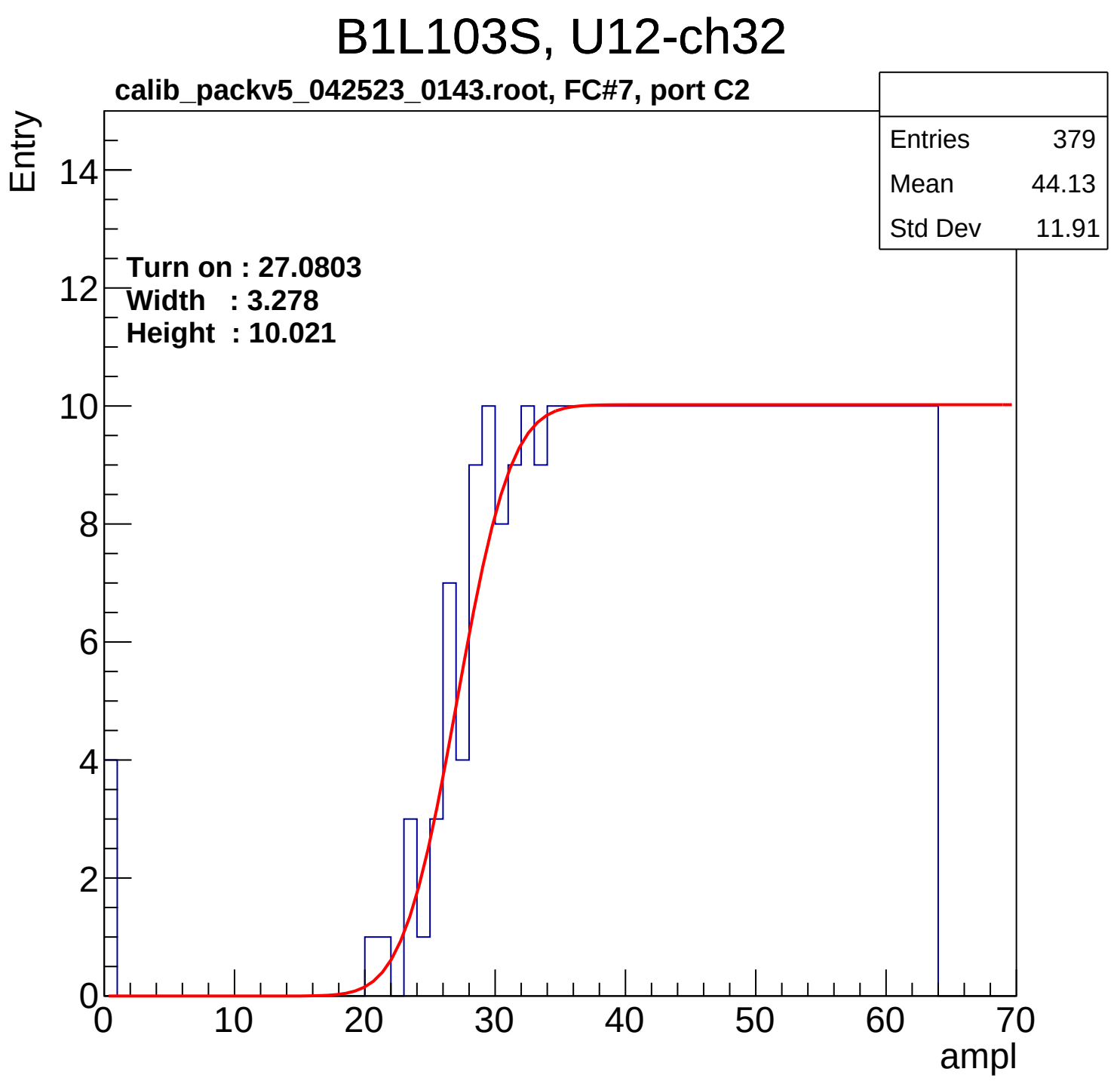

B1L103S, U12-ch27
calib_packv5_042523_0143.root, FC#7, port C2
Entries 377
Mean 44.48
Std Dev 11.24
Turn on : 28.6892
Width : 3.298
Height : 10.108
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

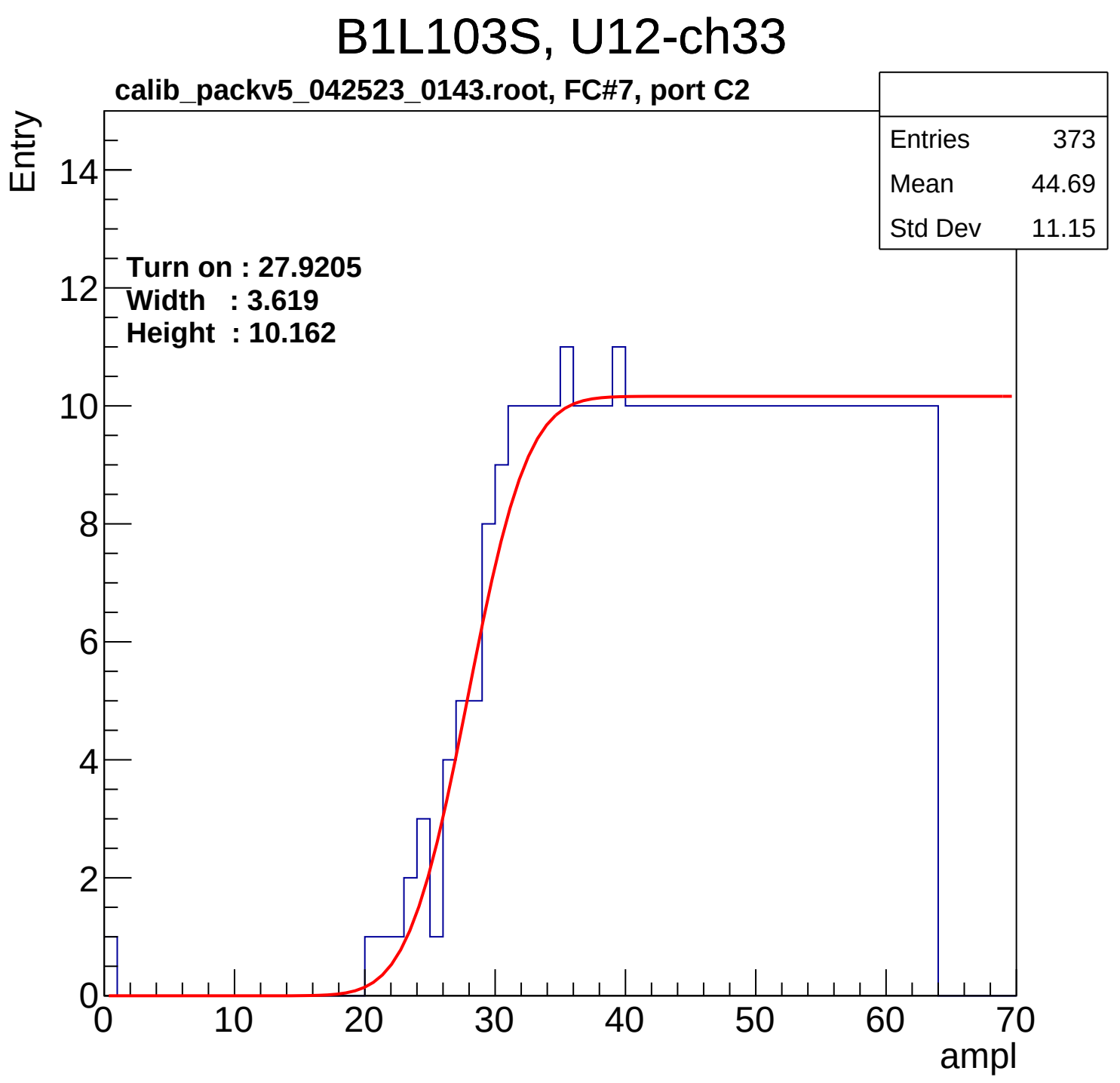

B1L103S, U12-ch28
calib_packv5_042523_0143.root, FC#7, port C2
Entries 355
Mean 45.39
Std Dev 11.14
Turn on : 29.1578
Width : 3.045
Height : 10.042
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

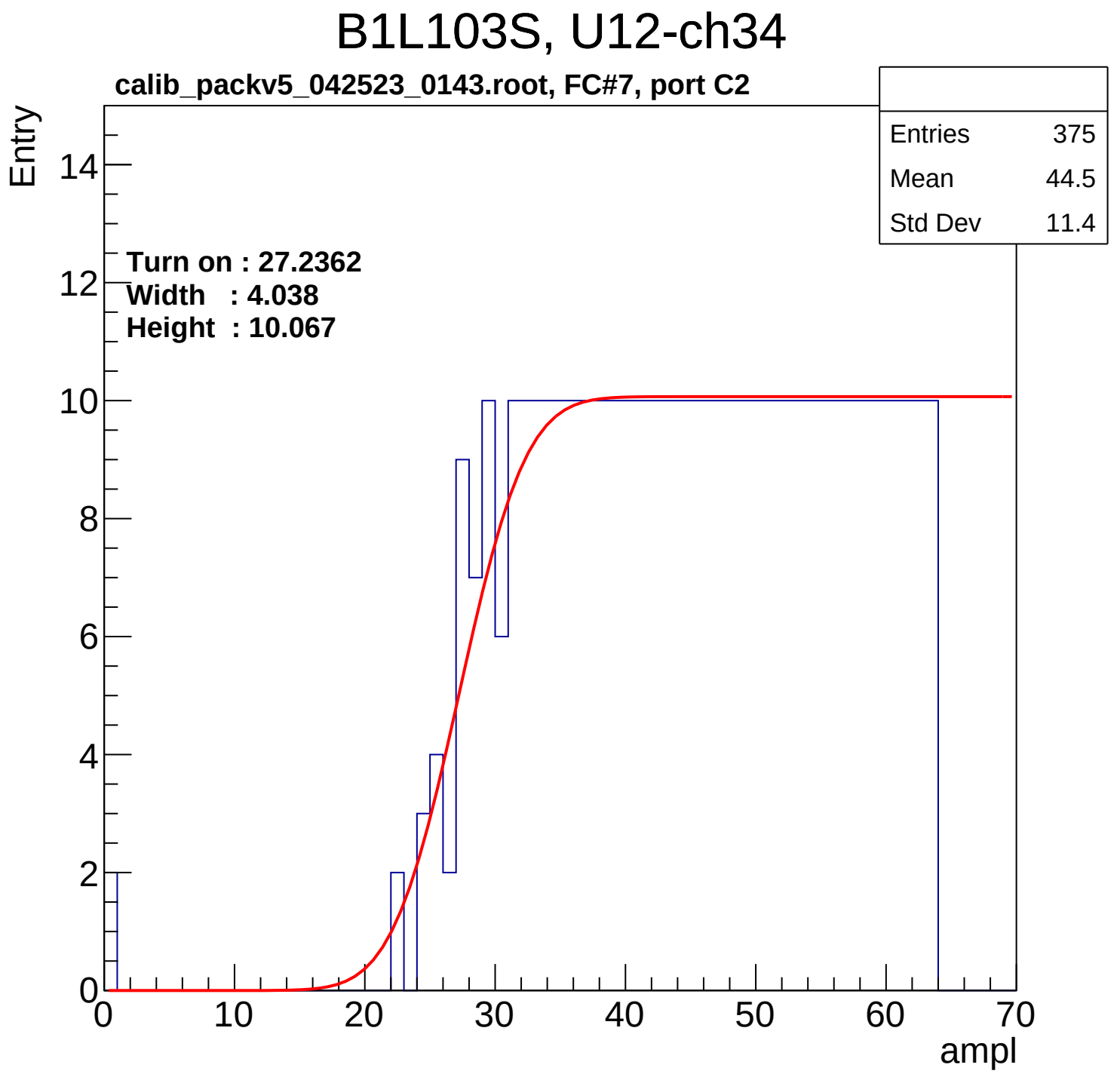

B1L103S, U12-ch29
calib_packv5_042523_0143.root, FC#7, port C2
Entries 369
Mean 44.74
Std Dev 11.43
Turn on : 27.7900
Width : 2.569
Height : 10.033
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

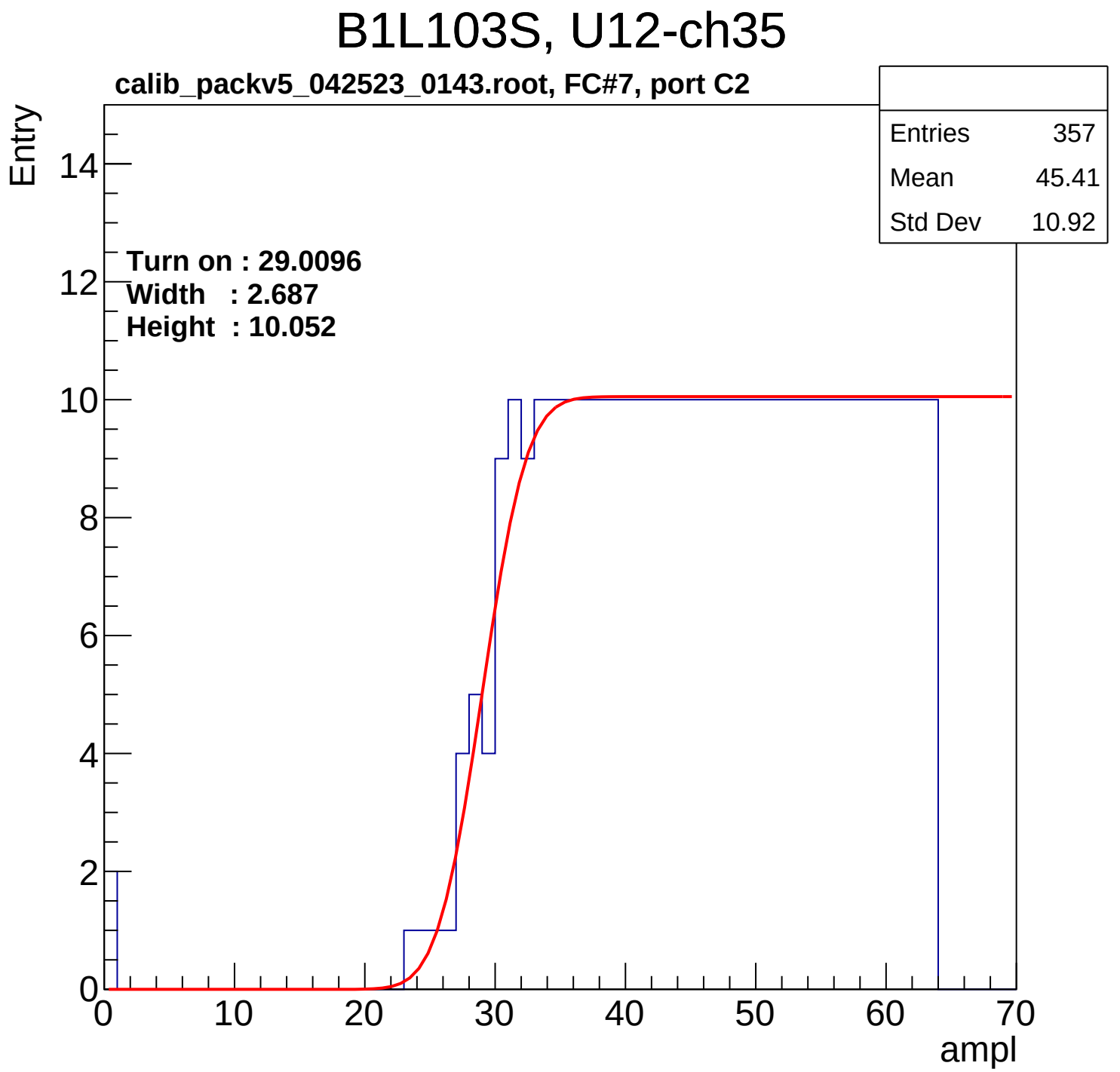

B1L103S, U12-ch30
calib_packv5_042523_0143.root, FC#7, port C2
Entries 359
Mean 45.42
Std Dev 10.68
Turn on : 28.6275
Width : 2.107
Height : 10.058
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

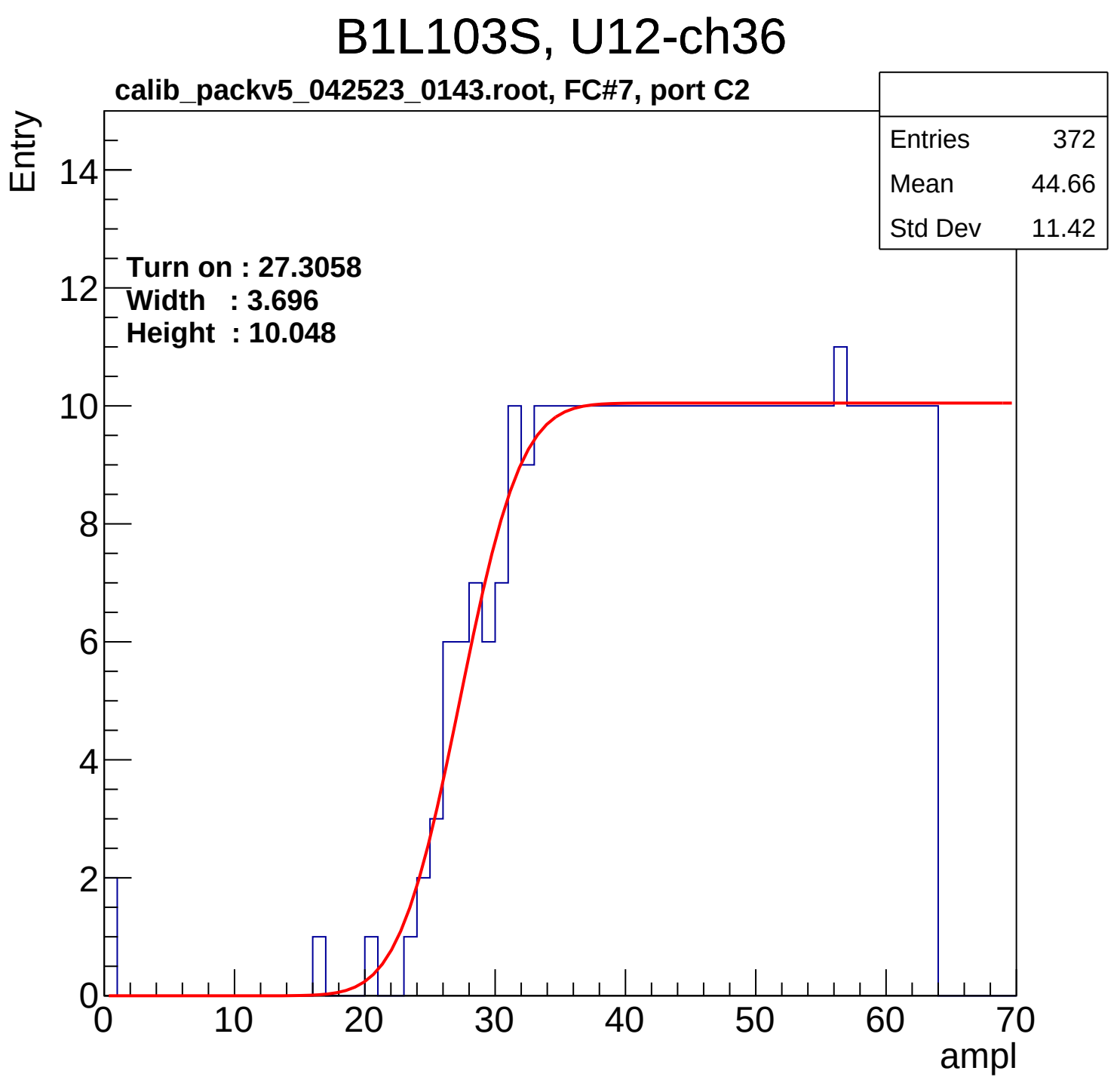

B1L103S, U12-ch31
calib_packv5_042523_0143.root, FC#7, port C2
Entries 353
Mean 45.65
Std Dev 10.63
Turn on : 29.4669
Width : 3.439
Height : 10.075
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

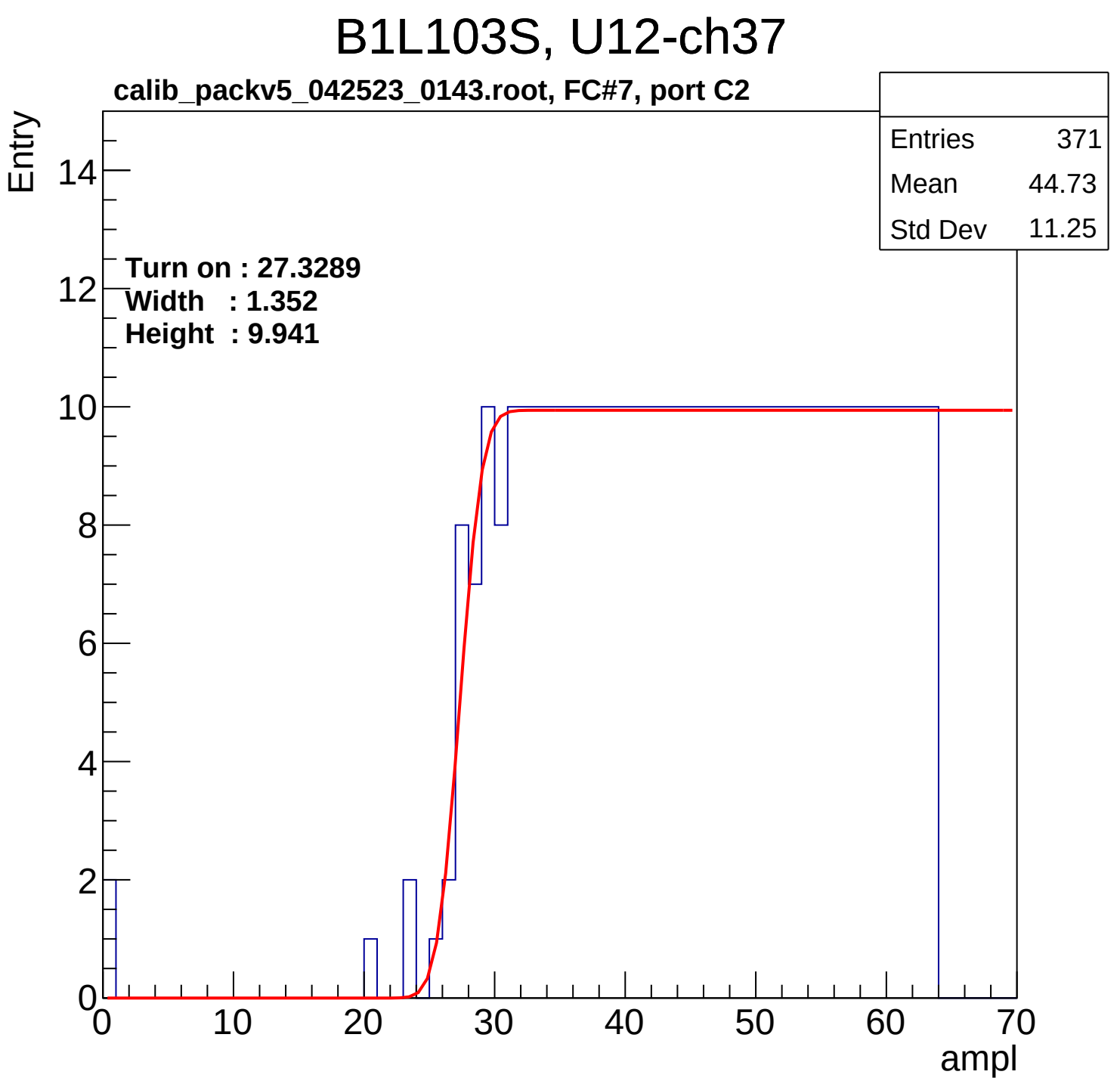

B1L103S, U12-ch32
calib_packv5_042523_0143.root, FC#7, port C2
Entries 379
Mean 44.13
Std Dev 11.91
Turn on : 27.0803
Width : 3.278
Height : 10.021
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

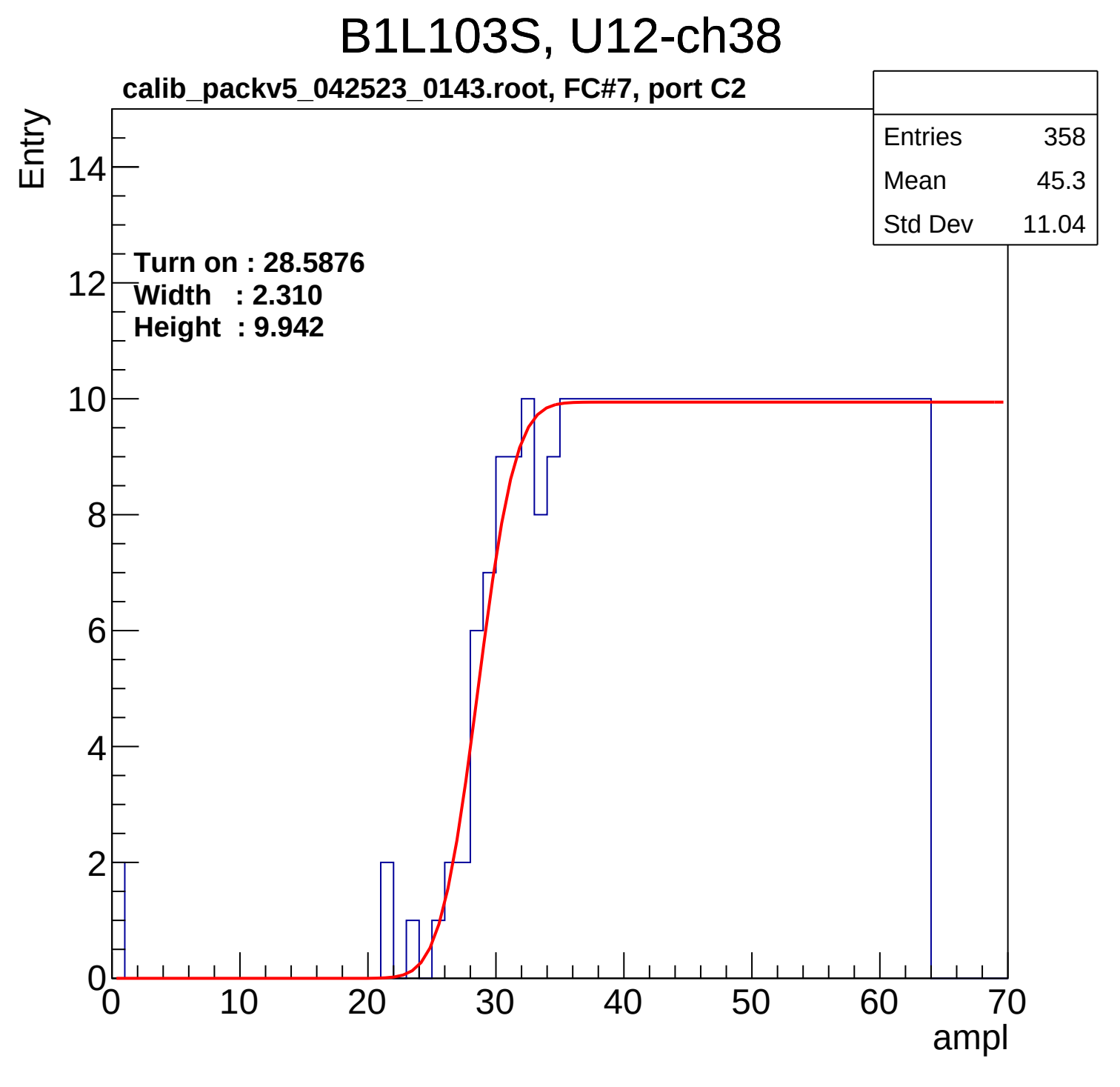

B1L103S, U12-ch33
calib_packv5_042523_0143.root, FC#7, port C2
Entries 373
Mean 44.69
Std Dev 11.15
Turn on : 27.9205
Width : 3.619
Height : 10.162
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

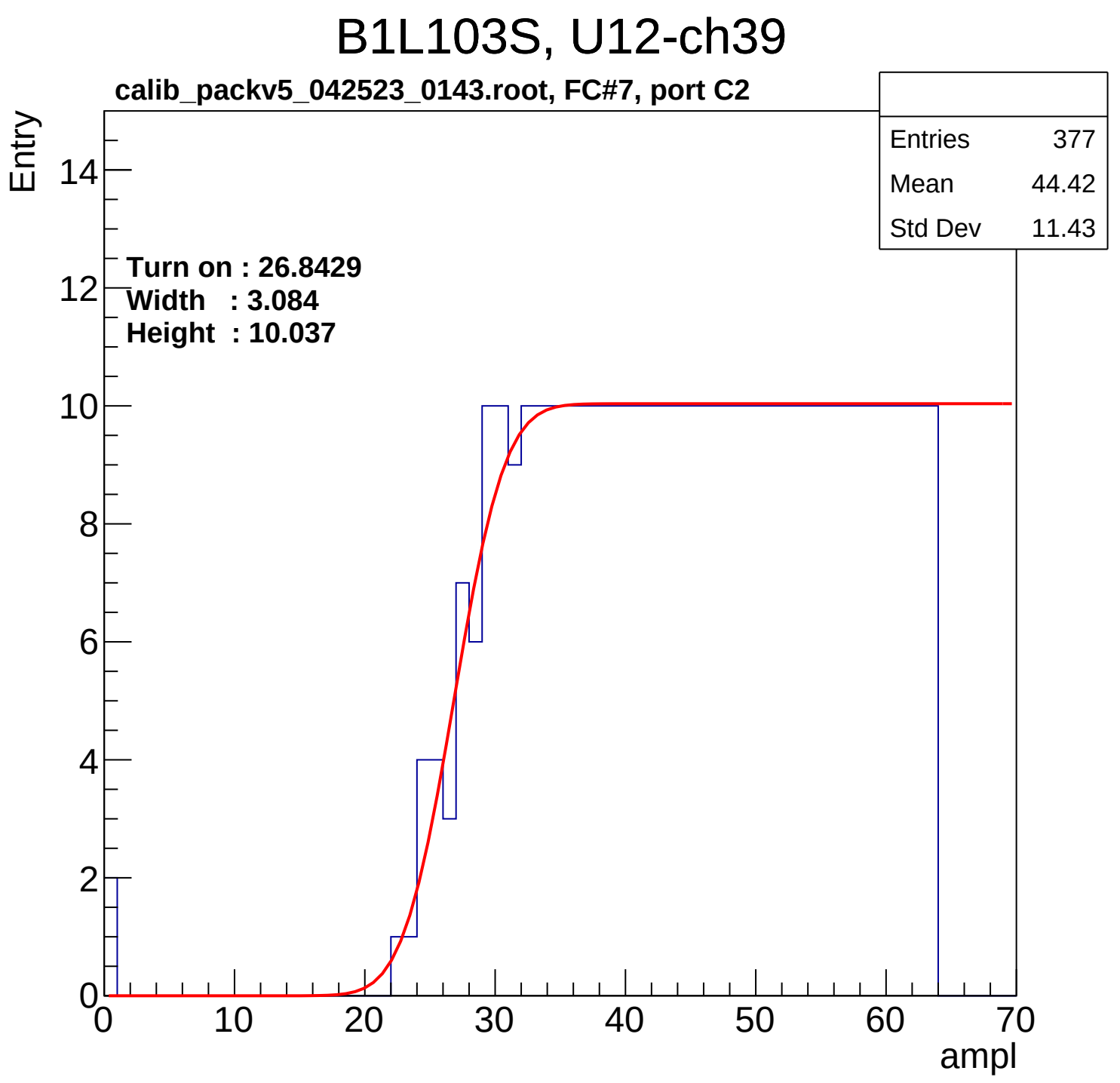

B1L103S, U12-ch34
calib_packv5_042523_0143.root, FC#7, port C2
Entries 375
Mean 44.5
Std Dev 11.4
Turn on : 27.2362
Width : 4.038
Height : 10.067
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

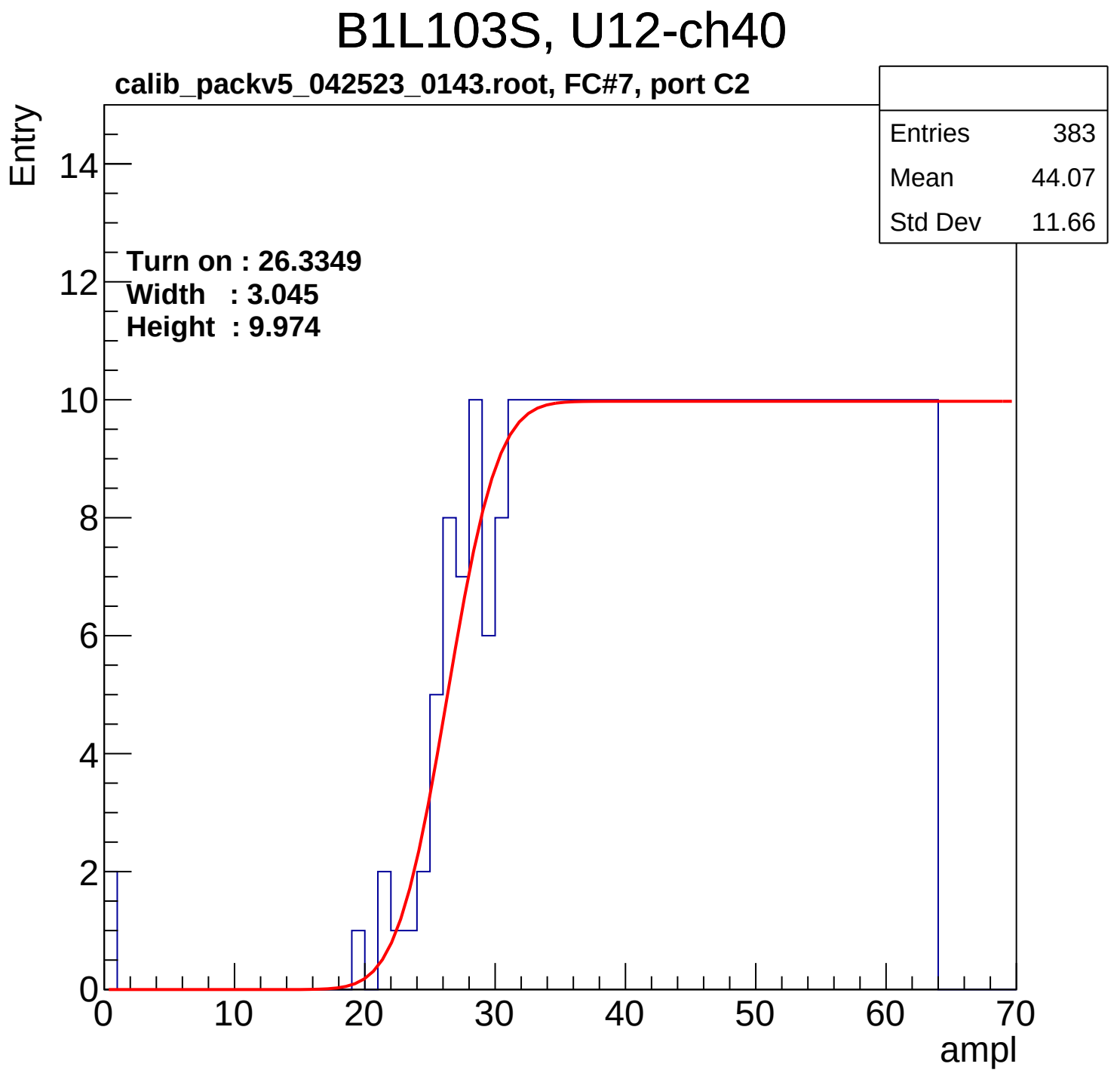

B1L103S, U12-ch35
calib_packv5_042523_0143.root, FC#7, port C2
Entries 357
Mean 45.41
Std Dev 10.92
Turn on : 29.0096
Width : 2.687
Height : 10.052
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

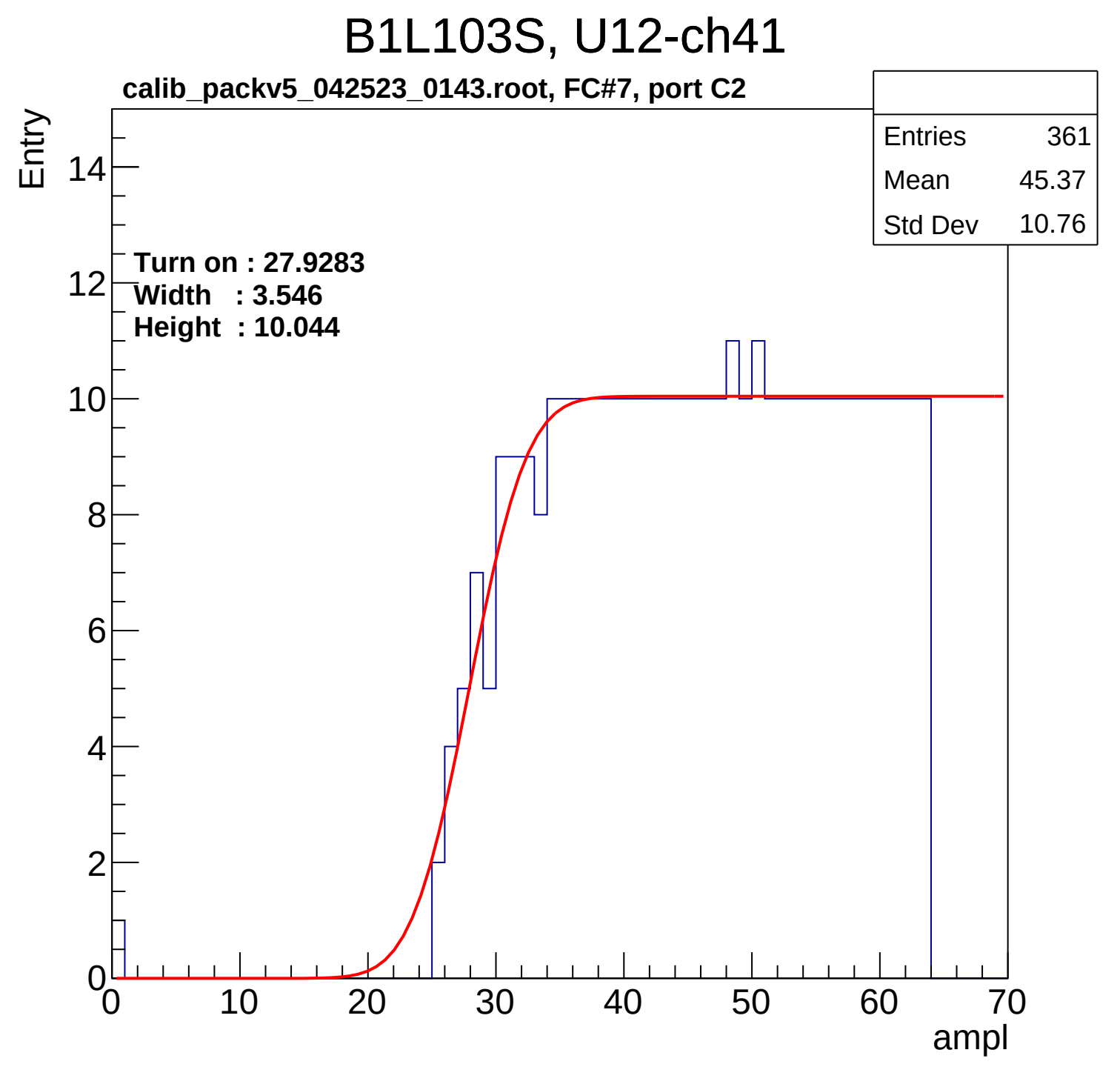

B1L103S, U12-ch36
calib_packv5_042523_0143.root, FC#7, port C2
Entries 372
Mean 44.66
Std Dev 11.42
Turn on : 27.3058
Width : 3.696
Height : 10.048
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

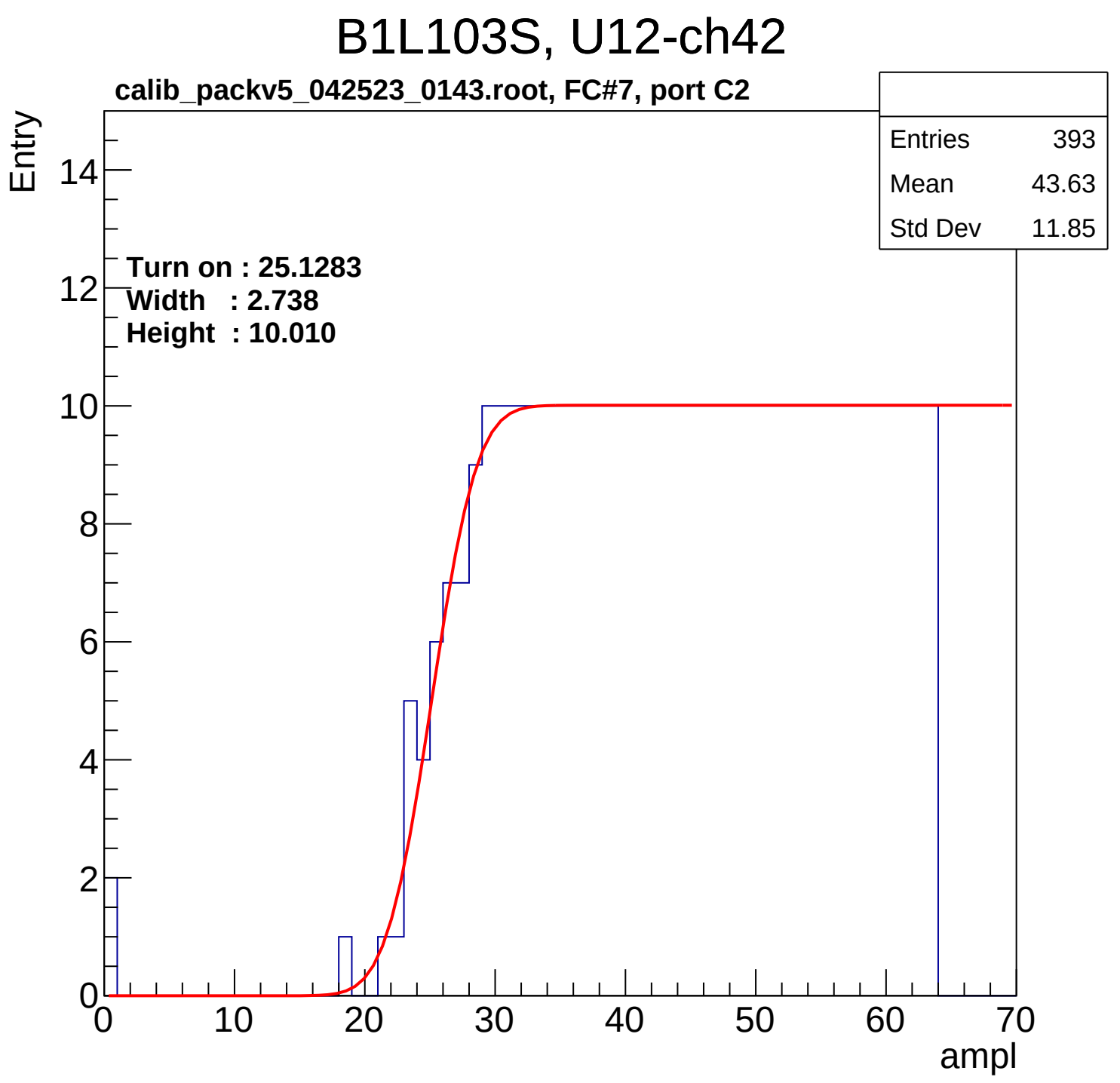

B1L103S, U12-ch37
calib_packv5_042523_0143.root, FC#7, port C2
Entries 371
Mean 44.73
Std Dev 11.25
Turn on : 27.3289
Width : 1.352
Height : 9.941
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

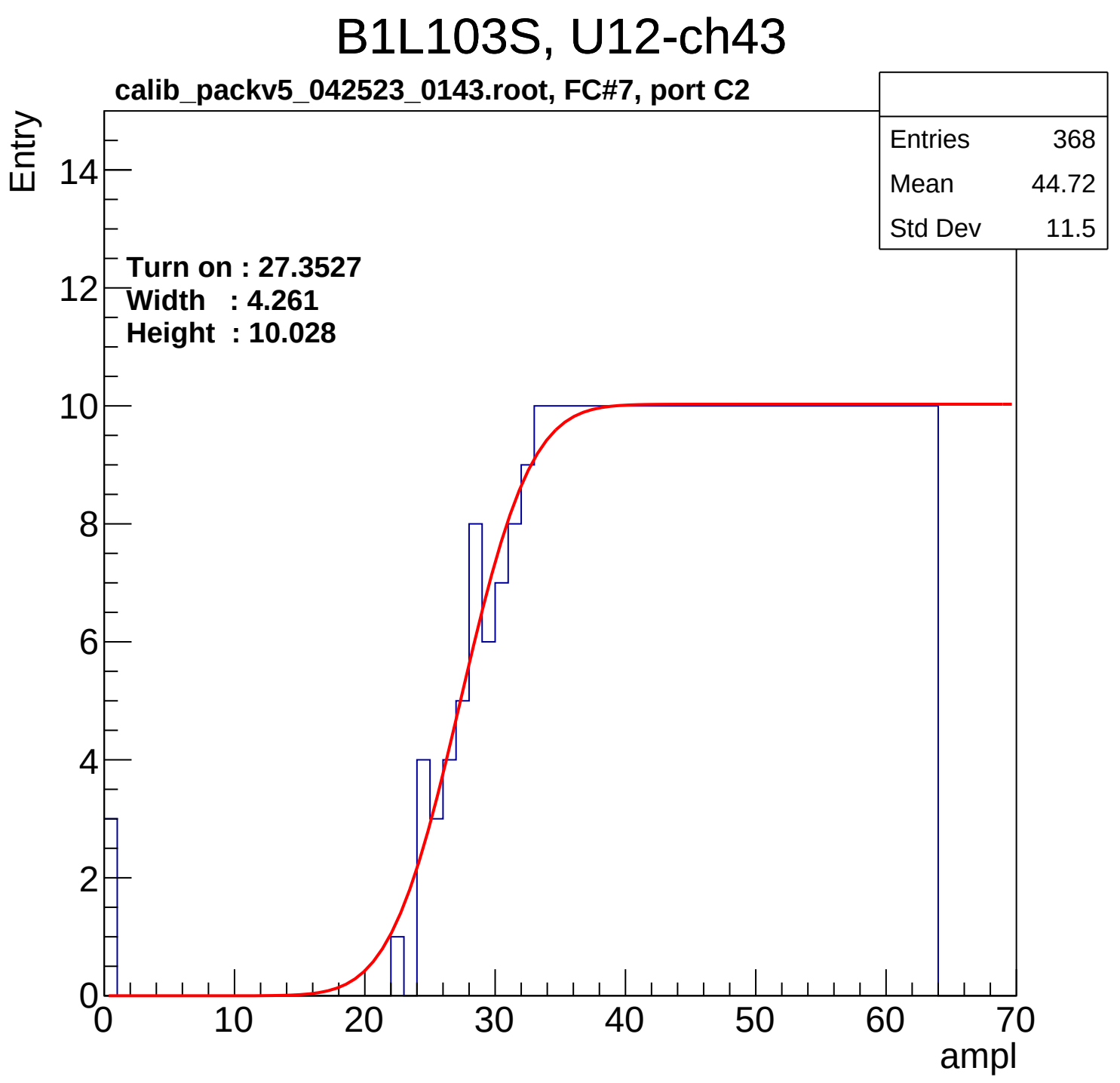

B1L103S, U12-ch38
calib_packv5_042523_0143.root, FC#7, port C2
Entries 358
Mean 45.3
Std Dev 11.04
Turn on : 28.5876
Width : 2.310
Height : 9.942
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

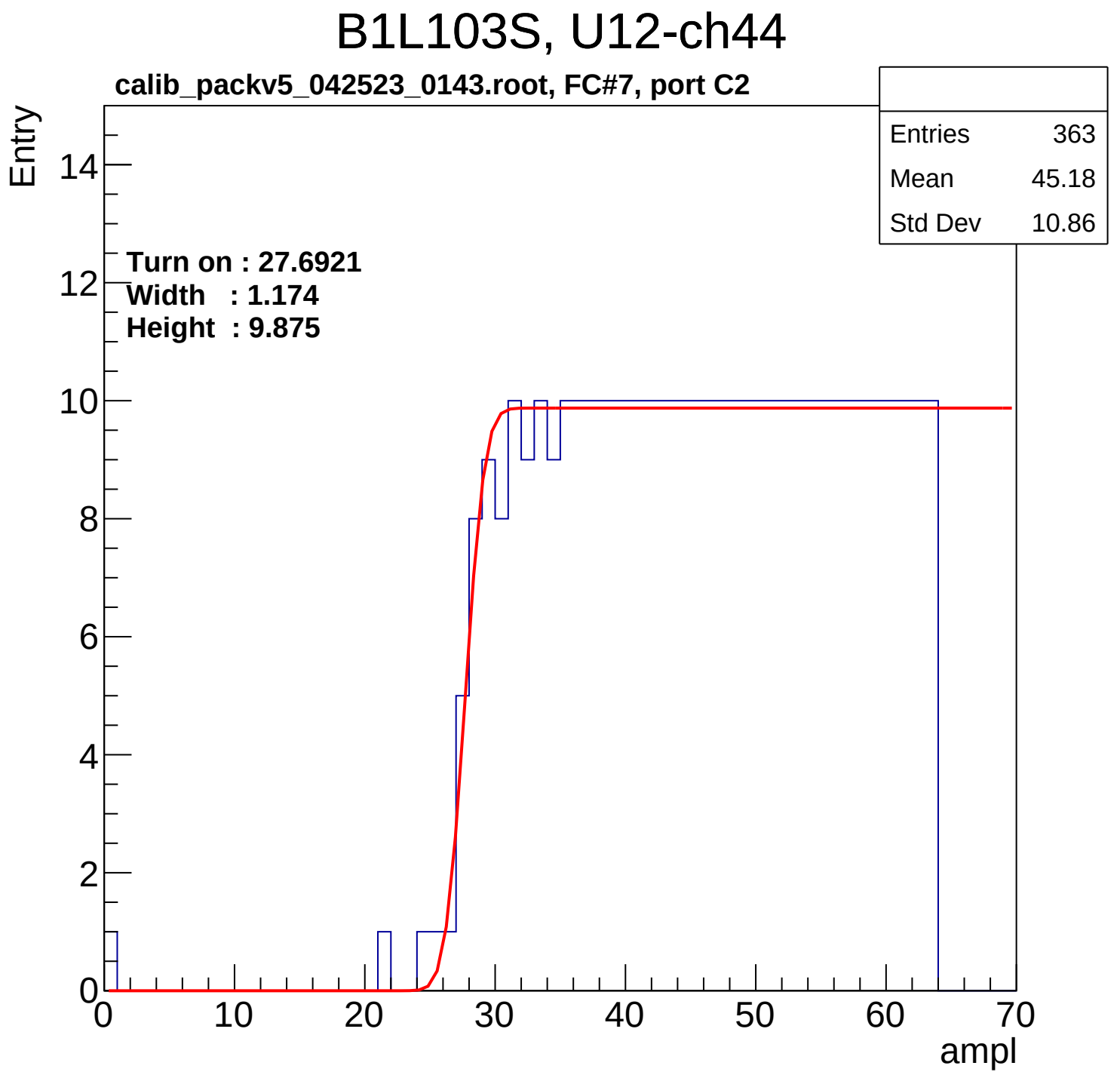

B1L103S, U12-ch39
calib_packv5_042523_0143.root, FC#7, port C2
Entries 377
Mean 44.42
Std Dev 11.43
Turn on : 26.8429
Width : 3.084
Height : 10.037
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

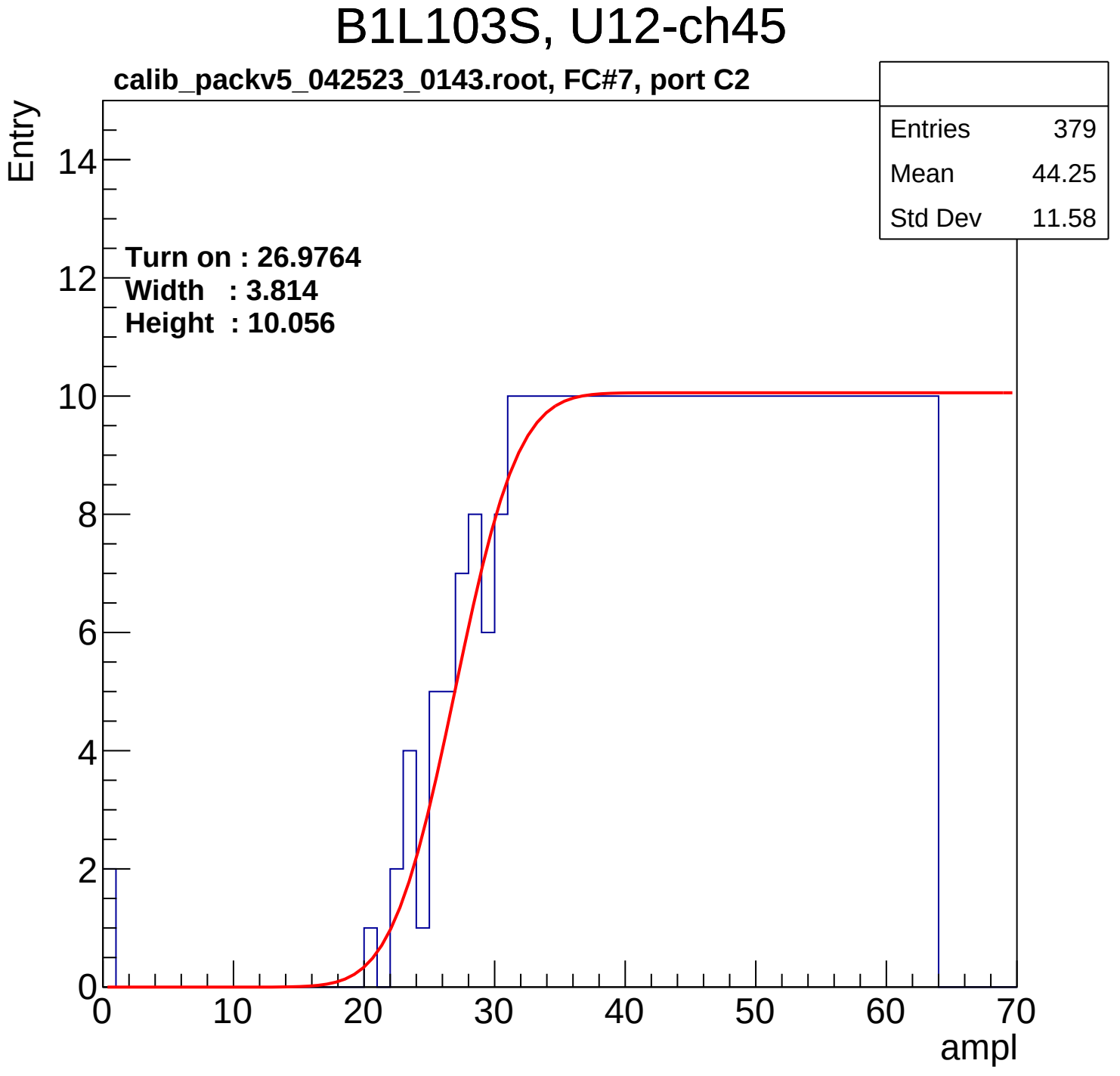

B1L103S, U12-ch40
calib_packv5_042523_0143.root, FC#7, port C2
Entries 383
Mean 44.07
Std Dev 11.66
Turn on : 26.3349
Width : 3.045
Height : 9.974
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

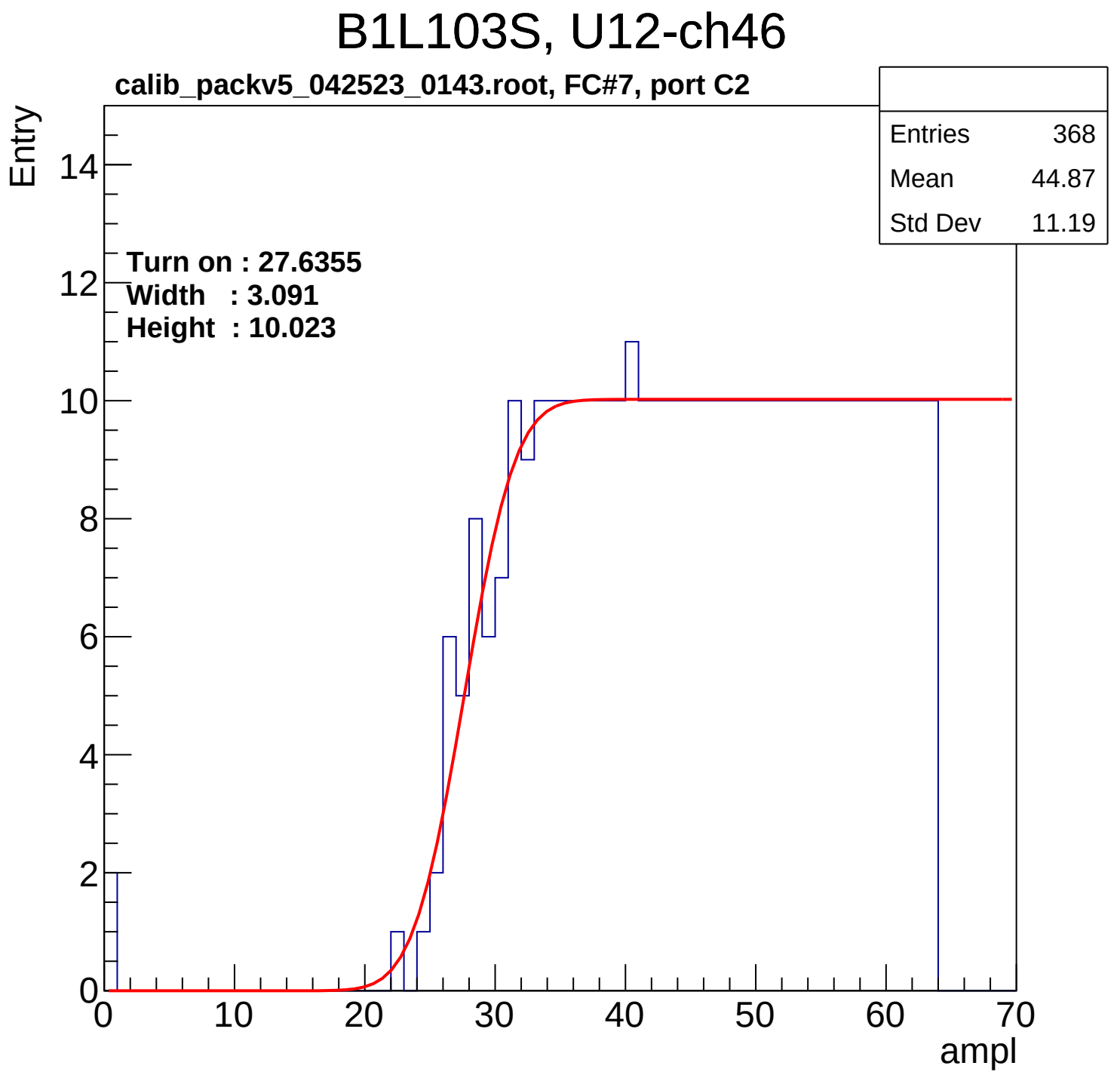

B1L103S, U12-ch41
calib_packv5_042523_0143.root, FC#7, port C2
Entries 361
Mean 45.37
Std Dev 10.76
Turn on : 27.9283
Width : 3.546
Height : 10.044
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

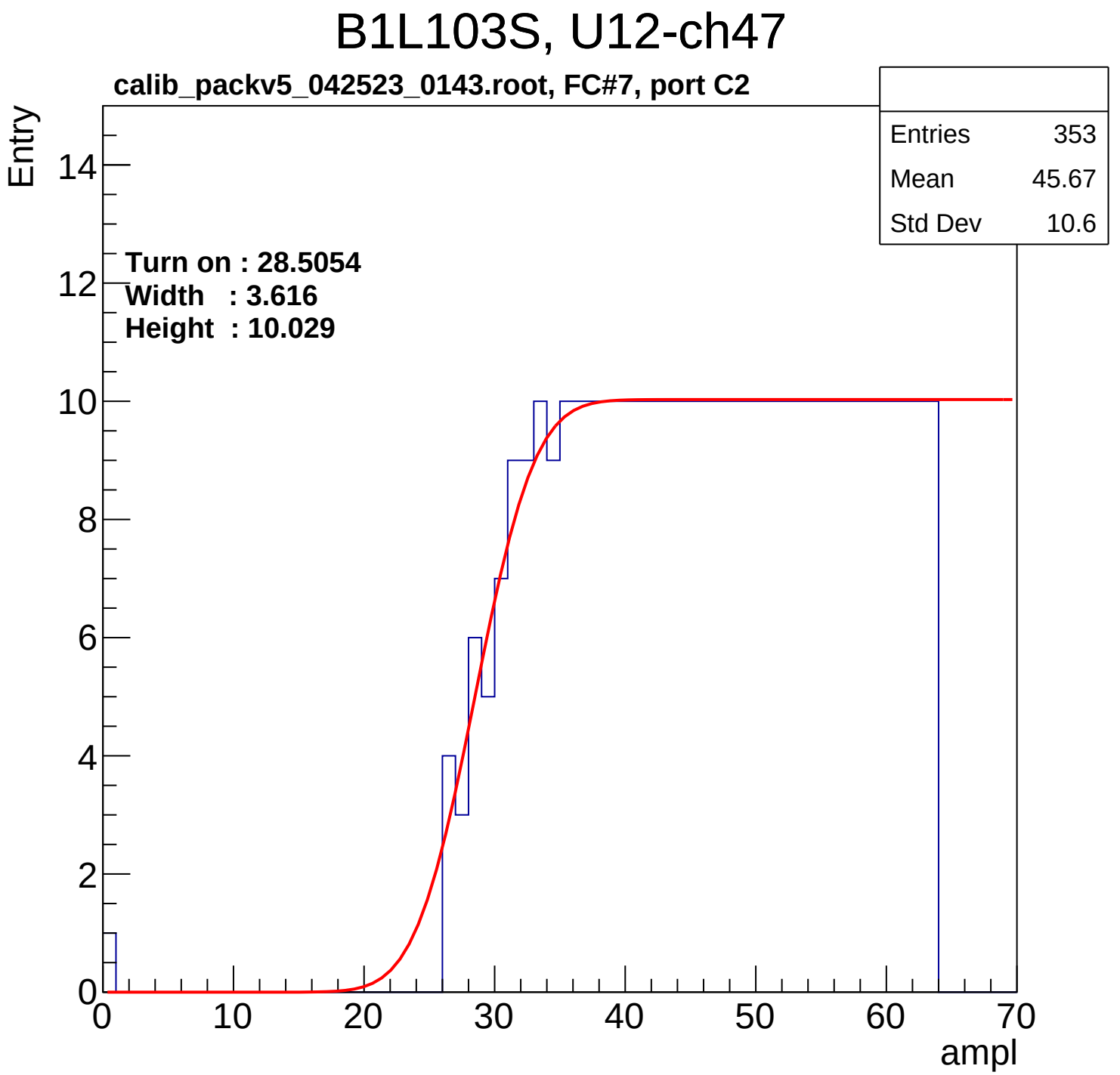

B1L103S, U12-ch42
calib_packv5_042523_0143.root, FC#7, port C2
Entries 393
Mean 43.63
Std Dev 11.85
Turn on : 25.1283
Width : 2.738
Height : 10.010
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

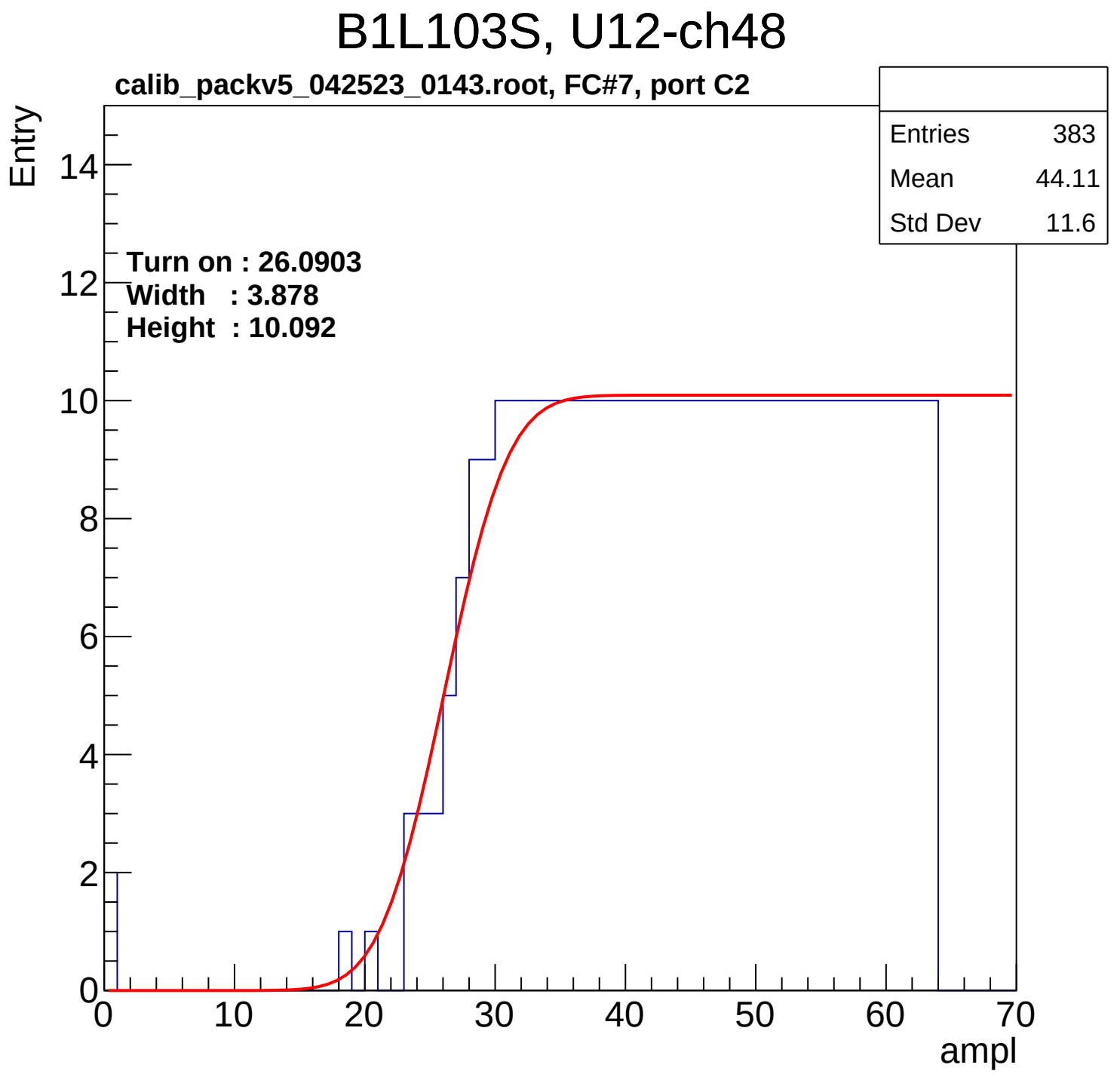

B1L103S, U12-ch43
calib_packv5_042523_0143.root, FC#7, port C2
Entries 368
Mean 44.72
Std Dev 11.5
Turn on : 27.3527
Width : 4.261
Height : 10.028
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

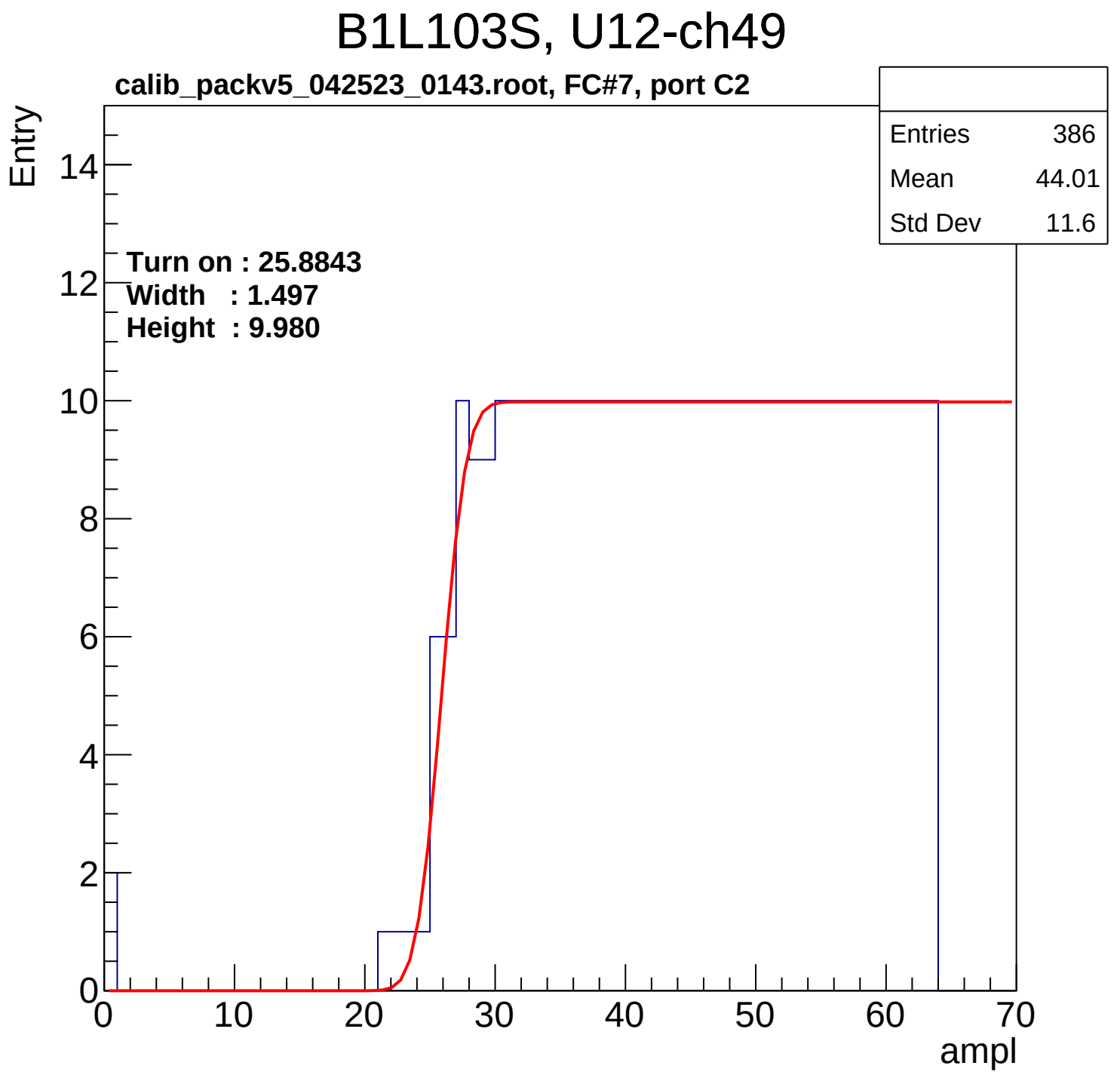

B1L103S, U12-ch44
calib_packv5_042523_0143.root, FC#7, port C2
Entries 363
Mean 45.18
Std Dev 10.86
Turn on : 27.6921
Width : 1.174
Height : 9.875
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

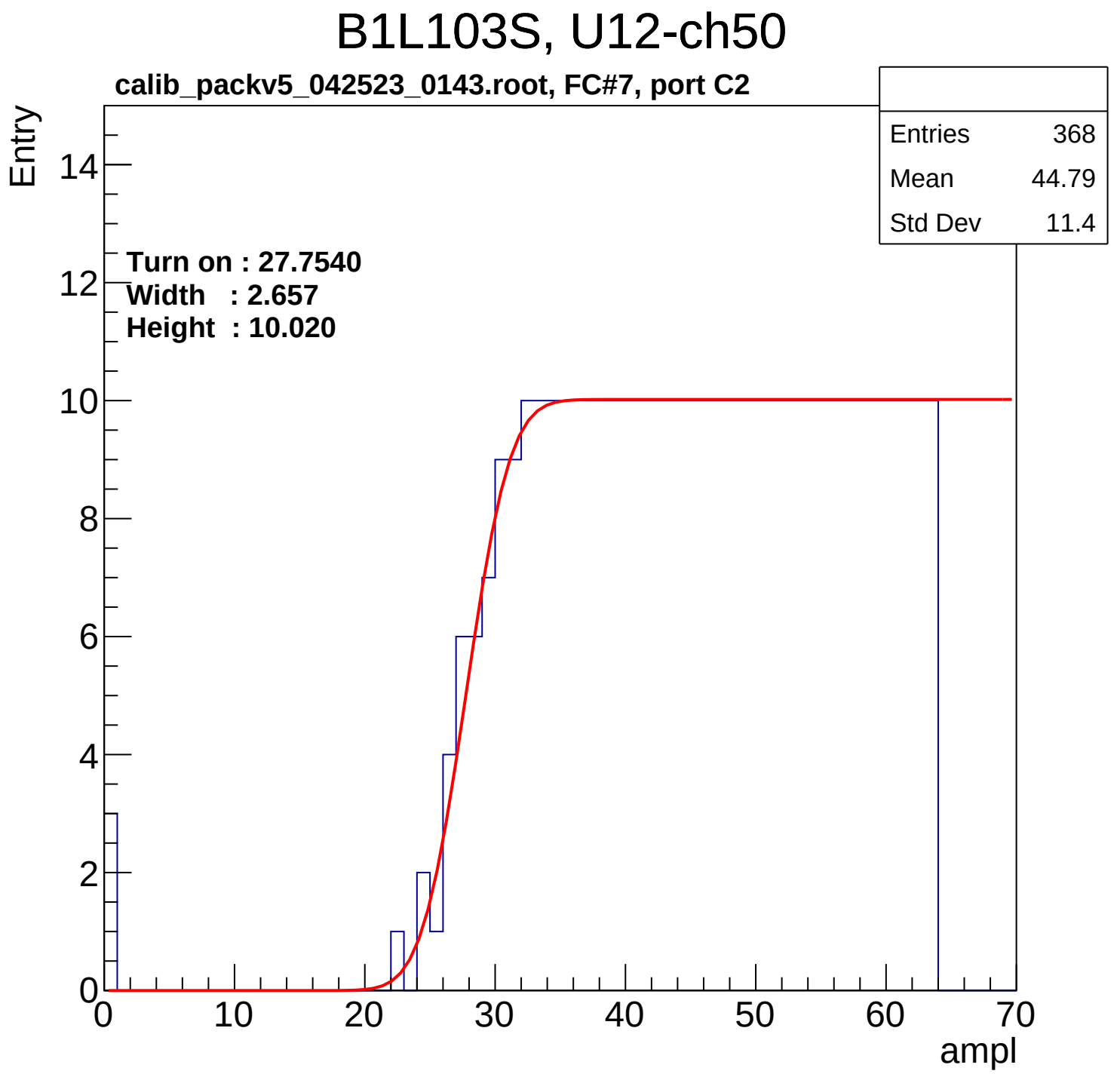

B1L103S, U12-ch45
calib_packv5_042523_0143.root, FC#7, port C2
Entries 379
Mean 44.25
Std Dev 11.58
Turn on : 26.9764
Width : 3.814
Height : 10.056
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

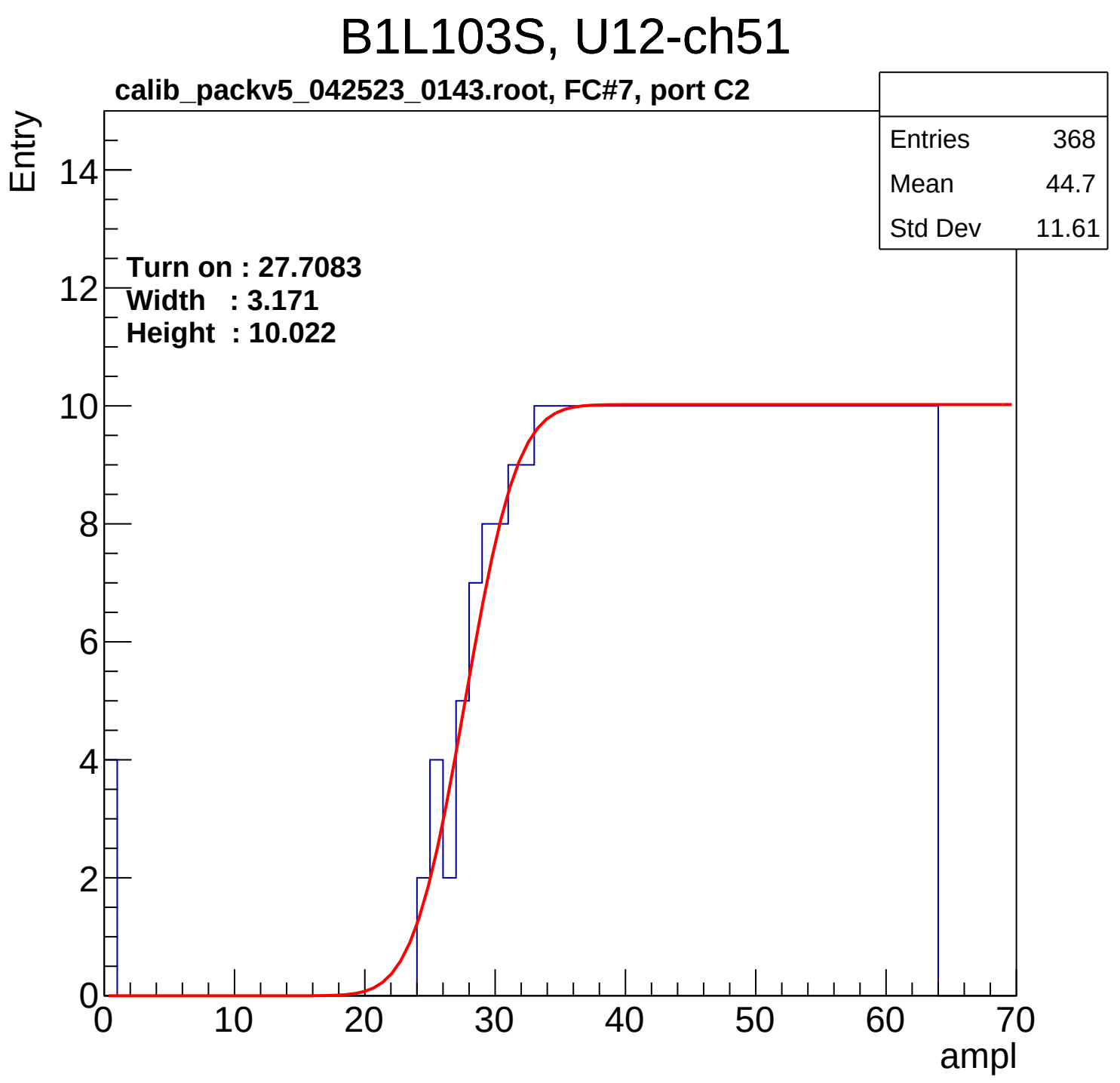

B1L103S, U12-ch46
calib_packv5_042523_0143.root, FC#7, port C2
Entries 368
Mean 44.87
Std Dev 11.19
Turn on : 27.6355
Width : 3.091
Height : 10.023
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

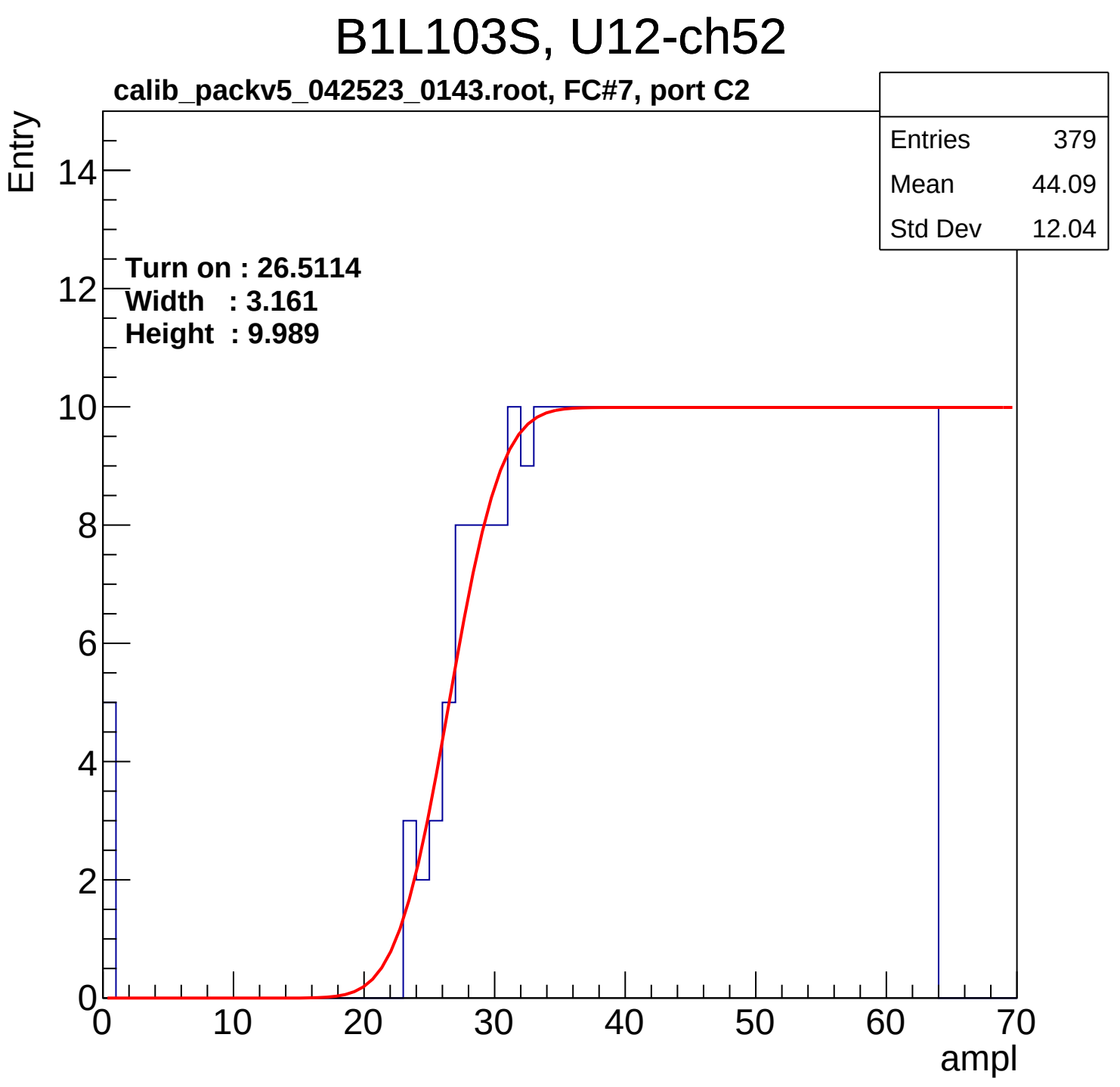

B1L103S, U12-ch47
calib_packv5_042523_0143.root, FC#7, port C2
Entries 353
Mean 45.67
Std Dev 10.6
Turn on : 28.5054
Width : 3.616
Height : 10.029
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

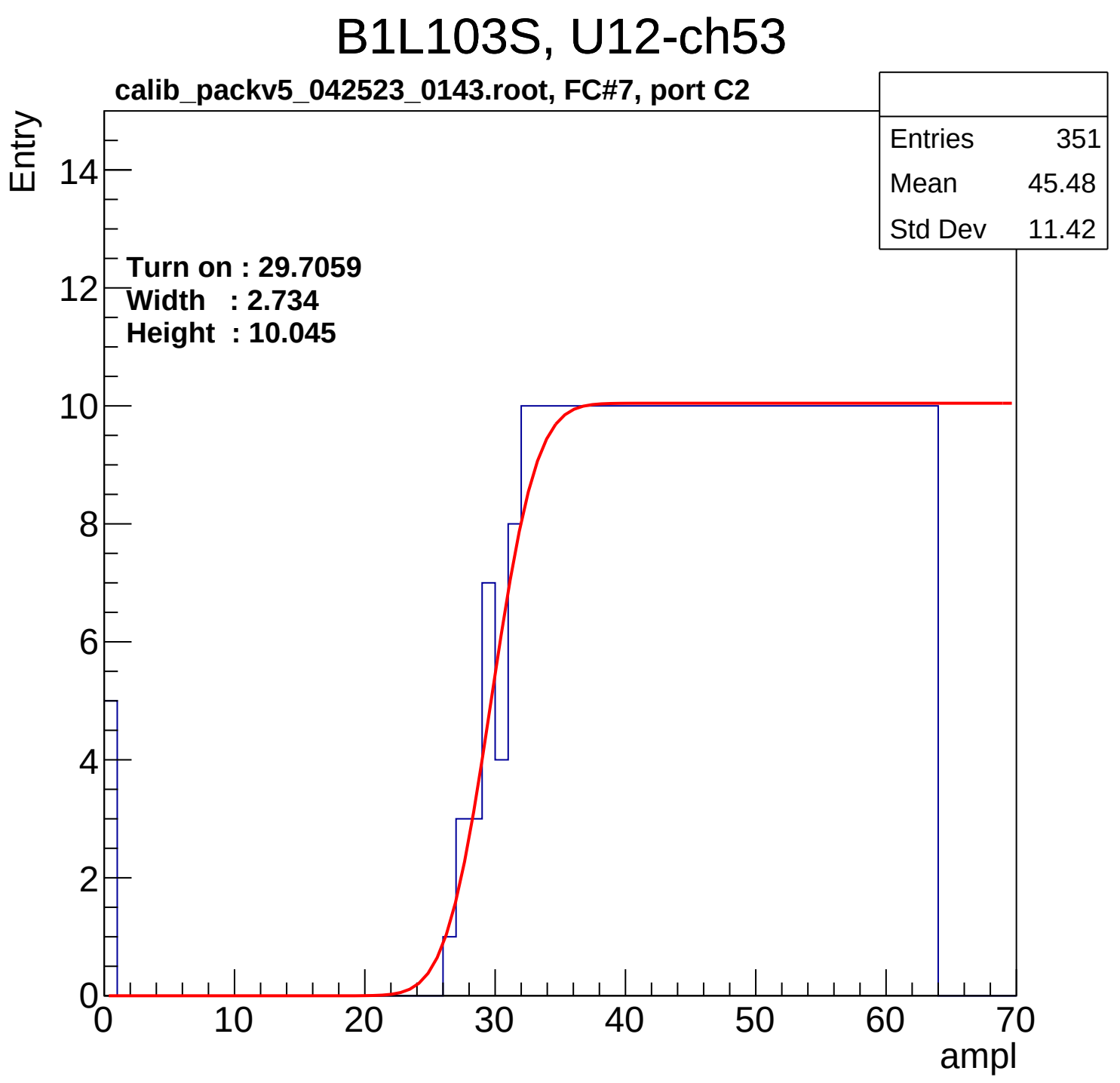

B1L103S, U12-ch48
calib_packv5_042523_0143.root, FC#7, port C2
Entries 383
Mean 44.11
Std Dev 11.6
Turn on : 26.0903
Width : 3.878
Height : 10.092
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

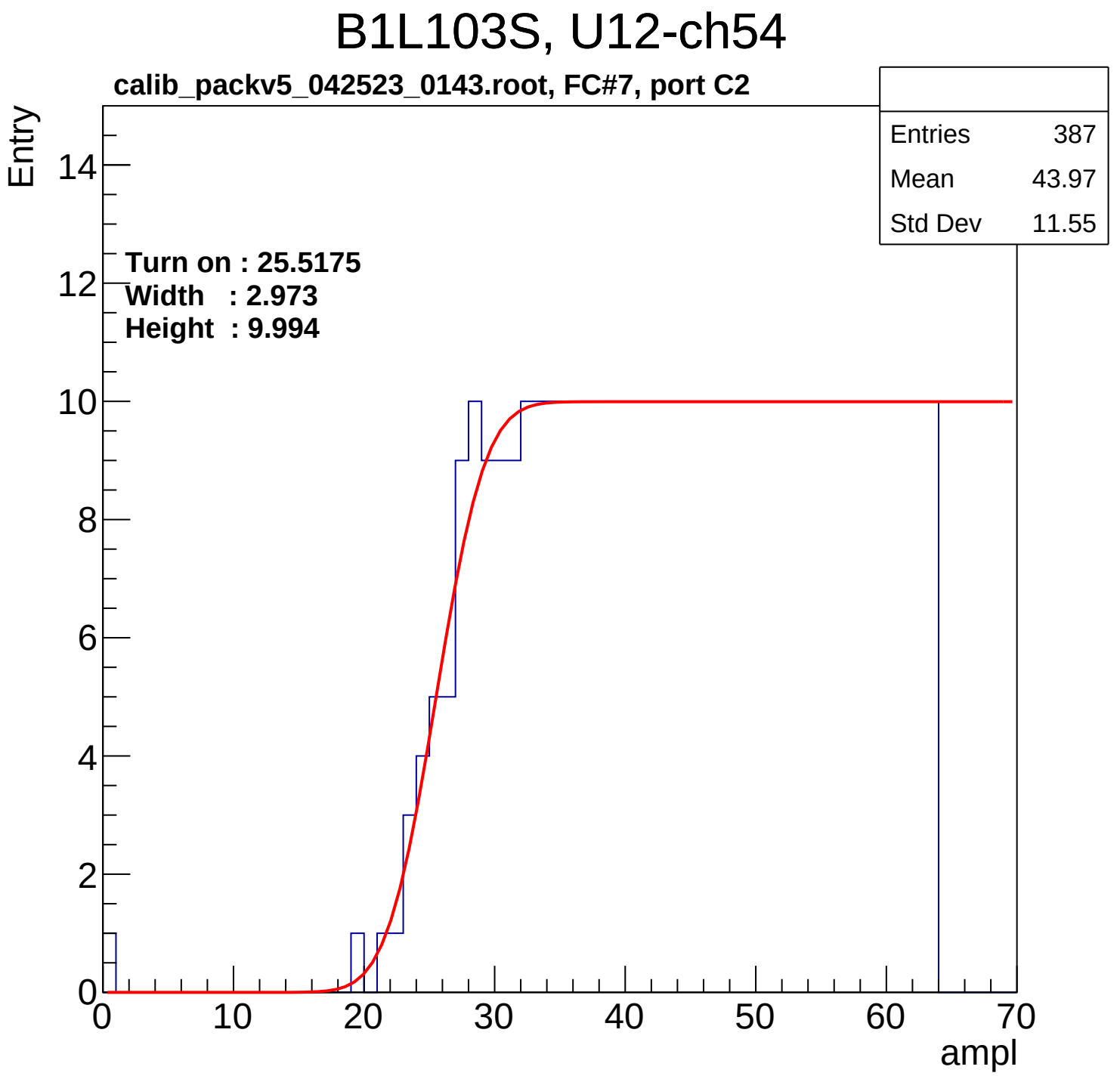

B1L103S, U12-ch49
calib_packv5_042523_0143.root, FC#7, port C2
Entries 386
Mean 44.01
Std Dev 11.6
Turn on : 25.8843
Width : 1.497
Height : 9.980
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

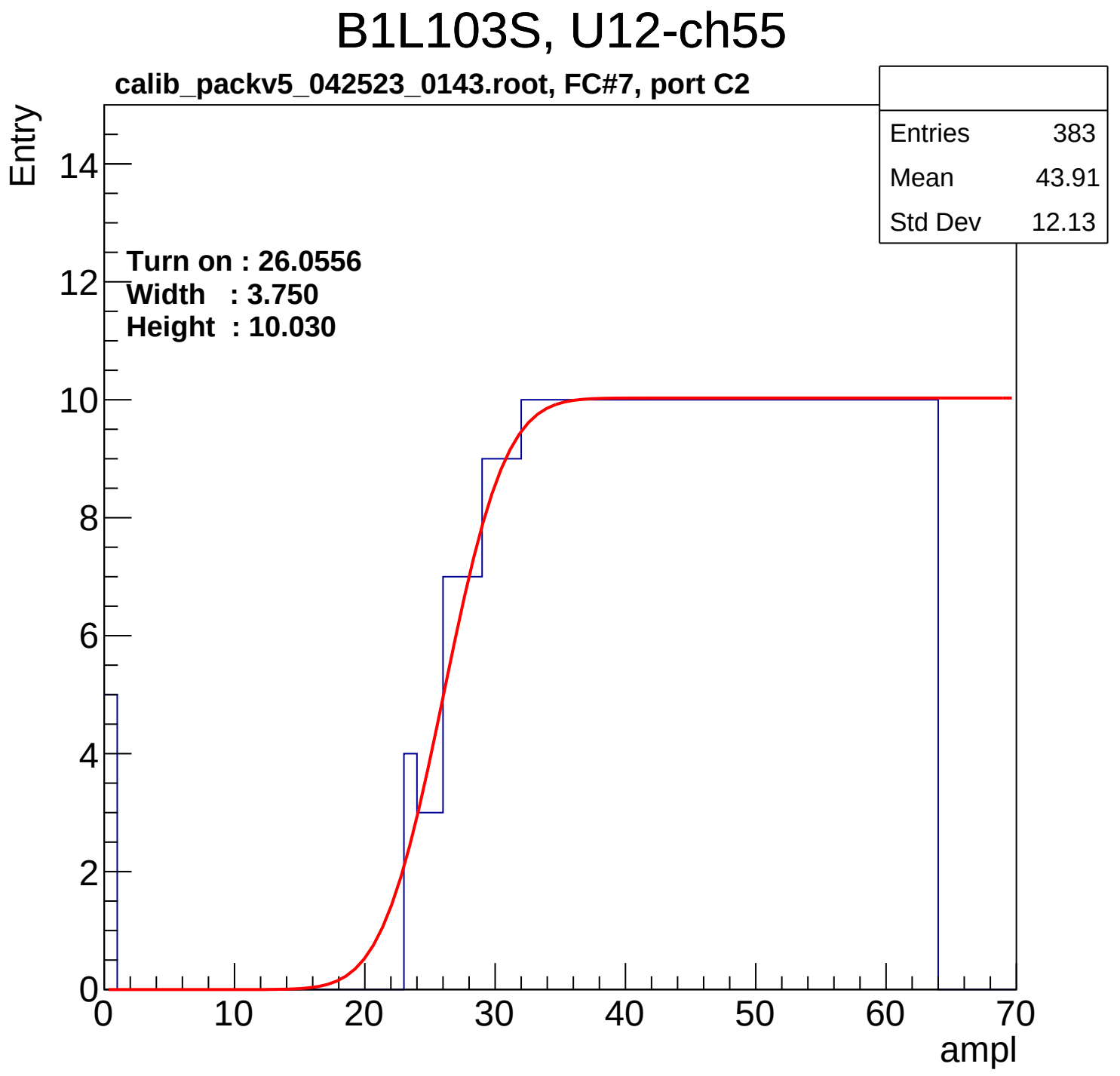

B1L103S, U12-ch50
calib_packv5_042523_0143.root, FC#7, port C2
Entries 368
Mean 44.79
Std Dev 11.4
Turn on : 27.7540
Width : 2.657
Height : 10.020
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

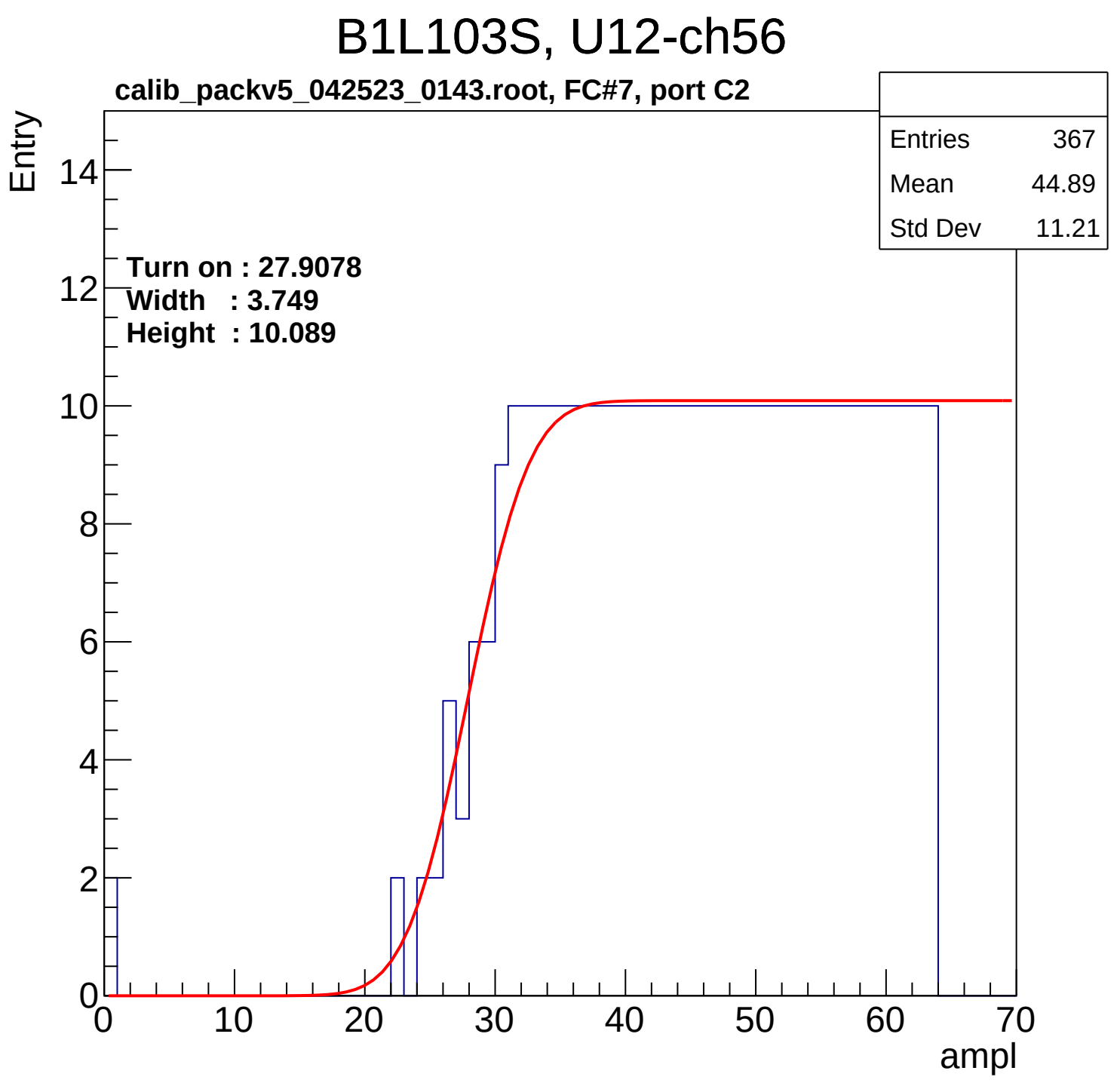

B1L103S, U12-ch51
calib_packv5_042523_0143.root, FC#7, port C2
Entries 368
Mean 44.7
Std Dev 11.61
Turn on : 27.7083
Width : 3.171
Height : 10.022
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

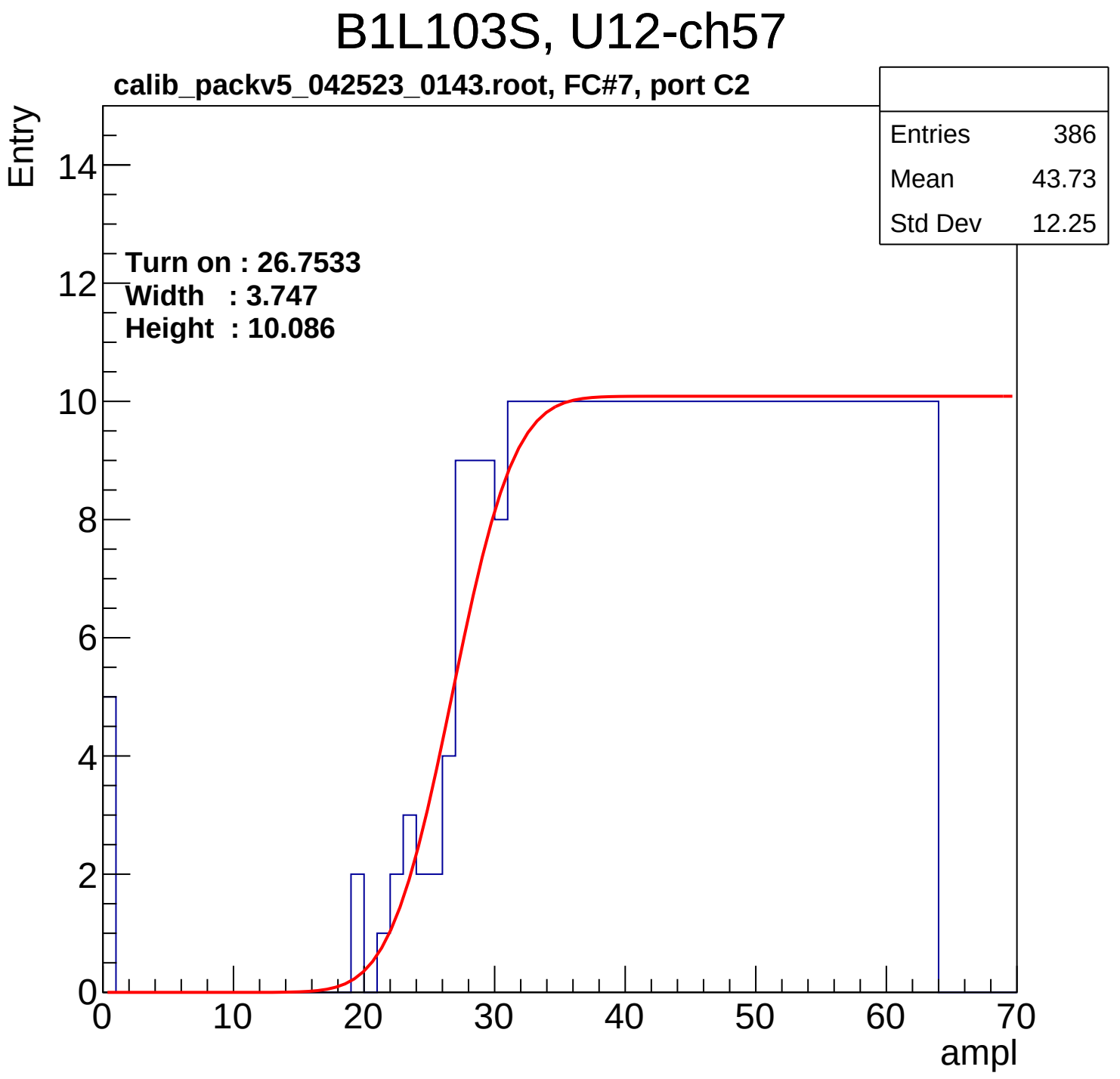

B1L103S, U12-ch52
calib_packv5_042523_0143.root, FC#7, port C2
Entries 379
Mean 44.09
Std Dev 12.04
Turn on : 26.5114
Width : 3.161
Height : 9.989
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

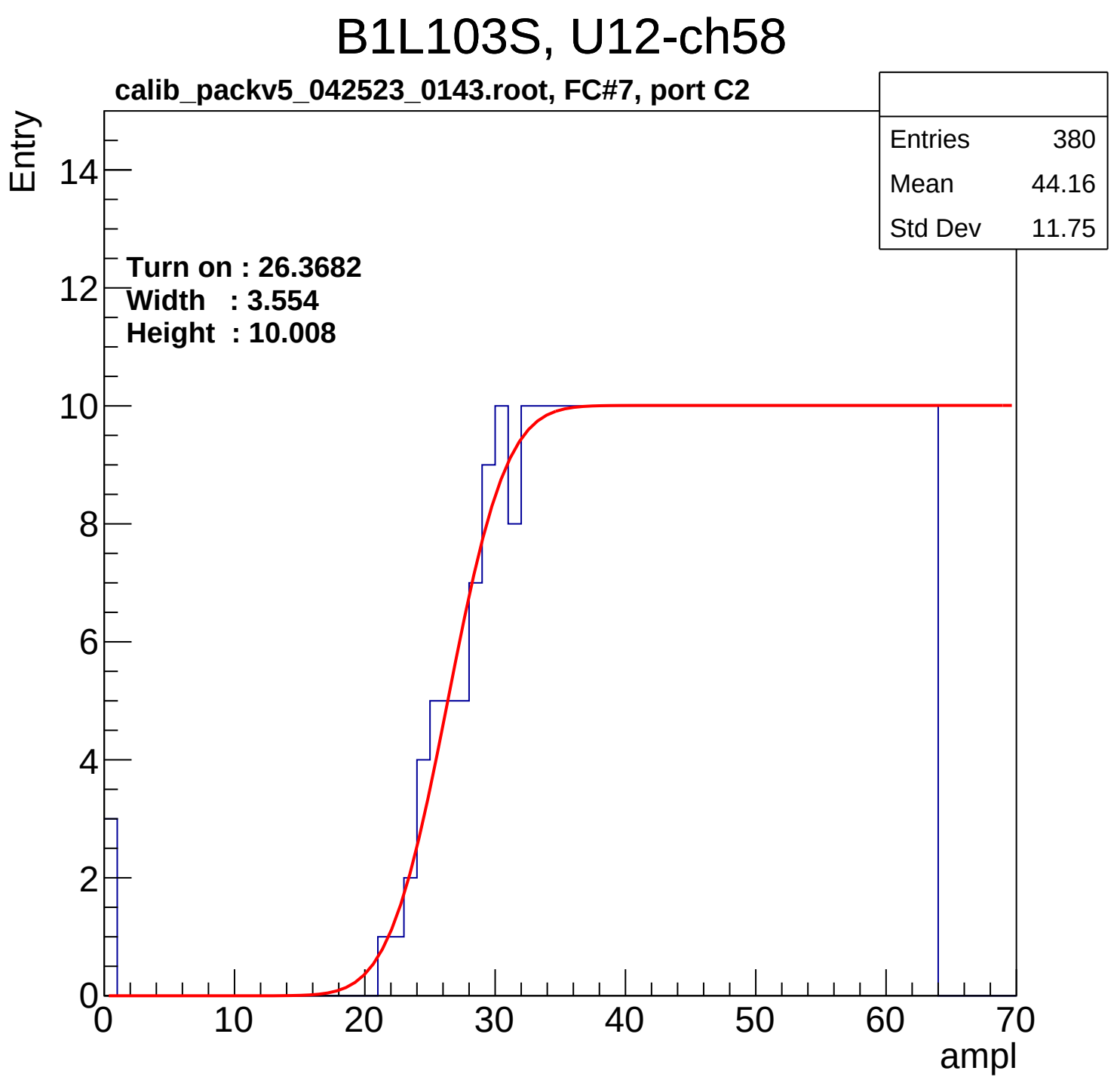

B1L103S, U12-ch53
calib_packv5_042523_0143.root, FC#7, port C2
Entries 351
Mean 45.48
Std Dev 11.42
Turn on : 29.7059
Width : 2.734
Height : 10.045
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

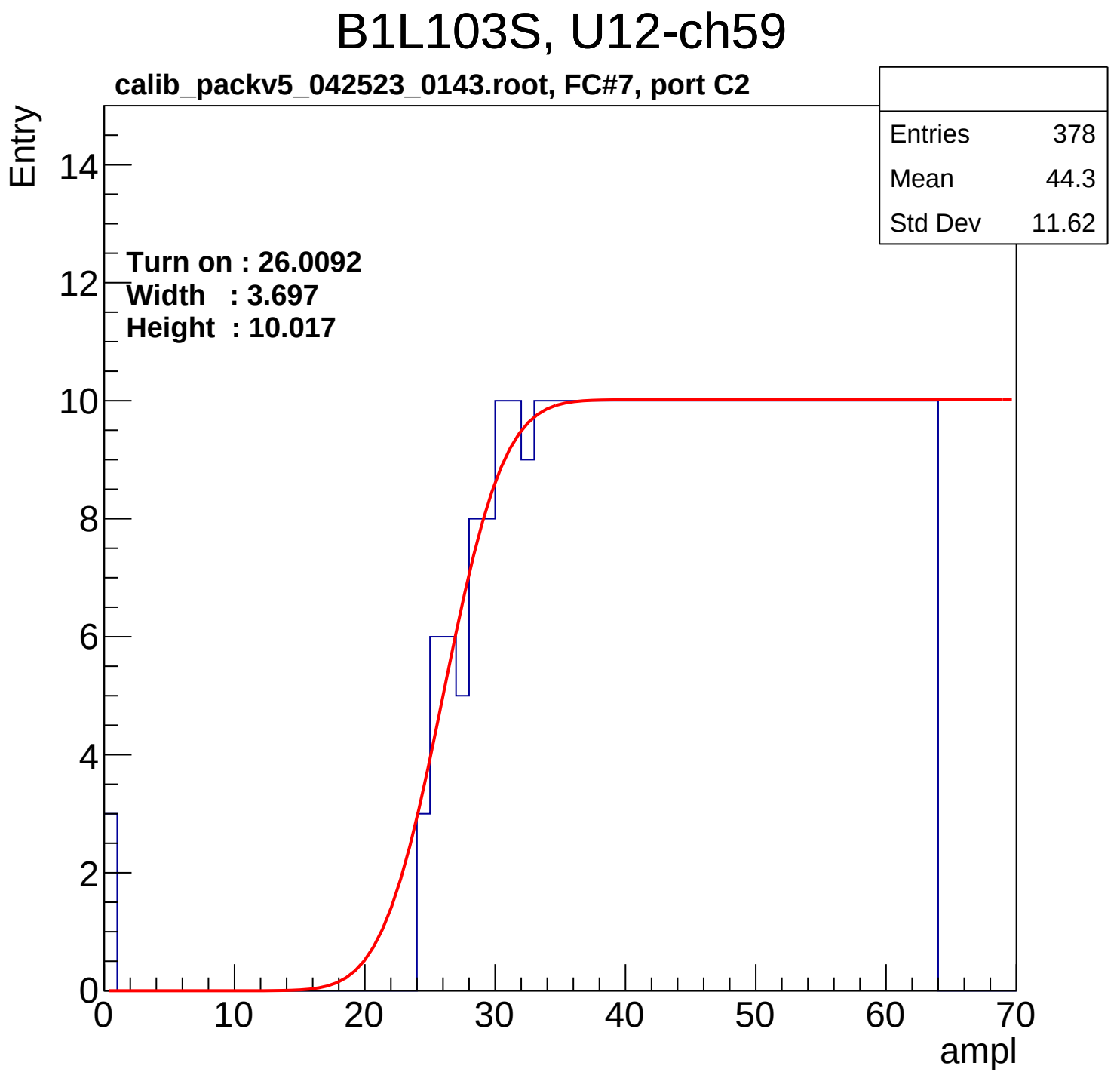

B1L103S, U12-ch54
calib_packv5_042523_0143.root, FC#7, port C2
Entries 387
Mean 43.97
Std Dev 11.55
Turn on : 25.5175
Width : 2.973
Height : 9.994
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

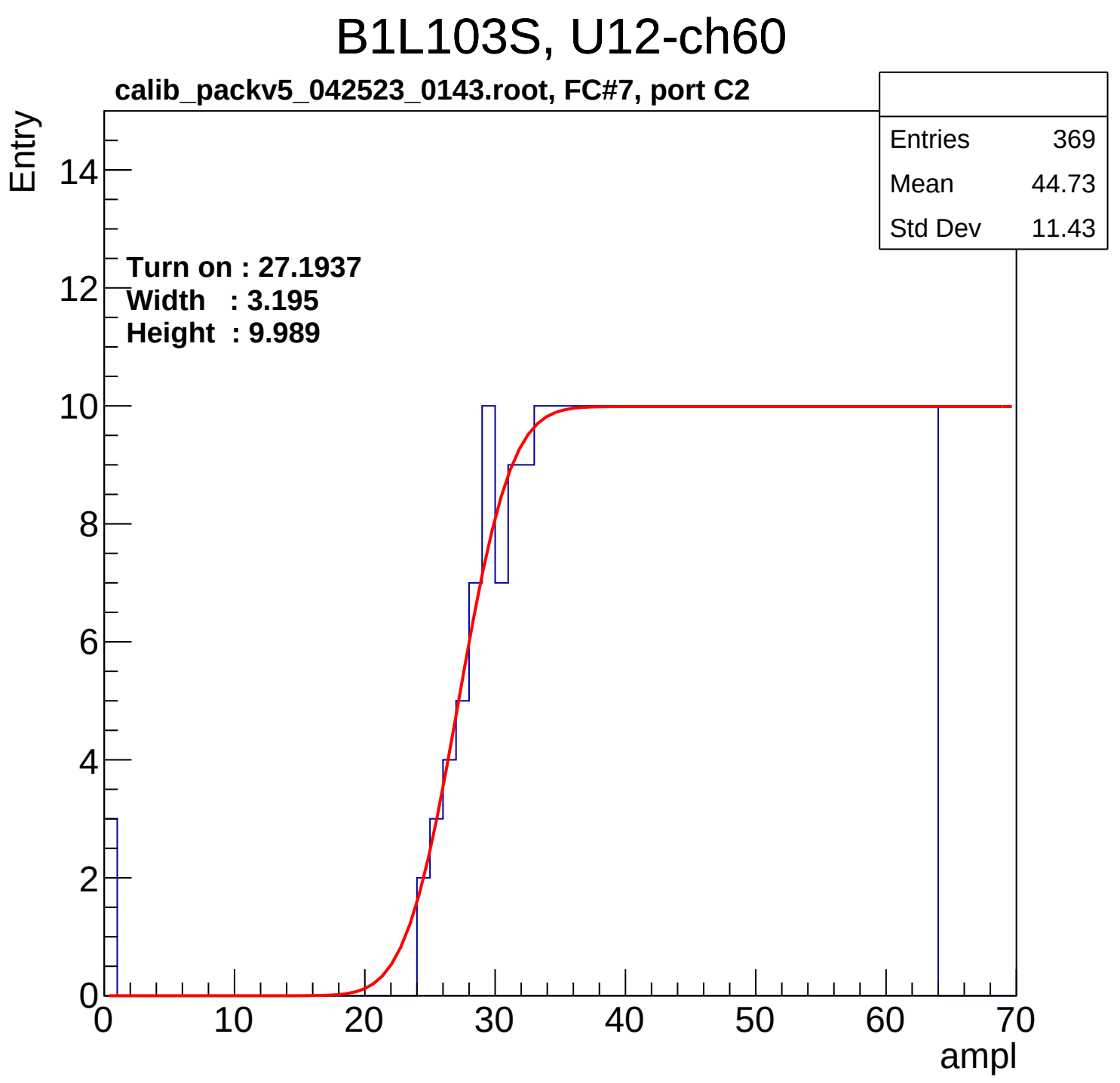

B1L103S, U12-ch55
calib_packv5_042523_0143.root, FC#7, port C2
Entries 383
Mean 43.91
Std Dev 12.13
Turn on : 26.0556
Width : 3.750
Height : 10.030
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

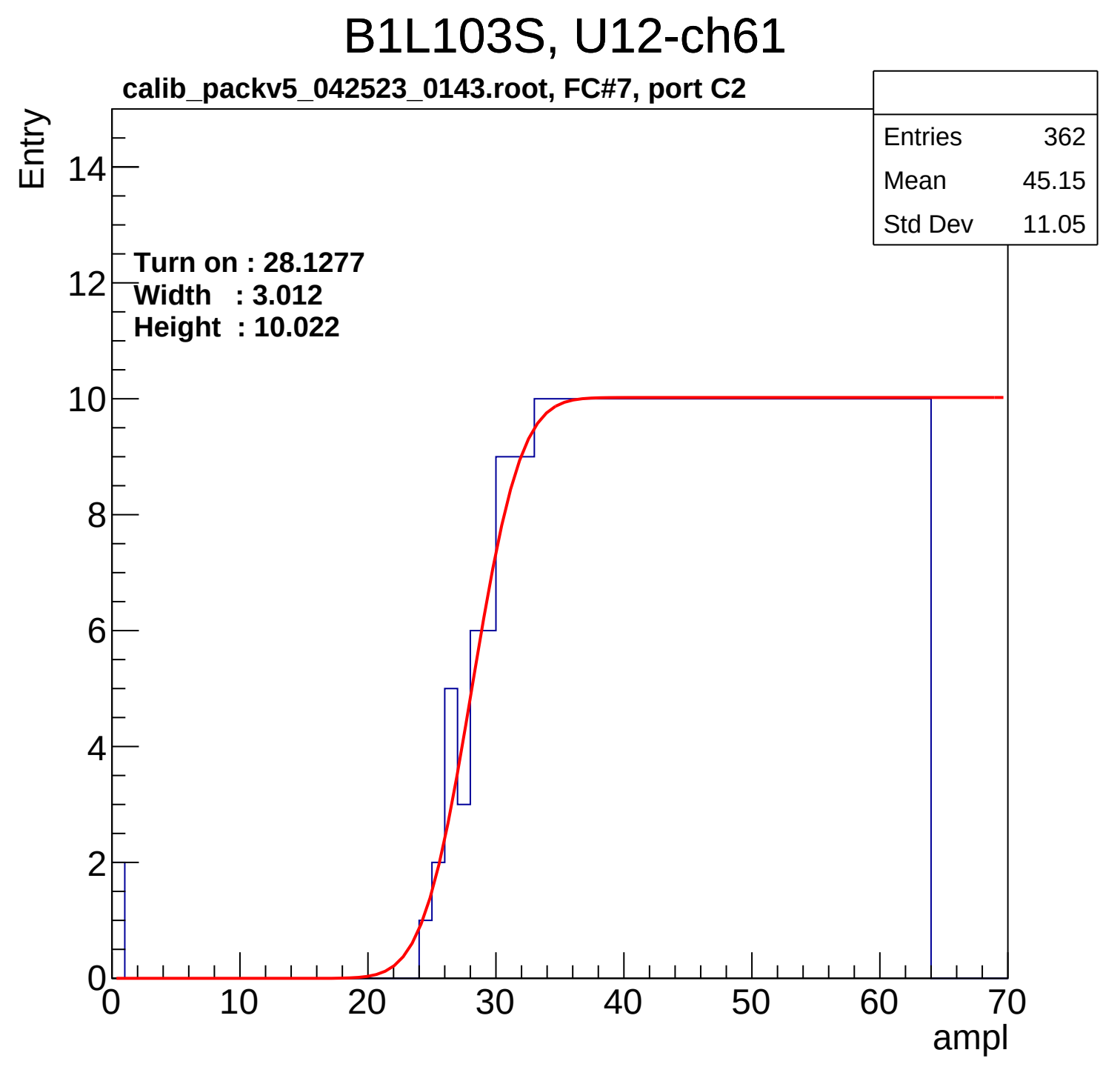

B1L103S, U12-ch56
calib_packv5_042523_0143.root, FC#7, port C2
Entries 367
Mean 44.89
Std Dev 11.21
Turn on : 27.9078
Width : 3.749
Height : 10.089
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

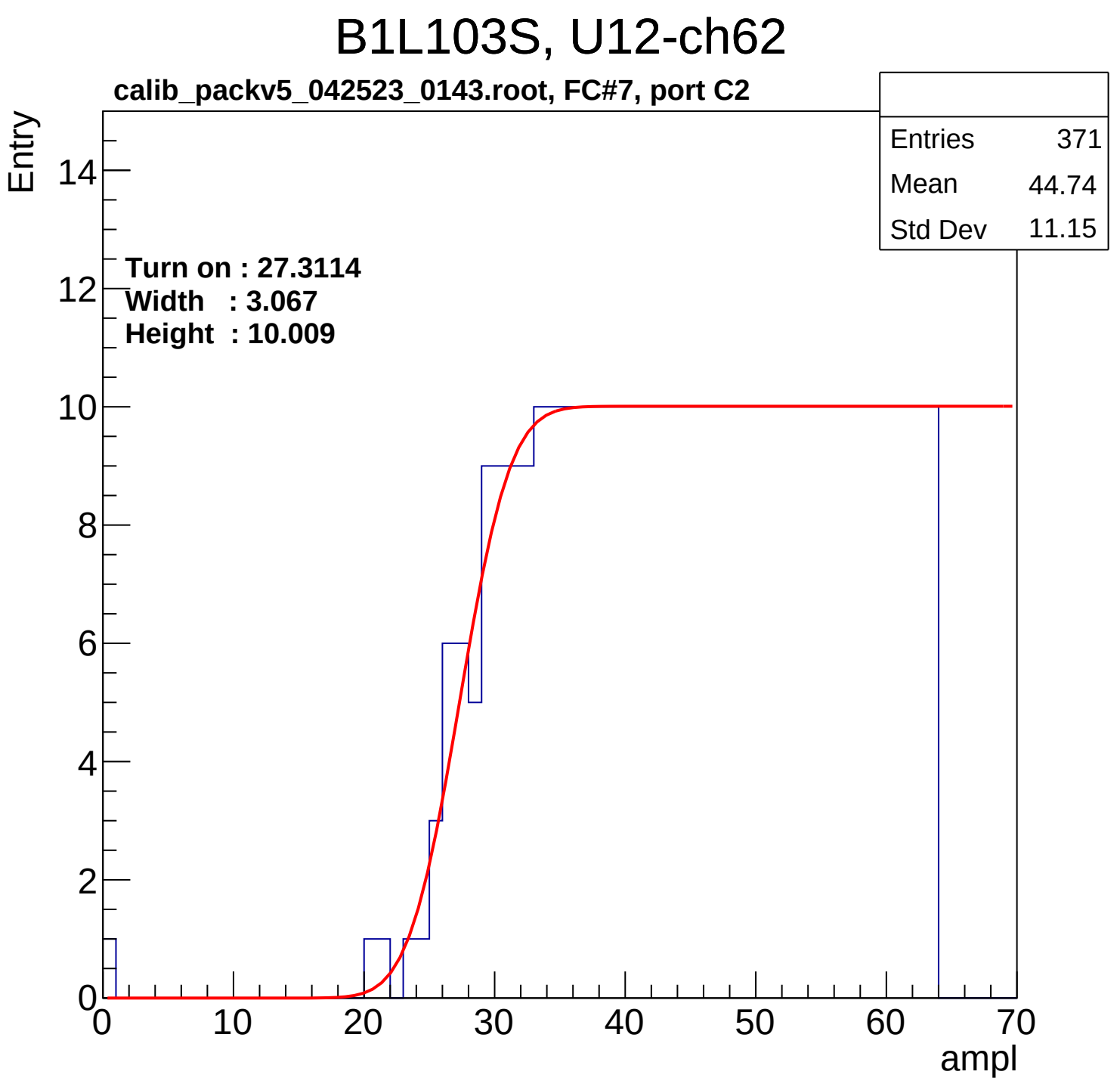

B1L103S, U12-ch57
calib_packv5_042523_0143.root, FC#7, port C2
Entries 386
Mean 43.73
Std Dev 12.25
Turn on : 26.7533
Width : 3.747
Height : 10.086
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

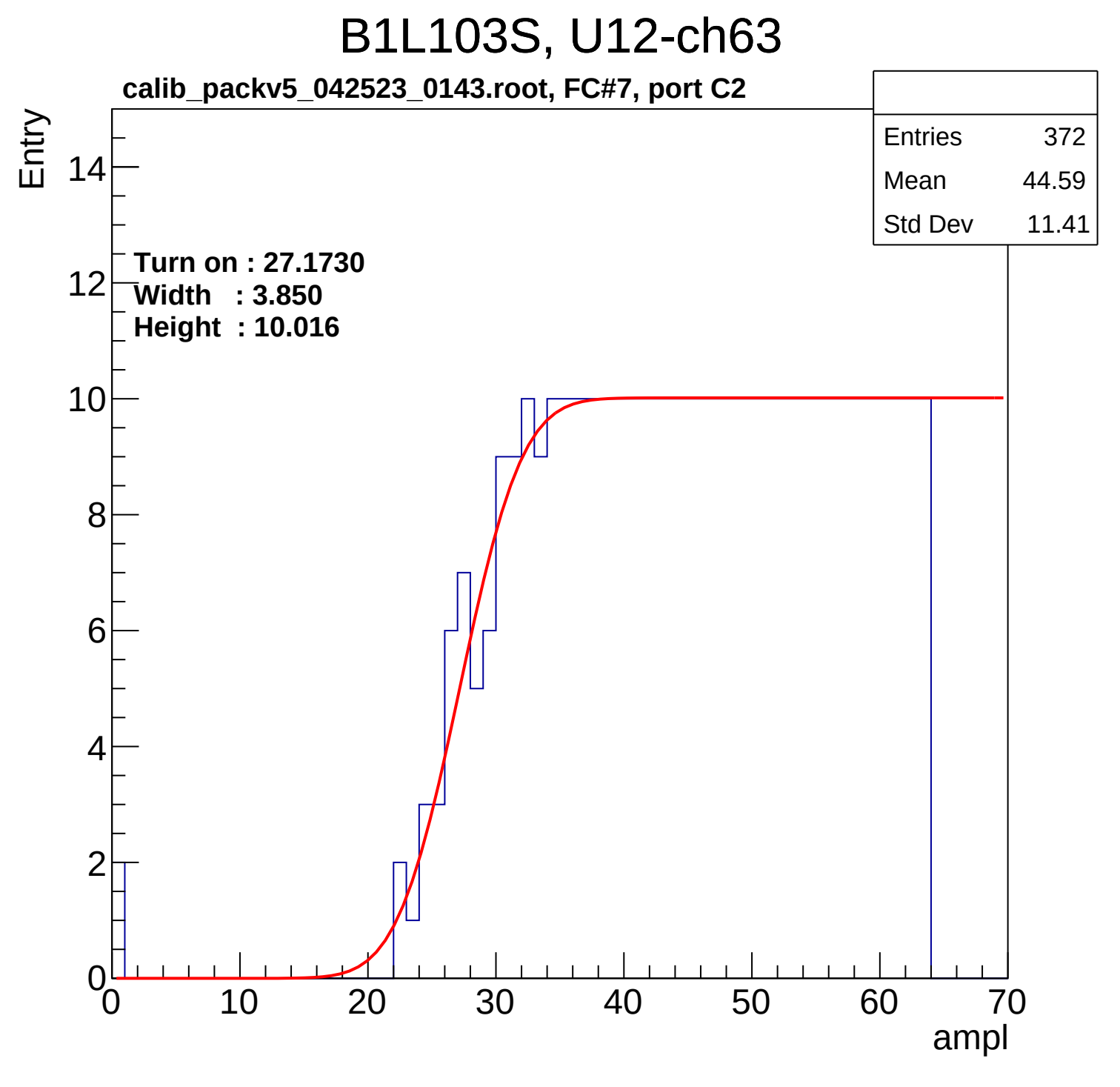

B1L103S, U12-ch58
calib_packv5_042523_0143.root, FC#7, port C2
Entries 380
Mean 44.16
Std Dev 11.75
Turn on : 26.3682
Width : 3.554
Height : 10.008
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

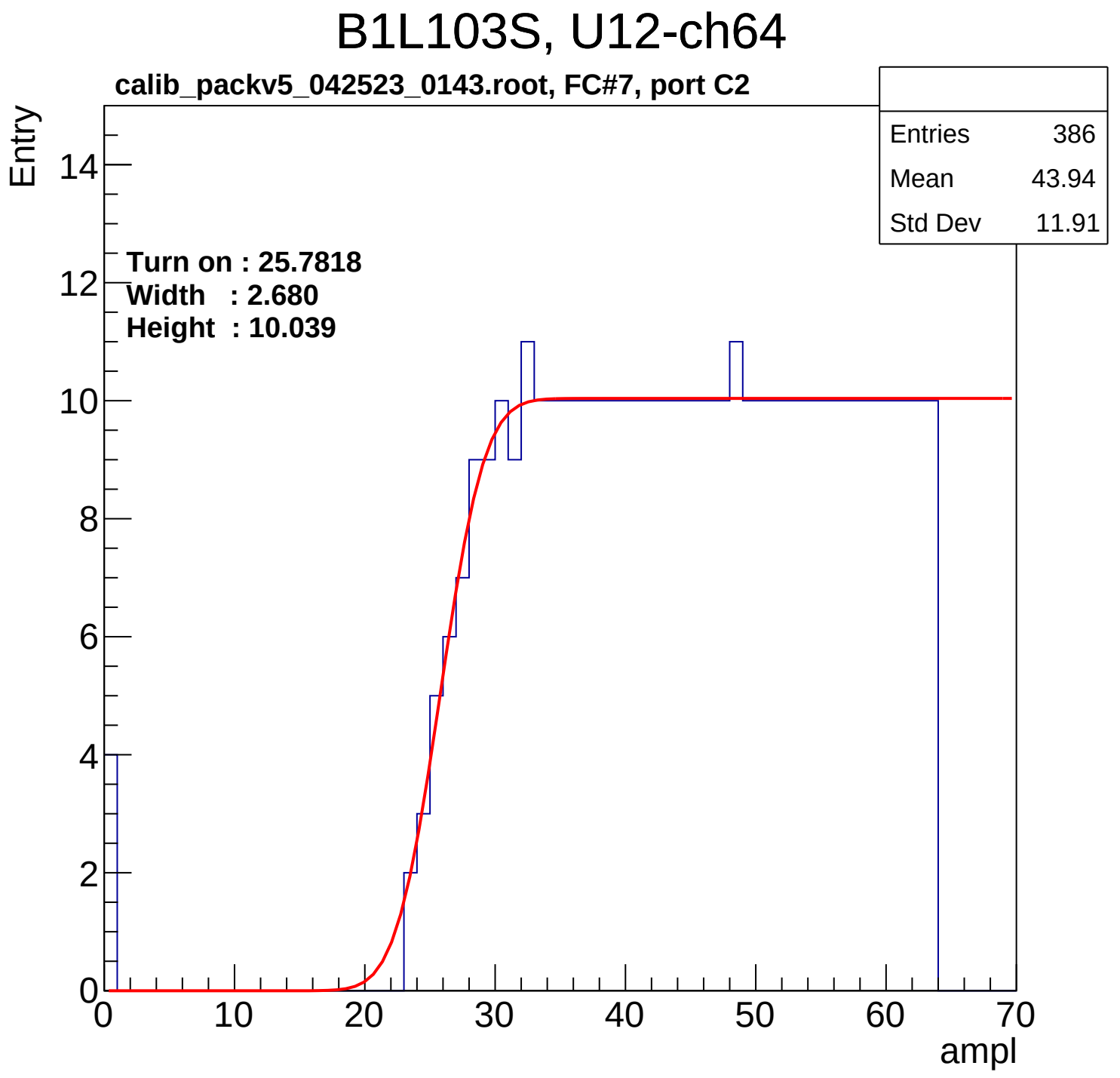

B1L103S, U12-ch59
calib_packv5_042523_0143.root, FC#7, port C2
Entries 378
Mean 44.3
Std Dev 11.62
Turn on : 26.0092
Width : 3.697
Height : 10.017
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

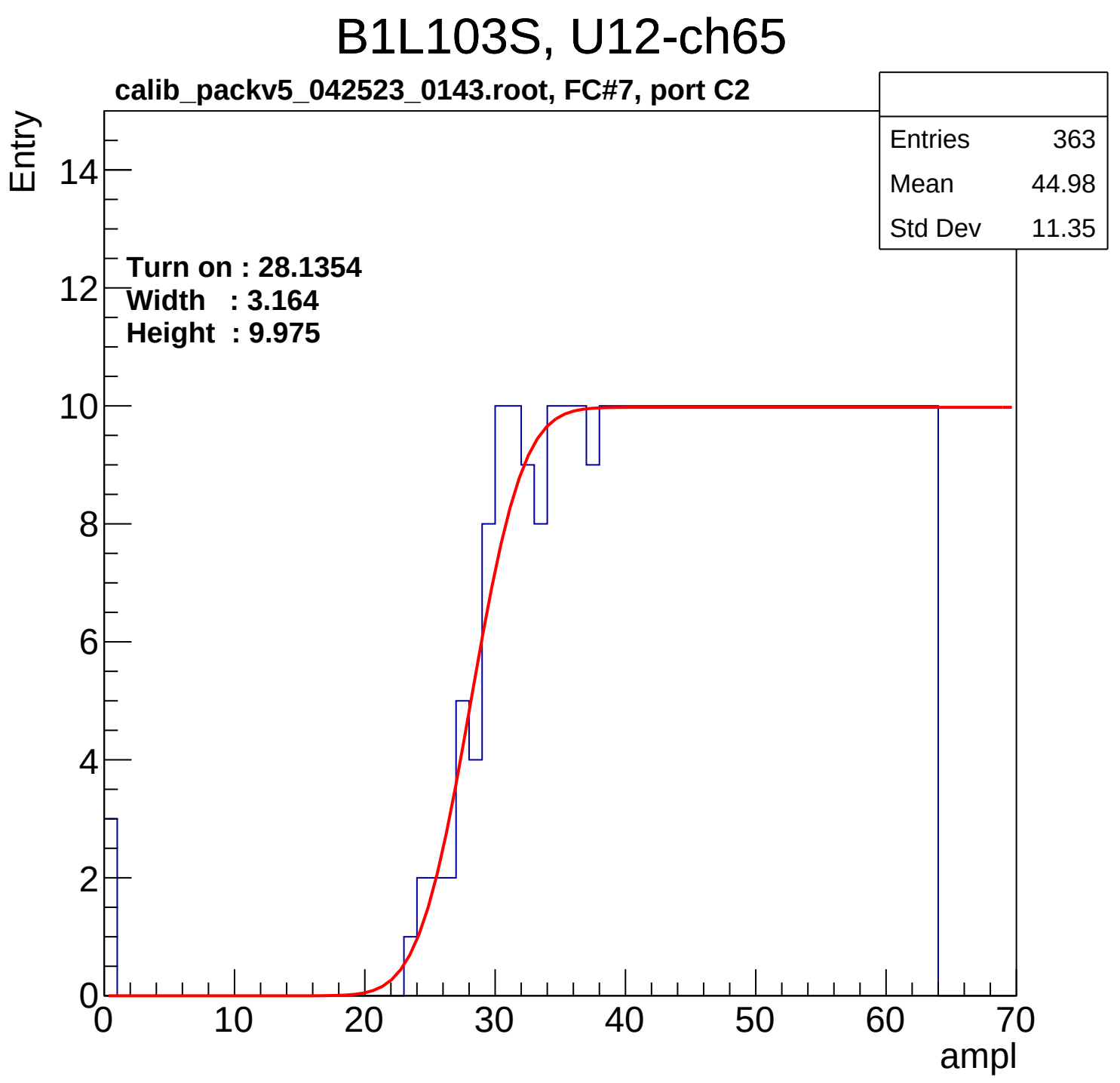

B1L103S, U12-ch60
calib_packv5_042523_0143.root, FC#7, port C2
Entries 369
Mean 44.73
Std Dev 11.43
Turn on : 27.1937
Width : 3.195
Height : 9.989
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

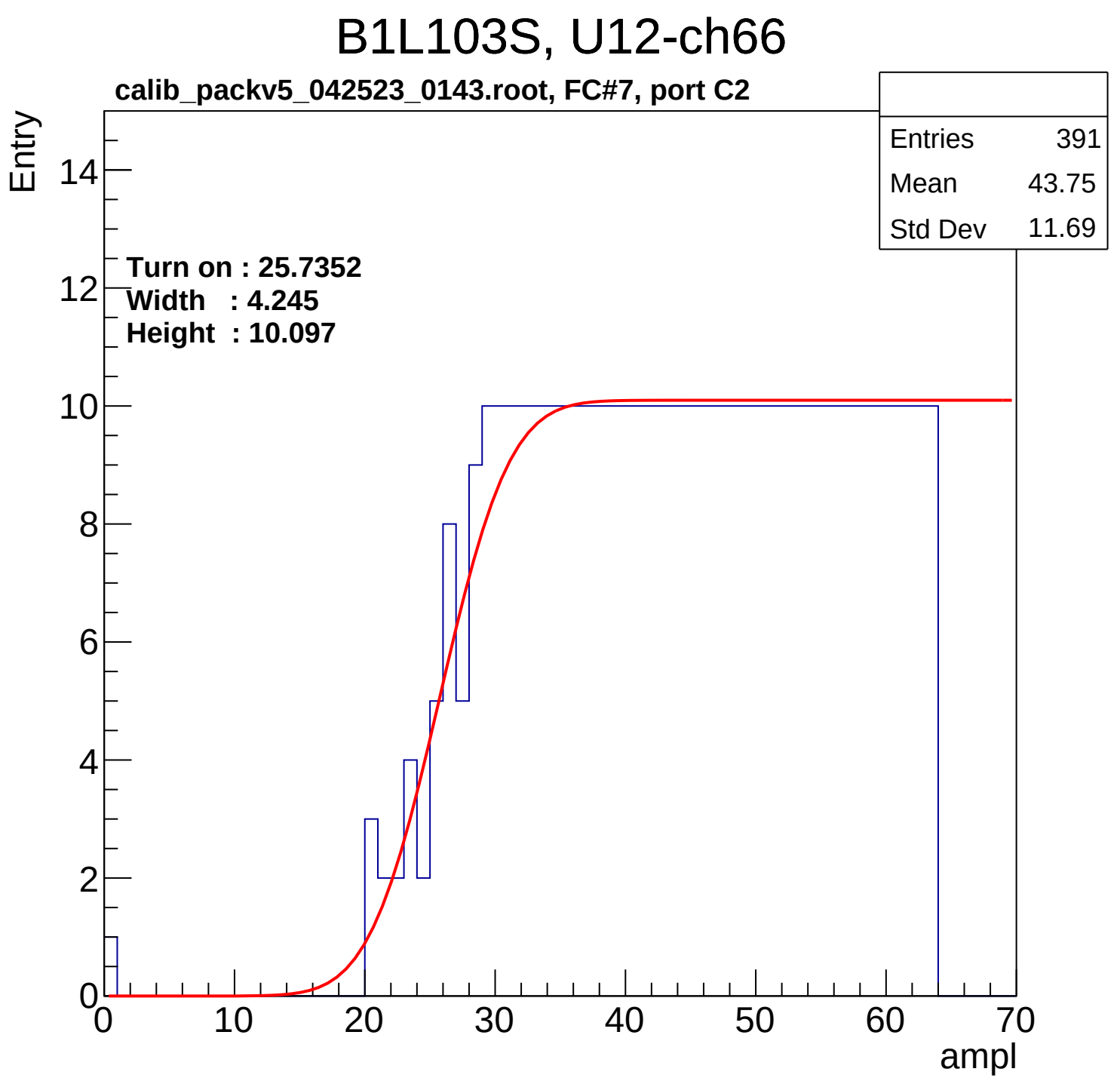

B1L103S, U12-ch61
calib_packv5_042523_0143.root, FC#7, port C2
Entries 362
Mean 45.15
Std Dev 11.05
Turn on : 28.1277
Width : 3.012
Height : 10.022
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

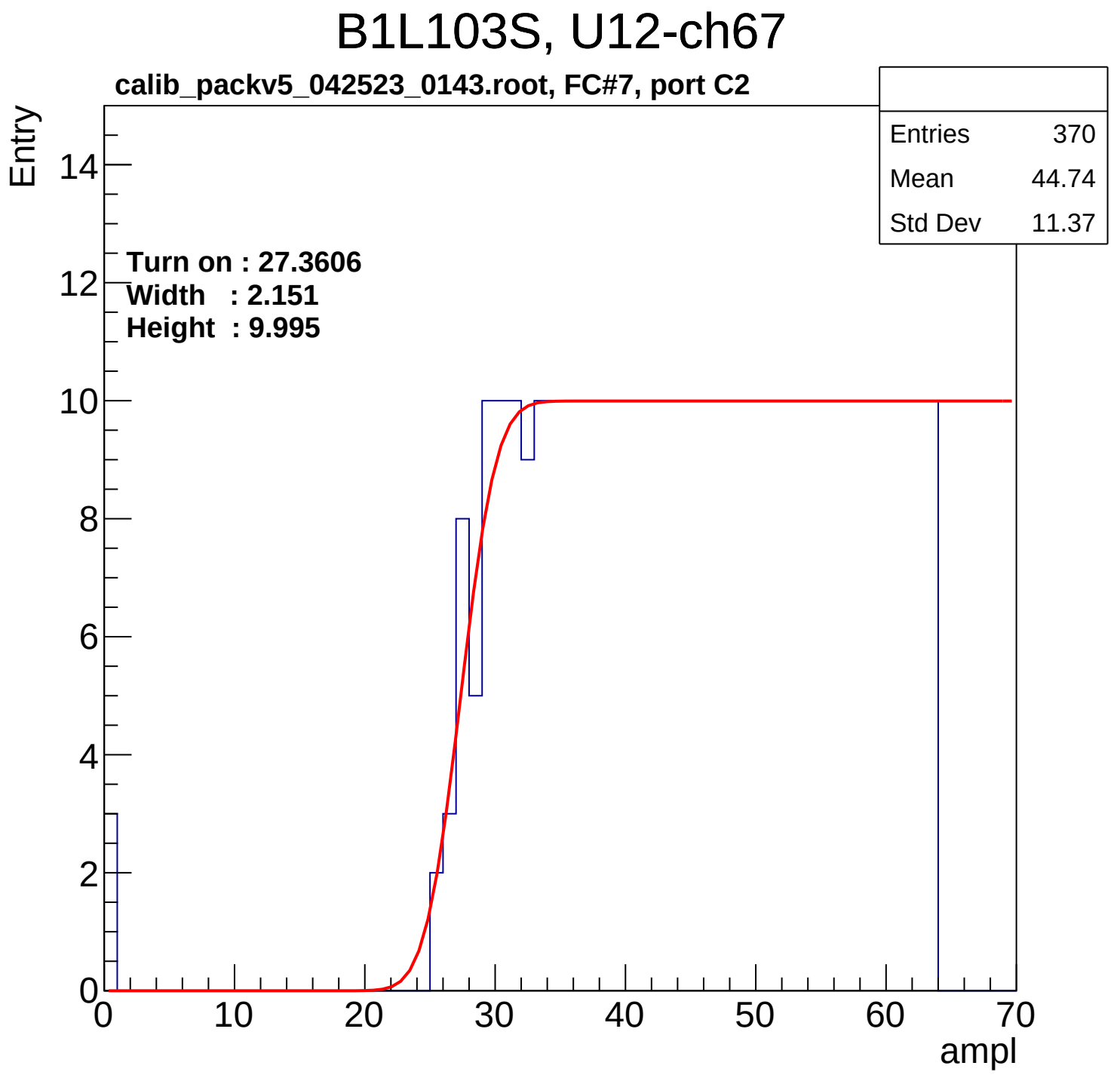

B1L103S, U12-ch62
calib_packv5_042523_0143.root, FC#7, port C2
Entries 371
Mean 44.74
Std Dev 11.15
Turn on : 27.3114
Width : 3.067
Height : 10.009
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

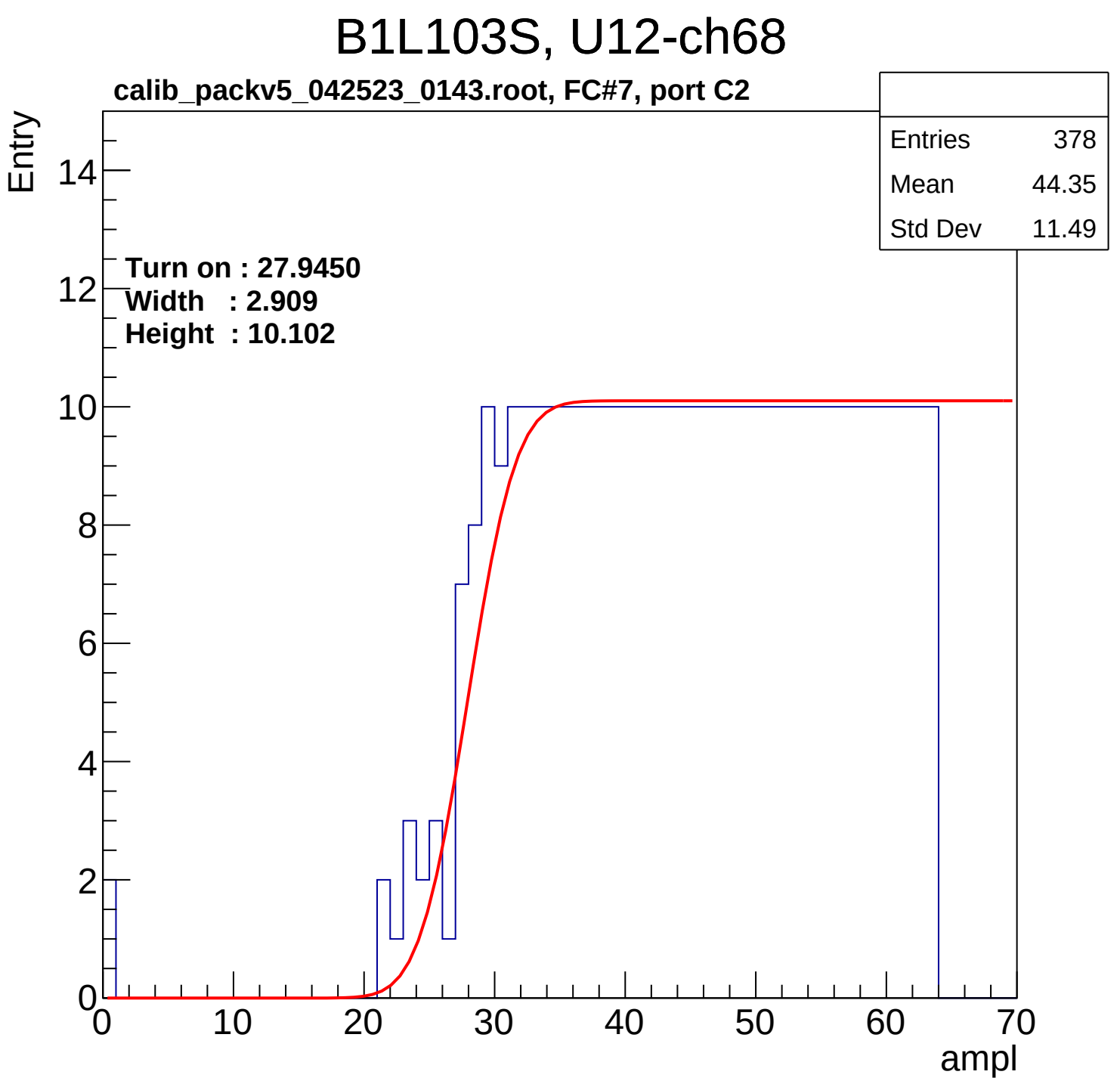

B1L103S, U12-ch63
calib_packv5_042523_0143.root, FC#7, port C2
Entries 372
Mean 44.59
Std Dev 11.41
Turn on : 27.1730
Width : 3.850
Height : 10.016
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

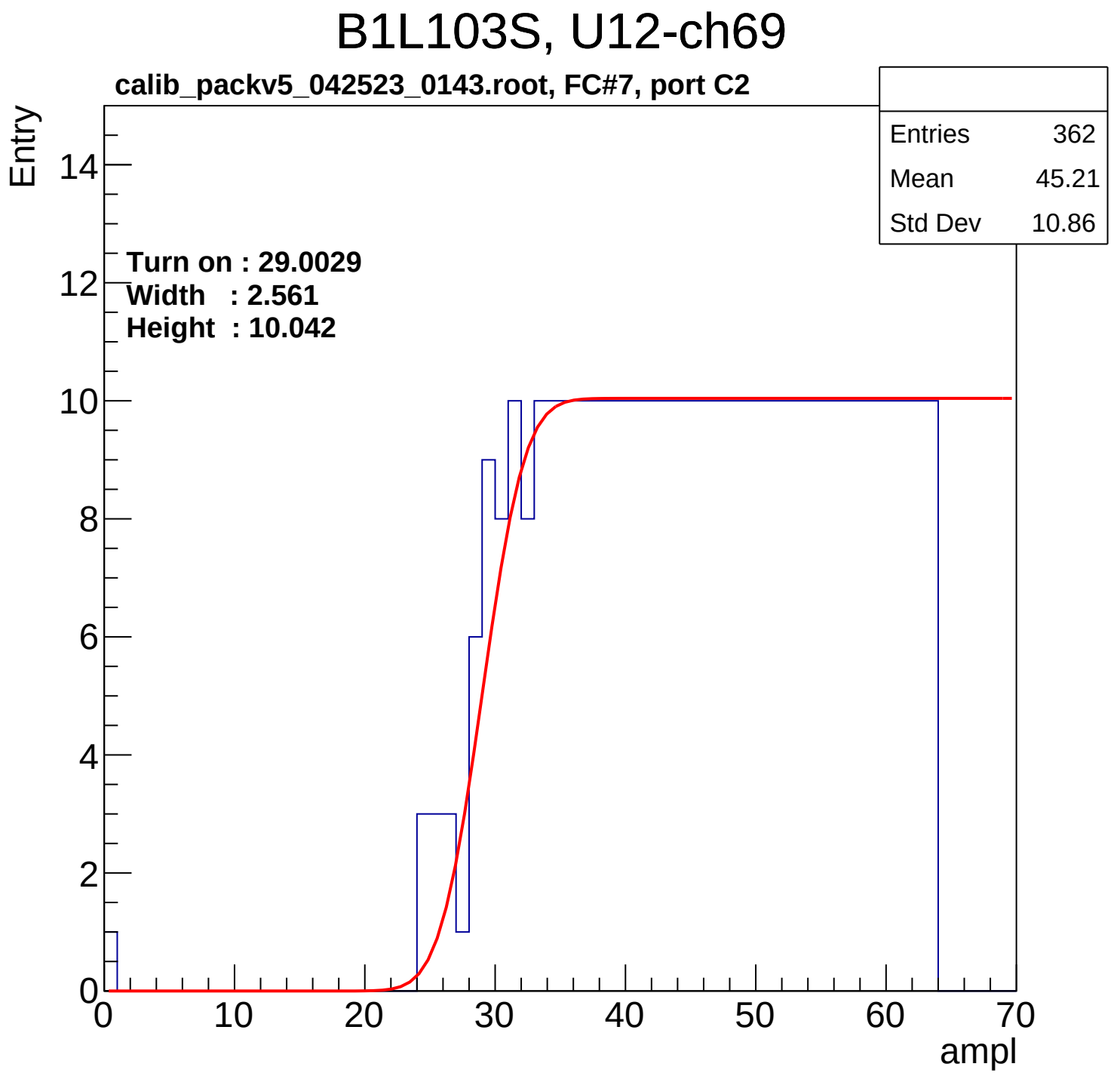

B1L103S, U12-ch64
calib_packv5_042523_0143.root, FC#7, port C2
Entries 386
Mean 43.94
Std Dev 11.91
Turn on : 25.7818
Width : 2.680
Height : 10.039
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

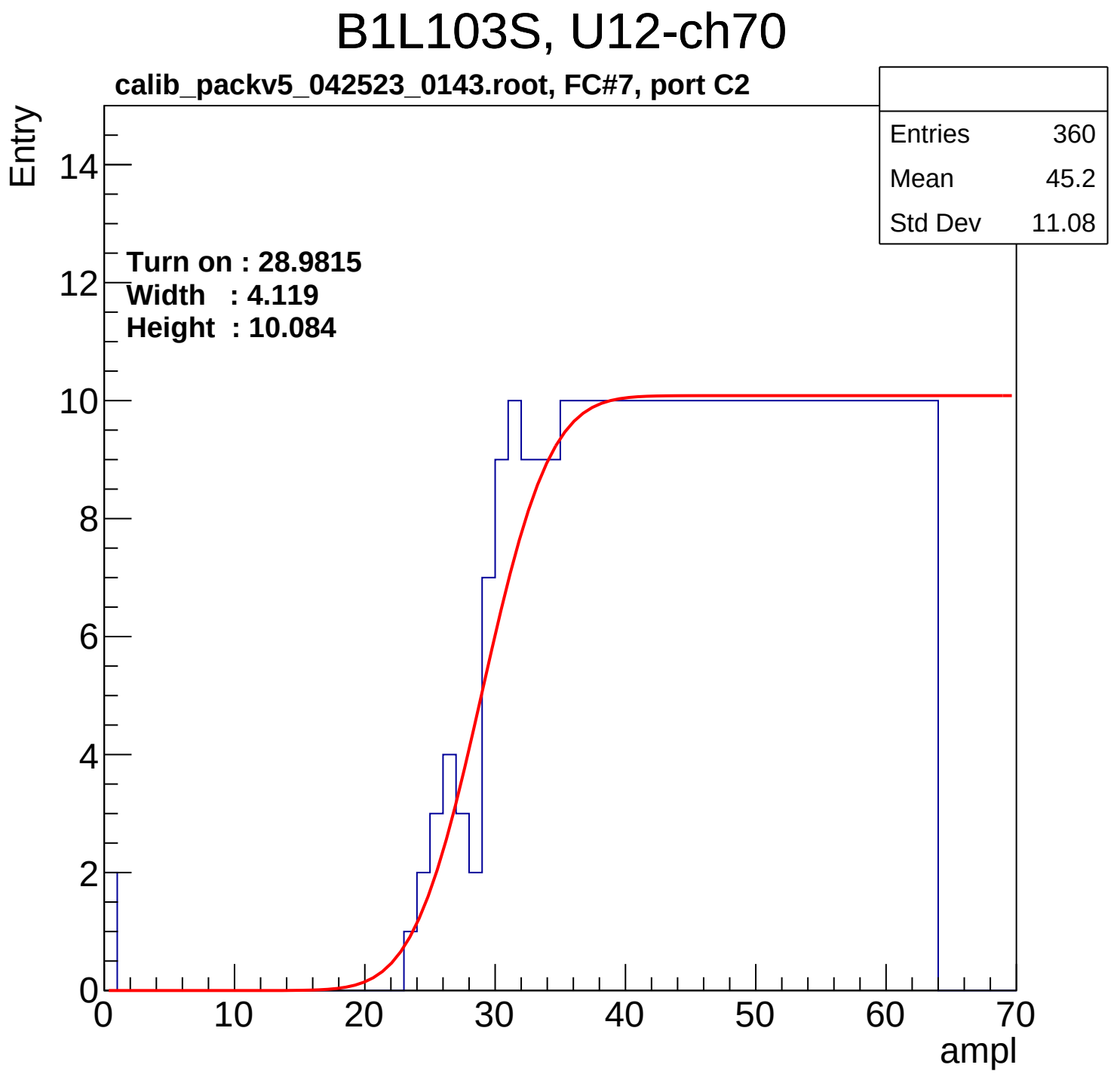

B1L103S, U12-ch65
calib_packv5_042523_0143.root, FC#7, port C2
Entries 363
Mean 44.98
Std Dev 11.35
Turn on : 28.1354
Width : 3.164
Height : 9.975
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

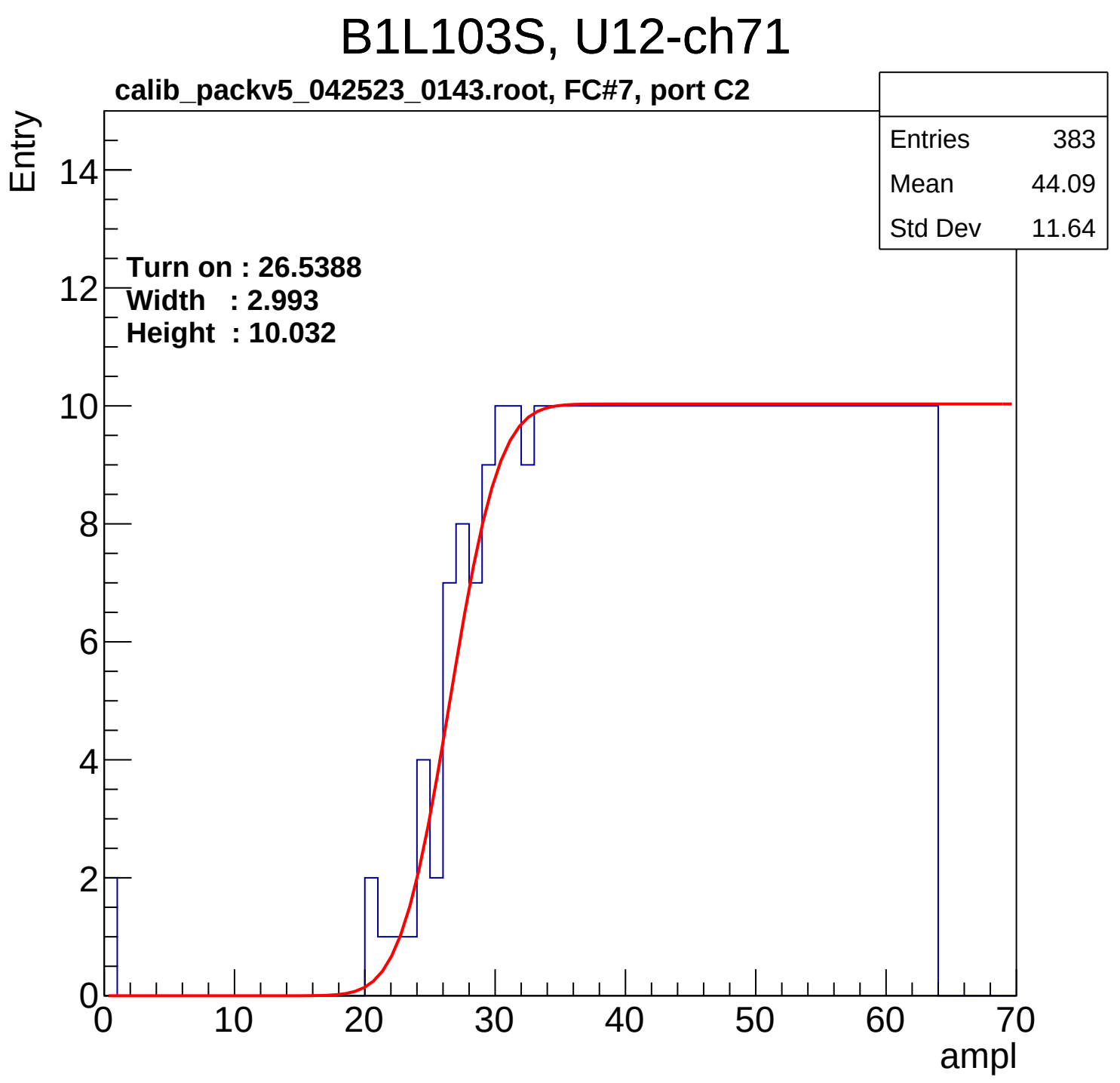

B1L103S, U12-ch66
calib_packv5_042523_0143.root, FC#7, port C2
Entries 391
Mean 43.75
Std Dev 11.69
Turn on : 25.7352
Width : 4.245
Height : 10.097
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

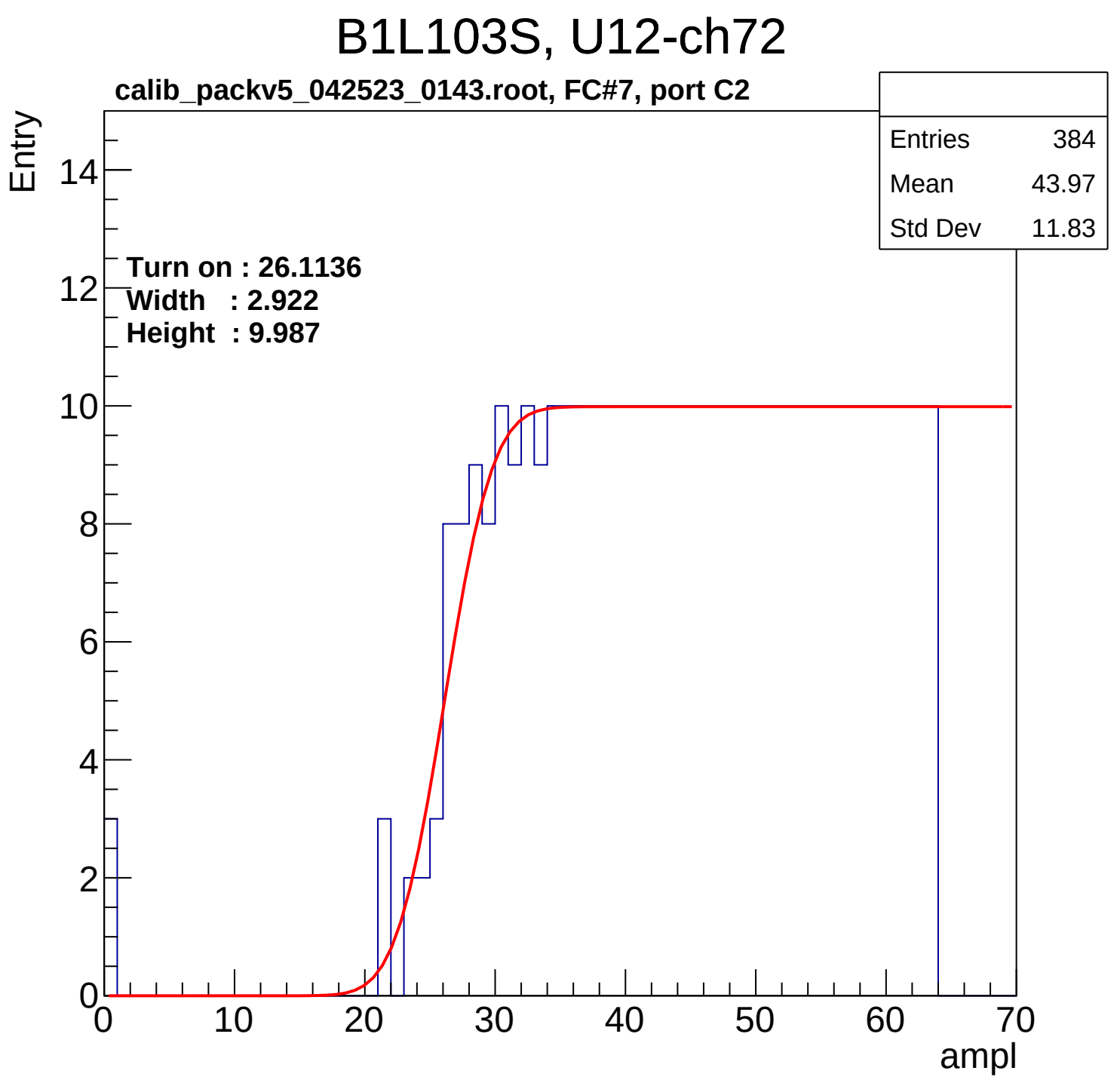

B1L103S, U12-ch67
calib_packv5_042523_0143.root, FC#7, port C2
Entries 370
Mean 44.74
Std Dev 11.37
Turn on : 27.3606
Width : 2.151
Height : 9.995
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

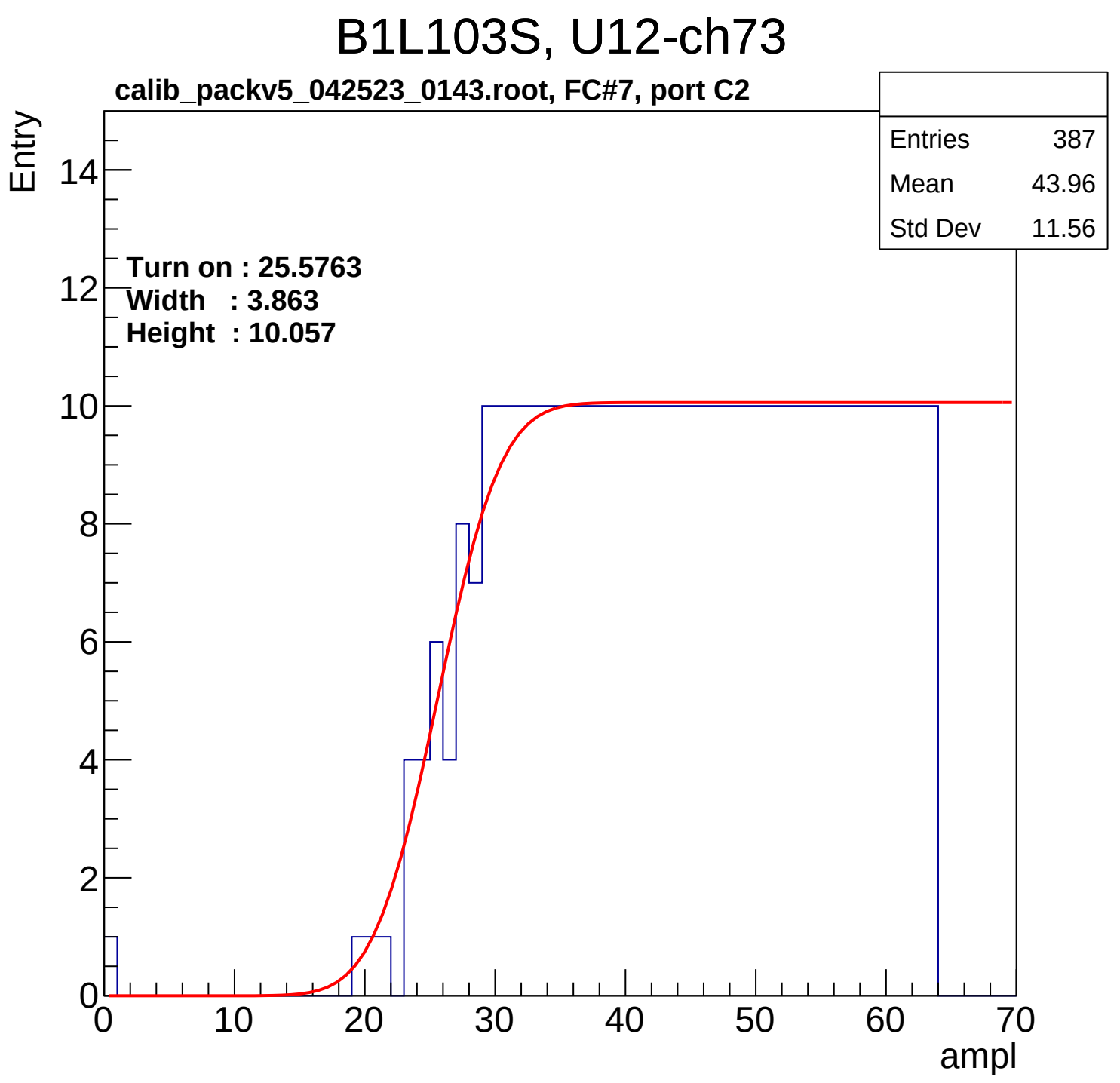

B1L103S, U12-ch68
calib_packv5_042523_0143.root, FC#7, port C2
Entries 378
Mean 44.35
Std Dev 11.49
Turn on : 27.9450
Width : 2.909
Height : 10.102
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

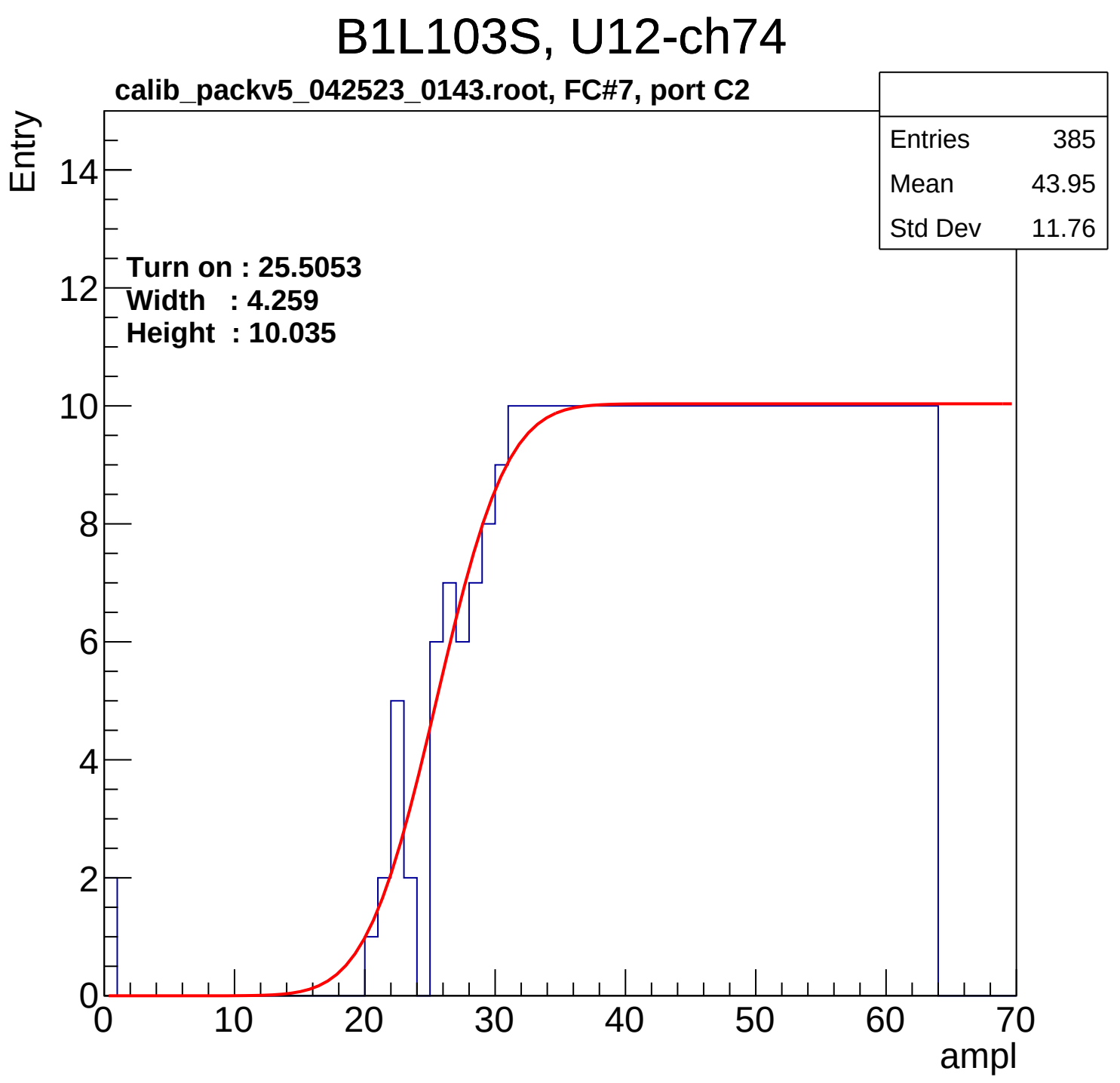

B1L103S, U12-ch69
calib_packv5_042523_0143.root, FC#7, port C2
Entries 362
Mean 45.21
Std Dev 10.86
Turn on : 29.0029
Width : 2.561
Height : 10.042
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

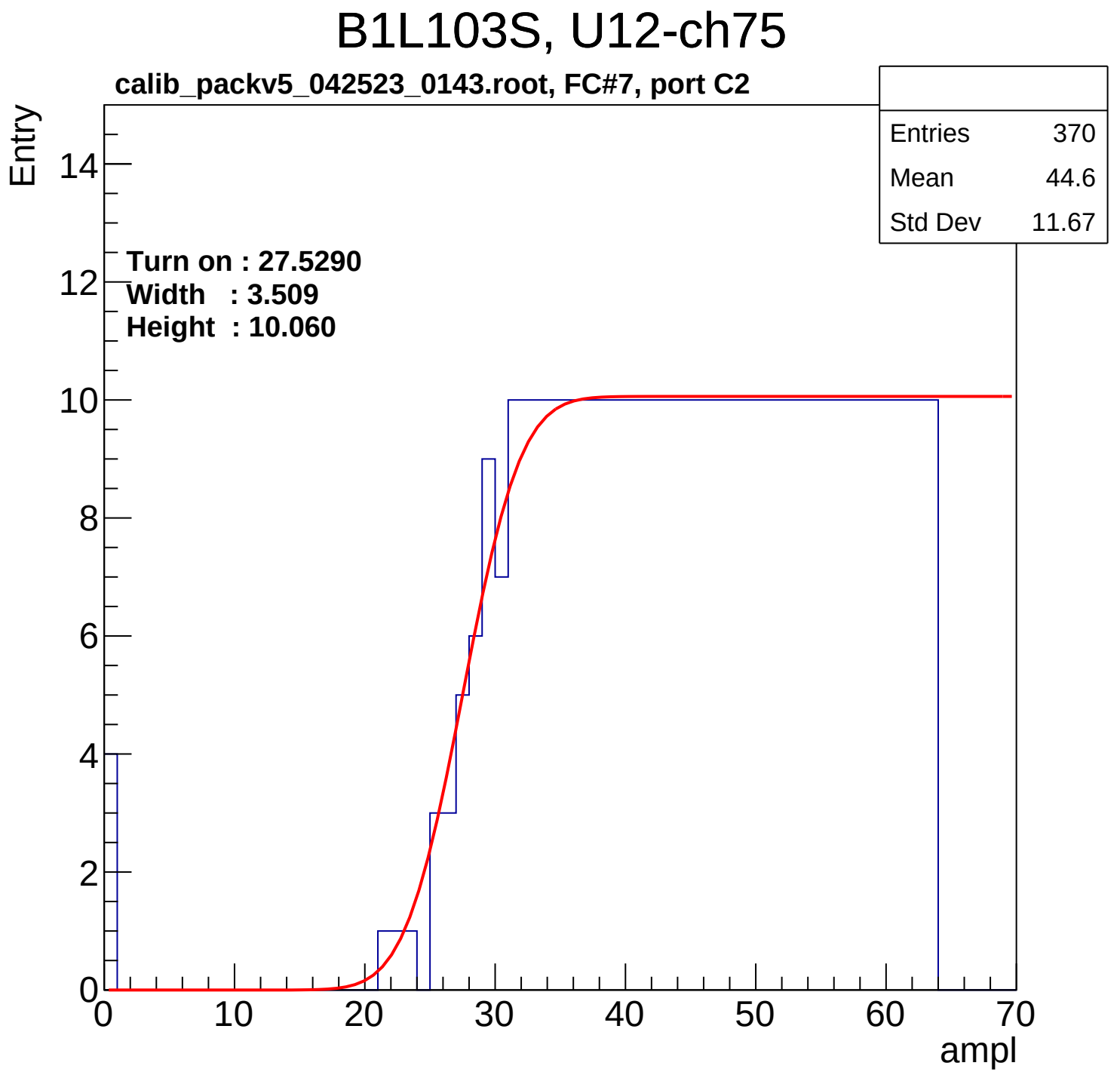

B1L103S, U12-ch70
calib_packv5_042523_0143.root, FC#7, port C2
Entries 360
Mean 45.2
Std Dev 11.08
Turn on : 28.9815
Width : 4.119
Height : 10.084
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

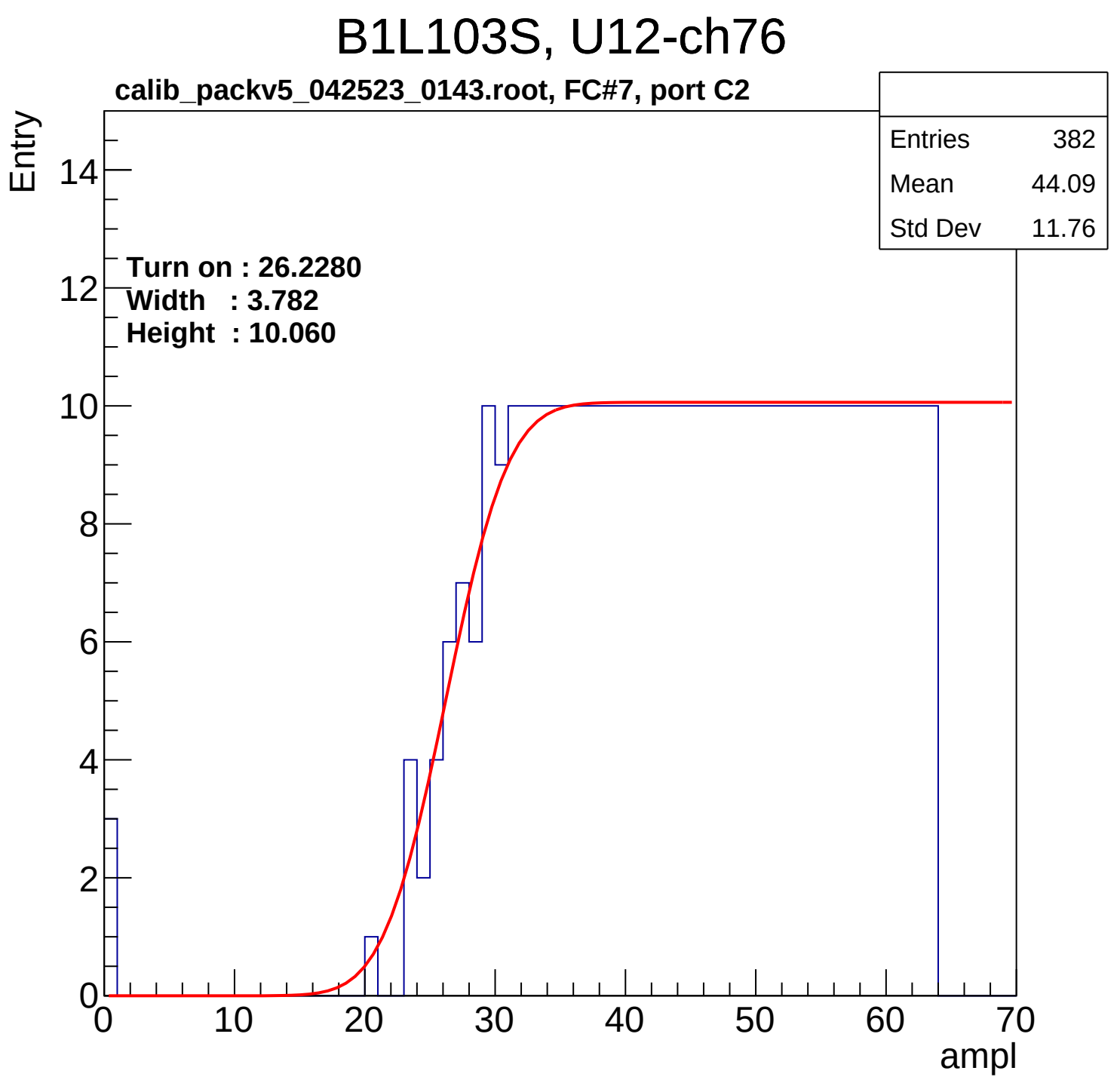

B1L103S, U12-ch71
calib_packv5_042523_0143.root, FC#7, port C2
Entries 383
Mean 44.09
Std Dev 11.64
Turn on : 26.5388
Width : 2.993
Height : 10.032
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

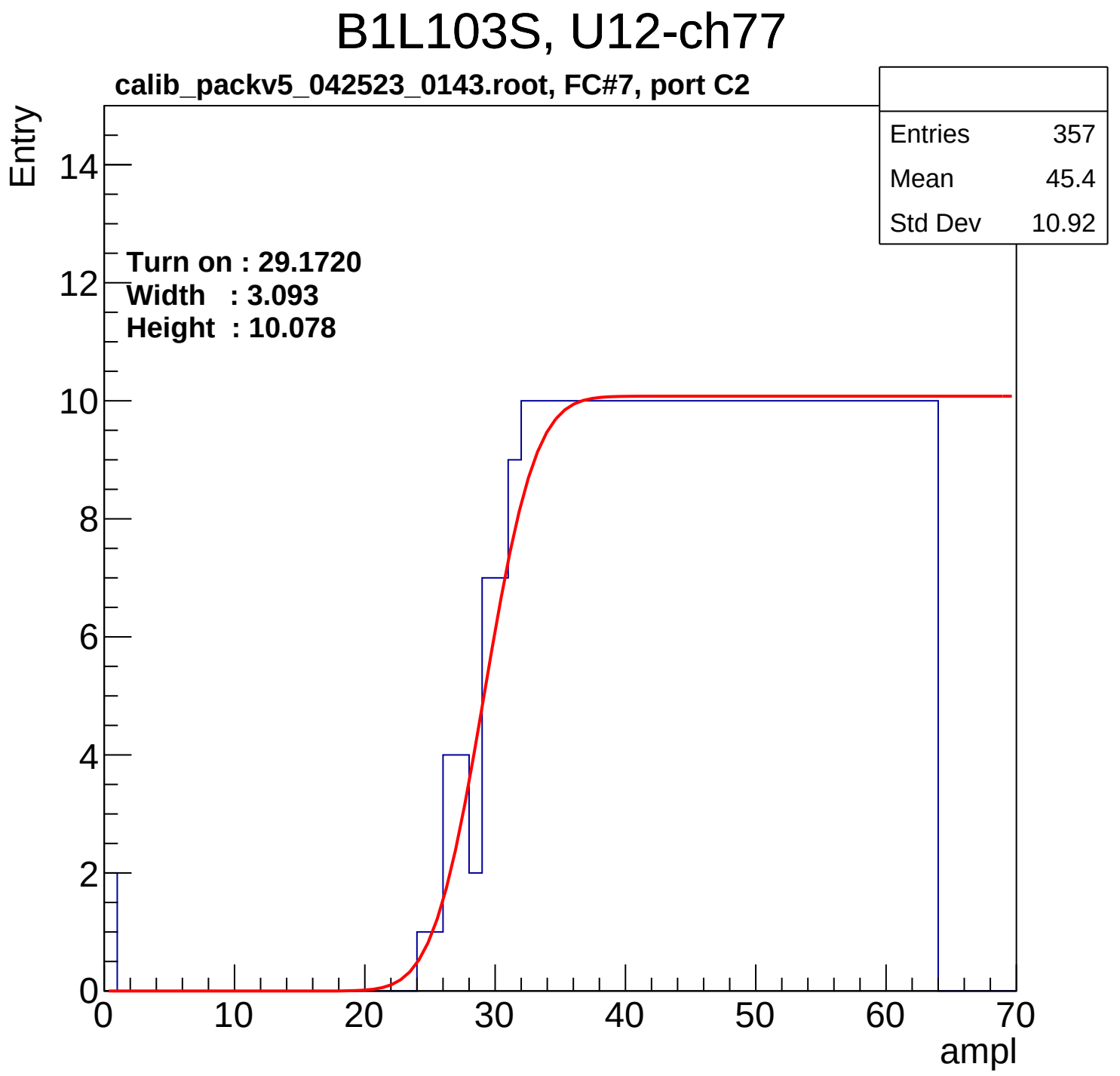

B1L103S, U12-ch72
calib_packv5_042523_0143.root, FC#7, port C2
Entries 384
Mean 43.97
Std Dev 11.83
Turn on : 26.1136
Width : 2.922
Height : 9.987
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

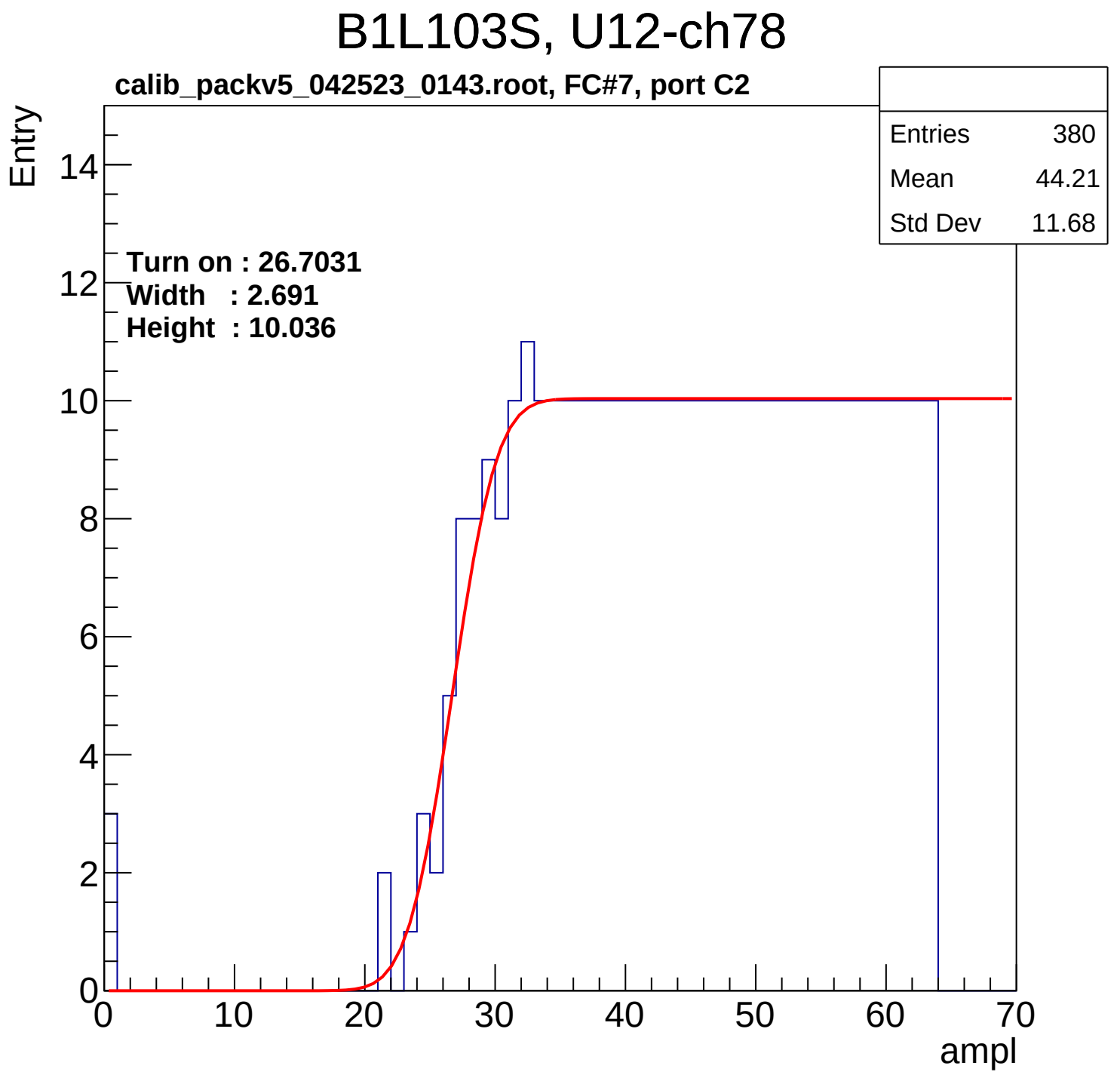

B1L103S, U12-ch73
calib_packv5_042523_0143.root, FC#7, port C2
Entries 387
Mean 43.96
Std Dev 11.56
Turn on : 25.5763
Width : 3.863
Height : 10.057
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

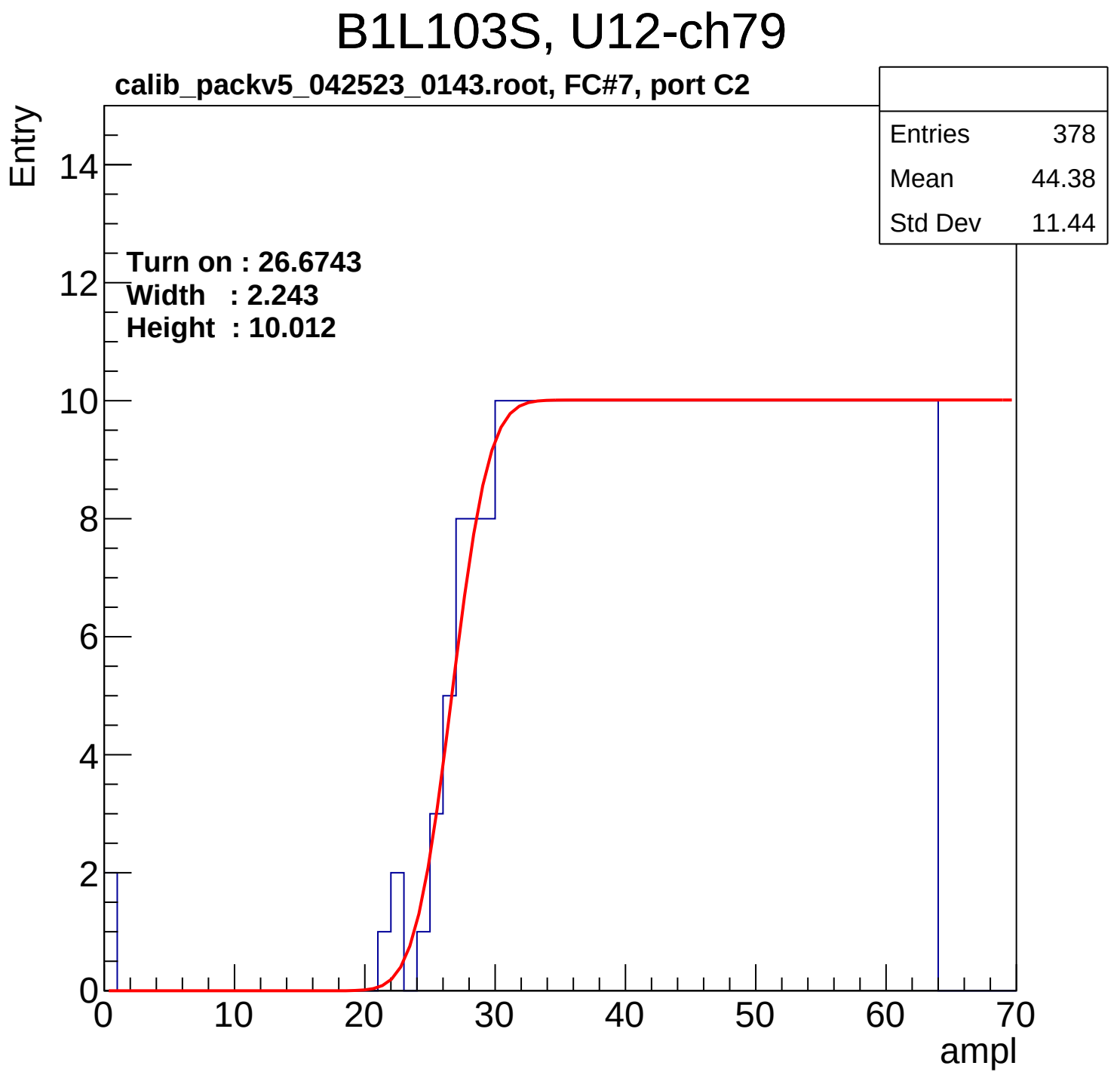

B1L103S, U12-ch74
calib_packv5_042523_0143.root, FC#7, port C2
Entries 385
Mean 43.95
Std Dev 11.76
Turn on : 25.5053
Width : 4.259
Height : 10.035
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

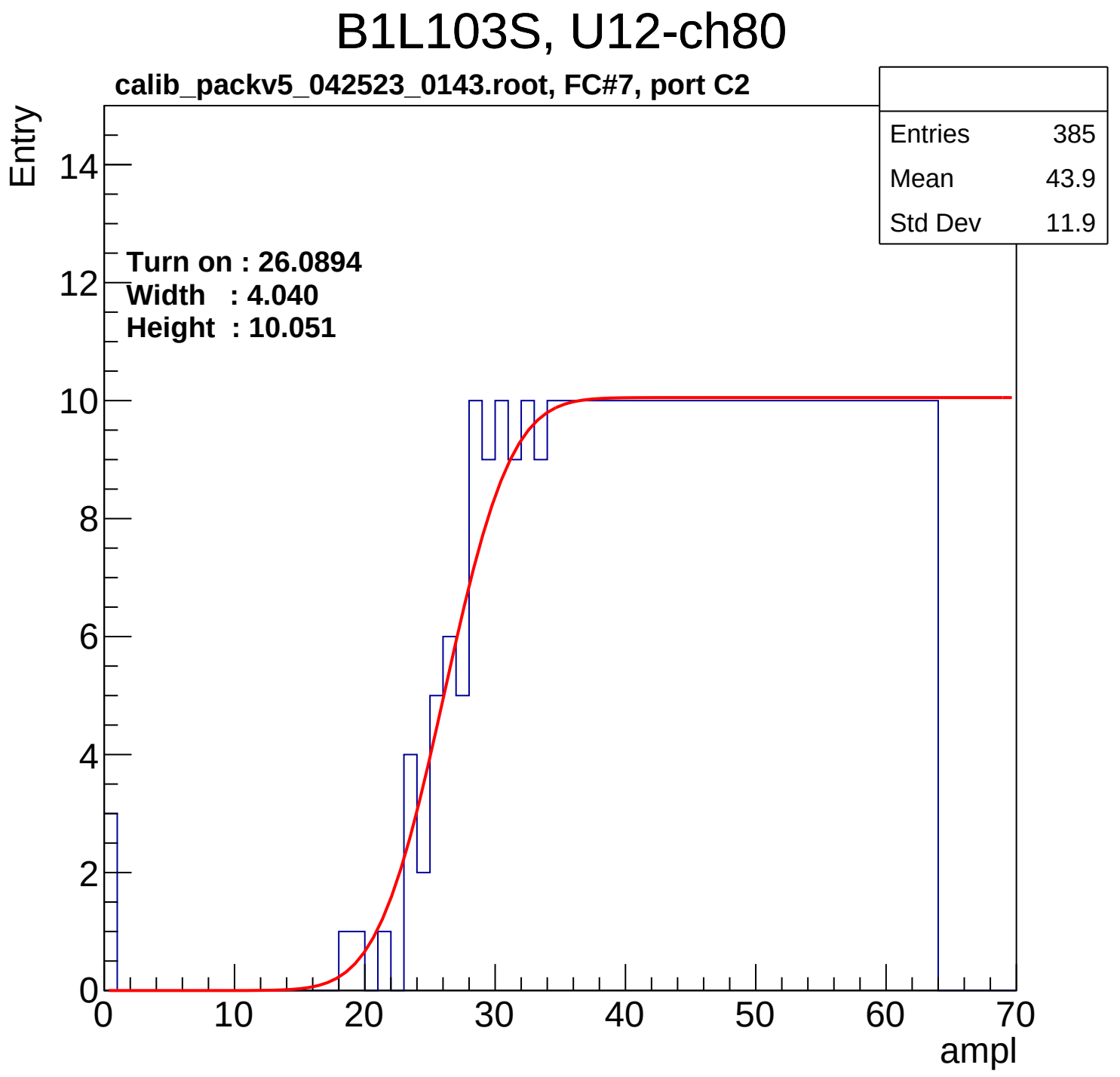

B1L103S, U12-ch75
calib_packv5_042523_0143.root, FC#7, port C2
Entries 370
Mean 44.6
Std Dev 11.67
Turn on : 27.5290
Width : 3.509
Height : 10.060
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

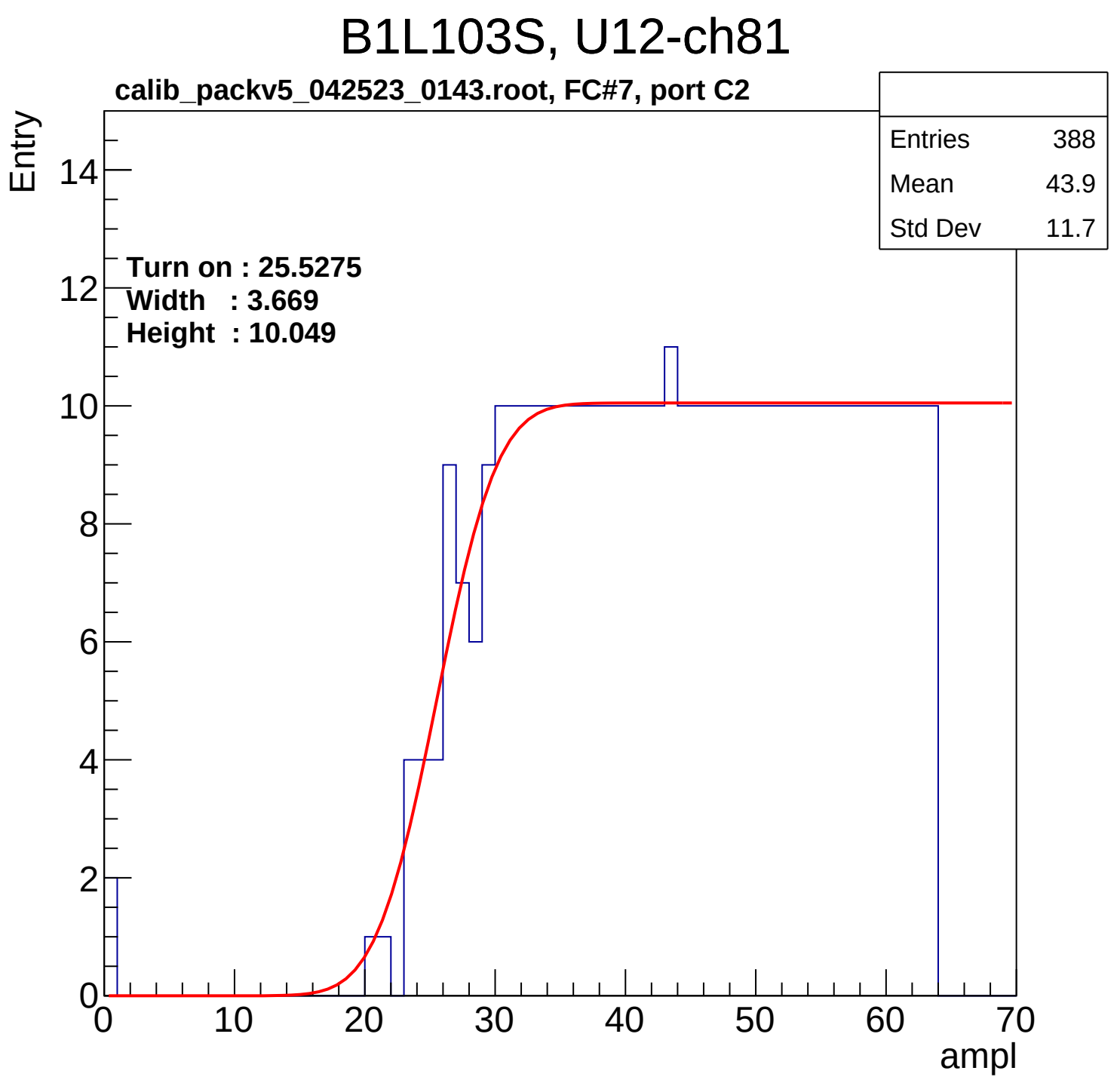

B1L103S, U12-ch76
calib_packv5_042523_0143.root, FC#7, port C2
Entries 382
Mean 44.09
Std Dev 11.76
Turn on : 26.2280
Width : 3.782
Height : 10.060
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

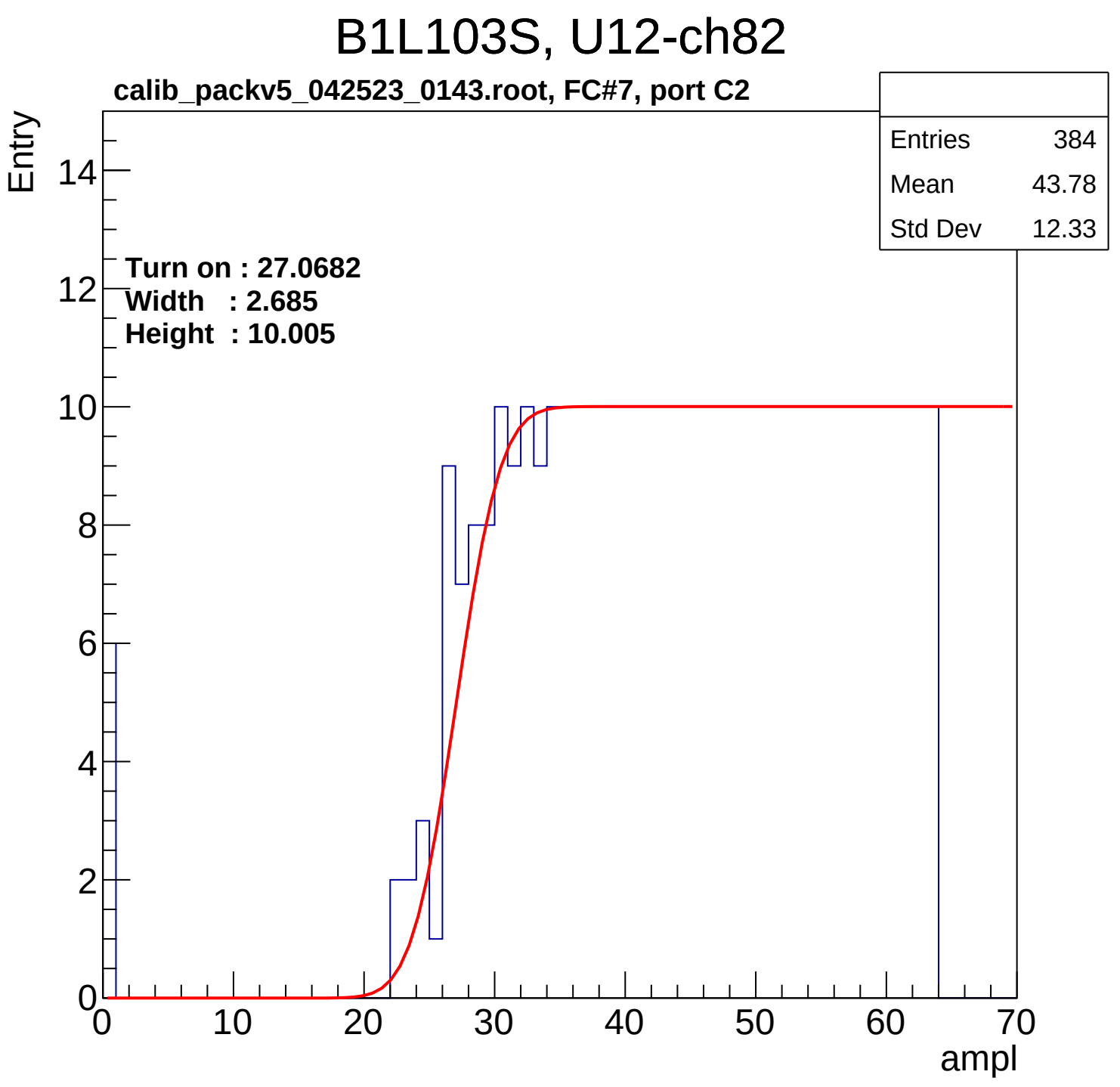

B1L103S, U12-ch77
calib_packv5_042523_0143.root, FC#7, port C2
Entries 357
Mean 45.4
Std Dev 10.92
Turn on : 29.1720
Width : 3.093
Height : 10.078
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

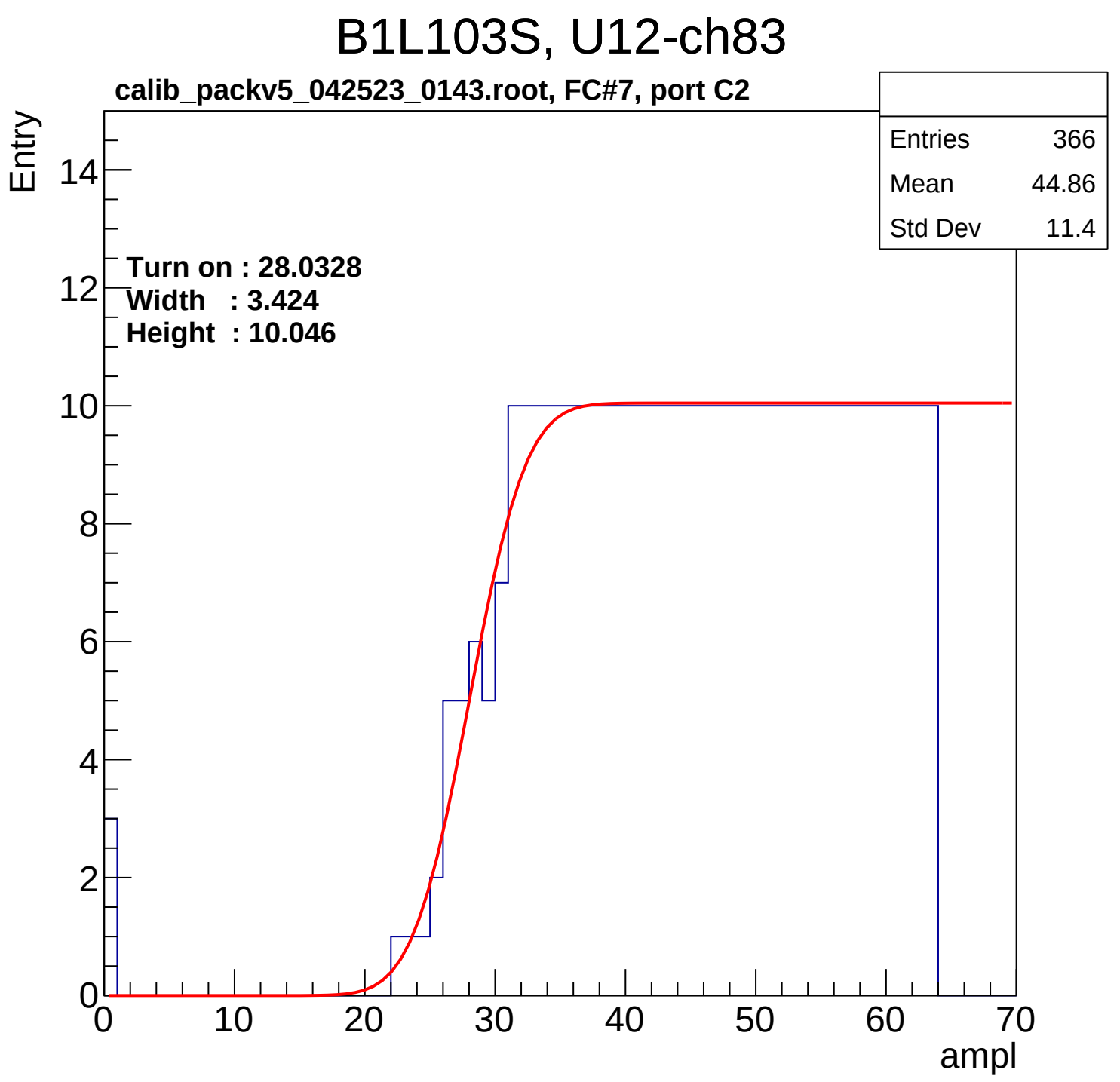

B1L103S, U12-ch78
calib_packv5_042523_0143.root, FC#7, port C2
Entries 380
Mean 44.21
Std Dev 11.68
Turn on : 26.7031
Width : 2.691
Height : 10.036
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

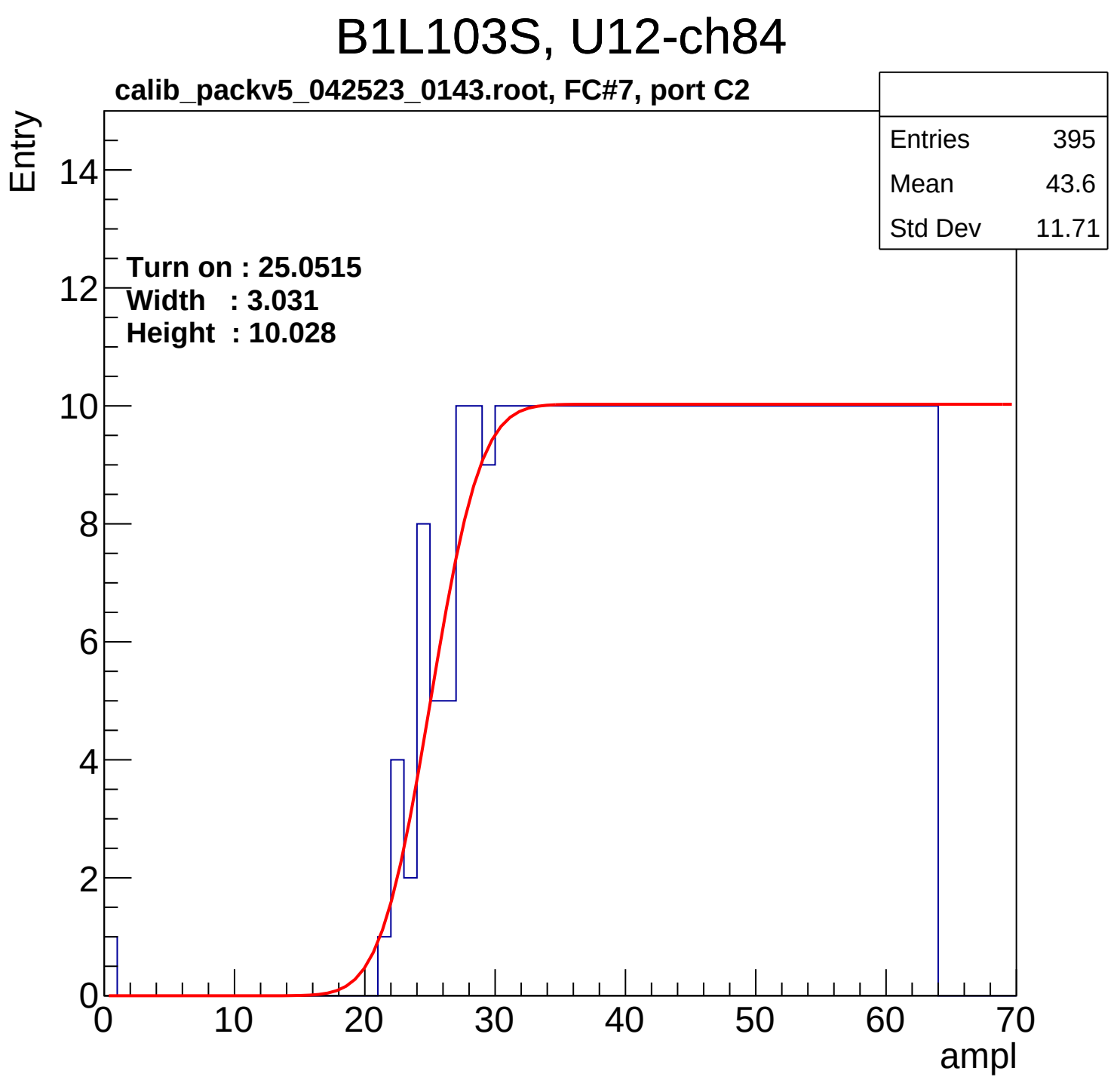

B1L103S, U12-ch79
calib_packv5_042523_0143.root, FC#7, port C2
Entries 378
Mean 44.38
Std Dev 11.44
Turn on : 26.6743
Width : 2.243
Height : 10.012
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

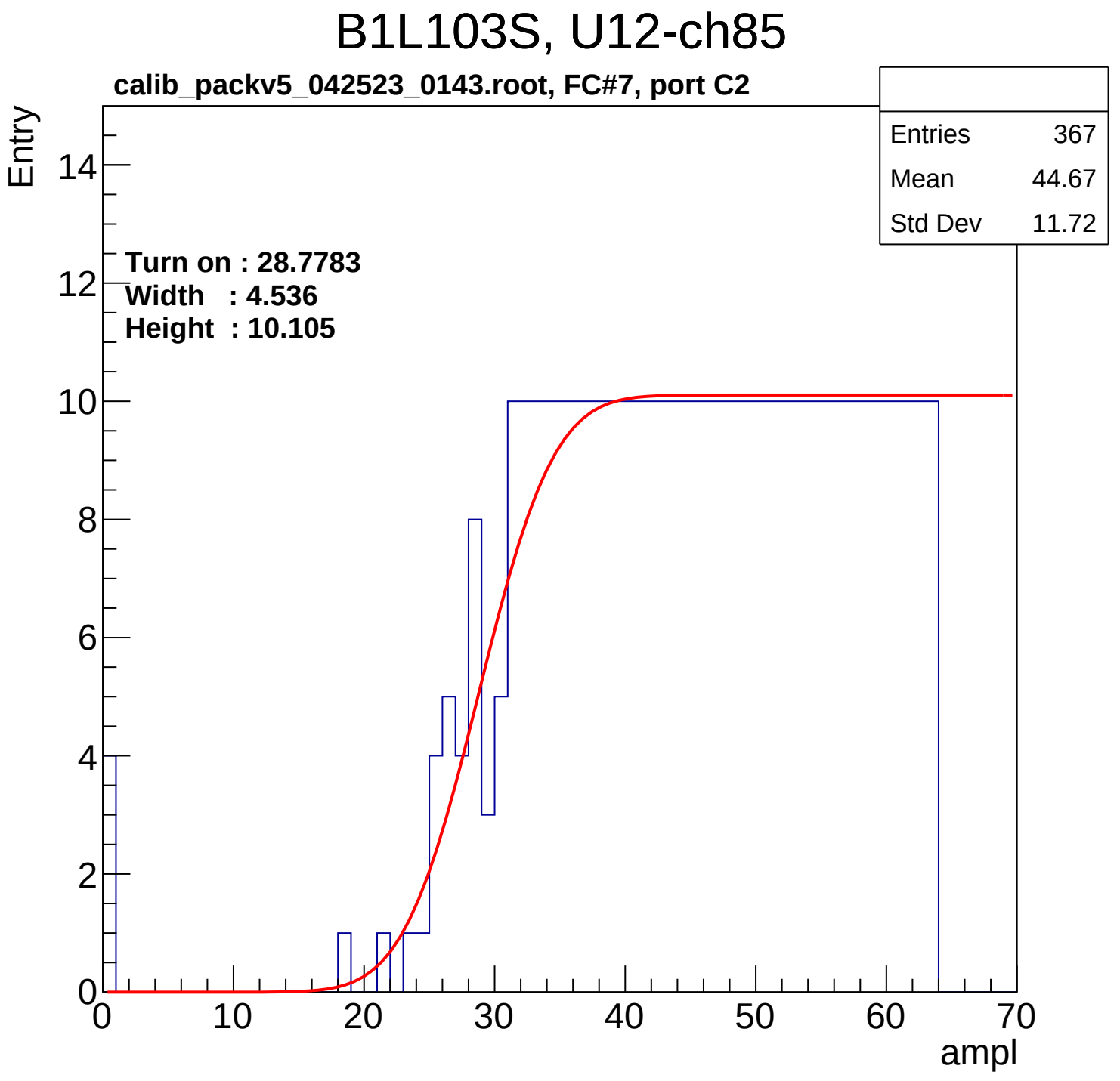

B1L103S, U12-ch80
calib_packv5_042523_0143.root, FC#7, port C2
Entries 385
Mean 43.9
Std Dev 11.9
Turn on : 26.0894
Width : 4.040
Height : 10.051
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

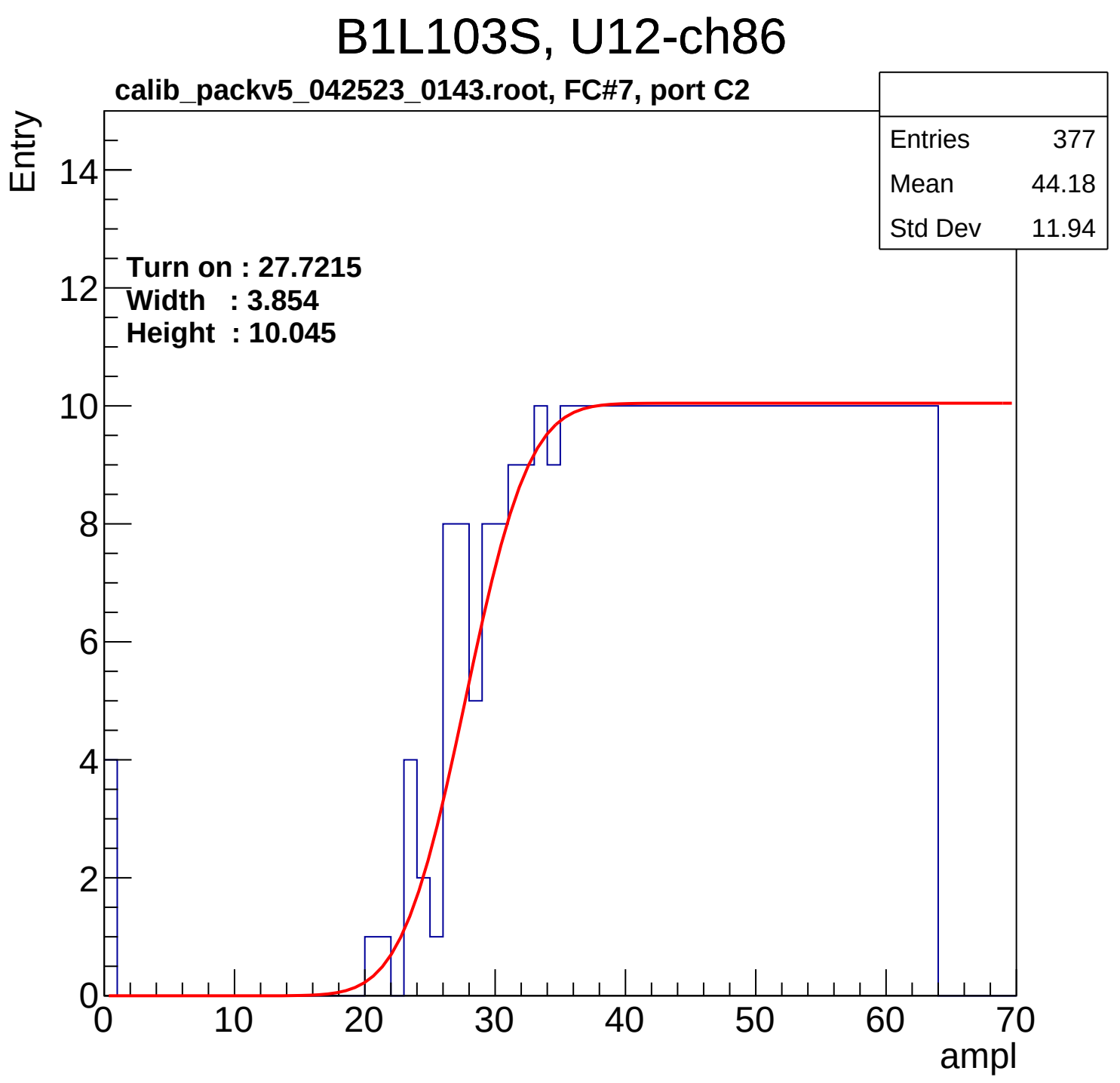

B1L103S, U12-ch81
calib_packv5_042523_0143.root, FC#7, port C2
Entries 388
Mean 43.9
Std Dev 11.7
Turn on : 25.5275
Width : 3.669
Height : 10.049
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

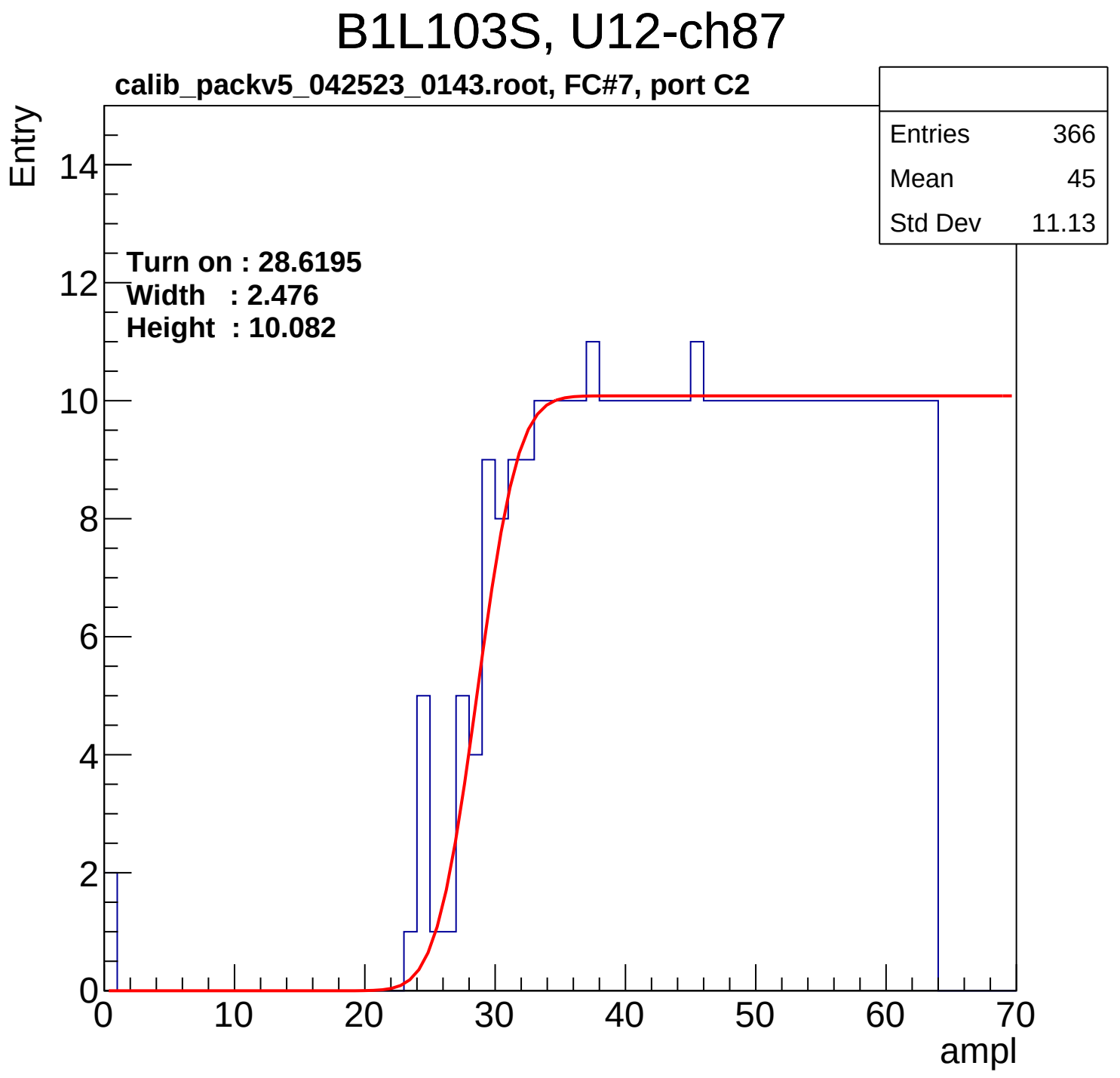

B1L103S, U12-ch82
calib_packv5_042523_0143.root, FC#7, port C2
Entries 384
Mean 43.78
Std Dev 12.33
Turn on : 27.0682
Width : 2.685
Height : 10.005
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

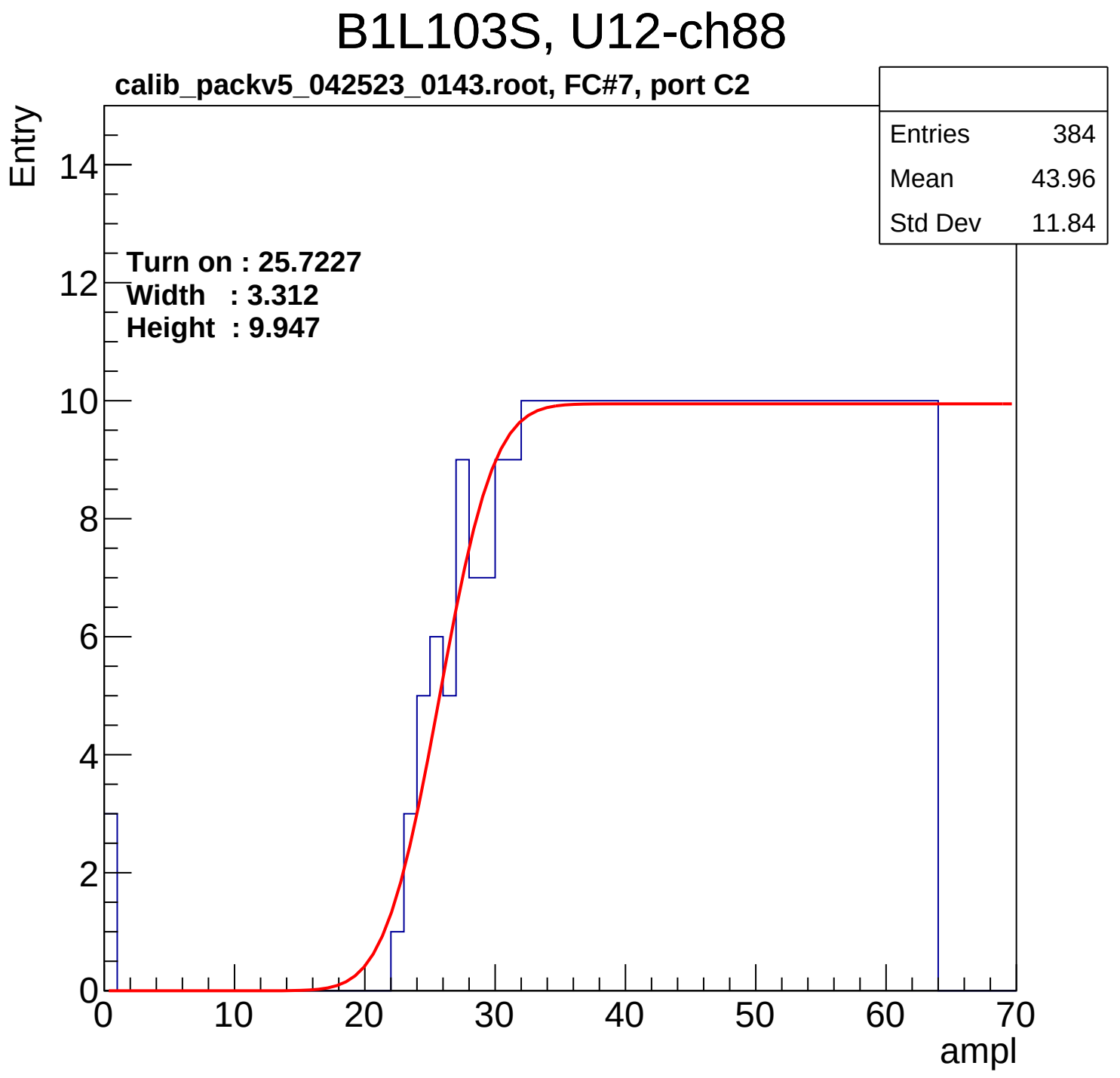

B1L103S, U12-ch83
calib_packv5_042523_0143.root, FC#7, port C2
Entries 366
Mean 44.86
Std Dev 11.4
Turn on : 28.0328
Width : 3.424
Height : 10.046
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

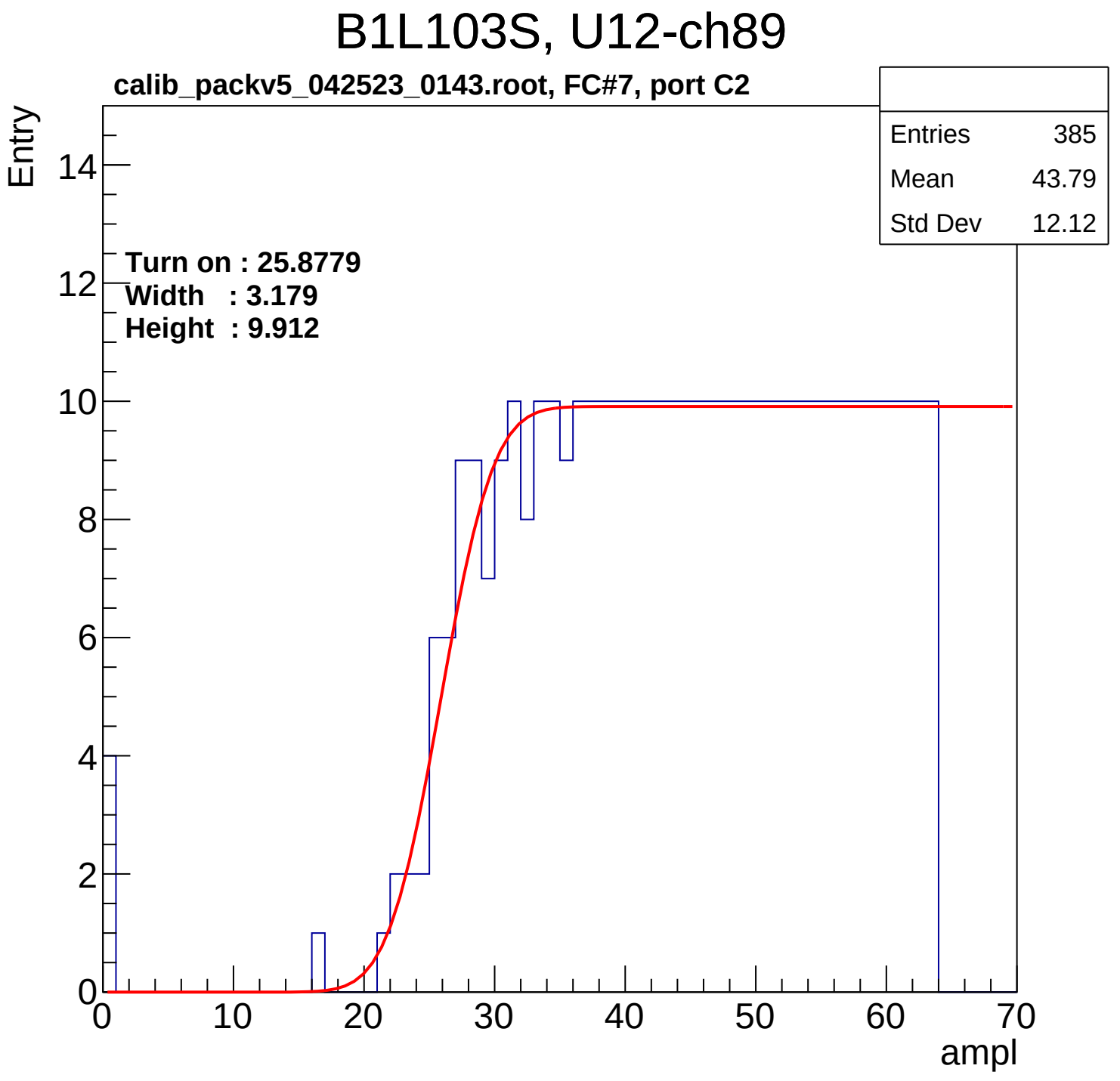

B1L103S, U12-ch84
calib_packv5_042523_0143.root, FC#7, port C2
Entries 395
Mean 43.6
Std Dev 11.71
Turn on : 25.0515
Width : 3.031
Height : 10.028
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

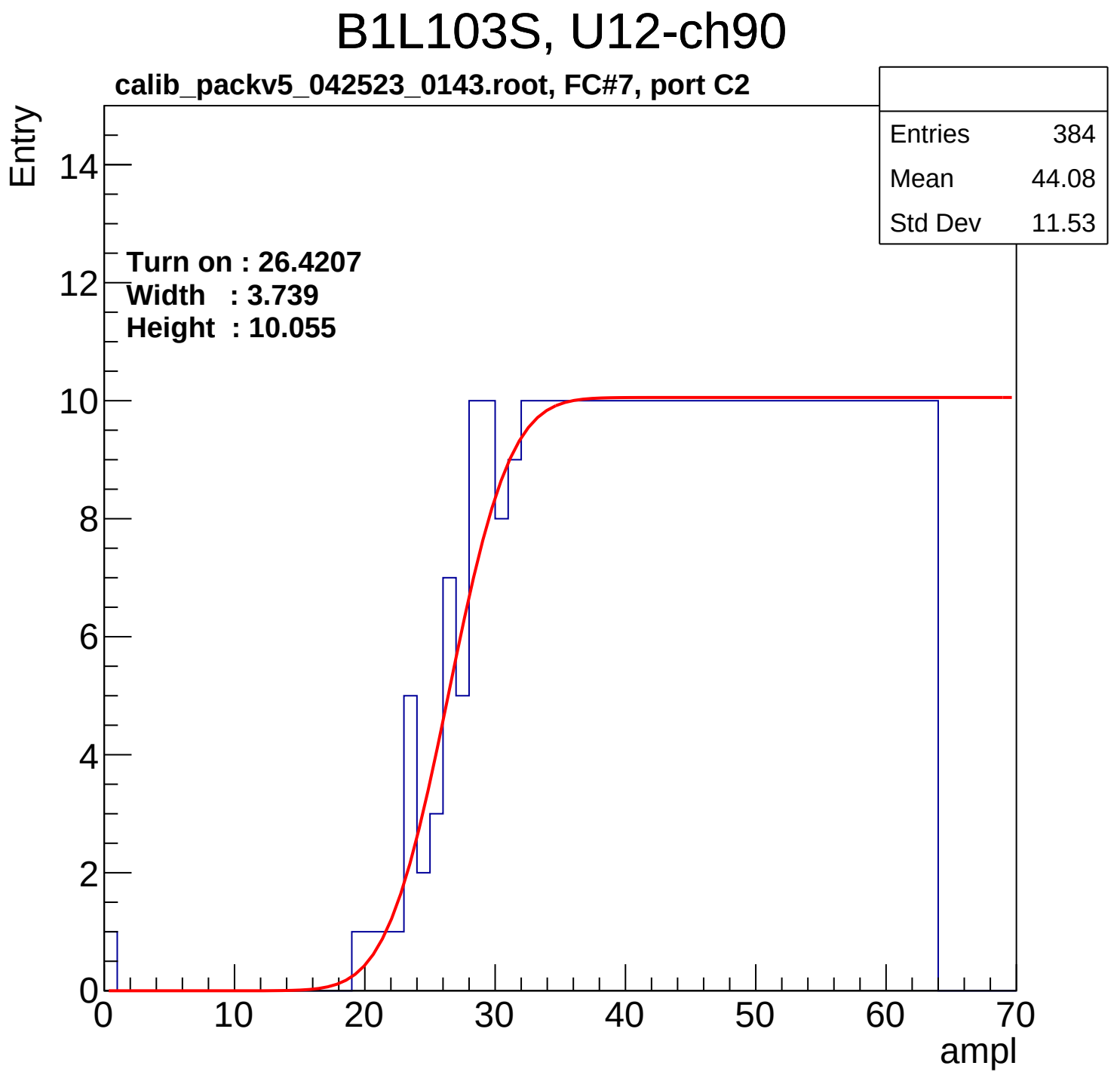

B1L103S, U12-ch85
calib_packv5_042523_0143.root, FC#7, port C2
Entries 367
Mean 44.67
Std Dev 11.72
Turn on : 28.7783
Width : 4.536
Height : 10.105
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

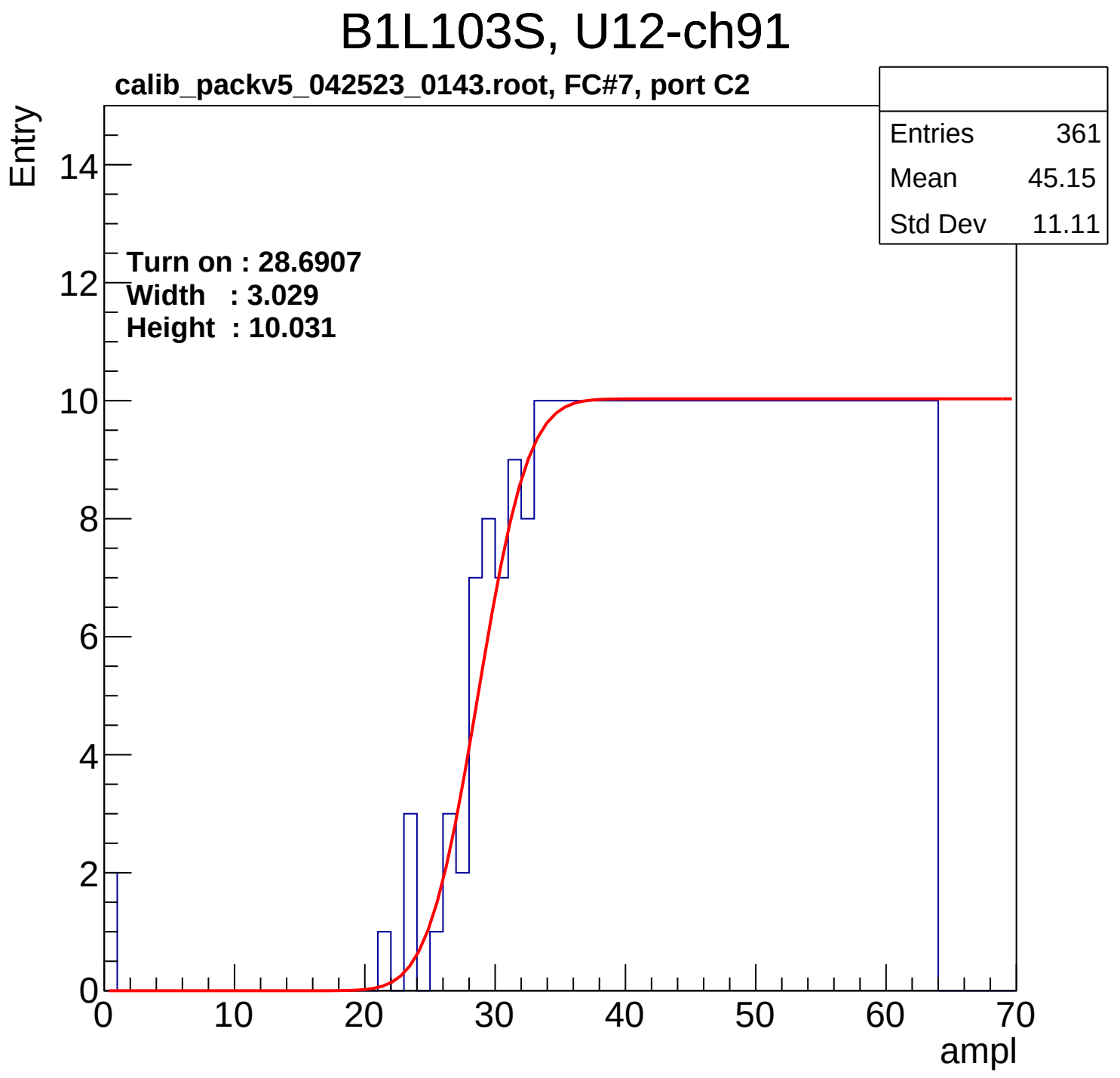

B1L103S, U12-ch86
calib_packv5_042523_0143.root, FC#7, port C2
Entries 377
Mean 44.18
Std Dev 11.94
Turn on : 27.7215
Width : 3.854
Height : 10.045
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

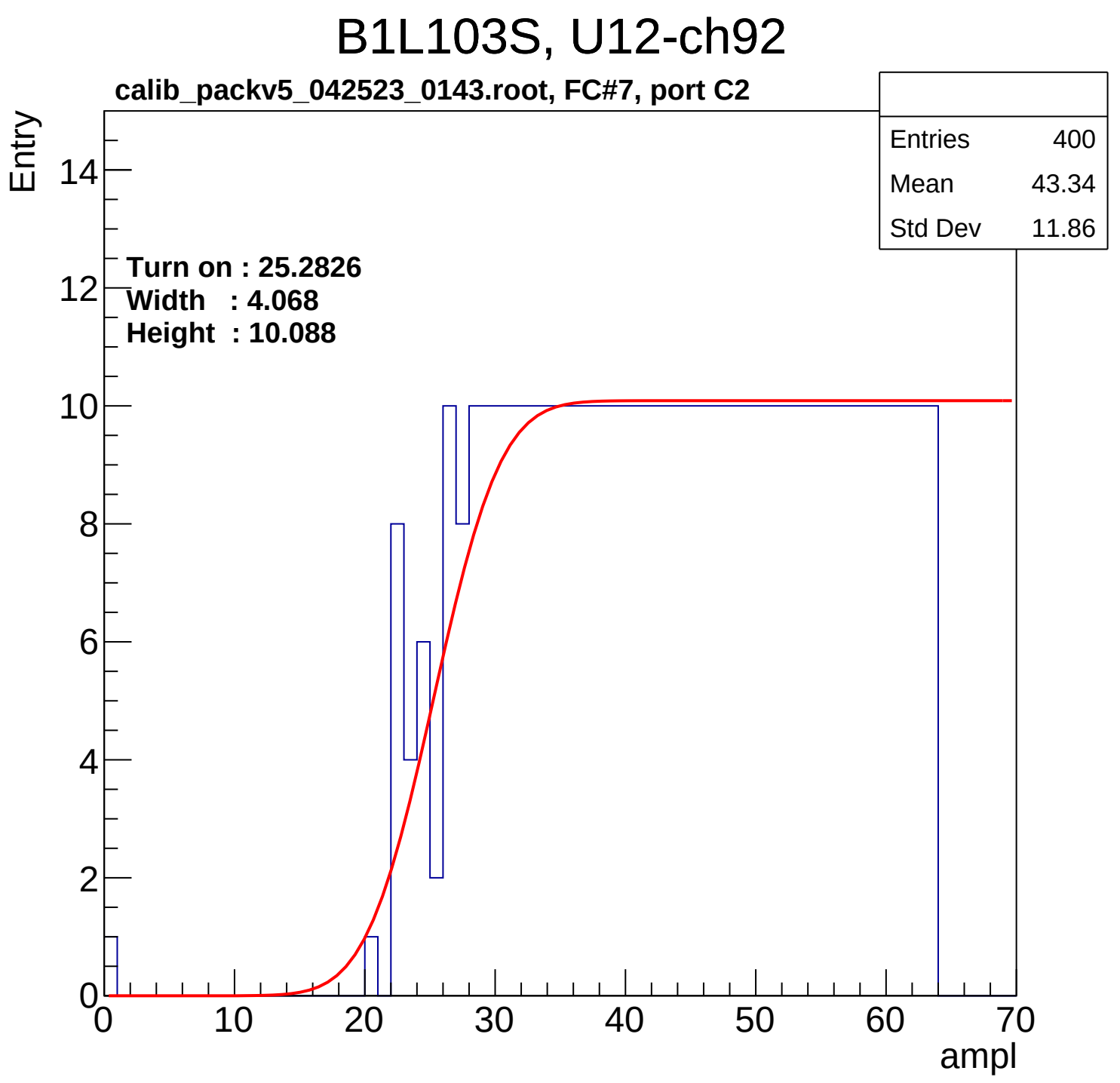

B1L103S, U12-ch87
calib_packv5_042523_0143.root, FC#7, port C2
Entries 366
Mean 45
Std Dev 11.13
Turn on : 28.6195
Width : 2.476
Height : 10.082
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

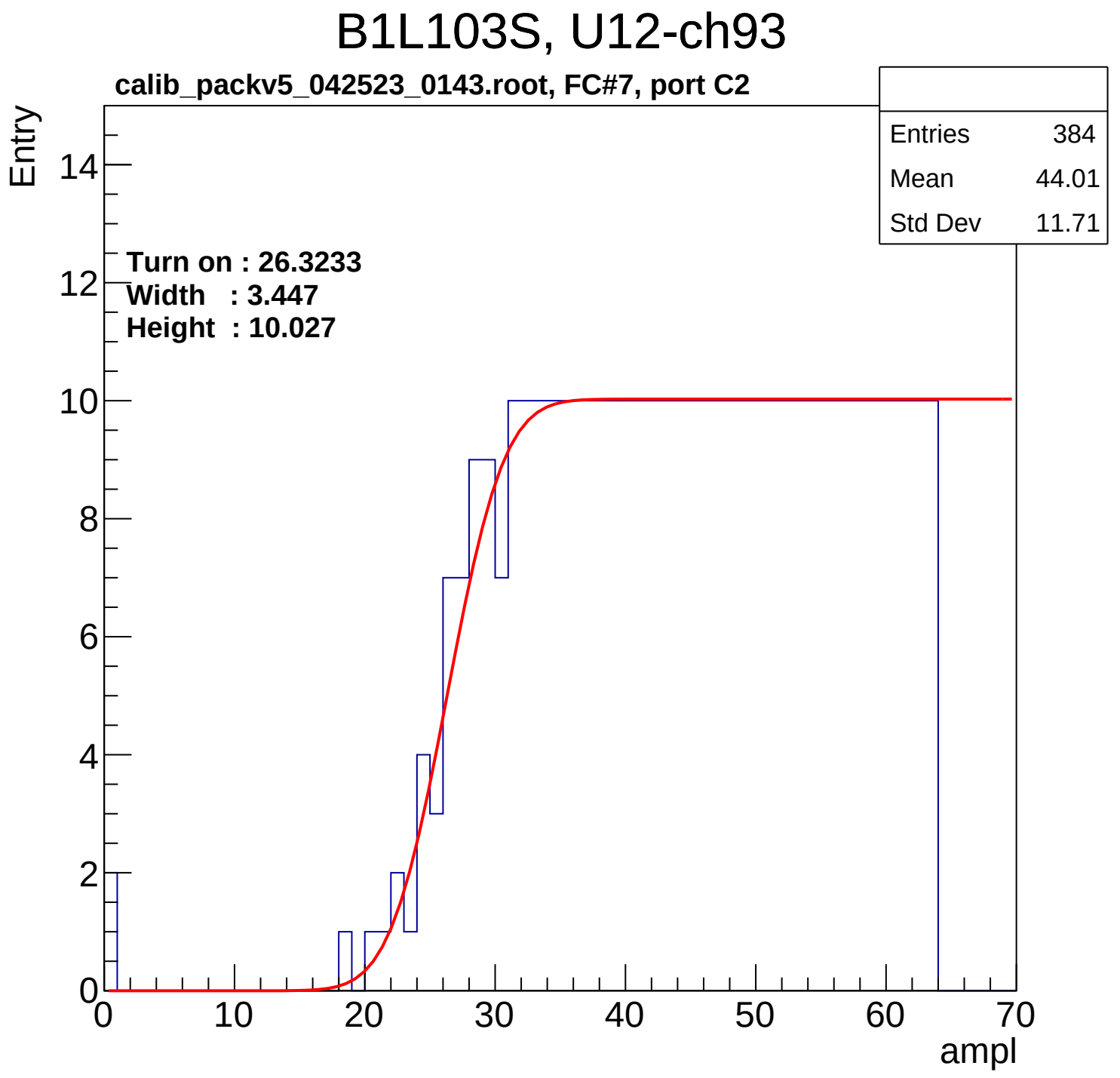

B1L103S, U12-ch88
calib_packv5_042523_0143.root, FC#7, port C2
Entries 384
Mean 43.96
Std Dev 11.84
Turn on : 25.7227
Width : 3.312
Height : 9.947
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

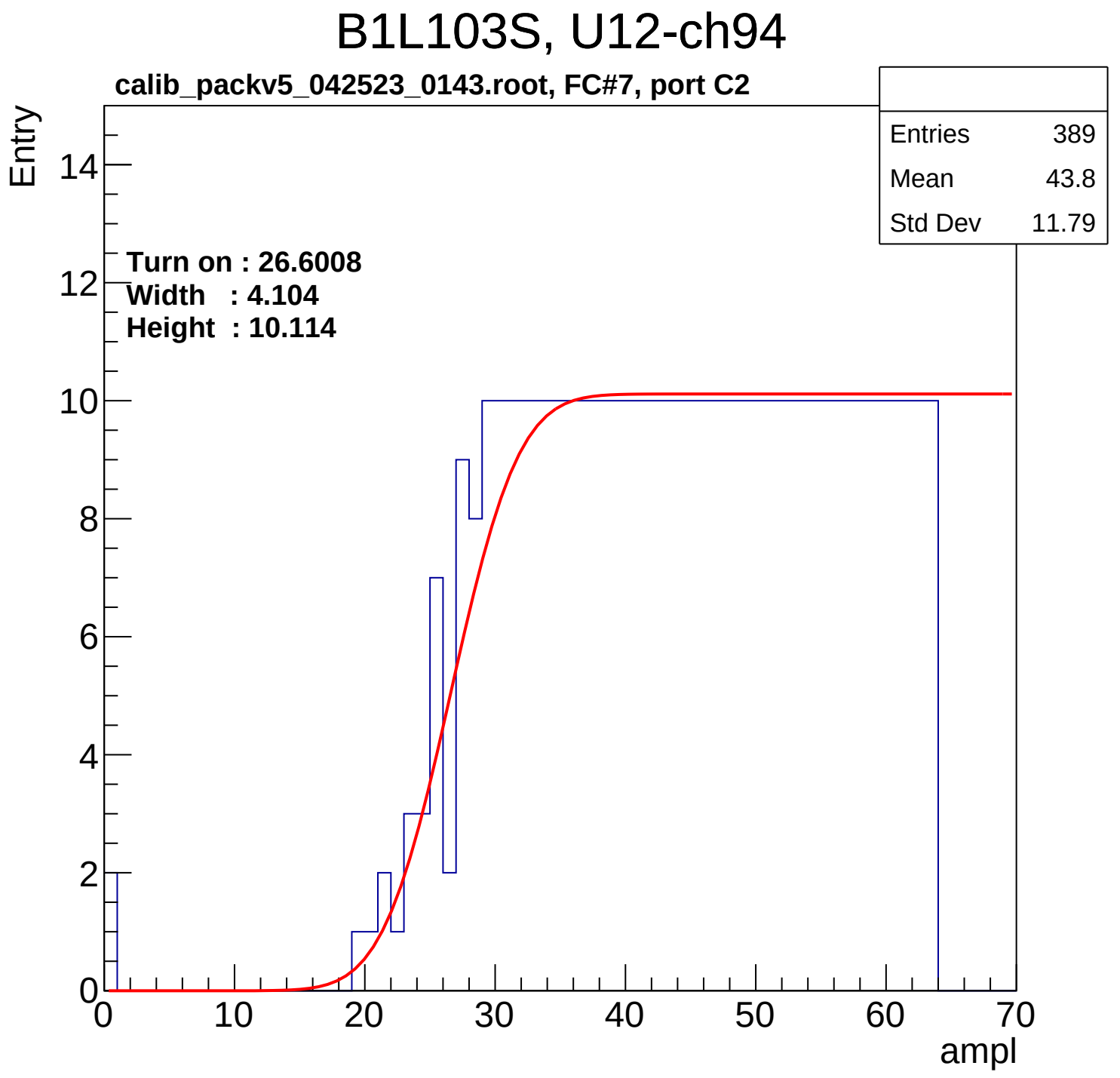

B1L103S, U12-ch89
calib_packv5_042523_0143.root, FC#7, port C2
Entries 385
Mean 43.79
Std Dev 12.12
Turn on : 25.8779
Width : 3.179
Height : 9.912
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

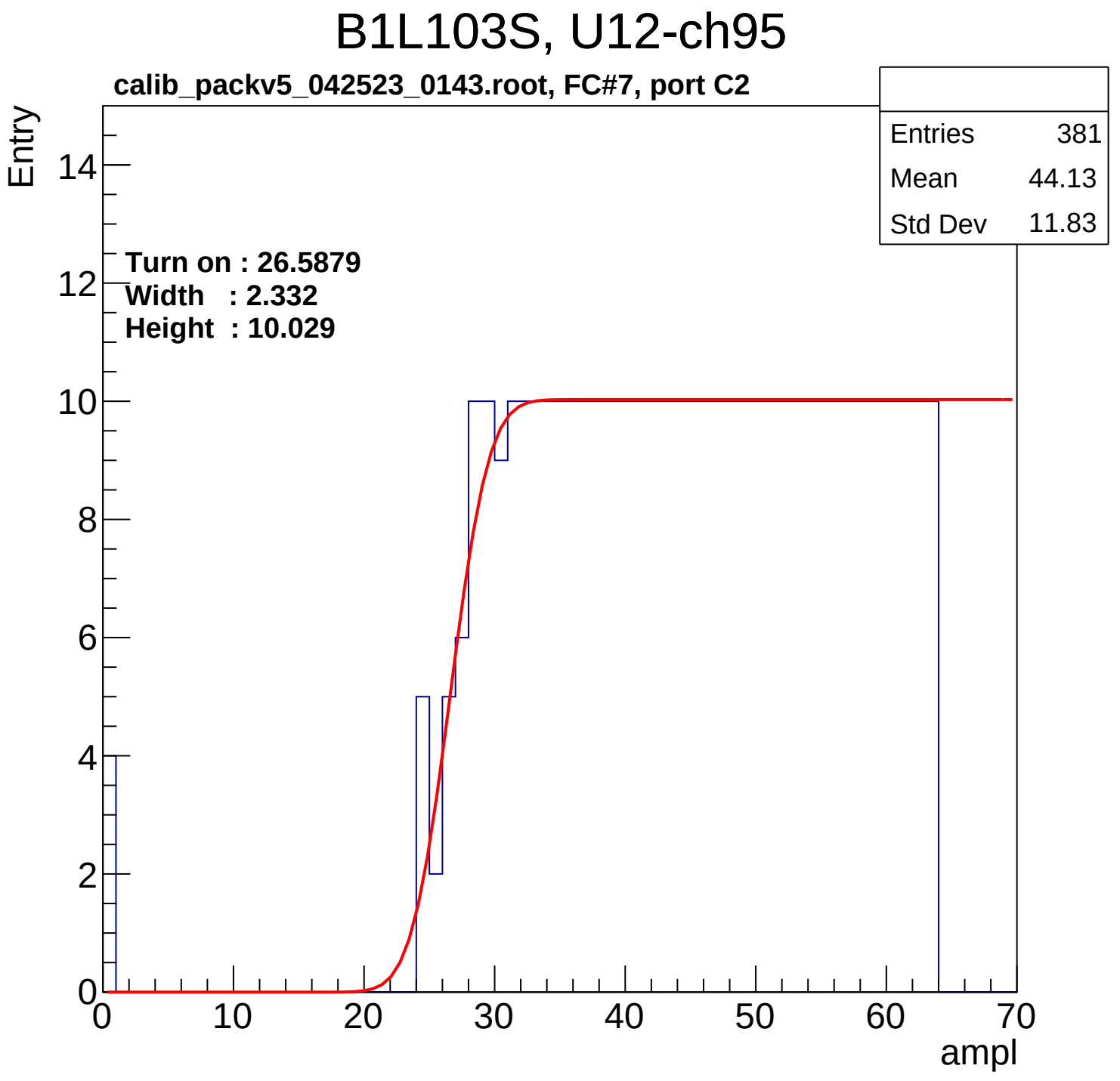

B1L103S, U12-ch90
calib_packv5_042523_0143.root, FC#7, port C2
Entries 384
Mean 44.08
Std Dev 11.53
Turn on : 26.4207
Width : 3.739
Height : 10.055
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

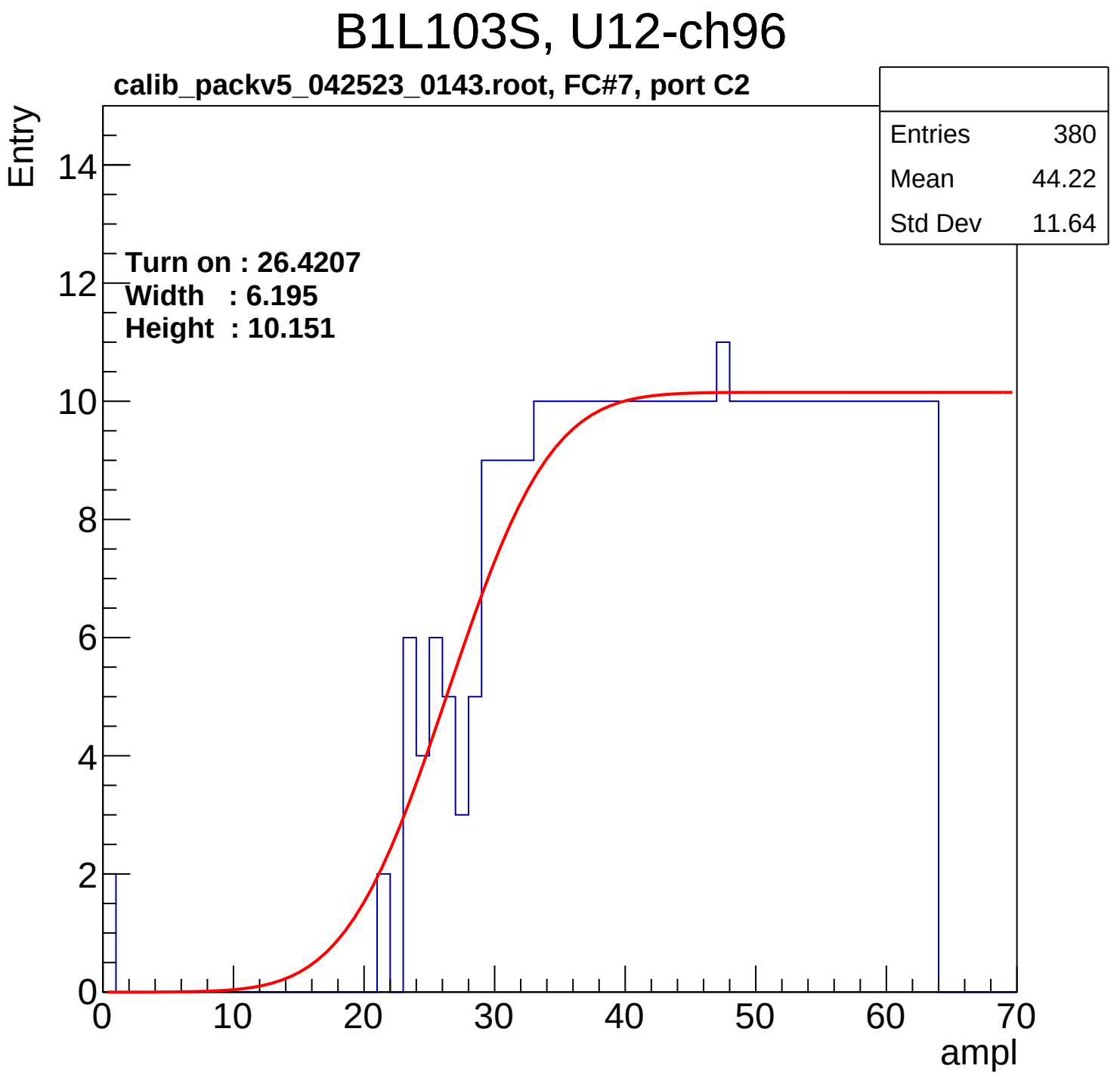

B1L103S, U12-ch91
calib_packv5_042523_0143.root, FC#7, port C2
Entries 361
Mean 45.15
Std Dev 11.11
Turn on : 28.6907
Width : 3.029
Height : 10.031
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

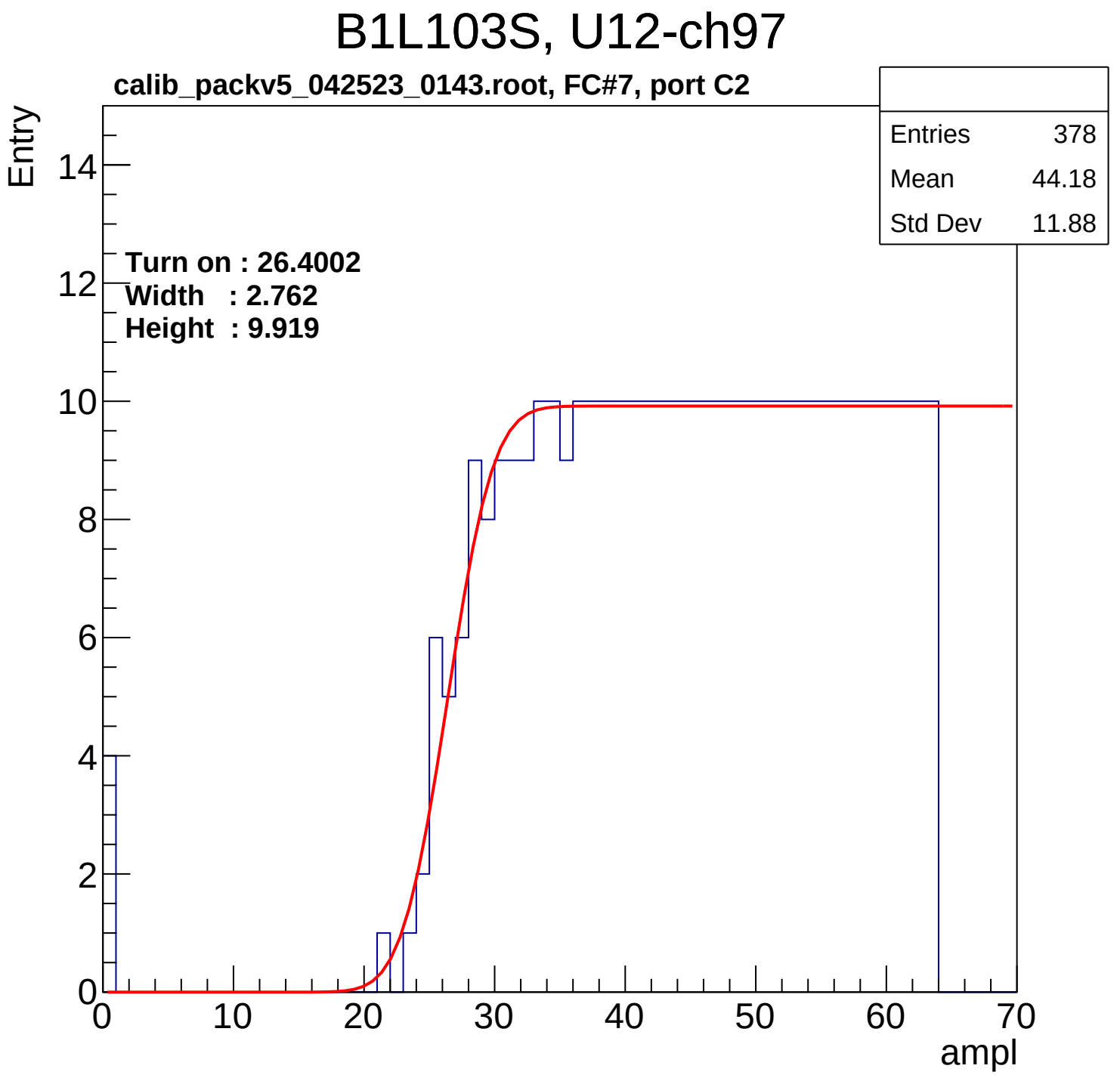

B1L103S, U12-ch92
calib_packv5_042523_0143.root, FC#7, port C2
Entries 400
Mean 43.34
Std Dev 11.86
Turn on : 25.2826
Width : 4.068
Height : 10.088
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

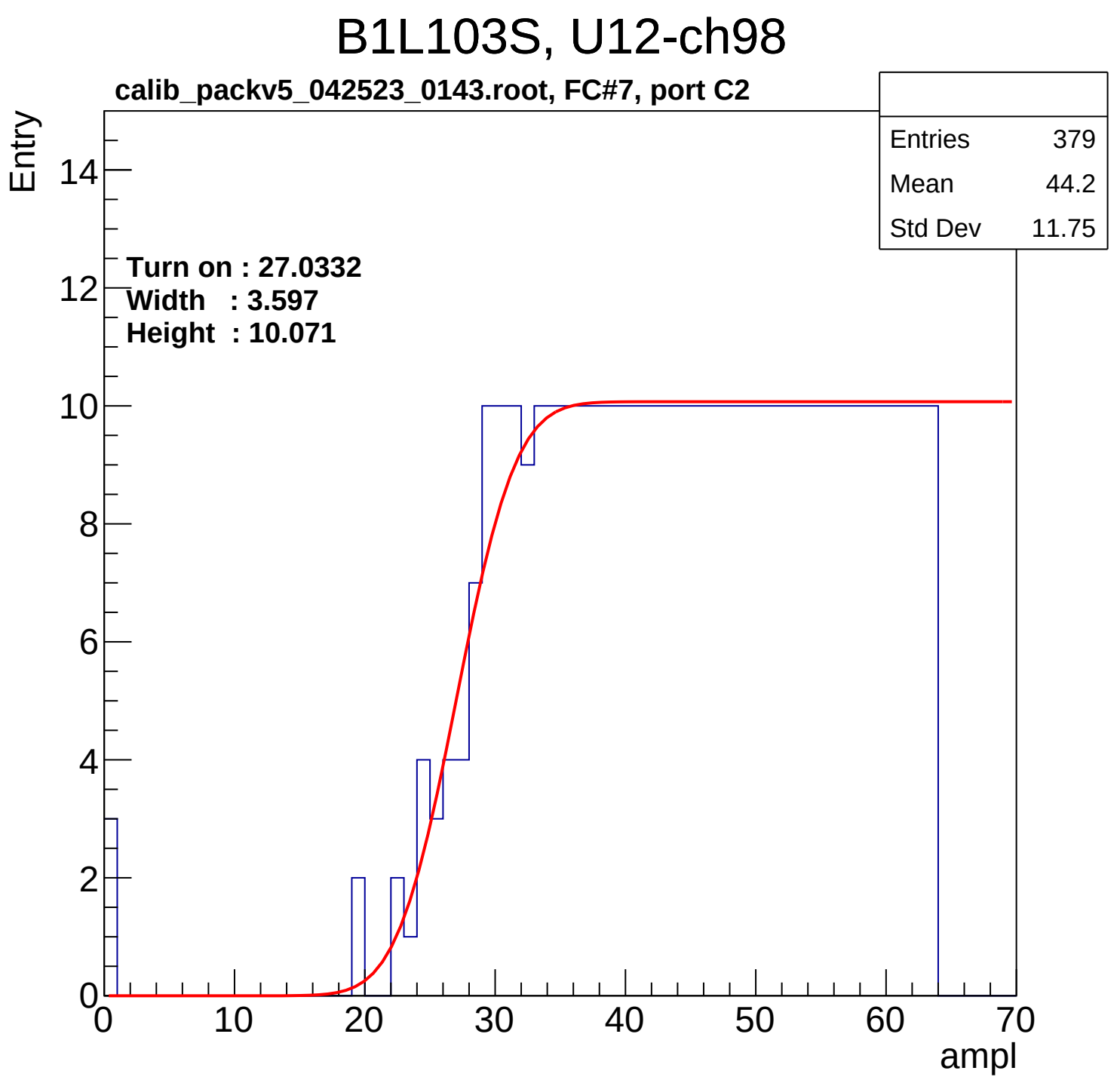

B1L103S, U12-ch93
calib_packv5_042523_0143.root, FC#7, port C2
Entries 384
Mean 44.01
Std Dev 11.71
Turn on : 26.3233
Width : 3.447
Height : 10.027
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

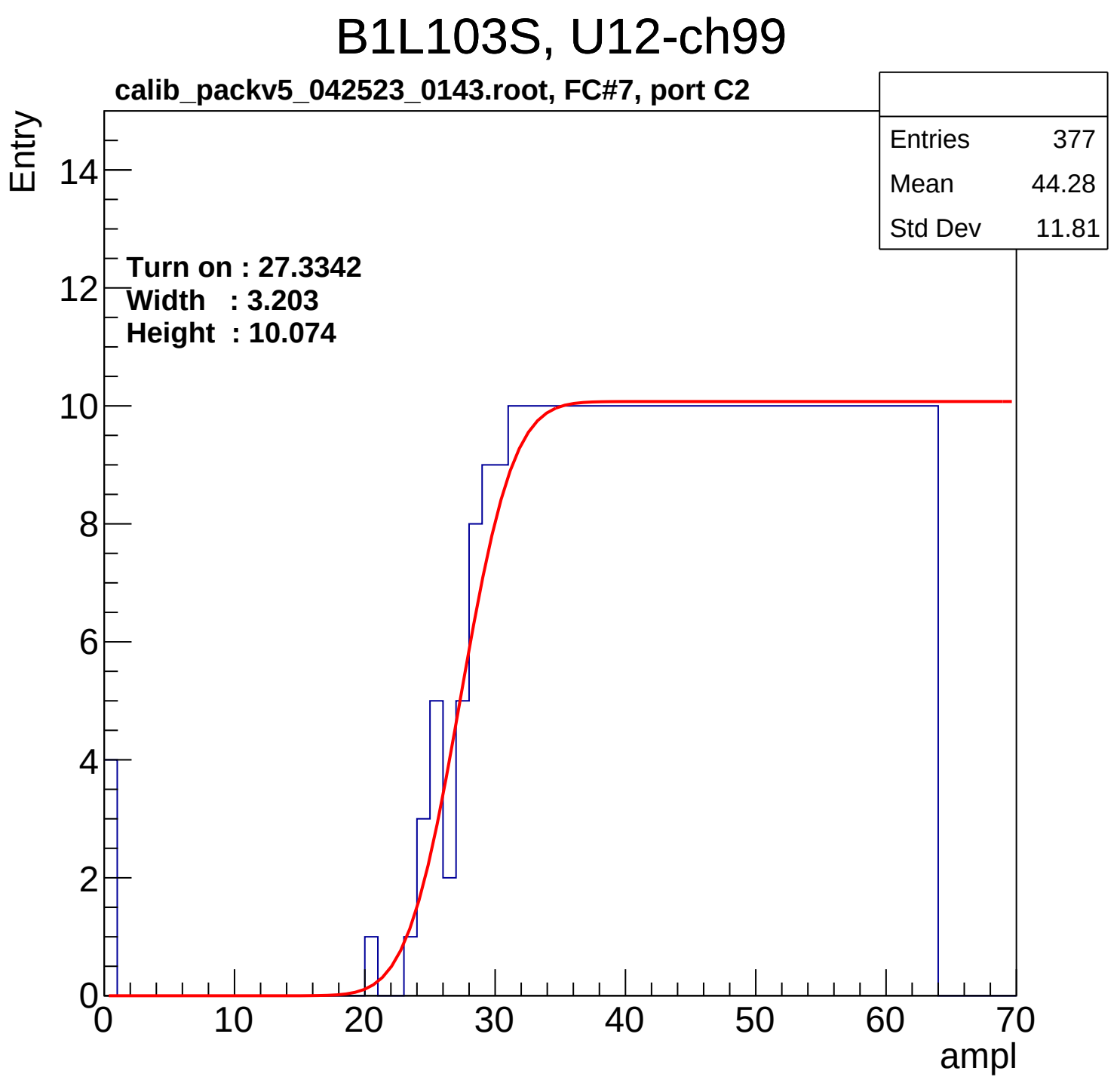

B1L103S, U12-ch94
calib_packv5_042523_0143.root, FC#7, port C2
Entries 389
Mean 43.8
Std Dev 11.79
Turn on : 26.6008
Width : 4.104
Height : 10.114
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

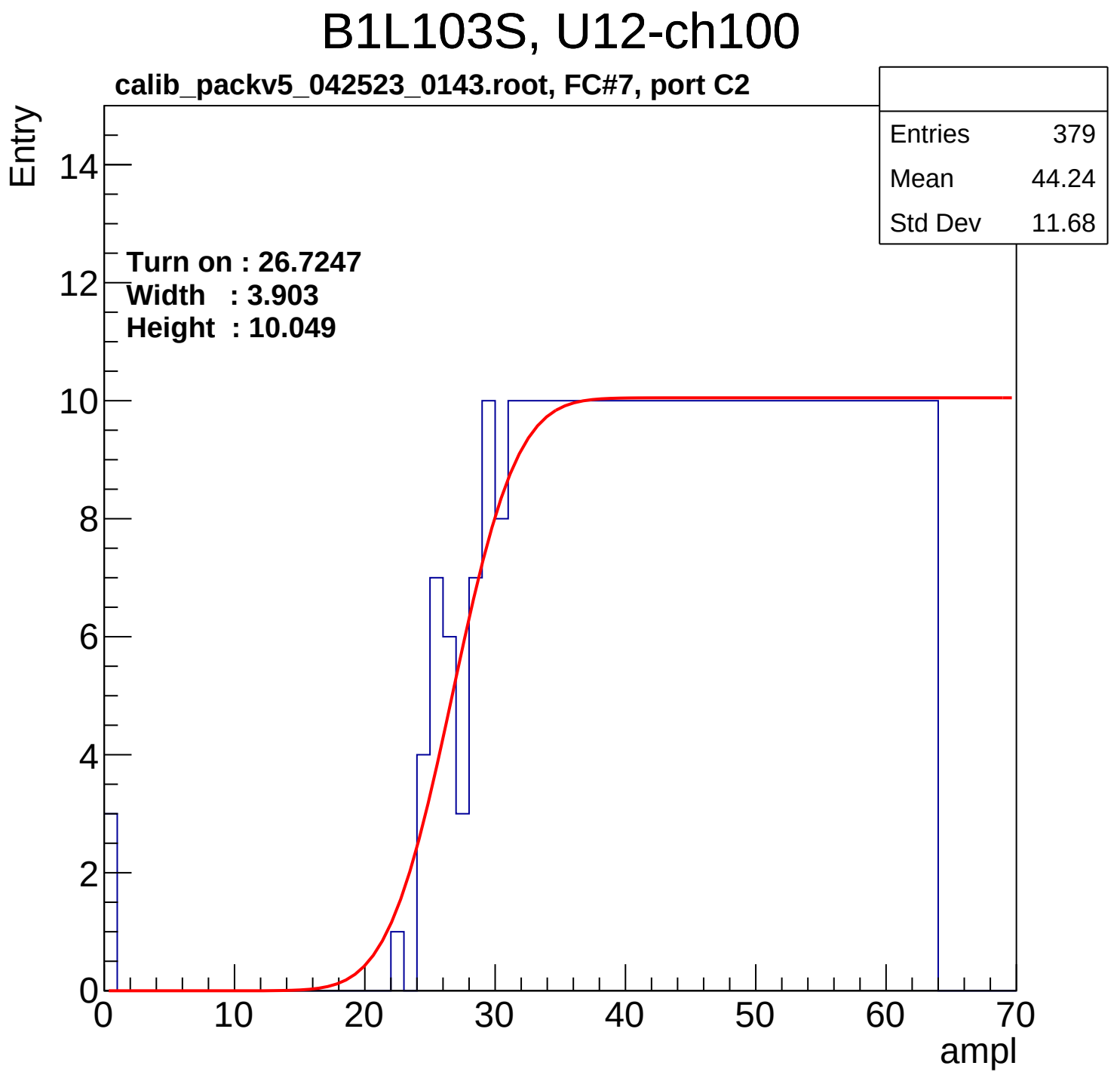

B1L103S, U12-ch95
calib_packv5_042523_0143.root, FC#7, port C2
Entries 381
Mean 44.13
Std Dev 11.83
Turn on : 26.5879
Width : 2.332
Height : 10.029
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

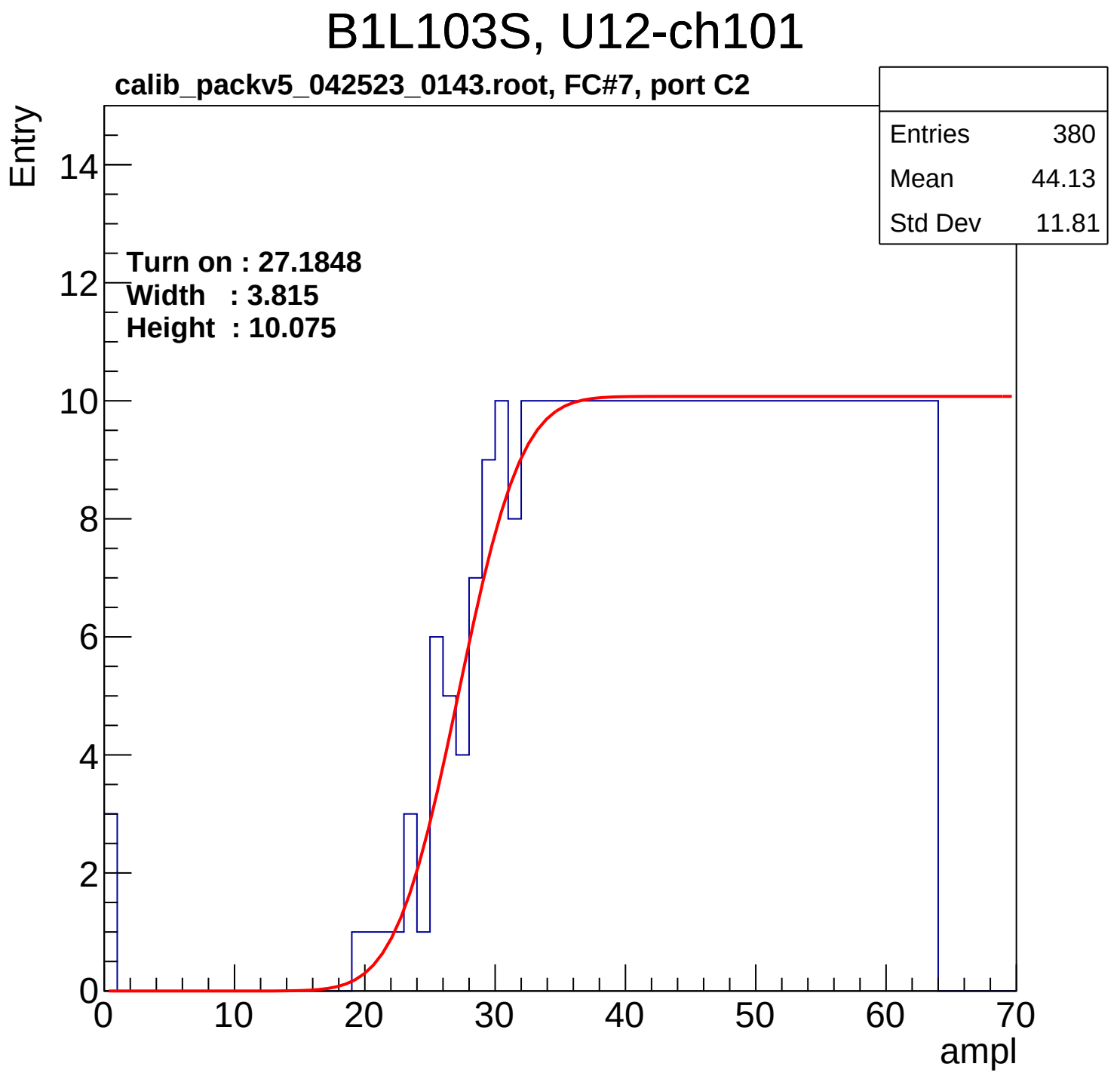

B1L103S, U12-ch96
calib_packv5_042523_0143.root, FC#7, port C2
Entries 380
Mean 44.22
Std Dev 11.64
Turn on : 26.4207
Width : 6.195
Height : 10.151
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

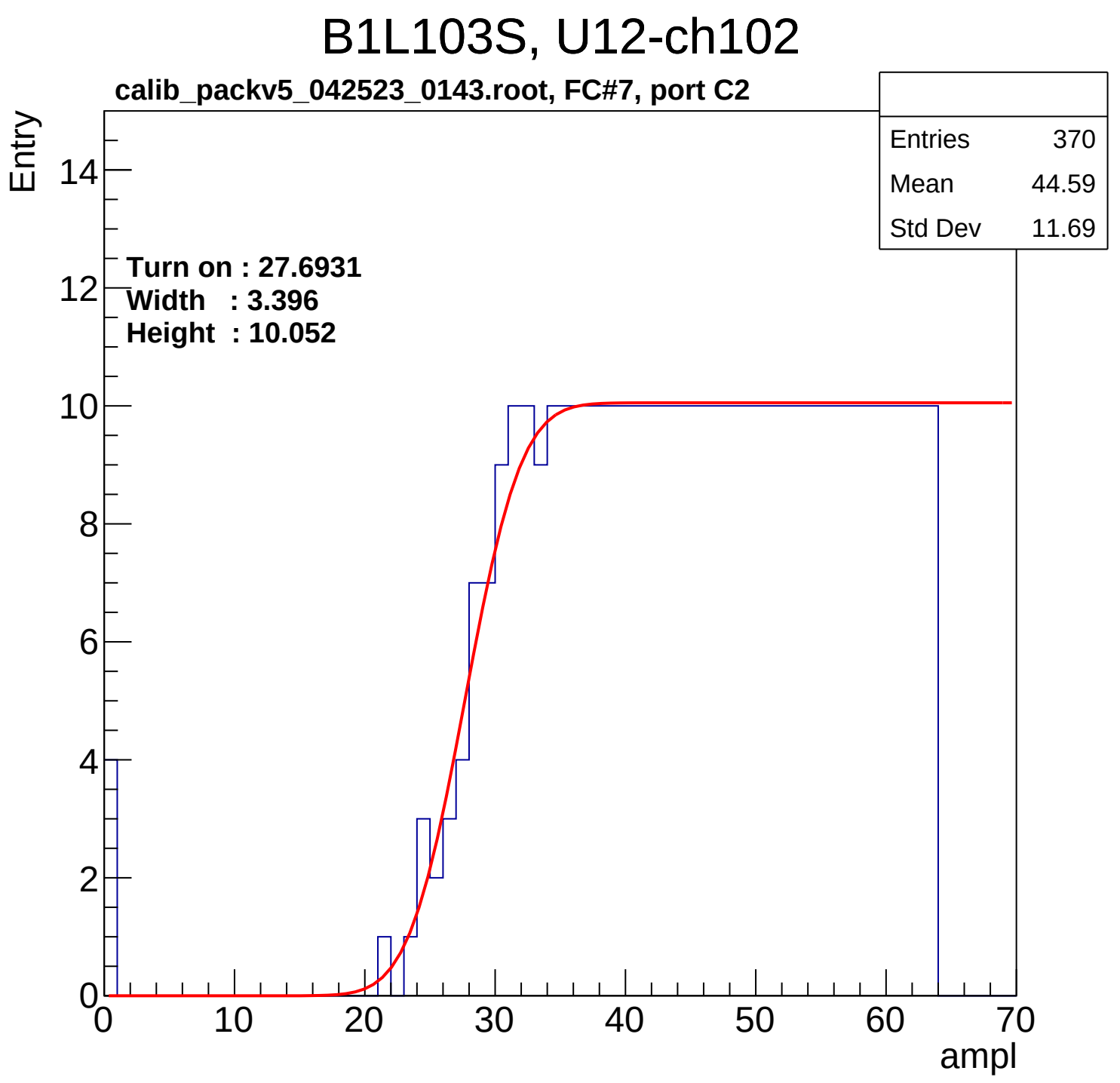

B1L103S, U12-ch97
calib_packv5_042523_0143.root, FC#7, port C2
Entries 378
Mean 44.18
Std Dev 11.88
Turn on : 26.4002
Width : 2.762
Height : 9.919
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

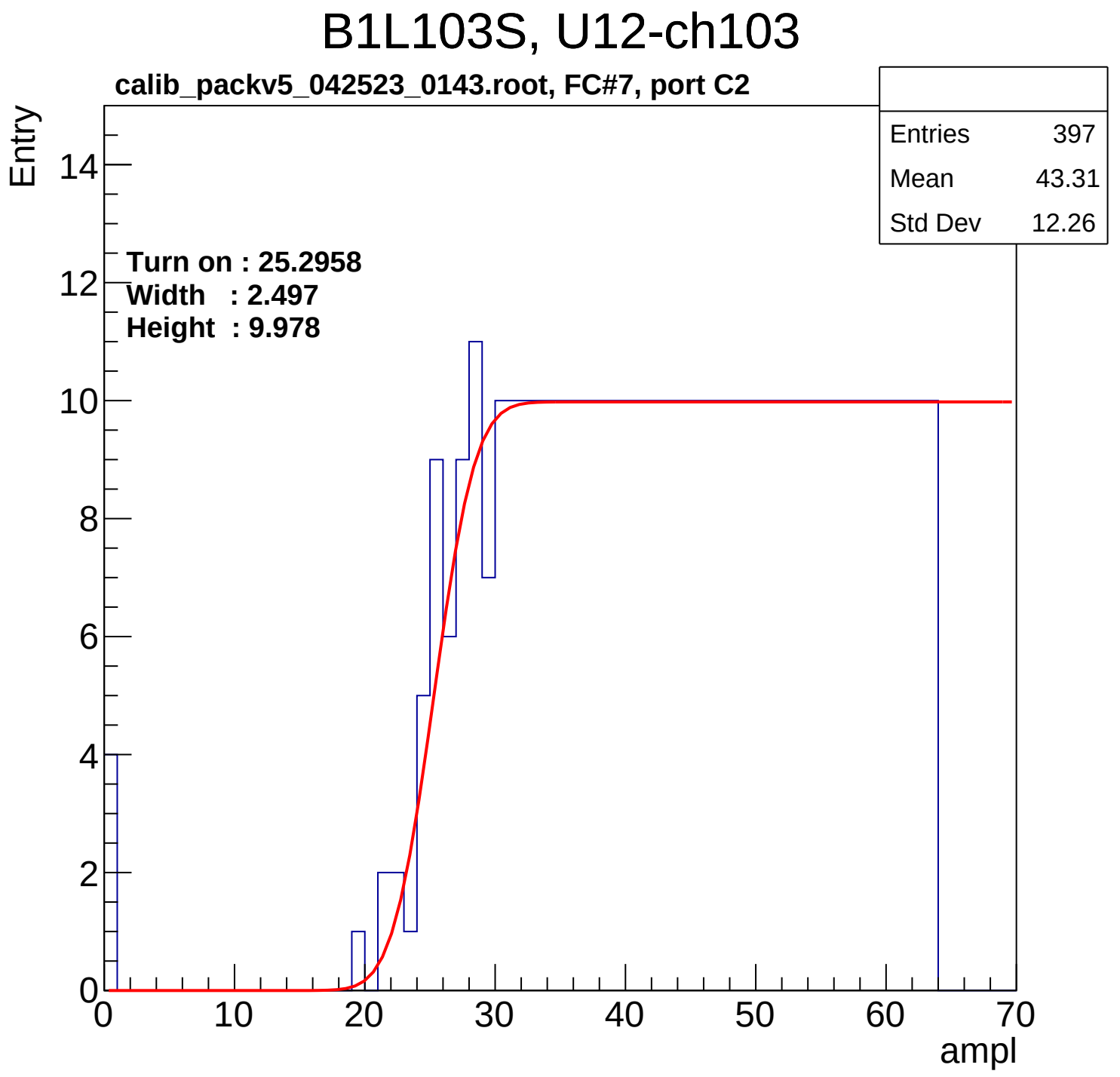

B1L103S, U12-ch98
calib_packv5_042523_0143.root, FC#7, port C2
Entries 379
Mean 44.2
Std Dev 11.75
Turn on : 27.0332
Width : 3.597
Height : 10.071
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

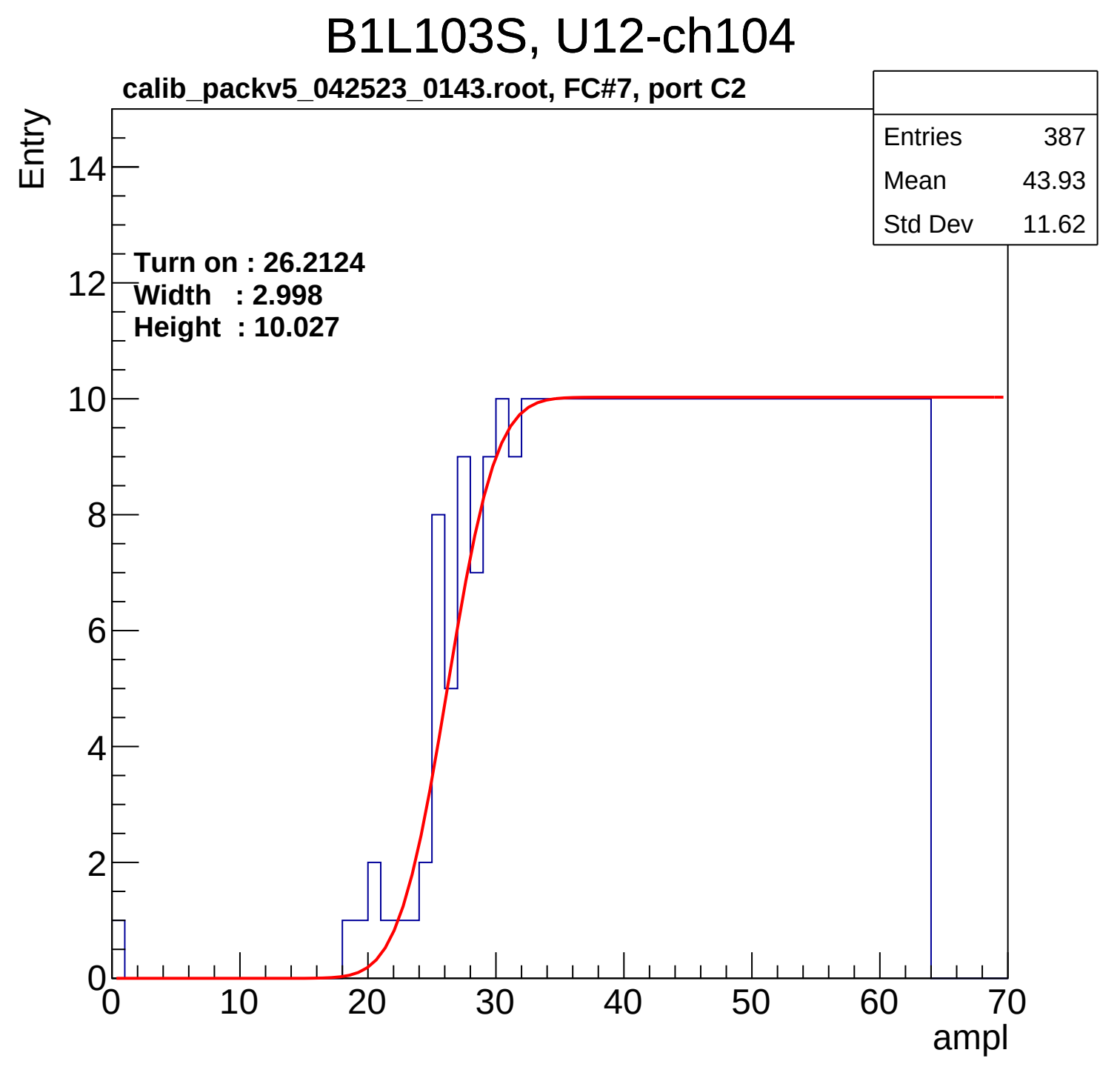

B1L103S, U12-ch99
calib_packv5_042523_0143.root, FC#7, port C2
Entries 377
Mean 44.28
Std Dev 11.81
Turn on : 27.3342
Width : 3.203
Height : 10.074
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

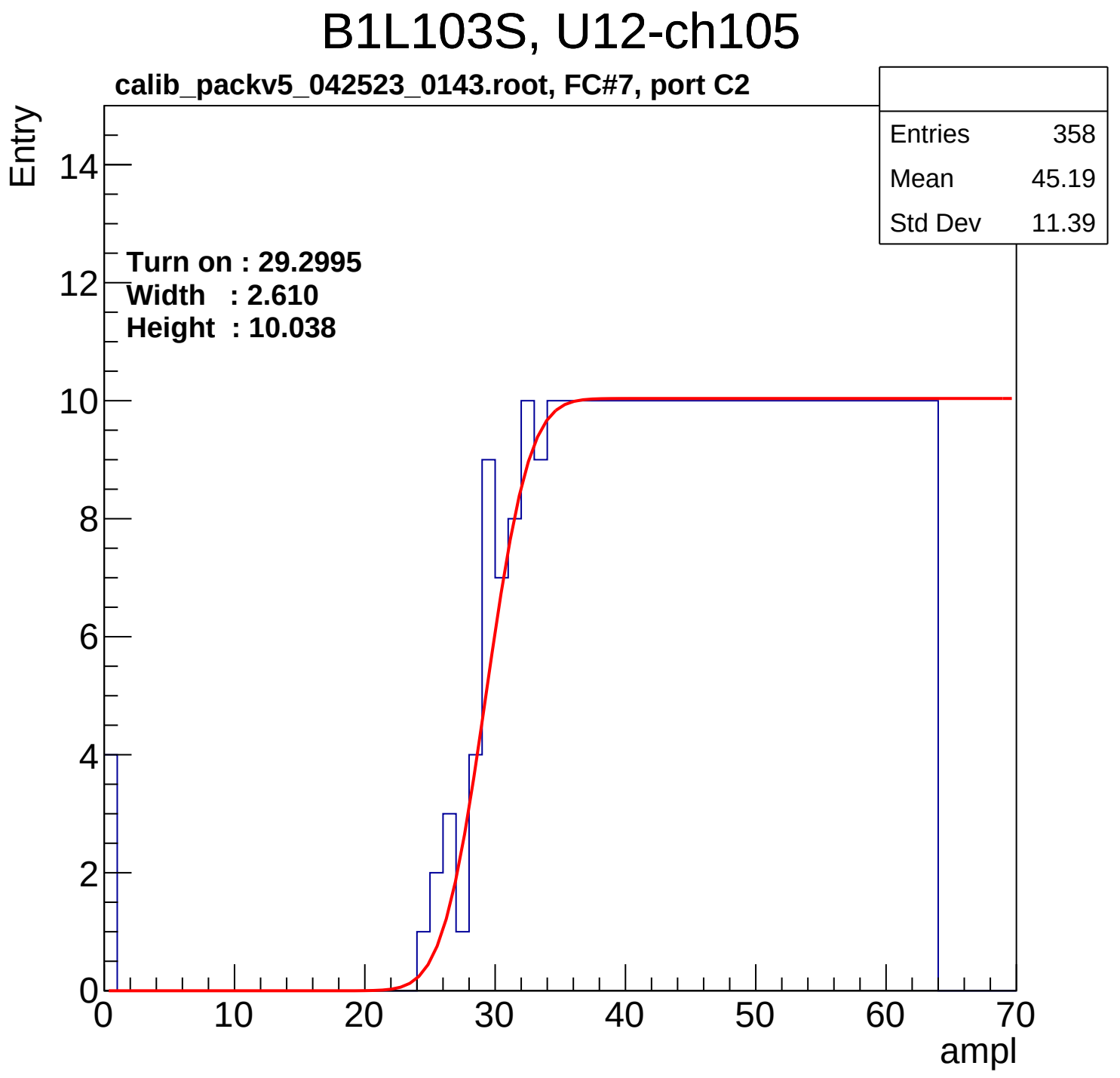

B1L103S, U12-ch100
calib_packv5_042523_0143.root, FC#7, port C2
Entries 379
Mean 44.24
Std Dev 11.68
Turn on : 26.7247
Width : 3.903
Height : 10.049
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

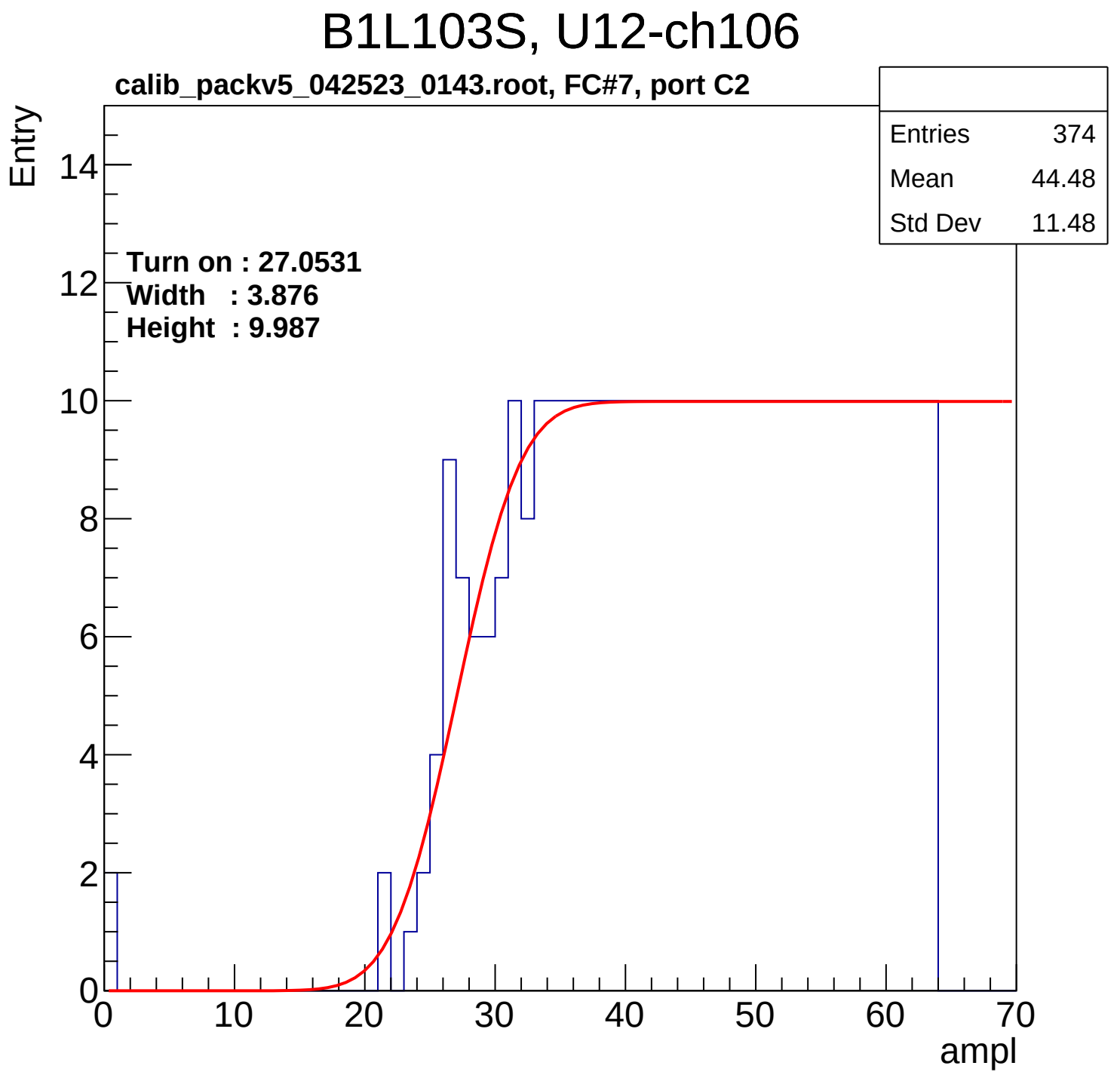

B1L103S, U12-ch101
calib_packv5_042523_0143.root, FC#7, port C2
Entries 380
Mean 44.13
Std Dev 11.81
Turn on : 27.1848
Width : 3.815
Height : 10.075
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

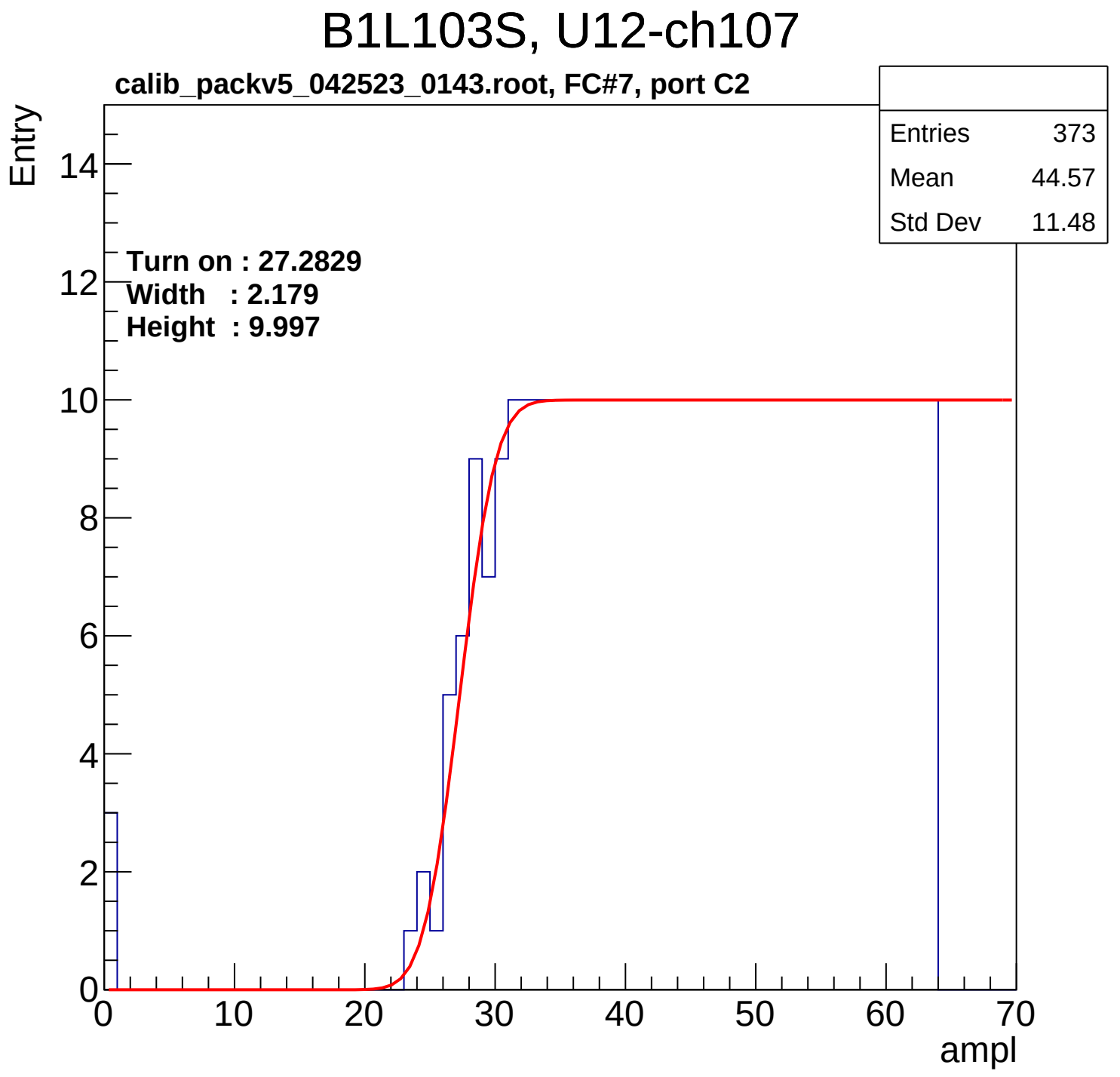

B1L103S, U12-ch102
calib_packv5_042523_0143.root, FC#7, port C2
Entries 370
Mean 44.59
Std Dev 11.69
Turn on : 27.6931
Width : 3.396
Height : 10.052
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

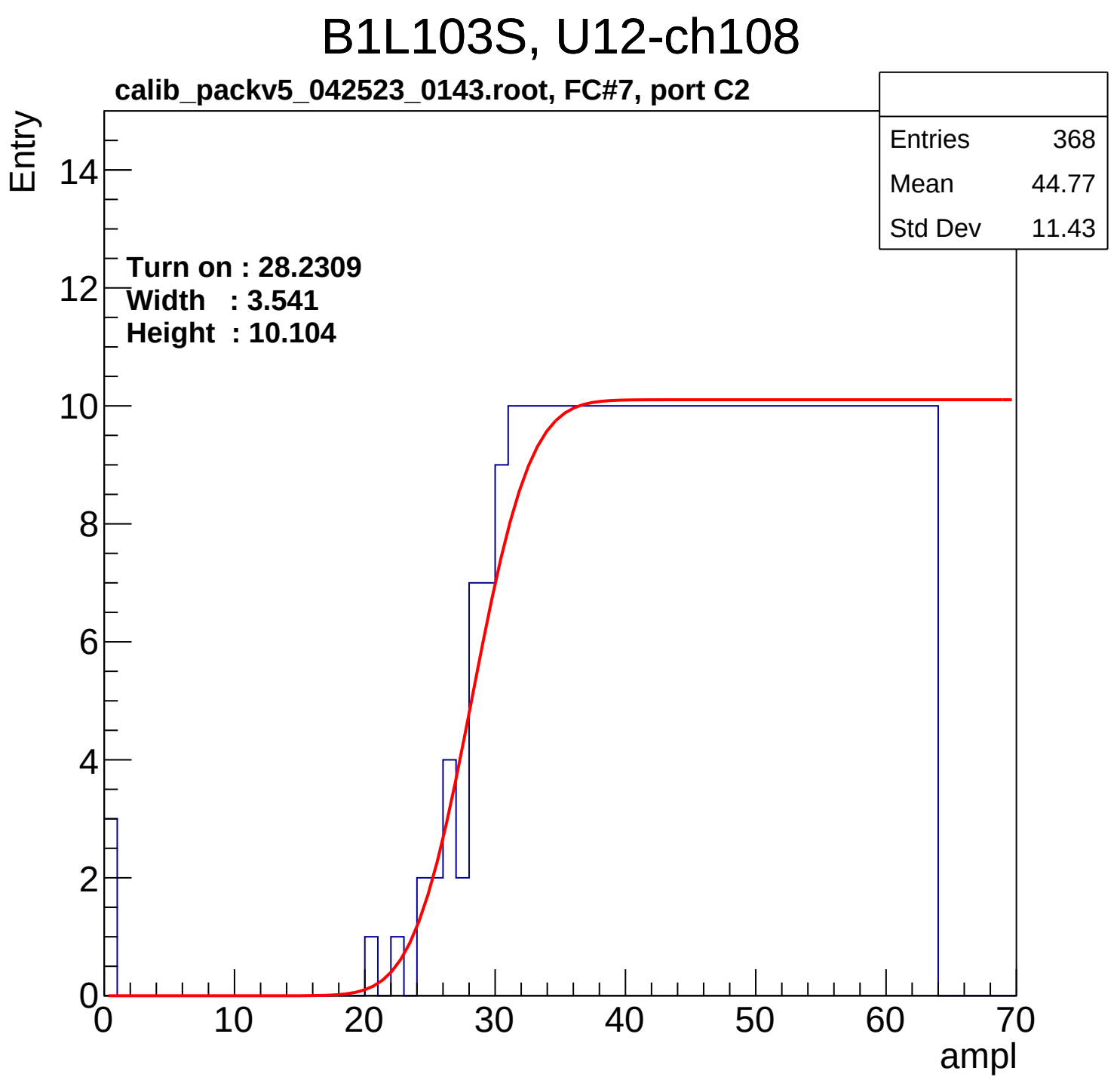

B1L103S, U12-ch103
calib_packv5_042523_0143.root, FC#7, port C2
Entries 397
Mean 43.31
Std Dev 12.26
Turn on : 25.2958
Width : 2.497
Height : 9.978
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

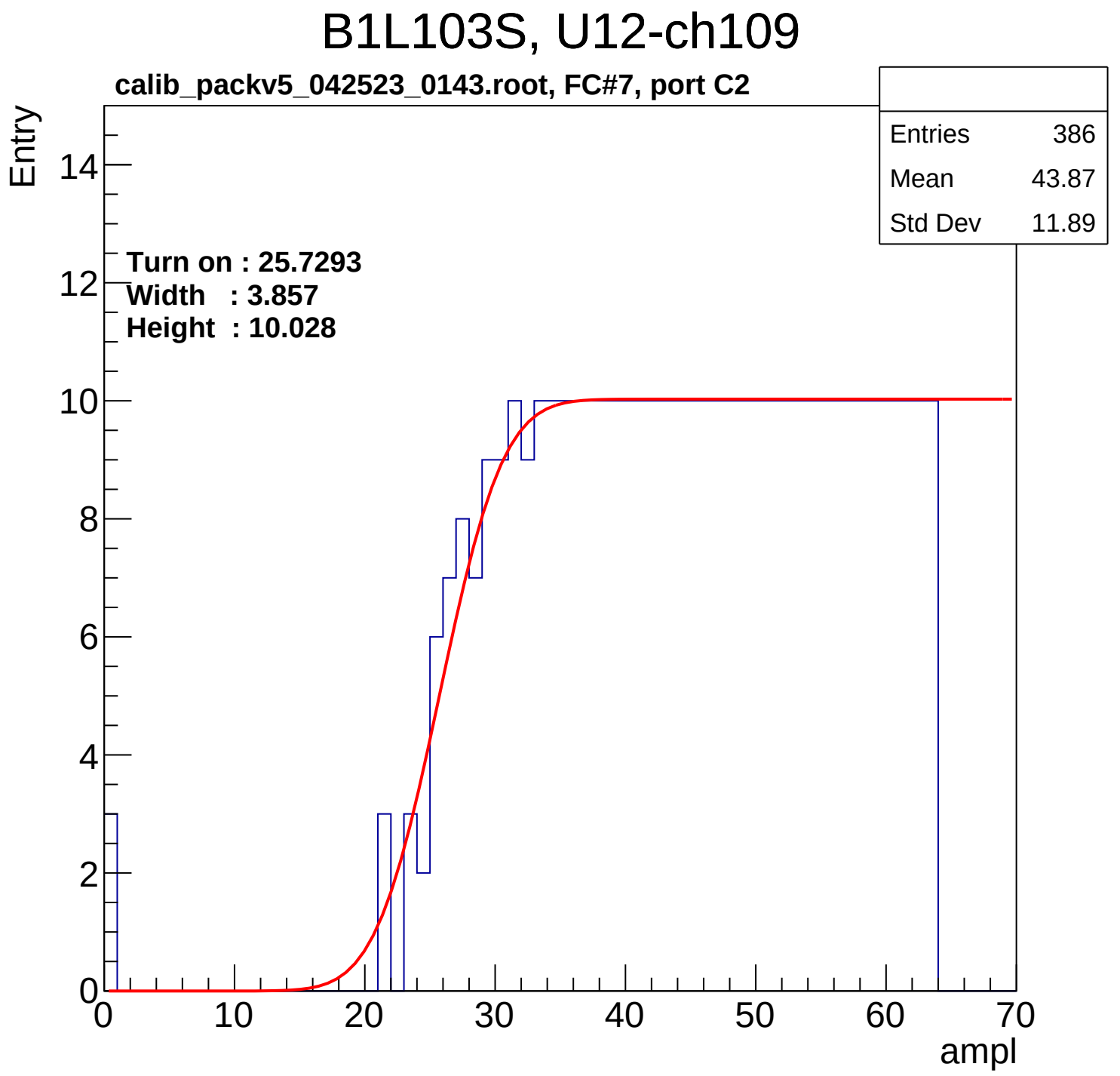

B1L103S, U12-ch104
calib_packv5_042523_0143.root, FC#7, port C2
Entries 387
Mean 43.93
Std Dev 11.62
Turn on : 26.2124
Width : 2.998
Height : 10.027
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

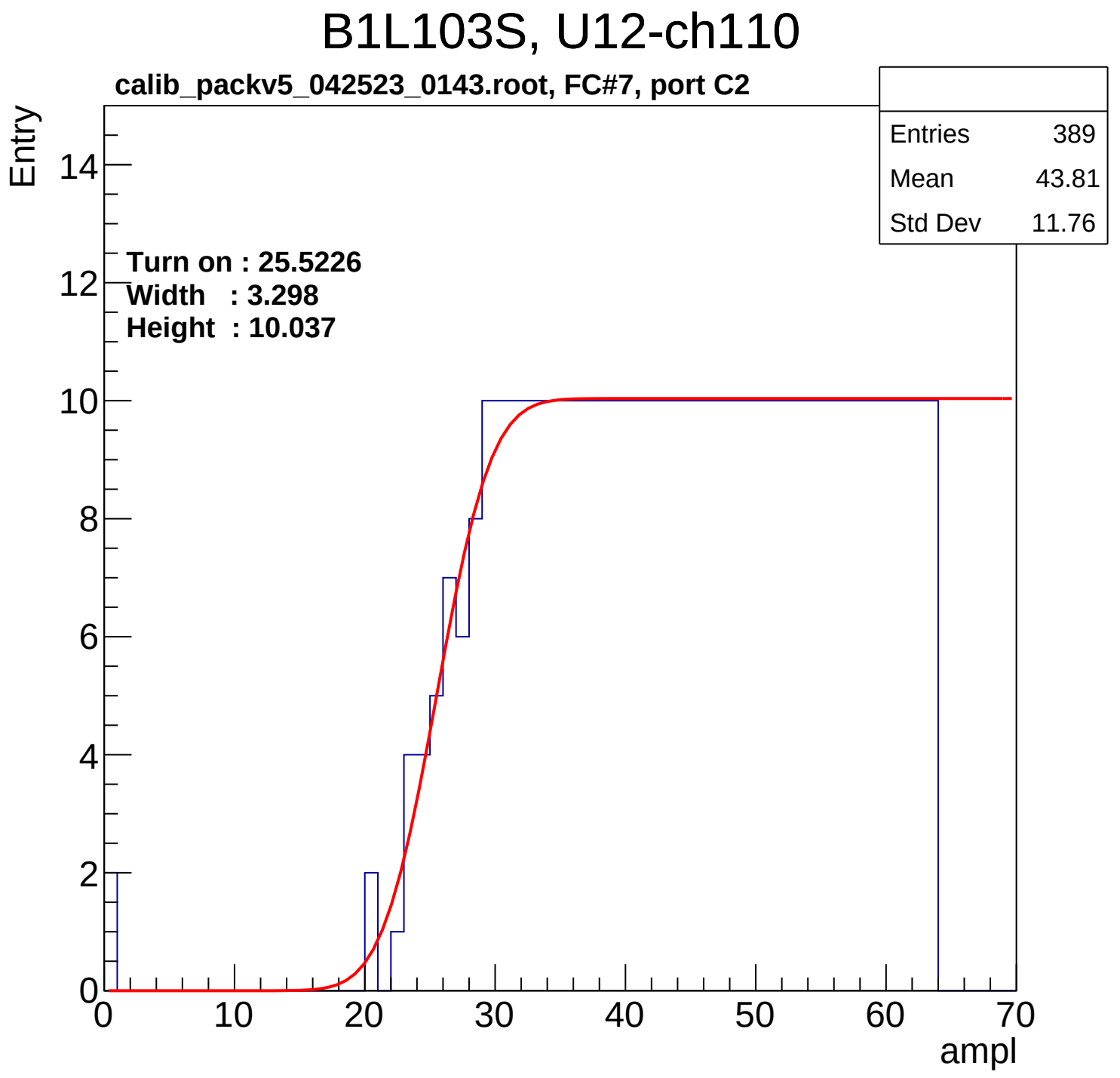

B1L103S, U12-ch105
calib_packv5_042523_0143.root, FC#7, port C2
Entries 358
Mean 45.19
Std Dev 11.39
Turn on : 29.2995
Width : 2.610
Height : 10.038
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

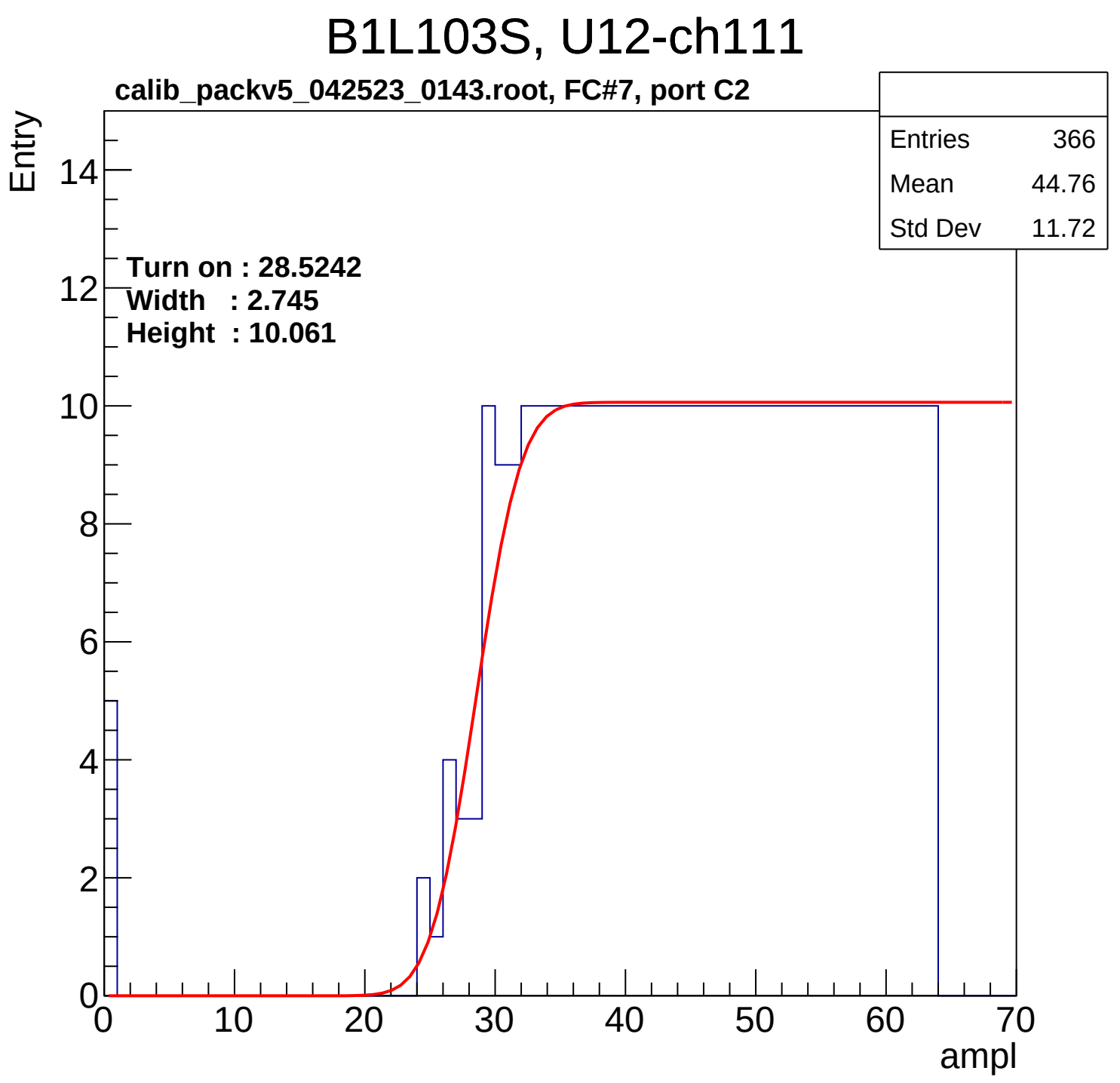

B1L103S, U12-ch106
calib_packv5_042523_0143.root, FC#7, port C2
Entries 374
Mean 44.48
Std Dev 11.48
Turn on : 27.0531
Width : 3.876
Height : 9.987
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

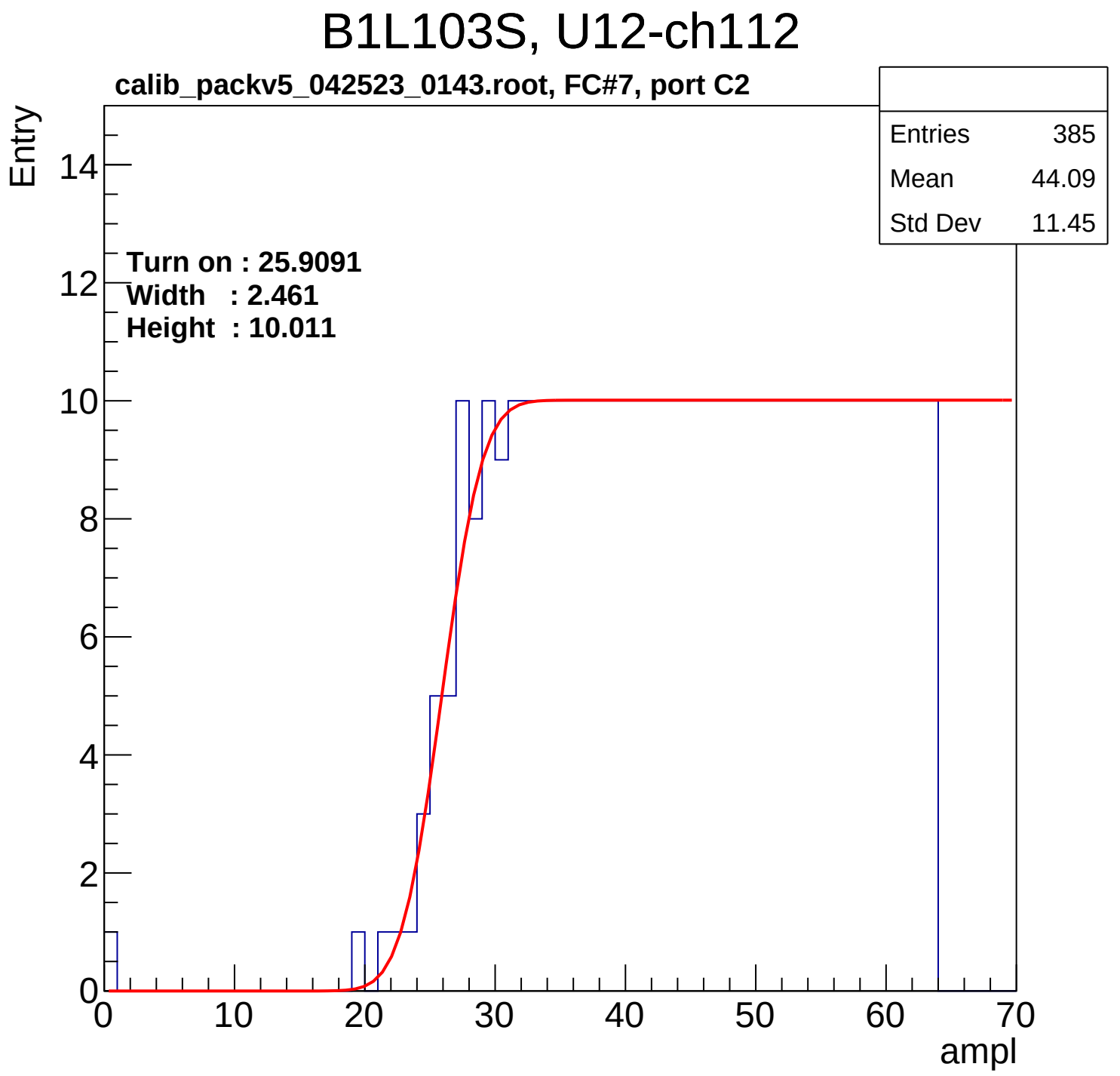

B1L103S, U12-ch107
calib_packv5_042523_0143.root, FC#7, port C2
Entries 373
Mean 44.57
Std Dev 11.48
Turn on : 27.2829
Width : 2.179
Height : 9.997
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

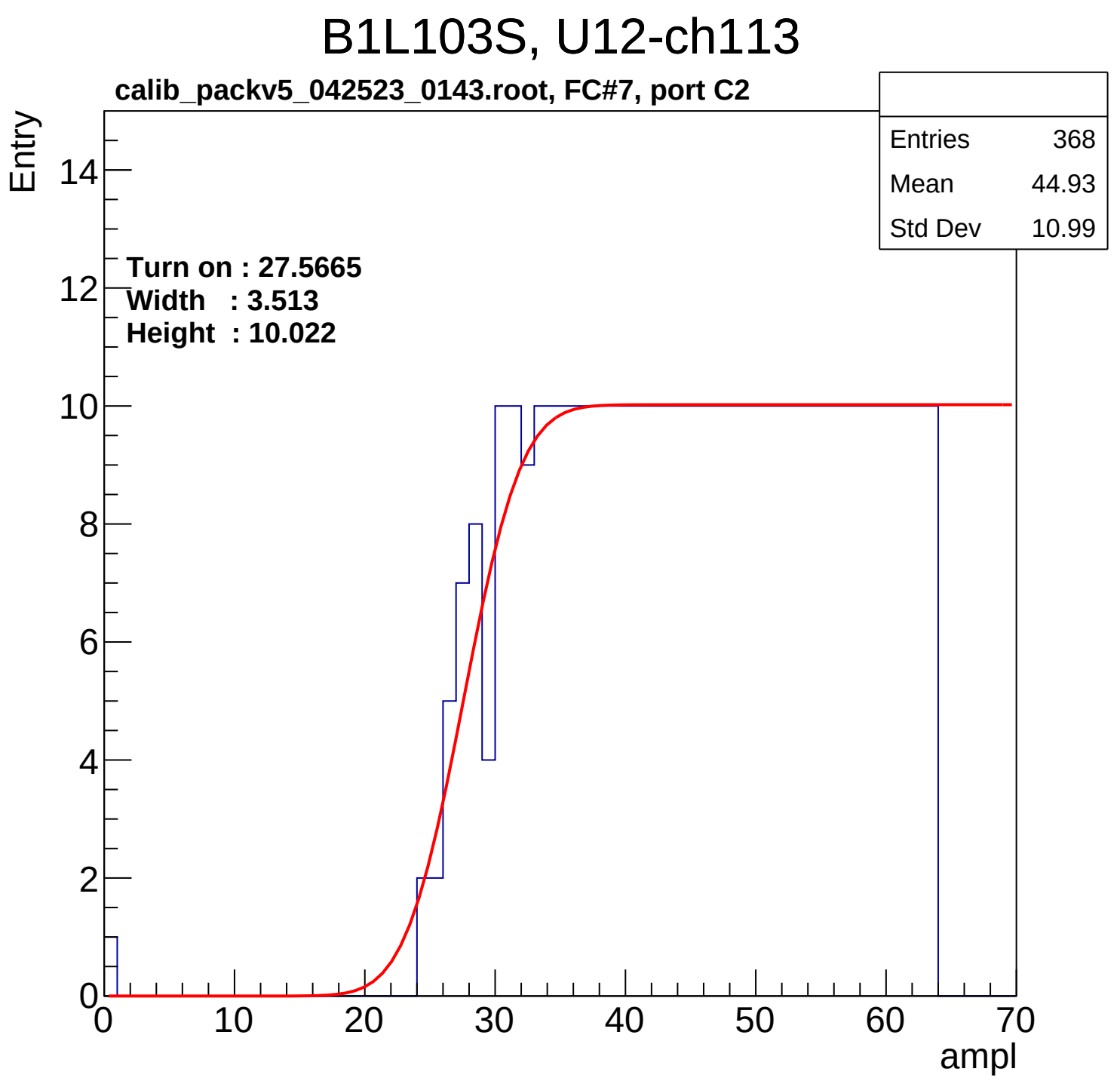

B1L103S, U12-ch108
calib_packv5_042523_0143.root, FC#7, port C2
Entries 368
Mean 44.77
Std Dev 11.43
Turn on : 28.2309
Width : 3.541
Height : 10.104
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

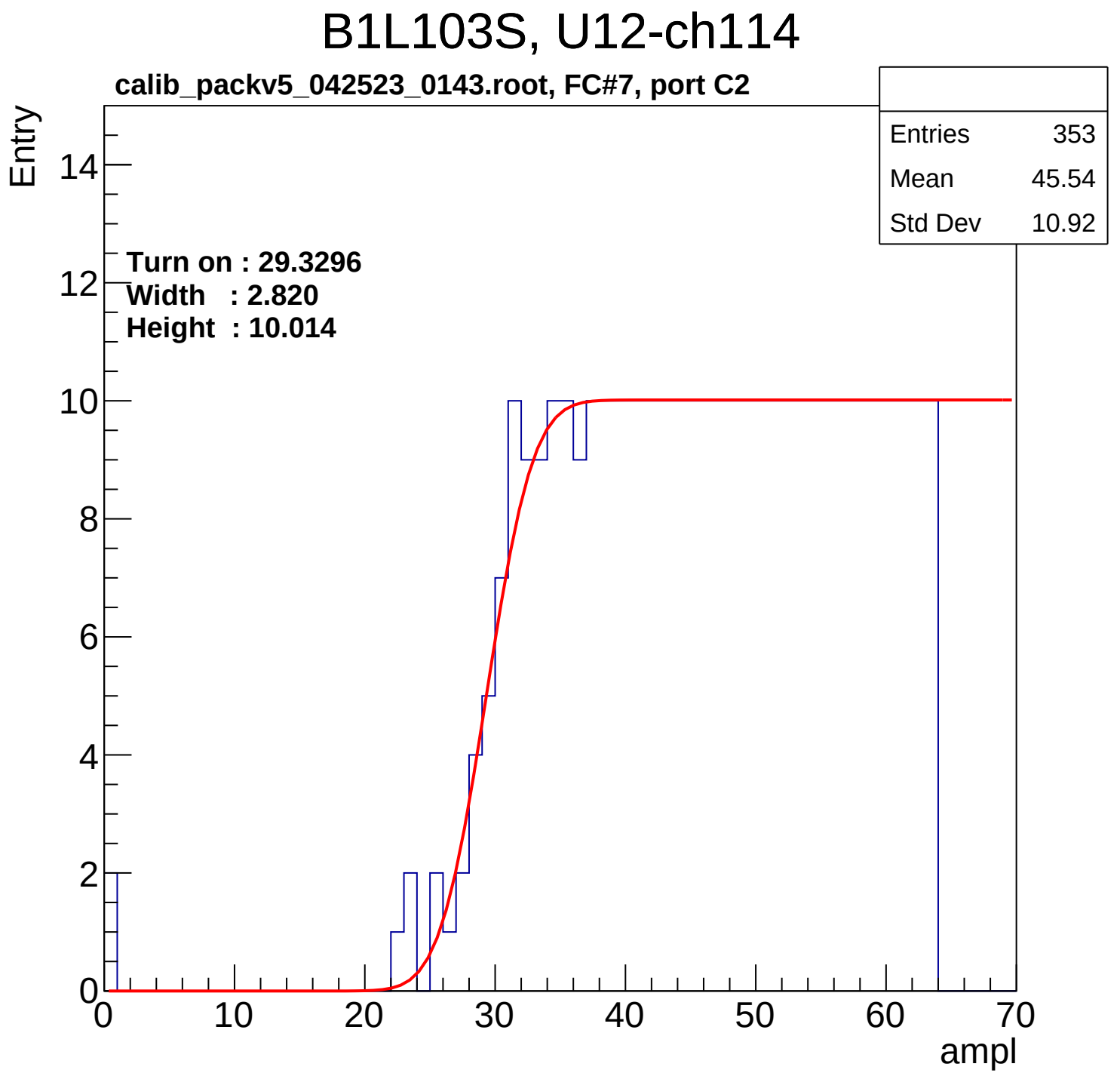

B1L103S, U12-ch109
calib_packv5_042523_0143.root, FC#7, port C2
Entries 386
Mean 43.87
Std Dev 11.89
Turn on : 25.7293
Width : 3.857
Height : 10.028
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

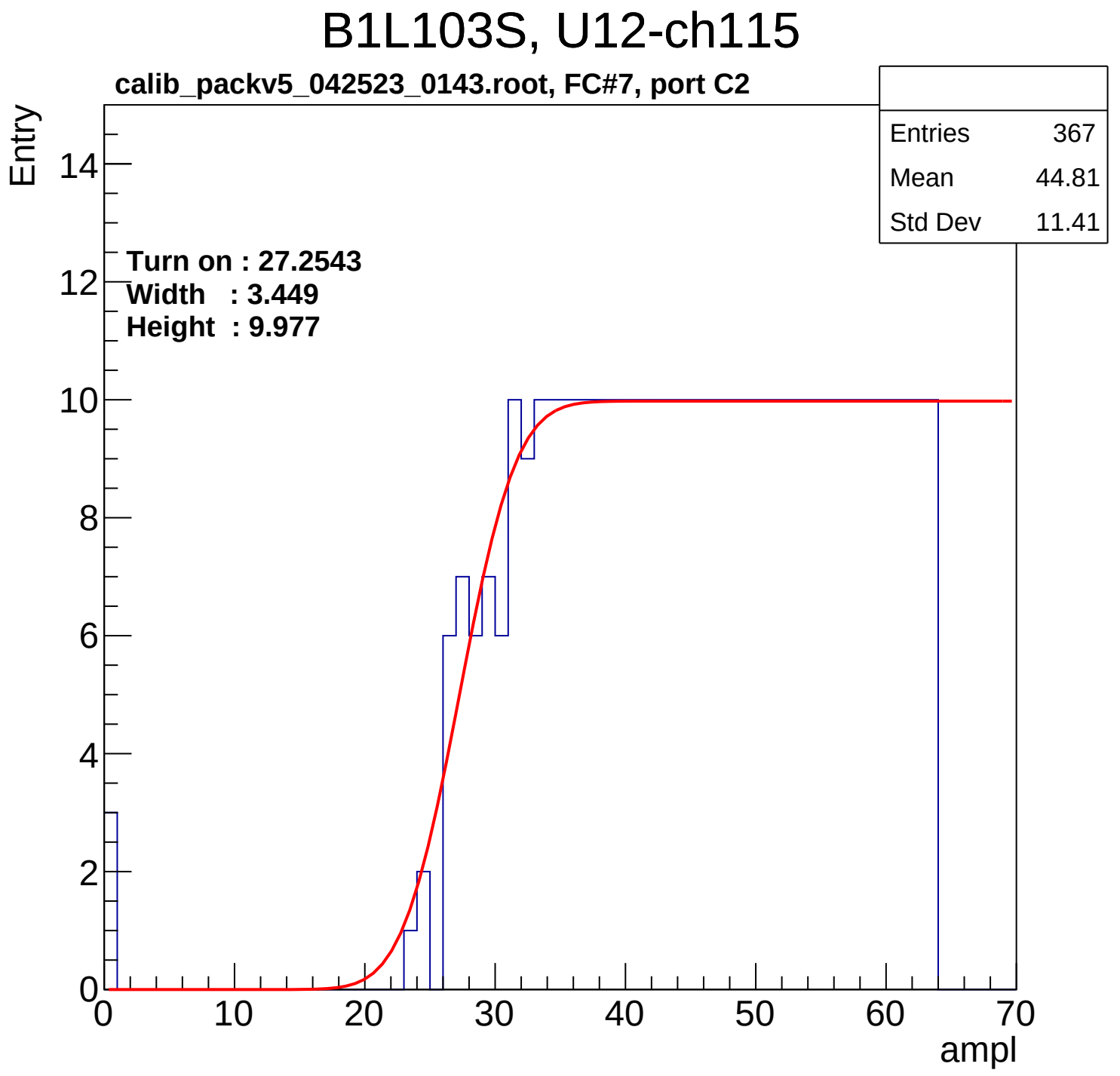

B1L103S, U12-ch110
calib_packv5_042523_0143.root, FC#7, port C2
Entries 389
Mean 43.81
Std Dev 11.76
Turn on : 25.5226
Width : 3.298
Height : 10.037
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

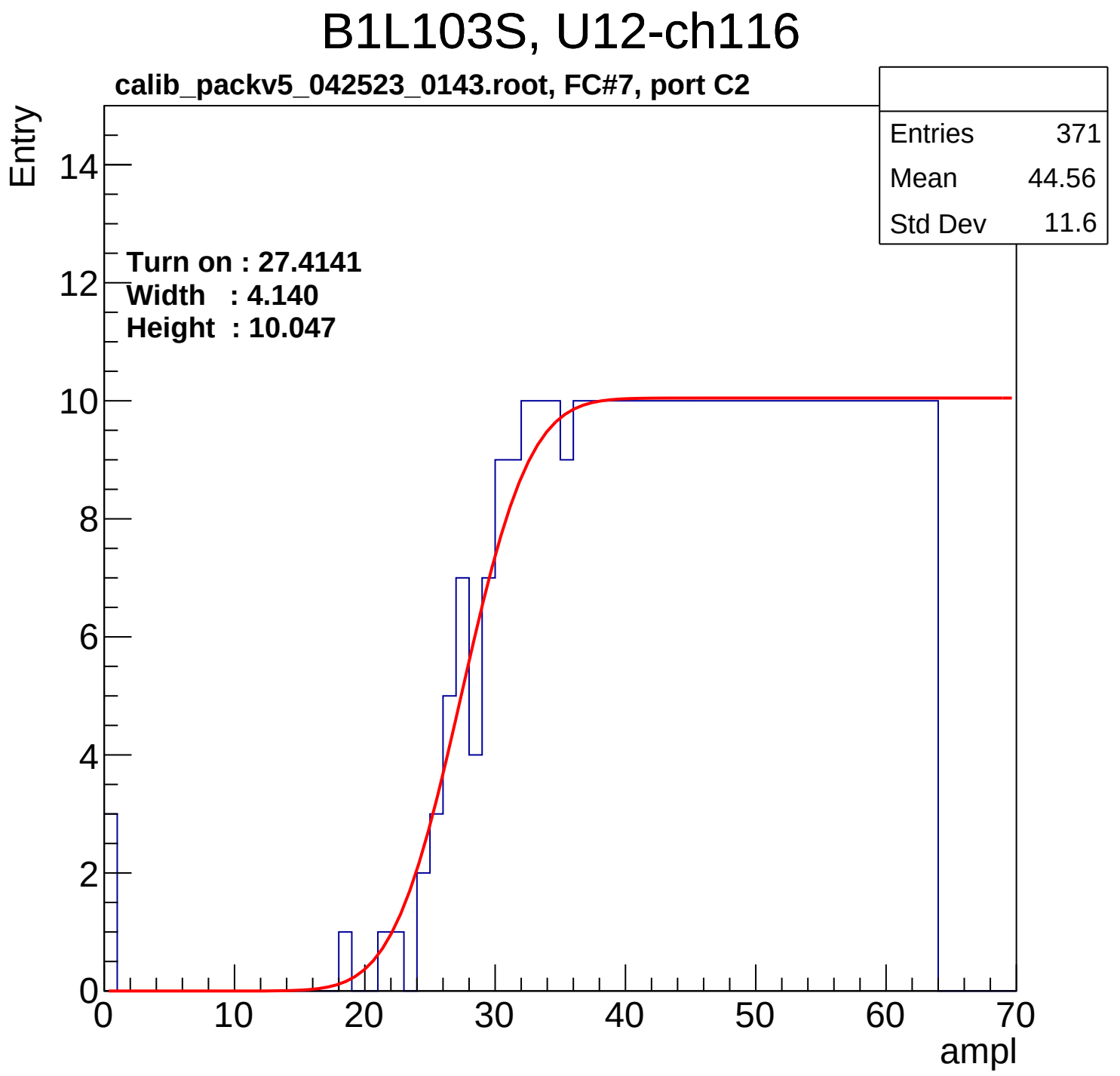

B1L103S, U12-ch111
calib_packv5_042523_0143.root, FC#7, port C2
Entries 366
Mean 44.76
Std Dev 11.72
Turn on : 28.5242
Width : 2.745
Height : 10.061
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

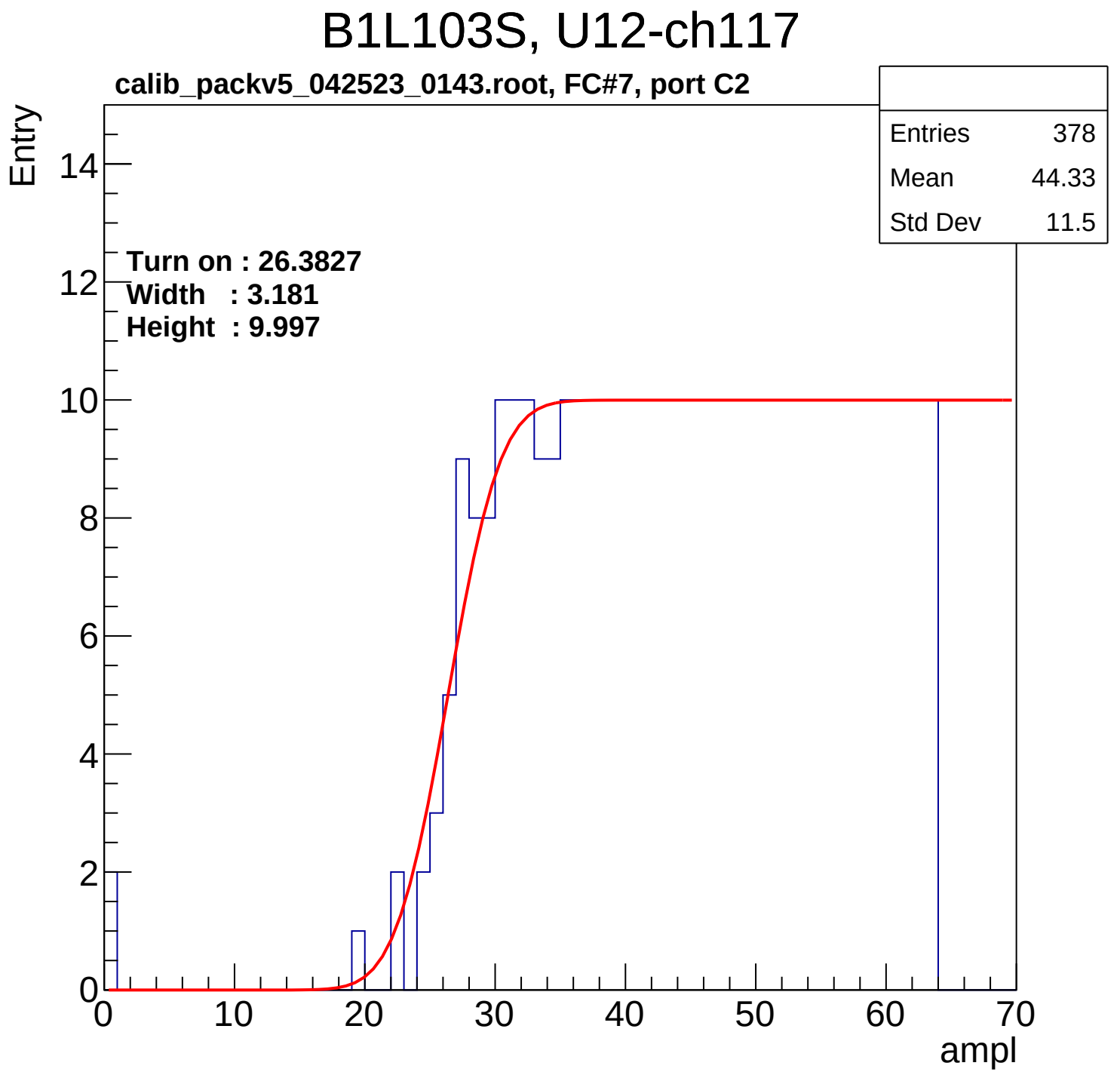

B1L103S, U12-ch112
calib_packv5_042523_0143.root, FC#7, port C2
Entries 385
Mean 44.09
Std Dev 11.45
Turn on : 25.9091
Width : 2.461
Height : 10.011
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

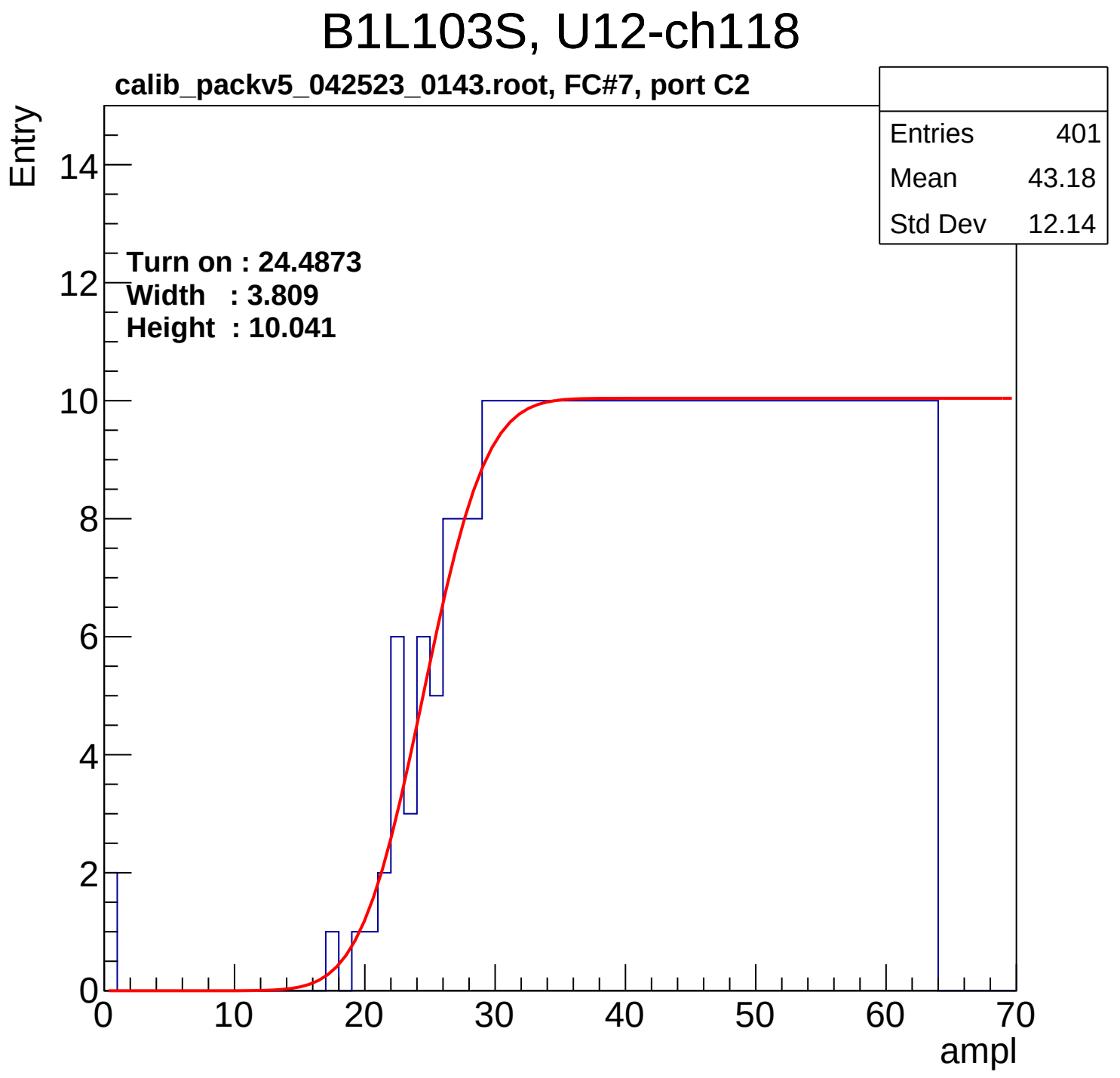

B1L103S, U12-ch113
calib_packv5_042523_0143.root, FC#7, port C2
Entries 368
Mean 44.93
Std Dev 10.99
Turn on : 27.5665
Width : 3.513
Height : 10.022
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

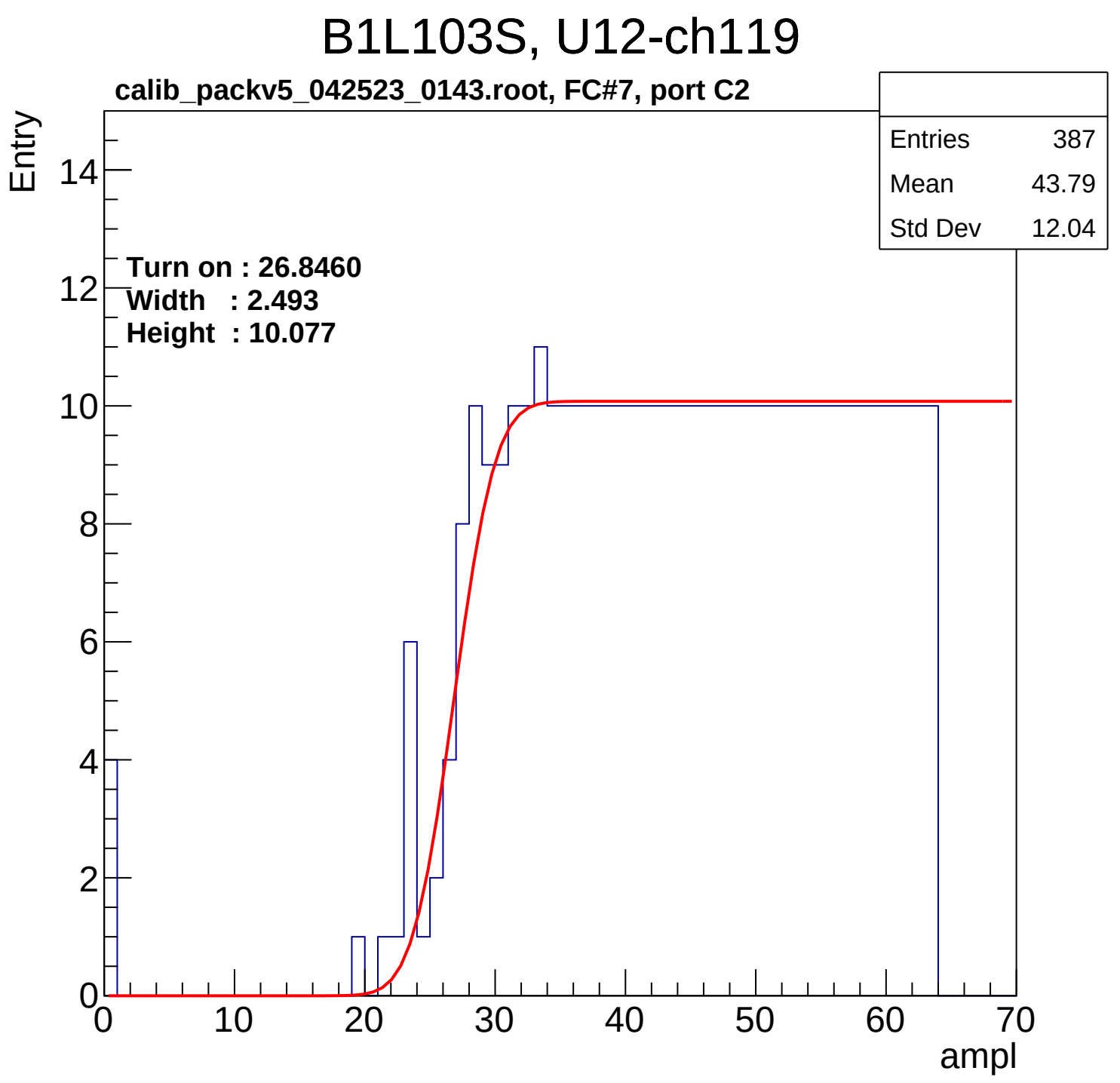

B1L103S, U12-ch114
calib_packv5_042523_0143.root, FC#7, port C2
Entries 353
Mean 45.54
Std Dev 10.92
Turn on : 29.3296
Width : 2.820
Height : 10.014
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

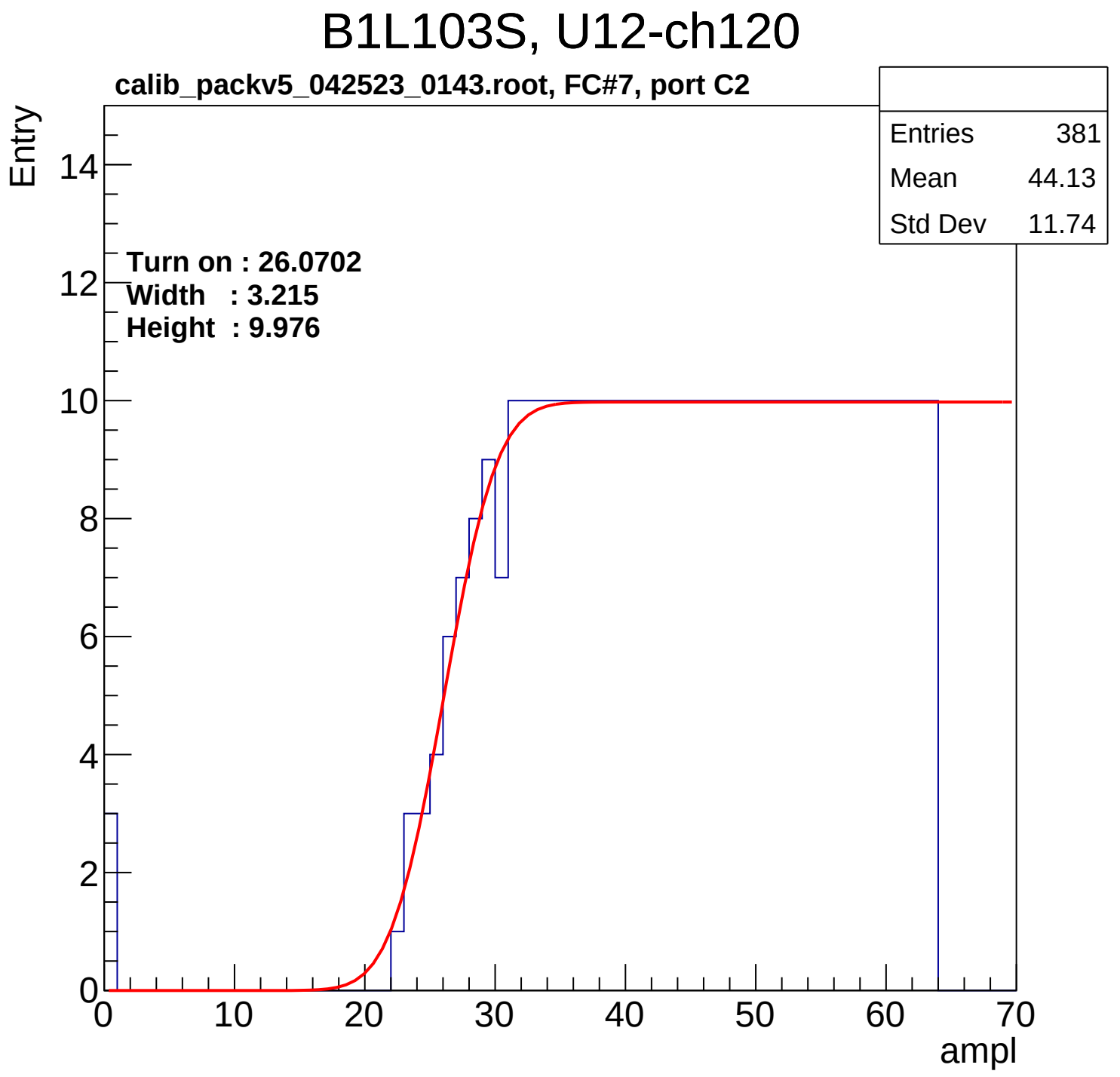

B1L103S, U12-ch115
calib_packv5_042523_0143.root, FC#7, port C2
Entries 367
Mean 44.81
Std Dev 11.41
Turn on : 27.2543
Width : 3.449
Height : 9.977
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

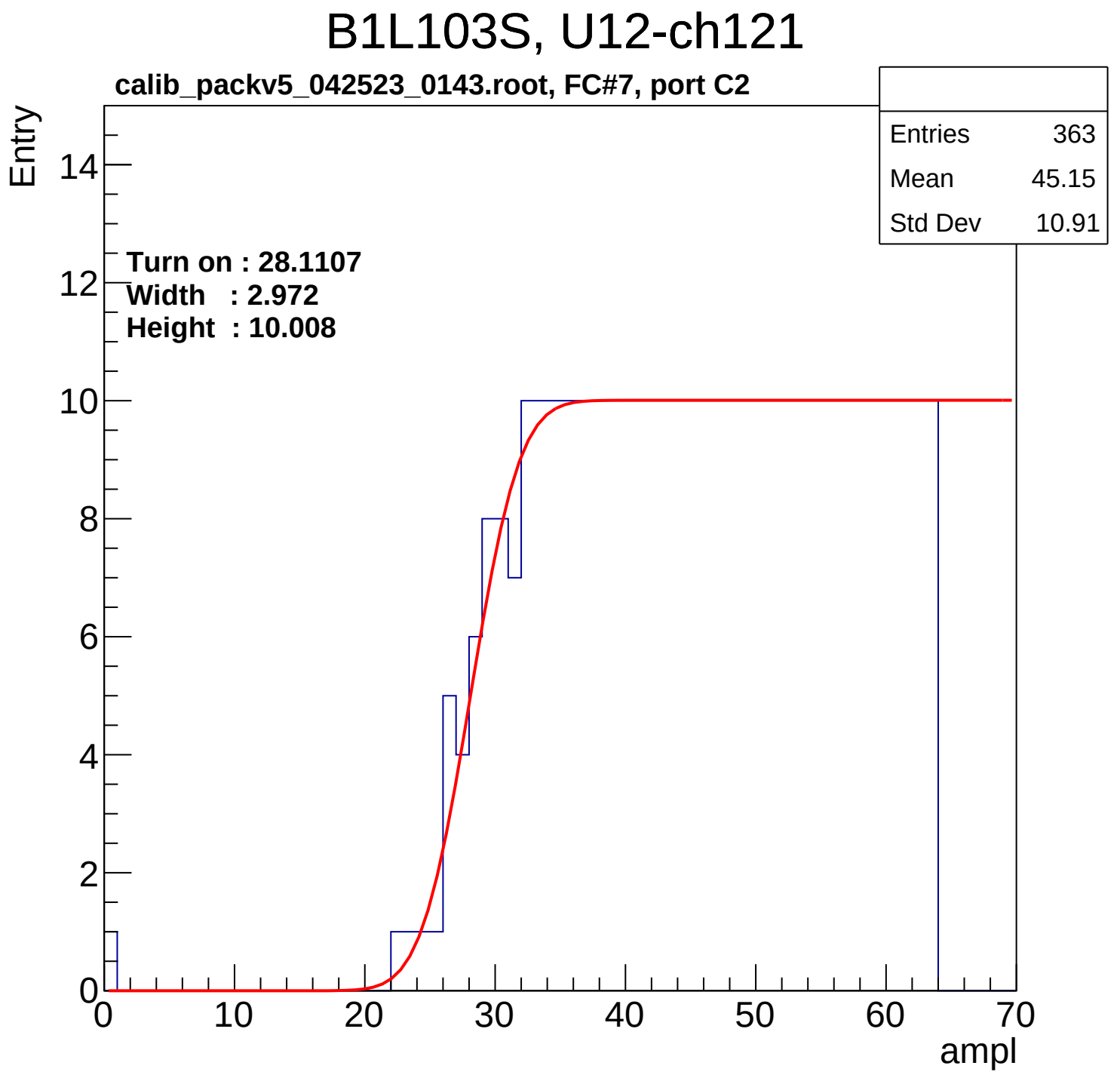

B1L103S, U12-ch116
calib_packv5_042523_0143.root, FC#7, port C2
Entries 371
Mean 44.56
Std Dev 11.6
Turn on : 27.4141
Width : 4.140
Height : 10.047
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

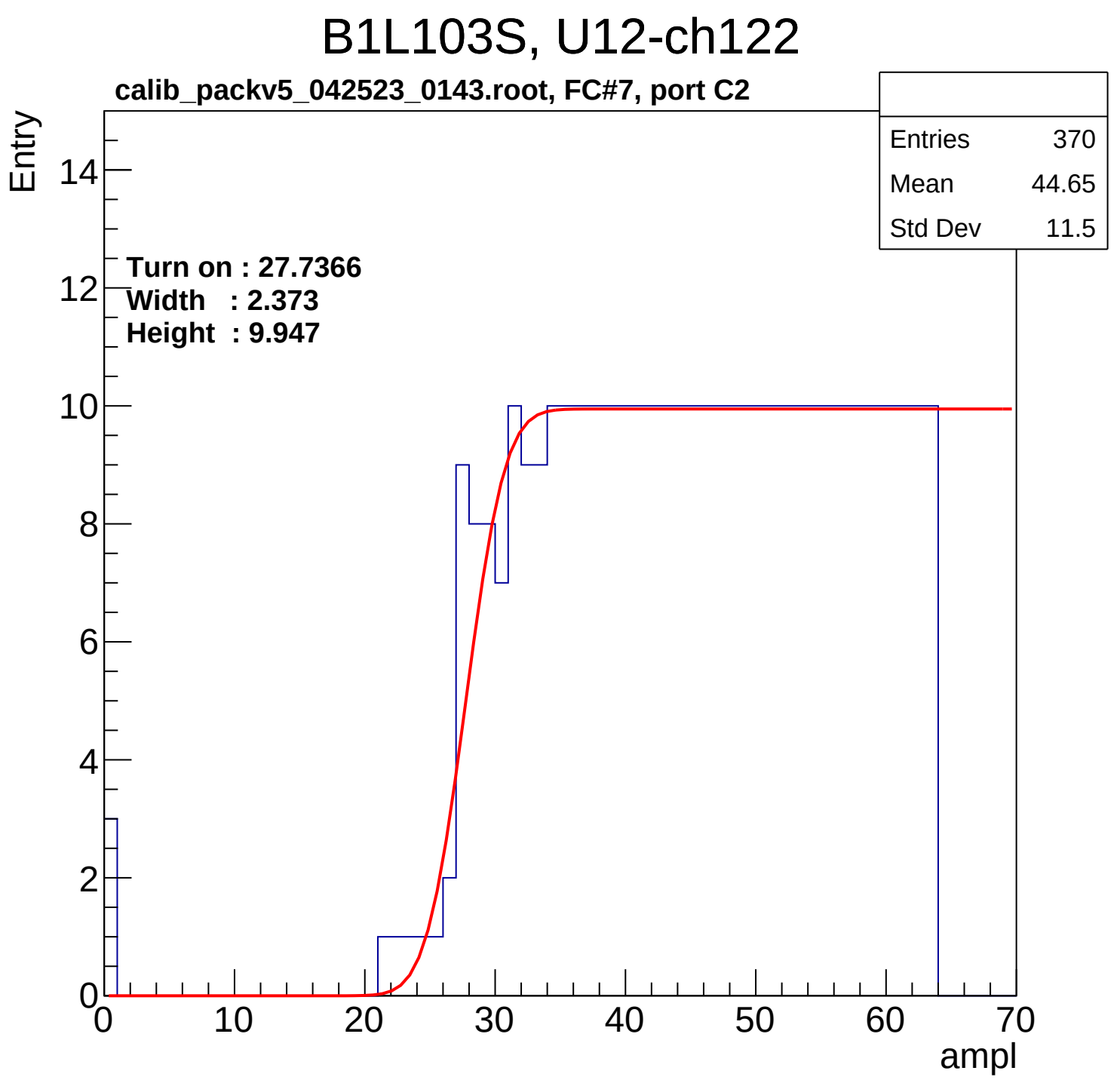

B1L103S, U12-ch117
calib_packv5_042523_0143.root, FC#7, port C2
Entries 378
Mean 44.33
Std Dev 11.5
Turn on : 26.3827
Width : 3.181
Height : 9.997
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

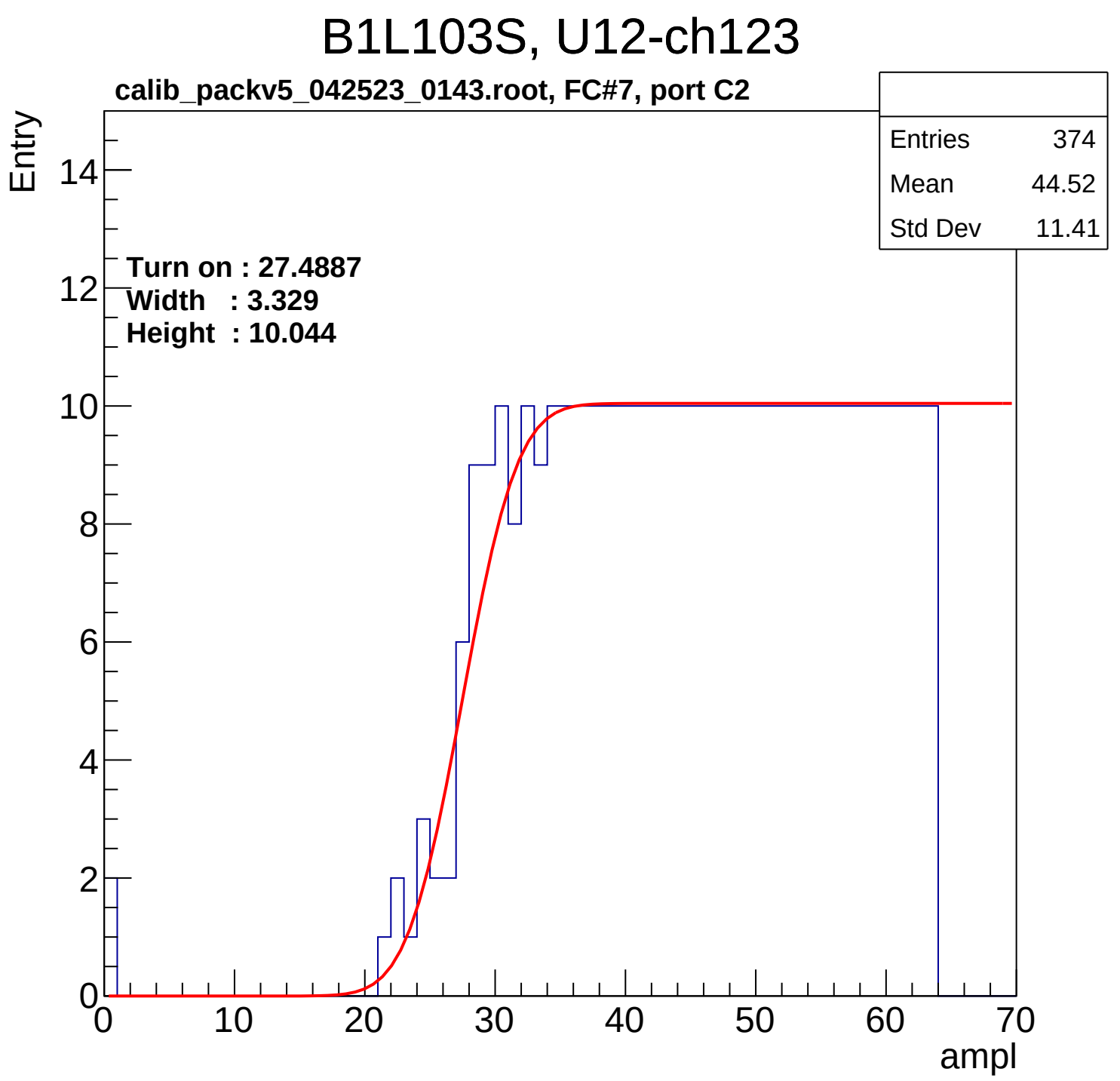

B1L103S, U12-ch118
calib_packv5_042523_0143.root, FC#7, port C2
Entries 401
Mean 43.18
Std Dev 12.14
Turn on : 24.4873
Width : 3.809
Height : 10.041
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

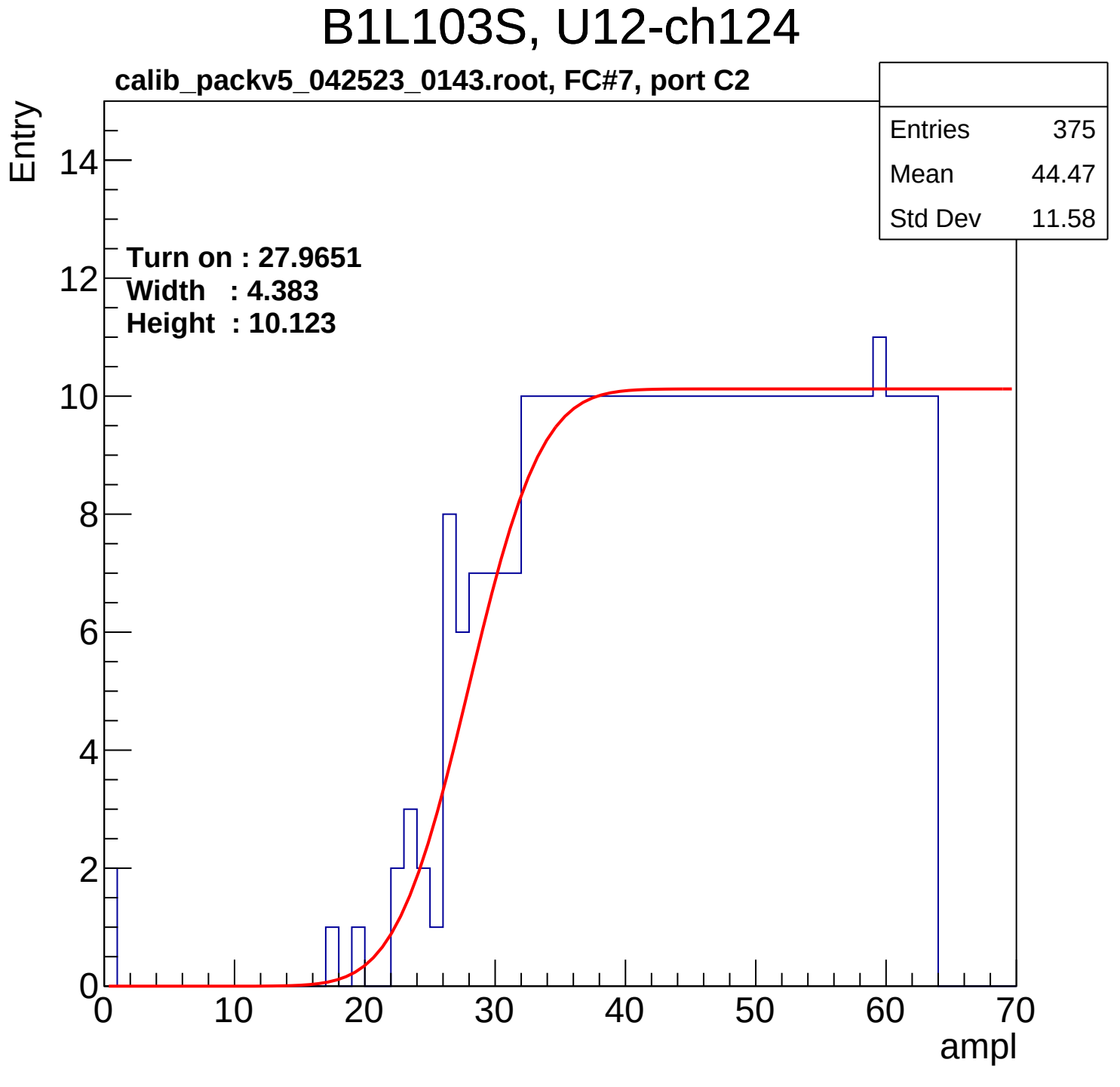

B1L103S, U12-ch119
calib_packv5_042523_0143.root, FC#7, port C2
Entries 387
Mean 43.79
Std Dev 12.04
Turn on : 26.8460
Width : 2.493
Height : 10.077
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

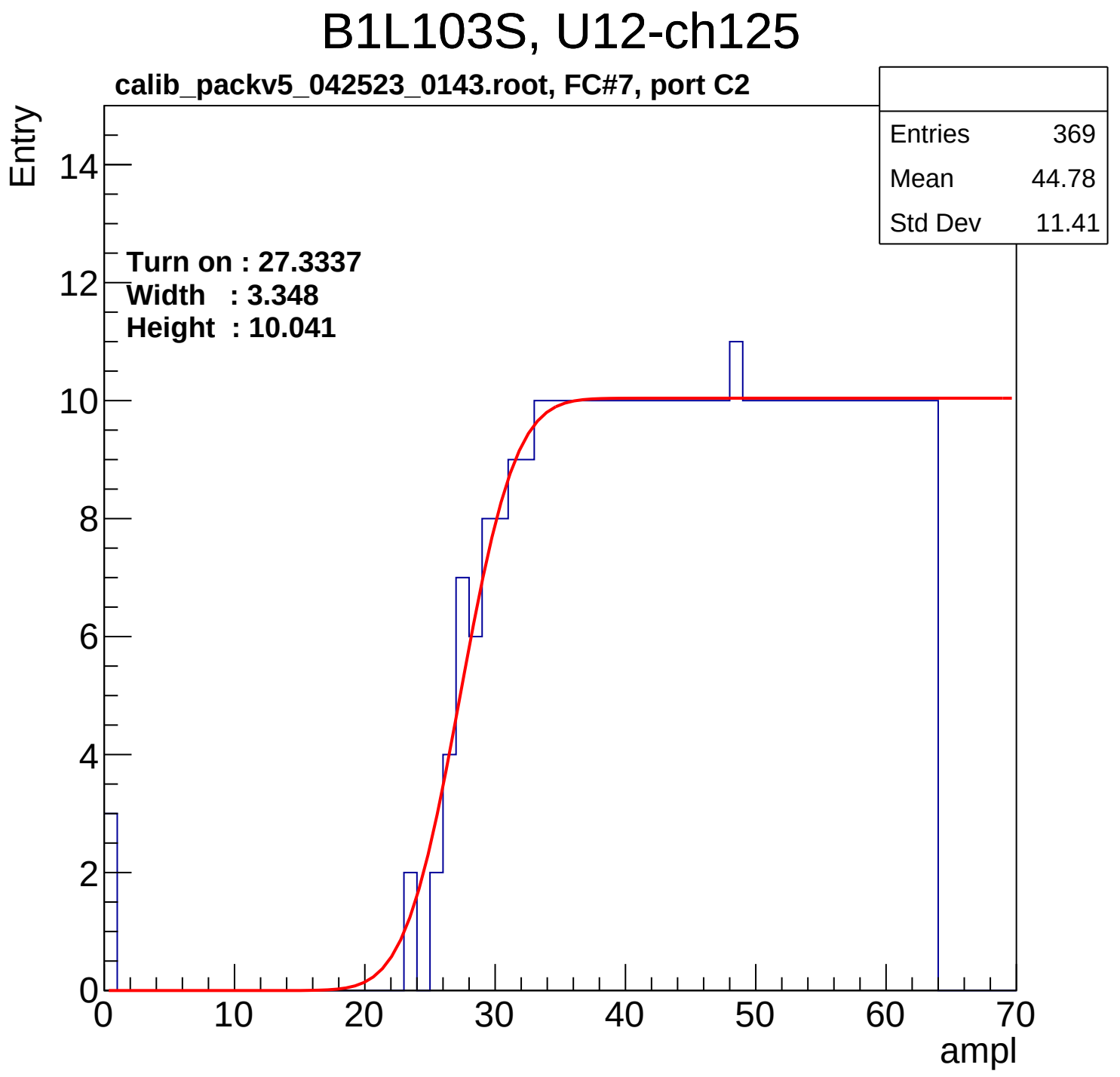

B1L103S, U12-ch120
calib_packv5_042523_0143.root, FC#7, port C2
Entries 381
Mean 44.13
Std Dev 11.74
Turn on : 26.0702
Width : 3.215
Height : 9.976
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

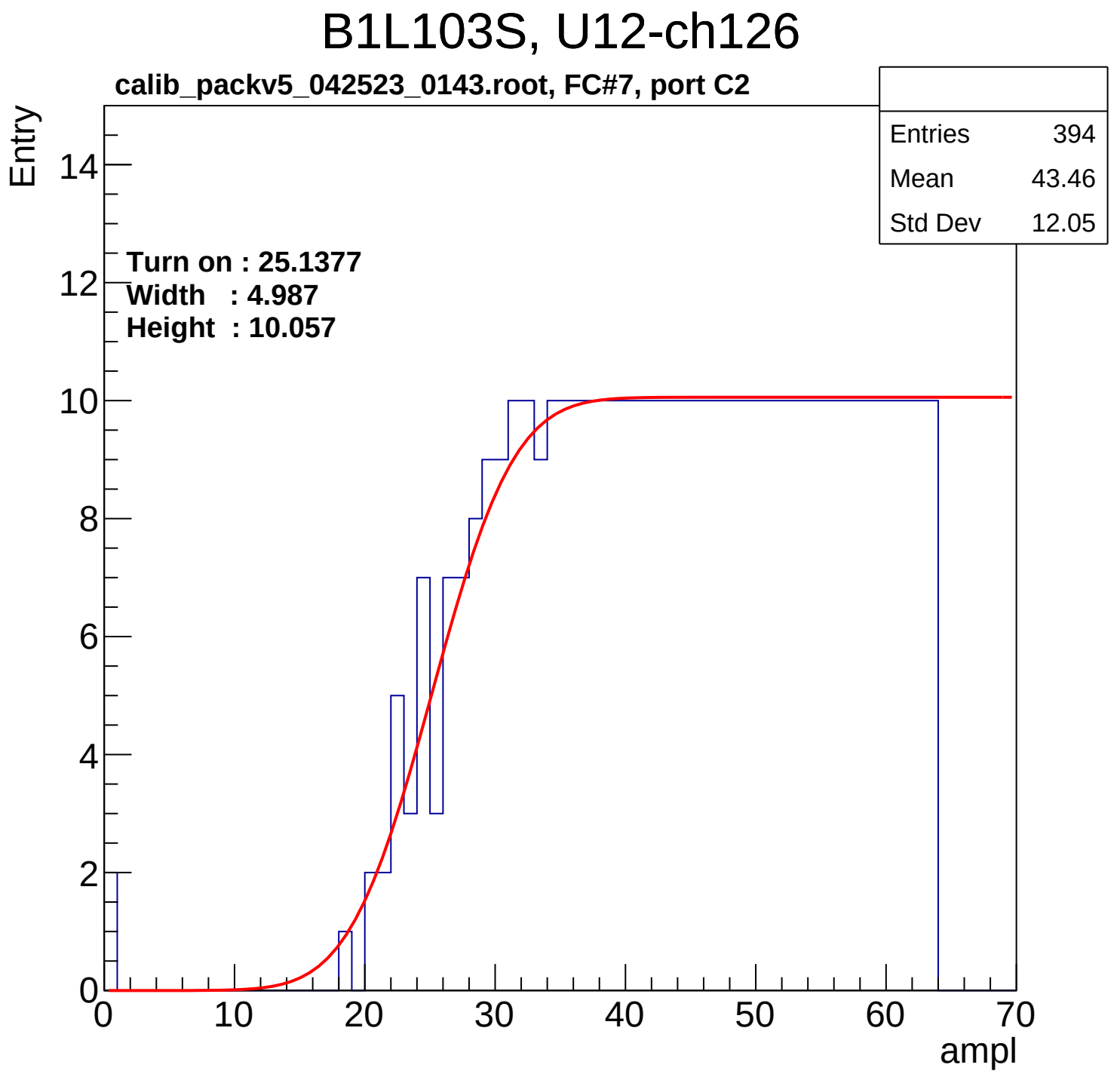

B1L103S, U12-ch121
calib_packv5_042523_0143.root, FC#7, port C2
Entries 363
Mean 45.15
Std Dev 10.91
Turn on : 28.1107
Width : 2.972
Height : 10.008
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

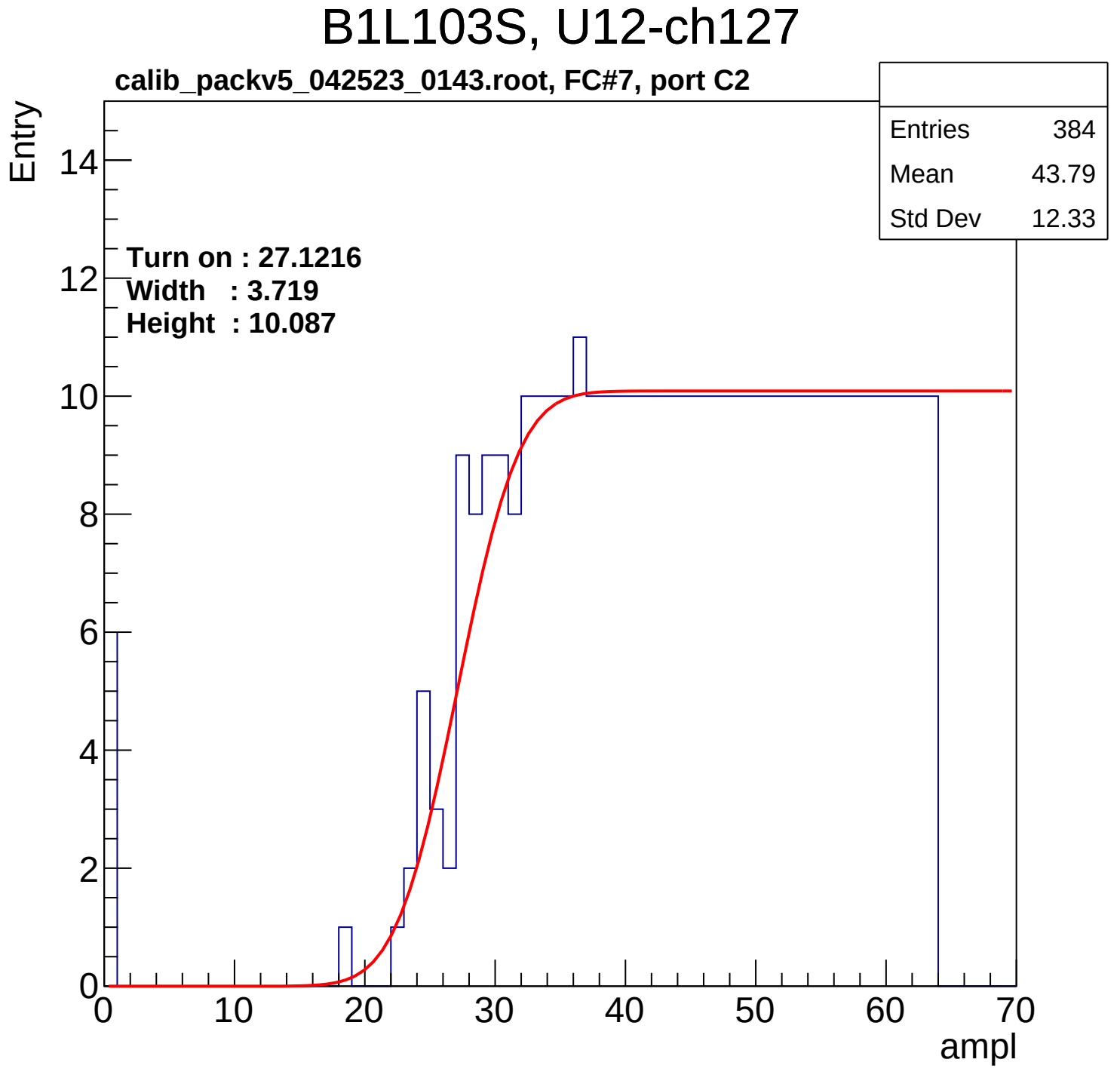

B1L103S, U12-ch122
calib_packv5_042523_0143.root, FC#7, port C2
Entries 370
Mean 44.65
Std Dev 11.5
Turn on : 27.7366
Width : 2.373
Height : 9.947
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

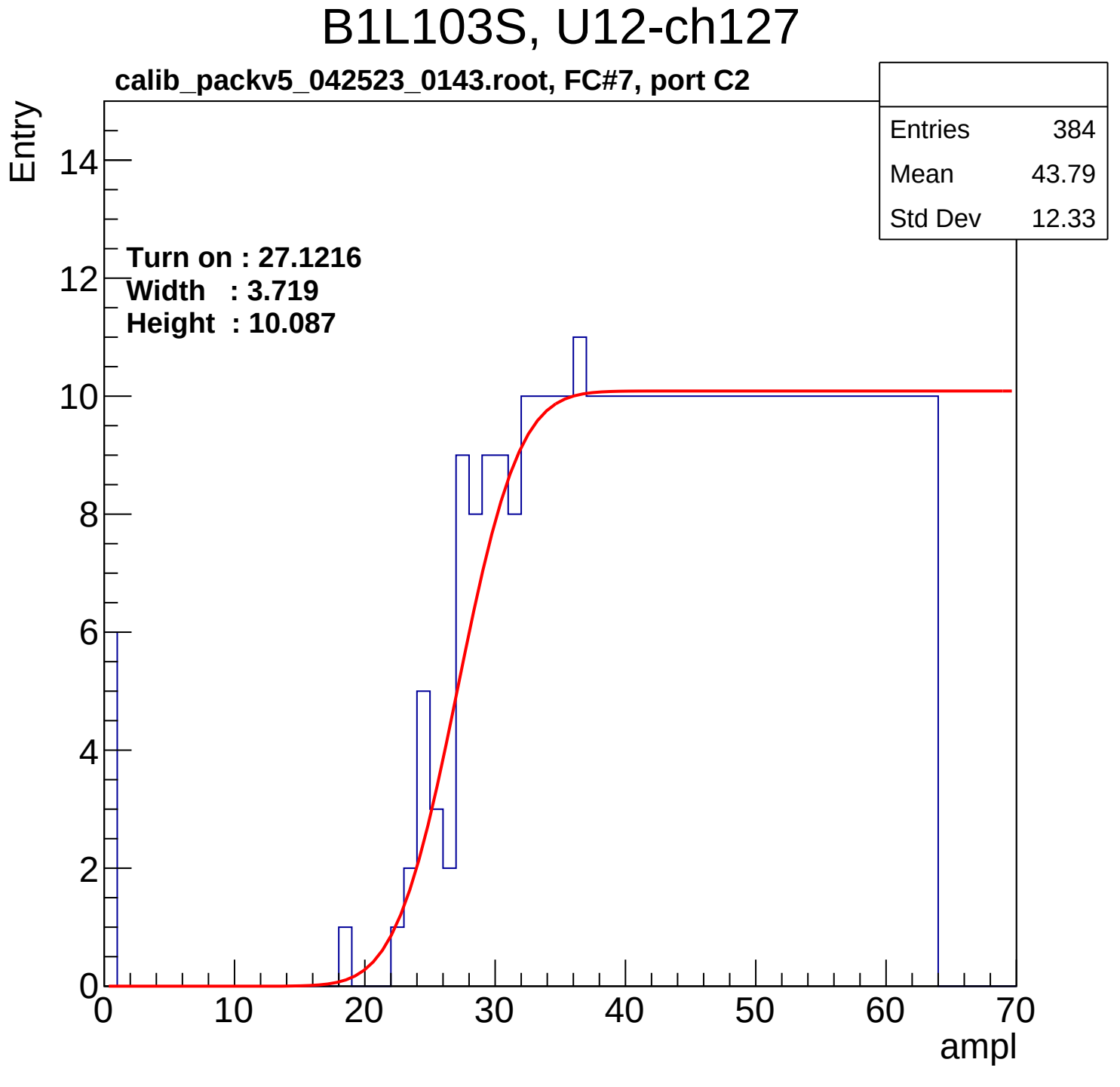

B1L103S, U12-ch123
calib_packv5_042523_0143.root, FC#7, port C2
Entries 374
Mean 44.52
Std Dev 11.41
Turn on : 27.4887
Width : 3.329
Height : 10.044
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U12-ch124
calib_packv5_042523_0143.root, FC#7, port C2
Entries 375
Mean 44.47
Std Dev 11.58
Turn on : 27.9651
Width : 4.383
Height : 10.123
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U12-ch125
calib_packv5_042523_0143.root, FC#7, port C2
Entries 369
Mean 44.78
Std Dev 11.41
Turn on : 27.3337
Width : 3.348
Height : 10.041
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U12-ch126
calib_packv5_042523_0143.root, FC#7, port C2
Entries 394
Mean 43.46
Std Dev 12.05
Turn on : 25.1377
Width : 4.987
Height : 10.057
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U12-ch127
calib_packv5_042523_0143.root, FC#7, port C2
Entries 384
Mean 43.79
Std Dev 12.33
Turn on : 27.1216
Width : 3.719
Height : 10.087
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U12-ch127
calib_packv5_042523_0143.root, FC#7, port C2
Entries 384
Mean 43.79
Std Dev 12.33
Turn on : 27.1216
Width : 3.719
Height : 10.087
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70