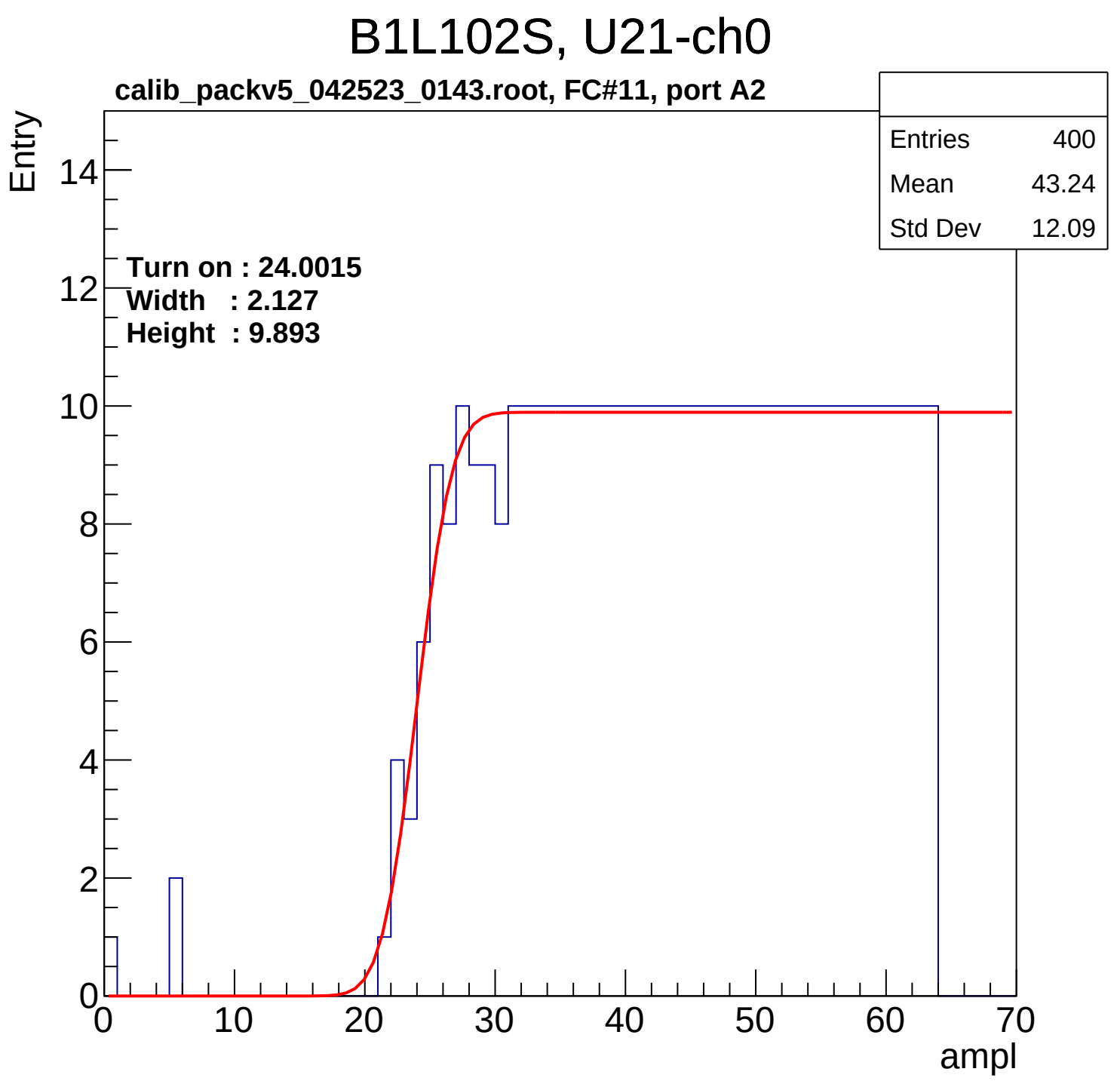
B1L102S, U21-ch0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 400
Mean 43.24
Std Dev 12.09
Turn on : 24.0015
Width : 2.127
Height : 9.893
Entry
ampl
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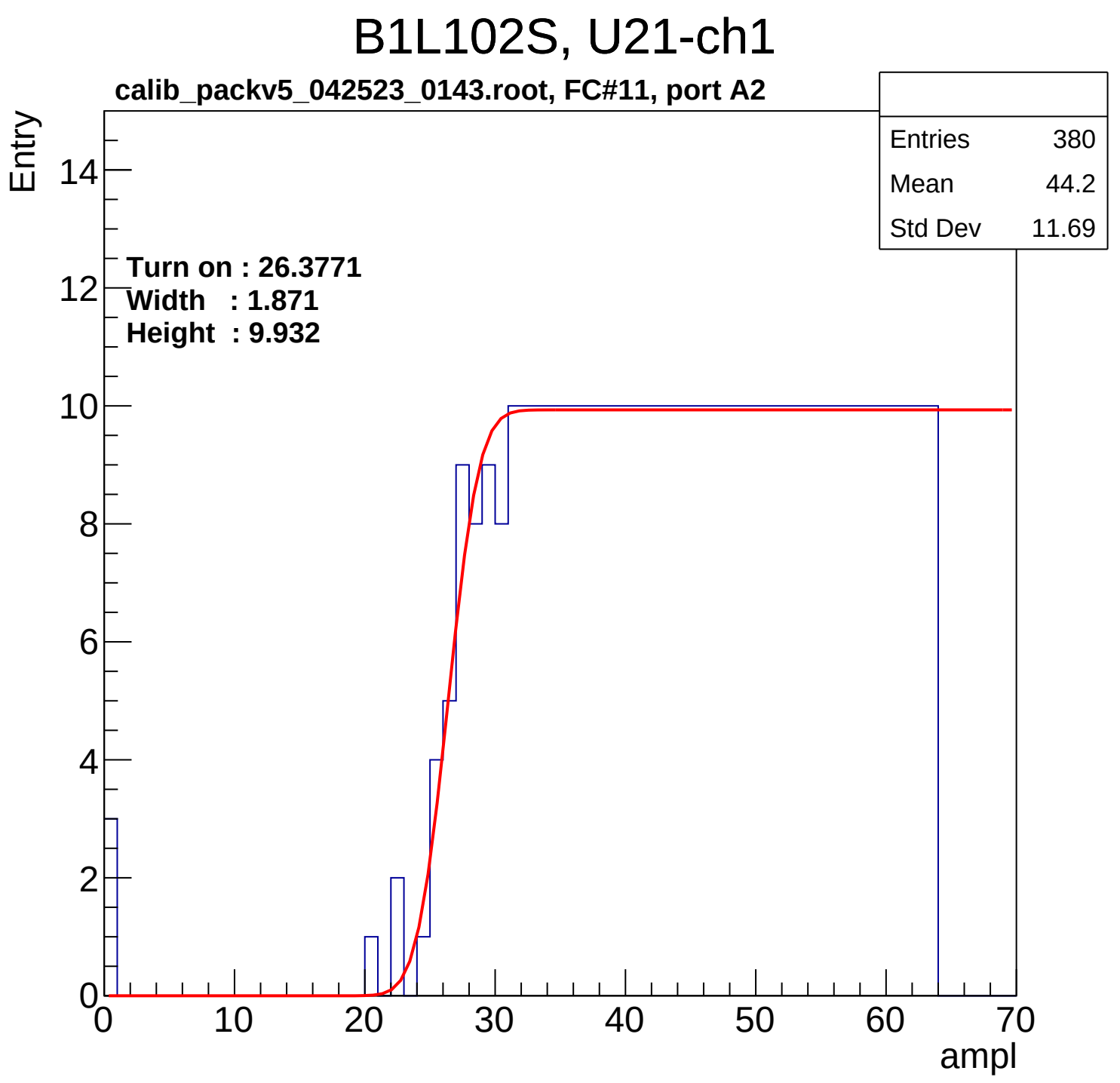
B1L102S, U21-ch1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 380
Mean 44.2
Std Dev 11.69
Turn on : 26.3771
Width : 1.871
Height : 9.932
Entry
ampl
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2
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6
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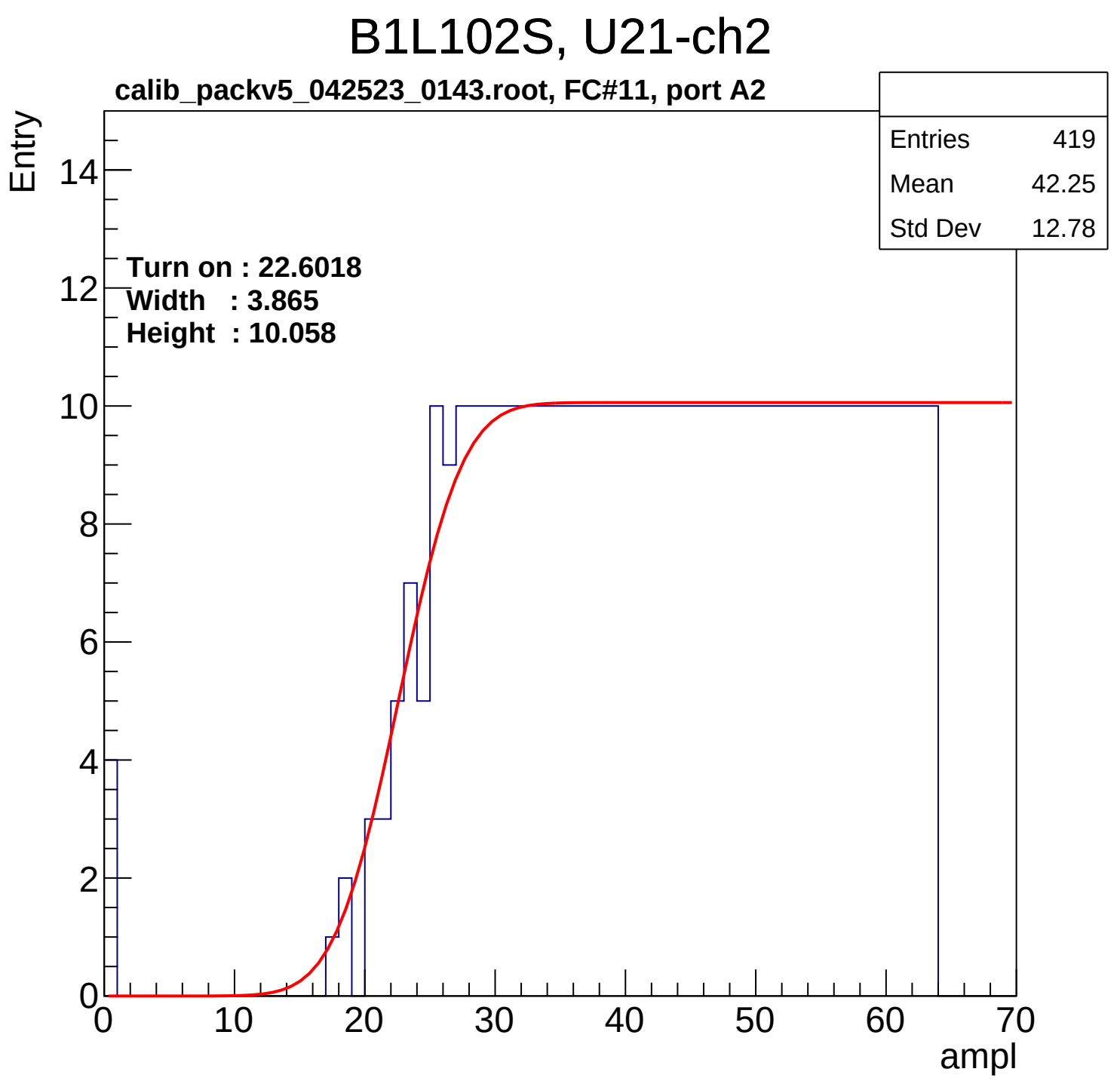
B1L102S, U21-ch2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 419
Mean 42.25
Std Dev 12.78
Turn on : 22.6018
Width : 3.865
Height : 10.058
Entry
ampl
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2
4
6
8
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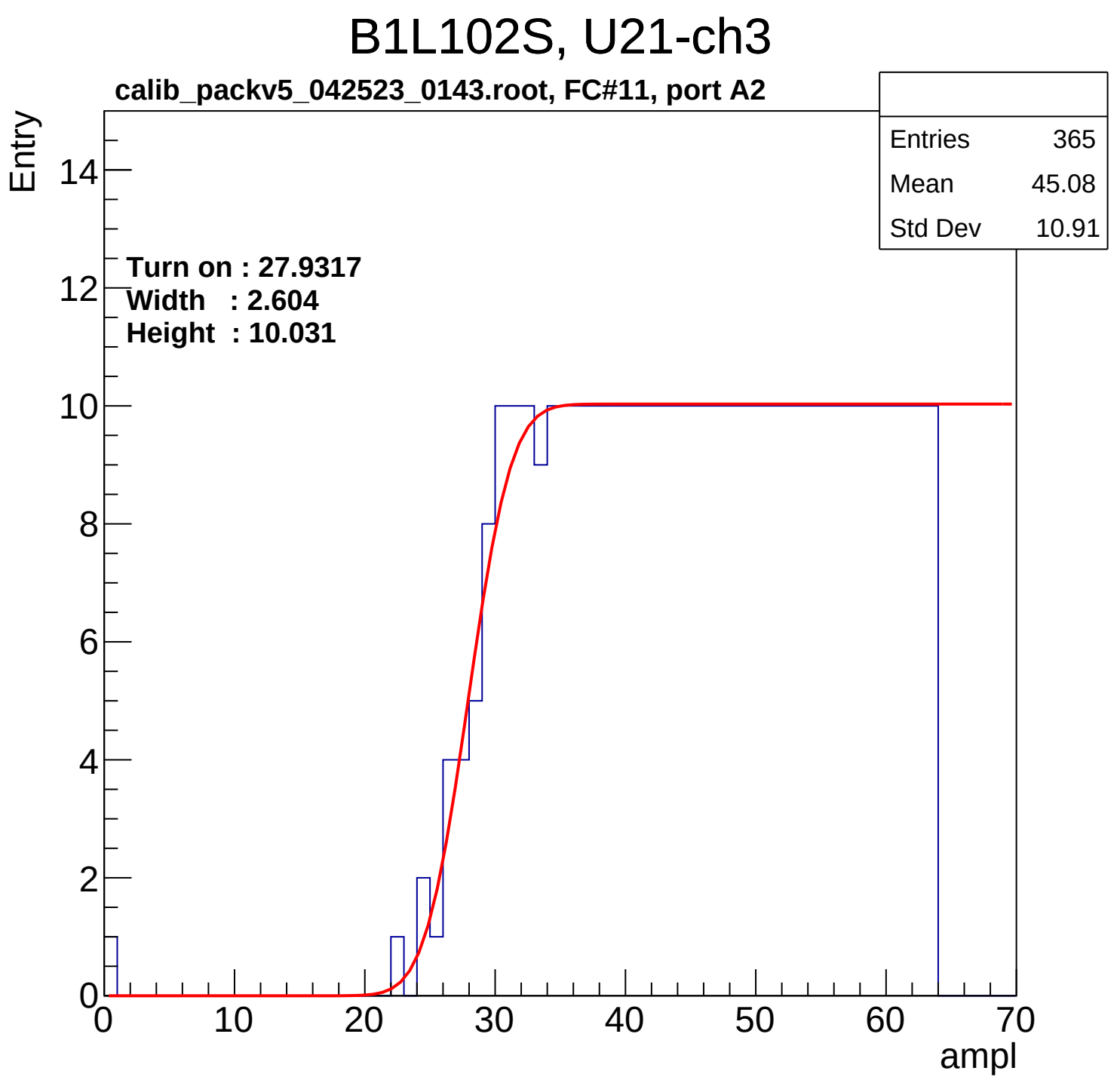
B1L102S, U21-ch3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 365
Mean 45.08
Std Dev 10.91
Turn on : 27.9317
Width : 2.604
Height : 10.031
Entry
ampl
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2
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6
8
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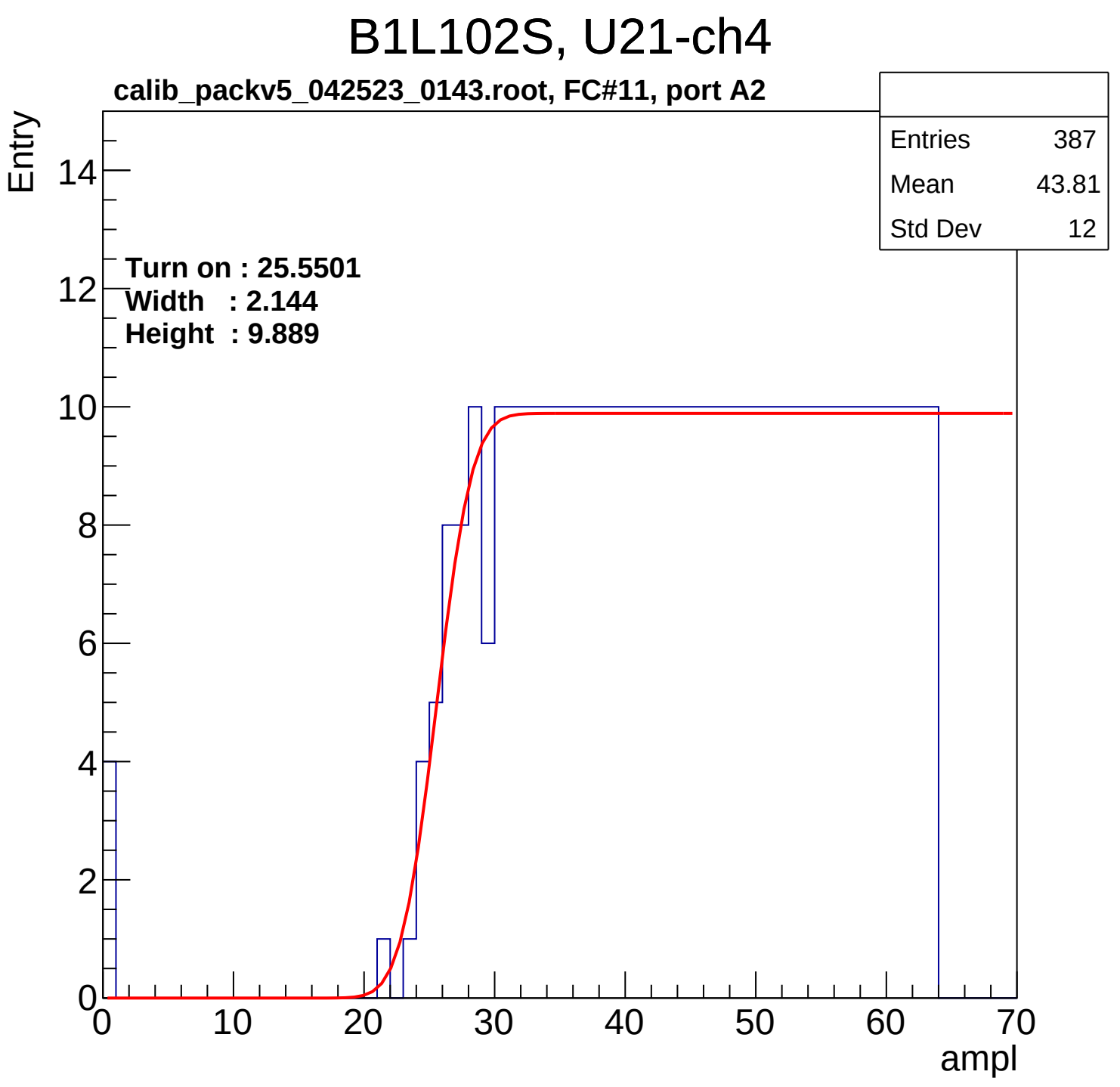
B1L102S, U21-ch4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 43.81
Std Dev 12
Turn on : 25.5501
Width : 2.144
Height : 9.889
Entry
ampl
0
2
4
6
8
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12
14
0
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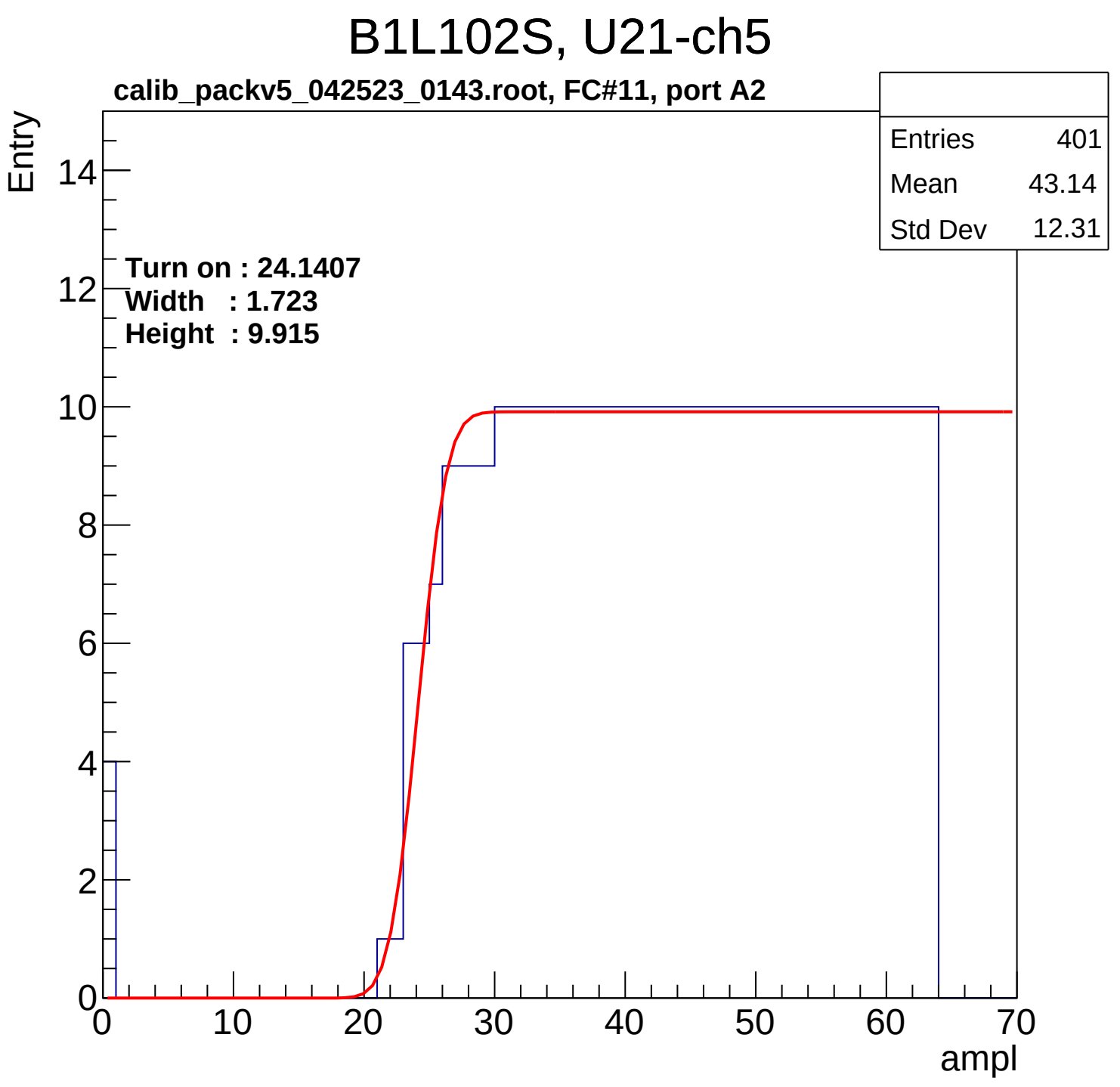
B1L102S, U21-ch5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 401
Mean 43.14
Std Dev 12.31
Turn on : 24.1407
Width : 1.723
Height : 9.915
Entry
ampl
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2
4
6
8
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0
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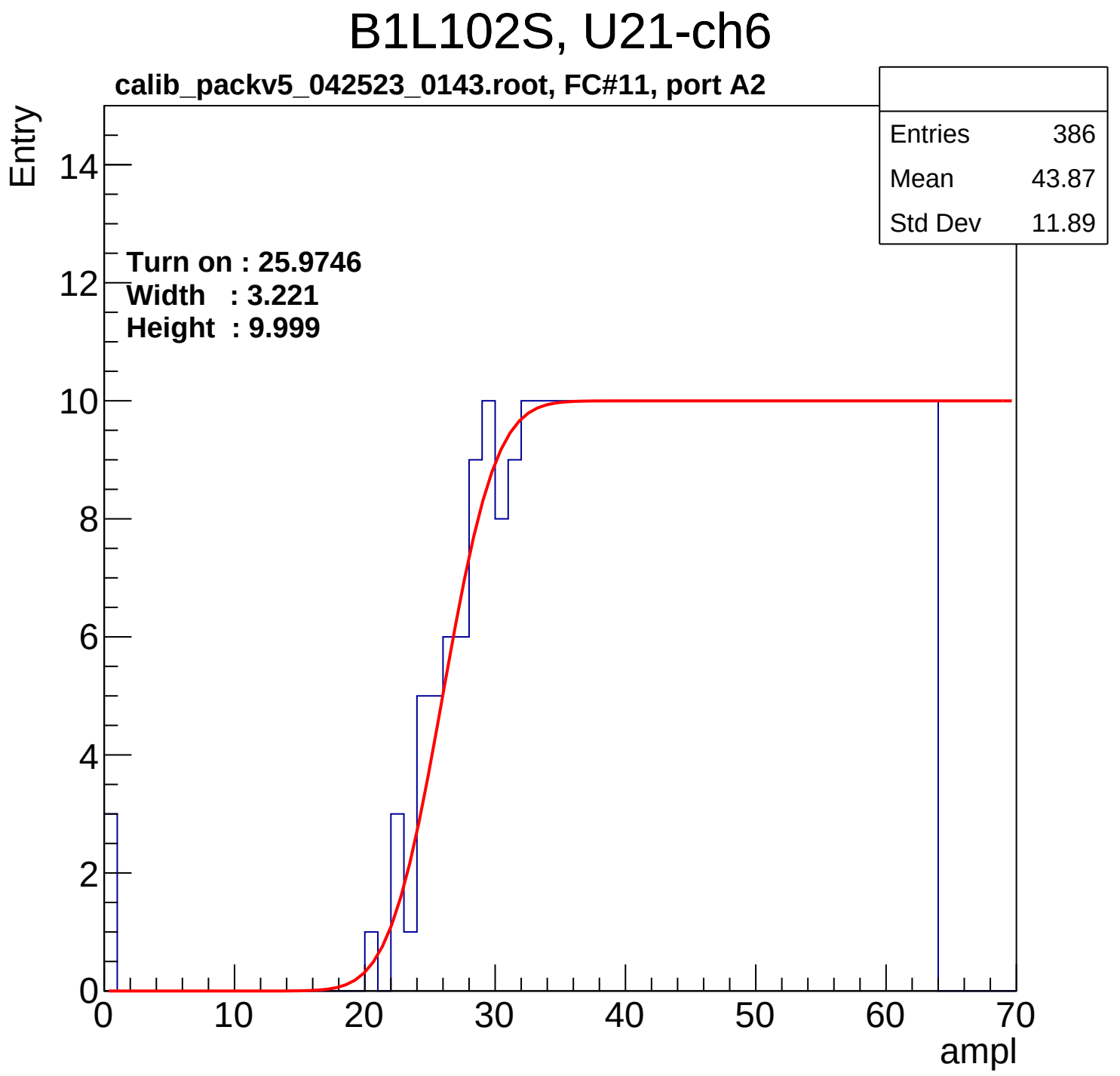
B1L102S, U21-ch6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 386
Mean 43.87
Std Dev 11.89
Turn on : 25.9746
Width : 3.221
Height : 9.999
Entry
ampl
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2
4
6
8
10
12
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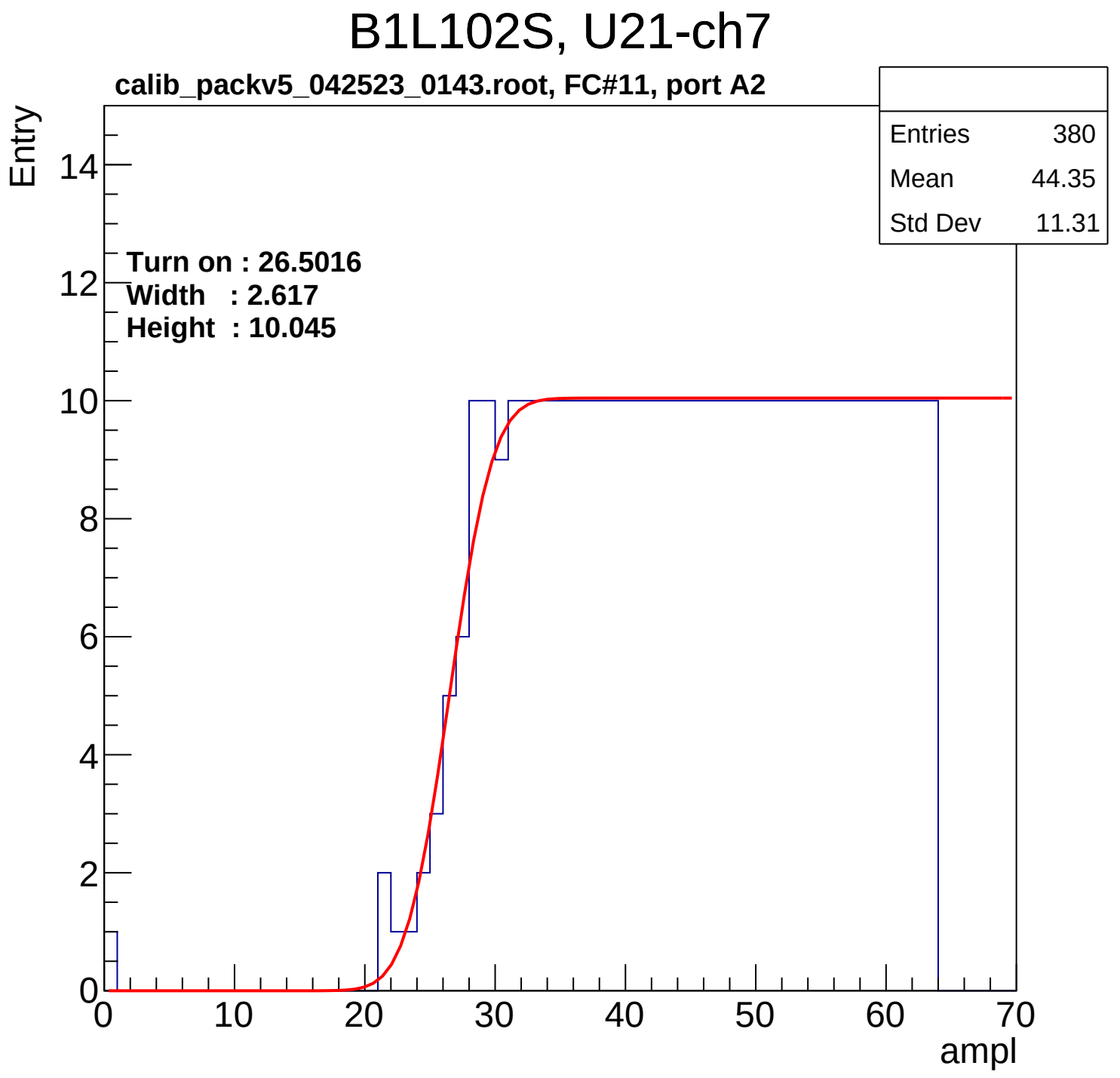
B1L102S, U21-ch7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 380
Mean 44.35
Std Dev 11.31
Turn on : 26.5016
Width : 2.617
Height : 10.045
Entry
ampl
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6
8
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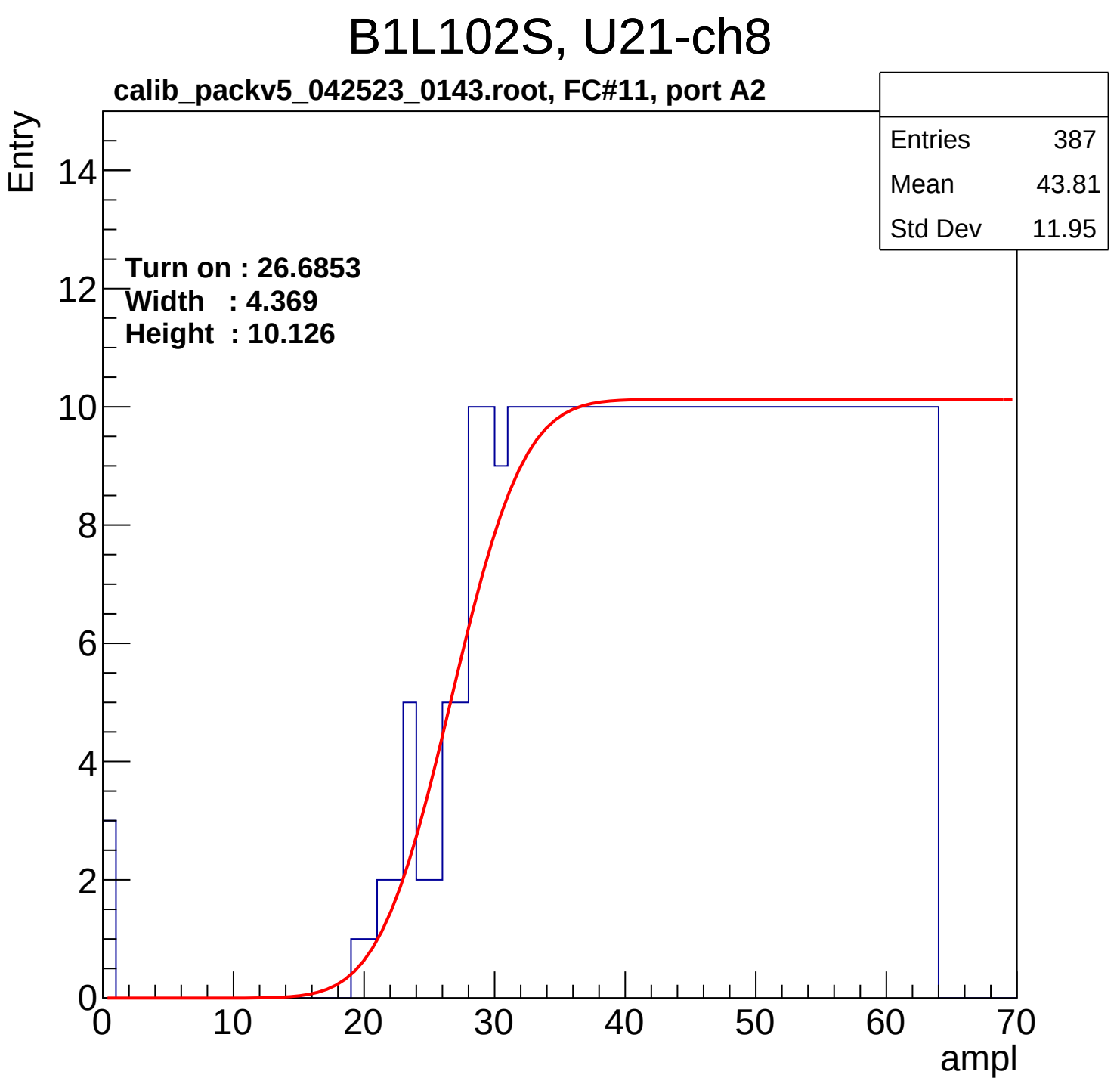
B1L102S, U21-ch8
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 43.81
Std Dev 11.95
Turn on : 26.6853
Width : 4.369
Height : 10.126
Entry
ampl
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6
8
10
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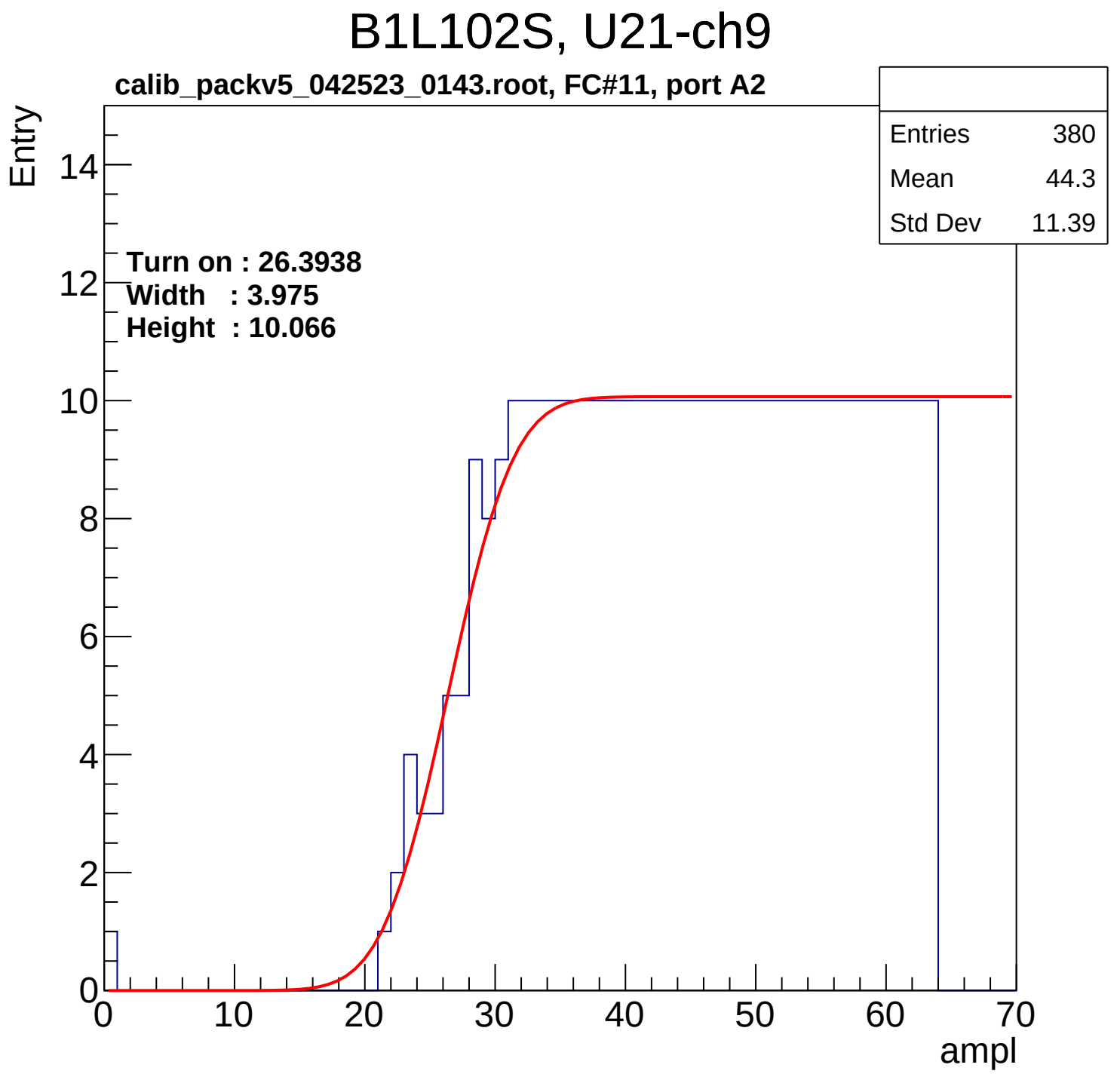
B1L102S, U21-ch9
calib_packv5_042523_0143.root, FC#11, port A2
Entries 380
Mean 44.3
Std Dev 11.39
Turn on : 26.3938
Width : 3.975
Height : 10.066
Entry
ampl
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4
6
8
10
12
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0
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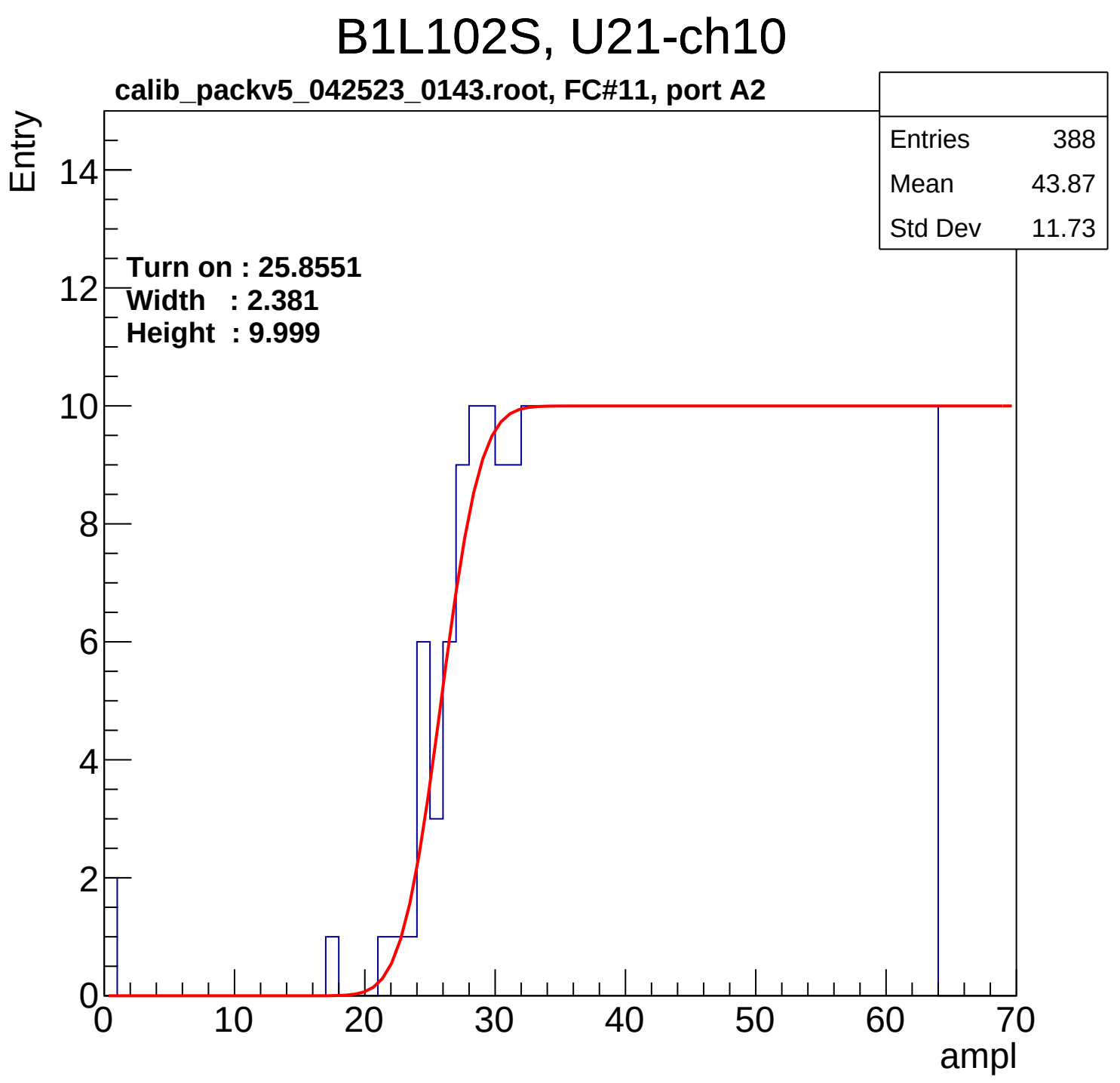
B1L102S, U21-ch10
calib_packv5_042523_0143.root, FC#11, port A2
Entries 388
Mean 43.87
Std Dev 11.73
Turn on : 25.8551
Width : 2.381
Height : 9.999
Entry
ampl
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2
4
6
8
10
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60
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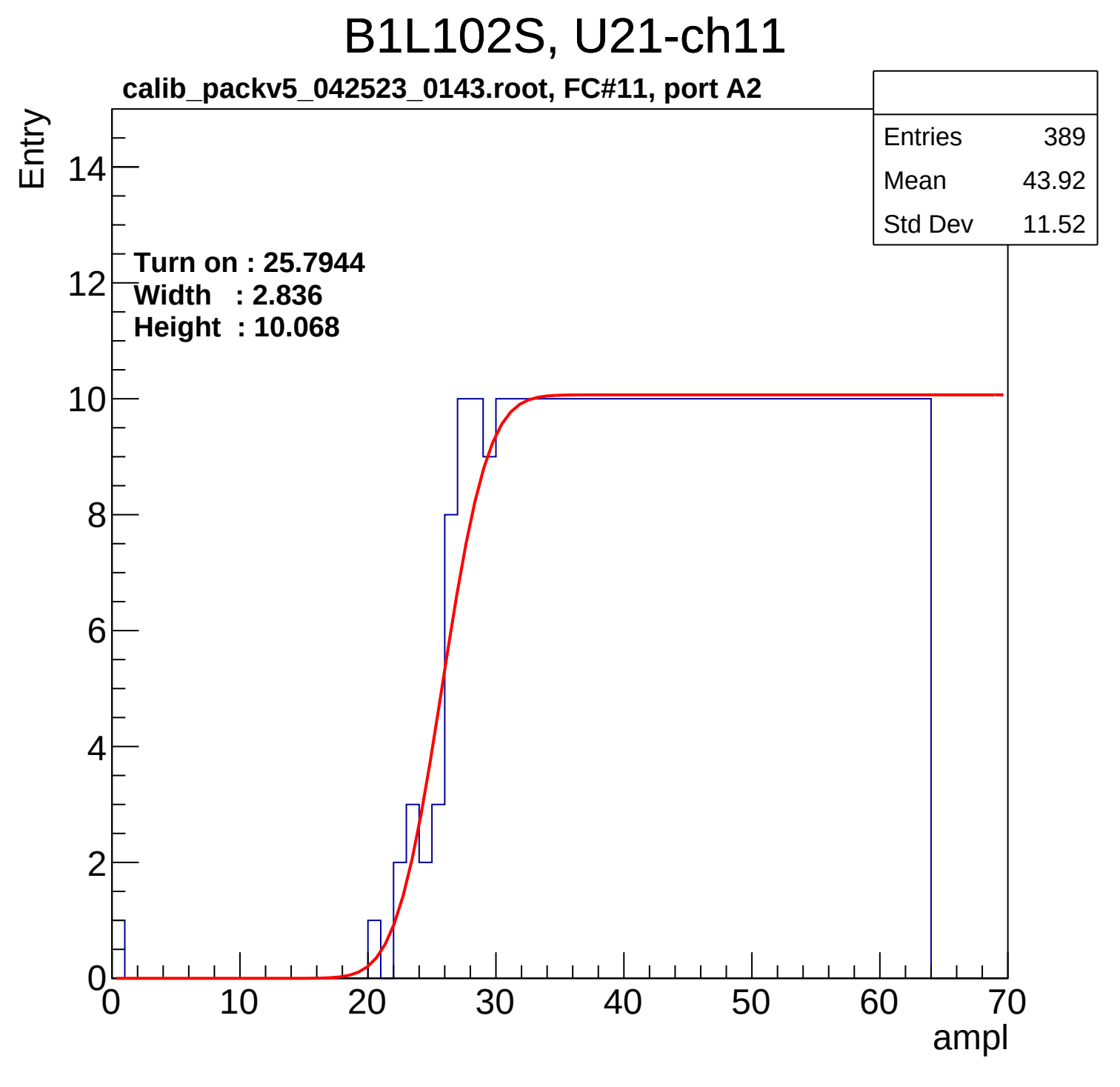
B1L102S, U21-ch11
calib_packv5_042523_0143.root, FC#11, port A2
Entries 389
Mean 43.92
Std Dev 11.52
Turn on : 25.7944
Width : 2.836
Height : 10.068
Entry
ampl
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6
8
10
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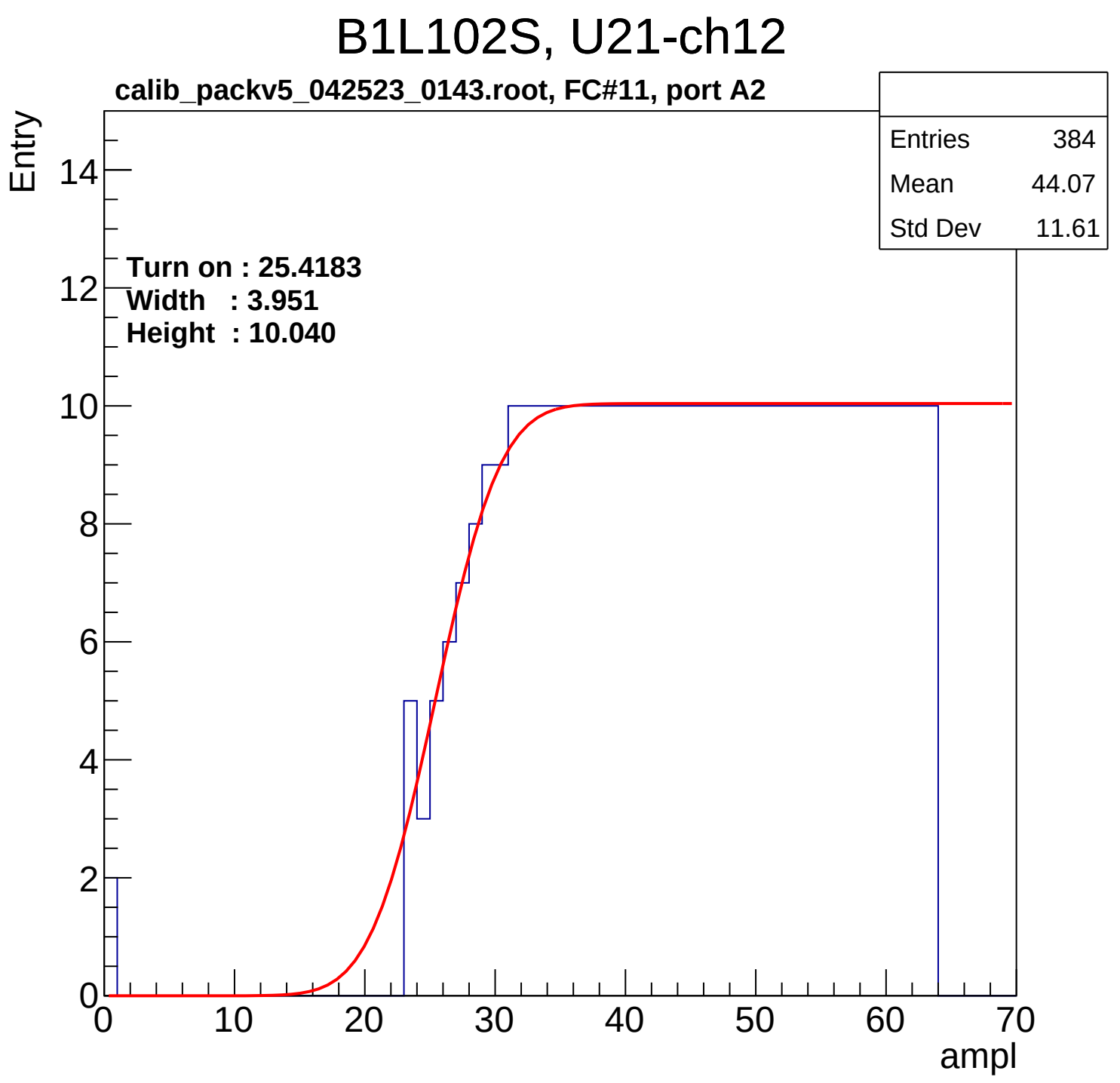
B1L102S, U21-ch12
calib_packv5_042523_0143.root, FC#11, port A2
Entries 384
Mean 44.07
Std Dev 11.61
Turn on : 25.4183
Width : 3.951
Height : 10.040
Entry
ampl
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6
8
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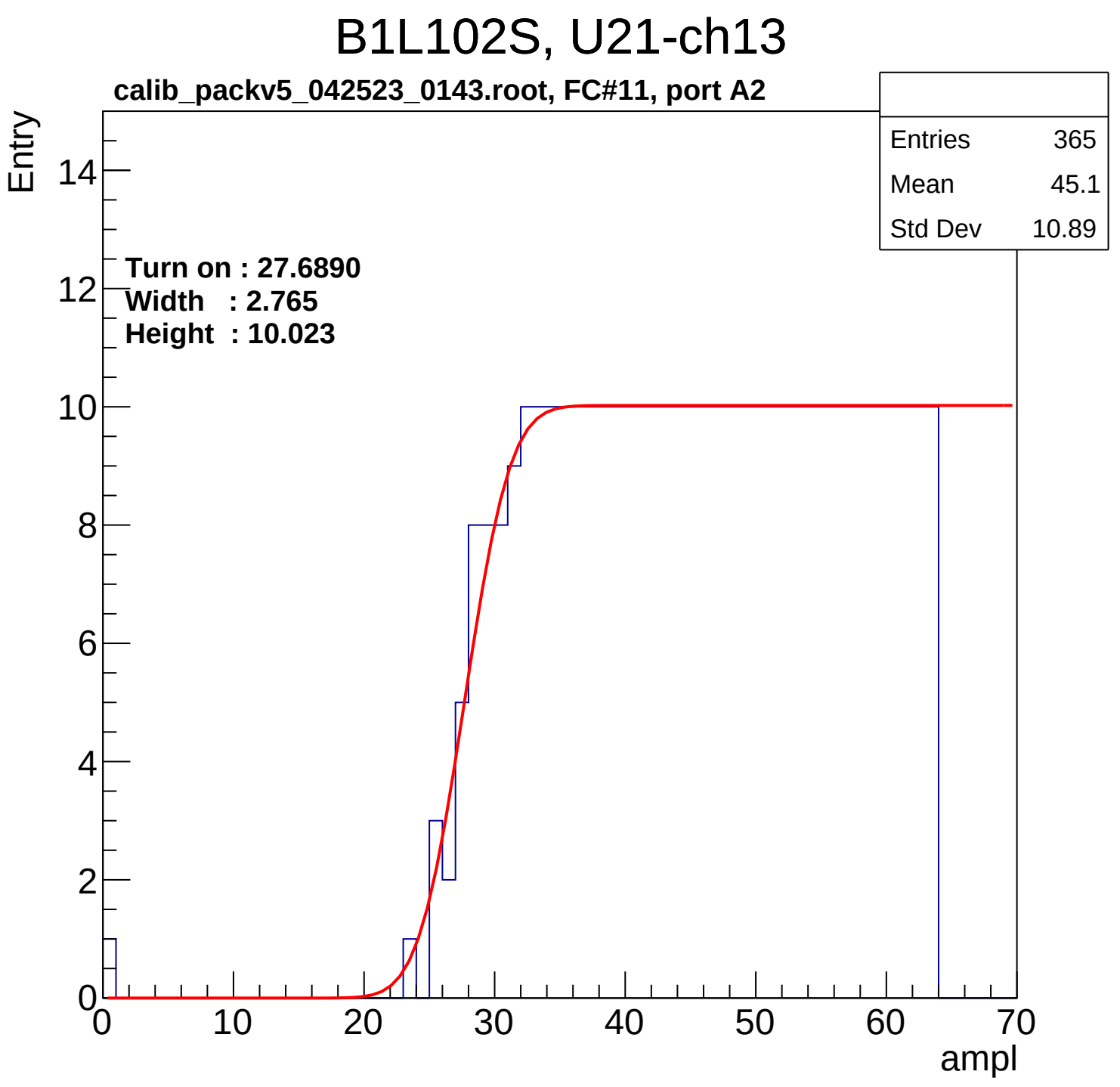
B1L102S, U21-ch13
calib_packv5_042523_0143.root, FC#11, port A2
Entries 365
Mean 45.1
Std Dev 10.89
Turn on : 27.6890
Width : 2.765
Height : 10.023
Entry
ampl
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4
6
8
10
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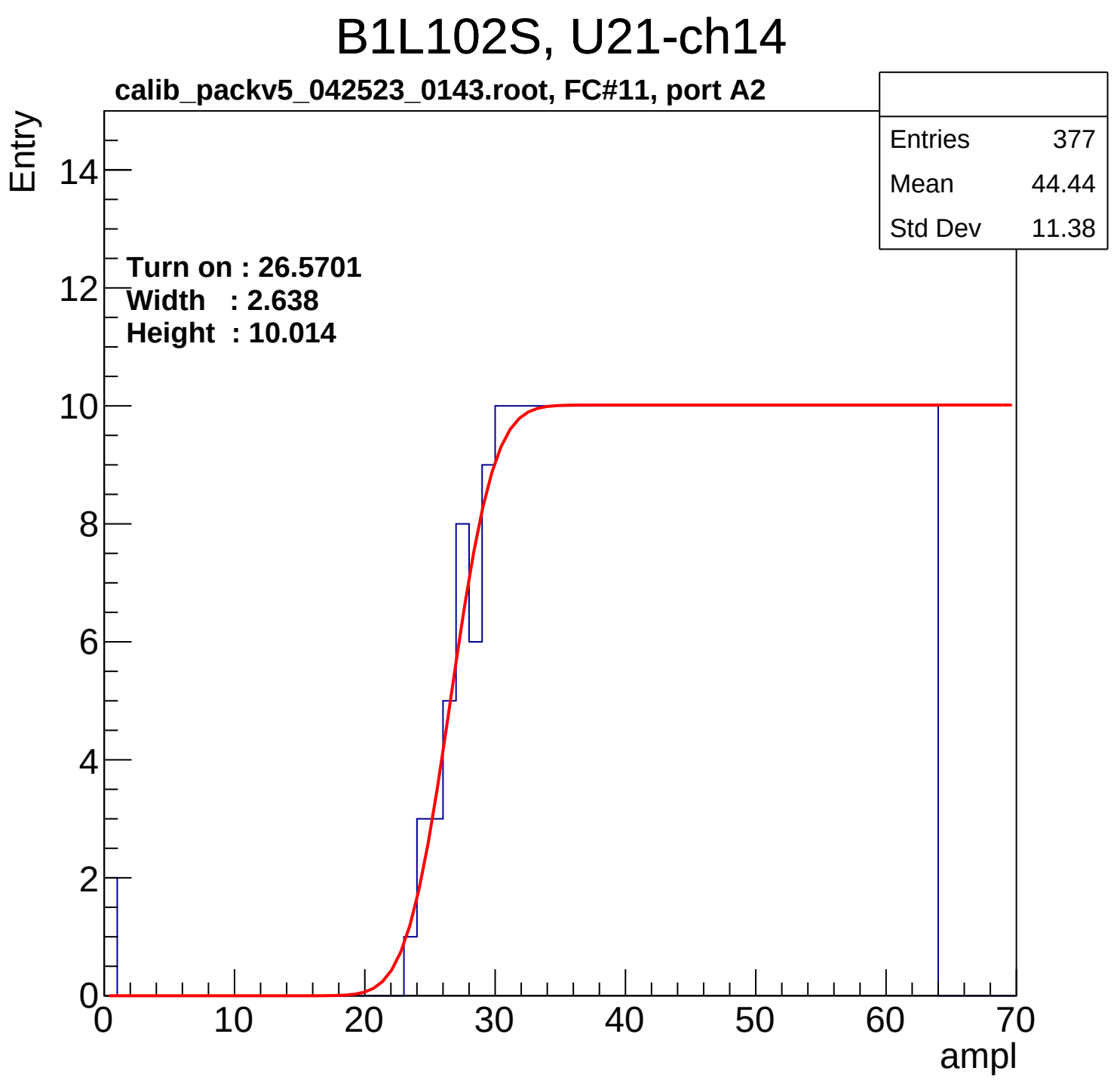
B1L102S, U21-ch14
calib_packv5_042523_0143.root, FC#11, port A2
Entries 377
Mean 44.44
Std Dev 11.38
Turn on : 26.5701
Width : 2.638
Height : 10.014
Entry
ampl
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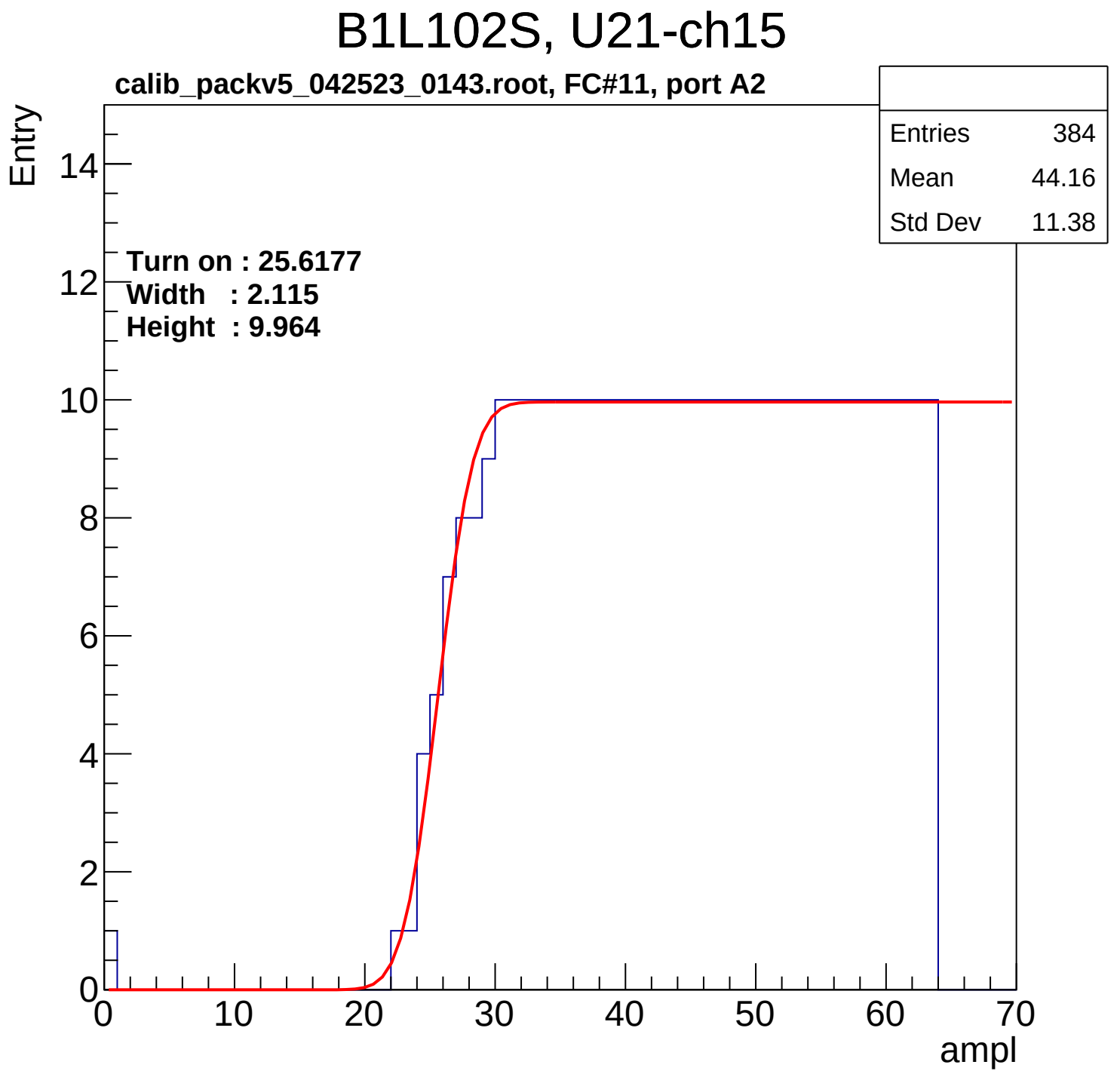
B1L102S, U21-ch15
calib_packv5_042523_0143.root, FC#11, port A2
Entries 384
Mean 44.16
Std Dev 11.38
Turn on : 25.6177
Width : 2.115
Height : 9.964
Entry
ampl
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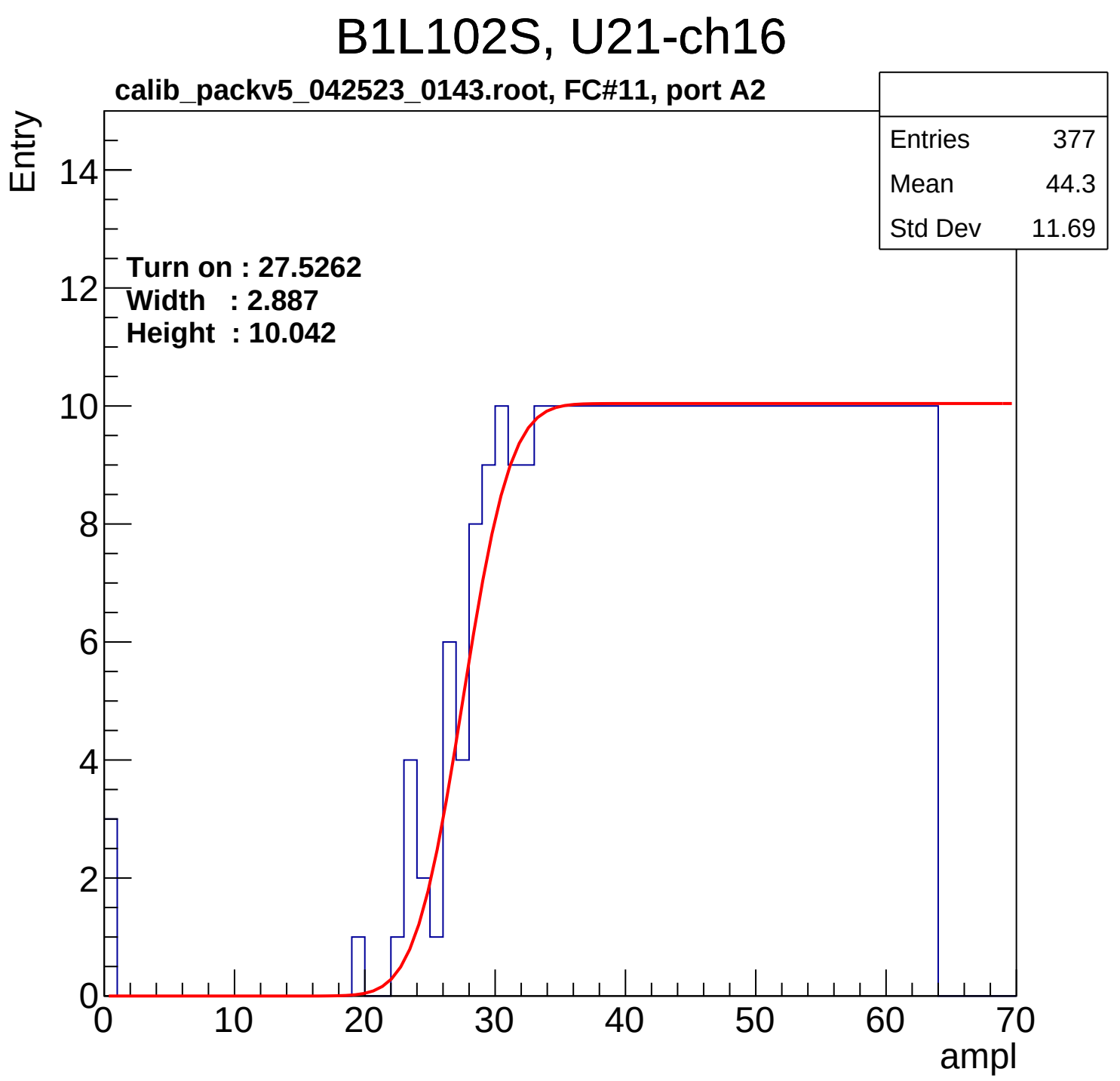
B1L102S, U21-ch16
calib_packv5_042523_0143.root, FC#11, port A2
Entries 377
Mean 44.3
Std Dev 11.69
Turn on : 27.5262
Width : 2.887
Height : 10.042
Entry
ampl
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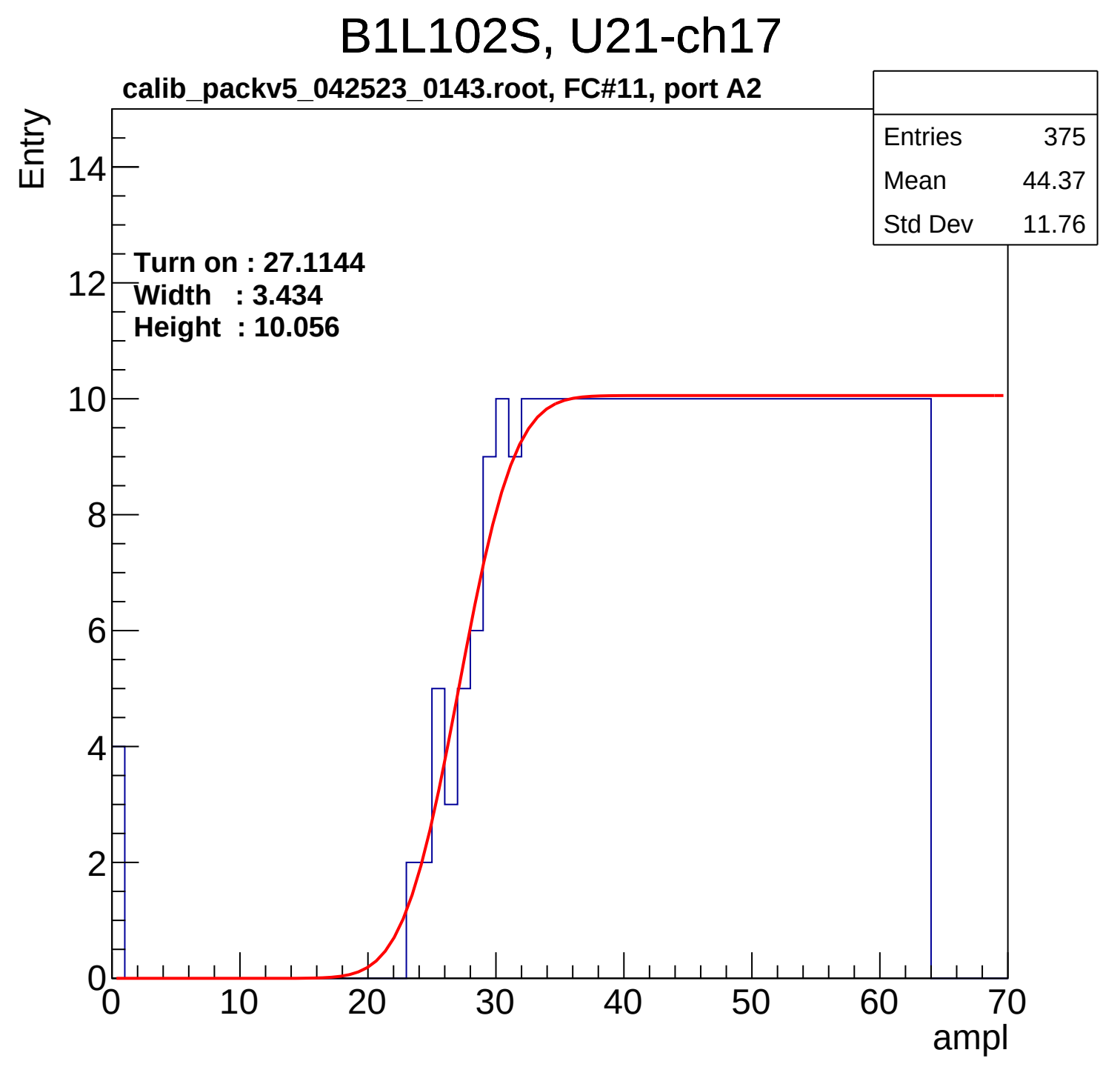
B1L102S, U21-ch17
calib_packv5_042523_0143.root, FC#11, port A2
Entries 375
Mean 44.37
Std Dev 11.76
Turn on : 27.1144
Width : 3.434
Height : 10.056
Entry
ampl
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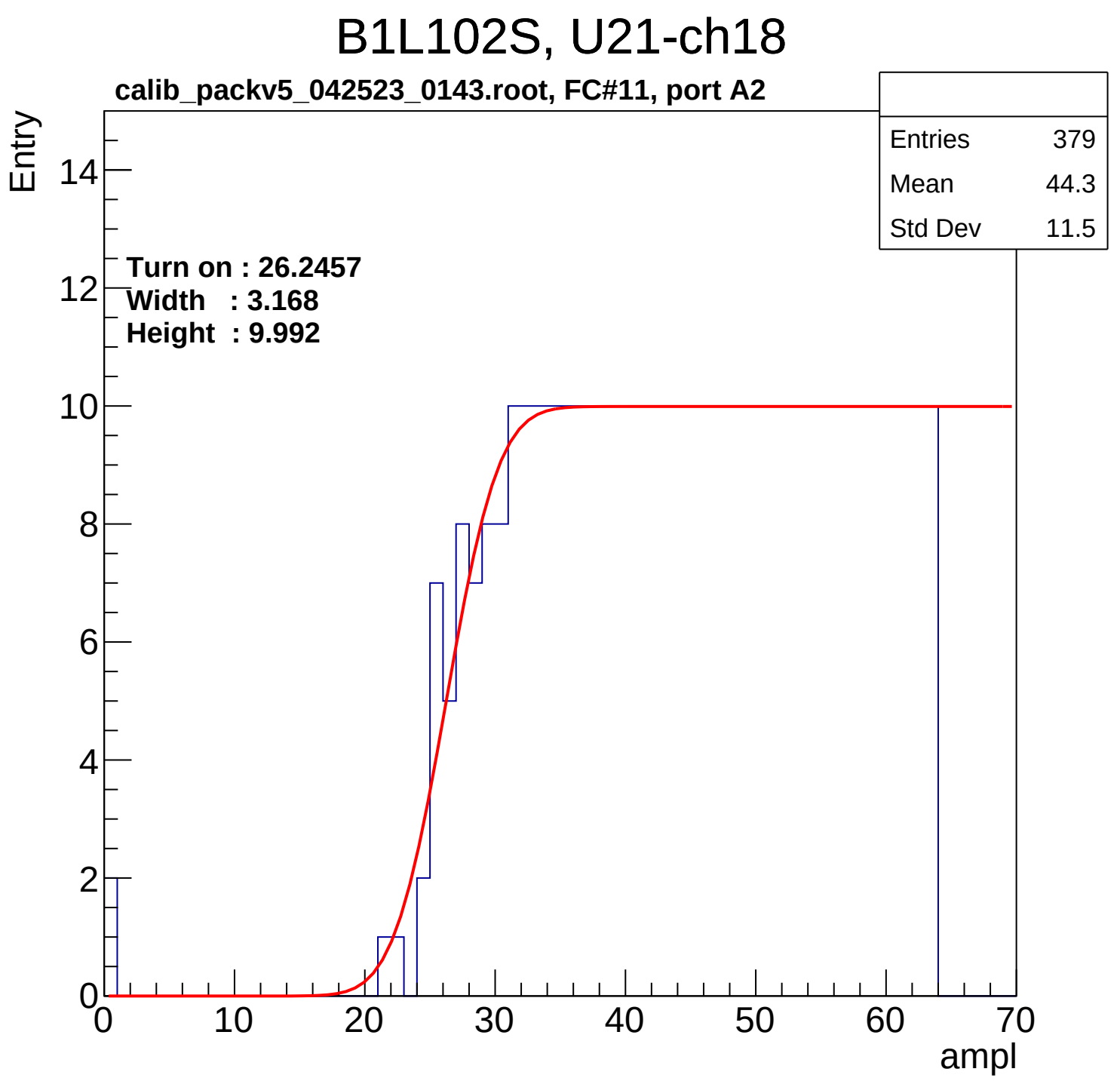
B1L102S, U21-ch18
calib_packv5_042523_0143.root, FC#11, port A2
Entries 379
Mean 44.3
Std Dev 11.5
Turn on : 26.2457
Width : 3.168
Height : 9.992
Entry
ampl
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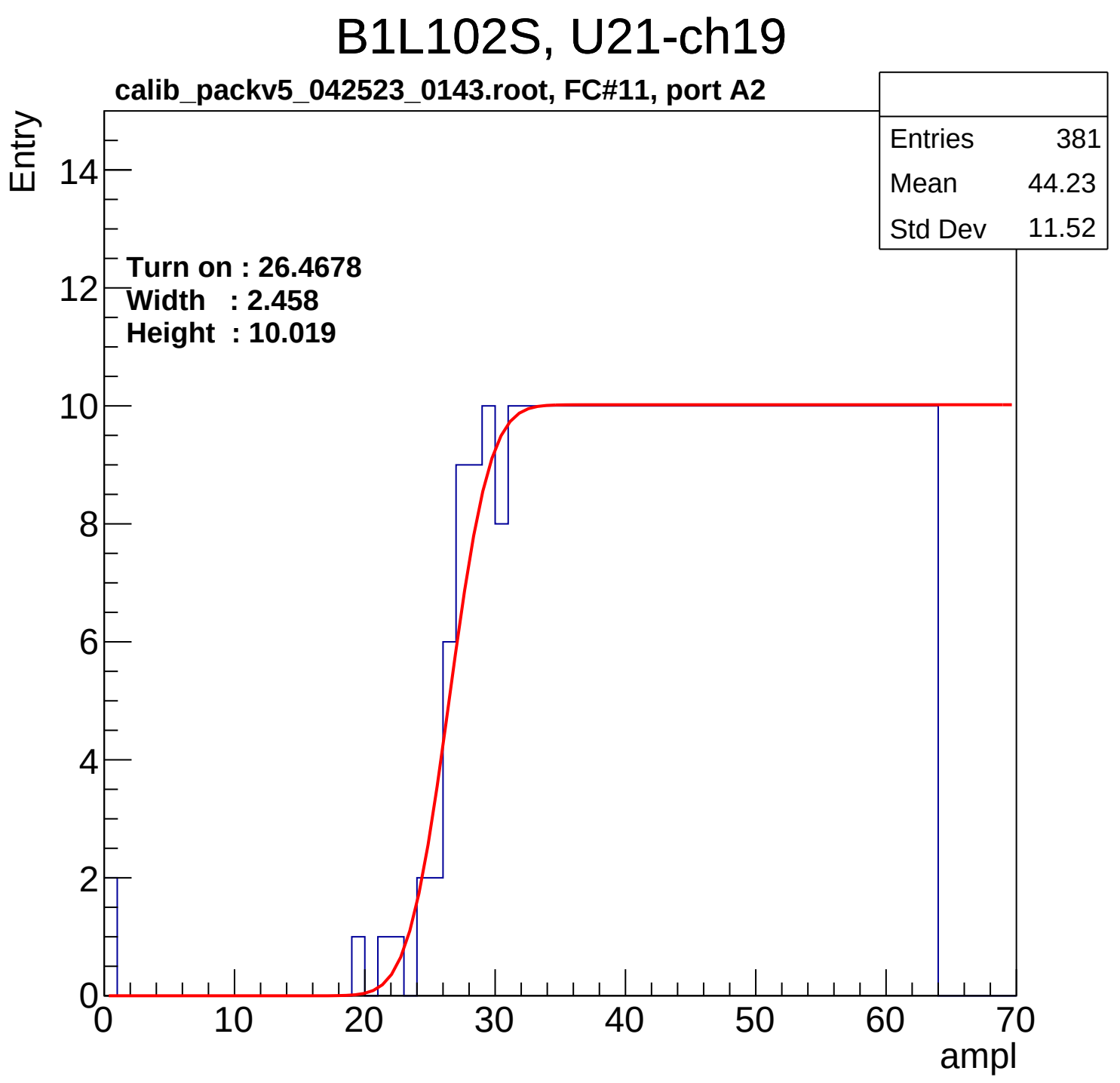
B1L102S, U21-ch19
calib_packv5_042523_0143.root, FC#11, port A2
Entries 381
Mean 44.23
Std Dev 11.52
Turn on : 26.4678
Width : 2.458
Height : 10.019
Entry
ampl
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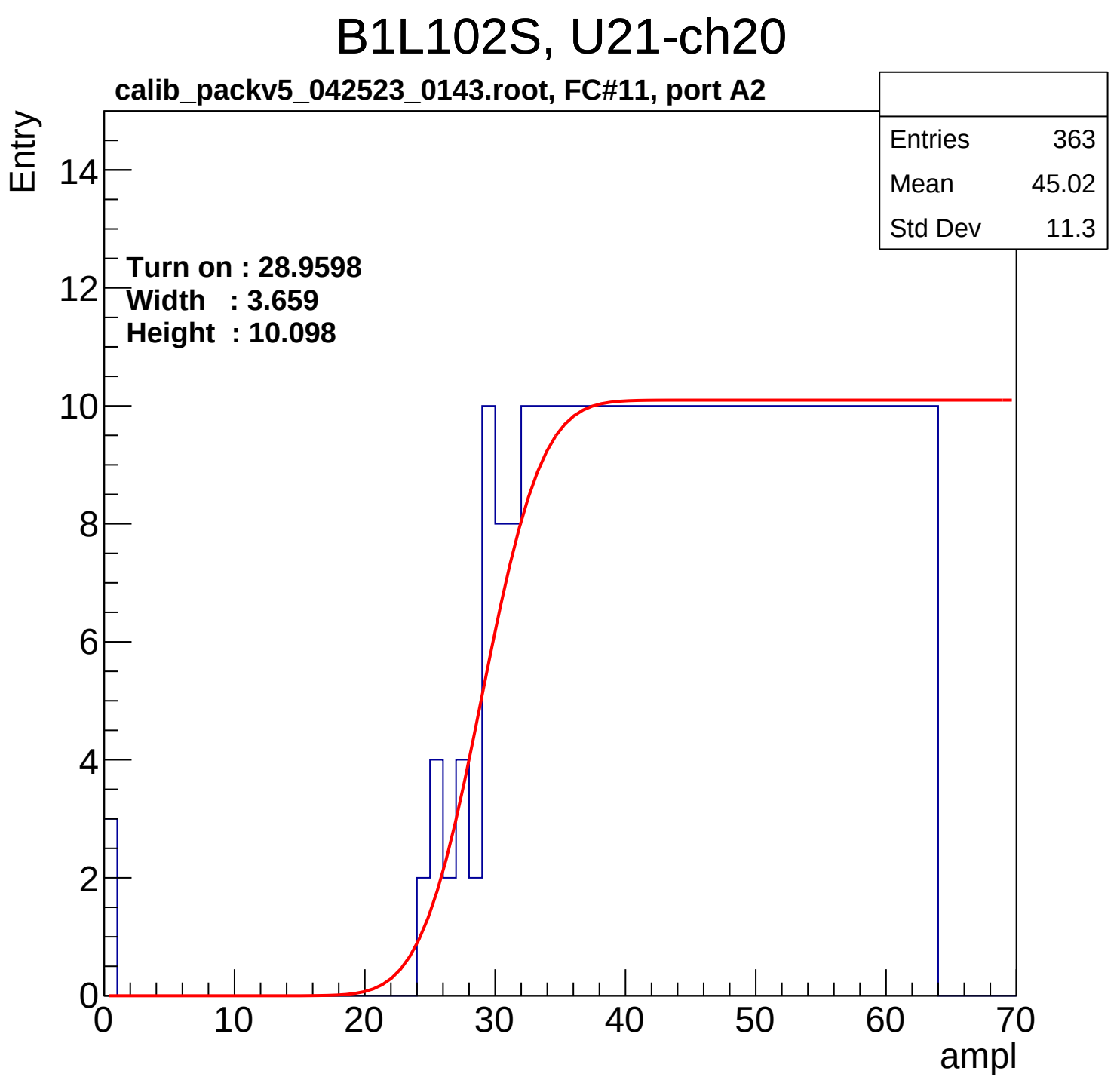
B1L102S, U21-ch20
calib_packv5_042523_0143.root, FC#11, port A2
Entries 363
Mean 45.02
Std Dev 11.3
Turn on : 28.9598
Width : 3.659
Height : 10.098
Entry
ampl
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8
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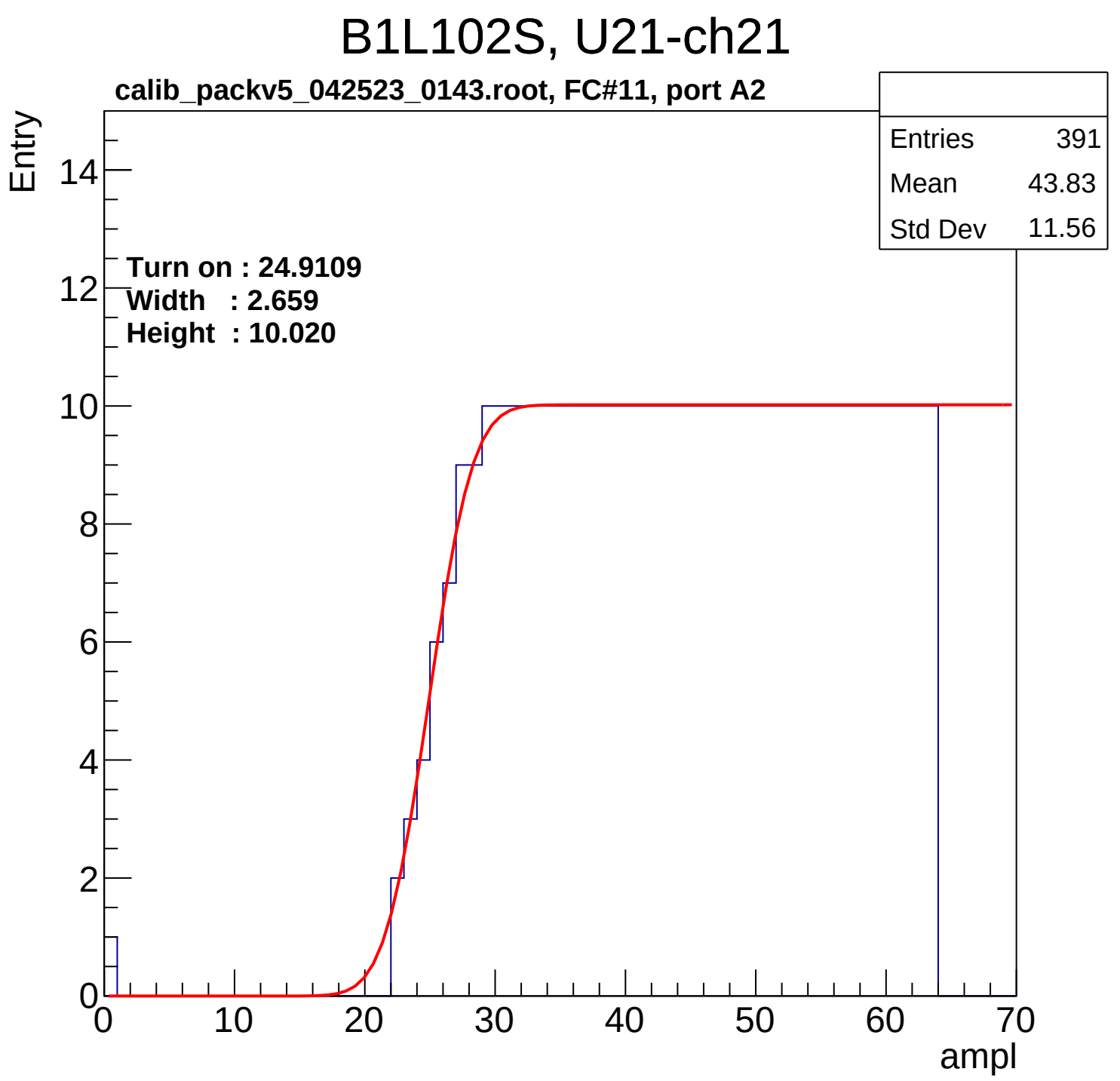
B1L102S, U21-ch21
calib_packv5_042523_0143.root, FC#11, port A2
Entries 391
Mean 43.83
Std Dev 11.56
Turn on : 24.9109
Width : 2.659
Height : 10.020
Entry
ampl
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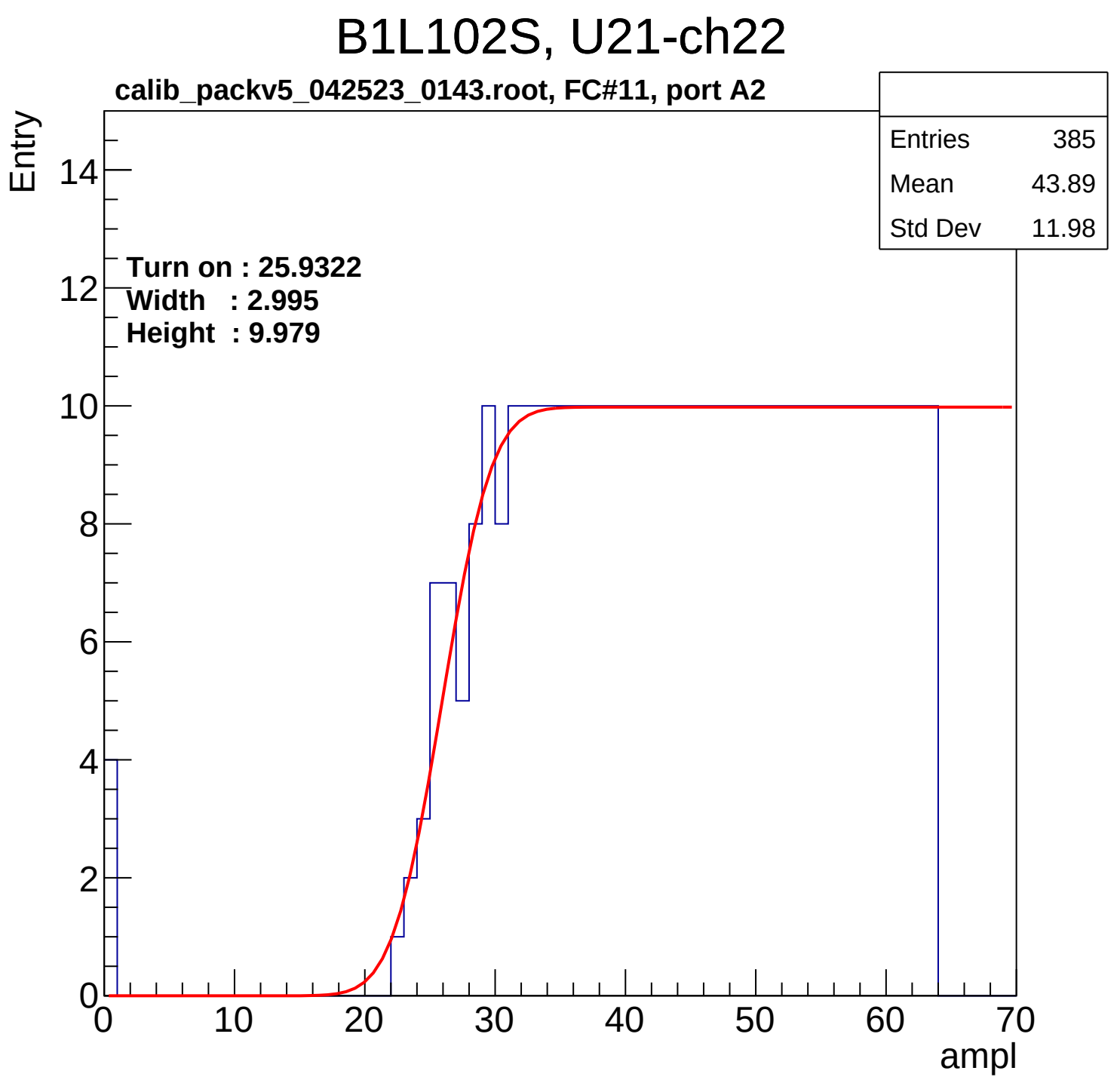
B1L102S, U21-ch22
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 43.89
Std Dev 11.98
Turn on : 25.9322
Width : 2.995
Height : 9.979
Entry
ampl
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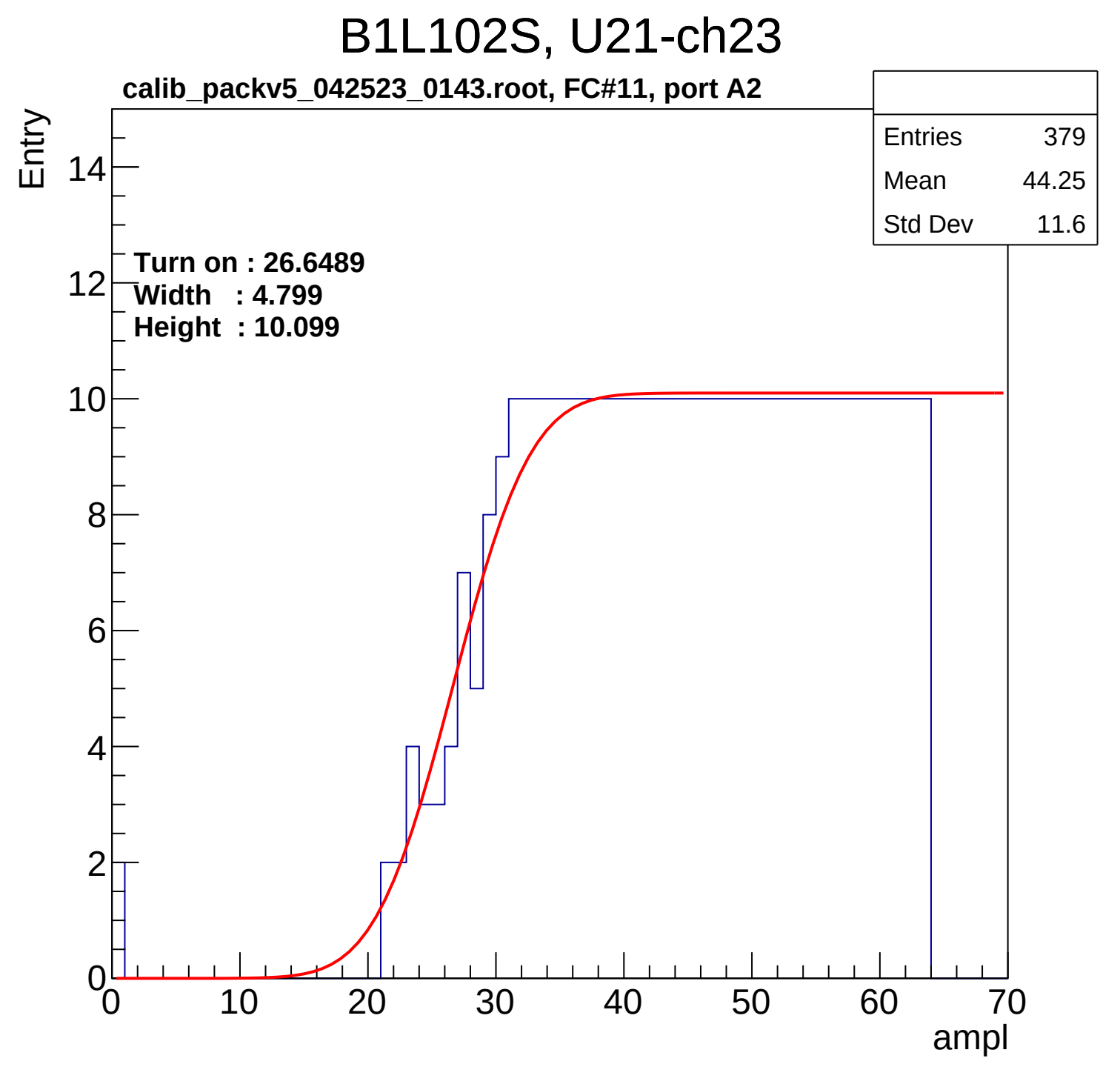
B1L102S, U21-ch23
calib_packv5_042523_0143.root, FC#11, port A2
Entries 379
Mean 44.25
Std Dev 11.6
Turn on : 26.6489
Width : 4.799
Height : 10.099
Entry
ampl
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6
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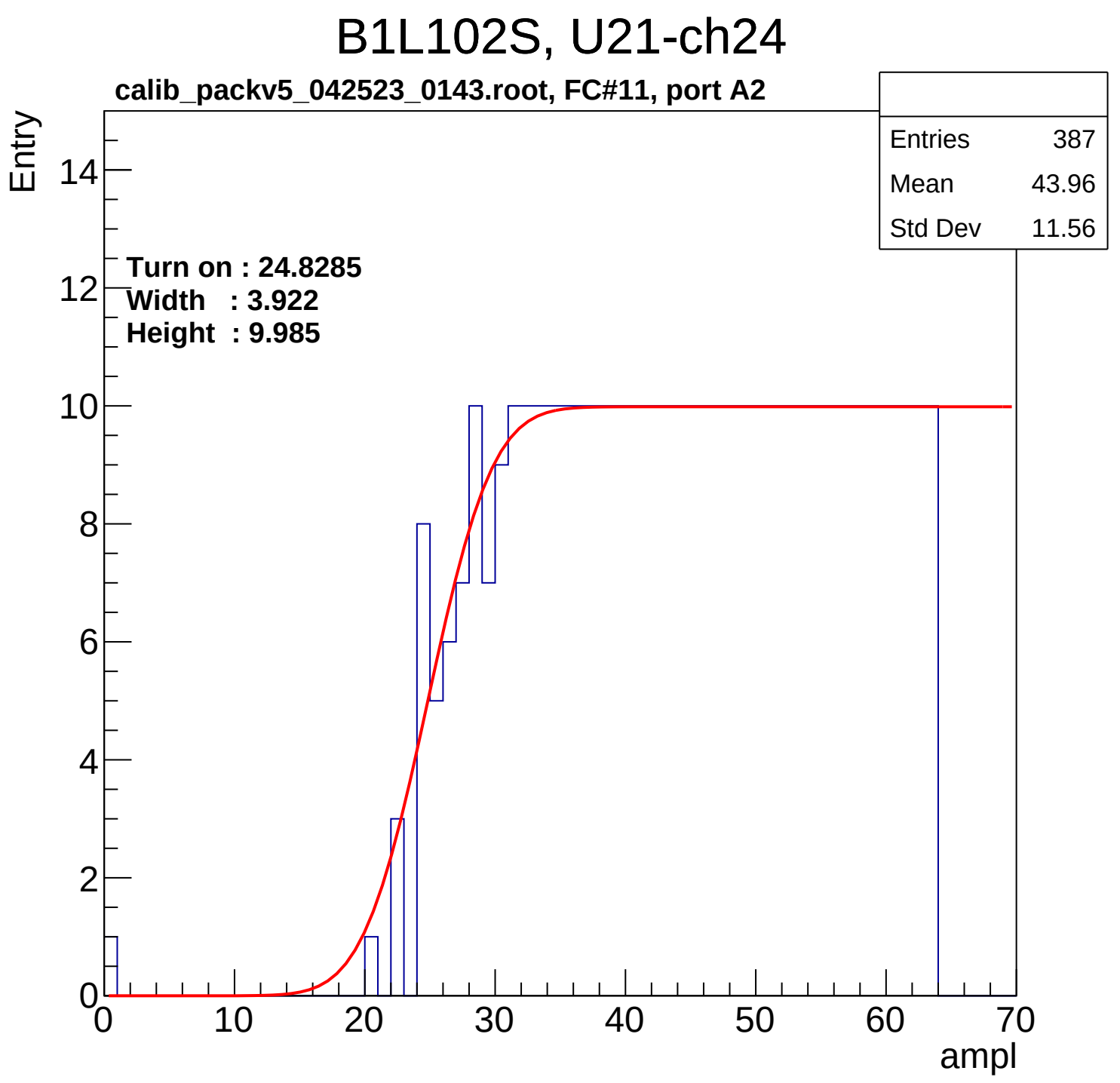
B1L102S, U21-ch24
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 43.96
Std Dev 11.56
Turn on : 24.8285
Width : 3.922
Height : 9.985
Entry
ampl
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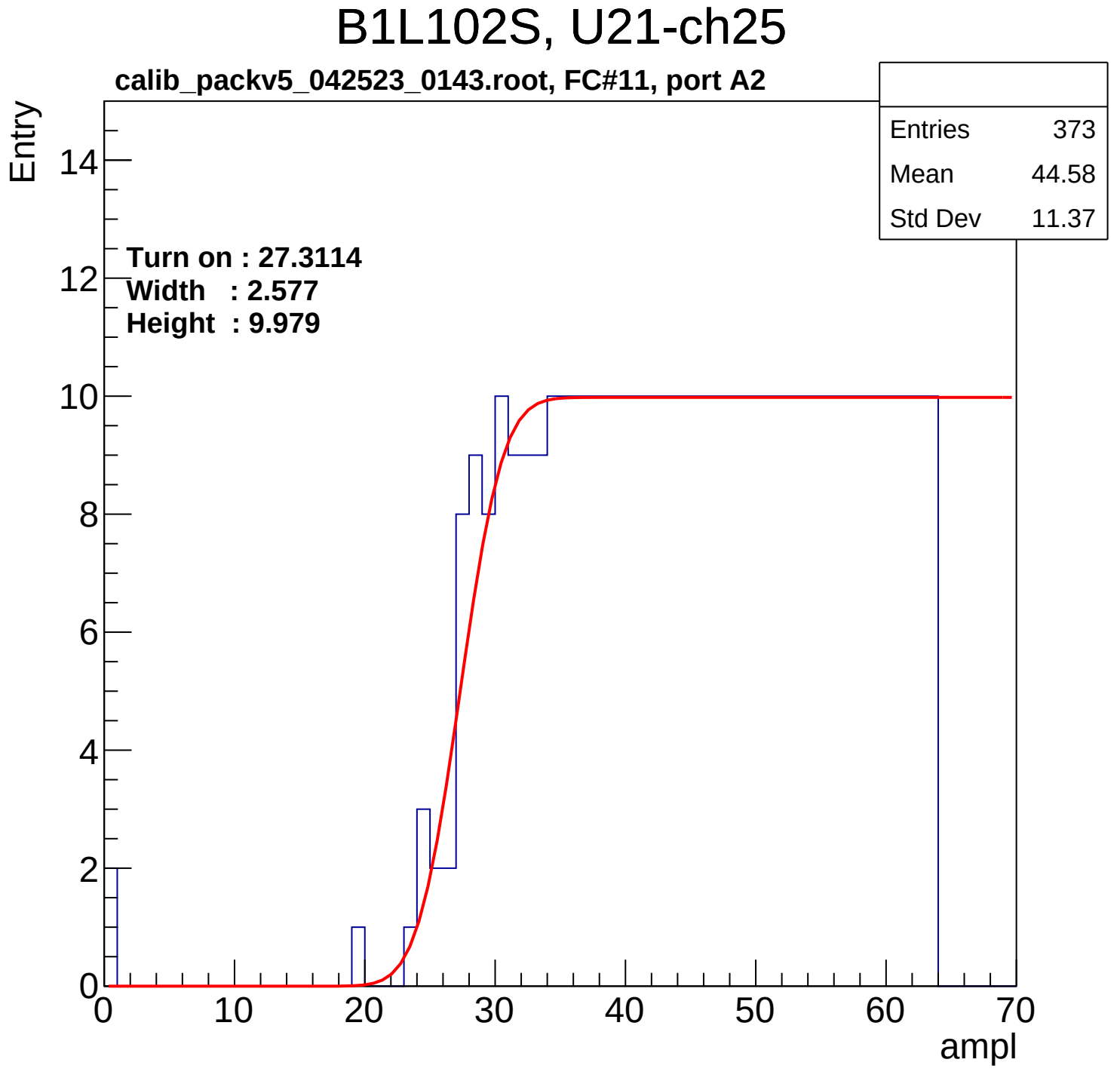
B1L102S, U21-ch25
calib_packv5_042523_0143.root, FC#11, port A2
Entries 373
Mean 44.58
Std Dev 11.37
Turn on : 27.3114
Width : 2.577
Height : 9.979
Entry
ampl
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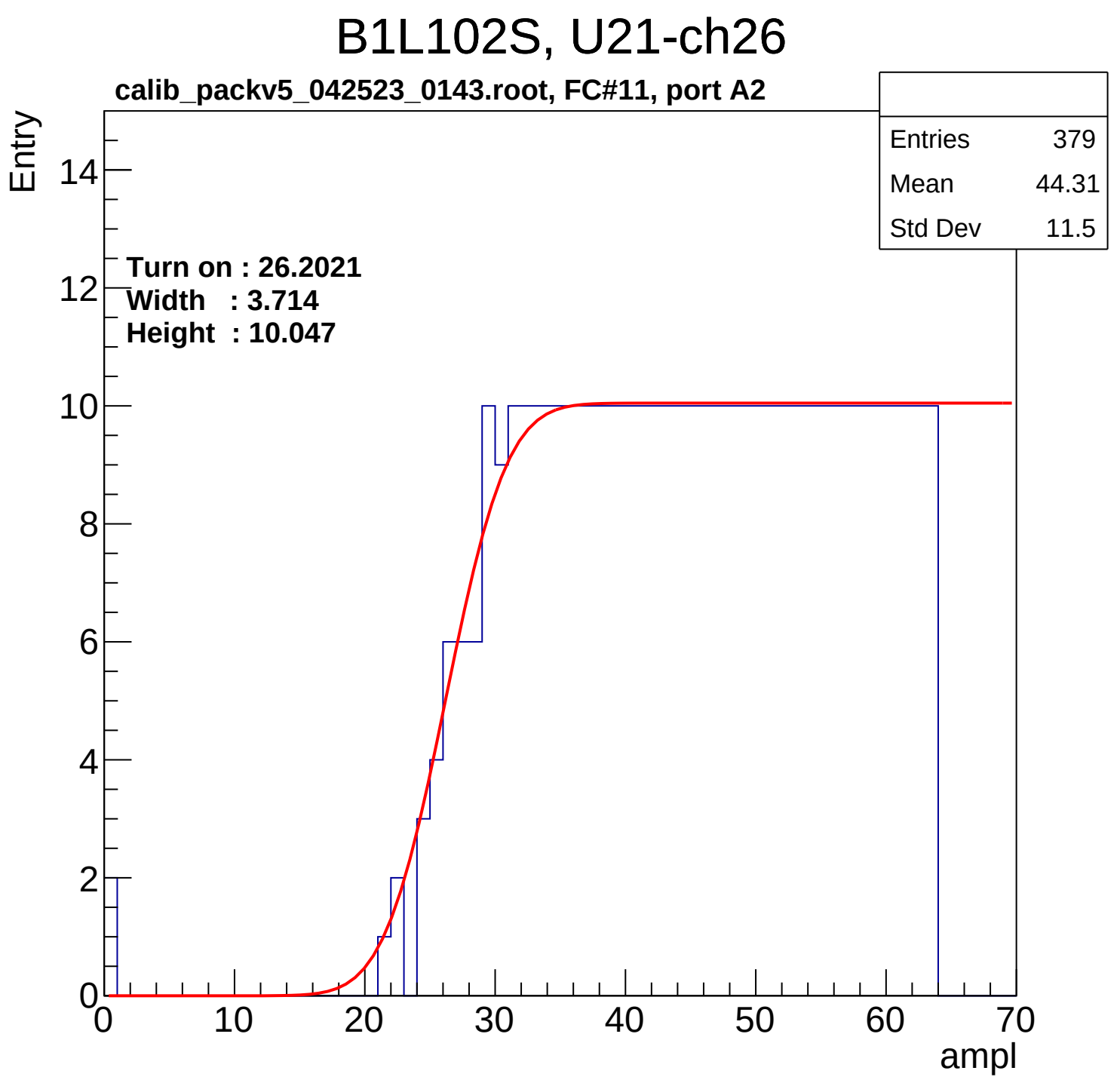
B1L102S, U21-ch26
calib_packv5_042523_0143.root, FC#11, port A2
Entries 379
Mean 44.31
Std Dev 11.5
Turn on : 26.2021
Width : 3.714
Height : 10.047
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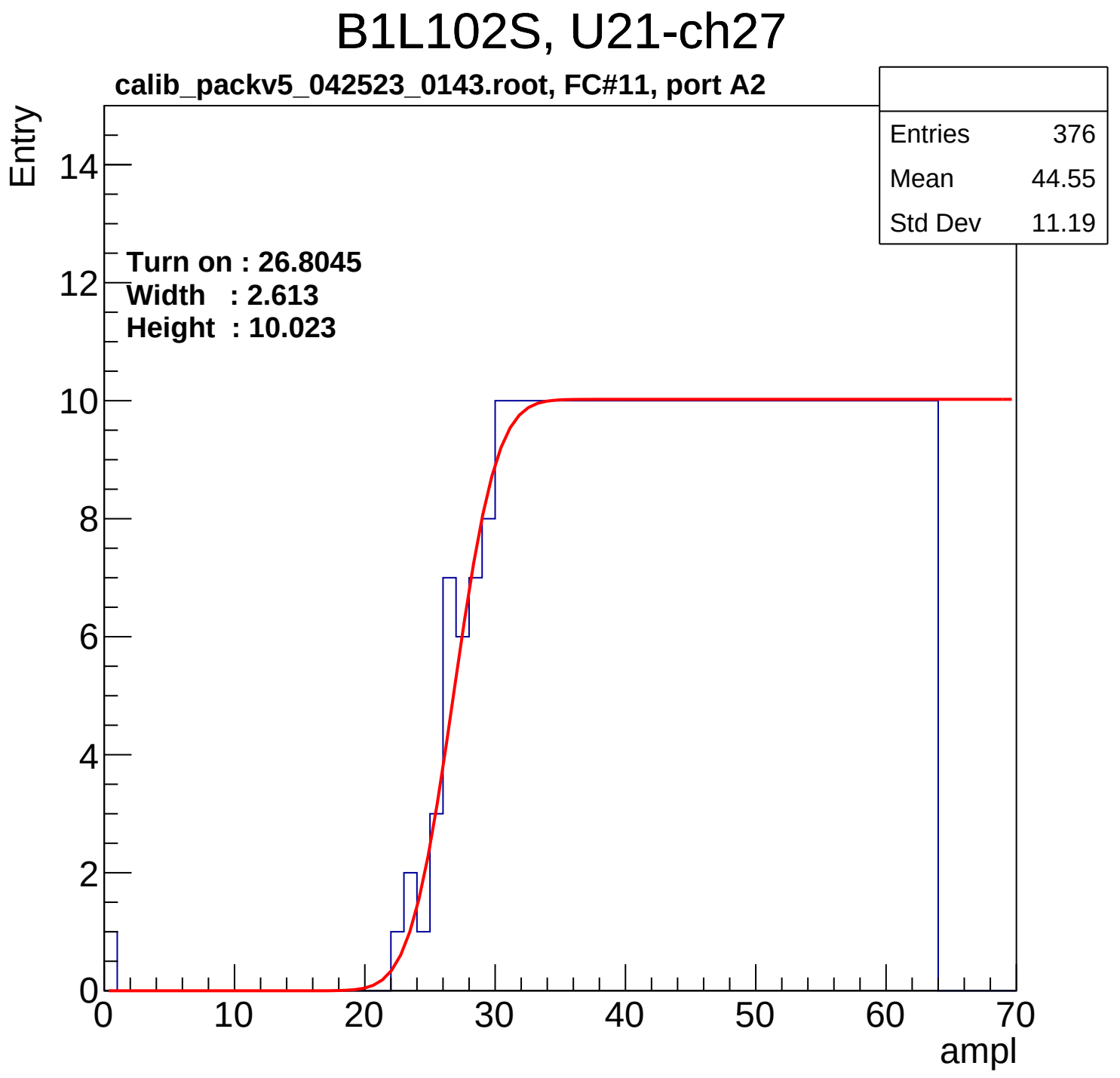
B1L102S, U21-ch27
calib_packv5_042523_0143.root, FC#11, port A2
Entries 376
Mean 44.55
Std Dev 11.19
Turn on : 26.8045
Width : 2.613
Height : 10.023
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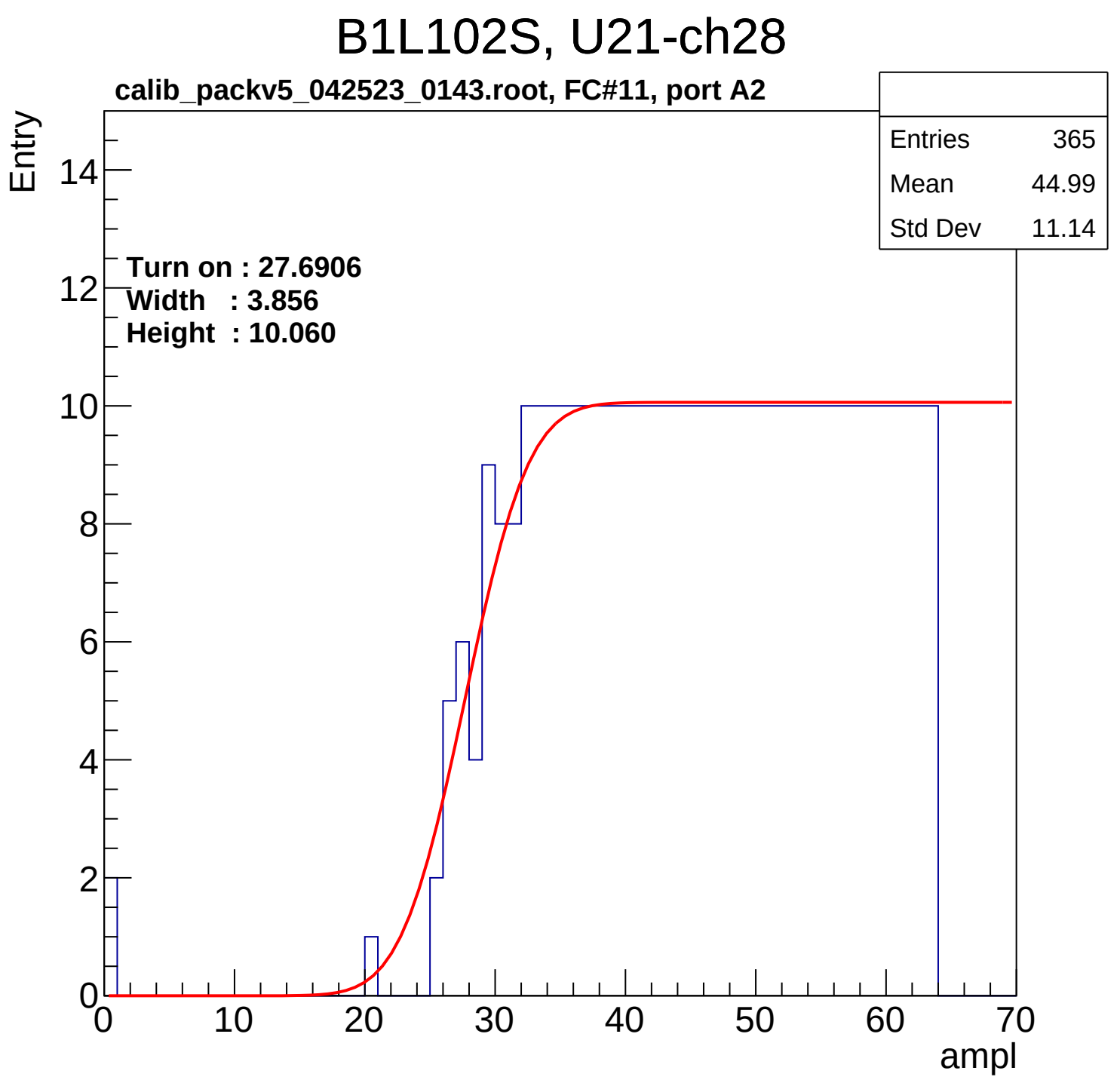
B1L102S, U21-ch28
calib_packv5_042523_0143.root, FC#11, port A2
Entries 365
Mean 44.99
Std Dev 11.14
Turn on : 27.6906
Width : 3.856
Height : 10.060
Entry
ampl
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4
6
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12
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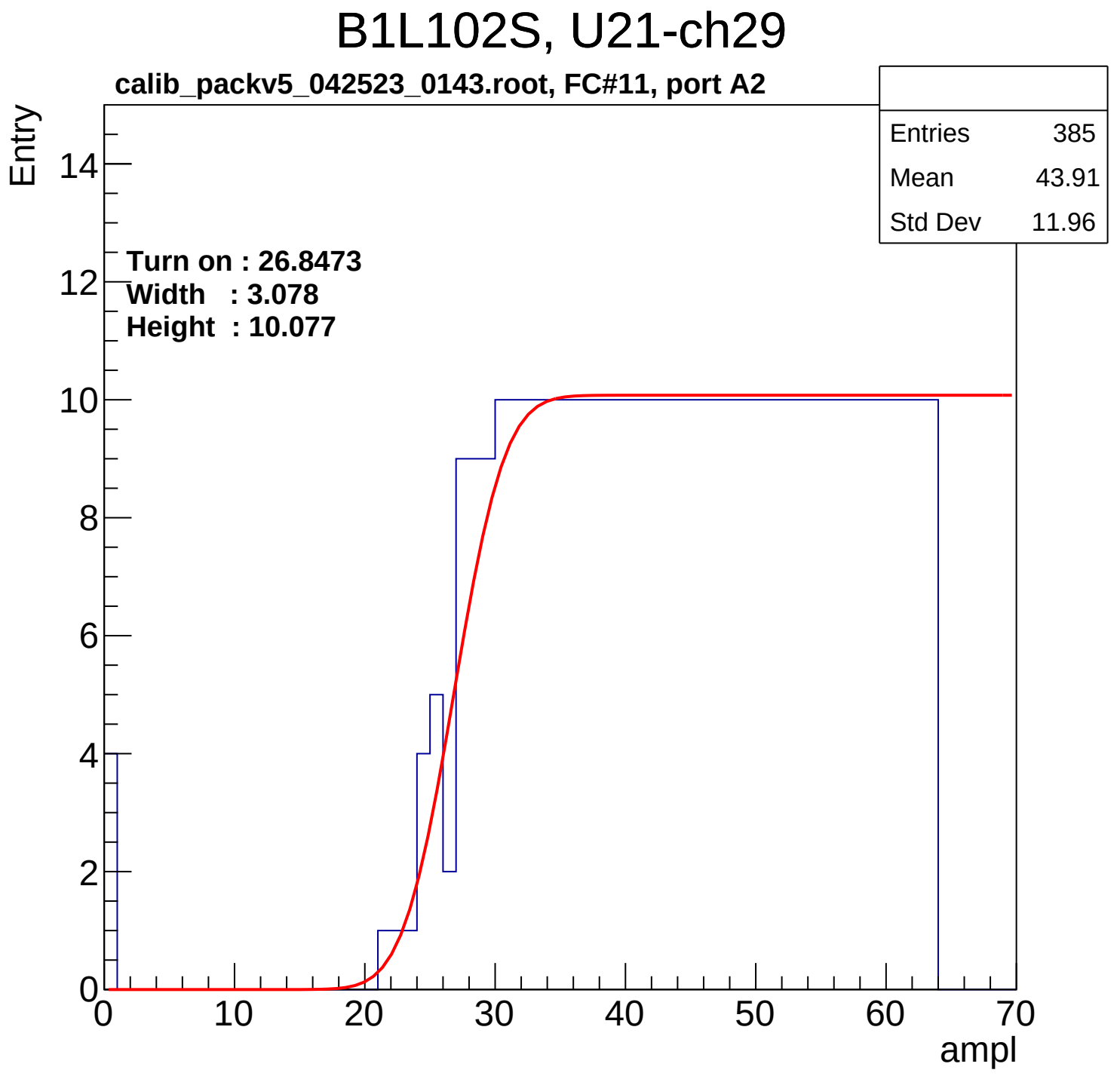
B1L102S, U21-ch29
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 43.91
Std Dev 11.96
Turn on : 26.8473
Width : 3.078
Height : 10.077
Entry
ampl
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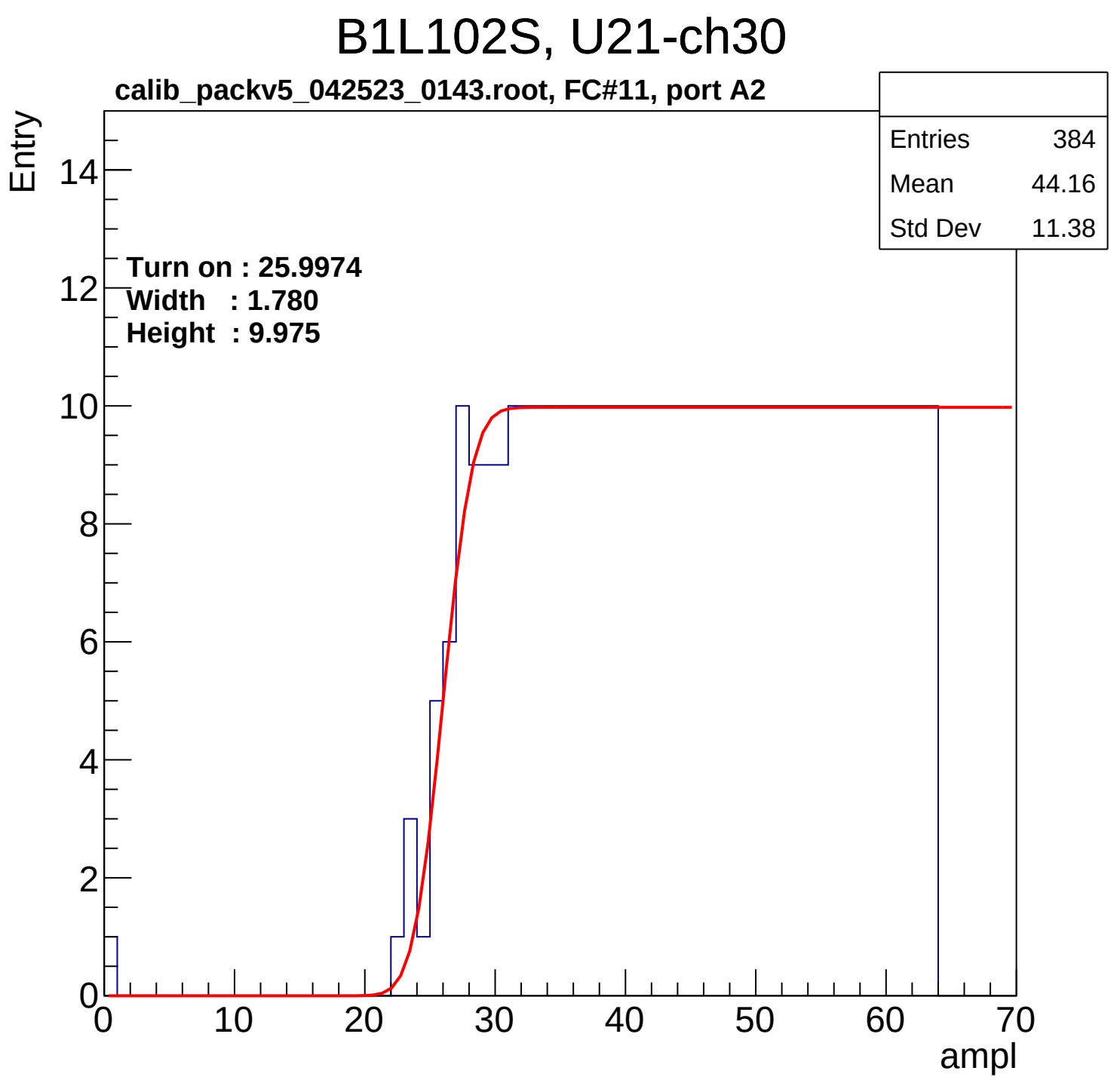
B1L102S, U21-ch30
calib_packv5_042523_0143.root, FC#11, port A2
Entries 384
Mean 44.16
Std Dev 11.38
Turn on : 25.9974
Width : 1.780
Height : 9.975
Entry
ampl
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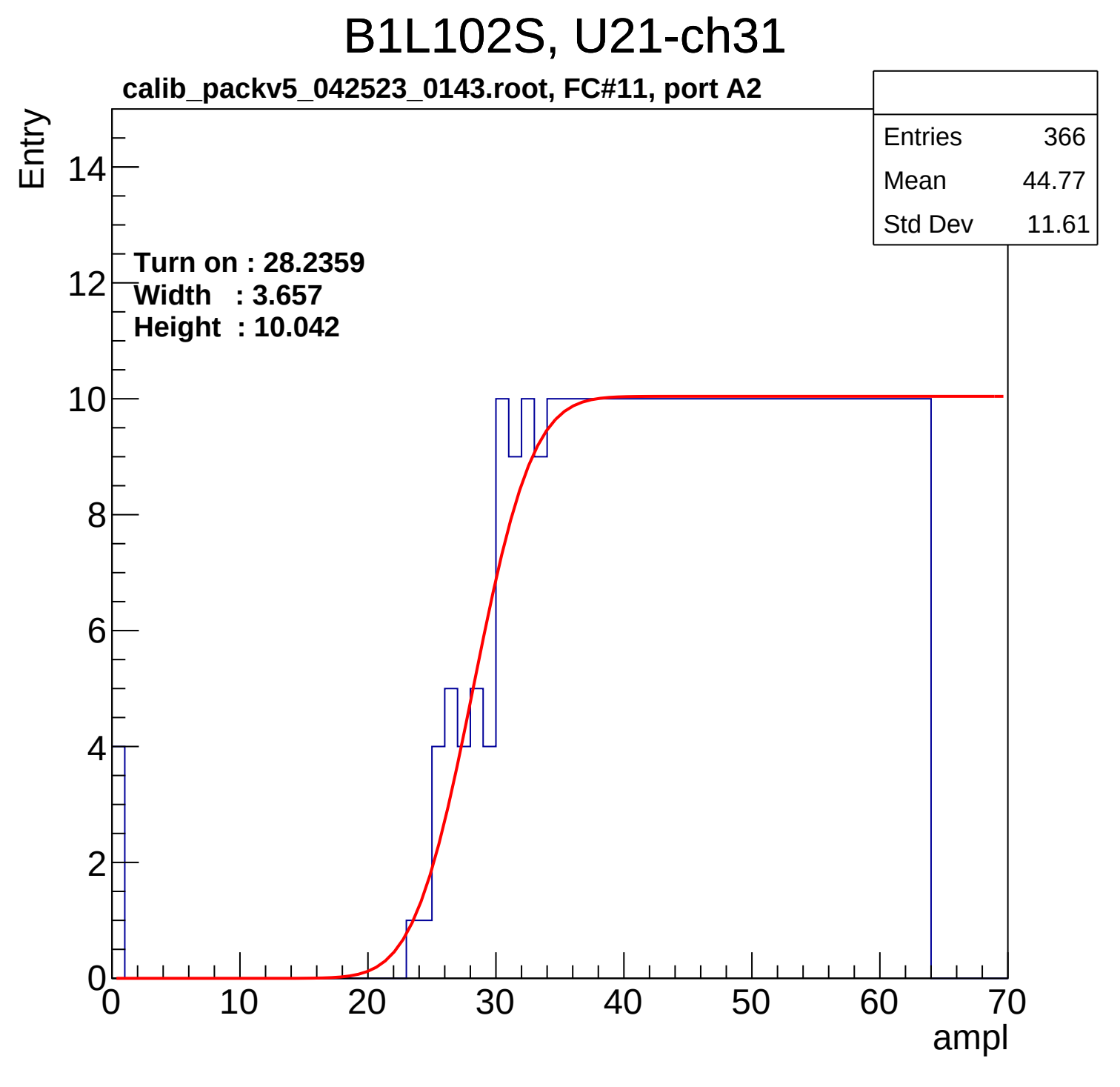
B1L102S, U21-ch31
calib_packv5_042523_0143.root, FC#11, port A2
Entries 366
Mean 44.77
Std Dev 11.61
Turn on : 28.2359
Width : 3.657
Height : 10.042
Entry
ampl
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4
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8
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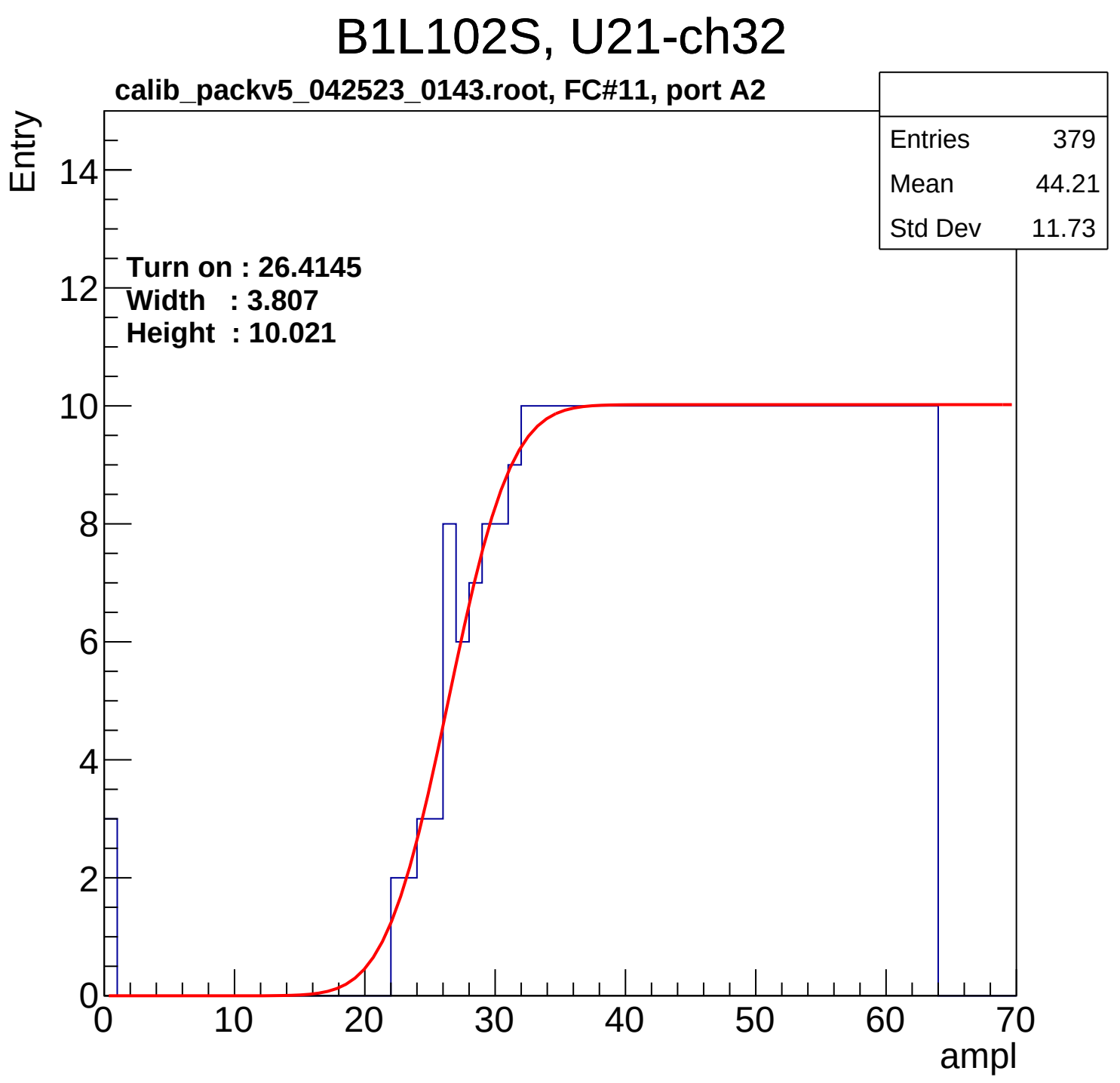
B1L102S, U21-ch32
calib_packv5_042523_0143.root, FC#11, port A2
Entries 379
Mean 44.21
Std Dev 11.73
Turn on : 26.4145
Width : 3.807
Height : 10.021
Entry
ampl
0
2
4
6
8
10
12
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0
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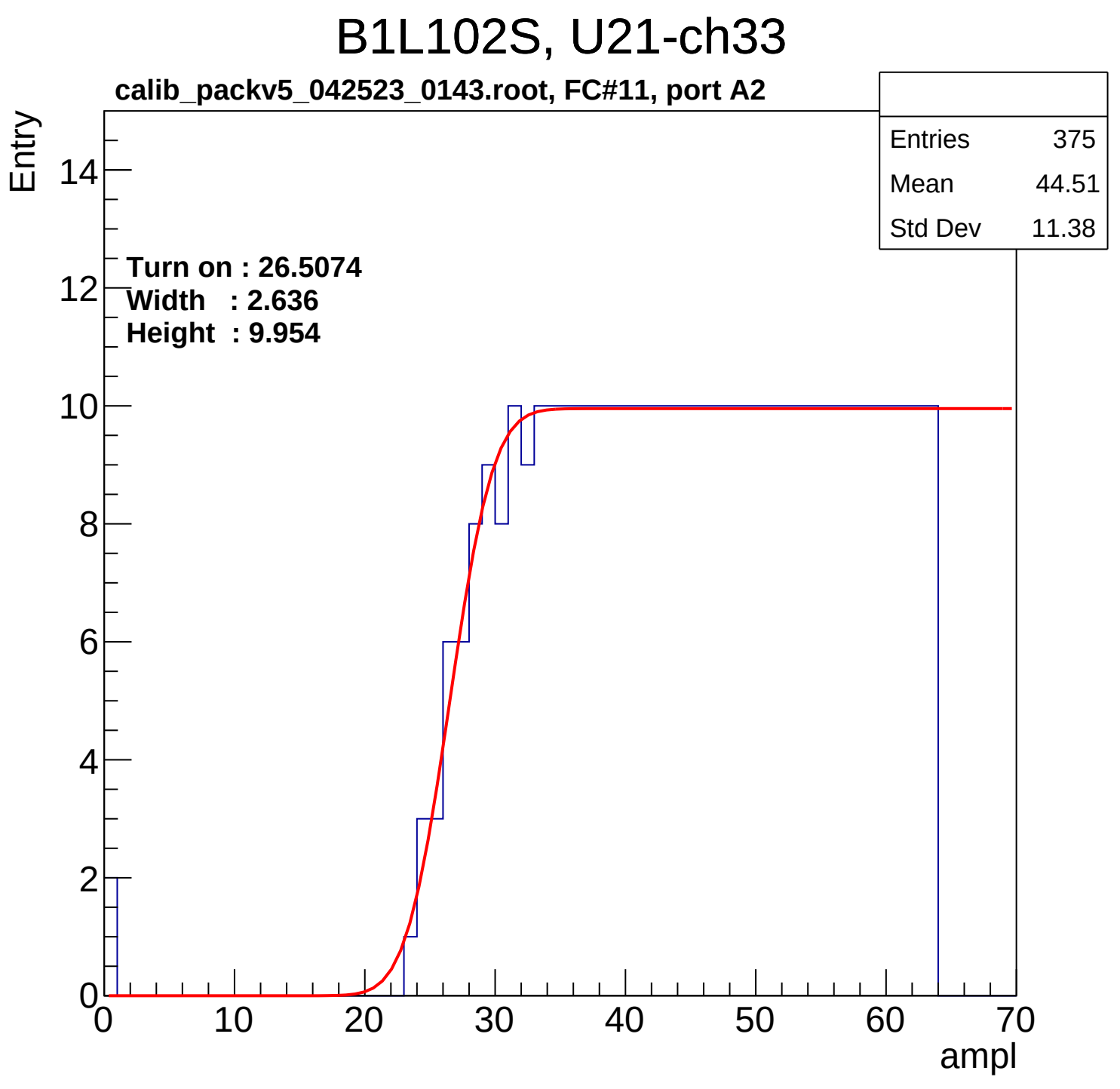
B1L102S, U21-ch33
calib_packv5_042523_0143.root, FC#11, port A2
Entries 375
Mean 44.51
Std Dev 11.38
Turn on : 26.5074
Width : 2.636
Height : 9.954
Entry
ampl
0
2
4
6
8
10
12
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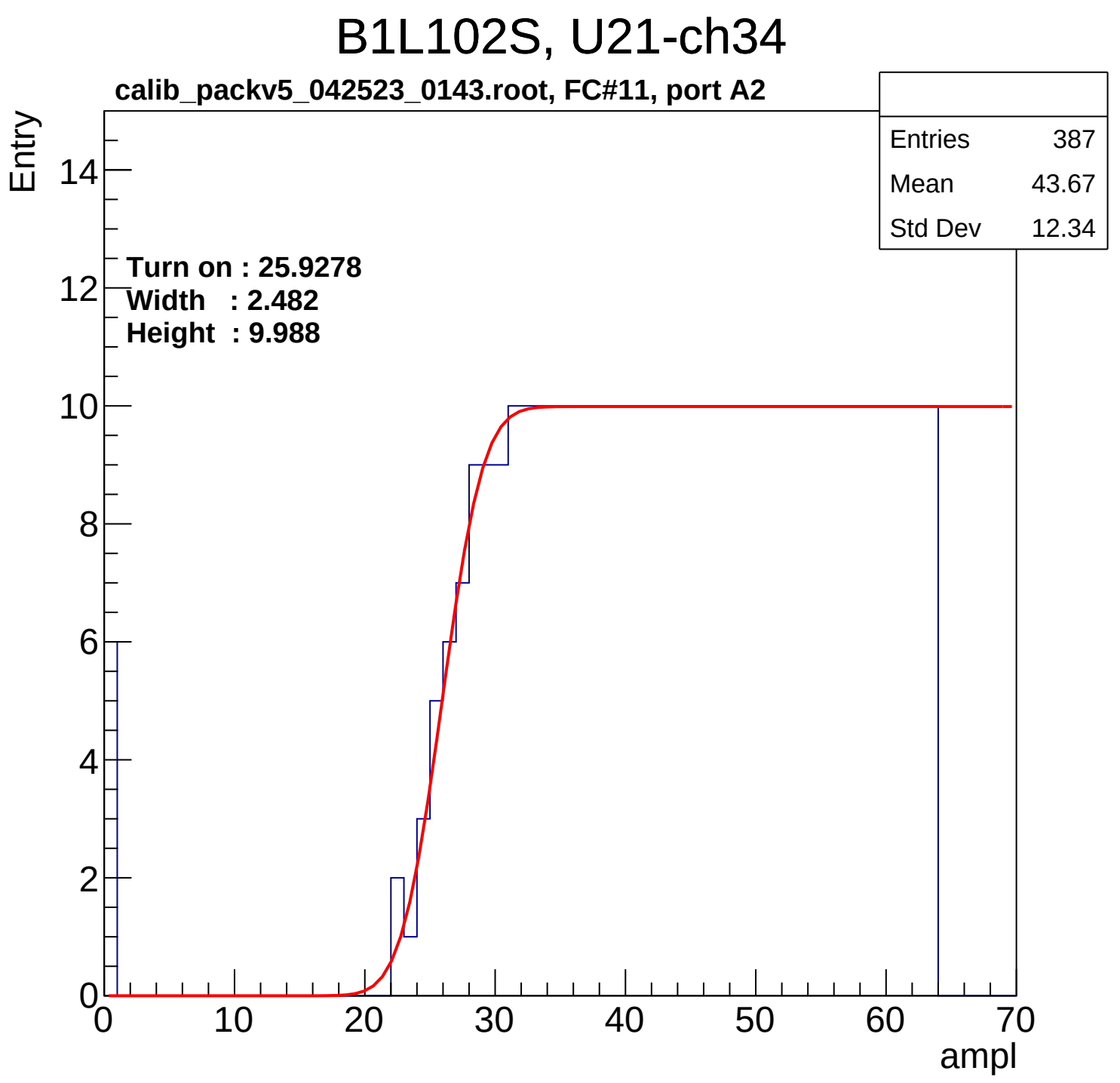
B1L102S, U21-ch34
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 43.67
Std Dev 12.34
Turn on : 25.9278
Width : 2.482
Height : 9.988
Entry
ampl
0
2
4
6
8
10
12
14
0
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60
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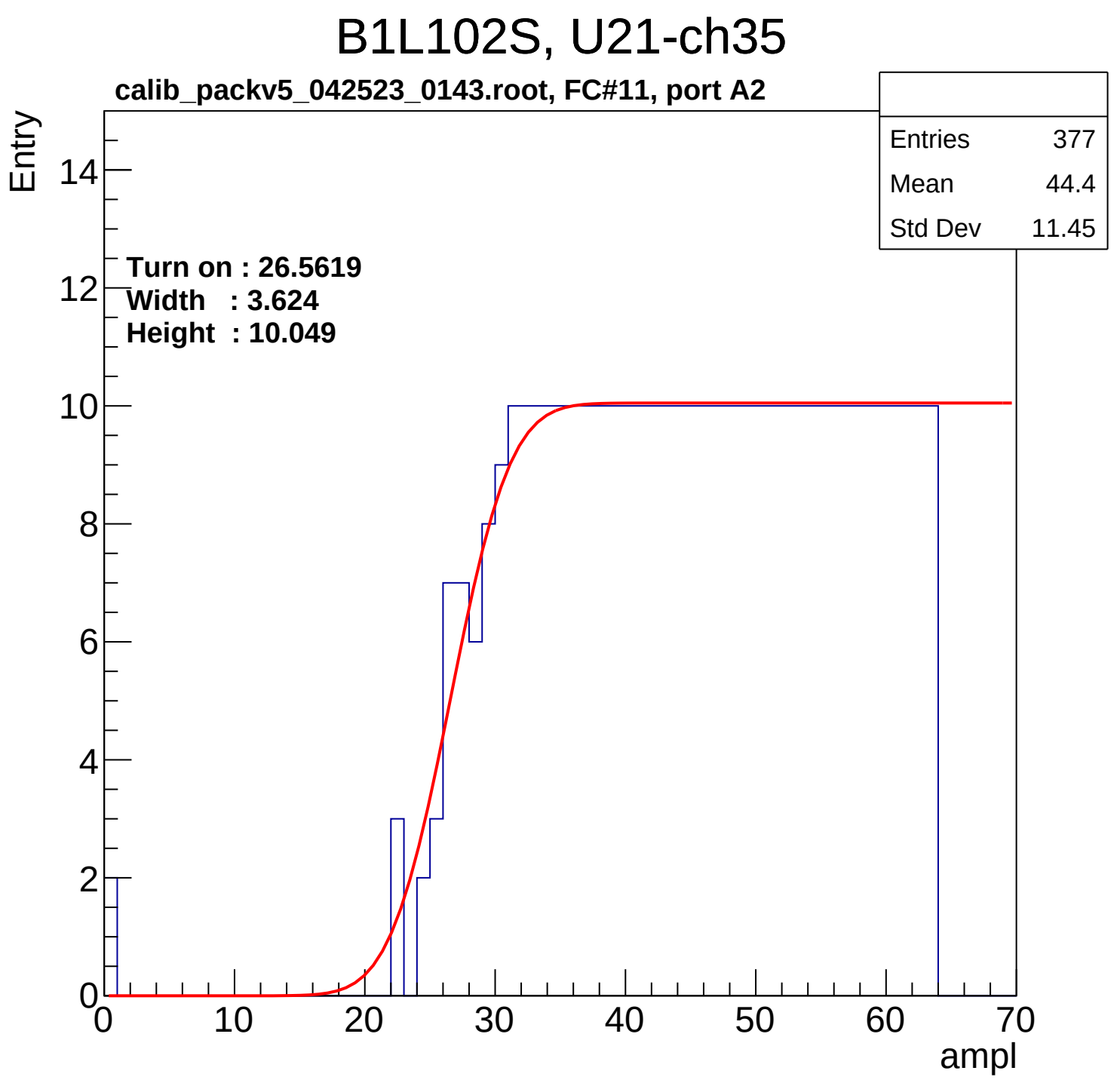
B1L102S, U21-ch35
calib_packv5_042523_0143.root, FC#11, port A2
Entries 377
Mean 44.4
Std Dev 11.45
Turn on : 26.5619
Width : 3.624
Height : 10.049
Entry
ampl
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4
6
8
10
12
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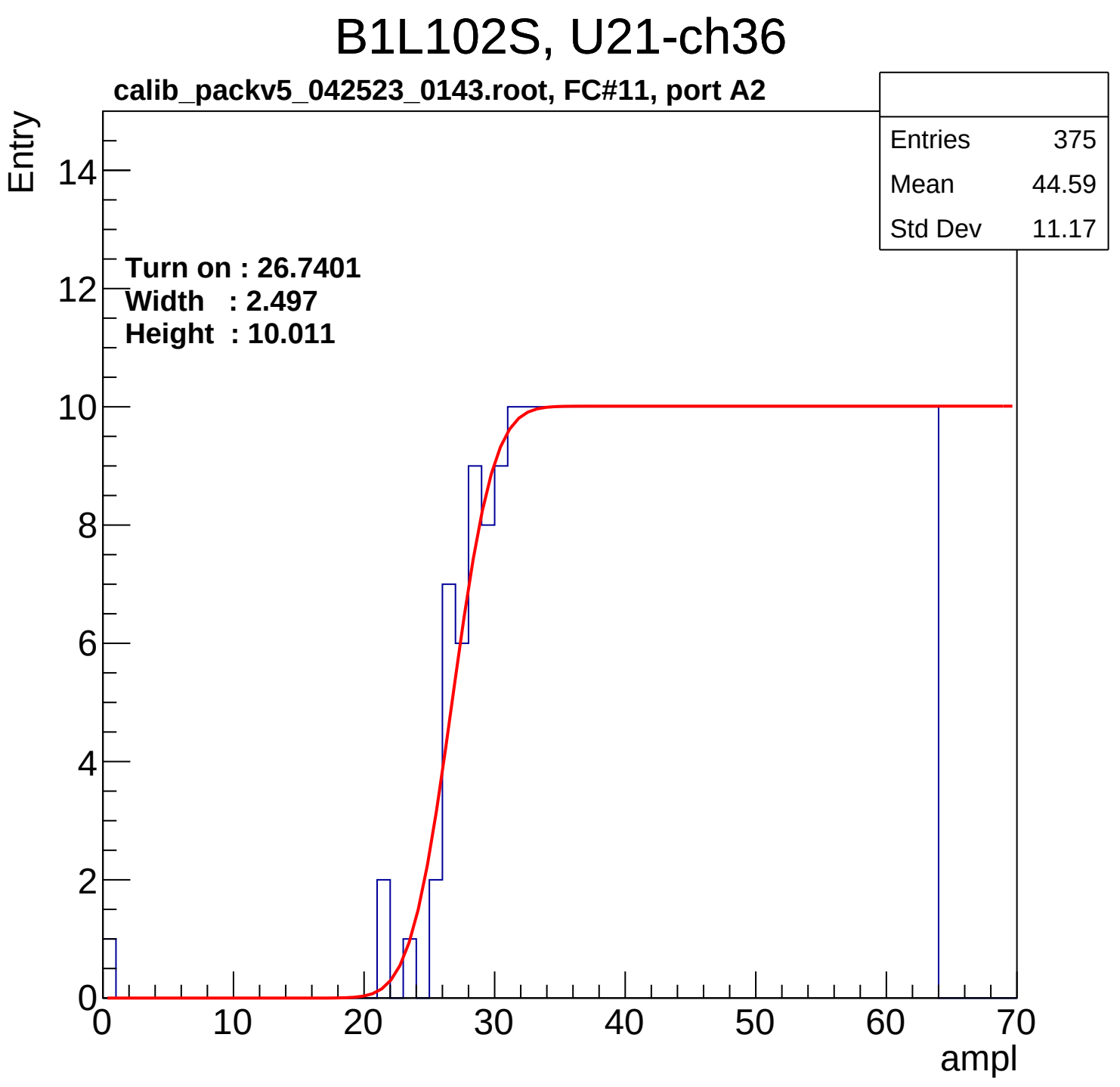
B1L102S, U21-ch36
calib_packv5_042523_0143.root, FC#11, port A2
Entries 375
Mean 44.59
Std Dev 11.17
Turn on : 26.7401
Width : 2.497
Height : 10.011
Entry
ampl
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2
4
6
8
10
12
14
0
10
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60
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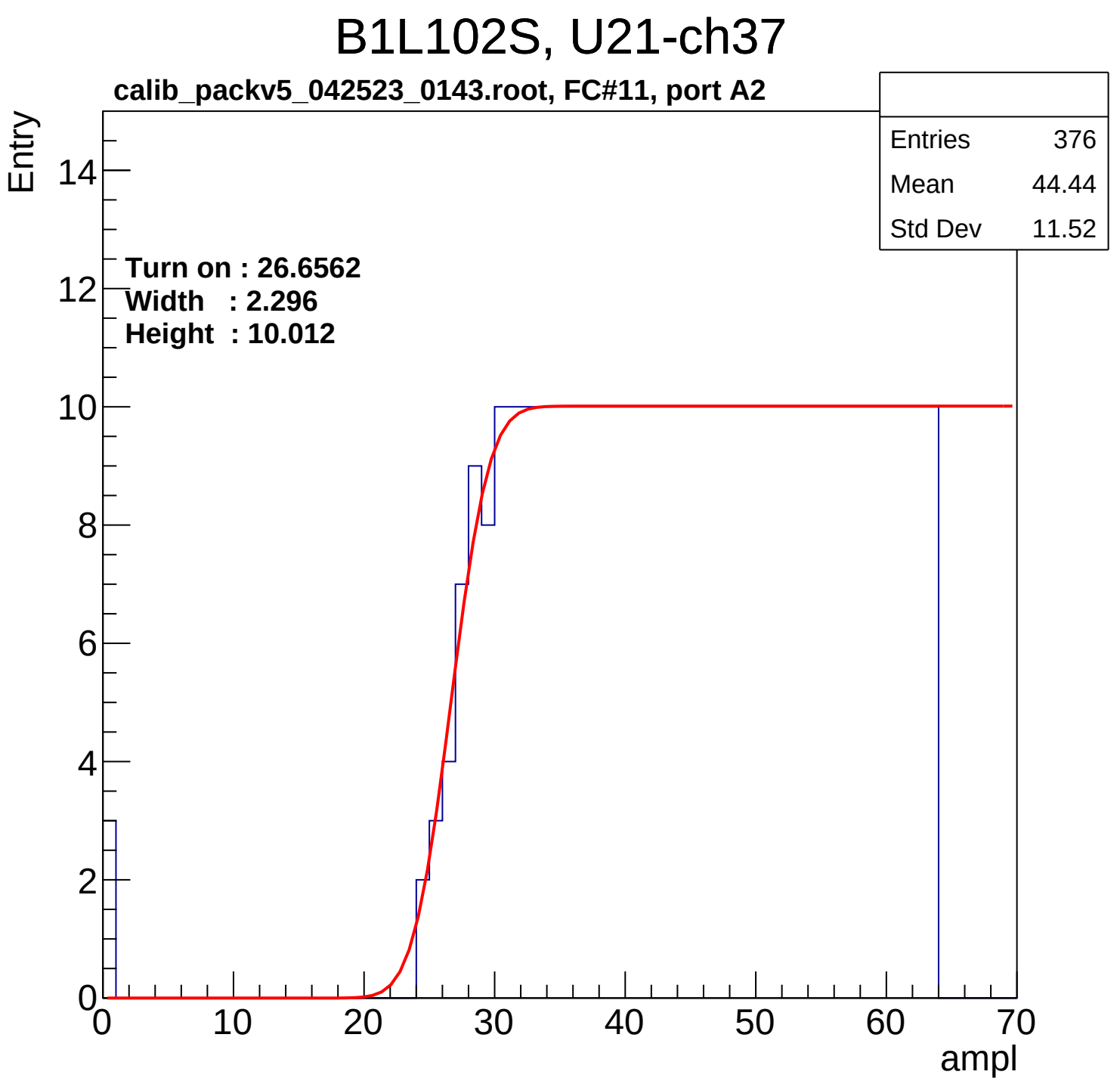
B1L102S, U21-ch37
calib_packv5_042523_0143.root, FC#11, port A2
Entries 376
Mean 44.44
Std Dev 11.52
Turn on : 26.6562
Width : 2.296
Height : 10.012
Entry
ampl
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4
6
8
10
12
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0
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60
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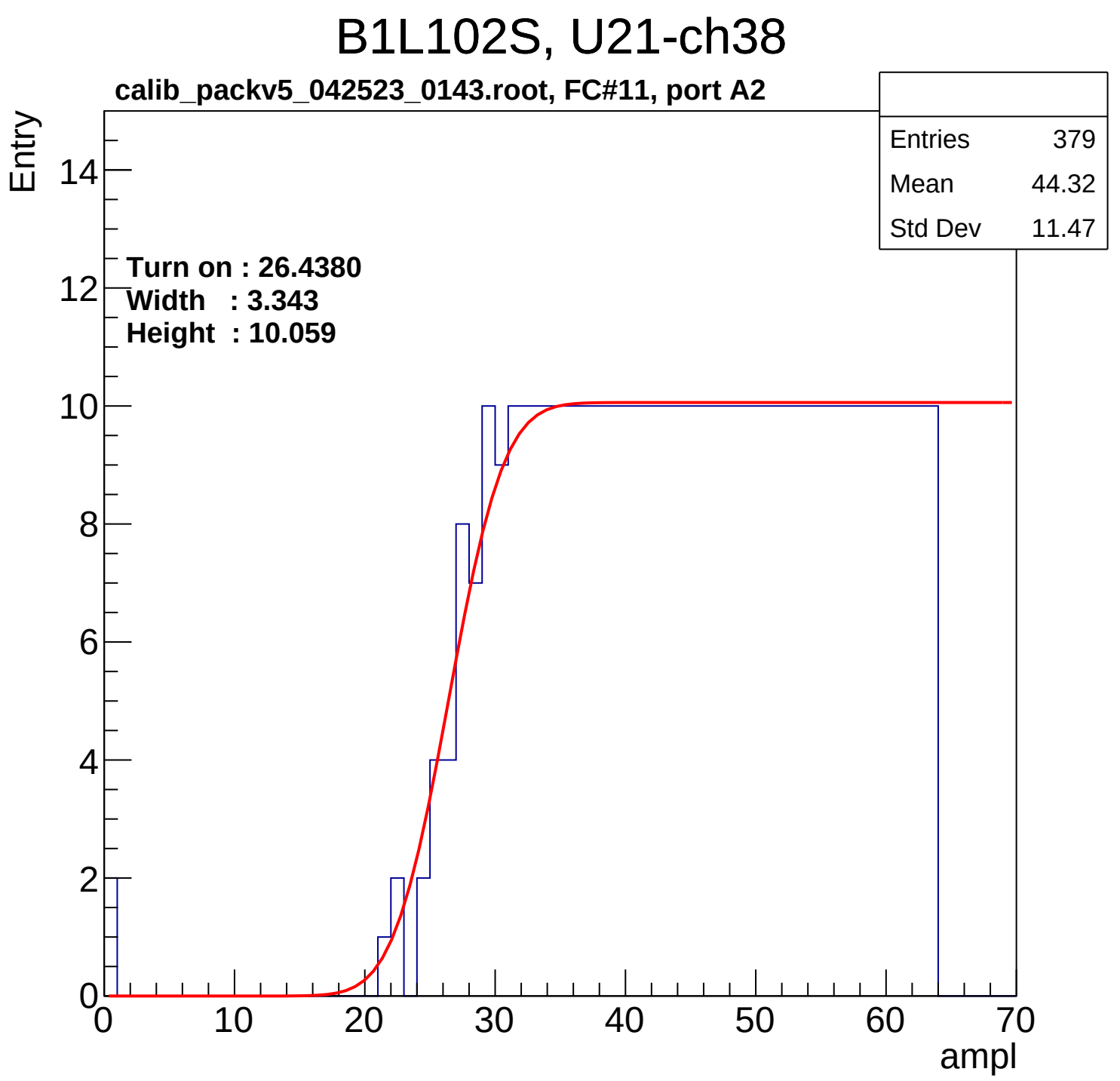
B1L102S, U21-ch38
calib_packv5_042523_0143.root, FC#11, port A2
Entries 379
Mean 44.32
Std Dev 11.47
Turn on : 26.4380
Width : 3.343
Height : 10.059
Entry
ampl
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2
4
6
8
10
12
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60
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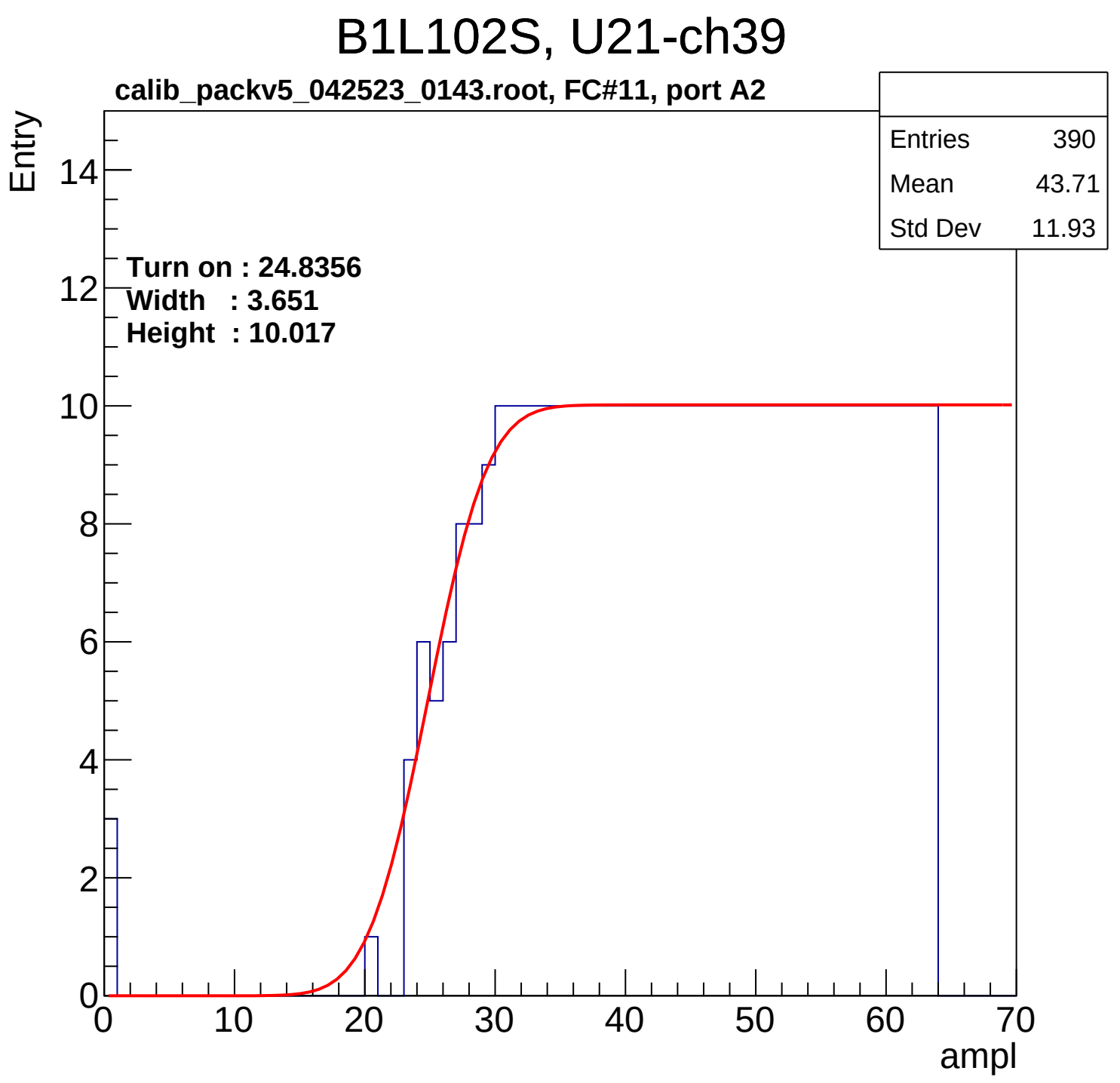
B1L102S, U21-ch39
calib_packv5_042523_0143.root, FC#11, port A2
Entries 390
Mean 43.71
Std Dev 11.93
Turn on : 24.8356
Width : 3.651
Height : 10.017
Entry
ampl
0
2
4
6
8
10
12
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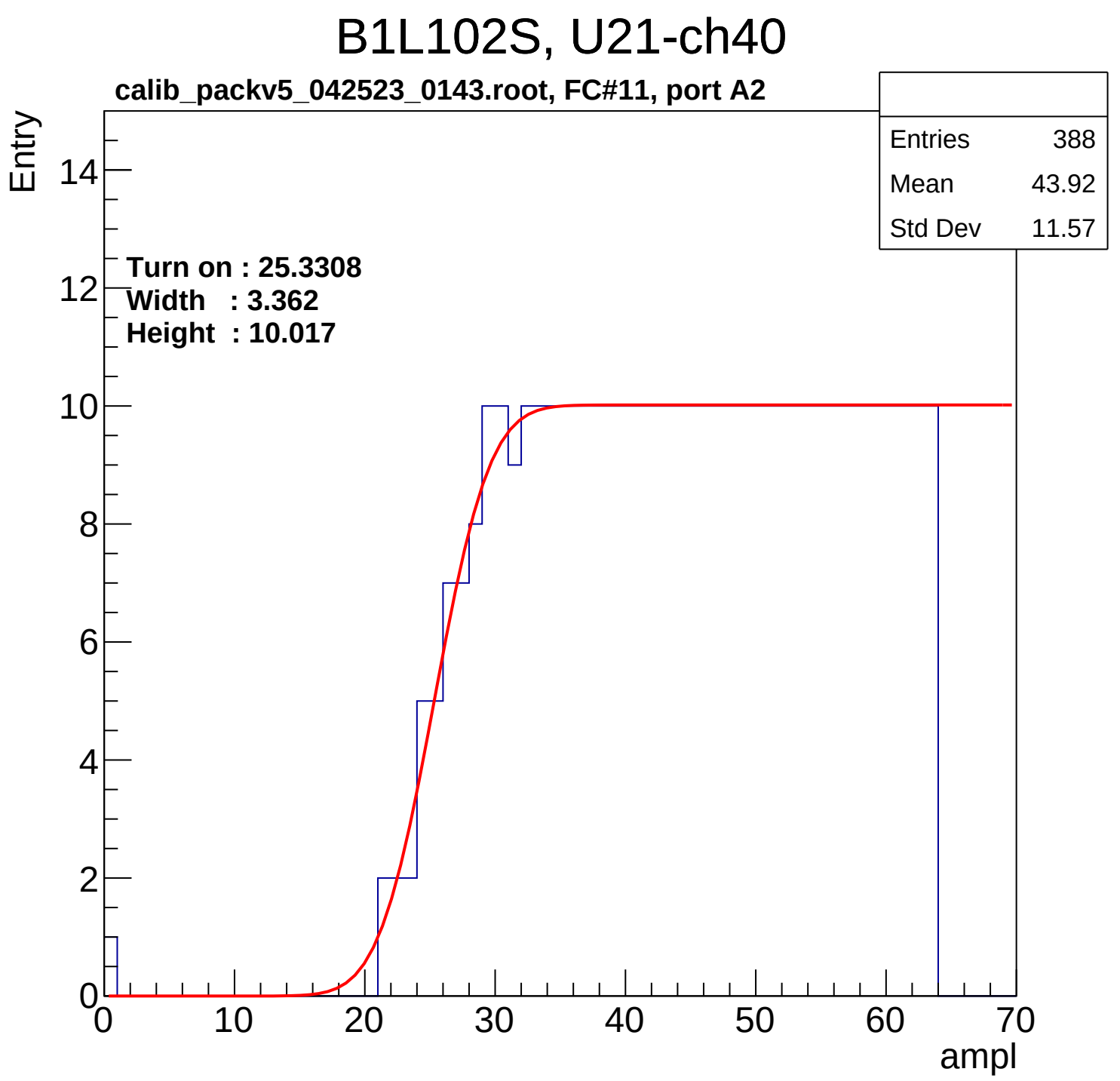
B1L102S, U21-ch40
calib_packv5_042523_0143.root, FC#11, port A2
Entries 388
Mean 43.92
Std Dev 11.57
Turn on : 25.3308
Width : 3.362
Height : 10.017
Entry
ampl
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4
6
8
10
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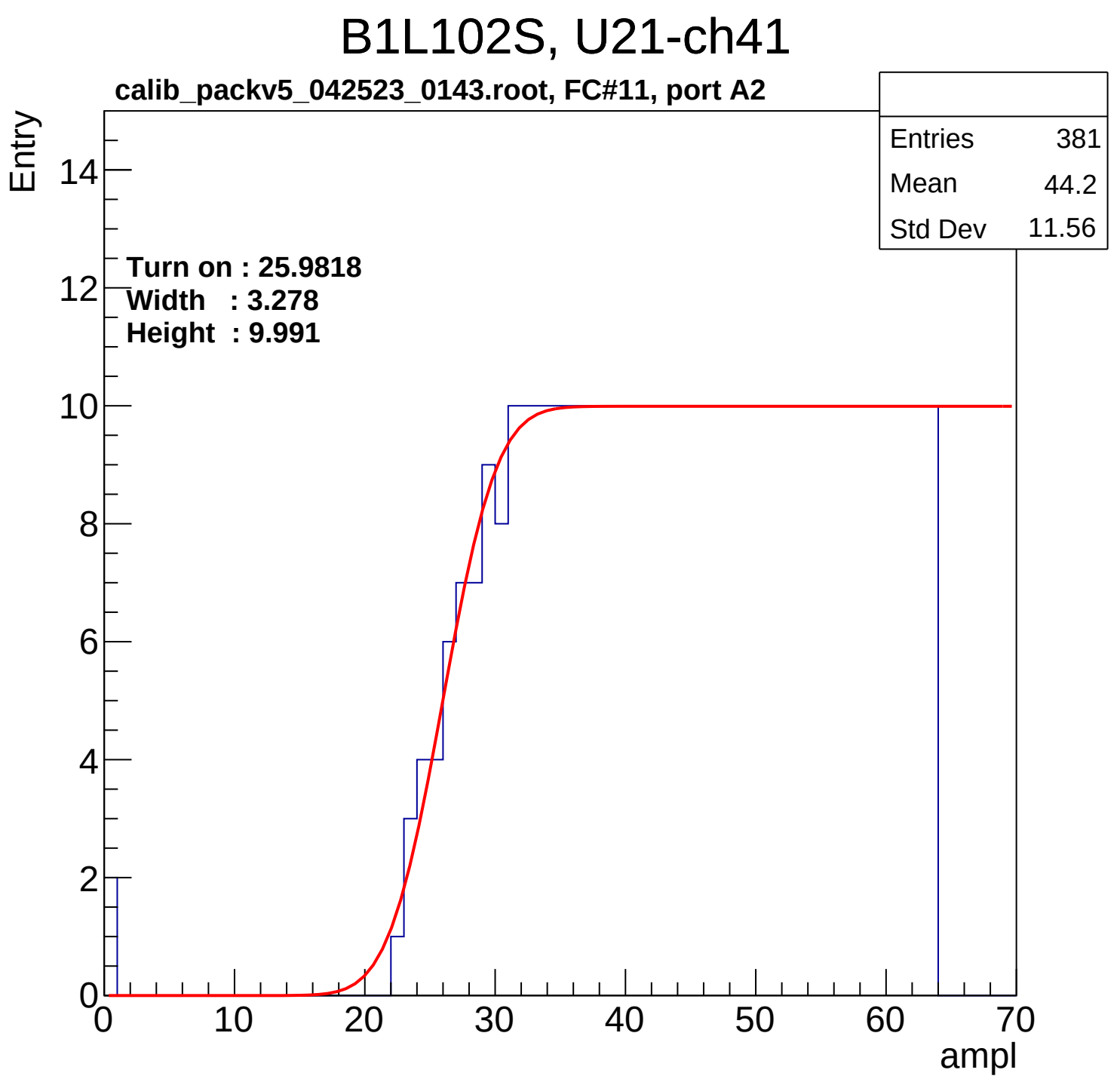
B1L102S, U21-ch41
calib_packv5_042523_0143.root, FC#11, port A2
Entries 381
Mean 44.2
Std Dev 11.56
Turn on : 25.9818
Width : 3.278
Height : 9.991
Entry
ampl
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6
8
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12
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20
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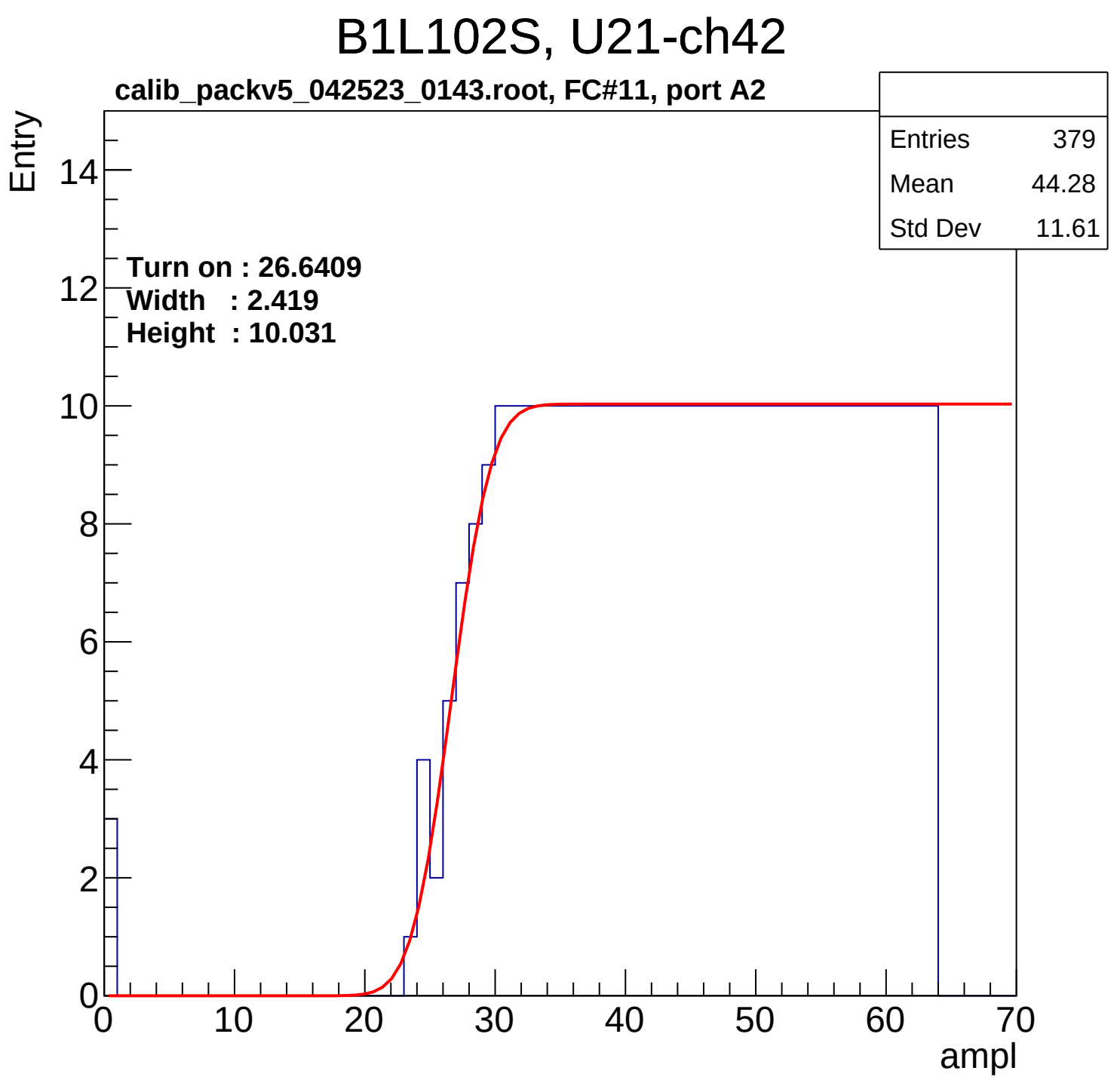
B1L102S, U21-ch42
calib_packv5_042523_0143.root, FC#11, port A2
Entries 379
Mean 44.28
Std Dev 11.61
Turn on : 26.6409
Width : 2.419
Height : 10.031
Entry
ampl
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2
4
6
8
10
12
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0
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20
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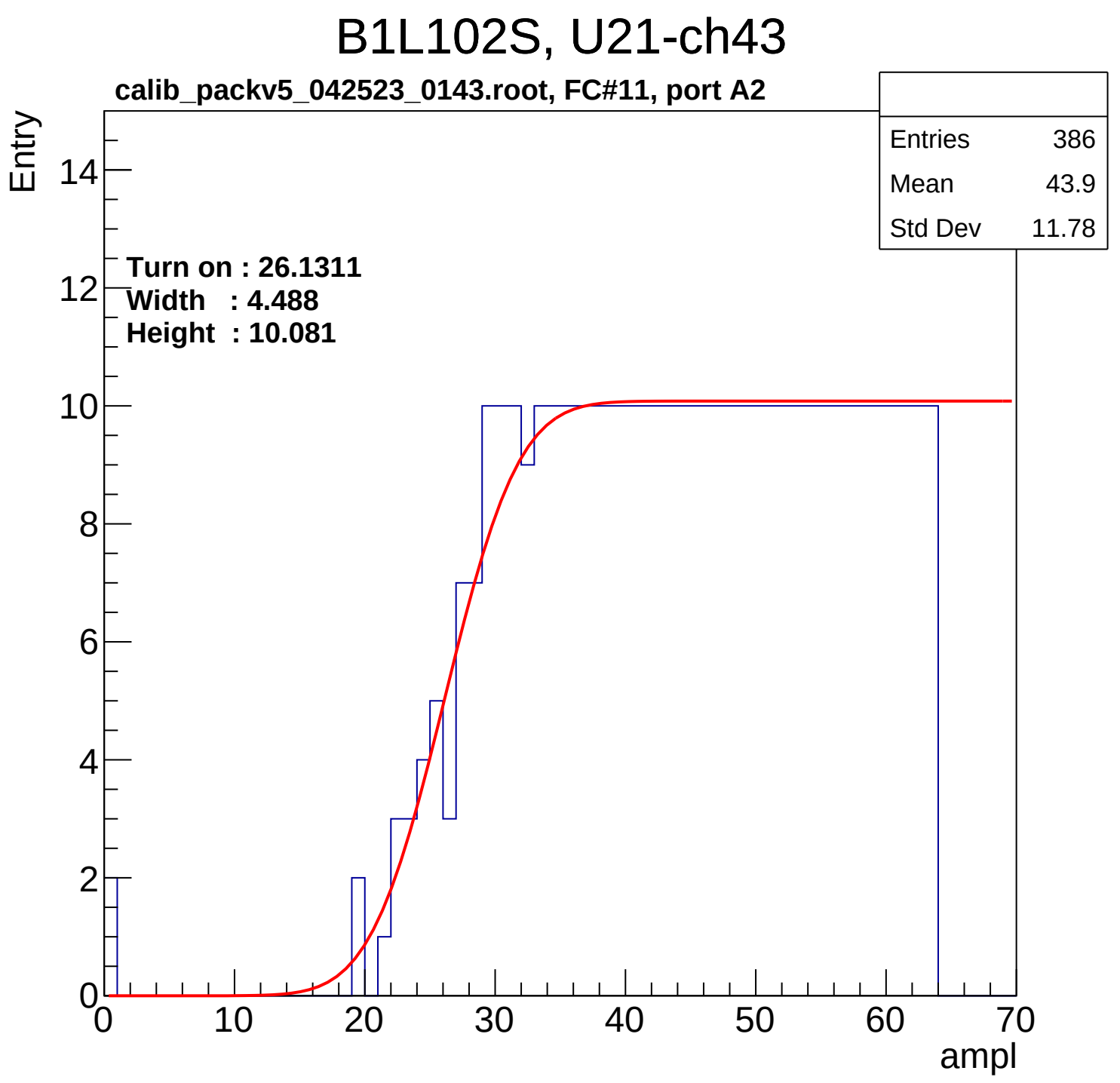
B1L102S, U21-ch43
calib_packv5_042523_0143.root, FC#11, port A2
Entries 386
Mean 43.9
Std Dev 11.78
Turn on : 26.1311
Width : 4.488
Height : 10.081
Entry
ampl
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6
8
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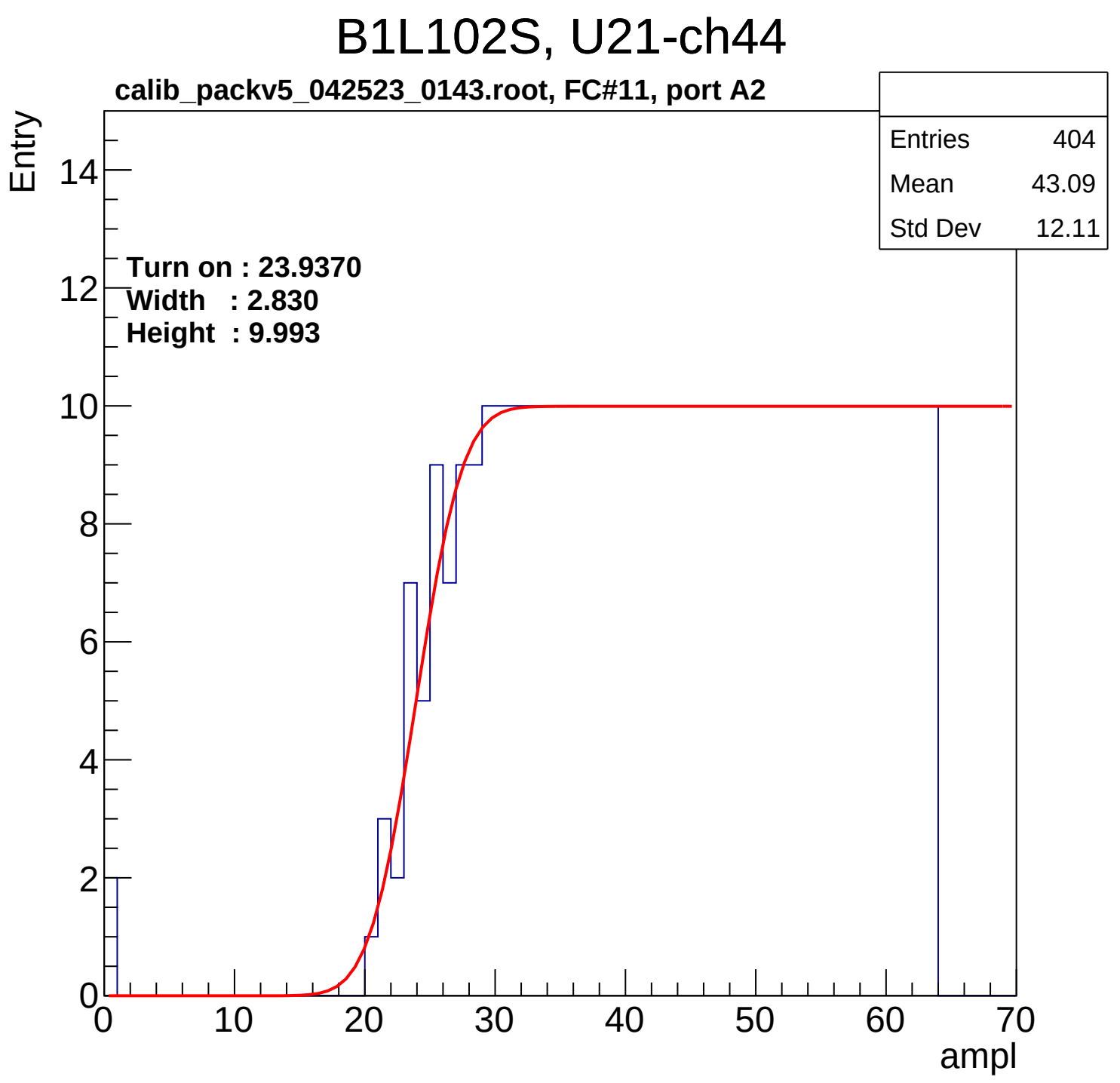
B1L102S, U21-ch44
calib_packv5_042523_0143.root, FC#11, port A2
Entries 404
Mean 43.09
Std Dev 12.11
Turn on : 23.9370
Width : 2.830
Height : 9.993
Entry
ampl
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2
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6
8
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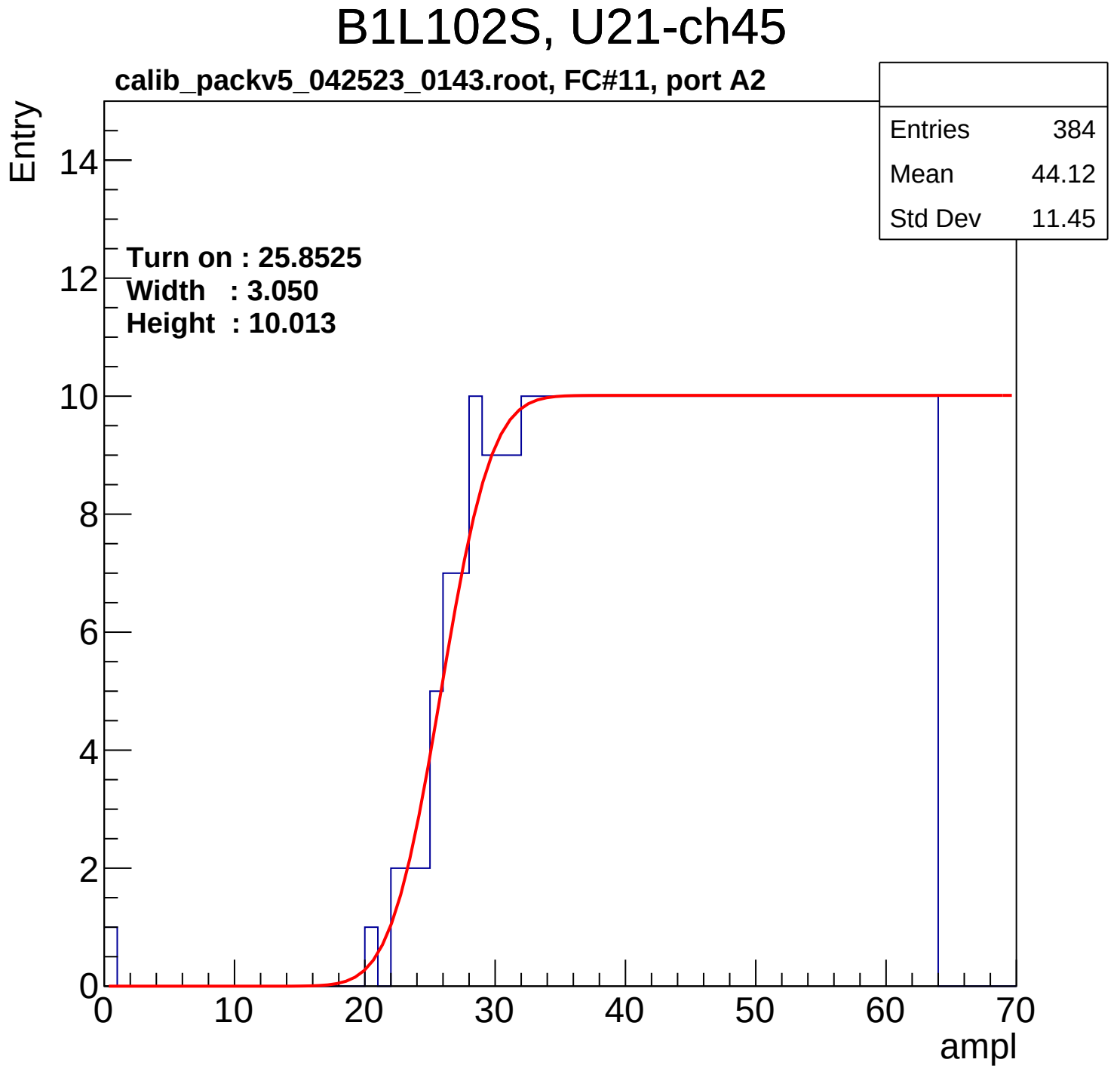
B1L102S, U21-ch45
calib_packv5_042523_0143.root, FC#11, port A2
Entries 384
Mean 44.12
Std Dev 11.45
Turn on : 25.8525
Width : 3.050
Height : 10.013
Entry
ampl
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6
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10
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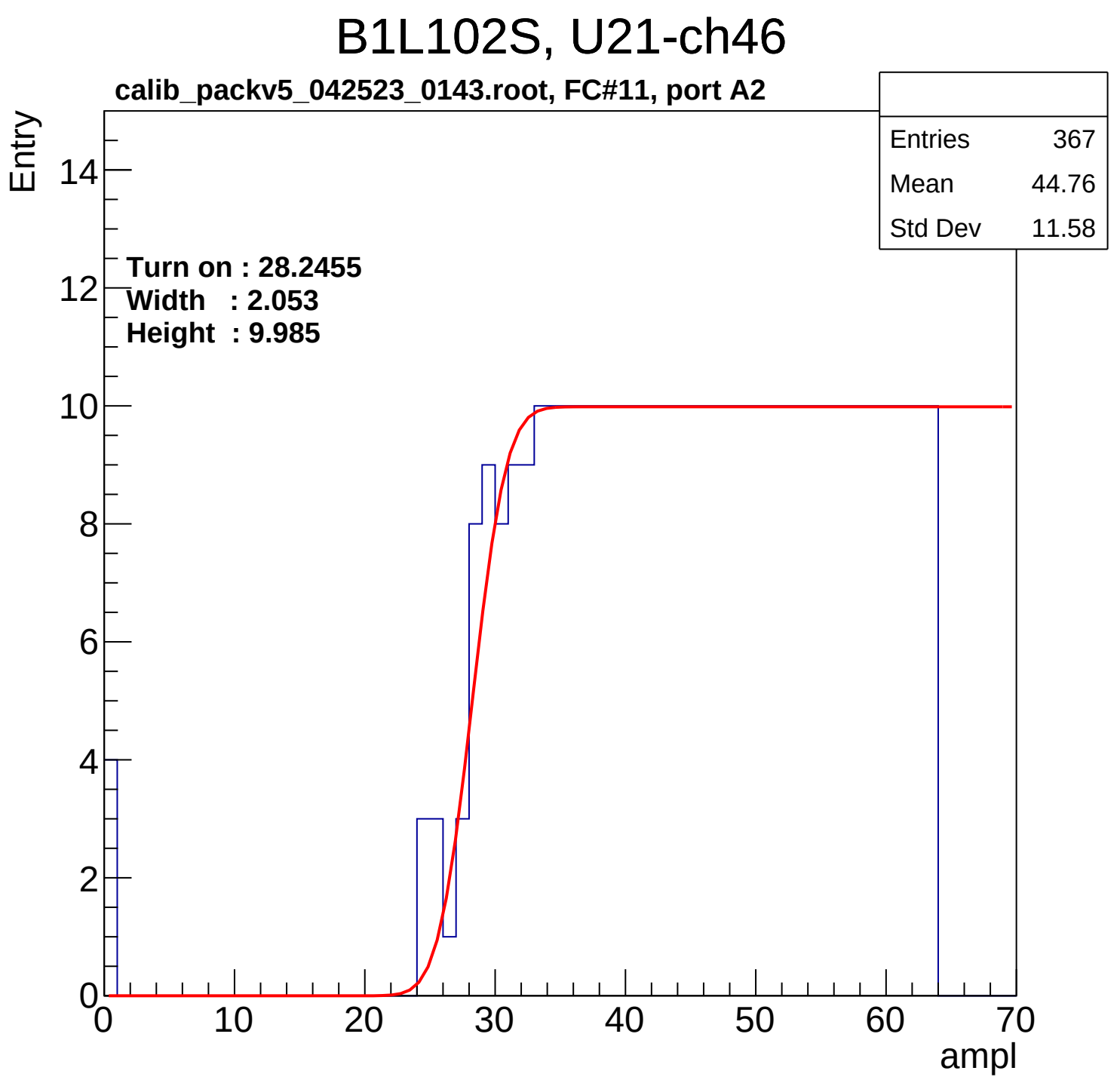
B1L102S, U21-ch46
calib_packv5_042523_0143.root, FC#11, port A2
Entries 367
Mean 44.76
Std Dev 11.58
Turn on : 28.2455
Width : 2.053
Height : 9.985
Entry
ampl
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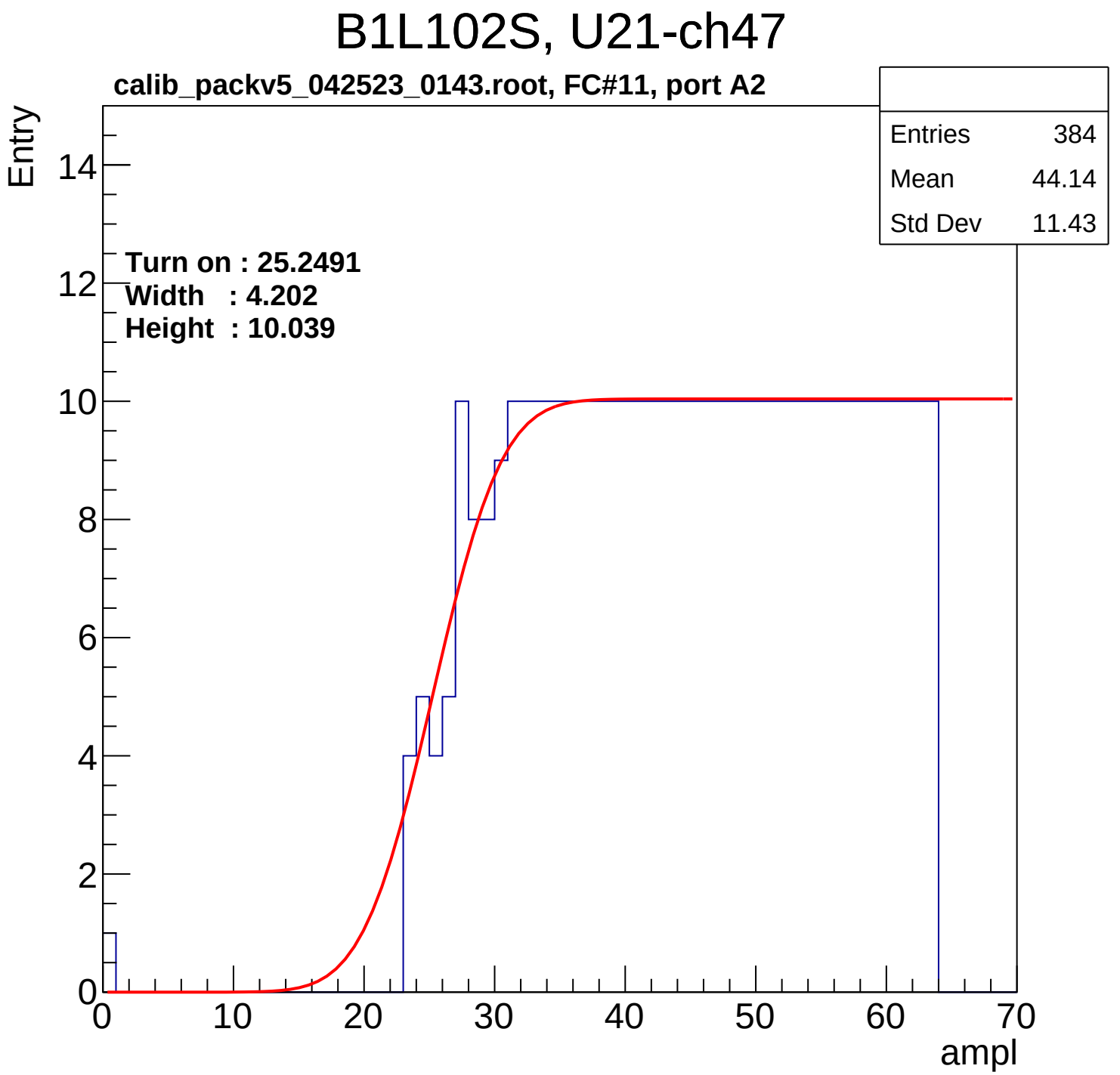
B1L102S, U21-ch47
calib_packv5_042523_0143.root, FC#11, port A2
Entries 384
Mean 44.14
Std Dev 11.43
Turn on : 25.2491
Width : 4.202
Height : 10.039
Entry
ampl
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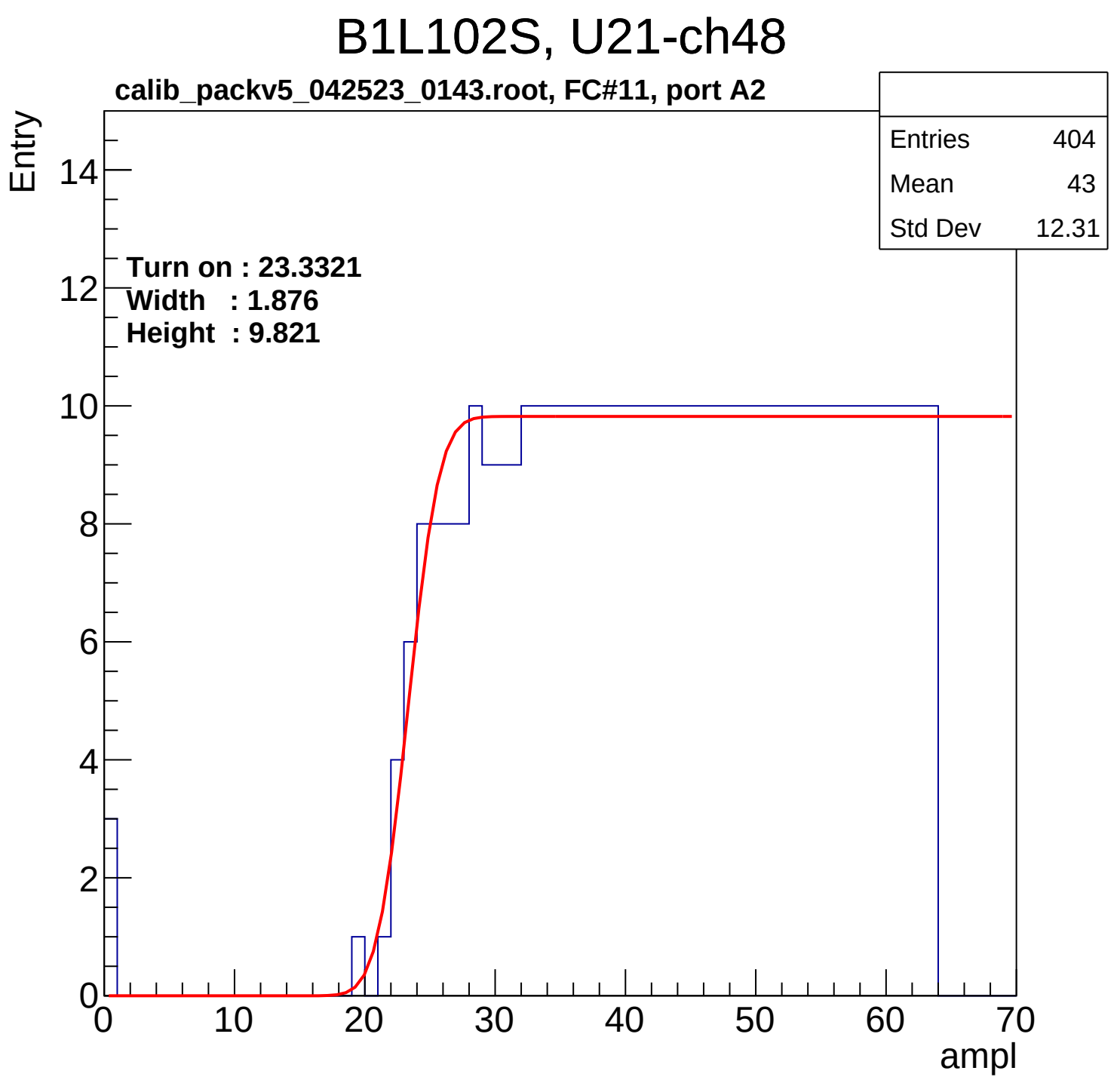
B1L102S, U21-ch48
calib_packv5_042523_0143.root, FC#11, port A2
Entries 404
Mean 43
Std Dev 12.31
Turn on : 23.3321
Width : 1.876
Height : 9.821
Entry
ampl
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2
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6
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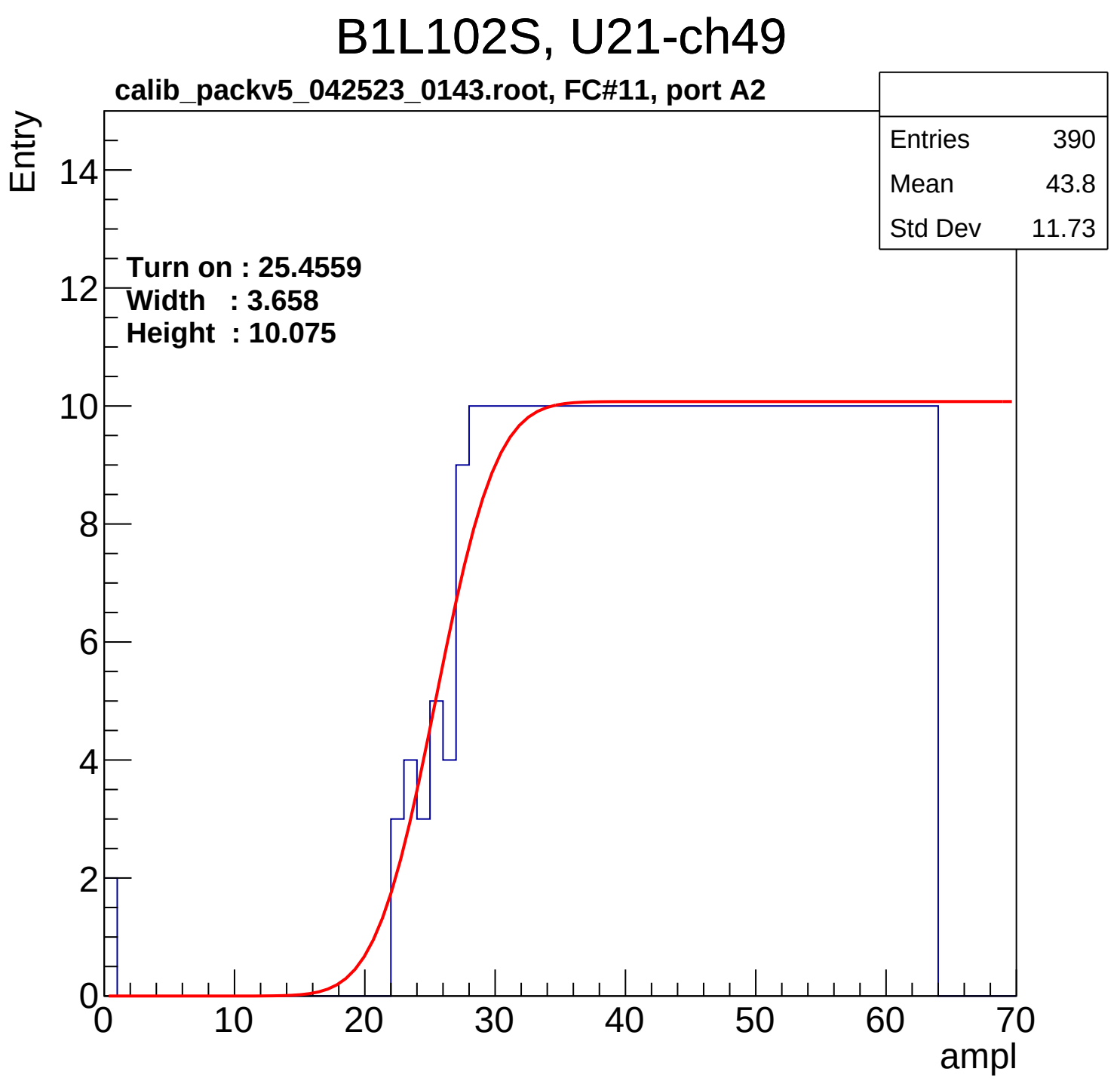
B1L102S, U21-ch49
calib_packv5_042523_0143.root, FC#11, port A2
Entries 390
Mean 43.8
Std Dev 11.73
Turn on : 25.4559
Width : 3.658
Height : 10.075
Entry
ampl
0
2
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8
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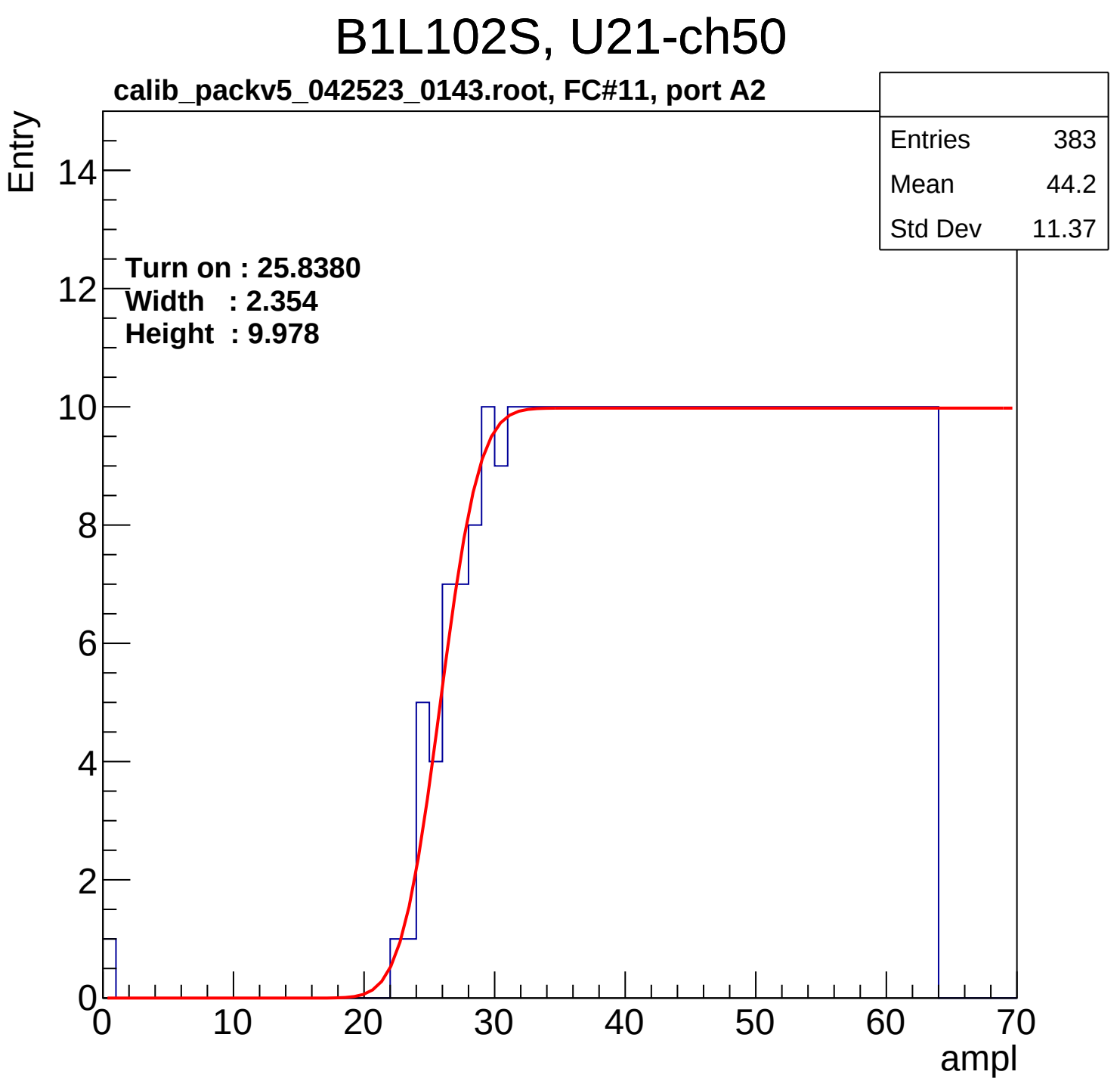
B1L102S, U21-ch50
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 44.2
Std Dev 11.37
Turn on : 25.8380
Width : 2.354
Height : 9.978
Entry
ampl
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2
4
6
8
10
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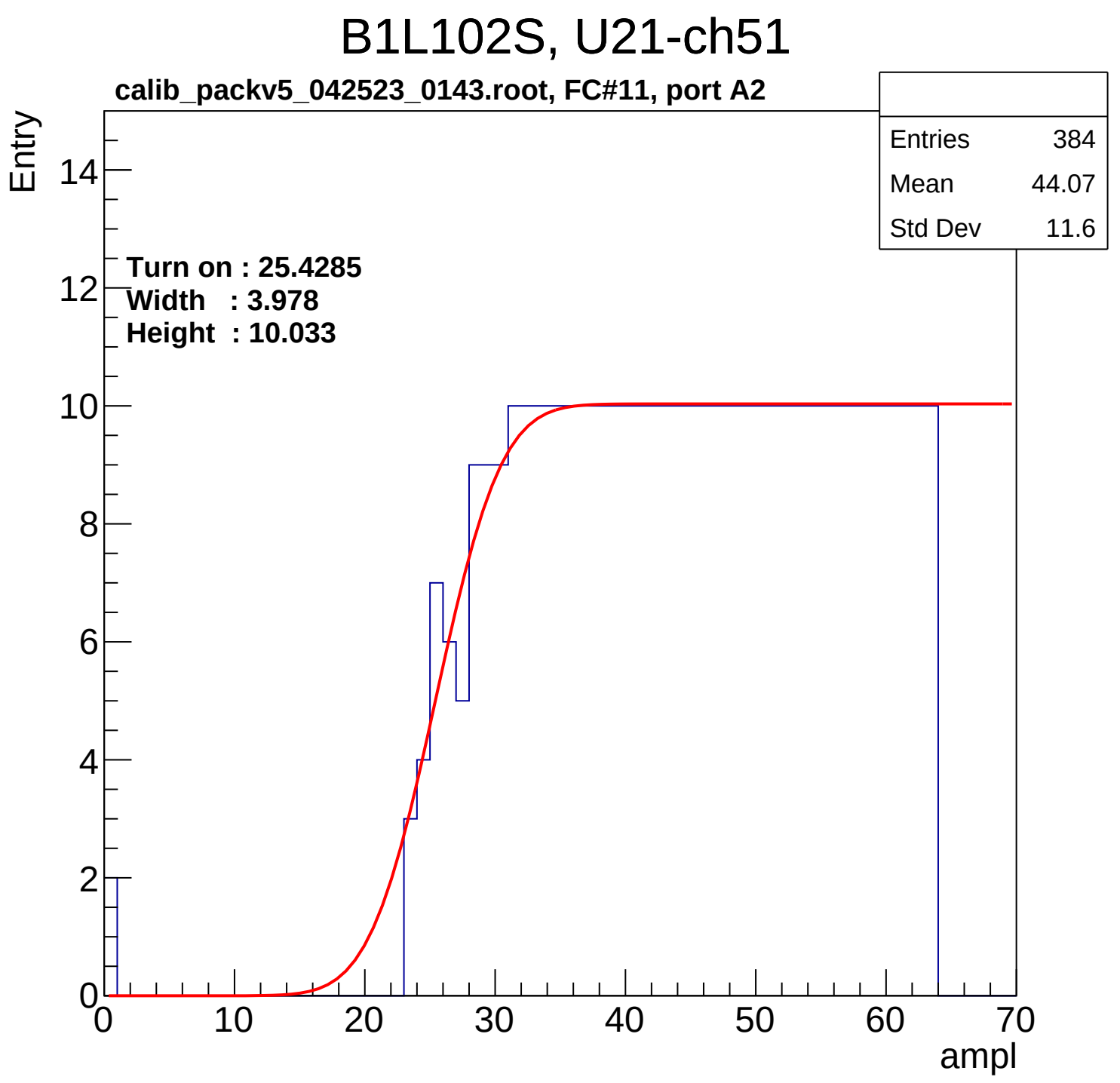
B1L102S, U21-ch51
calib_packv5_042523_0143.root, FC#11, port A2
Entries 384
Mean 44.07
Std Dev 11.6
Turn on : 25.4285
Width : 3.978
Height : 10.033
Entry
ampl
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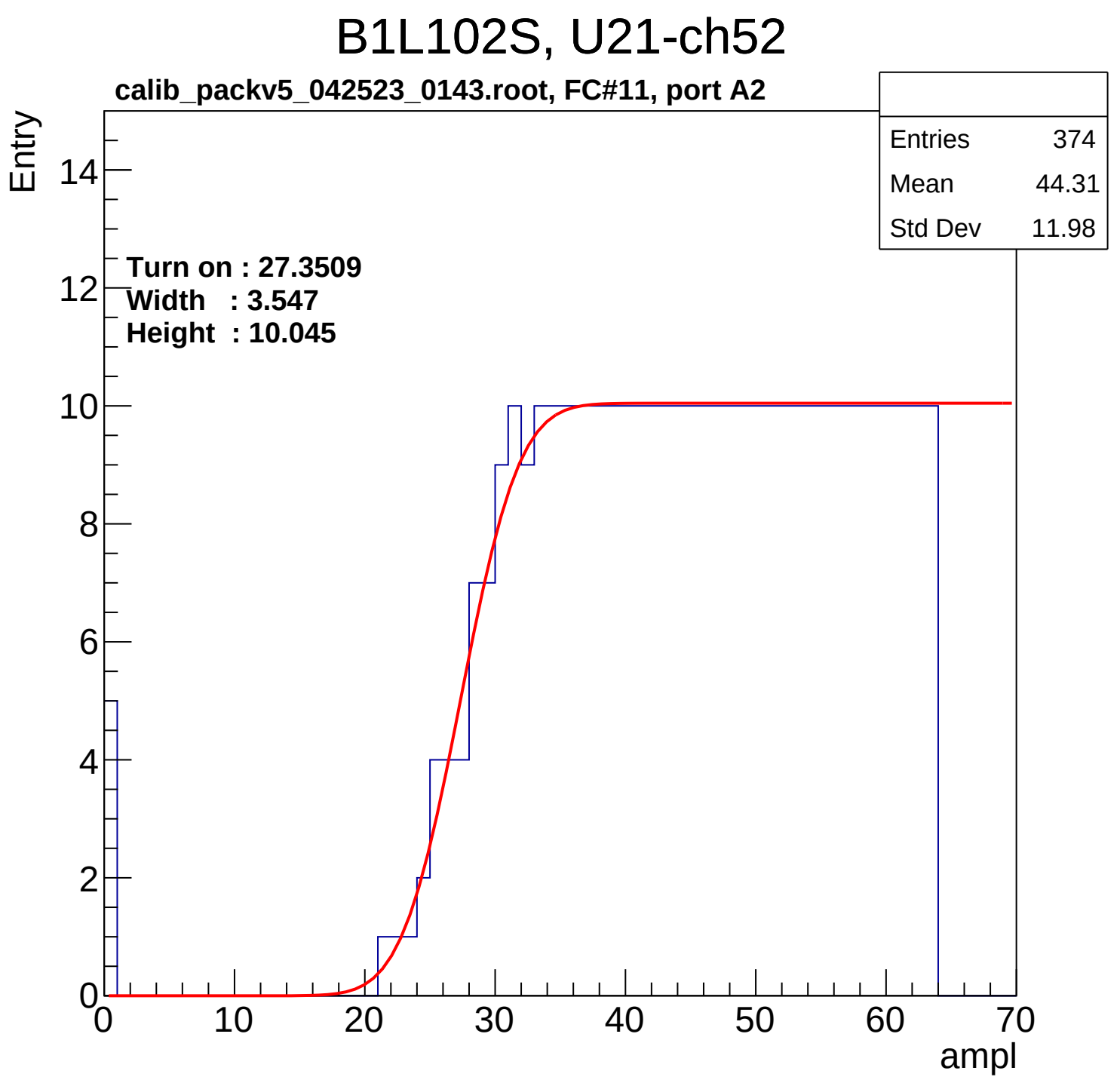
B1L102S, U21-ch52
calib_packv5_042523_0143.root, FC#11, port A2
Entries 374
Mean 44.31
Std Dev 11.98
Turn on : 27.3509
Width : 3.547
Height : 10.045
Entry
ampl
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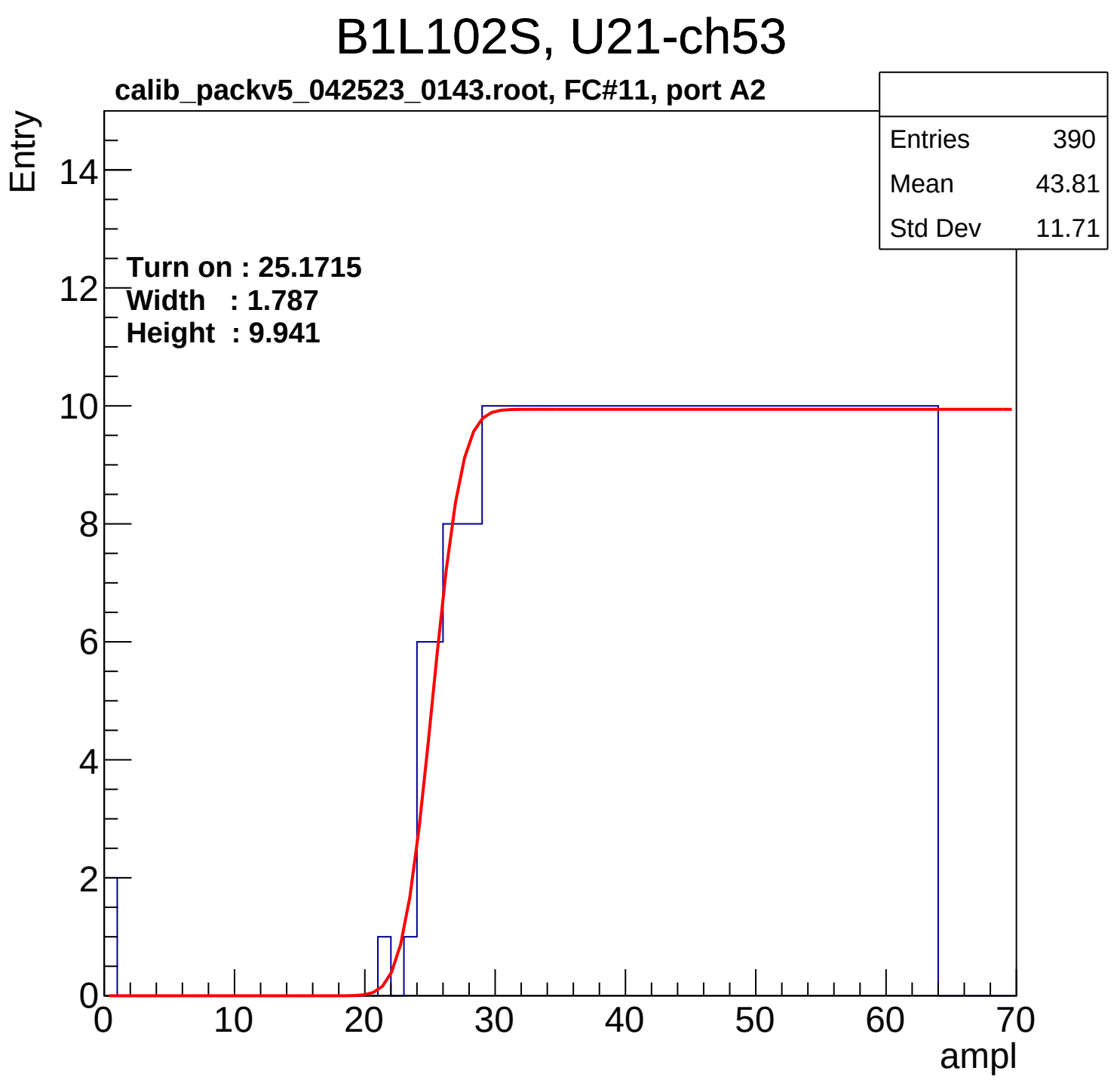
B1L102S, U21-ch53
calib_packv5_042523_0143.root, FC#11, port A2
Entries 390
Mean 43.81
Std Dev 11.71
Turn on : 25.1715
Width : 1.787
Height : 9.941
Entry
ampl
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8
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0
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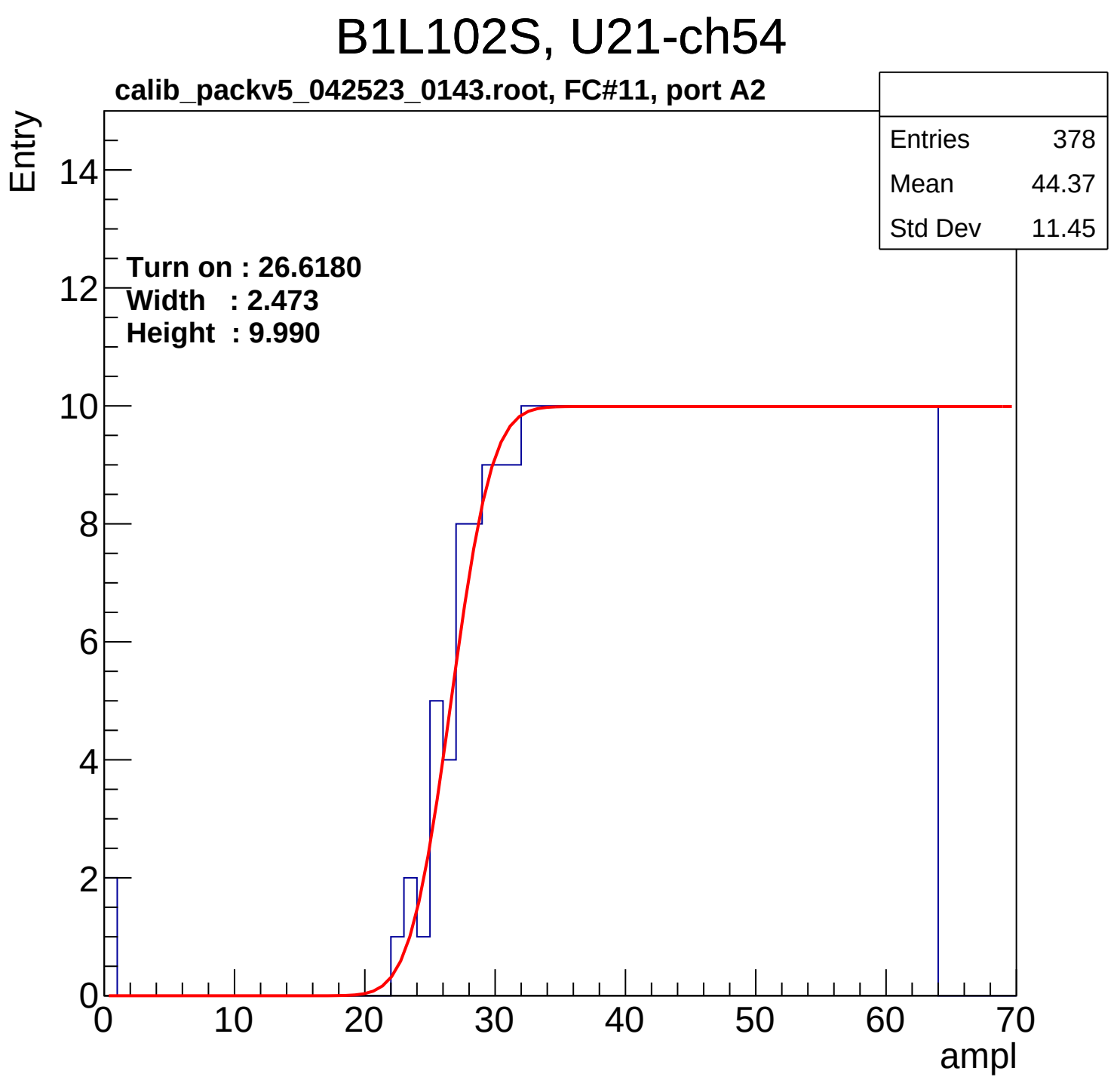
B1L102S, U21-ch54
calib_packv5_042523_0143.root, FC#11, port A2
Entries 378
Mean 44.37
Std Dev 11.45
Turn on : 26.6180
Width : 2.473
Height : 9.990
Entry
ampl
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2
4
6
8
10
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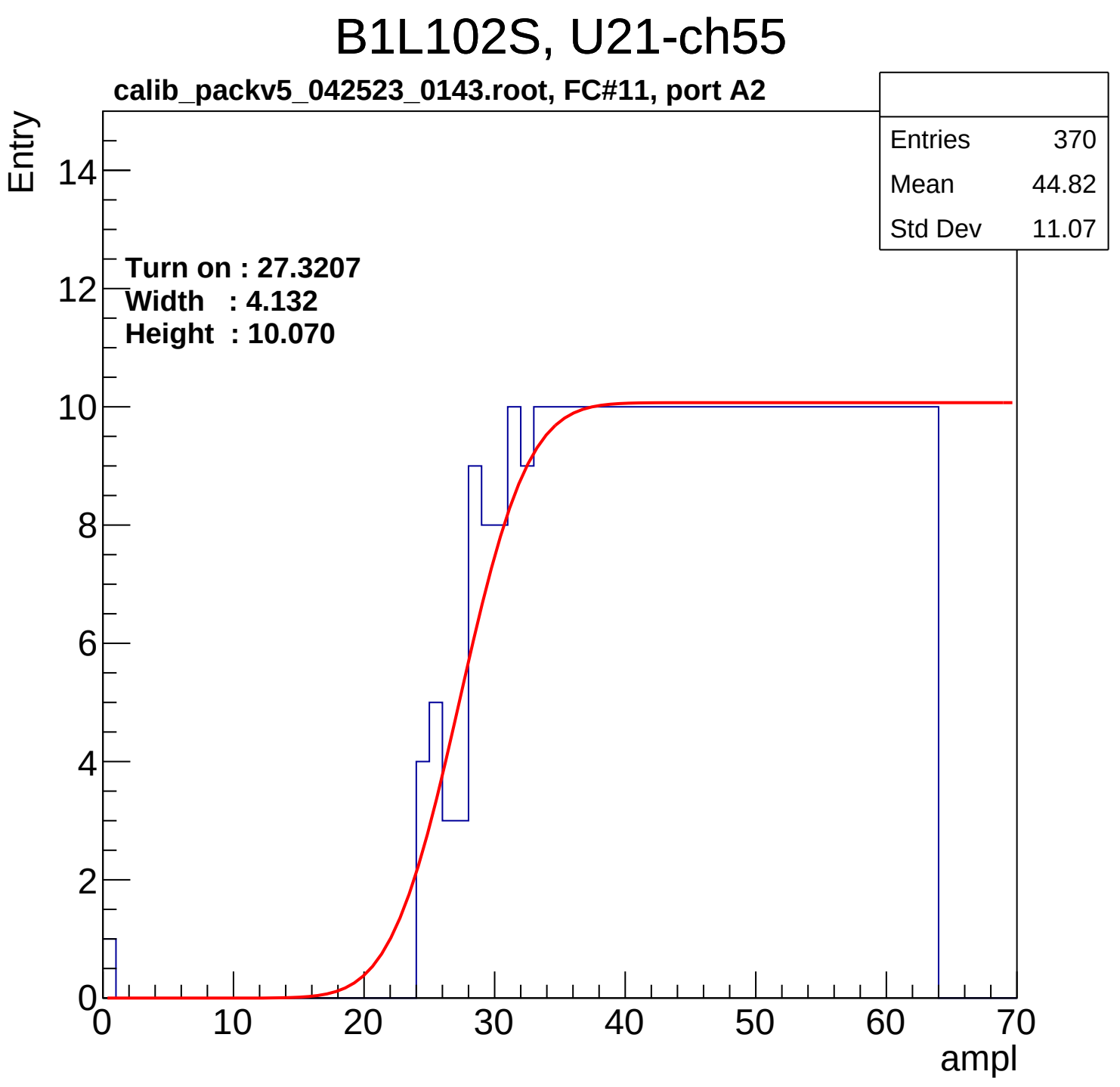
B1L102S, U21-ch55
calib_packv5_042523_0143.root, FC#11, port A2
Entries 370
Mean 44.82
Std Dev 11.07
Turn on : 27.3207
Width : 4.132
Height : 10.070
Entry
ampl
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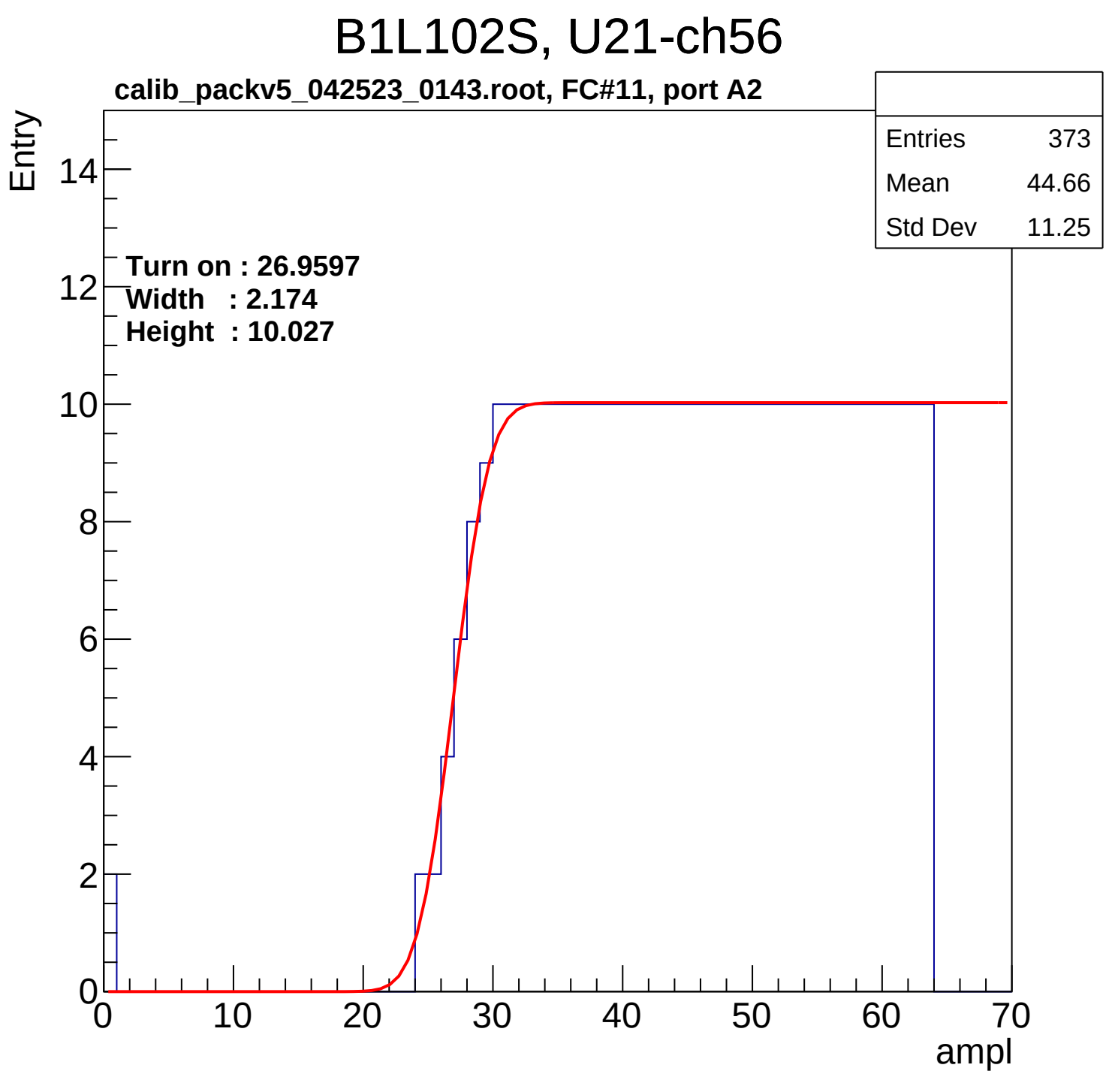
B1L102S, U21-ch56
calib_packv5_042523_0143.root, FC#11, port A2
Entries 373
Mean 44.66
Std Dev 11.25
Turn on : 26.9597
Width : 2.174
Height : 10.027
Entry
ampl
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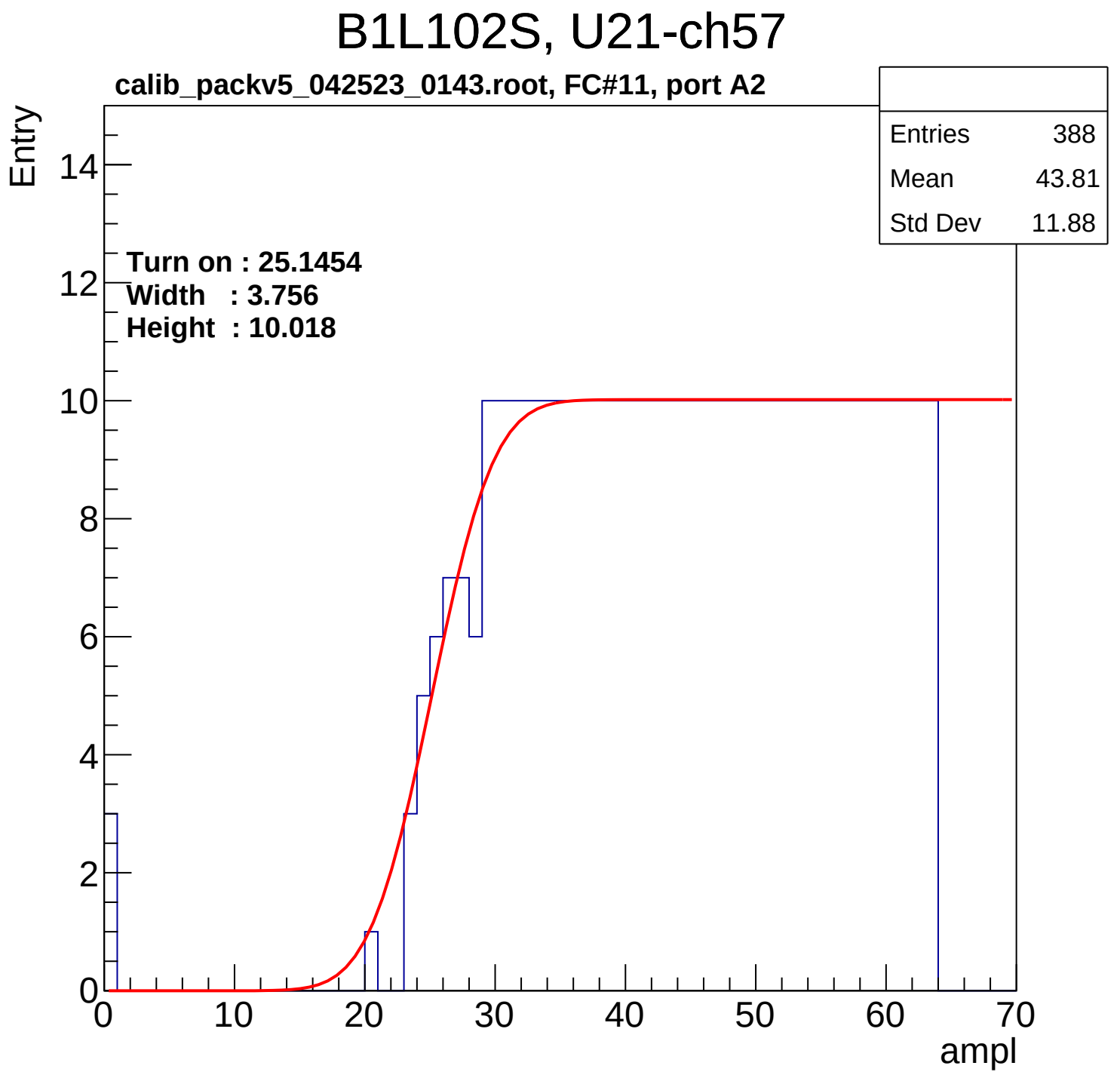
B1L102S, U21-ch57
calib_packv5_042523_0143.root, FC#11, port A2
Entries 388
Mean 43.81
Std Dev 11.88
Turn on : 25.1454
Width : 3.756
Height : 10.018
Entry
ampl
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4
6
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12
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10
20
30
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50
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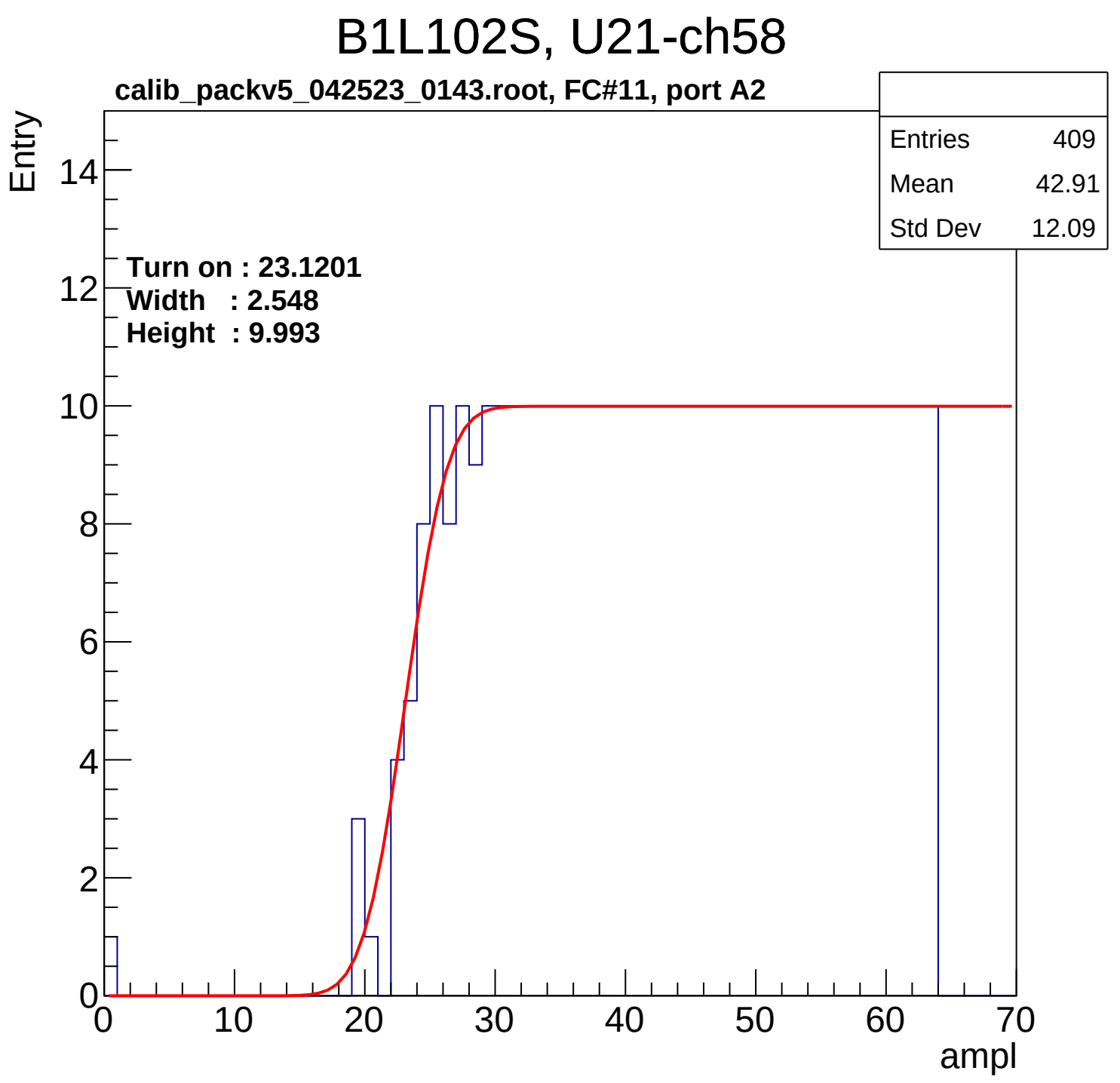
B1L102S, U21-ch58
calib_packv5_042523_0143.root, FC#11, port A2
Entries 409
Mean 42.91
Std Dev 12.09
Turn on : 23.1201
Width : 2.548
Height : 9.993
Entry
ampl
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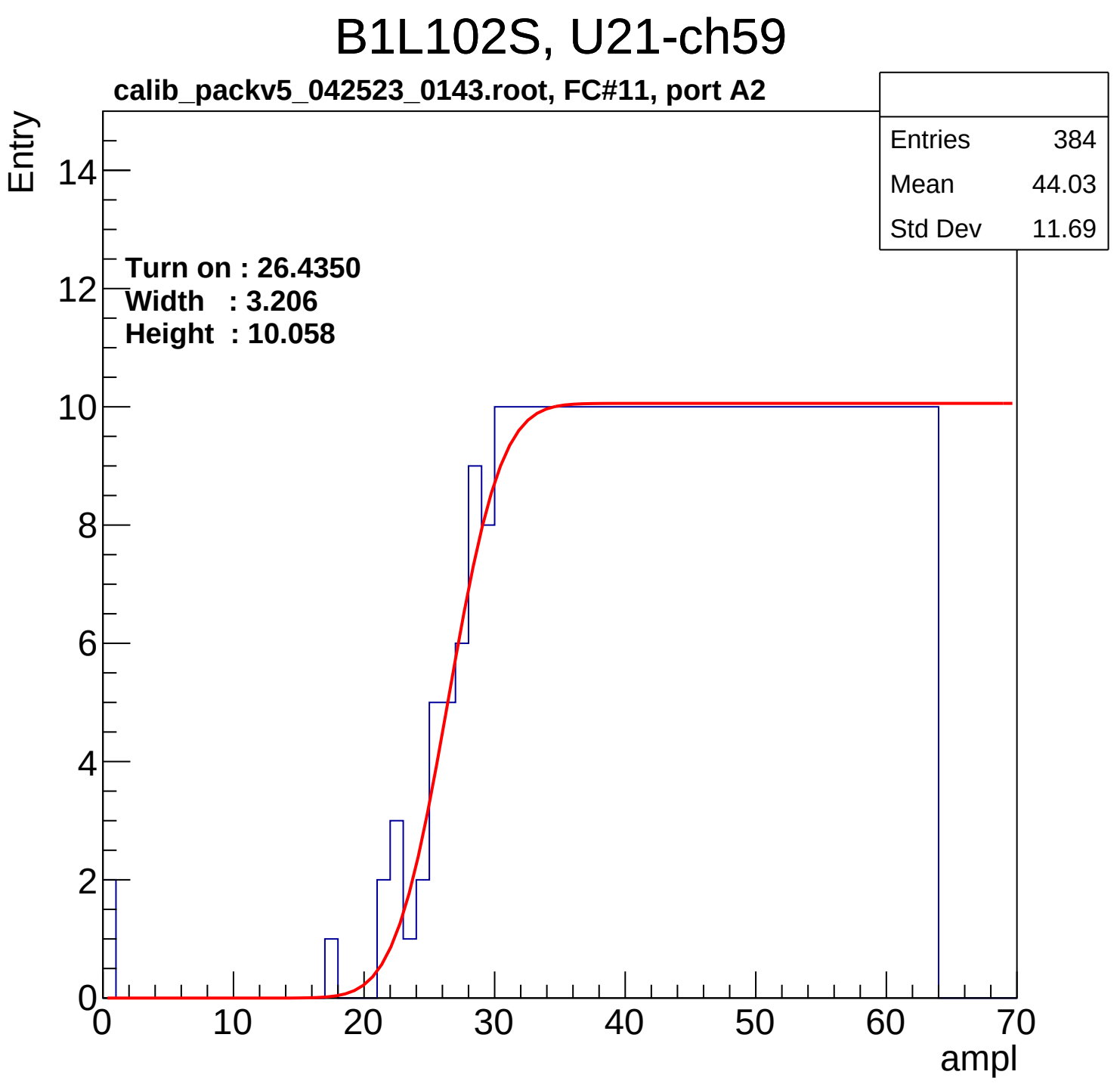
B1L102S, U21-ch59
calib_packv5_042523_0143.root, FC#11, port A2
Entries 384
Mean 44.03
Std Dev 11.69
Turn on : 26.4350
Width : 3.206
Height : 10.058
Entry
ampl
0
2
4
6
8
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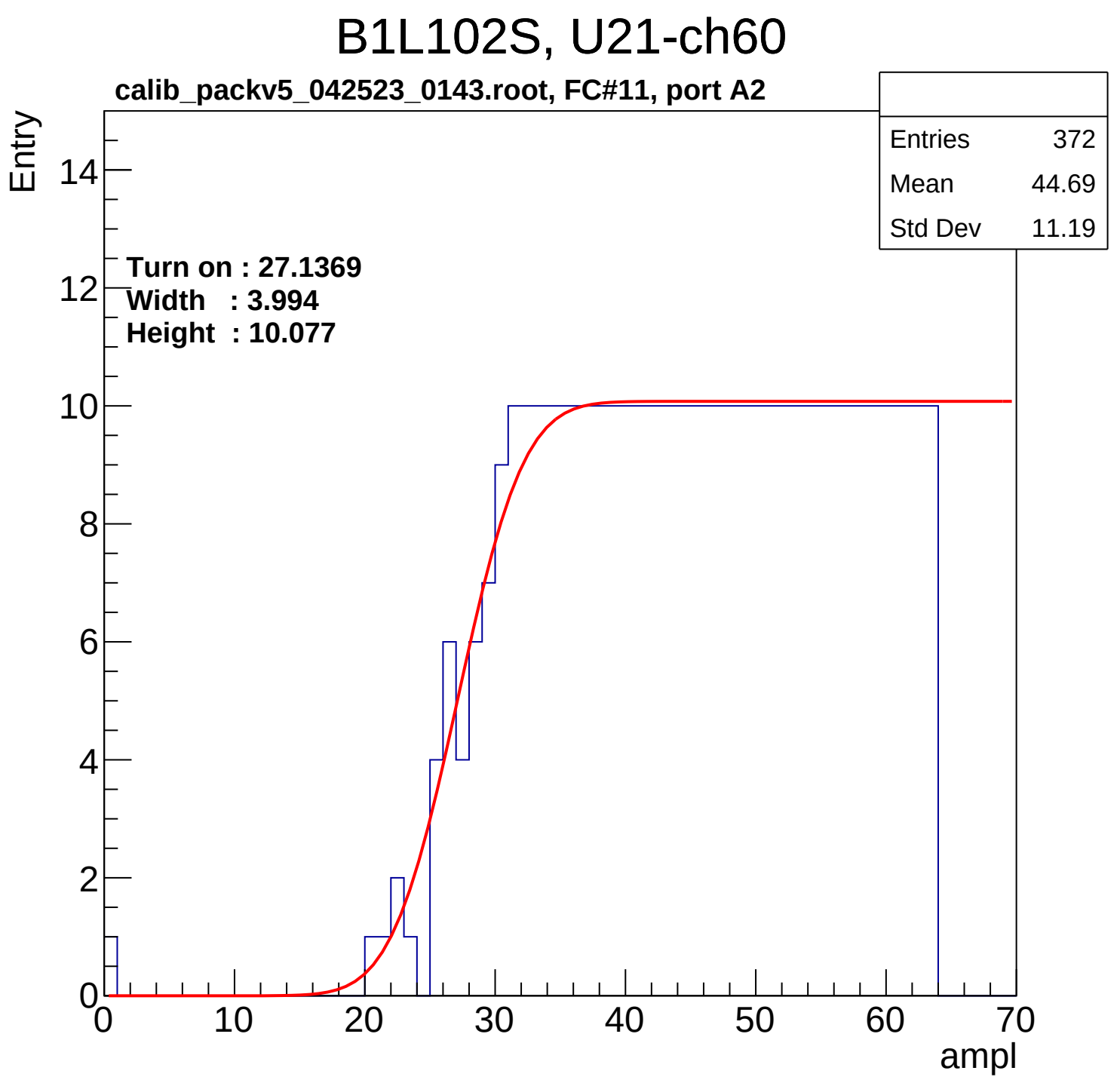
B1L102S, U21-ch60
calib_packv5_042523_0143.root, FC#11, port A2
Entries 372
Mean 44.69
Std Dev 11.19
Turn on : 27.1369
Width : 3.994
Height : 10.077
Entry
ampl
0
2
4
6
8
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0
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20
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60
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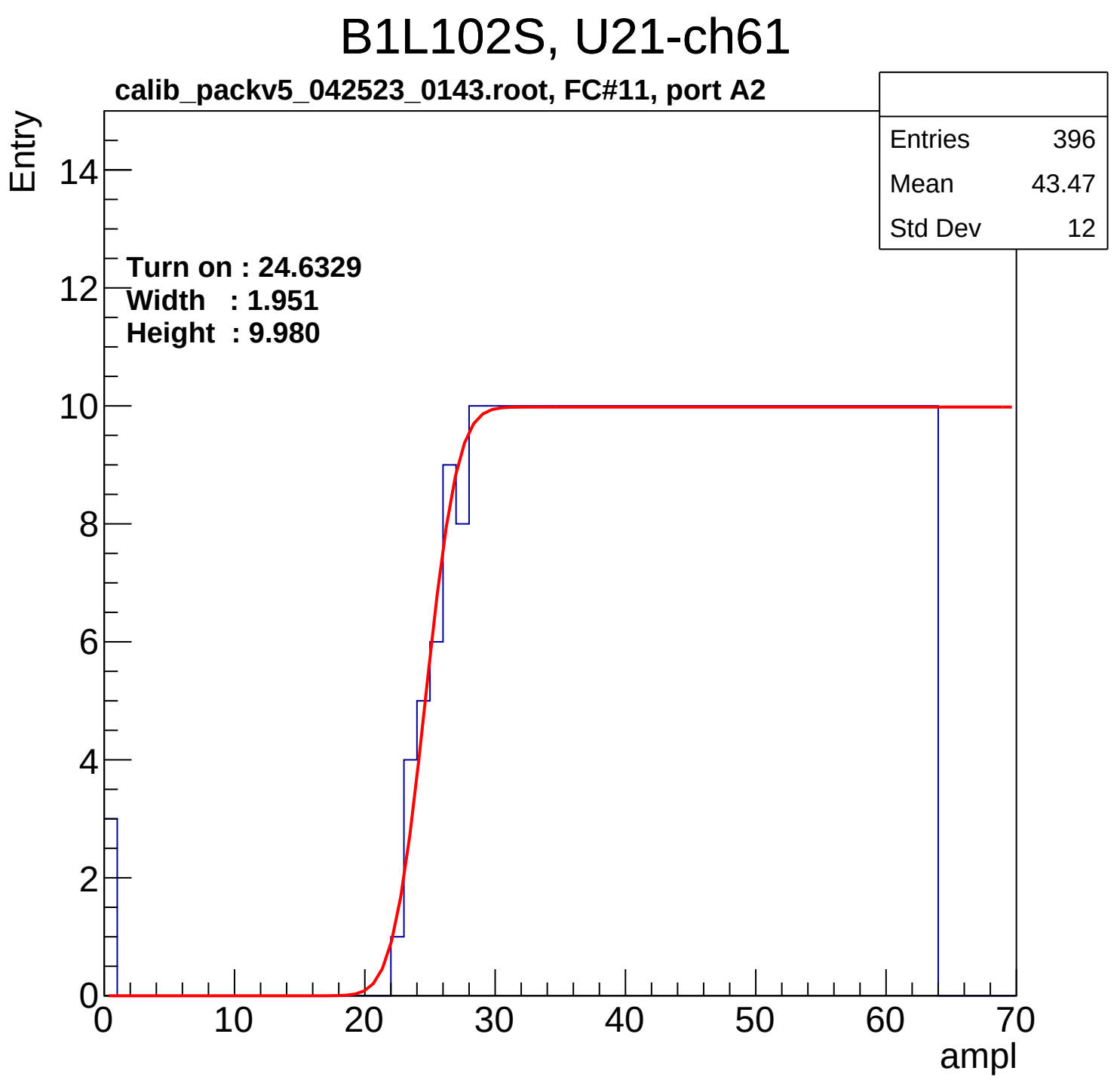
B1L102S, U21-ch61
calib_packv5_042523_0143.root, FC#11, port A2
Entries 396
Mean 43.47
Std Dev 12
Turn on : 24.6329
Width : 1.951
Height : 9.980
Entry
ampl
0
2
4
6
8
10
12
14
0
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60
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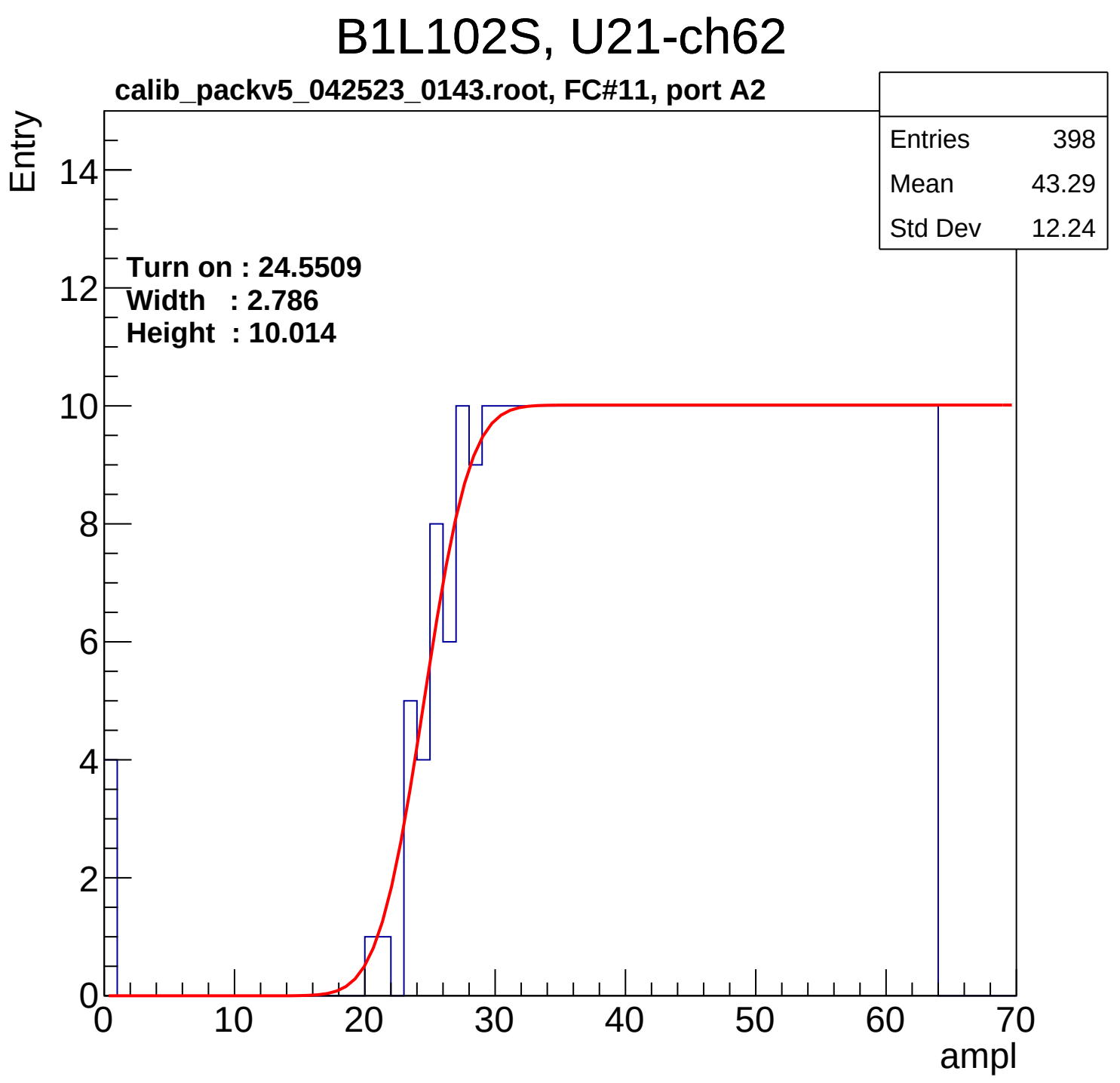
B1L102S, U21-ch62
calib_packv5_042523_0143.root, FC#11, port A2
Entries 398
Mean 43.29
Std Dev 12.24
Turn on : 24.5509
Width : 2.786
Height : 10.014
Entry
ampl
0
2
4
6
8
10
12
14
0
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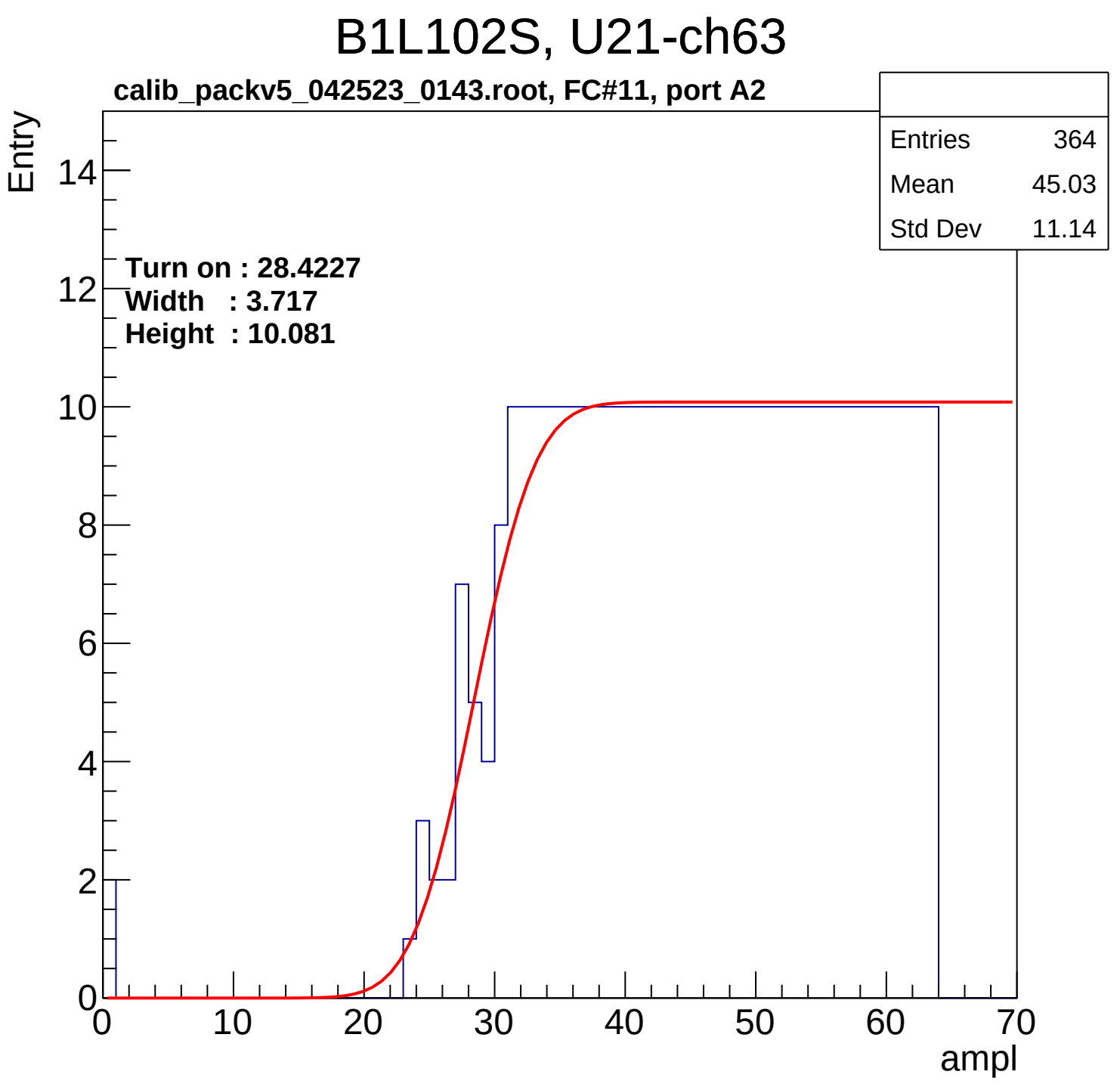
B1L102S, U21-ch63
calib_packv5_042523_0143.root, FC#11, port A2
Entries 364
Mean 45.03
Std Dev 11.14
Turn on : 28.4227
Width : 3.717
Height : 10.081
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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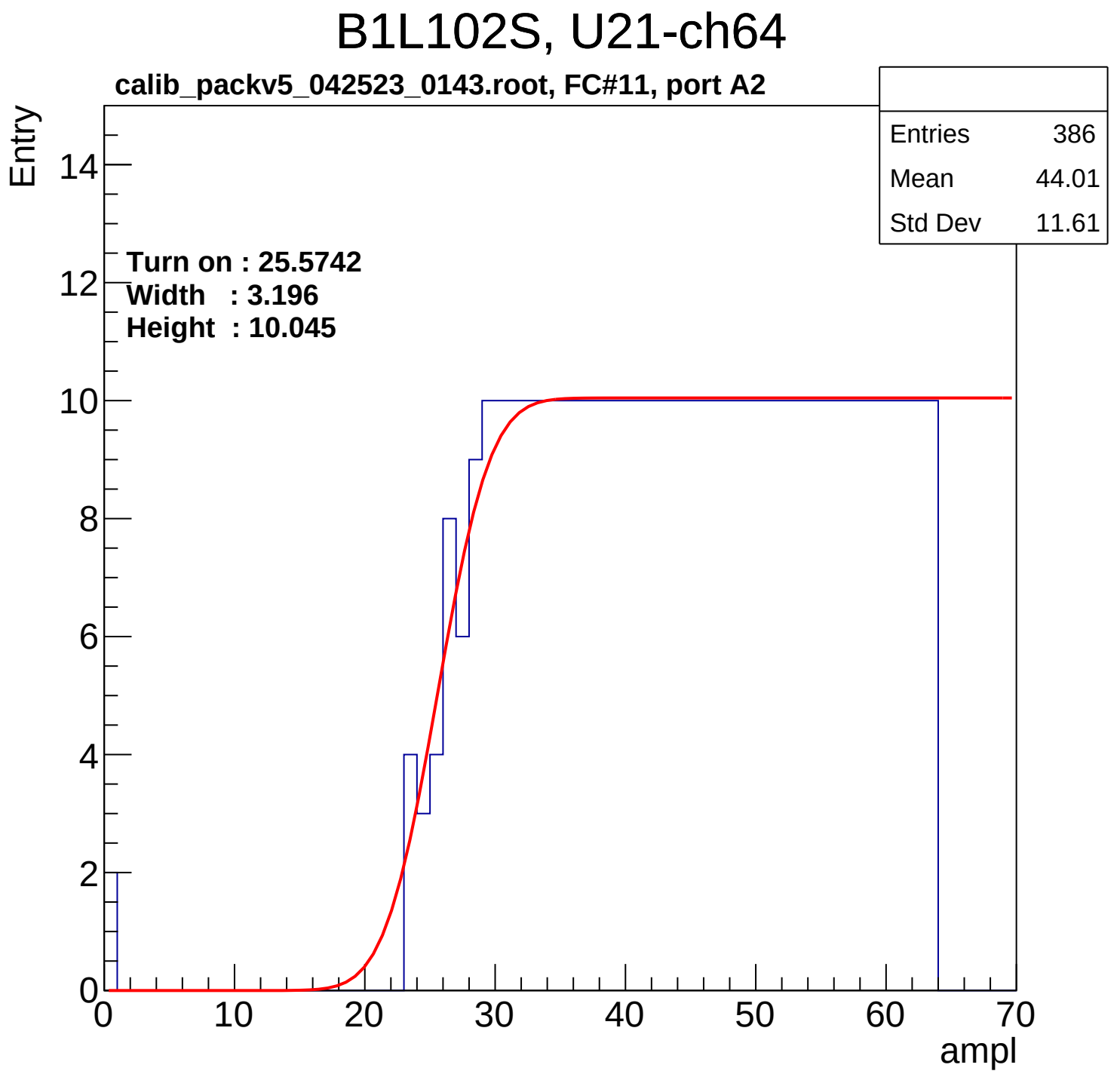
B1L102S, U21-ch64
calib_packv5_042523_0143.root, FC#11, port A2
Entries 386
Mean 44.01
Std Dev 11.61
Turn on : 25.5742
Width : 3.196
Height : 10.045
Entry
ampl
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2
4
6
8
10
12
14
0
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20
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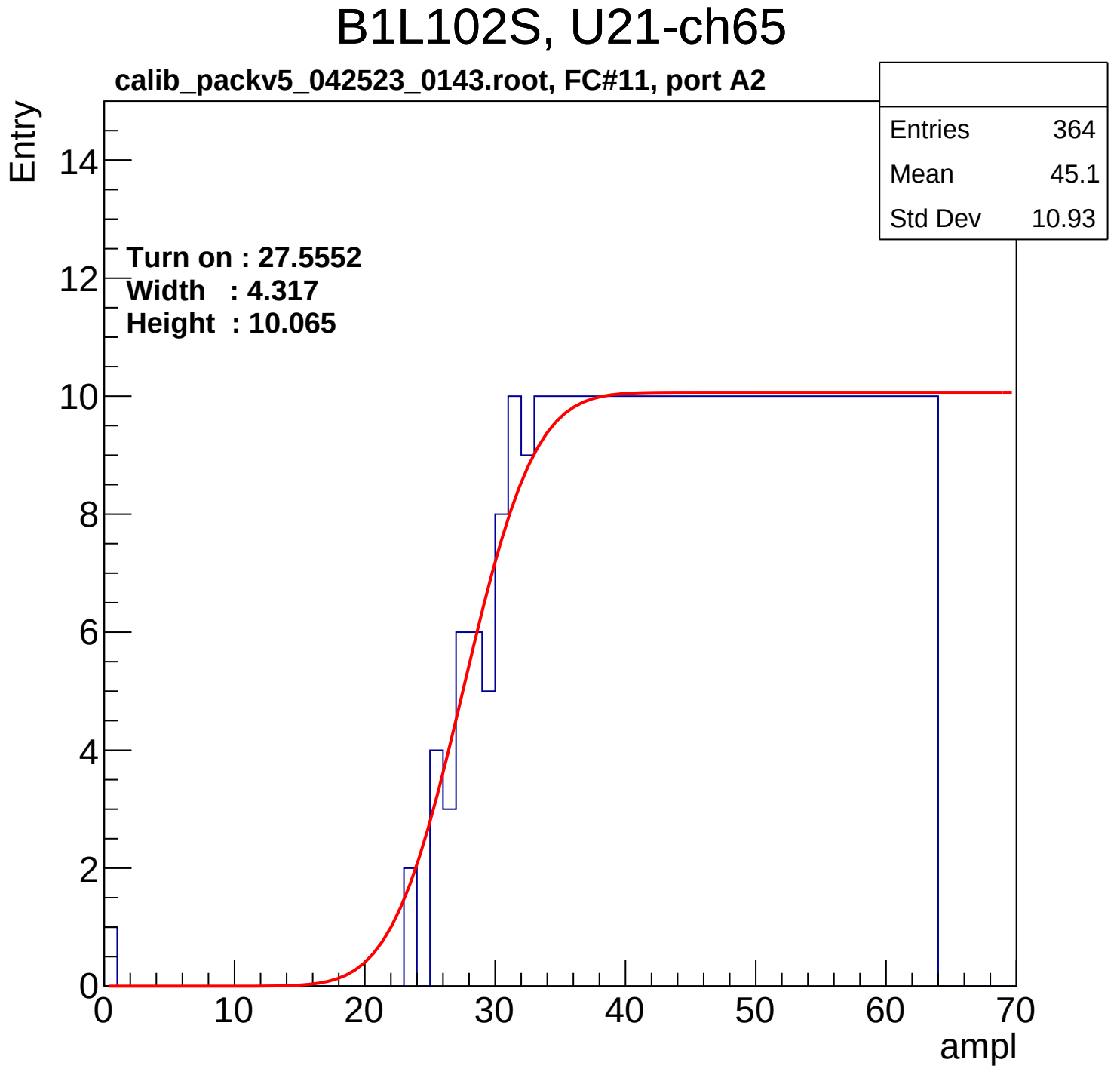
B1L102S, U21-ch65
calib_packv5_042523_0143.root, FC#11, port A2
Entries 364
Mean 45.1
Std Dev 10.93
Turn on : 27.5552
Width : 4.317
Height : 10.065
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
50
60
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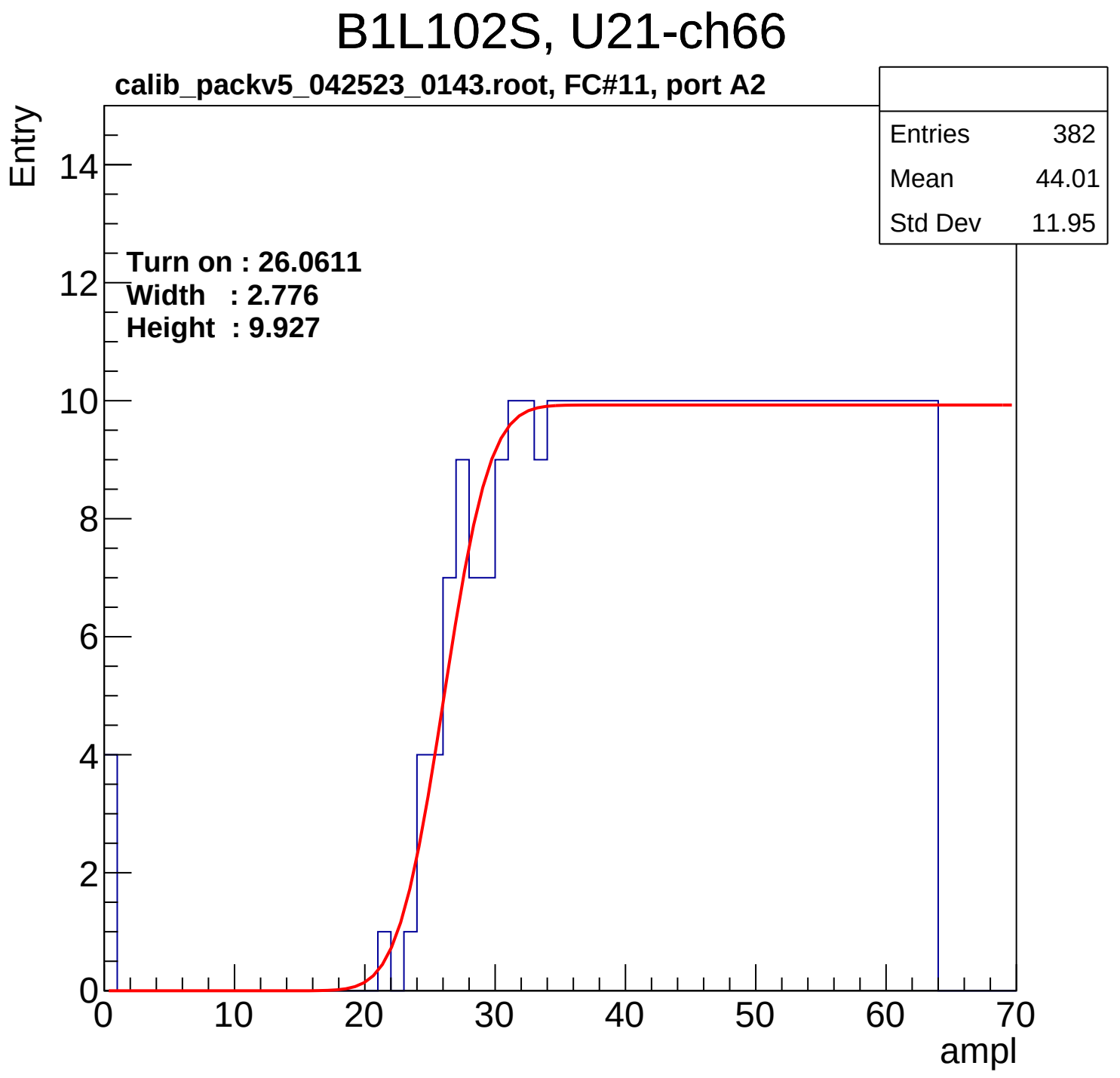
B1L102S, U21-ch66
calib_packv5_042523_0143.root, FC#11, port A2
Entries 382
Mean 44.01
Std Dev 11.95
Turn on : 26.0611
Width : 2.776
Height : 9.927
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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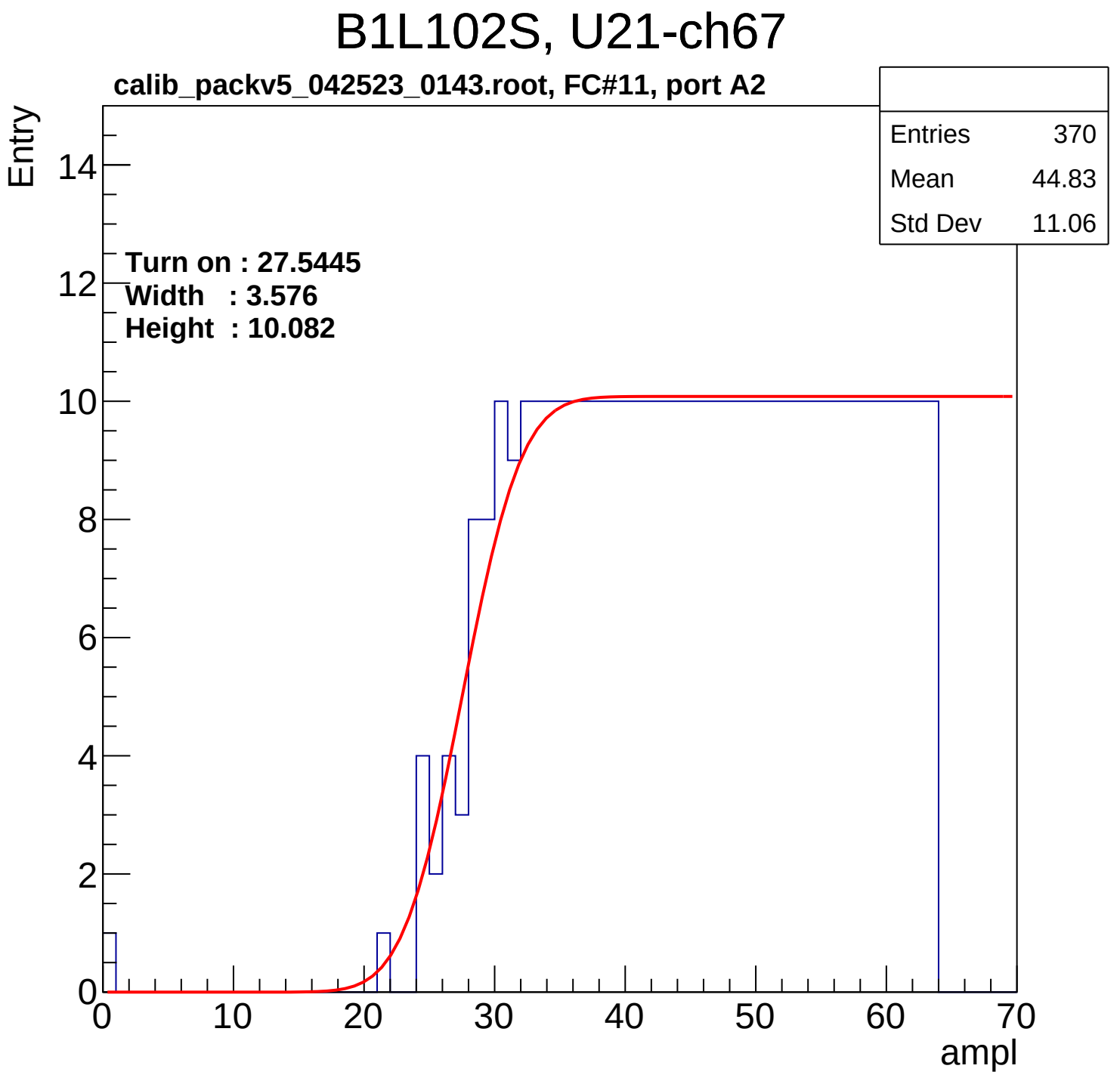
B1L102S, U21-ch67
calib_packv5_042523_0143.root, FC#11, port A2
Entries 370
Mean 44.83
Std Dev 11.06
Turn on : 27.5445
Width : 3.576
Height : 10.082
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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40
50
60
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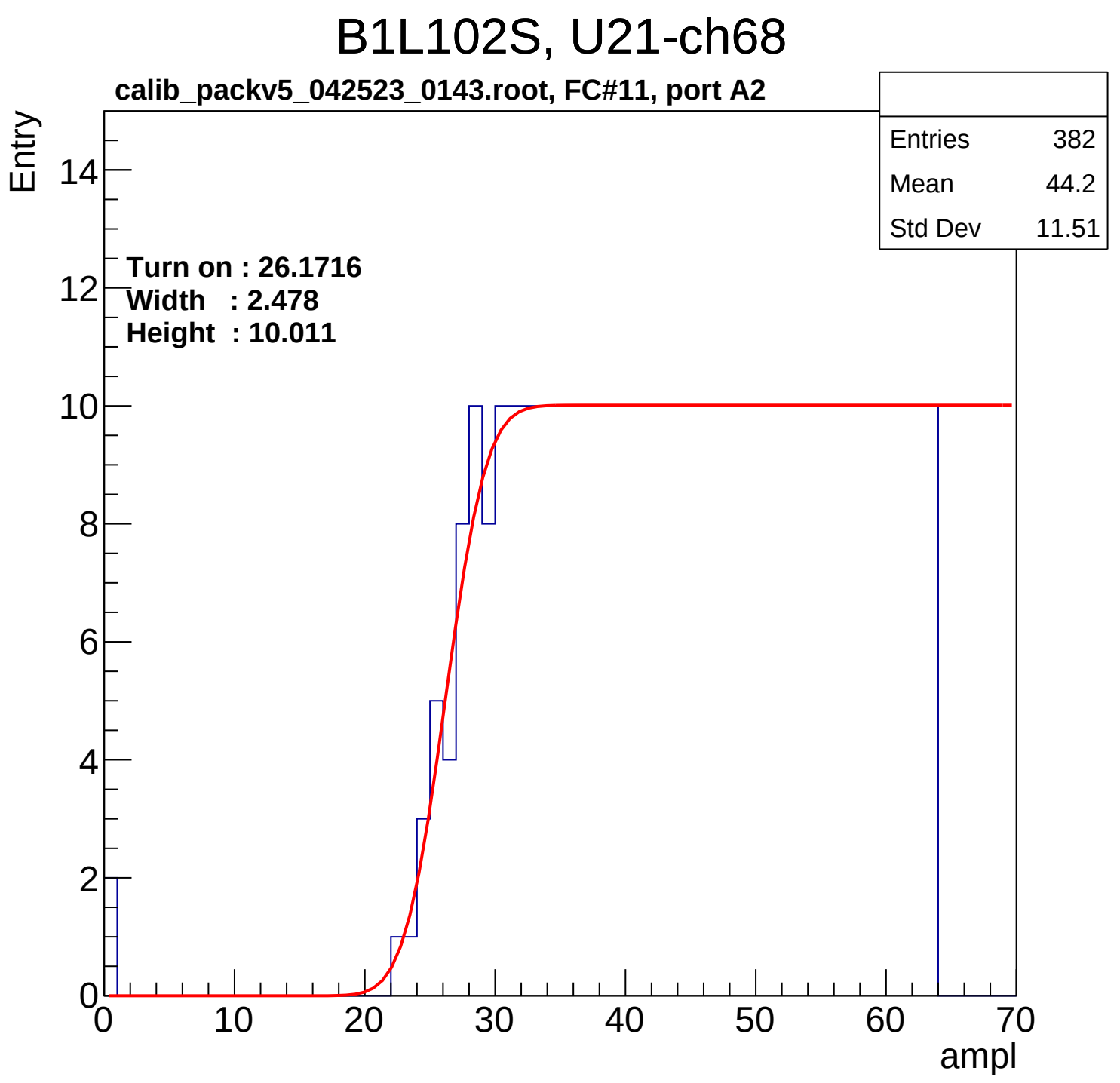
B1L102S, U21-ch68
calib_packv5_042523_0143.root, FC#11, port A2
Entries 382
Mean 44.2
Std Dev 11.51
Turn on : 26.1716
Width : 2.478
Height : 10.011
Entry
ampl
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2
4
6
8
10
12
14
0
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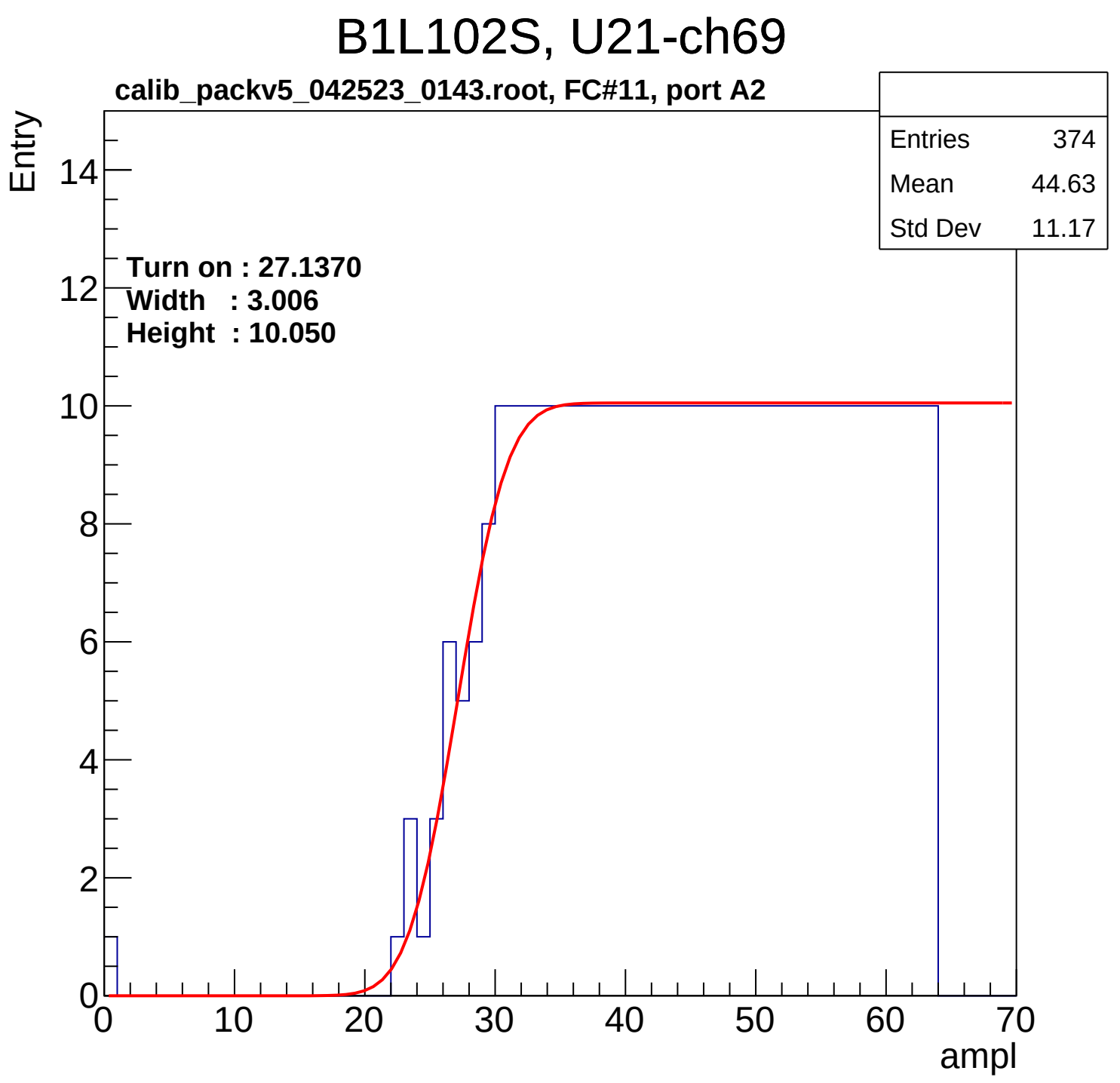
B1L102S, U21-ch69
calib_packv5_042523_0143.root, FC#11, port A2
Entries 374
Mean 44.63
Std Dev 11.17
Turn on : 27.1370
Width : 3.006
Height : 10.050
Entry
ampl
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2
4
6
8
10
12
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0
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20
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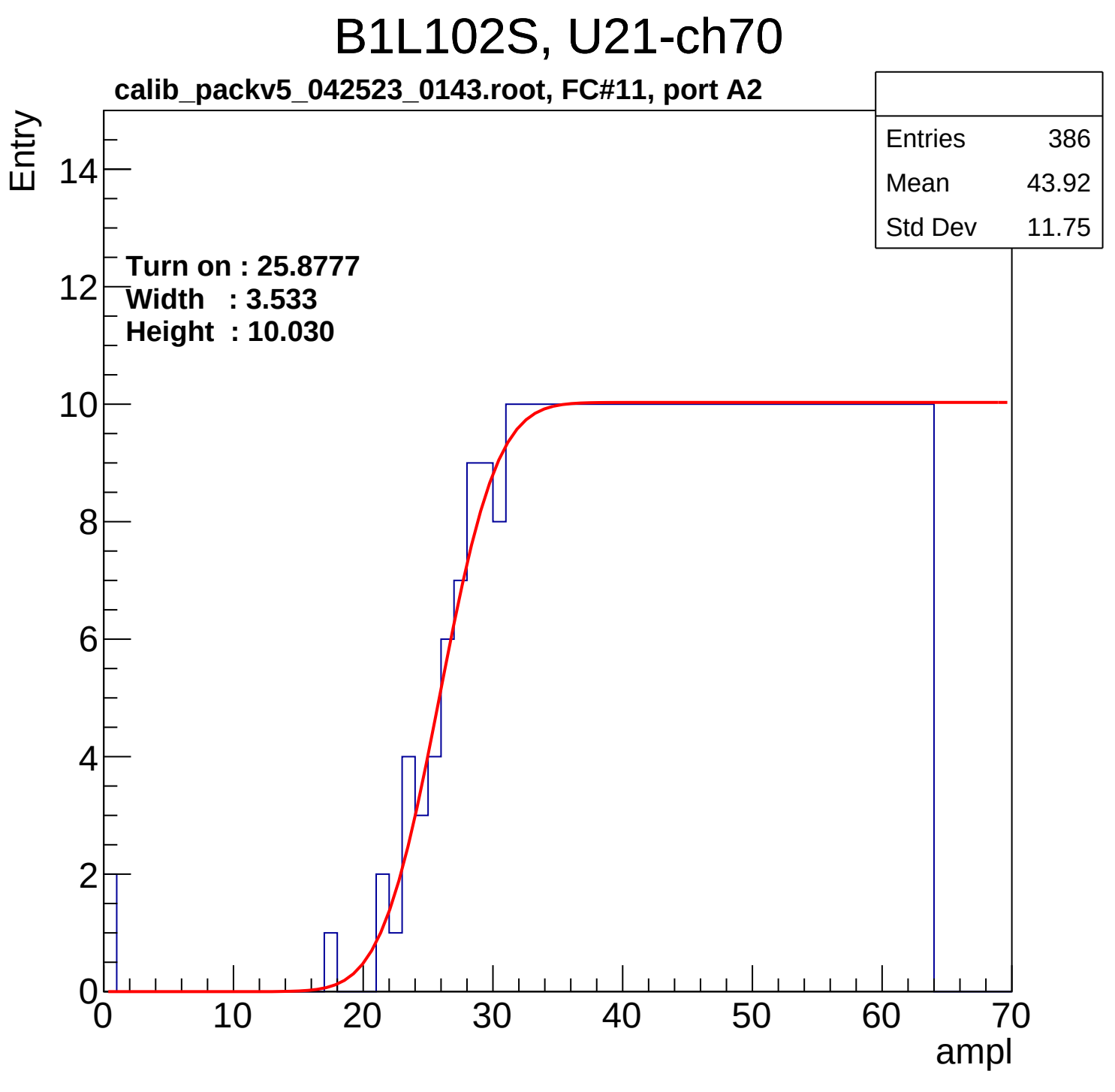
B1L102S, U21-ch70
calib_packv5_042523_0143.root, FC#11, port A2
Entries 386
Mean 43.92
Std Dev 11.75
Turn on : 25.8777
Width : 3.533
Height : 10.030
Entry
ampl
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2
4
6
8
10
12
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0
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20
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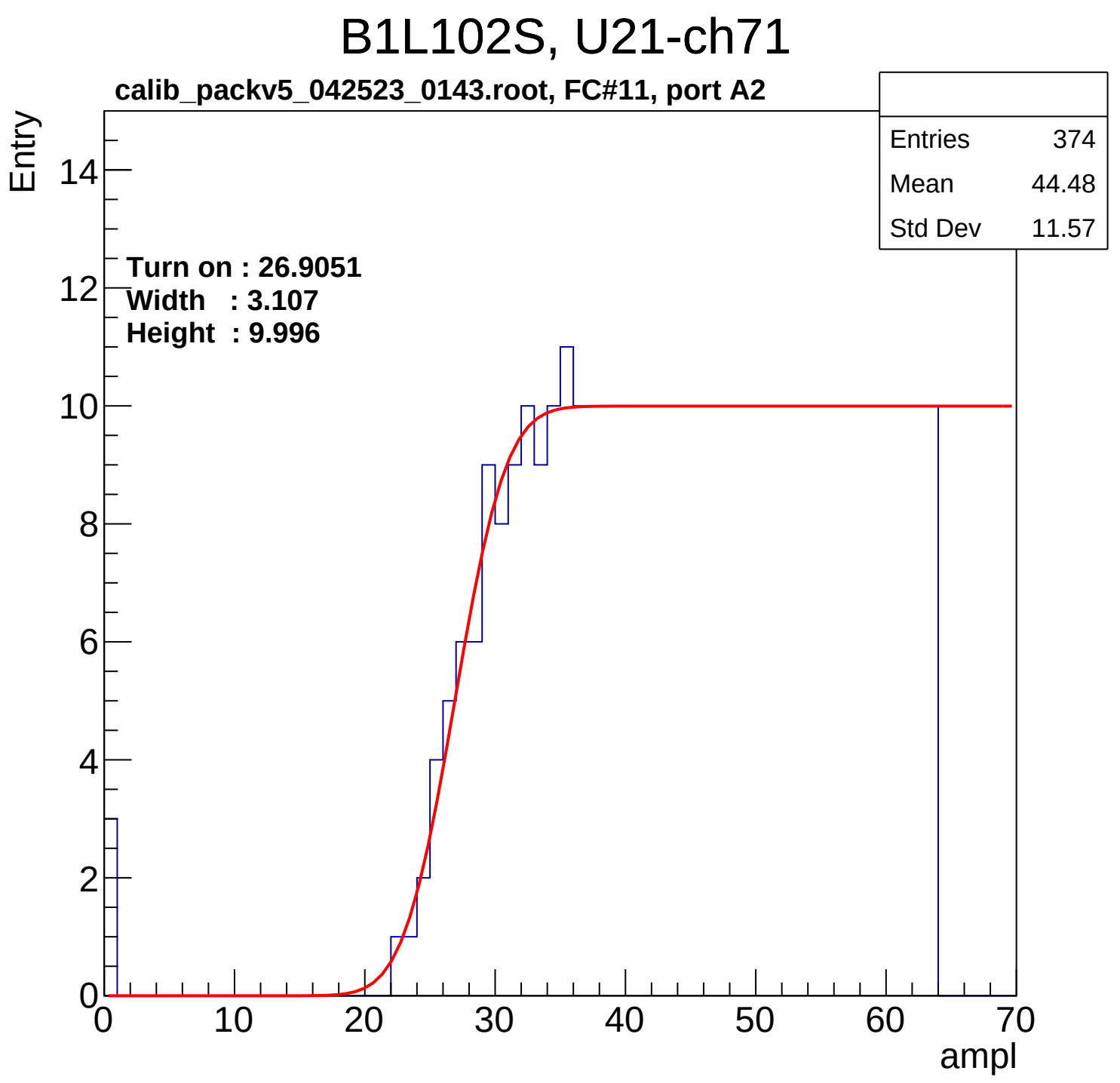
B1L102S, U21-ch71
calib_packv5_042523_0143.root, FC#11, port A2
Entries 374
Mean 44.48
Std Dev 11.57
Turn on : 26.9051
Width : 3.107
Height : 9.996
Entry
ampl
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4
6
8
10
12
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0
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20
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60
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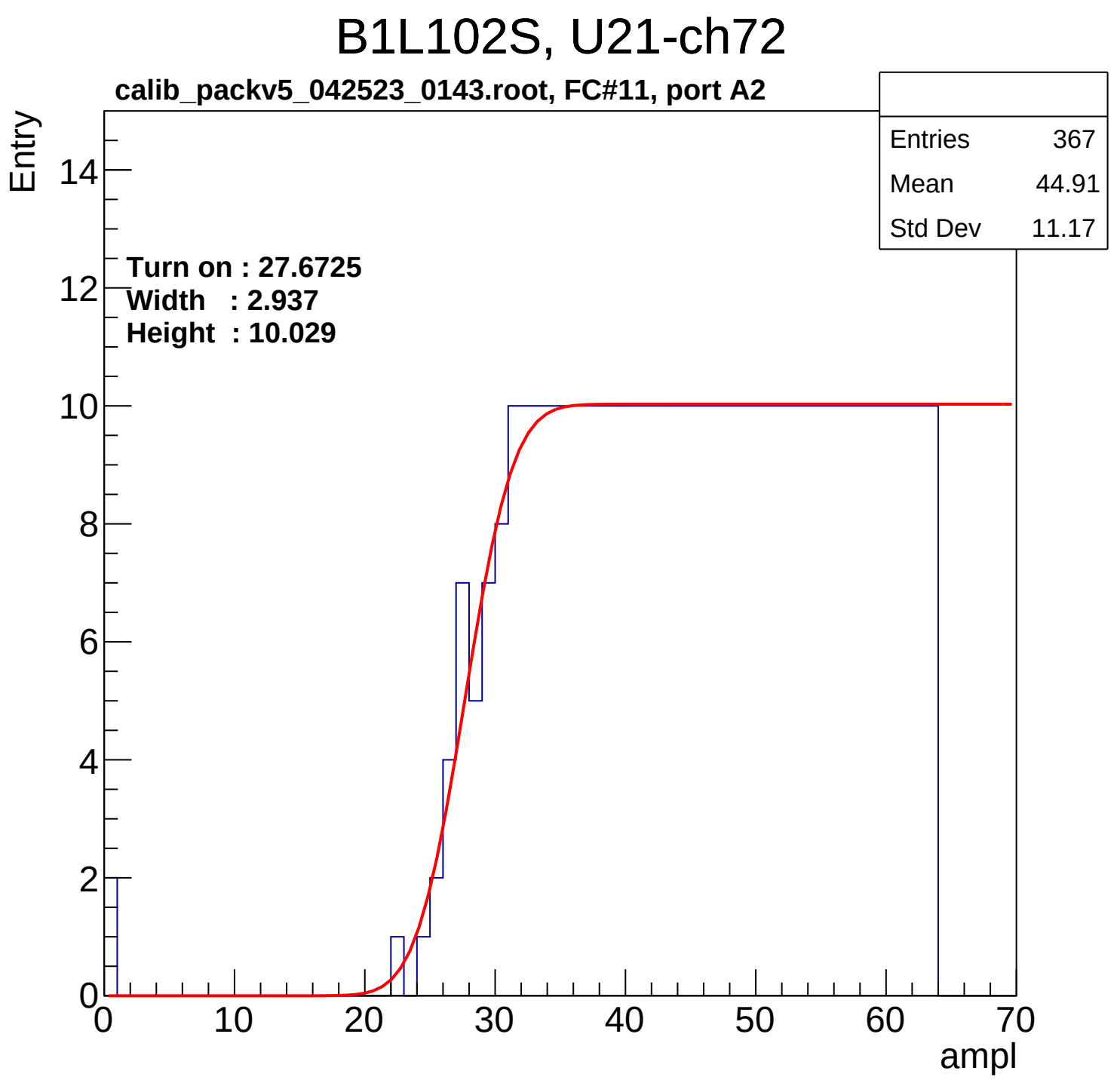
B1L102S, U21-ch72
calib_packv5_042523_0143.root, FC#11, port A2
Entries 367
Mean 44.91
Std Dev 11.17
Turn on : 27.6725
Width : 2.937
Height : 10.029
Entry
ampl
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2
4
6
8
10
12
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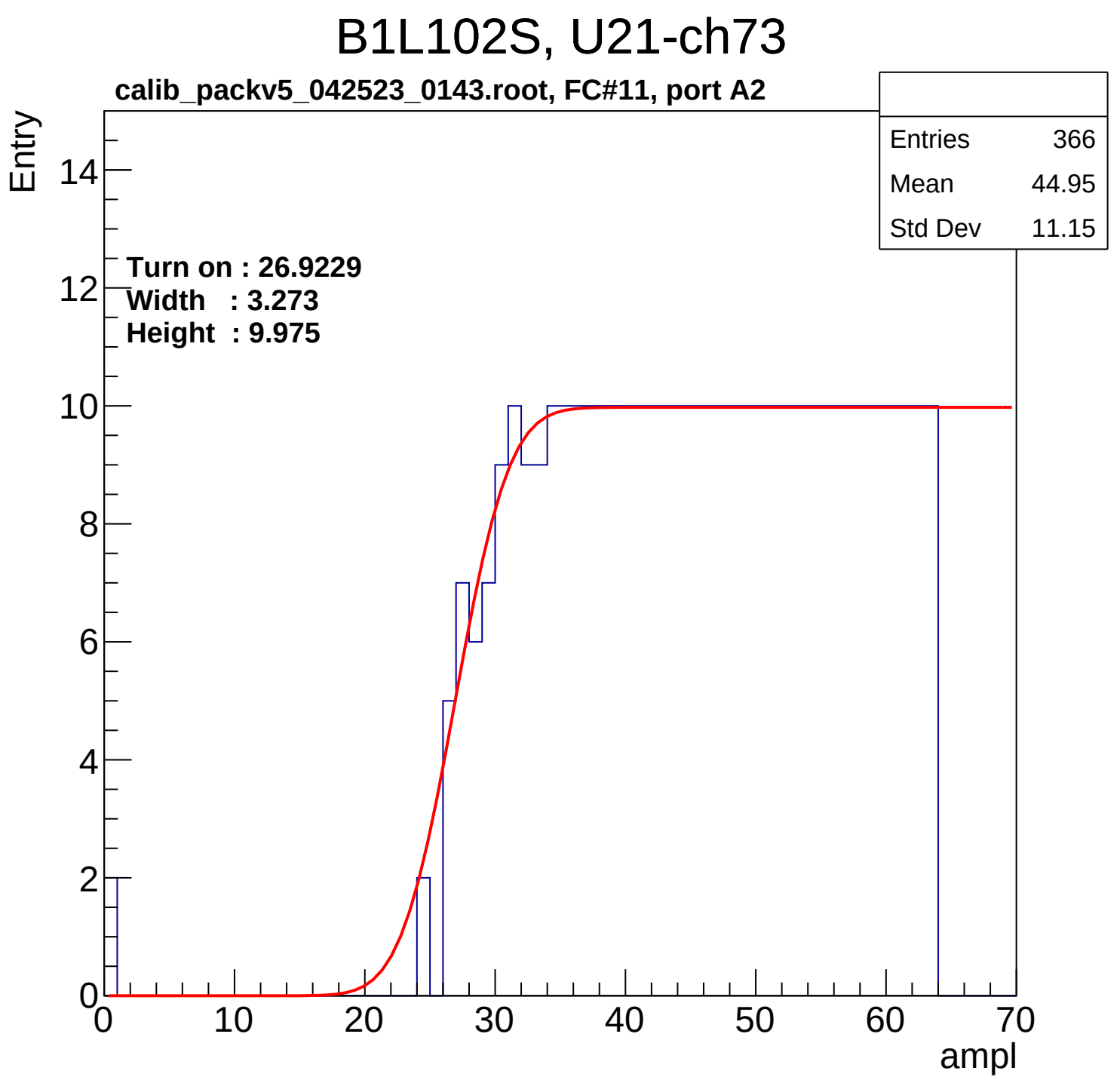
B1L102S, U21-ch73
calib_packv5_042523_0143.root, FC#11, port A2
Entries 366
Mean 44.95
Std Dev 11.15
Turn on : 26.9229
Width : 3.273
Height : 9.975
Entry
ampl
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6
8
10
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20
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60
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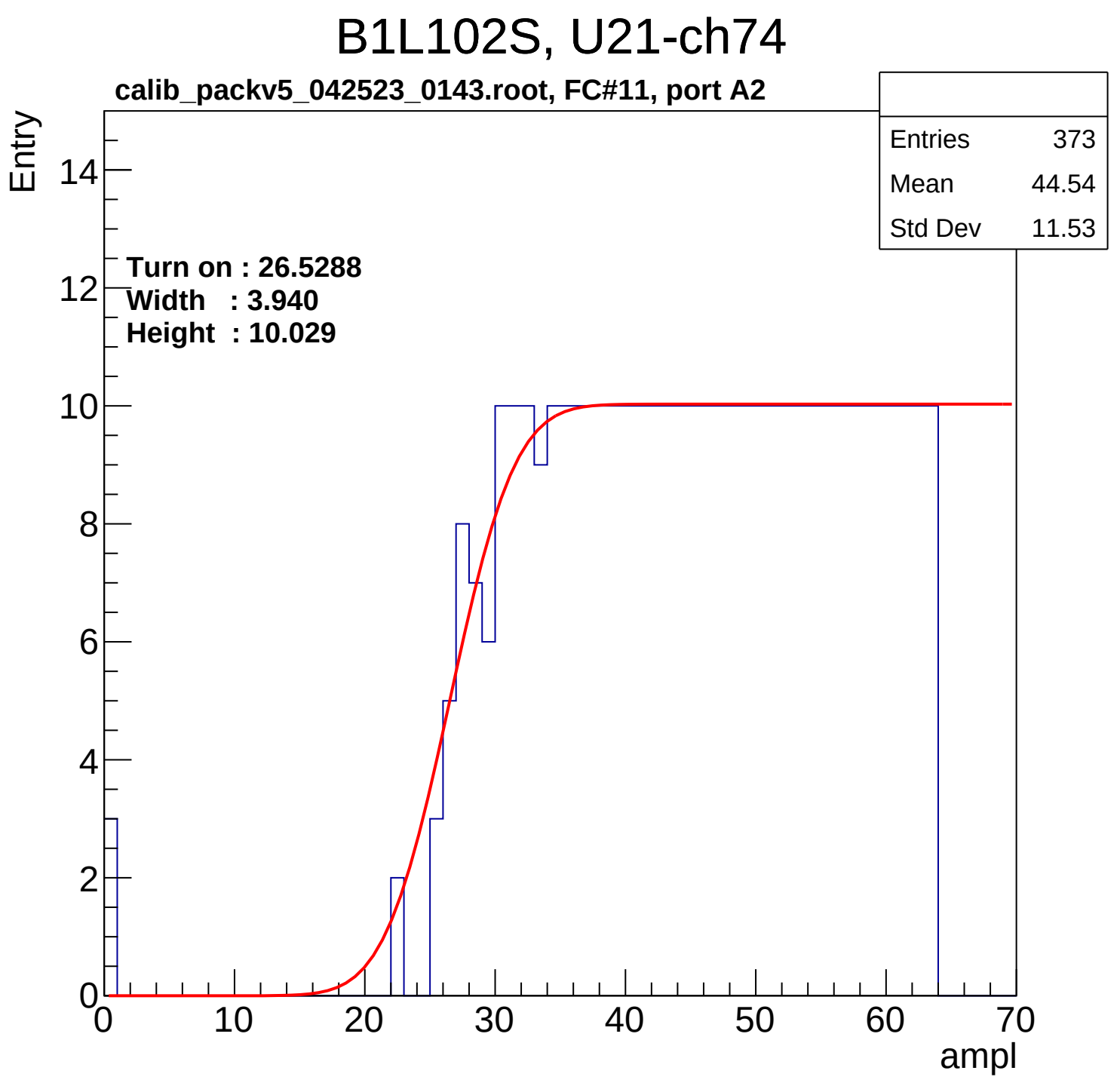
B1L102S, U21-ch74
calib_packv5_042523_0143.root, FC#11, port A2
Entries 373
Mean 44.54
Std Dev 11.53
Turn on : 26.5288
Width : 3.940
Height : 10.029
Entry
ampl
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8
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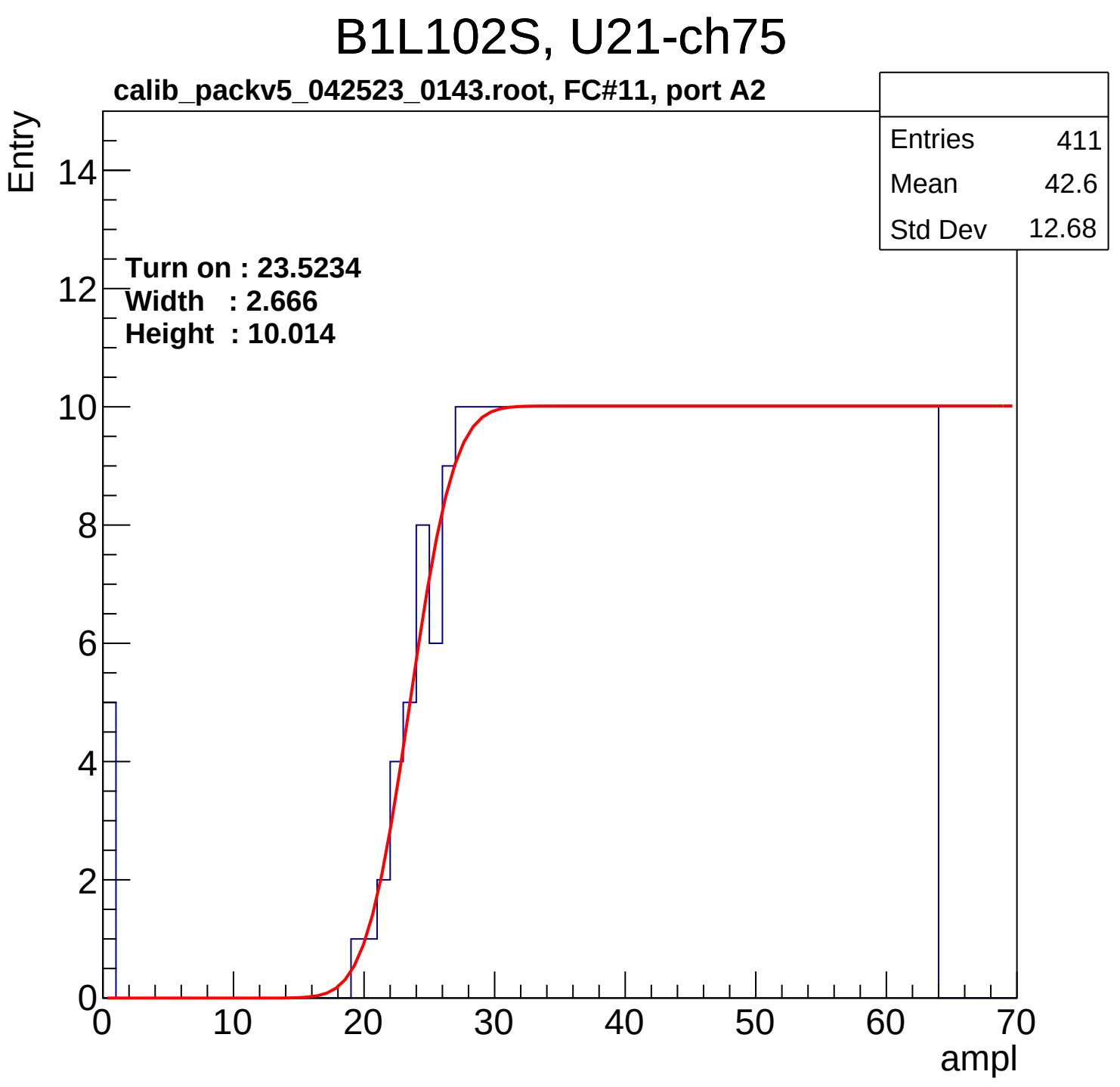
B1L102S, U21-ch75
calib_packv5_042523_0143.root, FC#11, port A2
Entries 411
Mean 42.6
Std Dev 12.68
Turn on : 23.5234
Width : 2.666
Height : 10.014
Entry
ampl
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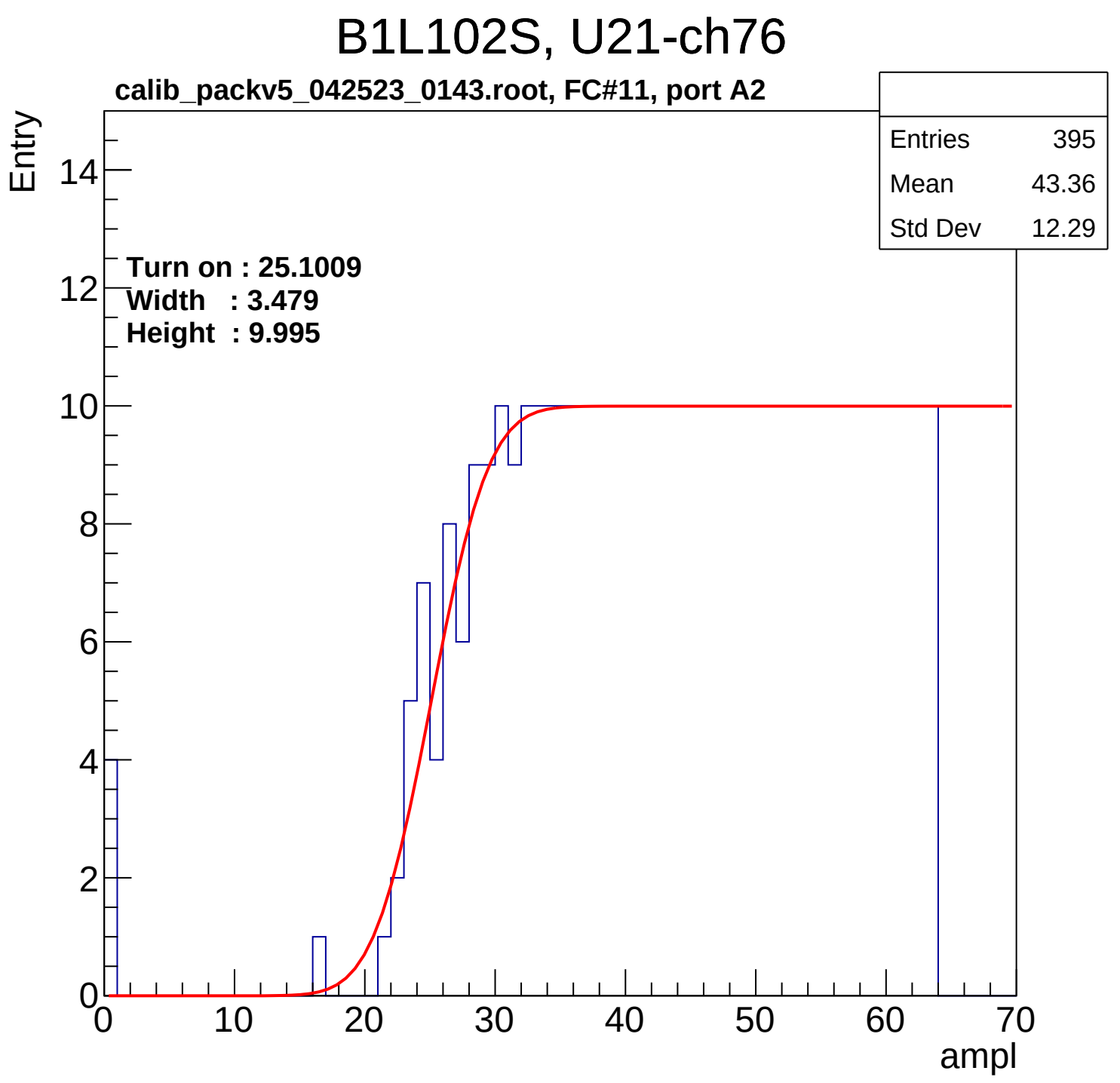
B1L102S, U21-ch76
calib_packv5_042523_0143.root, FC#11, port A2
Entries 395
Mean 43.36
Std Dev 12.29
Turn on : 25.1009
Width : 3.479
Height : 9.995
Entry
ampl
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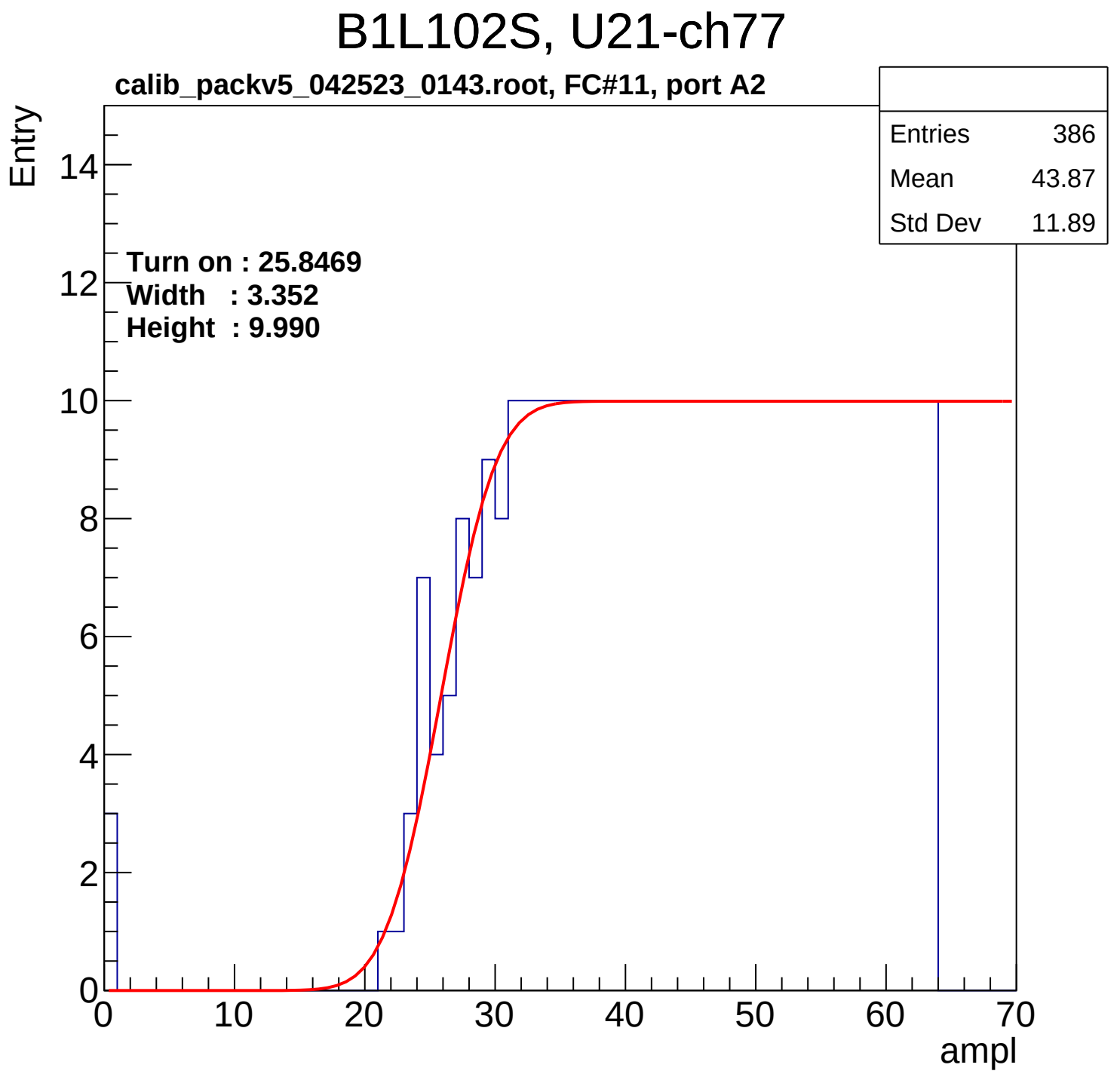
B1L102S, U21-ch77
calib_packv5_042523_0143.root, FC#11, port A2
Entries 386
Mean 43.87
Std Dev 11.89
Turn on : 25.8469
Width : 3.352
Height : 9.990
Entry
ampl
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8
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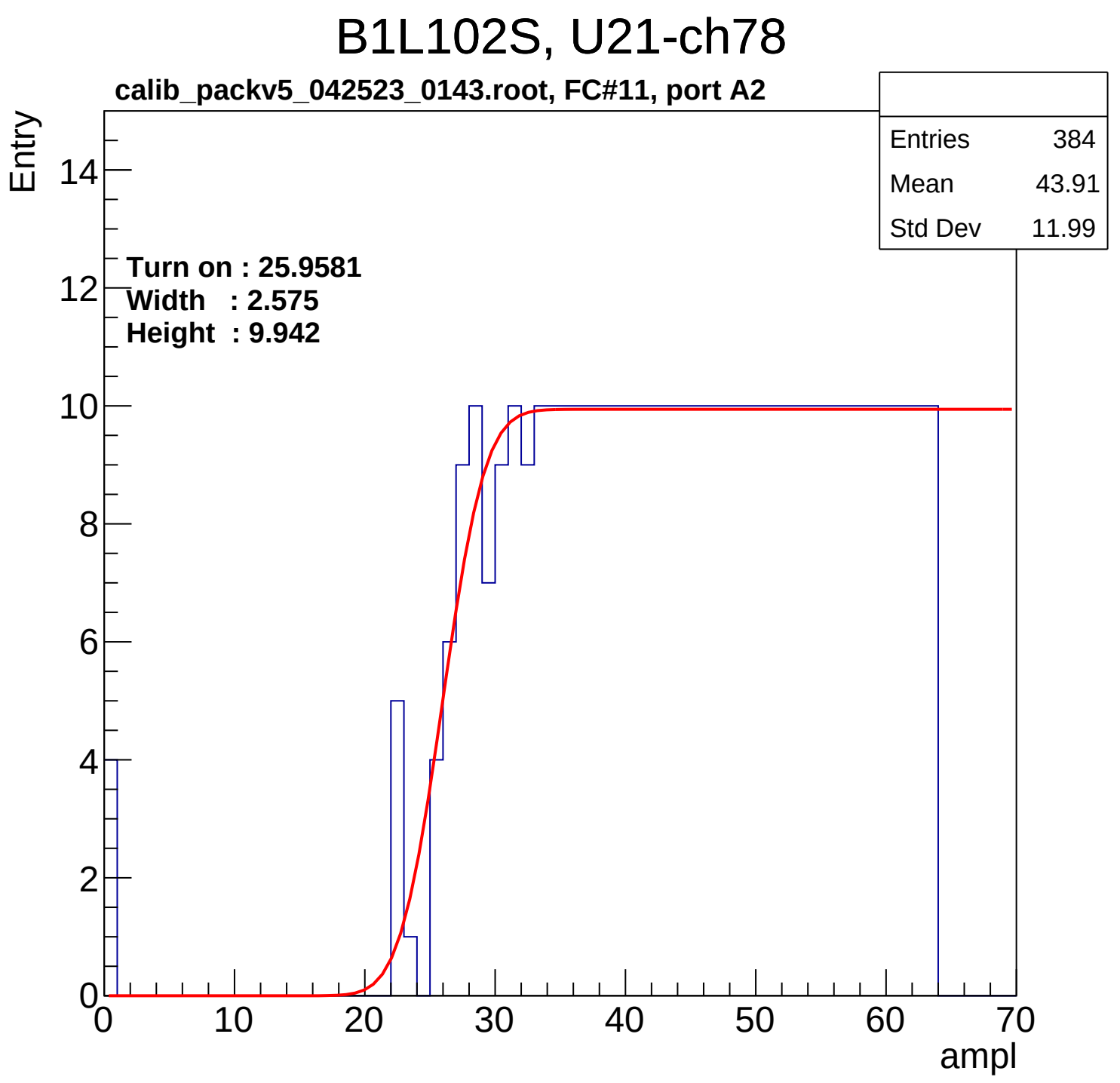
B1L102S, U21-ch78
calib_packv5_042523_0143.root, FC#11, port A2
Entries 384
Mean 43.91
Std Dev 11.99
Turn on : 25.9581
Width : 2.575
Height : 9.942
Entry
ampl
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8
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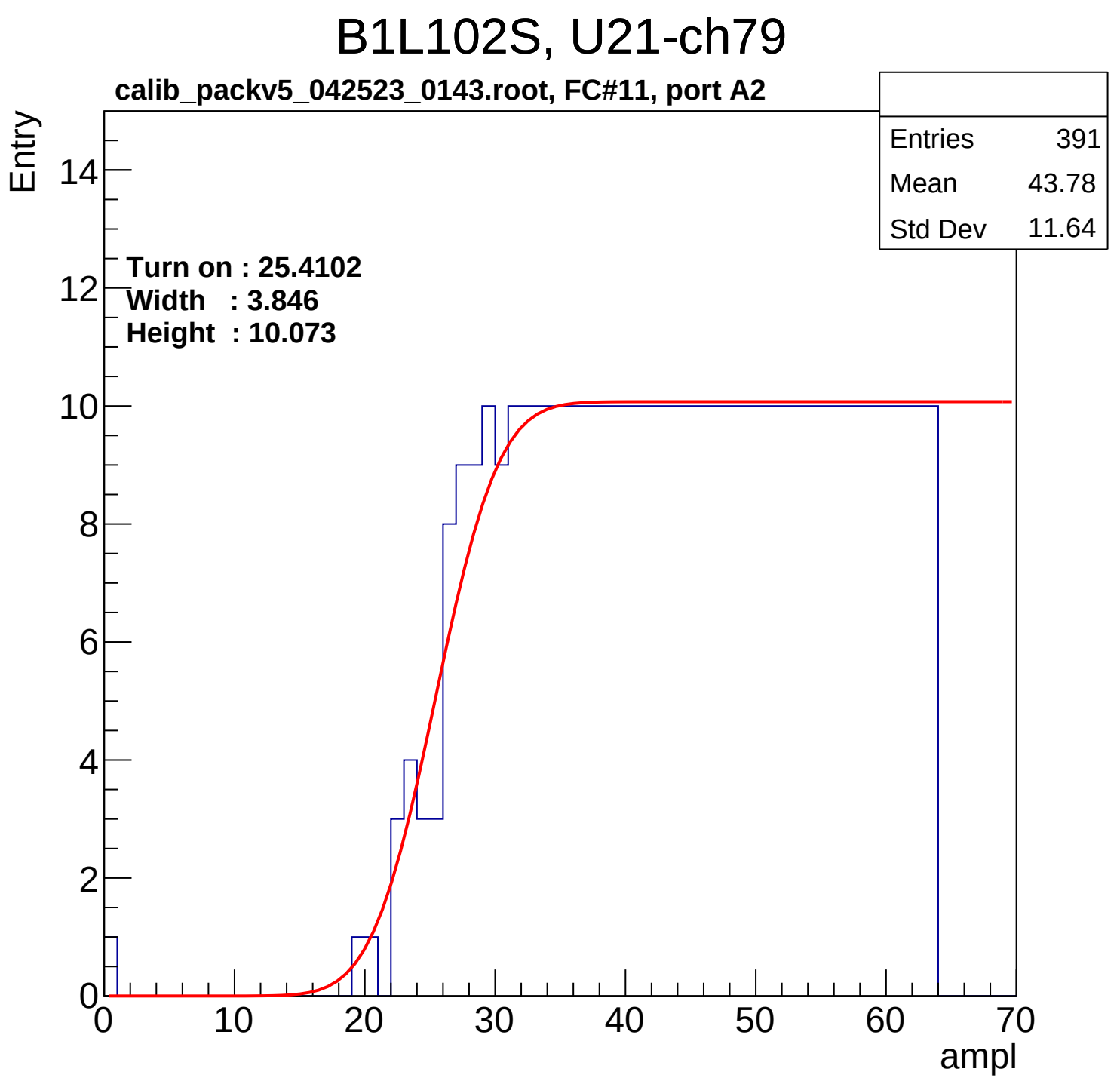
B1L102S, U21-ch79
calib_packv5_042523_0143.root, FC#11, port A2
Entries 391
Mean 43.78
Std Dev 11.64
Turn on : 25.4102
Width : 3.846
Height : 10.073
Entry
ampl
0
2
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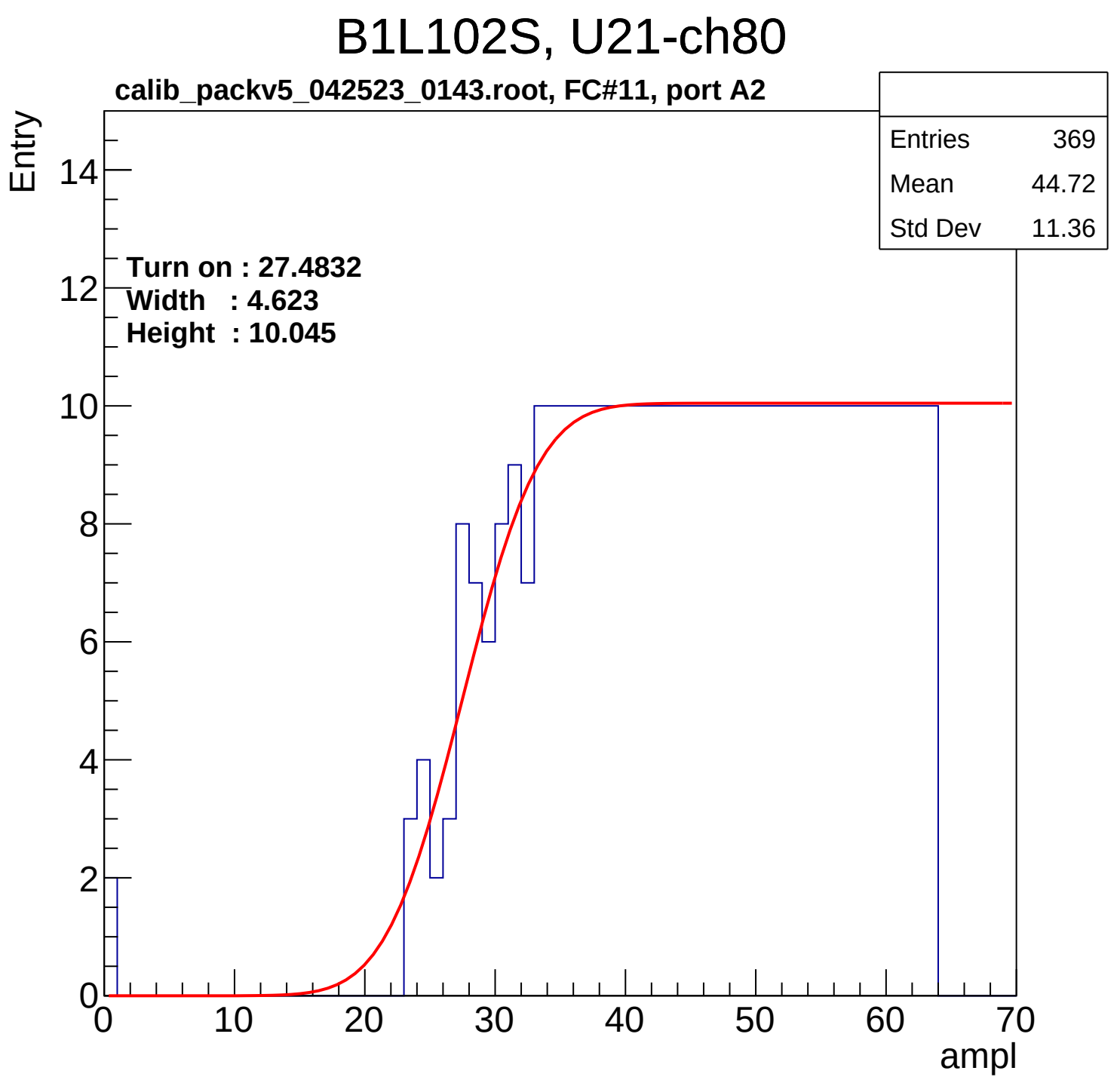
B1L102S, U21-ch80
calib_packv5_042523_0143.root, FC#11, port A2
Entries 369
Mean 44.72
Std Dev 11.36
Turn on : 27.4832
Width : 4.623
Height : 10.045
Entry
ampl
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4
6
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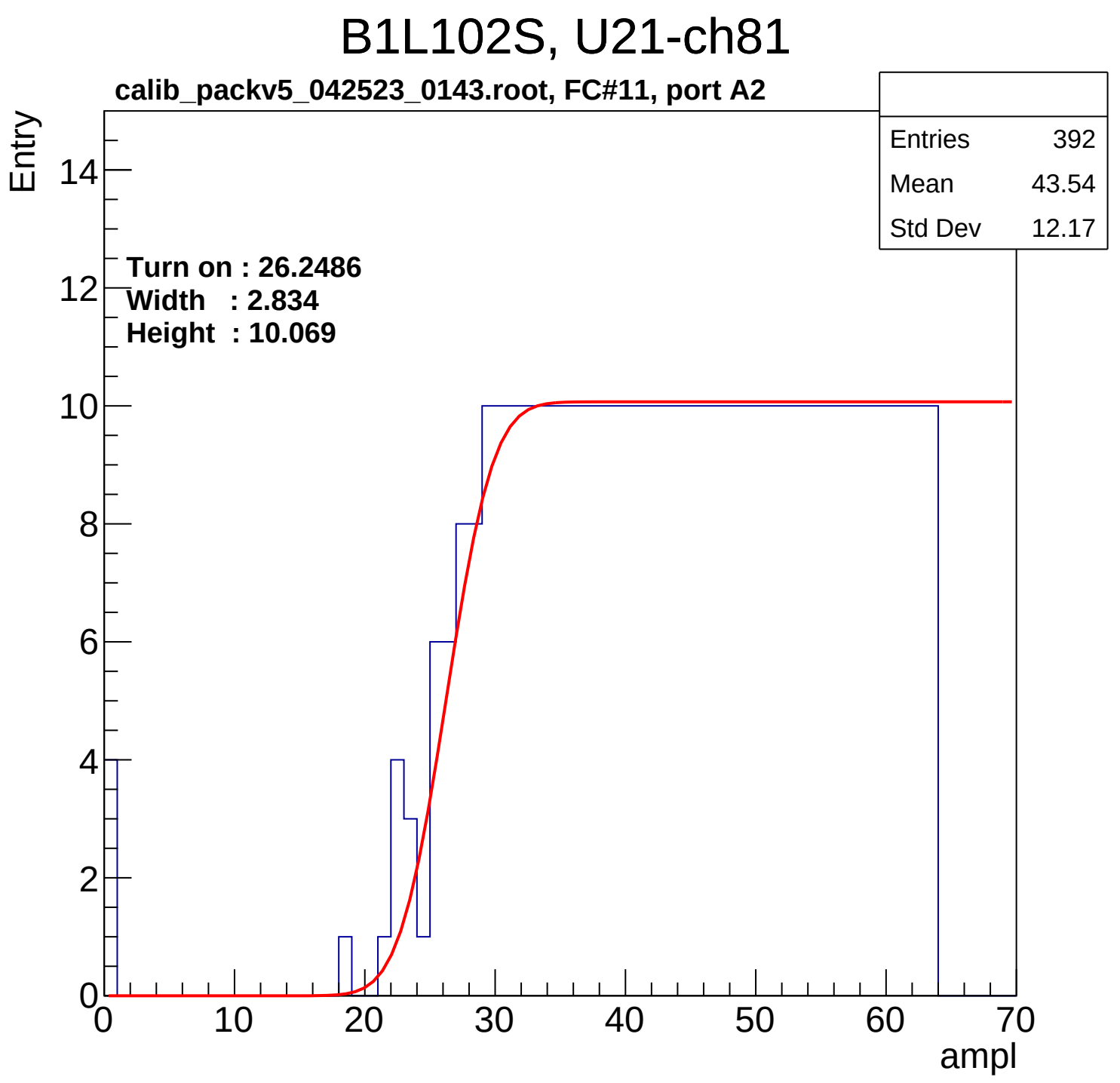
B1L102S, U21-ch81
calib_packv5_042523_0143.root, FC#11, port A2
Entries 392
Mean 43.54
Std Dev 12.17
Turn on : 26.2486
Width : 2.834
Height : 10.069
Entry
ampl
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2
4
6
8
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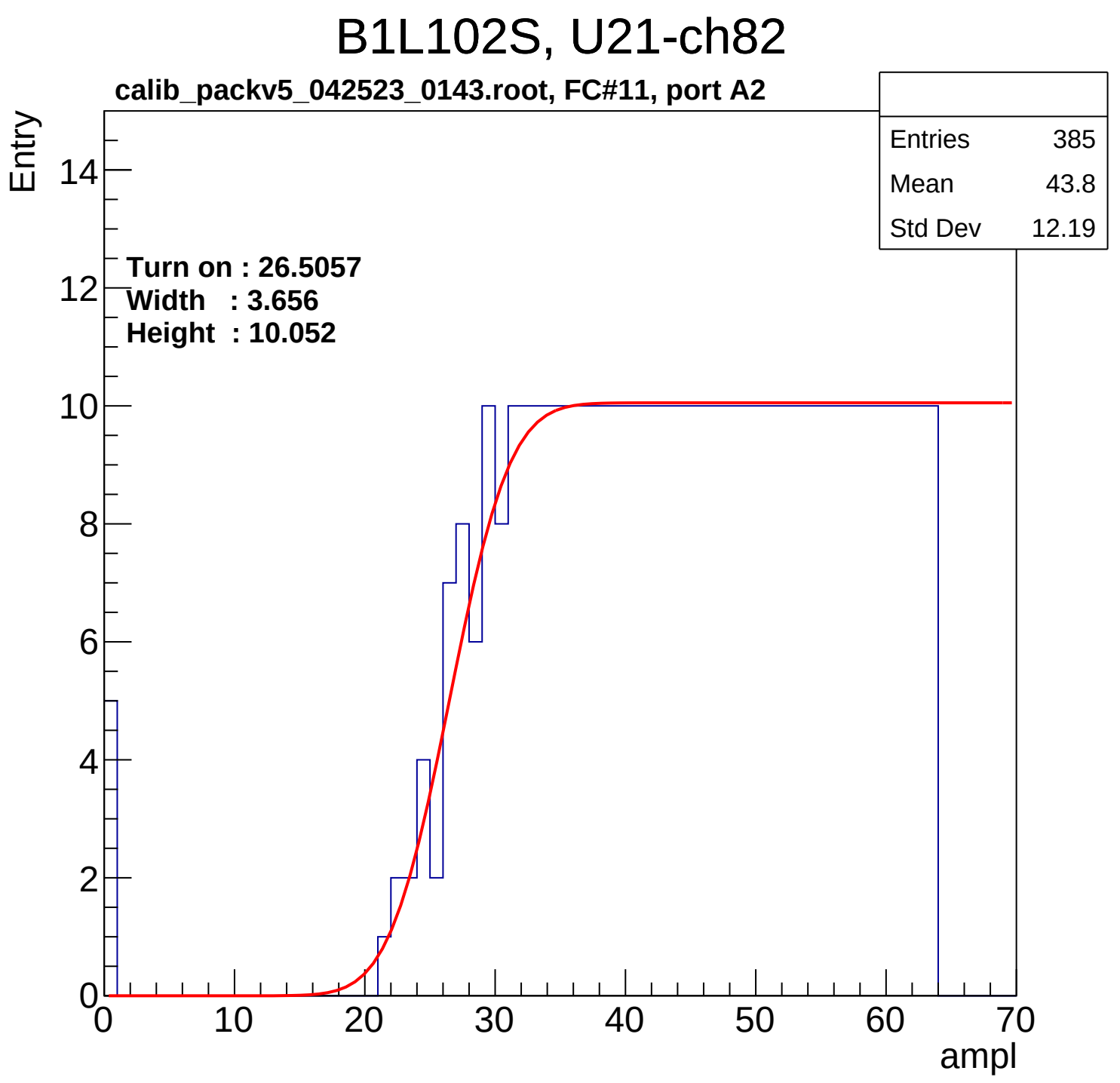
B1L102S, U21-ch82
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 43.8
Std Dev 12.19
Turn on : 26.5057
Width : 3.656
Height : 10.052
Entry
ampl
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4
6
8
10
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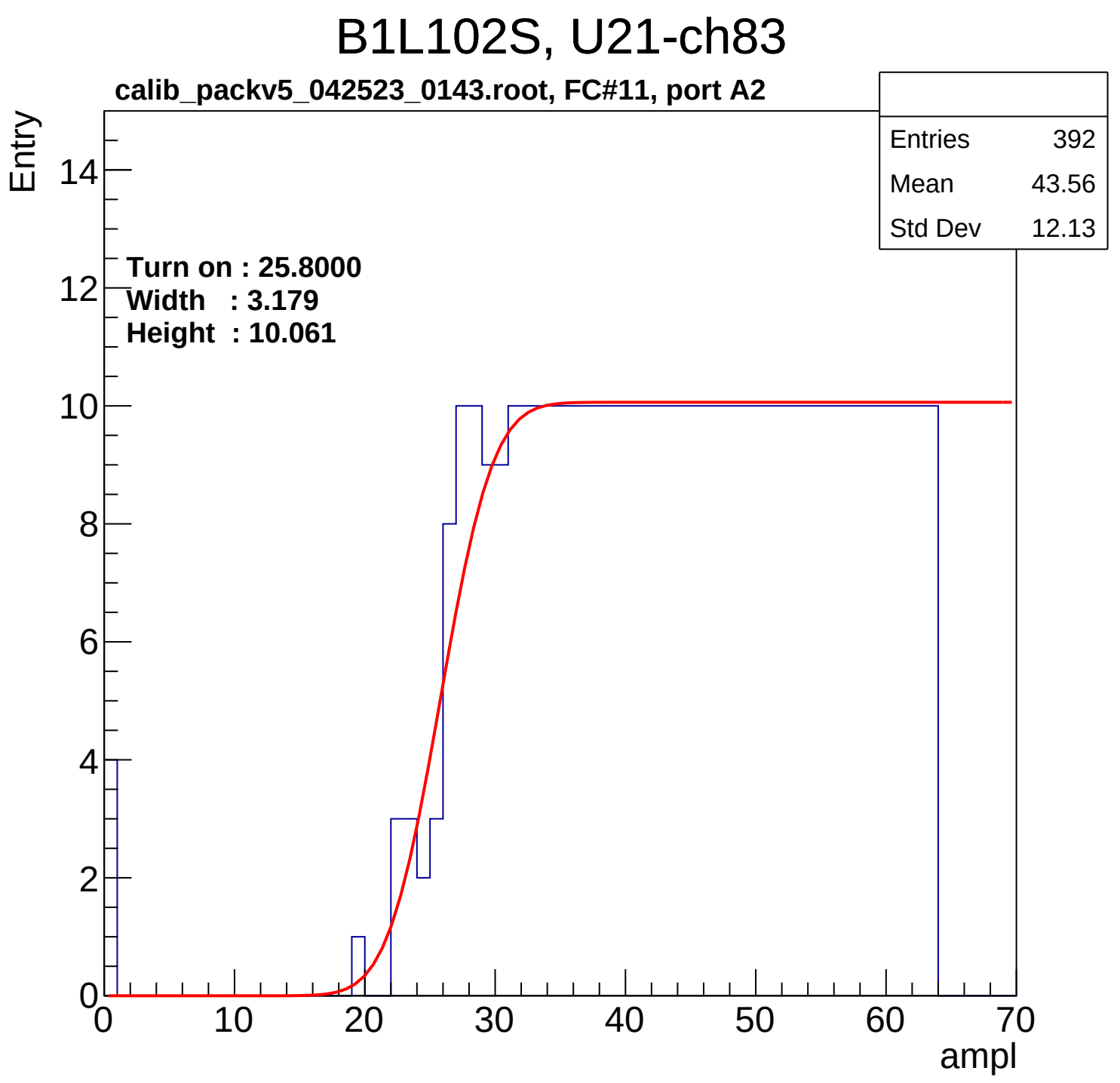
B1L102S, U21-ch83
calib_packv5_042523_0143.root, FC#11, port A2
Entries 392
Mean 43.56
Std Dev 12.13
Turn on : 25.8000
Width : 3.179
Height : 10.061
Entry
ampl
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6
8
10
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0
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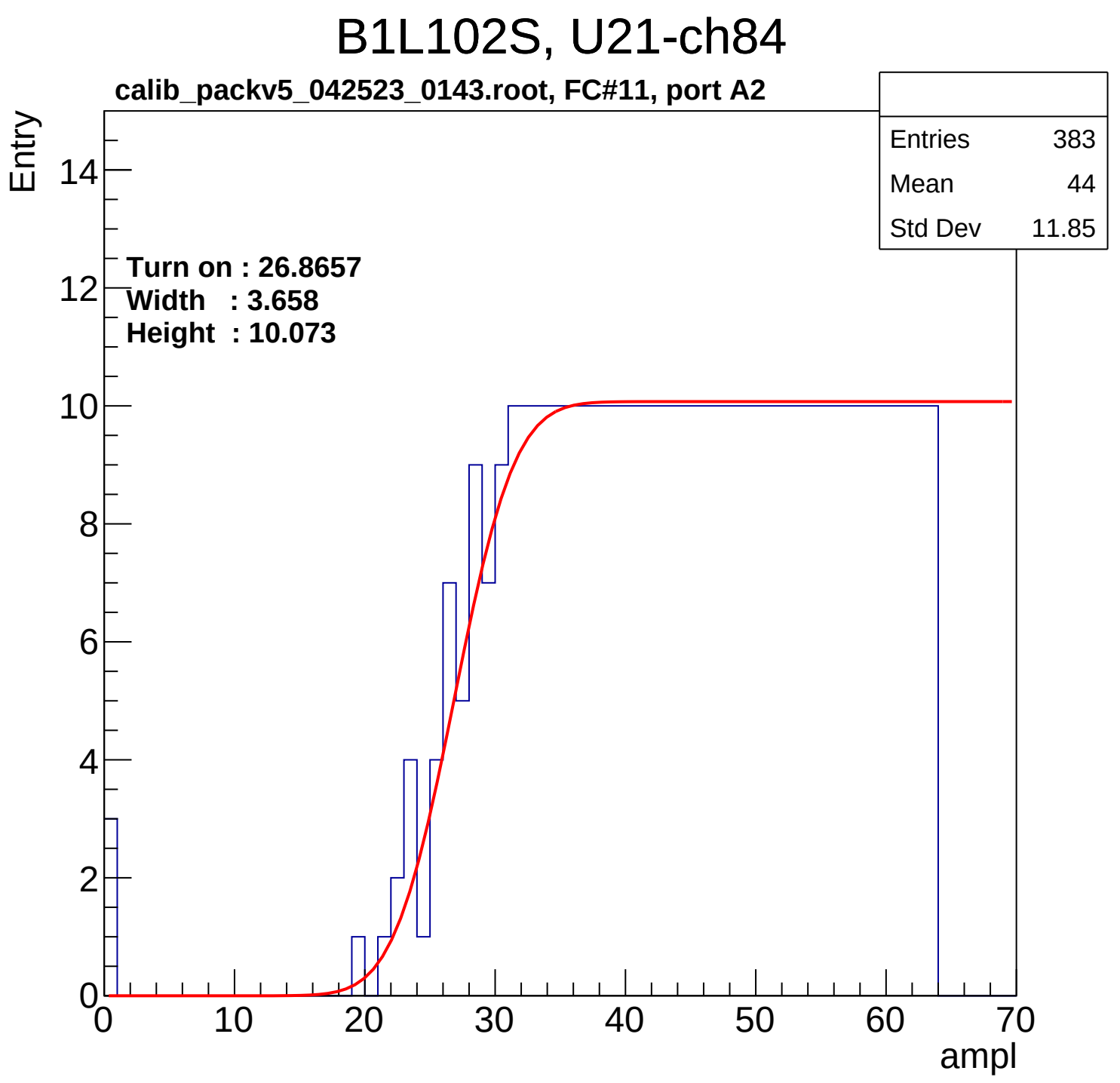
B1L102S, U21-ch84
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 44
Std Dev 11.85
Turn on : 26.8657
Width : 3.658
Height : 10.073
Entry
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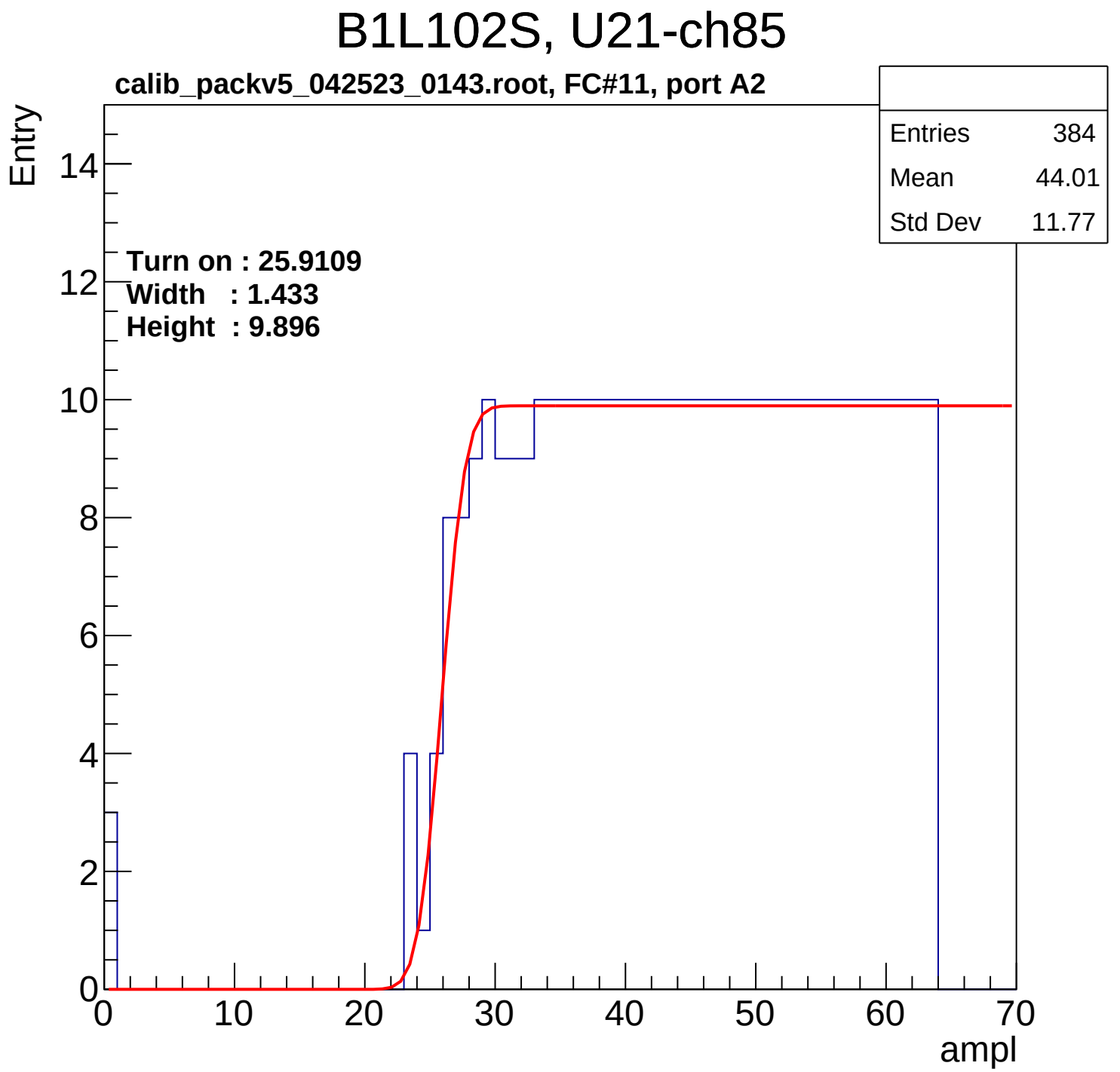
B1L102S, U21-ch85
calib_packv5_042523_0143.root, FC#11, port A2
Entries 384
Mean 44.01
Std Dev 11.77
Turn on : 25.9109
Width : 1.433
Height : 9.896
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ampl
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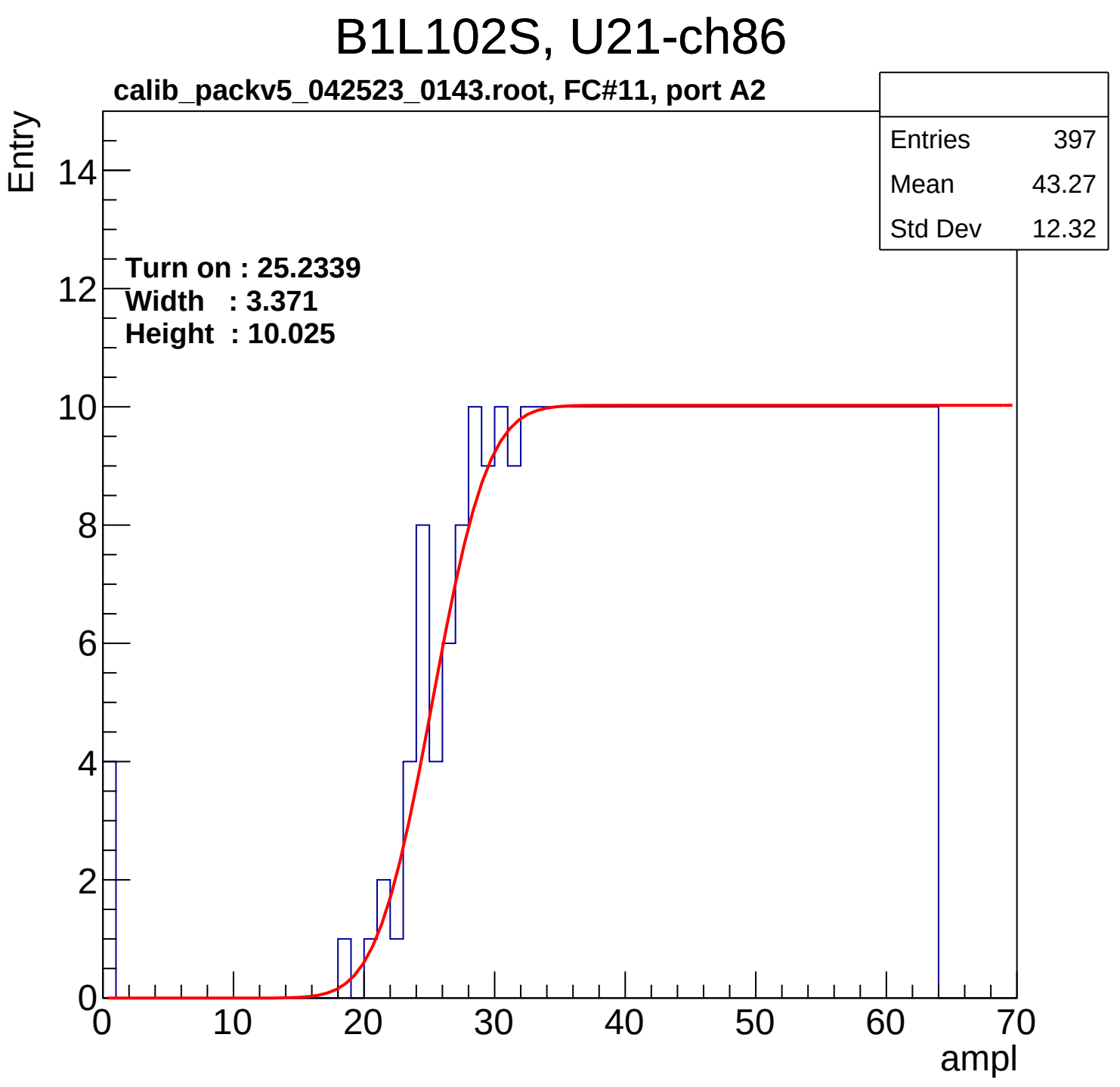
B1L102S, U21-ch86
calib_packv5_042523_0143.root, FC#11, port A2
Entries 397
Mean 43.27
Std Dev 12.32
Turn on : 25.2339
Width : 3.371
Height : 10.025
Entry
ampl
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6
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12
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10
20
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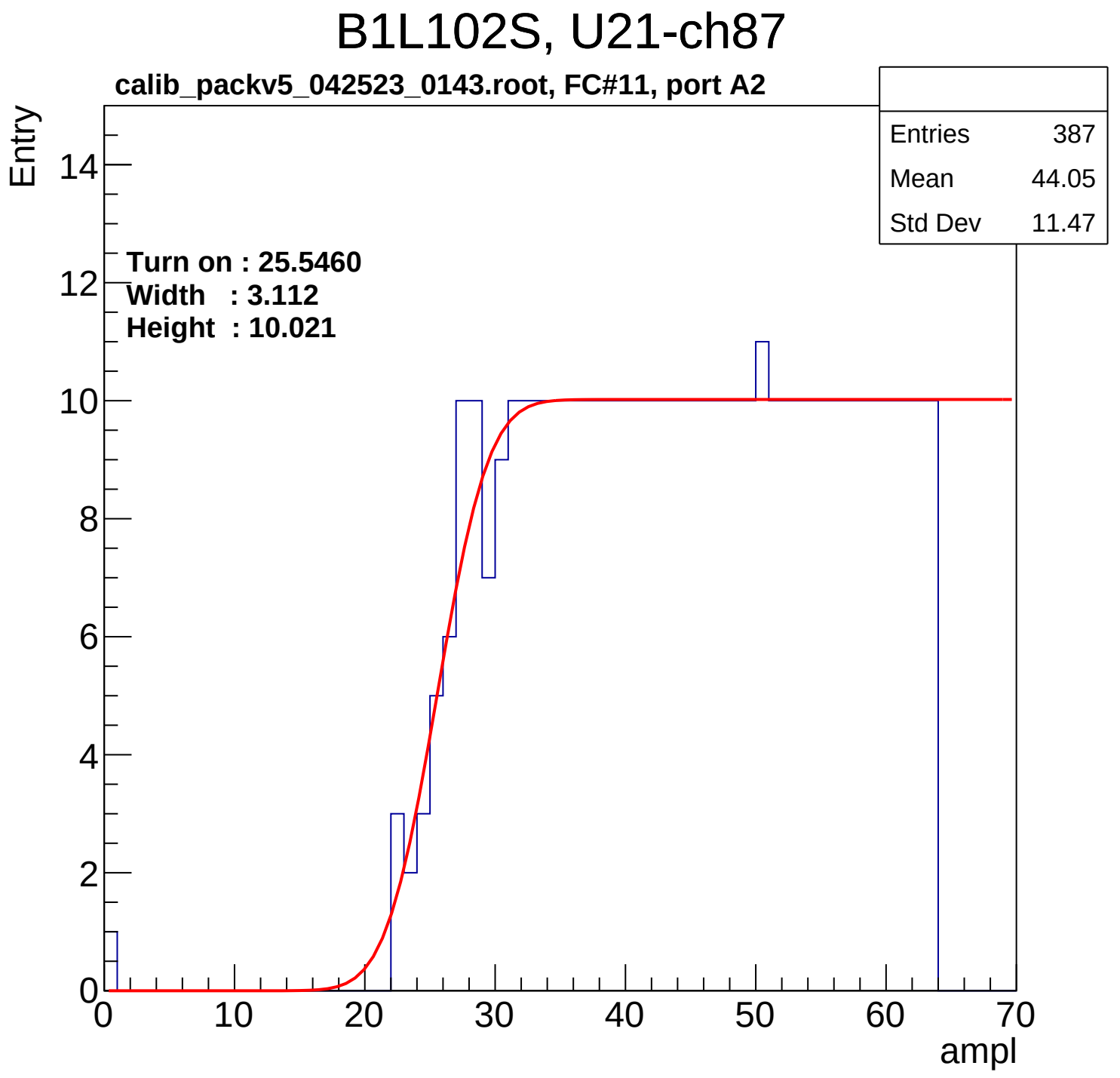
B1L102S, U21-ch87
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 44.05
Std Dev 11.47
Turn on : 25.5460
Width : 3.112
Height : 10.021
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ampl
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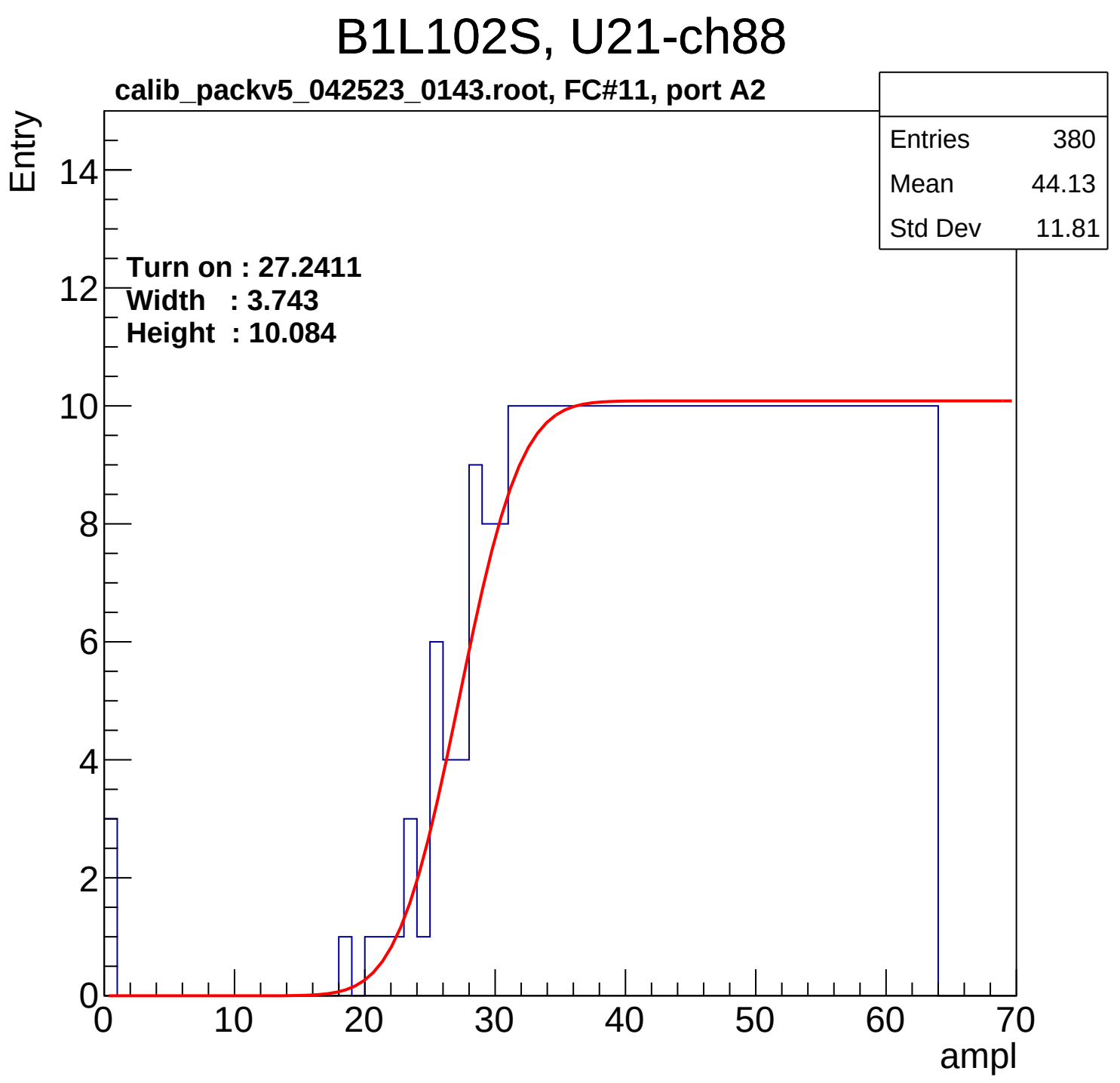
B1L102S, U21-ch88
calib_packv5_042523_0143.root, FC#11, port A2
Entries 380
Mean 44.13
Std Dev 11.81
Turn on : 27.2411
Width : 3.743
Height : 10.084
Entry
ampl
0
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4
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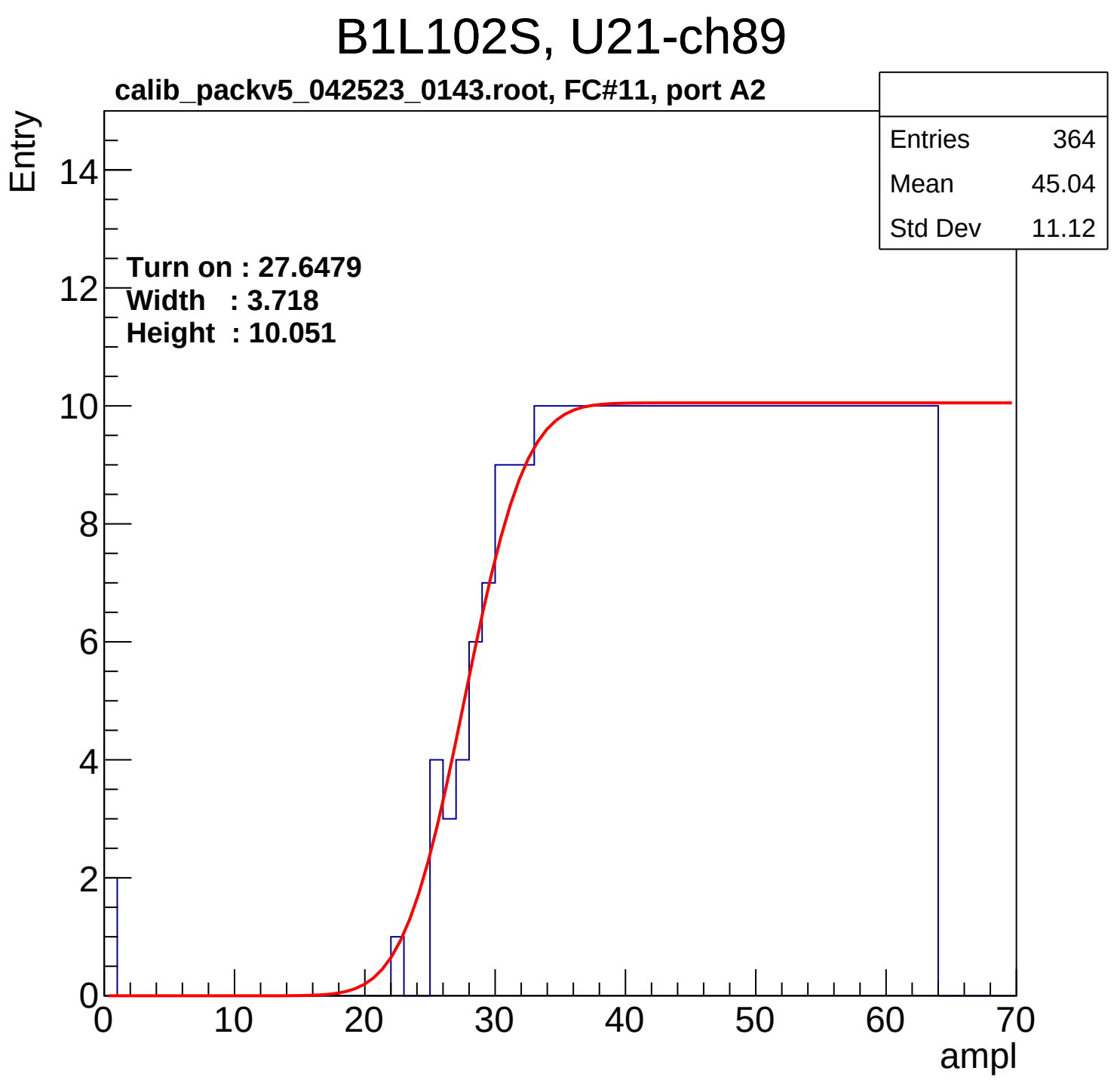
B1L102S, U21-ch89
calib_packv5_042523_0143.root, FC#11, port A2
Entries 364
Mean 45.04
Std Dev 11.12
Turn on : 27.6479
Width : 3.718
Height : 10.051
Entry
ampl
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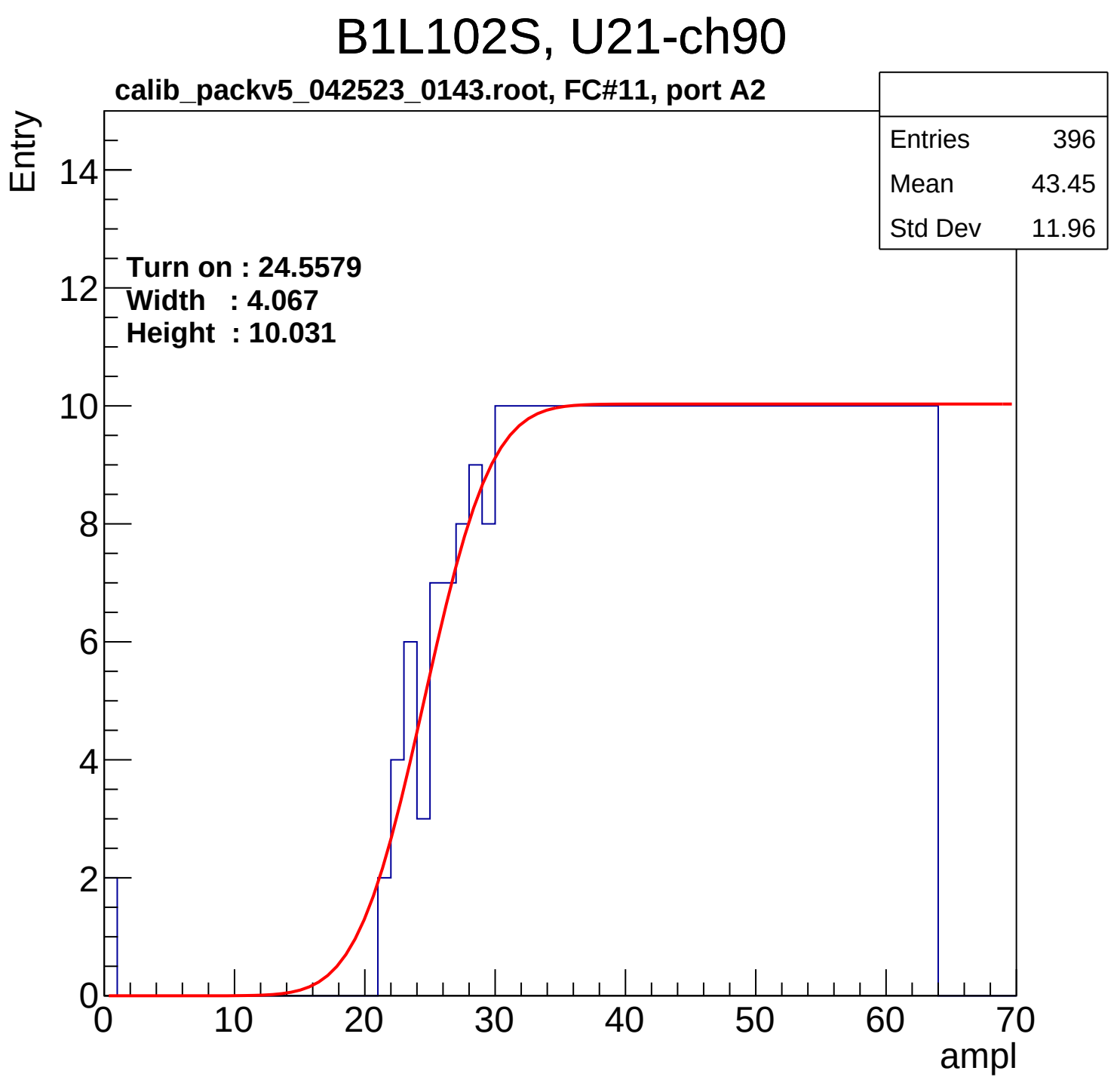
B1L102S, U21-ch90
calib_packv5_042523_0143.root, FC#11, port A2
Entries 396
Mean 43.45
Std Dev 11.96
Turn on : 24.5579
Width : 4.067
Height : 10.031
Entry
ampl
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2
4
6
8
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12
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0
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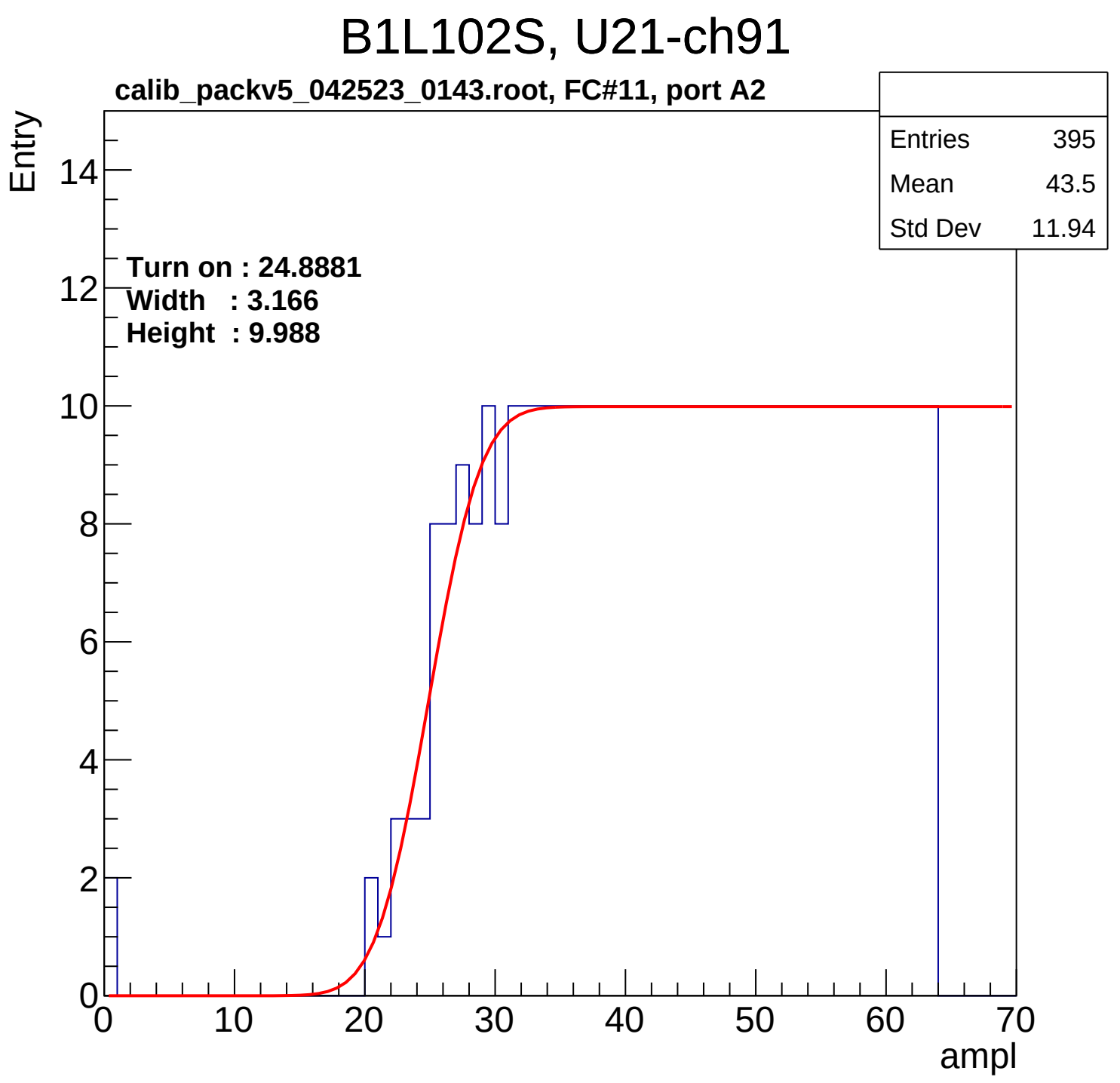
B1L102S, U21-ch91
calib_packv5_042523_0143.root, FC#11, port A2
Entries 395
Mean 43.5
Std Dev 11.94
Turn on : 24.8881
Width : 3.166
Height : 9.988
Entry
ampl
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2
4
6
8
10
12
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0
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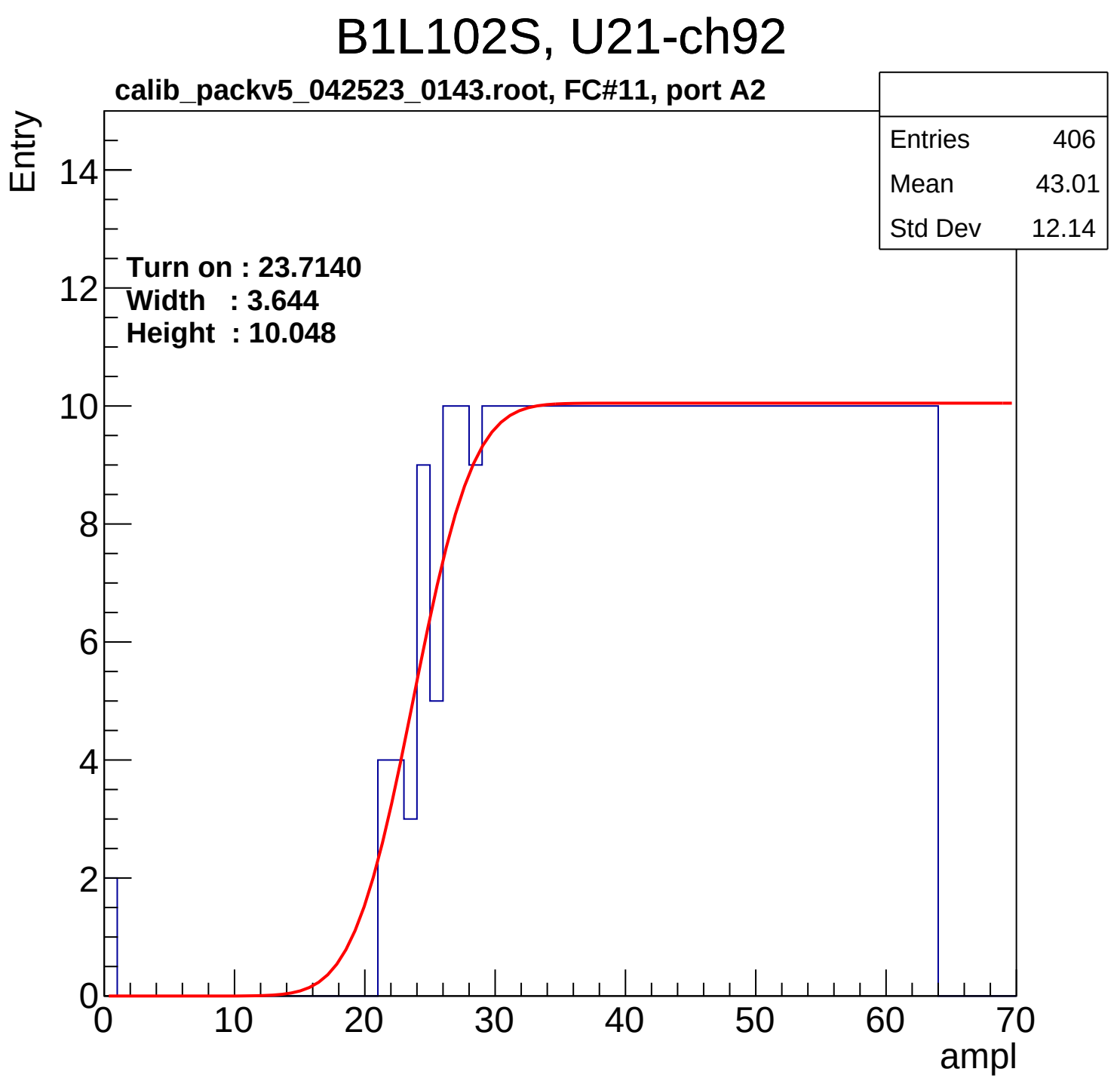
B1L102S, U21-ch92
calib_packv5_042523_0143.root, FC#11, port A2
Entries 406
Mean 43.01
Std Dev 12.14
Turn on : 23.7140
Width : 3.644
Height : 10.048
Entry
ampl
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4
6
8
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12
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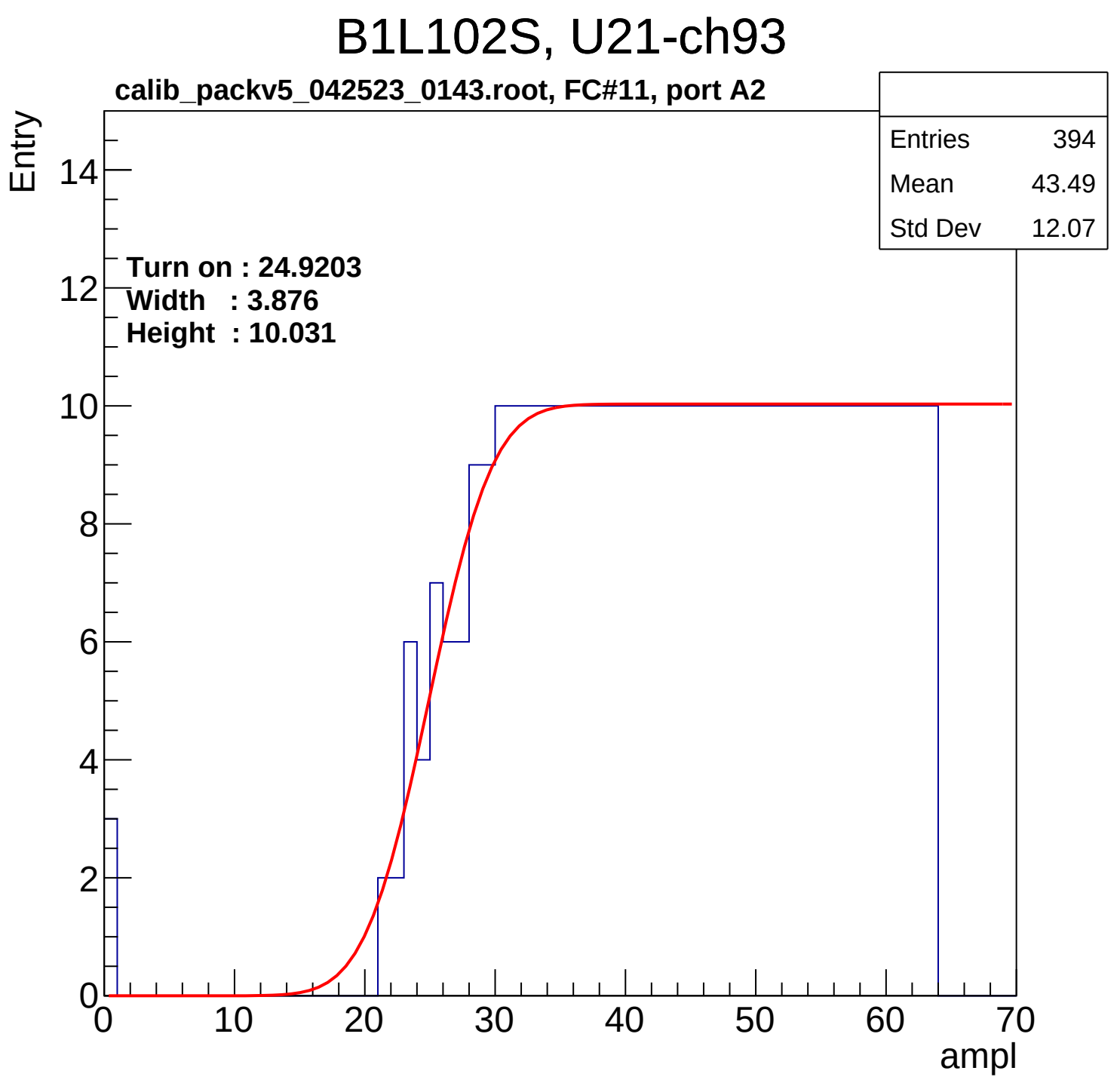
B1L102S, U21-ch93
calib_packv5_042523_0143.root, FC#11, port A2
Entries 394
Mean 43.49
Std Dev 12.07
Turn on : 24.9203
Width : 3.876
Height : 10.031
Entry
ampl
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2
4
6
8
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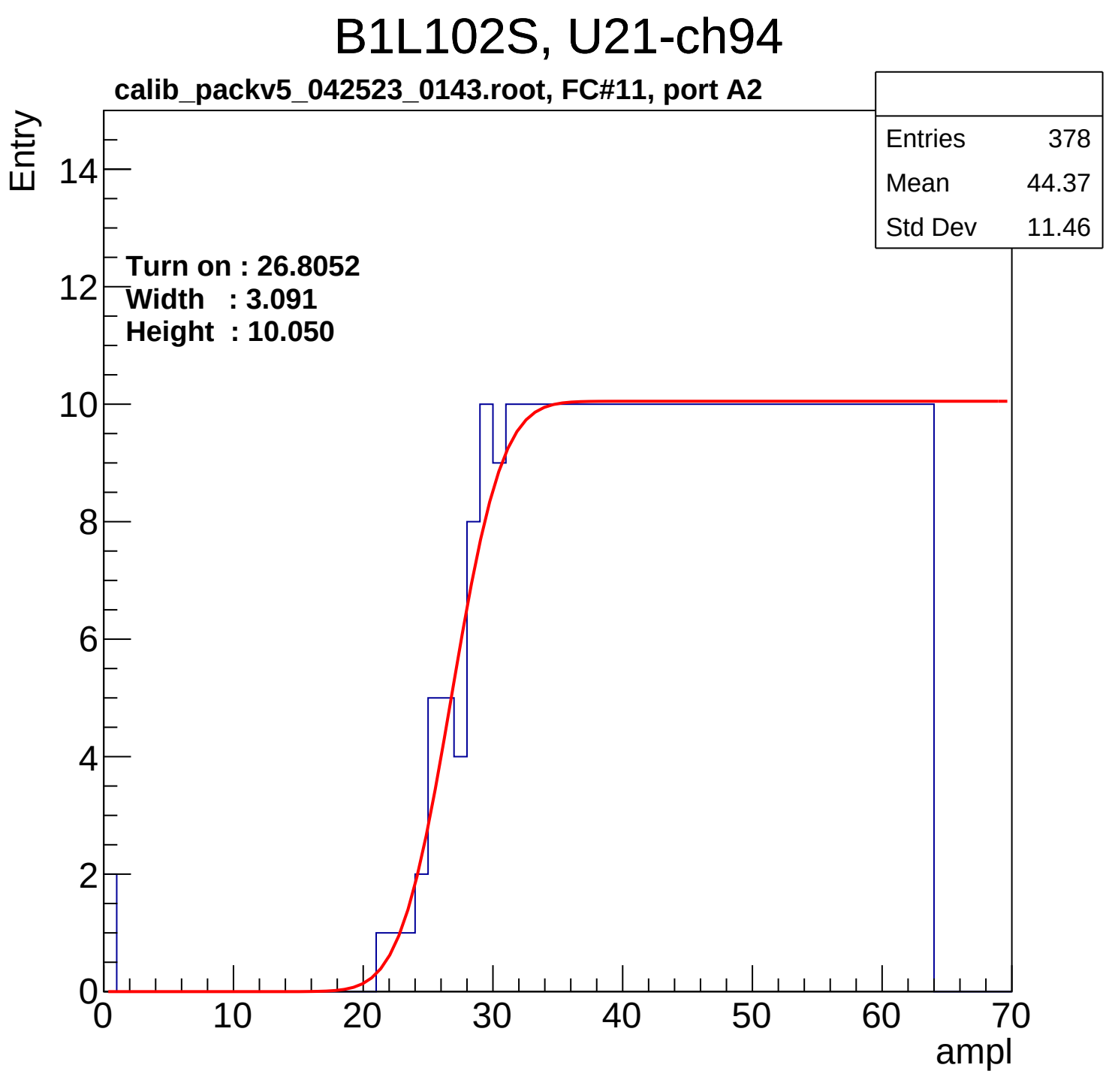
B1L102S, U21-ch94
calib_packv5_042523_0143.root, FC#11, port A2
Entries 378
Mean 44.37
Std Dev 11.46
Turn on : 26.8052
Width : 3.091
Height : 10.050
Entry
ampl
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6
8
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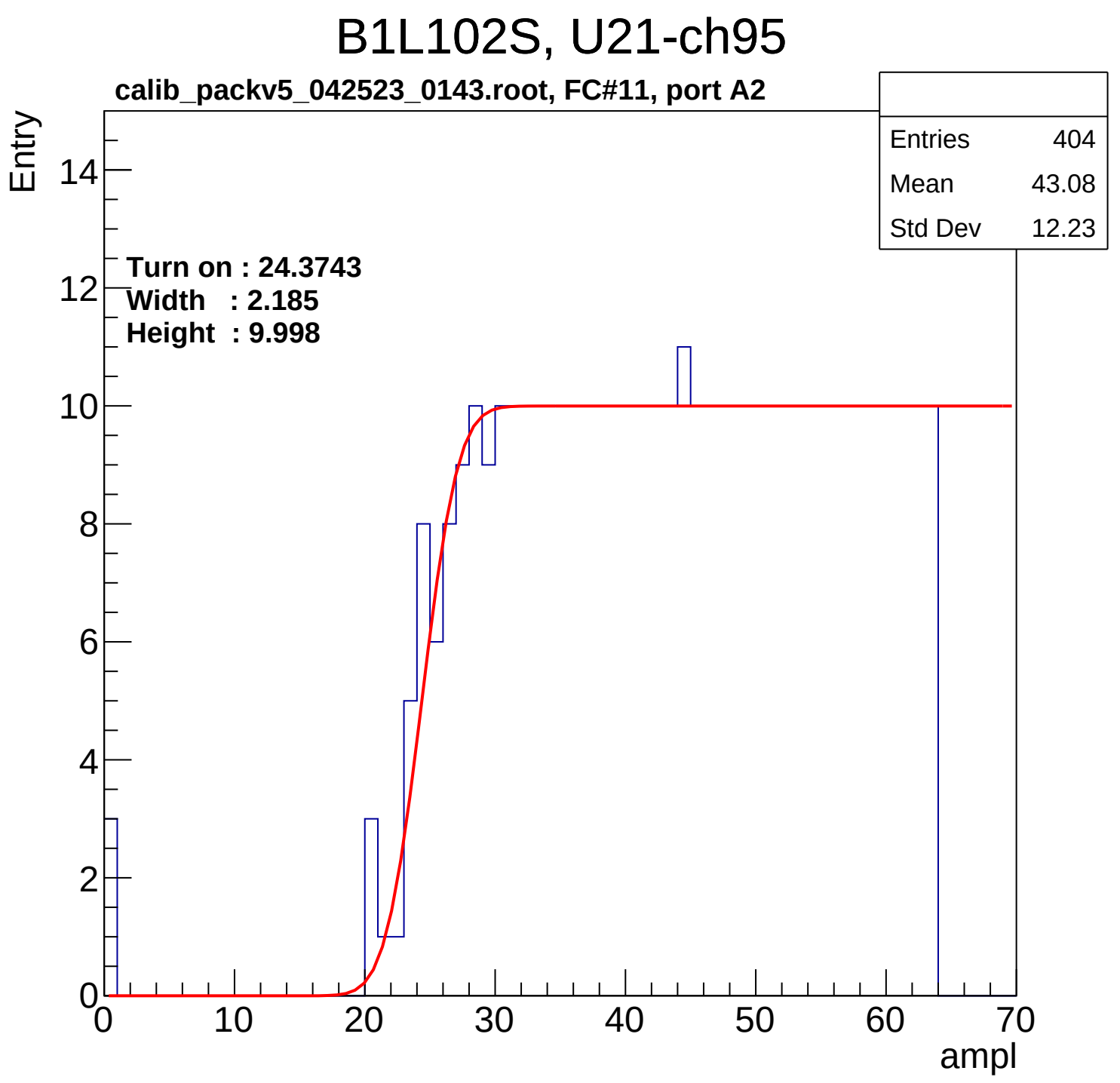
B1L102S, U21-ch95
calib_packv5_042523_0143.root, FC#11, port A2
Entries 404
Mean 43.08
Std Dev 12.23
Turn on : 24.3743
Width : 2.185
Height : 9.998
Entry
ampl
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6
8
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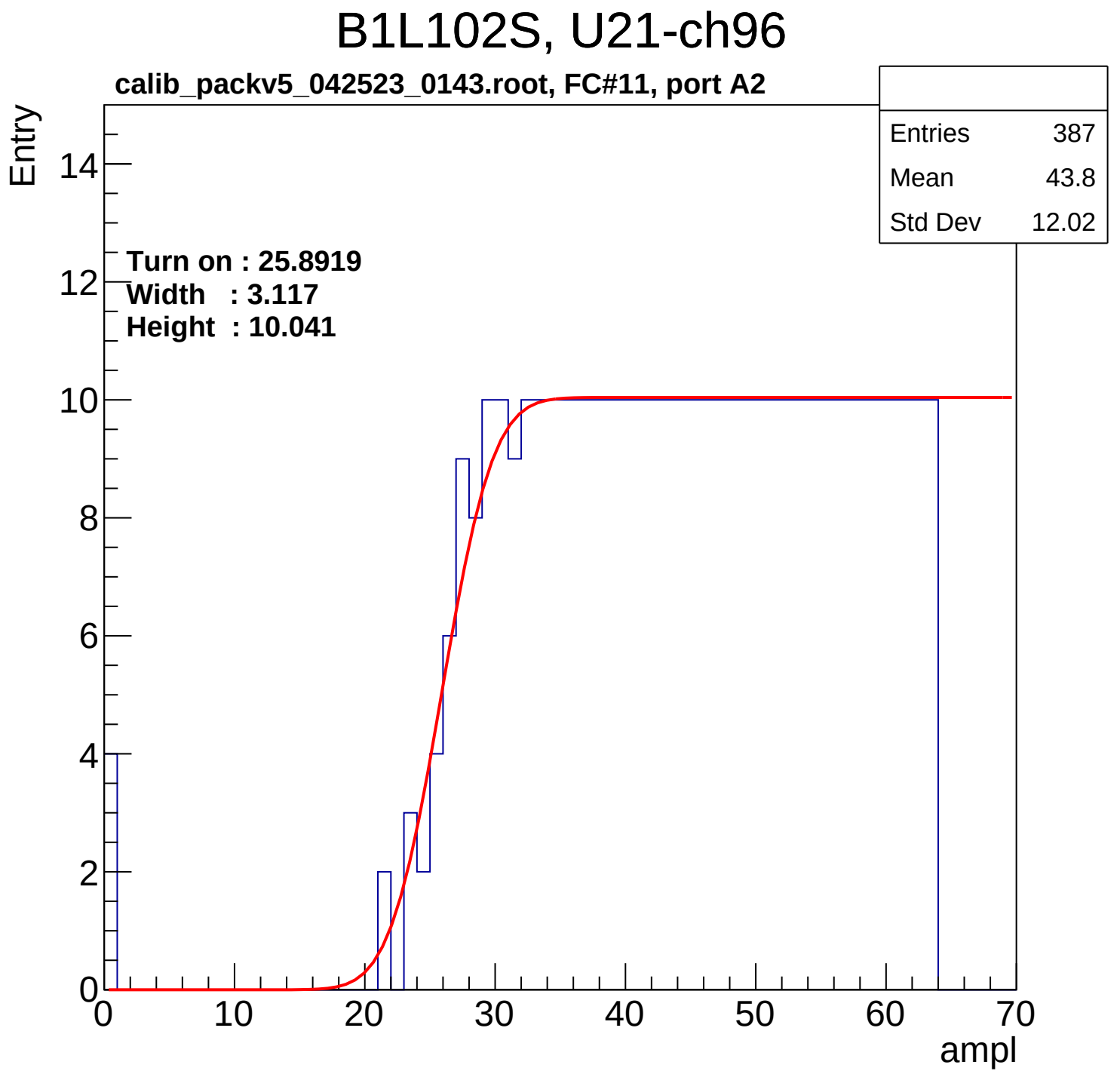
B1L102S, U21-ch96
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 43.8
Std Dev 12.02
Turn on : 25.8919
Width : 3.117
Height : 10.041
Entry
ampl
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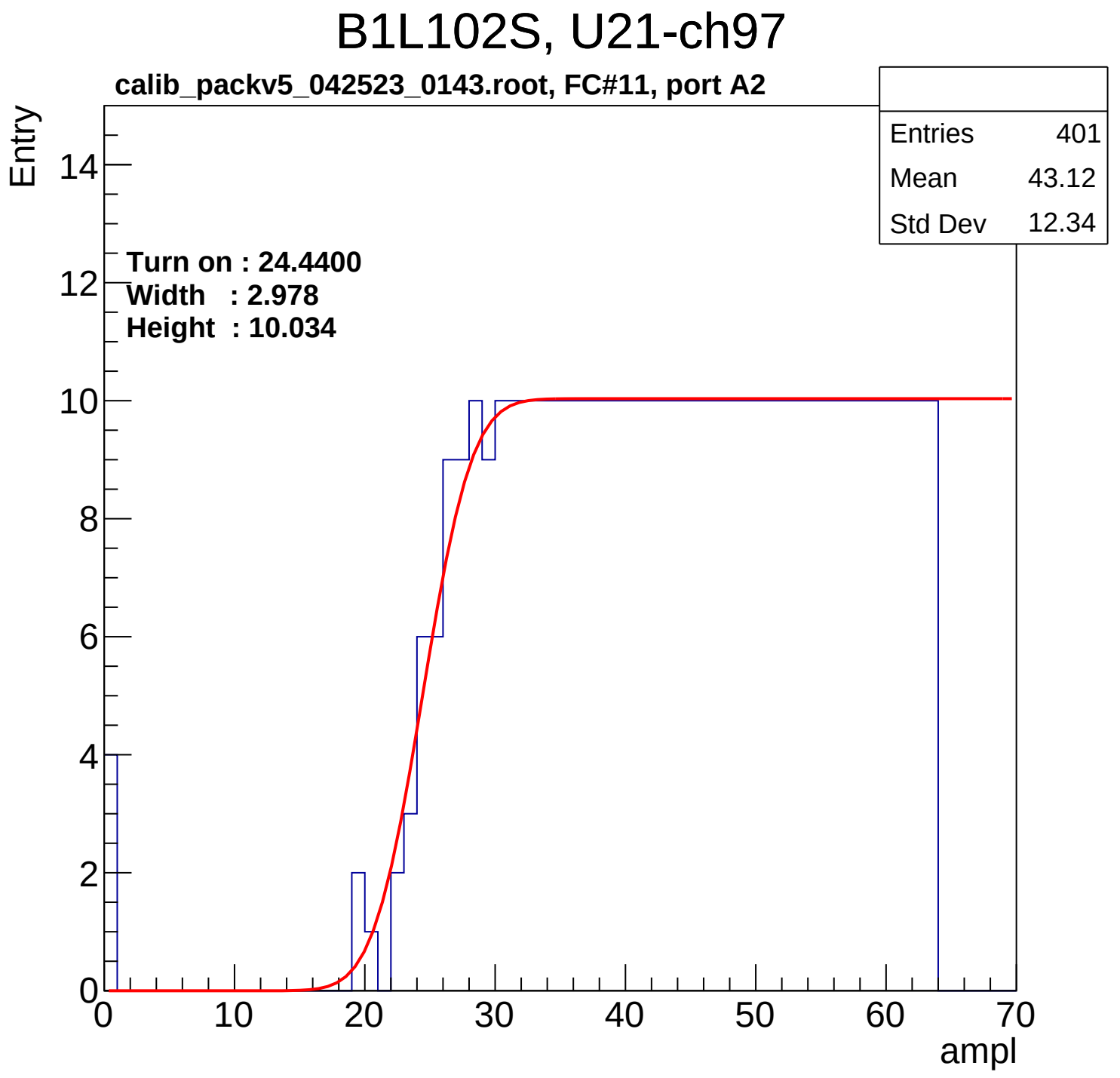
B1L102S, U21-ch97
calib_packv5_042523_0143.root, FC#11, port A2
Entries 401
Mean 43.12
Std Dev 12.34
Turn on : 24.4400
Width : 2.978
Height : 10.034
Entry
ampl
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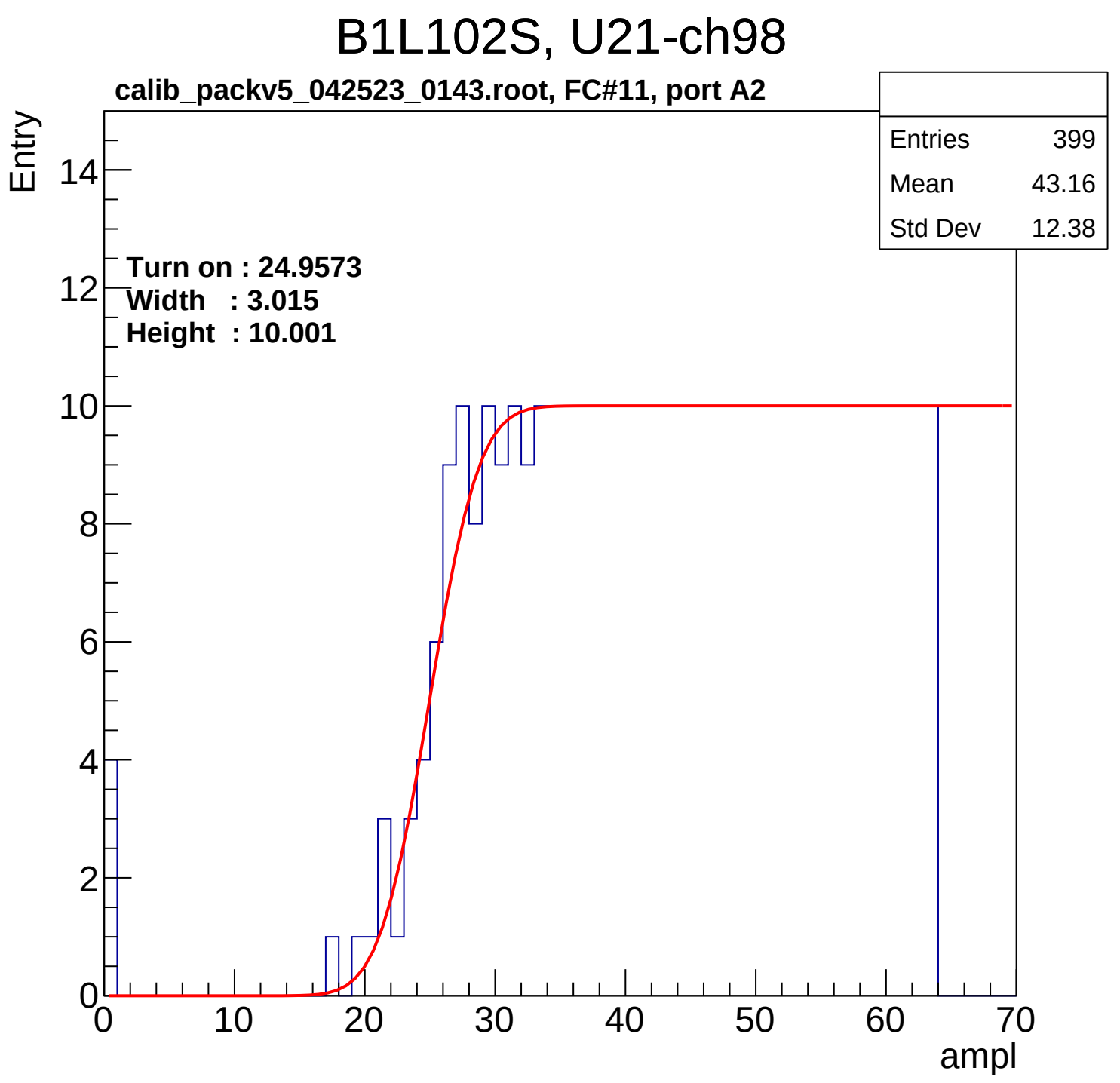
B1L102S, U21-ch98
calib_packv5_042523_0143.root, FC#11, port A2
Entries 399
Mean 43.16
Std Dev 12.38
Turn on : 24.9573
Width : 3.015
Height : 10.001
Entry
ampl
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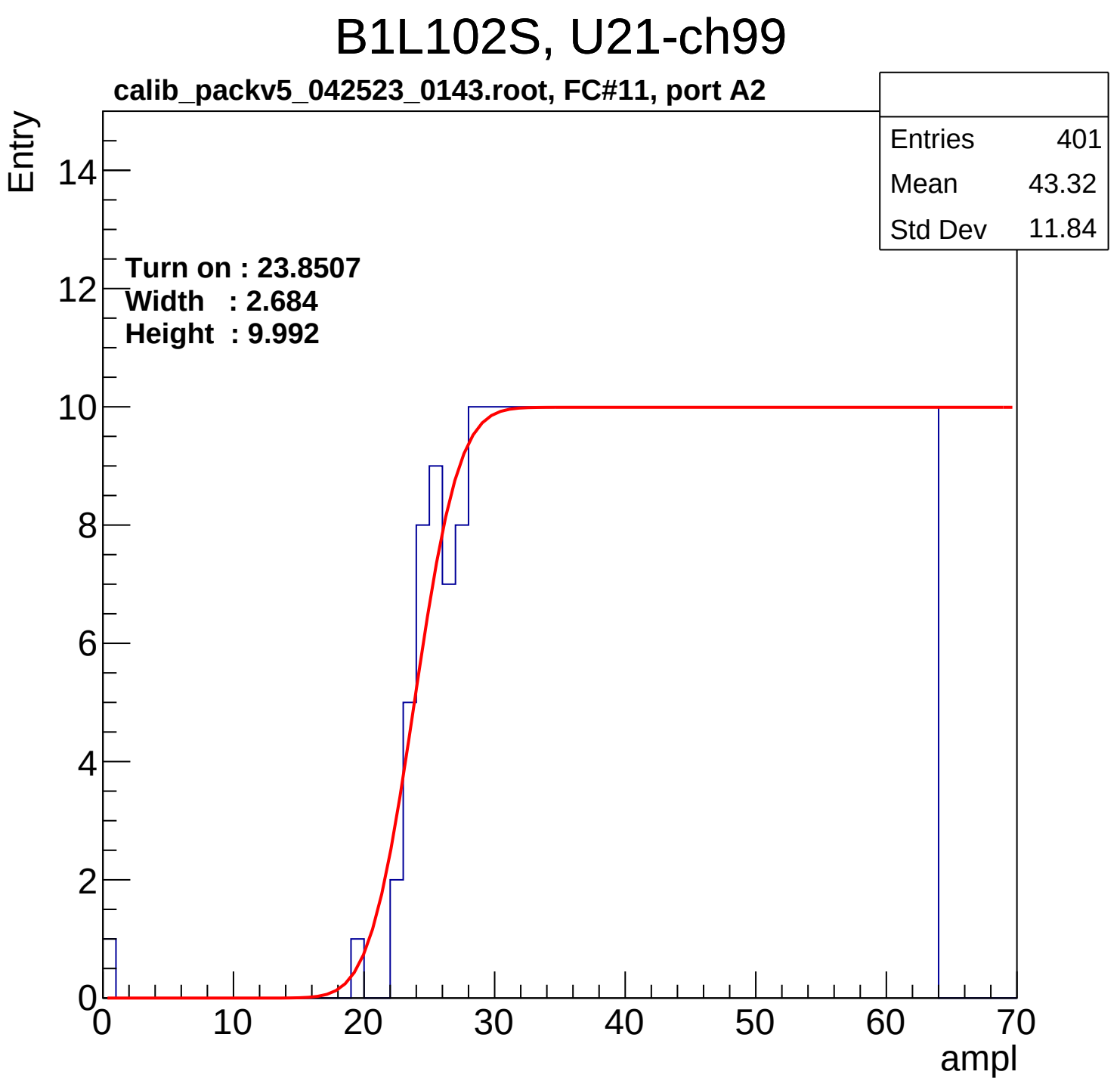
B1L102S, U21-ch99
calib_packv5_042523_0143.root, FC#11, port A2
Entries 401
Mean 43.32
Std Dev 11.84
Turn on : 23.8507
Width : 2.684
Height : 9.992
Entry
ampl
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6
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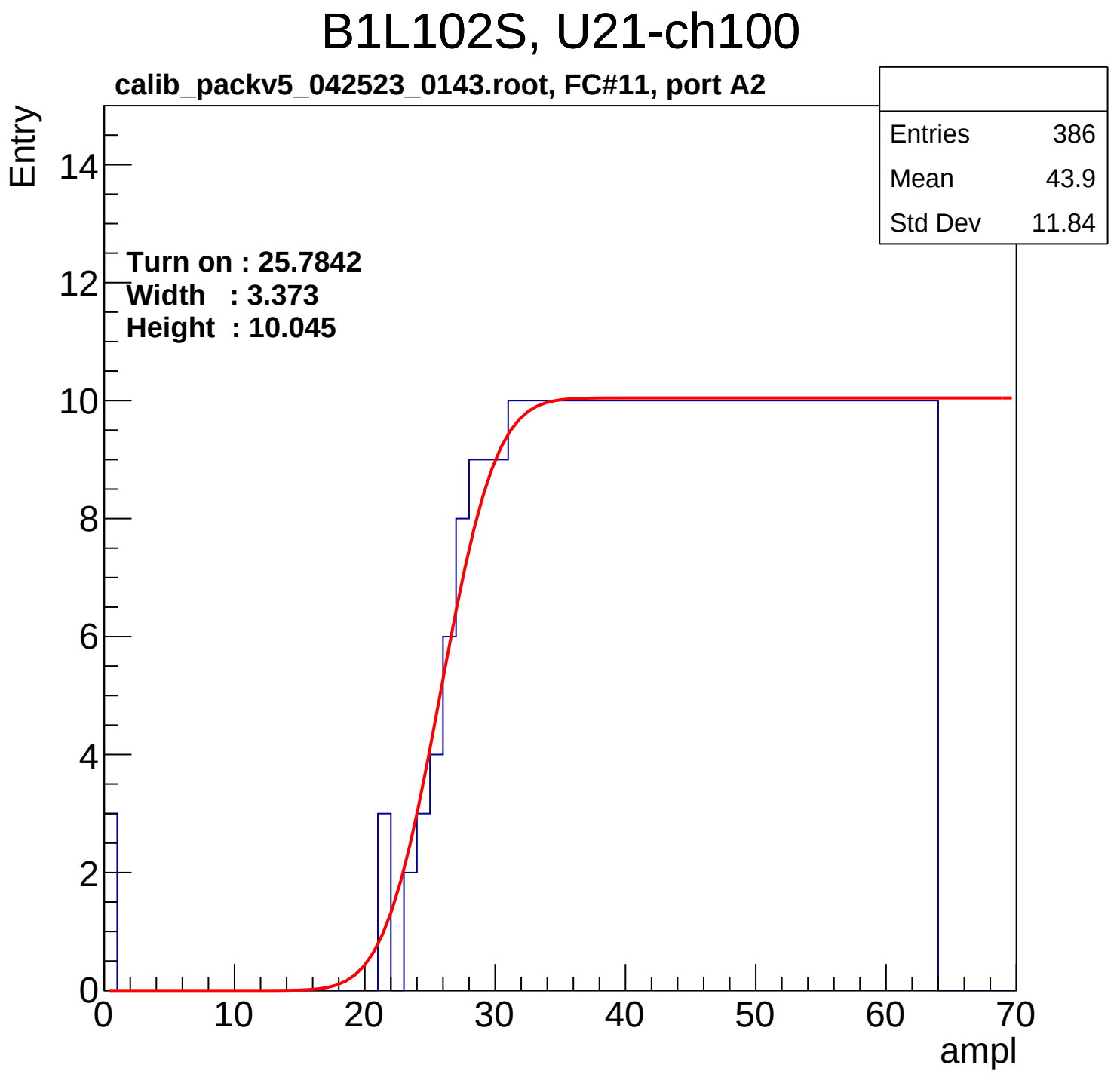
B1L102S, U21-ch100
calib_packv5_042523_0143.root, FC#11, port A2
Entries 386
Mean 43.9
Std Dev 11.84
Turn on : 25.7842
Width : 3.373
Height : 10.045
Entry
ampl
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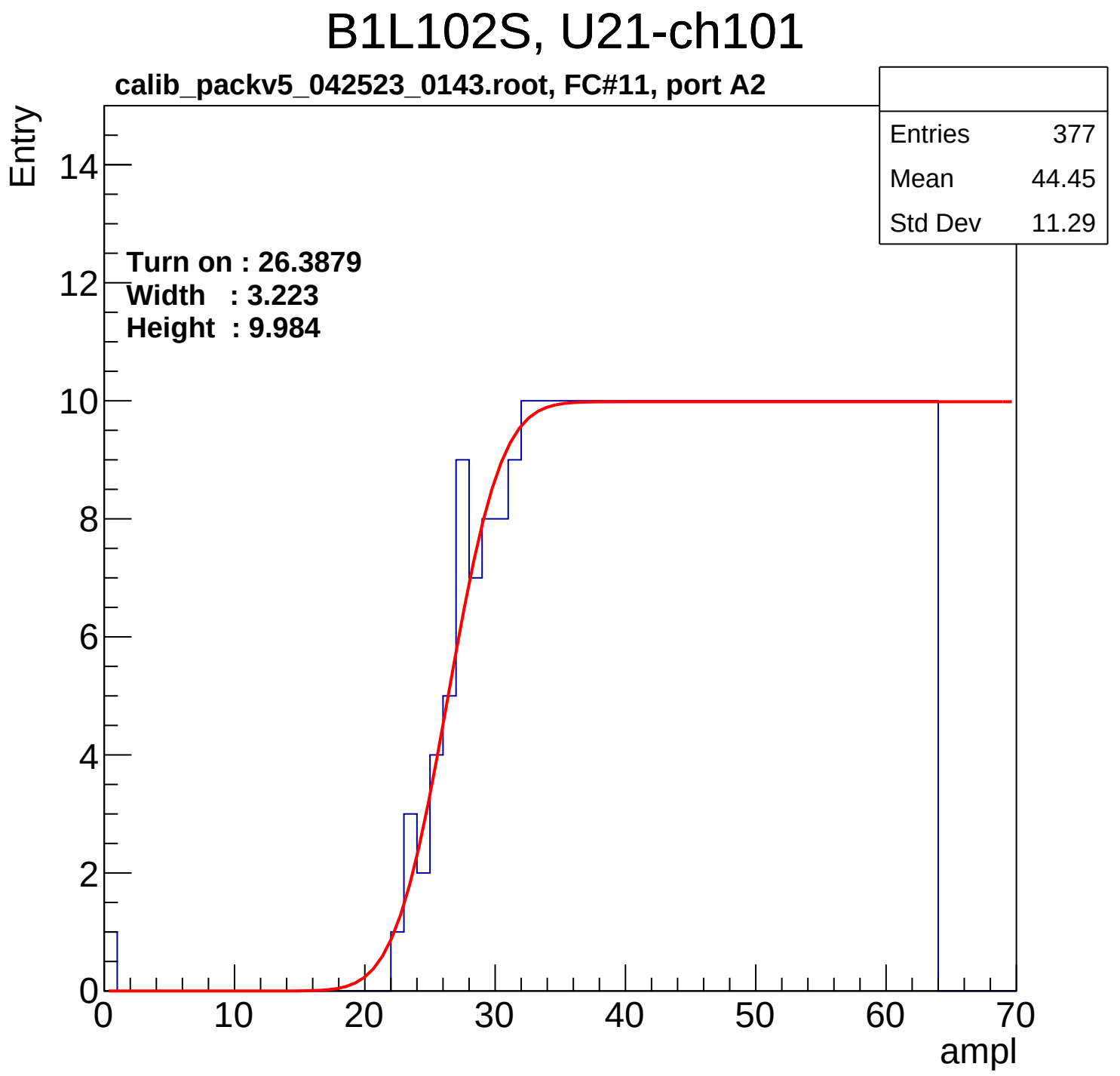
B1L102S, U21-ch101
calib_packv5_042523_0143.root, FC#11, port A2
Entries 377
Mean 44.45
Std Dev 11.29
Turn on : 26.3879
Width : 3.223
Height : 9.984
Entry
ampl
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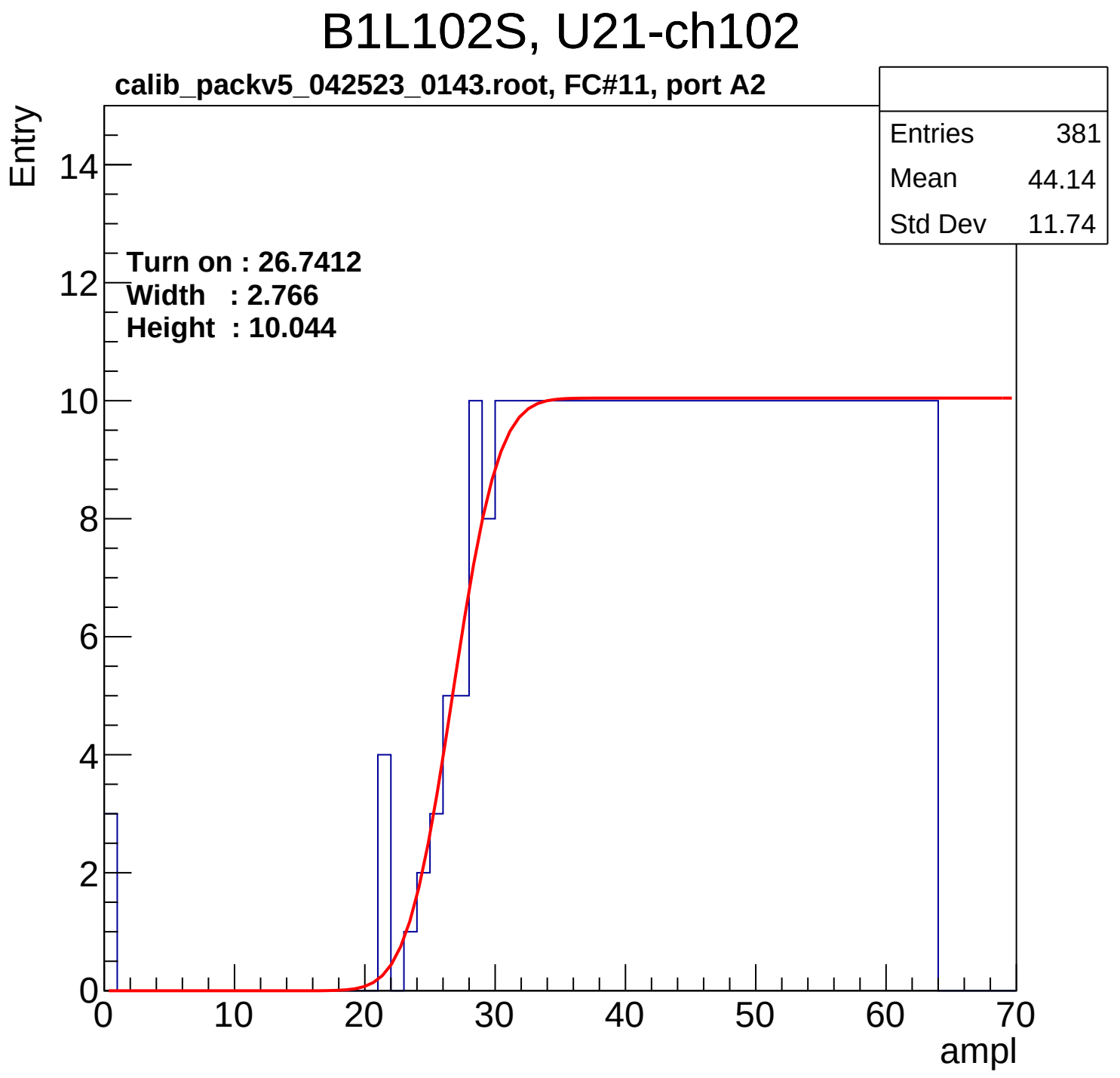
B1L102S, U21-ch102
calib_packv5_042523_0143.root, FC#11, port A2
Entries 381
Mean 44.14
Std Dev 11.74
Turn on : 26.7412
Width : 2.766
Height : 10.044
Entry
ampl
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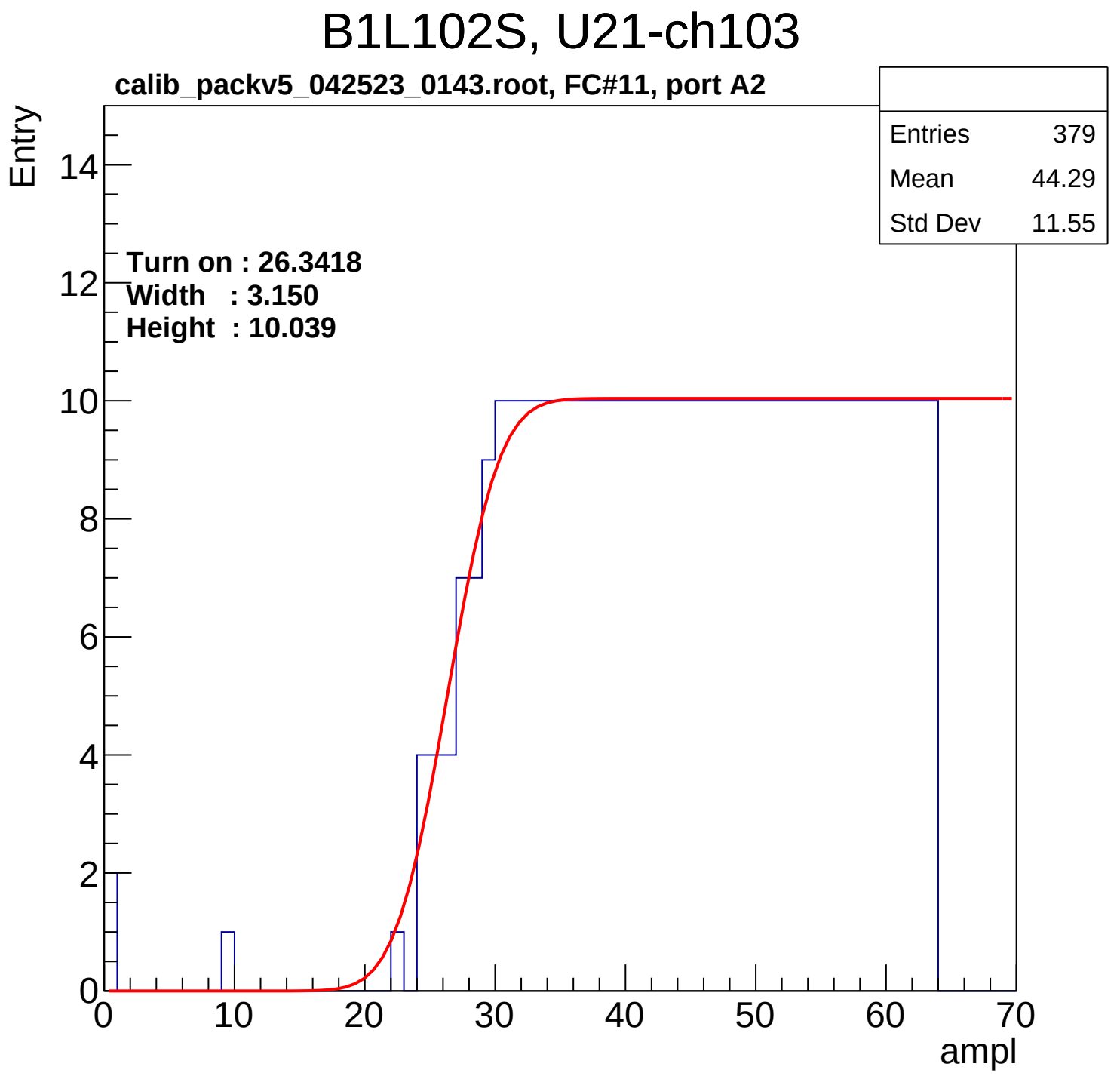
B1L102S, U21-ch103
calib_packv5_042523_0143.root, FC#11, port A2
Entries 379
Mean 44.29
Std Dev 11.55
Turn on : 26.3418
Width : 3.150
Height : 10.039
Entry
ampl
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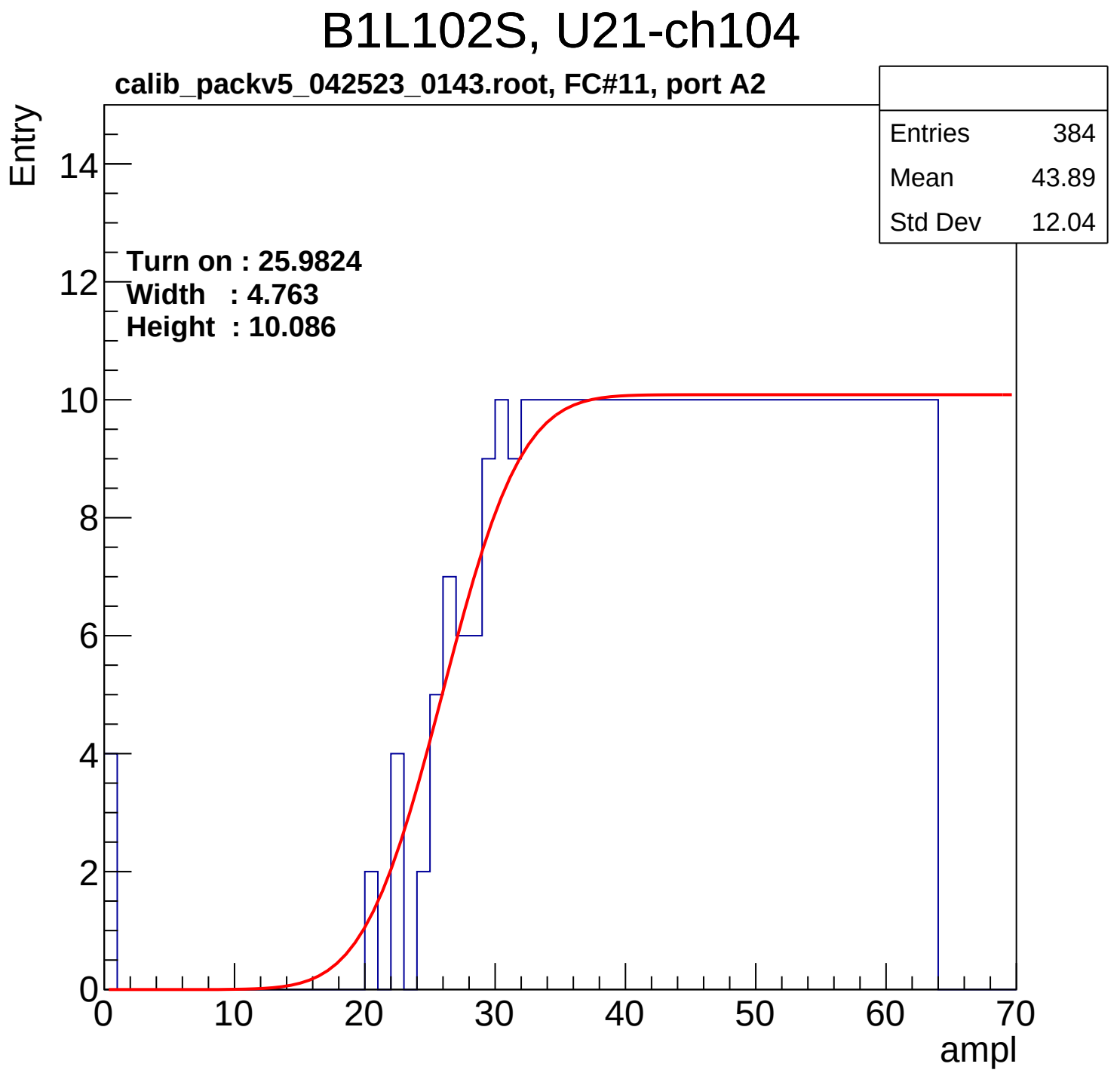
B1L102S, U21-ch104
calib_packv5_042523_0143.root, FC#11, port A2
Entries 384
Mean 43.89
Std Dev 12.04
Turn on : 25.9824
Width : 4.763
Height : 10.086
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ampl
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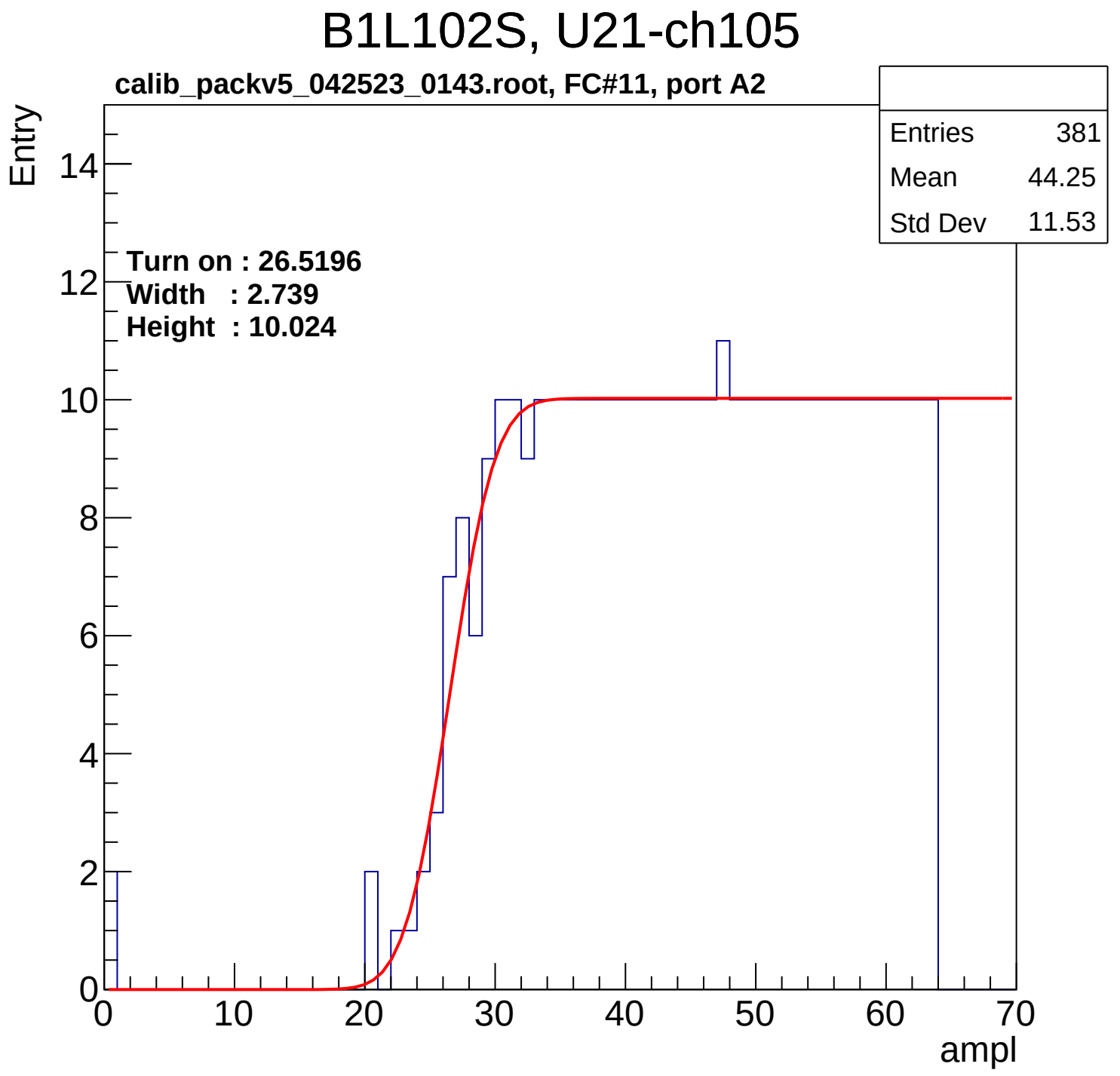
B1L102S, U21-ch105
calib_packv5_042523_0143.root, FC#11, port A2
Entries 381
Mean 44.25
Std Dev 11.53
Turn on : 26.5196
Width : 2.739
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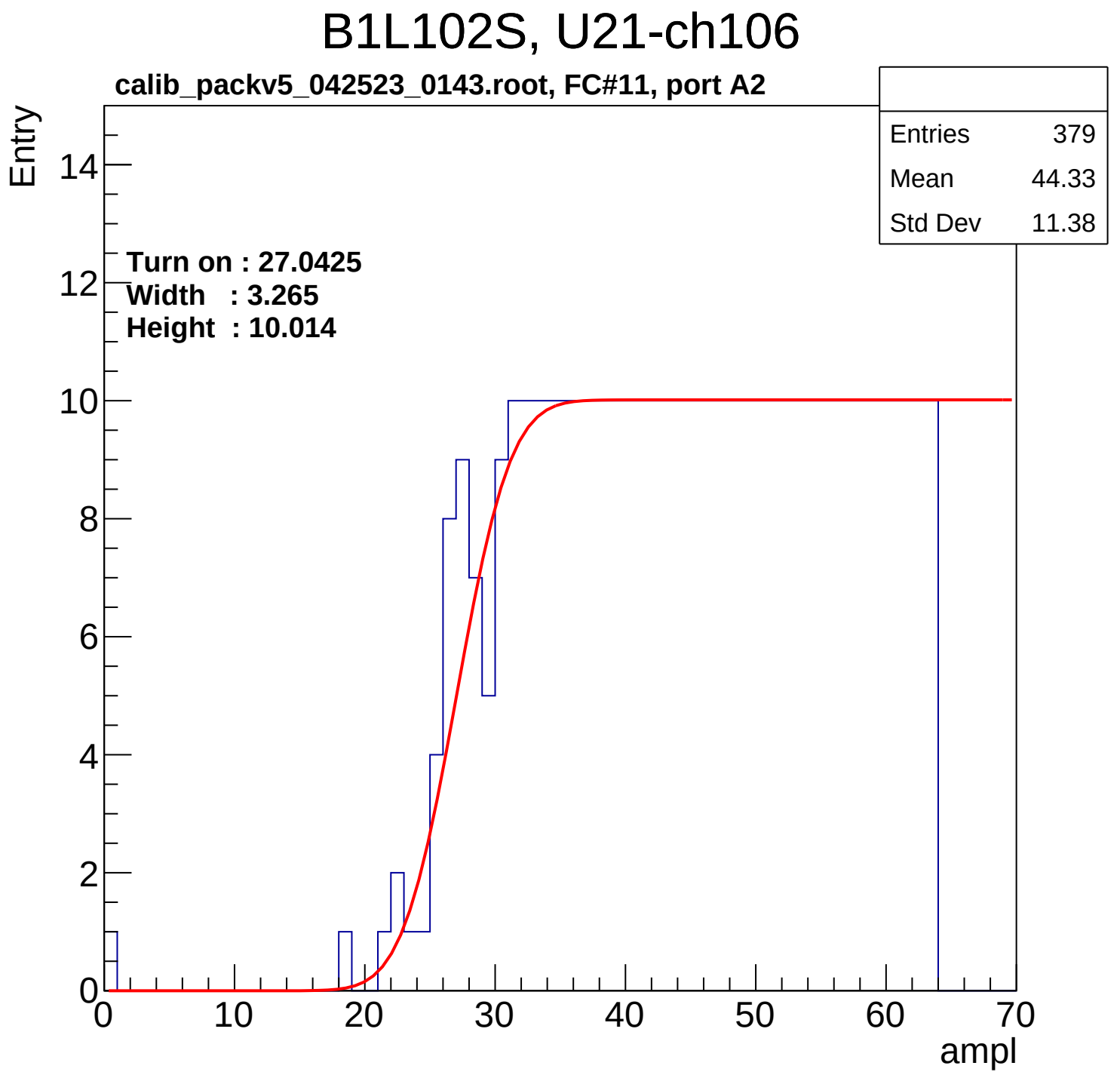
B1L102S, U21-ch106
calib_packv5_042523_0143.root, FC#11, port A2
Entries 379
Mean 44.33
Std Dev 11.38
Turn on : 27.0425
Width : 3.265
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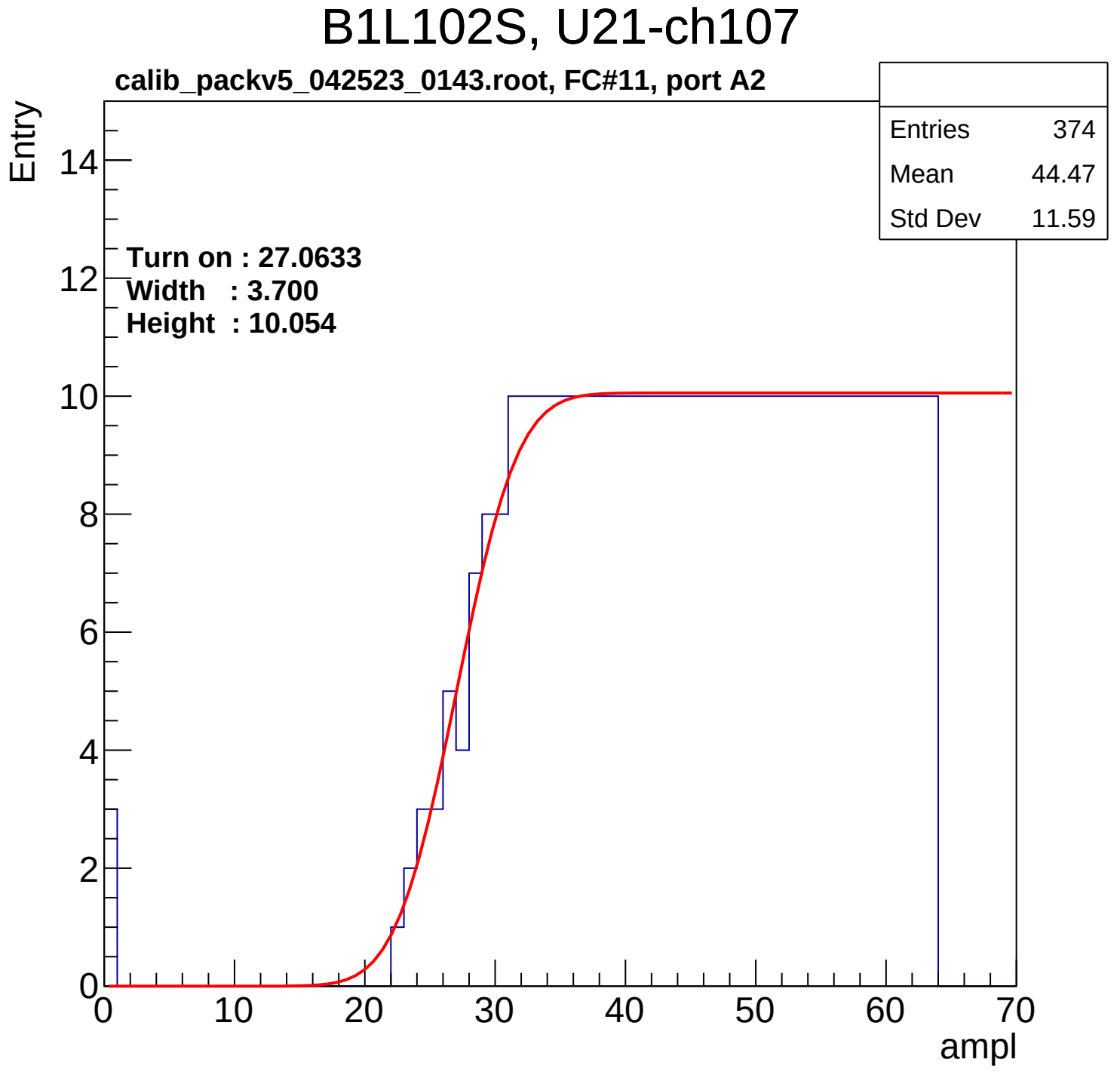
B1L102S, U21-ch107
calib_packv5_042523_0143.root, FC#11, port A2
Entries 374
Mean 44.47
Std Dev 11.59
Turn on : 27.0633
Width : 3.700
Height : 10.054
Entry
ampl
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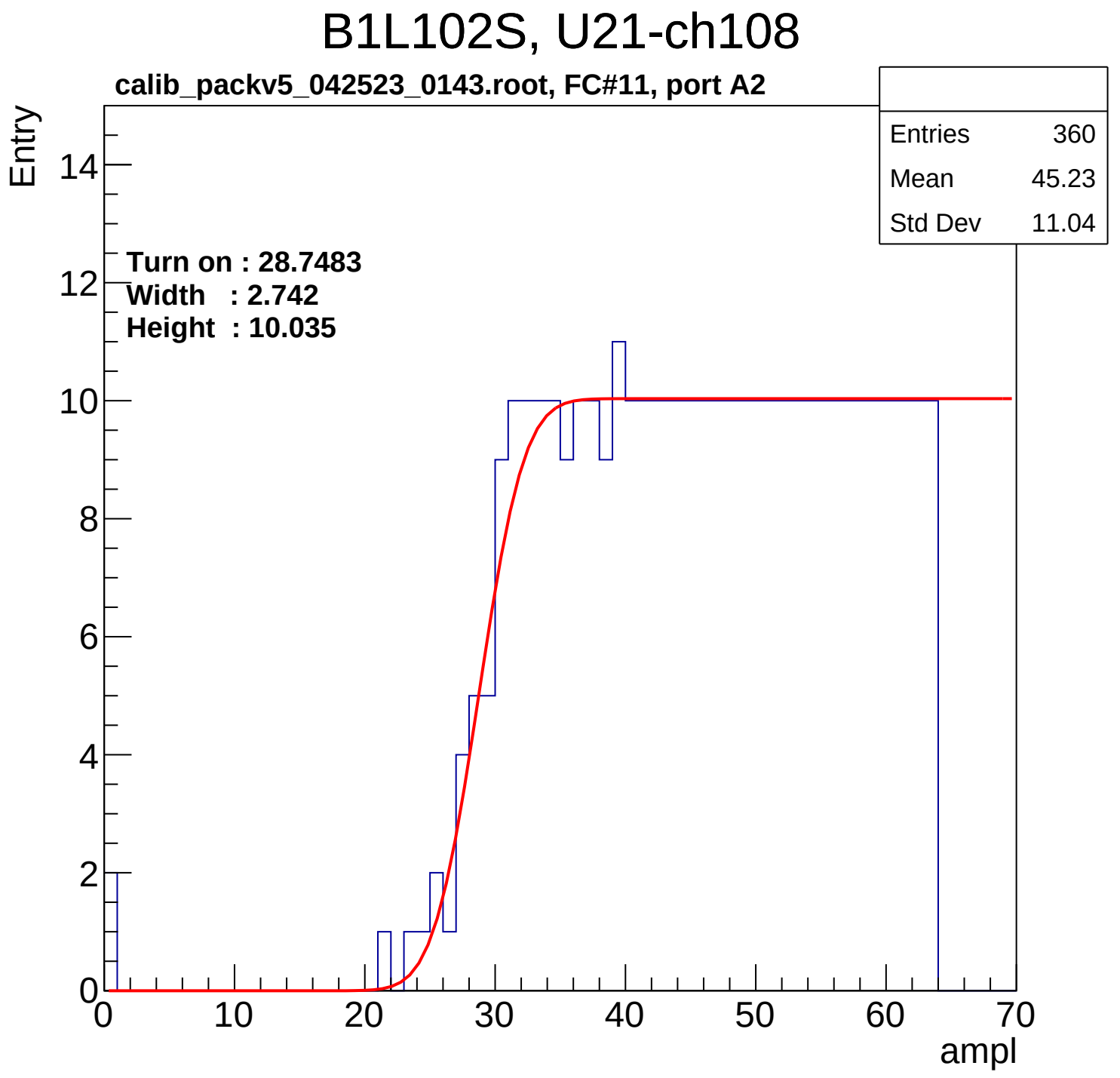
B1L102S, U21-ch108
calib_packv5_042523_0143.root, FC#11, port A2
Entries 360
Mean 45.23
Std Dev 11.04
Turn on : 28.7483
Width : 2.742
Height : 10.035
Entry
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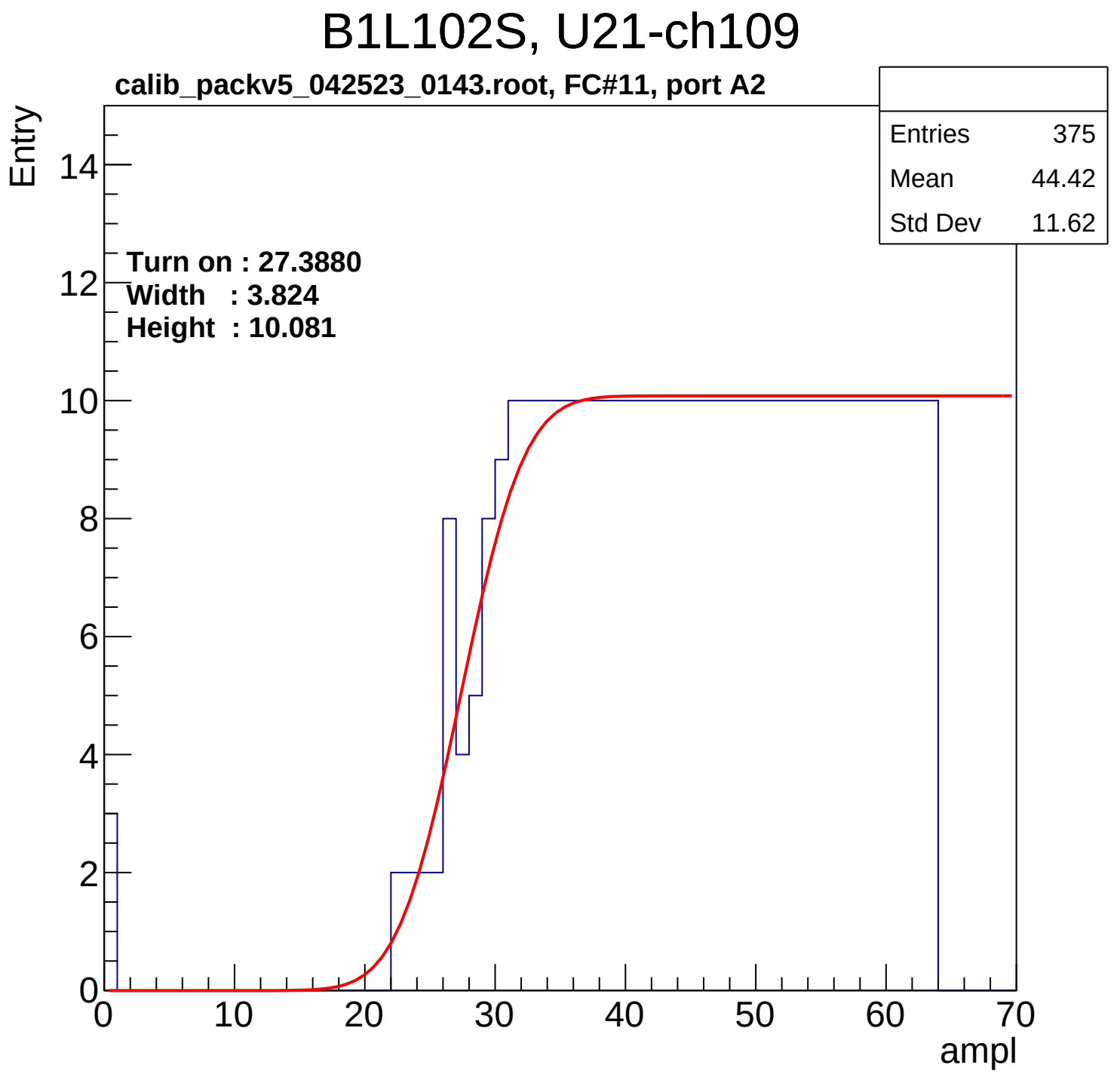
B1L102S, U21-ch109
calib_packv5_042523_0143.root, FC#11, port A2
Entries 375
Mean 44.42
Std Dev 11.62
Turn on : 27.3880
Width : 3.824
Height : 10.081
Entry
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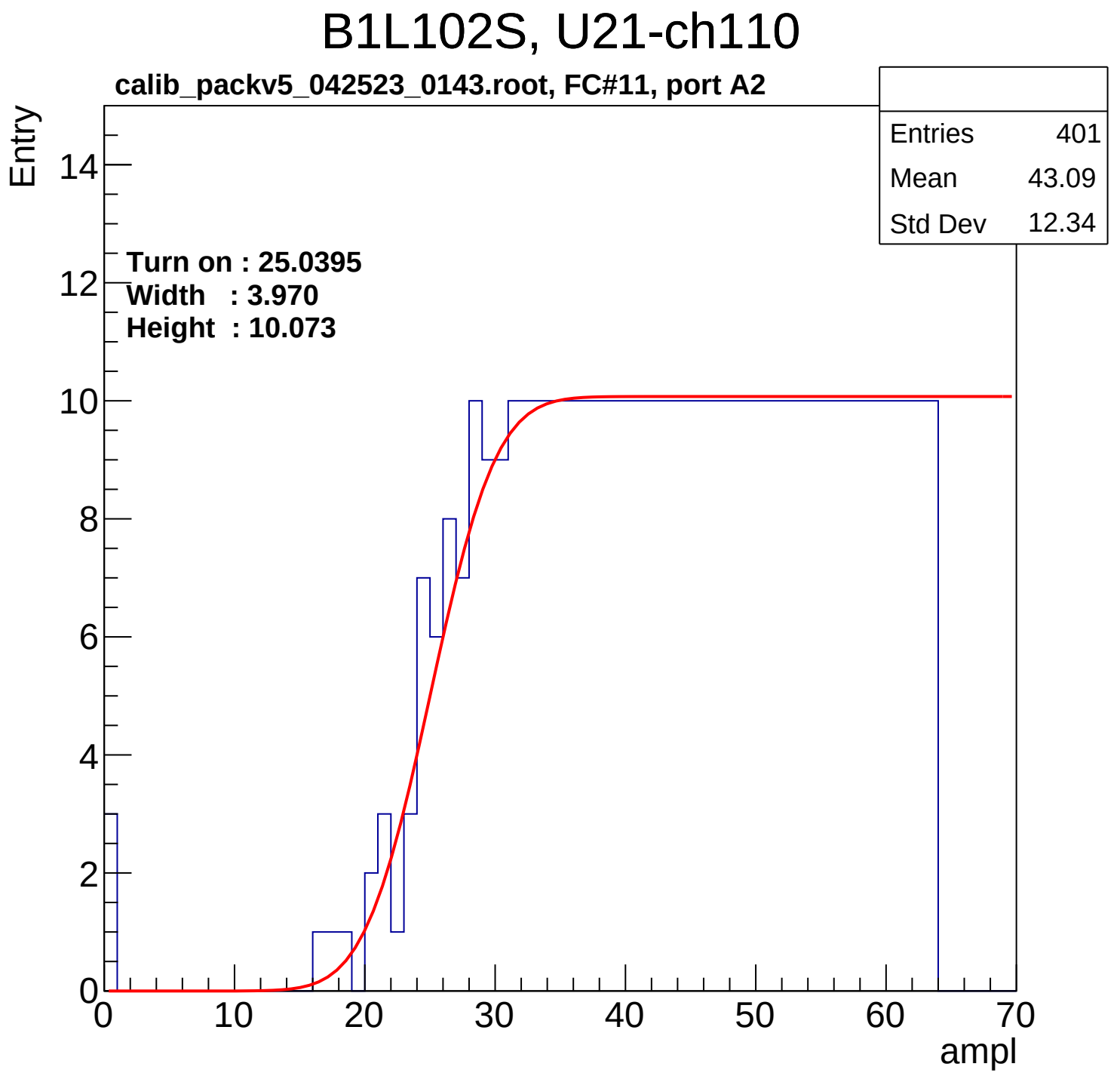
B1L102S, U21-ch110
calib_packv5_042523_0143.root, FC#11, port A2
Entries 401
Mean 43.09
Std Dev 12.34
Turn on : 25.0395
Width : 3.970
Height : 10.073
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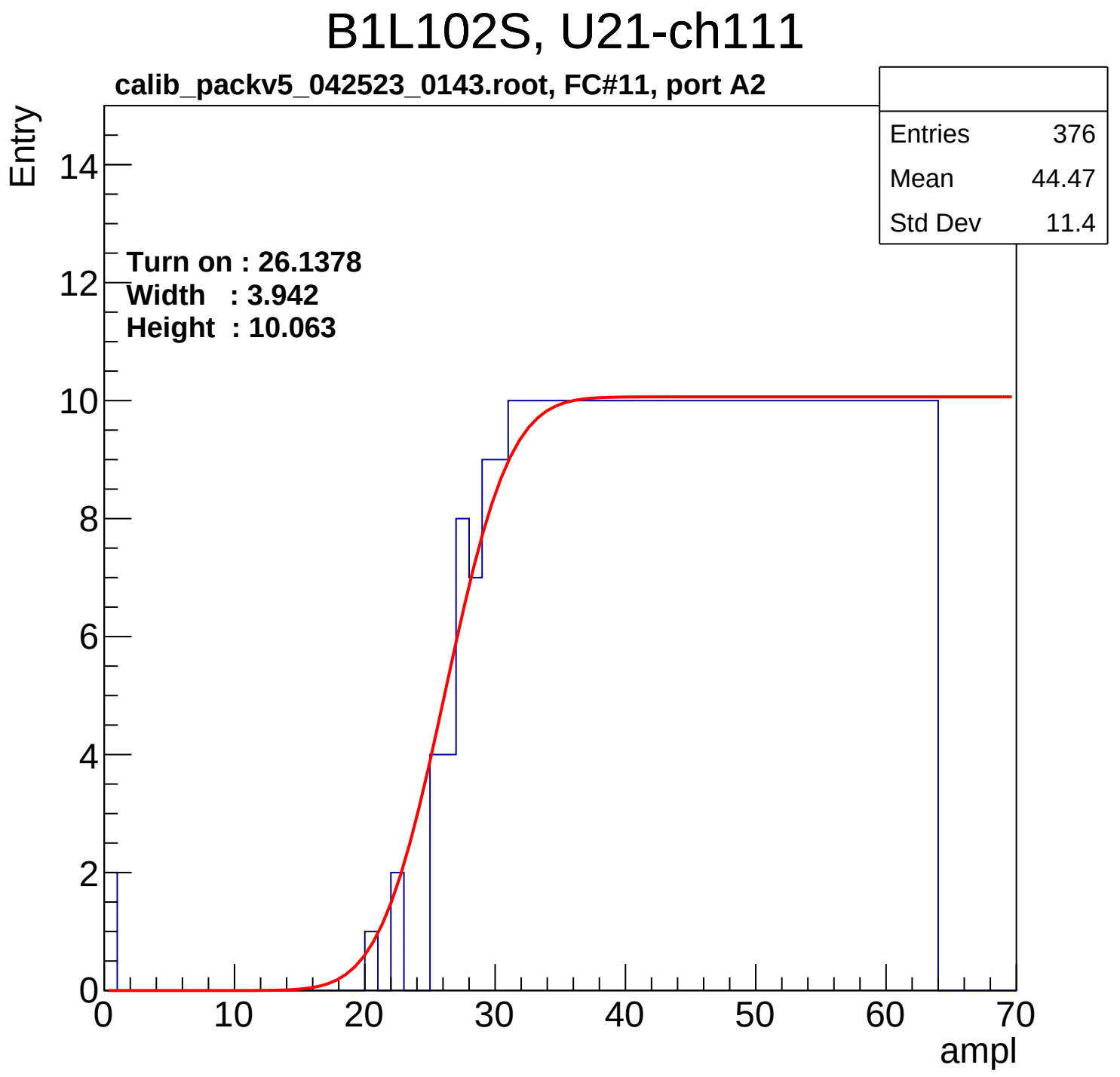
B1L102S, U21-ch111
calib_packv5_042523_0143.root, FC#11, port A2
Entries 376
Mean 44.47
Std Dev 11.4
Turn on : 26.1378
Width : 3.942
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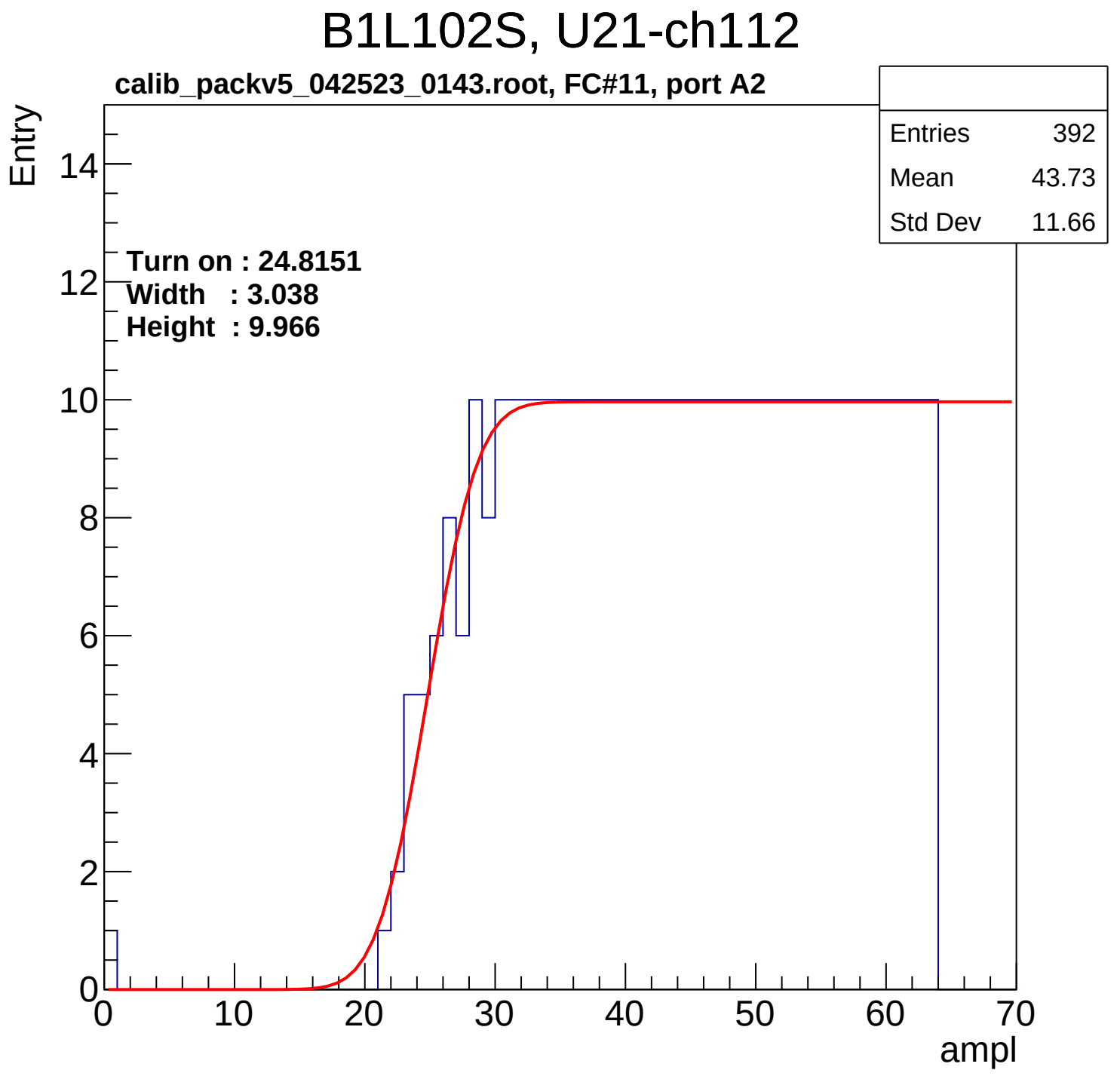
B1L102S, U21-ch112
calib_packv5_042523_0143.root, FC#11, port A2
Entries 392
Mean 43.73
Std Dev 11.66
Turn on : 24.8151
Width : 3.038
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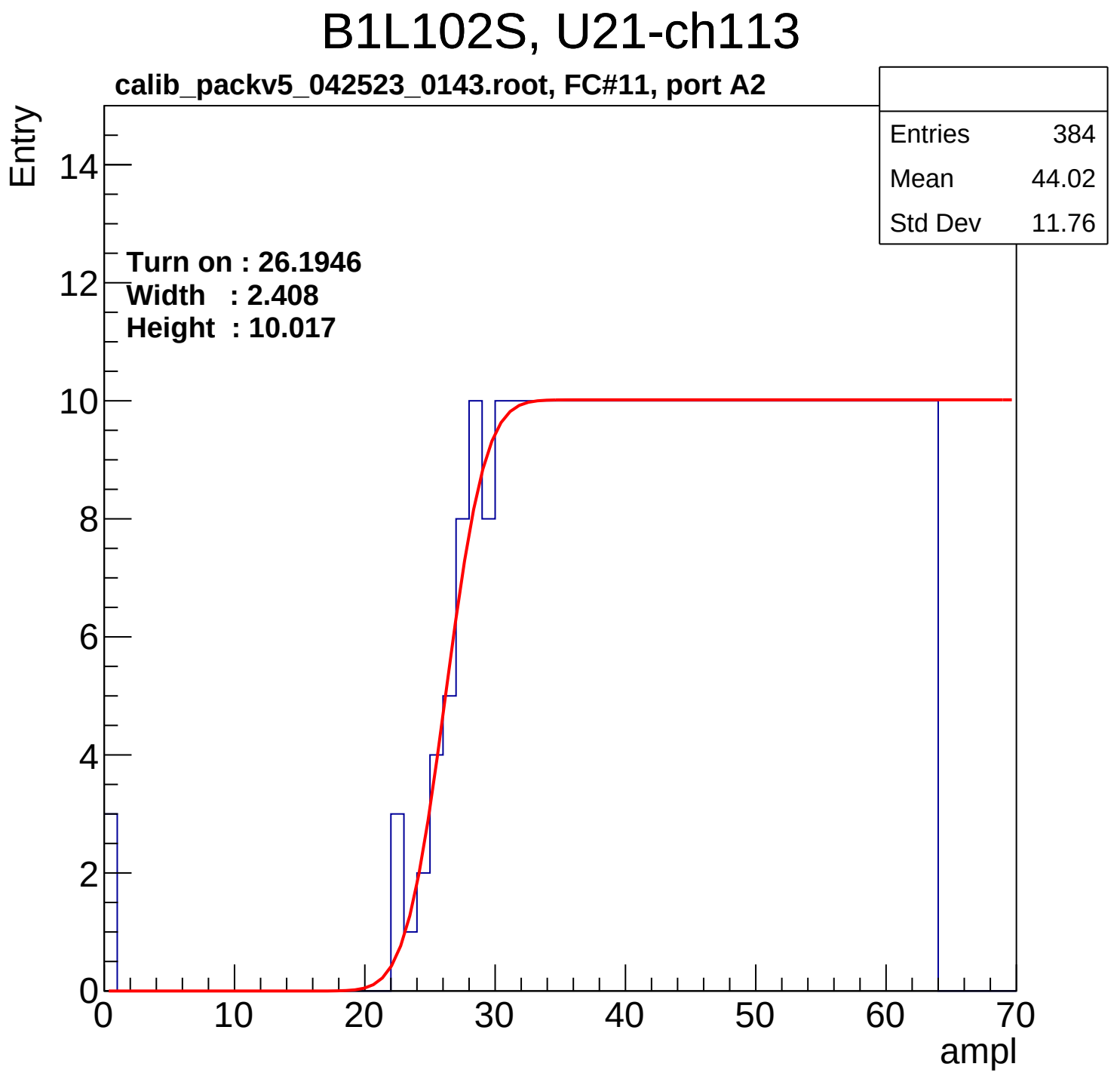
B1L102S, U21-ch113
calib_packv5_042523_0143.root, FC#11, port A2
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Std Dev 11.76
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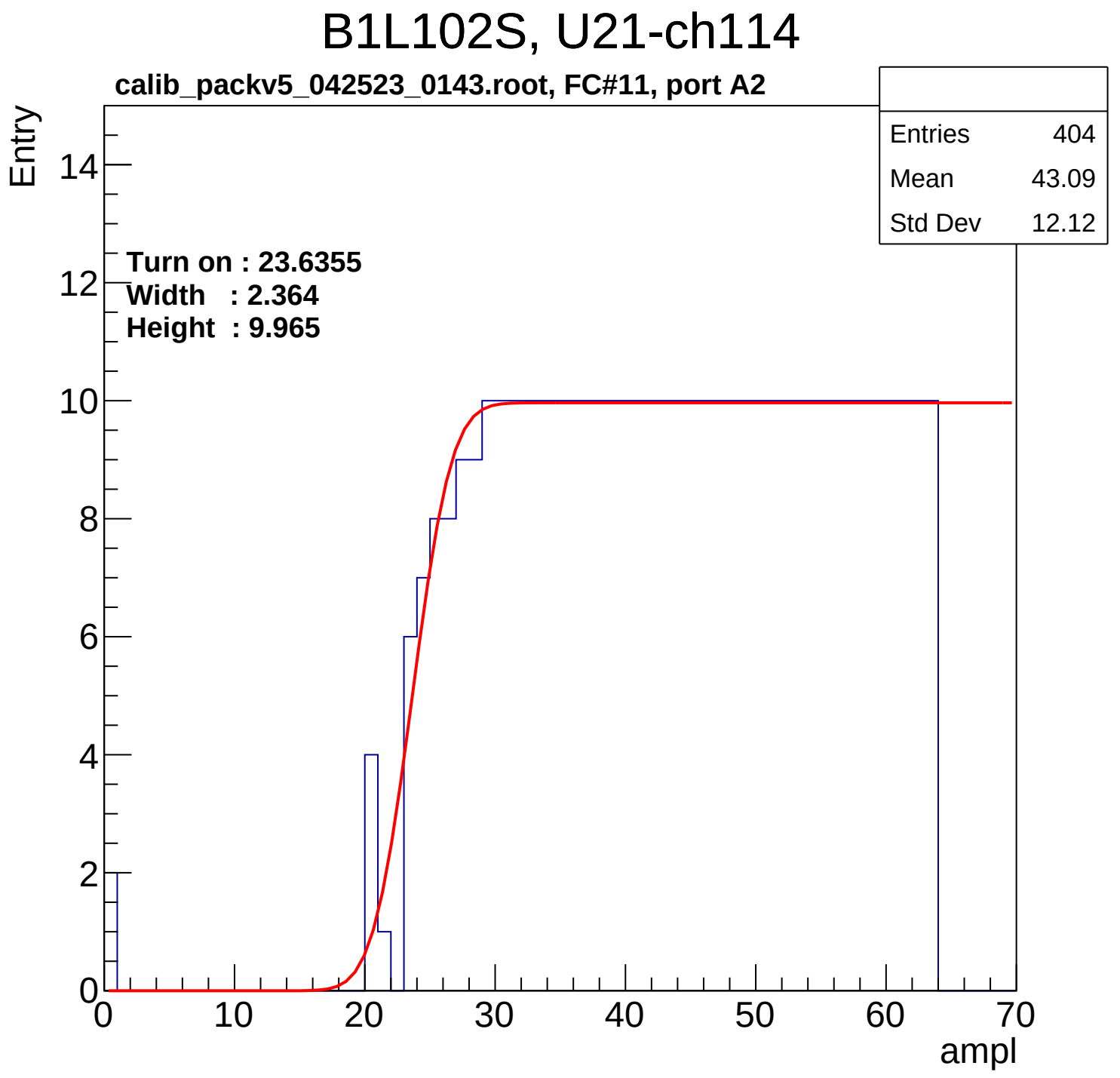
B1L102S, U21-ch114
calib_packv5_042523_0143.root, FC#11, port A2
Entries 404
Mean 43.09
Std Dev 12.12
Turn on : 23.6355
Width : 2.364
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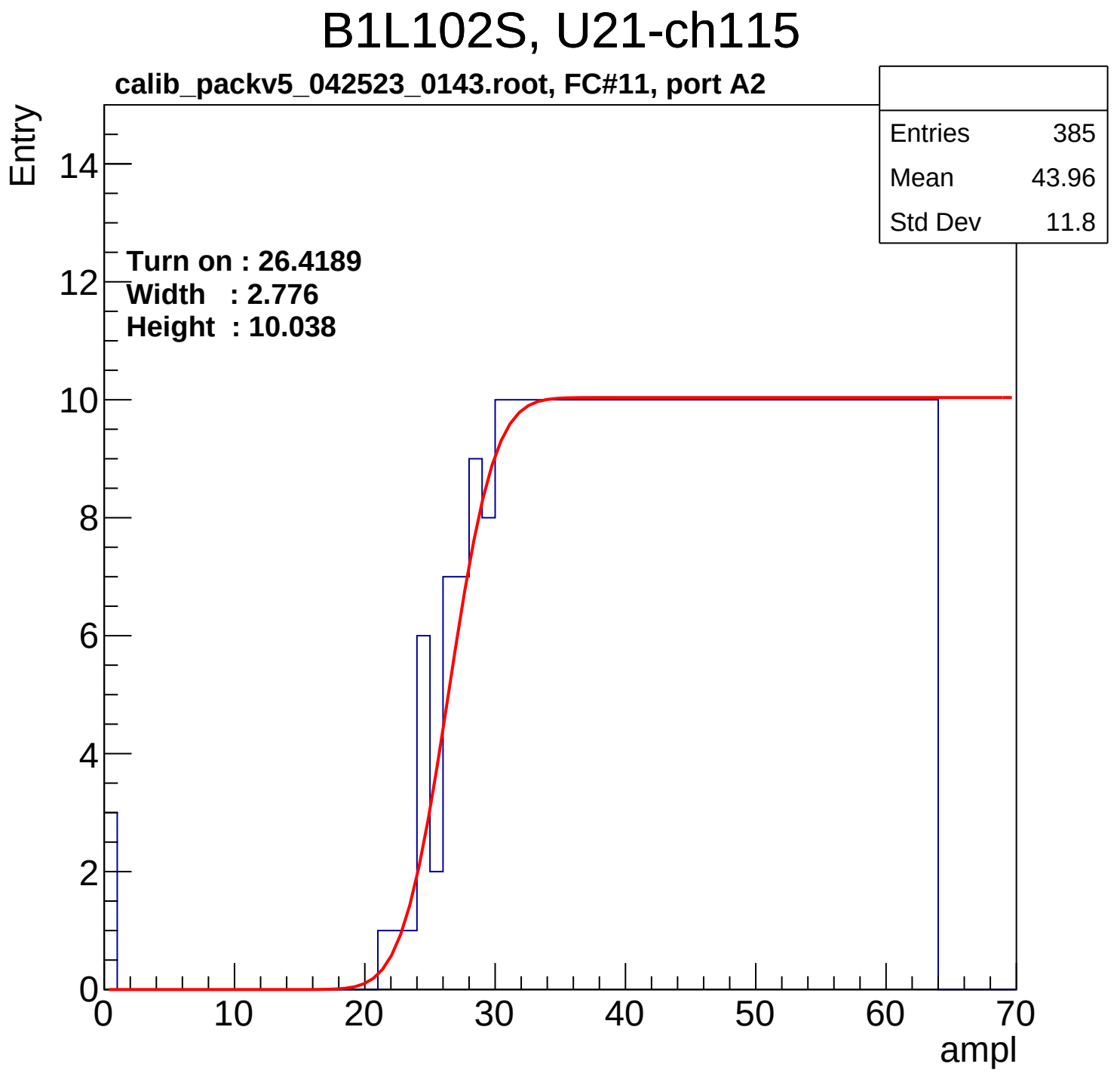
B1L102S, U21-ch115
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 43.96
Std Dev 11.8
Turn on : 26.4189
Width : 2.776
Height : 10.038
Entry
ampl
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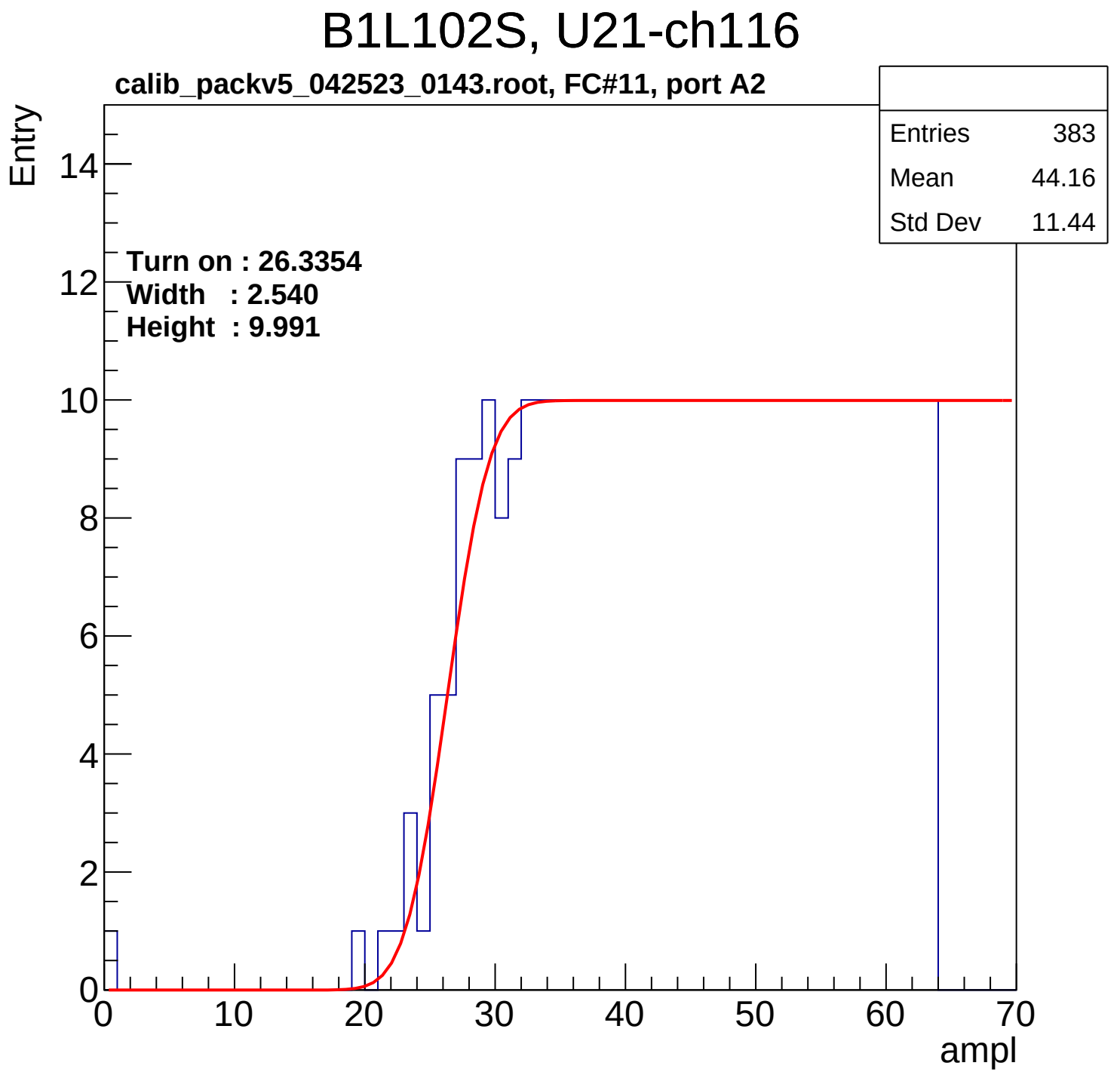
B1L102S, U21-ch116
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 44.16
Std Dev 11.44
Turn on : 26.3354
Width : 2.540
Height : 9.991
Entry
ampl
0
2
4
6
8
10
12
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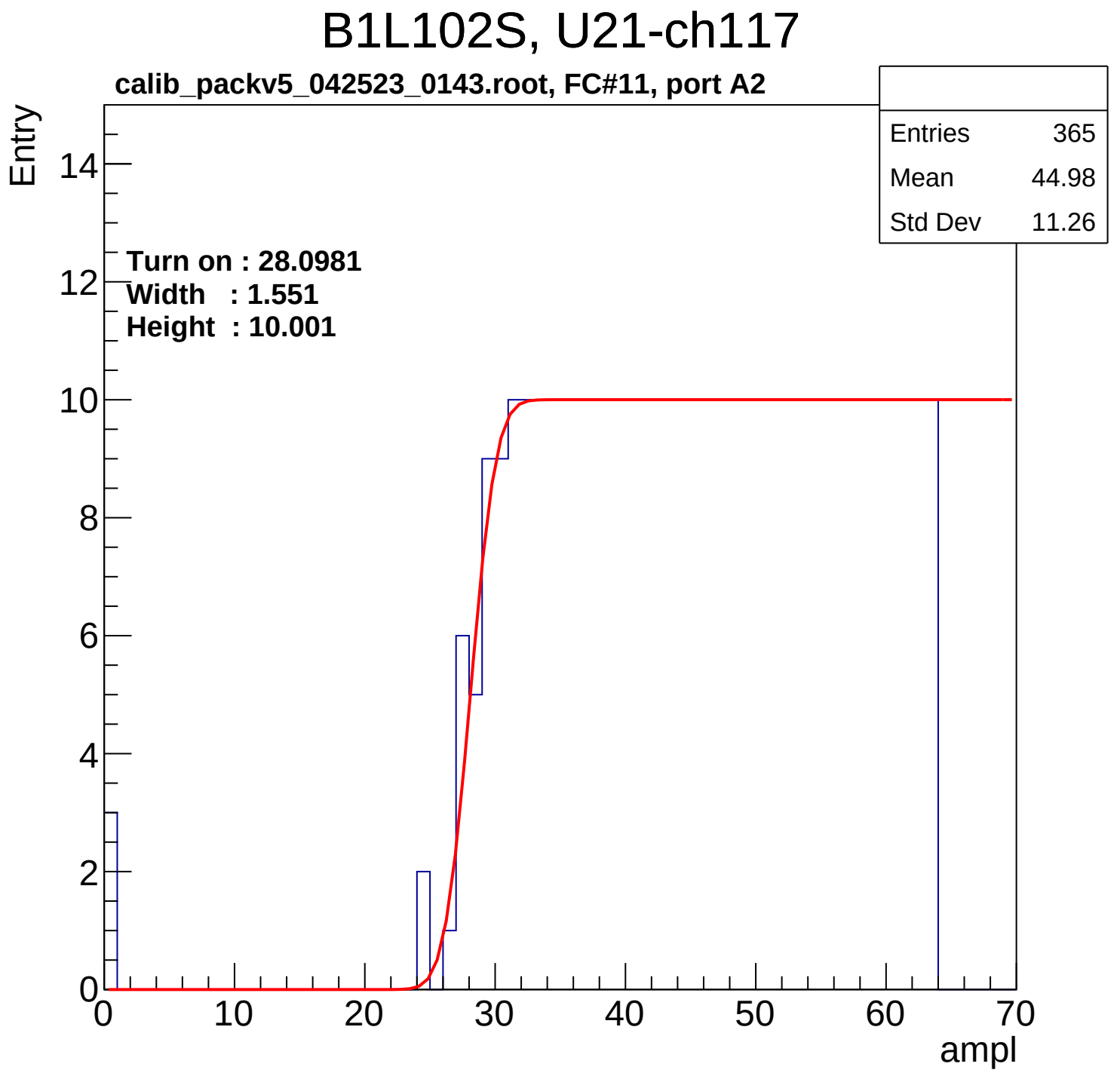
B1L102S, U21-ch117
calib_packv5_042523_0143.root, FC#11, port A2
Entries 365
Mean 44.98
Std Dev 11.26
Turn on : 28.0981
Width : 1.551
Height : 10.001
Entry
ampl
0
2
4
6
8
10
12
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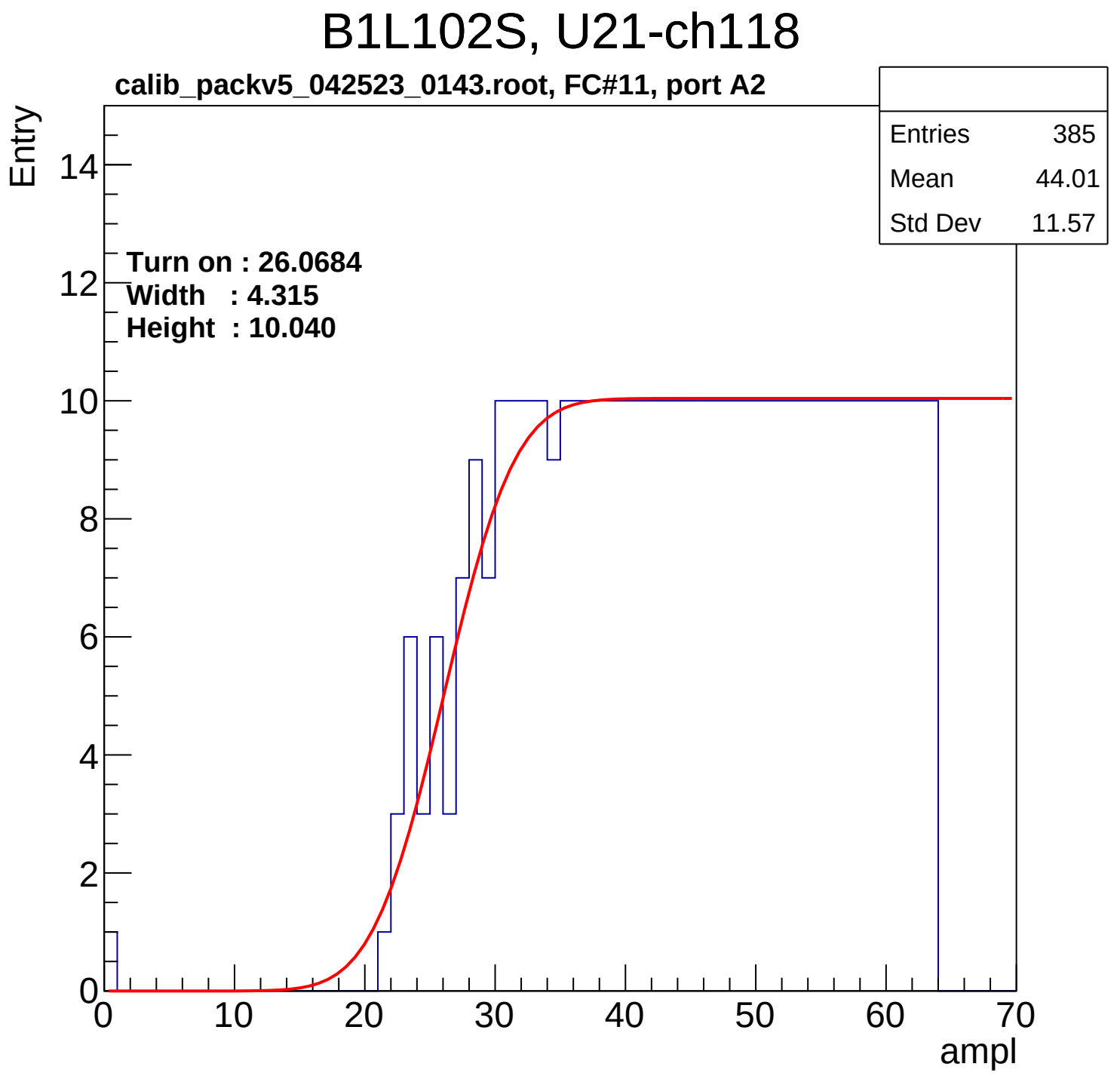
B1L102S, U21-ch118
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 44.01
Std Dev 11.57
Turn on : 26.0684
Width : 4.315
Height : 10.040
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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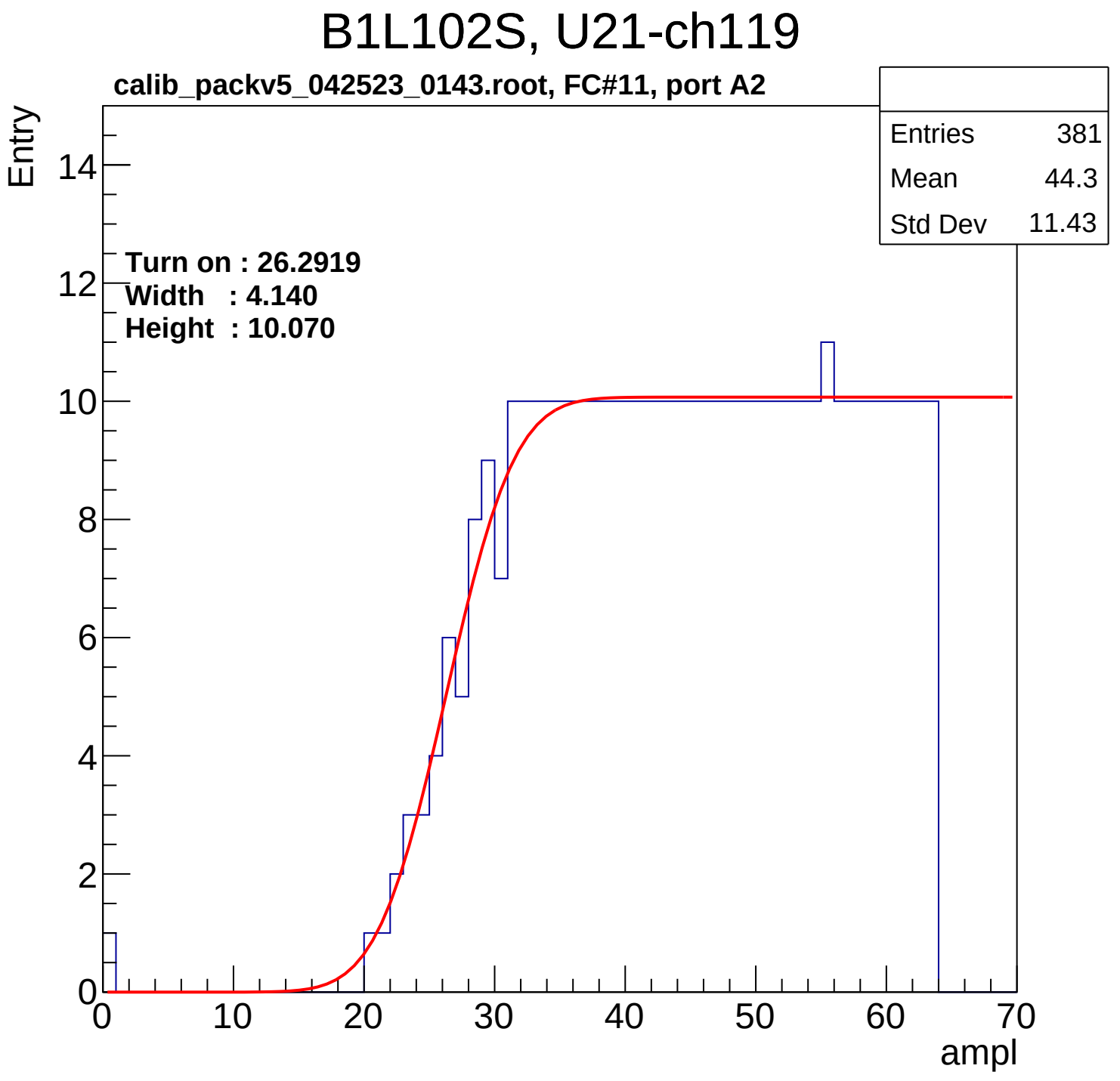
B1L102S, U21-ch119
calib_packv5_042523_0143.root, FC#11, port A2
Entries 381
Mean 44.3
Std Dev 11.43
Turn on : 26.2919
Width : 4.140
Height : 10.070
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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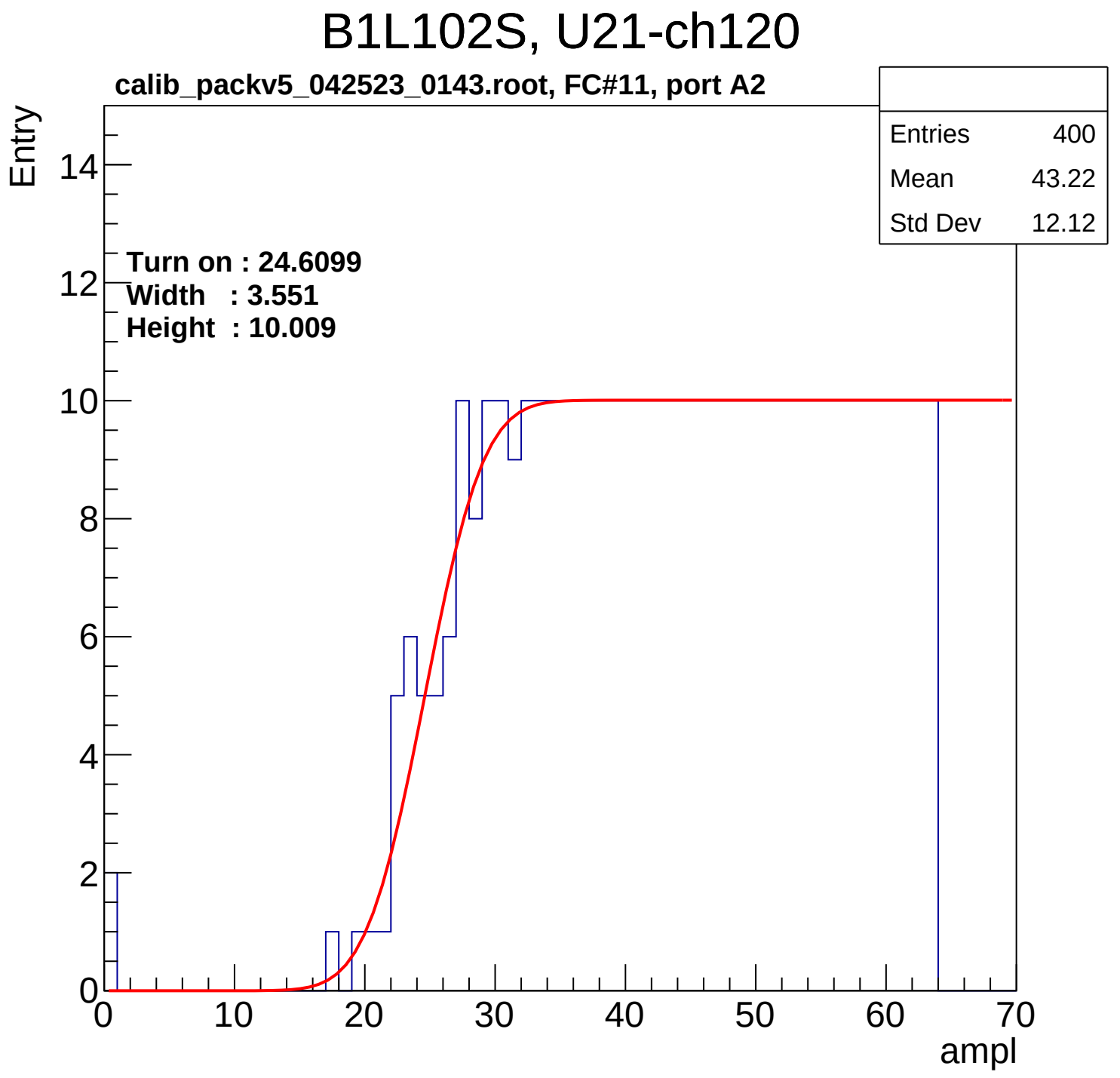
B1L102S, U21-ch120
calib_packv5_042523_0143.root, FC#11, port A2
Entries 400
Mean 43.22
Std Dev 12.12
Turn on : 24.6099
Width : 3.551
Height : 10.009
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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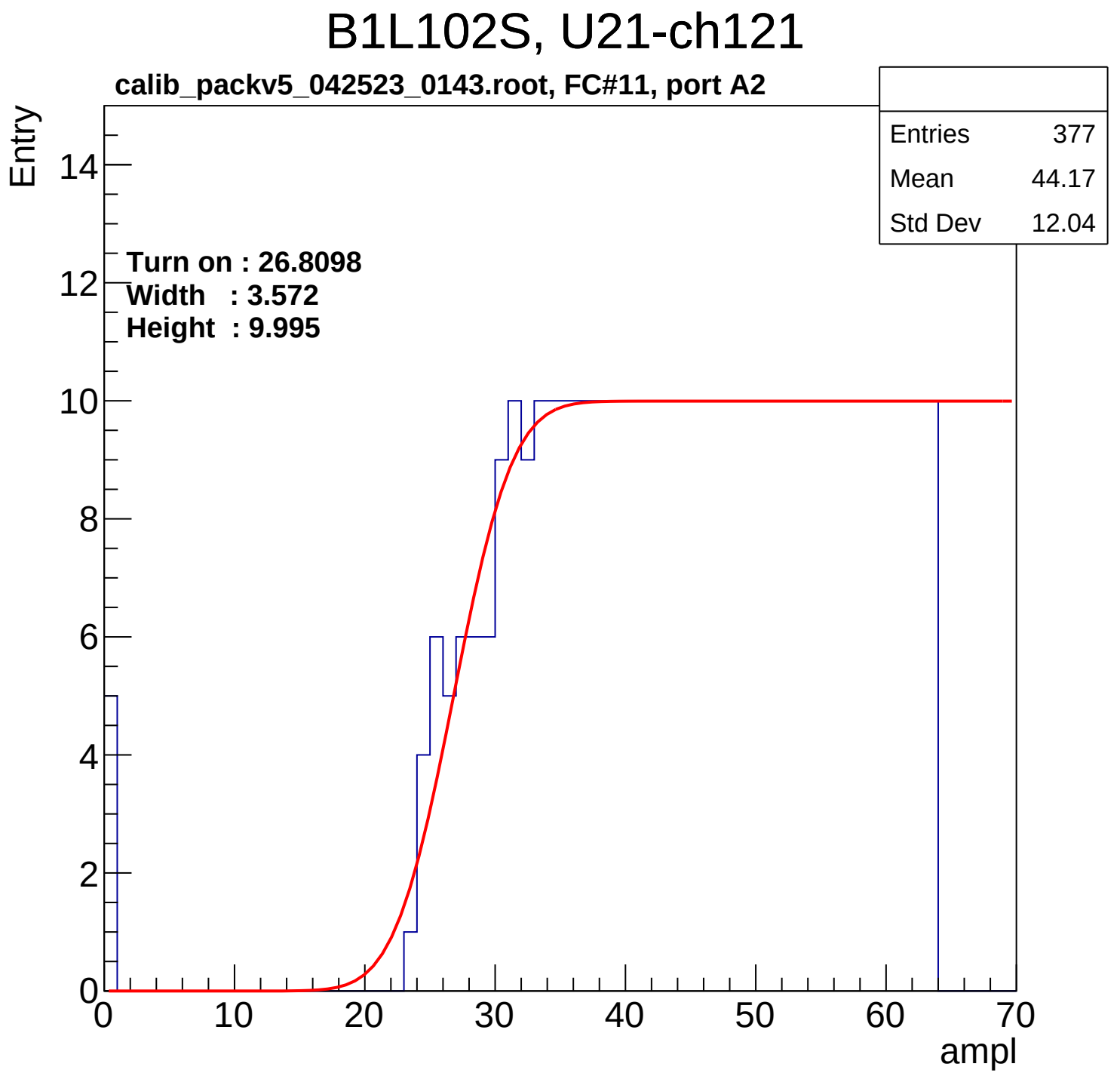
B1L102S, U21-ch121
calib_packv5_042523_0143.root, FC#11, port A2
Entries 377
Mean 44.17
Std Dev 12.04
Turn on : 26.8098
Width : 3.572
Height : 9.995
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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60
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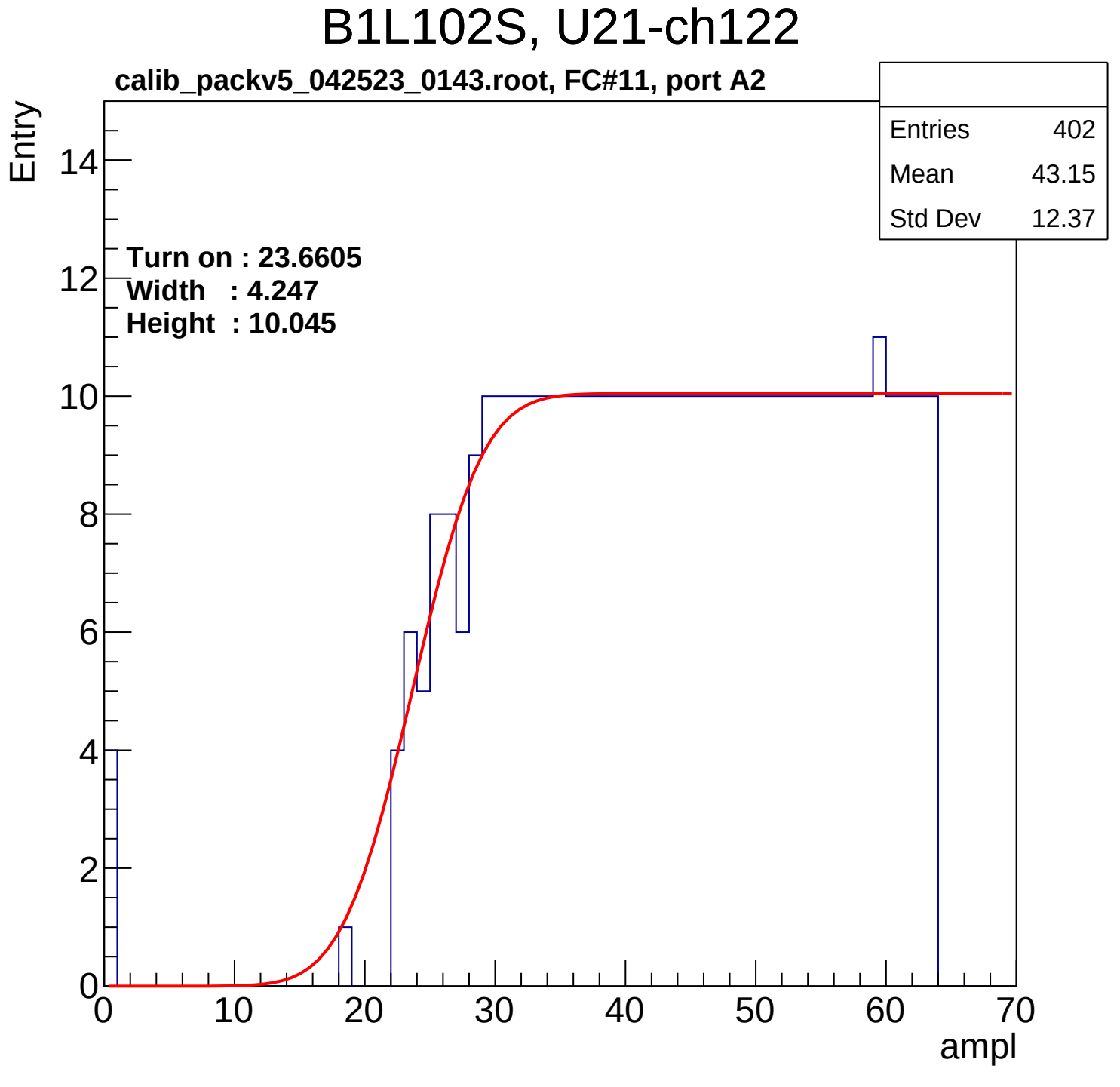
B1L102S, U21-ch122
calib_packv5_042523_0143.root, FC#11, port A2
Entries 402
Mean 43.15
Std Dev 12.37
Turn on : 23.6605
Width : 4.247
Height : 10.045
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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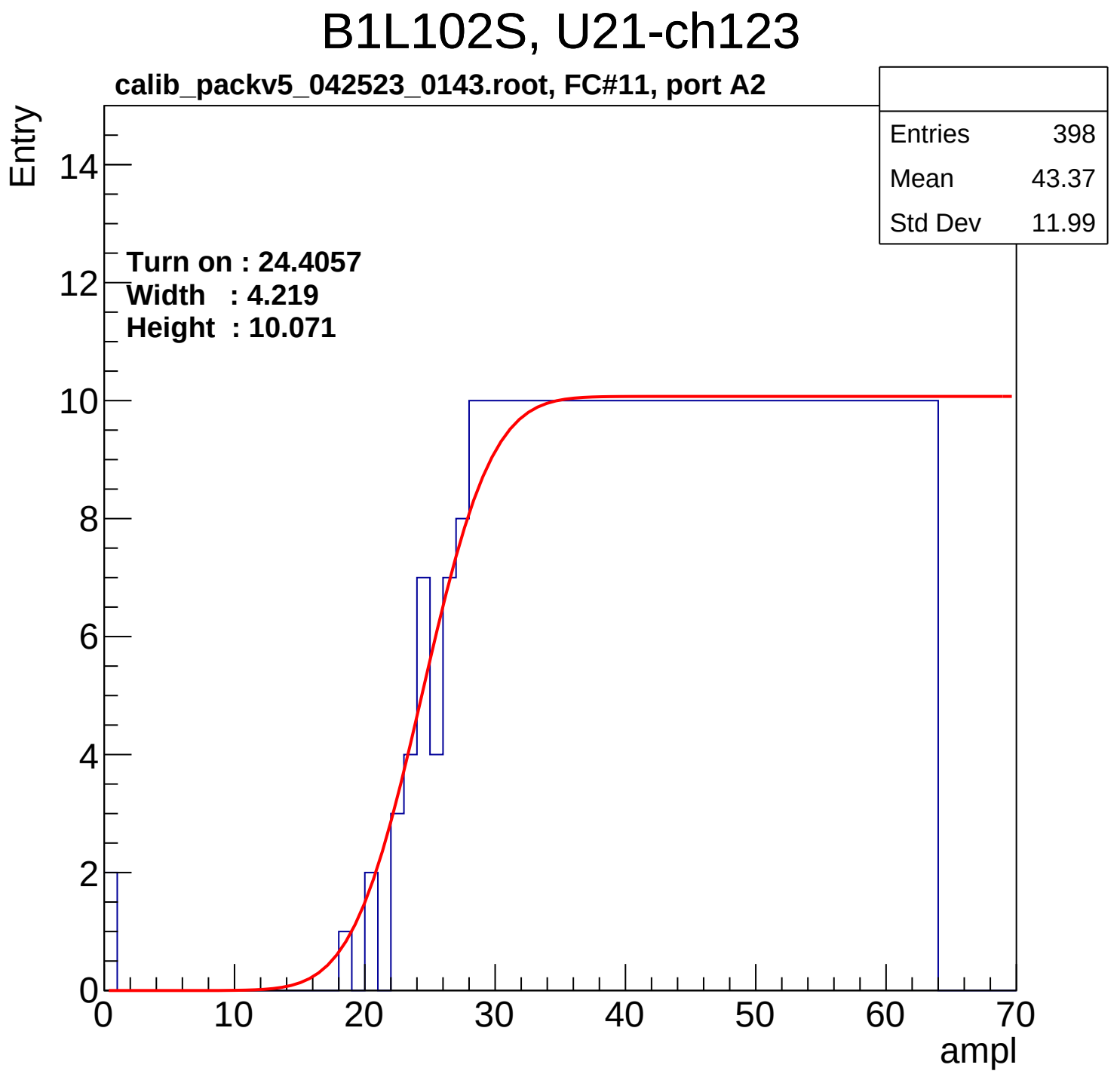
B1L102S, U21-ch123
calib_packv5_042523_0143.root, FC#11, port A2
Entries 398
Mean 43.37
Std Dev 11.99
Turn on : 24.4057
Width : 4.219
Height : 10.071
Entry
ampl
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2
4
6
8
10
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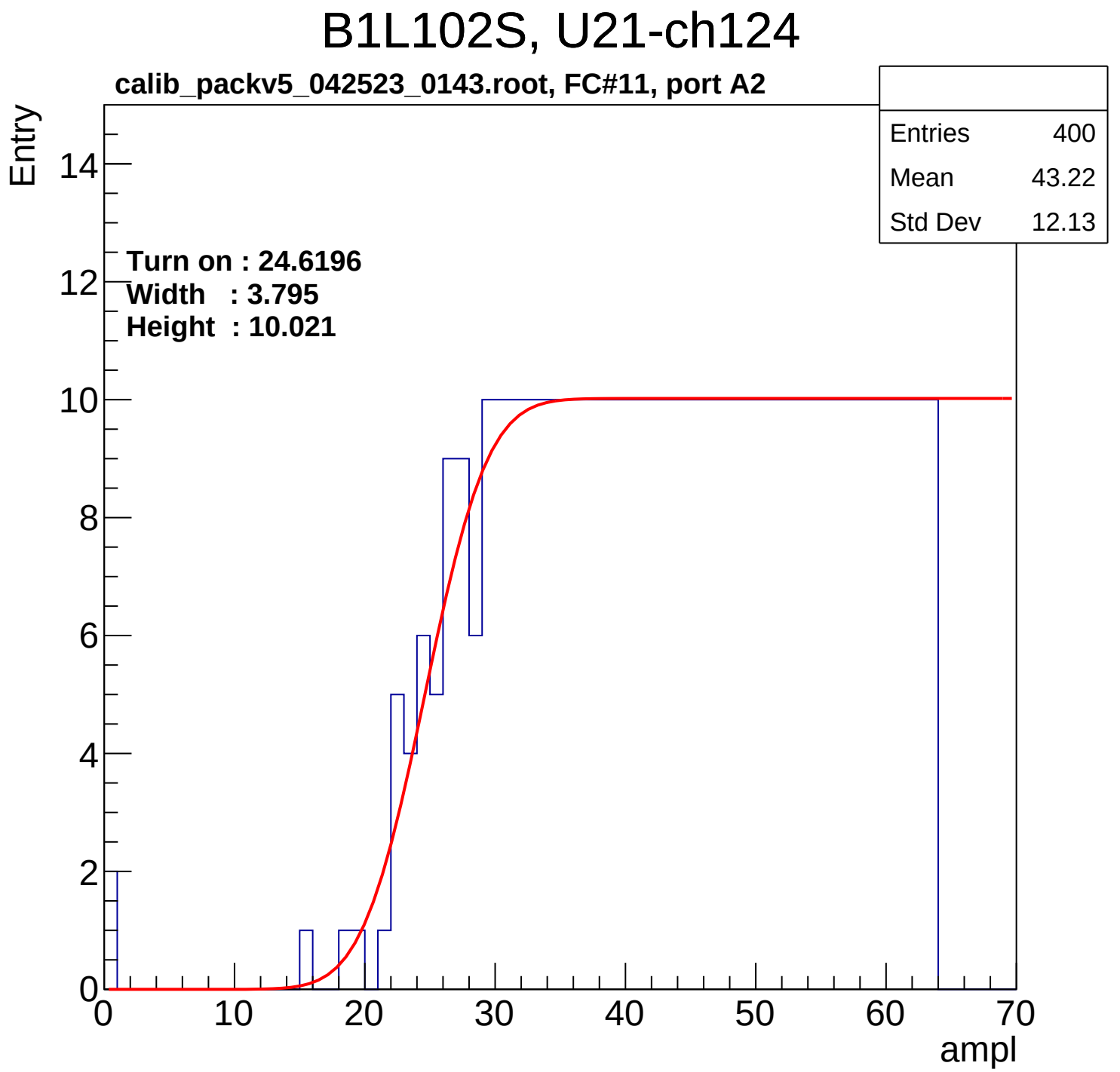
0
10
20
30
40
50
60
70


B1L102S, U21-ch124
calib_packv5_042523_0143.root, FC#11, port A2
Entries 400
Mean 43.22
Std Dev 12.13
Turn on : 24.6196
Width : 3.795
Height : 10.021
Entry
ampl
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4
6
8
10
12
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0
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20
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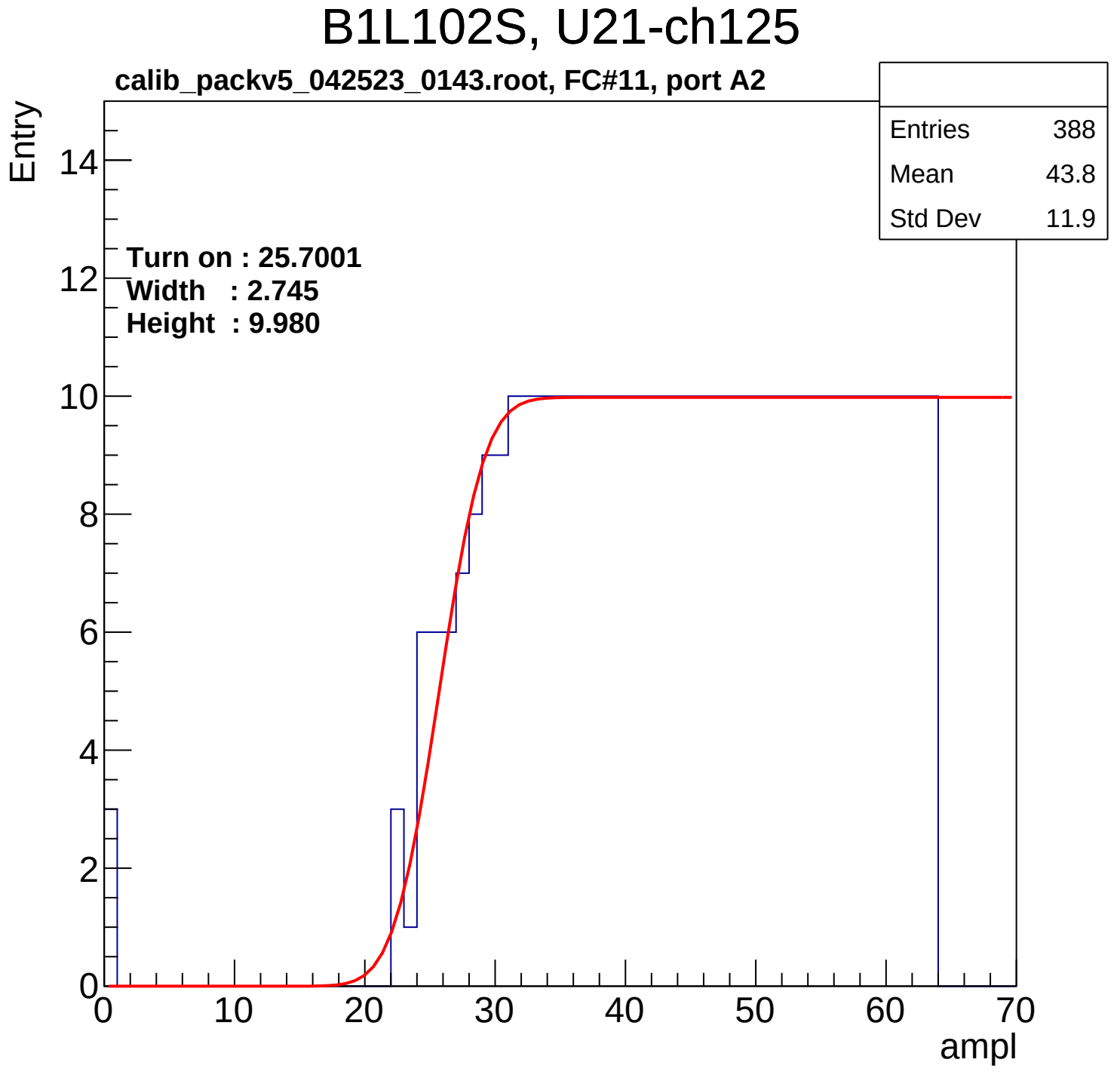
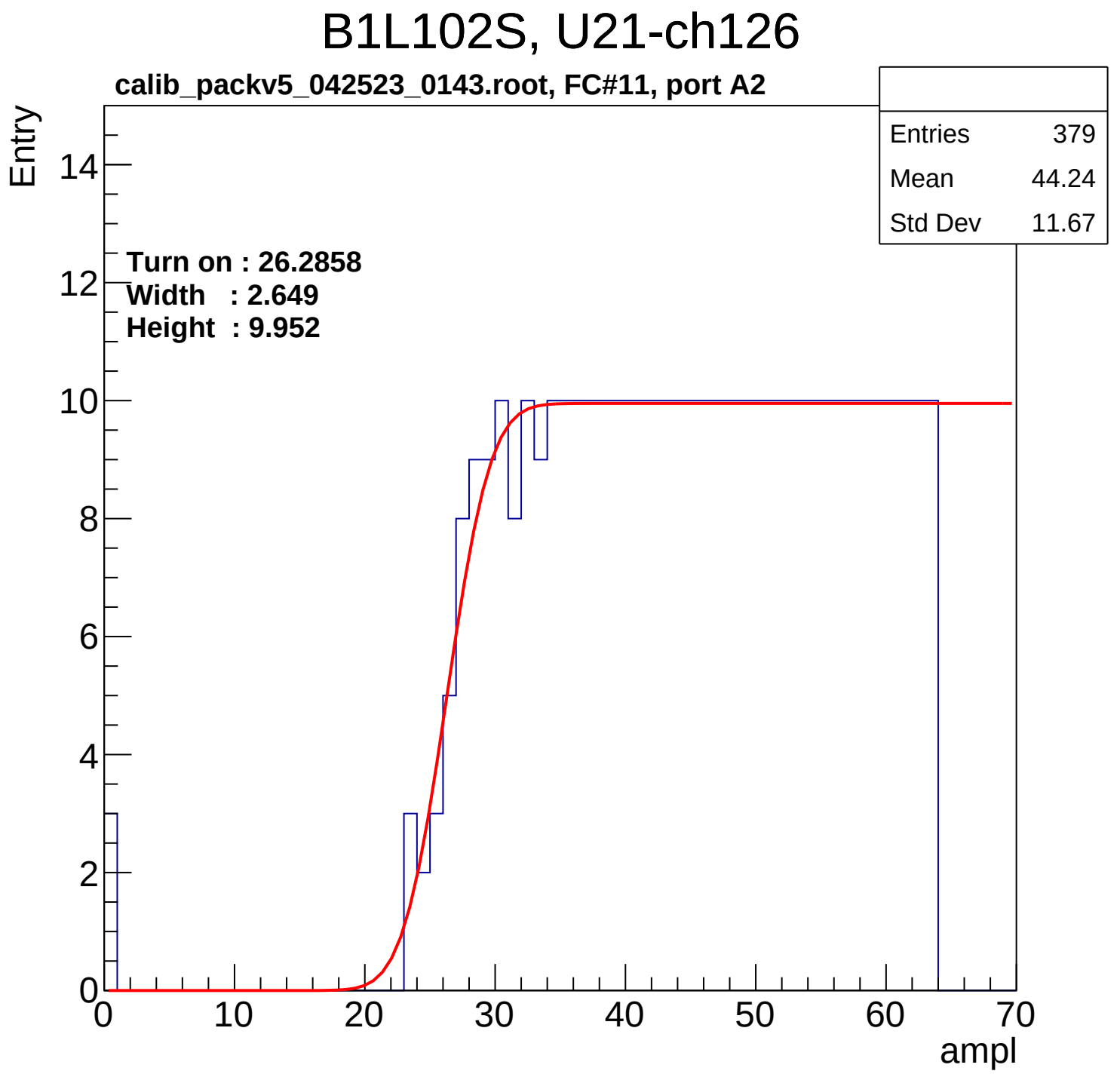
40
50
60
70


B1L102S, U21-ch125
calib_packv5_042523_0143.root, FC#11, port A2
Entries 388
Mean 43.8
Std Dev 11.9
Turn on : 25.7001
Width : 2.745
Height : 9.980
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L102S, U21-ch126
calib_packv5_042523_0143.root, FC#11, port A2
Entries 379
Mean 44.24
Std Dev 11.67
Turn on : 26.2858
Width : 2.649
Height : 9.952
Entry
ampl
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2
4
6
8
10
12
14
0
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20
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40
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60
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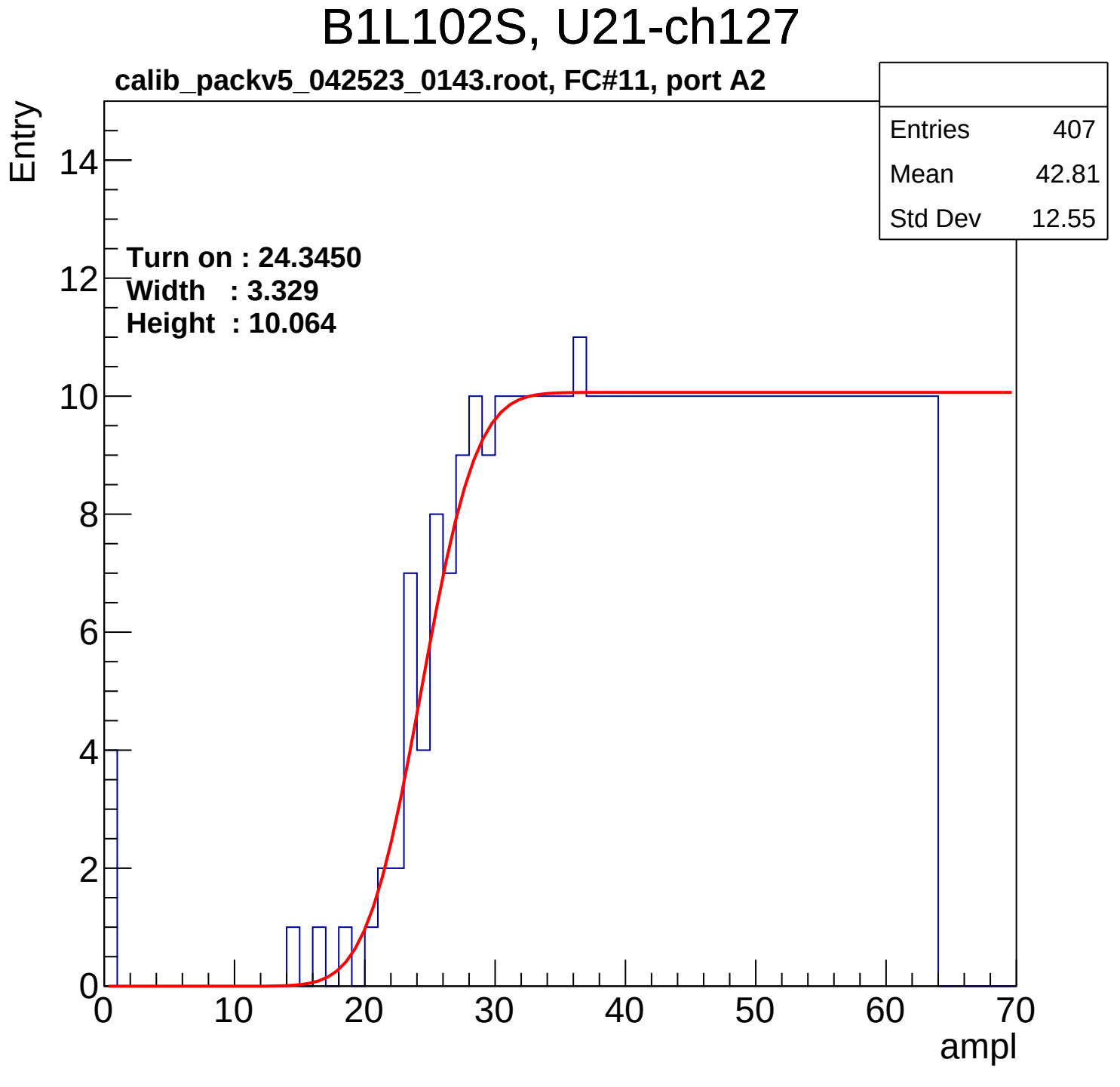
B1L102S, U21-ch127
calib_packv5_042523_0143.root, FC#11, port A2
Entries 407
Mean 42.81
Std Dev 12.55
Turn on : 24.3450
Width : 3.329
Height : 10.064
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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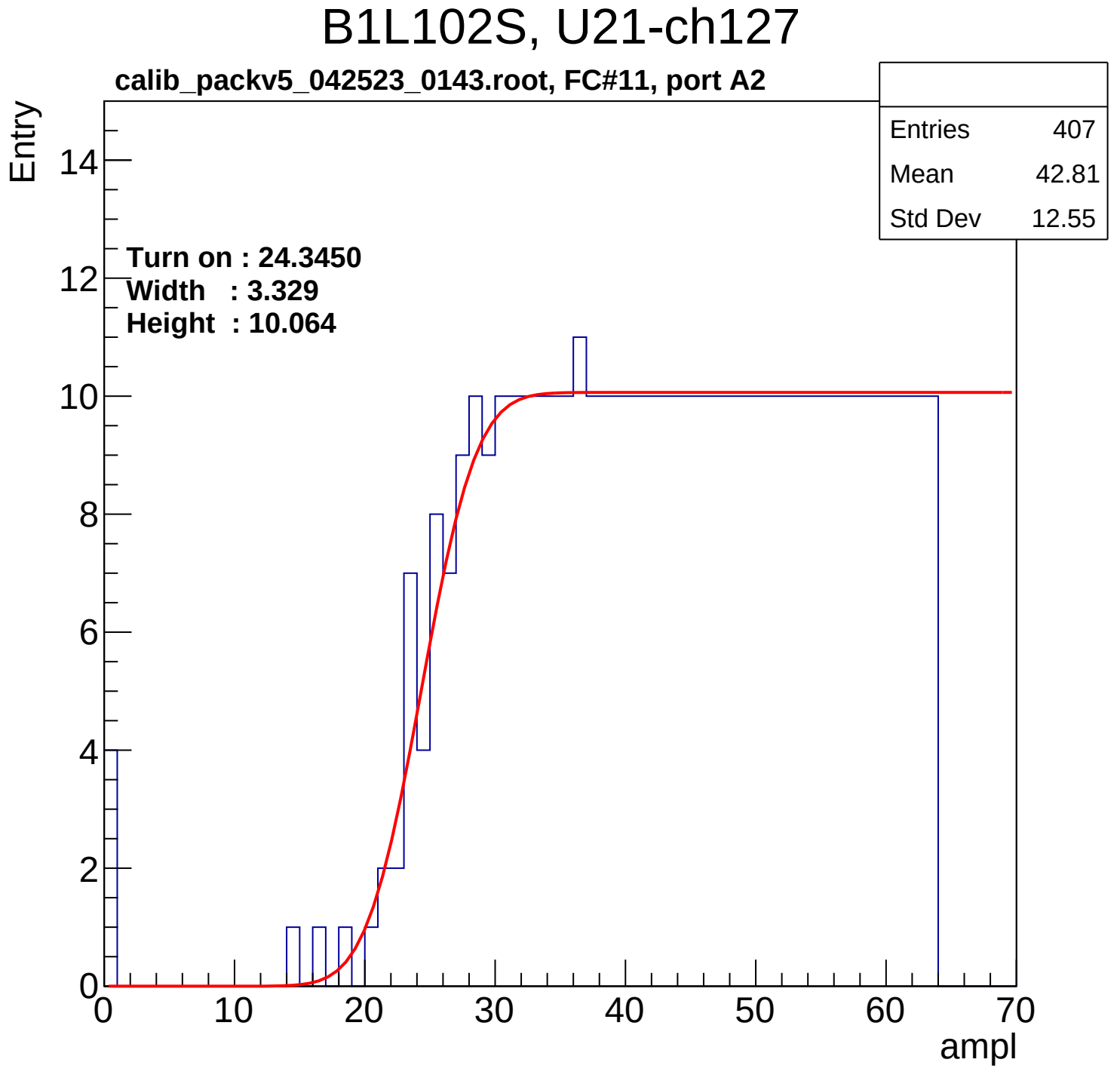
B1L102S, U21-ch127
calib_packv5_042523_0143.root, FC#11, port A2
Entries 407
Mean 42.81
Std Dev 12.55
Turn on : 24.3450
Width : 3.329
Height : 10.064
Entry
ampl
0
2
4
6
8
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12
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0
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40
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