



# B1L102S, U20-ch0, adc0

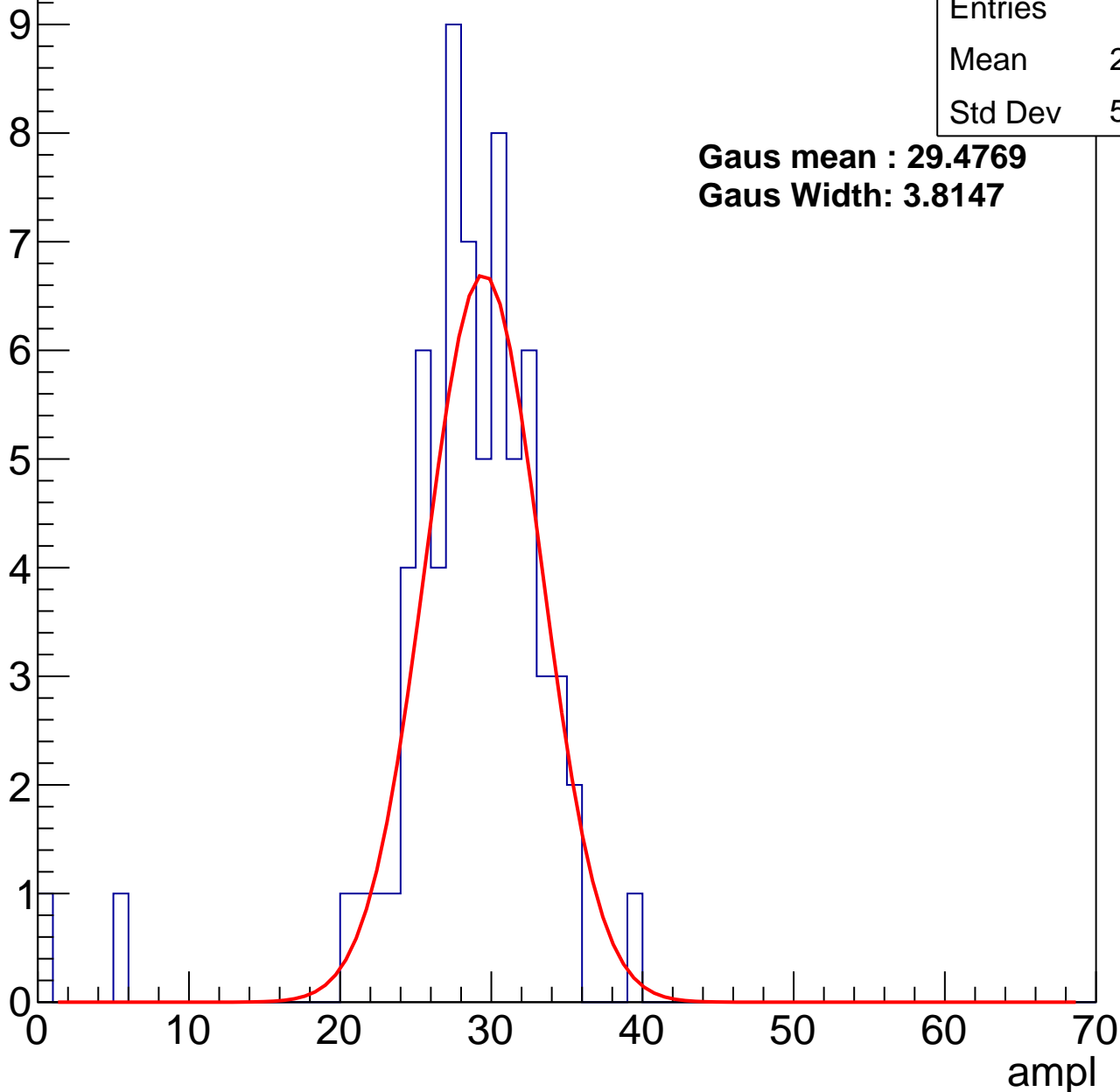
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	27.86
Std Dev	5.658

**Gaus mean : 29.4769**

**Gaus Width: 3.8147**



# B1L102S, U20-ch0, adc1

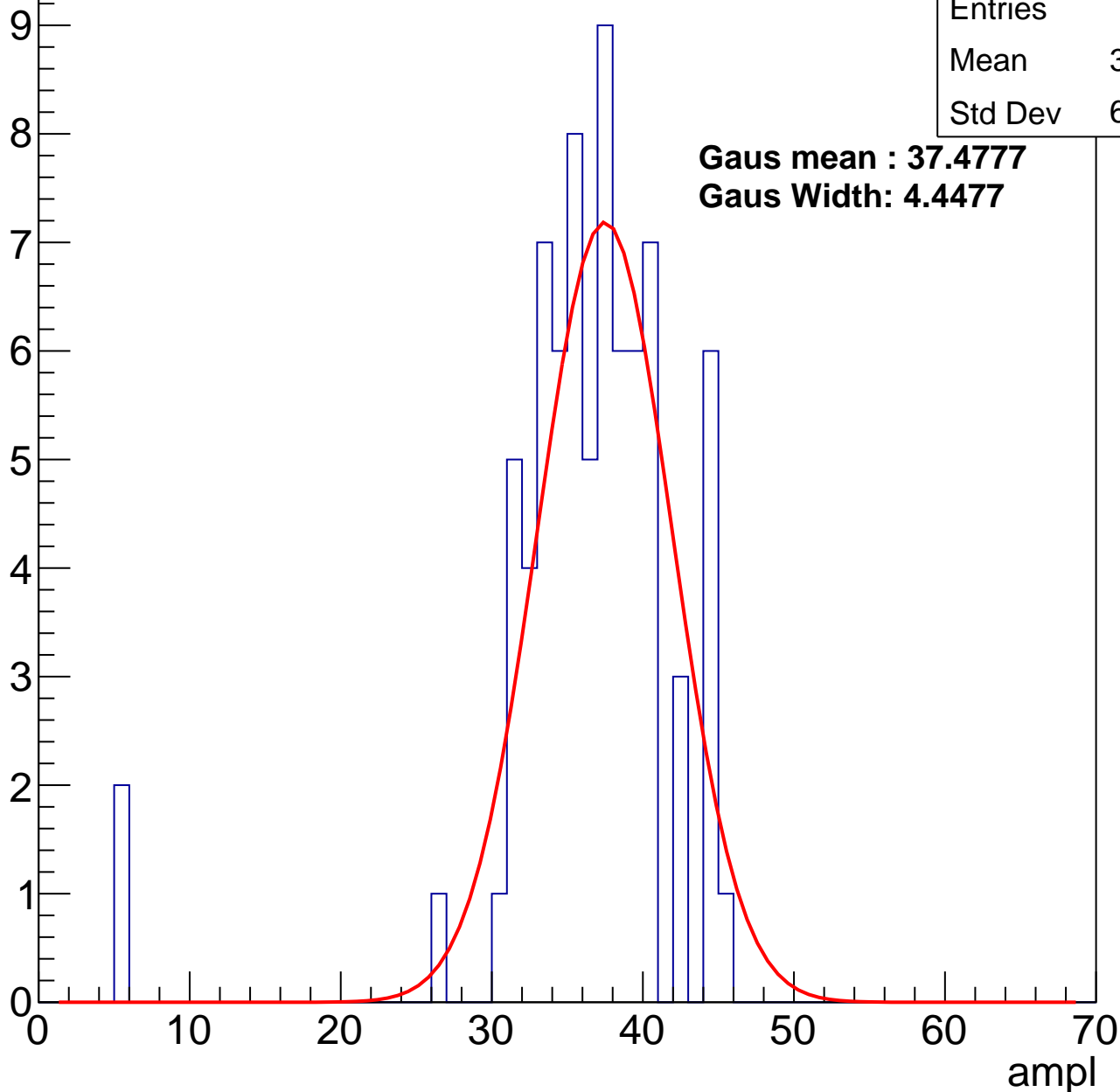
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	35.77
Std Dev	6.355

**Gaus mean : 37.4777**

**Gaus Width: 4.4477**



# B1L102S, U20-ch0, adc2

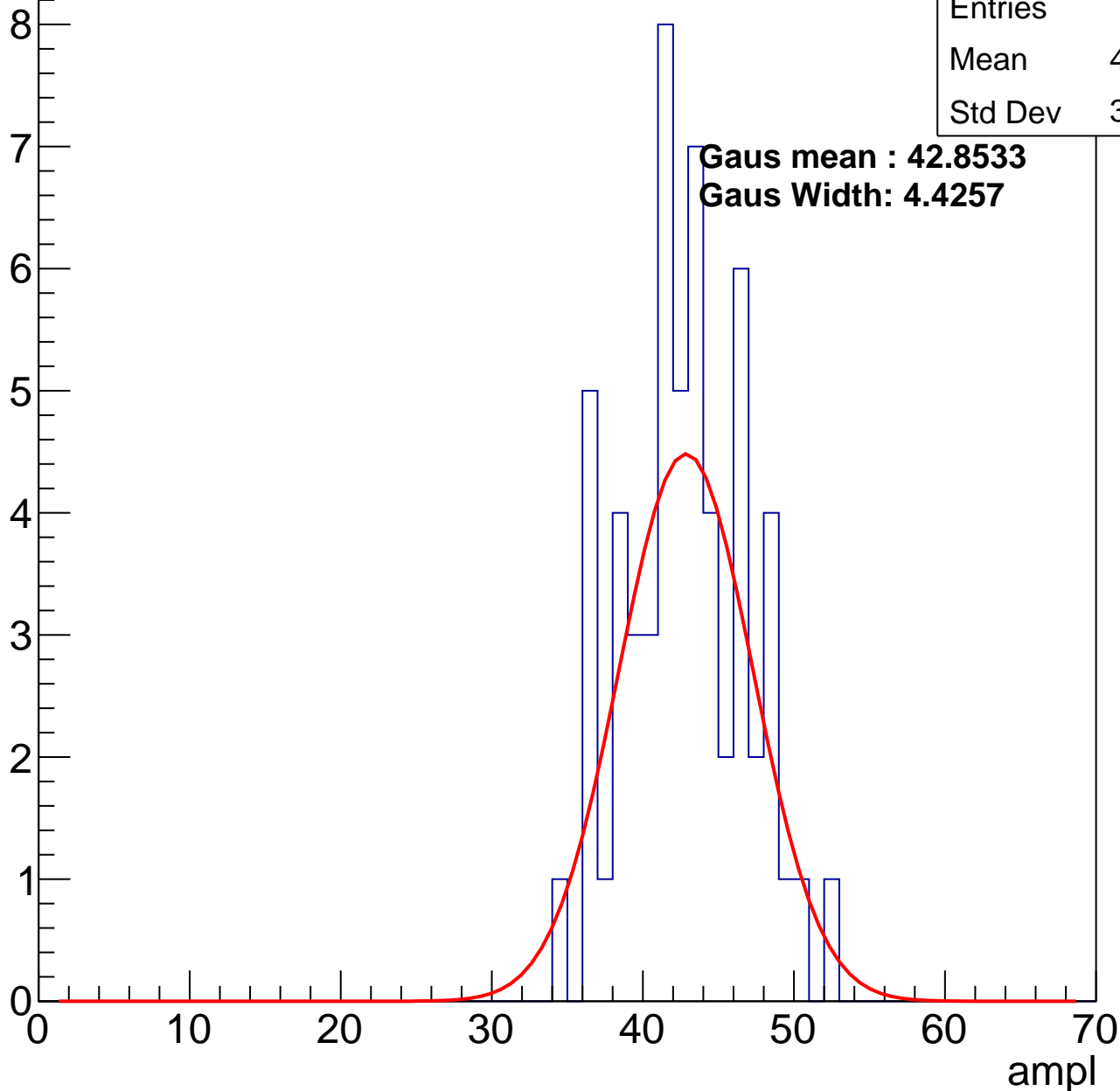
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	42.38
Std Dev	3.973

**Gaus mean : 42.8533**

**Gaus Width: 4.4257**

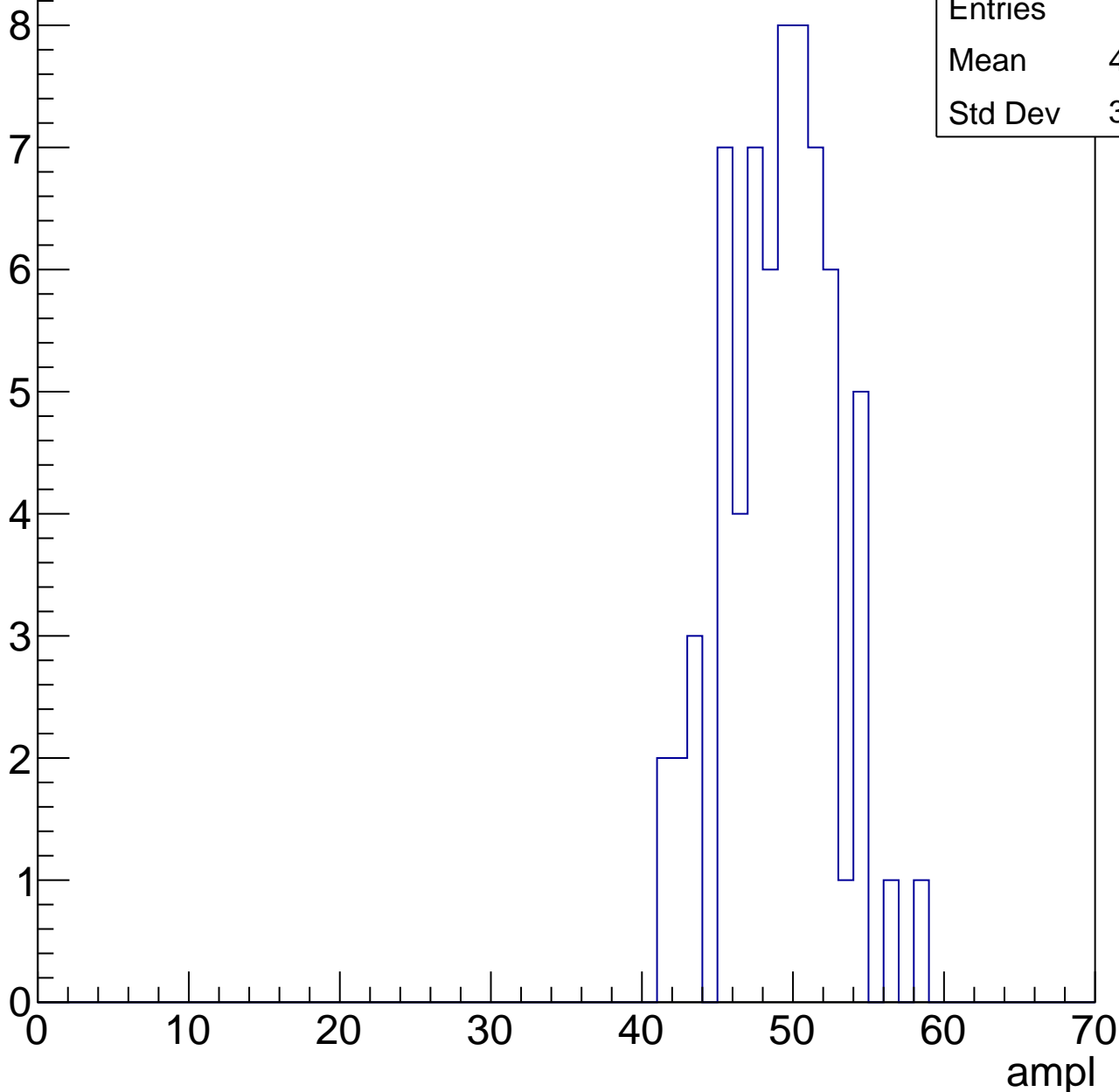


# B1L102S, U20-ch0, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	48.66
Std Dev	3.575

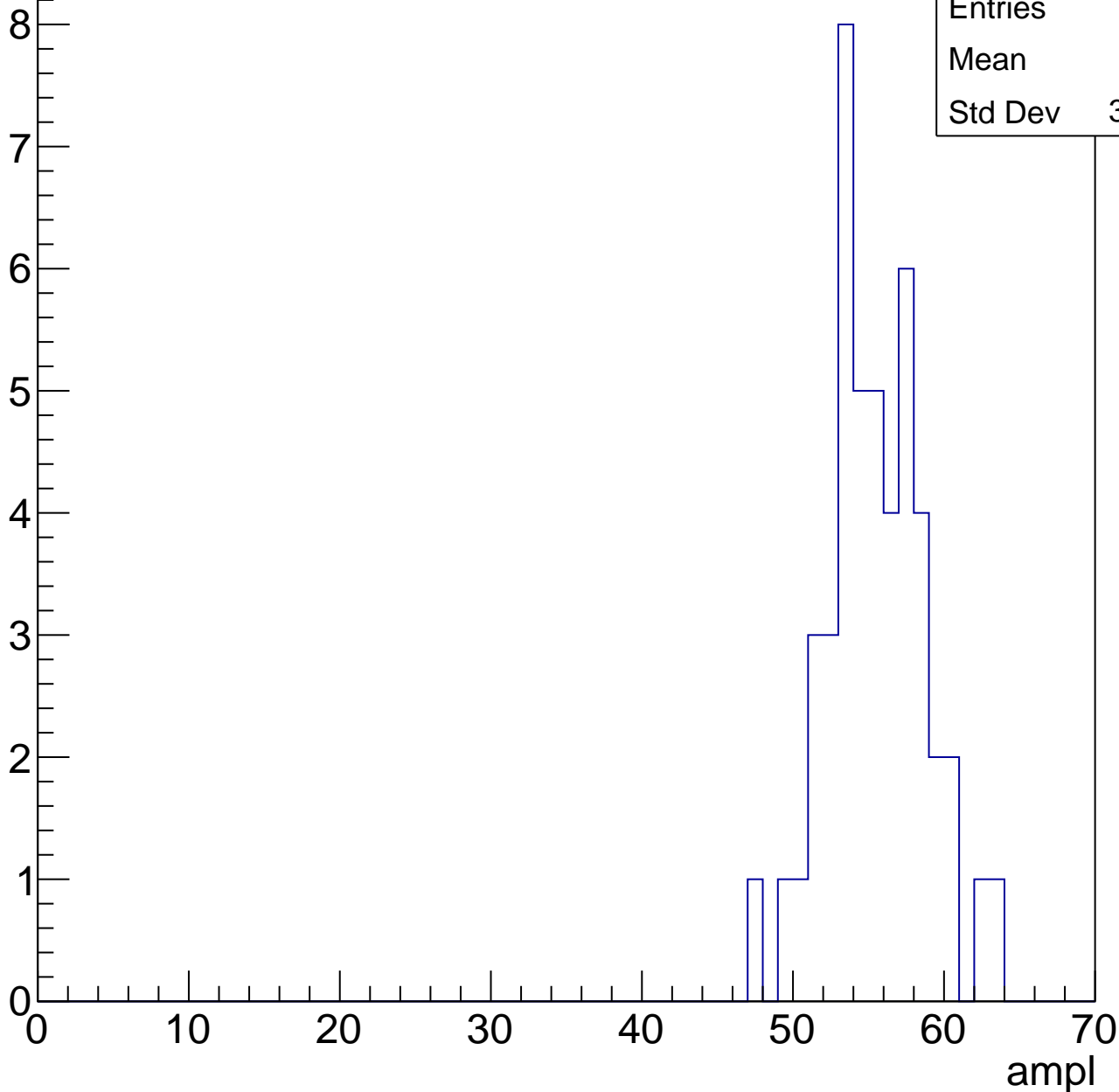


# B1L102S, U20-ch0, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	47
Mean	55
Std Dev	3.249

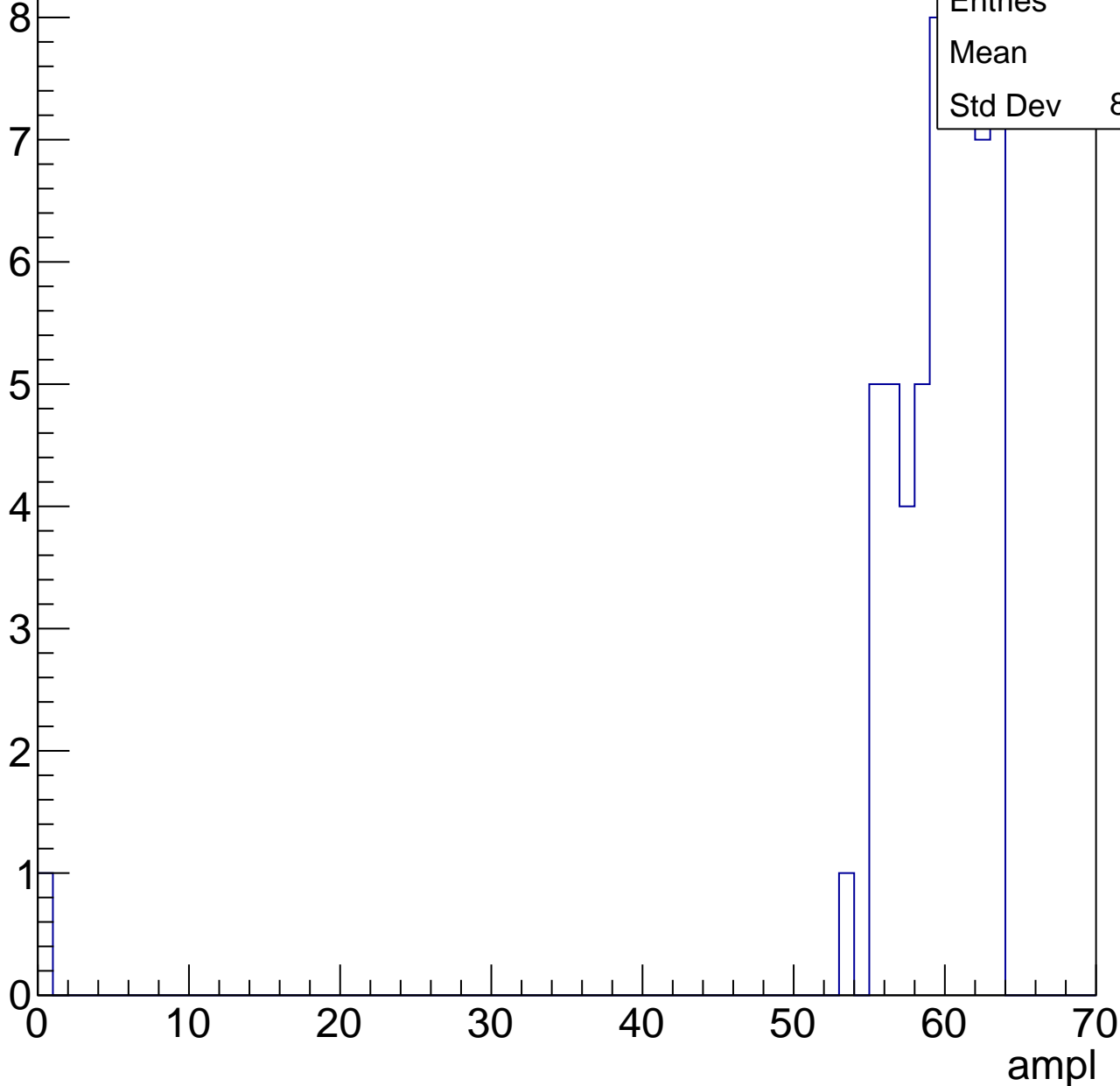


# B1L102S, U20-ch0, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	58.4
Std Dev	8.034



# B1L102S, U20-ch0, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

0

10

20

30

40

50

60

ampl

Entries	5
Mean	61.8
Std Dev	0.7483



# B1L102S, U20-ch0, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch1, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	77
Mean	30.22
Std Dev	3.737

**Gaus mean : 30.6773**

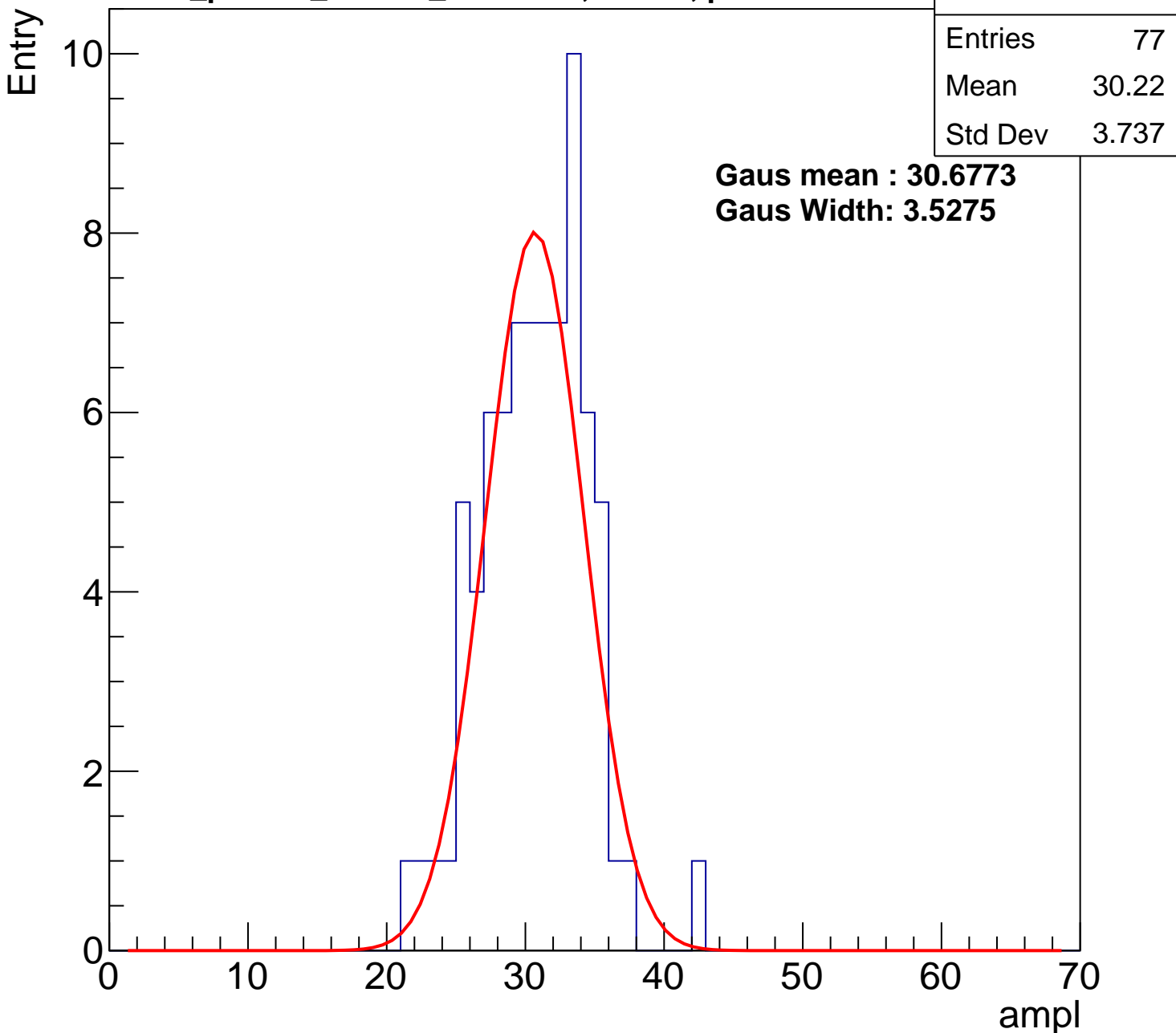
**Gaus Width: 3.5275**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U20-ch1, adc1

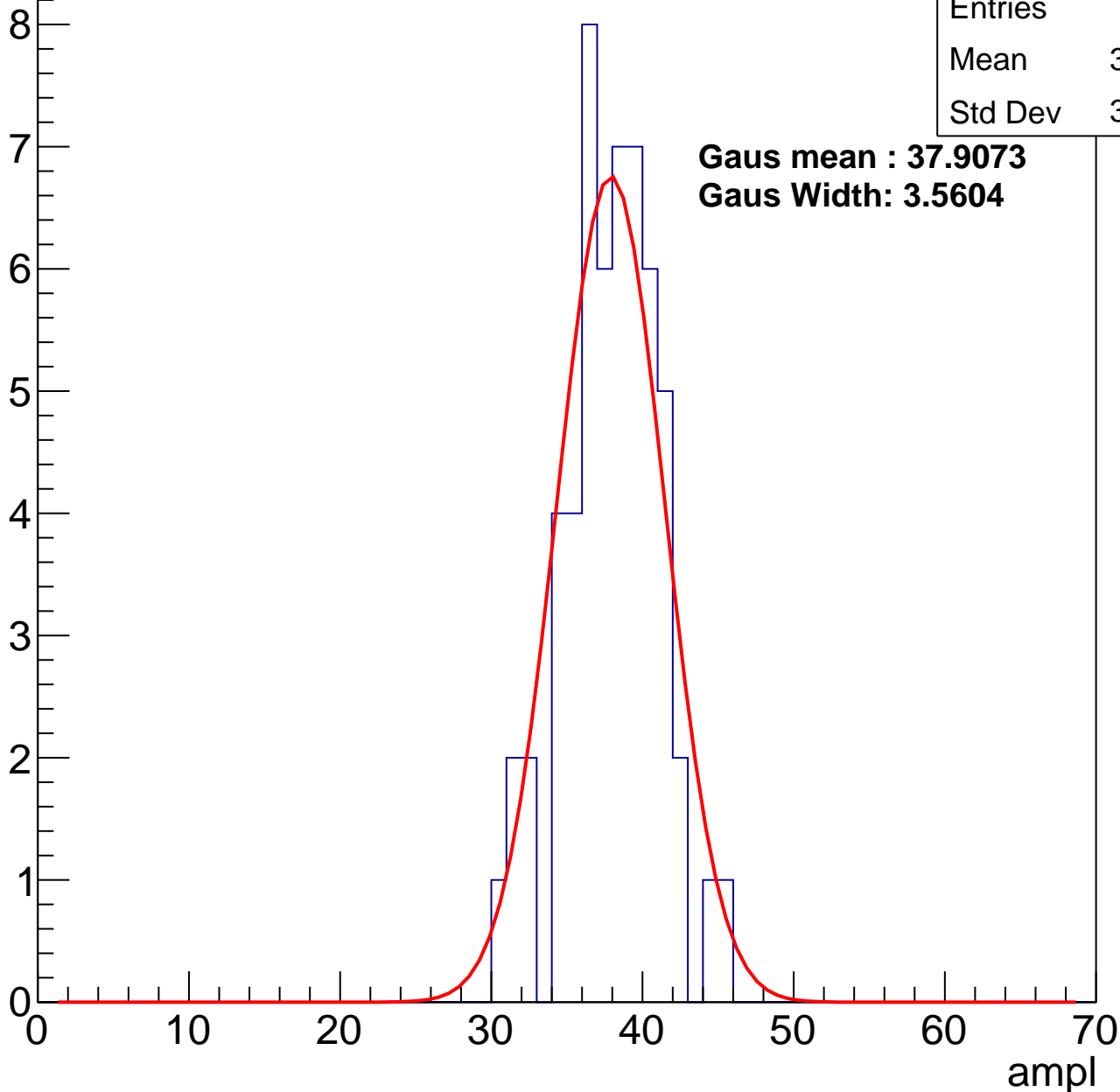
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	37.48
Std Dev	3.134

**Gaus mean : 37.9073**

**Gaus Width: 3.5604**



# B1L102S, U20-ch1, adc2

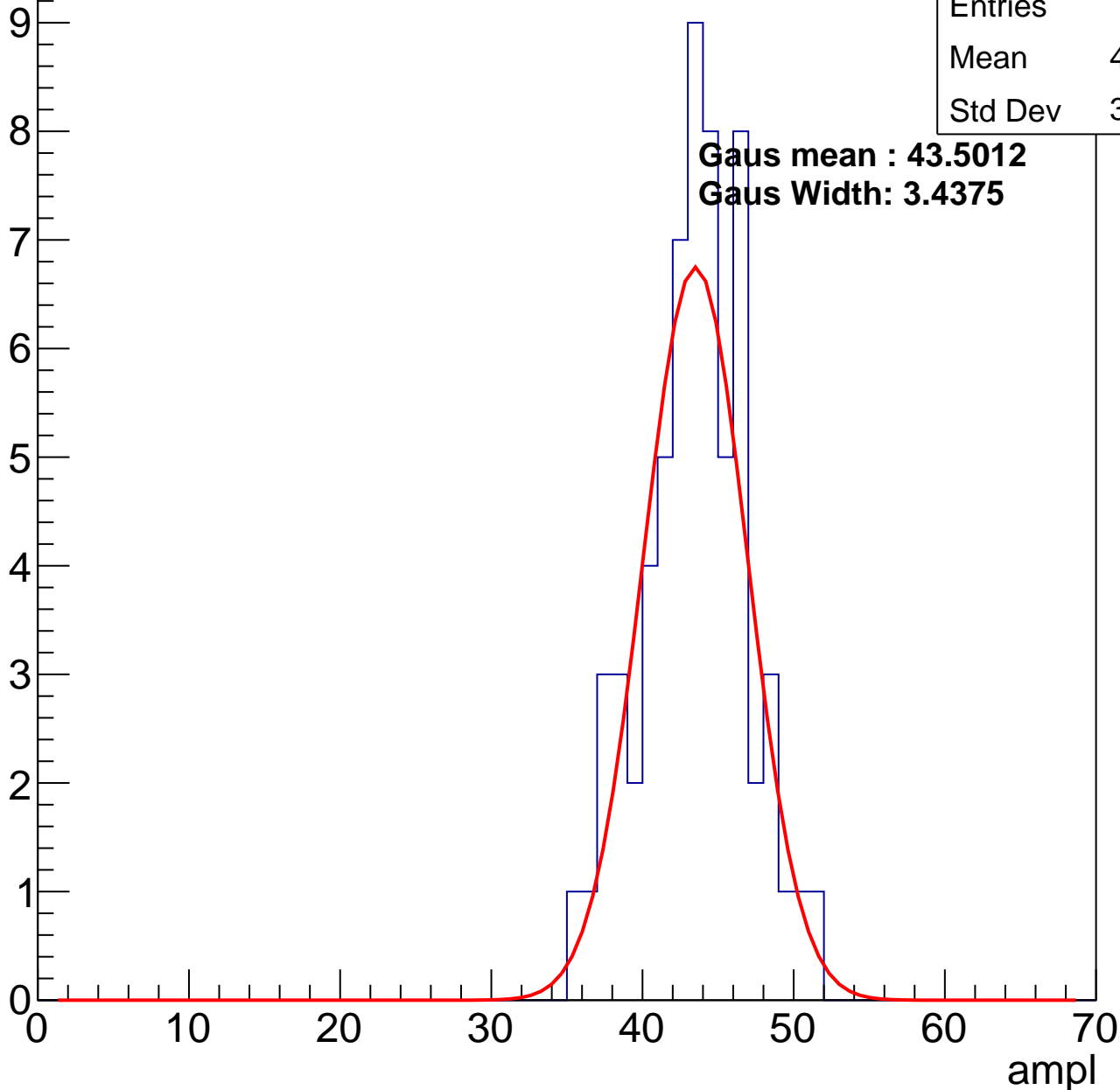
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	43.02
Std Dev	3.416

**Gaus mean : 43.5012**

**Gaus Width: 3.4375**

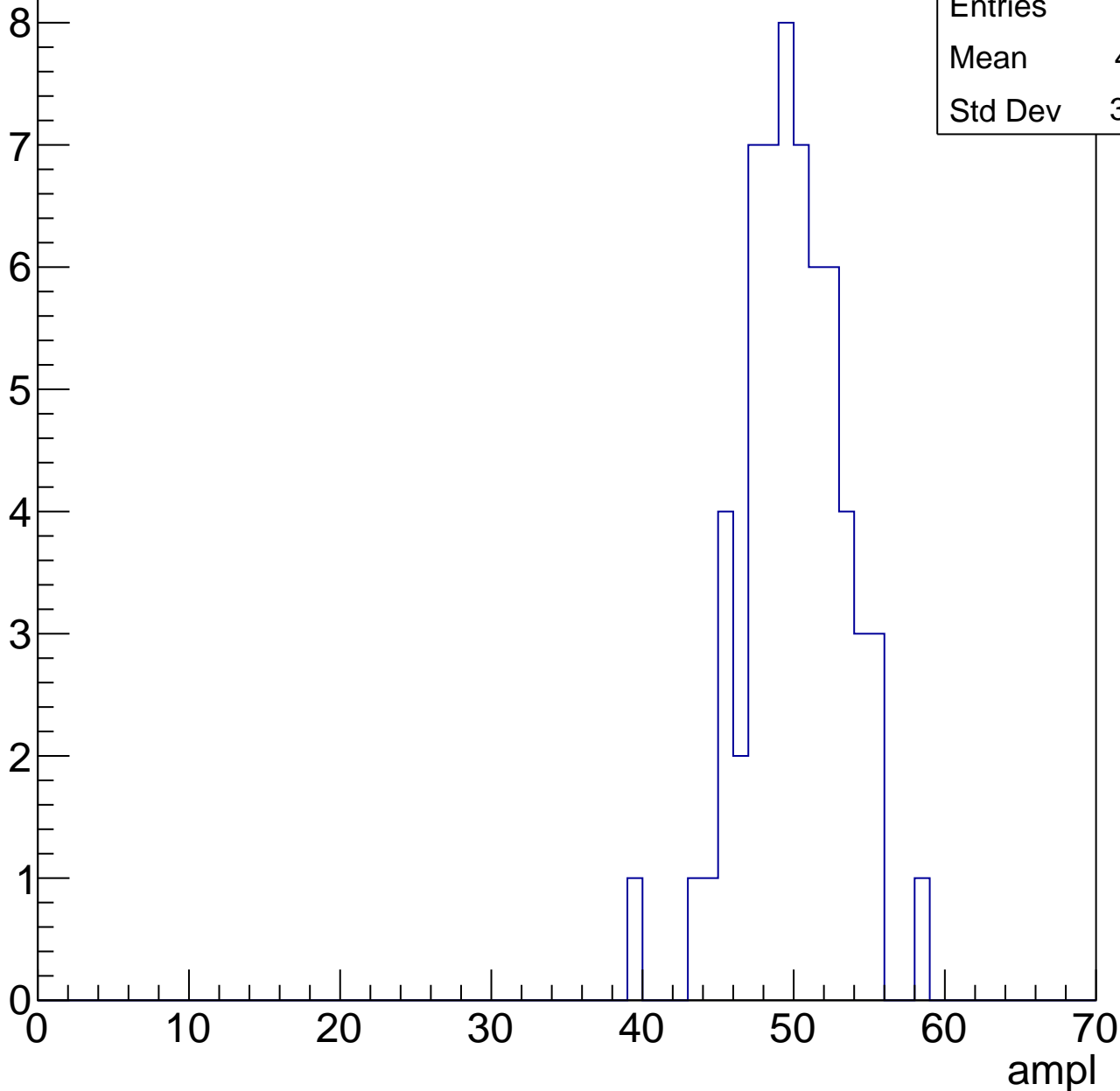


# B1L102S, U20-ch1, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

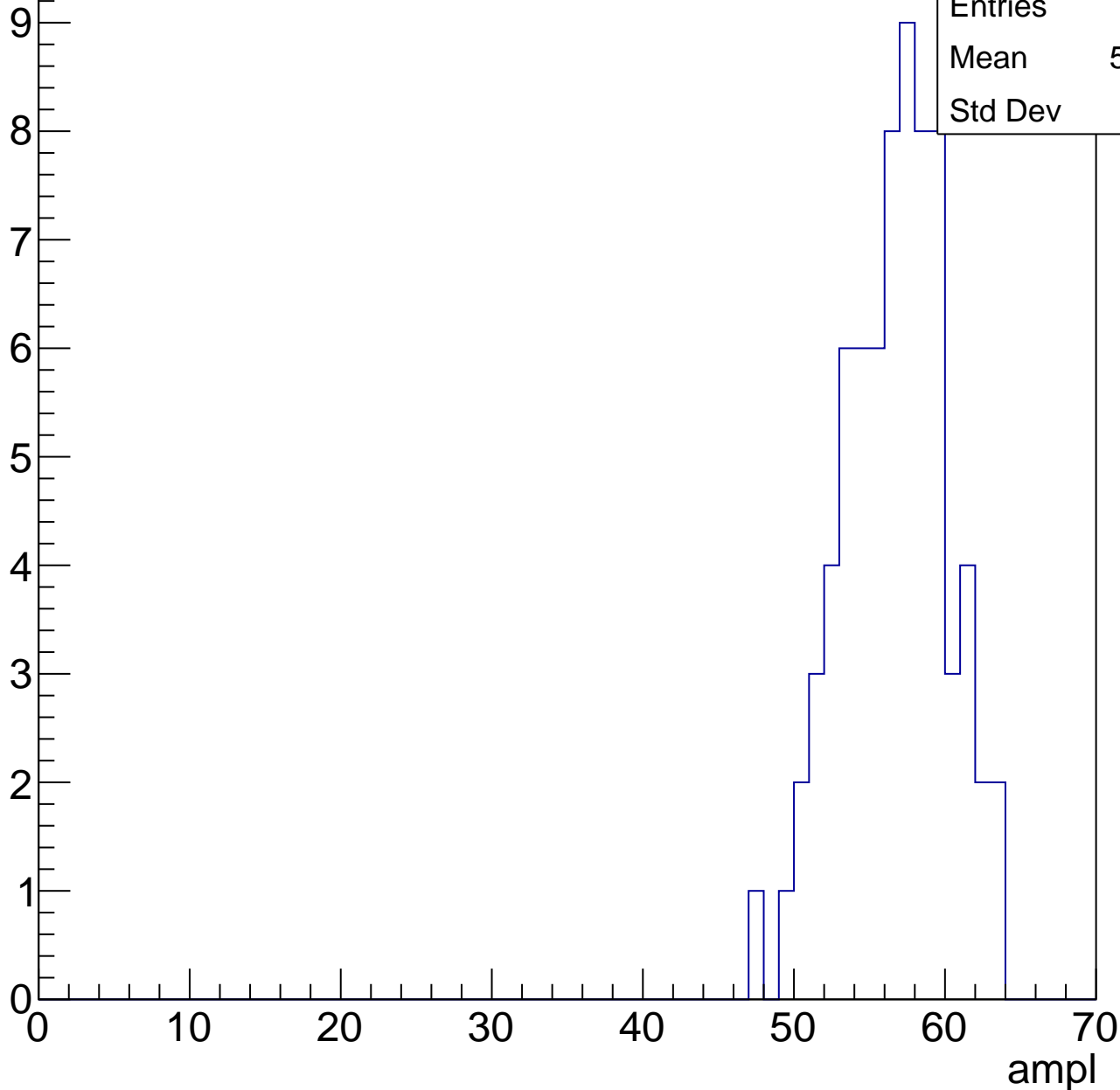
Entries	61
Mean	49.51
Std Dev	3.327



# B1L102S, U20-ch1, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

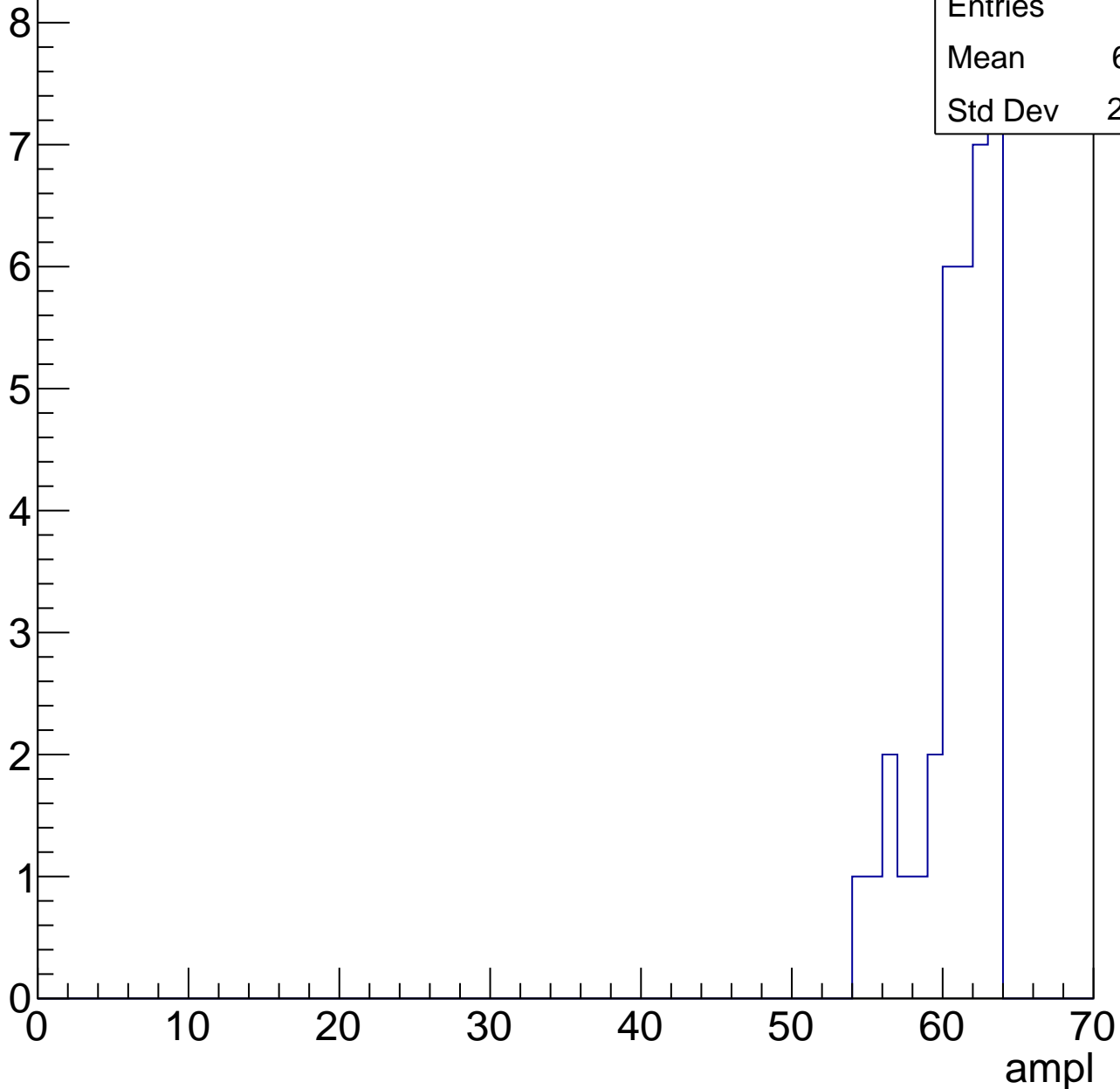


# B1L102S, U20-ch1, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

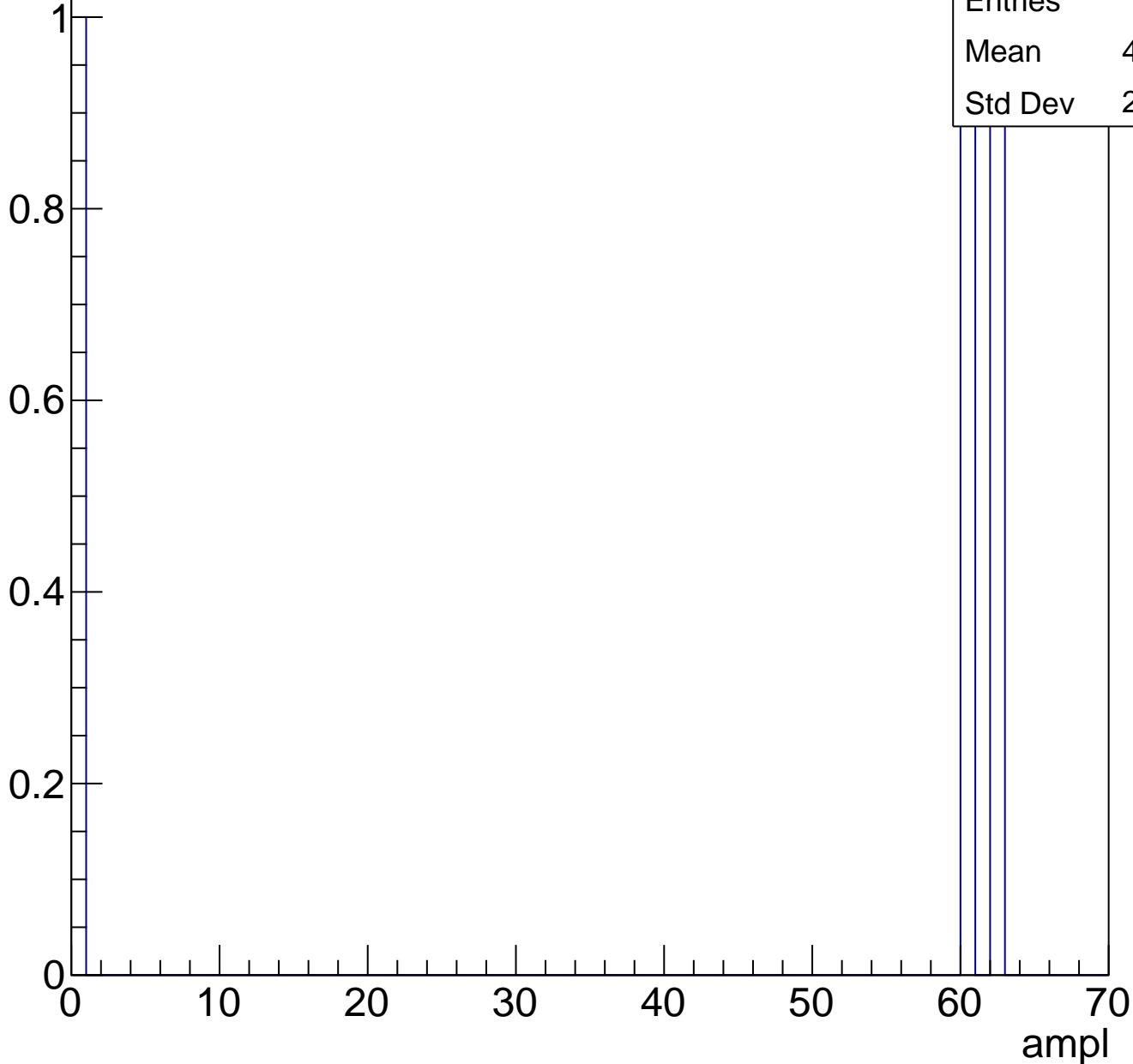
Entries	35
Mean	60.51
Std Dev	2.419



# B1L102S, U20-ch1, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U20-ch1, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L102S, U20-ch2, adc0

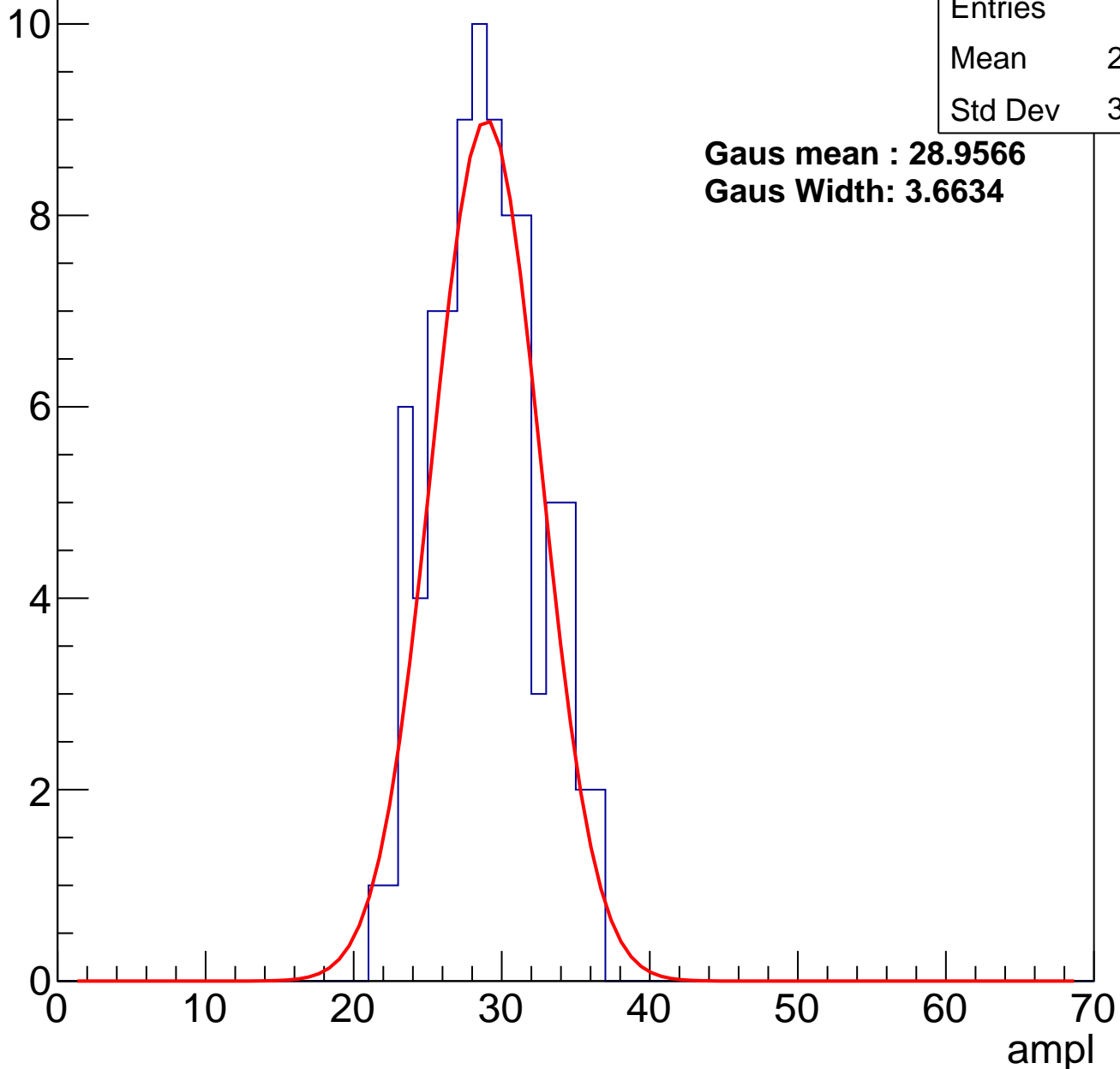
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	87
Mean	28.49
Std Dev	3.507

**Gaus mean : 28.9566**

**Gaus Width: 3.6634**

Entry



# B1L102S, U20-ch2, adc1

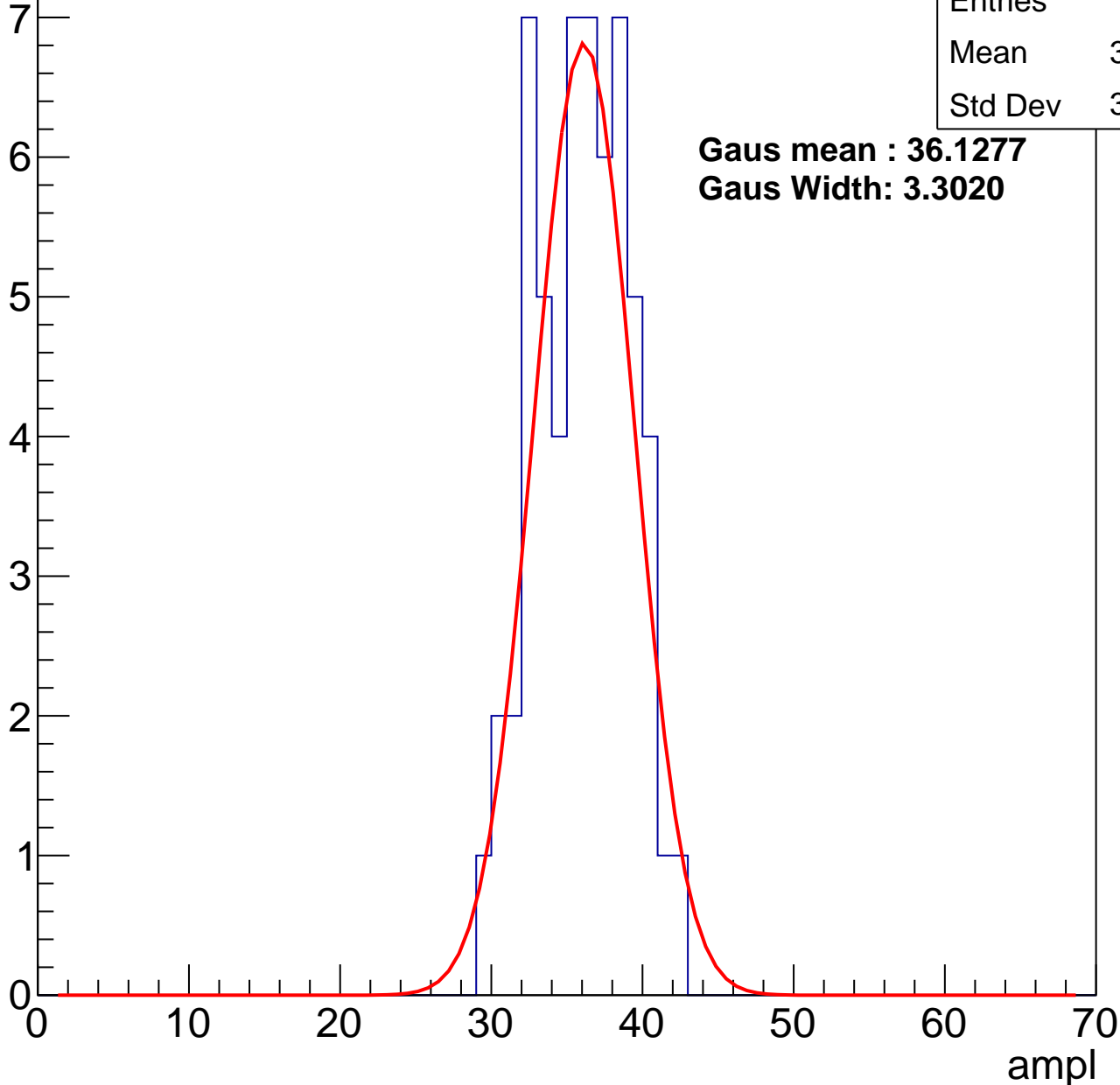
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	35.58
Std Dev	3.038

**Gaus mean : 36.1277**

**Gaus Width: 3.3020**



# B1L102S, U20-ch2, adc2

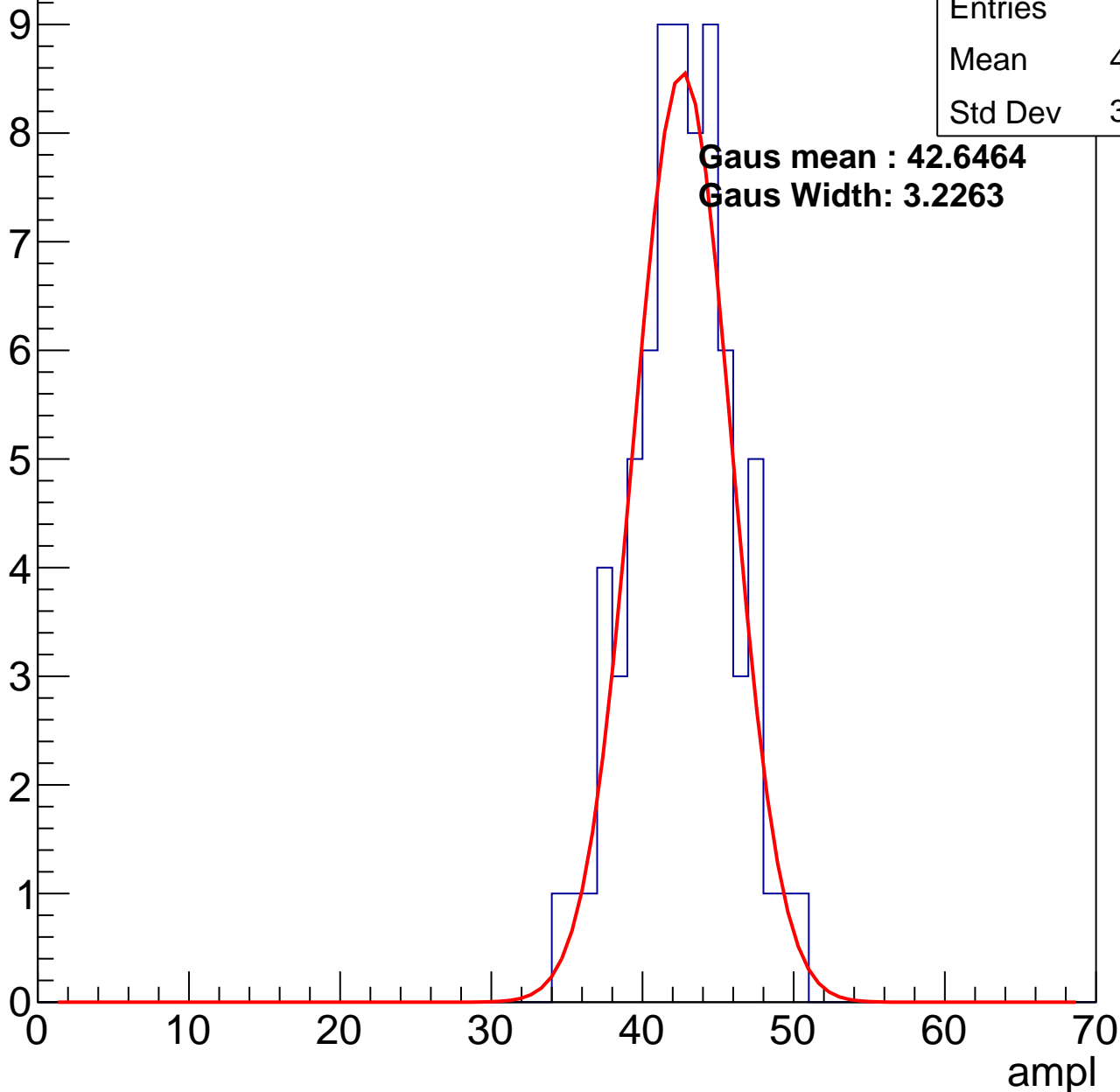
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	42.18
Std Dev	3.295

**Gaus mean : 42.6464**

**Gaus Width: 3.2263**

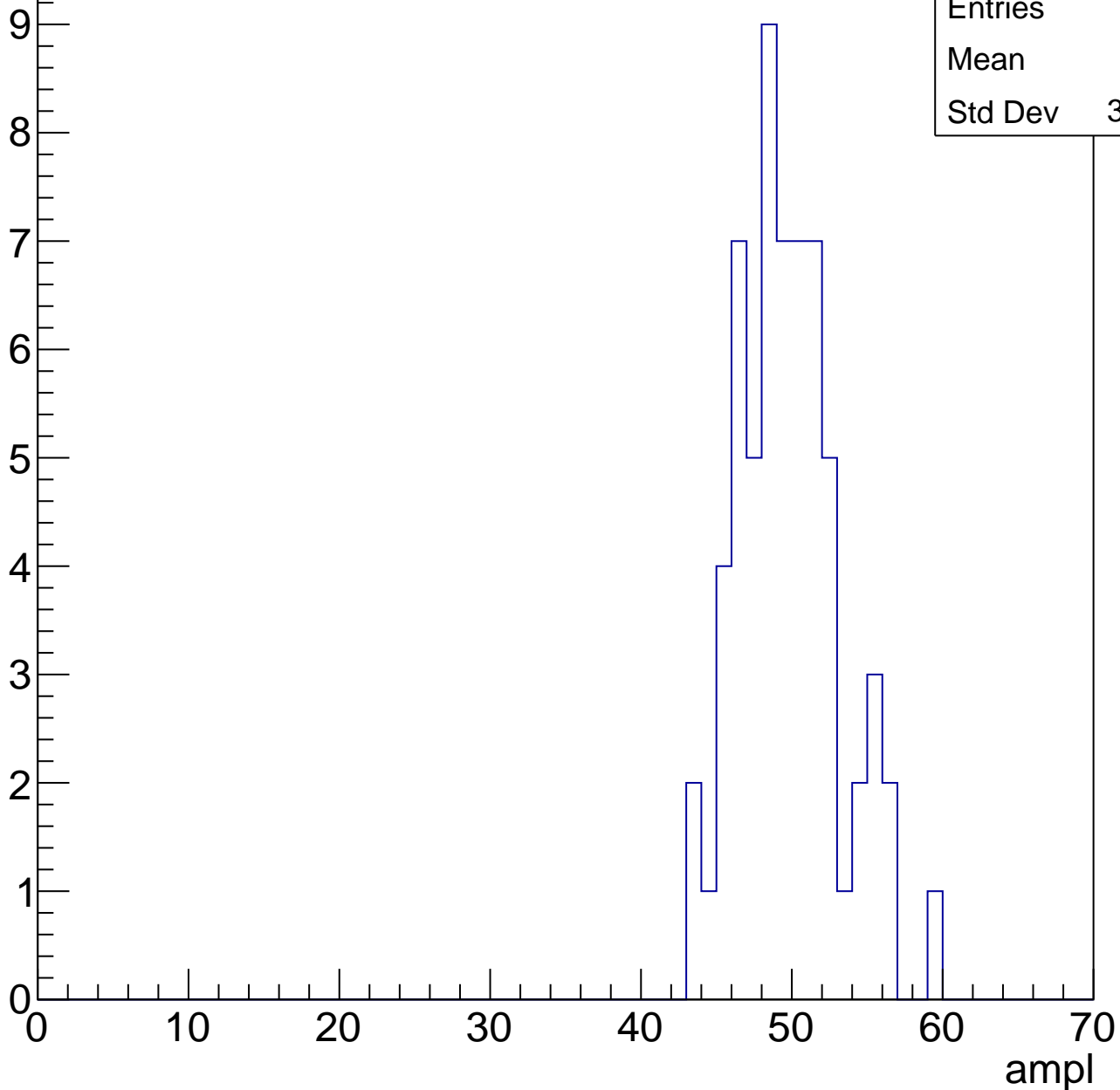


# B1L102S, U20-ch2, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	49.3
Std Dev	3.332

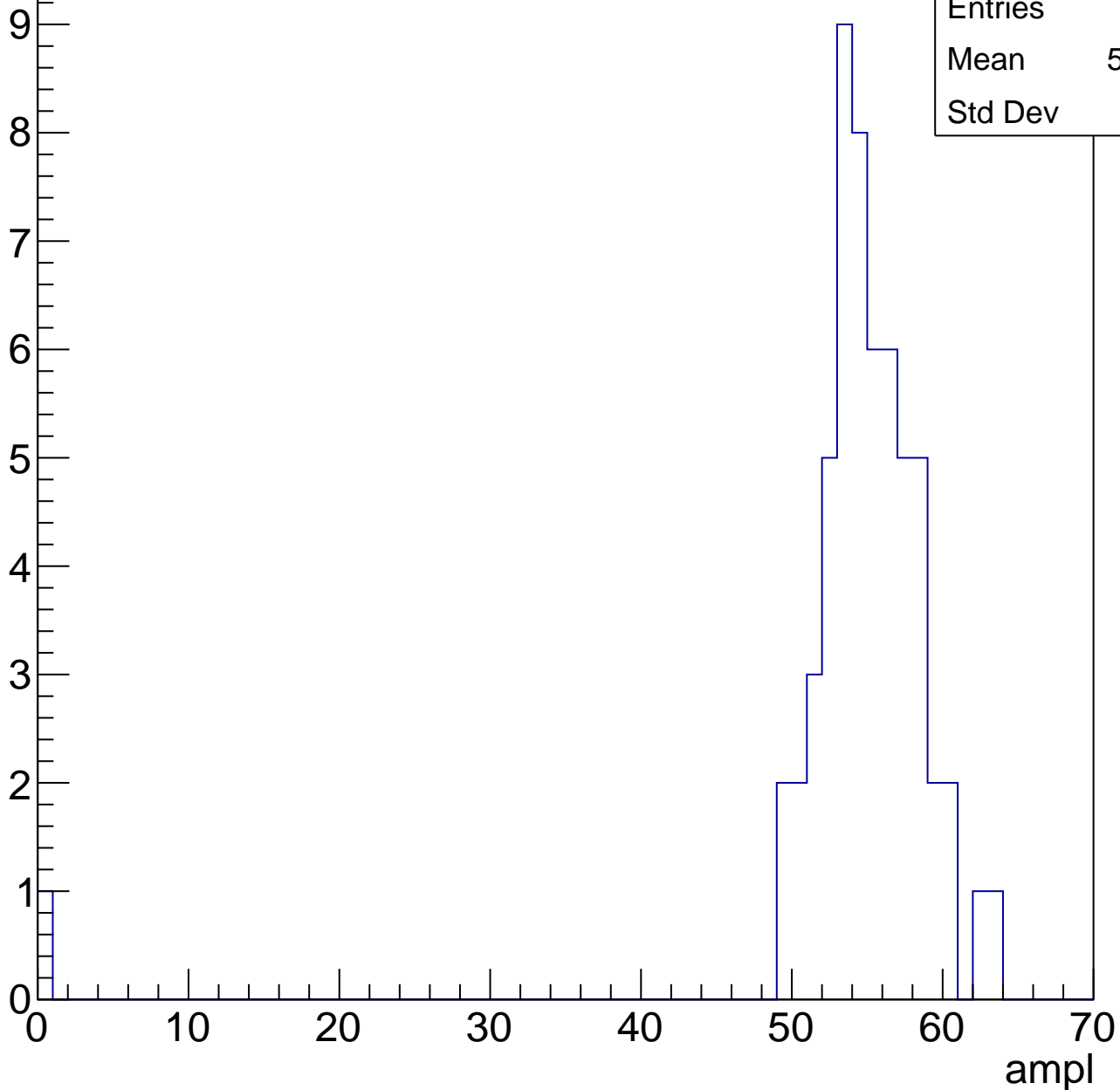


# B1L102S, U20-ch2, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	53.86
Std Dev	7.74



# B1L102S, U20-ch2, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

7  
6  
5  
4  
3  
2  
1  
0

Entries	44
Mean	59.8
Std Dev	2.211

ampl

0 10 20 30 40 50 60 70

0

1

2

3

4

5

6

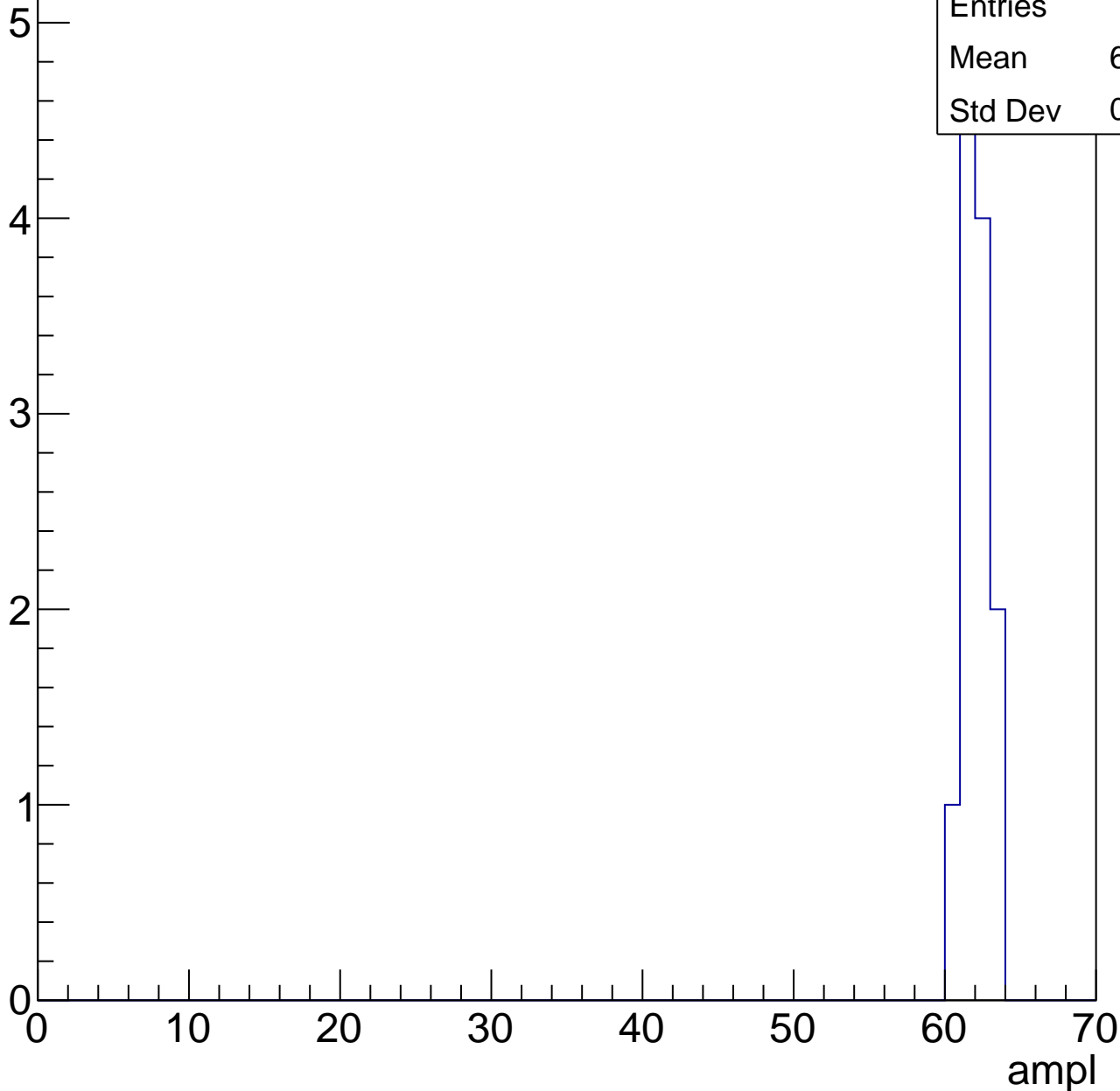
7

# B1L102S, U20-ch2, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	12
Mean	61.58
Std Dev	0.862





# B1L102S, U20-ch2, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	9.5
Std Dev	9.5

# B1L102S, U20-ch3, adc0

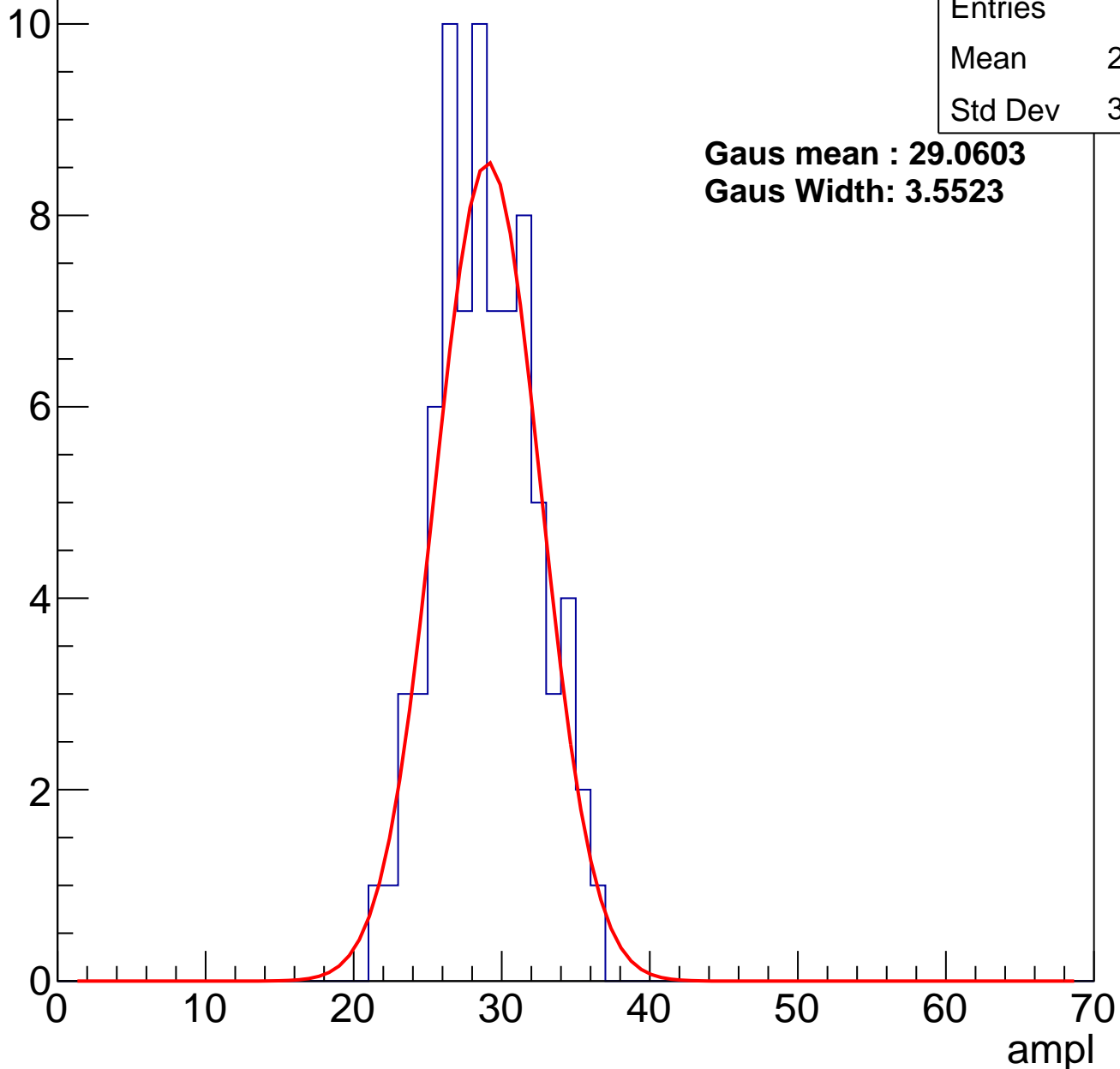
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	78
Mean	28.53
Std Dev	3.312

**Gaus mean : 29.0603**

**Gaus Width: 3.5523**

Entry



# B1L102S, U20-ch3, adc1

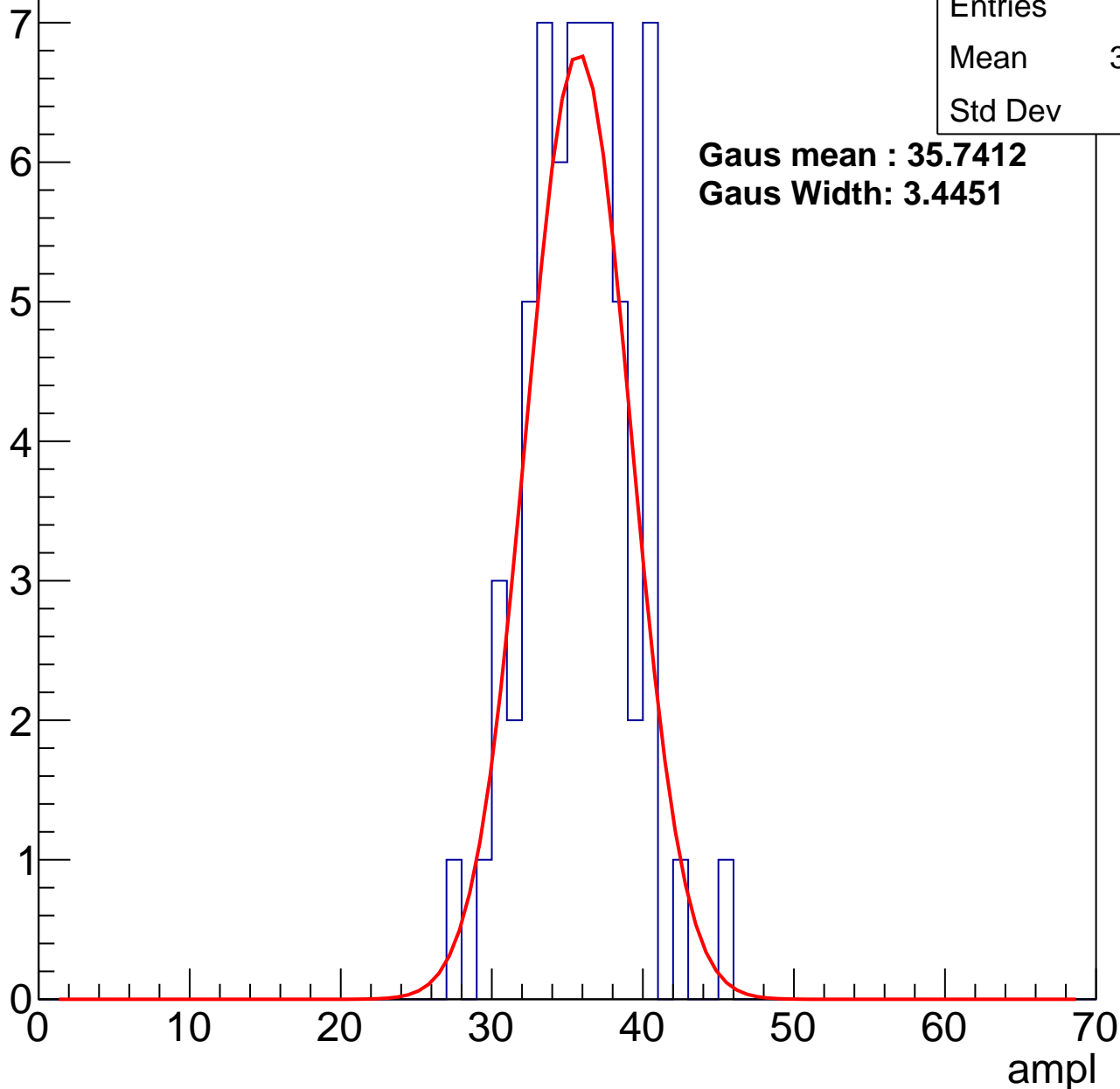
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	35.39
Std Dev	3.39

**Gaus mean : 35.7412**

**Gaus Width: 3.4451**



# B1L102S, U20-ch3, adc2

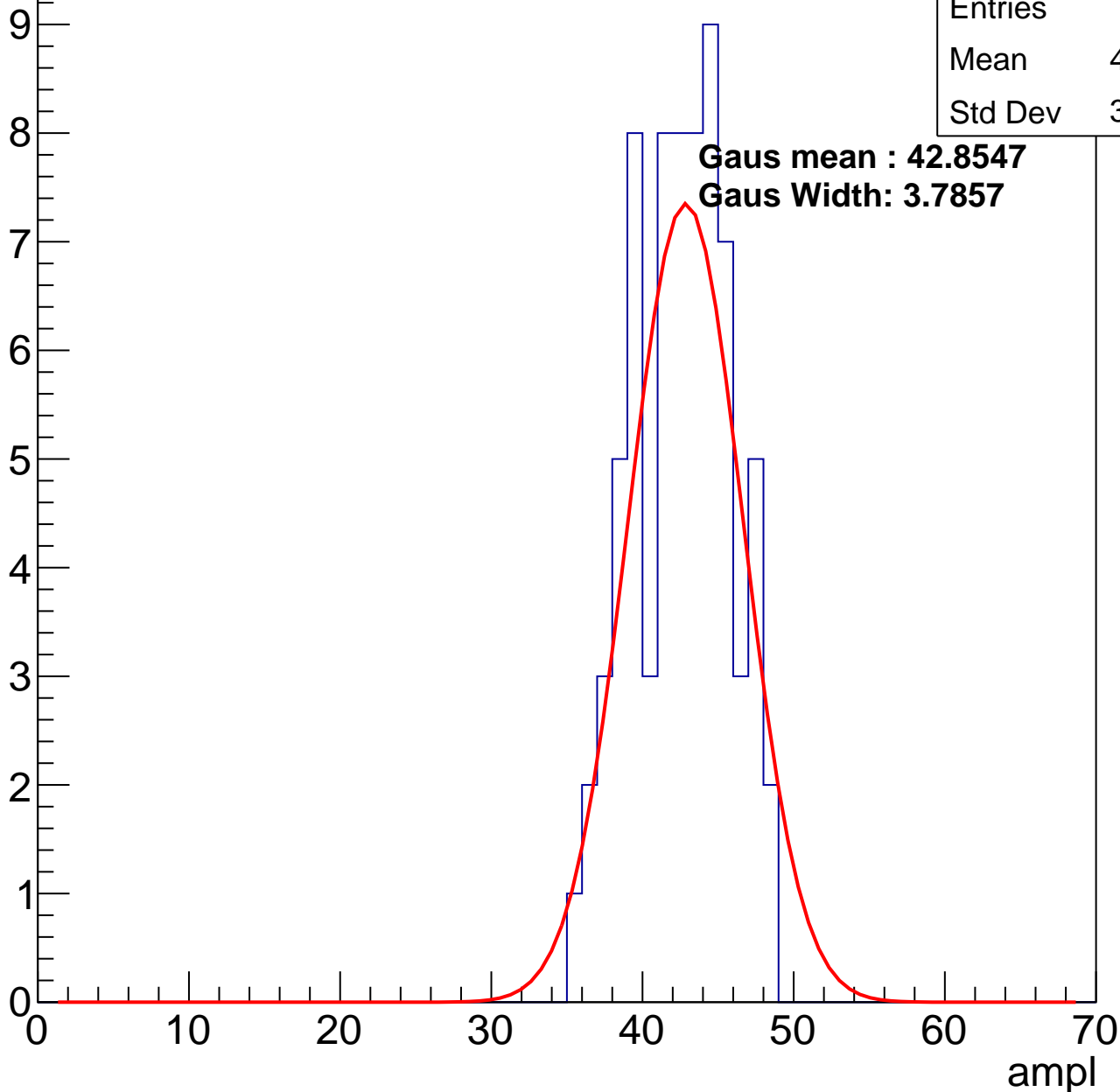
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	42.06
Std Dev	3.162

**Gaus mean : 42.8547**

**Gaus Width: 3.7857**



# B1L102S, U20-ch3, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

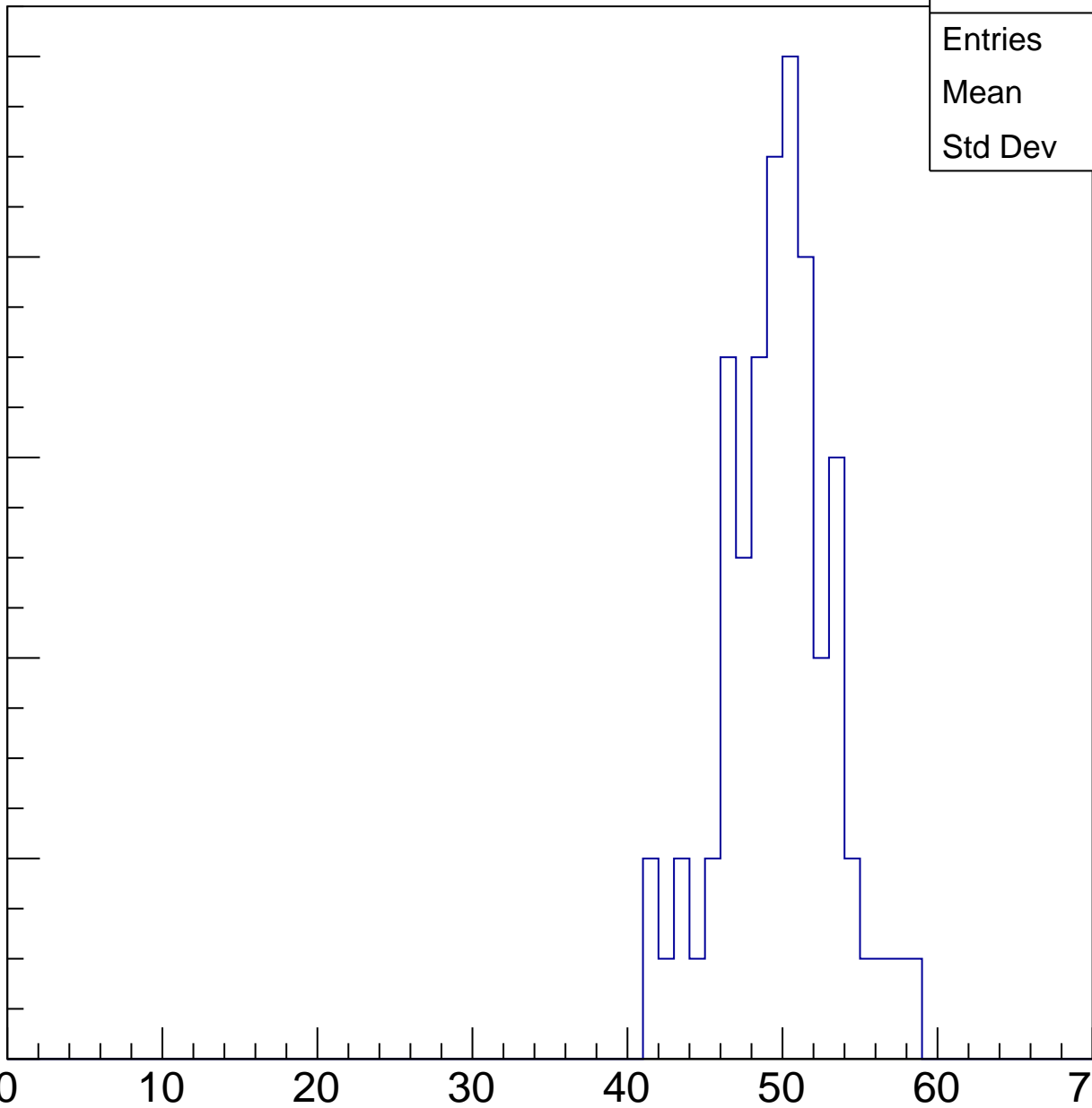
Entries	70
Mean	49.23
Std Dev	3.477

Entry

10  
8  
6  
4  
2  
0

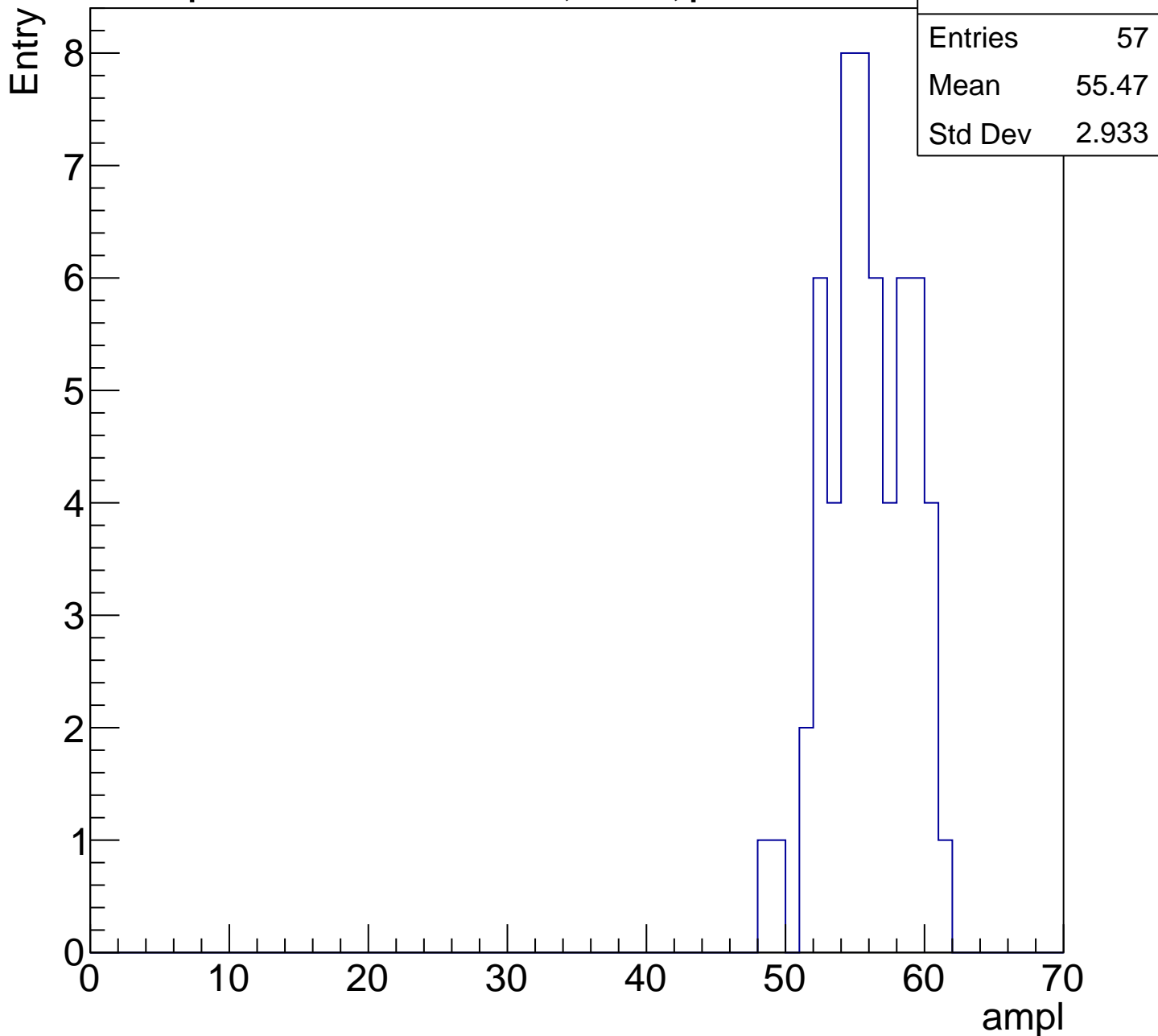
0 10 20 30 40 50 60 70

ampl



# B1L102S, U20-ch3, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

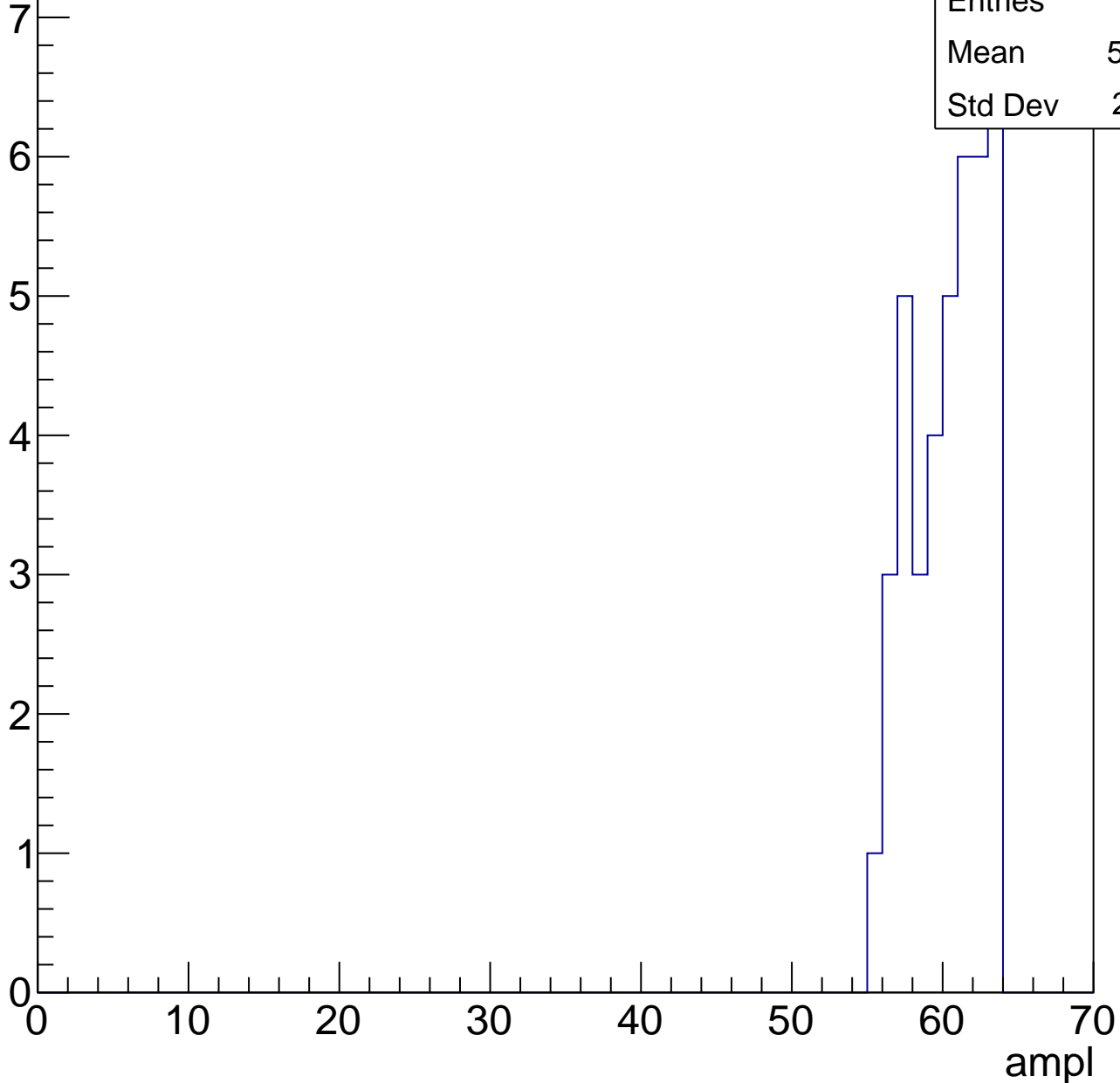


# B1L102S, U20-ch3, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

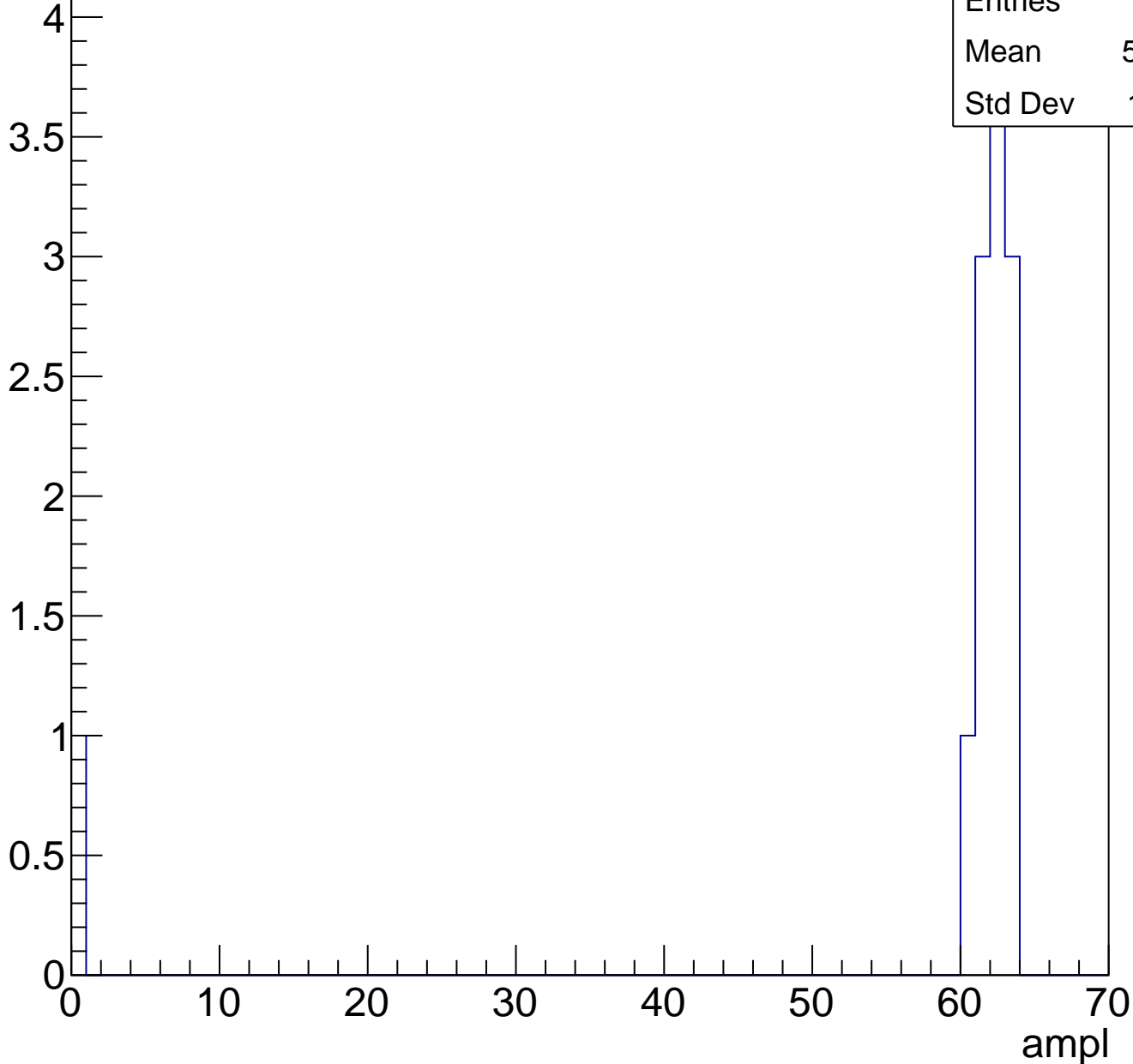
Entries	40
Mean	59.92
Std Dev	2.381



# B1L102S, U20-ch3, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U20-ch3, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	10
Std Dev	10

# B1L102S, U20-ch4, adc0

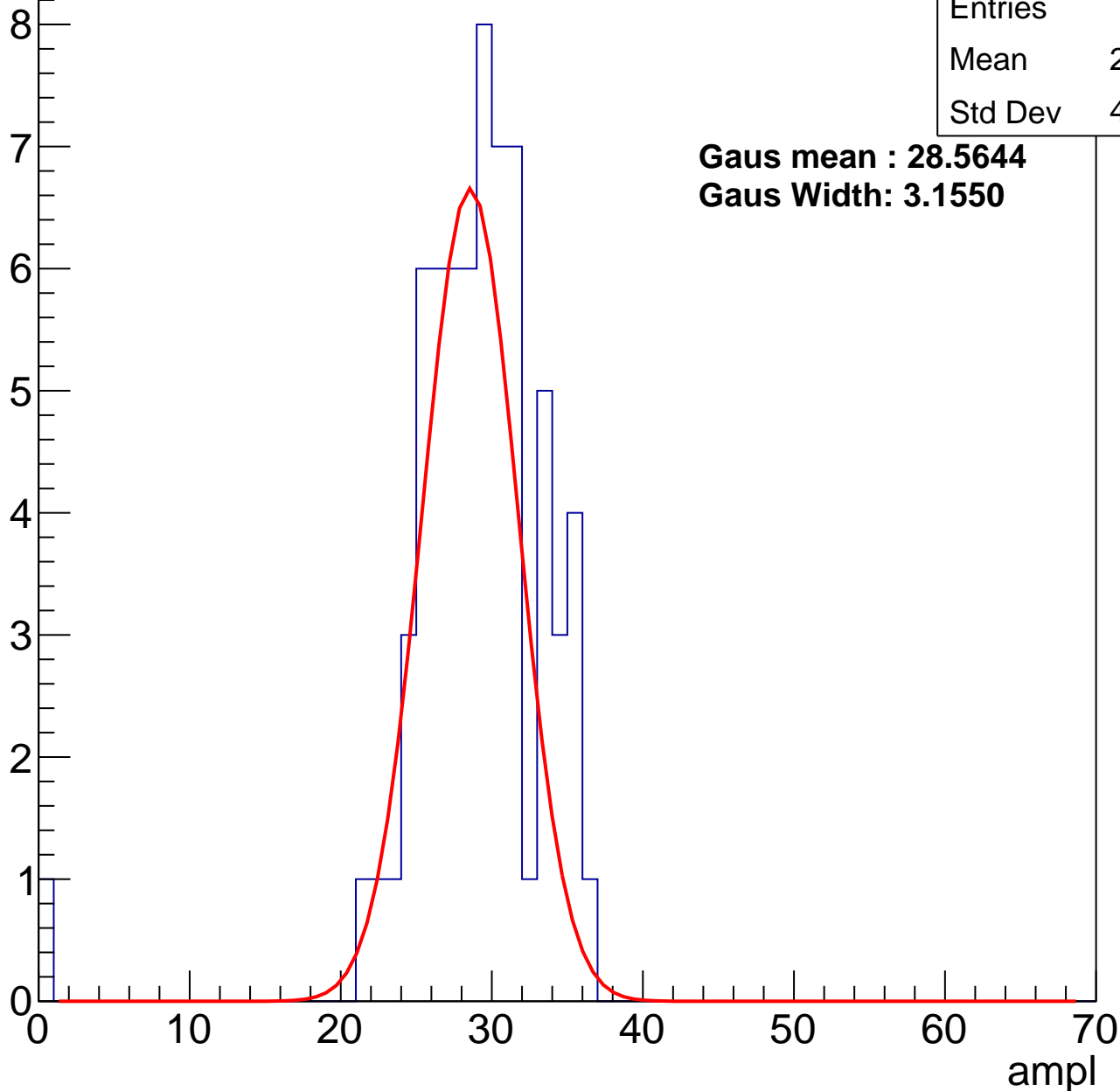
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	28.48
Std Dev	4.915

**Gaus mean : 28.5644**

**Gaus Width: 3.1550**



# B1L102S, U20-ch4, adc1

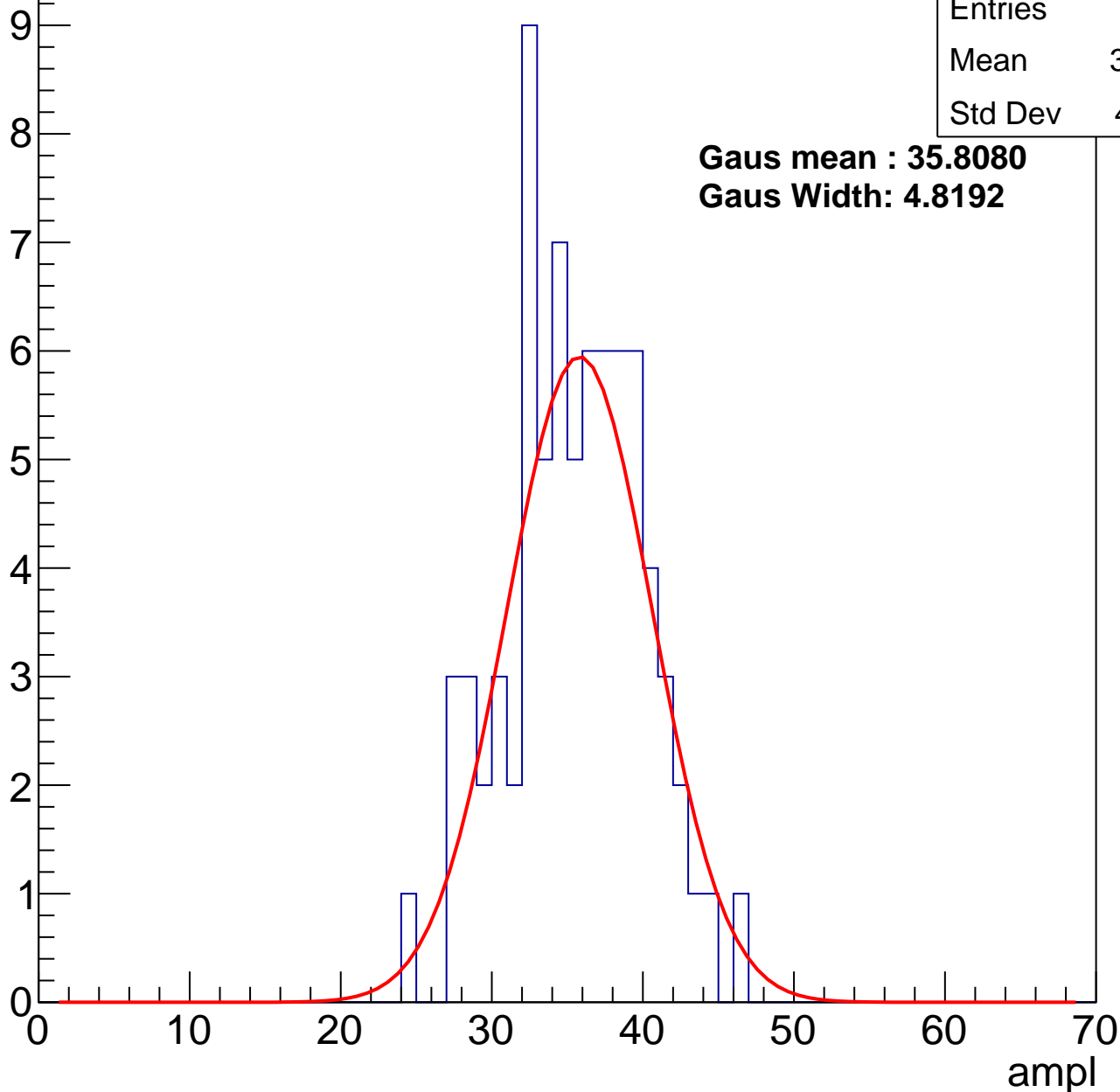
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	35.07
Std Dev	4.441

**Gaus mean : 35.8080**

**Gaus Width: 4.8192**



# B1L102S, U20-ch4, adc2

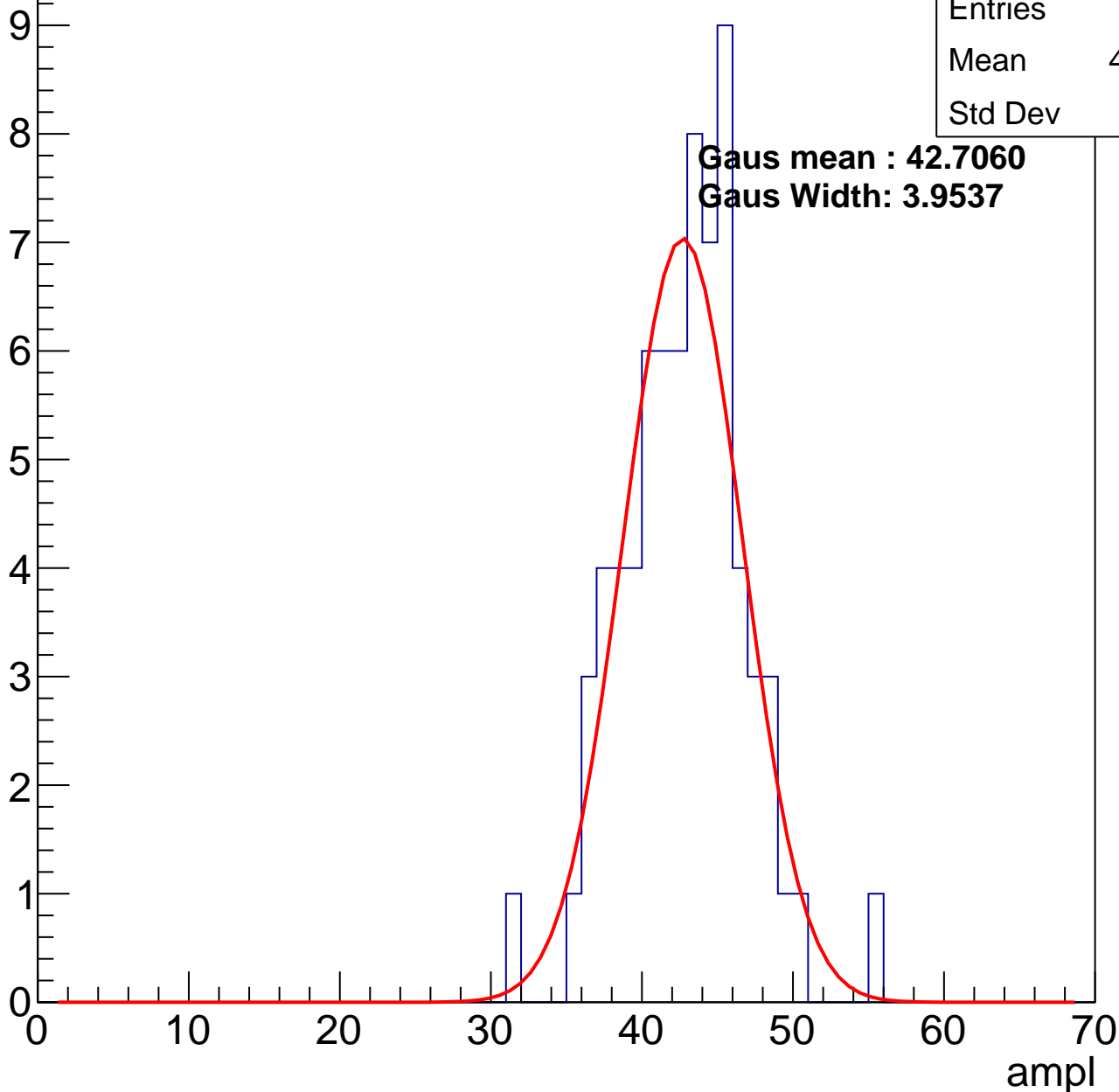
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	42.33
Std Dev	3.99

**Gaus mean : 42.7060**

**Gaus Width: 3.9537**

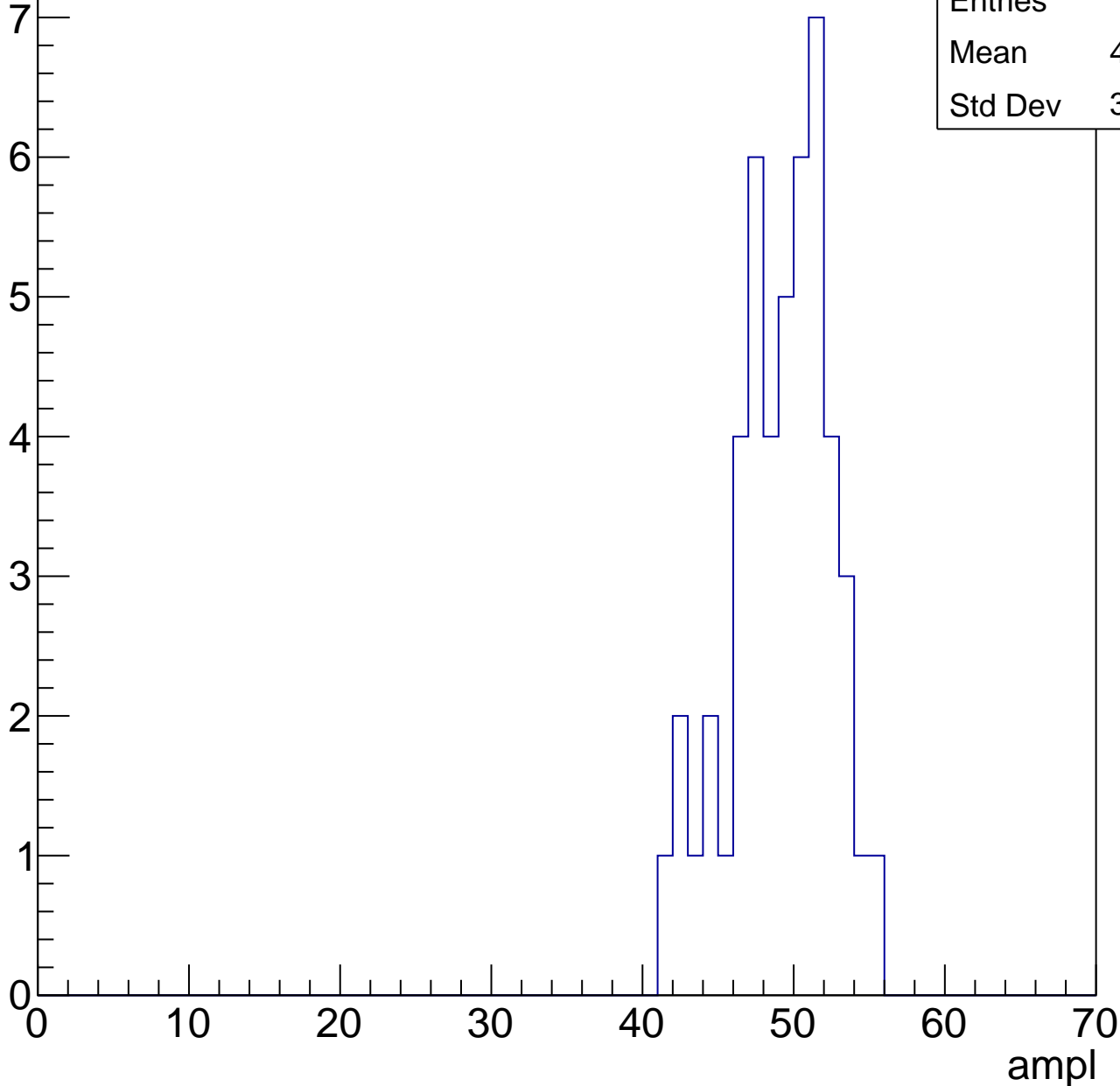


# B1L102S, U20-ch4, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

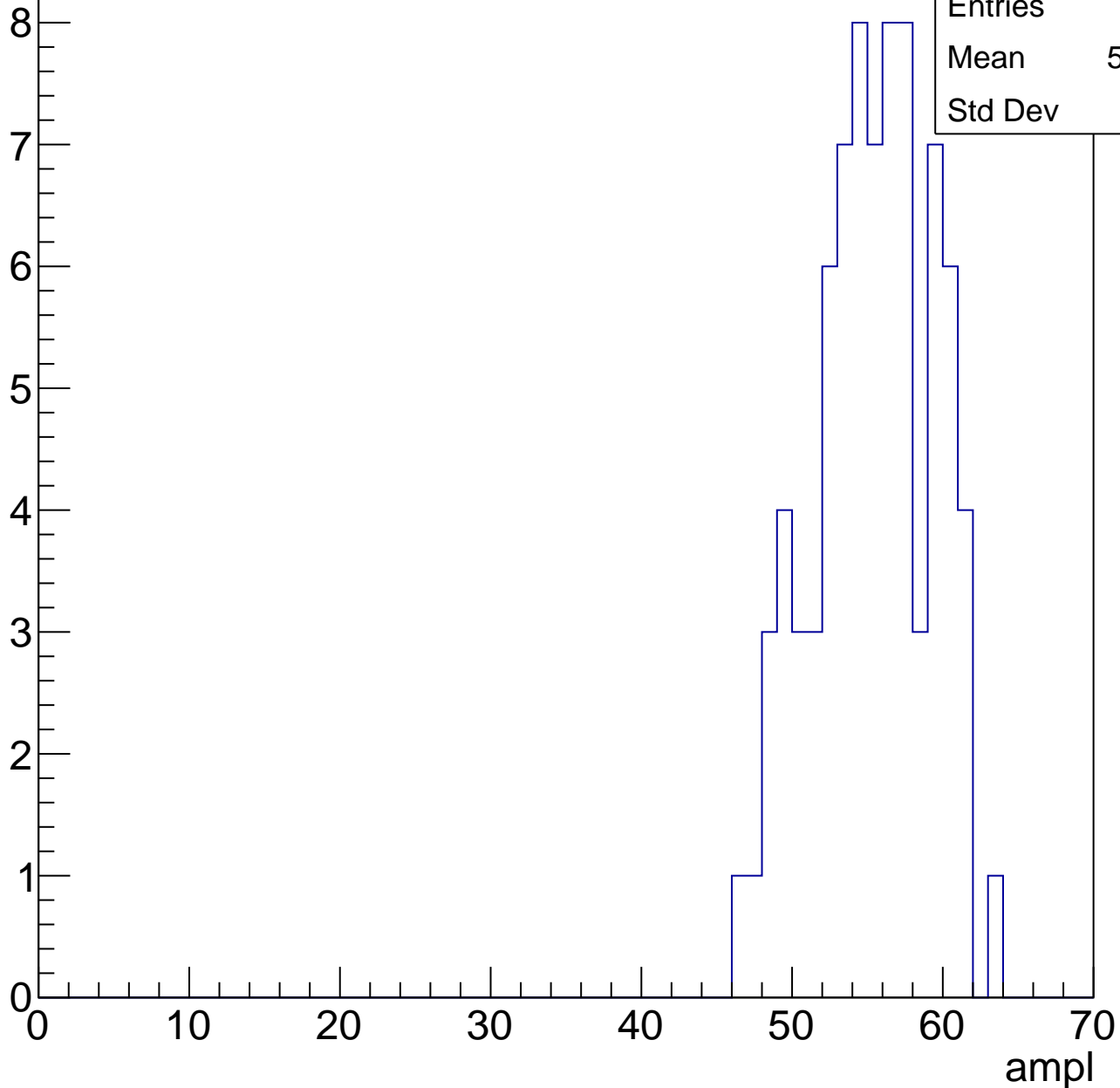
Entries	48
Mean	48.69
Std Dev	3.235



# B1L102S, U20-ch4, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

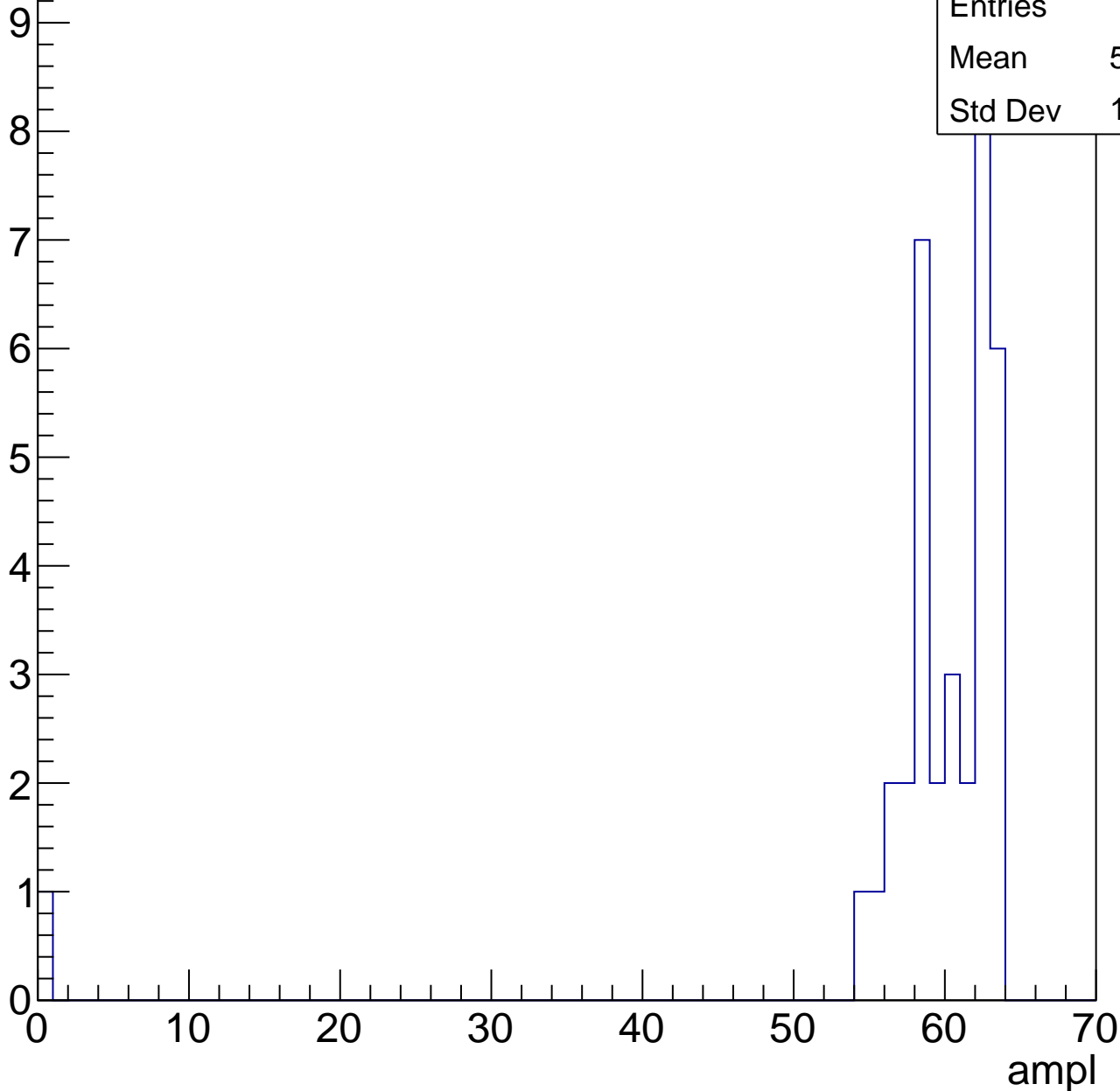


# B1L102S, U20-ch4, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

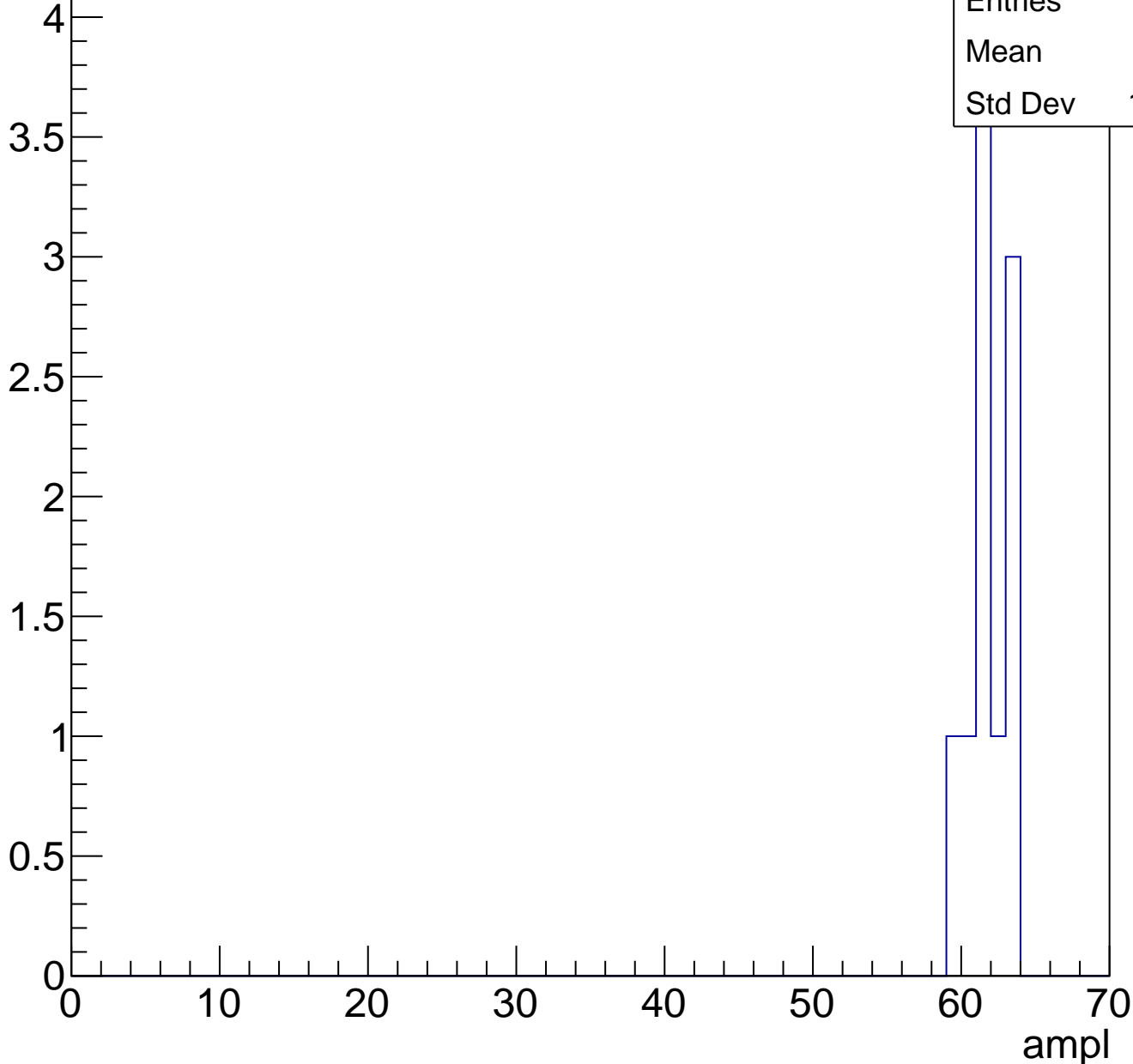
Entries	36
Mean	58.25
Std Dev	10.17



# B1L102S, U20-ch4, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	10
Mean	61.4
Std Dev	1.281



# B1L102S, U20-ch4, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U20-ch5, adc0

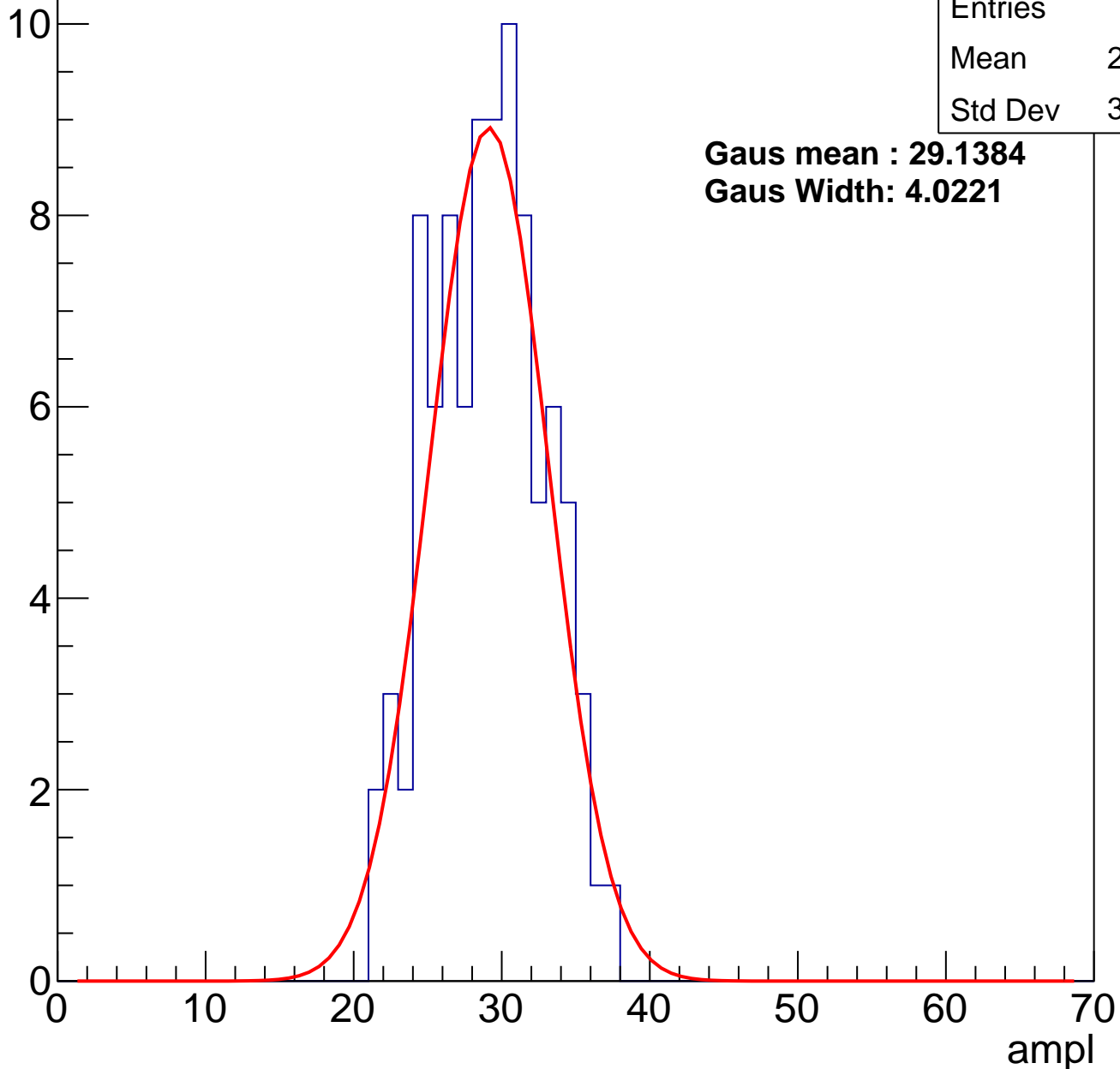
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	92
Mean	28.62
Std Dev	3.706

**Gaus mean : 29.1384**

**Gaus Width: 4.0221**

Entry



# B1L102S, U20-ch5, adc1

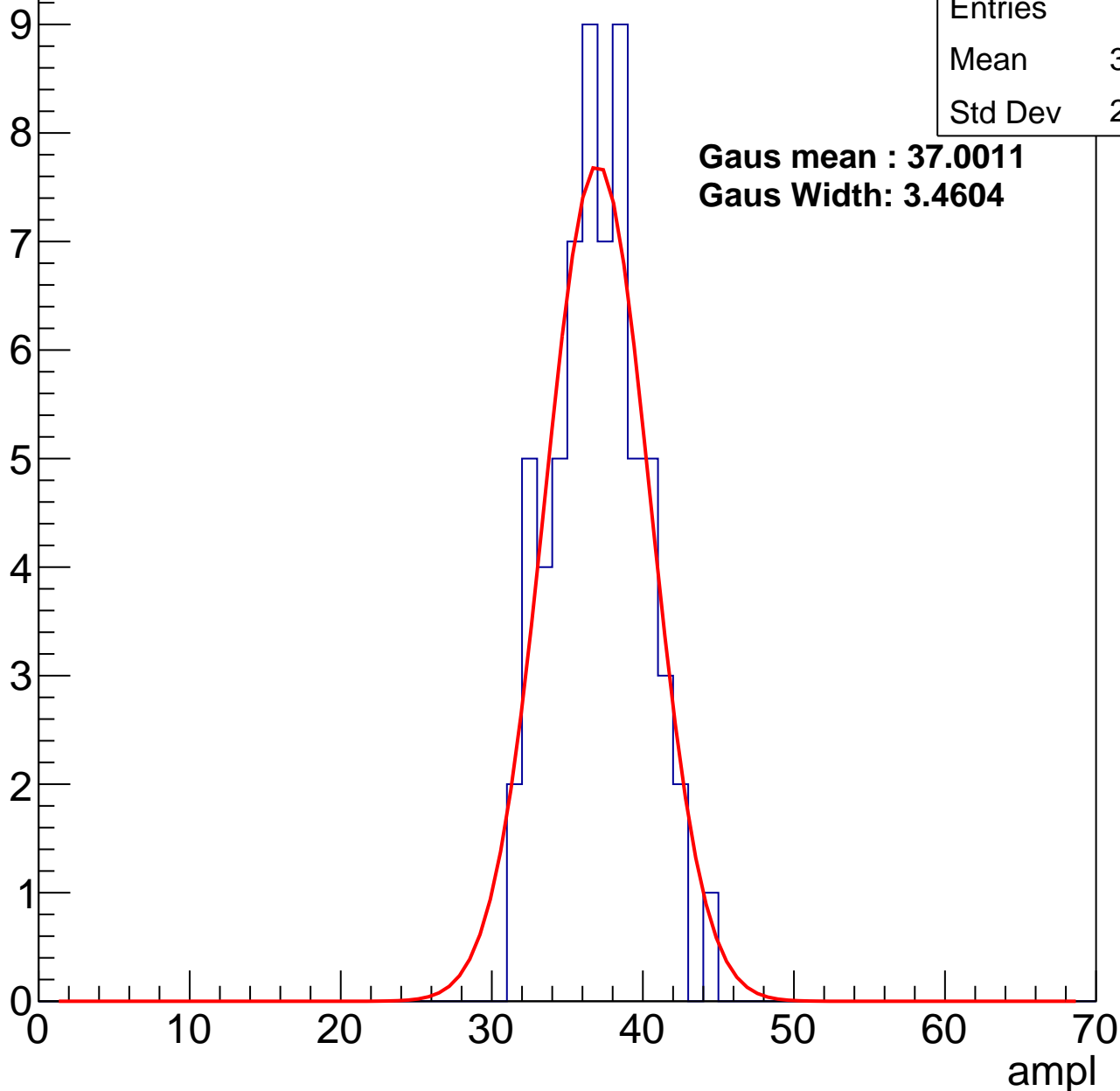
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	36.56
Std Dev	2.936

**Gaus mean : 37.0011**

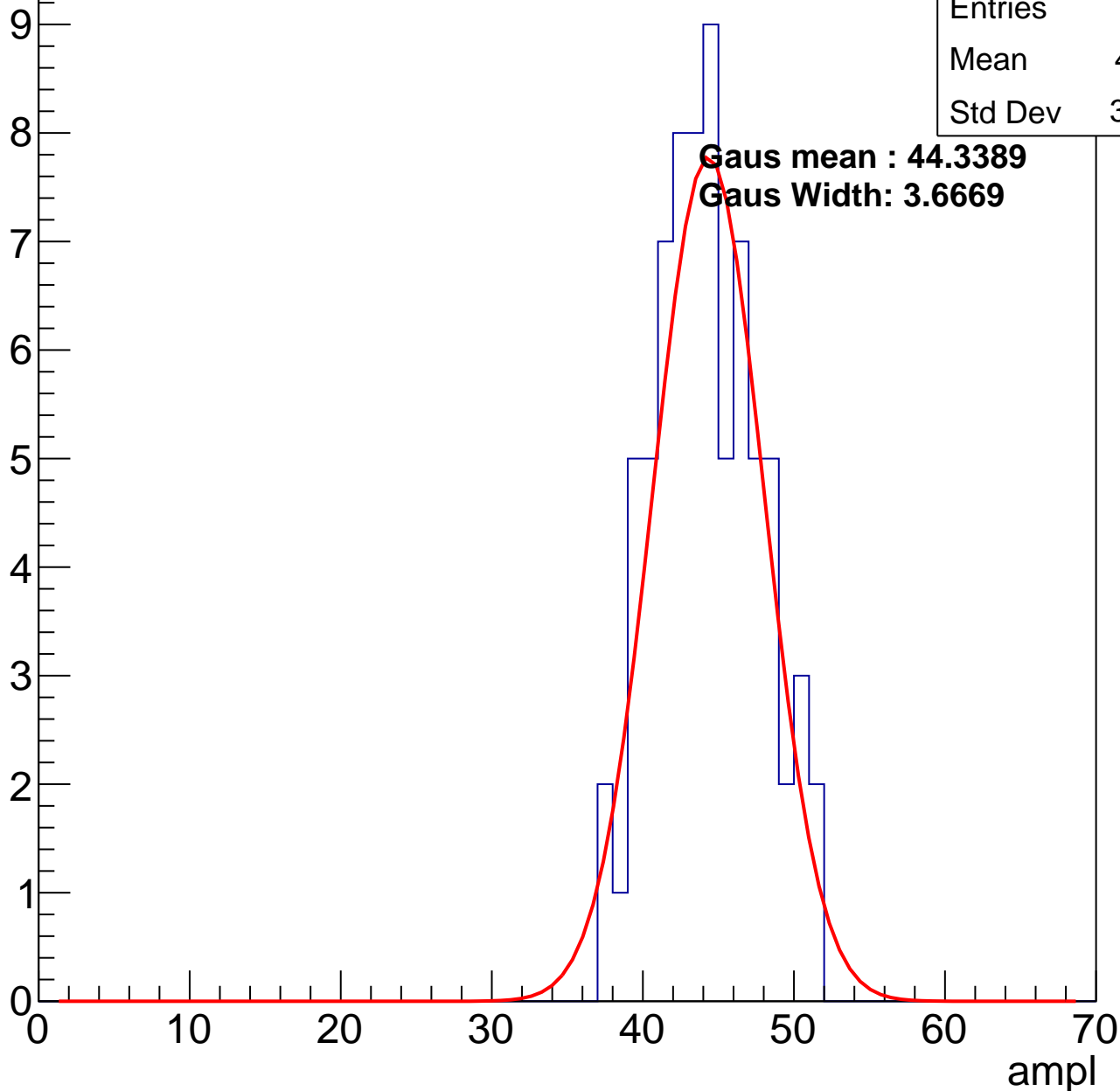
**Gaus Width: 3.4604**



# B1L102S, U20-ch5, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

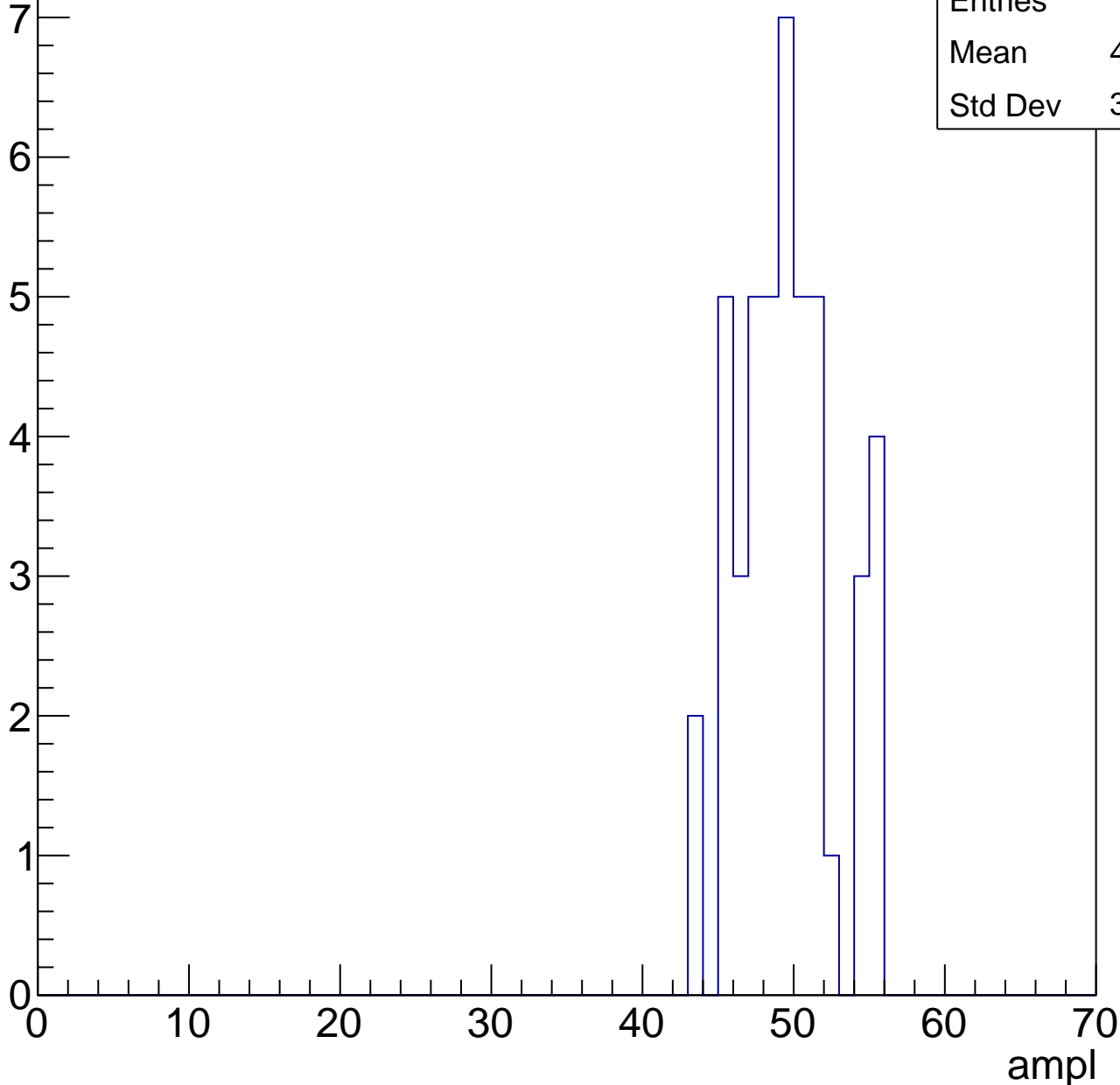


# B1L102S, U20-ch5, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	45
Mean	49.02
Std Dev	3.187

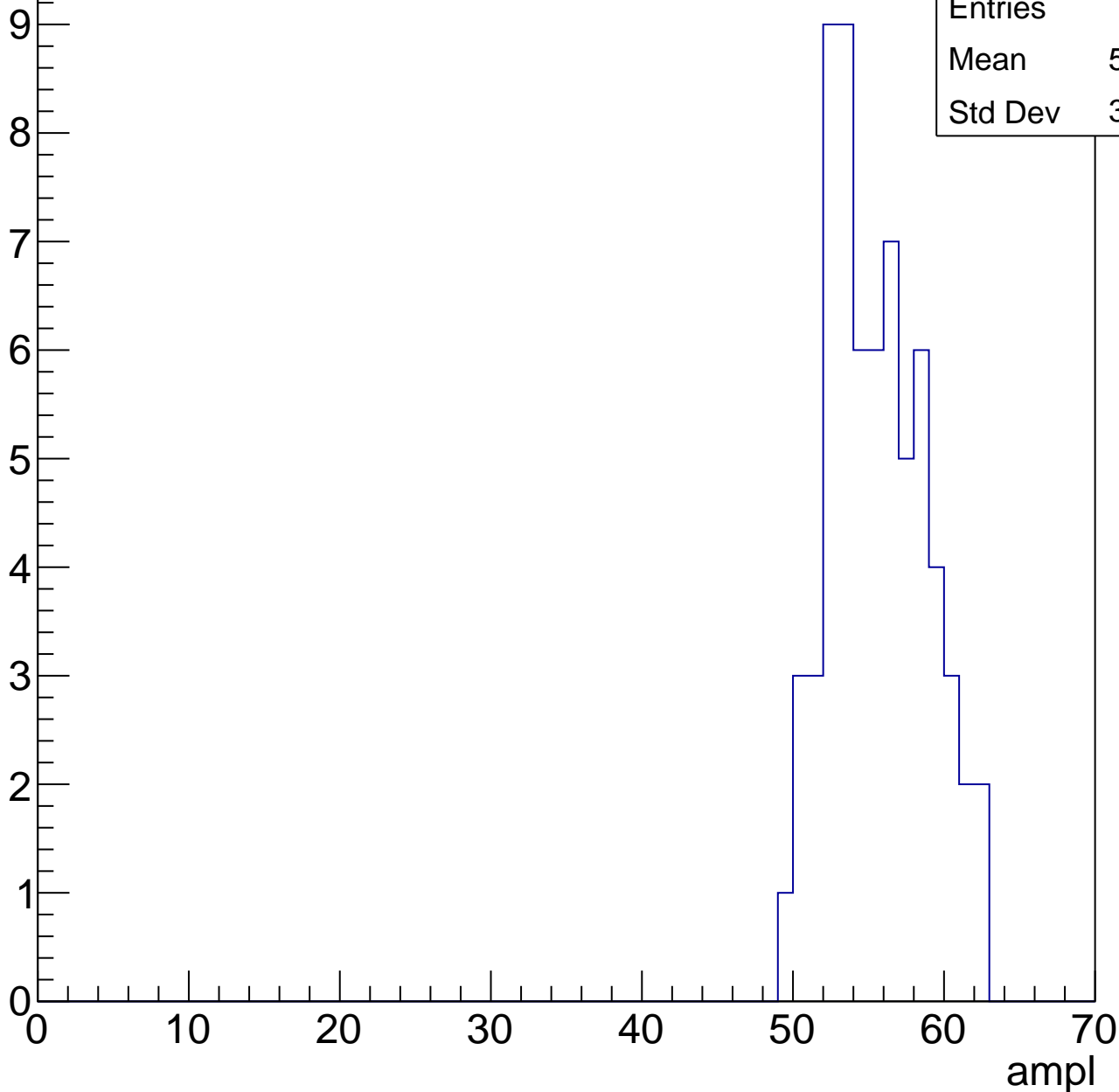


# B1L102S, U20-ch5, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	55.12
Std Dev	3.189

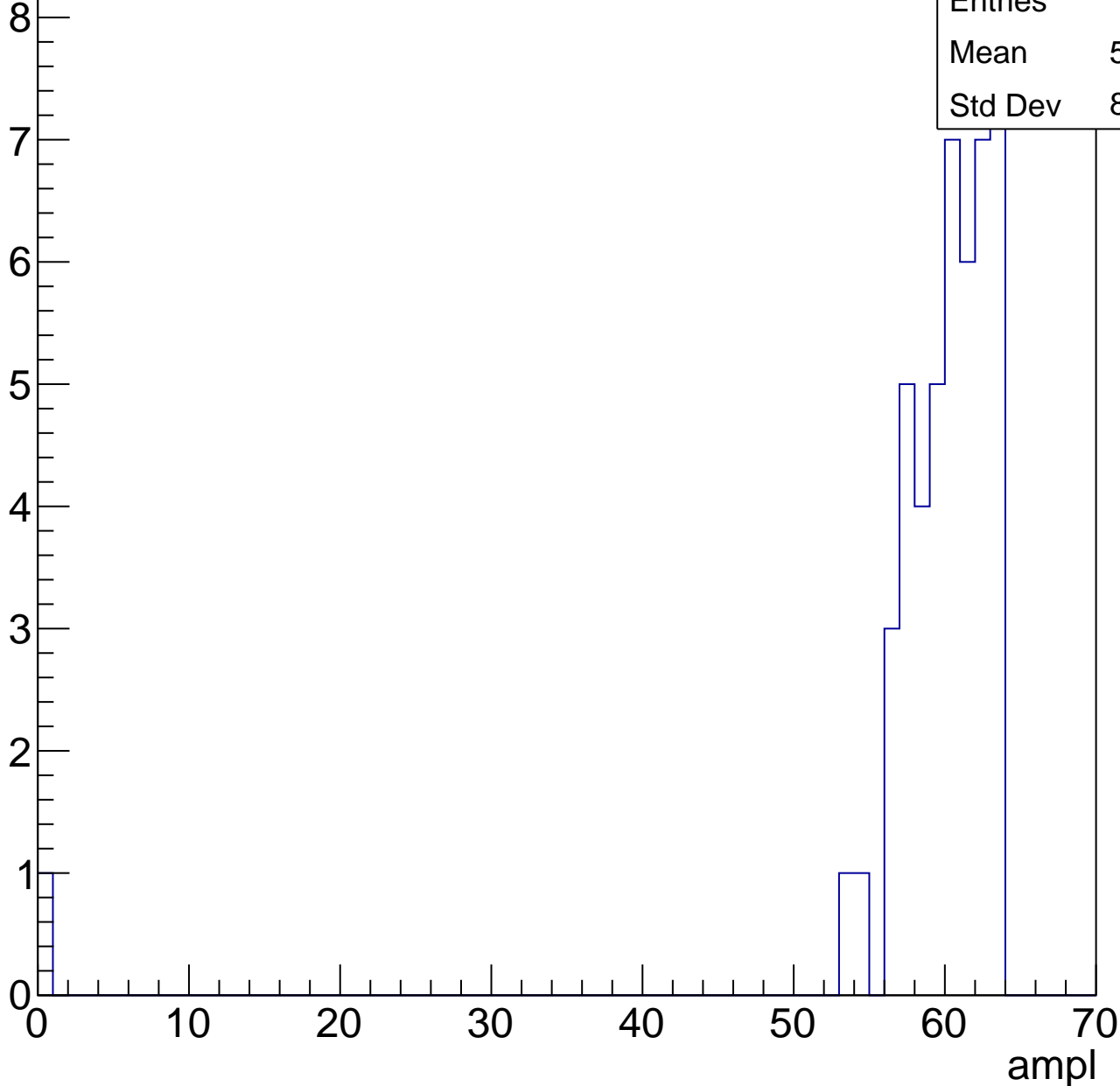


# B1L102S, U20-ch5, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	48
Mean	58.56
Std Dev	8.904



# B1L102S, U20-ch5, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

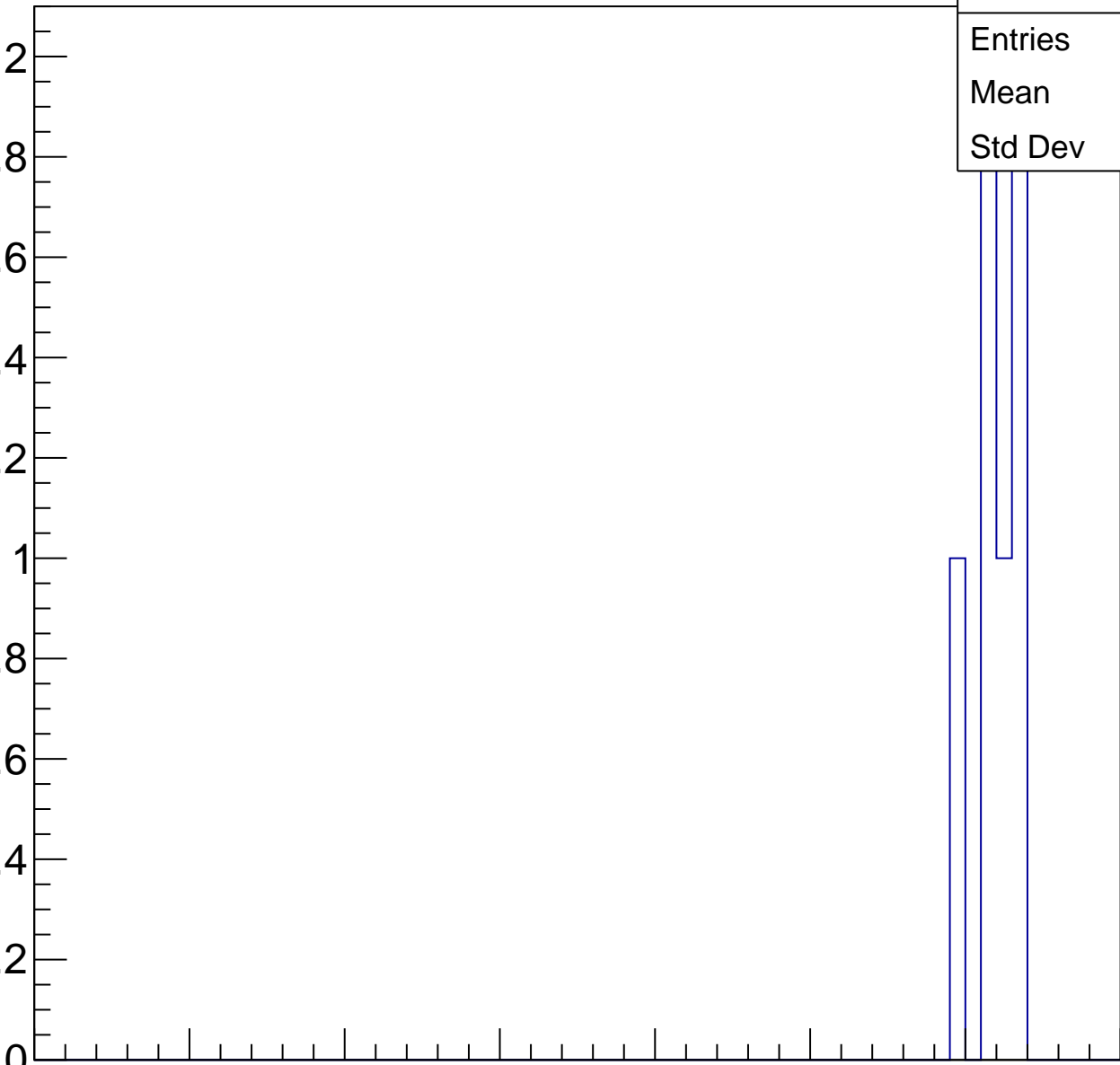
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	61.5
Std Dev	1.384

0 10 20 30 40 50 60 70

ampl





# B1L102S, U20-ch5, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch6, adc0

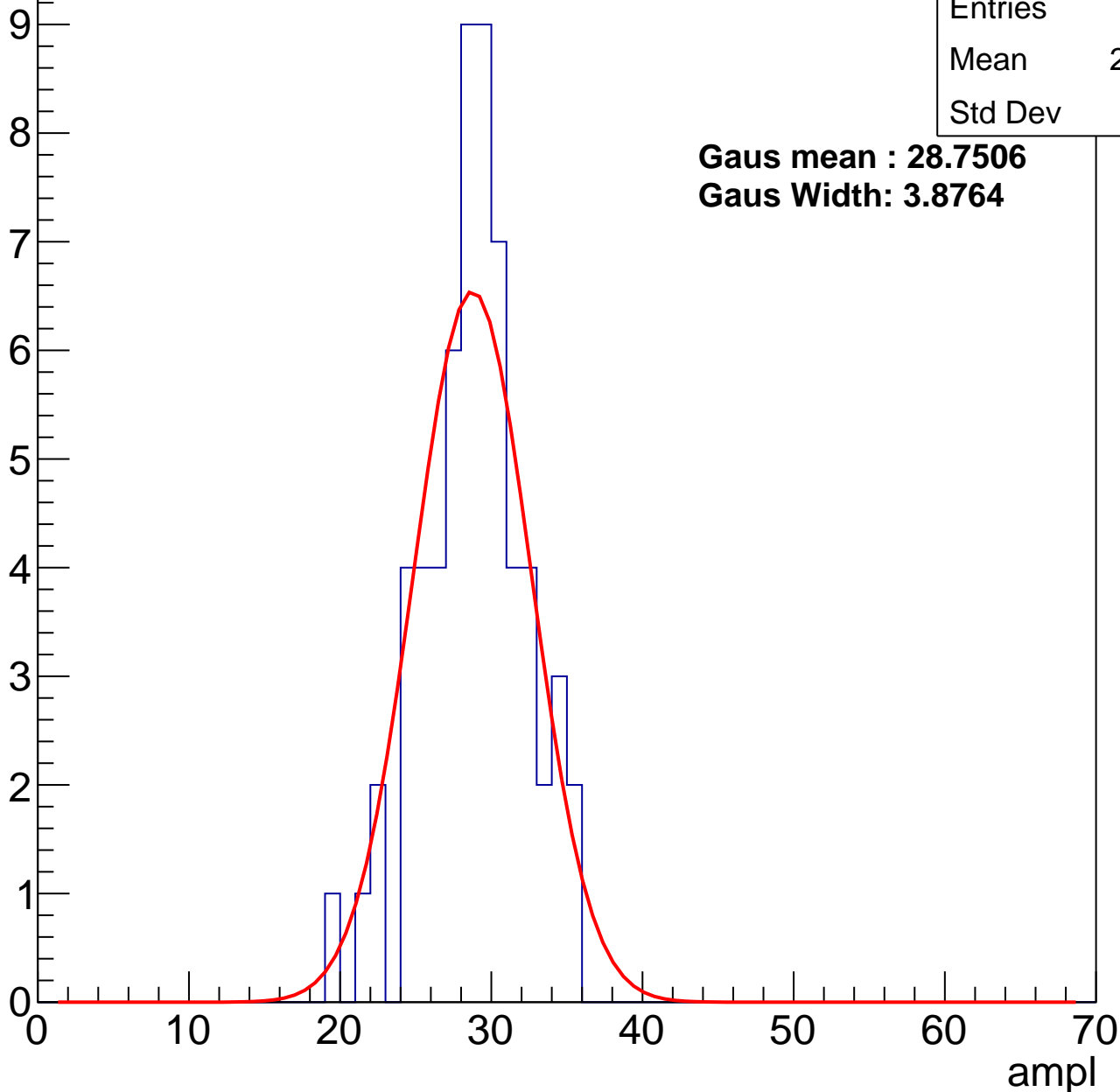
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	28.37
Std Dev	3.38

**Gaus mean : 28.7506**

**Gaus Width: 3.8764**



# B1L102S, U20-ch6, adc1

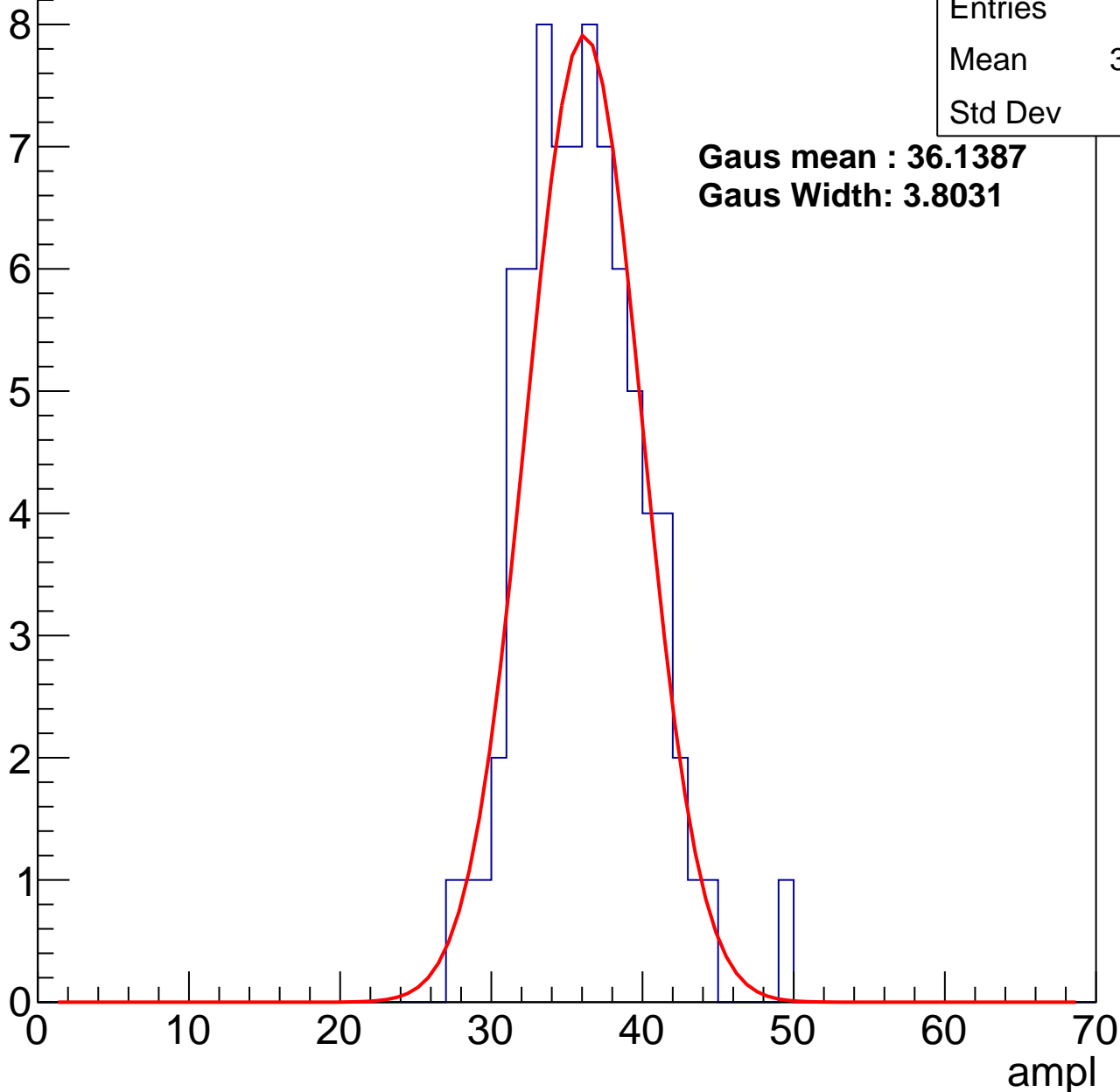
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	78
Mean	35.68
Std Dev	3.93

**Gaus mean : 36.1387**

**Gaus Width: 3.8031**



# B1L102S, U20-ch6, adc2

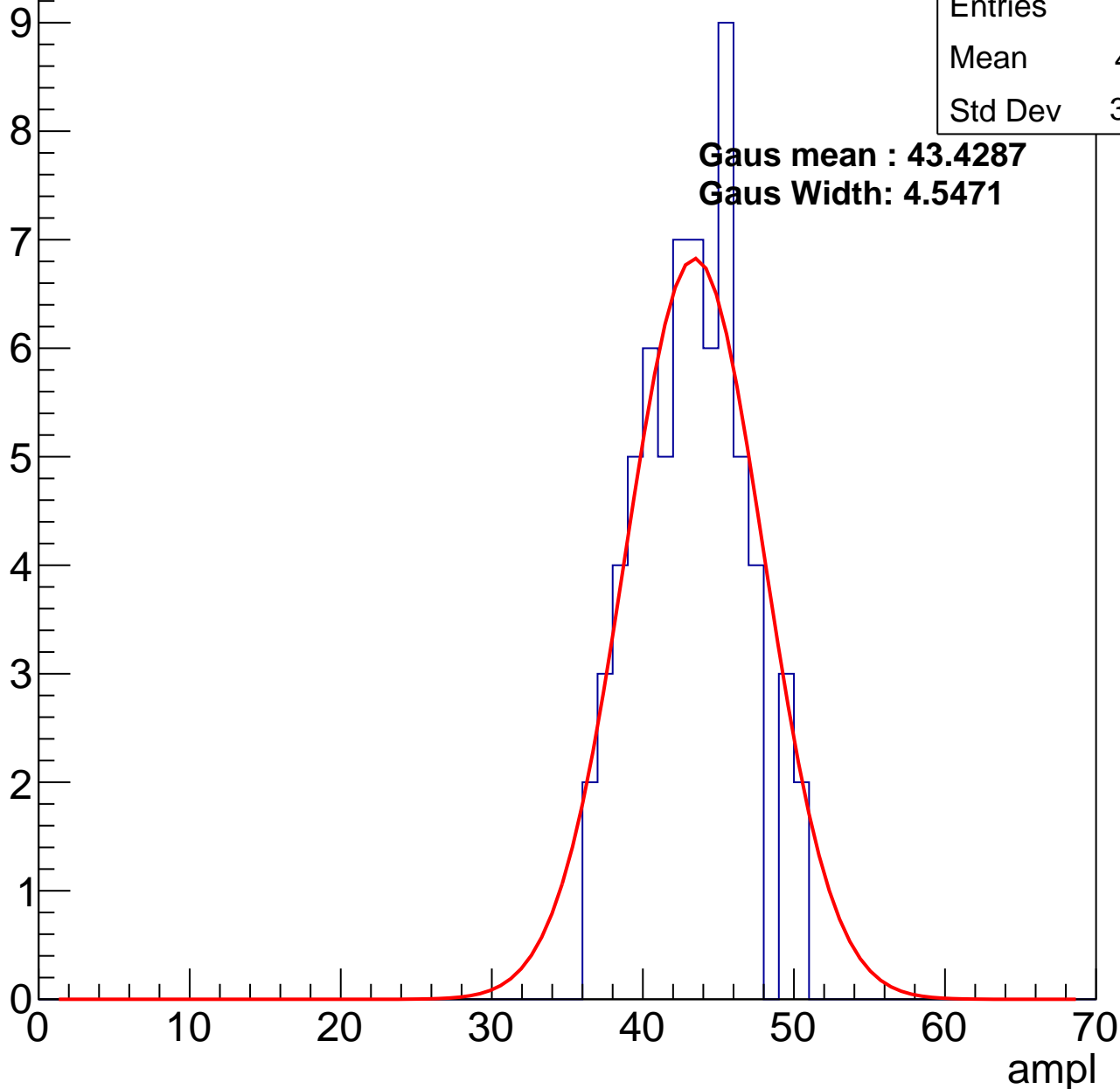
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	42.71
Std Dev	3.469

**Gaus mean : 43.4287**

**Gaus Width: 4.5471**

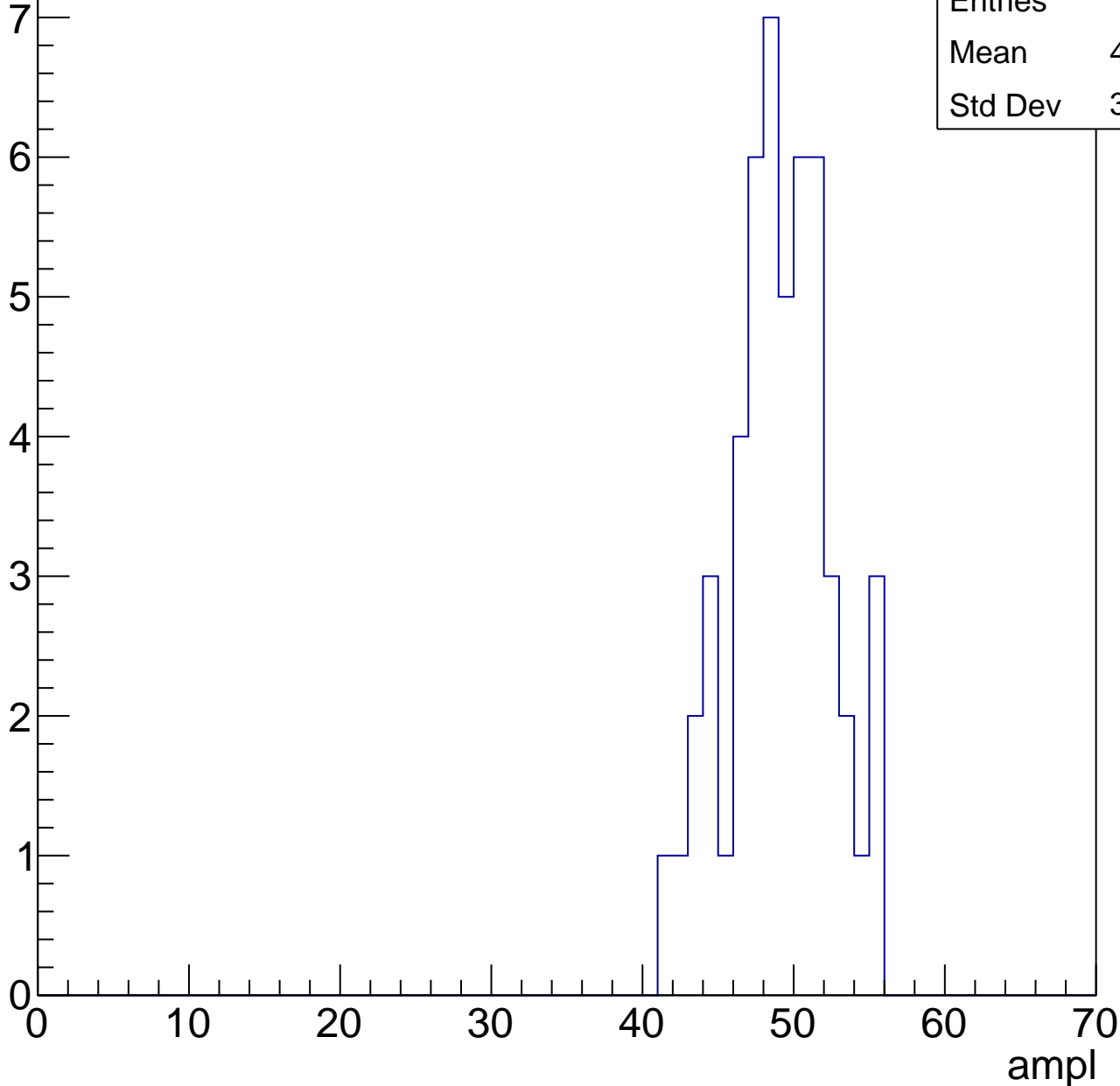


# B1L102S, U20-ch6, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

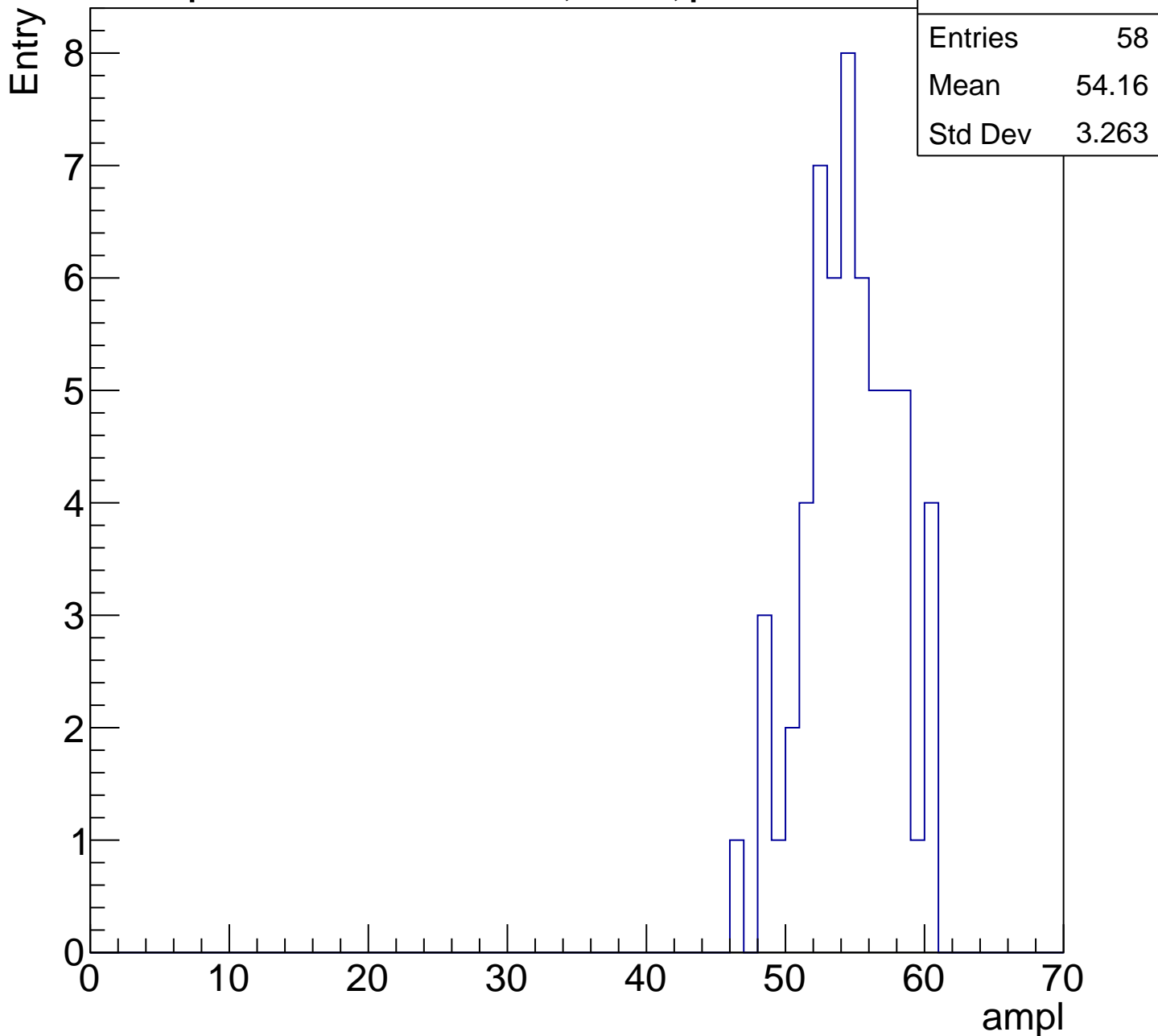
Entry

Entries	51
Mean	48.63
Std Dev	3.308



# B1L102S, U20-ch6, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

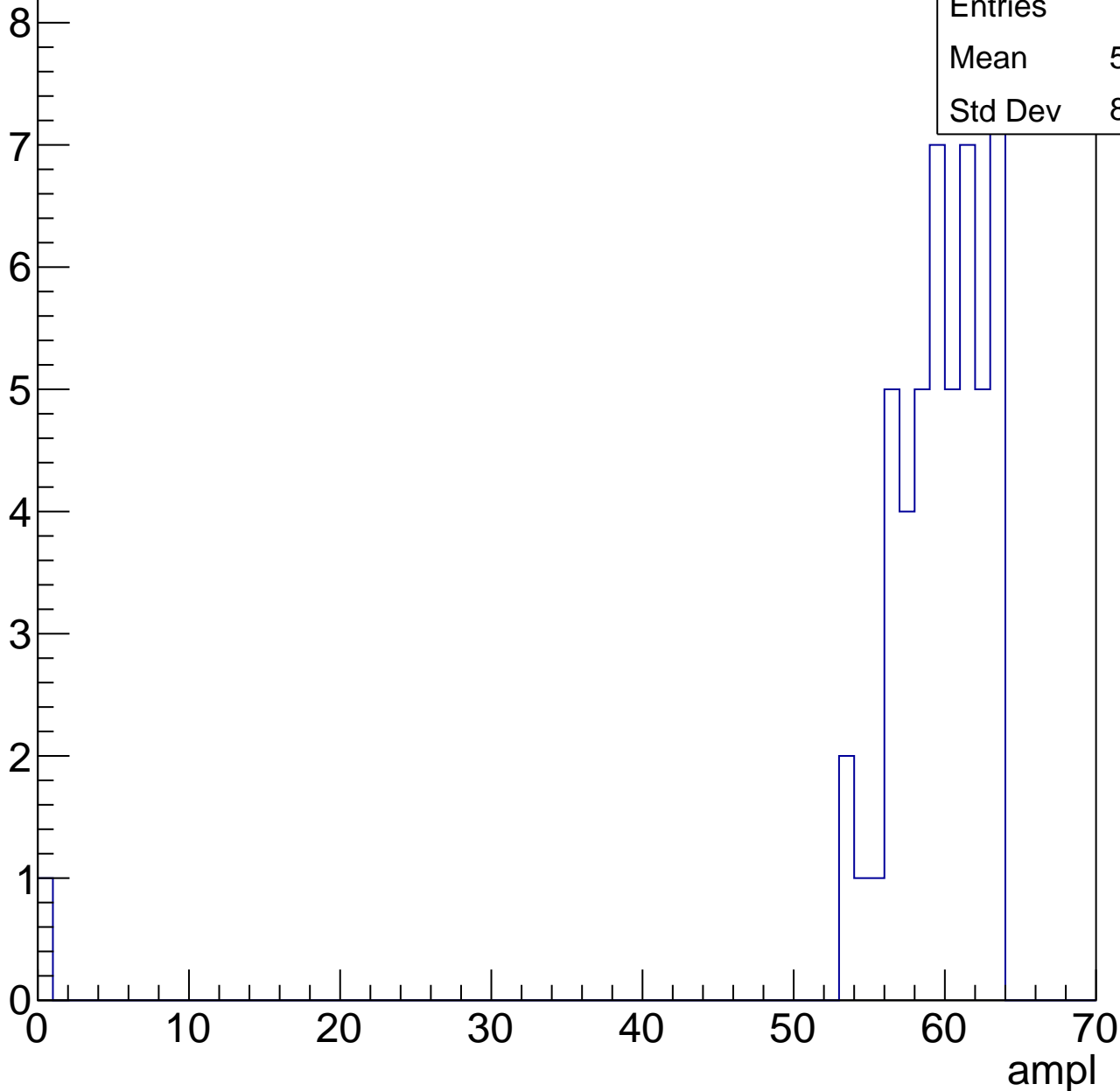


# B1L102S, U20-ch6, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	58.18
Std Dev	8.668

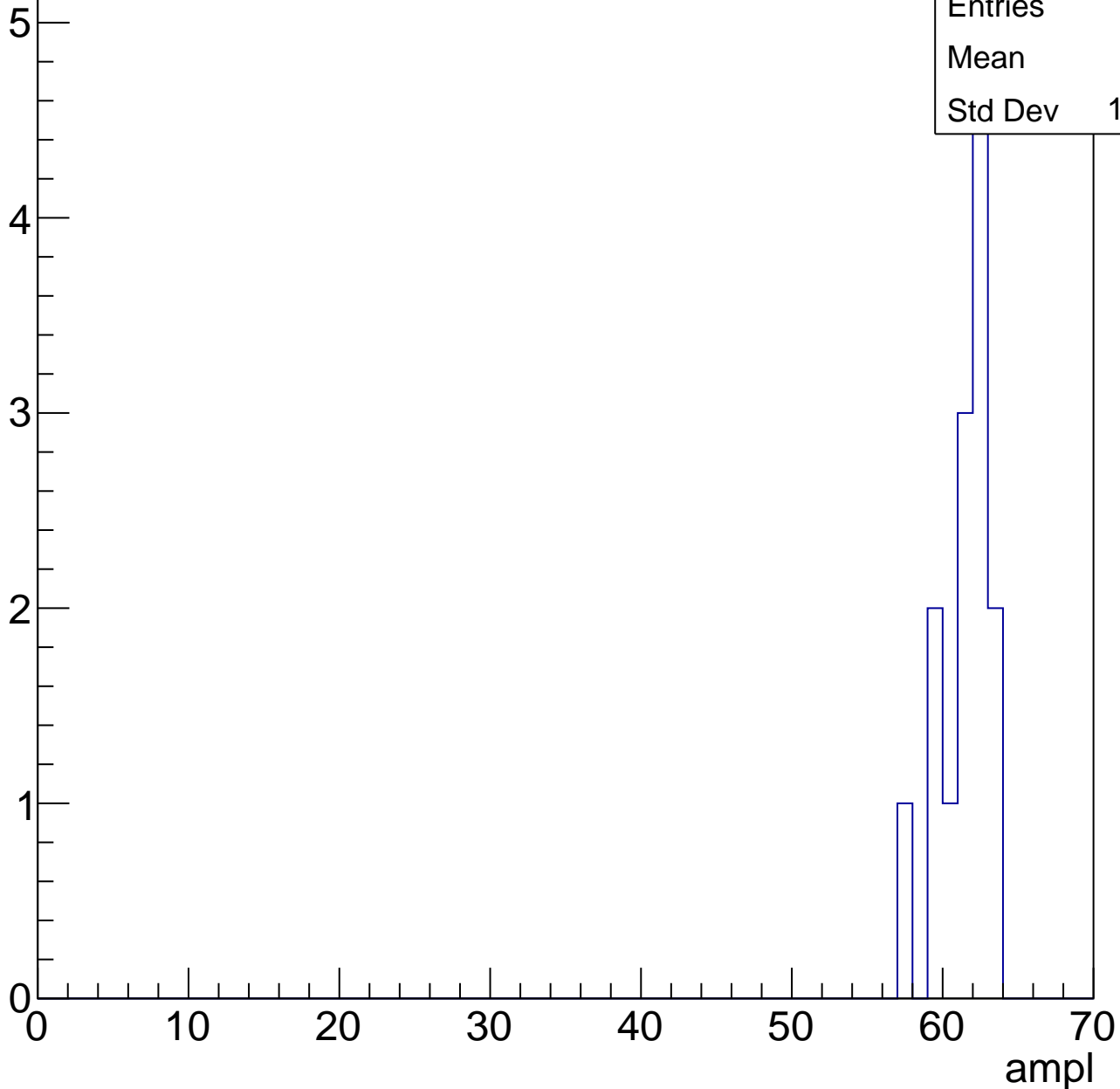


# B1L102S, U20-ch6, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	14
Mean	61
Std Dev	1.648





# B1L102S, U20-ch6, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U20-ch7, adc0

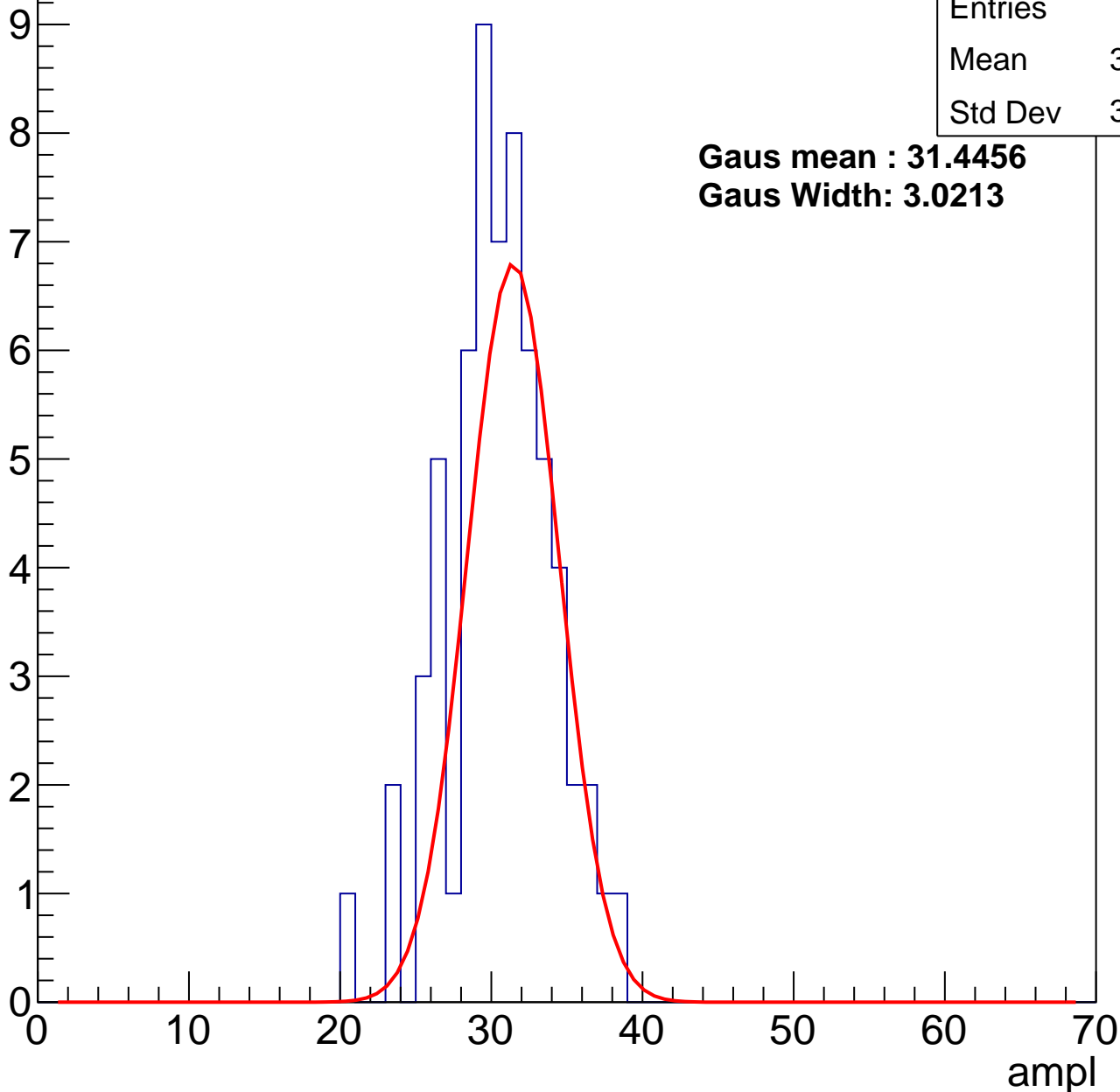
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	30.08
Std Dev	3.497

**Gaus mean : 31.4456**

**Gaus Width: 3.0213**



# B1L102S, U20-ch7, adc1

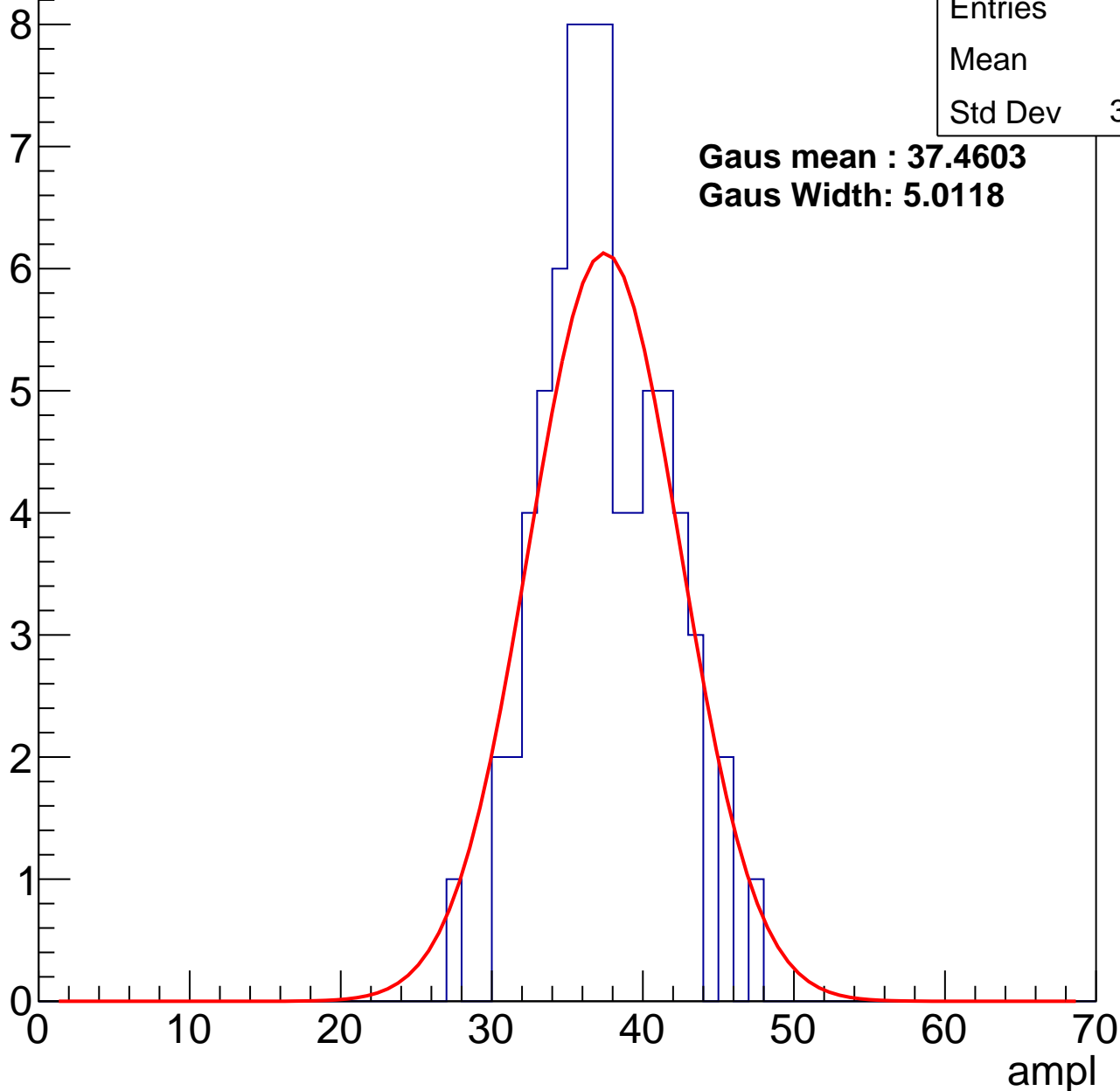
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	36.9
Std Dev	3.952

**Gaus mean : 37.4603**

**Gaus Width: 5.0118**

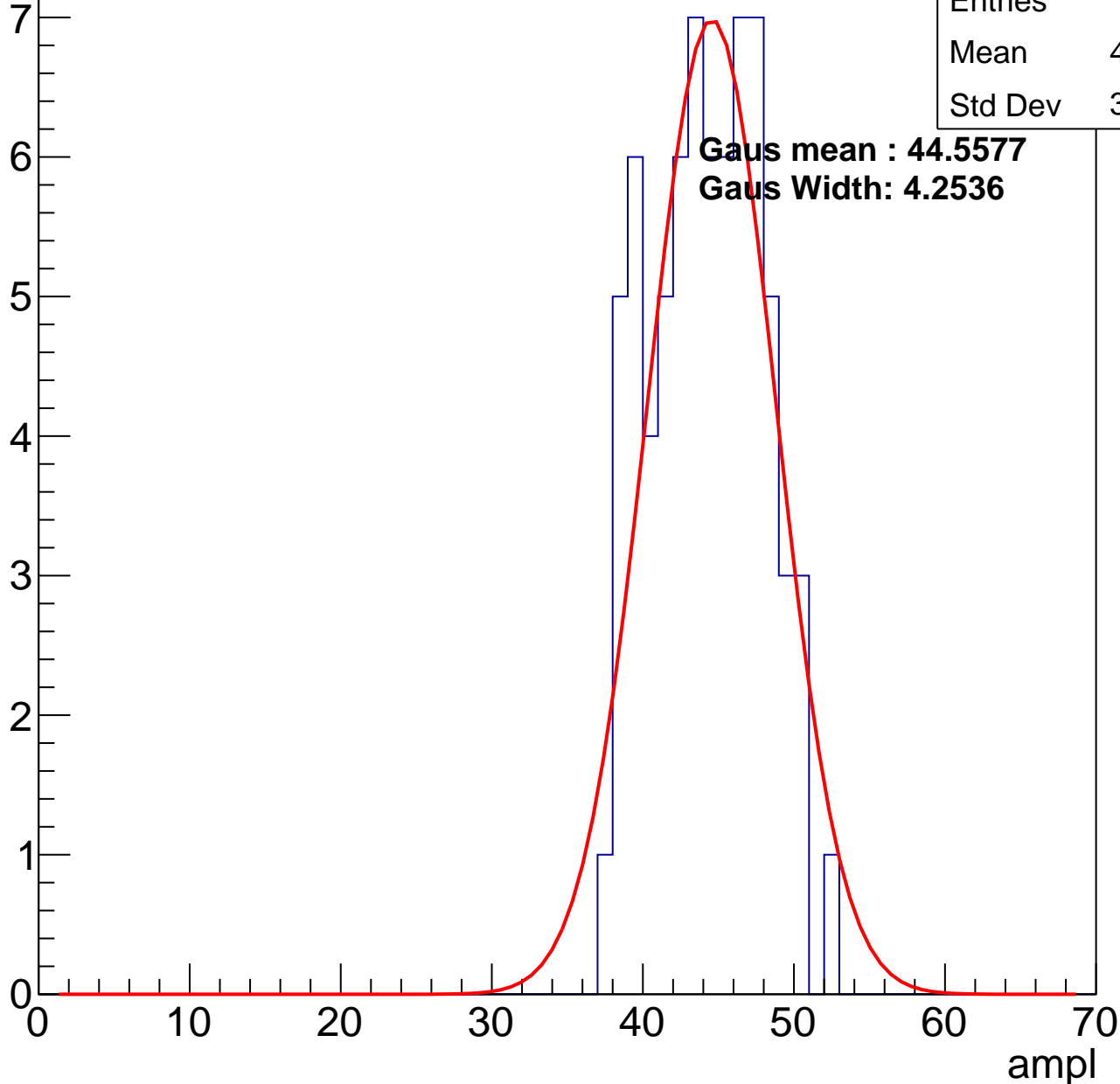


# B1L102S, U20-ch7, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	43.79
Std Dev	3.613

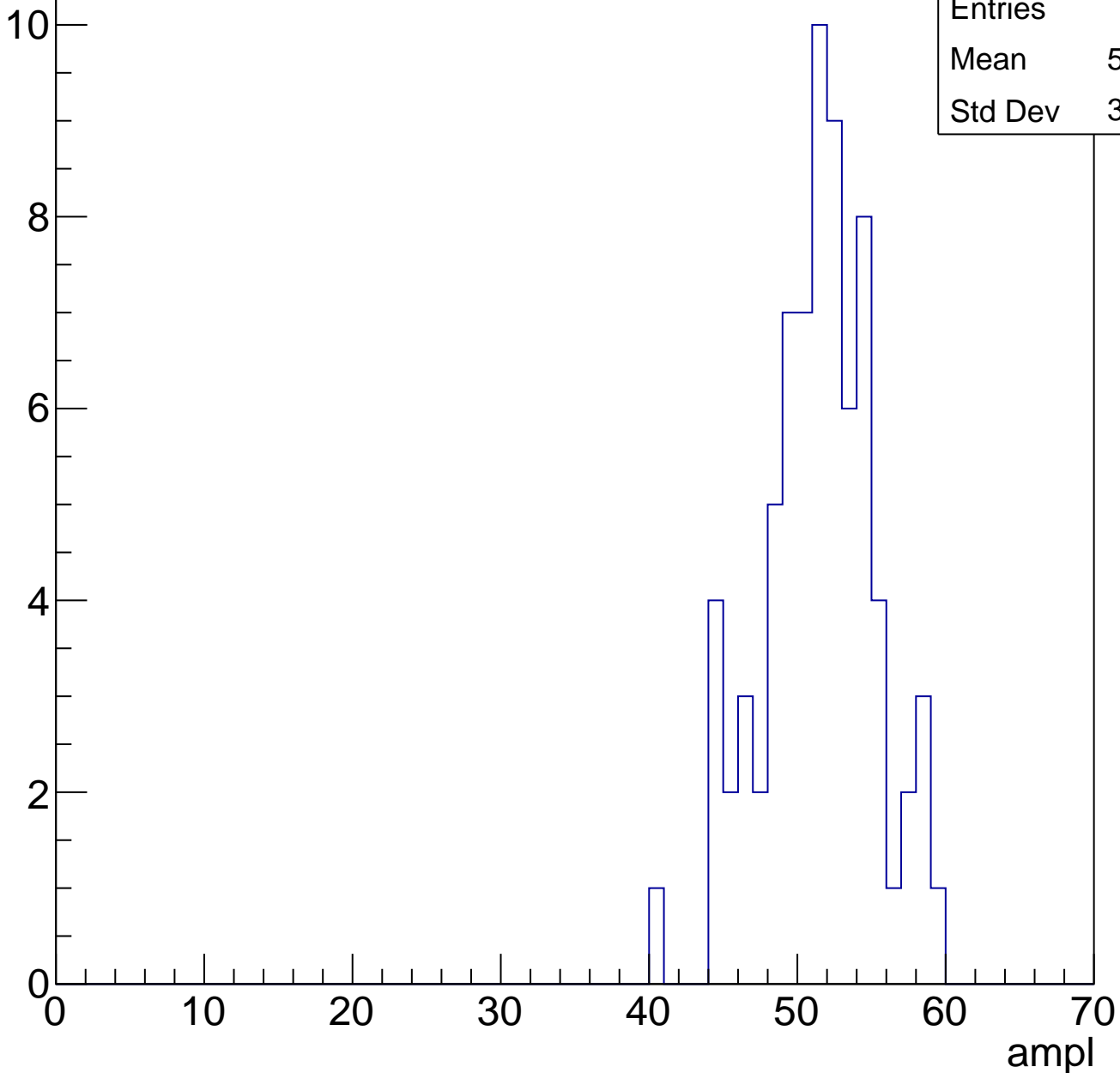


# B1L102S, U20-ch7, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	50.96
Std Dev	3.747

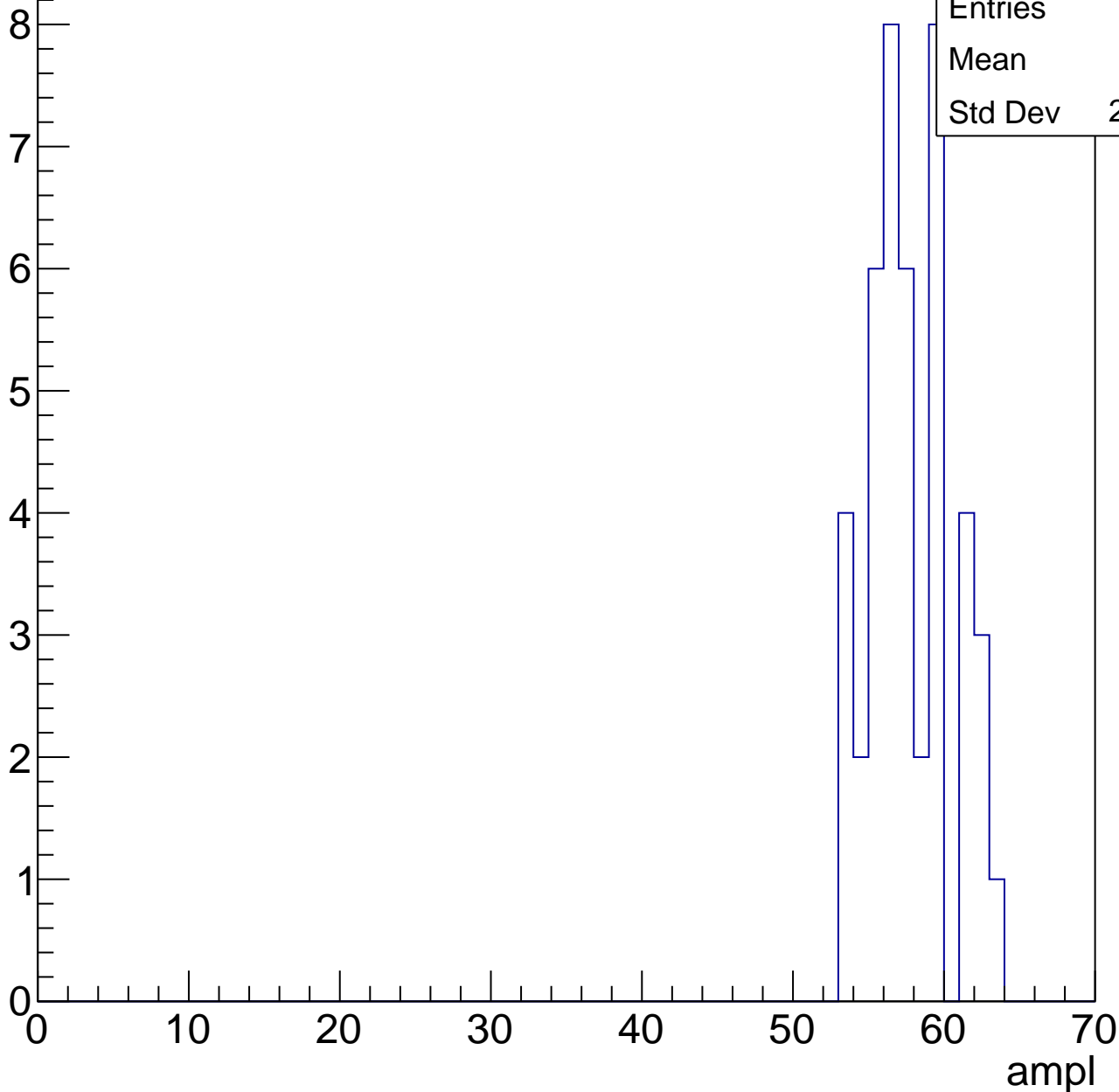


# B1L102S, U20-ch7, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	44
Mean	57.3
Std Dev	2.693

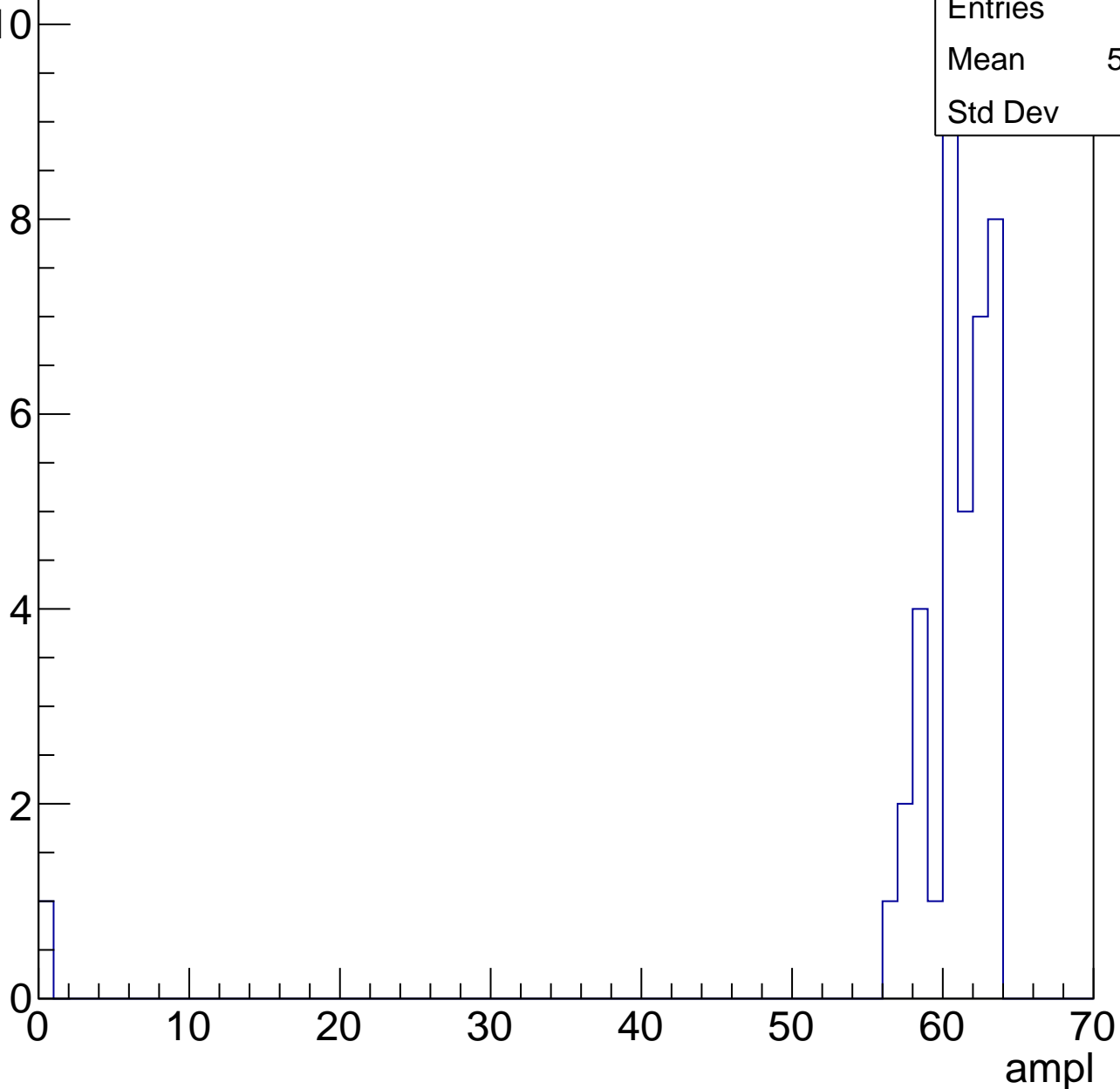


# B1L102S, U20-ch7, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

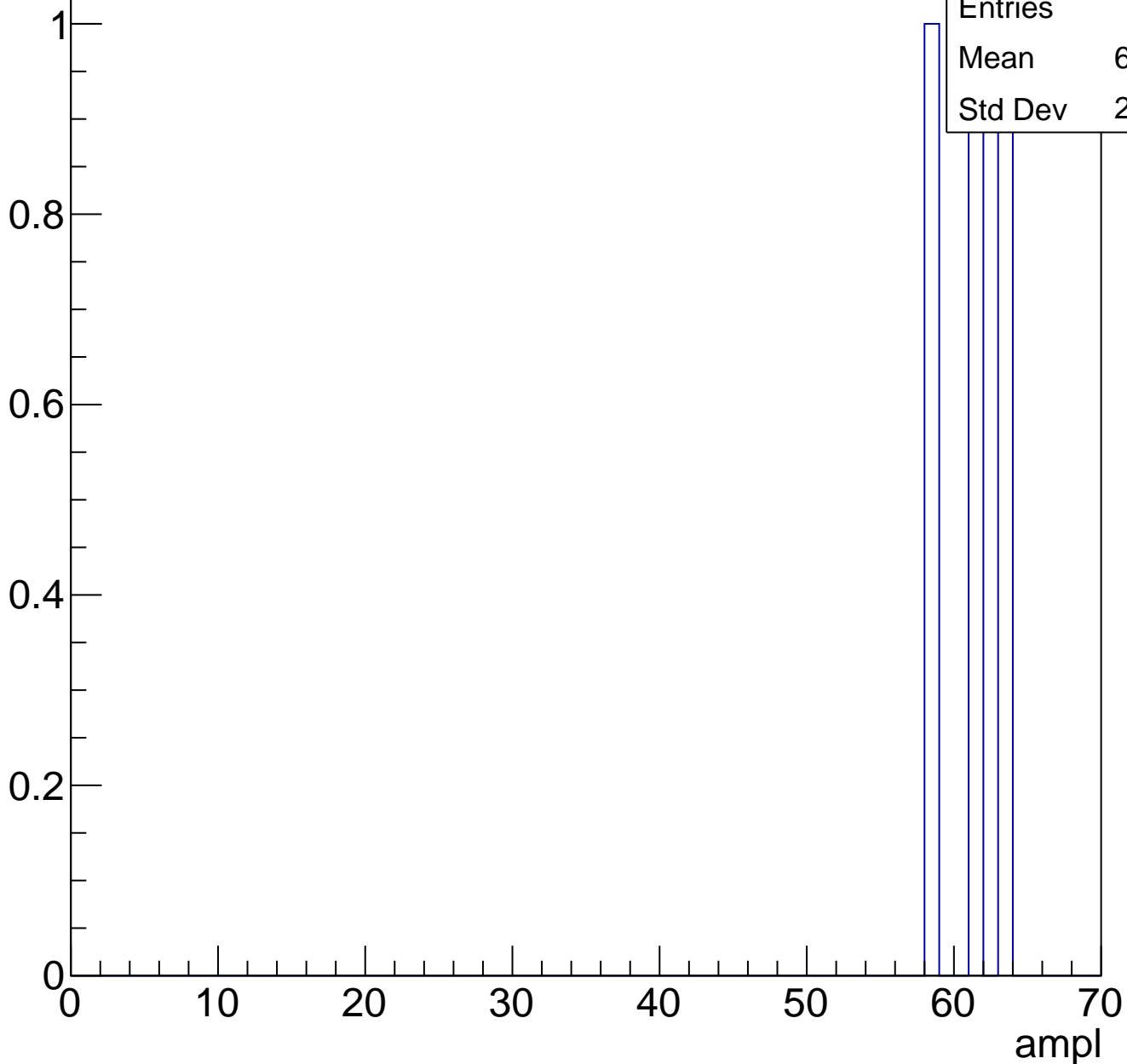
Entries	39
Mean	59.08
Std Dev	9.77



# B1L102S, U20-ch7, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U20-ch7, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U20-ch8, adc0

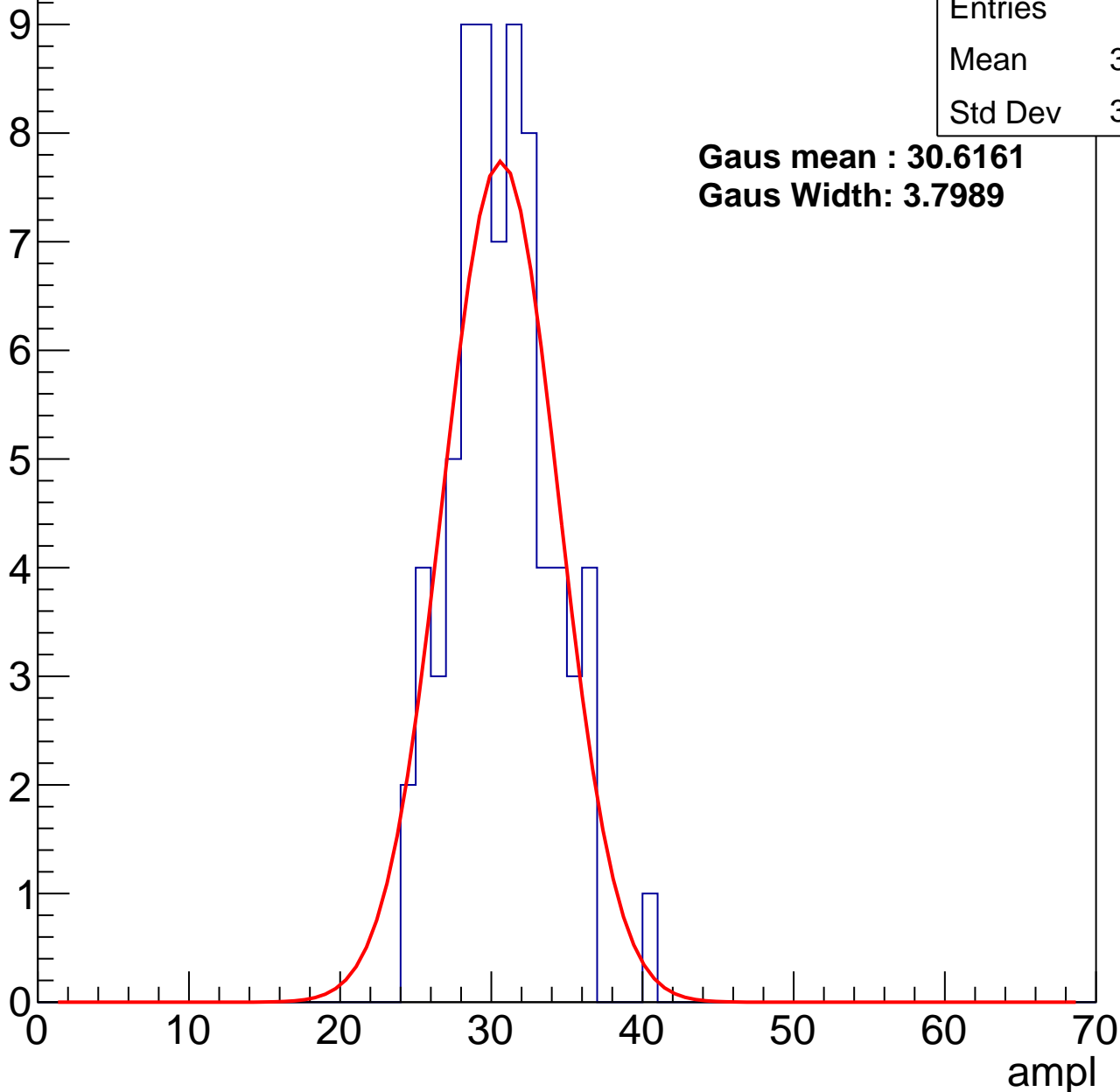
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	30.22
Std Dev	3.263

**Gaus mean : 30.6161**

**Gaus Width: 3.7989**



# B1L102S, U20-ch8, adc1

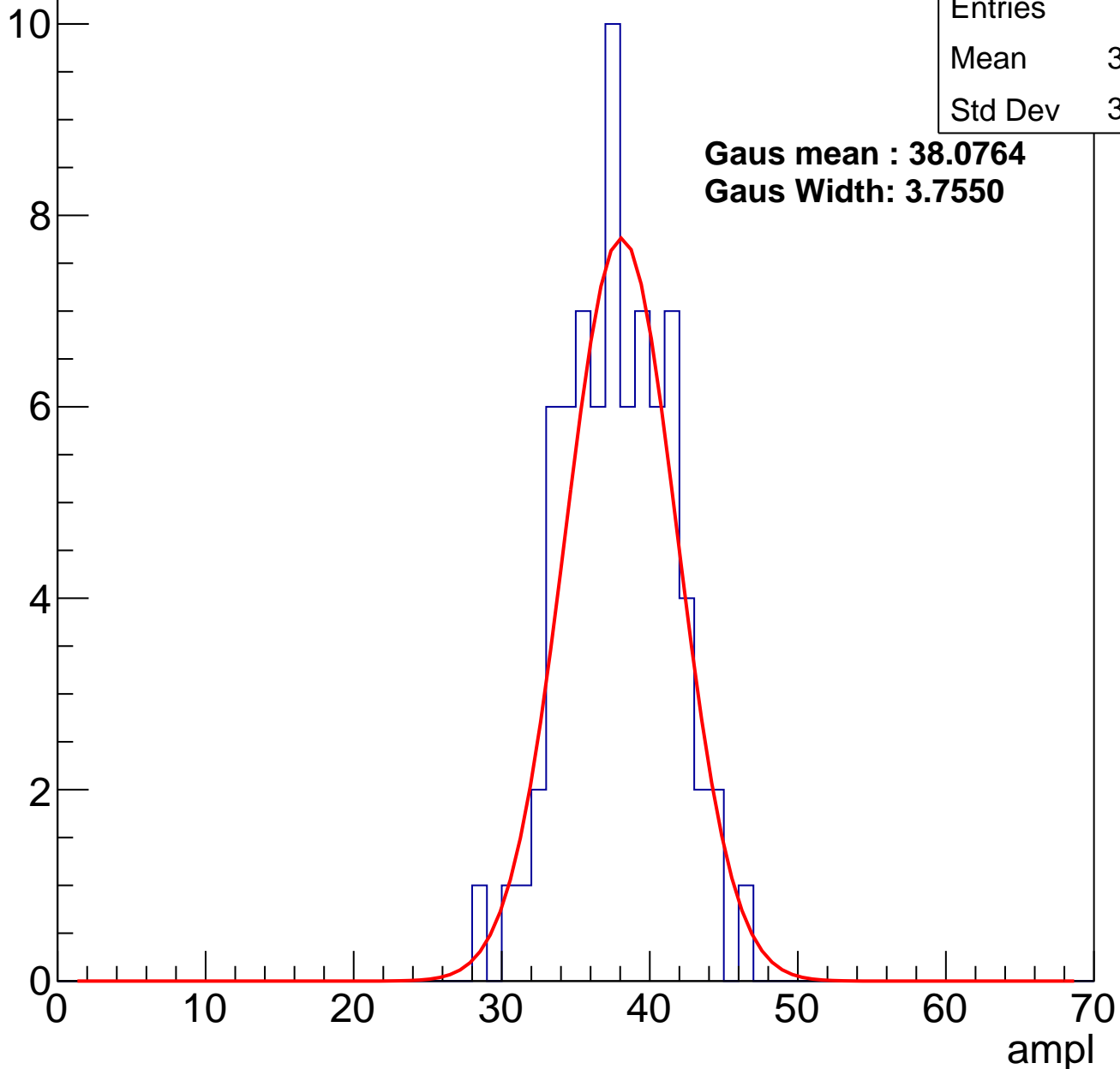
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	75
Mean	37.36
Std Dev	3.543

**Gaus mean : 38.0764**

**Gaus Width: 3.7550**

Entry



# B1L102S, U20-ch8, adc2

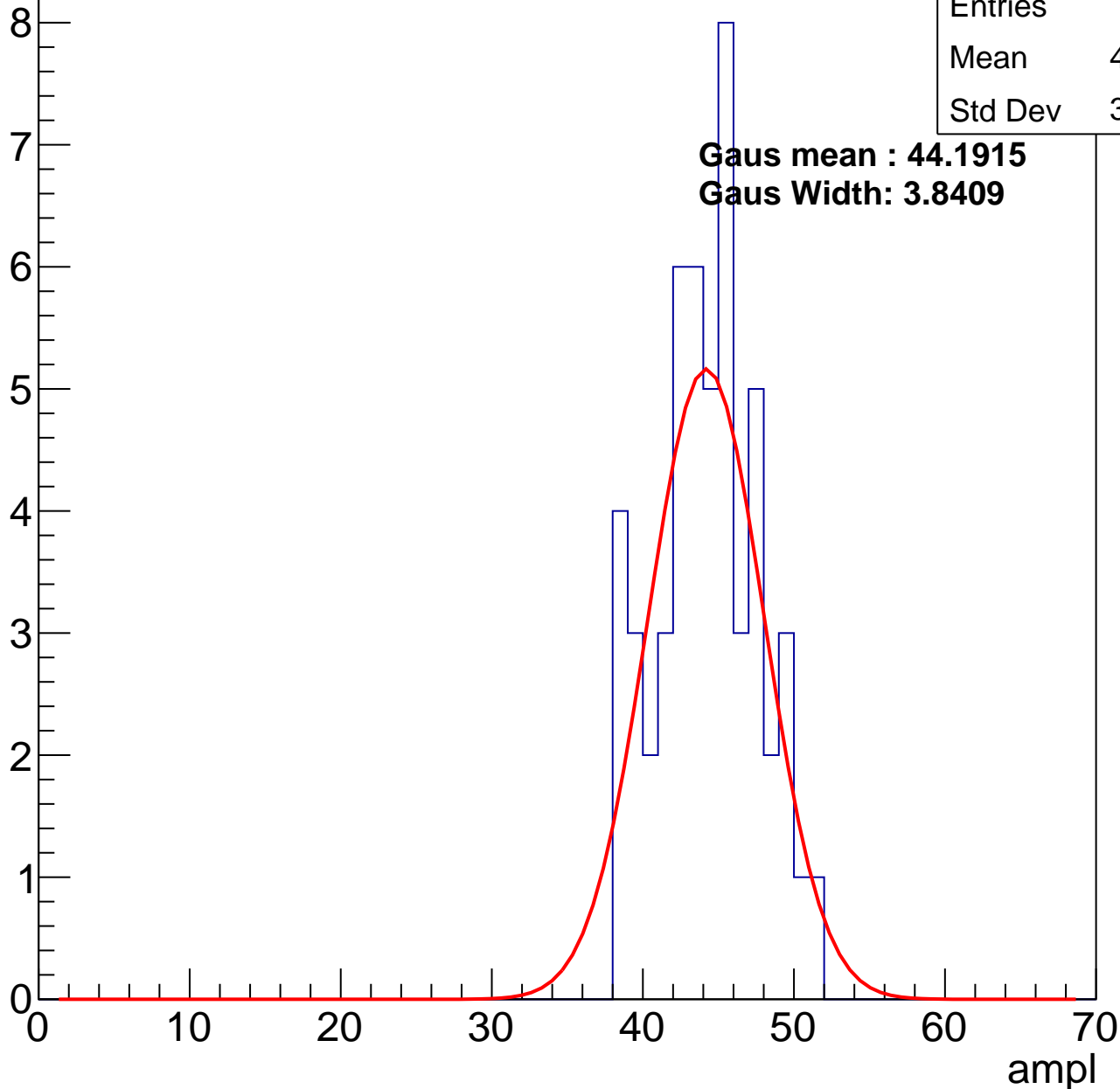
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	43.83
Std Dev	3.292

**Gaus mean : 44.1915**

**Gaus Width: 3.8409**

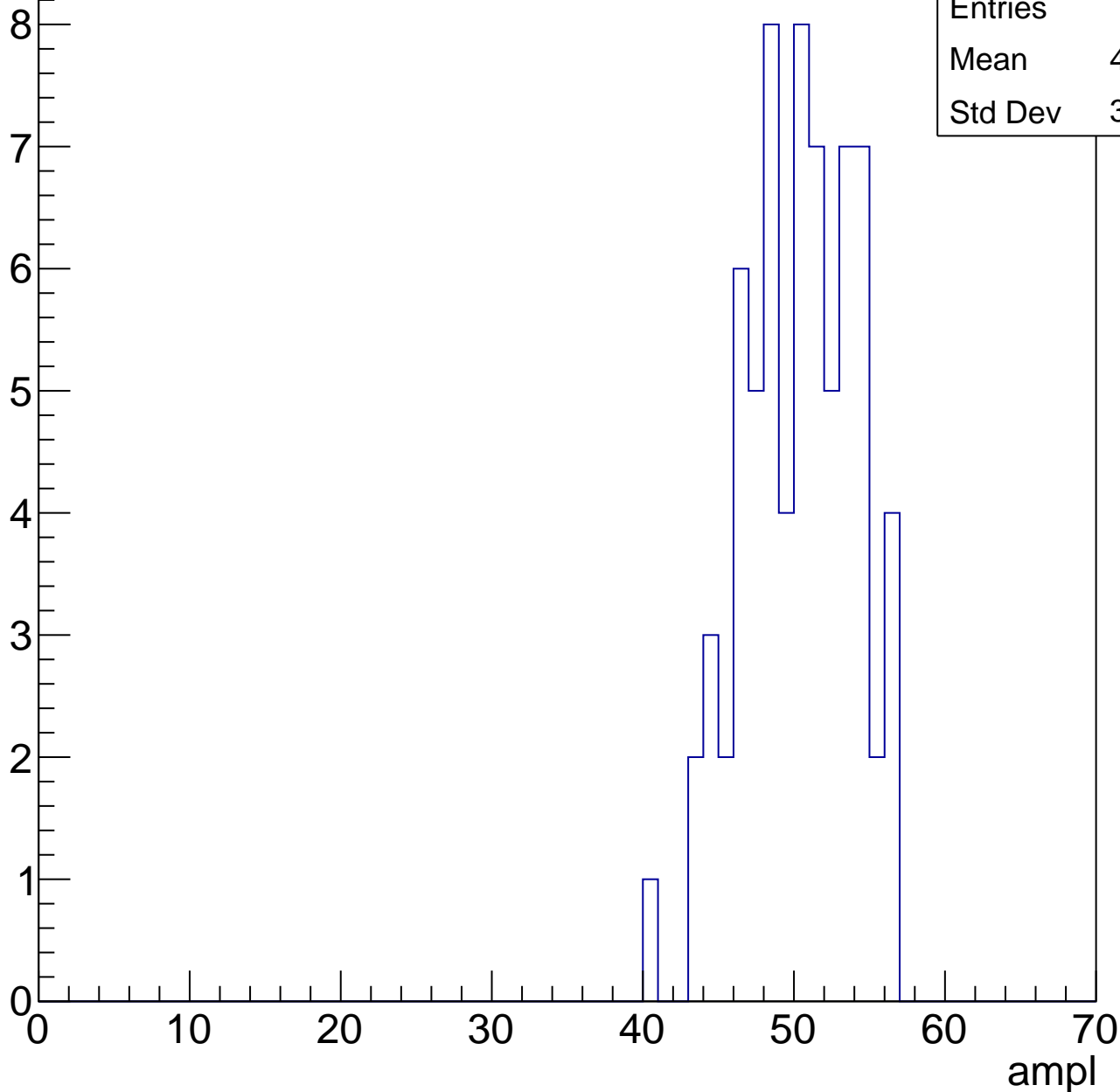


# B1L102S, U20-ch8, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	49.85
Std Dev	3.614

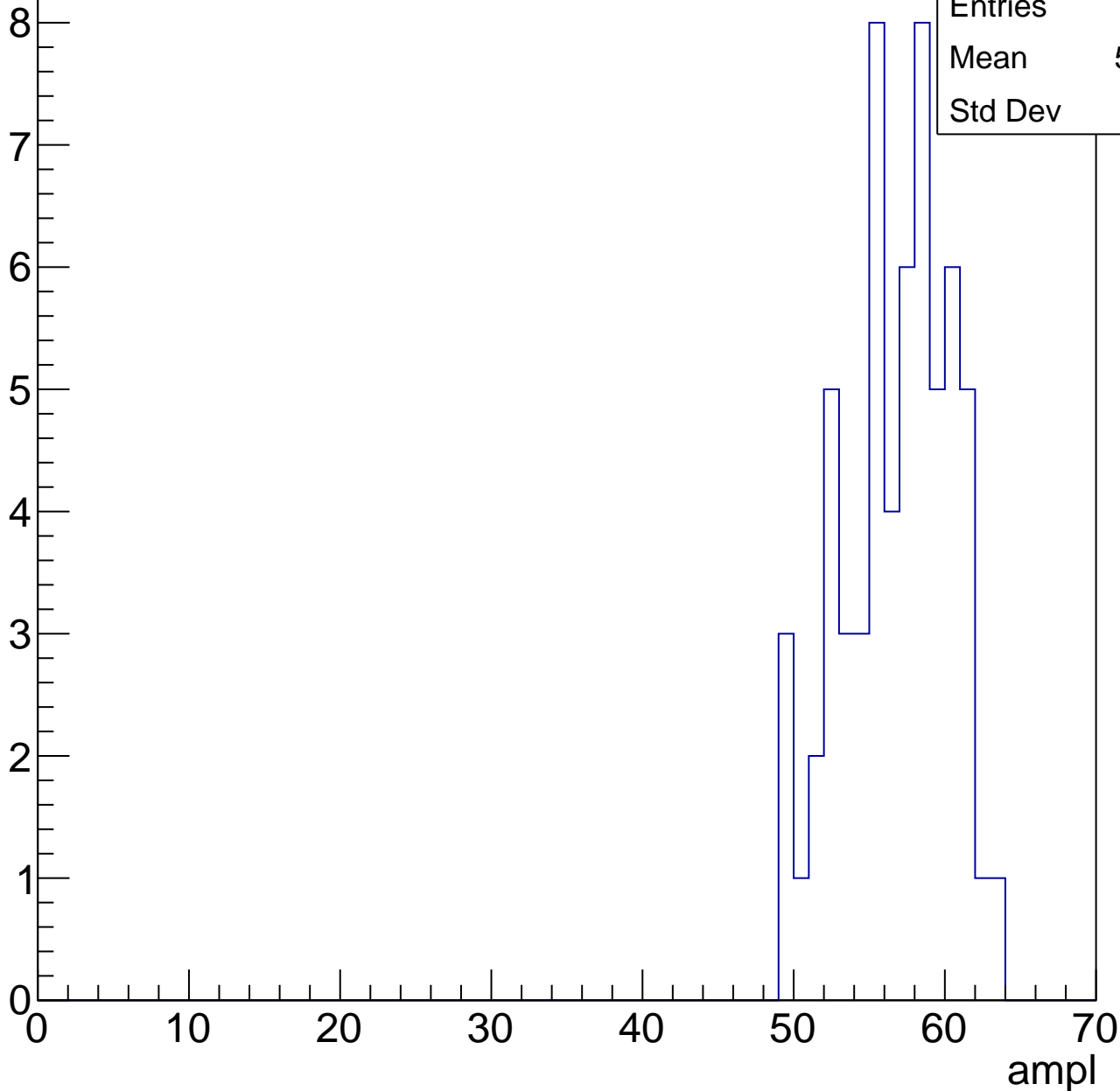


# B1L102S, U20-ch8, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	56.31
Std Dev	3.49

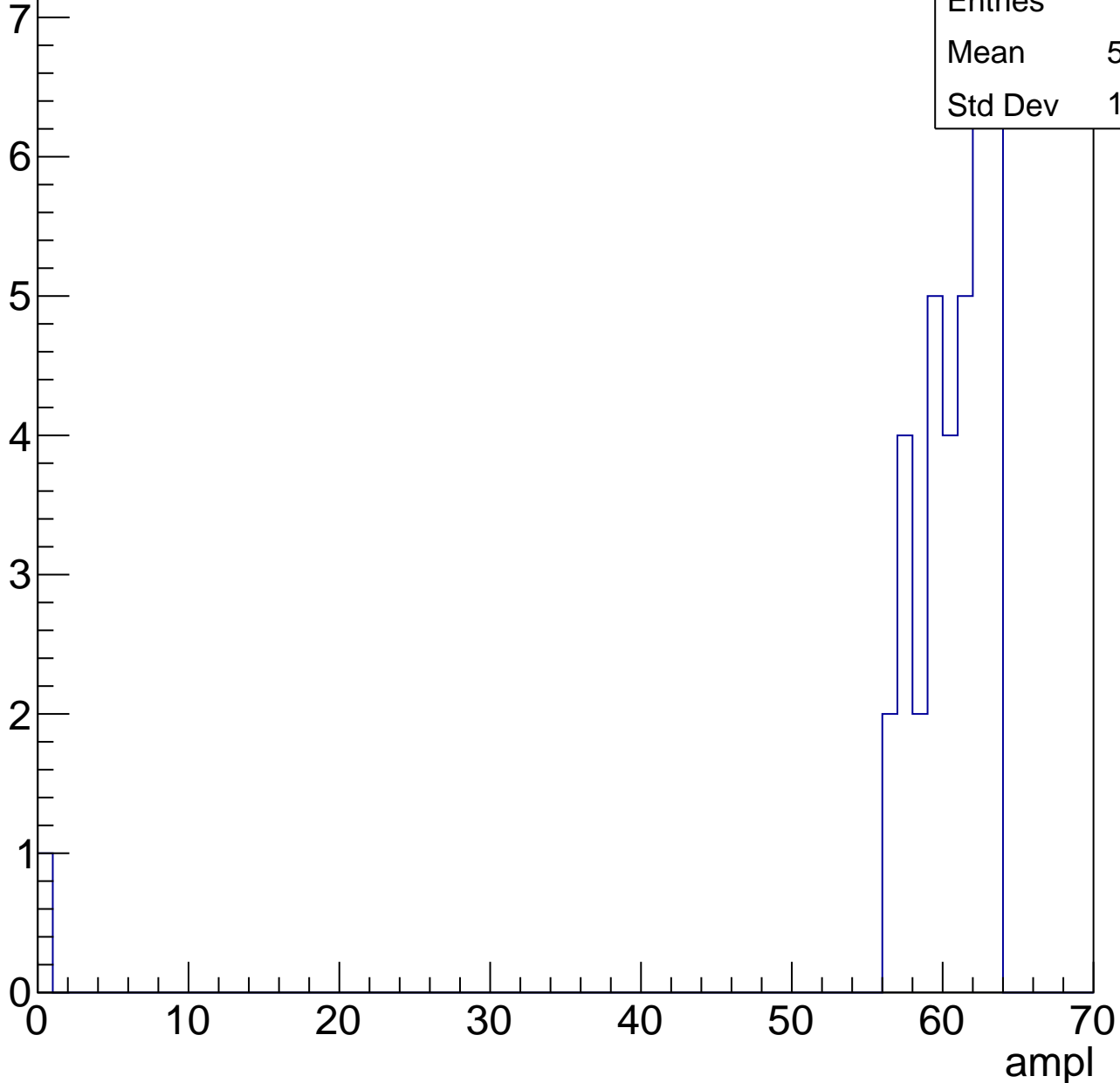


# B1L102S, U20-ch8, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	37
Mean	58.68
Std Dev	10.02



# B1L102S, U20-ch8, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U20-ch8, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch9, adc0

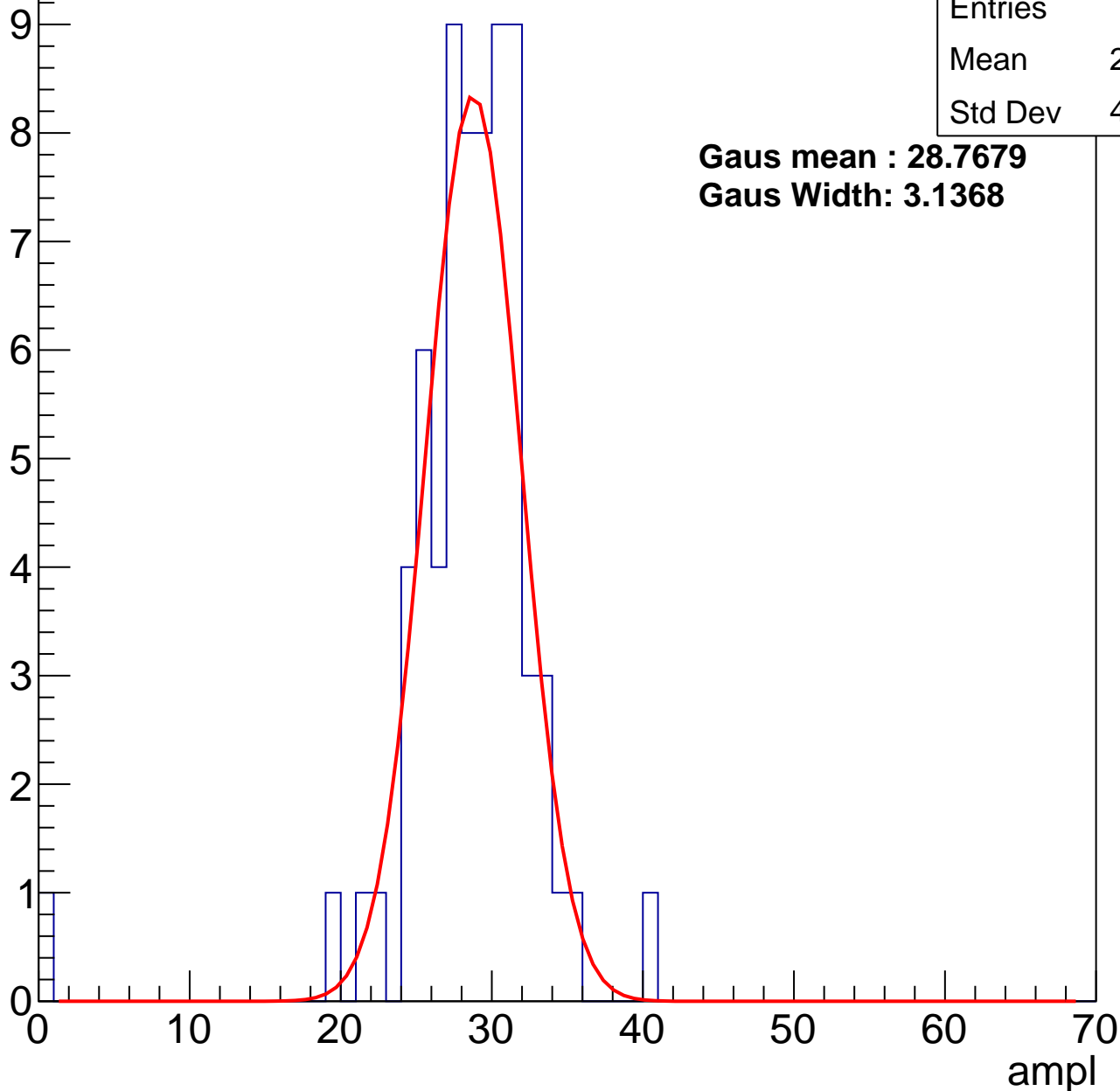
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	28.06
Std Dev	4.736

**Gaus mean : 28.7679**

**Gaus Width: 3.1368**

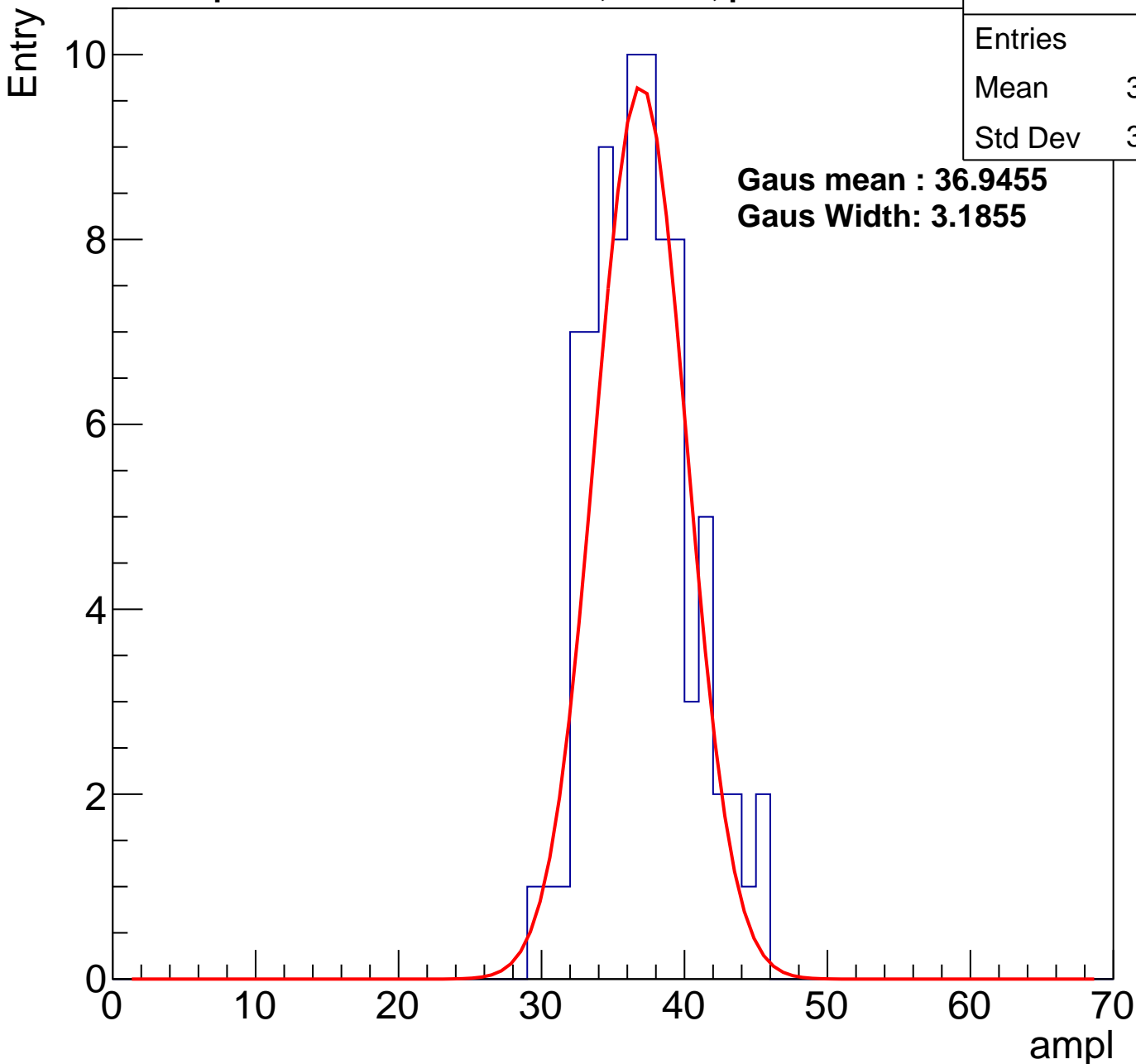


# B1L102S, U20-ch9, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	85
Mean	36.54
Std Dev	3.408

**Gaus mean : 36.9455**  
**Gaus Width: 3.1855**



# B1L102S, U20-ch9, adc2

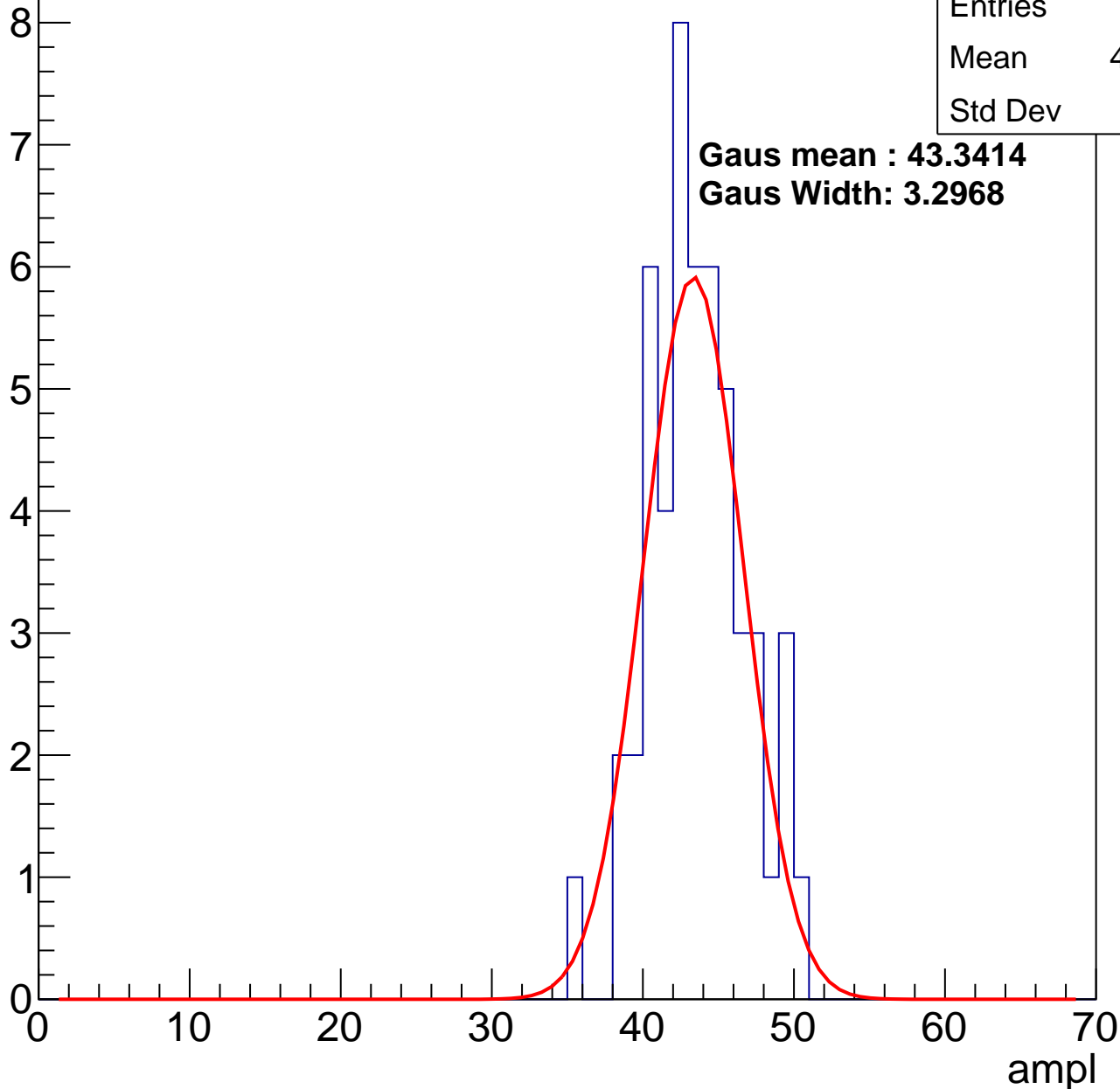
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	43.14
Std Dev	3.15

**Gaus mean : 43.3414**

**Gaus Width: 3.2968**

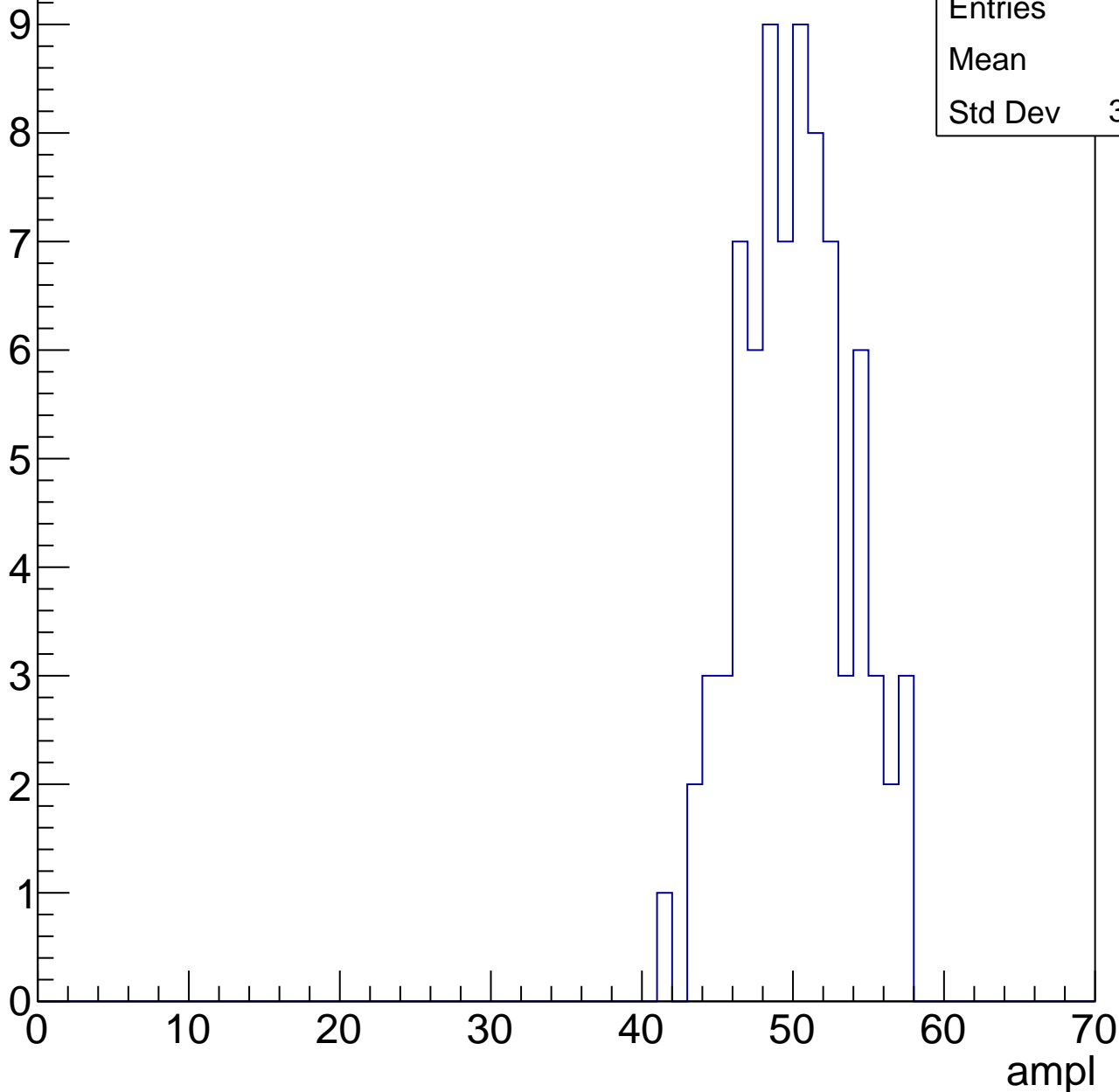


# B1L102S, U20-ch9, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	79
Mean	49.7
Std Dev	3.587

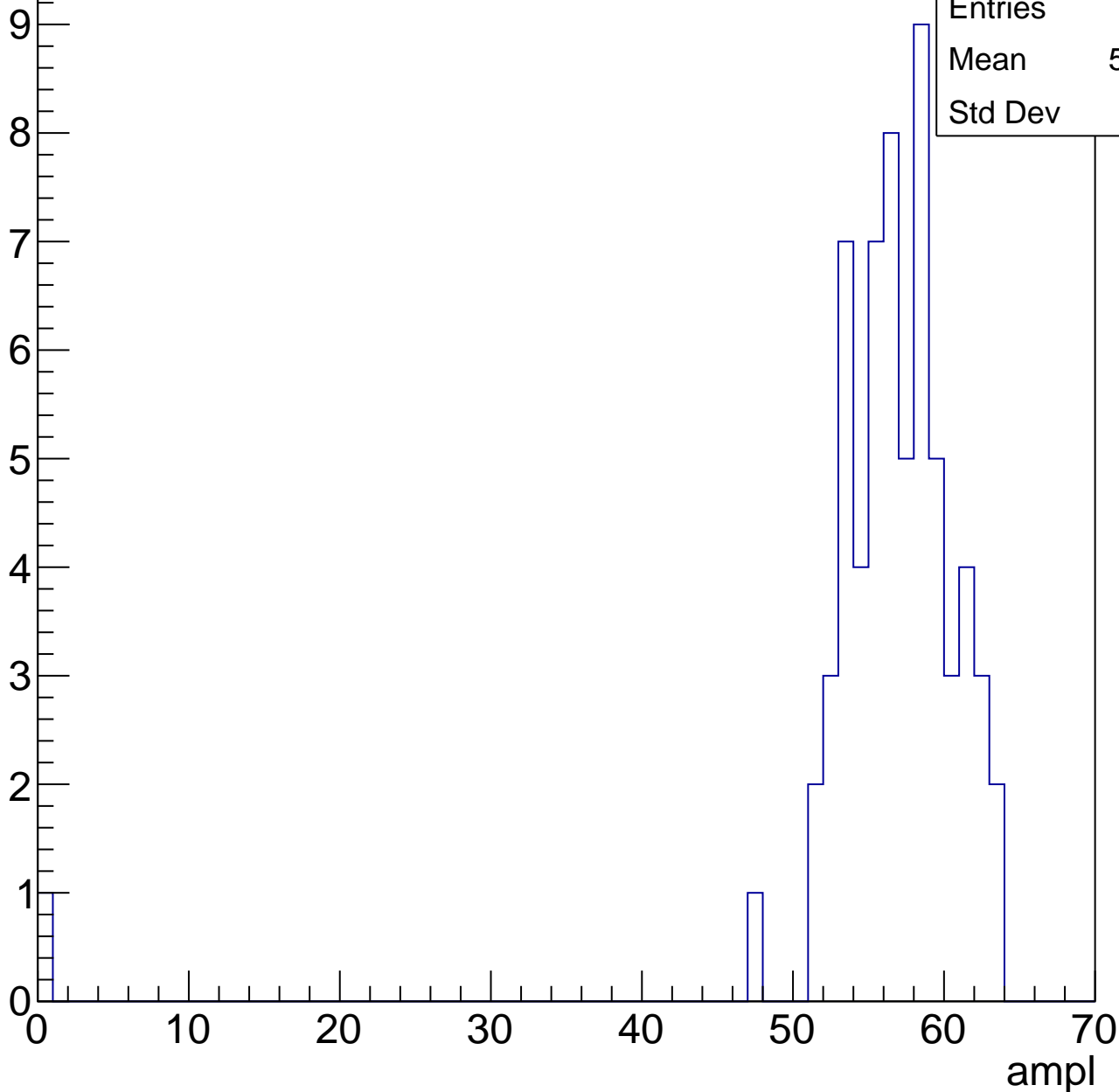


# B1L102S, U20-ch9, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

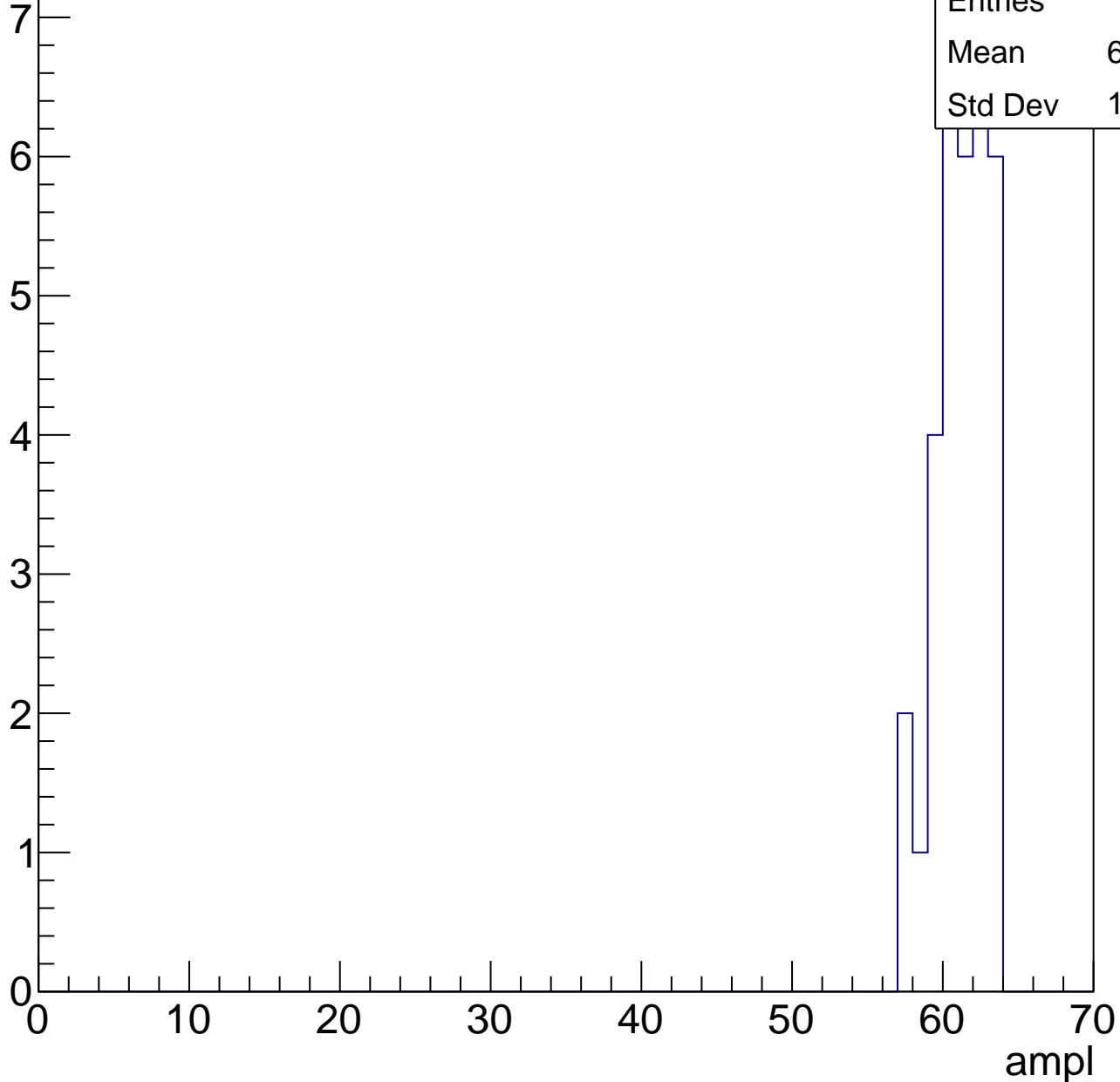
Entries	64
Mean	55.67
Std Dev	7.74



# B1L102S, U20-ch9, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	33
Mean	60.79
Std Dev	1.683

# B1L102S, U20-ch9, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U20-ch9, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch10, adc0

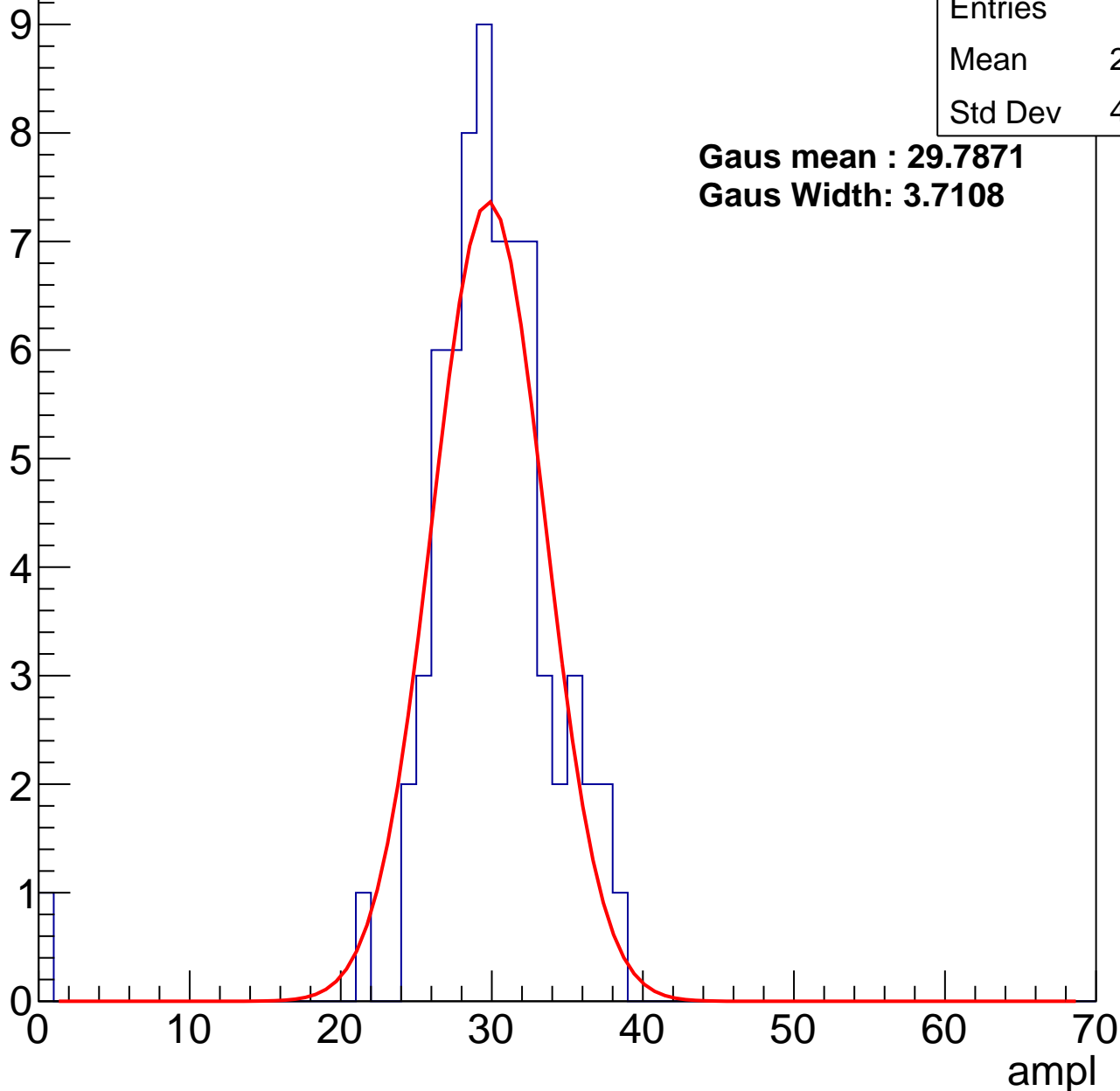
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	29.34
Std Dev	4.916

**Gaus mean : 29.7871**

**Gaus Width: 3.7108**



# B1L102S, U20-ch10, adc1

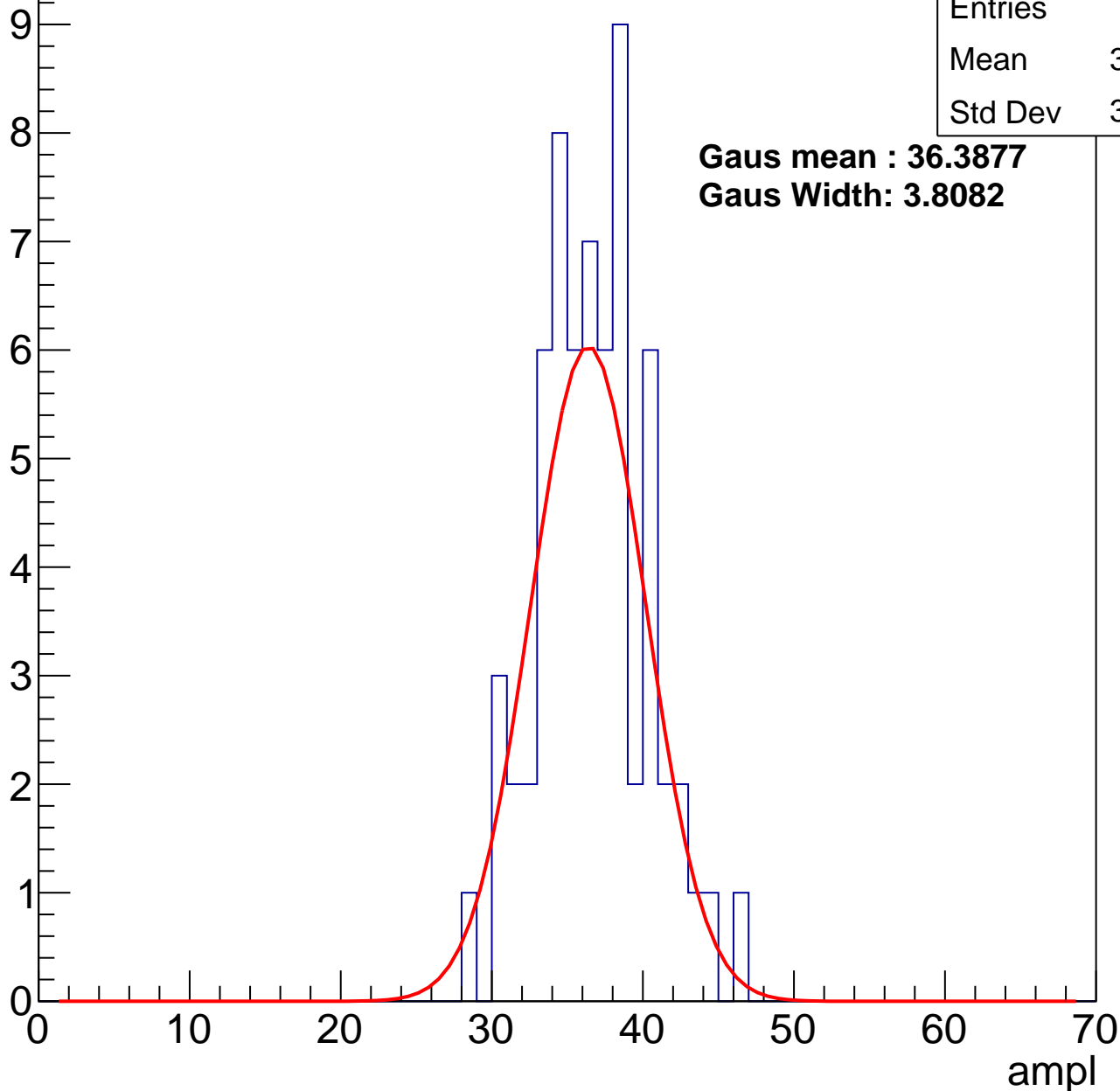
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	36.26
Std Dev	3.579

**Gaus mean : 36.3877**

**Gaus Width: 3.8082**



# B1L102S, U20-ch10, adc2

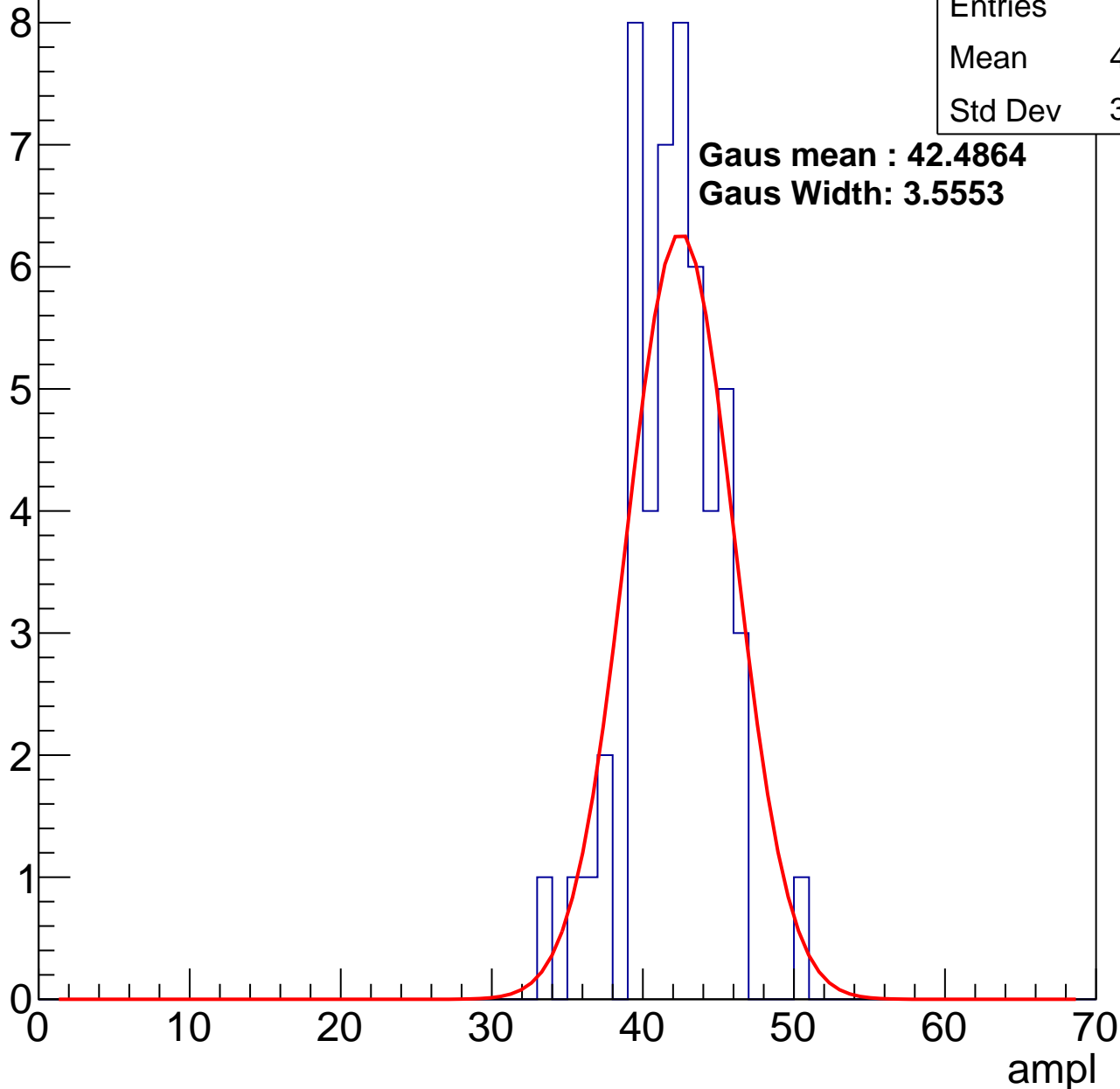
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	41.57
Std Dev	3.069

**Gaus mean : 42.4864**

**Gaus Width: 3.5553**

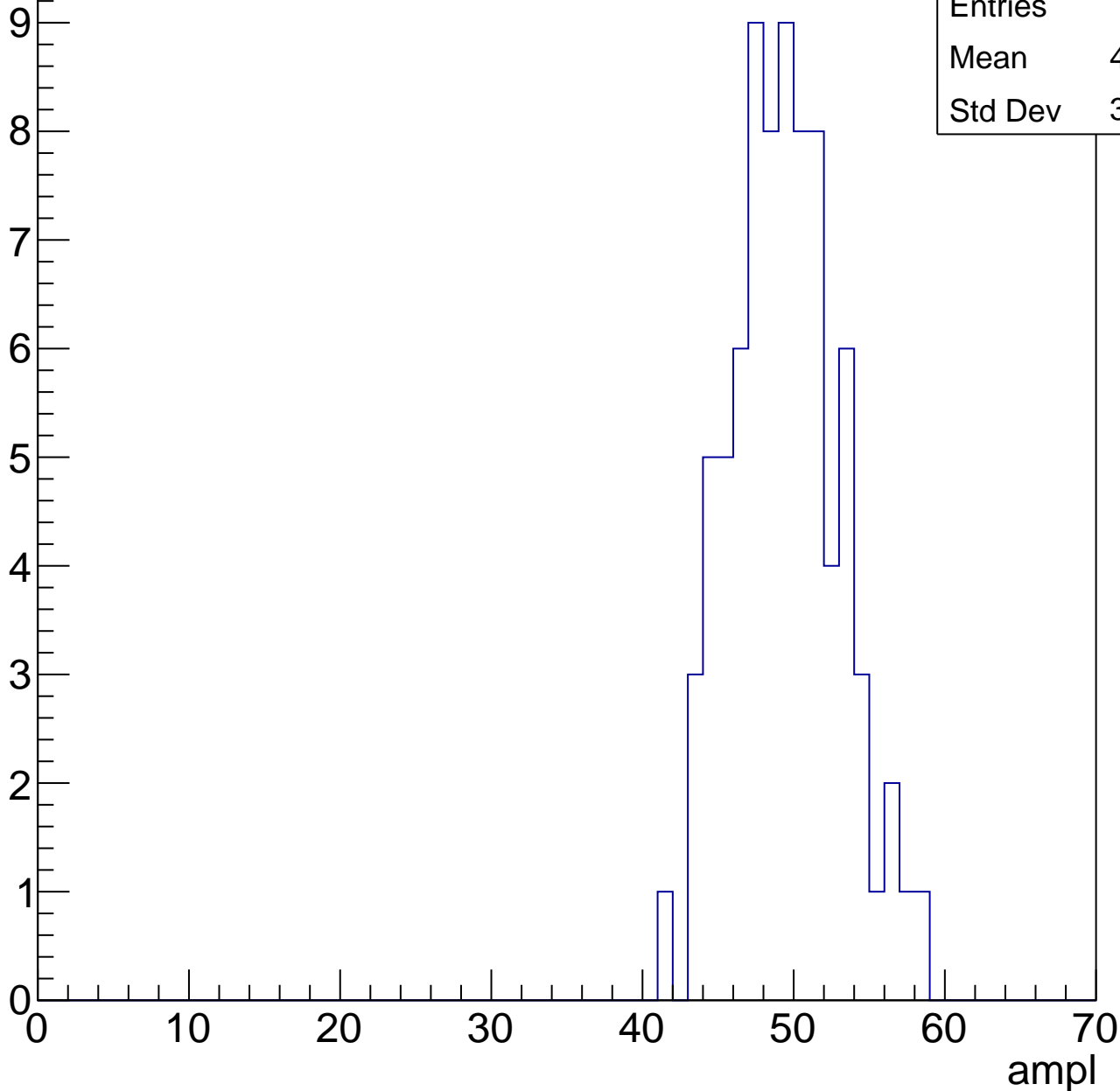


# B1L102S, U20-ch10, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

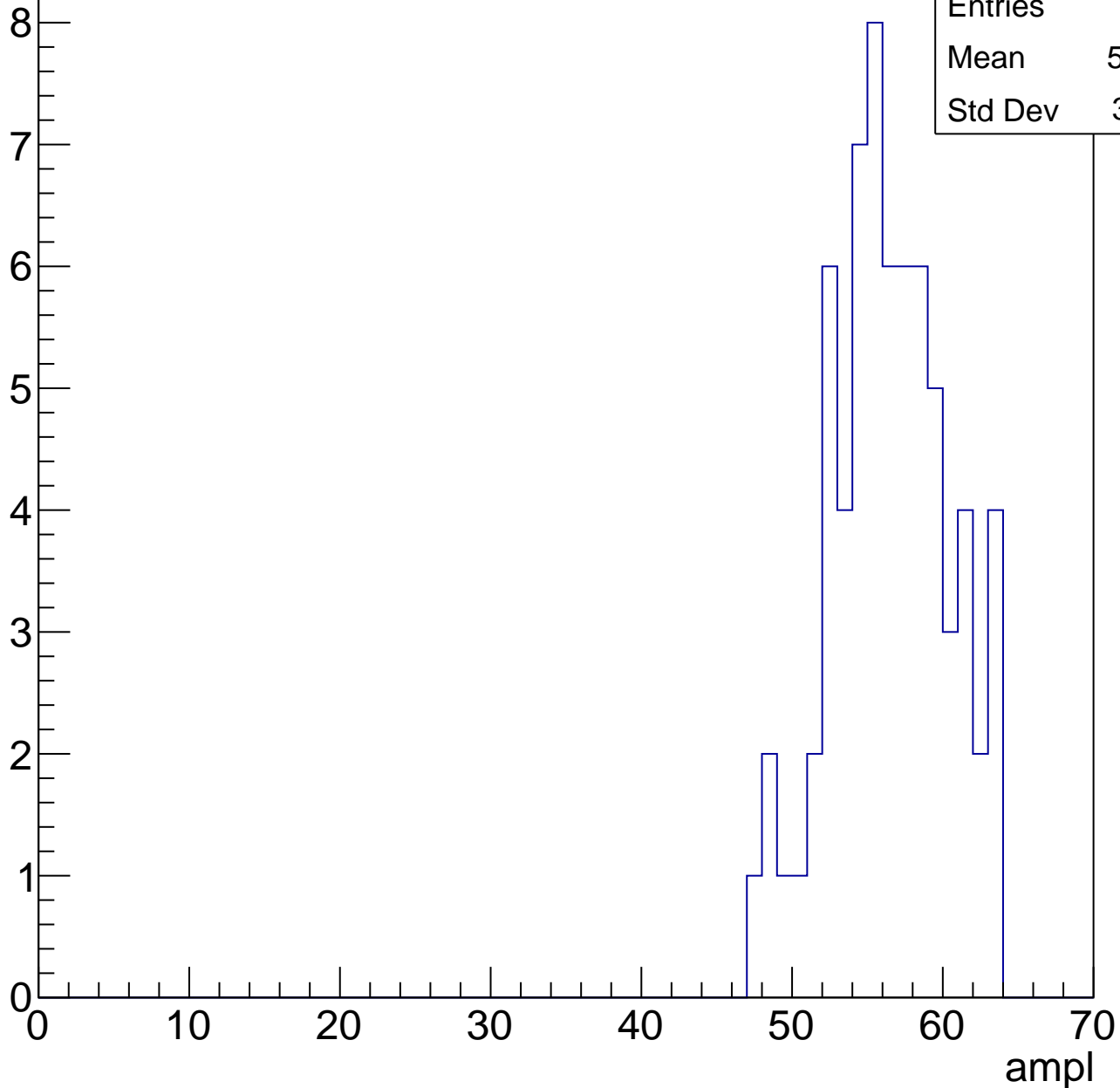
Entries	80
Mean	48.96
Std Dev	3.537



# B1L102S, U20-ch10, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



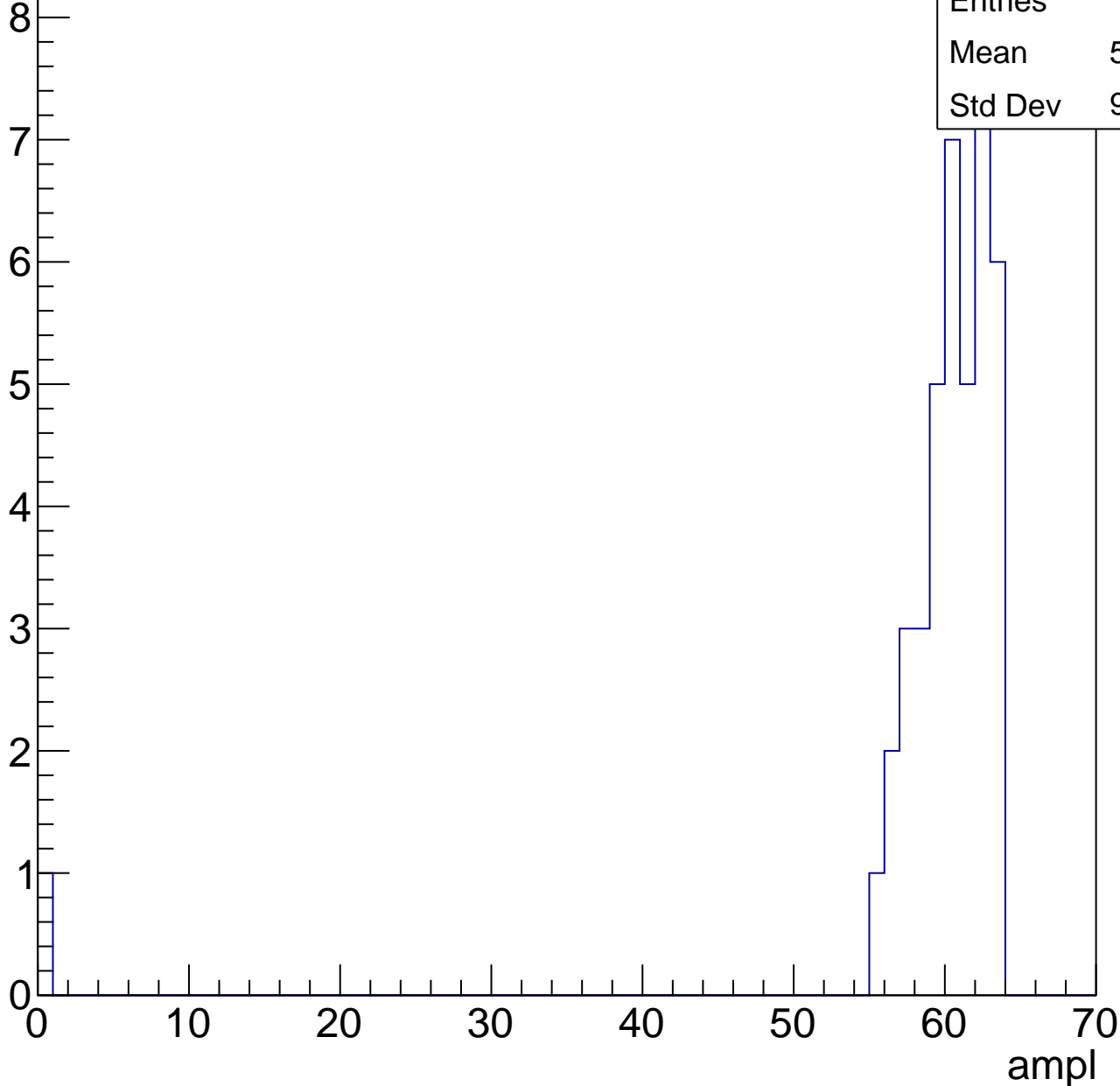
Entries	68
Mean	55.99
Std Dev	3.841

# B1L102S, U20-ch10, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	41
Mean	58.68
Std Dev	9.526



# B1L102S, U20-ch10, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U20-ch10, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch11, adc0

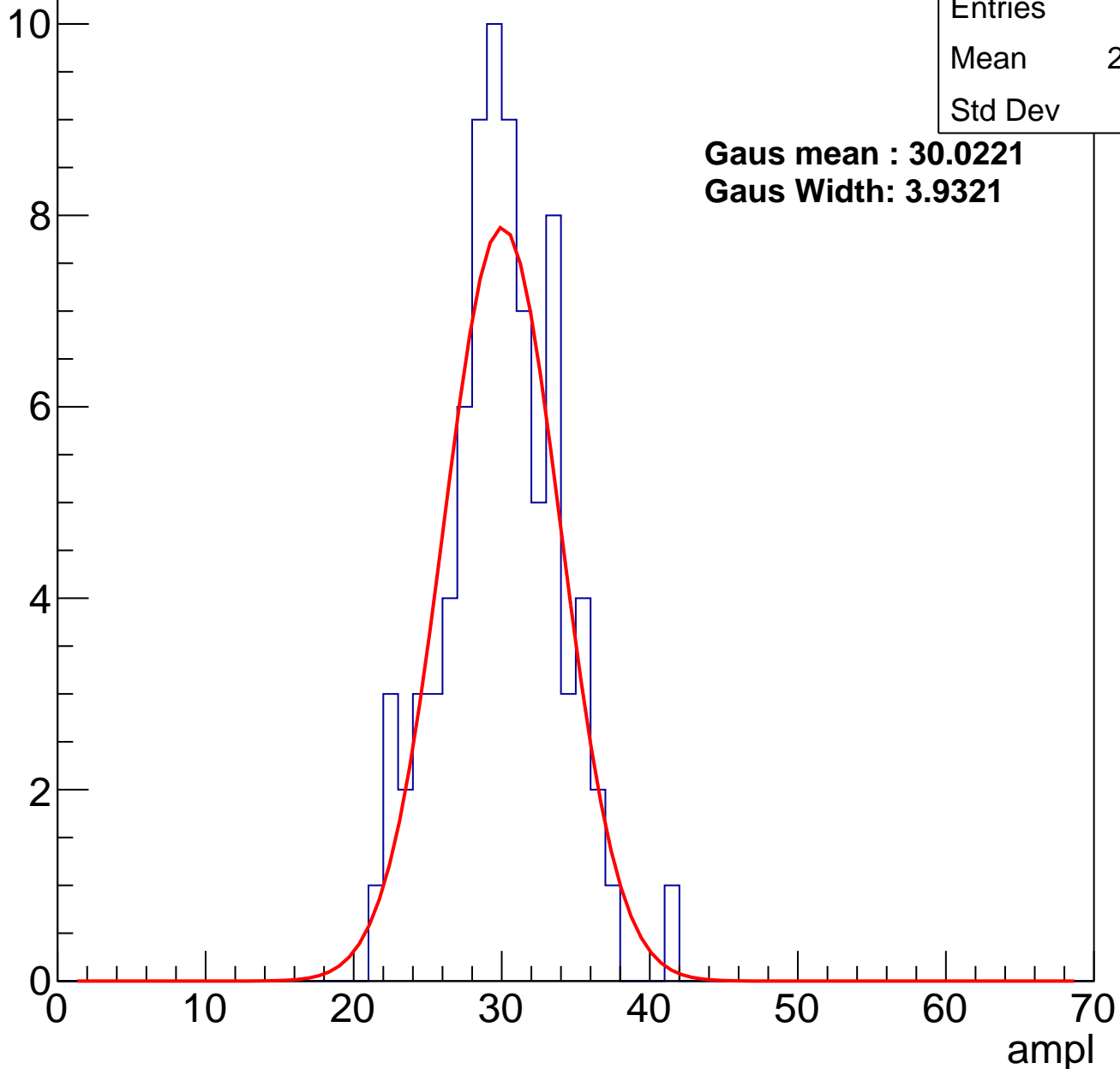
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	81
Mean	29.52
Std Dev	3.83

**Gaus mean : 30.0221**

**Gaus Width: 3.9321**

Entry



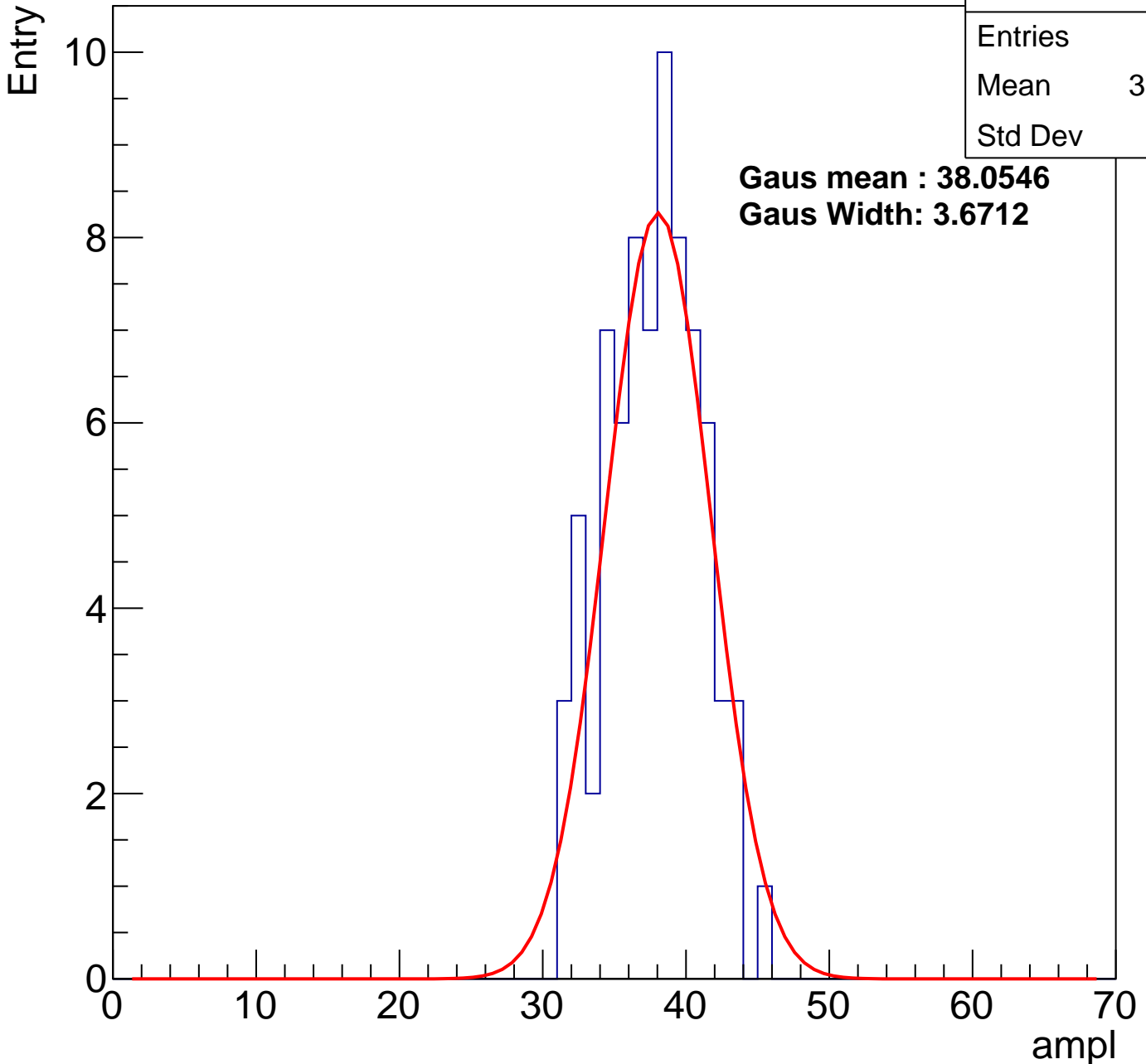
# B1L102S, U20-ch11, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	76
Mean	37.26
Std Dev	3.25

**Gaus mean : 38.0546**

**Gaus Width: 3.6712**



# B1L102S, U20-ch11, adc2

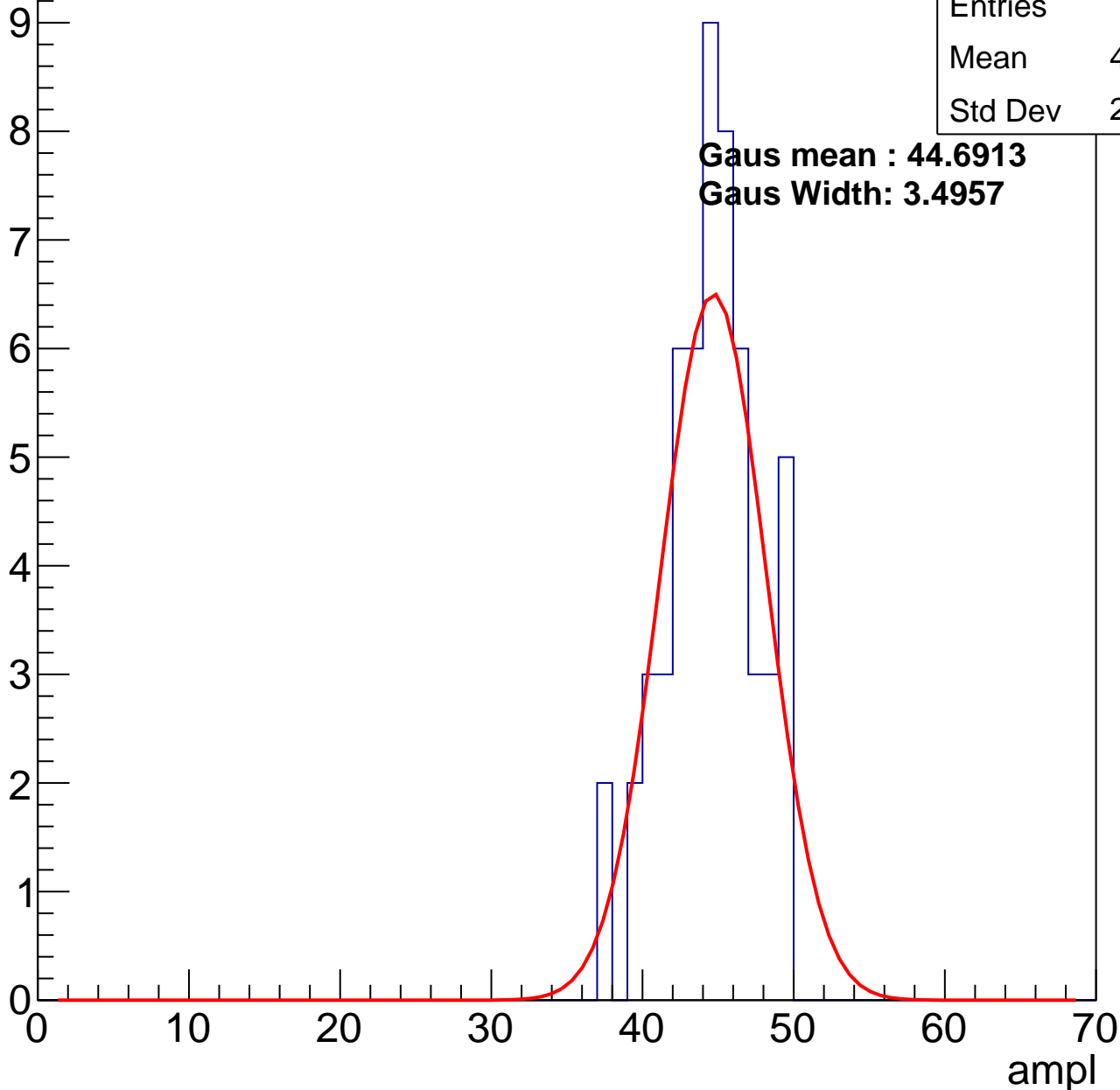
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	44.05
Std Dev	2.942

**Gaus mean : 44.6913**

**Gaus Width: 3.4957**

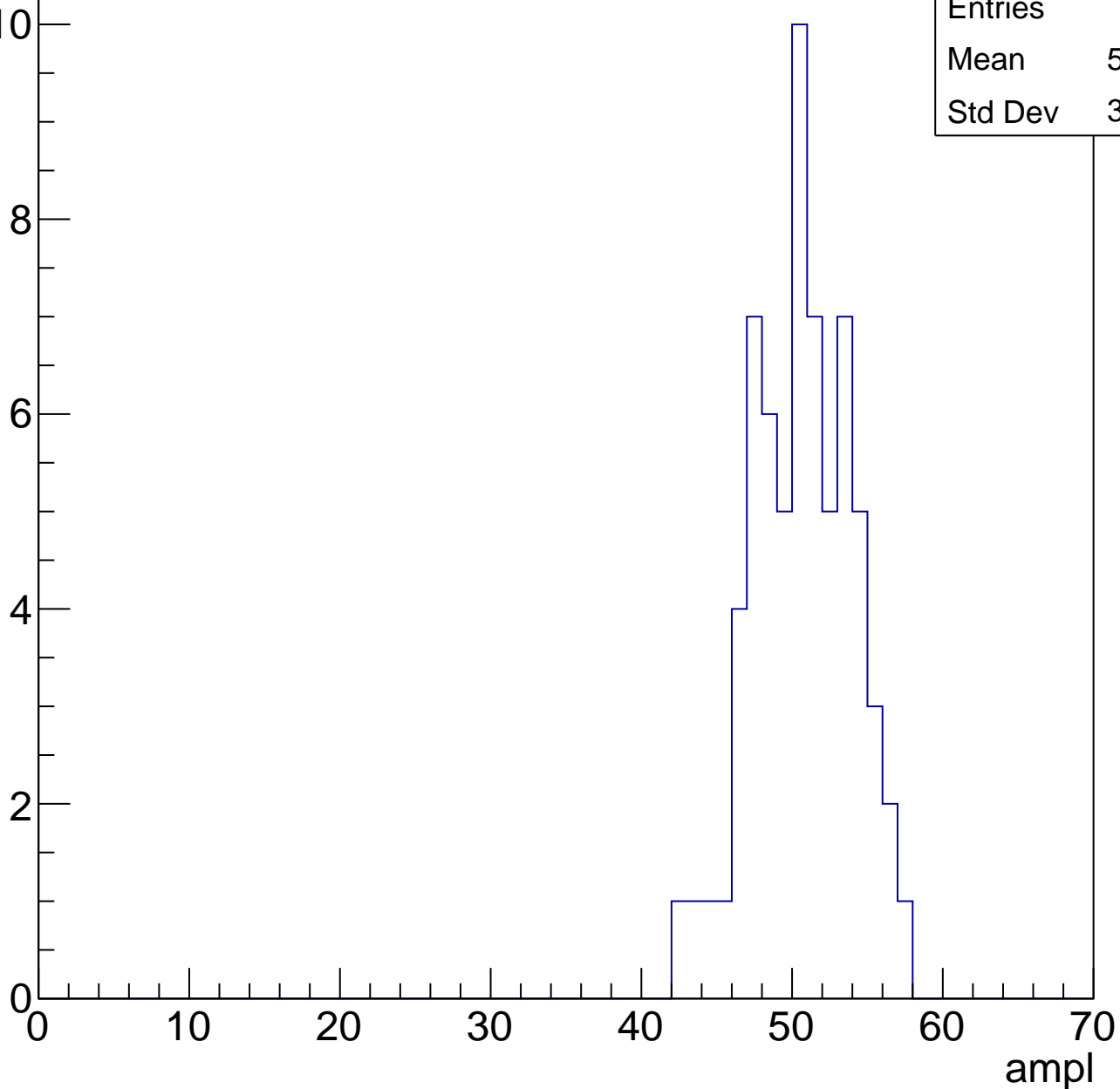


# B1L102S, U20-ch11, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	50.18
Std Dev	3.242

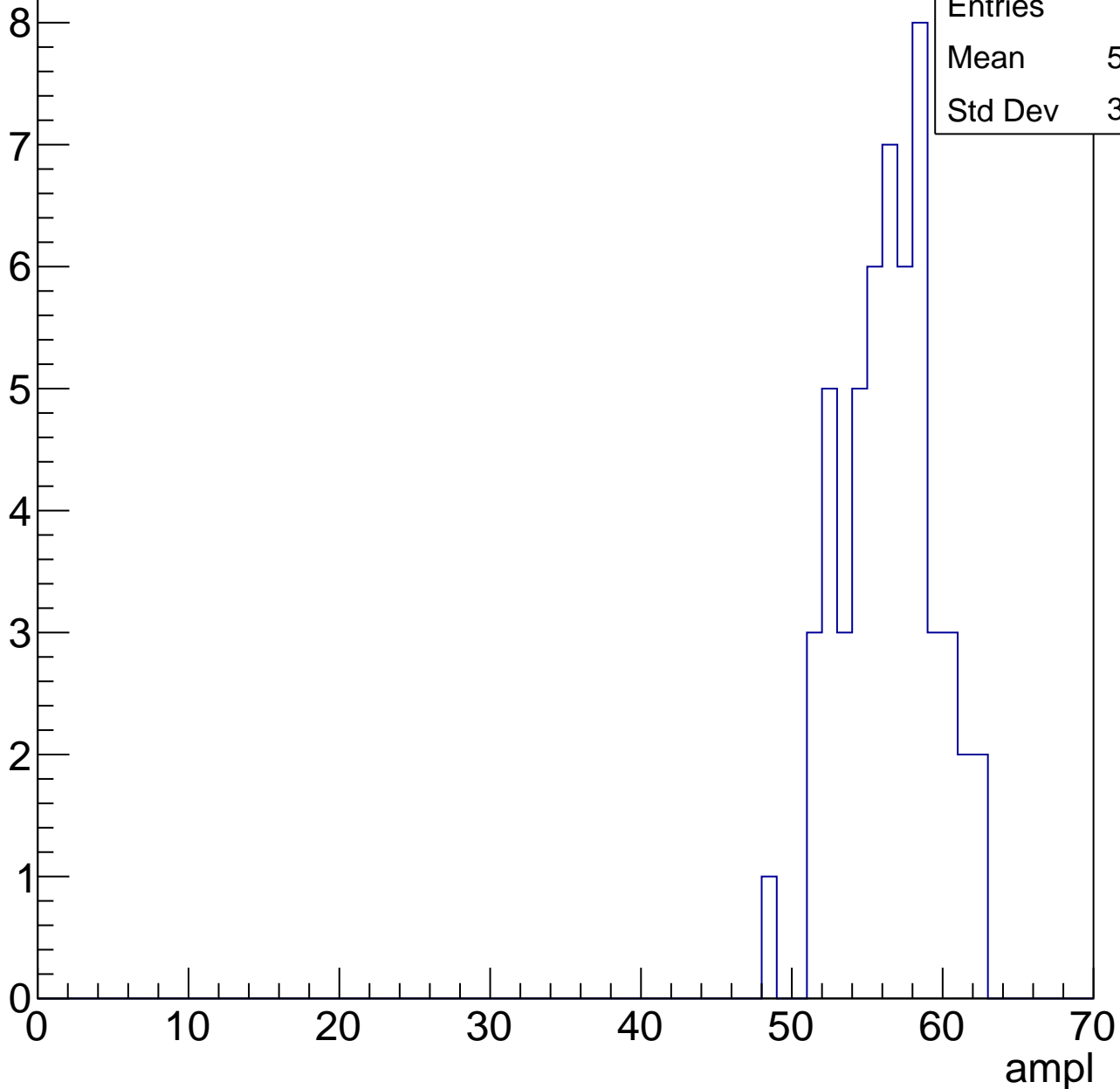


# B1L102S, U20-ch11, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	55.94
Std Dev	3.064

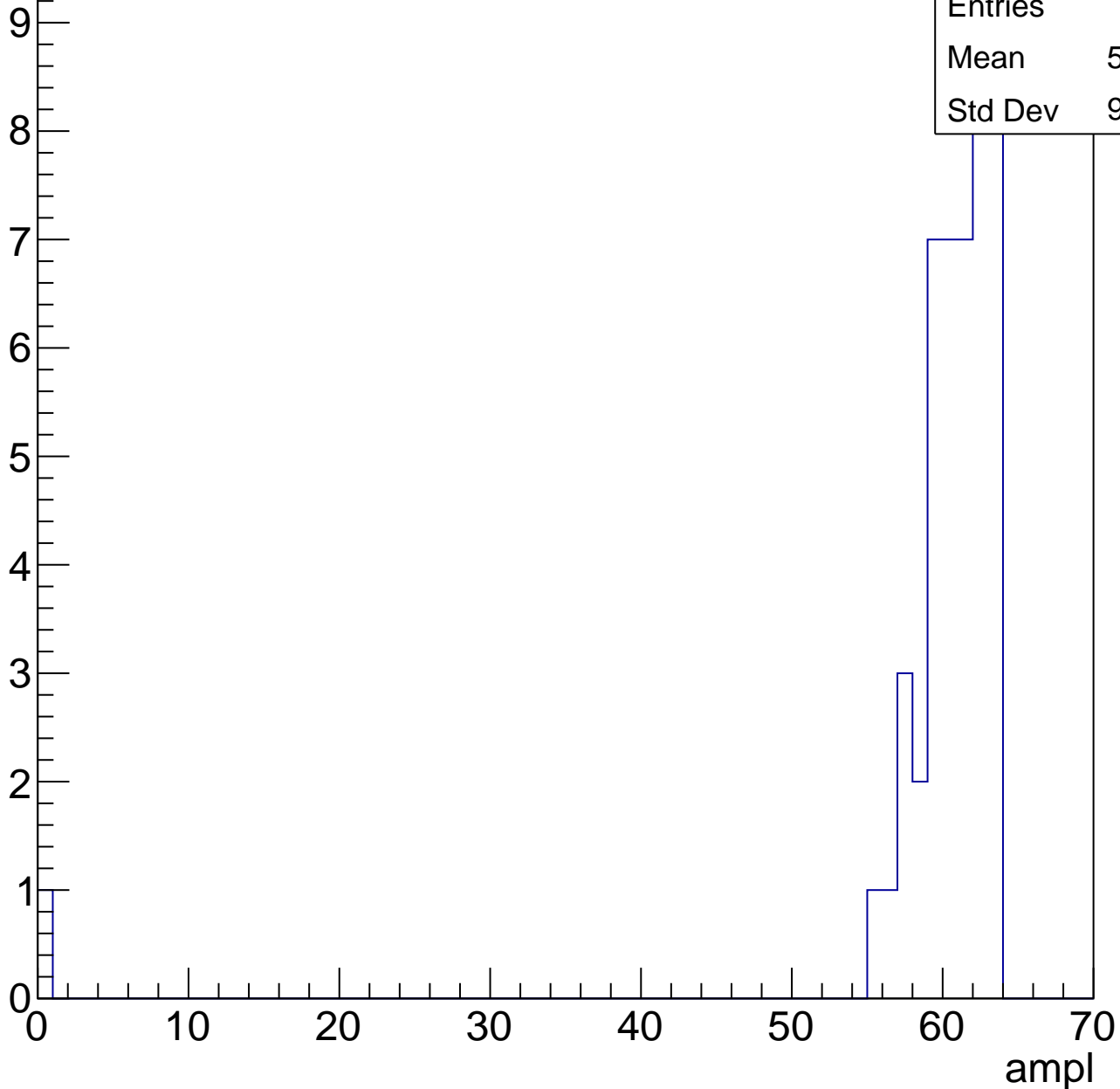


# B1L102S, U20-ch11, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	46
Mean	59.15
Std Dev	9.053



# B1L102S, U20-ch11, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

2

Mean

62

Std Dev

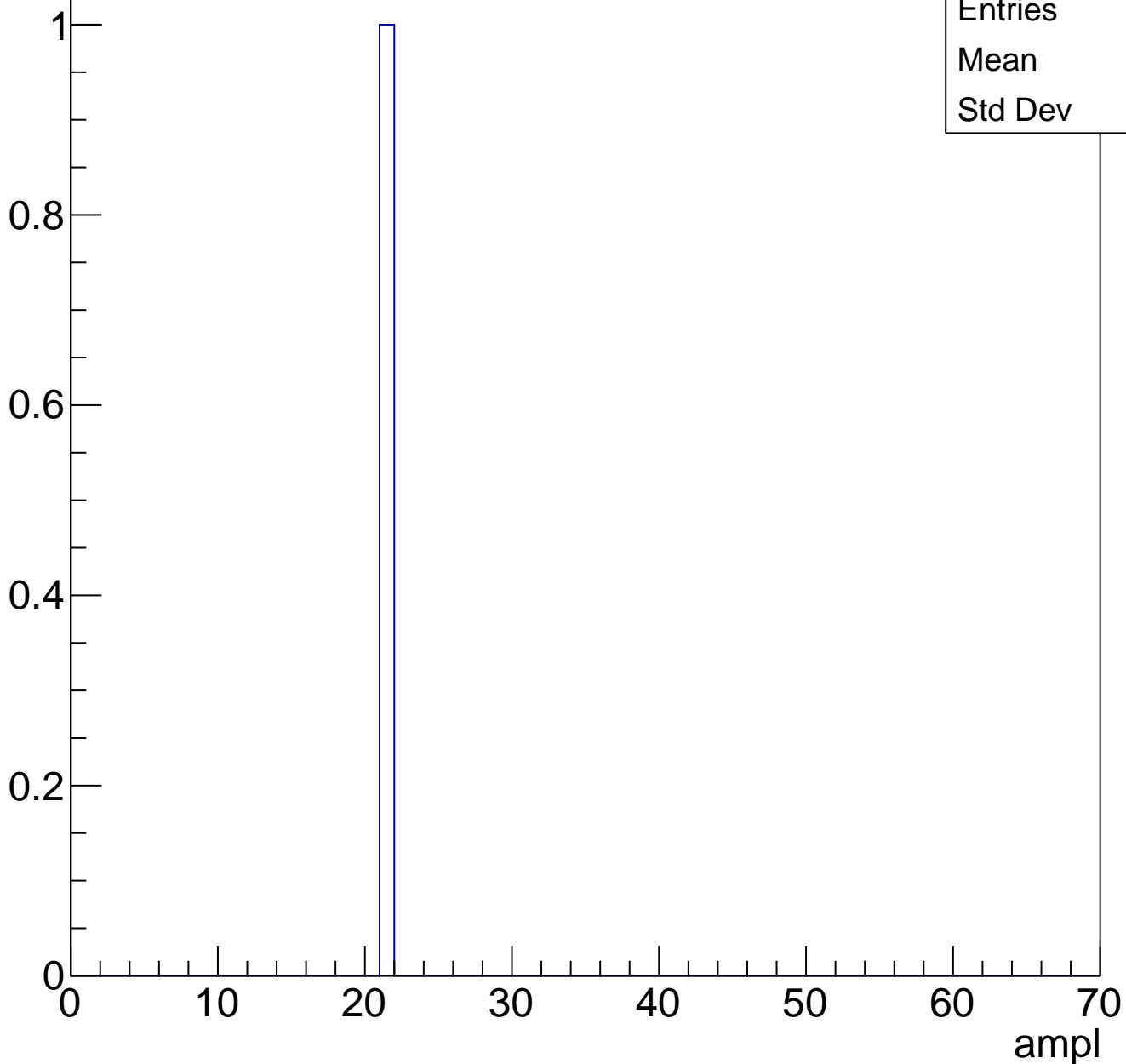
1



# B1L102S, U20-ch11, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch12, adc0

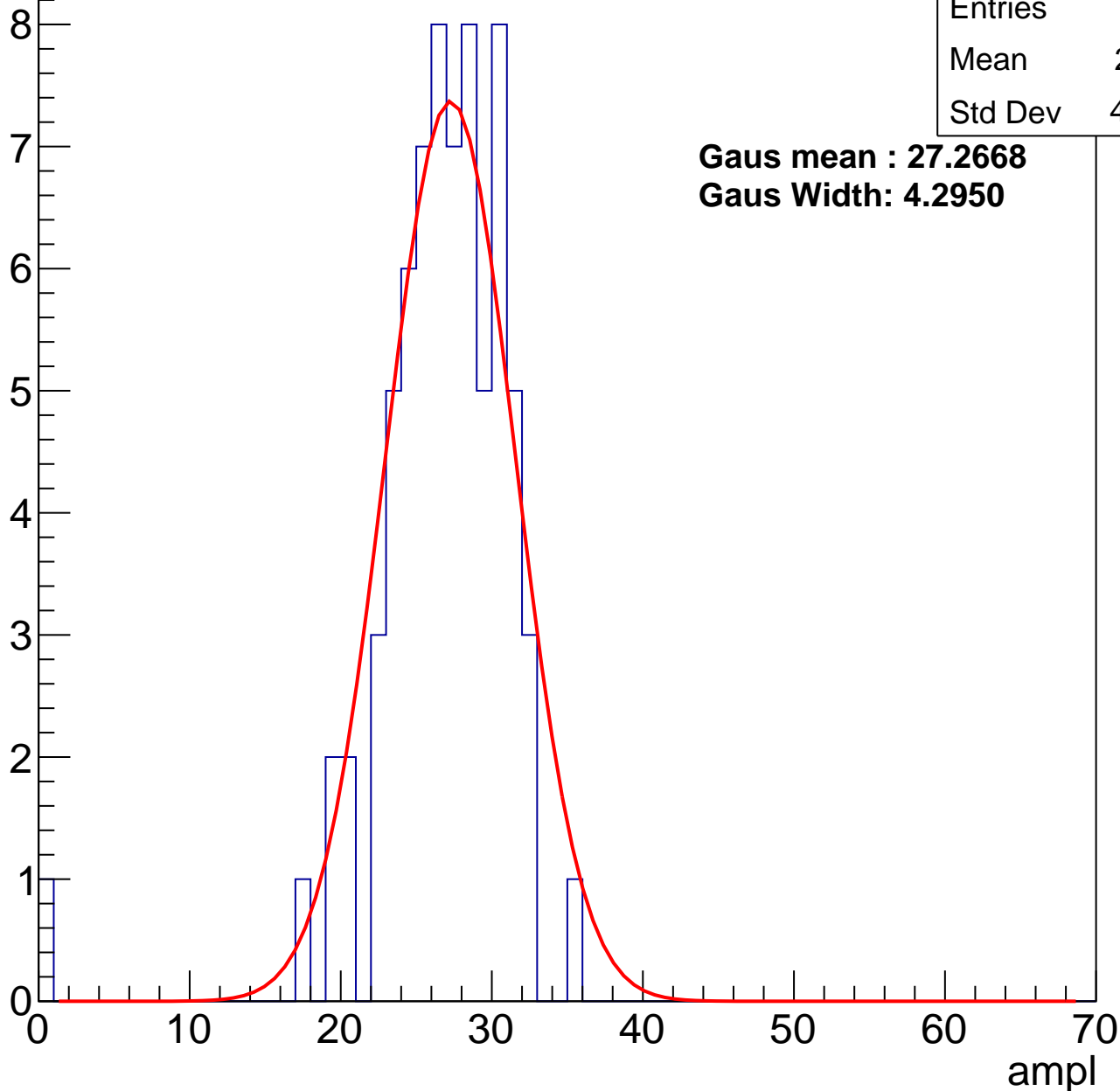
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	26.21
Std Dev	4.675

**Gaus mean : 27.2668**

**Gaus Width: 4.2950**



# B1L102S, U20-ch12, adc1

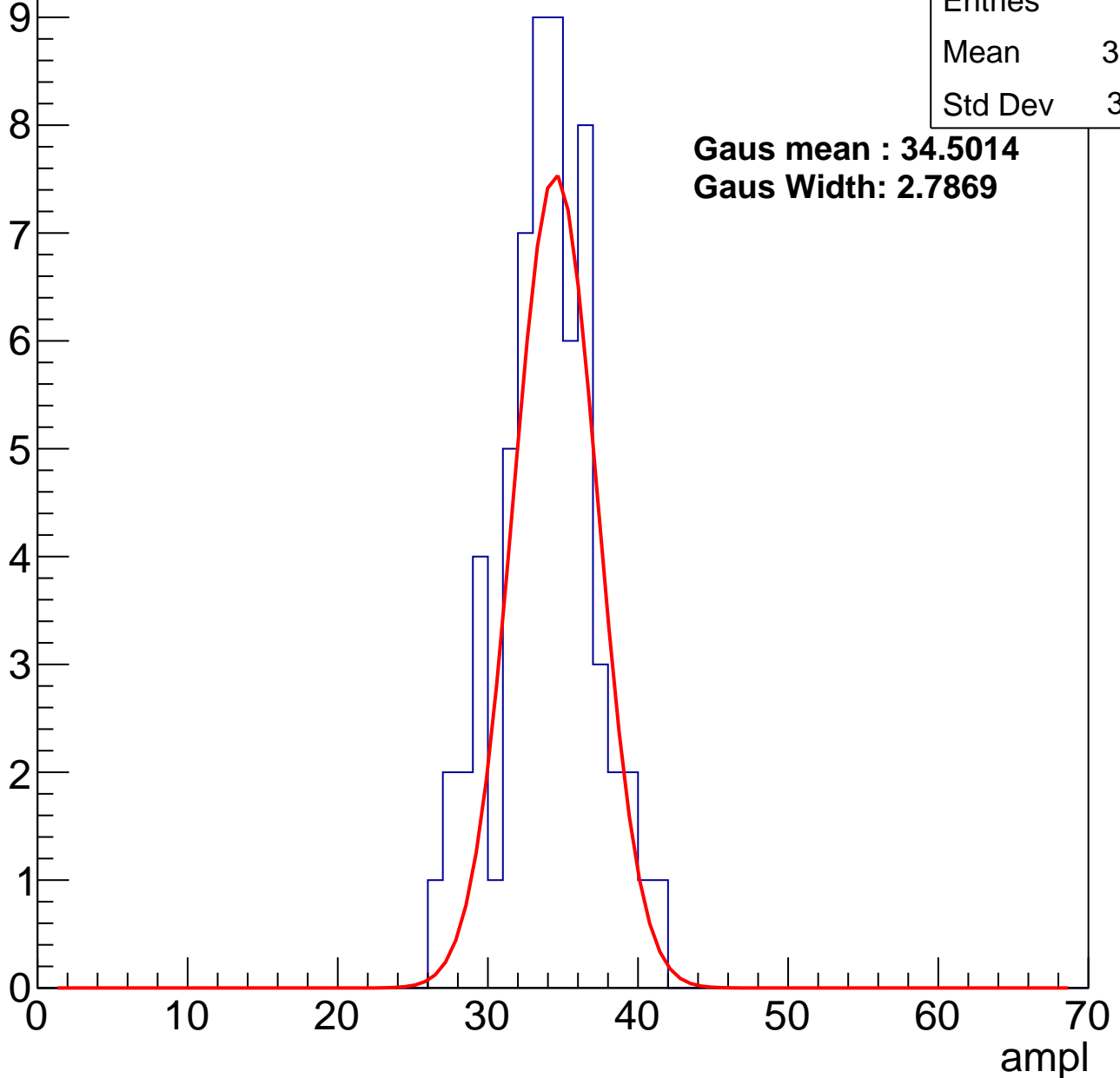
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	33.46
Std Dev	3.201

**Gaus mean : 34.5014**

**Gaus Width: 2.7869**



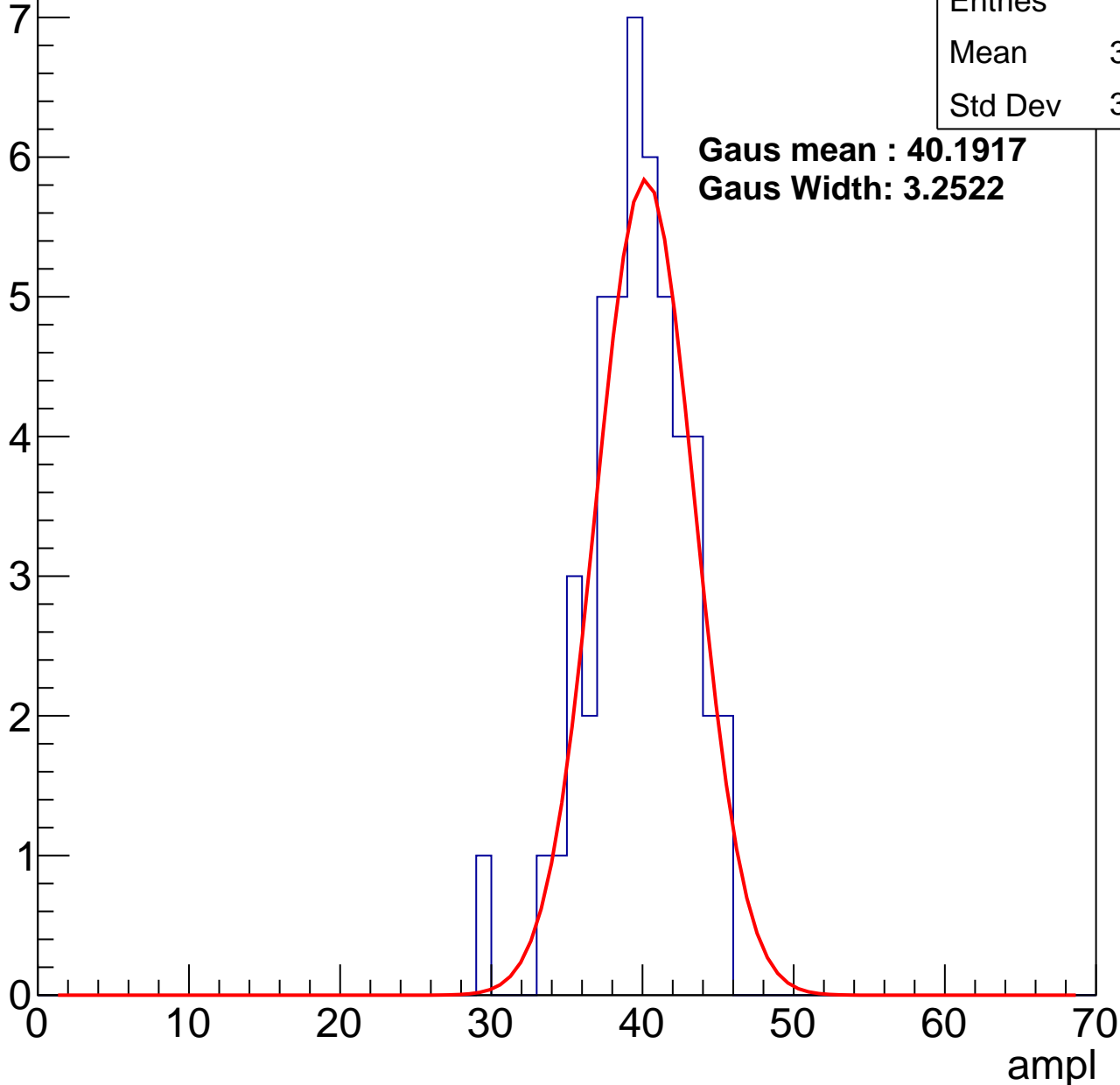
# B1L102S, U20-ch12, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	48
Mean	39.25
Std Dev	3.218

**Gaus mean : 40.1917**  
**Gaus Width: 3.2522**



# B1L102S, U20-ch12, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	79
Mean	45.14
Std Dev	3.648

Entry

10

8

6

4

2

0

0

10

20

30

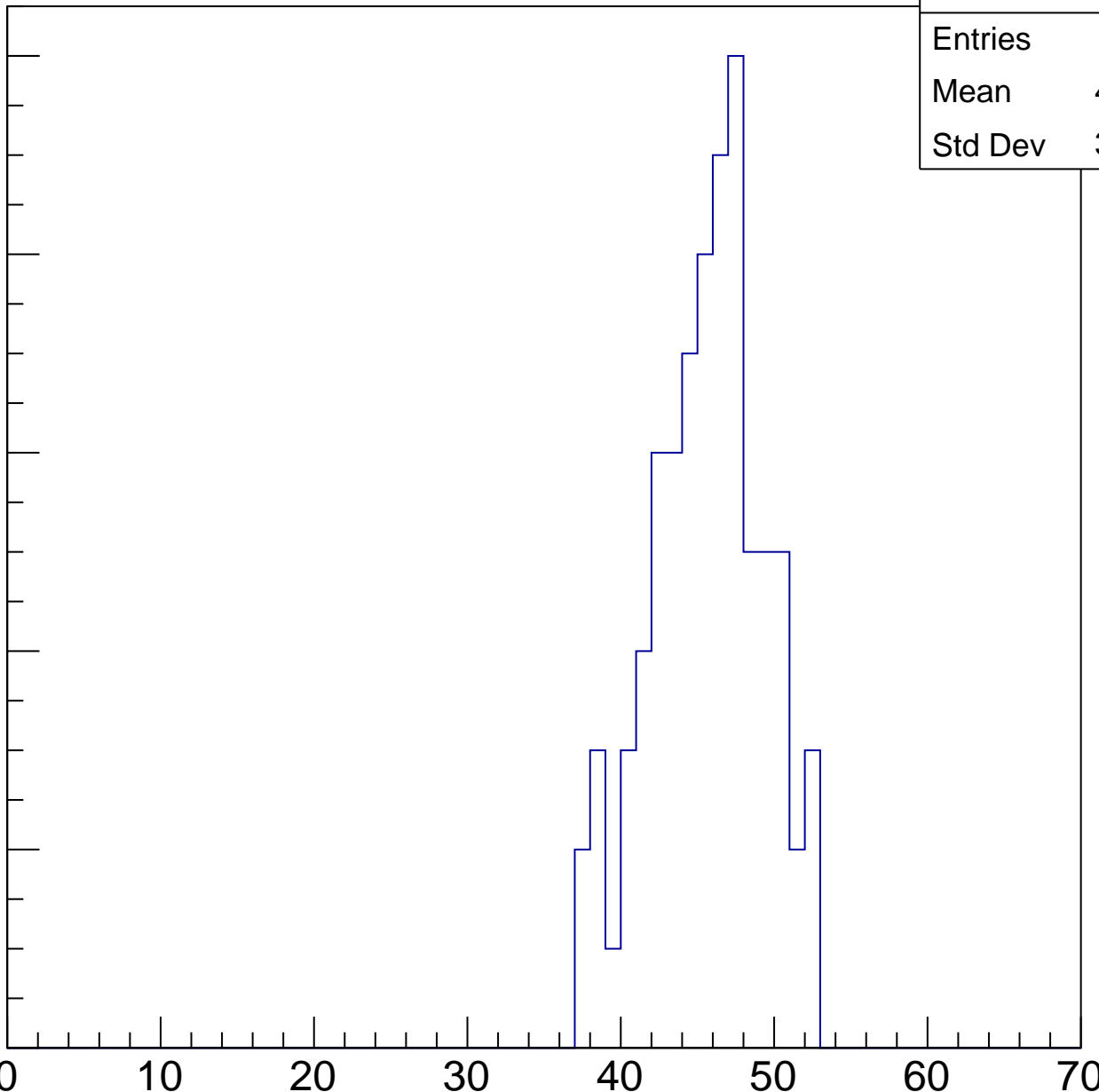
40

50

60

70

ampl

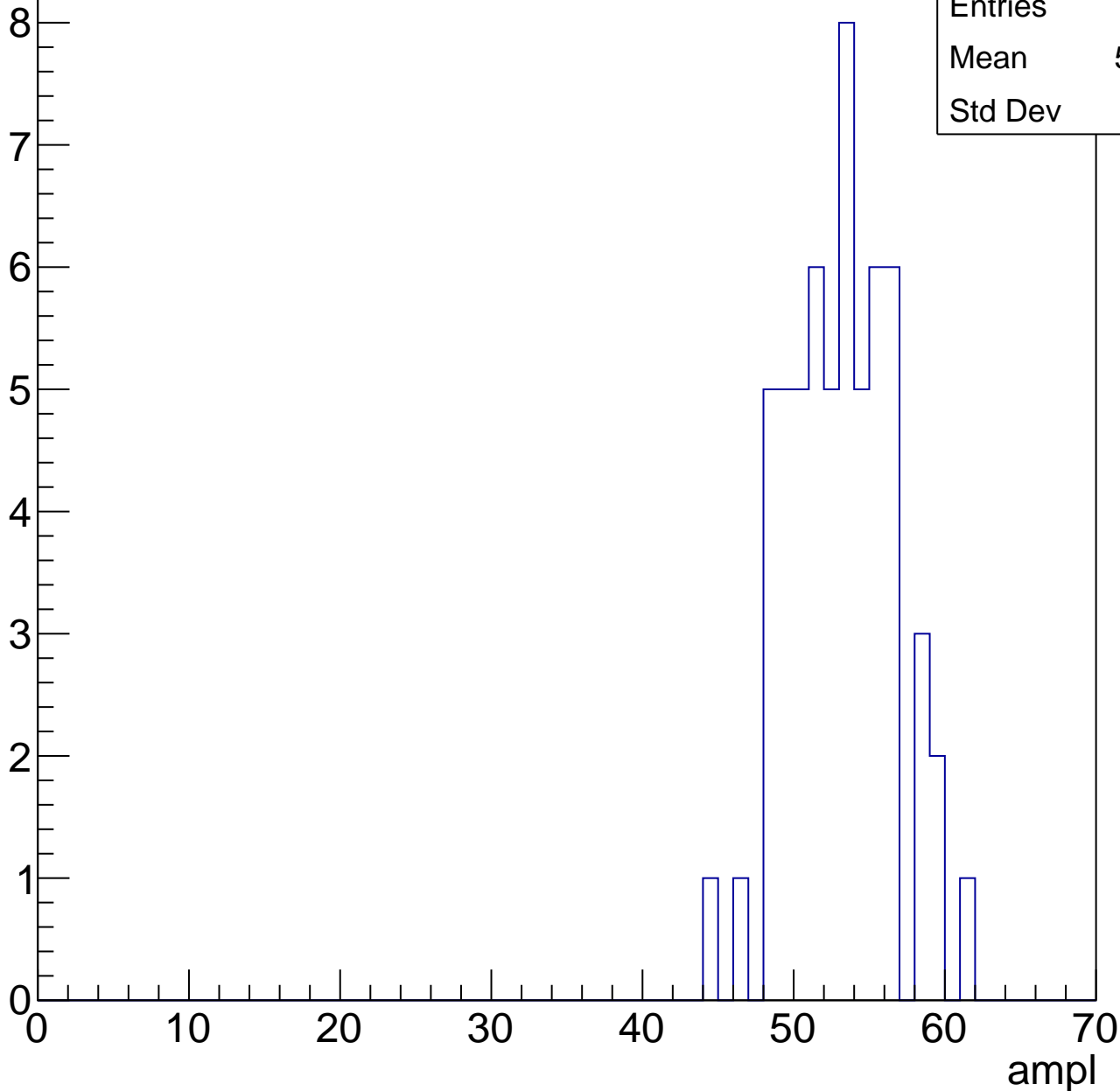


# B1L102S, U20-ch12, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	52.61
Std Dev	3.43



# B1L102S, U20-ch12, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

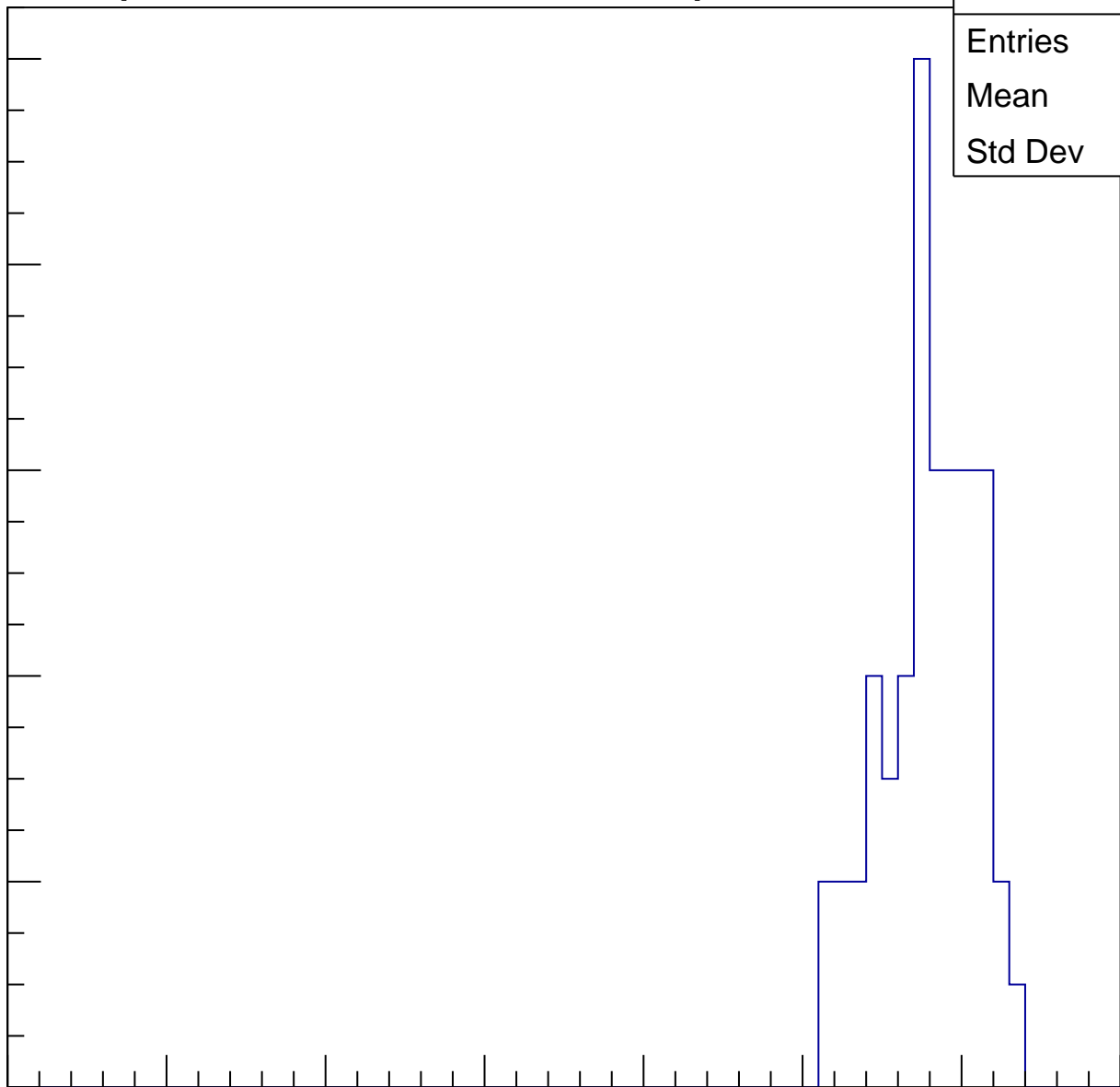
Entries	54
Mean	57.44
Std Dev	2.923

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

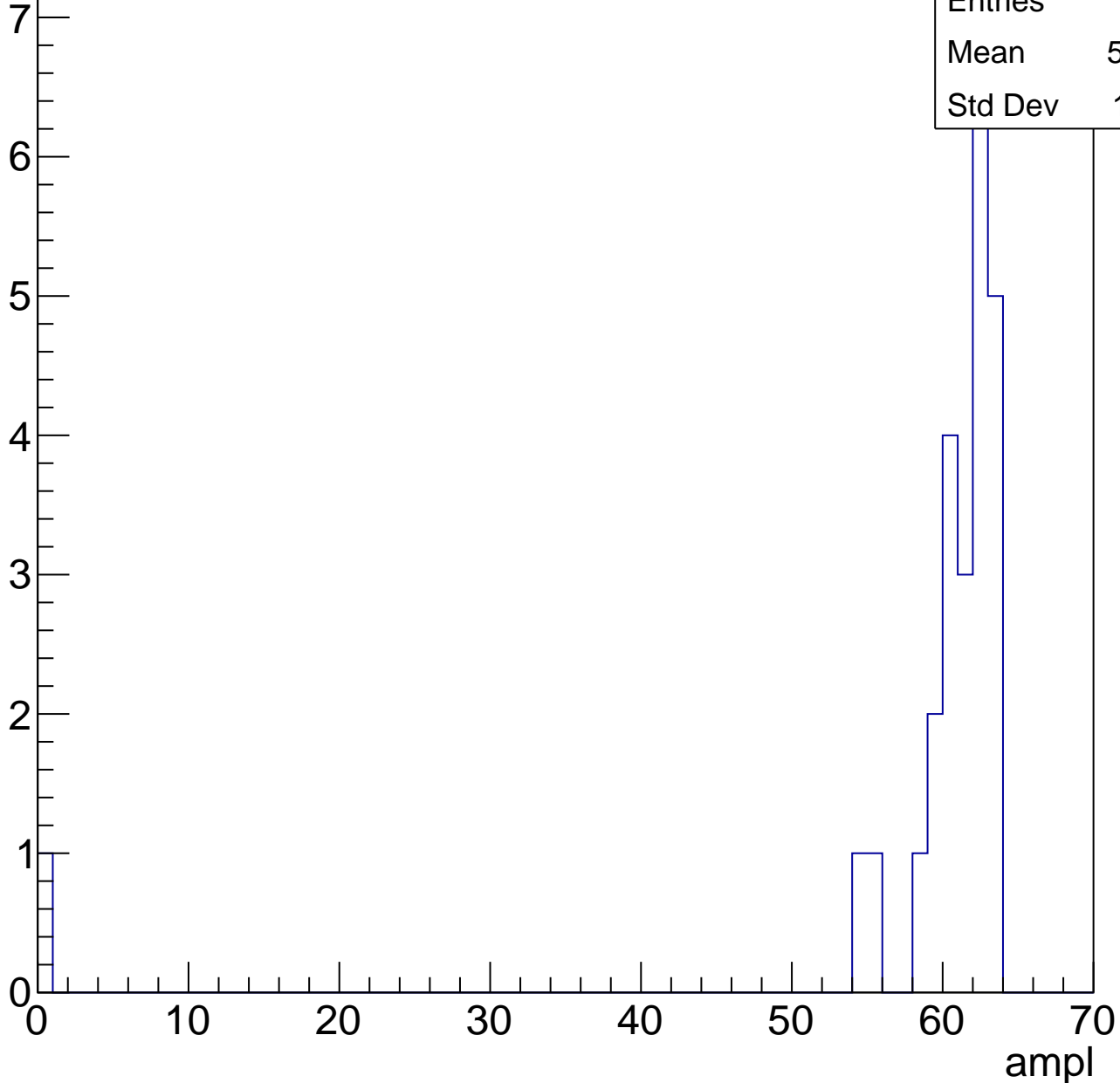


# B1L102S, U20-ch12, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	25
Mean	58.28
Std Dev	12.11

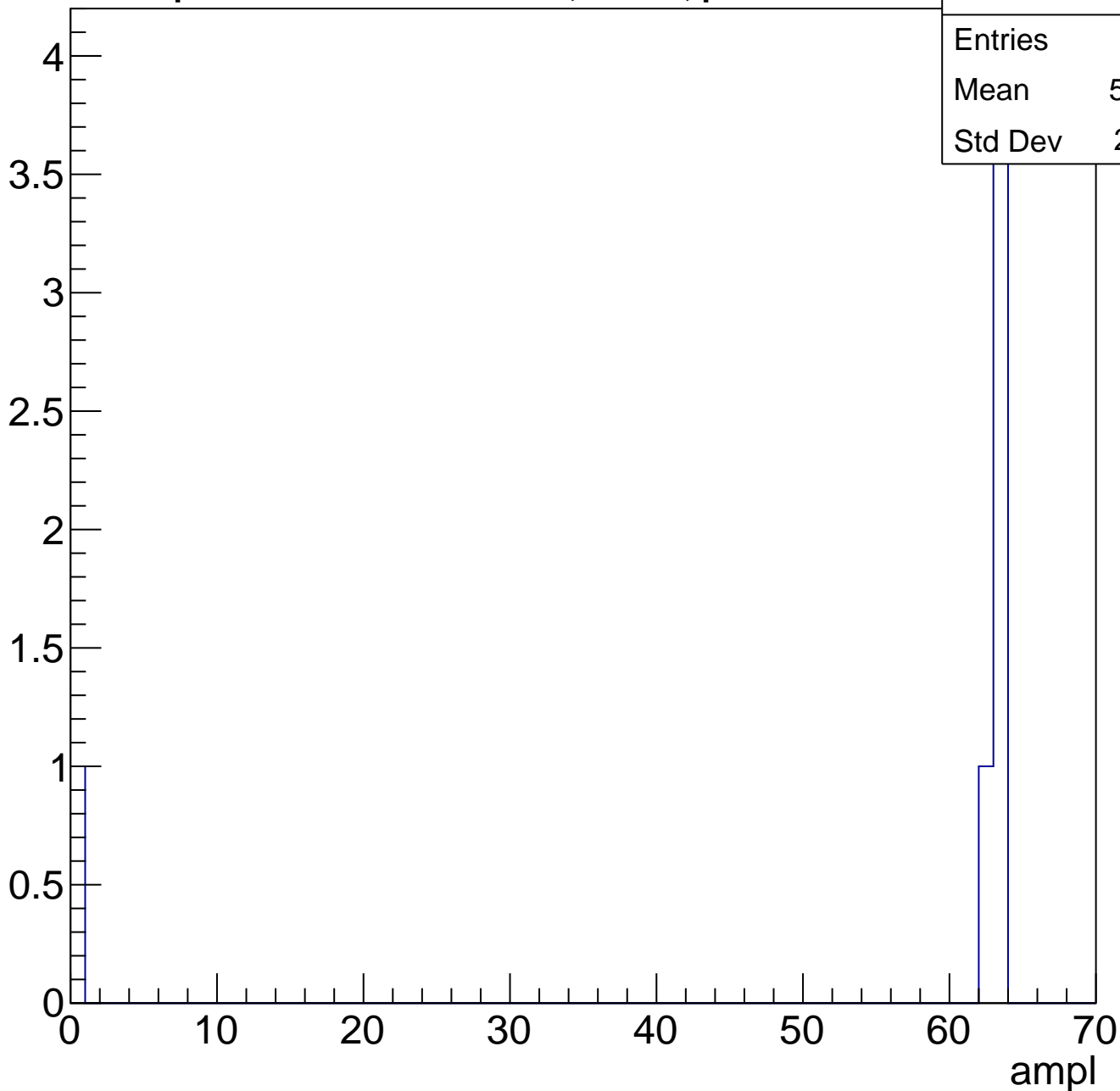




# B1L102S, U20-ch12, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch13, adc0

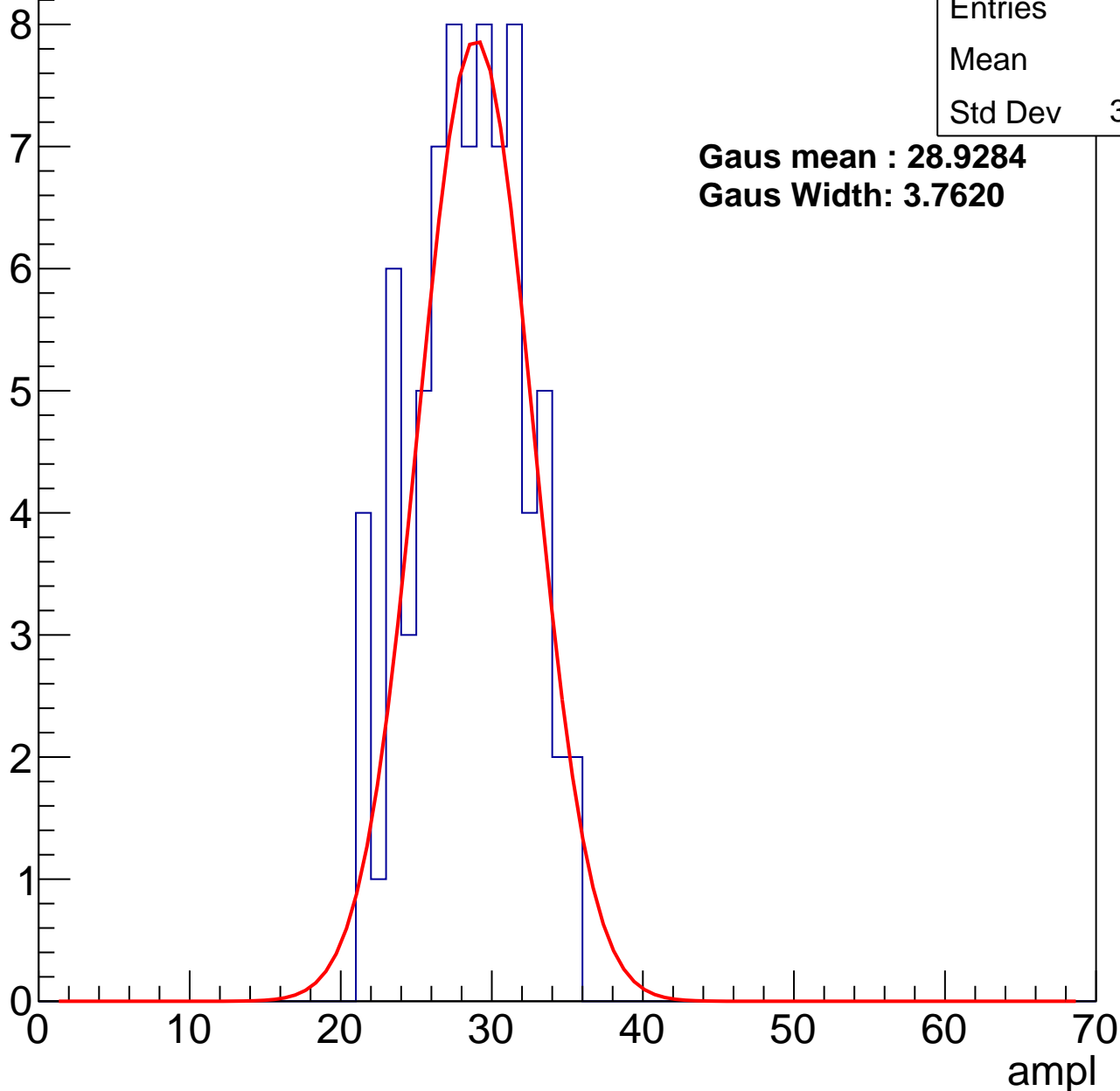
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	28
Std Dev	3.564

**Gaus mean : 28.9284**

**Gaus Width: 3.7620**



# B1L102S, U20-ch13, adc1

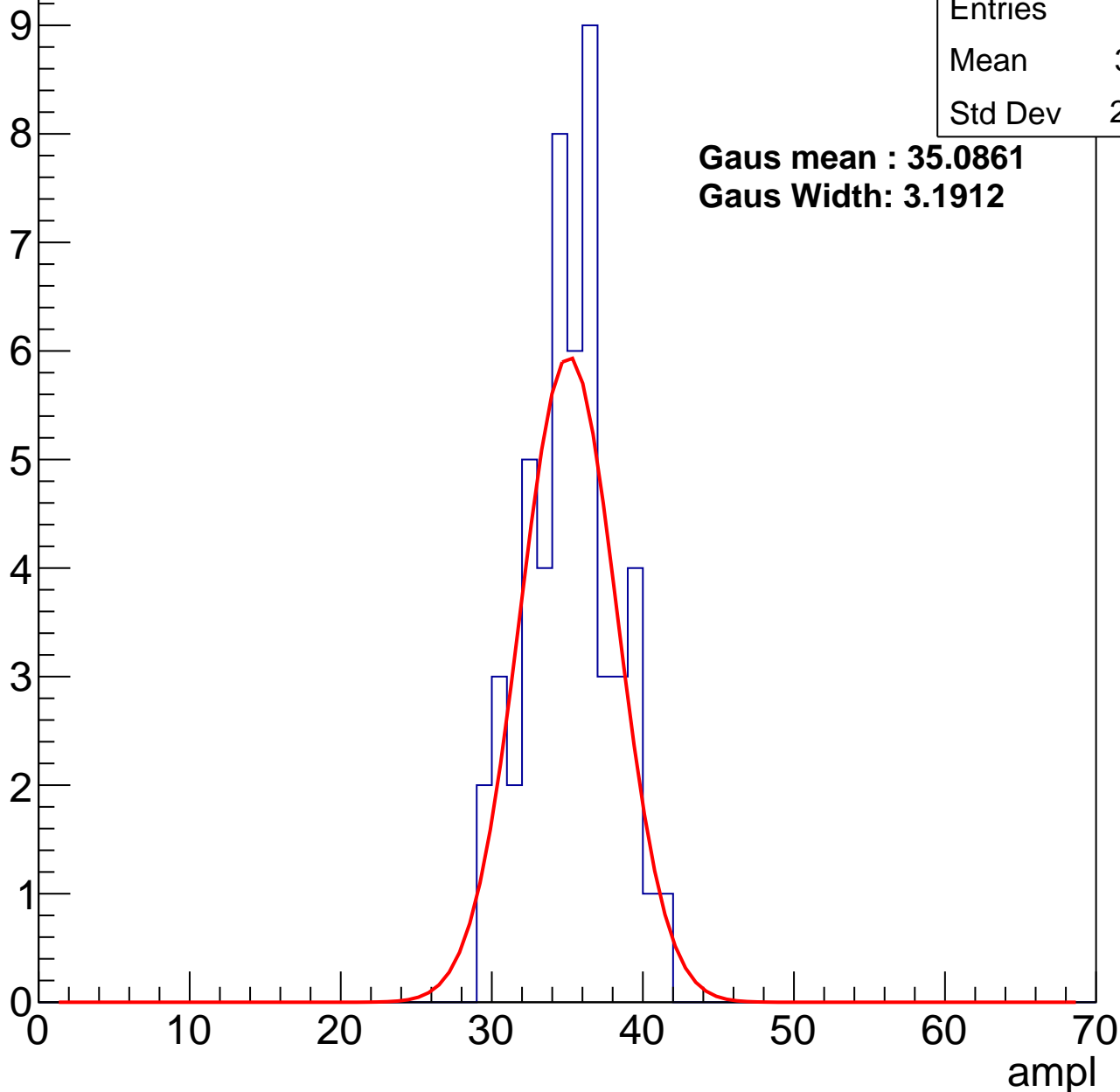
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	34.71
Std Dev	2.858

**Gaus mean : 35.0861**

**Gaus Width: 3.1912**



# B1L102S, U20-ch13, adc2

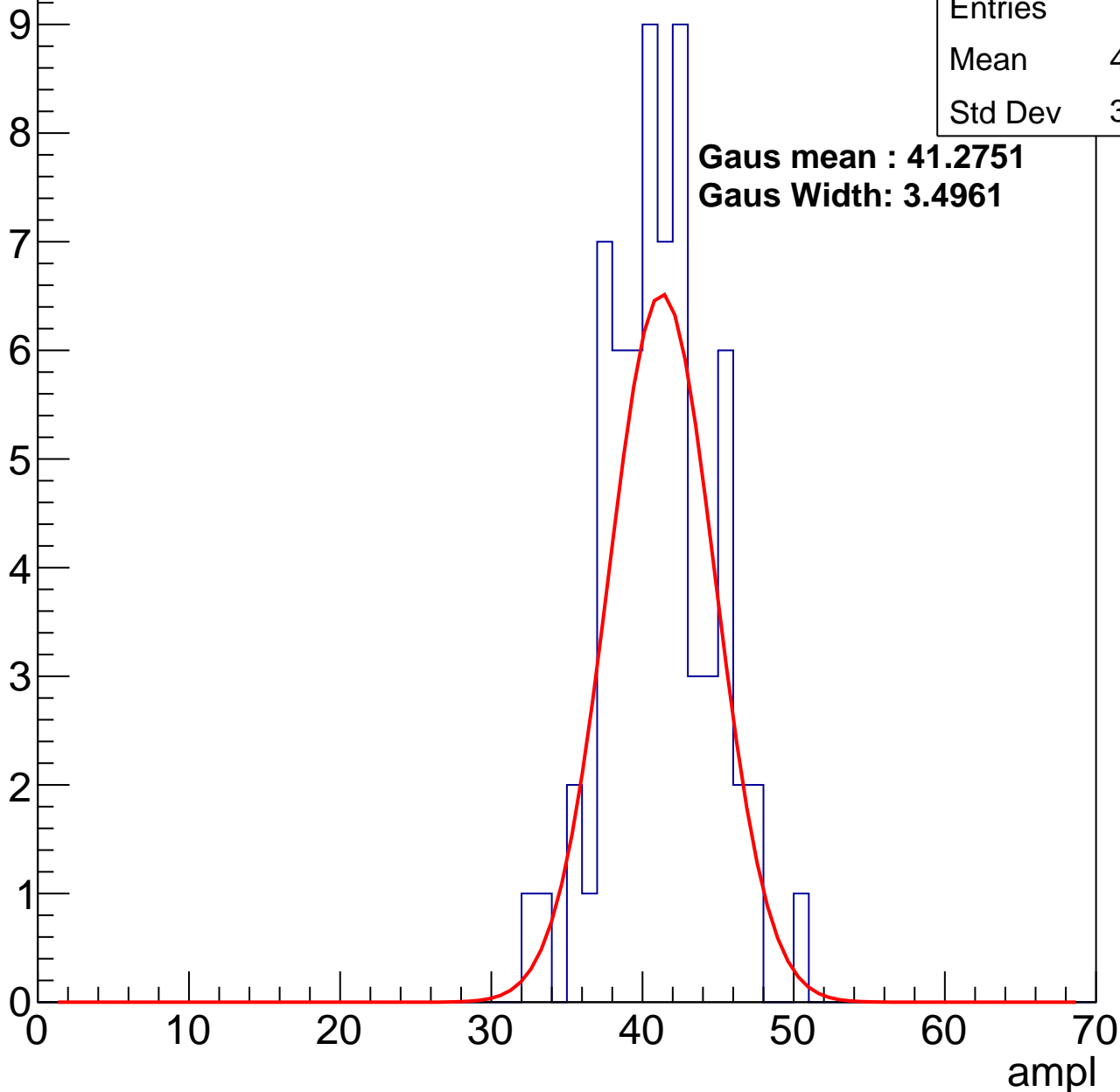
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	40.67
Std Dev	3.439

**Gaus mean : 41.2751**

**Gaus Width: 3.4961**

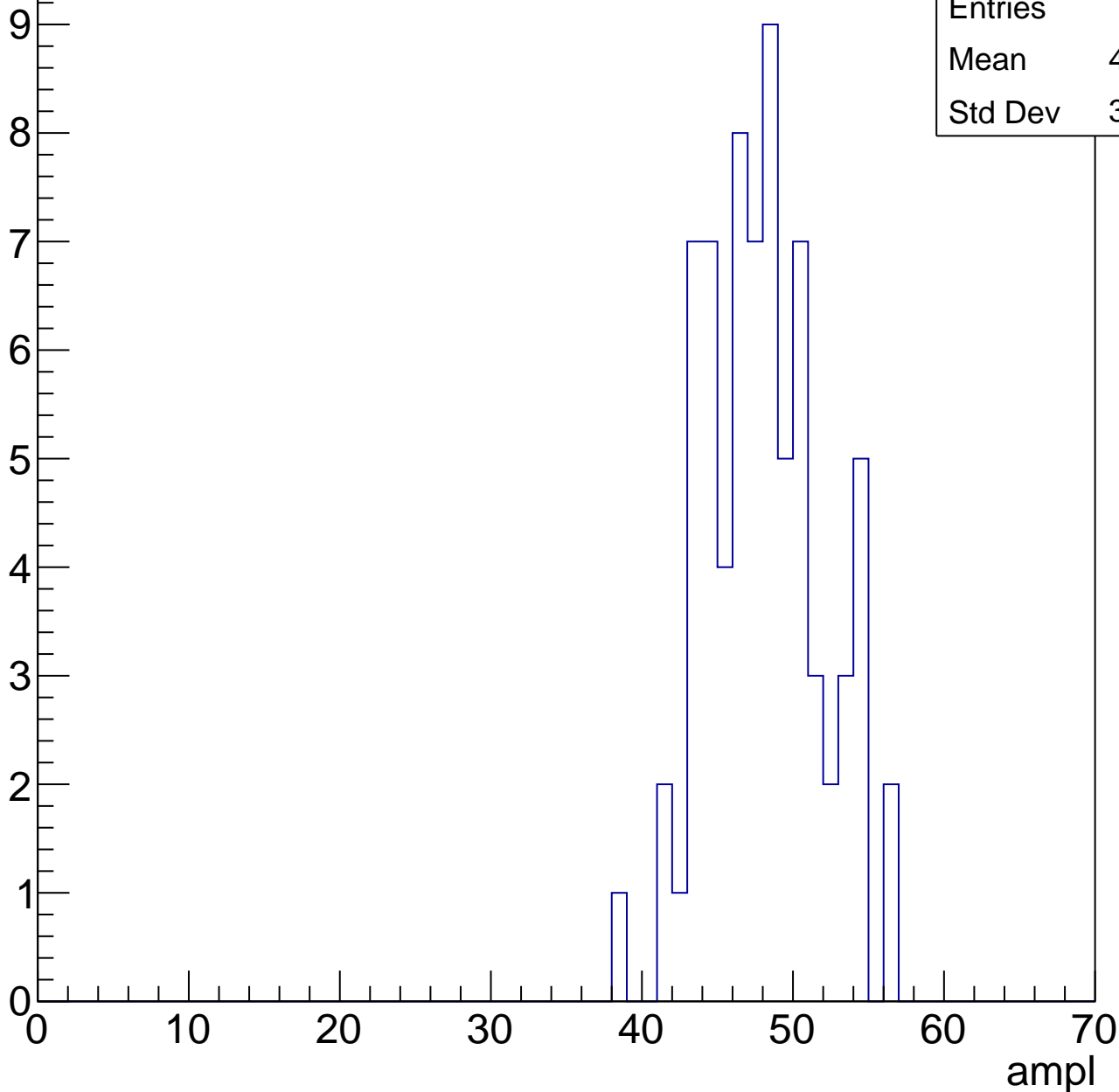


# B1L102S, U20-ch13, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	47.58
Std Dev	3.807

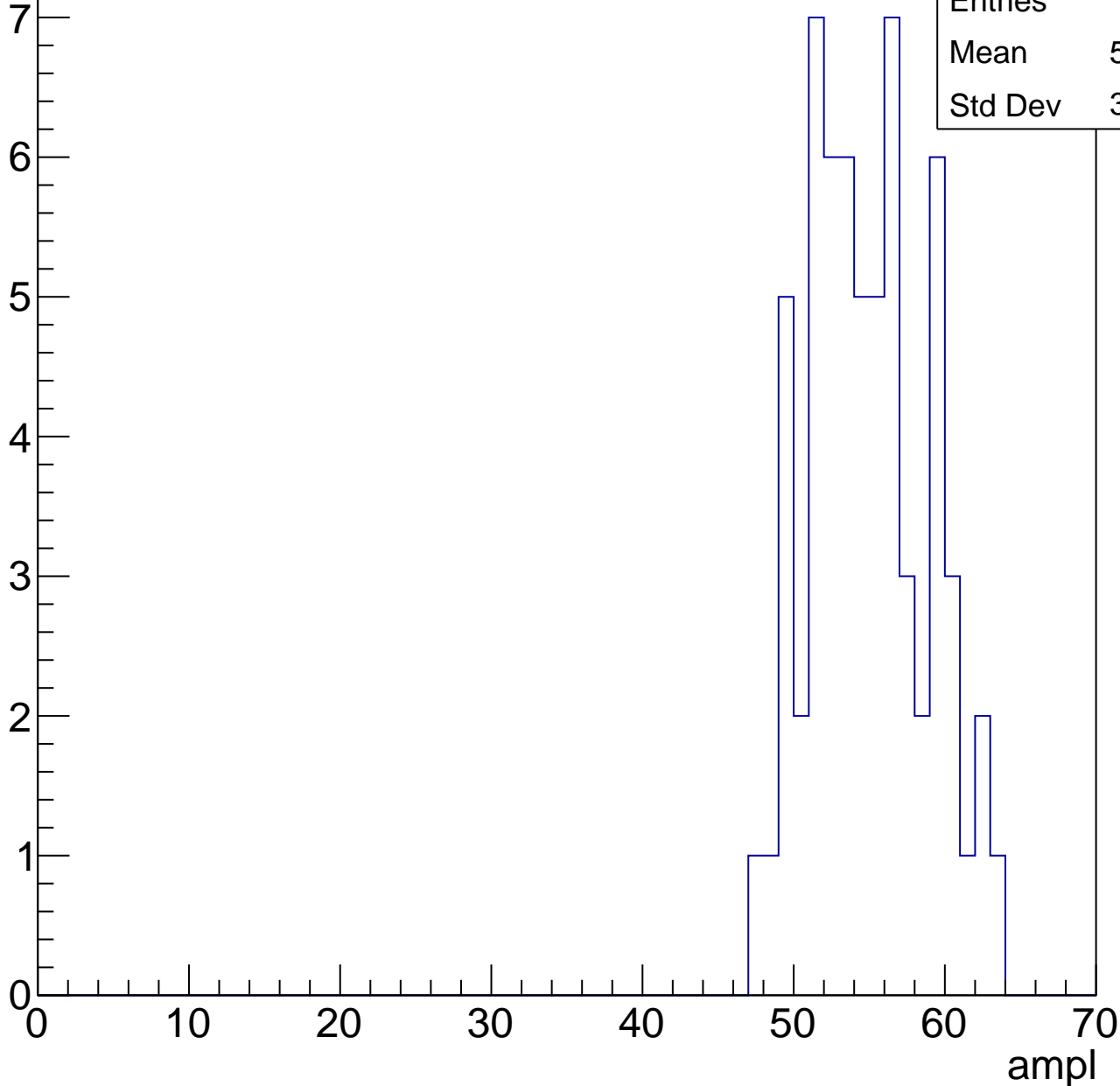


# B1L102S, U20-ch13, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

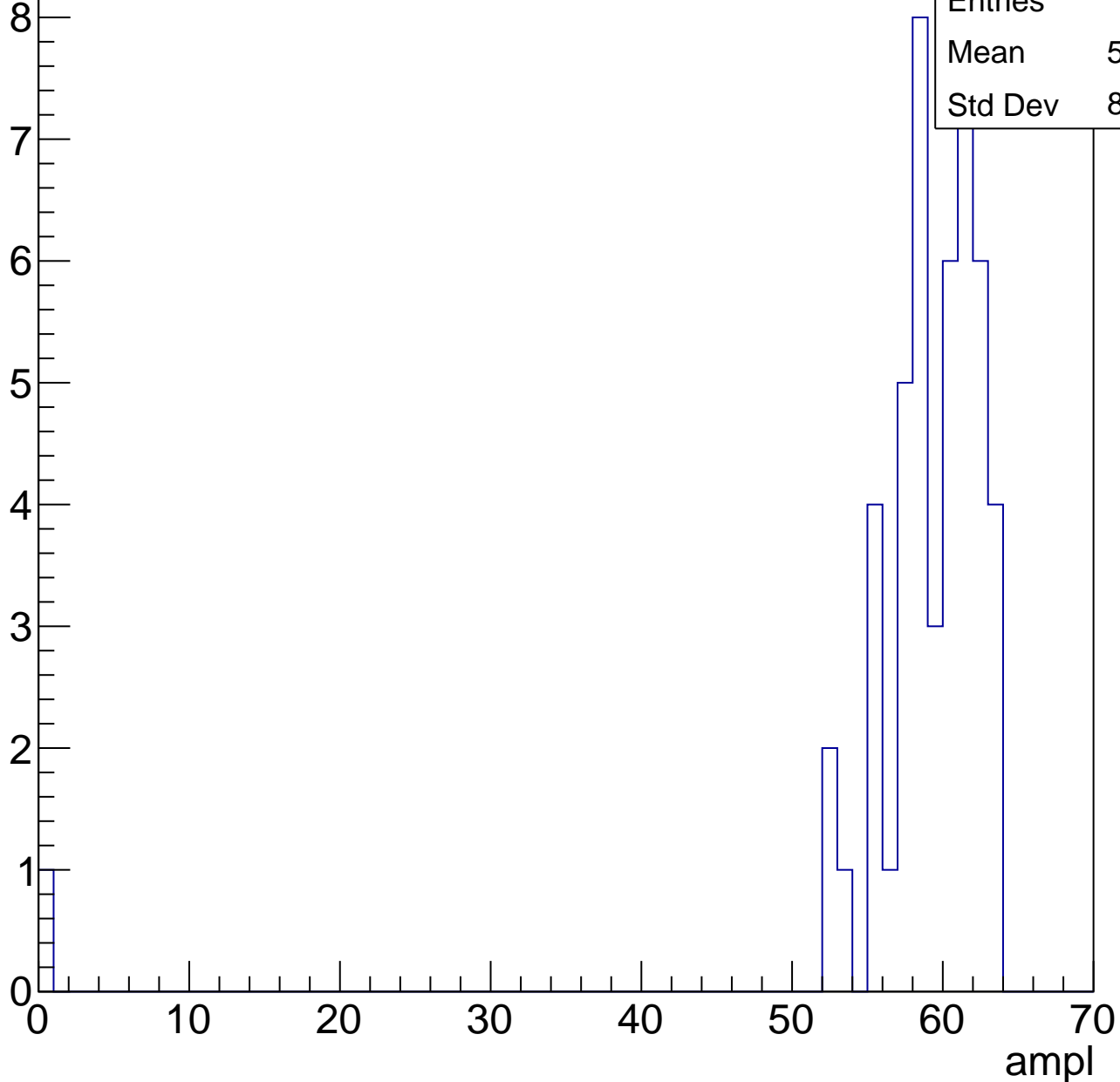
Entries	63
Mean	54.49
Std Dev	3.837



# B1L102S, U20-ch13, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

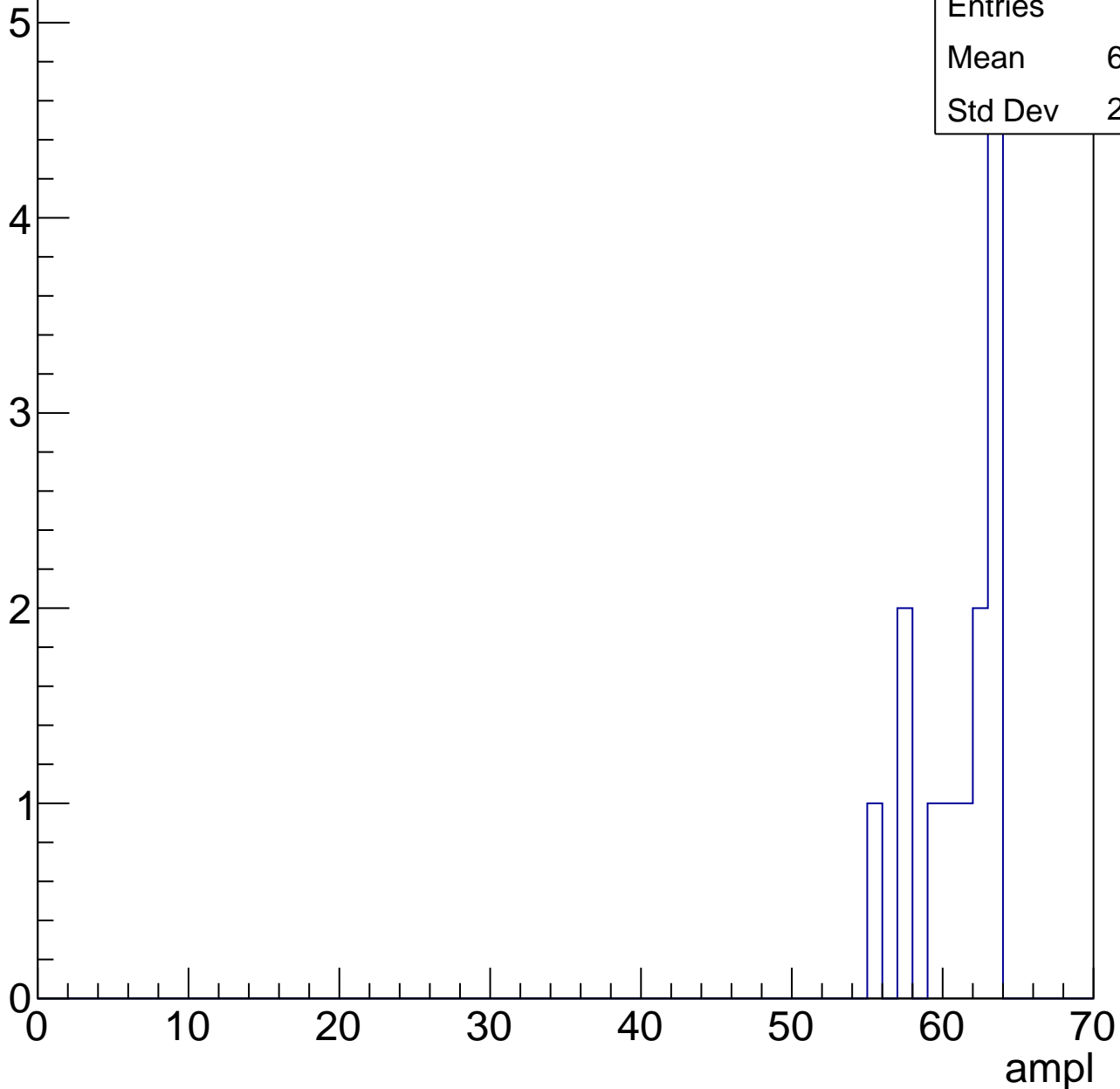


# B1L102S, U20-ch13, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	13
Mean	60.62
Std Dev	2.676

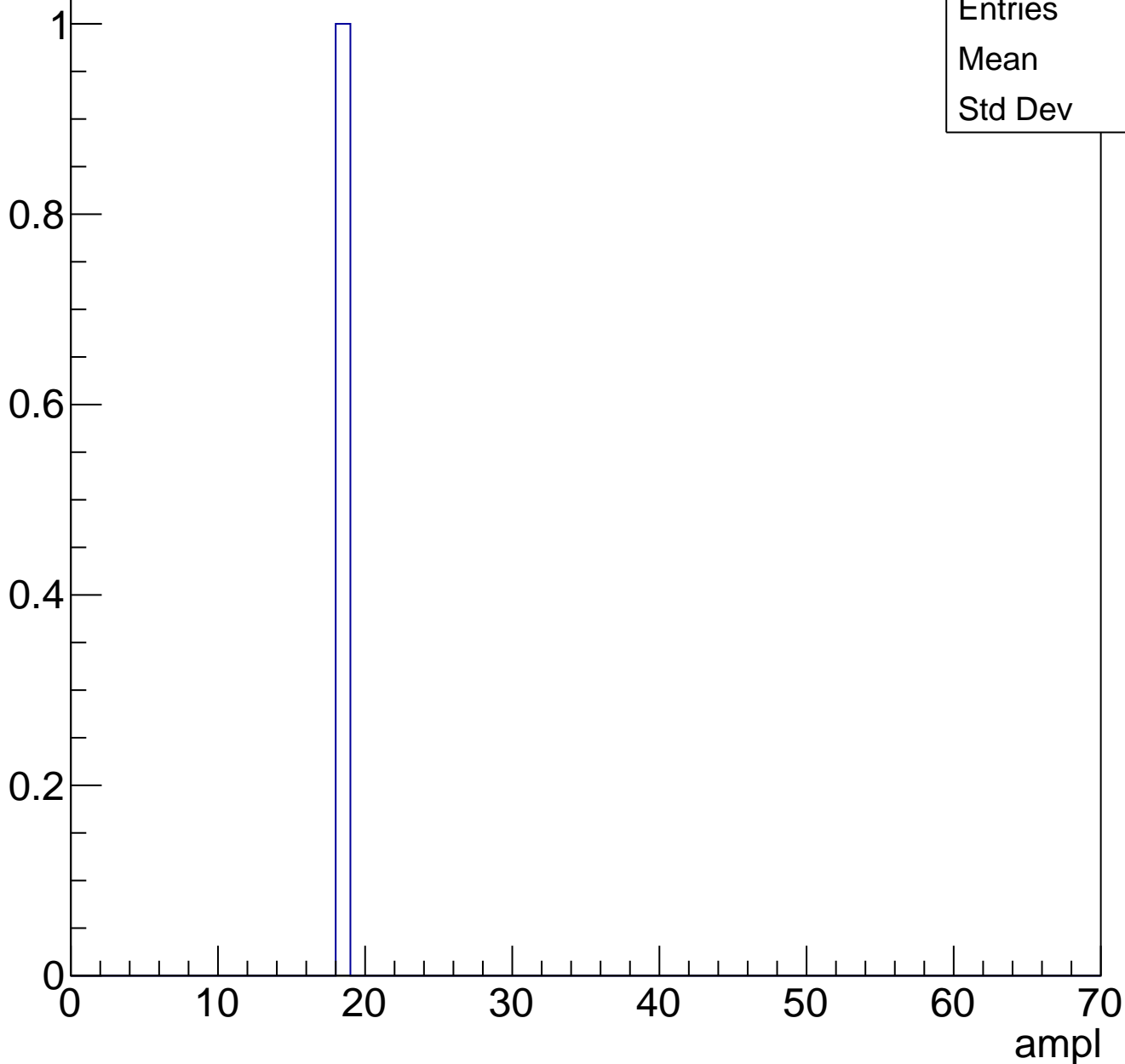




# B1L102S, U20-ch13, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch14, adc0

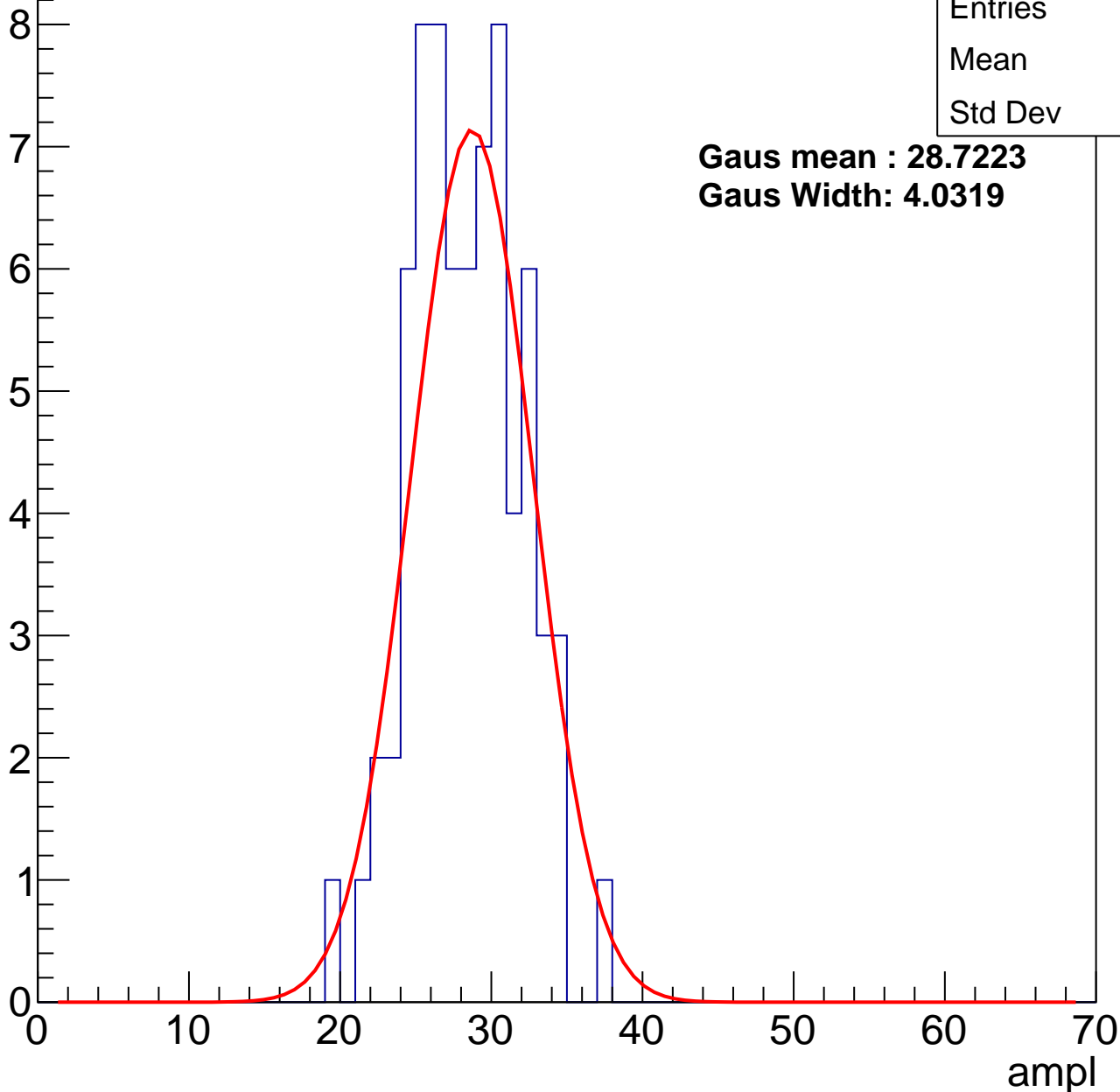
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	27.9
Std Dev	3.52

**Gaus mean : 28.7223**

**Gaus Width: 4.0319**



# B1L102S, U20-ch14, adc1

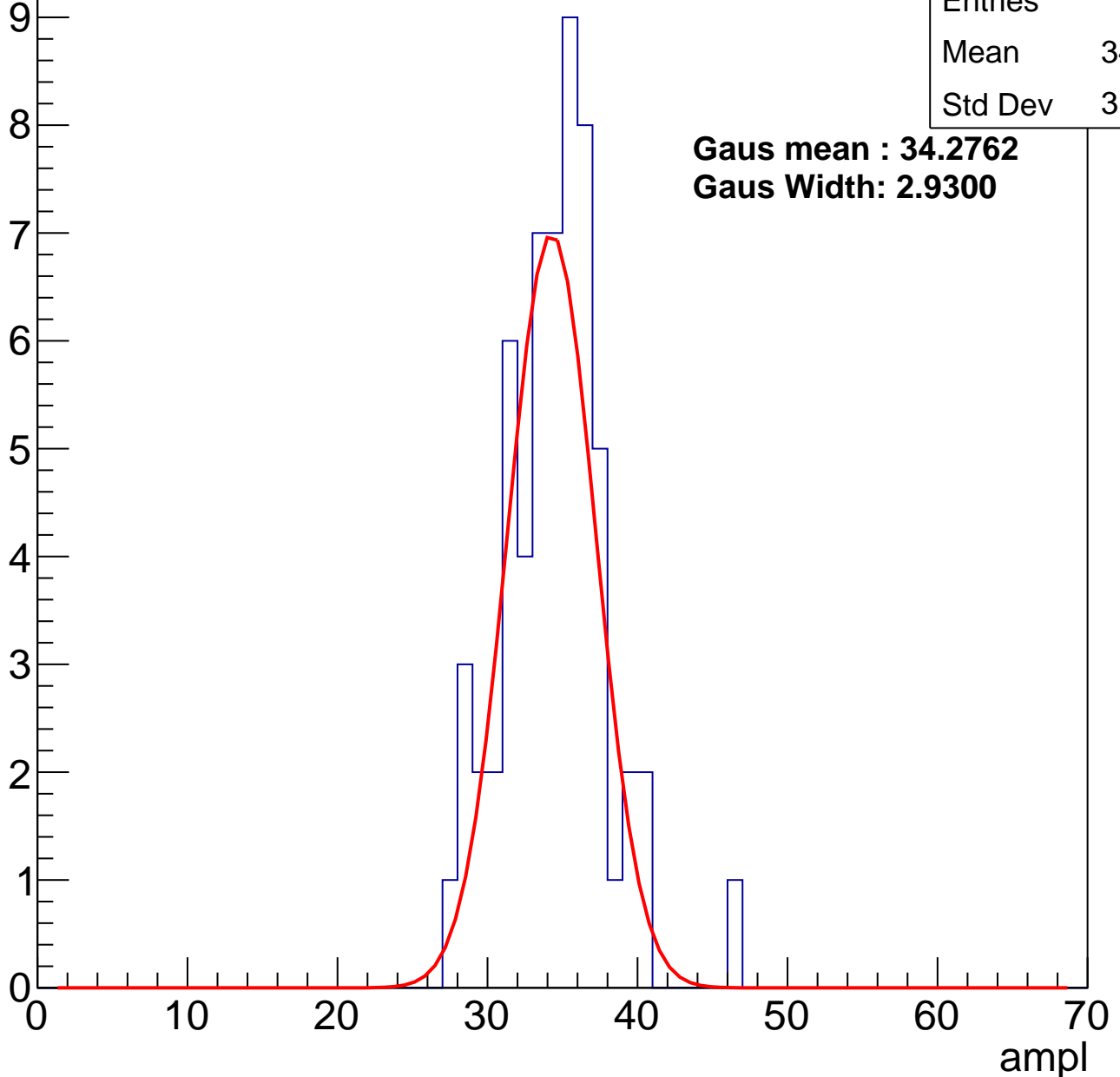
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	34.03
Std Dev	3.376

**Gaus mean : 34.2762**

**Gaus Width: 2.9300**



# B1L102S, U20-ch14, adc2

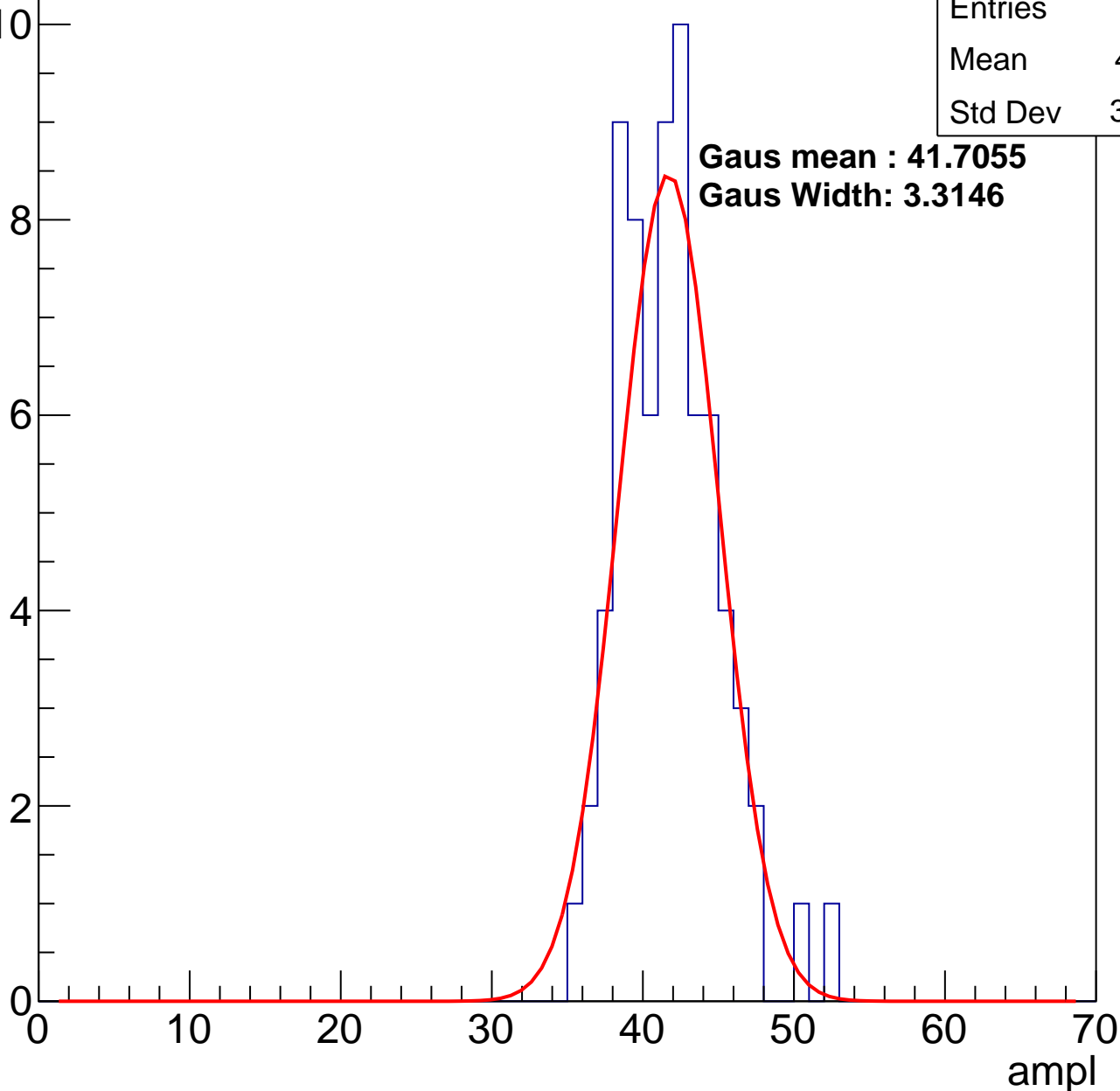
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	41.31
Std Dev	3.256

**Gaus mean : 41.7055**

**Gaus Width: 3.3146**

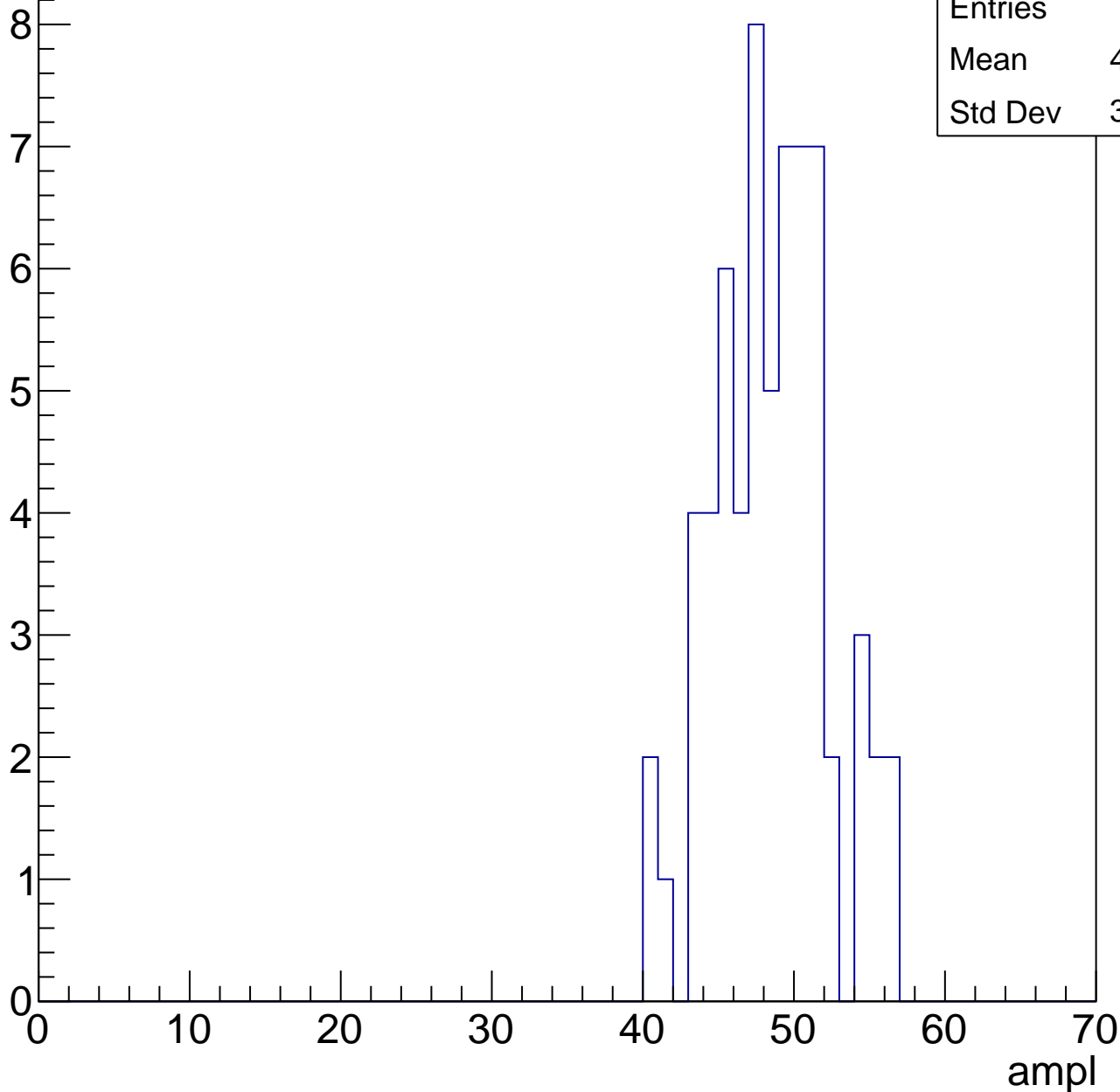


# B1L102S, U20-ch14, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	48.08
Std Dev	3.714

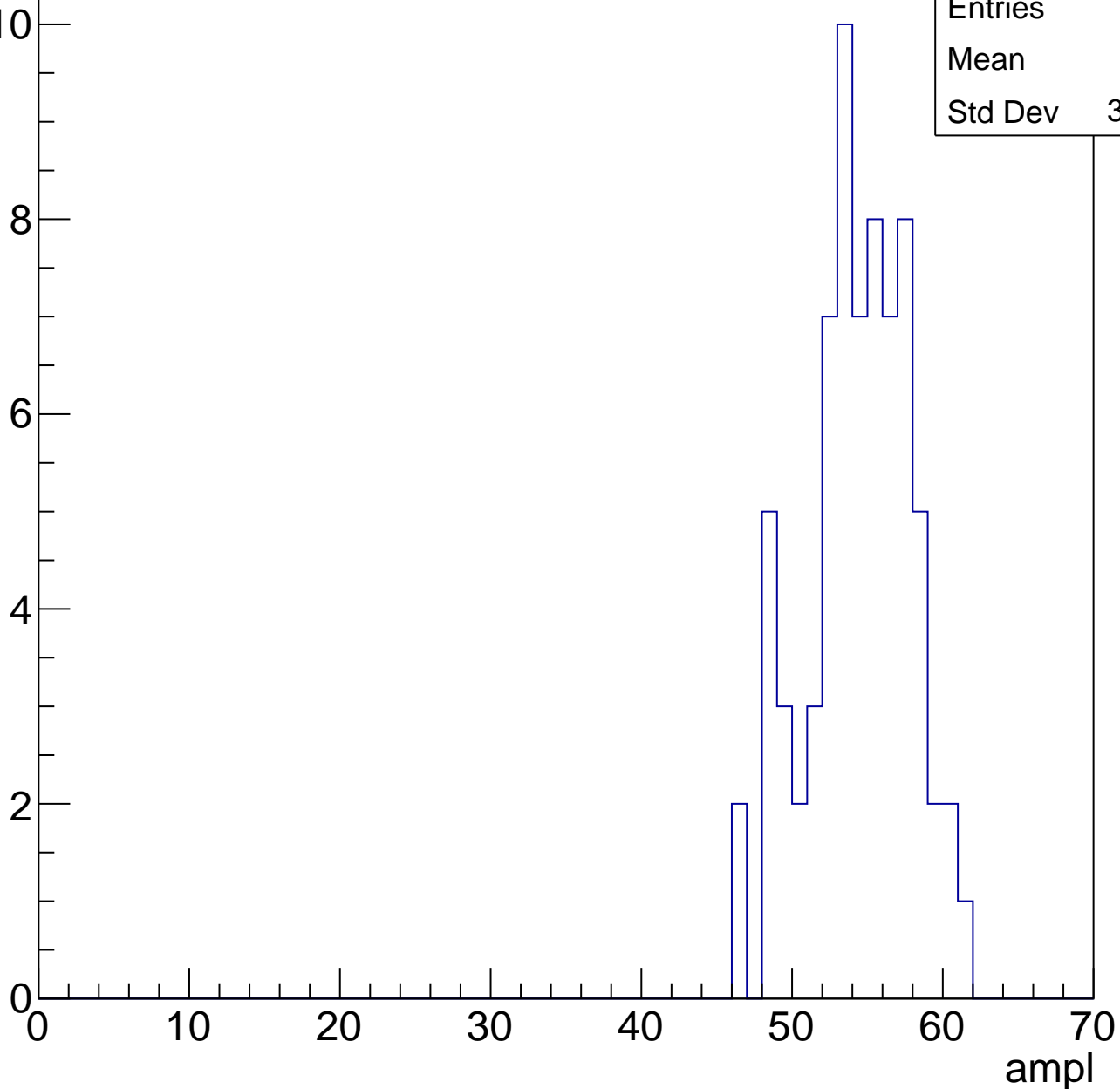


# B1L102S, U20-ch14, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	53.9
Std Dev	3.412

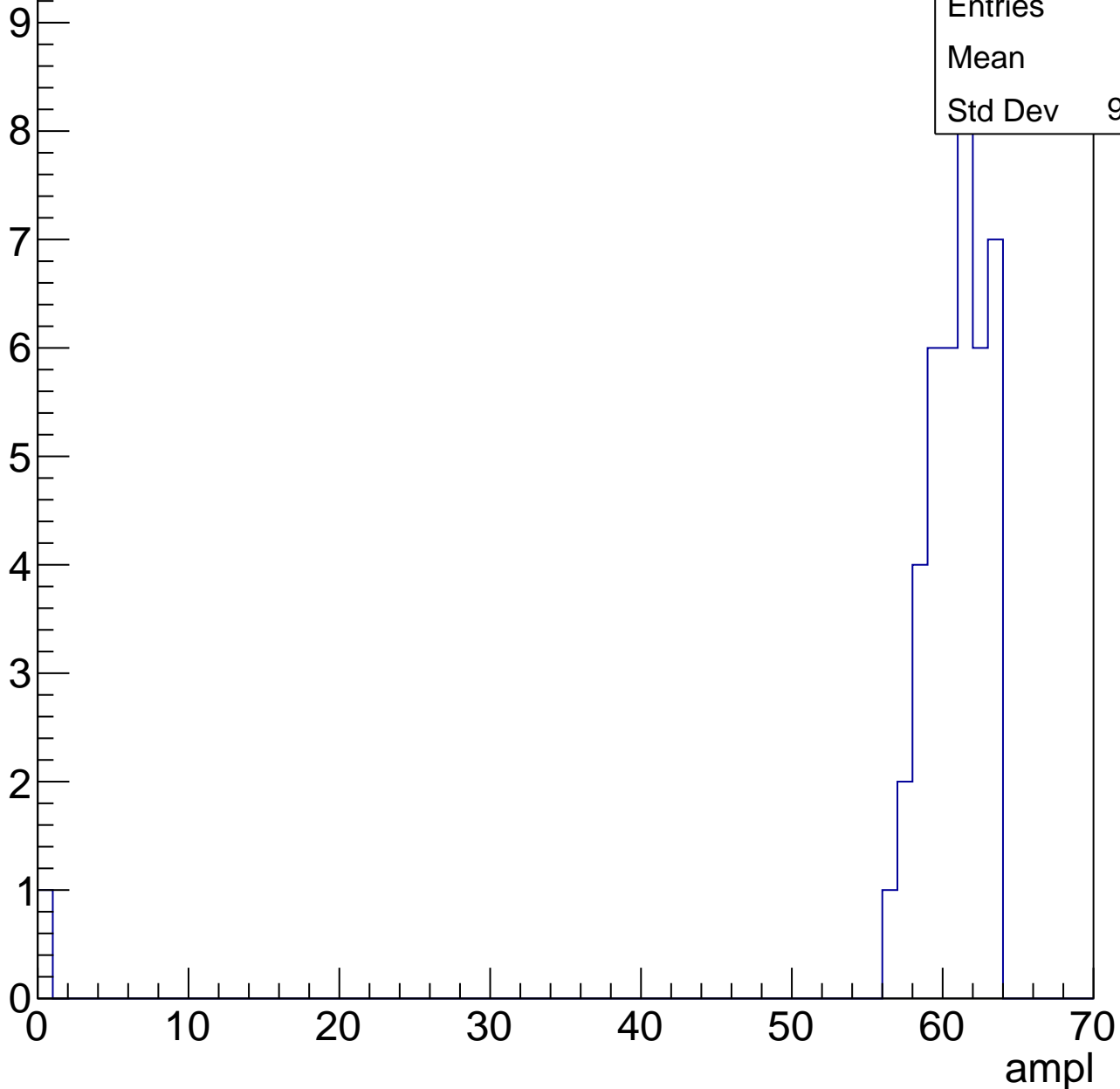


# B1L102S, U20-ch14, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

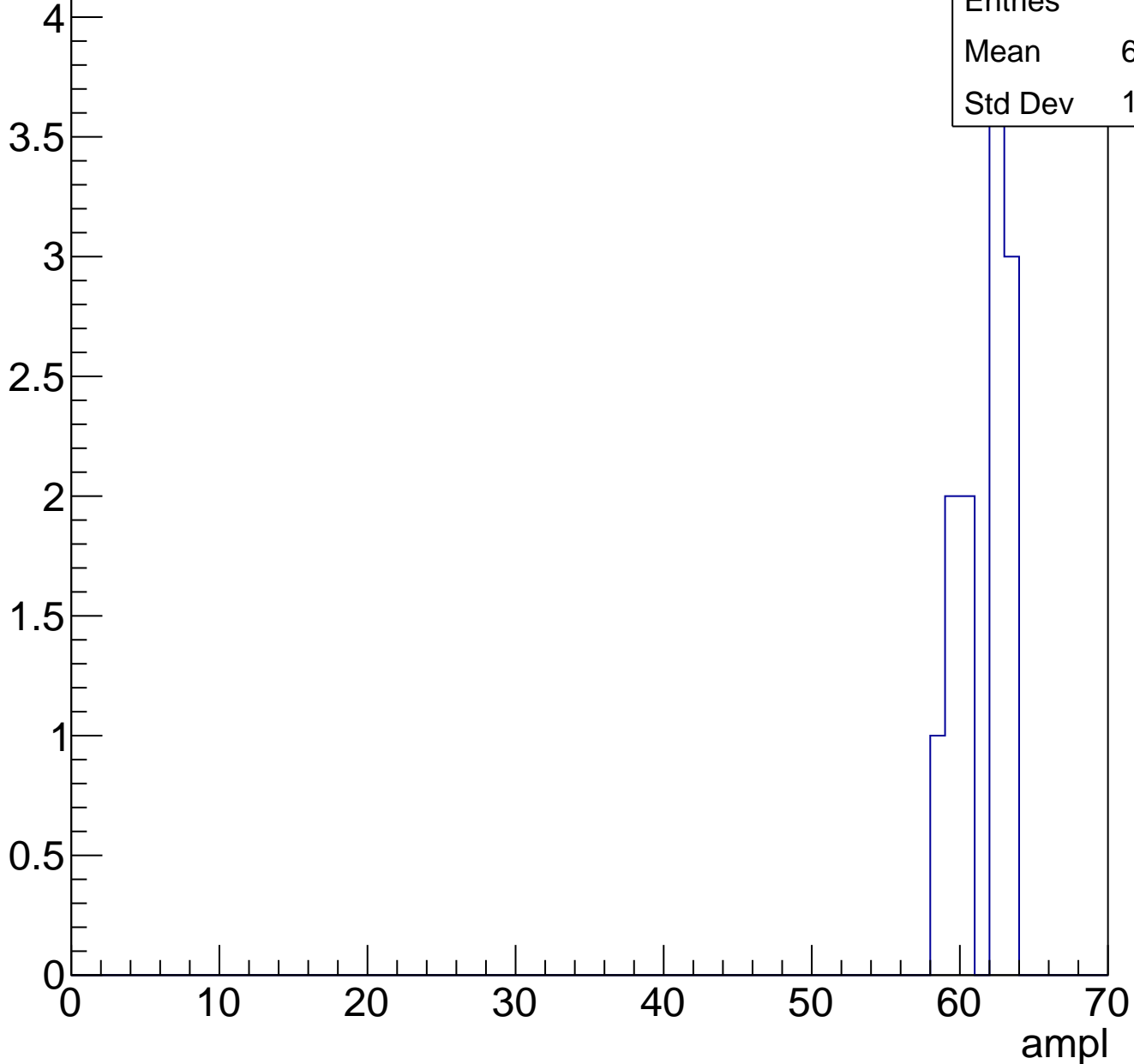
Entries	42
Mean	59
Std Dev	9.399



# B1L102S, U20-ch14, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

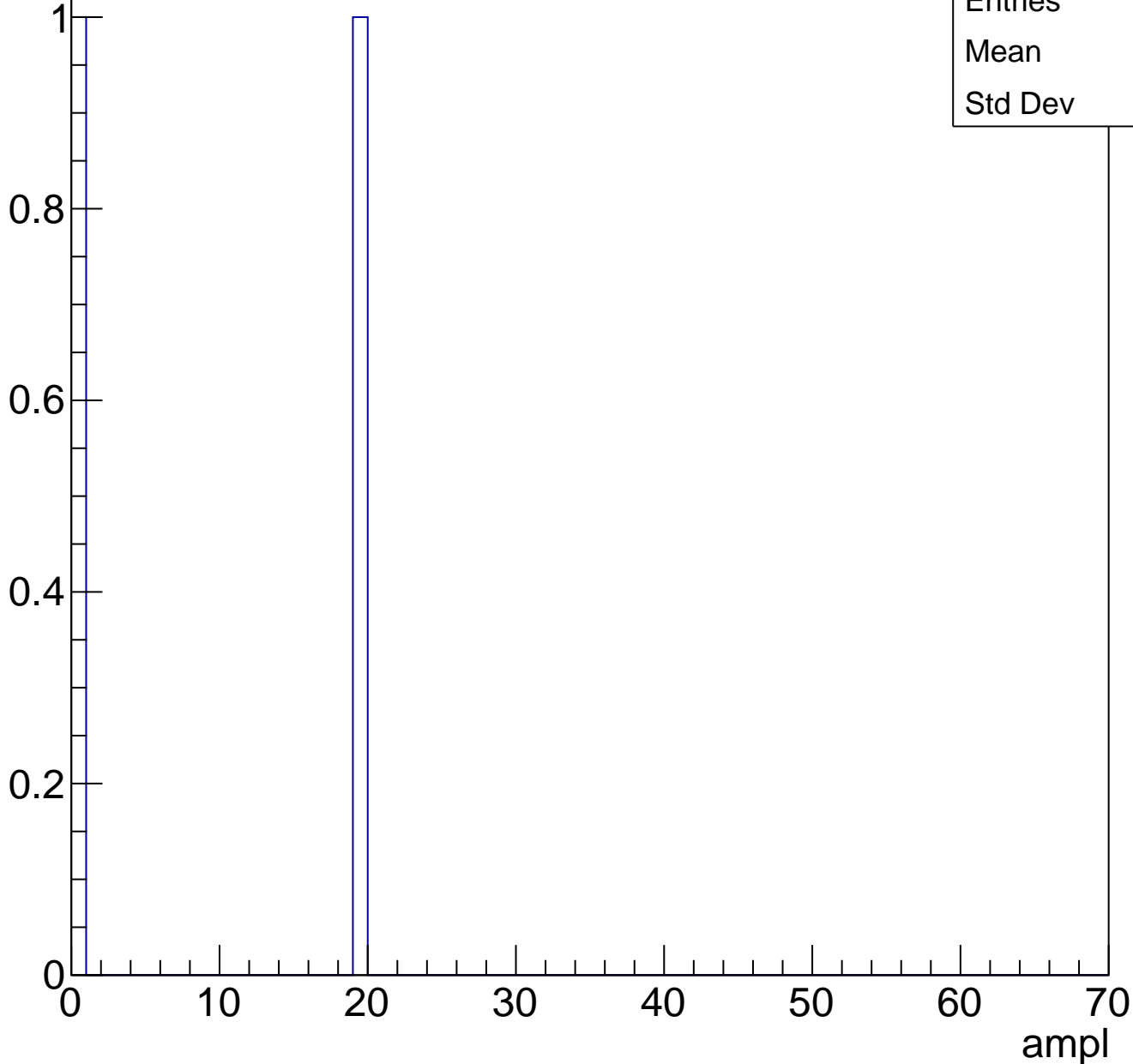




# B1L102S, U20-ch14, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch15, adc0

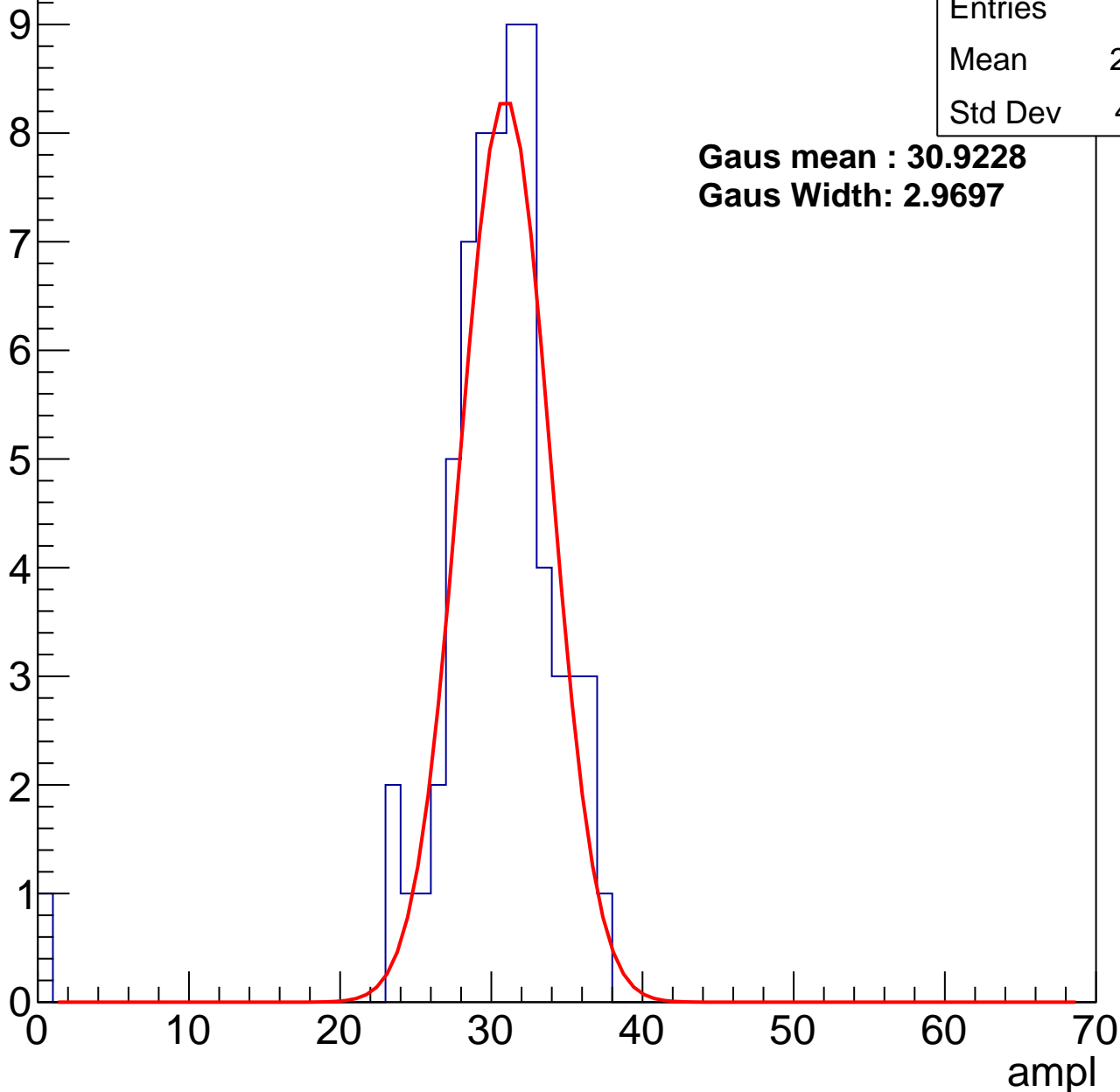
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	29.87
Std Dev	4.781

**Gaus mean : 30.9228**

**Gaus Width: 2.9697**



# B1L102S, U20-ch15, adc1

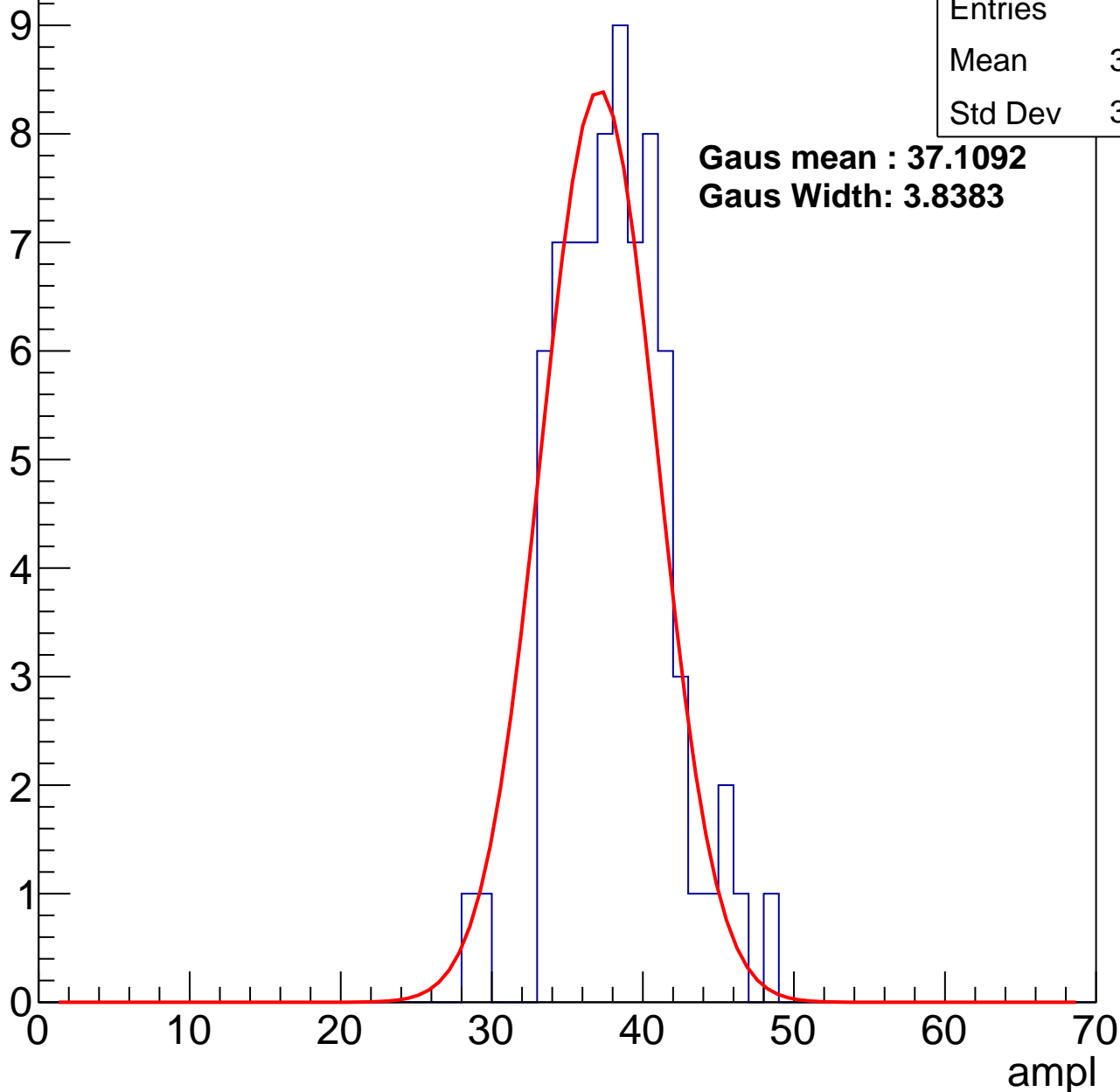
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	37.68
Std Dev	3.625

**Gaus mean : 37.1092**

**Gaus Width: 3.8383**



# B1L102S, U20-ch15, adc2

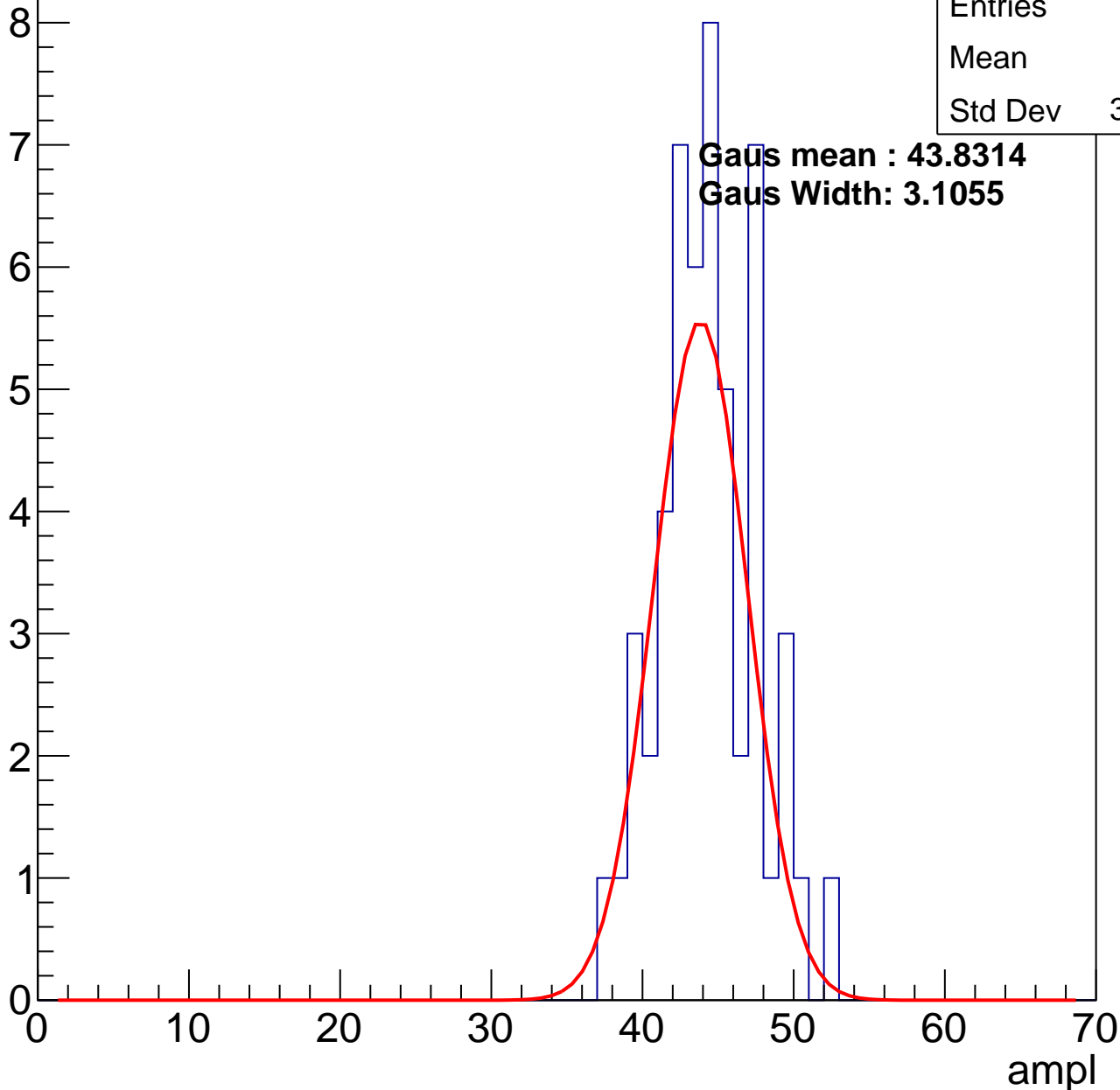
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	43.9
Std Dev	3.188

**Gaus mean : 43.8314**

**Gaus Width: 3.1055**



# B1L102S, U20-ch15, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	70
Mean	49.74
Std Dev	3.332

Entry

10

8

6

4

2

0

0

10

20

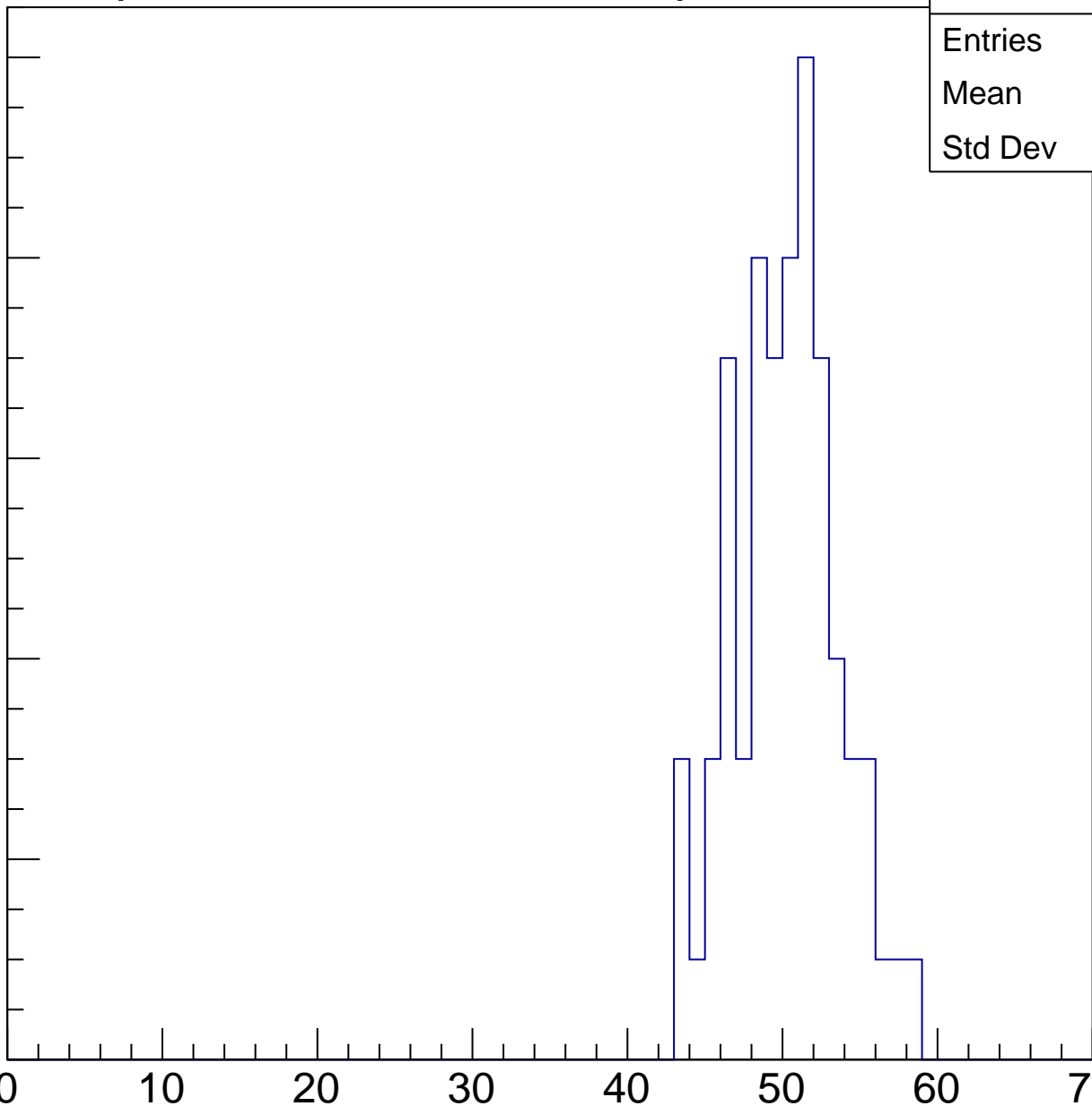
30

40

50

60

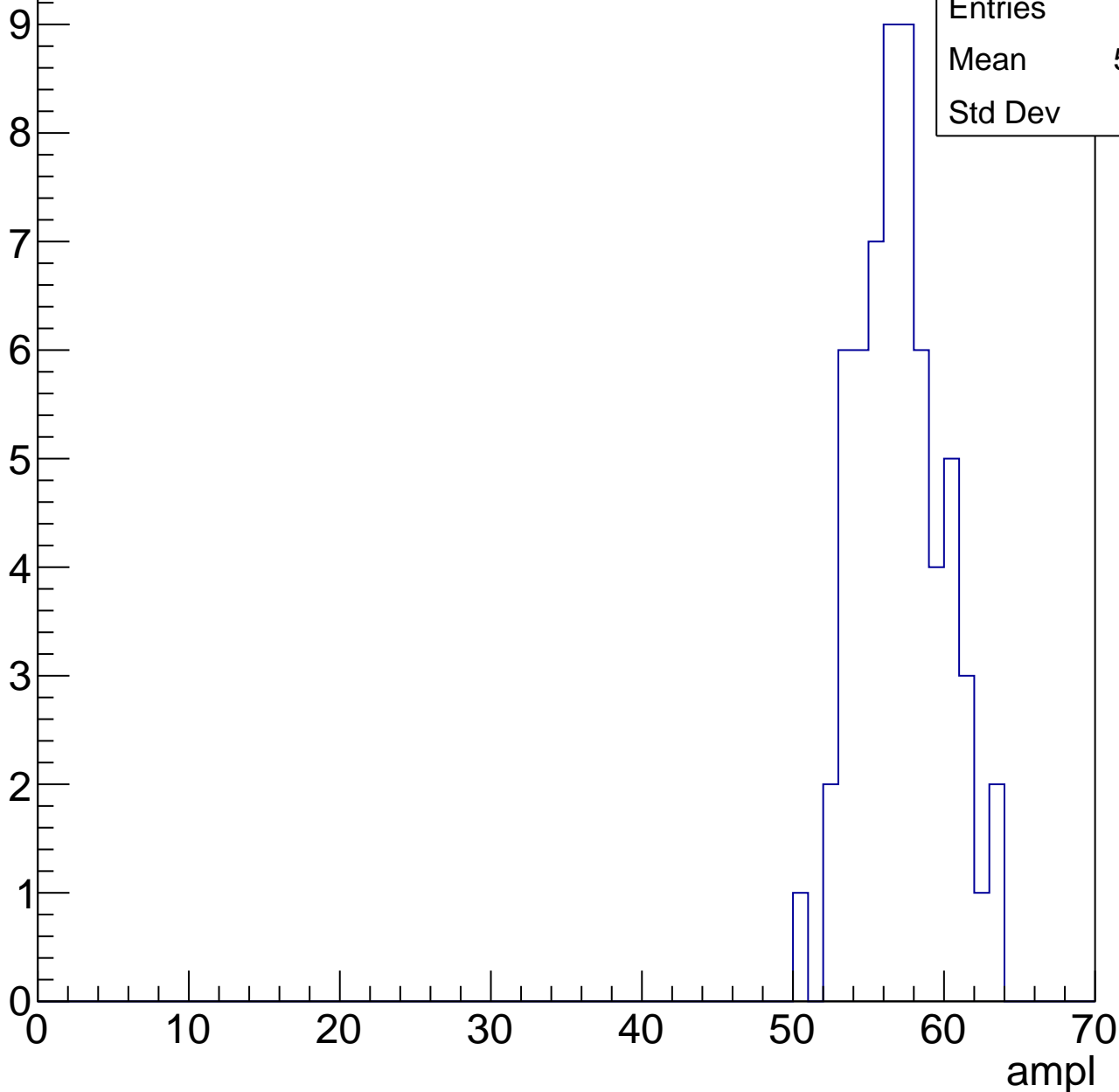
ampl



# B1L102S, U20-ch15, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

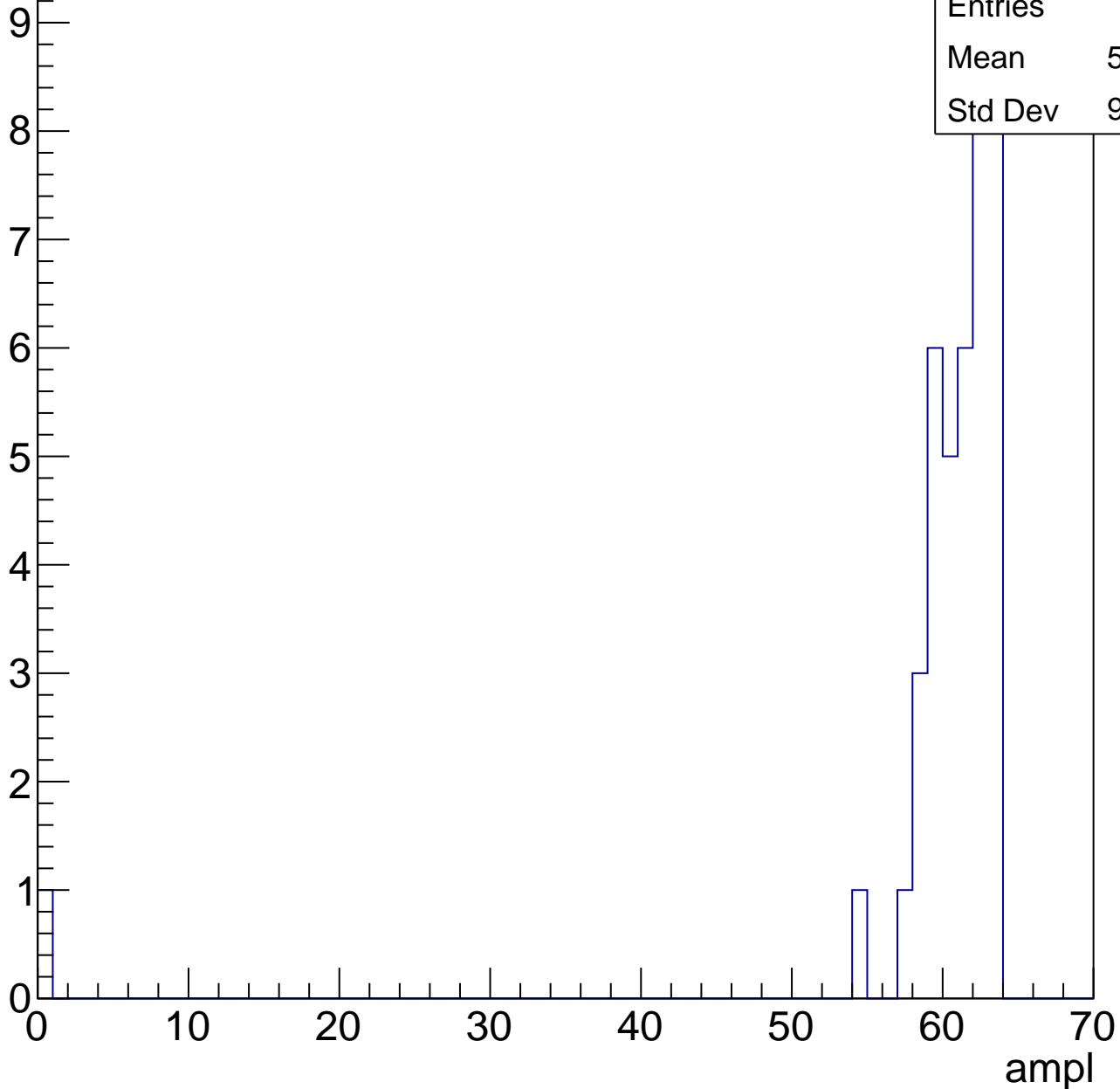


# B1L102S, U20-ch15, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	40
Mean	59.17
Std Dev	9.682



# B1L102S, U20-ch15, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U20-ch15, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	20
Std Dev	0

ampl

# B1L102S, U20-ch16, adc0

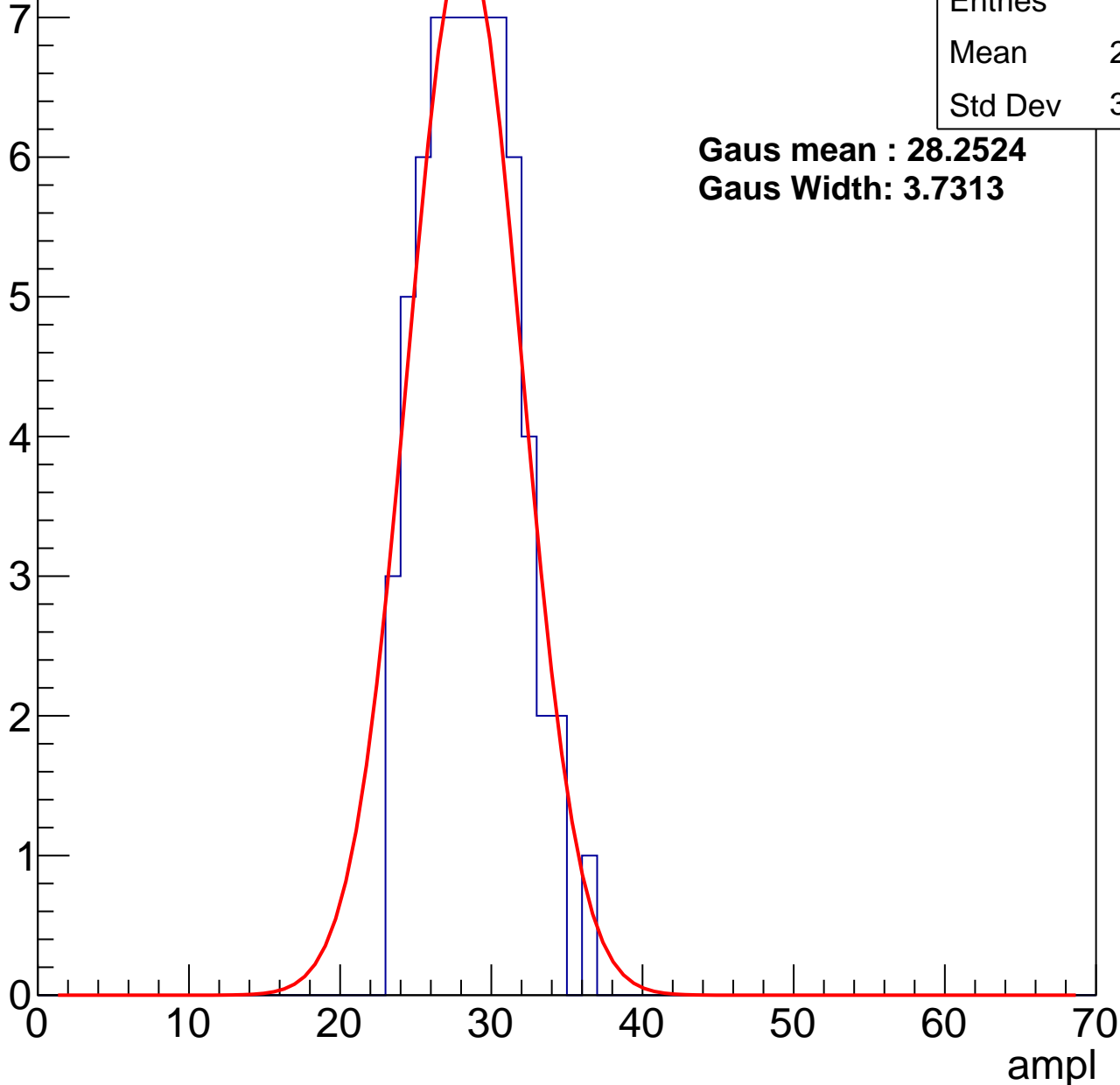
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	28.17
Std Dev	3.013

**Gaus mean : 28.2524**

**Gaus Width: 3.7313**



# B1L102S, U20-ch16, adc1

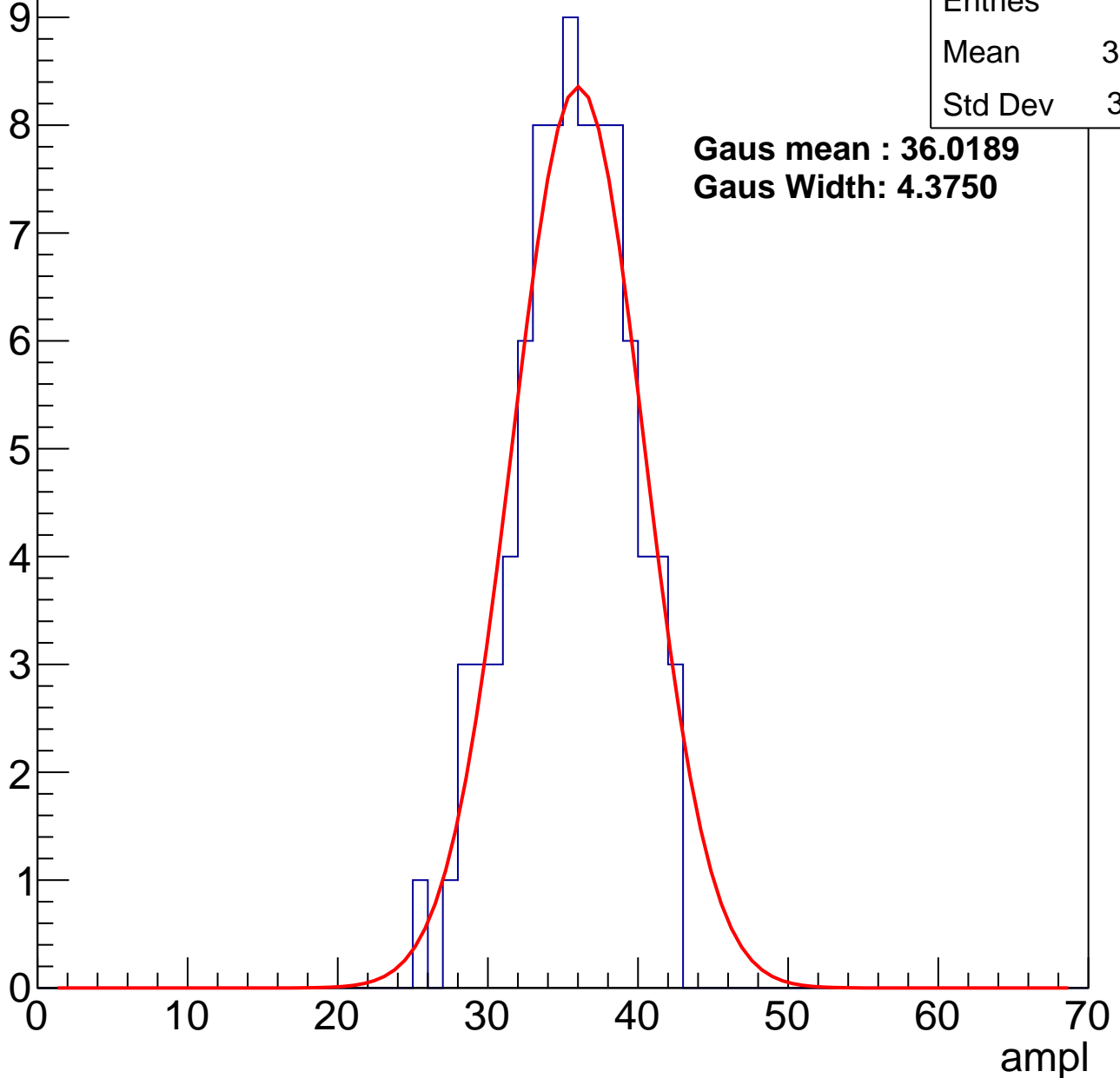
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	87
Mean	35.08
Std Dev	3.791

**Gaus mean : 36.0189**

**Gaus Width: 4.3750**



# B1L102S, U20-ch16, adc2

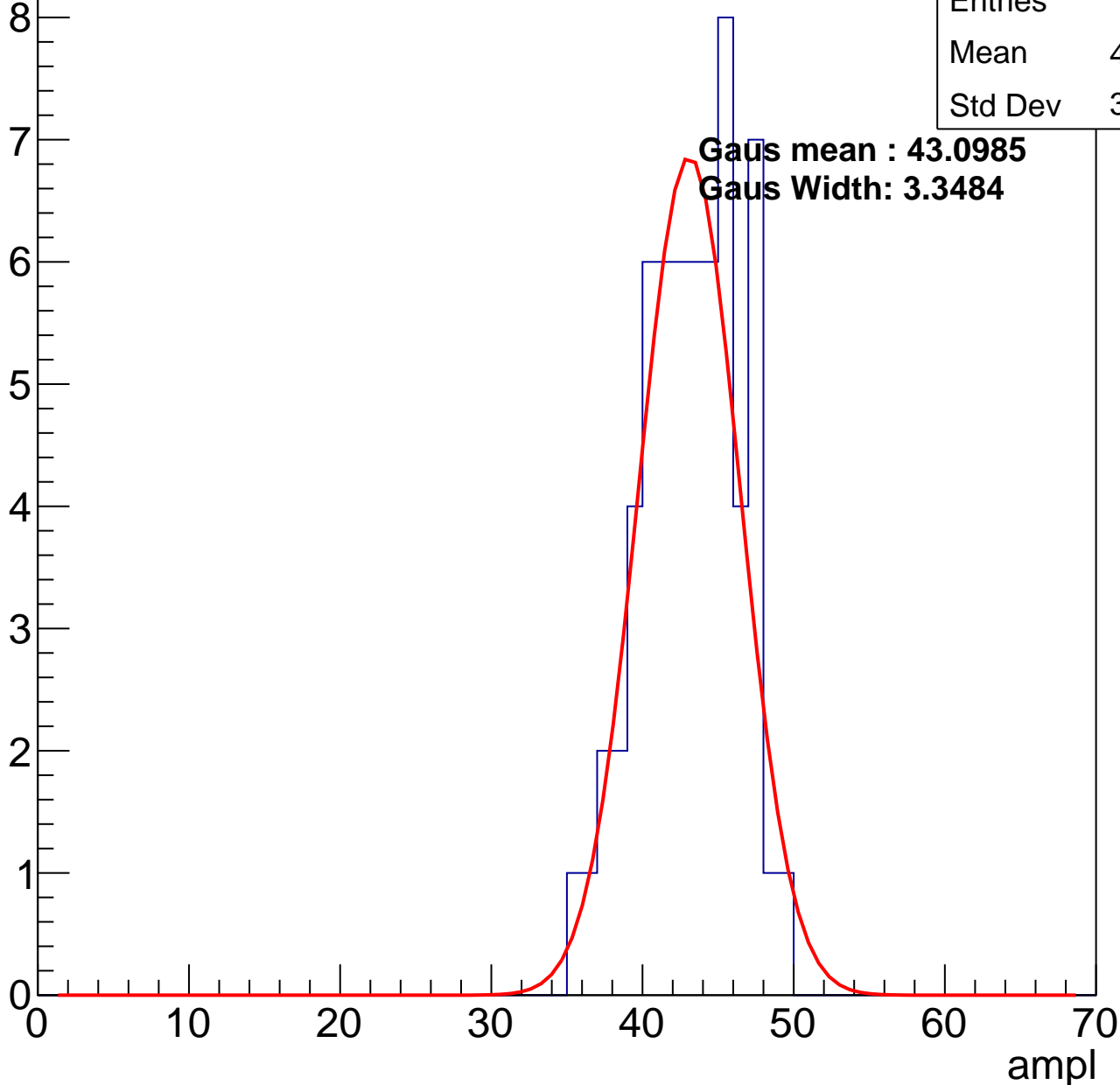
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	42.74
Std Dev	3.203

**Gaus mean : 43.0985**

**Gaus Width: 3.3484**

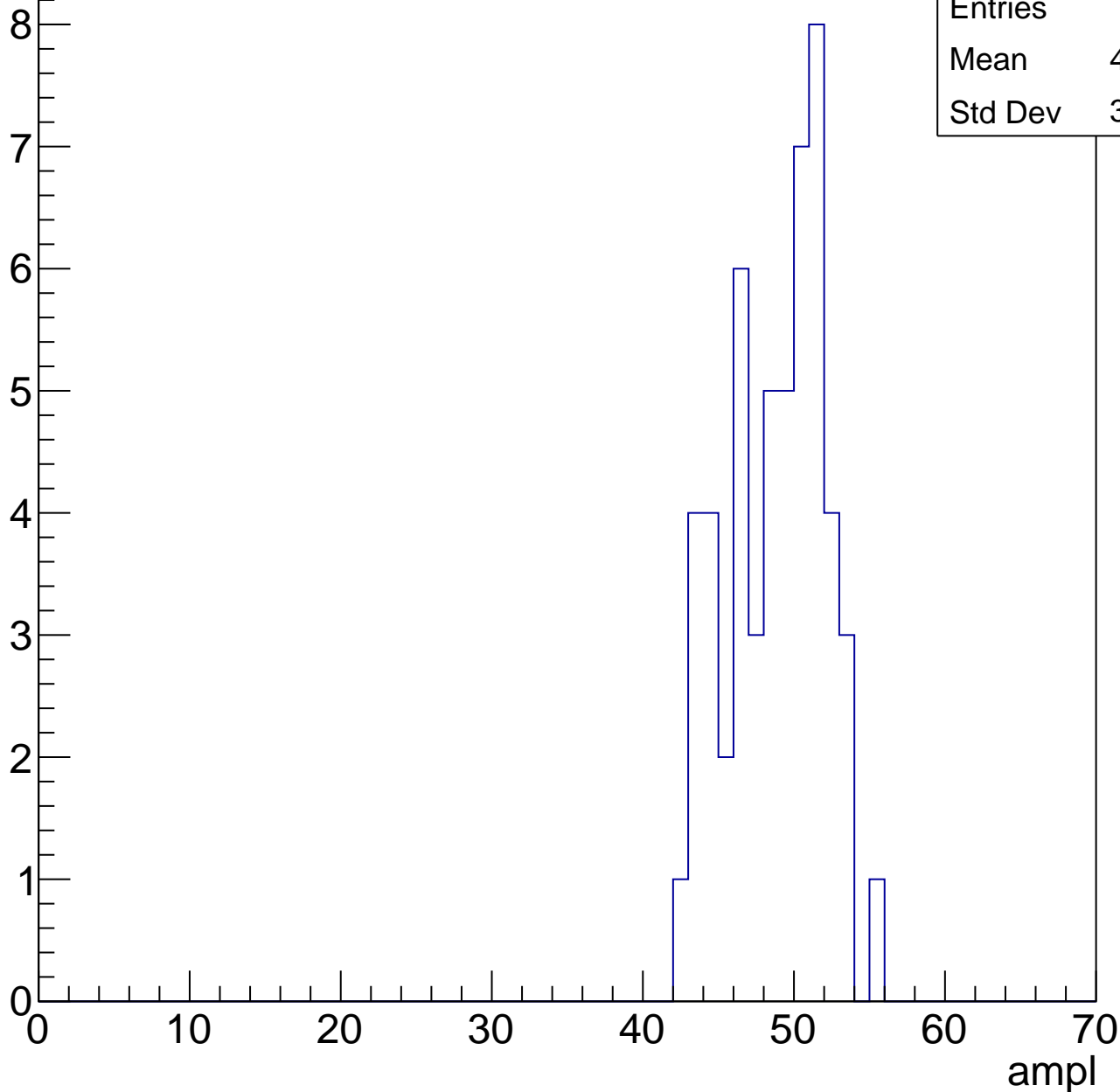


# B1L102S, U20-ch16, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	48.34
Std Dev	3.168

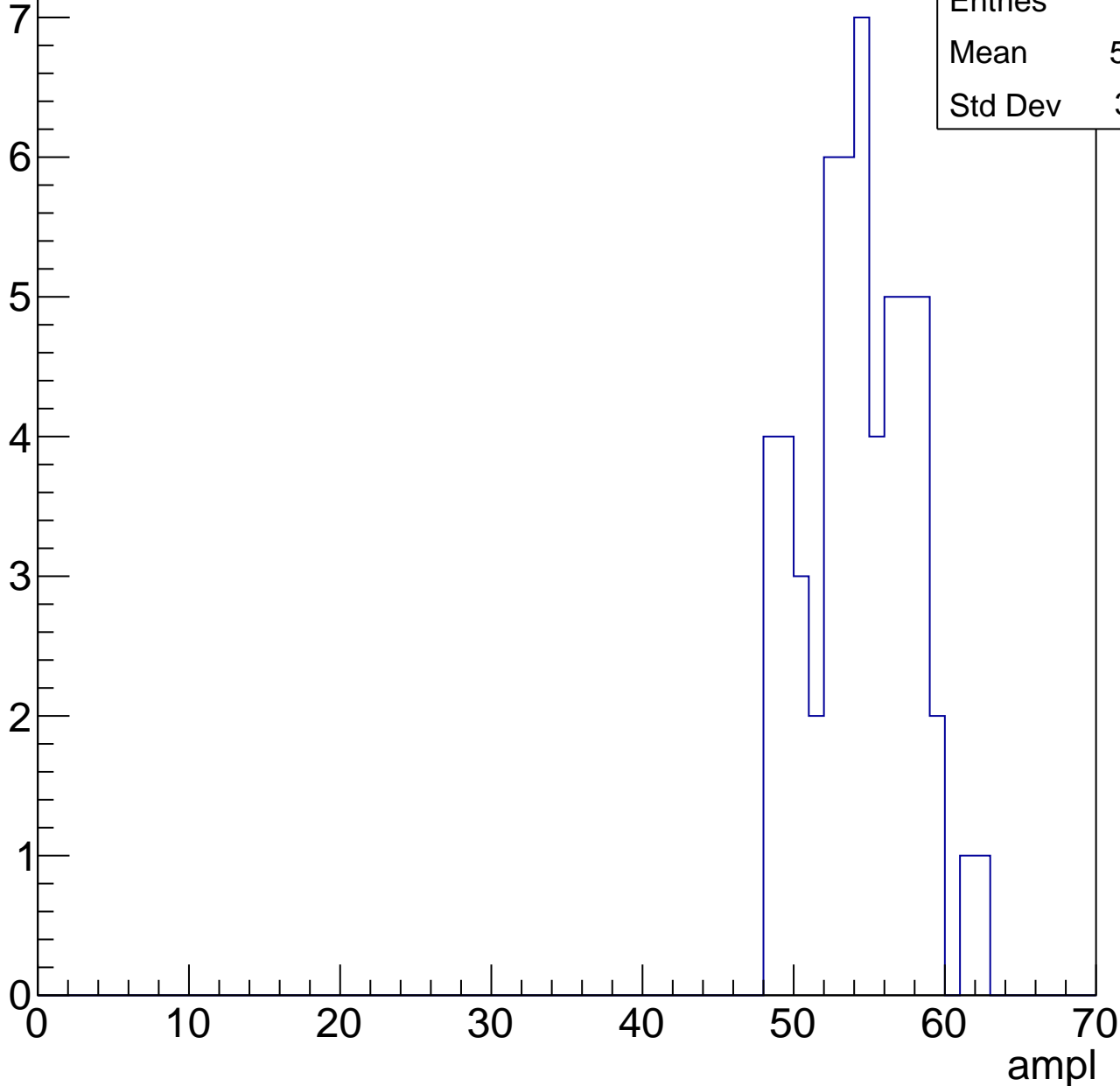


# B1L102S, U20-ch16, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

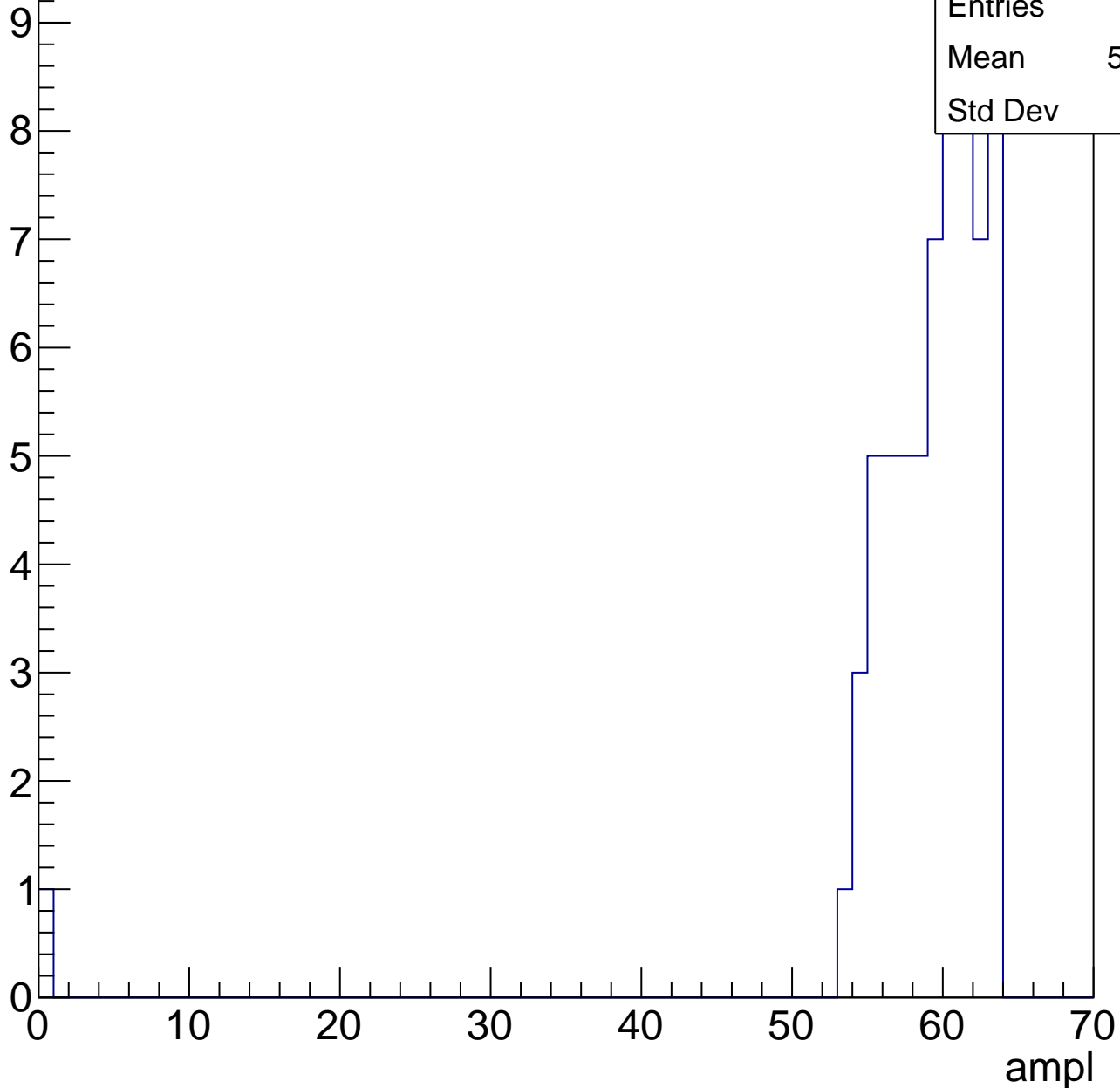
Entries	55
Mean	53.89
Std Dev	3.441



# B1L102S, U20-ch16, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

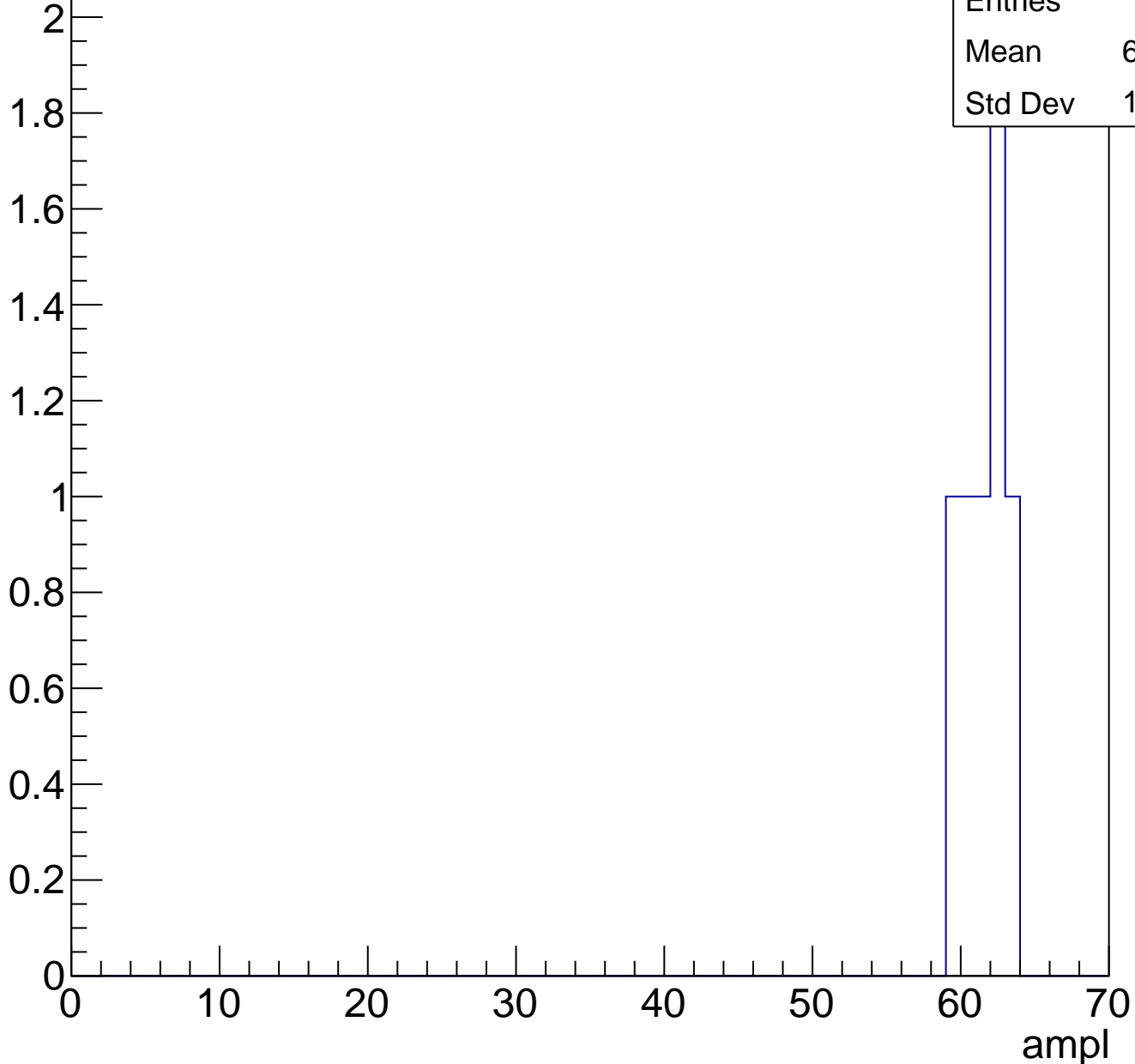
Entry



# B1L102S, U20-ch16, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U20-ch16, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch17, adc0

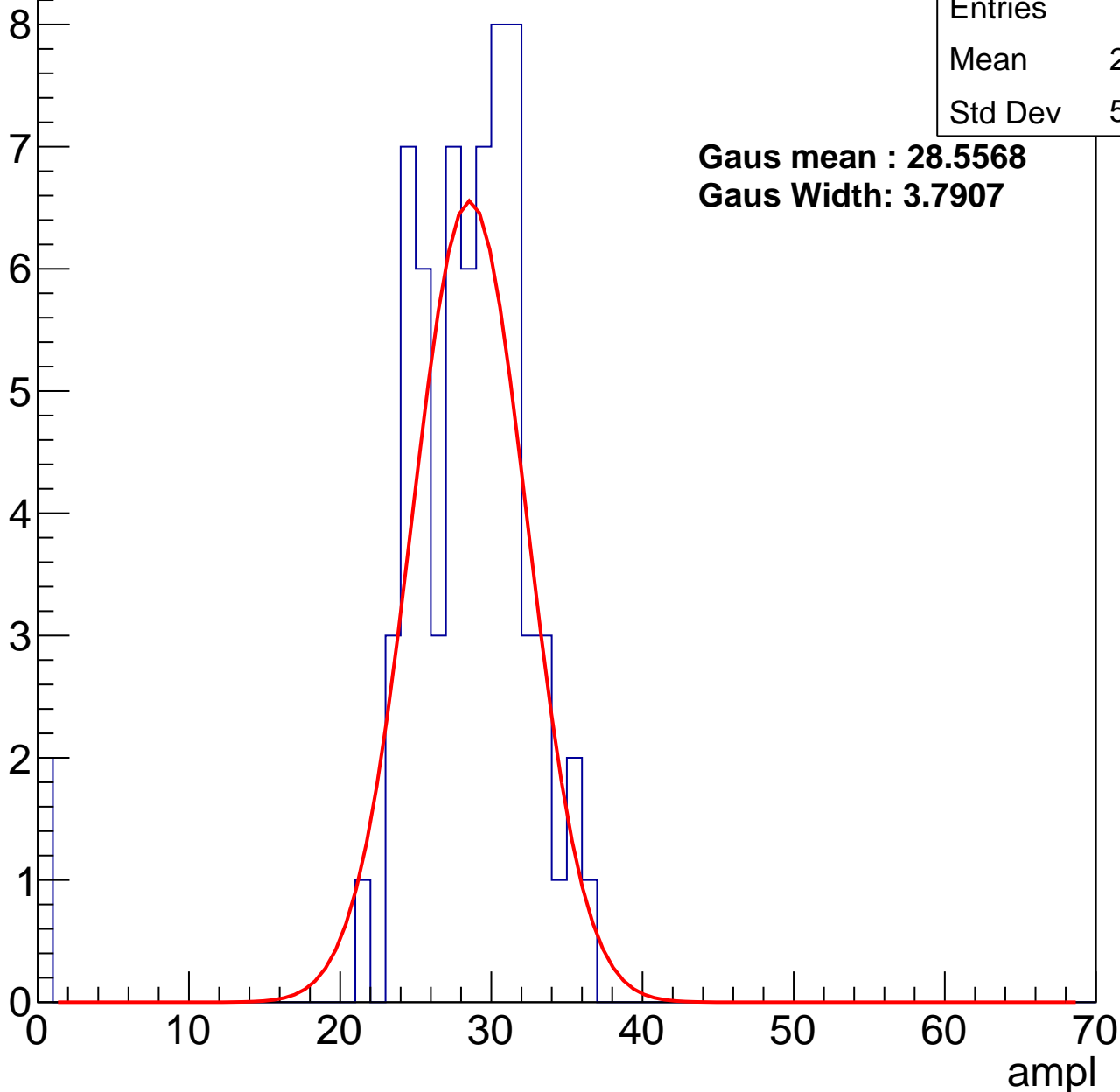
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	27.49
Std Dev	5.804

**Gaus mean : 28.5568**

**Gaus Width: 3.7907**



# B1L102S, U20-ch17, adc1

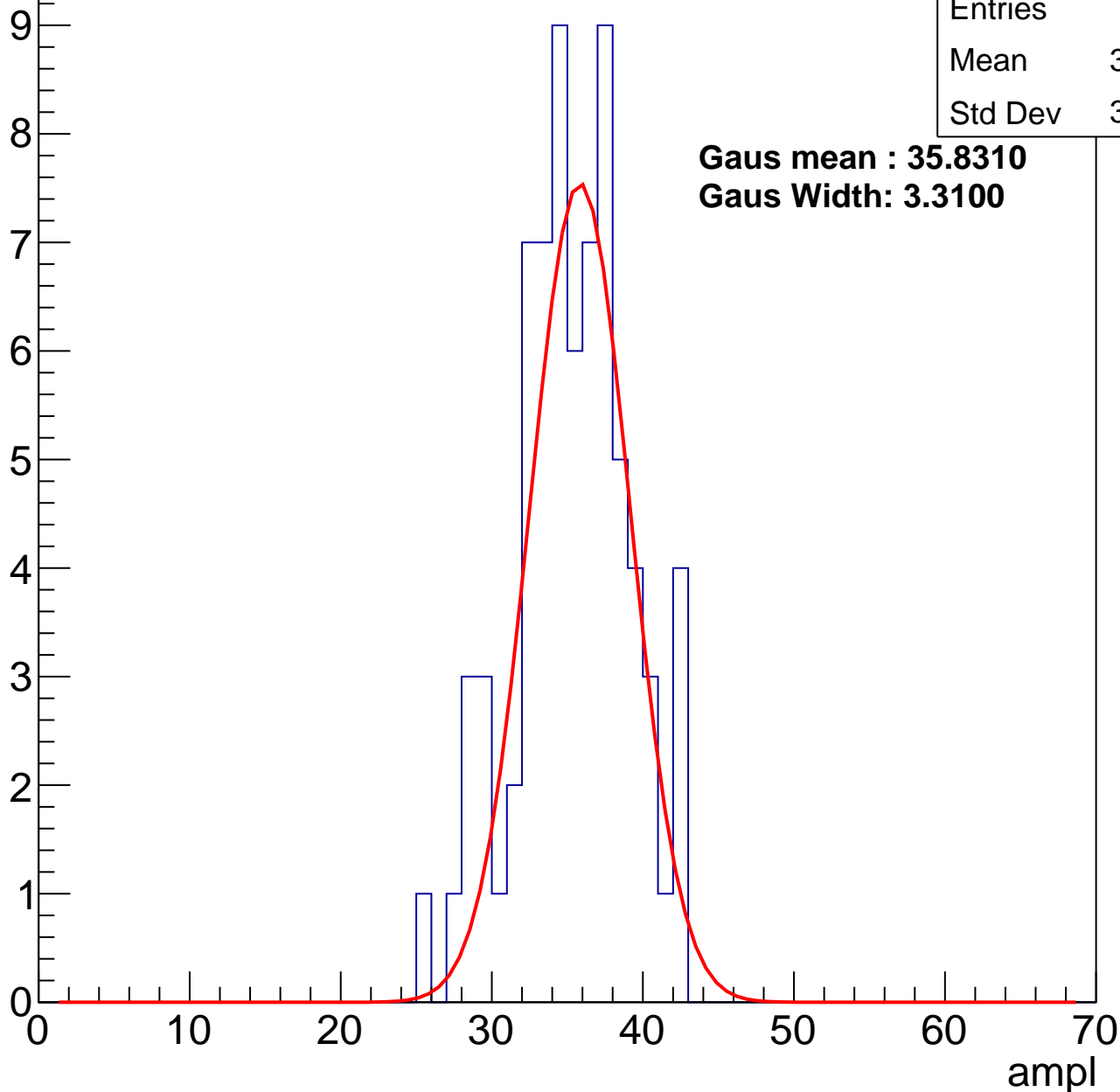
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	34.88
Std Dev	3.763

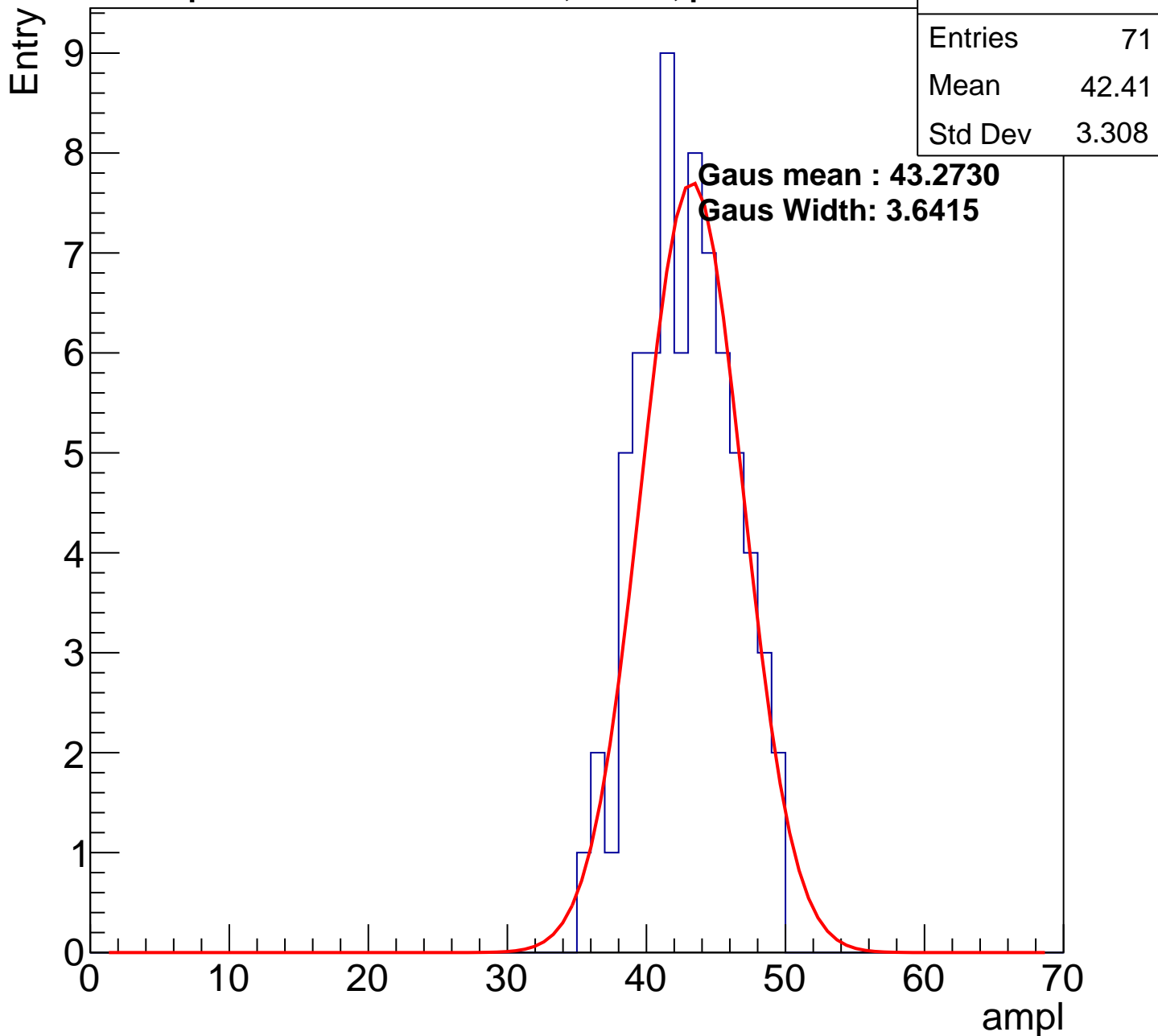
**Gaus mean : 35.8310**

**Gaus Width: 3.3100**



# B1L102S, U20-ch17, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

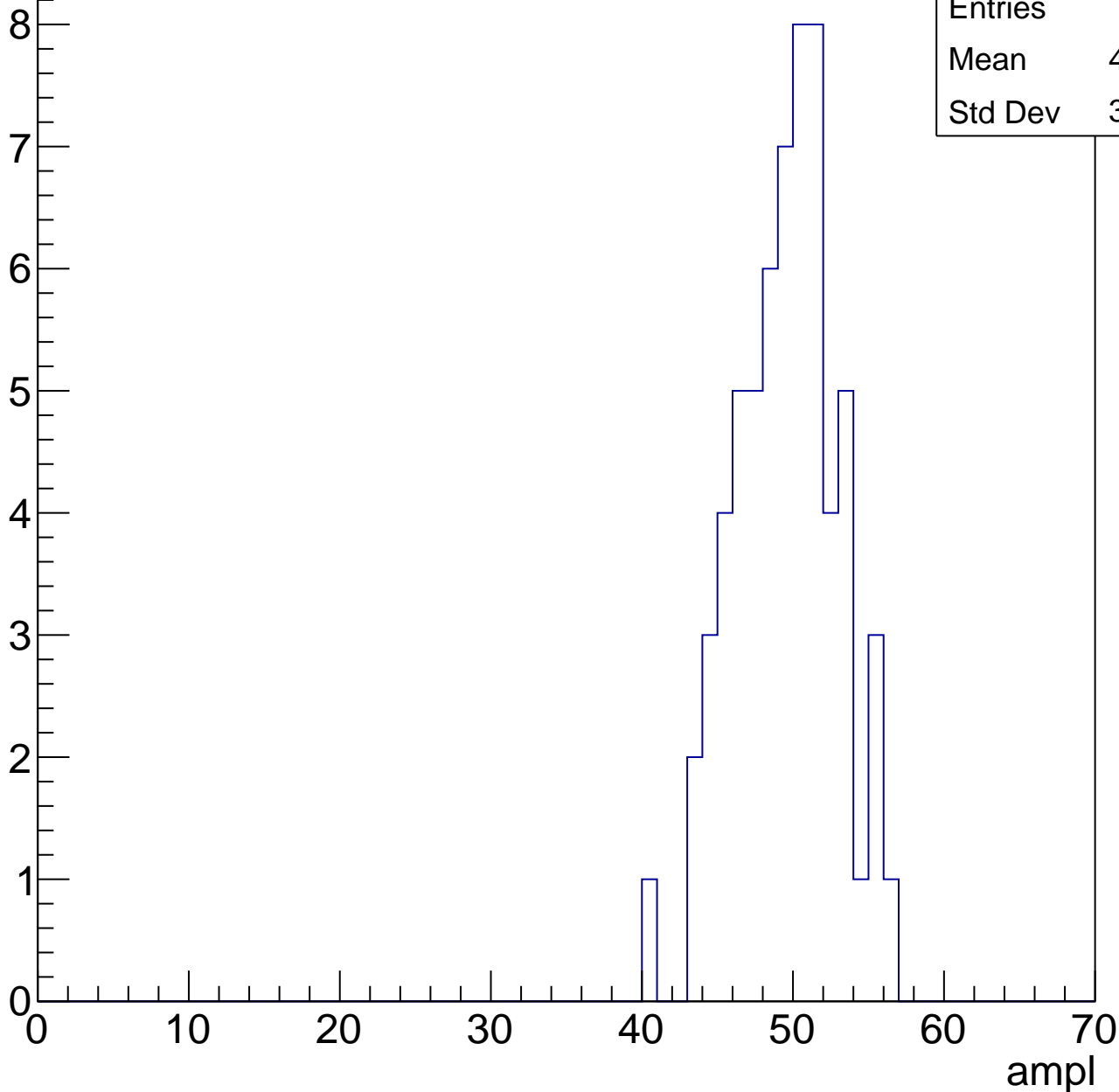


# B1L102S, U20-ch17, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	49.05
Std Dev	3.335

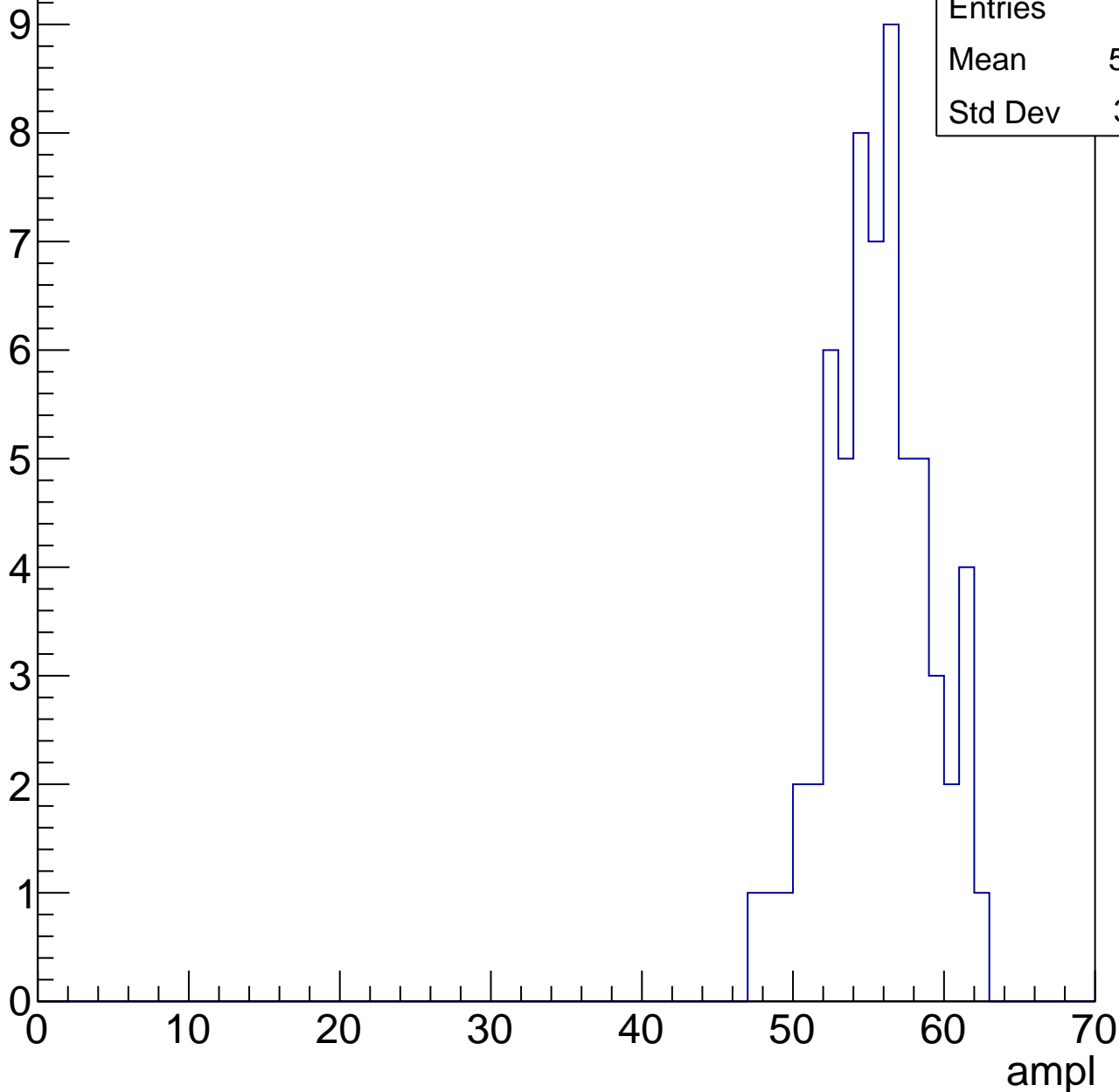


# B1L102S, U20-ch17, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	55.19
Std Dev	3.301

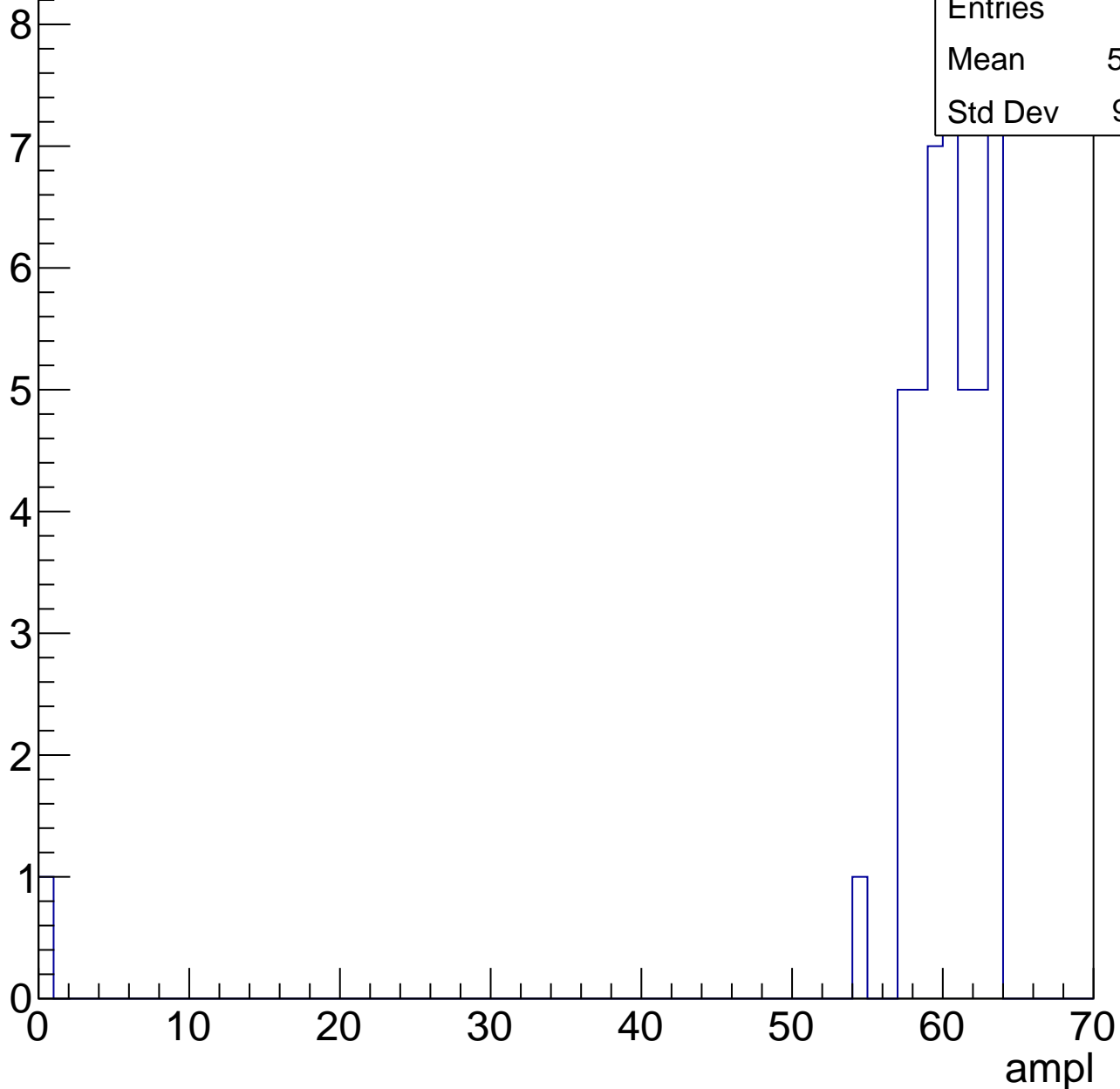


# B1L102S, U20-ch17, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	45
Mean	58.69
Std Dev	9.101



# B1L102S, U20-ch17, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U20-ch17, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch18, adc0

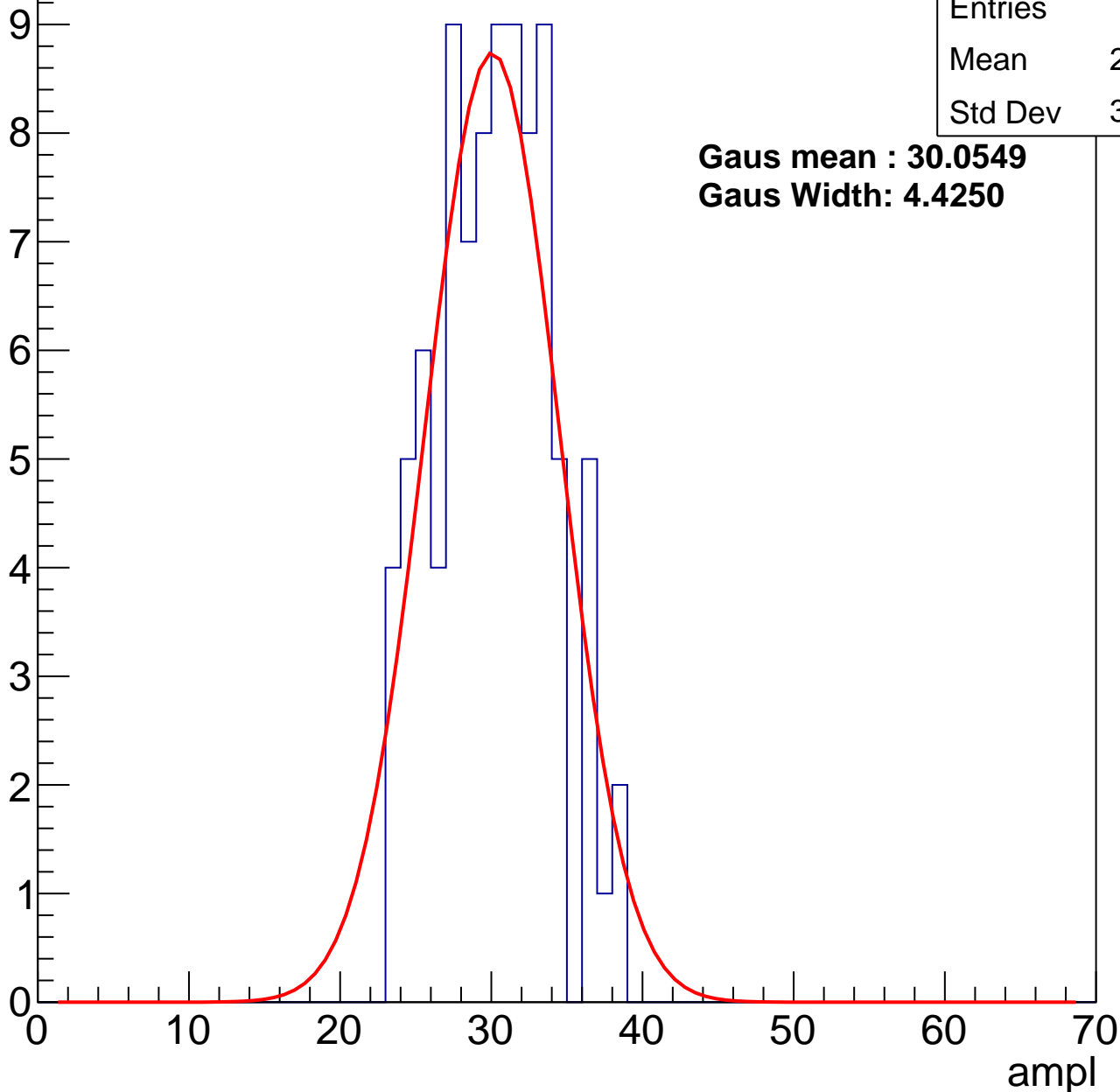
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	91
Mean	29.69
Std Dev	3.717

**Gaus mean : 30.0549**

**Gaus Width: 4.4250**



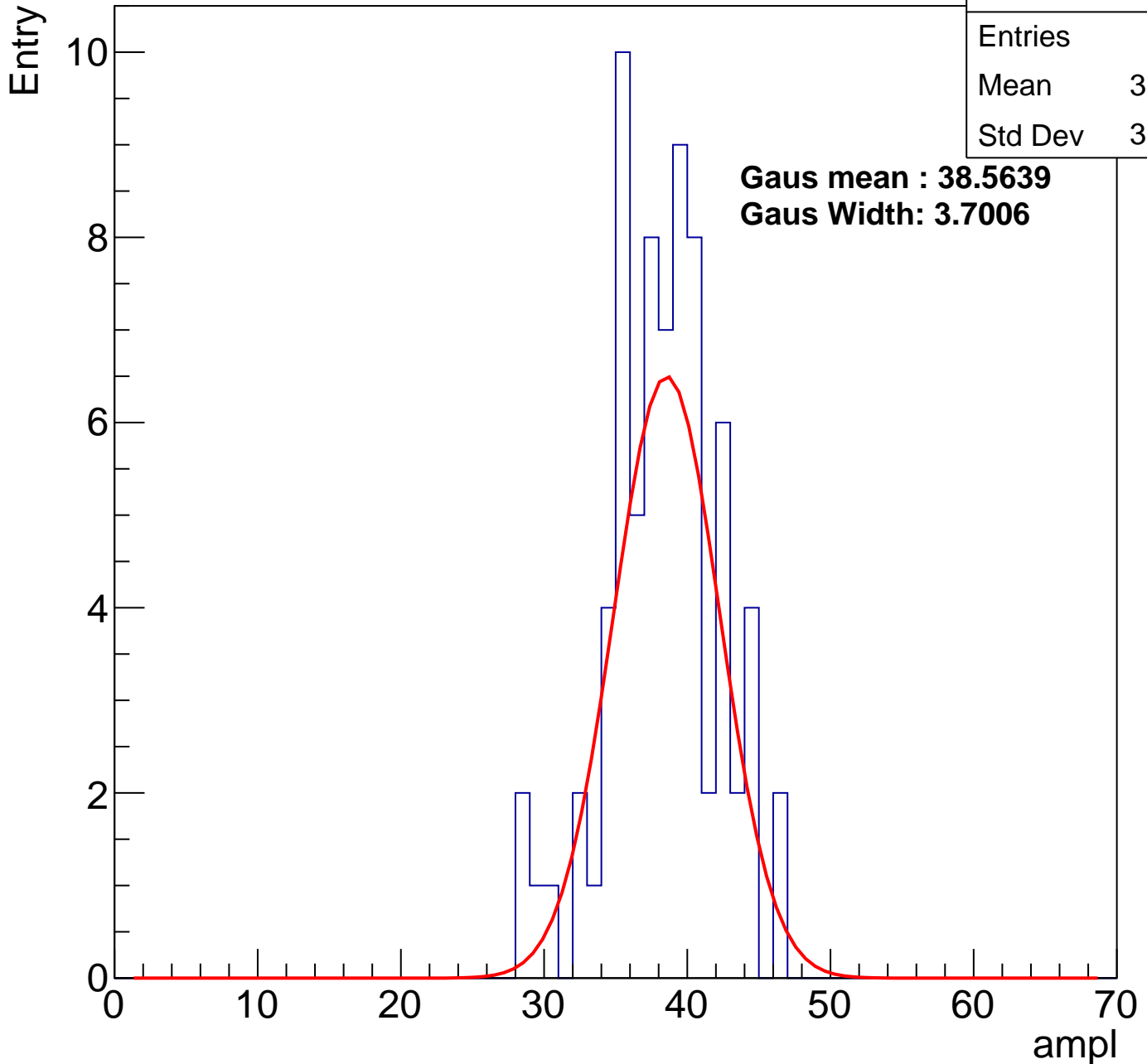
# B1L102S, U20-ch18, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	74
Mean	37.82
Std Dev	3.853

**Gaus mean : 38.5639**

**Gaus Width: 3.7006**



# B1L102S, U20-ch18, adc2

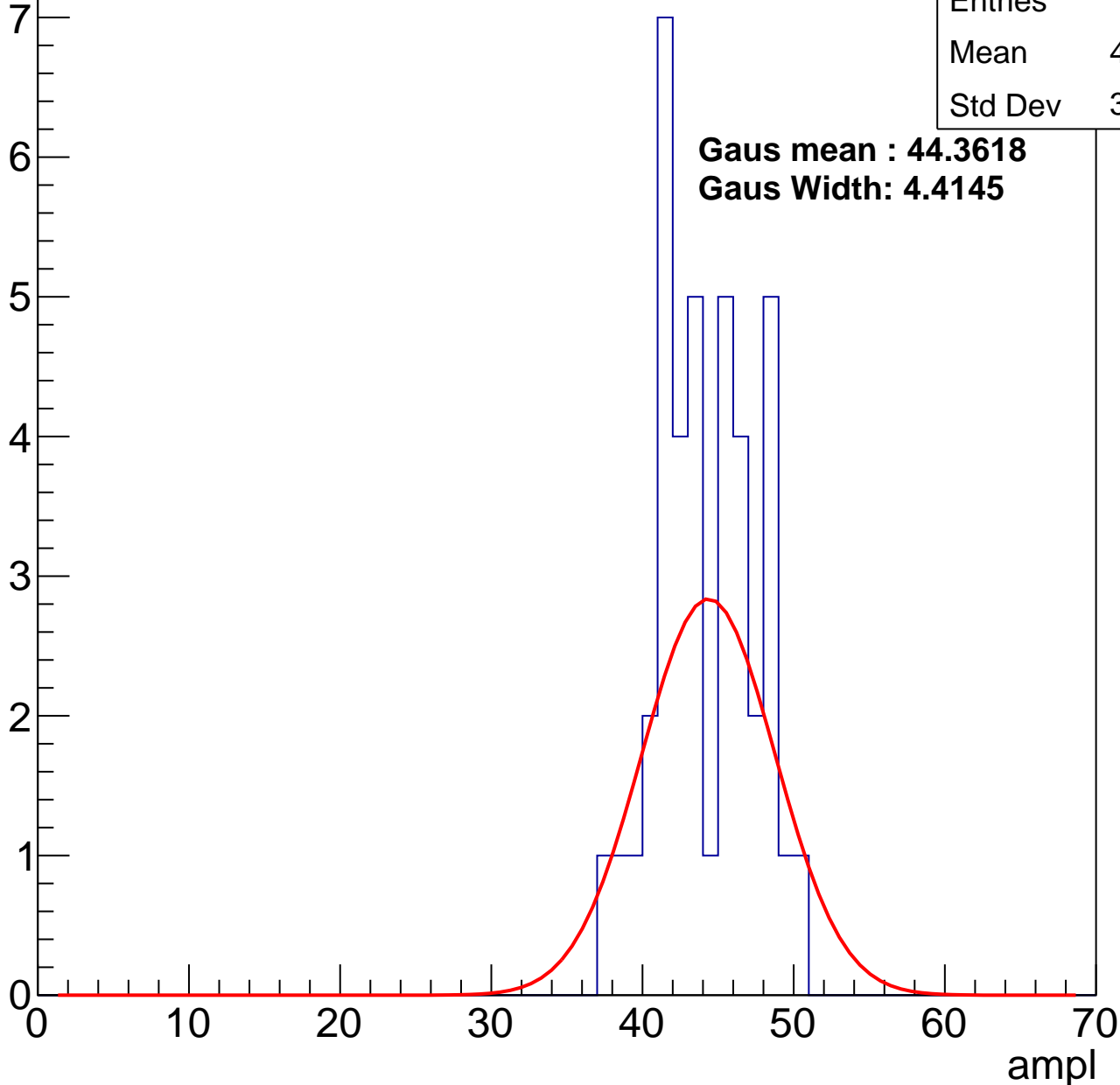
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	40
Mean	43.75
Std Dev	3.176

**Gaus mean : 44.3618**

**Gaus Width: 4.4145**

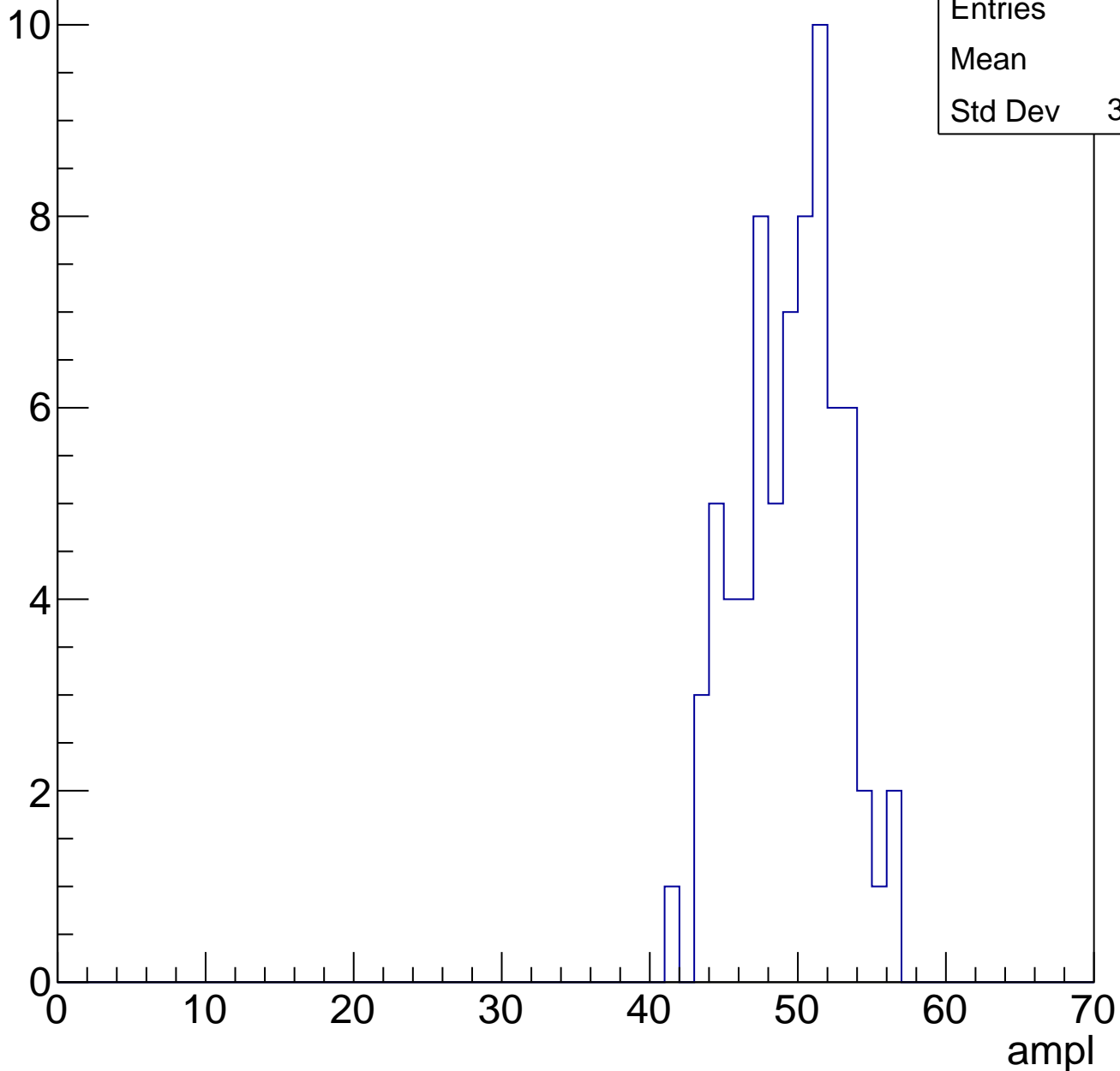


# B1L102S, U20-ch18, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	72
Mean	49
Std Dev	3.367

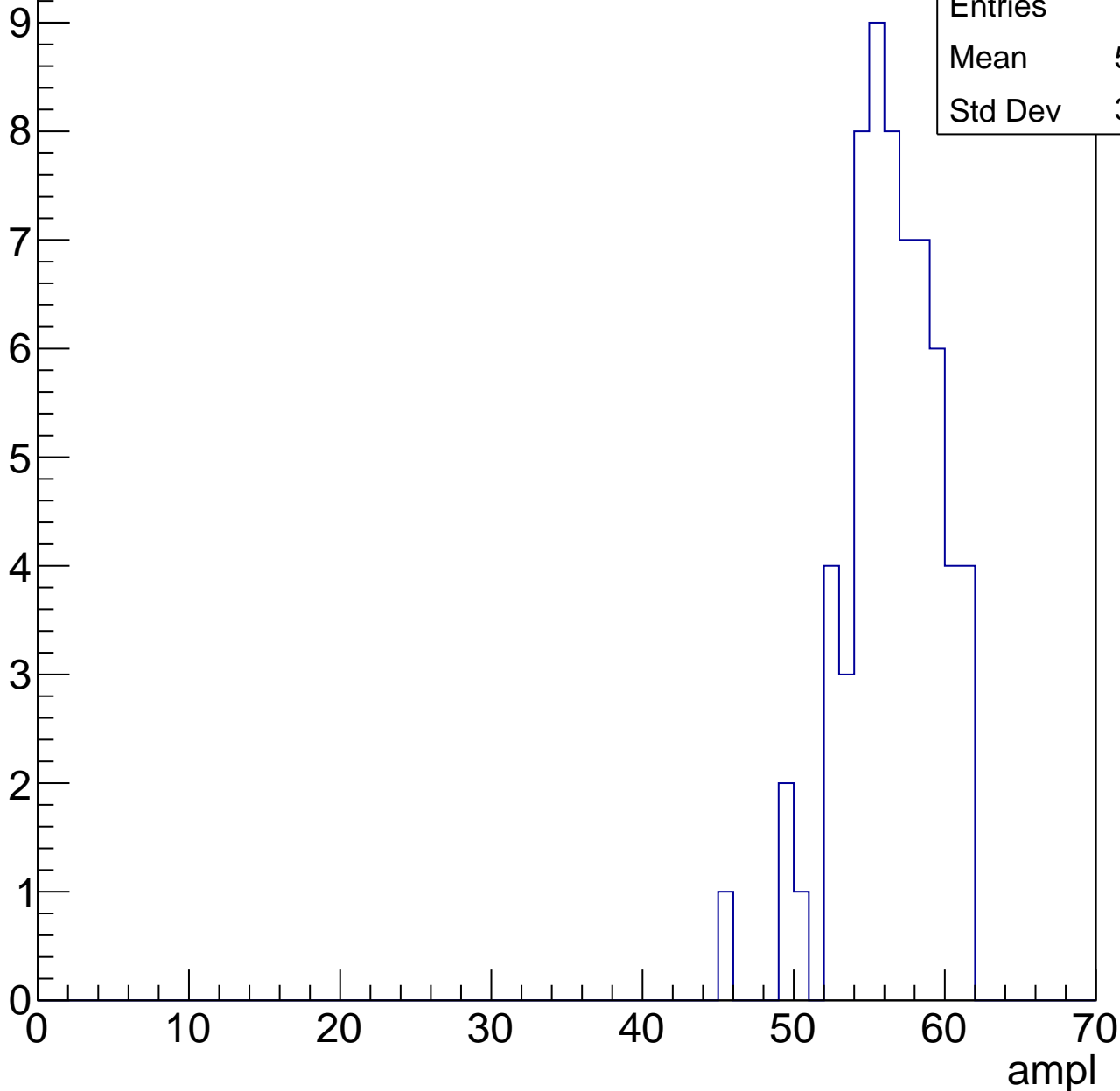
Entry



# B1L102S, U20-ch18, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

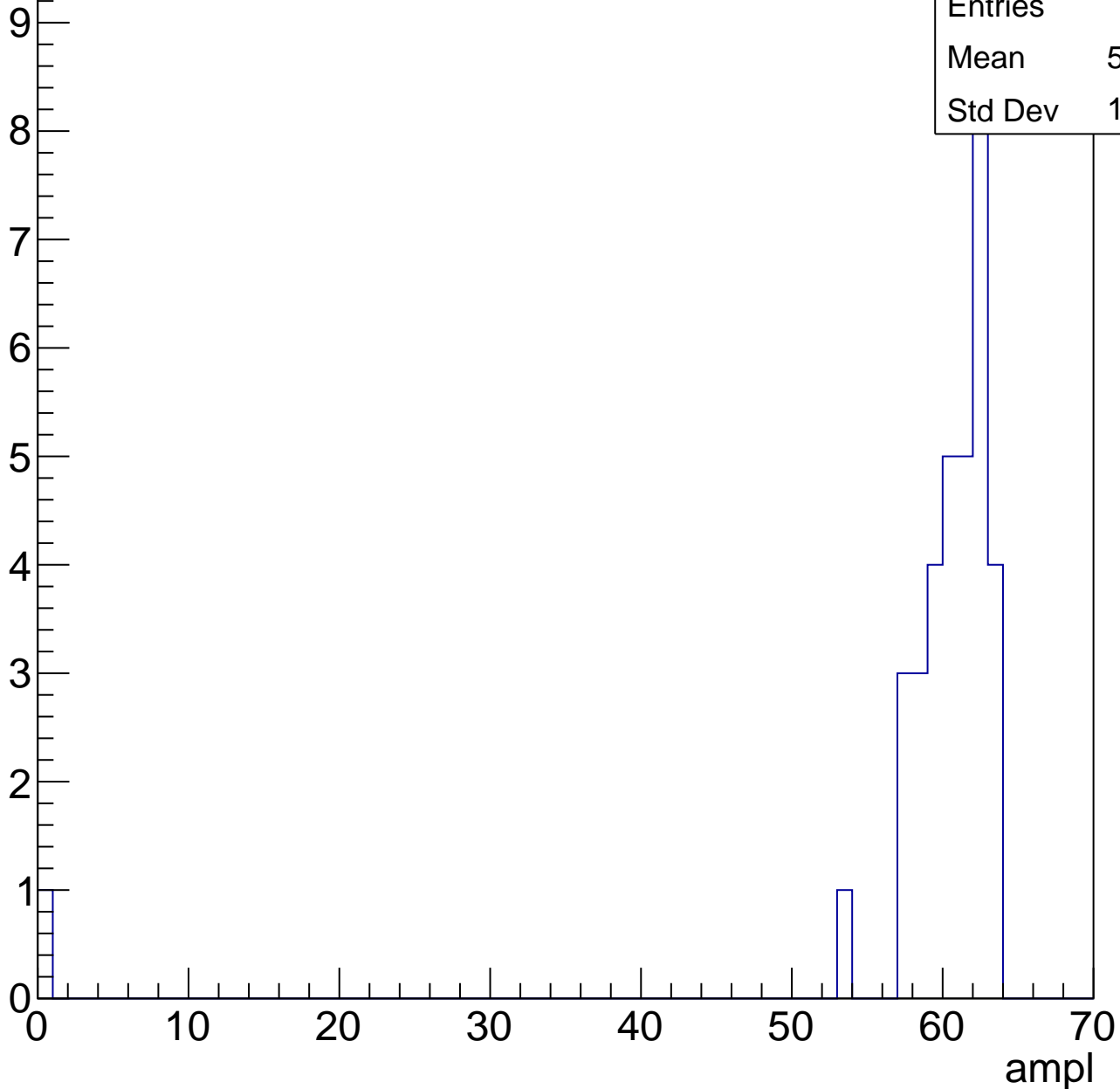


# B1L102S, U20-ch18, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	35
Mean	58.54
Std Dev	10.27

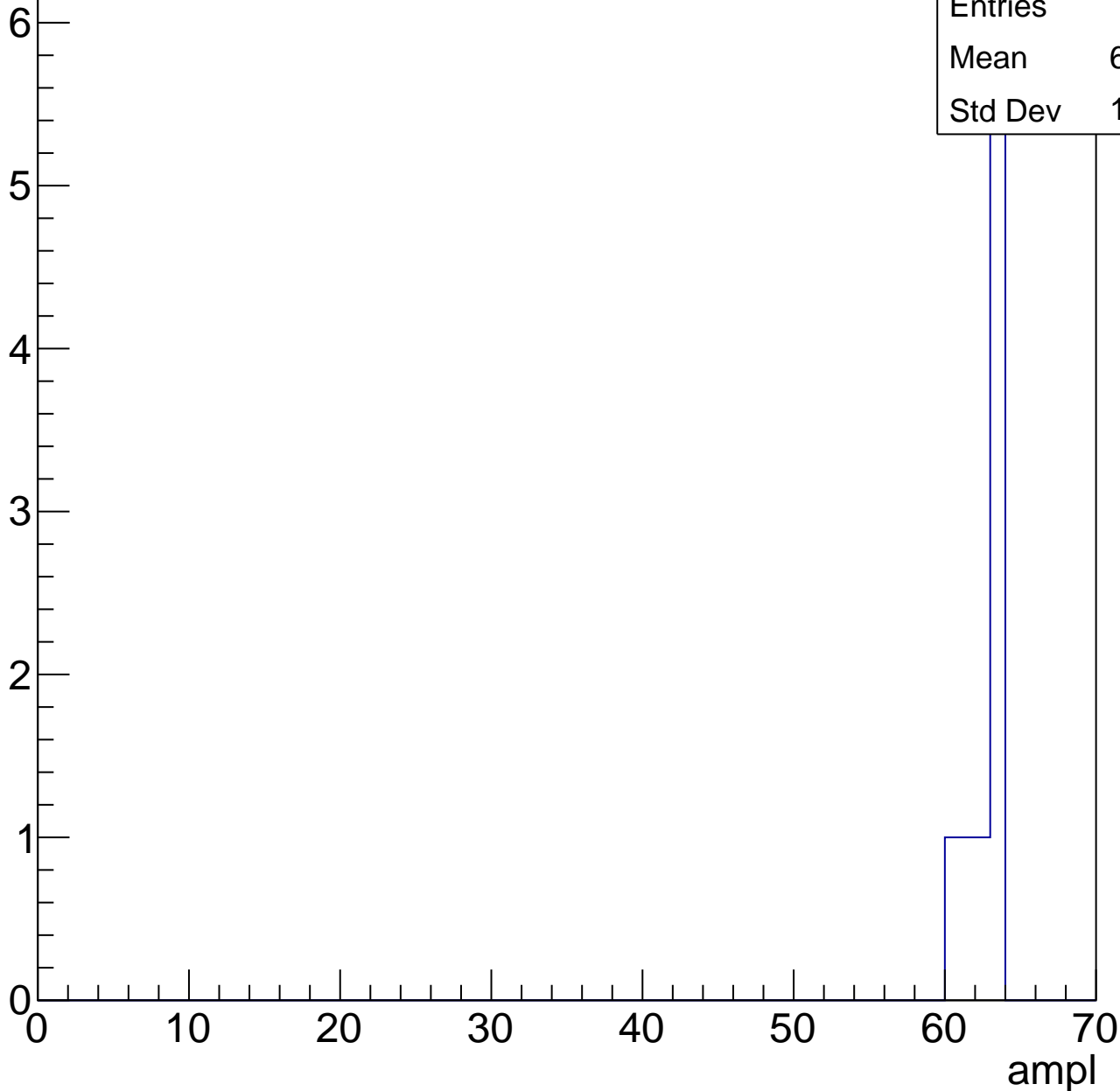


# B1L102S, U20-ch18, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	9
Mean	62.33
Std Dev	1.054





# B1L102S, U20-ch18, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch19, adc0

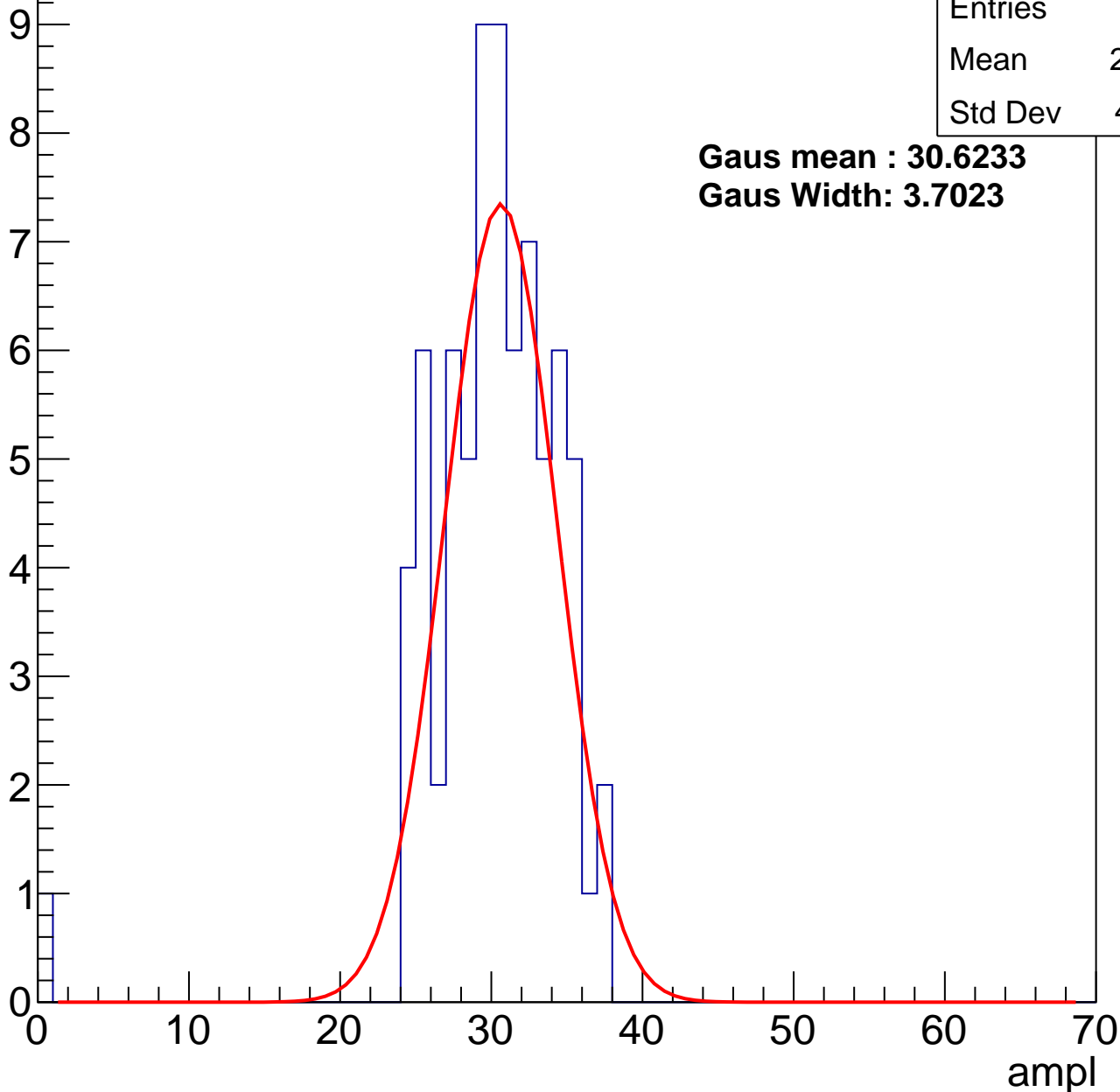
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	29.66
Std Dev	4.841

**Gaus mean : 30.6233**

**Gaus Width: 3.7023**



# B1L102S, U20-ch19, adc1

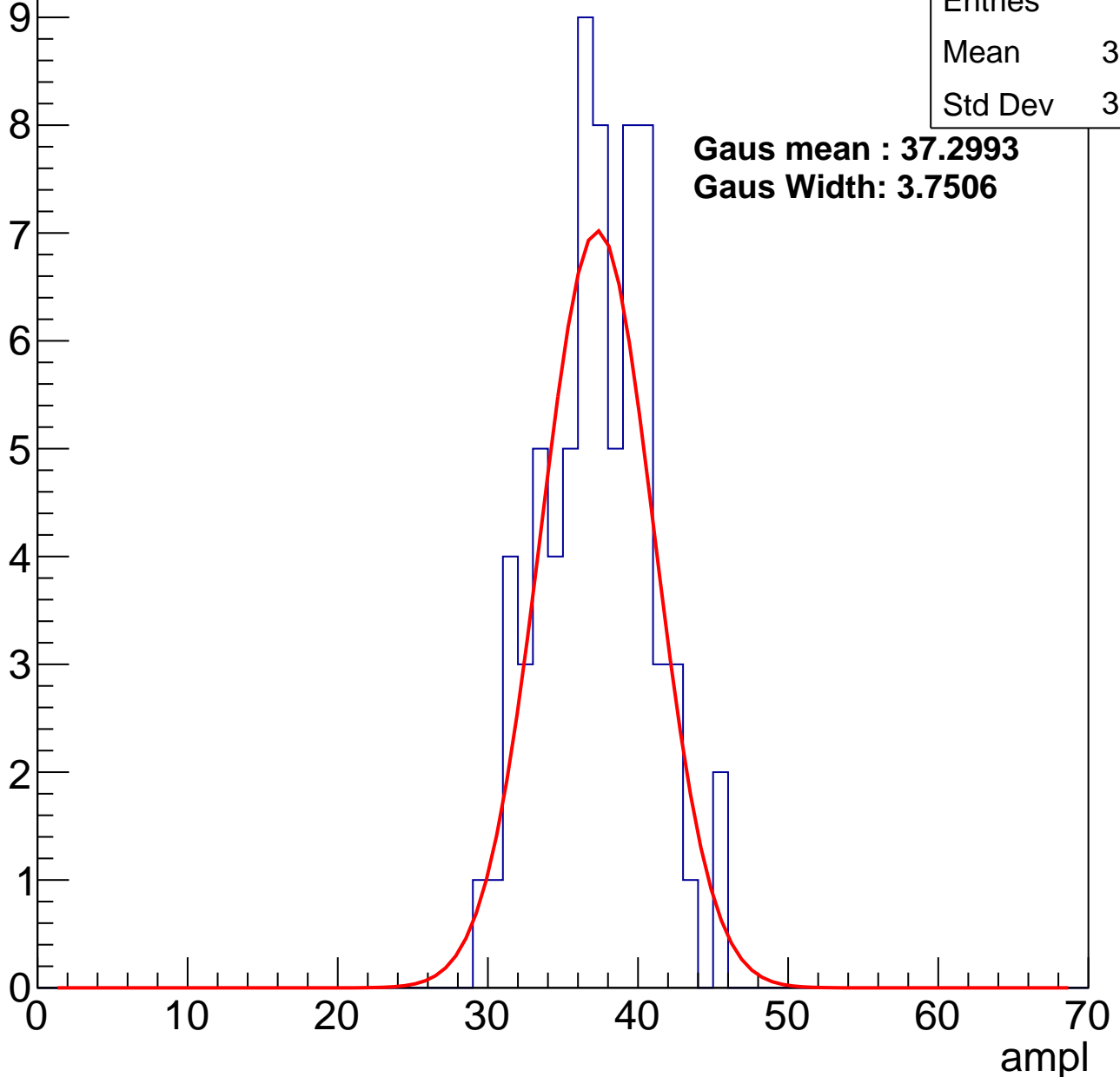
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	36.84
Std Dev	3.528

**Gaus mean : 37.2993**

**Gaus Width: 3.7506**

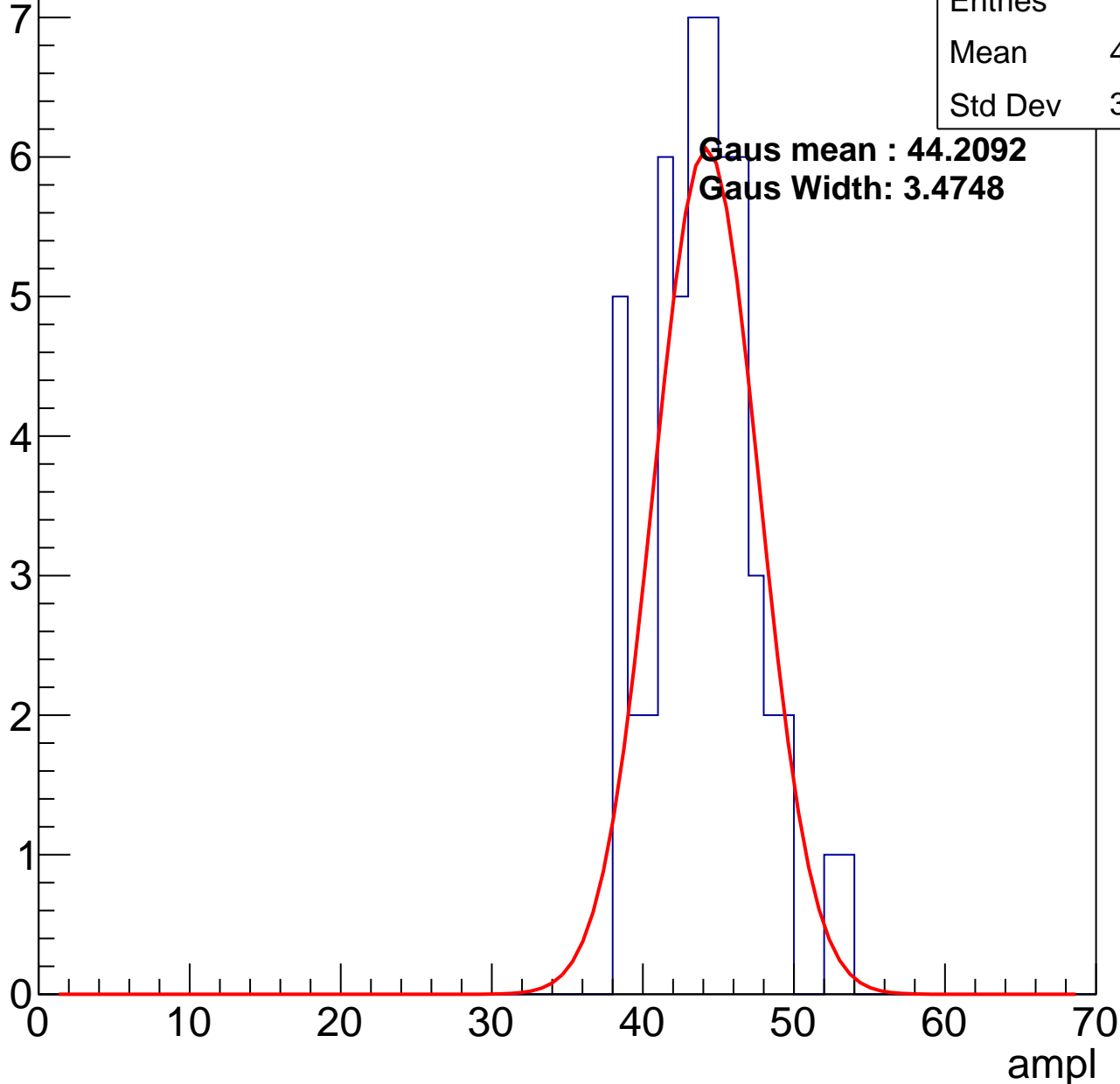


# B1L102S, U20-ch19, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	43.62
Std Dev	3.355

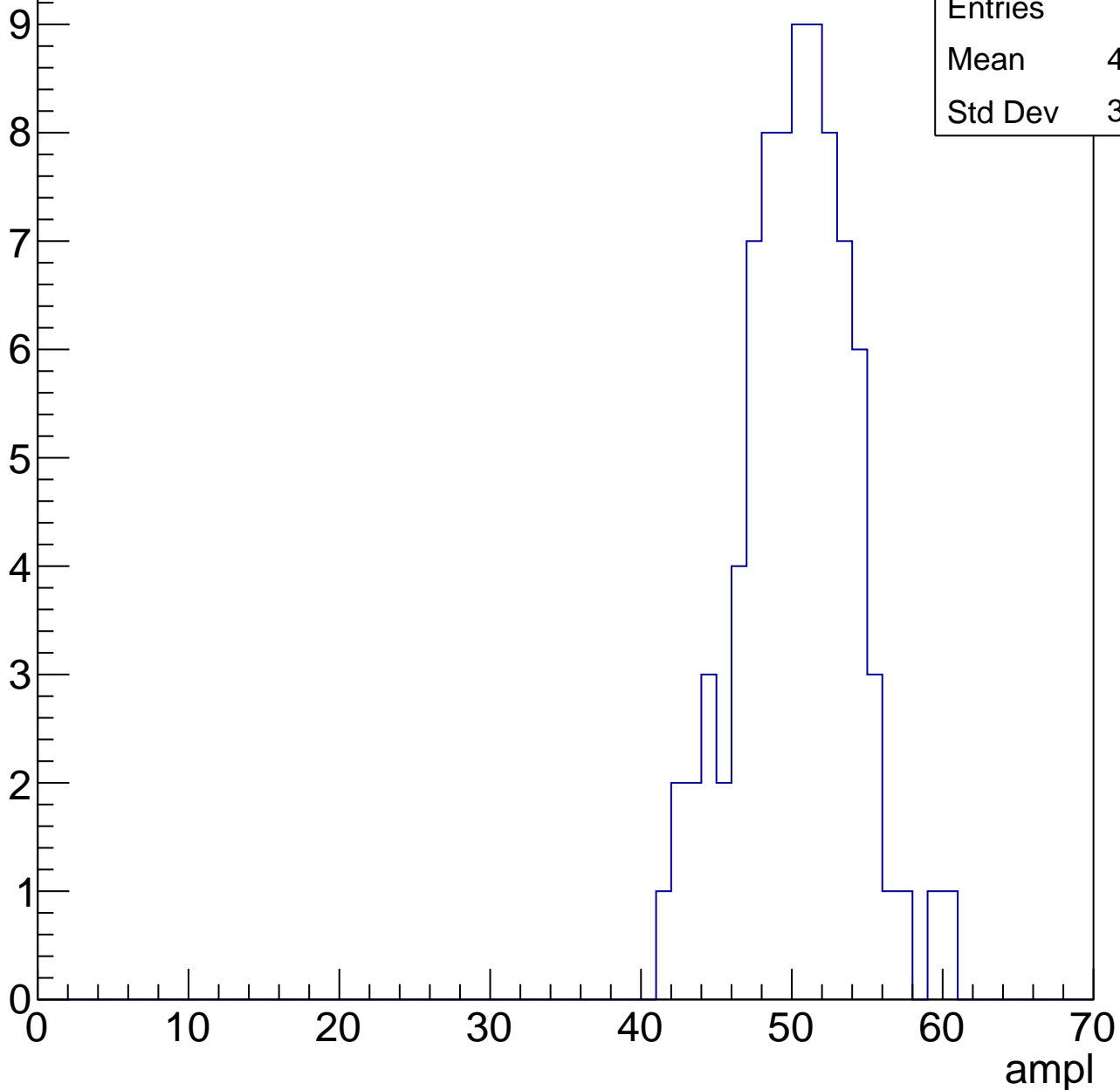


# B1L102S, U20-ch19, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

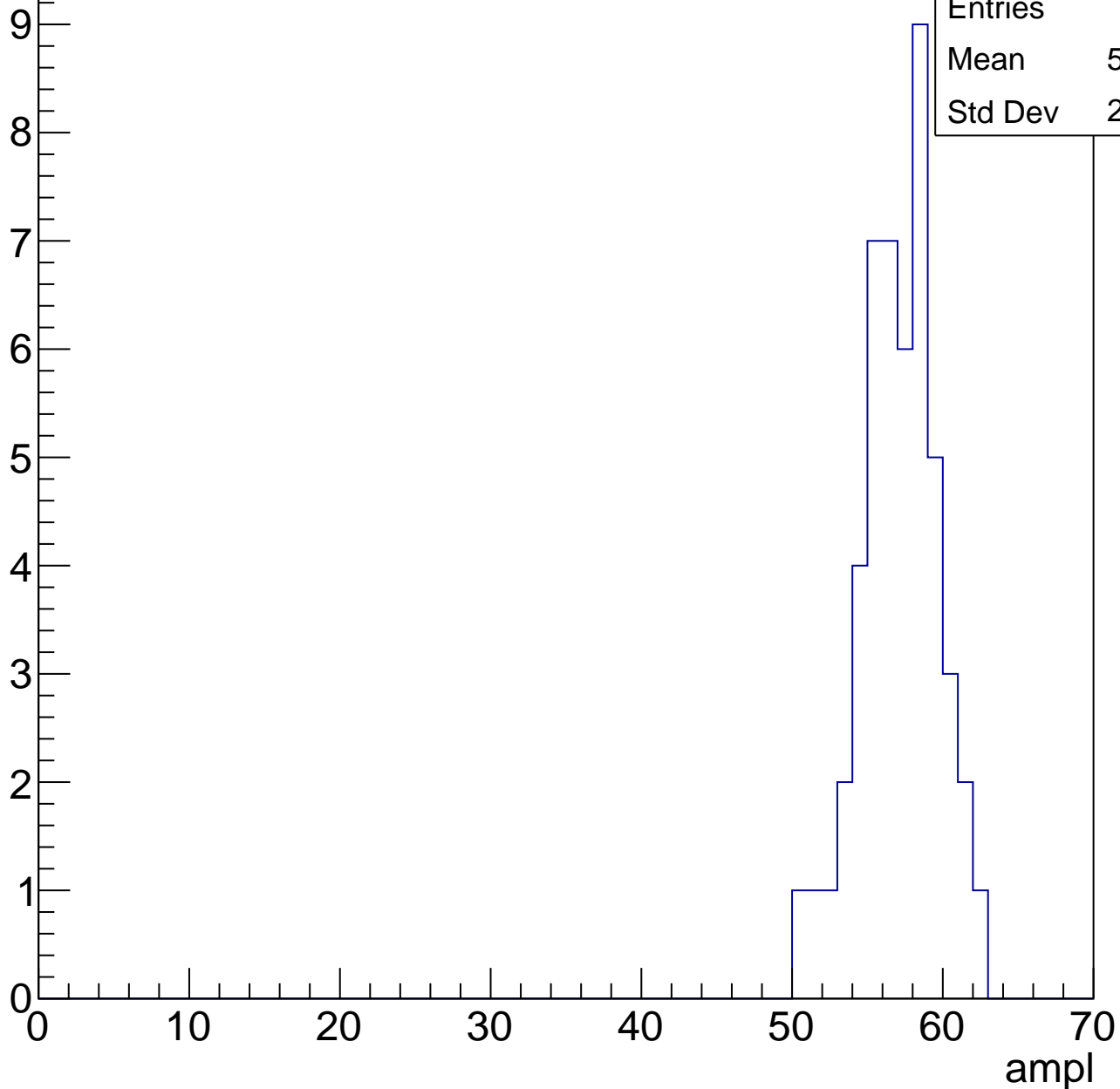
Entries	83
Mean	49.87
Std Dev	3.757



# B1L102S, U20-ch19, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

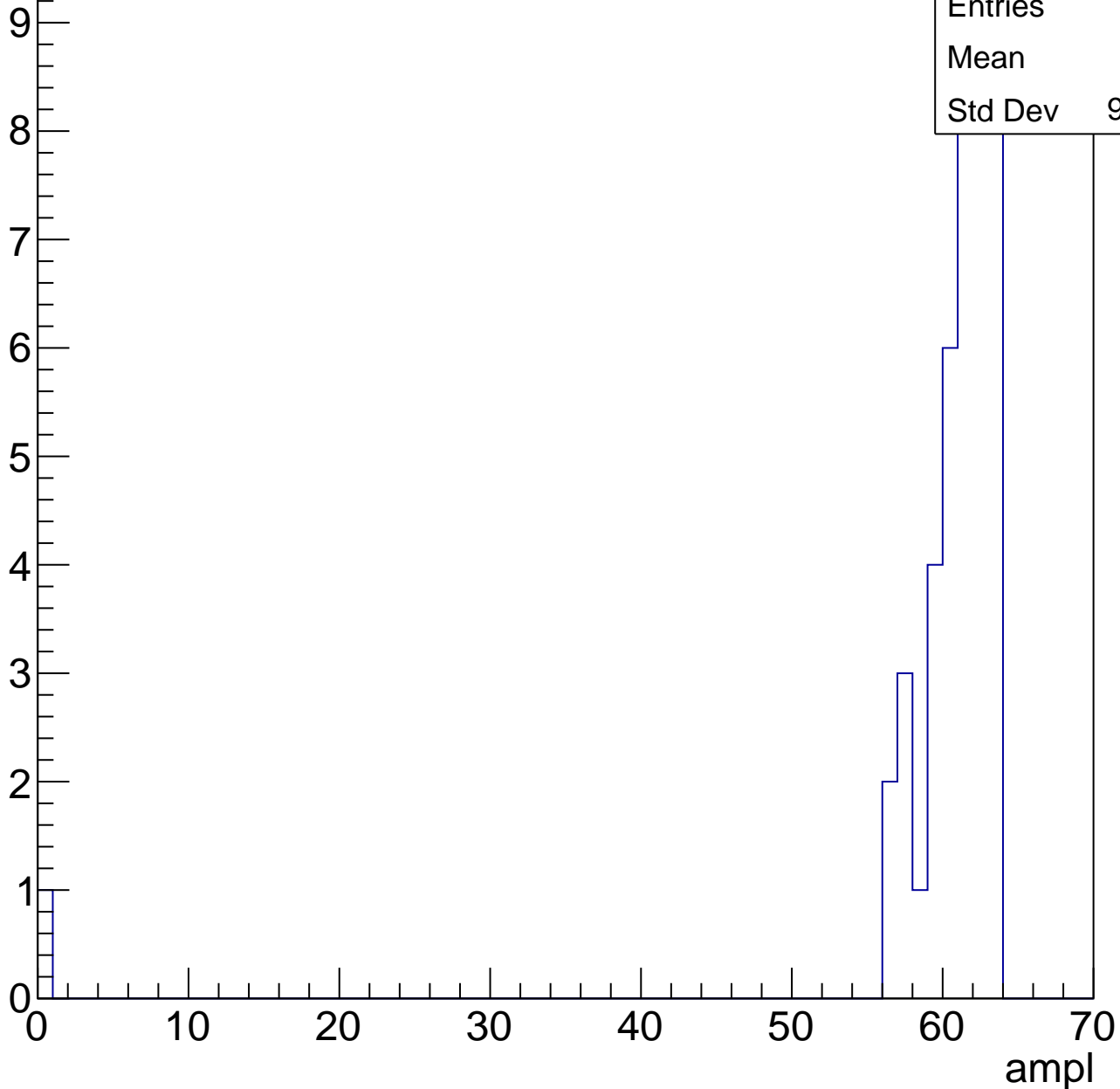
Entry



# B1L102S, U20-ch19, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch19, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U20-ch19, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	11
Std Dev	11

# B1L102S, U20-ch20, adc0

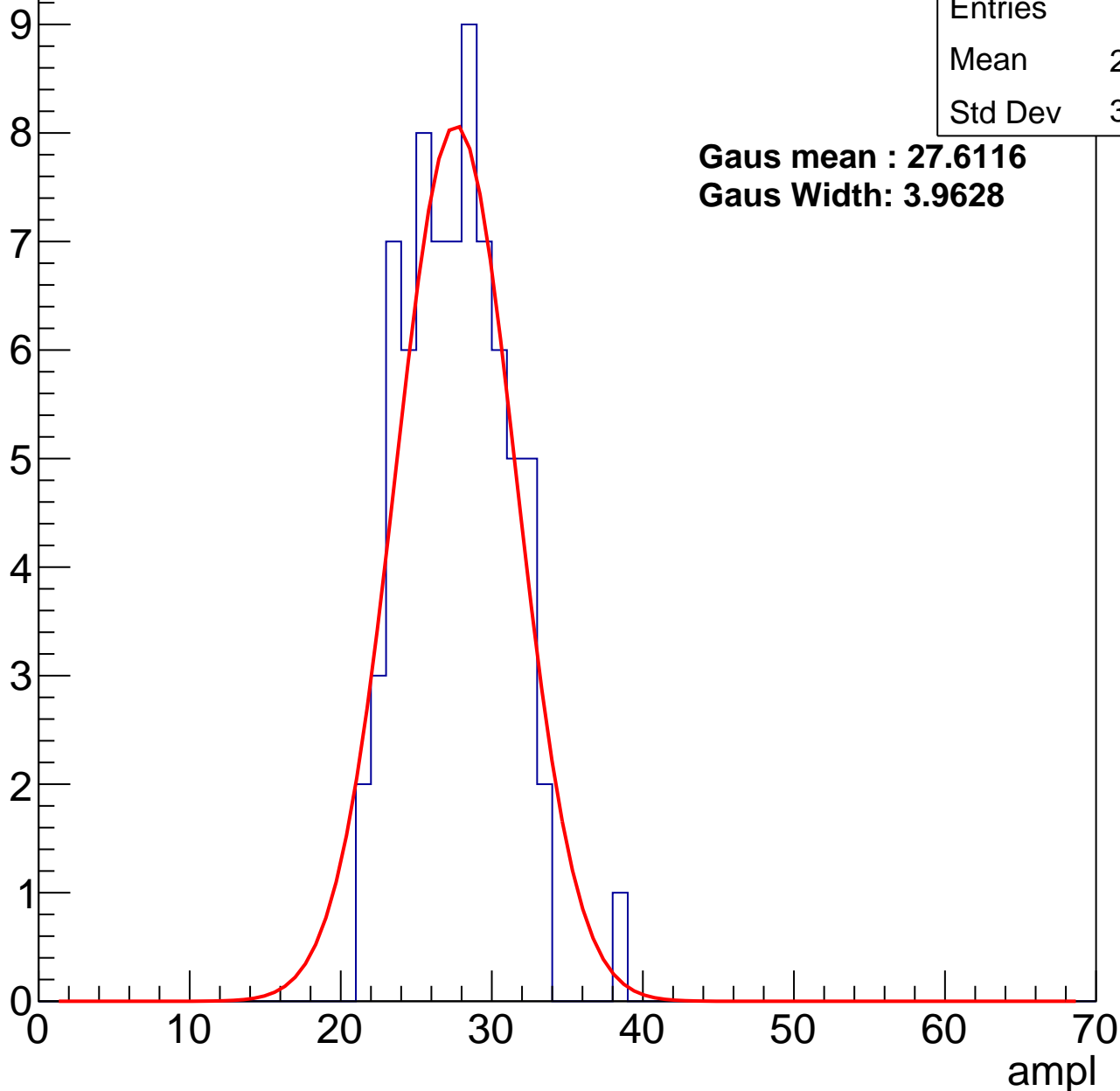
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	27.17
Std Dev	3.344

**Gaus mean : 27.6116**

**Gaus Width: 3.9628**



# B1L102S, U20-ch20, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	70
Mean	34.21
Std Dev	3.464

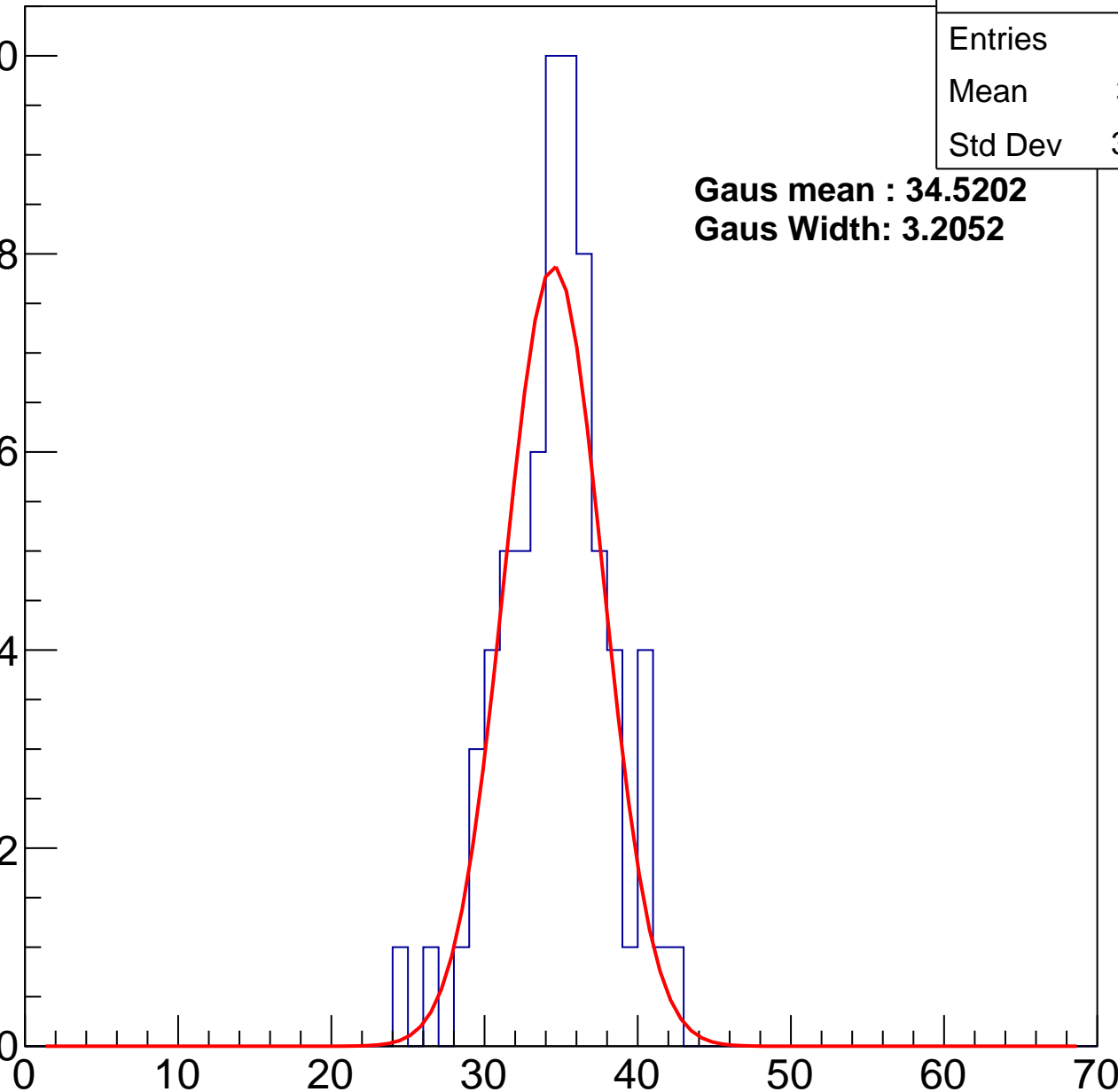
**Gaus mean : 34.5202**

**Gaus Width: 3.2052**

Entry

10  
8  
6  
4  
2  
0

ampl



# B1L102S, U20-ch20, adc2

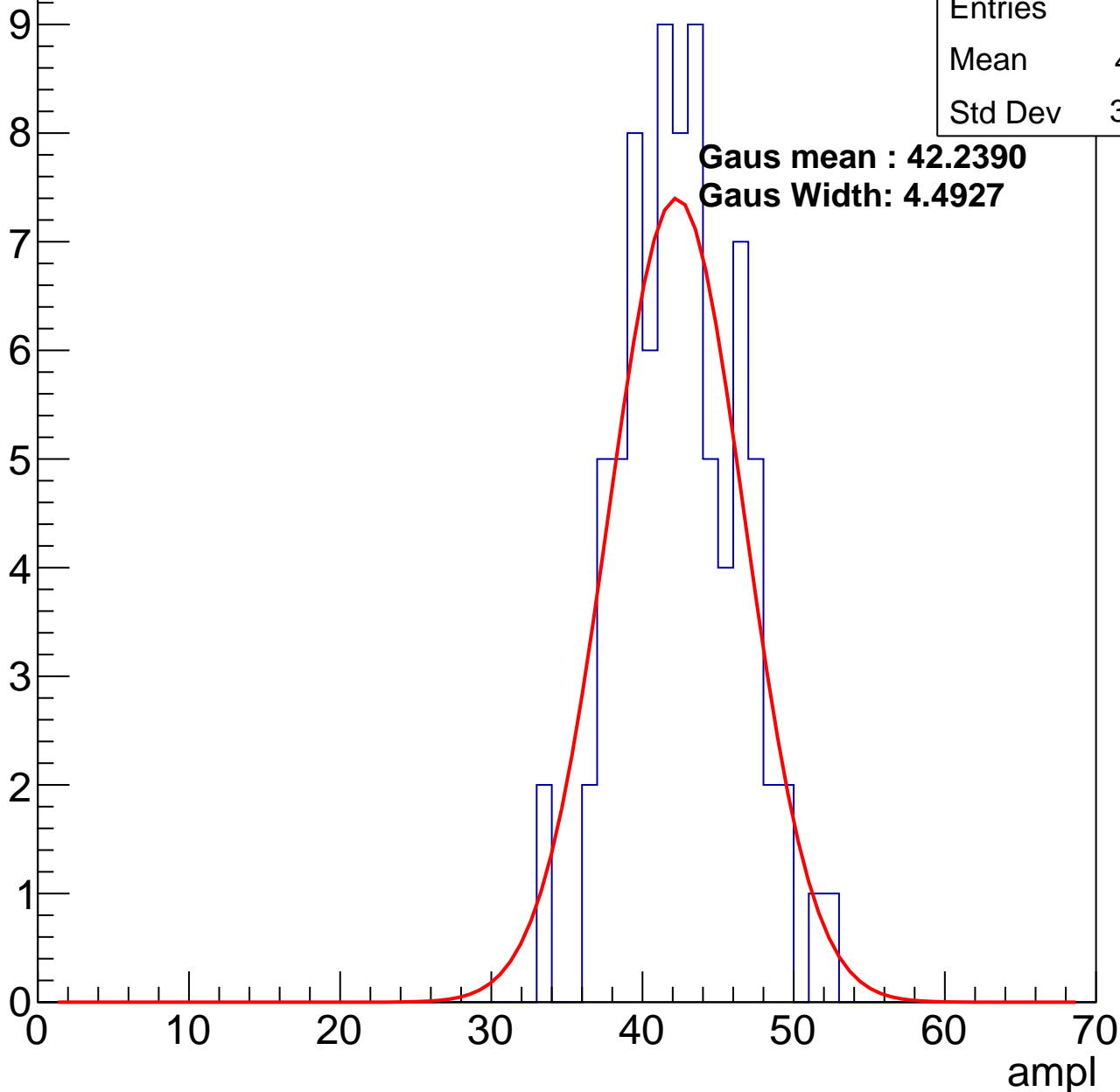
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	81
Mean	42.11
Std Dev	3.843

**Gaus mean : 42.2390**

**Gaus Width: 4.4927**

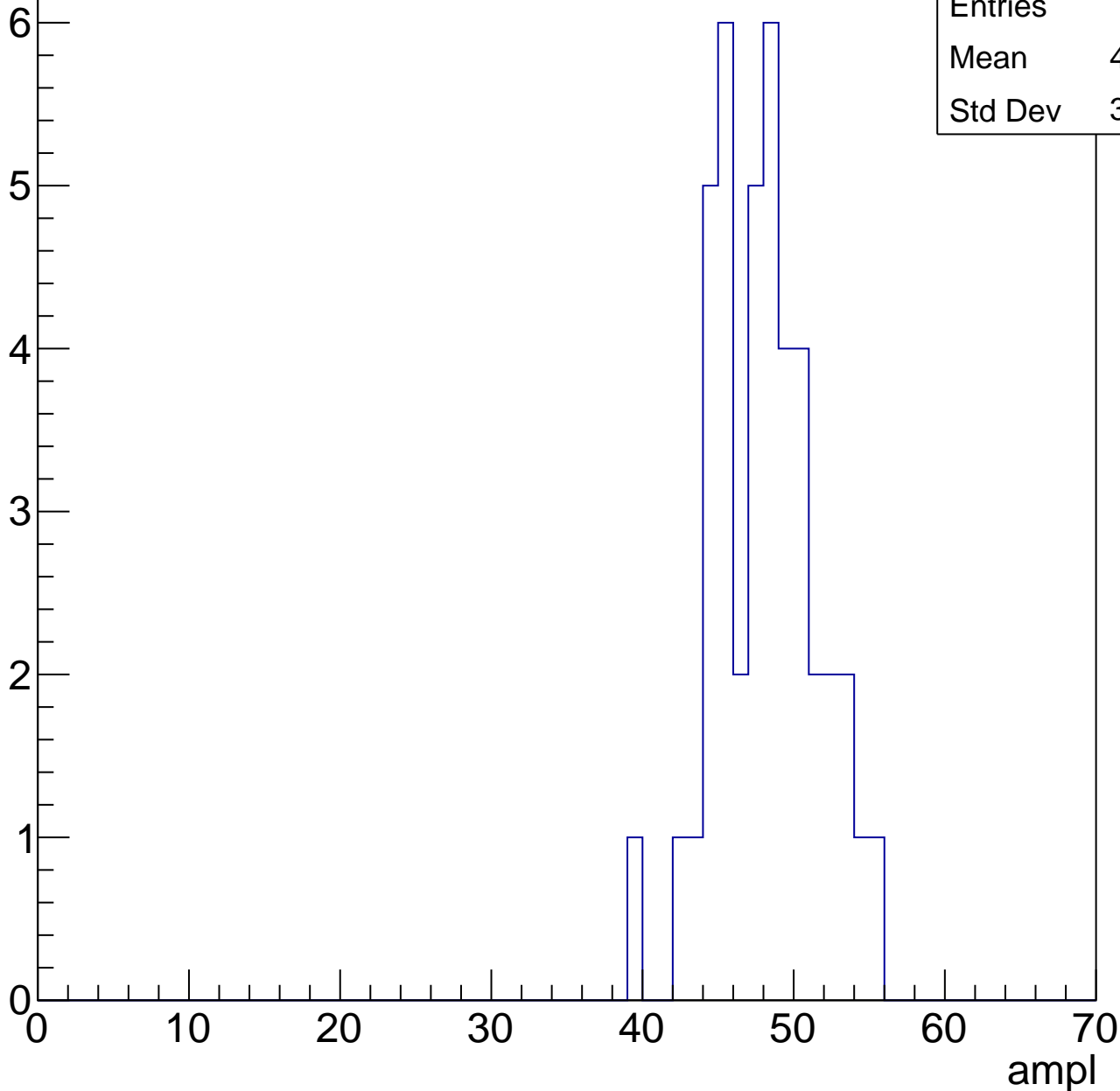


# B1L102S, U20-ch20, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	43
Mean	47.58
Std Dev	3.364

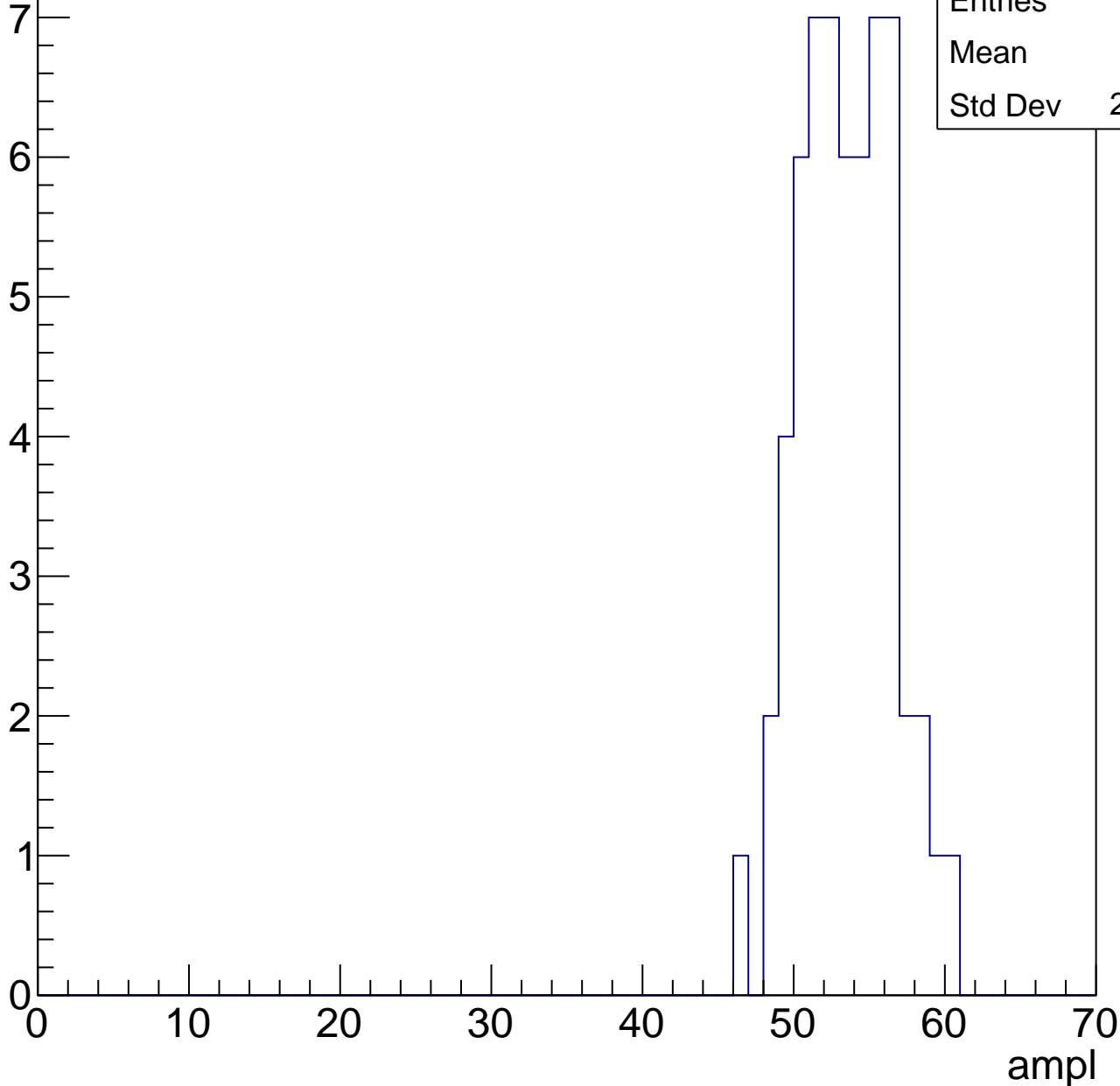


# B1L102S, U20-ch20, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

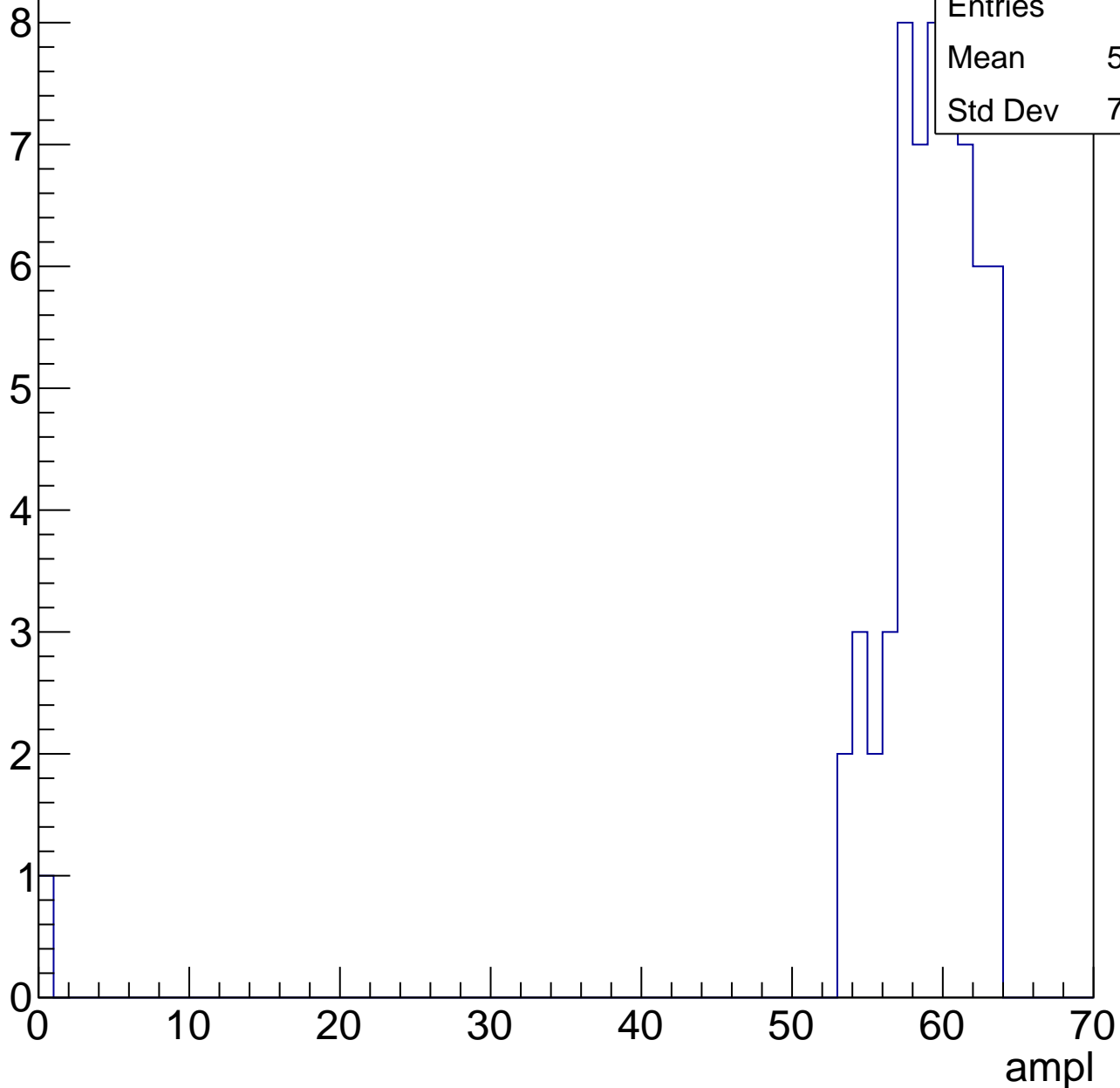
Entries	59
Mean	53
Std Dev	2.957



# B1L102S, U20-ch20, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch20, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

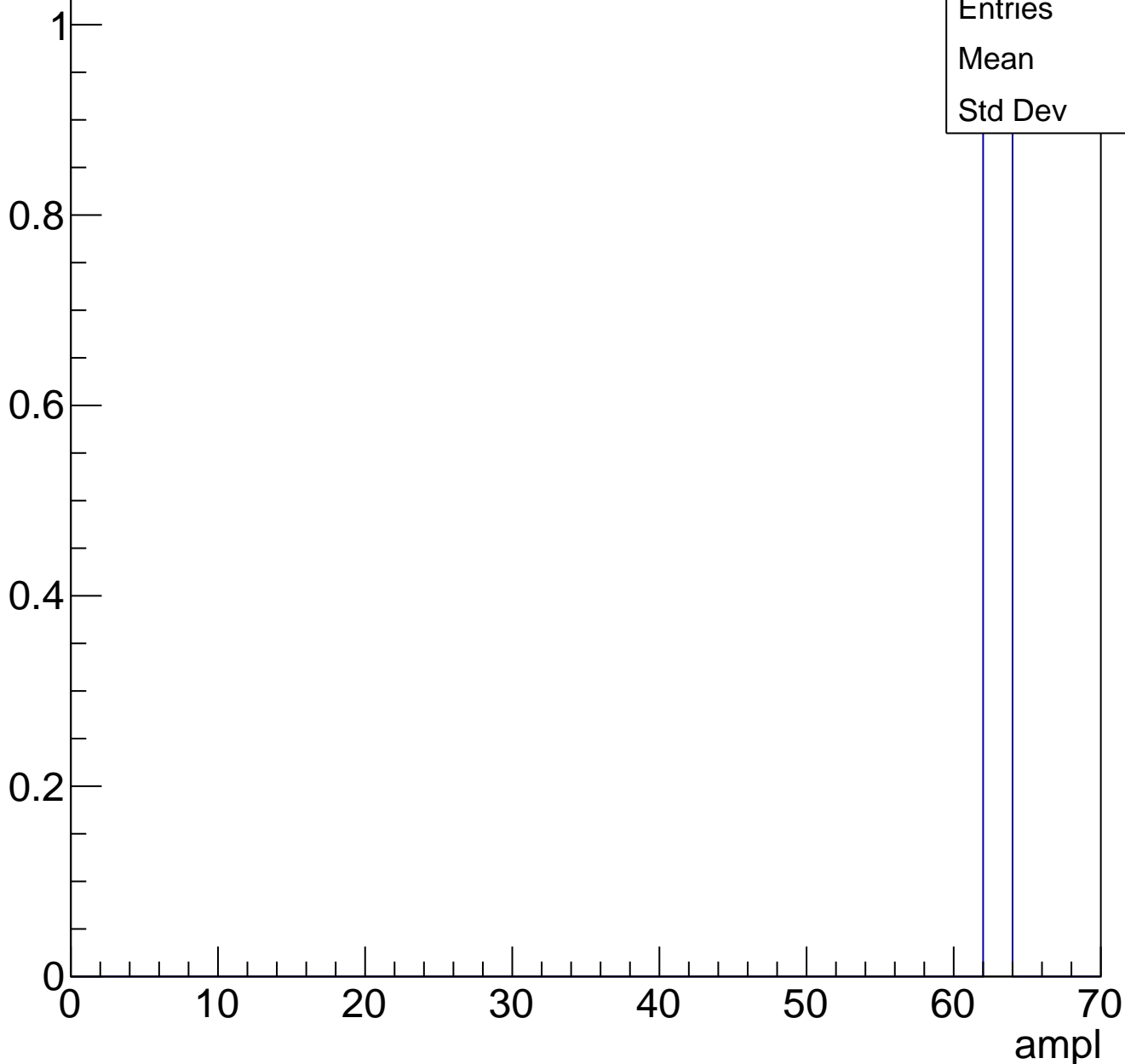
Entries	12
Mean	61.25
Std Dev	1.534



# B1L102S, U20-ch20, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch21, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	78
Mean	27.97
Std Dev	5.491

**Gaus mean : 29.3112**

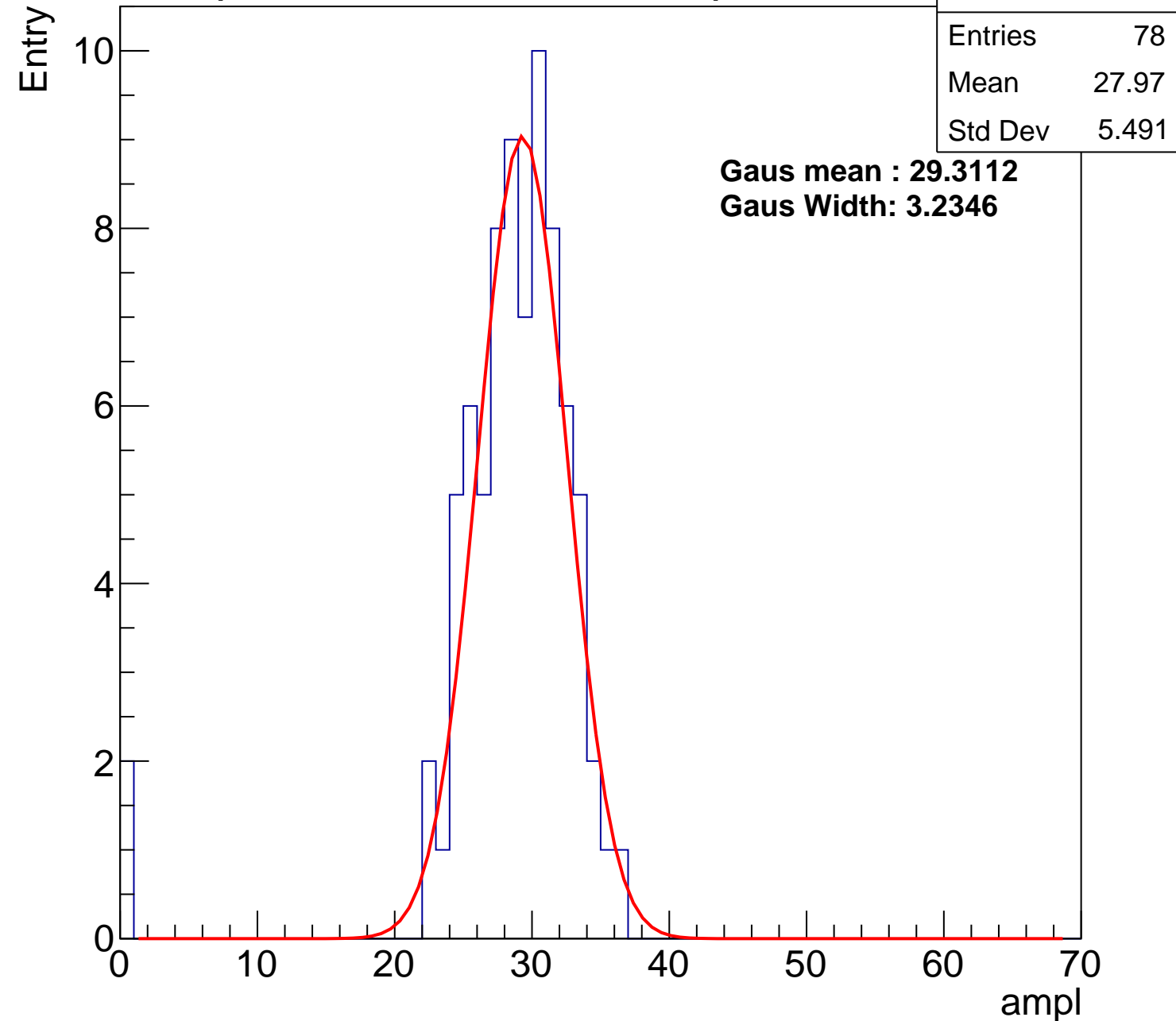
**Gaus Width: 3.2346**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U20-ch21, adc1

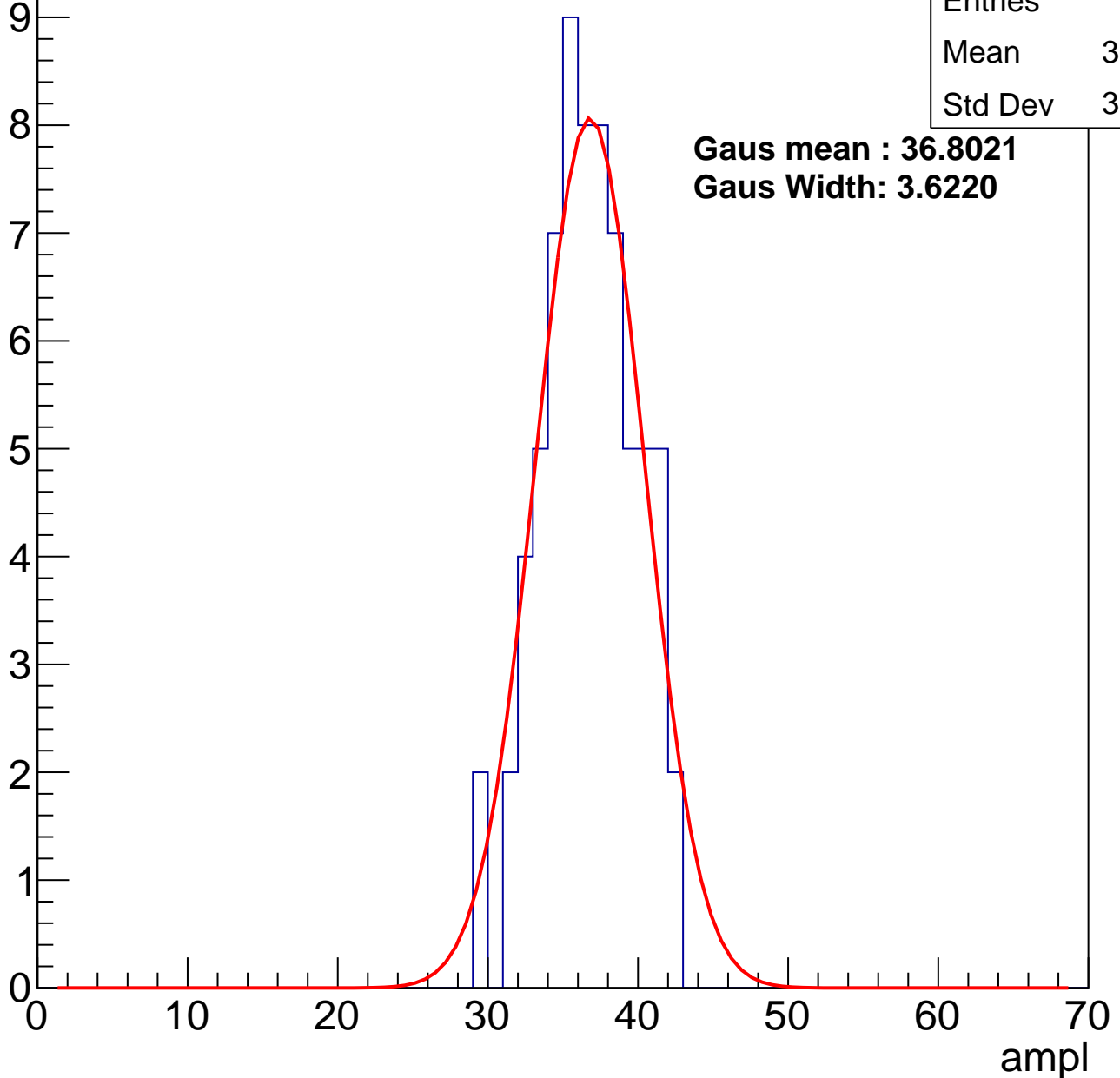
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	36.23
Std Dev	3.065

**Gaus mean : 36.8021**

**Gaus Width: 3.6220**



# B1L102S, U20-ch21, adc2

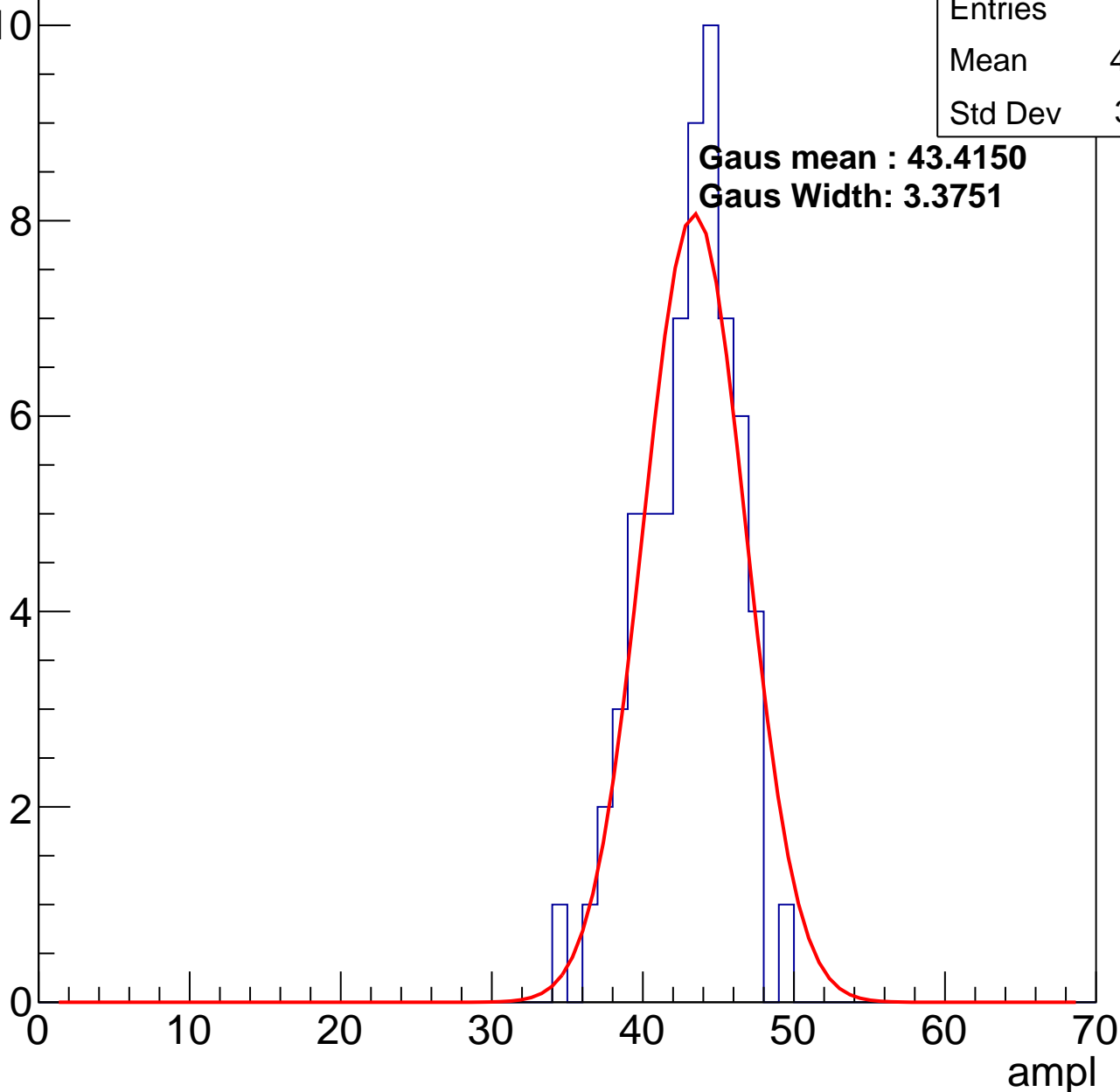
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	42.53
Std Dev	3.031

**Gaus mean : 43.4150**

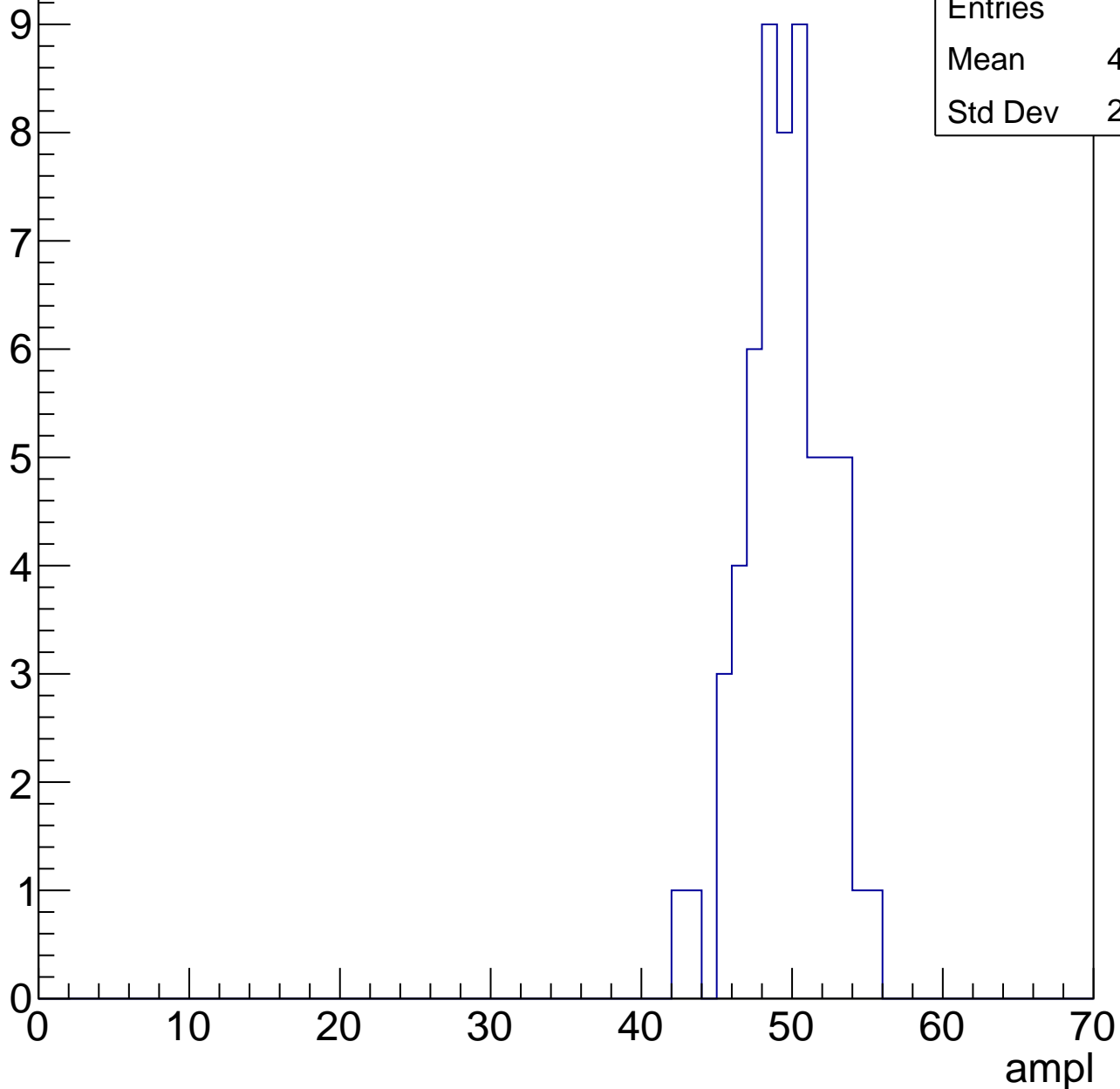
**Gaus Width: 3.3751**



# B1L102S, U20-ch21, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

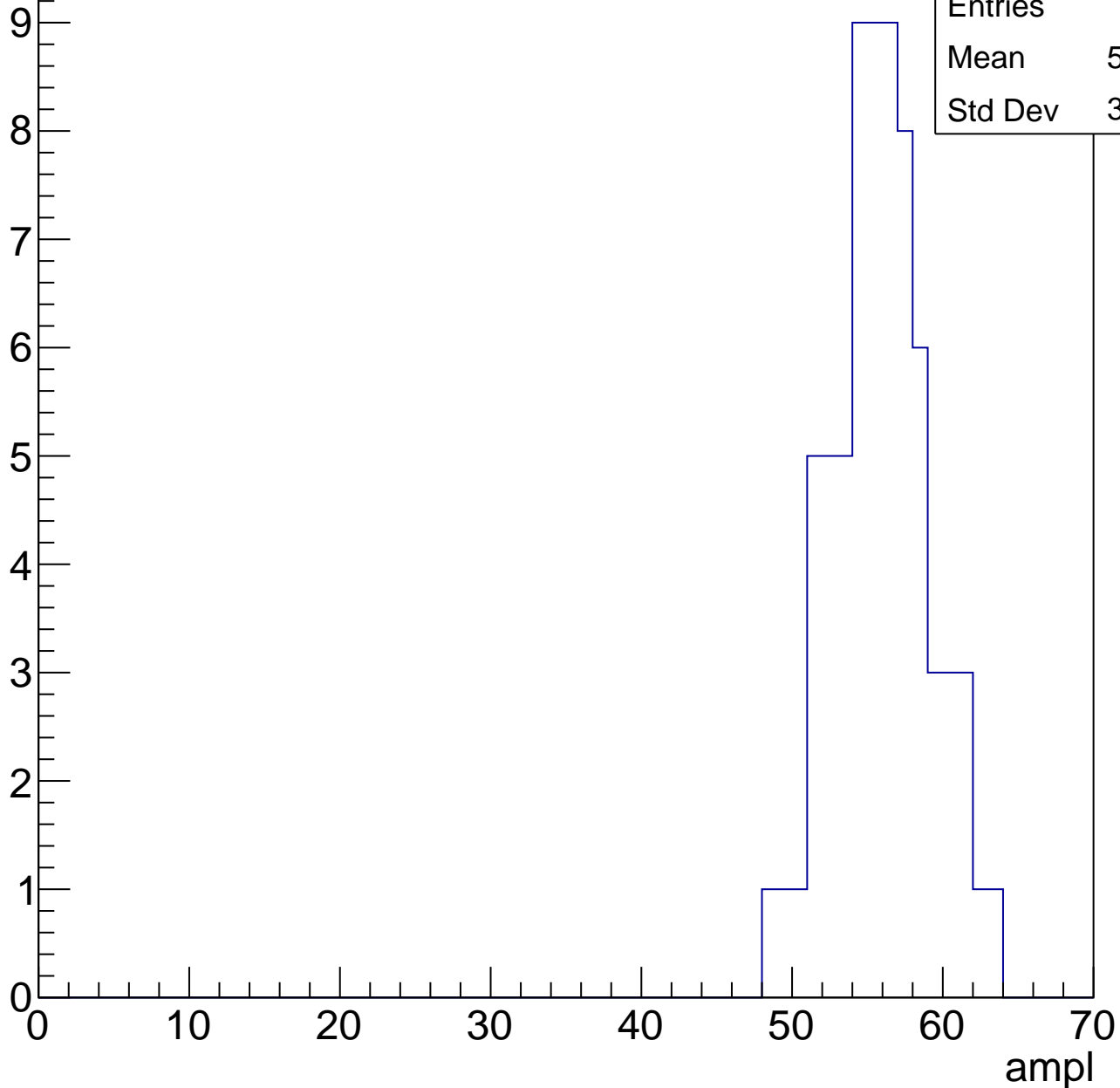


Entries	58
Mean	49.12
Std Dev	2.679

# B1L102S, U20-ch21, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



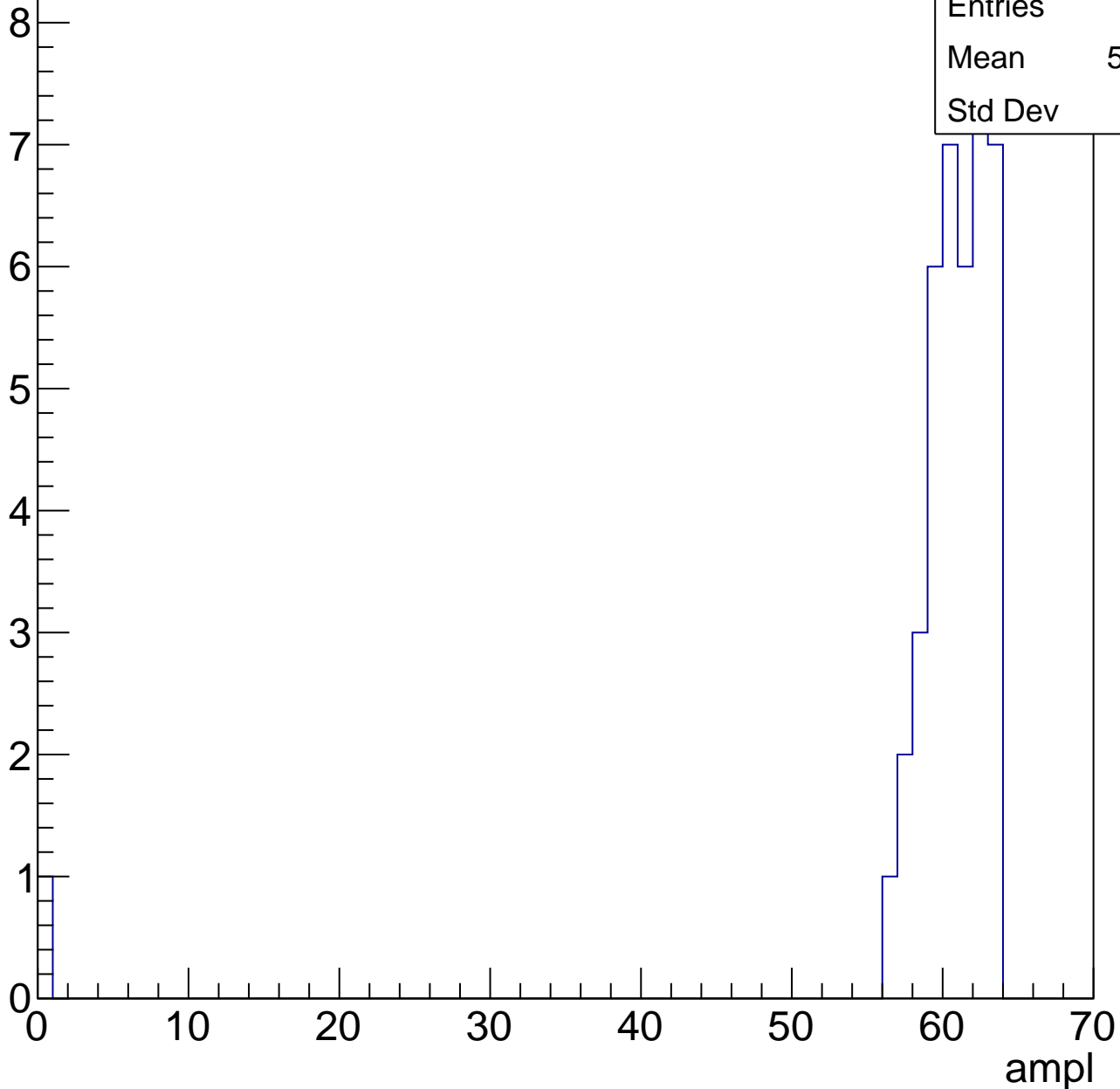
Entries	70
Mean	55.44
Std Dev	3.138

# B1L102S, U20-ch21, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

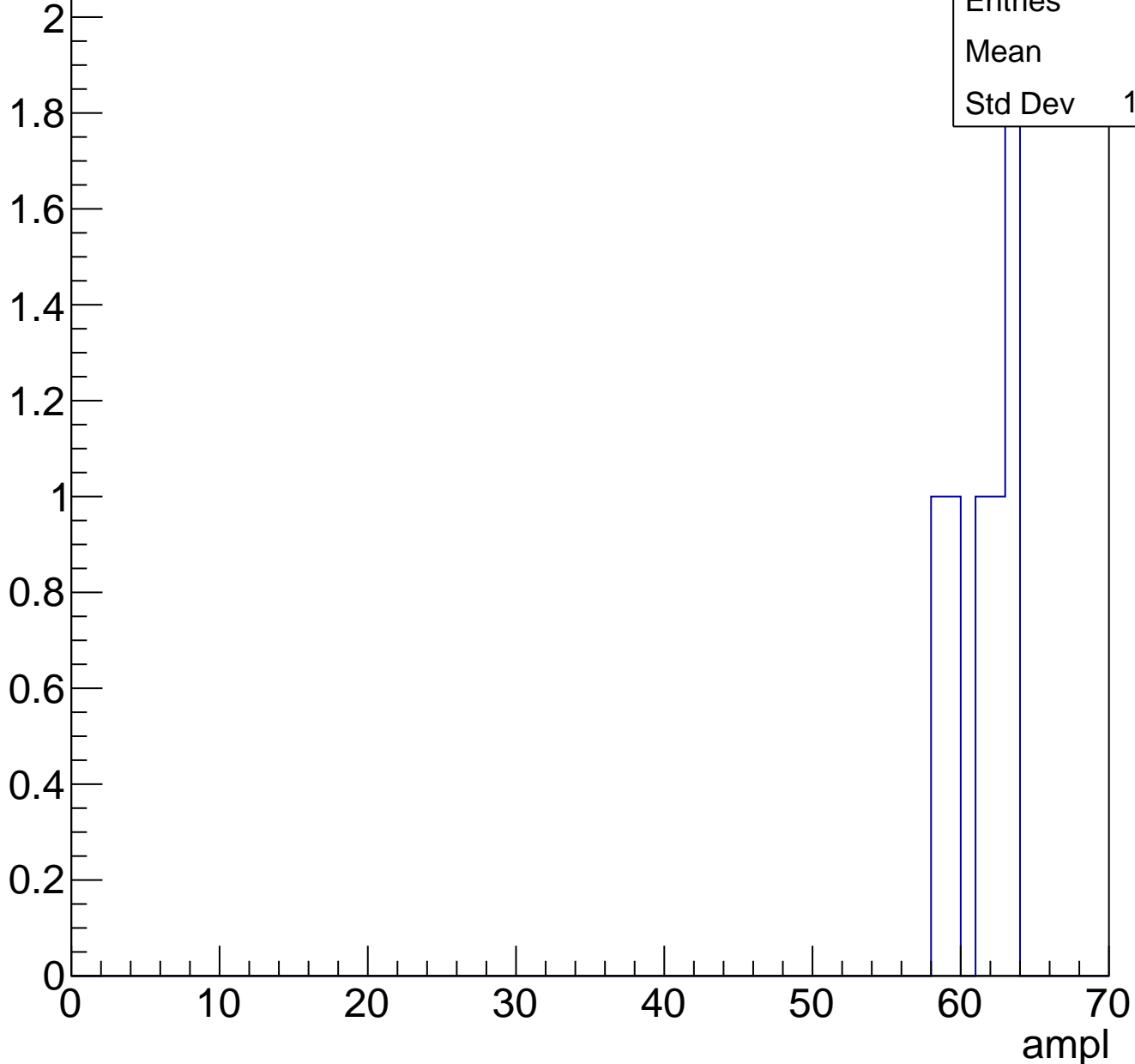
Entries	41
Mean	59.05
Std Dev	9.52



# B1L102S, U20-ch21, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U20-ch21, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	20
Std Dev	0

# B1L102S, U20-ch22, adc0

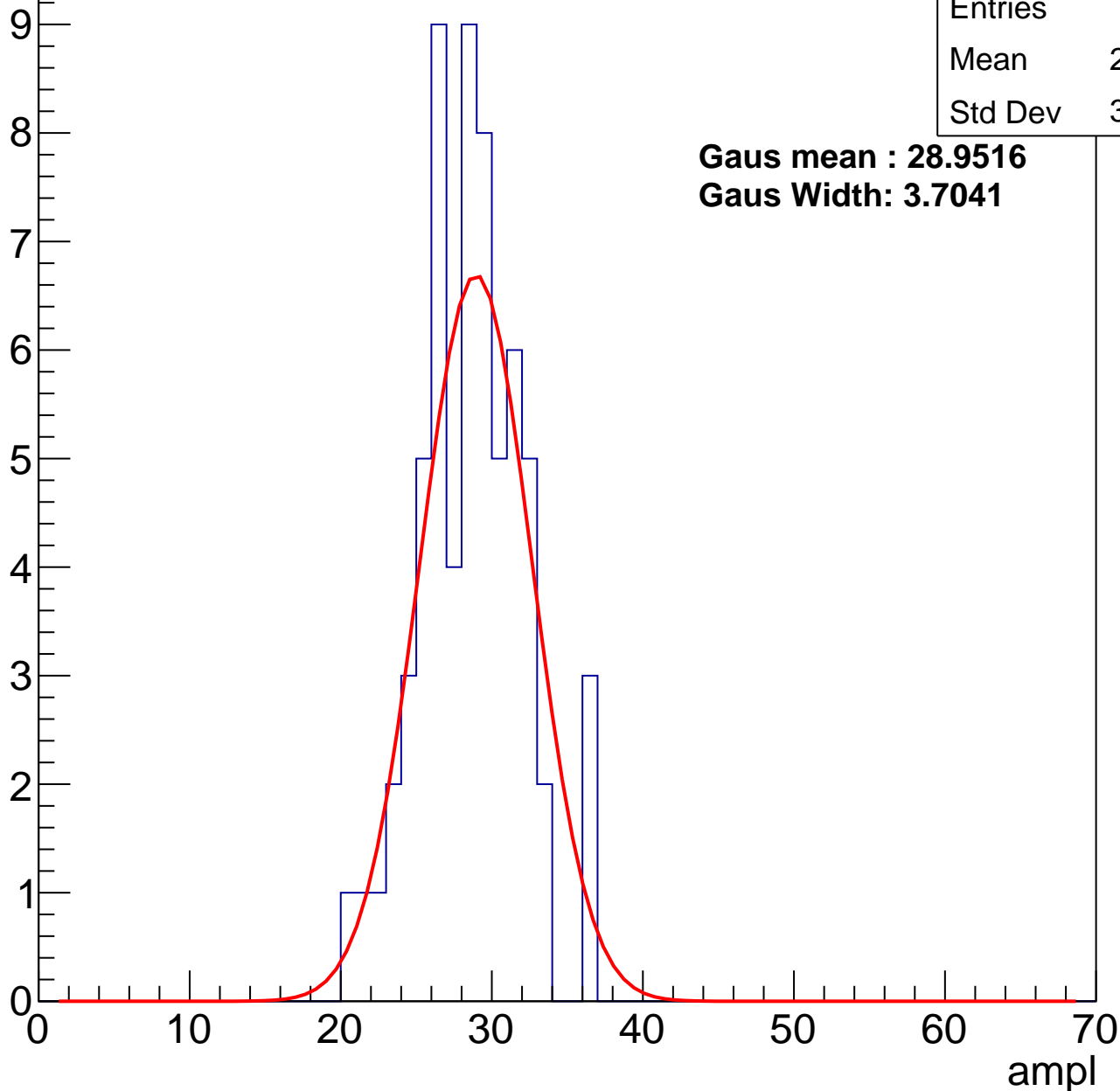
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	28.16
Std Dev	3.388

**Gaus mean : 28.9516**

**Gaus Width: 3.7041**



# B1L102S, U20-ch22, adc1

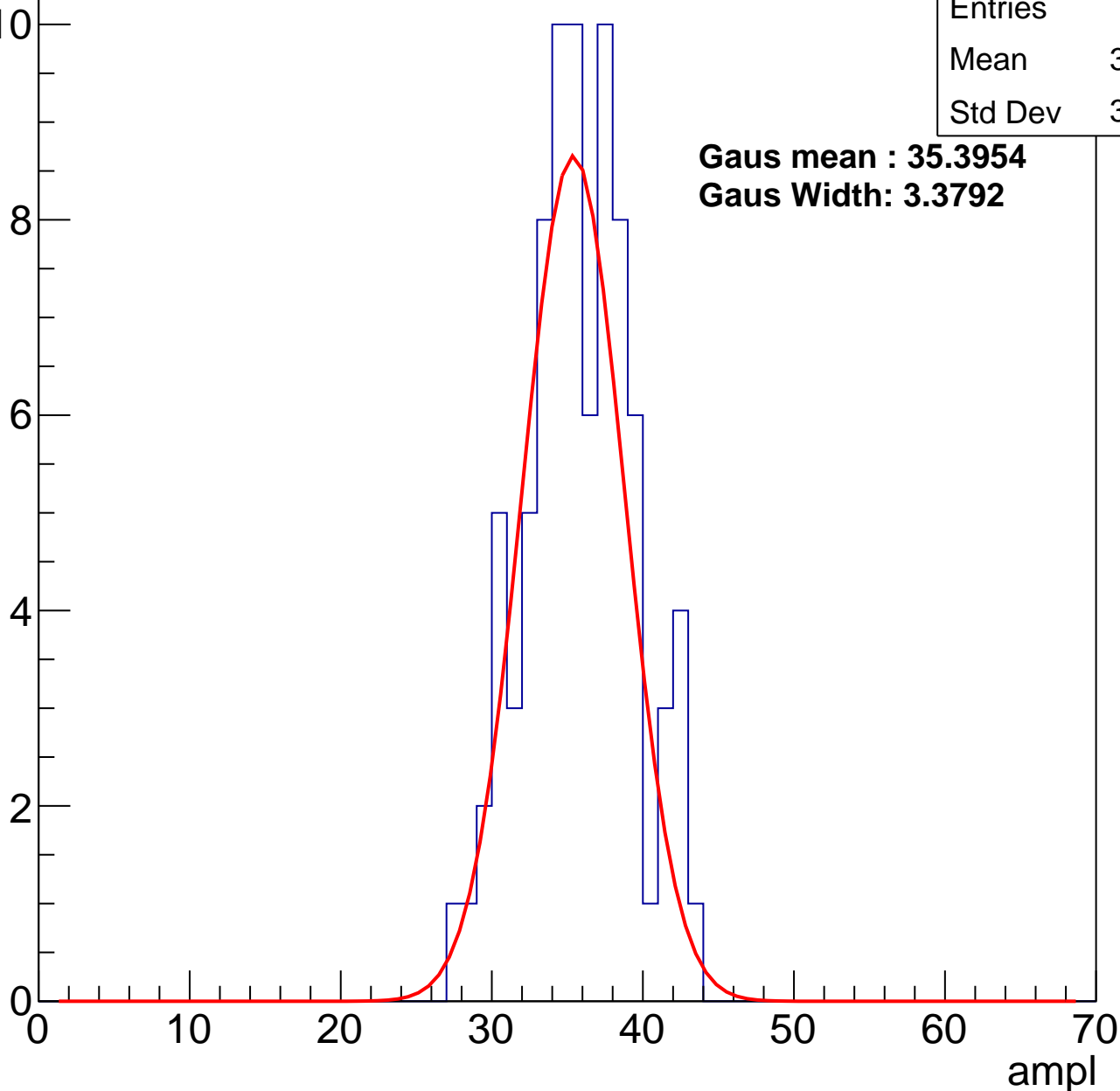
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	84
Mean	35.33
Std Dev	3.523

**Gaus mean : 35.3954**

**Gaus Width: 3.3792**



# B1L102S, U20-ch22, adc2

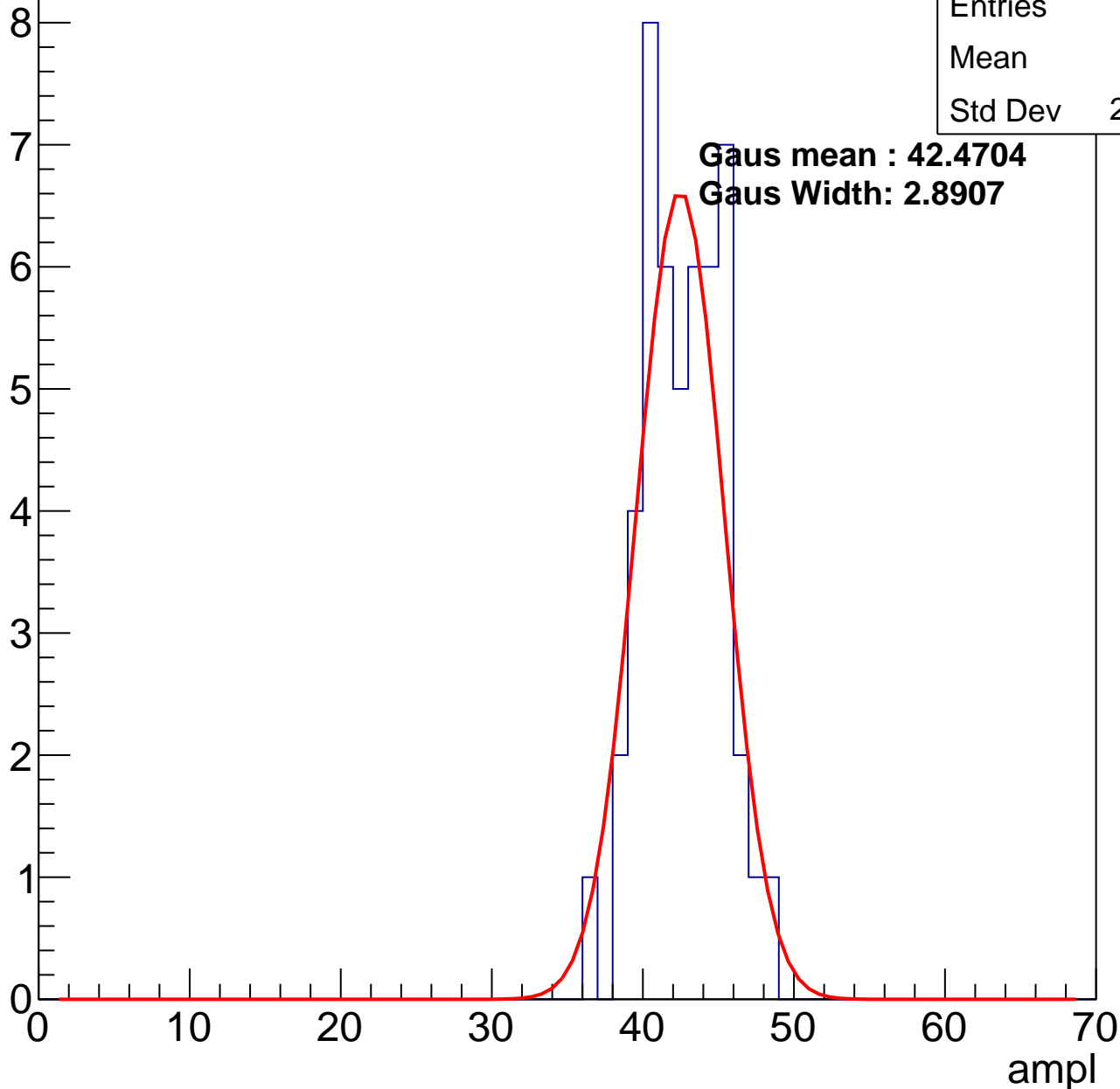
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	42.2
Std Dev	2.579

**Gaus mean : 42.4704**

**Gaus Width: 2.8907**

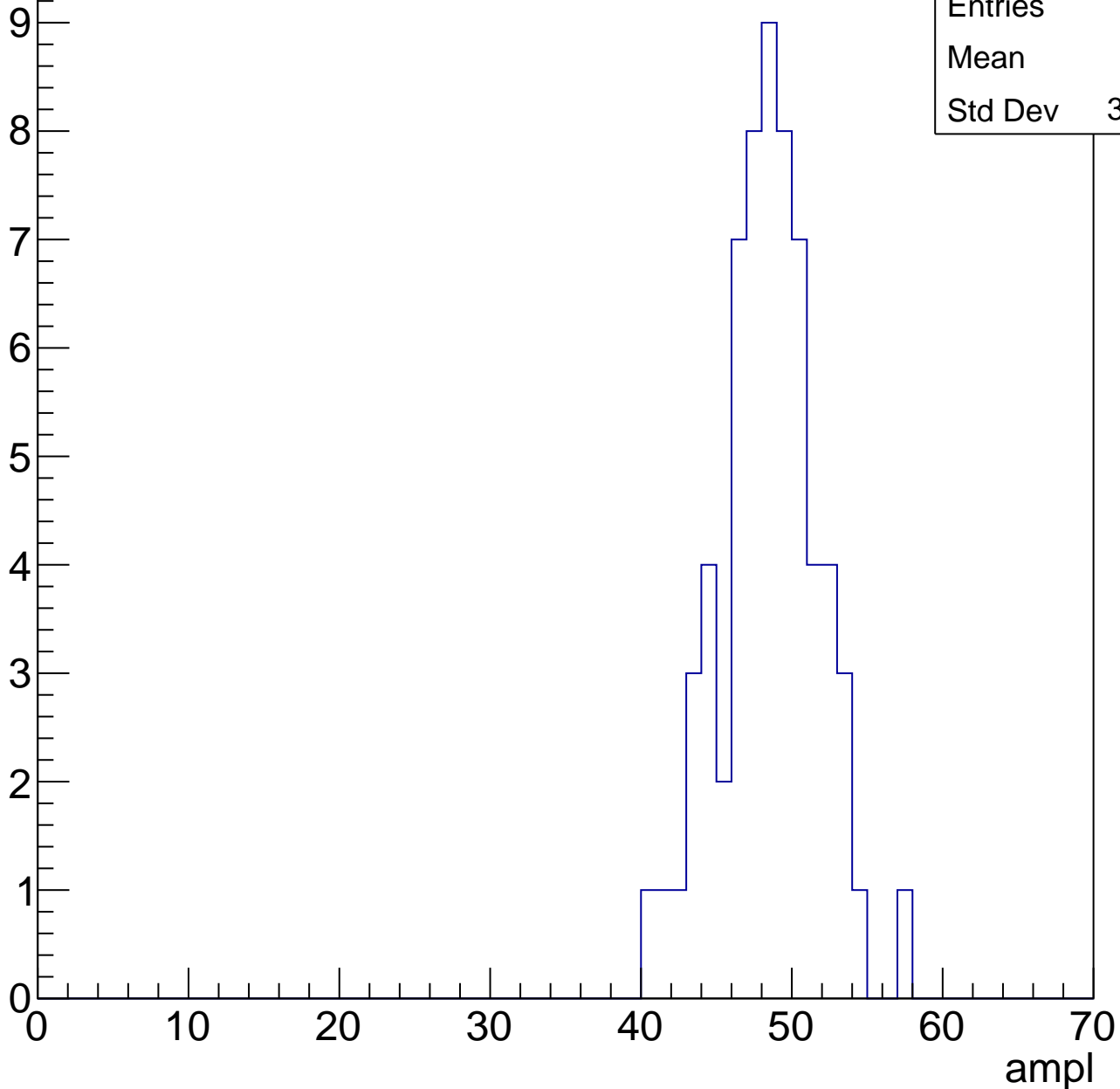


# B1L102S, U20-ch22, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	48
Std Dev	3.236

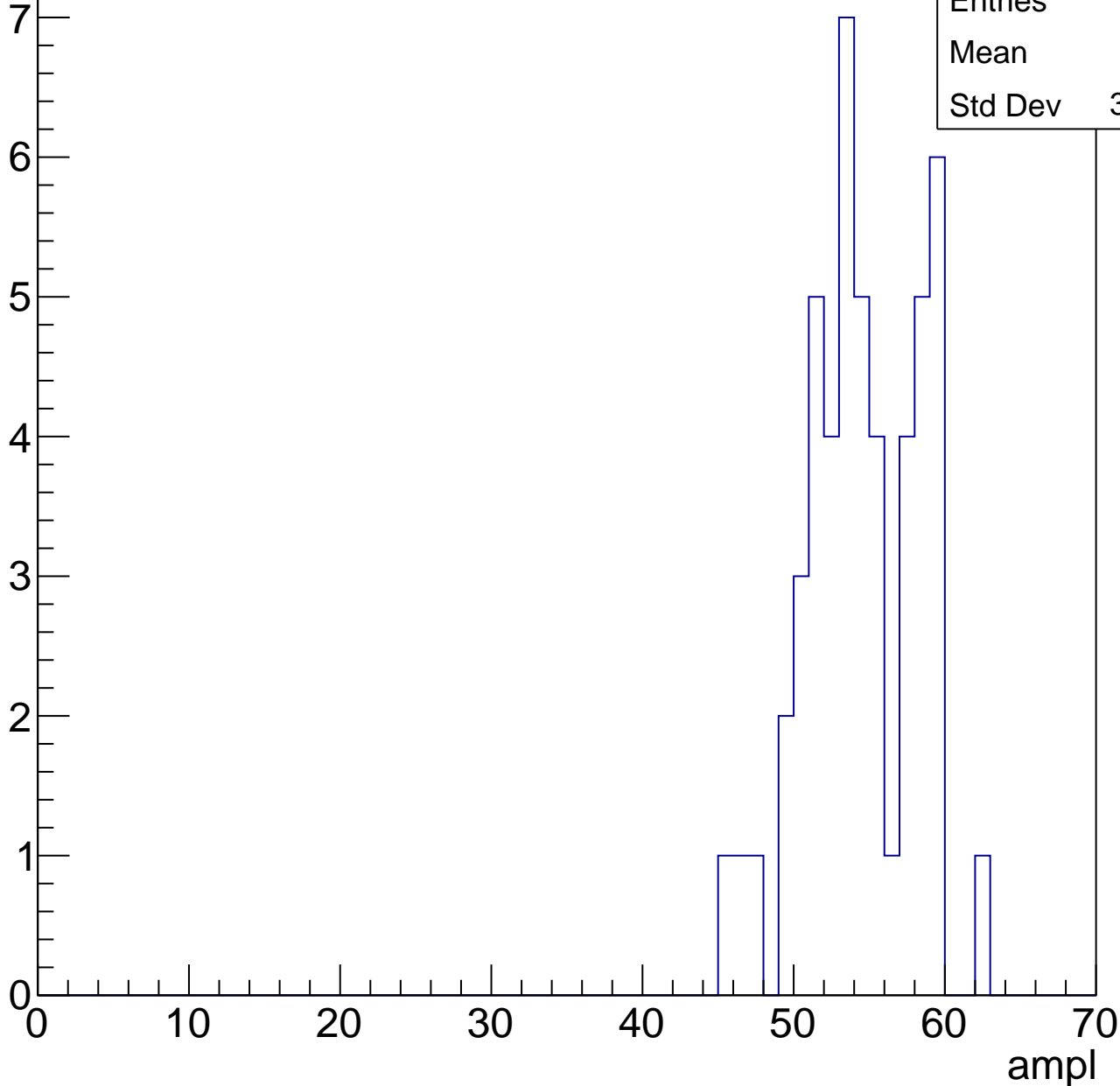


# B1L102S, U20-ch22, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	54
Std Dev	3.736

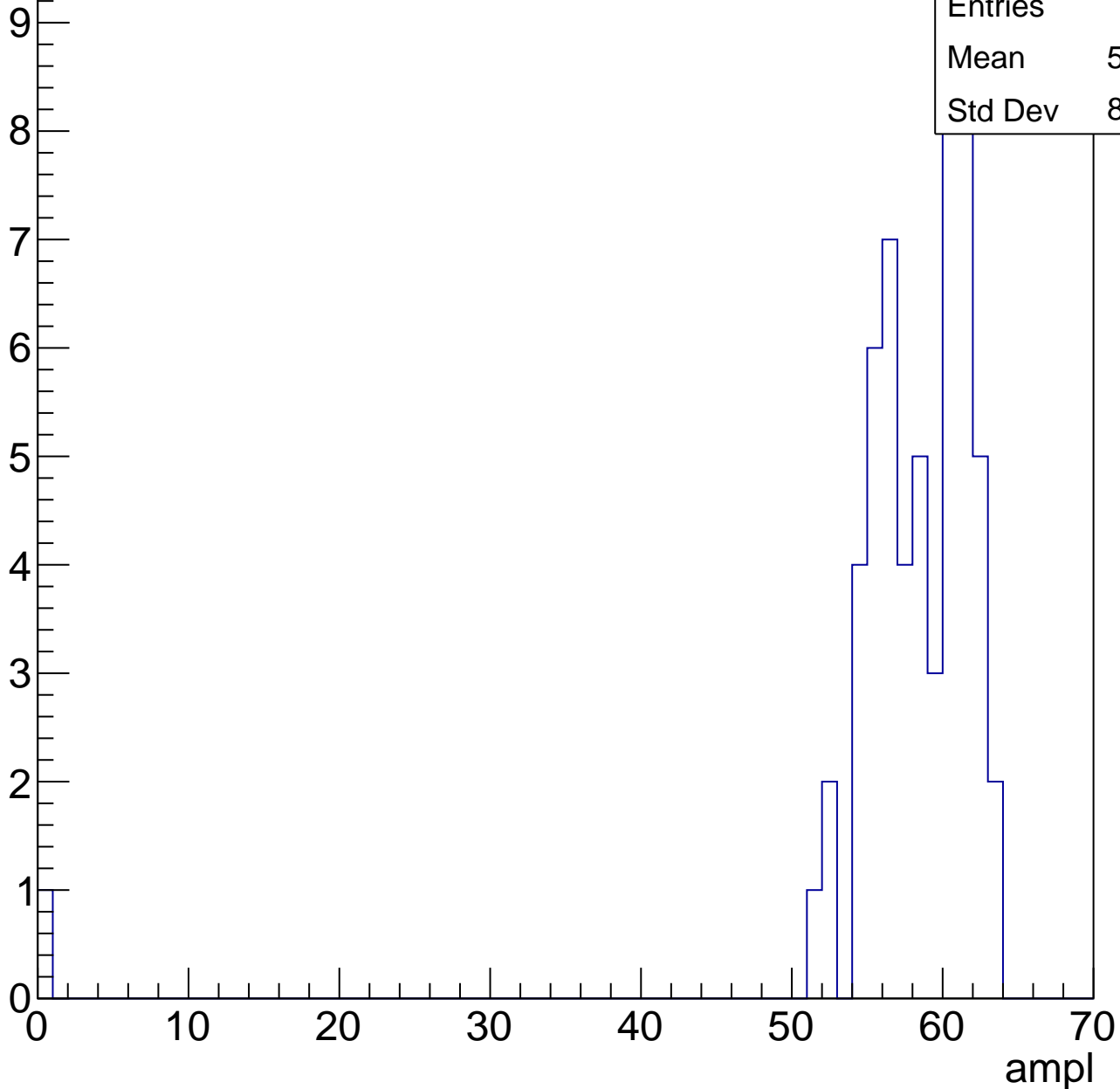


# B1L102S, U20-ch22, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	57.05
Std Dev	8.192

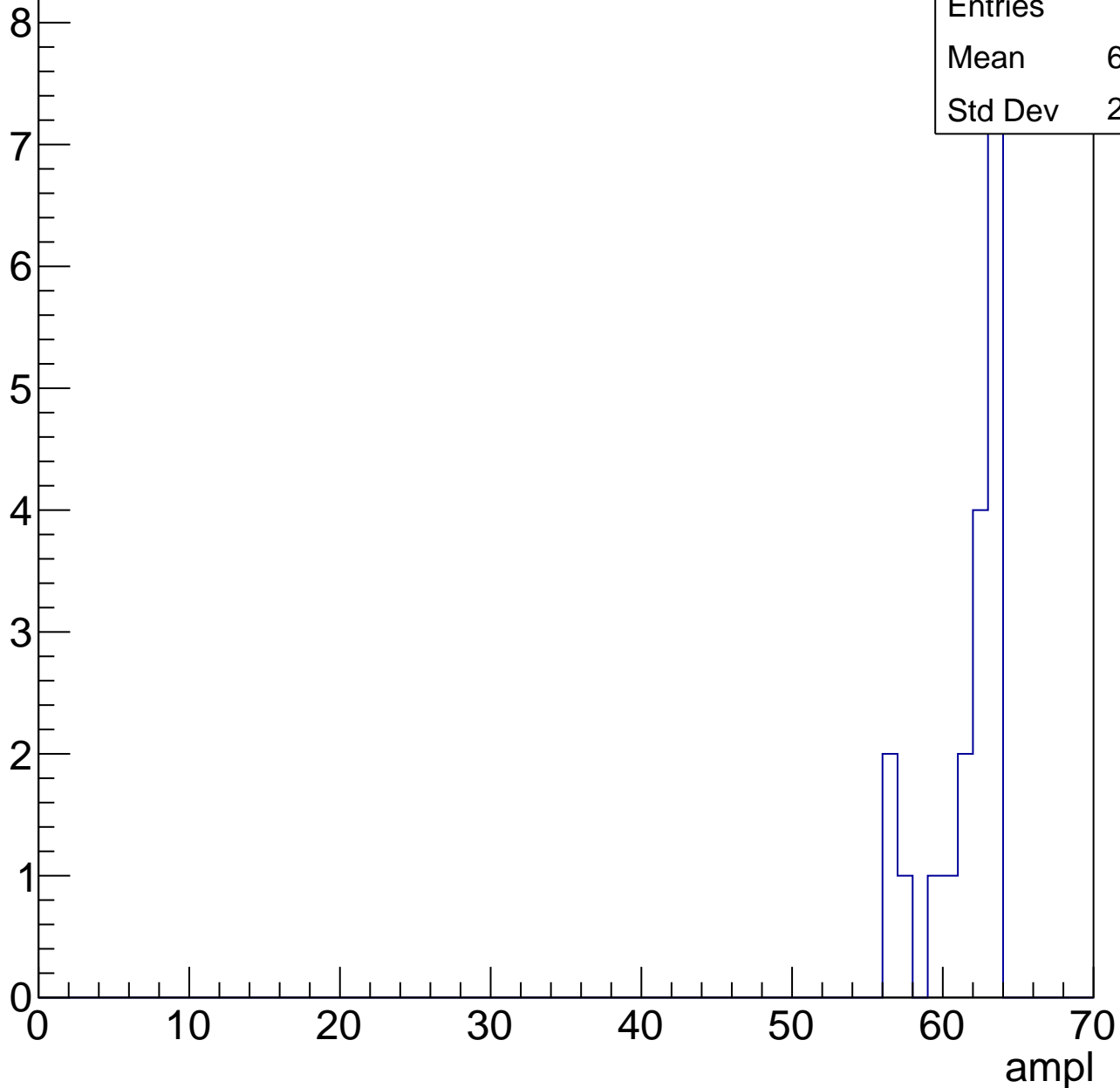


# B1L102S, U20-ch22, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	19
Mean	61.16
Std Dev	2.368





# B1L102S, U20-ch22, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L102S, U20-ch23, adc0

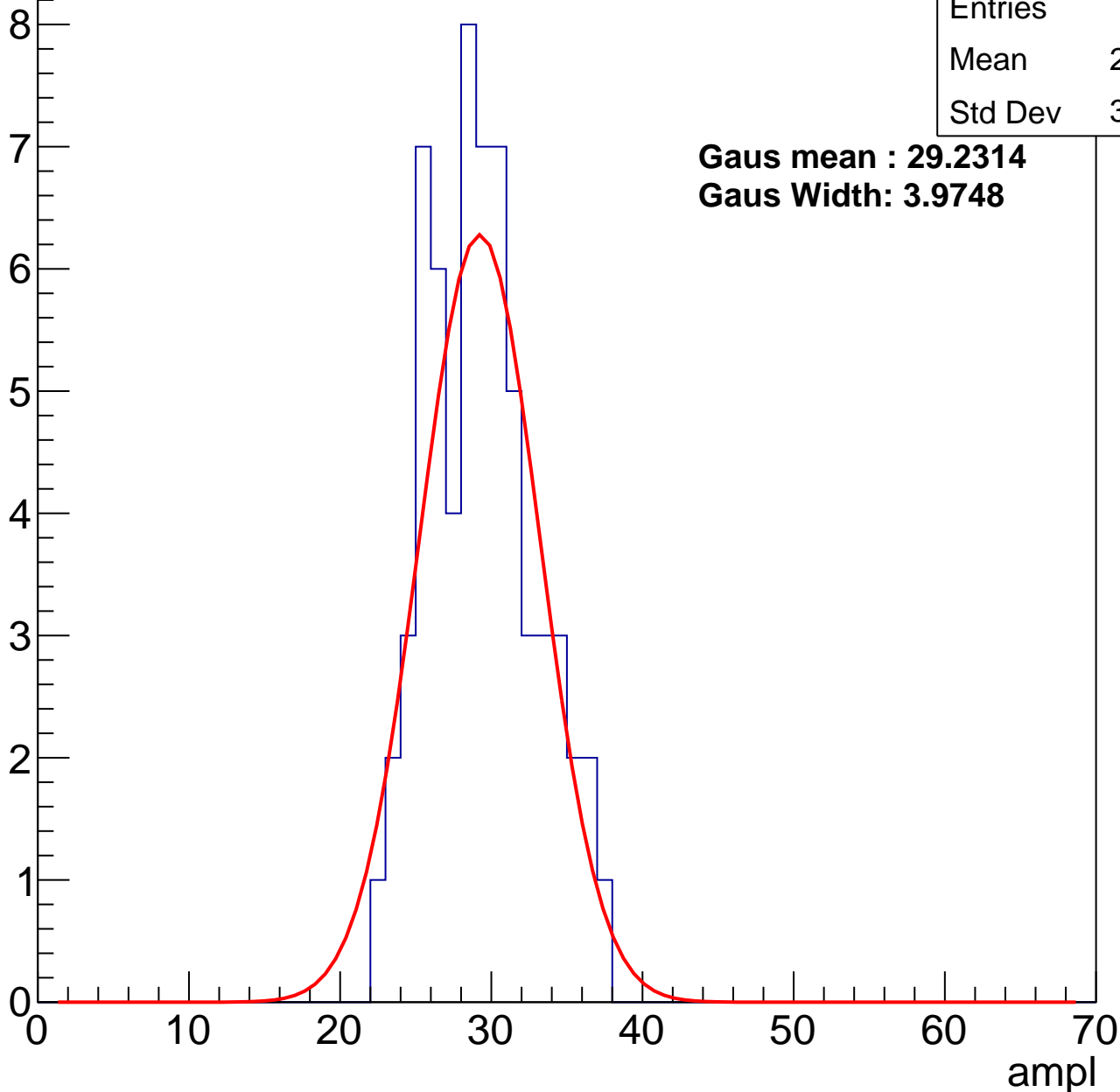
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	28.86
Std Dev	3.526

**Gaus mean : 29.2314**

**Gaus Width: 3.9748**



# B1L102S, U20-ch23, adc1

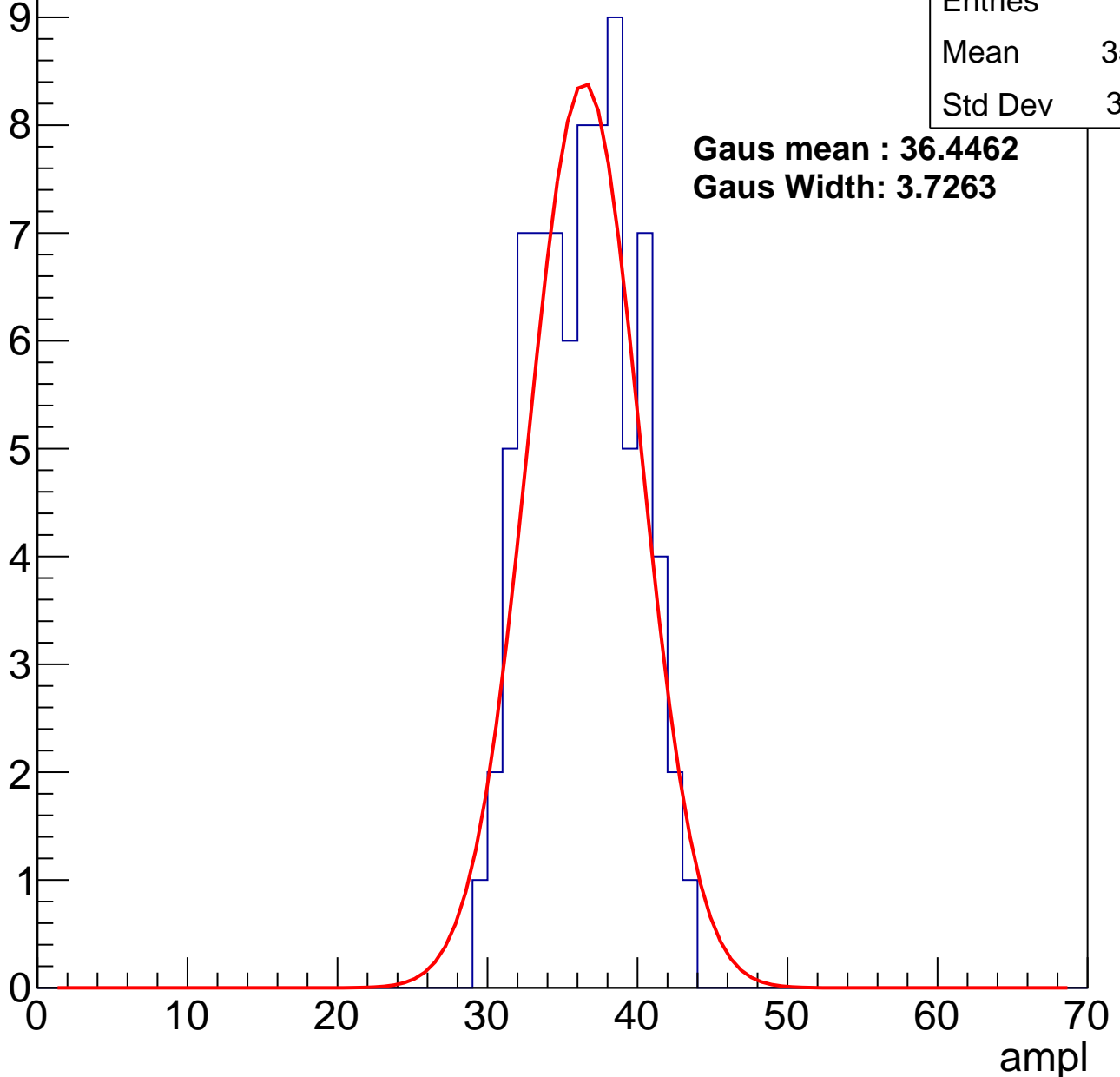
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	79
Mean	35.94
Std Dev	3.331

**Gaus mean : 36.4462**

**Gaus Width: 3.7263**



# B1L102S, U20-ch23, adc2

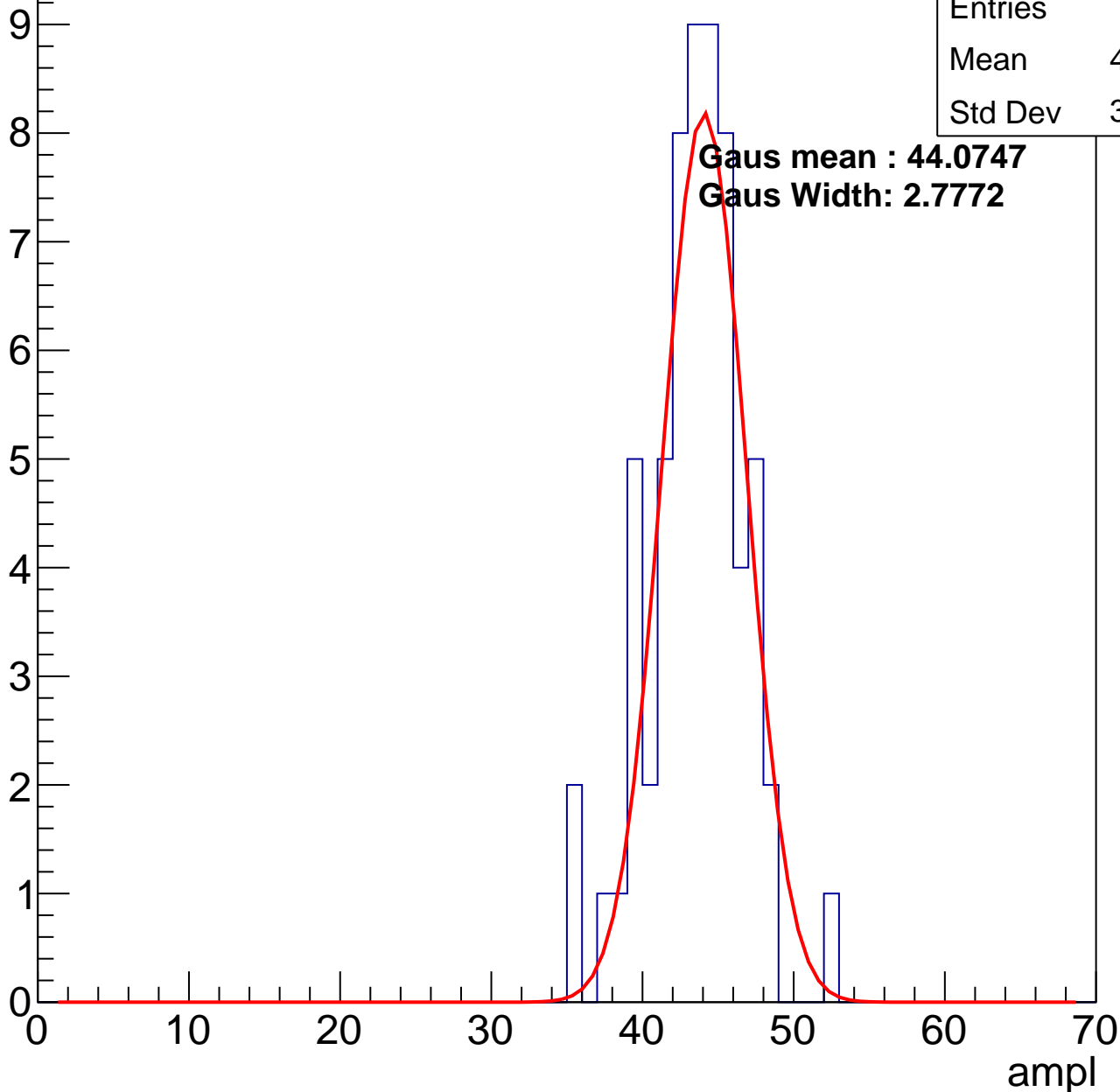
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	43.08
Std Dev	3.118

**Gaus mean : 44.0747**

**Gaus Width: 2.7772**

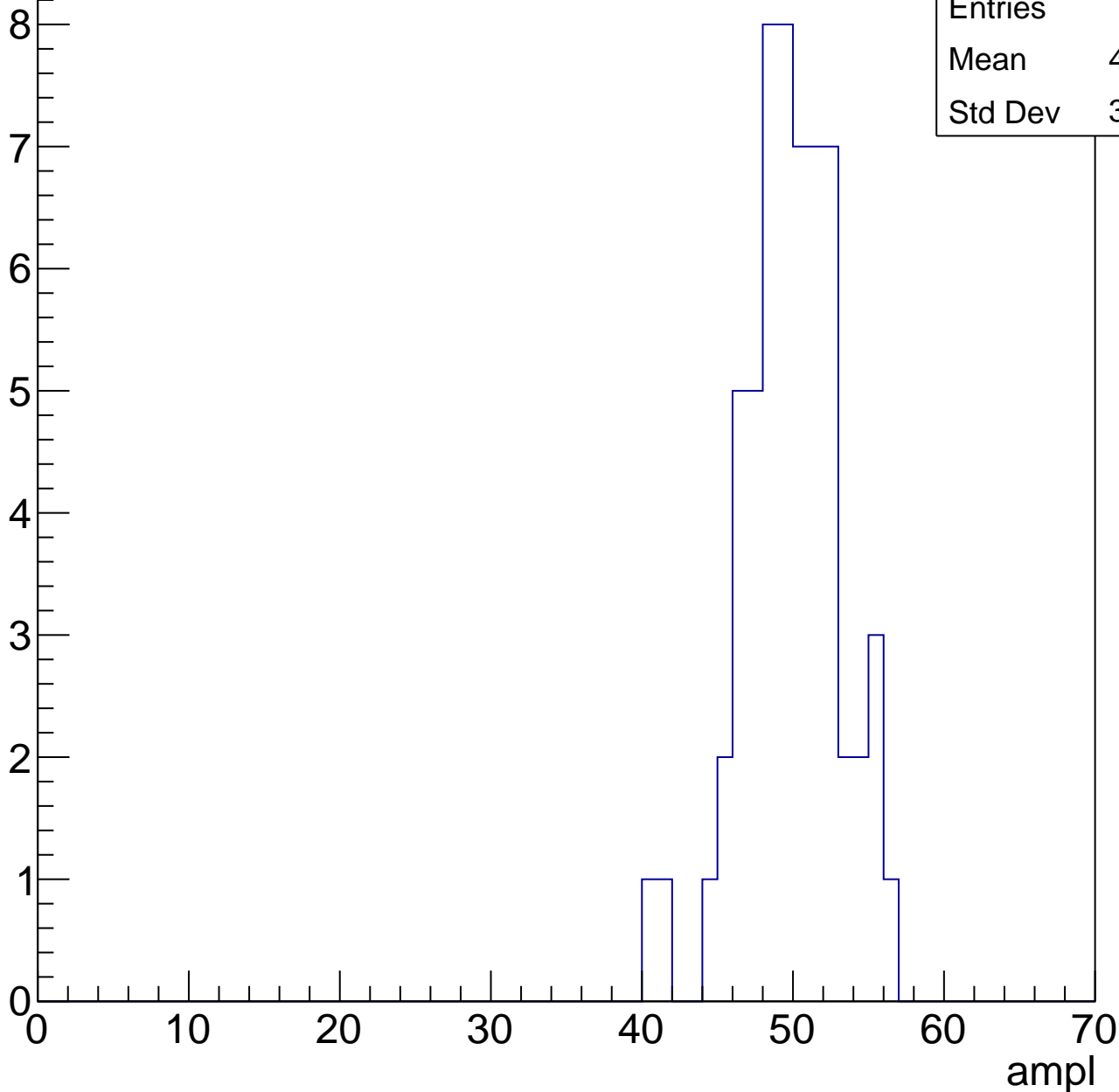


# B1L102S, U20-ch23, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	49.37
Std Dev	3.173

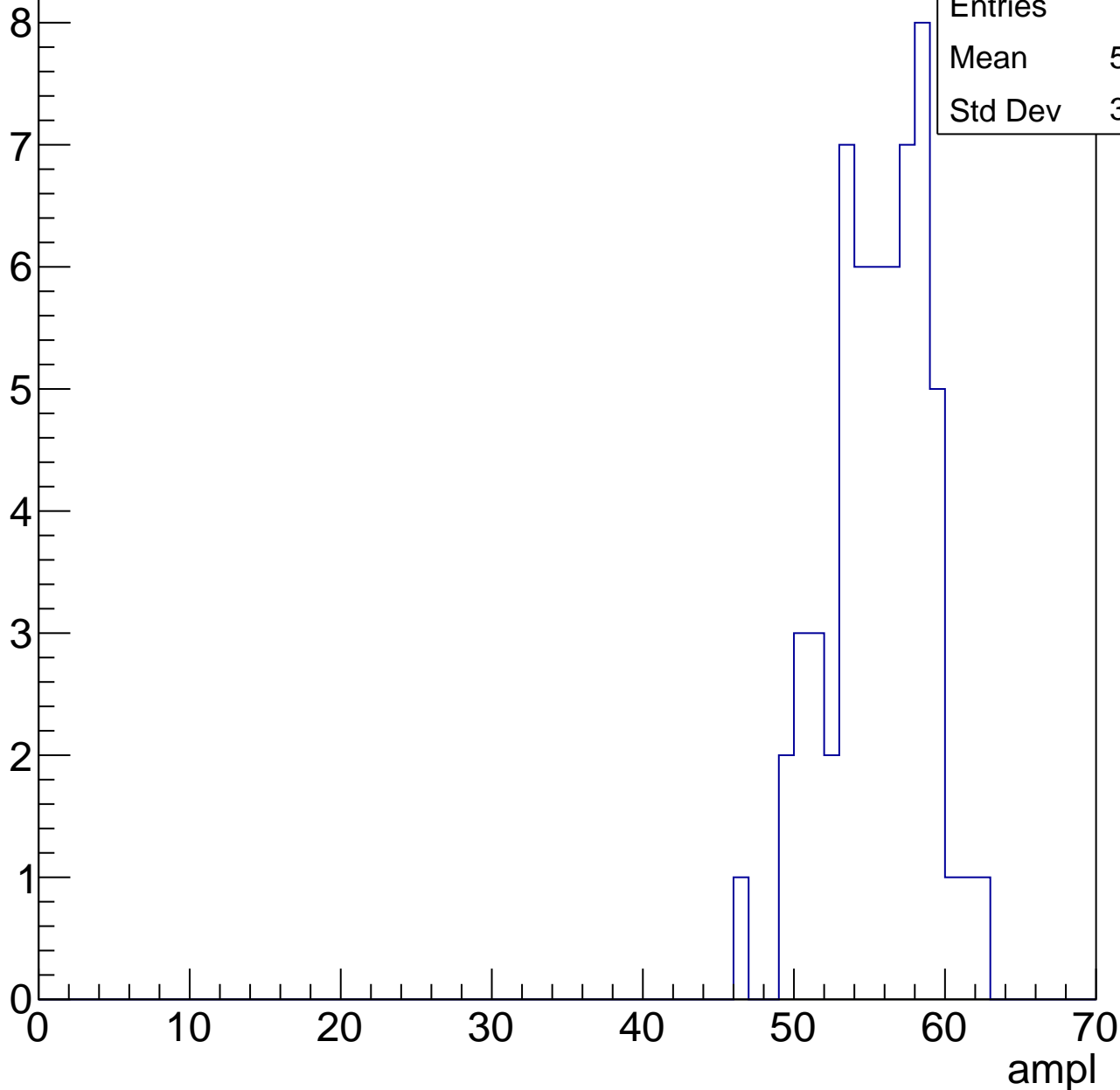


# B1L102S, U20-ch23, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

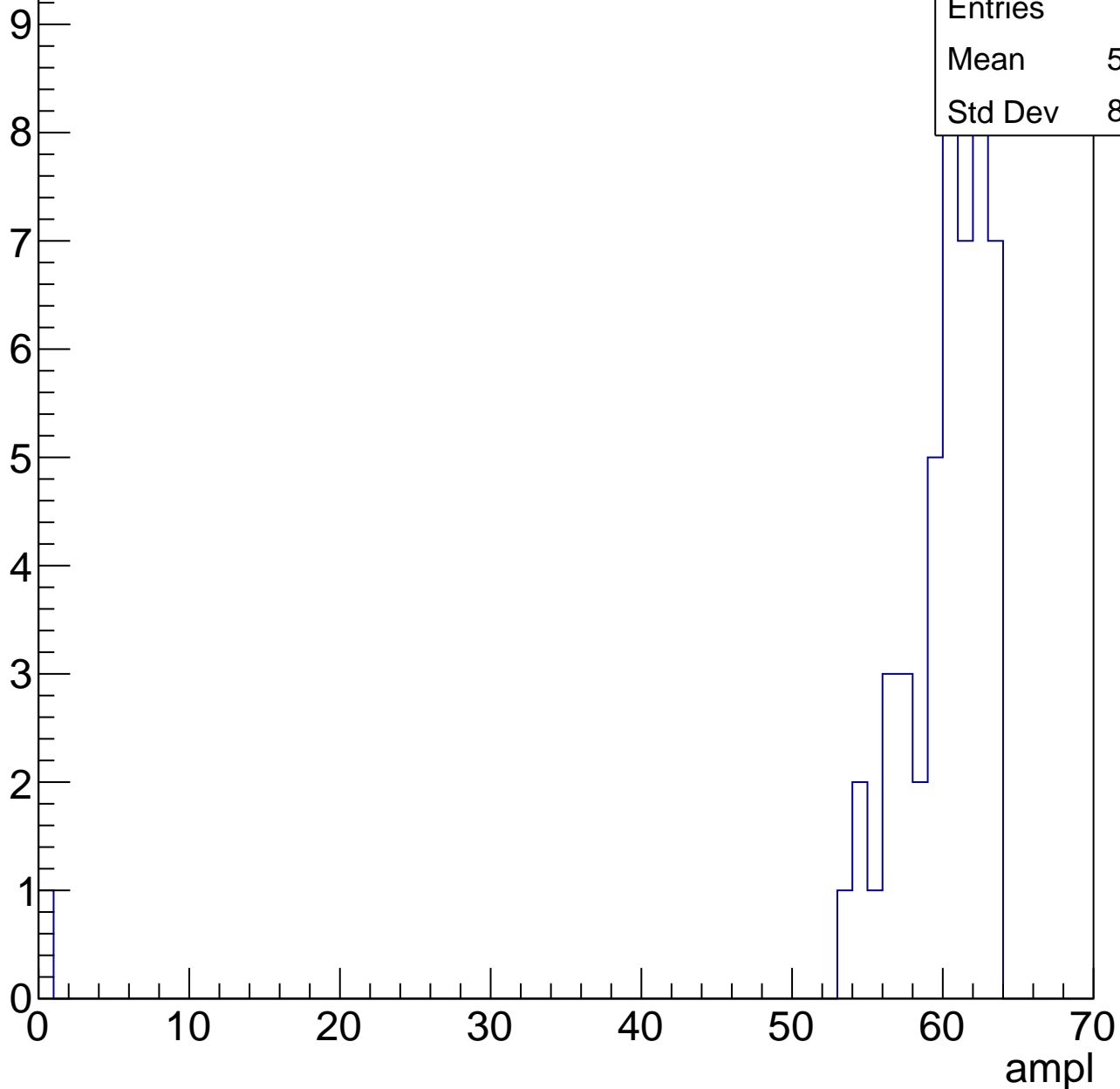
Entries	59
Mean	55.14
Std Dev	3.249



# B1L102S, U20-ch23, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch23, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U20-ch23, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch24, adc0

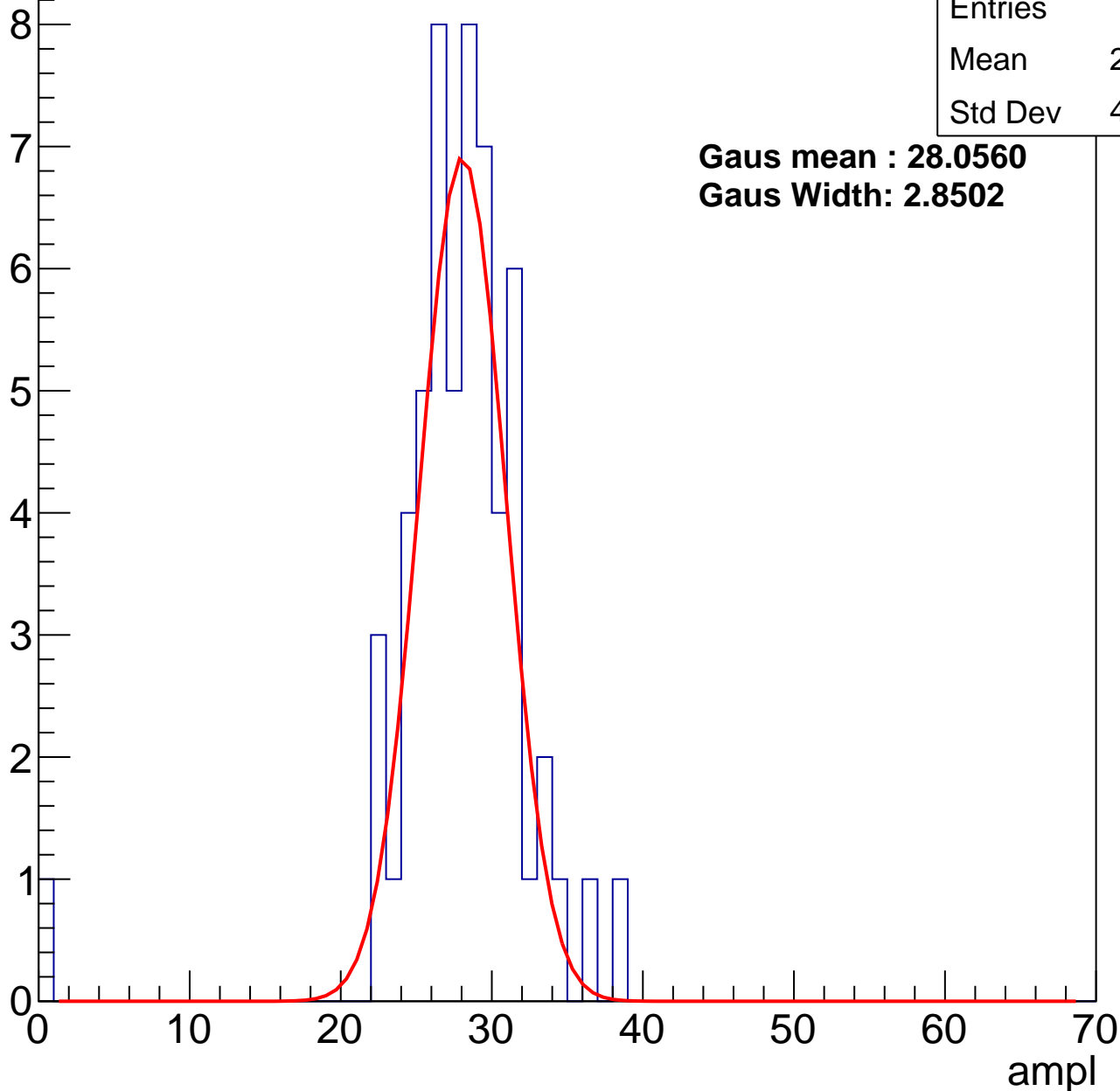
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	27.45
Std Dev	4.893

**Gaus mean : 28.0560**

**Gaus Width: 2.8502**



# B1L102S, U20-ch24, adc1

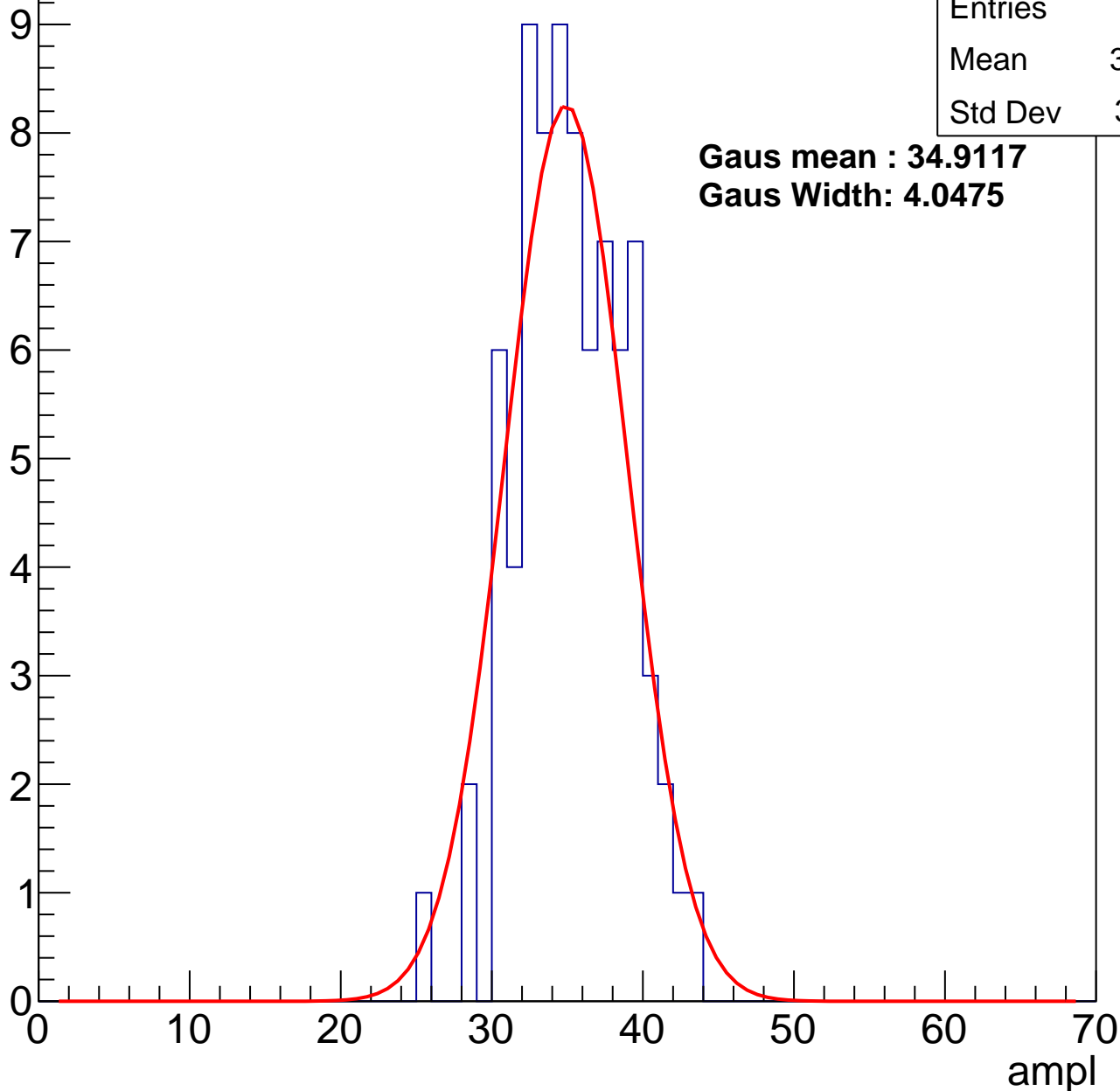
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	80
Mean	34.83
Std Dev	3.521

**Gaus mean : 34.9117**

**Gaus Width: 4.0475**



# B1L102S, U20-ch24, adc2

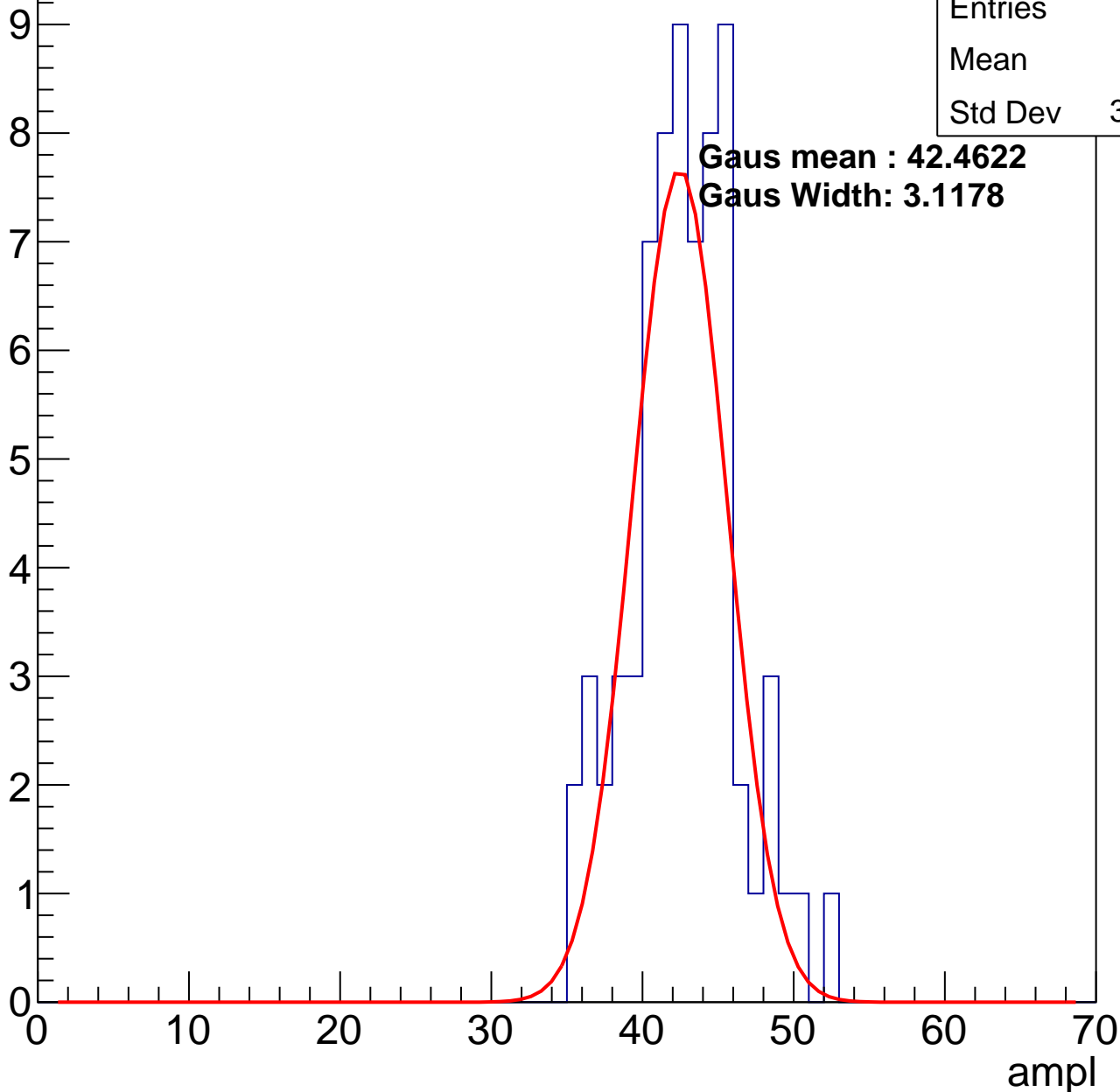
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	42.3
Std Dev	3.502

**Gaus mean : 42.4622**

**Gaus Width: 3.1178**

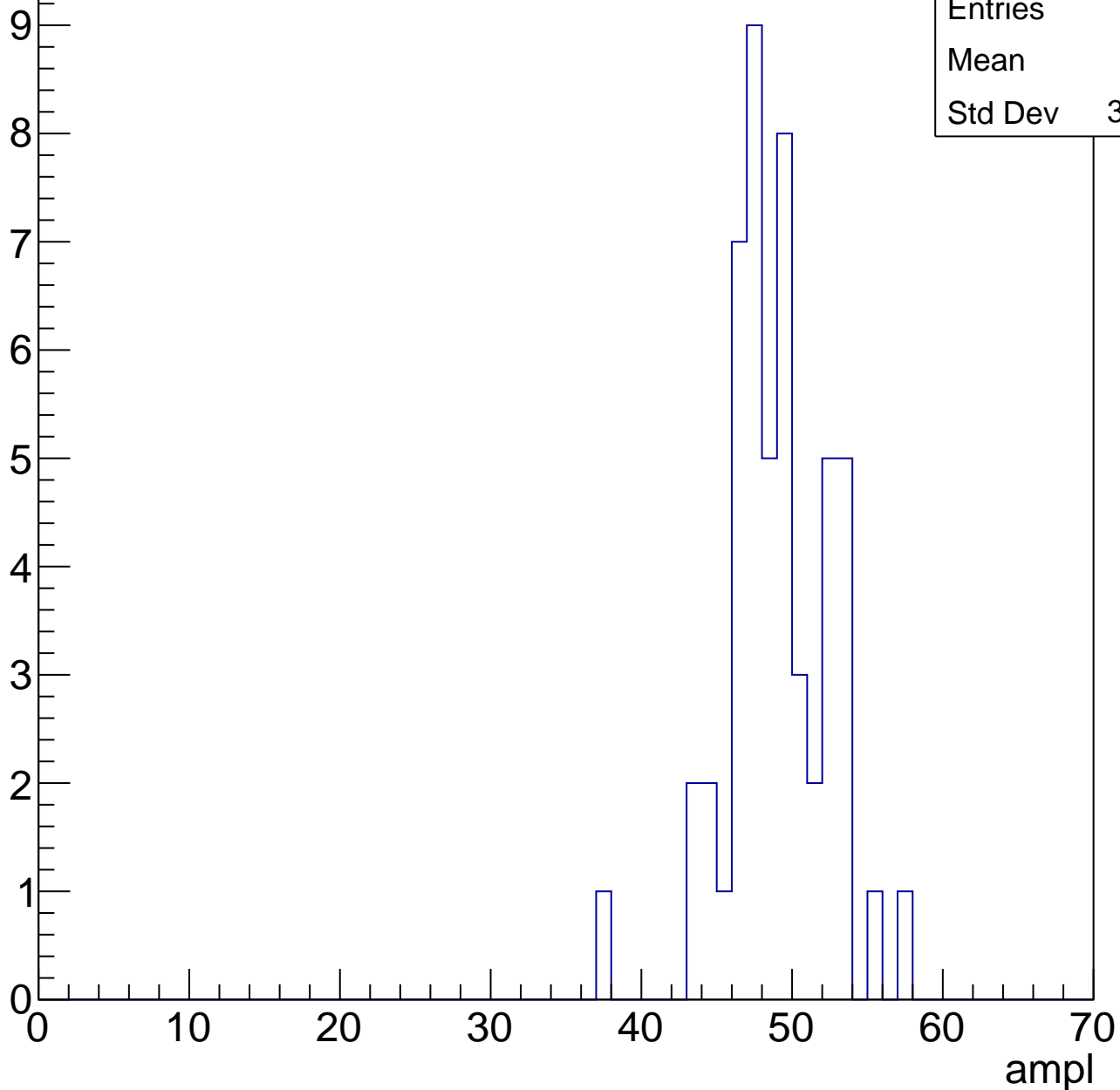


# B1L102S, U20-ch24, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	48.5
Std Dev	3.422

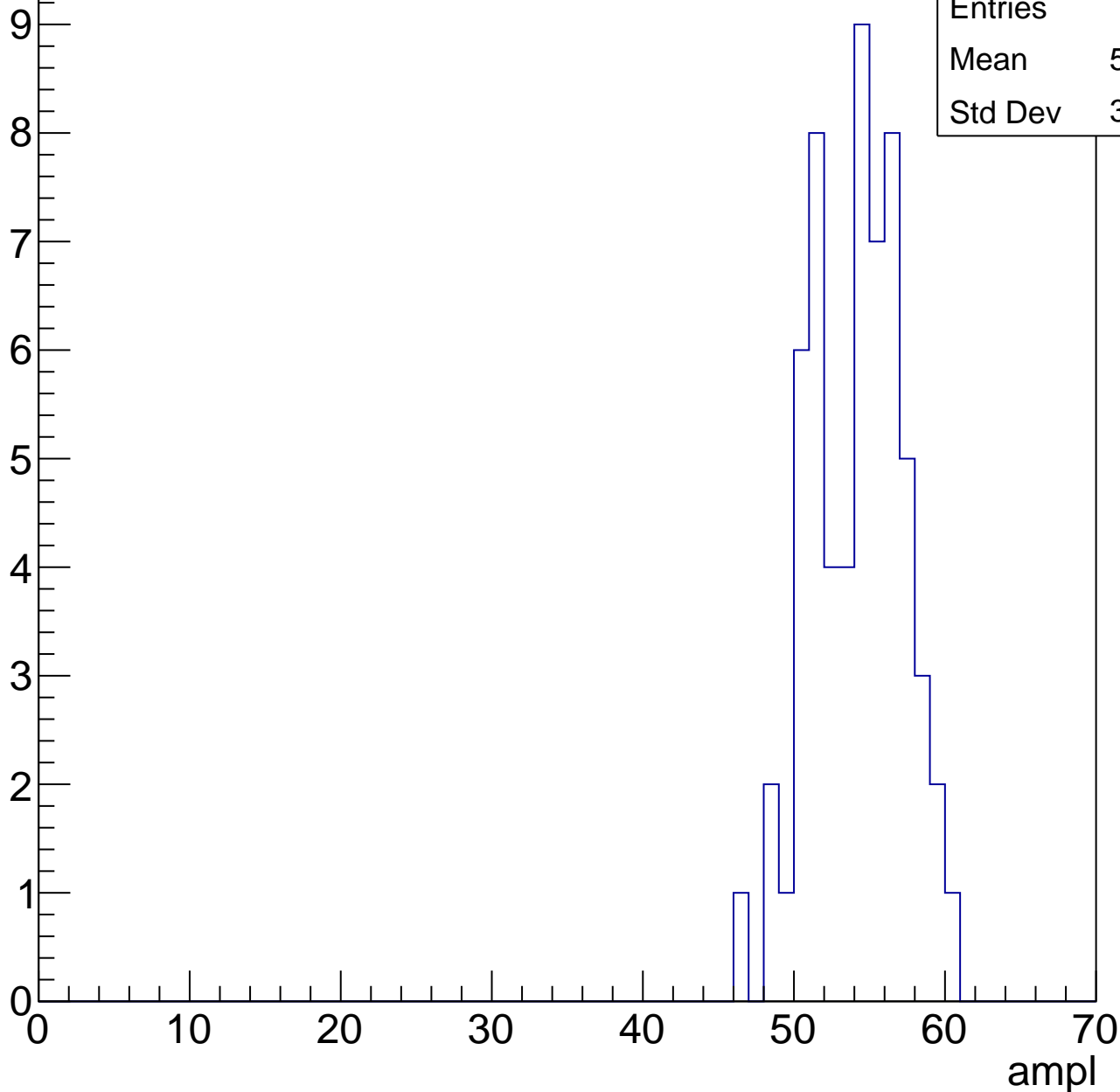


# B1L102S, U20-ch24, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	53.69
Std Dev	3.033



# B1L102S, U20-ch24, adc5

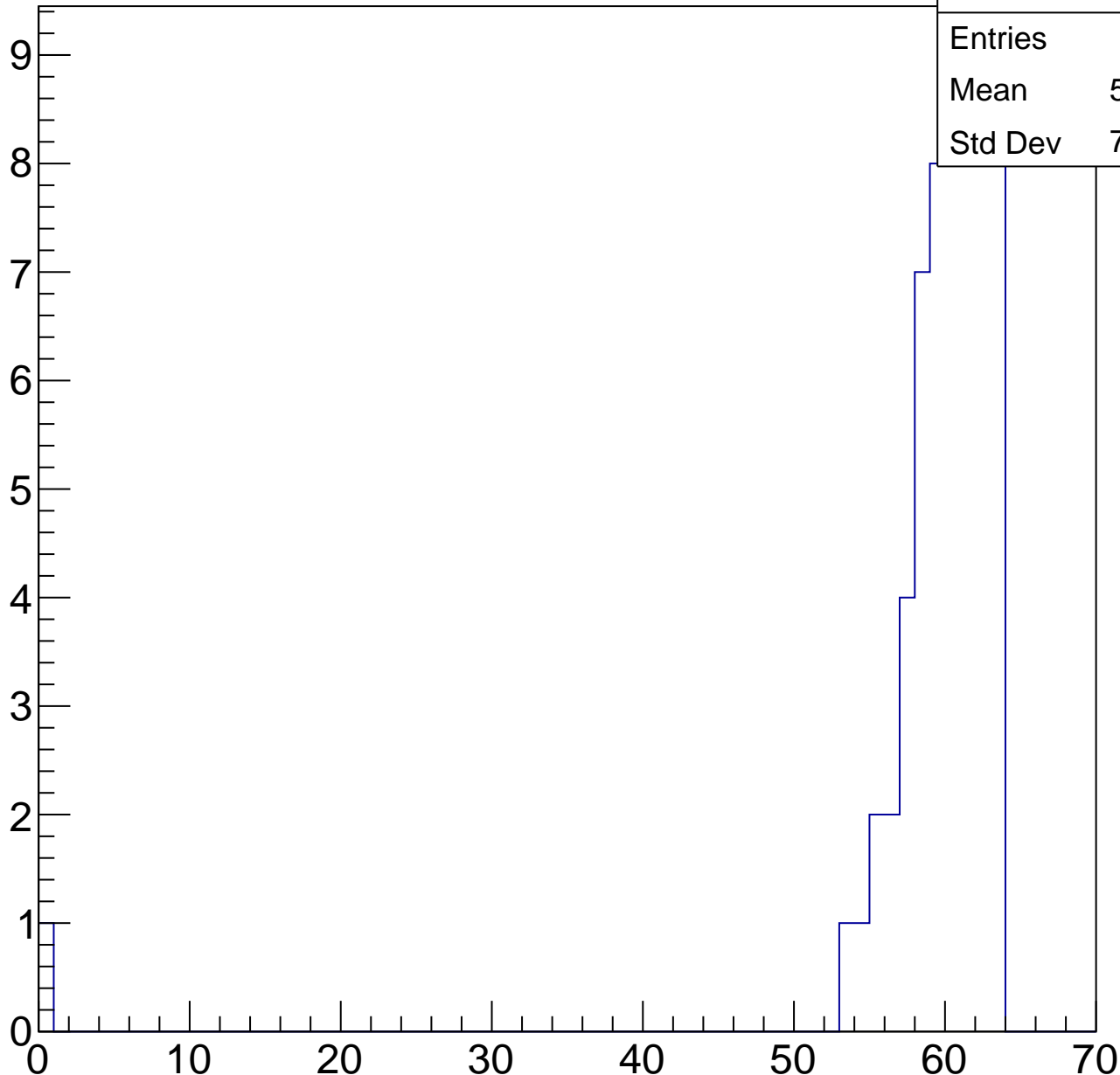
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	61
Mean	58.82
Std Dev	7.974

ampl



# B1L102S, U20-ch24, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U20-ch24, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U20-ch25, adc0

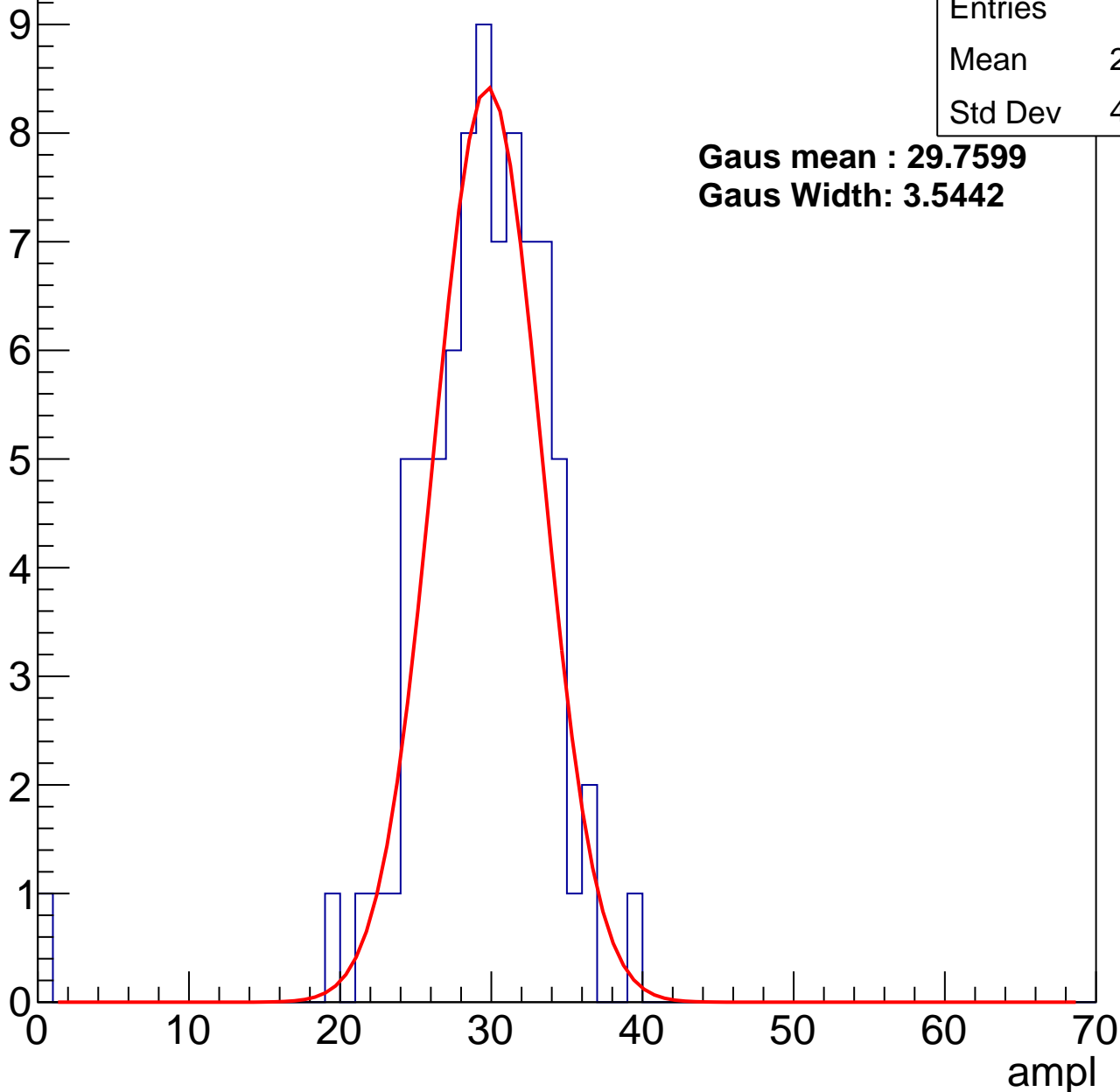
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	81
Mean	28.84
Std Dev	4.898

**Gaus mean : 29.7599**

**Gaus Width: 3.5442**



# B1L102S, U20-ch25, adc1

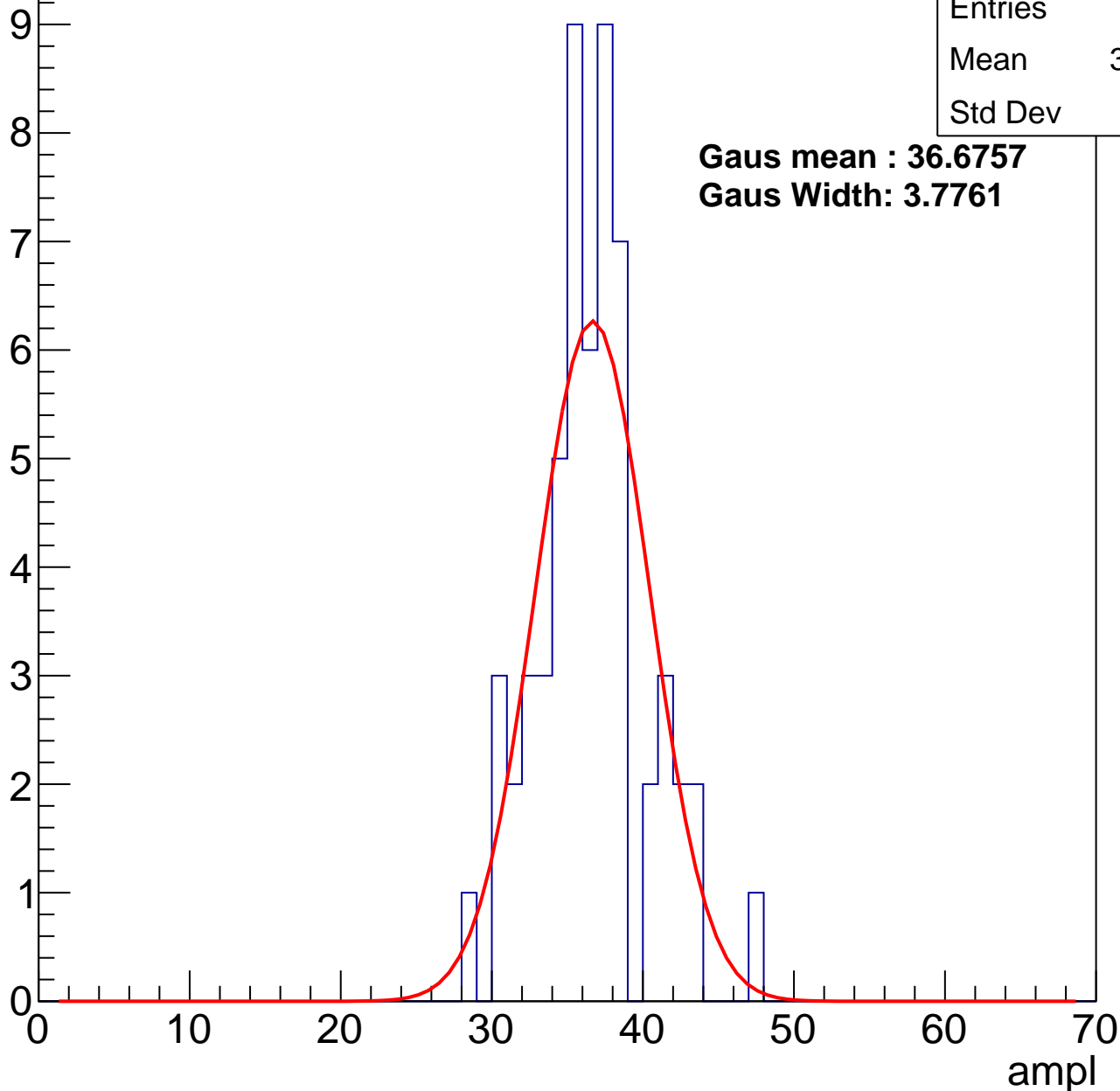
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	36.12
Std Dev	3.62

**Gaus mean : 36.6757**

**Gaus Width: 3.7761**



# B1L102S, U20-ch25, adc2

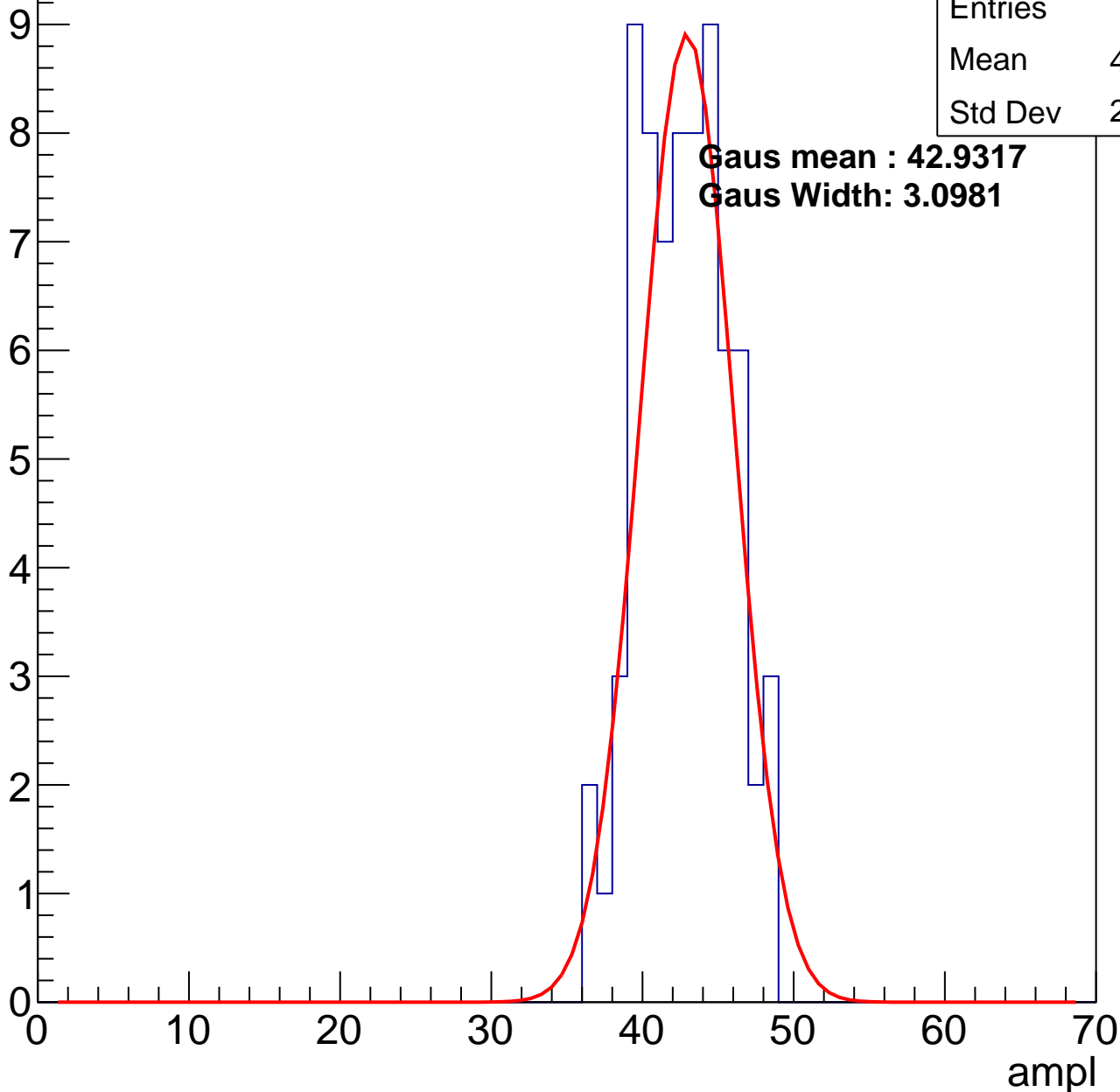
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	42.24
Std Dev	2.918

**Gaus mean : 42.9317**

**Gaus Width: 3.0981**

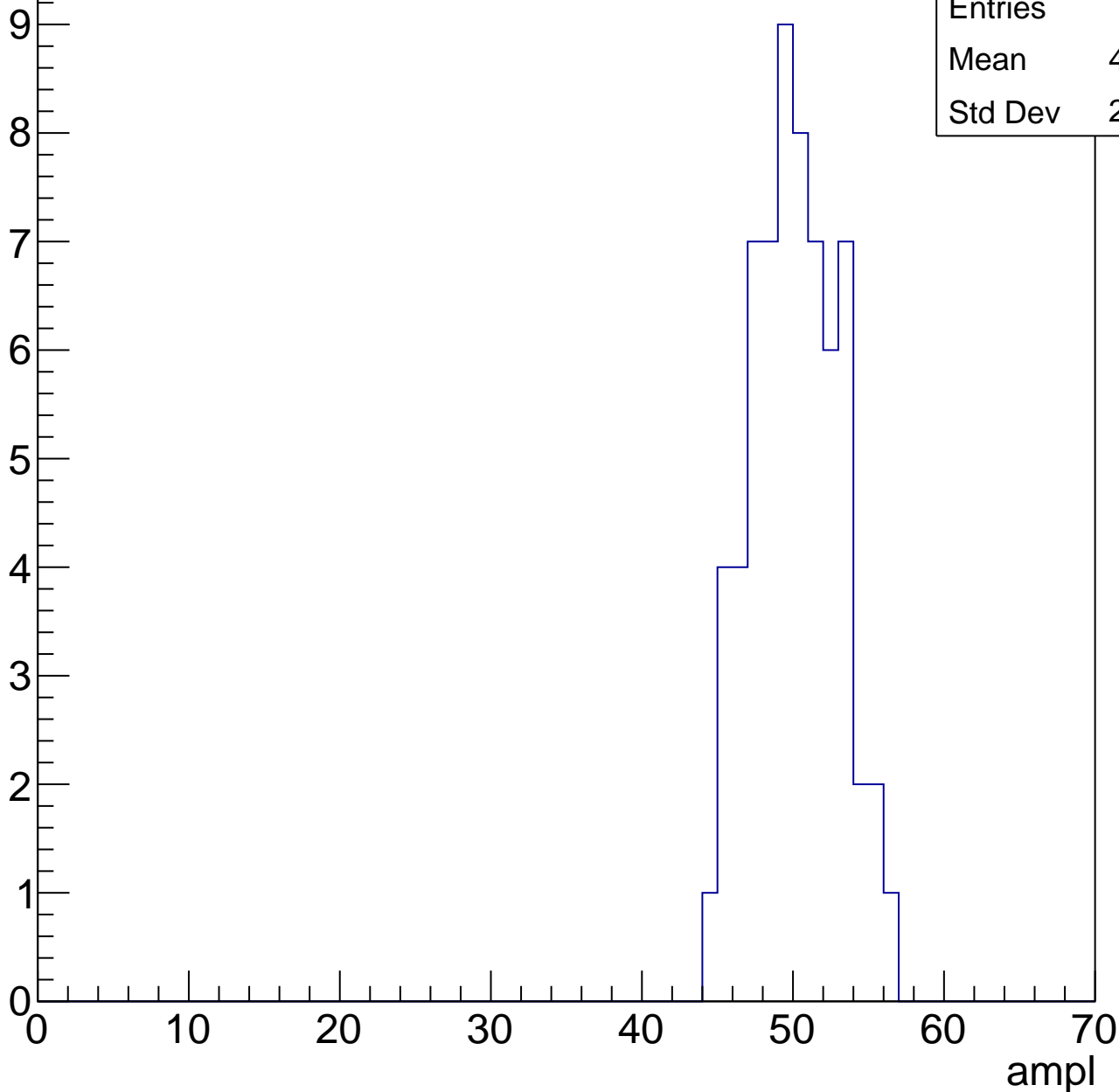


# B1L102S, U20-ch25, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	49.66
Std Dev	2.786

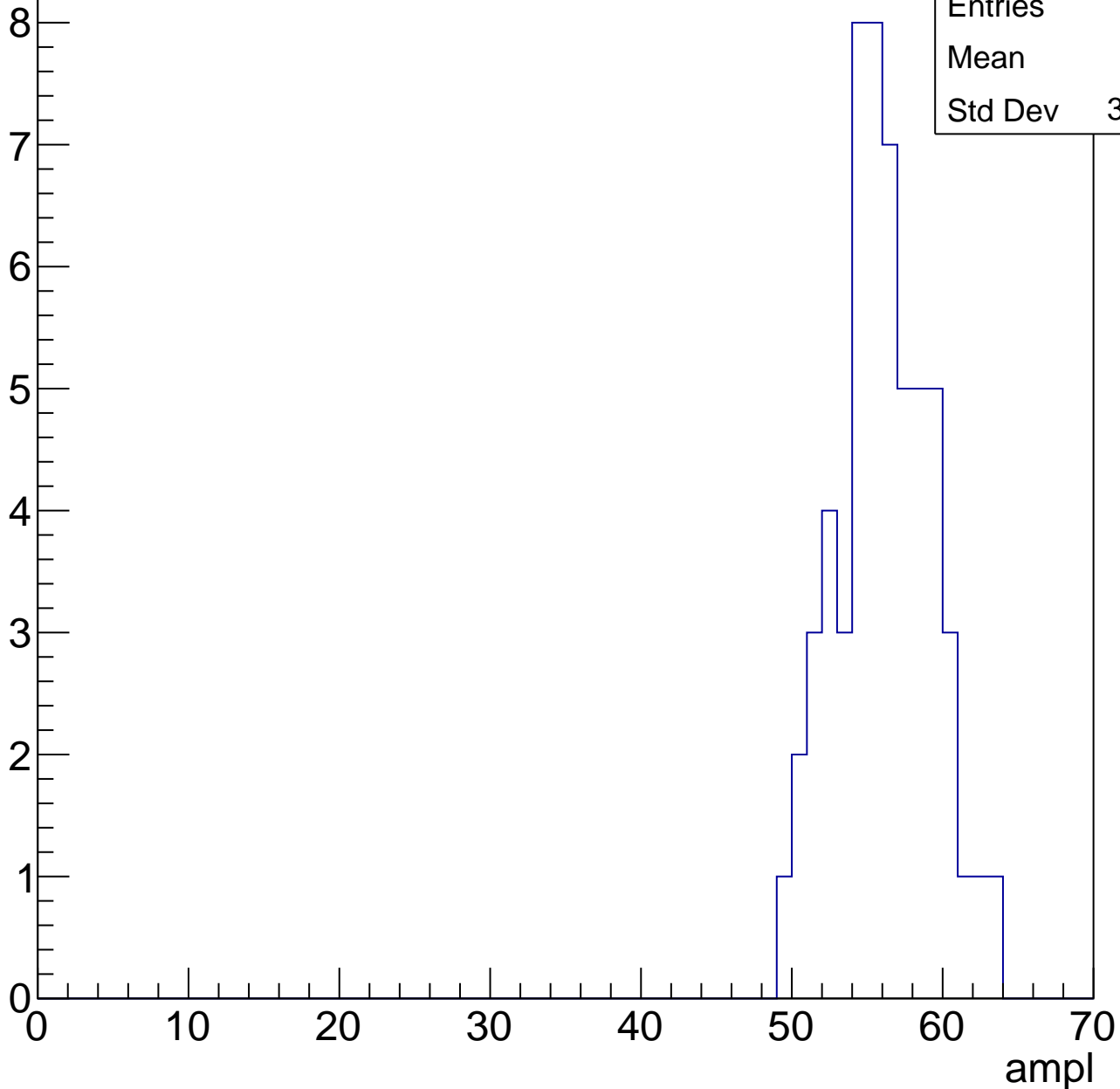


# B1L102S, U20-ch25, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	55.6
Std Dev	3.094

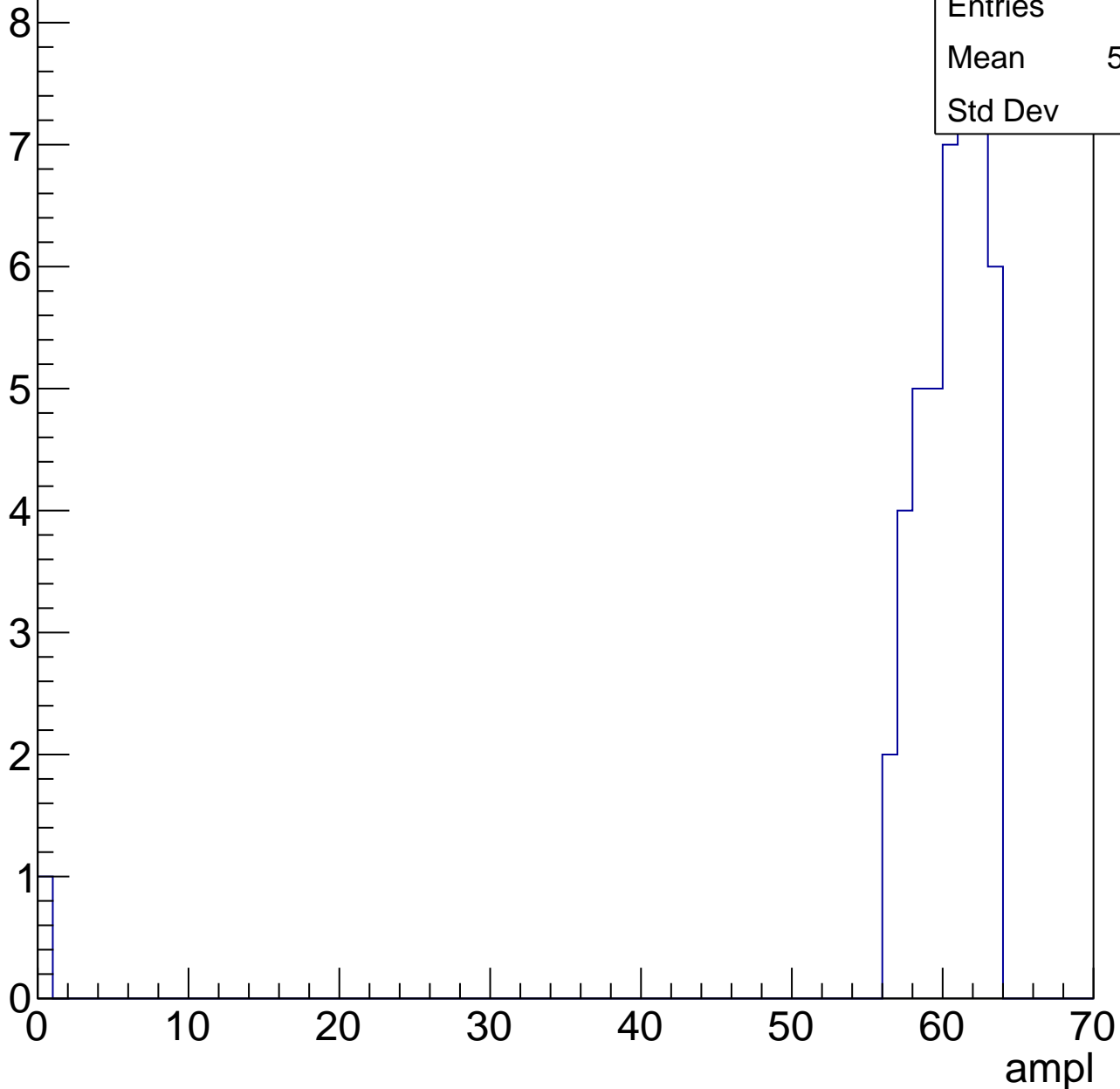


# B1L102S, U20-ch25, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

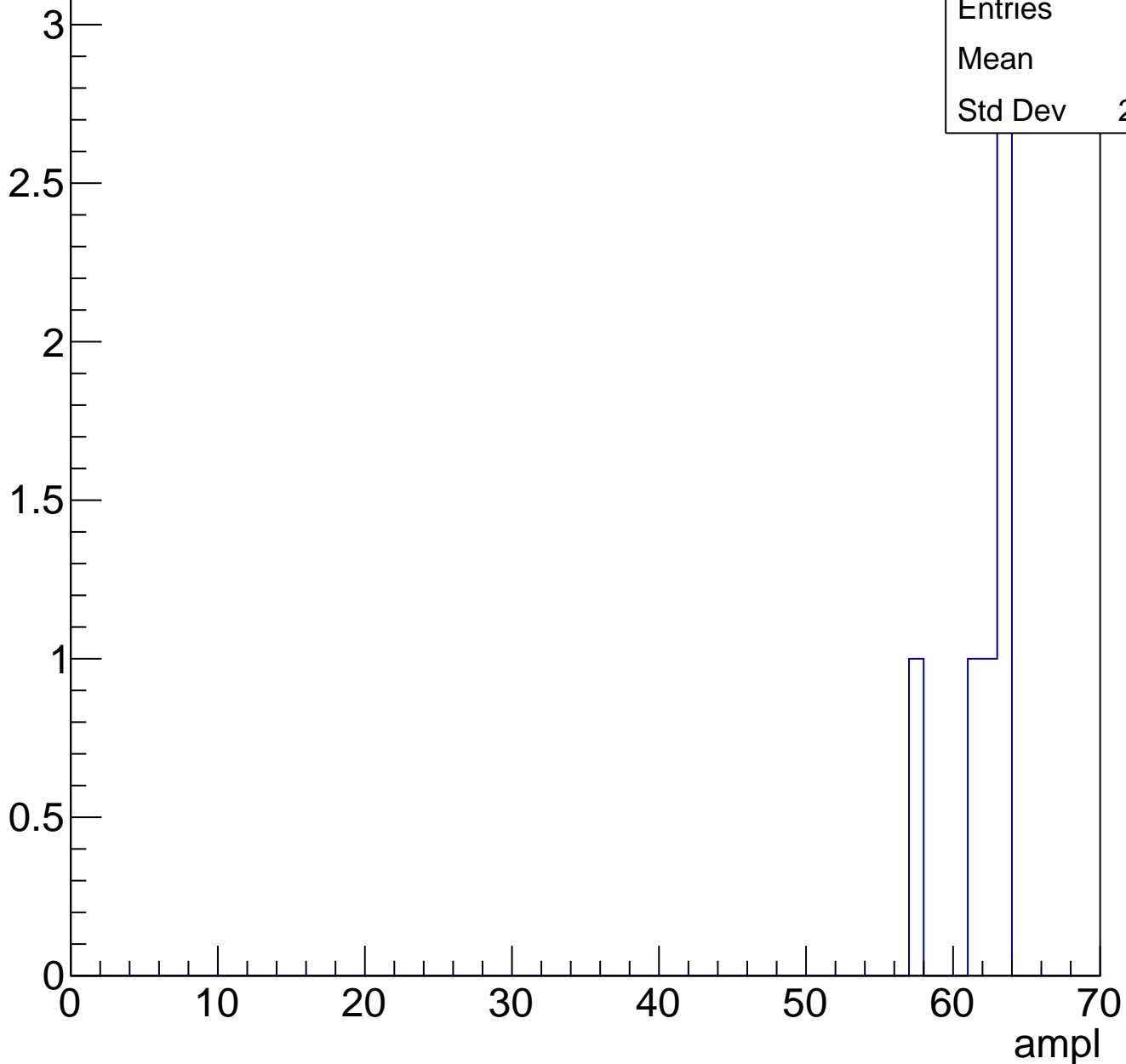
Entries	46
Mean	58.85
Std Dev	9



# B1L102S, U20-ch25, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U20-ch25, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L102S, U20-ch26, adc0

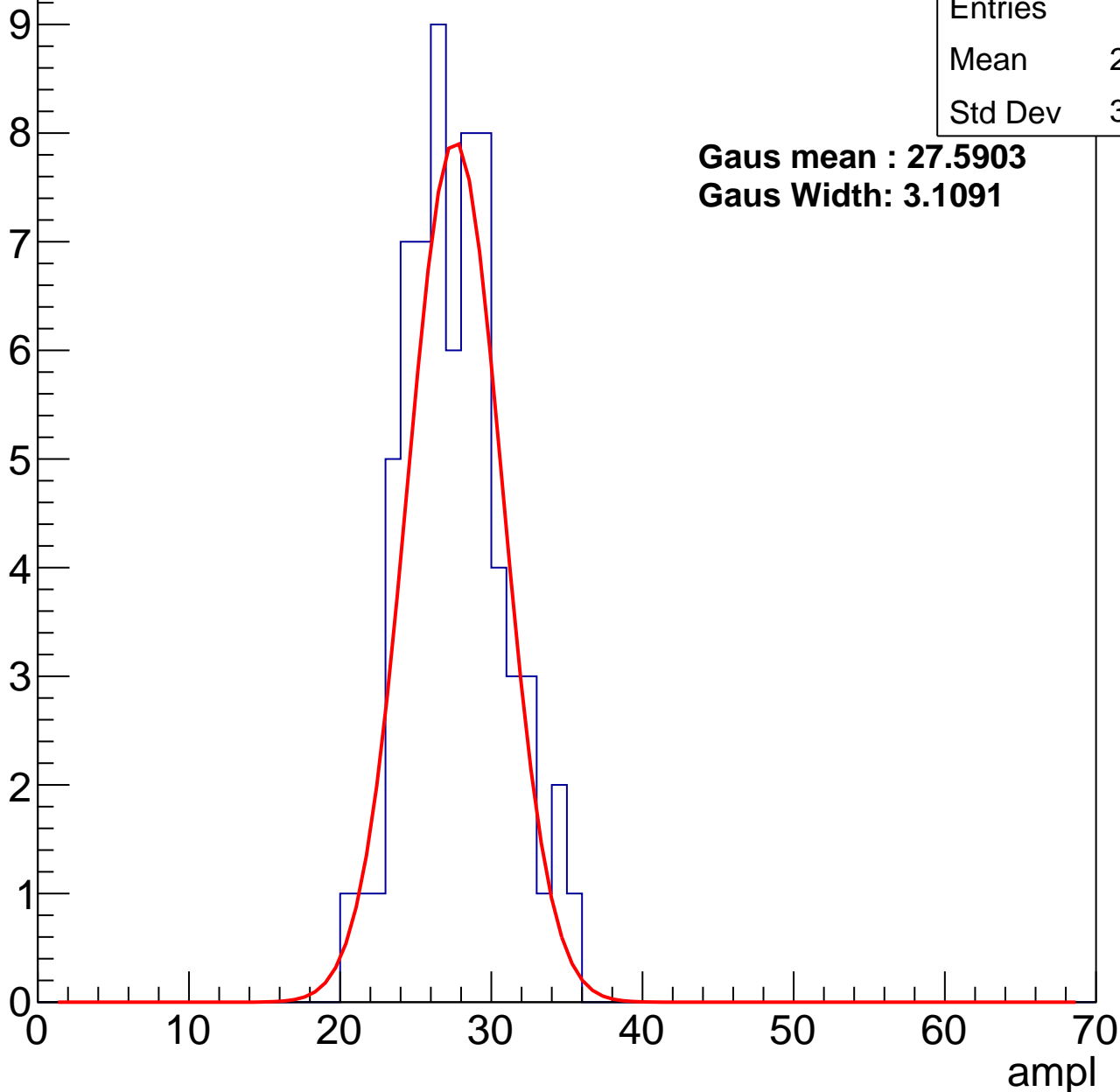
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	27.13
Std Dev	3.199

**Gaus mean : 27.5903**

**Gaus Width: 3.1091**



# B1L102S, U20-ch26, adc1

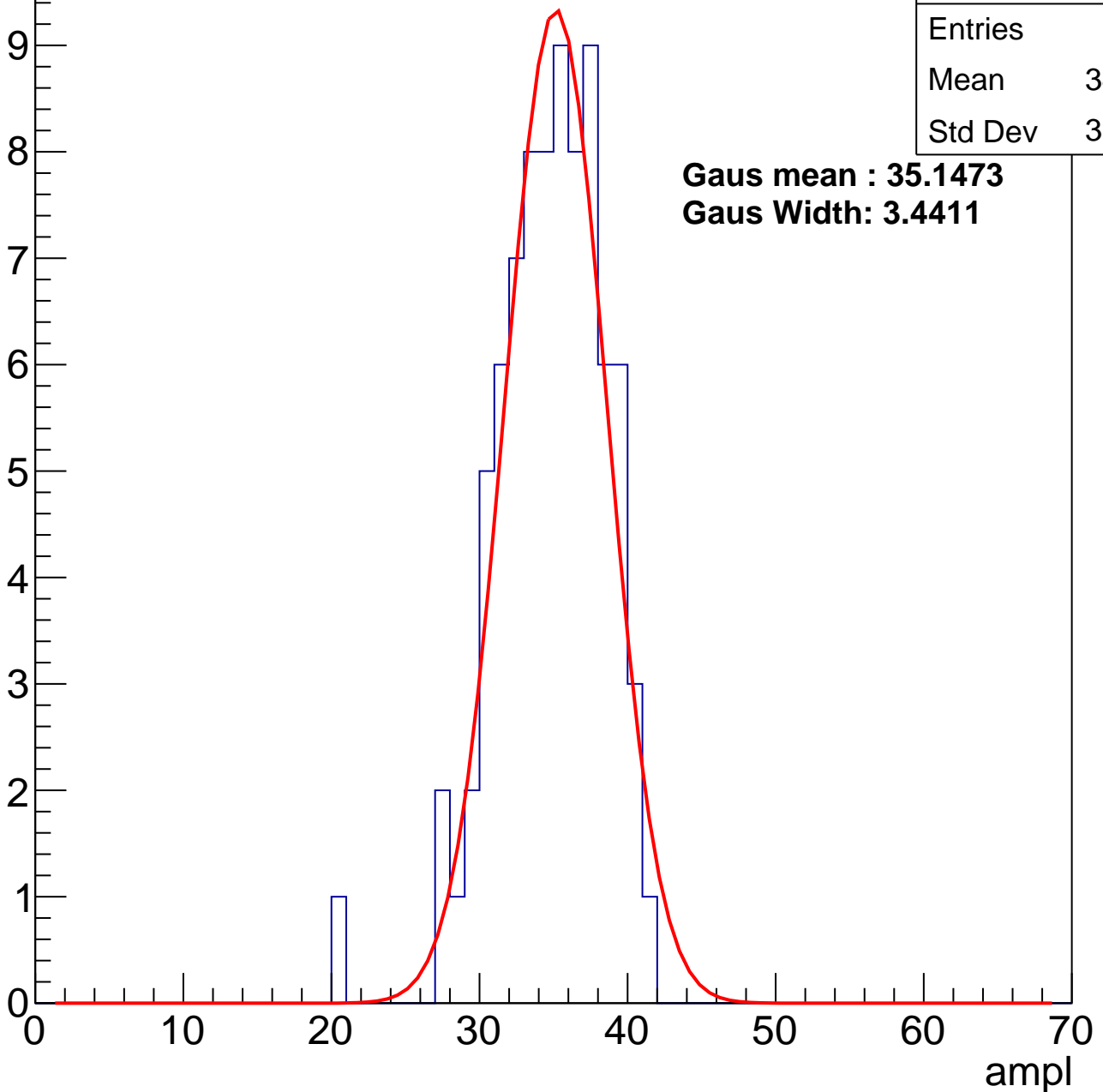
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	82
Mean	34.33
Std Dev	3.606

**Gaus mean : 35.1473**

**Gaus Width: 3.4411**



# B1L102S, U20-ch26, adc2

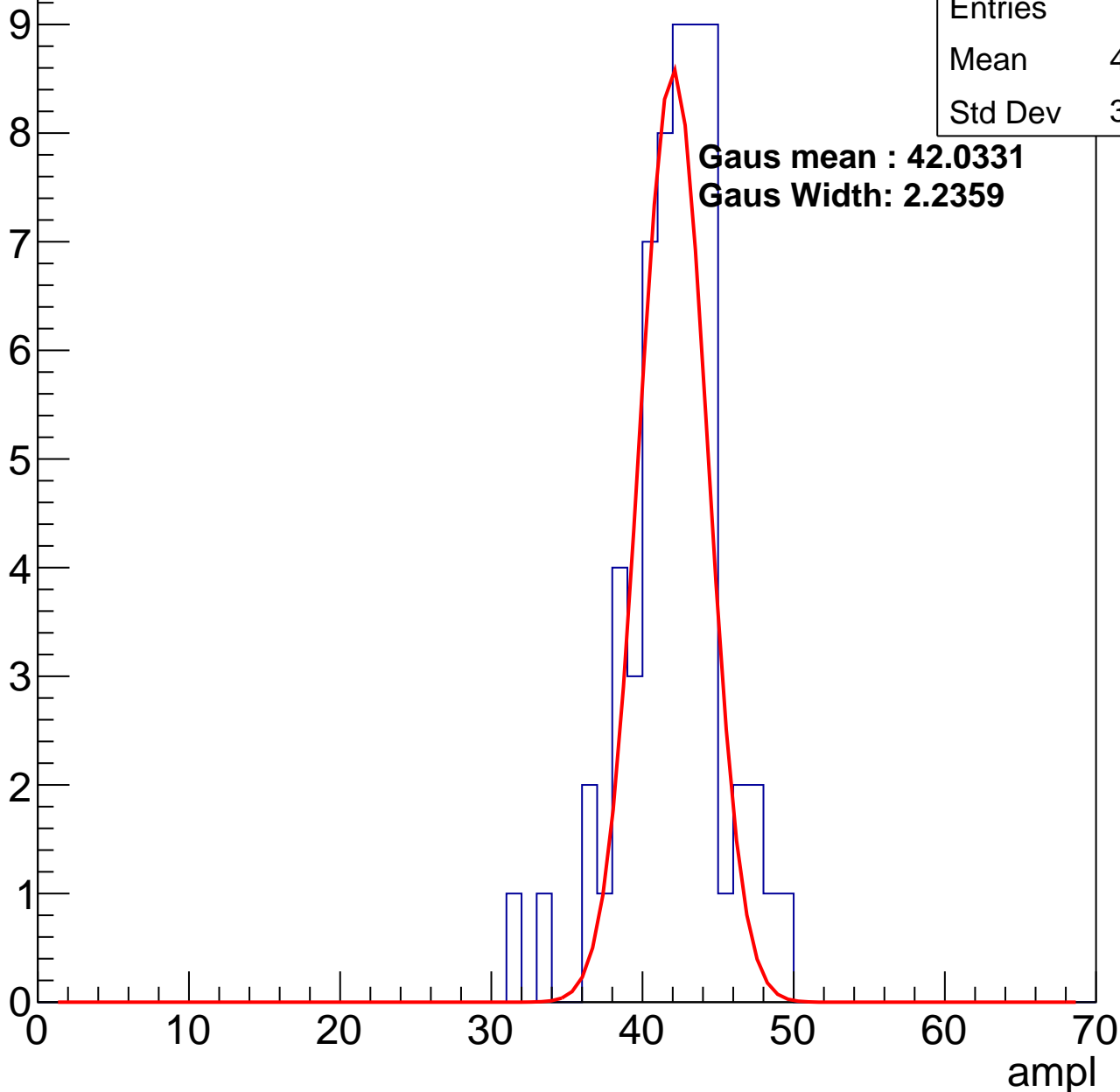
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	41.62
Std Dev	3.235

**Gaus mean : 42.0331**

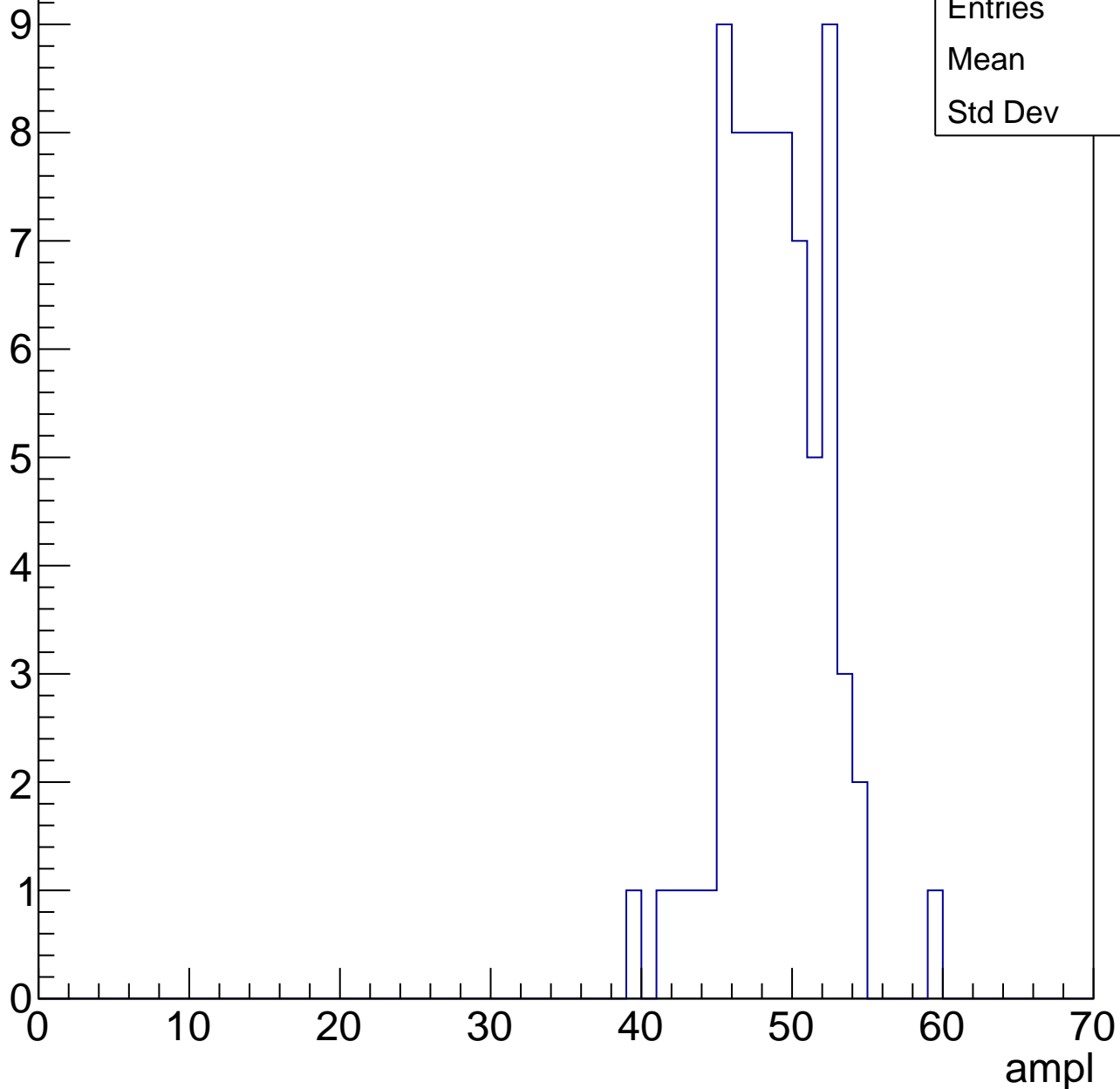
**Gaus Width: 2.2359**



# B1L102S, U20-ch26, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

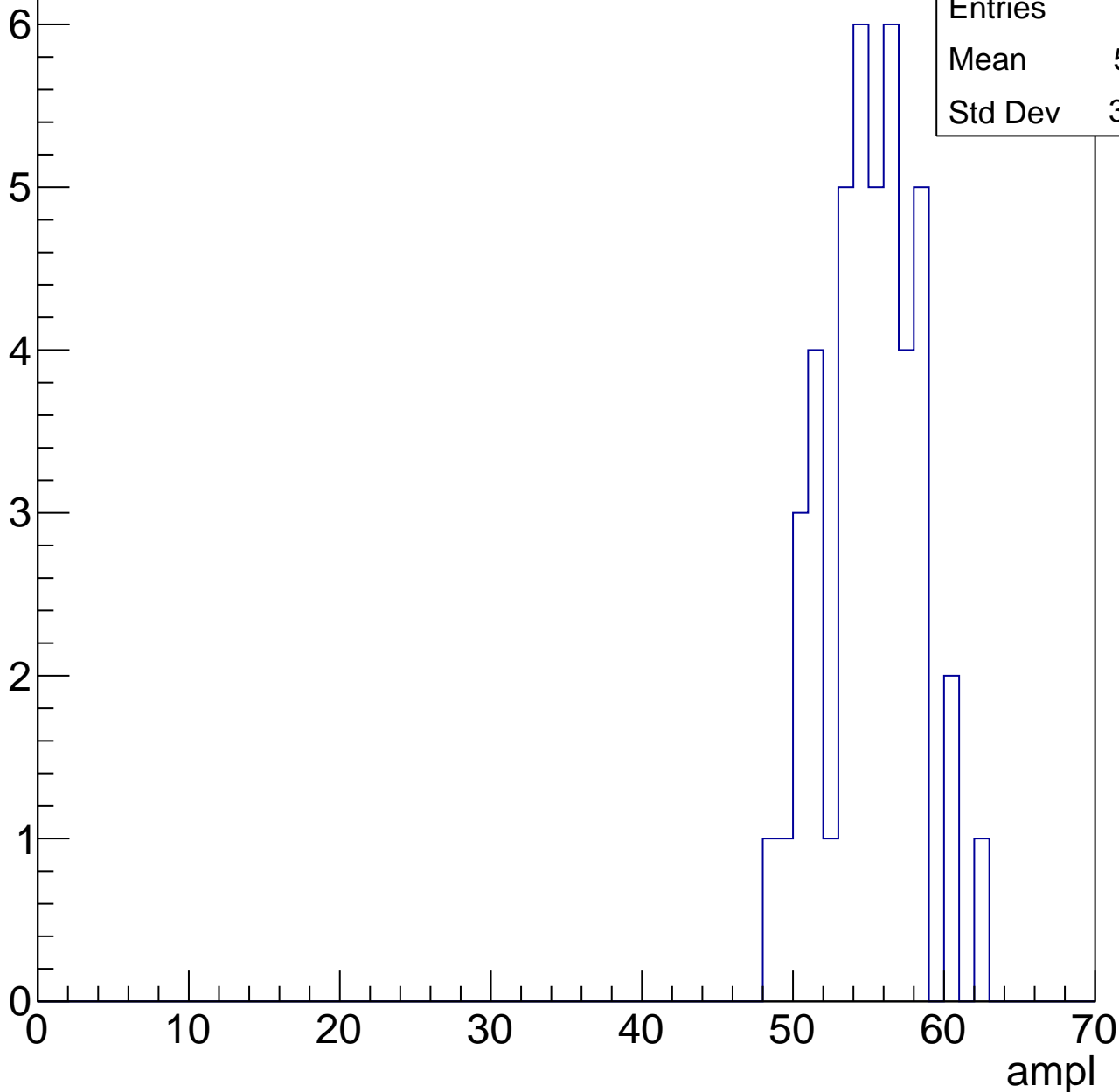


# B1L102S, U20-ch26, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	44
Mean	54.61
Std Dev	3.084



# B1L102S, U20-ch26, adc5

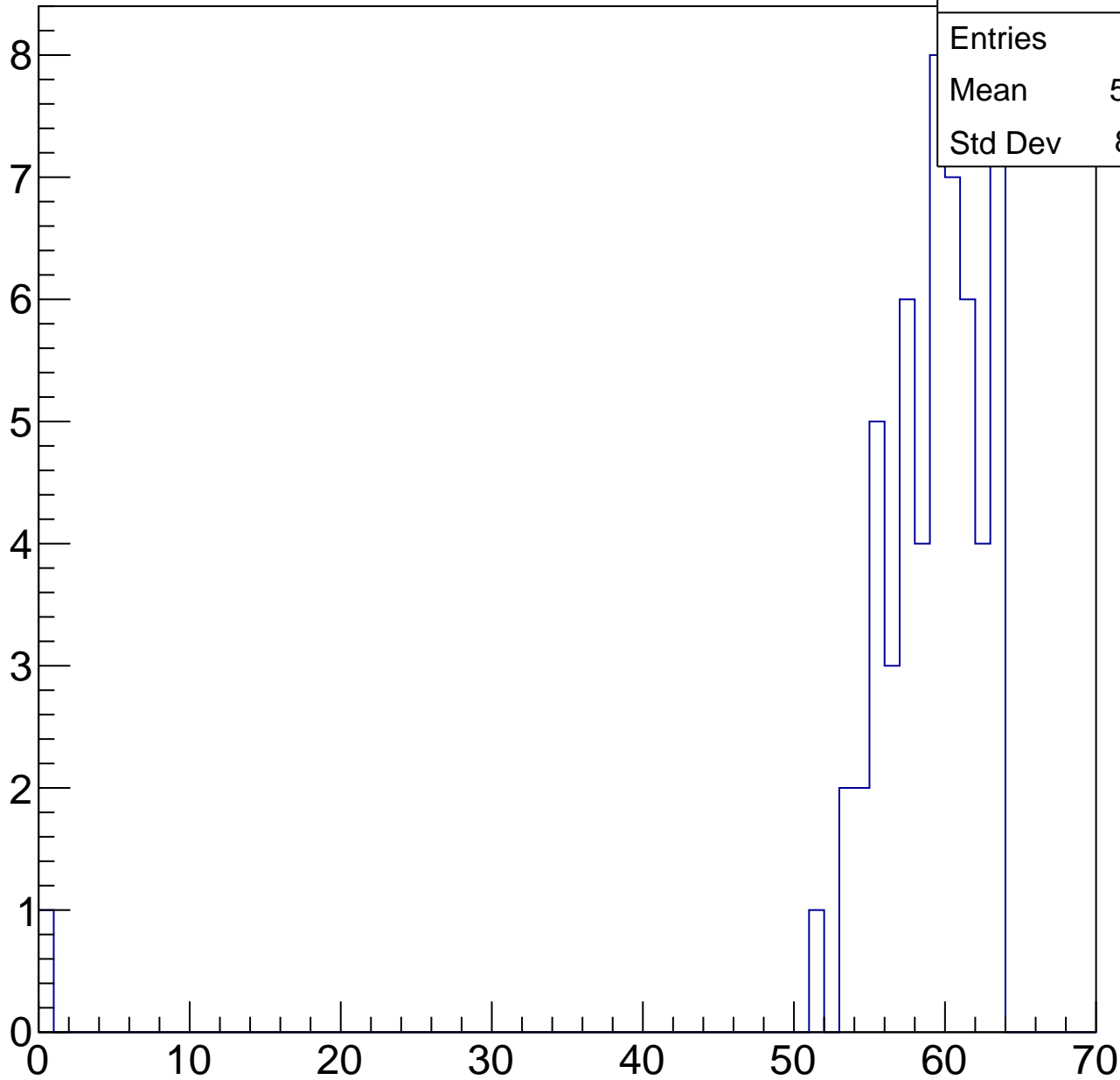
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	57
Mean	57.75
Std Dev	8.281

ampl

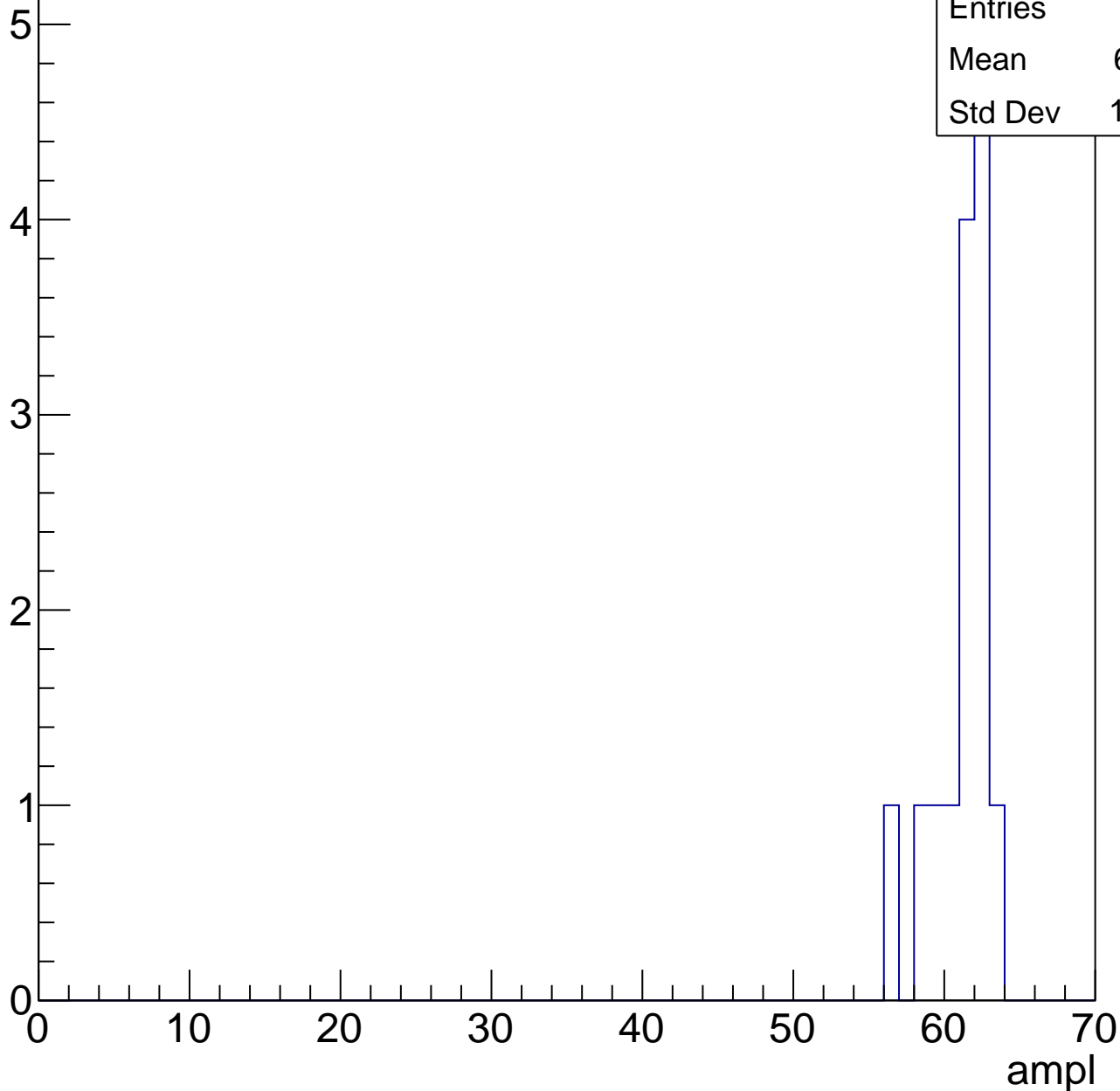


# B1L102S, U20-ch26, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	14
Mean	60.71
Std Dev	1.829





# B1L102S, U20-ch26, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch27, adc0

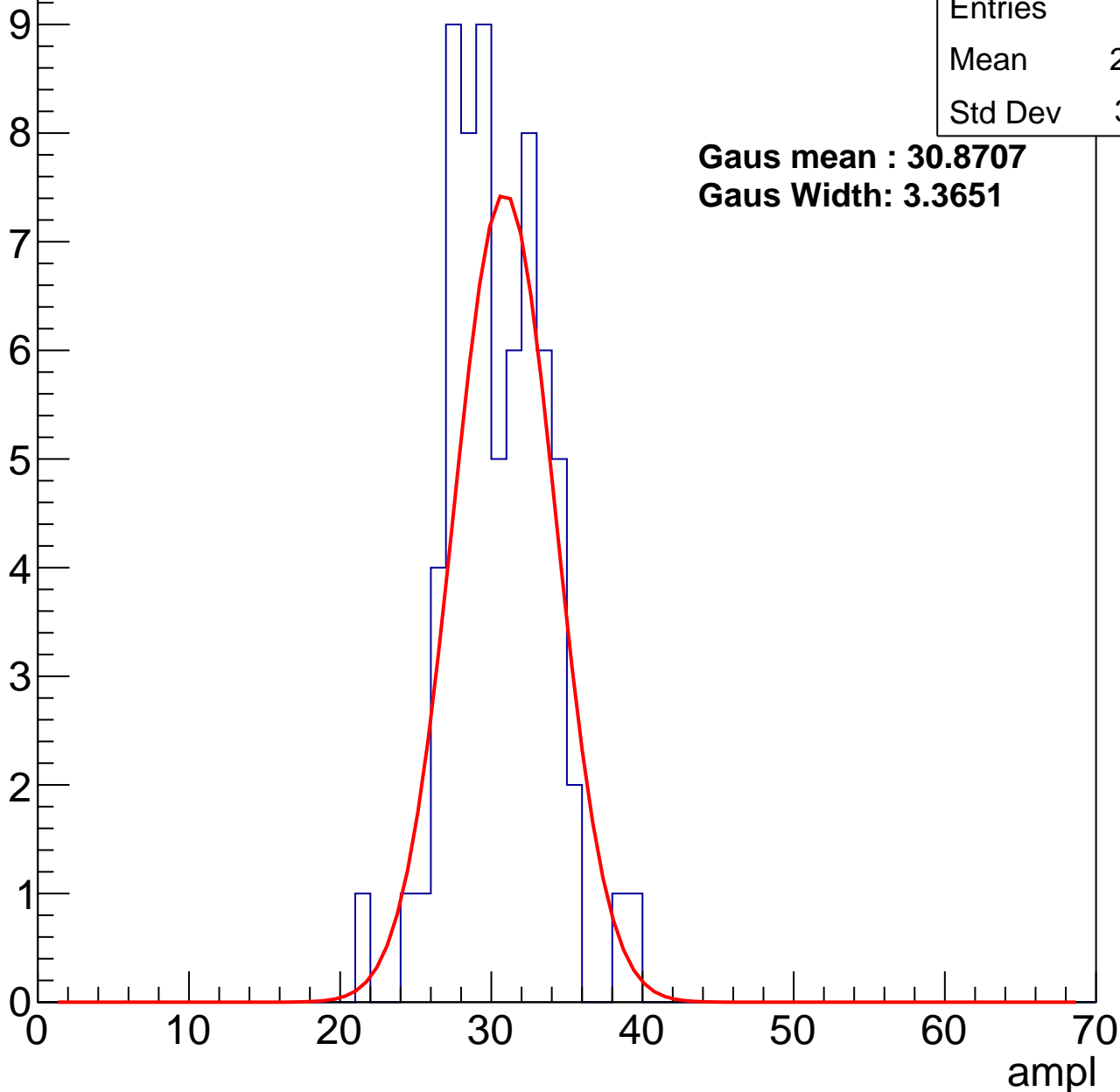
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	29.99
Std Dev	3.221

**Gaus mean : 30.8707**

**Gaus Width: 3.3651**



# B1L102S, U20-ch27, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	79
Mean	37.13
Std Dev	3.664

**Gaus mean : 37.6606**

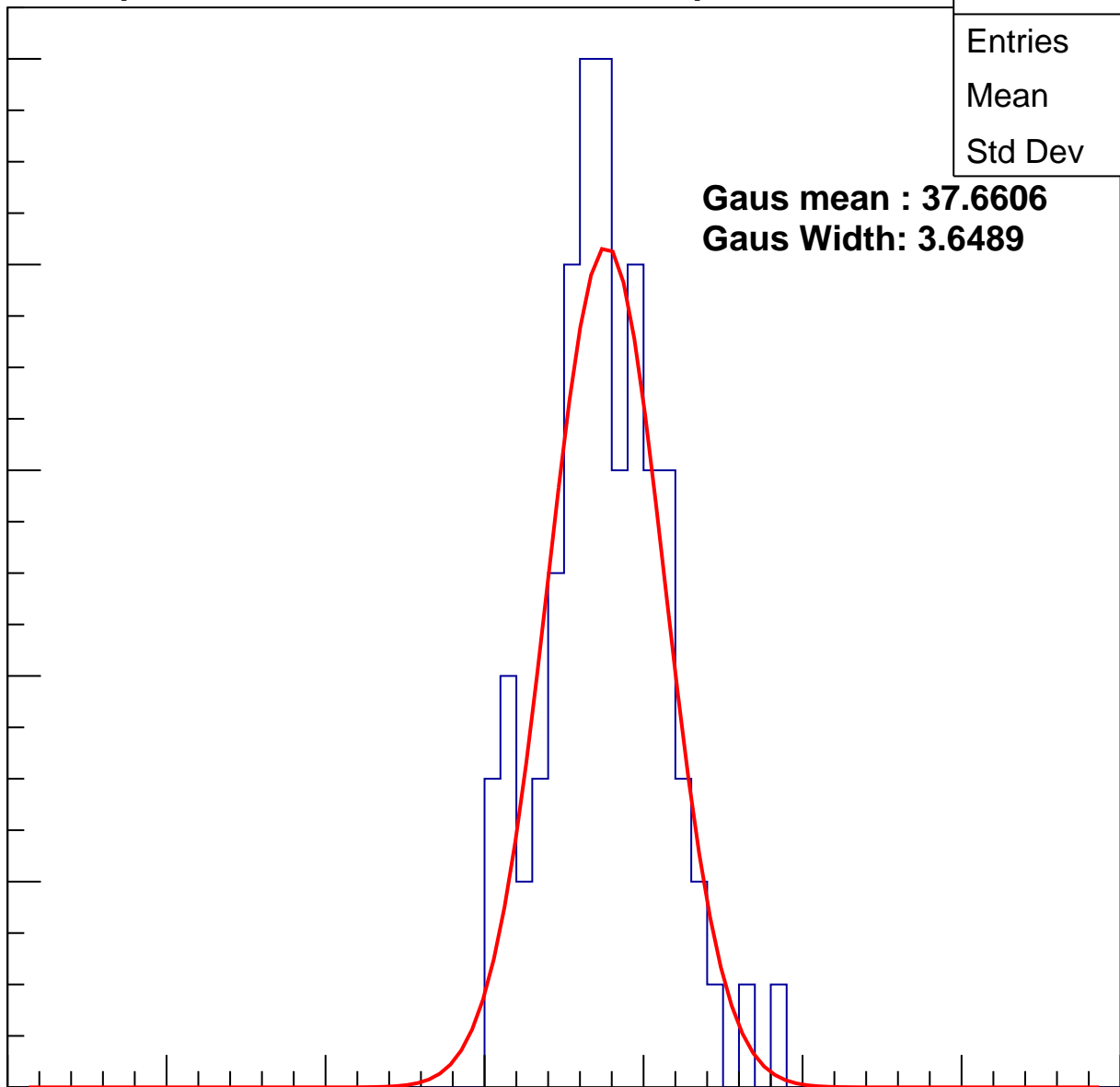
**Gaus Width: 3.6489**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U20-ch27, adc2

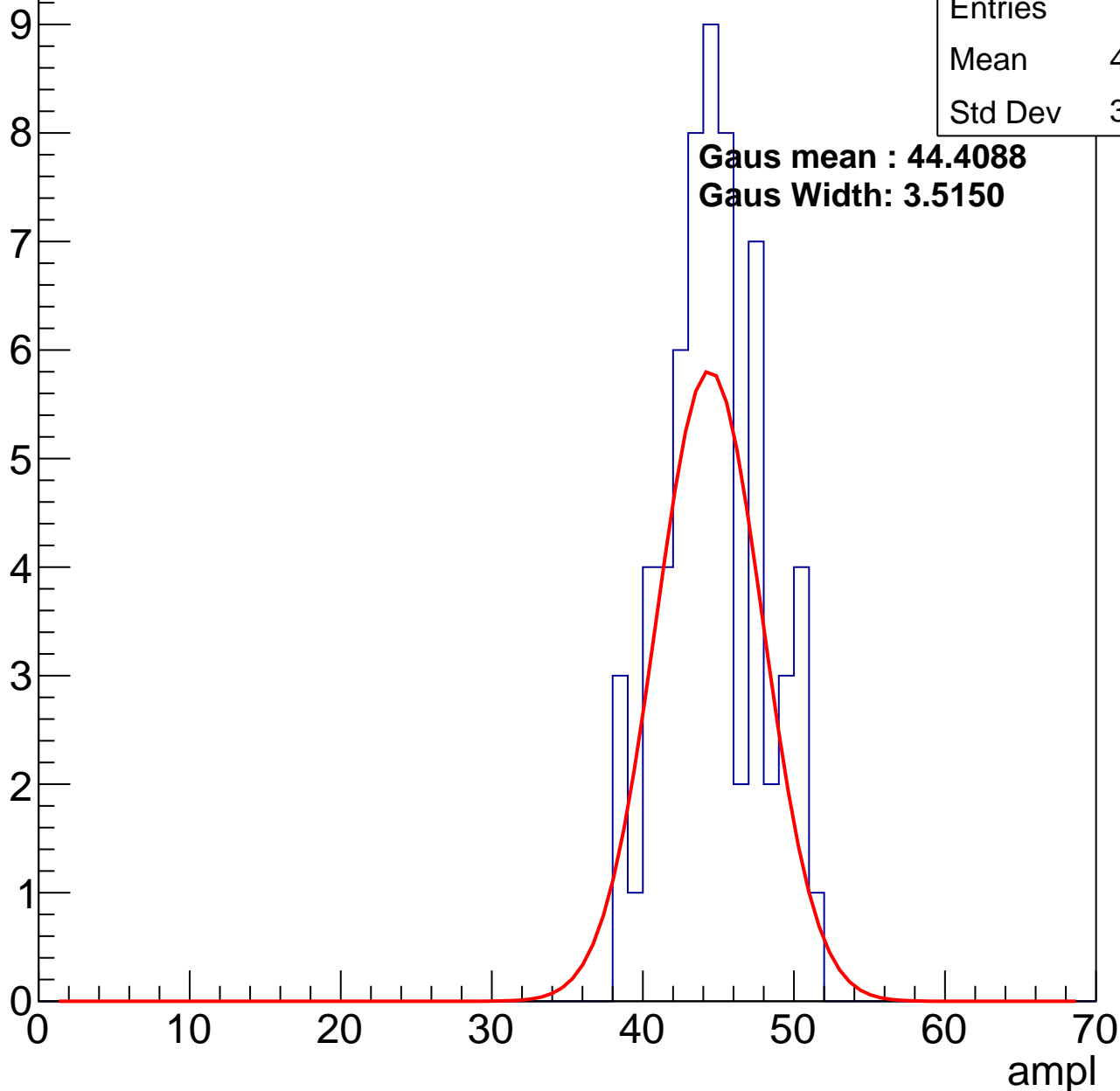
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	44.26
Std Dev	3.213

**Gaus mean : 44.4088**

**Gaus Width: 3.5150**

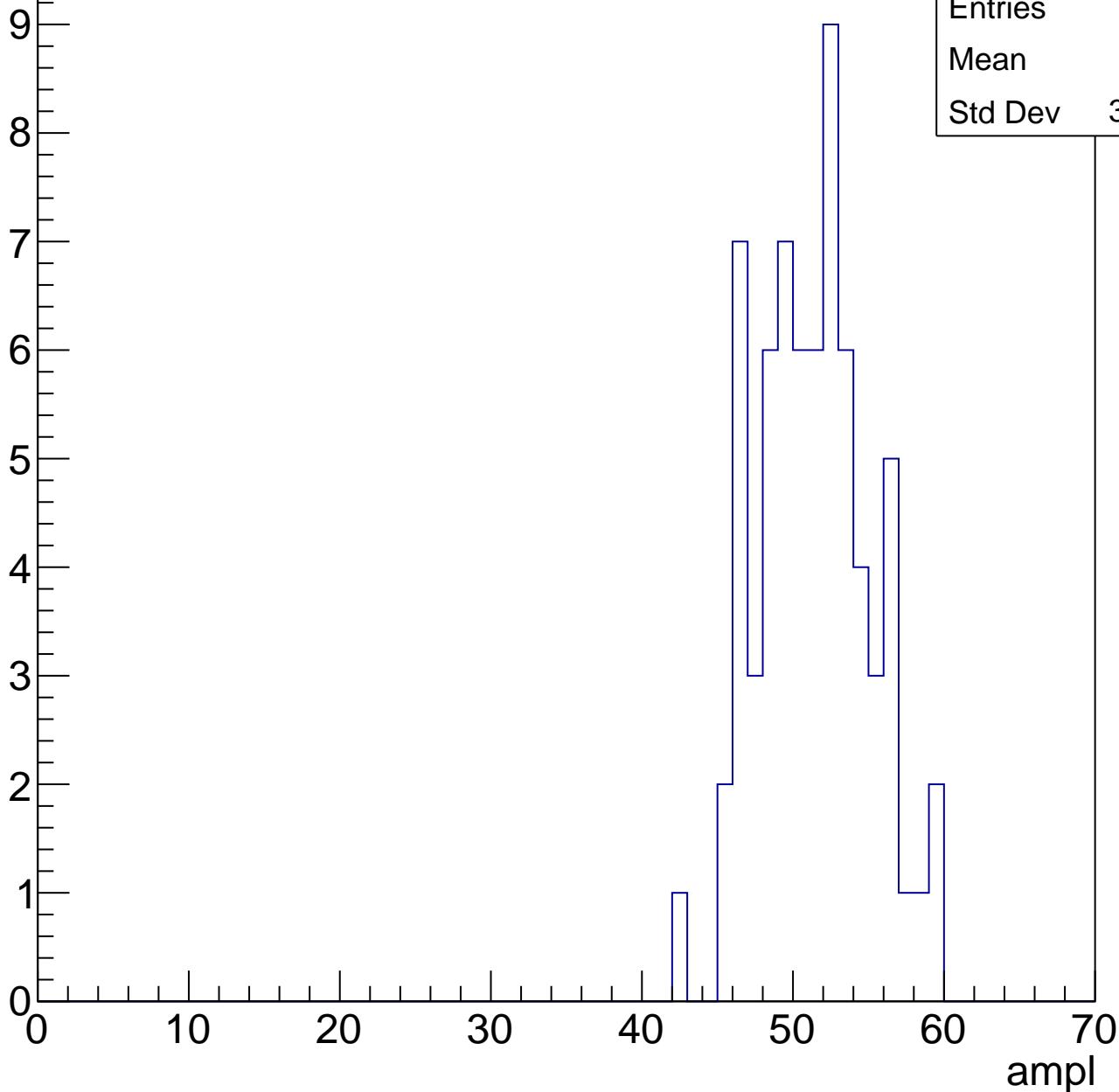


# B1L102S, U20-ch27, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	50.9
Std Dev	3.648

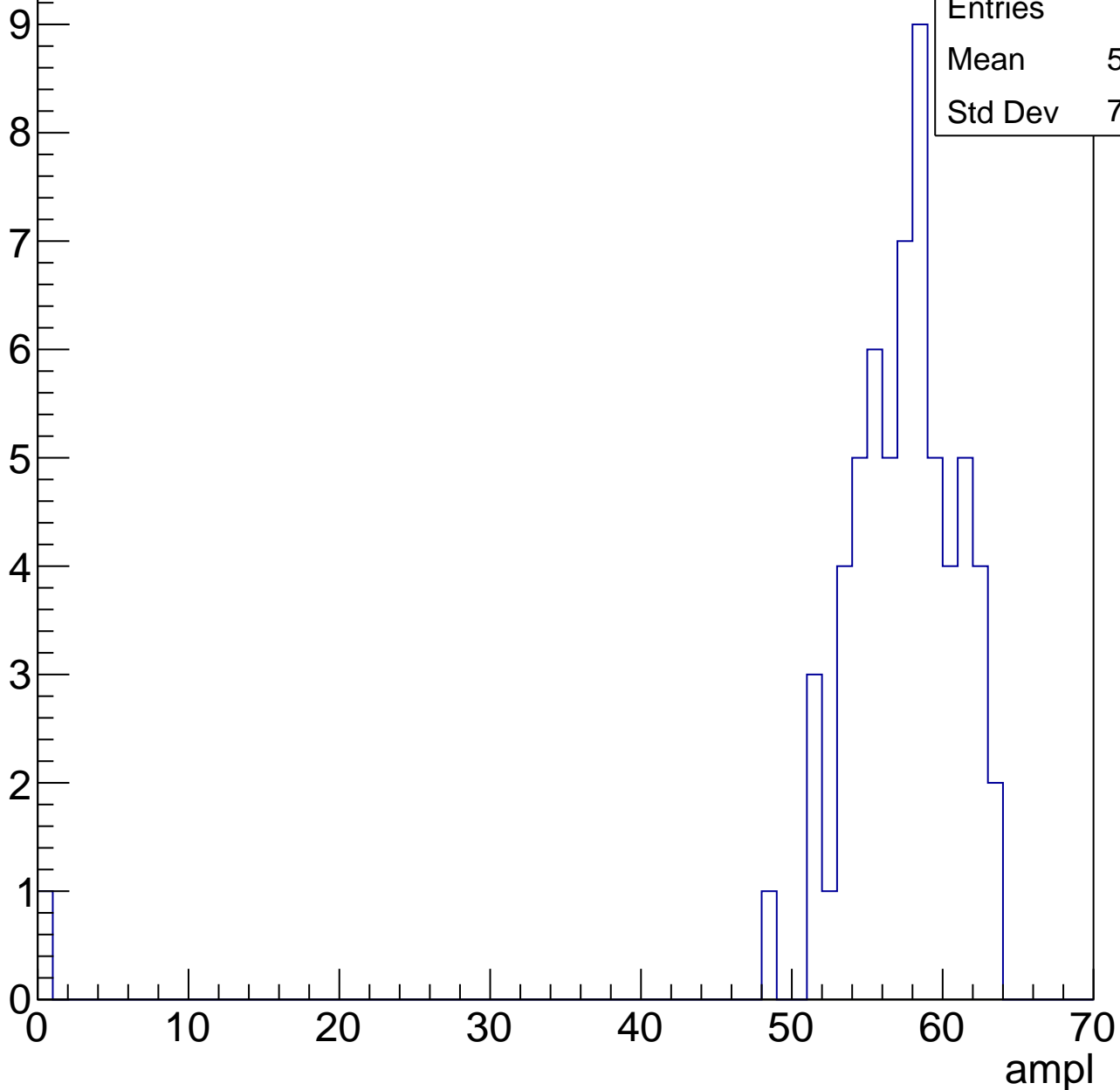


# B1L102S, U20-ch27, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

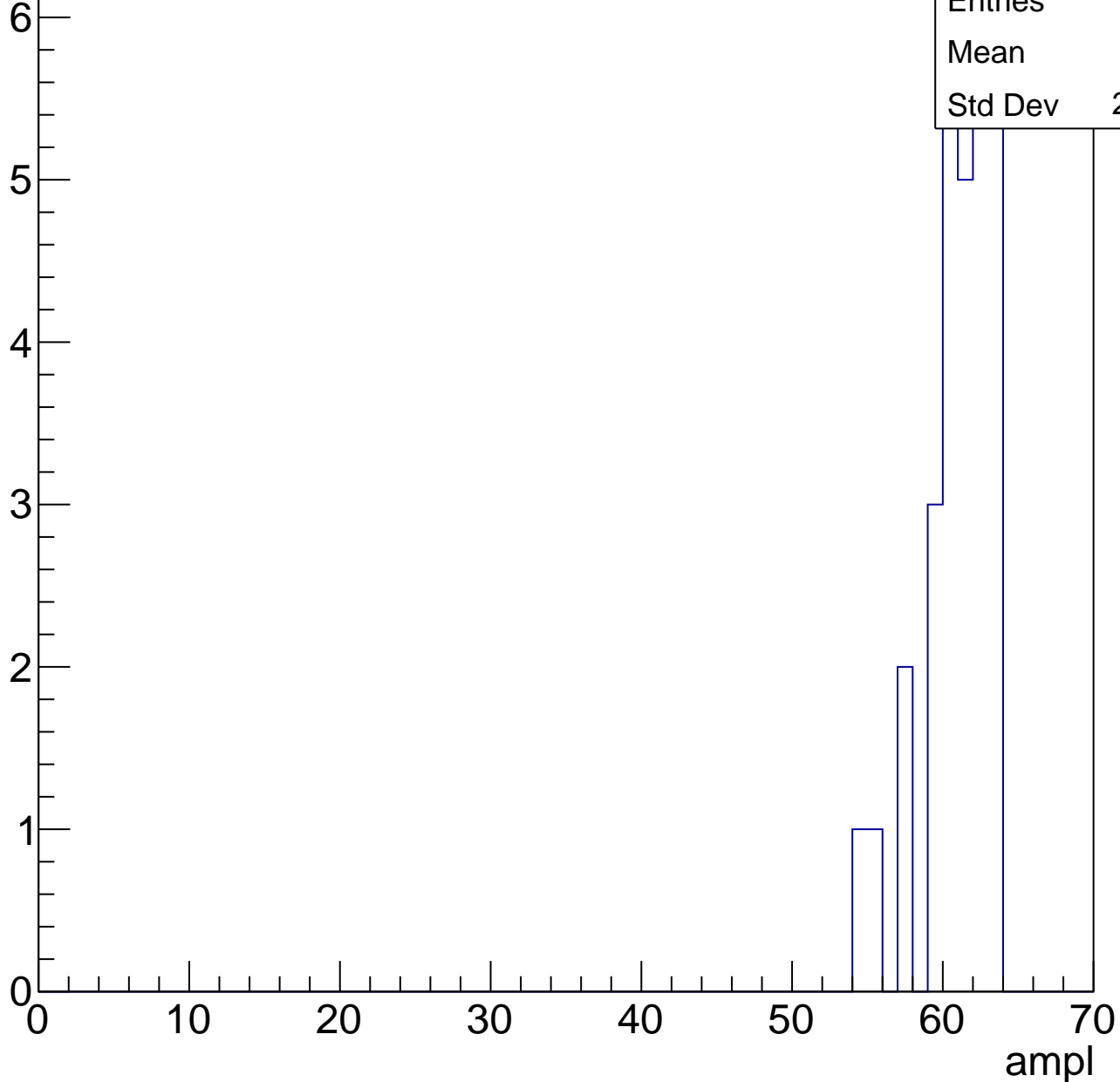
Entries	62
Mean	56.13
Std Dev	7.902



# B1L102S, U20-ch27, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch27, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U20-ch27, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U20-ch28, adc0

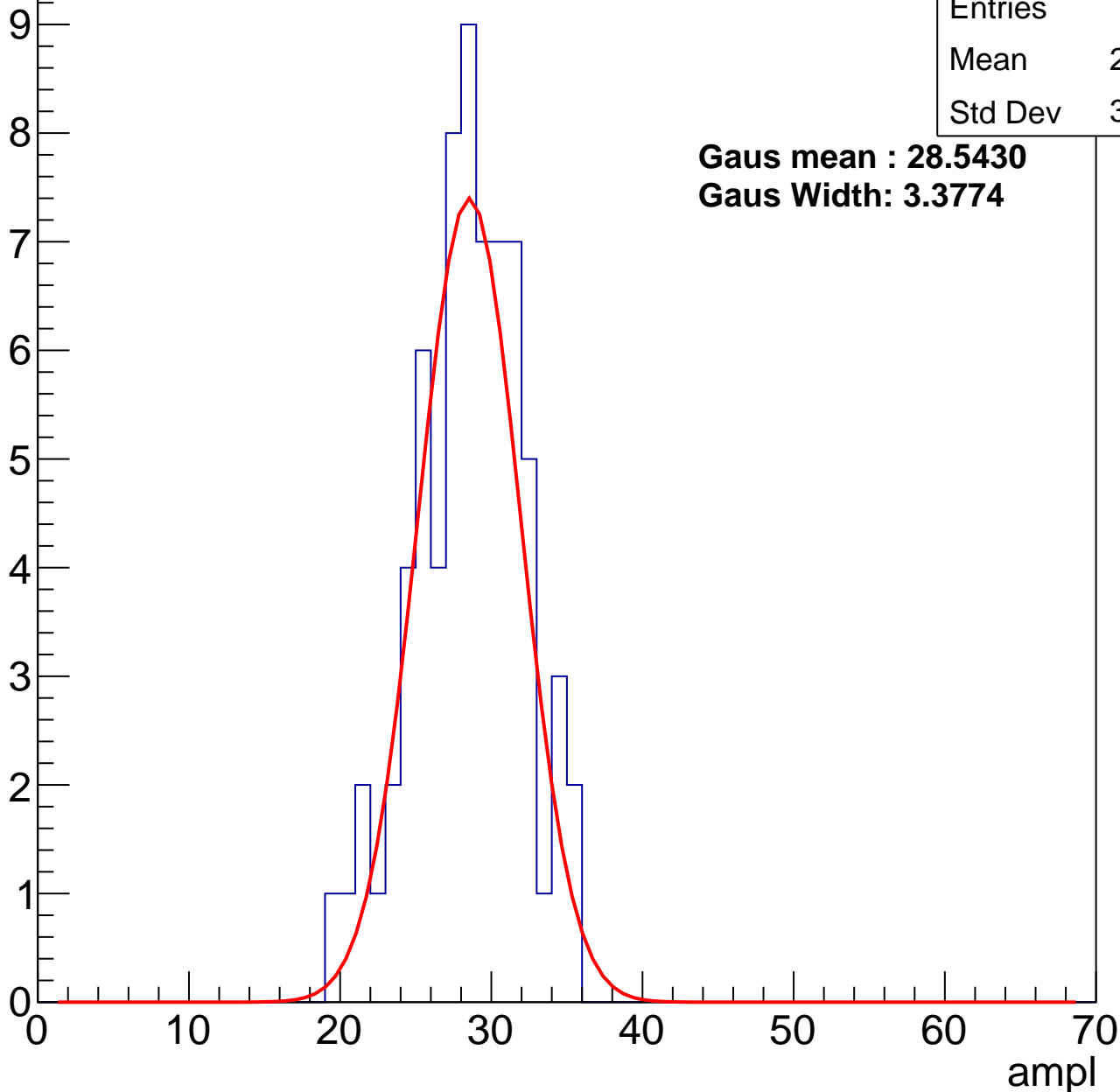
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	28.03
Std Dev	3.546

**Gaus mean : 28.5430**

**Gaus Width: 3.3774**



# B1L102S, U20-ch28, adc1

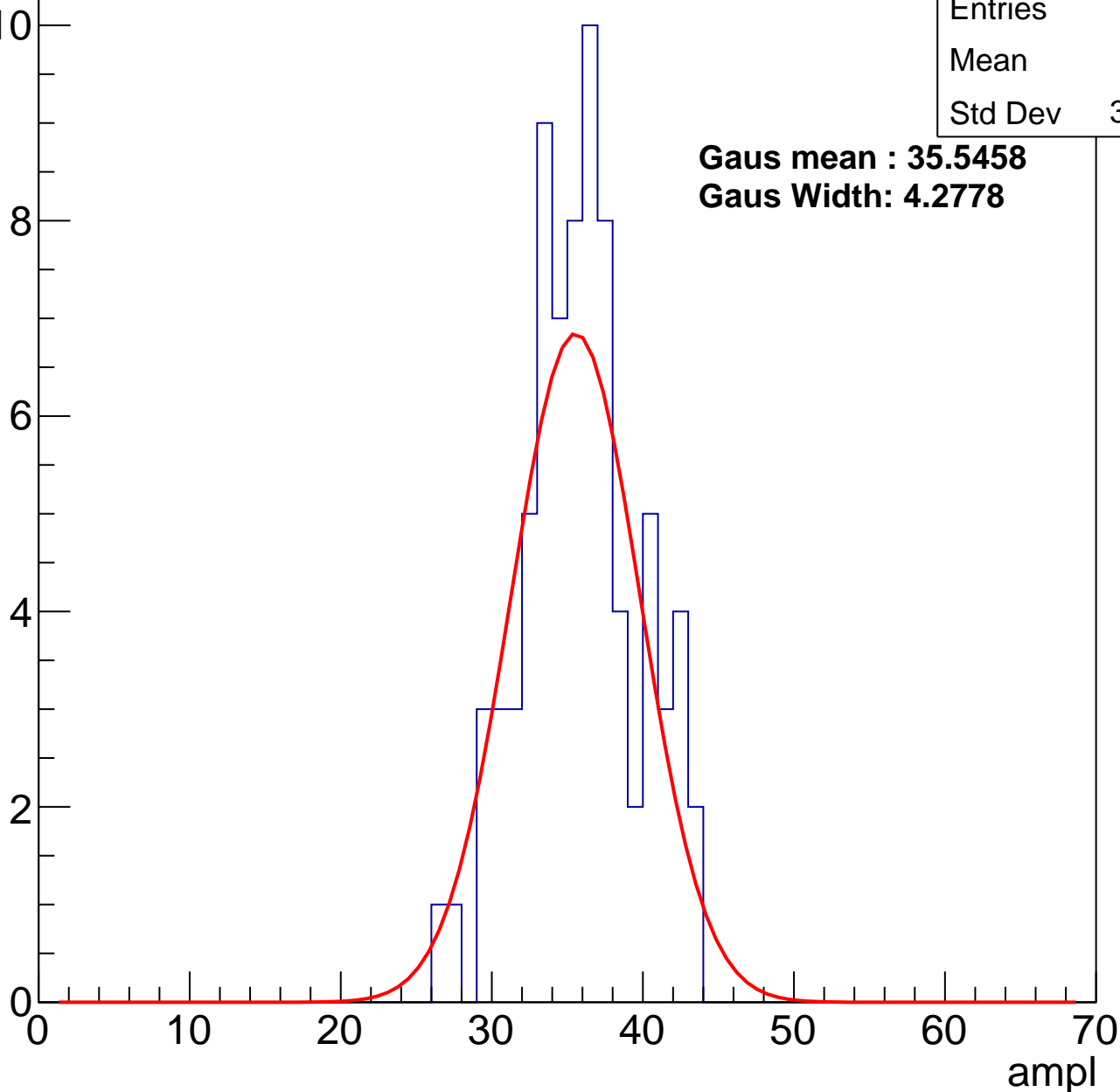
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	78
Mean	35.4
Std Dev	3.787

**Gaus mean : 35.5458**

**Gaus Width: 4.2778**



# B1L102S, U20-ch28, adc2

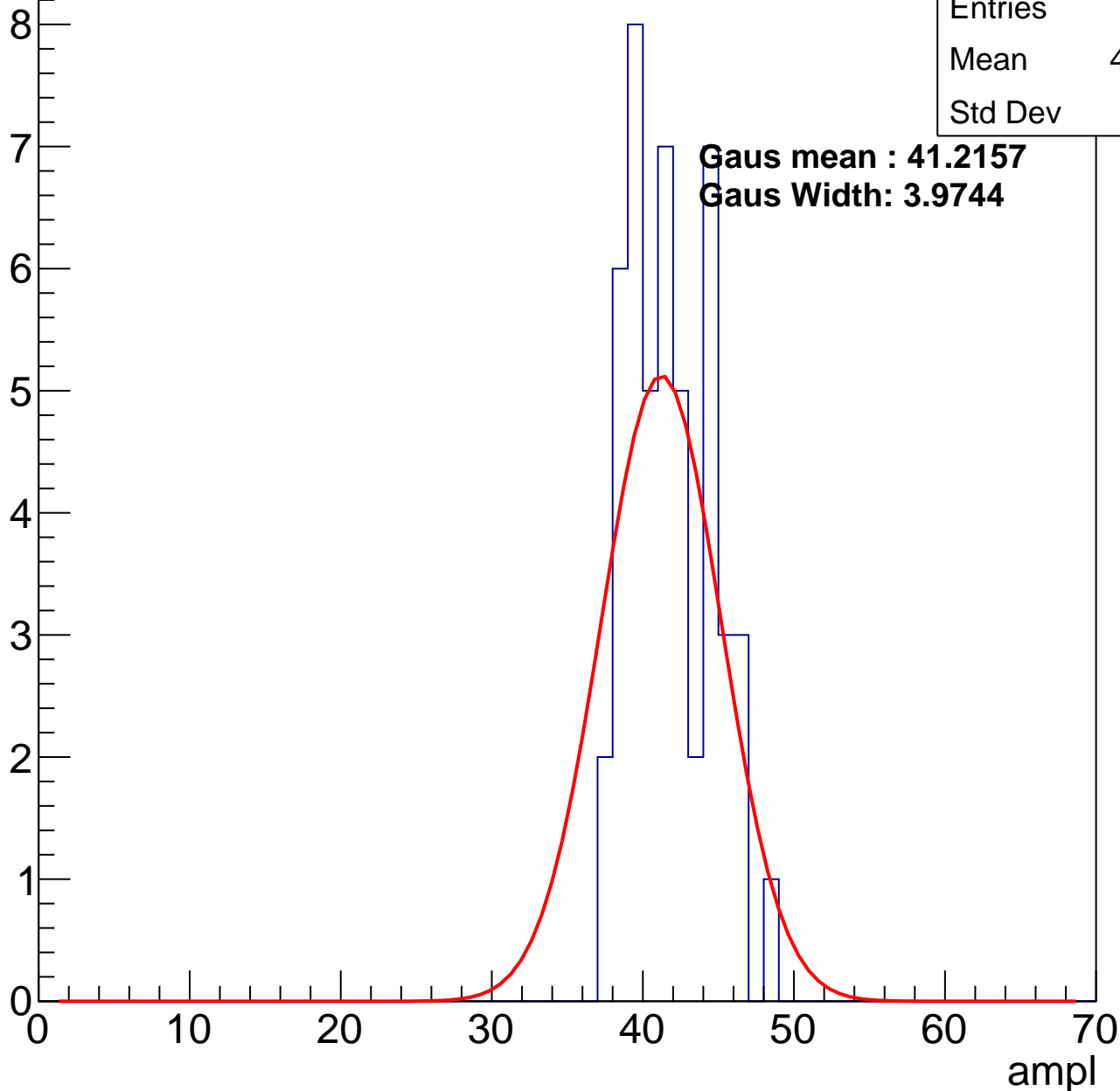
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	41.35
Std Dev	2.73

**Gaus mean : 41.2157**

**Gaus Width: 3.9744**



# B1L102S, U20-ch28, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

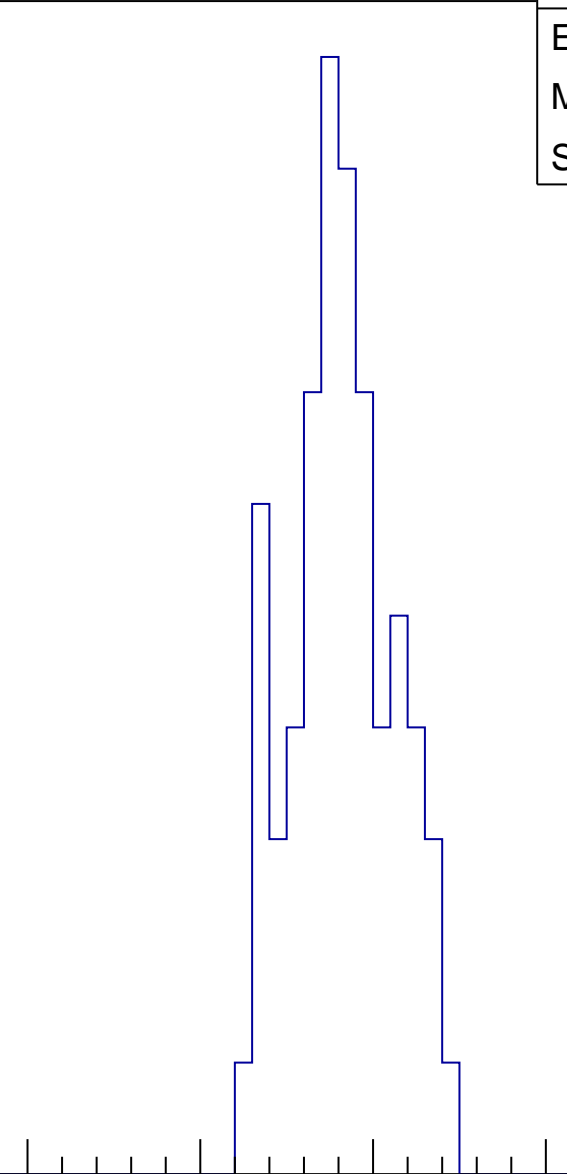
Entries	64
Mean	47.73
Std Dev	2.922

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

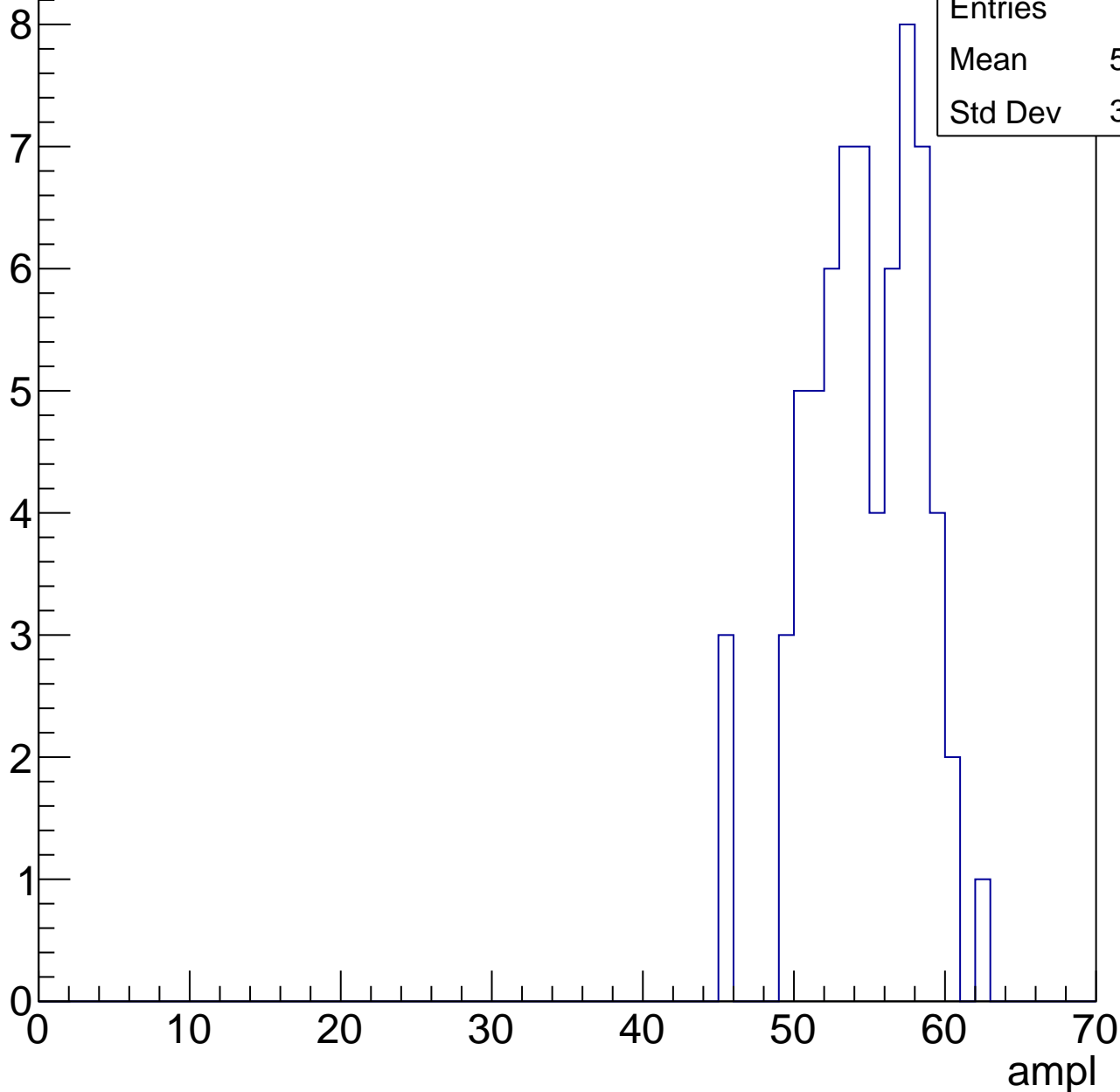


# B1L102S, U20-ch28, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	54.18
Std Dev	3.678

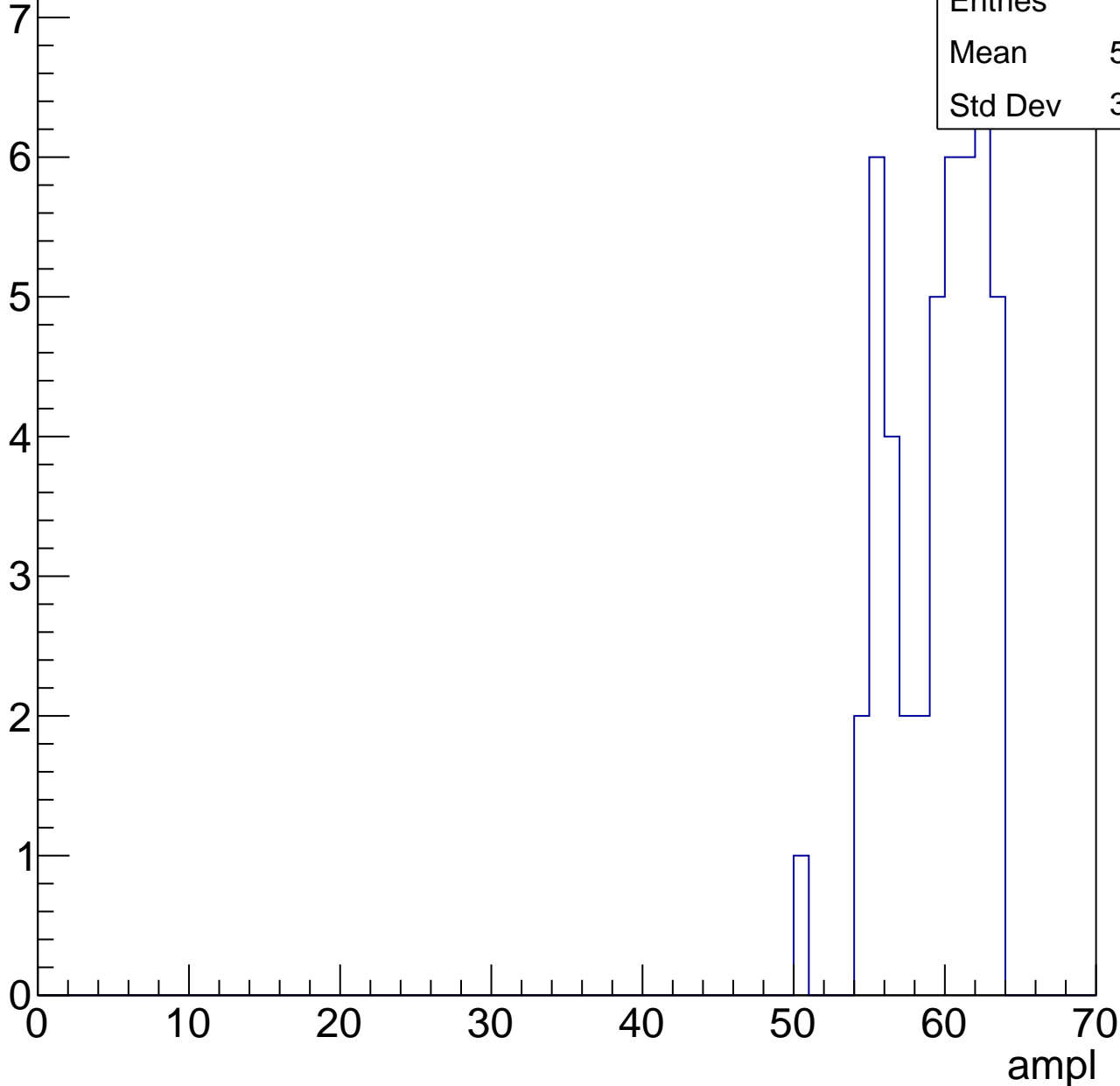


# B1L102S, U20-ch28, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	46
Mean	58.96
Std Dev	3.113

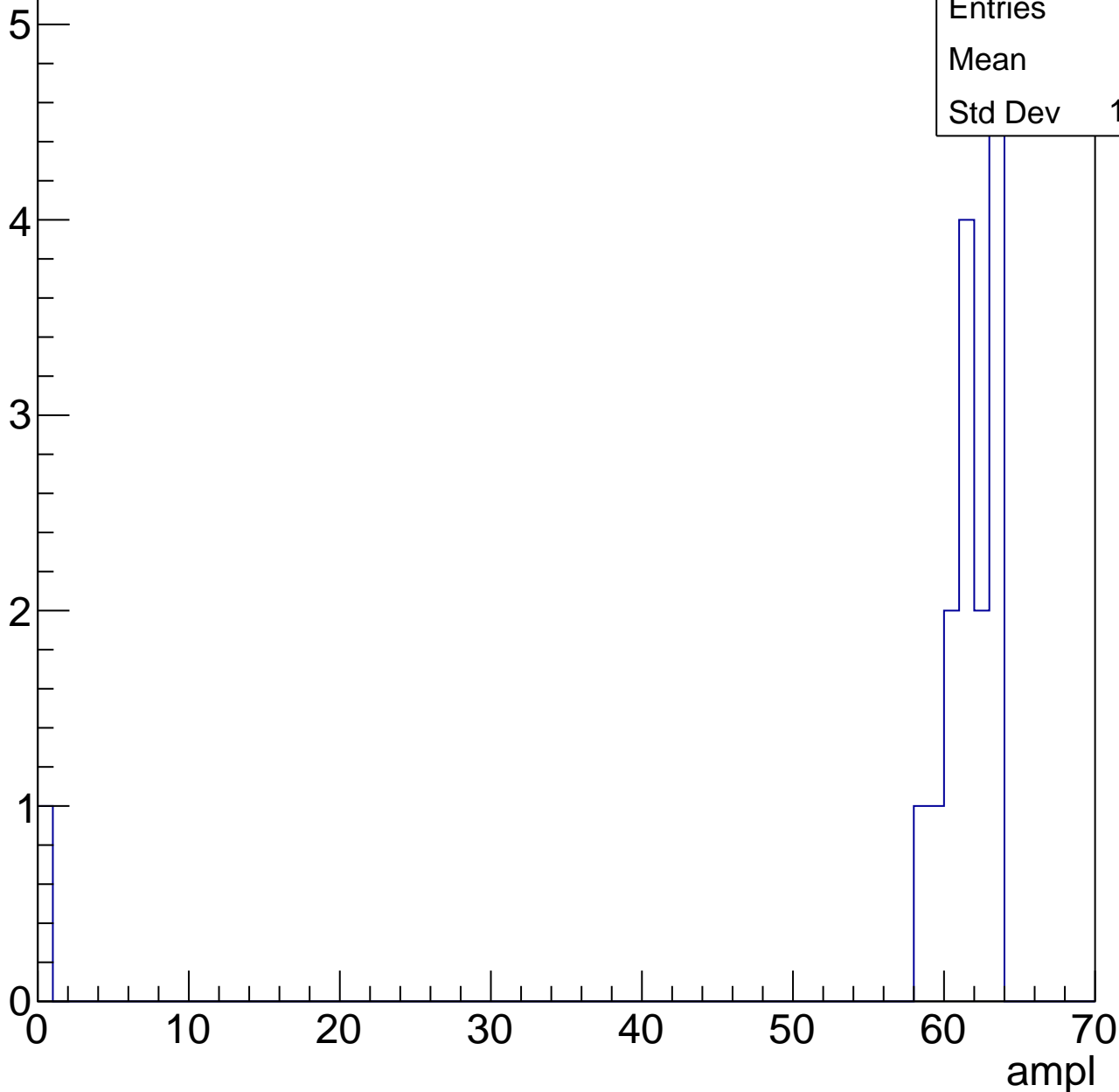


# B1L102S, U20-ch28, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	16
Mean	57.5
Std Dev	14.92





# B1L102S, U20-ch28, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U20-ch29, adc0

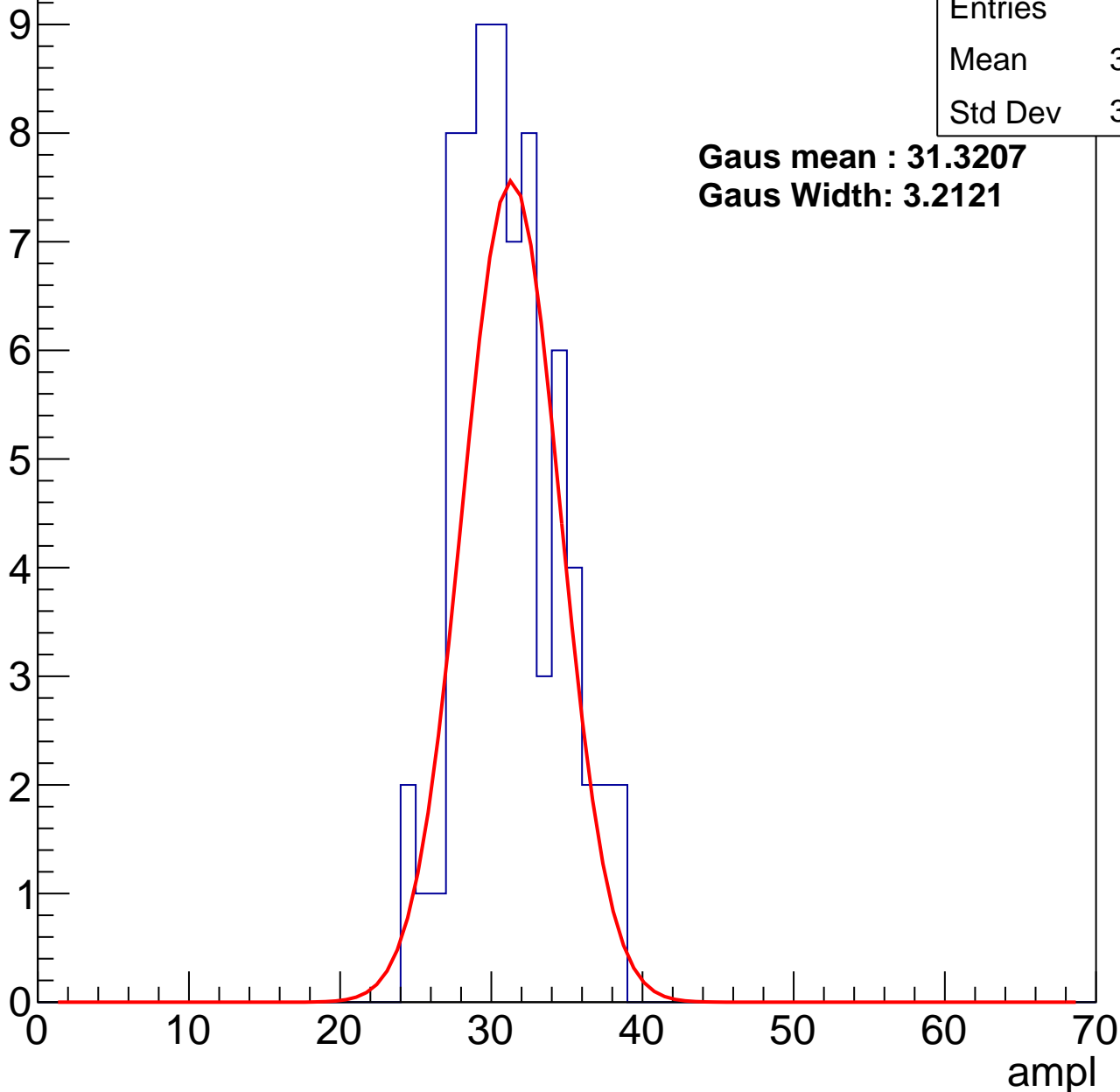
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	30.67
Std Dev	3.236

**Gaus mean : 31.3207**

**Gaus Width: 3.2121**



# B1L102S, U20-ch29, adc1

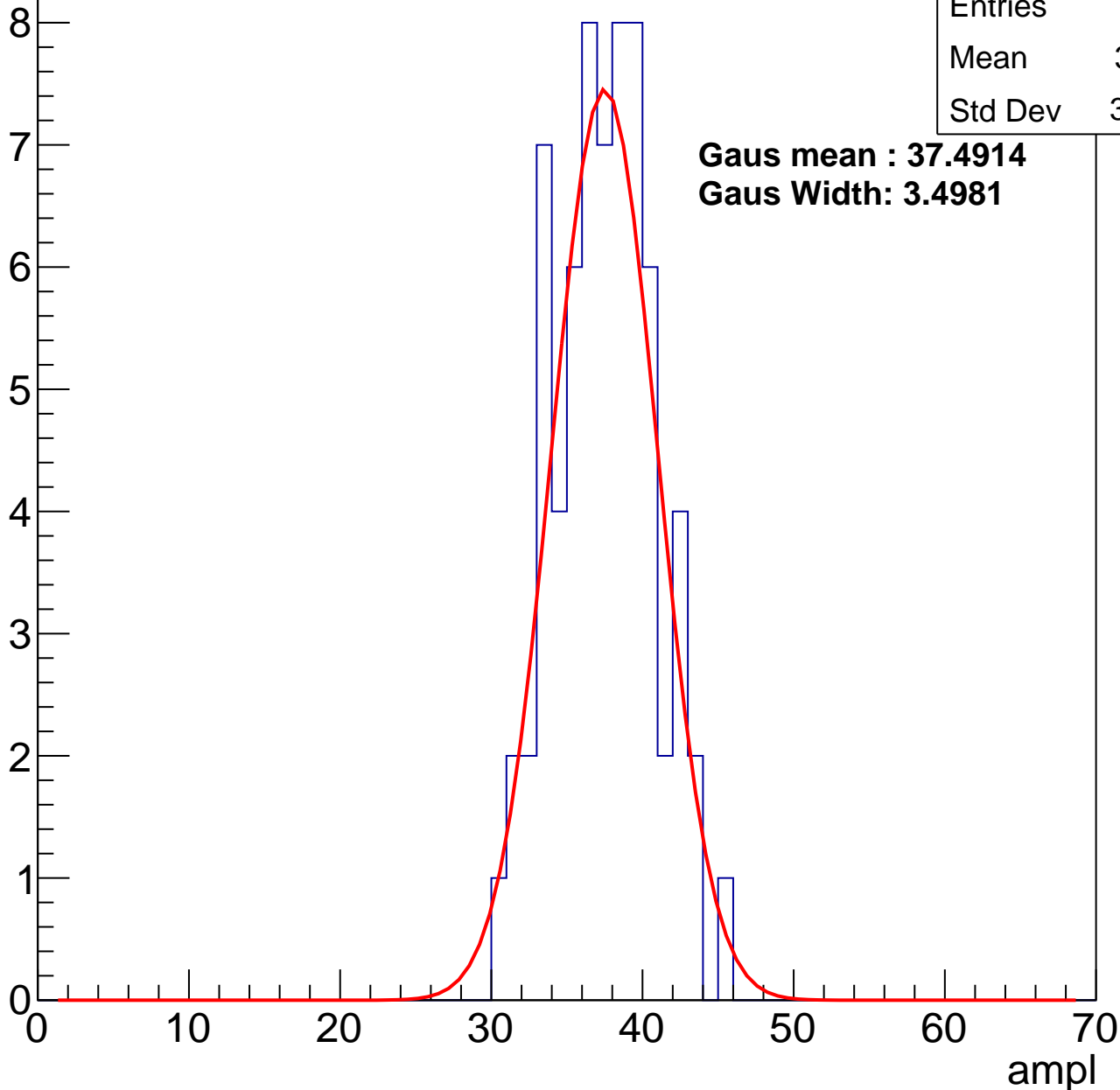
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	37.01
Std Dev	3.238

**Gaus mean : 37.4914**

**Gaus Width: 3.4981**



# B1L102S, U20-ch29, adc2

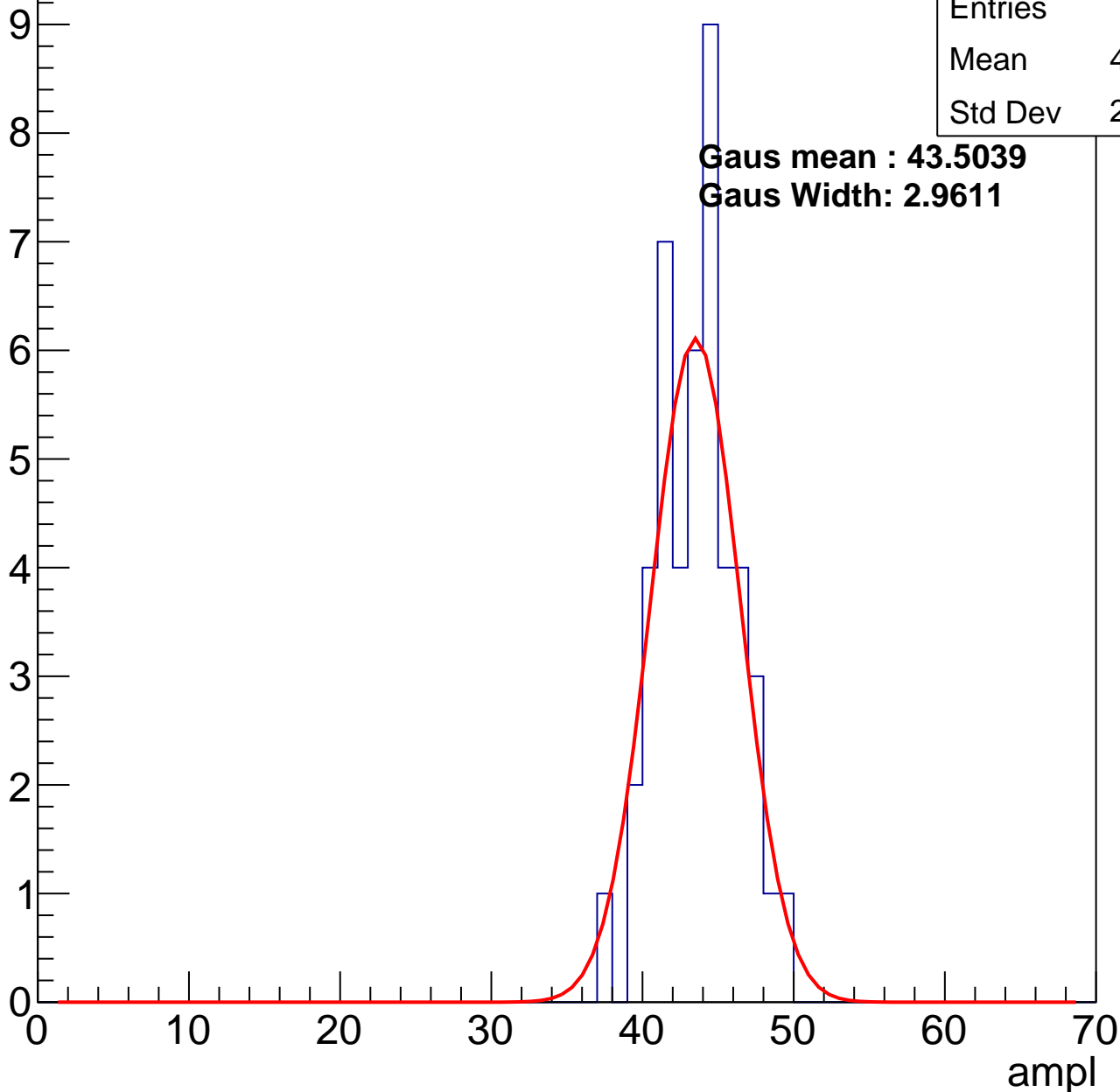
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	46
Mean	43.17
Std Dev	2.573

**Gaus mean : 43.5039**

**Gaus Width: 2.9611**



# B1L102S, U20-ch29, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	78
Mean	49.32
Std Dev	3.384

Entry

10

8

6

4

2

0

0

10

20

30

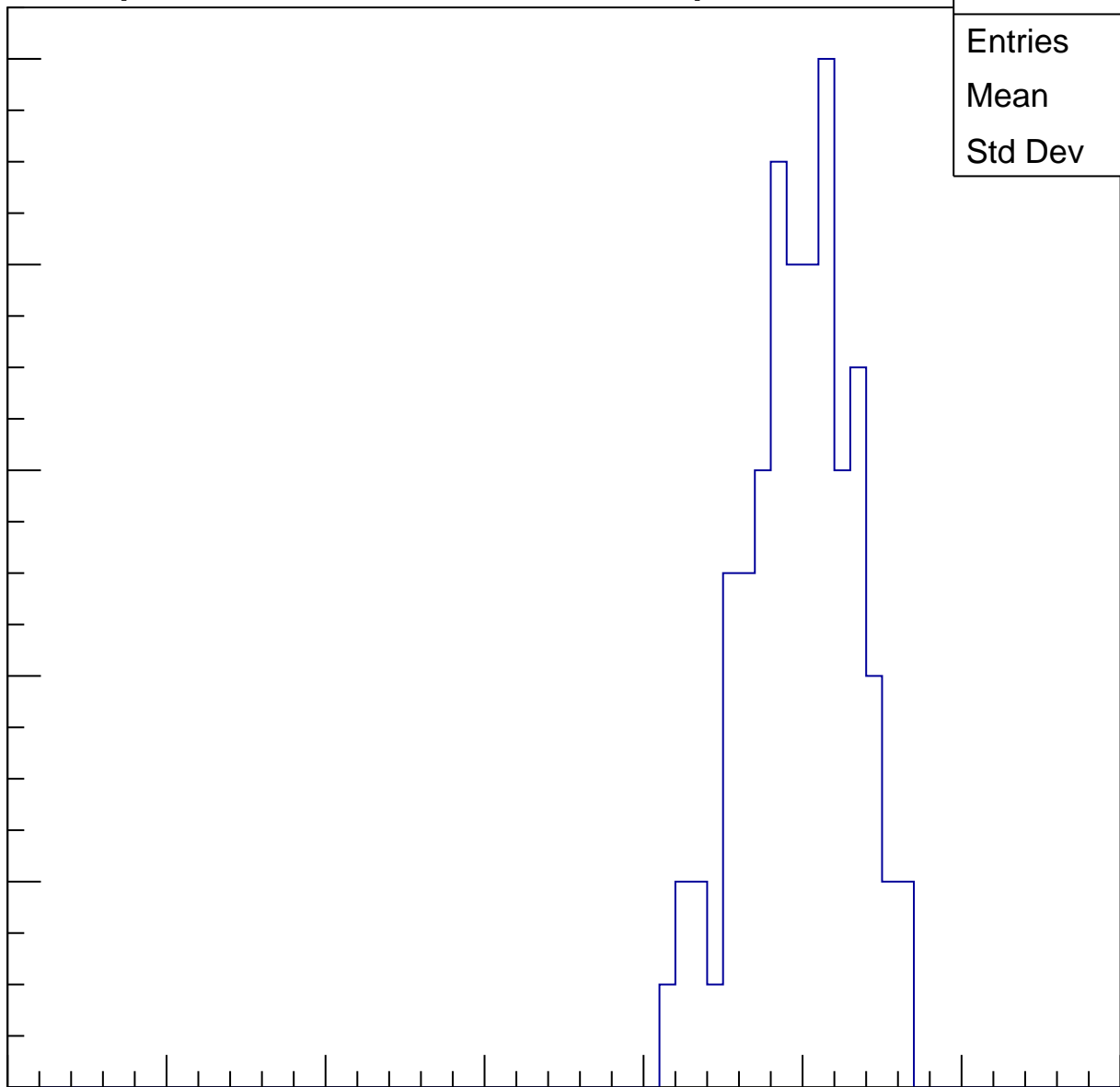
40

50

60

70

ampl

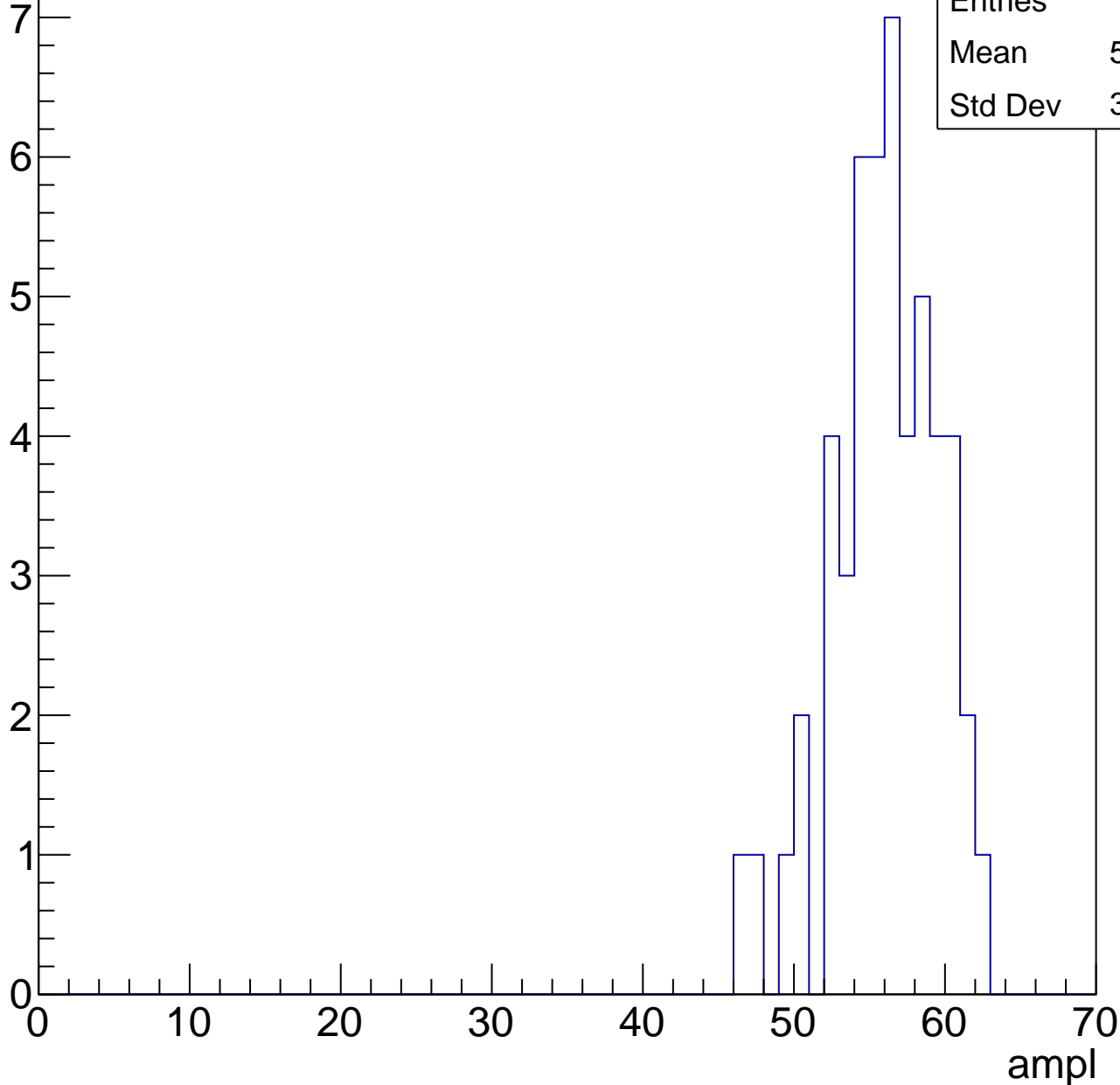


# B1L102S, U20-ch29, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

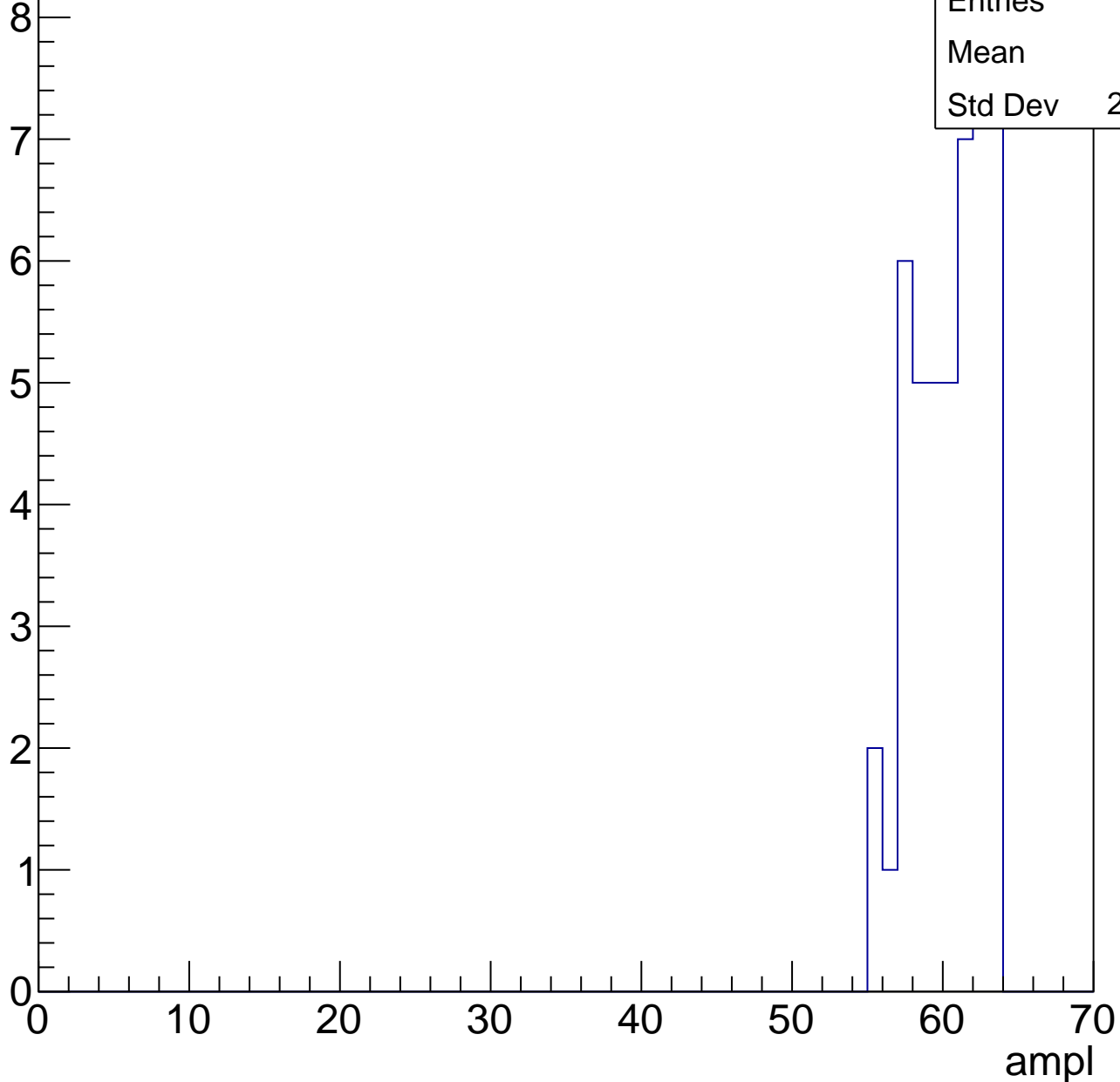
Entries	51
Mean	55.55
Std Dev	3.494



# B1L102S, U20-ch29, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

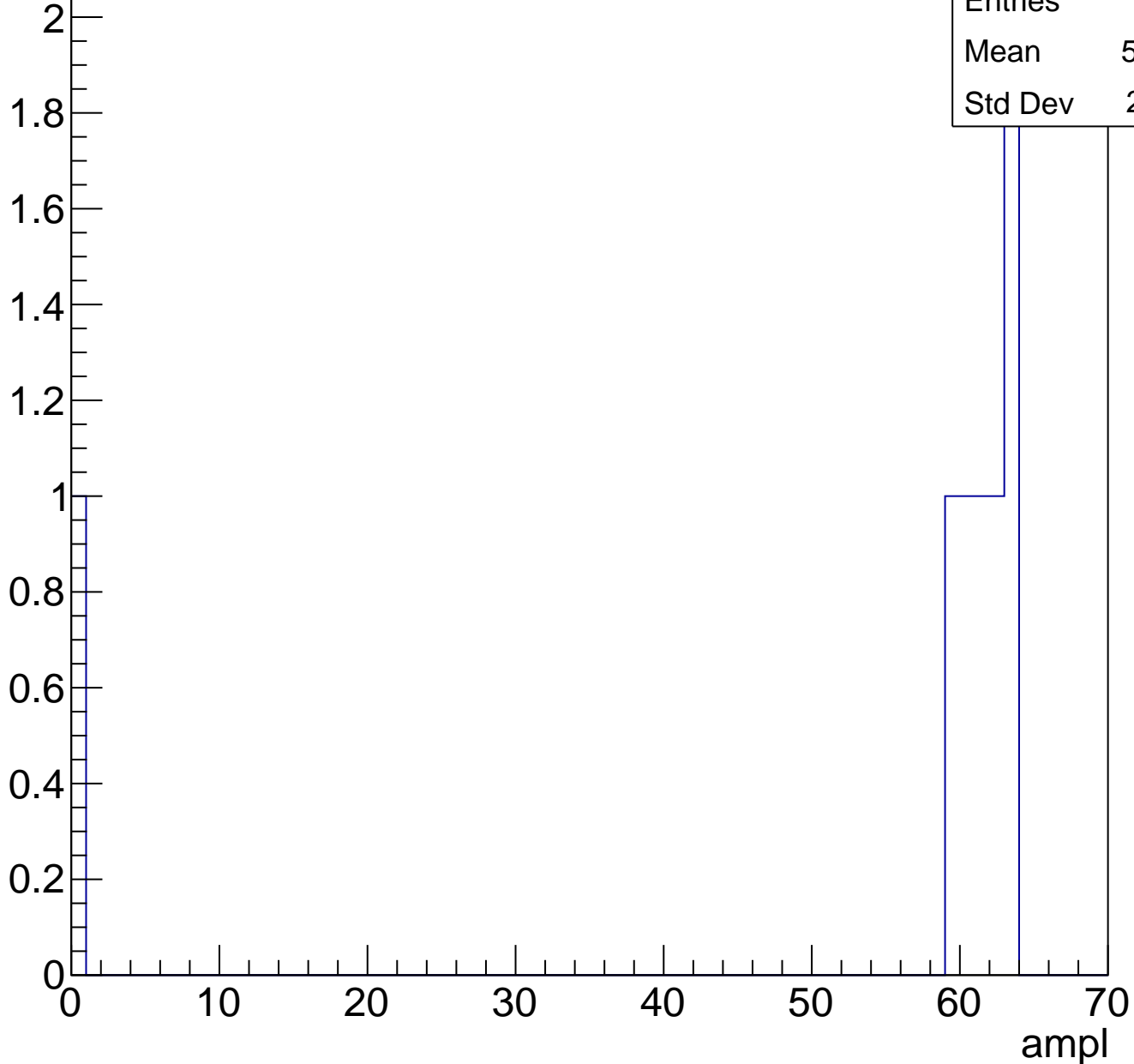


Entries	47
Mean	60
Std Dev	2.334

# B1L102S, U20-ch29, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U20-ch29, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch30, adc0

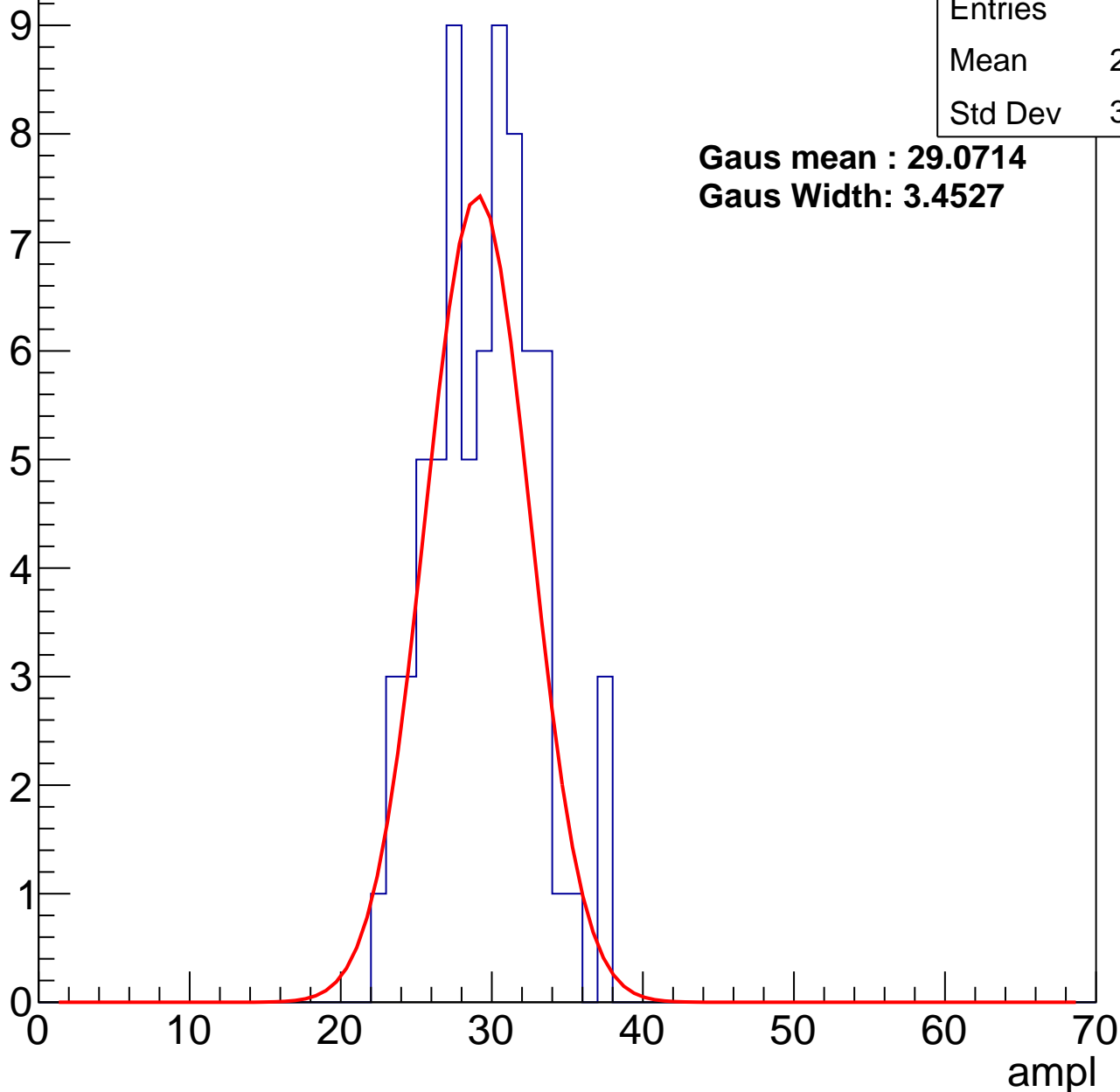
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	29.06
Std Dev	3.443

**Gaus mean : 29.0714**

**Gaus Width: 3.4527**



# B1L102S, U20-ch30, adc1

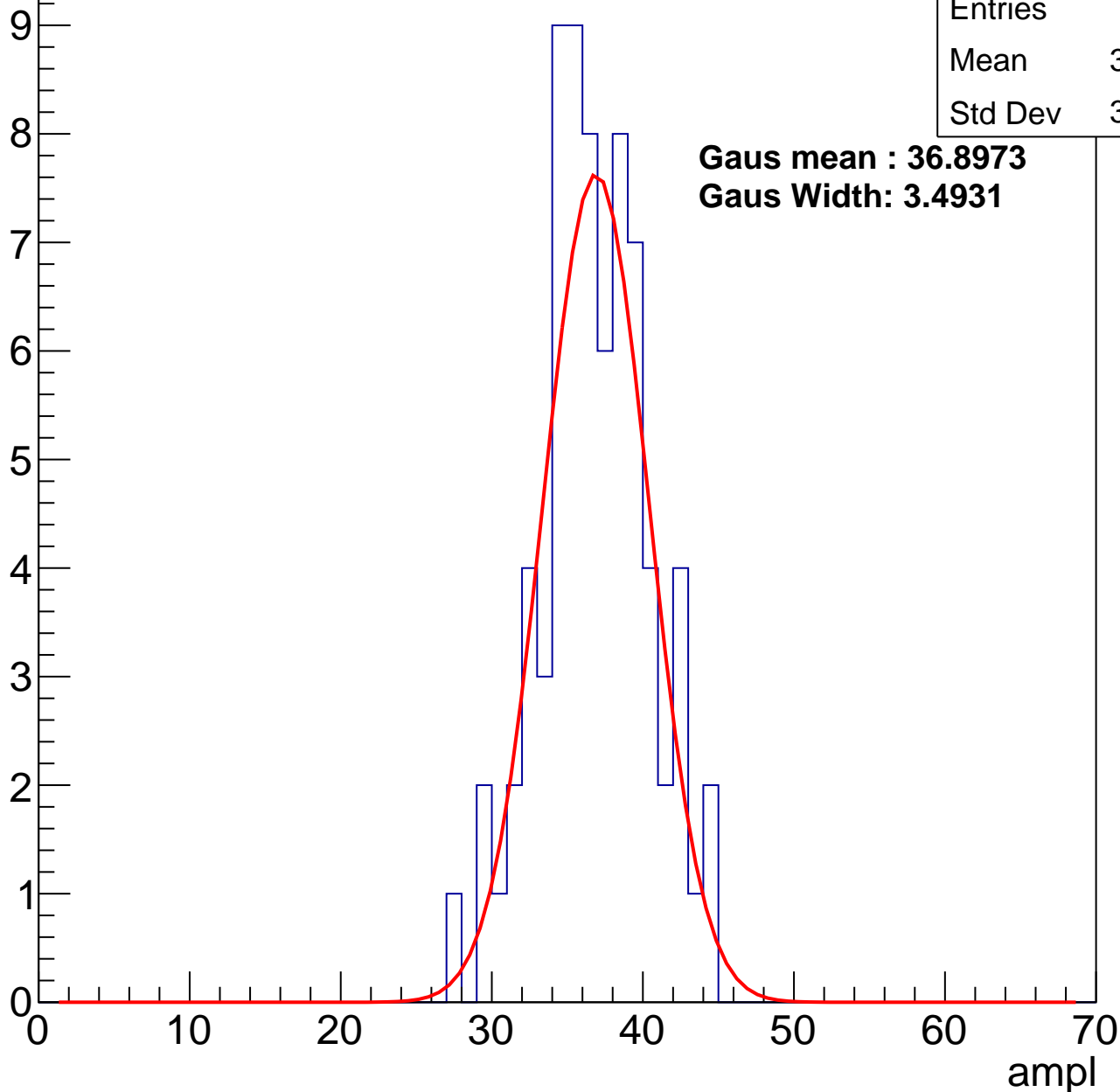
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	36.34
Std Dev	3.566

**Gaus mean : 36.8973**

**Gaus Width: 3.4931**



# B1L102S, U20-ch30, adc2

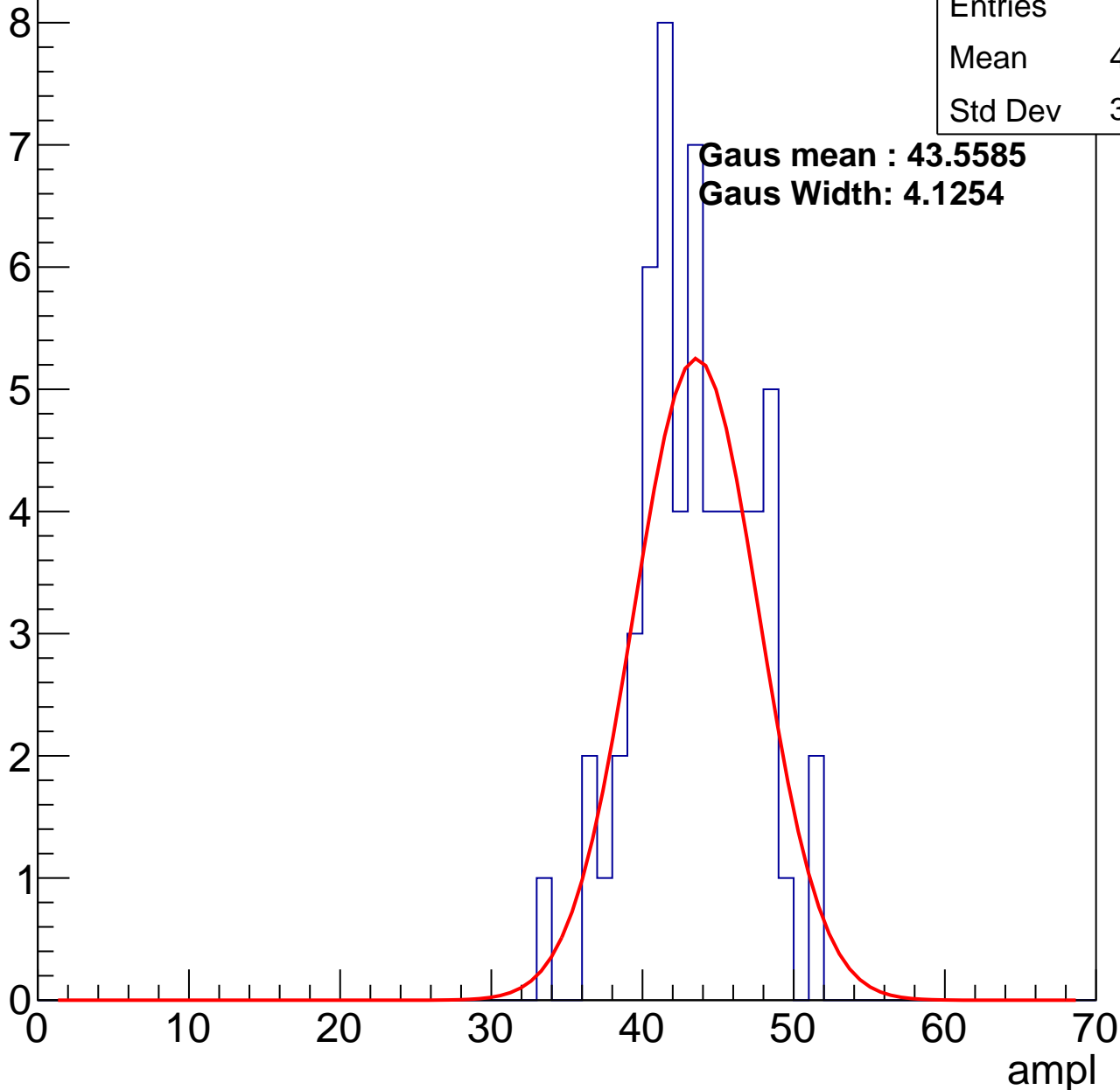
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	42.95
Std Dev	3.785

**Gaus mean : 43.5585**

**Gaus Width: 4.1254**

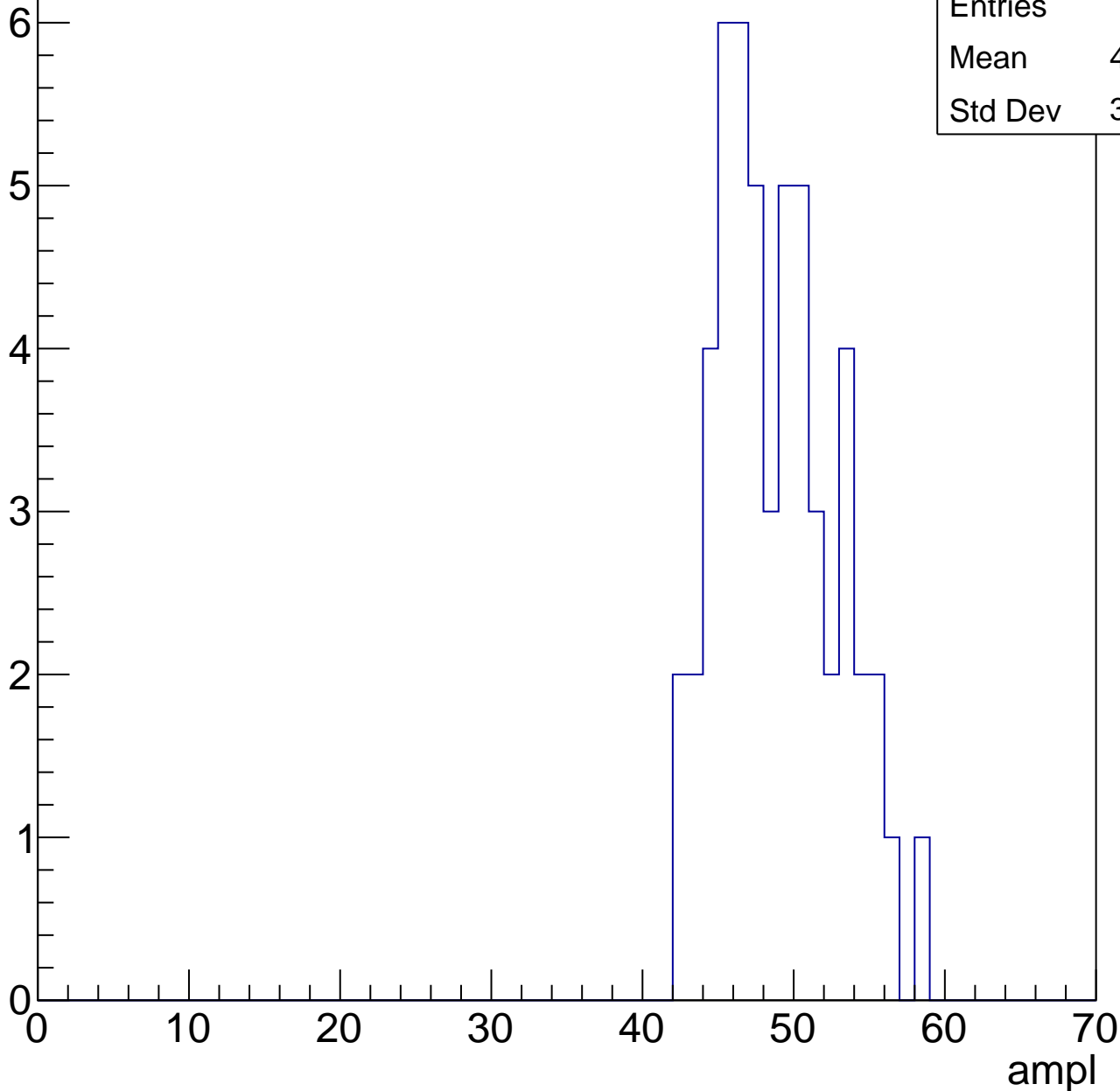


# B1L102S, U20-ch30, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	48.43
Std Dev	3.829

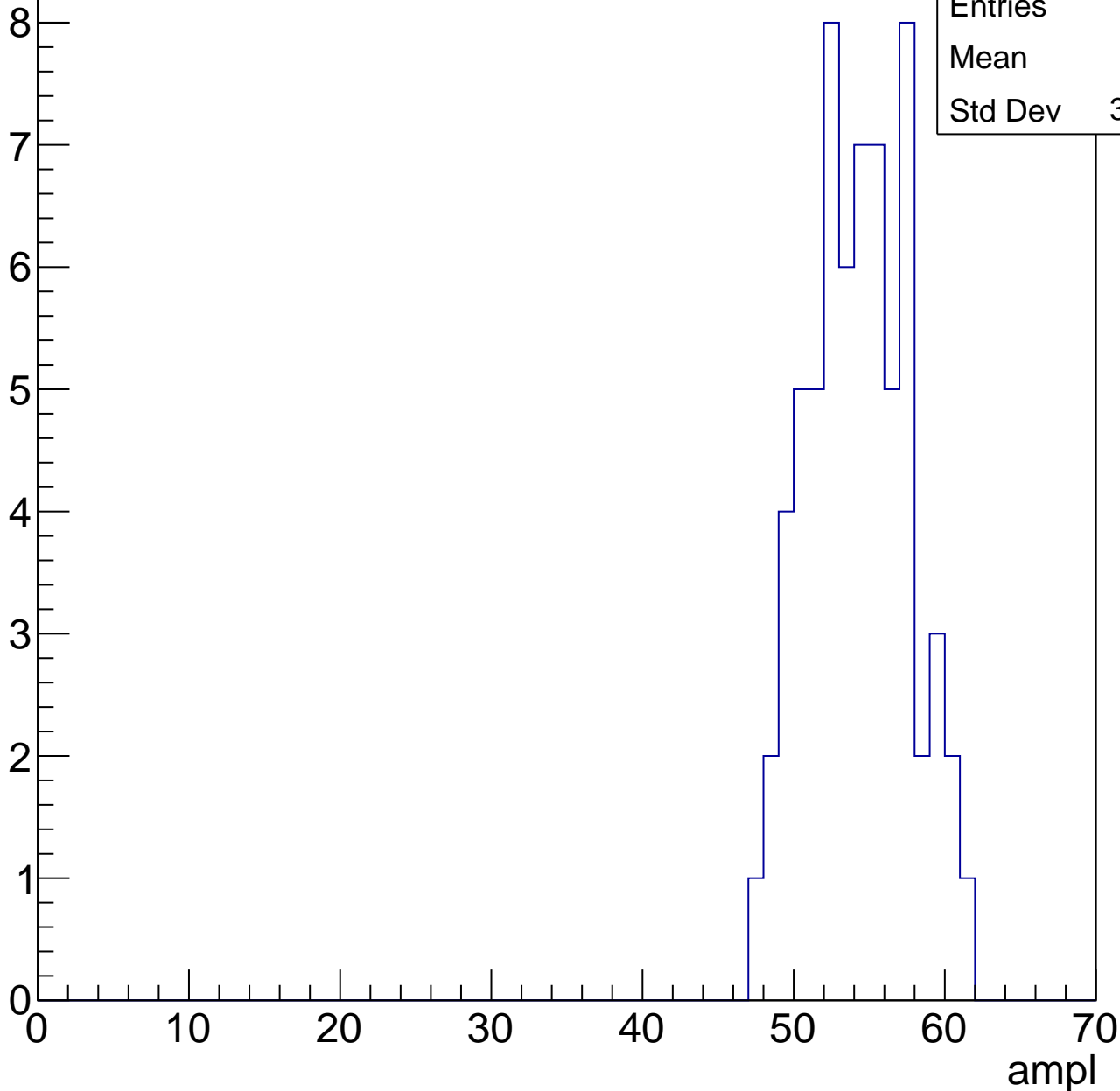


# B1L102S, U20-ch30, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	53.8
Std Dev	3.276



# B1L102S, U20-ch30, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

7

6

5

4

3

2

1

0

Entries

47

Mean

59.66

Std Dev

2.364

ampl

0

10

20

30

40

50

60

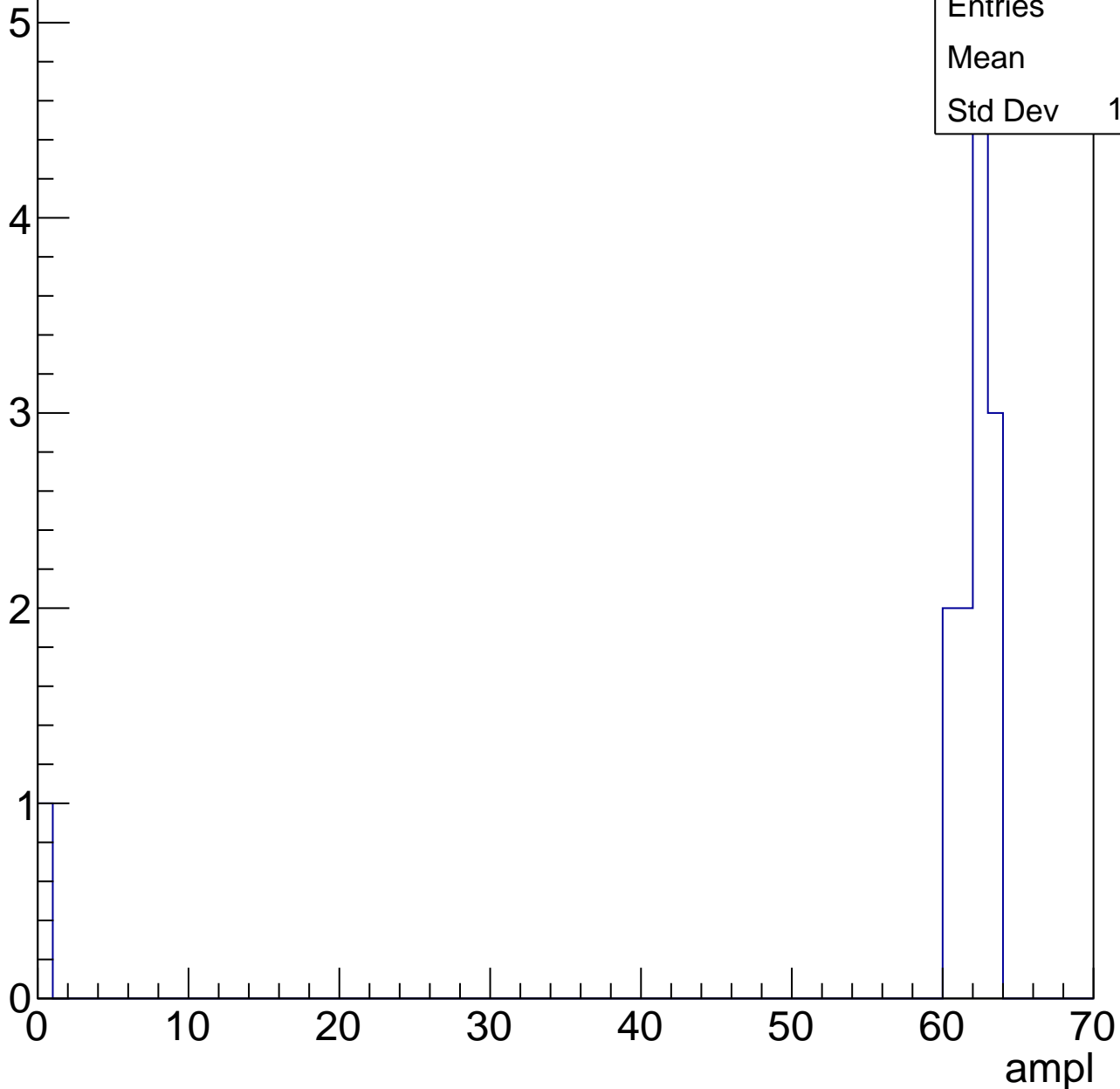
70

# B1L102S, U20-ch30, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	13
Mean	57
Std Dev	16.48





# B1L102S, U20-ch30, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch31, adc0

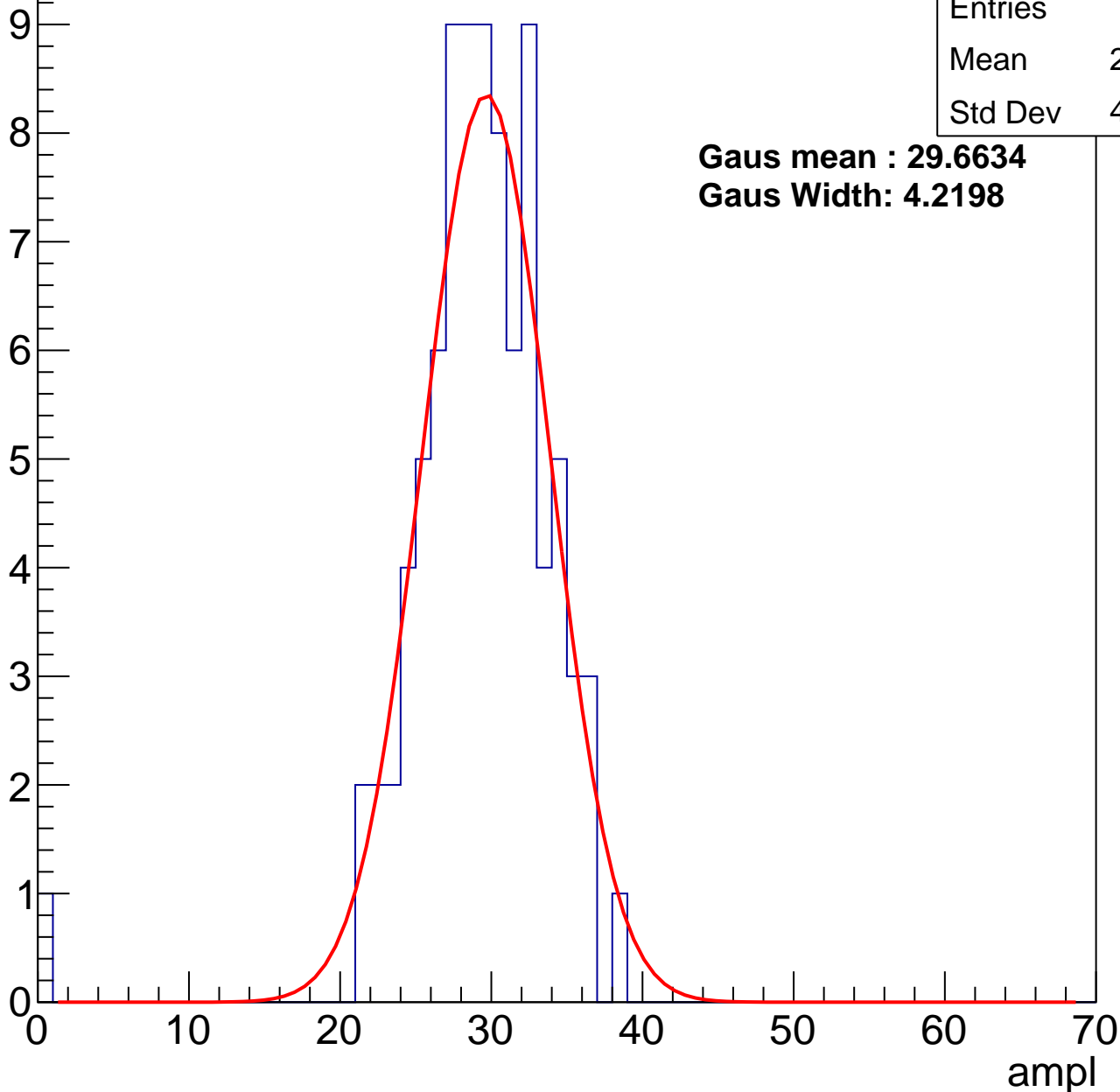
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	88
Mean	28.77
Std Dev	4.828

**Gaus mean : 29.6634**

**Gaus Width: 4.2198**



# B1L102S, U20-ch31, adc1

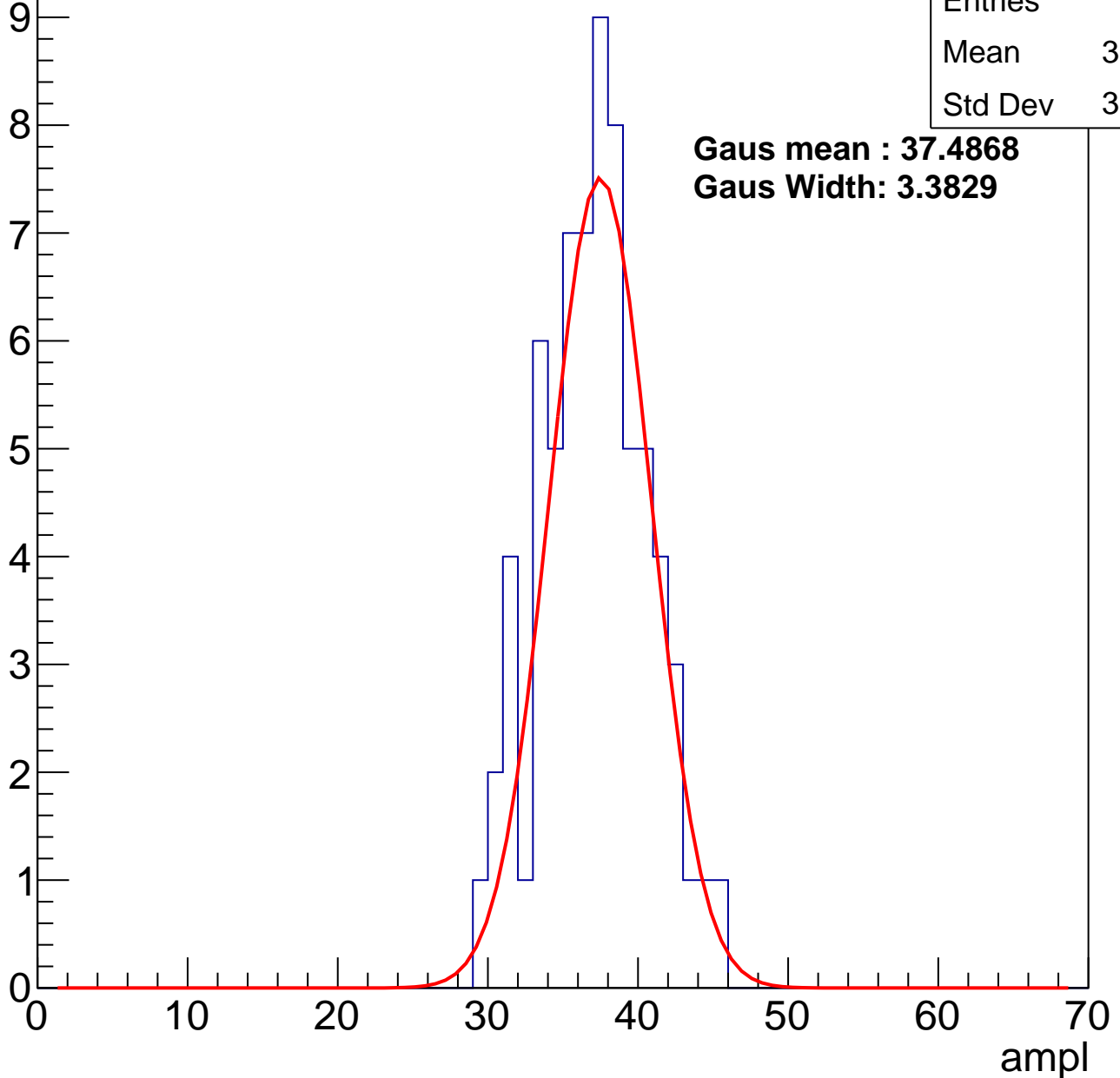
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	36.63
Std Dev	3.502

**Gaus mean : 37.4868**

**Gaus Width: 3.3829**



# B1L102S, U20-ch31, adc2

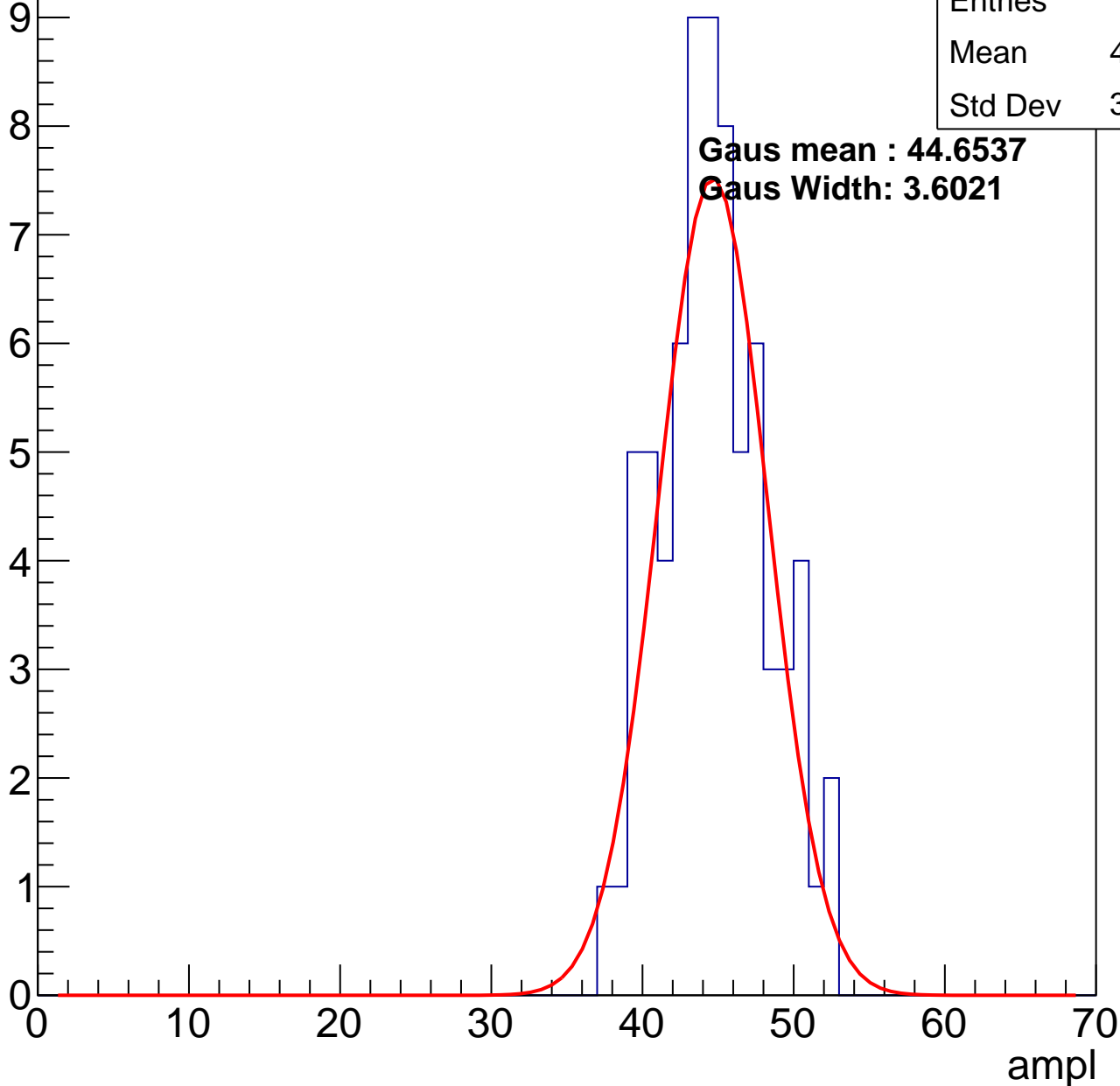
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	44.26
Std Dev	3.496

**Gaus mean : 44.6537**

**Gaus Width: 3.6021**

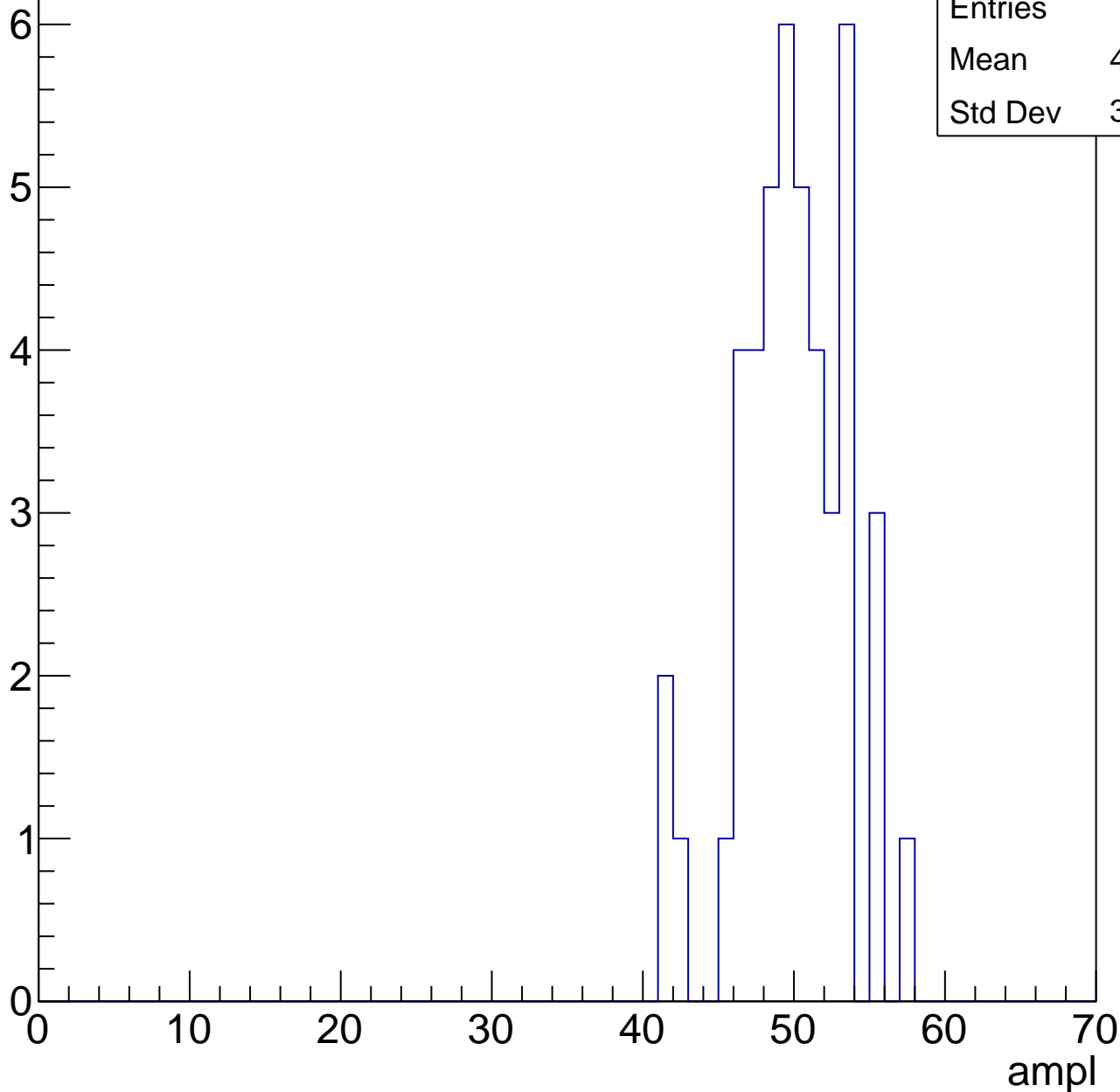


# B1L102S, U20-ch31, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	45
Mean	49.44
Std Dev	3.519

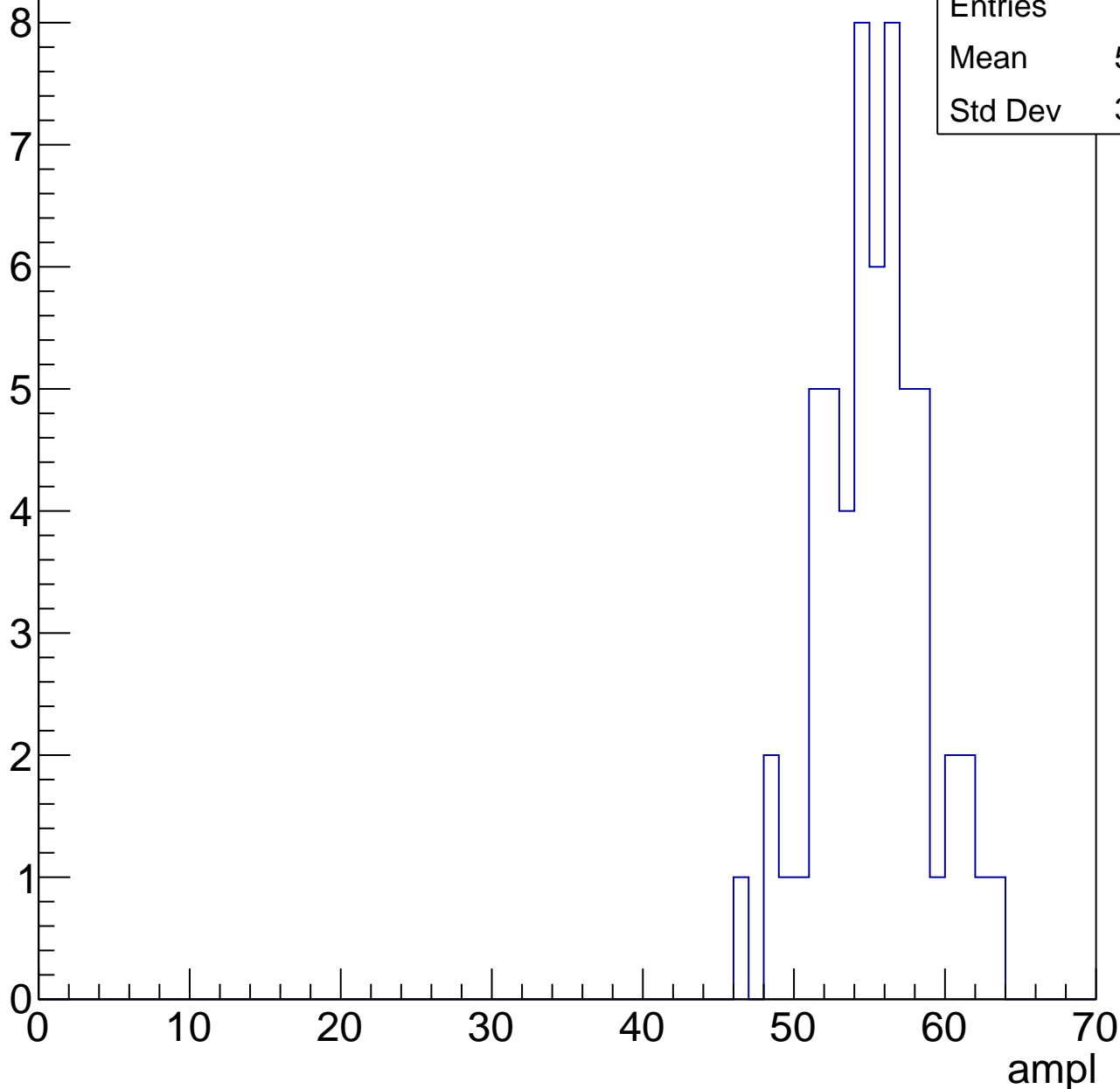


# B1L102S, U20-ch31, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	54.81
Std Dev	3.501

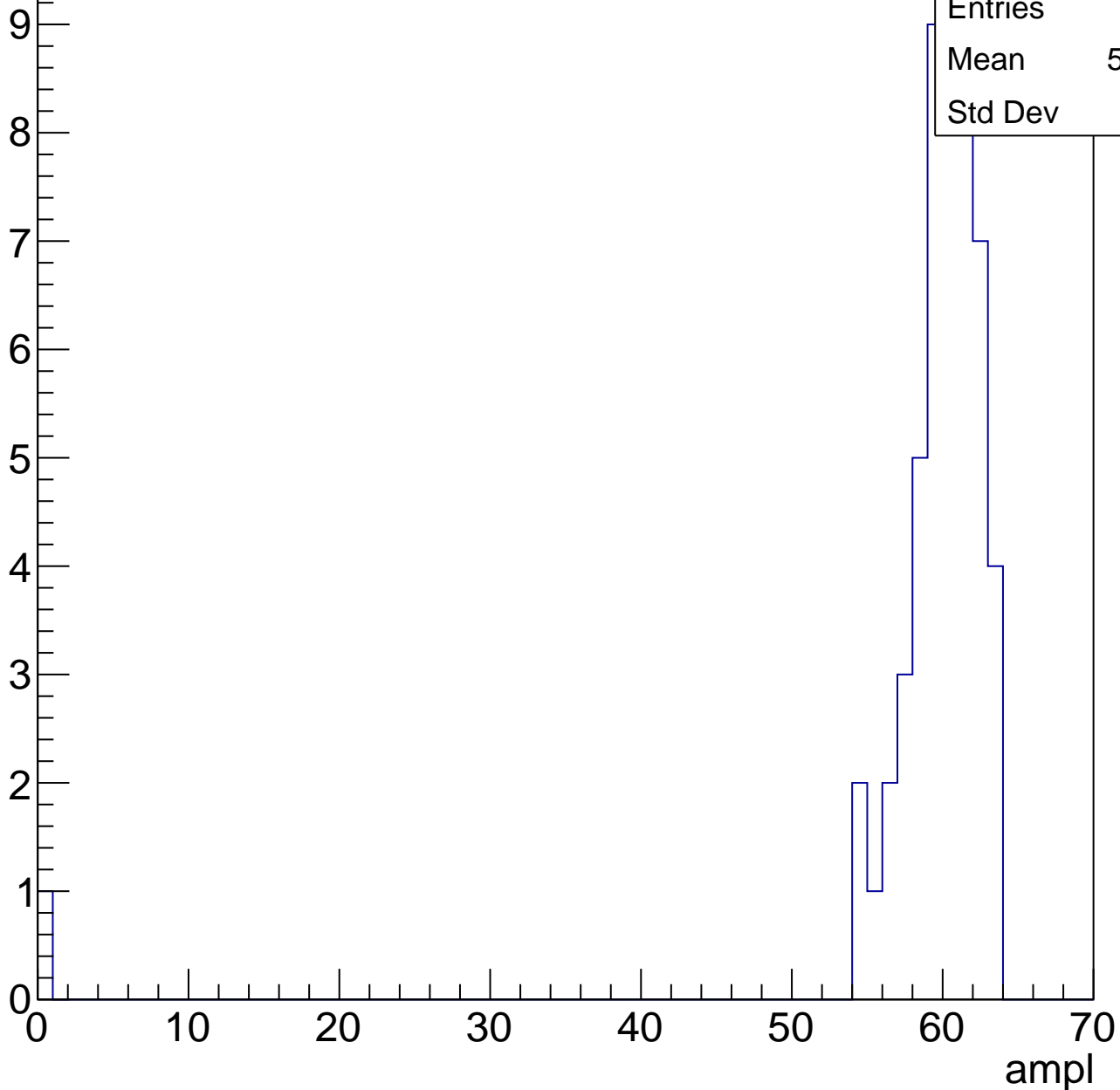


# B1L102S, U20-ch31, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	58.42
Std Dev	8.64

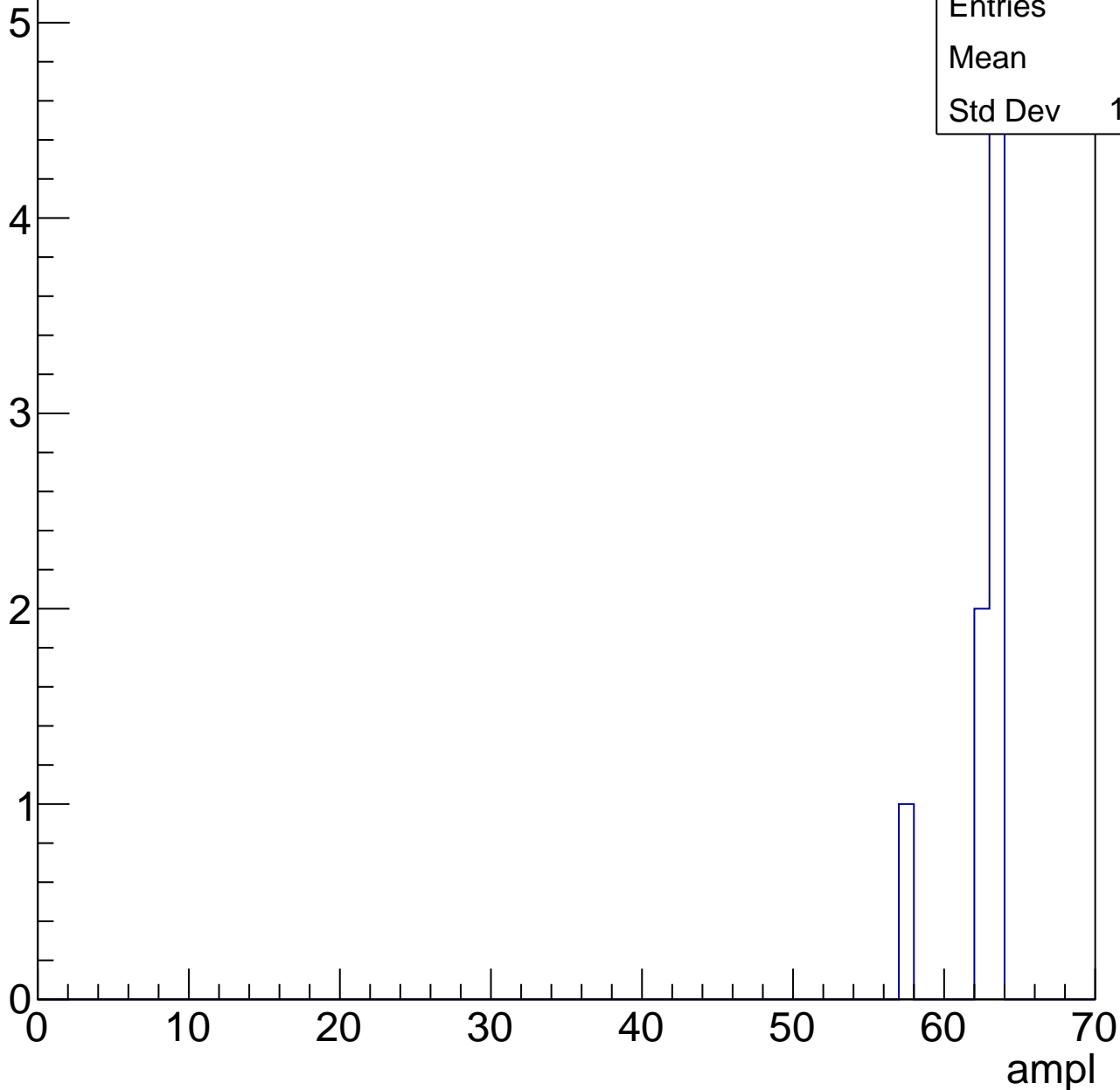


# B1L102S, U20-ch31, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	8
Mean	62
Std Dev	1.936





# B1L102S, U20-ch31, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U20-ch32, adc0

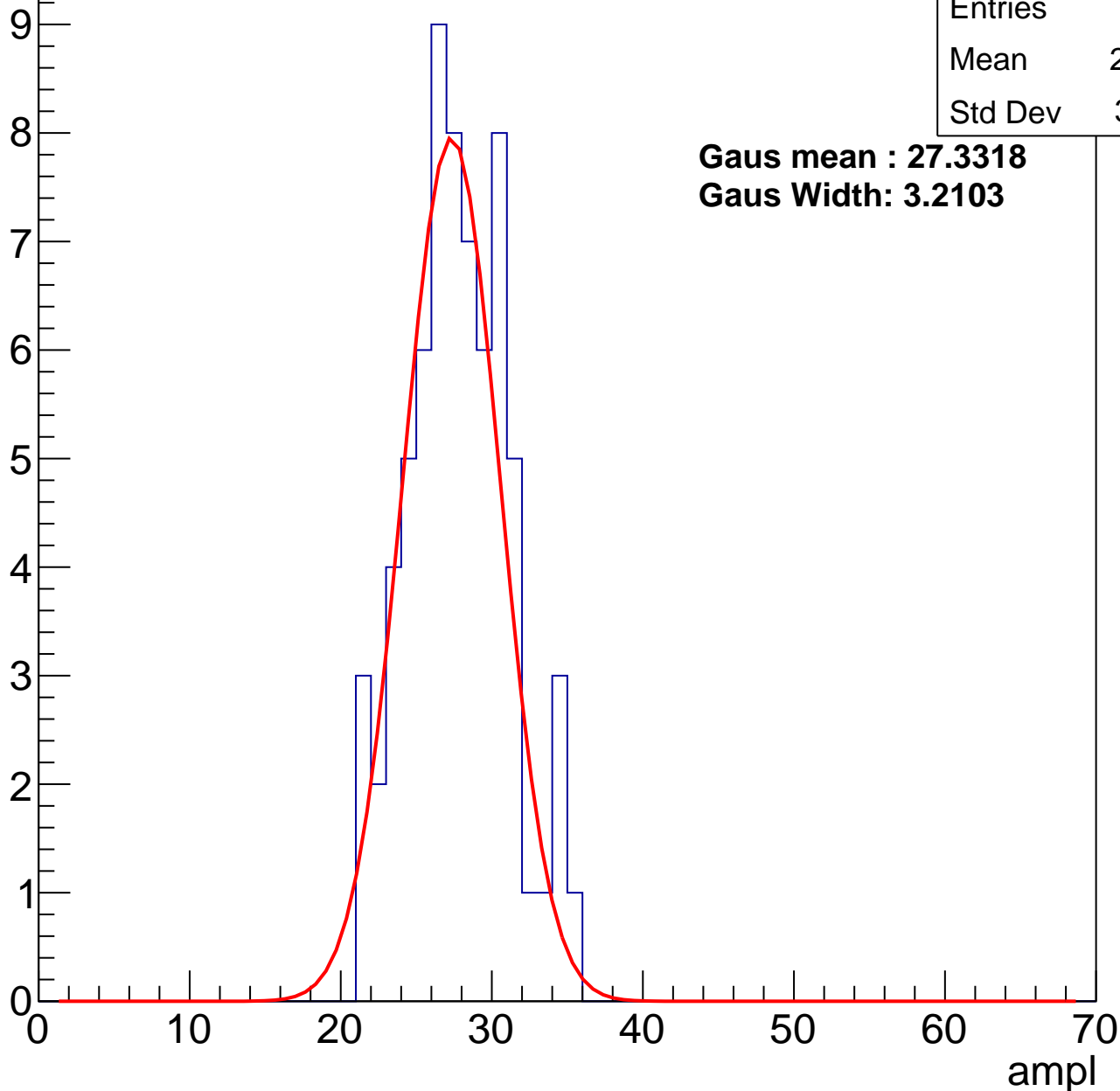
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	27.33
Std Dev	3.291

**Gaus mean : 27.3318**

**Gaus Width: 3.2103**



# B1L102S, U20-ch32, adc1

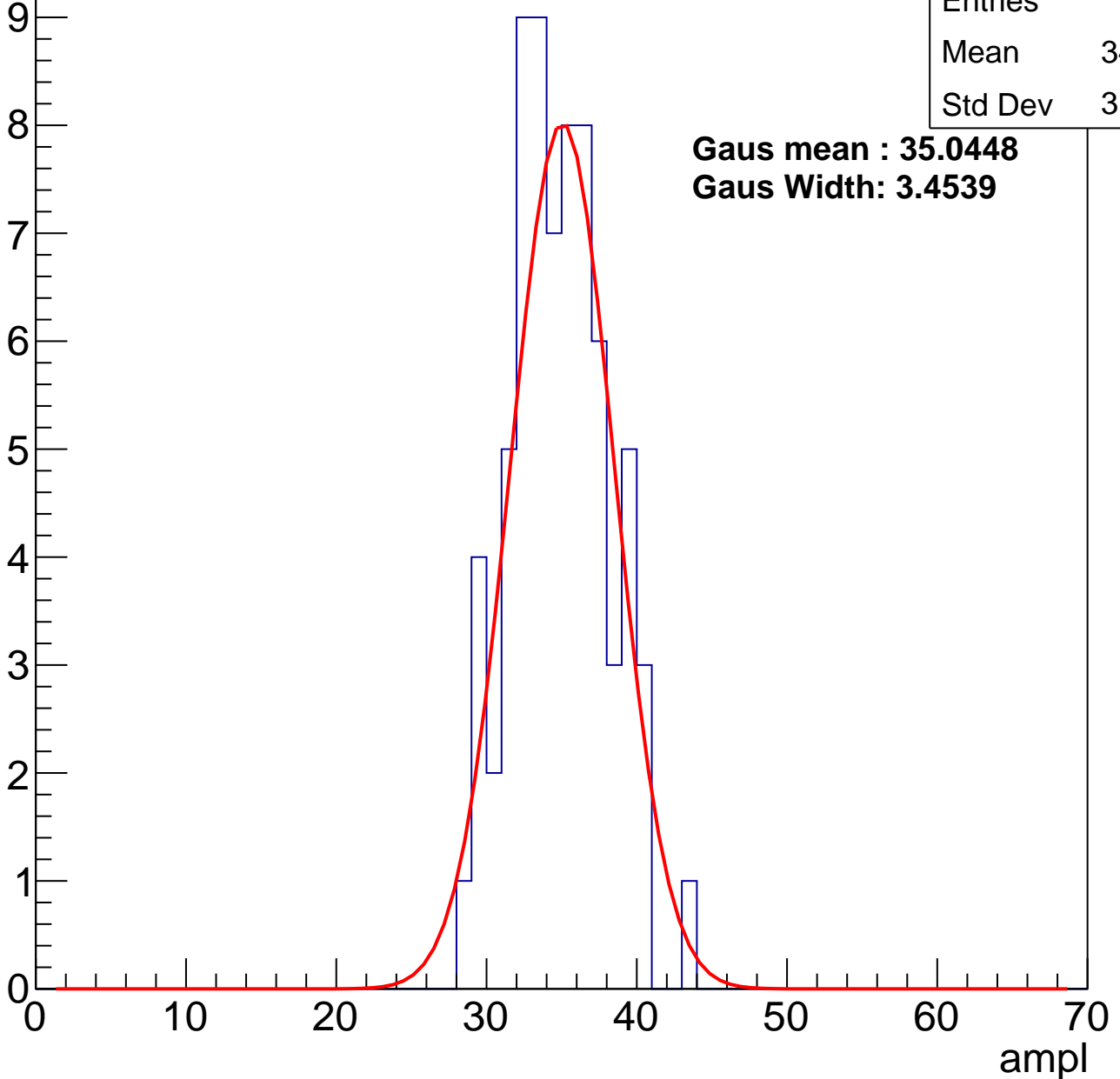
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	34.42
Std Dev	3.143

**Gaus mean : 35.0448**

**Gaus Width: 3.4539**



# B1L102S, U20-ch32, adc2

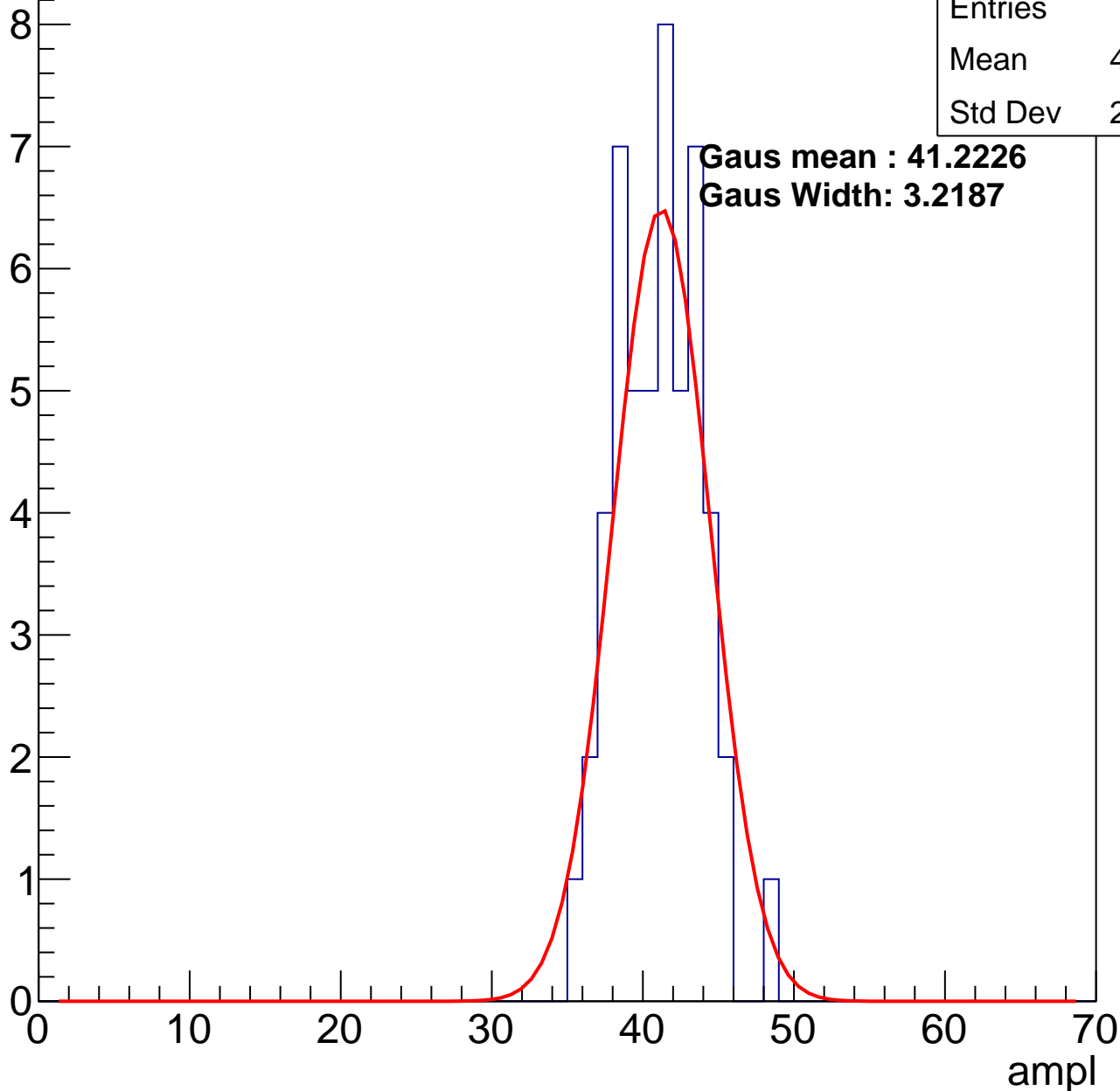
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	40.57
Std Dev	2.724

**Gaus mean : 41.2226**

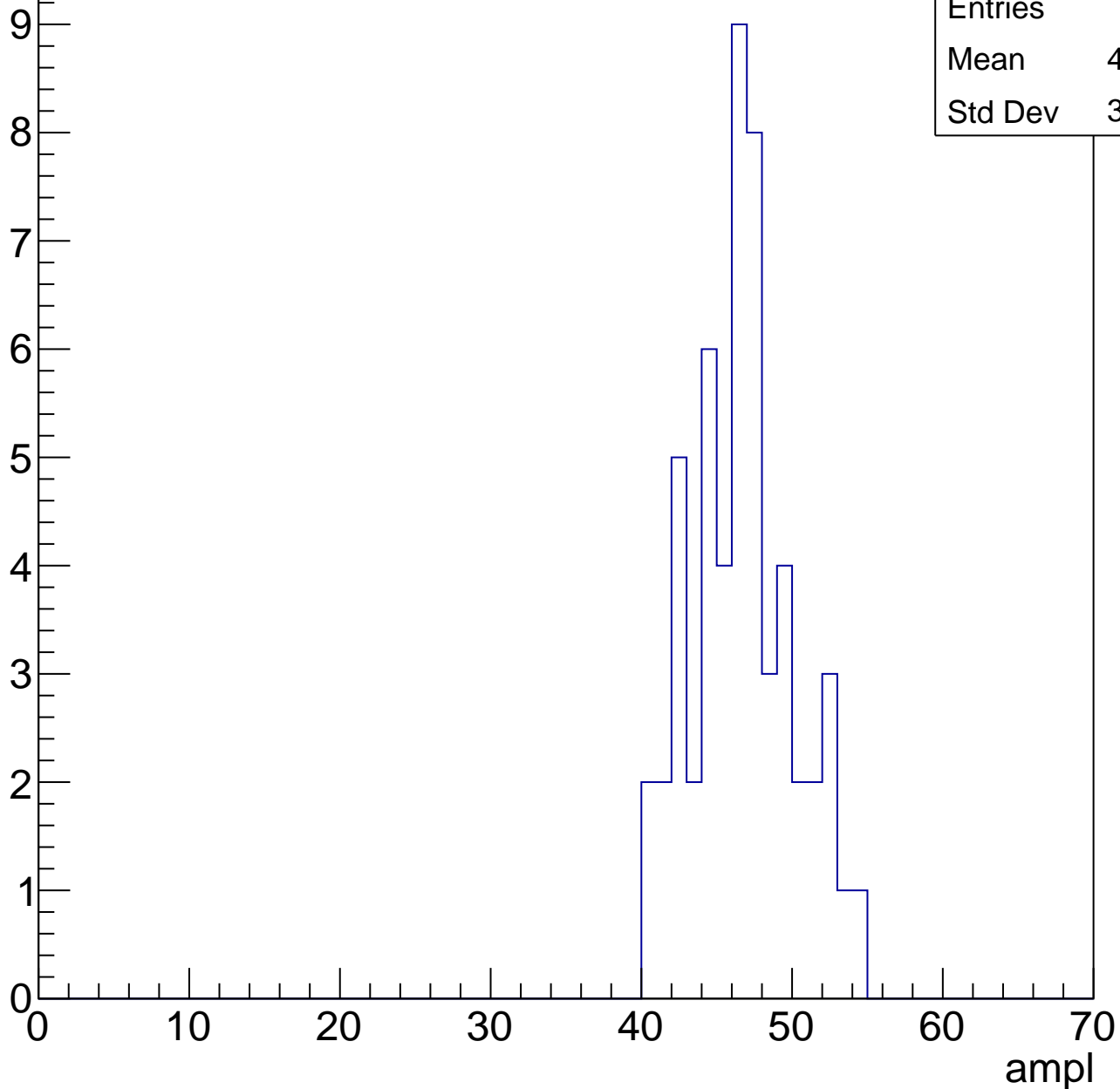
**Gaus Width: 3.2187**



# B1L102S, U20-ch32, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

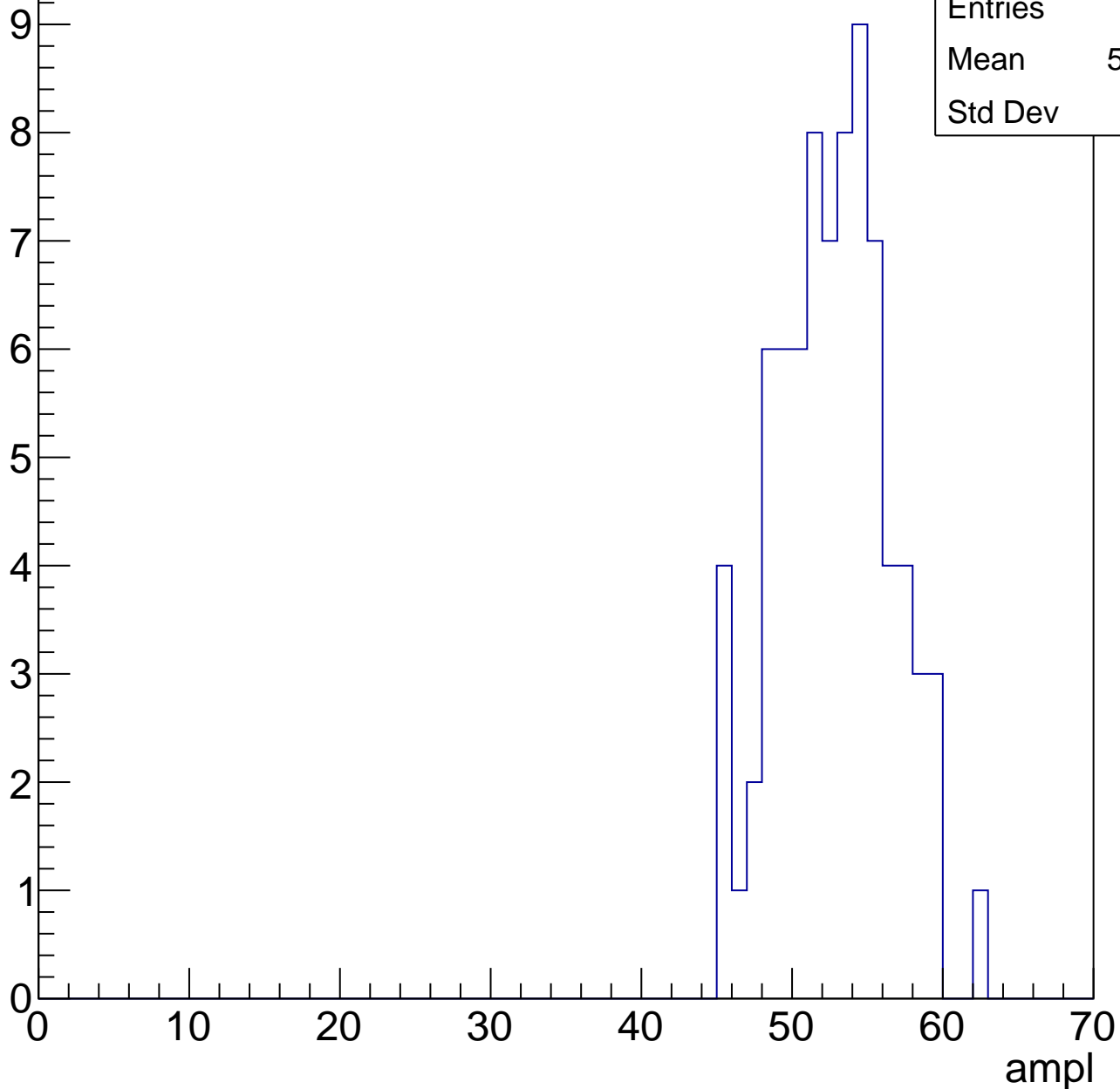
Entry



# B1L102S, U20-ch32, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

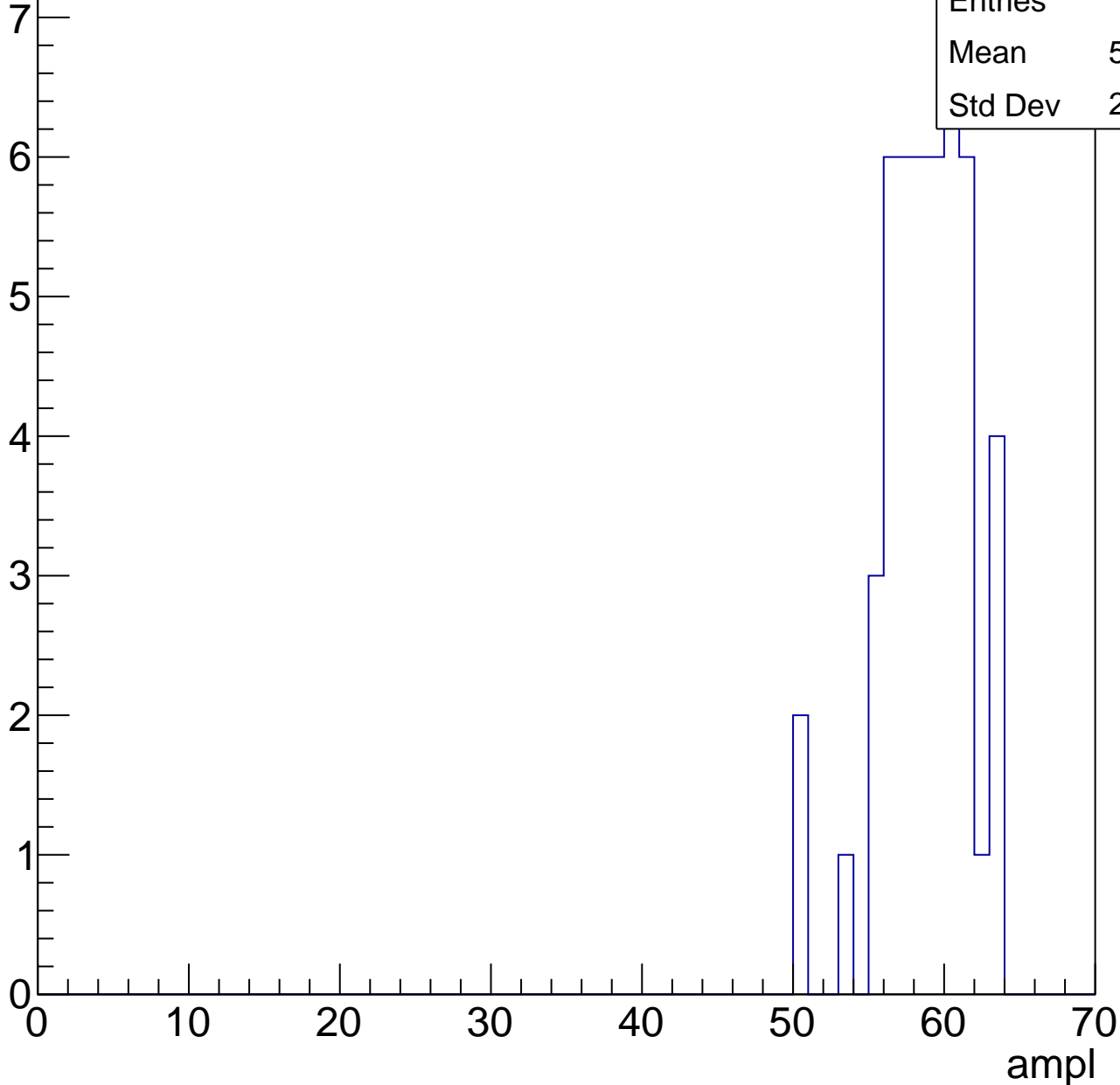


# B1L102S, U20-ch32, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	48
Mean	58.29
Std Dev	2.922

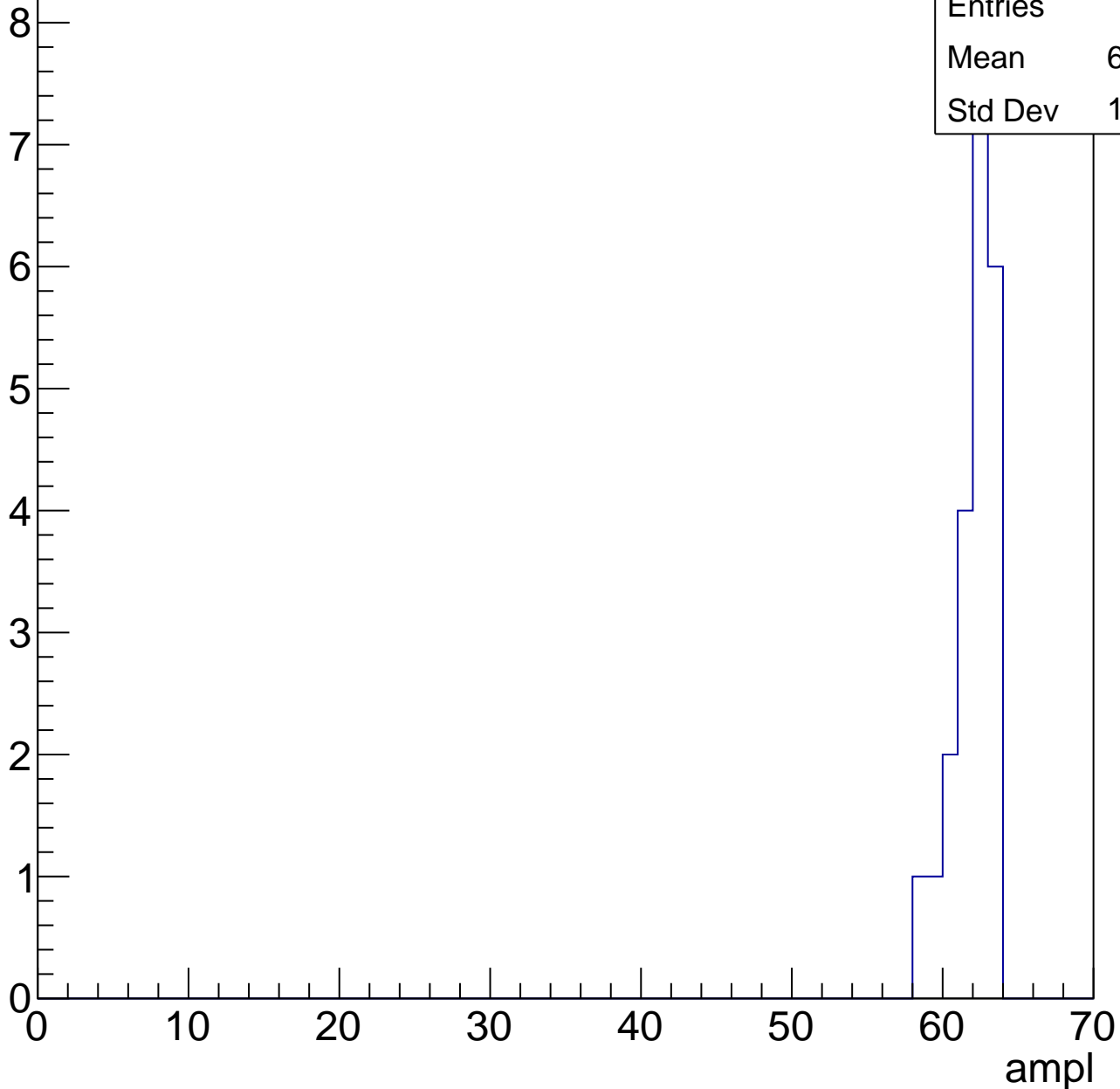


# B1L102S, U20-ch32, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	22
Mean	61.59
Std Dev	1.337

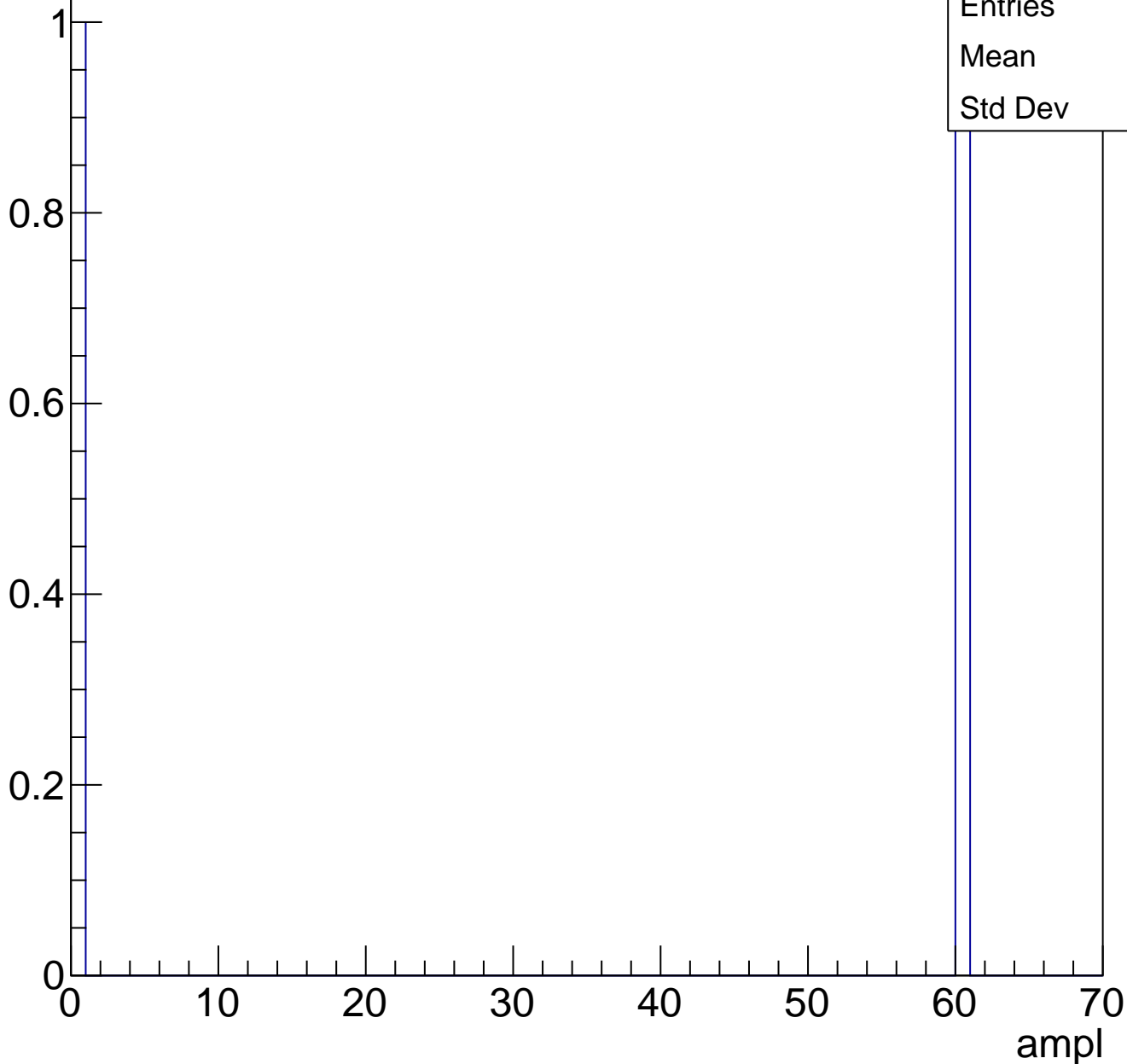




# B1L102S, U20-ch32, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch33, adc0

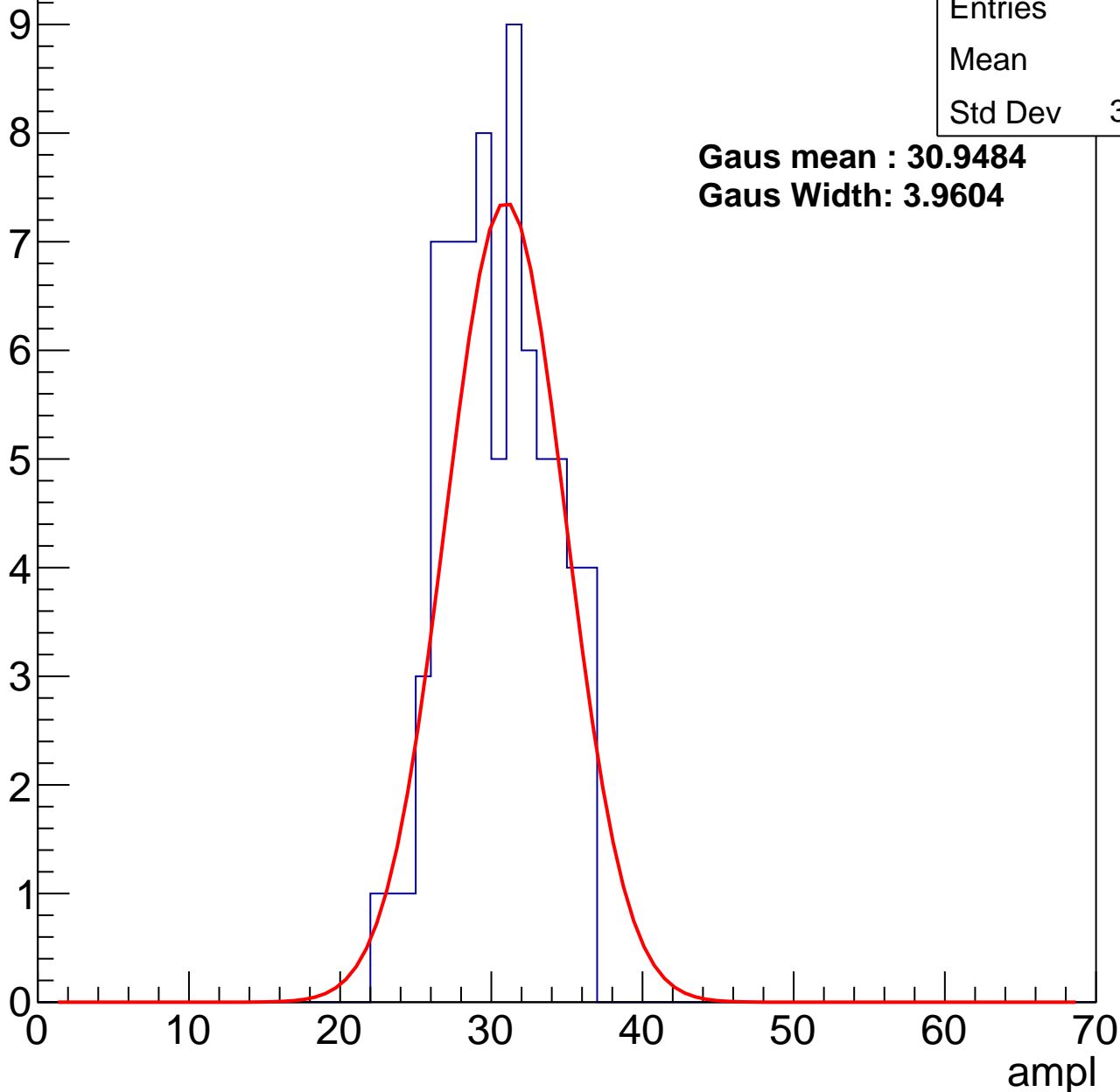
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	29.9
Std Dev	3.385

**Gaus mean : 30.9484**

**Gaus Width: 3.9604**



# B1L102S, U20-ch33, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	63
Mean	36.51
Std Dev	3.385

**Gaus mean : 37.0910**

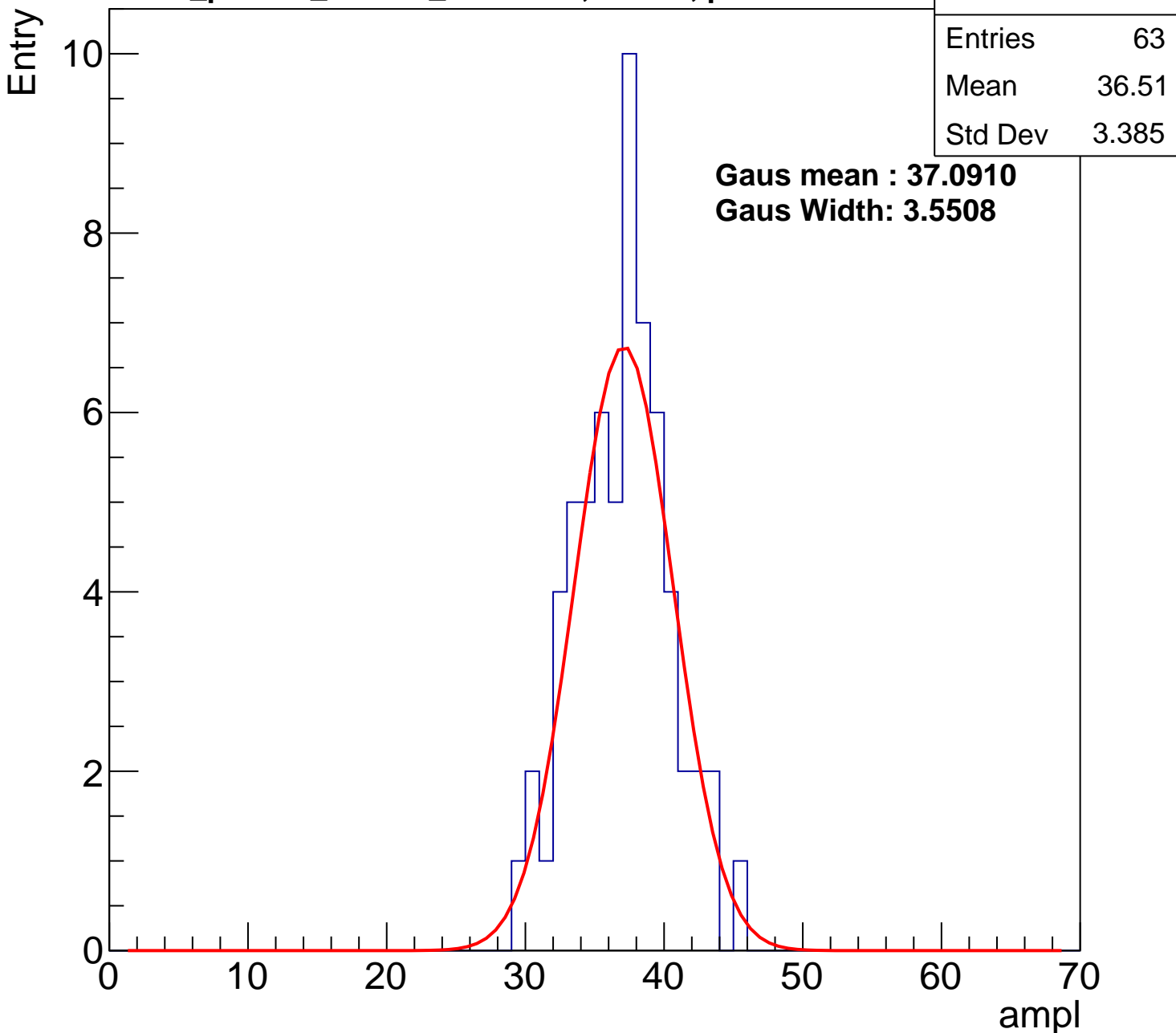
**Gaus Width: 3.5508**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U20-ch33, adc2

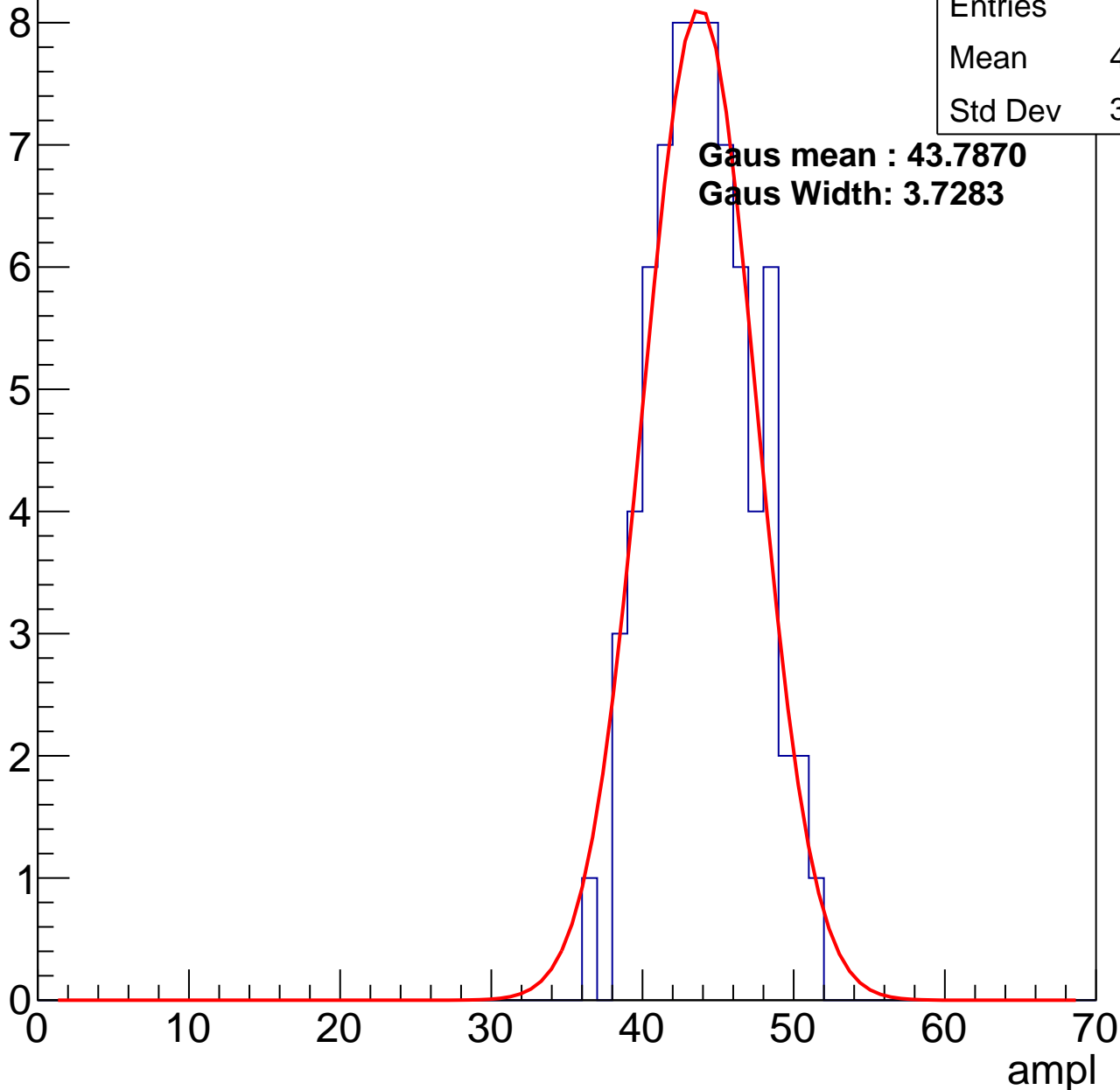
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	43.58
Std Dev	3.293

**Gaus mean : 43.7870**

**Gaus Width: 3.7283**

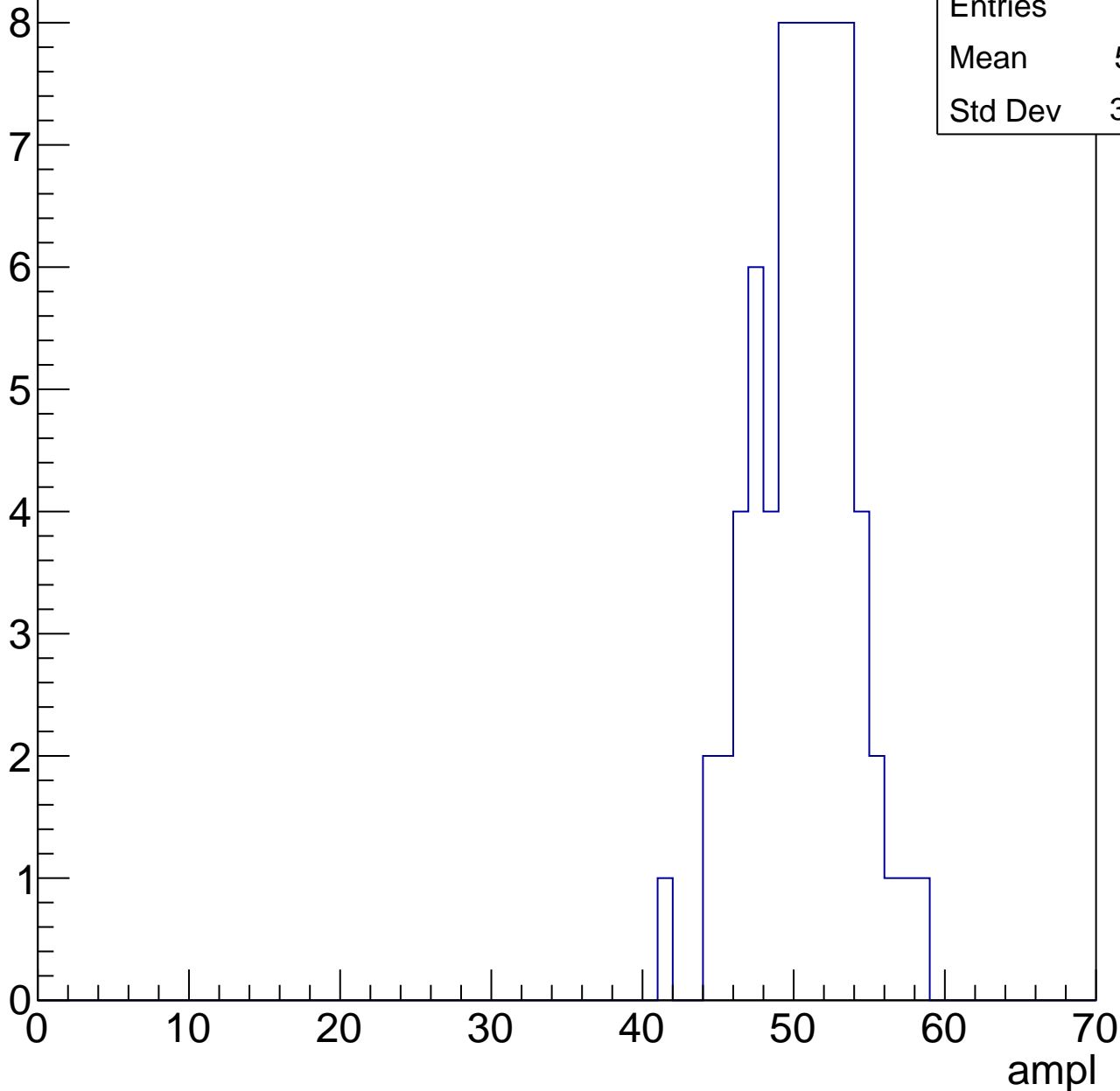


# B1L102S, U20-ch33, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	50.21
Std Dev	3.247

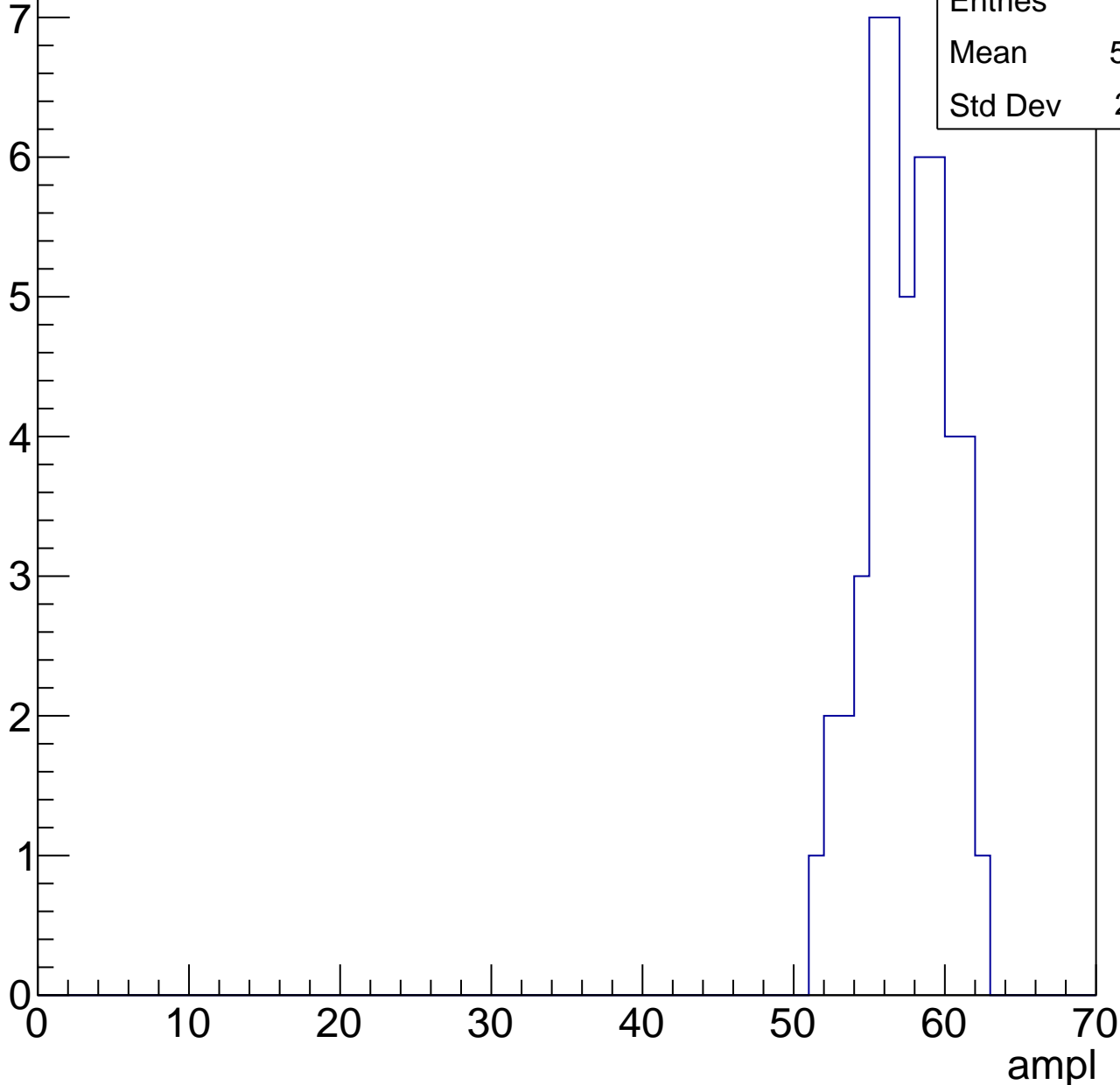


# B1L102S, U20-ch33, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	48
Mean	56.94
Std Dev	2.641

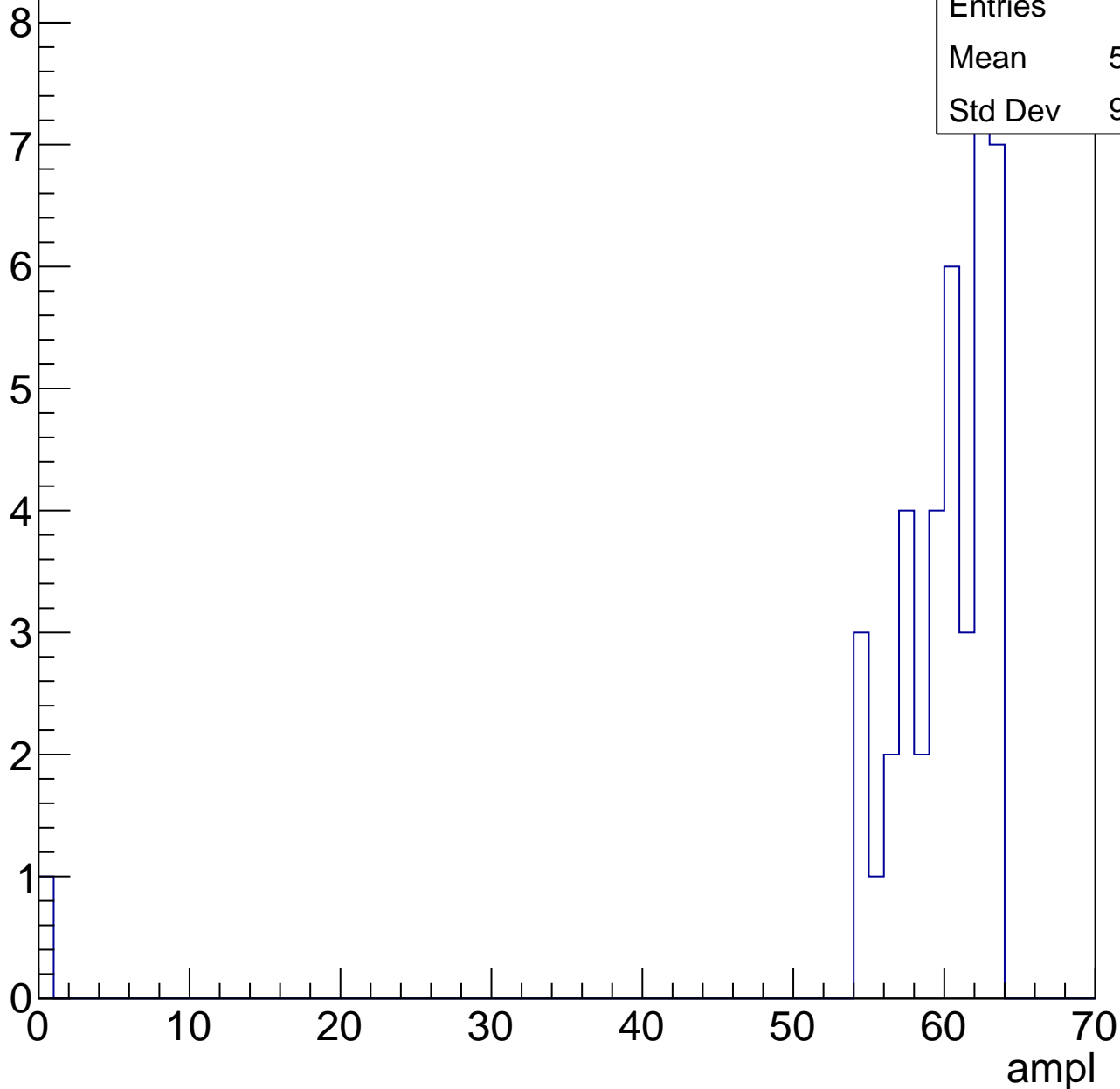


# B1L102S, U20-ch33, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

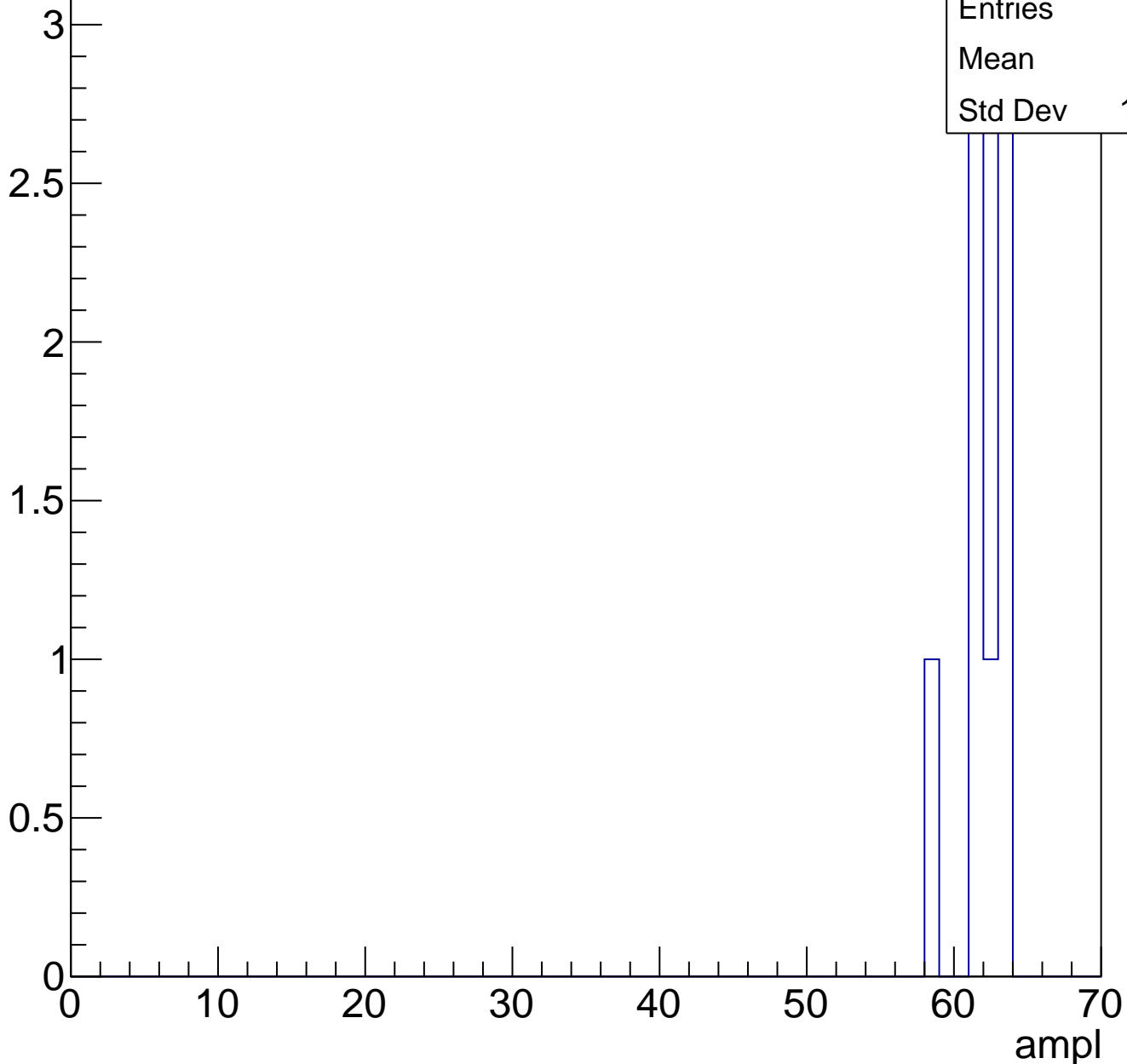
Entries	41
Mean	58.27
Std Dev	9.612



# B1L102S, U20-ch33, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U20-ch33, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L102S, U20-ch34, adc0

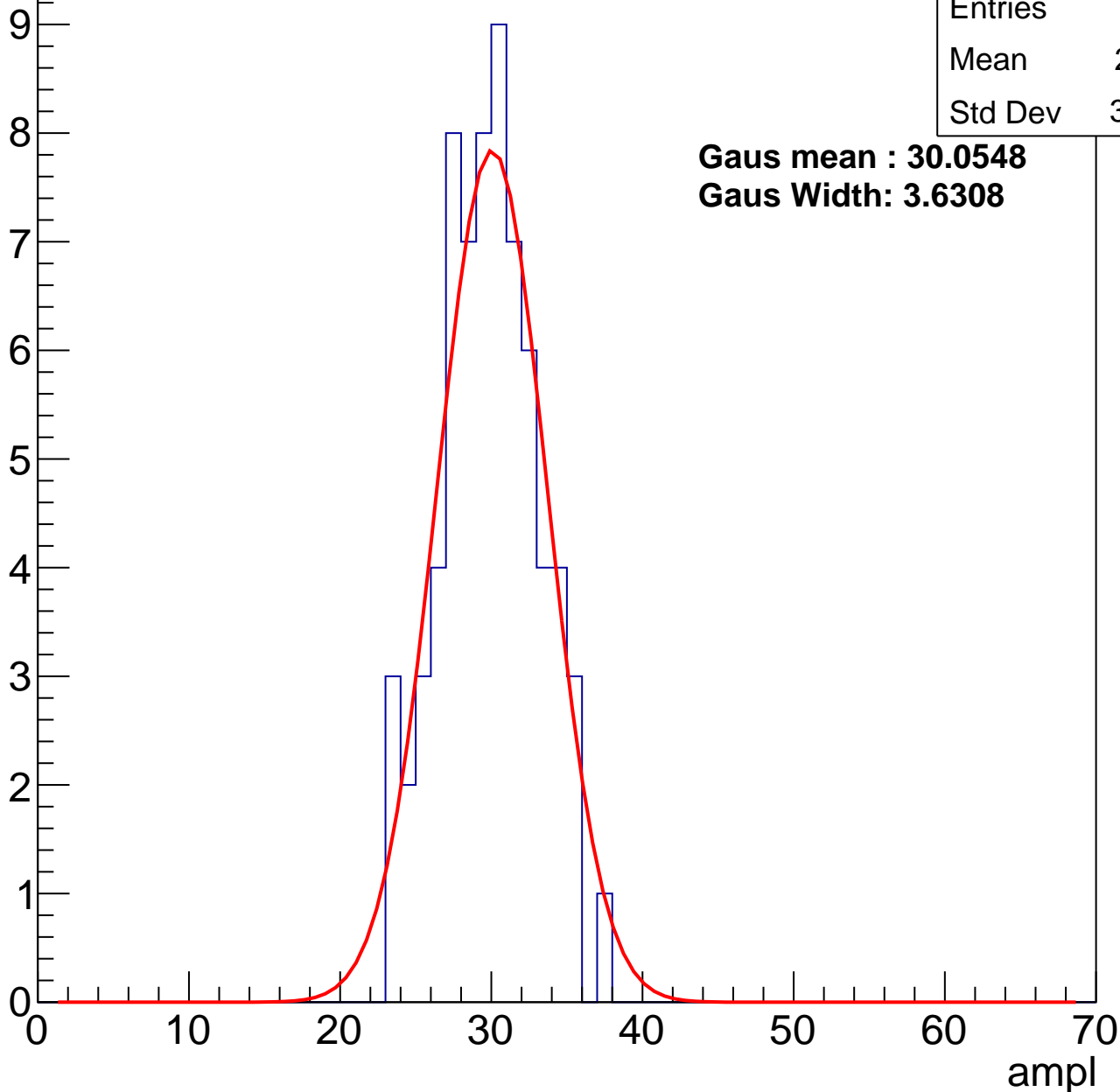
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	29.41
Std Dev	3.177

**Gaus mean : 30.0548**

**Gaus Width: 3.6308**



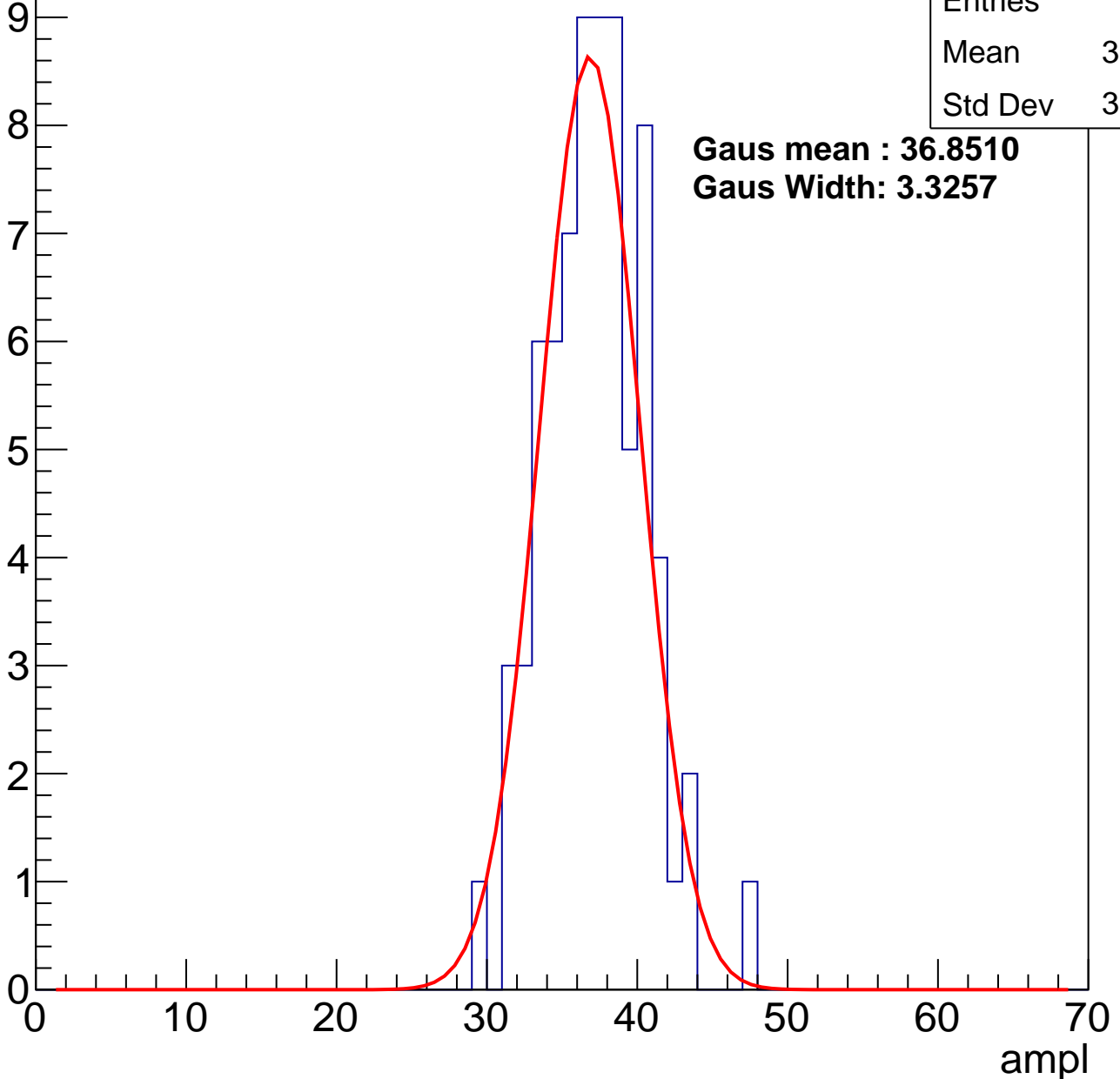
# B1L102S, U20-ch34, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	36.73
Std Dev	3.269

**Gaus mean : 36.8510**  
**Gaus Width: 3.3257**



# B1L102S, U20-ch34, adc2

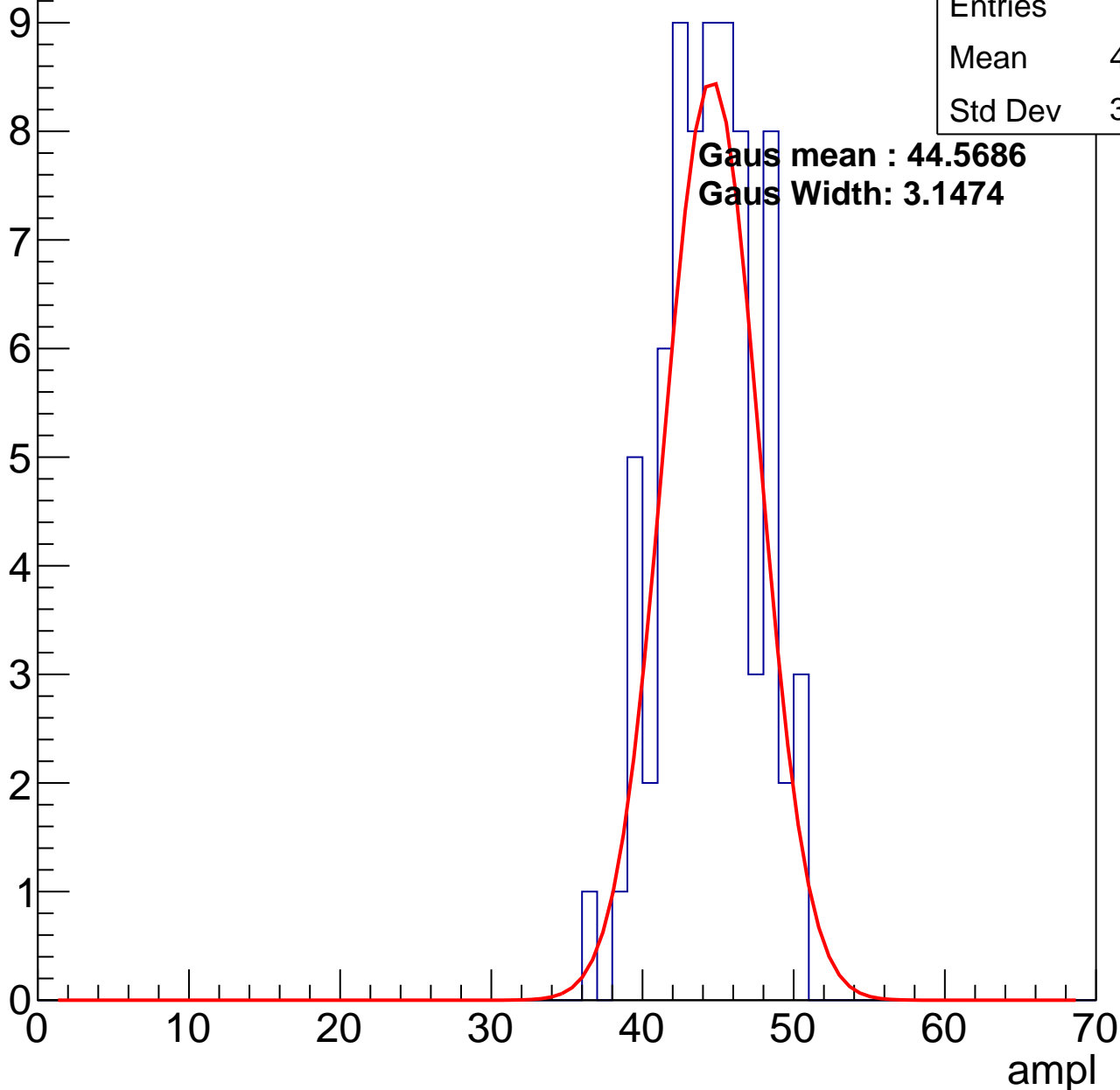
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	44.04
Std Dev	3.095

**Gaus mean : 44.5686**

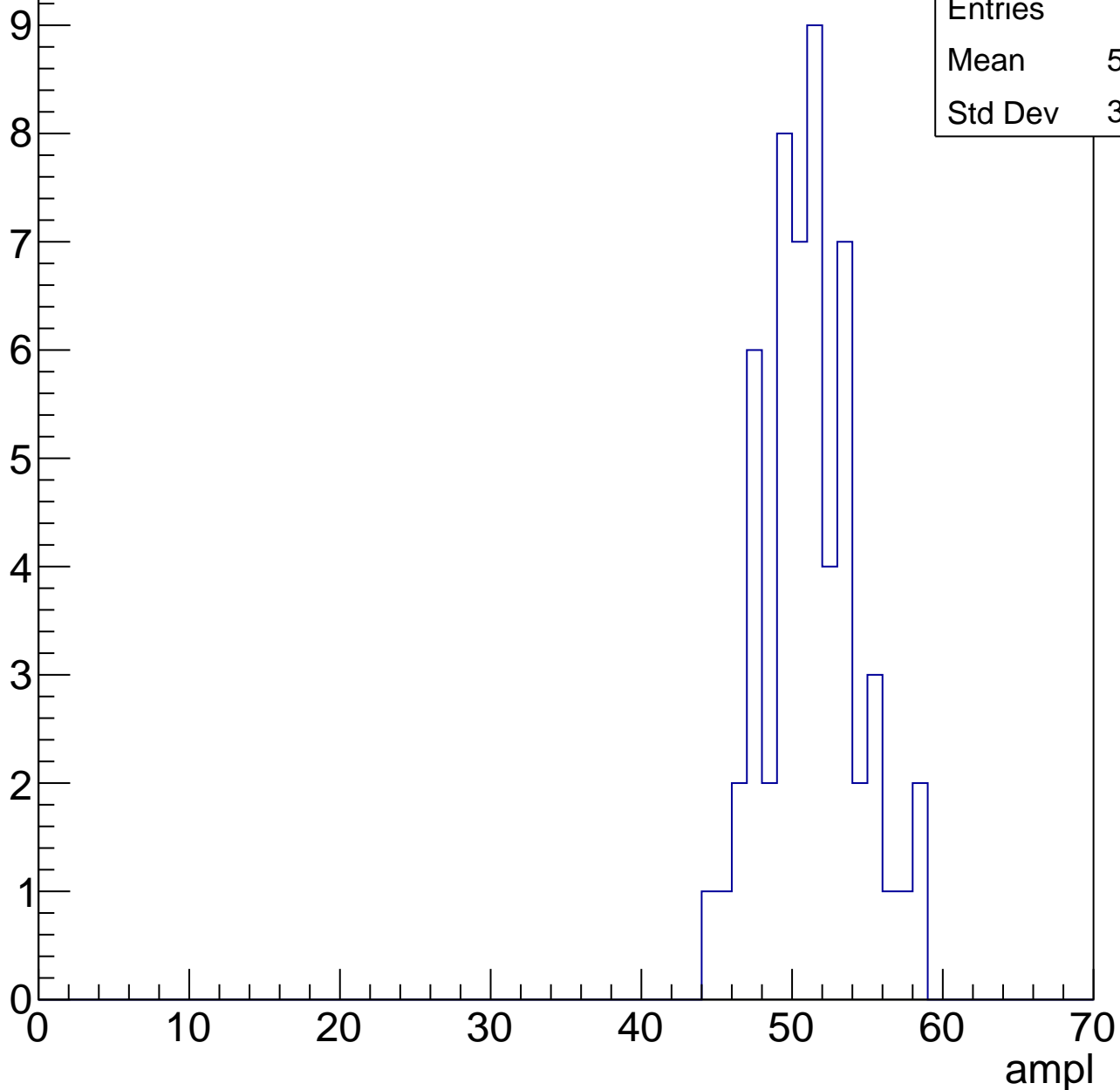
**Gaus Width: 3.1474**



# B1L102S, U20-ch34, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

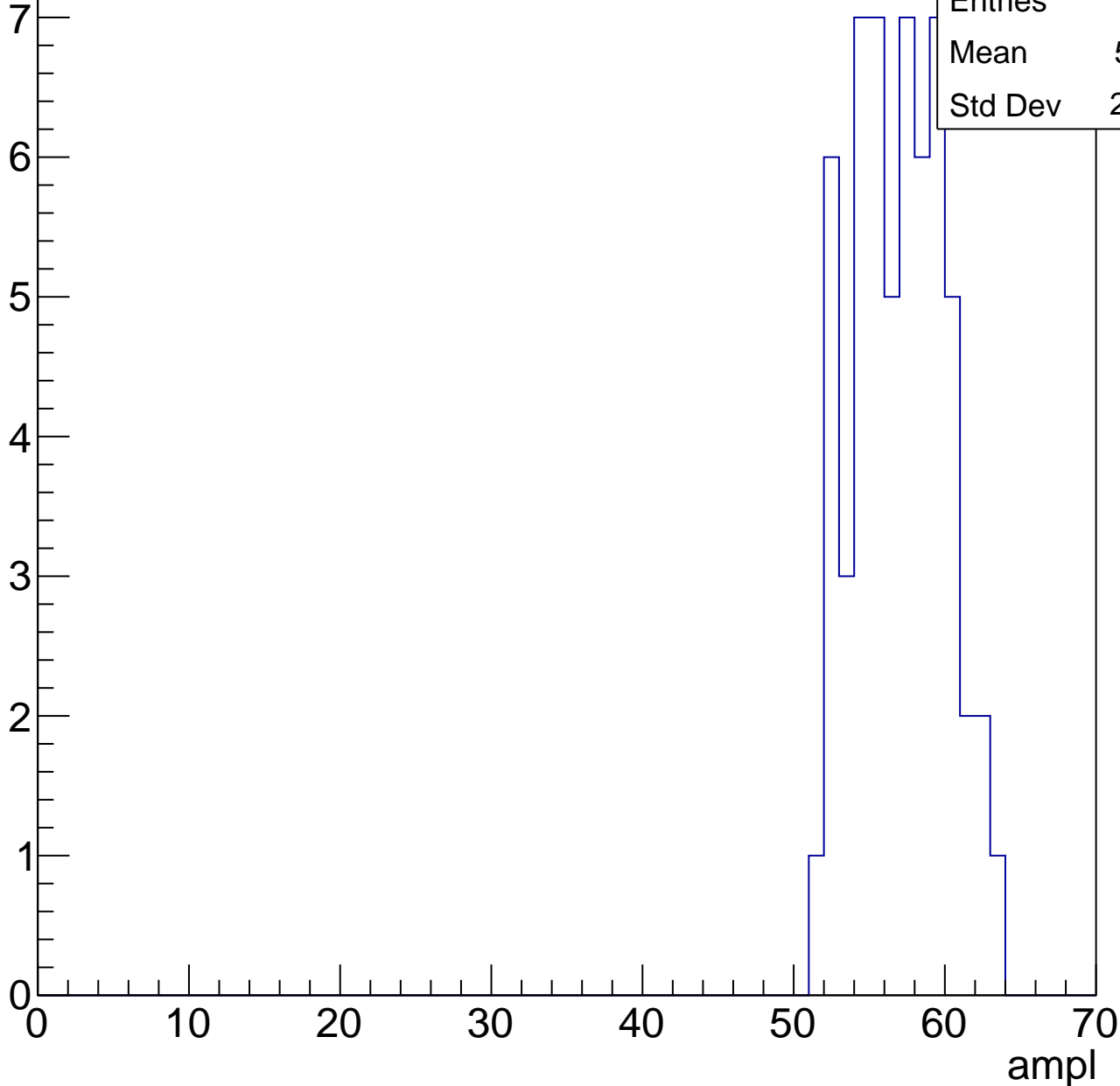


# B1L102S, U20-ch34, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	56.51
Std Dev	2.948

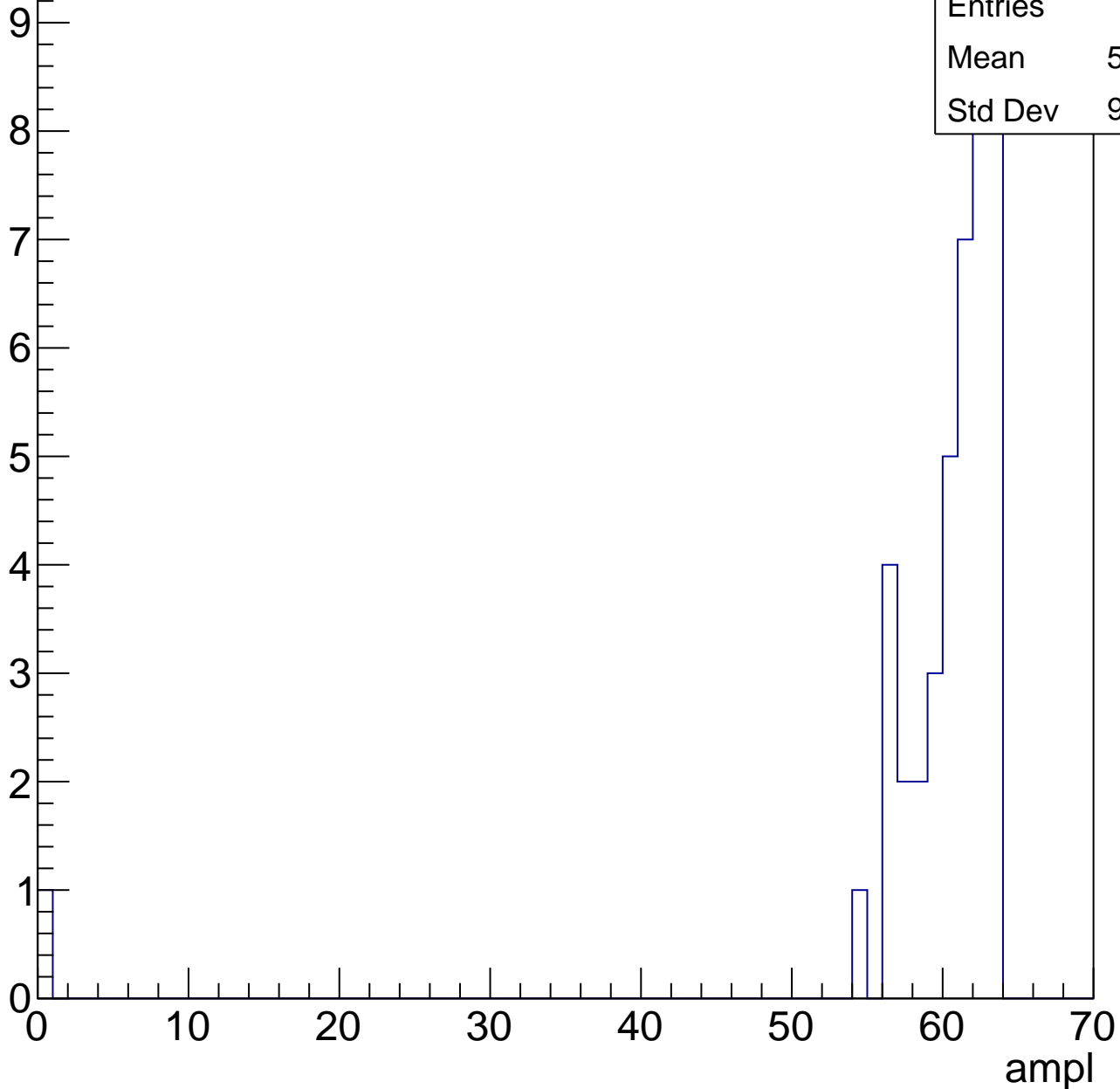


# B1L102S, U20-ch34, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	42
Mean	58.93
Std Dev	9.513



# B1L102S, U20-ch34, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U20-ch34, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U20-ch35, adc0

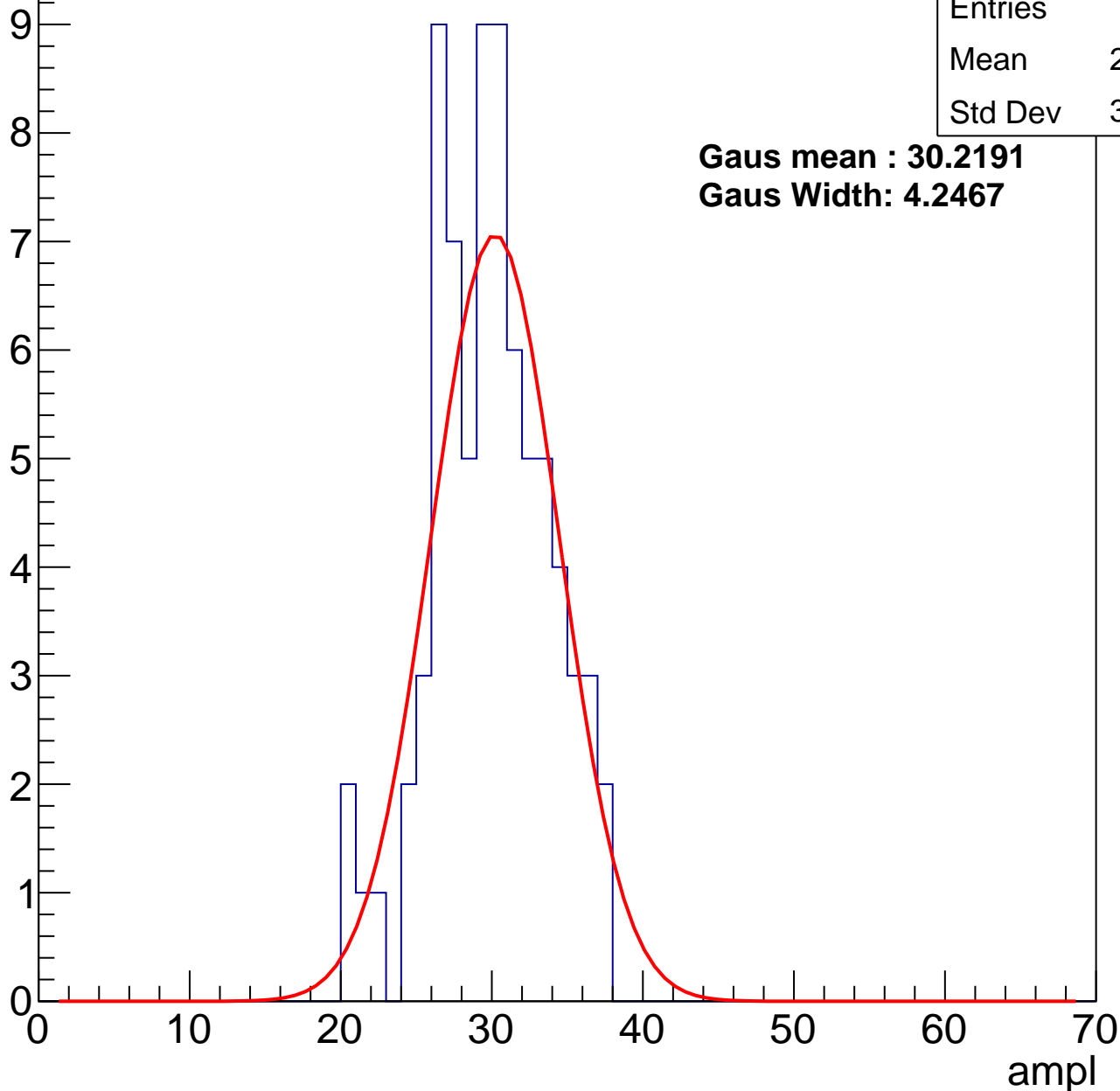
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	29.39
Std Dev	3.832

**Gaus mean : 30.2191**

**Gaus Width: 4.2467**



# B1L102S, U20-ch35, adc1

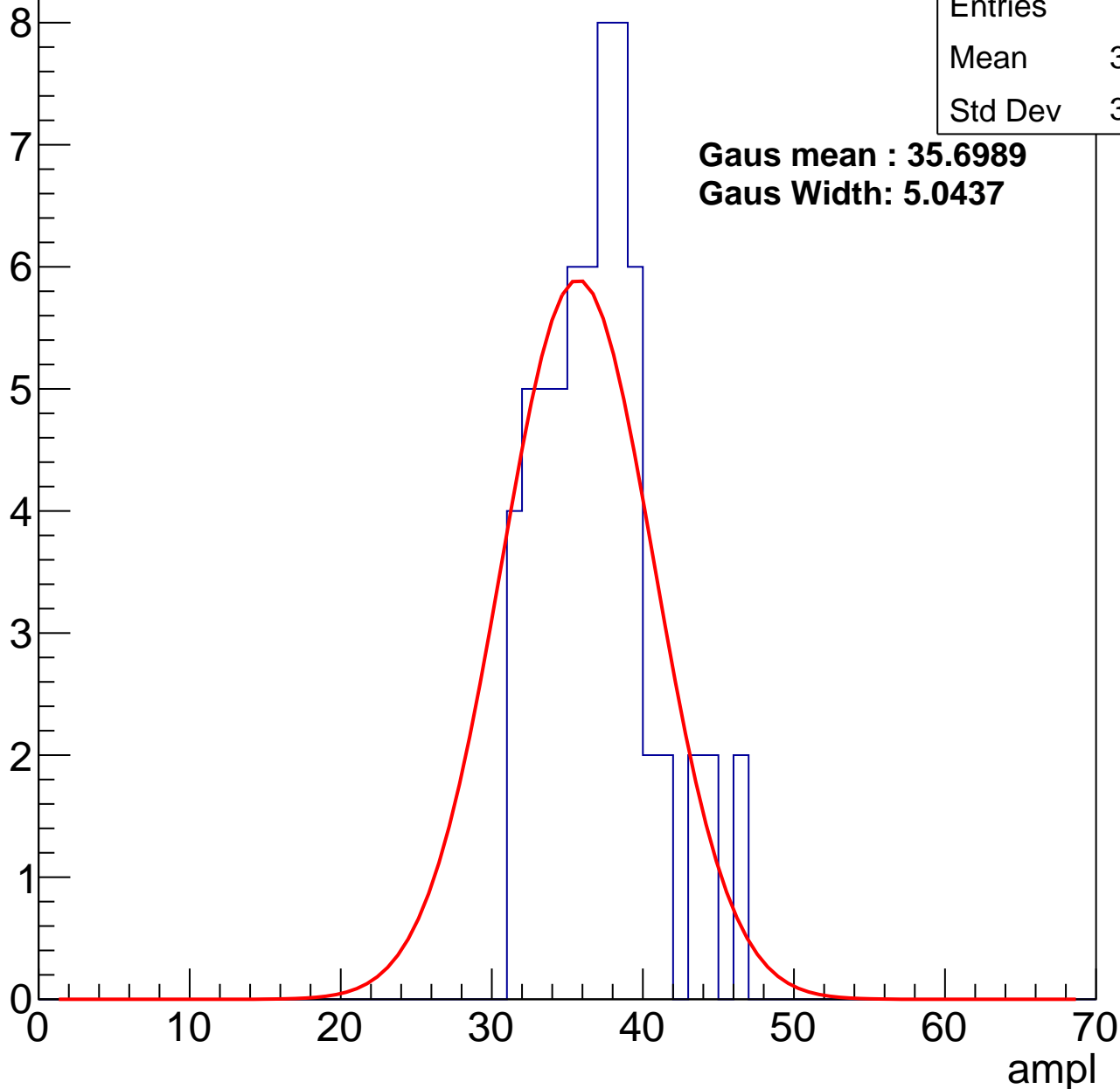
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	36.62
Std Dev	3.627

**Gaus mean : 35.6989**

**Gaus Width: 5.0437**



# B1L102S, U20-ch35, adc2

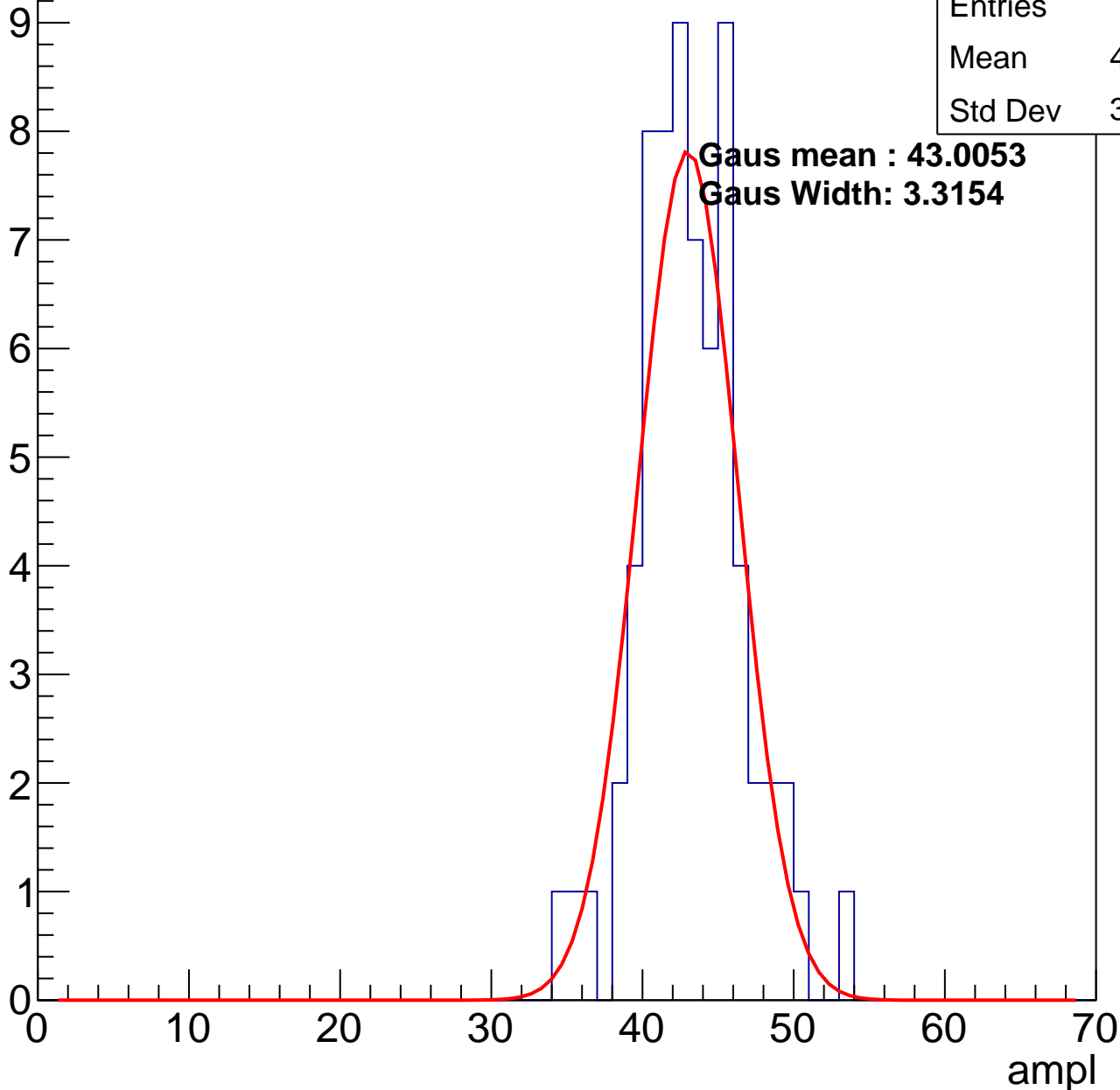
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	42.76
Std Dev	3.426

**Gaus mean : 43.0053**

**Gaus Width: 3.3154**

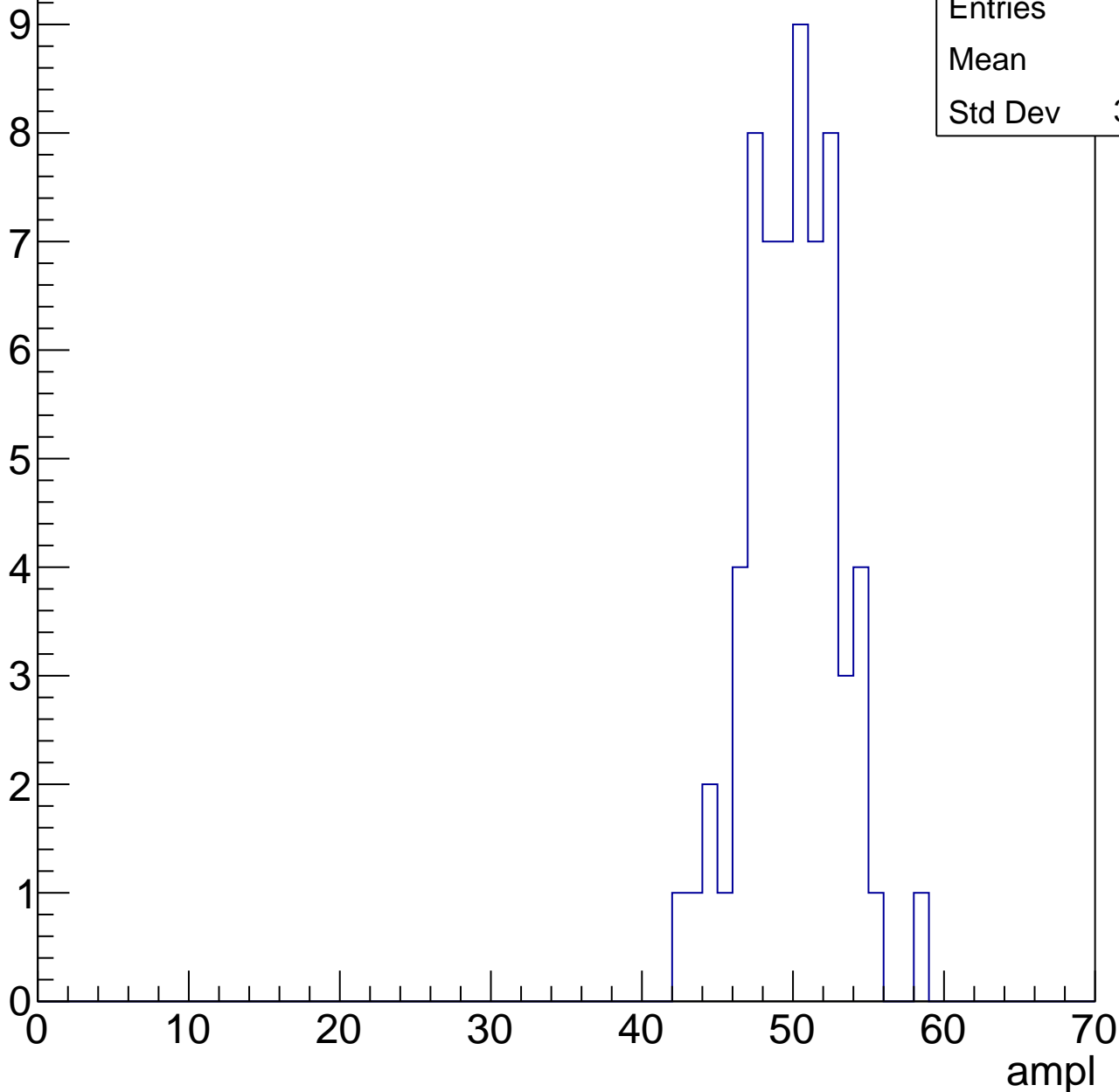


# B1L102S, U20-ch35, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	49.5
Std Dev	3.021

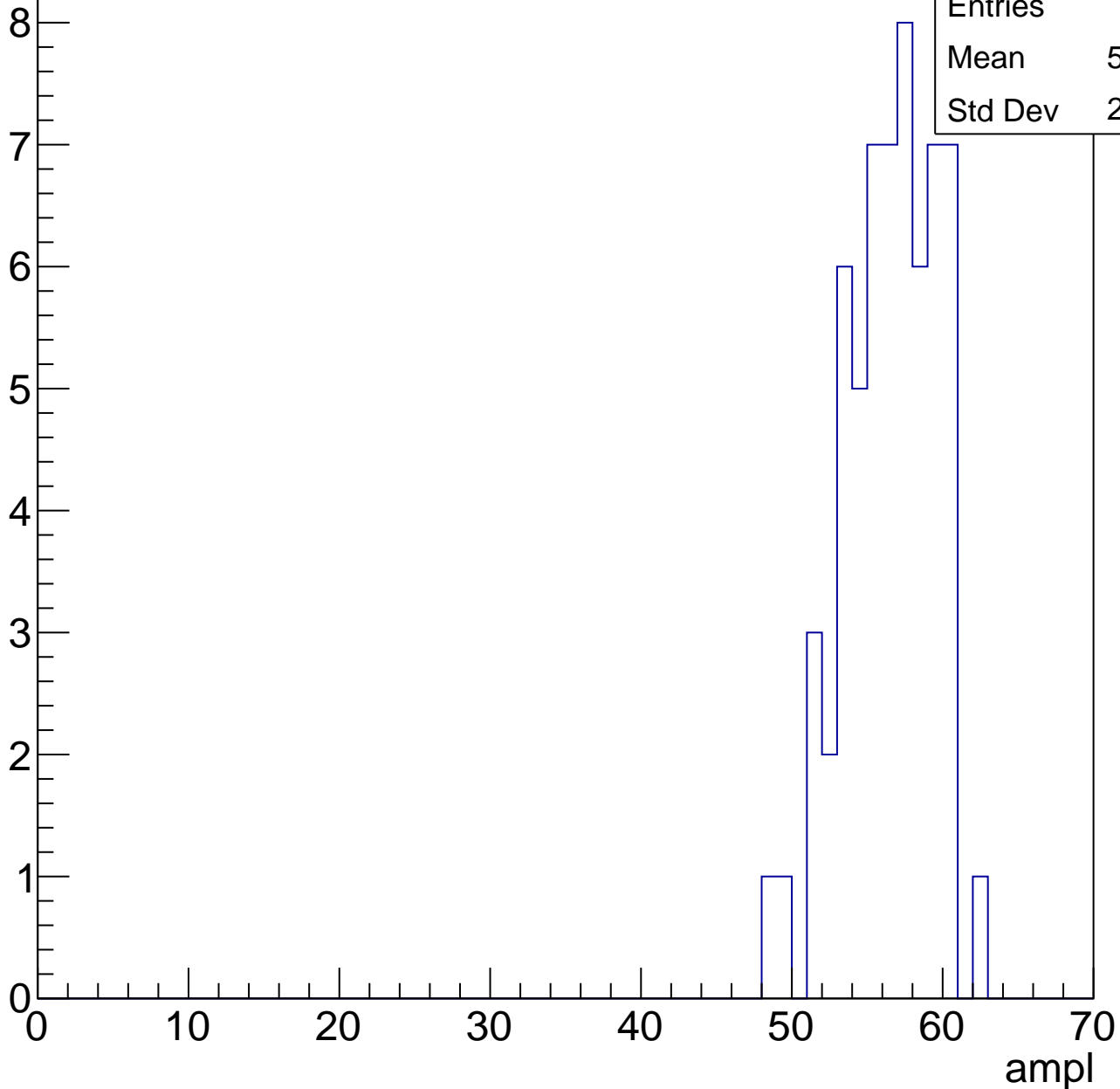


# B1L102S, U20-ch35, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	56.03
Std Dev	2.986

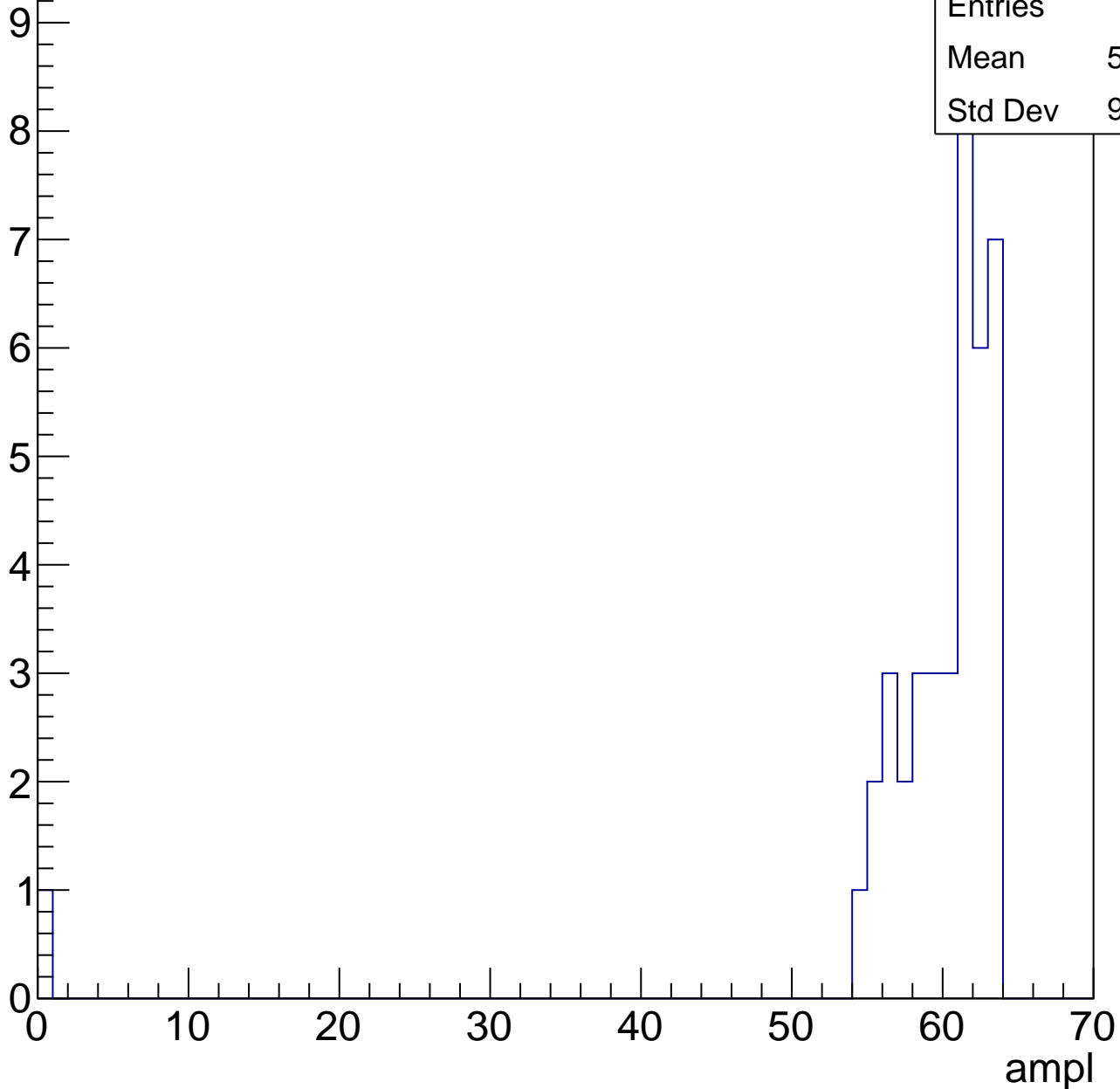


# B1L102S, U20-ch35, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	40
Mean	58.48
Std Dev	9.708



# B1L102S, U20-ch35, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U20-ch35, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch36, adc0

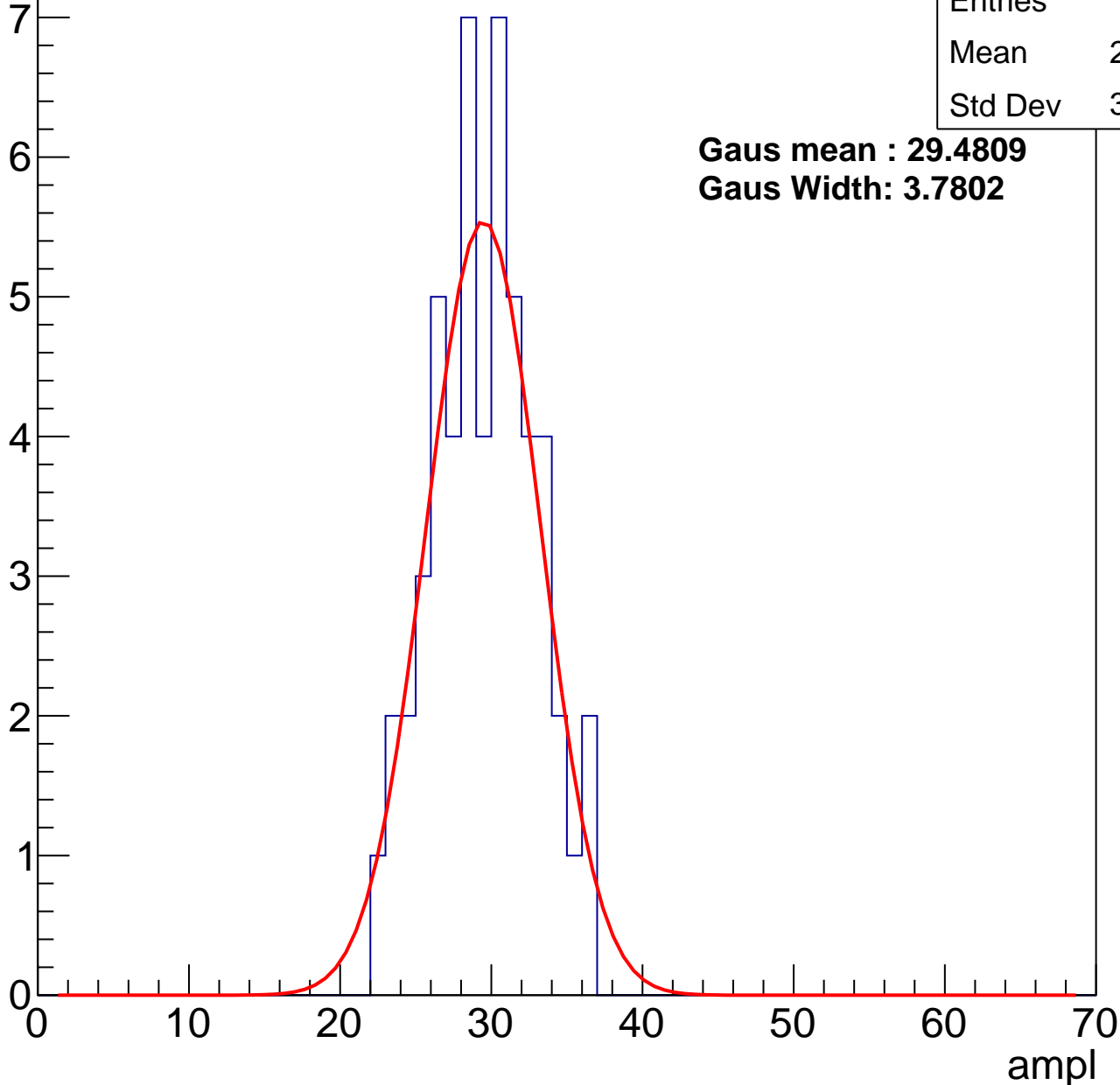
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	29.08
Std Dev	3.358

**Gaus mean : 29.4809**

**Gaus Width: 3.7802**



# B1L102S, U20-ch36, adc1

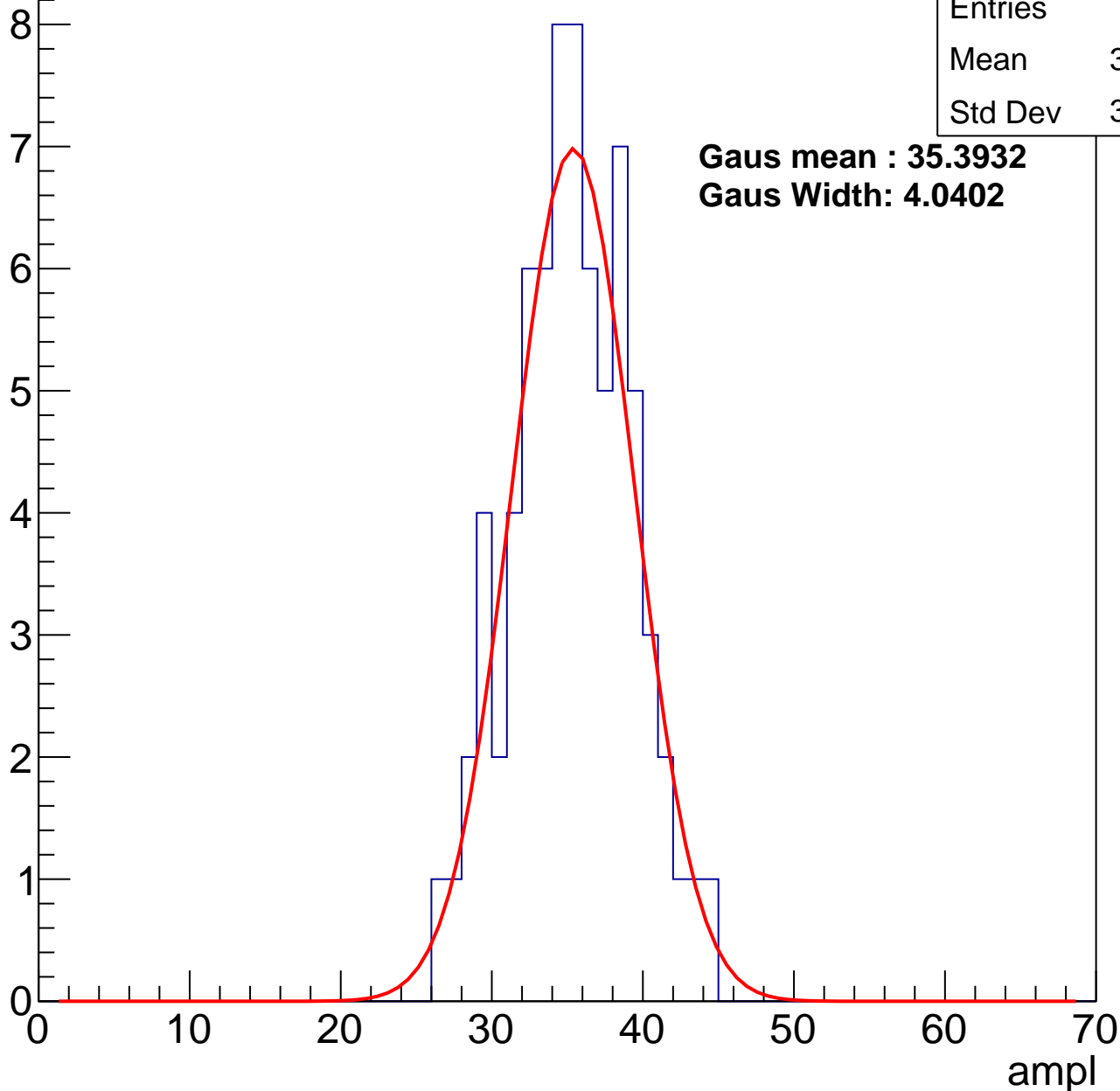
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	34.85
Std Dev	3.874

**Gaus mean : 35.3932**

**Gaus Width: 4.0402**



# B1L102S, U20-ch36, adc2

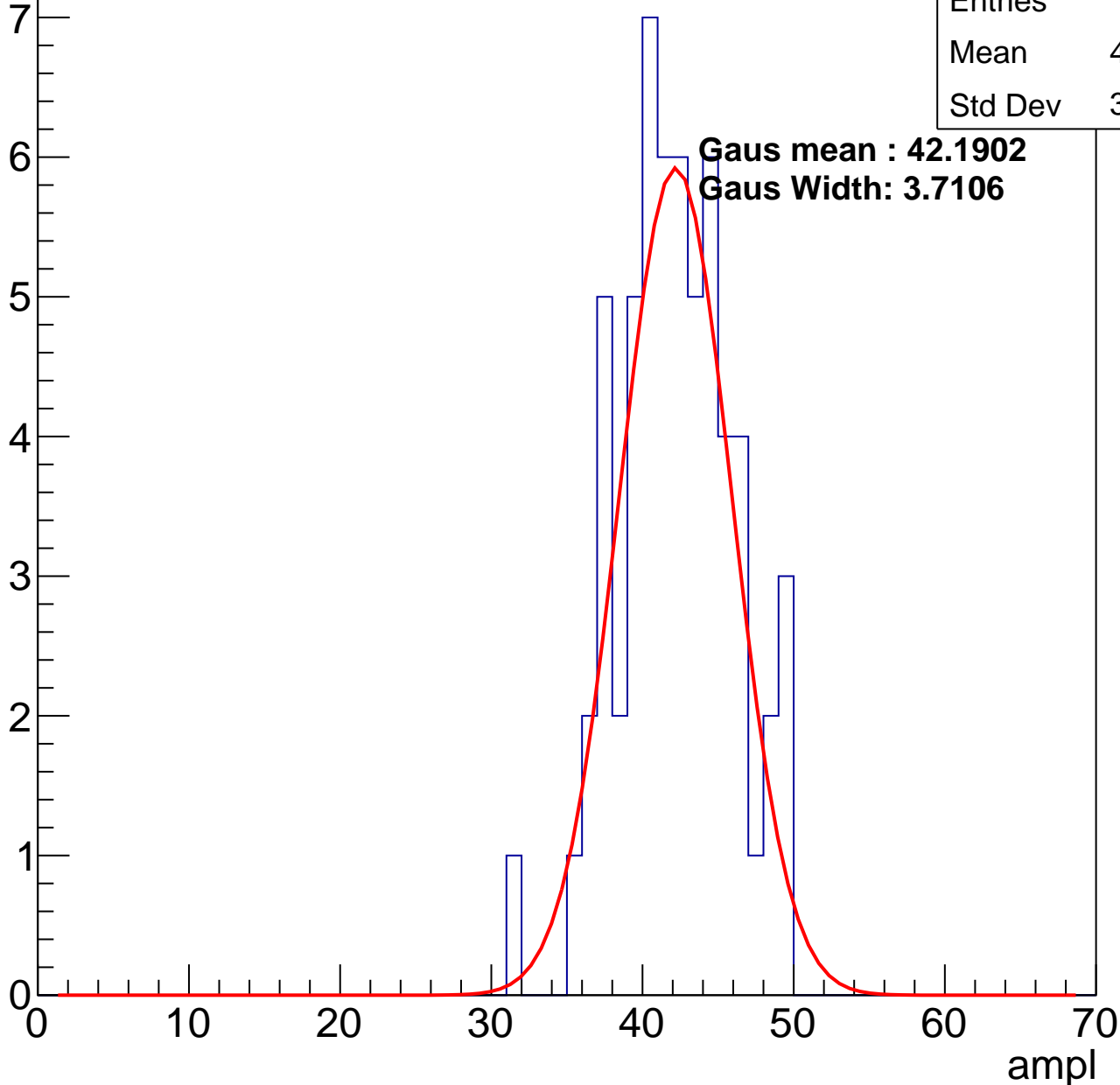
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	41.75
Std Dev	3.758

**Gaus mean : 42.1902**

**Gaus Width: 3.7106**

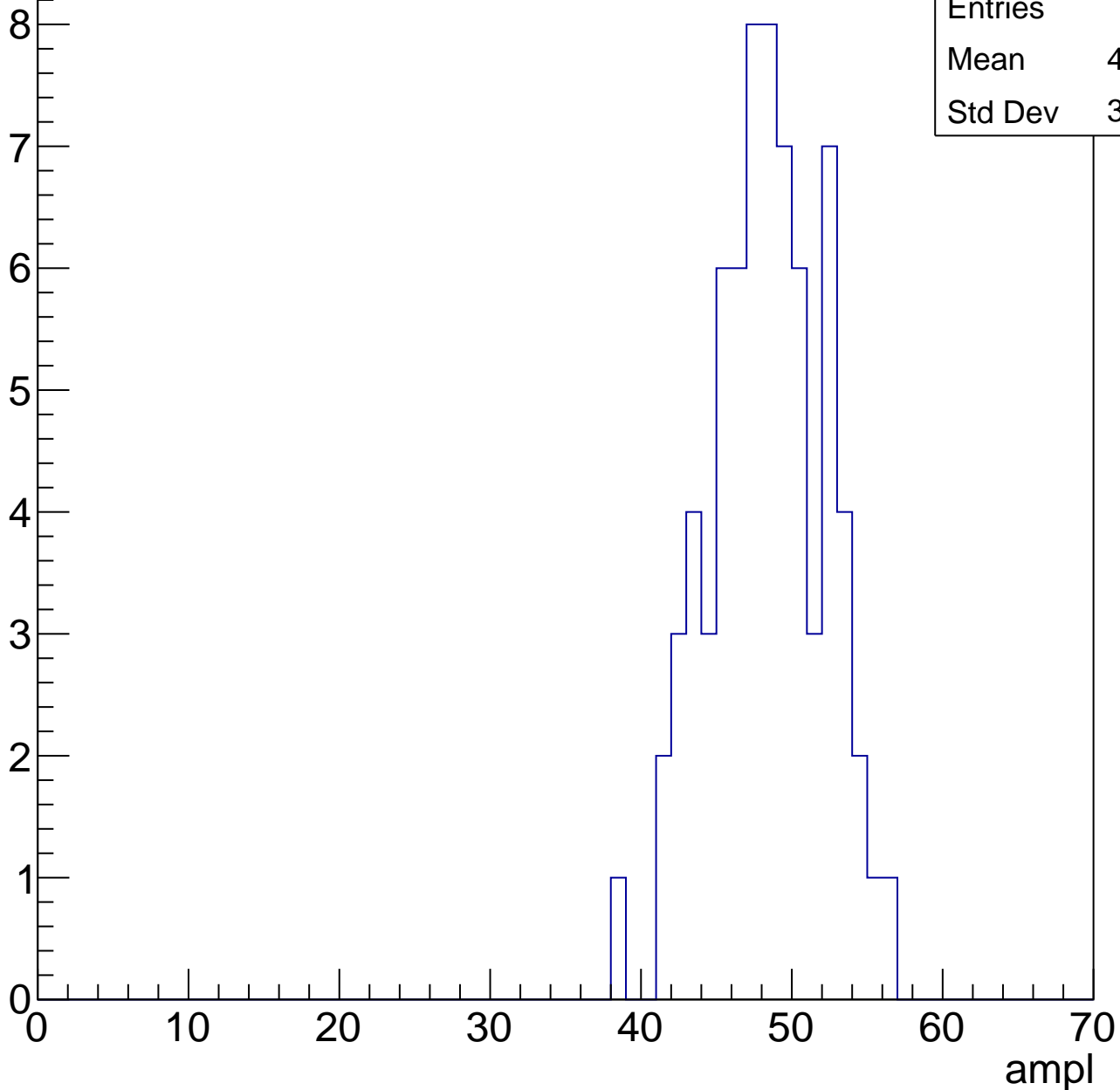


# B1L102S, U20-ch36, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	47.88
Std Dev	3.715

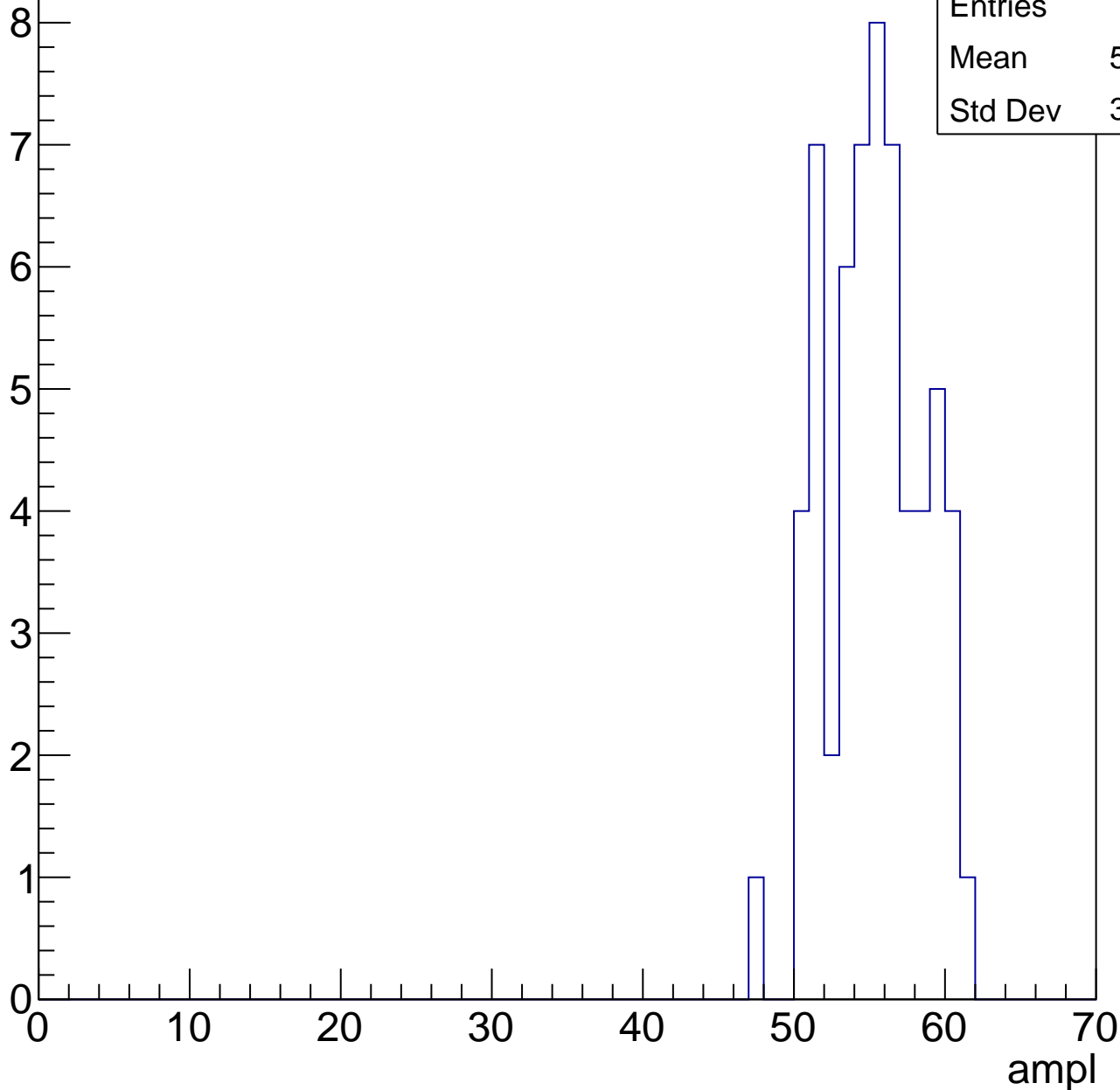


# B1L102S, U20-ch36, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	54.87
Std Dev	3.159

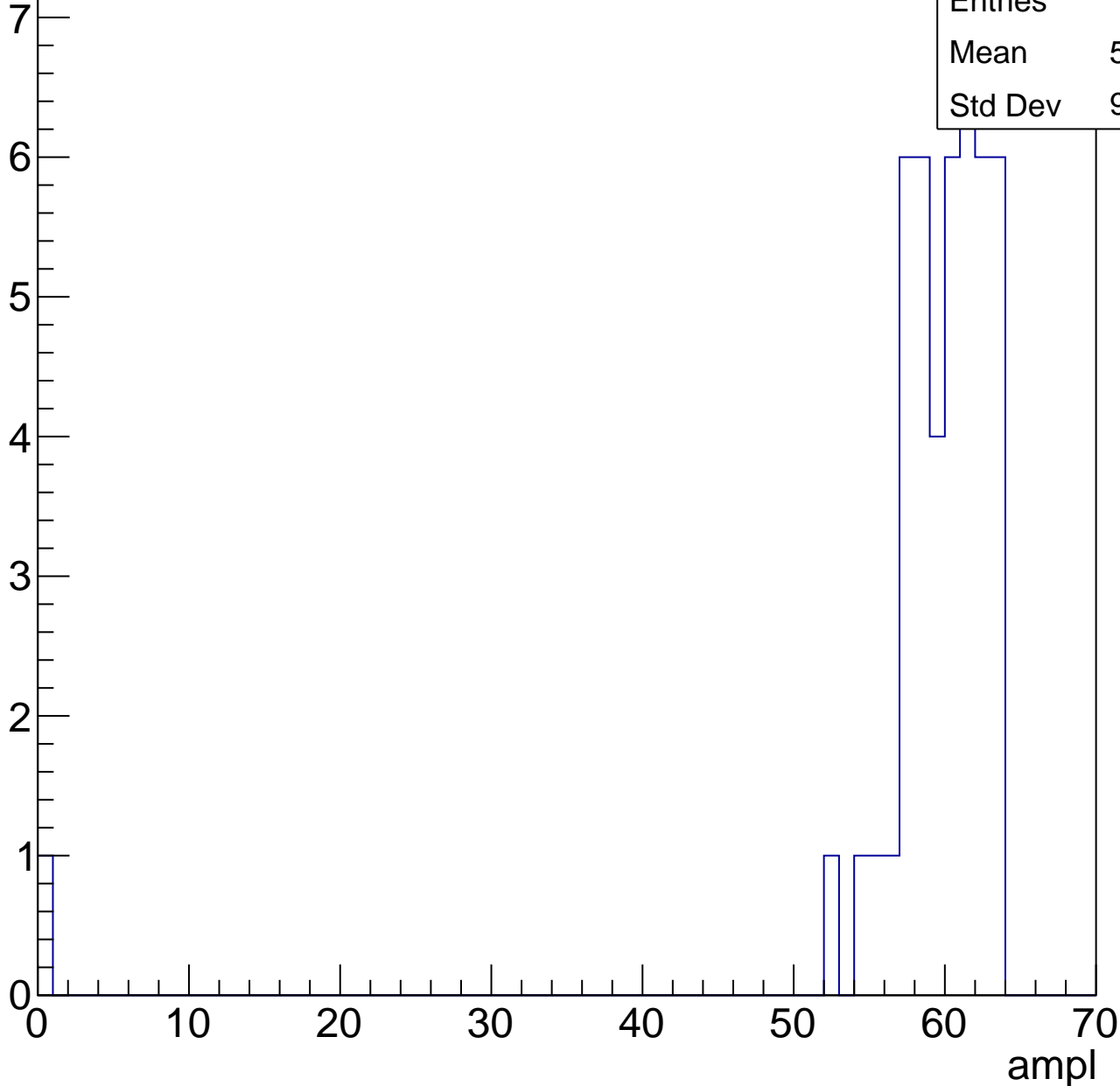


# B1L102S, U20-ch36, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

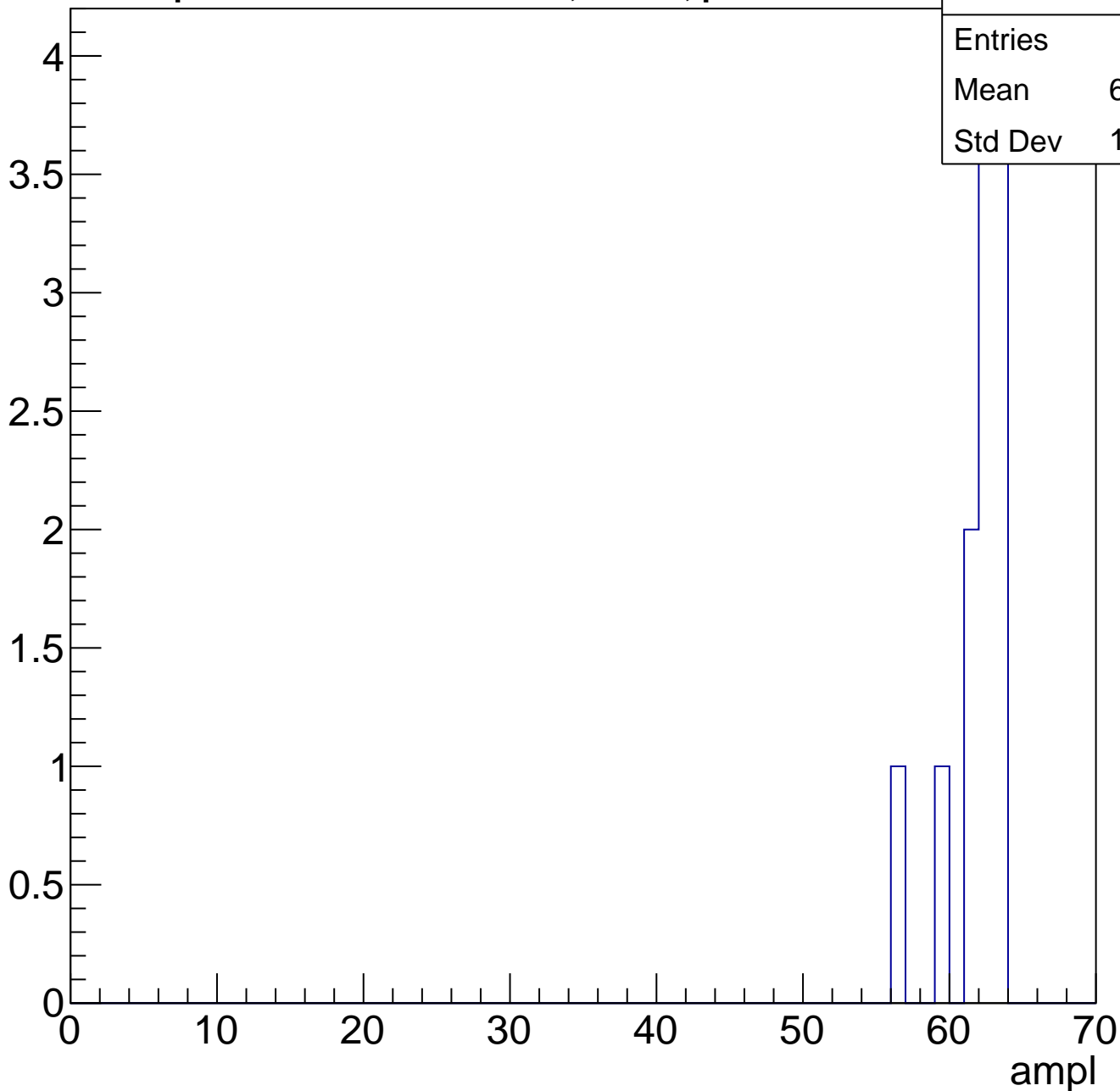
Entries	46
Mean	58.26
Std Dev	9.052



# B1L102S, U20-ch36, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	12
Mean	61.42
Std Dev	1.977



# B1L102S, U20-ch36, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch37, adc0

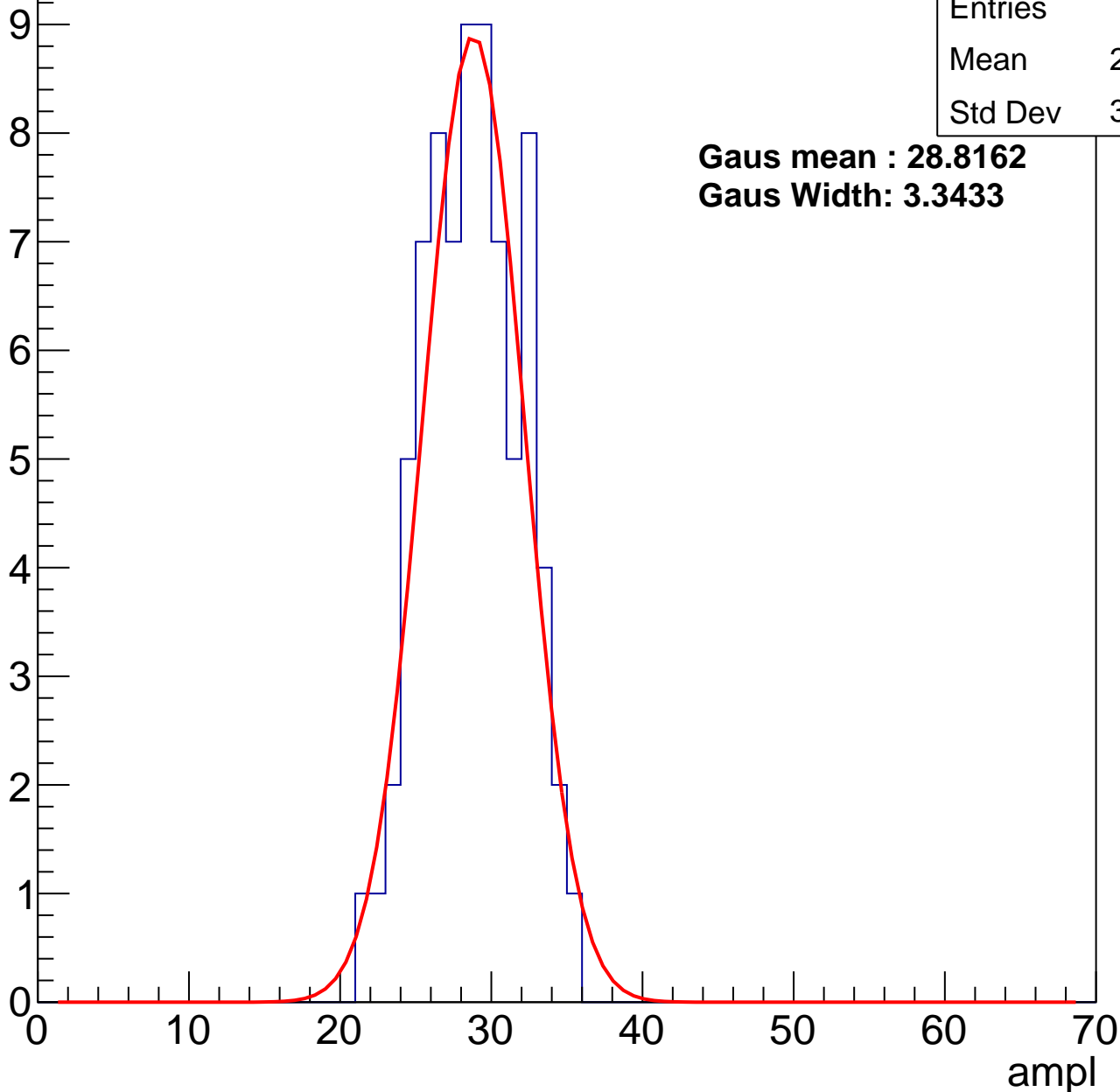
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	28.29
Std Dev	3.124

**Gaus mean : 28.8162**

**Gaus Width: 3.3433**



# B1L102S, U20-ch37, adc1

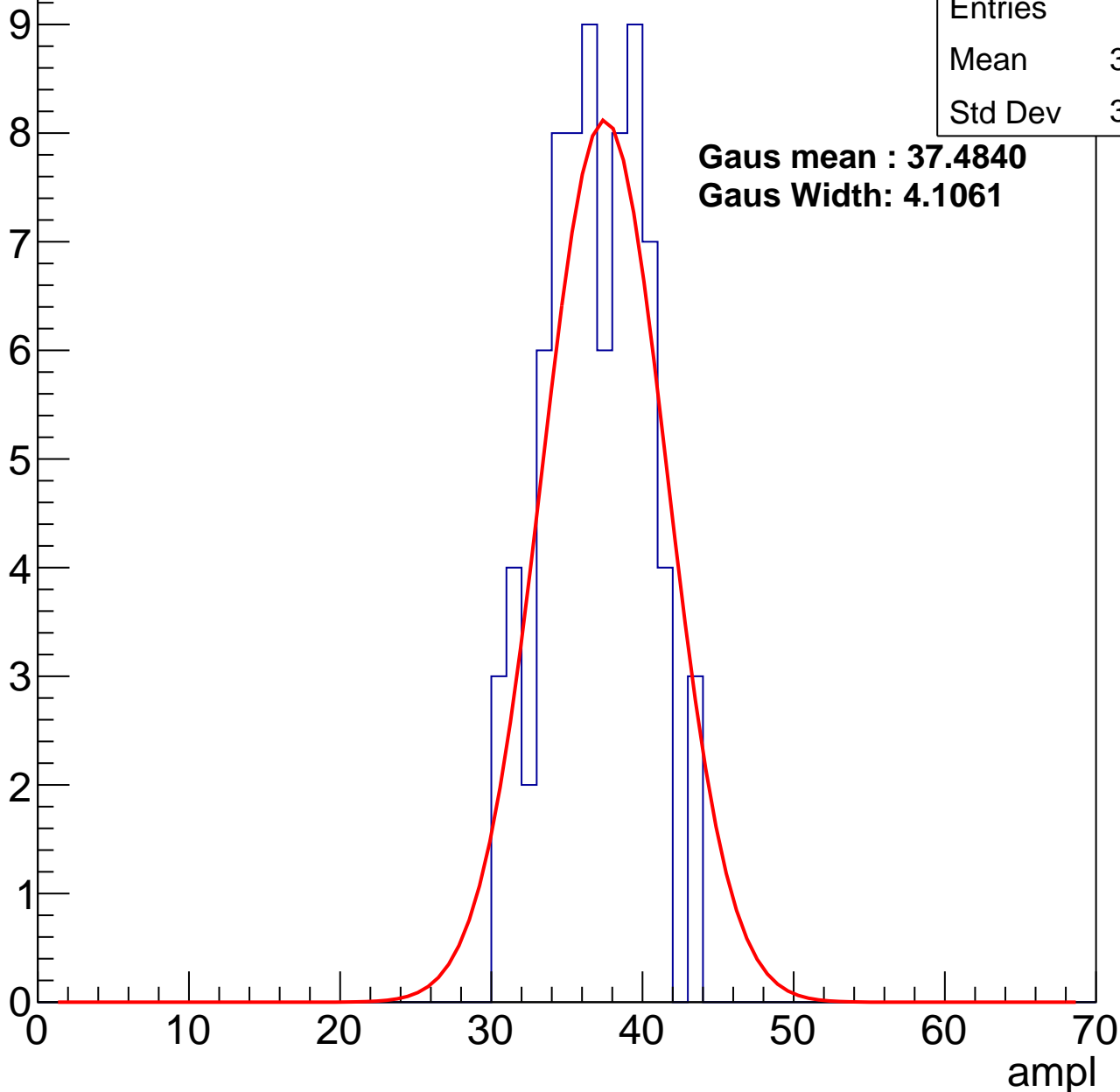
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	36.39
Std Dev	3.224

**Gaus mean : 37.4840**

**Gaus Width: 4.1061**



# B1L102S, U20-ch37, adc2

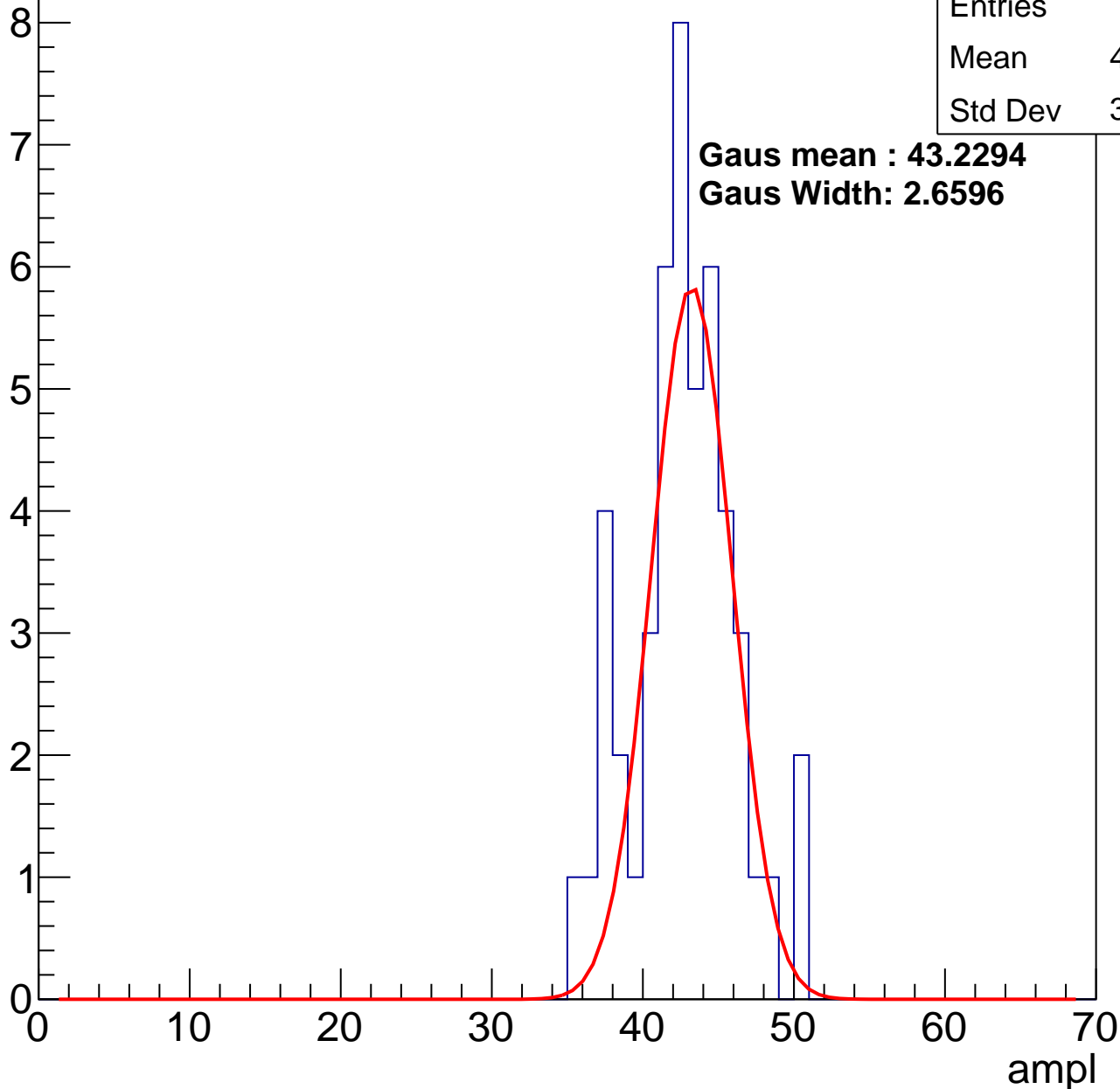
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	48
Mean	42.25
Std Dev	3.363

**Gaus mean : 43.2294**

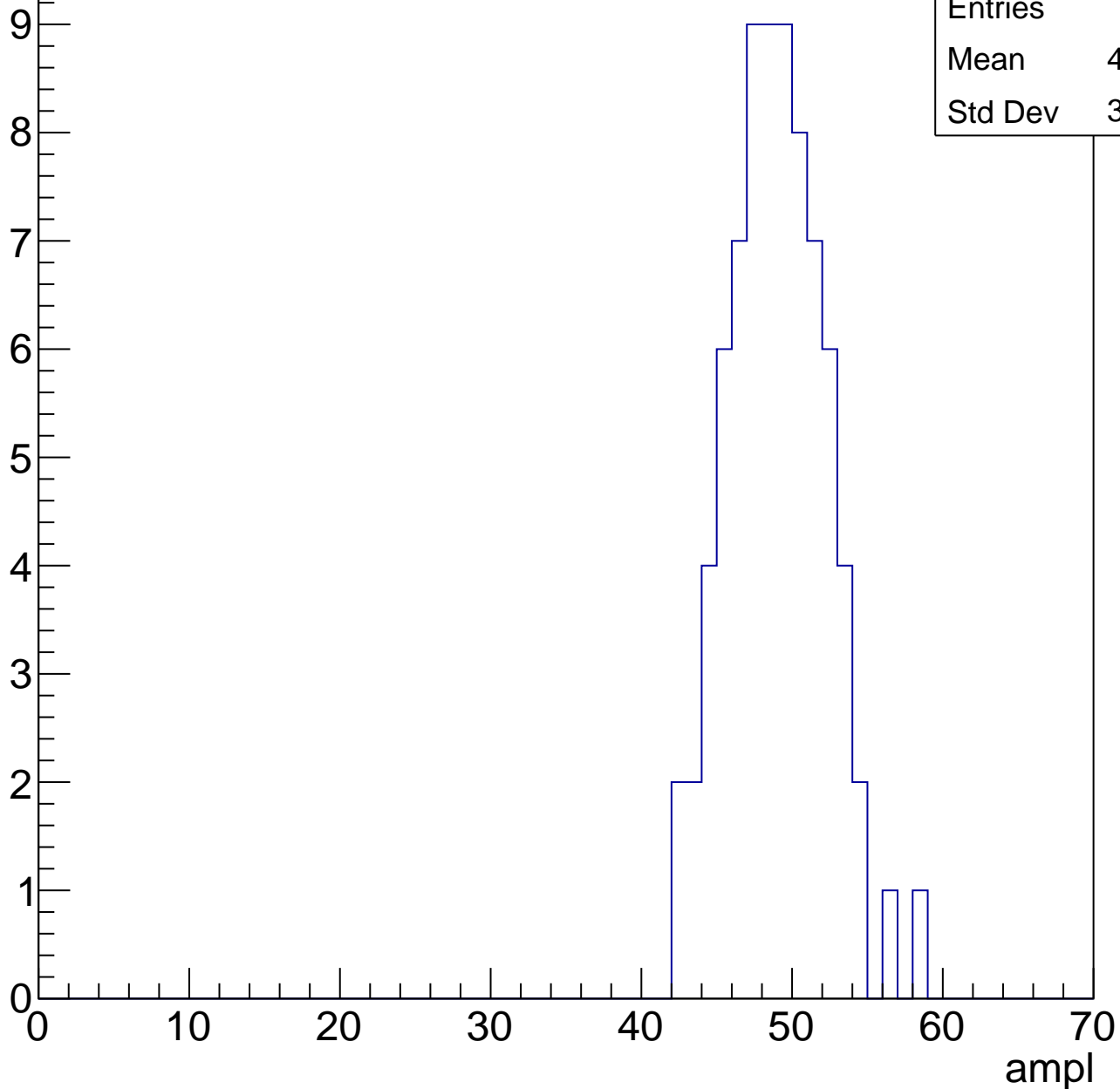
**Gaus Width: 2.6596**



# B1L102S, U20-ch37, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

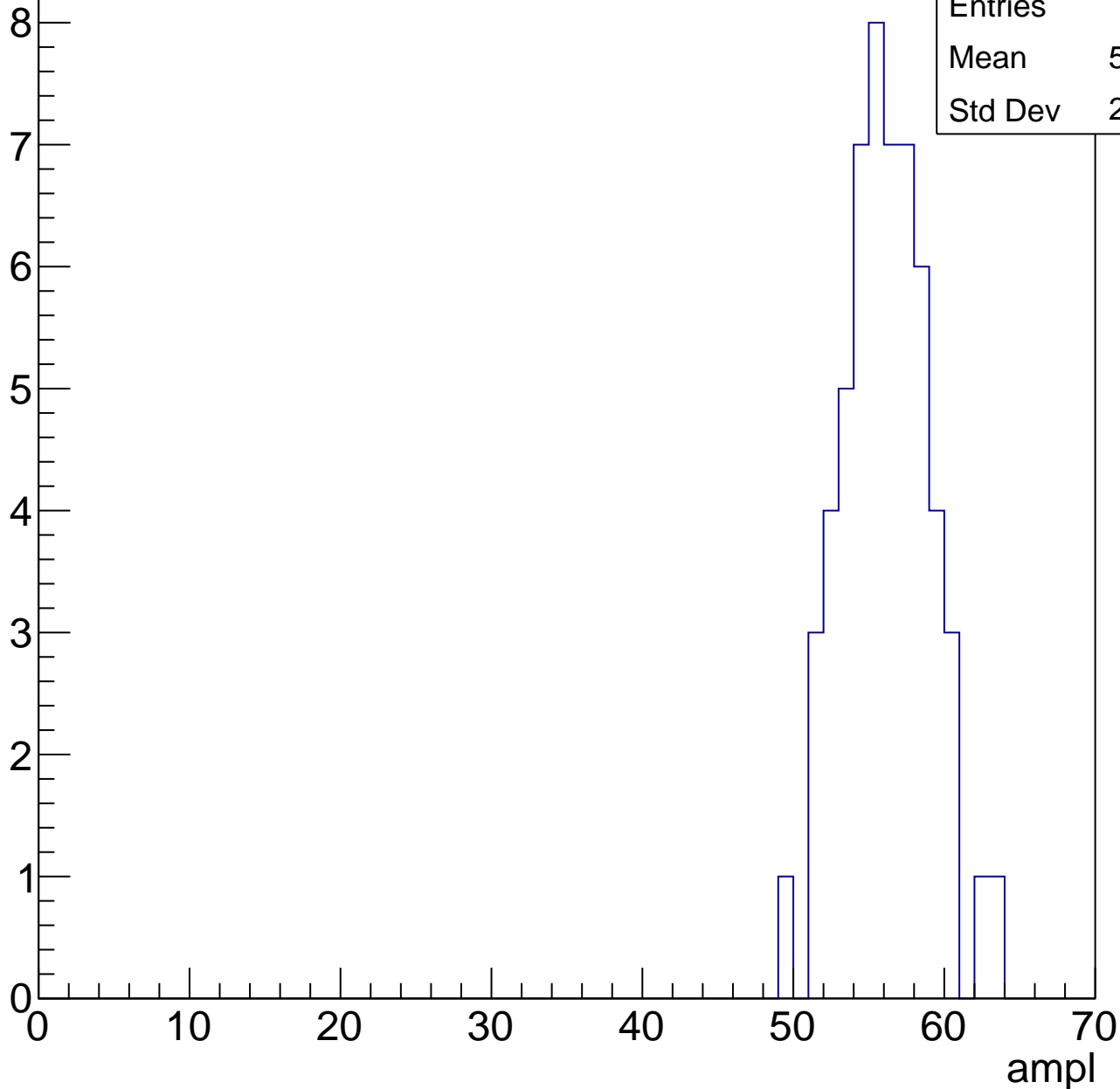


# B1L102S, U20-ch37, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	55.67
Std Dev	2.849

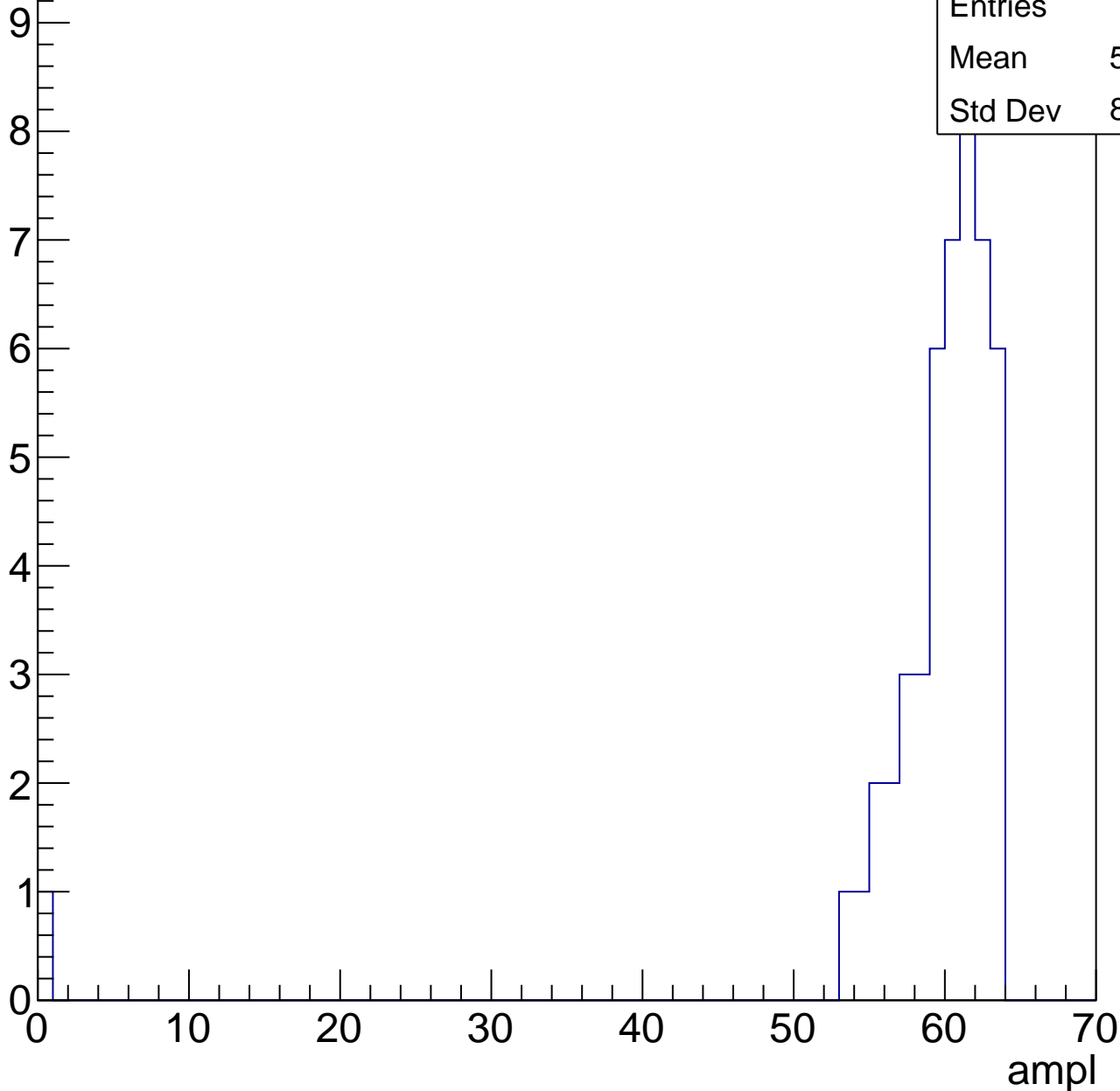


# B1L102S, U20-ch37, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	48
Mean	58.52
Std Dev	8.895



# B1L102S, U20-ch37, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

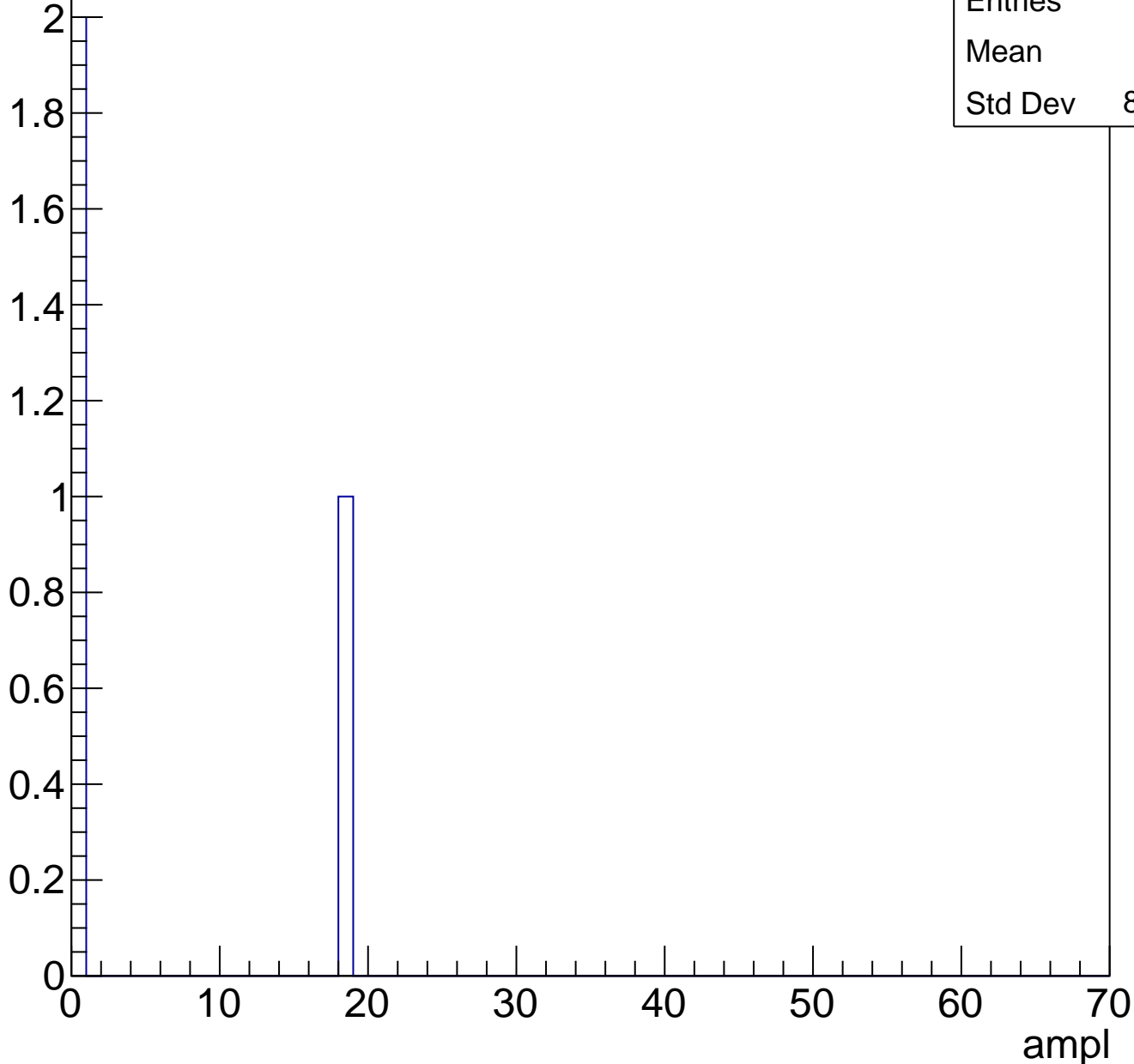




# B1L102S, U20-ch37, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	3
Mean	6
Std Dev	8.485

# B1L102S, U20-ch38, adc0

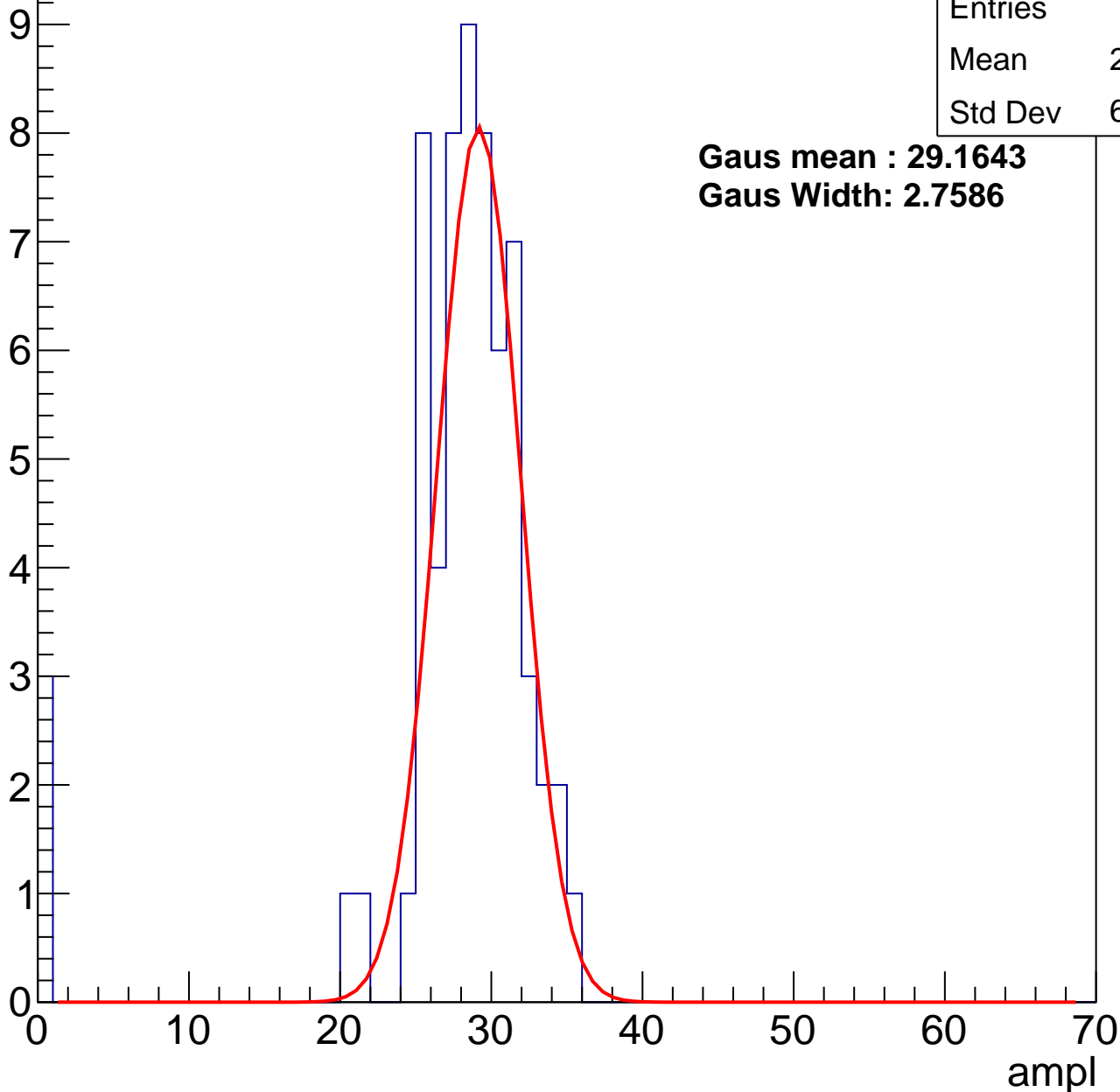
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	27.05
Std Dev	6.653

**Gaus mean : 29.1643**

**Gaus Width: 2.7586**



# B1L102S, U20-ch38, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	77
Mean	35.73
Std Dev	3.522

**Gaus mean : 36.1493**

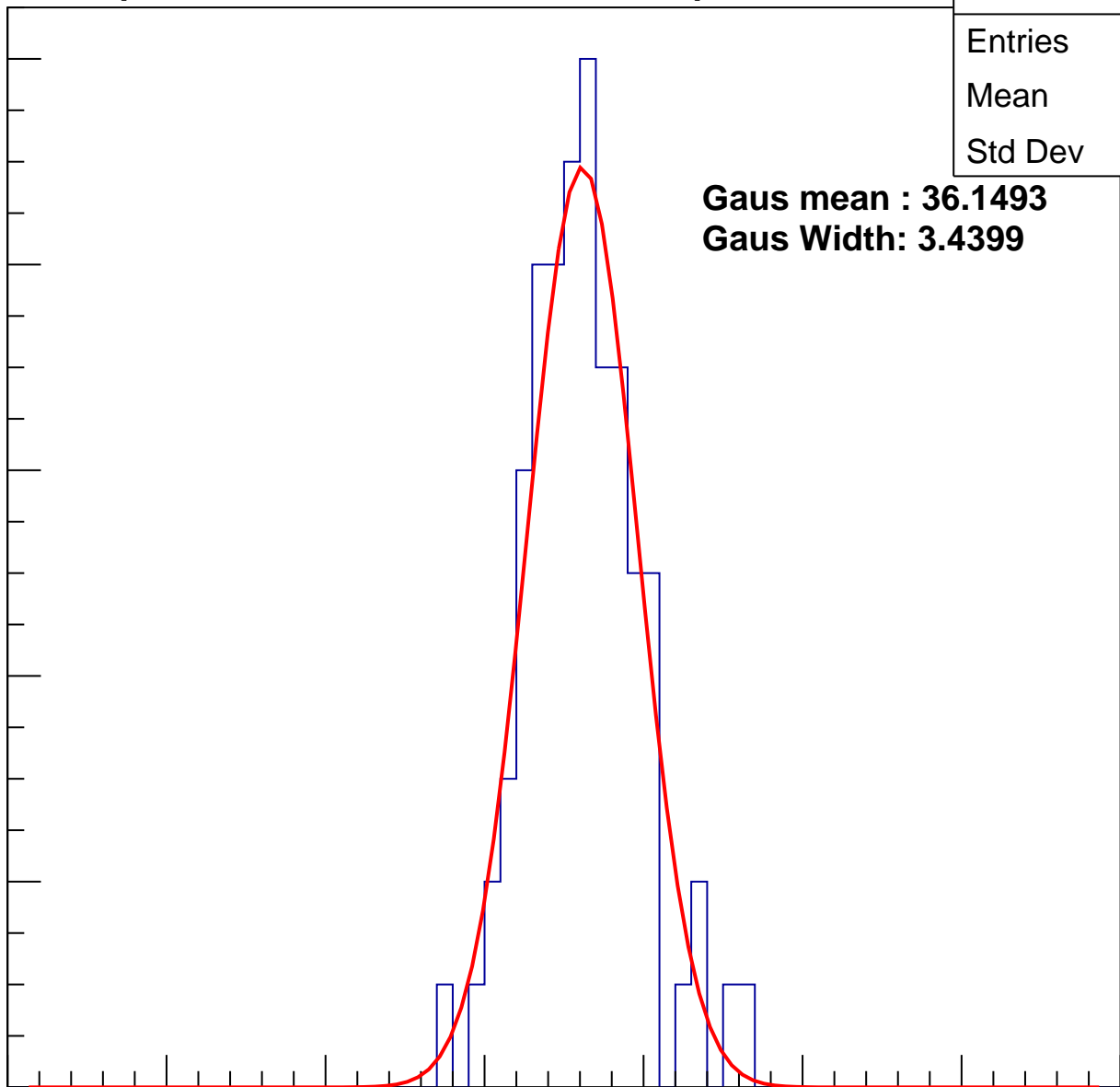
**Gaus Width: 3.4399**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U20-ch38, adc2

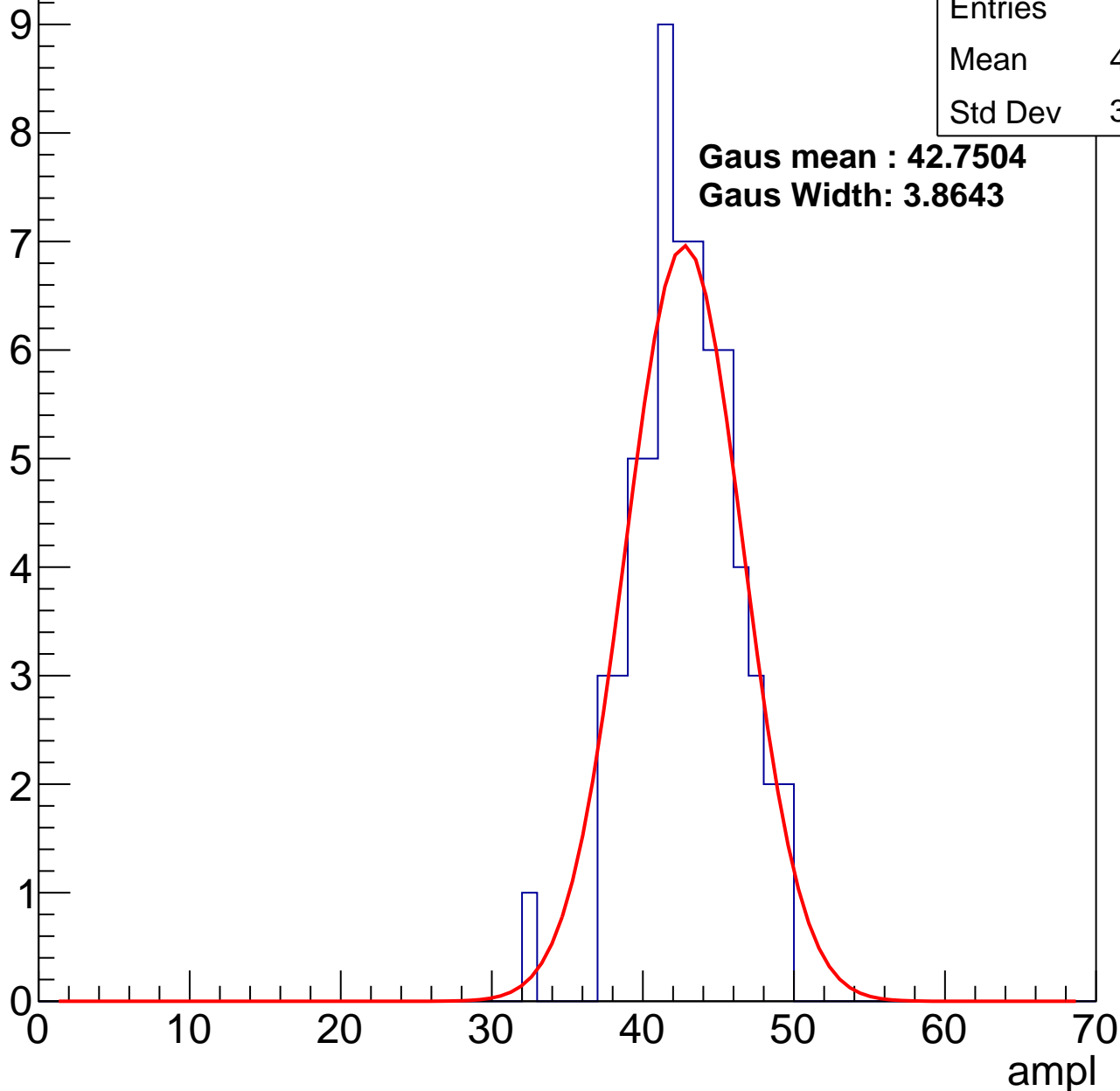
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	42.37
Std Dev	3.292

**Gaus mean : 42.7504**

**Gaus Width: 3.8643**

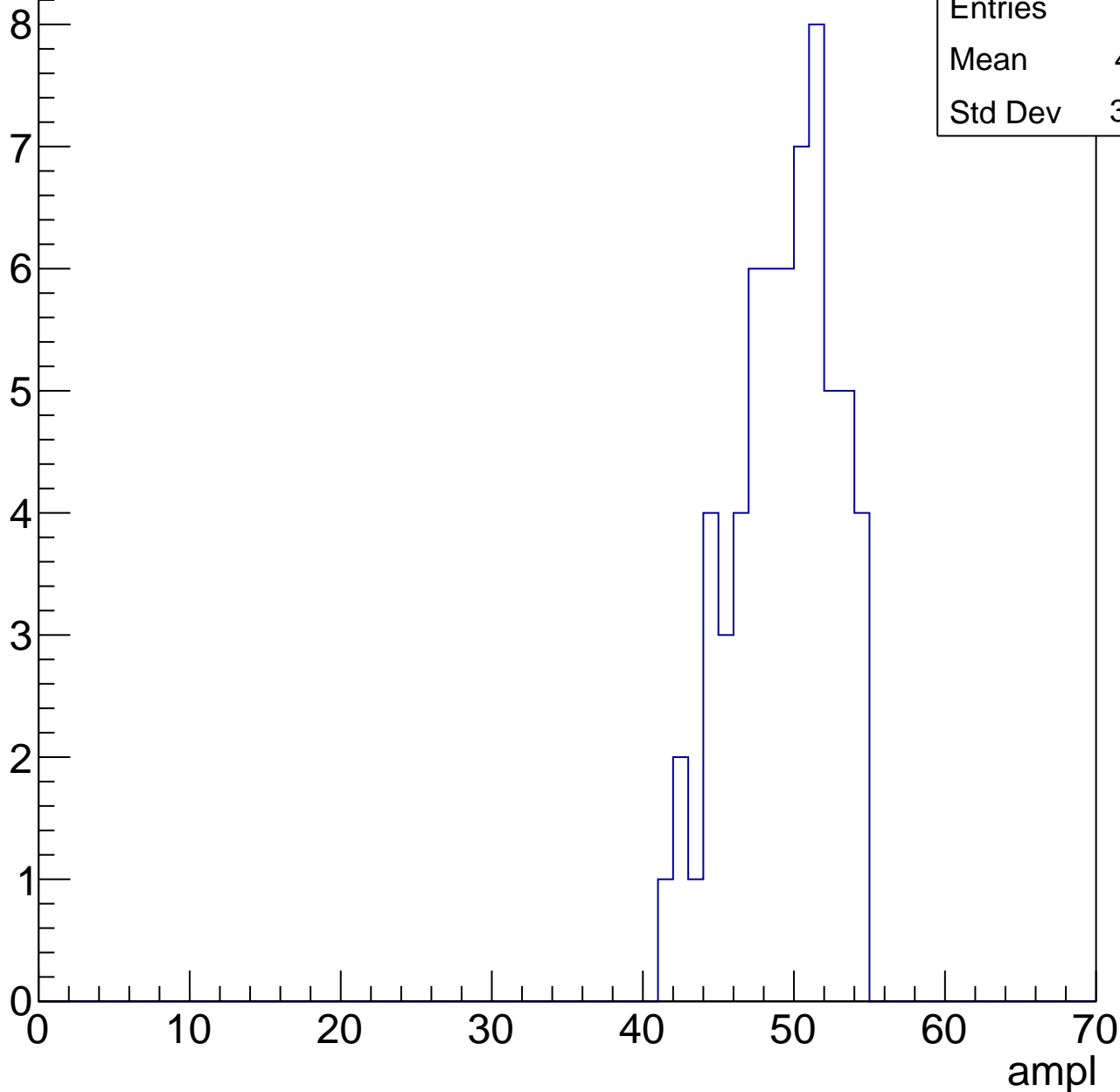


# B1L102S, U20-ch38, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	48.81
Std Dev	3.296

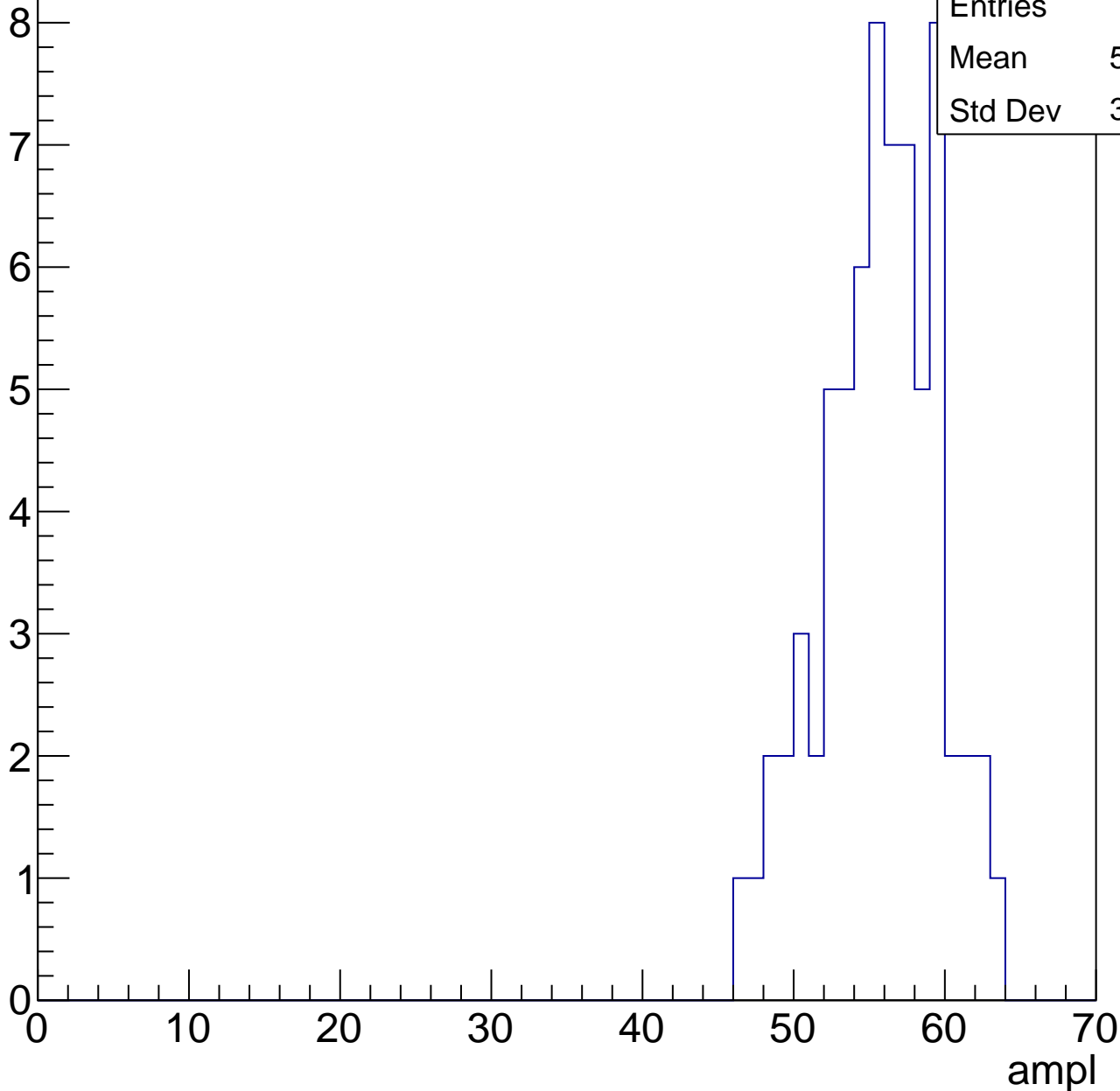


# B1L102S, U20-ch38, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	55.22
Std Dev	3.772

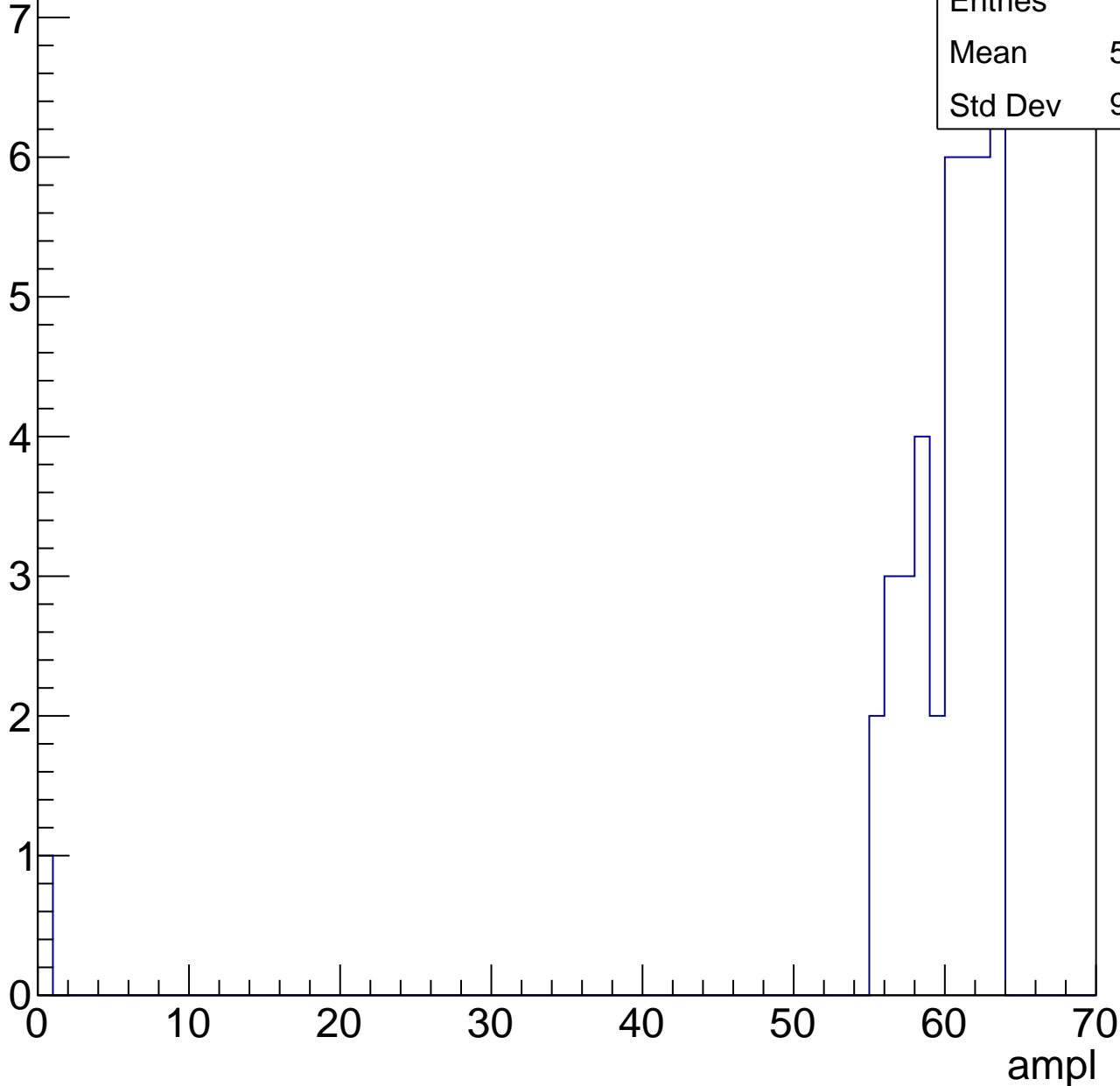


# B1L102S, U20-ch38, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

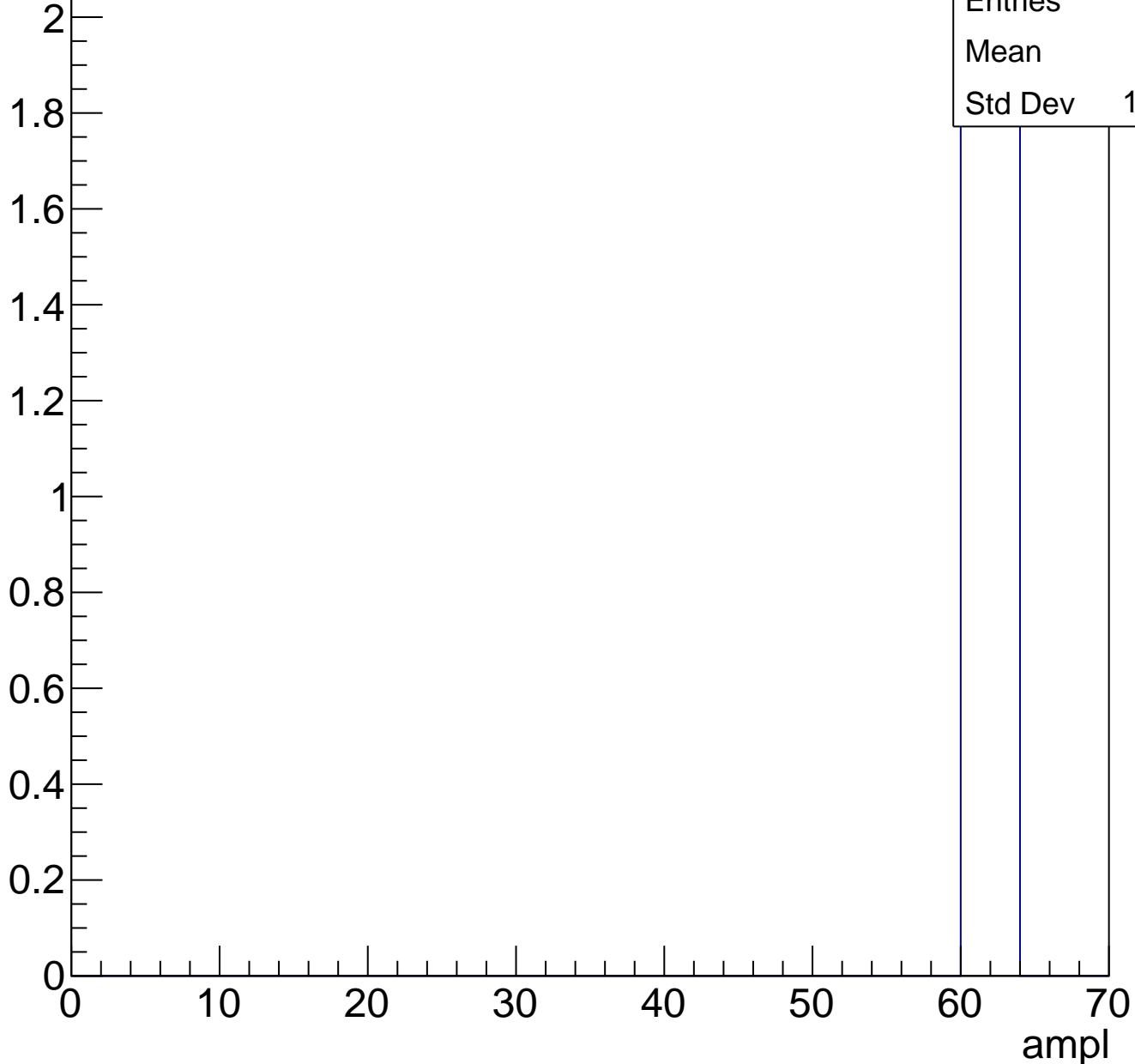
Entries	40
Mean	58.45
Std Dev	9.669



# B1L102S, U20-ch38, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

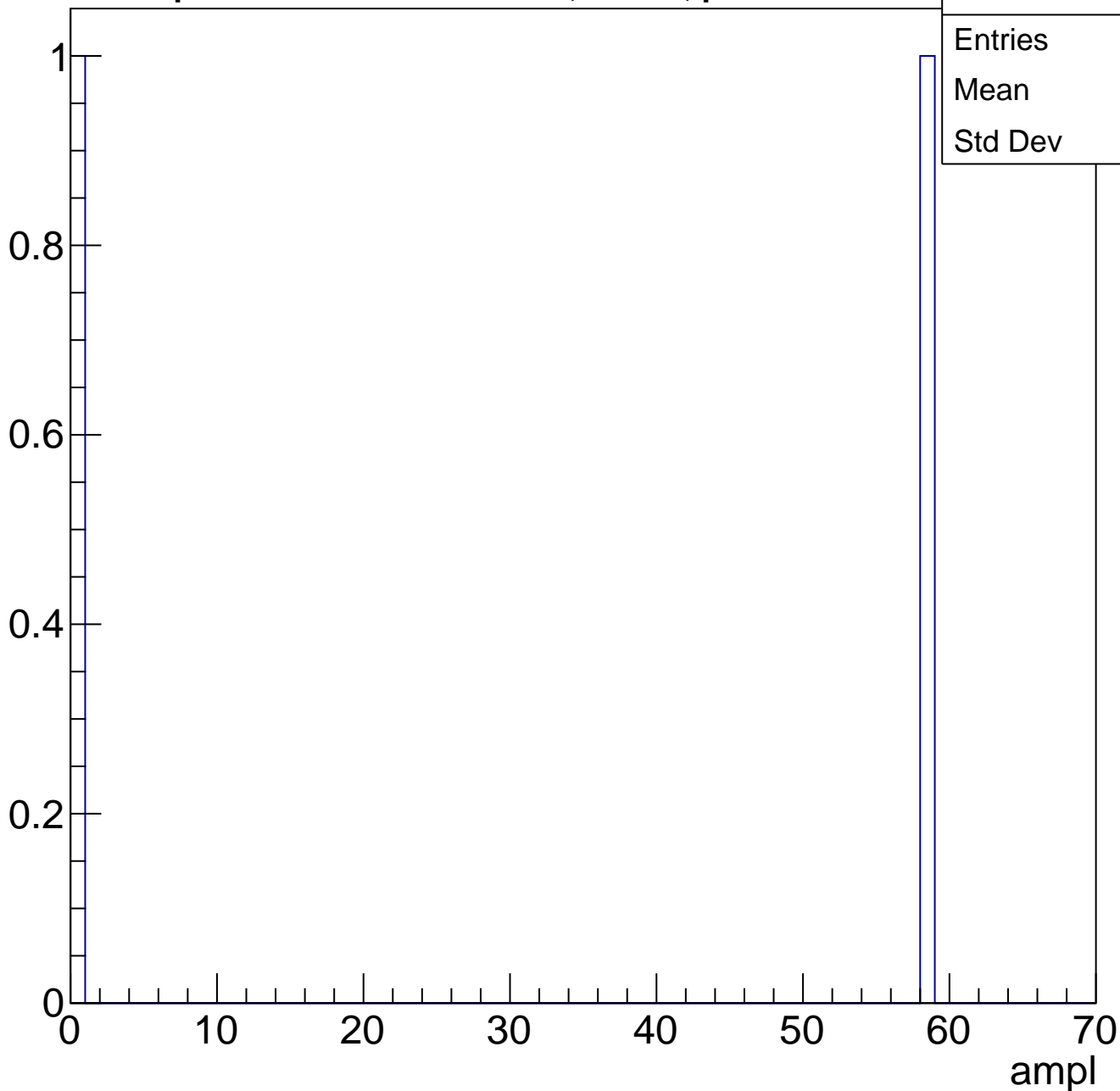




# B1L102S, U20-ch38, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch39, adc0

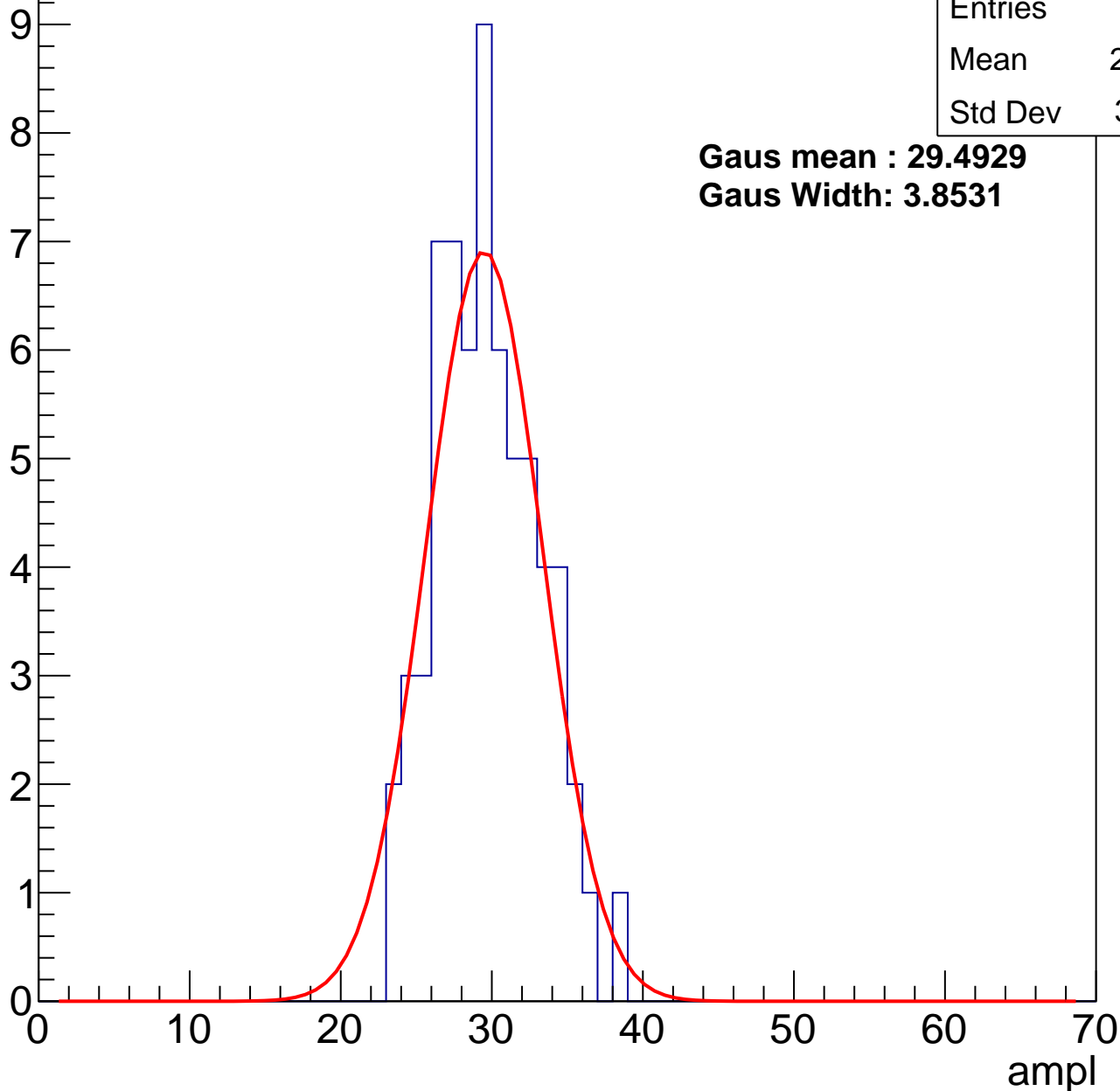
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	29.23
Std Dev	3.341

**Gaus mean : 29.4929**

**Gaus Width: 3.8531**



# B1L102S, U20-ch39, adc1

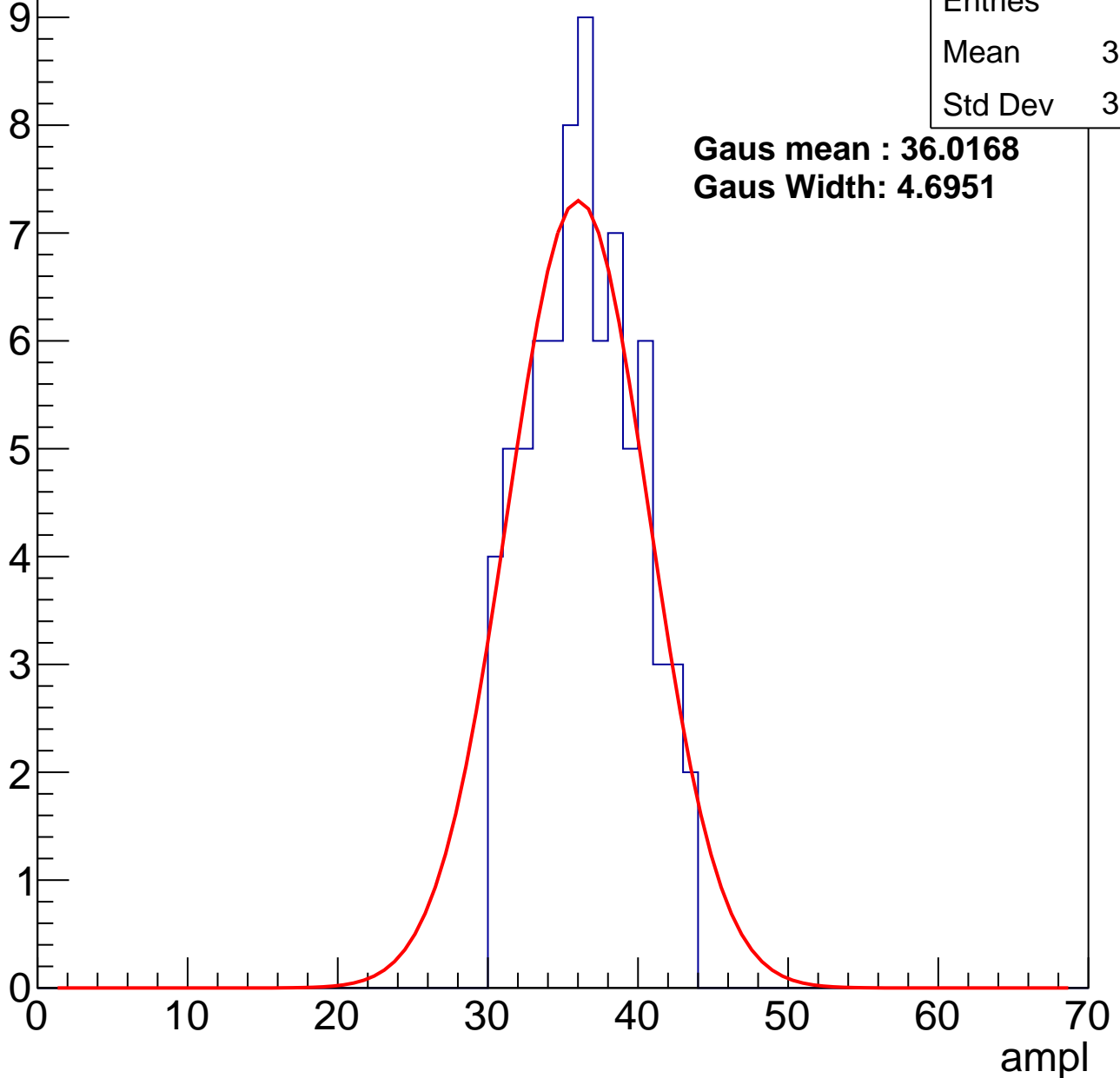
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	35.99
Std Dev	3.447

**Gaus mean : 36.0168**

**Gaus Width: 4.6951**



# B1L102S, U20-ch39, adc2

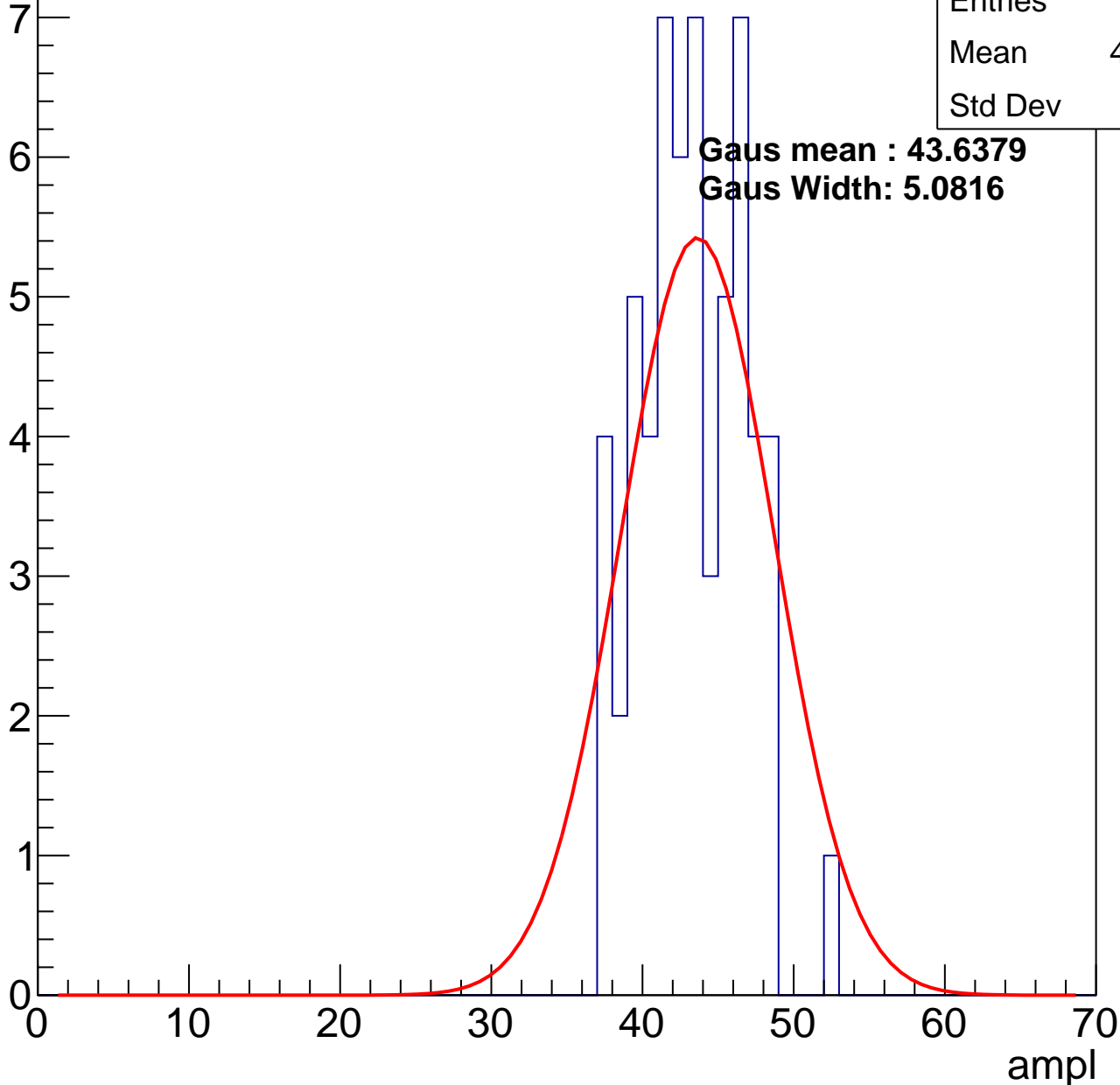
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	42.88
Std Dev	3.38

**Gaus mean : 43.6379**

**Gaus Width: 5.0816**

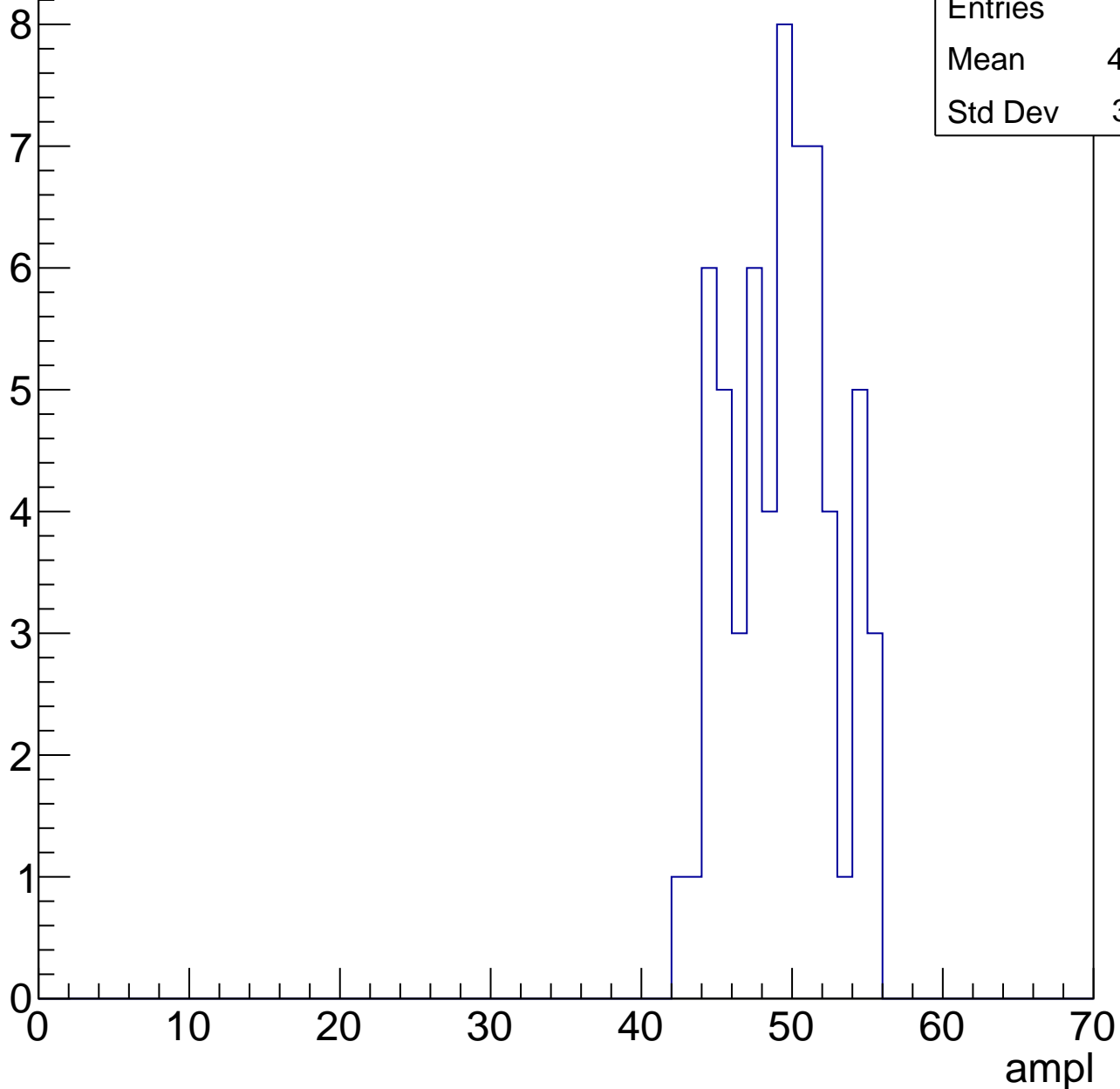


# B1L102S, U20-ch39, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	48.87
Std Dev	3.361

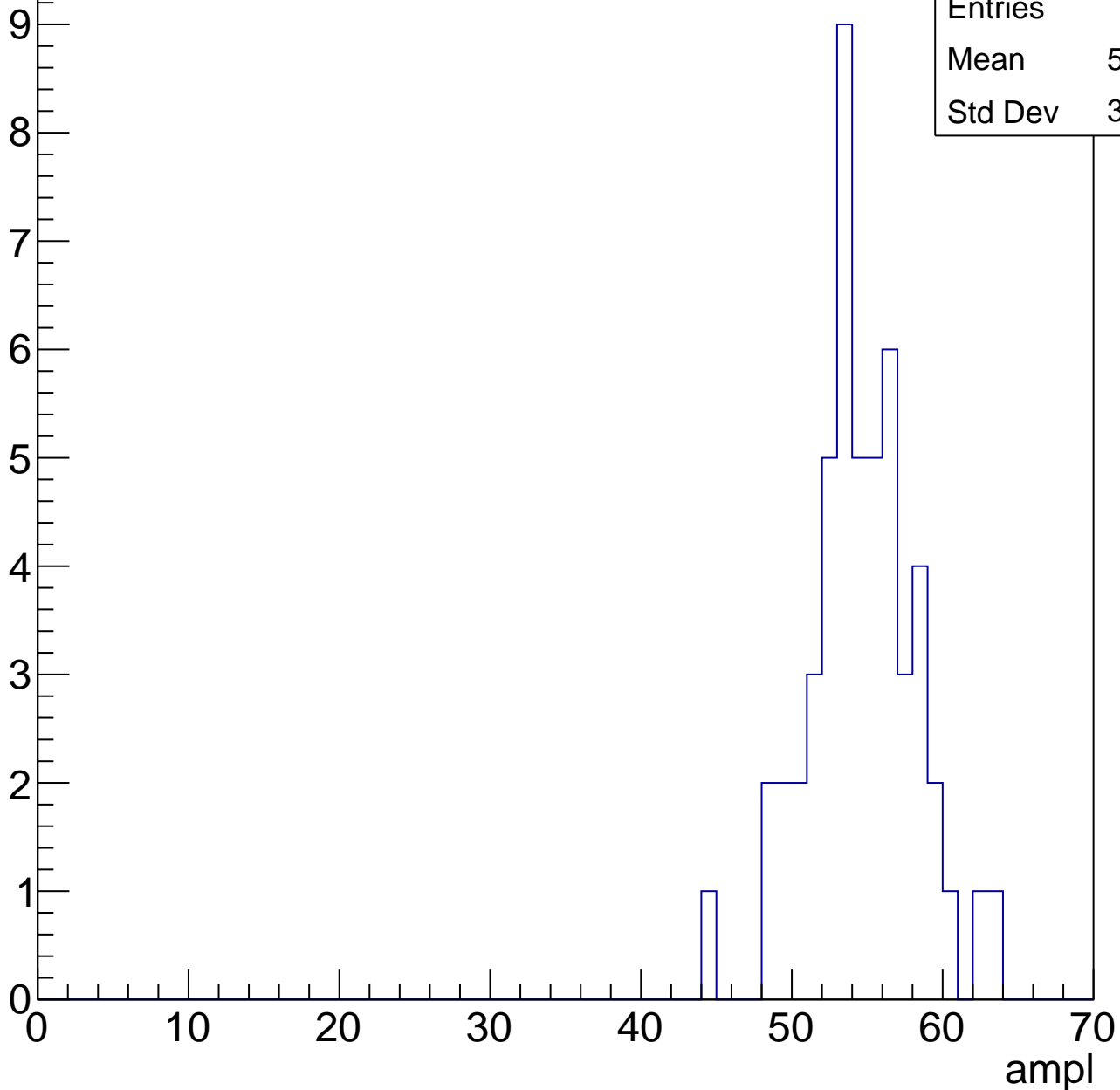


# B1L102S, U20-ch39, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	54.13
Std Dev	3.563

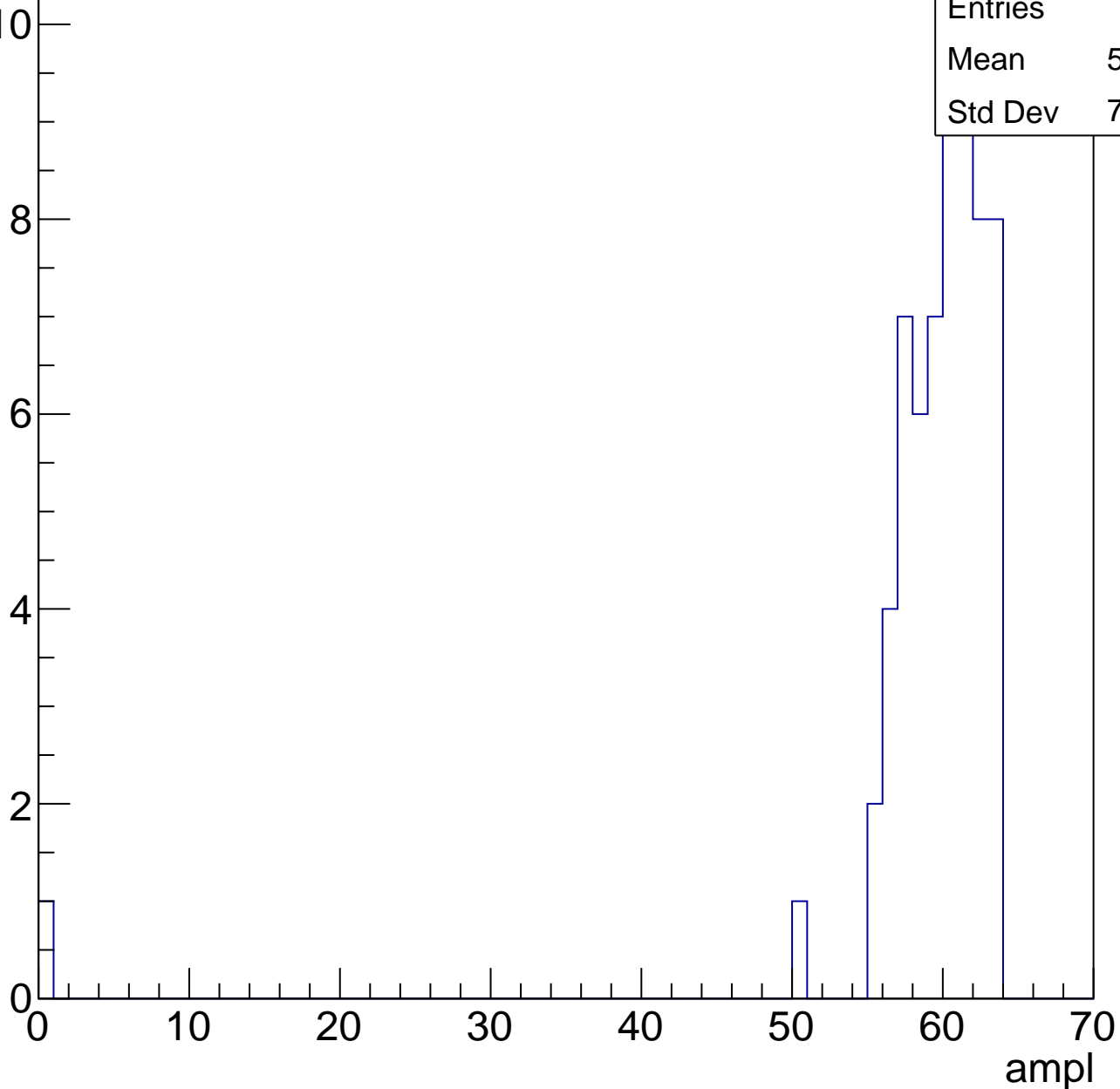


# B1L102S, U20-ch39, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

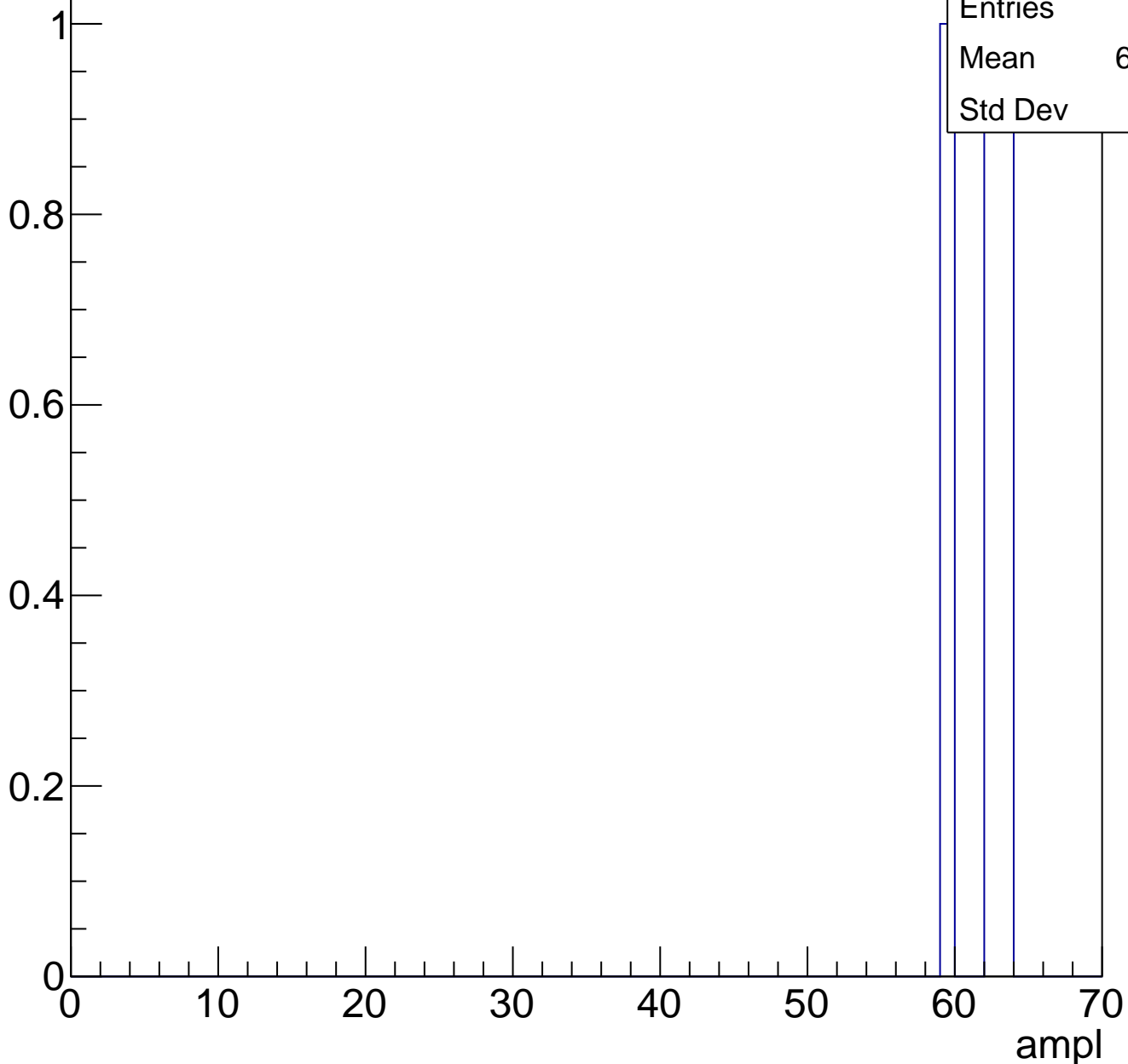
Entries	63
Mean	58.63
Std Dev	7.873



# B1L102S, U20-ch39, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U20-ch39, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch40, adc0

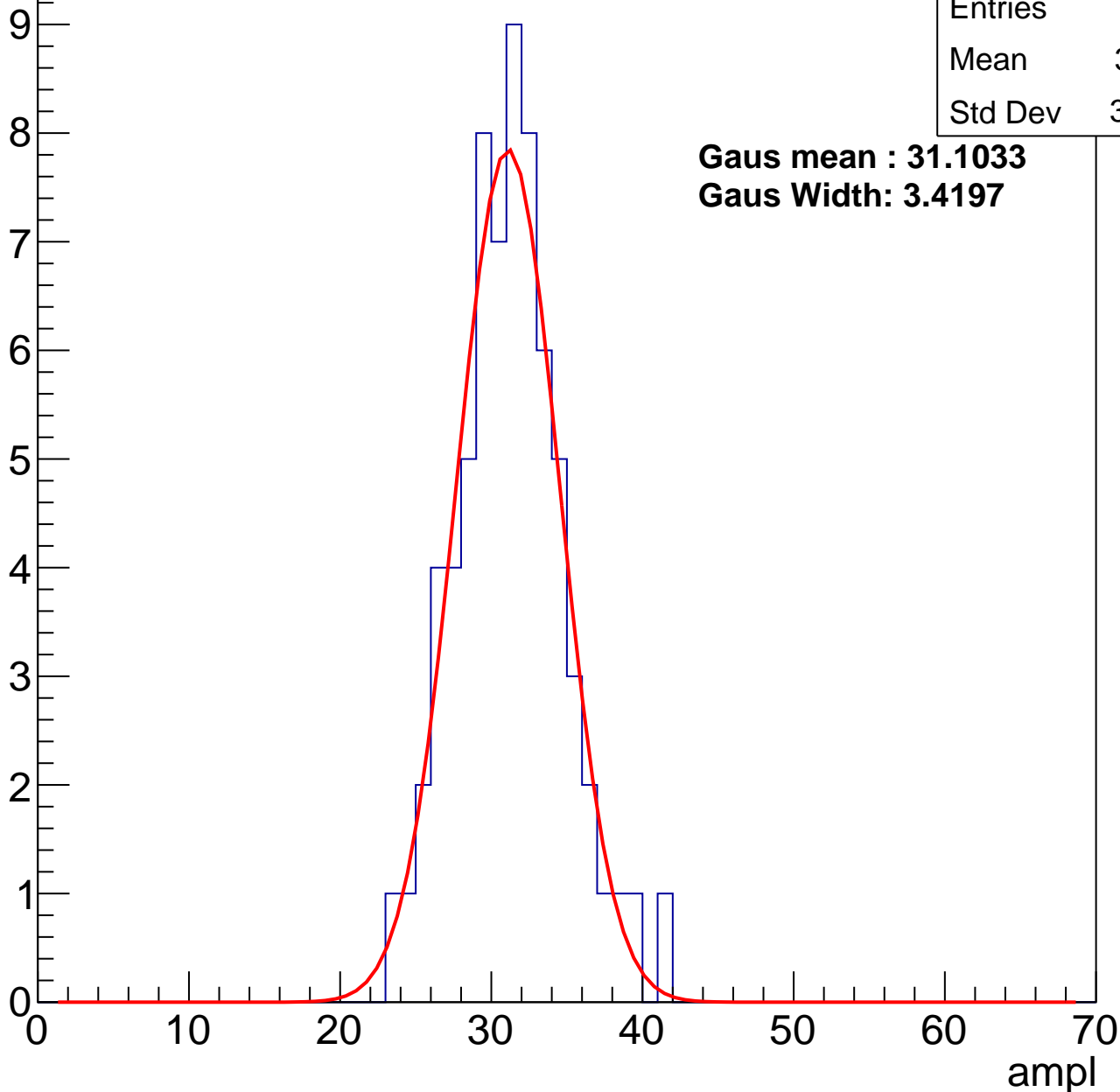
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	30.81
Std Dev	3.519

**Gaus mean : 31.1033**

**Gaus Width: 3.4197**



# B1L102S, U20-ch40, adc1

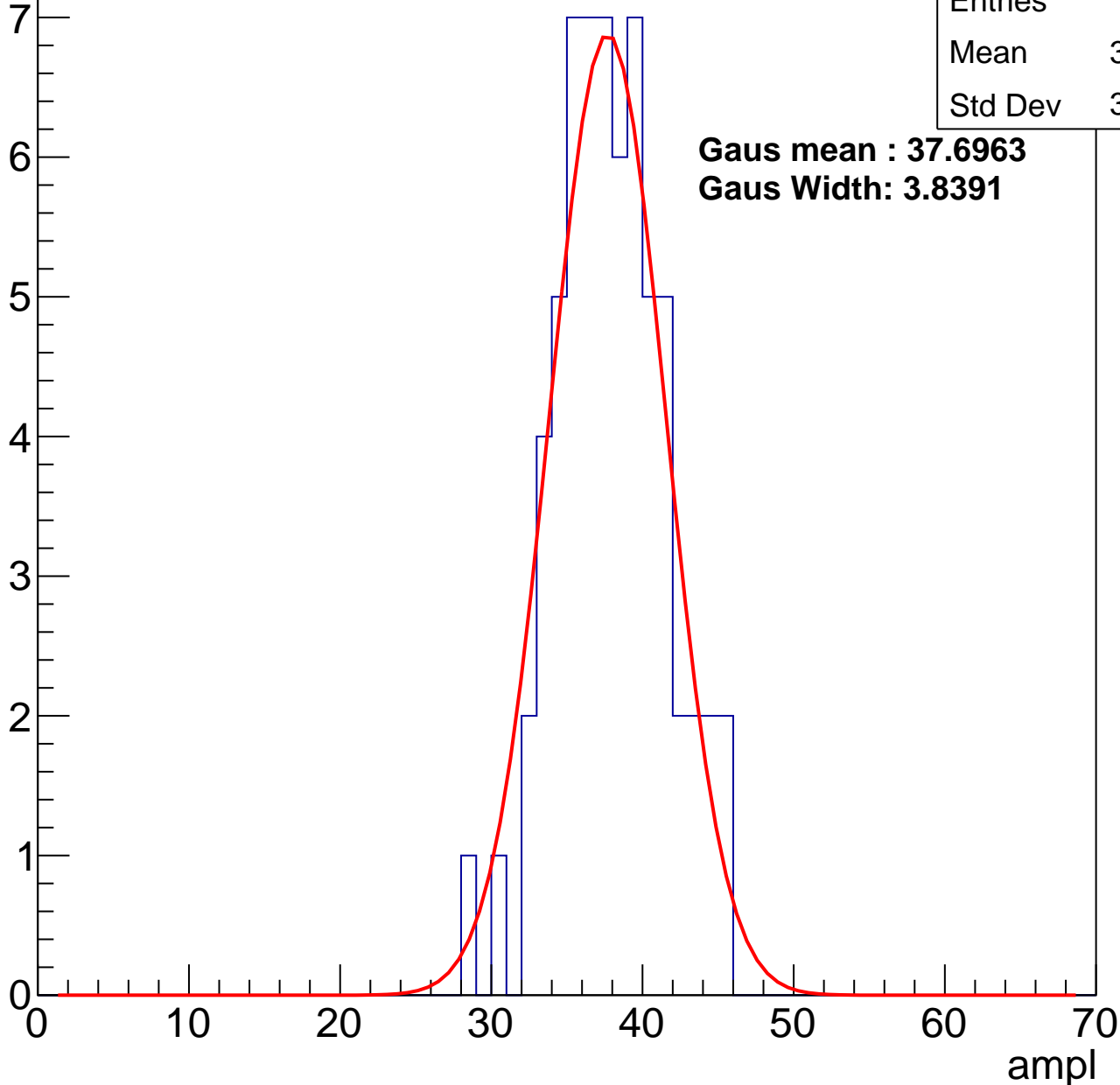
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	37.45
Std Dev	3.548

**Gaus mean : 37.6963**

**Gaus Width: 3.8391**



# B1L102S, U20-ch40, adc2

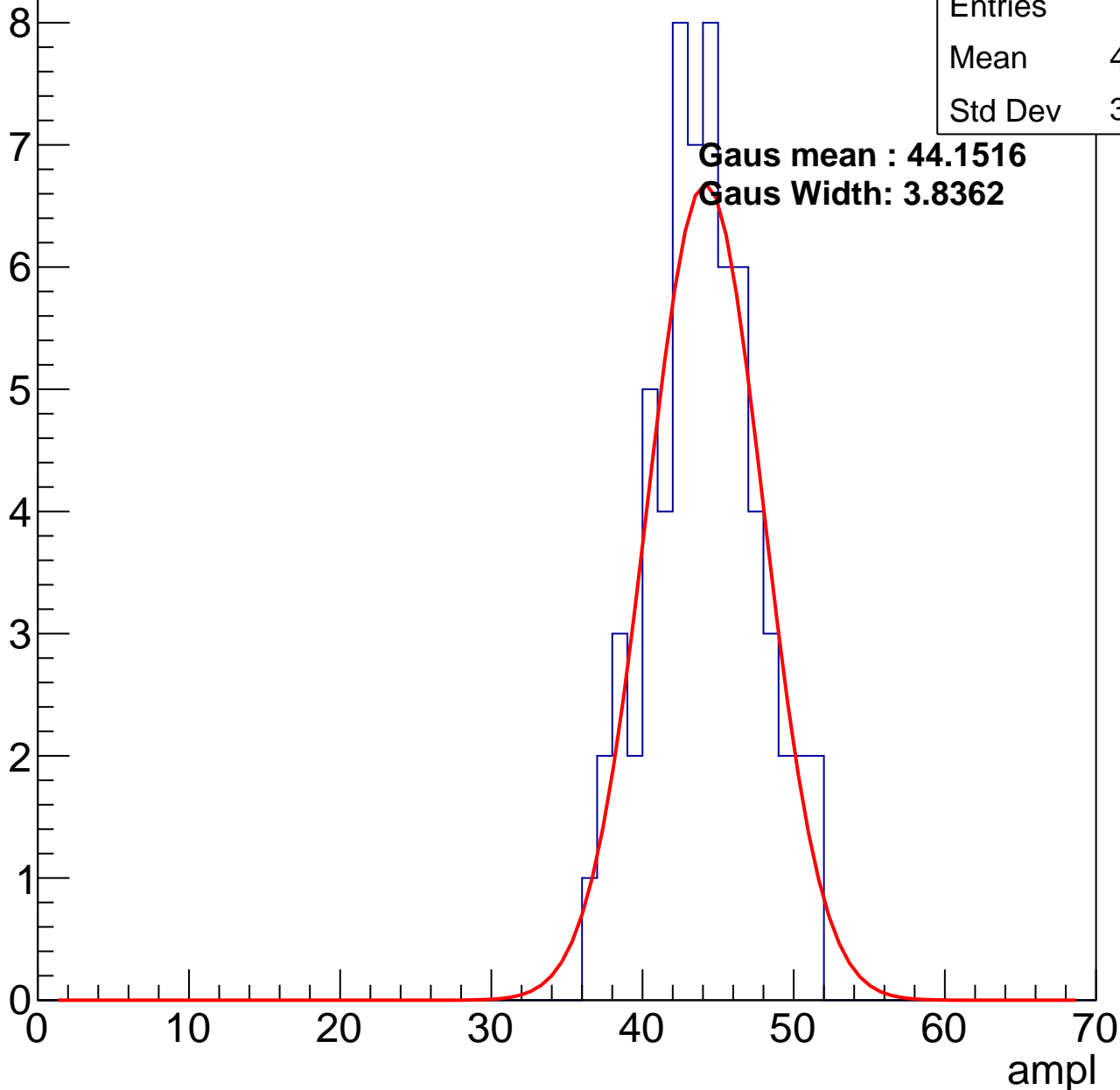
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	43.58
Std Dev	3.503

**Gaus mean : 44.1516**

**Gaus Width: 3.8362**

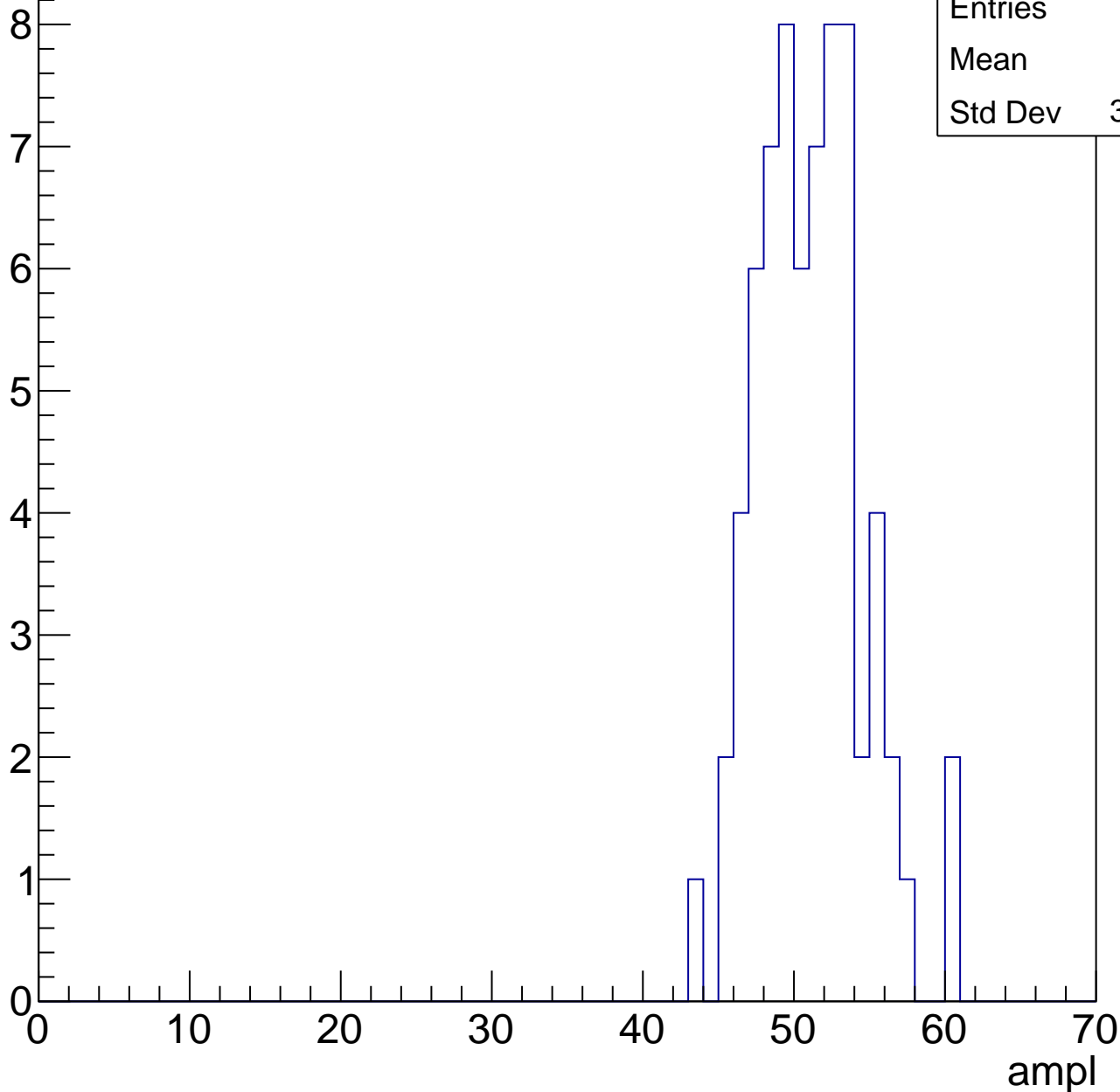


# B1L102S, U20-ch40, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	50.6
Std Dev	3.413

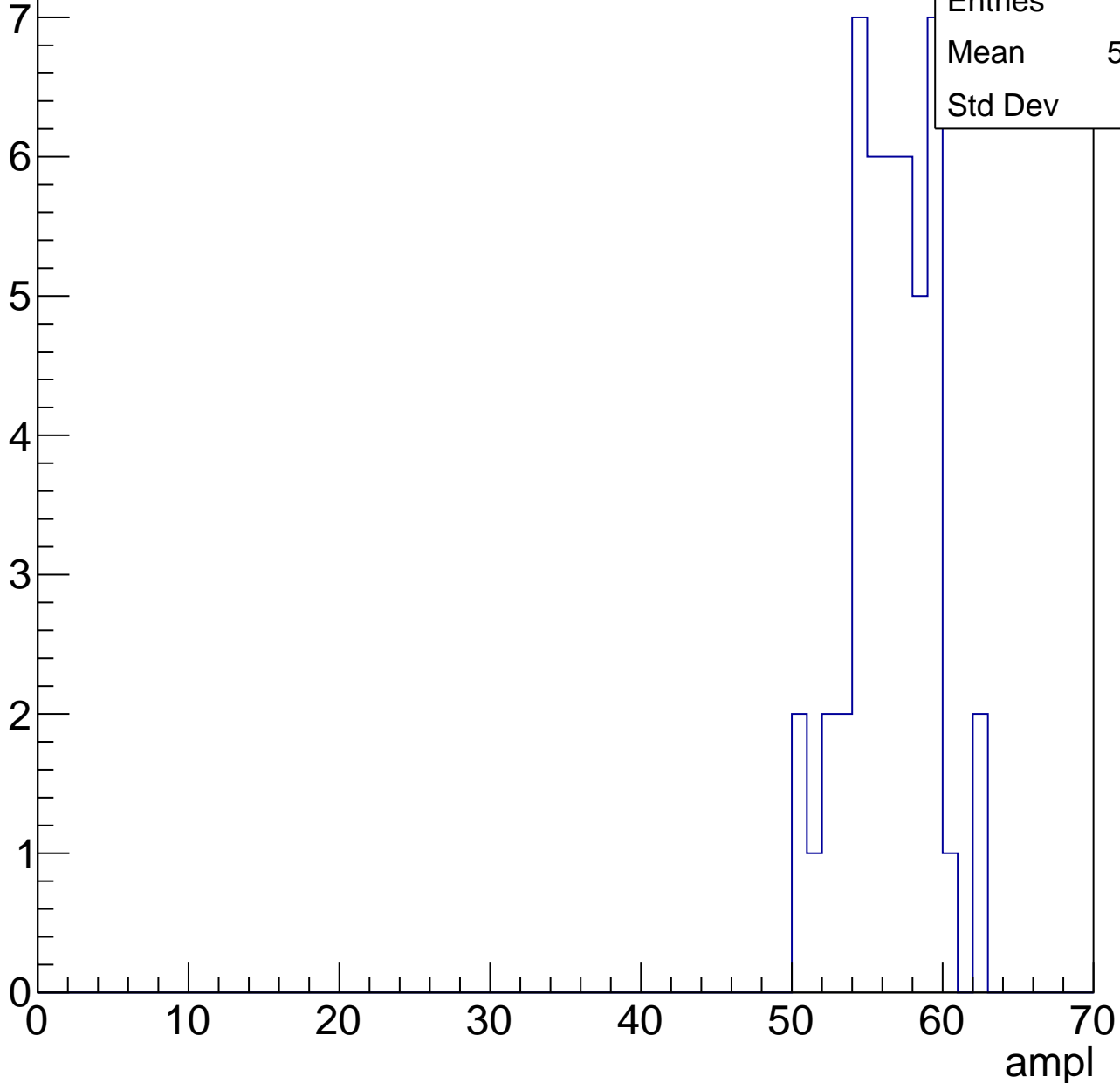


# B1L102S, U20-ch40, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	47
Mean	56.04
Std Dev	2.76

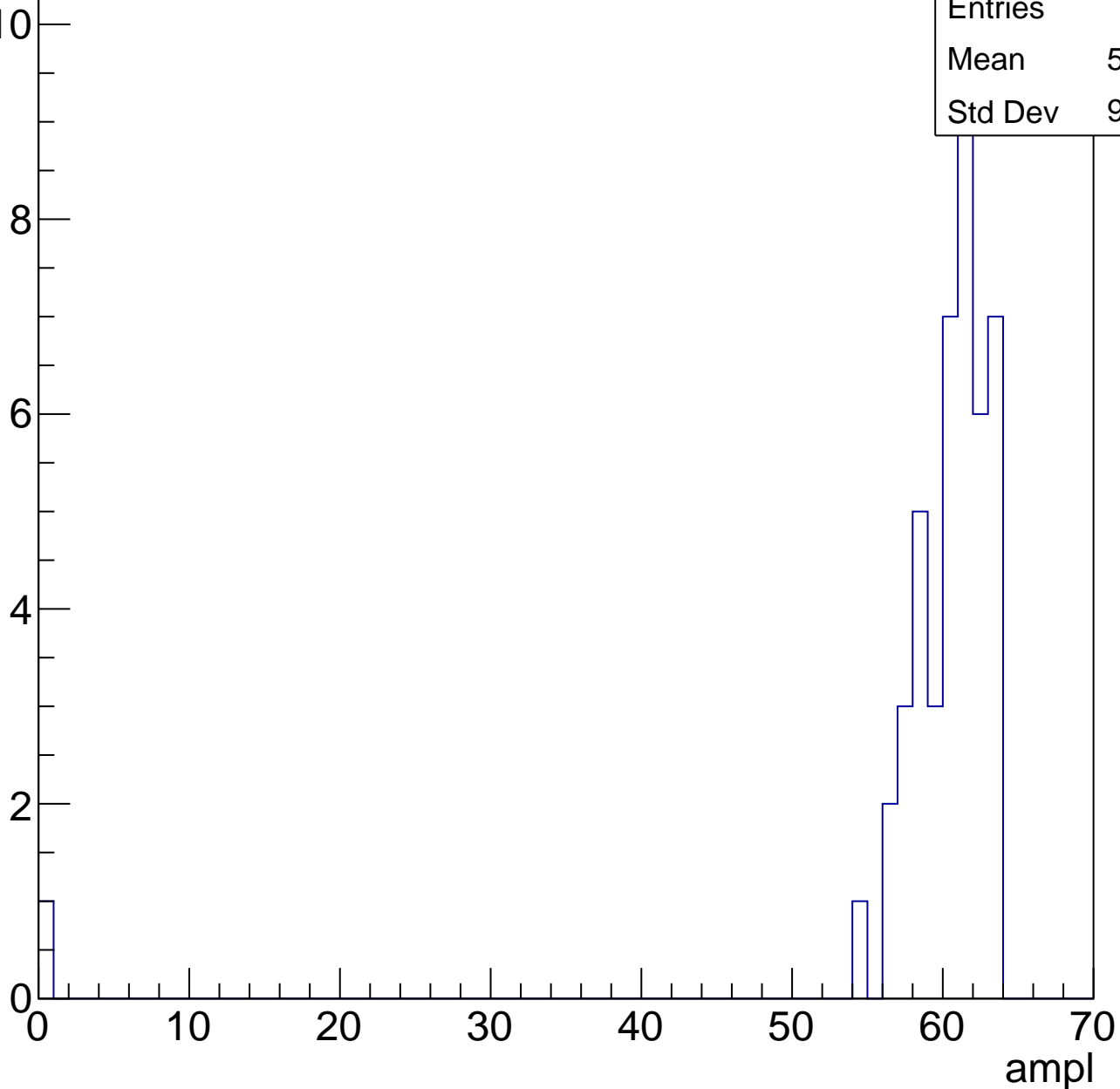


# B1L102S, U20-ch40, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	45
Mean	58.82
Std Dev	9.132



# B1L102S, U20-ch40, adc6

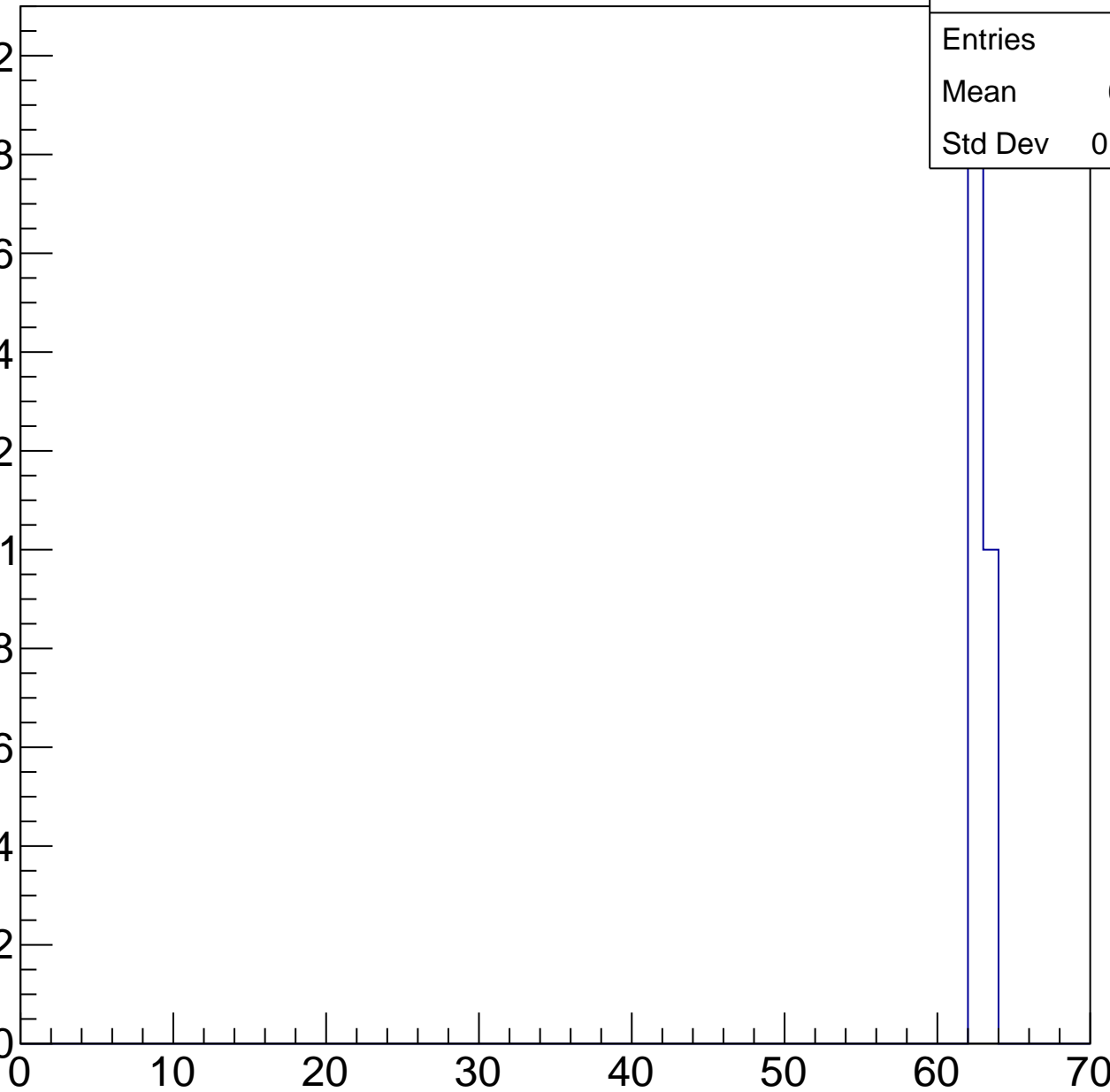
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.33
Std Dev	0.4714

ampl





# B1L102S, U20-ch40, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	63
Std Dev	0

# B1L102S, U20-ch41, adc0

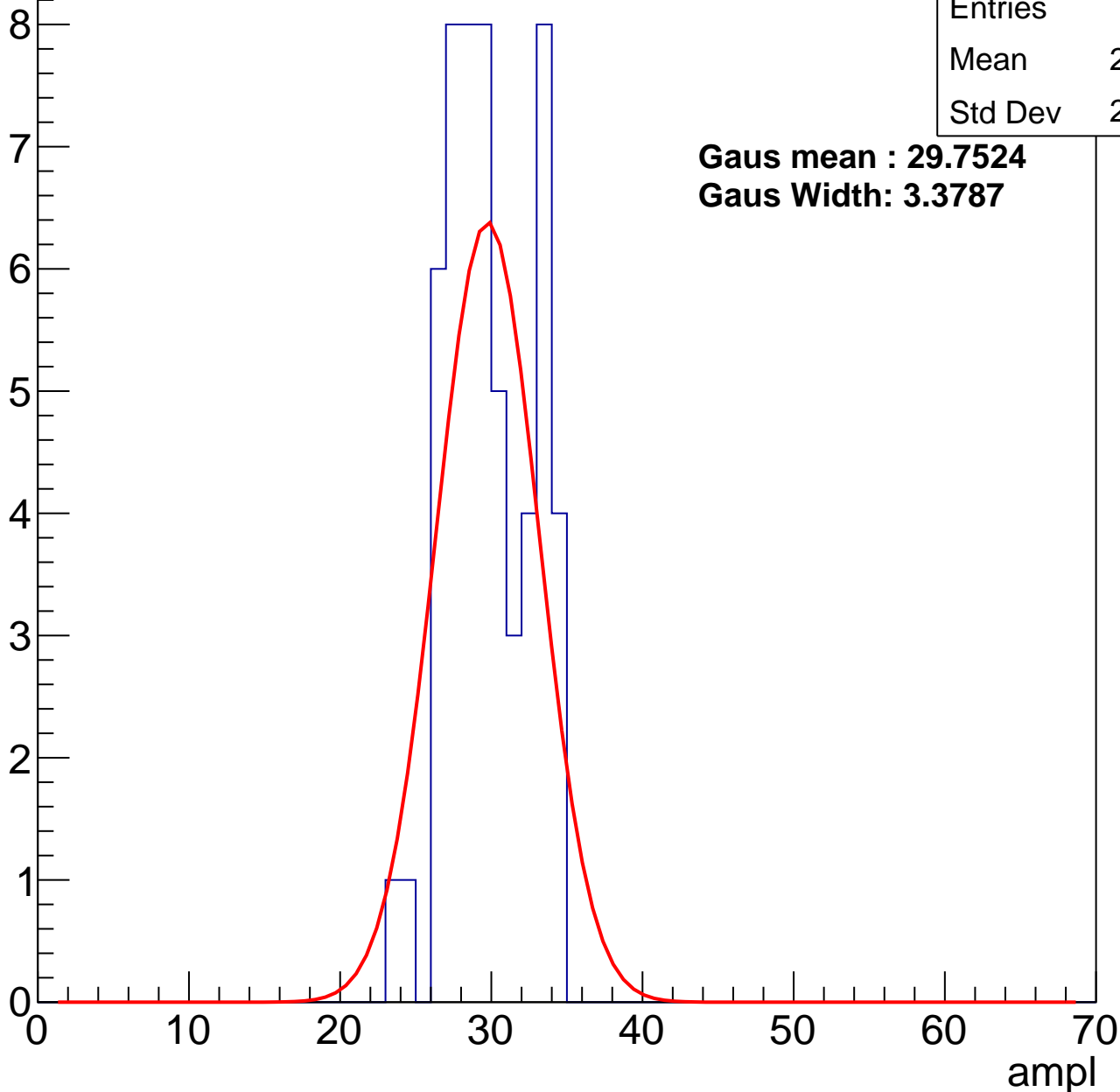
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	29.39
Std Dev	2.762

**Gaus mean : 29.7524**

**Gaus Width: 3.3787**



# B1L102S, U20-ch41, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	90
Mean	36.12
Std Dev	3.841

**Gaus mean : 37.1349**

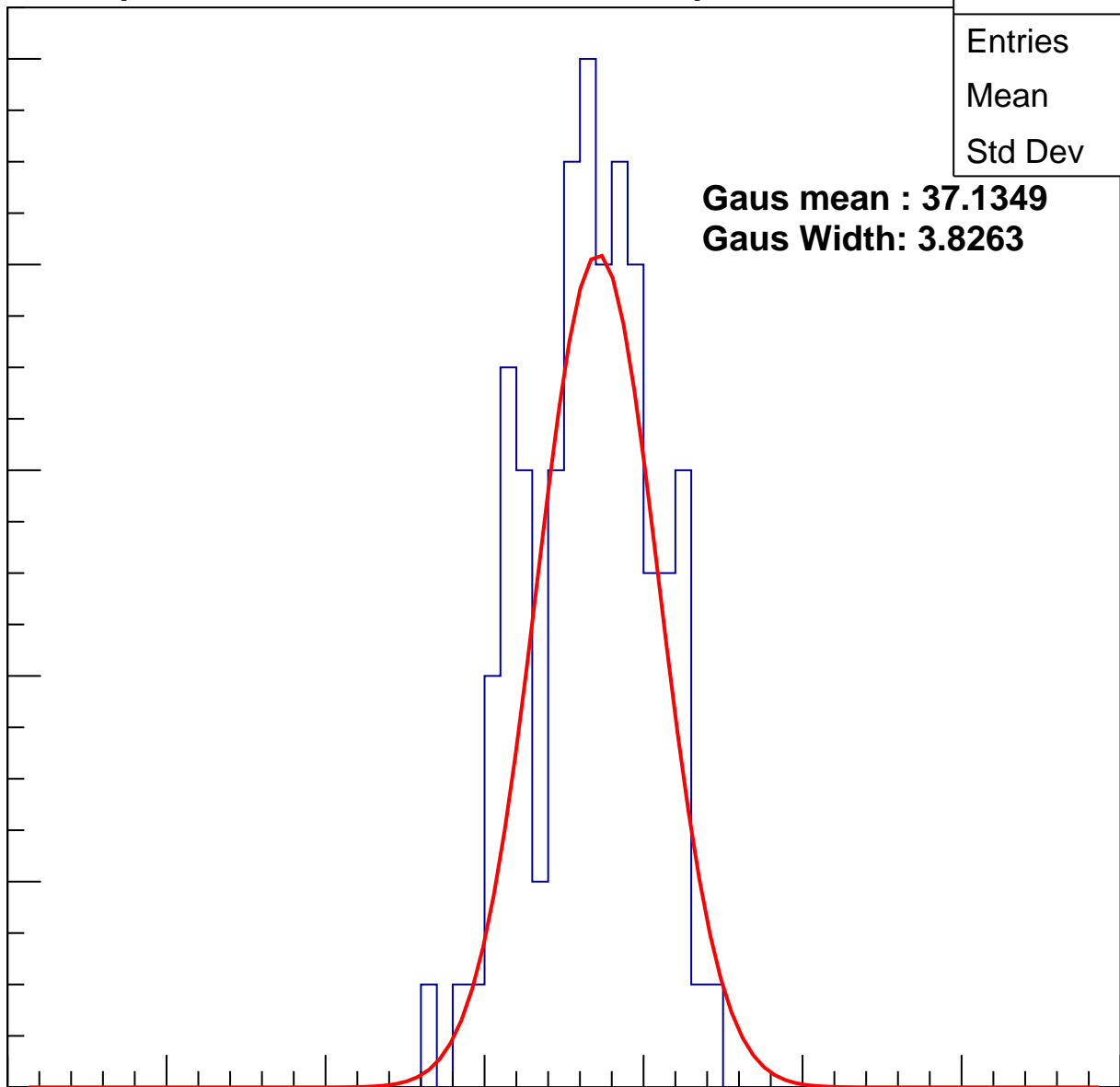
**Gaus Width: 3.8263**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U20-ch41, adc2

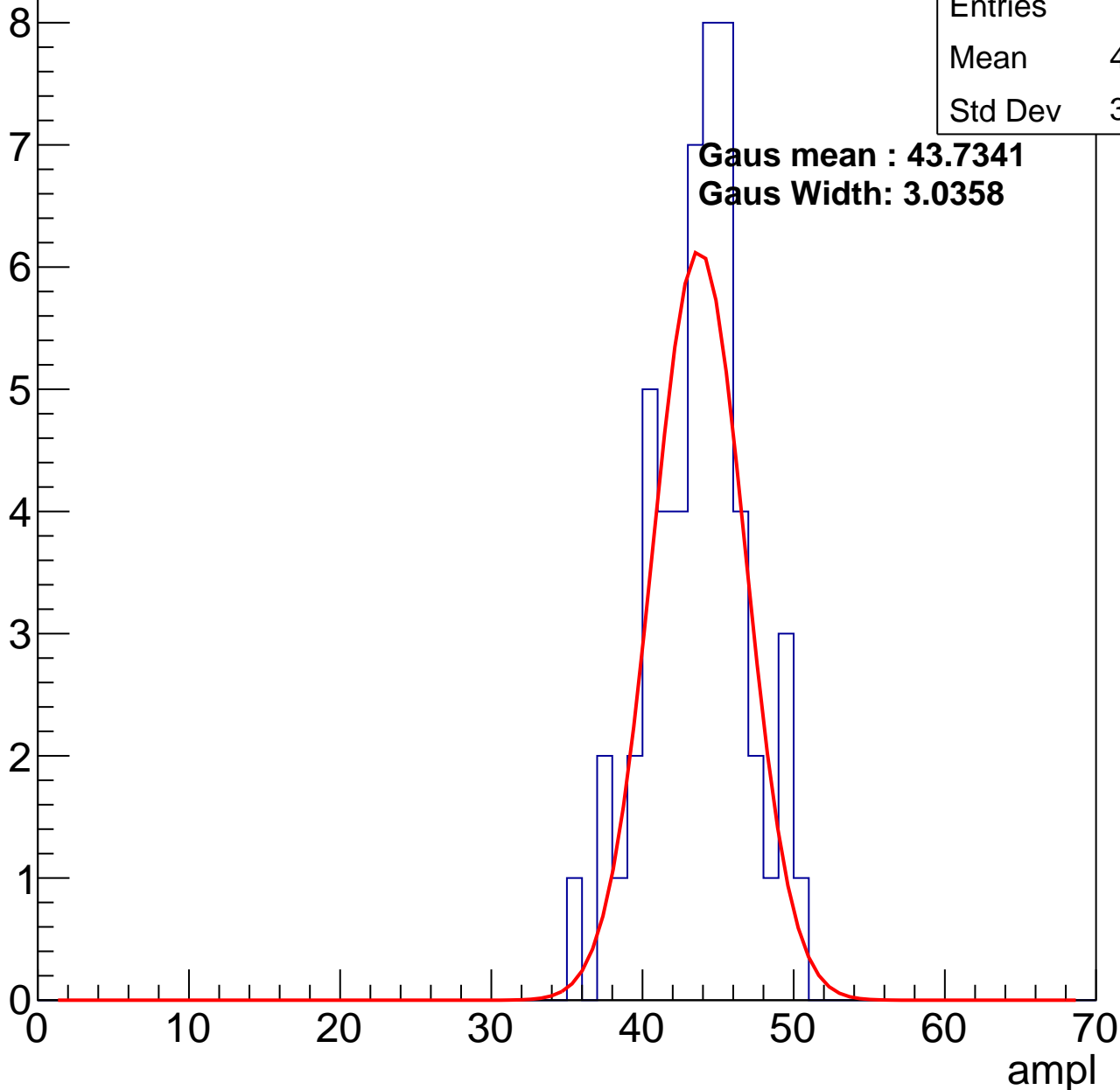
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	43.26
Std Dev	3.205

**Gaus mean : 43.7341**

**Gaus Width: 3.0358**

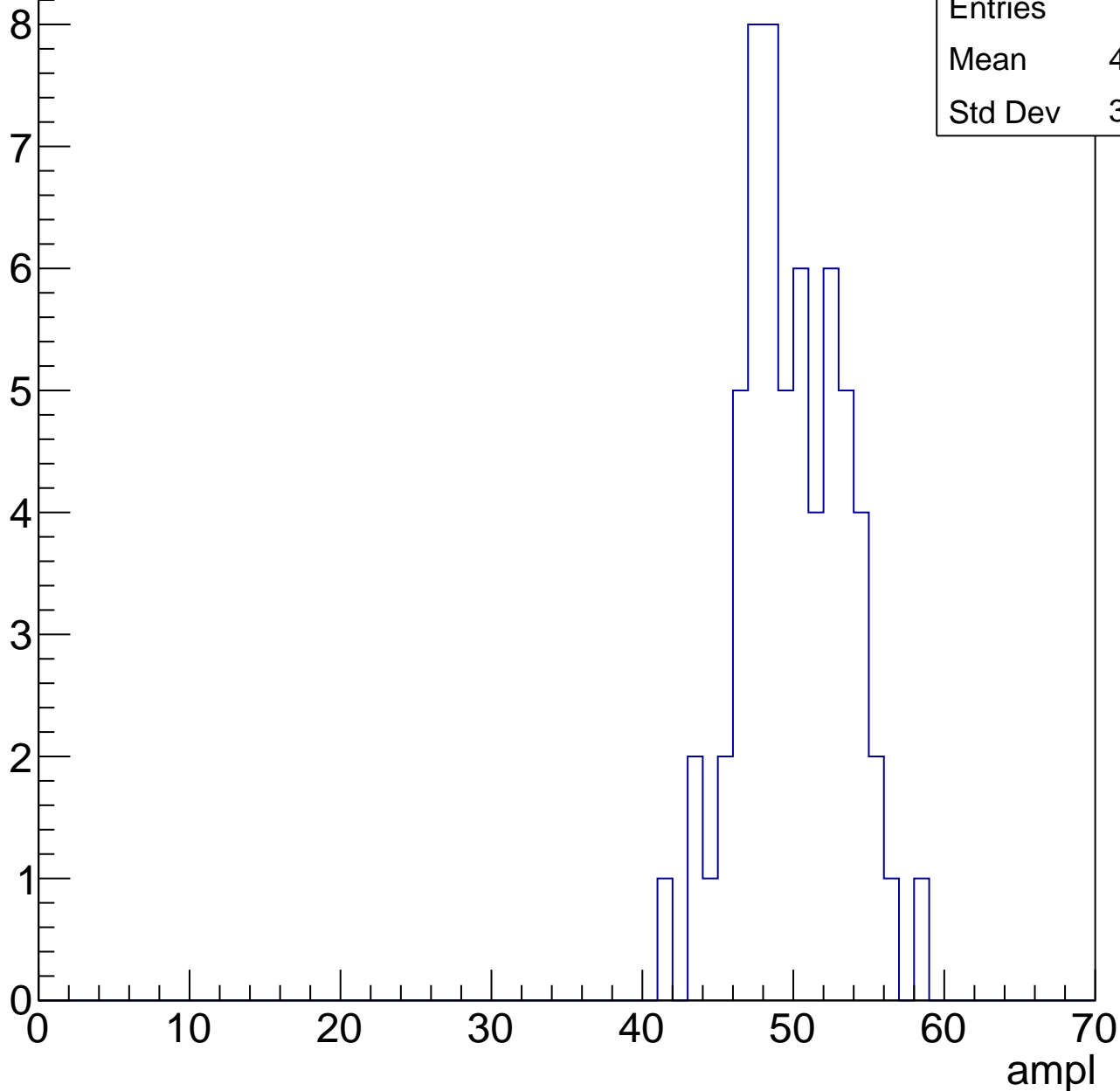


# B1L102S, U20-ch41, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	49.46
Std Dev	3.443

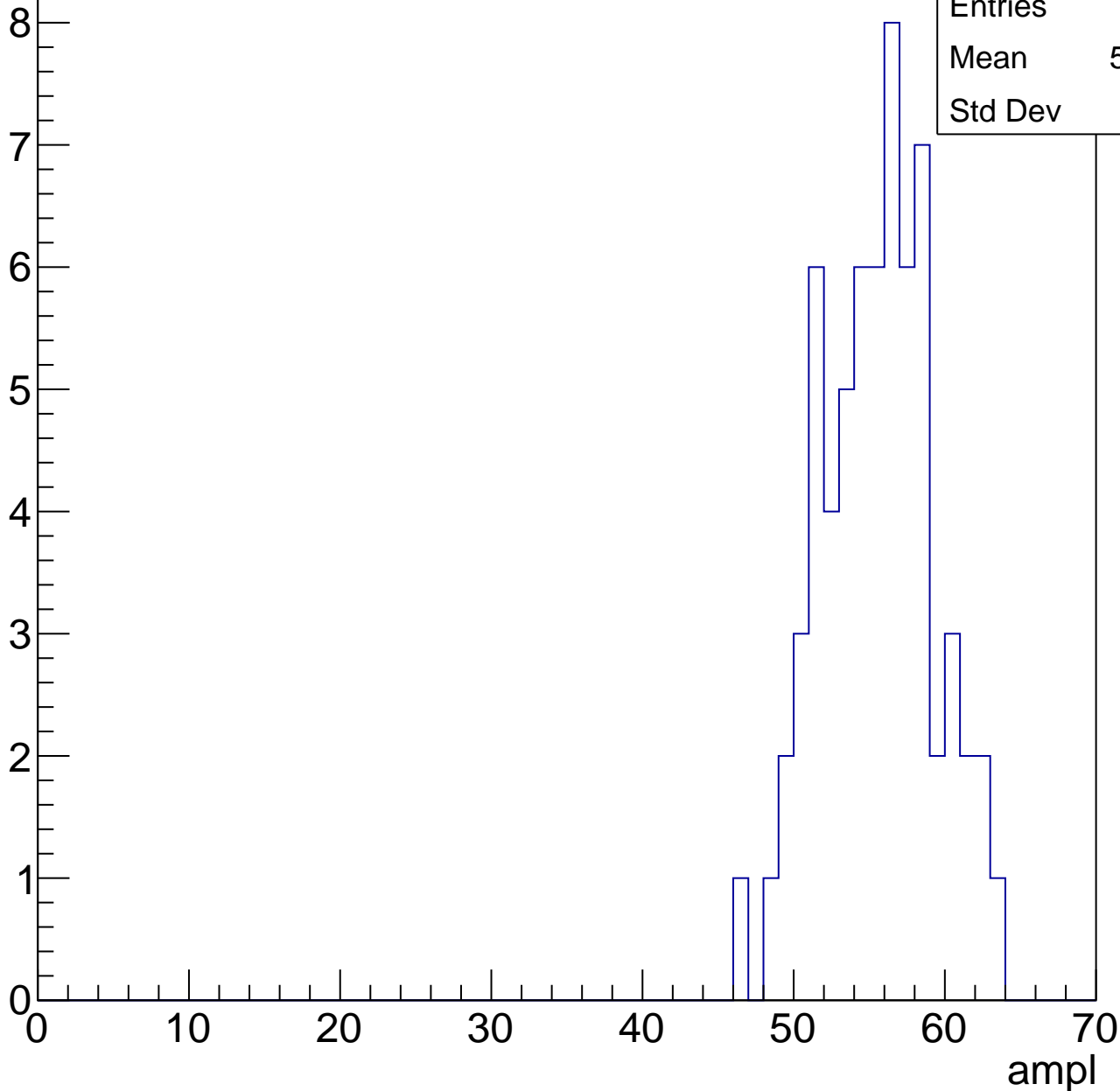


# B1L102S, U20-ch41, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	55.05
Std Dev	3.66



# B1L102S, U20-ch41, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	39
Mean	58.21
Std Dev	9.68

ampl

0

10

20

30

40

50

60

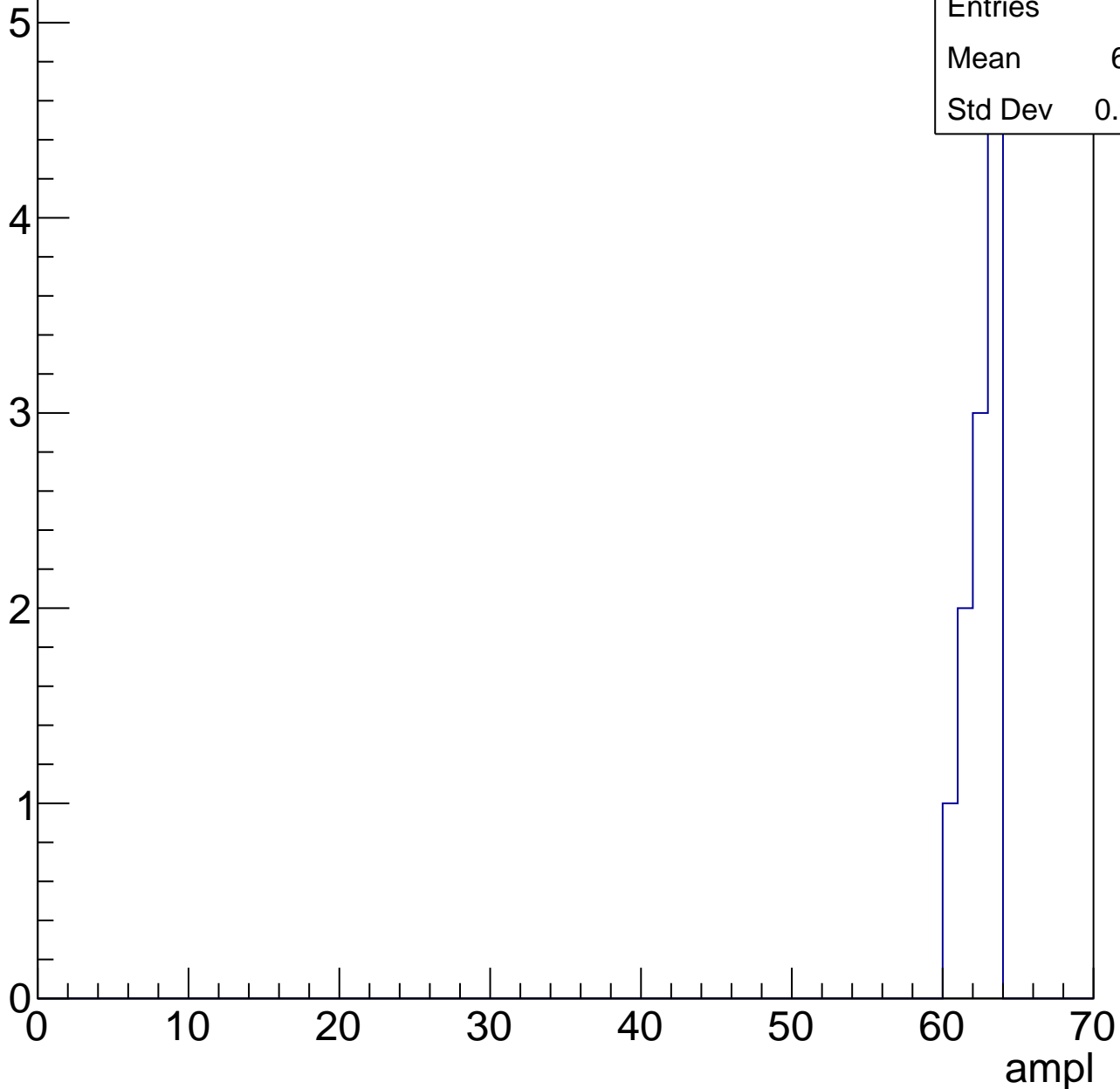
70

# B1L102S, U20-ch41, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	11
Mean	62.09
Std Dev	0.9959





# B1L102S, U20-ch41, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch42, adc0

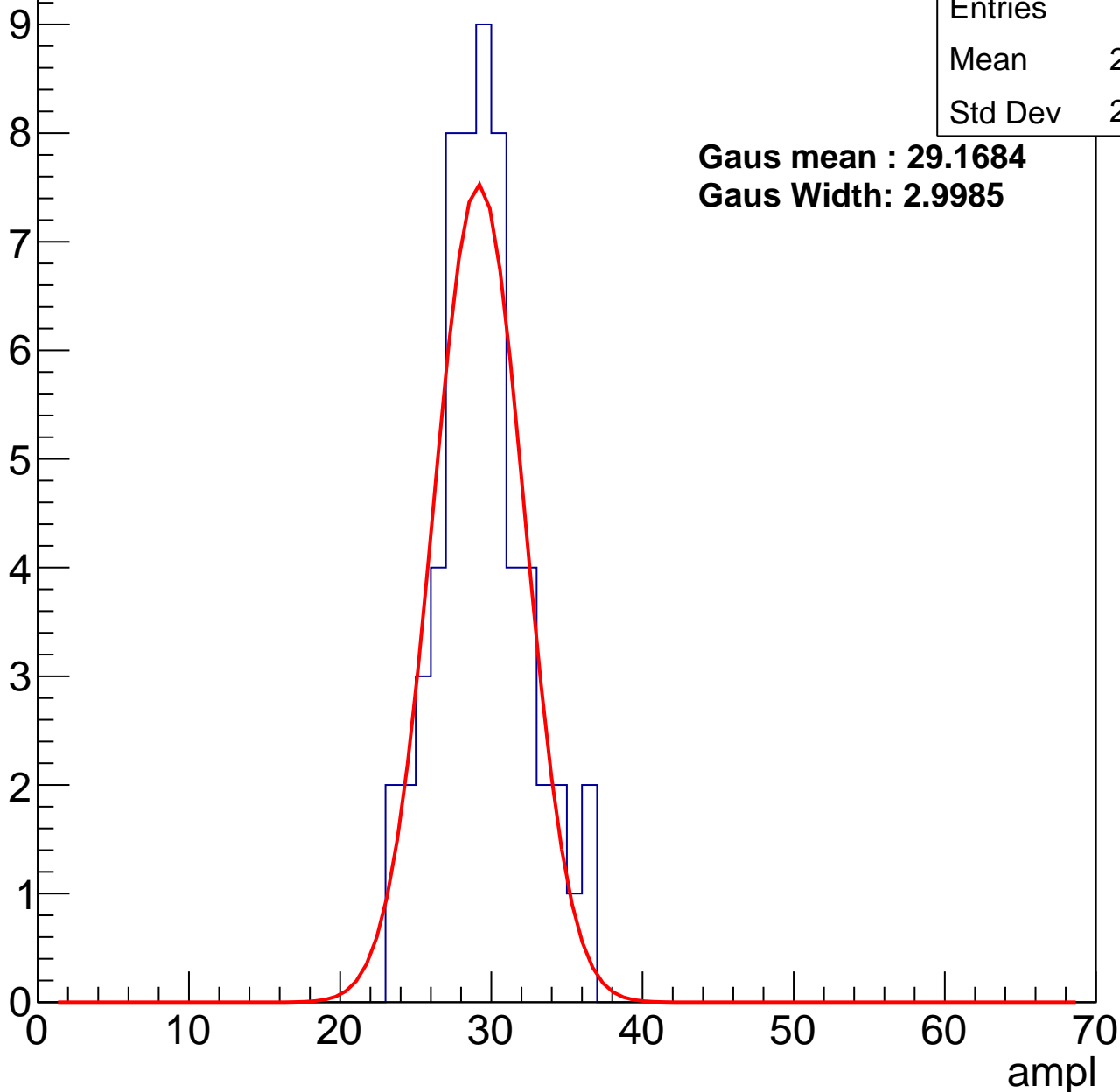
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	28.93
Std Dev	2.974

**Gaus mean : 29.1684**

**Gaus Width: 2.9985**



# B1L102S, U20-ch42, adc1

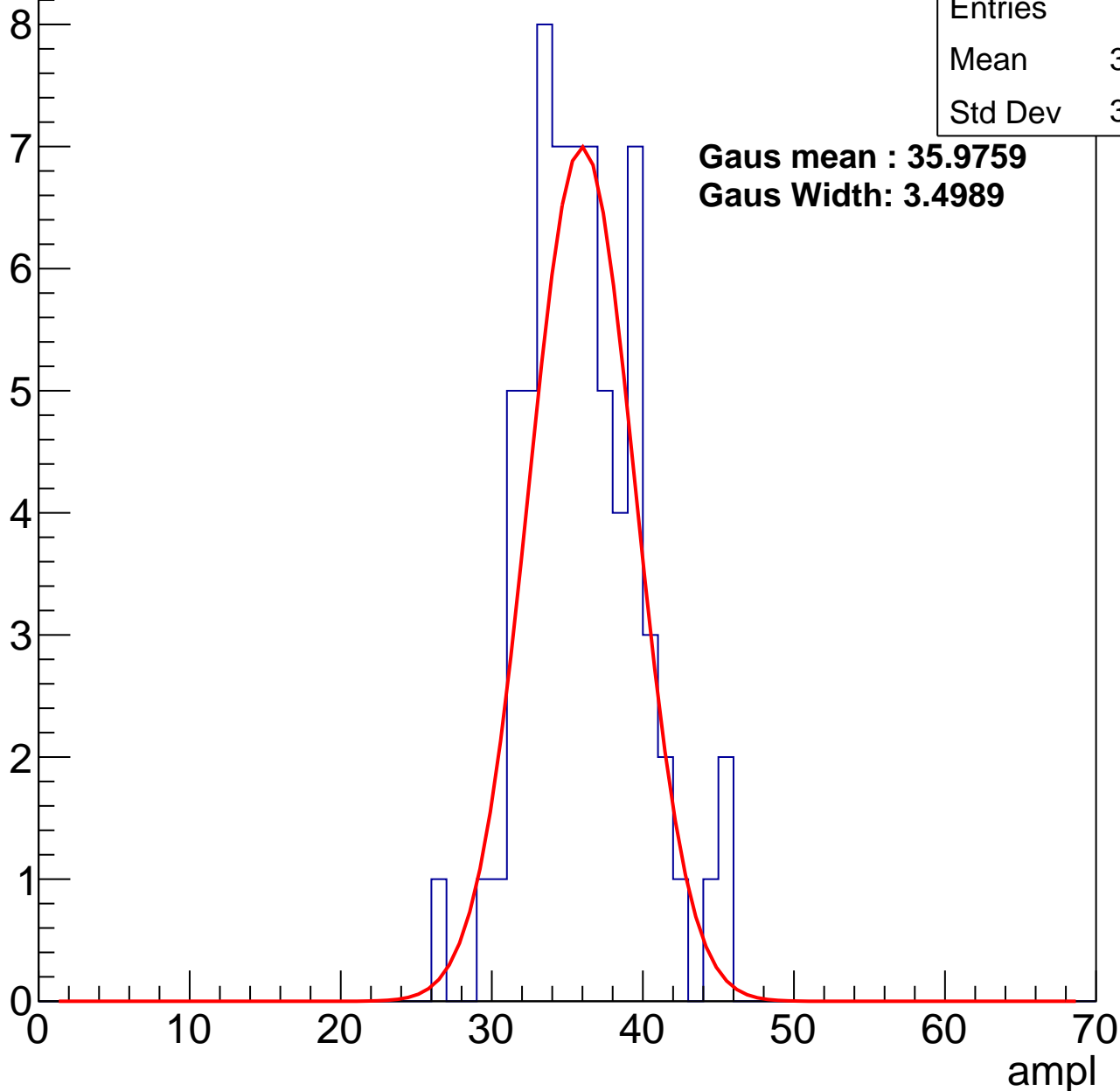
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	35.63
Std Dev	3.729

**Gaus mean : 35.9759**

**Gaus Width: 3.4989**



# B1L102S, U20-ch42, adc2

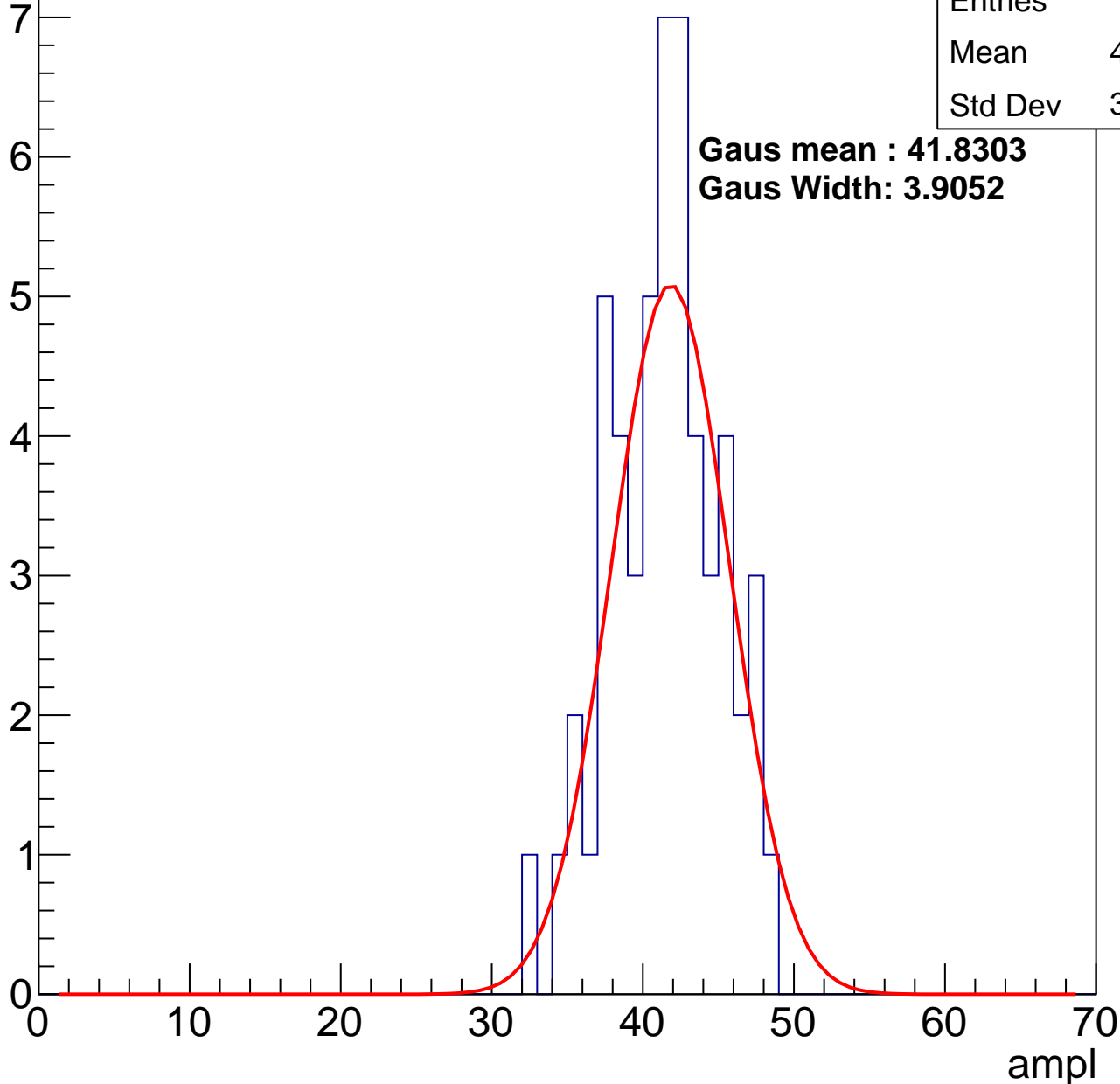
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	40.98
Std Dev	3.585

**Gaus mean : 41.8303**

**Gaus Width: 3.9052**

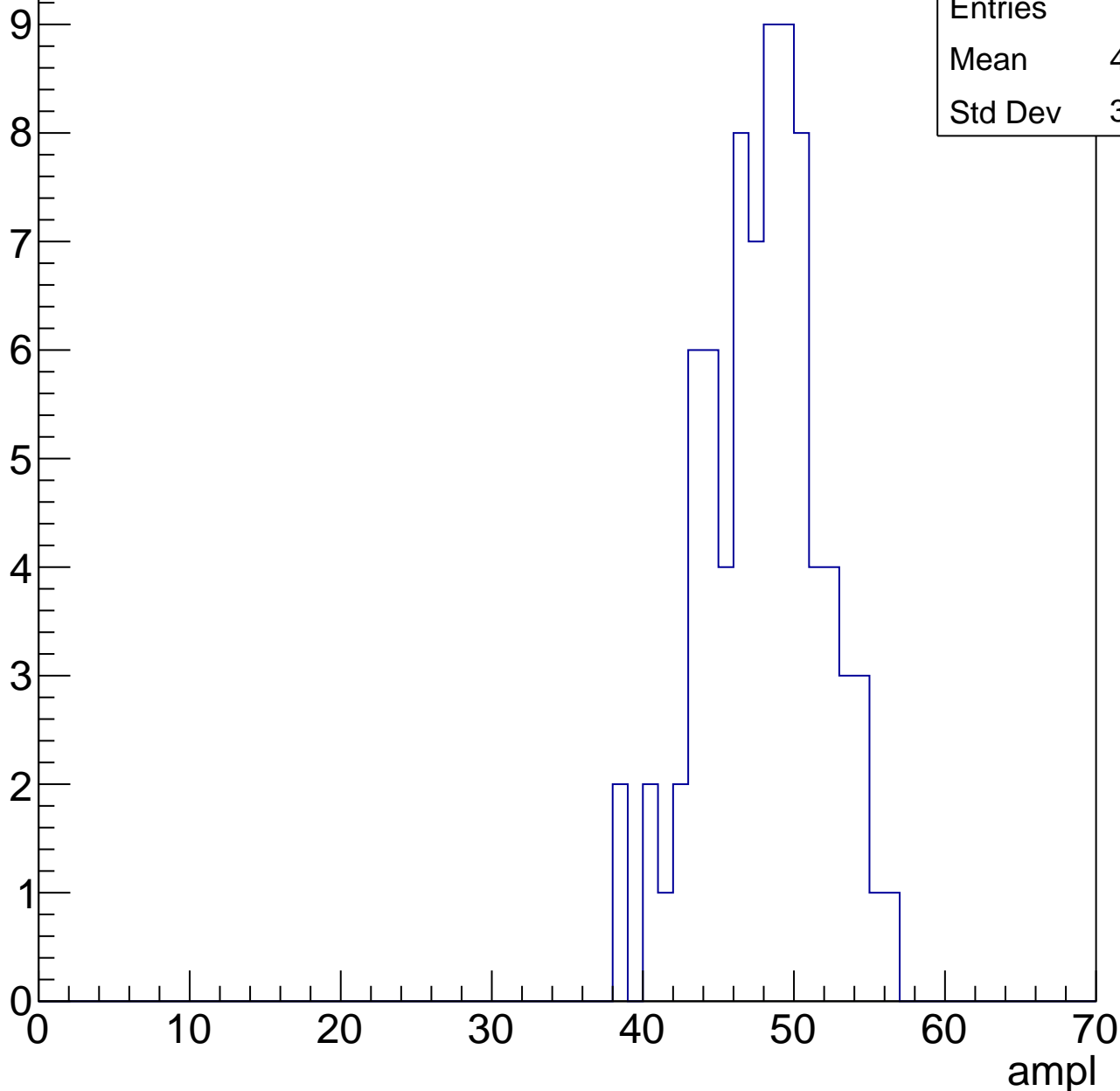


# B1L102S, U20-ch42, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

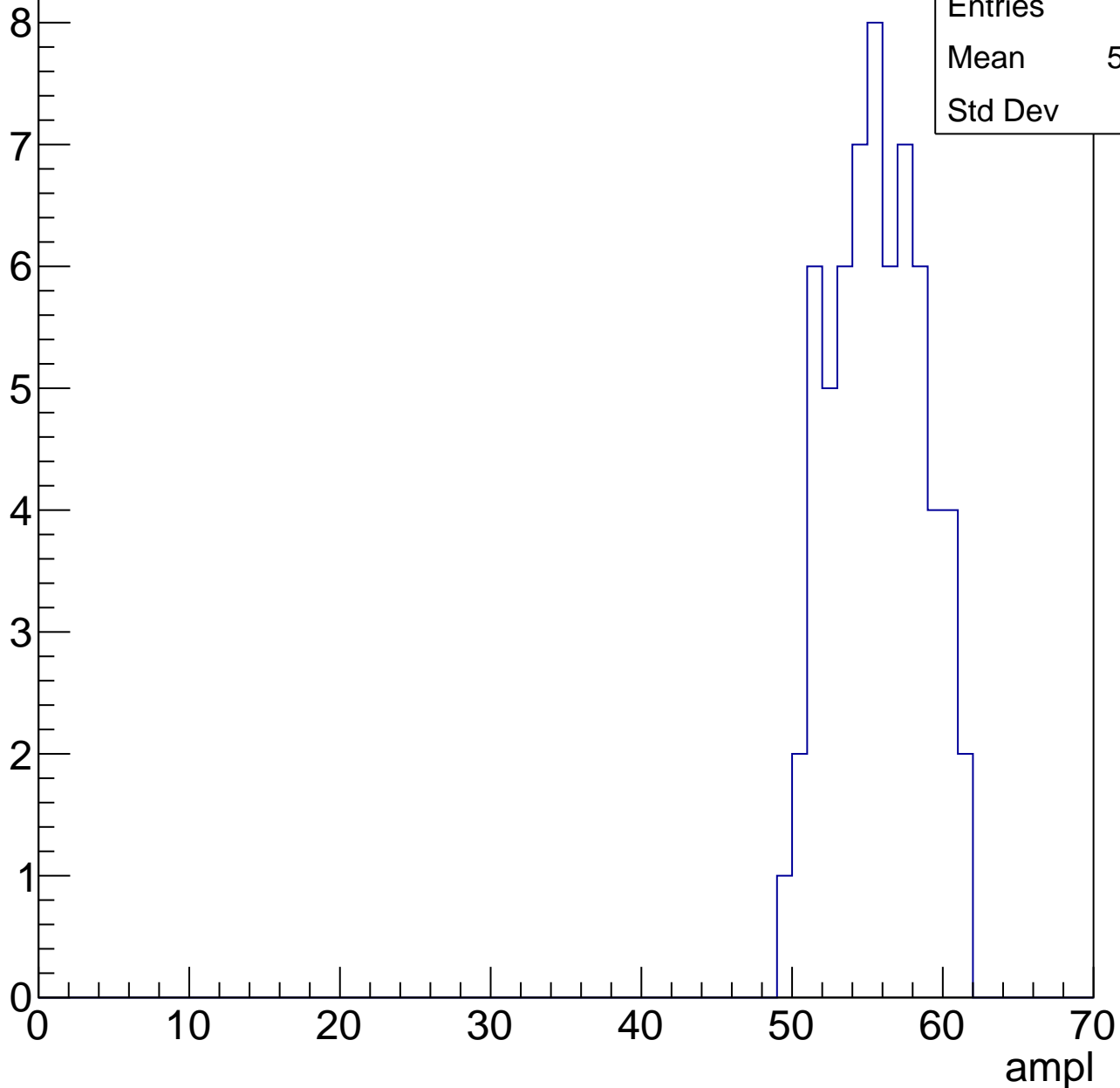
Entries	80
Mean	47.46
Std Dev	3.847



# B1L102S, U20-ch42, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



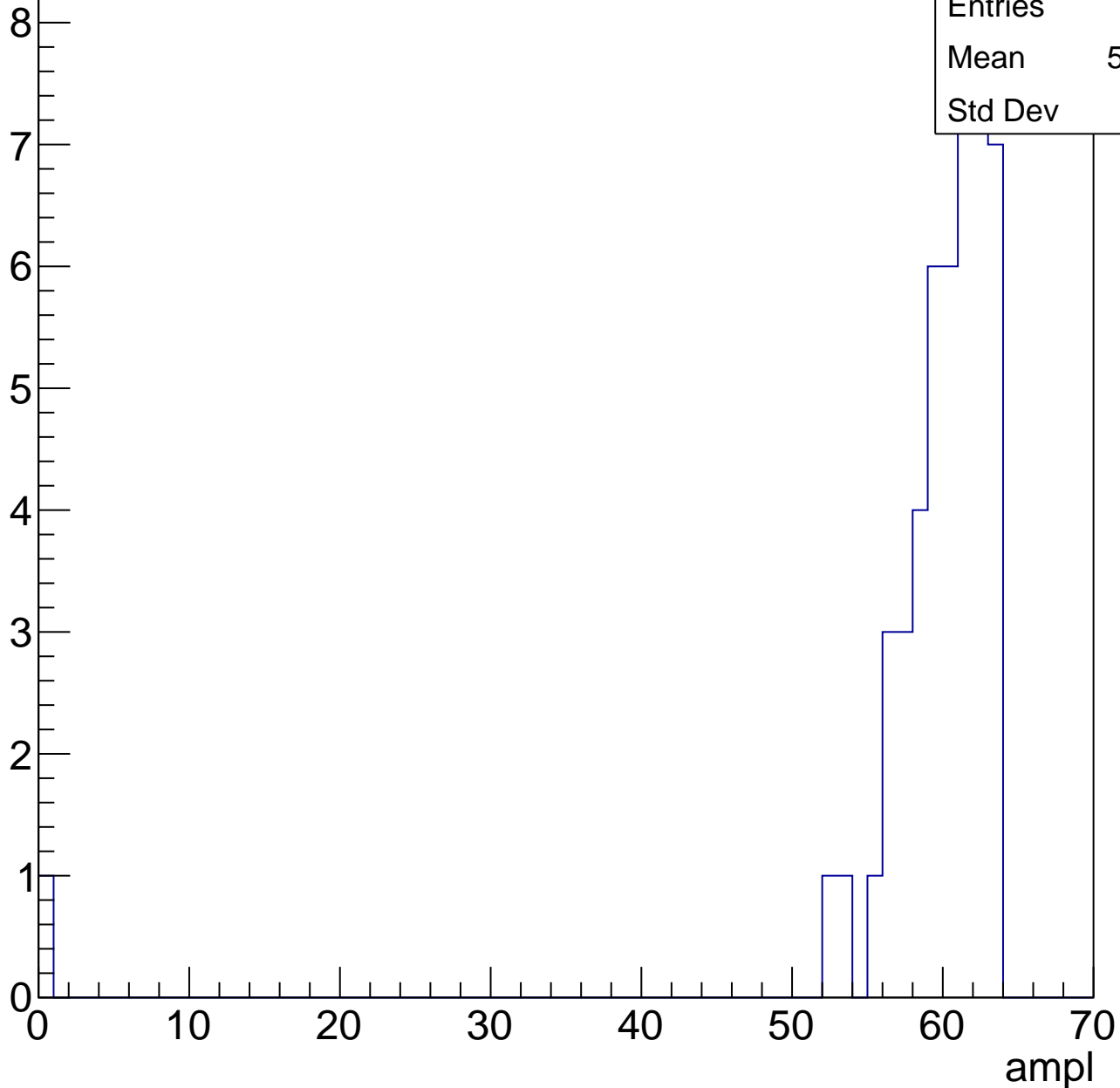
Entries	64
Mean	55.19
Std Dev	3.01

# B1L102S, U20-ch42, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	58.57
Std Dev	8.85



# B1L102S, U20-ch42, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U20-ch42, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	21
Std Dev	0

ampl

# B1L102S, U20-ch43, adc0

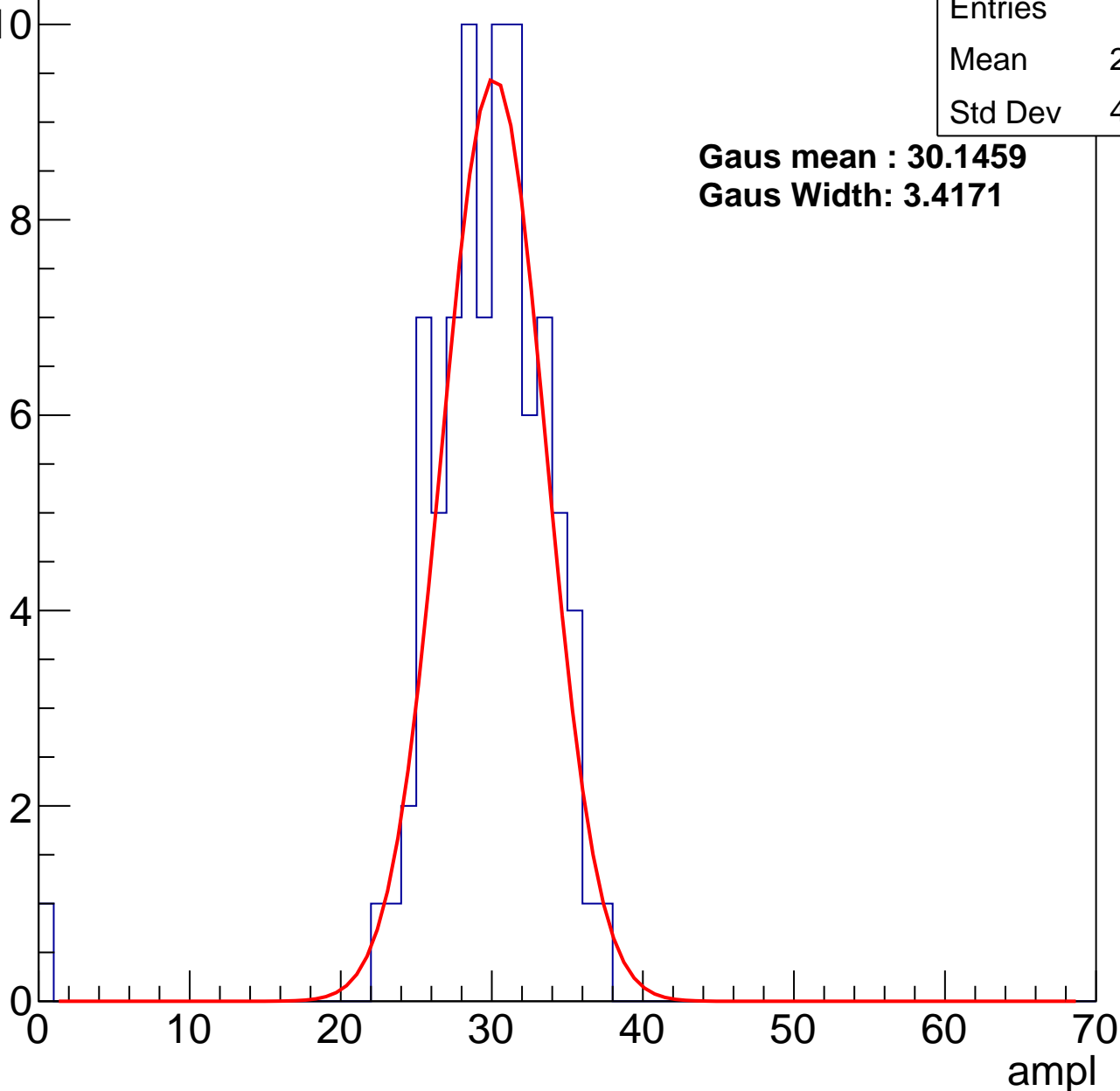
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	85
Mean	29.25
Std Dev	4.555

**Gaus mean : 30.1459**

**Gaus Width: 3.4171**



# B1L102S, U20-ch43, adc1

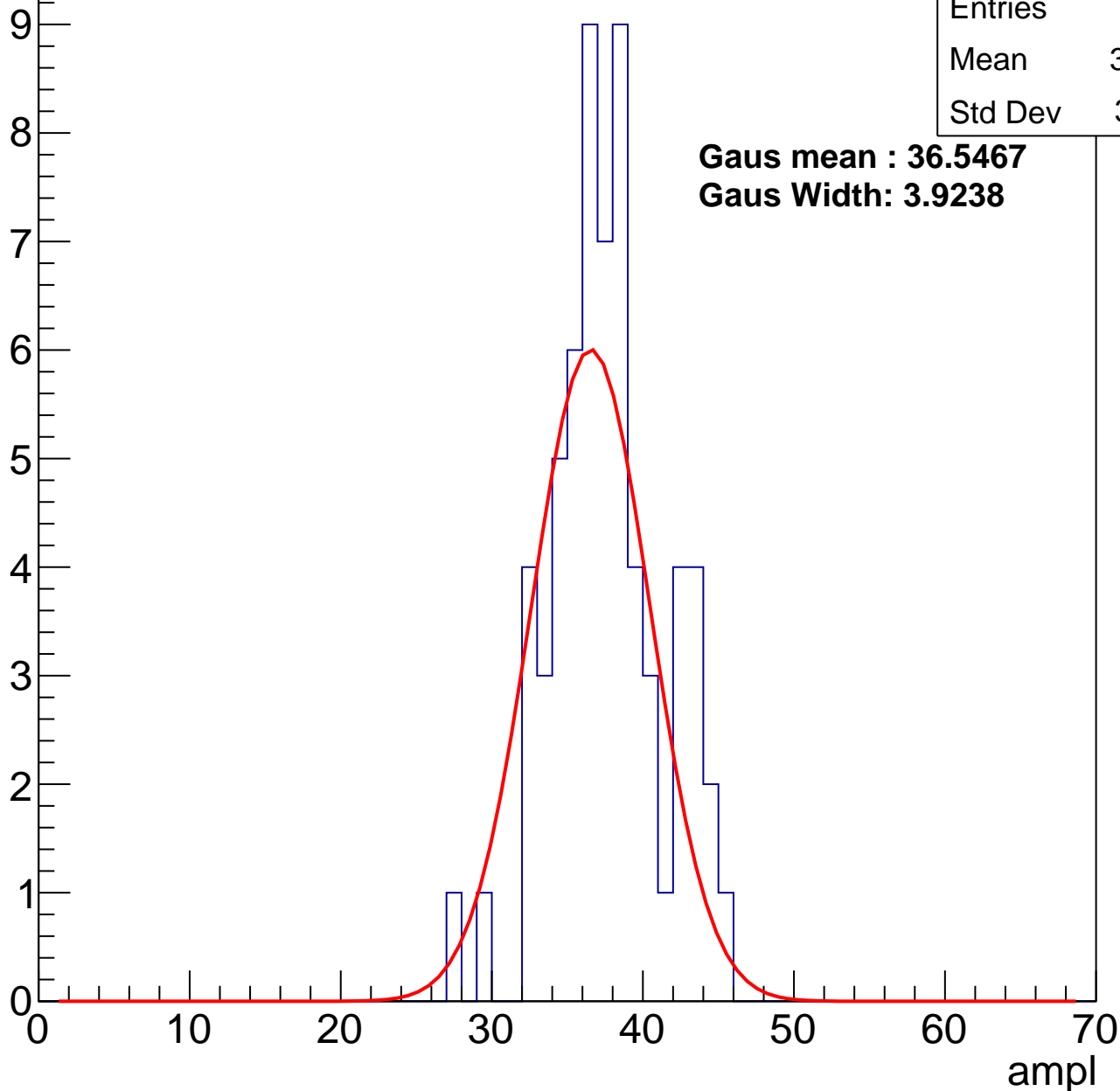
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	37.16
Std Dev	3.671

**Gaus mean : 36.5467**

**Gaus Width: 3.9238**



# B1L102S, U20-ch43, adc2

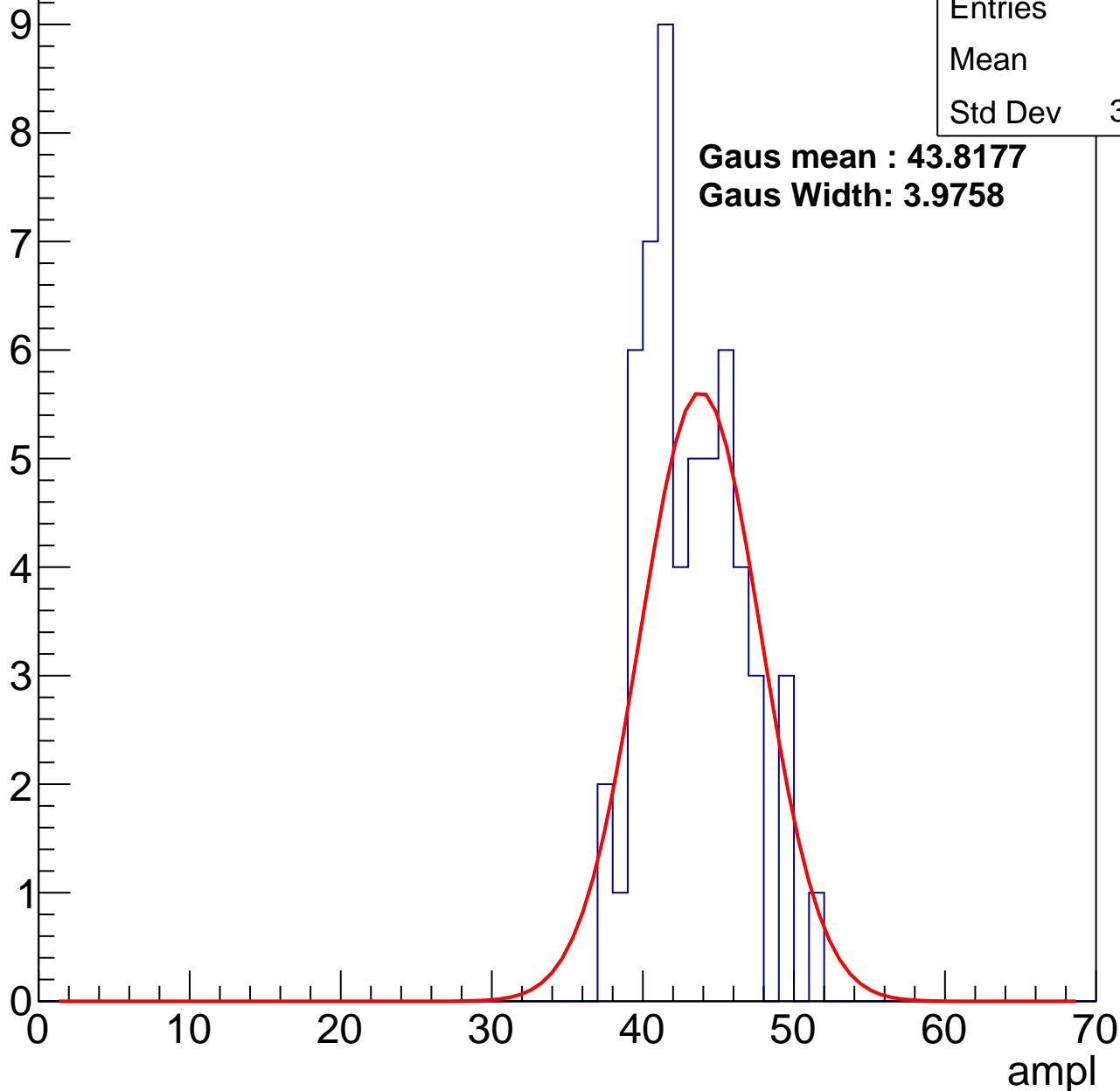
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	42.7
Std Dev	3.207

**Gaus mean : 43.8177**

**Gaus Width: 3.9758**

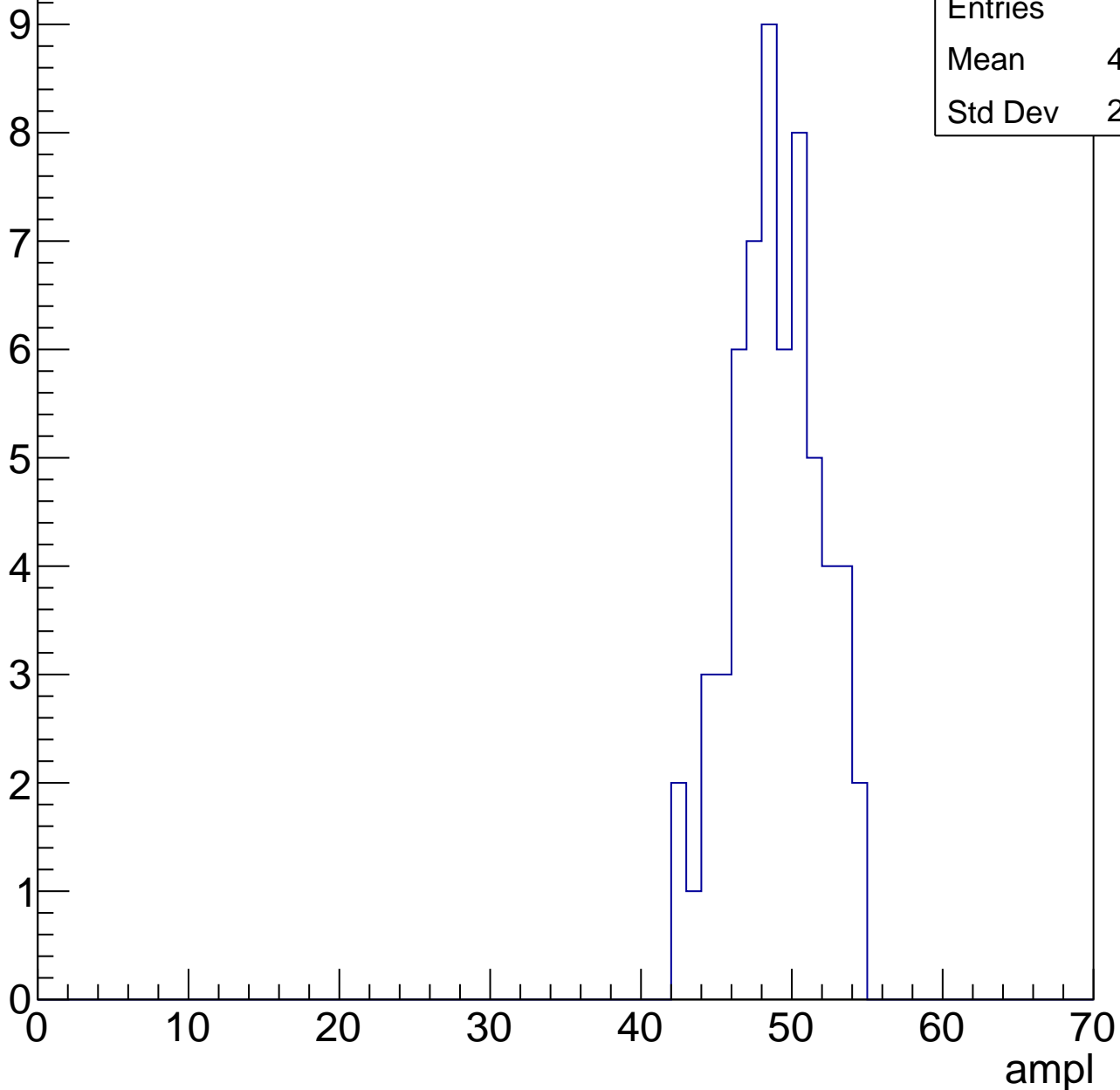


# B1L102S, U20-ch43, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	48.47
Std Dev	2.912

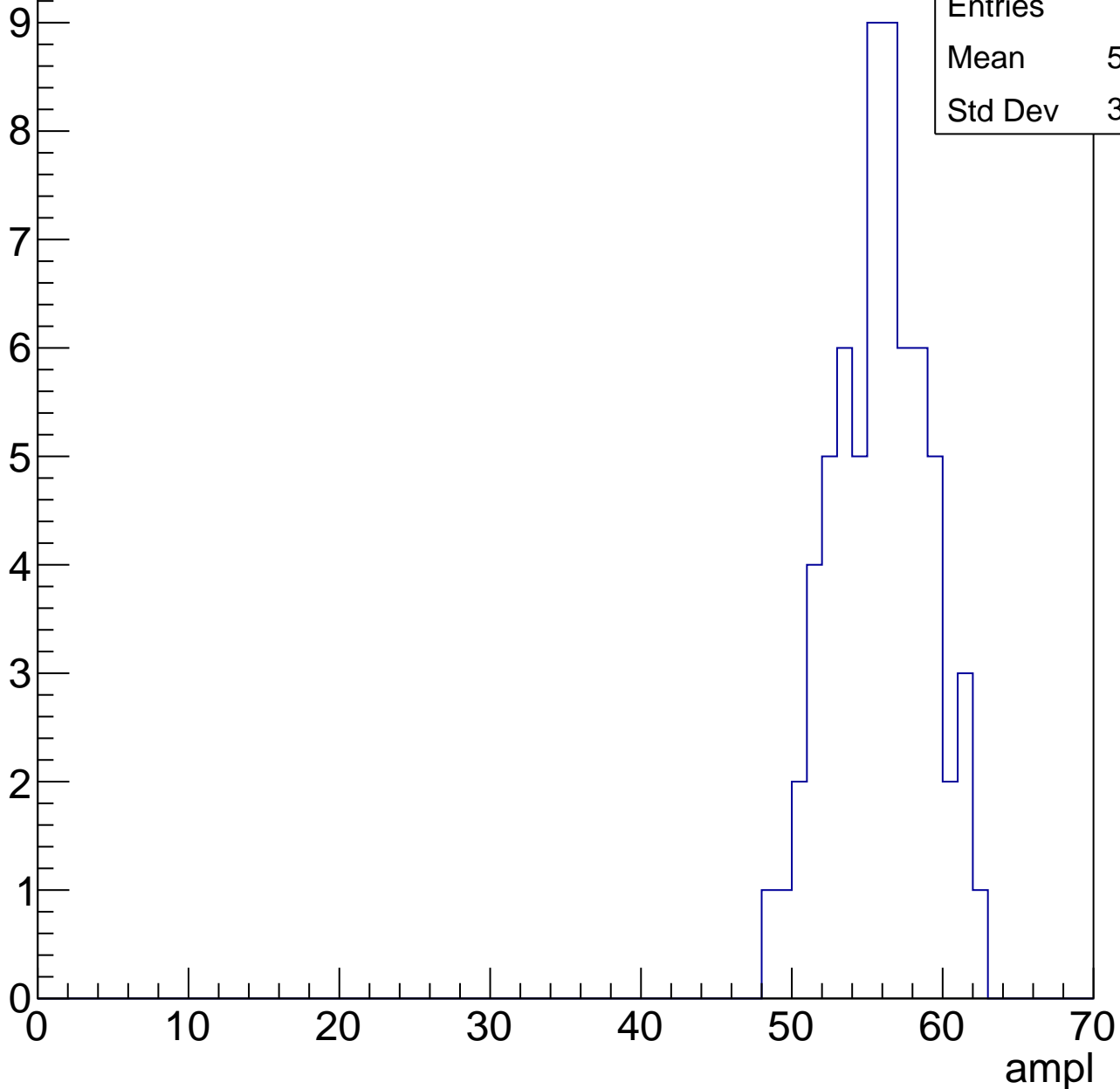


# B1L102S, U20-ch43, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	55.35
Std Dev	3.135

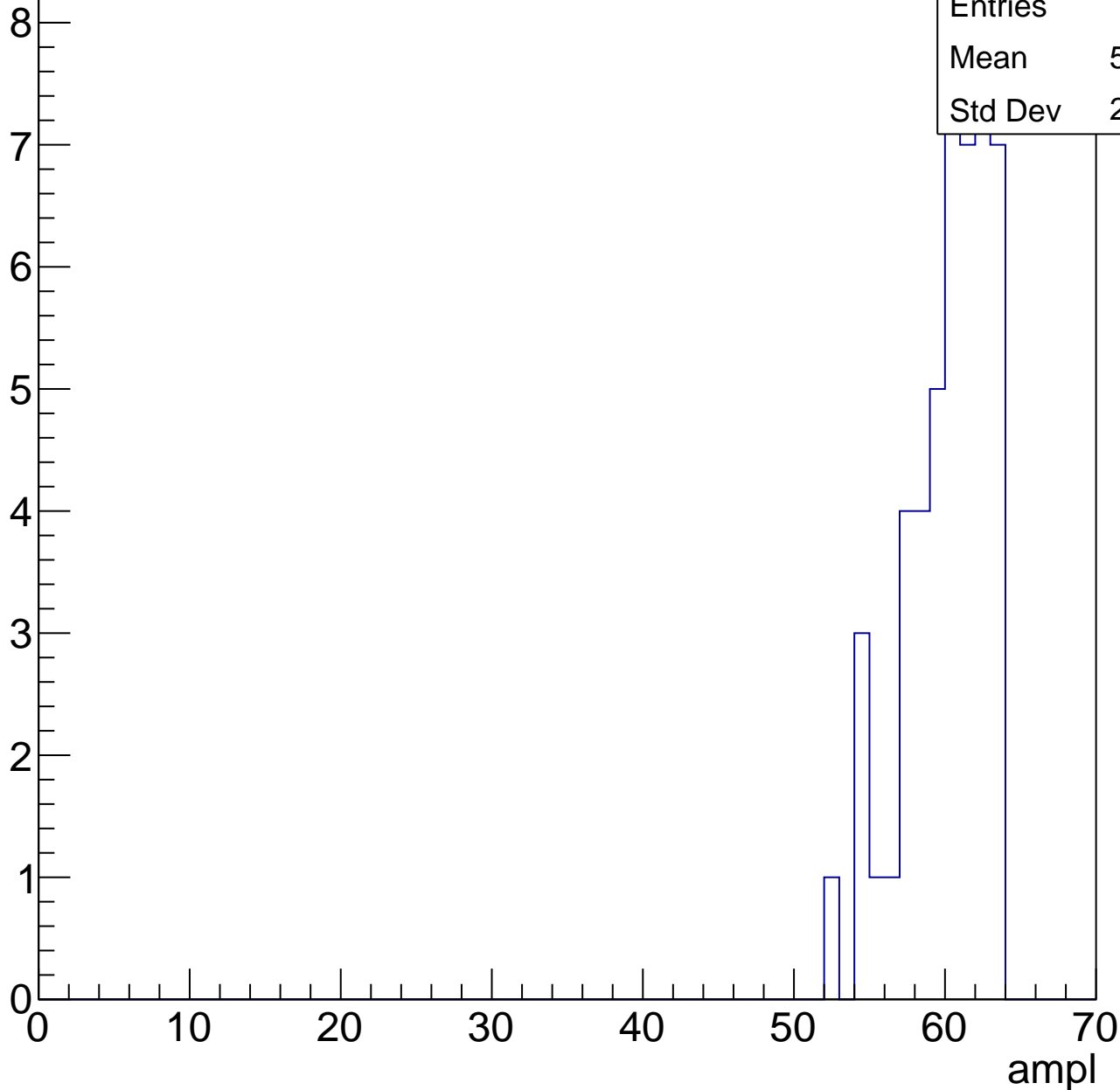


# B1L102S, U20-ch43, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	59.67
Std Dev	2.736



# B1L102S, U20-ch43, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U20-ch43, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch44, adc0

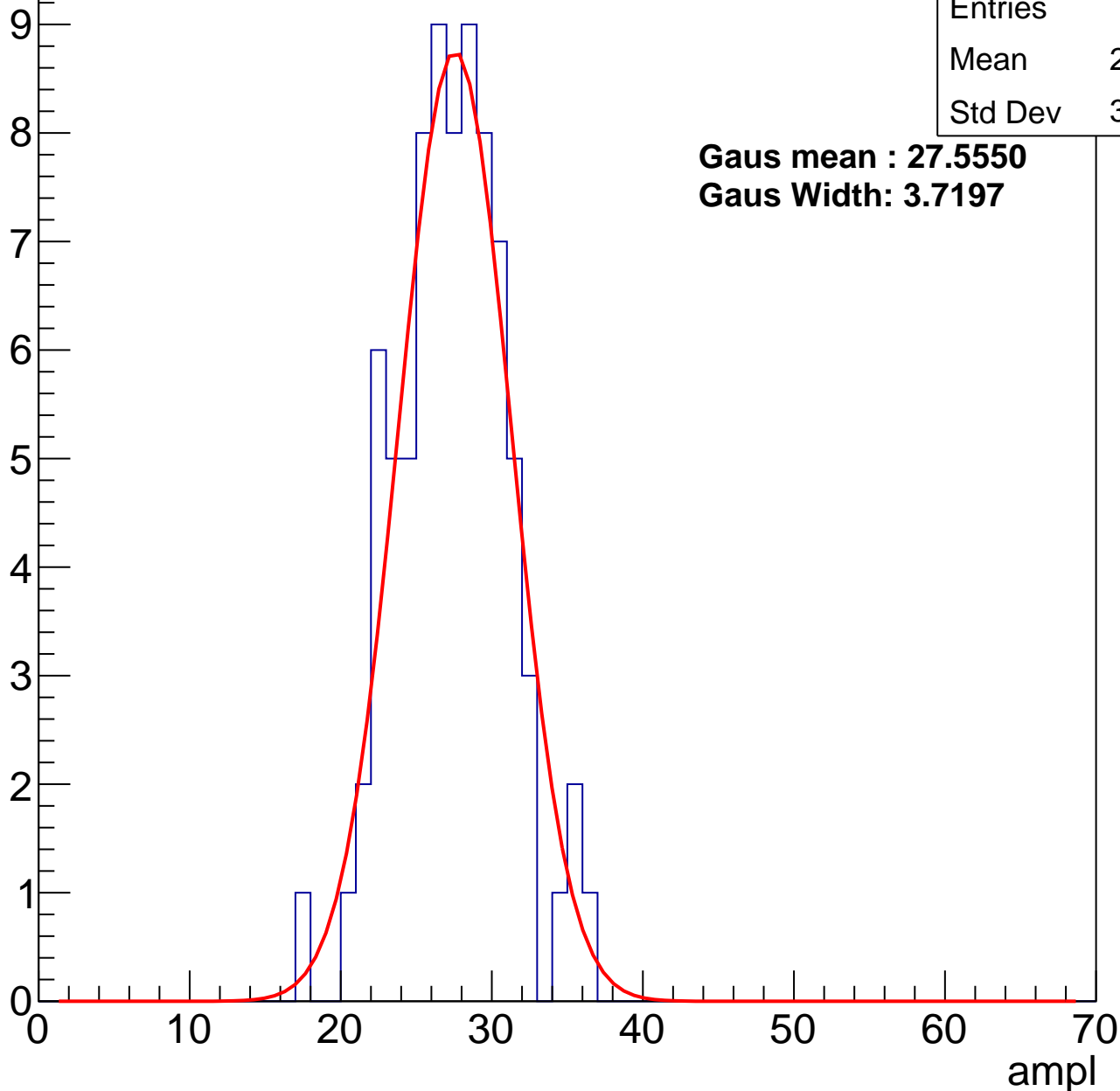
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	81
Mean	26.93
Std Dev	3.607

**Gaus mean : 27.5550**

**Gaus Width: 3.7197**



# B1L102S, U20-ch44, adc1

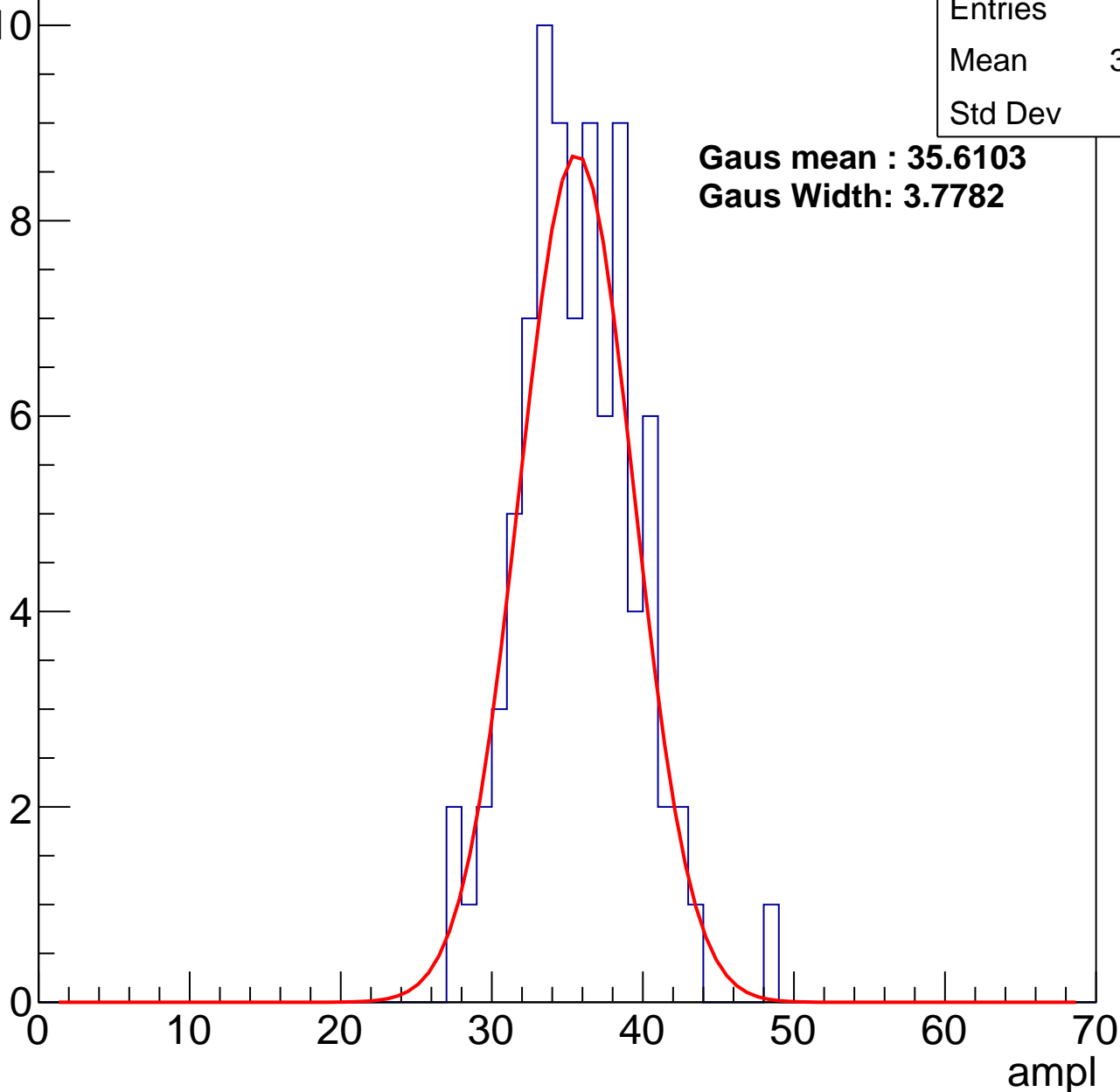
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	86
Mean	35.24
Std Dev	3.8

**Gaus mean : 35.6103**

**Gaus Width: 3.7782**



# B1L102S, U20-ch44, adc2

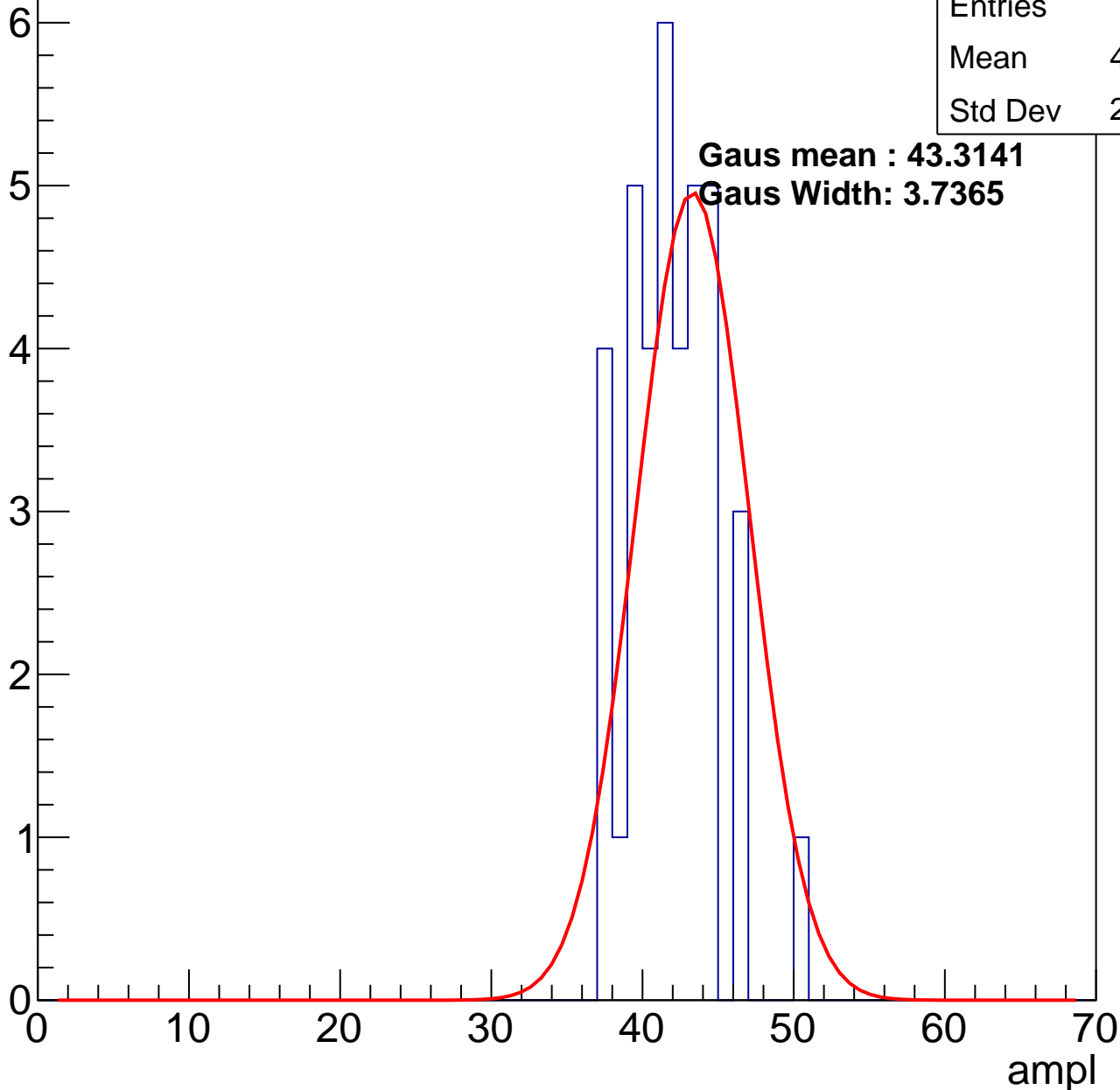
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	38
Mean	41.53
Std Dev	2.863

**Gaus mean : 43.3141**

**Gaus Width: 3.7365**

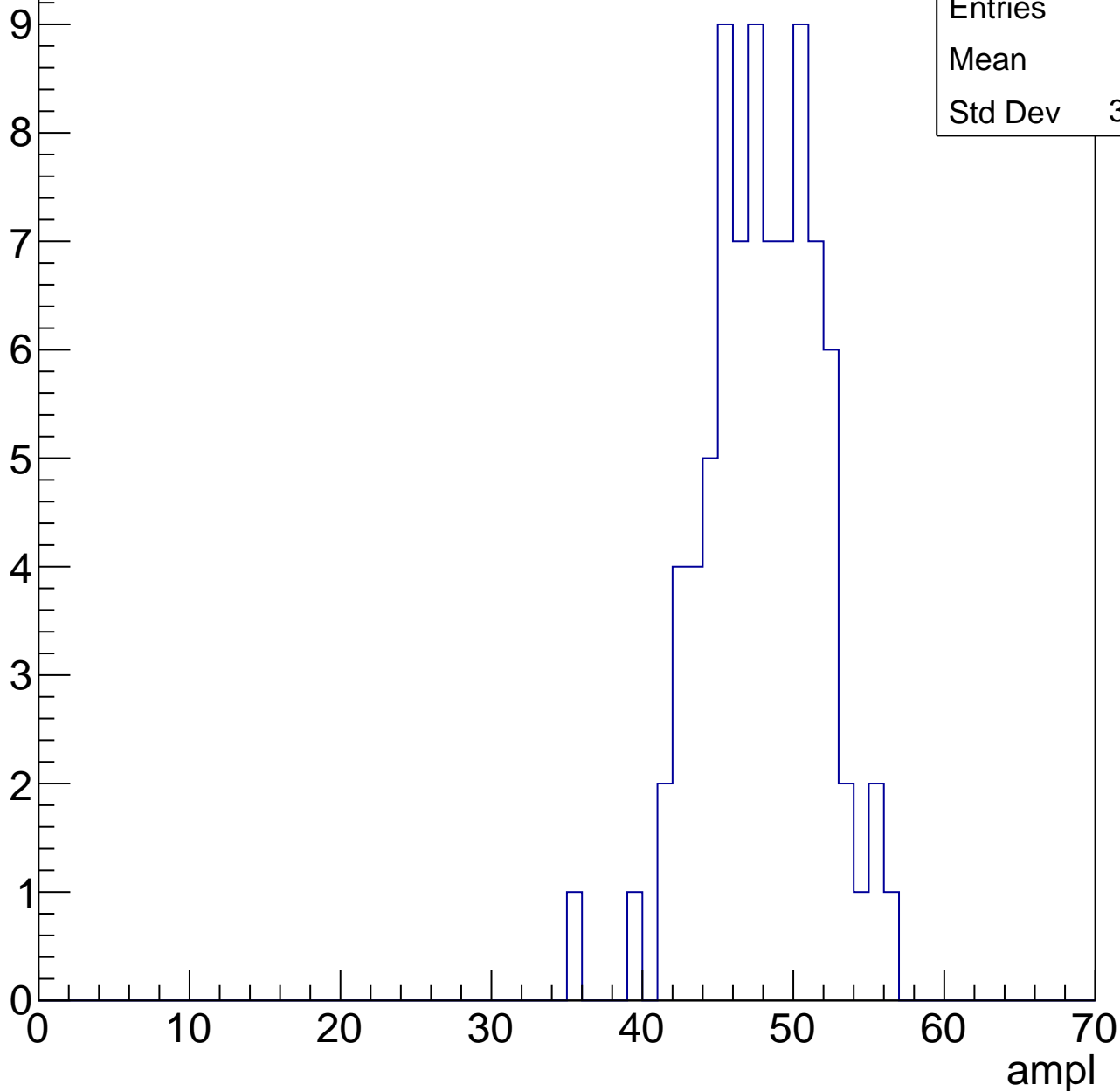


# B1L102S, U20-ch44, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	84
Mean	47.5
Std Dev	3.809

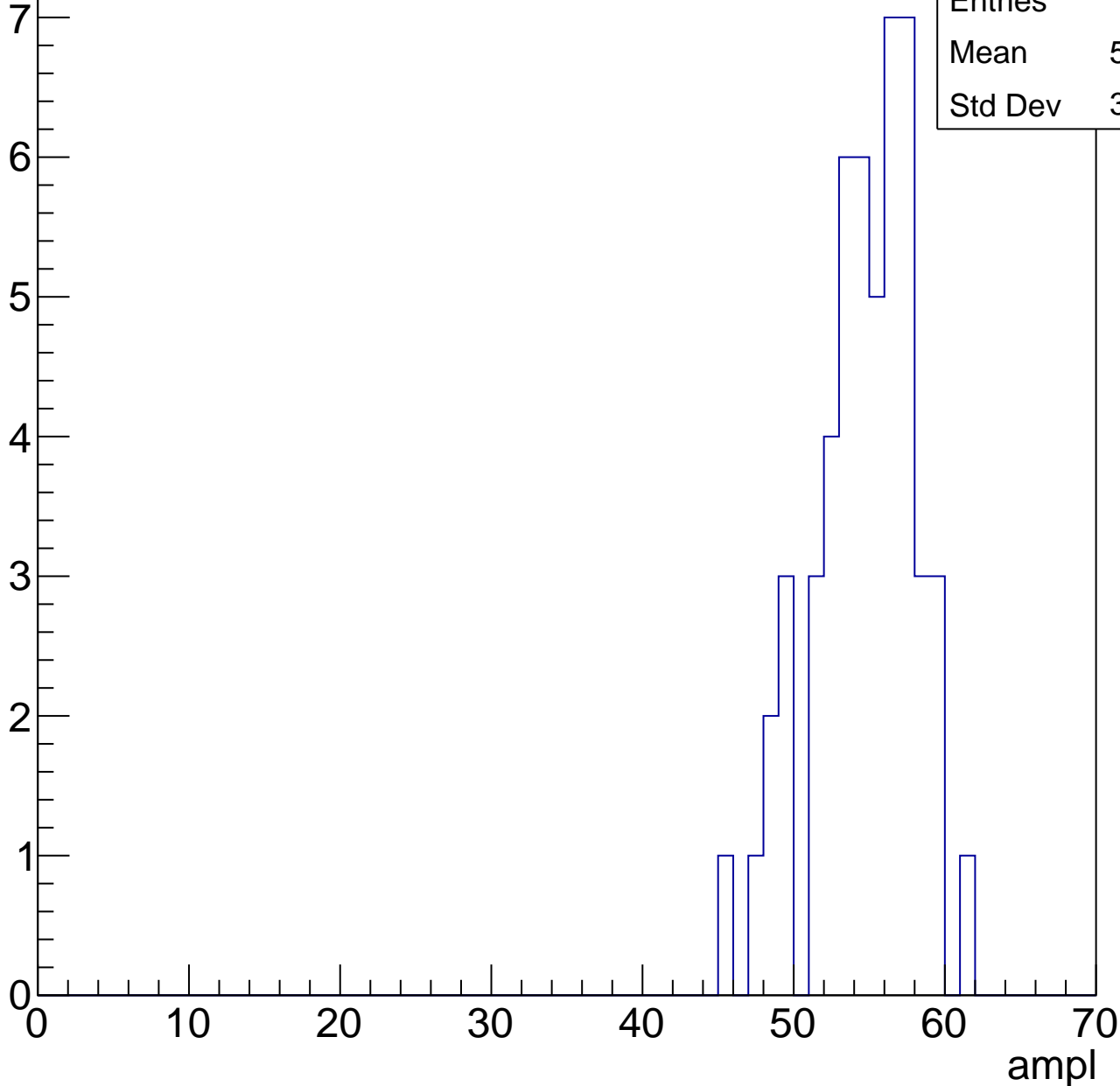


# B1L102S, U20-ch44, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	54.15
Std Dev	3.376

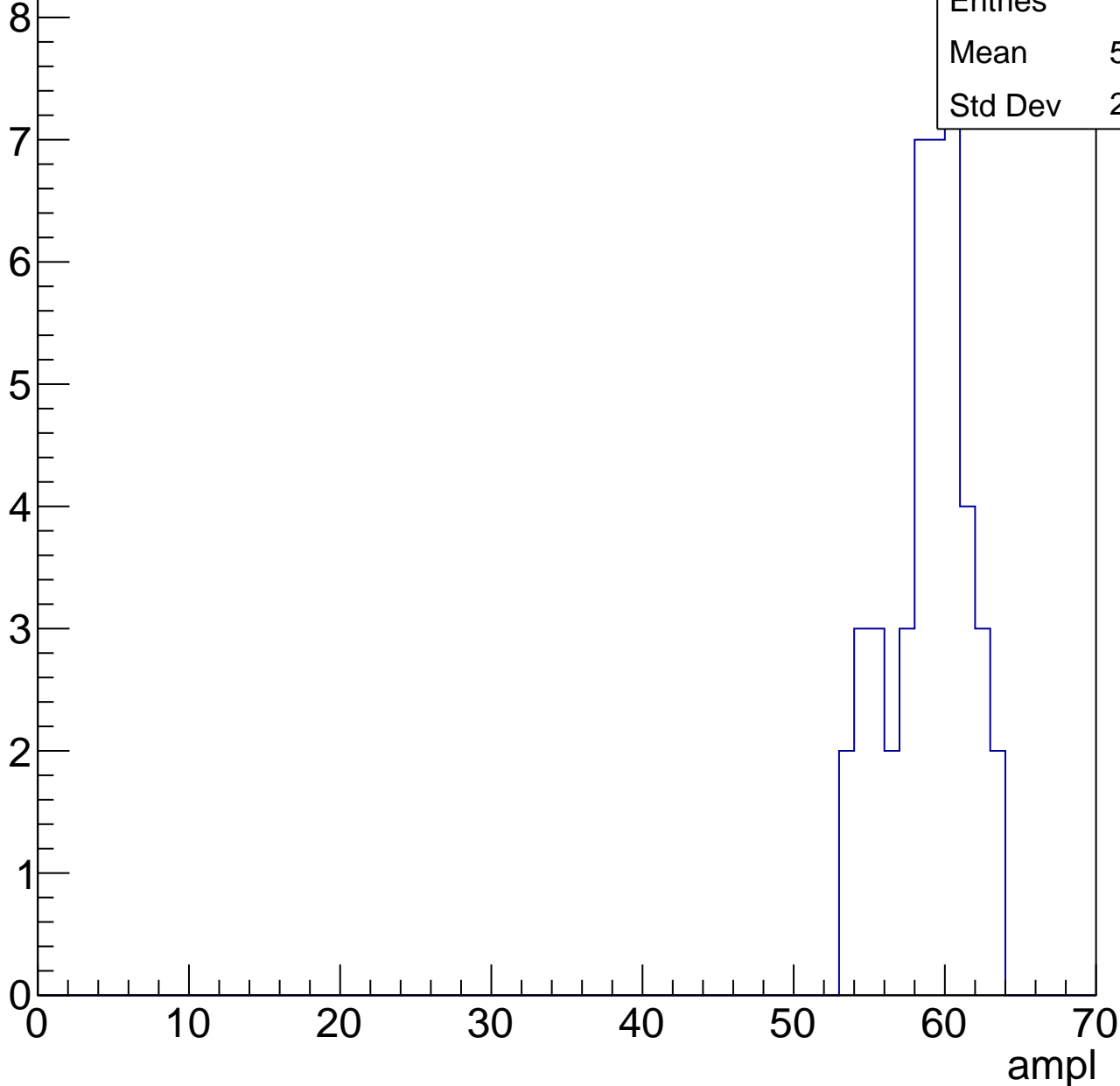


# B1L102S, U20-ch44, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	44
Mean	58.43
Std Dev	2.615

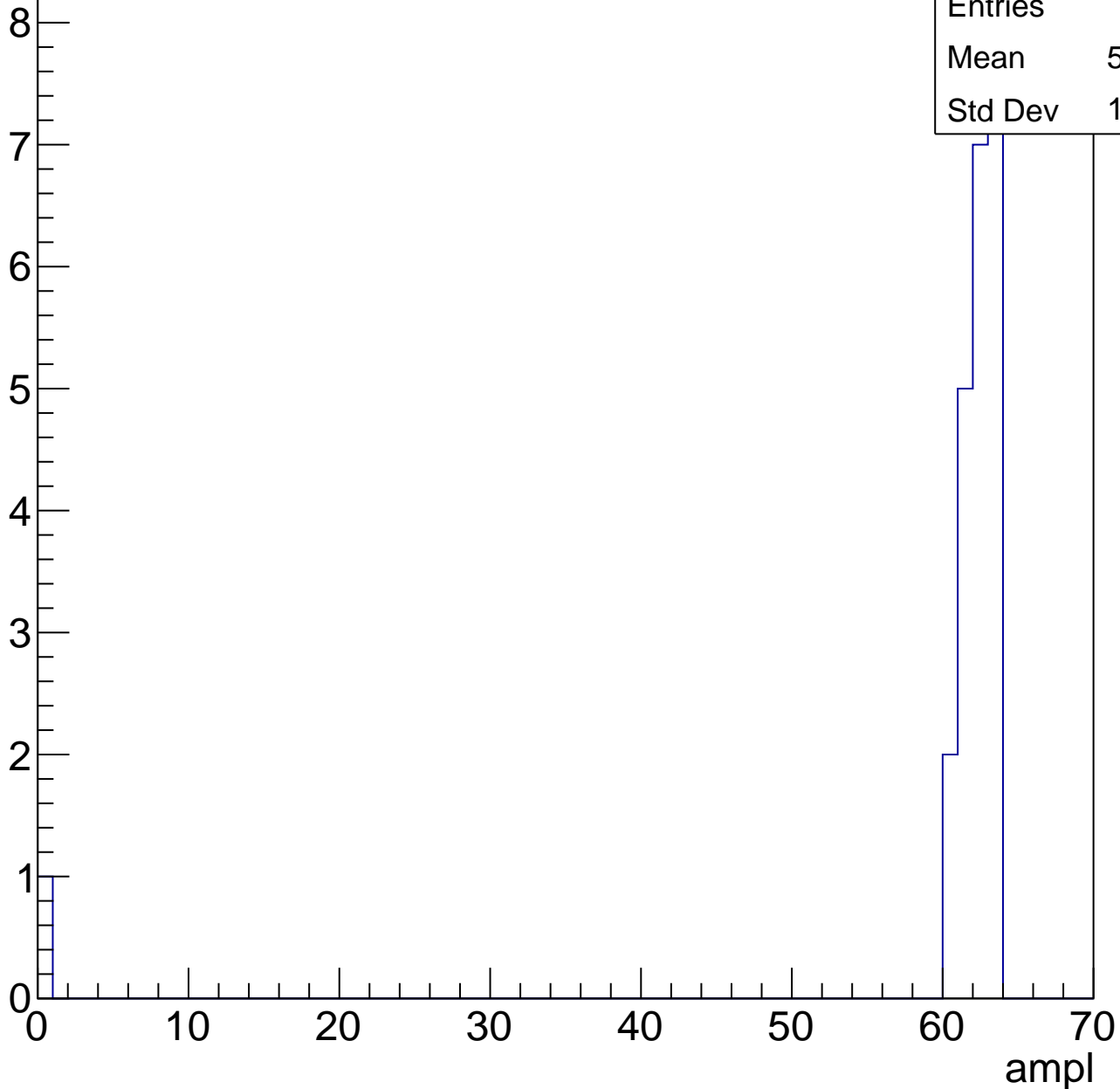


# B1L102S, U20-ch44, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	23
Mean	59.26
Std Dev	12.67





# B1L102S, U20-ch44, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U20-ch45, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	76
Mean	27.87
Std Dev	4.411

**Gaus mean : 28.7967**

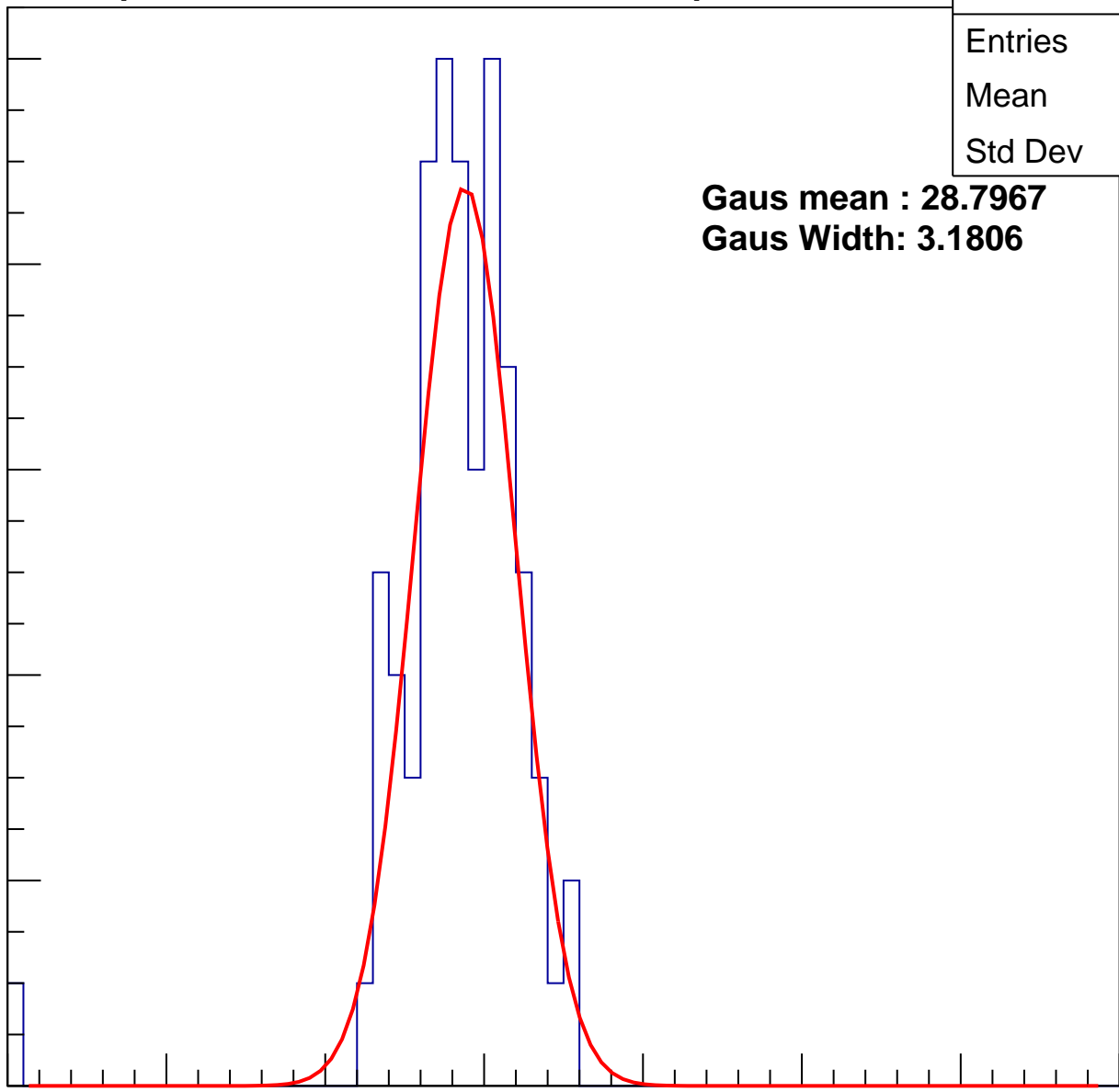
**Gaus Width: 3.1806**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U20-ch45, adc1

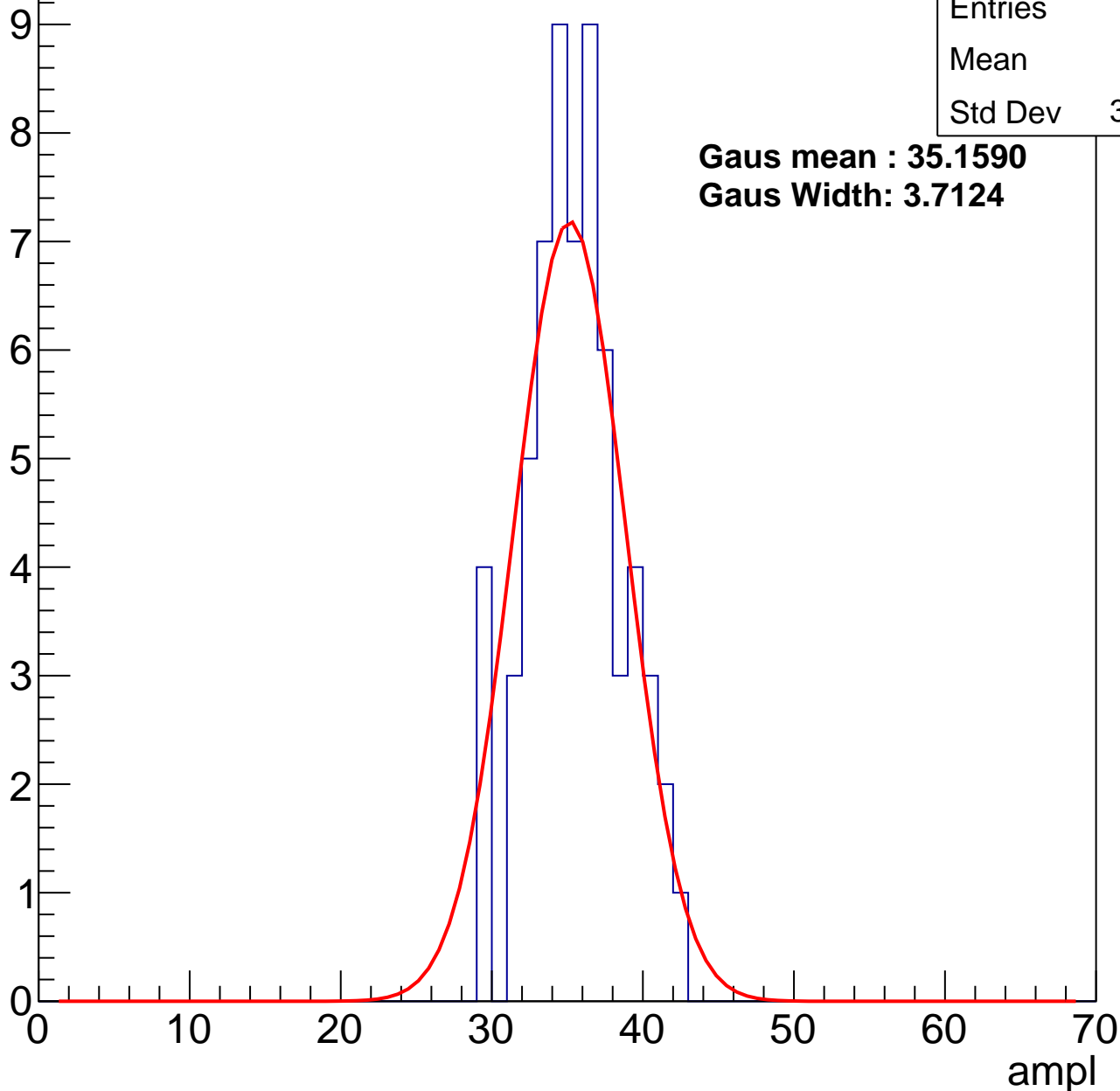
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	35.1
Std Dev	3.069

**Gaus mean : 35.1590**

**Gaus Width: 3.7124**



# B1L102S, U20-ch45, adc2

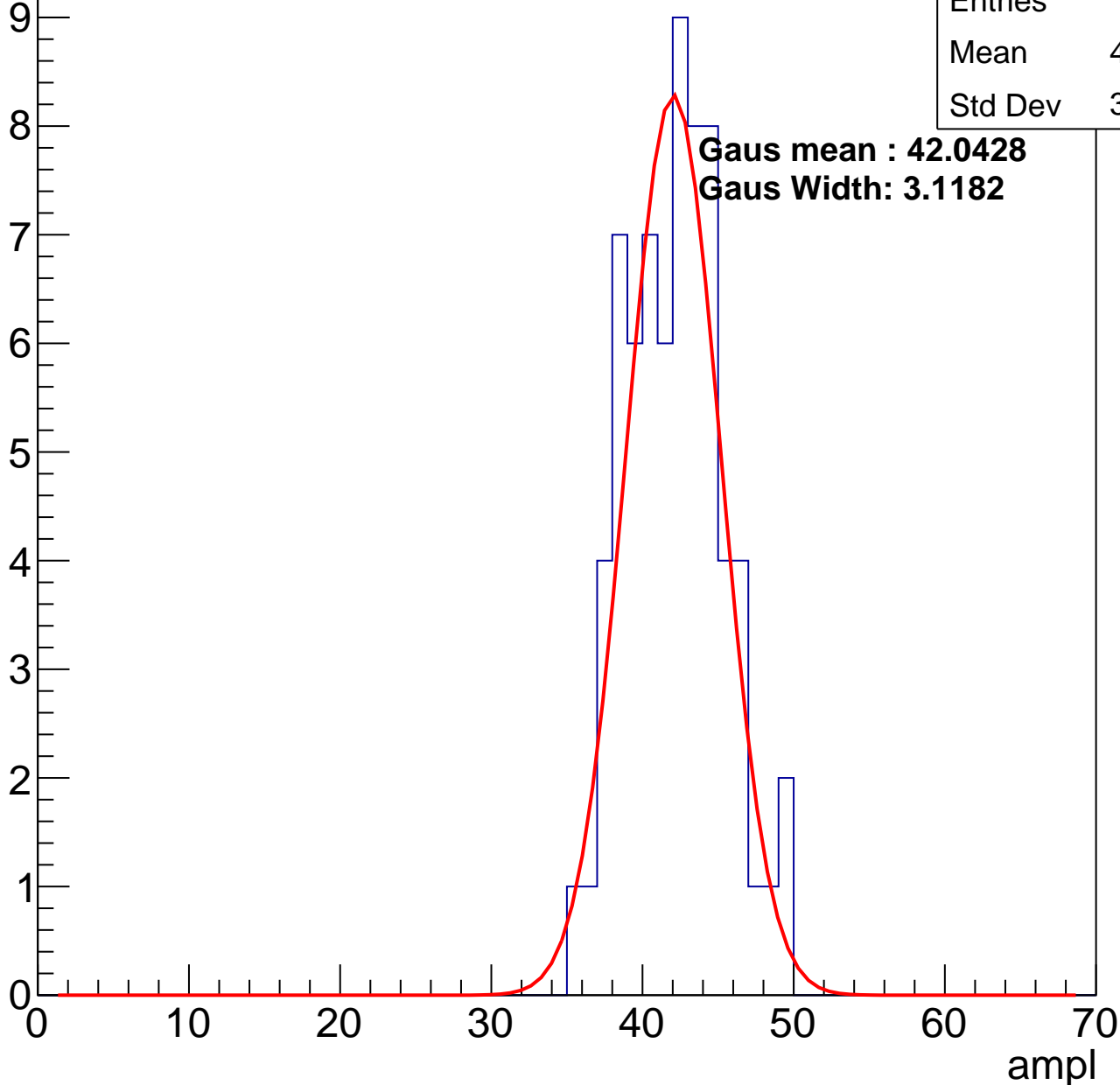
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	41.68
Std Dev	3.132

**Gaus mean : 42.0428**

**Gaus Width: 3.1182**



# B1L102S, U20-ch45, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	70
Mean	48.44
Std Dev	3.124

Entry

10

8

6

4

2

0

0

10

20

30

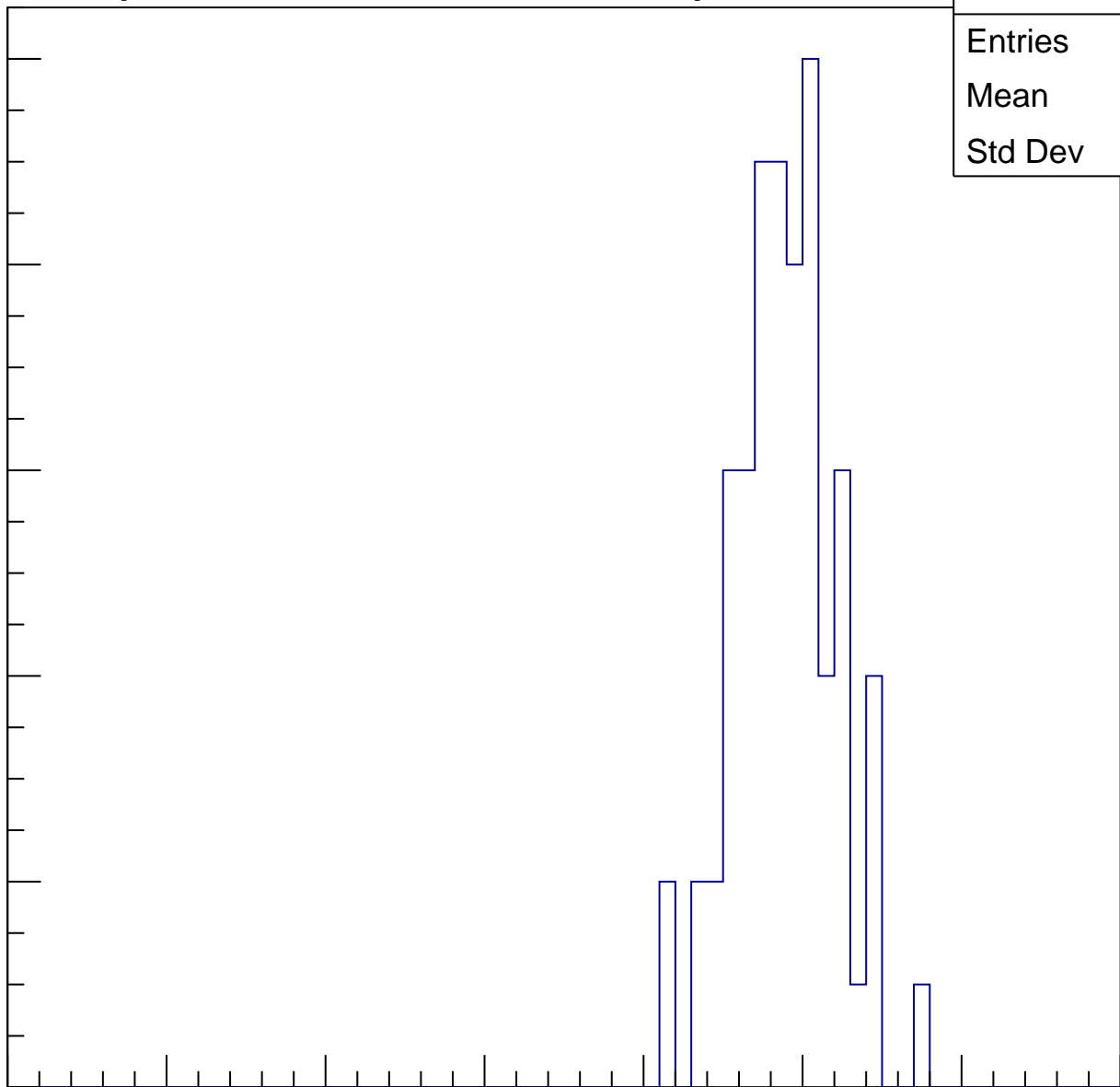
40

50

60

ampl

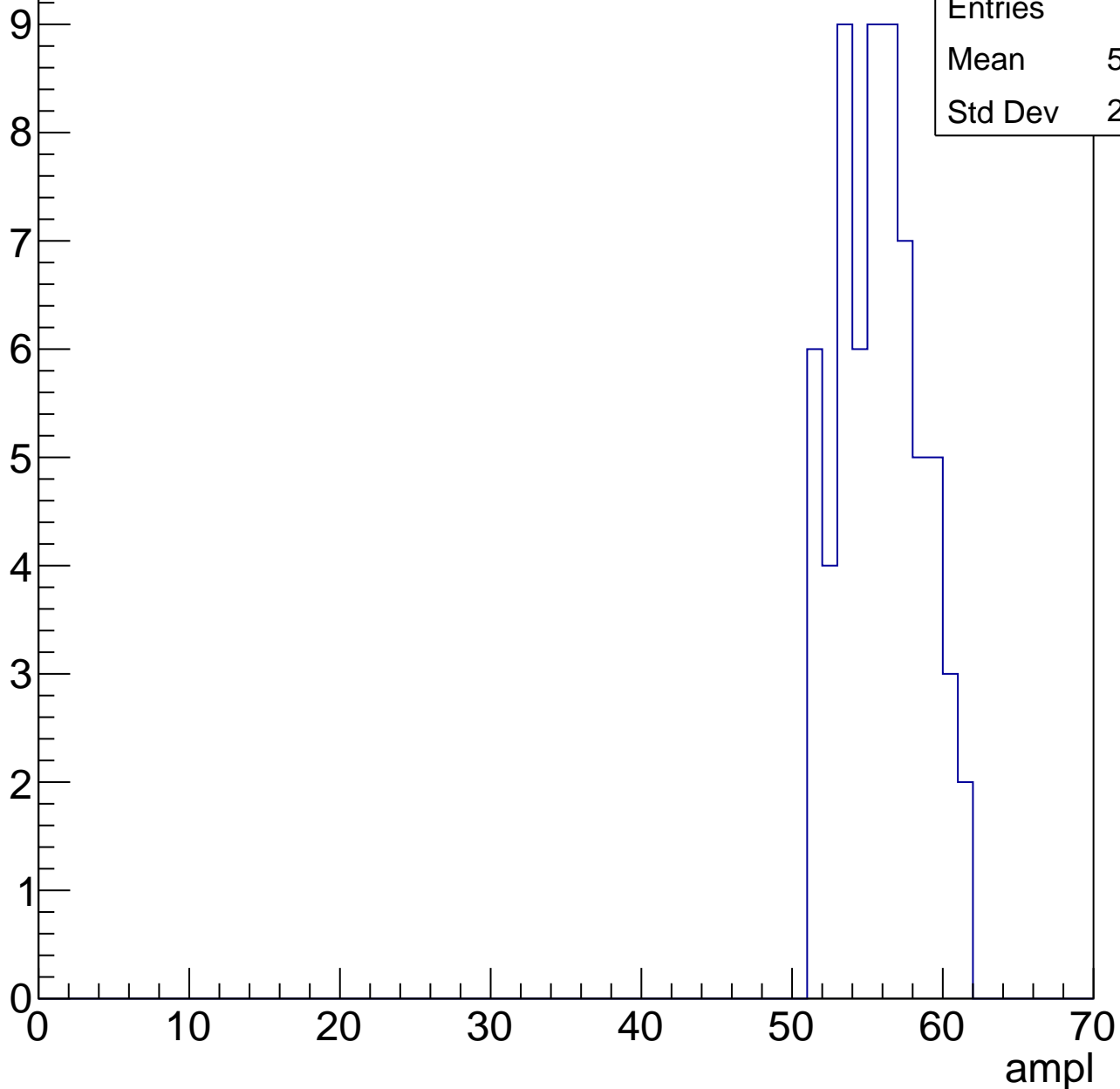
70



# B1L102S, U20-ch45, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

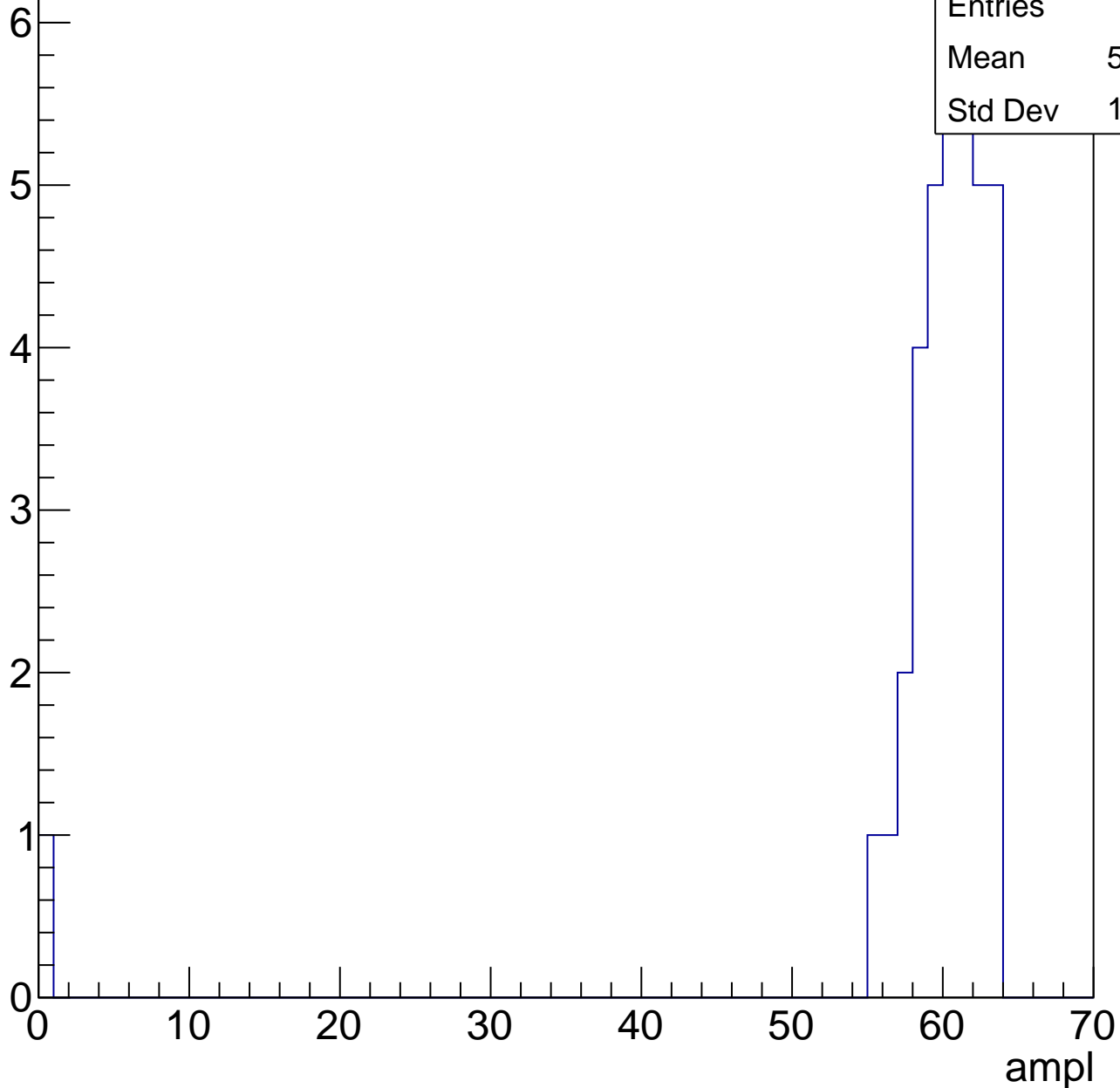


Entries	65
Mean	55.38
Std Dev	2.699

# B1L102S, U20-ch45, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

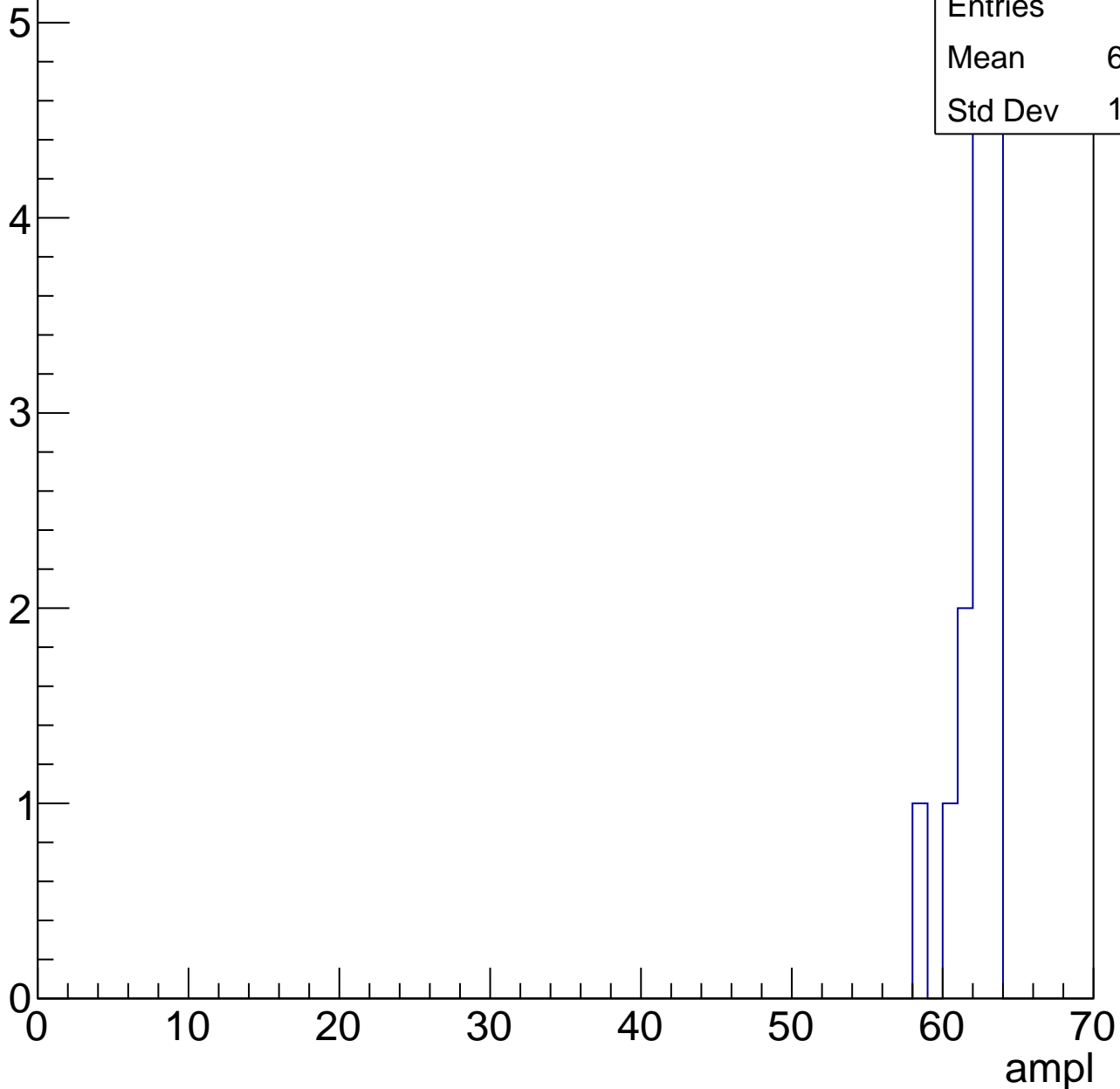


# B1L102S, U20-ch45, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	14
Mean	61.79
Std Dev	1.372





# B1L102S, U20-ch45, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch46, adc0

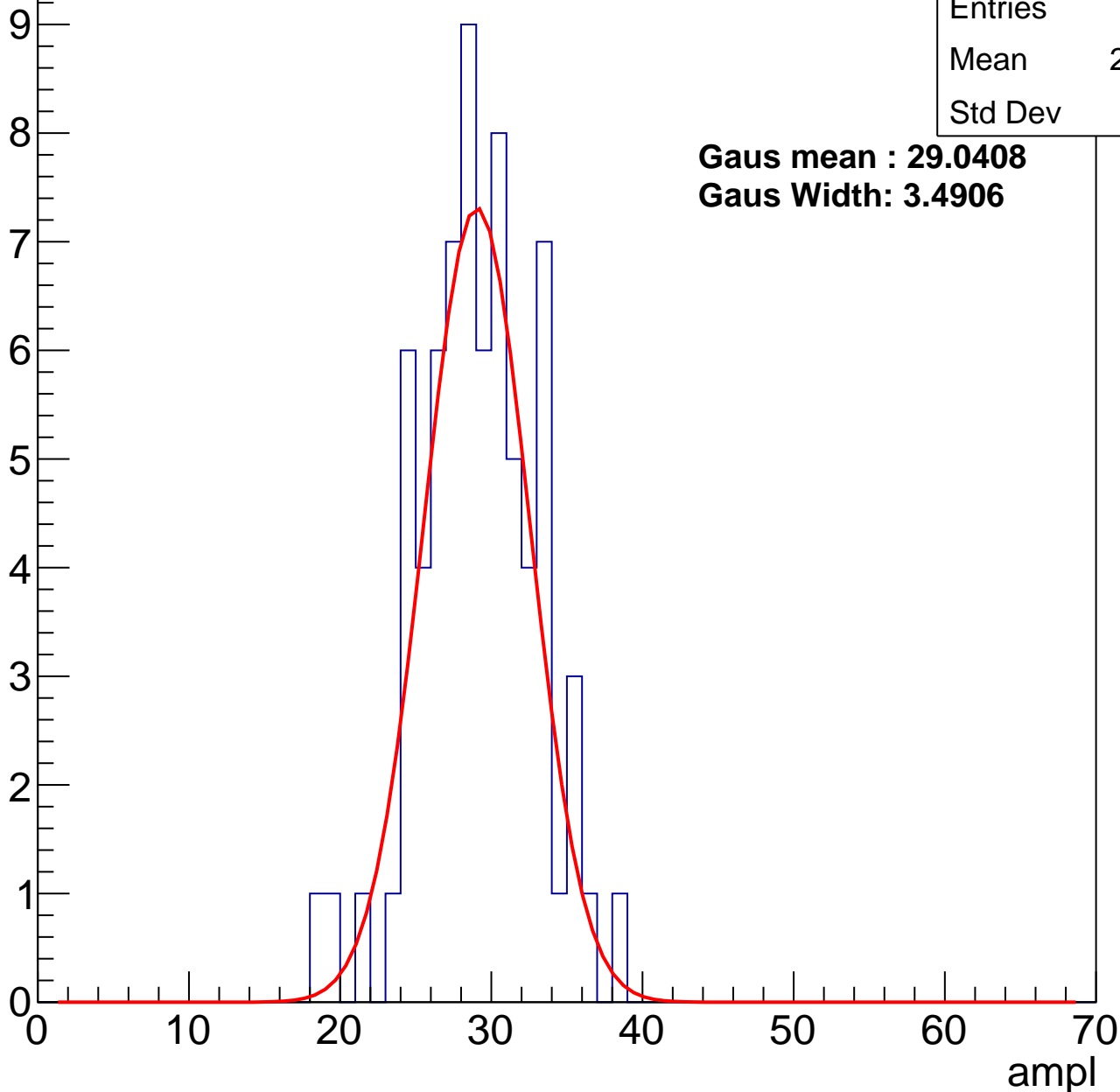
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	28.65
Std Dev	3.83

**Gaus mean : 29.0408**

**Gaus Width: 3.4906**



# B1L102S, U20-ch46, adc1

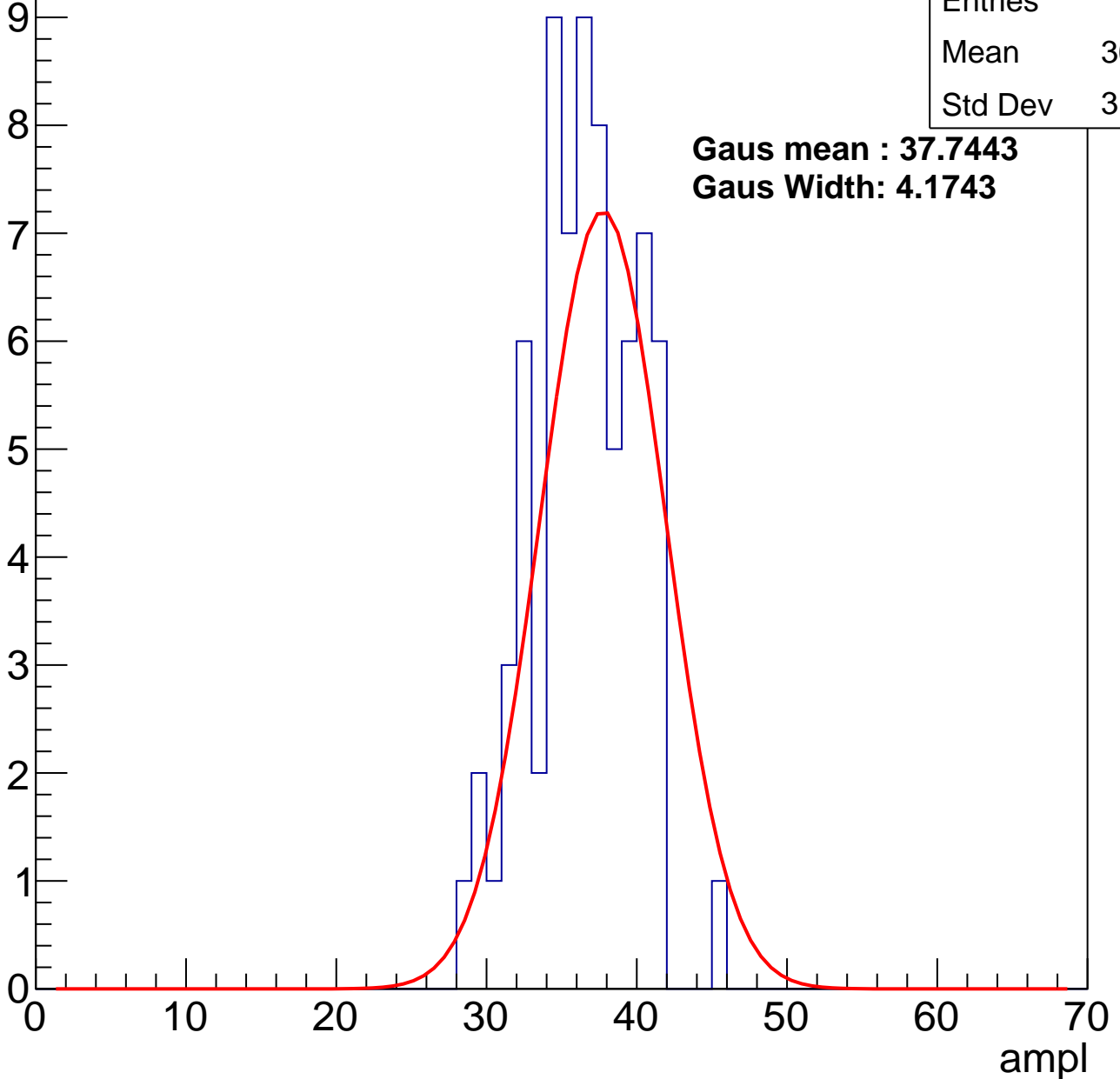
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	36.07
Std Dev	3.422

**Gaus mean : 37.7443**

**Gaus Width: 4.1743**



# B1L102S, U20-ch46, adc2

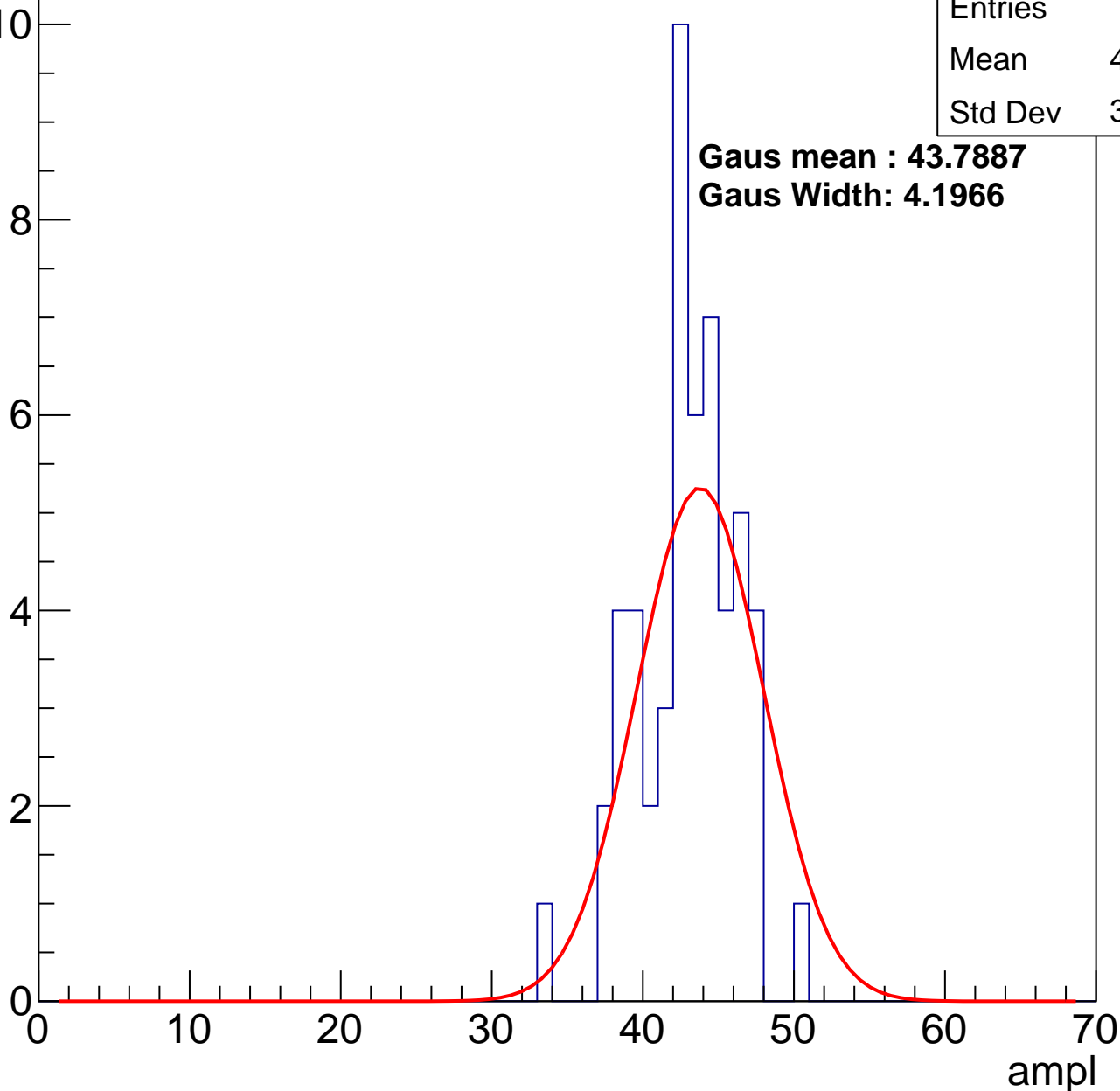
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	42.49
Std Dev	3.202

**Gaus mean : 43.7887**

**Gaus Width: 4.1966**

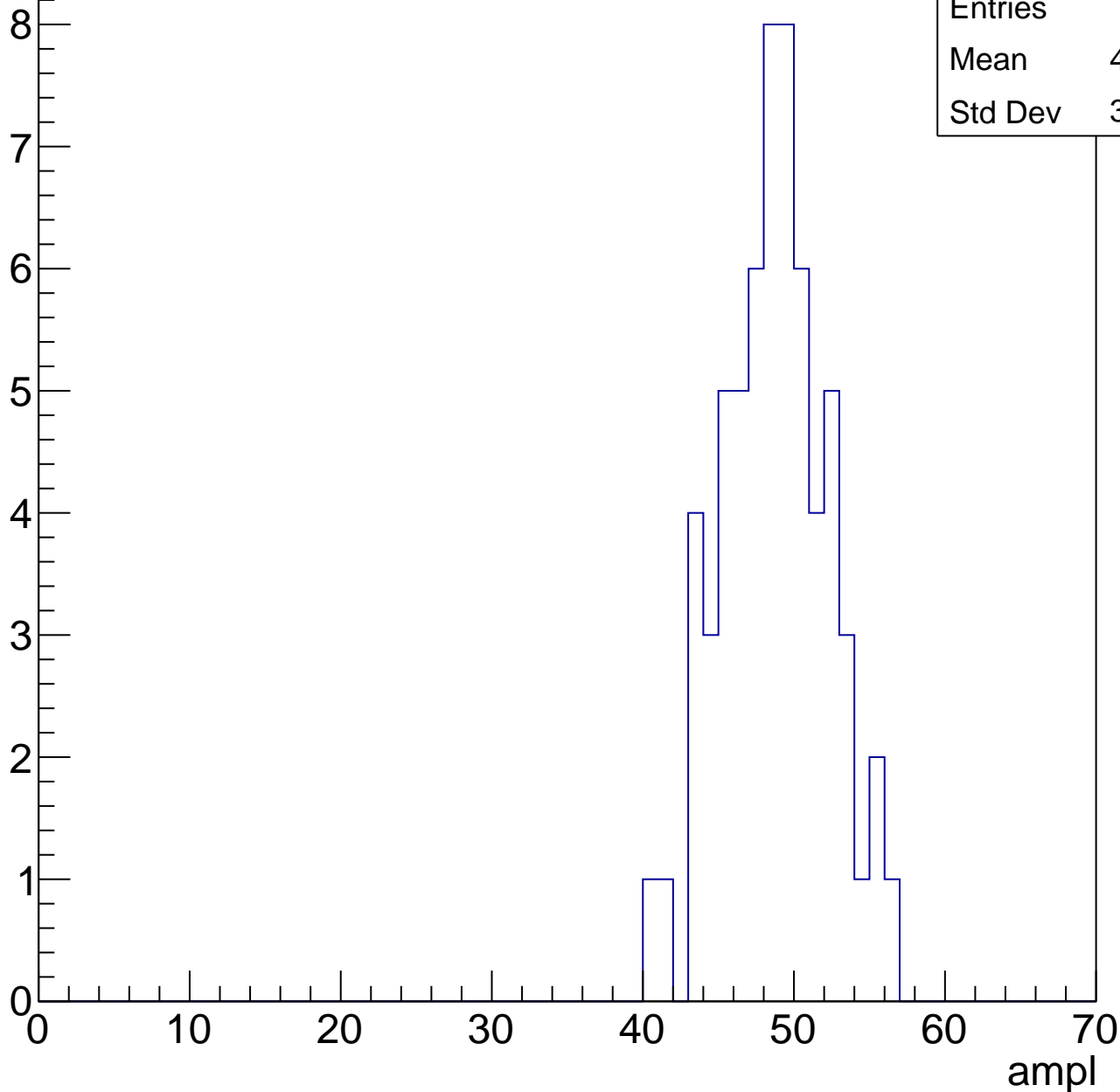


# B1L102S, U20-ch46, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	48.27
Std Dev	3.447

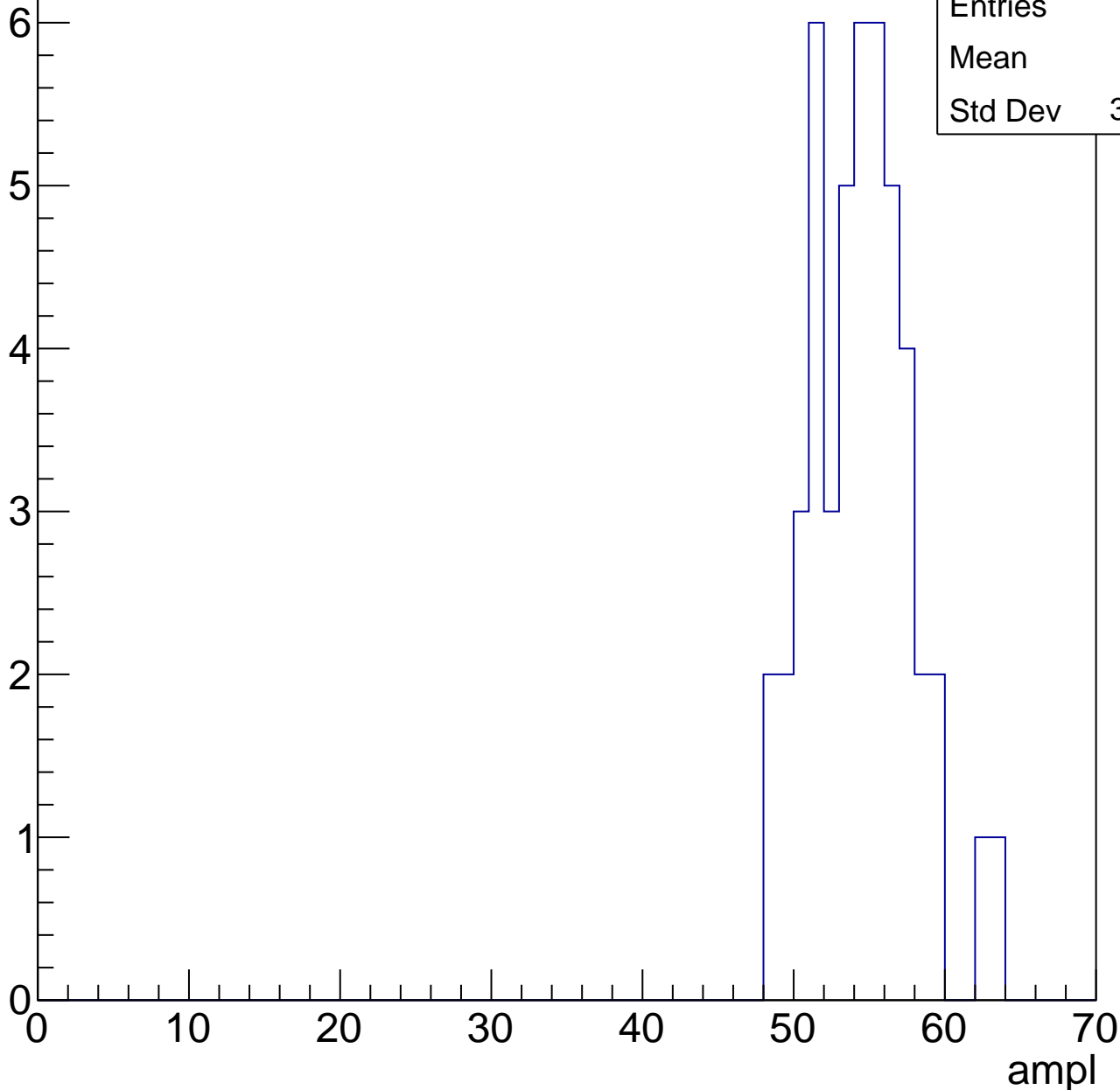


# B1L102S, U20-ch46, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	48
Mean	54
Std Dev	3.323



# B1L102S, U20-ch46, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

10

8

6

4

2

0

0

10

20

30

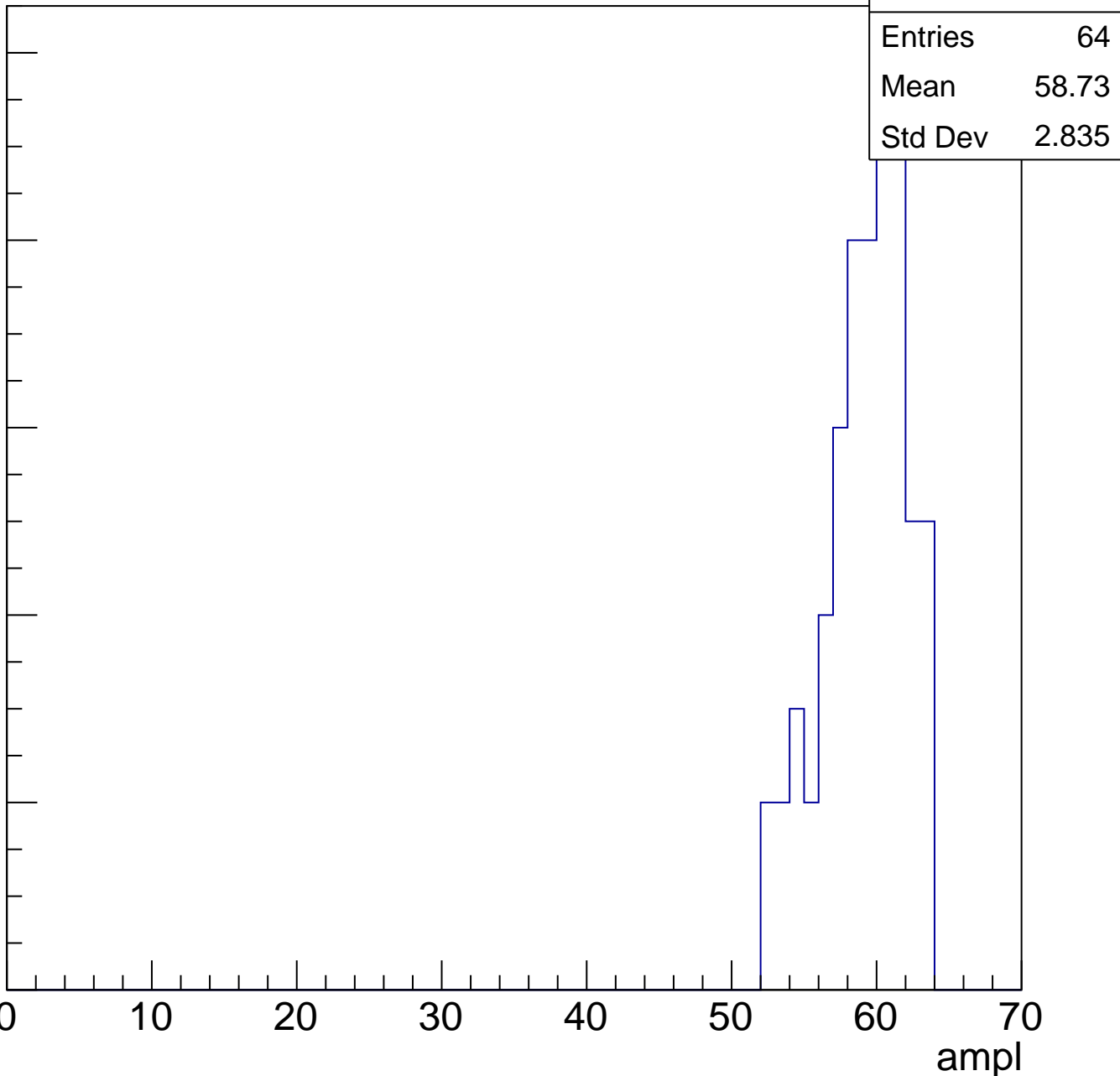
40

50

60

ampl

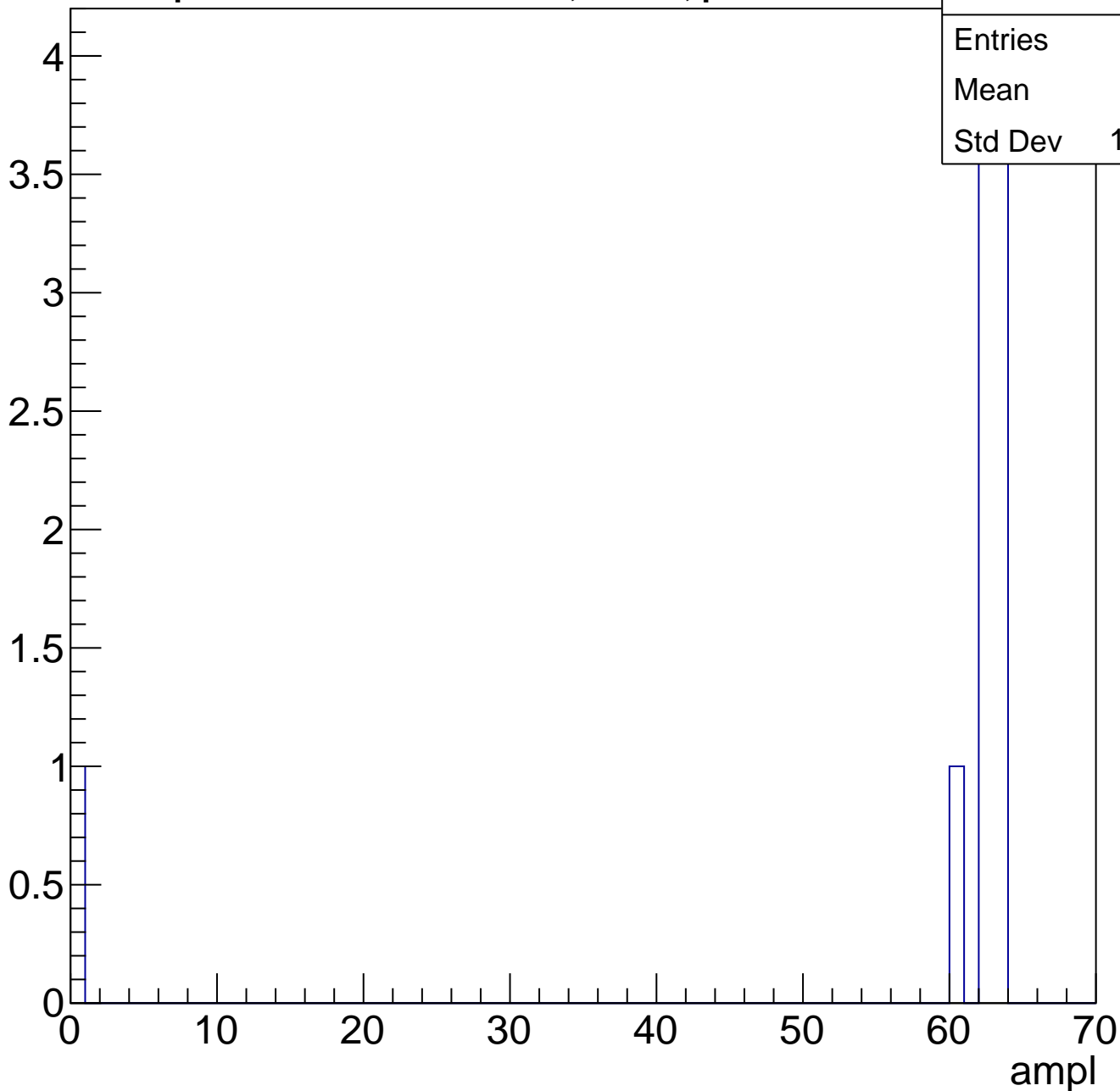
Entries	64
Mean	58.73
Std Dev	2.835



# B1L102S, U20-ch46, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U20-ch46, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

0

Mean

0

Std Dev

0

# B1L102S, U20-ch47, adc0

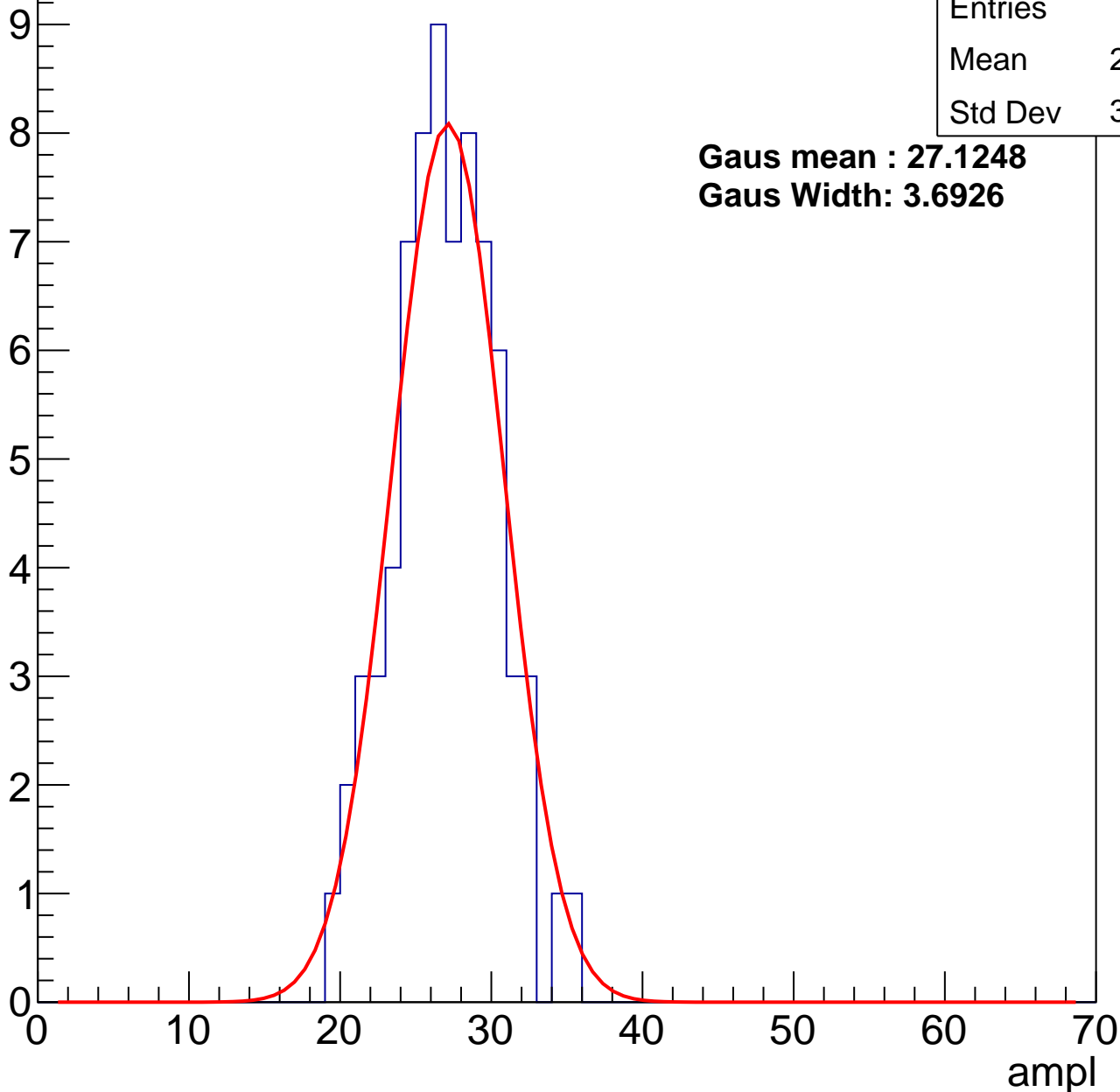
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	26.52
Std Dev	3.356

**Gaus mean : 27.1248**

**Gaus Width: 3.6926**



# B1L102S, U20-ch47, adc1

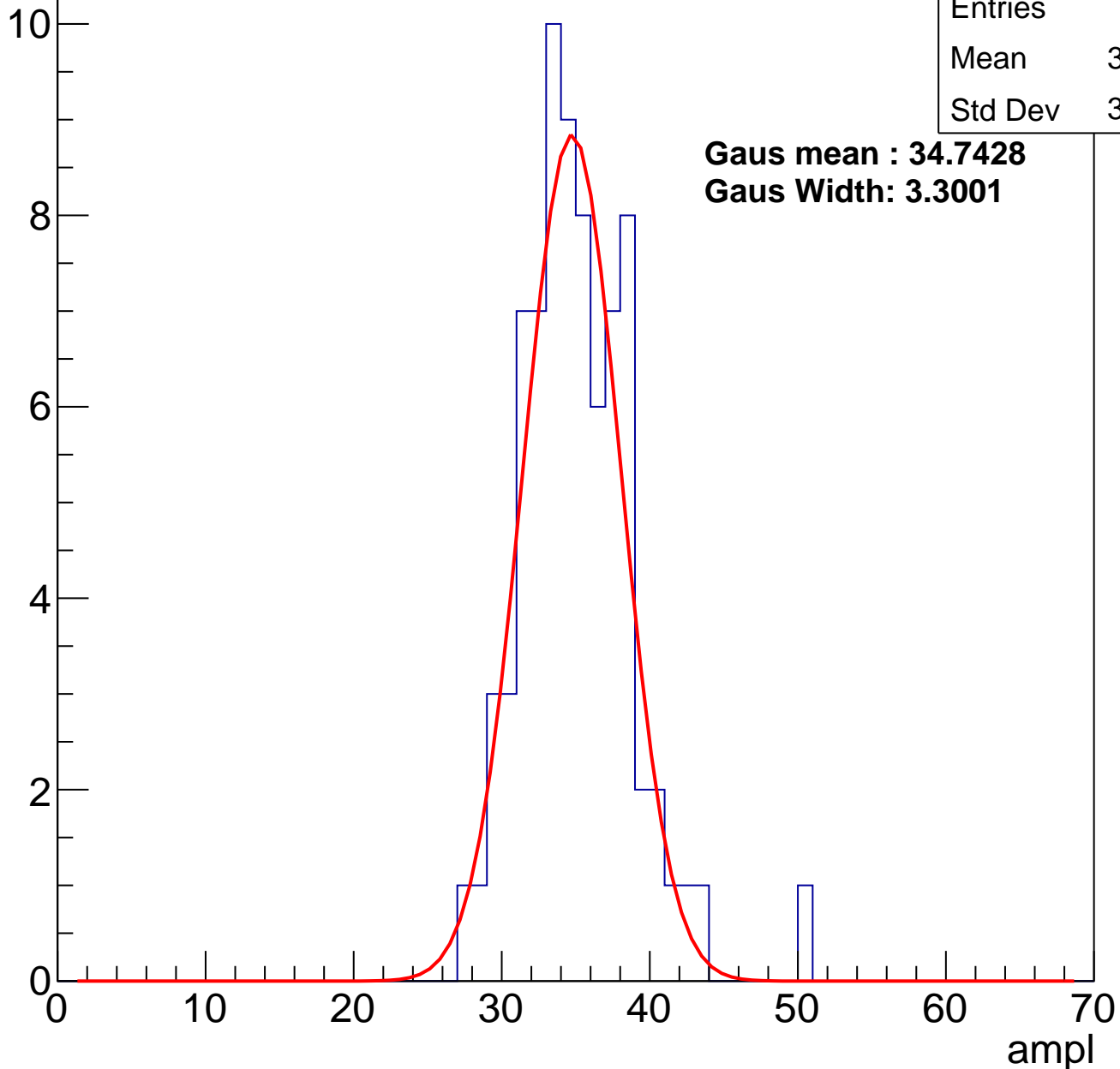
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	78
Mean	34.64
Std Dev	3.707

**Gaus mean : 34.7428**

**Gaus Width: 3.3001**

Entry



# B1L102S, U20-ch47, adc2

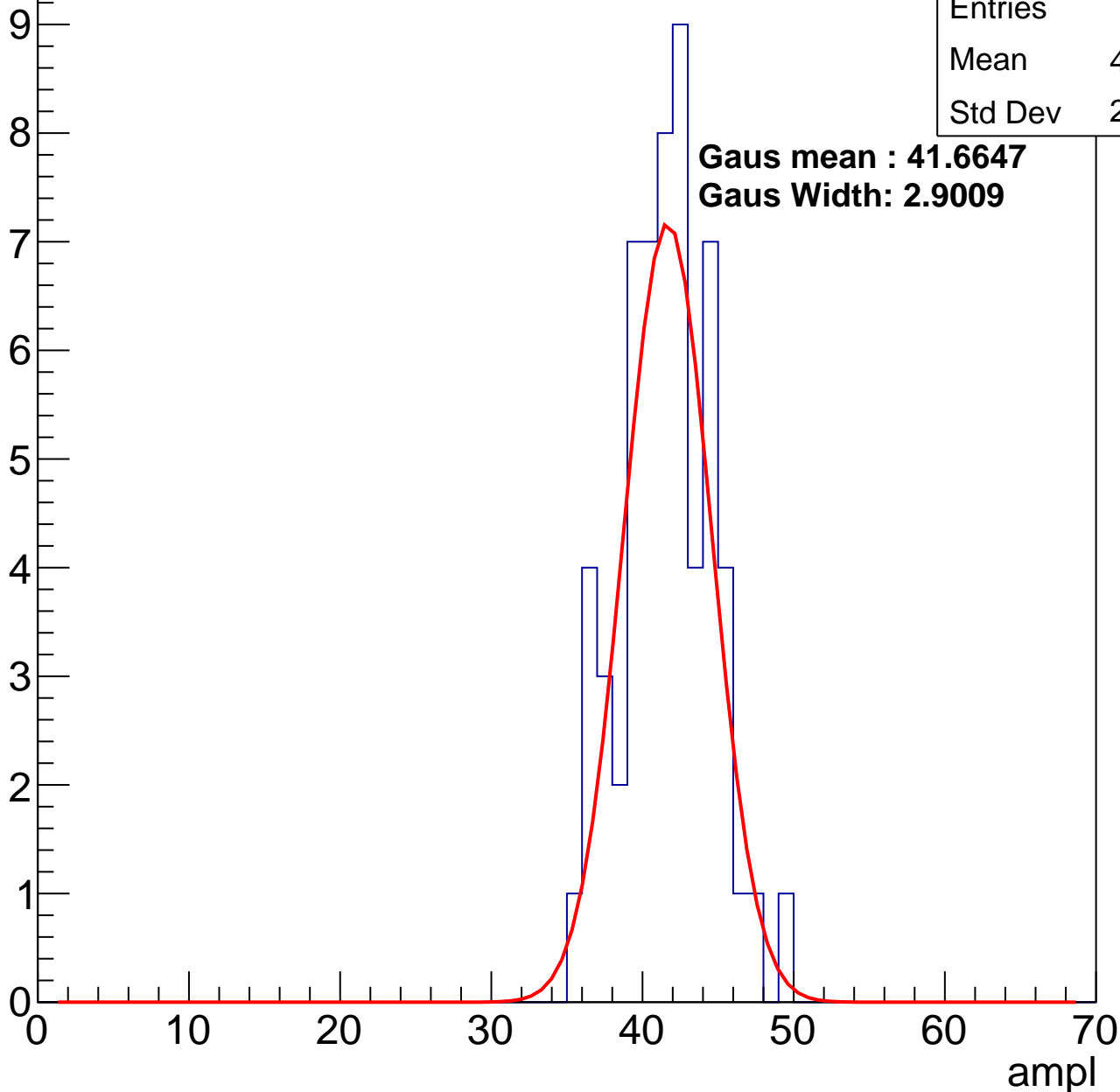
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	41.14
Std Dev	2.948

**Gaus mean : 41.6647**

**Gaus Width: 2.9009**



# B1L102S, U20-ch47, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

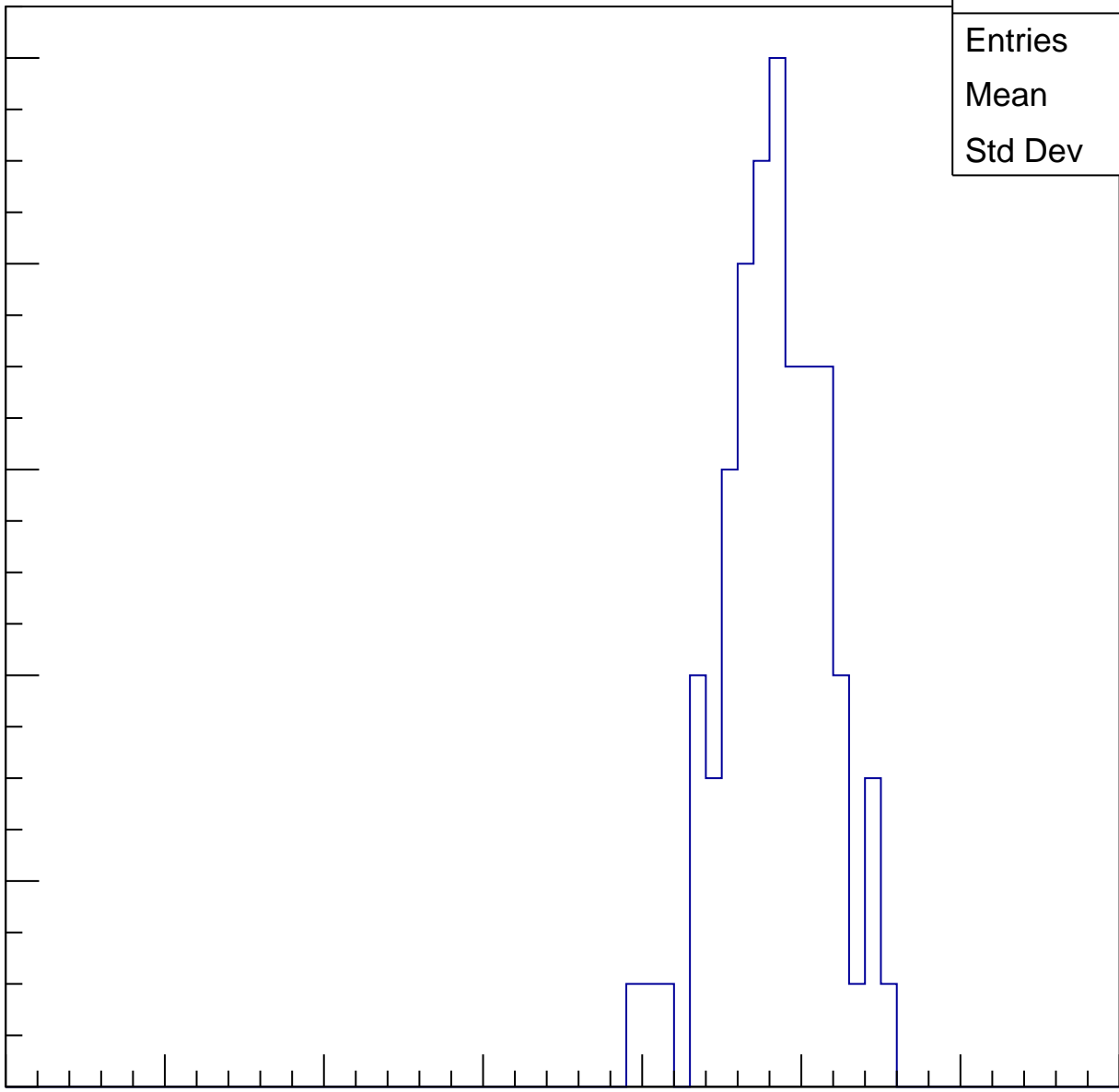
Entries	73
Mean	47.85
Std Dev	3.267

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

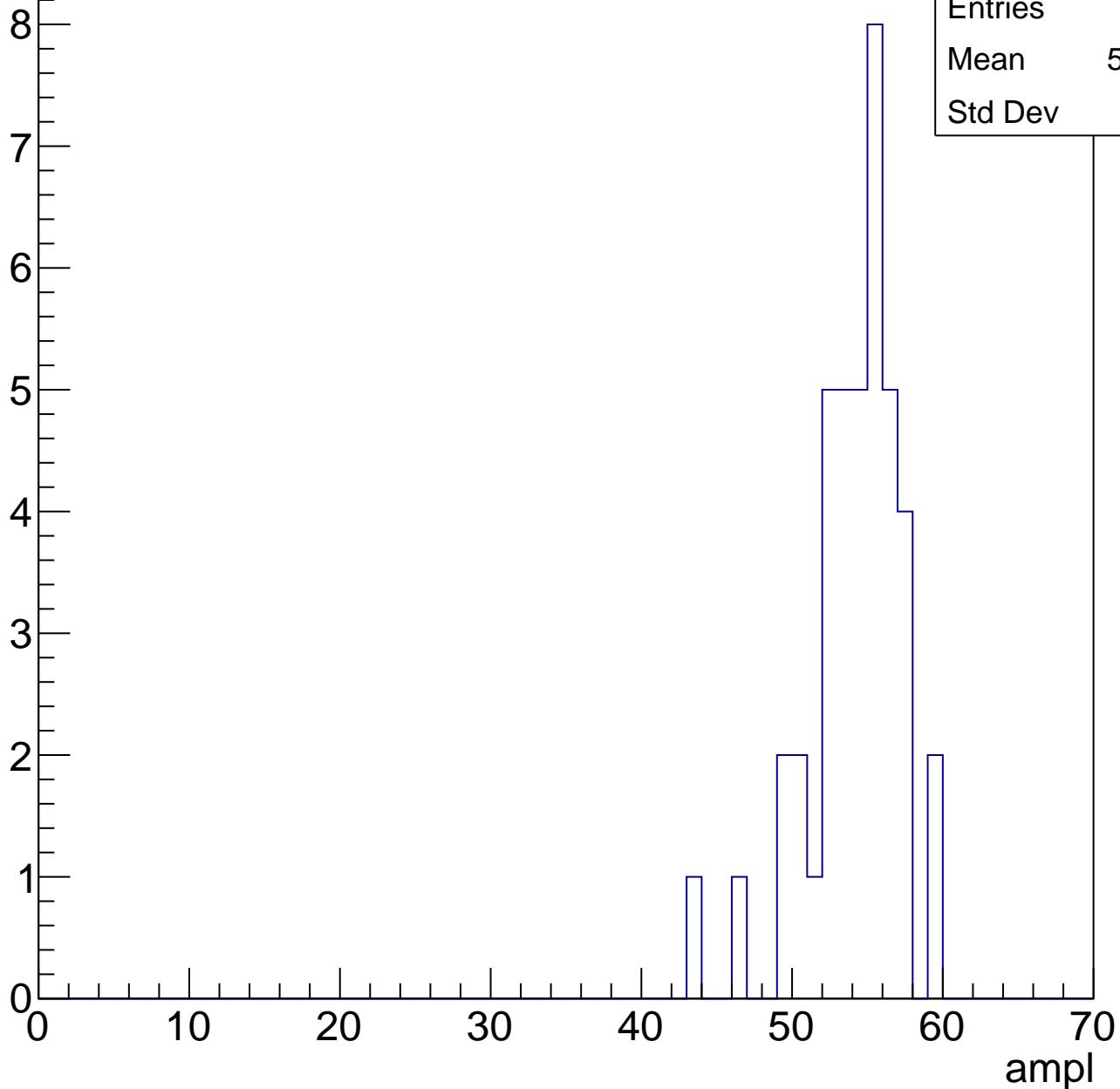


# B1L102S, U20-ch47, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	41
Mean	53.63
Std Dev	3.16



# B1L102S, U20-ch47, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	70
Mean	58.6
Std Dev	3.035

Entry

10

8

6

4

2

0

0

10

20

30

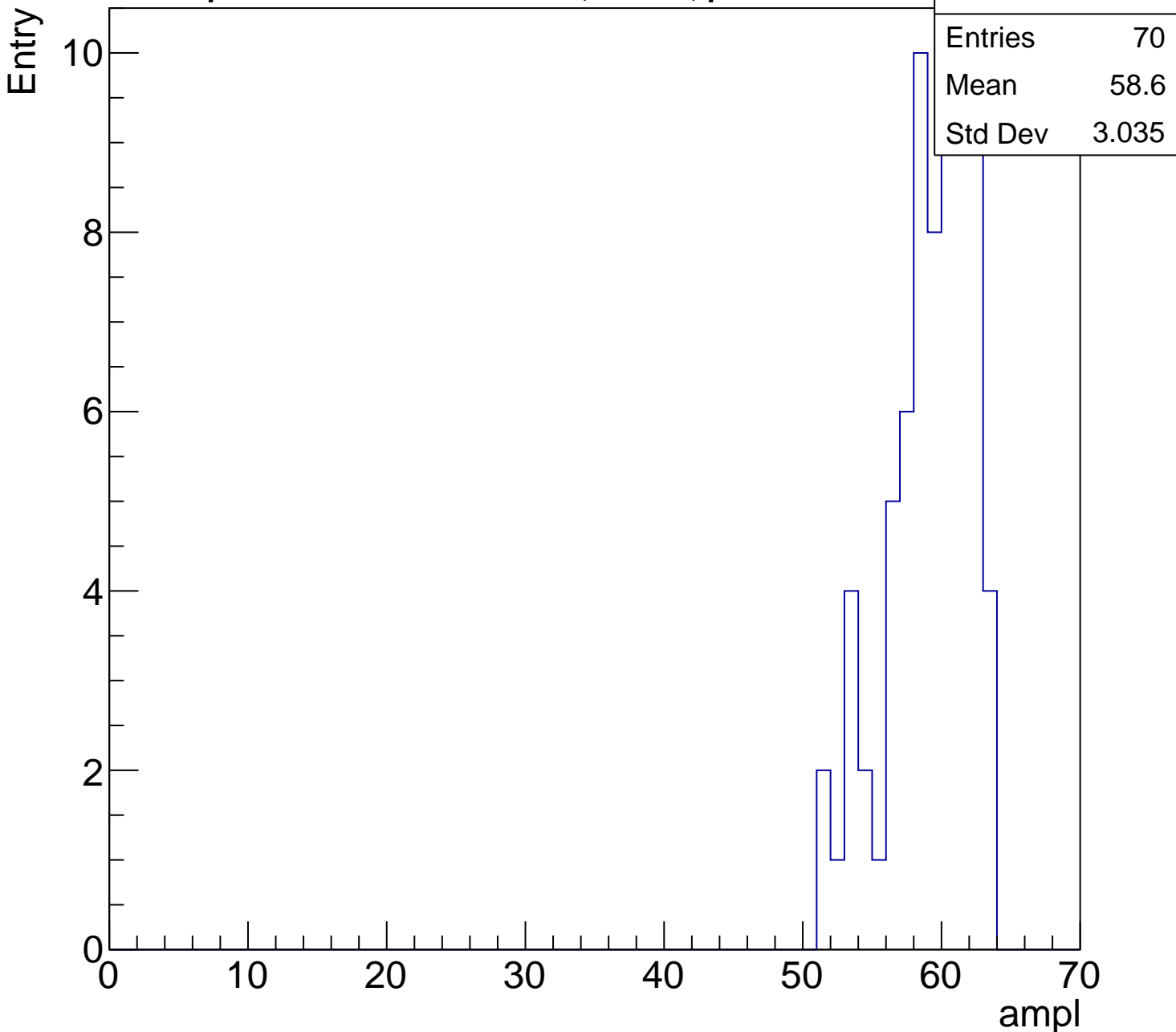
40

50

60

ampl

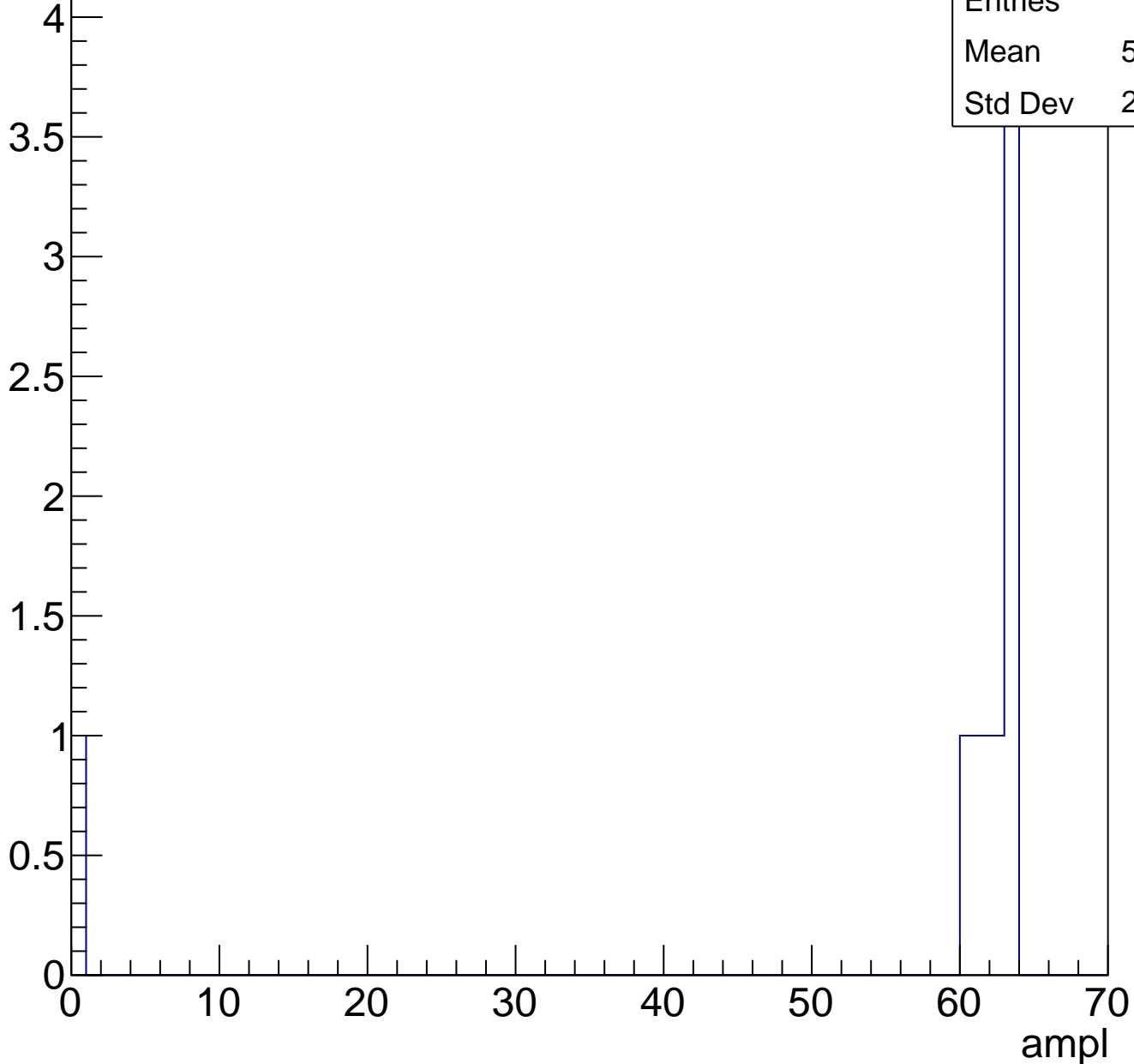
70



# B1L102S, U20-ch47, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U20-ch47, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	63
Std Dev	0

# B1L102S, U20-ch48, adc0

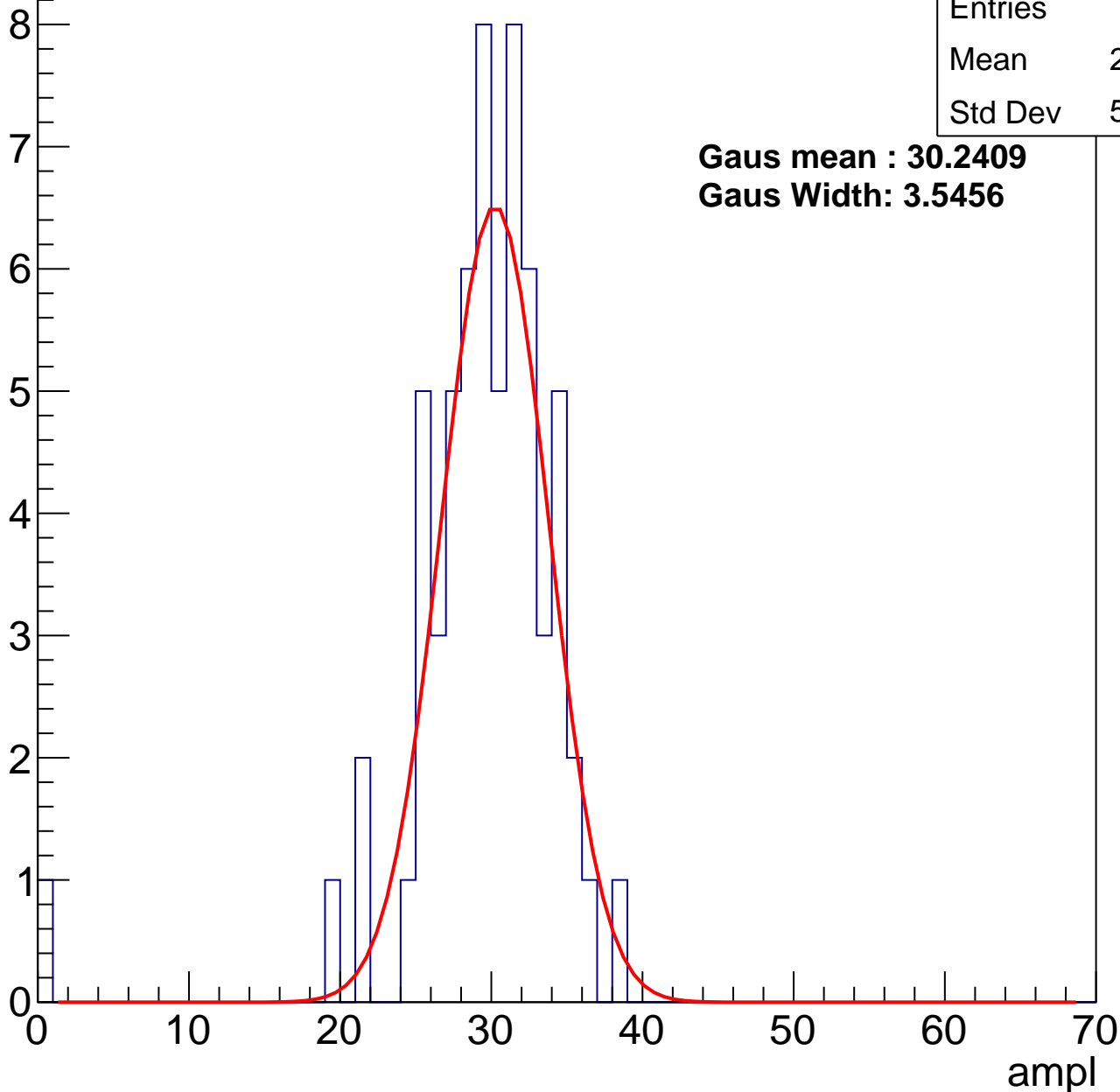
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	28.98
Std Dev	5.184

**Gaus mean : 30.2409**

**Gaus Width: 3.5456**



# B1L102S, U20-ch48, adc1

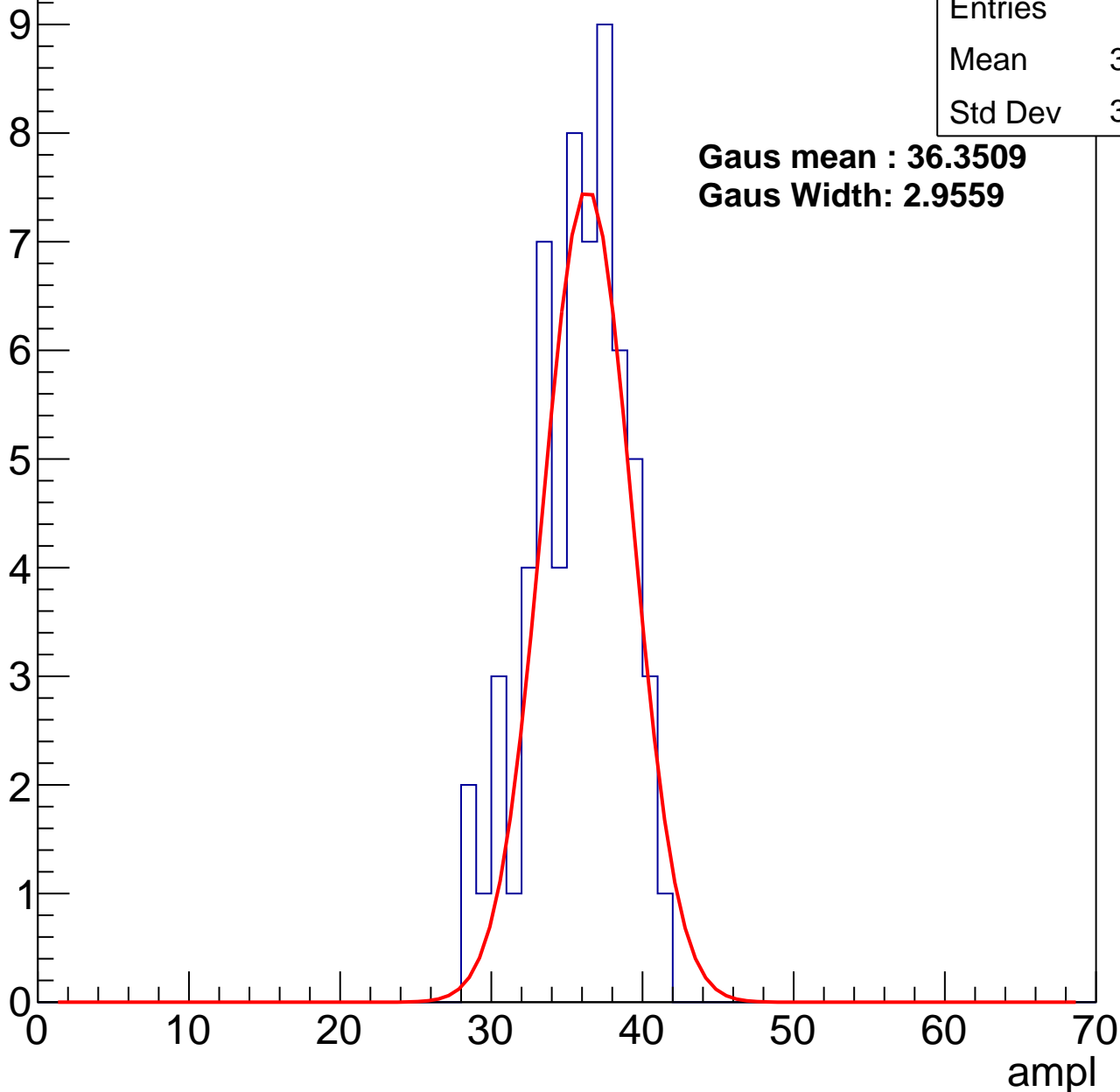
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	35.25
Std Dev	3.076

**Gaus mean : 36.3509**

**Gaus Width: 2.9559**



# B1L102S, U20-ch48, adc2

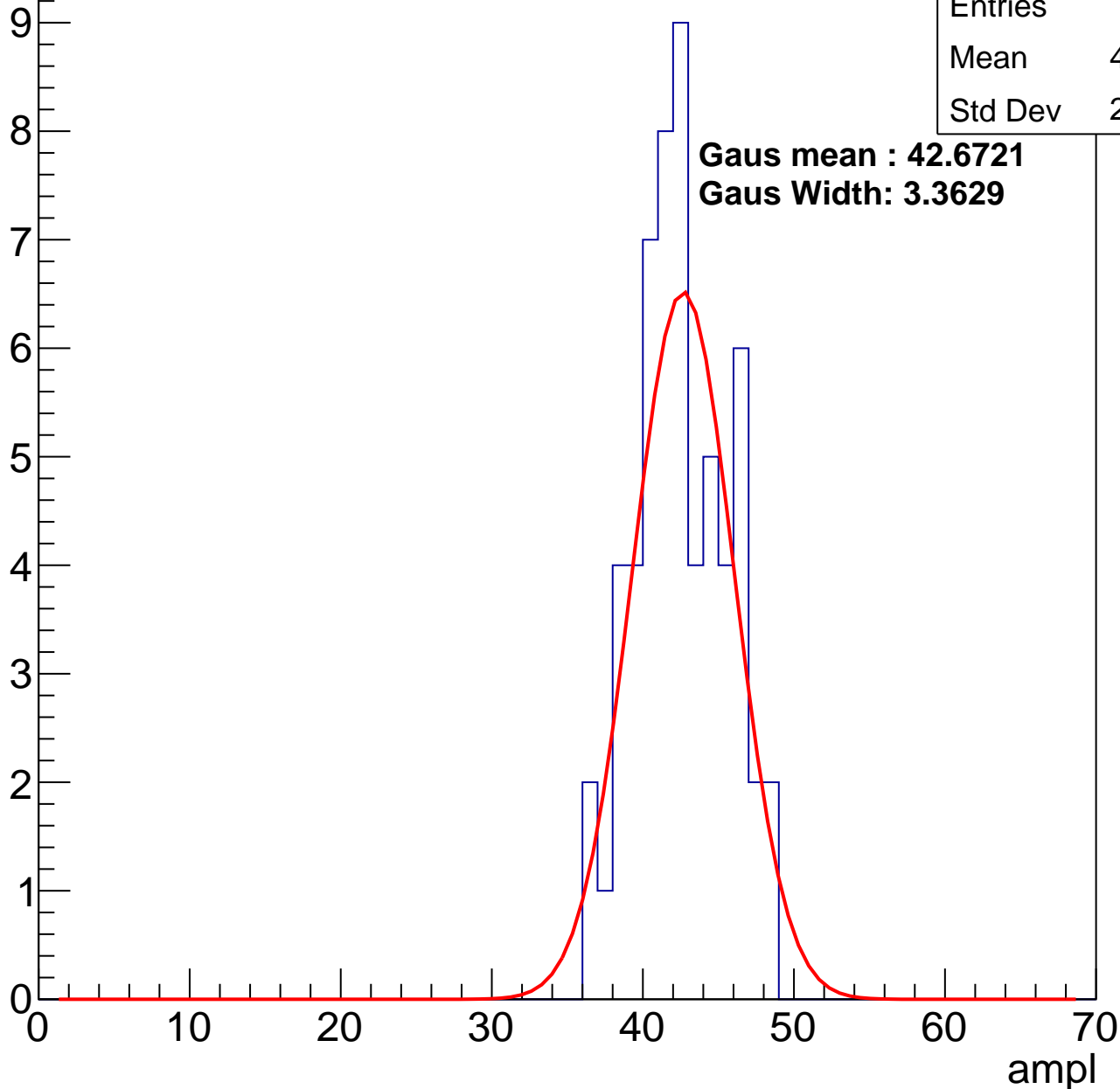
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	42.09
Std Dev	2.967

**Gaus mean : 42.6721**

**Gaus Width: 3.3629**

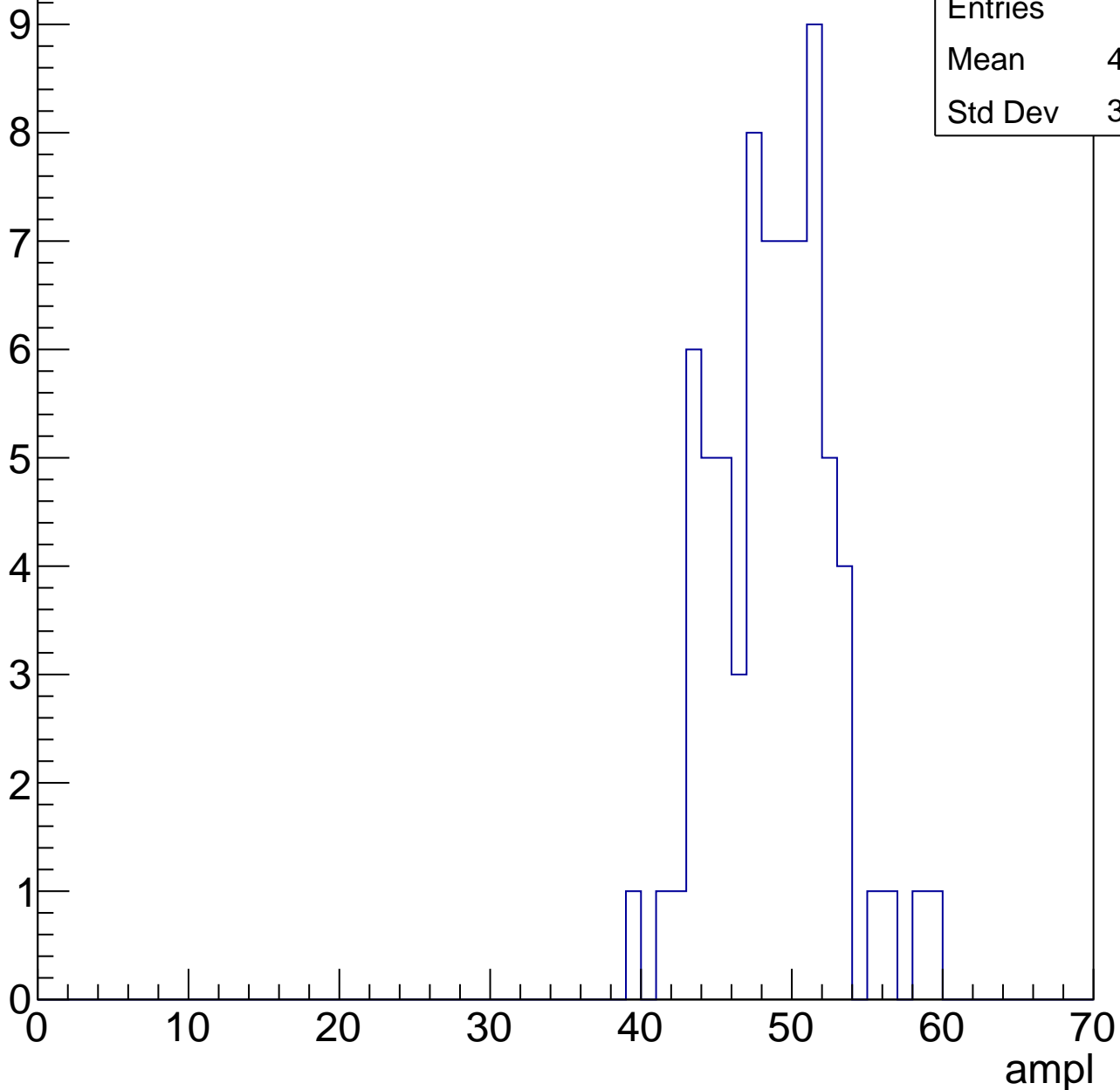


# B1L102S, U20-ch48, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	48.32
Std Dev	3.853



# B1L102S, U20-ch48, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

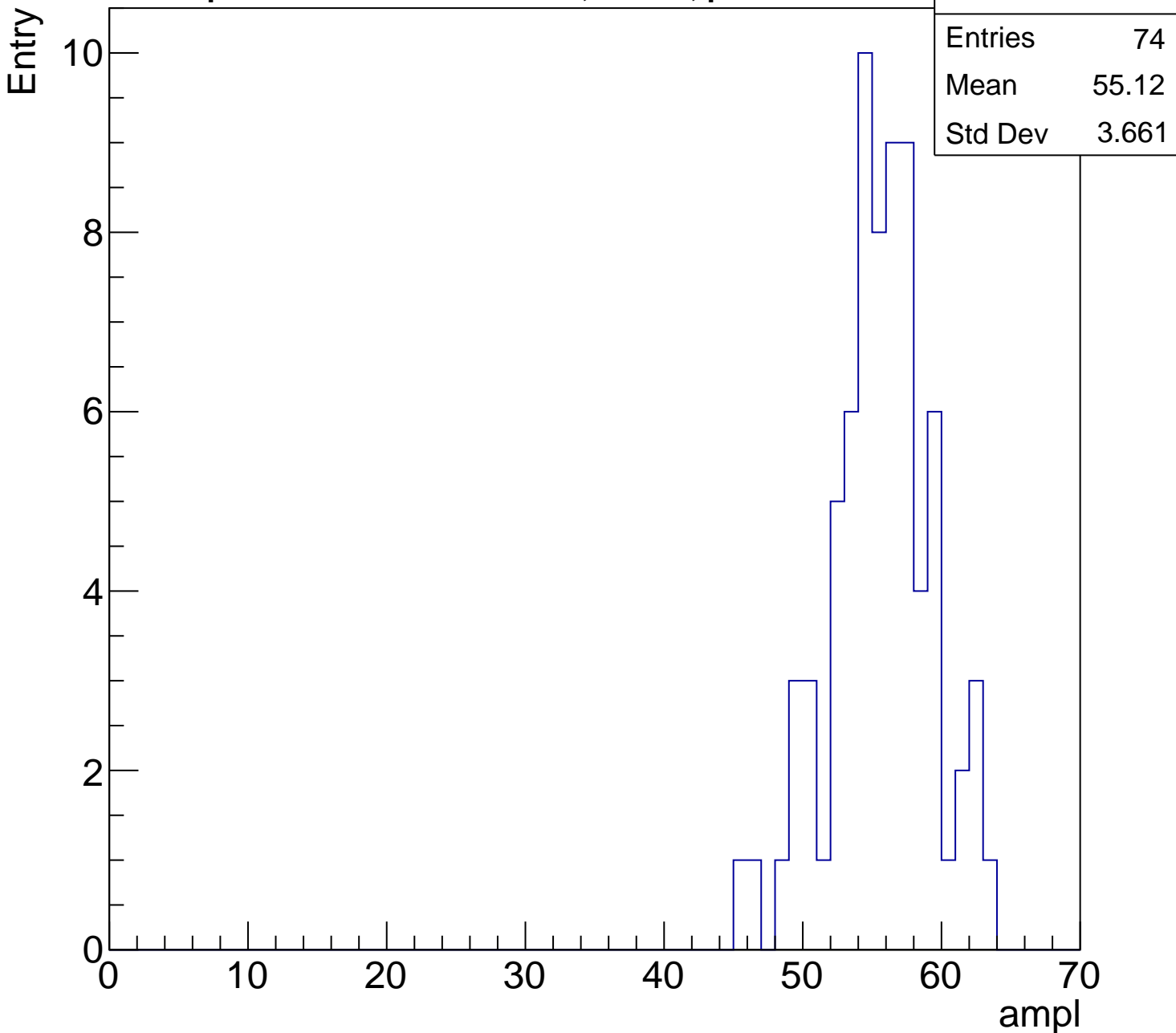
Entries	74
Mean	55.12
Std Dev	3.661

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L102S, U20-ch48, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

7

6

5

4

3

2

1

0

Entries	34
Mean	60.35
Std Dev	1.954

ampl

0

10

20

30

40

50

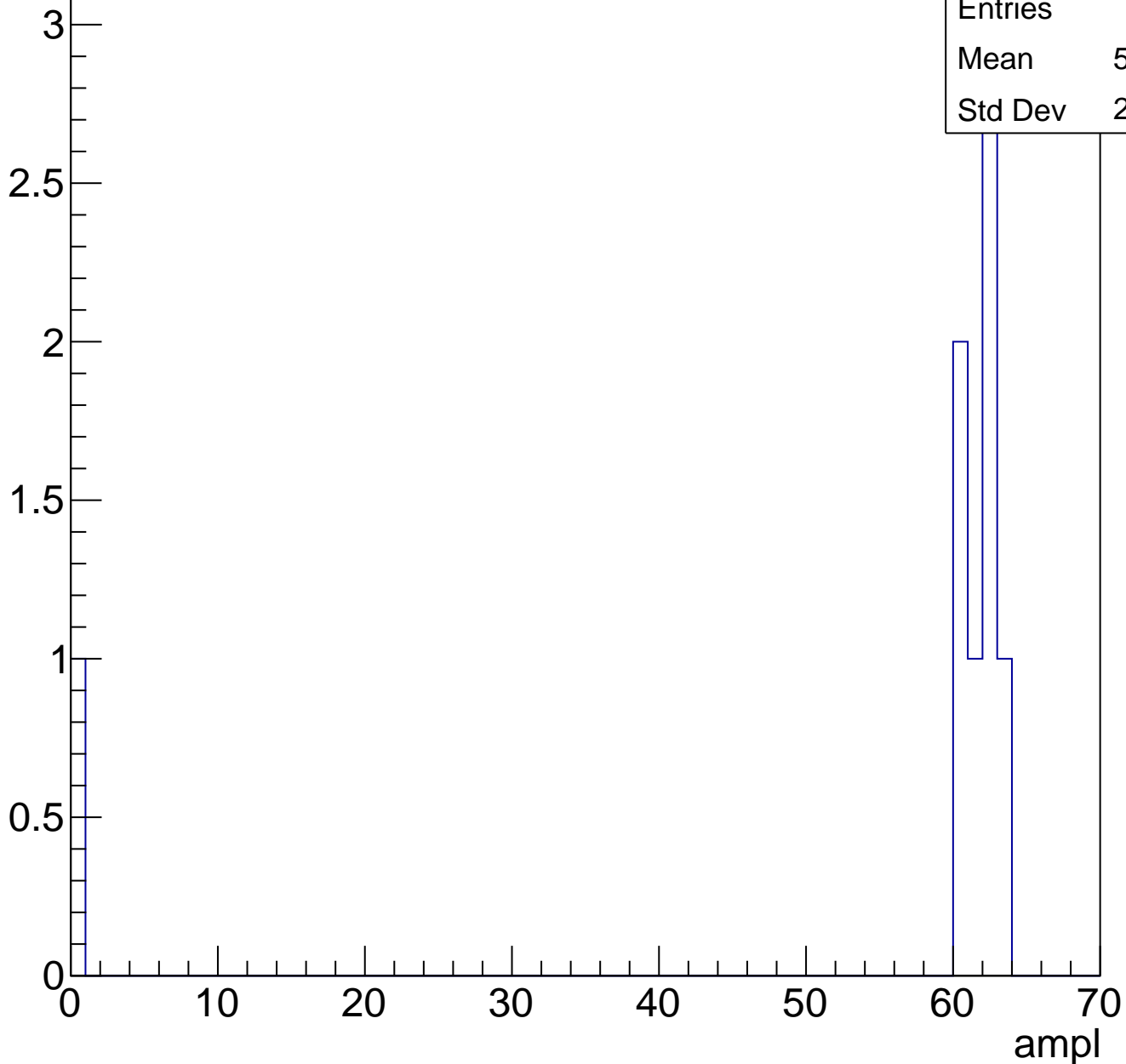
60

70

# B1L102S, U20-ch48, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U20-ch48, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch49, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	71
Mean	29.9
Std Dev	4.928

**Gaus mean : 30.5745**

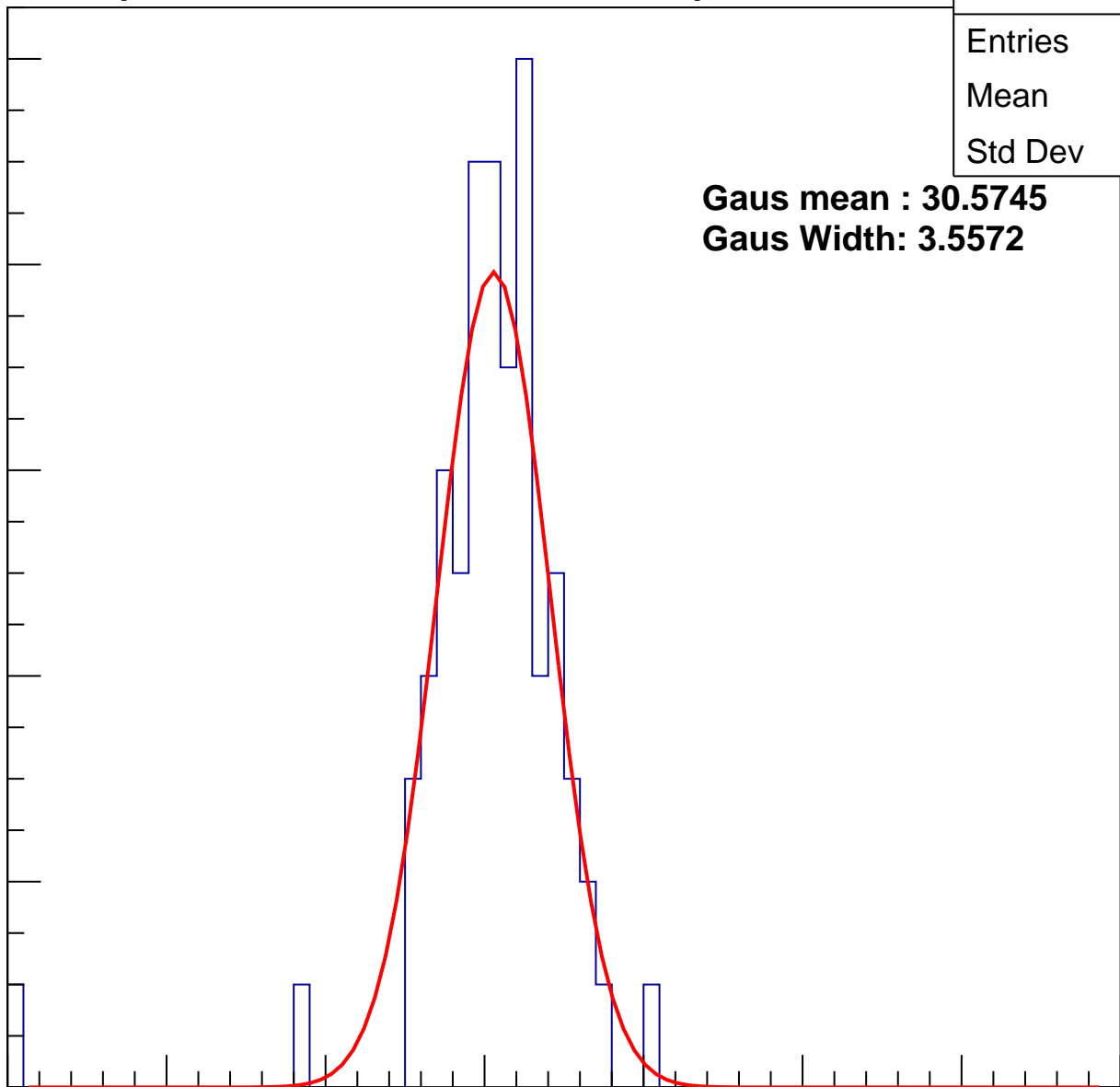
**Gaus Width: 3.5572**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



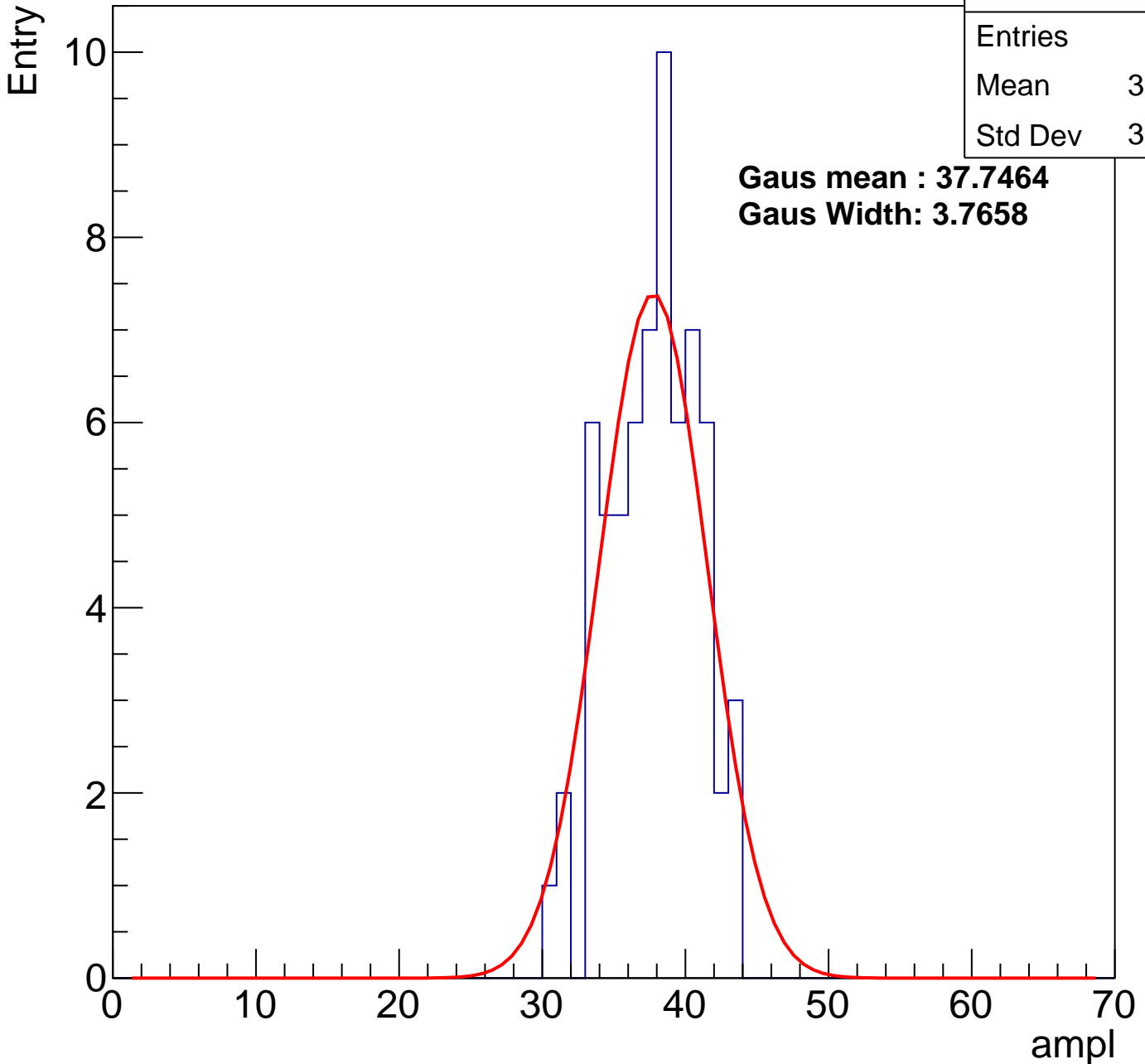
# B1L102S, U20-ch49, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	66
Mean	37.32
Std Dev	3.095

**Gaus mean : 37.7464**

**Gaus Width: 3.7658**



# B1L102S, U20-ch49, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	80
Mean	44.04
Std Dev	3.611

**Gaus mean : 45.0107**

**Gaus Width: 3.1847**

10

8

6

4

2

0

0

10

20

30

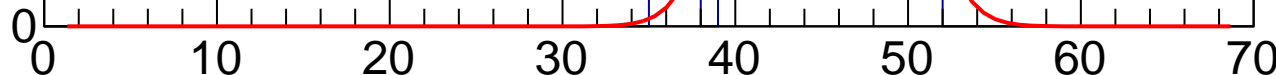
40

50

60

70

ampl

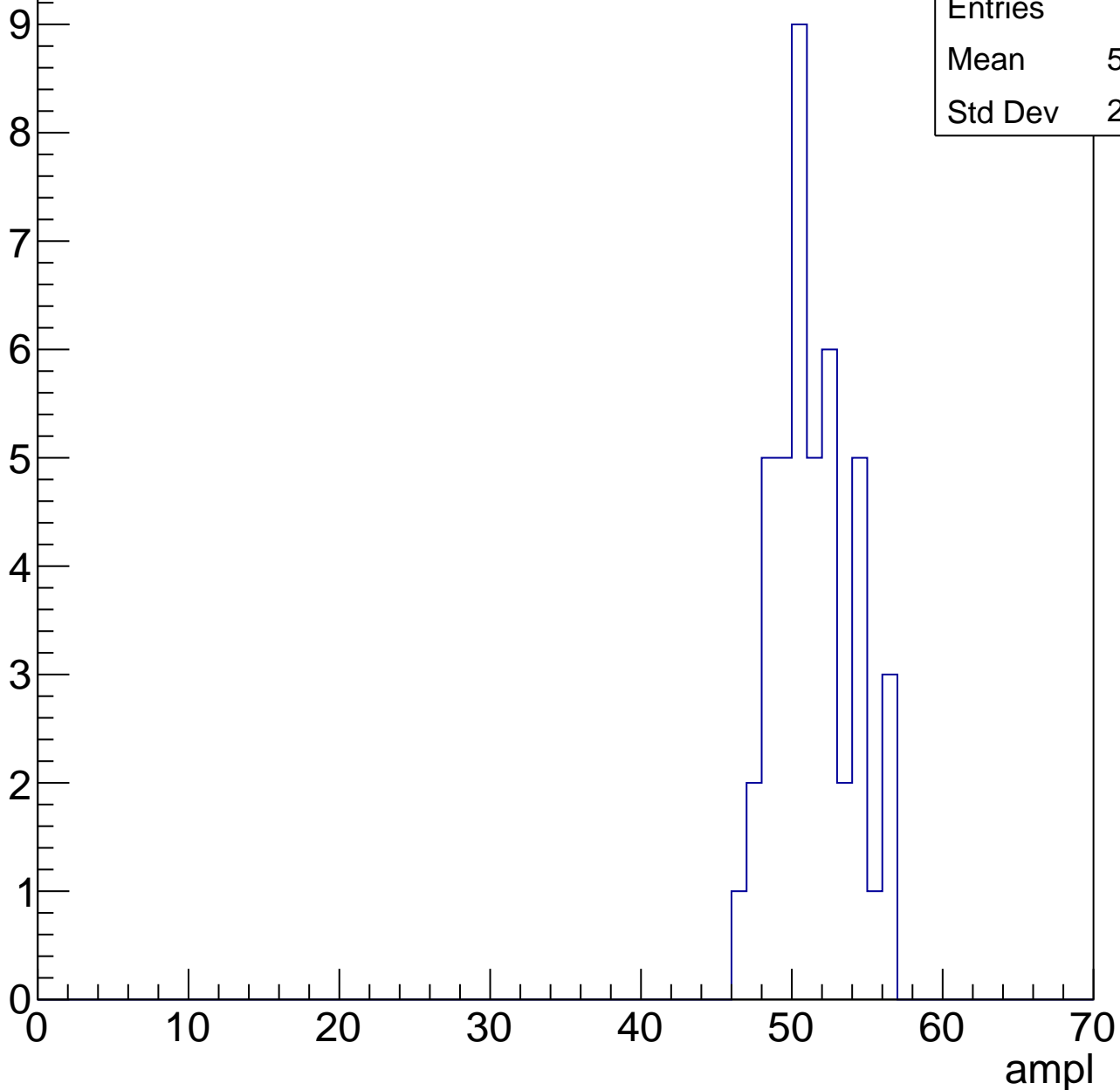


# B1L102S, U20-ch49, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	44
Mean	50.93
Std Dev	2.526

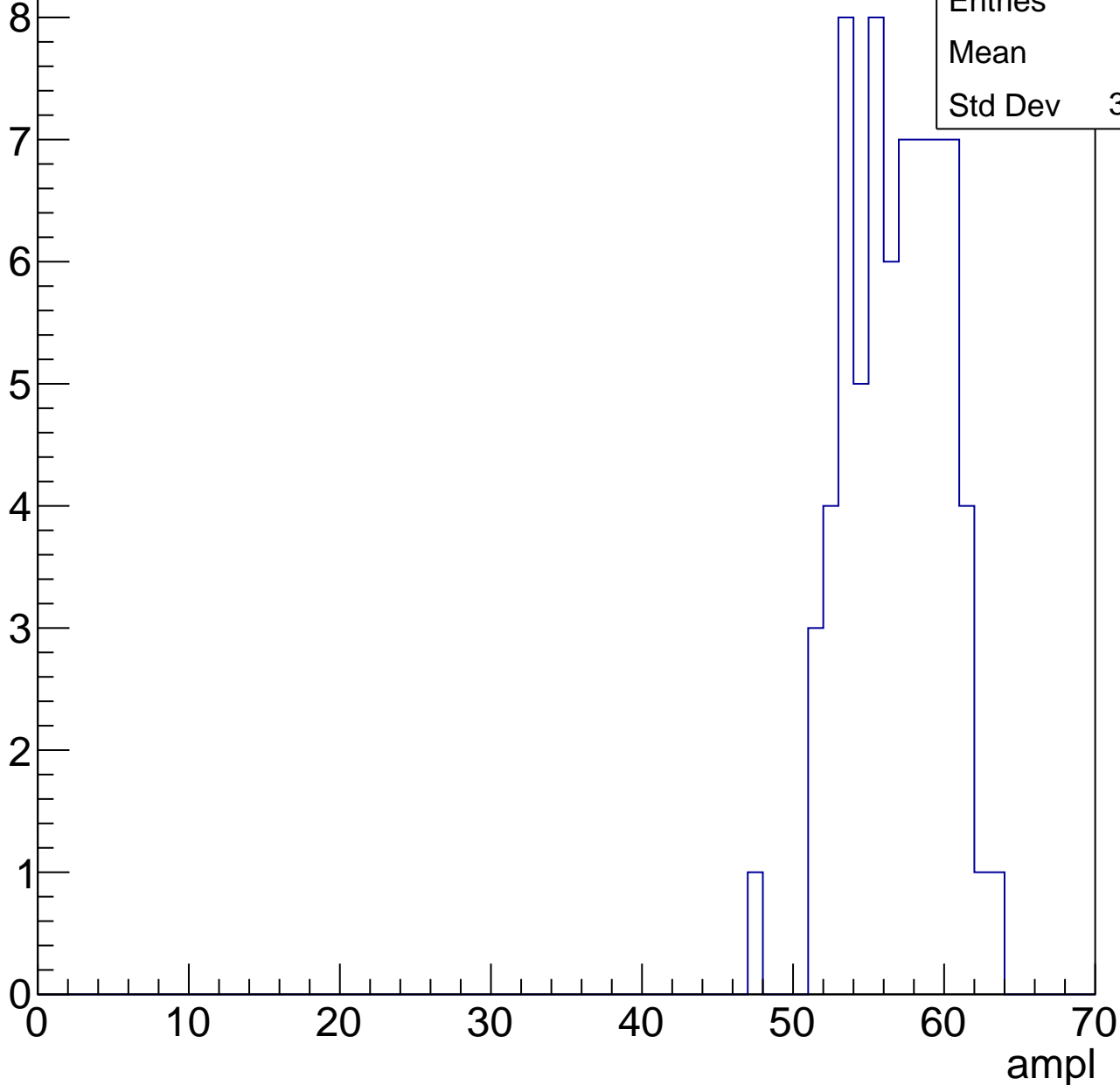


# B1L102S, U20-ch49, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	56.3
Std Dev	3.205

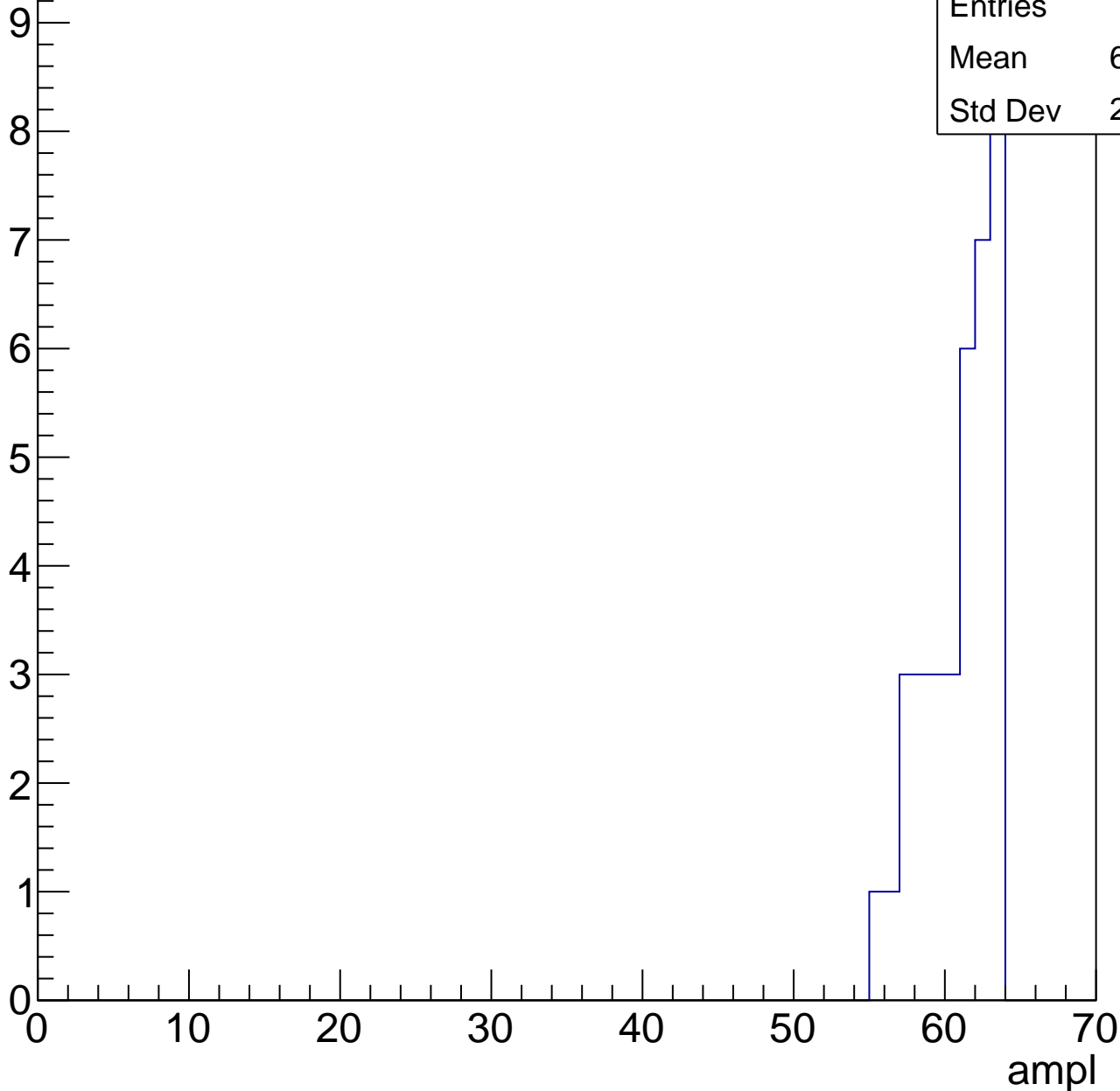


# B1L102S, U20-ch49, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

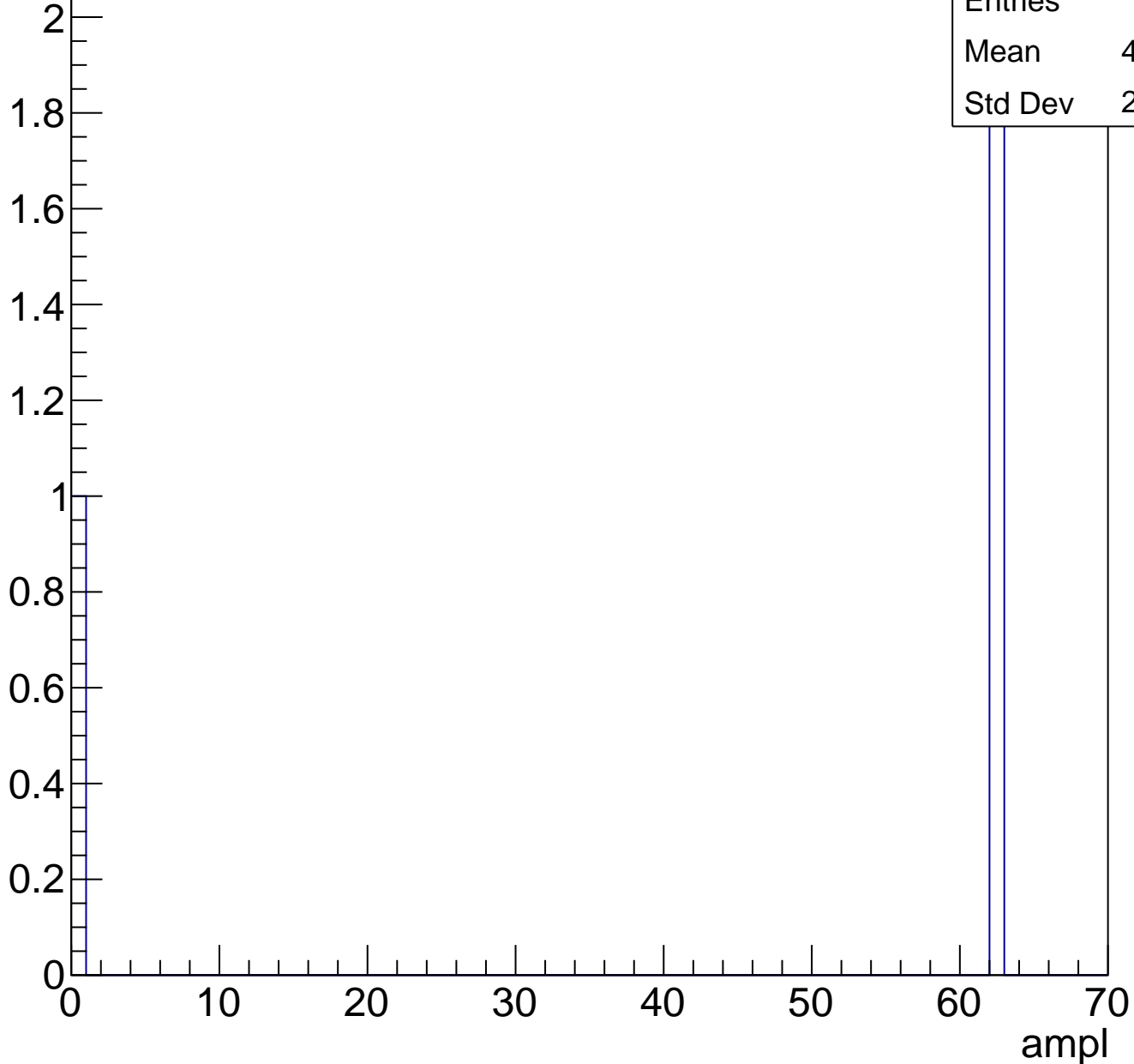
Entries	36
Mean	60.56
Std Dev	2.278



# B1L102S, U20-ch49, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U20-ch49, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L102S, U20-ch50, adc0

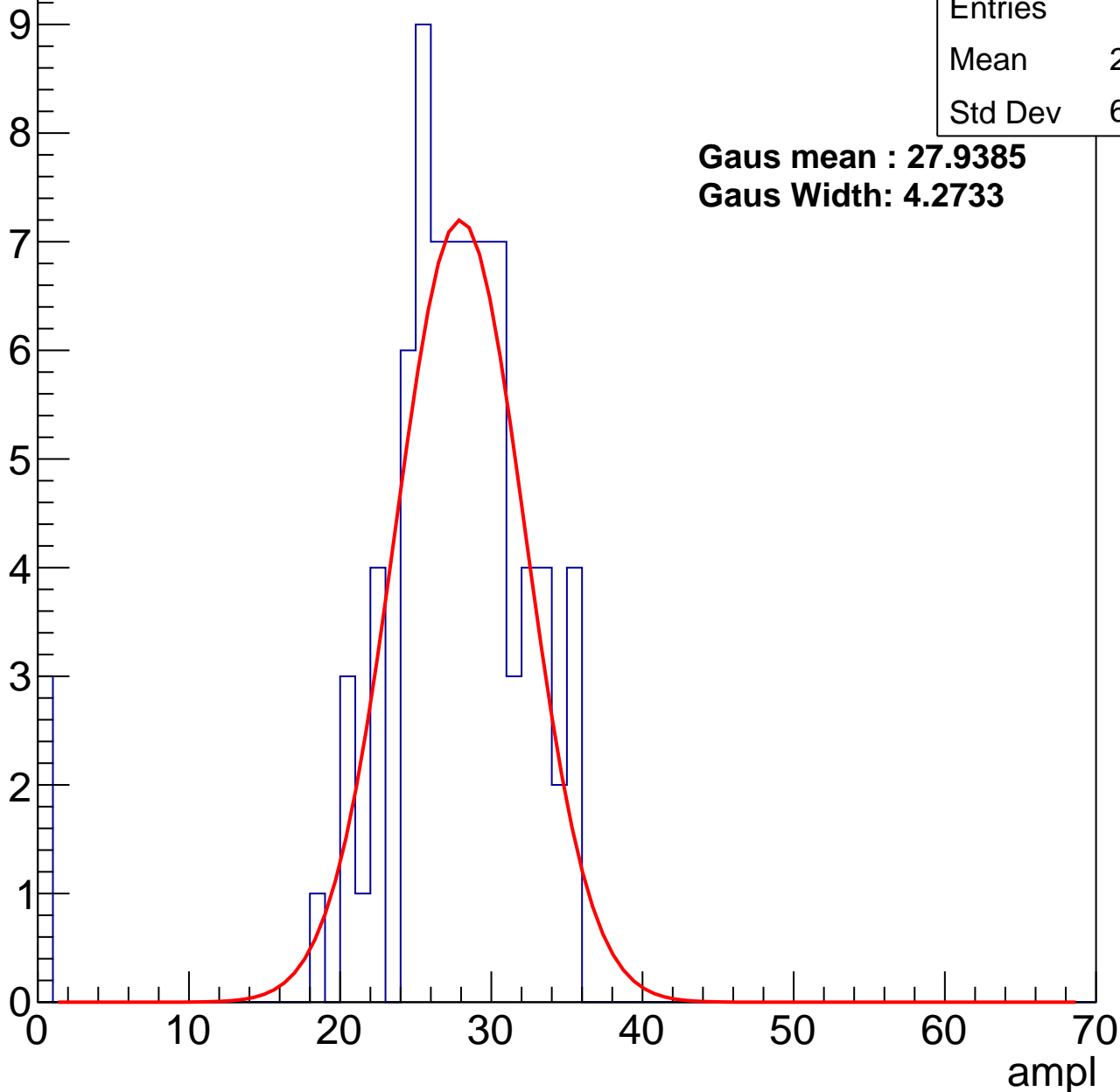
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	79
Mean	26.54
Std Dev	6.537

**Gaus mean : 27.9385**

**Gaus Width: 4.2733**



# B1L102S, U20-ch50, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	65
Mean	34.55
Std Dev	3.451

**Gaus mean : 35.3596**

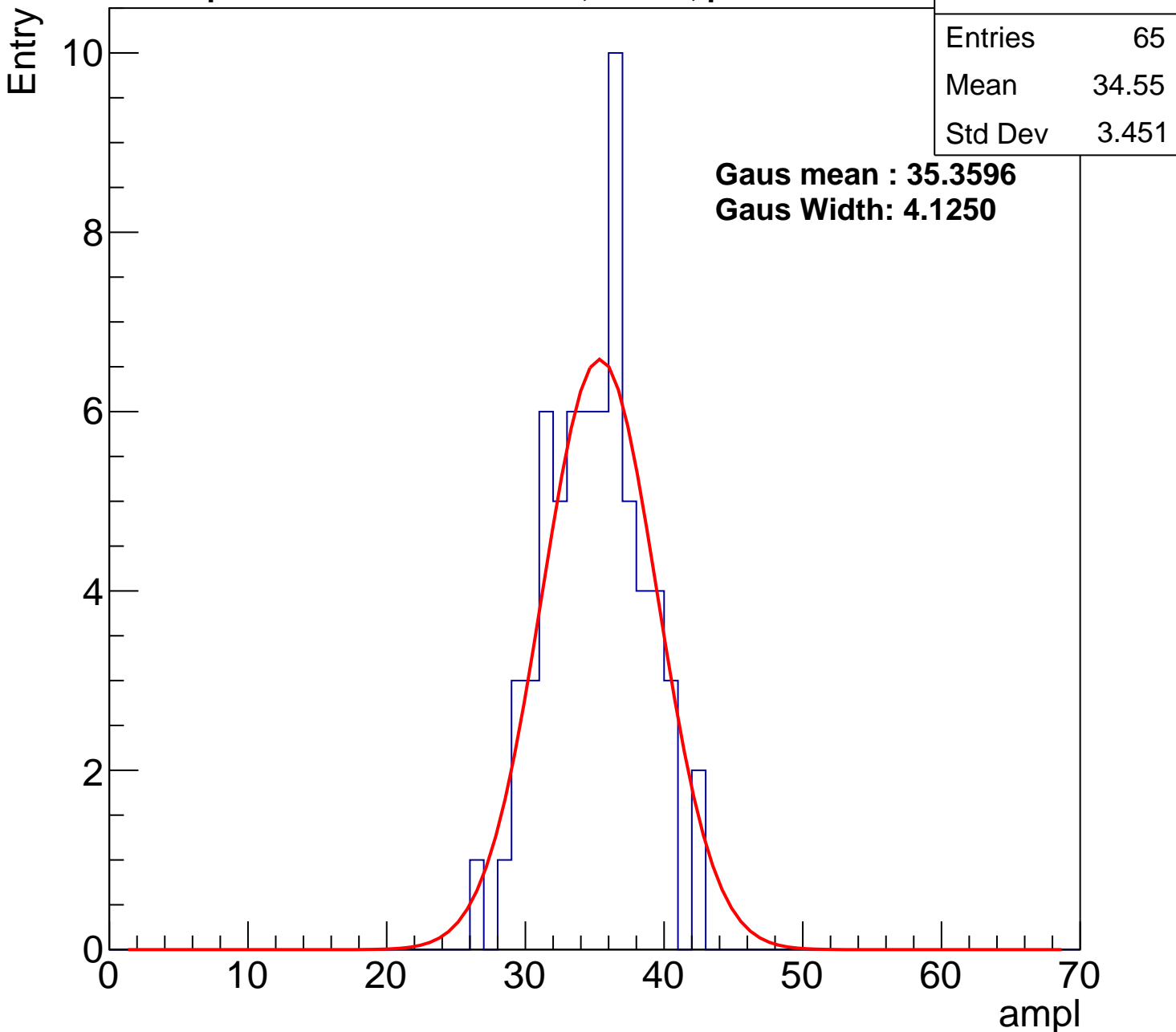
**Gaus Width: 4.1250**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U20-ch50, adc2

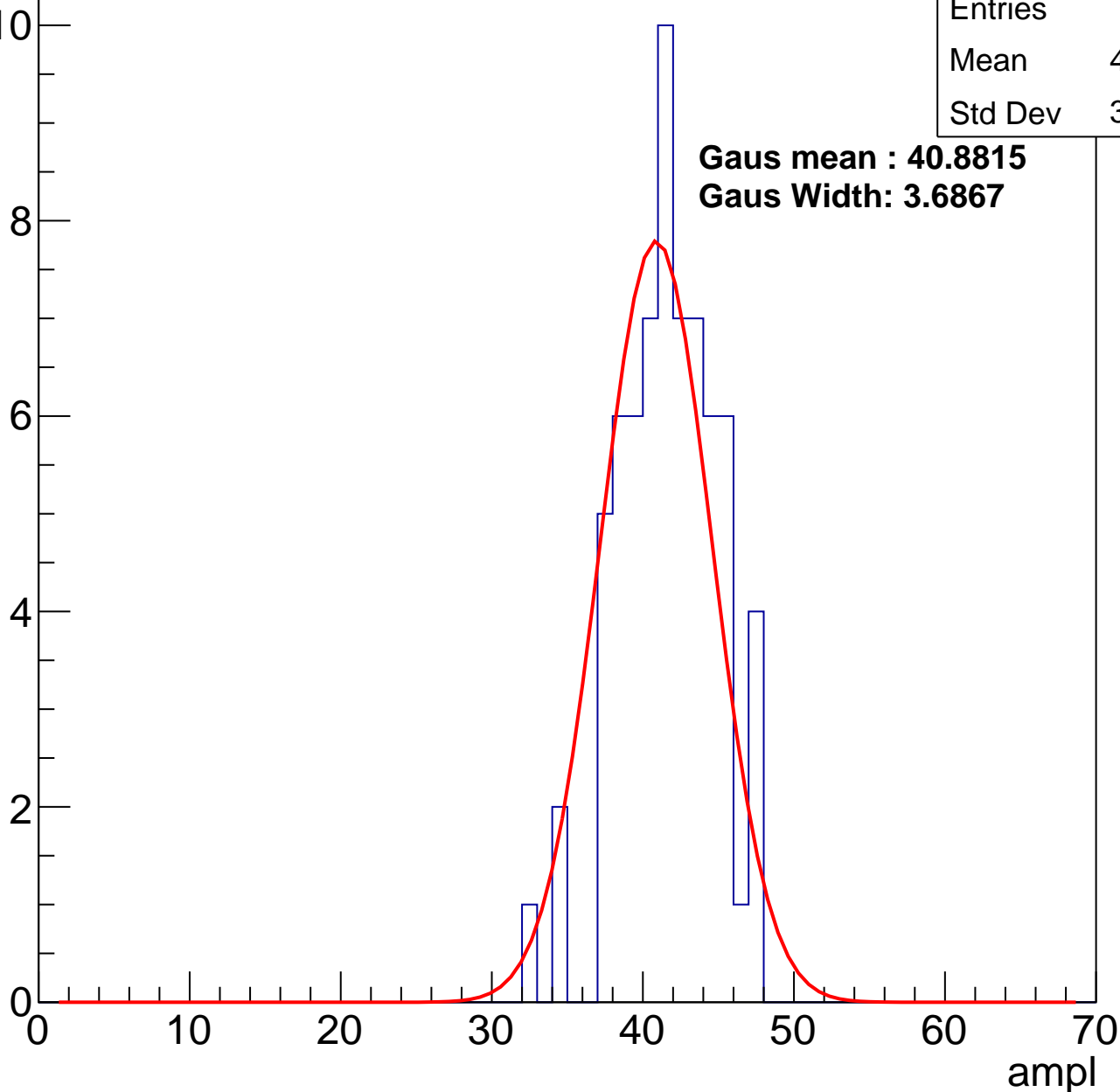
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	41.18
Std Dev	3.199

**Gaus mean : 40.8815**

**Gaus Width: 3.6867**



# B1L102S, U20-ch50, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

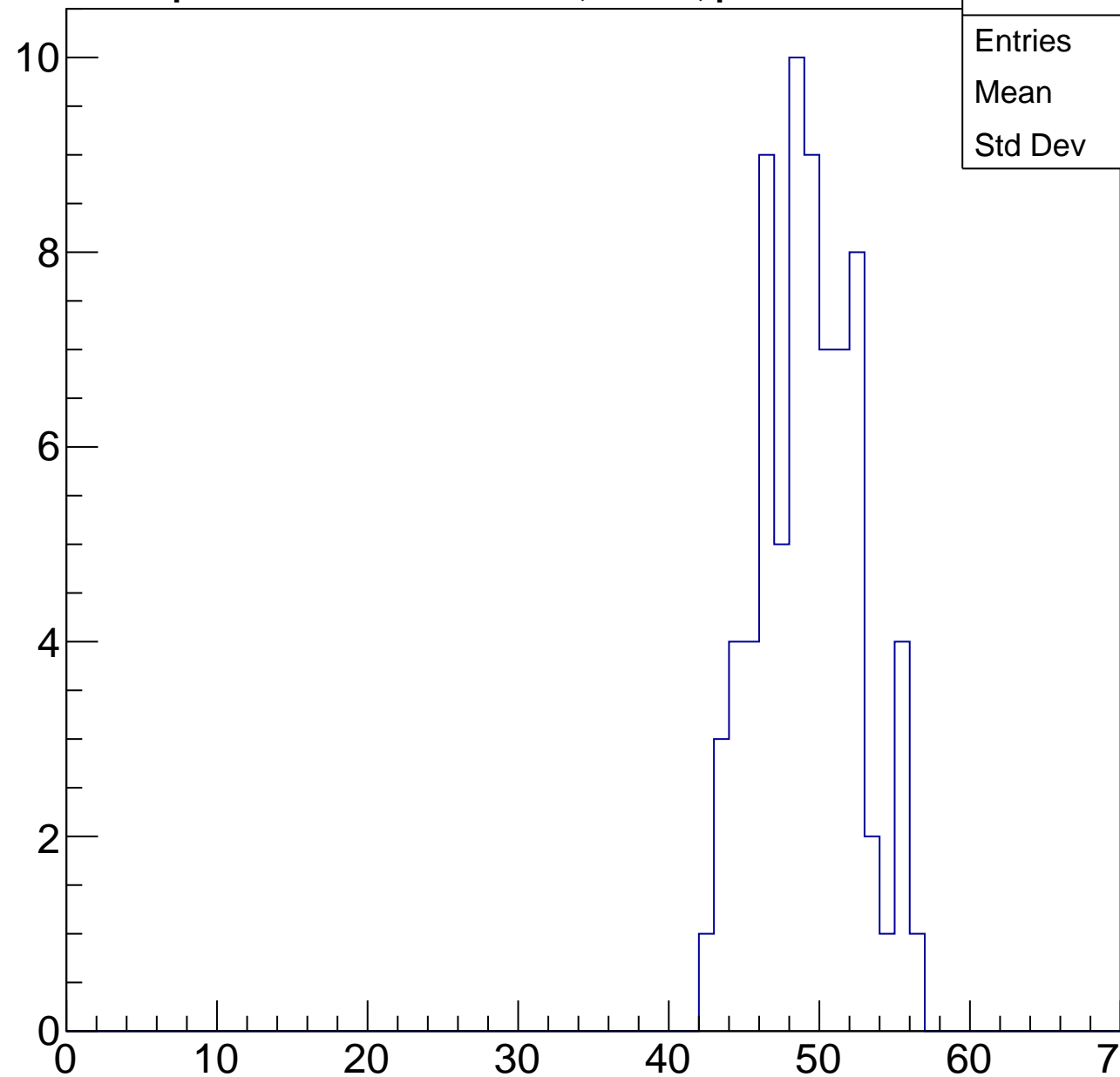
Entries	75
Mean	48.75
Std Dev	3.234

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

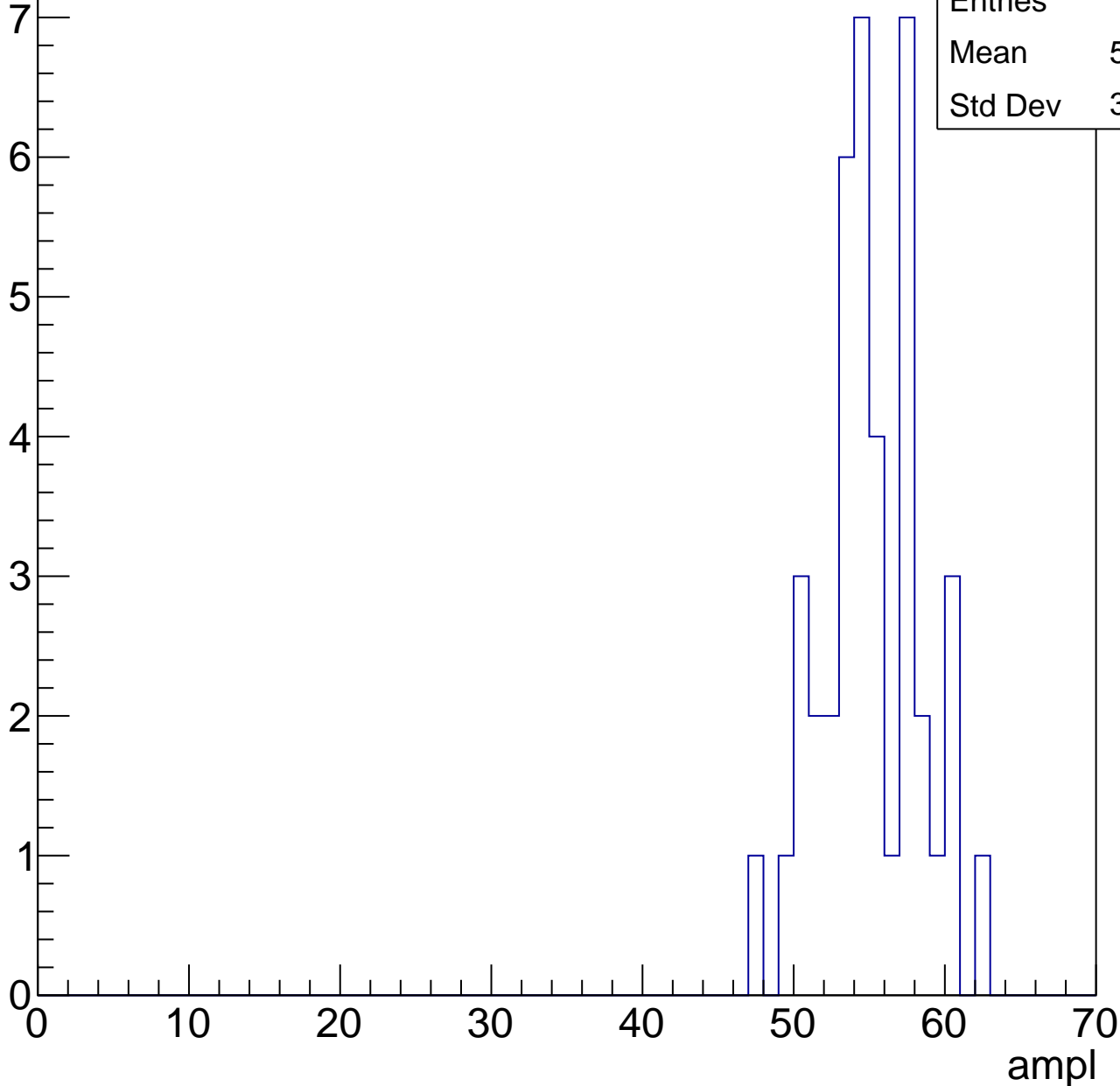


# B1L102S, U20-ch50, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	41
Mean	54.63
Std Dev	3.267

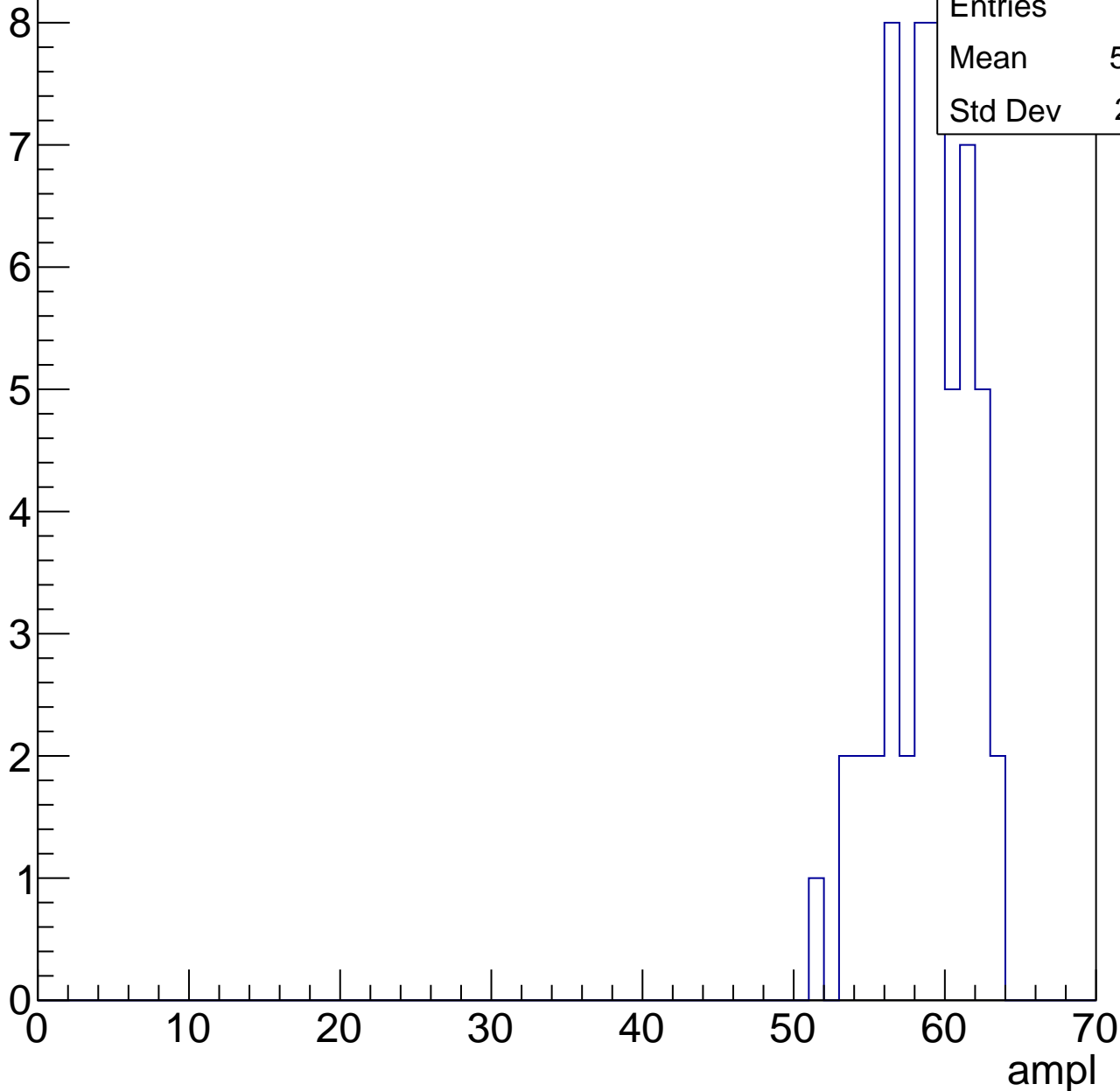


# B1L102S, U20-ch50, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	58.38
Std Dev	2.761

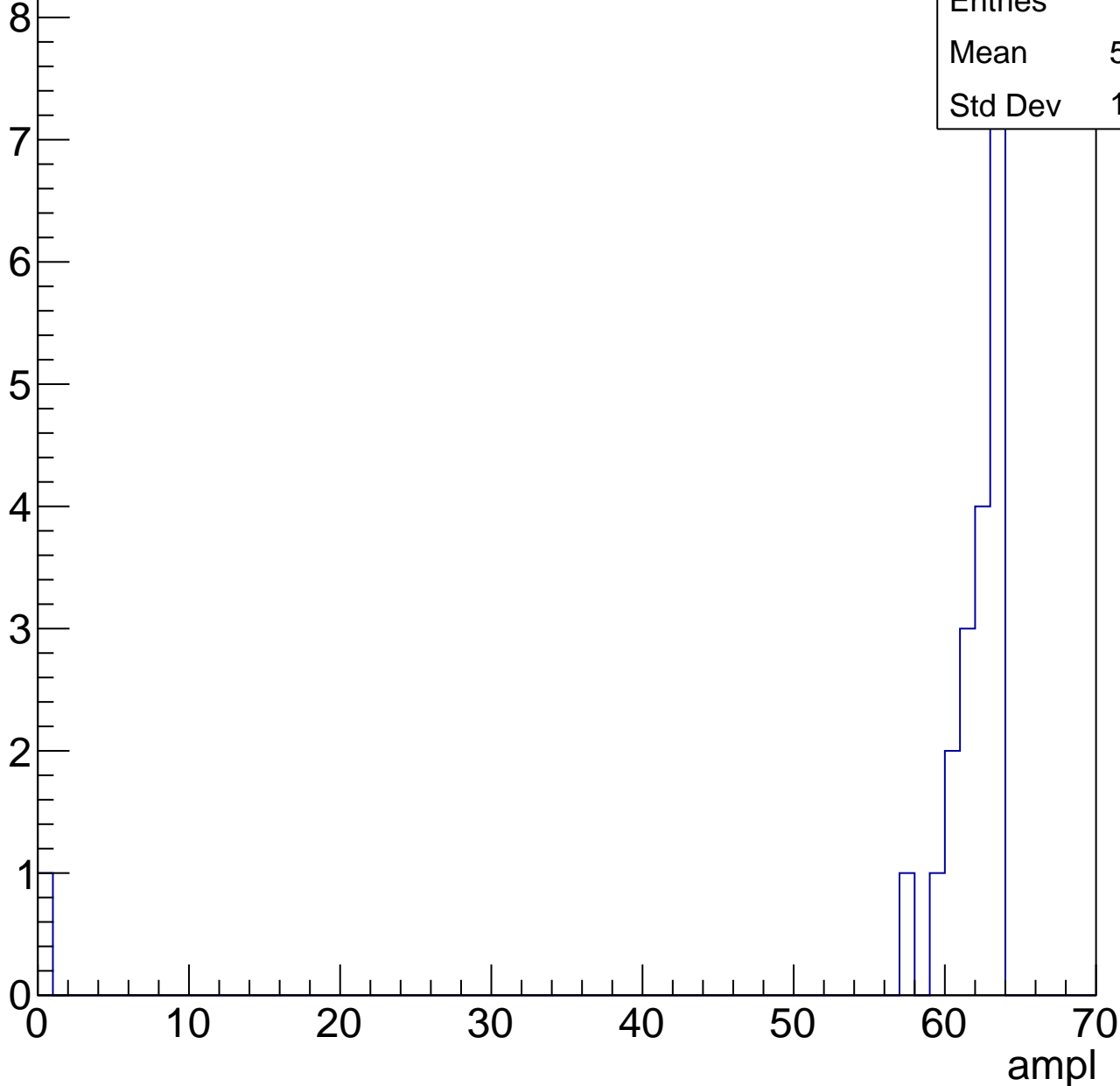


# B1L102S, U20-ch50, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	20
Mean	58.55
Std Dev	13.53





# B1L102S, U20-ch50, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch51, adc0

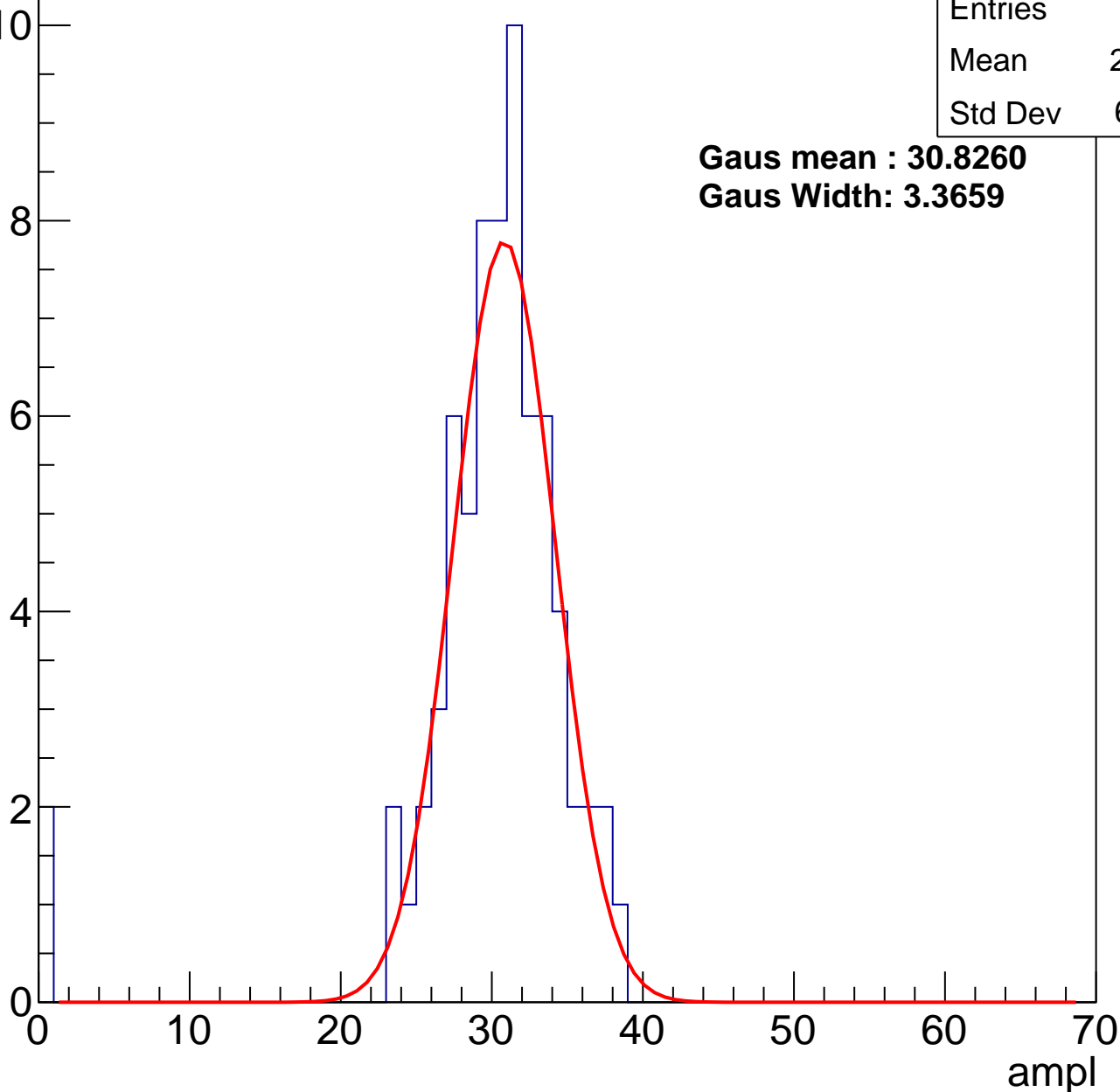
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	29.46
Std Dev	6.011

**Gaus mean : 30.8260**

**Gaus Width: 3.3659**



# B1L102S, U20-ch51, adc1

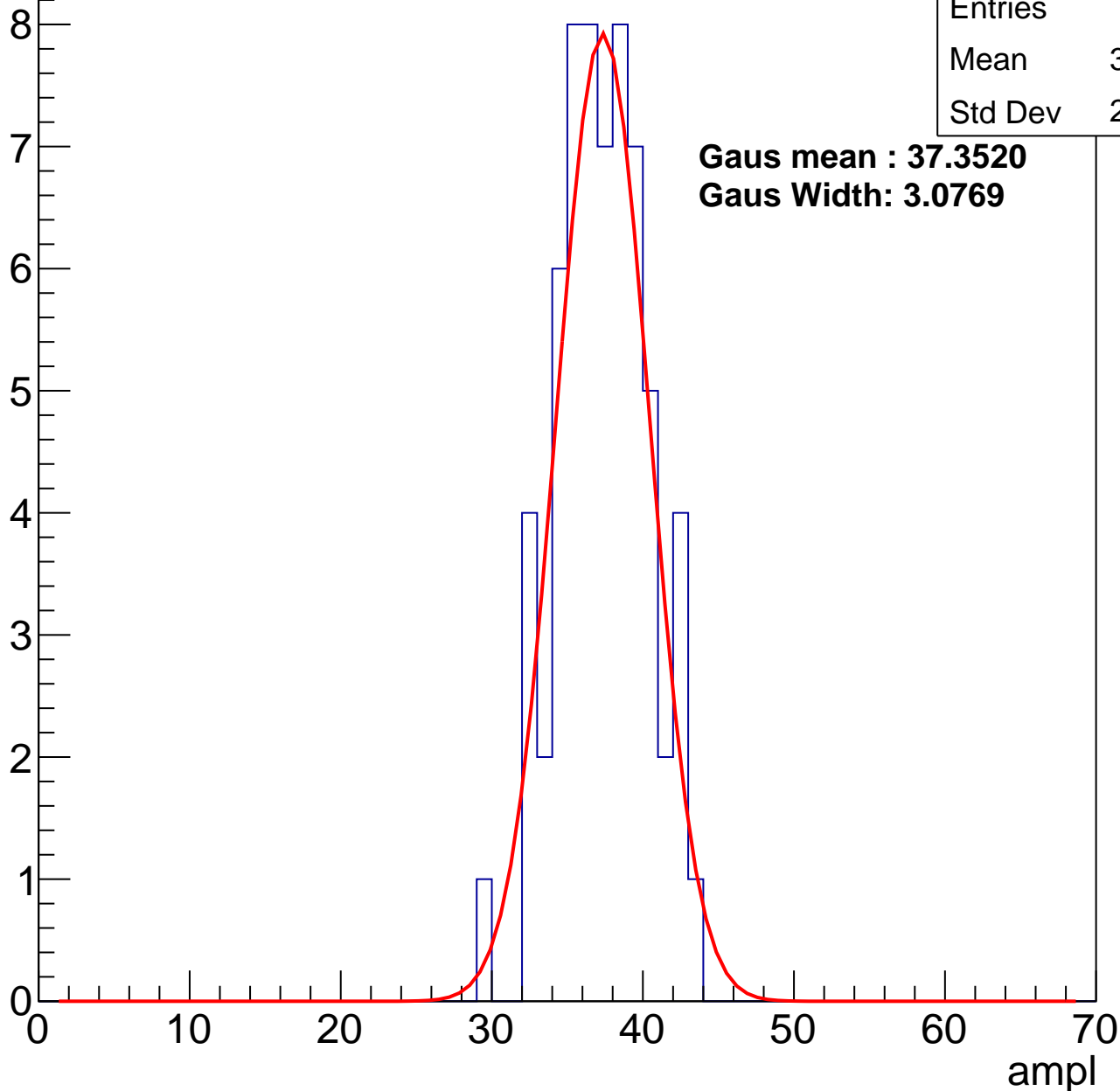
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	36.89
Std Dev	2.923

**Gaus mean : 37.3520**

**Gaus Width: 3.0769**



# B1L102S, U20-ch51, adc2

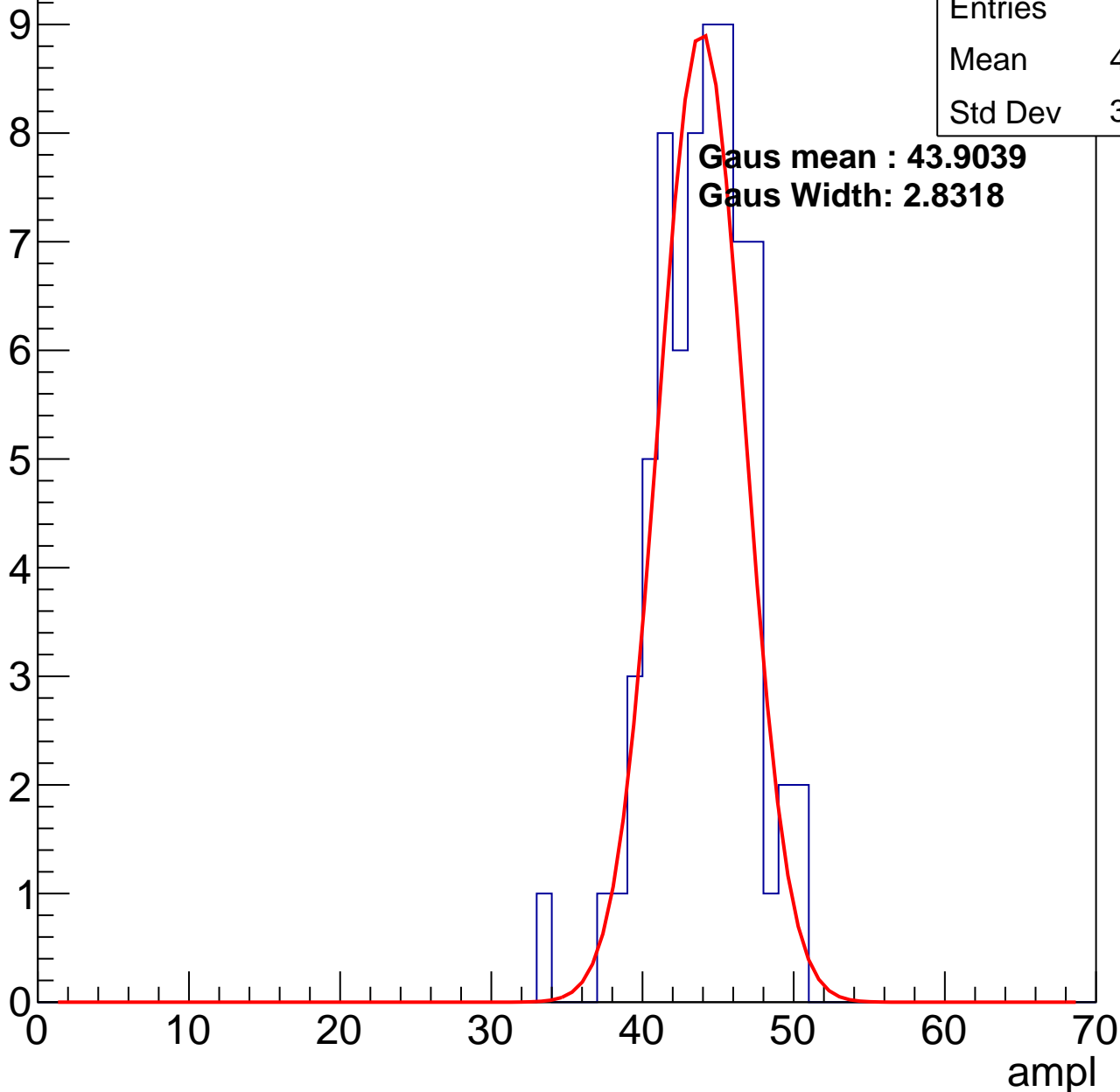
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	43.53
Std Dev	3.134

**Gaus mean : 43.9039**

**Gaus Width: 2.8318**

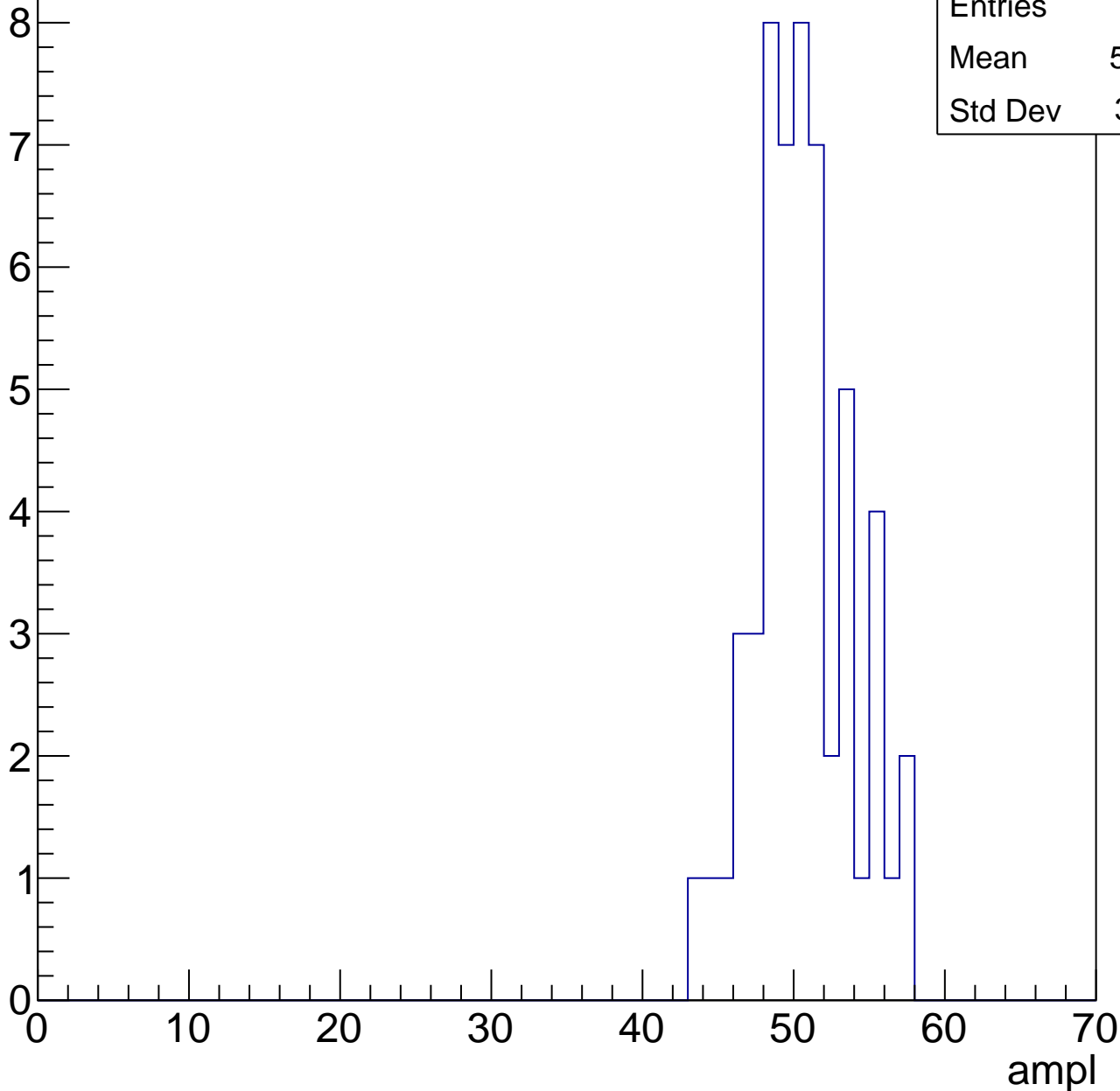


# B1L102S, U20-ch51, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	50.15
Std Dev	3.141

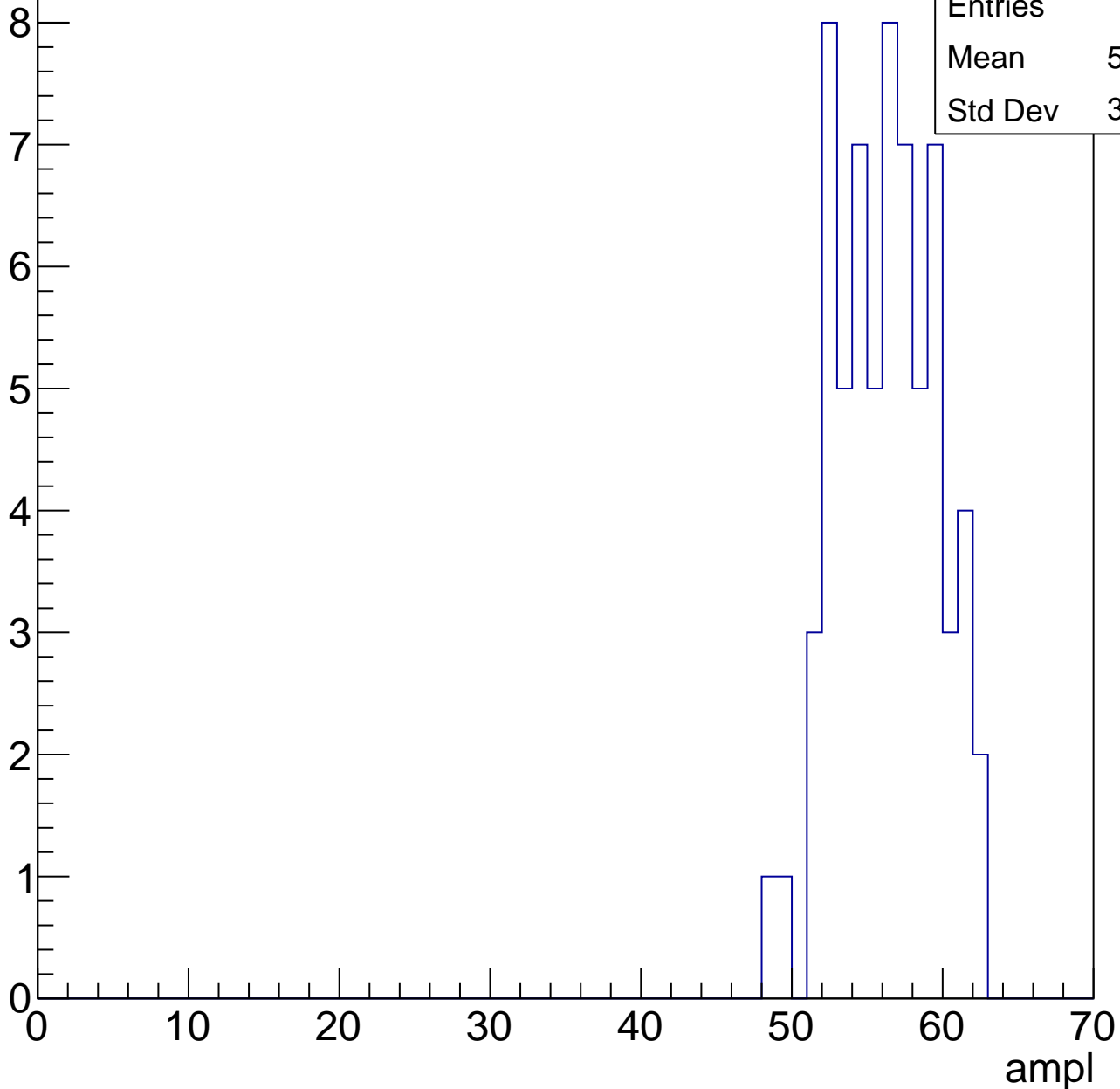


# B1L102S, U20-ch51, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	55.79
Std Dev	3.259

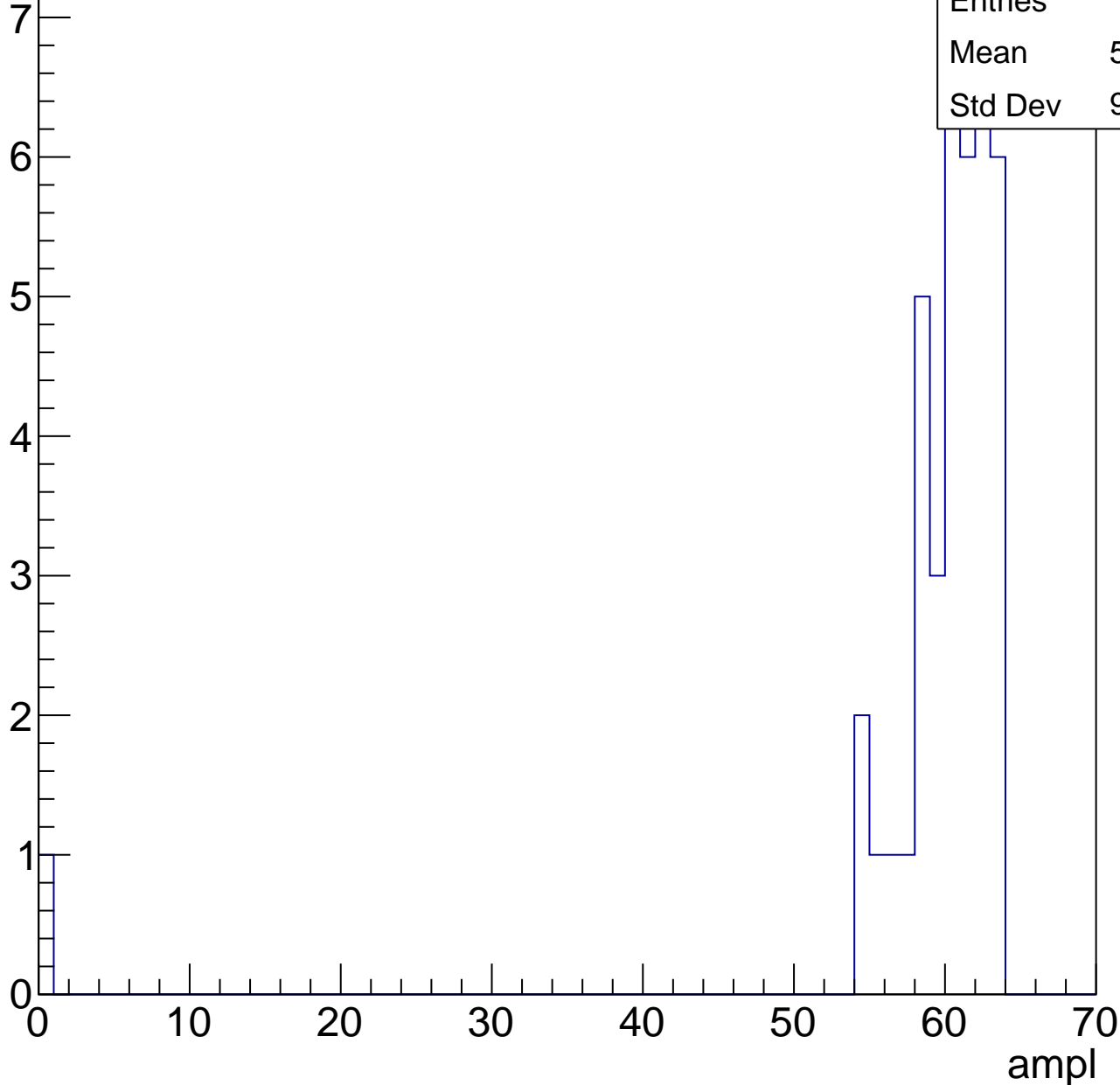


# B1L102S, U20-ch51, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

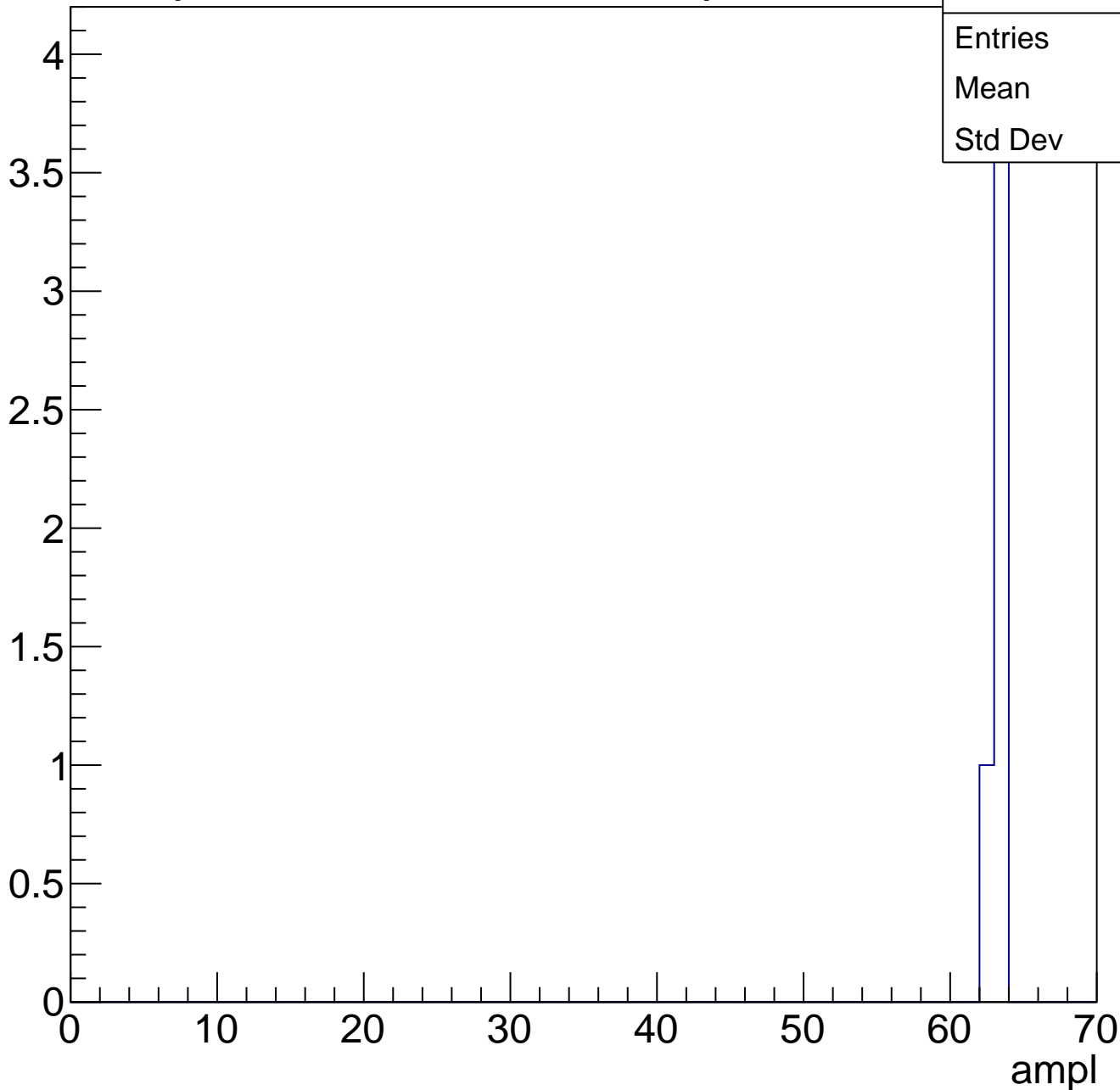
Entries	40
Mean	58.52
Std Dev	9.677



# B1L102S, U20-ch51, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



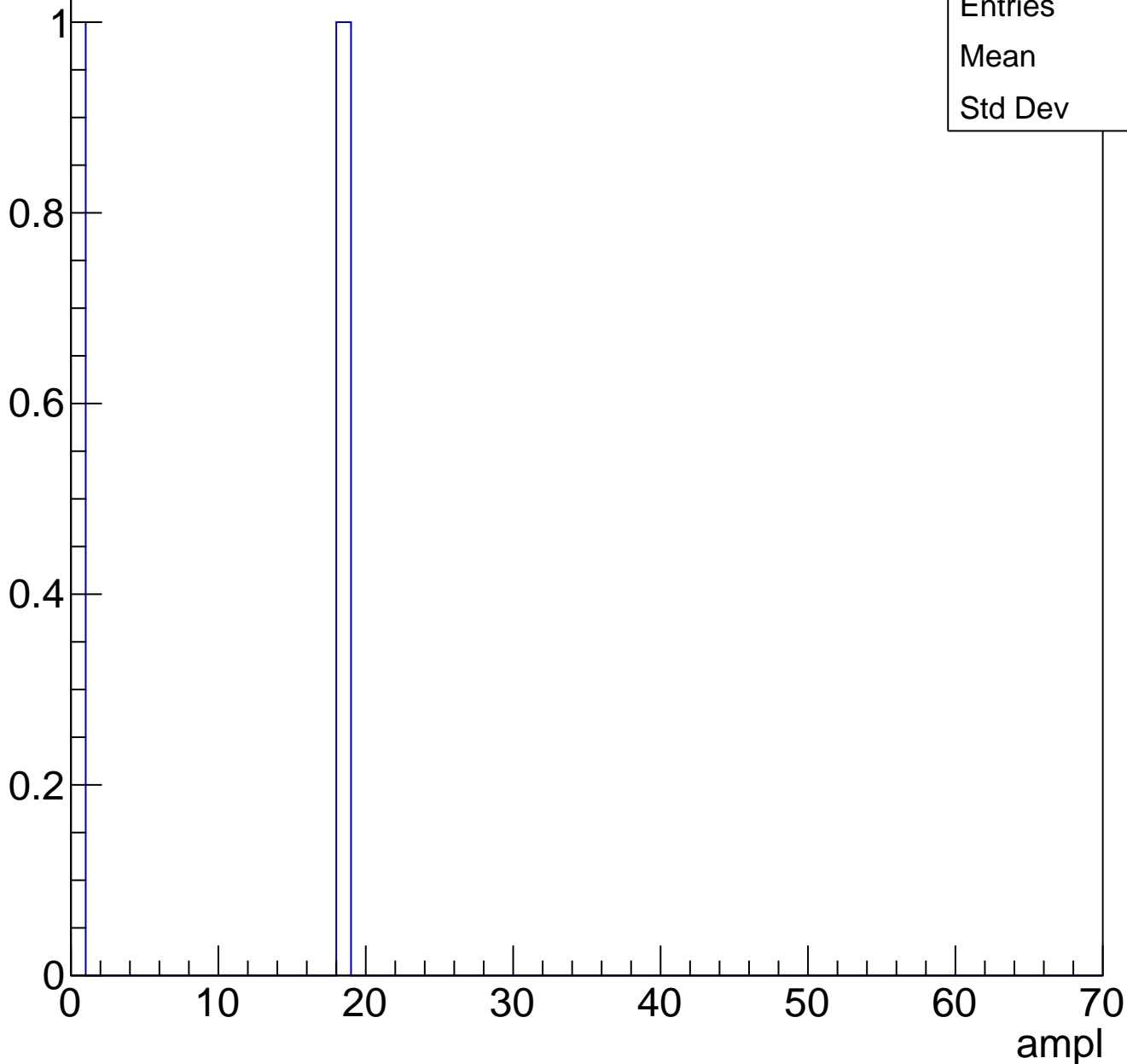
Entries	5
Mean	62.8
Std Dev	0.4



# B1L102S, U20-ch51, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch52, adc0

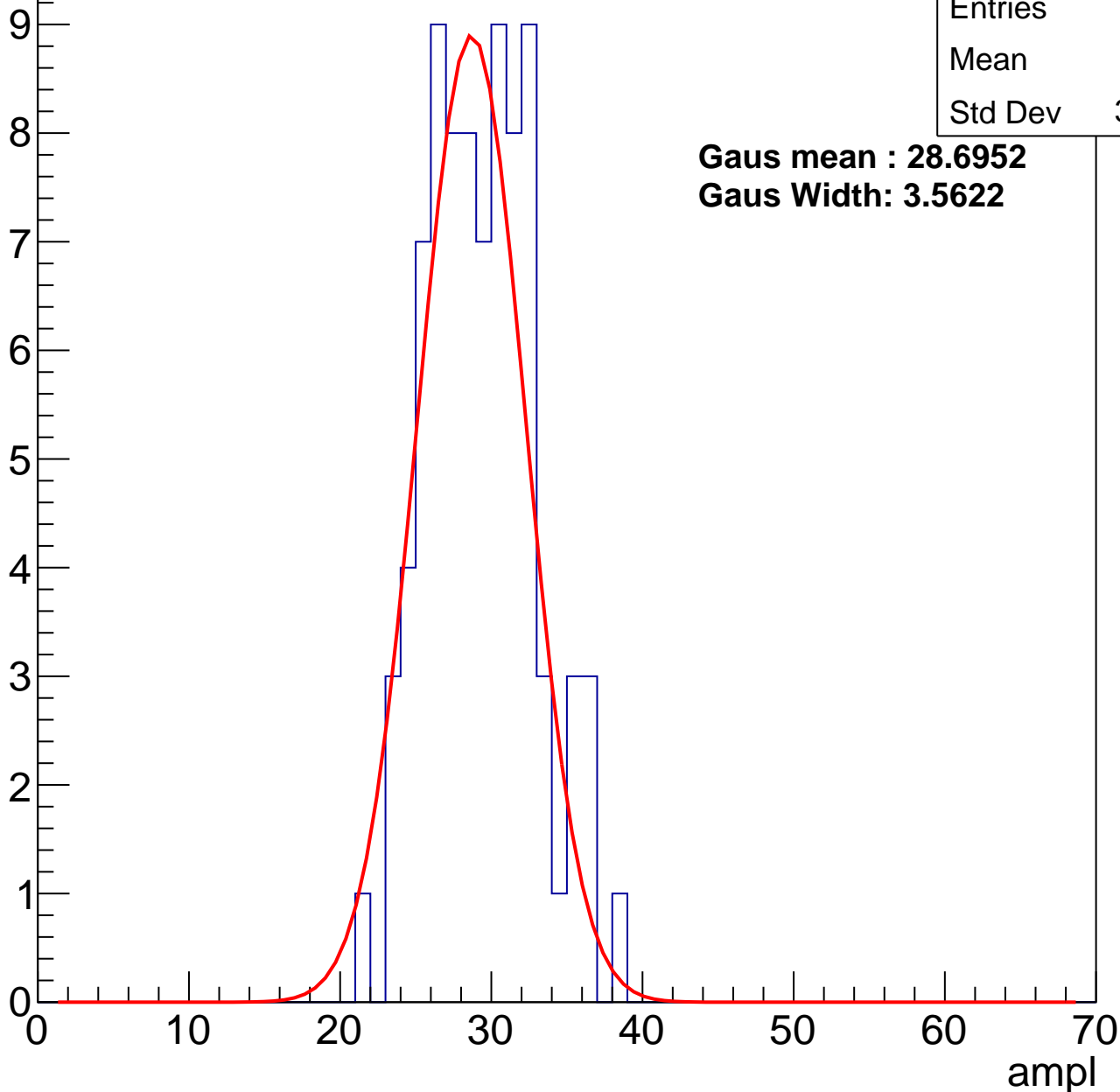
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	84
Mean	28.9
Std Dev	3.511

**Gaus mean : 28.6952**

**Gaus Width: 3.5622**



# B1L102S, U20-ch52, adc1

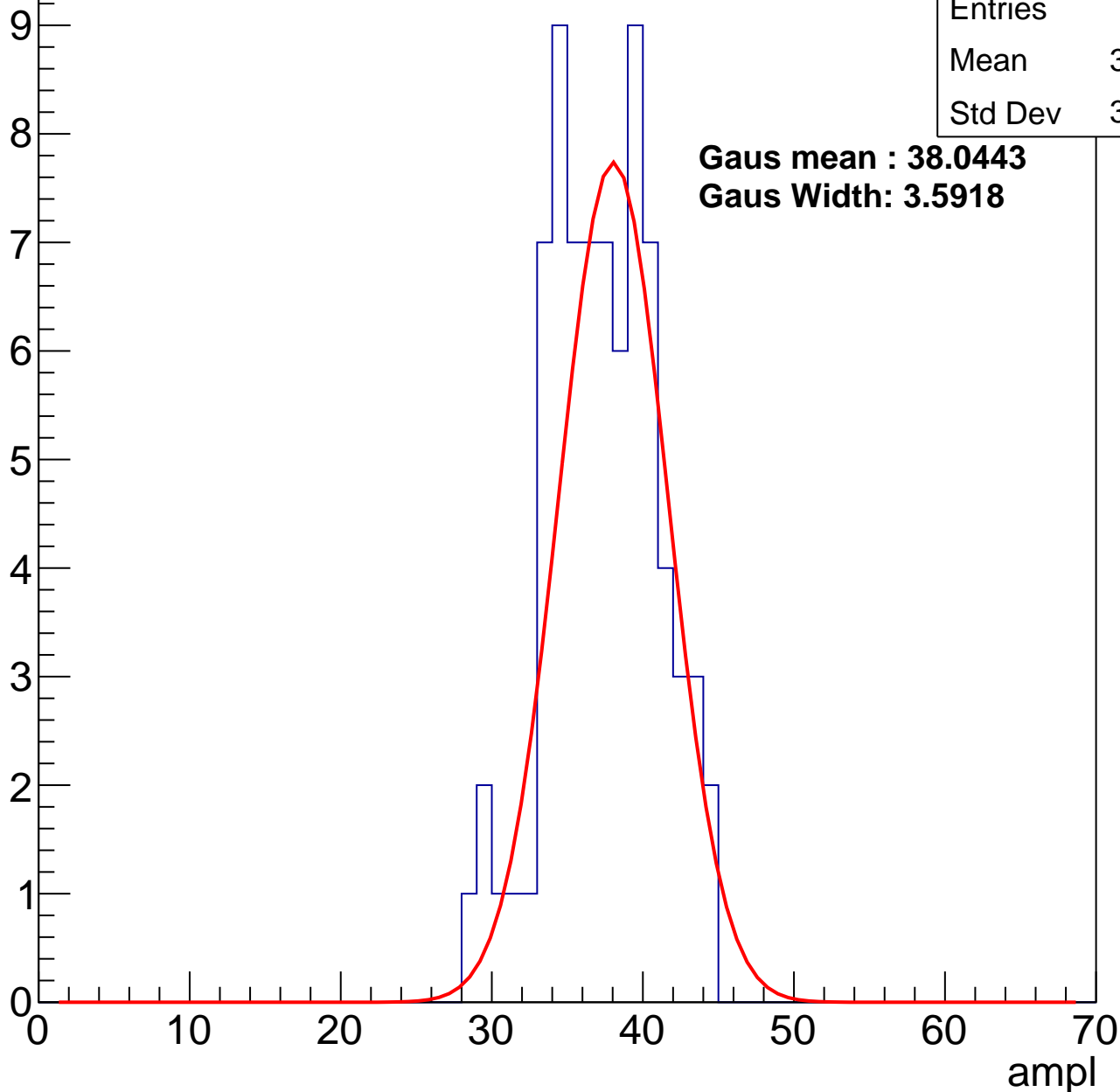
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	36.86
Std Dev	3.596

**Gaus mean : 38.0443**

**Gaus Width: 3.5918**



# B1L102S, U20-ch52, adc2

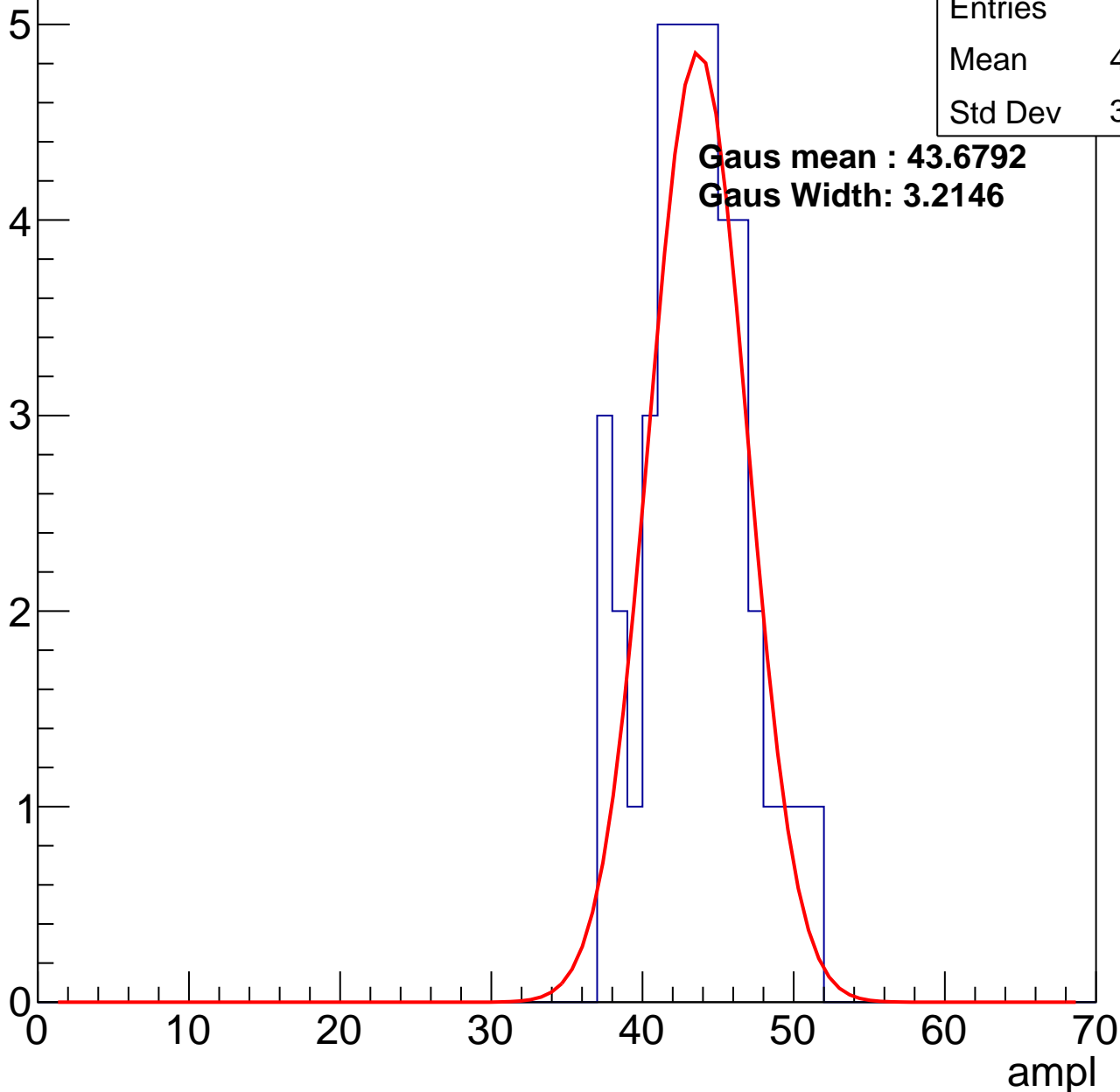
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	43
Mean	43.07
Std Dev	3.372

**Gaus mean : 43.6792**

**Gaus Width: 3.2146**

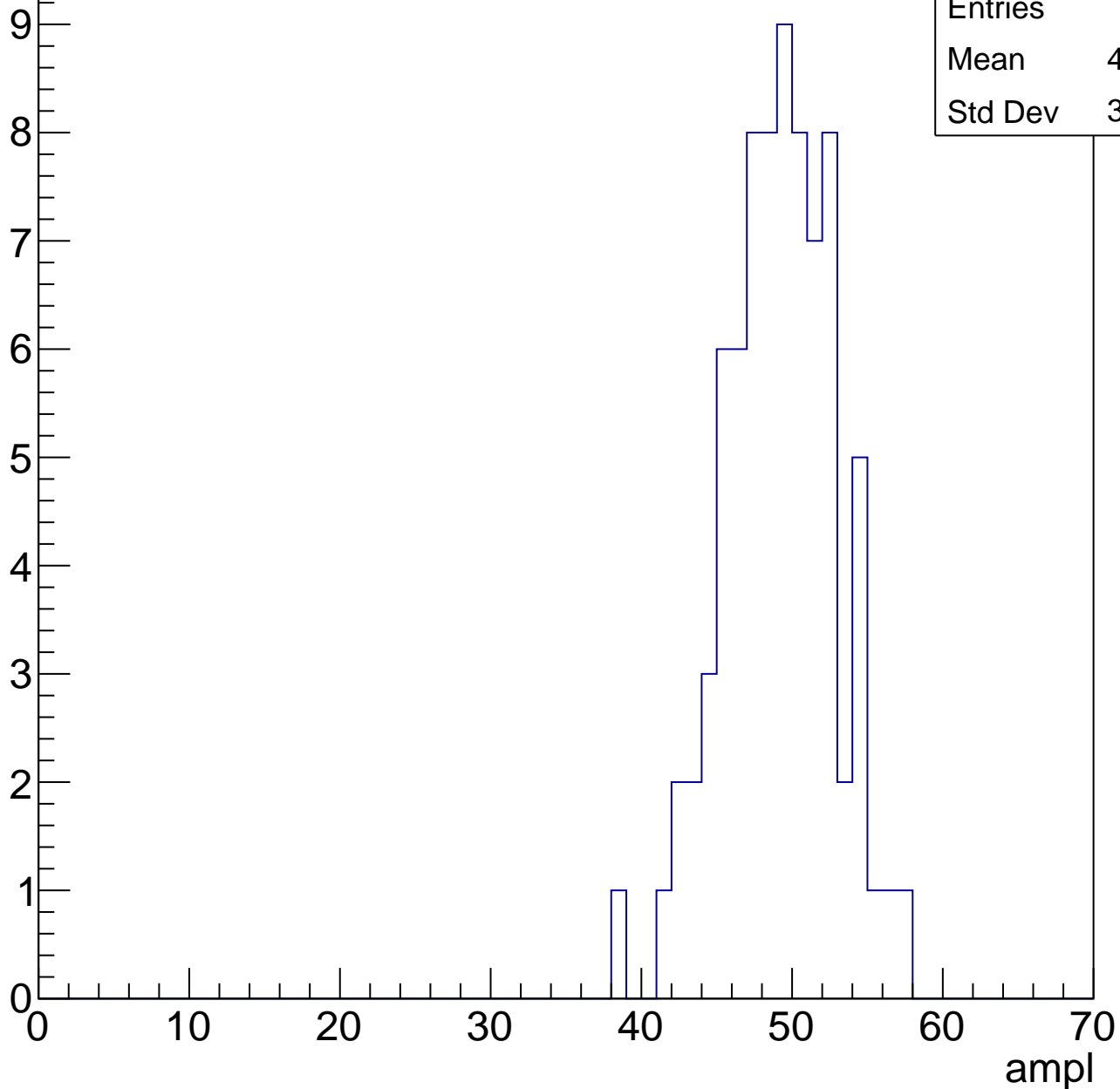


# B1L102S, U20-ch52, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	79
Mean	48.67
Std Dev	3.603

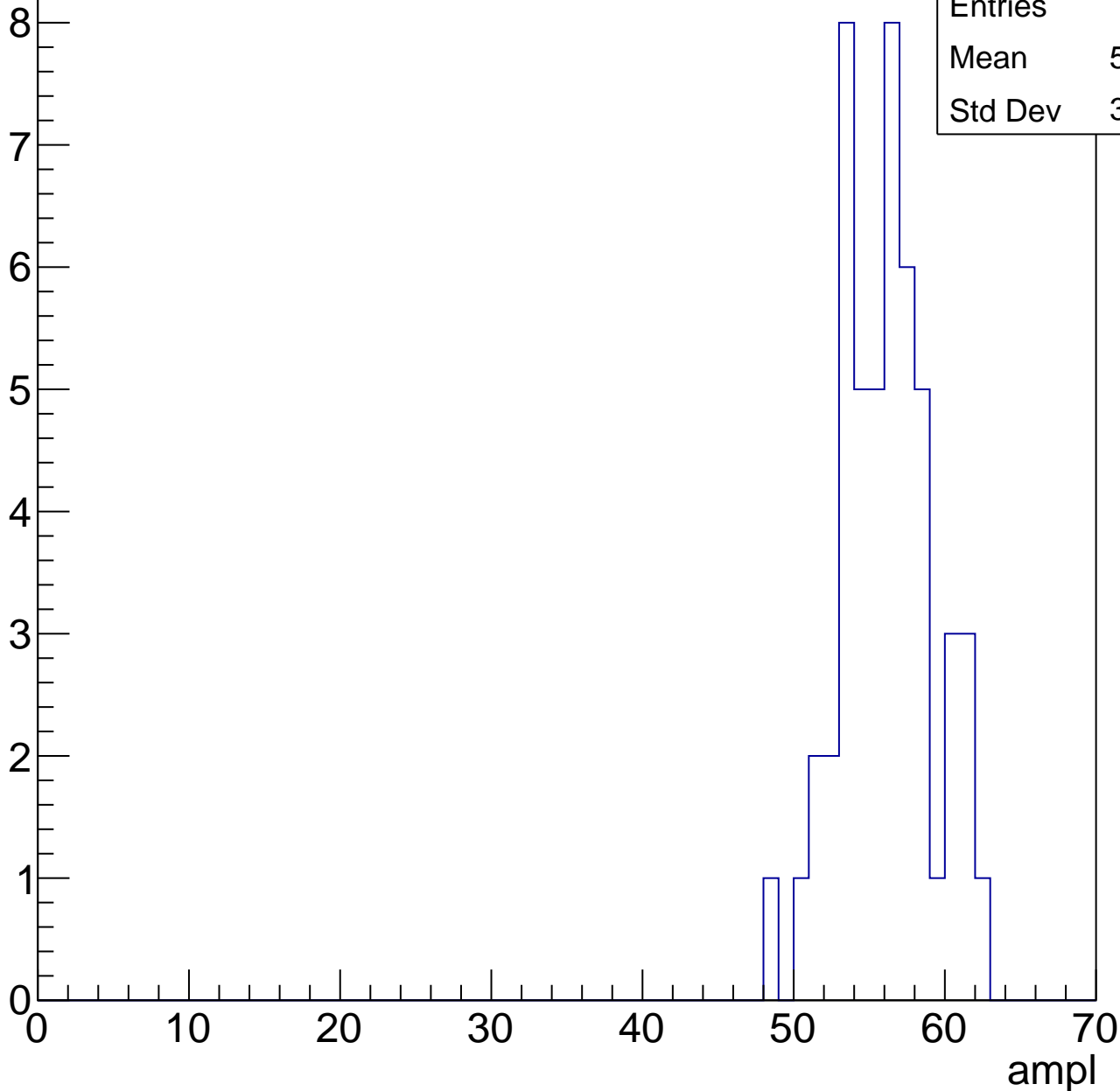


# B1L102S, U20-ch52, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	55.63
Std Dev	3.023



# B1L102S, U20-ch52, adc5

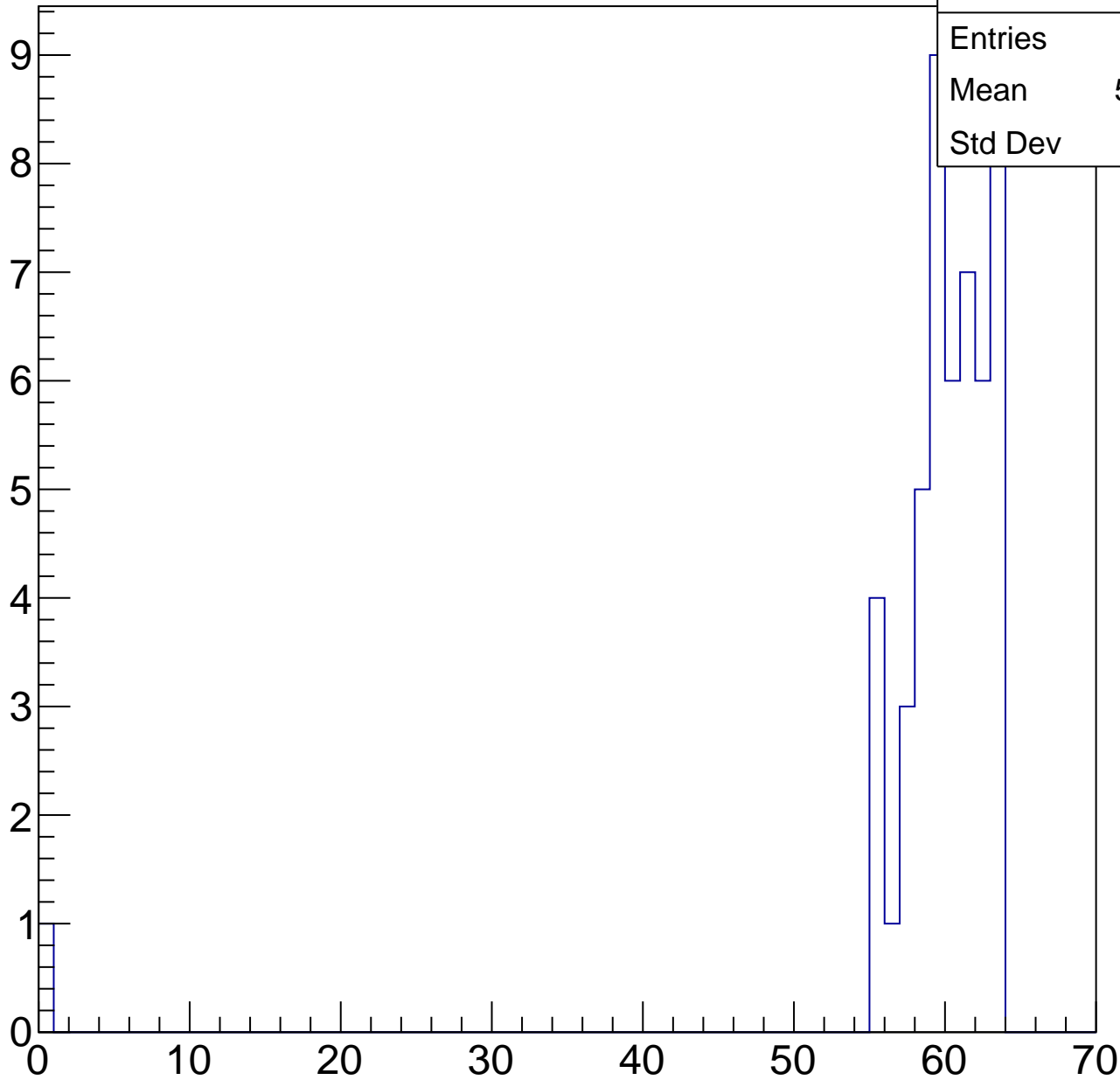
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	51
Mean	58.71
Std Dev	8.63

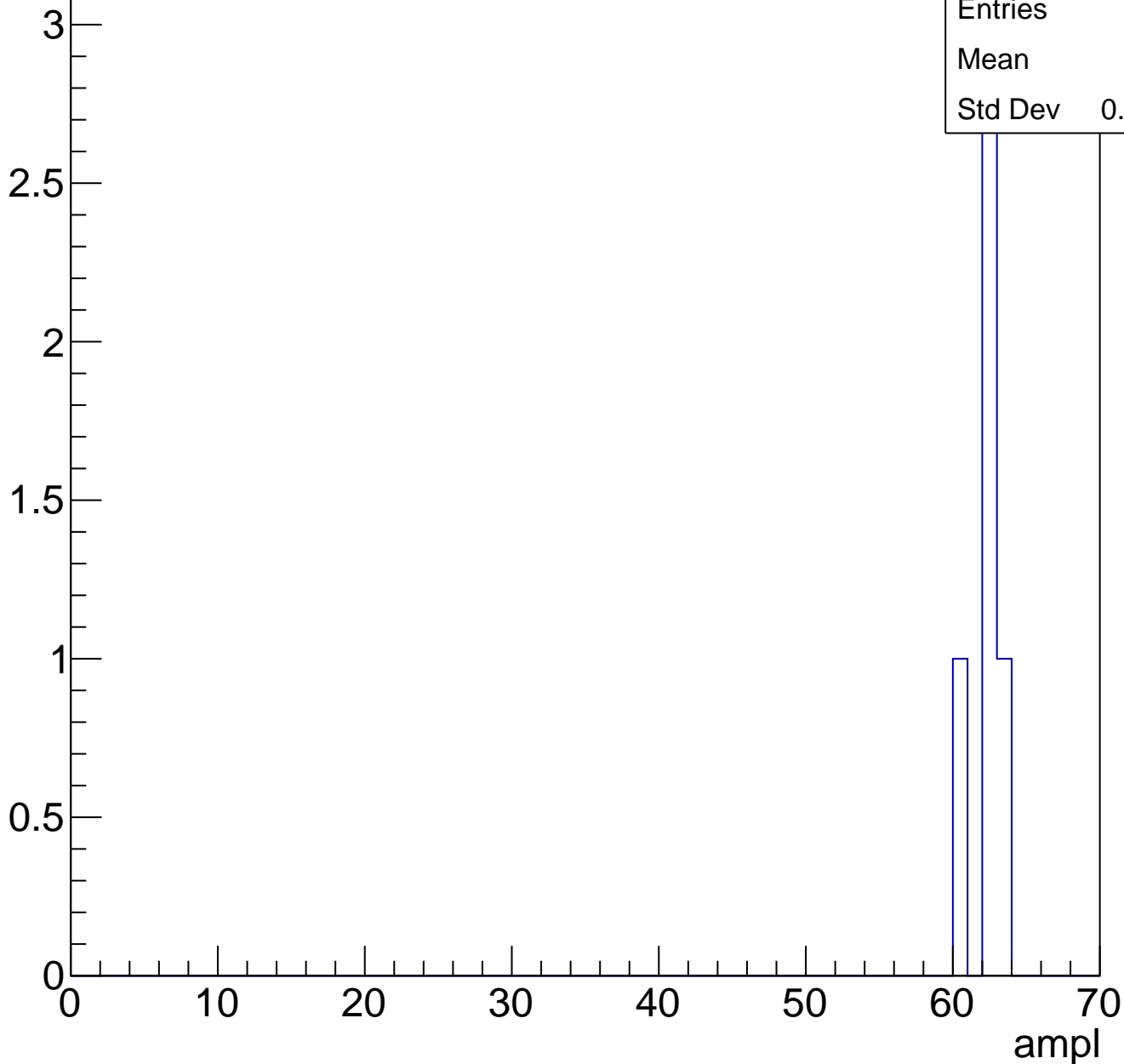
ampl



# B1L102S, U20-ch52, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U20-ch52, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch53, adc0

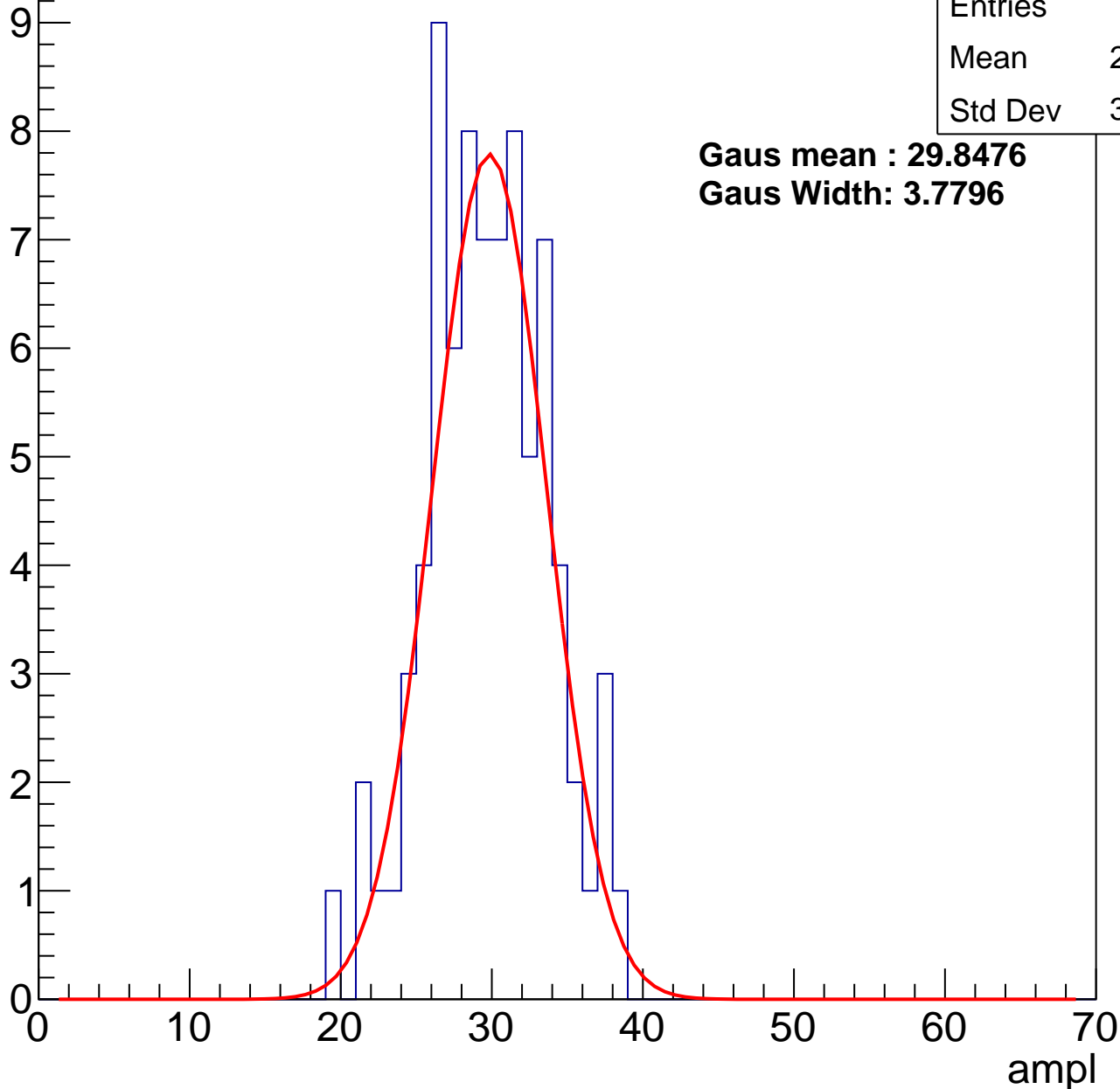
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	80
Mean	29.26
Std Dev	3.952

**Gaus mean : 29.8476**

**Gaus Width: 3.7796**



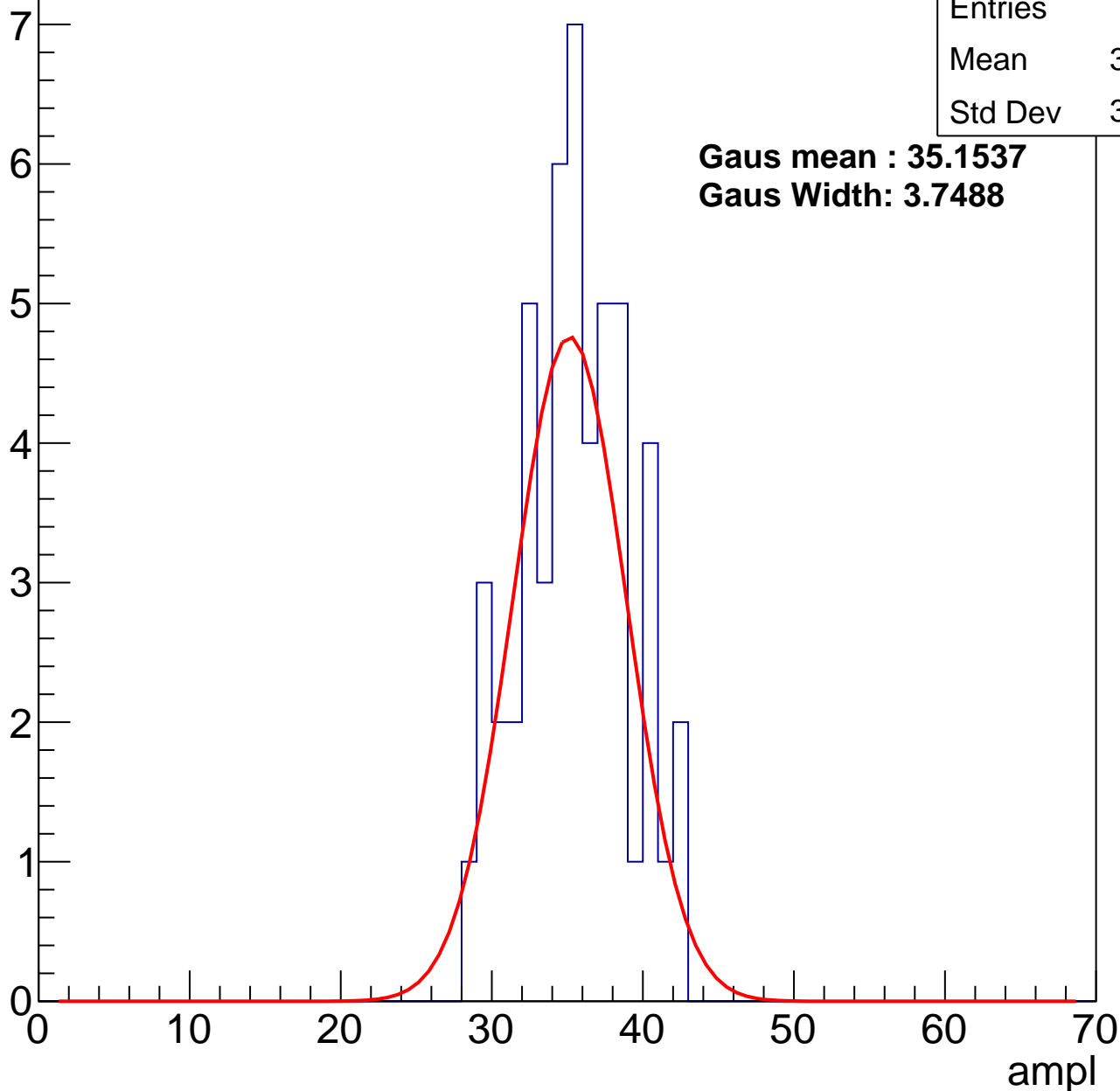
# B1L102S, U20-ch53, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	35.06
Std Dev	3.489

**Gaus mean : 35.1537**  
**Gaus Width: 3.7488**



# B1L102S, U20-ch53, adc2

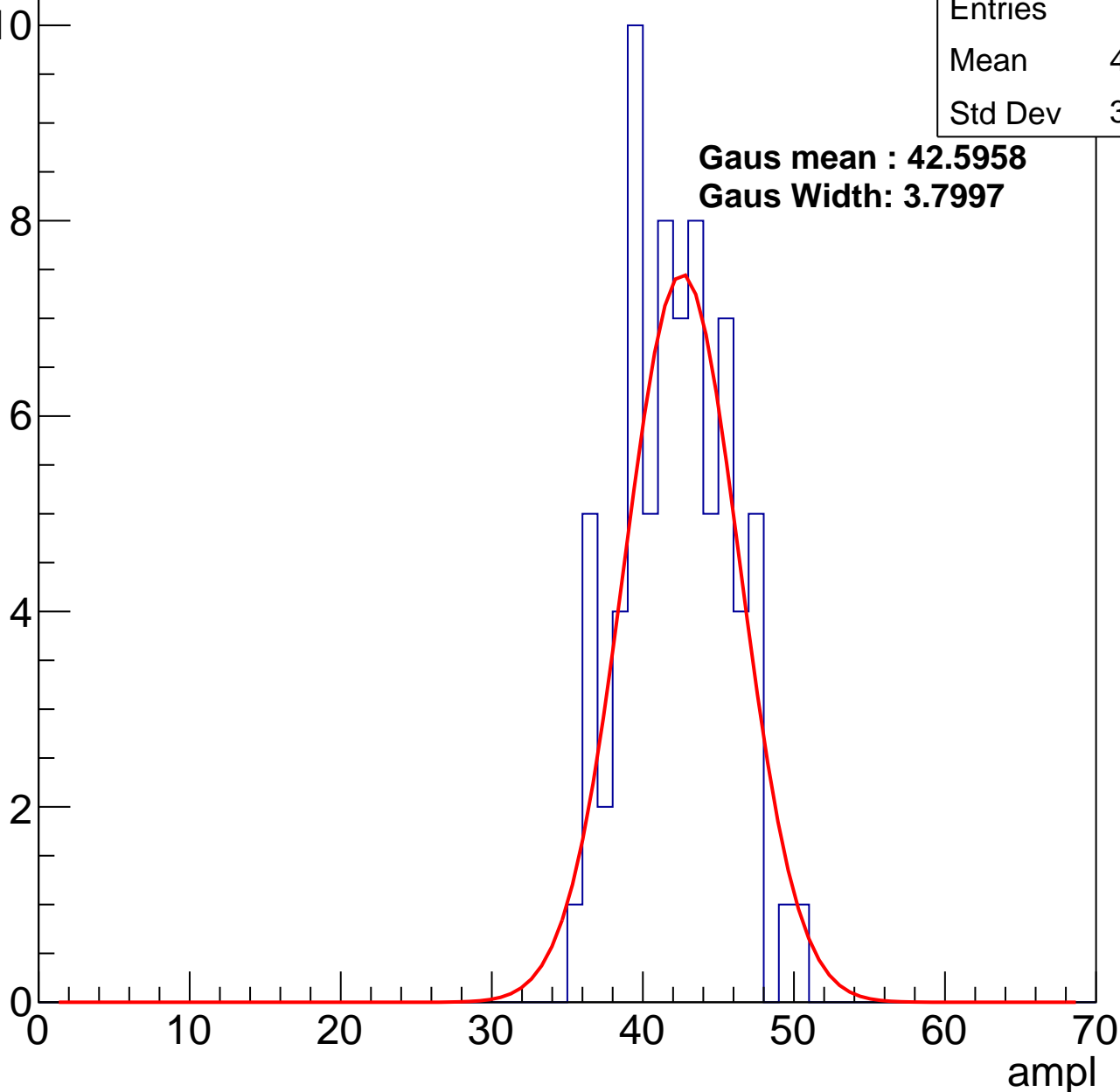
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	41.78
Std Dev	3.413

**Gaus mean : 42.5958**

**Gaus Width: 3.7997**

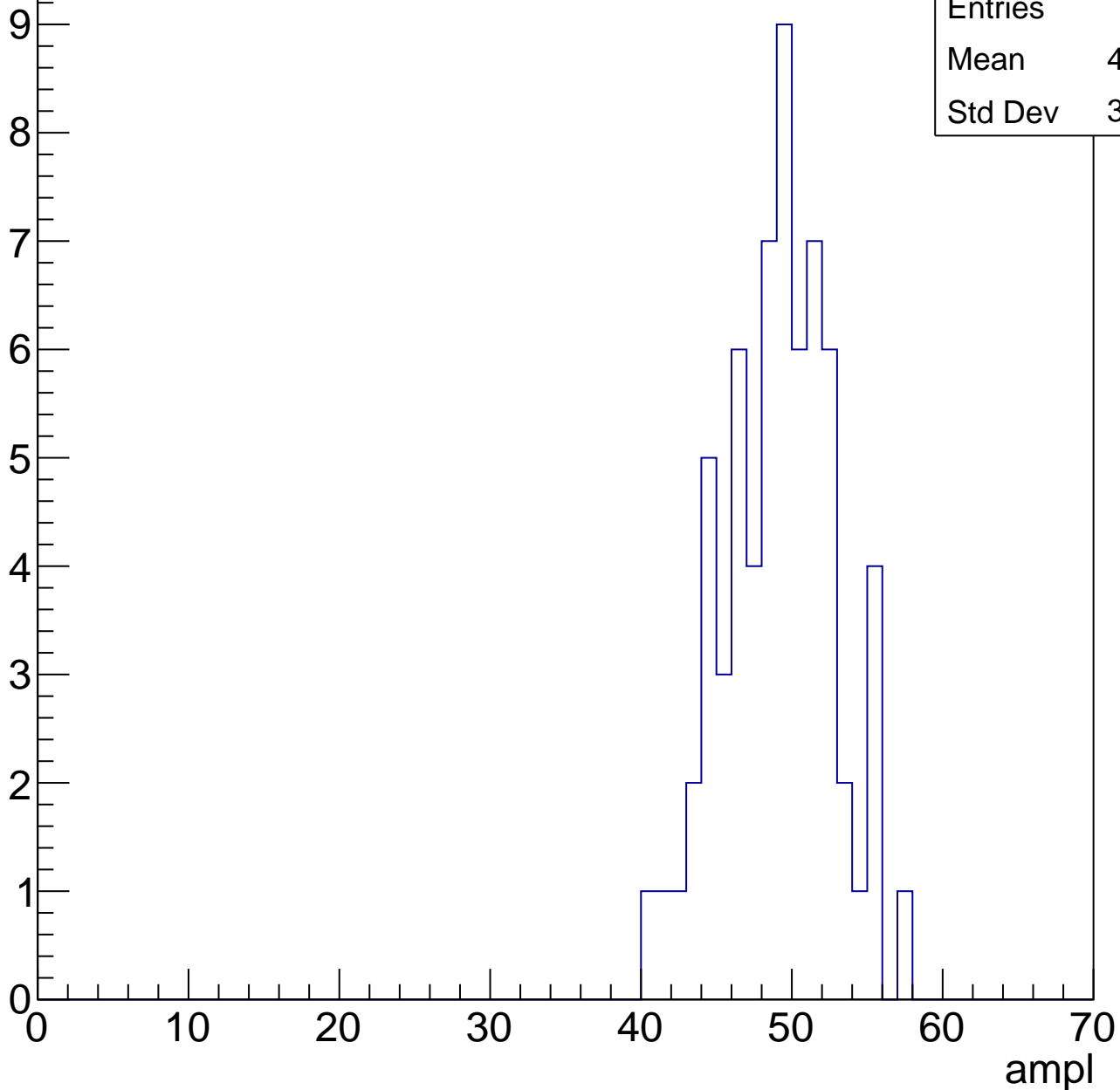


# B1L102S, U20-ch53, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	48.65
Std Dev	3.612

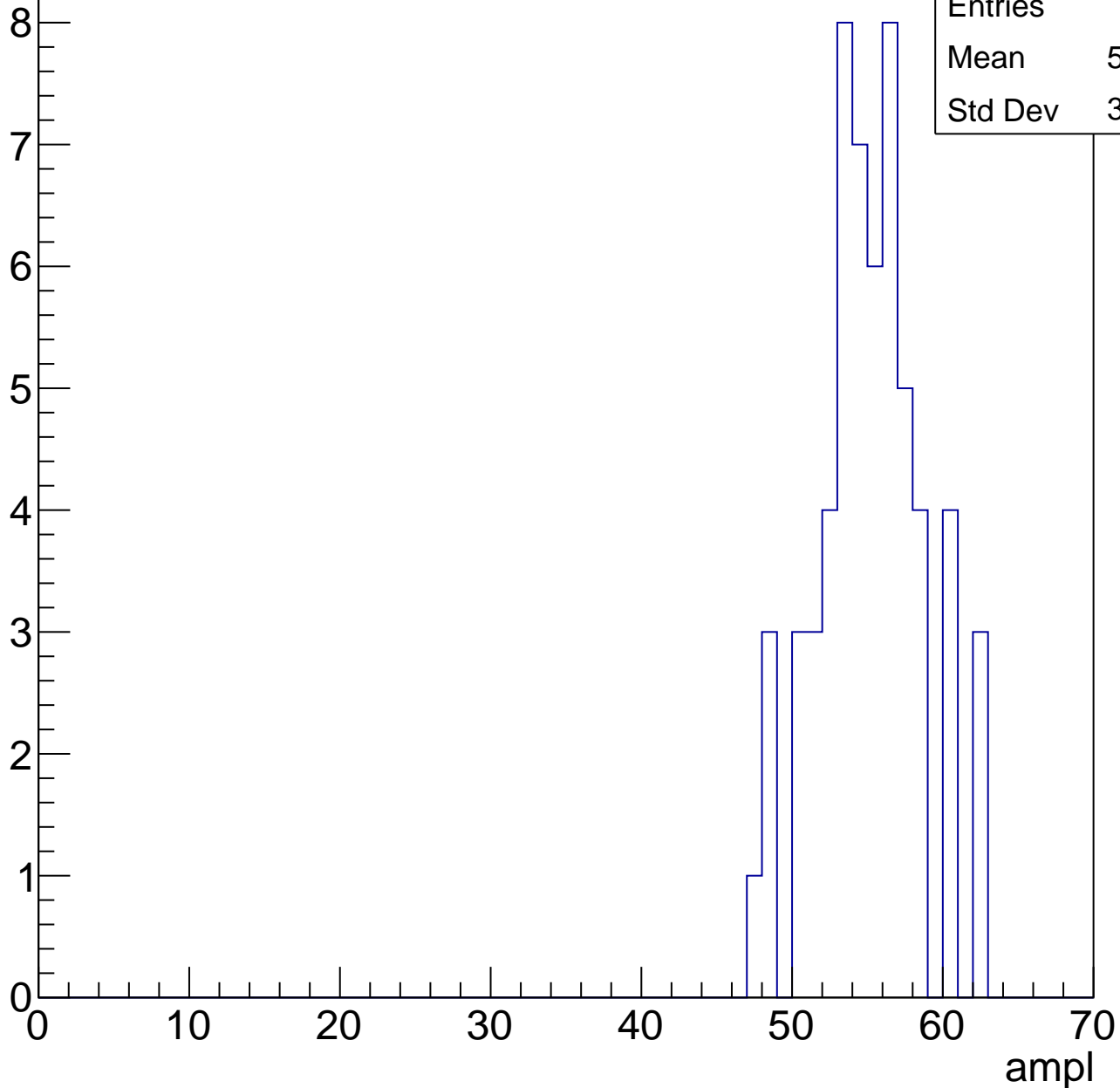


# B1L102S, U20-ch53, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	54.66
Std Dev	3.477

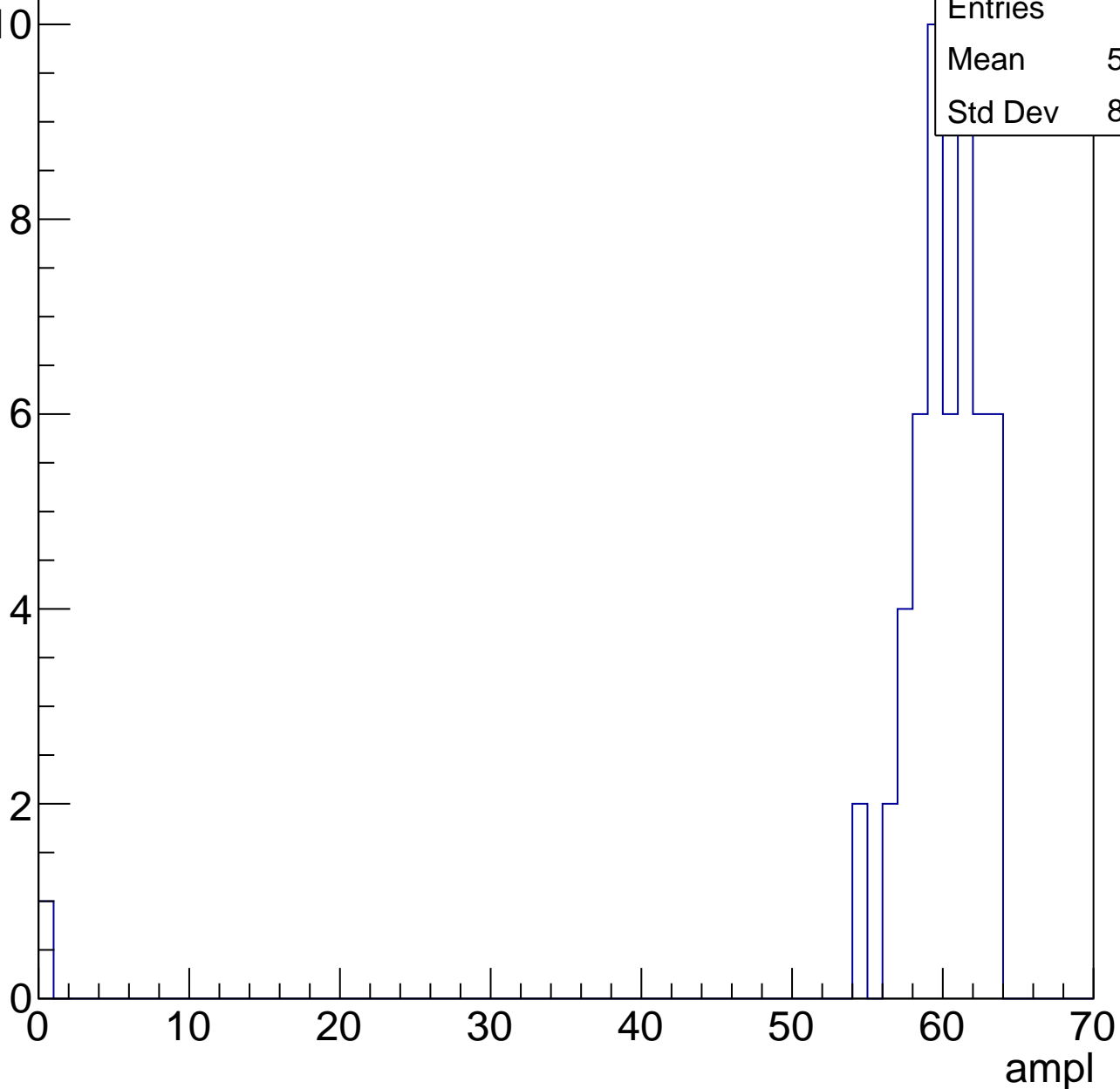


# B1L102S, U20-ch53, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

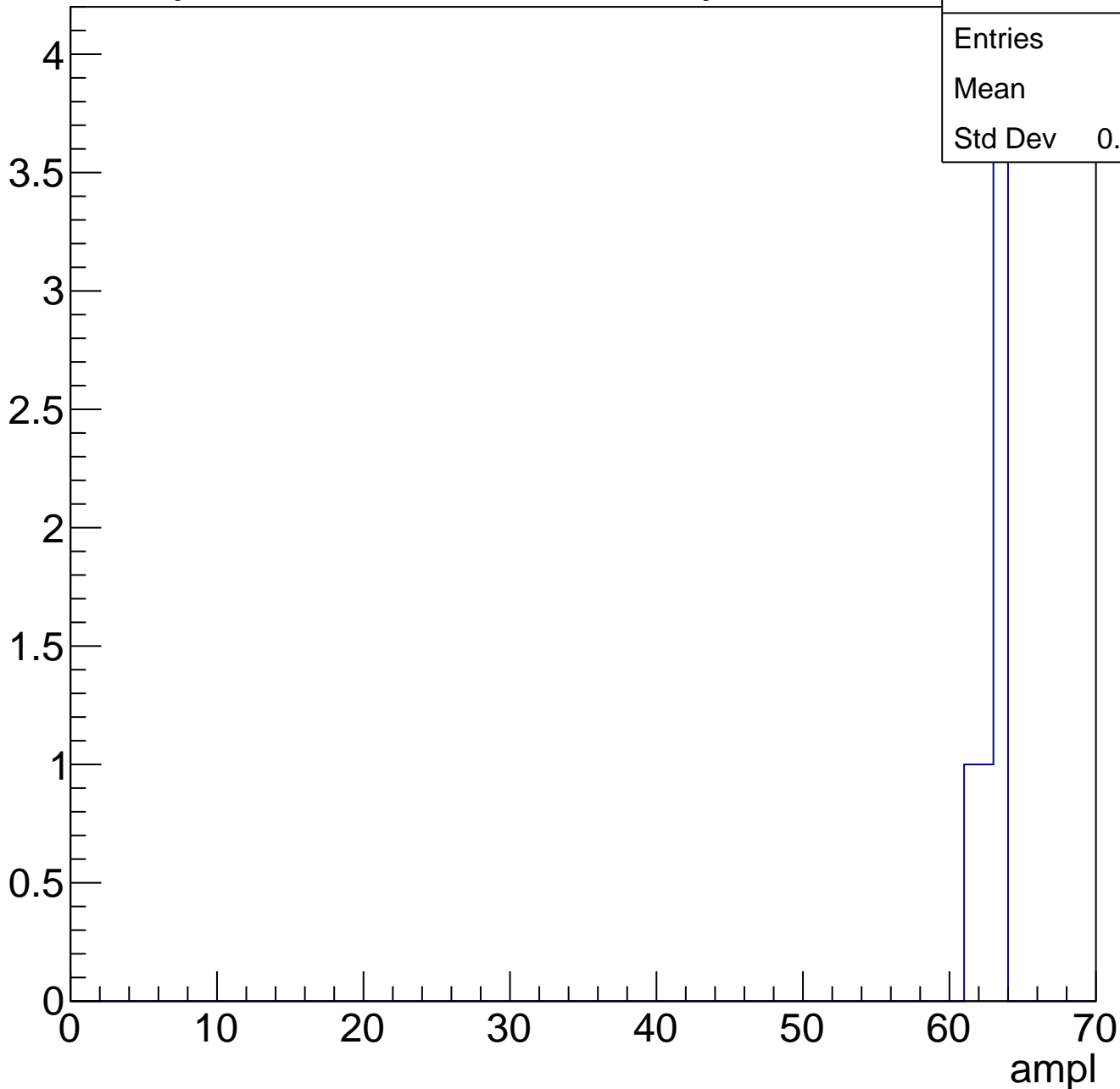
Entries	52
Mean	58.56
Std Dev	8.495



# B1L102S, U20-ch53, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U20-ch53, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch54, adc0

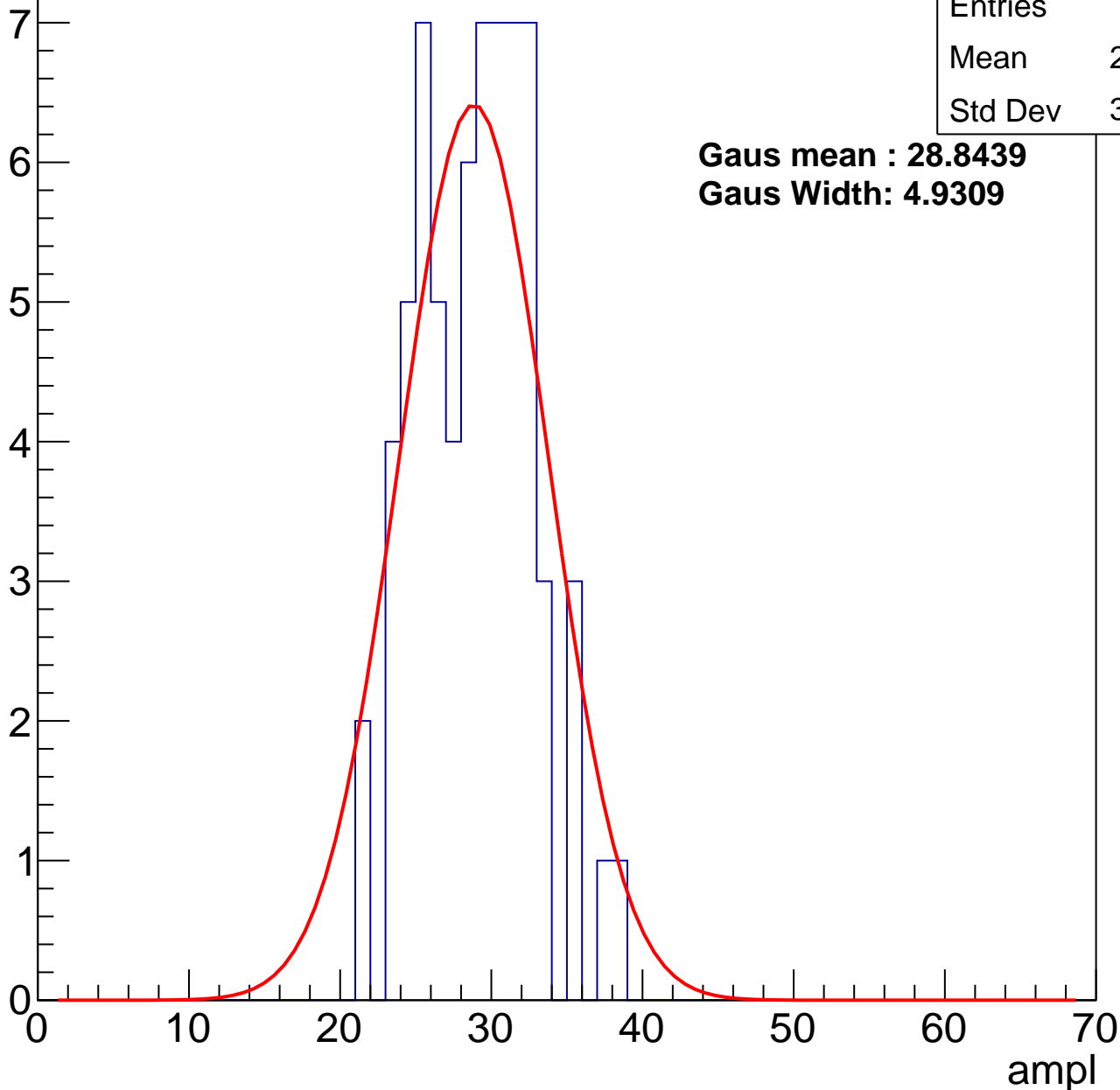
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	28.52
Std Dev	3.728

**Gaus mean : 28.8439**

**Gaus Width: 4.9309**



# B1L102S, U20-ch54, adc1

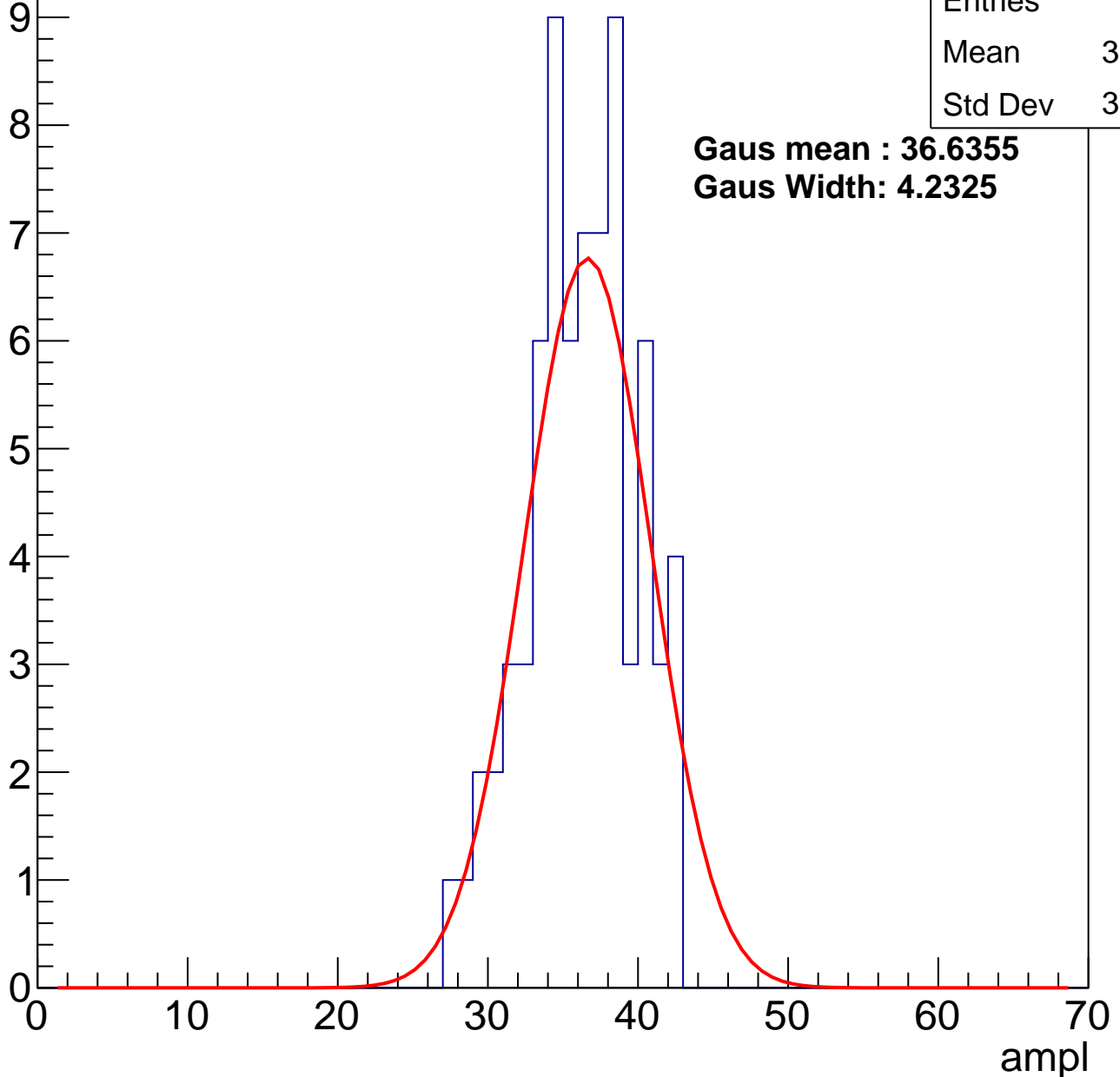
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	35.79
Std Dev	3.567

**Gaus mean : 36.6355**

**Gaus Width: 4.2325**



# B1L102S, U20-ch54, adc2

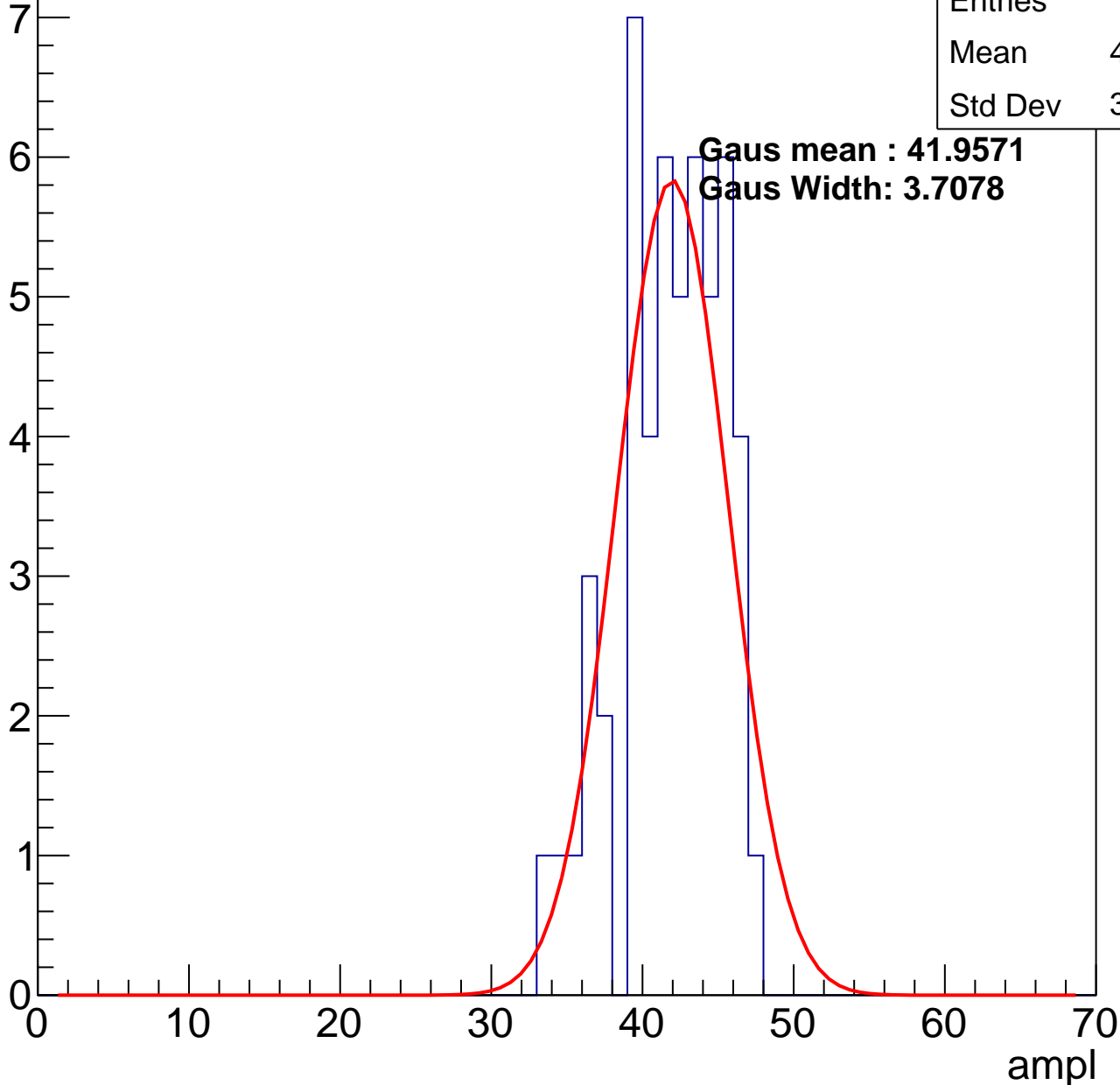
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	41.38
Std Dev	3.358

**Gaus mean : 41.9571**

**Gaus Width: 3.7078**

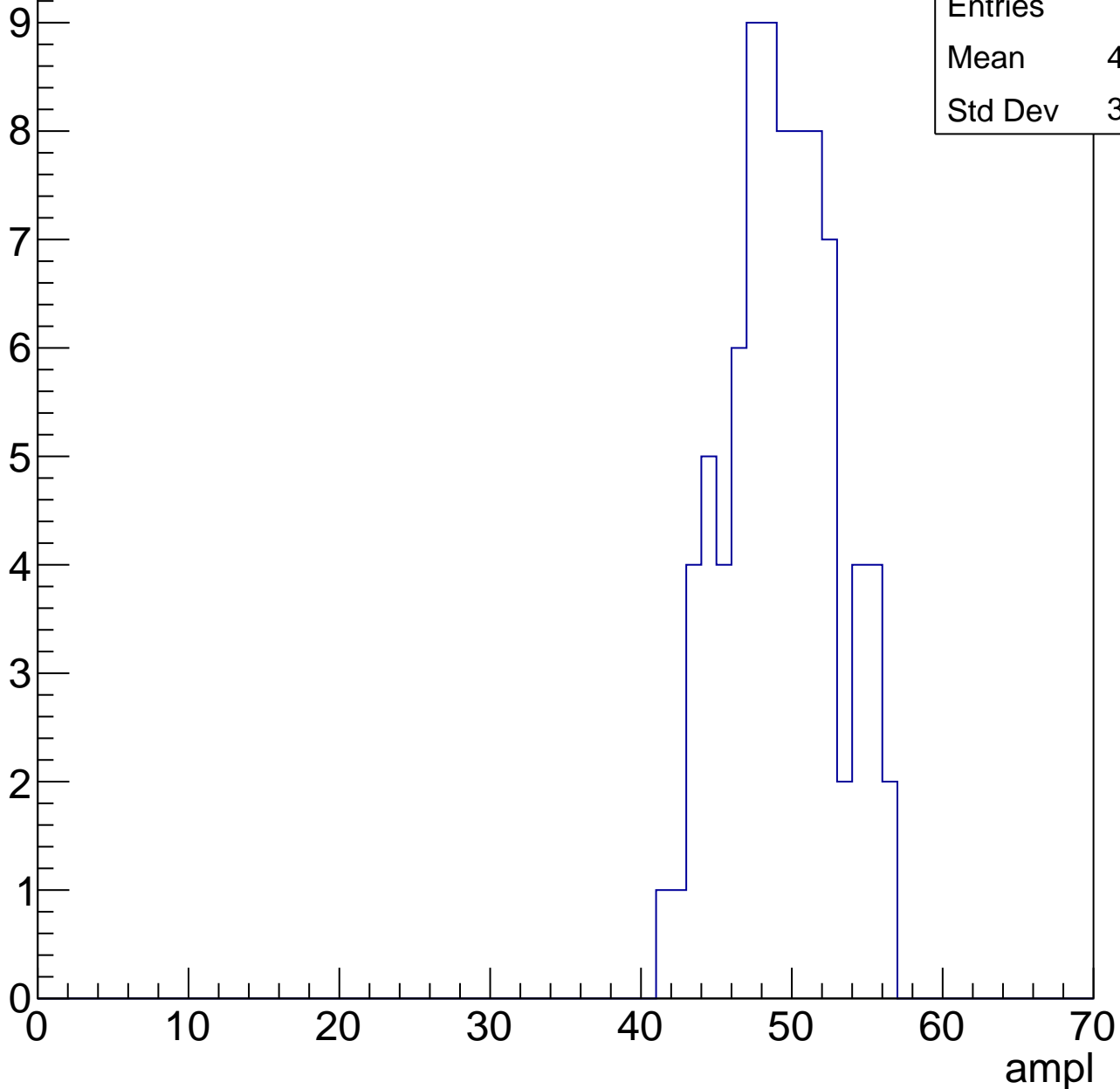


# B1L102S, U20-ch54, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	82
Mean	48.83
Std Dev	3.526

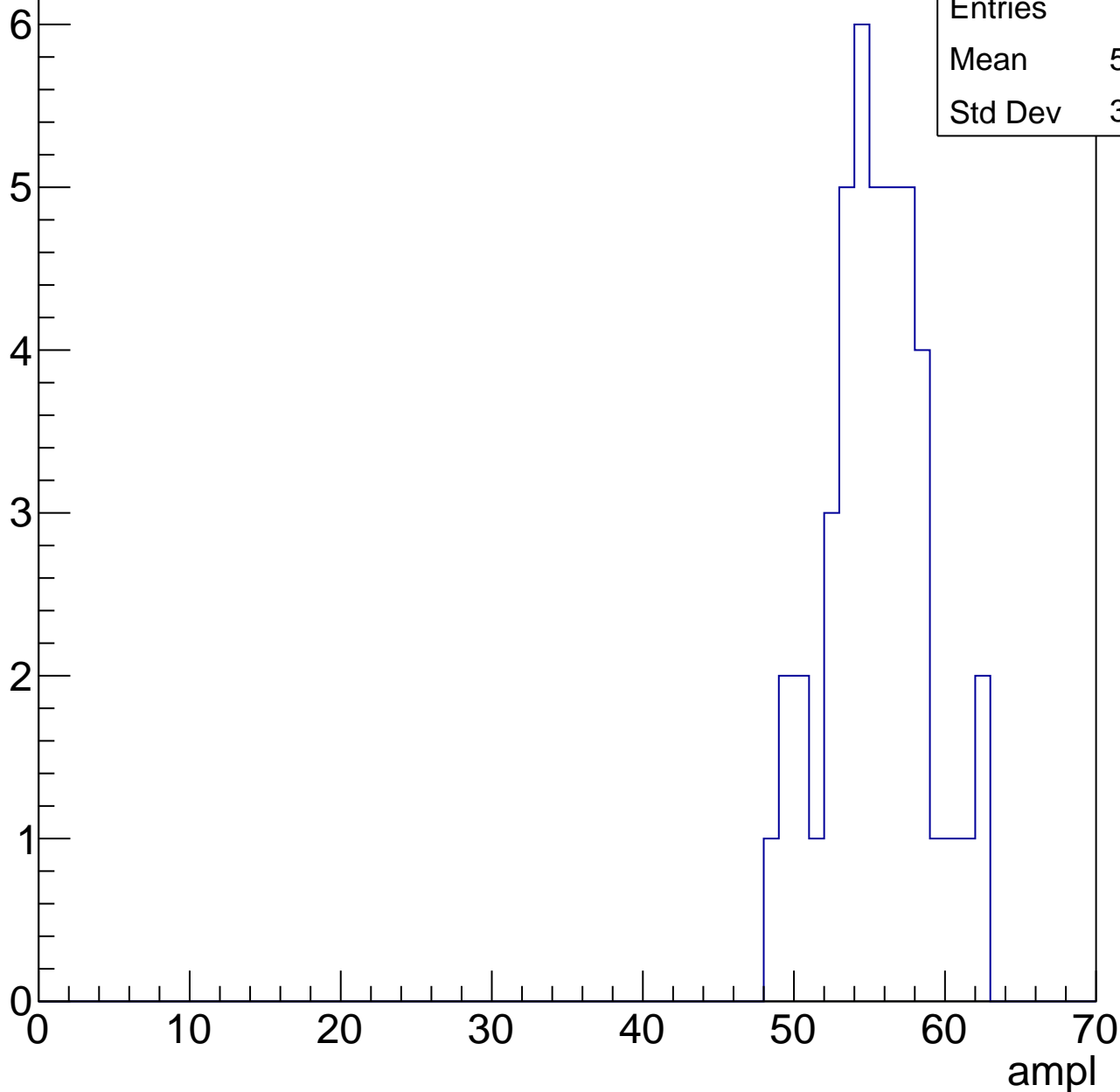


# B1L102S, U20-ch54, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	44
Mean	54.95
Std Dev	3.289

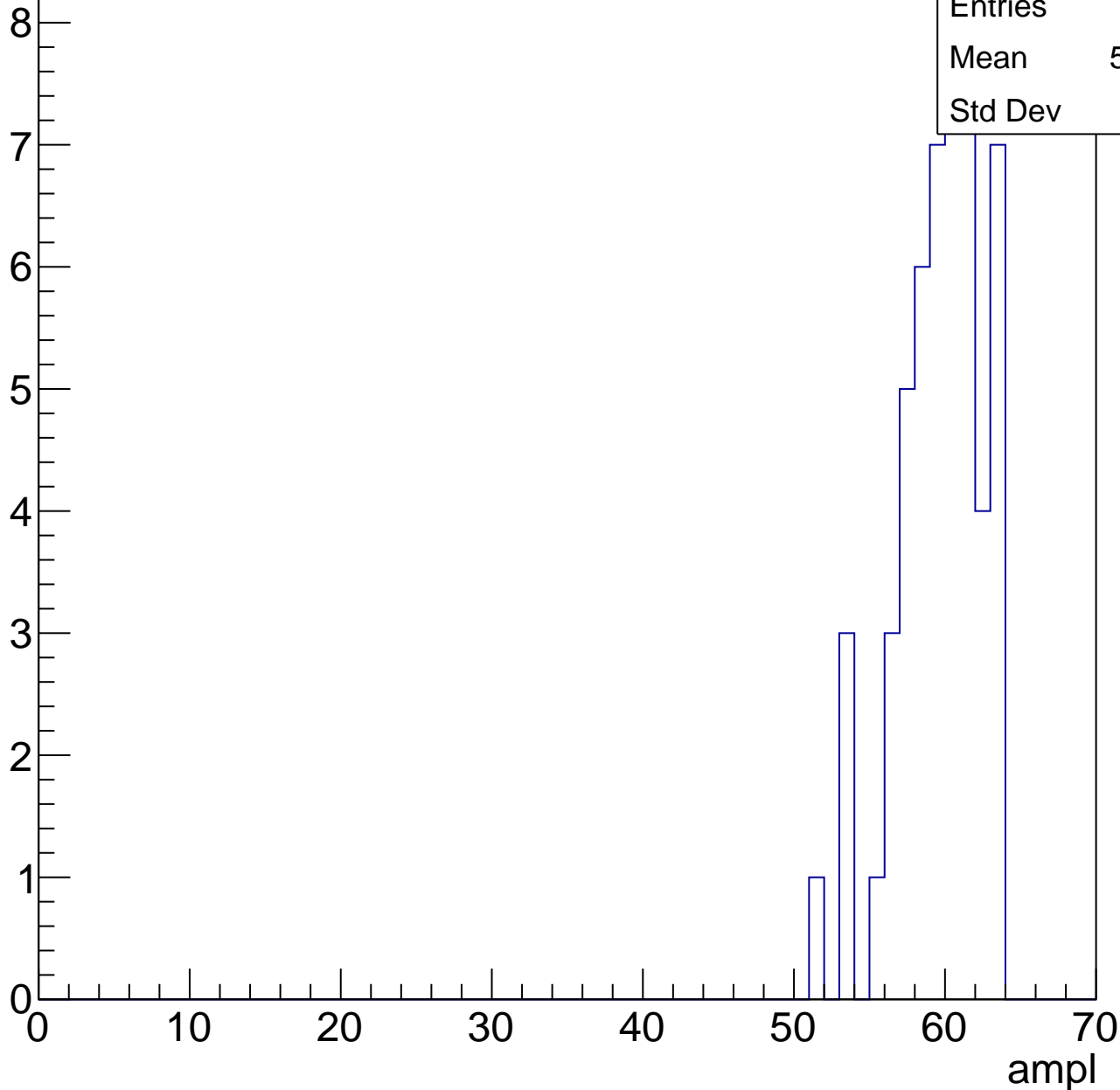


# B1L102S, U20-ch54, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	59.17
Std Dev	2.84



# B1L102S, U20-ch54, adc6

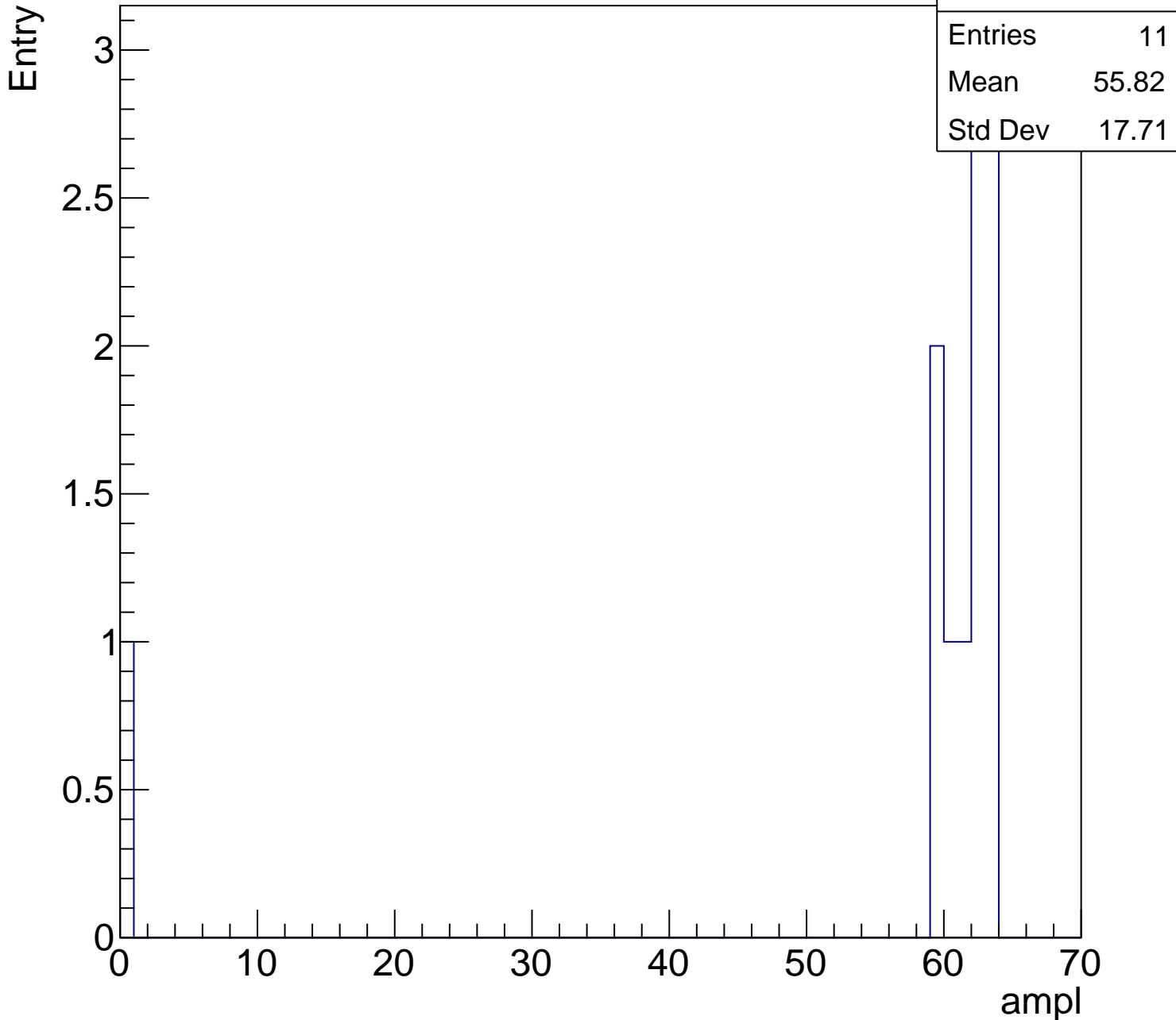
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

3  
2.5  
2  
1.5  
1  
0.5  
0

Entries	11
Mean	55.82
Std Dev	17.71

ampl





# B1L102S, U20-ch54, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch55, adc0

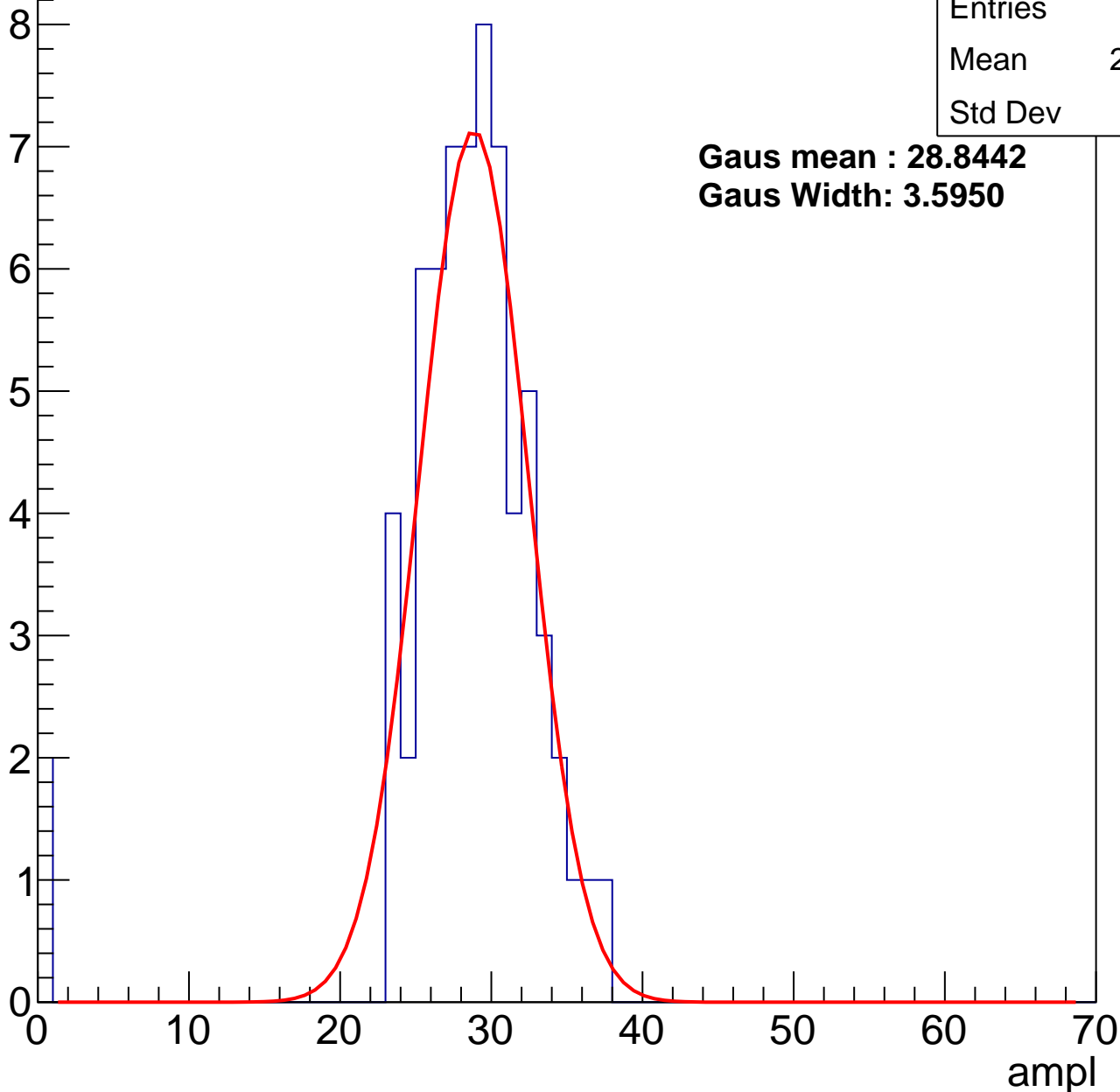
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	27.76
Std Dev	5.87

**Gaus mean : 28.8442**

**Gaus Width: 3.5950**



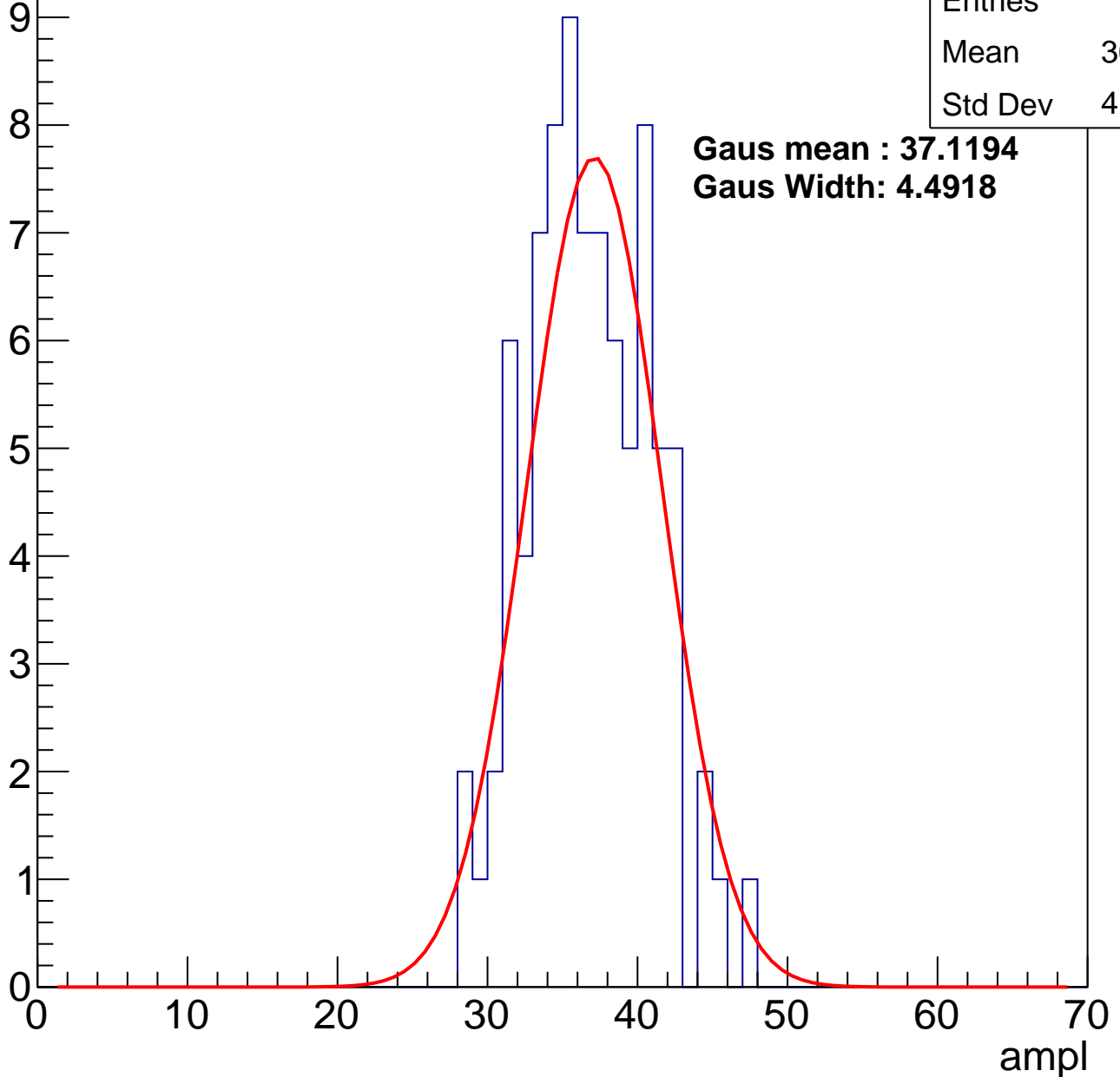
# B1L102S, U20-ch55, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	86
Mean	36.35
Std Dev	4.028

**Gaus mean : 37.1194**  
**Gaus Width: 4.4918**



# B1L102S, U20-ch55, adc2

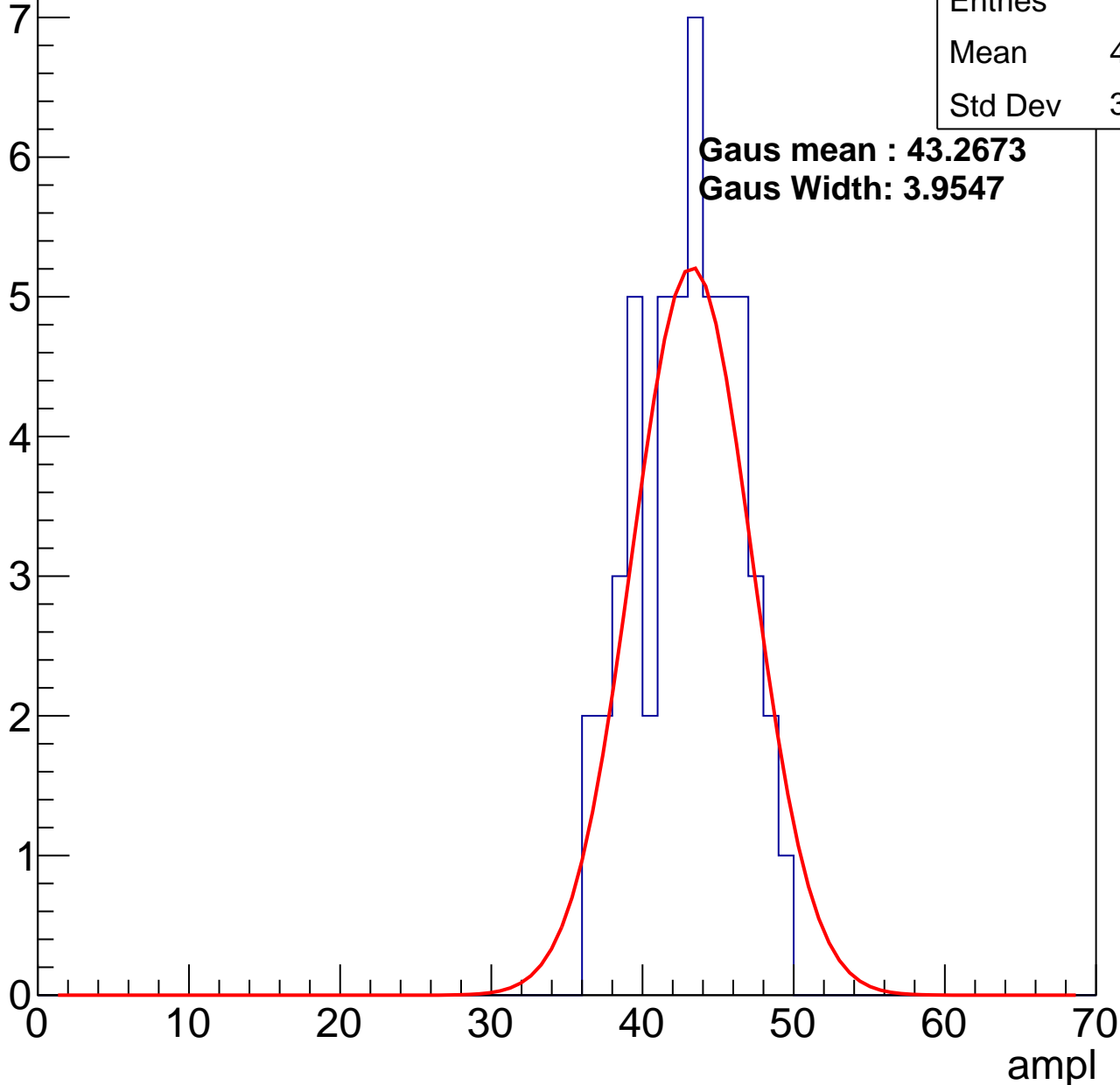
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	42.54
Std Dev	3.284

**Gaus mean : 43.2673**

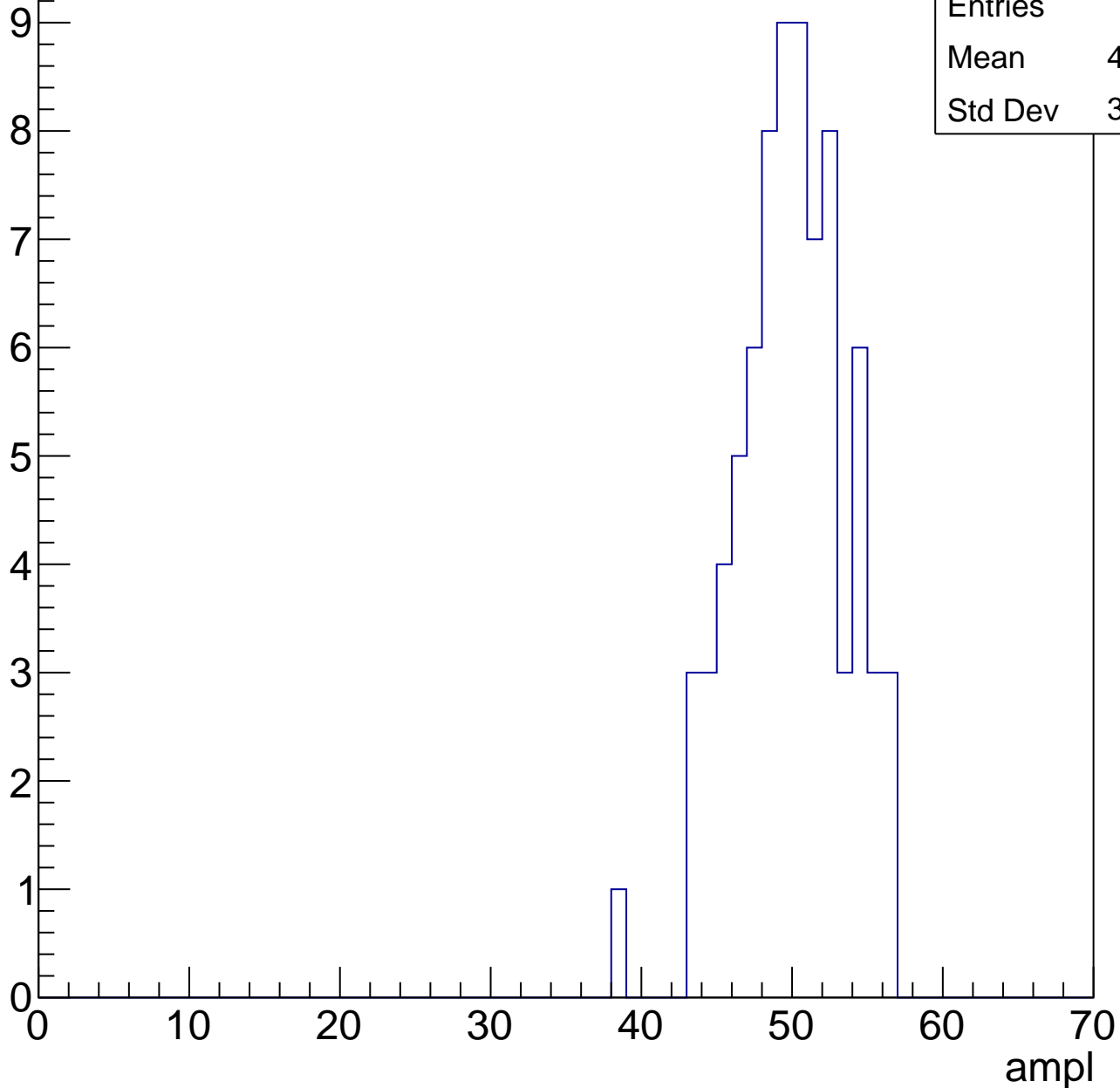
**Gaus Width: 3.9547**



# B1L102S, U20-ch55, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

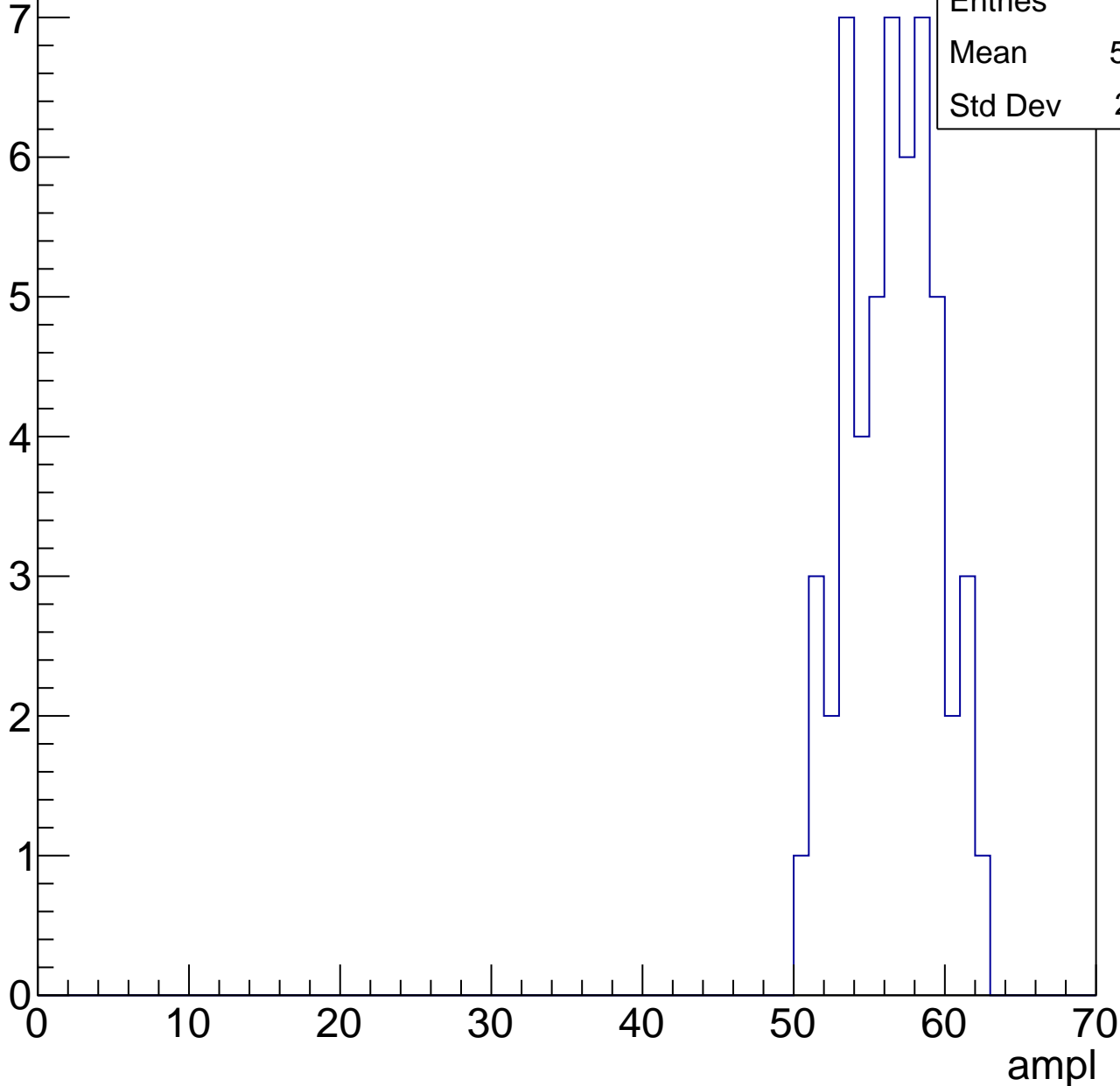


# B1L102S, U20-ch55, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	56.02
Std Dev	2.911

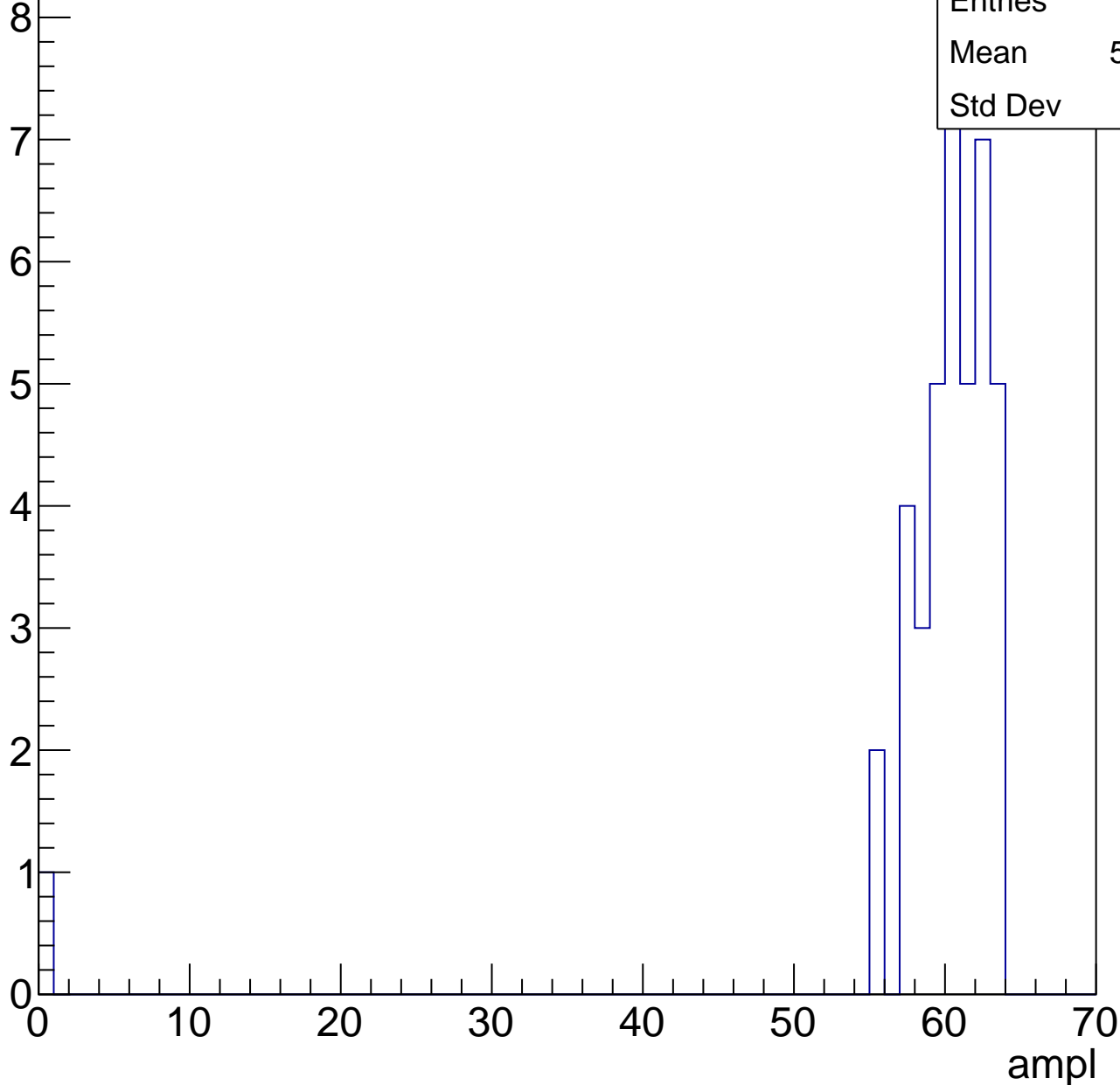


# B1L102S, U20-ch55, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	40
Mean	58.52
Std Dev	9.61

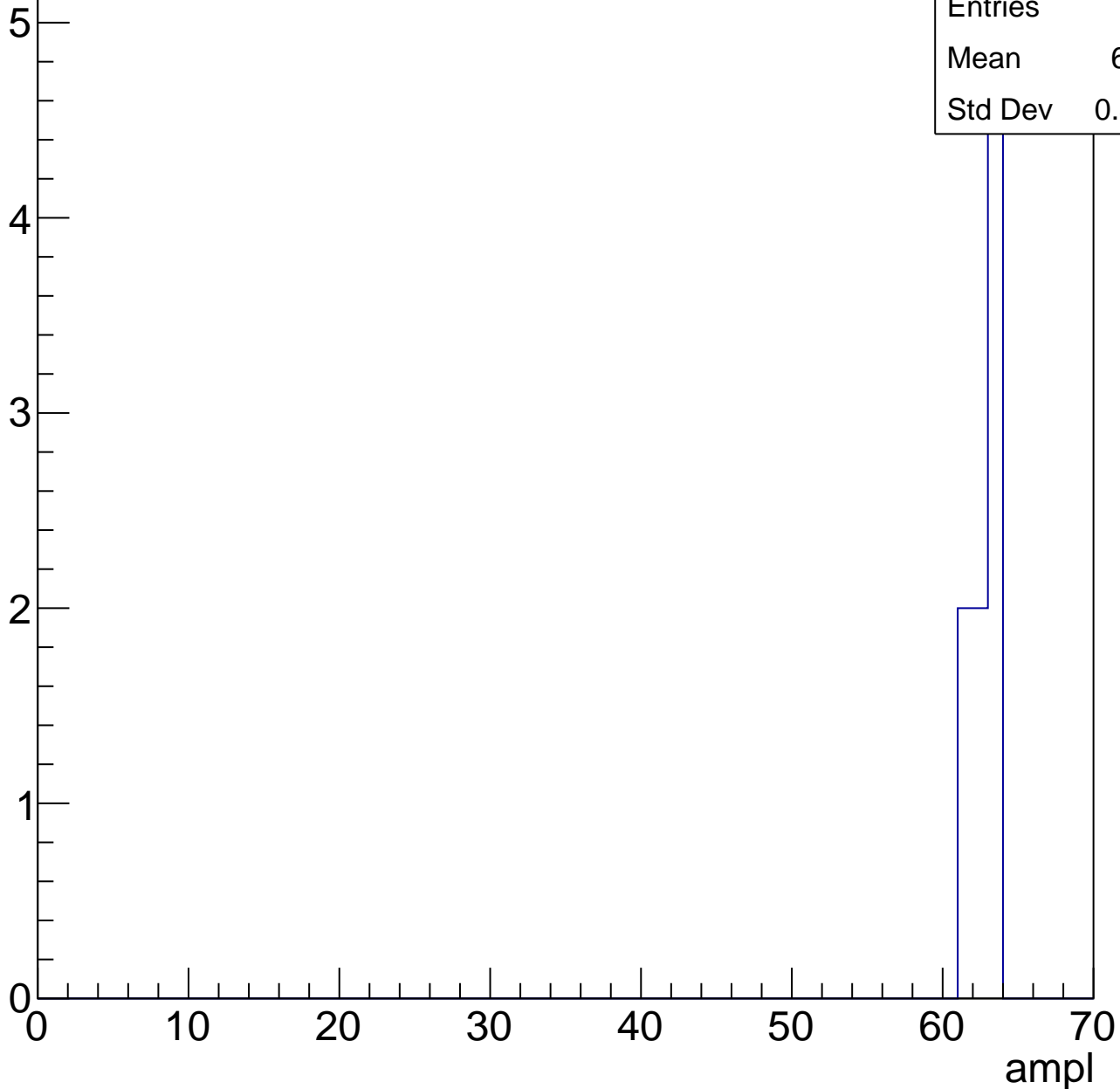


# B1L102S, U20-ch55, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	9
Mean	62.33
Std Dev	0.8165





# B1L102S, U20-ch55, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch56, adc0

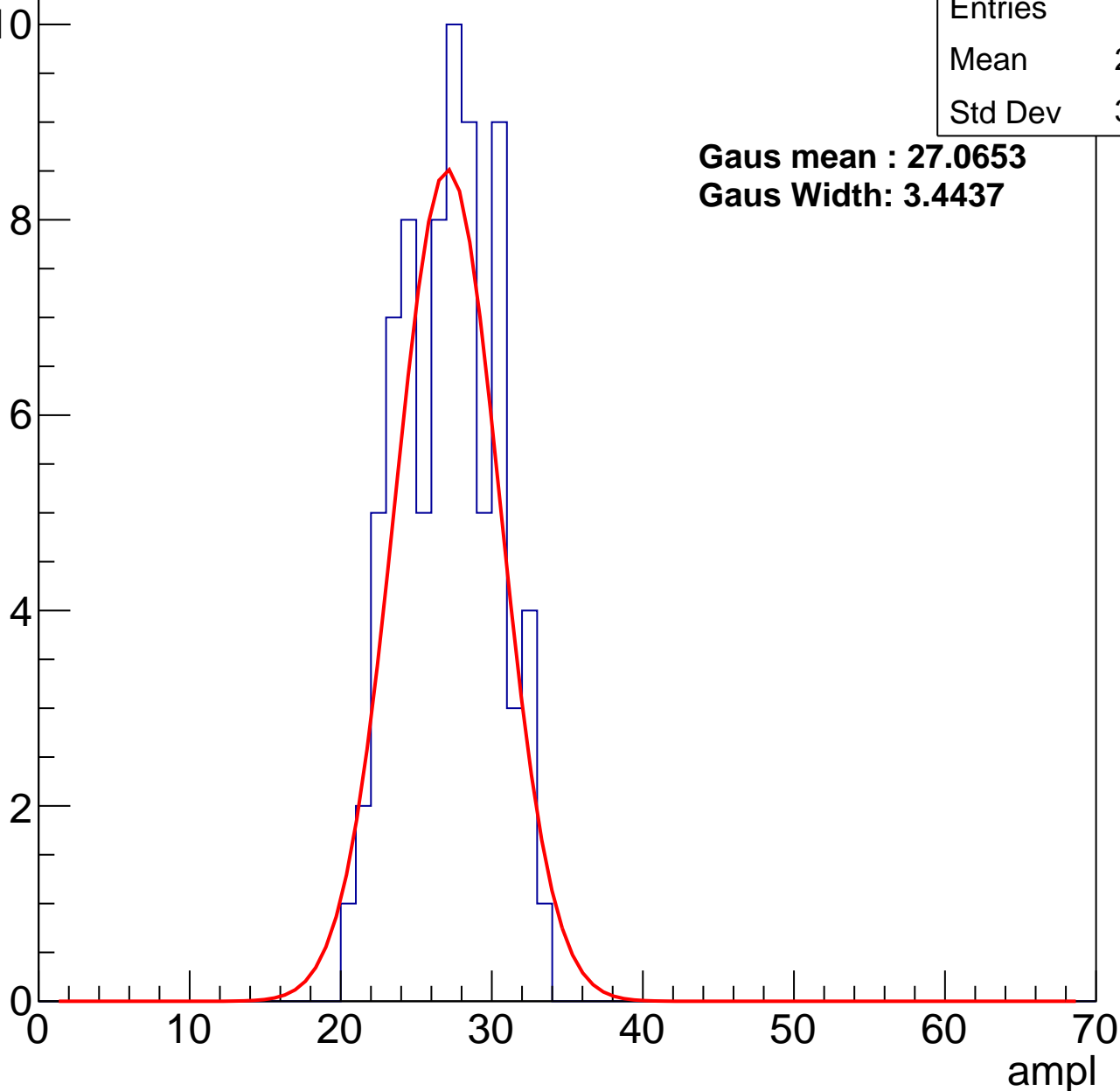
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	26.61
Std Dev	3.101

**Gaus mean : 27.0653**

**Gaus Width: 3.4437**



# B1L102S, U20-ch56, adc1

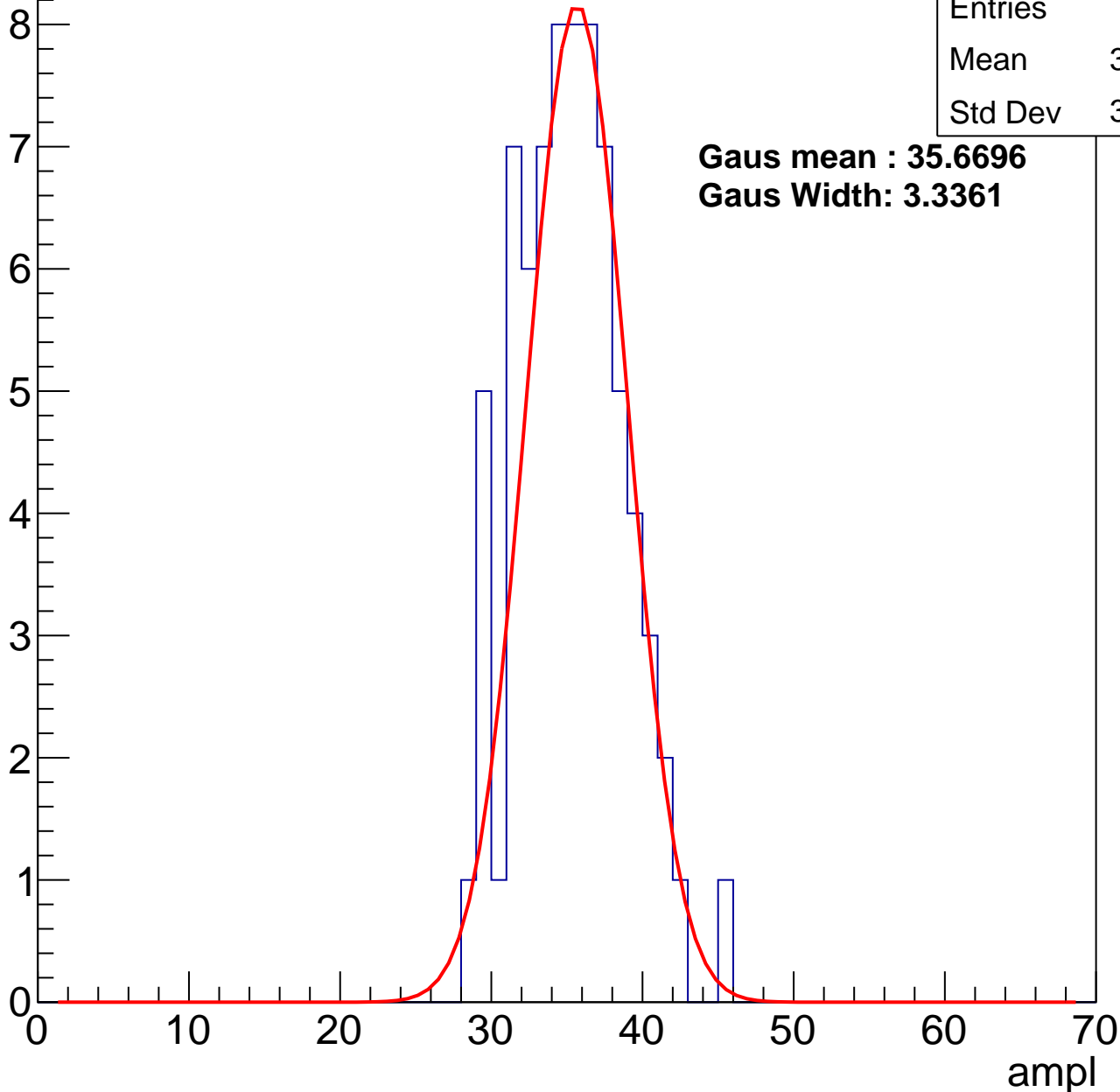
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	34.82
Std Dev	3.477

**Gaus mean : 35.6696**

**Gaus Width: 3.3361**



# B1L102S, U20-ch56, adc2

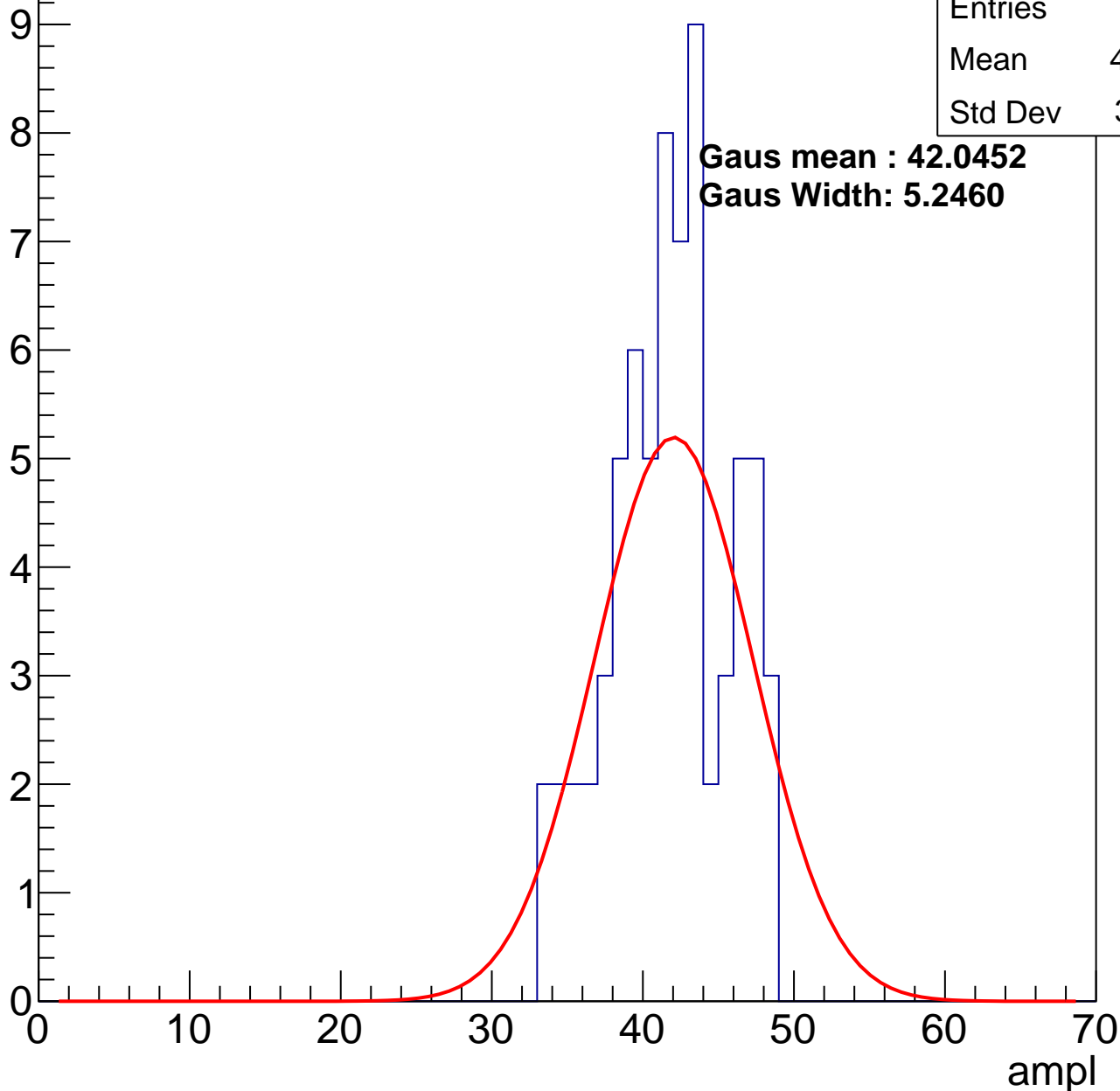
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	41.33
Std Dev	3.851

**Gaus mean : 42.0452**

**Gaus Width: 5.2460**

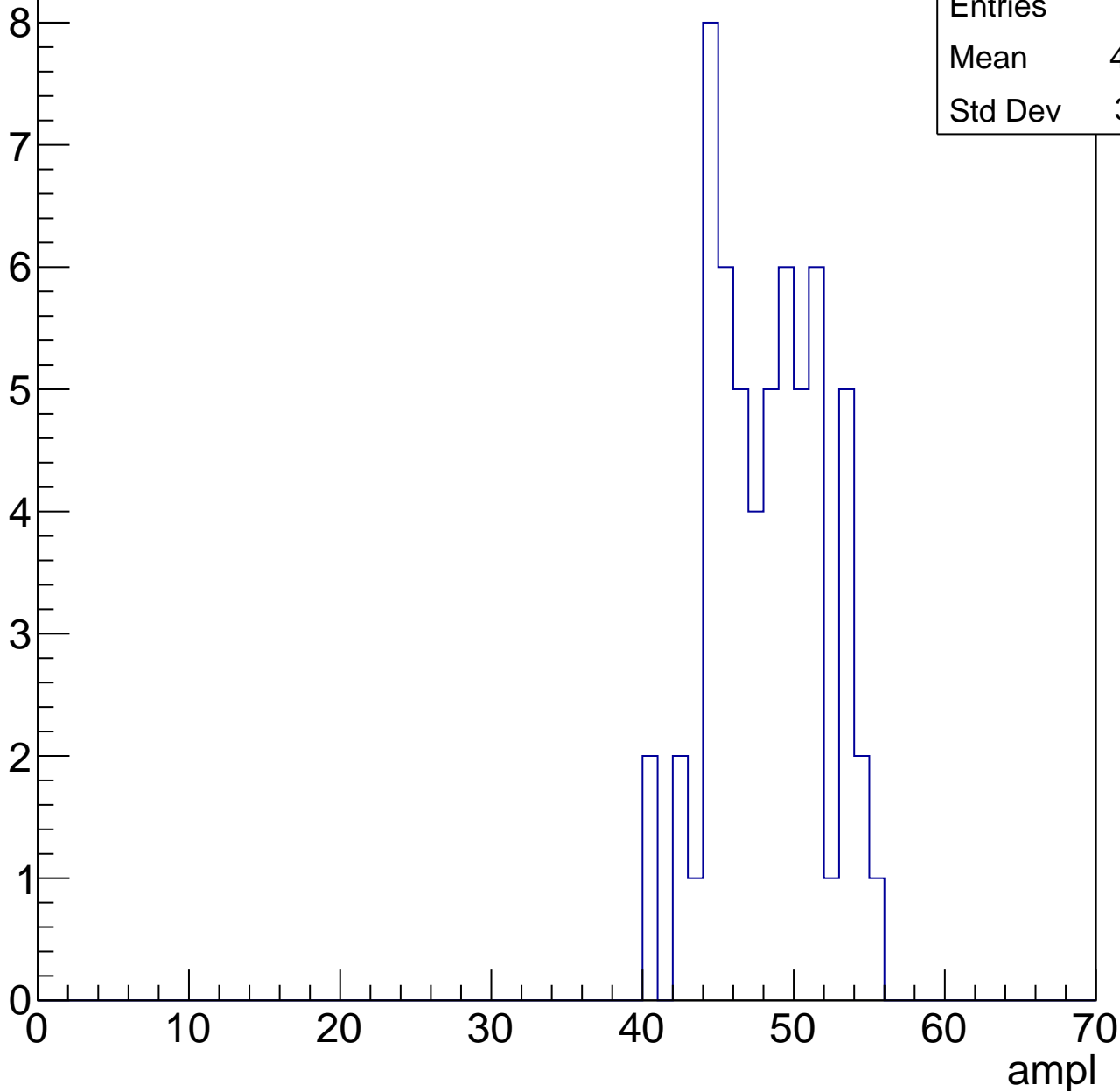


# B1L102S, U20-ch56, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

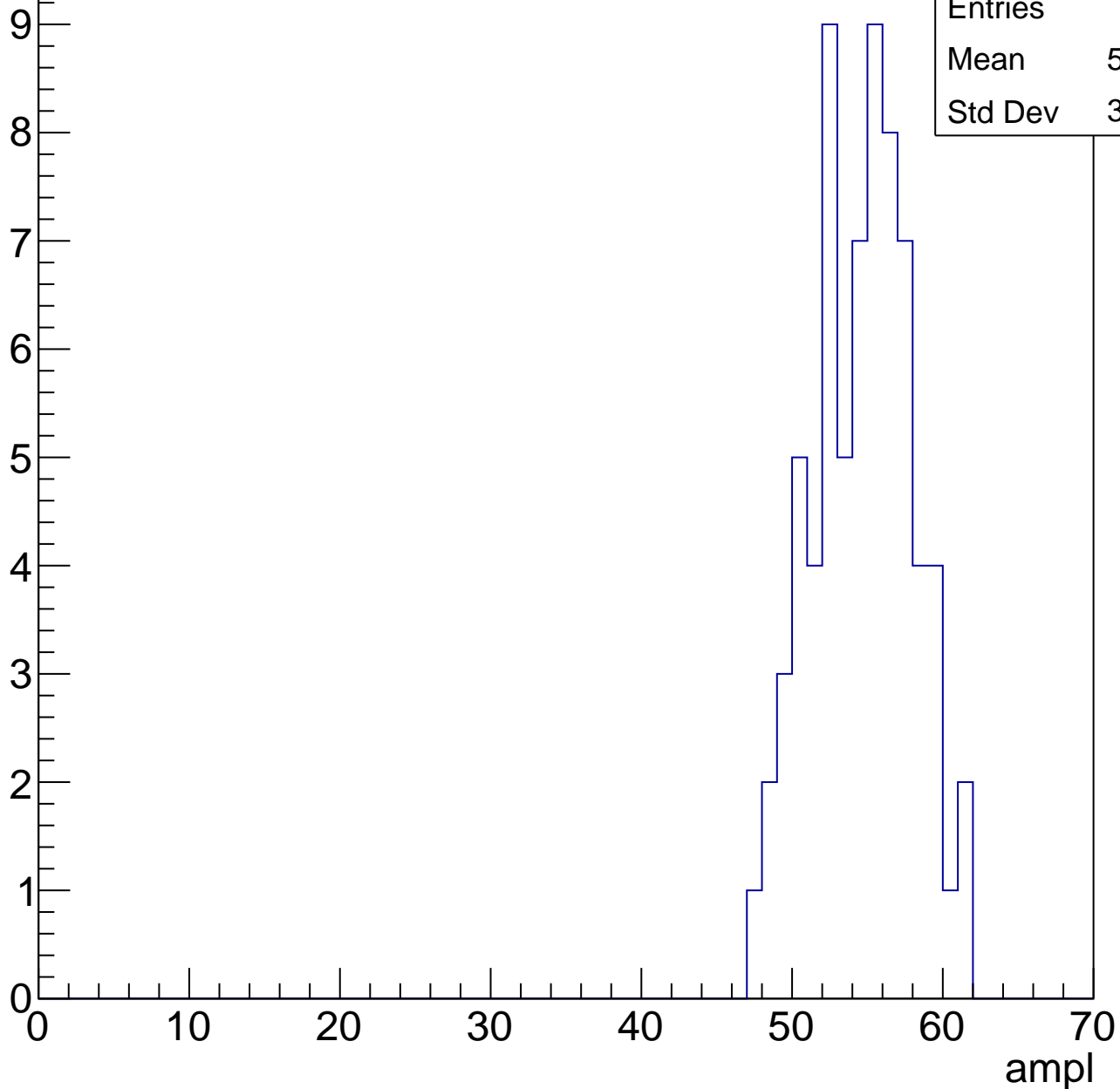
Entries	59
Mean	47.75
Std Dev	3.611



# B1L102S, U20-ch56, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



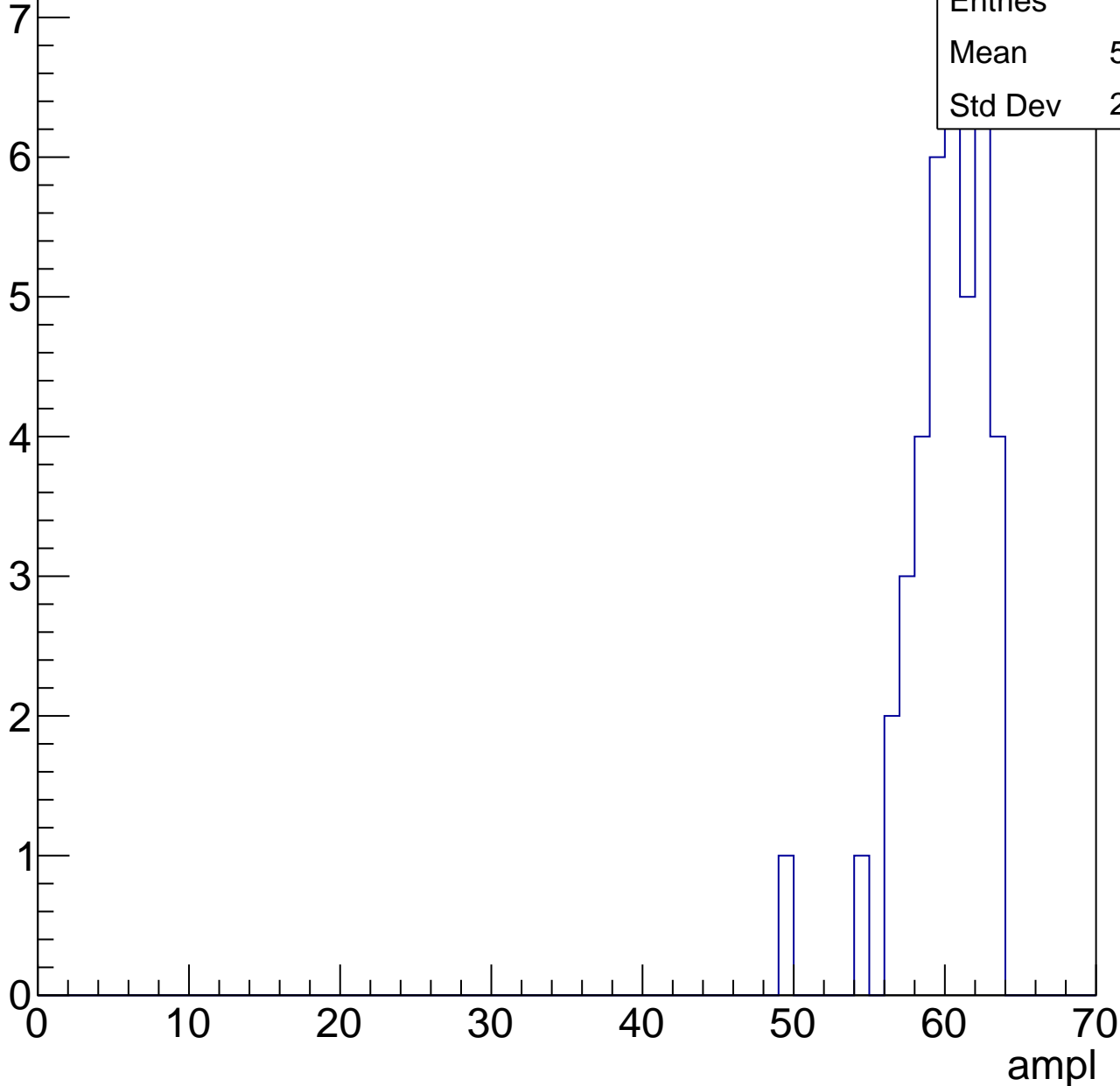
Entries	71
Mean	54.18
Std Dev	3.256

# B1L102S, U20-ch56, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	40
Mean	59.58
Std Dev	2.738

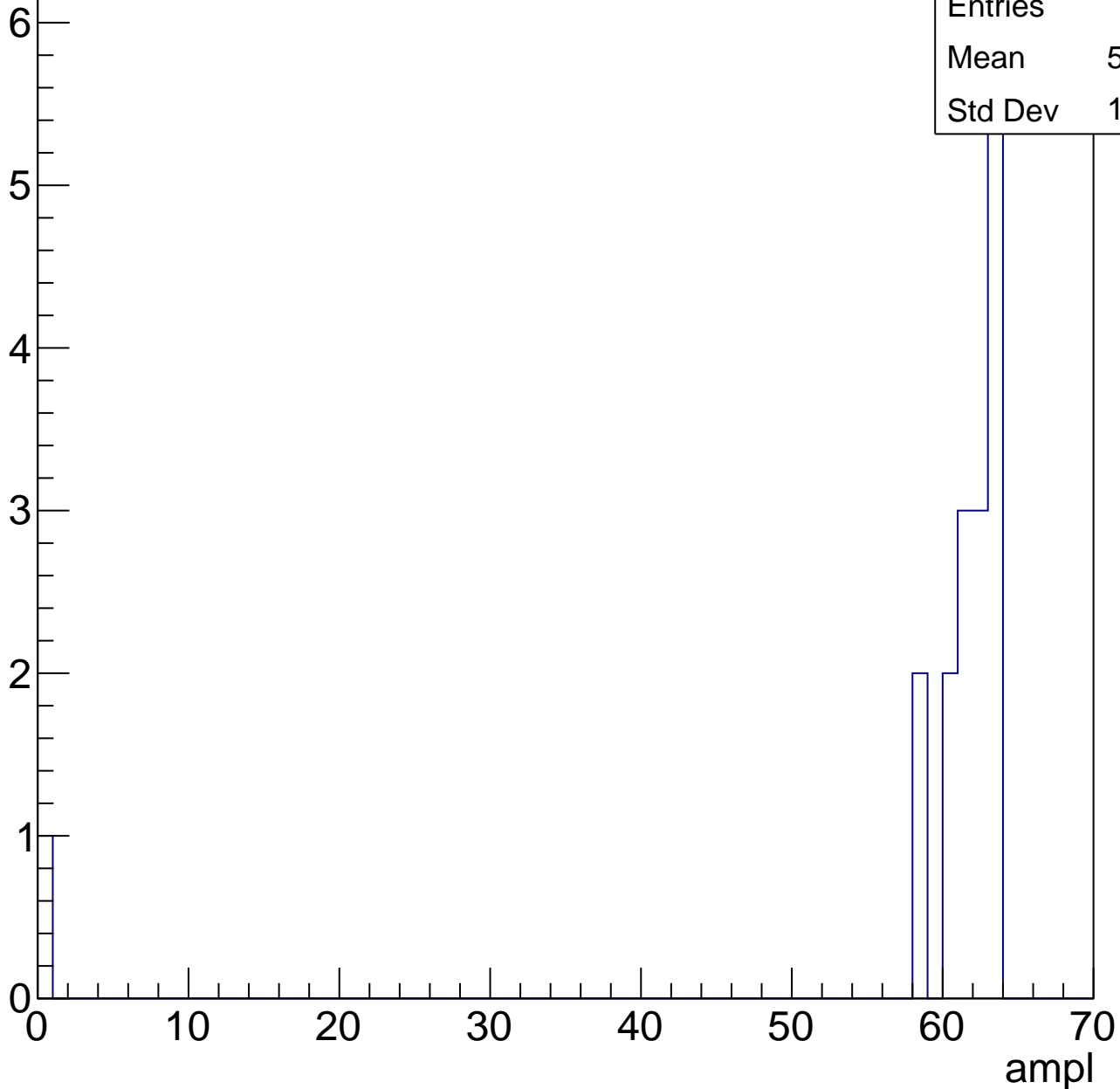


# B1L102S, U20-ch56, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	17
Mean	57.82
Std Dev	14.55

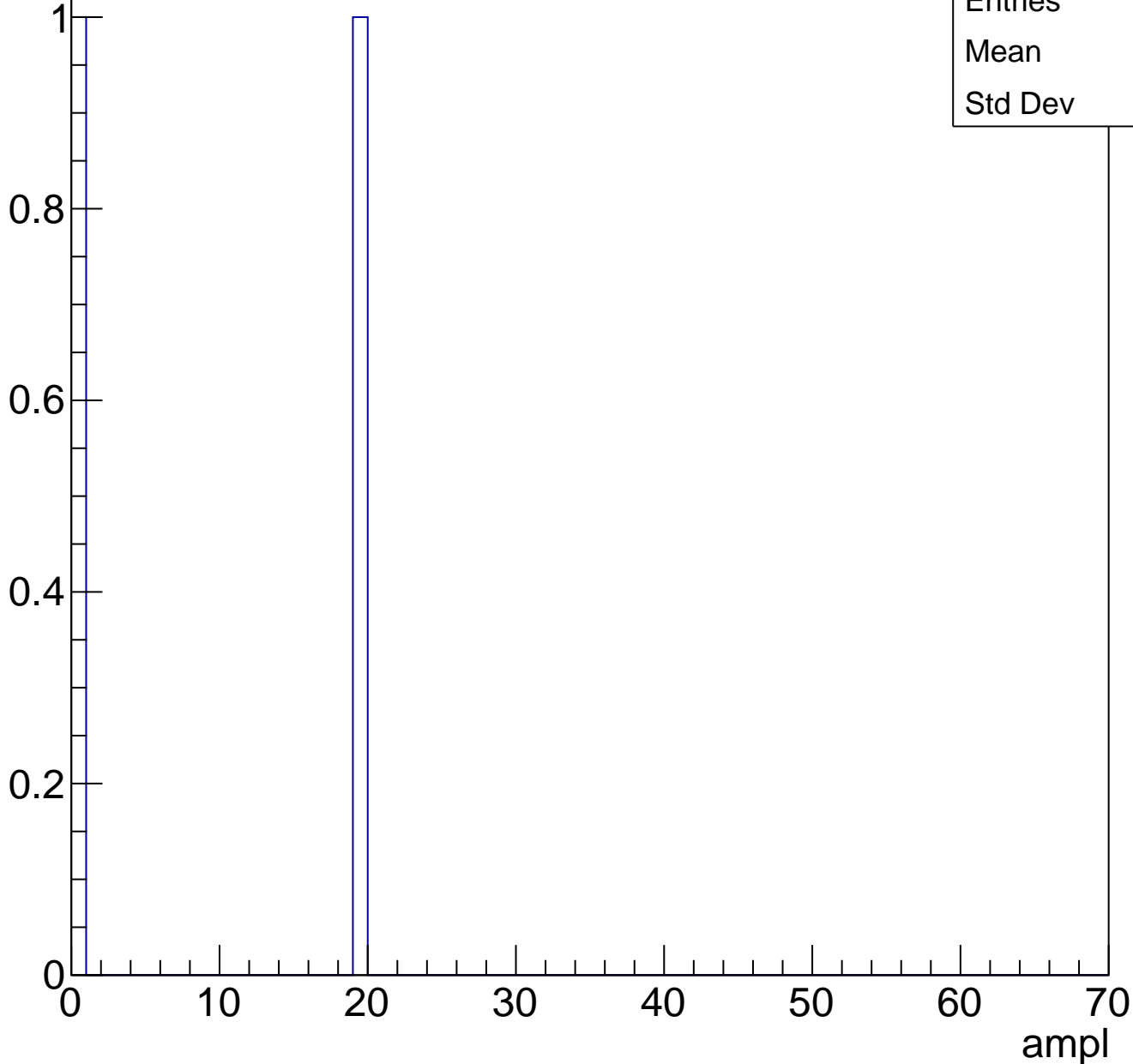




# B1L102S, U20-ch56, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch57, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	68
Mean	28.68
Std Dev	3.215

**Gaus mean : 28.9802**

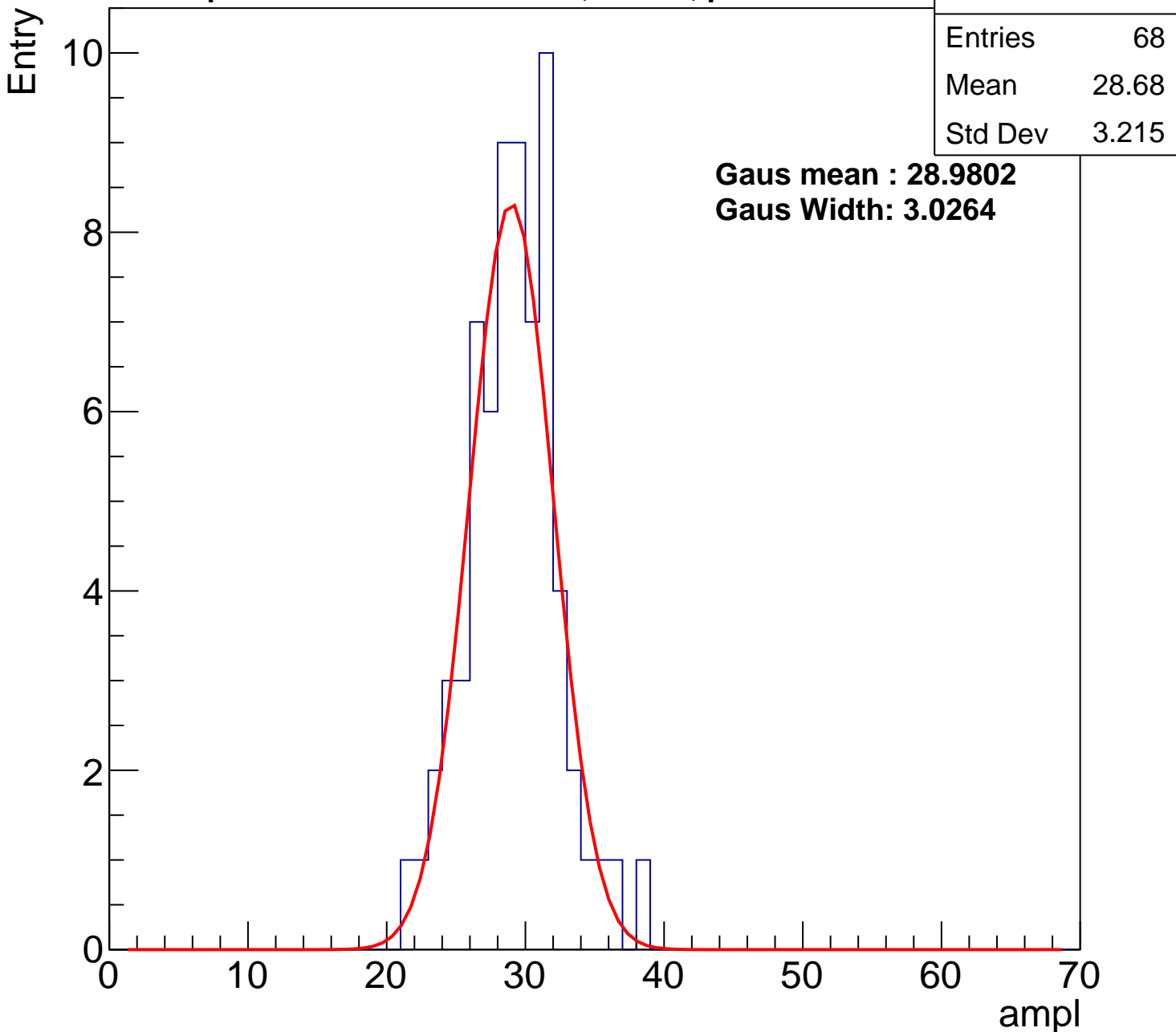
**Gaus Width: 3.0264**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U20-ch57, adc1

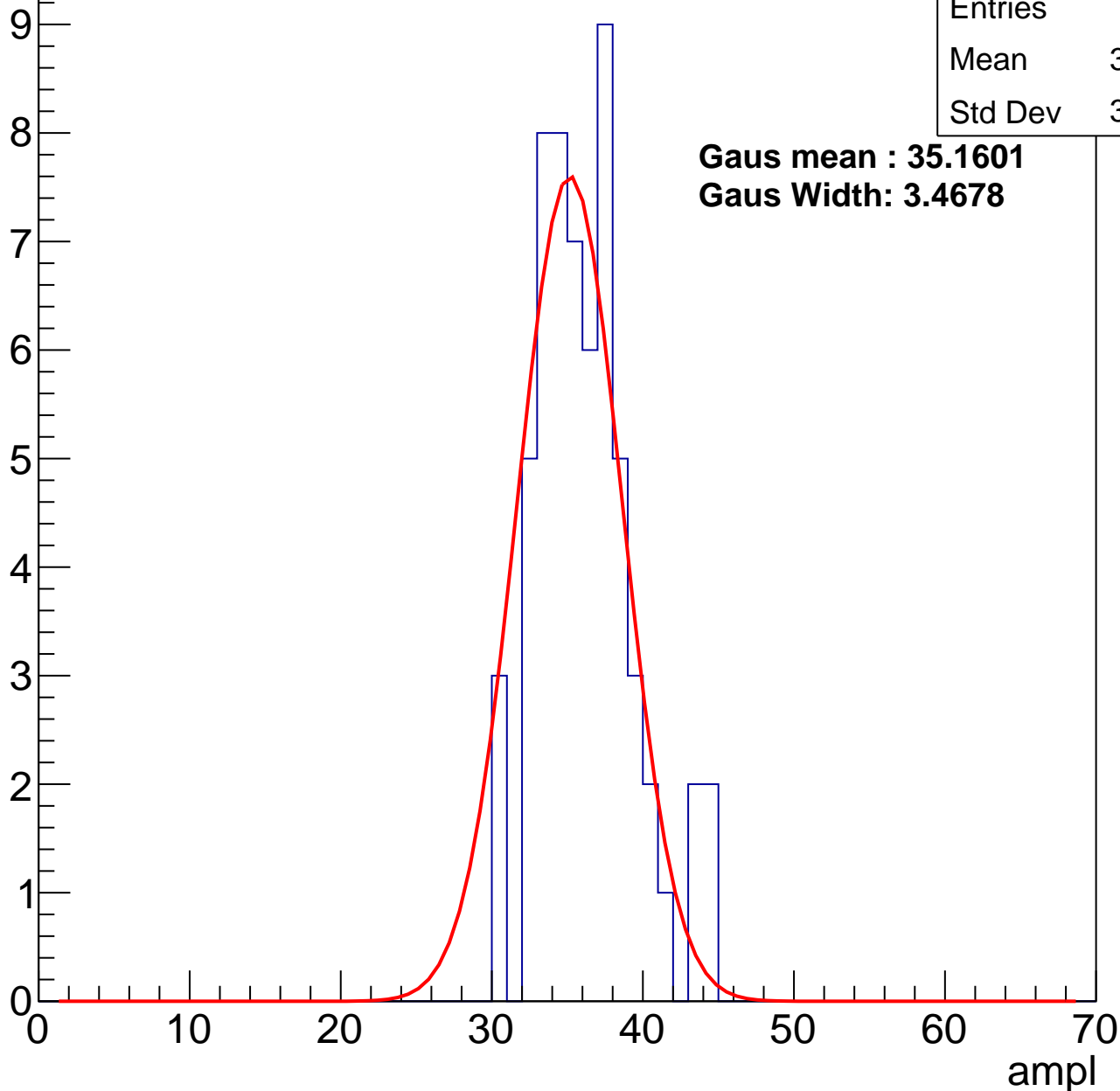
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	35.77
Std Dev	3.226

**Gaus mean : 35.1601**

**Gaus Width: 3.4678**



# B1L102S, U20-ch57, adc2

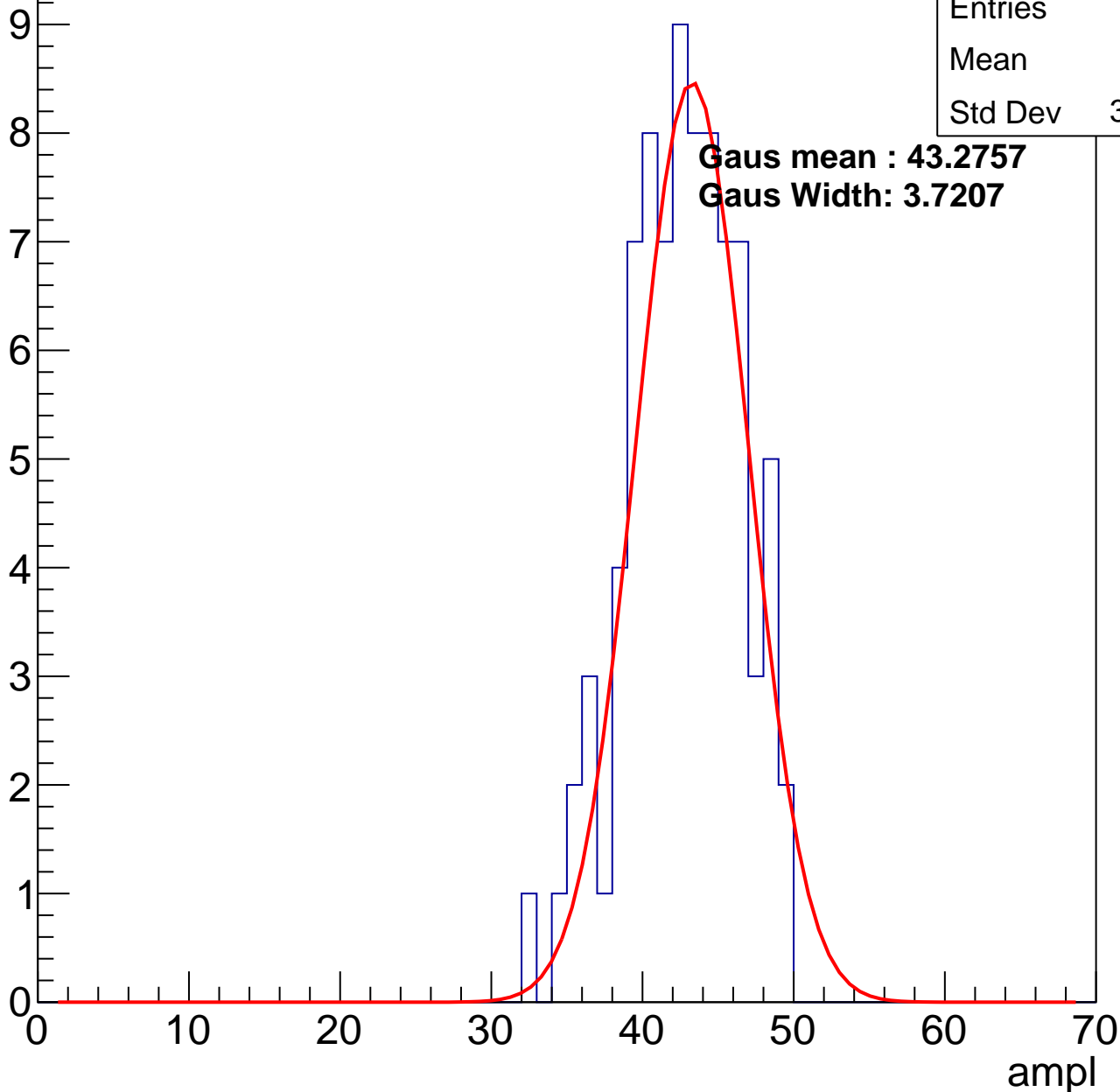
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	83
Mean	42.2
Std Dev	3.682

**Gaus mean : 43.2757**

**Gaus Width: 3.7207**

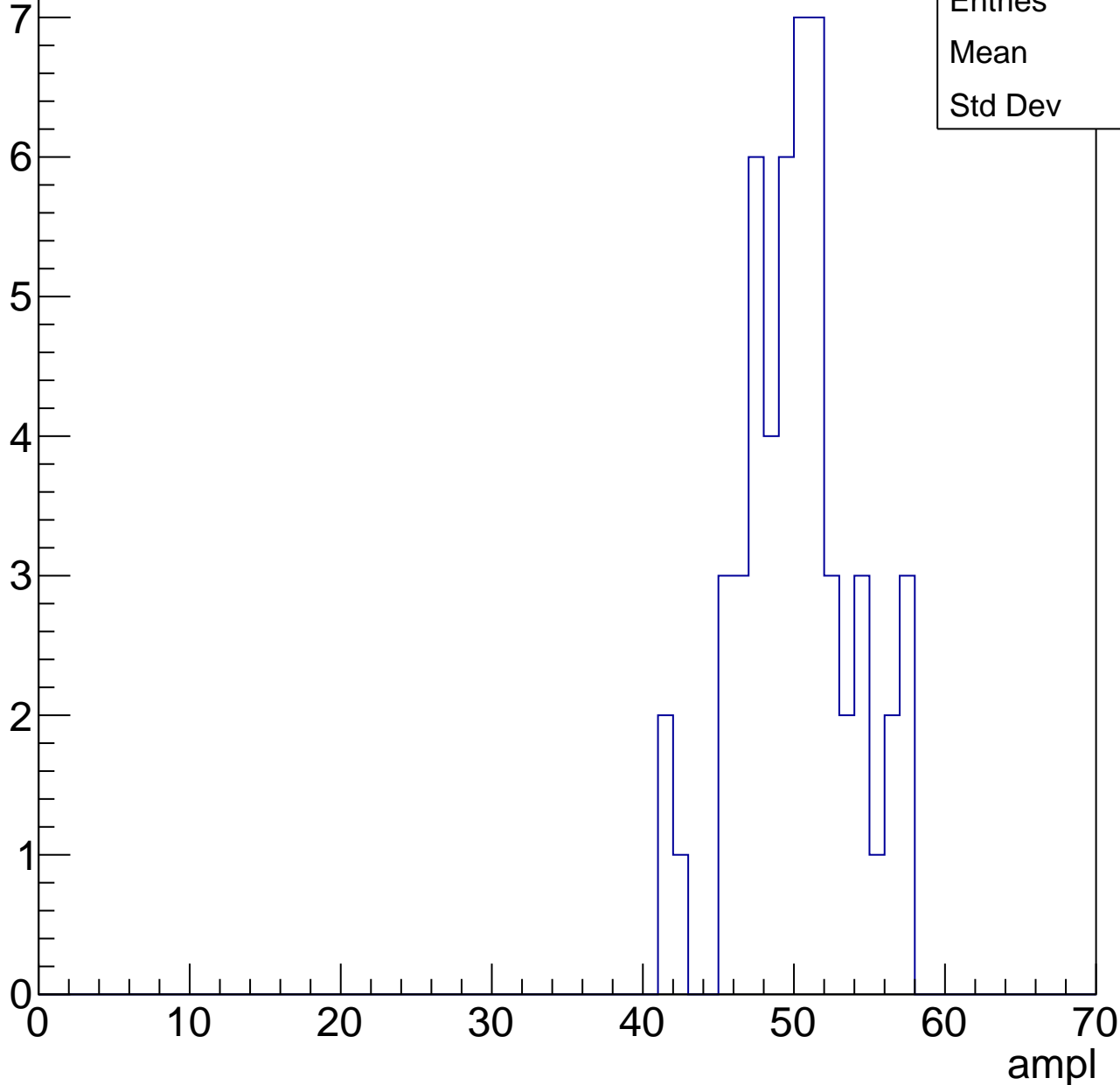


# B1L102S, U20-ch57, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

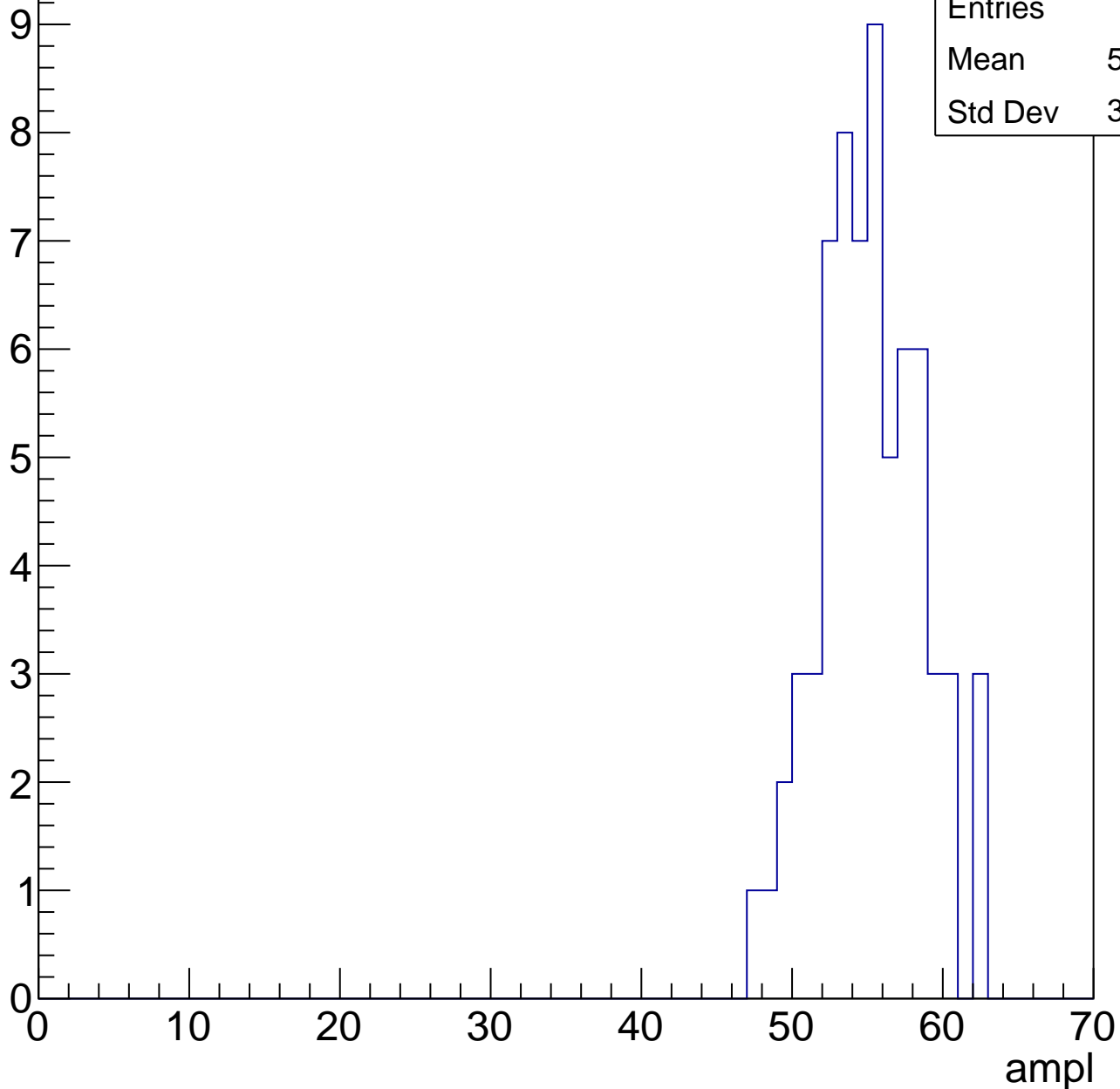
Entries	53
Mean	49.7
Std Dev	3.76



# B1L102S, U20-ch57, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

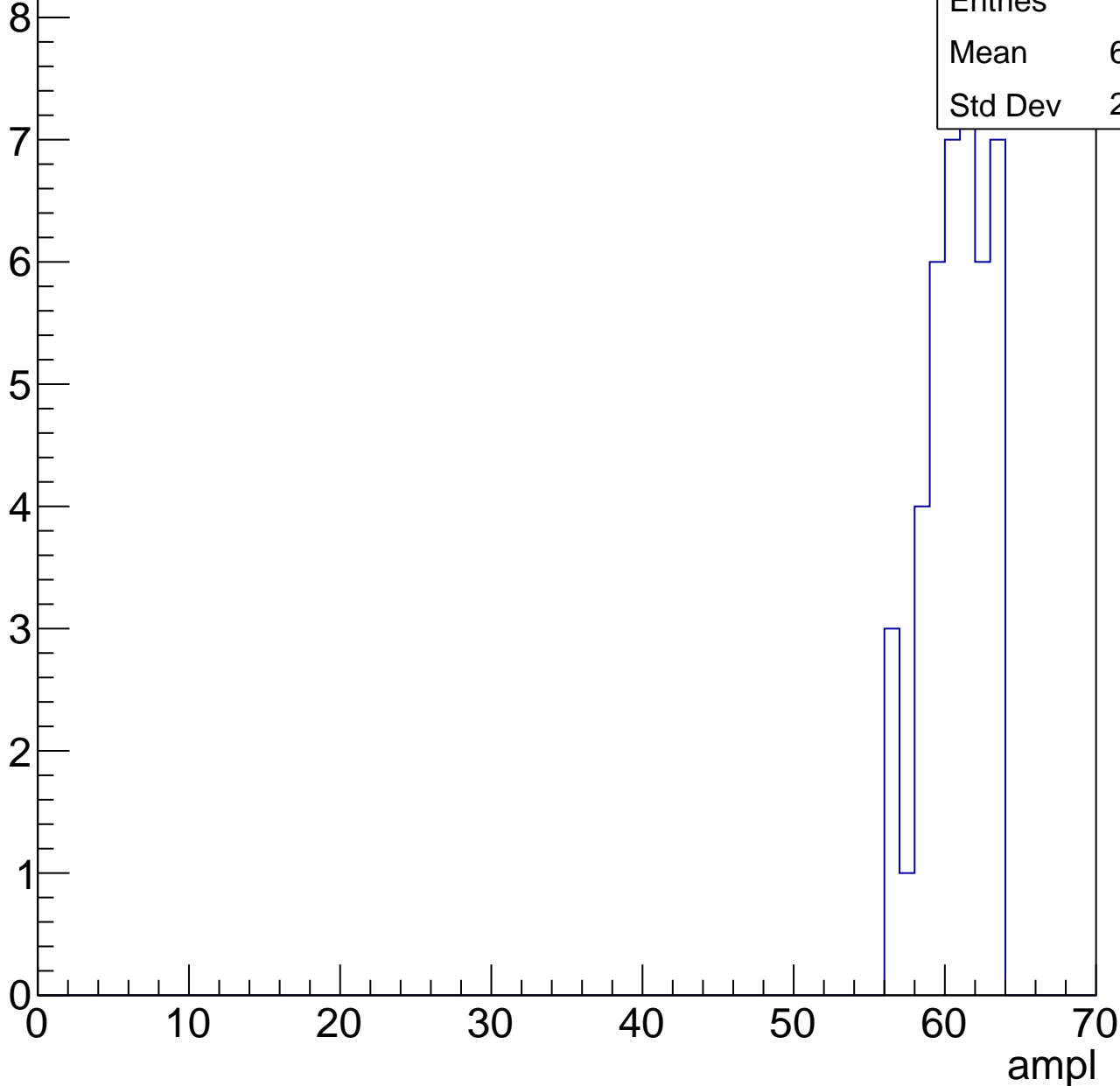


# B1L102S, U20-ch57, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

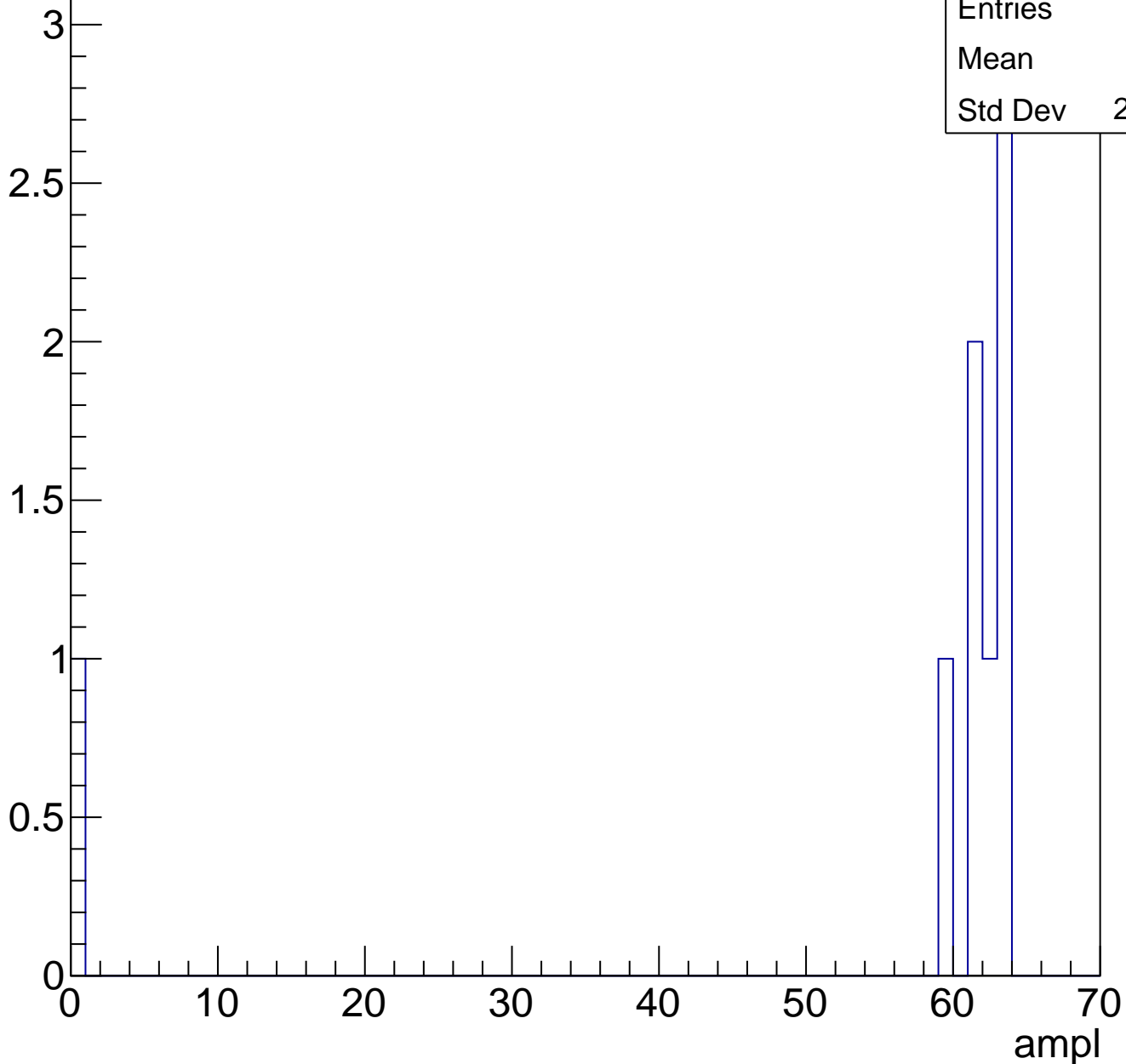
Entries	42
Mean	60.29
Std Dev	2.015



# B1L102S, U20-ch57, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U20-ch57, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch58, adc0

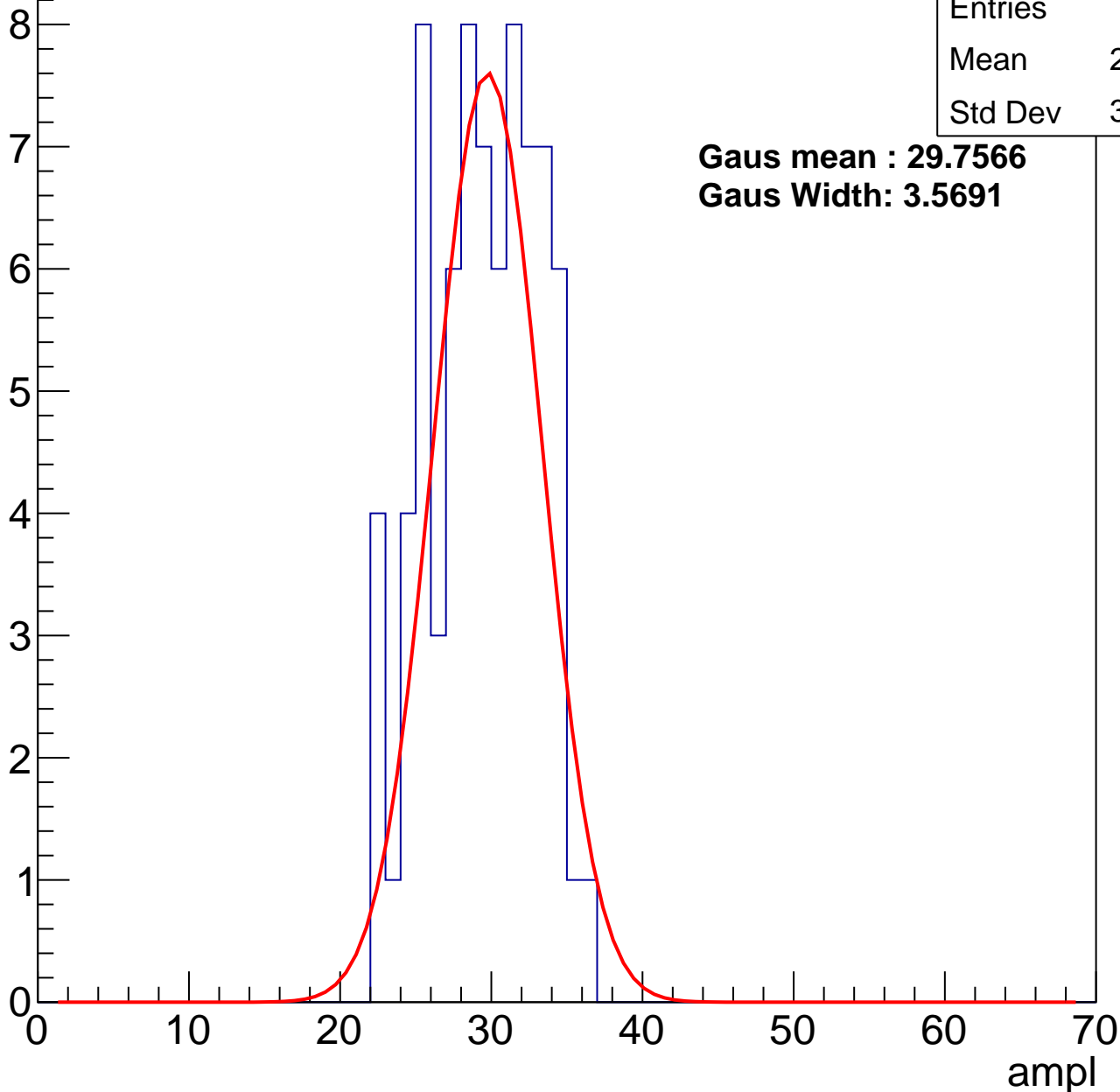
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	28.99
Std Dev	3.544

**Gaus mean : 29.7566**

**Gaus Width: 3.5691**



# B1L102S, U20-ch58, adc1

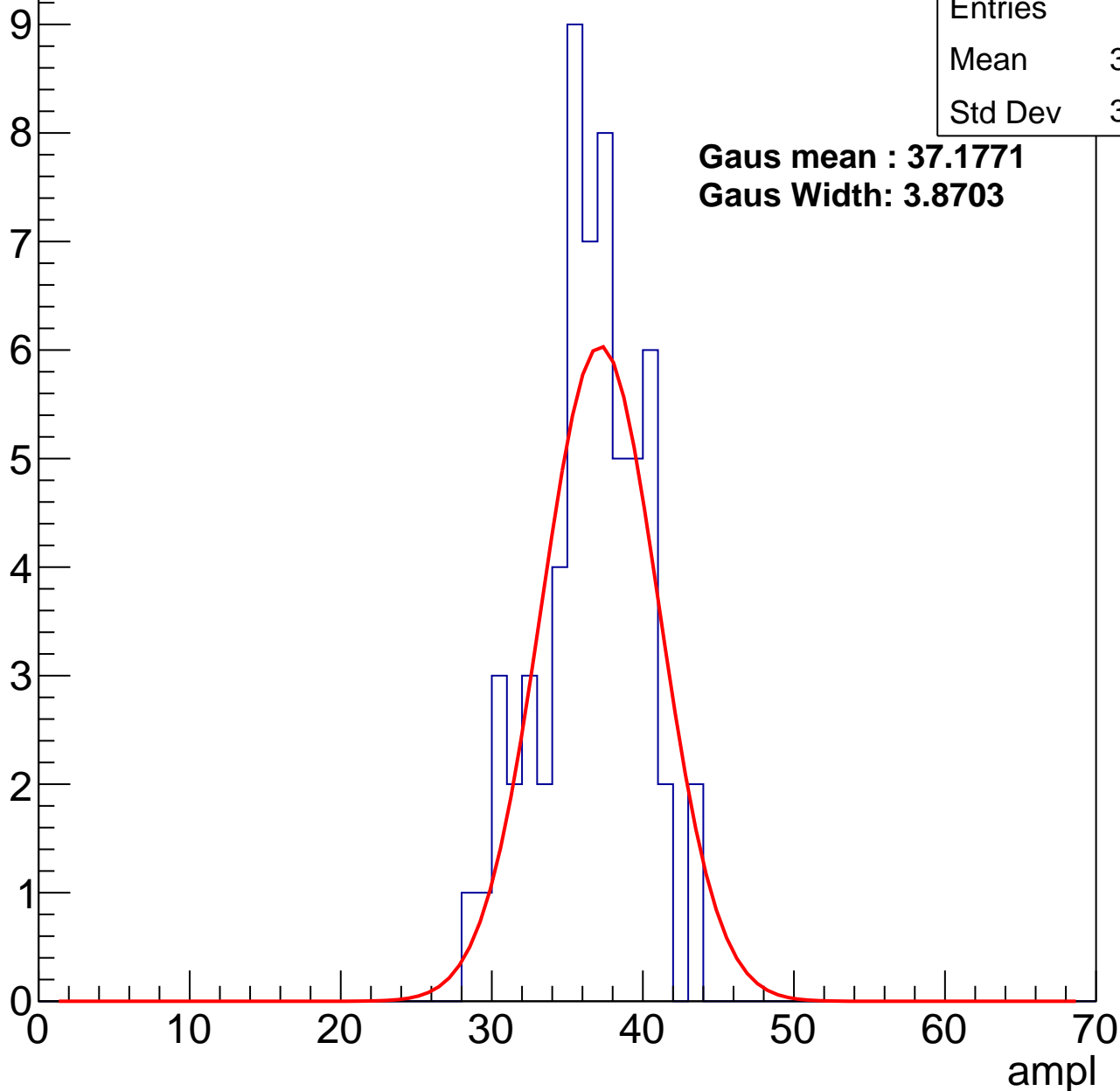
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	36.05
Std Dev	3.364

**Gaus mean : 37.1771**

**Gaus Width: 3.8703**



# B1L102S, U20-ch58, adc2

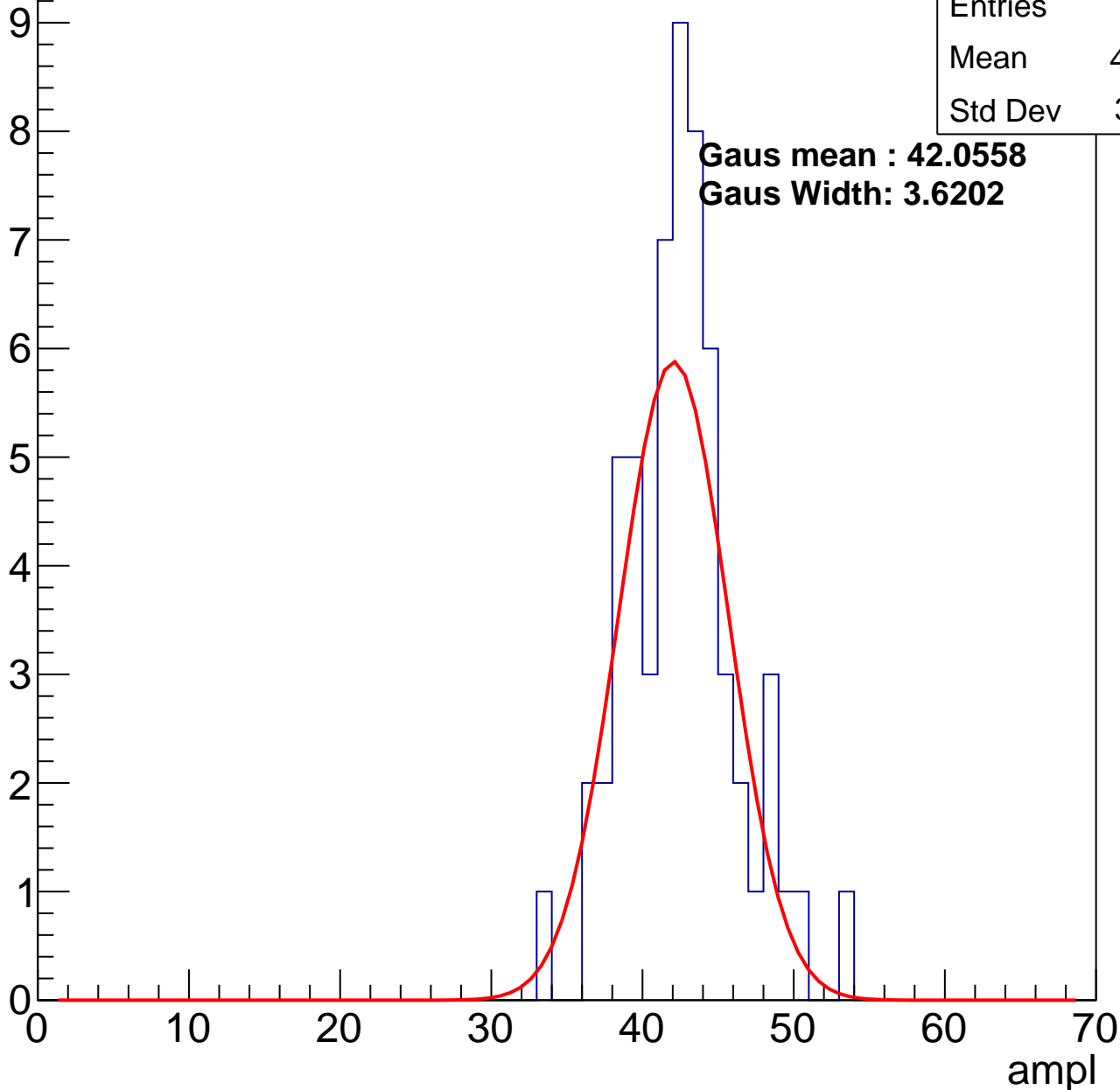
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	42.12
Std Dev	3.661

**Gaus mean : 42.0558**

**Gaus Width: 3.6202**

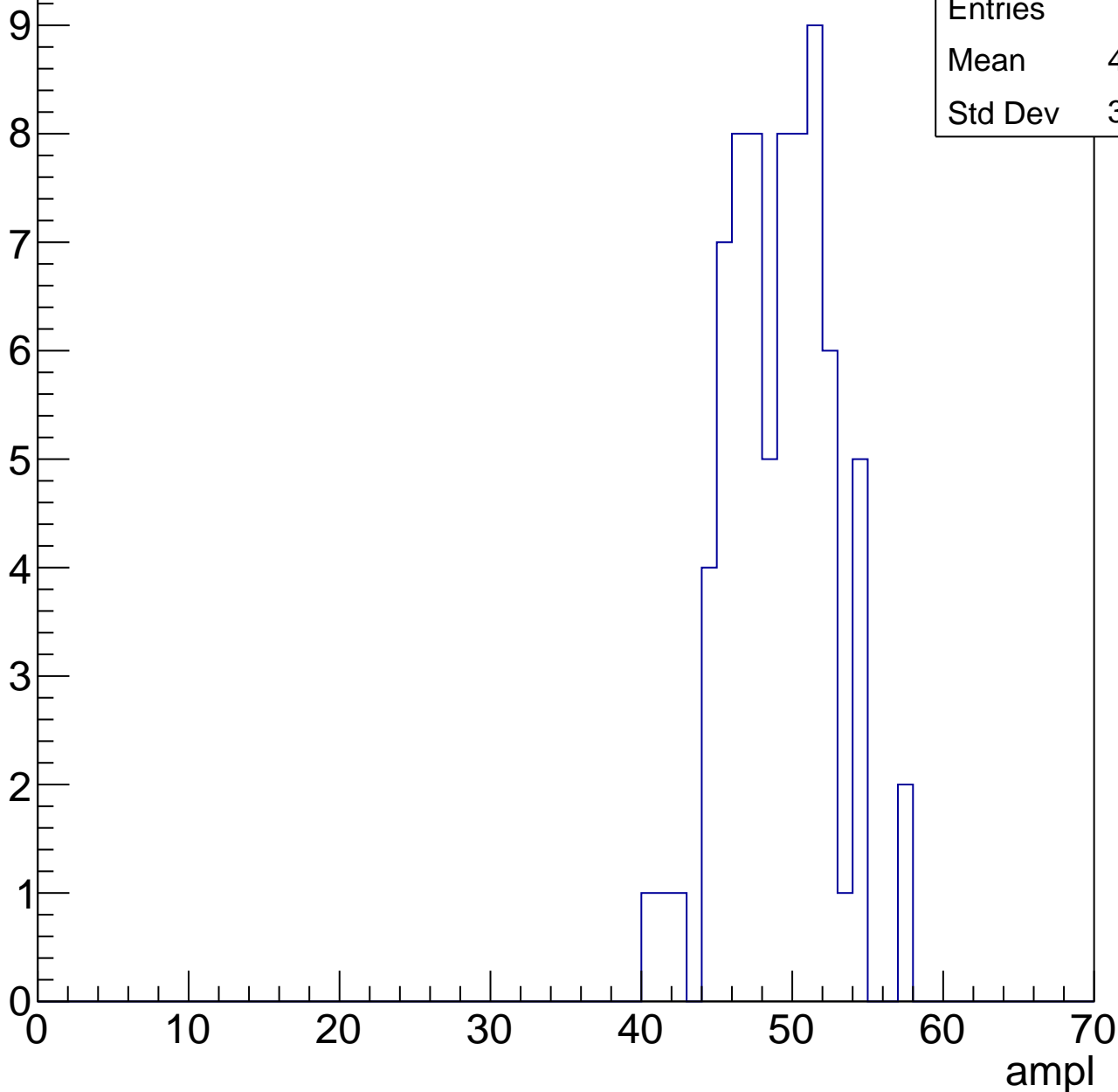


# B1L102S, U20-ch58, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	48.62
Std Dev	3.432

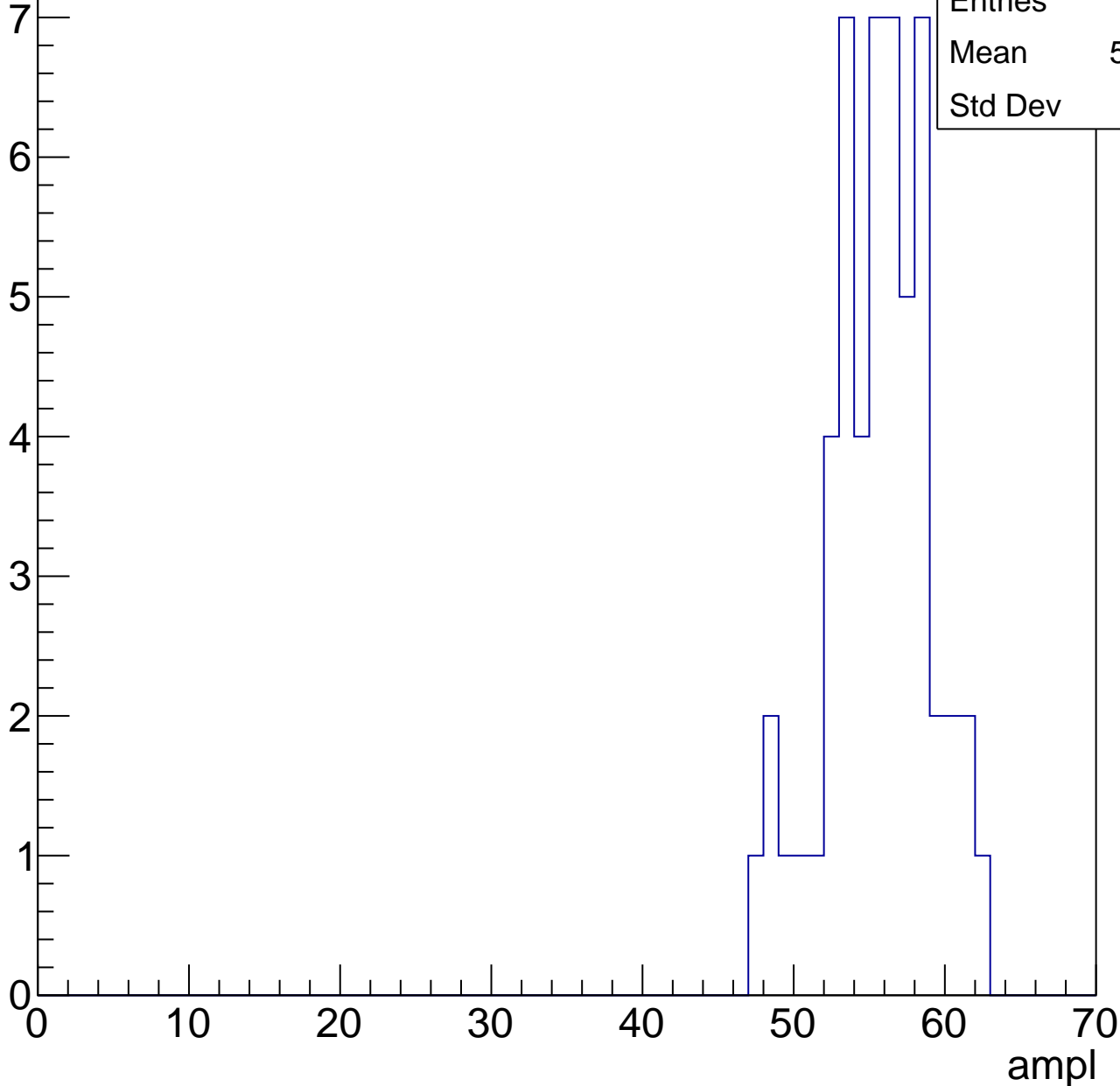


# B1L102S, U20-ch58, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	55.15
Std Dev	3.33

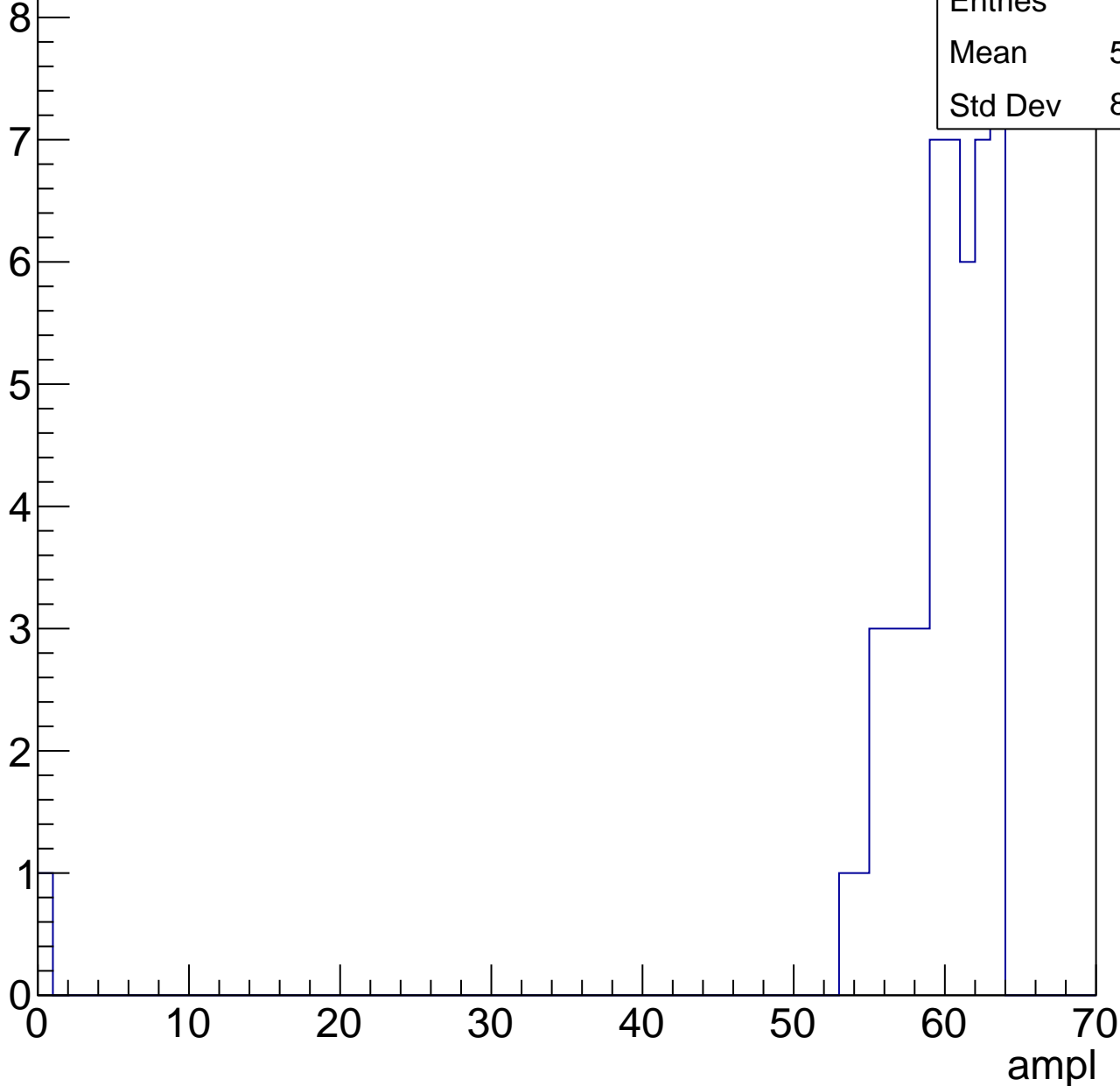


# B1L102S, U20-ch58, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	58.44
Std Dev	8.762



# B1L102S, U20-ch58, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

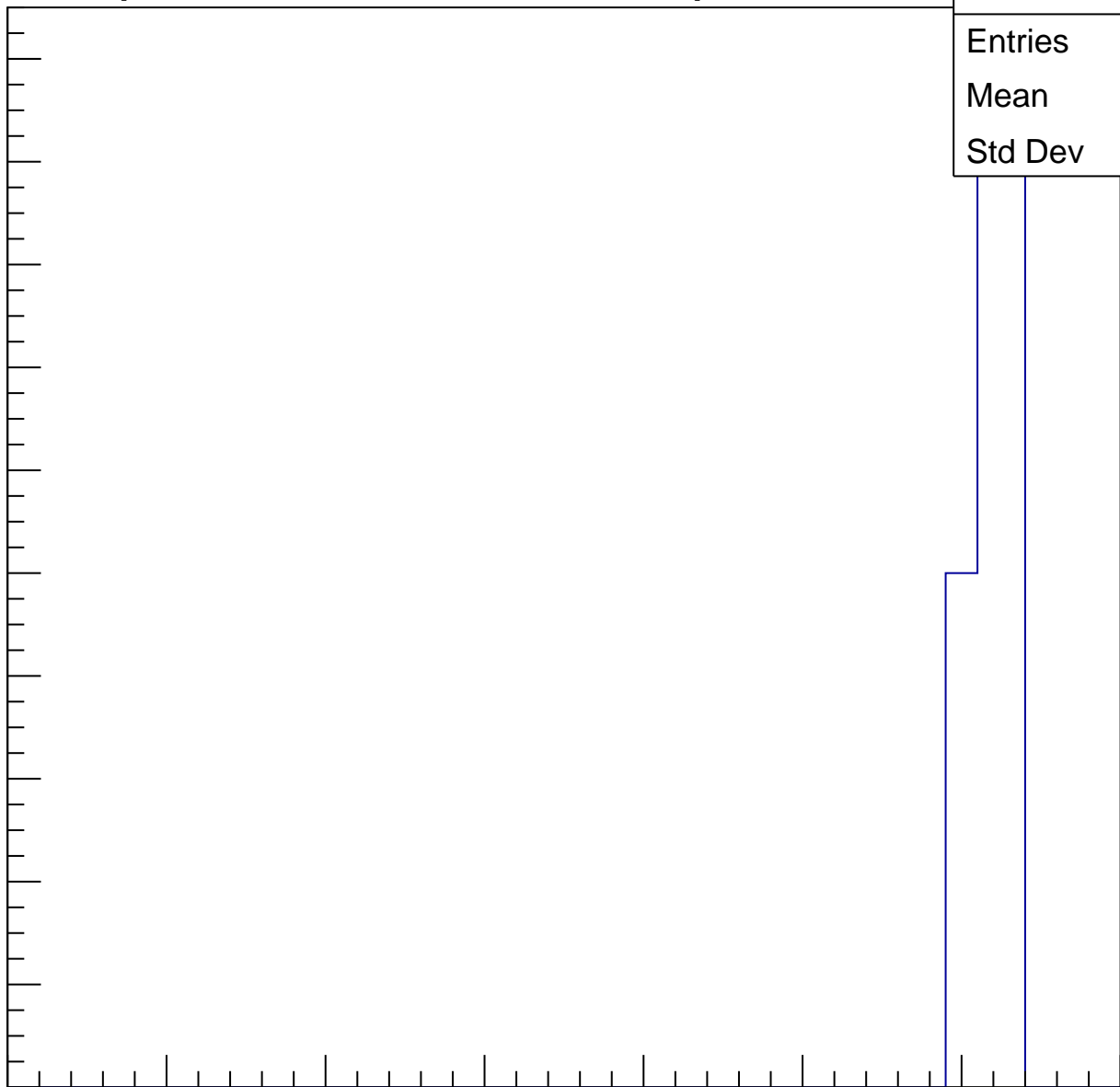
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	8
Mean	61.38
Std Dev	1.317

0 10 20 30 40 50 60 70

ampl





# B1L102S, U20-ch58, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch59, adc0

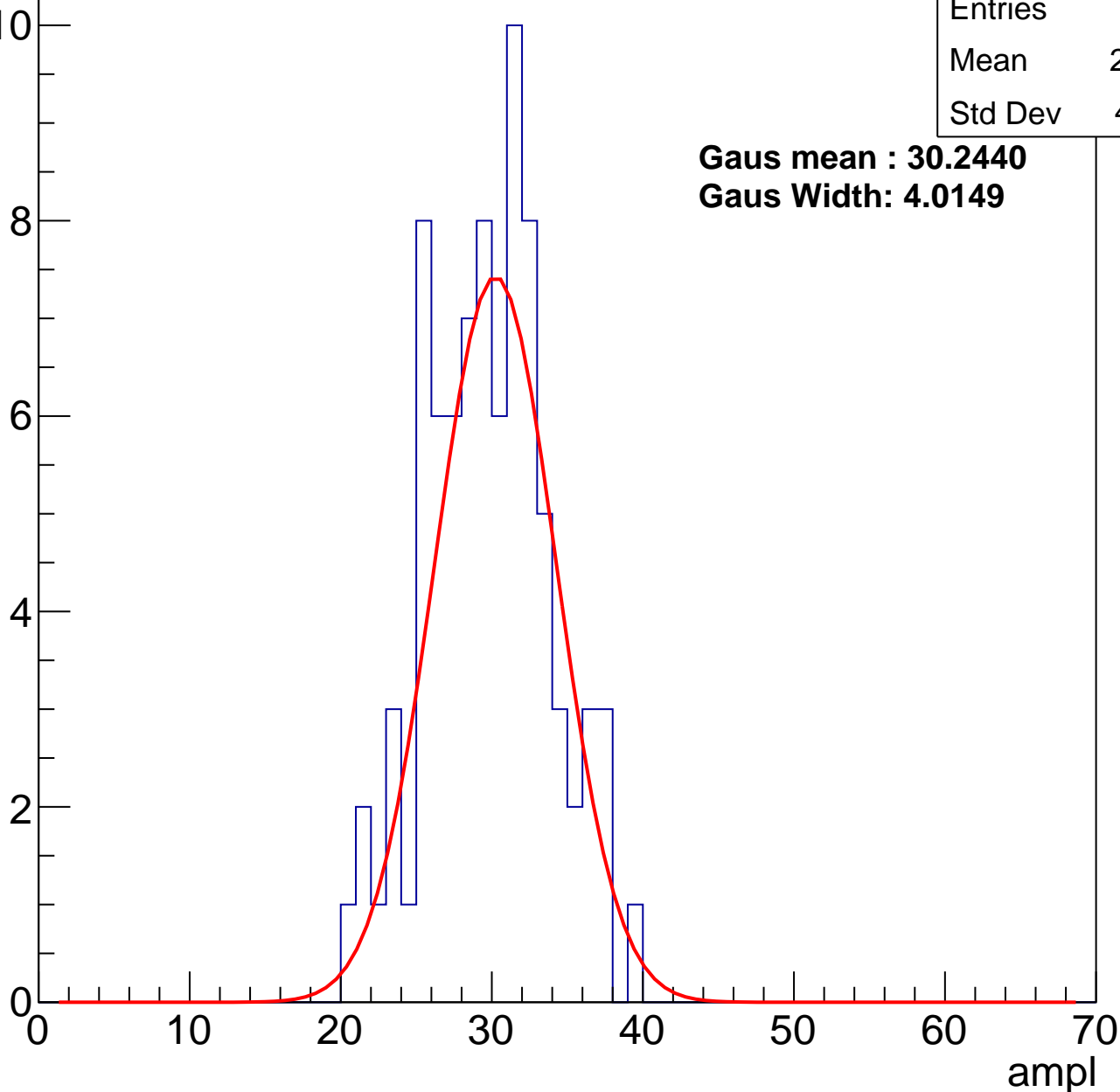
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	84
Mean	29.33
Std Dev	4.051

**Gaus mean : 30.2440**

**Gaus Width: 4.0149**



# B1L102S, U20-ch59, adc1

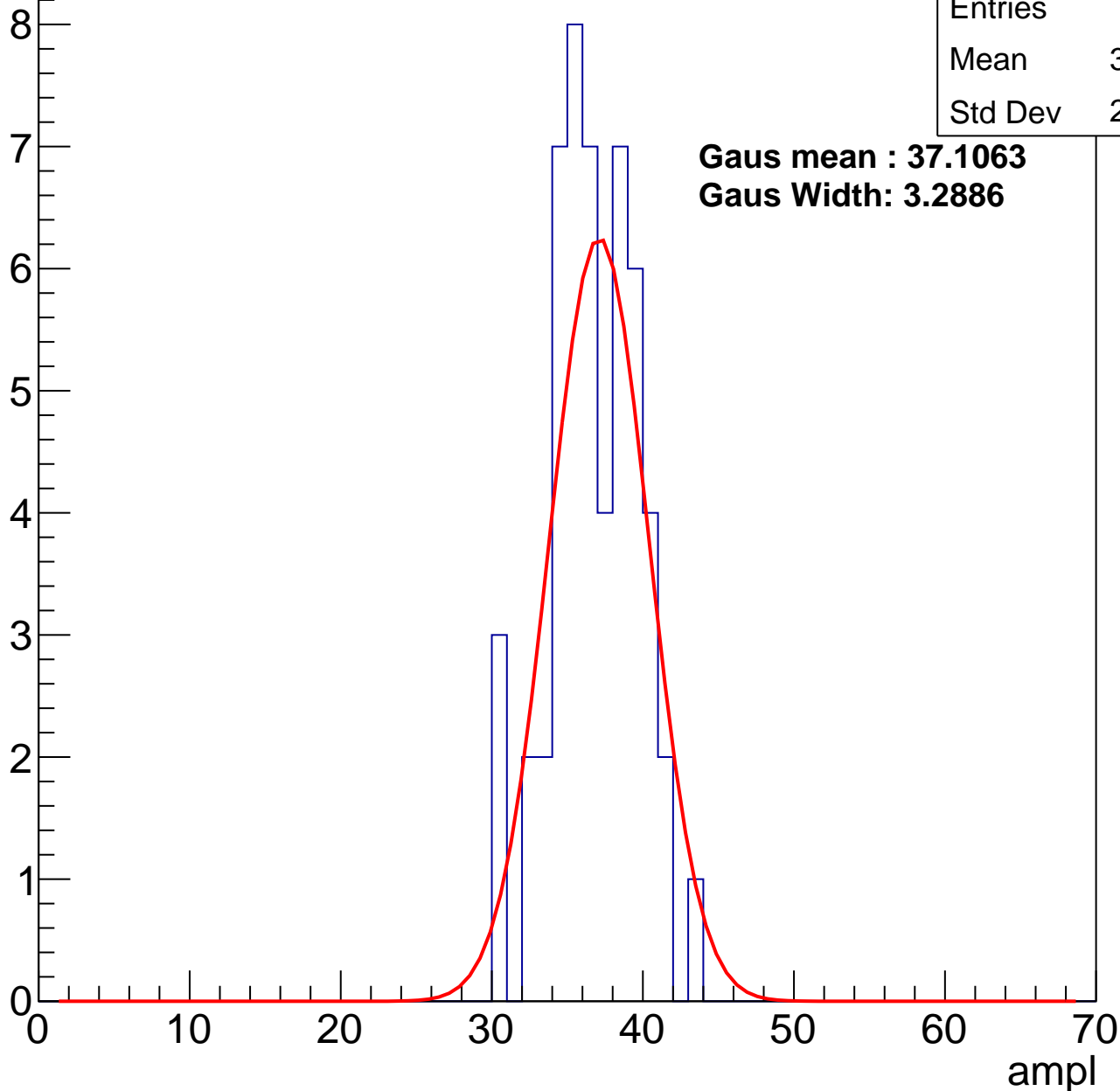
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	36.28
Std Dev	2.877

**Gaus mean : 37.1063**

**Gaus Width: 3.2886**



# B1L102S, U20-ch59, adc2

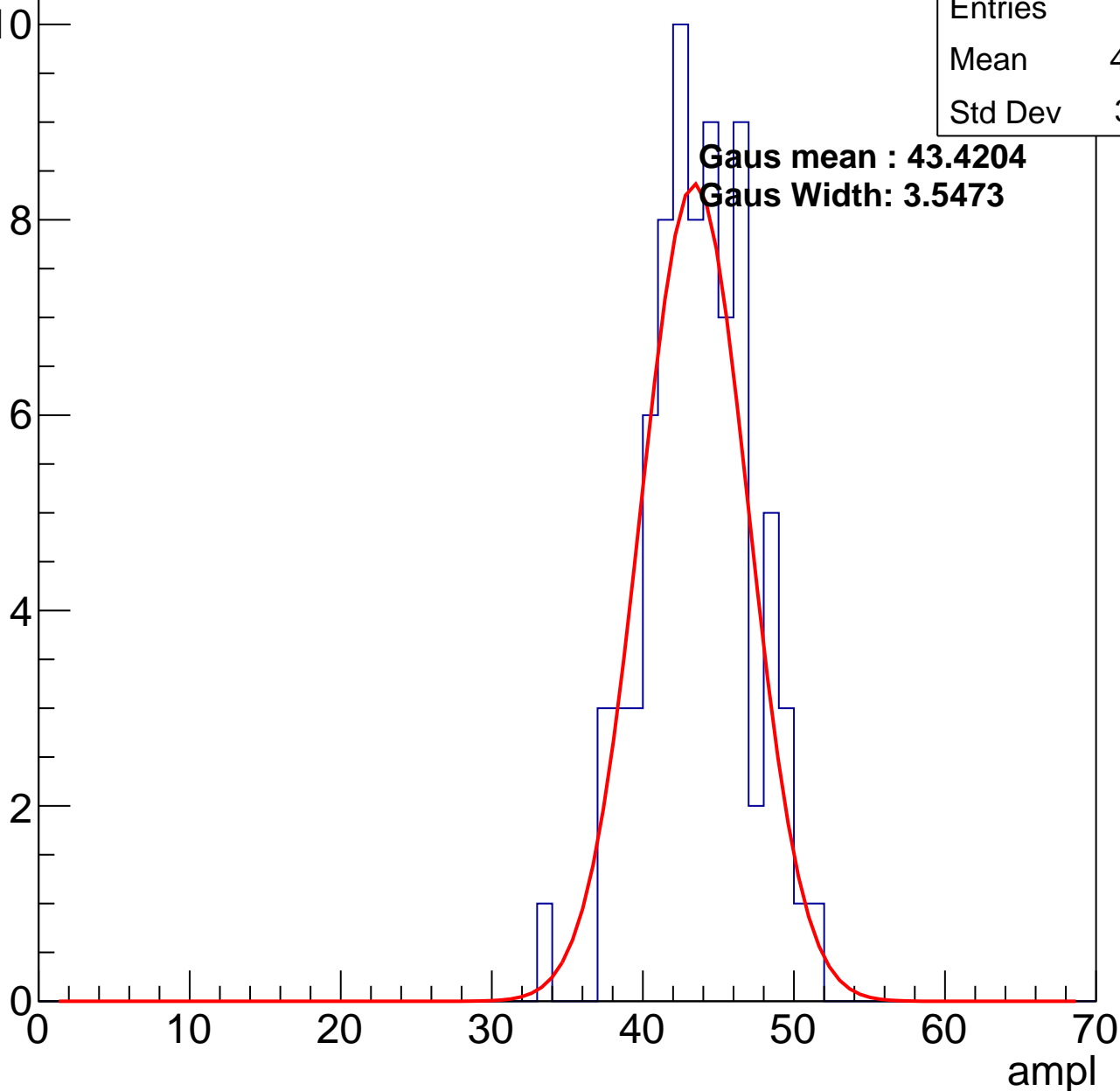
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	79
Mean	43.22
Std Dev	3.411

**Gaus mean : 43.4204**

**Gaus Width: 3.5473**

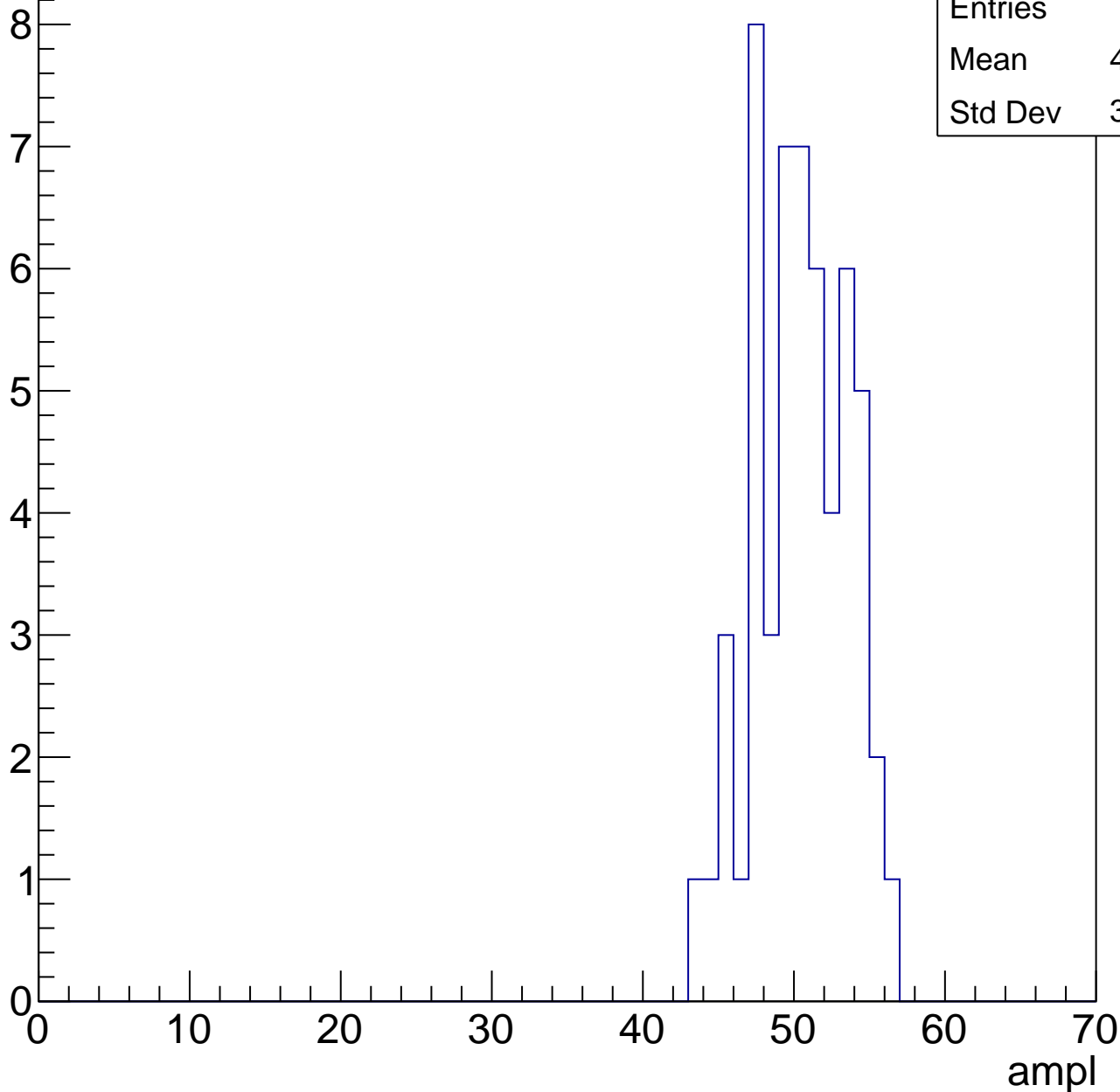


# B1L102S, U20-ch59, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	49.98
Std Dev	3.042

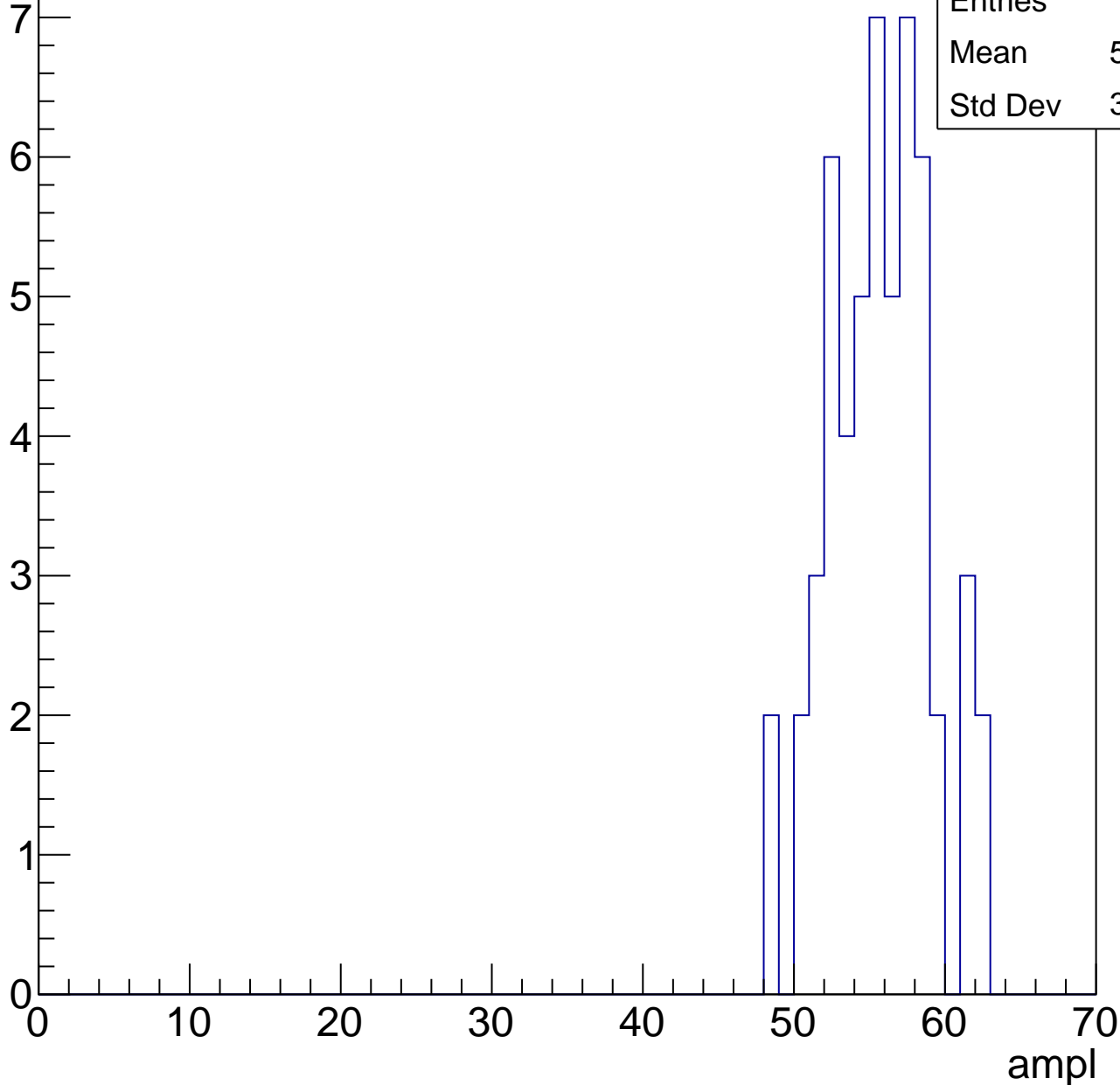


# B1L102S, U20-ch59, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	55.19
Std Dev	3.317



# B1L102S, U20-ch59, adc5

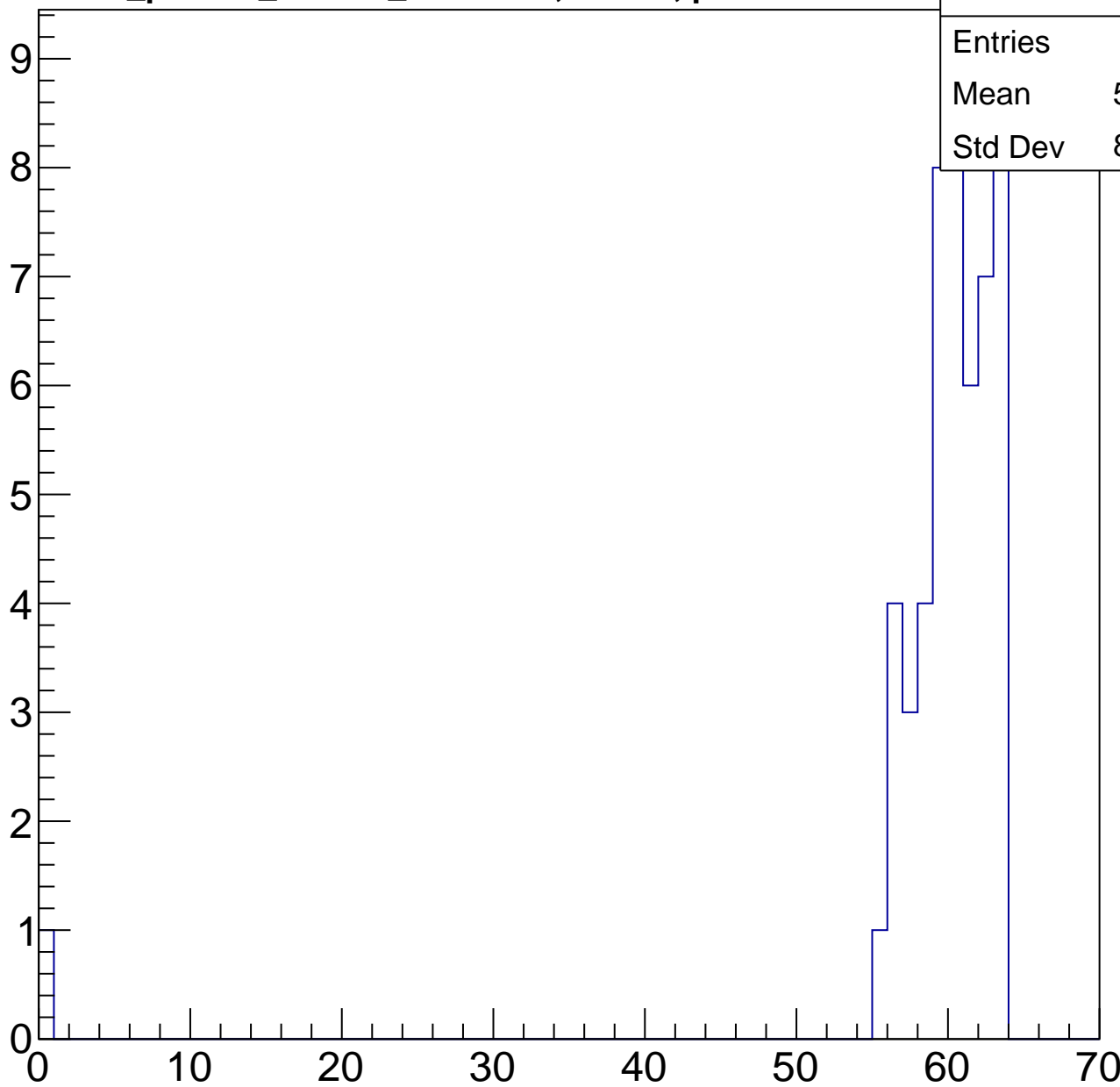
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	51
Mean	58.78
Std Dev	8.598

ampl



# B1L102S, U20-ch59, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

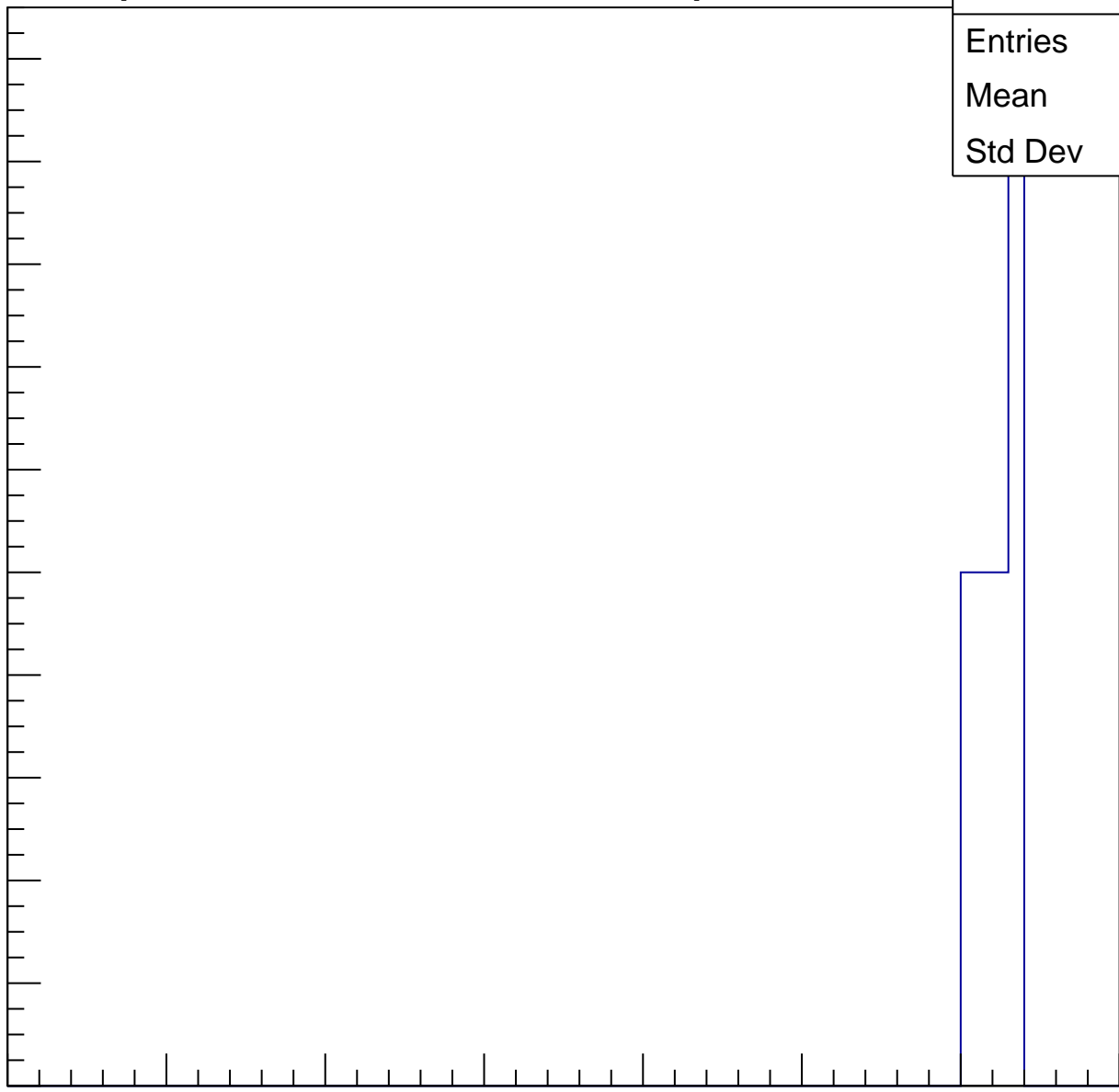
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	61.8
Std Dev	1.166

ampl

0 10 20 30 40 50 60 70





# B1L102S, U20-ch59, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U20-ch60, adc0

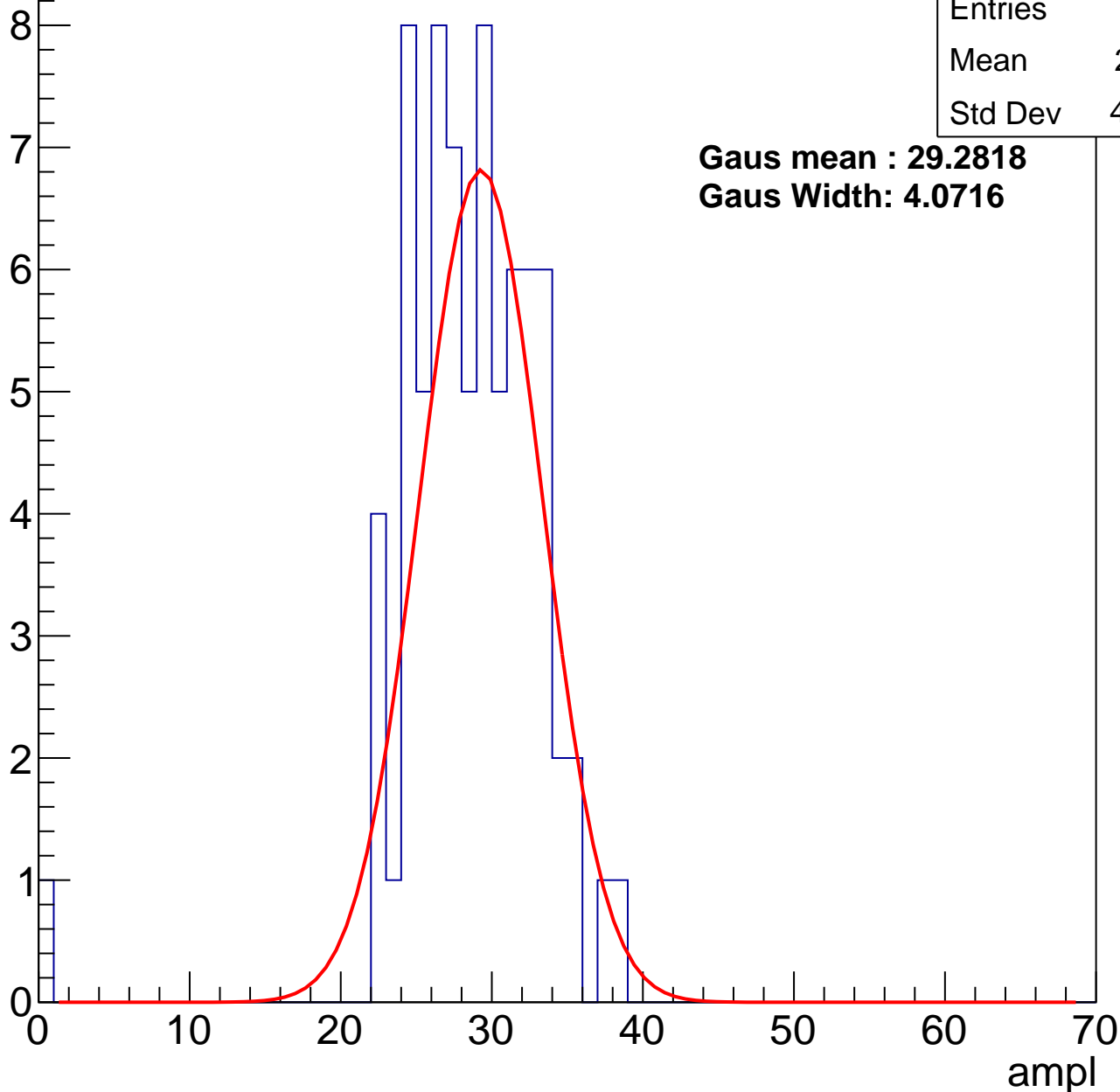
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	28.11
Std Dev	4.925

**Gaus mean : 29.2818**

**Gaus Width: 4.0716**



# B1L102S, U20-ch60, adc1

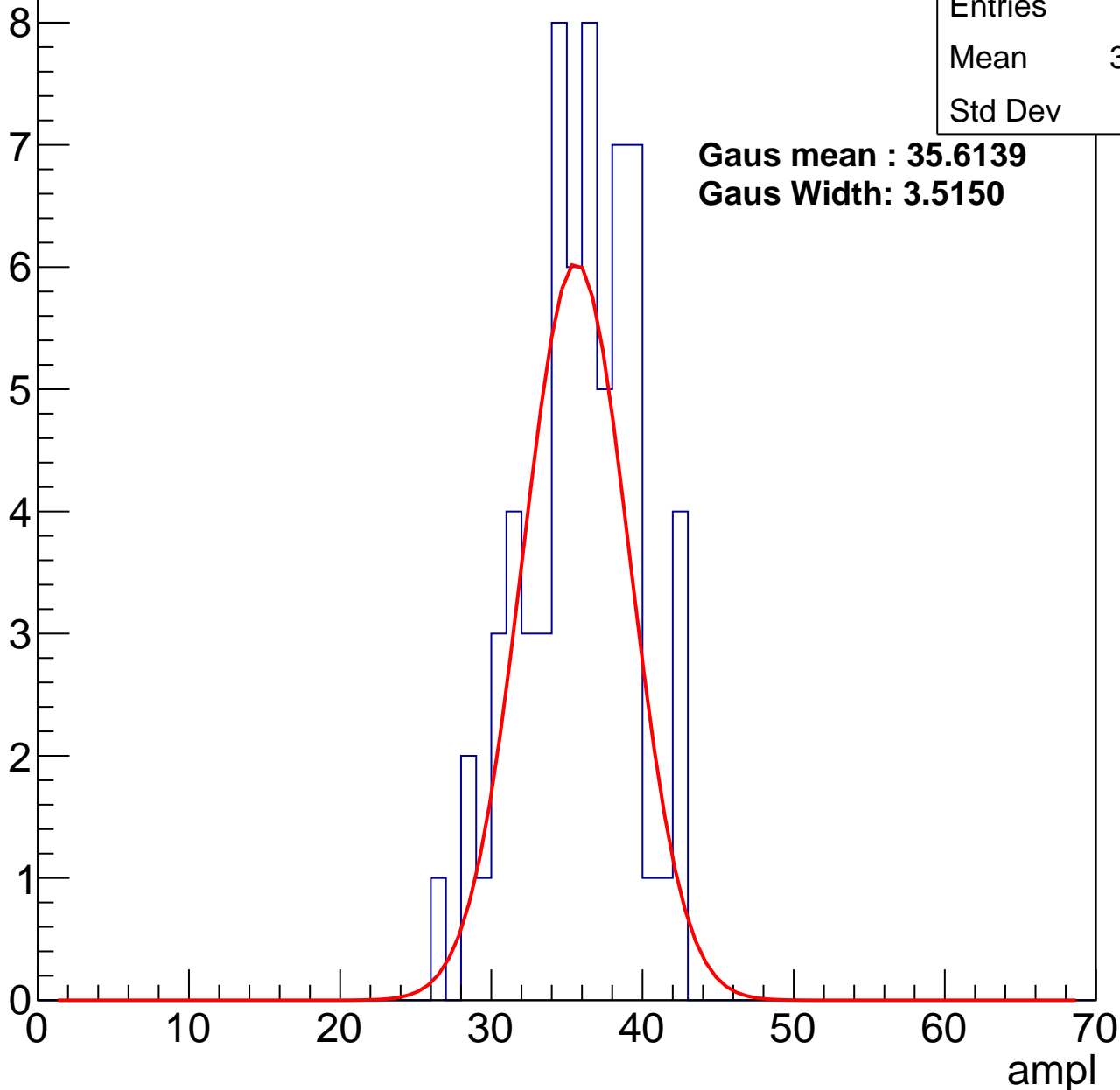
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	35.36
Std Dev	3.65

**Gaus mean : 35.6139**

**Gaus Width: 3.5150**



# B1L102S, U20-ch60, adc2

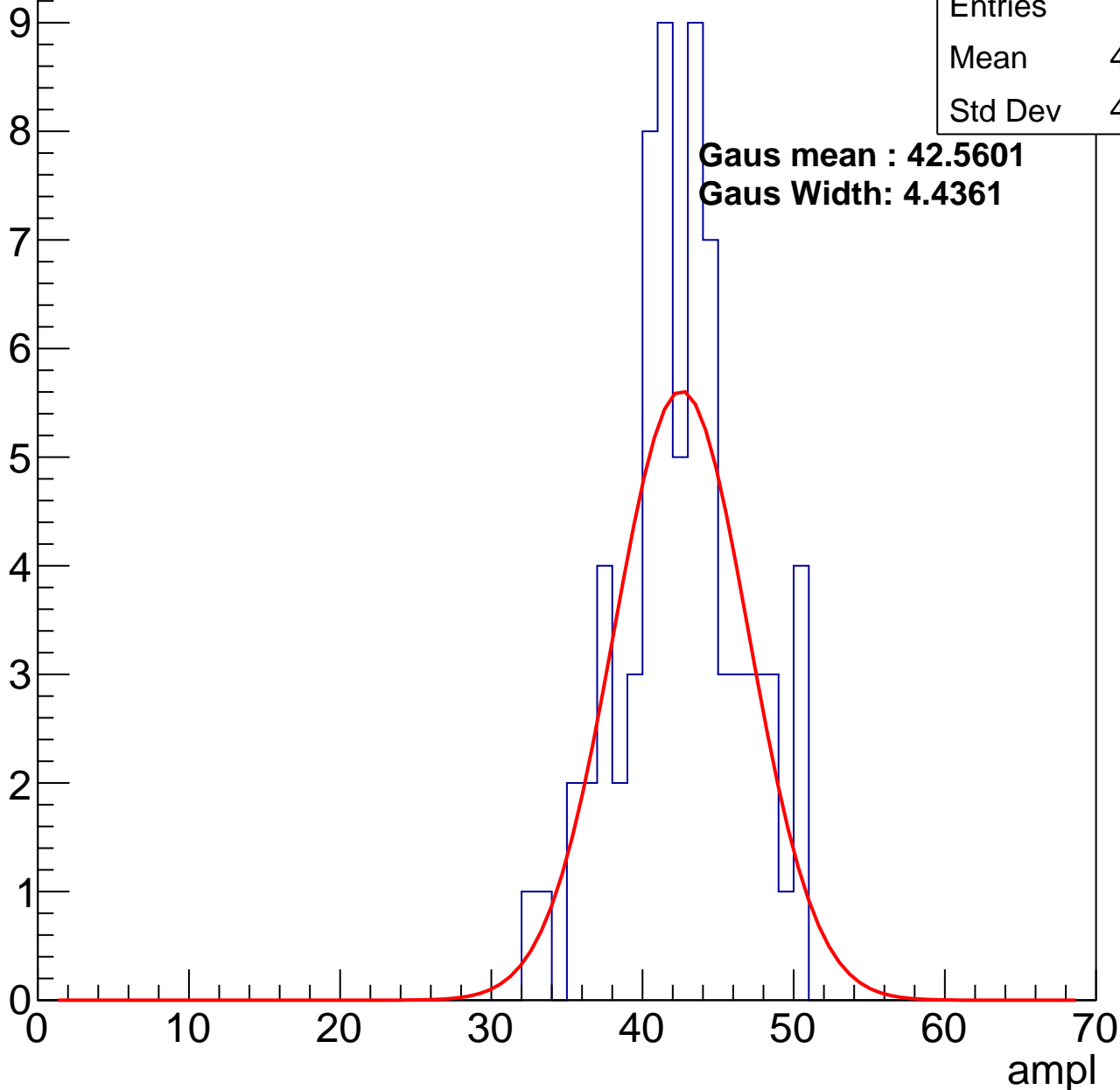
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	42.13
Std Dev	4.053

**Gaus mean : 42.5601**

**Gaus Width: 4.4361**

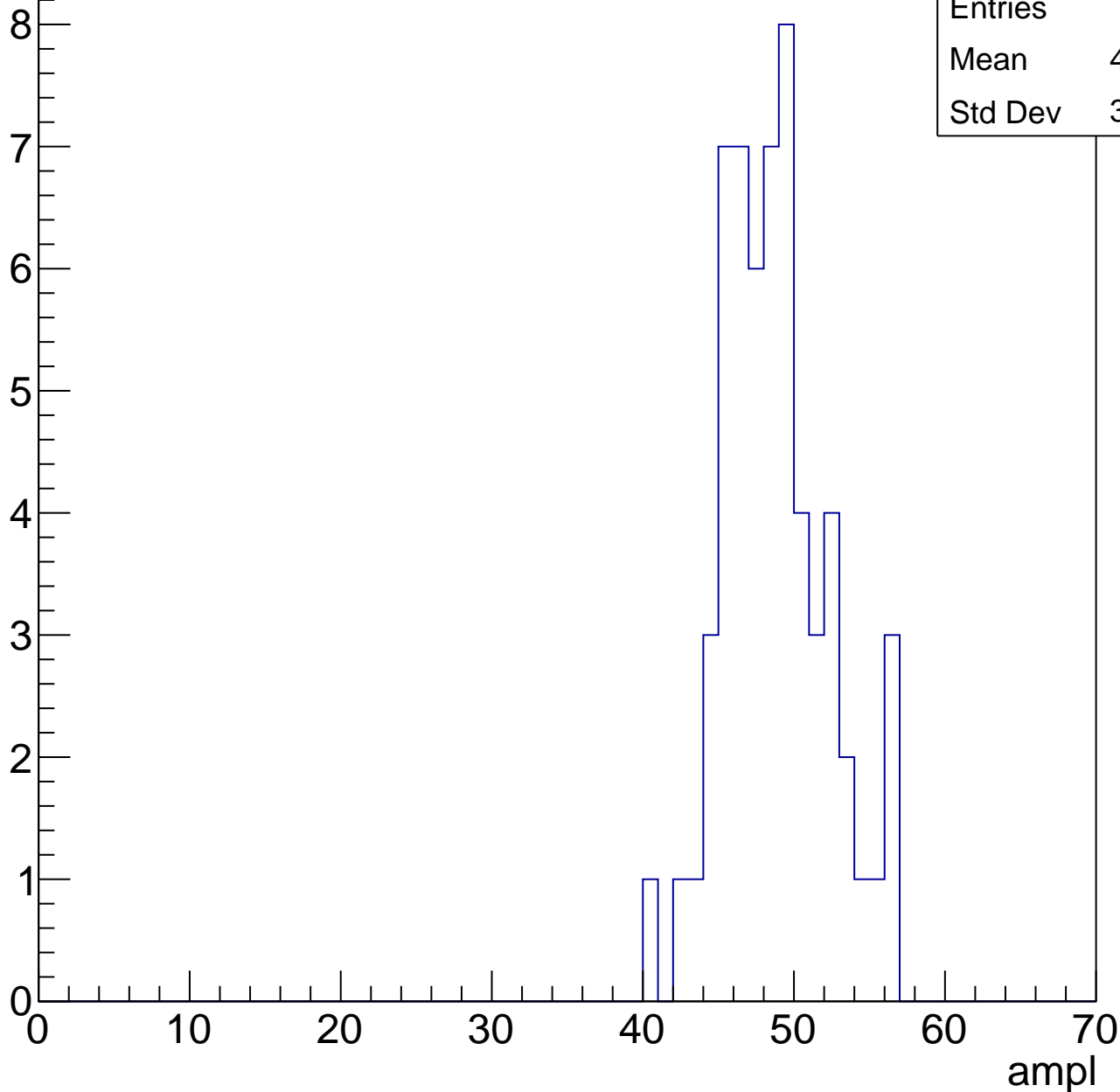


# B1L102S, U20-ch60, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	48.27
Std Dev	3.463

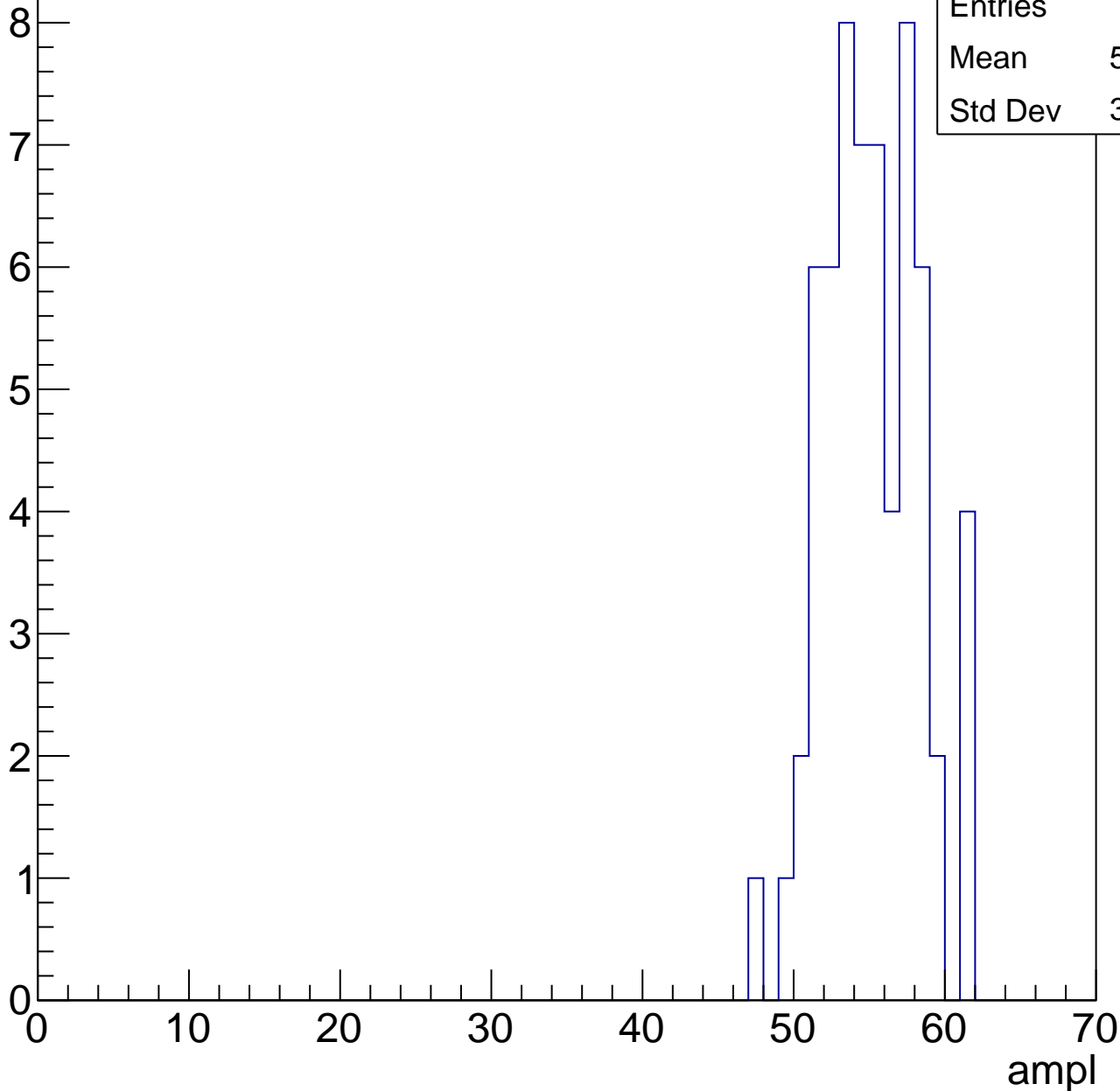


# B1L102S, U20-ch60, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

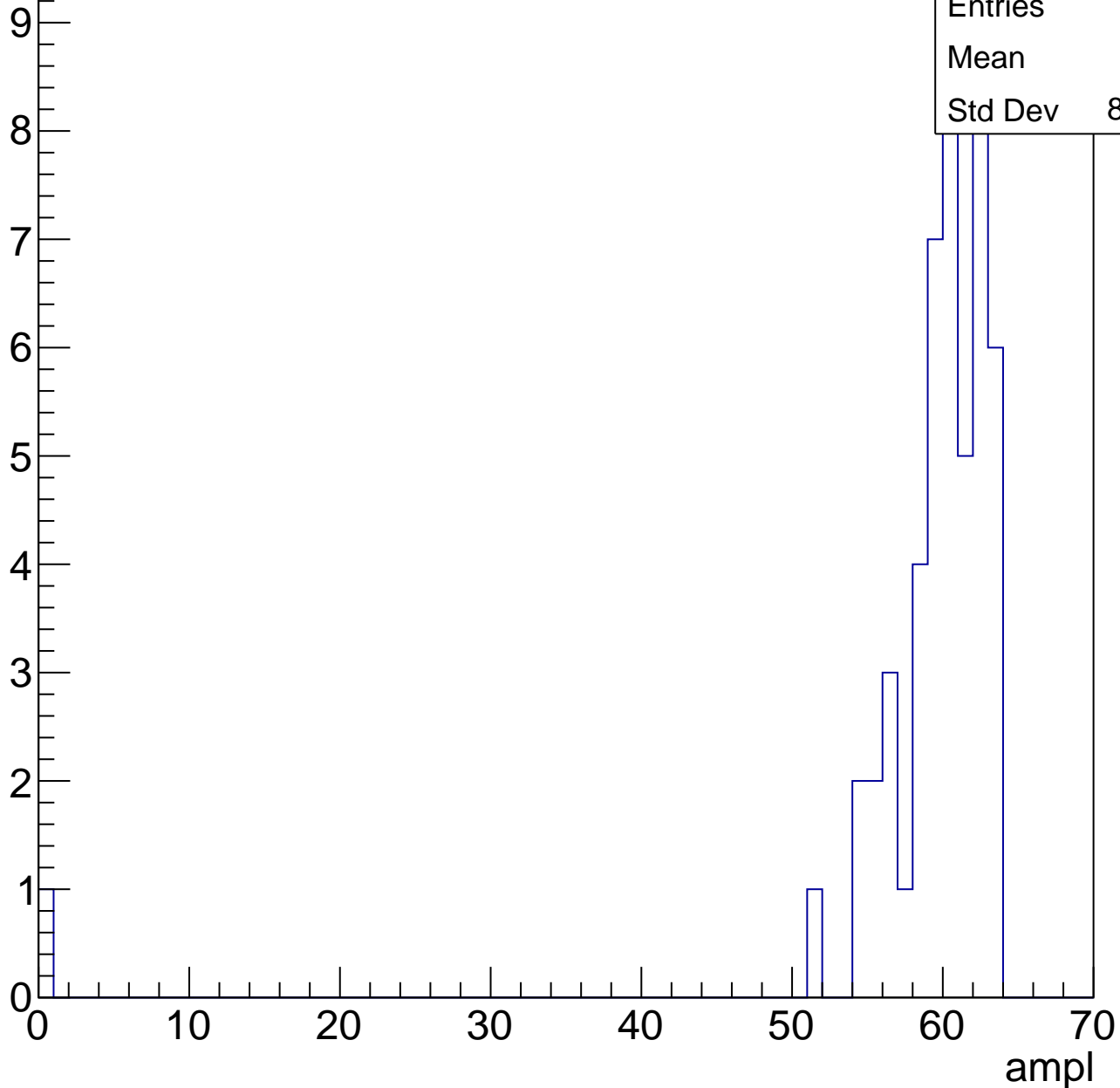
Entries	62
Mean	54.69
Std Dev	3.109



# B1L102S, U20-ch60, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

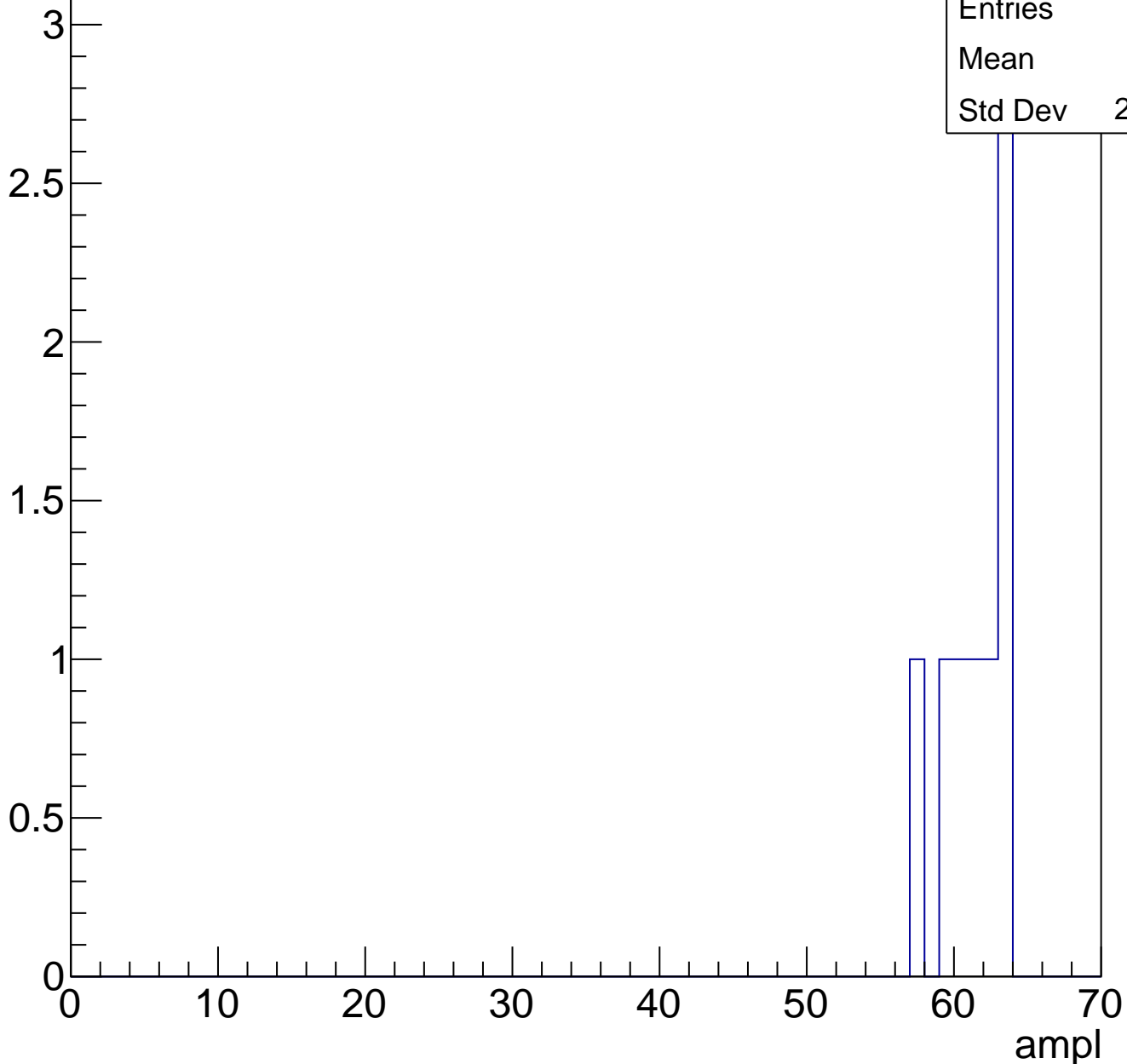
Entry



# B1L102S, U20-ch60, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U20-ch60, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch61, adc0

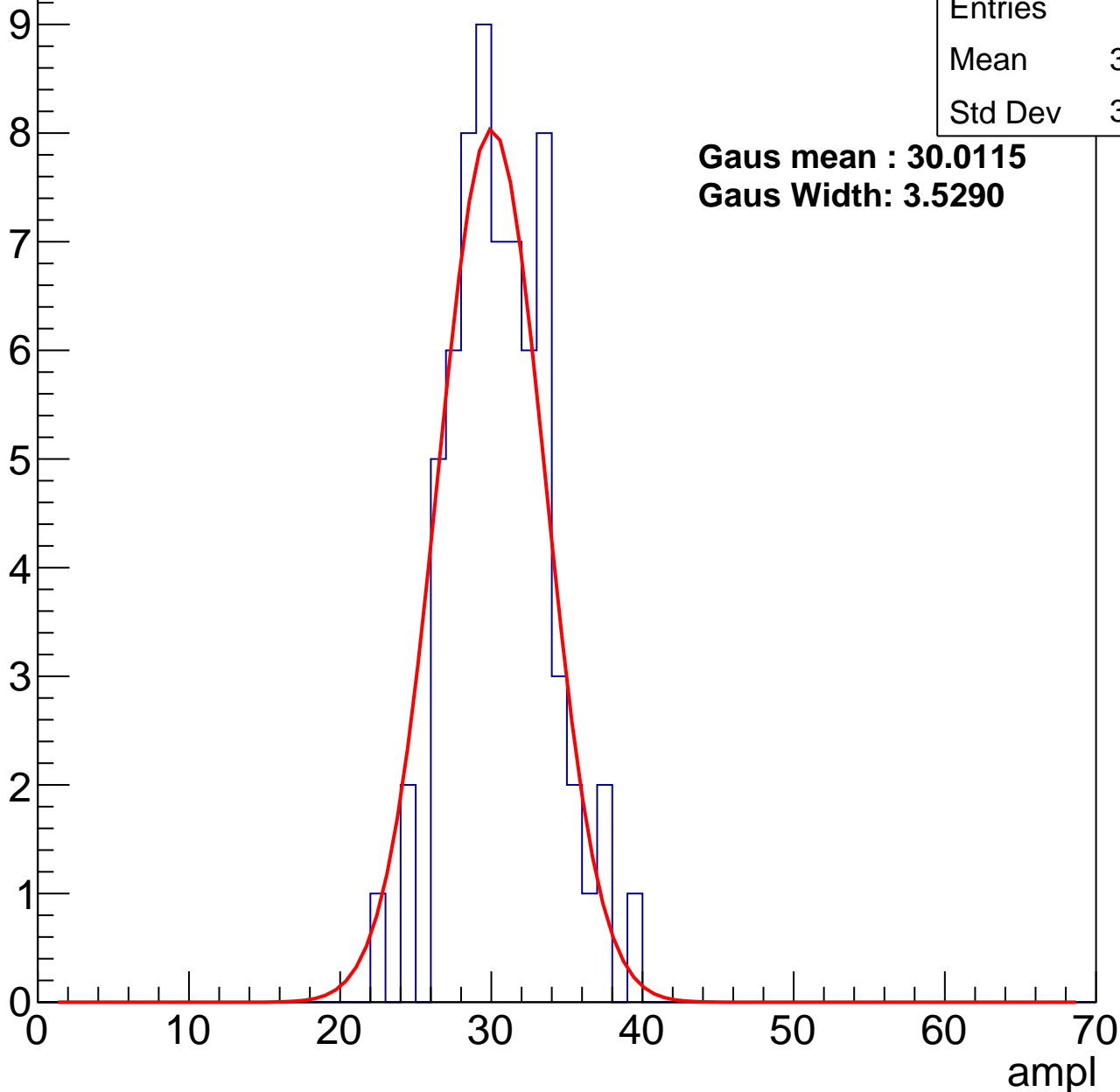
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	30.16
Std Dev	3.266

**Gaus mean : 30.0115**

**Gaus Width: 3.5290**



# B1L102S, U20-ch61, adc1

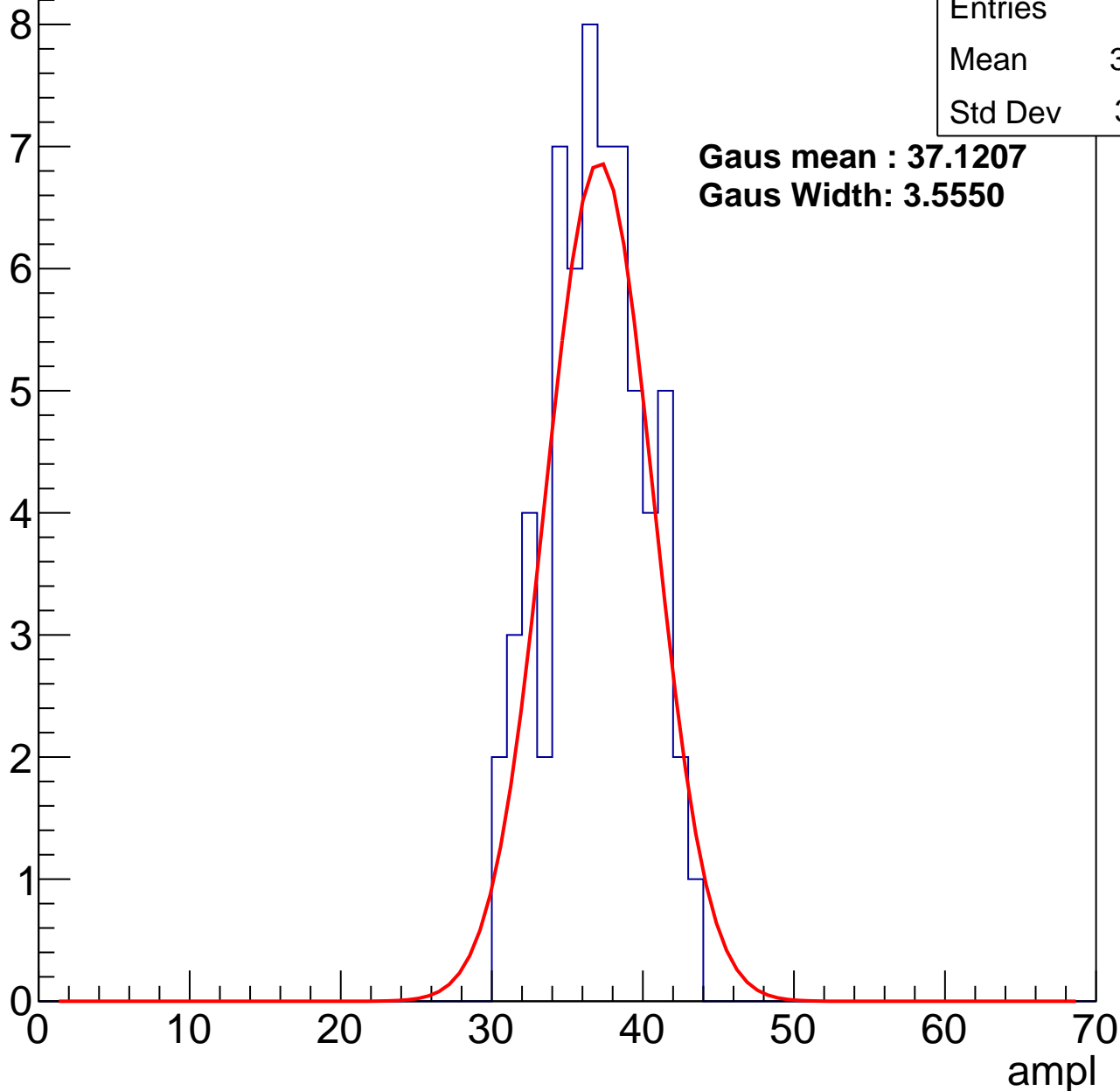
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	36.43
Std Dev	3.191

**Gaus mean : 37.1207**

**Gaus Width: 3.5550**

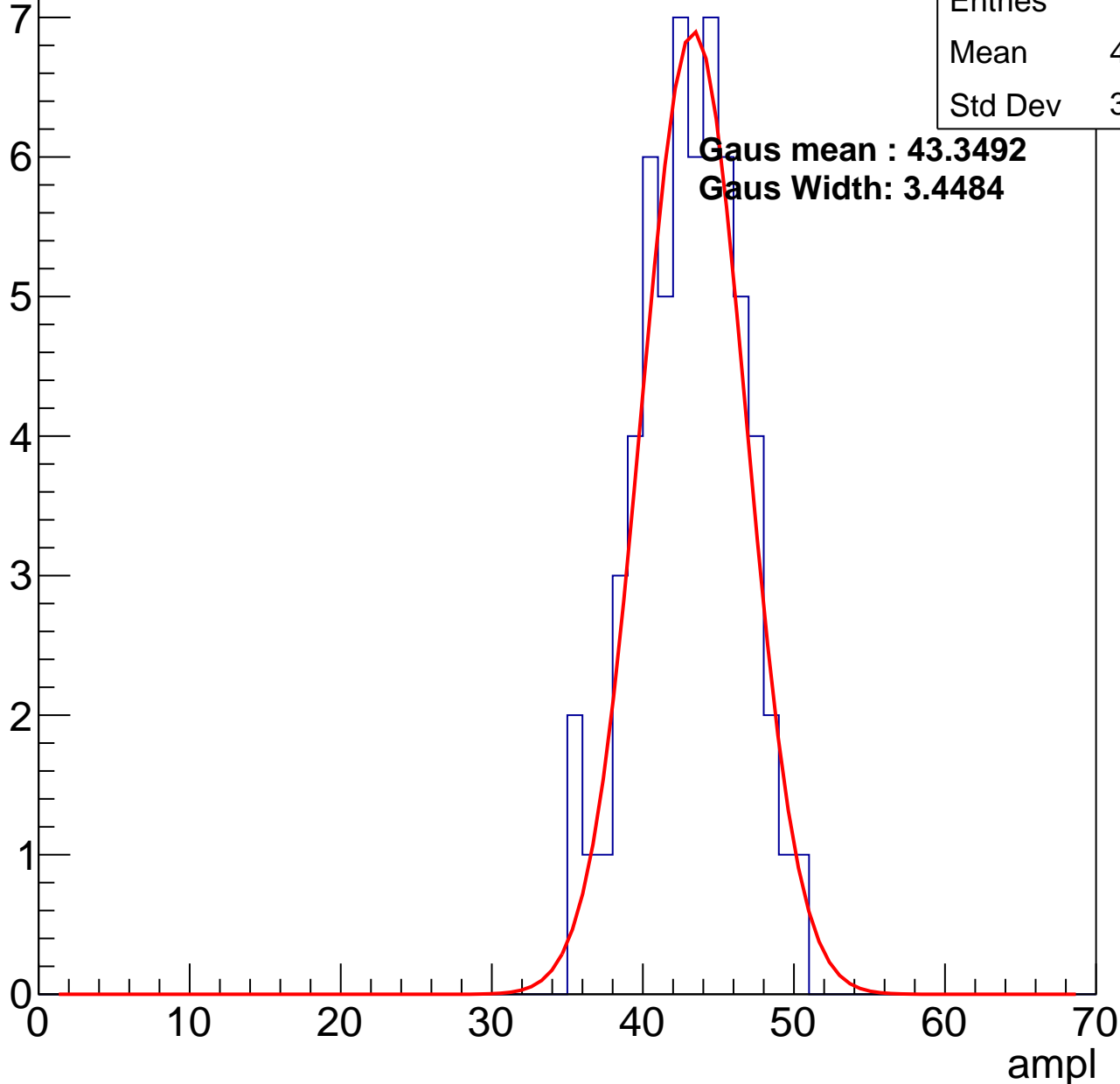


# B1L102S, U20-ch61, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

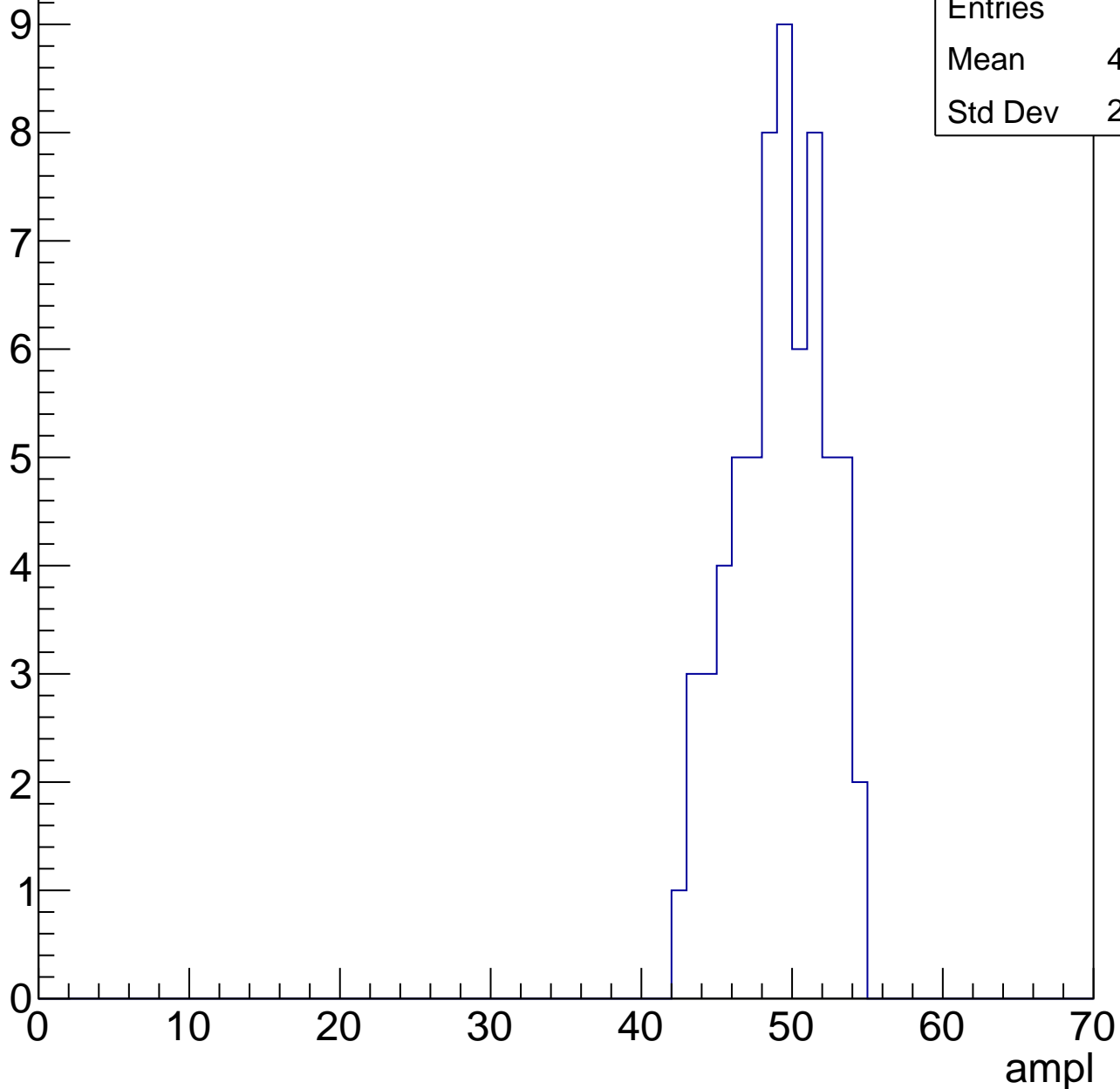
Entries	61
Mean	42.64
Std Dev	3.388



# B1L102S, U20-ch61, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

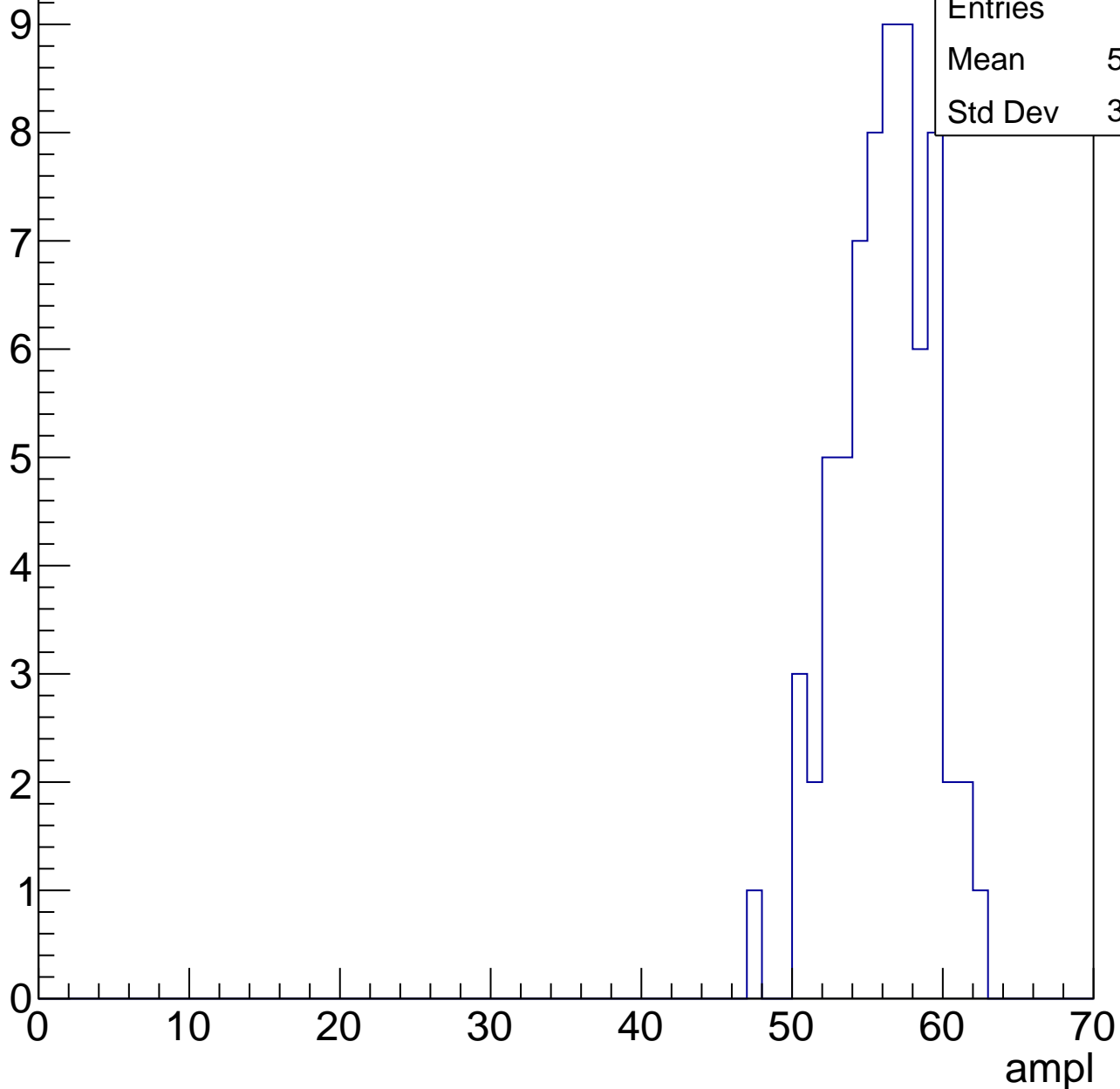


Entries	64
Mean	48.66
Std Dev	2.996

# B1L102S, U20-ch61, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch61, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	43
Mean	58.95
Std Dev	9.393

ampl

0 10 20 30 40 50 60 70

0

1

2

3

4

5

6

7

8

# B1L102S, U20-ch61, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U20-ch61, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U20-ch62, adc0

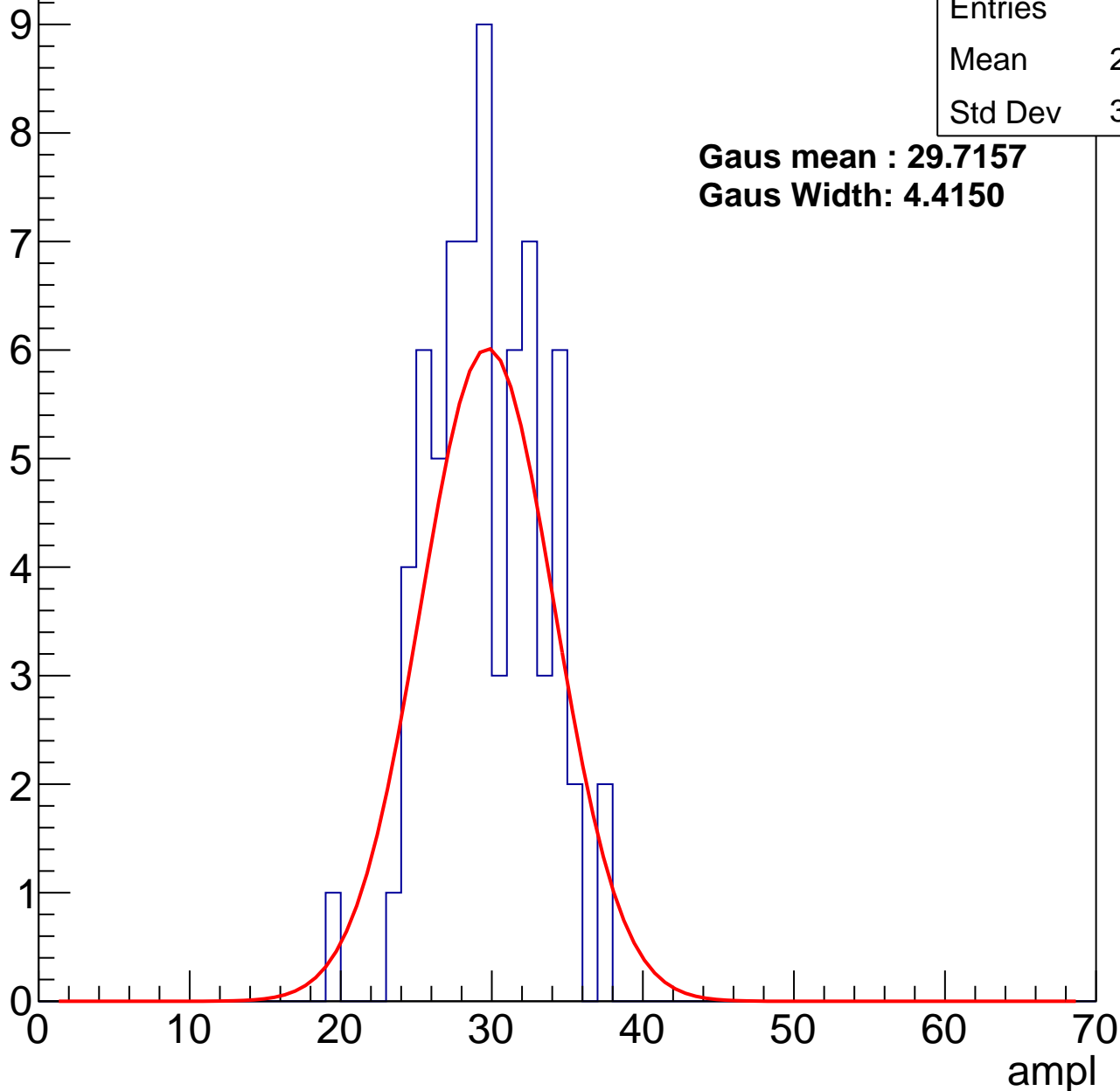
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	29.14
Std Dev	3.609

**Gaus mean : 29.7157**

**Gaus Width: 4.4150**



# B1L102S, U20-ch62, adc1

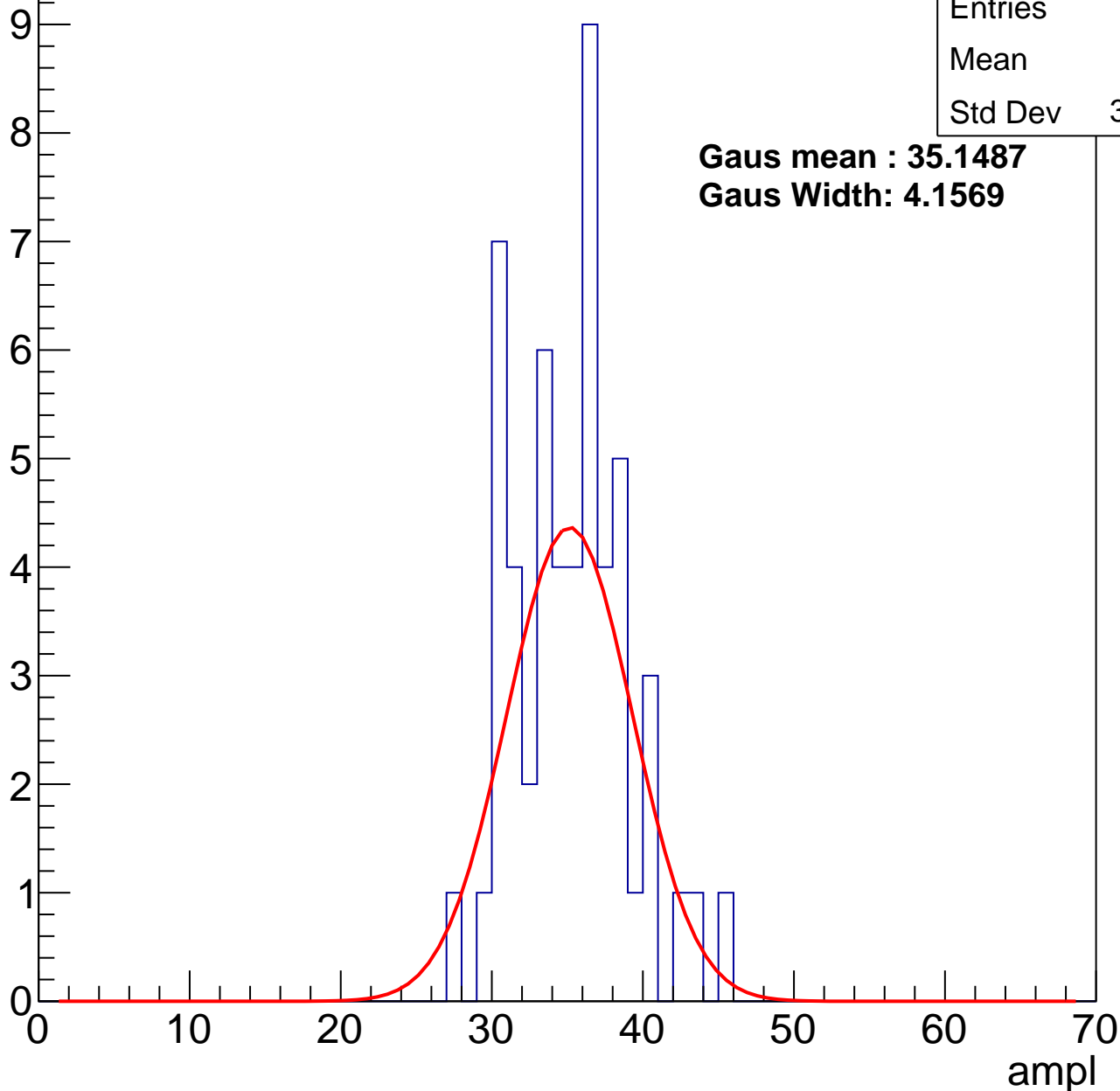
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	34.8
Std Dev	3.744

**Gaus mean : 35.1487**

**Gaus Width: 4.1569**



# B1L102S, U20-ch62, adc2

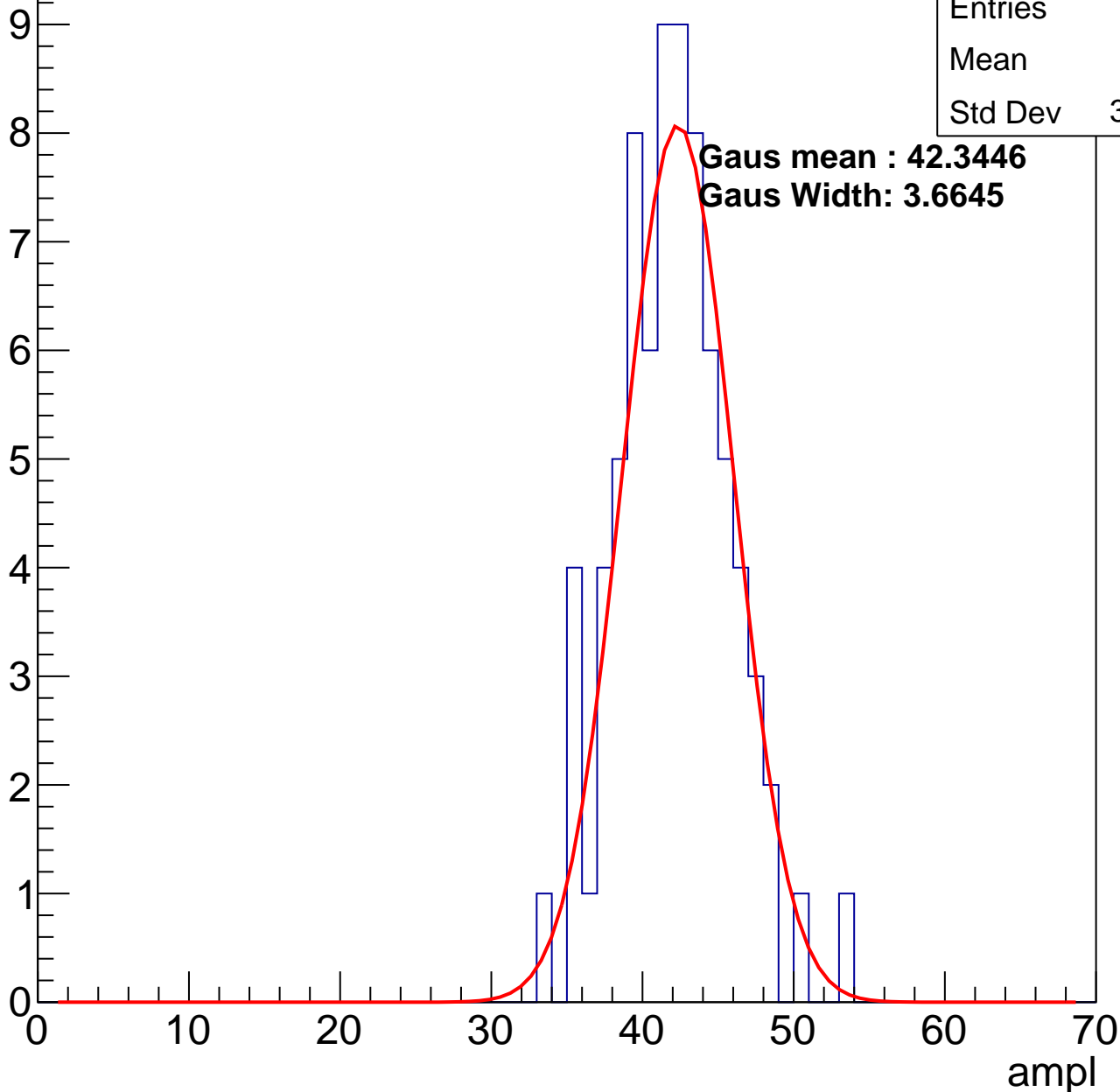
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	41.6
Std Dev	3.708

**Gaus mean : 42.3446**

**Gaus Width: 3.6645**

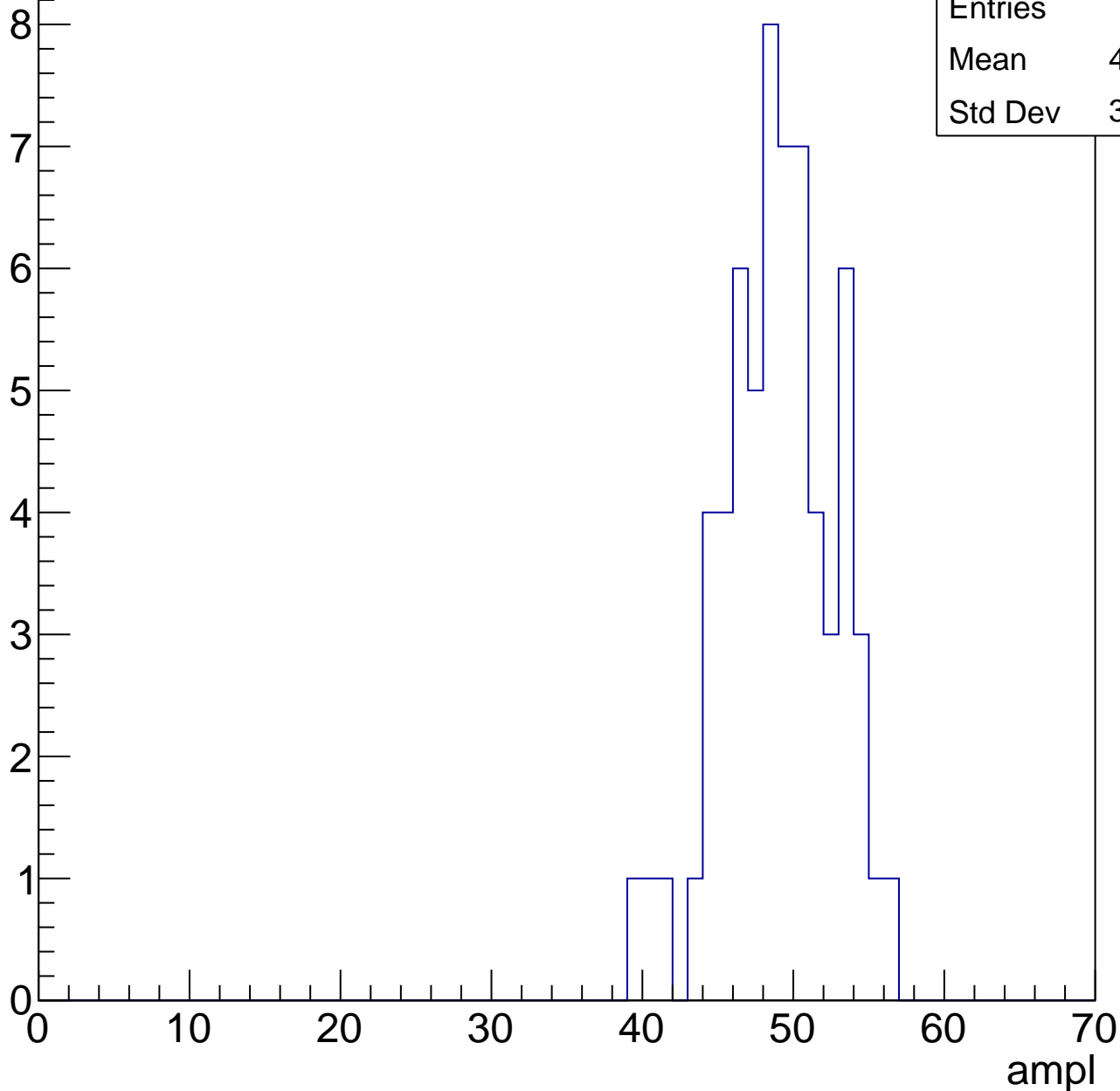


# B1L102S, U20-ch62, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

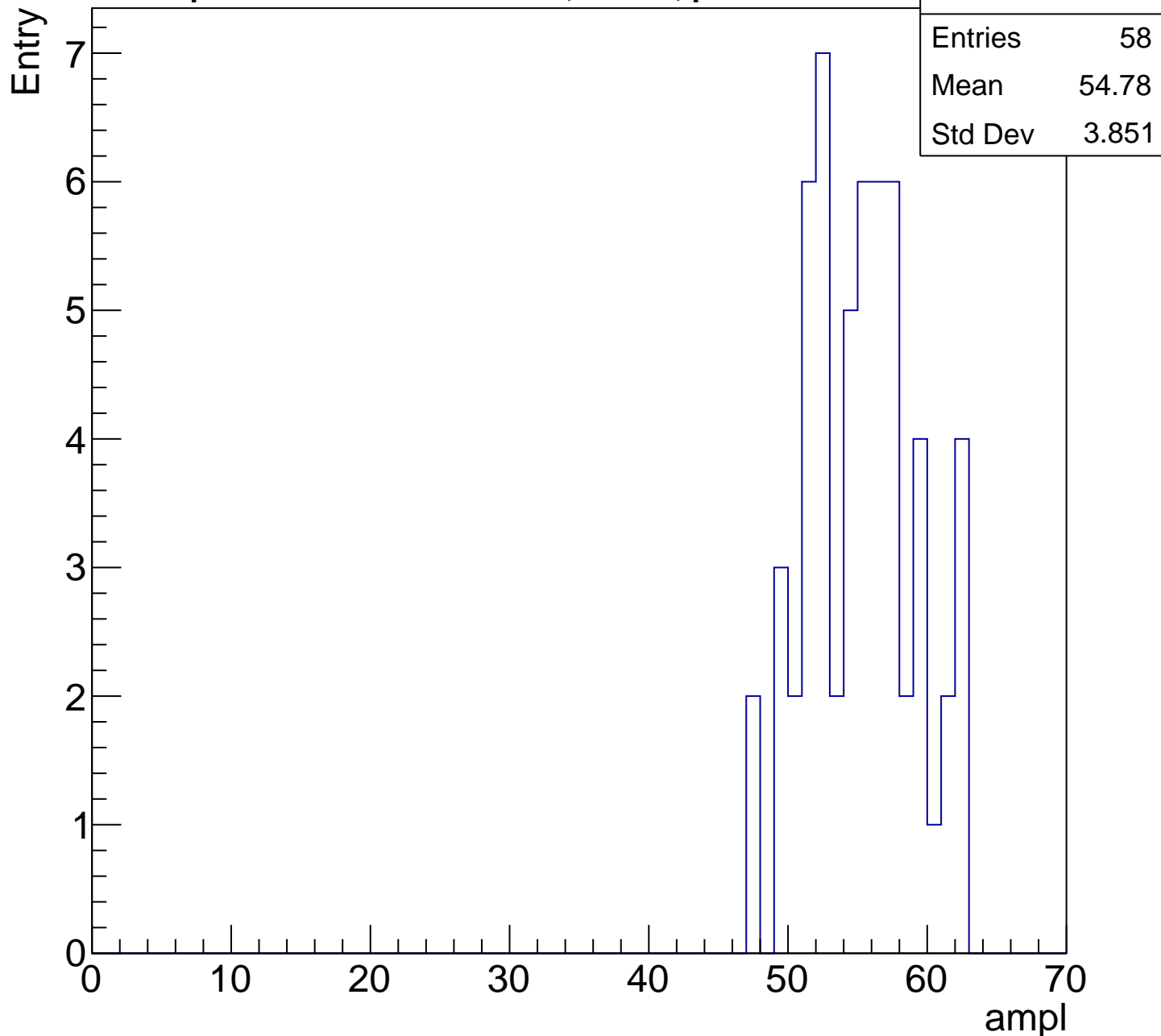
Entry

Entries	63
Mean	48.54
Std Dev	3.607



# B1L102S, U20-ch62, adc4

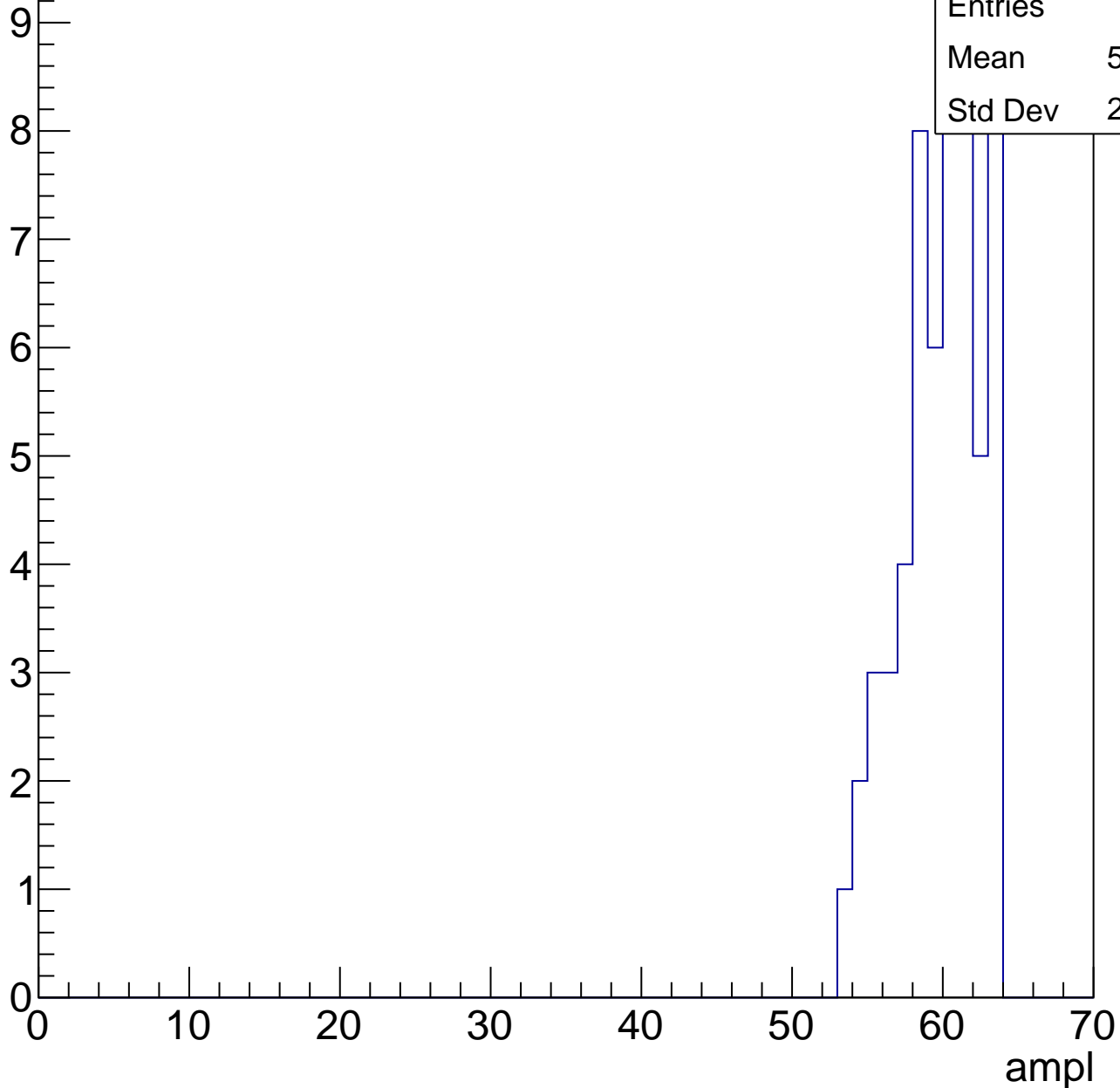
calib\_packv5\_042523\_0143.root, FC#11, port A2



# B1L102S, U20-ch62, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	57
Mean	59.33
Std Dev	2.625

# B1L102S, U20-ch62, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

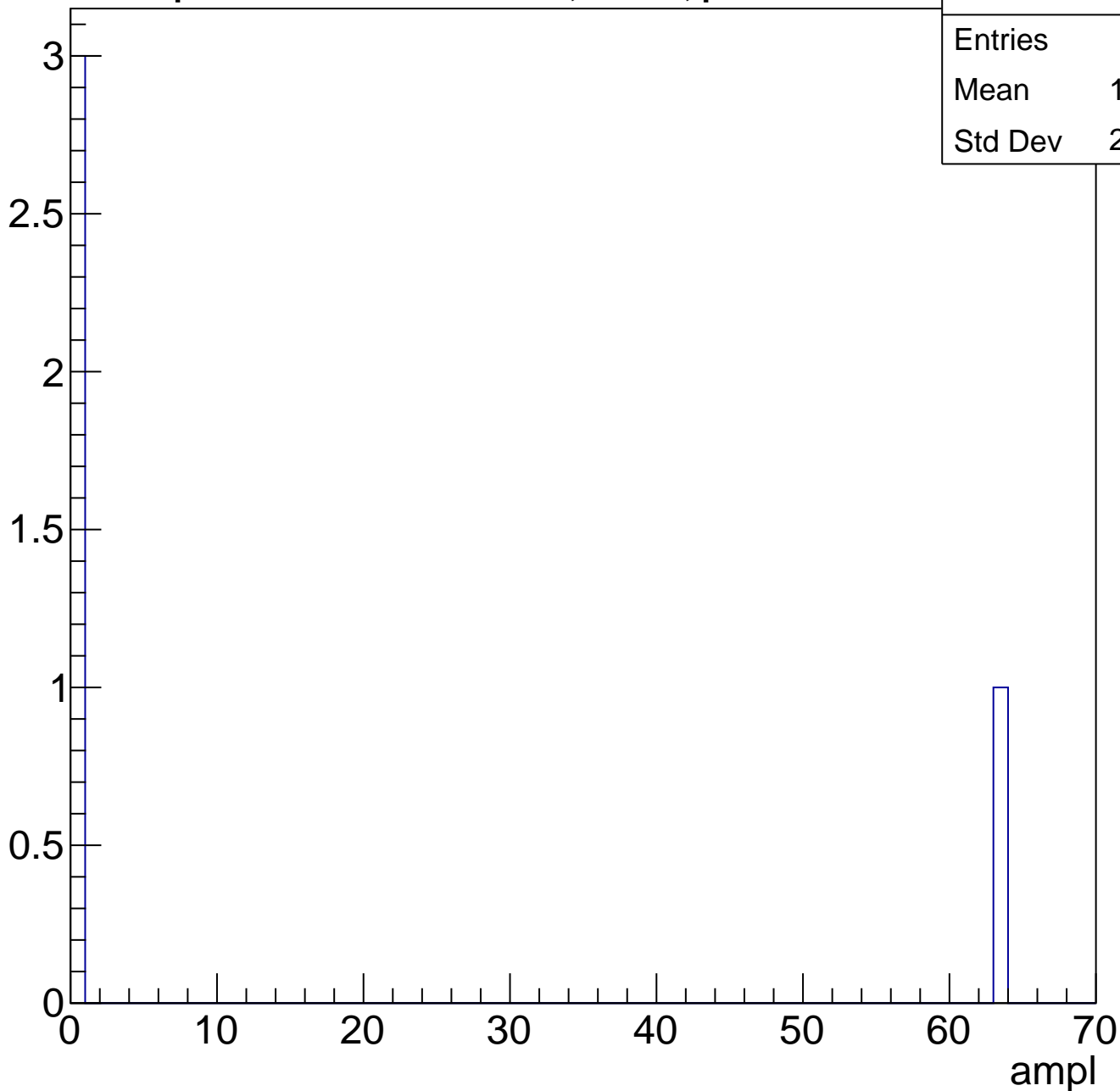




# B1L102S, U20-ch62, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch63, adc0

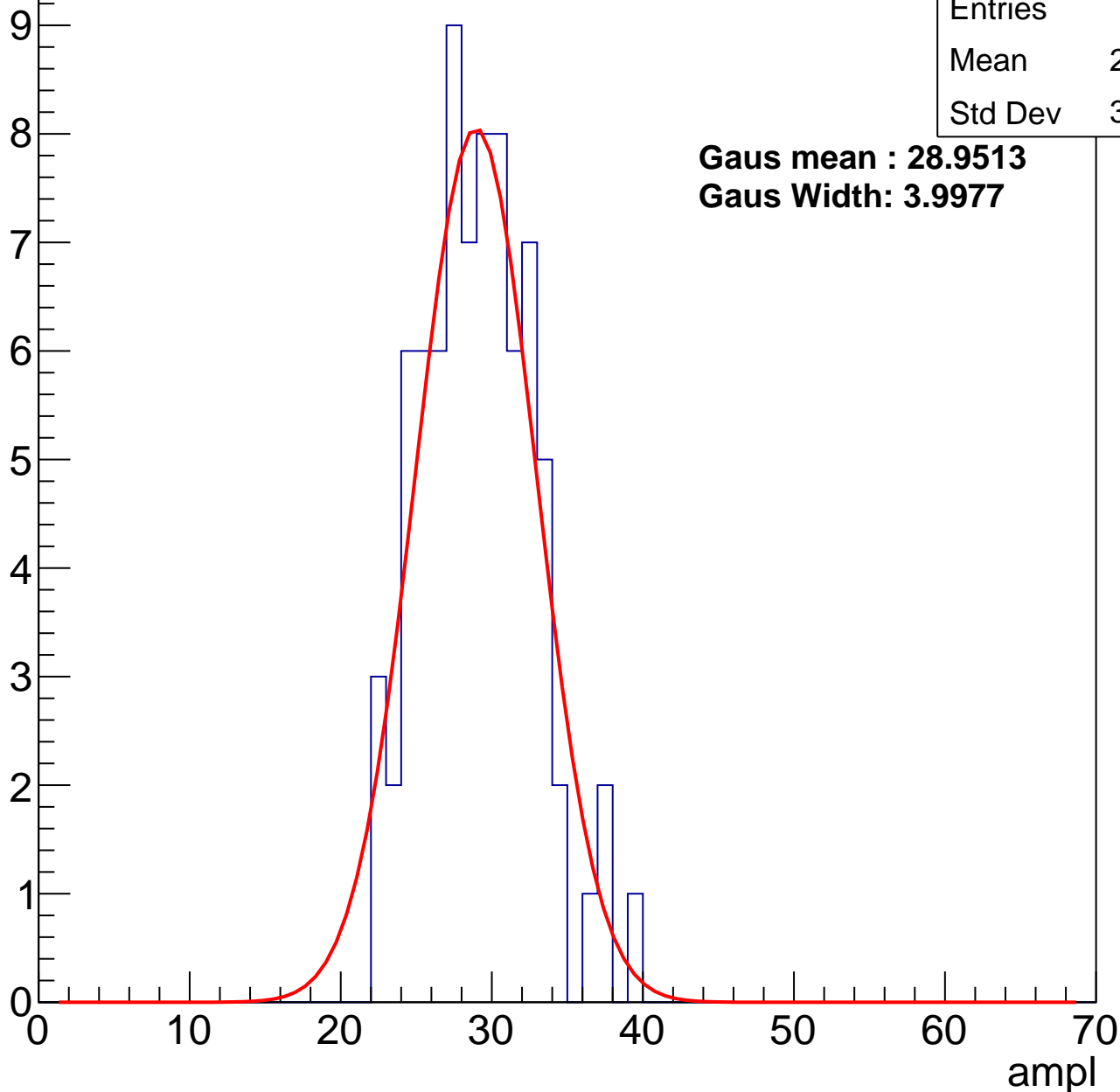
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	79
Mean	28.67
Std Dev	3.655

**Gaus mean : 28.9513**

**Gaus Width: 3.9977**



# B1L102S, U20-ch63, adc1

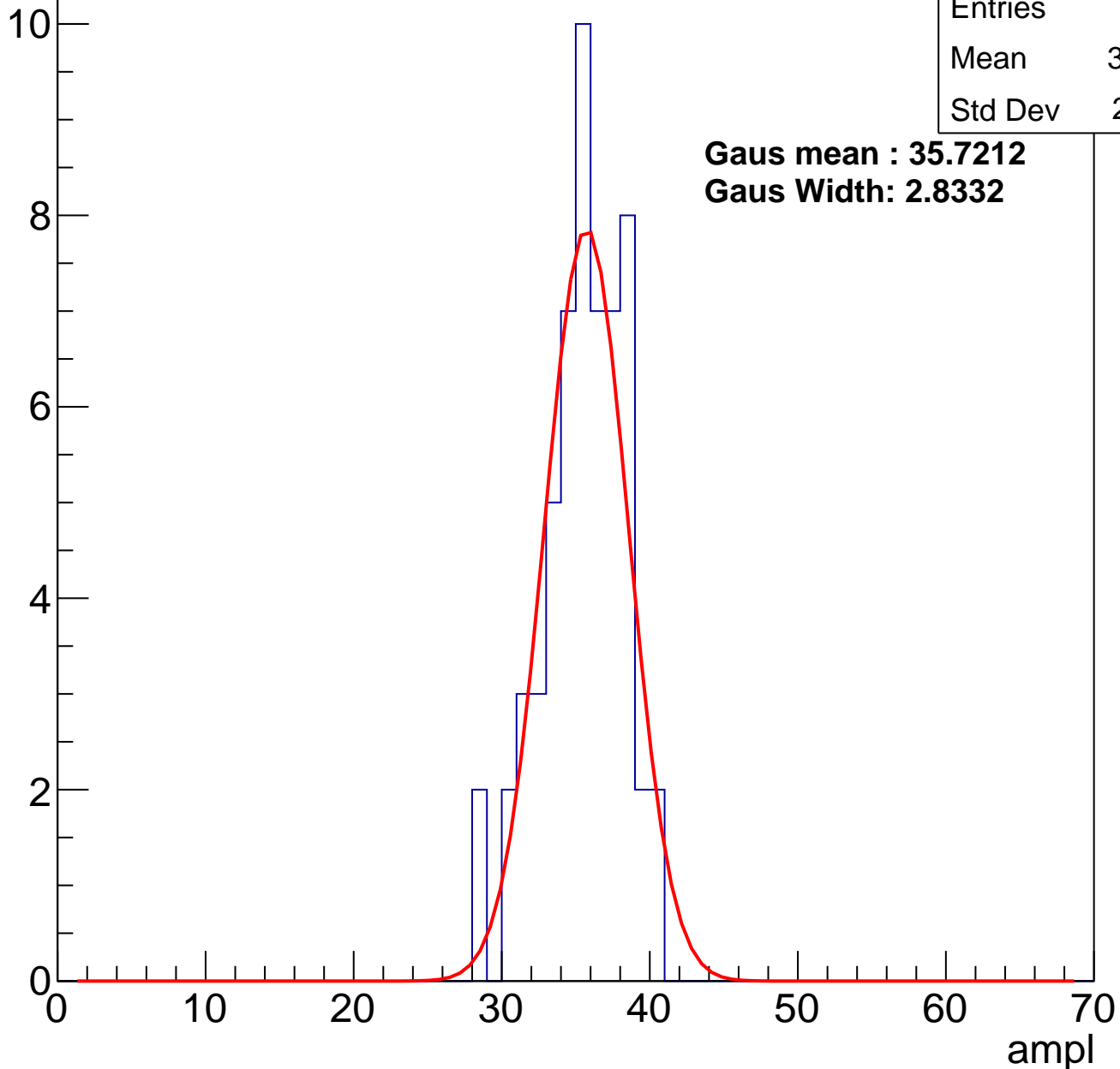
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	58
Mean	35.02
Std Dev	2.751

**Gaus mean : 35.7212**

**Gaus Width: 2.8332**

Entry



# B1L102S, U20-ch63, adc2

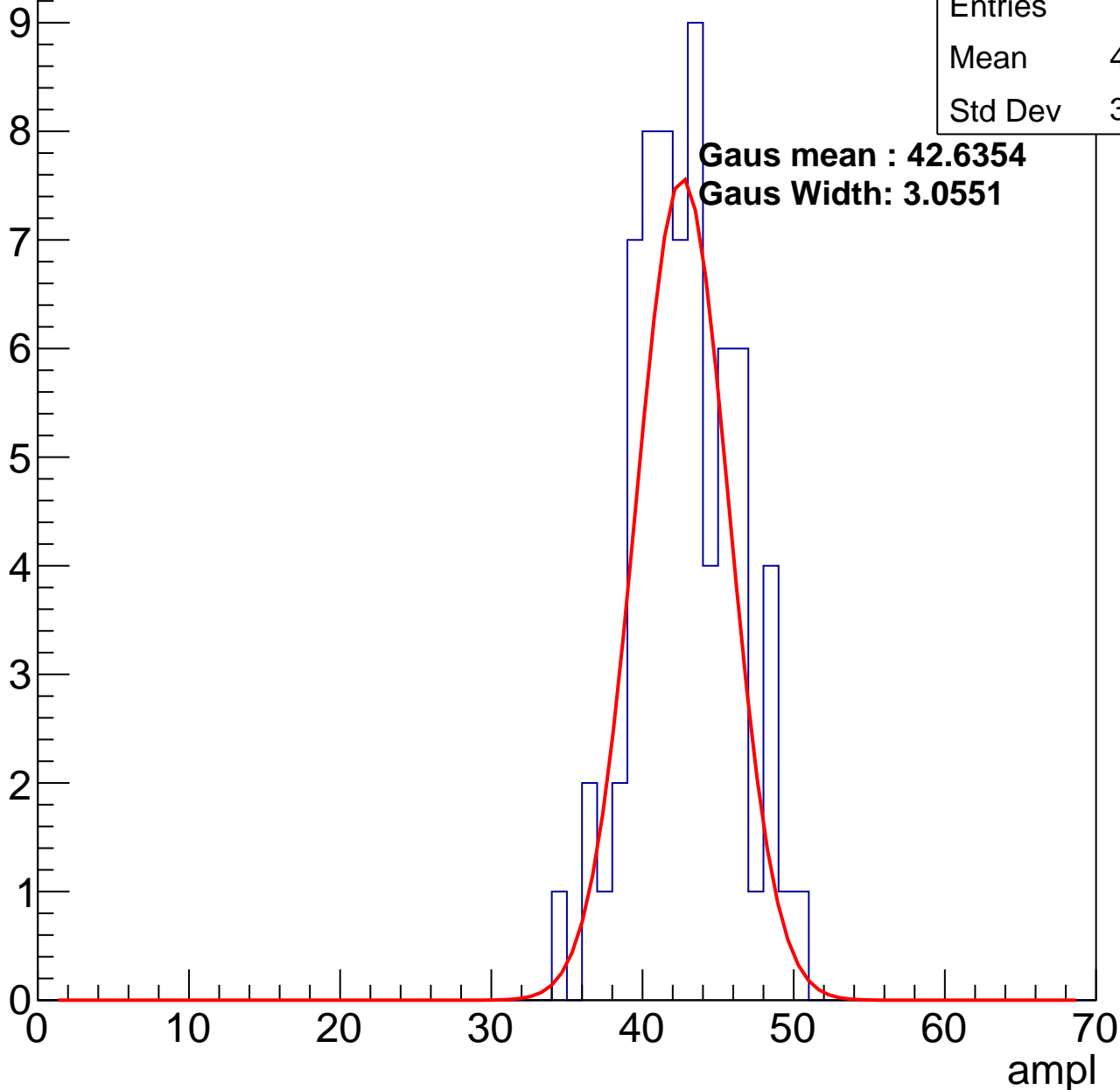
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	42.37
Std Dev	3.307

**Gaus mean : 42.6354**

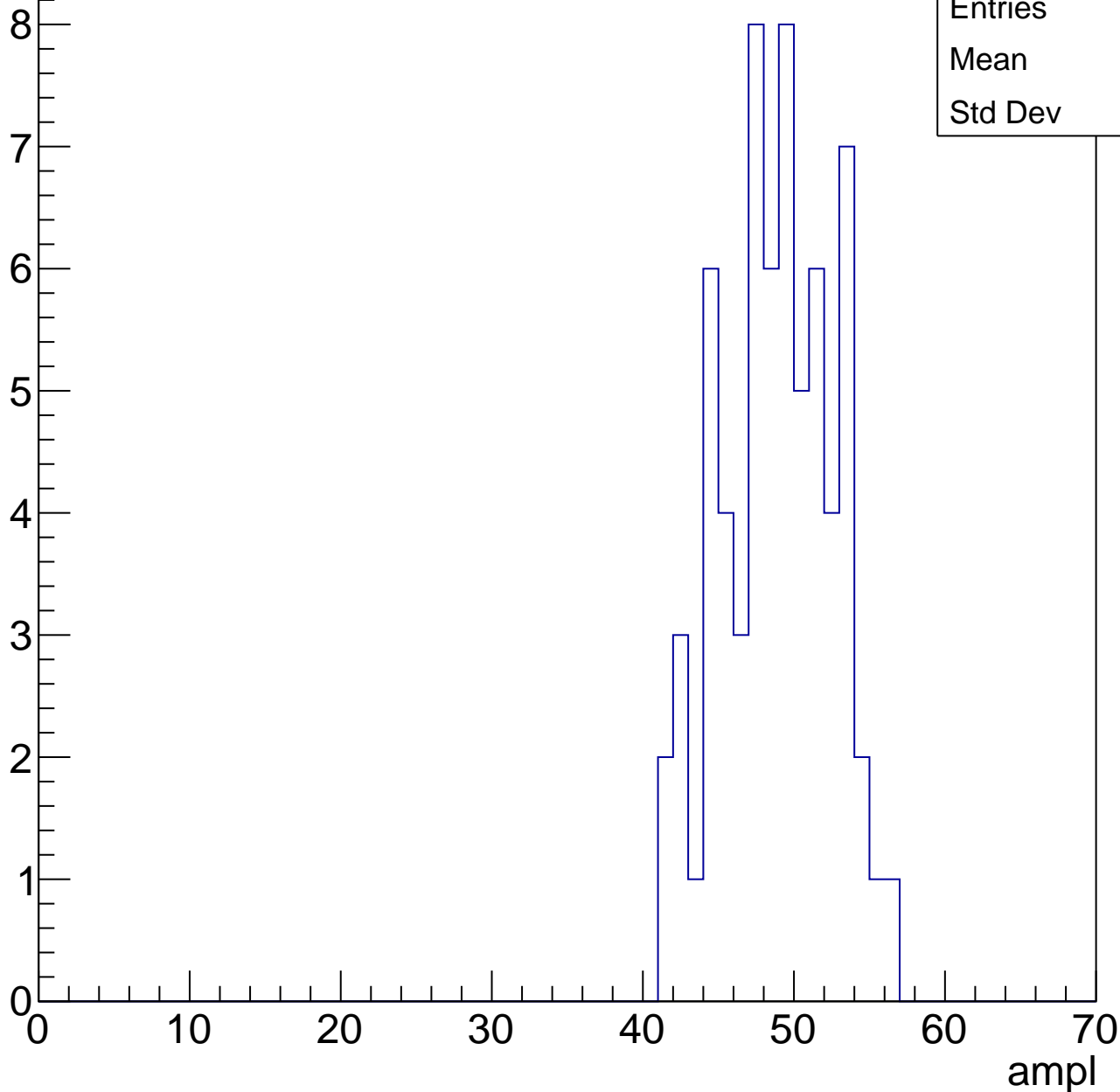
**Gaus Width: 3.0551**



# B1L102S, U20-ch63, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



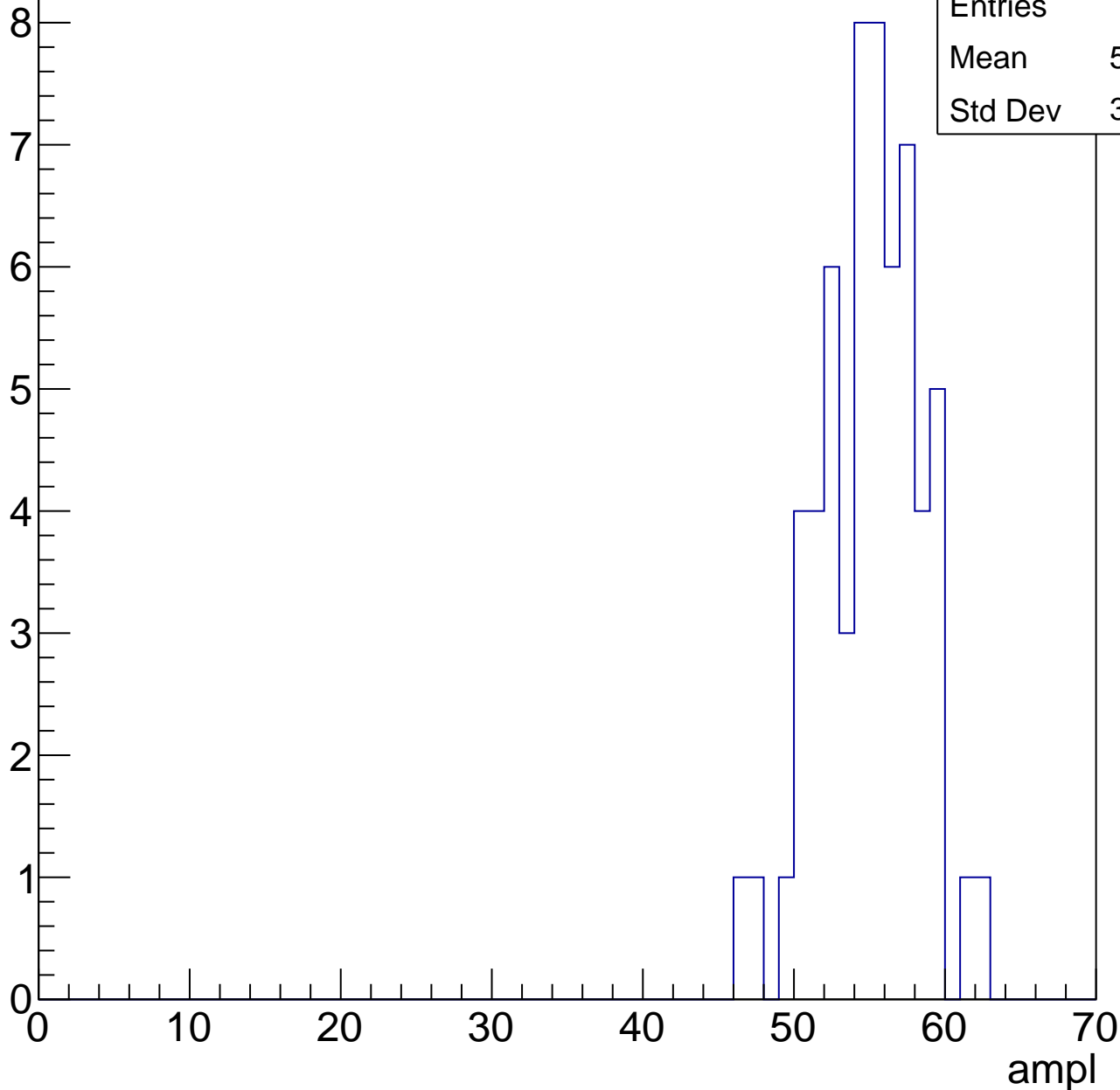
Entries	67
Mean	48.4
Std Dev	3.62

# B1L102S, U20-ch63, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

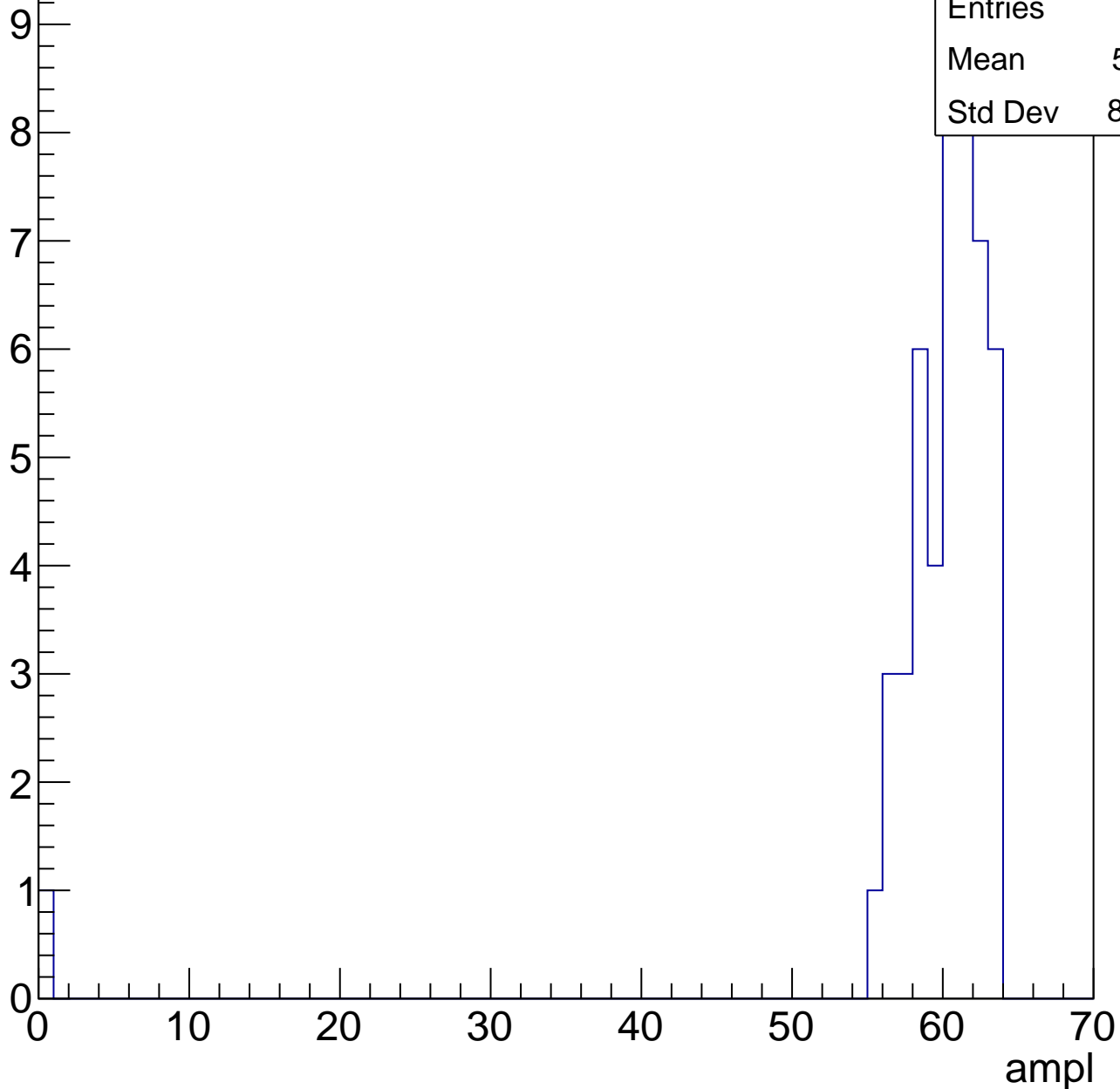
Entries	60
Mean	54.57
Std Dev	3.273



# B1L102S, U20-ch63, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch63, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries

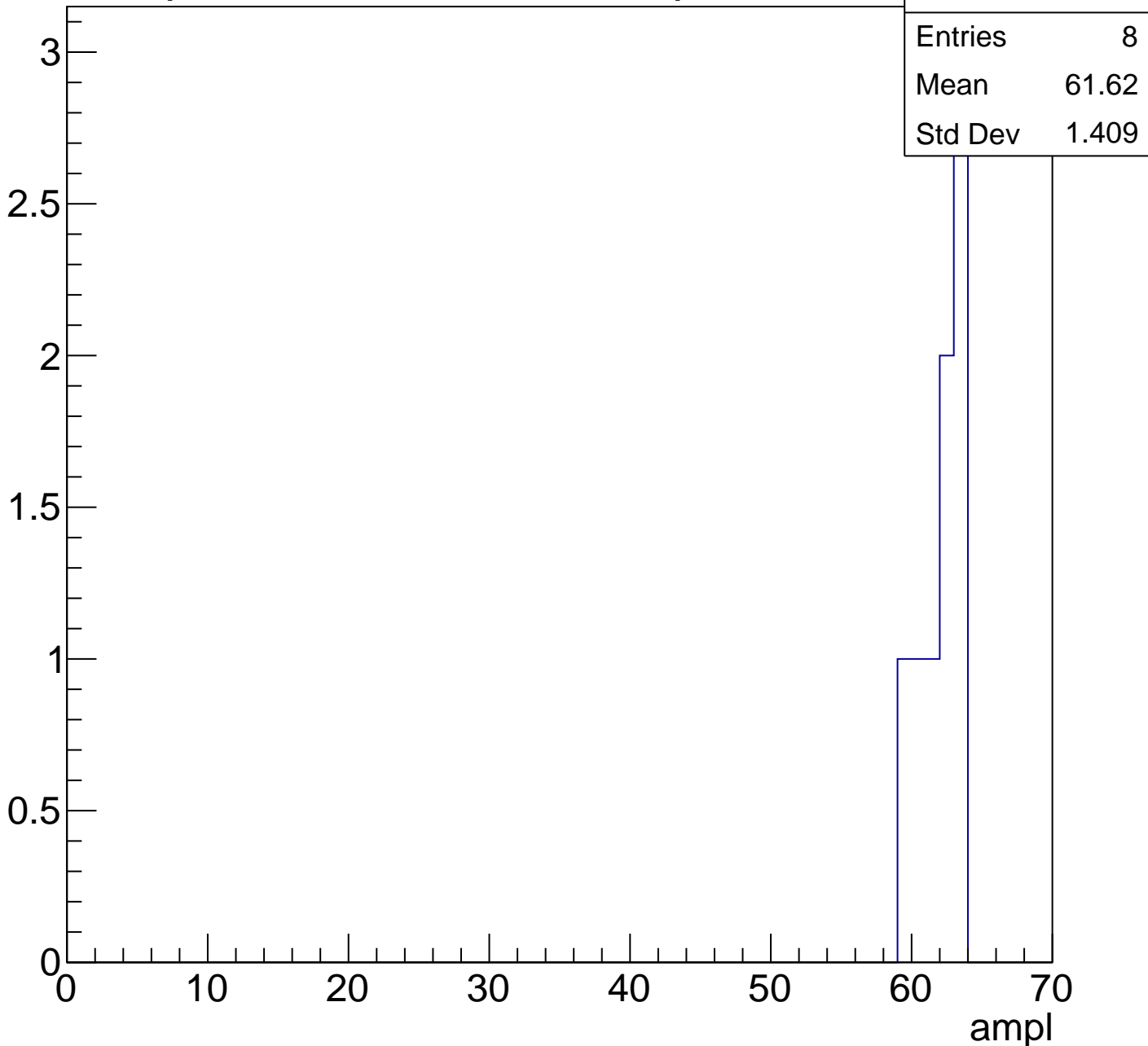
8

Mean

61.62

Std Dev

1.409

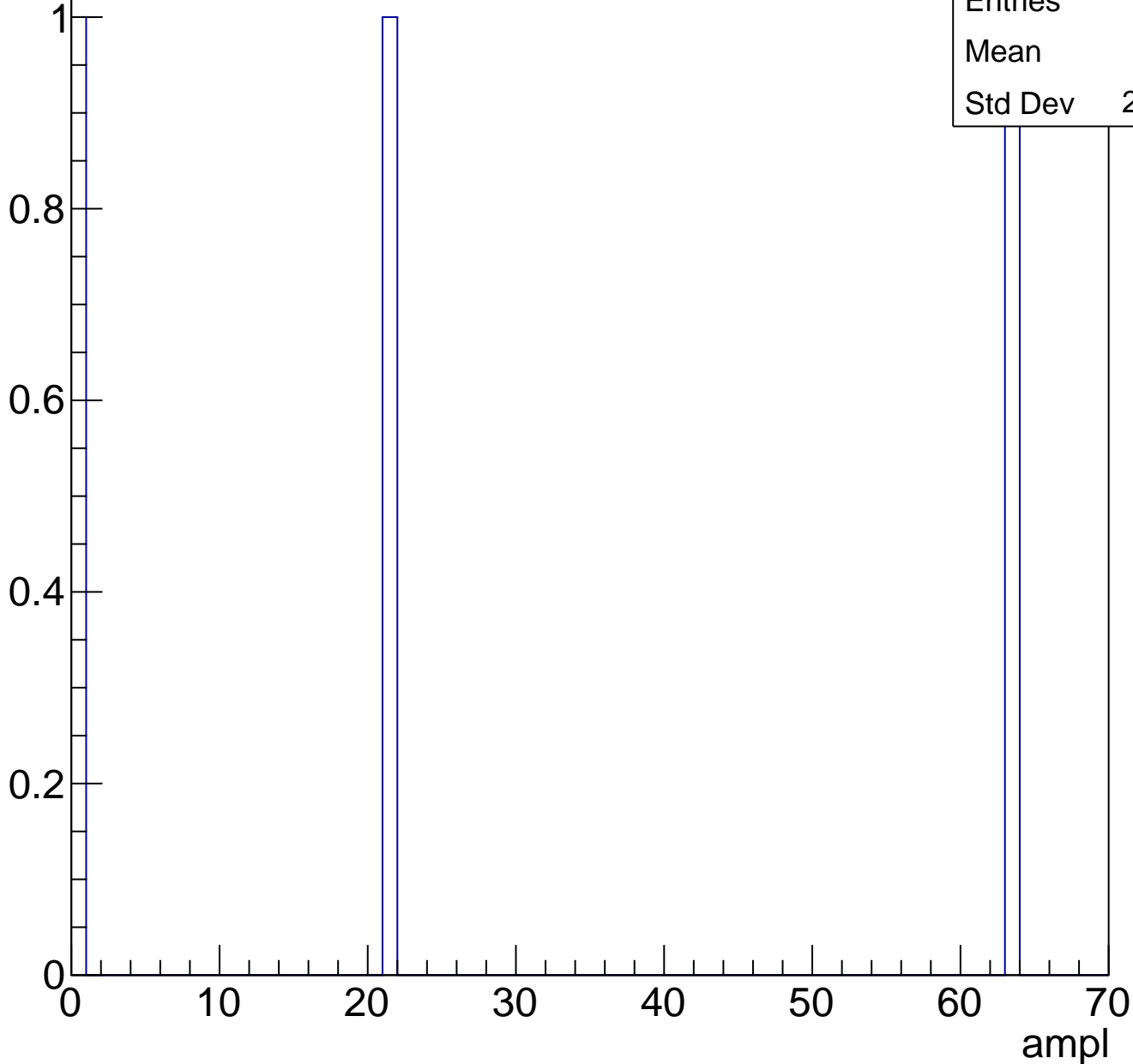




# B1L102S, U20-ch63, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	3
Mean	28
Std Dev	26.19

# B1L102S, U20-ch64, adc0

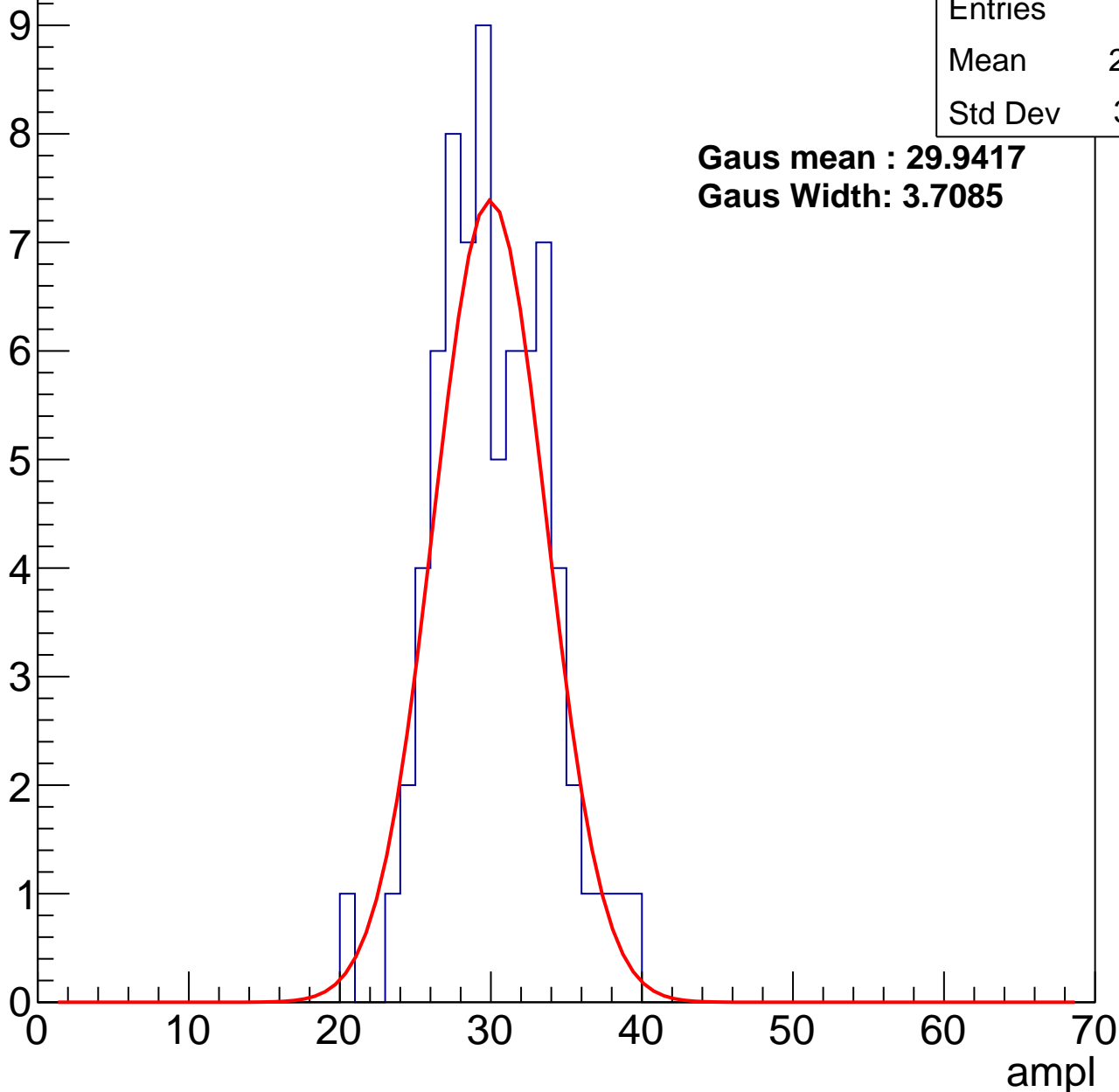
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	29.65
Std Dev	3.641

**Gaus mean : 29.9417**

**Gaus Width: 3.7085**



# B1L102S, U20-ch64, adc1

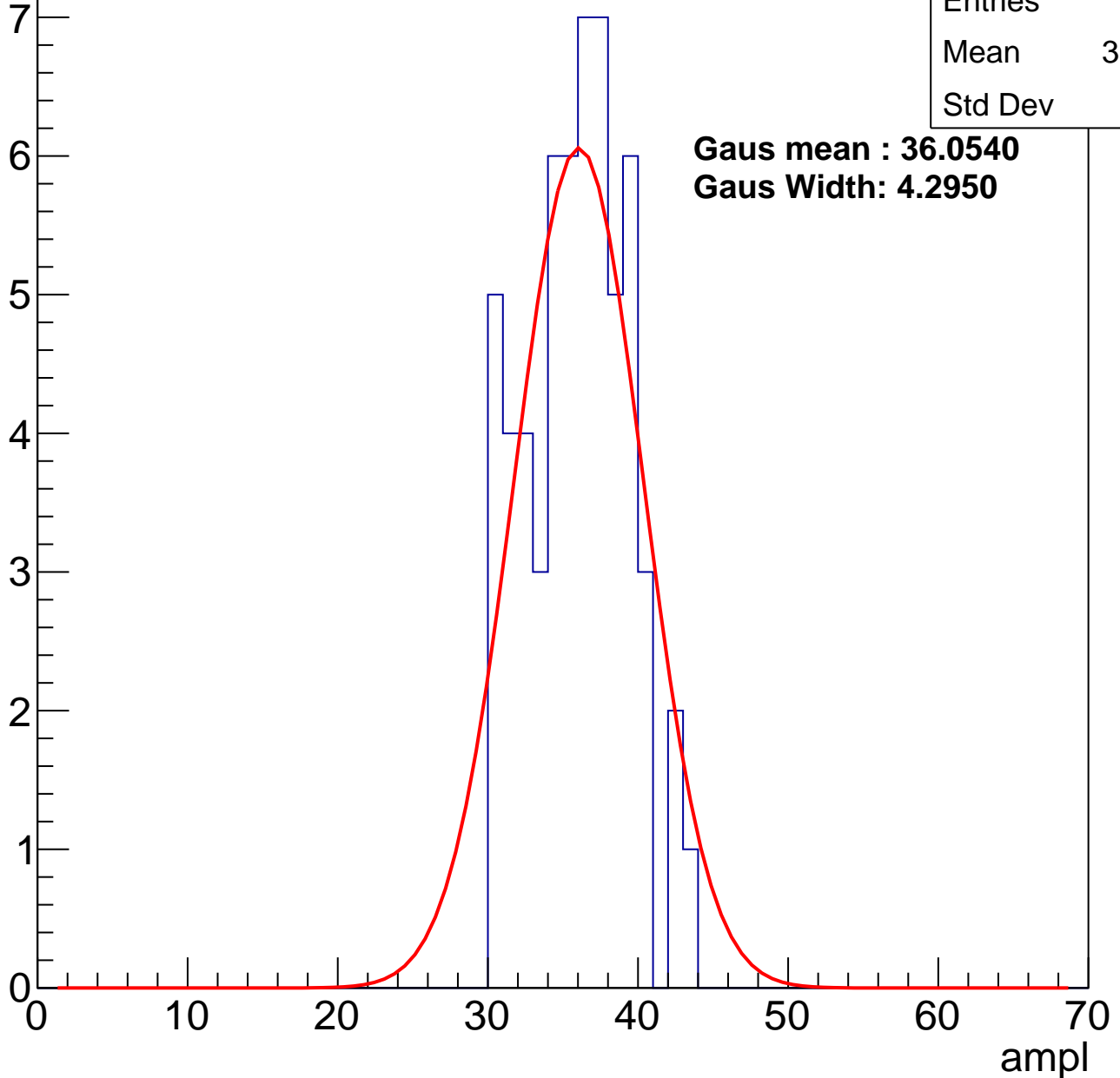
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	35.54
Std Dev	3.29

**Gaus mean : 36.0540**

**Gaus Width: 4.2950**



# B1L102S, U20-ch64, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	73
Mean	42.49
Std Dev	3.397

**Gaus mean : 43.1339**

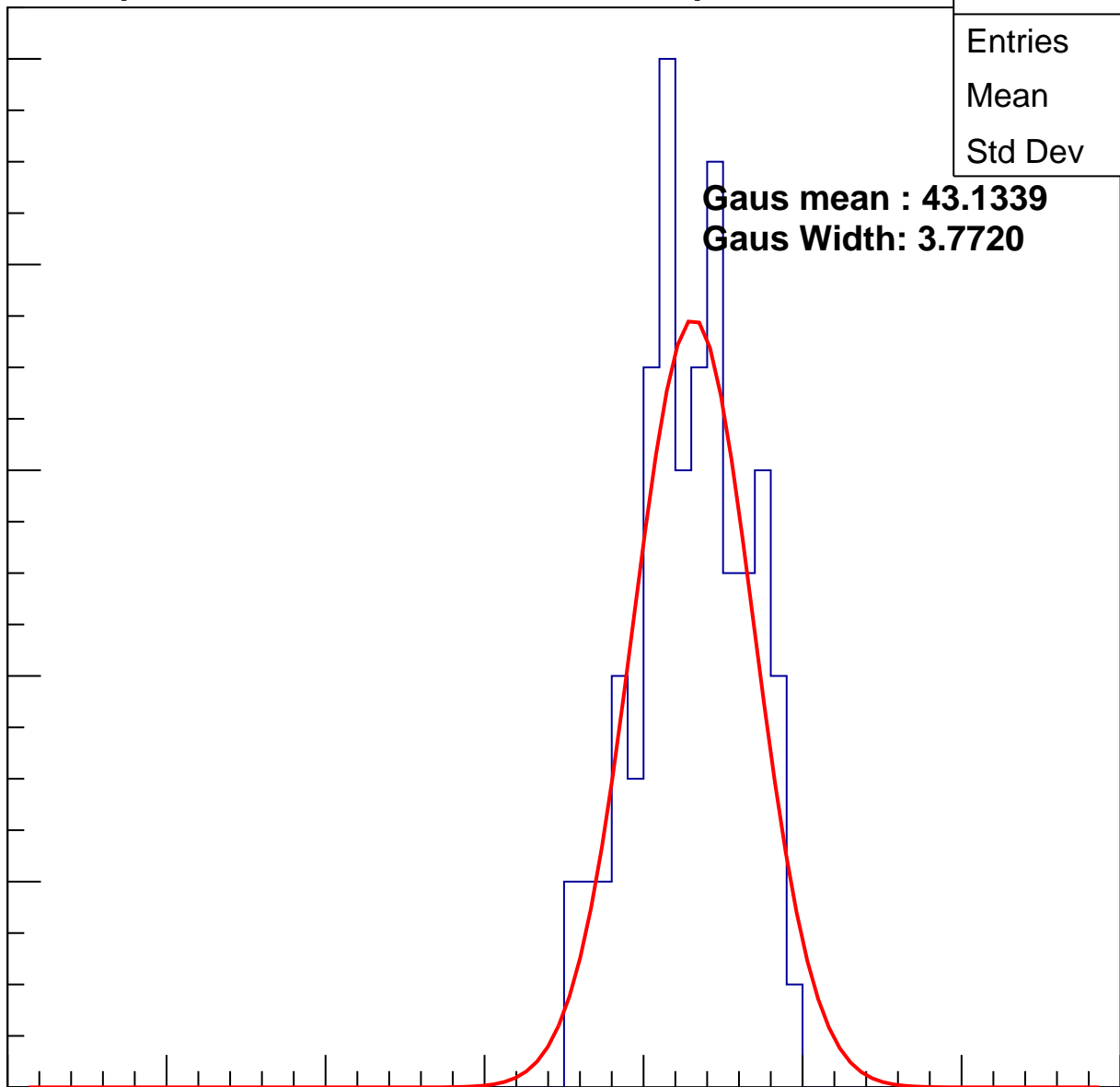
**Gaus Width: 3.7720**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

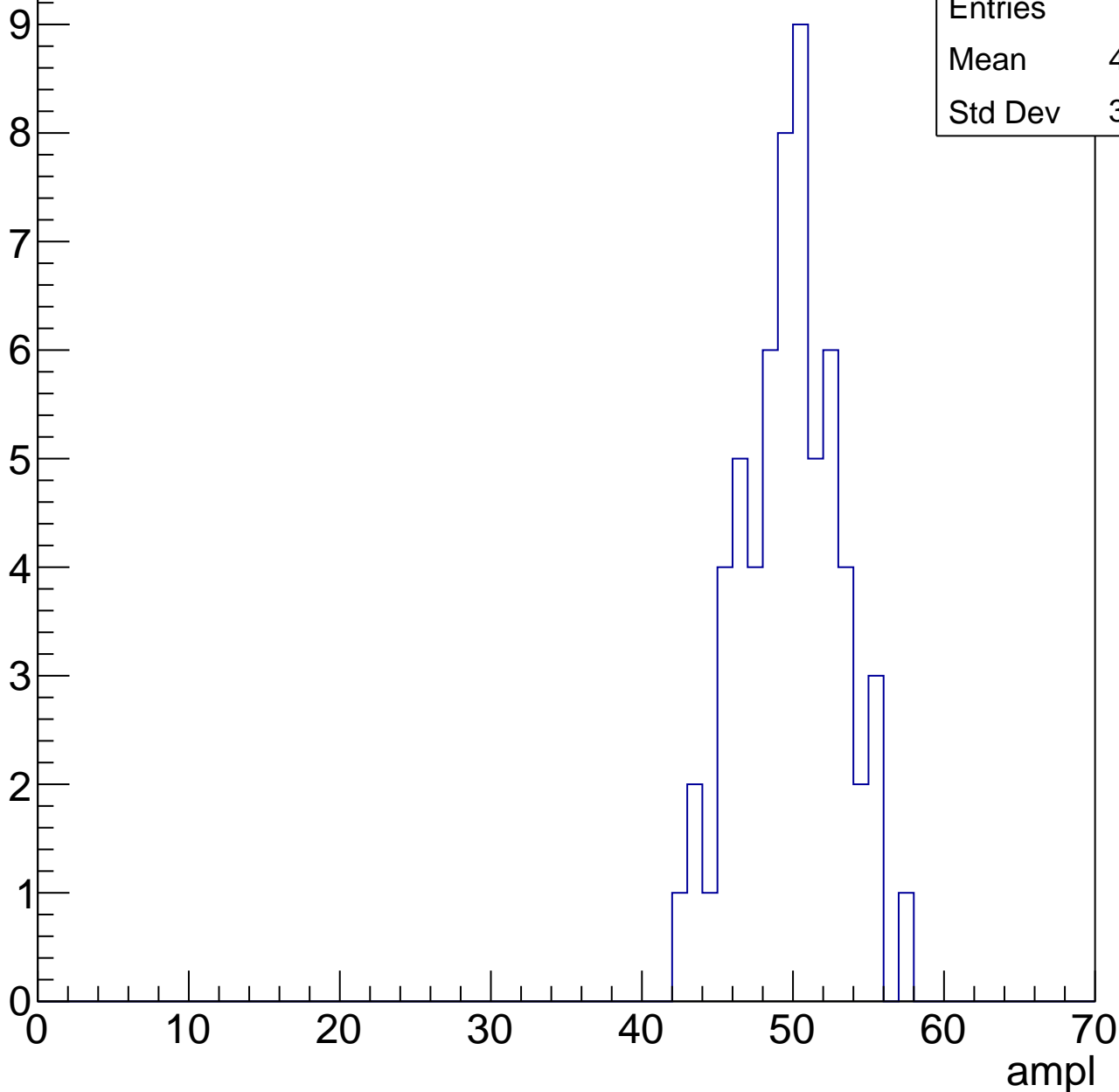


# B1L102S, U20-ch64, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

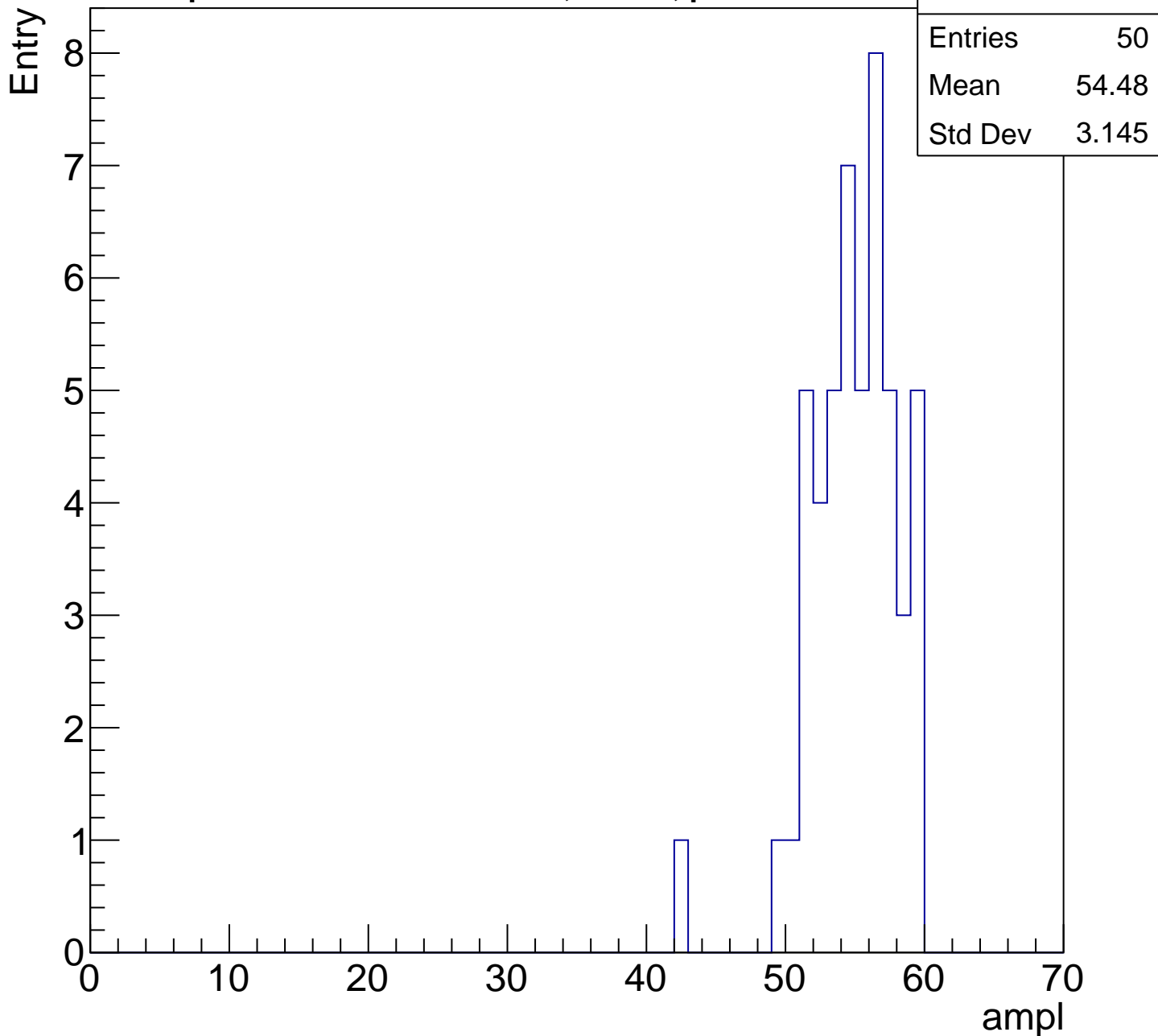
Entry

Entries	61
Mean	49.33
Std Dev	3.238



# B1L102S, U20-ch64, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

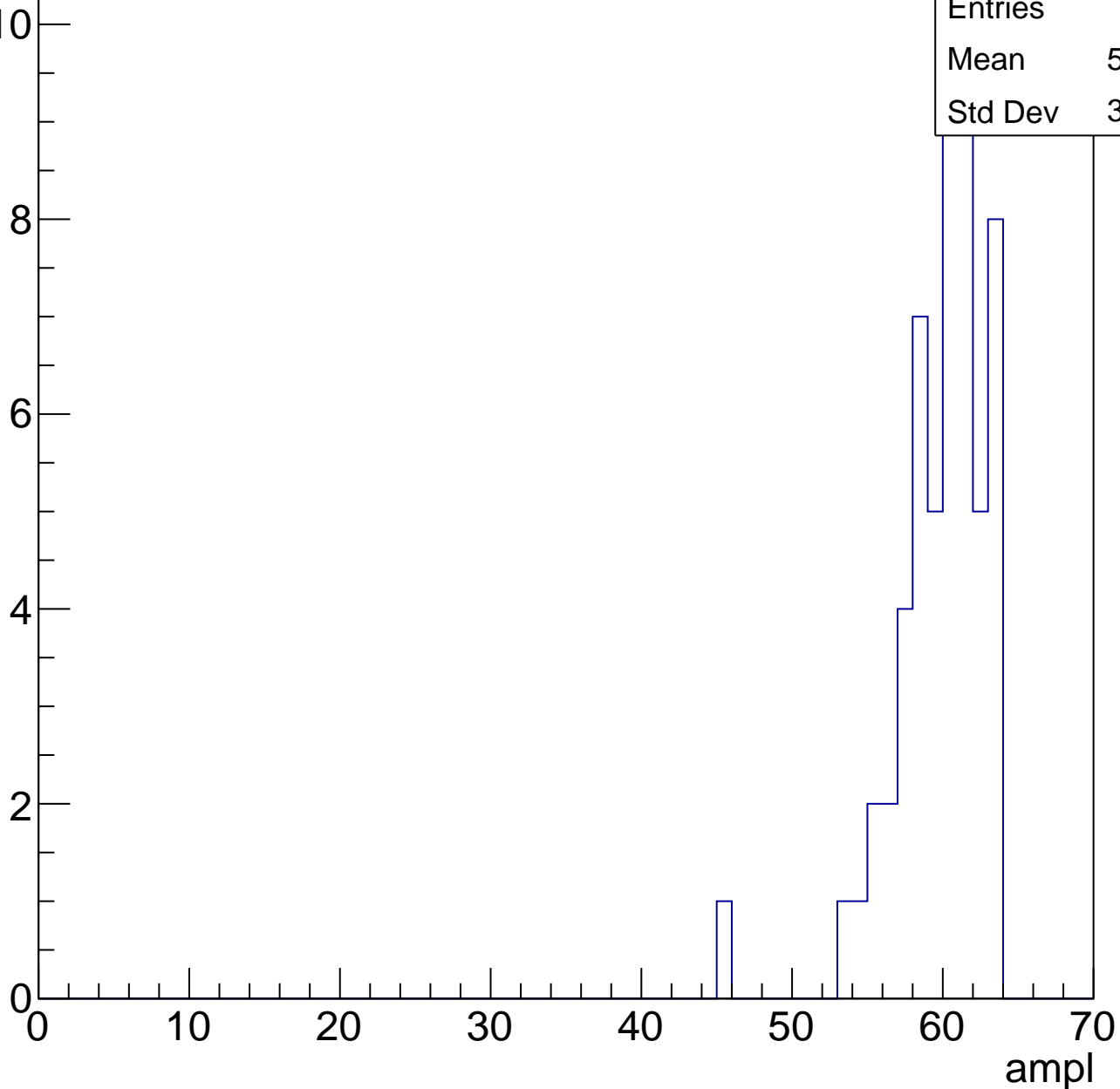


# B1L102S, U20-ch64, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

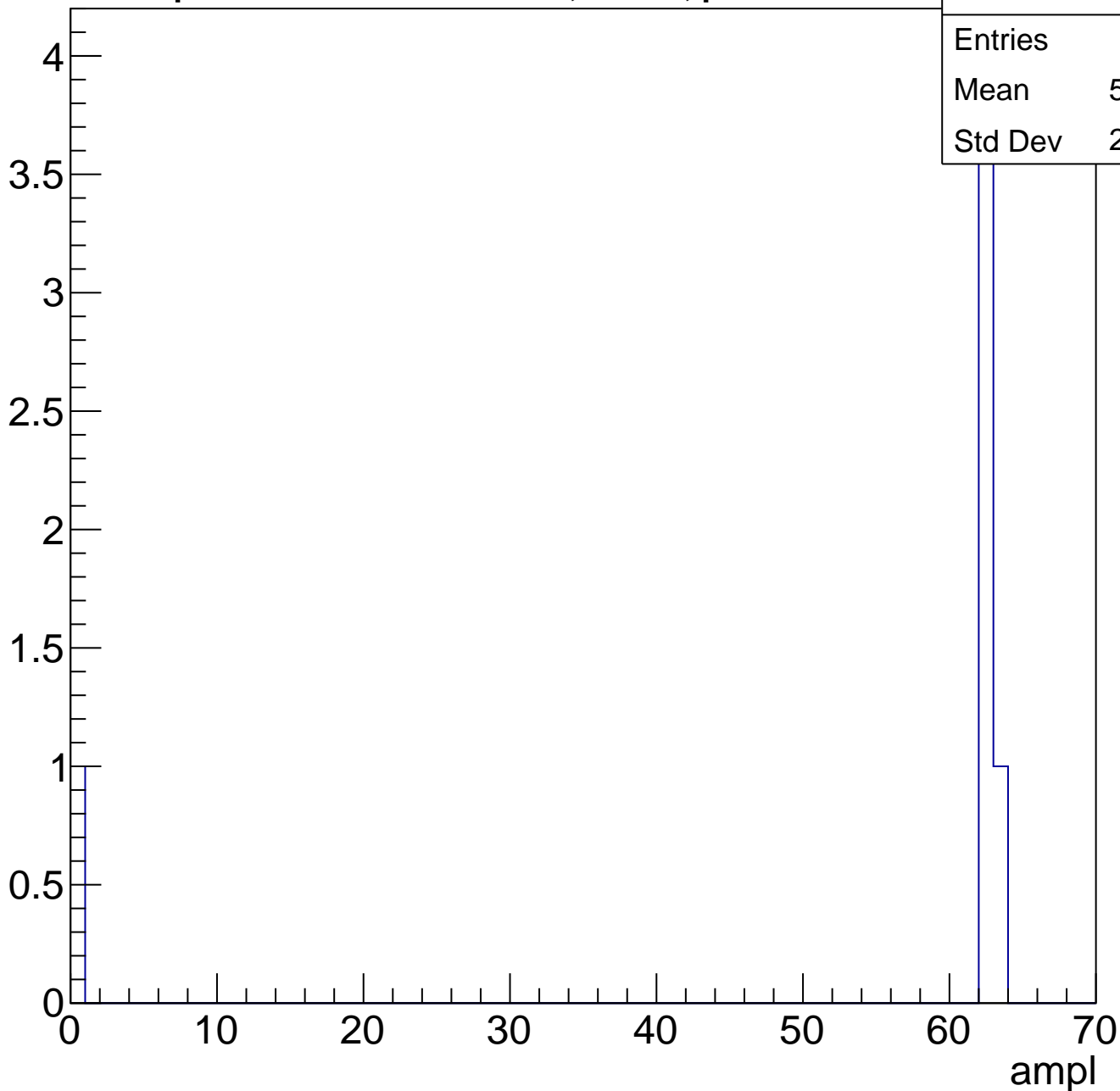
Entries	55
Mean	59.38
Std Dev	3.136



# B1L102S, U20-ch64, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

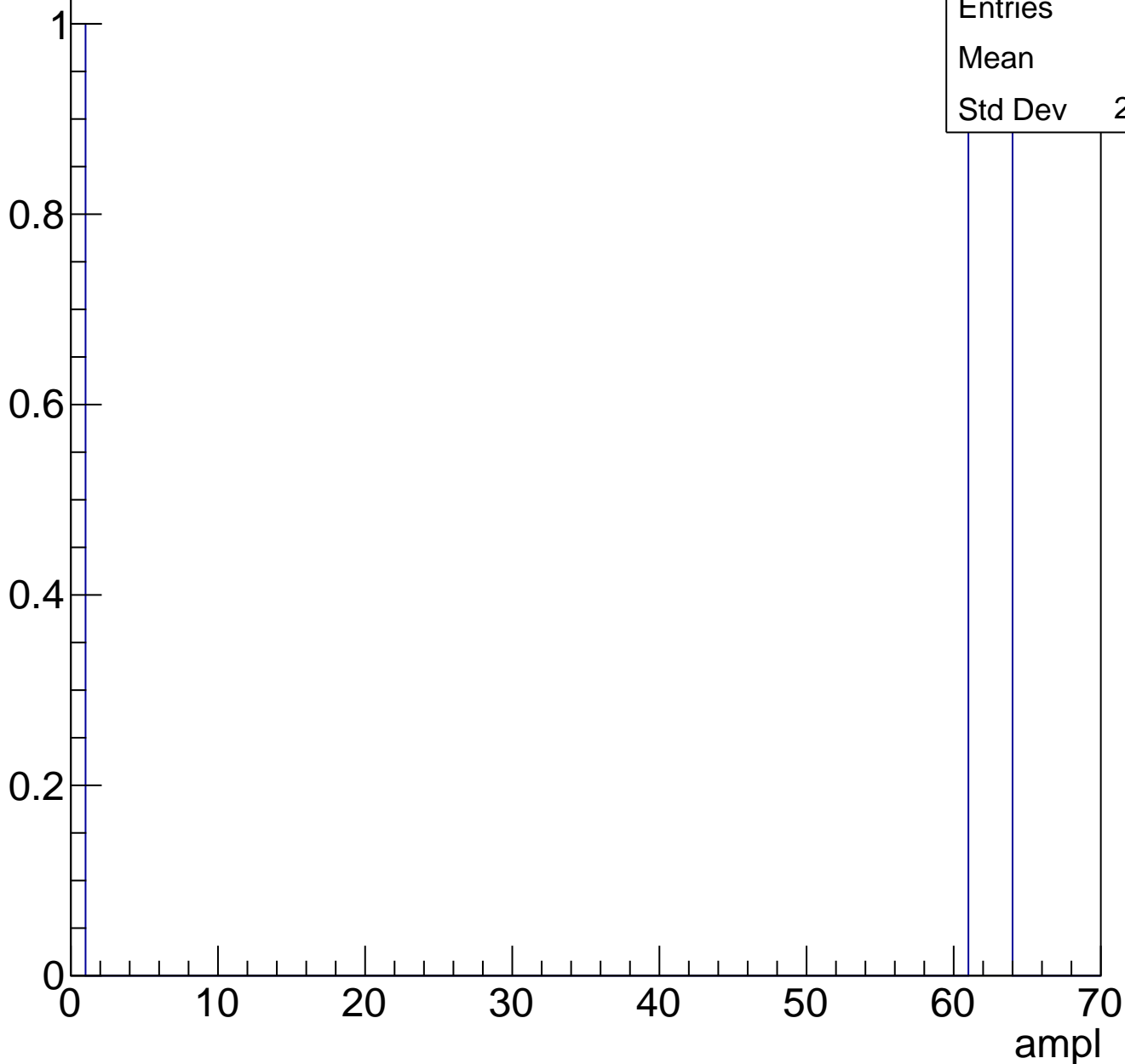




# B1L102S, U20-ch64, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch65, adc0

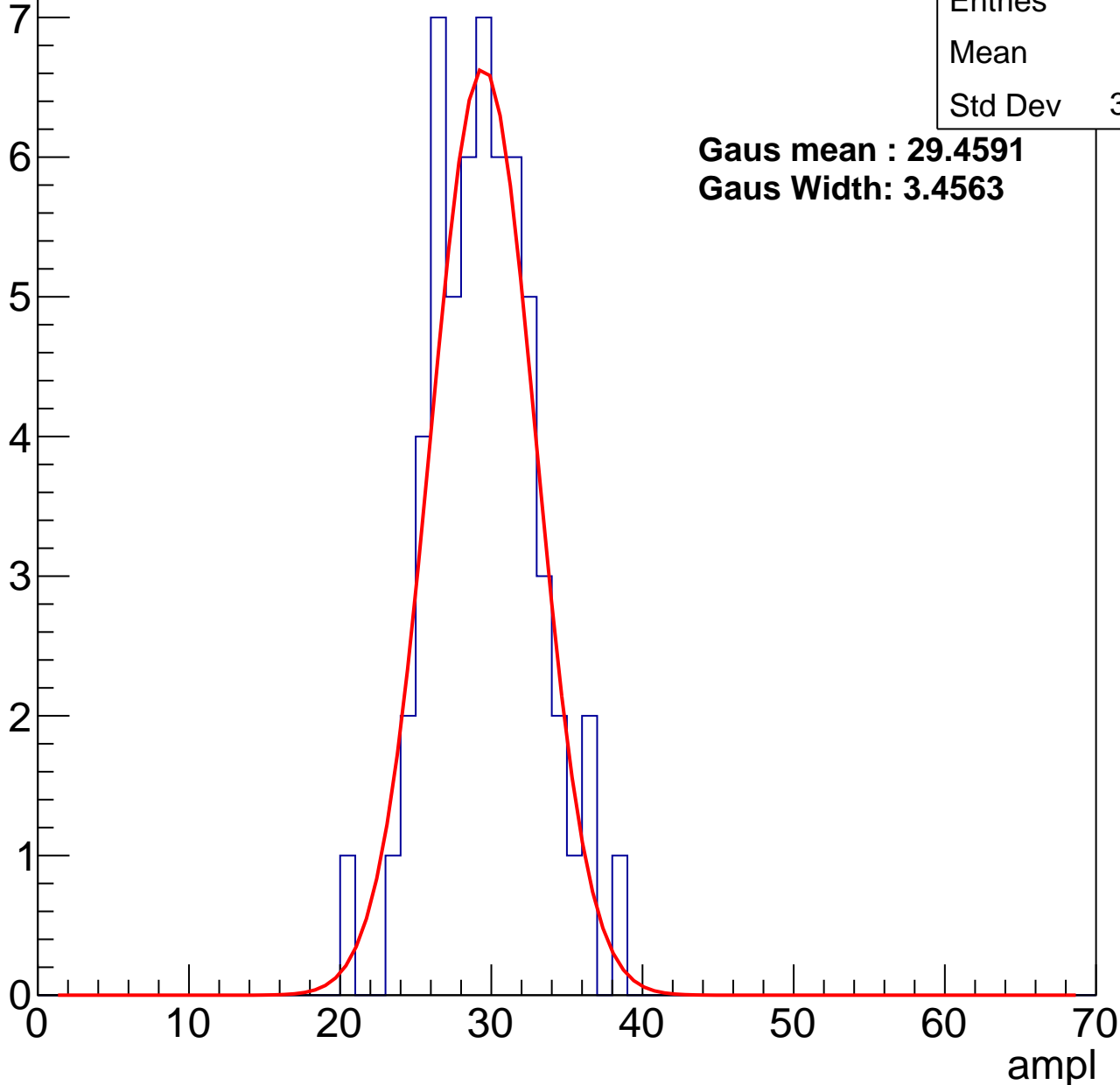
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	29.1
Std Dev	3.463

**Gaus mean : 29.4591**

**Gaus Width: 3.4563**



# B1L102S, U20-ch65, adc1

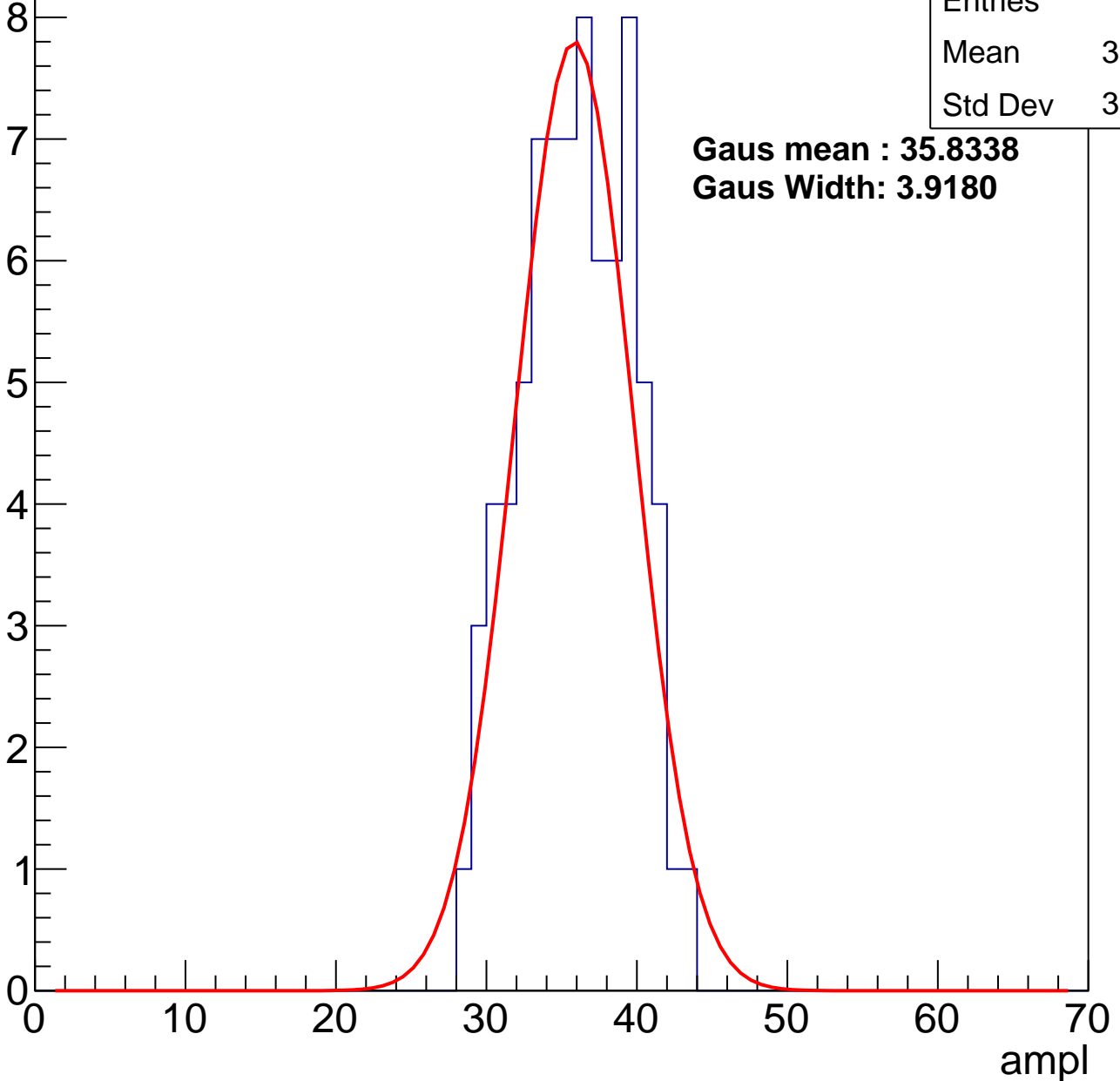
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	35.48
Std Dev	3.566

**Gaus mean : 35.8338**

**Gaus Width: 3.9180**



# B1L102S, U20-ch65, adc2

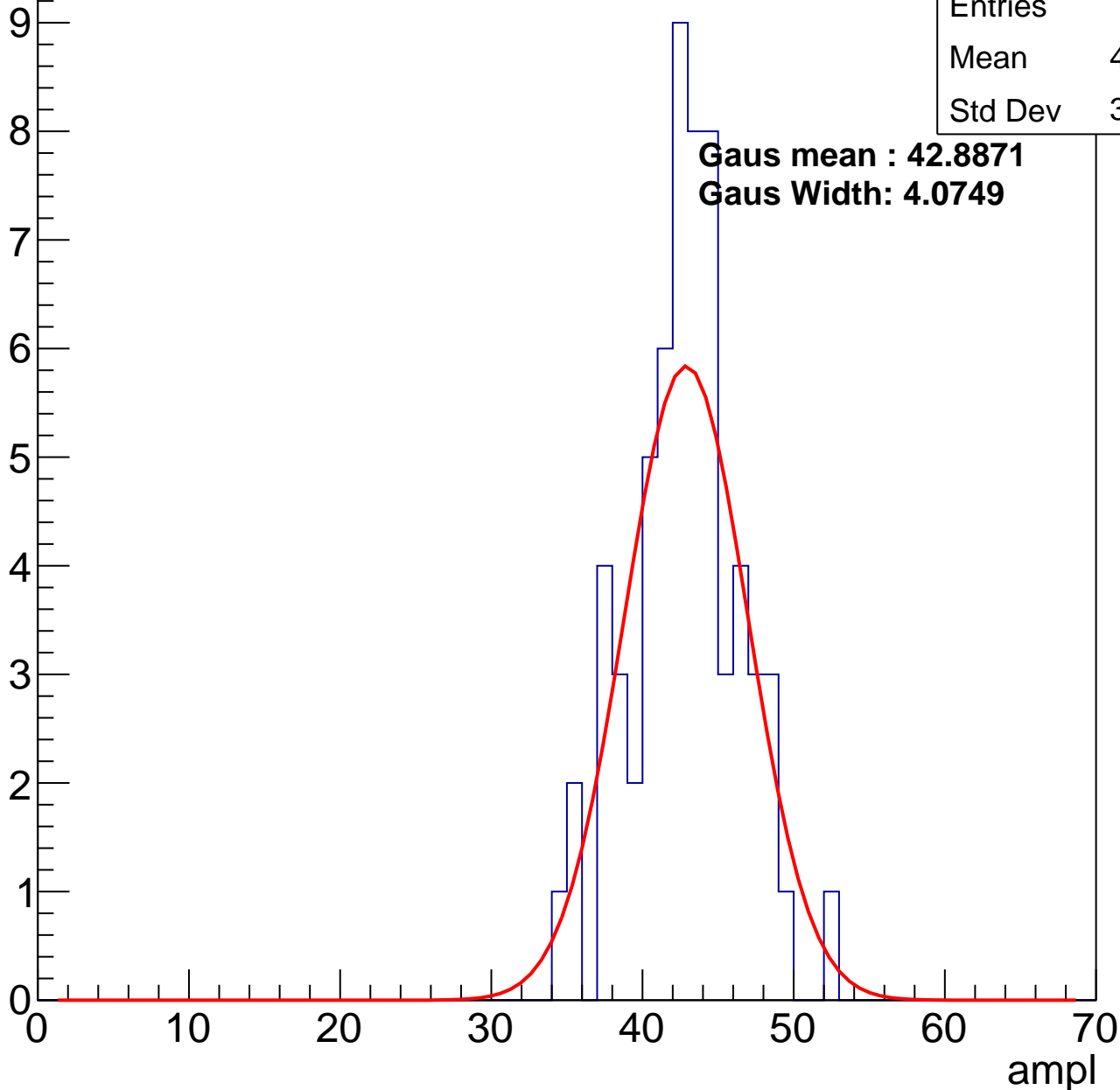
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	42.37
Std Dev	3.583

**Gaus mean : 42.8871**

**Gaus Width: 4.0749**

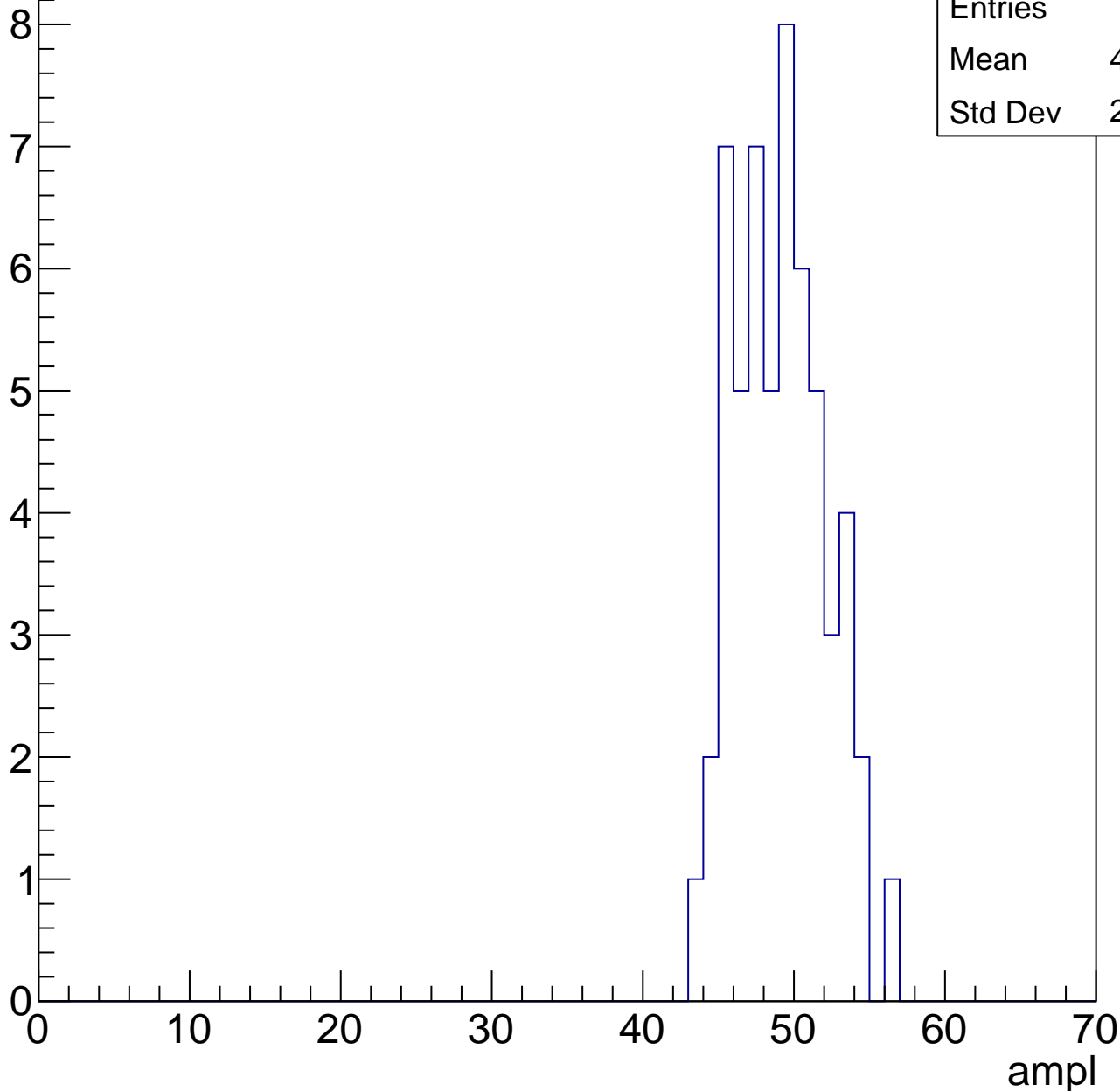


# B1L102S, U20-ch65, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

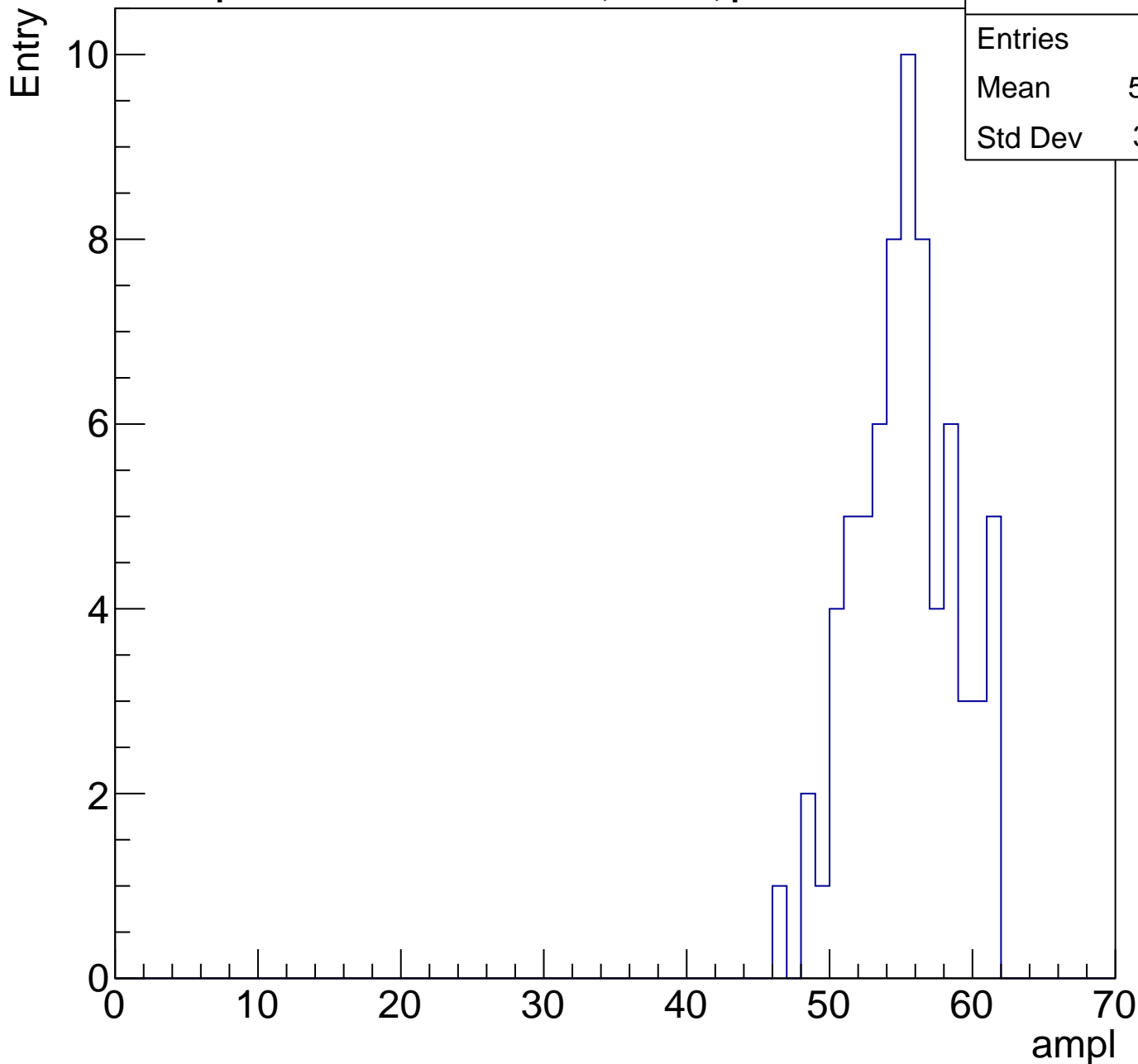
Entries	56
Mean	48.64
Std Dev	2.942



# B1L102S, U20-ch65, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	71
Mean	54.82
Std Dev	3.461

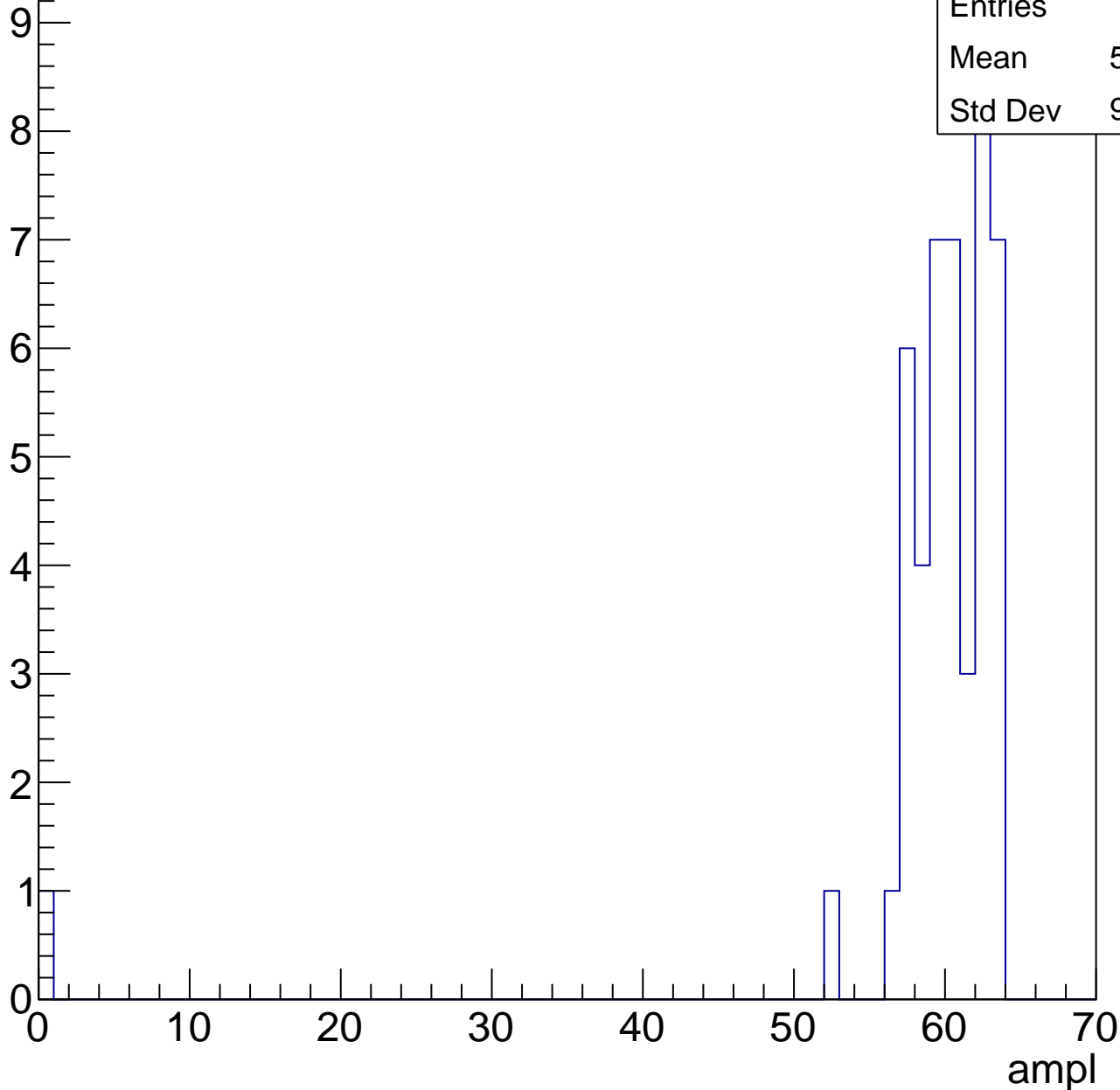


# B1L102S, U20-ch65, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	46
Mean	58.63
Std Dev	9.056



# B1L102S, U20-ch65, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U20-ch65, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U20-ch66, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	87
Mean	29.07
Std Dev	3.673

**Gaus mean : 29.6035**

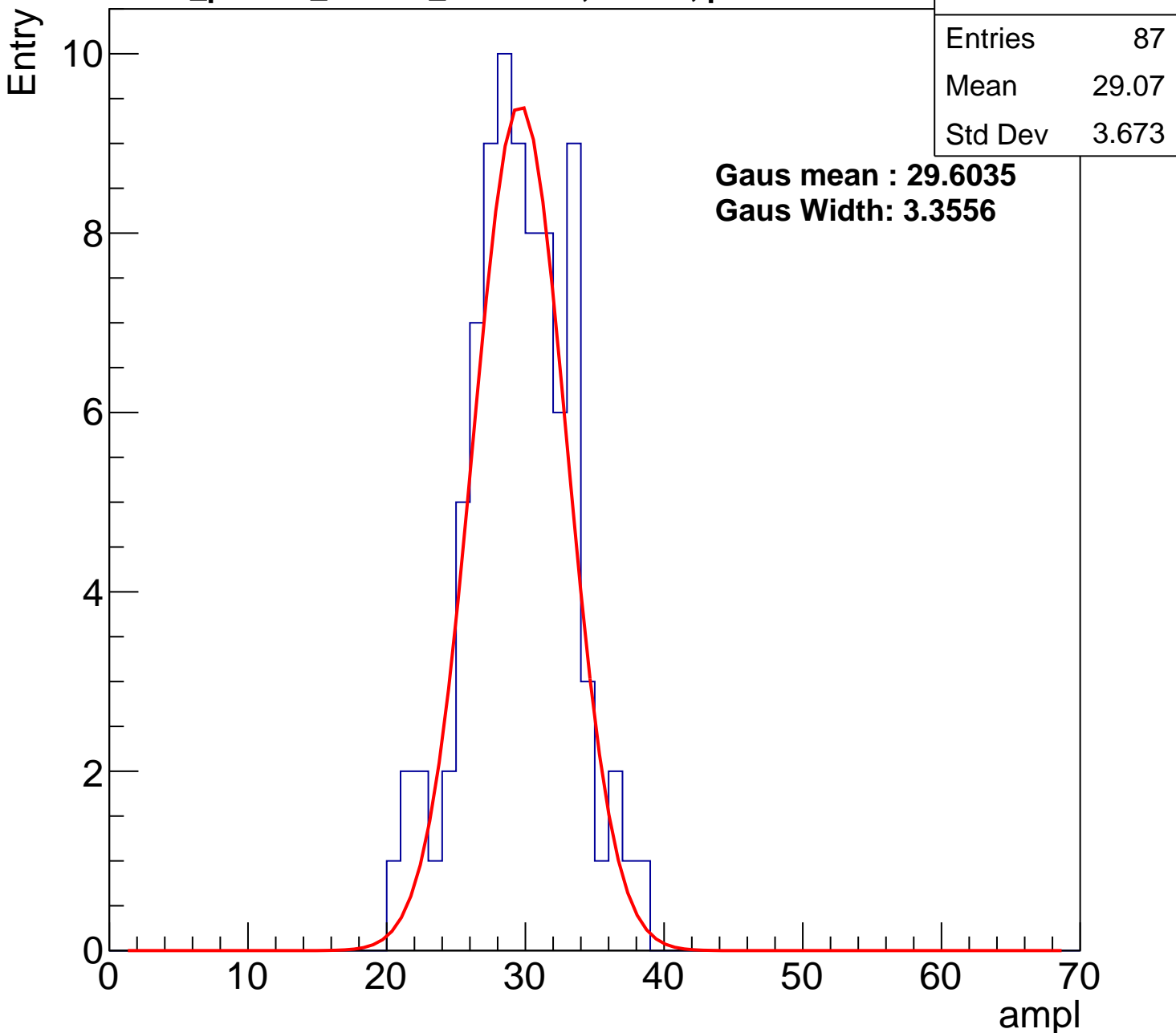
**Gaus Width: 3.3556**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U20-ch66, adc1

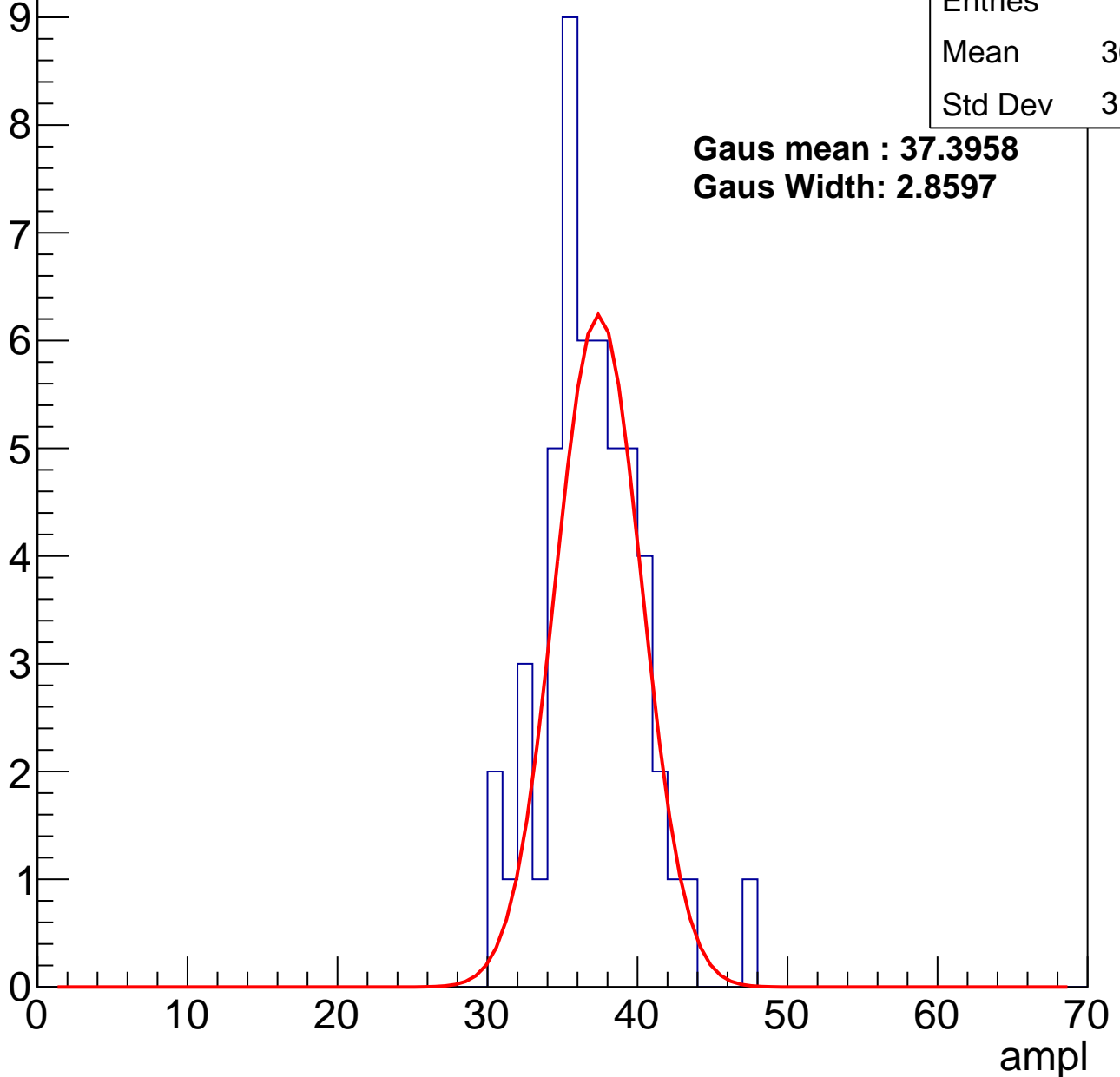
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	36.58
Std Dev	3.272

**Gaus mean : 37.3958**

**Gaus Width: 2.8597**



# B1L102S, U20-ch66, adc2

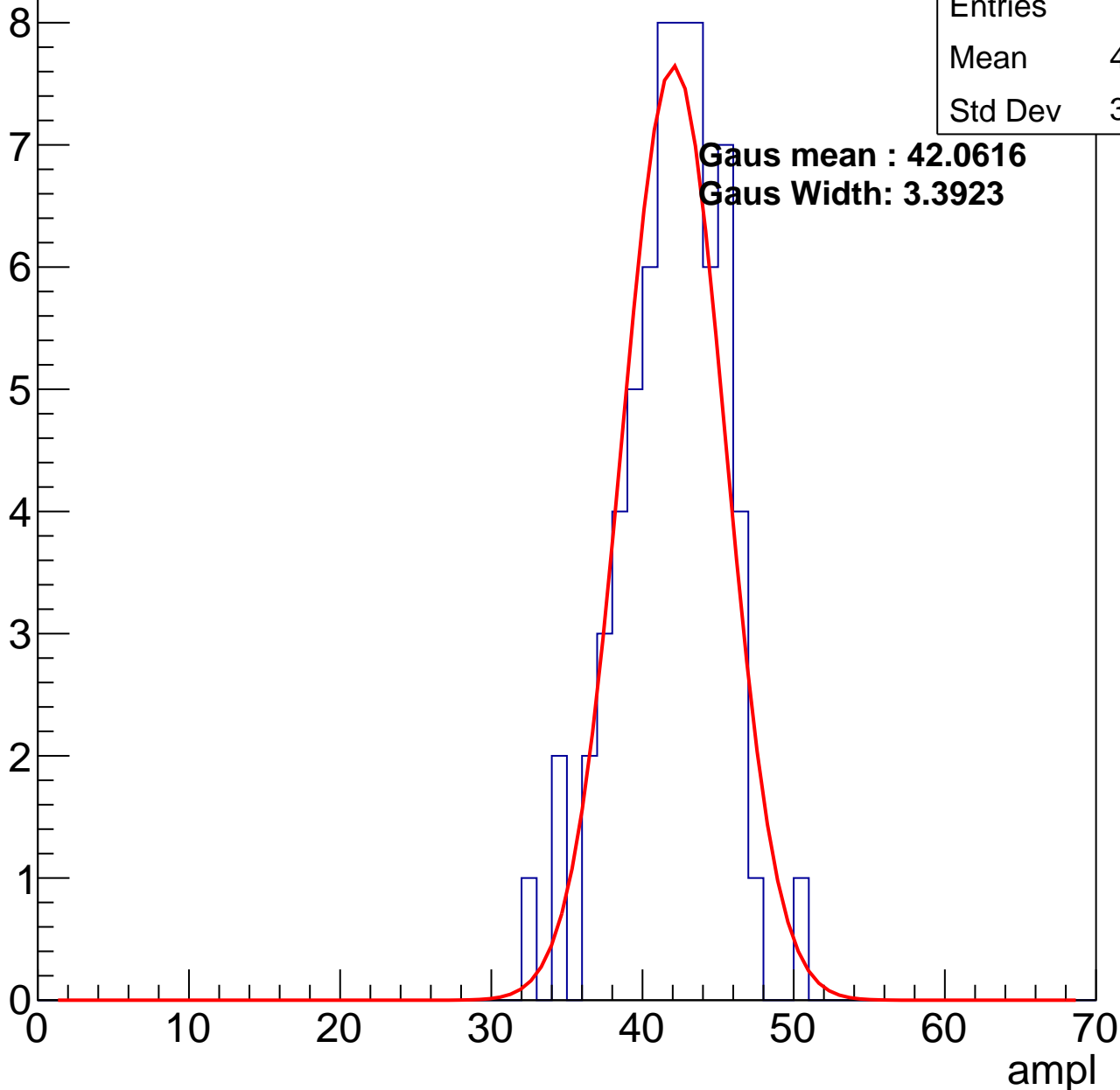
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	41.48
Std Dev	3.363

**Gaus mean : 42.0616**

**Gaus Width: 3.3923**

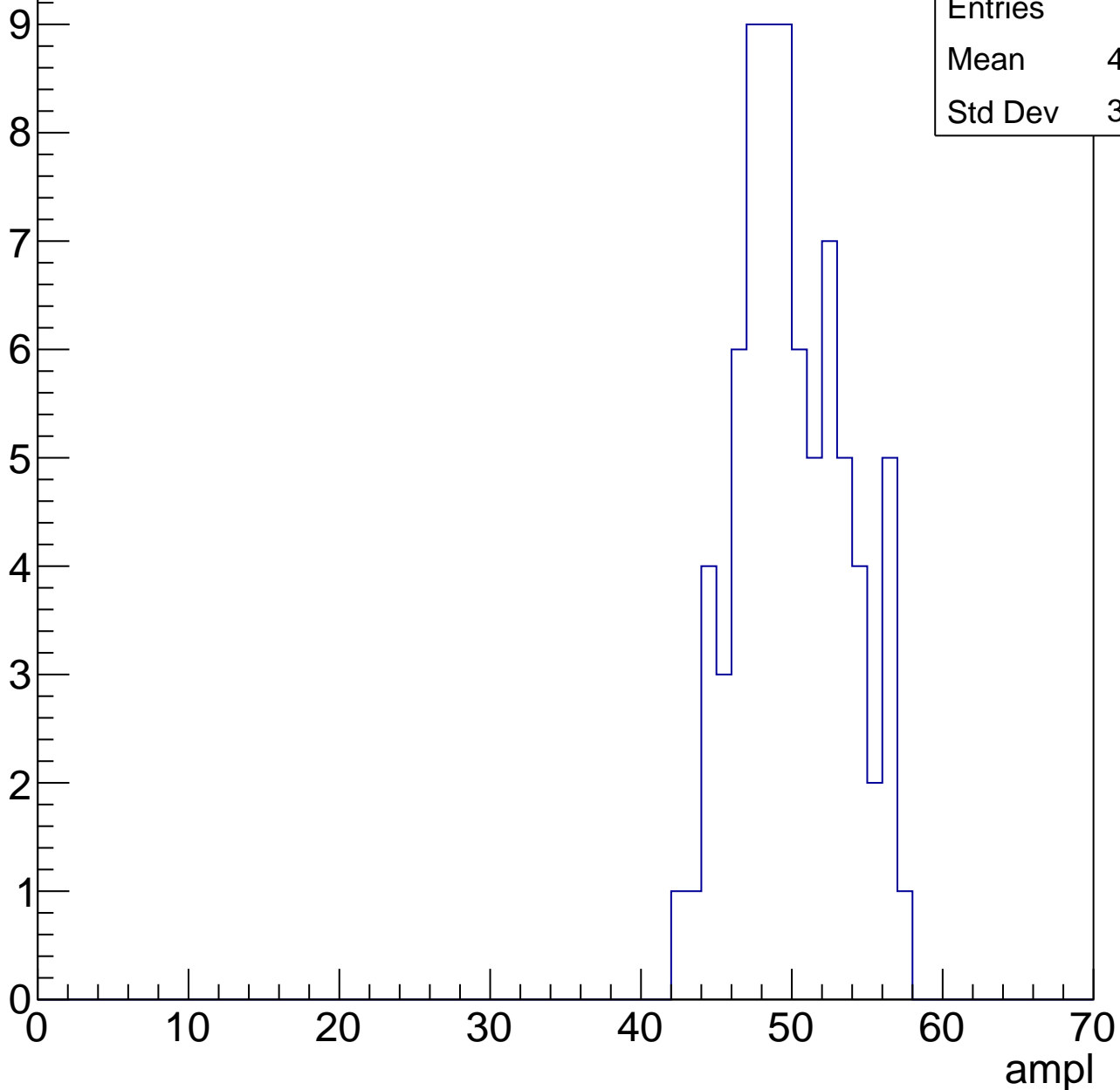


# B1L102S, U20-ch66, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	49.55
Std Dev	3.529

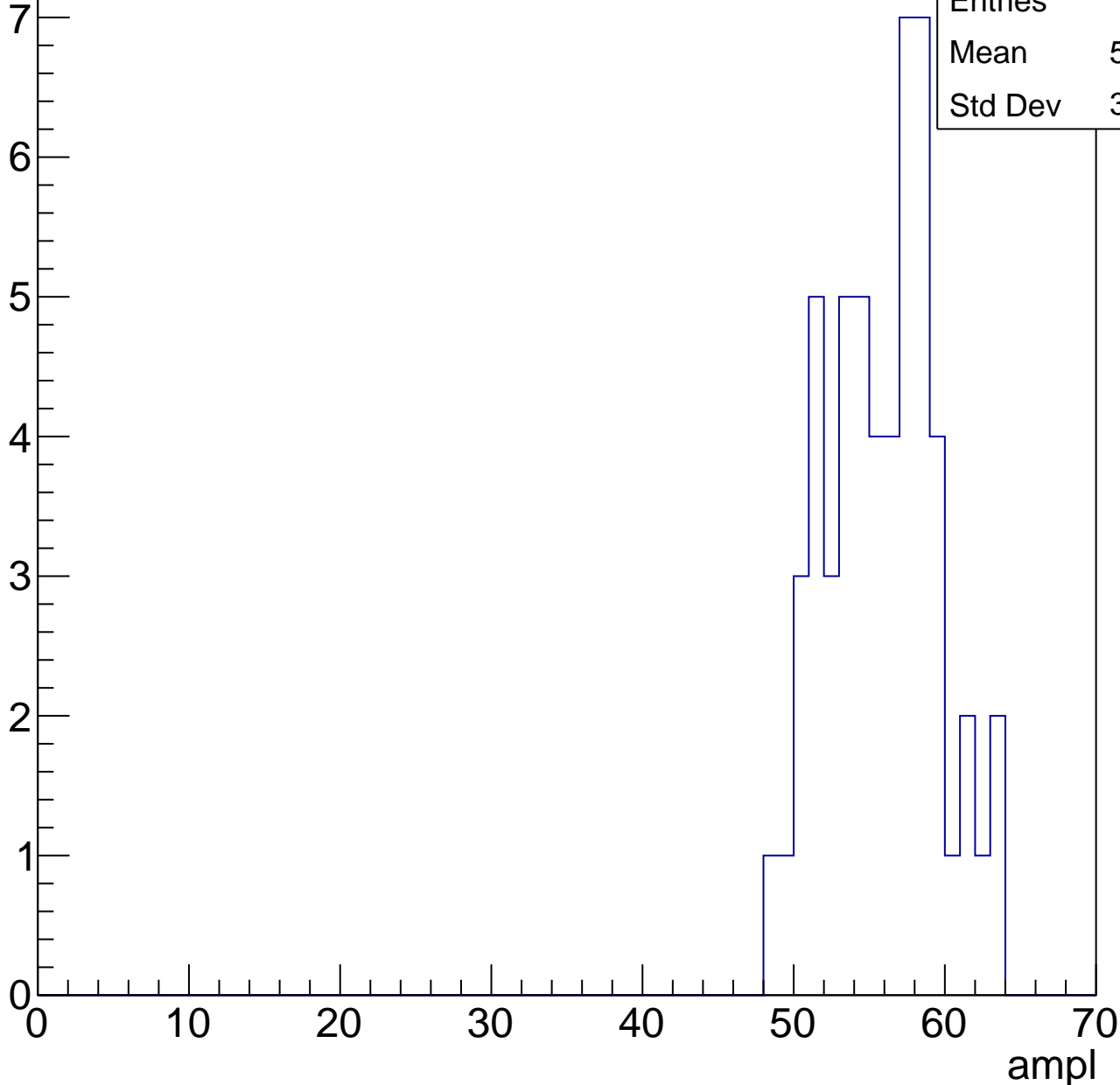


# B1L102S, U20-ch66, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	55.42
Std Dev	3.607

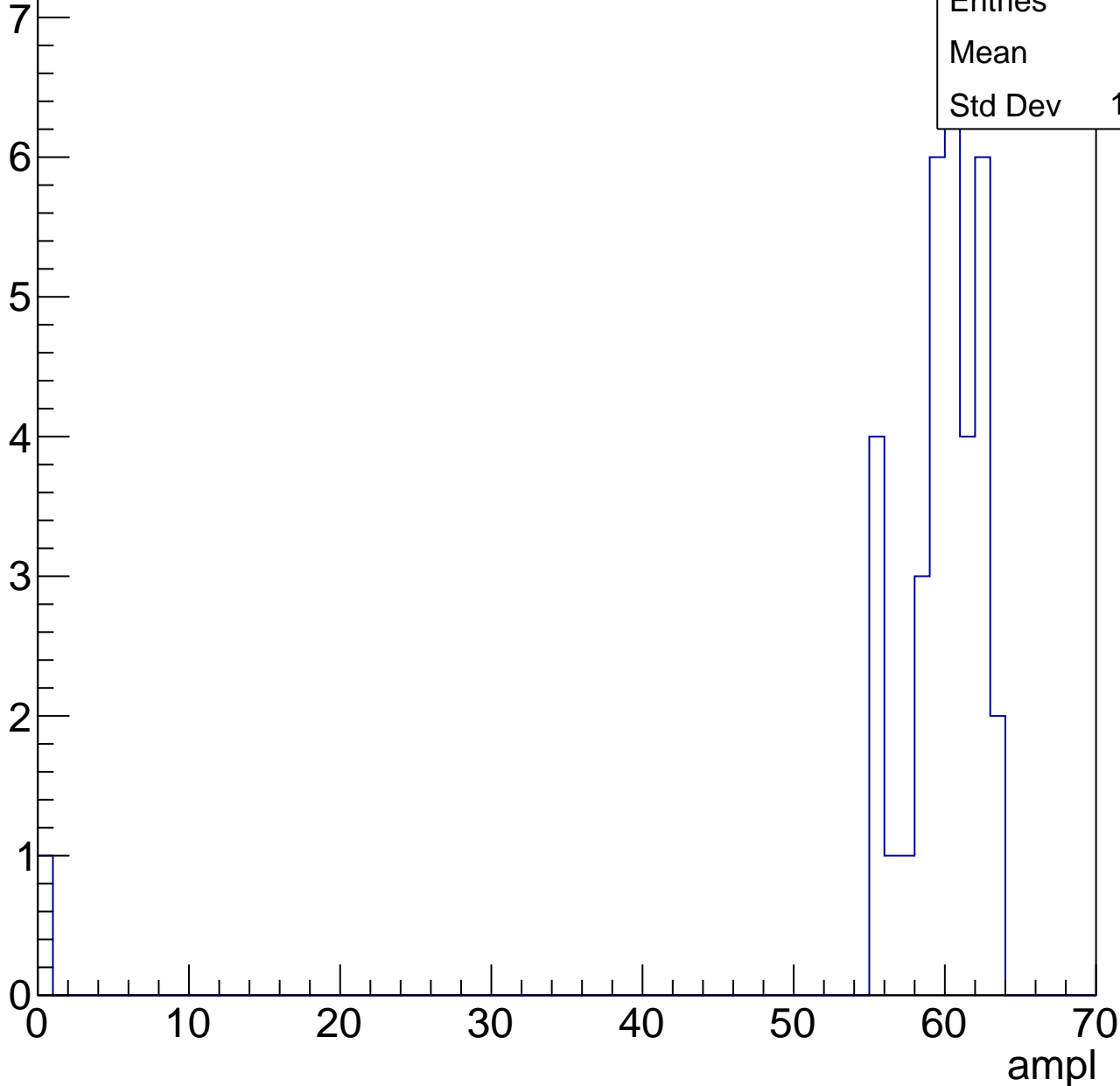


# B1L102S, U20-ch66, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	35
Mean	57.8
Std Dev	10.17

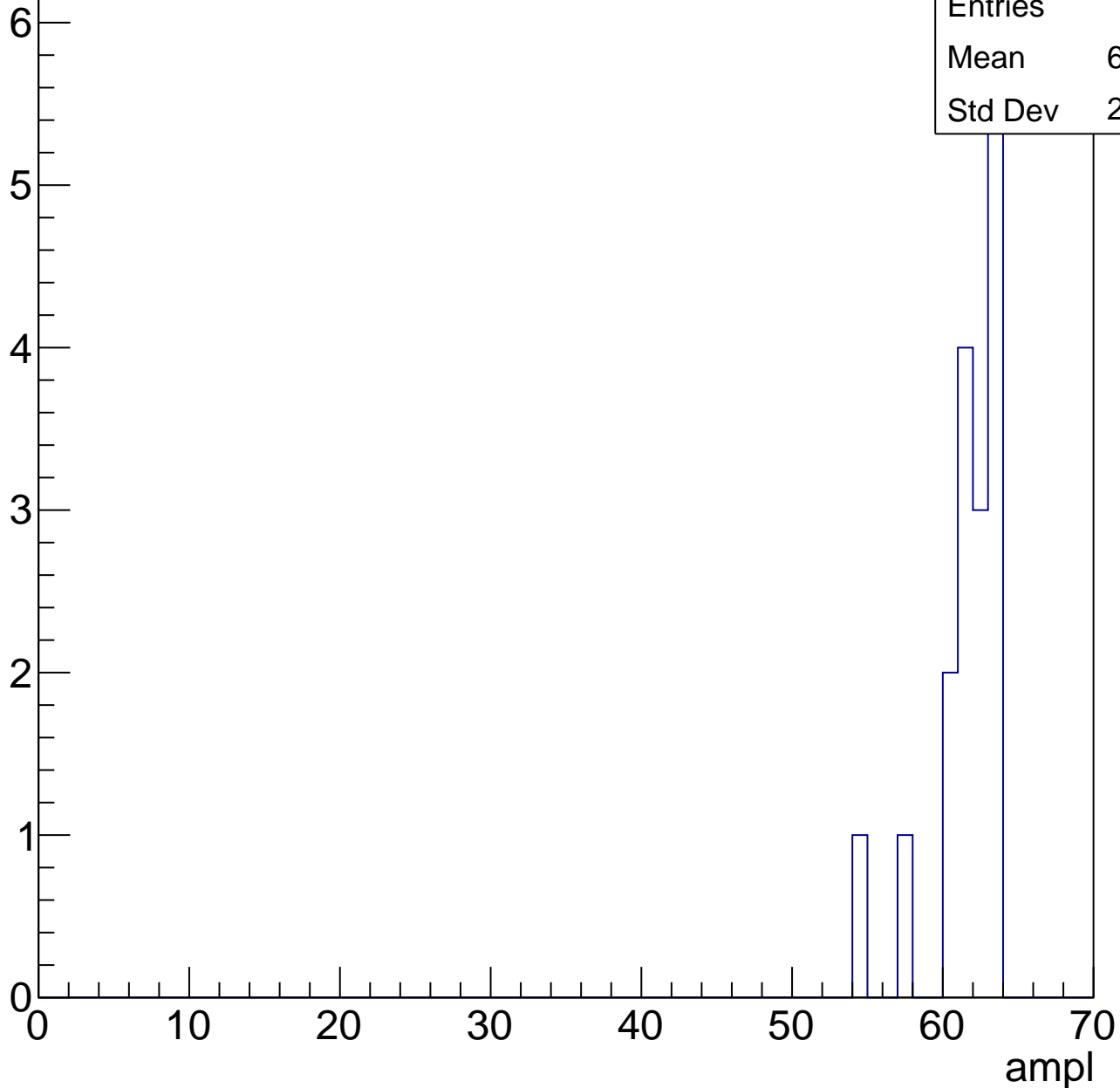


# B1L102S, U20-ch66, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	17
Mean	61.12
Std Dev	2.349





# B1L102S, U20-ch66, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U20-ch67, adc0

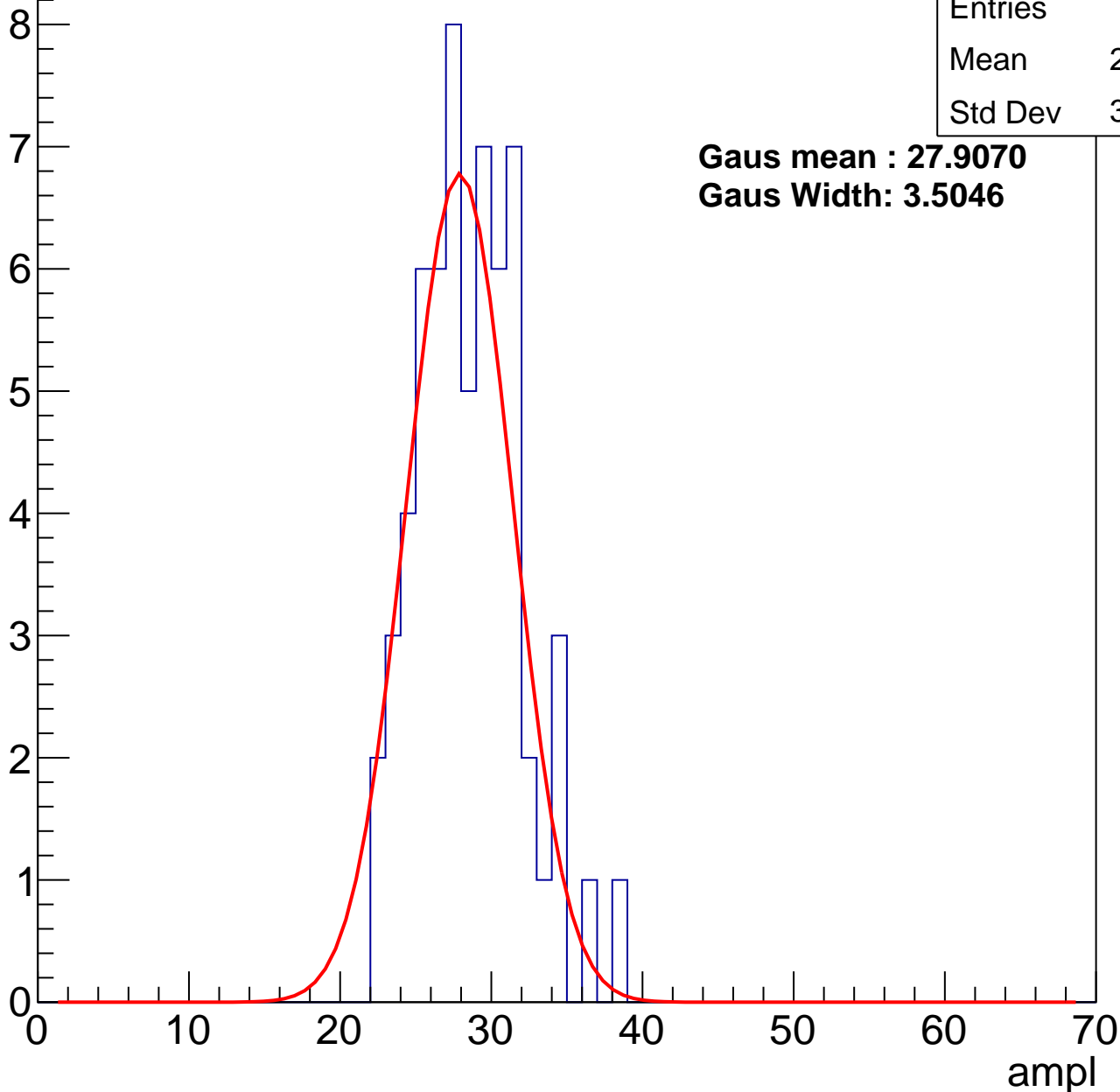
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	28.13
Std Dev	3.405

**Gaus mean : 27.9070**

**Gaus Width: 3.5046**



# B1L102S, U20-ch67, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	92
Mean	36.23
Std Dev	3.557

**Gaus mean : 36.6649**

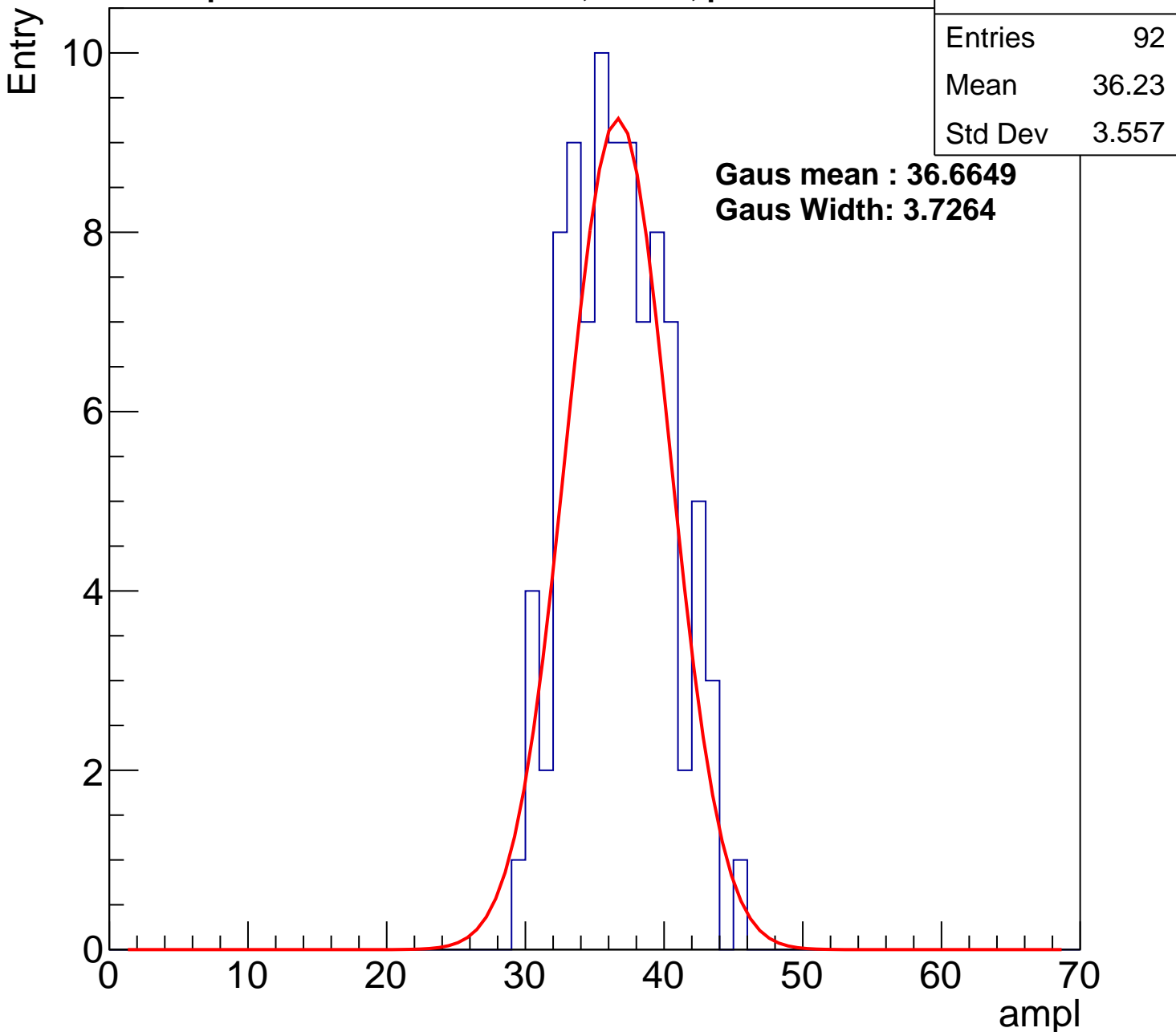
**Gaus Width: 3.7264**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U20-ch67, adc2

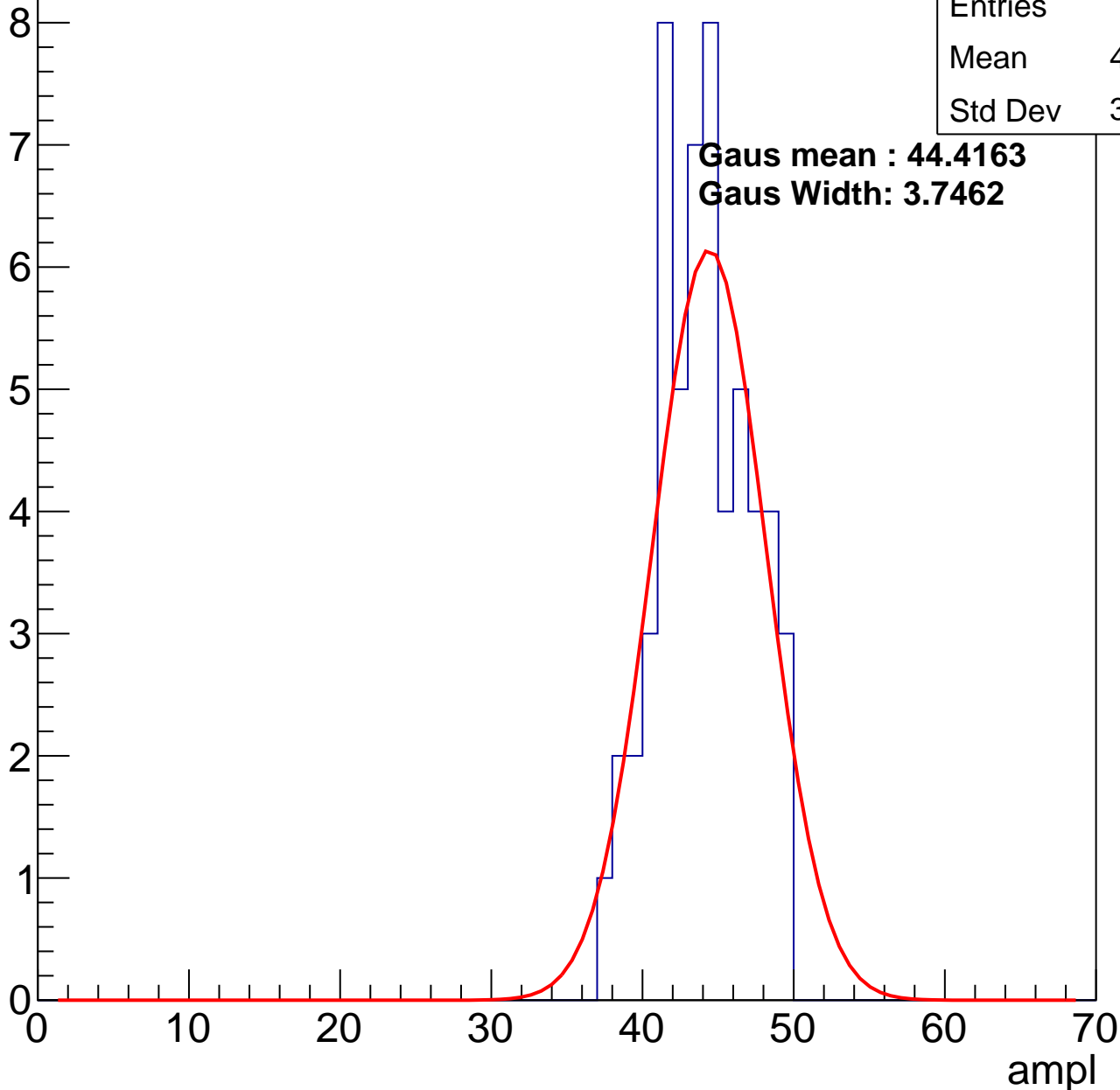
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	43.55
Std Dev	3.005

**Gaus mean : 44.4163**

**Gaus Width: 3.7462**

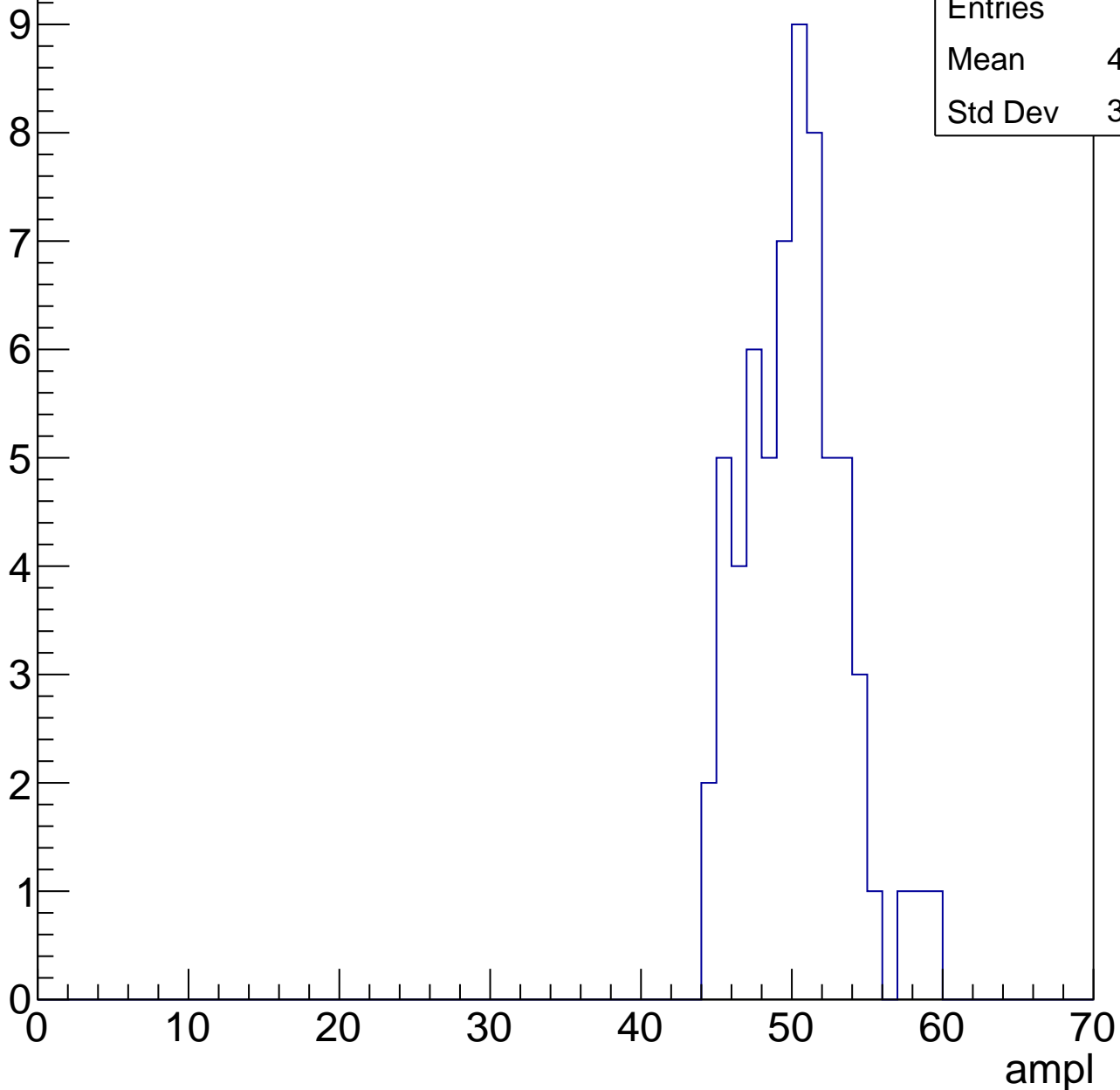


# B1L102S, U20-ch67, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	49.78
Std Dev	3.283

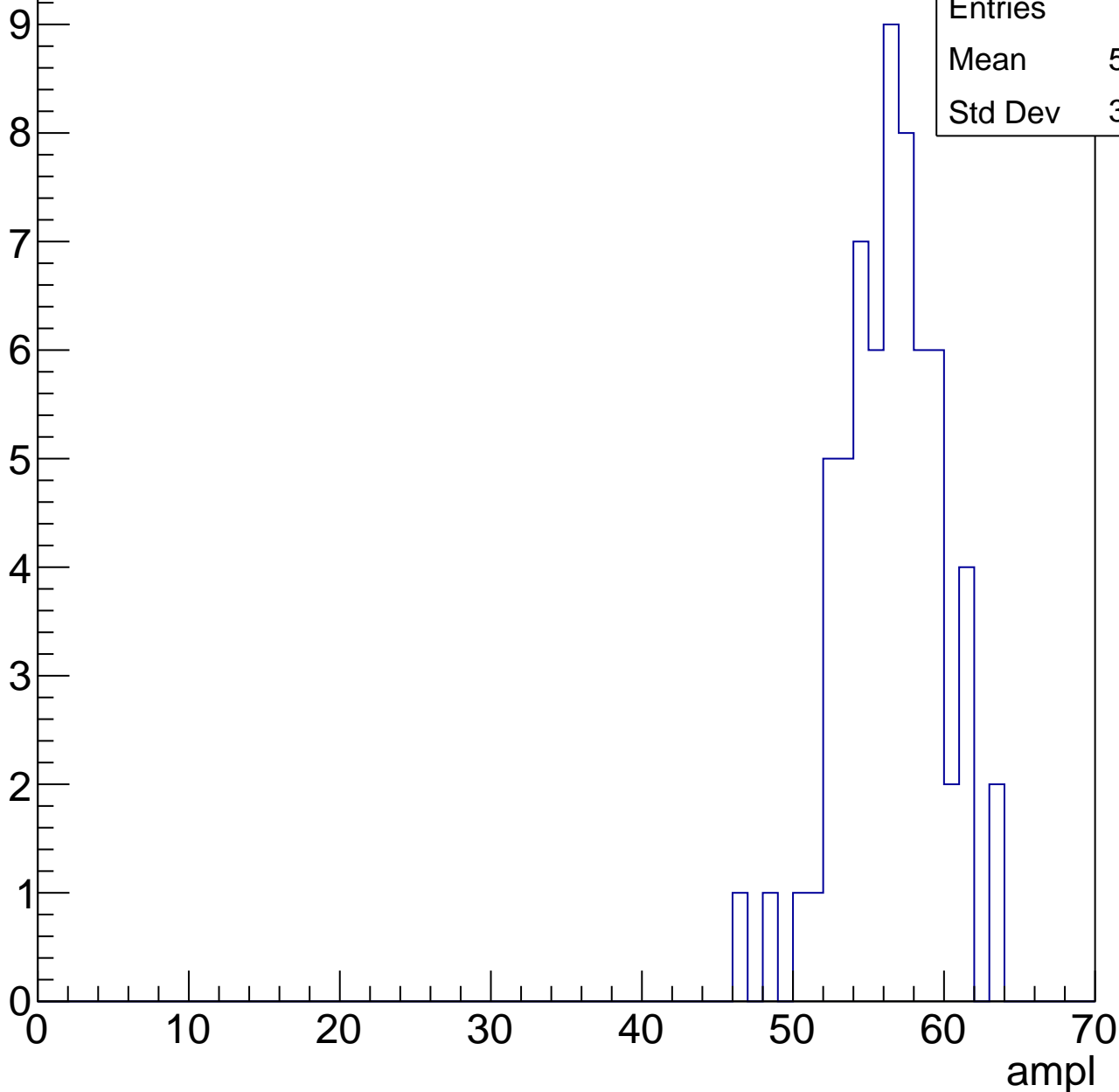


# B1L102S, U20-ch67, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	55.94
Std Dev	3.307

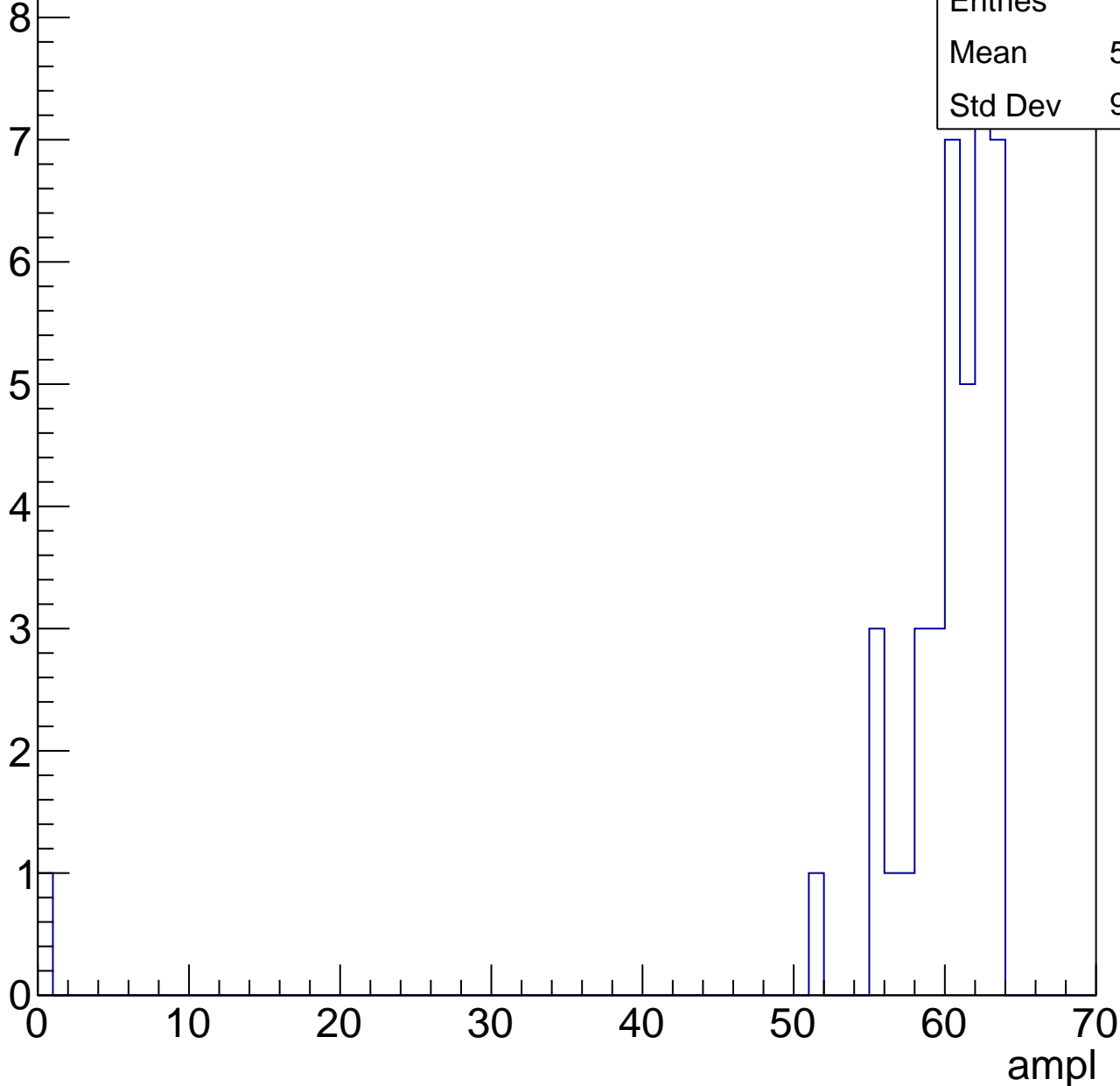


# B1L102S, U20-ch67, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	40
Mean	58.55
Std Dev	9.762



# B1L102S, U20-ch67, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U20-ch67, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch68, adc0

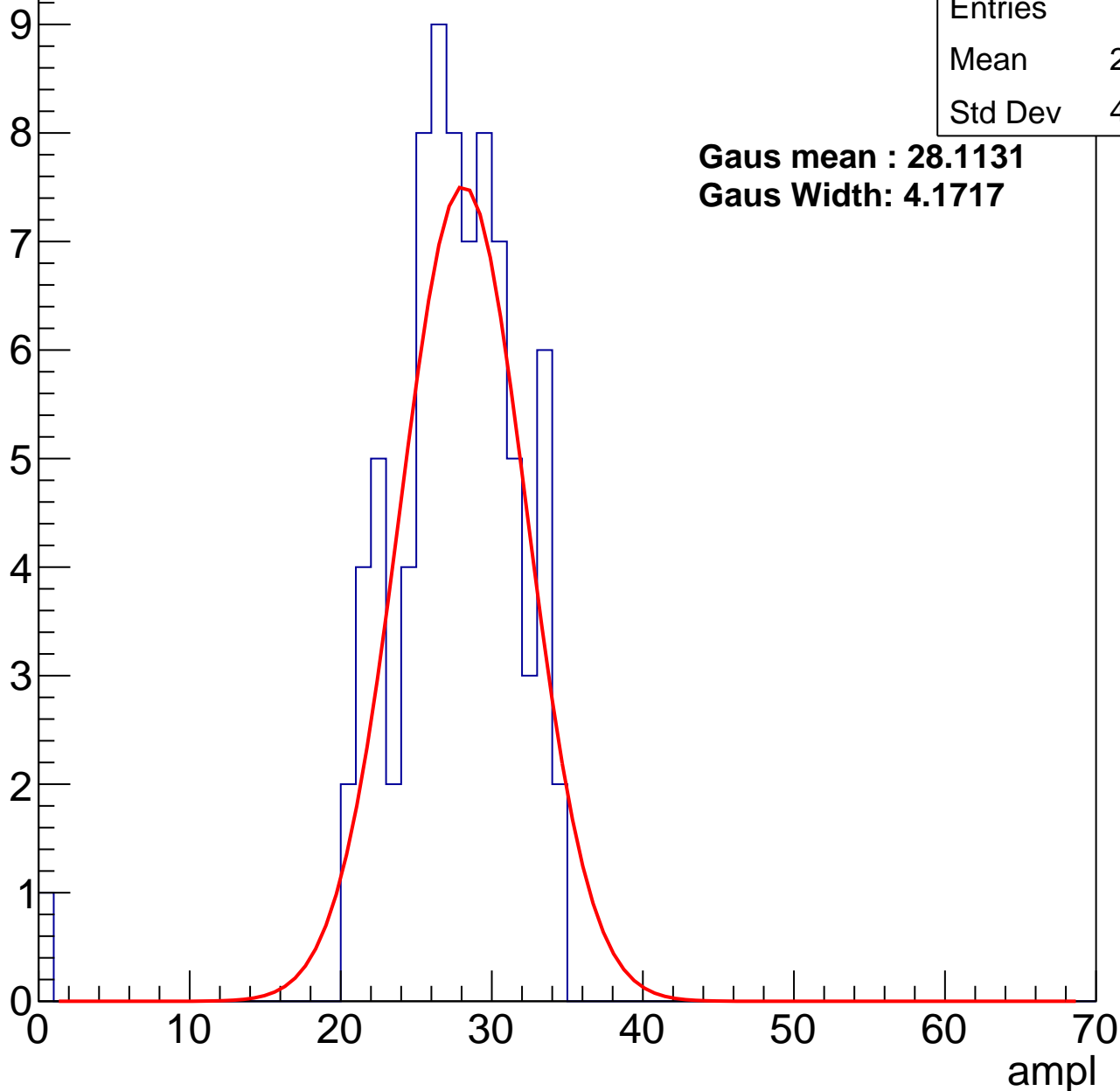
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	81
Mean	26.93
Std Dev	4.682

**Gaus mean : 28.1131**

**Gaus Width: 4.1717**



# B1L102S, U20-ch68, adc1

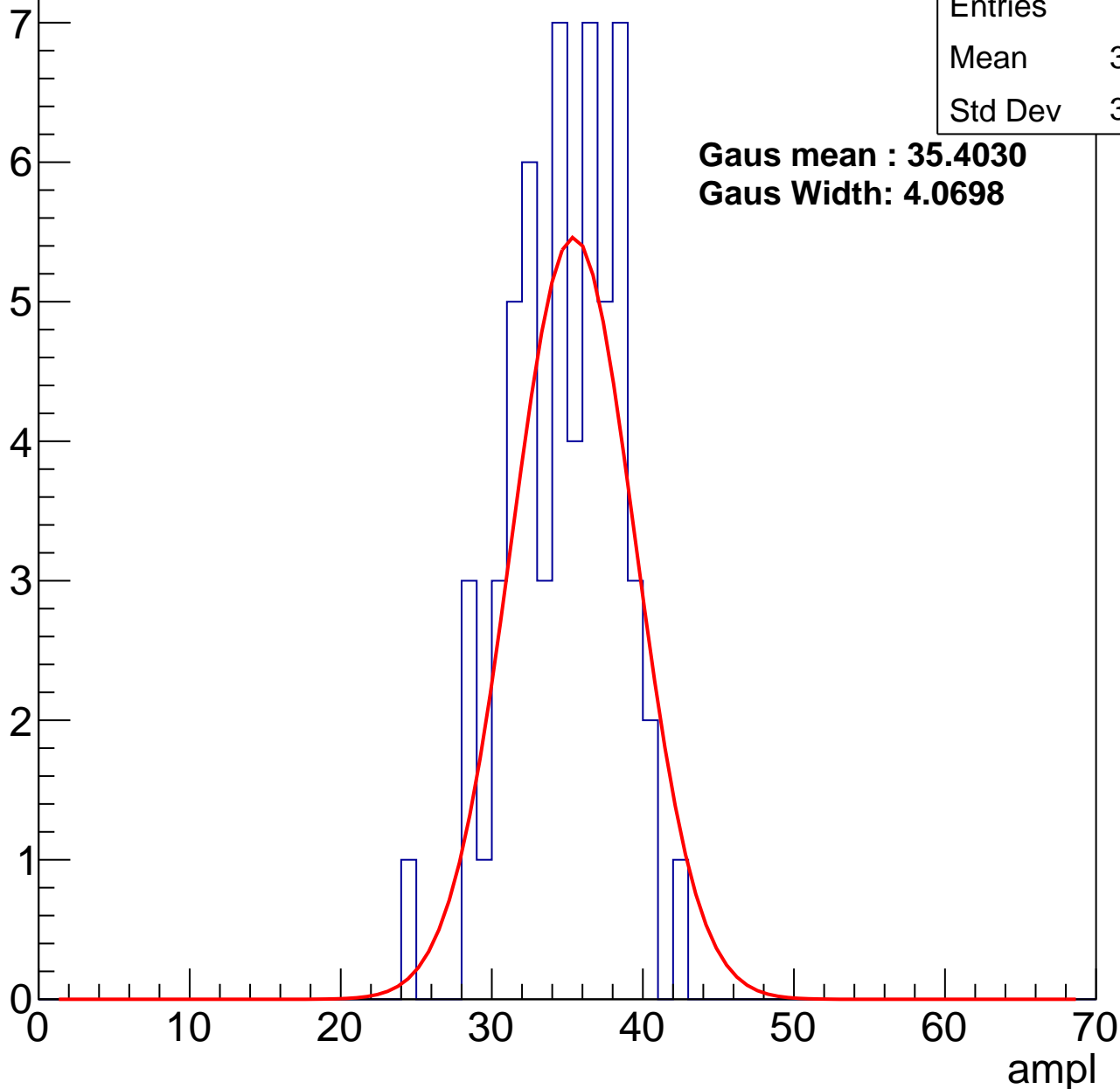
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	34.36
Std Dev	3.585

**Gaus mean : 35.4030**

**Gaus Width: 4.0698**



# B1L102S, U20-ch68, adc2

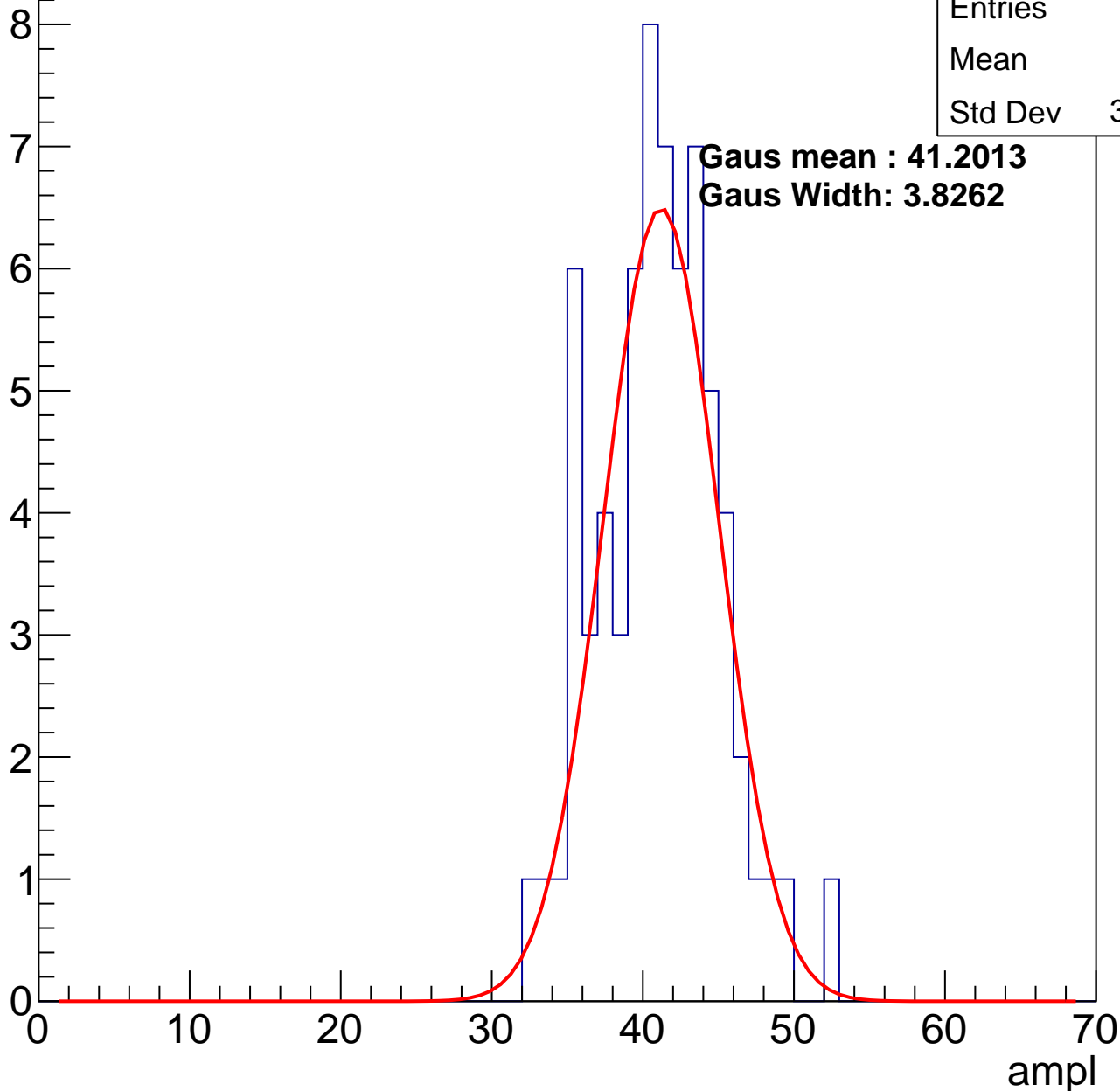
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	40.6
Std Dev	3.949

**Gaus mean : 41.2013**

**Gaus Width: 3.8262**

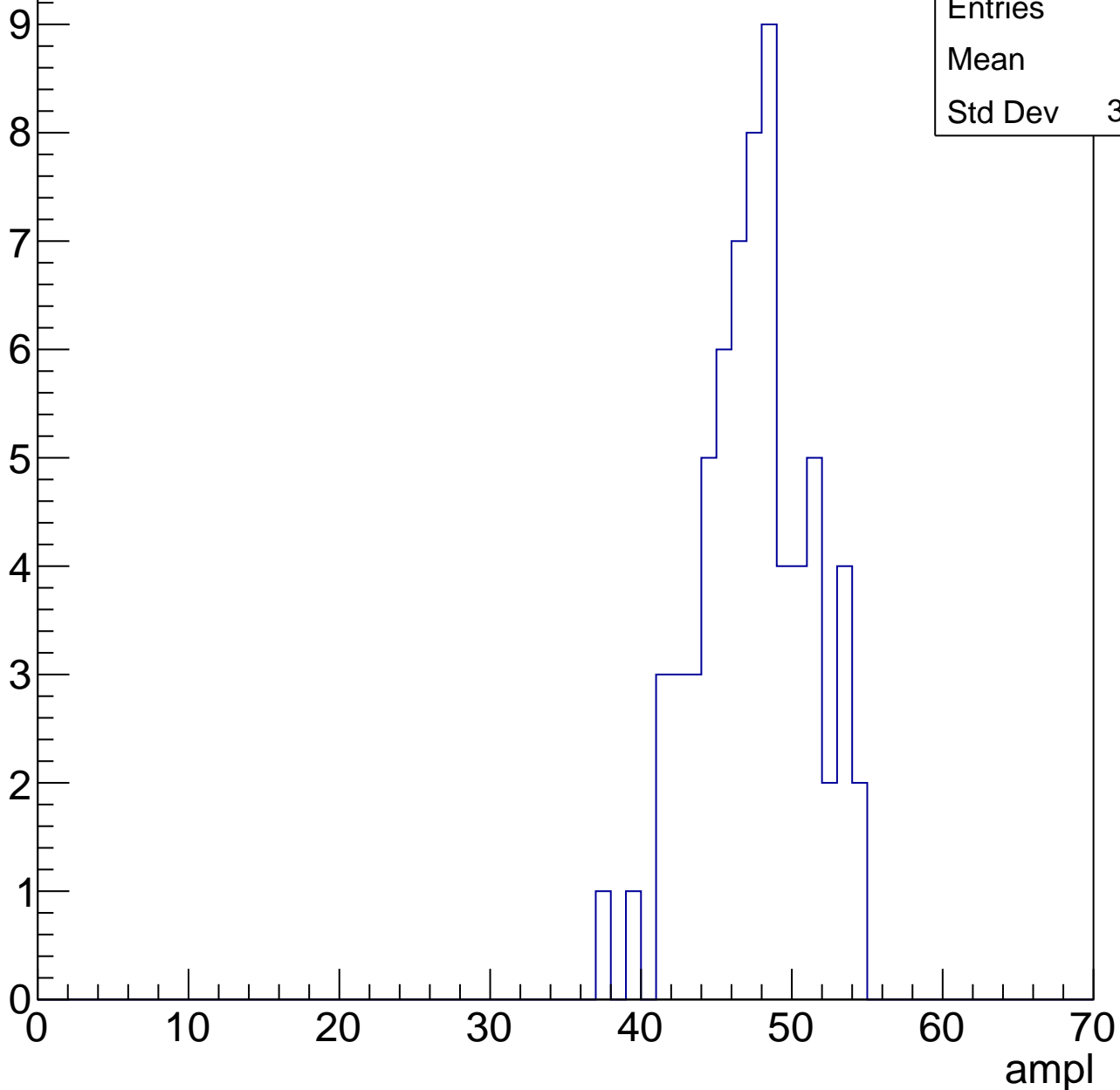


# B1L102S, U20-ch68, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	47
Std Dev	3.673

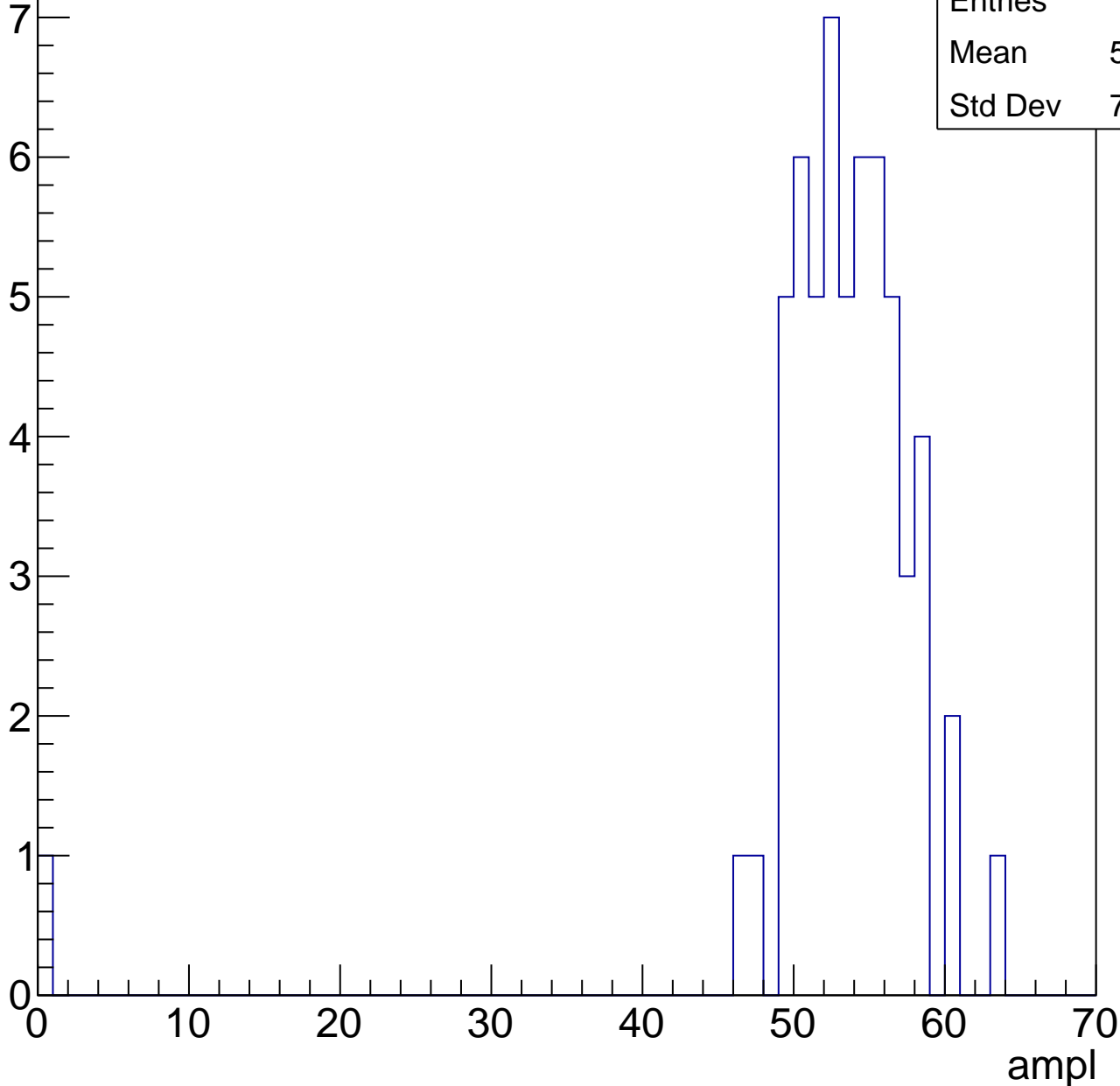


# B1L102S, U20-ch68, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	52.45
Std Dev	7.722



# B1L102S, U20-ch68, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

70

ampl

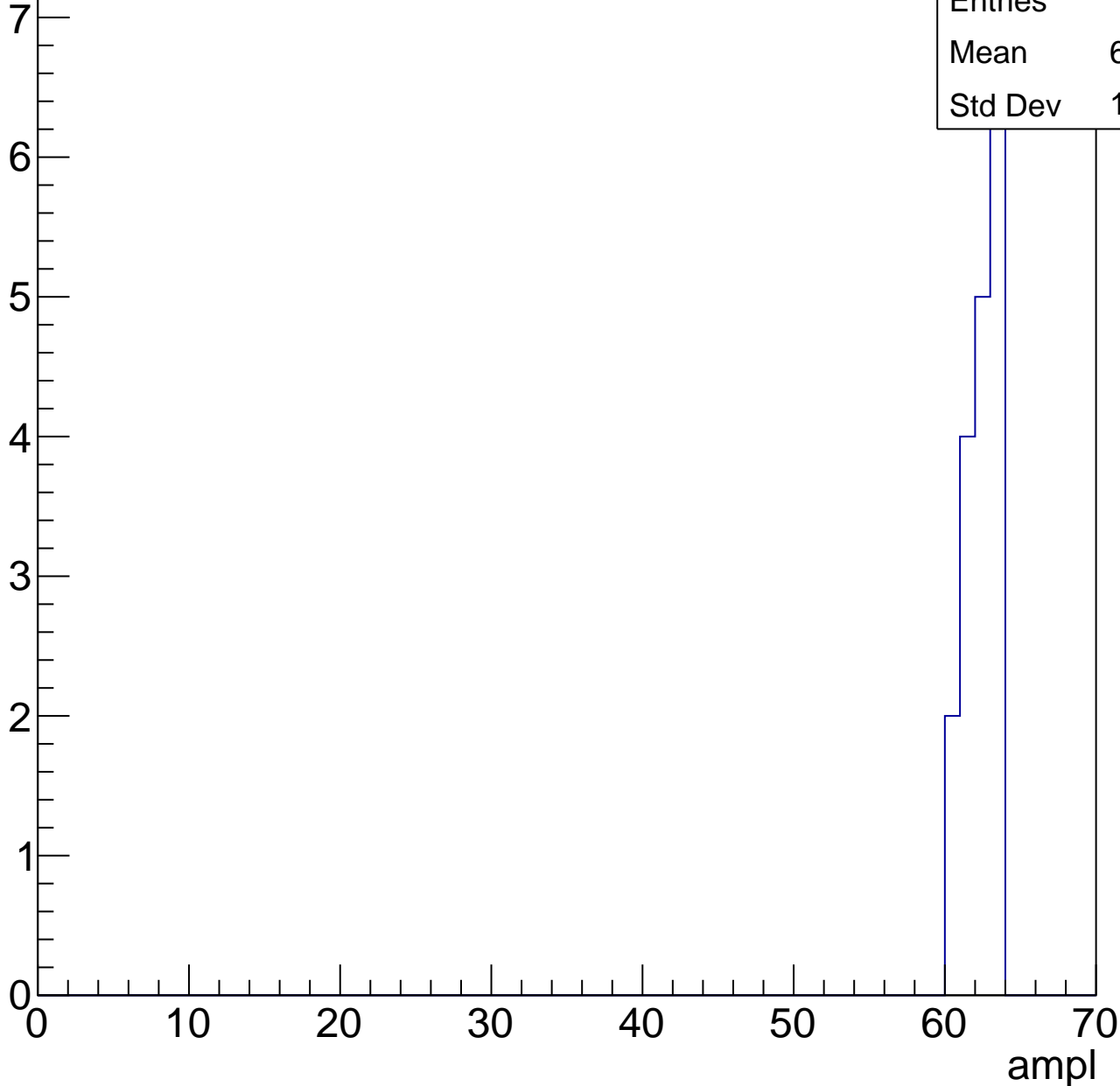
Entries	54
Mean	58.52
Std Dev	2.448

# B1L102S, U20-ch68, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	18
Mean	61.94
Std Dev	1.026





# B1L102S, U20-ch68, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	20
Std Dev	0

# B1L102S, U20-ch69, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	78
Mean	27.64
Std Dev	3.724

**Gaus mean : 28.1359**

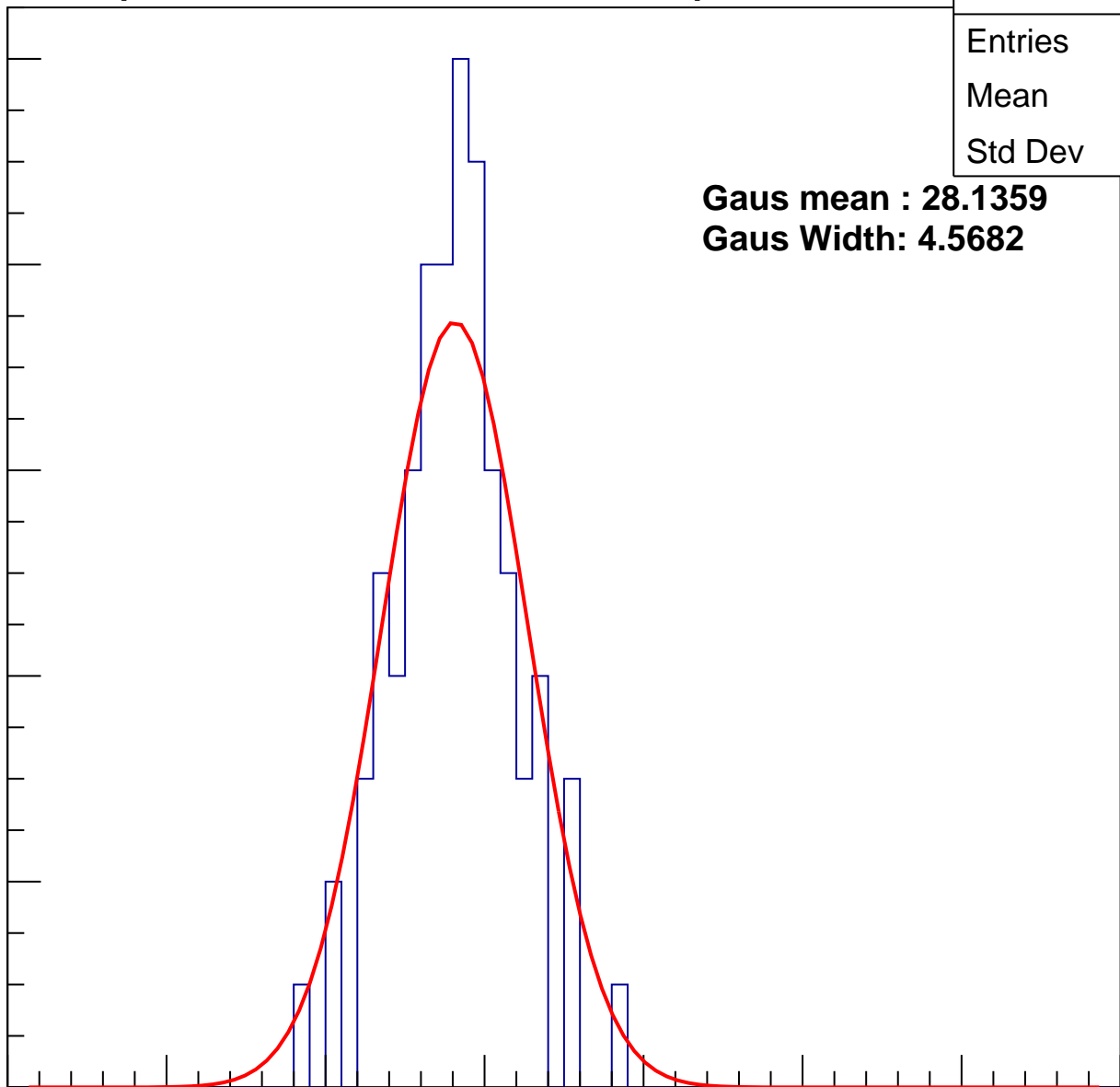
**Gaus Width: 4.5682**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L102S, U20-ch69, adc1

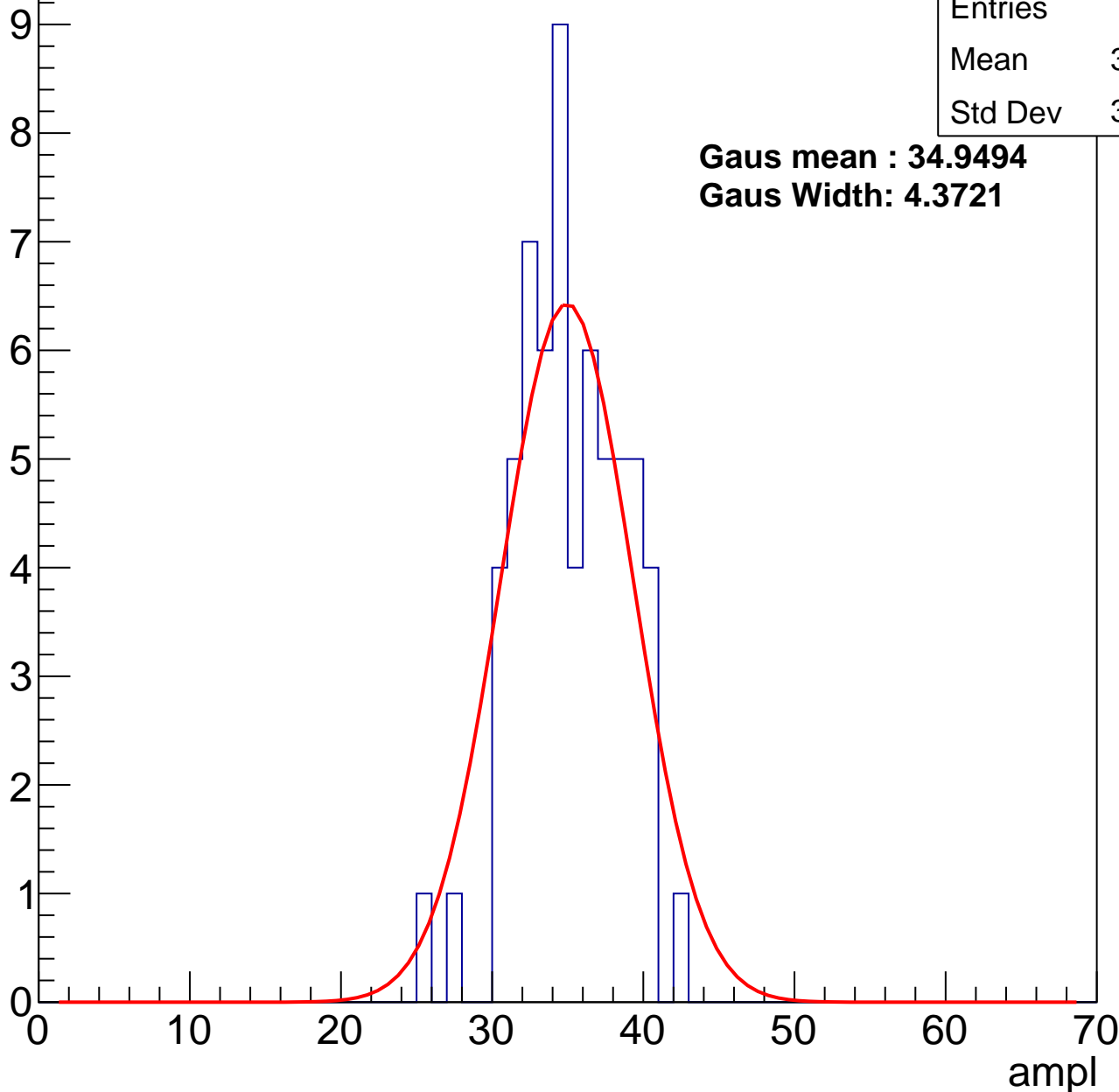
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	34.65
Std Dev	3.409

**Gaus mean : 34.9494**

**Gaus Width: 4.3721**



# B1L102S, U20-ch69, adc2

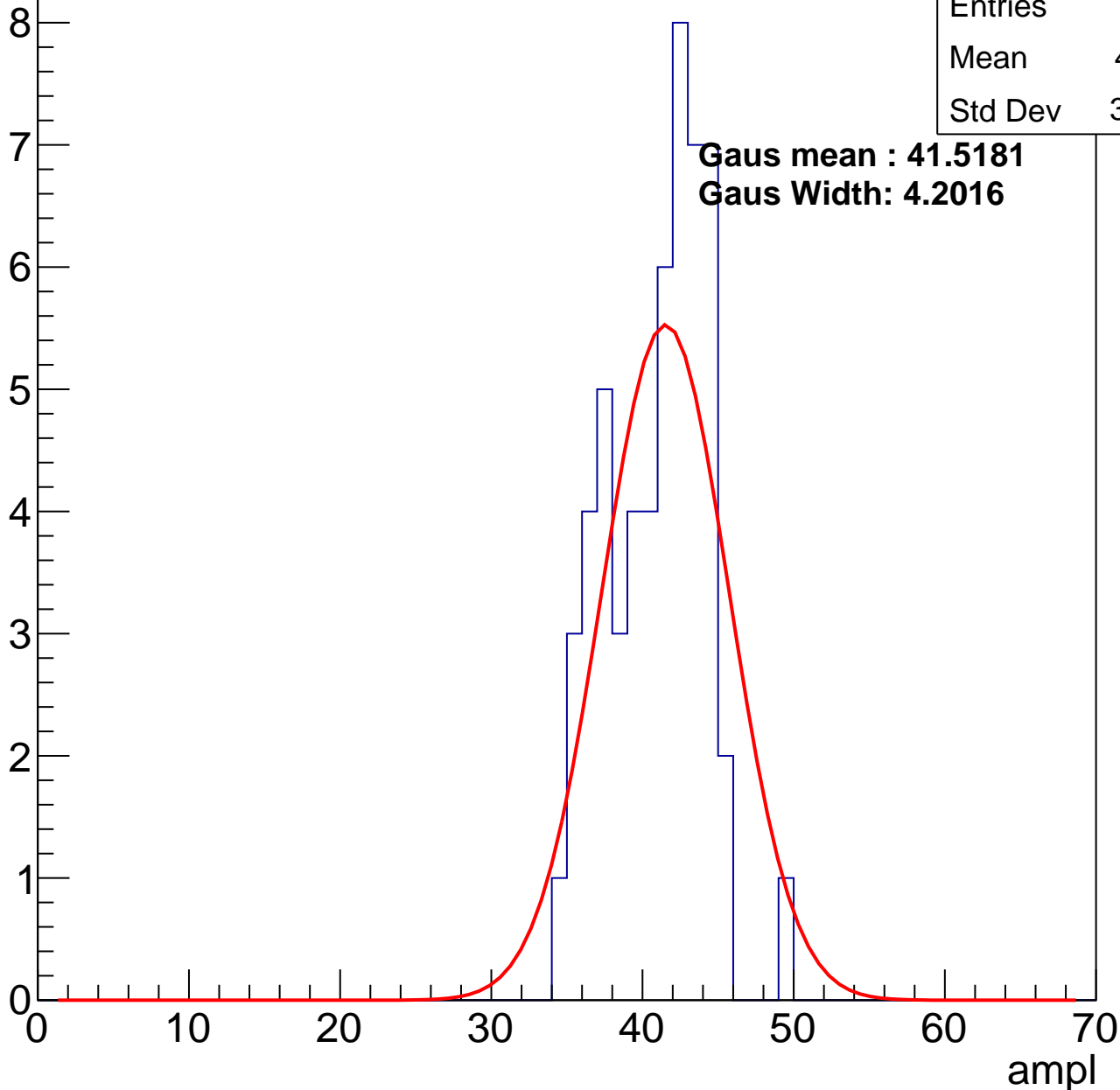
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	40.51
Std Dev	3.207

**Gaus mean : 41.5181**

**Gaus Width: 4.2016**

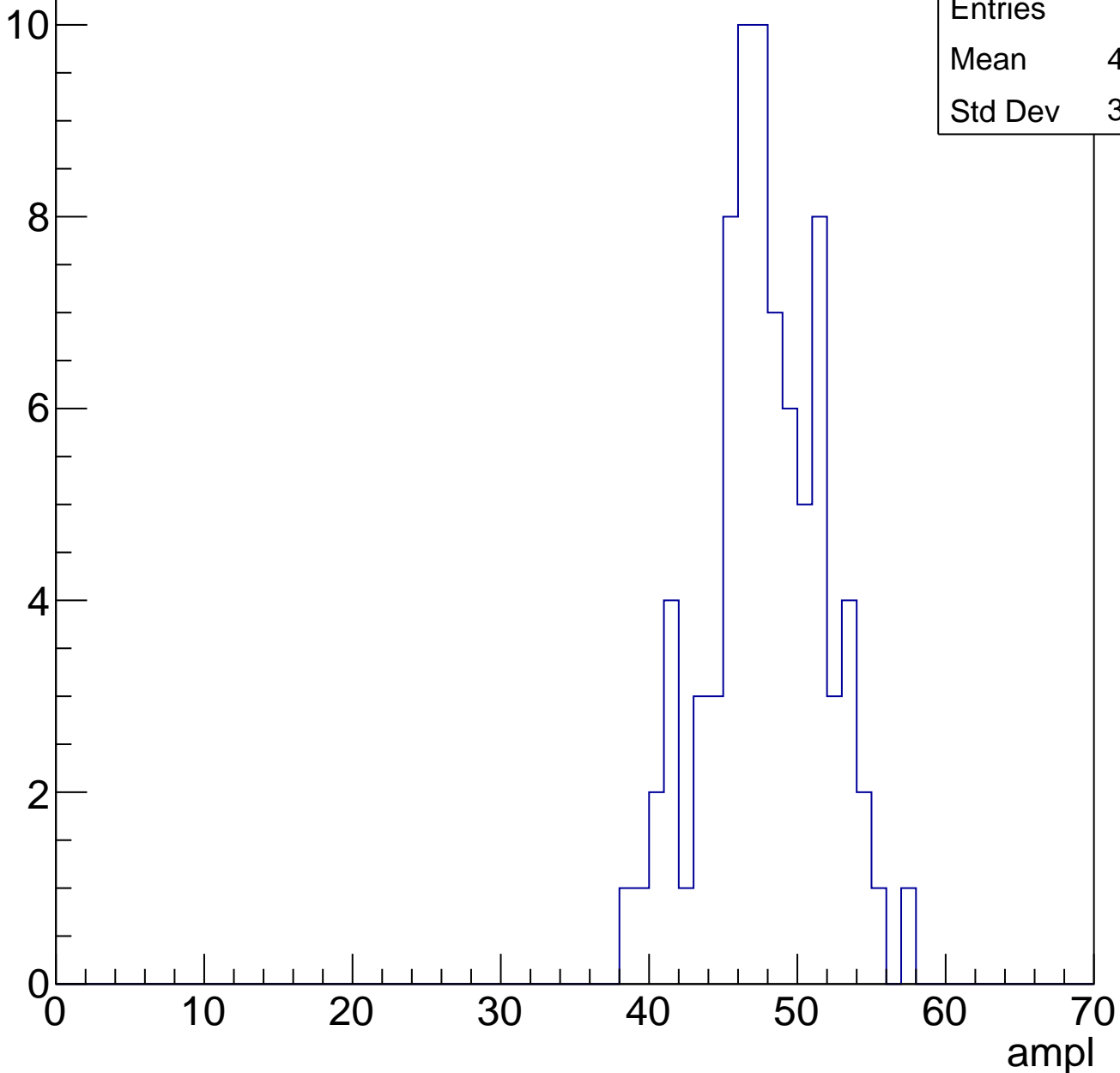


# B1L102S, U20-ch69, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	80
Mean	47.38
Std Dev	3.877

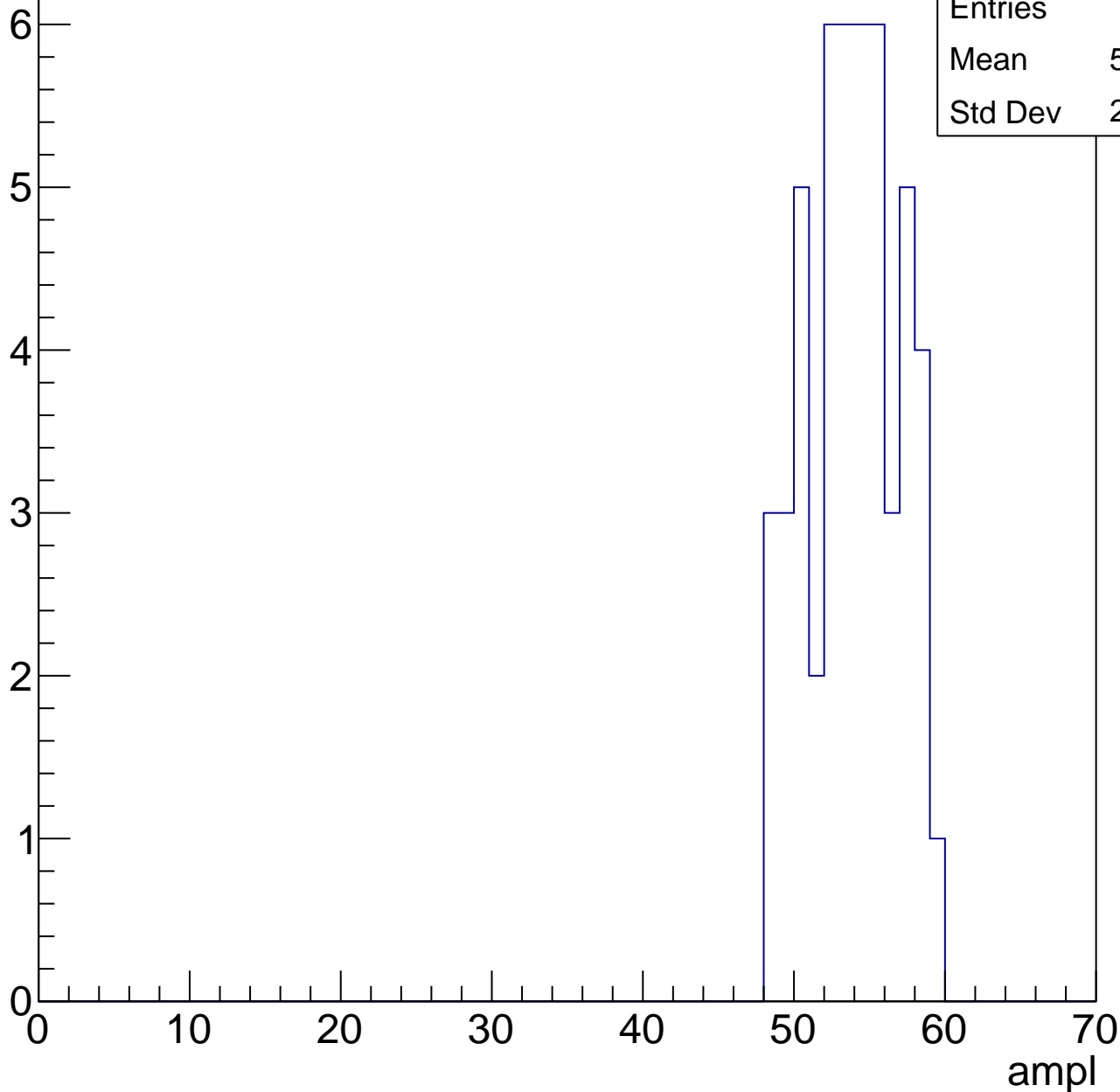


# B1L102S, U20-ch69, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

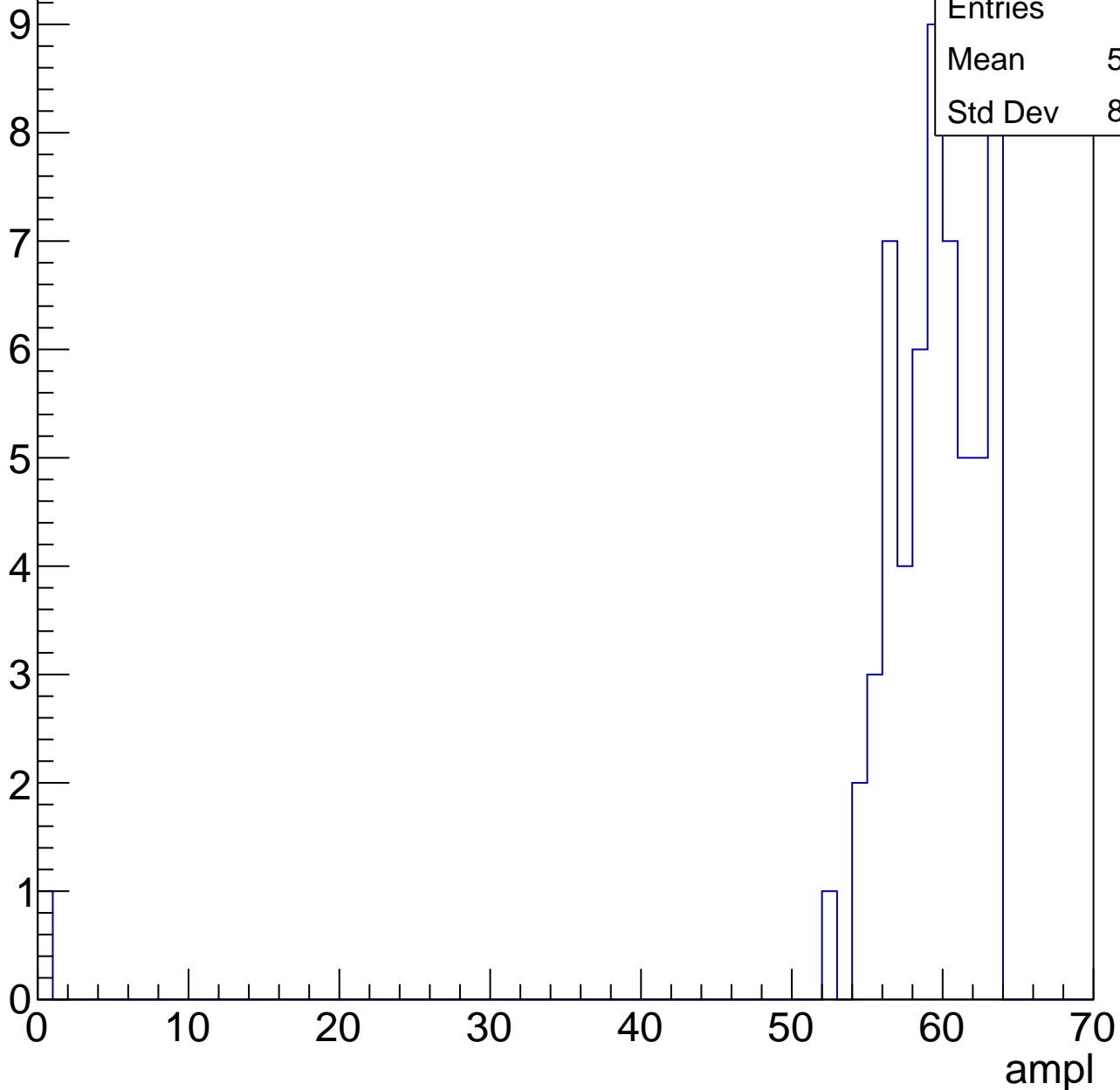
Entries	50
Mean	53.42
Std Dev	2.987



# B1L102S, U20-ch69, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

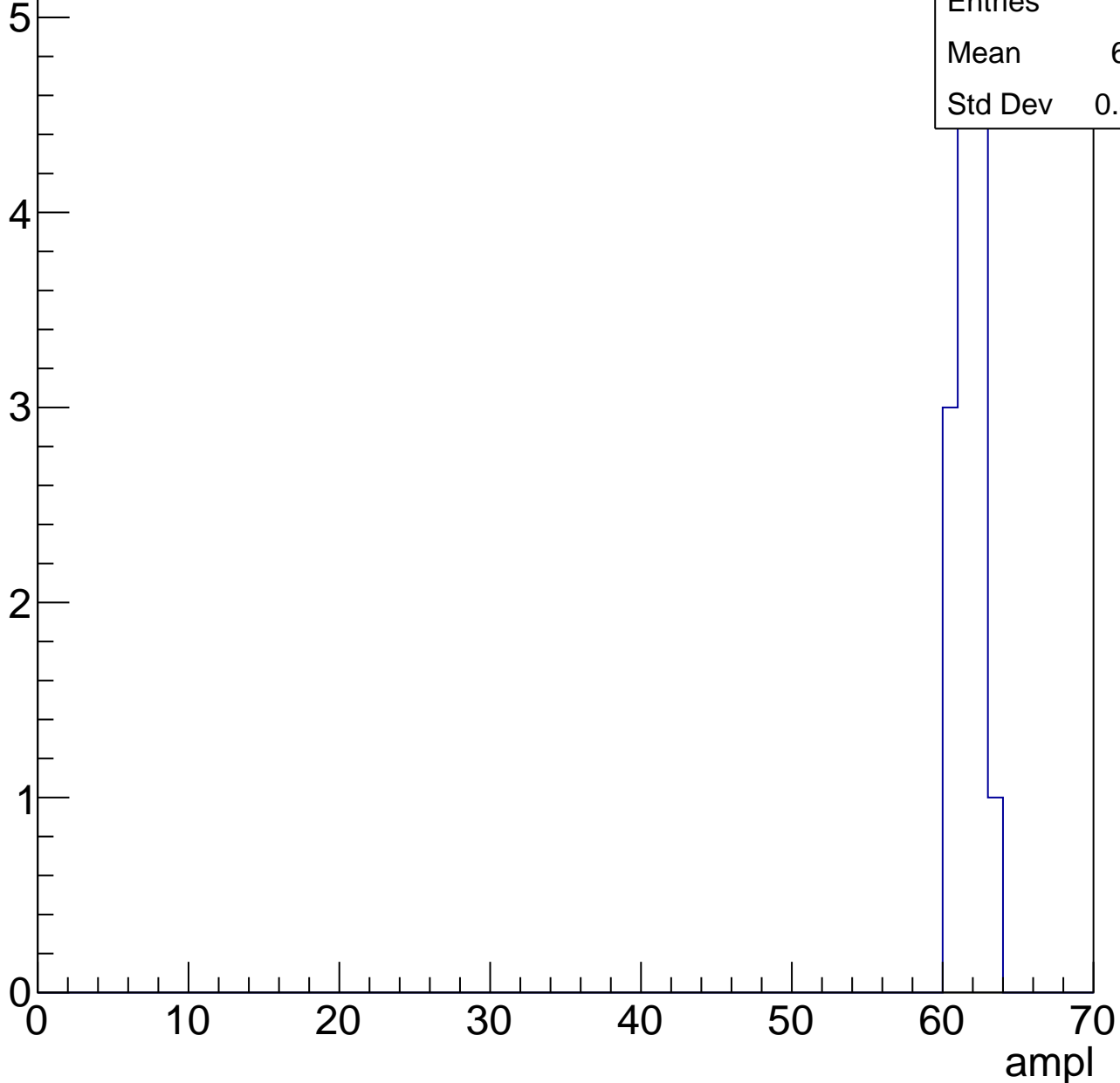


# B1L102S, U20-ch69, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	14
Mean	61.29
Std Dev	0.8806





# B1L102S, U20-ch69, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U20-ch70, adc0

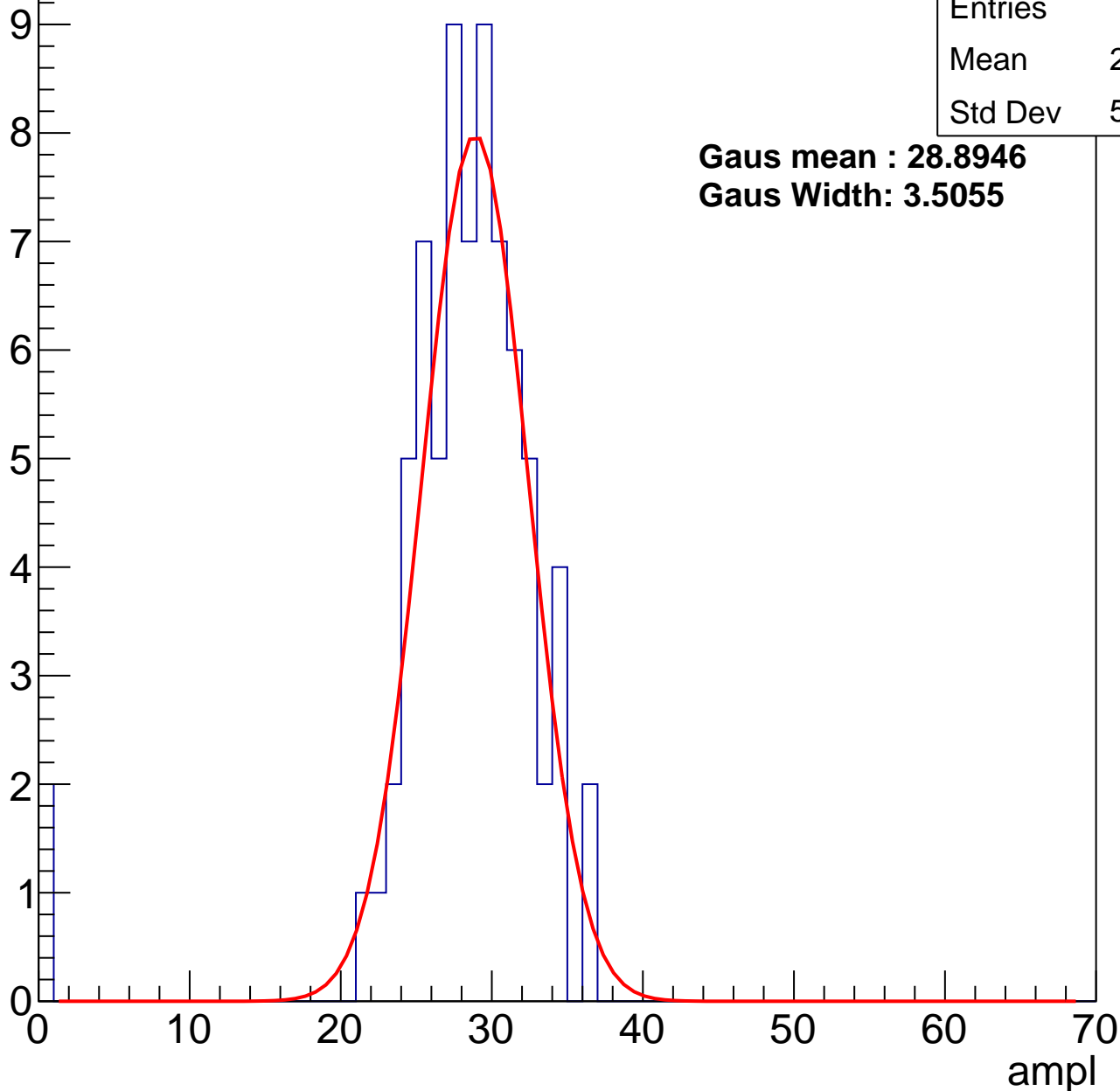
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	27.62
Std Dev	5.644

**Gaus mean : 28.8946**

**Gaus Width: 3.5055**



# B1L102S, U20-ch70, adc1

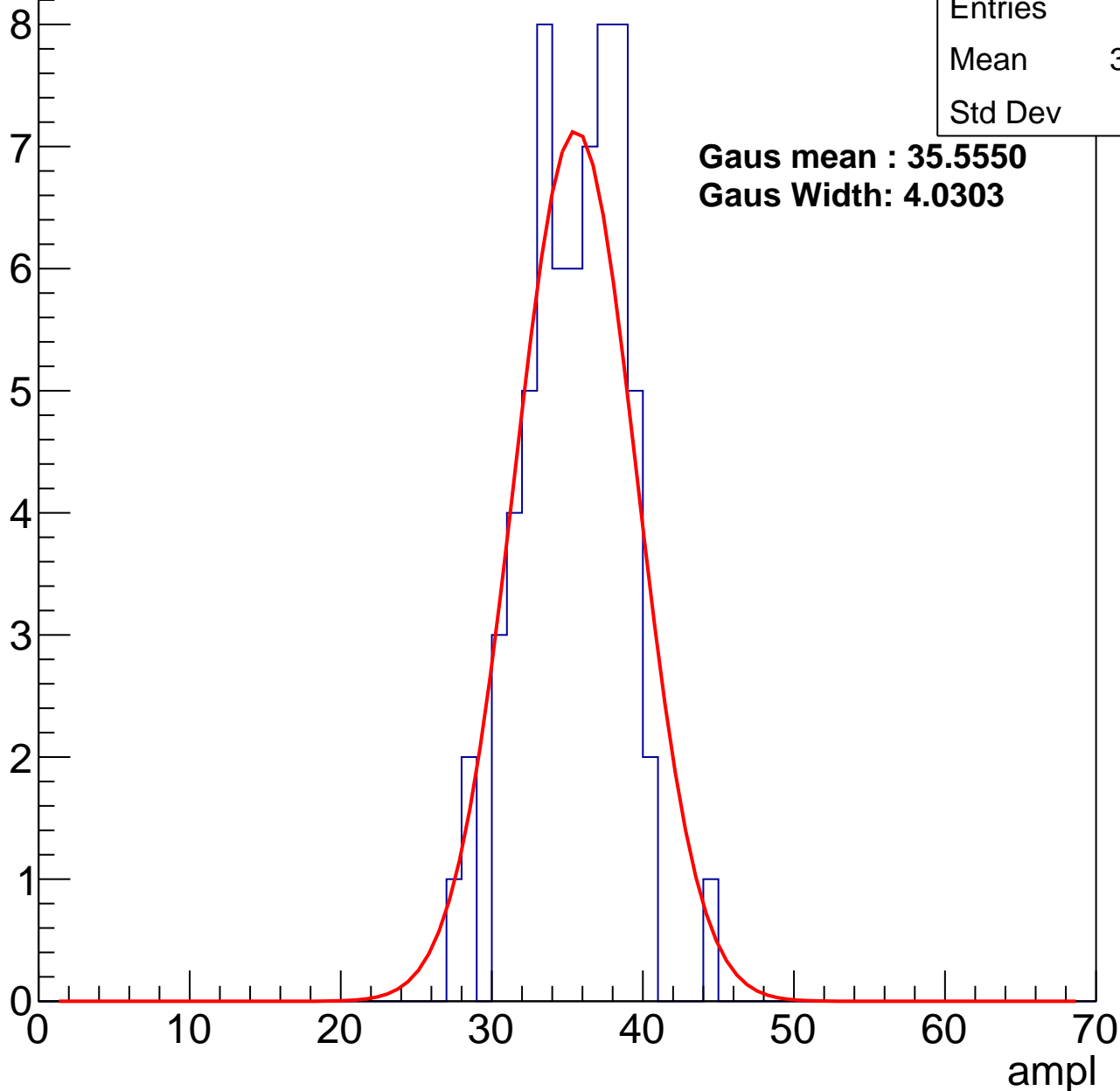
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	34.94
Std Dev	3.27

**Gaus mean : 35.5550**

**Gaus Width: 4.0303**



# B1L102S, U20-ch70, adc2

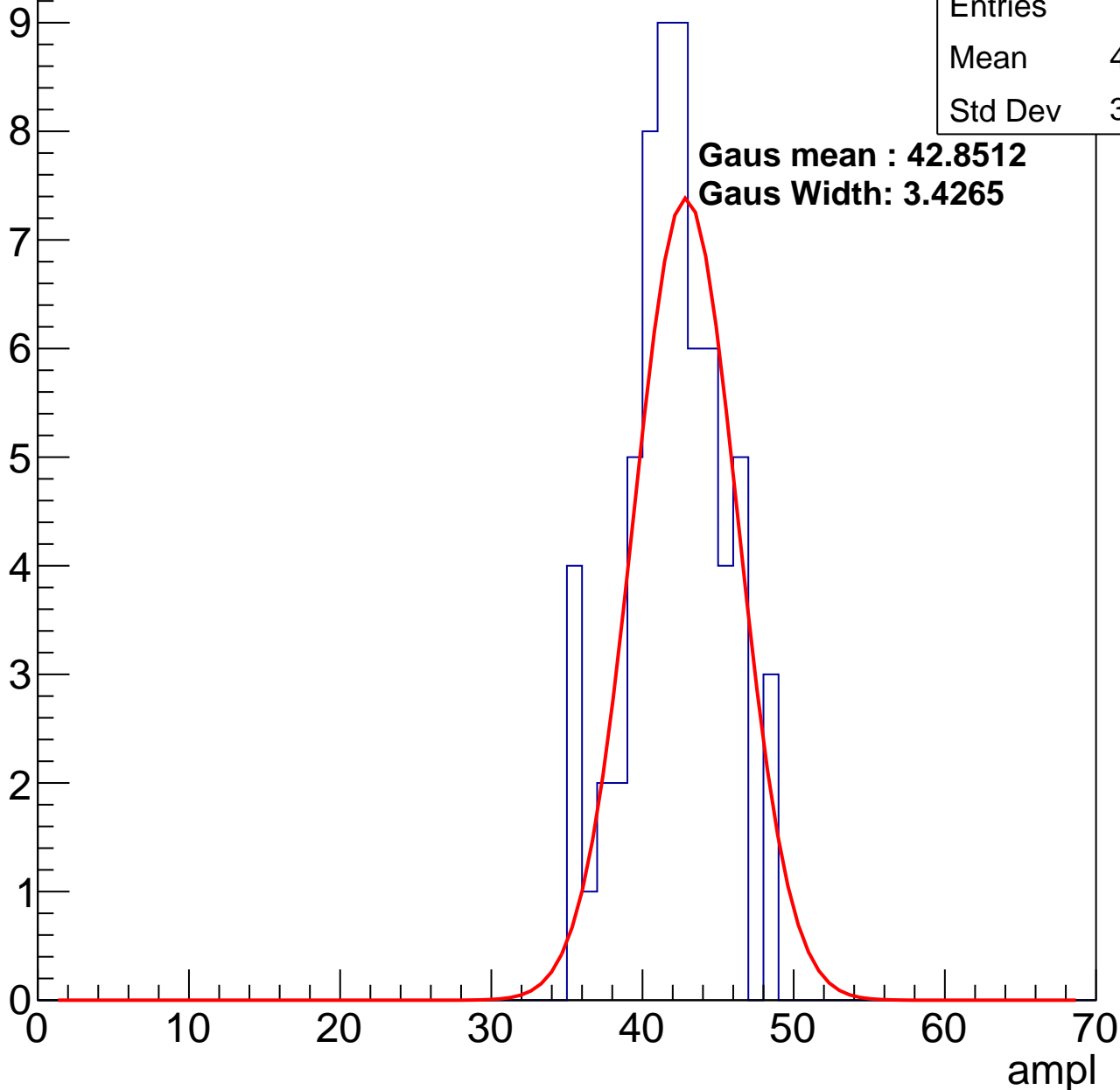
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	41.62
Std Dev	3.175

**Gaus mean : 42.8512**

**Gaus Width: 3.4265**

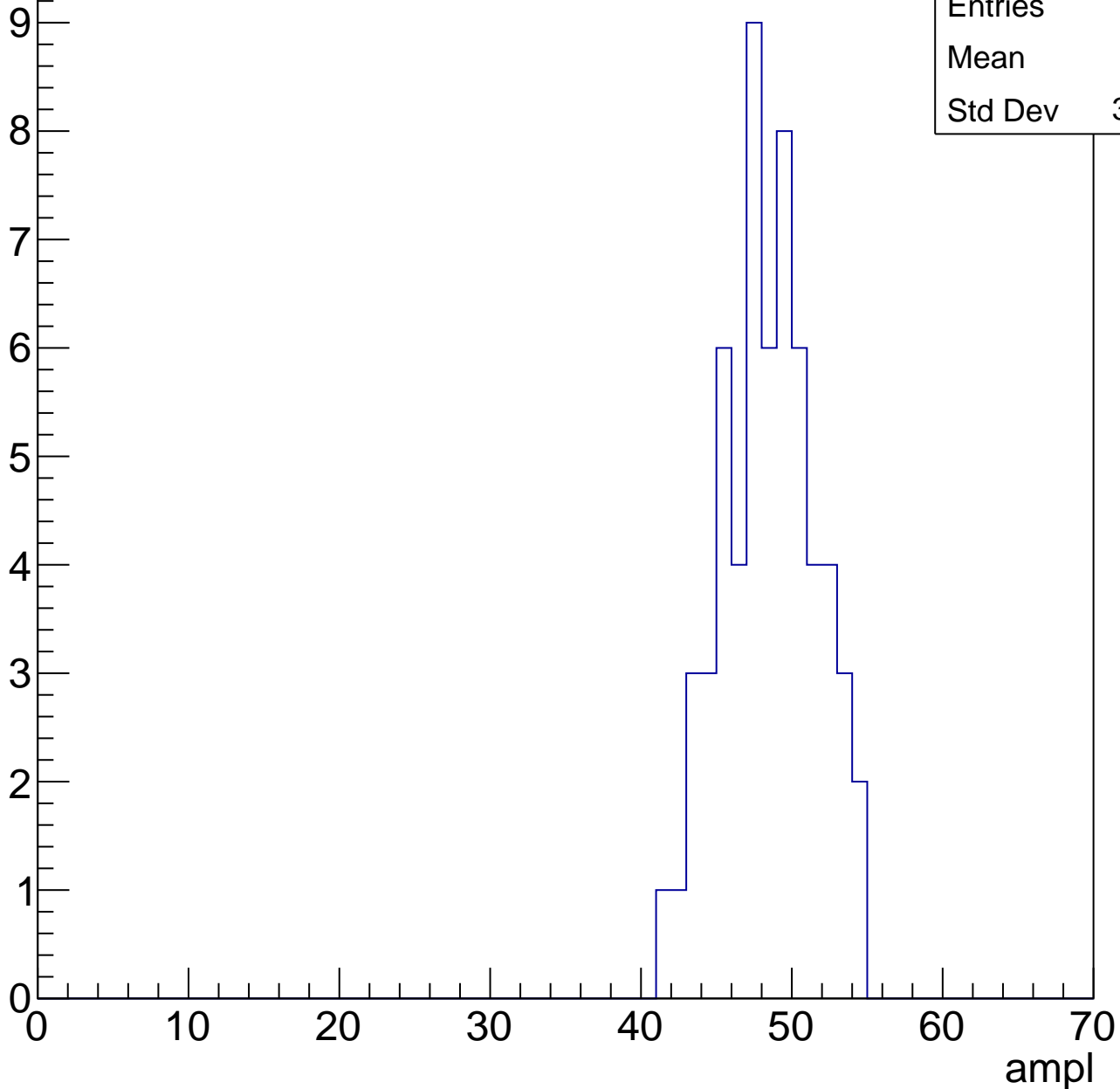


# B1L102S, U20-ch70, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	48
Std Dev	3.071

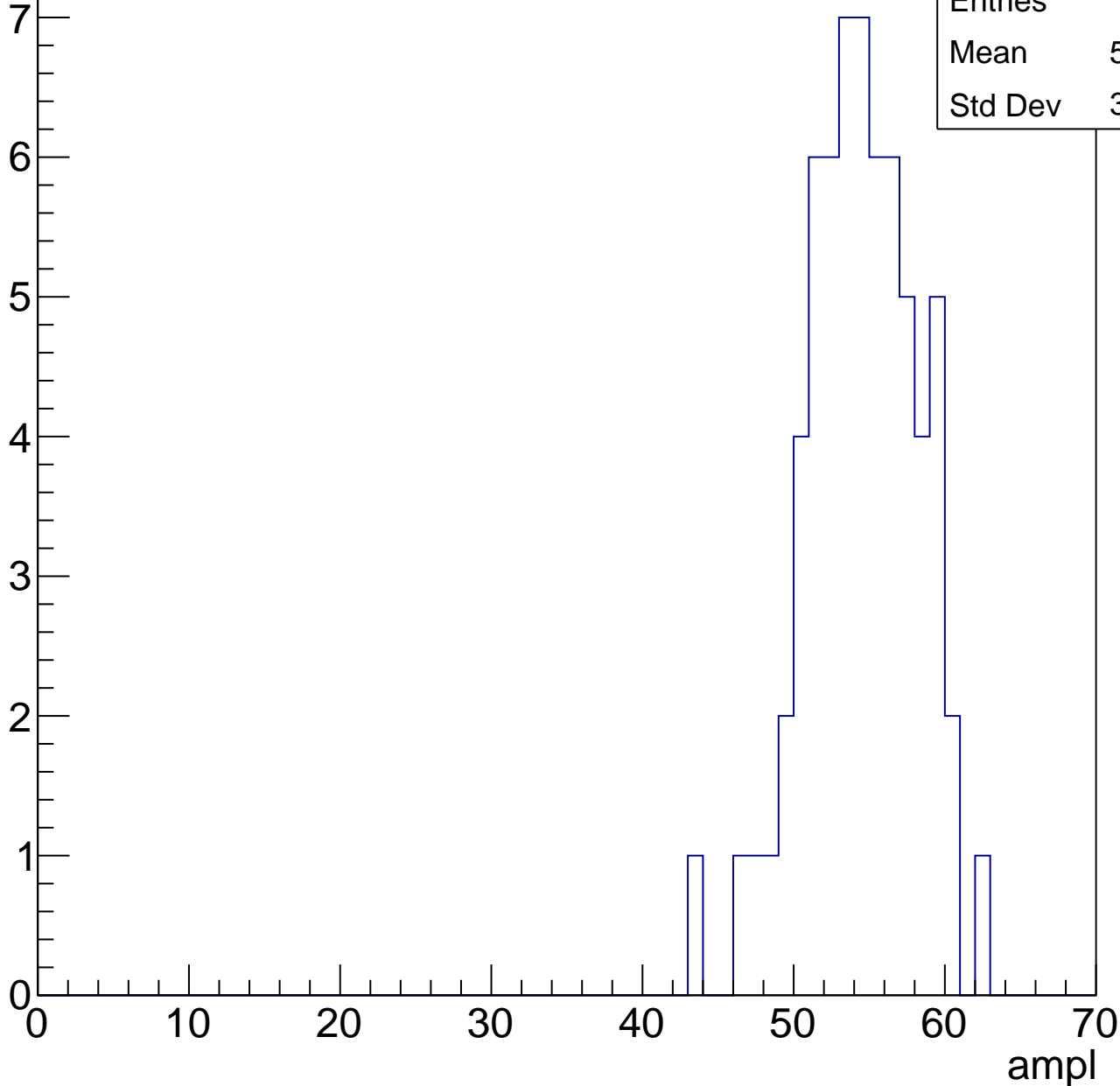


# B1L102S, U20-ch70, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	53.98
Std Dev	3.656

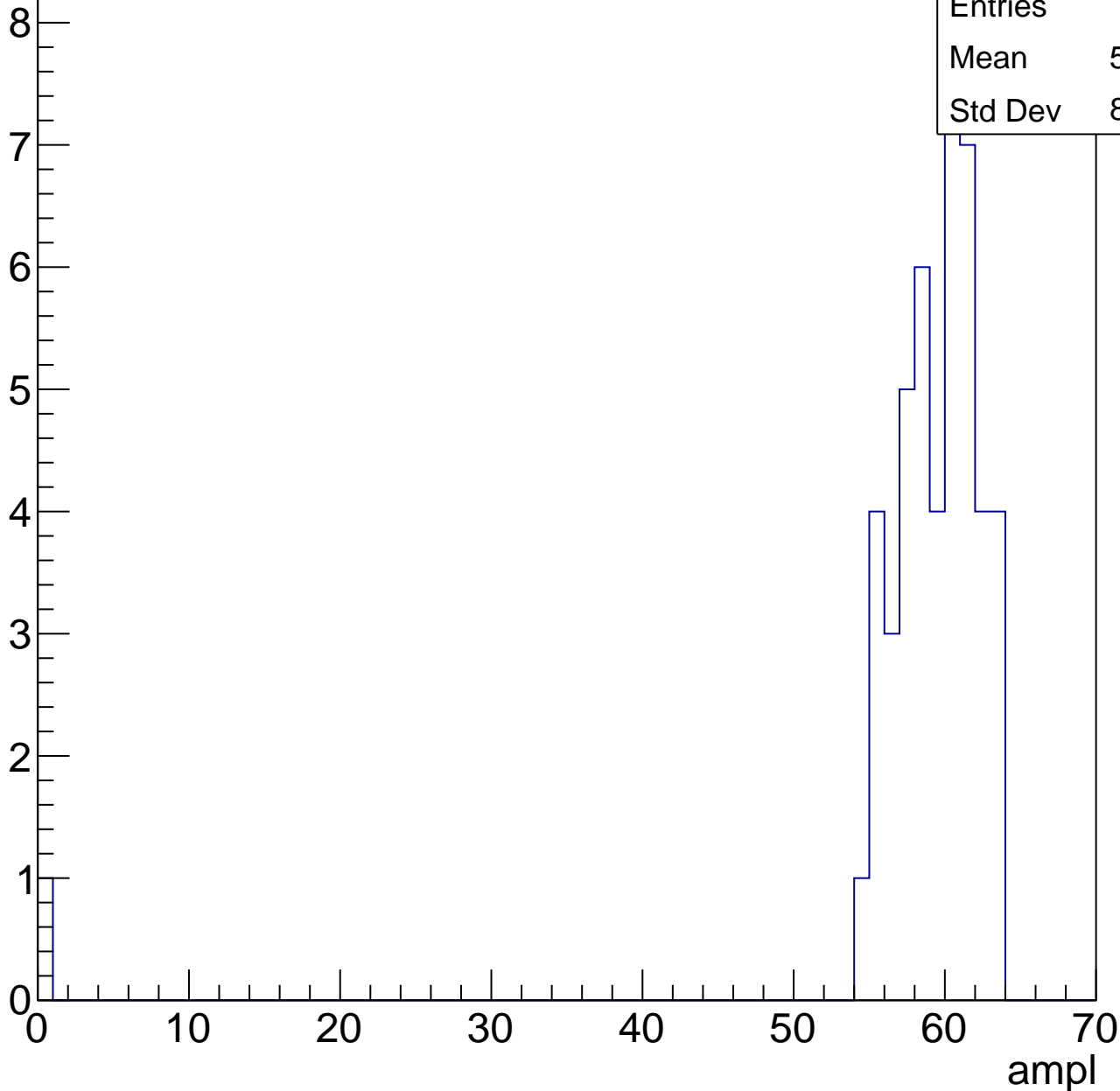


# B1L102S, U20-ch70, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	47
Mean	57.83
Std Dev	8.866

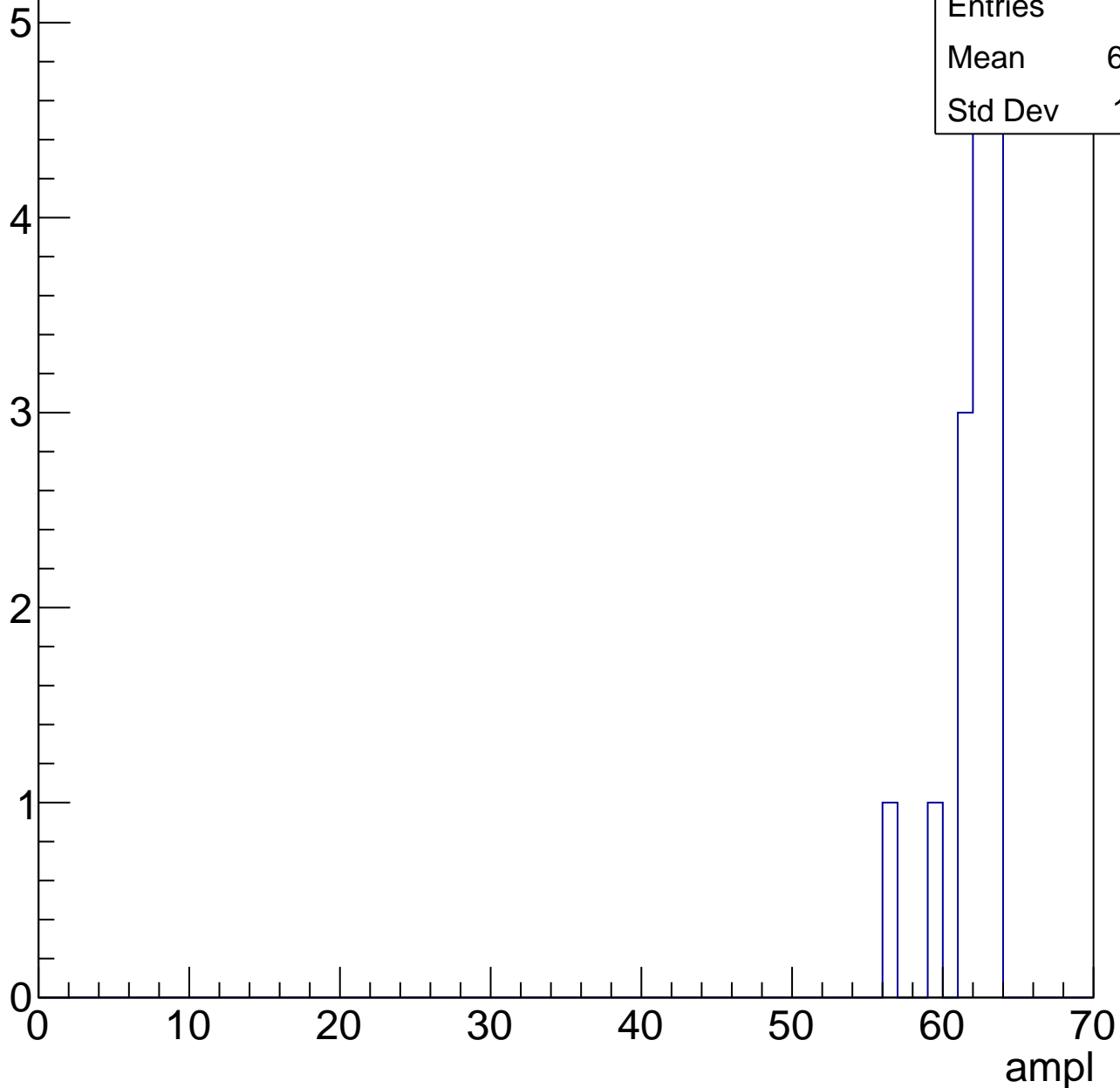


# B1L102S, U20-ch70, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	15
Mean	61.53
Std Dev	1.821





# B1L102S, U20-ch70, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch71, adc0

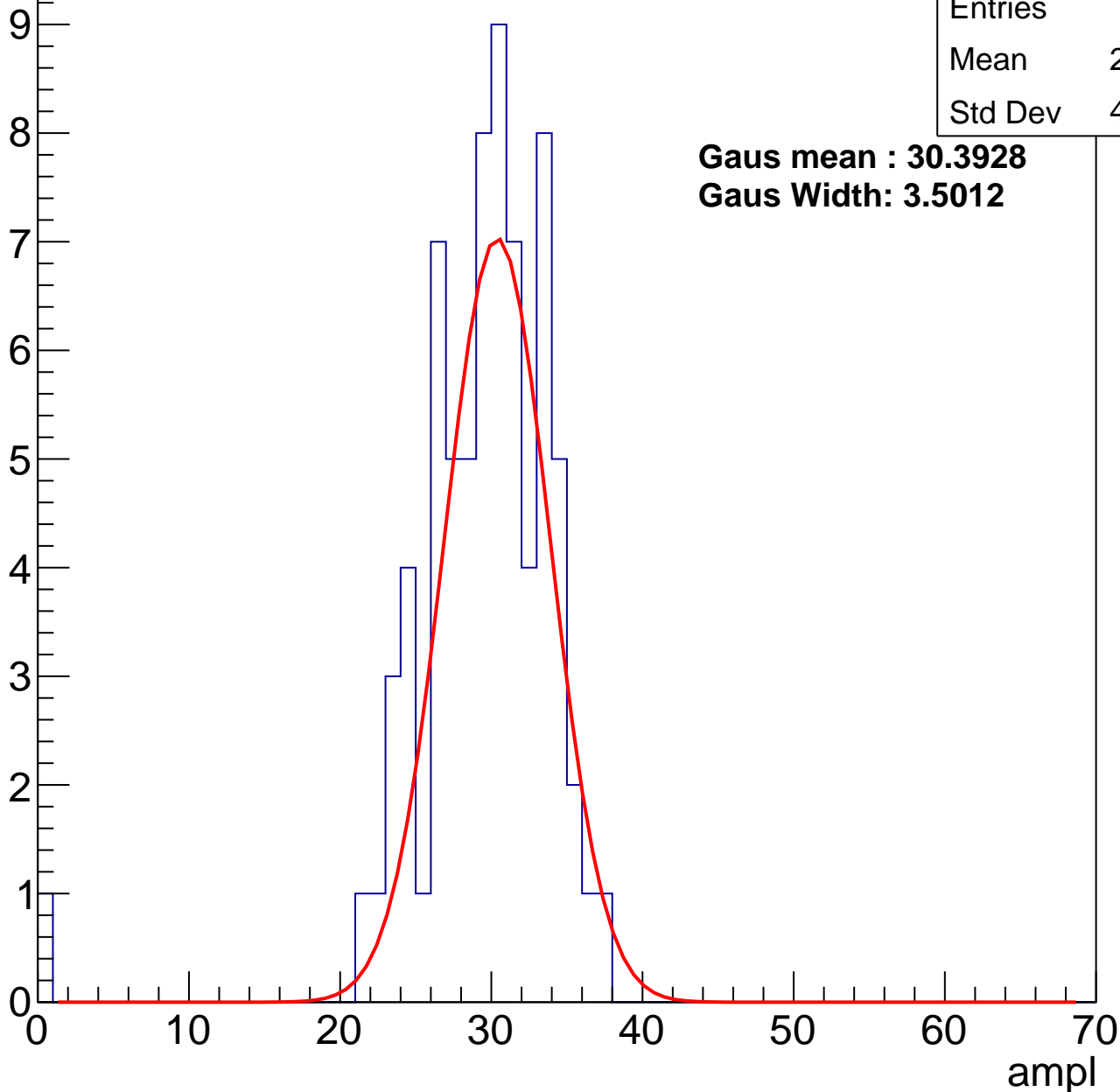
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	28.96
Std Dev	4.934

**Gaus mean : 30.3928**

**Gaus Width: 3.5012**



# B1L102S, U20-ch71, adc1

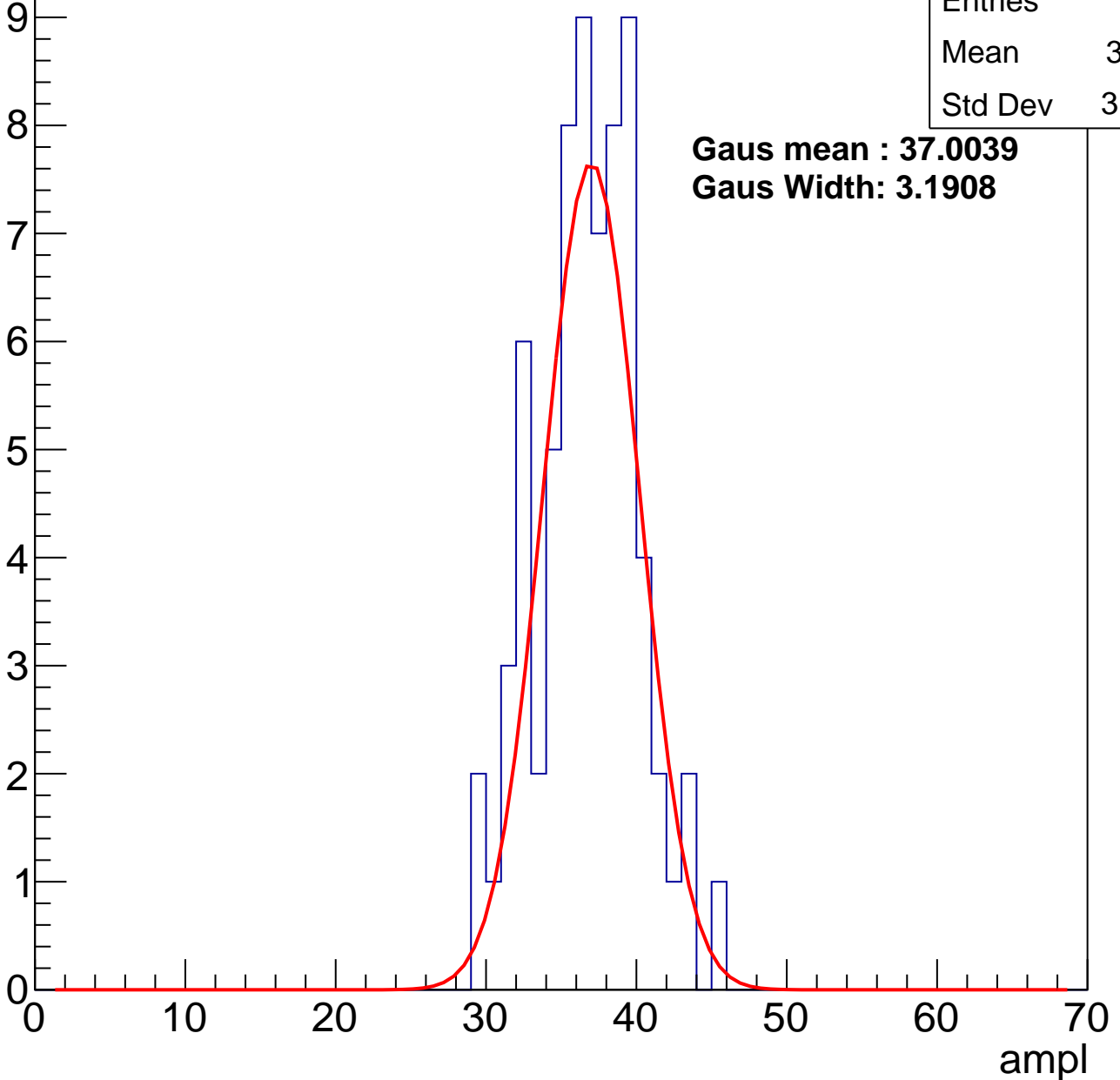
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	36.31
Std Dev	3.366

**Gaus mean : 37.0039**

**Gaus Width: 3.1908**



# B1L102S, U20-ch71, adc2

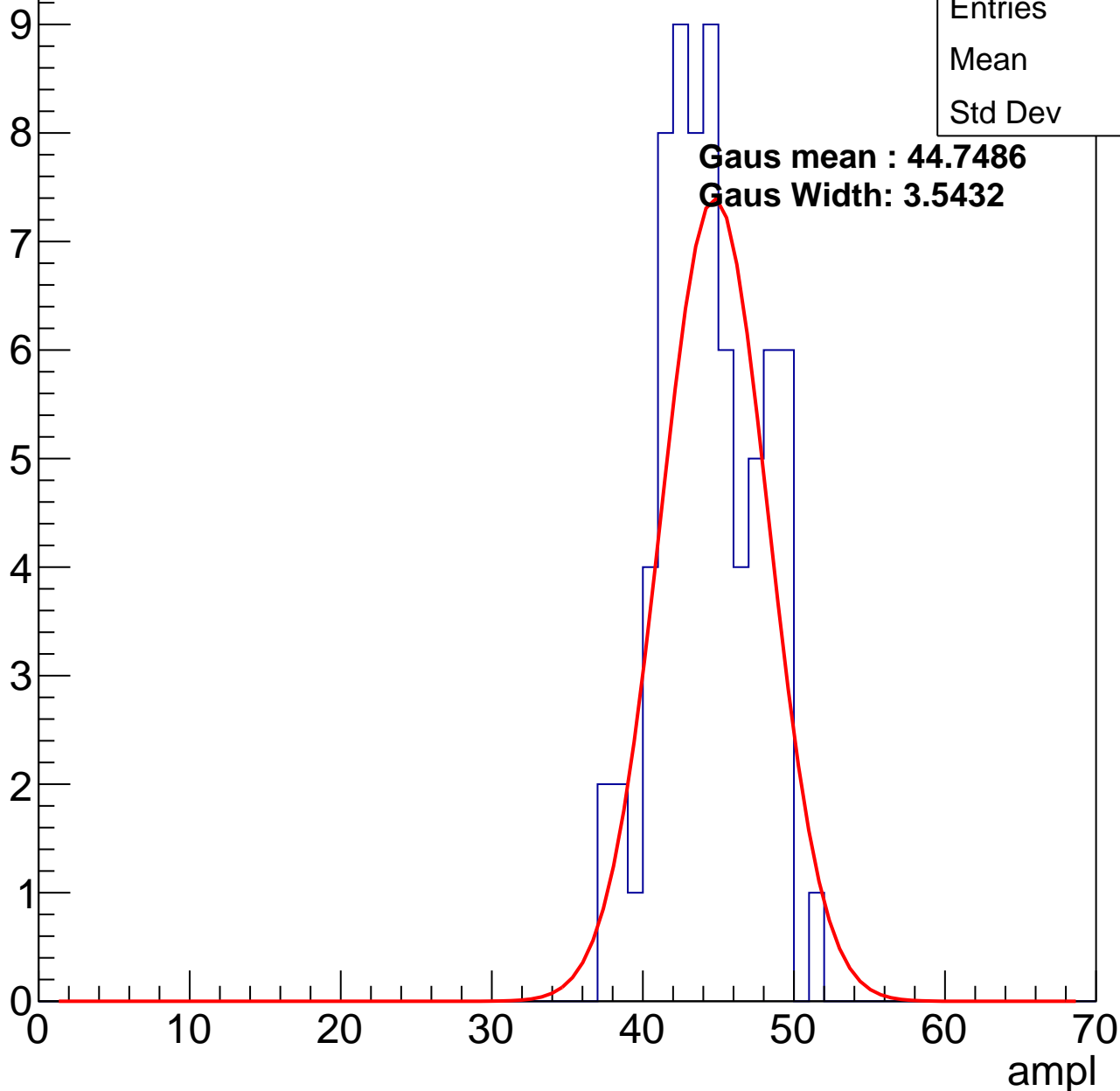
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	43.9
Std Dev	3.22

**Gaus mean : 44.7486**

**Gaus Width: 3.5432**

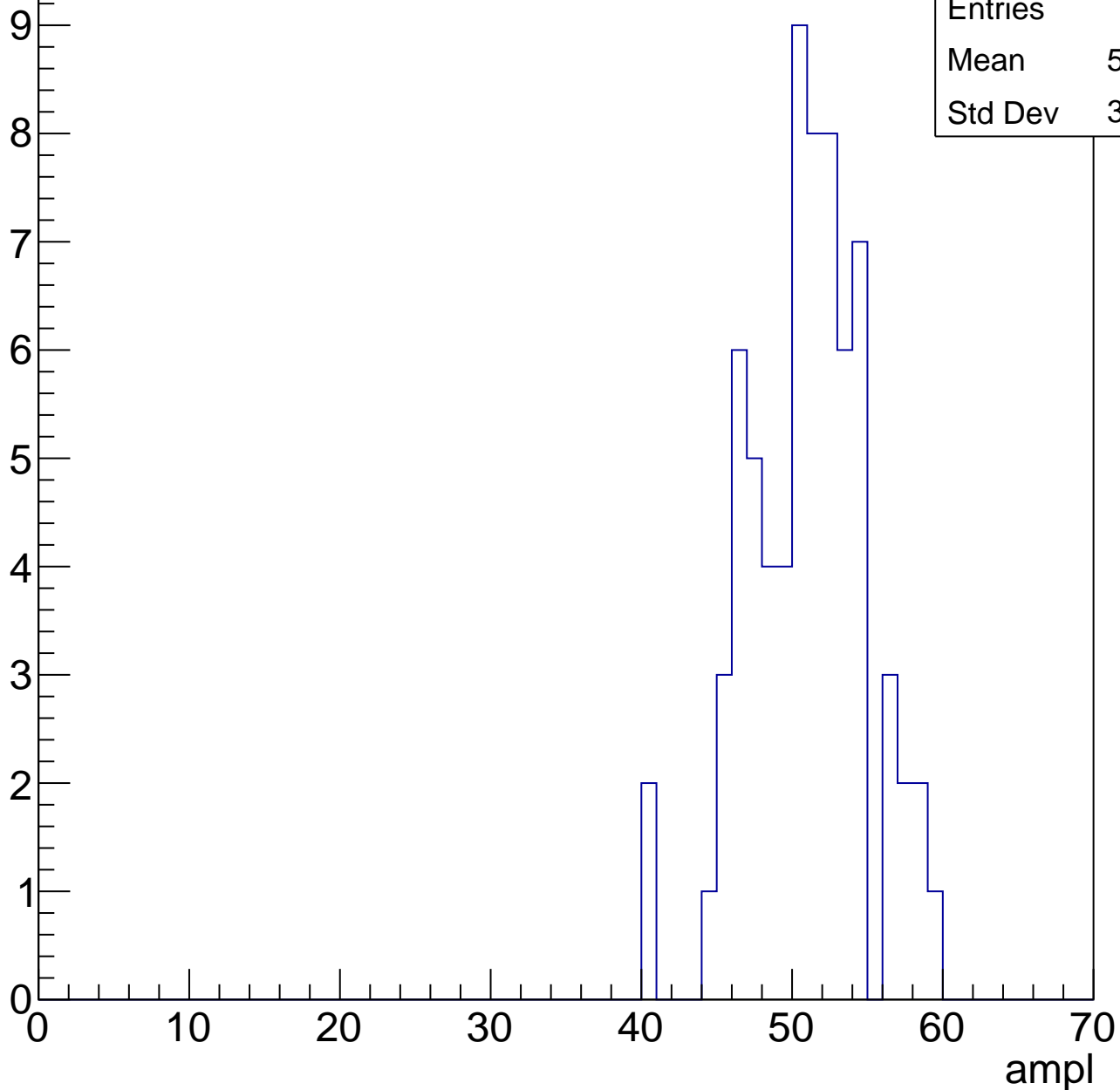


# B1L102S, U20-ch71, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	50.49
Std Dev	3.892

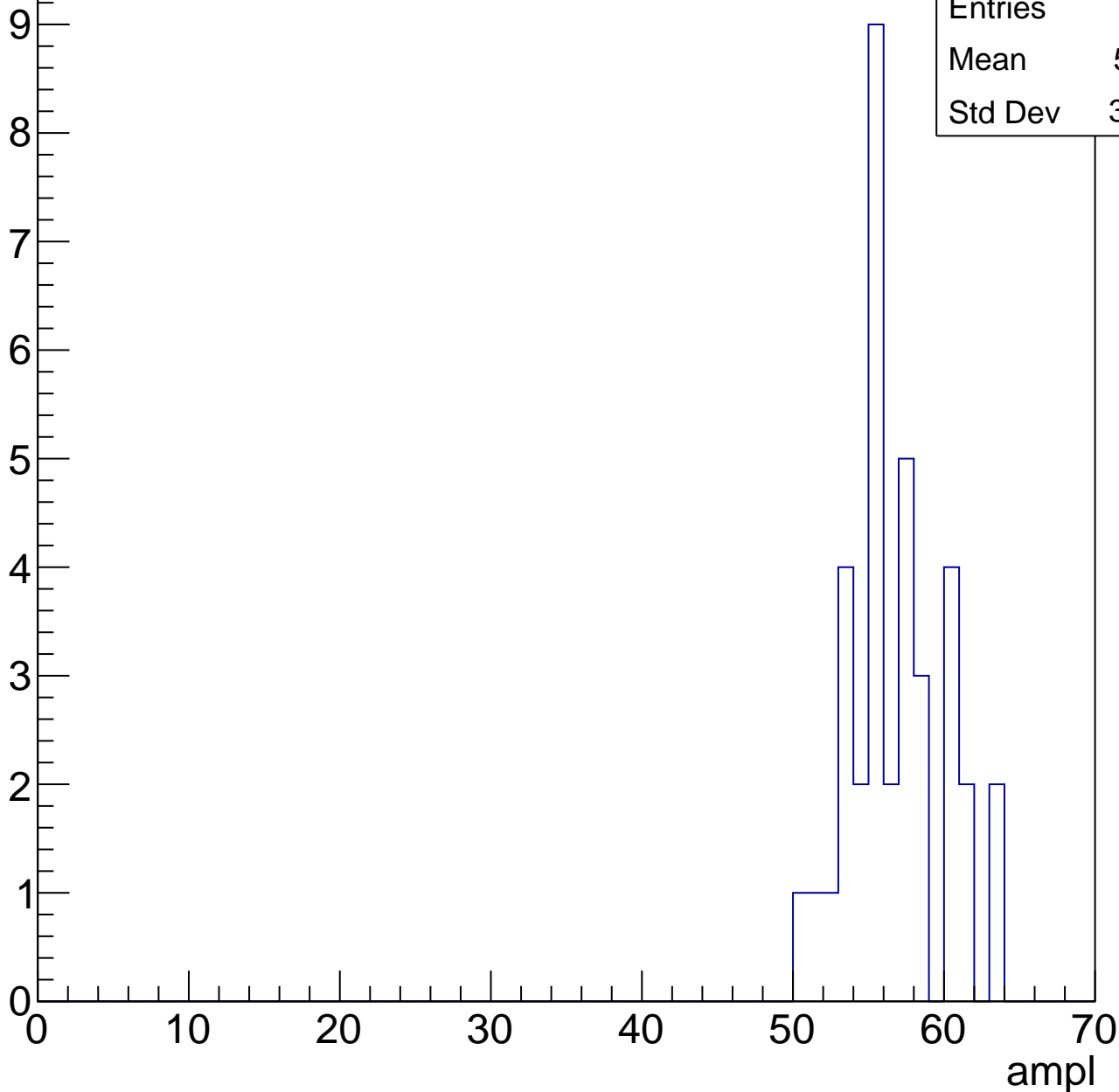


# B1L102S, U20-ch71, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

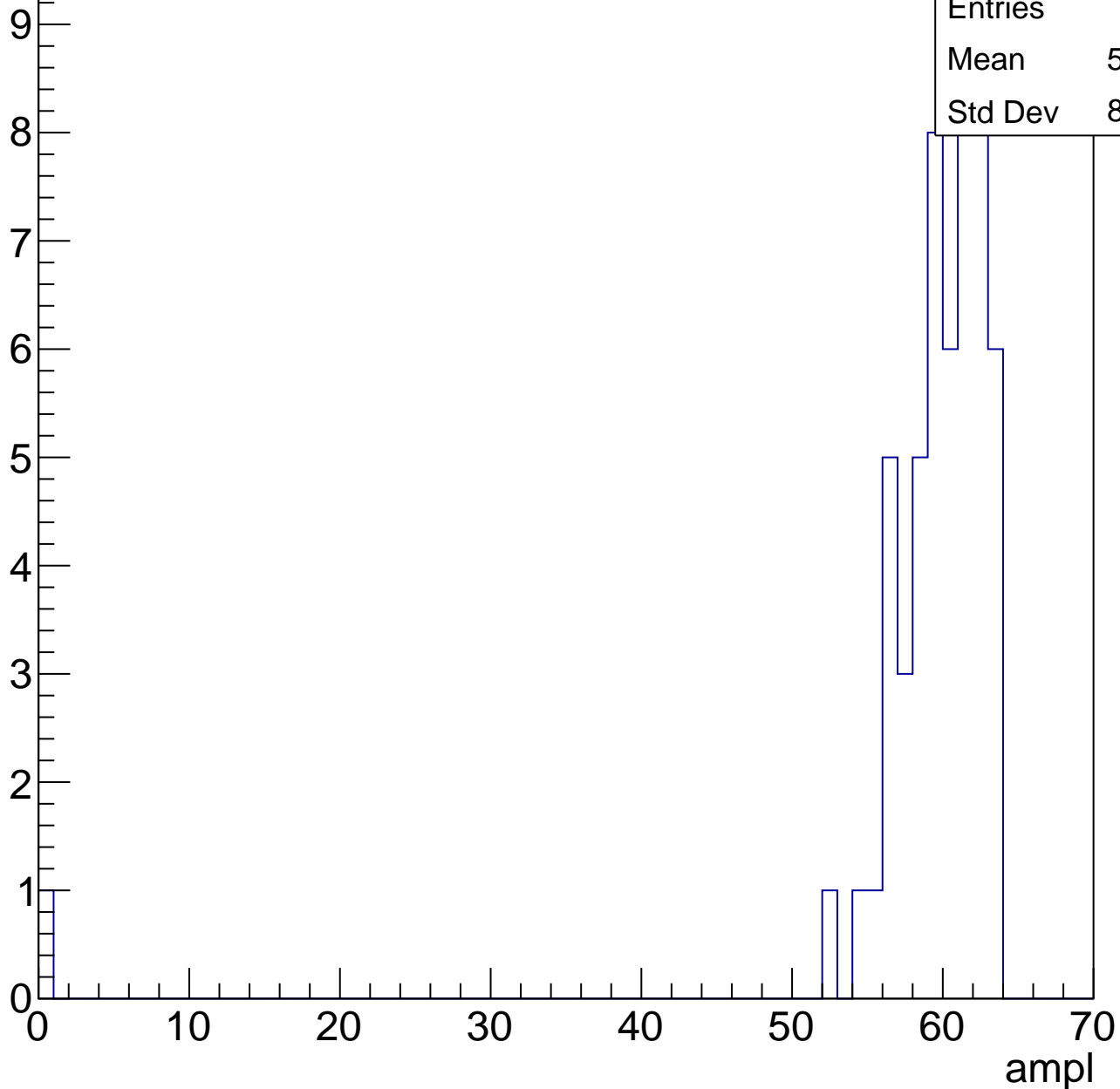
Entries	36
Mean	56.31
Std Dev	3.143



# B1L102S, U20-ch71, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch71, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U20-ch71, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L102S, U20-ch72, adc0

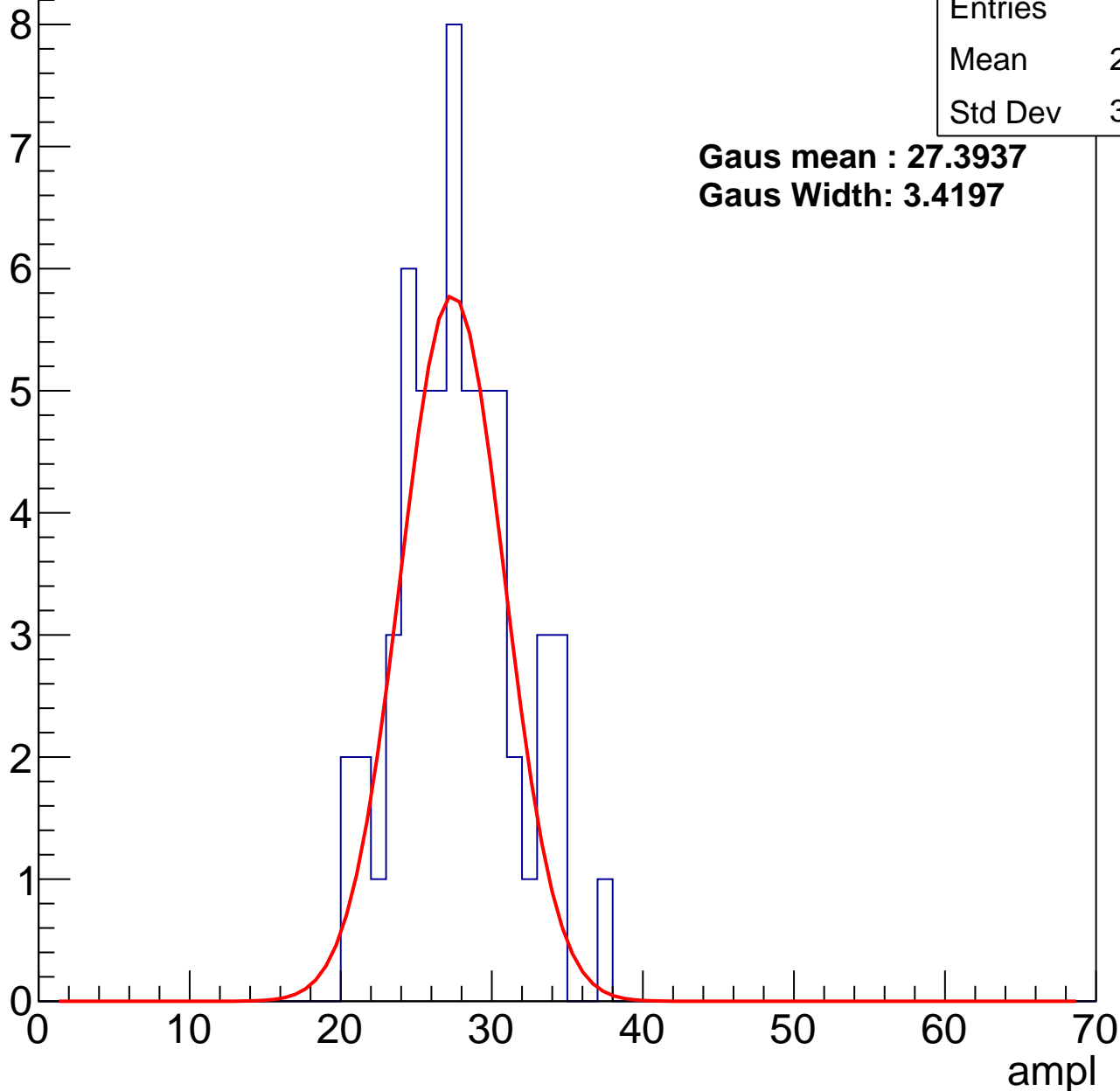
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	27.28
Std Dev	3.745

**Gaus mean : 27.3937**

**Gaus Width: 3.4197**



# B1L102S, U20-ch72, adc1

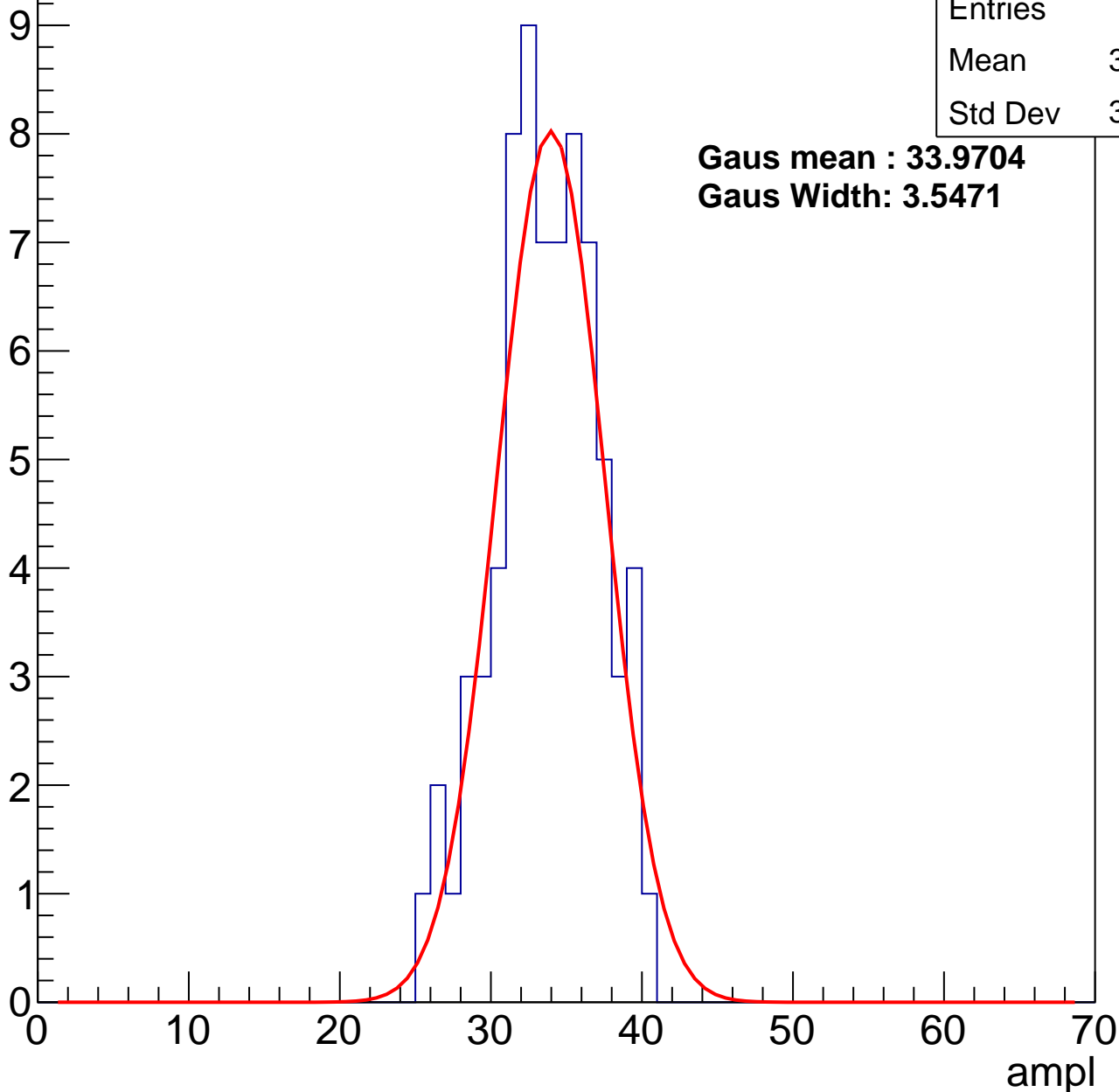
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	33.25
Std Dev	3.399

**Gaus mean : 33.9704**

**Gaus Width: 3.5471**



# B1L102S, U20-ch72, adc2

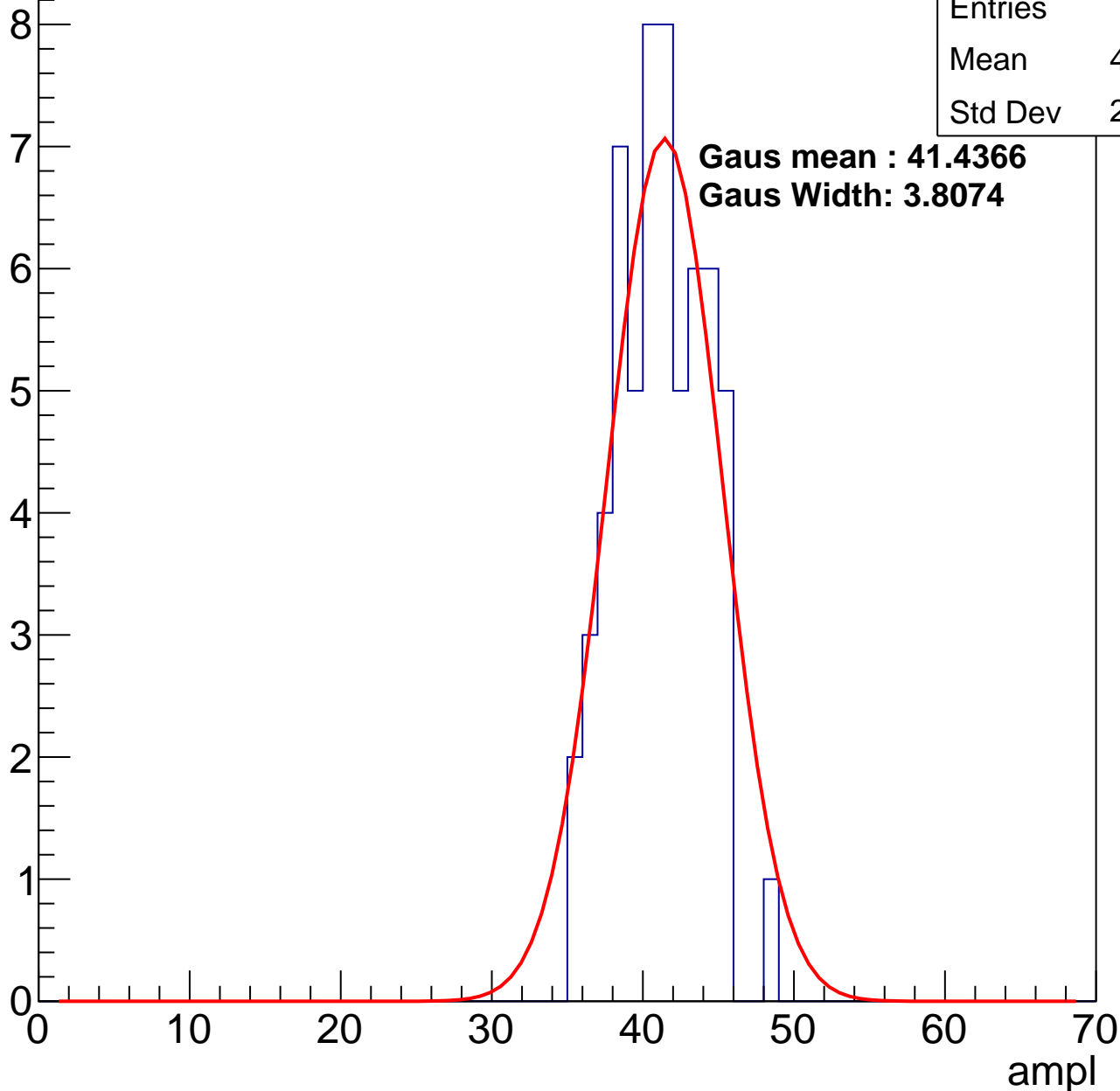
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	40.67
Std Dev	2.908

**Gaus mean : 41.4366**

**Gaus Width: 3.8074**

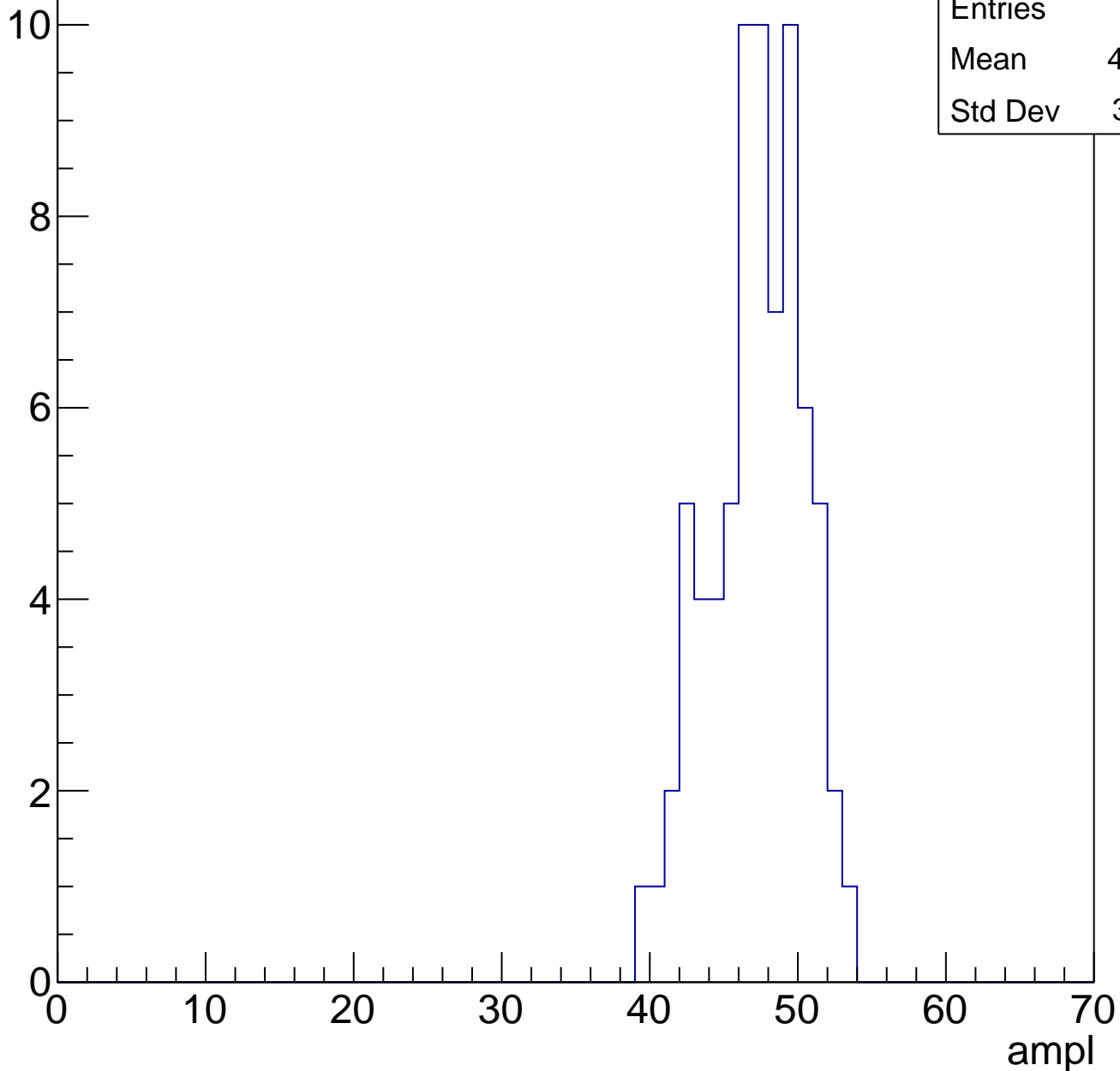


# B1L102S, U20-ch72, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	73
Mean	46.74
Std Dev	3.101

Entry

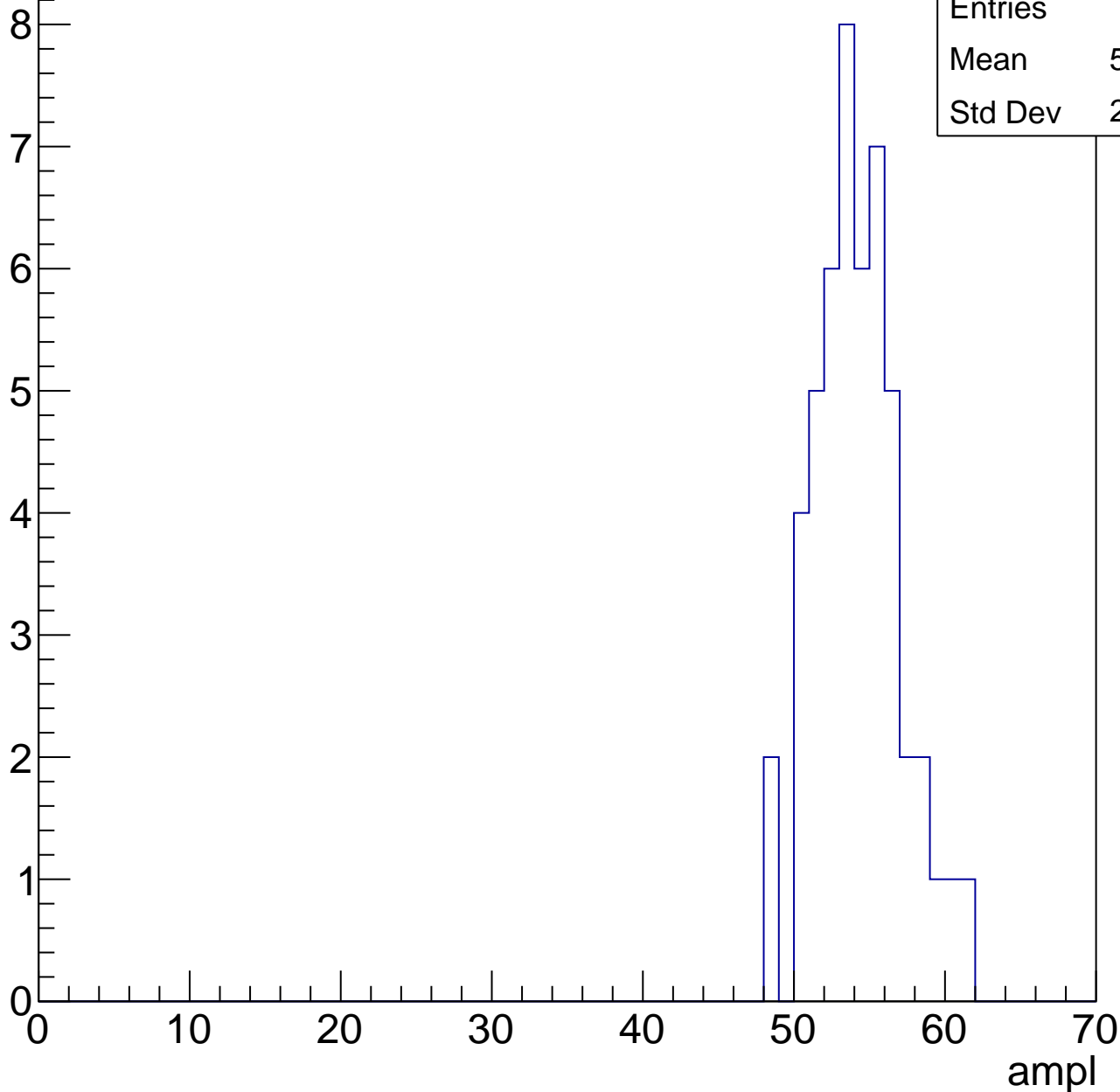


# B1L102S, U20-ch72, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

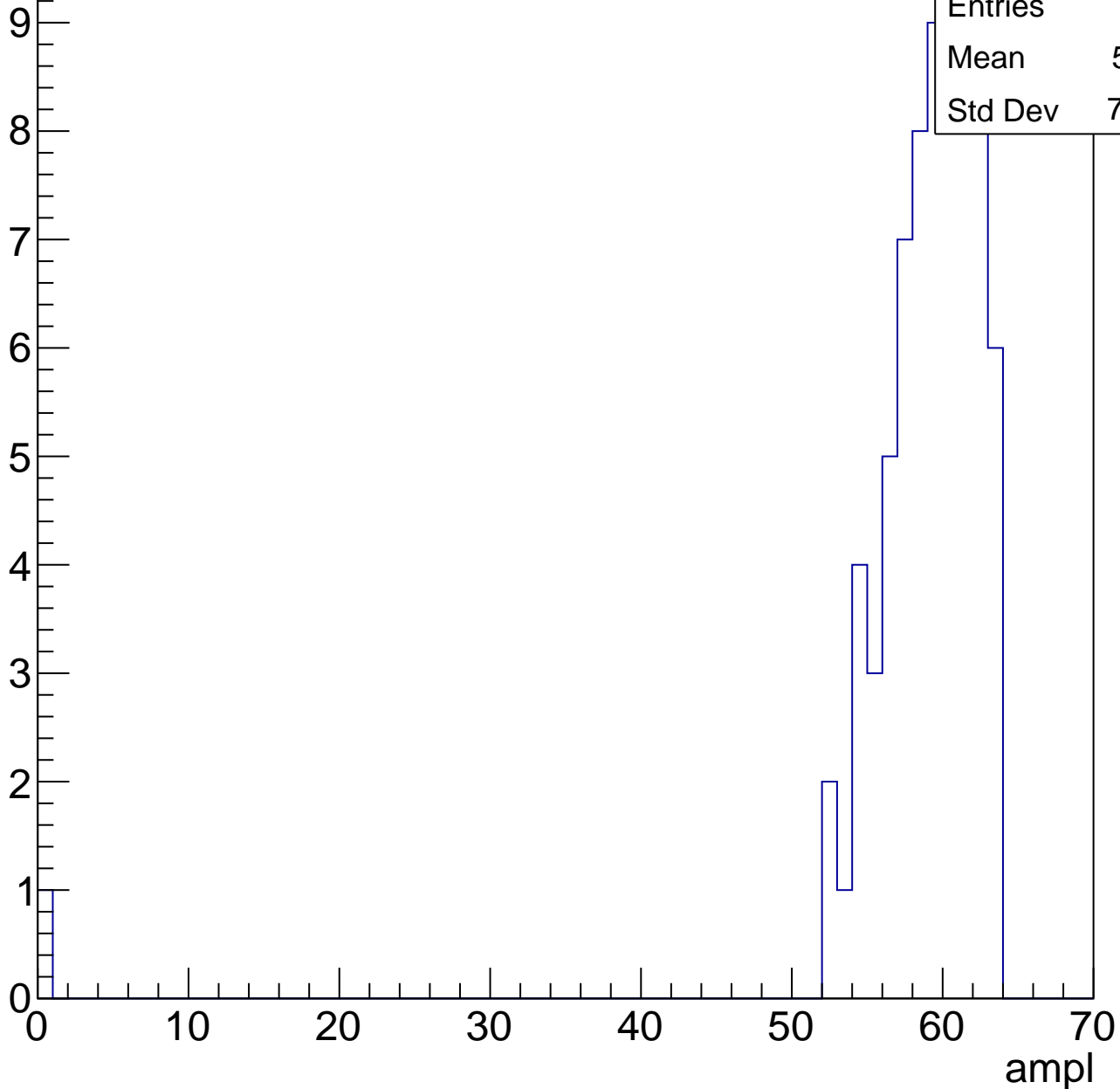
Entries	50
Mean	53.72
Std Dev	2.815



# B1L102S, U20-ch72, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

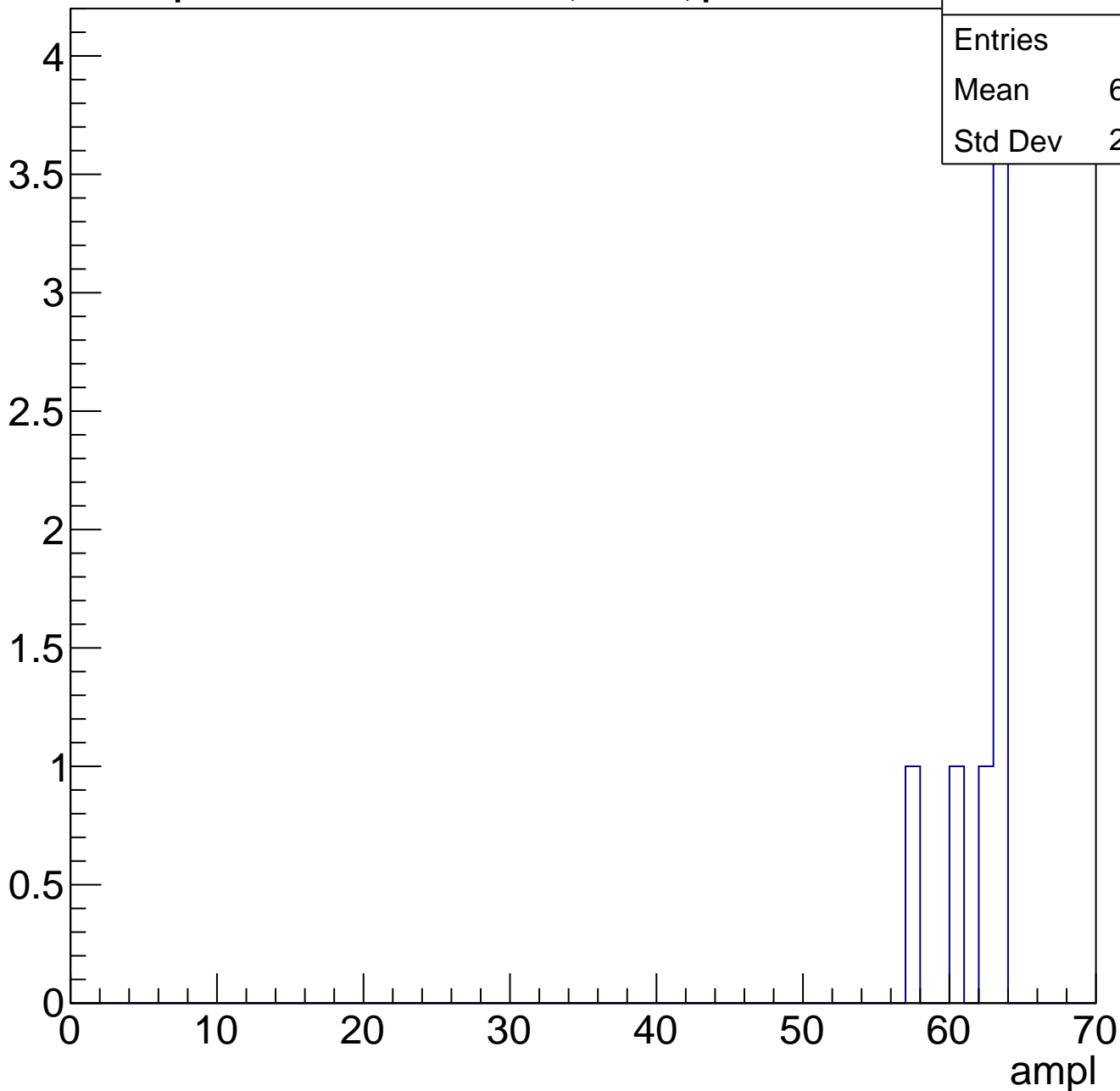


Entries	72
Mean	58.01
Std Dev	7.449

# B1L102S, U20-ch72, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U20-ch72, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L102S, U20-ch73, adc0

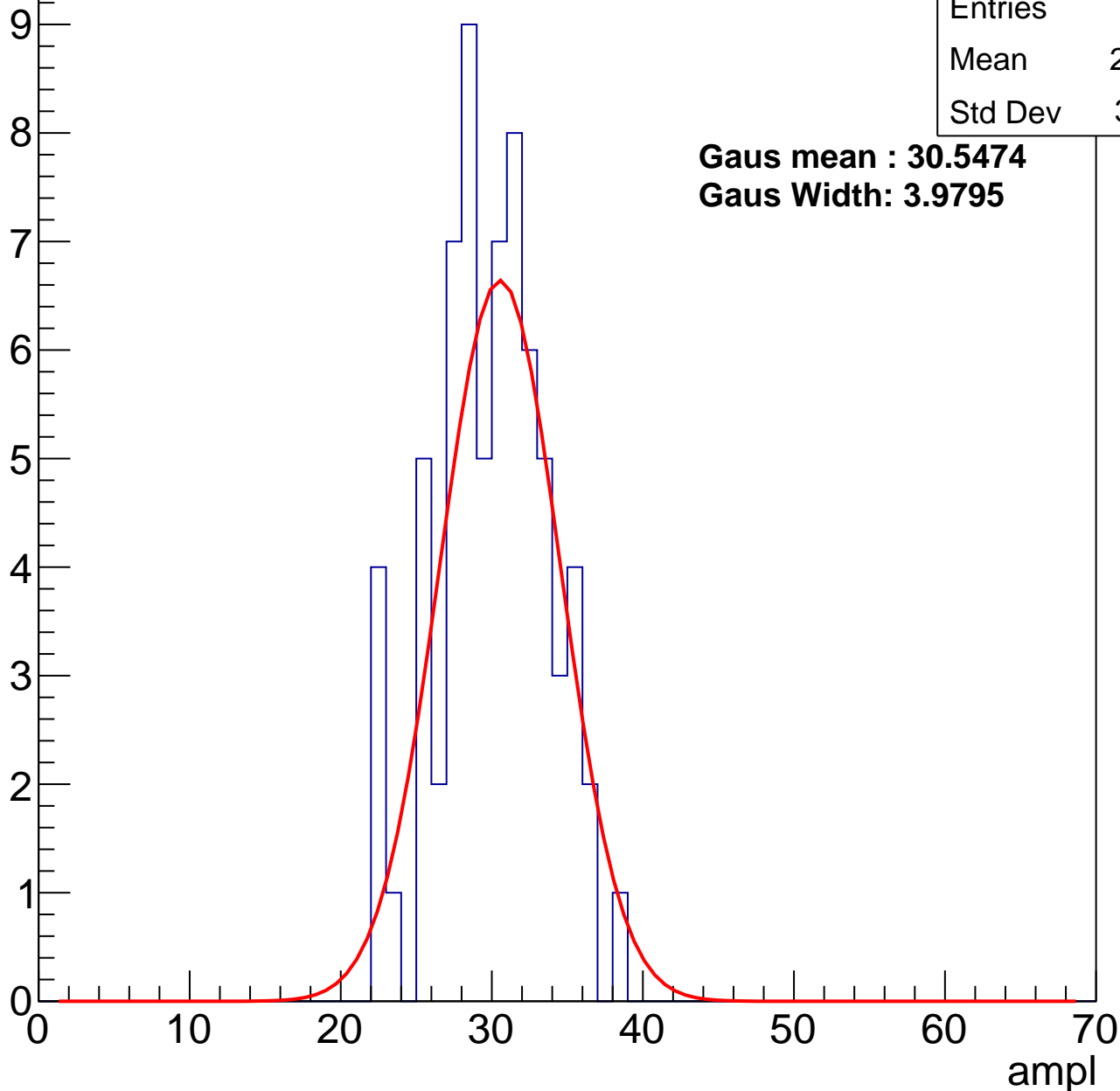
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	29.58
Std Dev	3.641

**Gaus mean : 30.5474**

**Gaus Width: 3.9795**



# B1L102S, U20-ch73, adc1

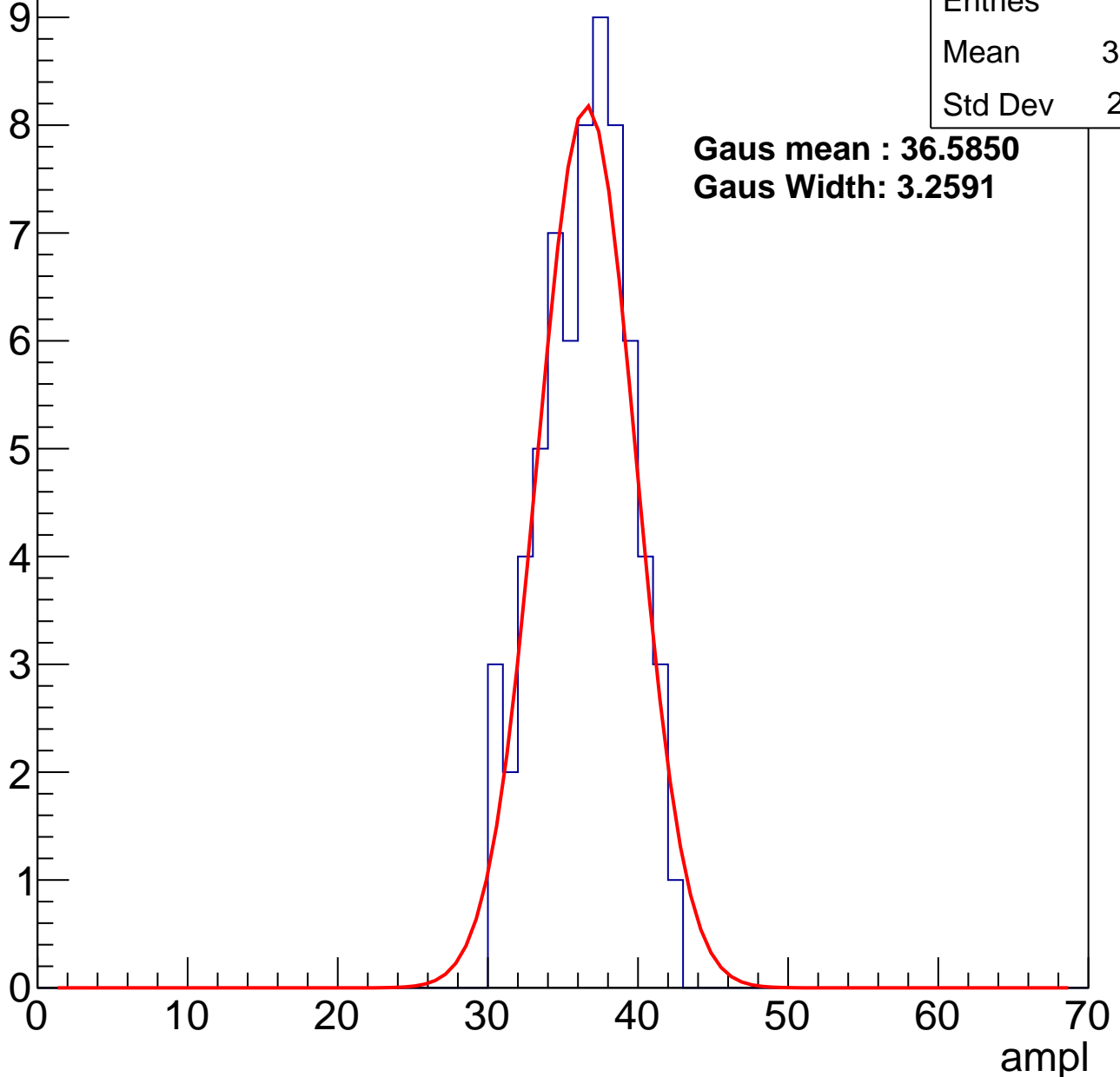
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	36.02
Std Dev	2.941

**Gaus mean : 36.5850**

**Gaus Width: 3.2591**



# B1L102S, U20-ch73, adc2

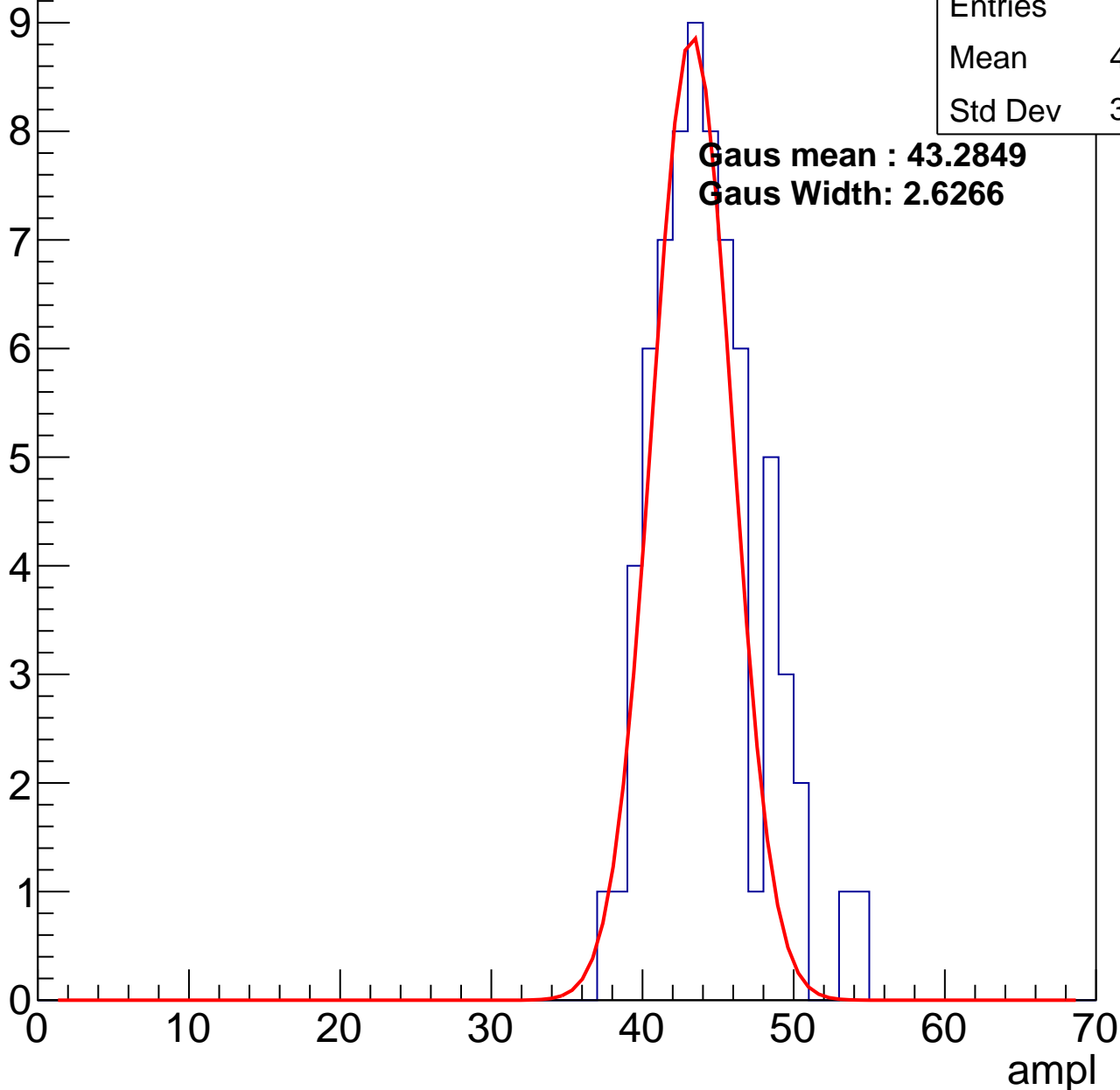
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	43.79
Std Dev	3.443

**Gaus mean : 43.2849**

**Gaus Width: 2.6266**

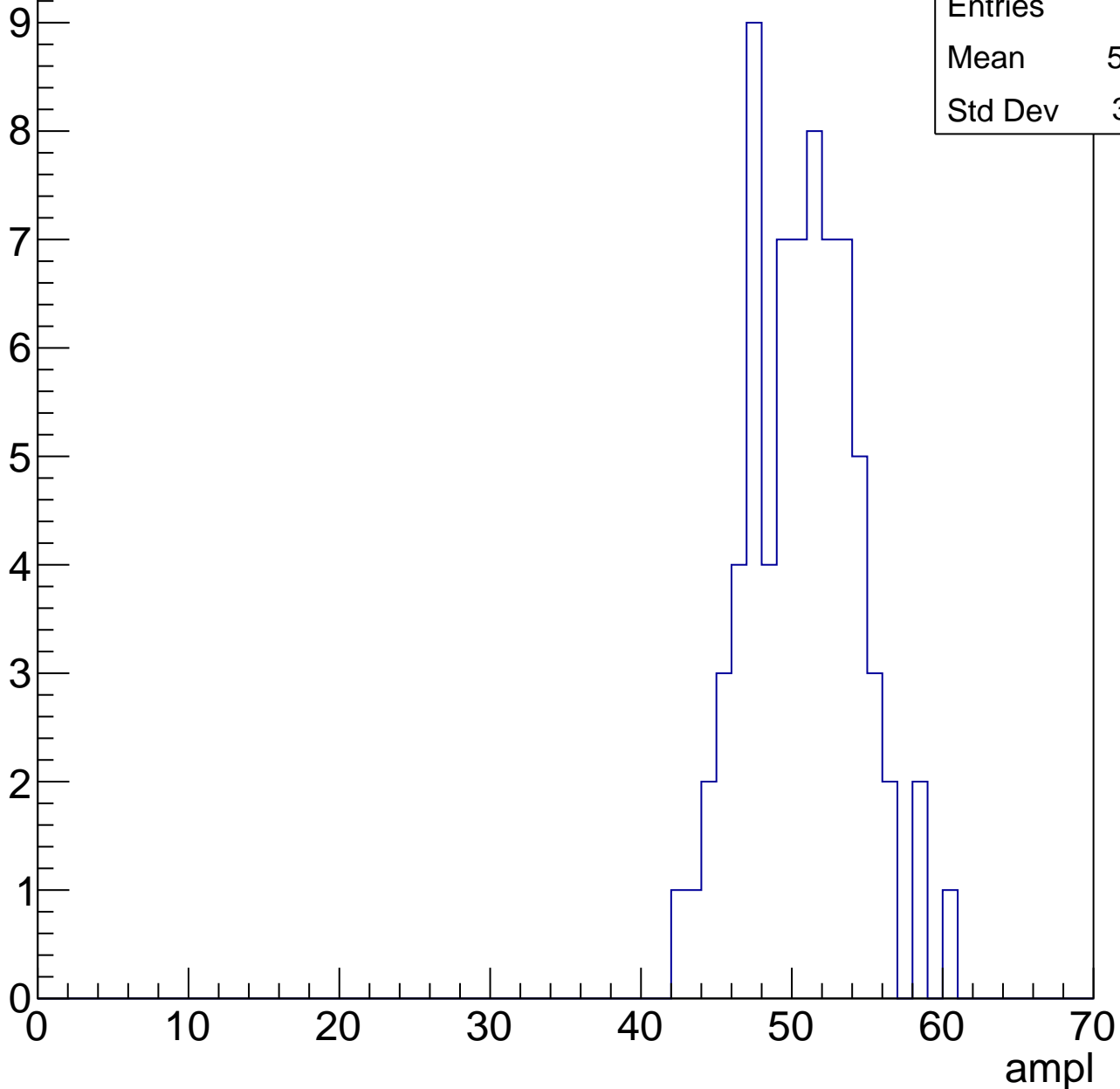


# B1L102S, U20-ch73, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	50.22
Std Dev	3.661

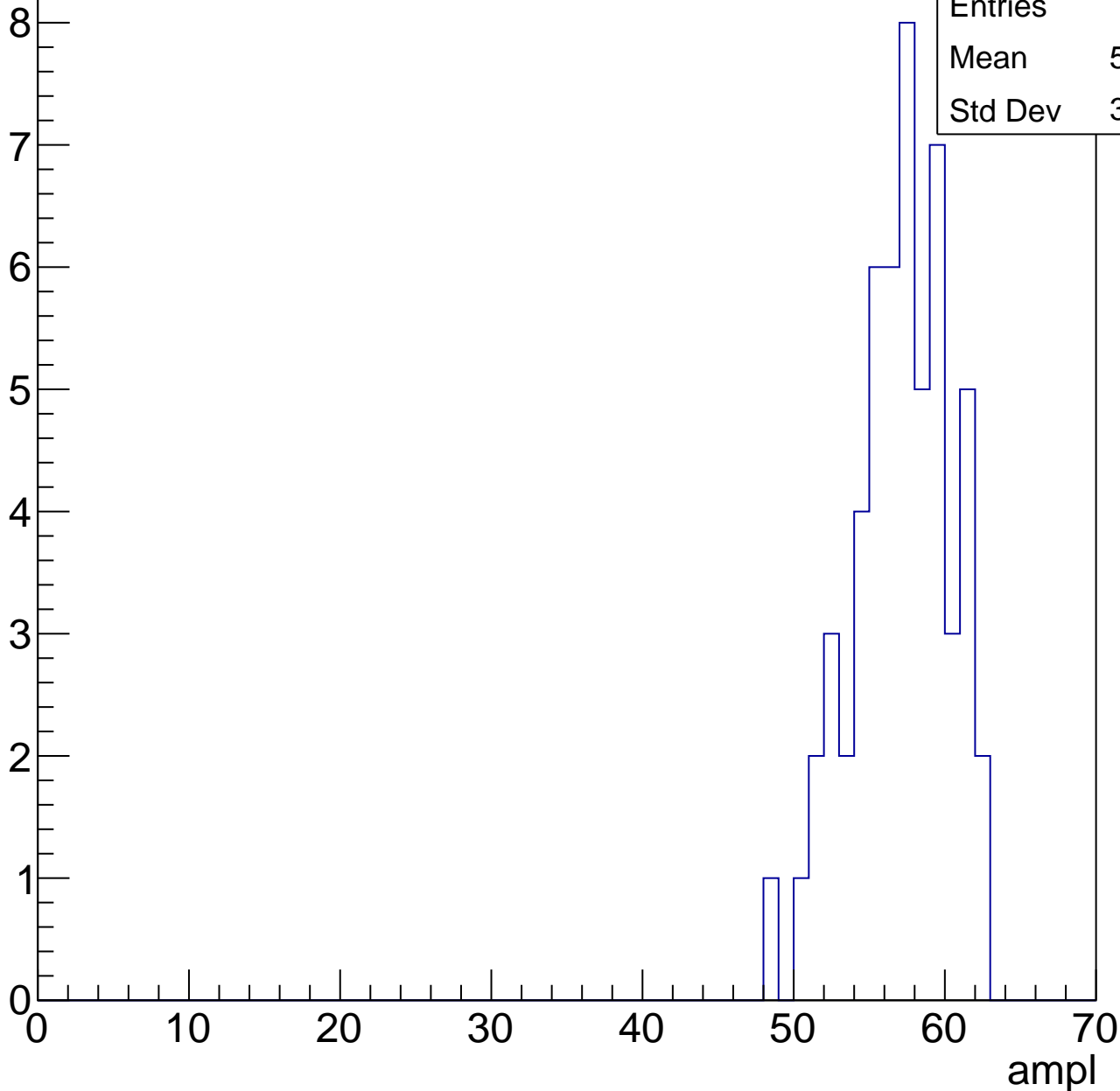


# B1L102S, U20-ch73, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	56.58
Std Dev	3.178

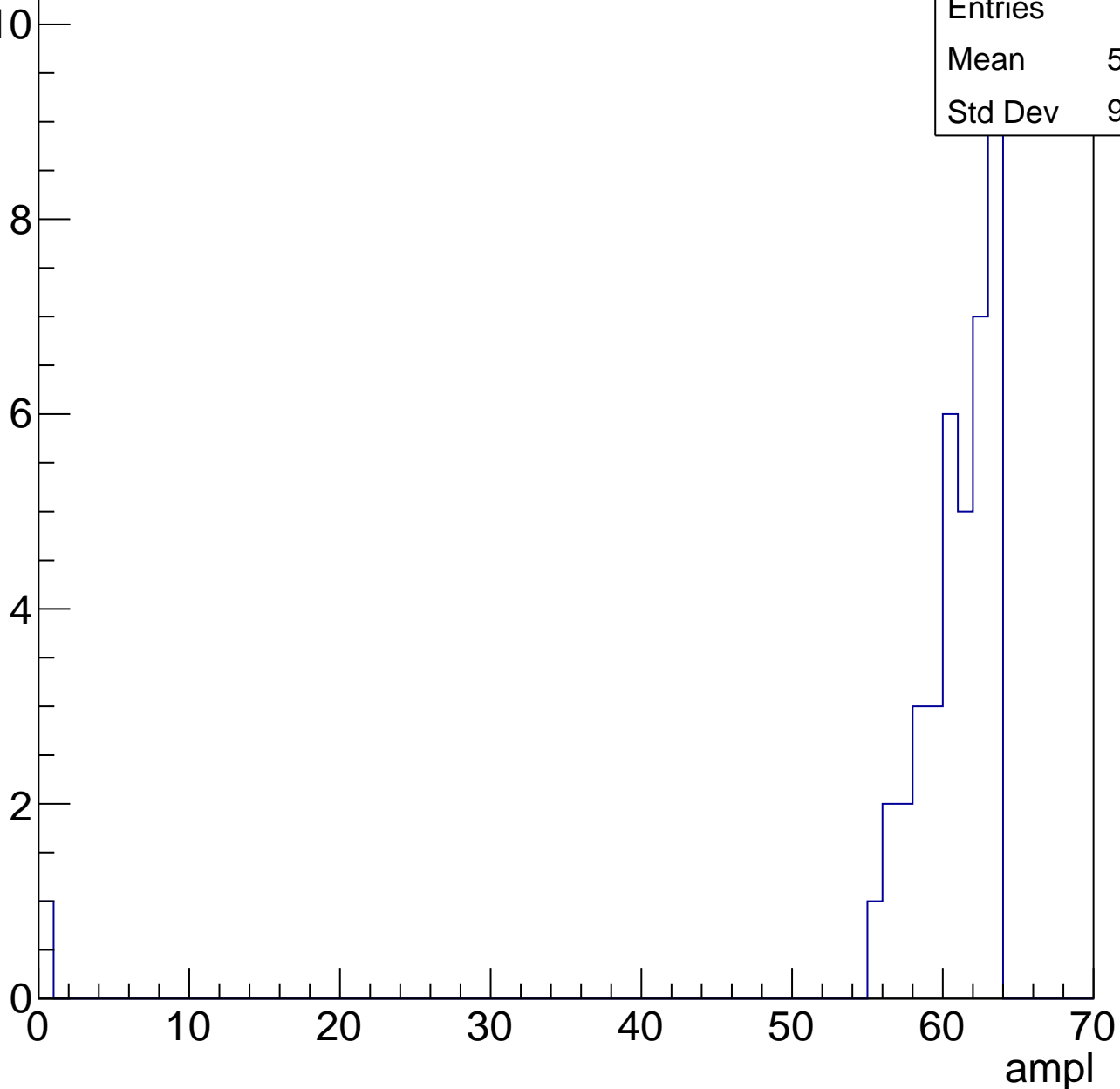


# B1L102S, U20-ch73, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	40
Mean	59.02
Std Dev	9.715



# B1L102S, U20-ch73, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U20-ch73, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch74, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	80
Mean	28.36
Std Dev	5.249

**Gaus mean : 28.5934**

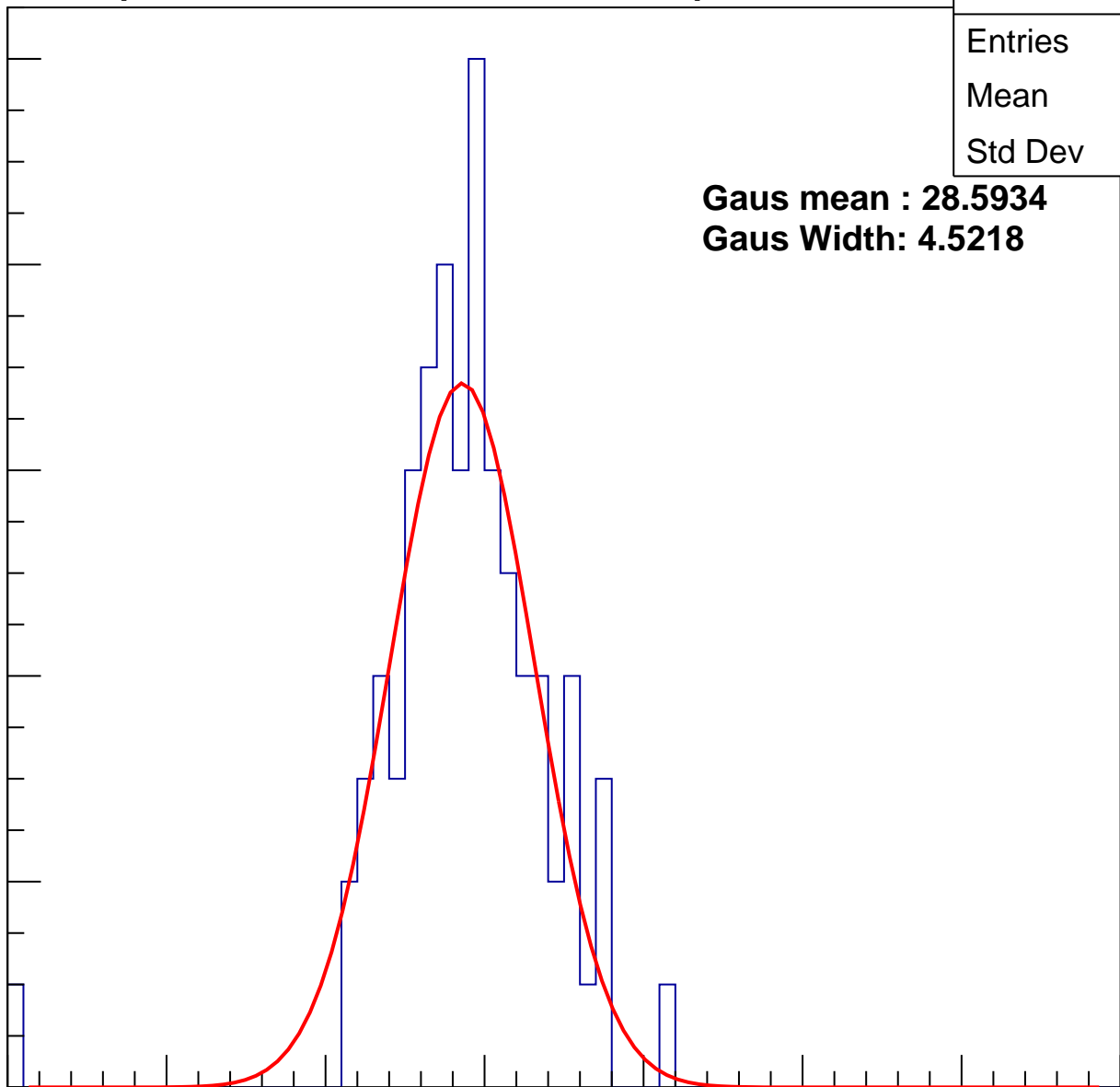
**Gaus Width: 4.5218**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U20-ch74, adc1

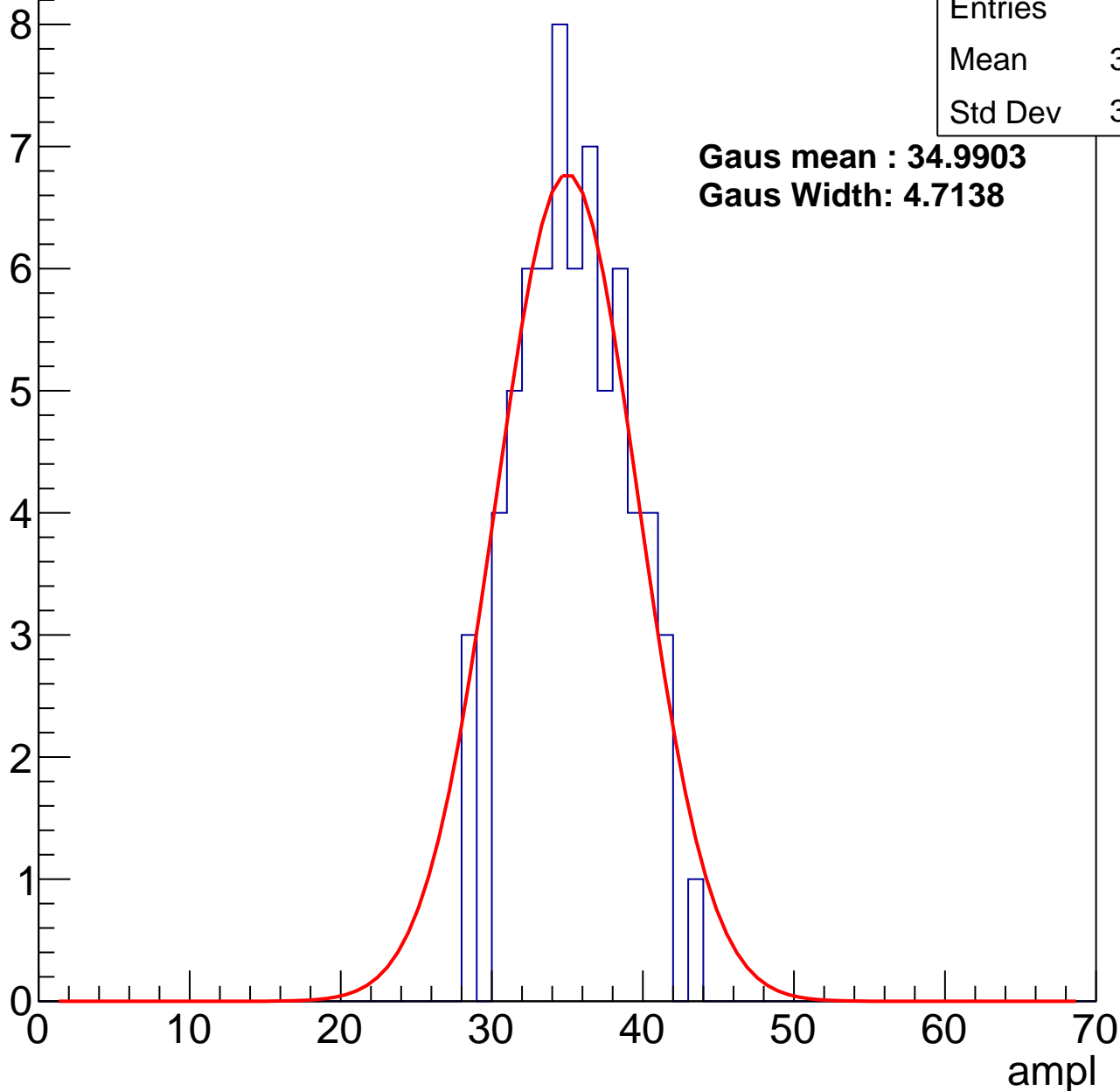
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	34.97
Std Dev	3.494

**Gaus mean : 34.9903**

**Gaus Width: 4.7138**



# B1L102S, U20-ch74, adc2

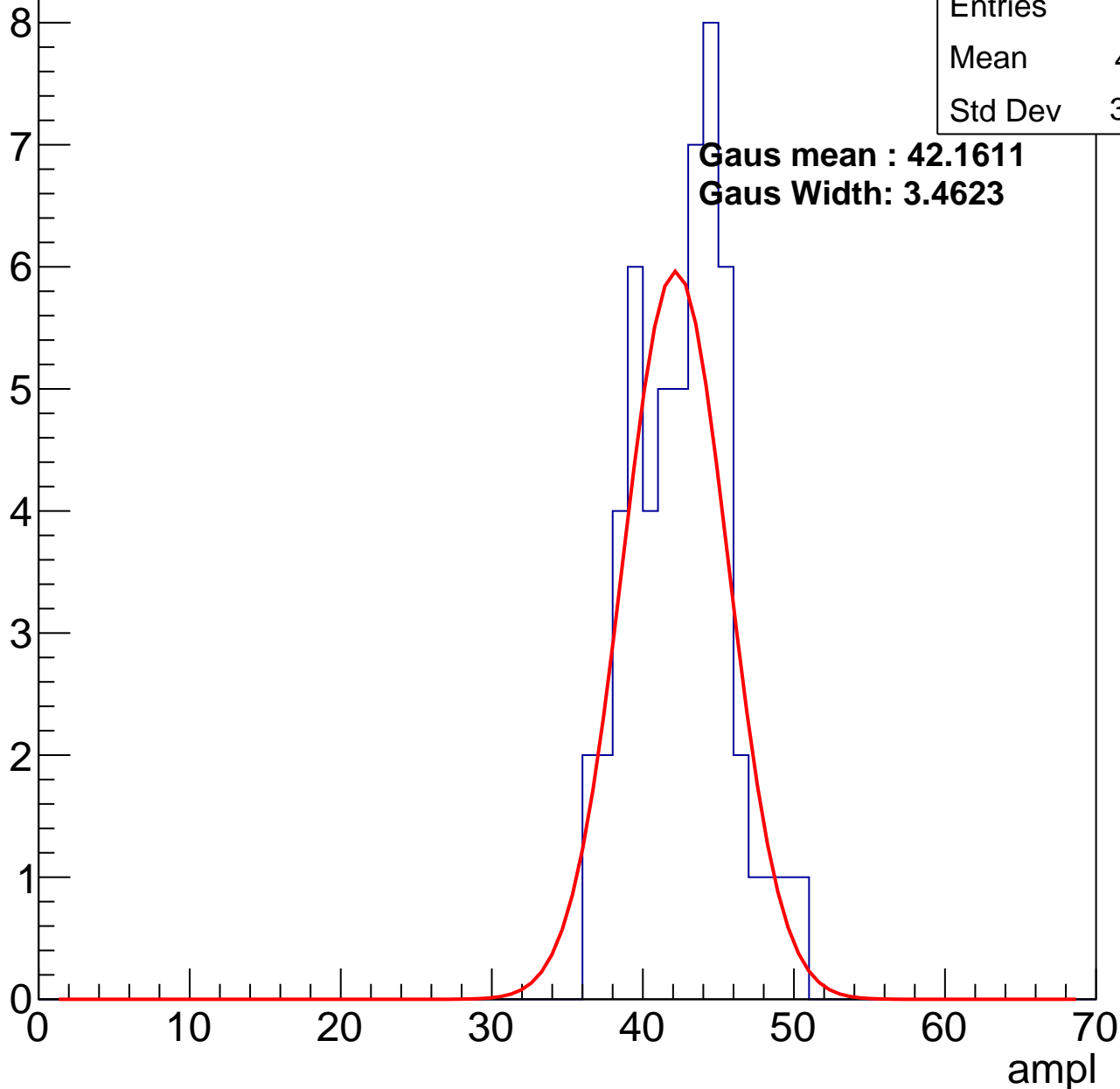
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	42.11
Std Dev	3.189

**Gaus mean : 42.1611**

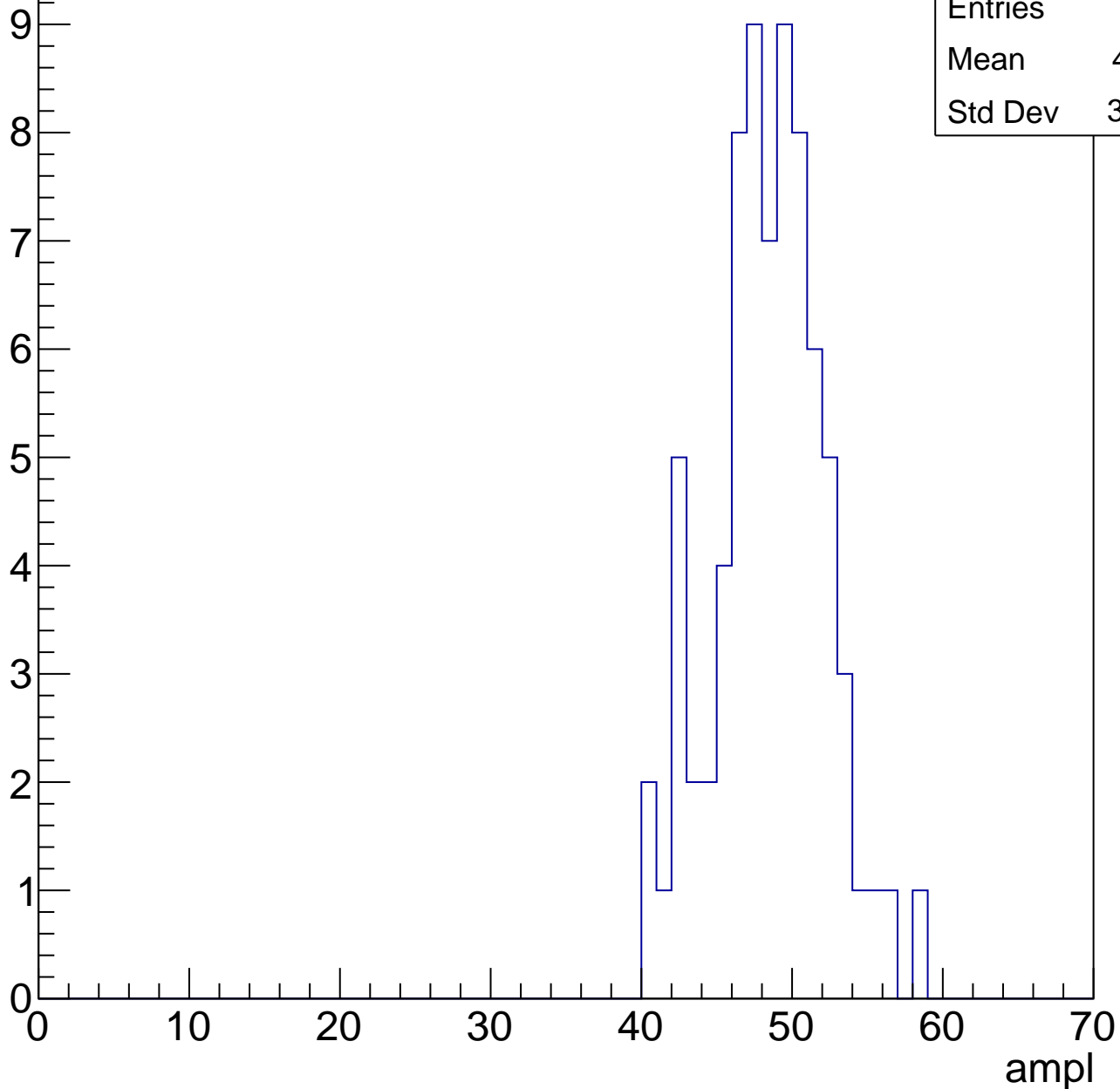
**Gaus Width: 3.4623**



# B1L102S, U20-ch74, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



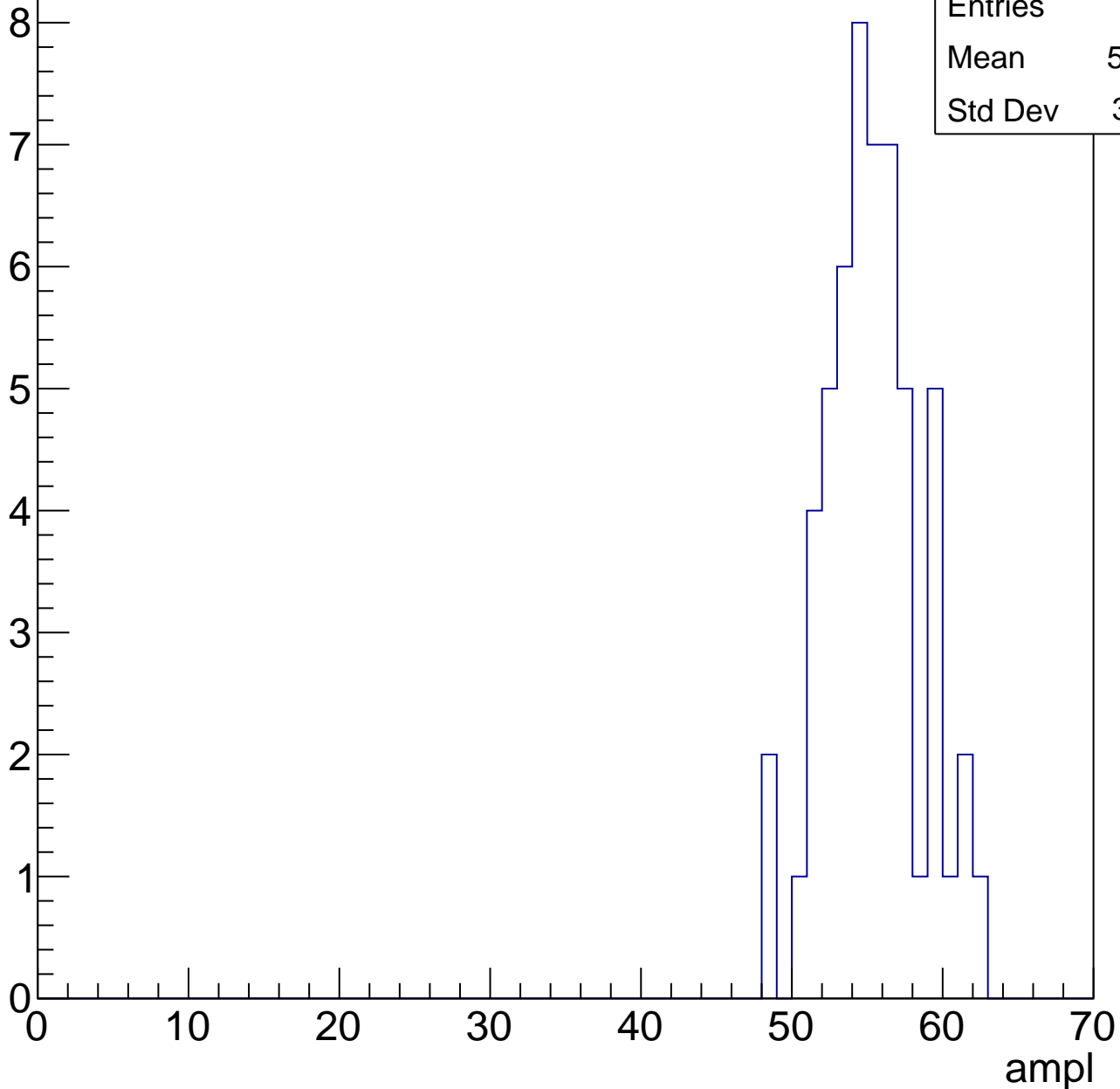
Entries	75
Mean	48.01
Std Dev	3.679

# B1L102S, U20-ch74, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

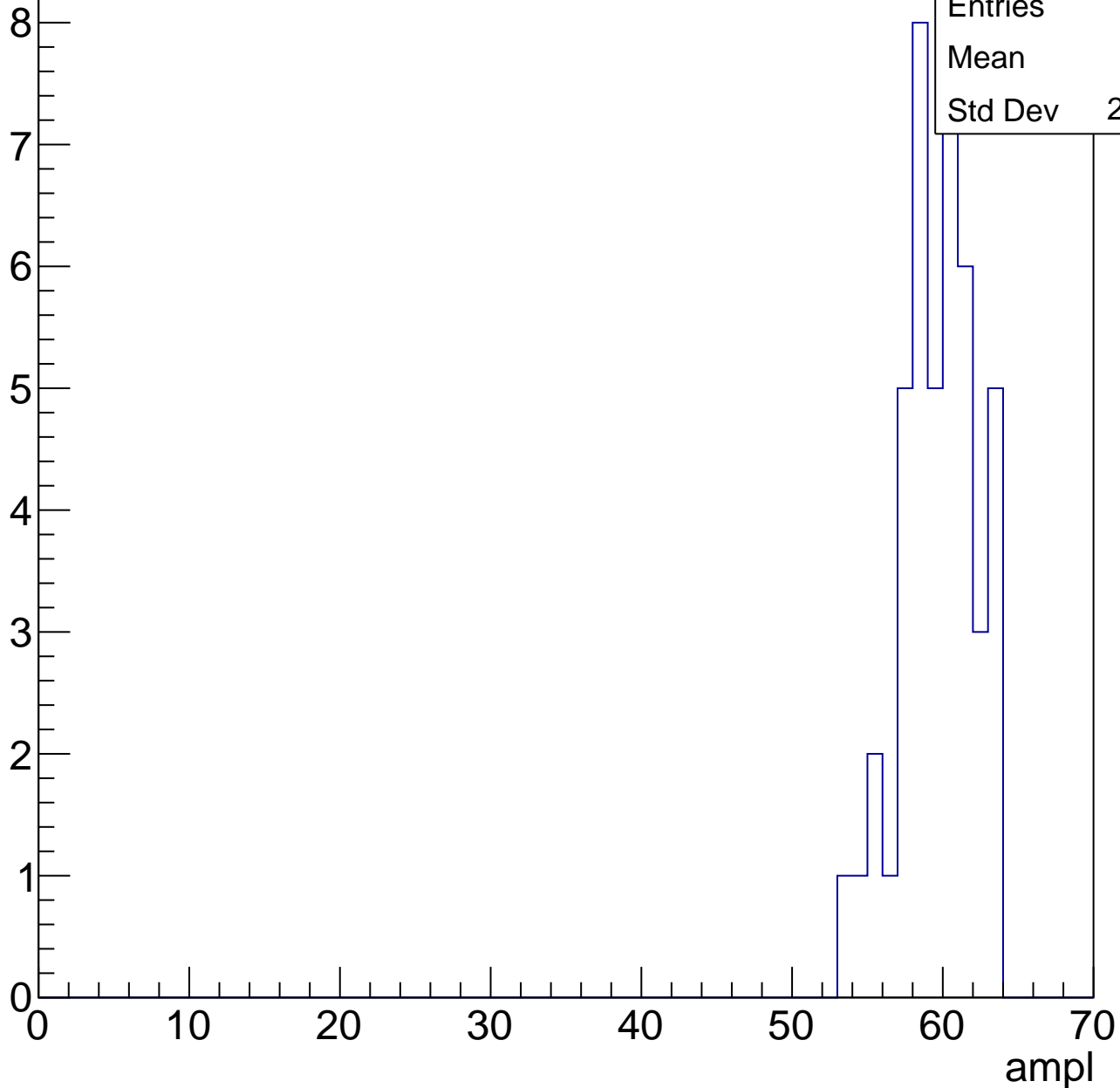
Entries	55
Mean	54.89
Std Dev	3.091



# B1L102S, U20-ch74, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

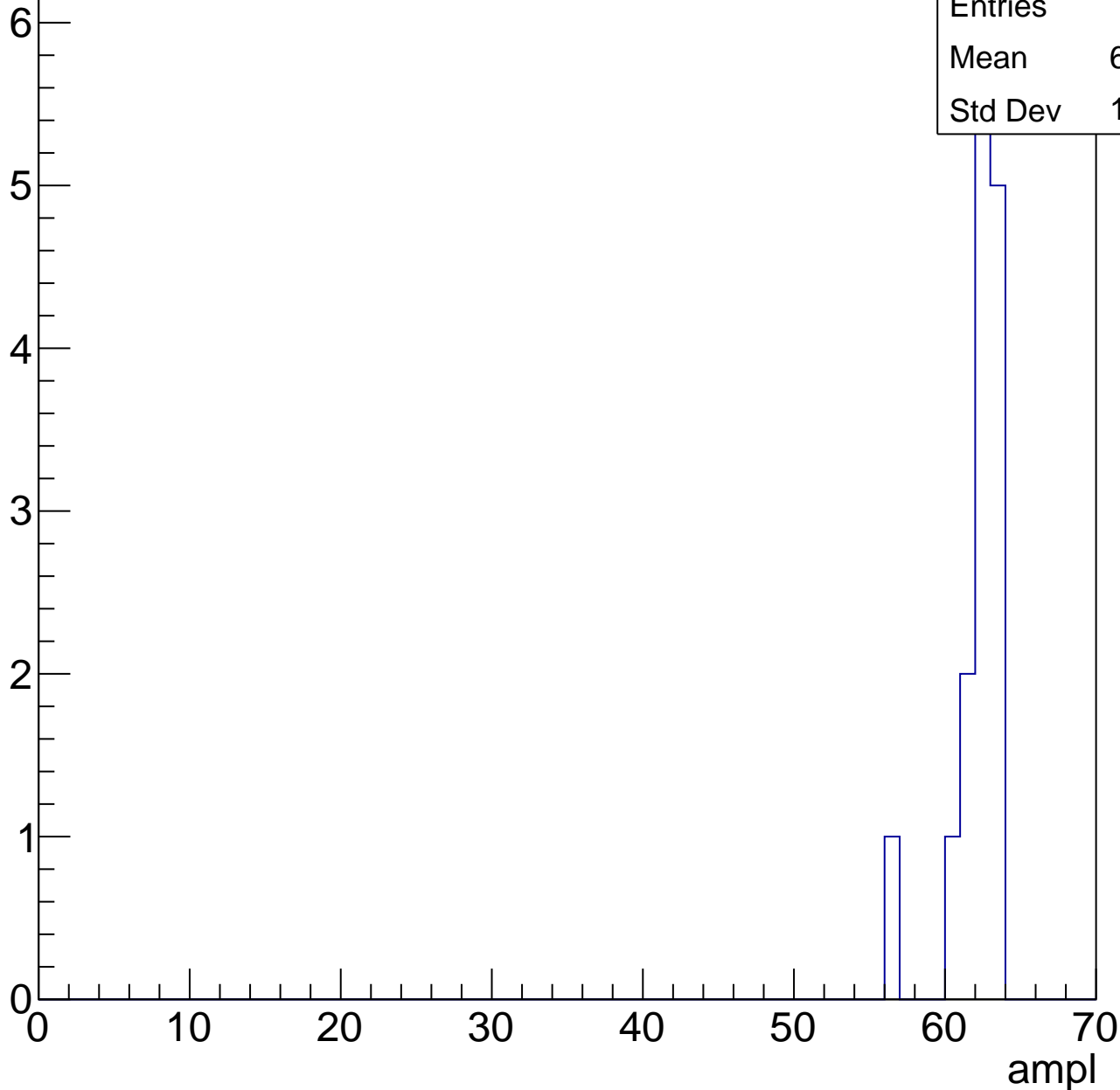


# B1L102S, U20-ch74, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	15
Mean	61.67
Std Dev	1.738





# B1L102S, U20-ch74, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch75, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	72
Mean	27.56
Std Dev	3.48

**Gaus mean : 27.6893**

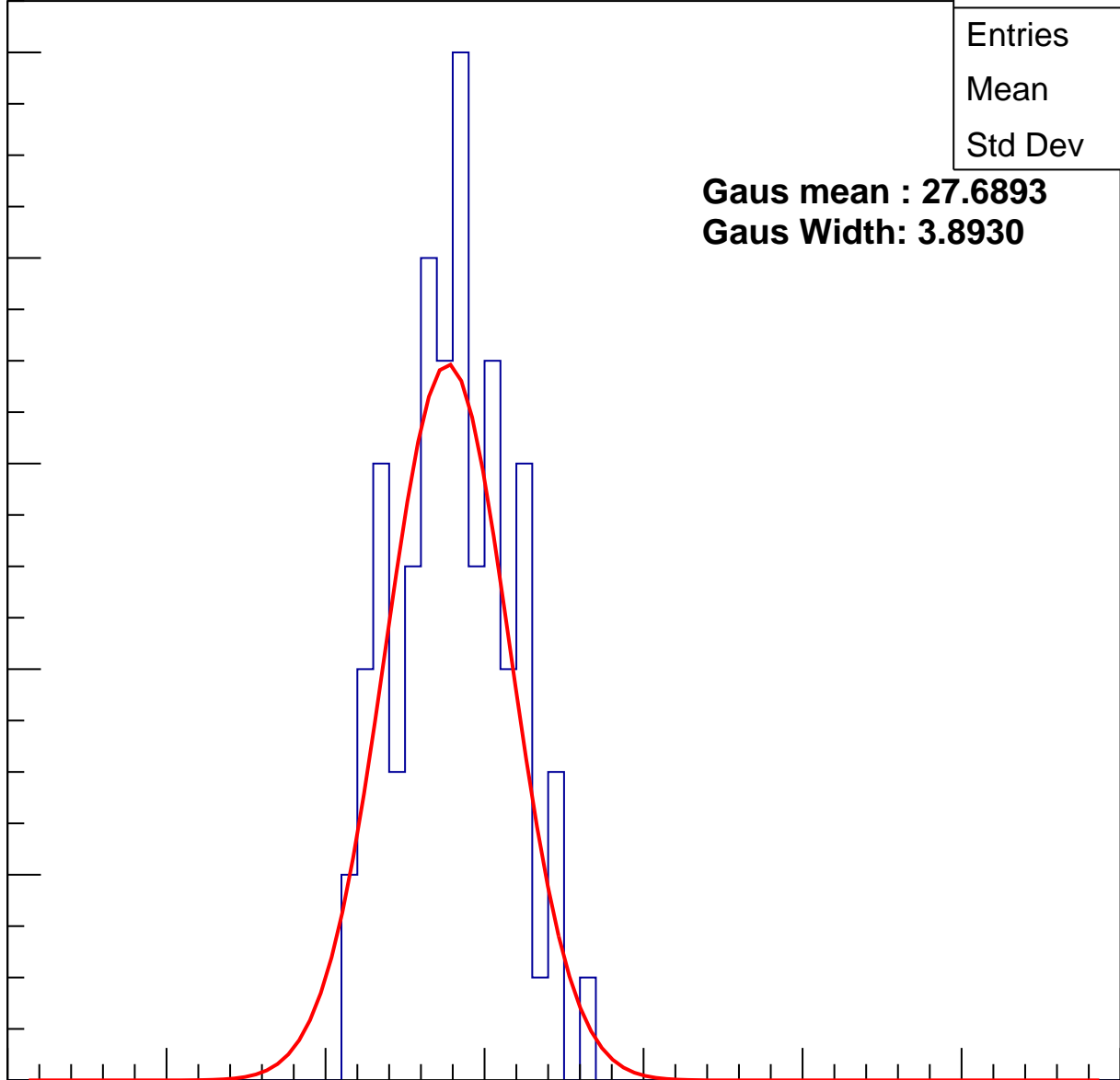
**Gaus Width: 3.8930**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



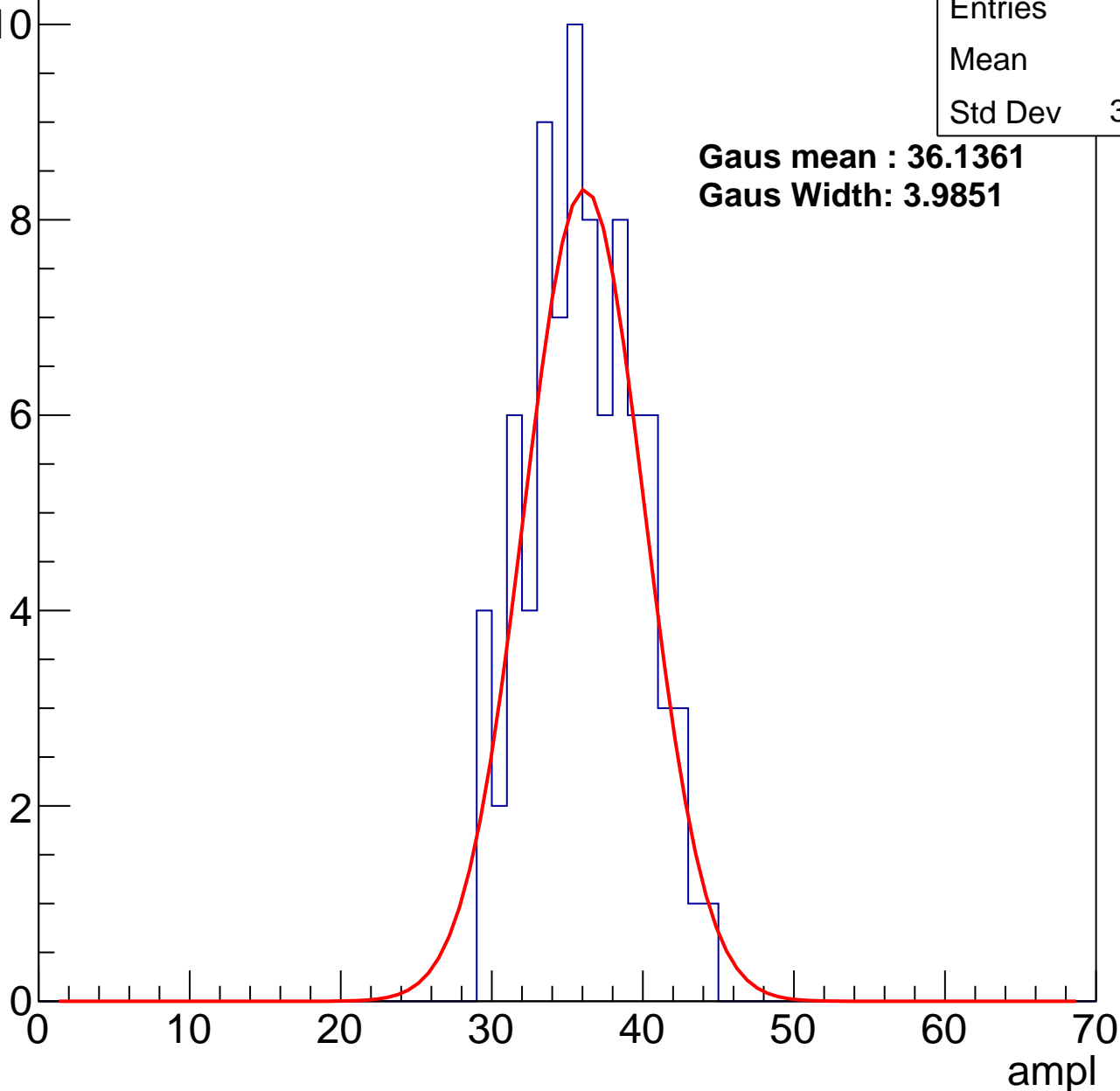
# B1L102S, U20-ch75, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	84
Mean	35.7
Std Dev	3.582

**Gaus mean : 36.1361**  
**Gaus Width: 3.9851**



# B1L102S, U20-ch75, adc2

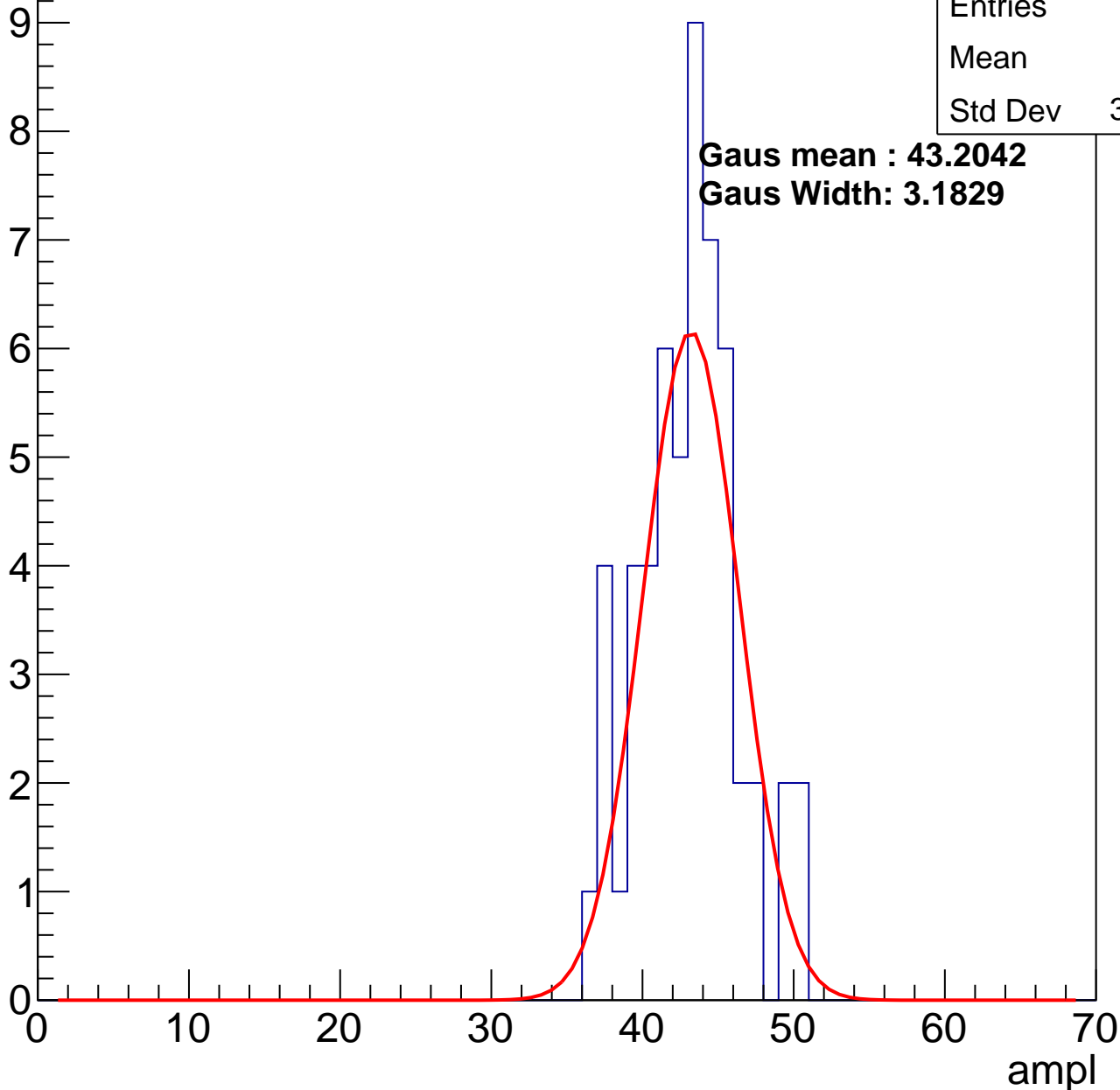
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	42.6
Std Dev	3.273

**Gaus mean : 43.2042**

**Gaus Width: 3.1829**

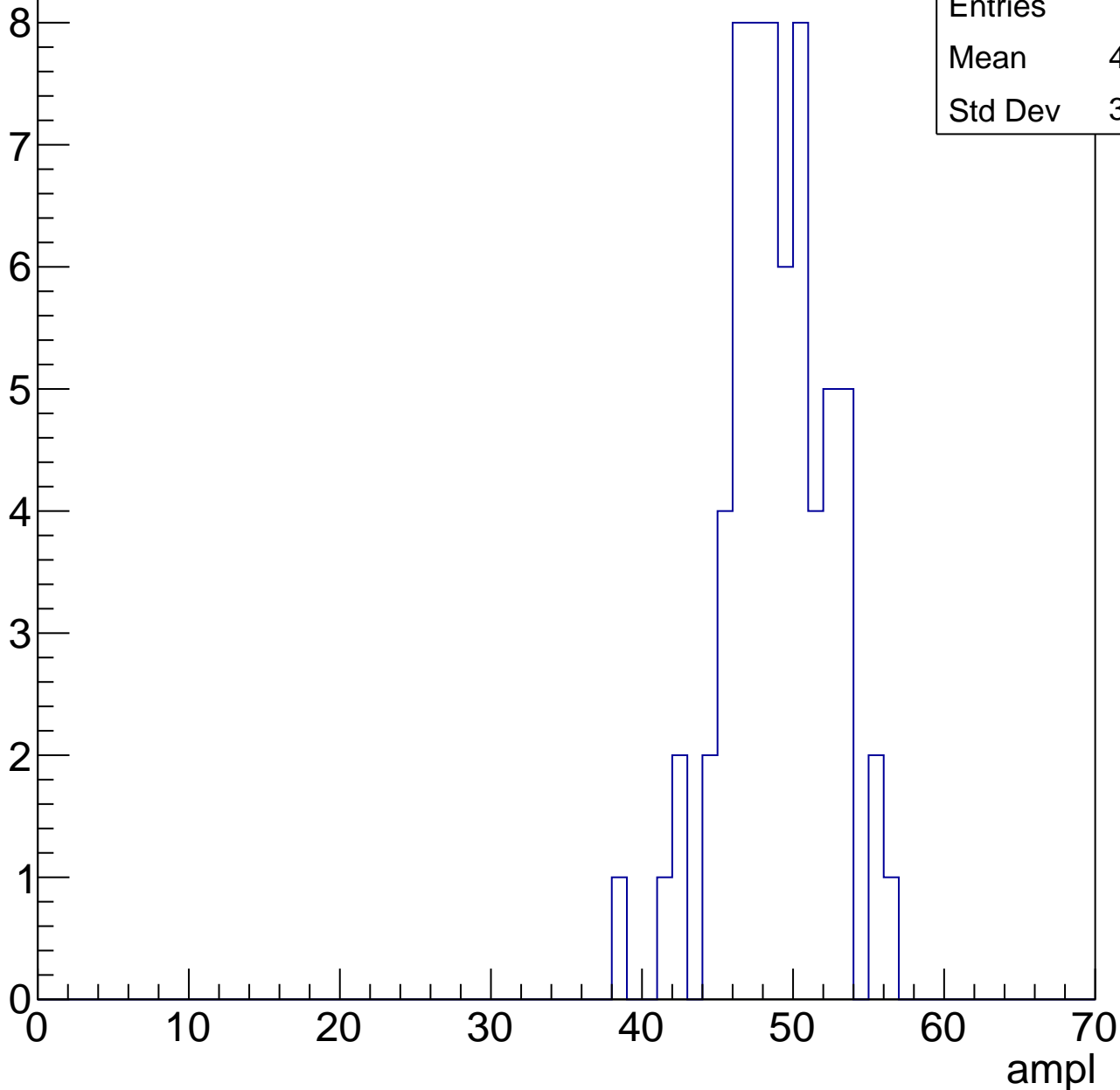


# B1L102S, U20-ch75, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

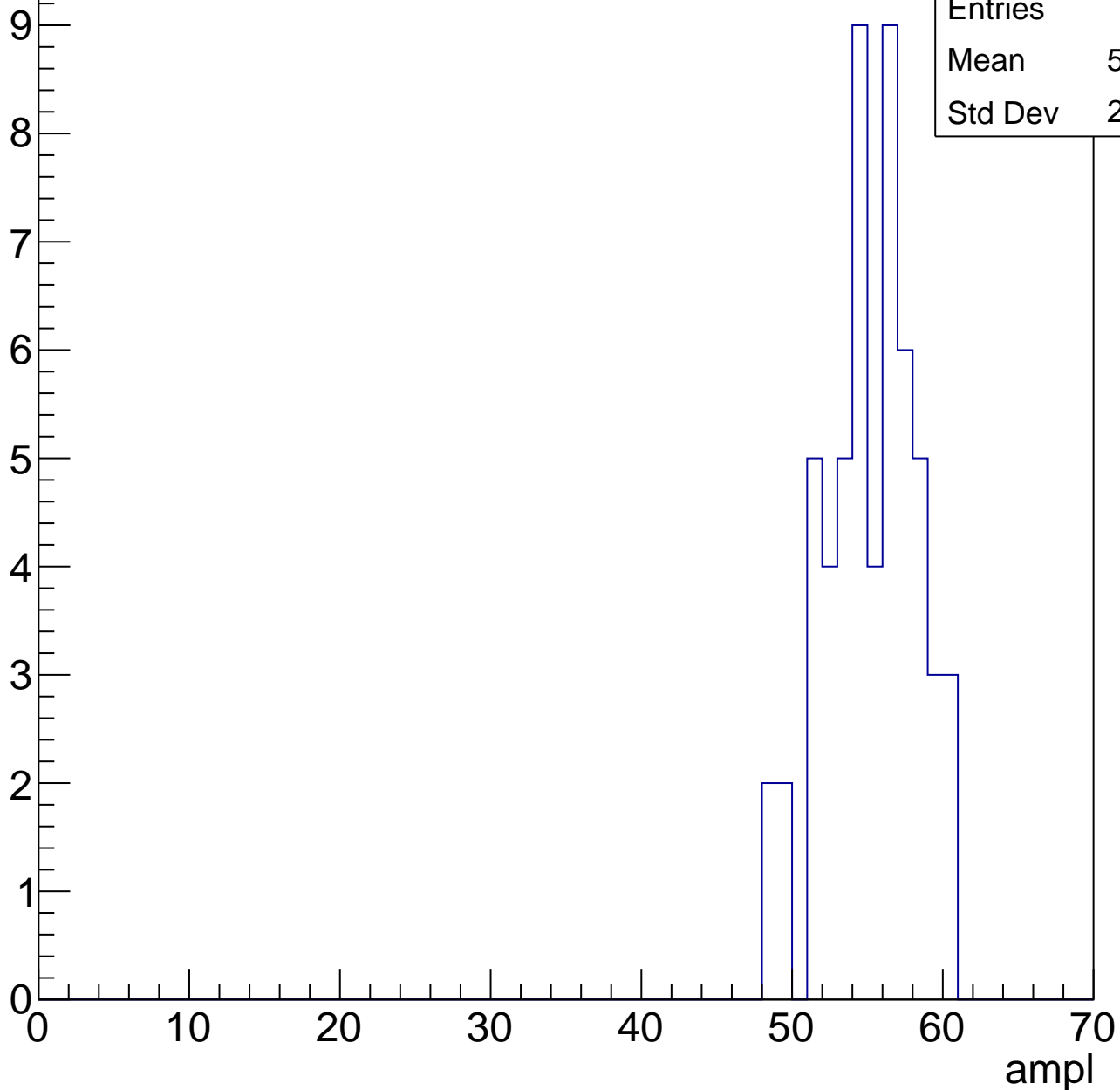
Entries	65
Mean	48.43
Std Dev	3.415



# B1L102S, U20-ch75, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

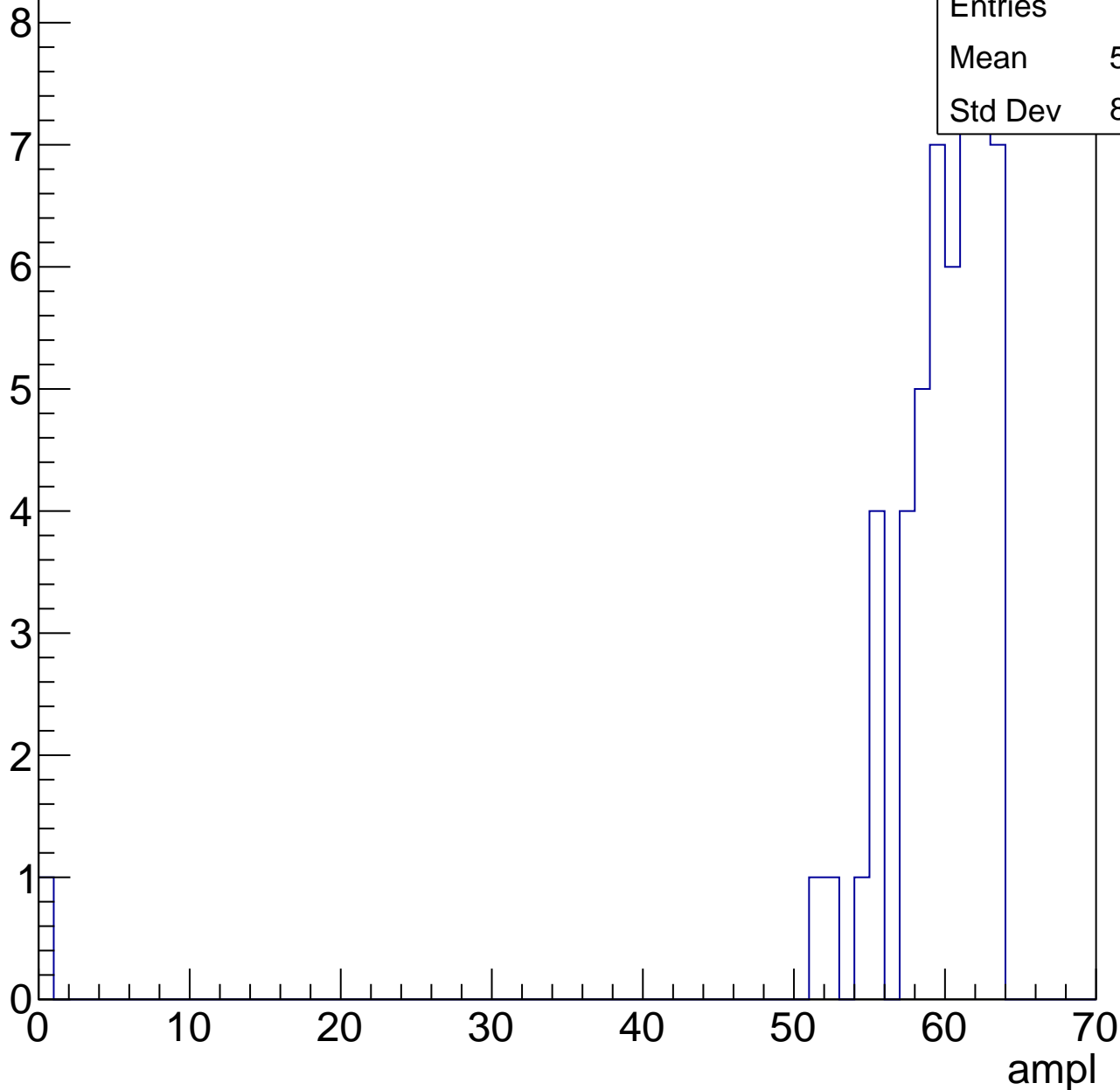


# B1L102S, U20-ch75, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

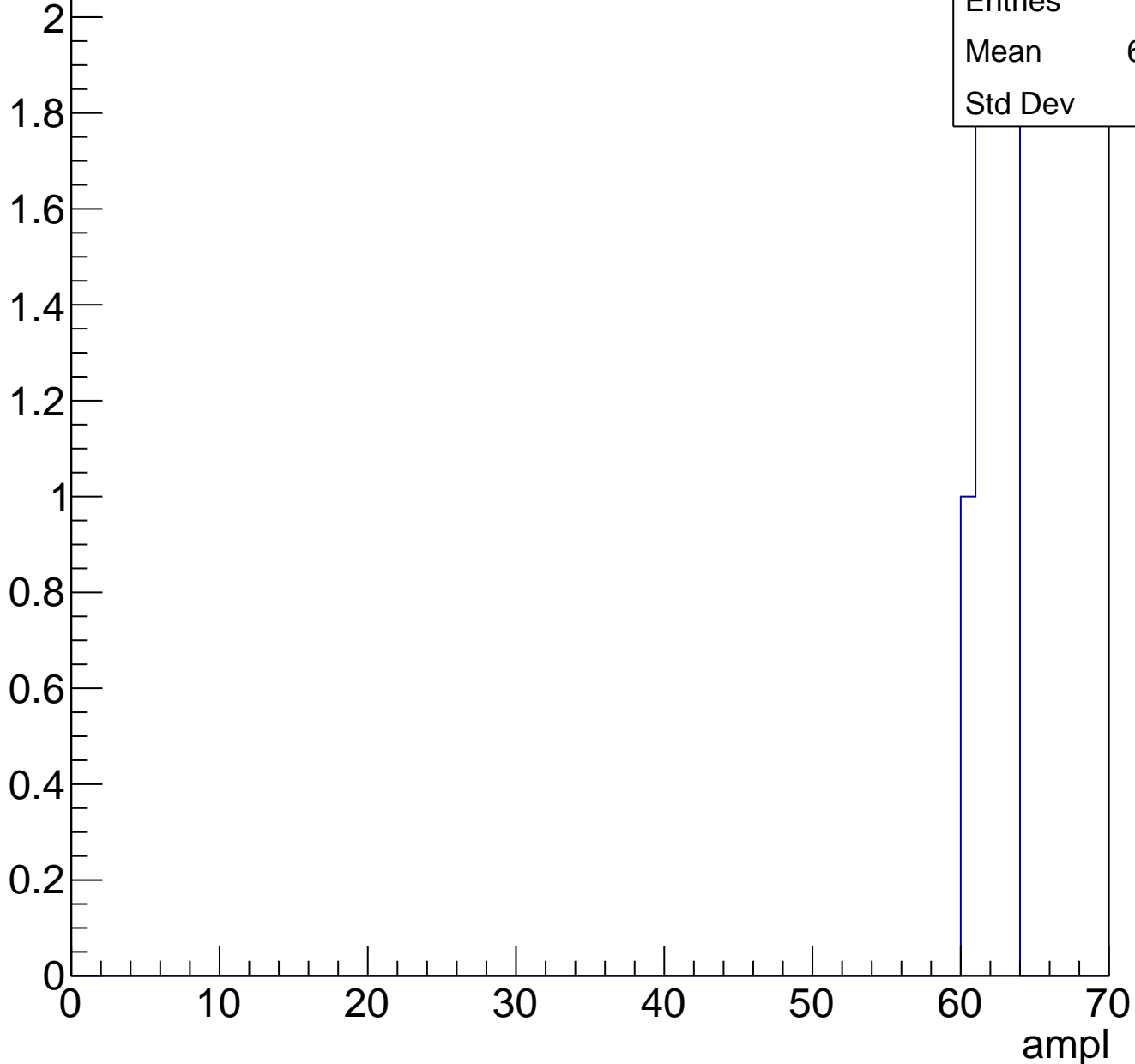
Entries	53
Mean	58.36
Std Dev	8.583



# B1L102S, U20-ch75, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U20-ch75, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	3
Mean	21
Std Dev	29.7

# B1L102S, U20-ch76, adc0

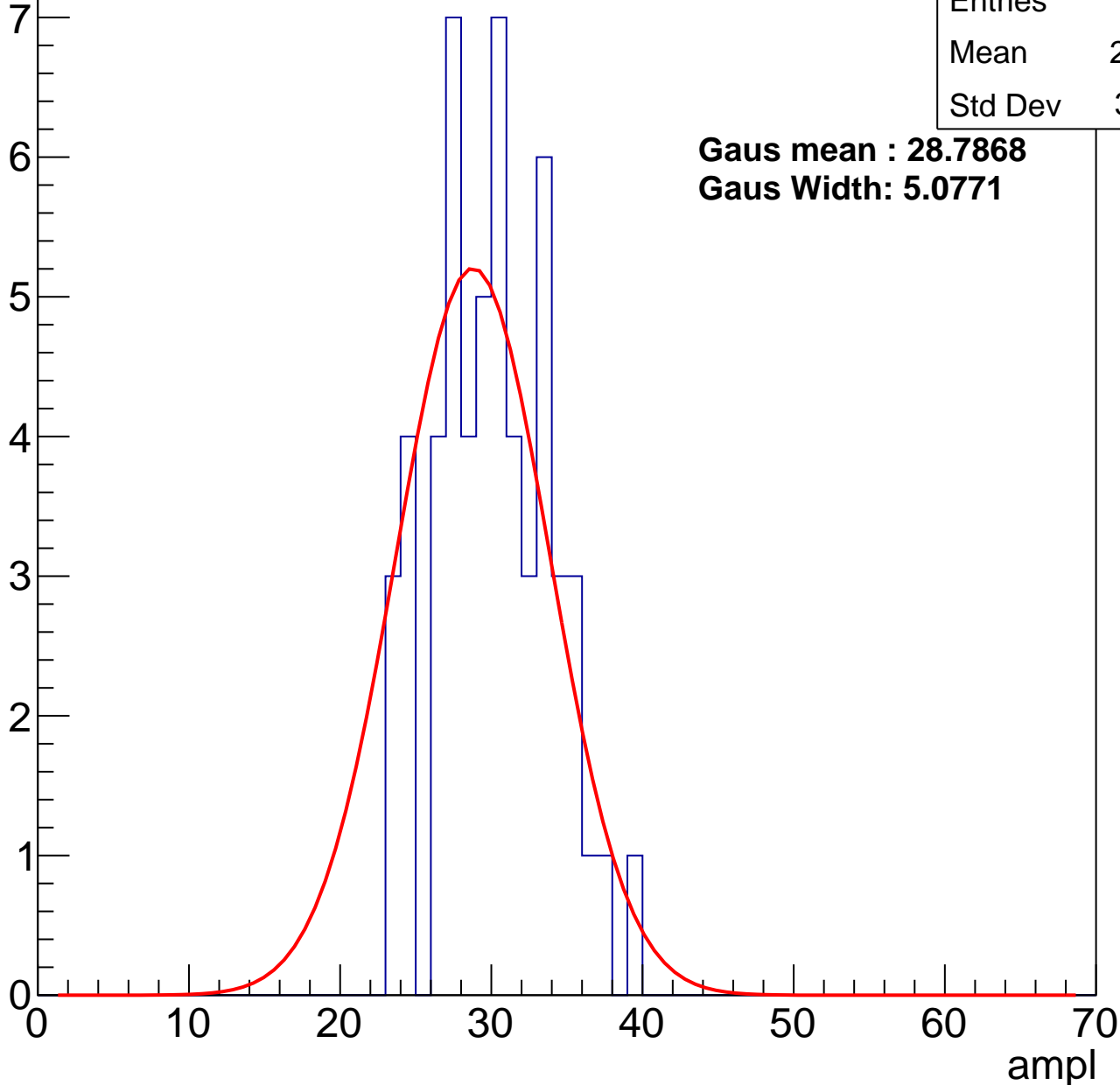
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	29.68
Std Dev	3.761

**Gaus mean : 28.7868**

**Gaus Width: 5.0771**



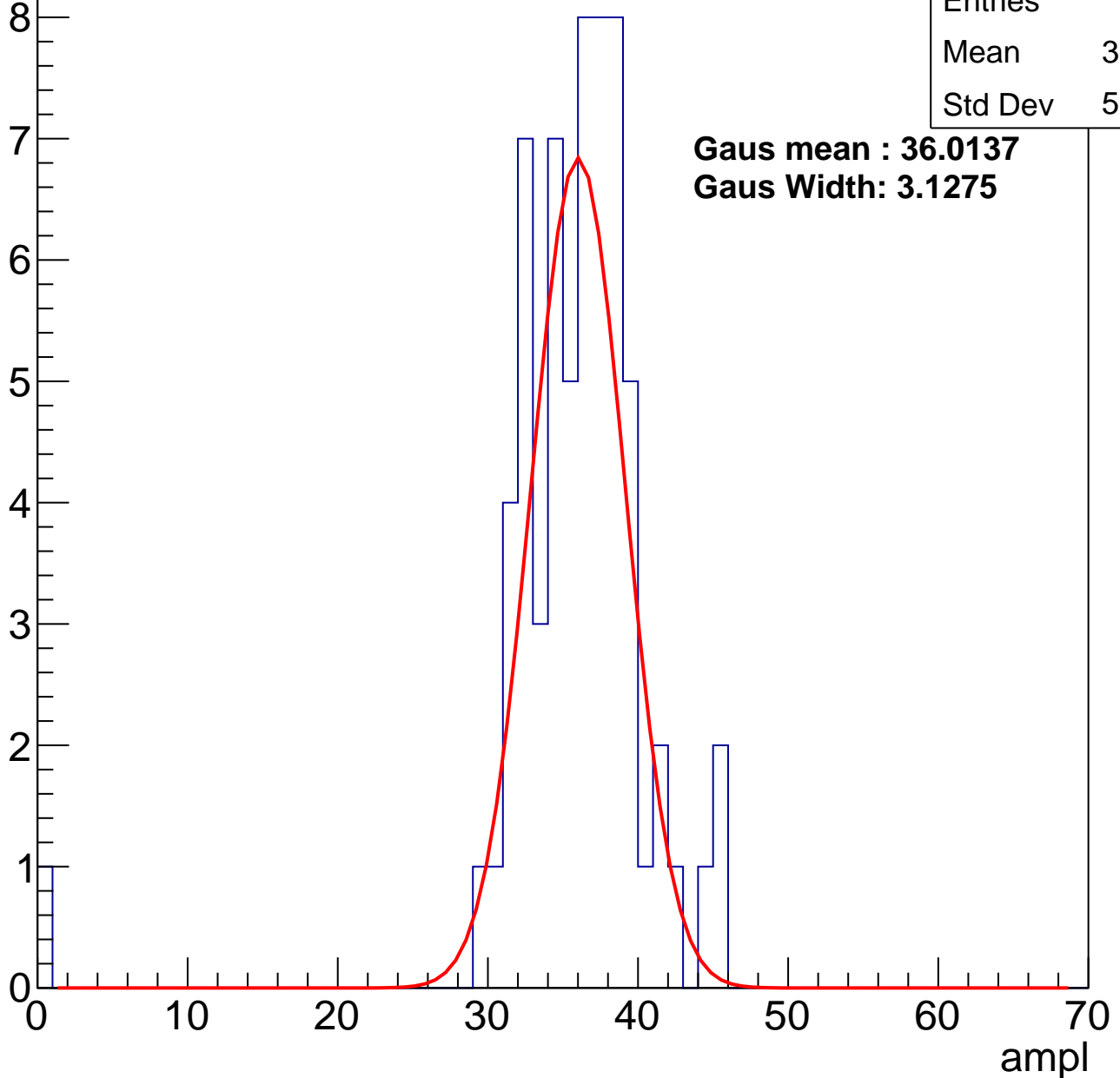
# B1L102S, U20-ch76, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	35.38
Std Dev	5.604

**Gaus mean : 36.0137**  
**Gaus Width: 3.1275**



# B1L102S, U20-ch76, adc2

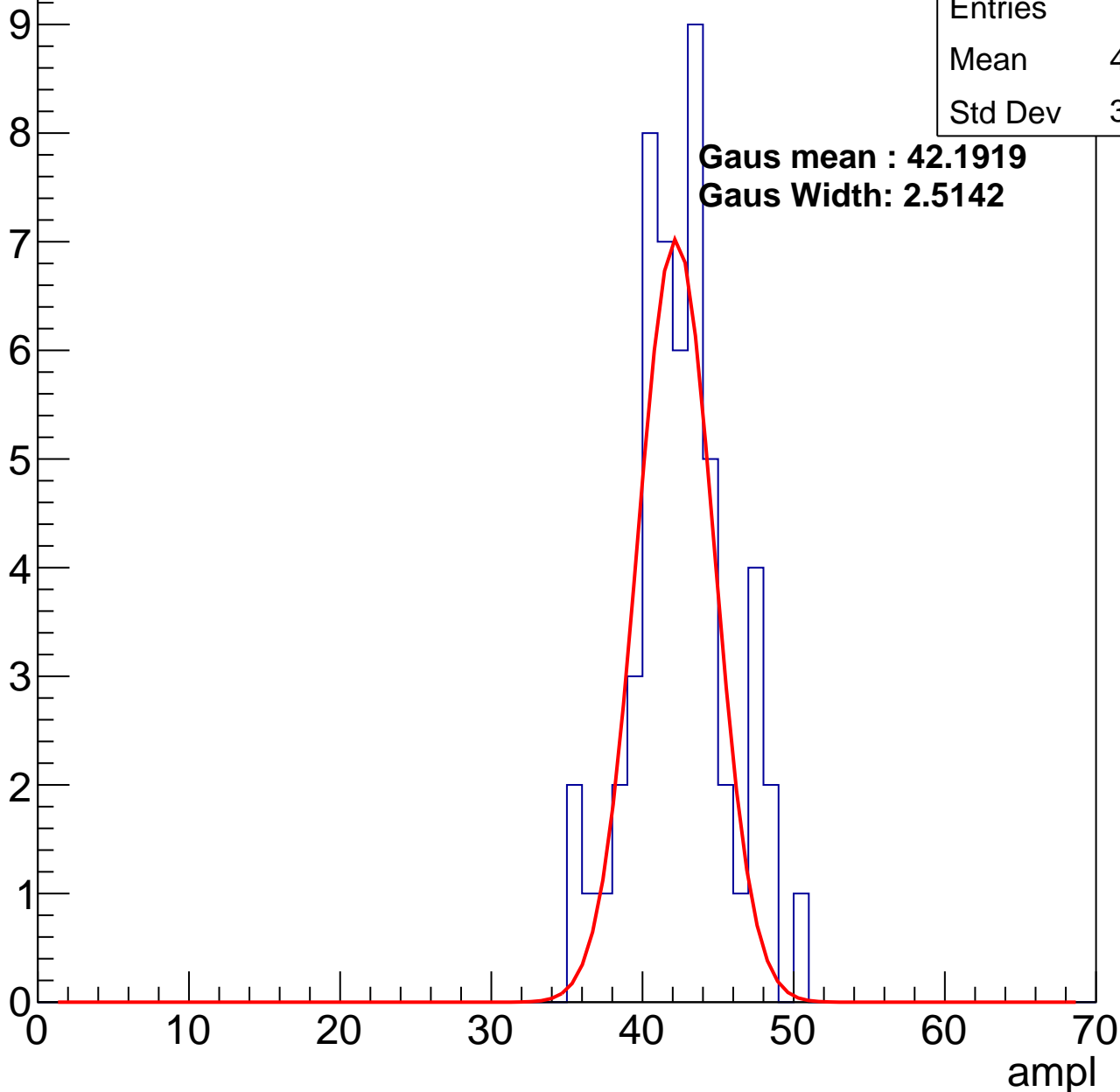
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	42.07
Std Dev	3.208

**Gaus mean : 42.1919**

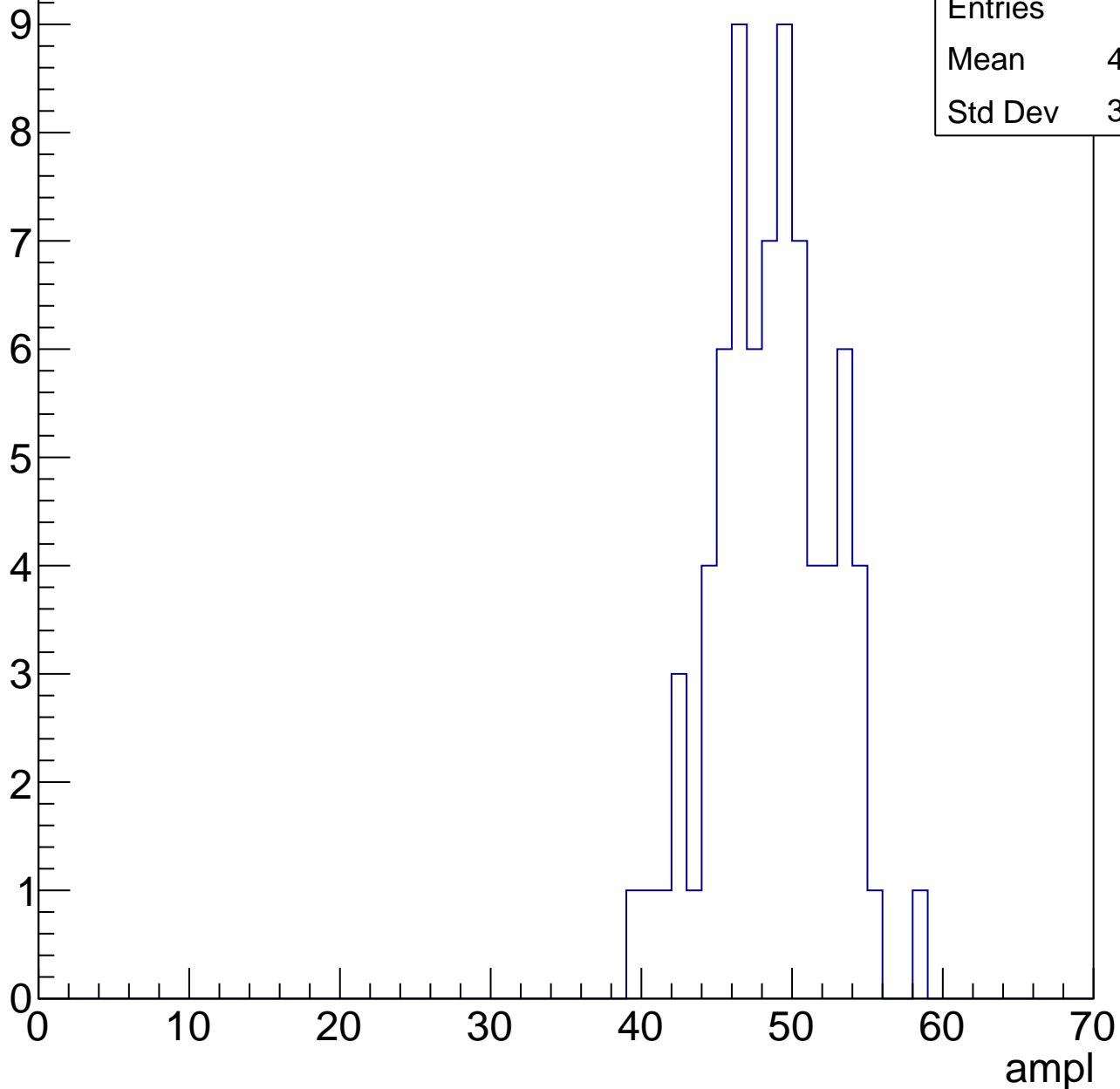
**Gaus Width: 2.5142**



# B1L102S, U20-ch76, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

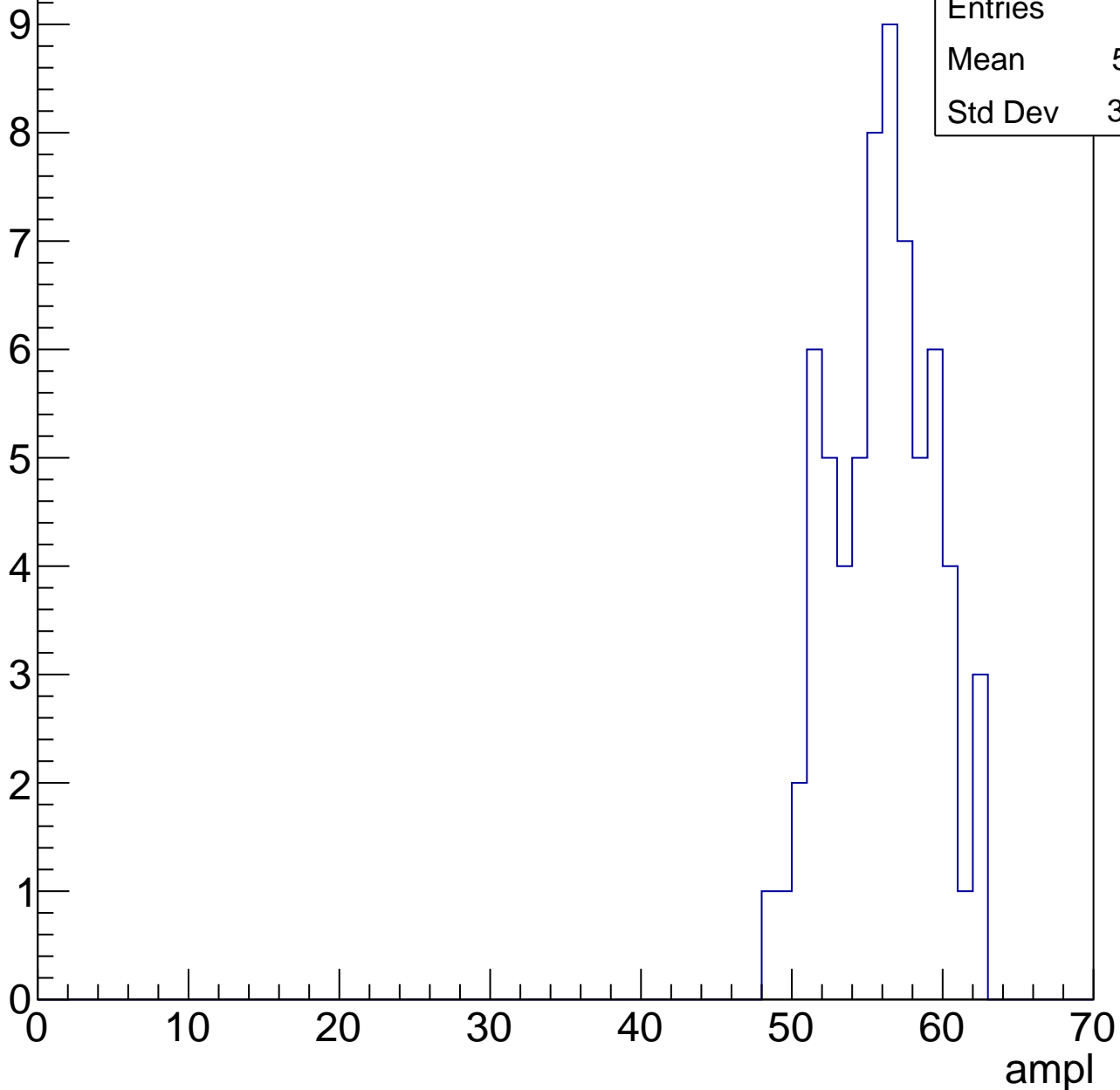


# B1L102S, U20-ch76, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	55.51
Std Dev	3.325

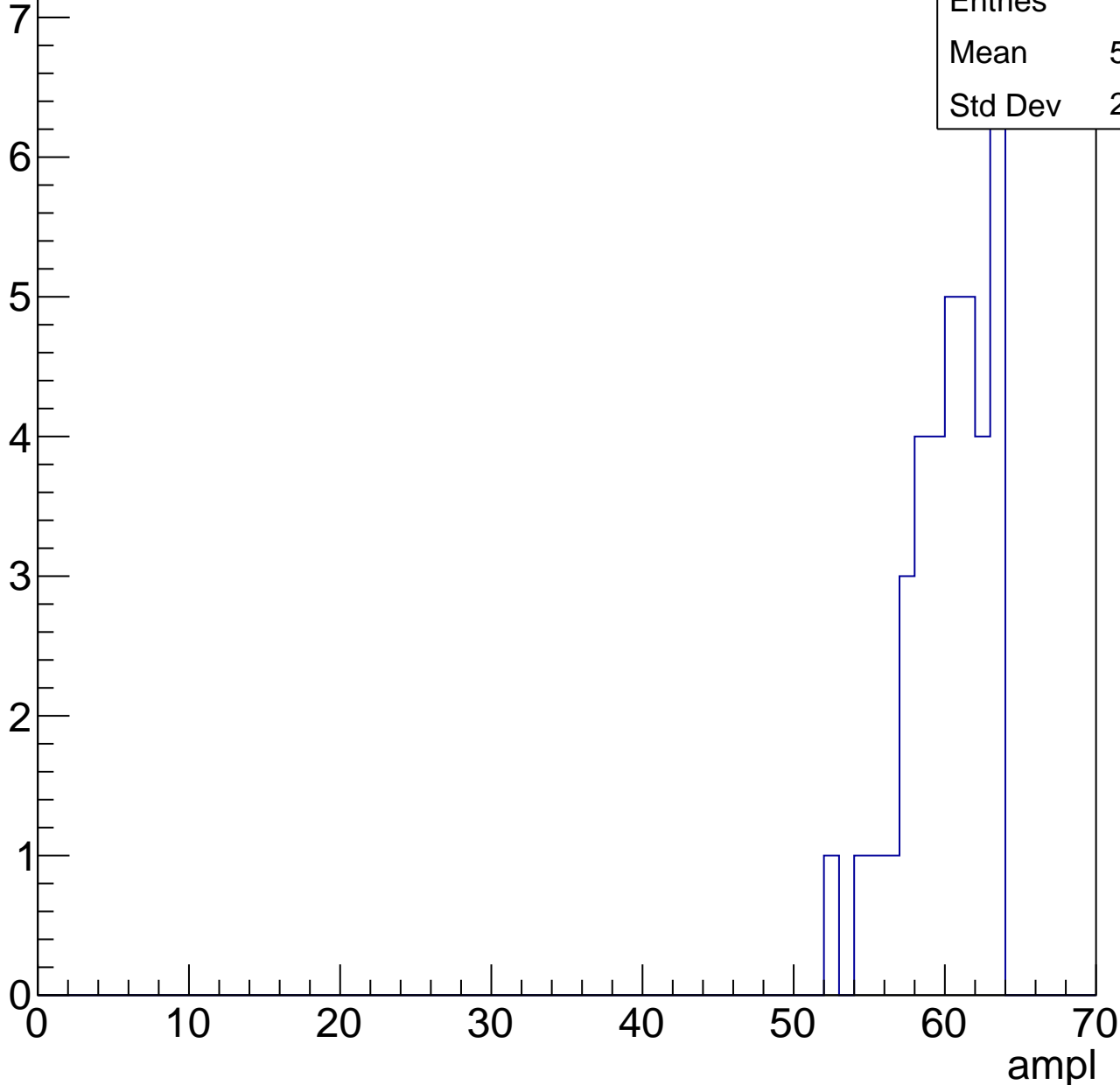


# B1L102S, U20-ch76, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

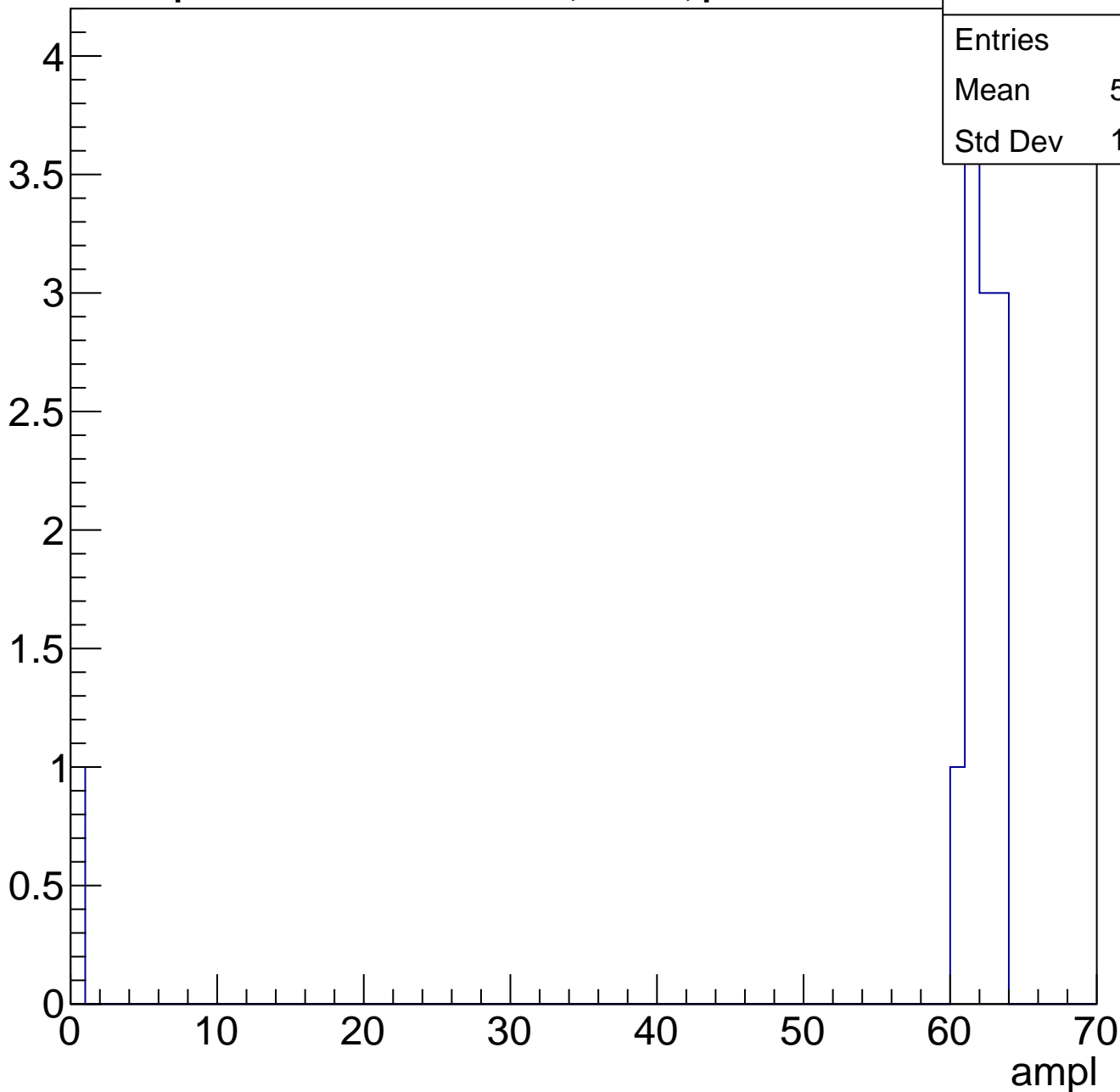
Entries	36
Mean	59.72
Std Dev	2.735



# B1L102S, U20-ch76, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U20-ch76, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	11
Std Dev	11

# B1L102S, U20-ch77, adc0

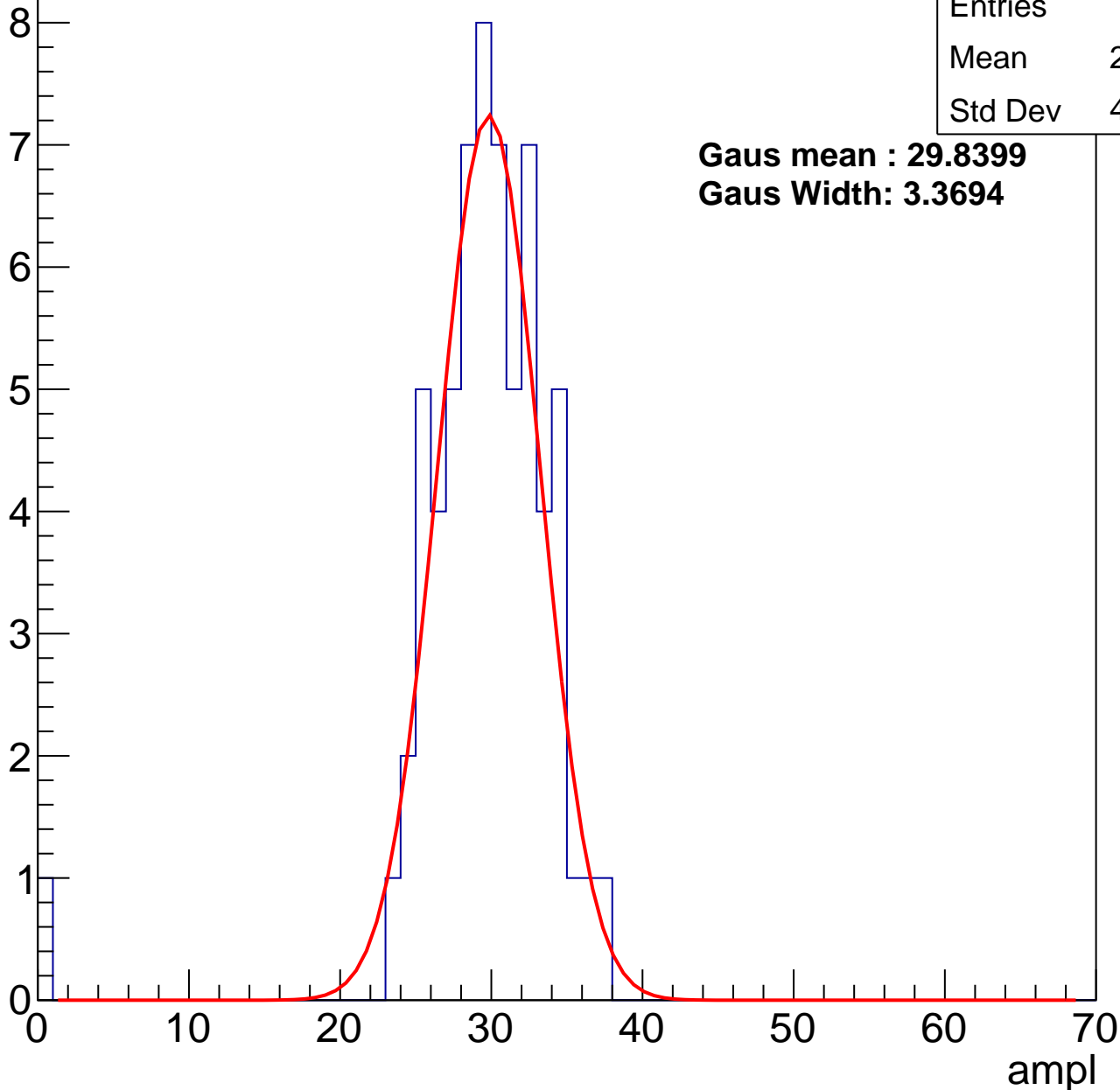
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	29.09
Std Dev	4.837

**Gaus mean : 29.8399**

**Gaus Width: 3.3694**



# B1L102S, U20-ch77, adc1

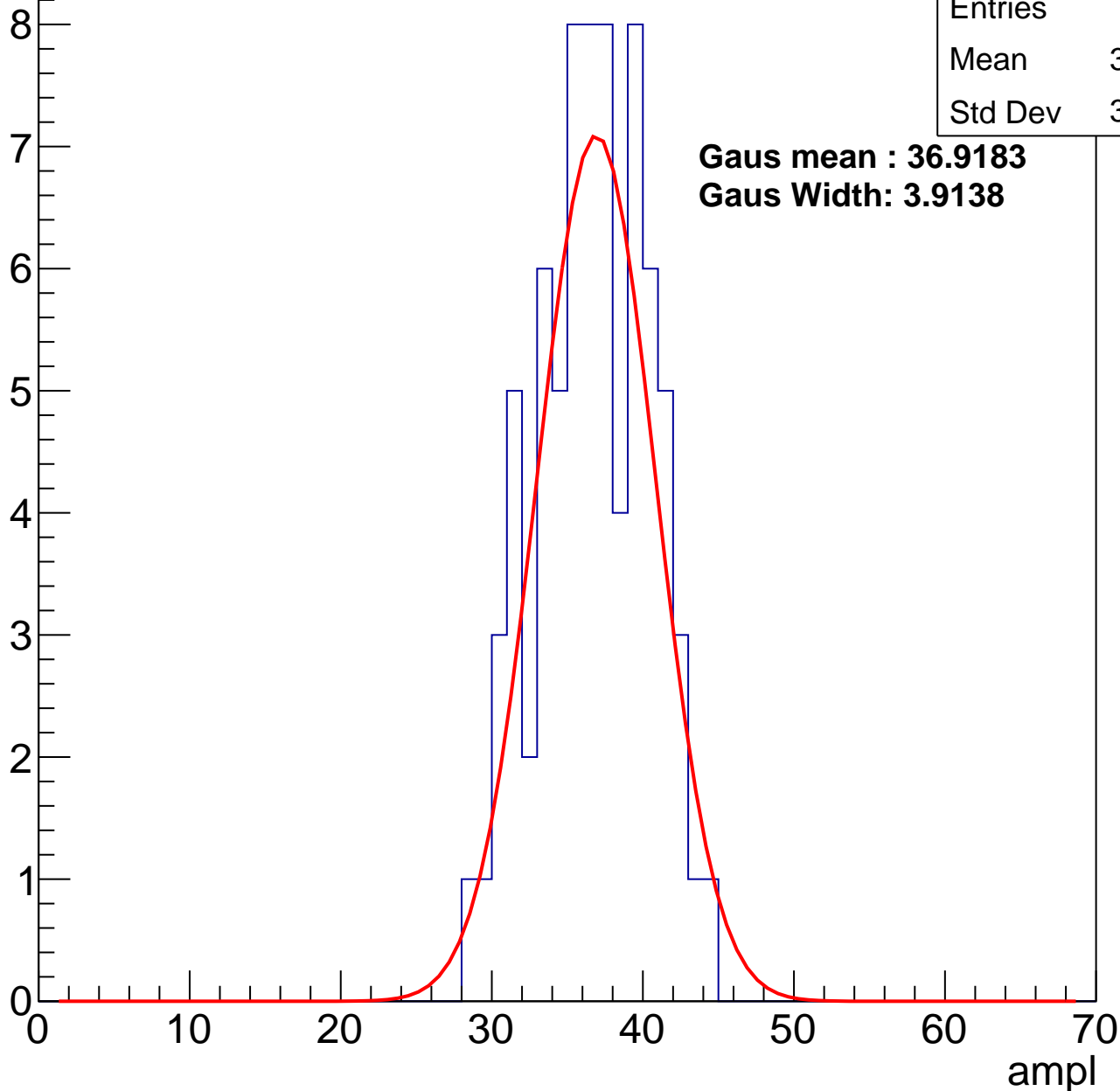
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	36.27
Std Dev	3.638

**Gaus mean : 36.9183**

**Gaus Width: 3.9138**



# B1L102S, U20-ch77, adc2

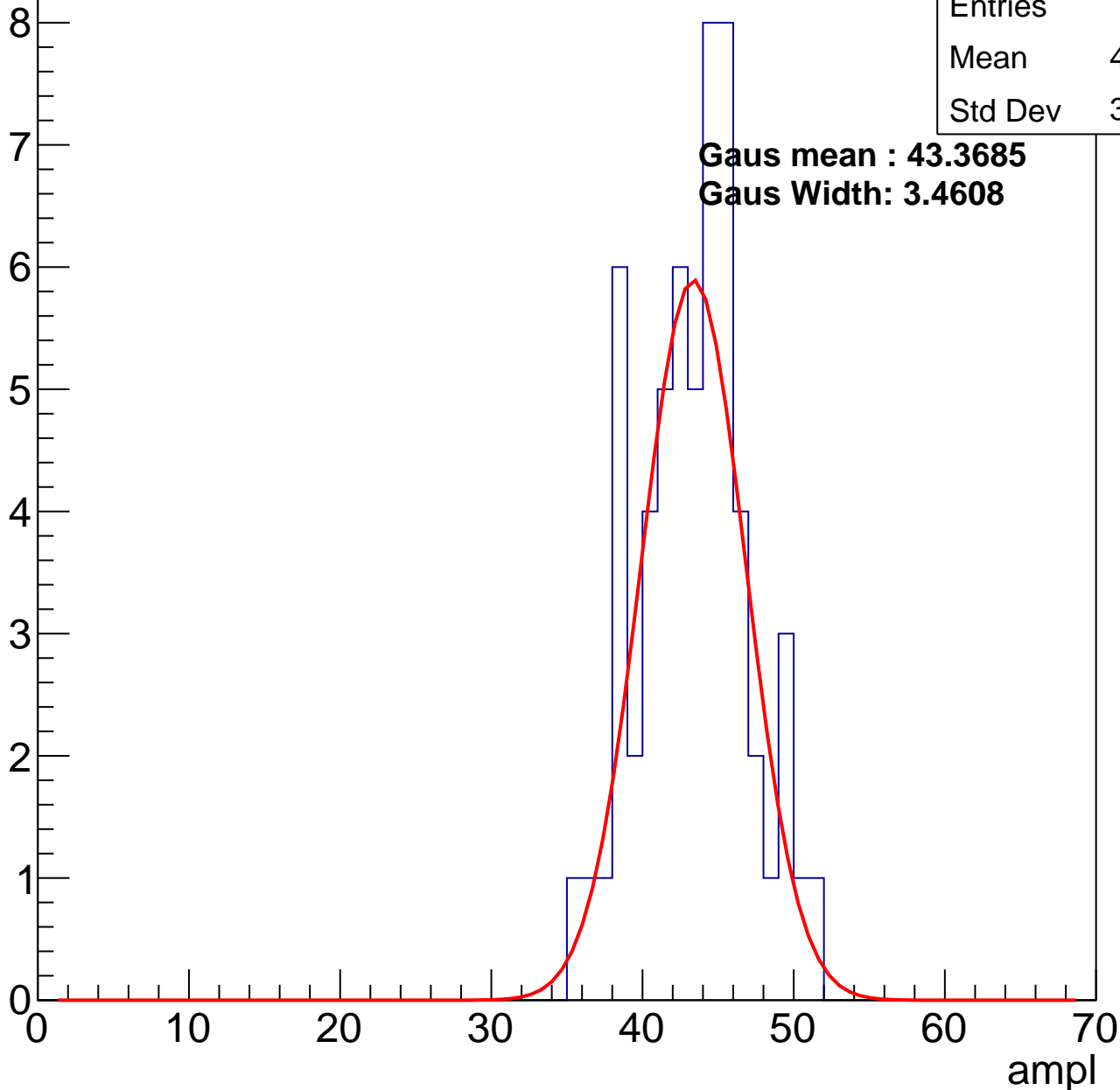
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	42.92
Std Dev	3.557

**Gaus mean : 43.3685**

**Gaus Width: 3.4608**

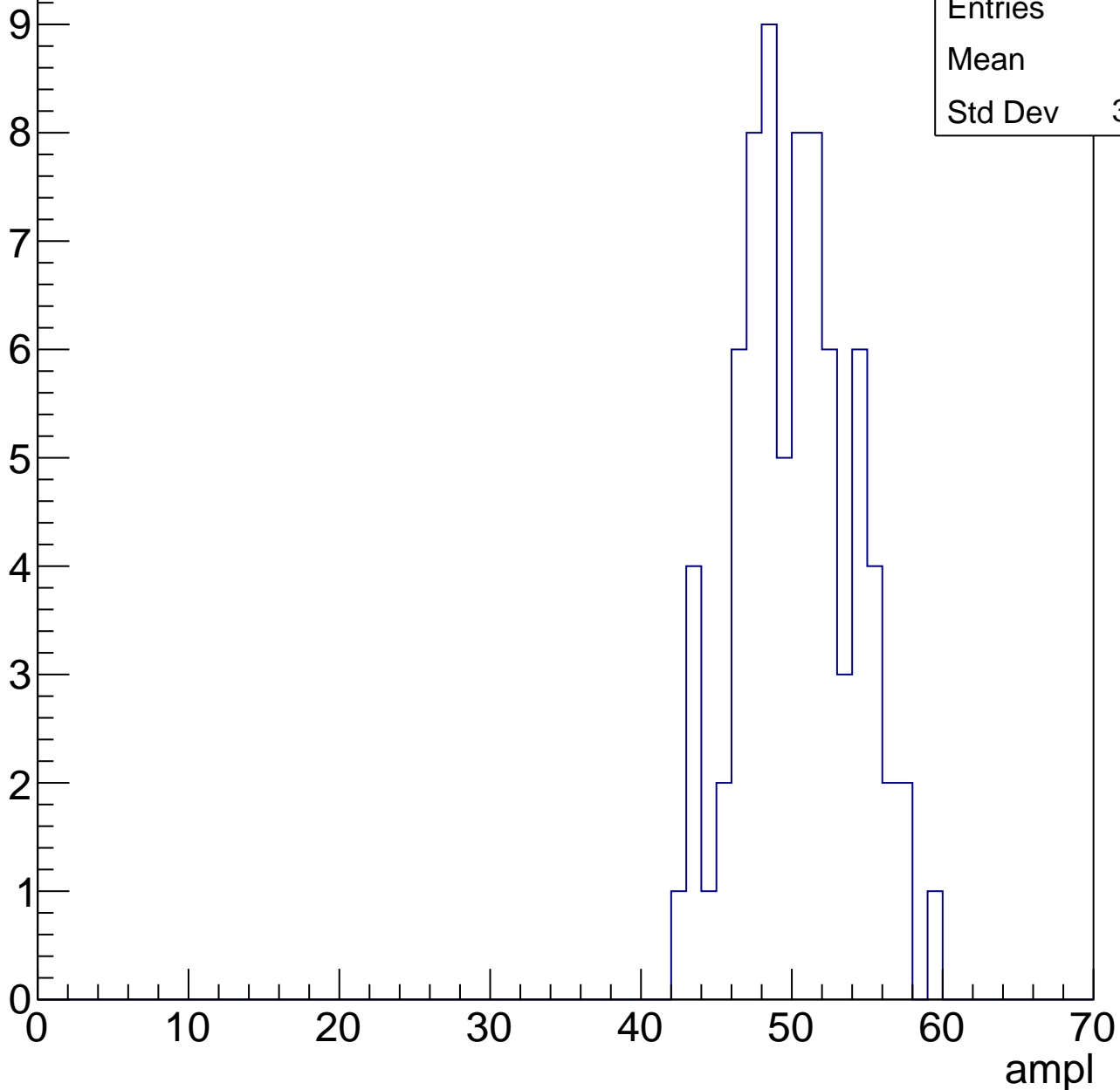


# B1L102S, U20-ch77, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	49.8
Std Dev	3.731

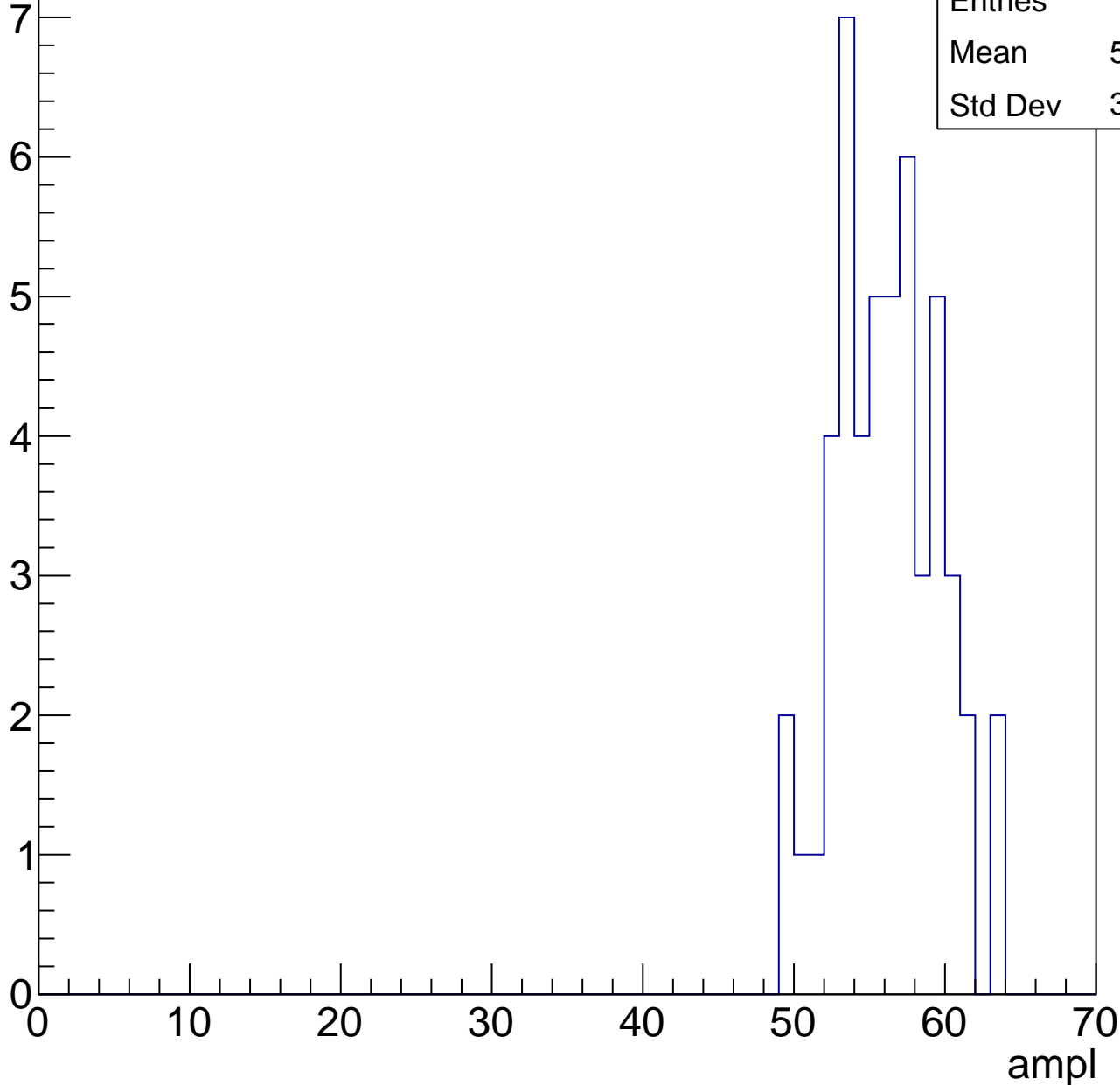


# B1L102S, U20-ch77, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	55.76
Std Dev	3.356

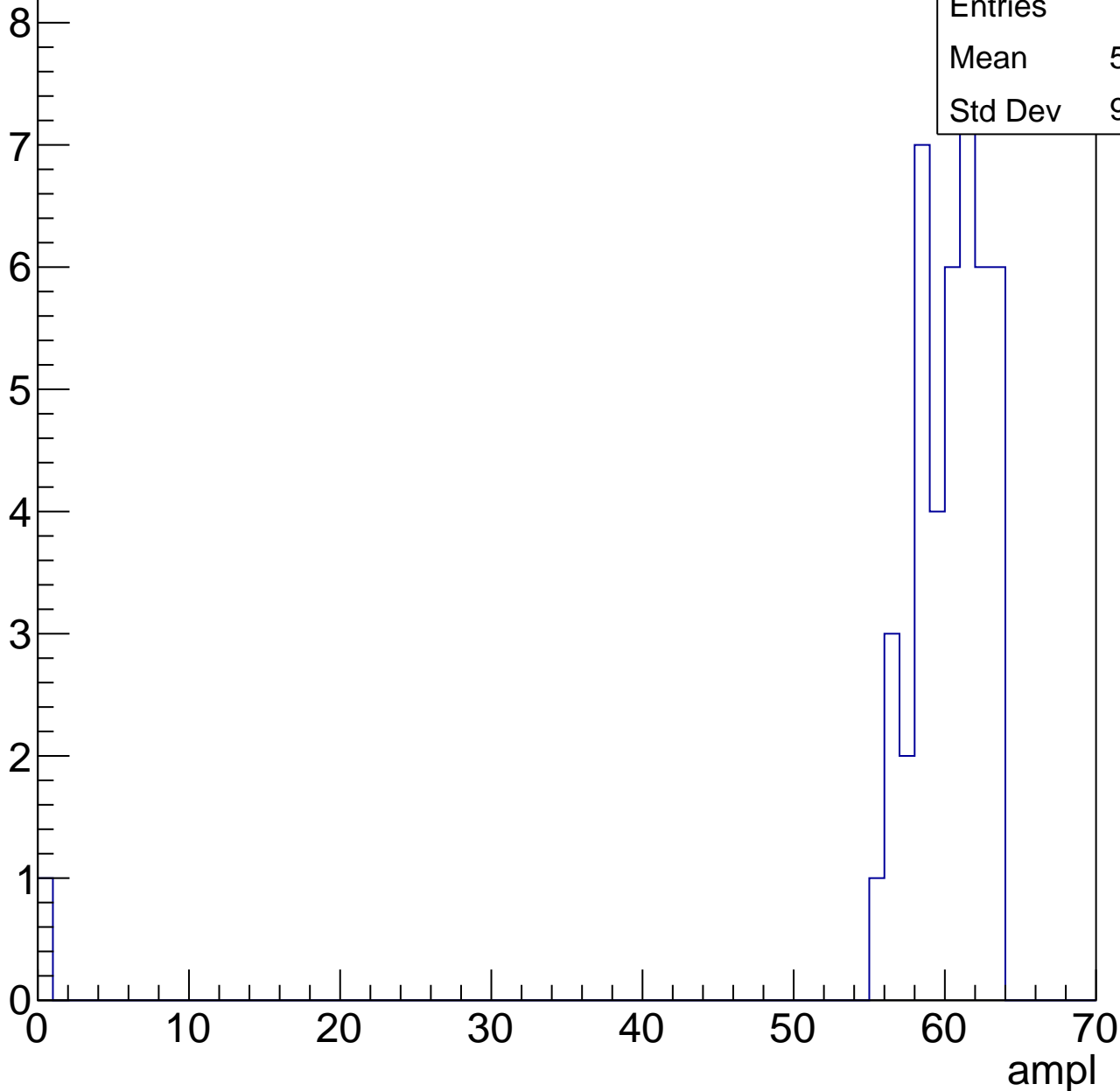


# B1L102S, U20-ch77, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

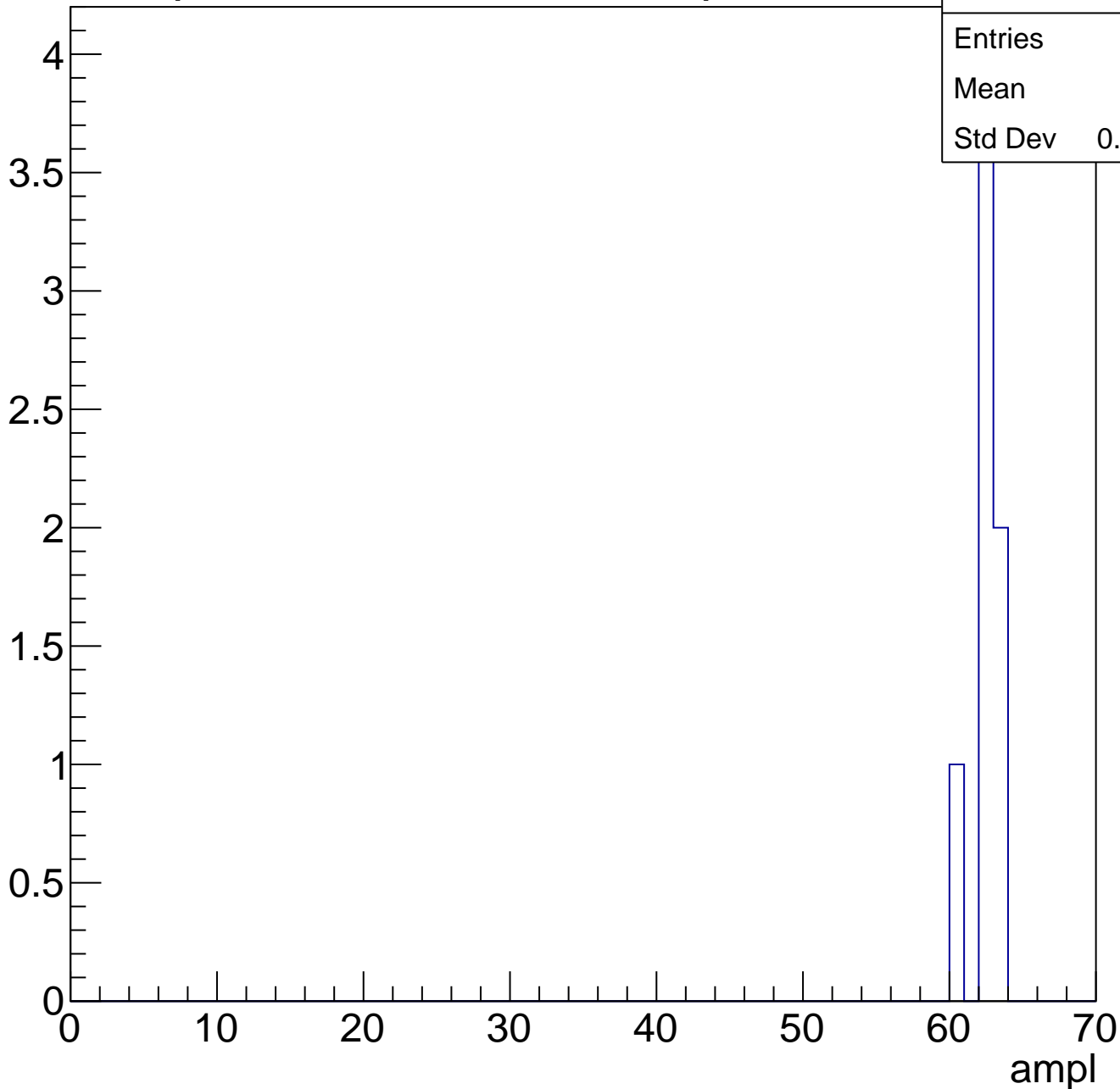
Entries	44
Mean	58.57
Std Dev	9.193



# B1L102S, U20-ch77, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U20-ch77, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch78, adc0

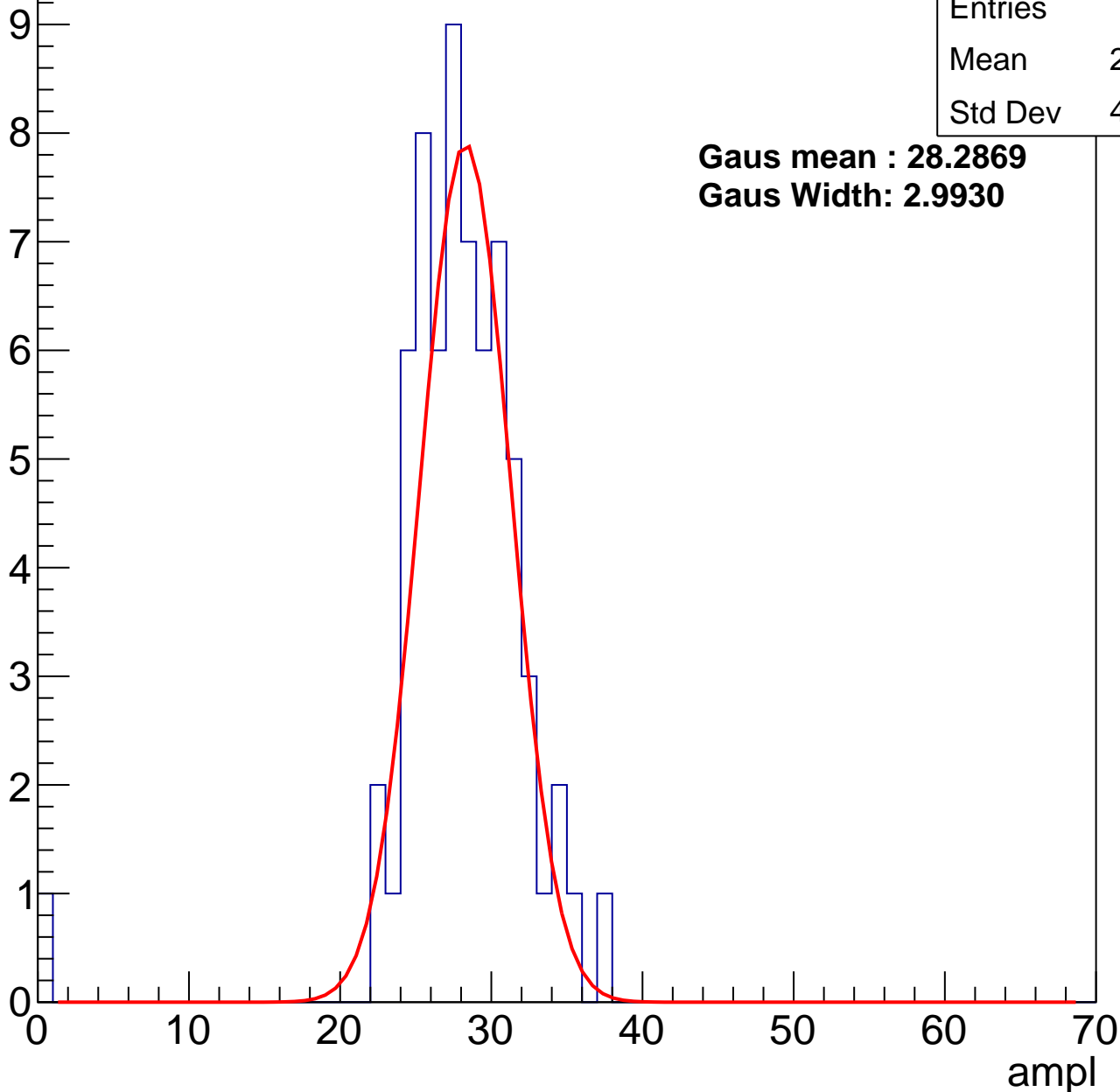
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	27.48
Std Dev	4.636

**Gaus mean : 28.2869**

**Gaus Width: 2.9930**



# B1L102S, U20-ch78, adc1

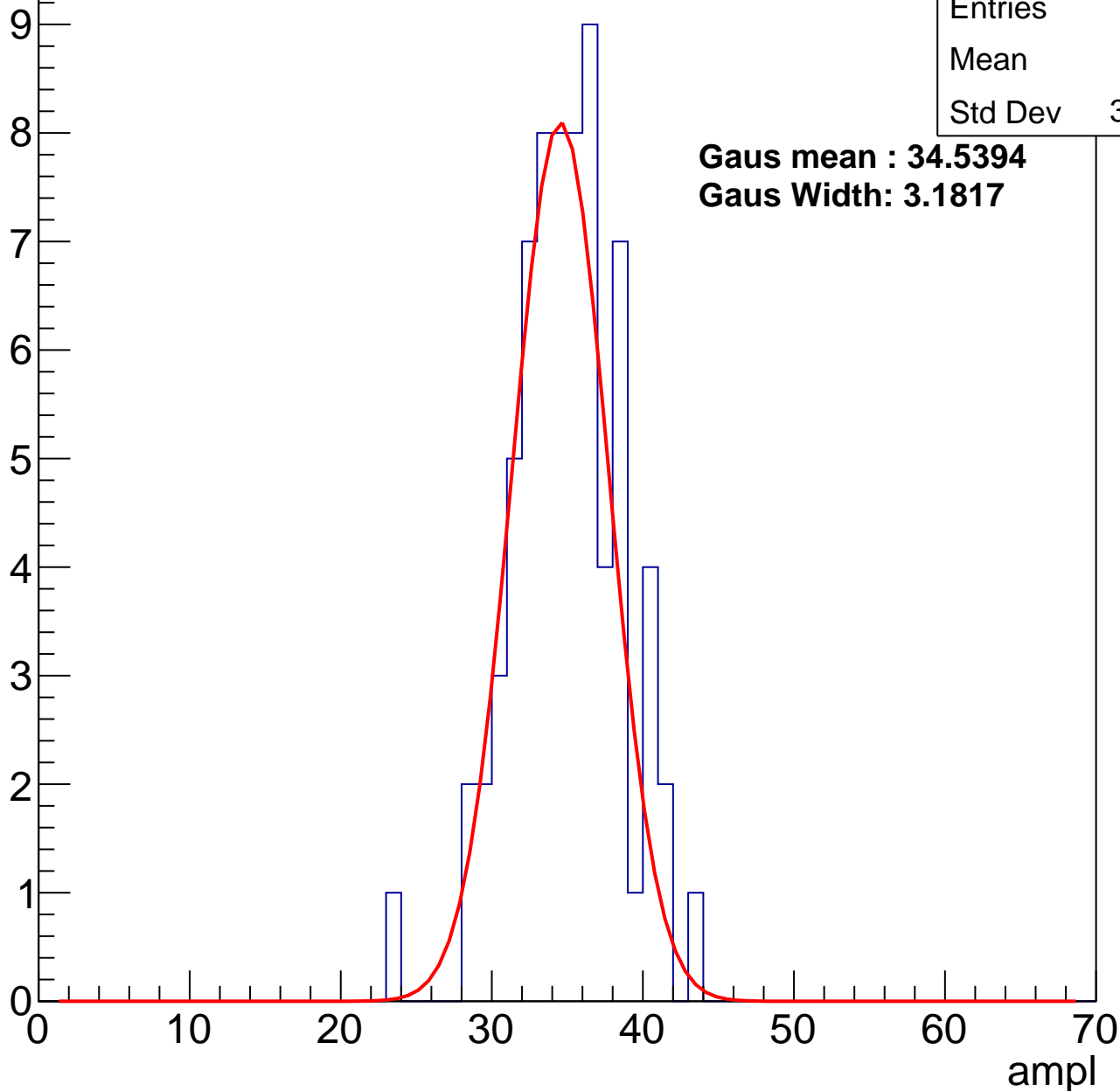
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	34.5
Std Dev	3.524

**Gaus mean : 34.5394**

**Gaus Width: 3.1817**



# B1L102S, U20-ch78, adc2

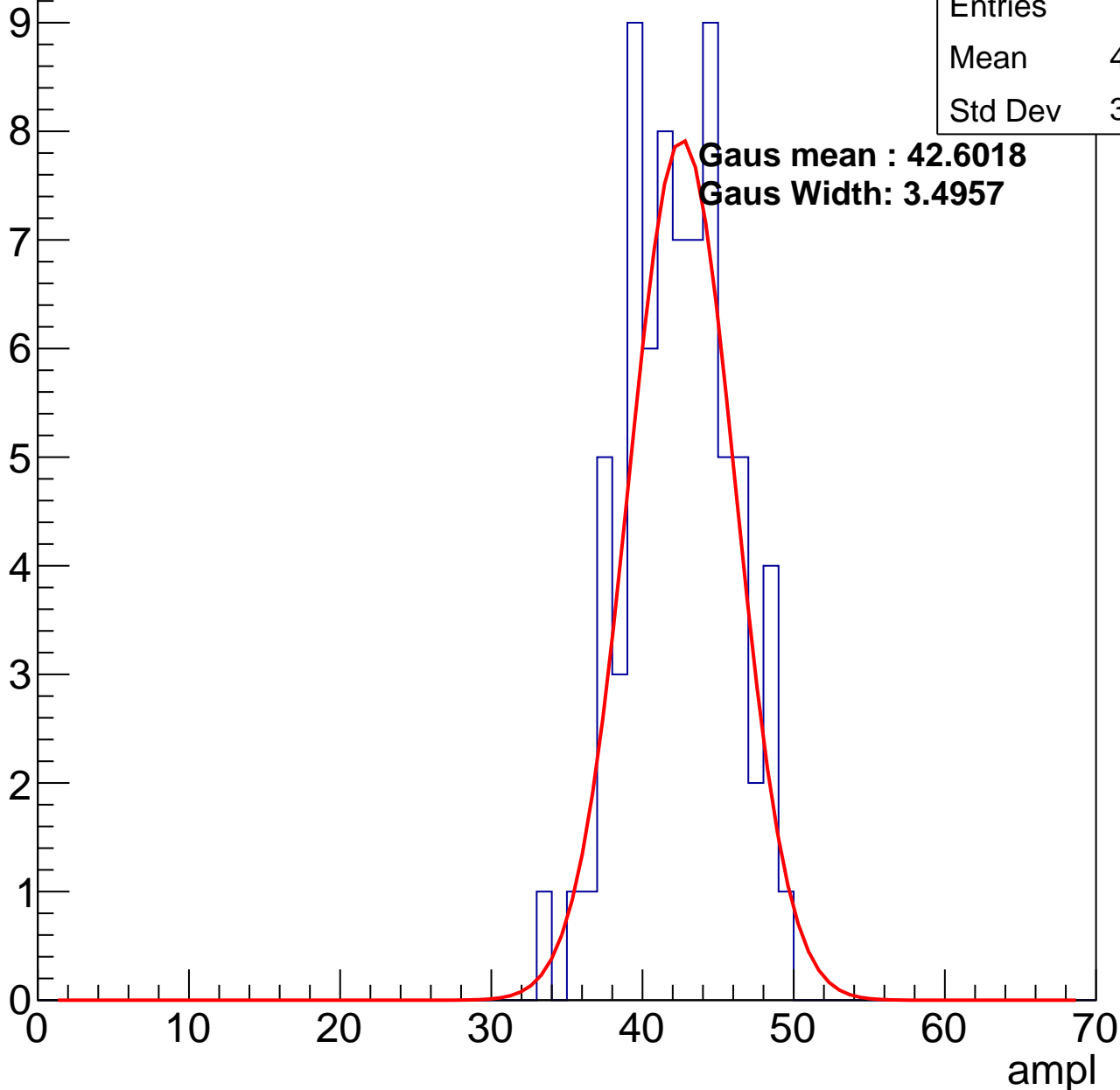
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	41.93
Std Dev	3.414

**Gaus mean : 42.6018**

**Gaus Width: 3.4957**

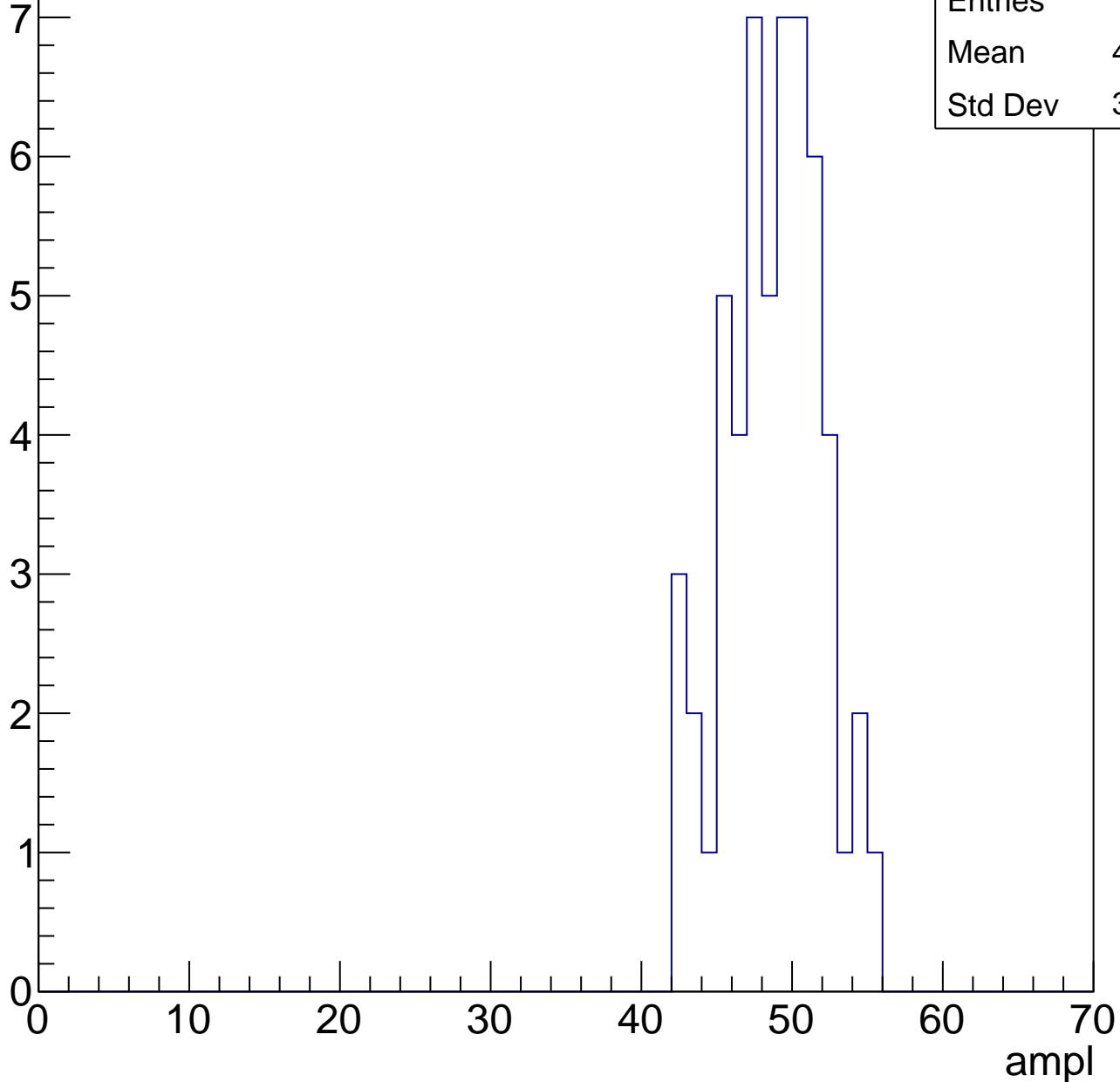


# B1L102S, U20-ch78, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

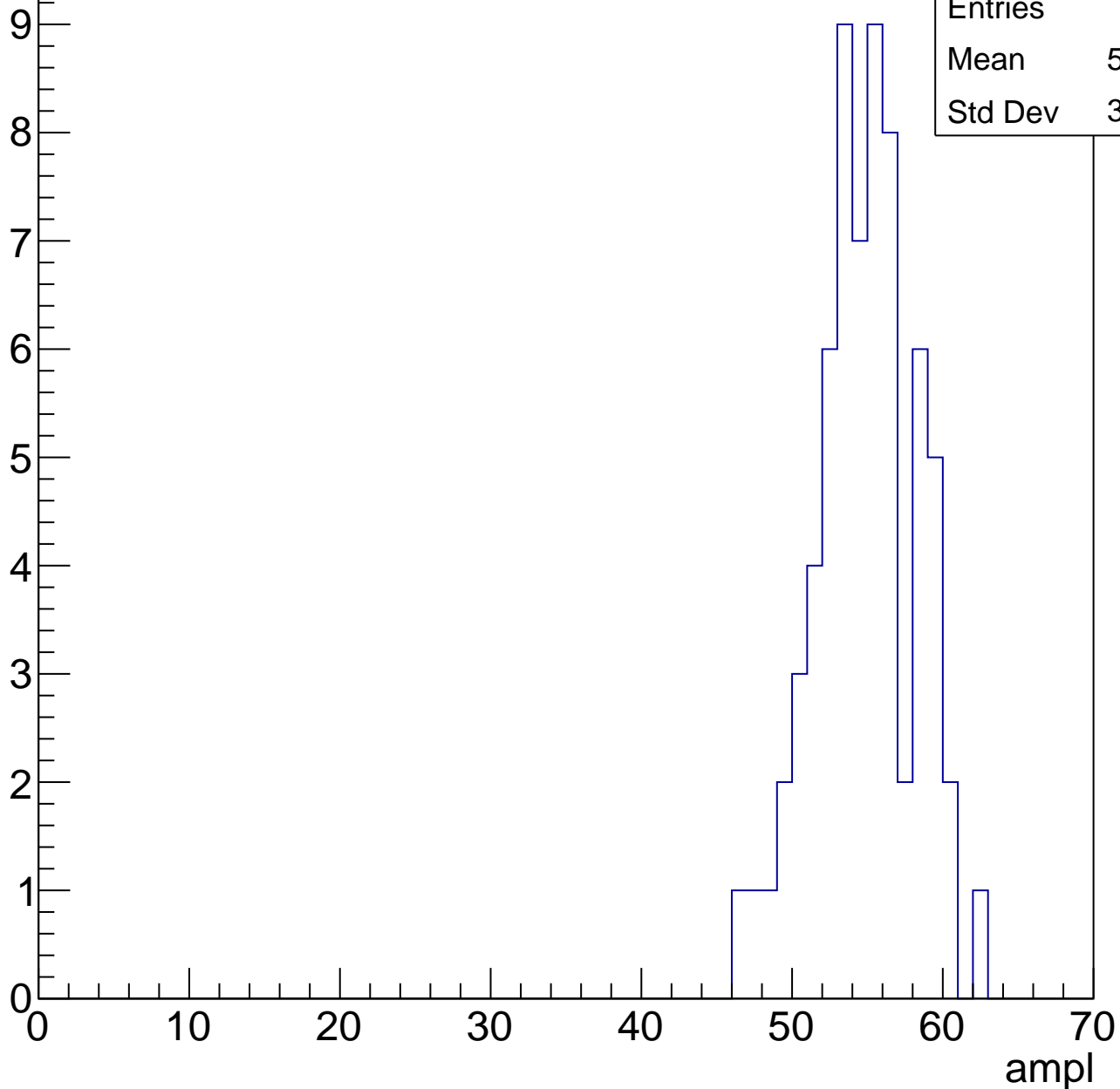
Entries	55
Mean	48.31
Std Dev	3.121



# B1L102S, U20-ch78, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

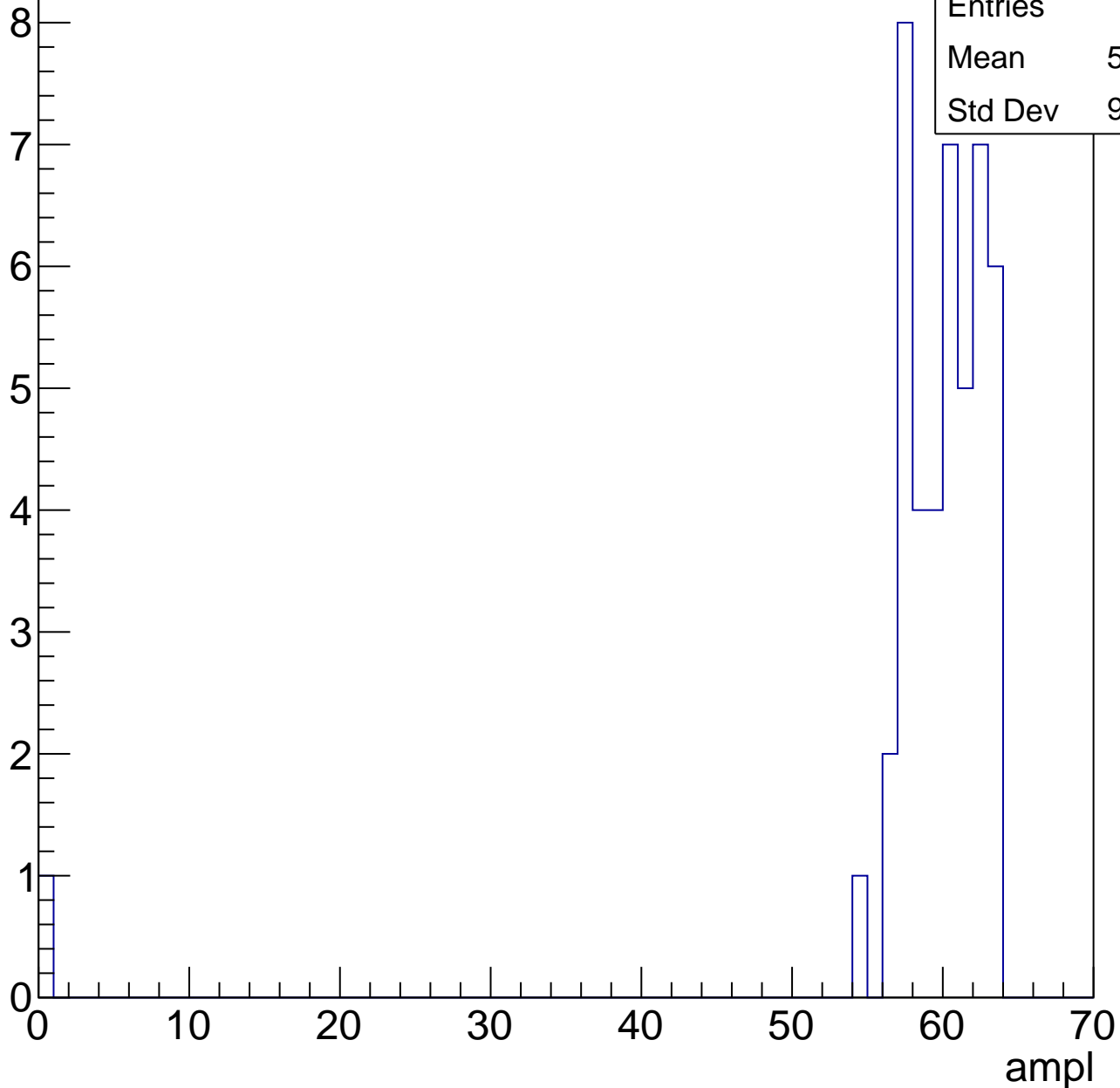


Entries	67
Mean	54.36
Std Dev	3.286

# B1L102S, U20-ch78, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

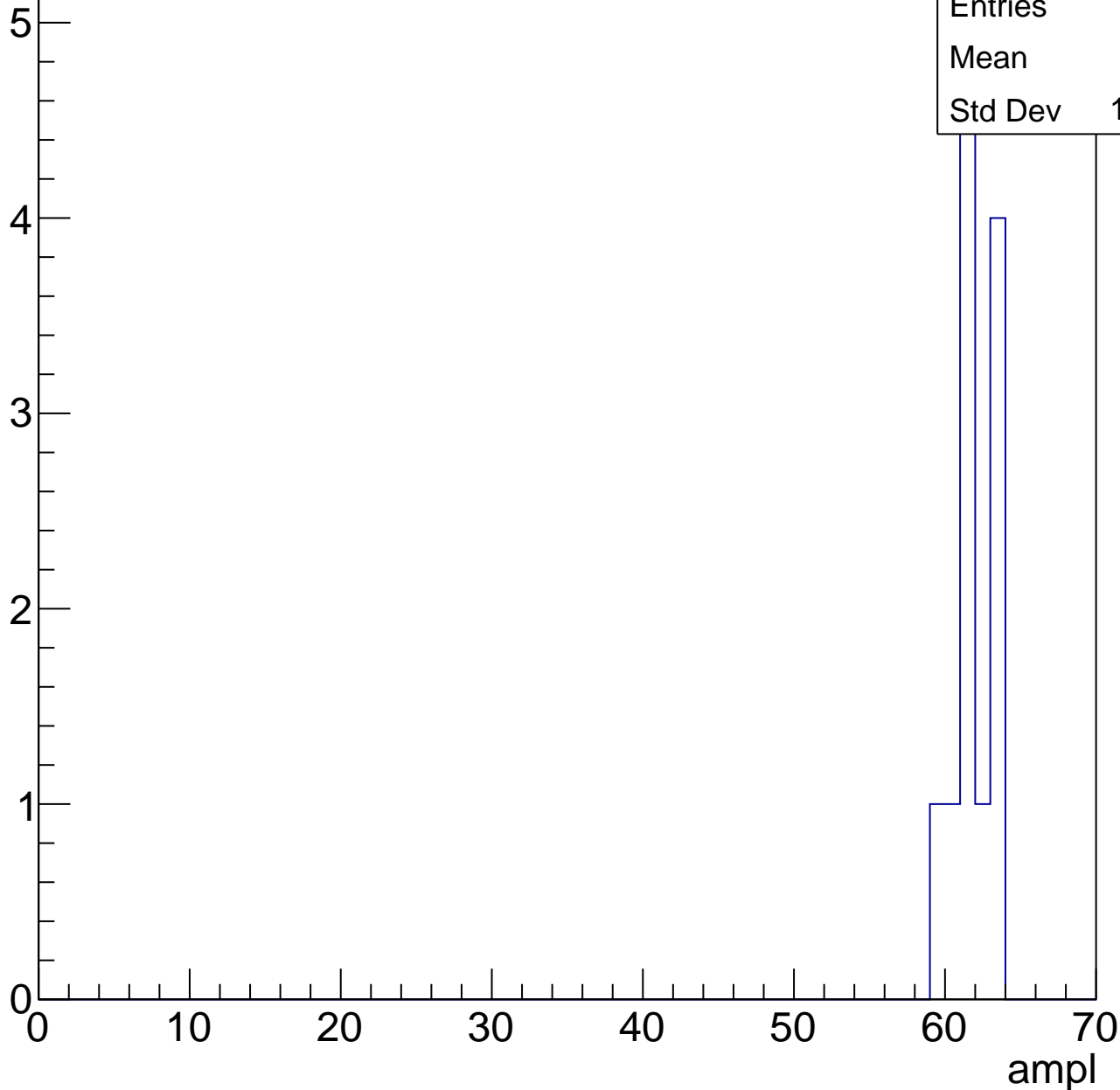


# B1L102S, U20-ch78, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	12
Mean	61.5
Std Dev	1.258





# B1L102S, U20-ch78, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch79, adc0

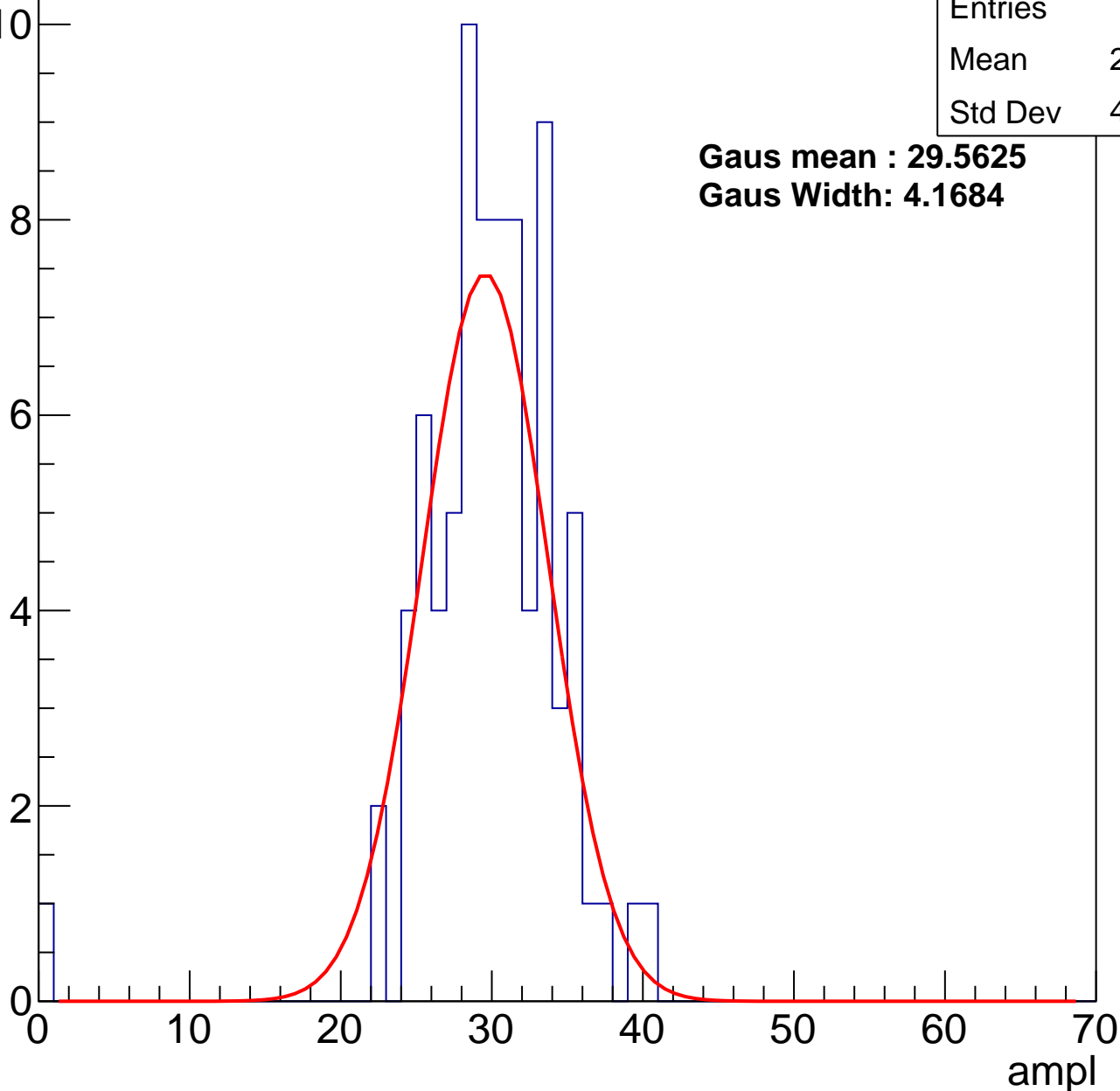
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	81
Mean	29.42
Std Dev	4.964

**Gaus mean : 29.5625**

**Gaus Width: 4.1684**



# B1L102S, U20-ch79, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	63
Mean	36.51
Std Dev	3.375

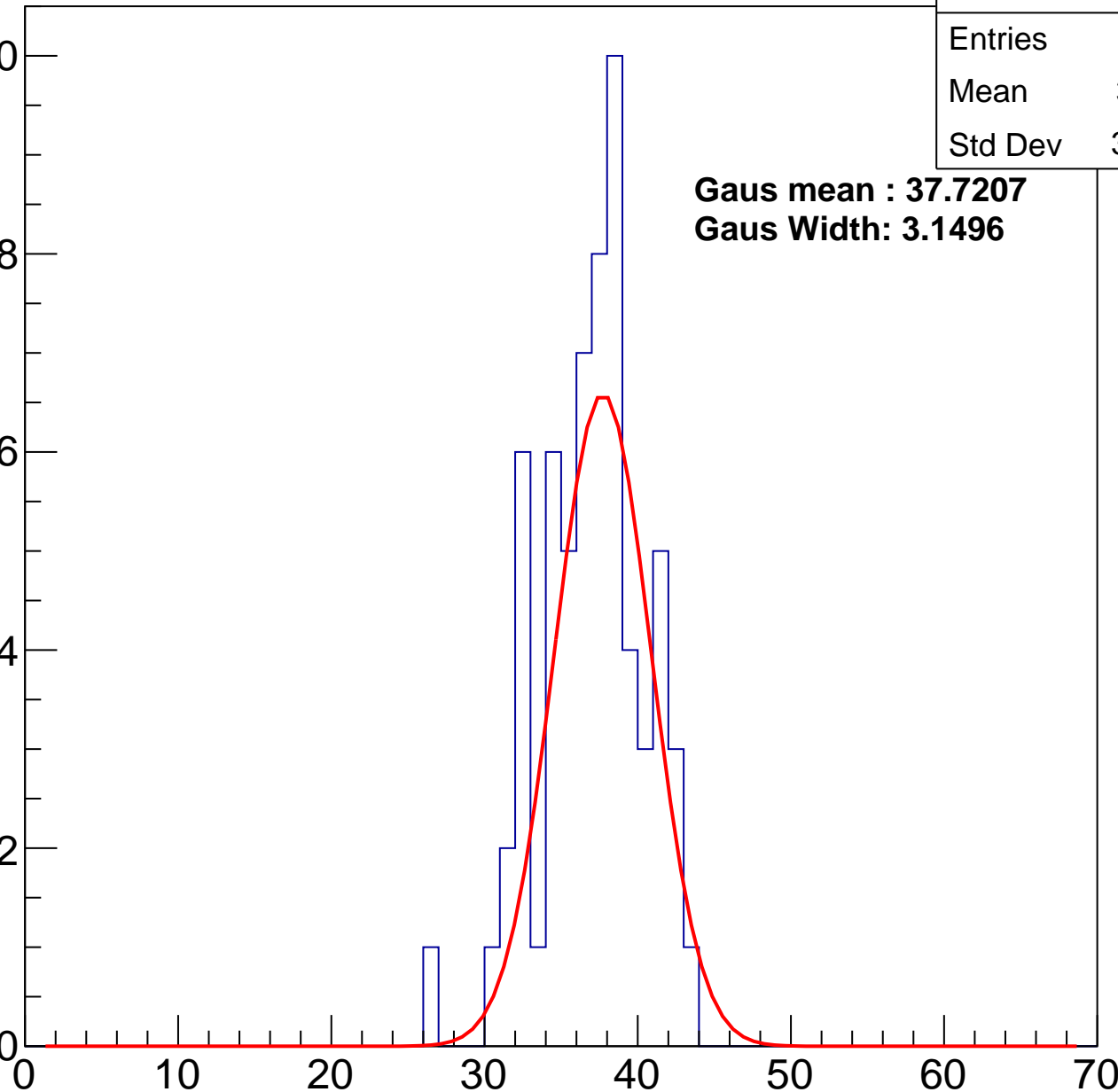
**Gaus mean : 37.7207**

**Gaus Width: 3.1496**

Entry

10  
8  
6  
4  
2  
0

ampl



# B1L102S, U20-ch79, adc2

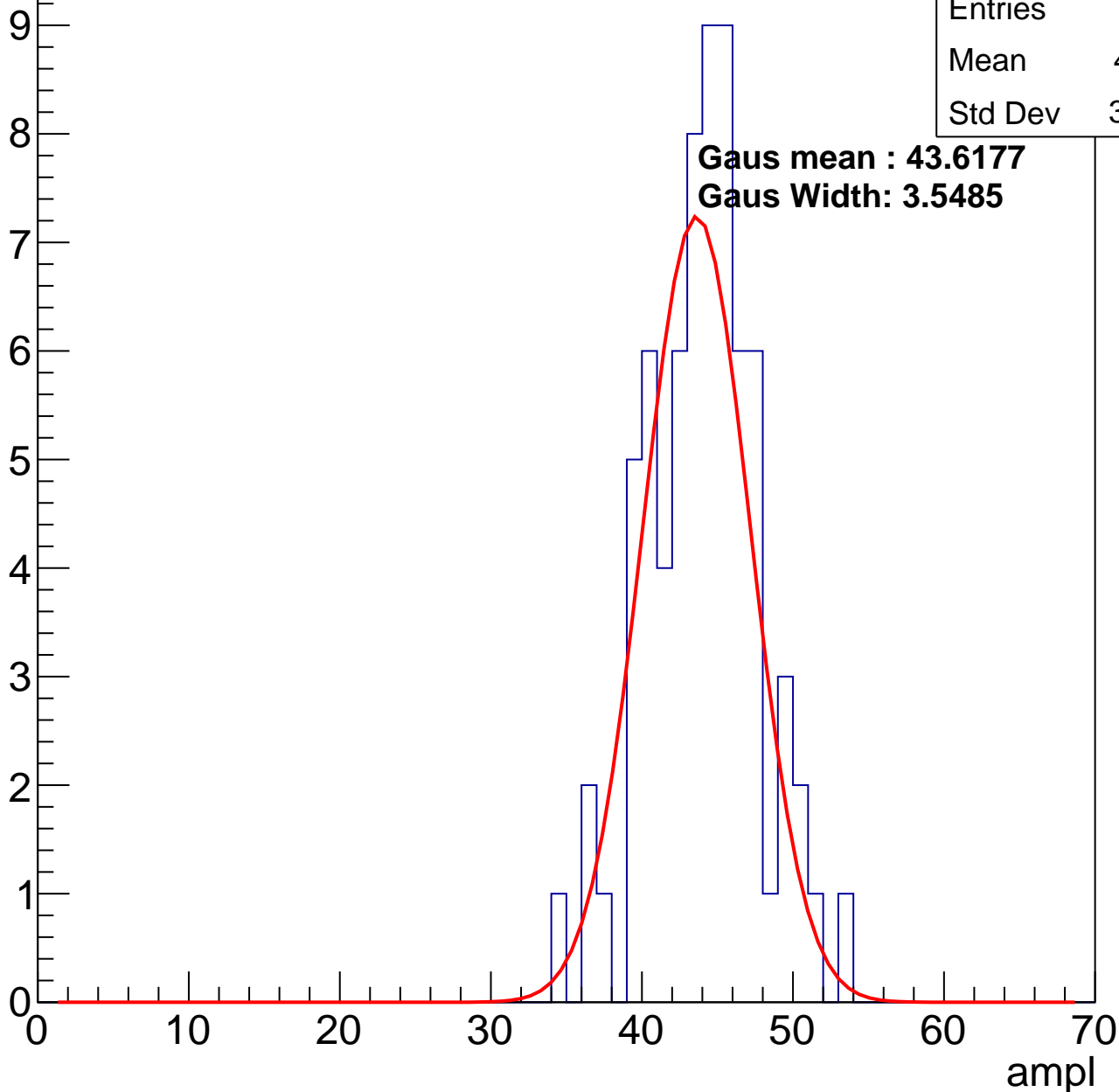
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	43.61
Std Dev	3.629

**Gaus mean : 43.6177**

**Gaus Width: 3.5485**

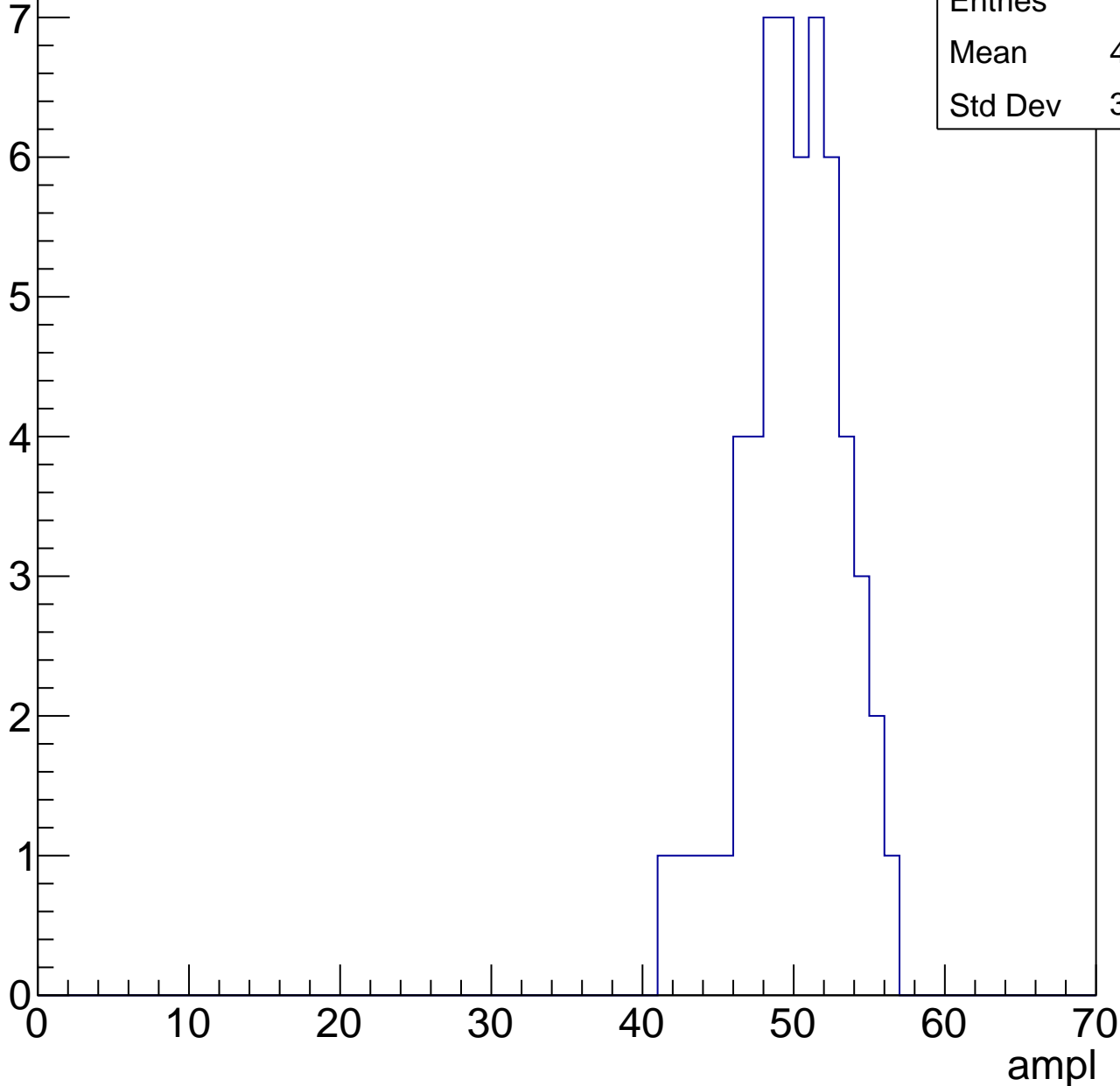


# B1L102S, U20-ch79, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	49.55
Std Dev	3.218

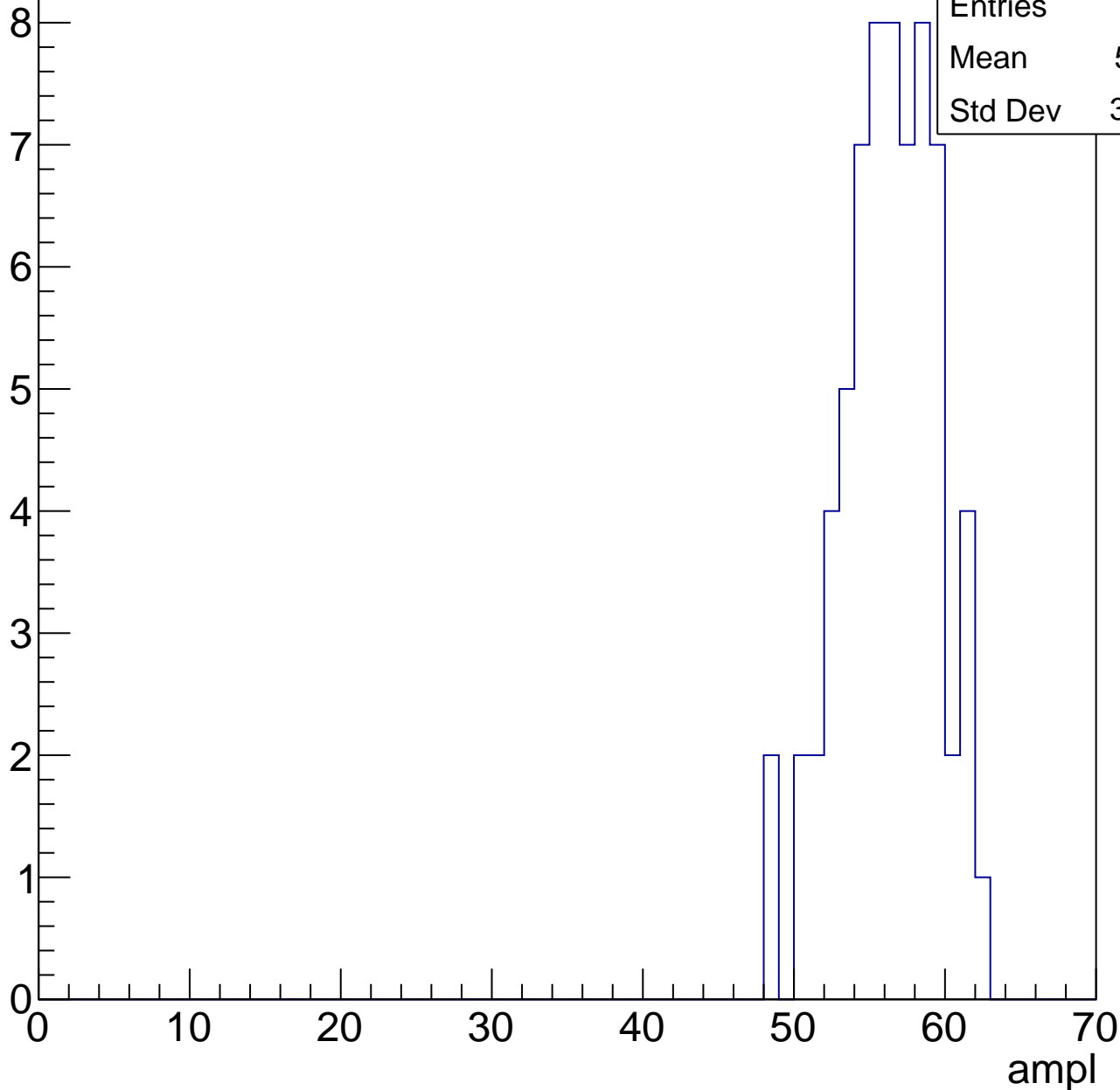


# B1L102S, U20-ch79, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

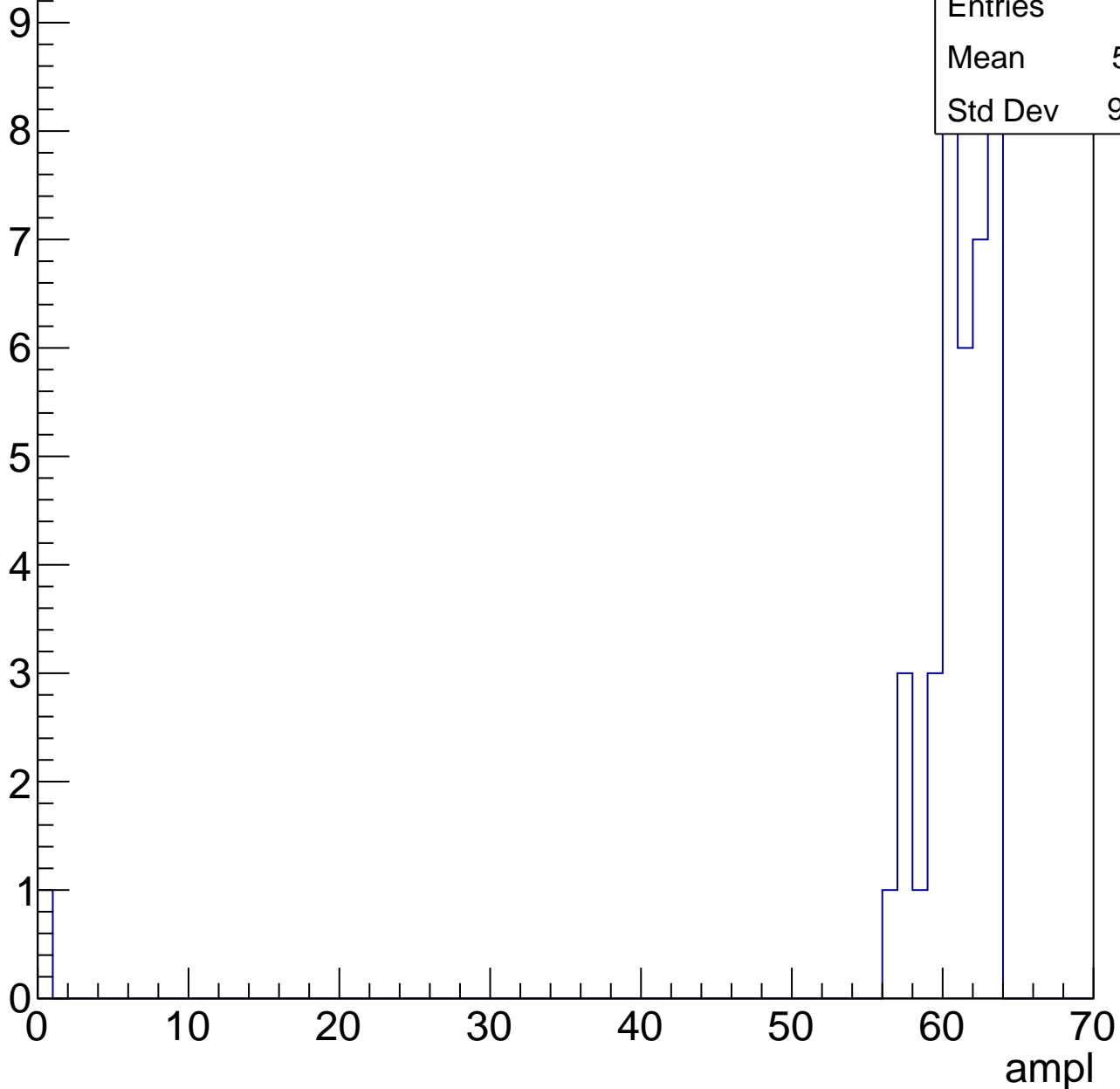
Entries	67
Mean	55.81
Std Dev	3.144



# B1L102S, U20-ch79, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

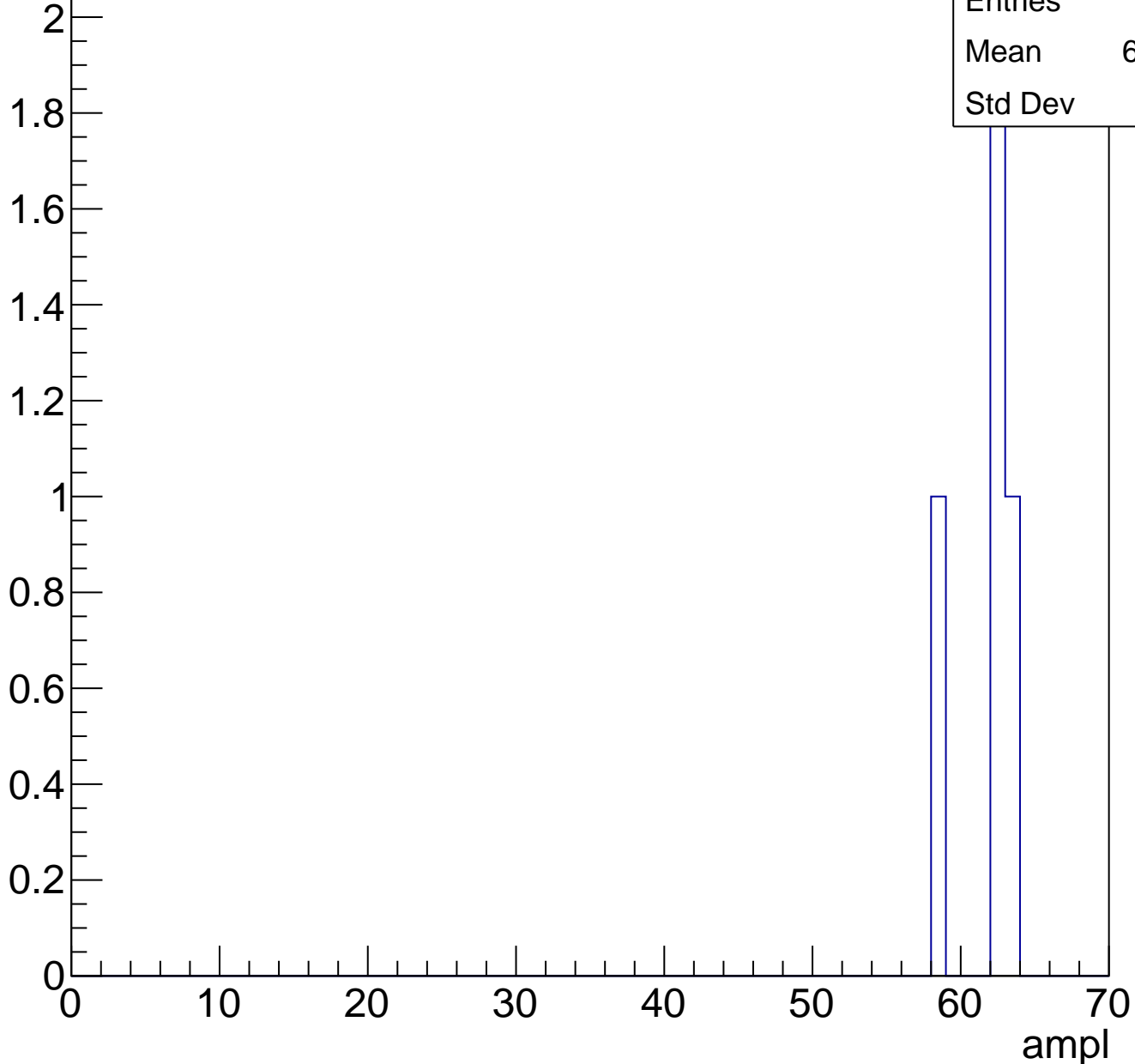


Entries	39
Mean	59.21
Std Dev	9.793

# B1L102S, U20-ch79, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

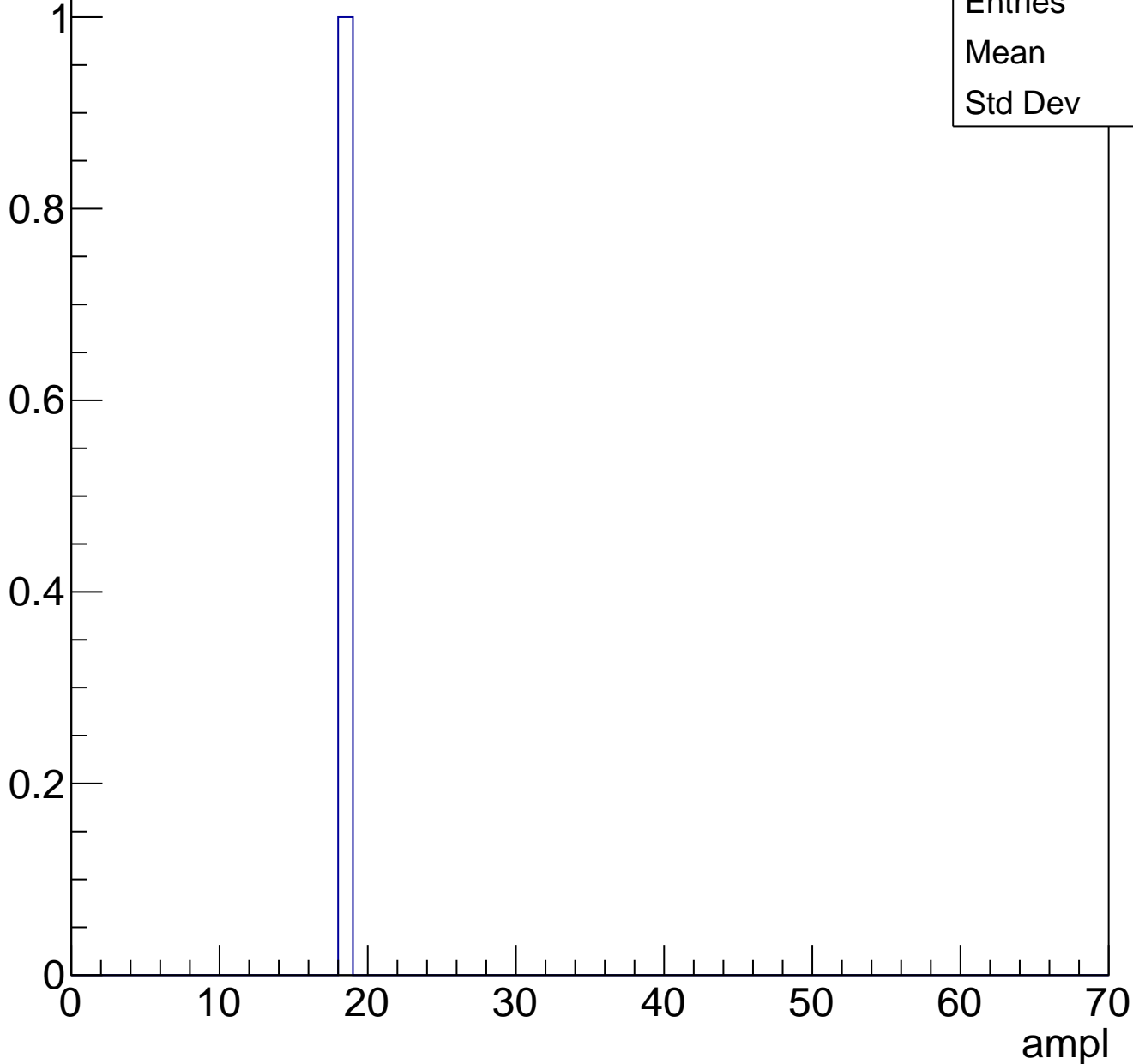




# B1L102S, U20-ch79, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch80, adc0

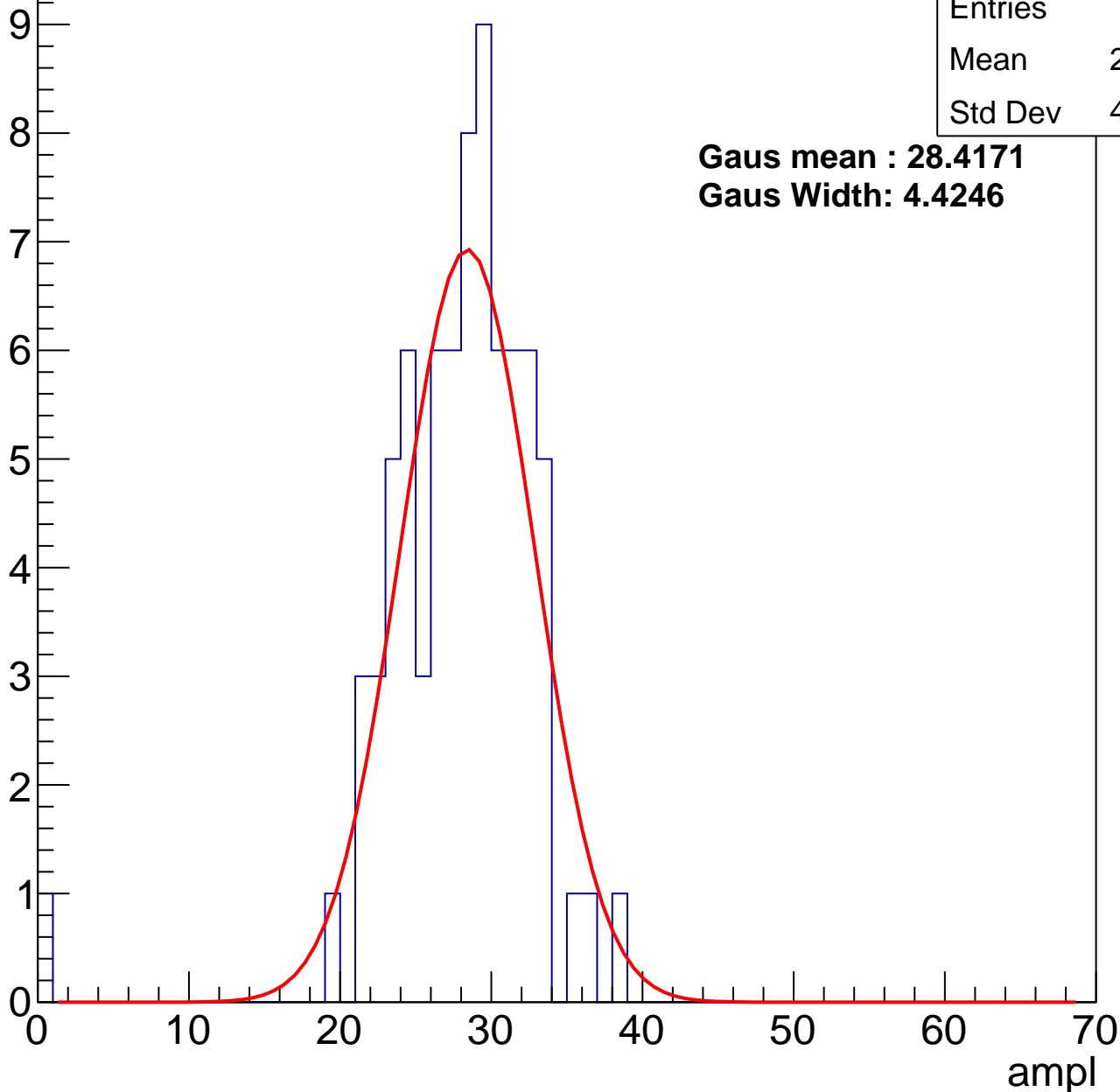
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	27.49
Std Dev	4.966

**Gaus mean : 28.4171**

**Gaus Width: 4.4246**



# B1L102S, U20-ch80, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	66
Mean	34.5
Std Dev	4.124

**Gaus mean : 35.7217**

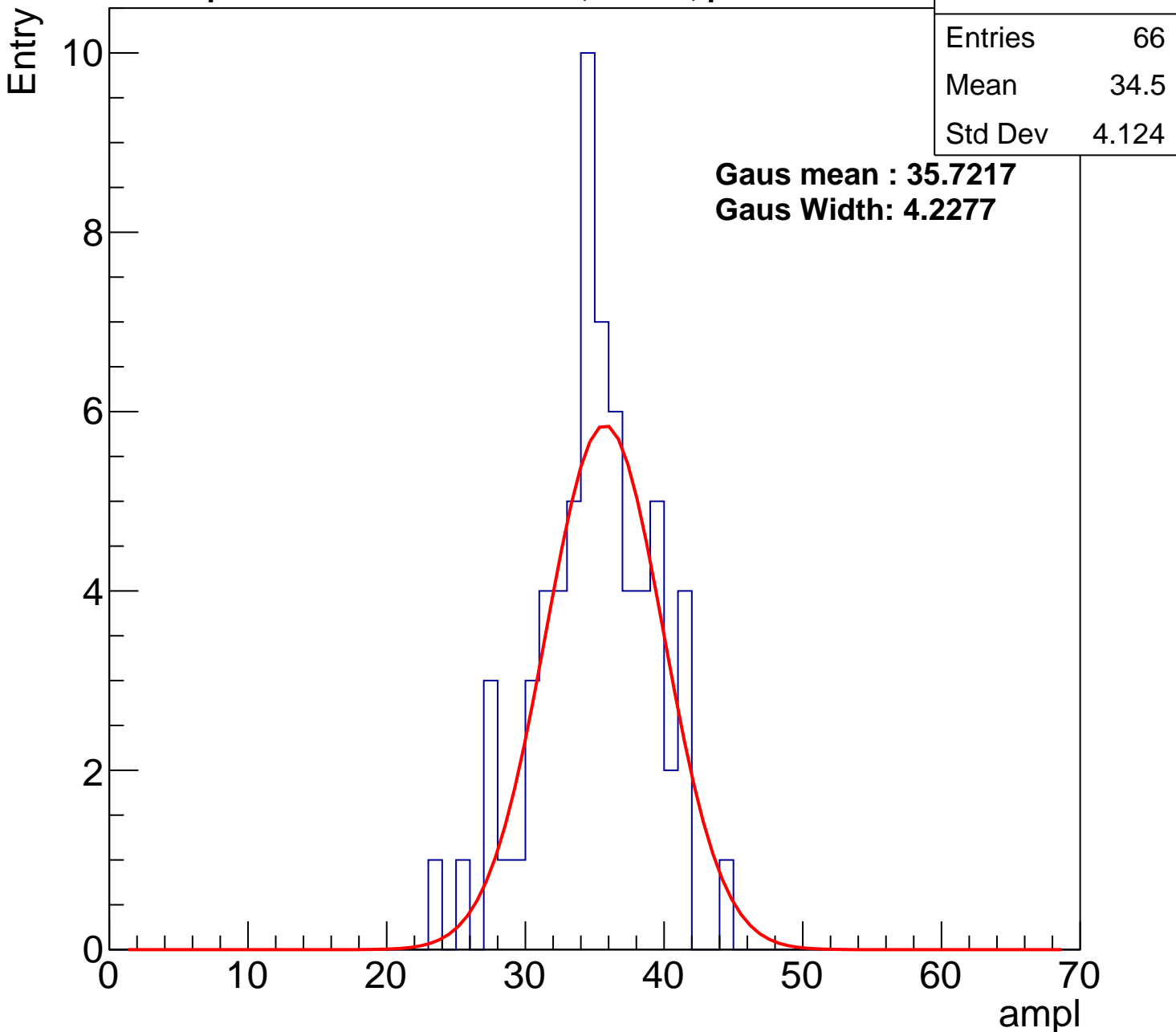
**Gaus Width: 4.2277**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U20-ch80, adc2

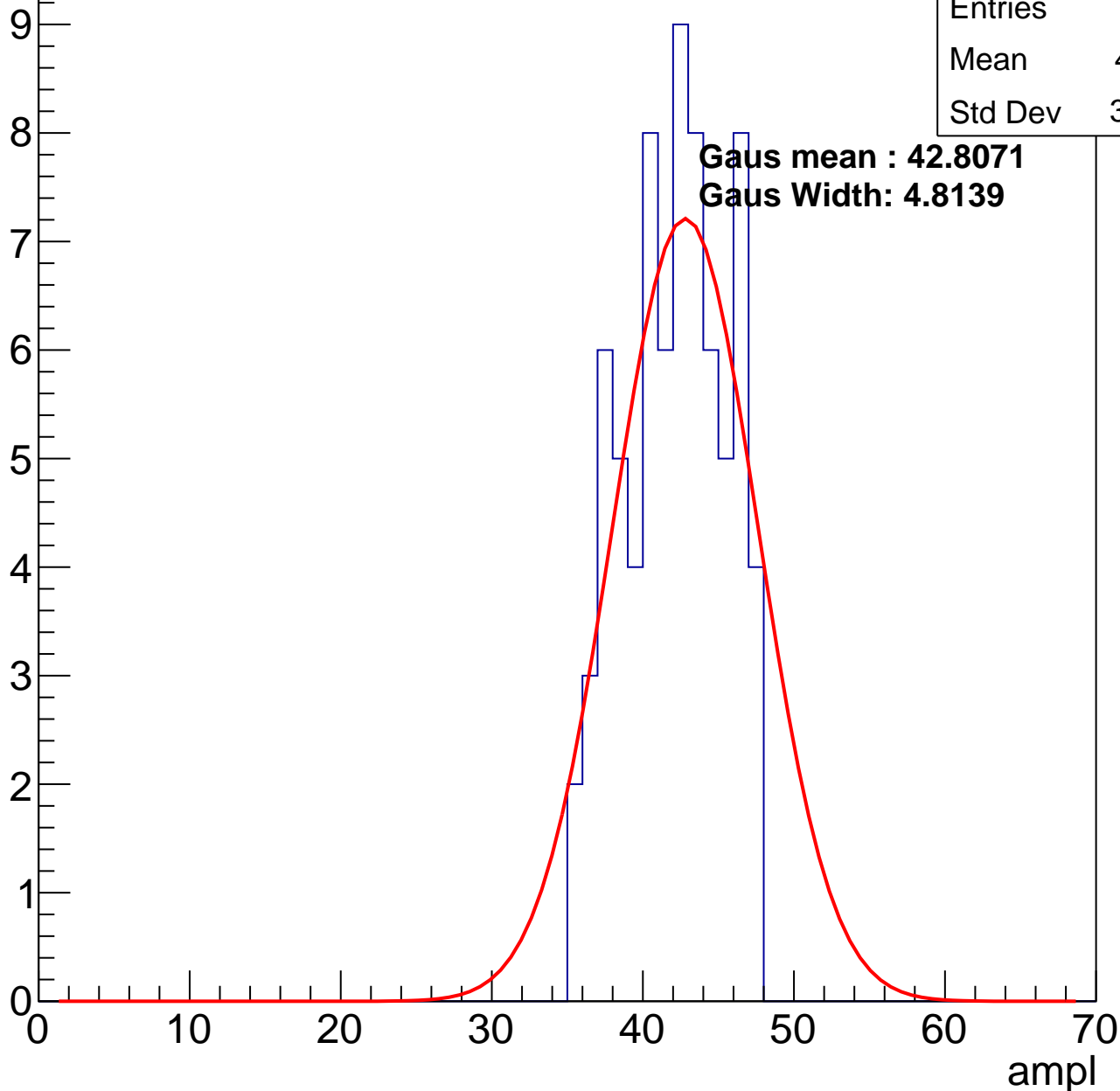
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	41.61
Std Dev	3.295

**Gaus mean : 42.8071**

**Gaus Width: 4.8139**



# B1L102S, U20-ch80, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

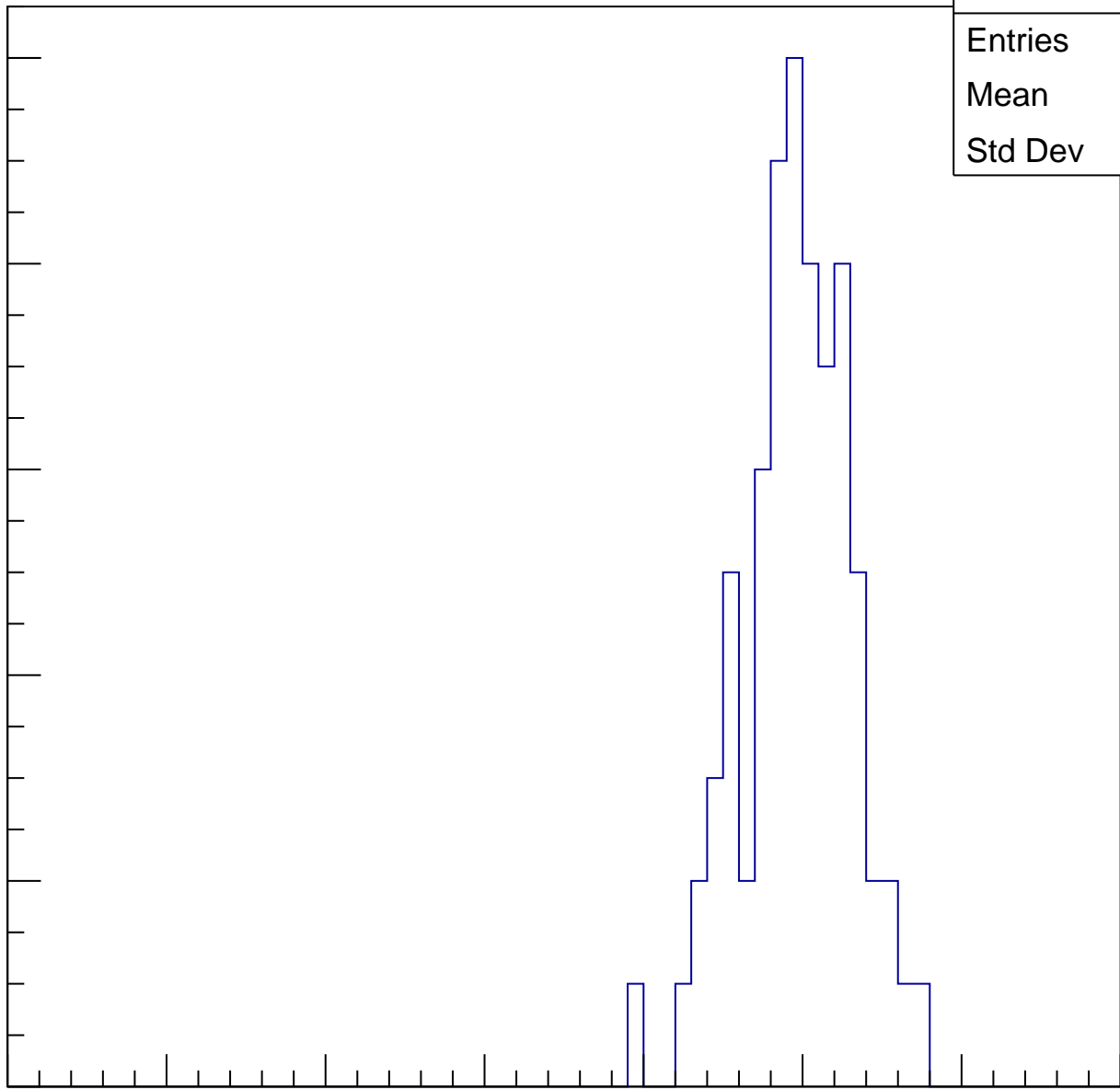
Entries	73
Mean	49.16
Std Dev	3.408

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

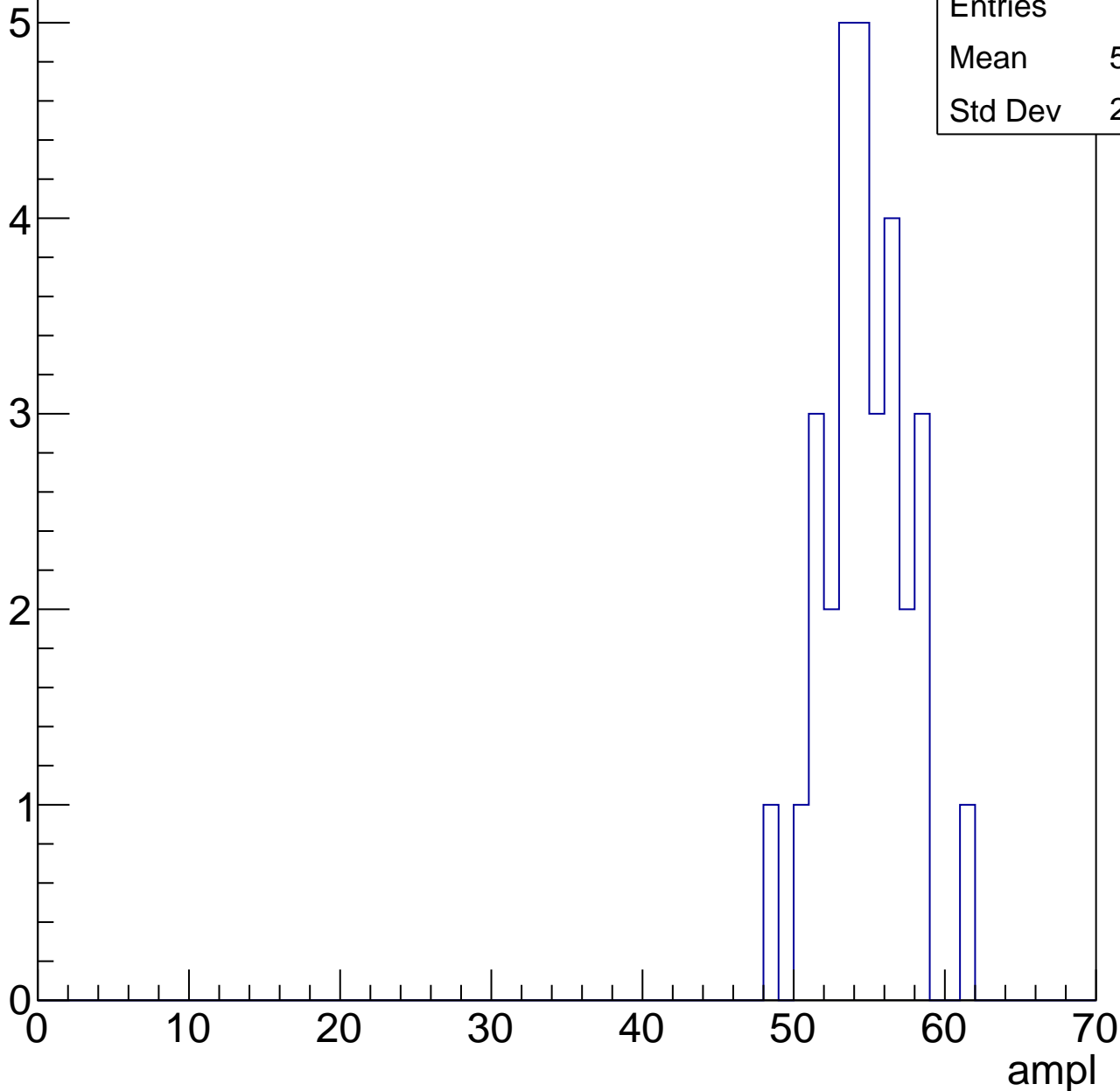


# B1L102S, U20-ch80, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	30
Mean	54.27
Std Dev	2.732



# B1L102S, U20-ch80, adc5

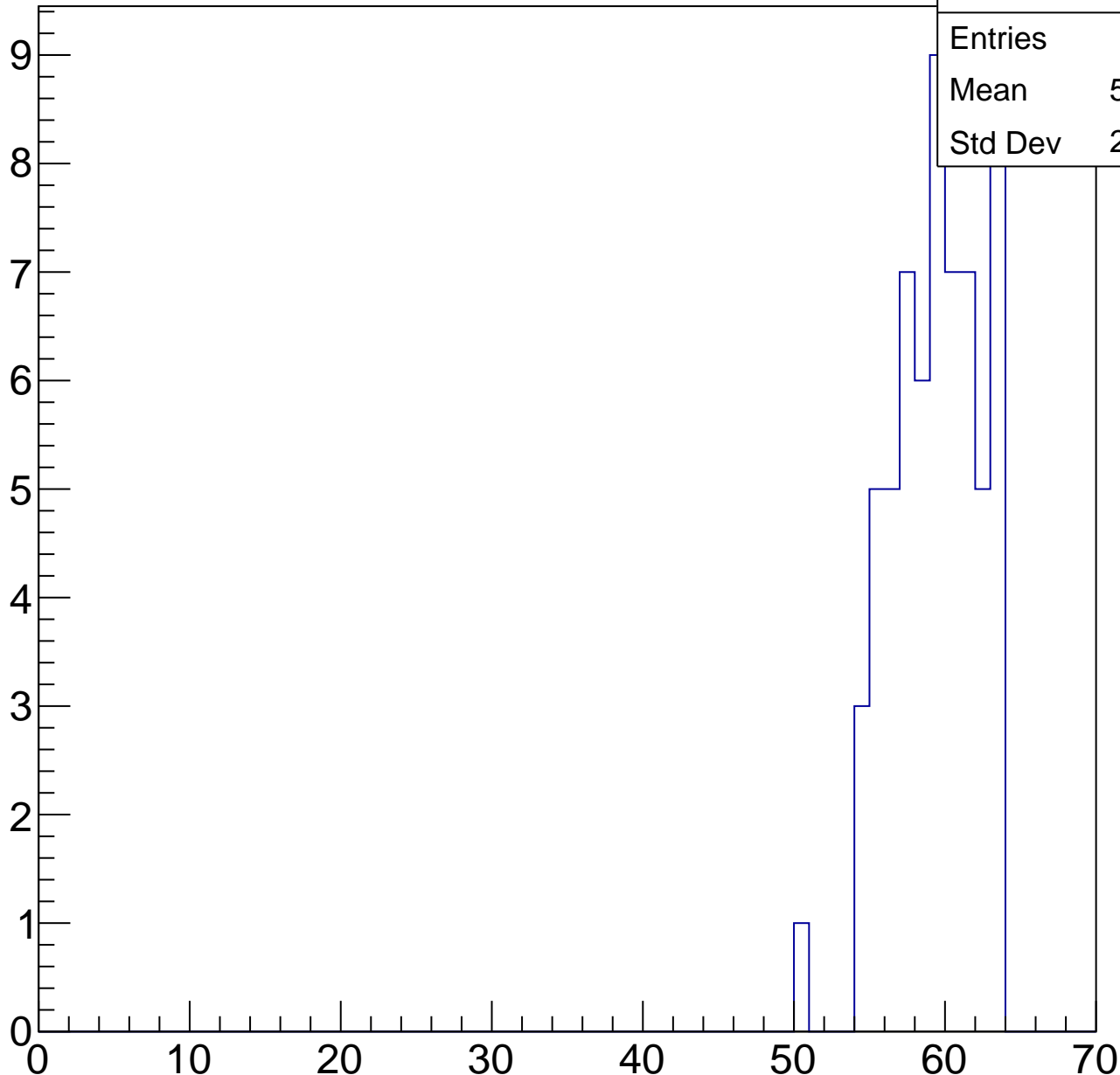
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	63
Mean	58.83
Std Dev	2.876

ampl

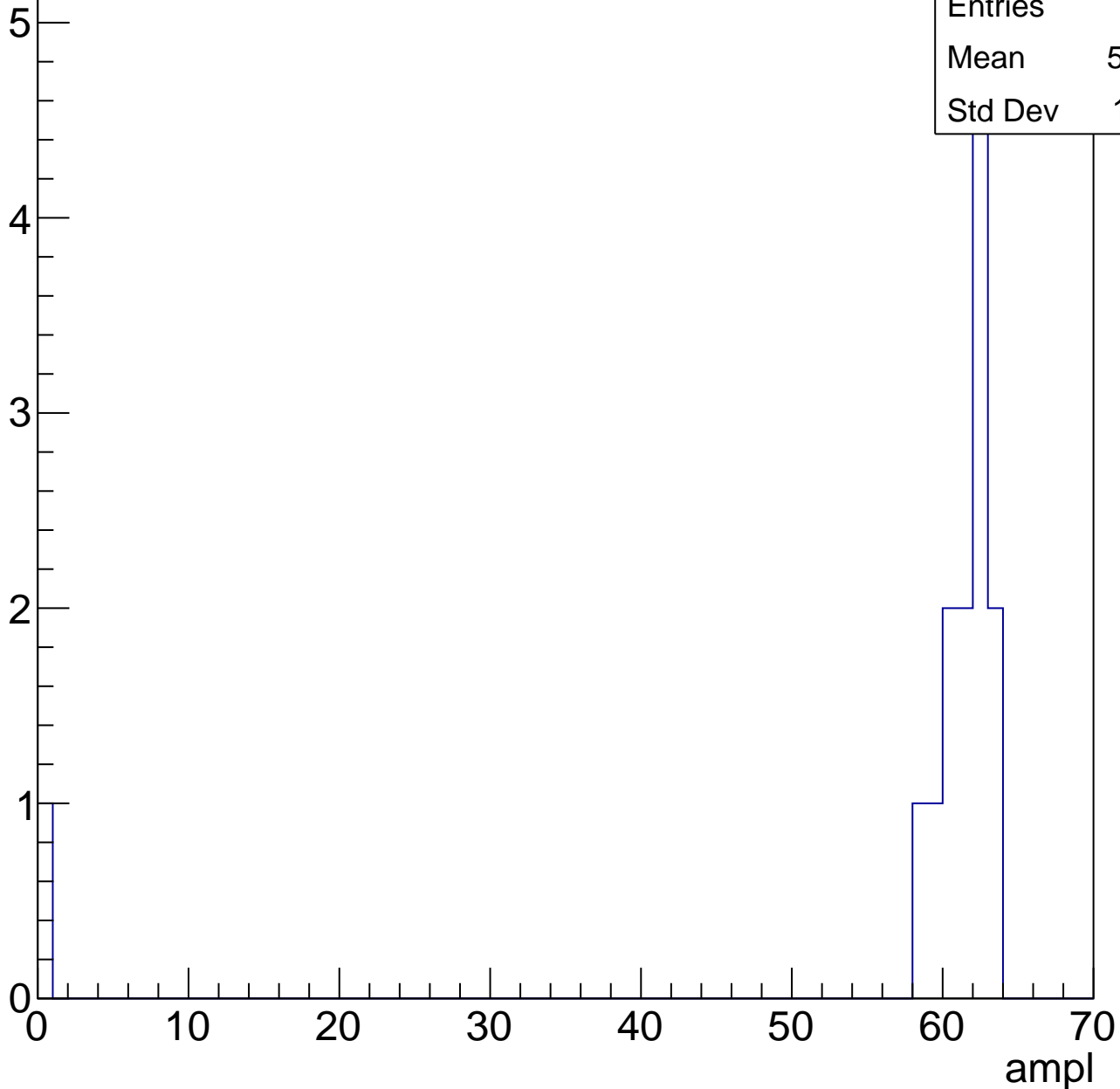


# B1L102S, U20-ch80, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	14
Mean	56.79
Std Dev	15.81

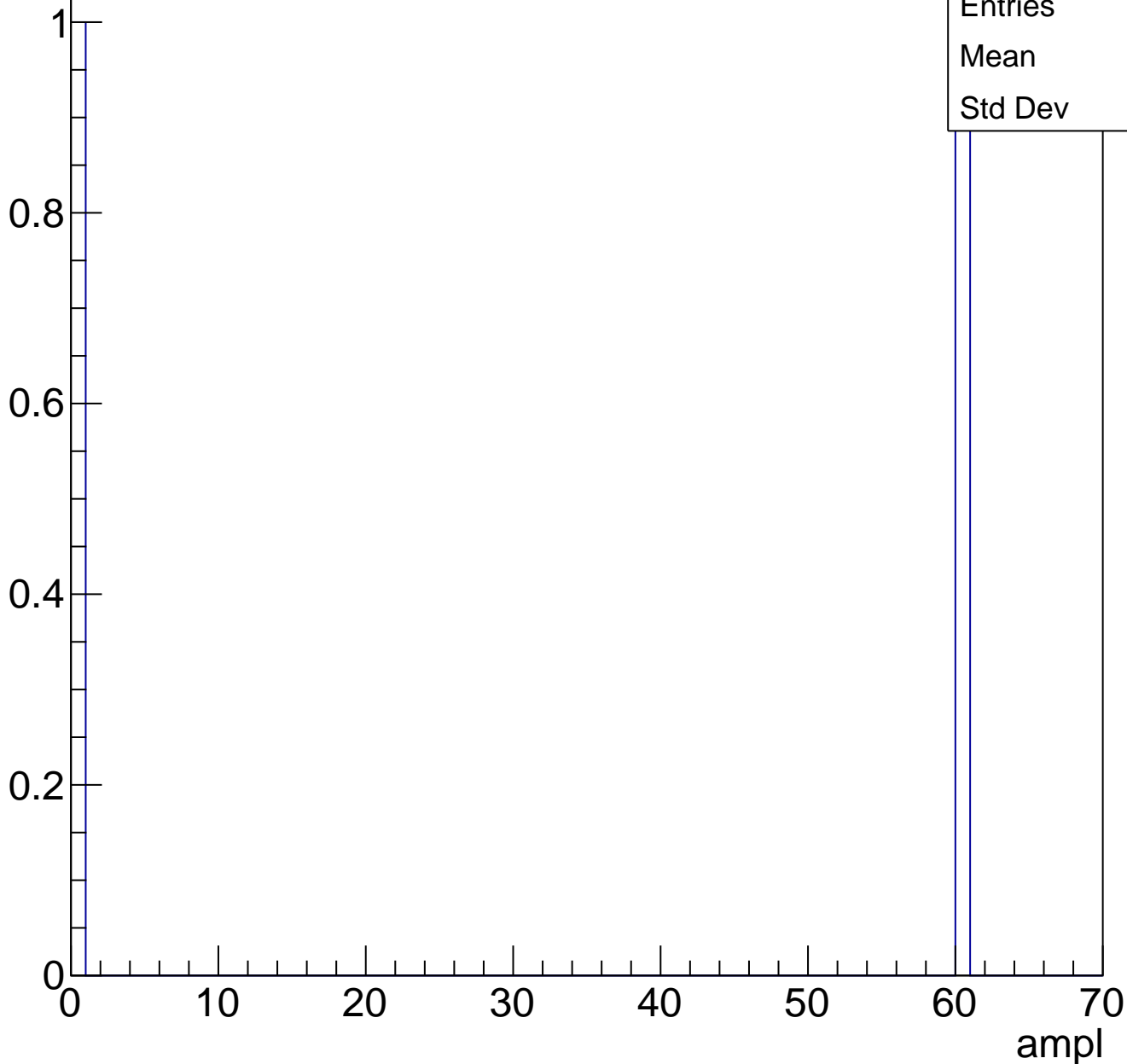




# B1L102S, U20-ch80, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch81, adc0

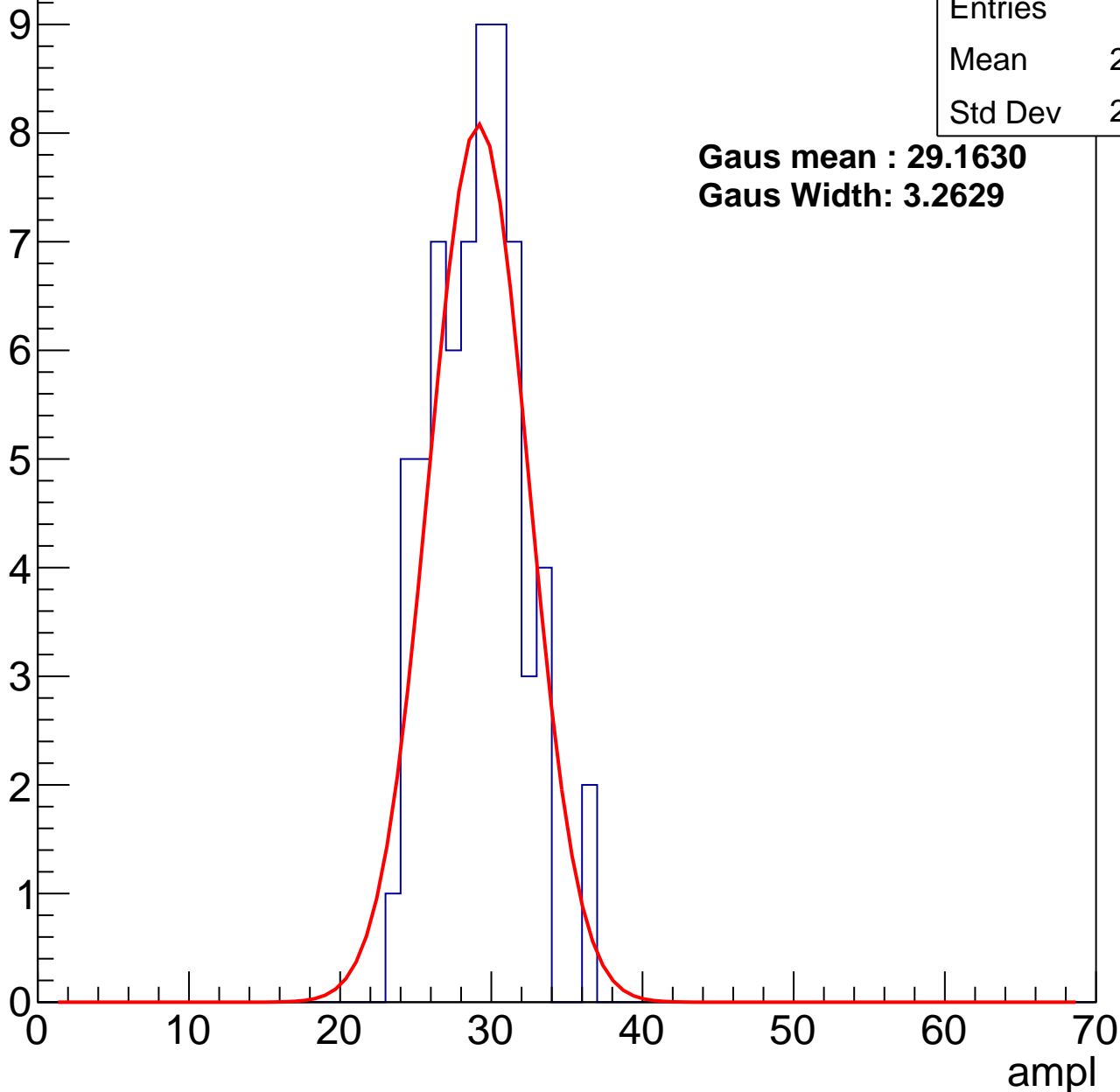
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	28.55
Std Dev	2.904

**Gaus mean : 29.1630**

**Gaus Width: 3.2629**



# B1L102S, U20-ch81, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	63
Mean	34.67
Std Dev	3.256

**Gaus mean : 34.6002**

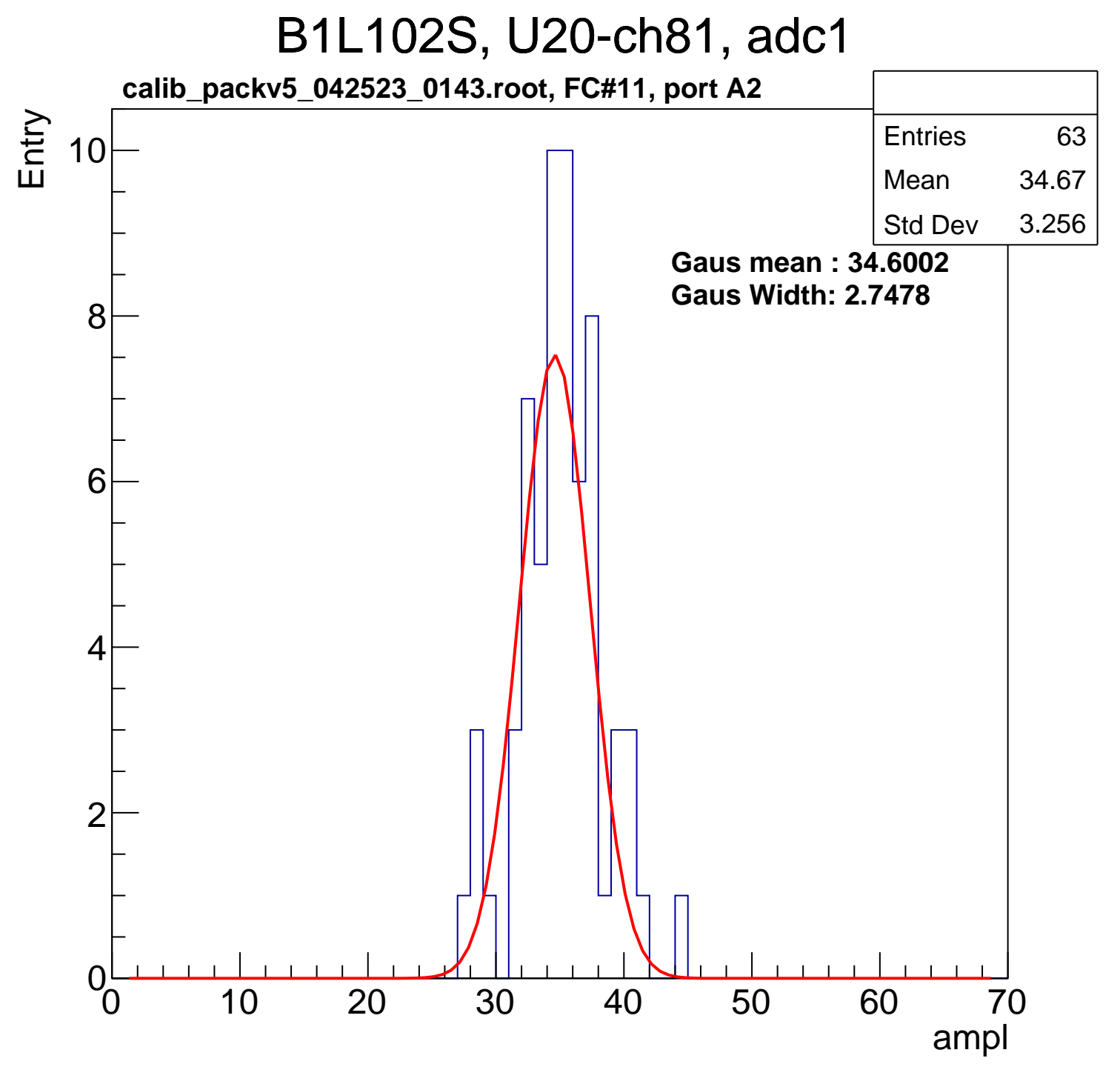
**Gaus Width: 2.7478**

Entry

10  
8  
6  
4  
2  
0

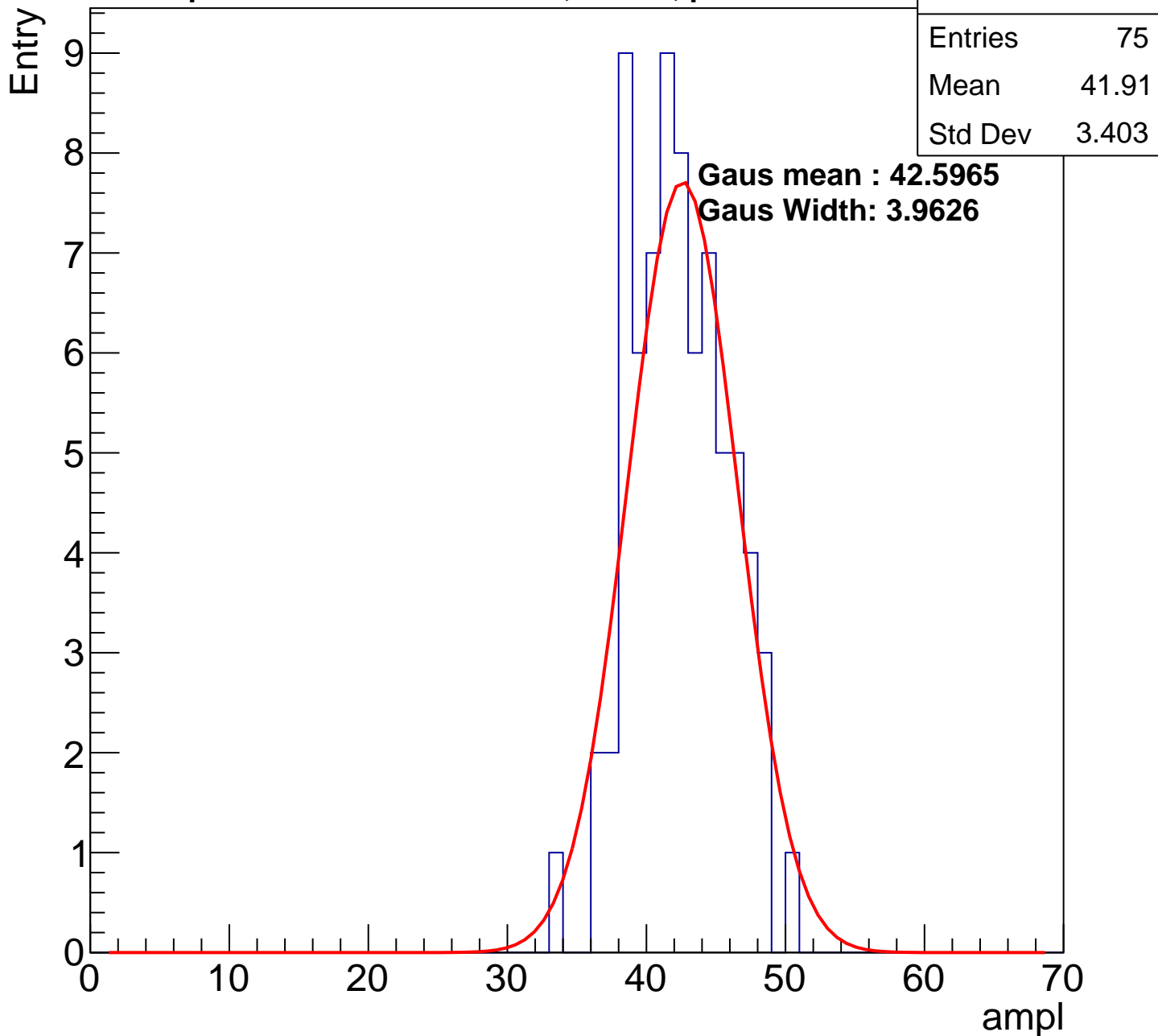
ampl

0 10 20 30 40 50 60 70



# B1L102S, U20-ch81, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

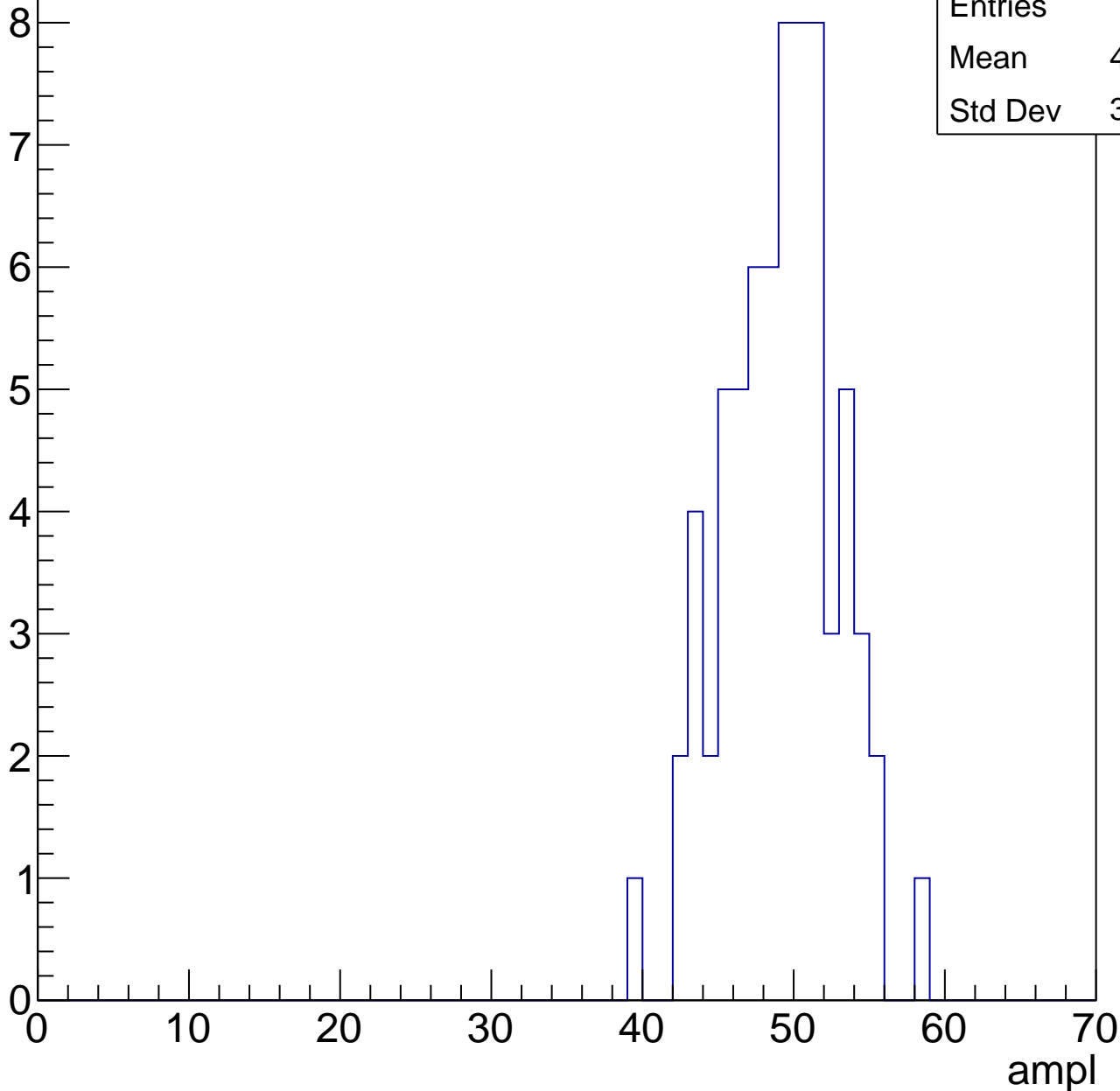


# B1L102S, U20-ch81, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	48.68
Std Dev	3.642

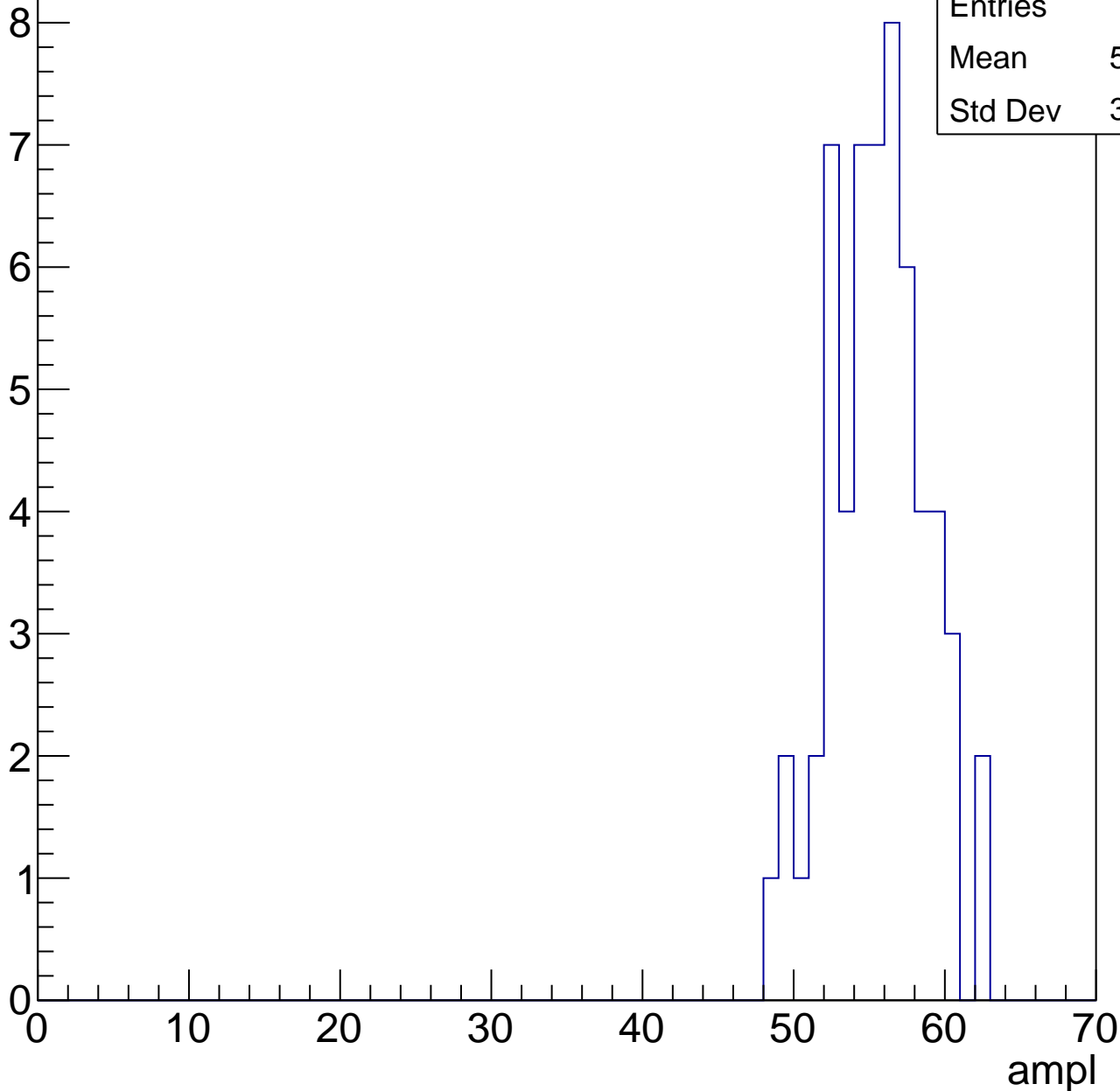


# B1L102S, U20-ch81, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	55.16
Std Dev	3.128

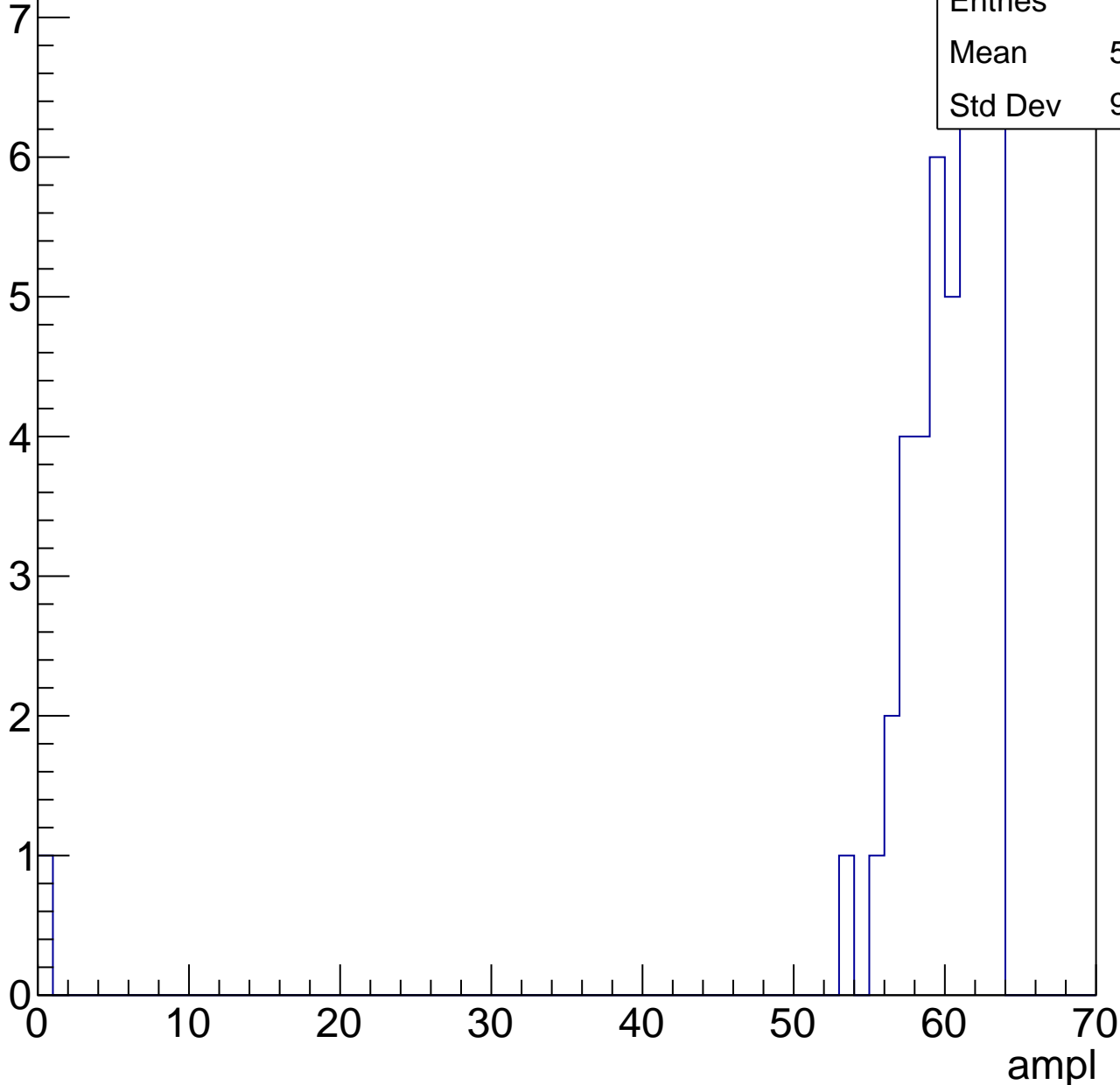


# B1L102S, U20-ch81, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	45
Mean	58.58
Std Dev	9.154



# B1L102S, U20-ch81, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries	10
Mean	61.2
Std Dev	1.536



# B1L102S, U20-ch81, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L102S, U20-ch82, adc0

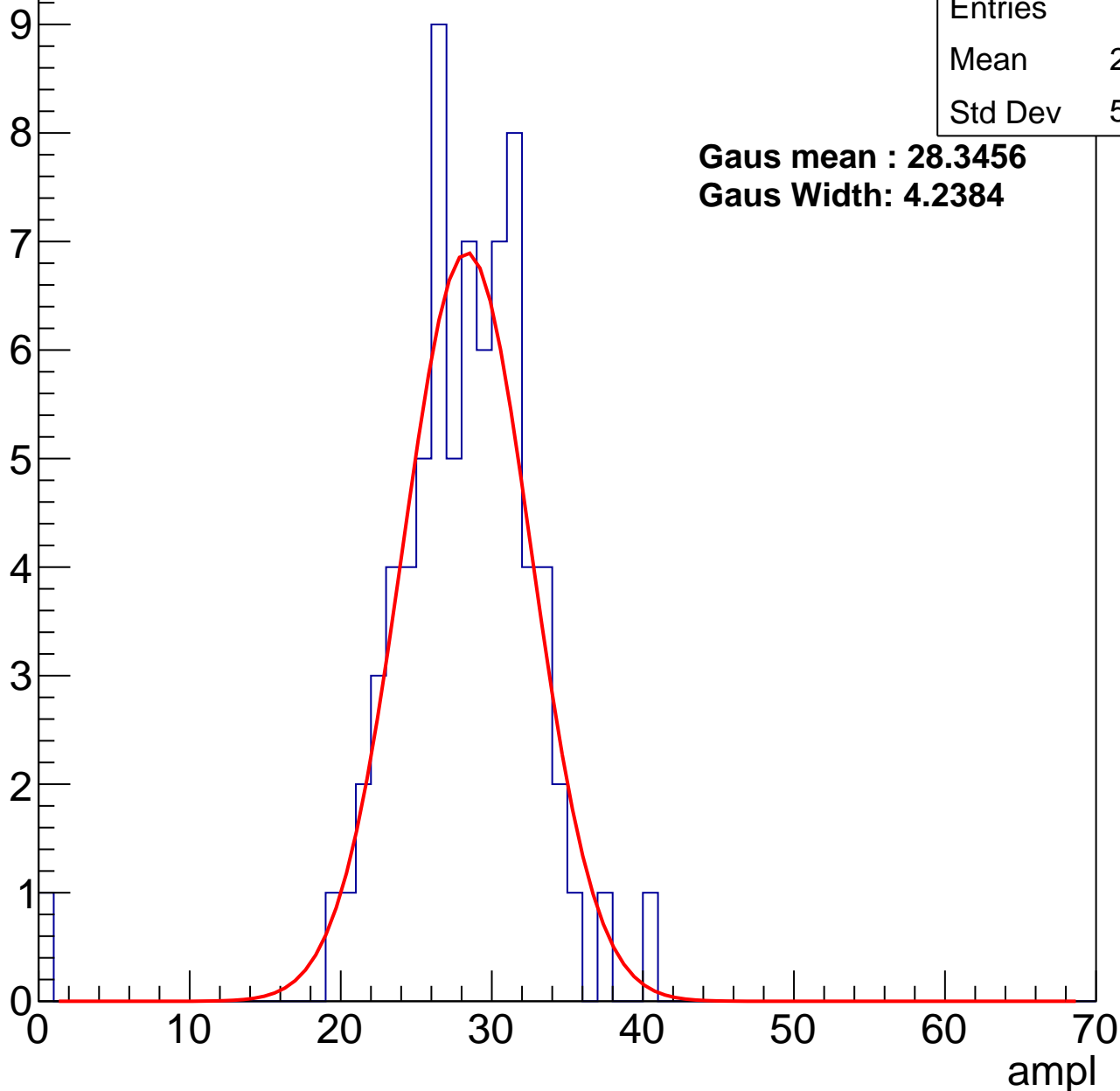
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	27.59
Std Dev	5.115

**Gaus mean : 28.3456**

**Gaus Width: 4.2384**



# B1L102S, U20-ch82, adc1

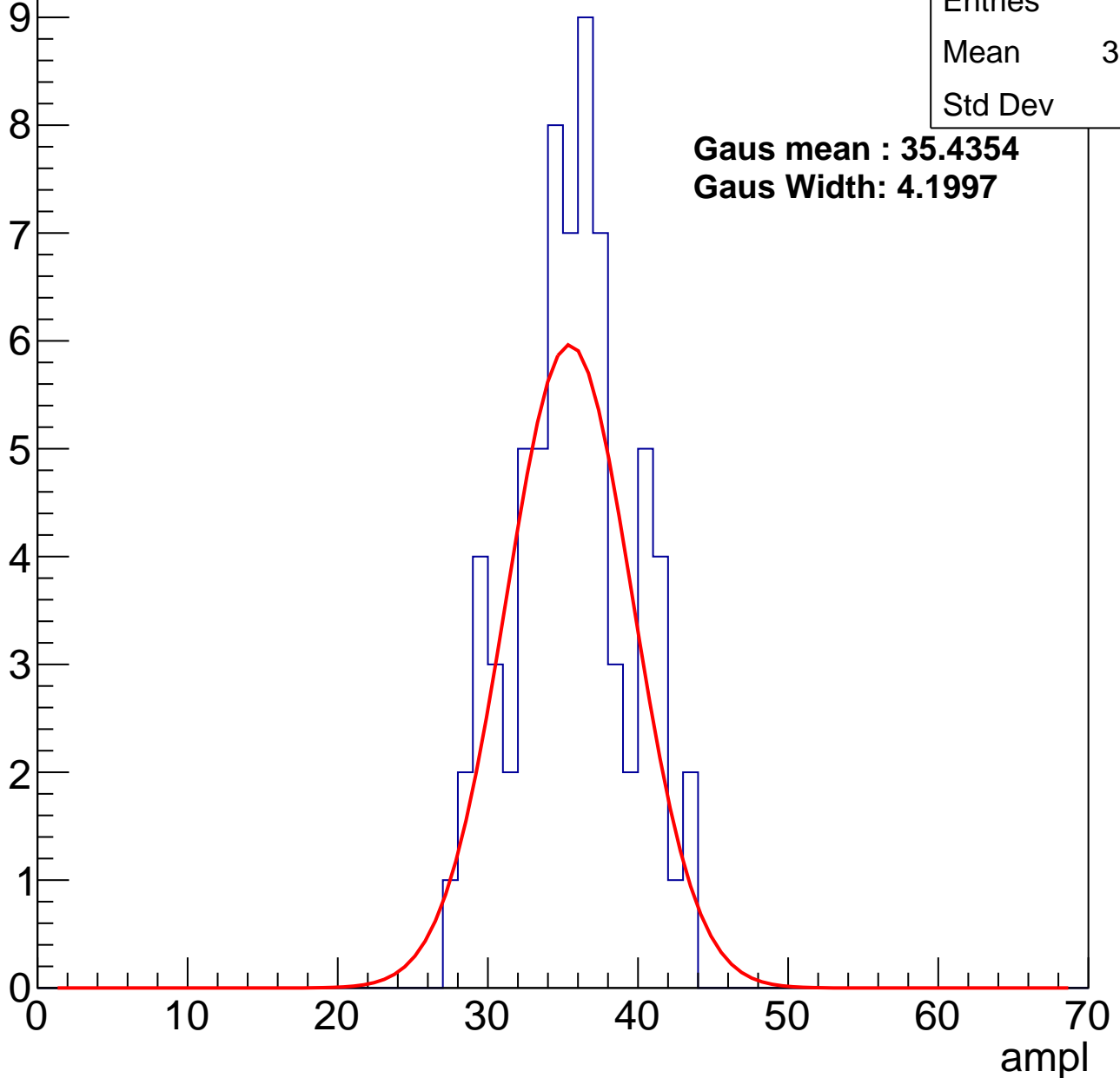
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	35.14
Std Dev	3.83

**Gaus mean : 35.4354**

**Gaus Width: 4.1997**



# B1L102S, U20-ch82, adc2

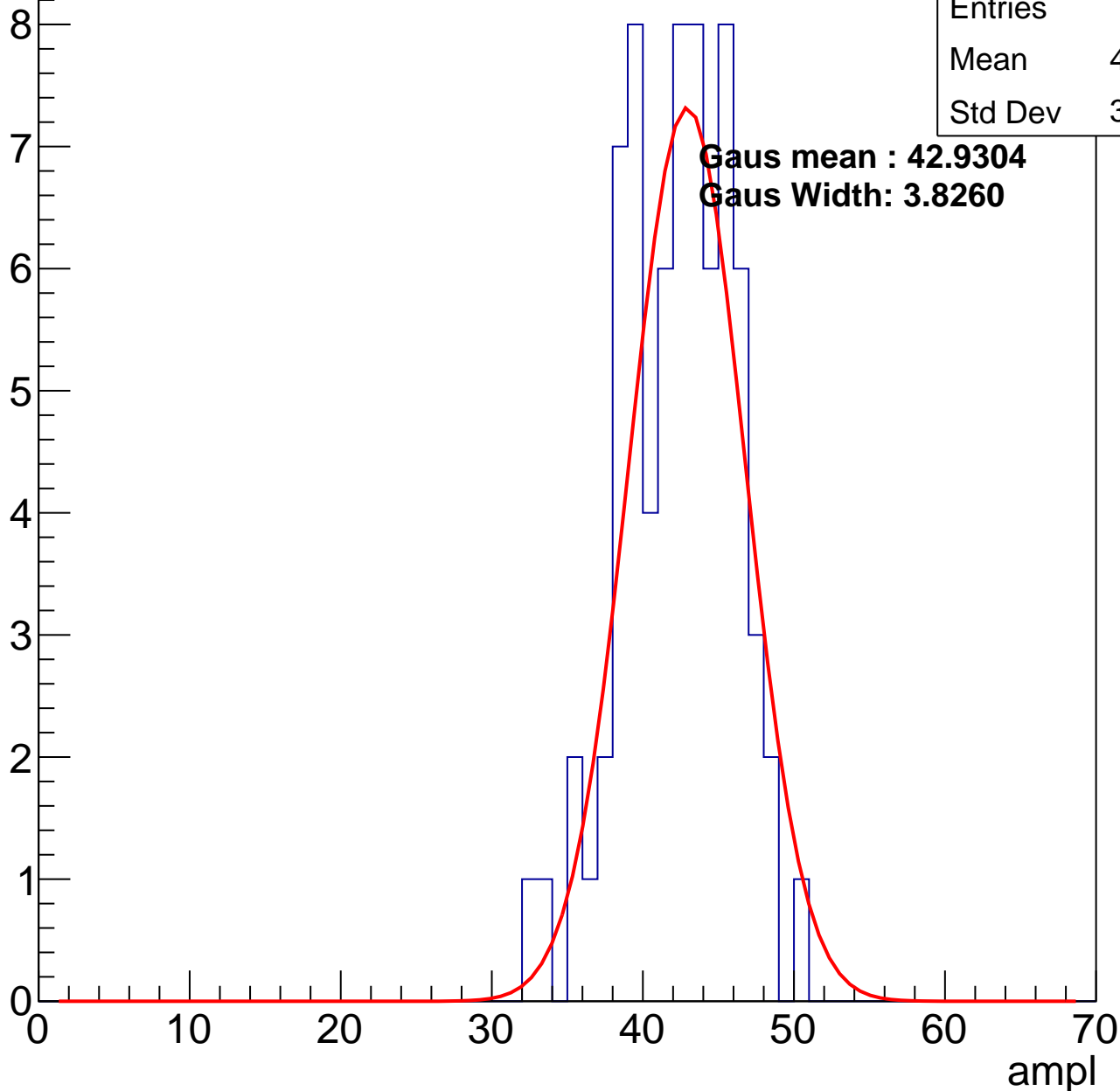
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	41.84
Std Dev	3.639

**Gaus mean : 42.9304**

**Gaus Width: 3.8260**

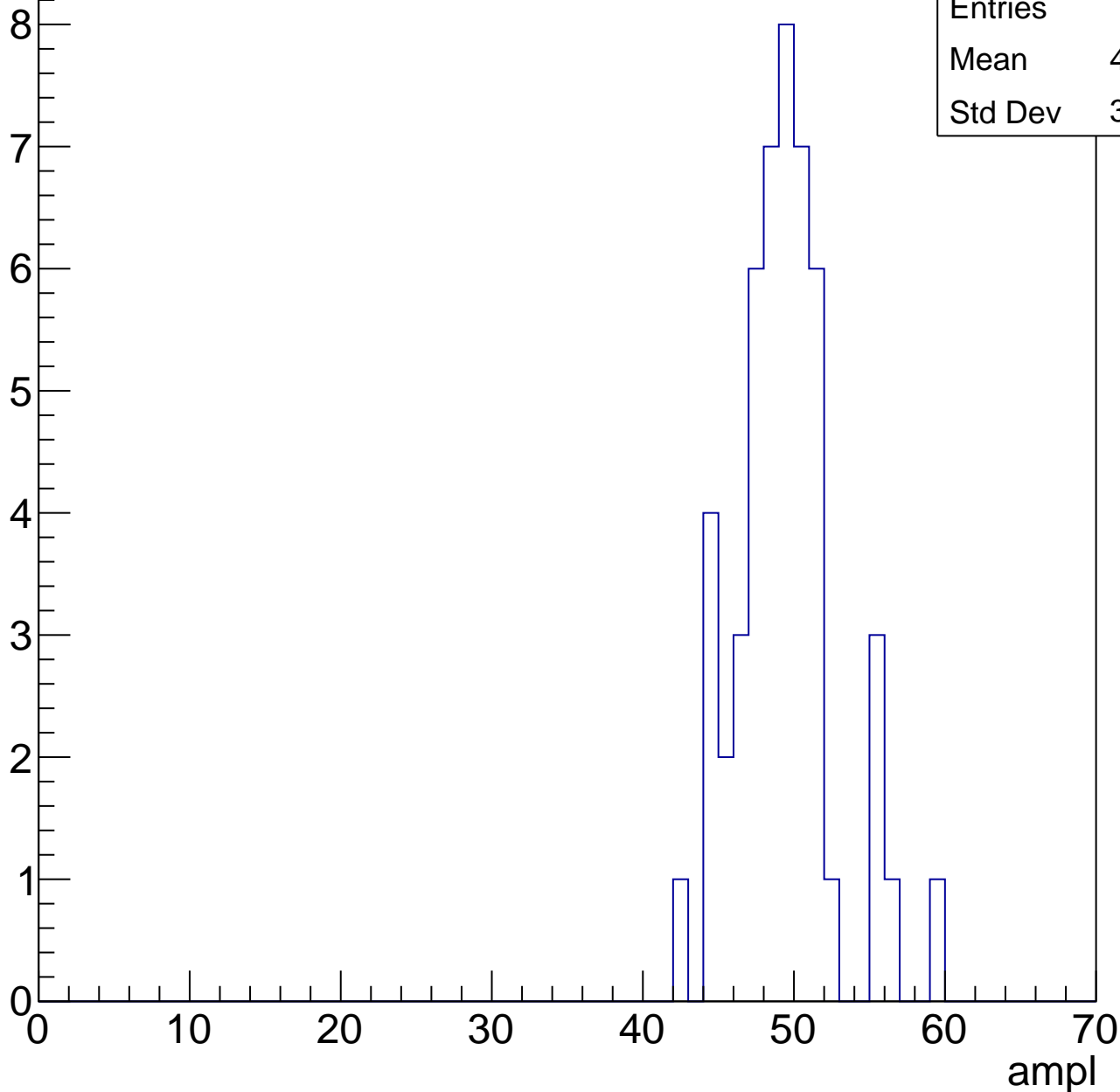


# B1L102S, U20-ch82, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	48.88
Std Dev	3.272



# B1L102S, U20-ch82, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	58
Mean	54.34
Std Dev	3.386

Entry

10

8

6

4

2

0

0

10

20

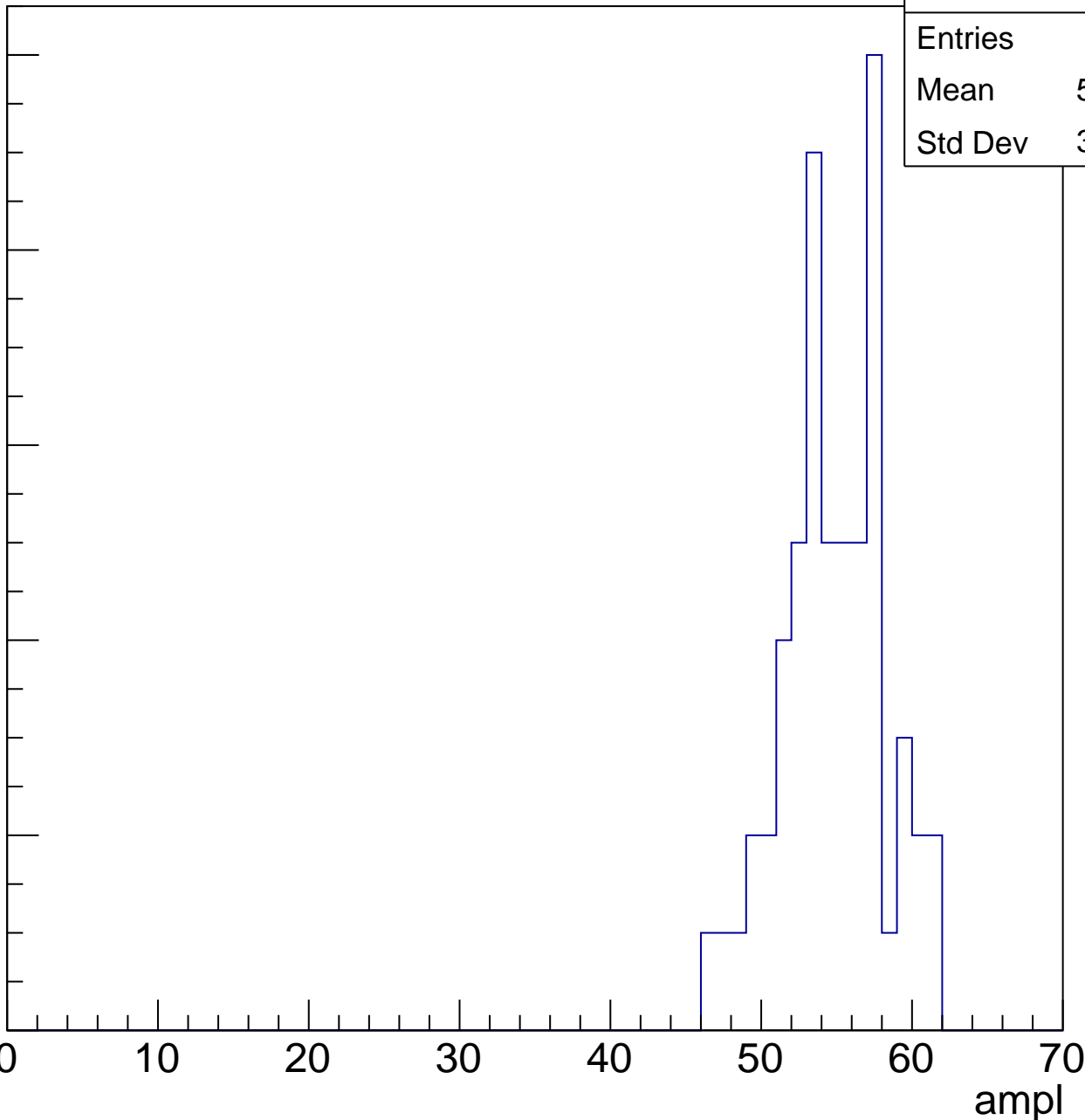
30

40

50

60

ampl

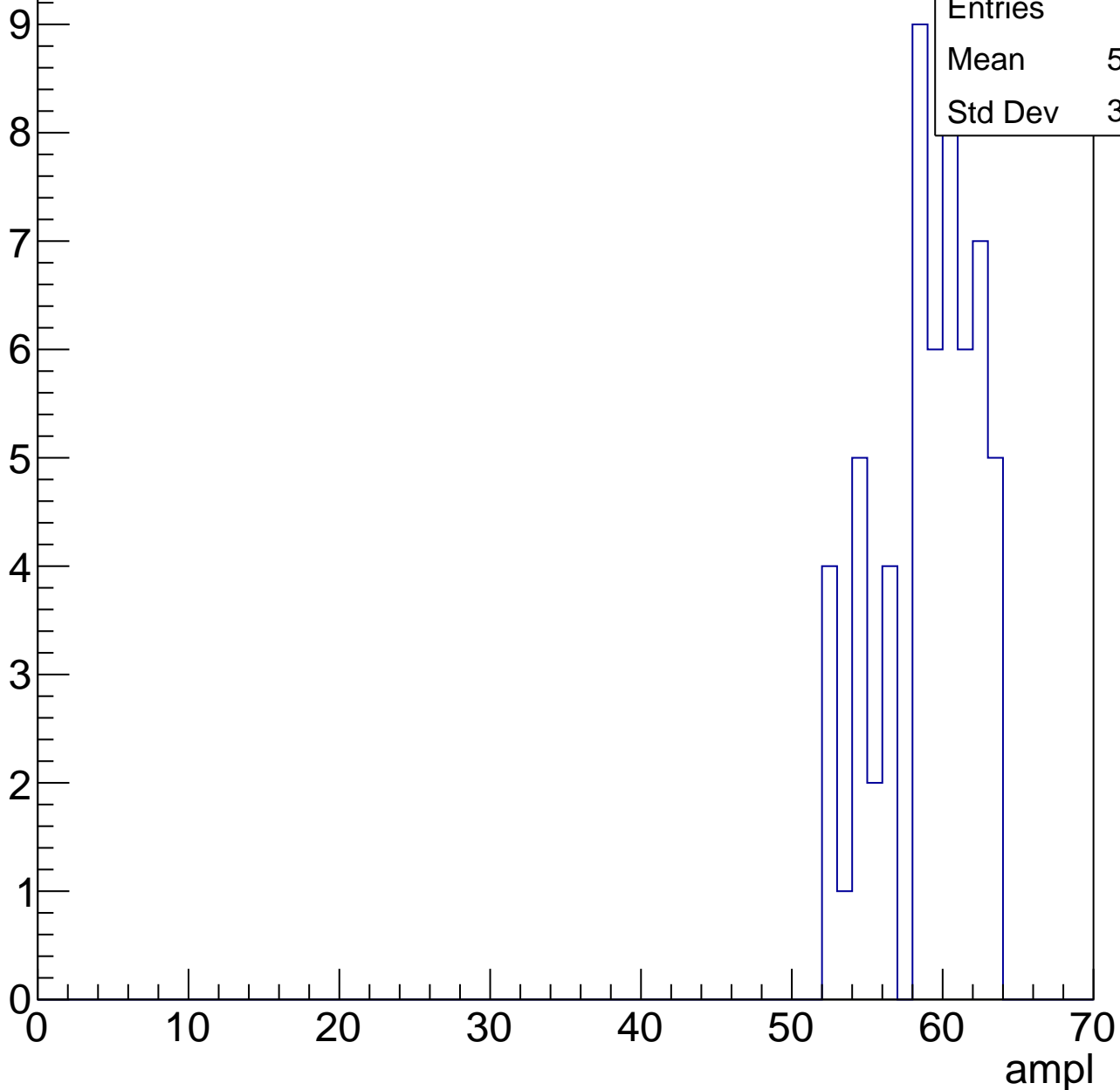


# B1L102S, U20-ch82, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	58.53
Std Dev	3.234

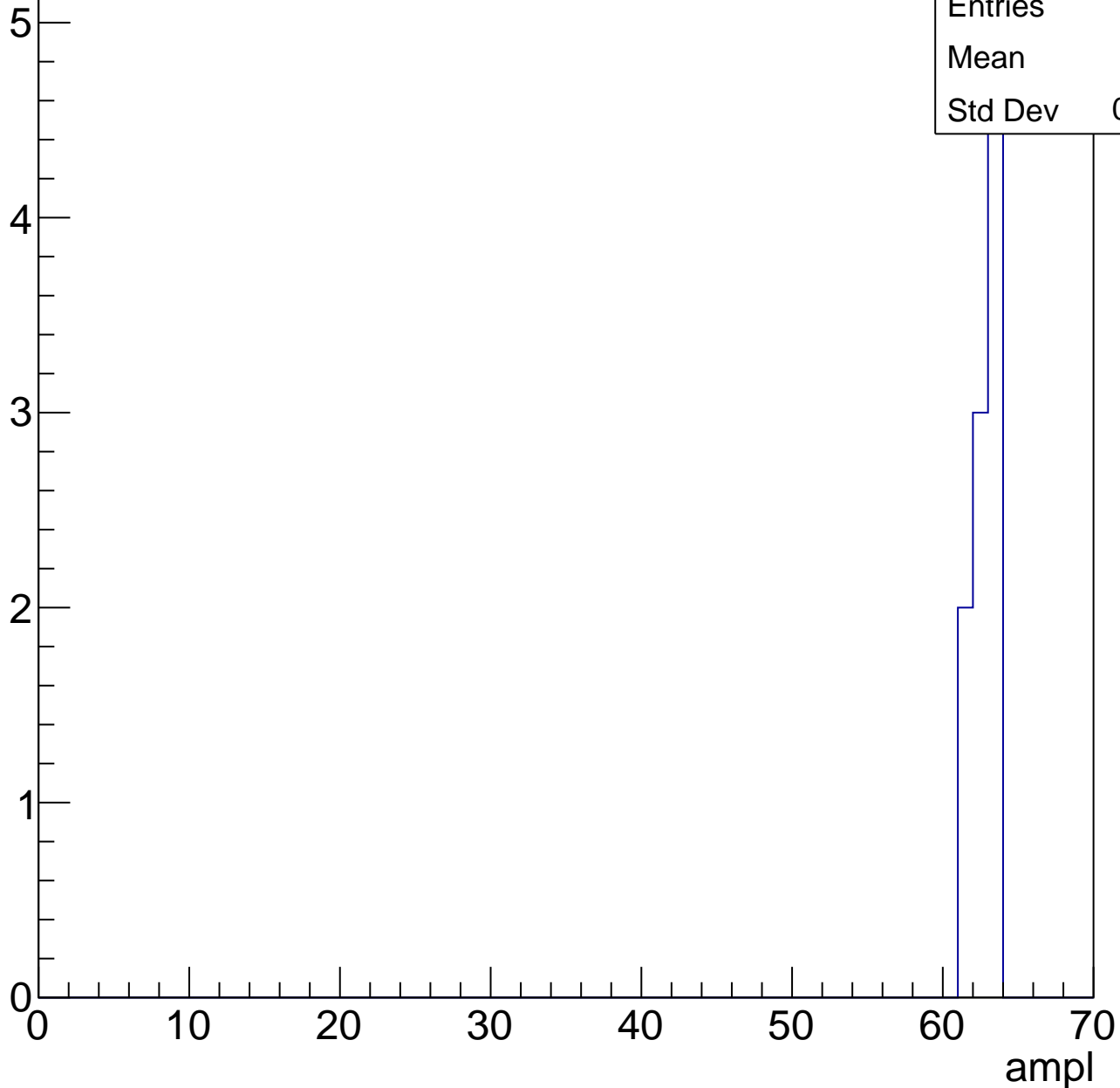


# B1L102S, U20-ch82, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	10
Mean	62.3
Std Dev	0.781





# B1L102S, U20-ch82, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch83, adc0

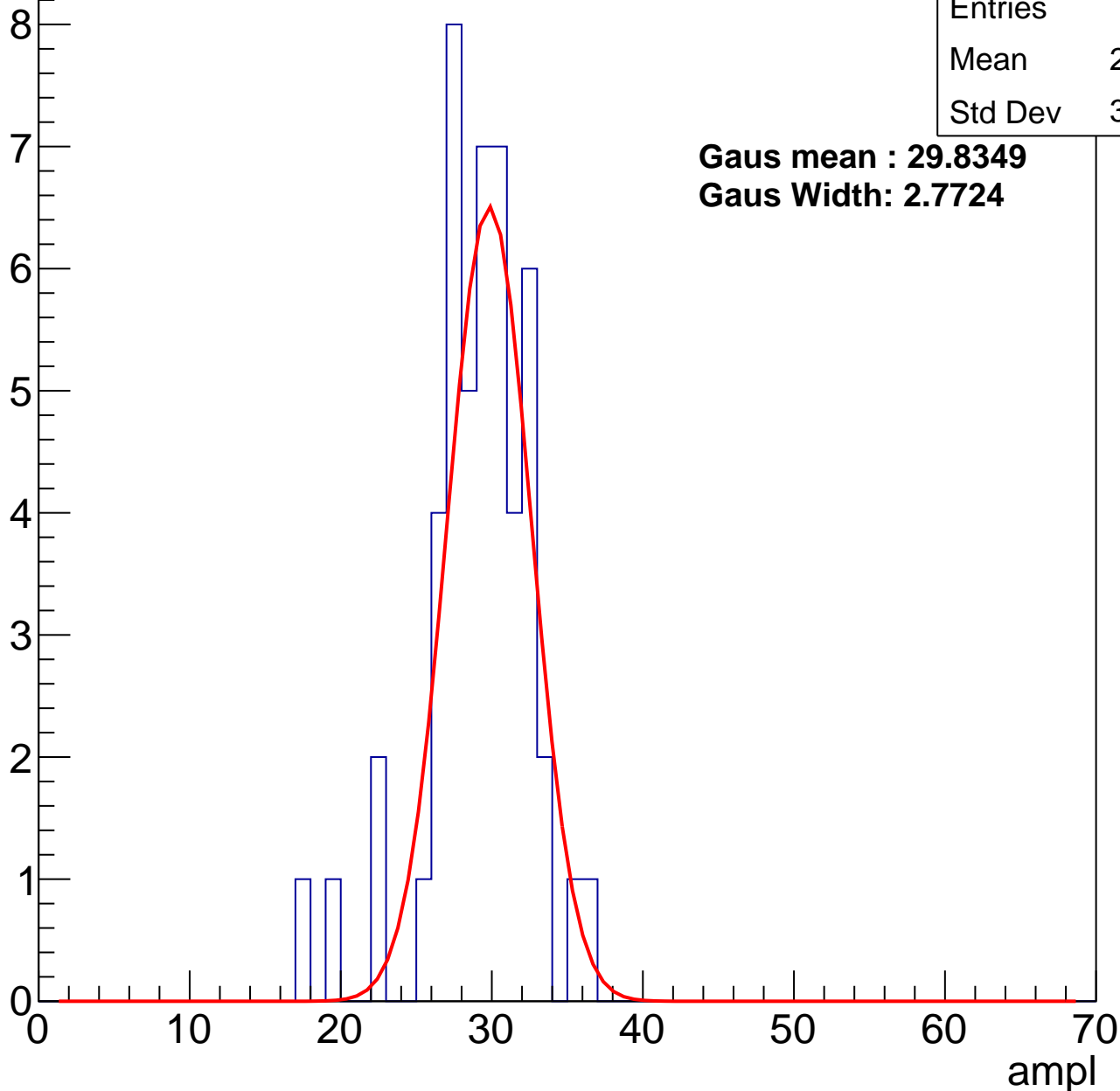
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	28.62
Std Dev	3.515

**Gaus mean : 29.8349**

**Gaus Width: 2.7724**



# B1L102S, U20-ch83, adc1

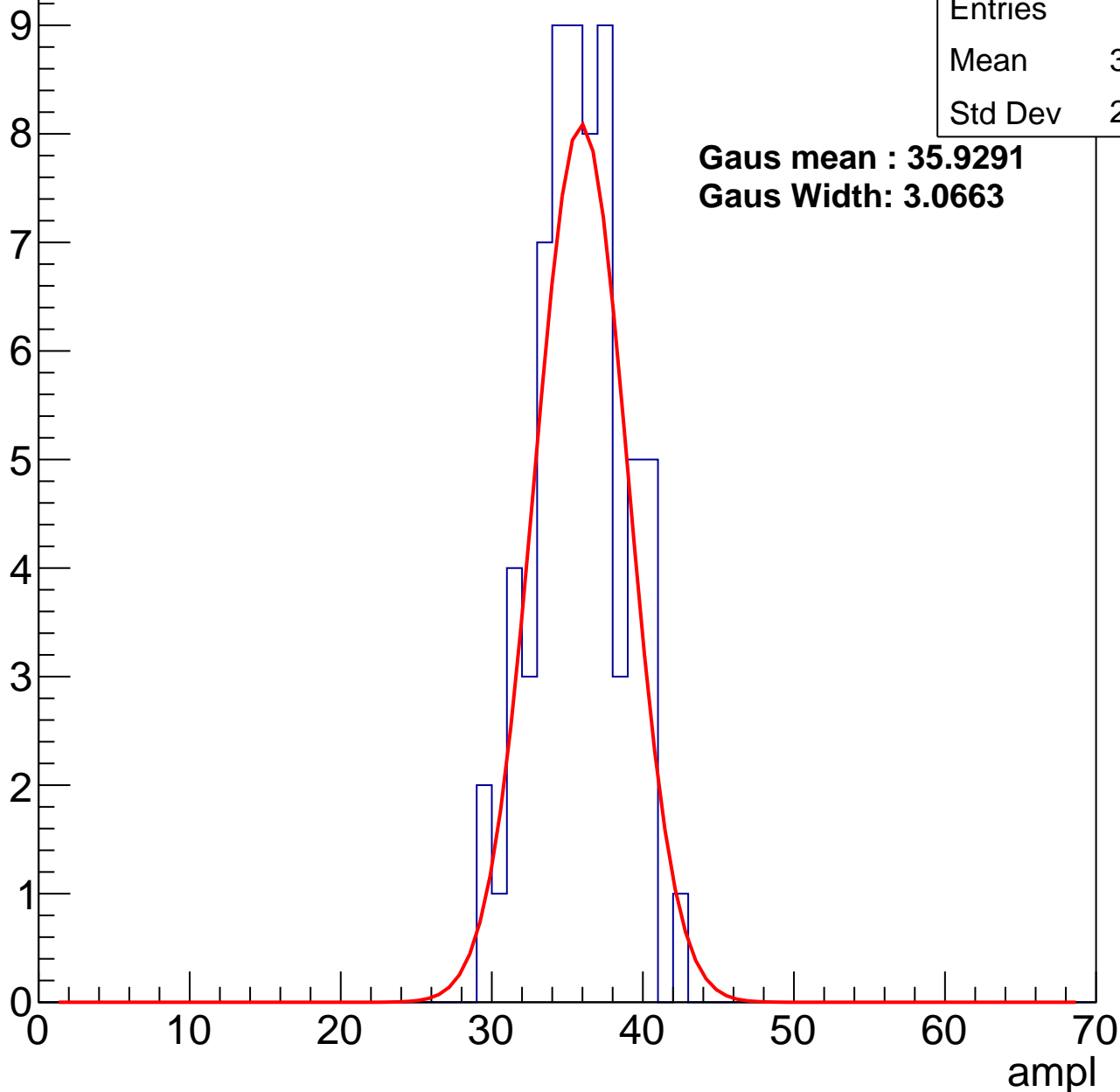
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	35.33
Std Dev	2.867

**Gaus mean : 35.9291**

**Gaus Width: 3.0663**



# B1L102S, U20-ch83, adc2

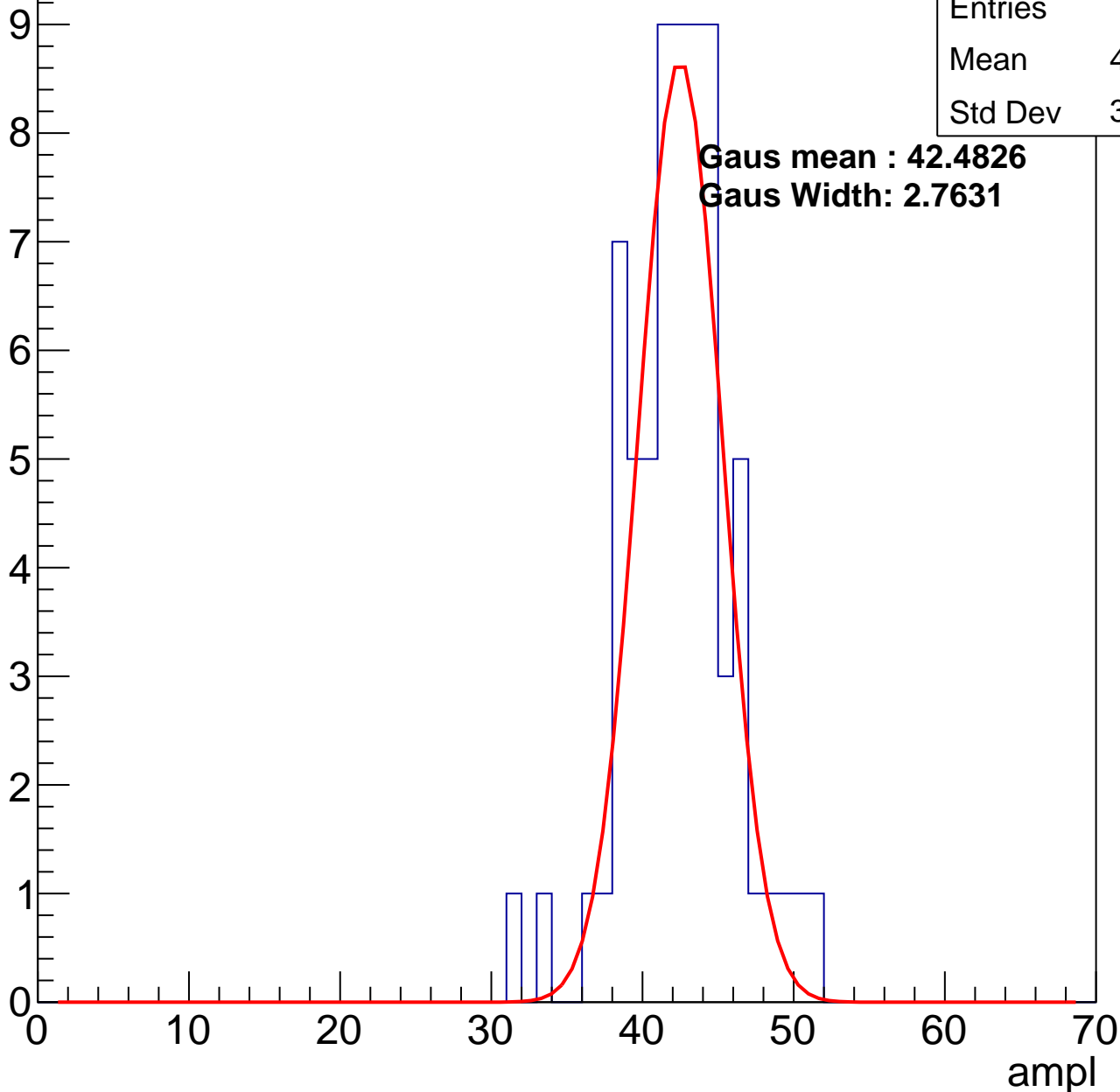
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	41.97
Std Dev	3.497

**Gaus mean : 42.4826**

**Gaus Width: 2.7631**

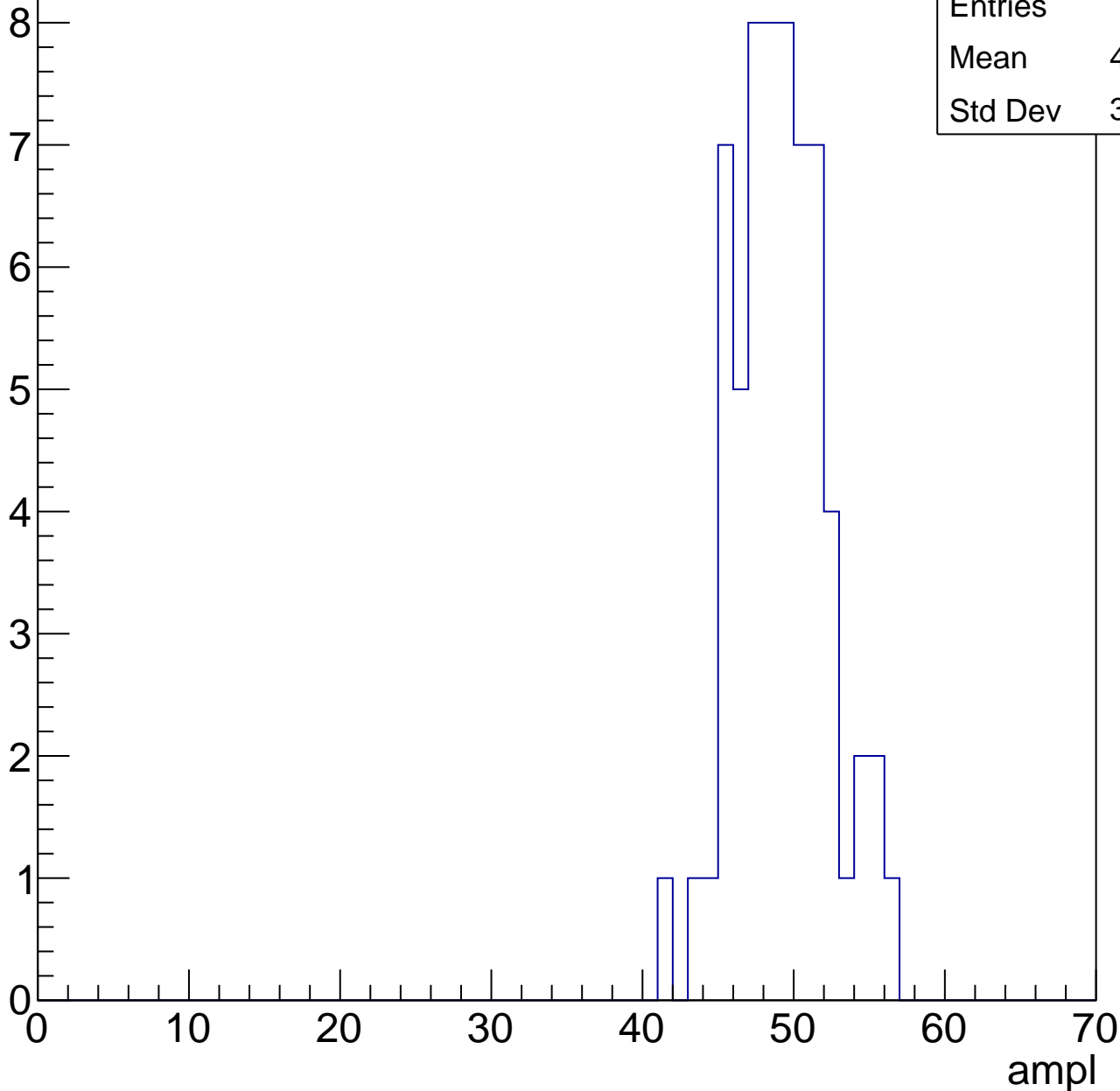


# B1L102S, U20-ch83, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

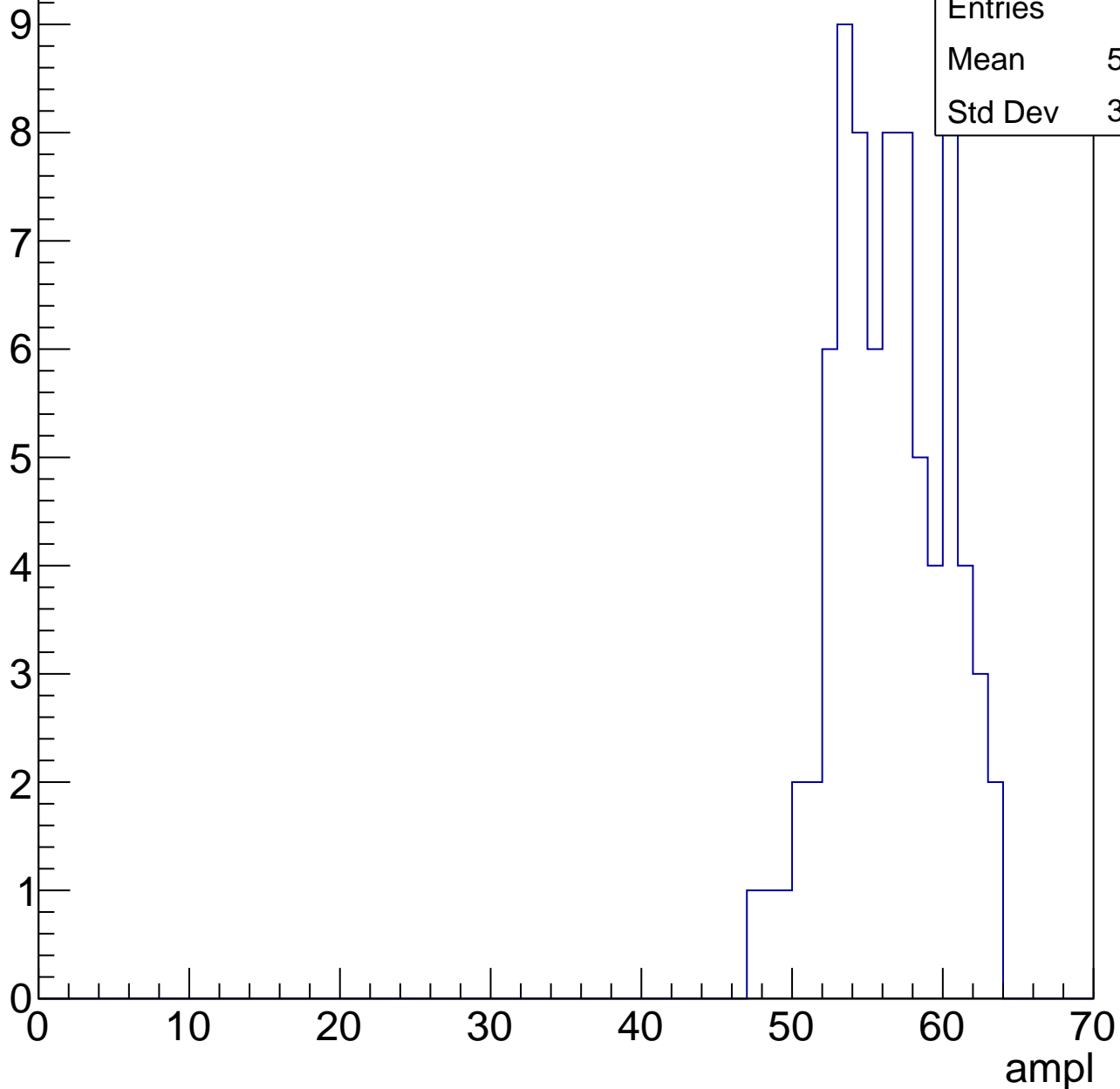
Entries	63
Mean	48.68
Std Dev	3.018



# B1L102S, U20-ch83, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

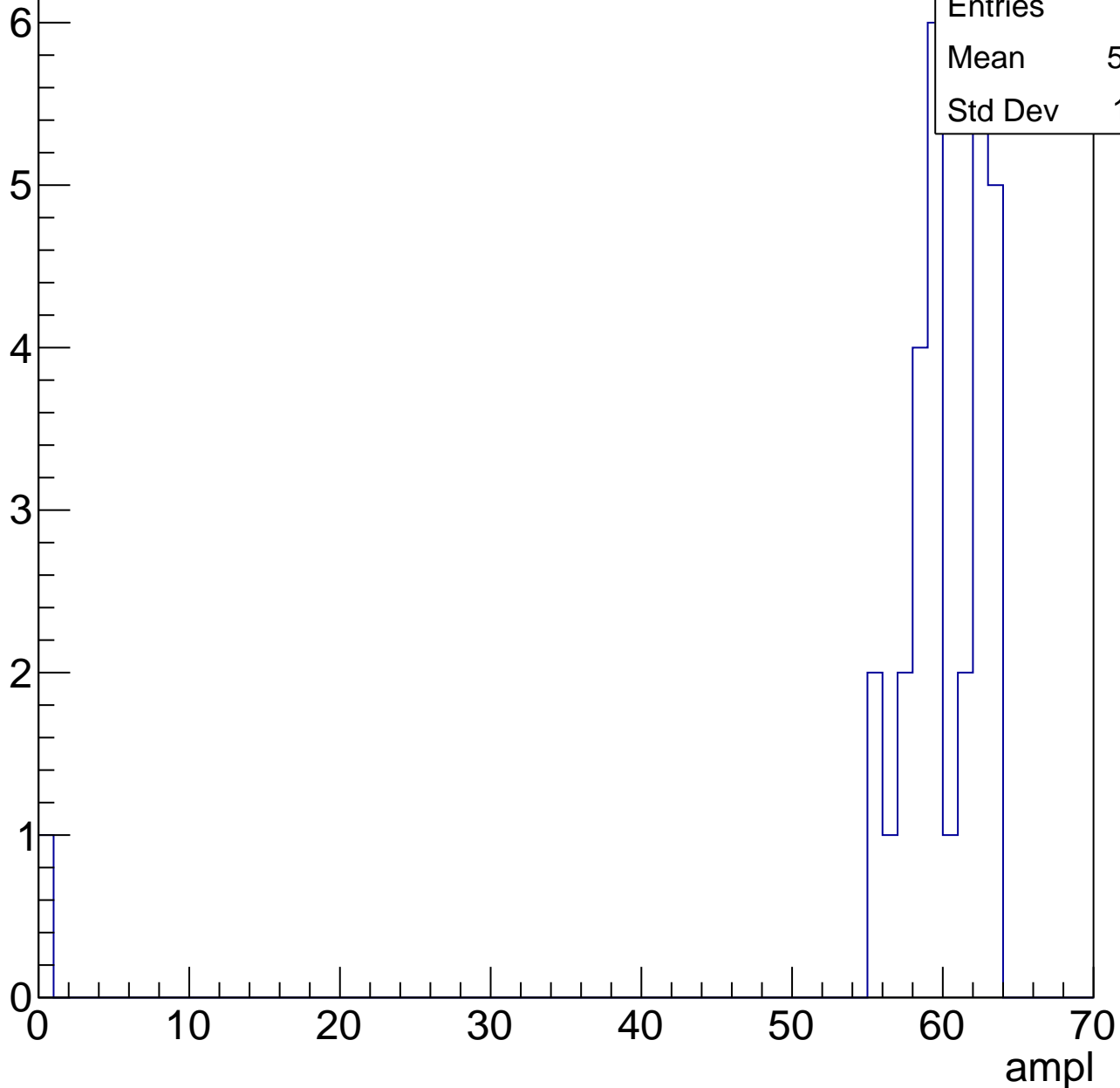


Entries	79
Mean	55.99
Std Dev	3.637

# B1L102S, U20-ch83, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

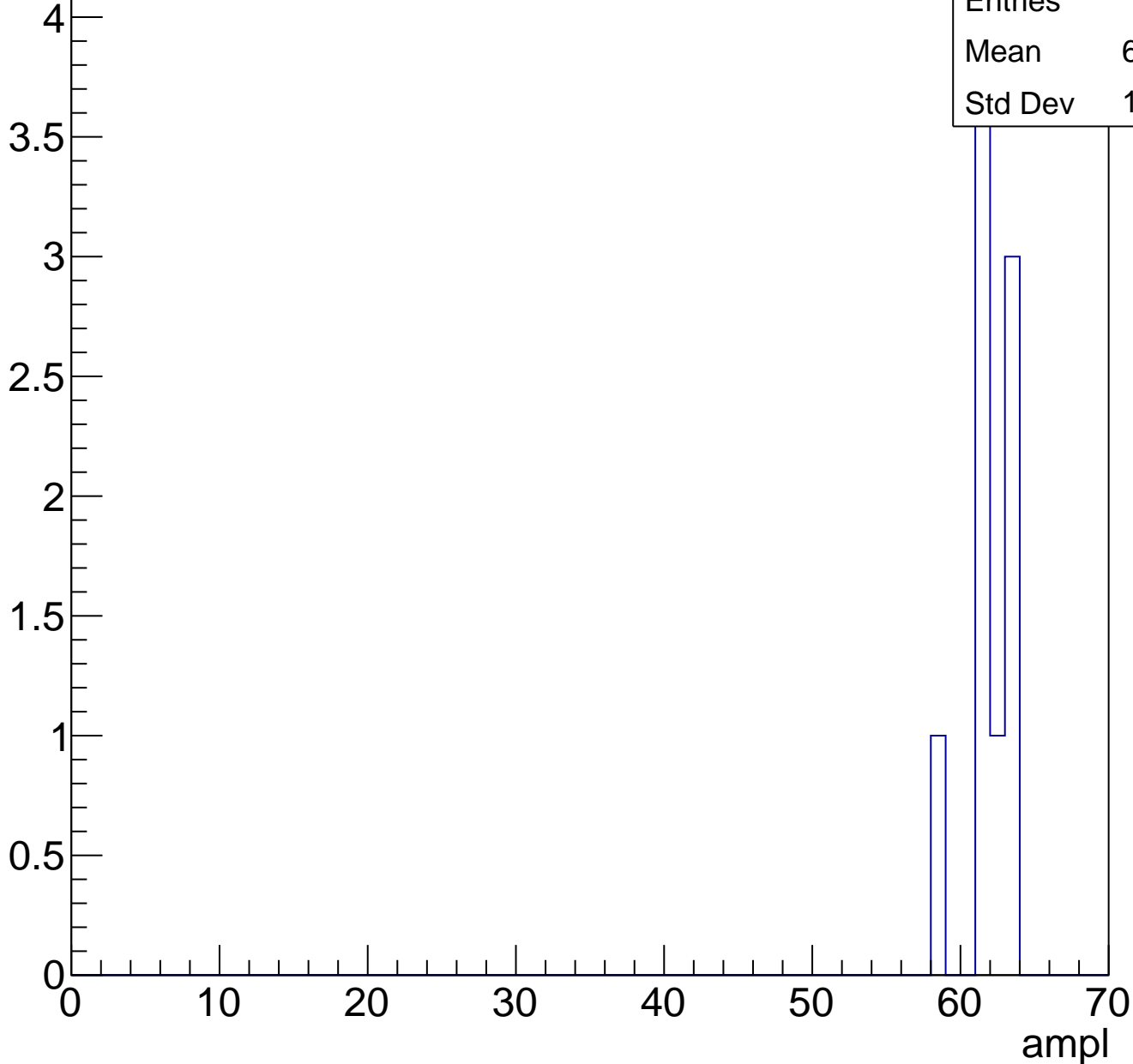
Entry



# B1L102S, U20-ch83, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U20-ch83, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

0

Mean

0

Std Dev

0

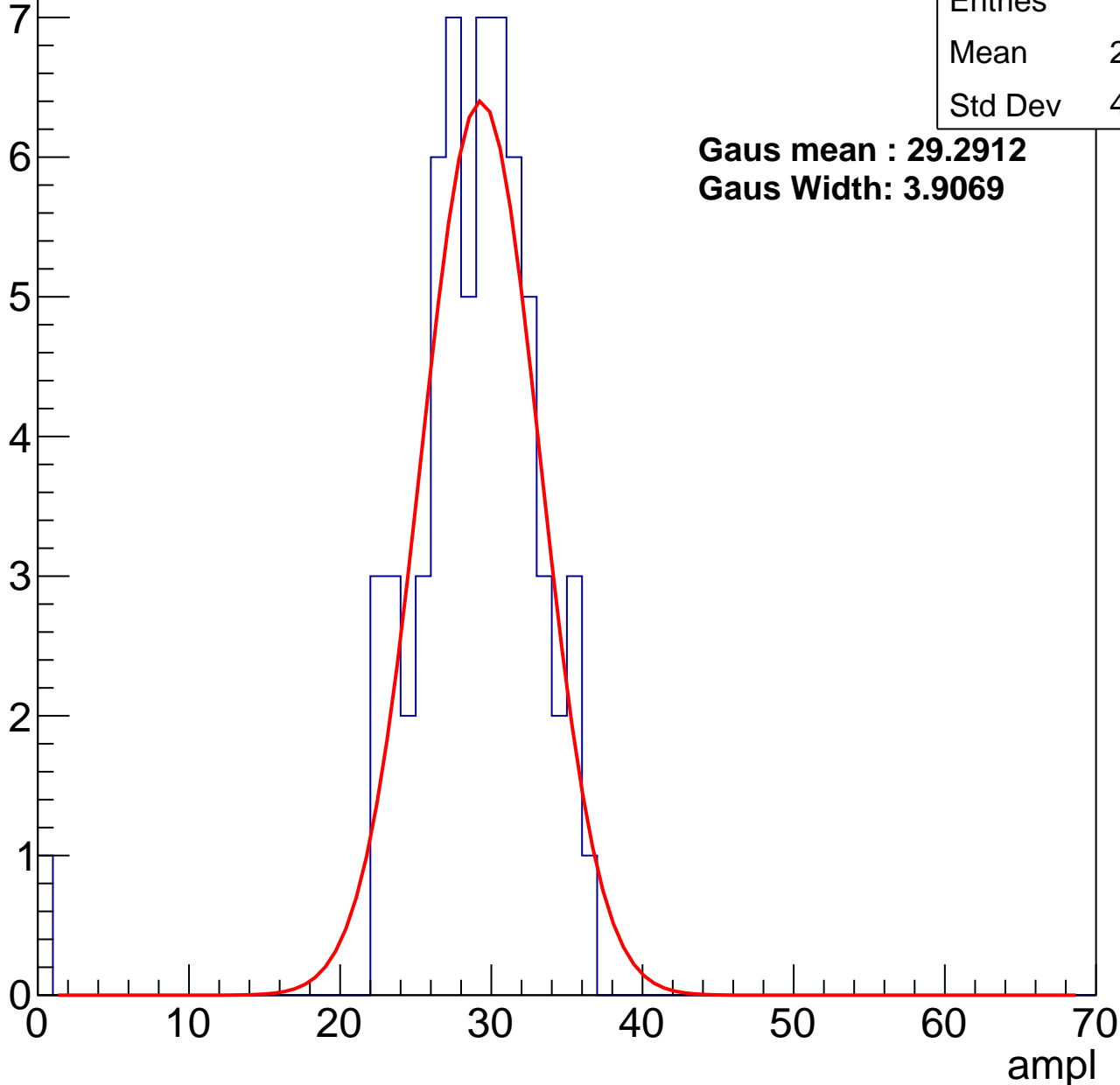
# B1L102S, U20-ch84, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	28.28
Std Dev	4.967

**Gaus mean : 29.2912**  
**Gaus Width: 3.9069**



# B1L102S, U20-ch84, adc1

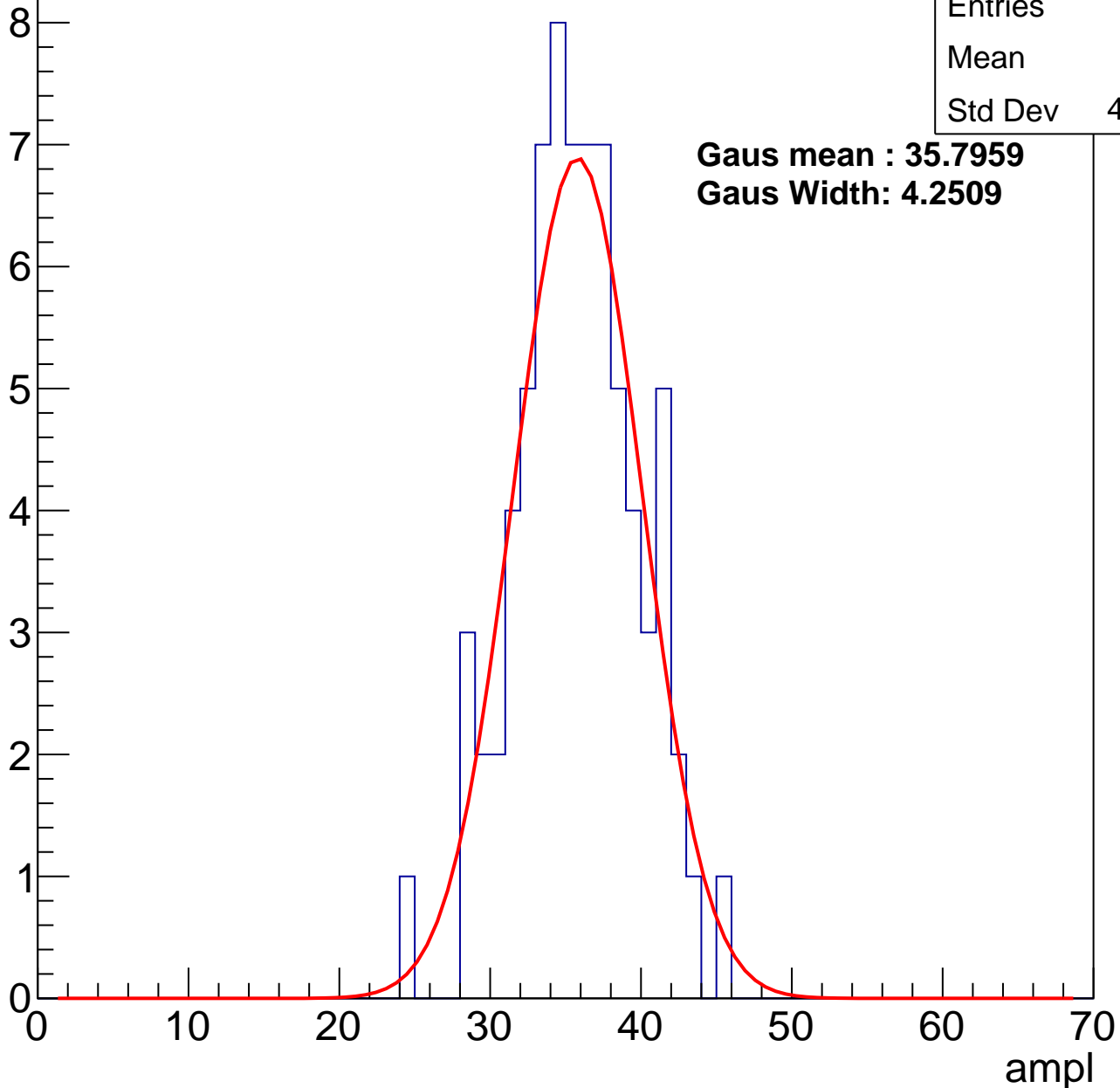
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	35.3
Std Dev	4.009

**Gaus mean : 35.7959**

**Gaus Width: 4.2509**



# B1L102S, U20-ch84, adc2

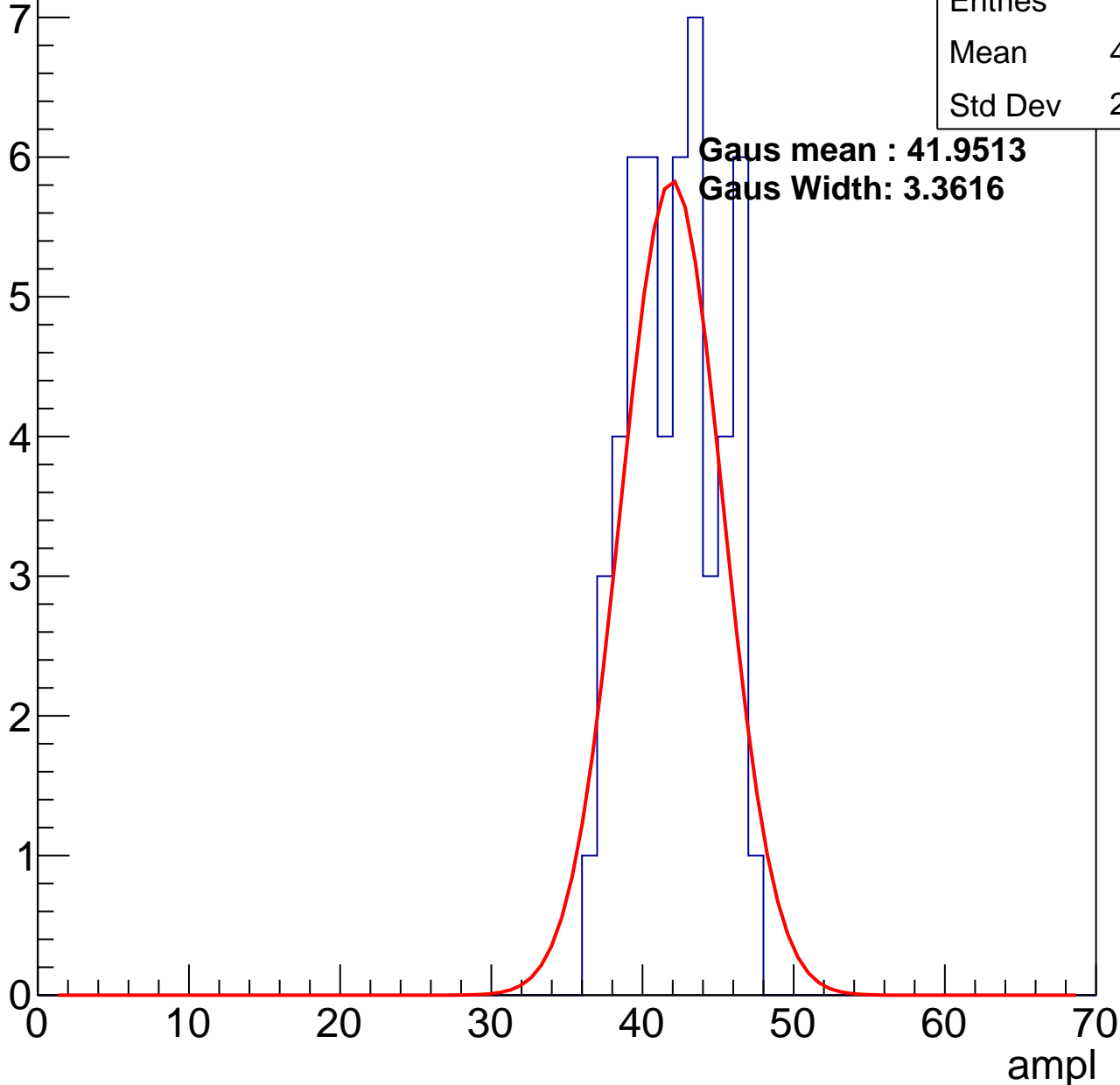
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	41.67
Std Dev	2.895

**Gaus mean : 41.9513**

**Gaus Width: 3.3616**

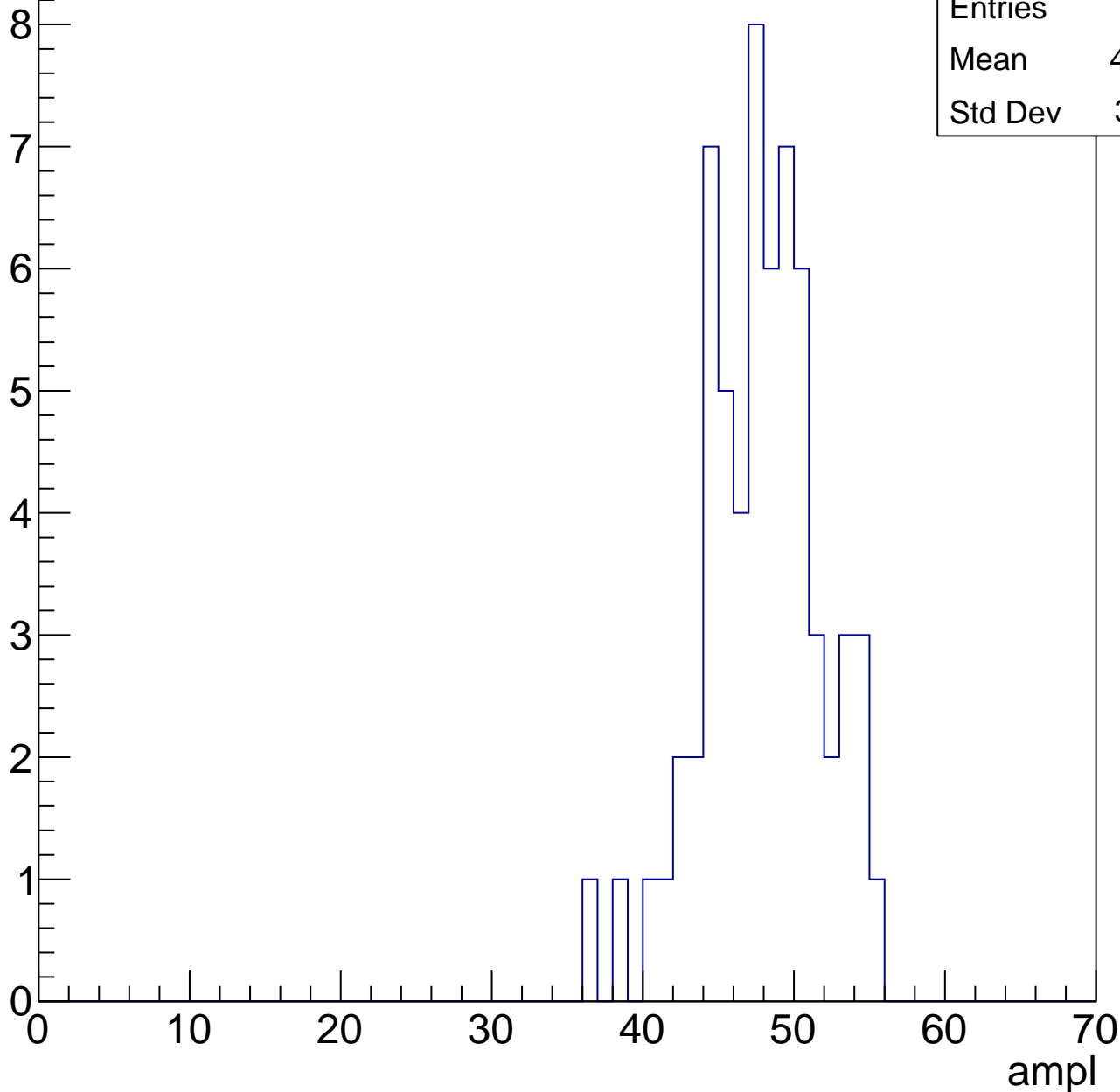


# B1L102S, U20-ch84, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	47.33
Std Dev	3.891

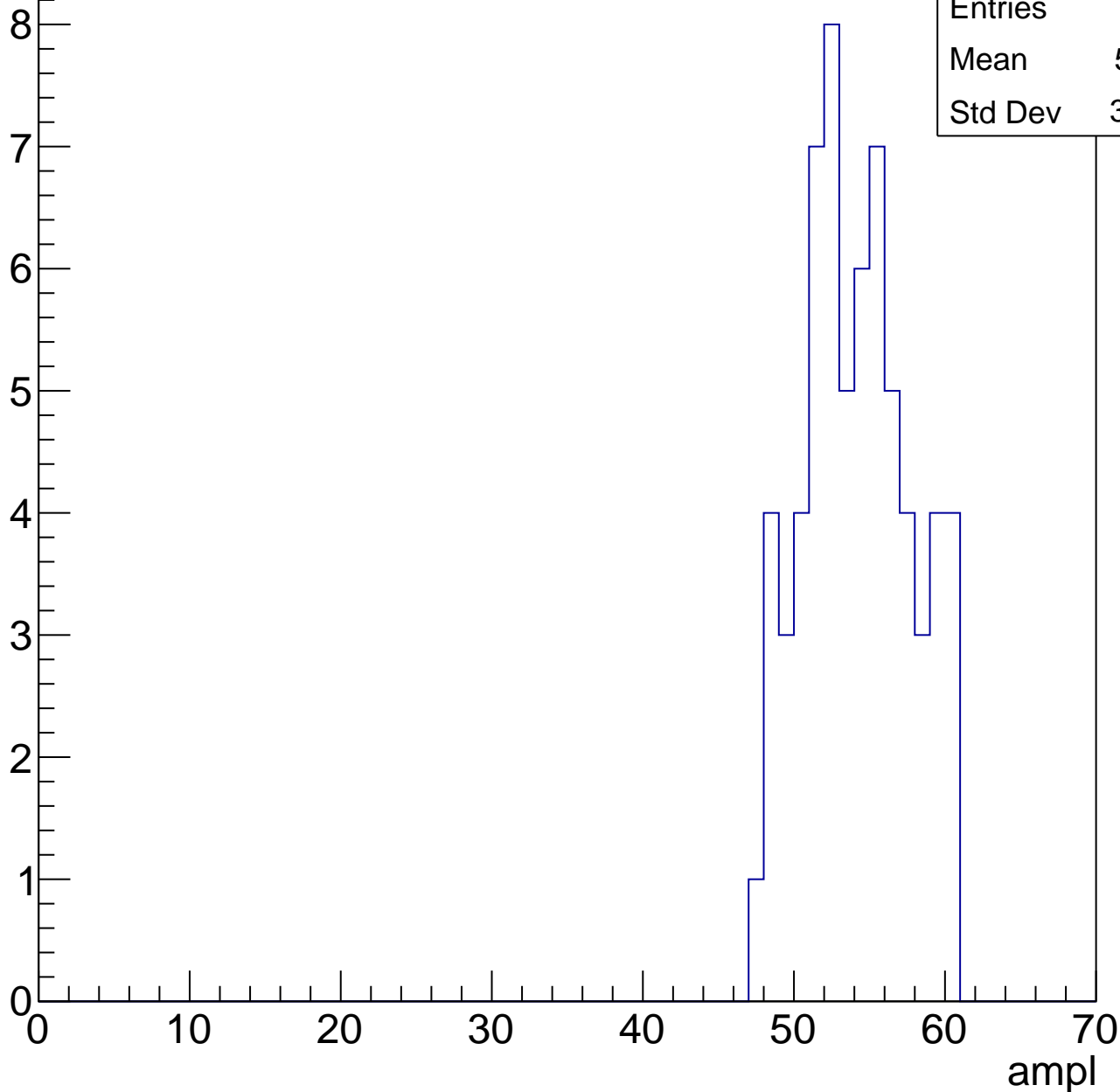


# B1L102S, U20-ch84, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	53.71
Std Dev	3.467

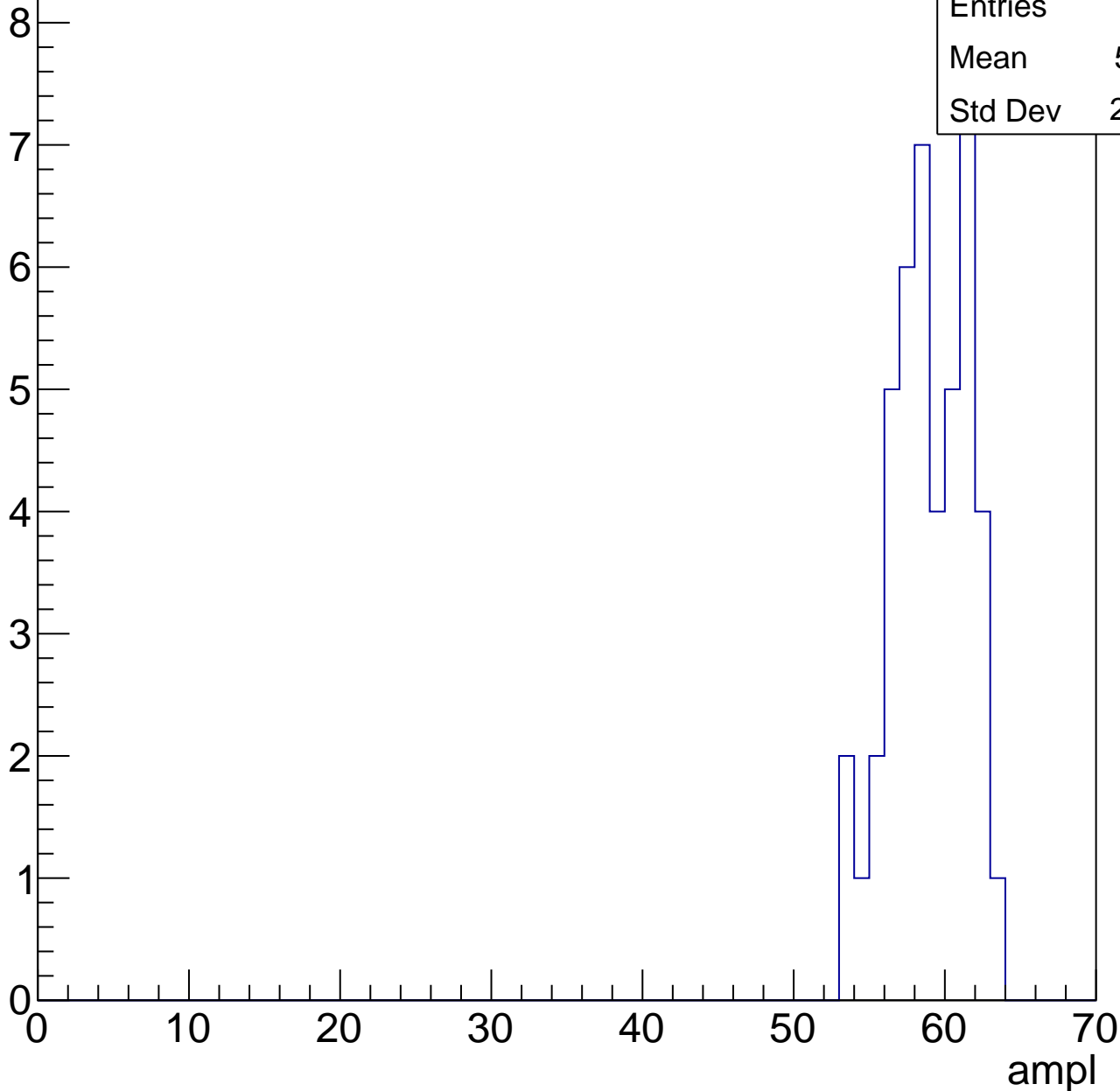


# B1L102S, U20-ch84, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	45
Mean	58.51
Std Dev	2.509

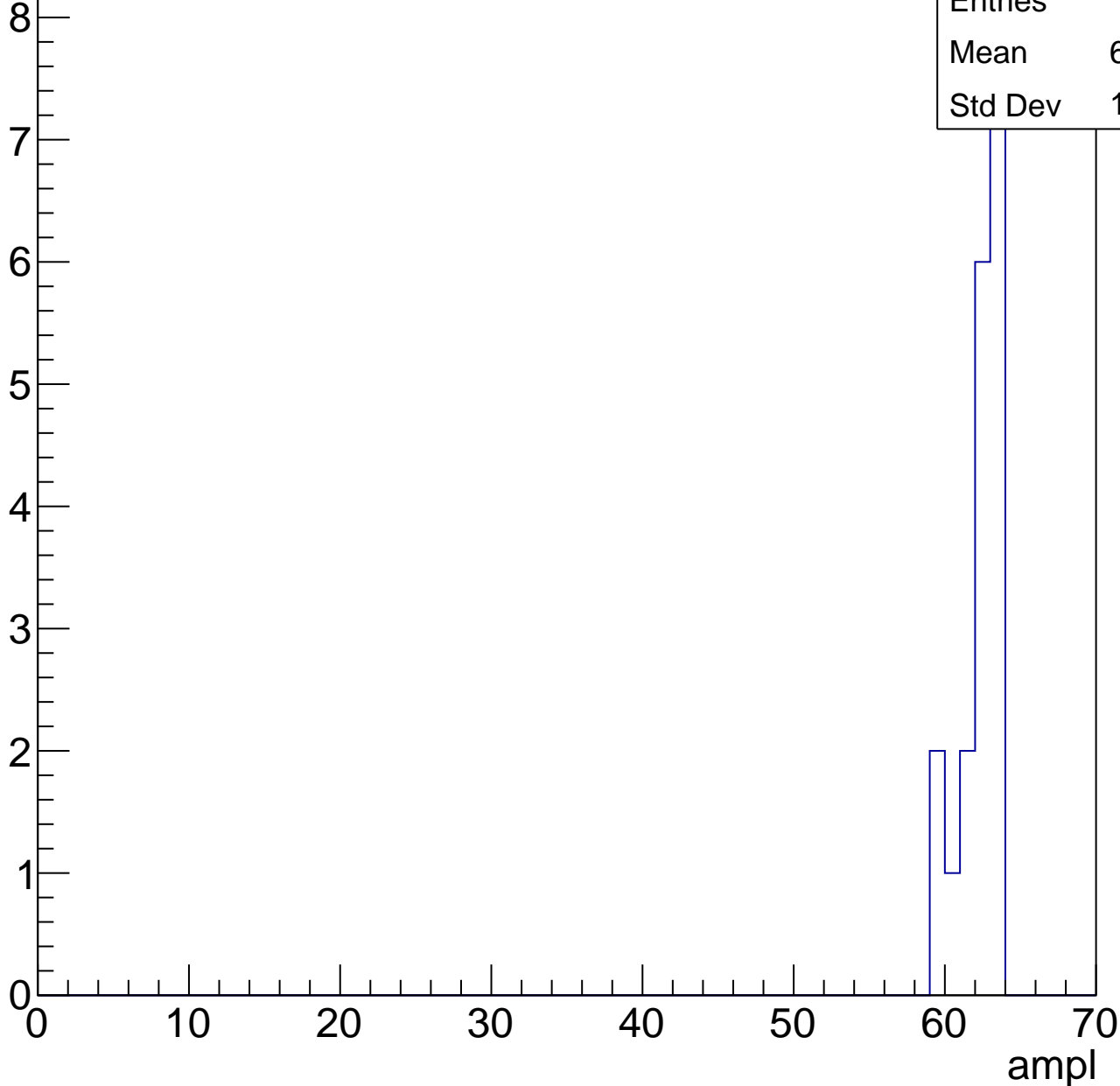


# B1L102S, U20-ch84, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	19
Mean	61.89
Std Dev	1.293

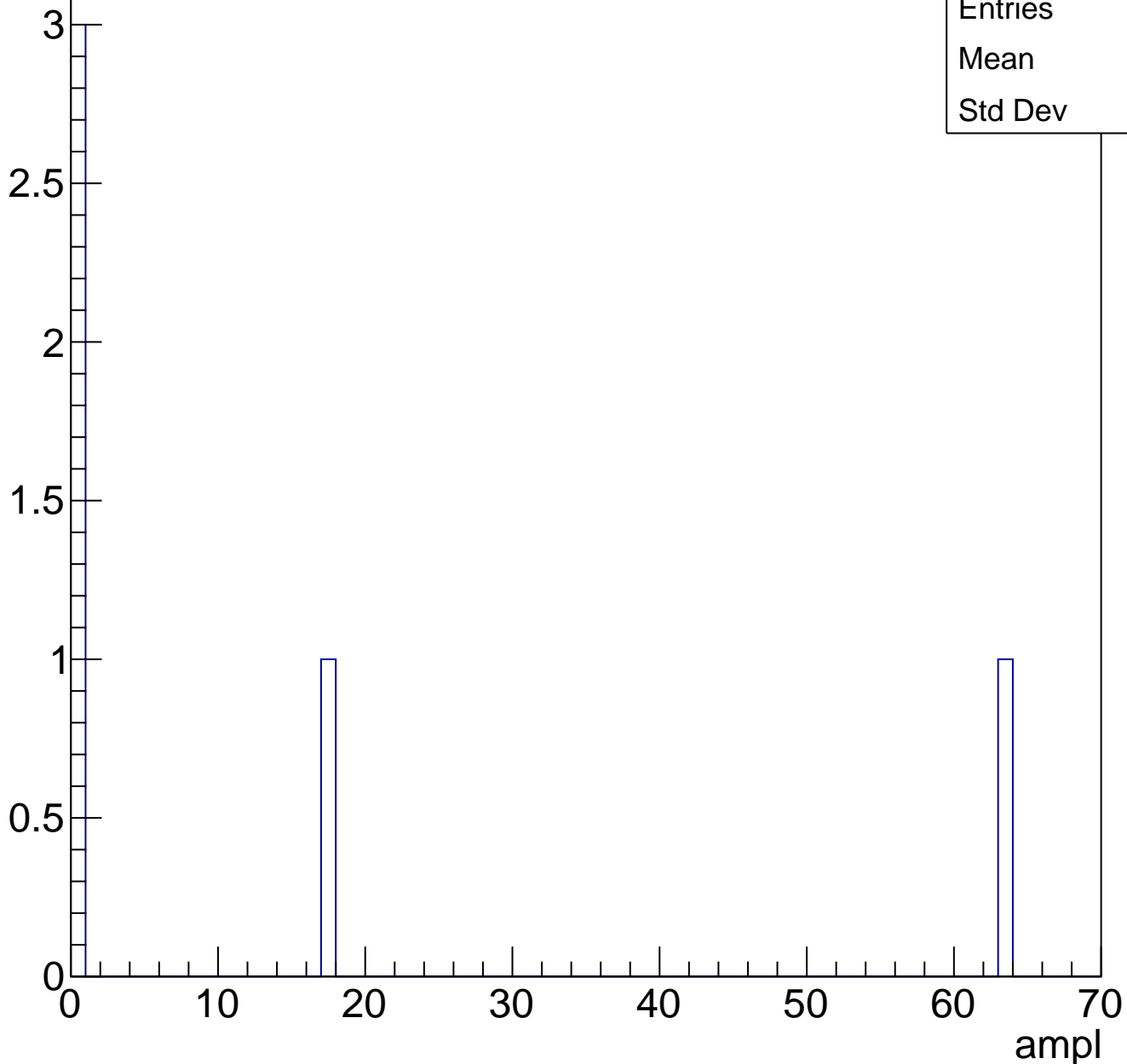




# B1L102S, U20-ch84, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	5
Mean	16
Std Dev	24.4

# B1L102S, U20-ch85, adc0

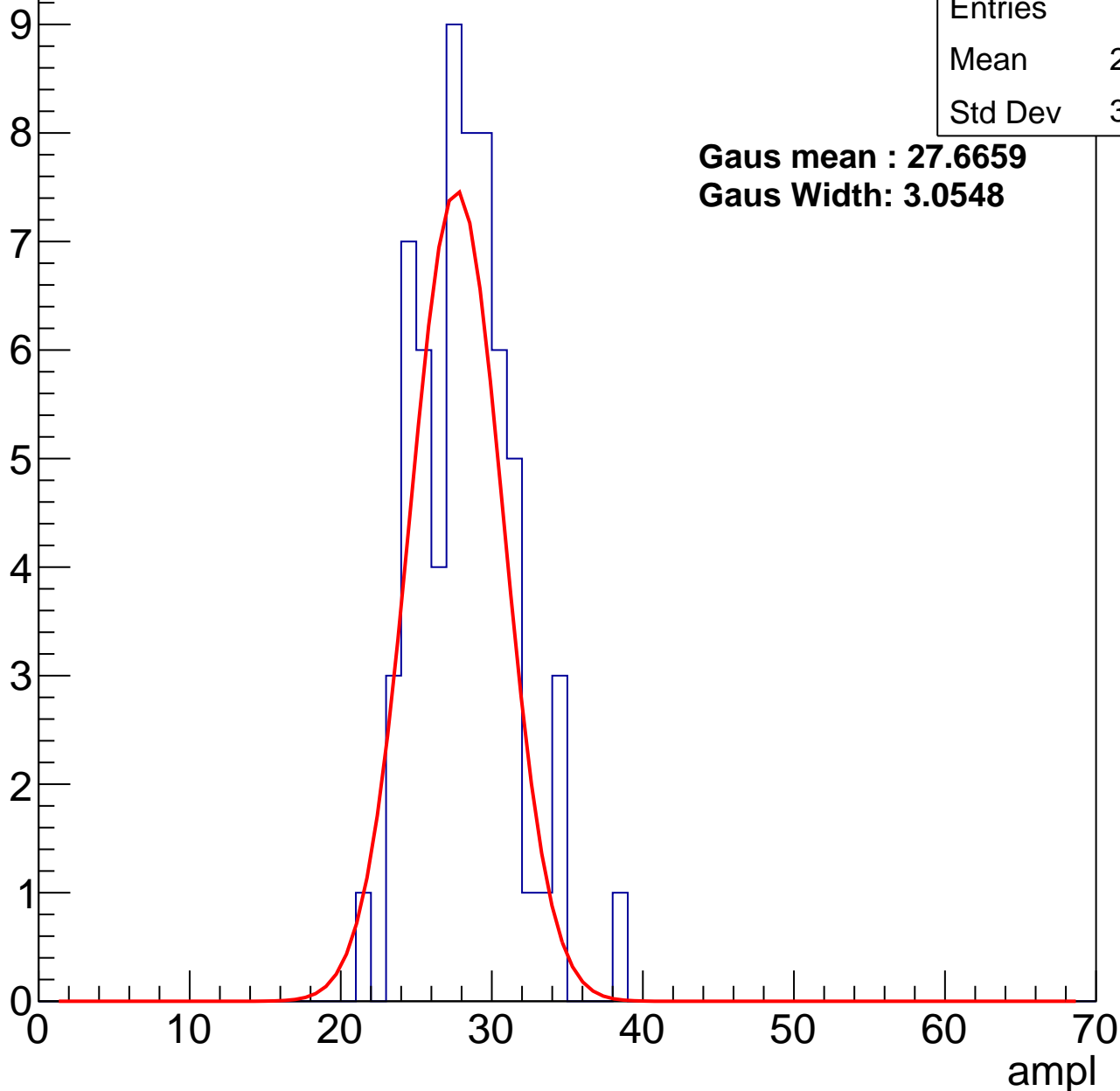
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	27.79
Std Dev	3.183

**Gaus mean : 27.6659**

**Gaus Width: 3.0548**



# B1L102S, U20-ch85, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	82
Mean	35.32
Std Dev	3.537

**Gaus mean : 35.8789**

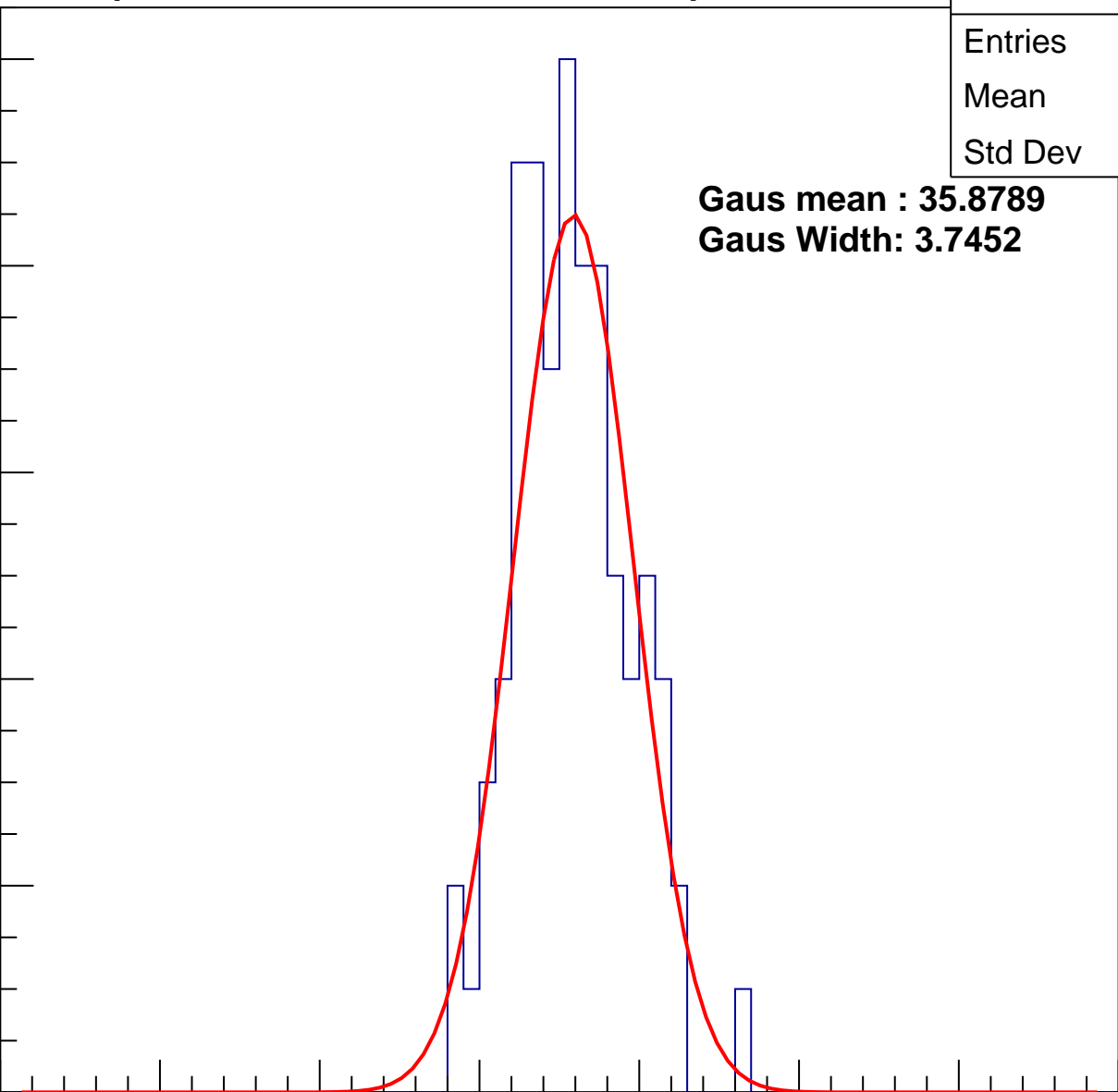
**Gaus Width: 3.7452**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U20-ch85, adc2

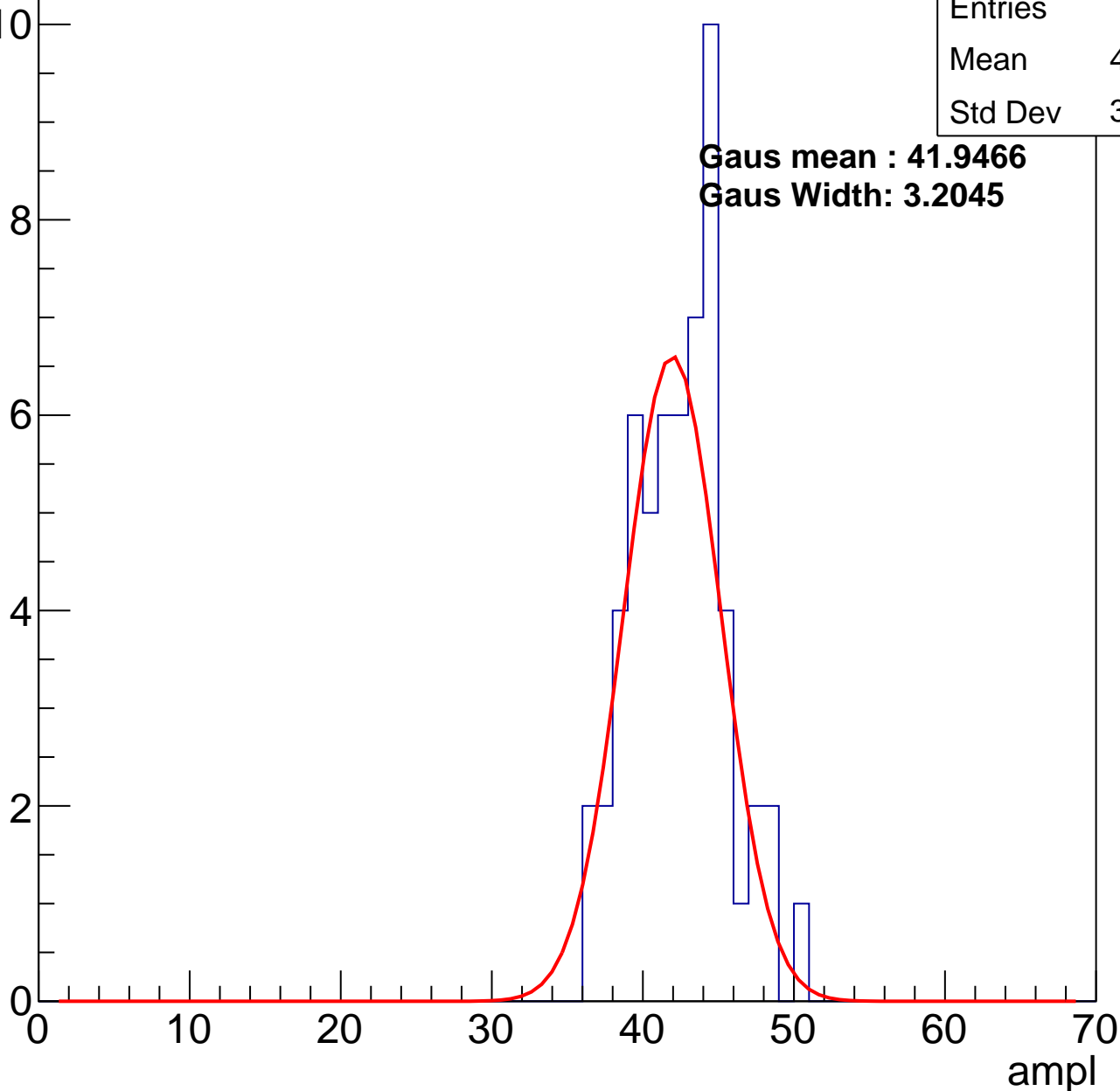
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	42.02
Std Dev	3.082

**Gaus mean : 41.9466**

**Gaus Width: 3.2045**

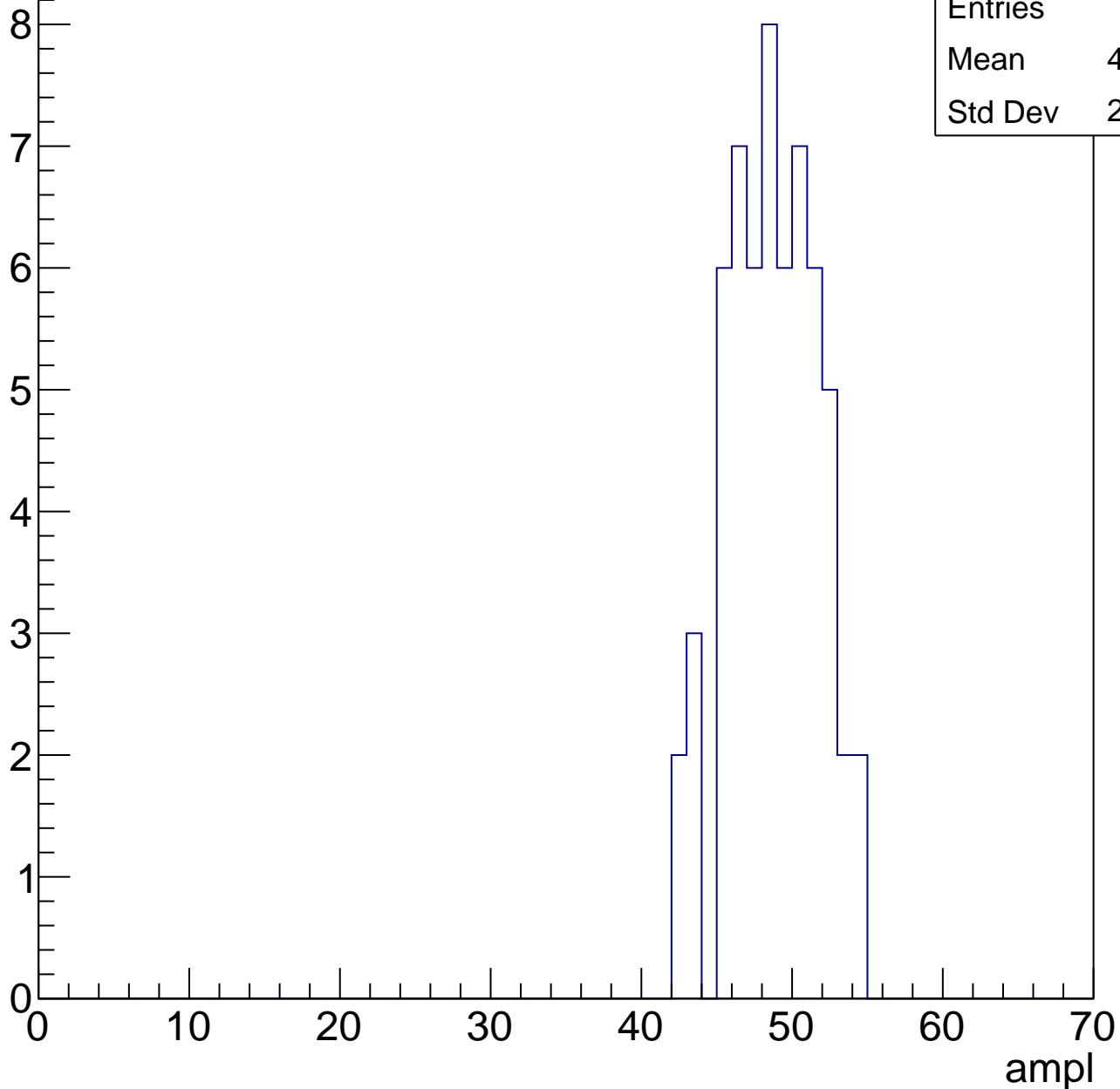


# B1L102S, U20-ch85, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	48.25
Std Dev	2.947

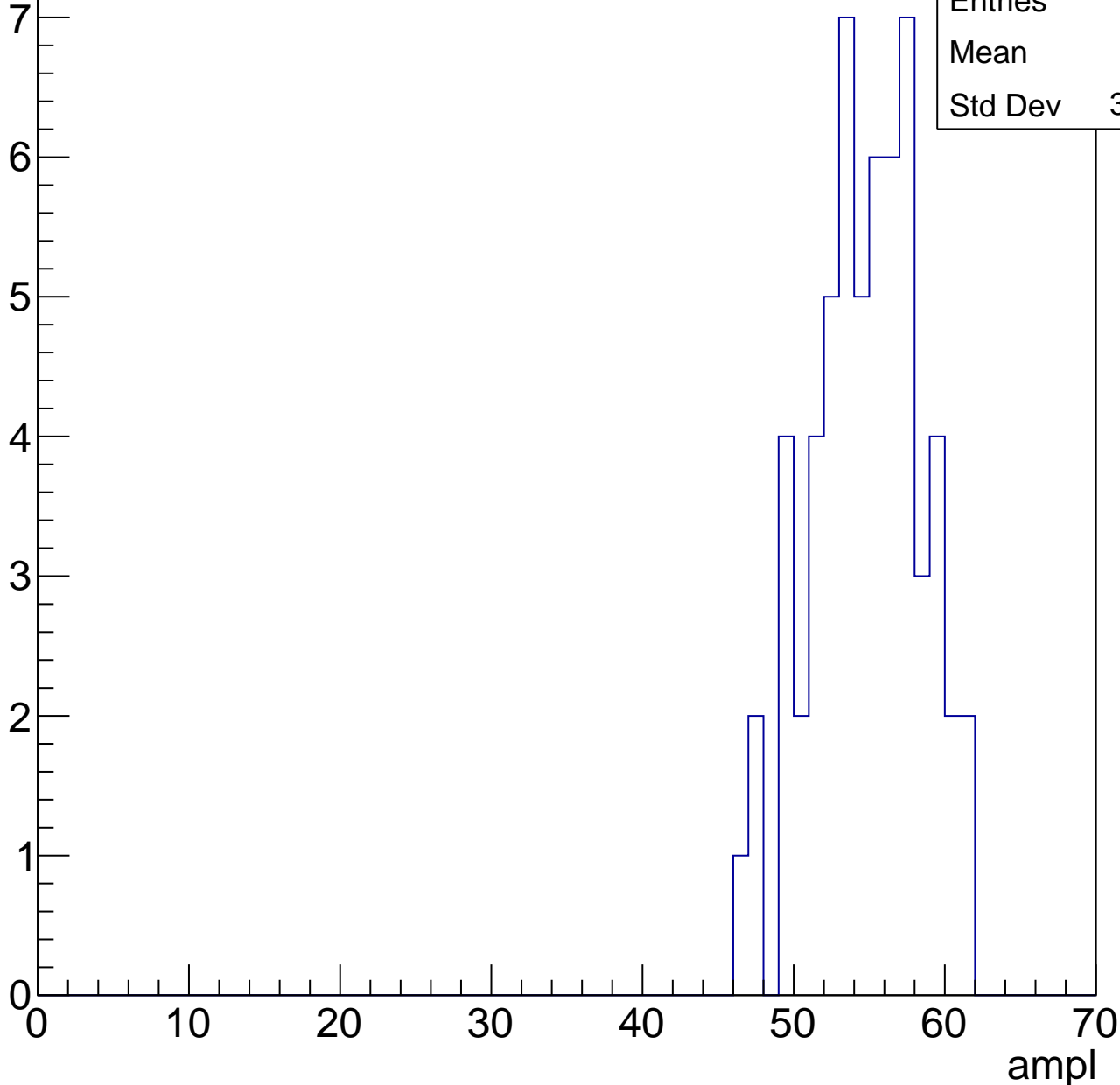


# B1L102S, U20-ch85, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	54.3
Std Dev	3.565



# B1L102S, U20-ch85, adc5

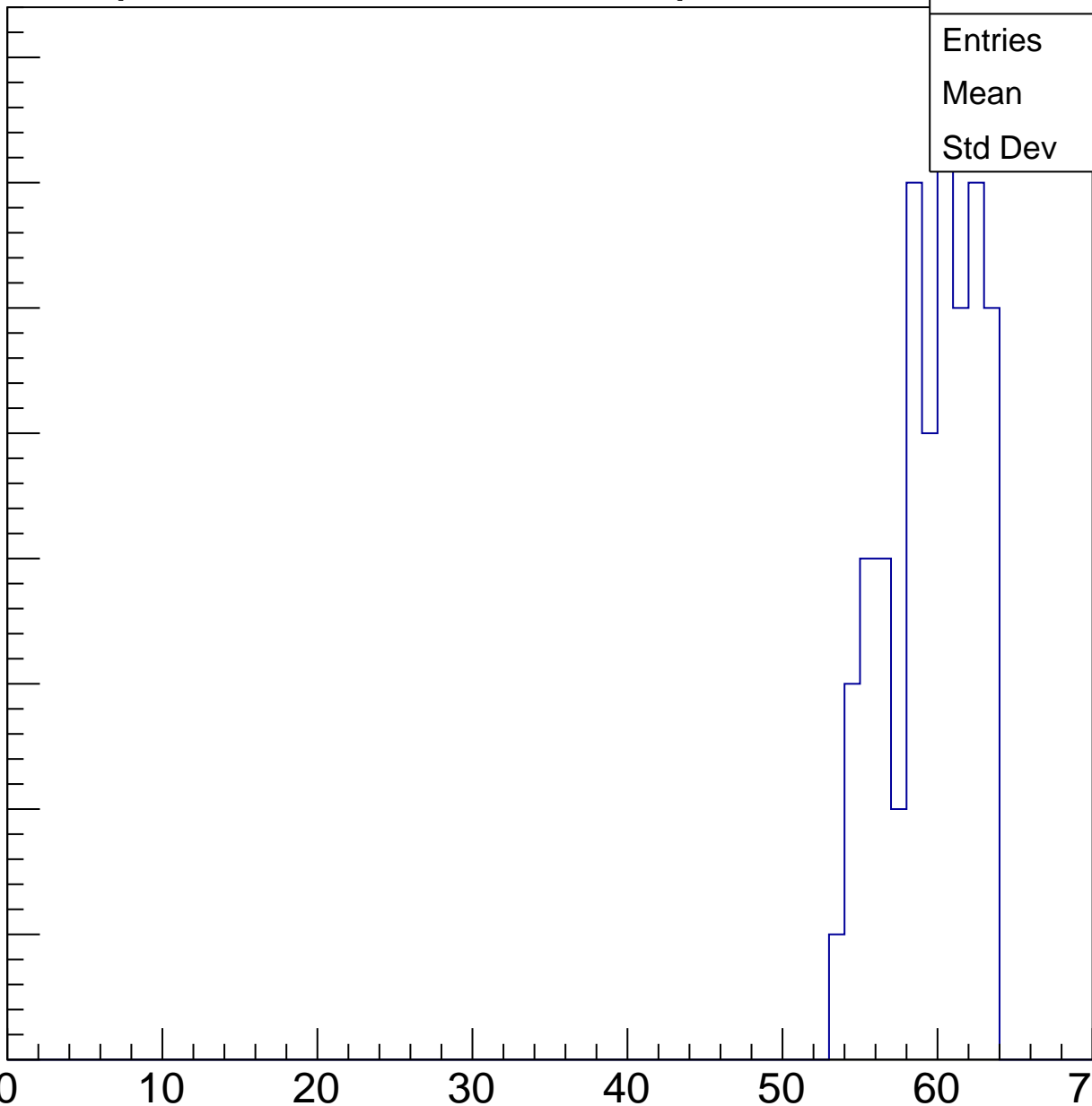
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	53
Mean	59.09
Std Dev	2.803

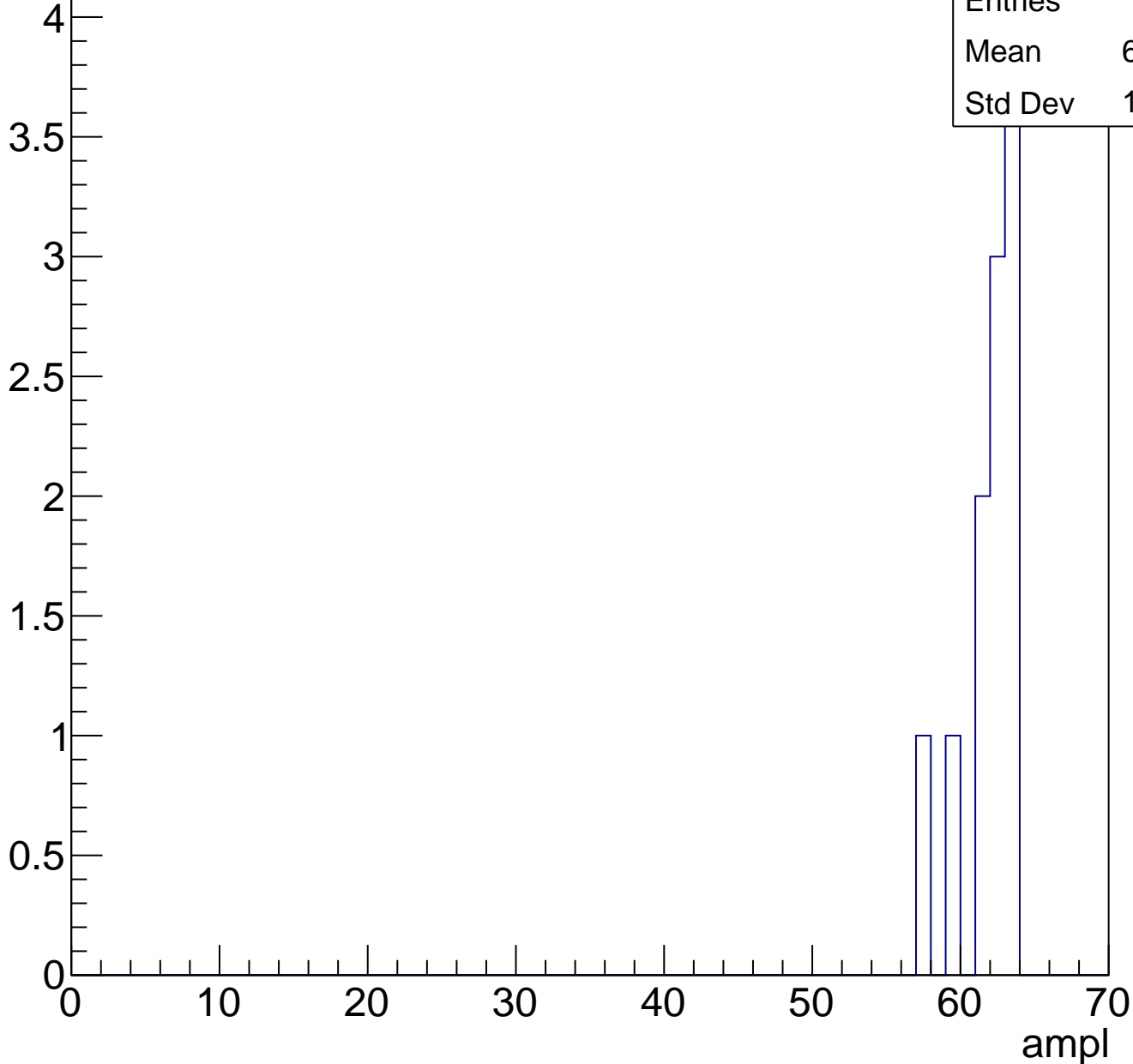
ampl



# B1L102S, U20-ch85, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U20-ch85, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L102S, U20-ch86, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	77
Mean	28.48
Std Dev	5.003

**Gaus mean : 29.8589**

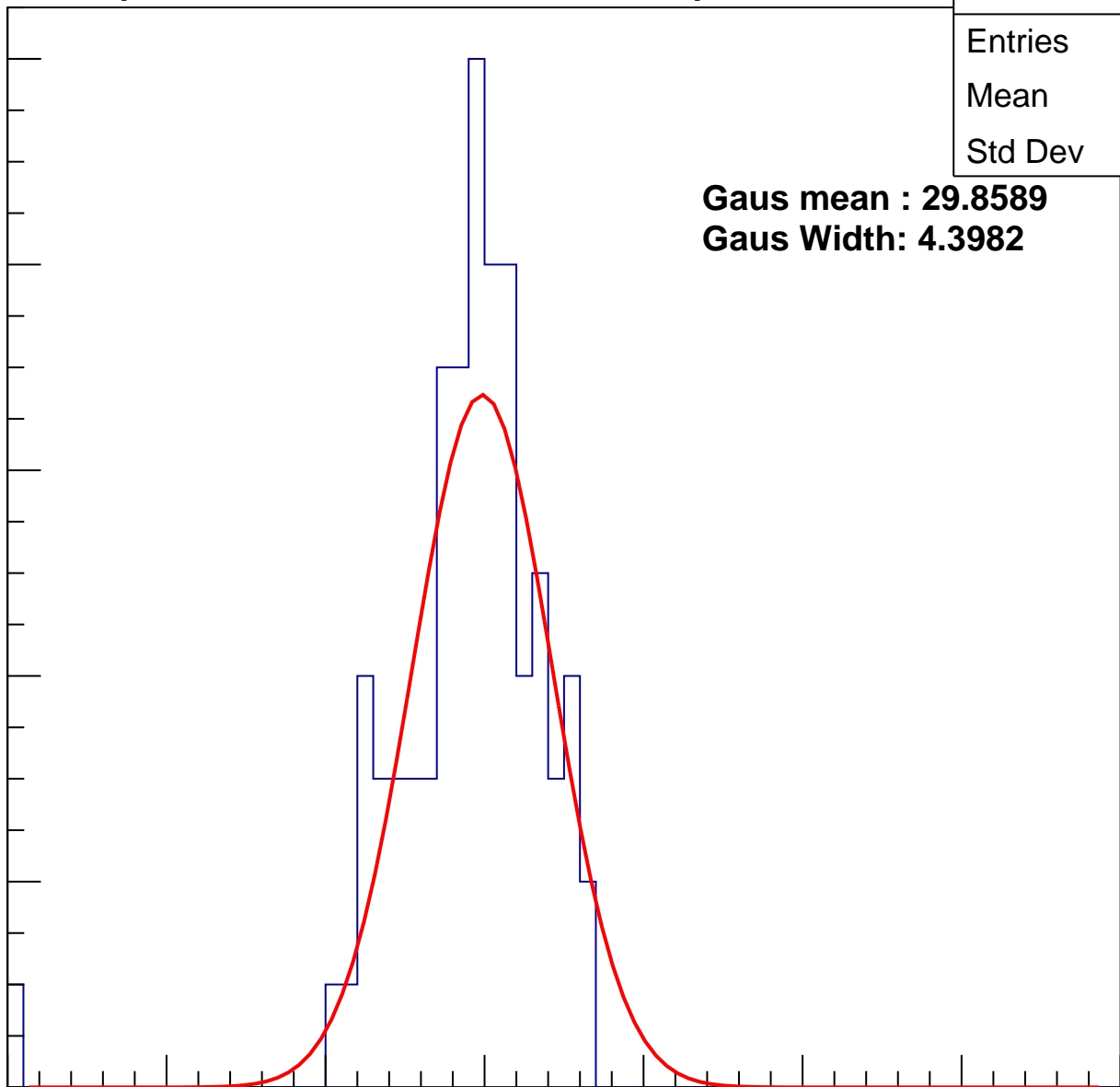
**Gaus Width: 4.3982**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U20-ch86, adc1

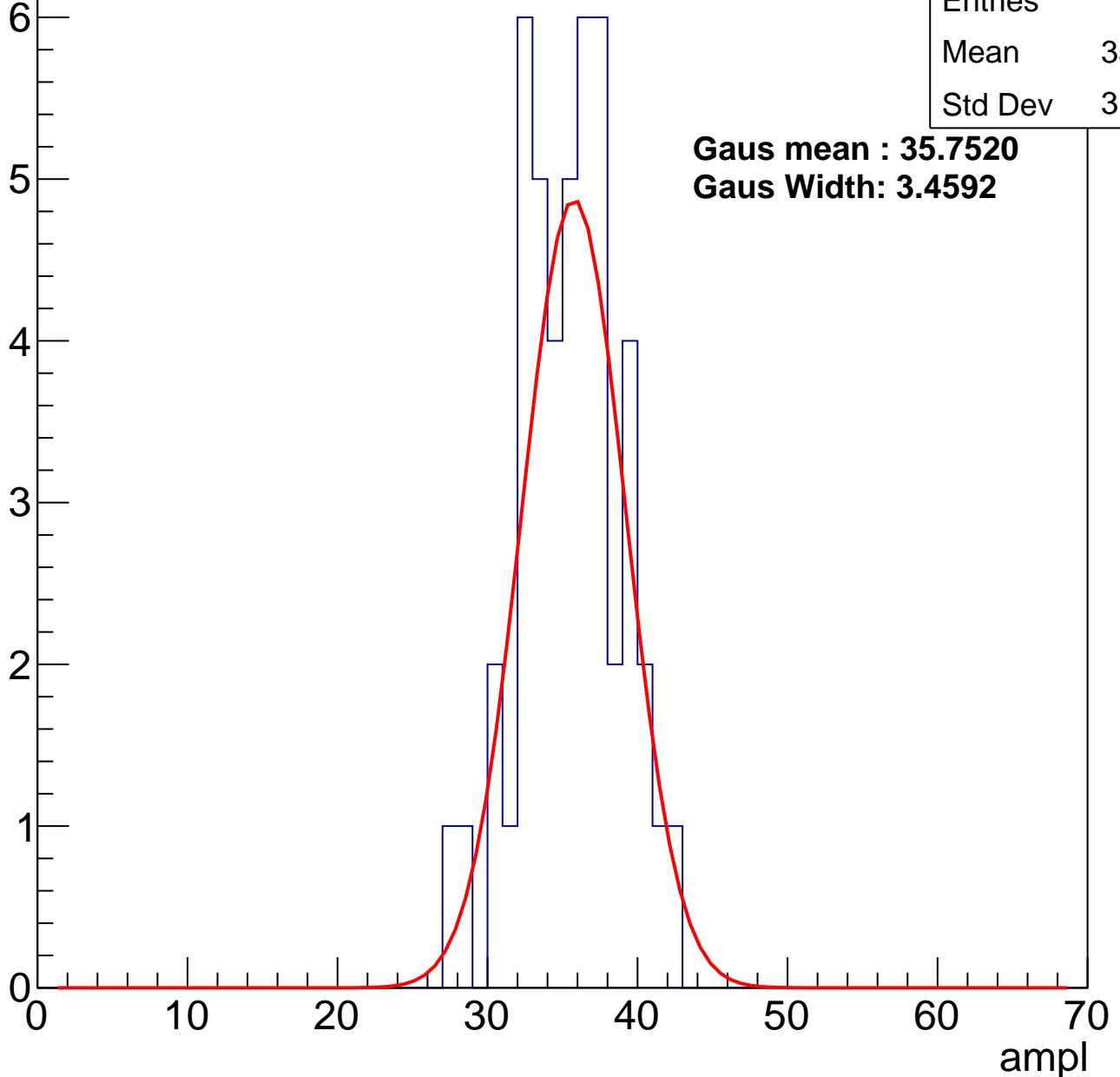
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	47
Mean	35.04
Std Dev	3.274

**Gaus mean : 35.7520**

**Gaus Width: 3.4592**



# B1L102S, U20-ch86, adc2

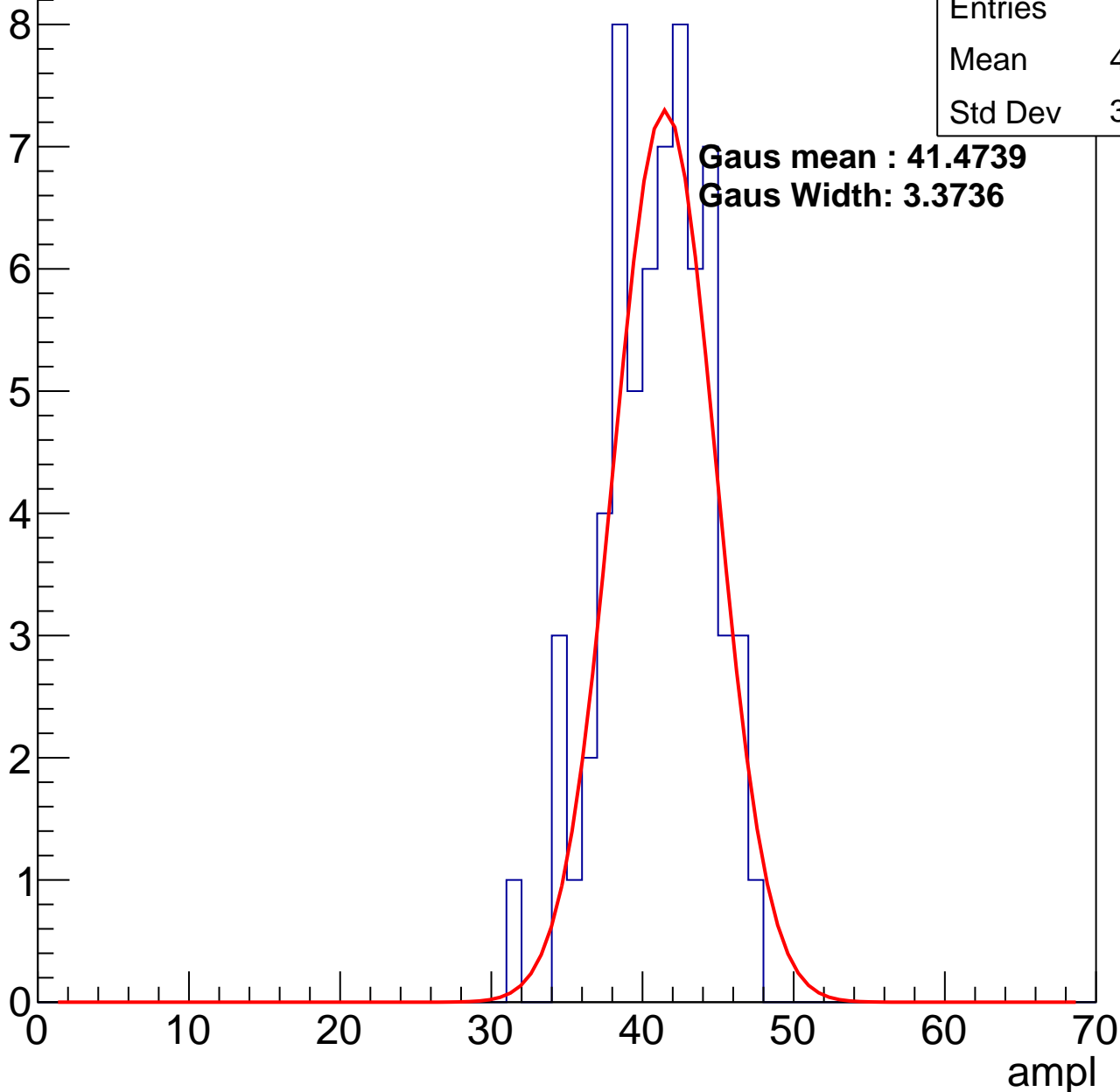
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	40.55
Std Dev	3.365

**Gaus mean : 41.4739**

**Gaus Width: 3.3736**

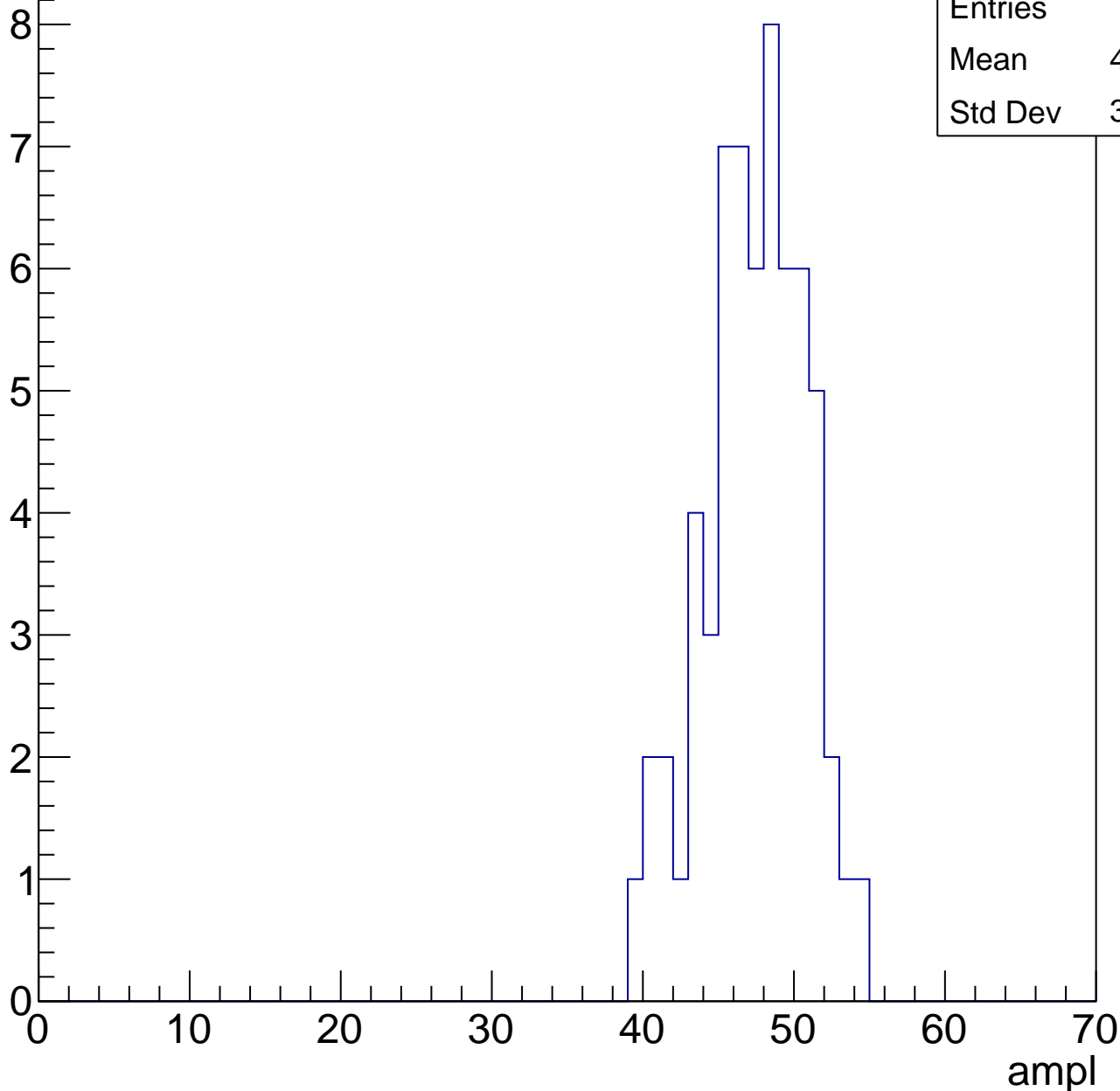


# B1L102S, U20-ch86, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	46.94
Std Dev	3.326

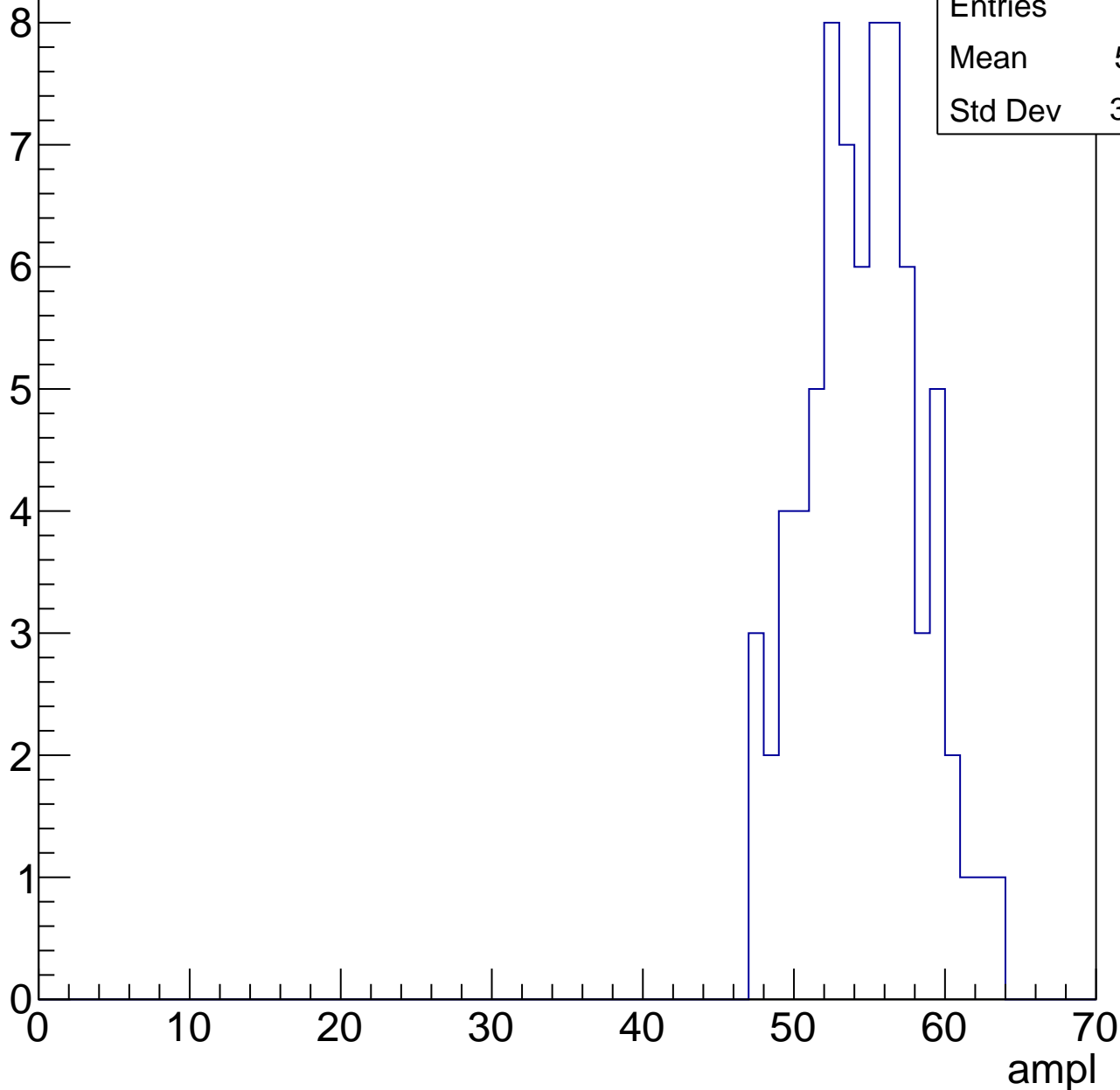


# B1L102S, U20-ch86, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

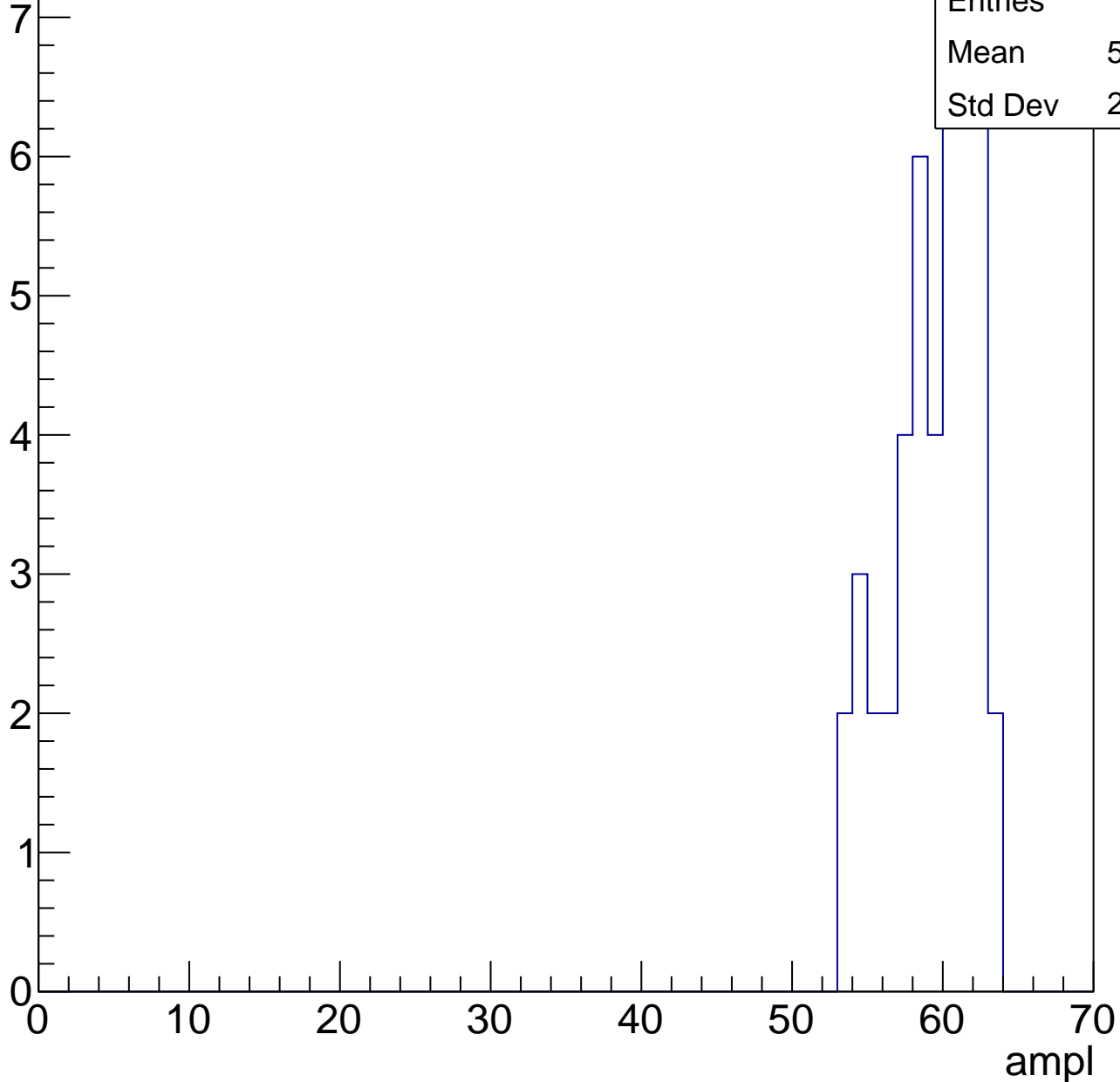
Entries	74
Mean	54.11
Std Dev	3.674



# B1L102S, U20-ch86, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

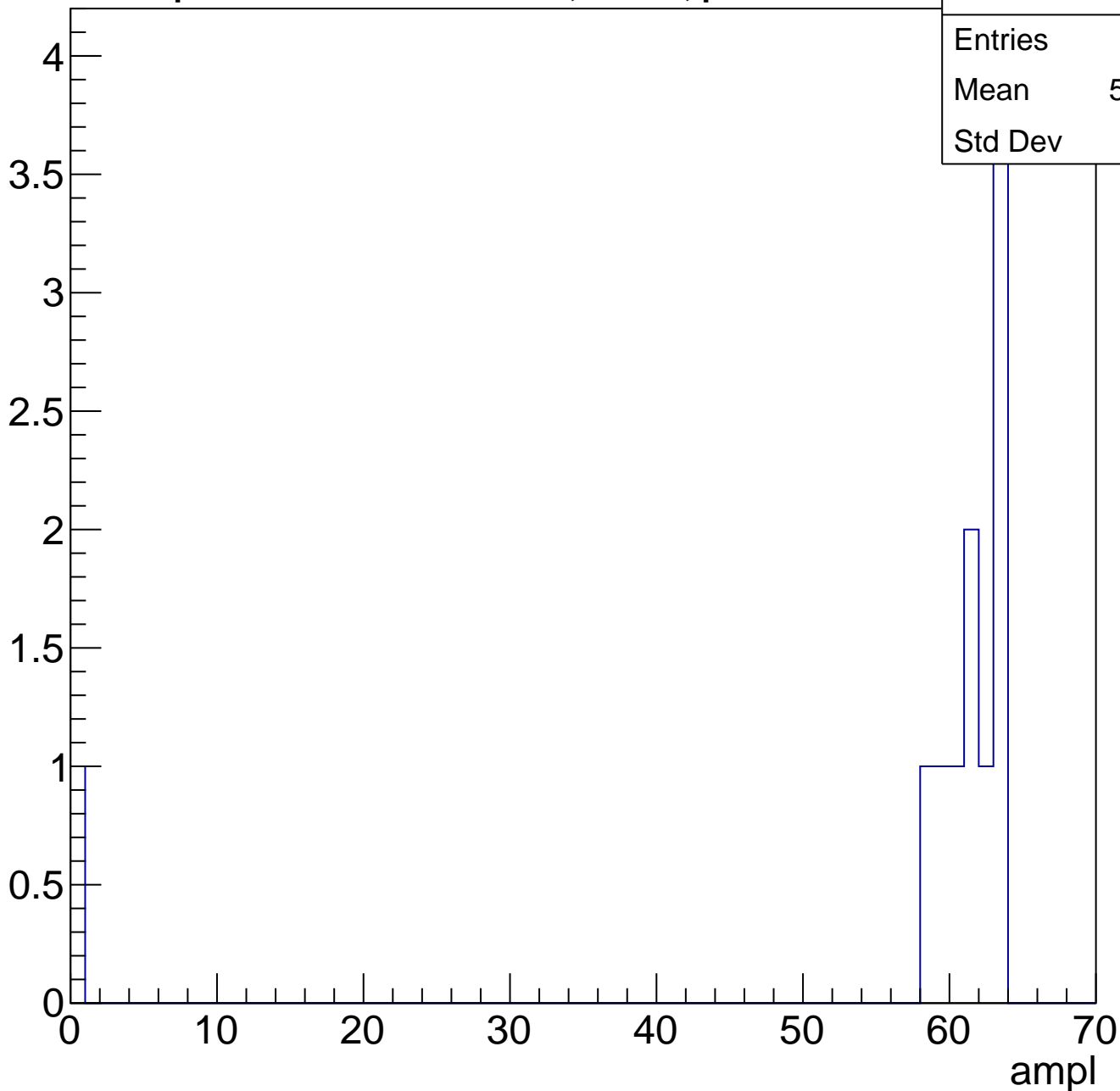
Entry



# B1L102S, U20-ch86, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

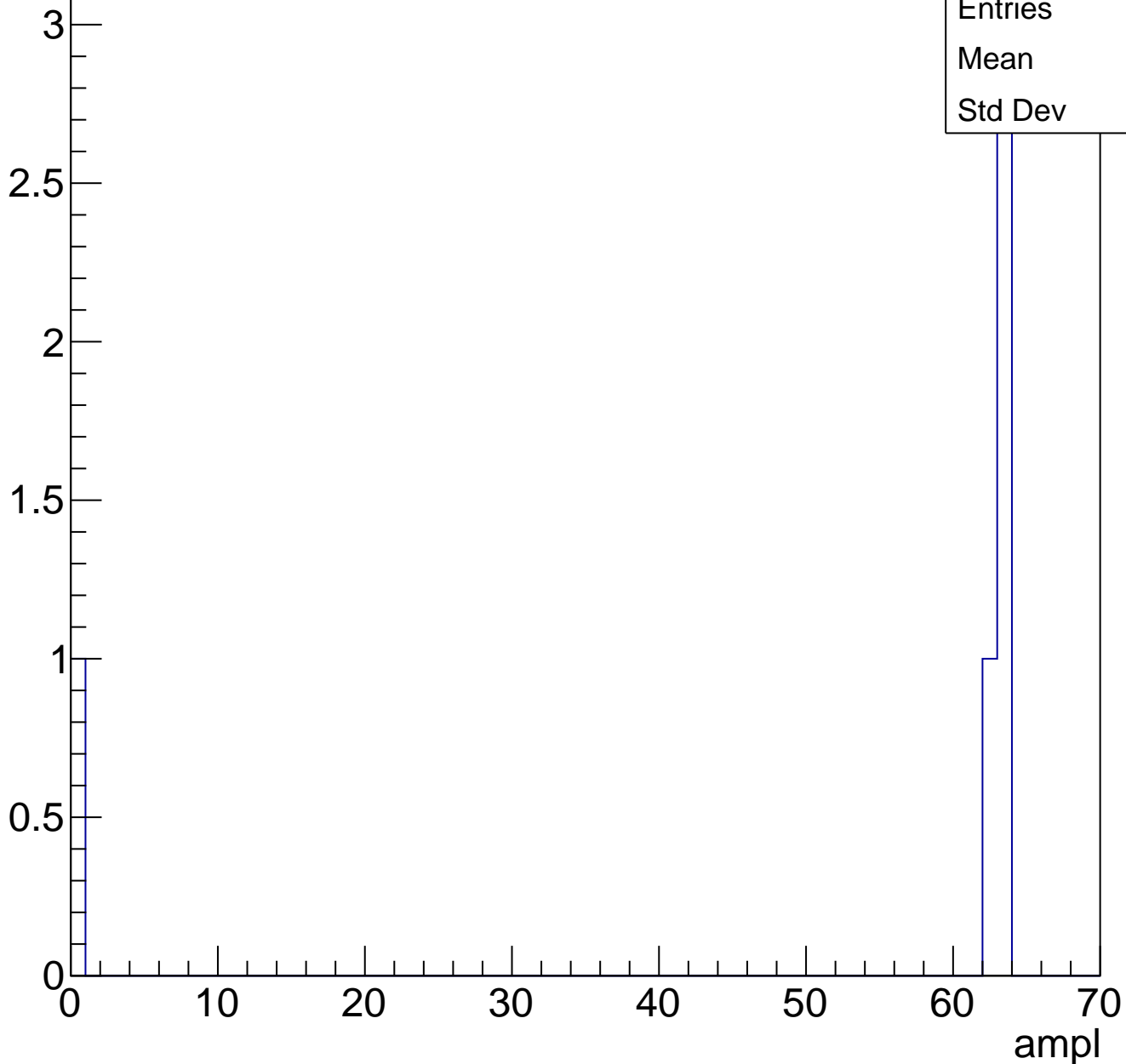




# B1L102S, U20-ch86, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch87, adc0

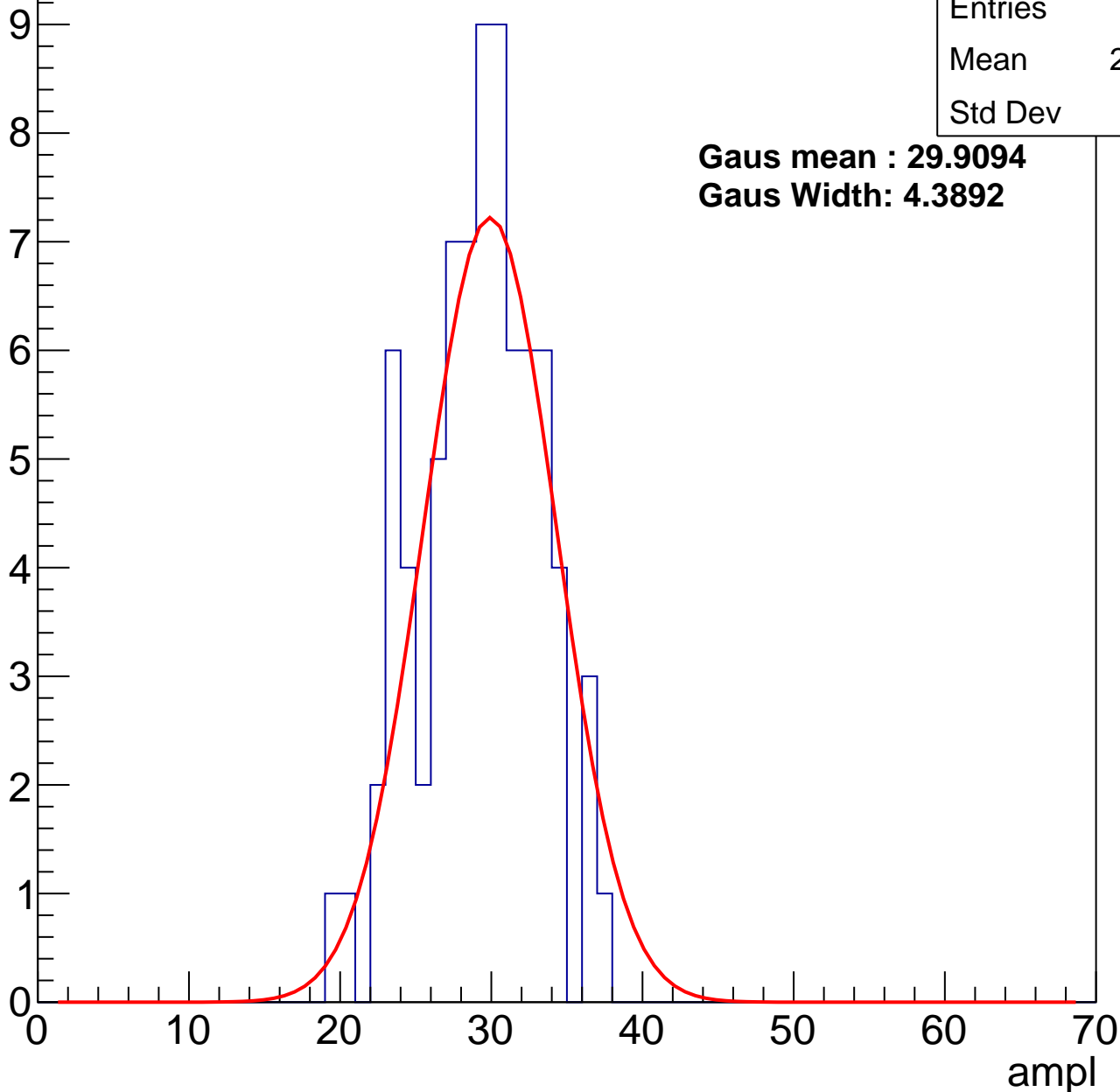
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	79
Mean	28.73
Std Dev	3.89

**Gaus mean : 29.9094**

**Gaus Width: 4.3892**



# B1L102S, U20-ch87, adc1

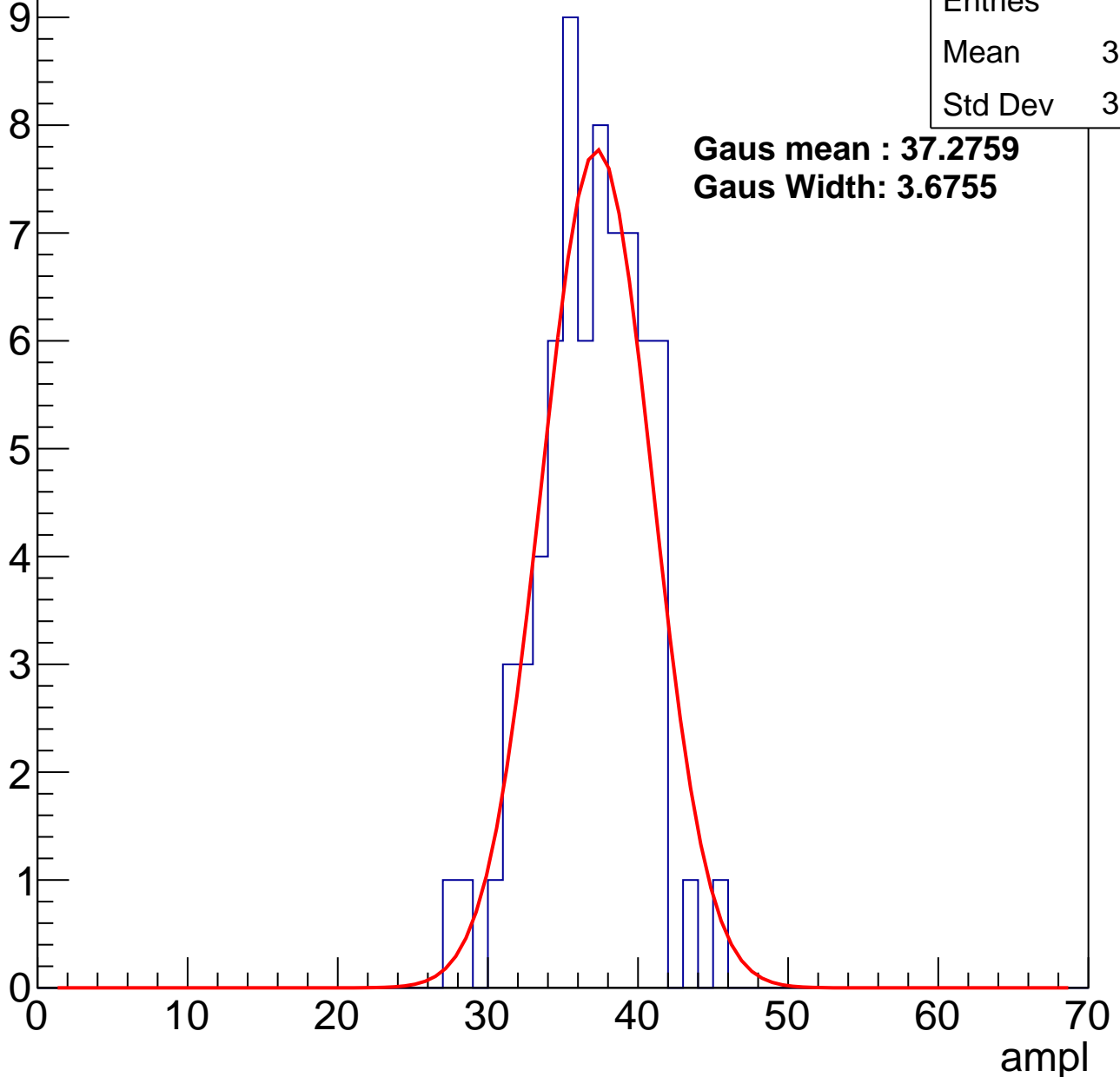
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	36.43
Std Dev	3.454

**Gaus mean : 37.2759**

**Gaus Width: 3.6755**



# B1L102S, U20-ch87, adc2

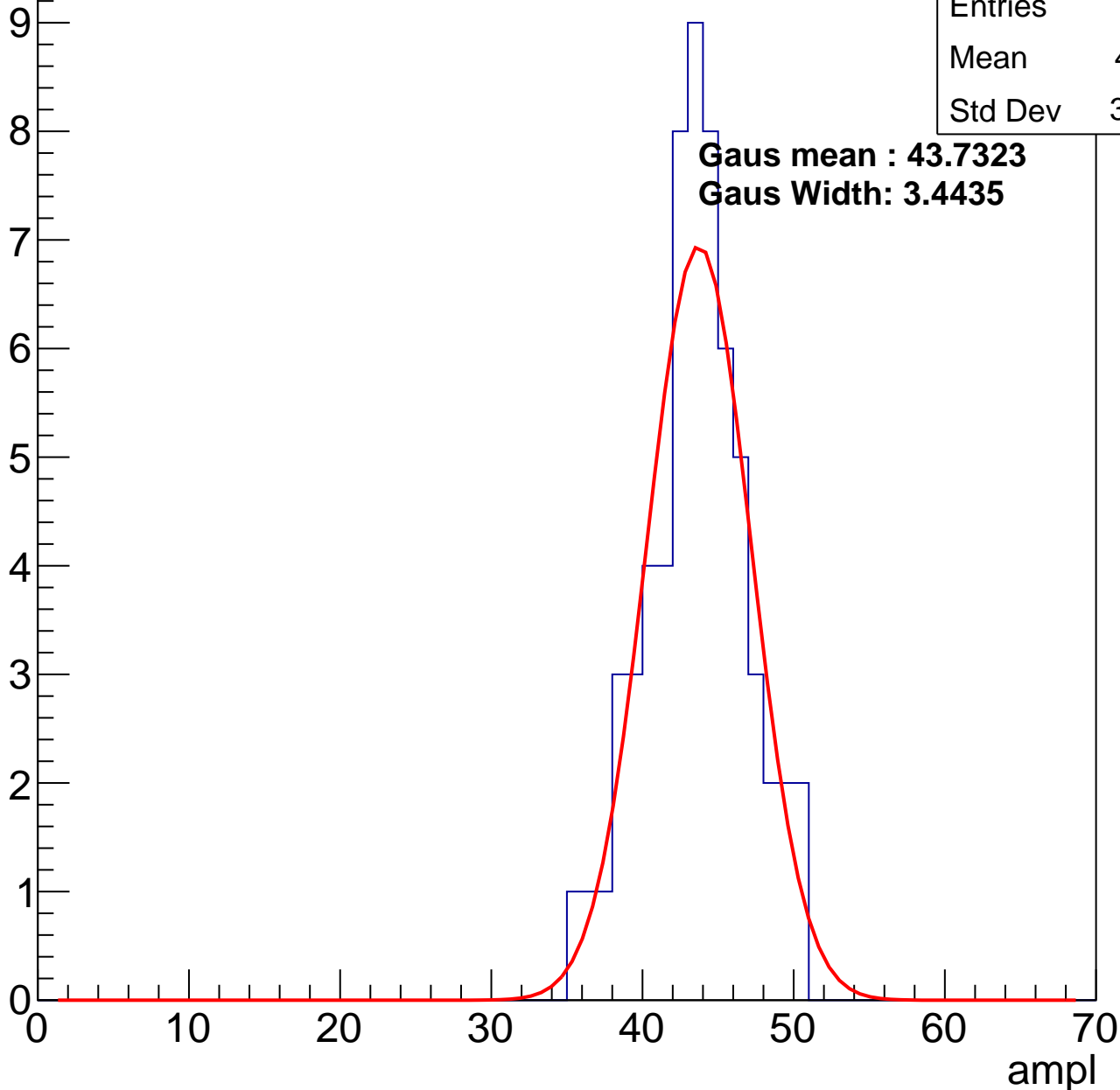
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	43.11
Std Dev	3.303

**Gaus mean : 43.7323**

**Gaus Width: 3.4435**

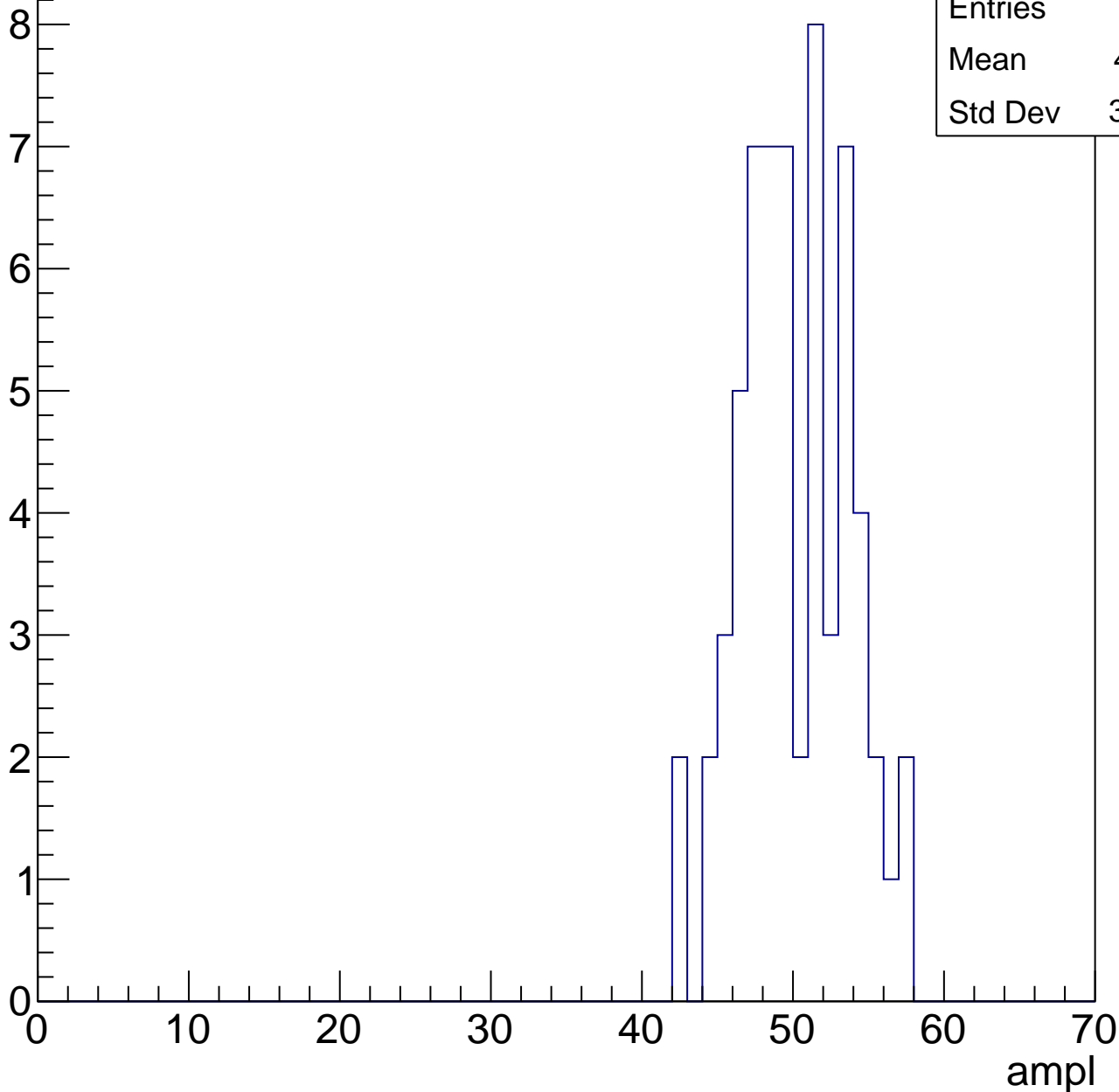


# B1L102S, U20-ch87, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

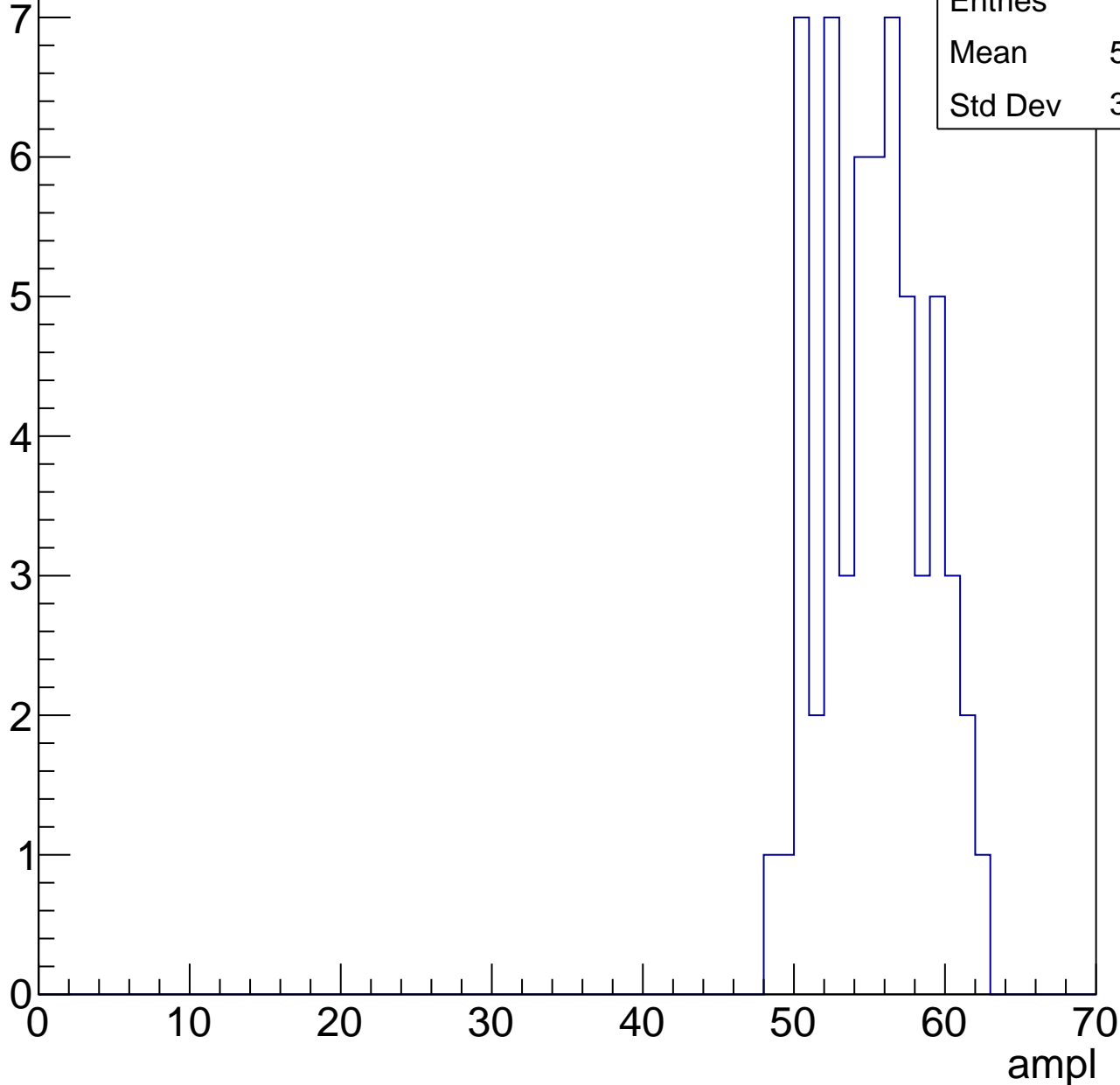
Entries	62
Mean	49.61
Std Dev	3.535



# B1L102S, U20-ch87, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch87, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

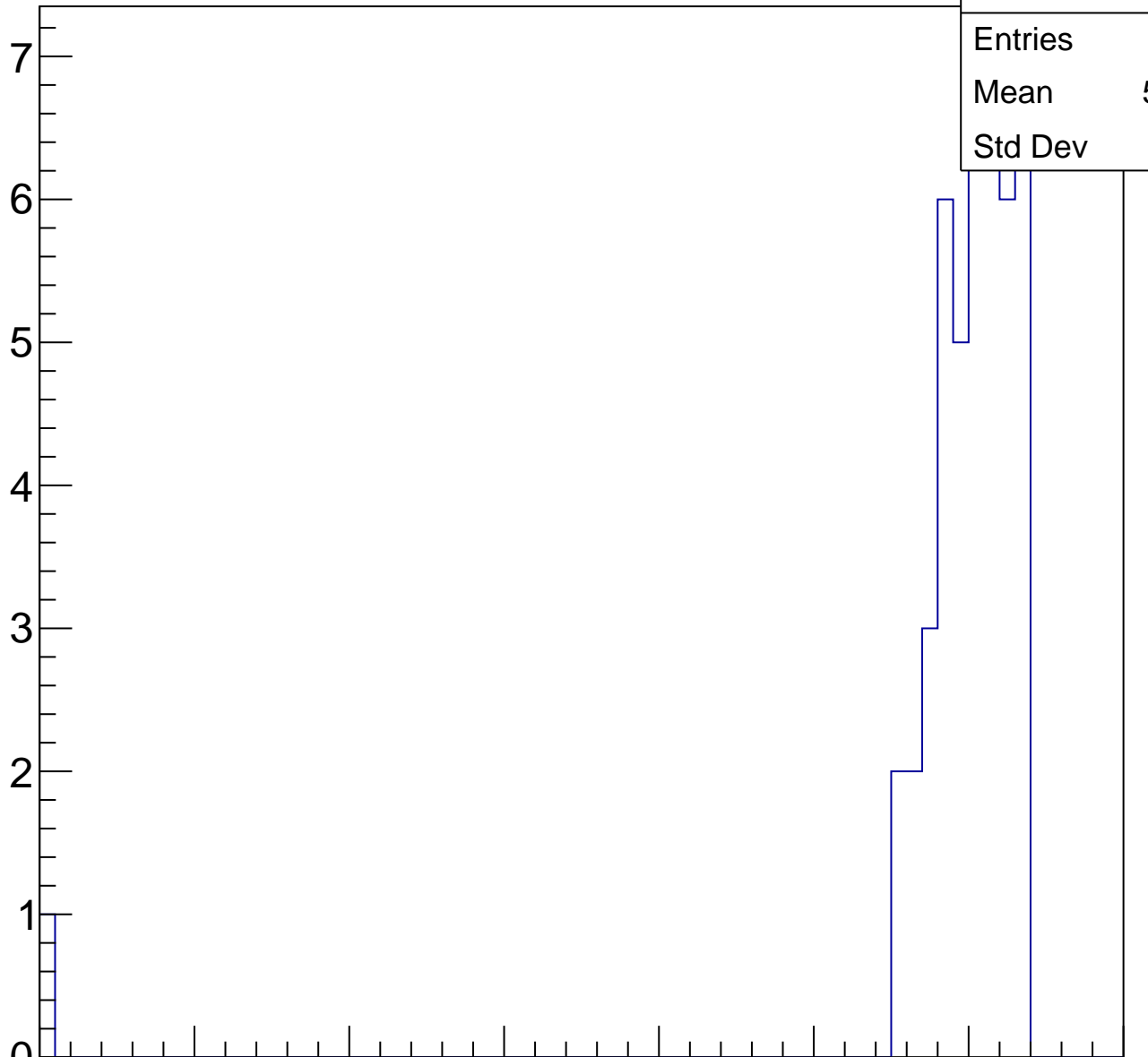
Entry

7  
6  
5  
4  
3  
2  
1  
0

Entries	46
Mean	58.61
Std Dev	9.02

ampl

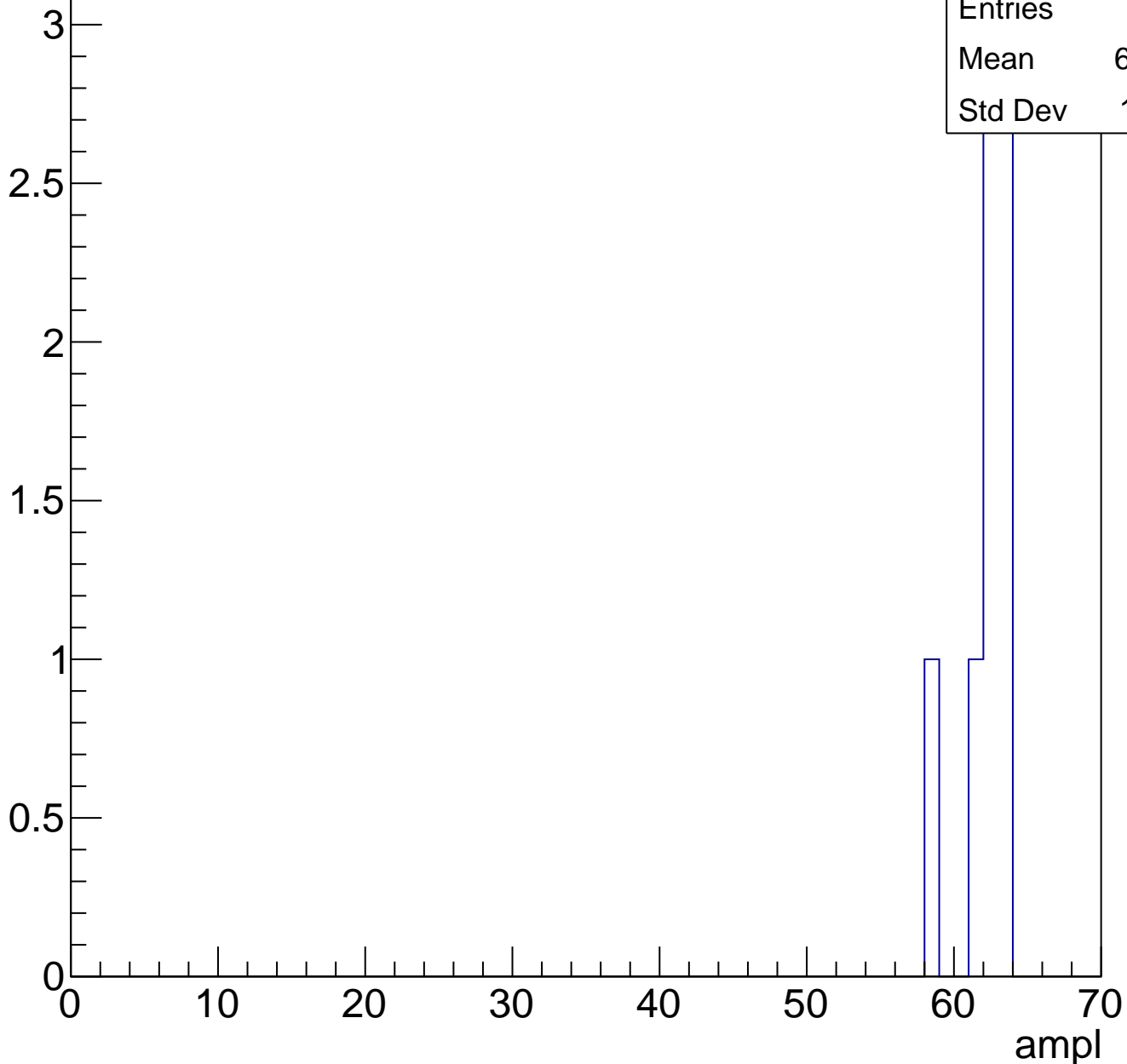
0 10 20 30 40 50 60 70



# B1L102S, U20-ch87, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U20-ch87, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U20-ch88, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	86
Mean	28.08
Std Dev	4.644

**Gaus mean : 28.7272**

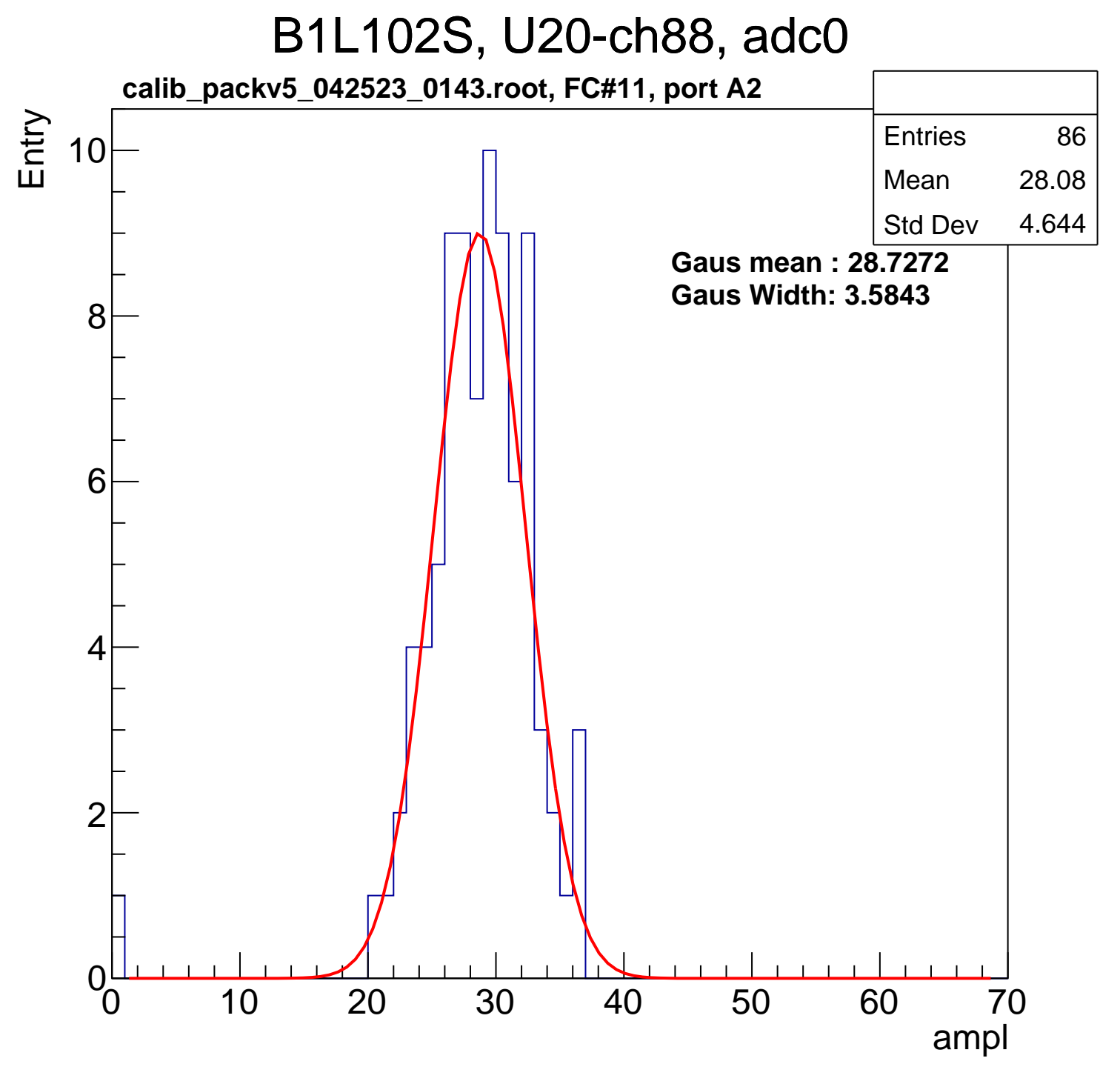
**Gaus Width: 3.5843**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



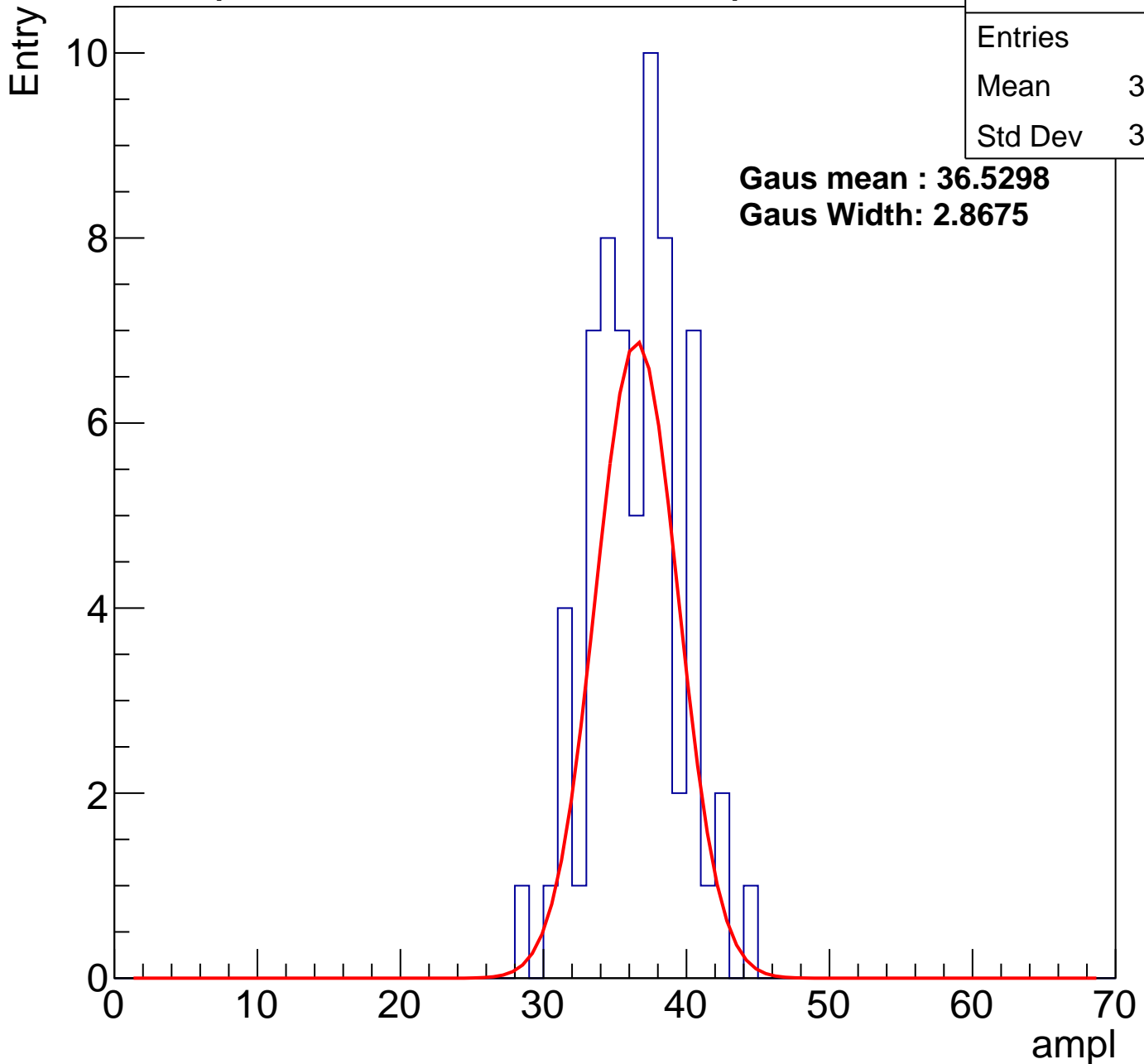
# B1L102S, U20-ch88, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	65
Mean	36.05
Std Dev	3.164

**Gaus mean : 36.5298**

**Gaus Width: 2.8675**



# B1L102S, U20-ch88, adc2

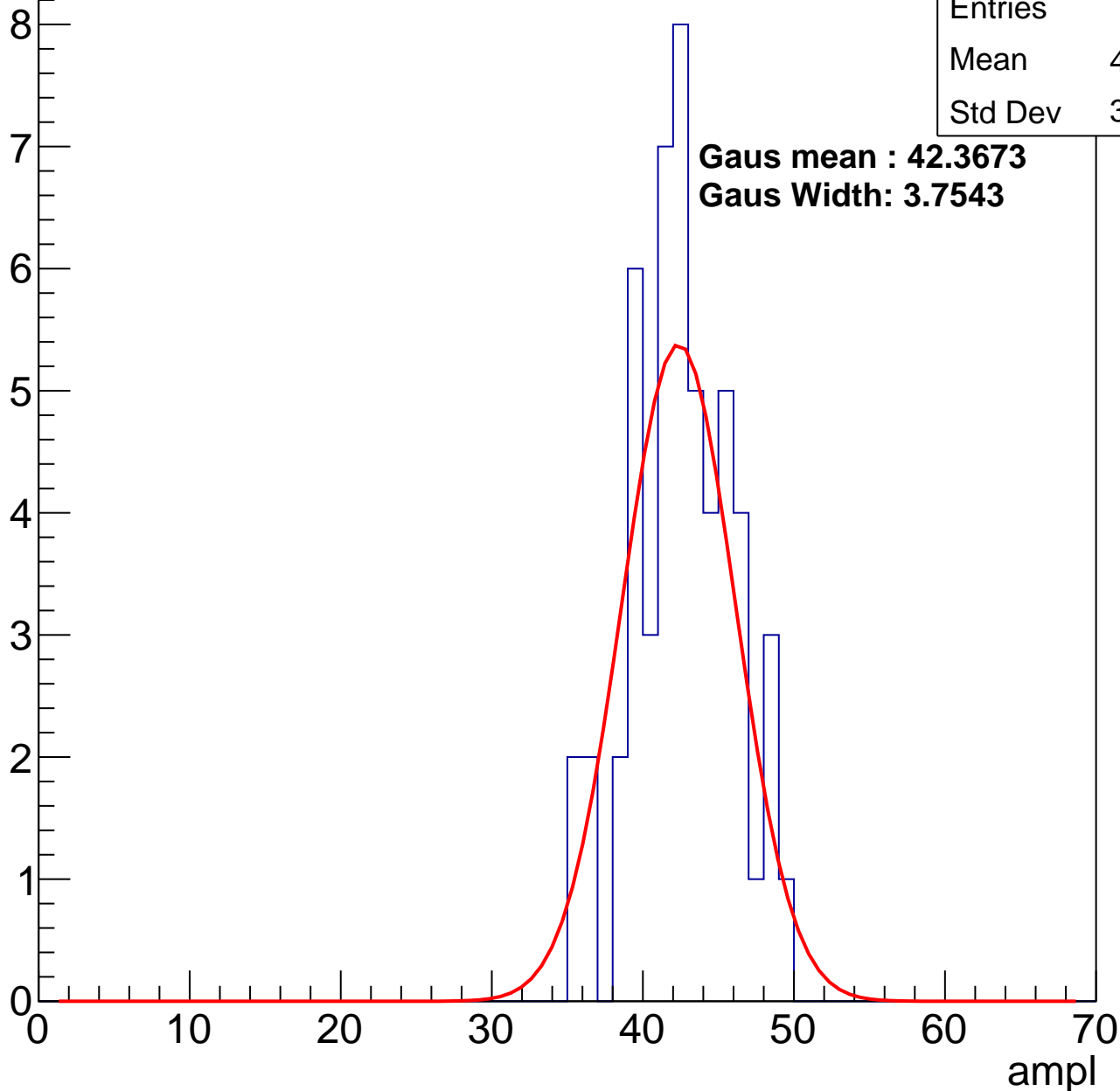
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	42.17
Std Dev	3.324

**Gaus mean : 42.3673**

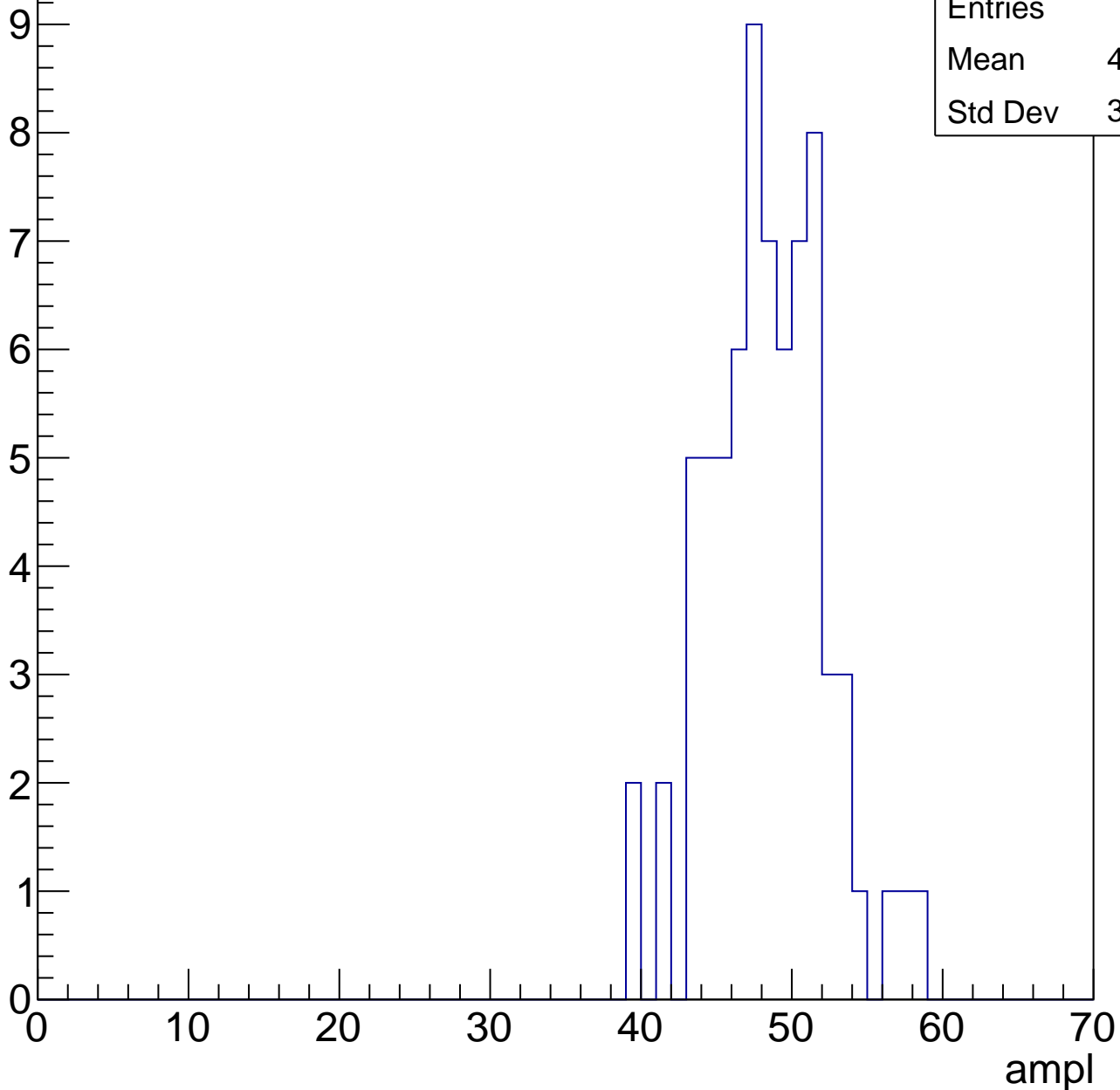
**Gaus Width: 3.7543**



# B1L102S, U20-ch88, adc3

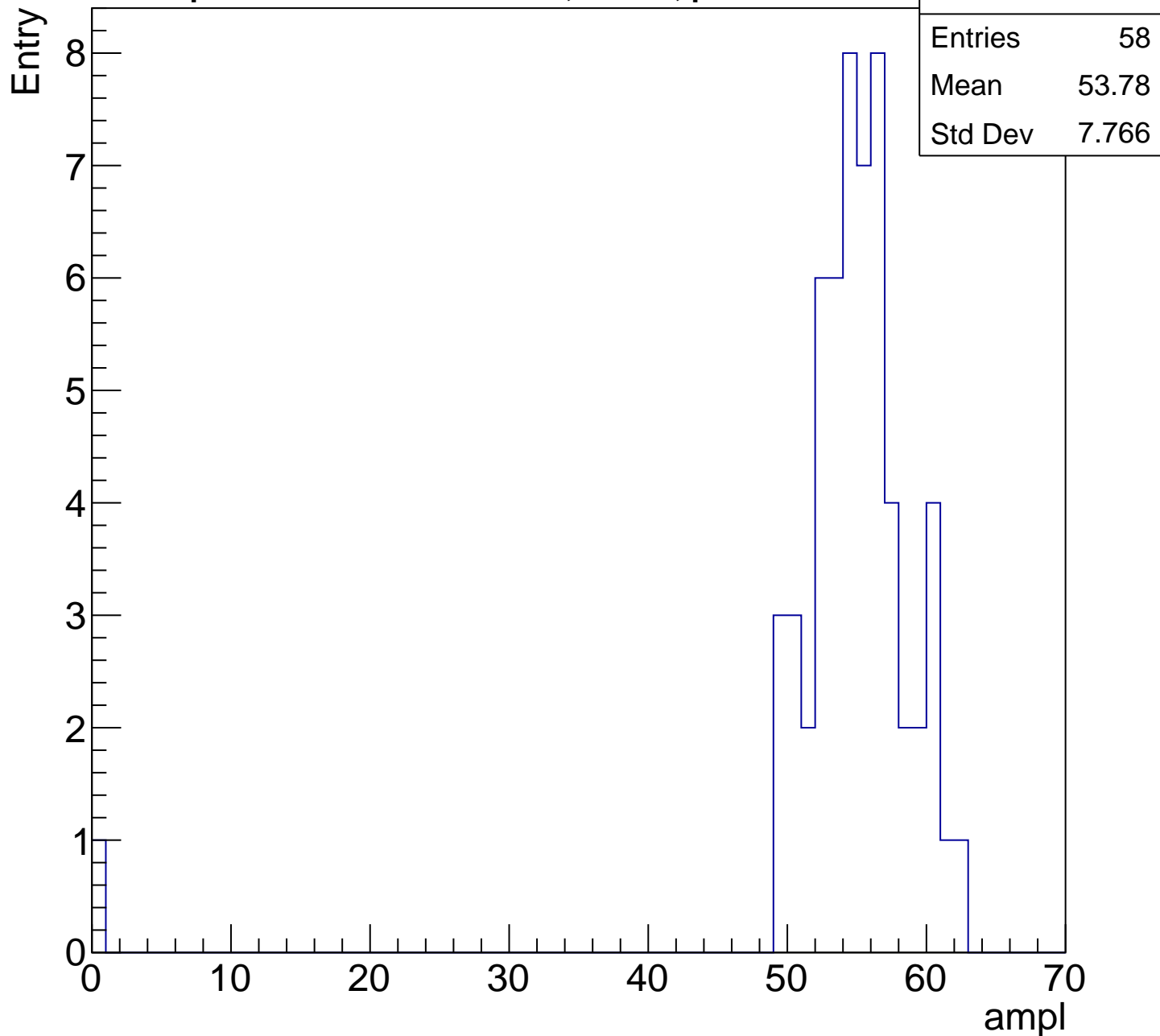
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch88, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2



# B1L102S, U20-ch88, adc5

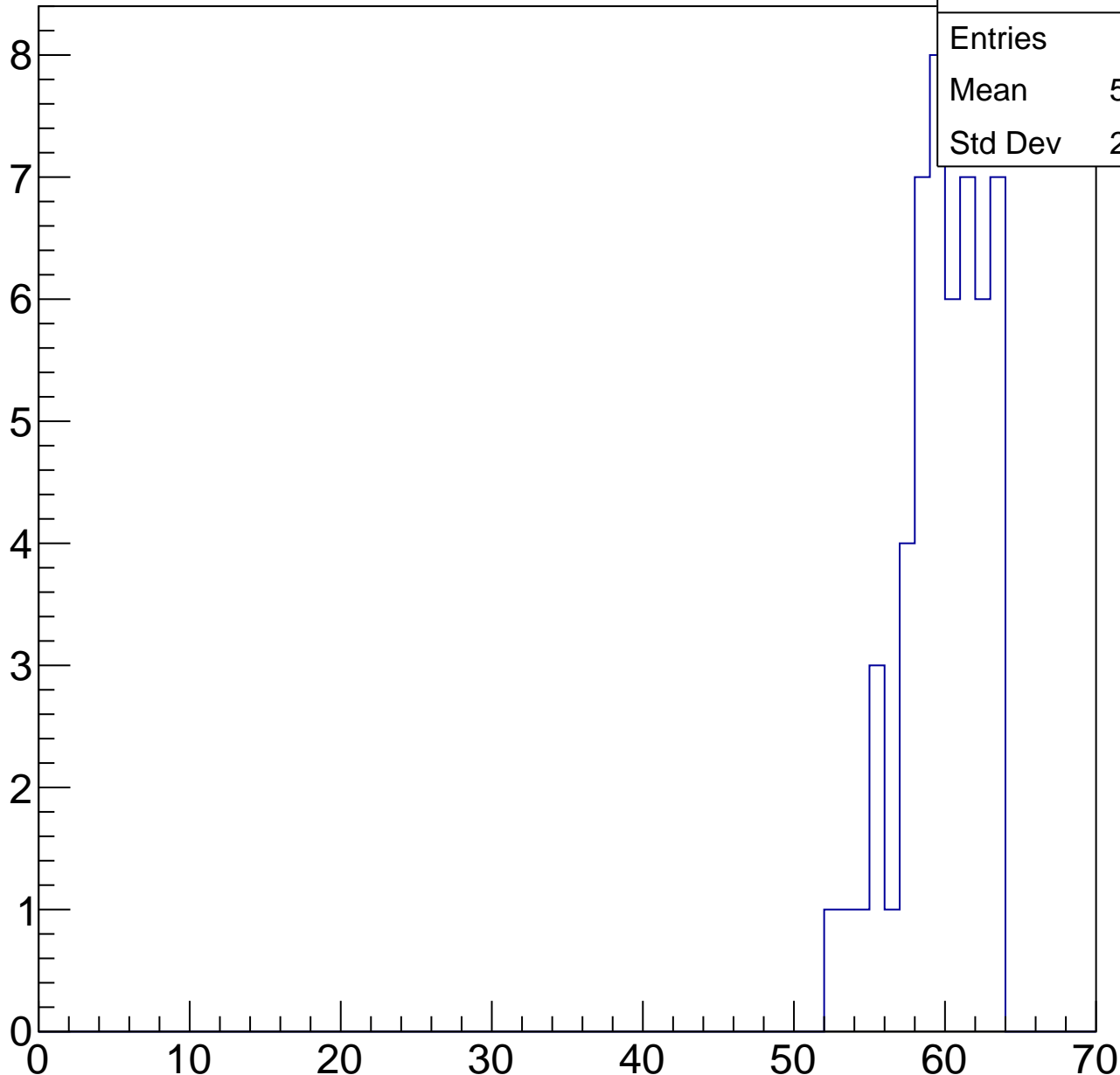
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	52
Mean	59.35
Std Dev	2.717

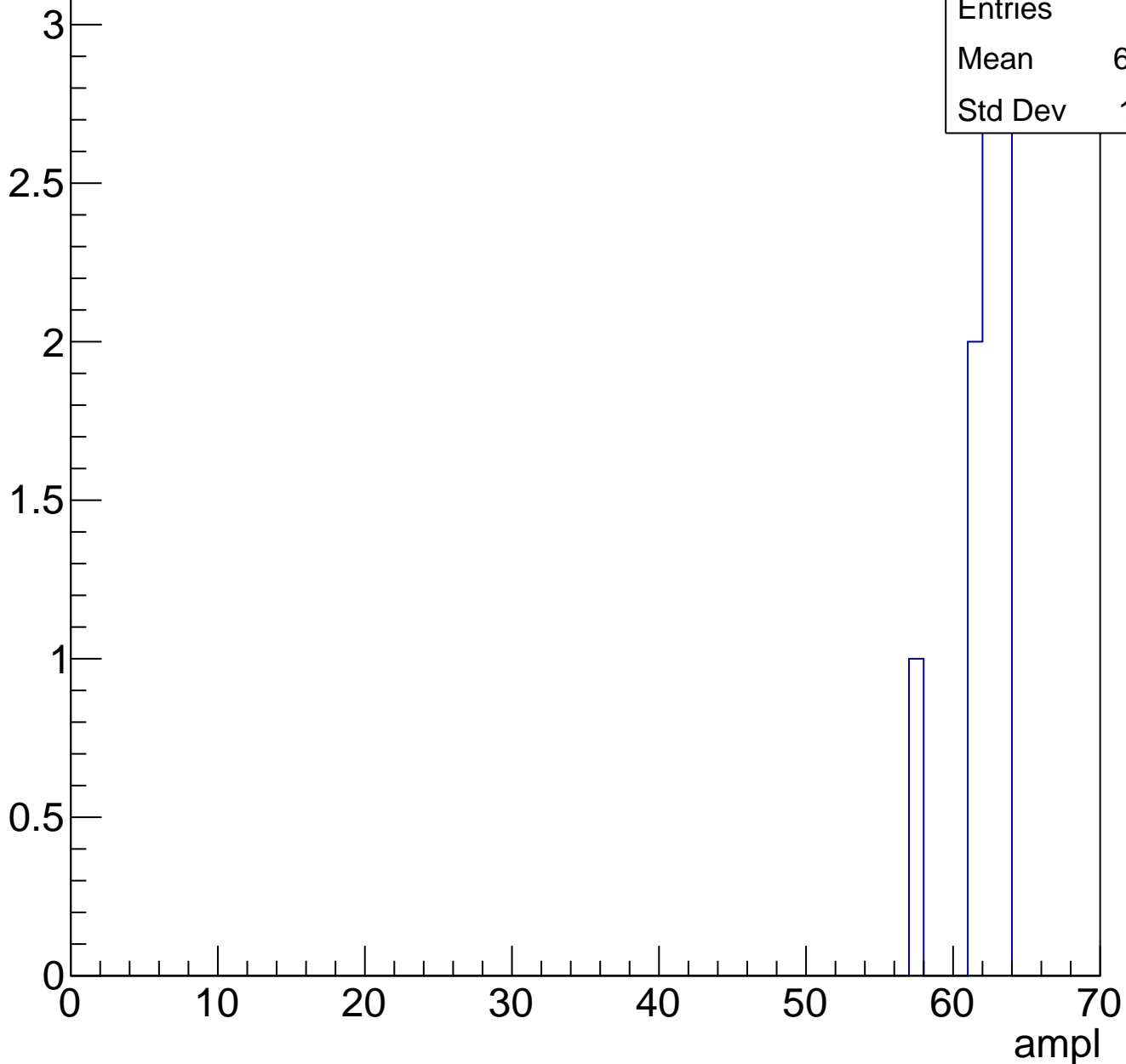
ampl



# B1L102S, U20-ch88, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U20-ch88, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U20-ch89, adc0

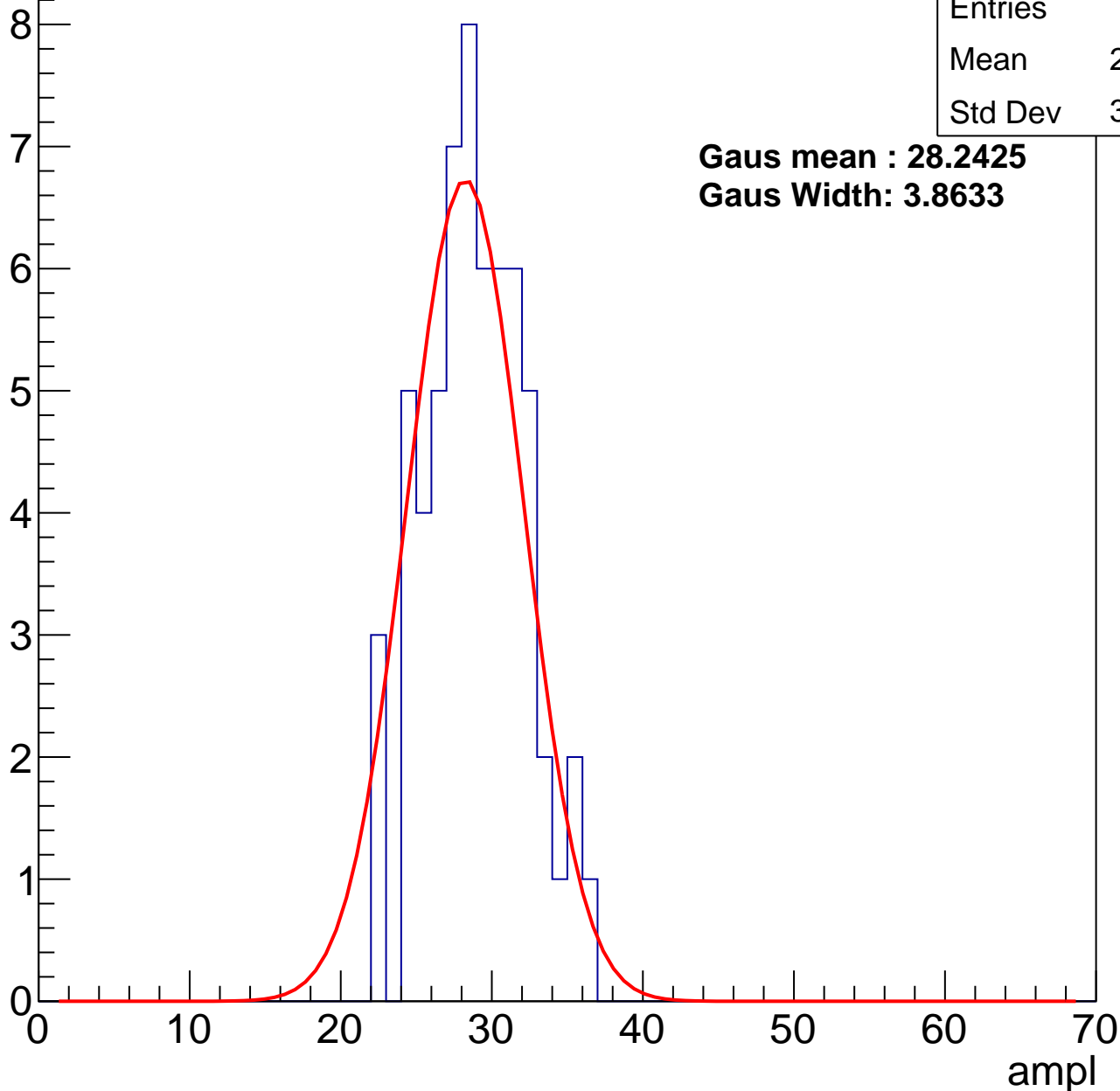
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	28.44
Std Dev	3.267

**Gaus mean : 28.2425**

**Gaus Width: 3.8633**



# B1L102S, U20-ch89, adc1

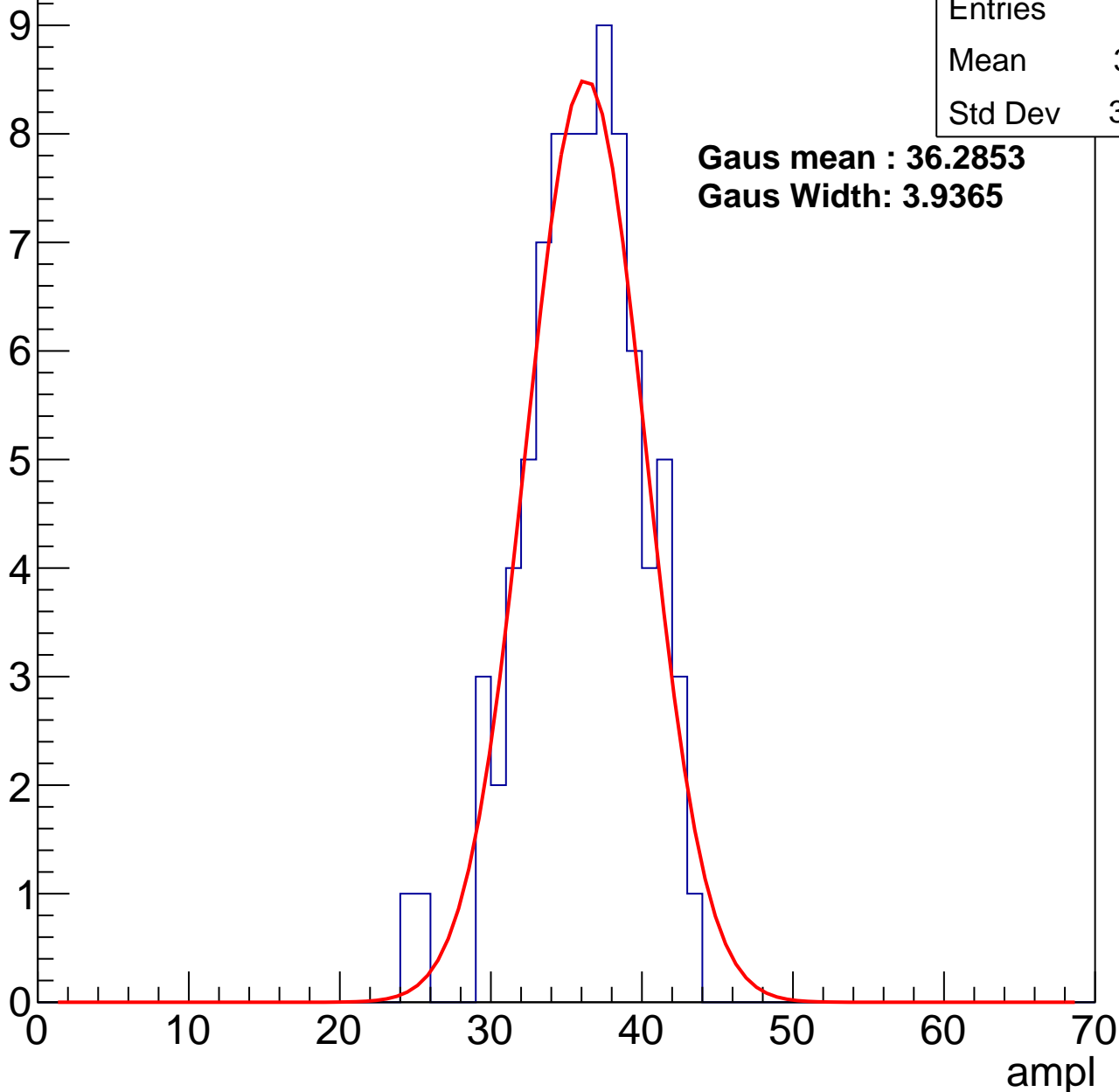
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	83
Mean	35.61
Std Dev	3.795

**Gaus mean : 36.2853**

**Gaus Width: 3.9365**



# B1L102S, U20-ch89, adc2

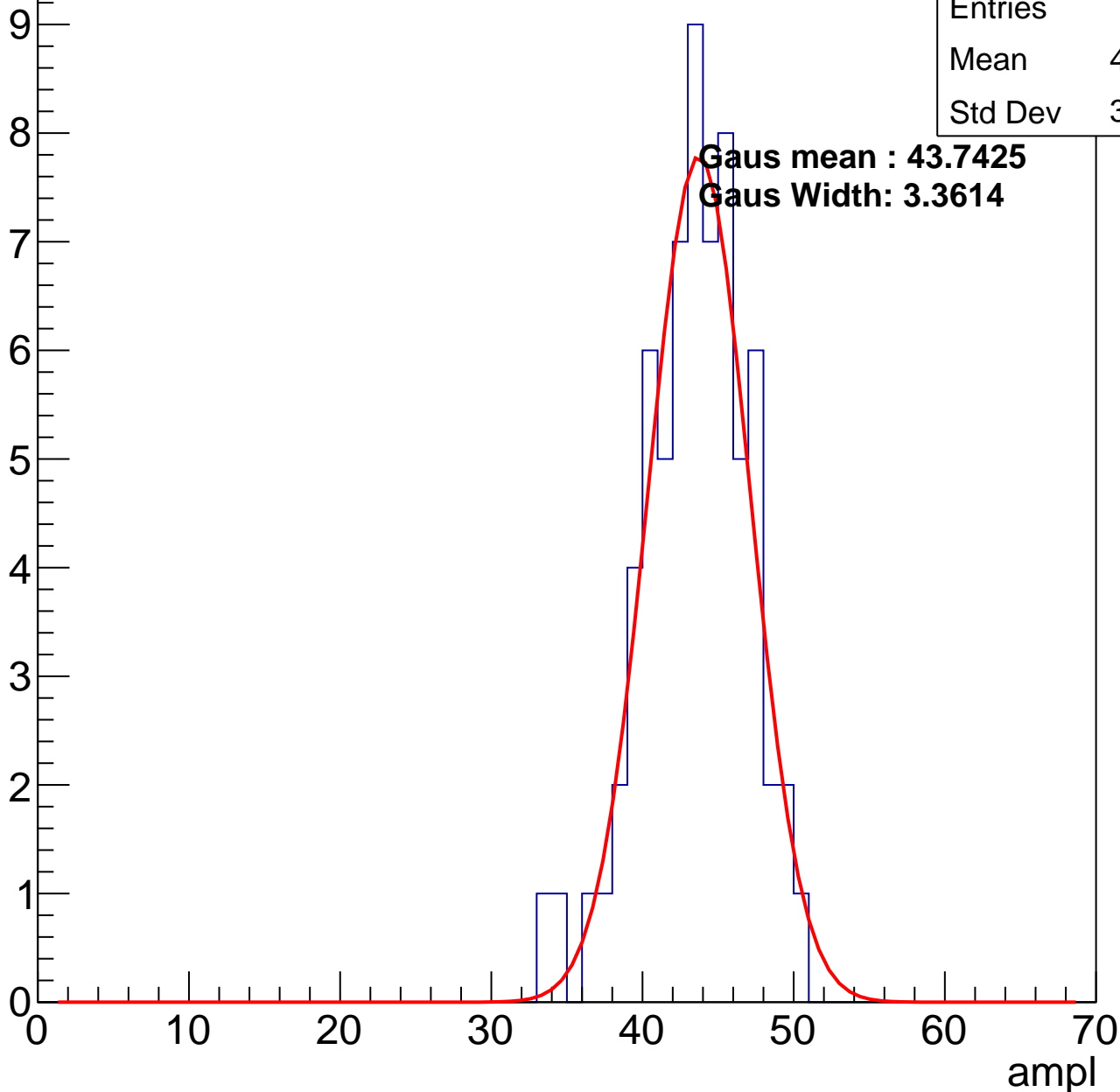
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	42.97
Std Dev	3.455

**Gaus mean : 43.7425**

**Gaus Width: 3.3614**

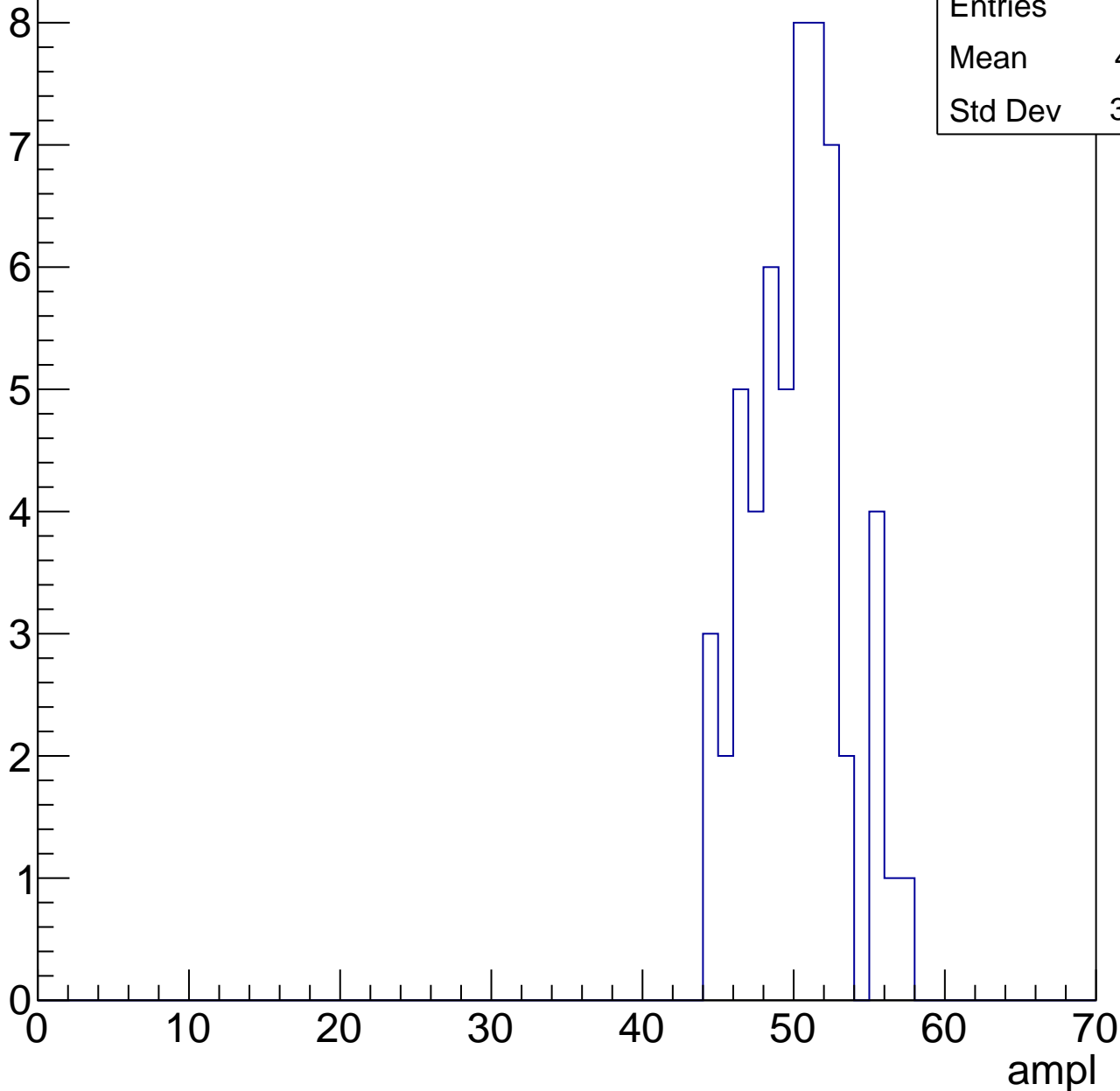


# B1L102S, U20-ch89, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	49.71
Std Dev	3.098

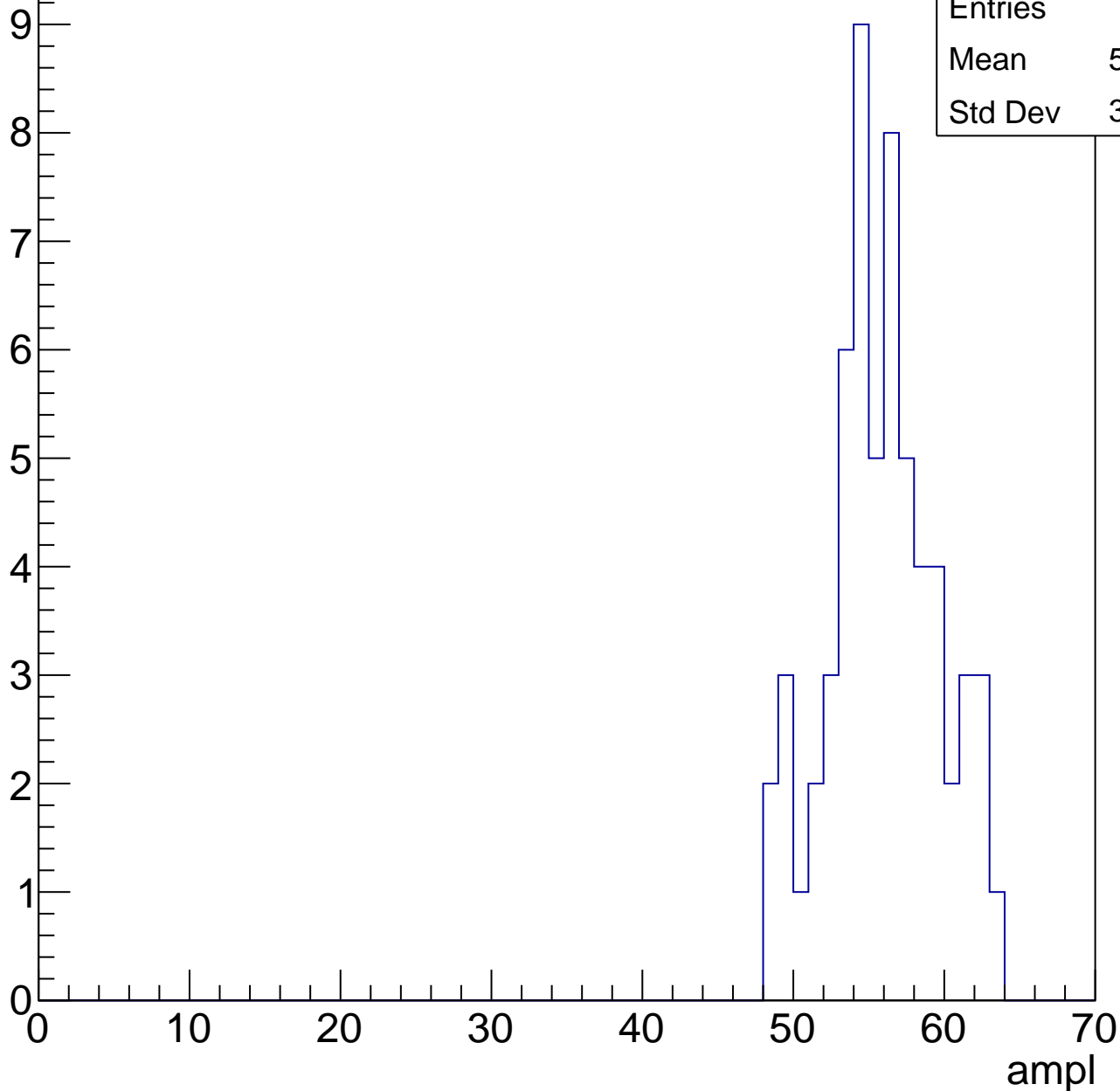


# B1L102S, U20-ch89, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	55.46
Std Dev	3.638

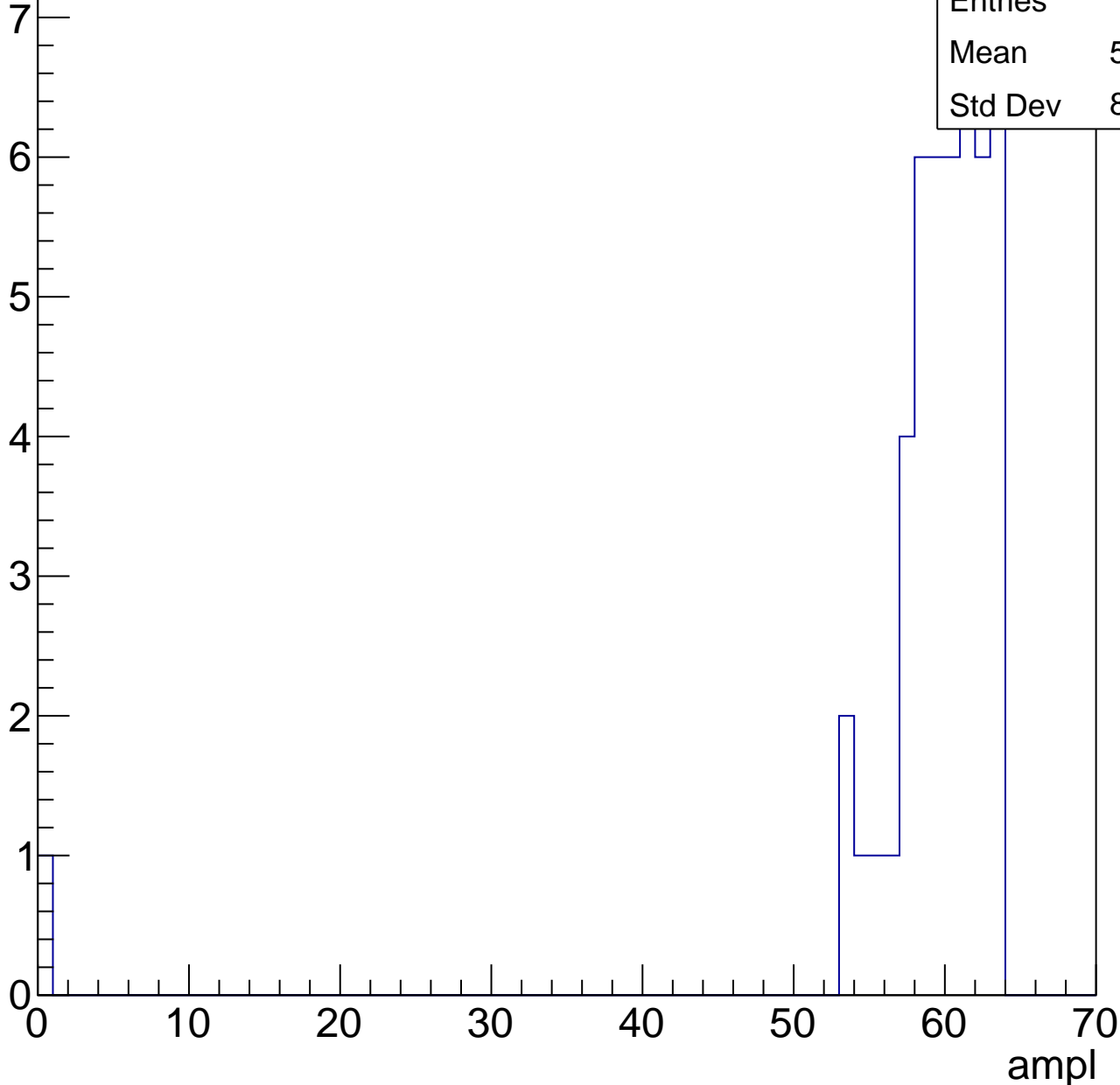


# B1L102S, U20-ch89, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	48
Mean	58.35
Std Dev	8.903



# B1L102S, U20-ch89, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

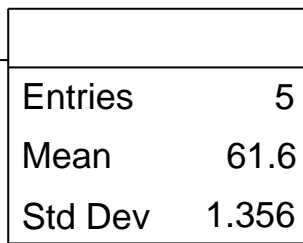
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	61.6
Std Dev	1.356

0 10 20 30 40 50 60 70

ampl





# B1L102S, U20-ch89, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch90, adc0

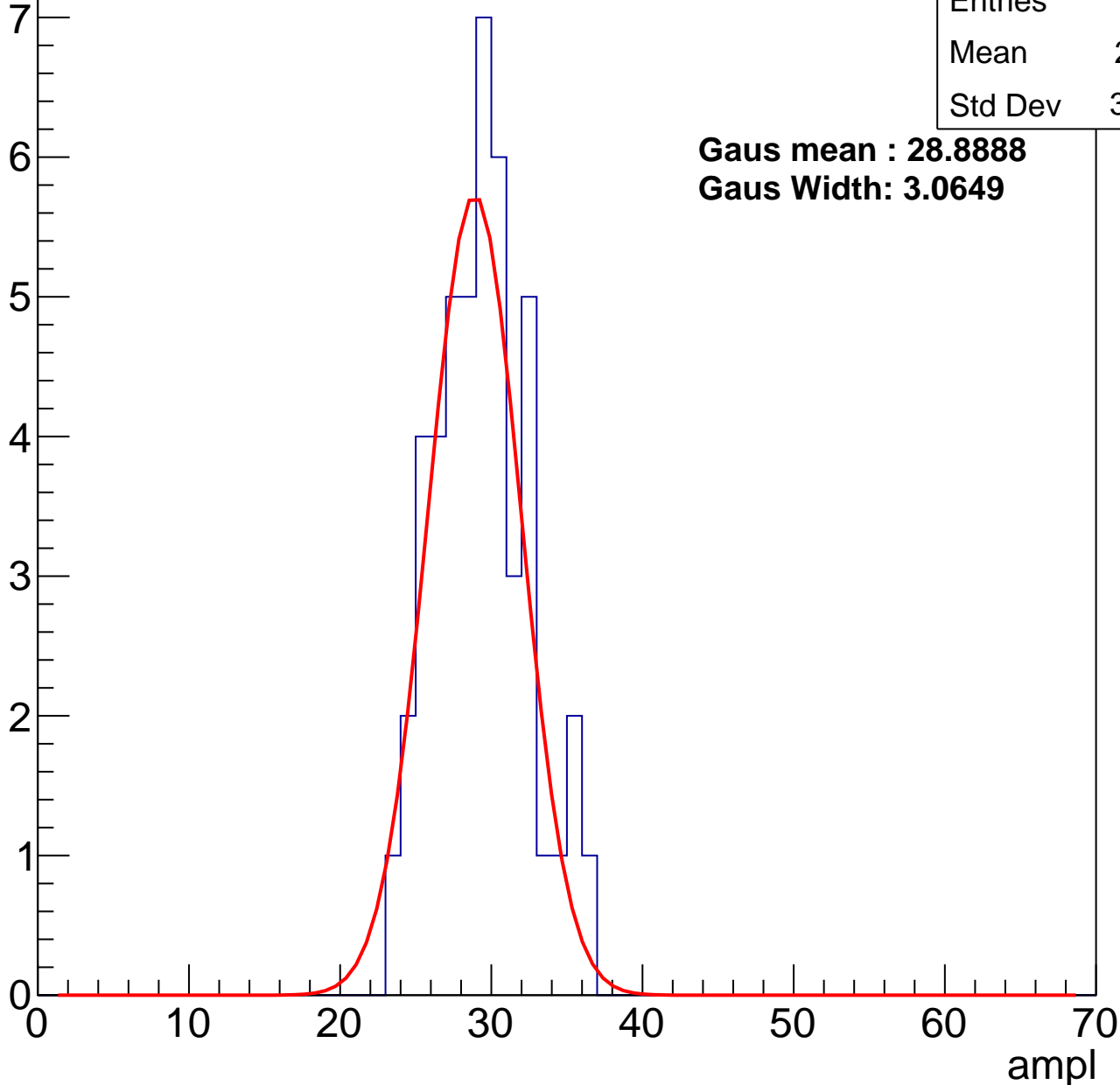
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	47
Mean	28.91
Std Dev	3.045

**Gaus mean : 28.8888**

**Gaus Width: 3.0649**



# B1L102S, U20-ch90, adc1

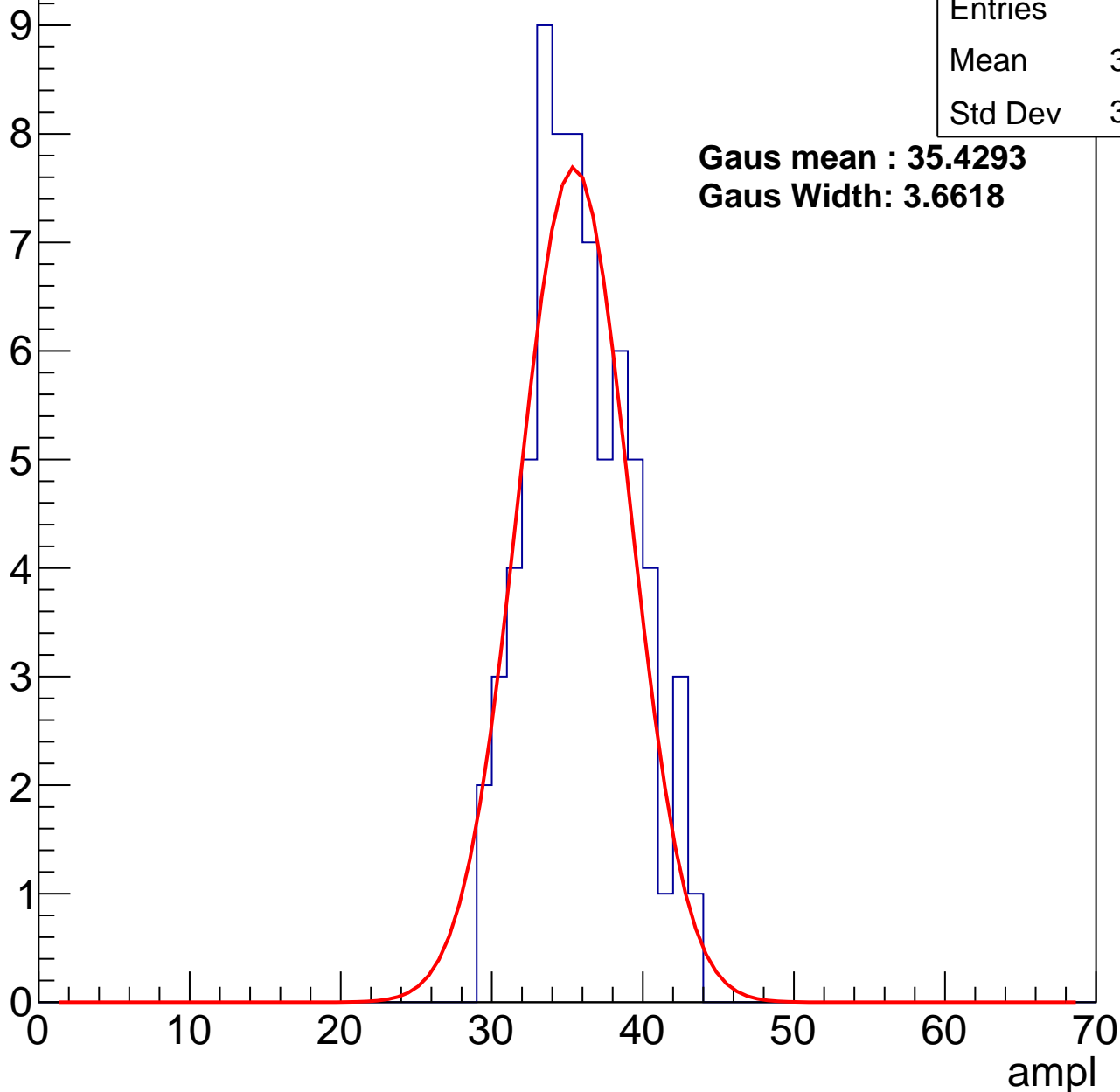
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	35.37
Std Dev	3.354

**Gaus mean : 35.4293**

**Gaus Width: 3.6618**



# B1L102S, U20-ch90, adc2

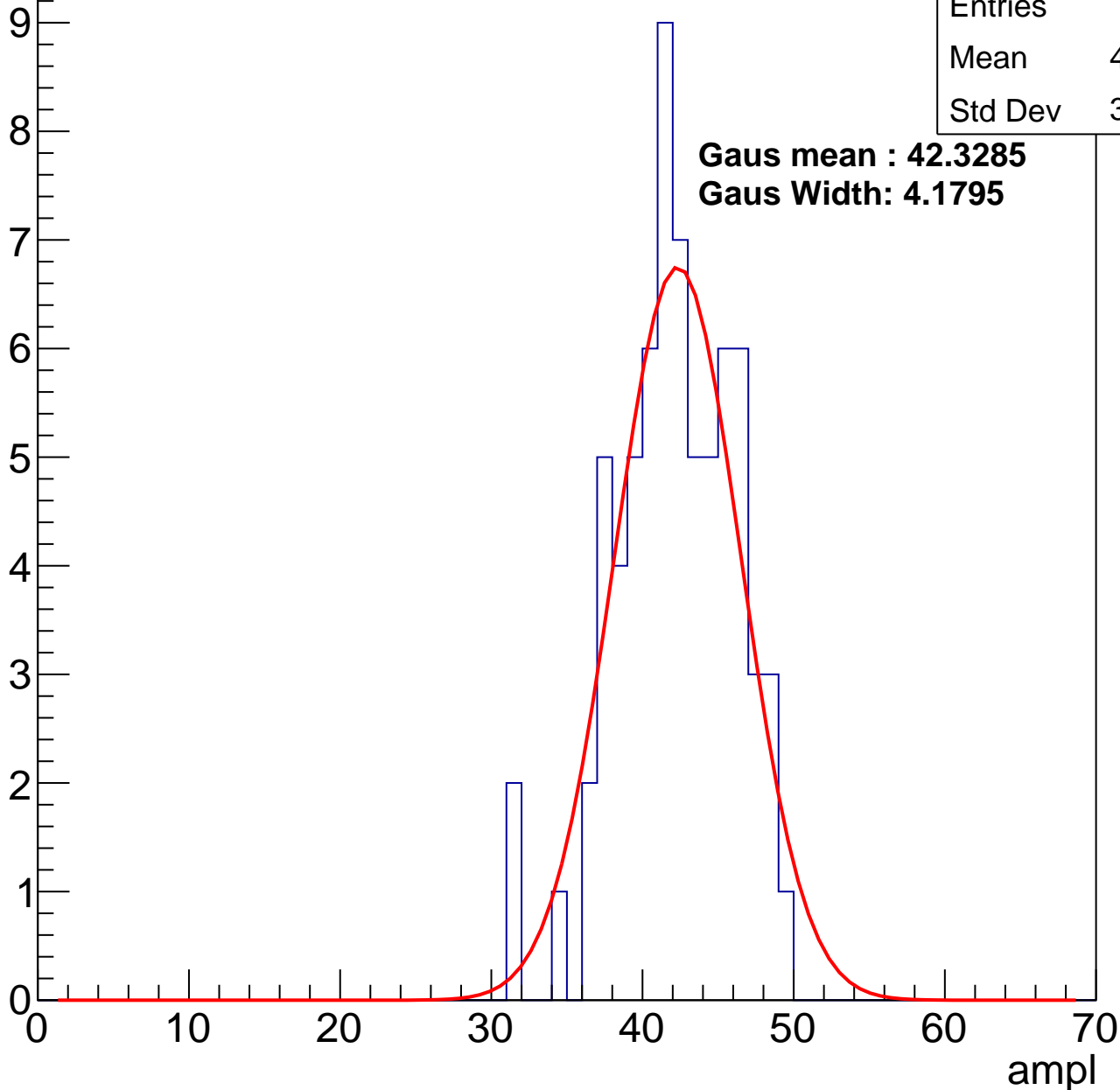
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	41.69
Std Dev	3.864

**Gaus mean : 42.3285**

**Gaus Width: 4.1795**

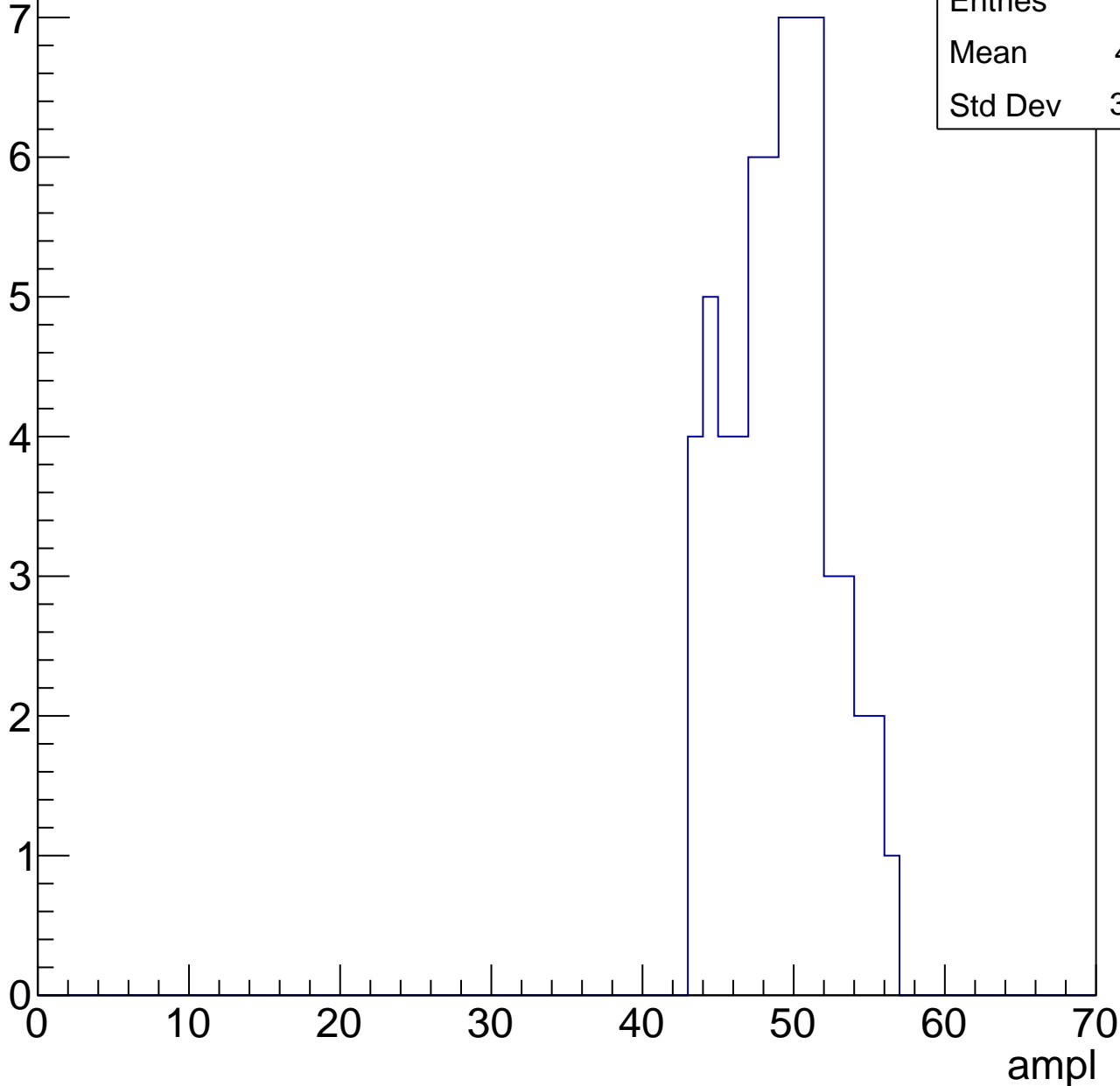


# B1L102S, U20-ch90, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	48.61
Std Dev	3.316

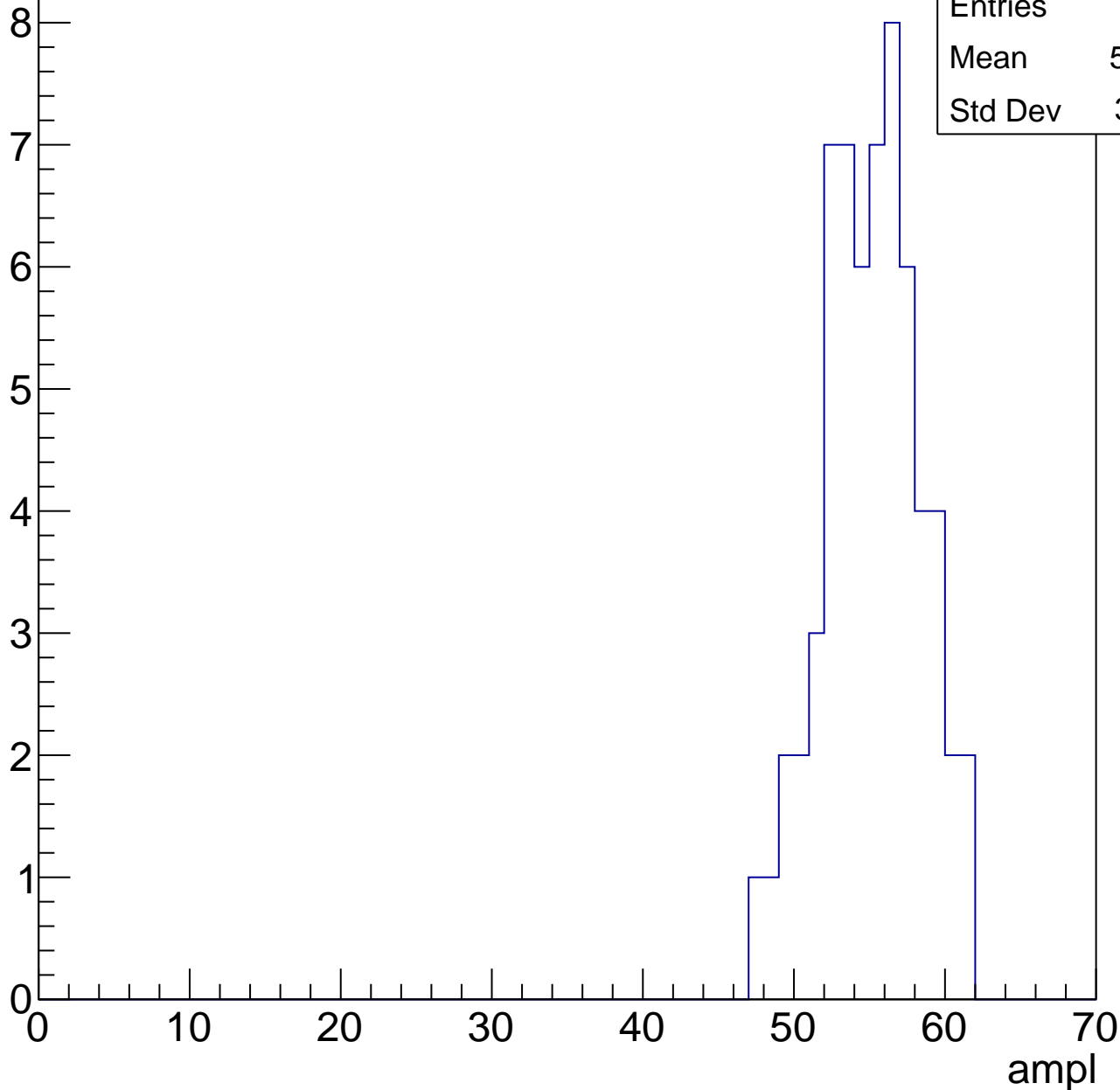


# B1L102S, U20-ch90, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	54.68
Std Dev	3.181

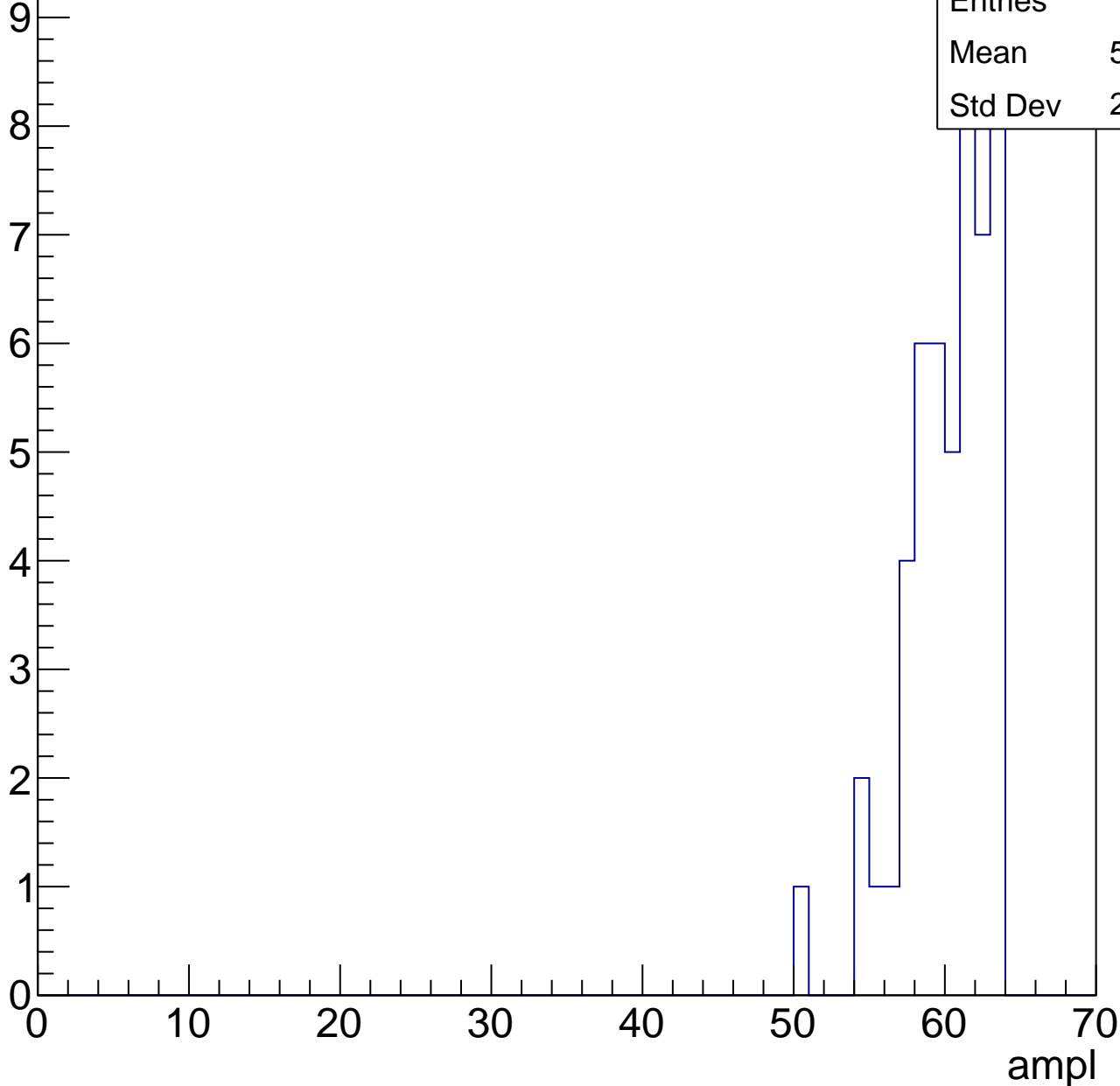


# B1L102S, U20-ch90, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

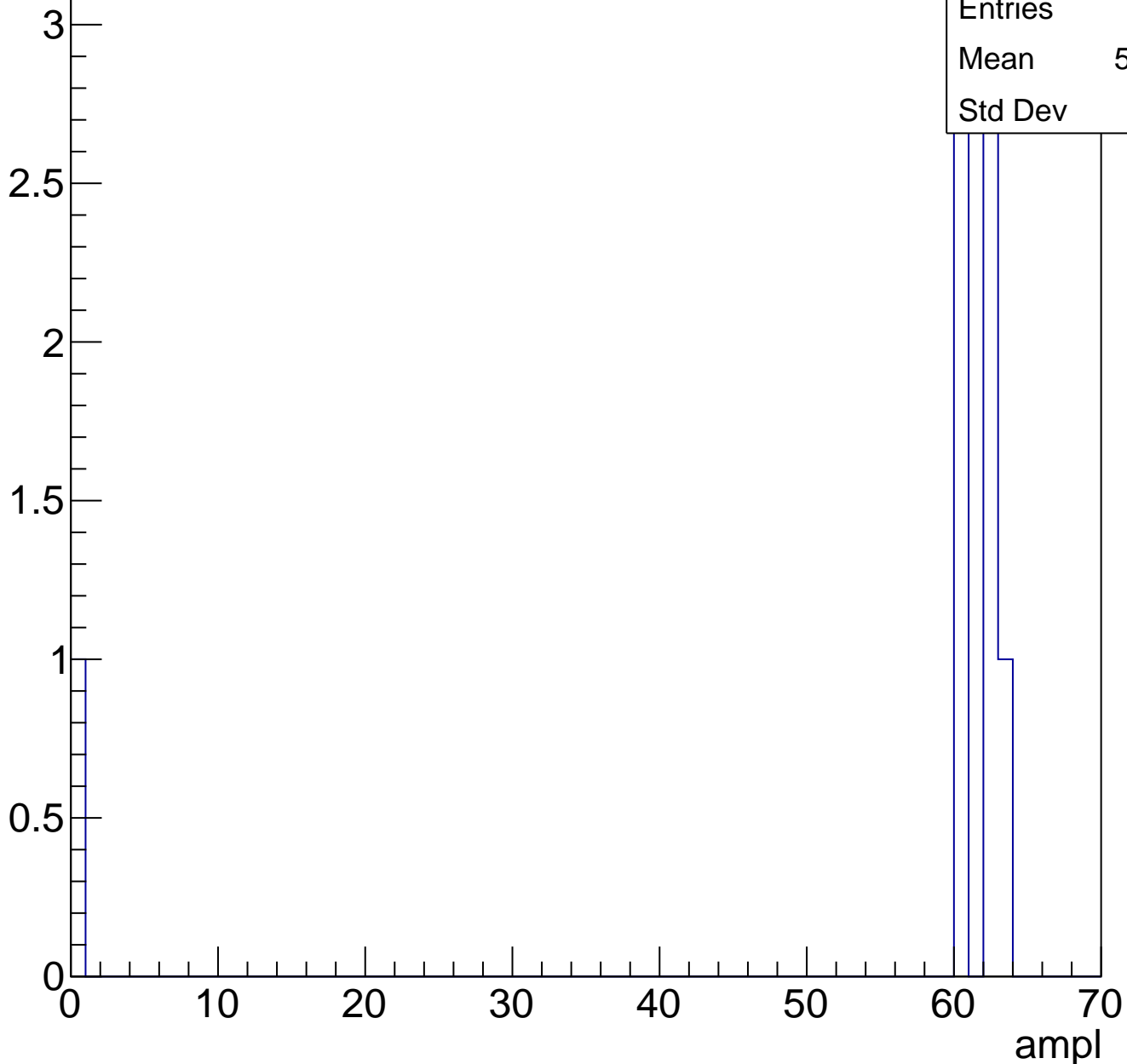
Entries	50
Mean	59.76
Std Dev	2.804



# B1L102S, U20-ch90, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U20-ch90, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch91, adc0

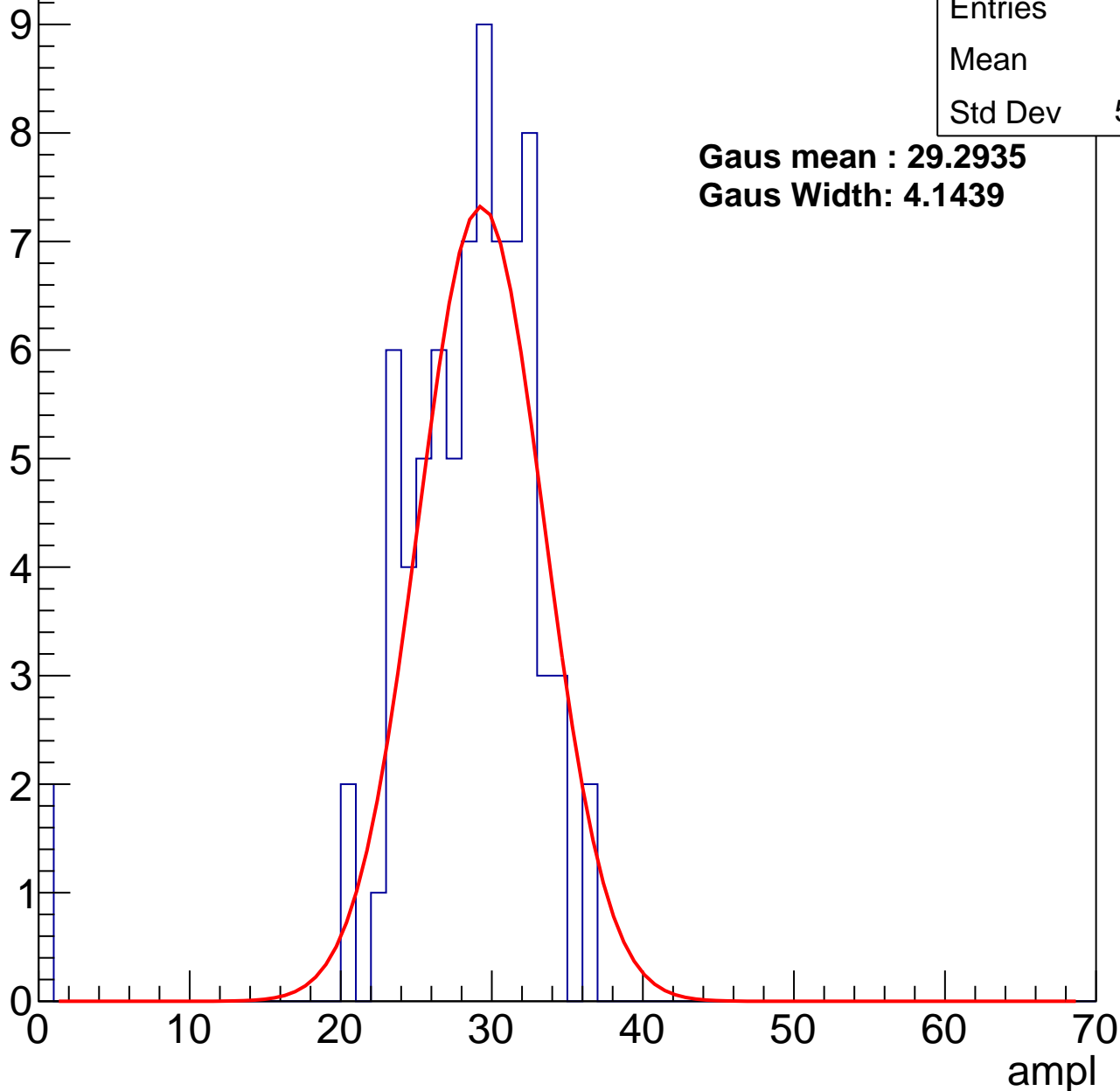
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	27.6
Std Dev	5.751

**Gaus mean : 29.2935**

**Gaus Width: 4.1439**



# B1L102S, U20-ch91, adc1

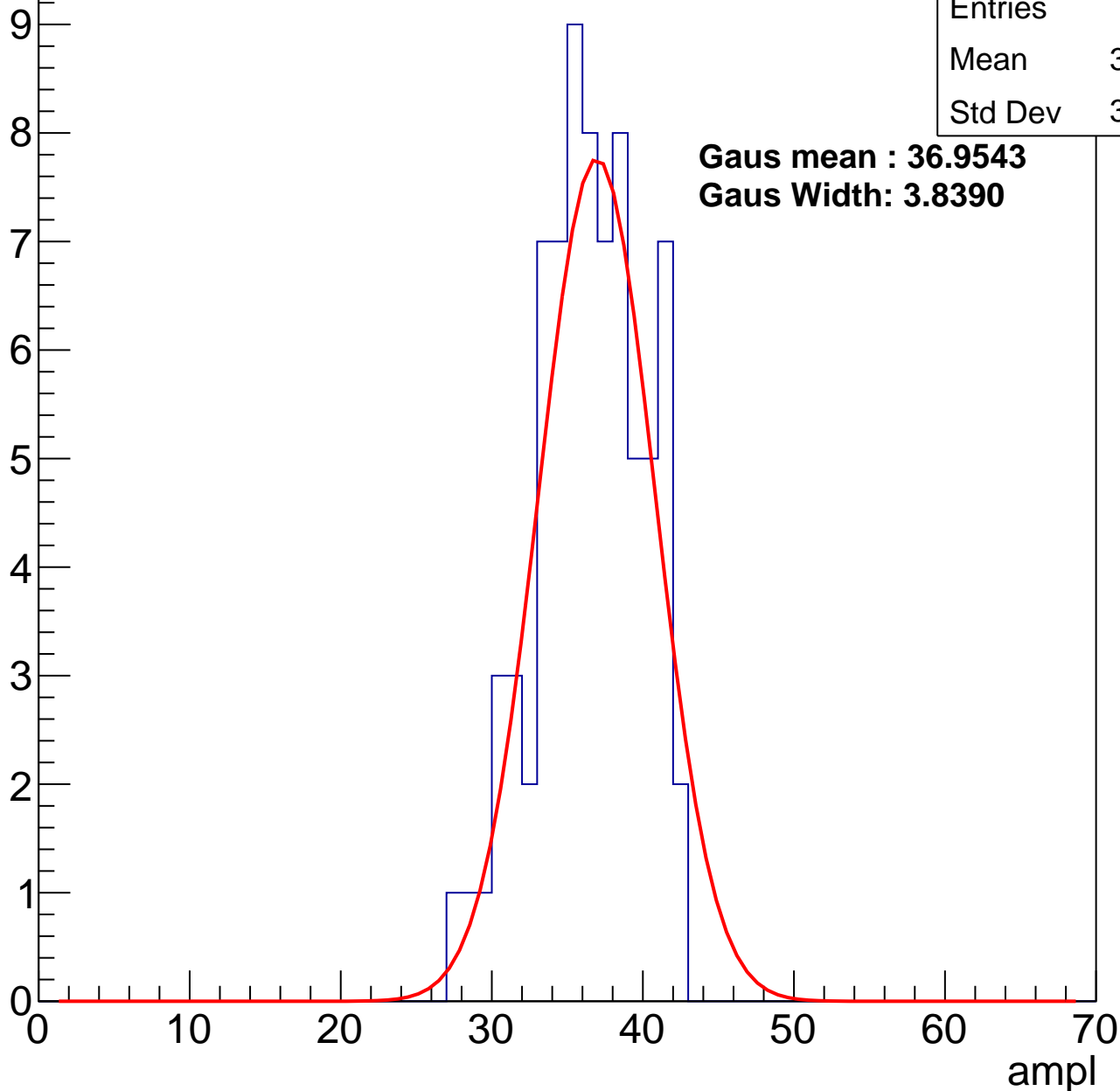
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	35.95
Std Dev	3.479

**Gaus mean : 36.9543**

**Gaus Width: 3.8390**



# B1L102S, U20-ch91, adc2

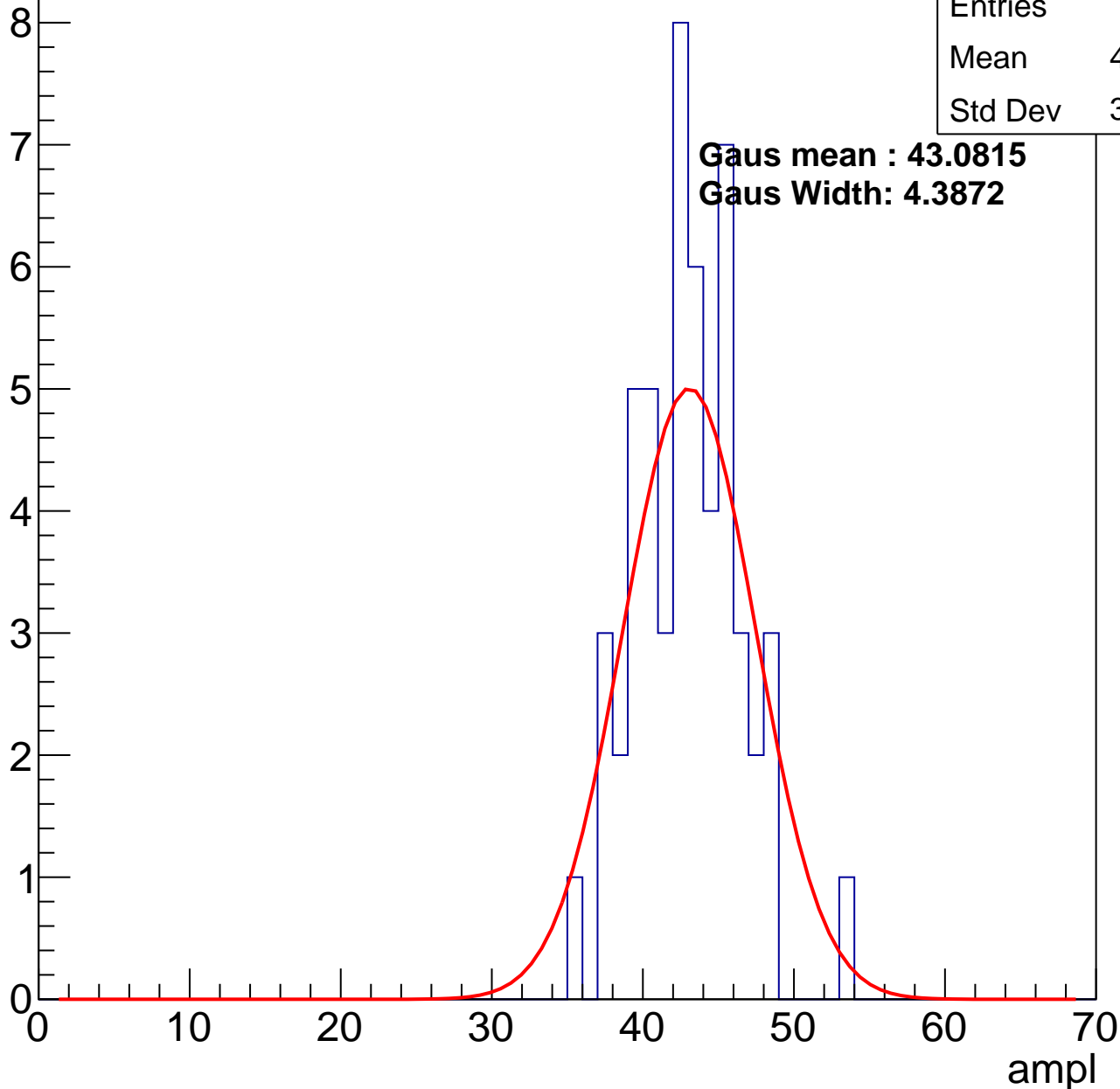
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	42.53
Std Dev	3.424

**Gaus mean : 43.0815**

**Gaus Width: 4.3872**



# B1L102S, U20-ch91, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	74
Mean	48.95
Std Dev	3.59

Entry

10

8

6

4

2

0

0

10

20

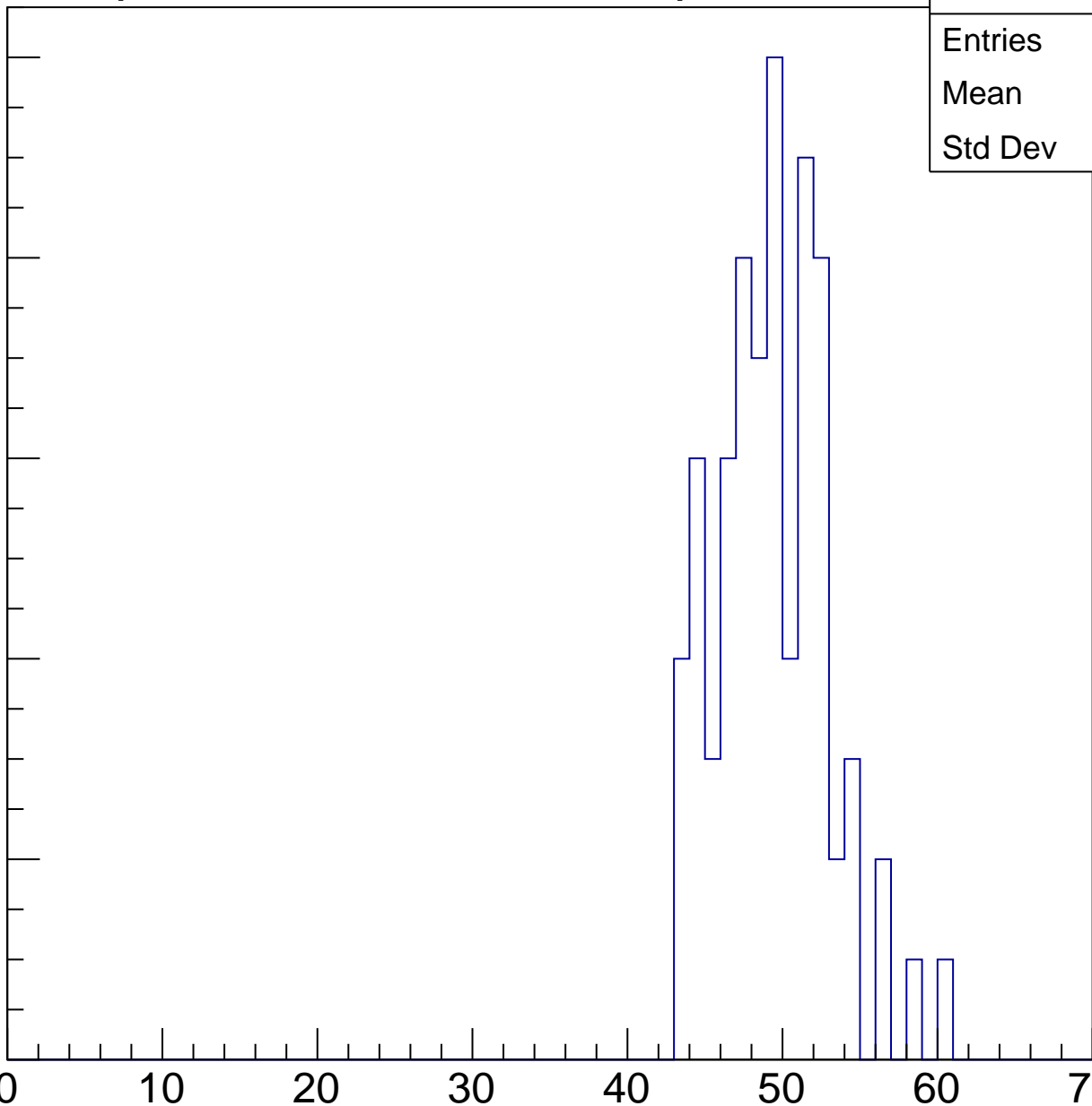
30

40

50

60

ampl

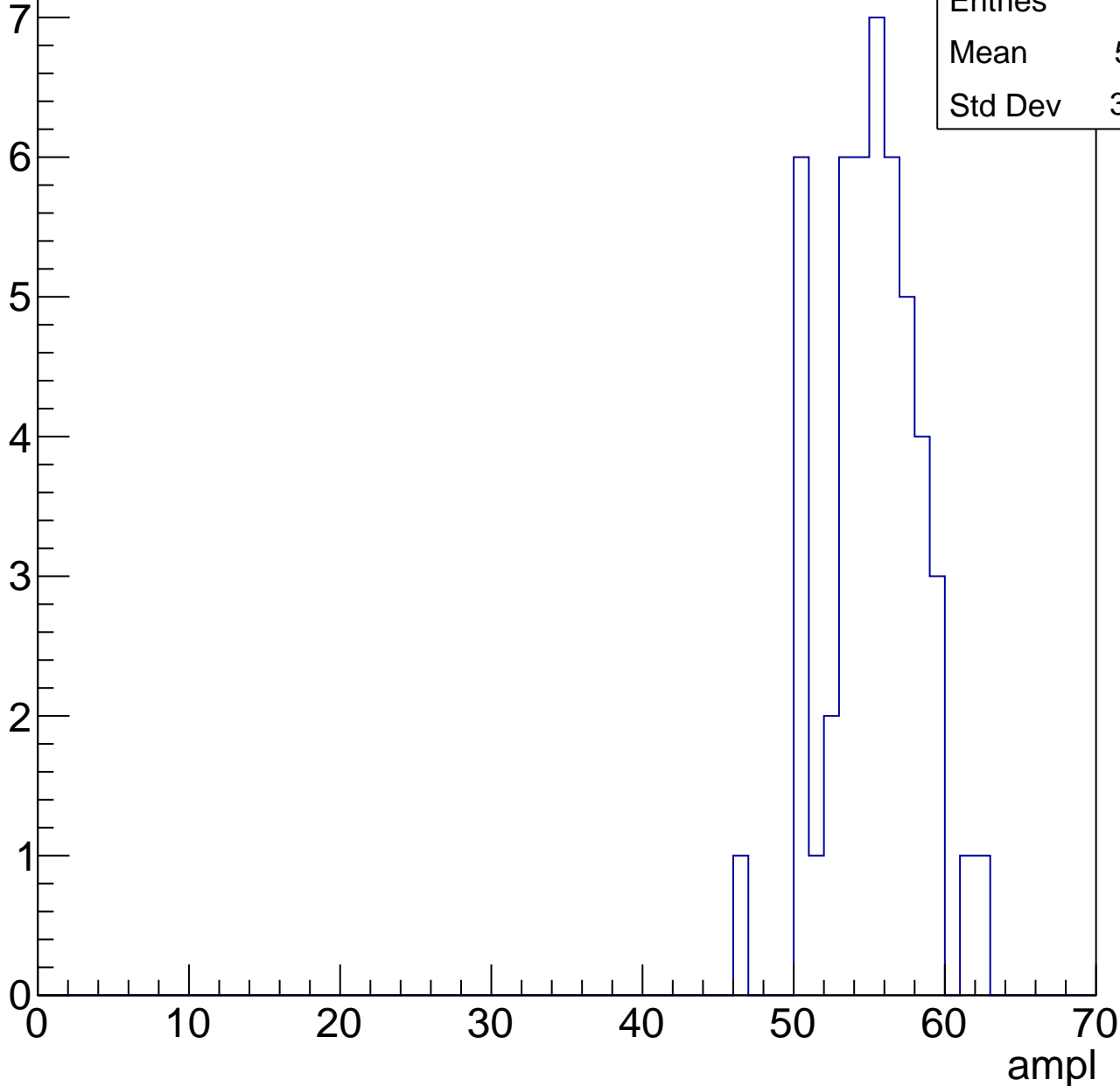


# B1L102S, U20-ch91, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

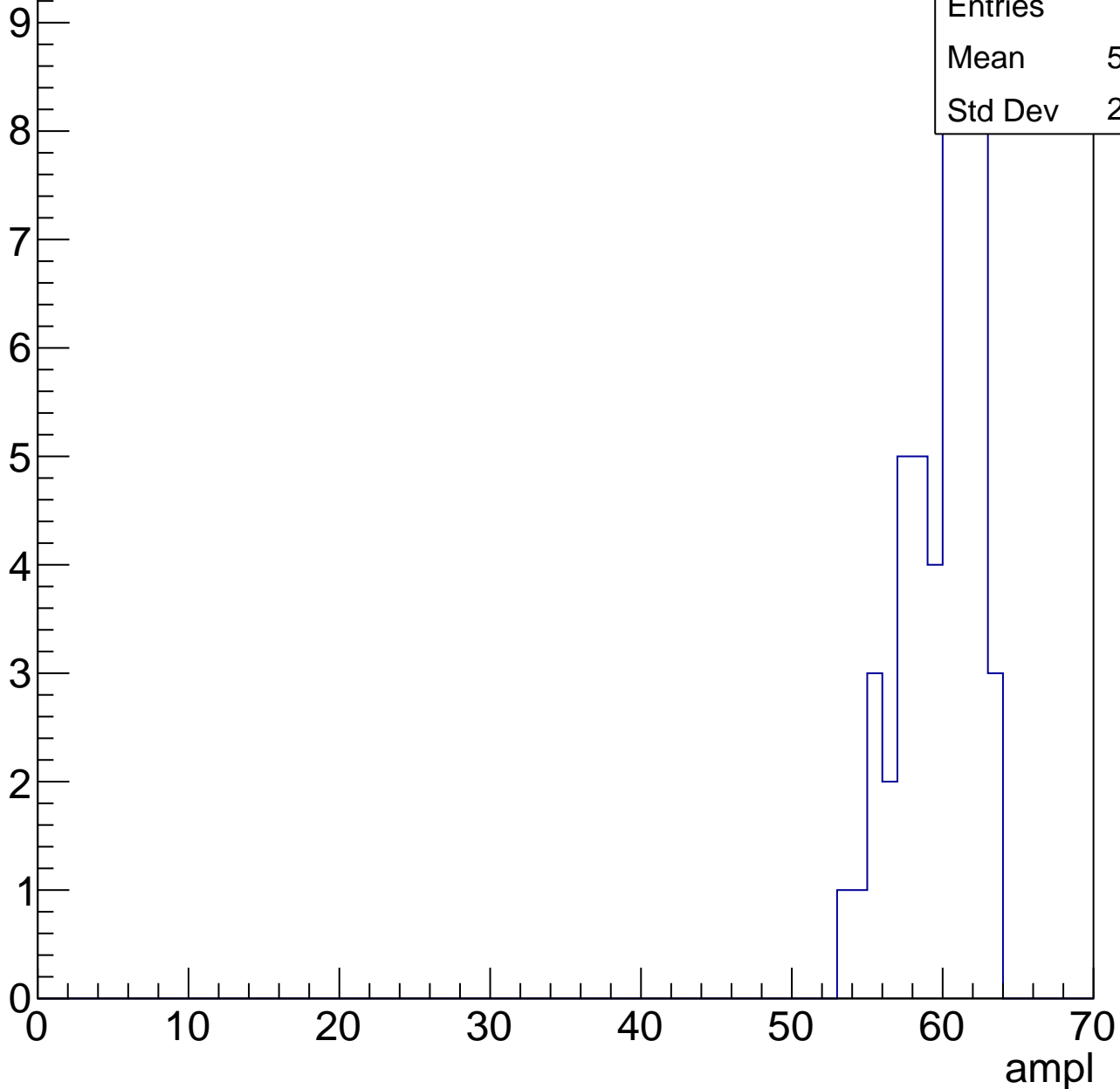
Entries	49
Mean	54.71
Std Dev	3.149



# B1L102S, U20-ch91, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



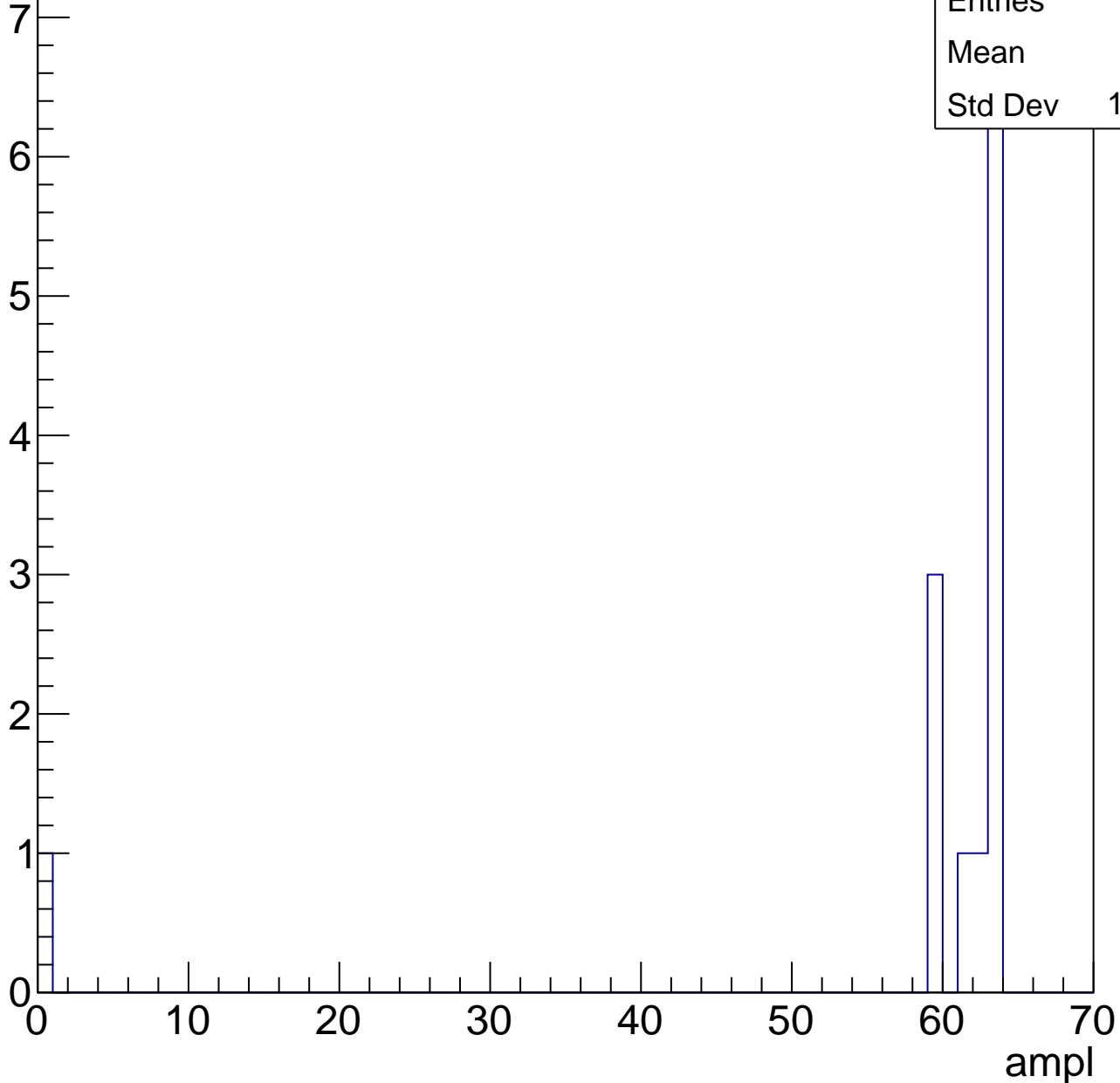
Entries	49
Mean	59.35
Std Dev	2.503

# B1L102S, U20-ch91, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	13
Mean	57
Std Dev	16.53





# B1L102S, U20-ch91, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	10
Std Dev	10

# B1L102S, U20-ch92, adc0

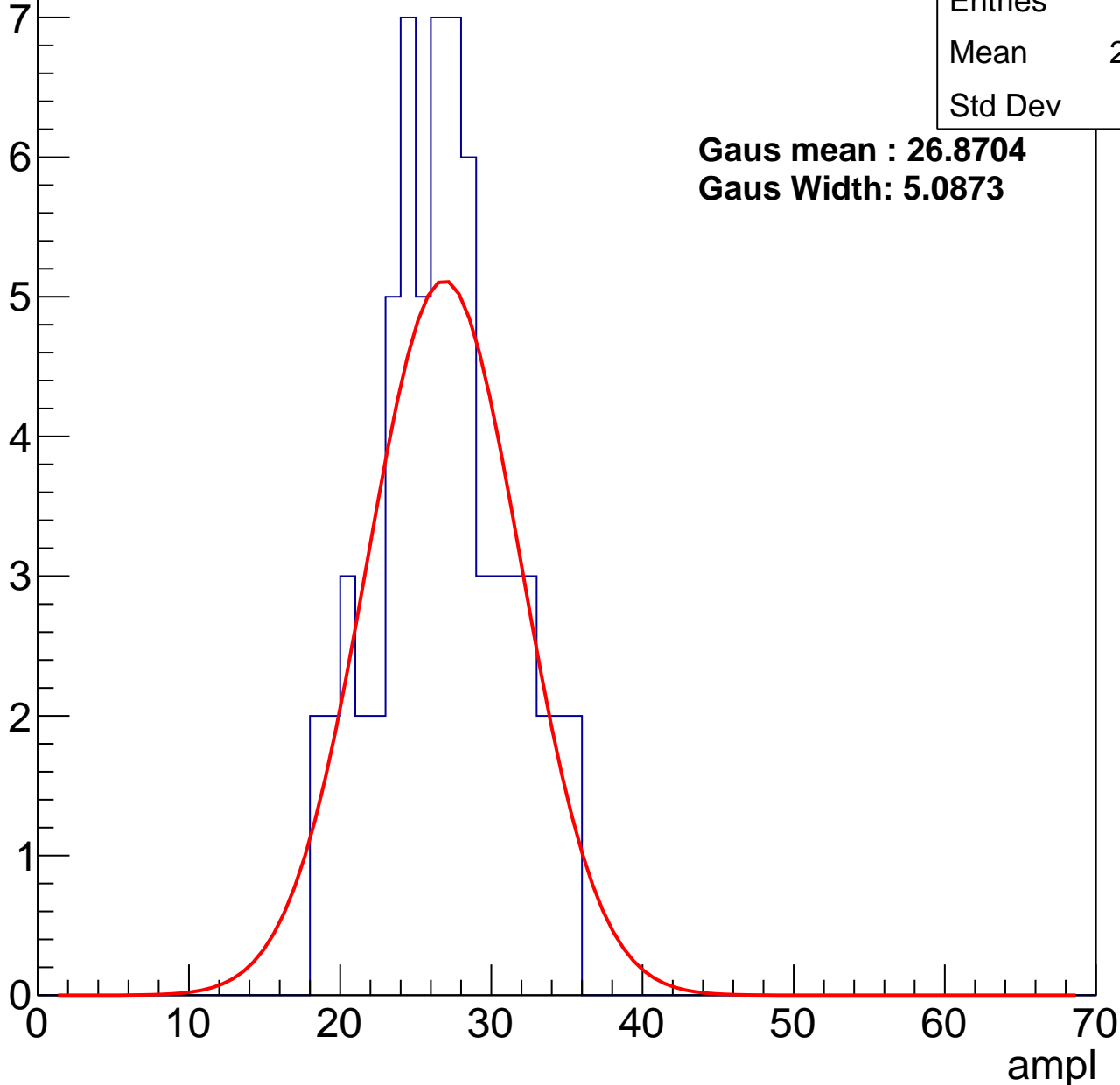
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	26.32
Std Dev	4.2

**Gaus mean : 26.8704**

**Gaus Width: 5.0873**



# B1L102S, U20-ch92, adc1

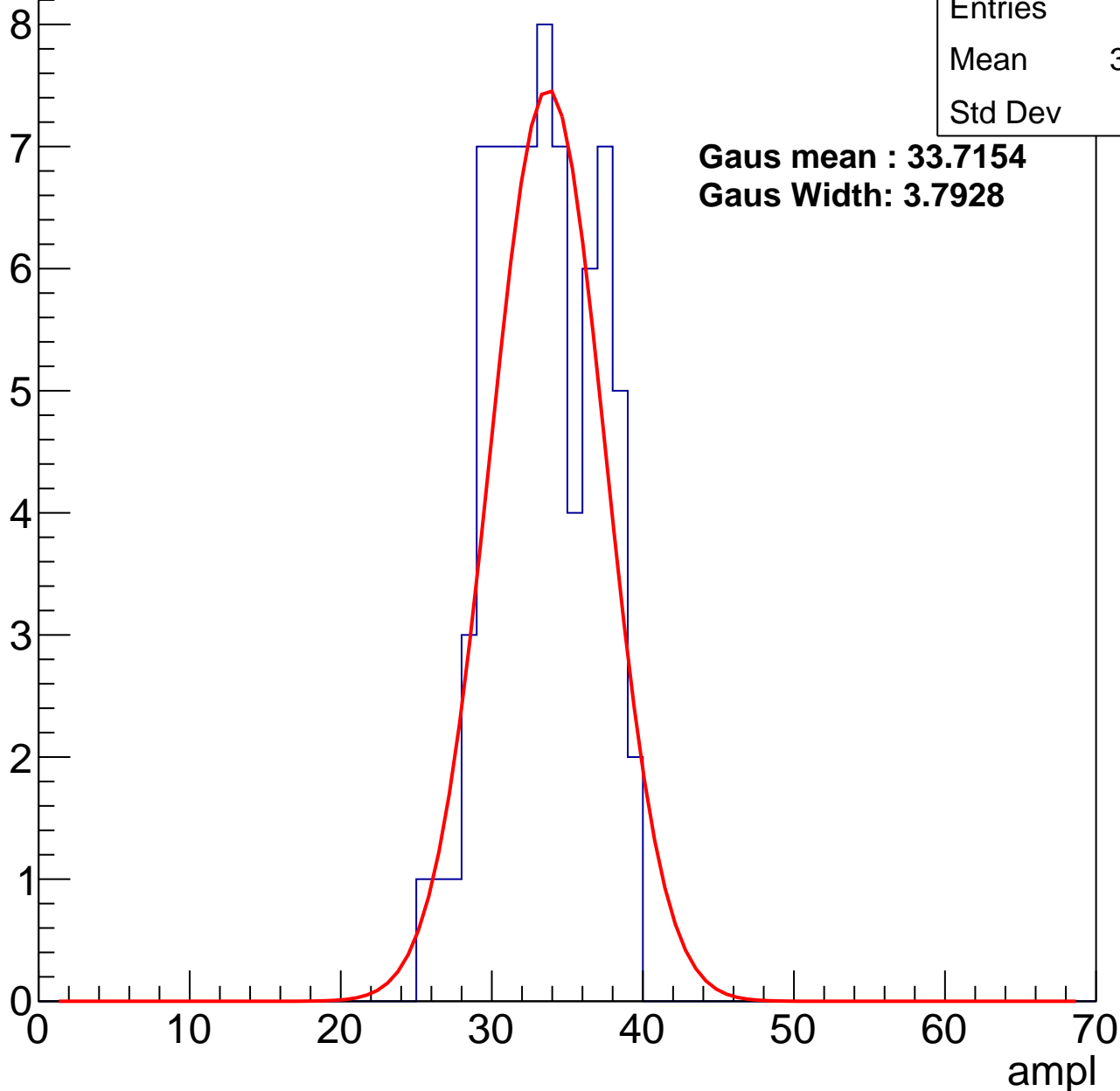
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	32.89
Std Dev	3.35

**Gaus mean : 33.7154**

**Gaus Width: 3.7928**



# B1L102S, U20-ch92, adc2

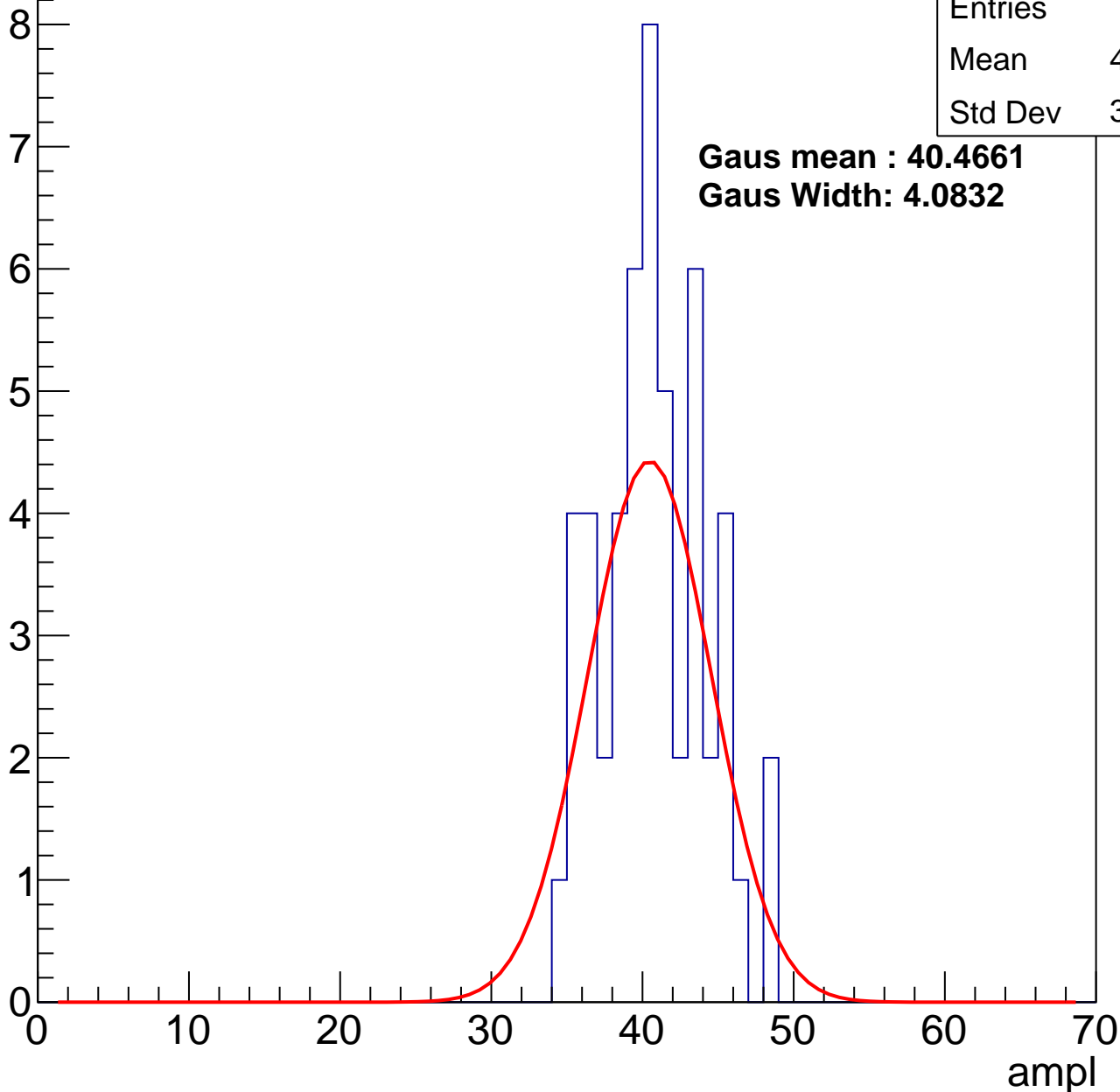
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	40.29
Std Dev	3.426

**Gaus mean : 40.4661**

**Gaus Width: 4.0832**

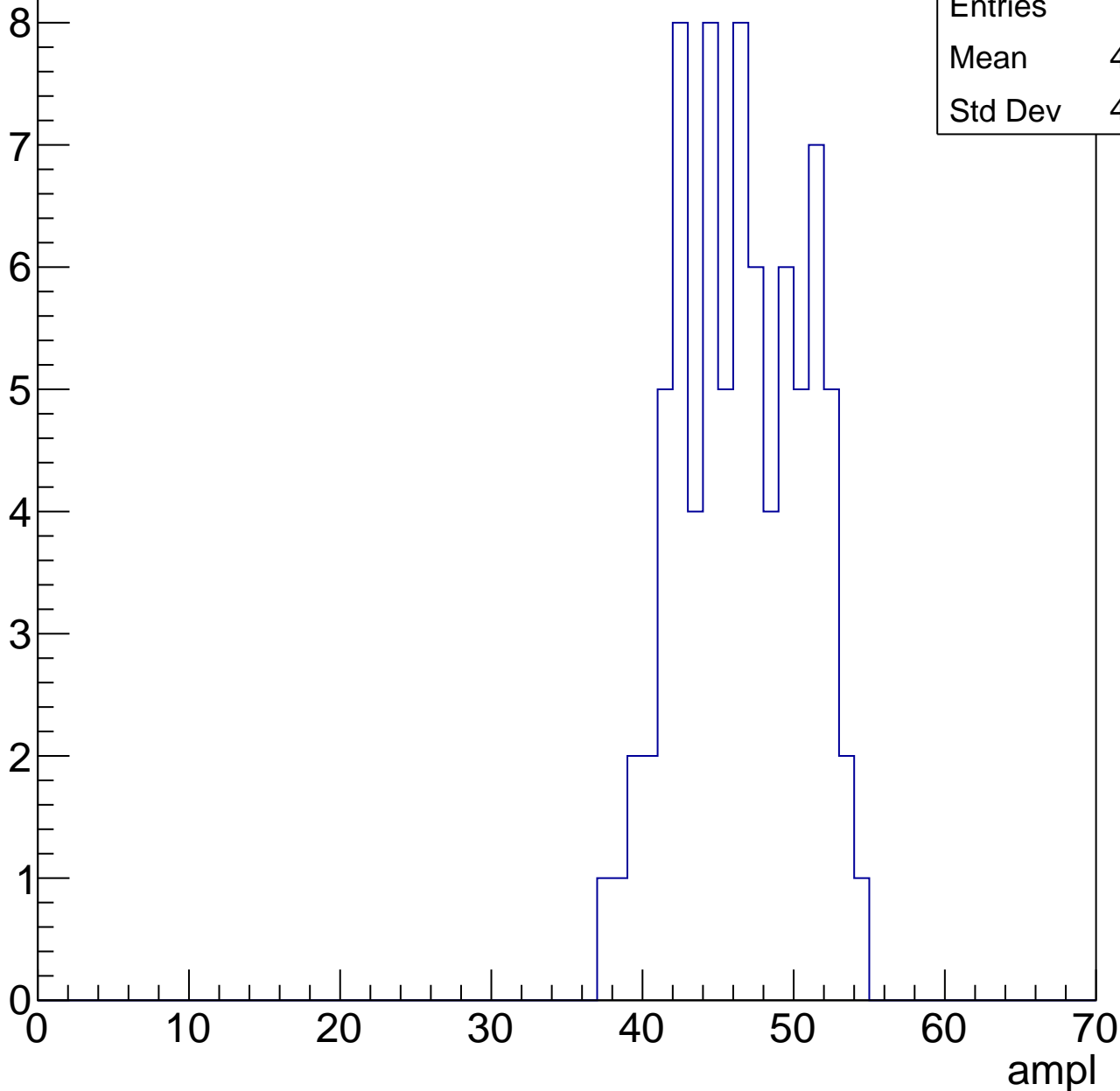


# B1L102S, U20-ch92, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	80
Mean	46.08
Std Dev	4.052

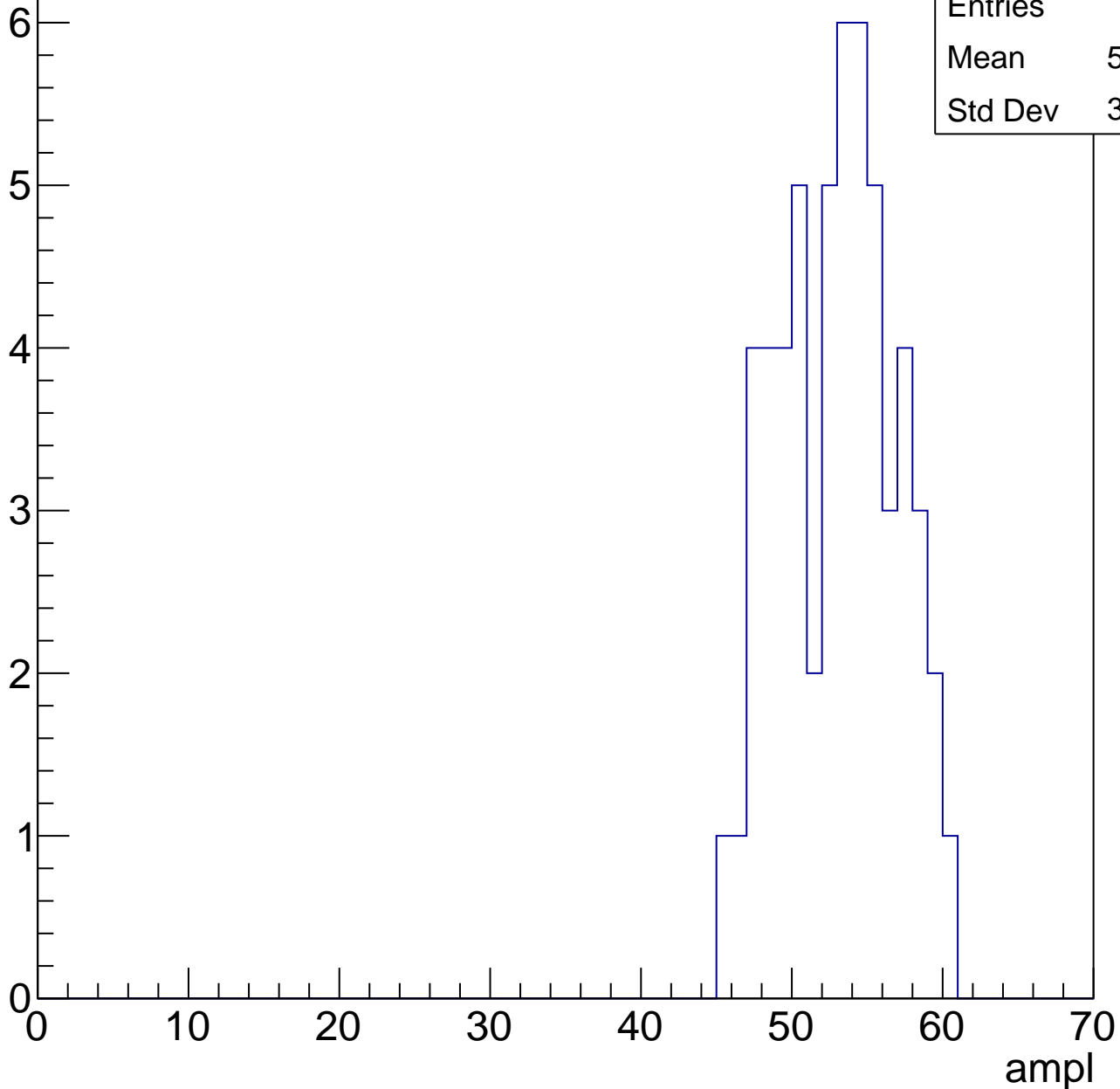


# B1L102S, U20-ch92, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	52.57
Std Dev	3.736

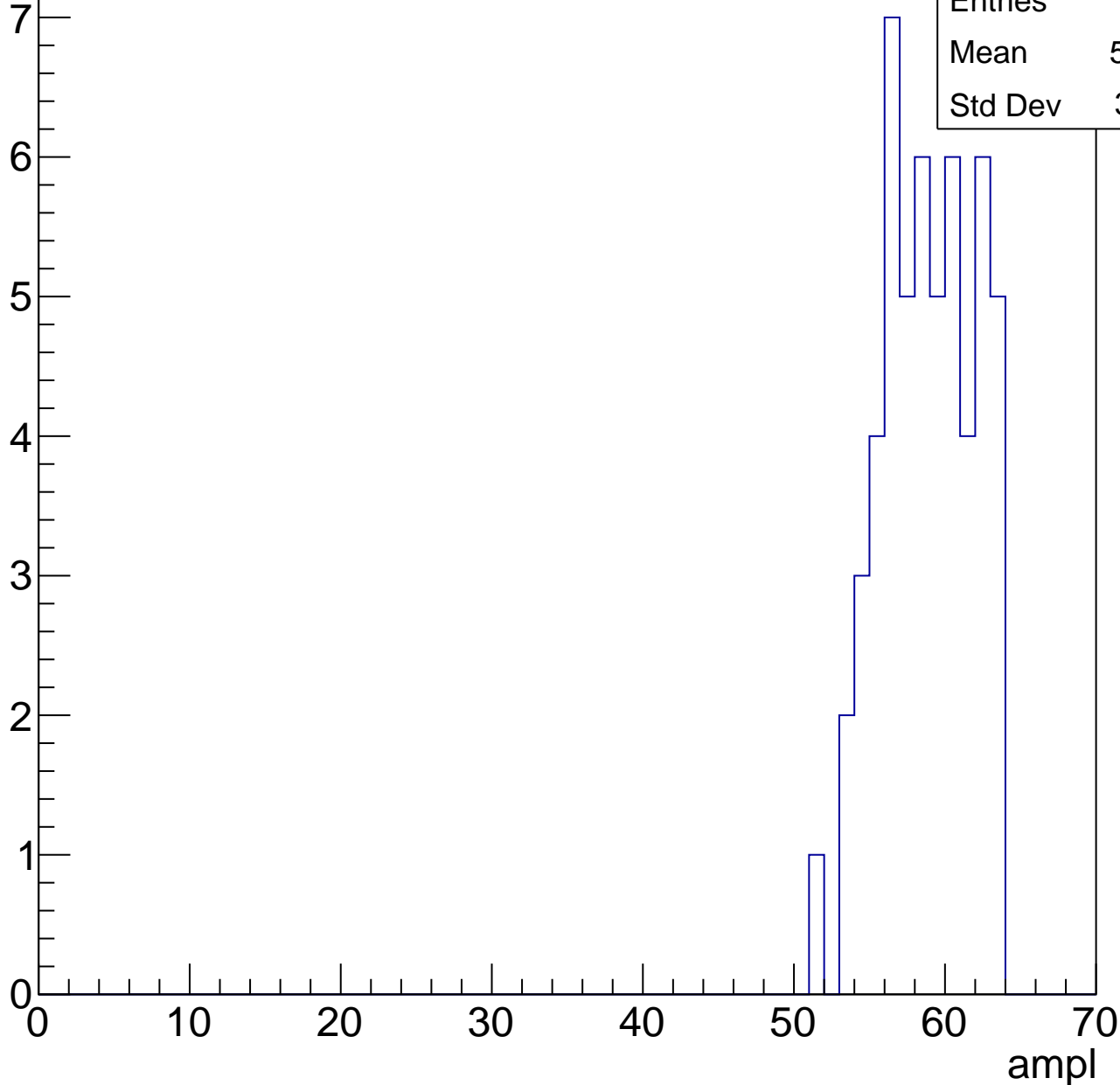


# B1L102S, U20-ch92, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	58.33
Std Dev	3.031

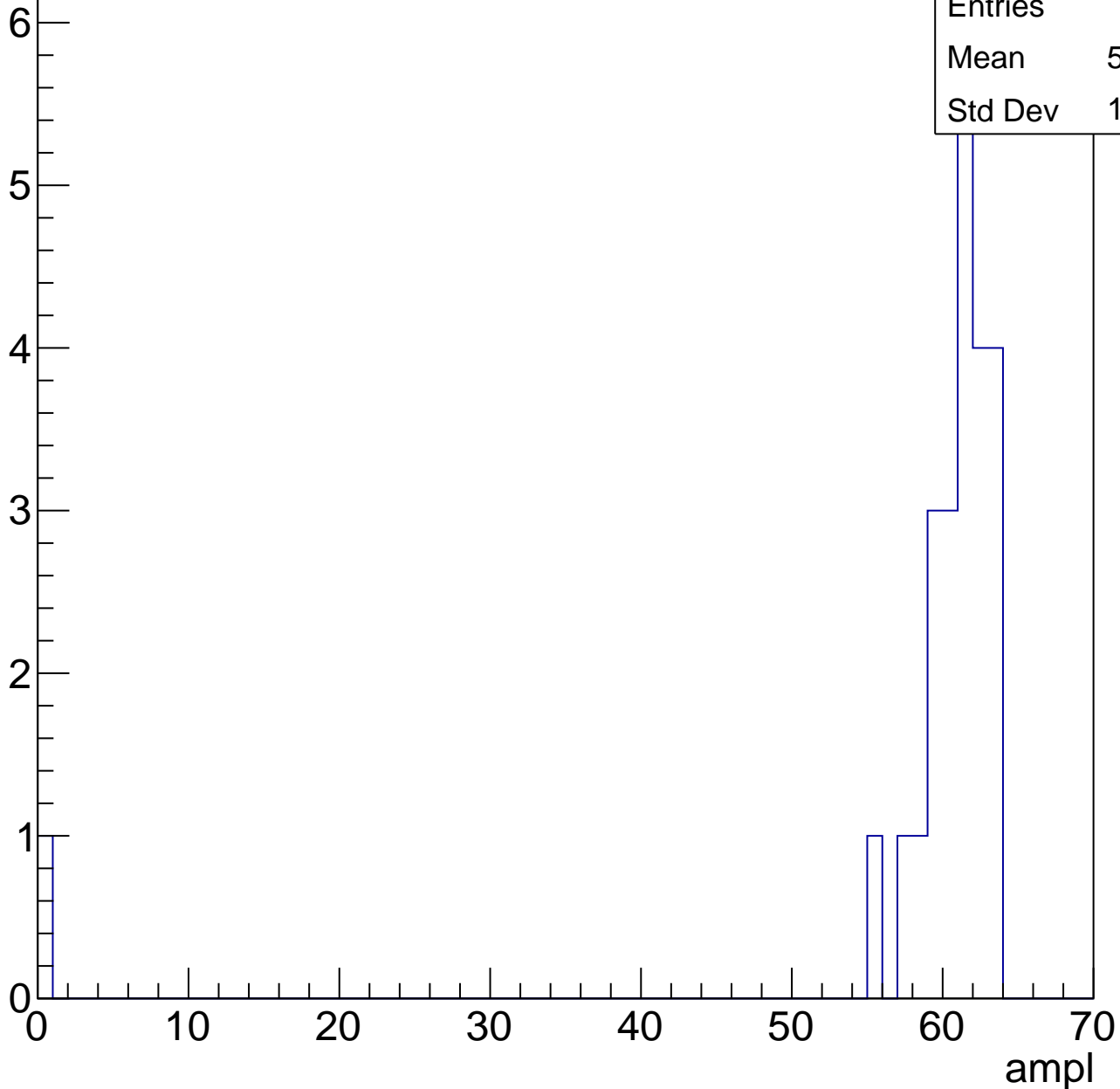


# B1L102S, U20-ch92, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	24
Mean	58.04
Std Dev	12.26





# B1L102S, U20-ch92, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch93, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	76
Mean	28.17
Std Dev	4.115

**Gaus mean : 29.5120**

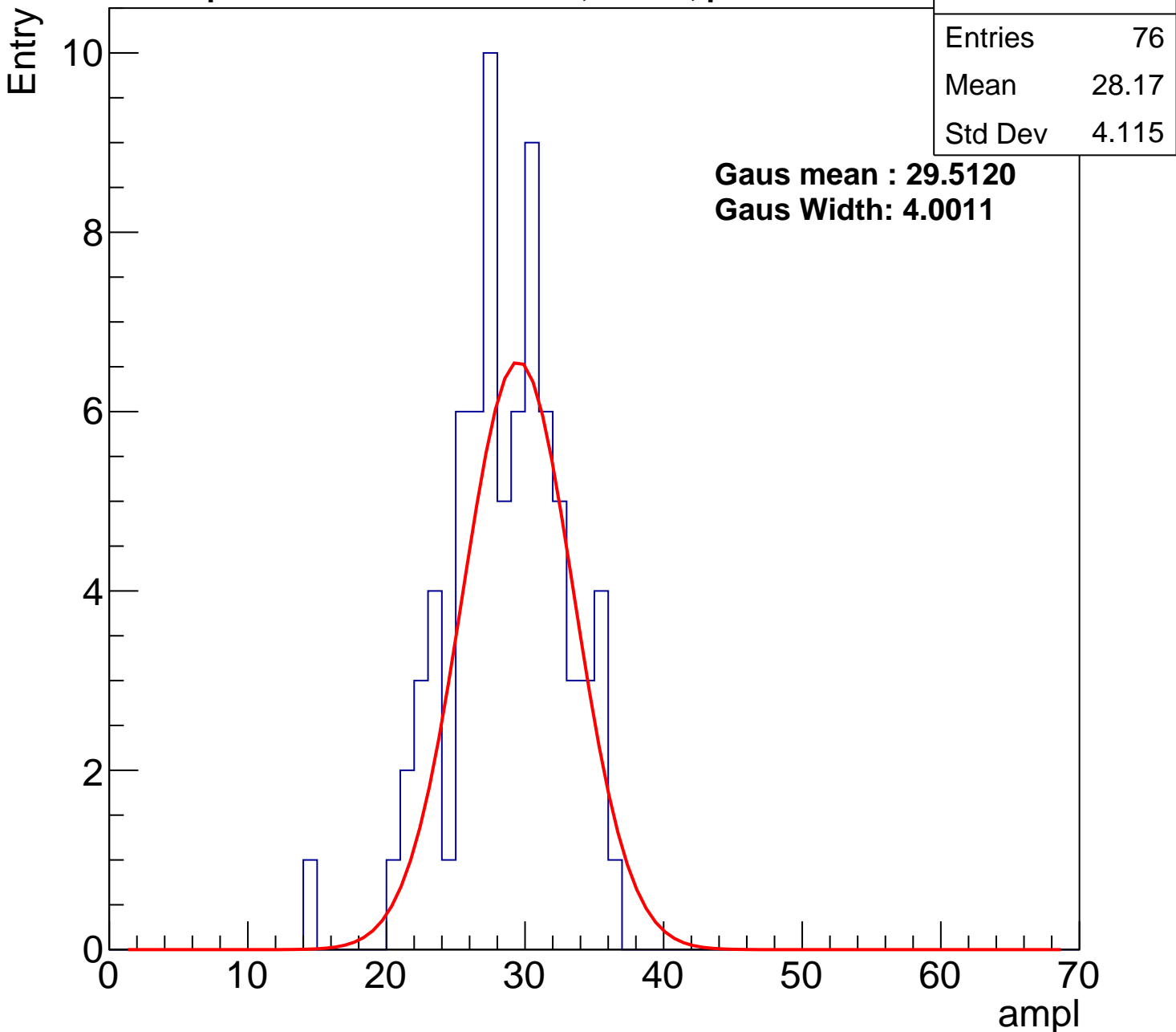
**Gaus Width: 4.0011**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U20-ch93, adc1

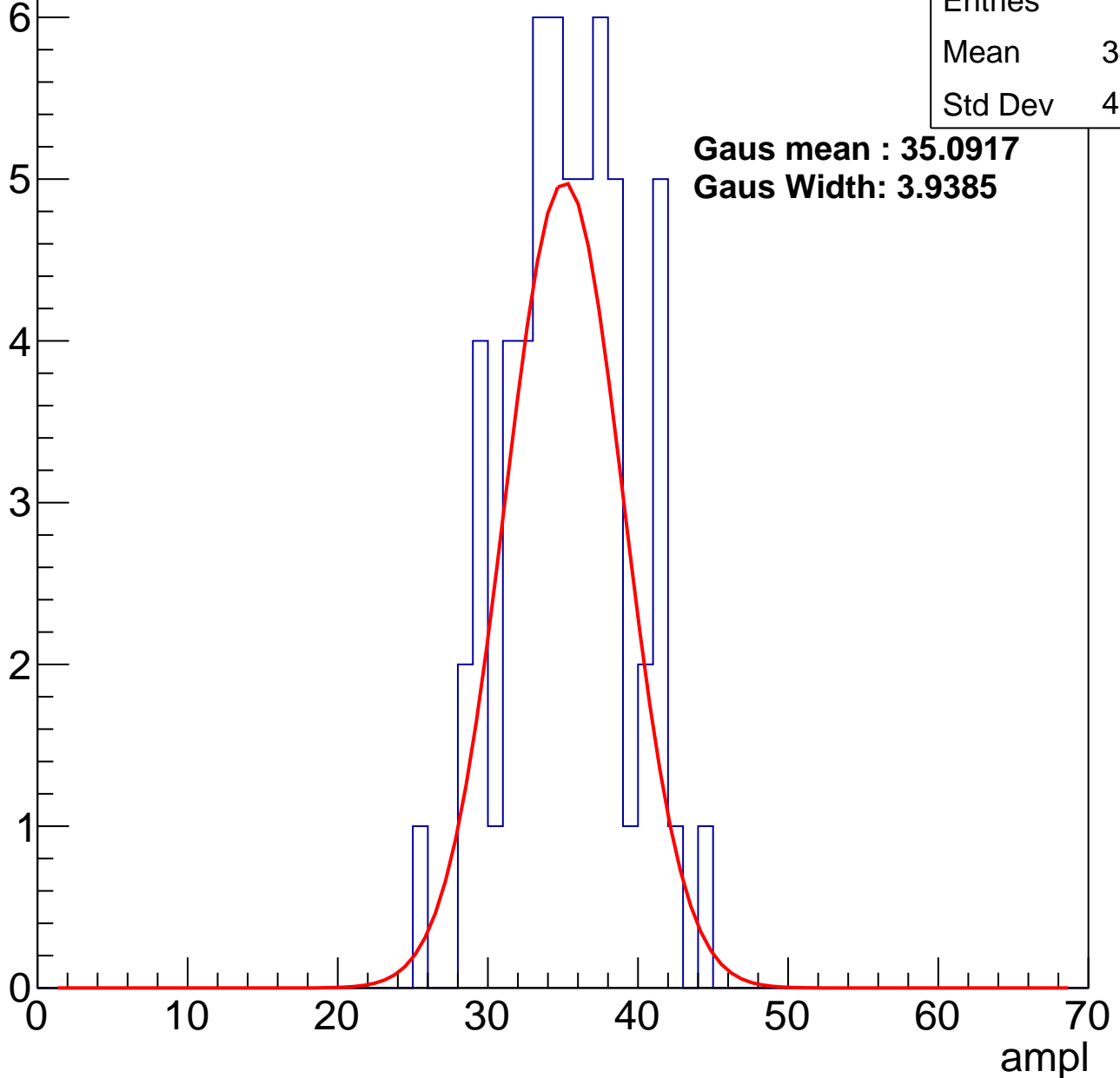
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	34.88
Std Dev	4.005

**Gaus mean : 35.0917**

**Gaus Width: 3.9385**



# B1L102S, U20-ch93, adc2

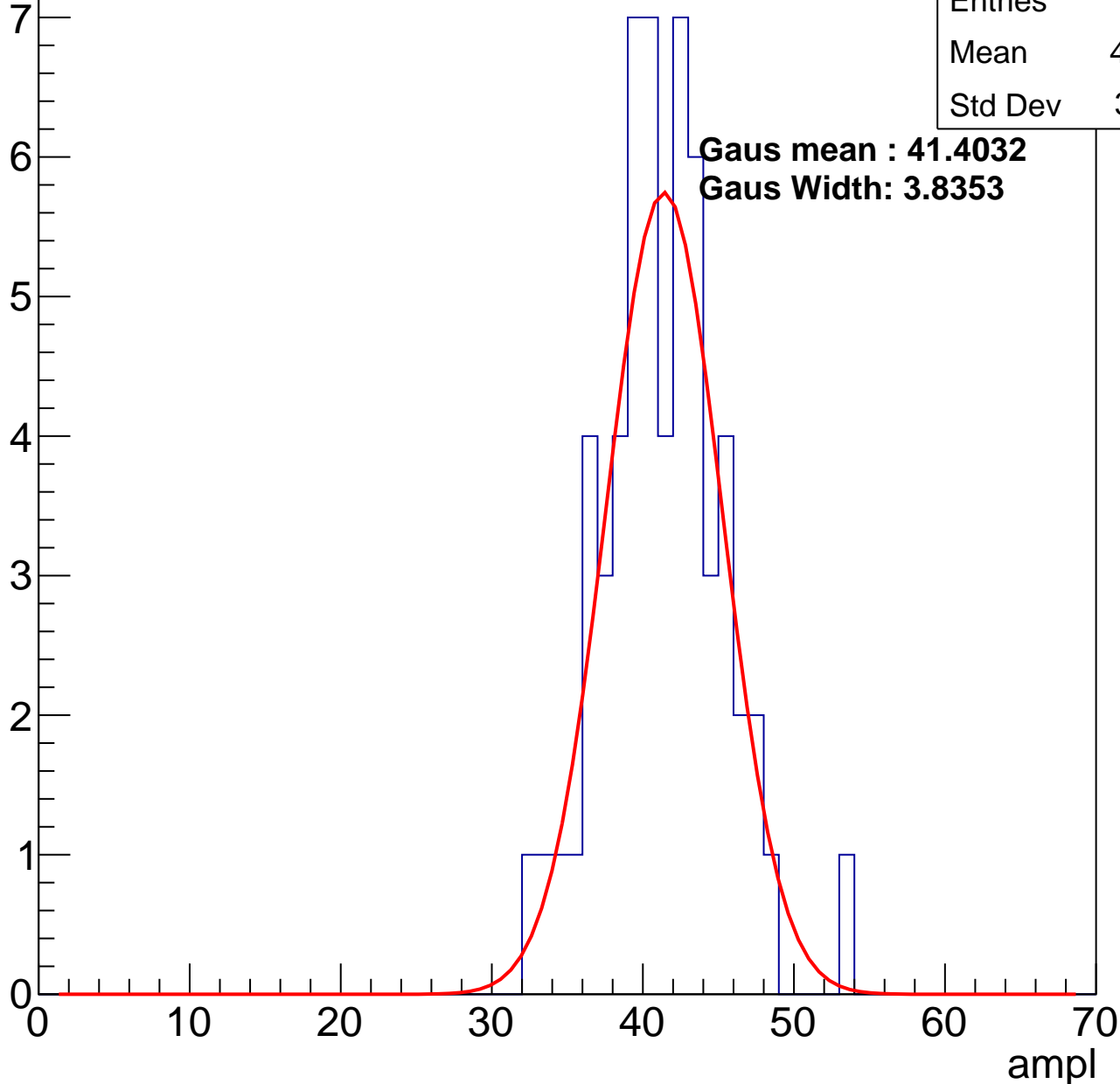
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	40.83
Std Dev	3.871

**Gaus mean : 41.4032**

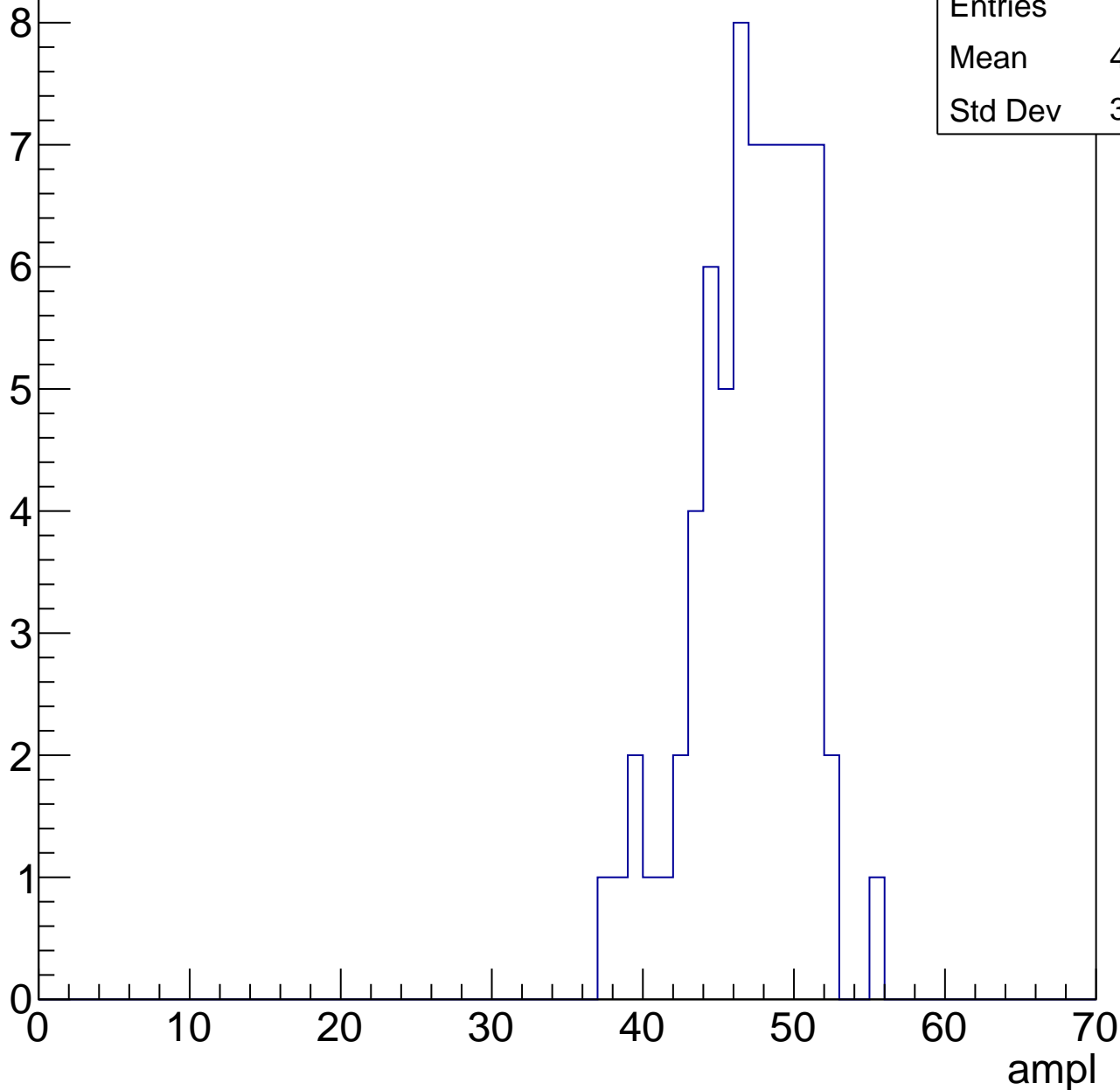
**Gaus Width: 3.8353**



# B1L102S, U20-ch93, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



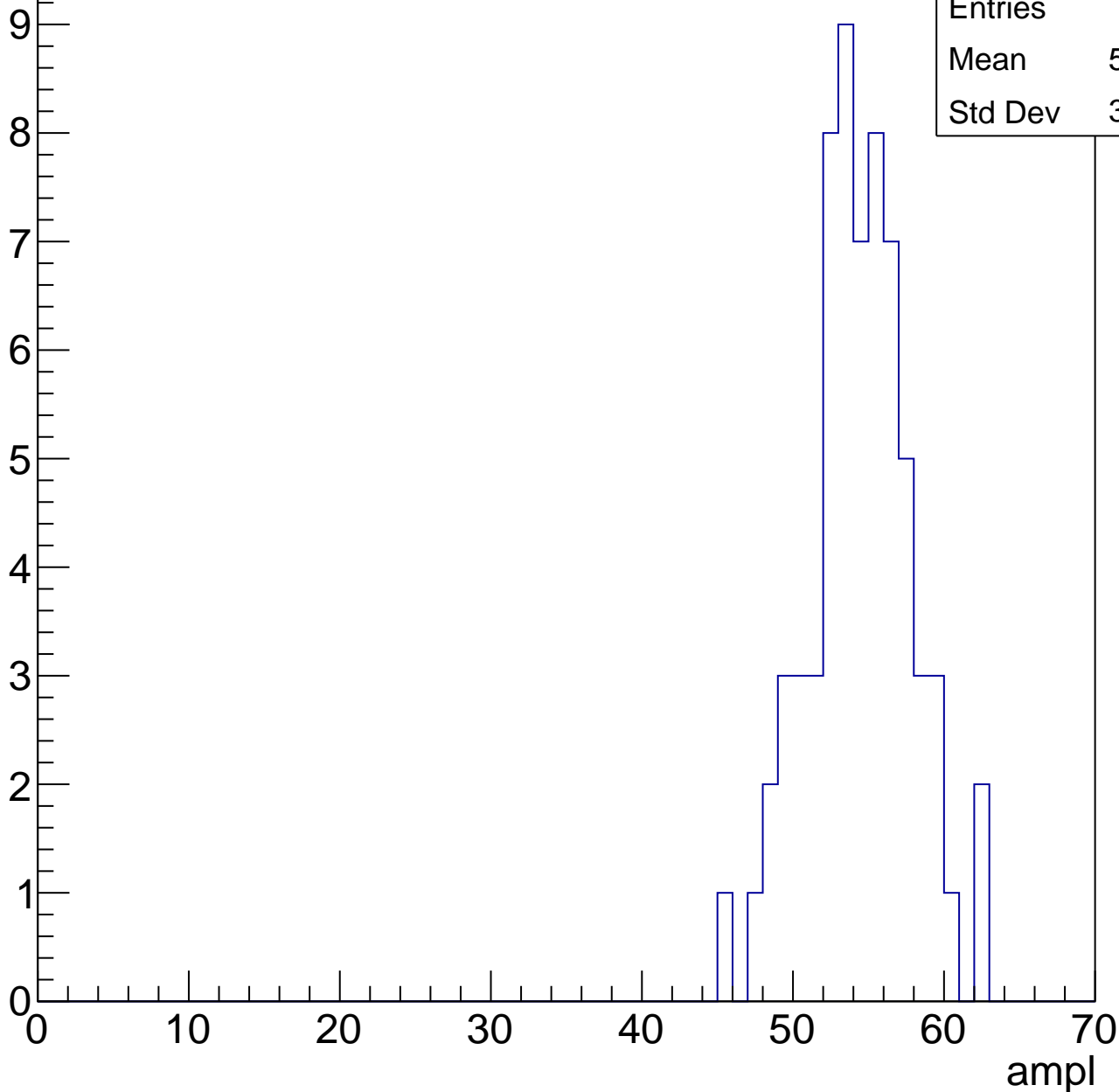
Entries	69
Mean	46.68
Std Dev	3.626

# B1L102S, U20-ch93, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	53.95
Std Dev	3.395



# B1L102S, U20-ch93, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	43
Mean	59.16
Std Dev	2.391

ampl

0 10 20 30 40 50 60 70

0

1

2

3

4

5

6

7

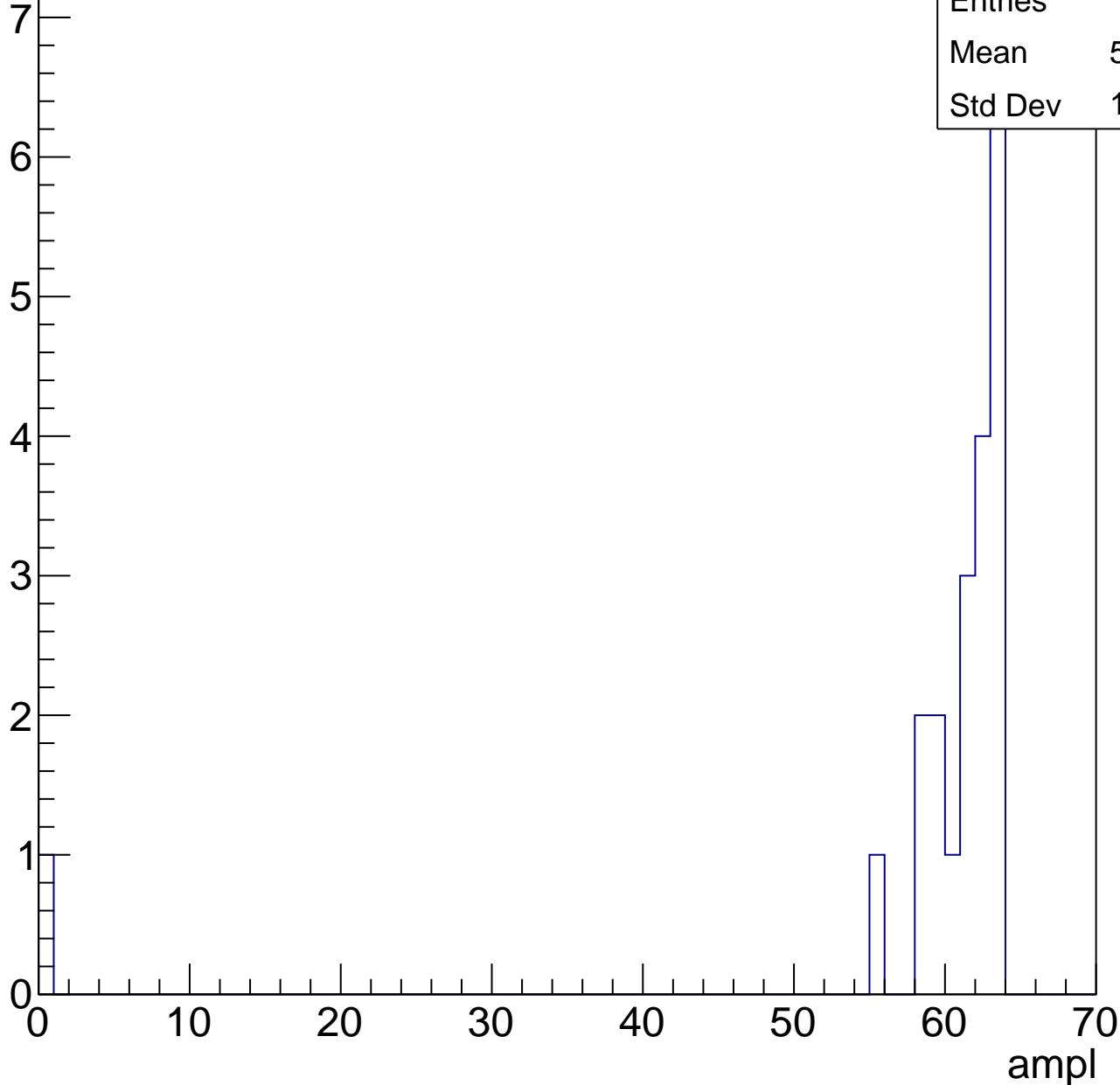
8

# B1L102S, U20-ch93, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	21
Mean	58.14
Std Dev	13.17





# B1L102S, U20-ch93, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L102S, U20-ch94, adc0

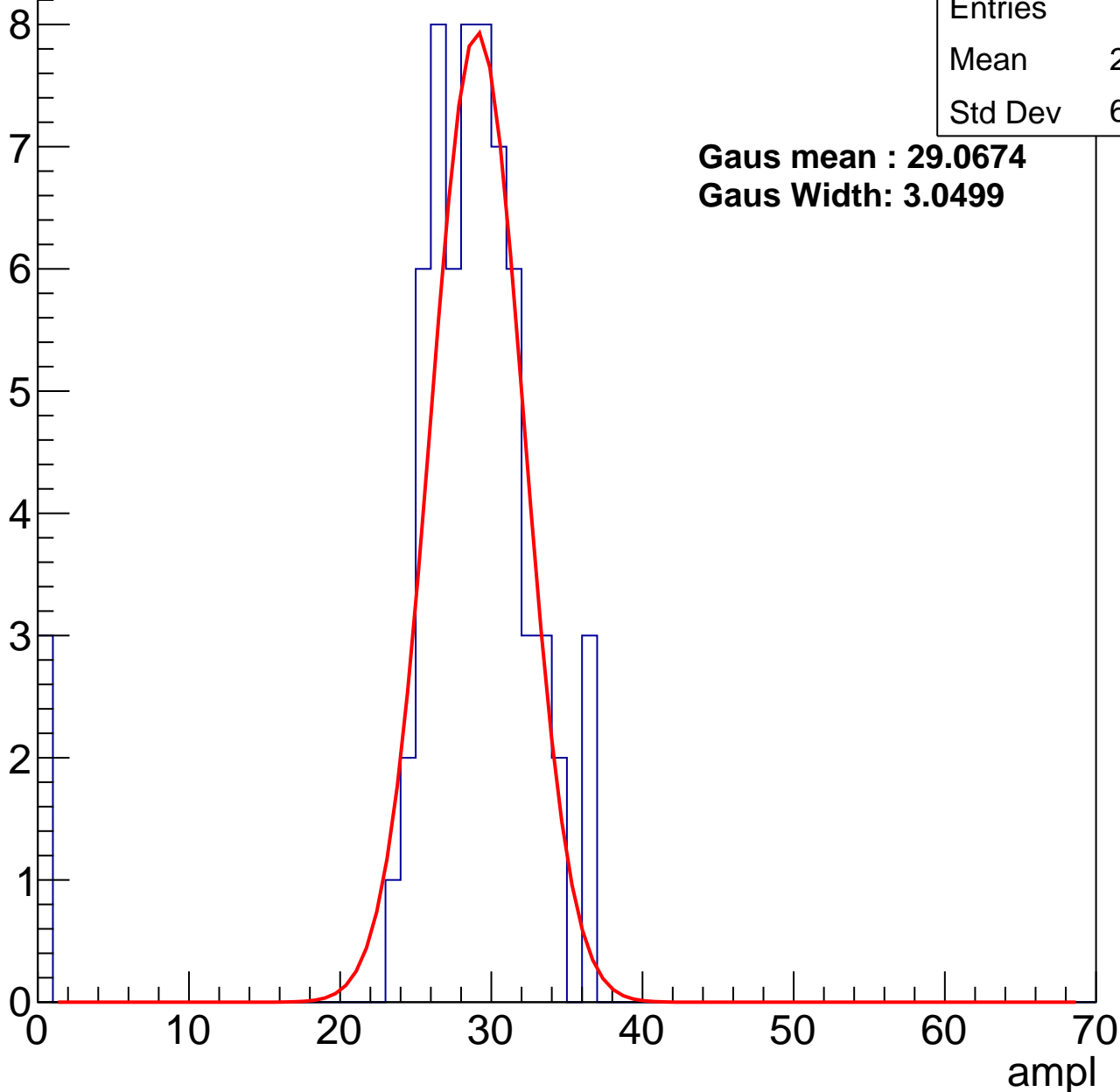
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	27.48
Std Dev	6.697

**Gaus mean : 29.0674**

**Gaus Width: 3.0499**



# B1L102S, U20-ch94, adc1

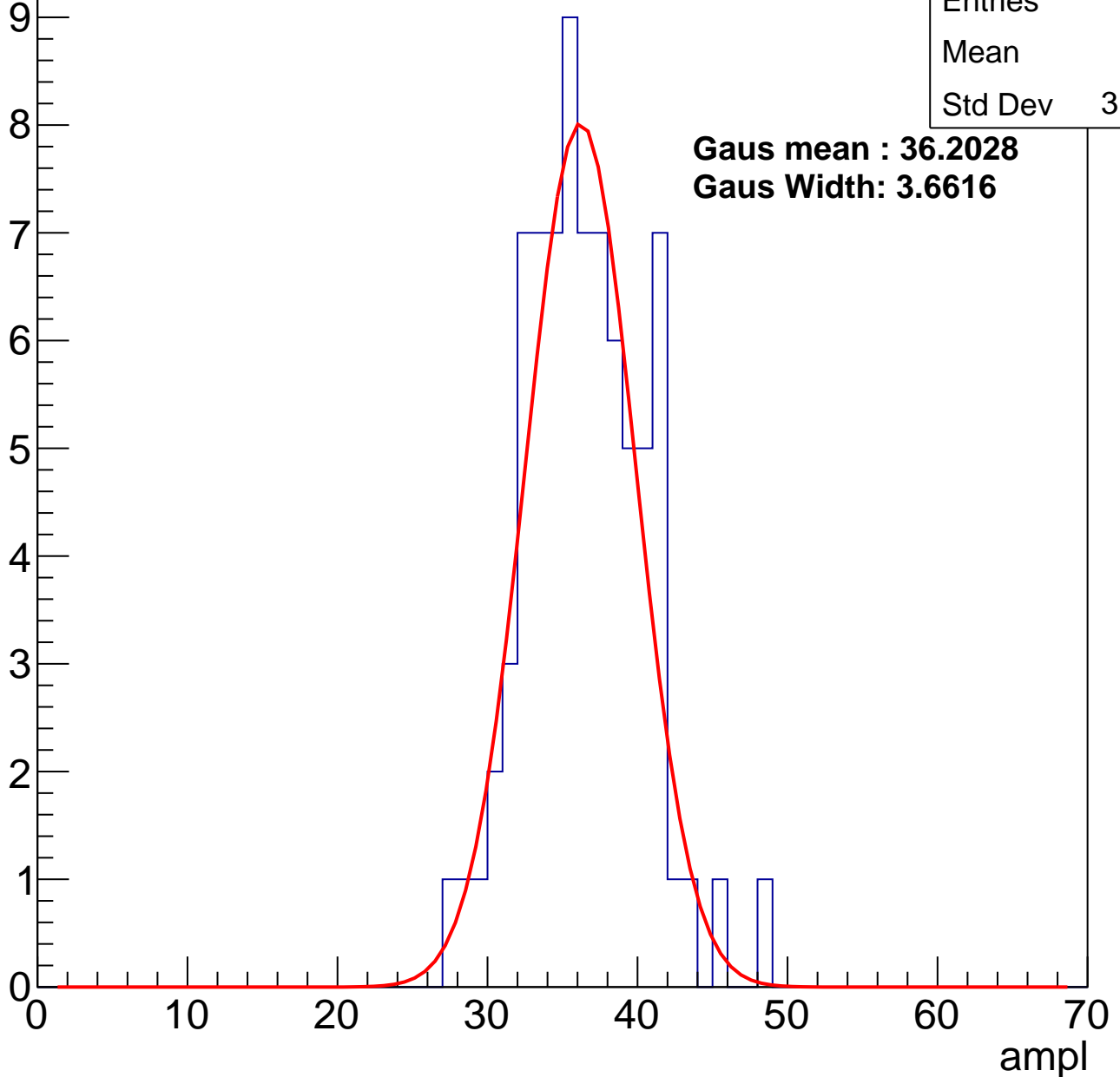
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	79
Mean	36
Std Dev	3.888

**Gaus mean : 36.2028**

**Gaus Width: 3.6616**



# B1L102S, U20-ch94, adc2

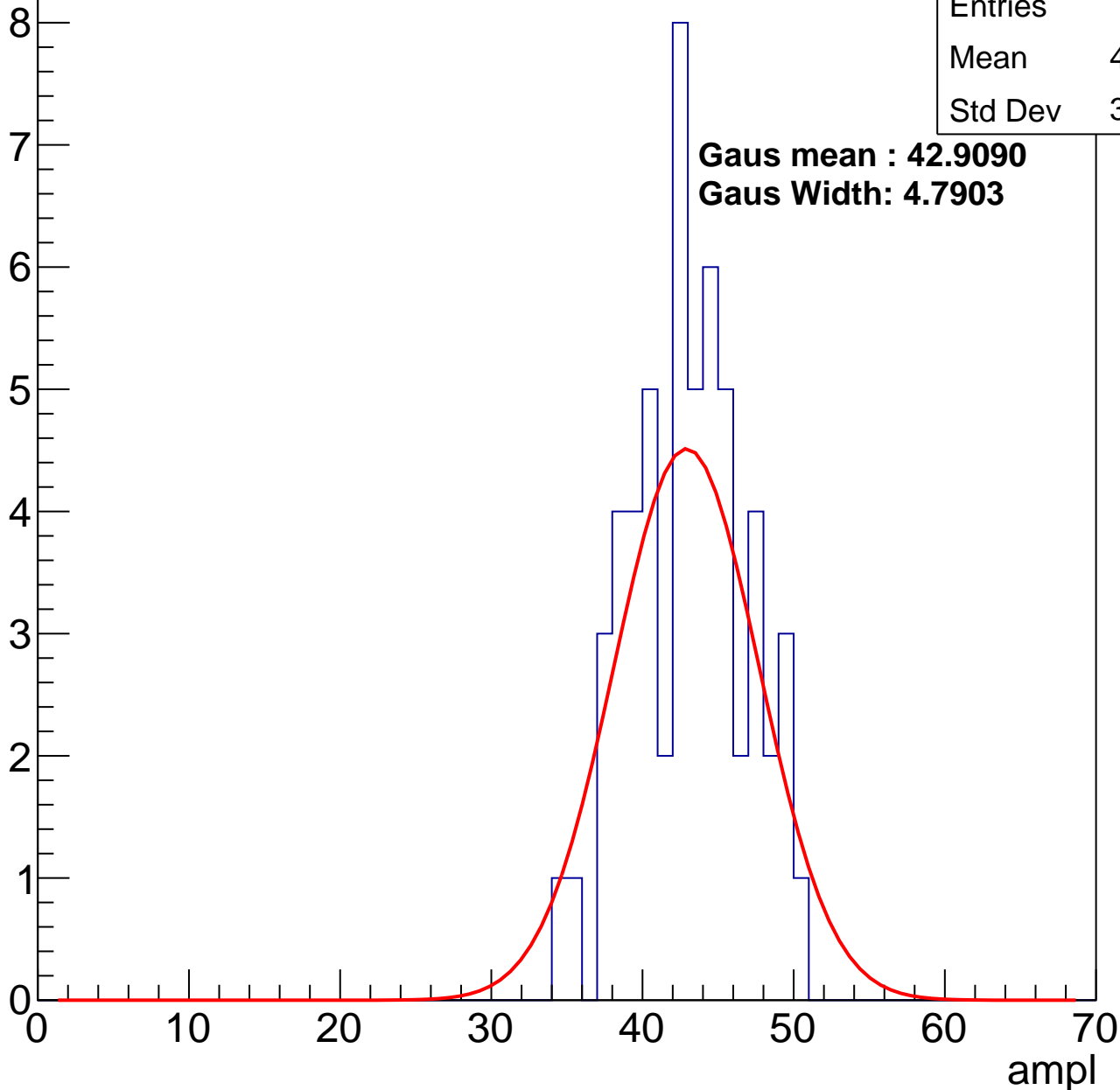
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	42.55
Std Dev	3.736

**Gaus mean : 42.9090**

**Gaus Width: 4.7903**

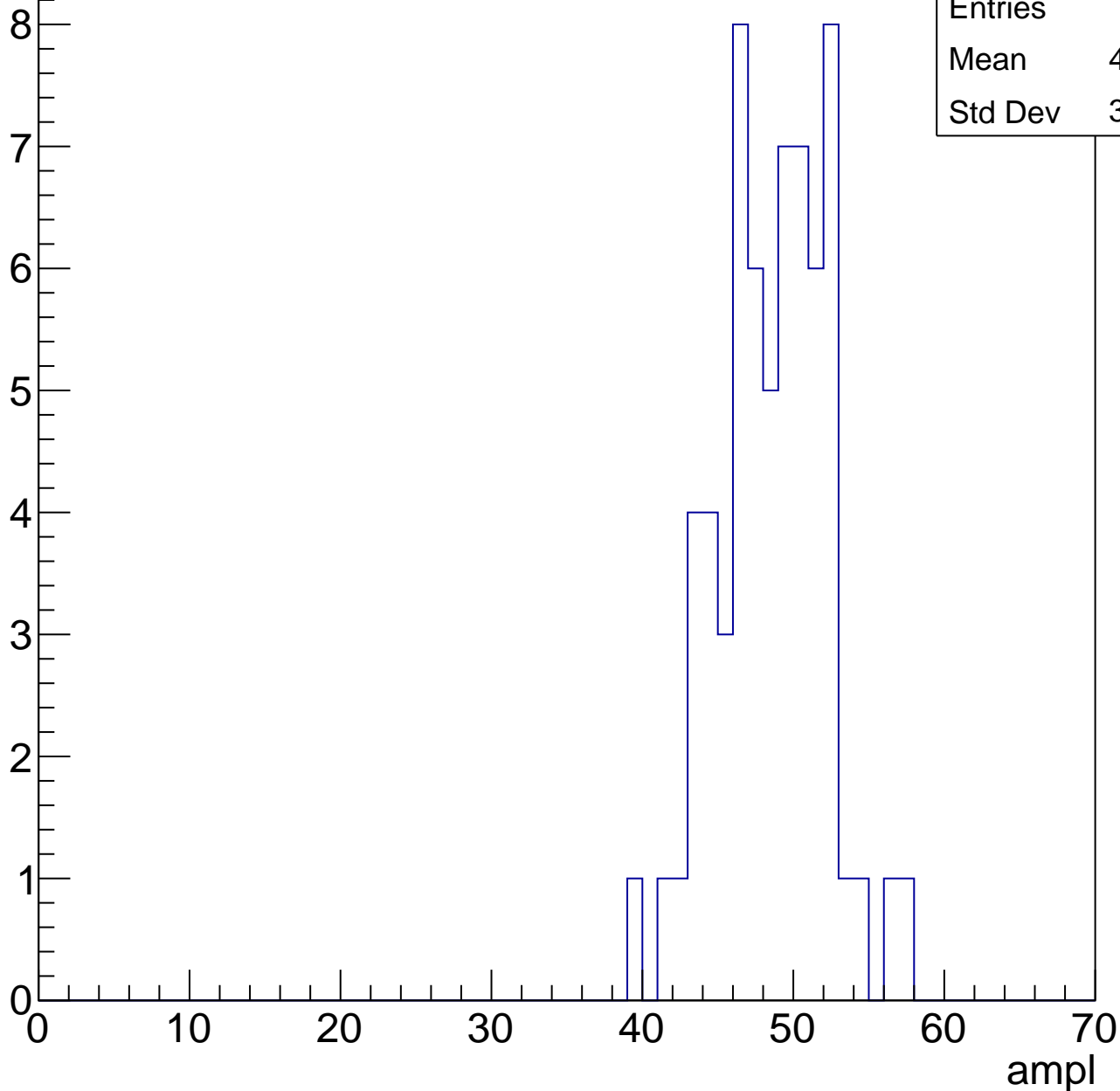


# B1L102S, U20-ch94, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	48.15
Std Dev	3.544

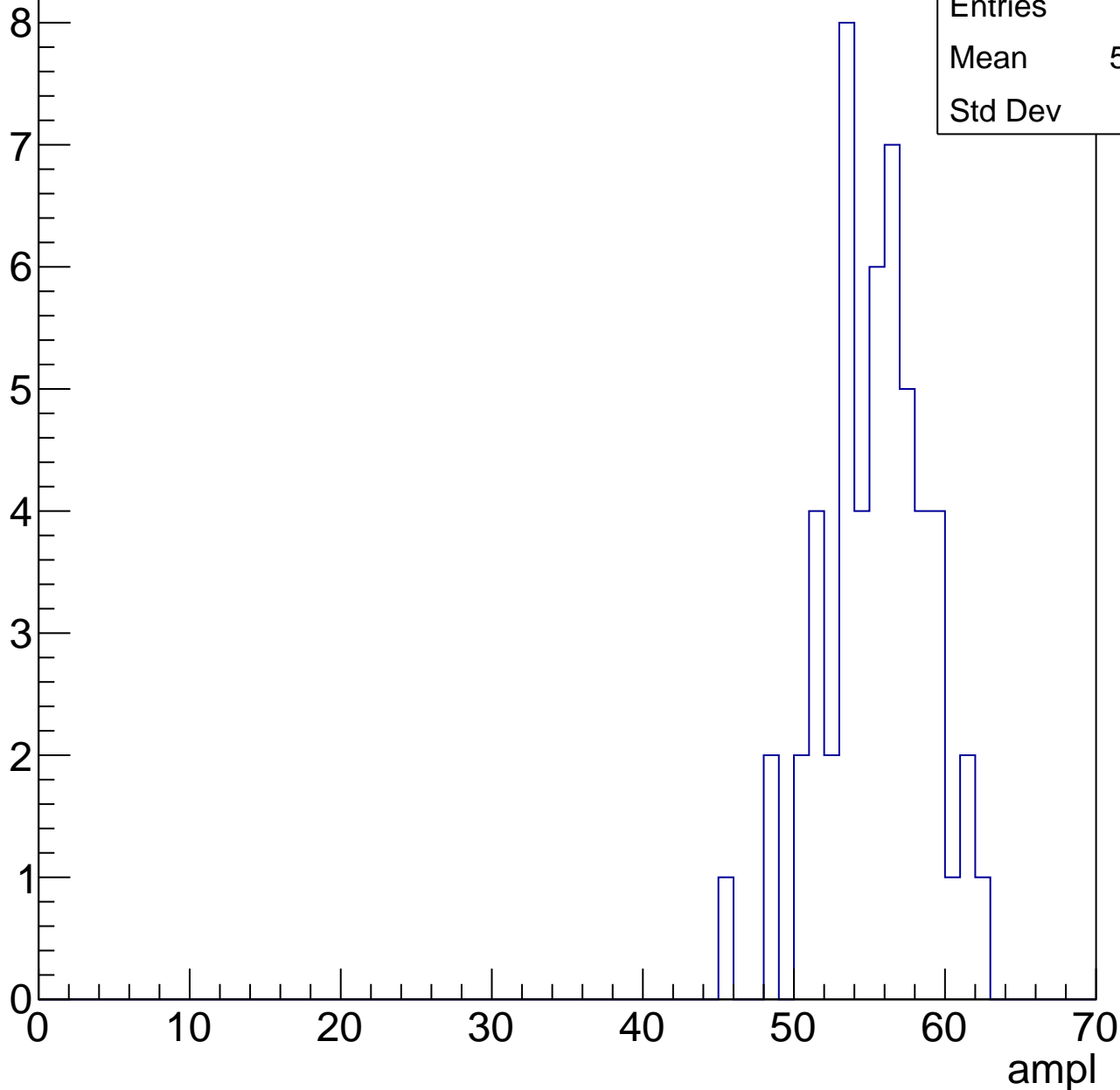


# B1L102S, U20-ch94, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	54.87
Std Dev	3.47

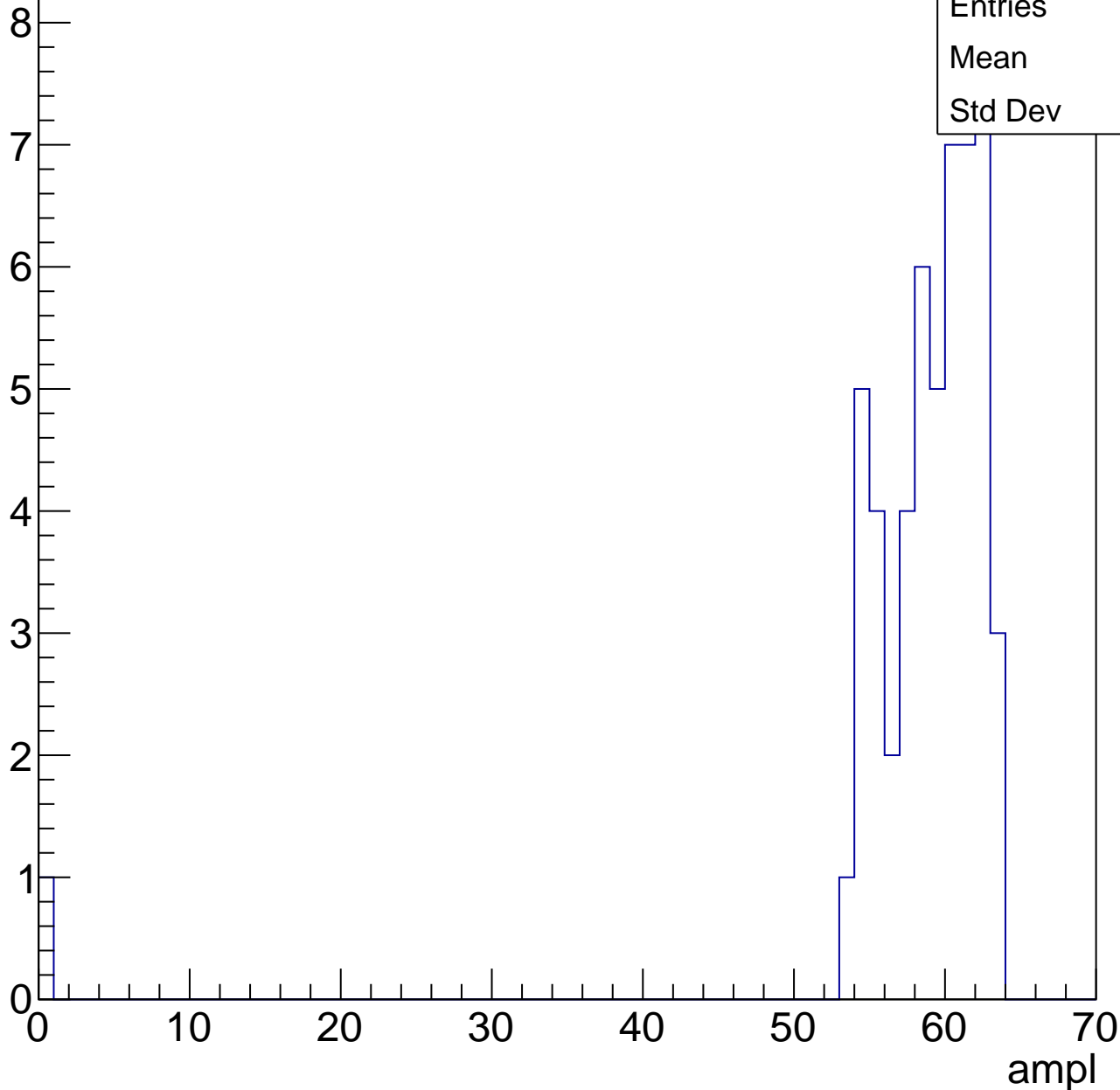


# B1L102S, U20-ch94, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	57.7
Std Dev	8.48

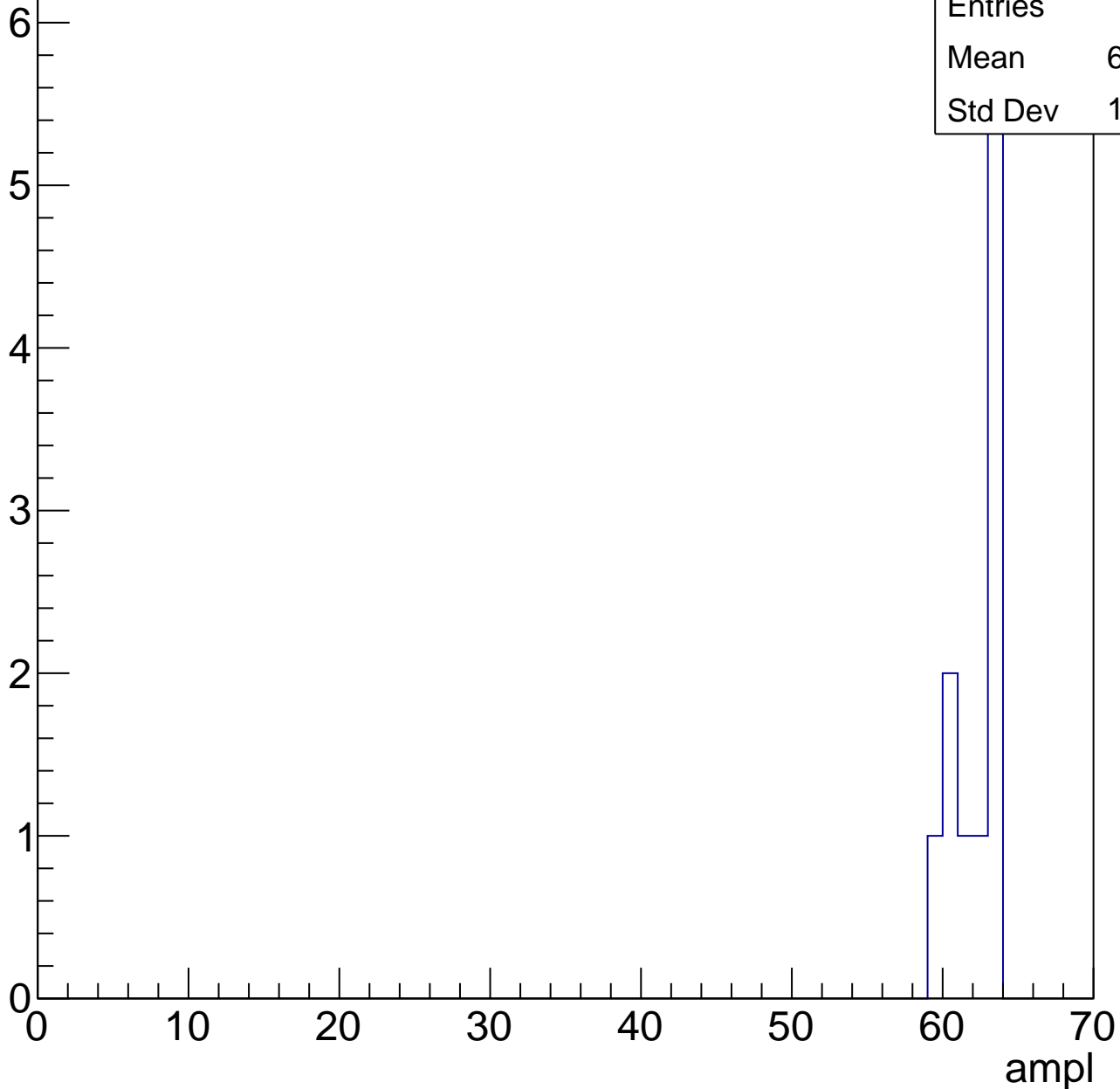


# B1L102S, U20-ch94, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	11
Mean	61.82
Std Dev	1.466

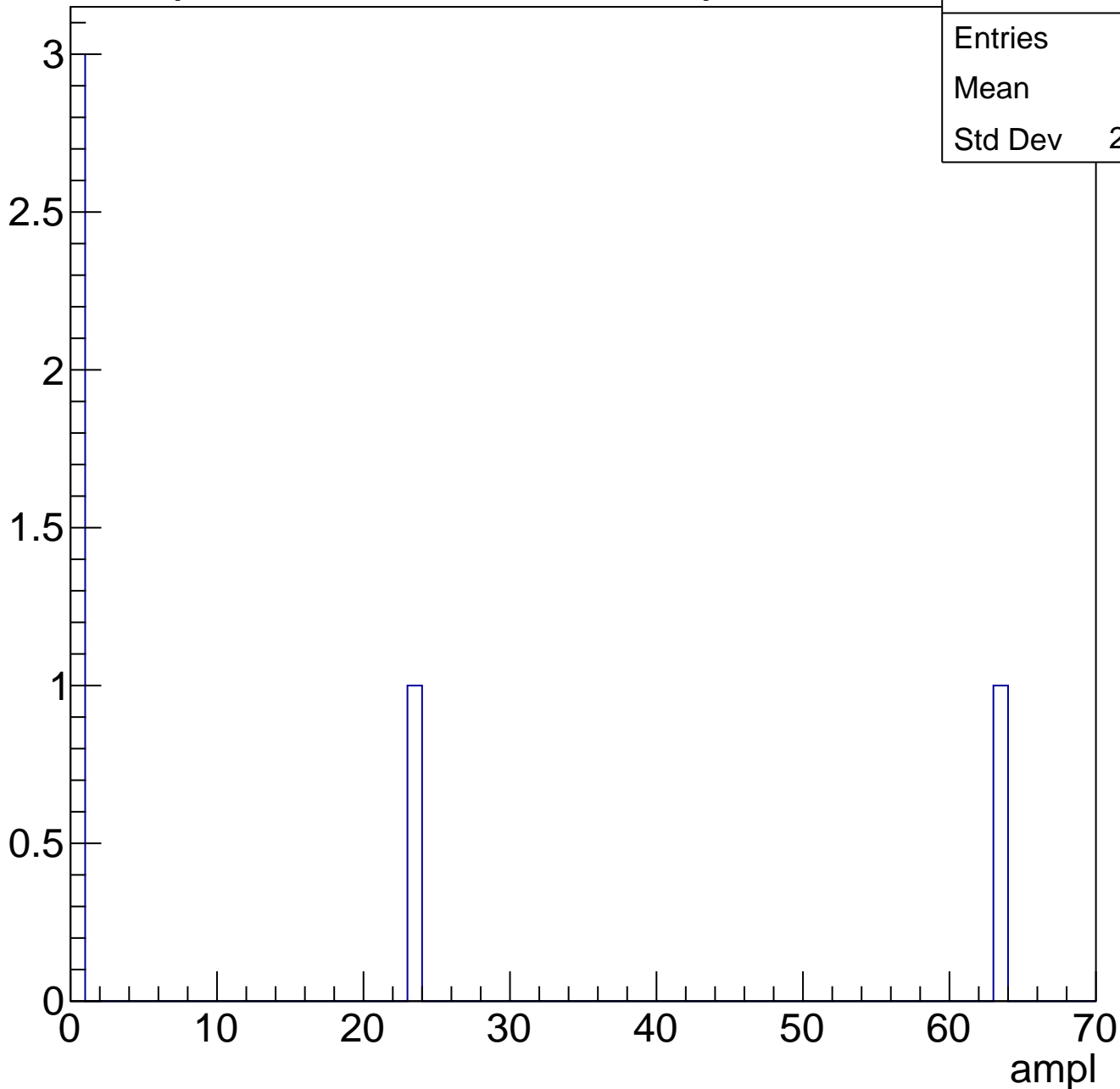




# B1L102S, U20-ch94, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	5
Mean	17.2
Std Dev	24.57

# B1L102S, U20-ch95, adc0

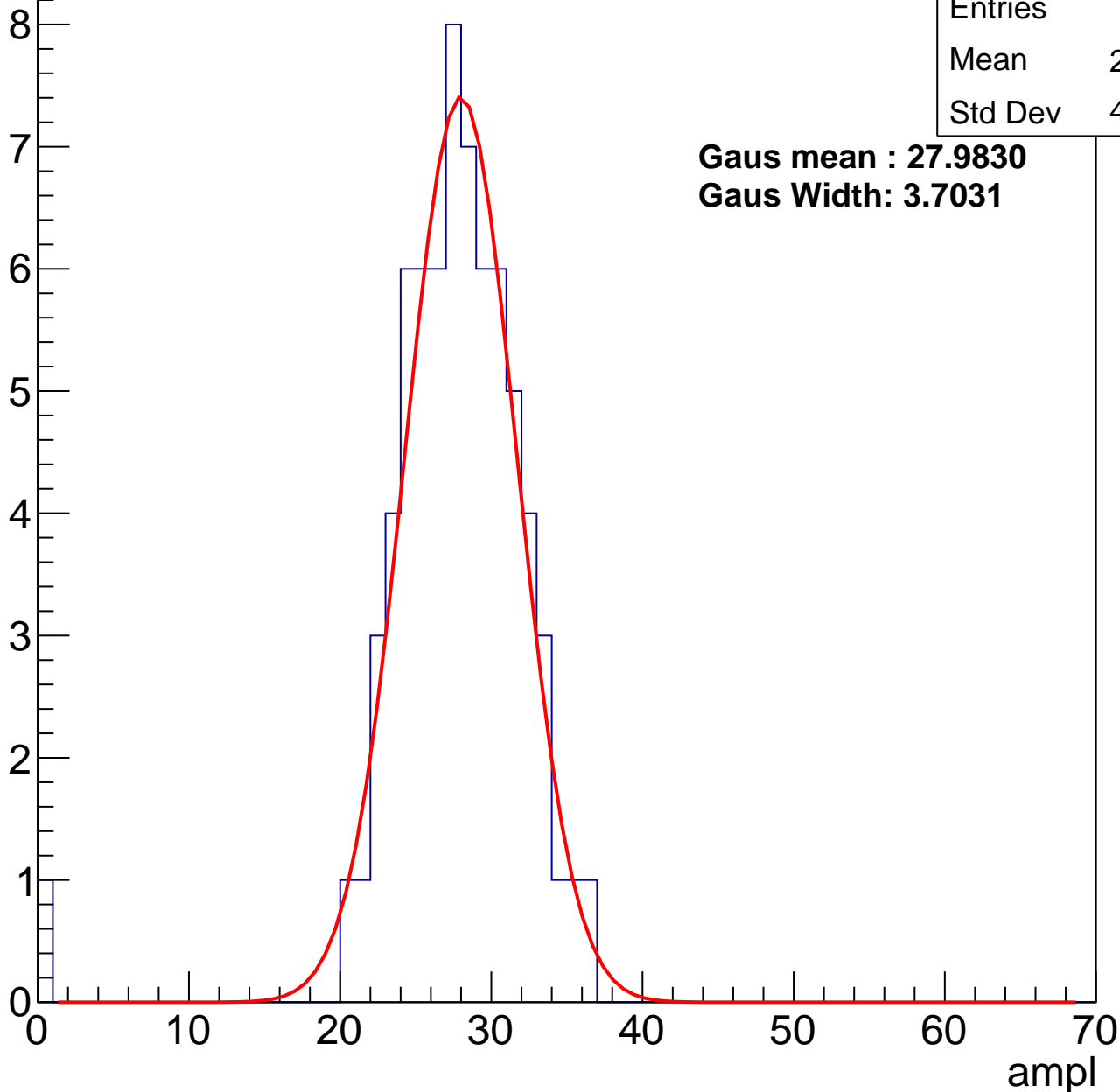
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	27.17
Std Dev	4.784

**Gaus mean : 27.9830**

**Gaus Width: 3.7031**



# B1L102S, U20-ch95, adc1

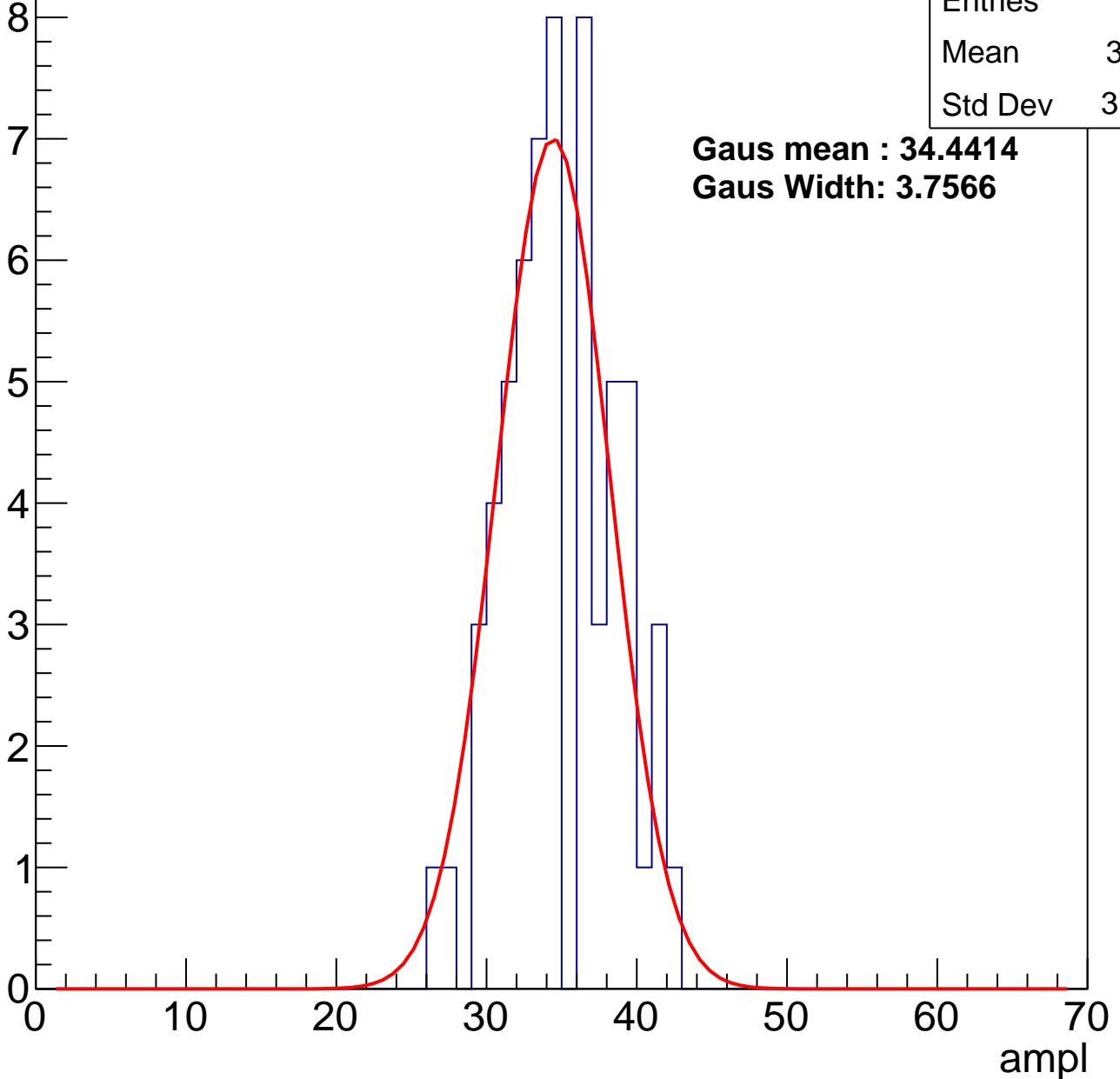
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	34.41
Std Dev	3.686

**Gaus mean : 34.4414**

**Gaus Width: 3.7566**



# B1L102S, U20-ch95, adc2

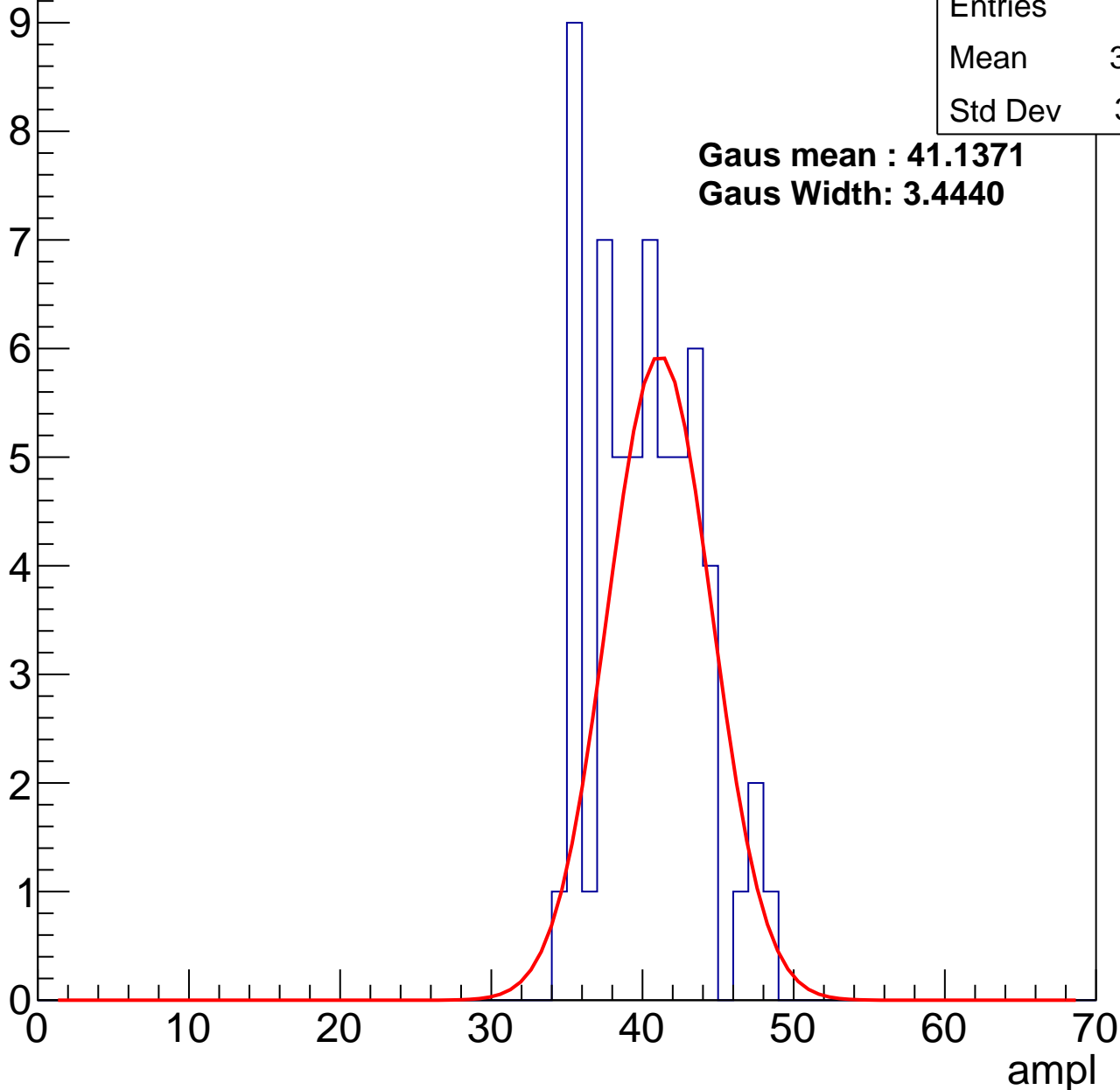
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	39.76
Std Dev	3.451

**Gaus mean : 41.1371**

**Gaus Width: 3.4440**

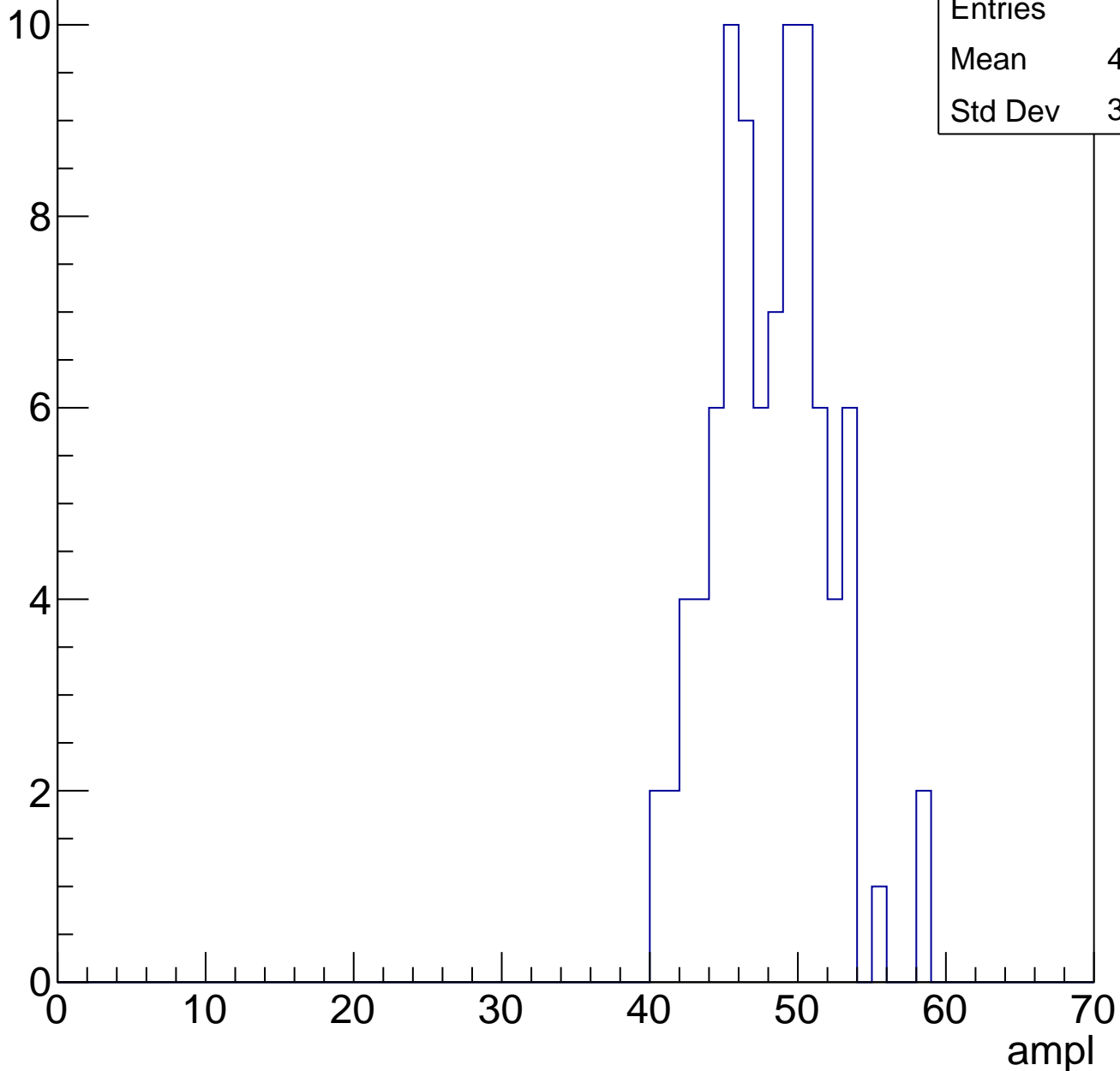


# B1L102S, U20-ch95, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

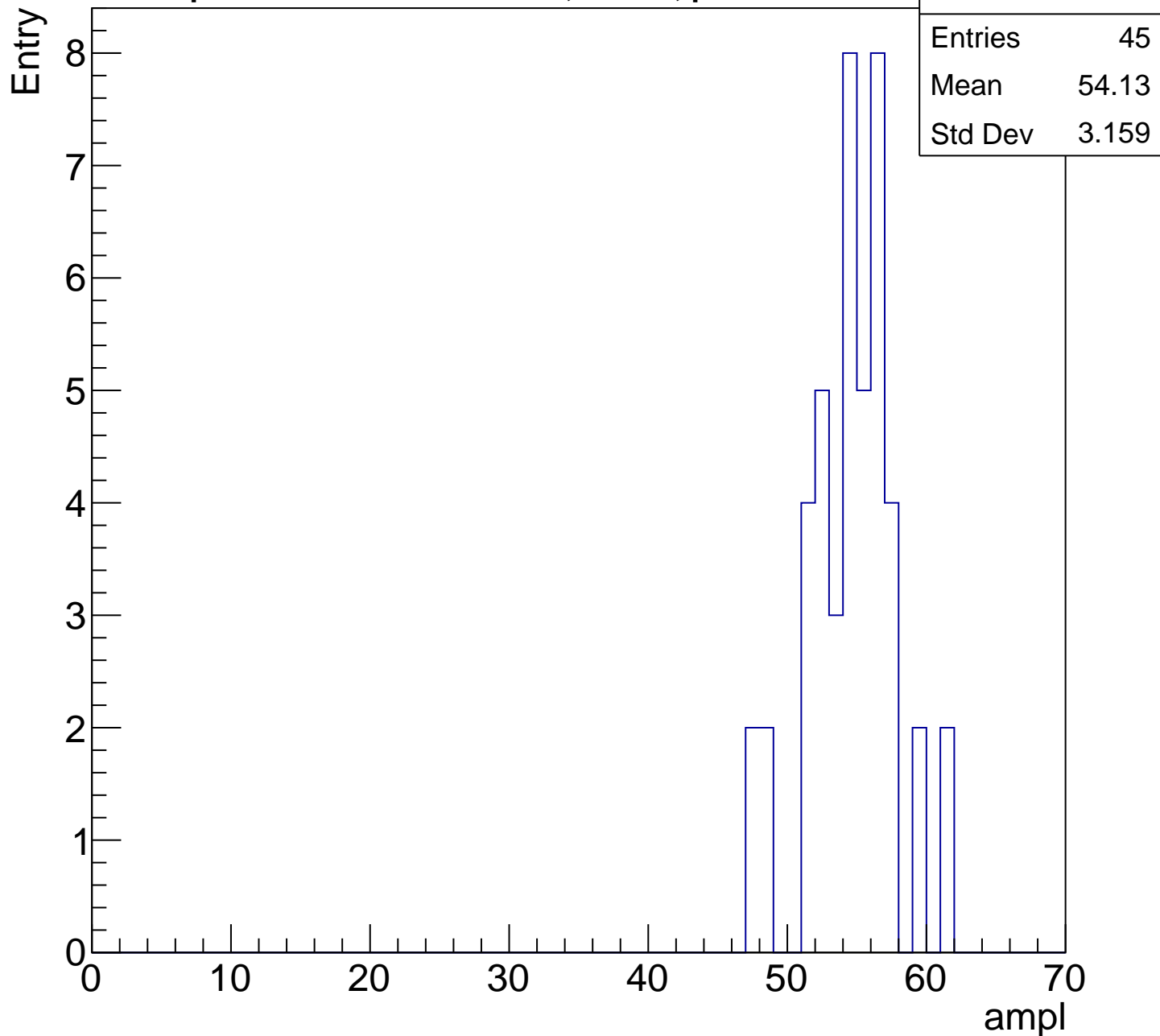
Entries	89
Mean	47.65
Std Dev	3.754

Entry



# B1L102S, U20-ch95, adc4

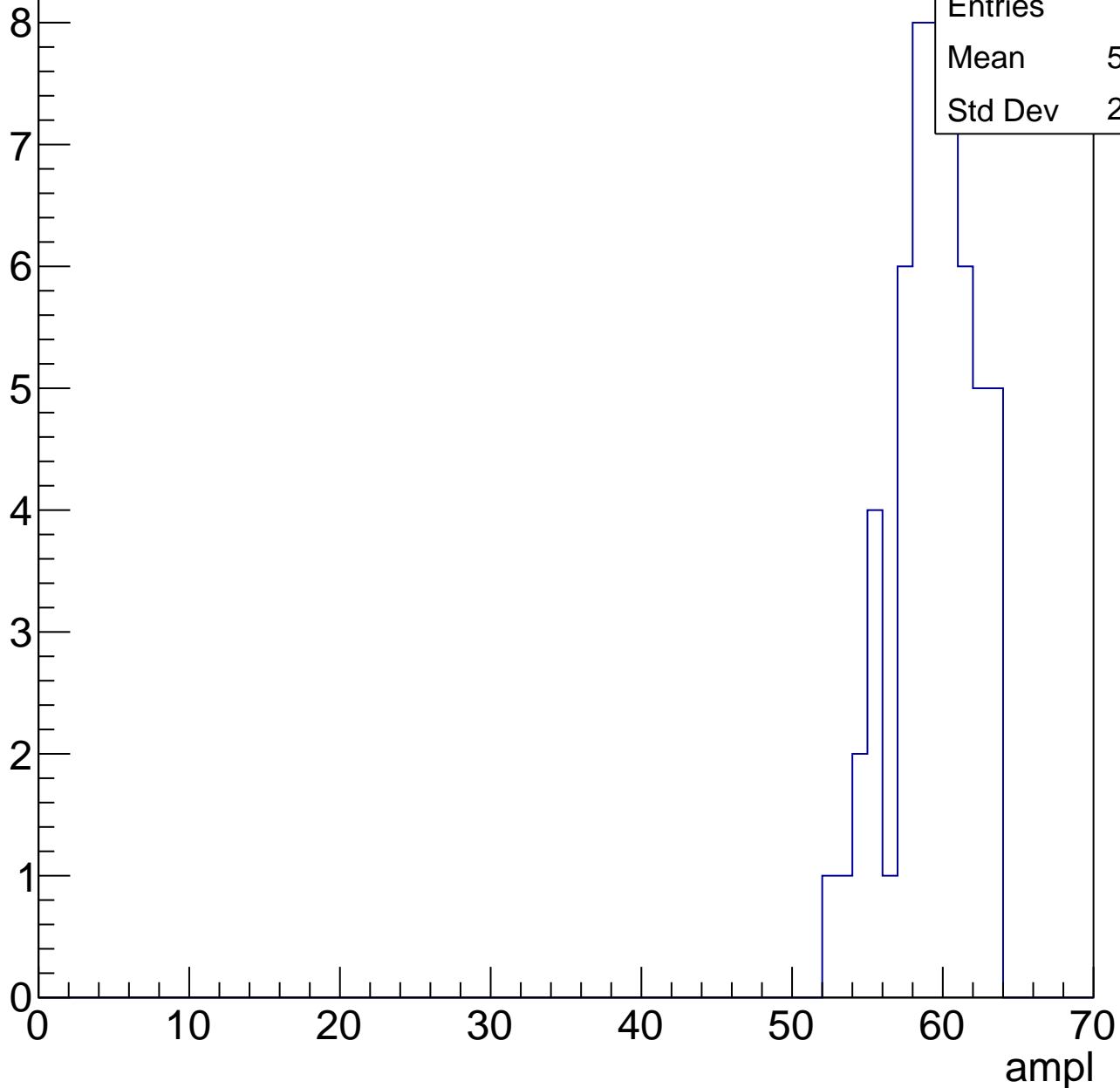
calib\_packv5\_042523\_0143.root, FC#11, port A2



# B1L102S, U20-ch95, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

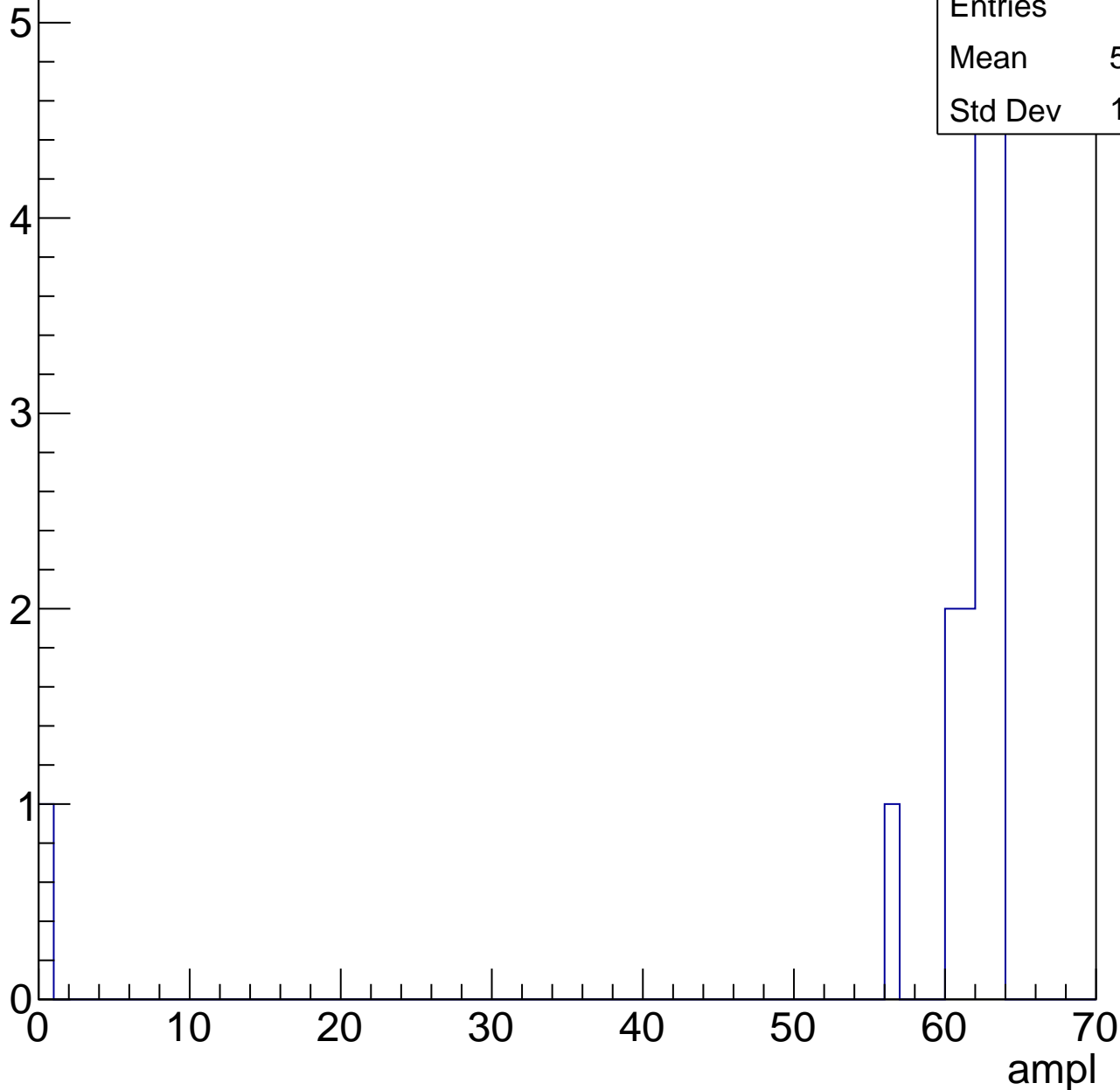


# B1L102S, U20-ch95, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	16
Mean	57.69
Std Dev	14.99





# B1L102S, U20-ch95, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch96, adc0

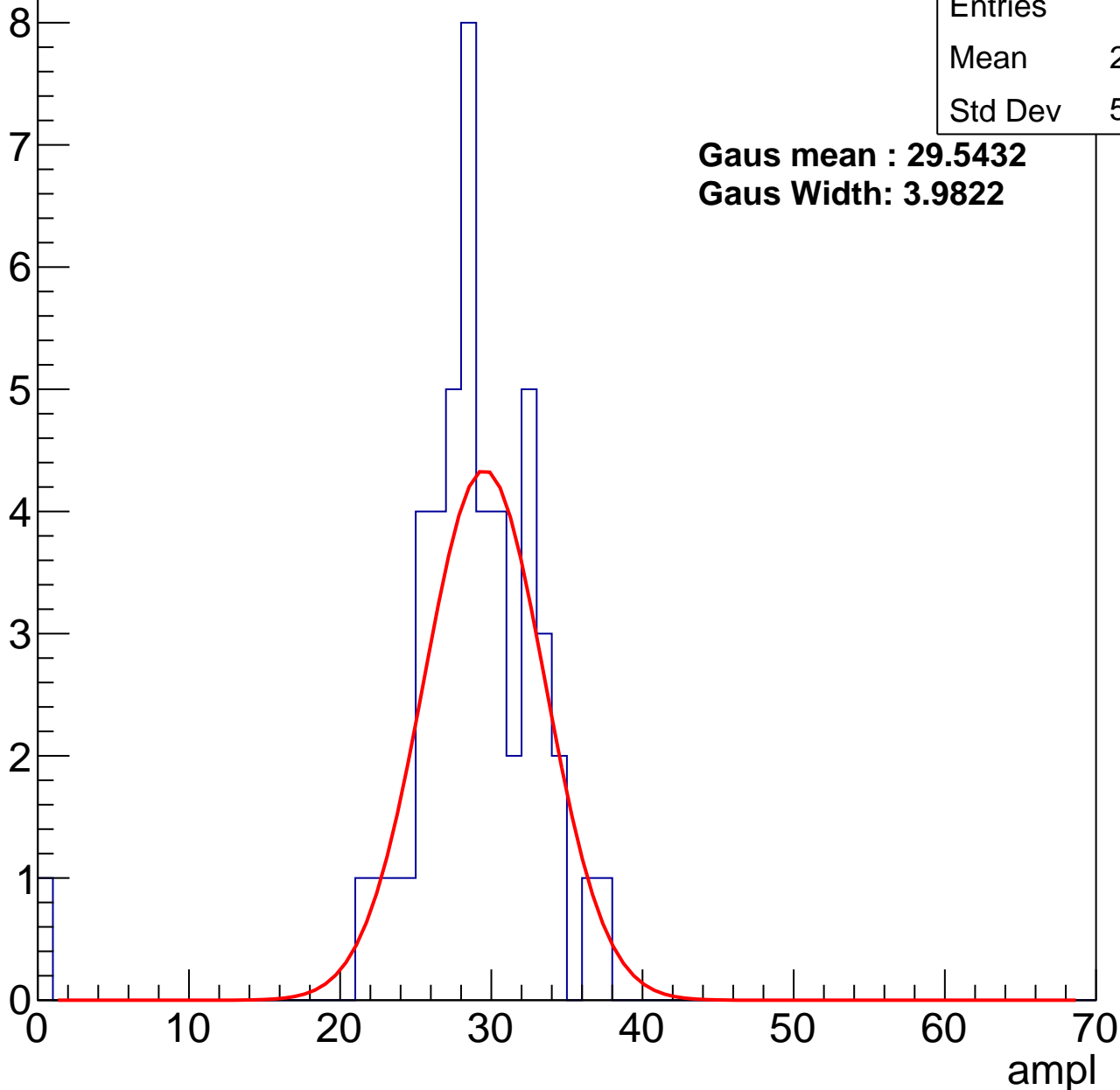
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	48
Mean	28.15
Std Dev	5.354

**Gaus mean : 29.5432**

**Gaus Width: 3.9822**



# B1L102S, U20-ch96, adc1

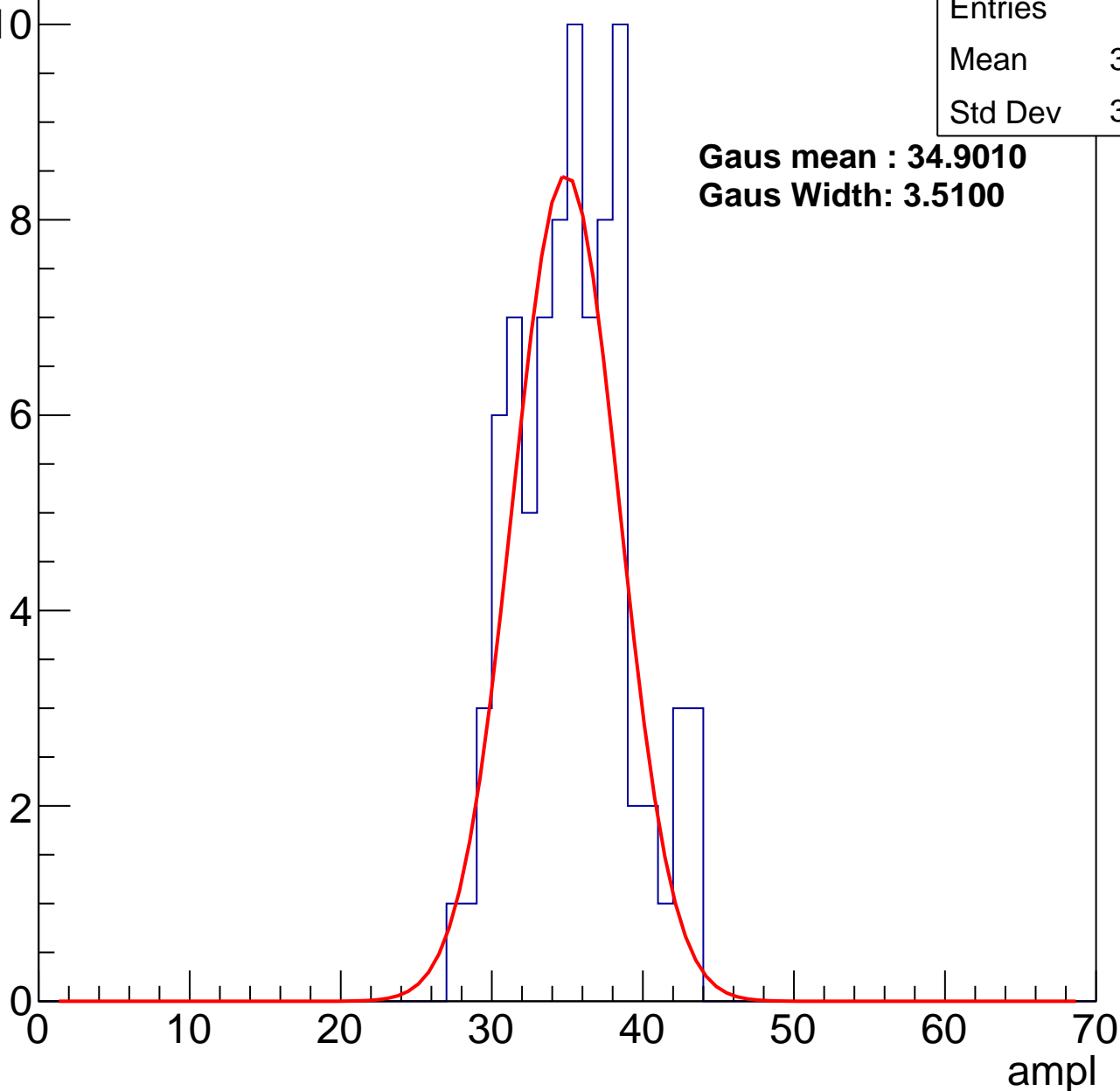
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	84
Mean	34.93
Std Dev	3.699

**Gaus mean : 34.9010**

**Gaus Width: 3.5100**



# B1L102S, U20-ch96, adc2

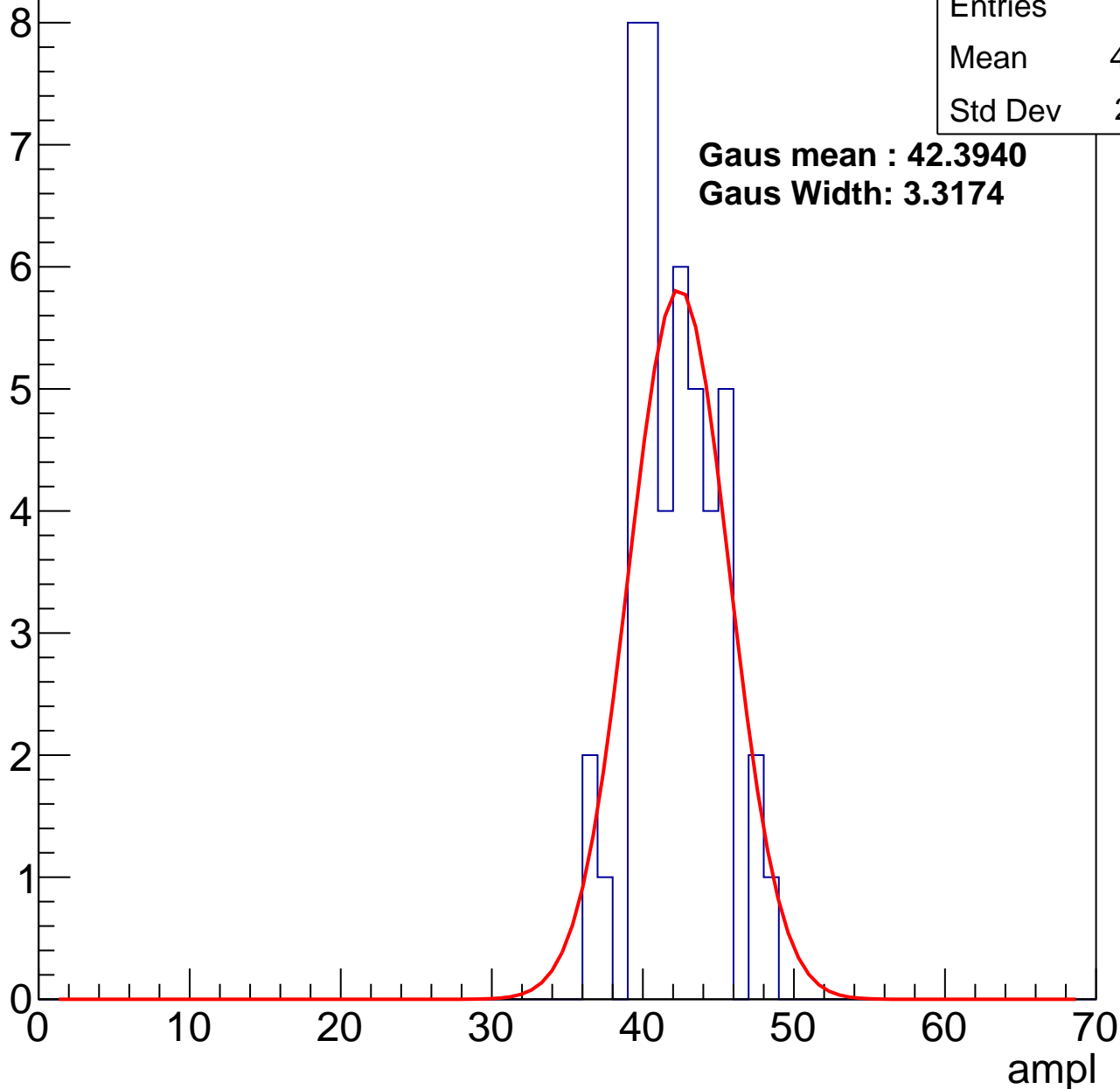
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	46
Mean	41.63
Std Dev	2.761

**Gaus mean : 42.3940**

**Gaus Width: 3.3174**



# B1L102S, U20-ch96, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

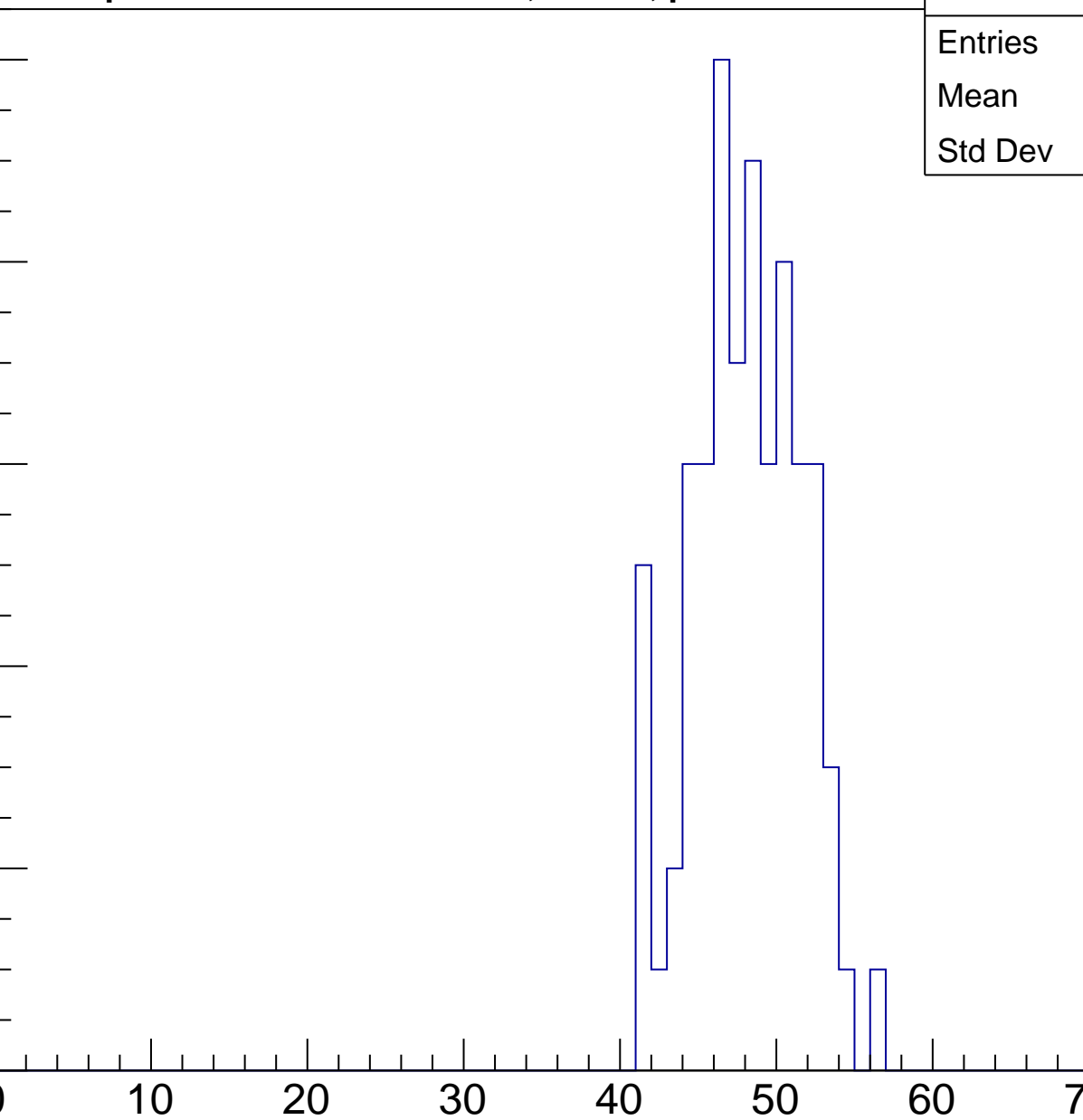
Entries	77
Mean	47.65
Std Dev	3.384

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

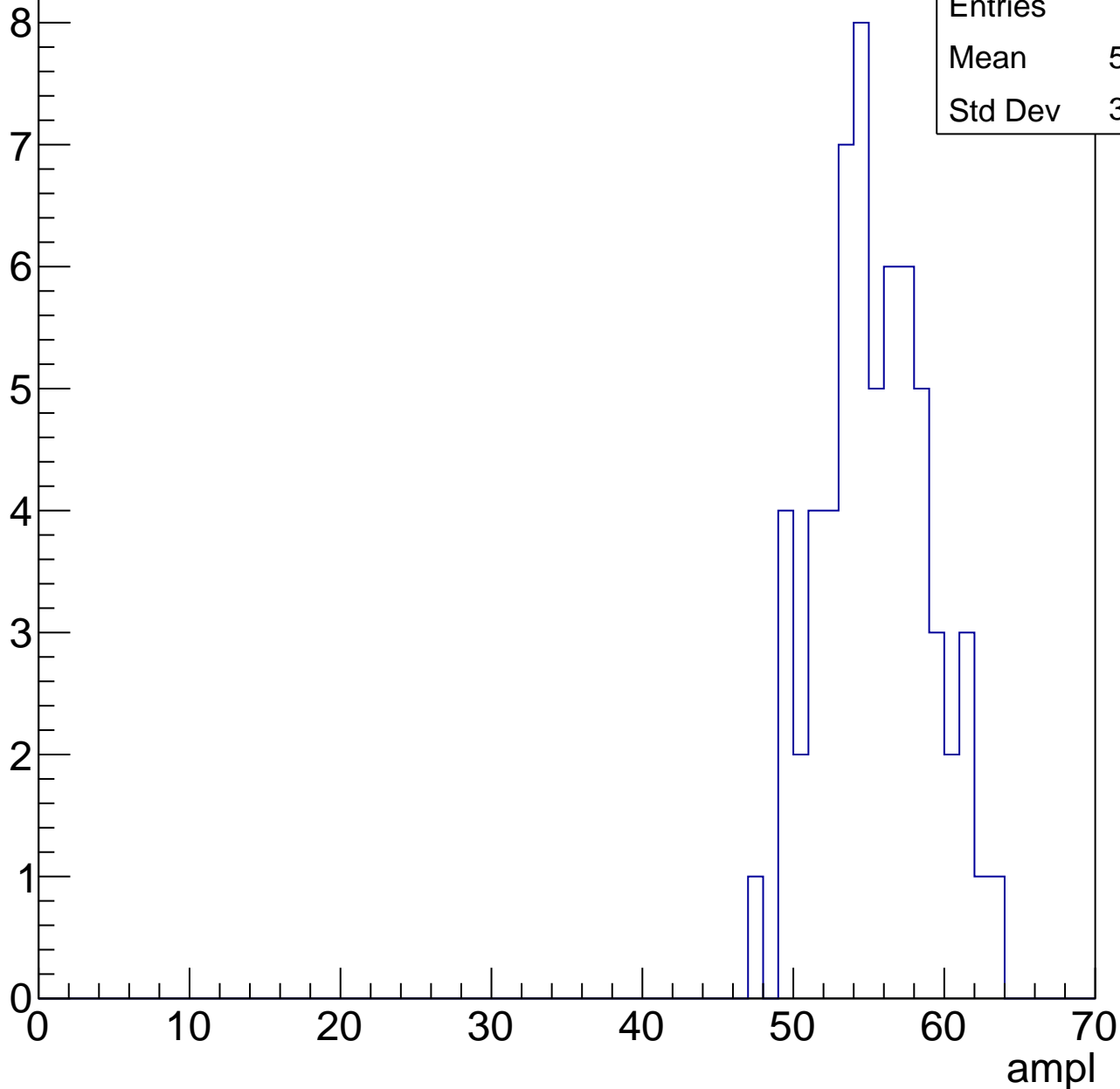


# B1L102S, U20-ch96, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	54.94
Std Dev	3.564

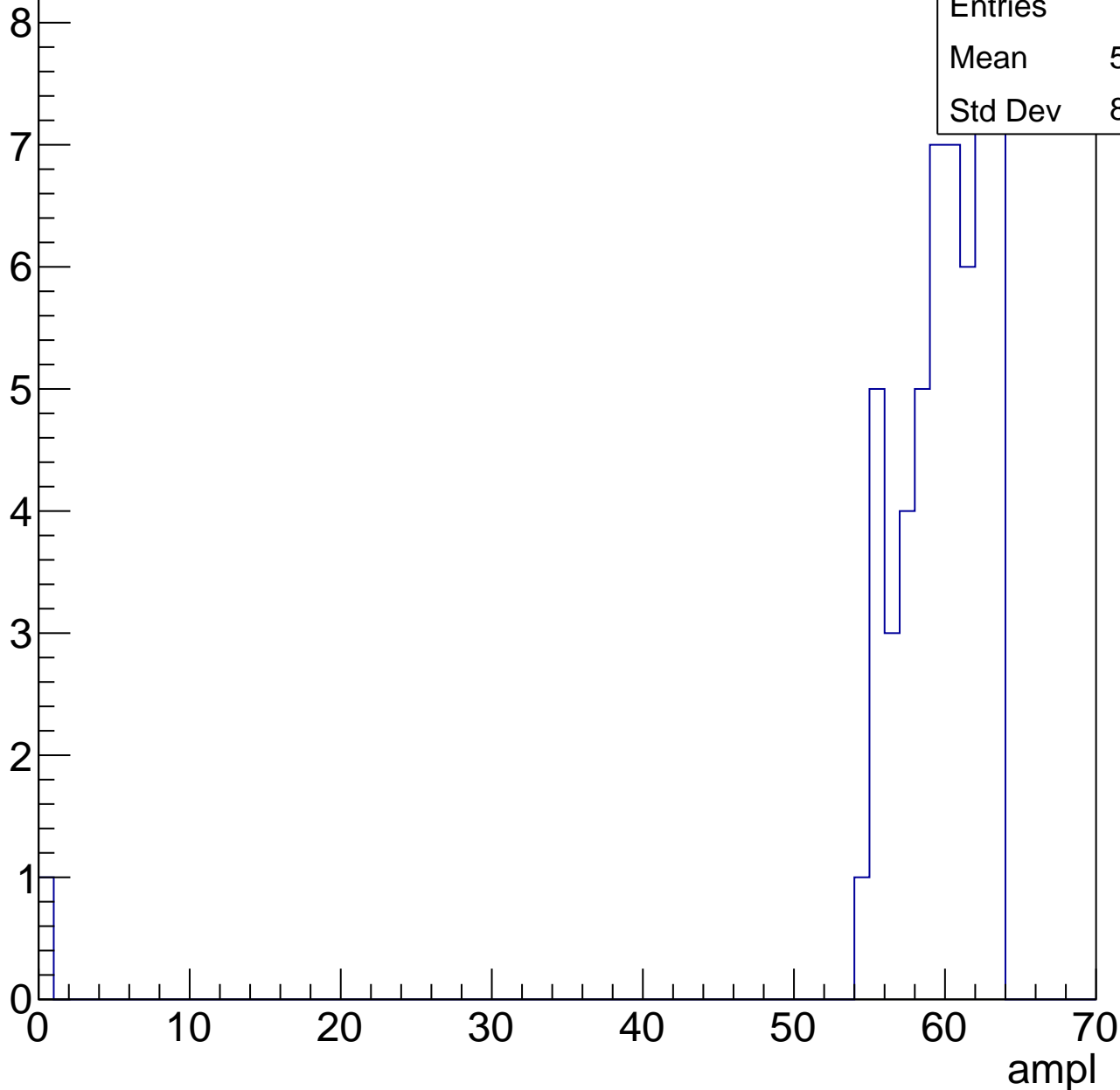


# B1L102S, U20-ch96, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	58.44
Std Dev	8.364



# B1L102S, U20-ch96, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

4

Mean

61.5

Std Dev

1.118



# B1L102S, U20-ch96, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U20-ch97, adc0

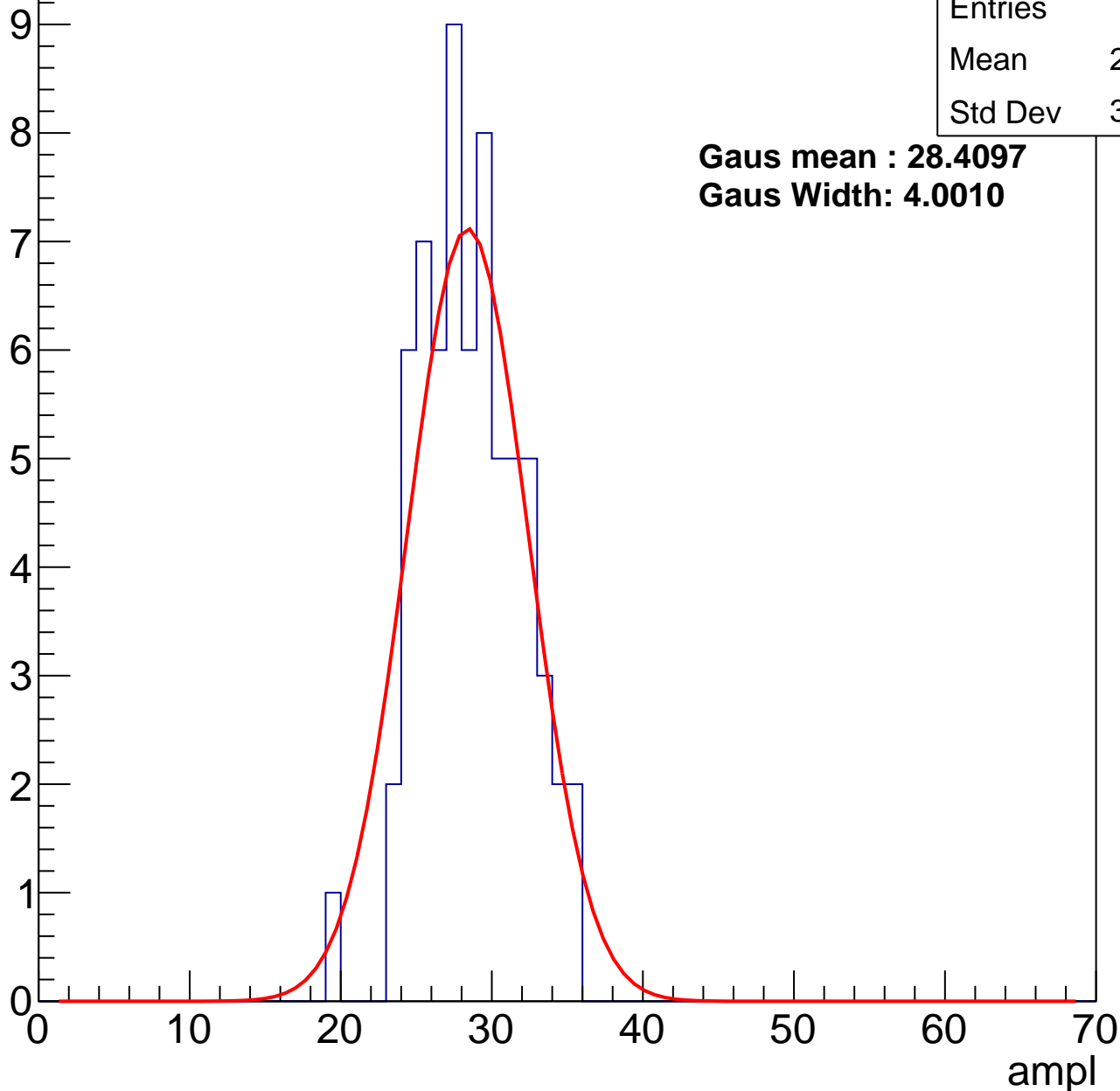
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	28.13
Std Dev	3.278

**Gaus mean : 28.4097**

**Gaus Width: 4.0010**



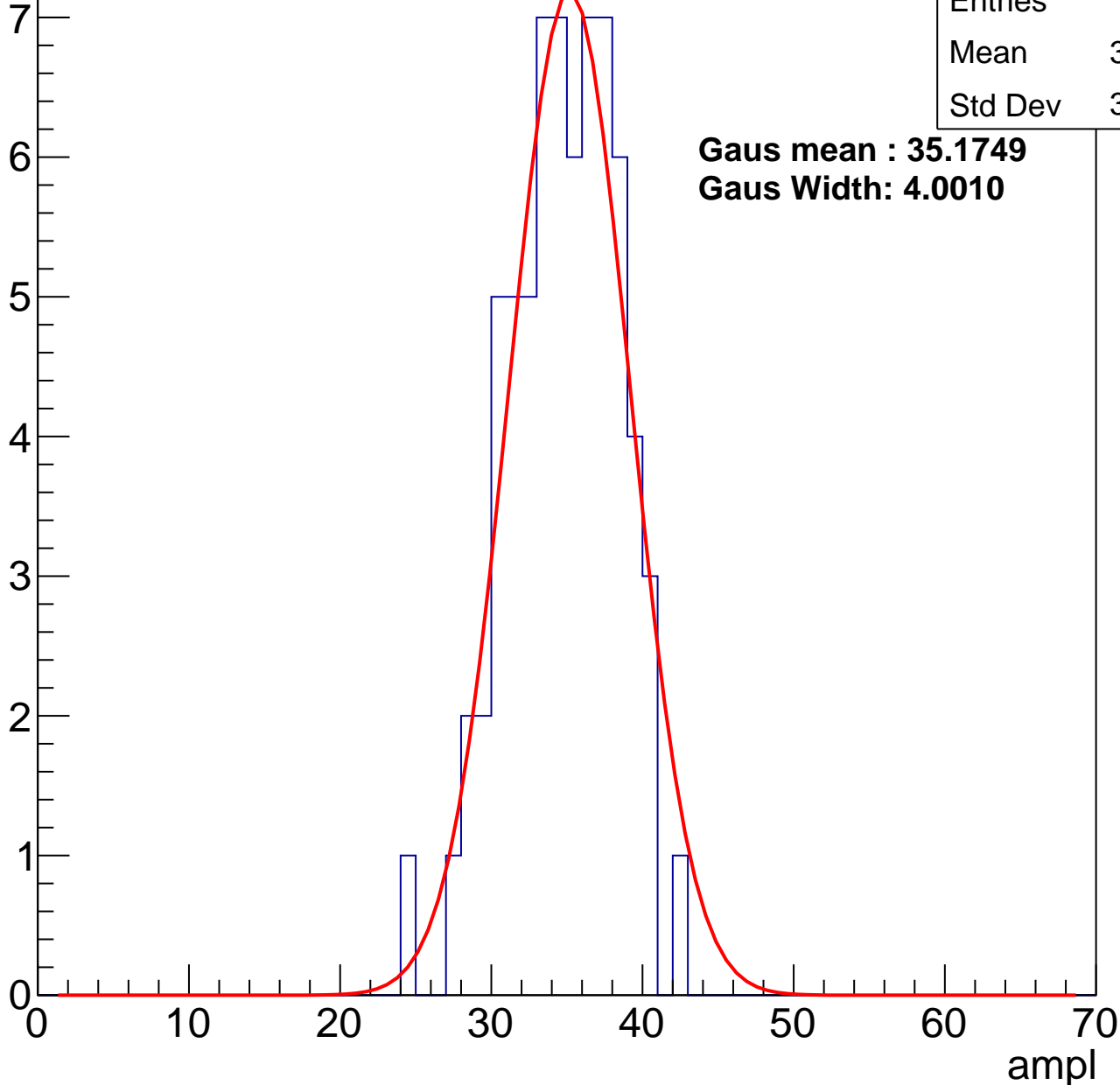
# B1L102S, U20-ch97, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	34.29
Std Dev	3.576

**Gaus mean : 35.1749**  
**Gaus Width: 4.0010**



# B1L102S, U20-ch97, adc2

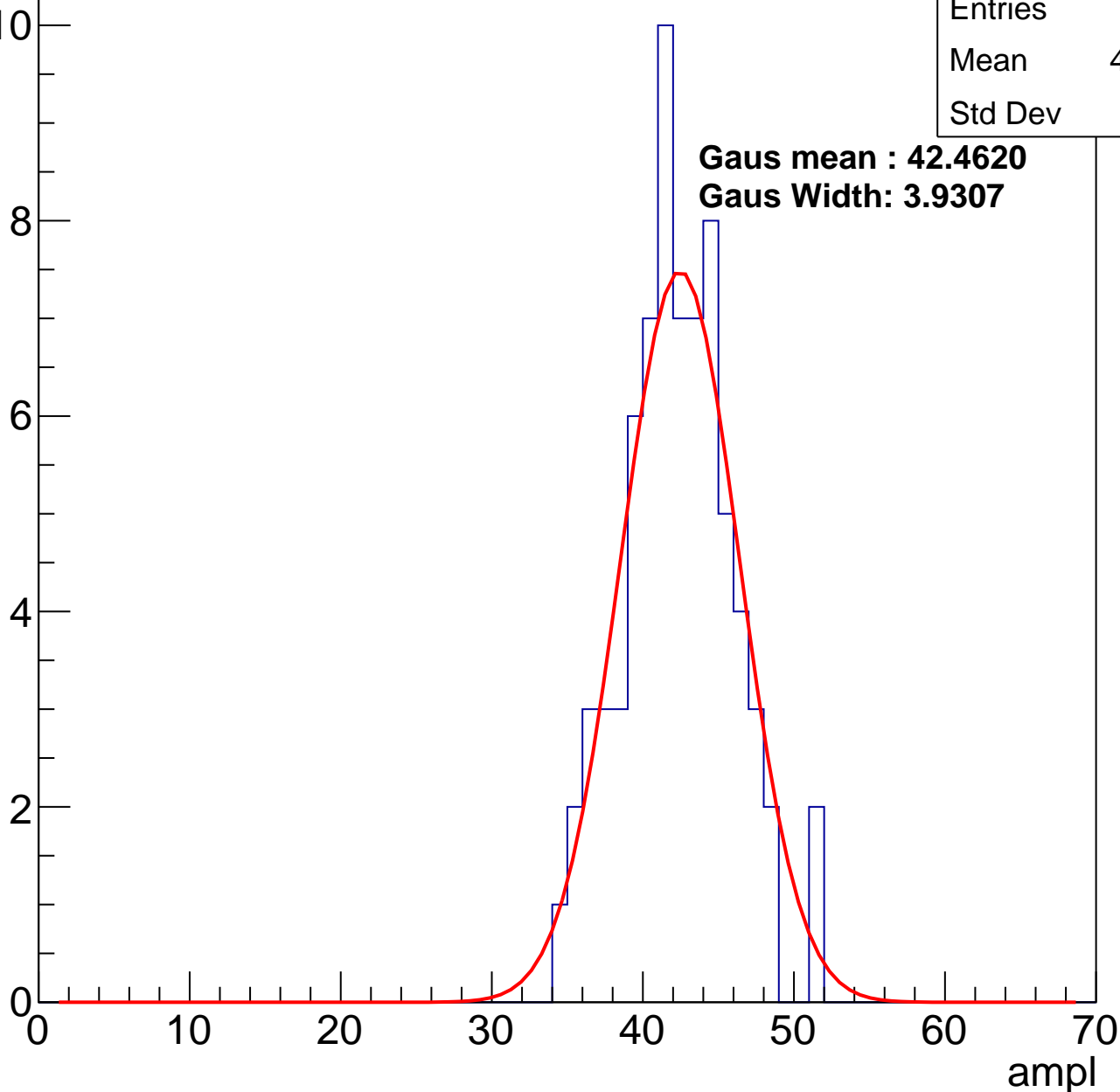
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	41.86
Std Dev	3.59

**Gaus mean : 42.4620**

**Gaus Width: 3.9307**

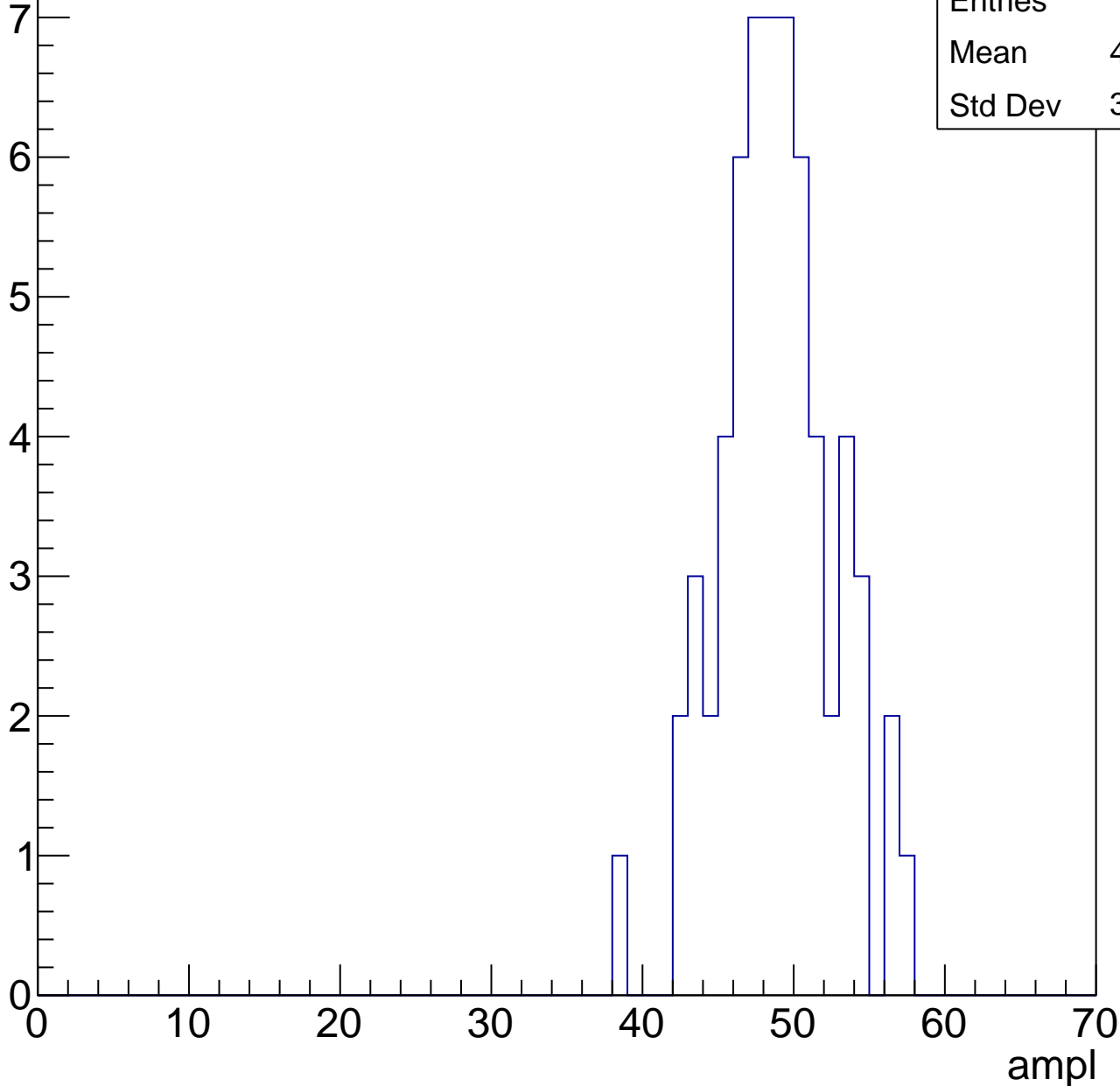


# B1L102S, U20-ch97, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	48.43
Std Dev	3.735

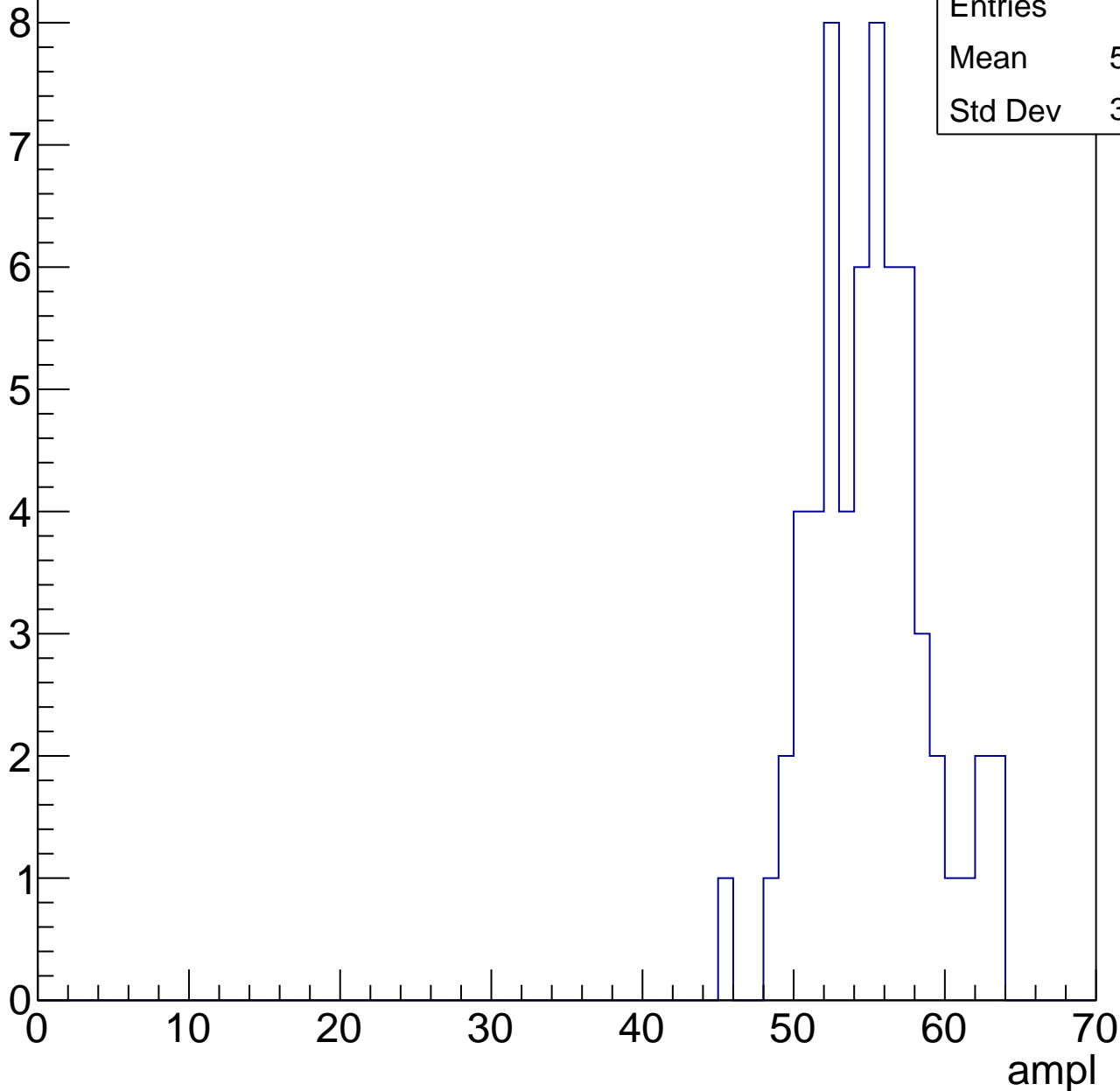


# B1L102S, U20-ch97, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

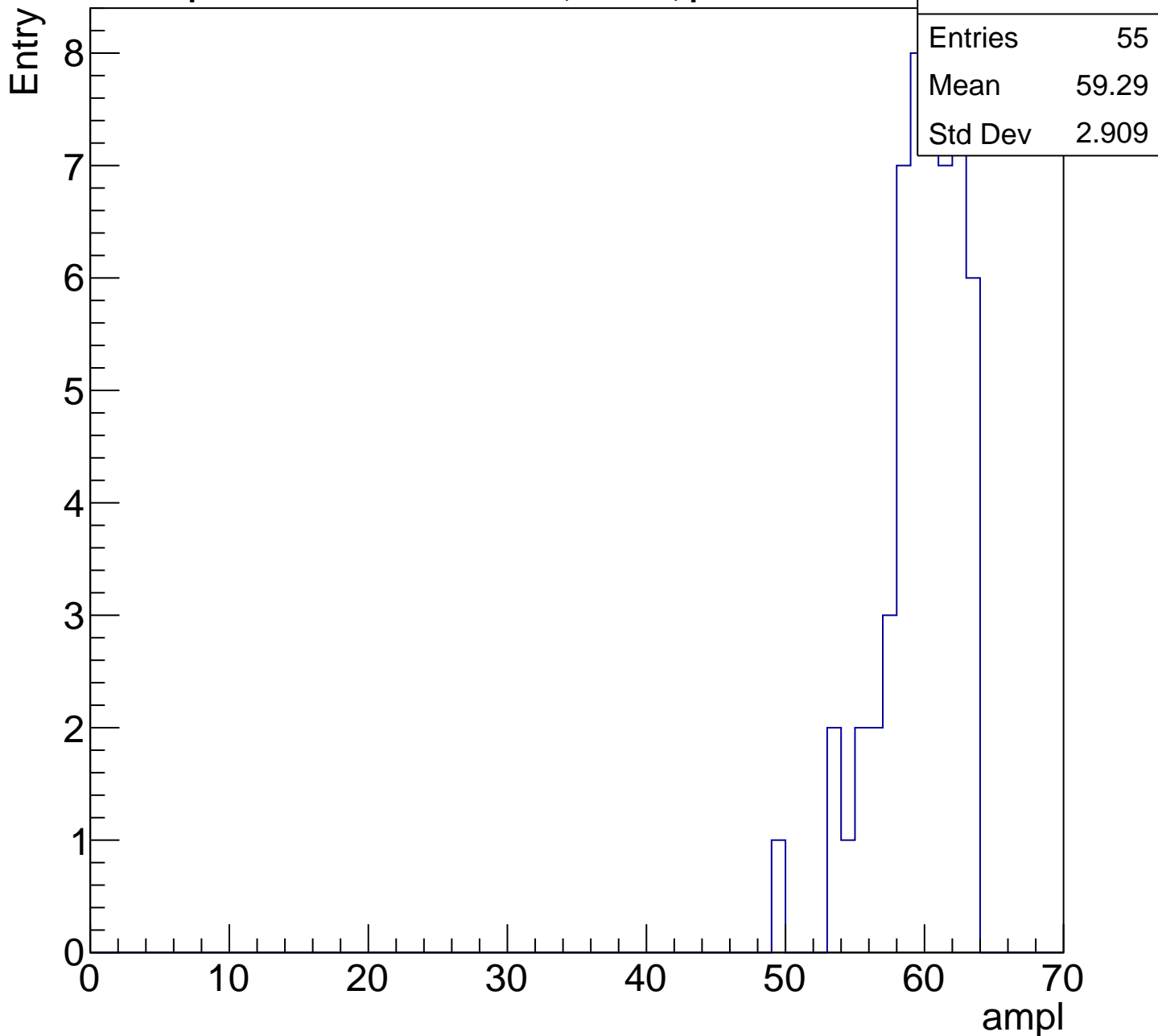
Entry

Entries	61
Mean	54.56
Std Dev	3.718



# B1L102S, U20-ch97, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2



# B1L102S, U20-ch97, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

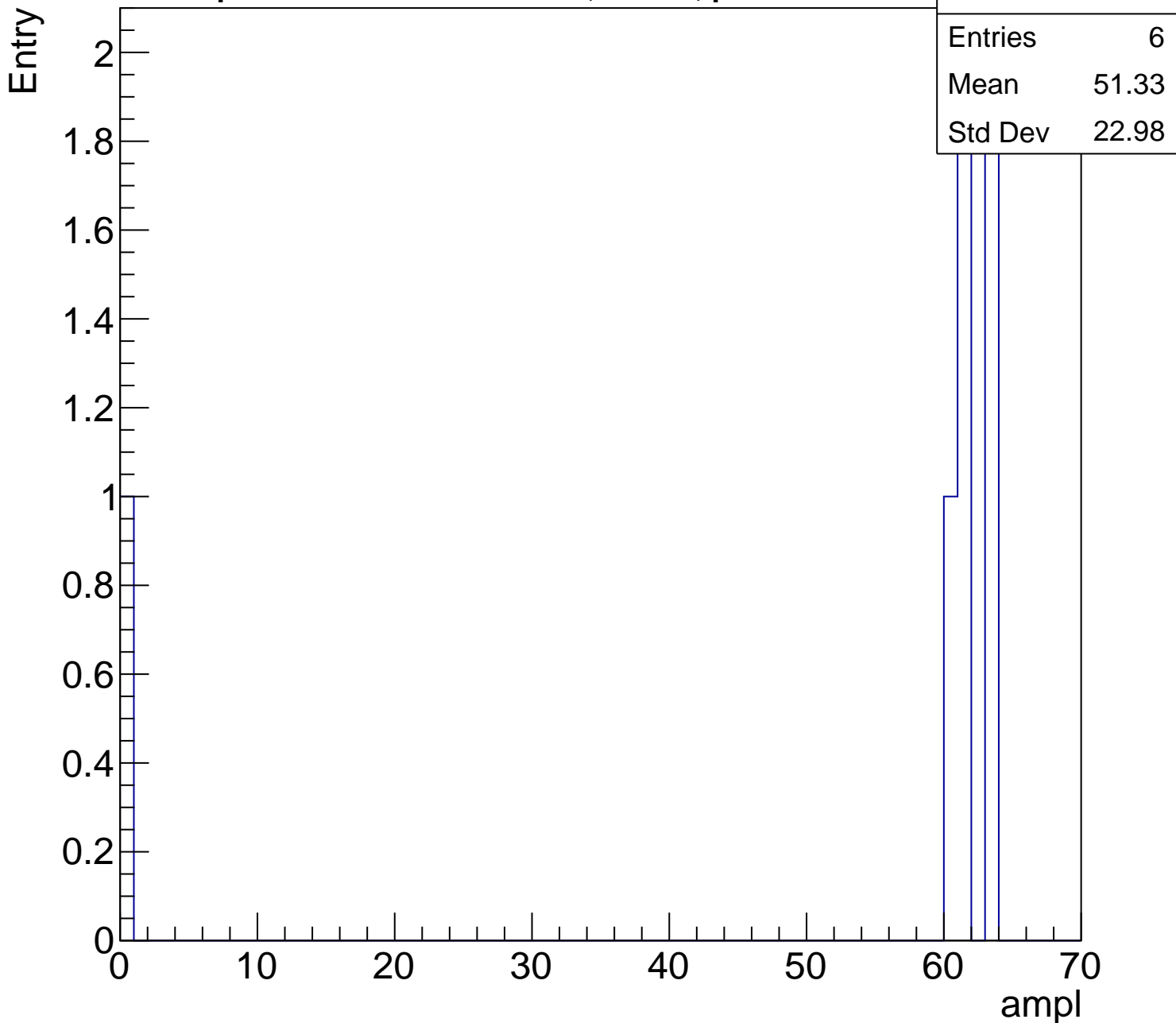
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	51.33
Std Dev	22.98

0 10 20 30 40 50 60 70

ampl





# B1L102S, U20-ch97, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U20-ch98, adc0

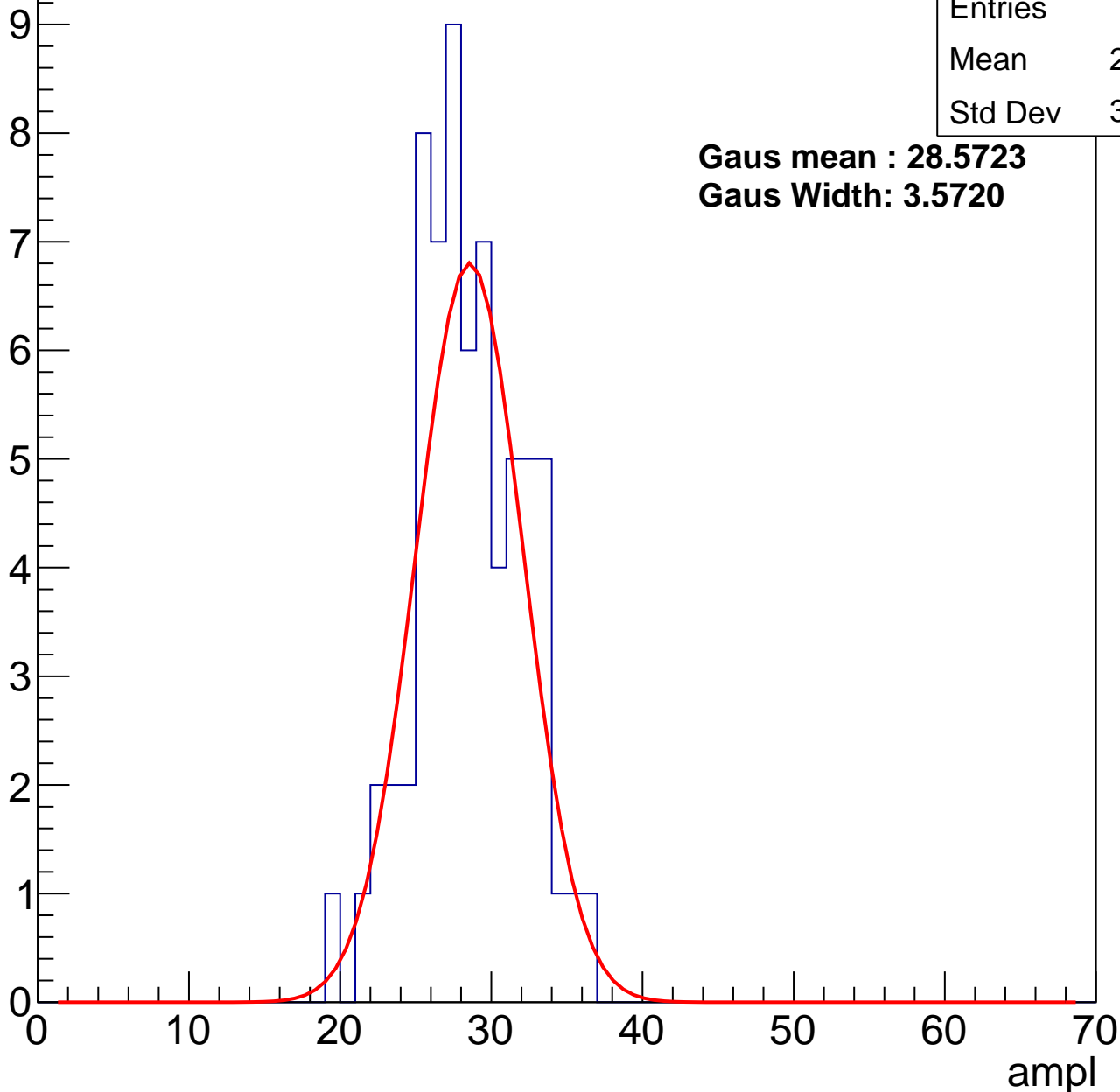
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	28.04
Std Dev	3.487

**Gaus mean : 28.5723**

**Gaus Width: 3.5720**



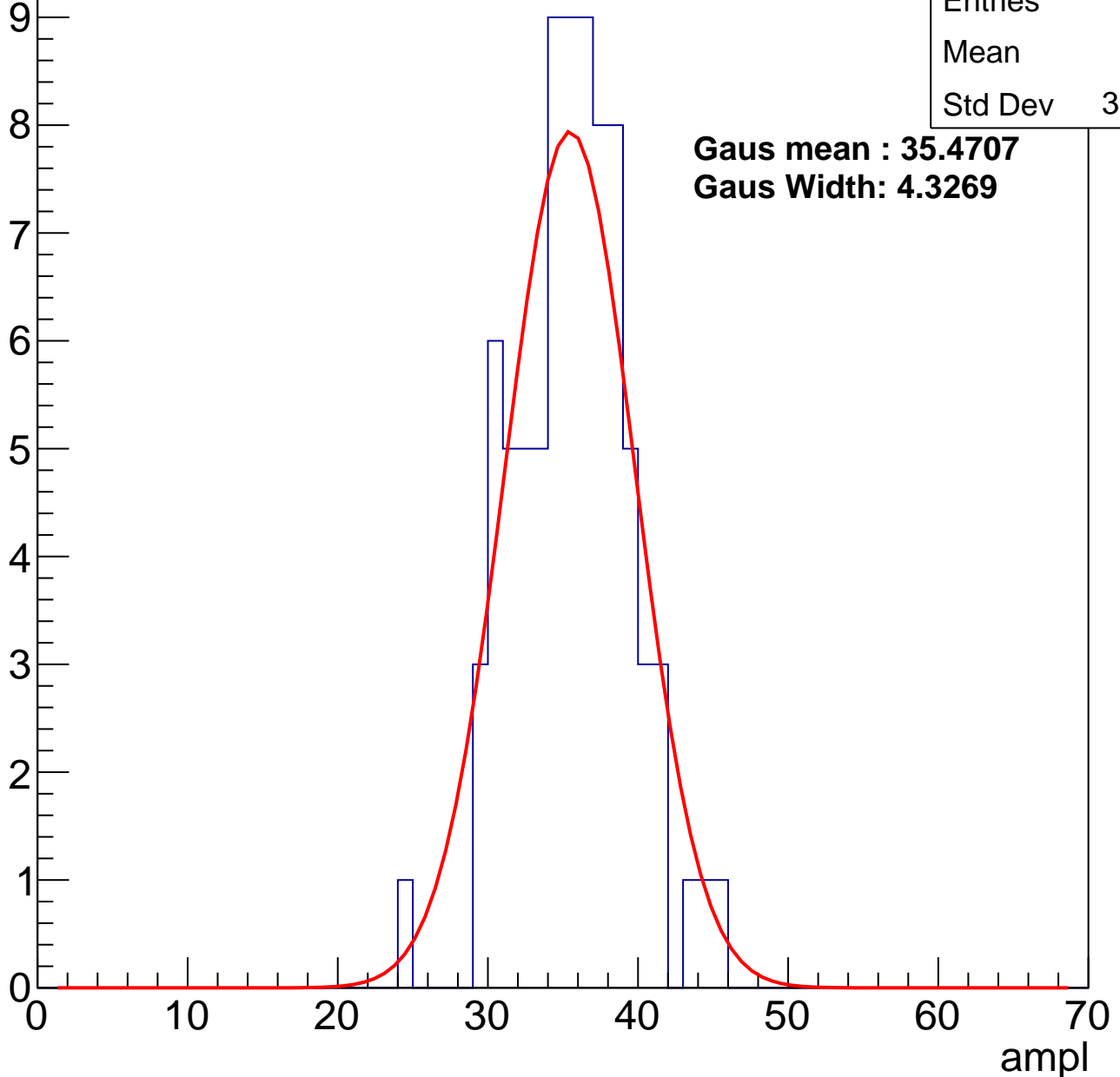
# B1L102S, U20-ch98, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	82
Mean	35.2
Std Dev	3.746

**Gaus mean : 35.4707**  
**Gaus Width: 4.3269**



# B1L102S, U20-ch98, adc2

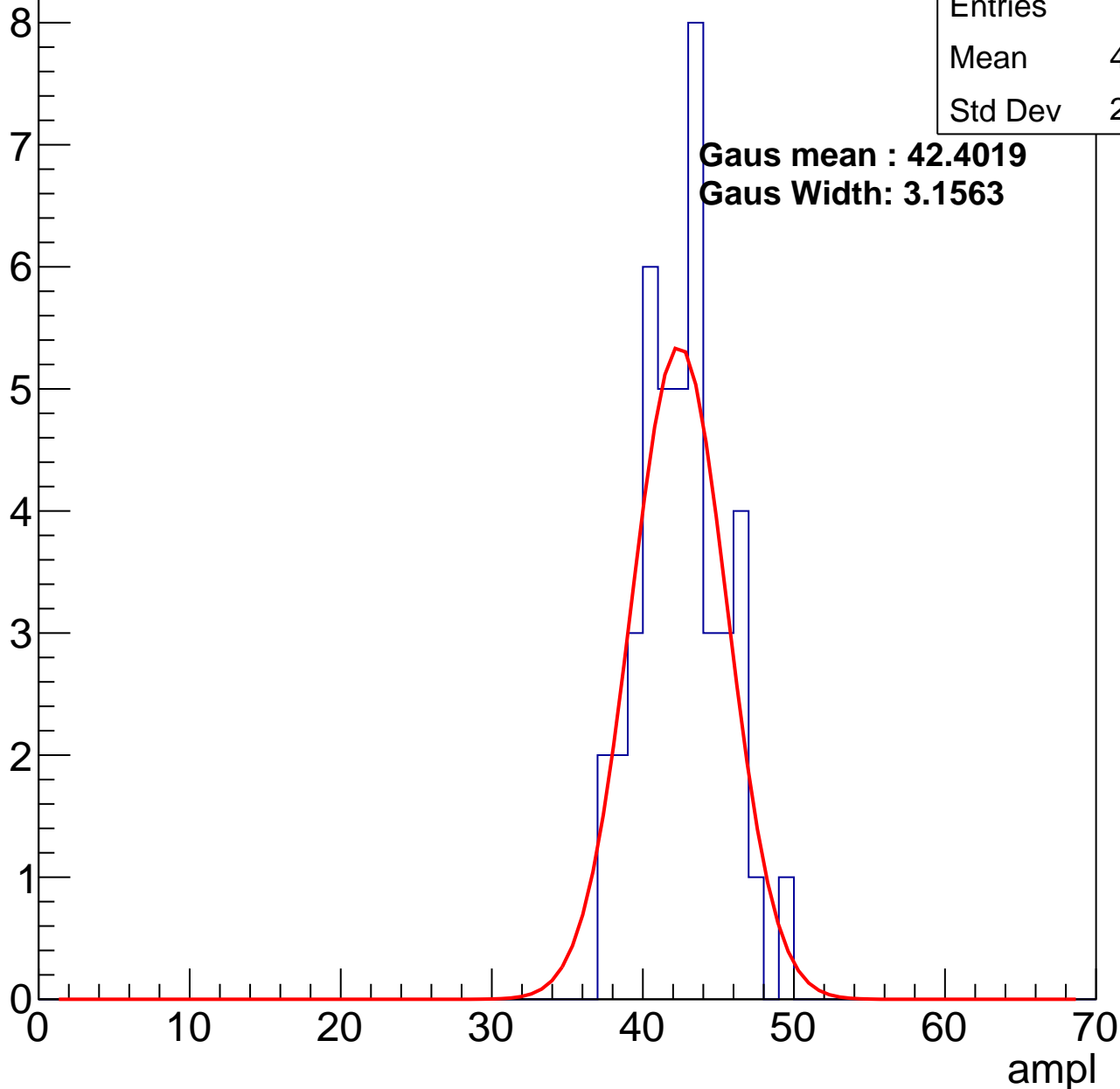
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	43
Mean	42.16
Std Dev	2.736

**Gaus mean : 42.4019**

**Gaus Width: 3.1563**

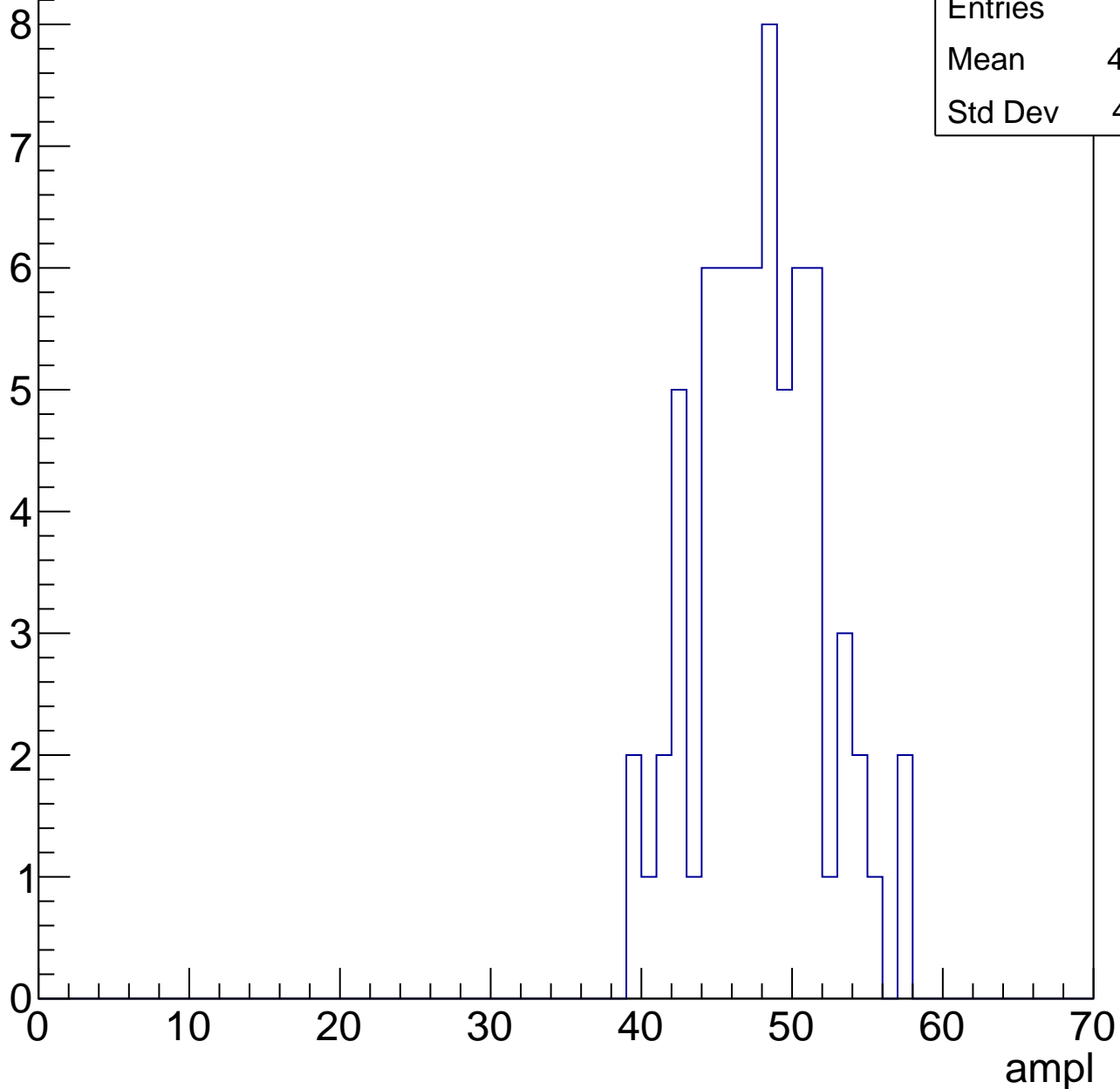


# B1L102S, U20-ch98, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	47.36
Std Dev	4.061

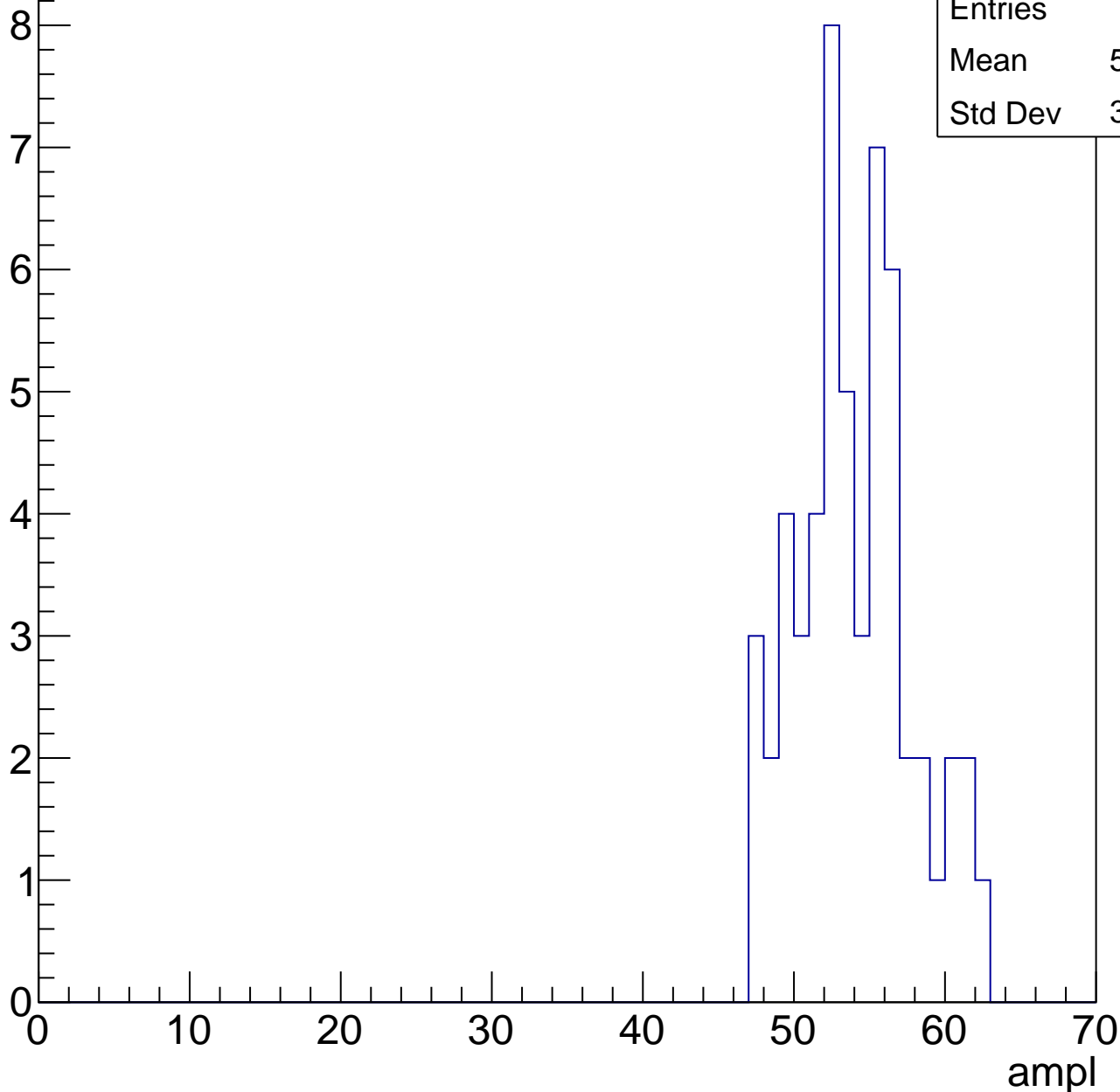


# B1L102S, U20-ch98, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	53.53
Std Dev	3.736



# B1L102S, U20-ch98, adc5

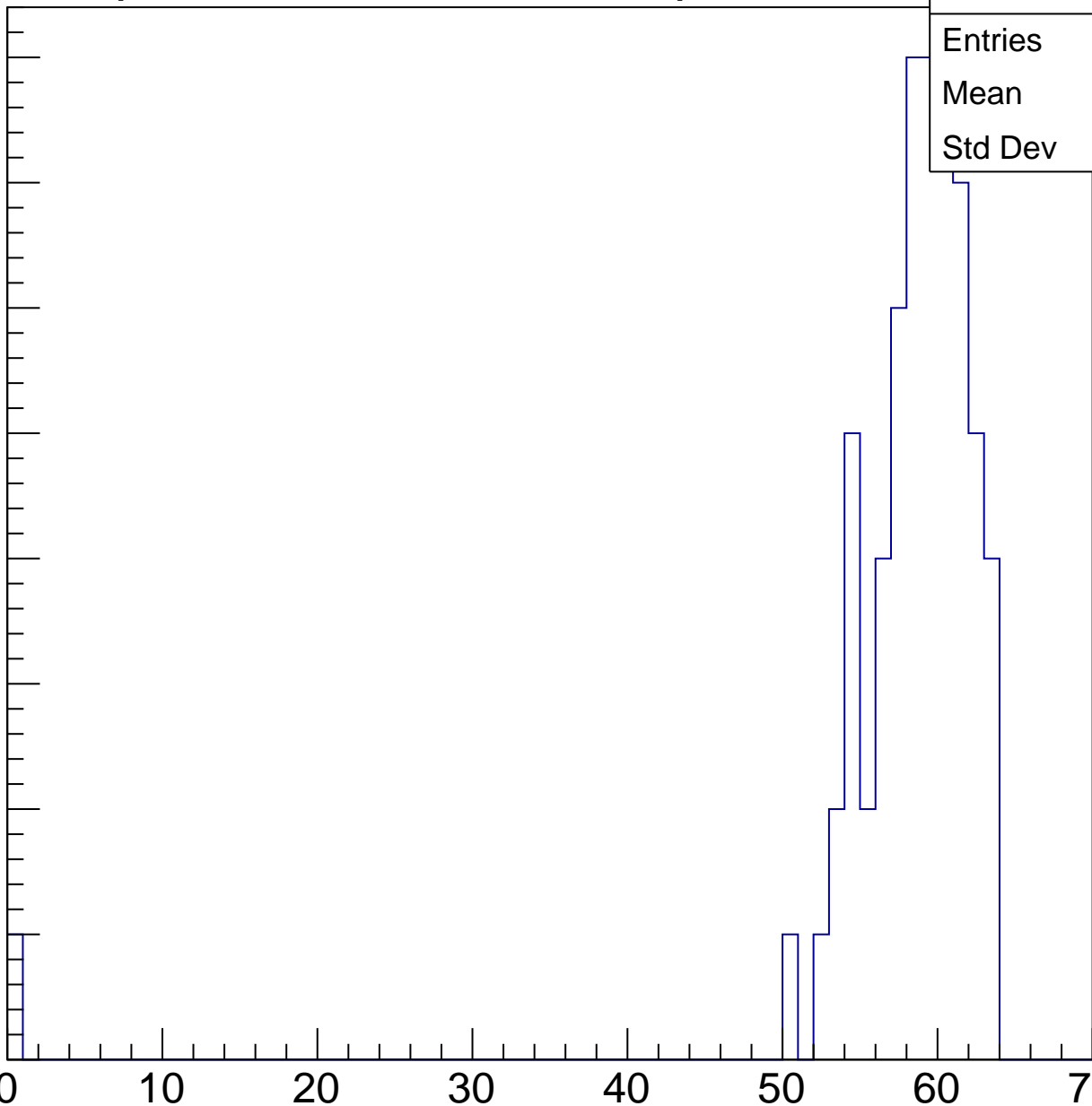
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	62
Mean	57.4
Std Dev	7.926

ampl

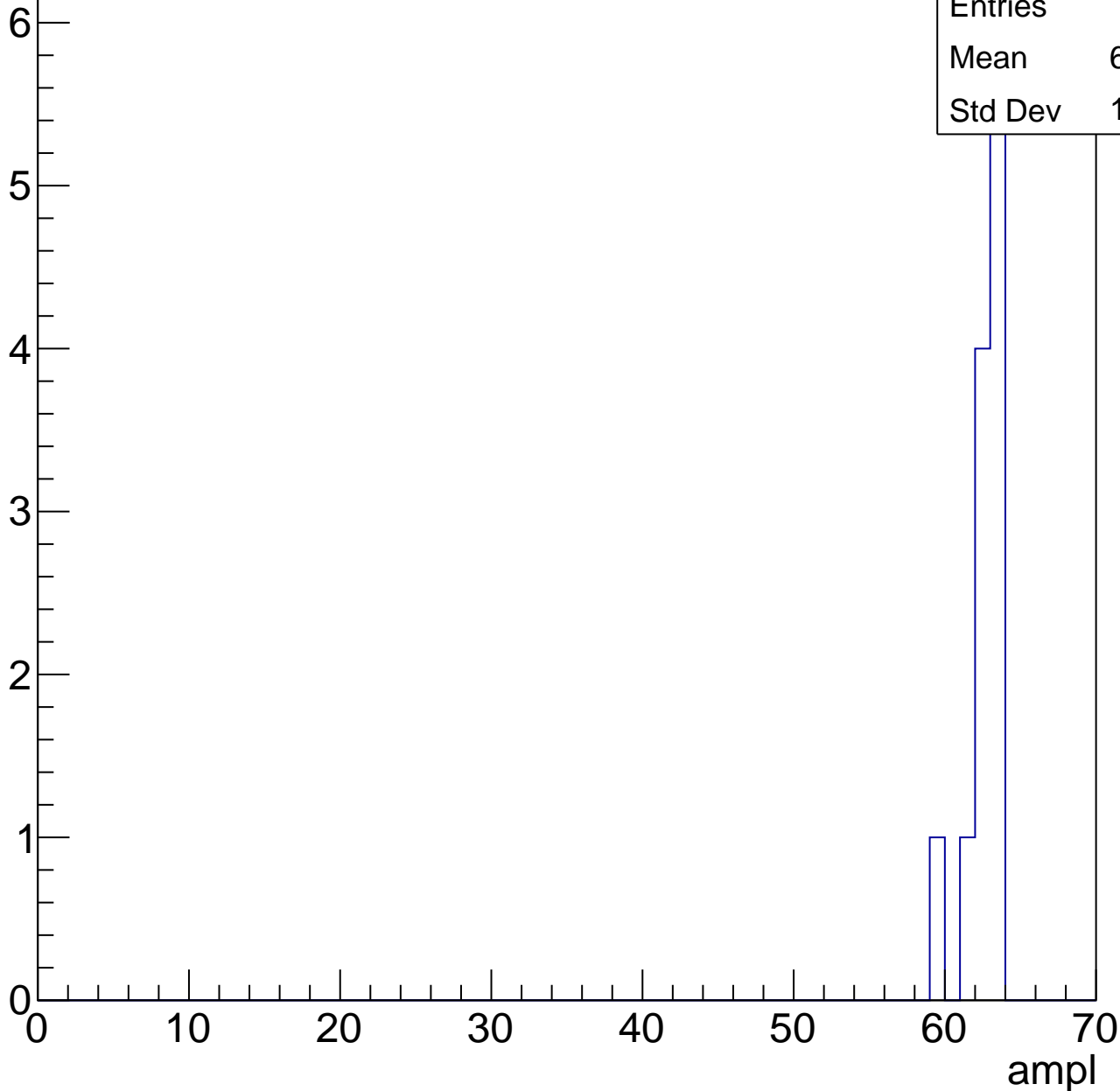


# B1L102S, U20-ch98, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	12
Mean	62.17
Std Dev	1.143





# B1L102S, U20-ch98, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch99, adc0

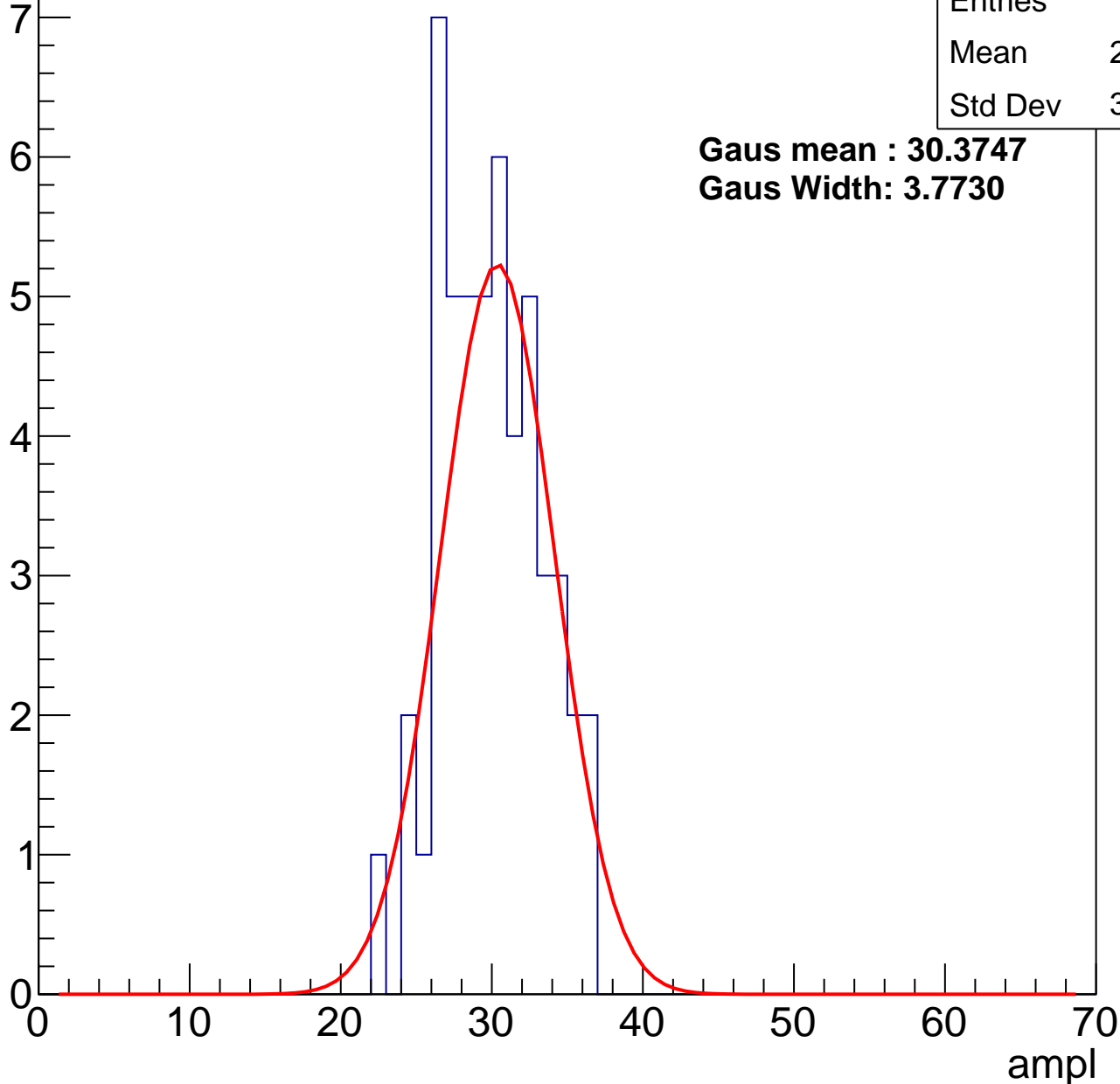
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	29.49
Std Dev	3.286

**Gaus mean : 30.3747**

**Gaus Width: 3.7730**



# B1L102S, U20-ch99, adc1

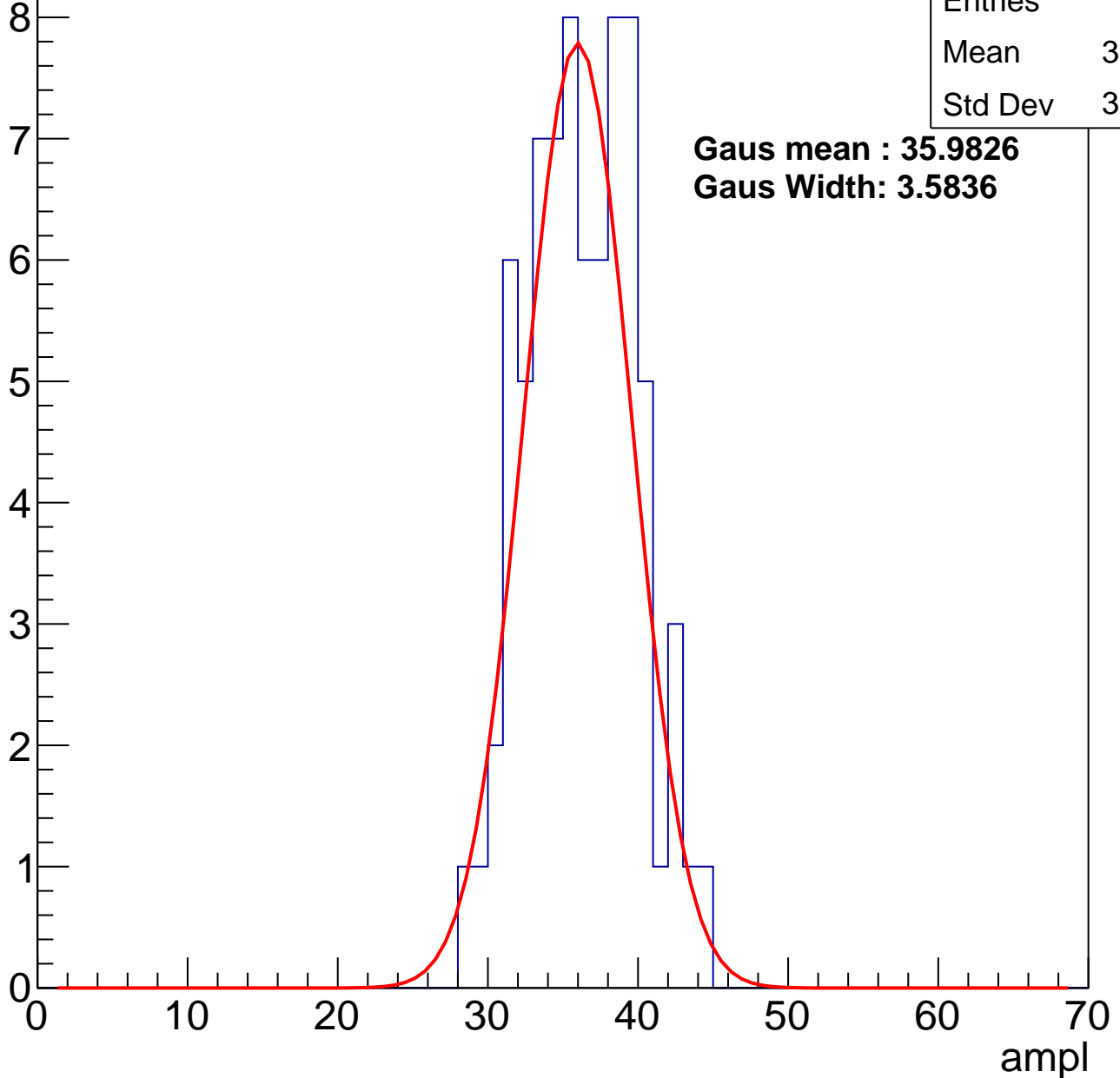
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	35.79
Std Dev	3.529

**Gaus mean : 35.9826**

**Gaus Width: 3.5836**



# B1L102S, U20-ch99, adc2

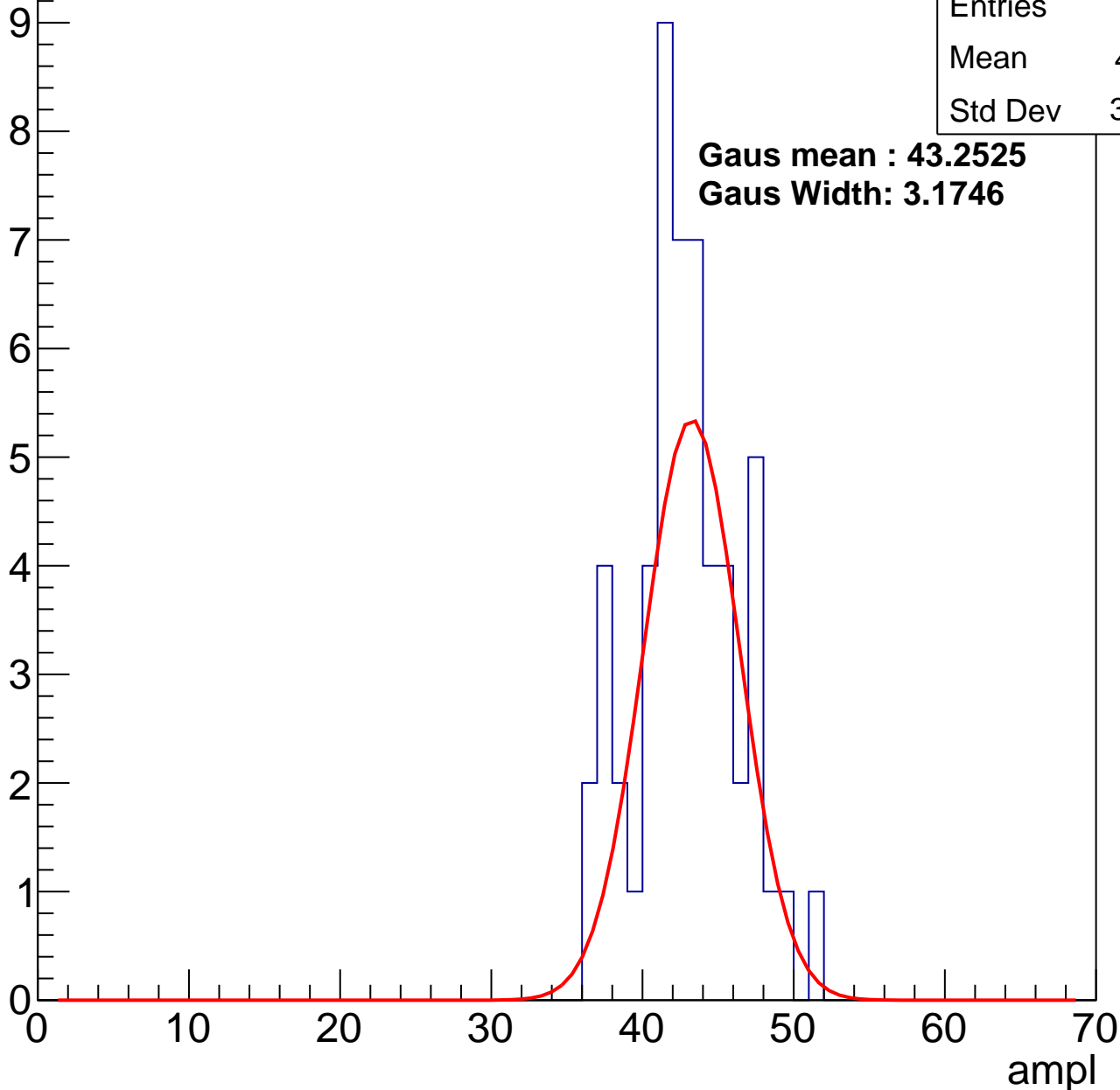
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	42.41
Std Dev	3.364

**Gaus mean : 43.2525**

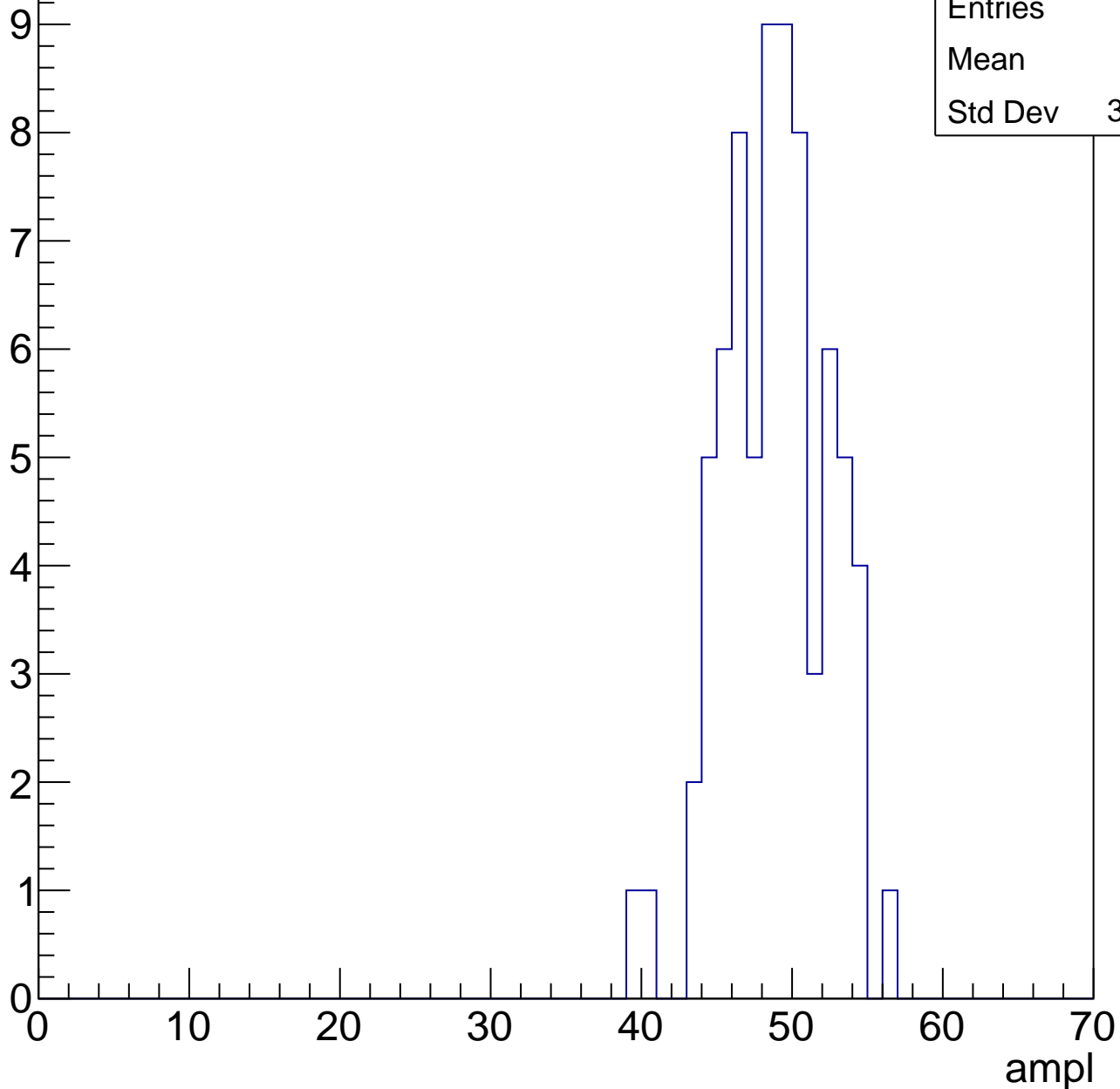
**Gaus Width: 3.1746**



# B1L102S, U20-ch99, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



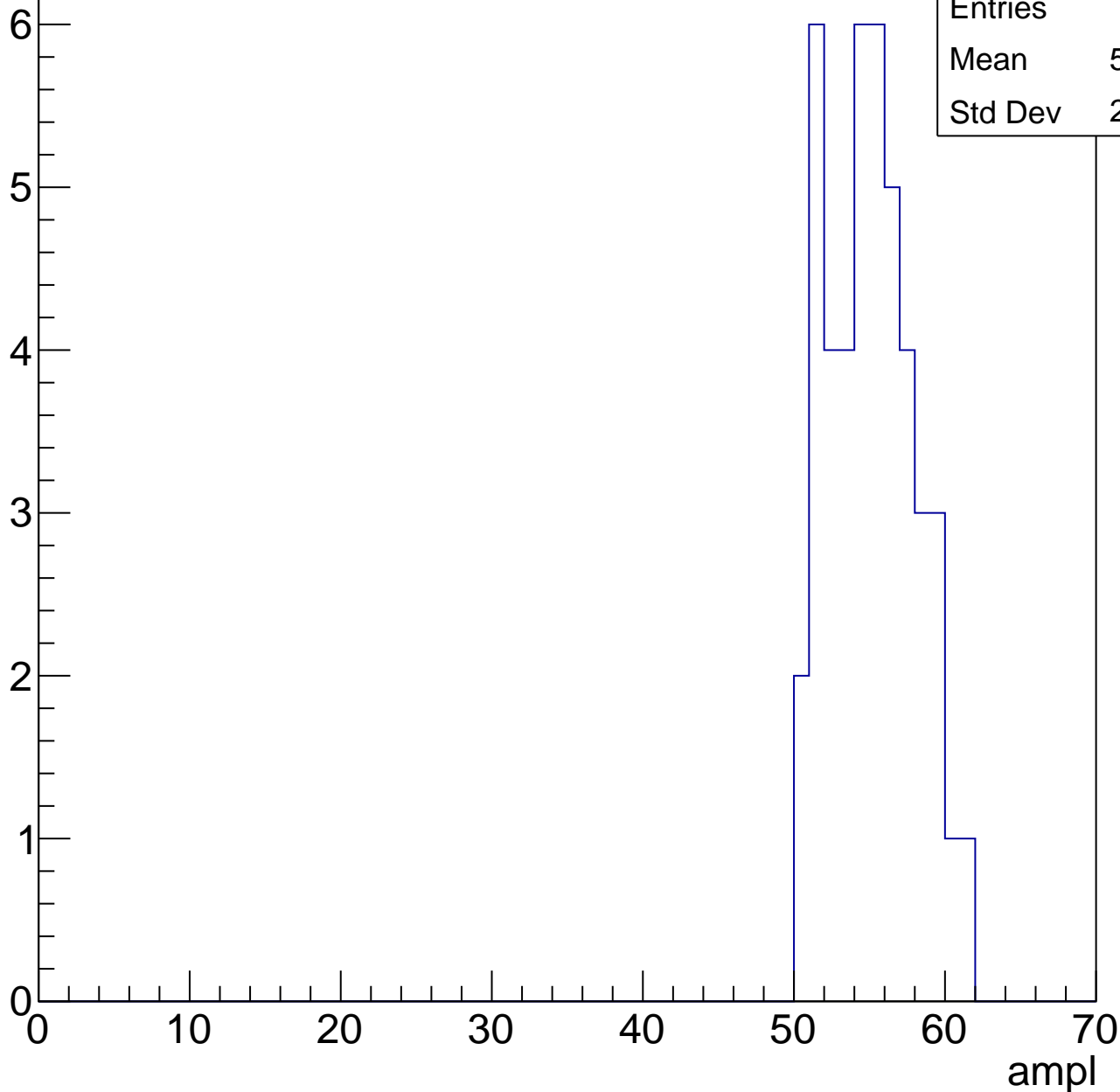
Entries	73
Mean	48.4
Std Dev	3.415

# B1L102S, U20-ch99, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

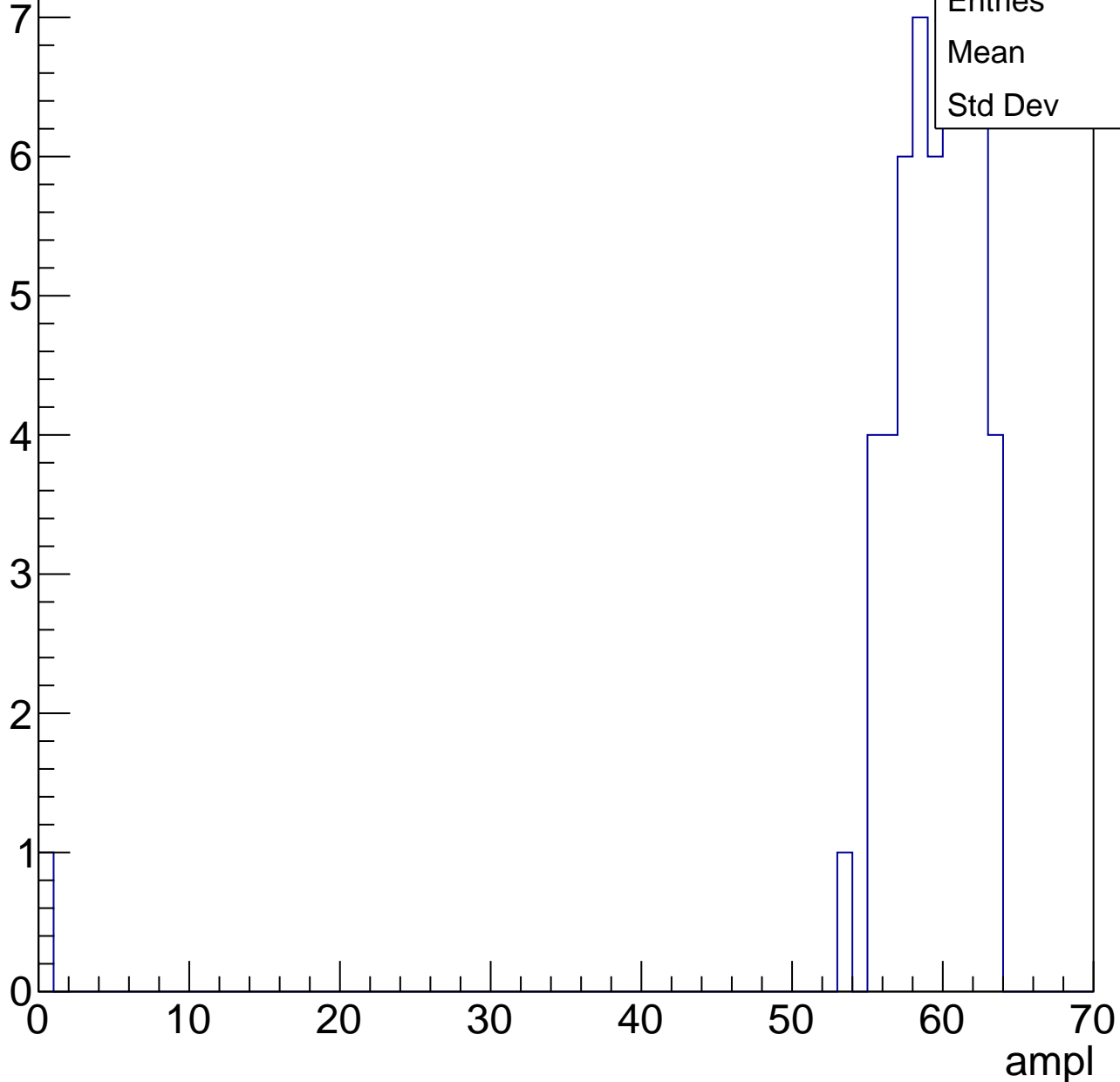
Entries	45
Mean	54.67
Std Dev	2.813



# B1L102S, U20-ch99, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

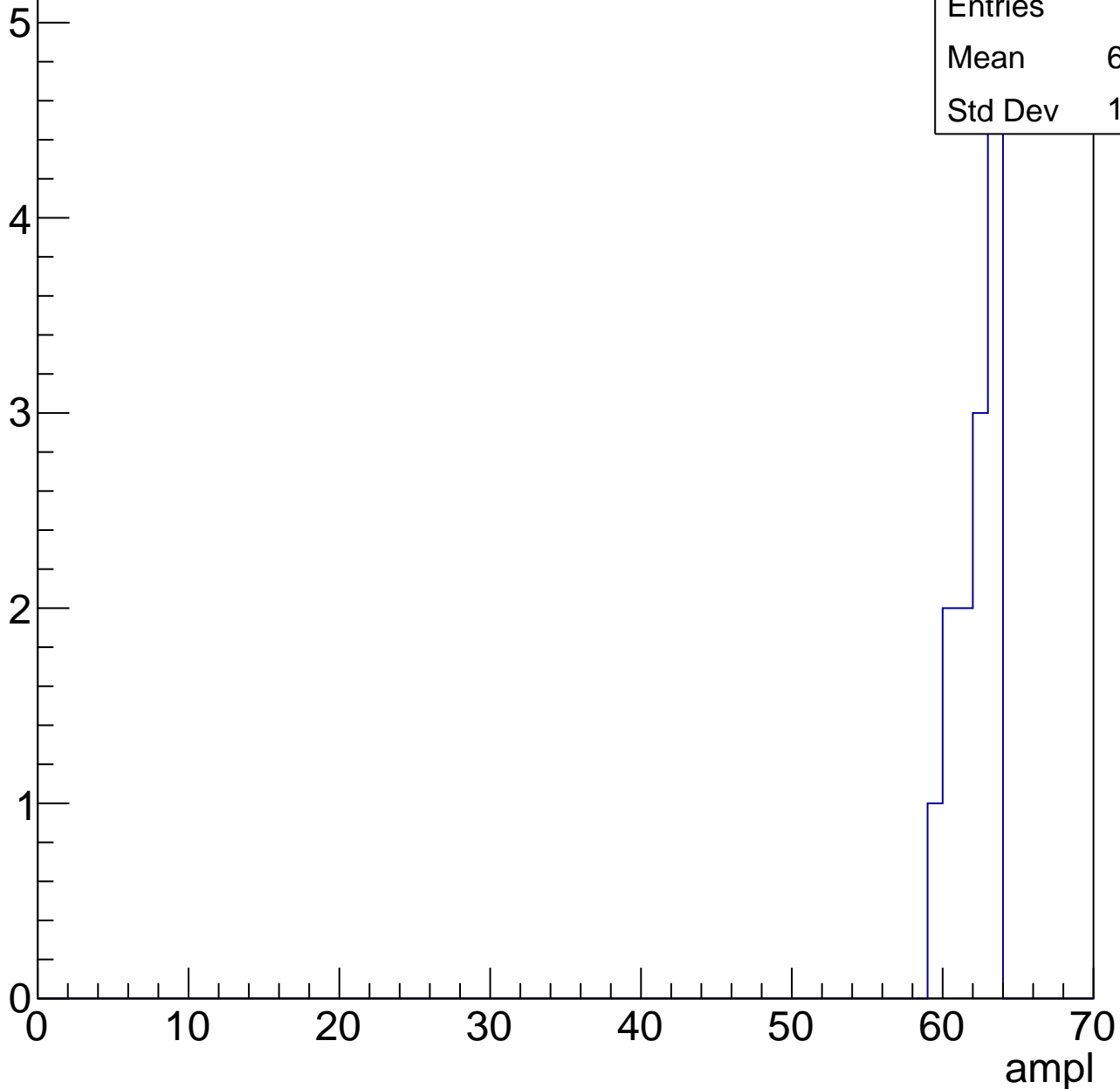


# B1L102S, U20-ch99, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	13
Mean	61.69
Std Dev	1.323





# B1L102S, U20-ch99, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	3
Mean	28.33
Std Dev	26.11

# B1L102S, U20-ch100, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	74
Mean	25.24
Std Dev	6.109

**Gaus mean : 26.7922**

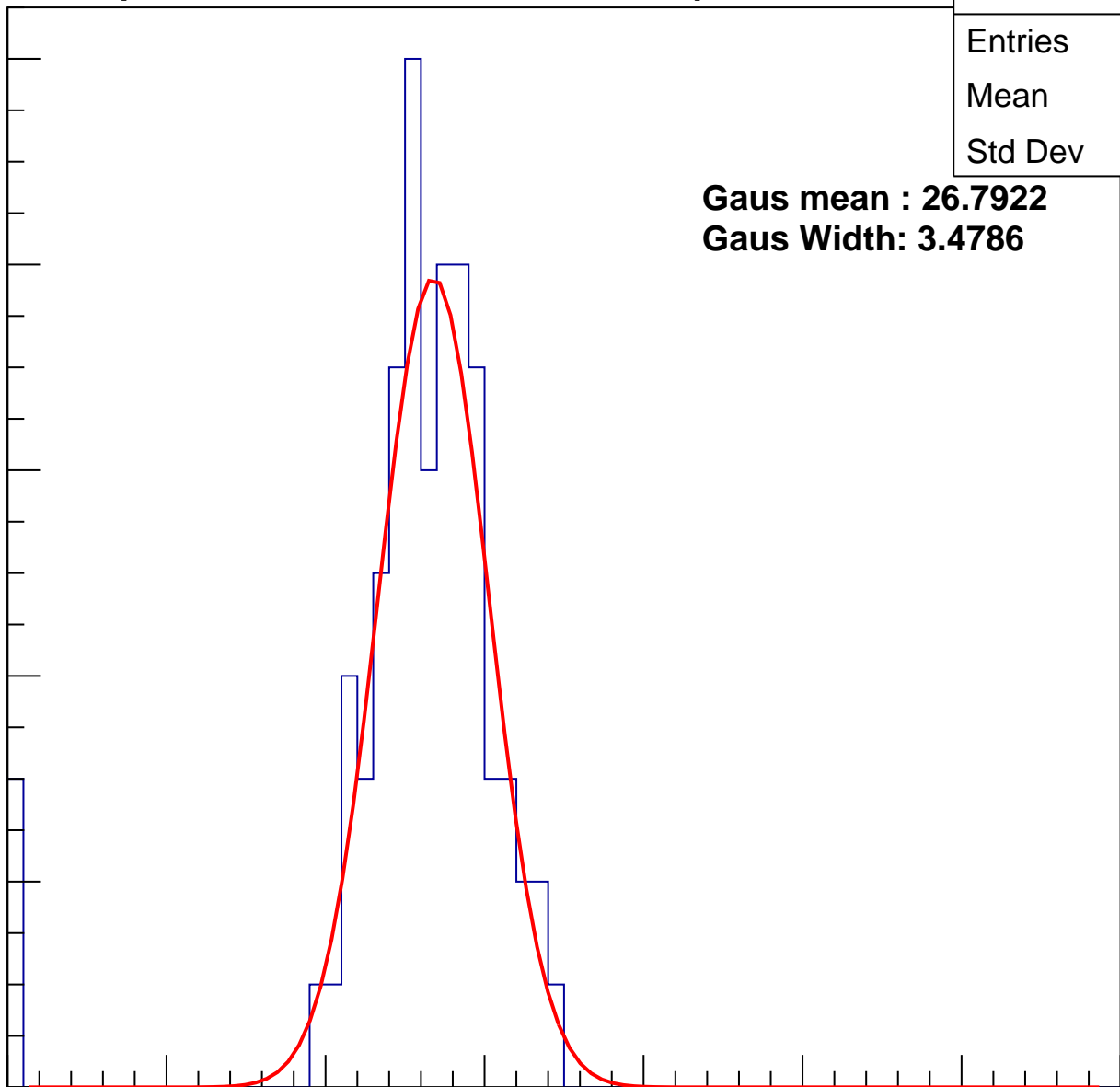
**Gaus Width: 3.4786**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U20-ch100, adc1

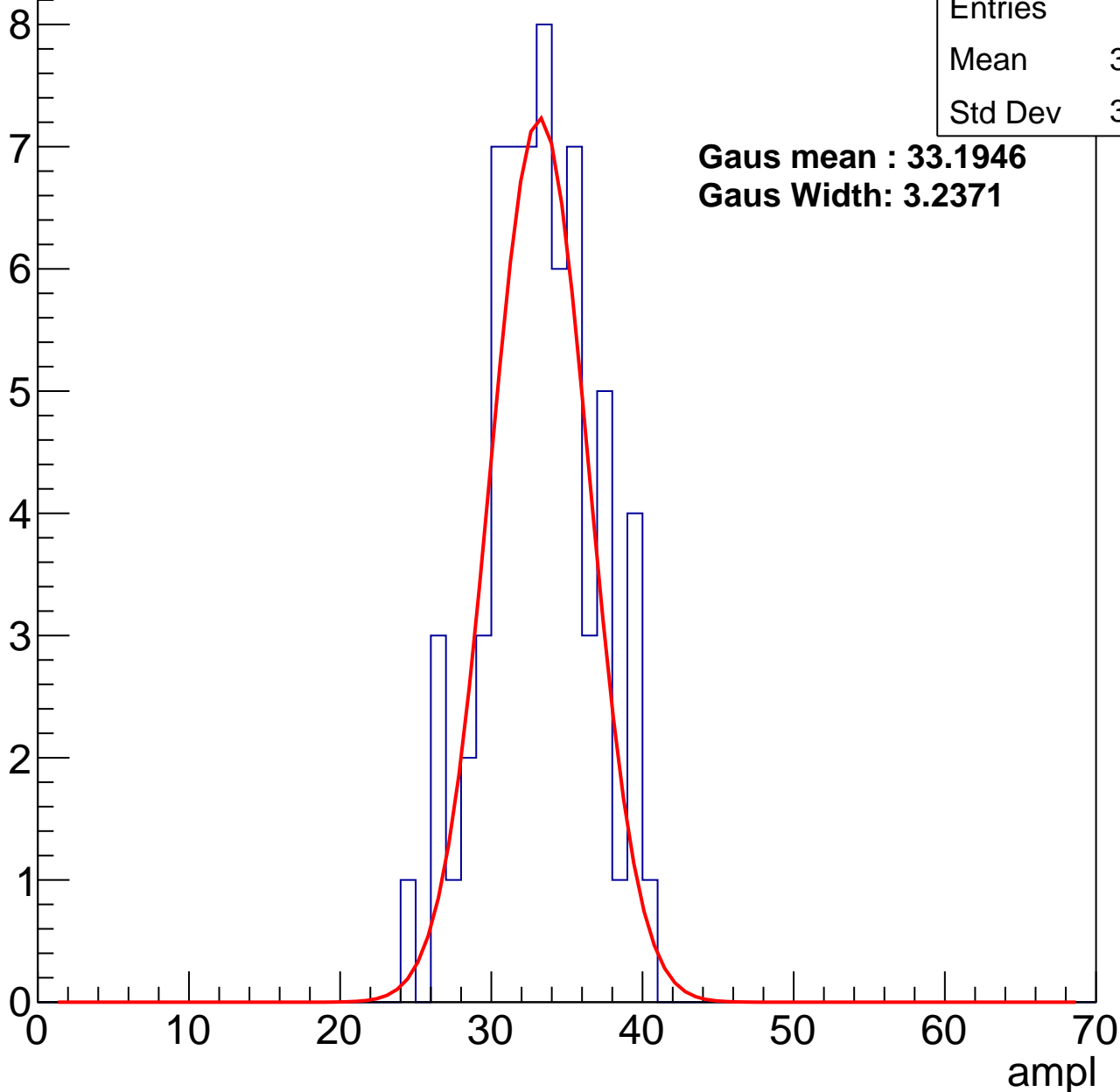
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	32.77
Std Dev	3.515

**Gaus mean : 33.1946**

**Gaus Width: 3.2371**



# B1L102S, U20-ch100, adc2

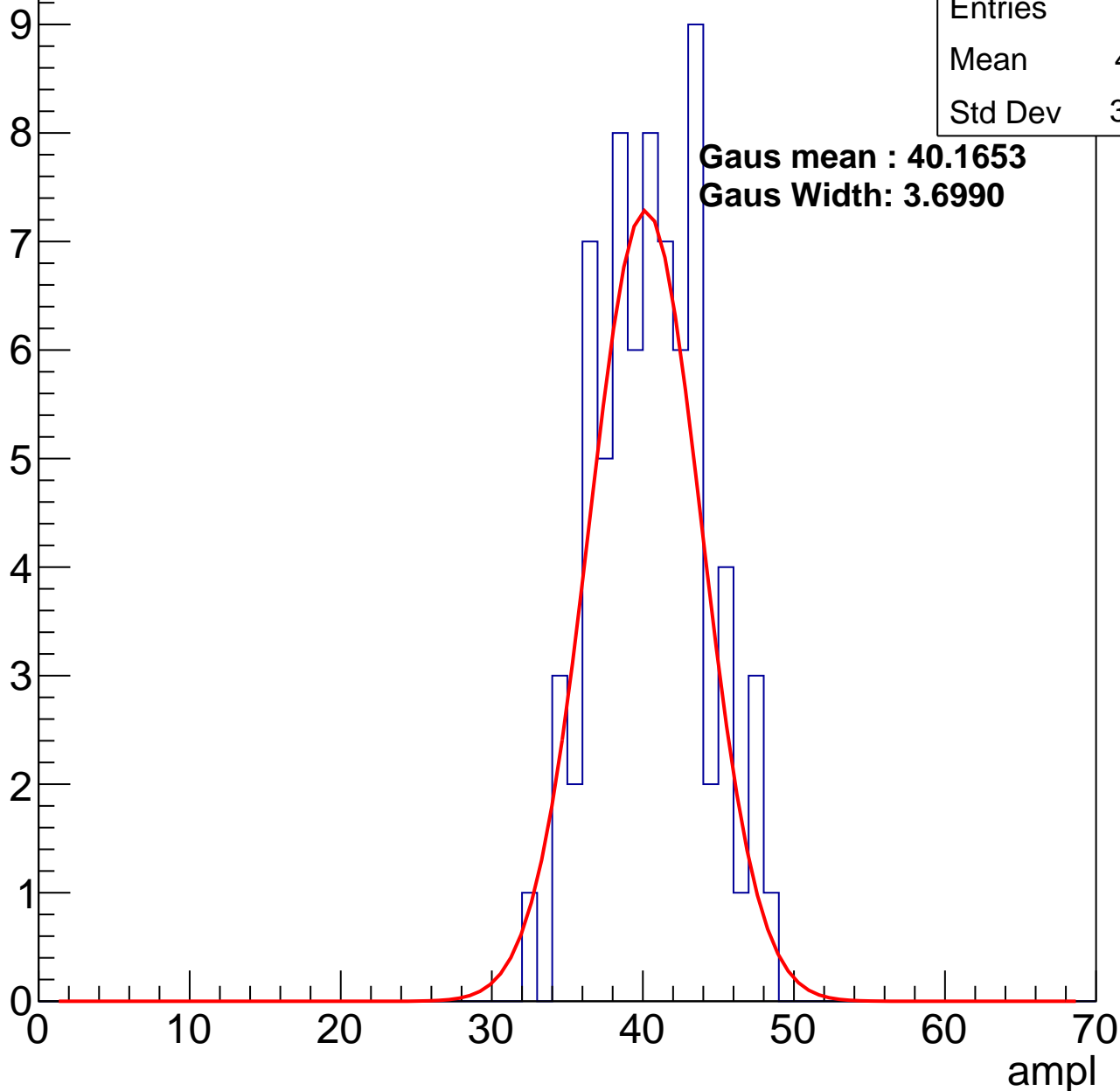
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	40.11
Std Dev	3.525

**Gaus mean : 40.1653**

**Gaus Width: 3.6990**

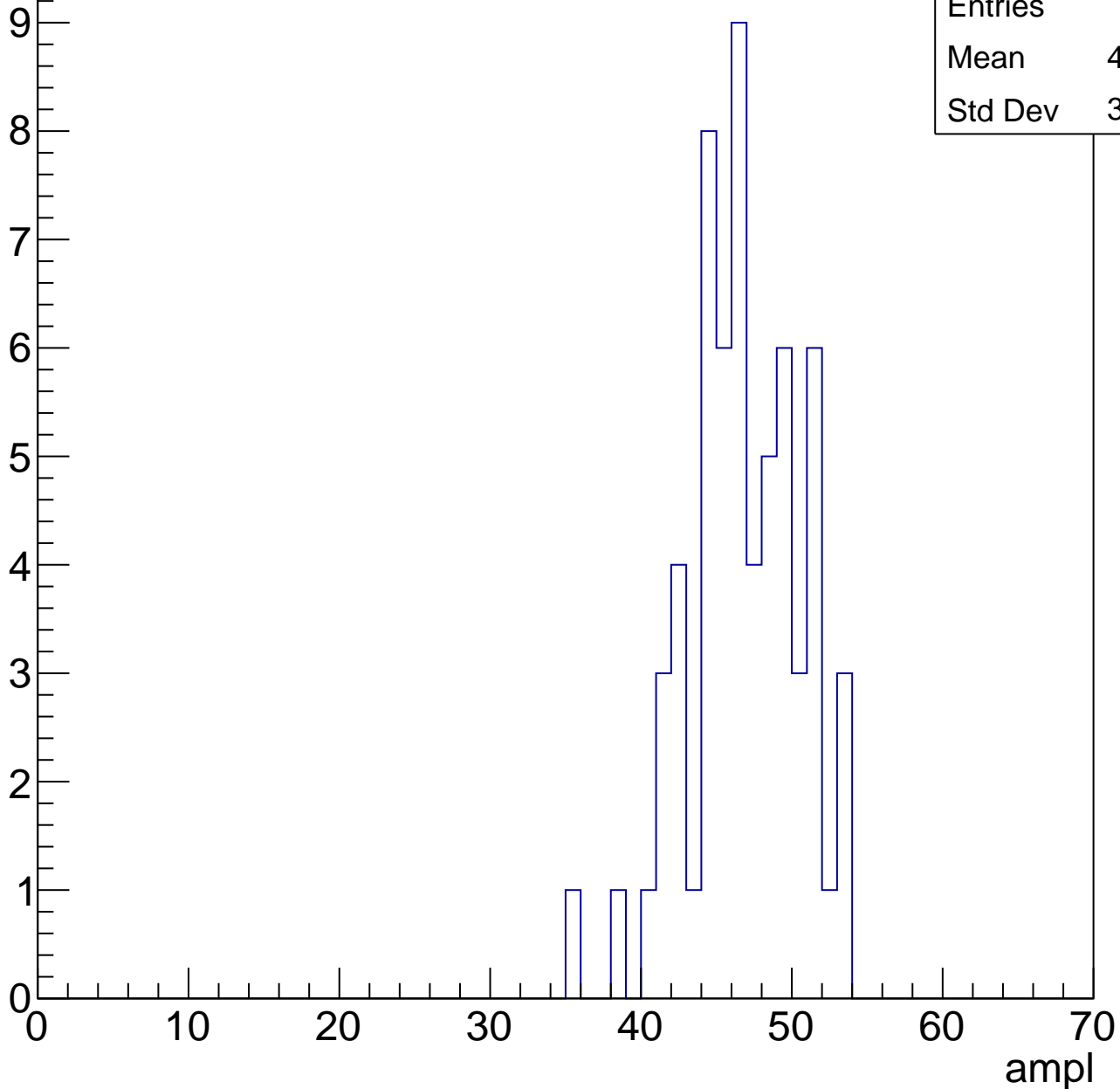


# B1L102S, U20-ch100, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	46.32
Std Dev	3.723

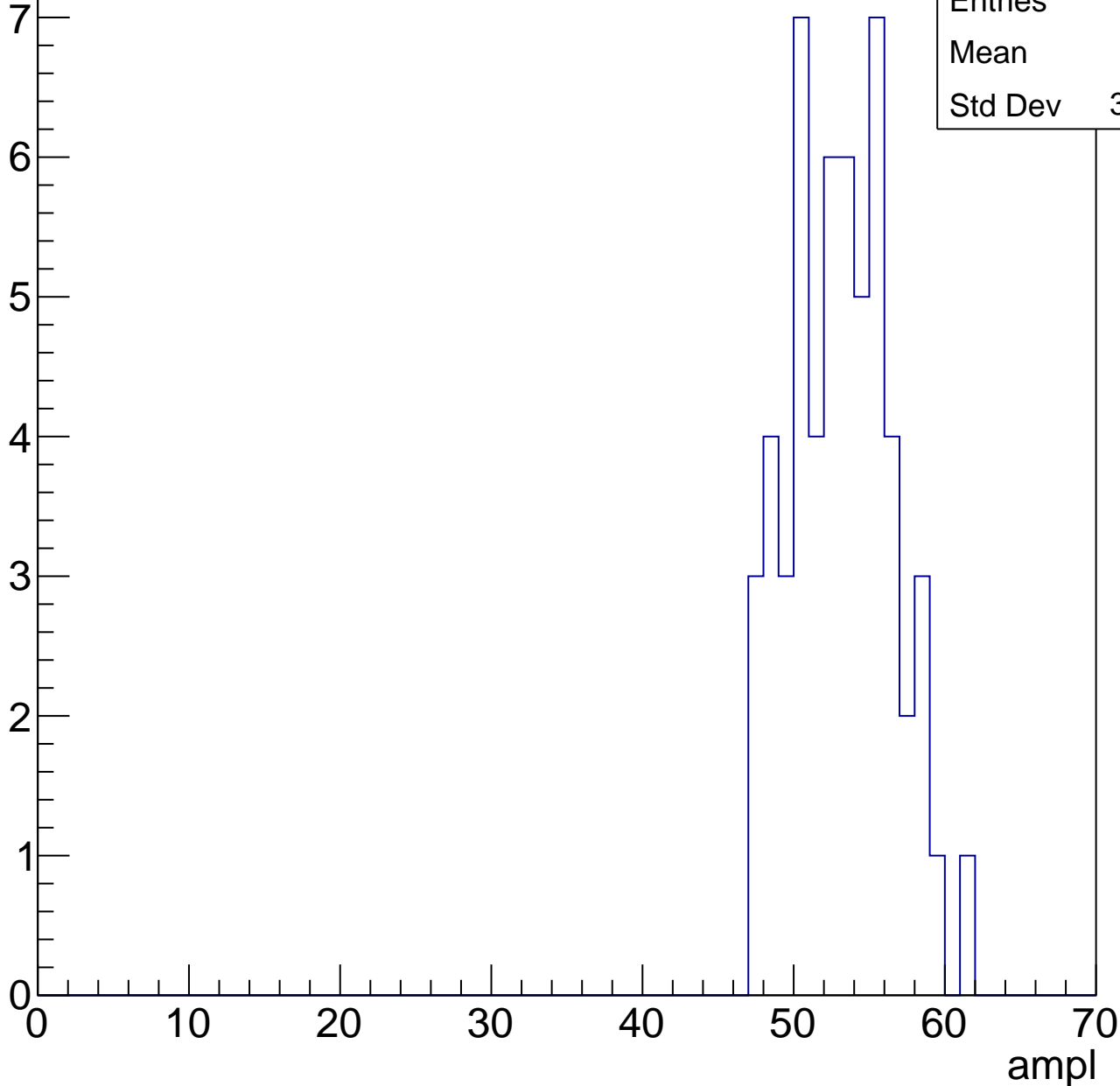


# B1L102S, U20-ch100, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

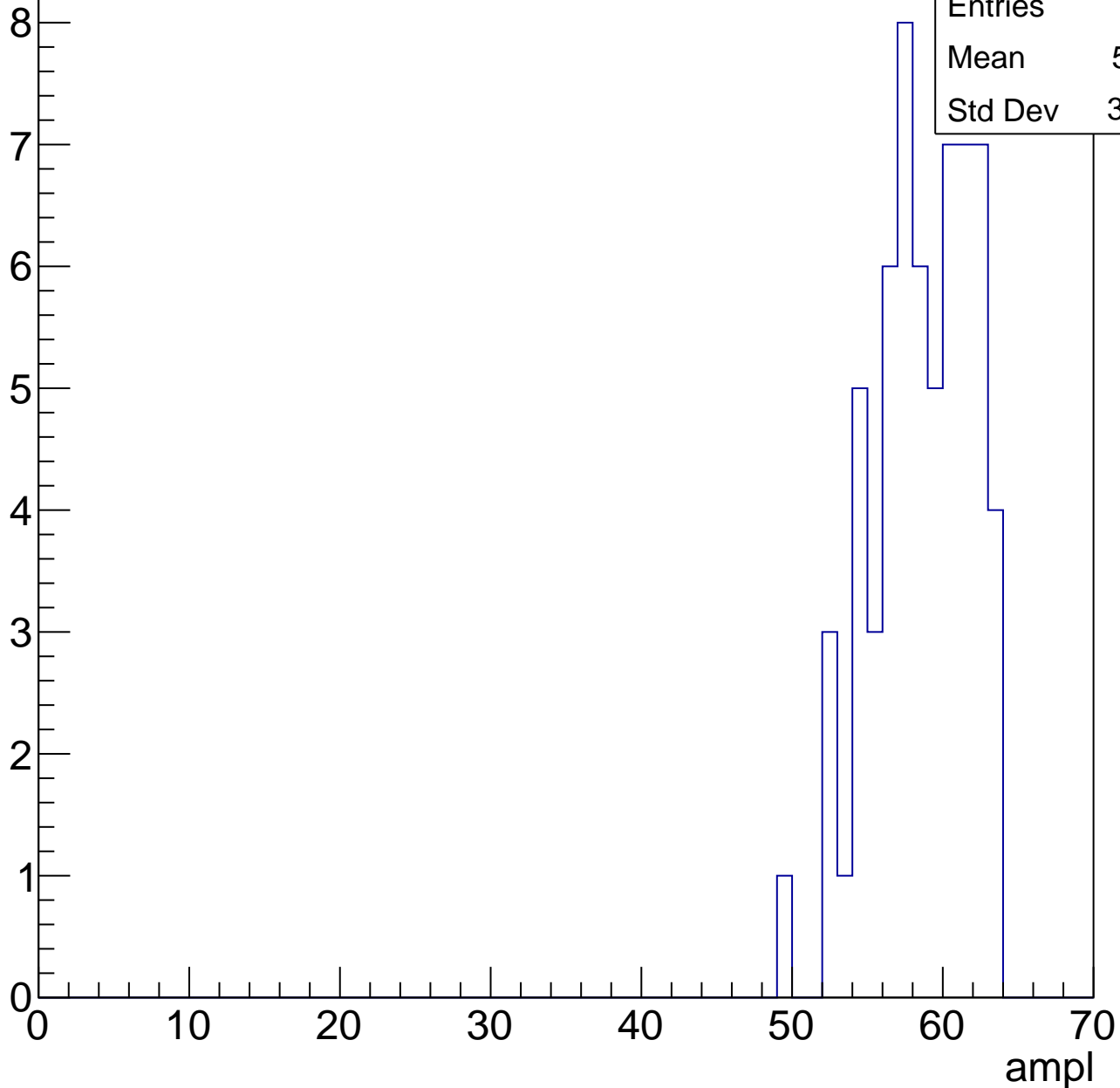
Entries	56
Mean	52.7
Std Dev	3.305



# B1L102S, U20-ch100, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

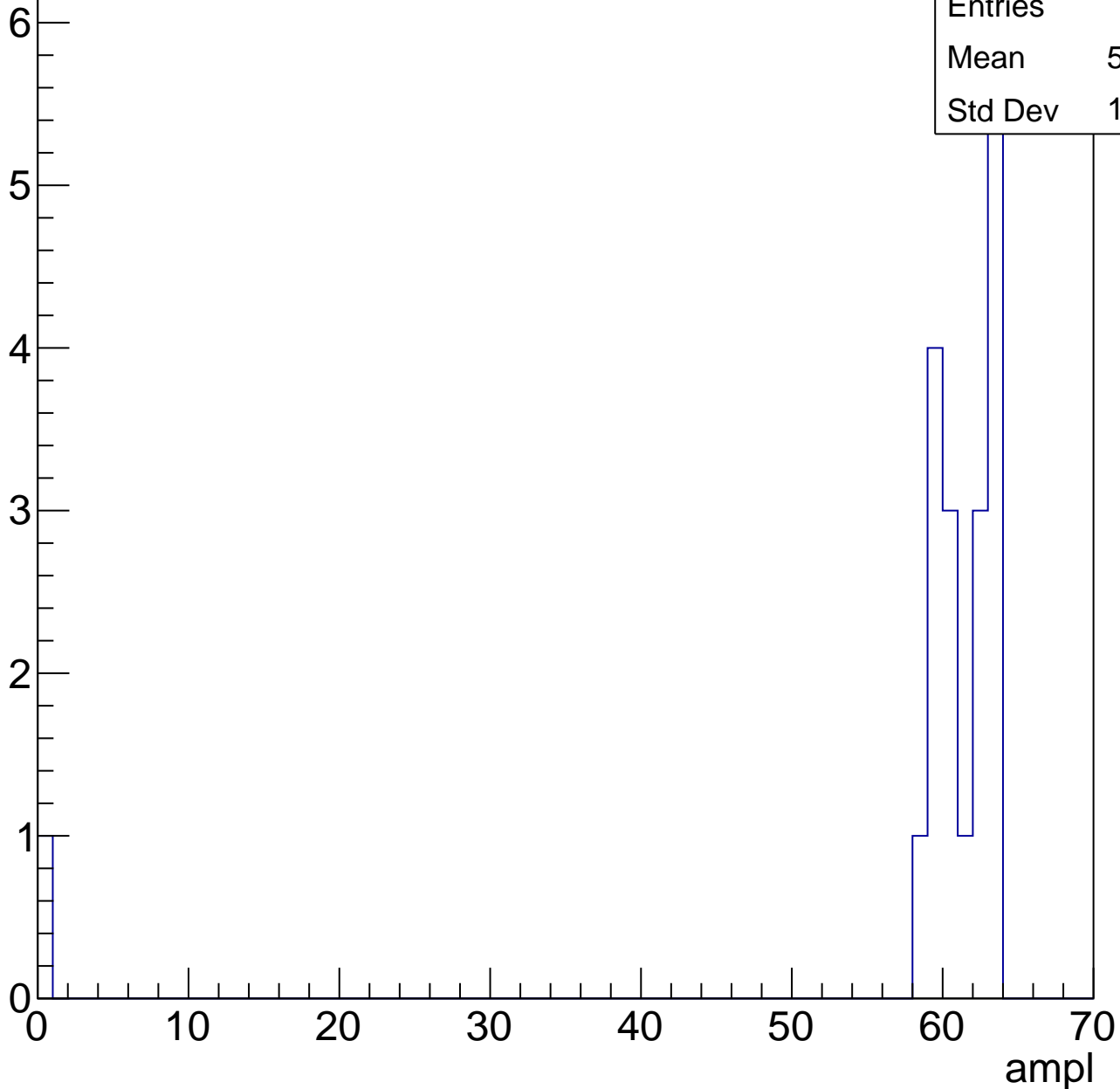


# B1L102S, U20-ch100, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	19
Mean	57.84
Std Dev	13.74





# B1L102S, U20-ch100, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch101, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	75
Mean	29.67
Std Dev	3.75

**Gaus mean : 29.9291**

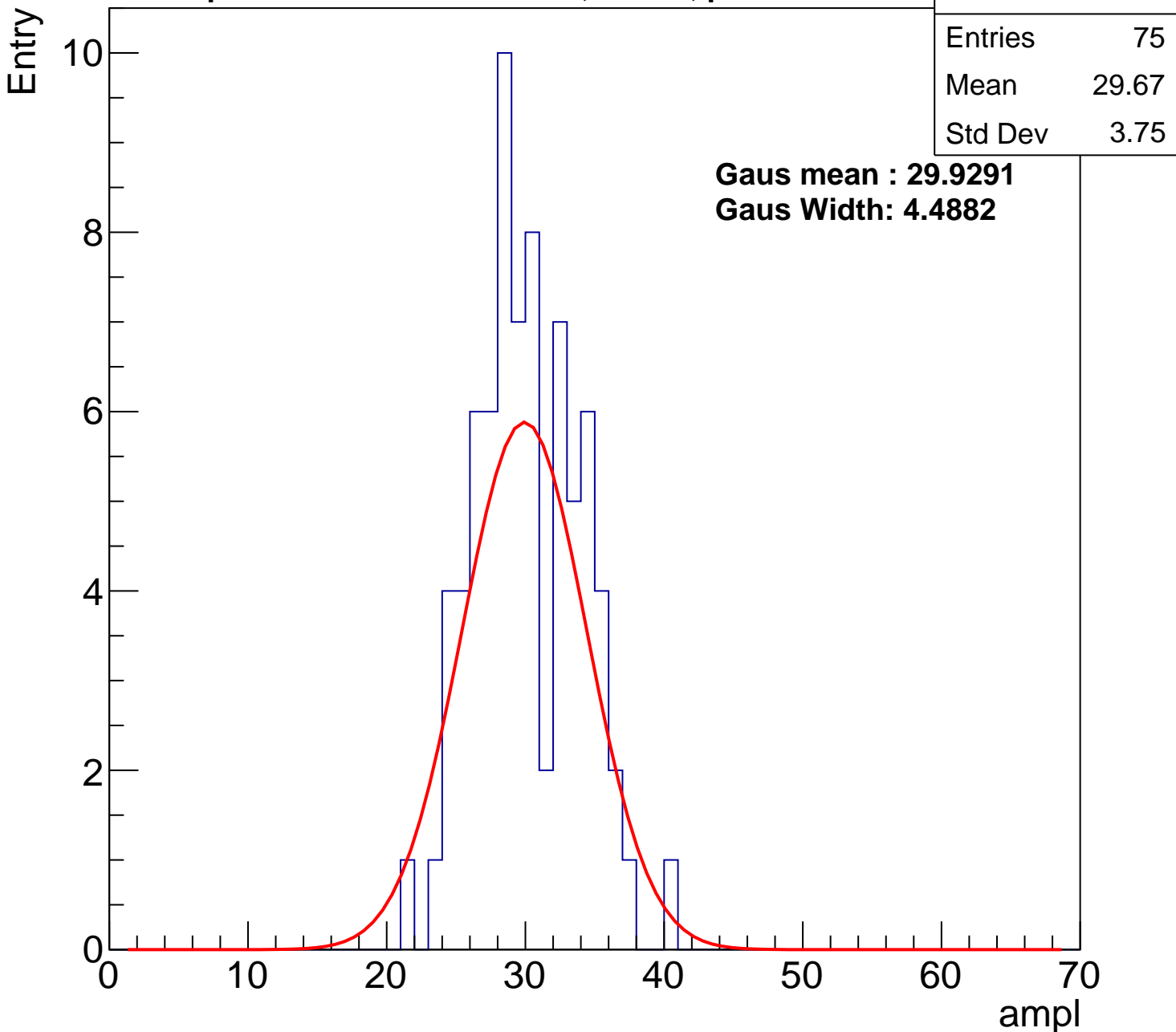
**Gaus Width: 4.4882**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U20-ch101, adc1

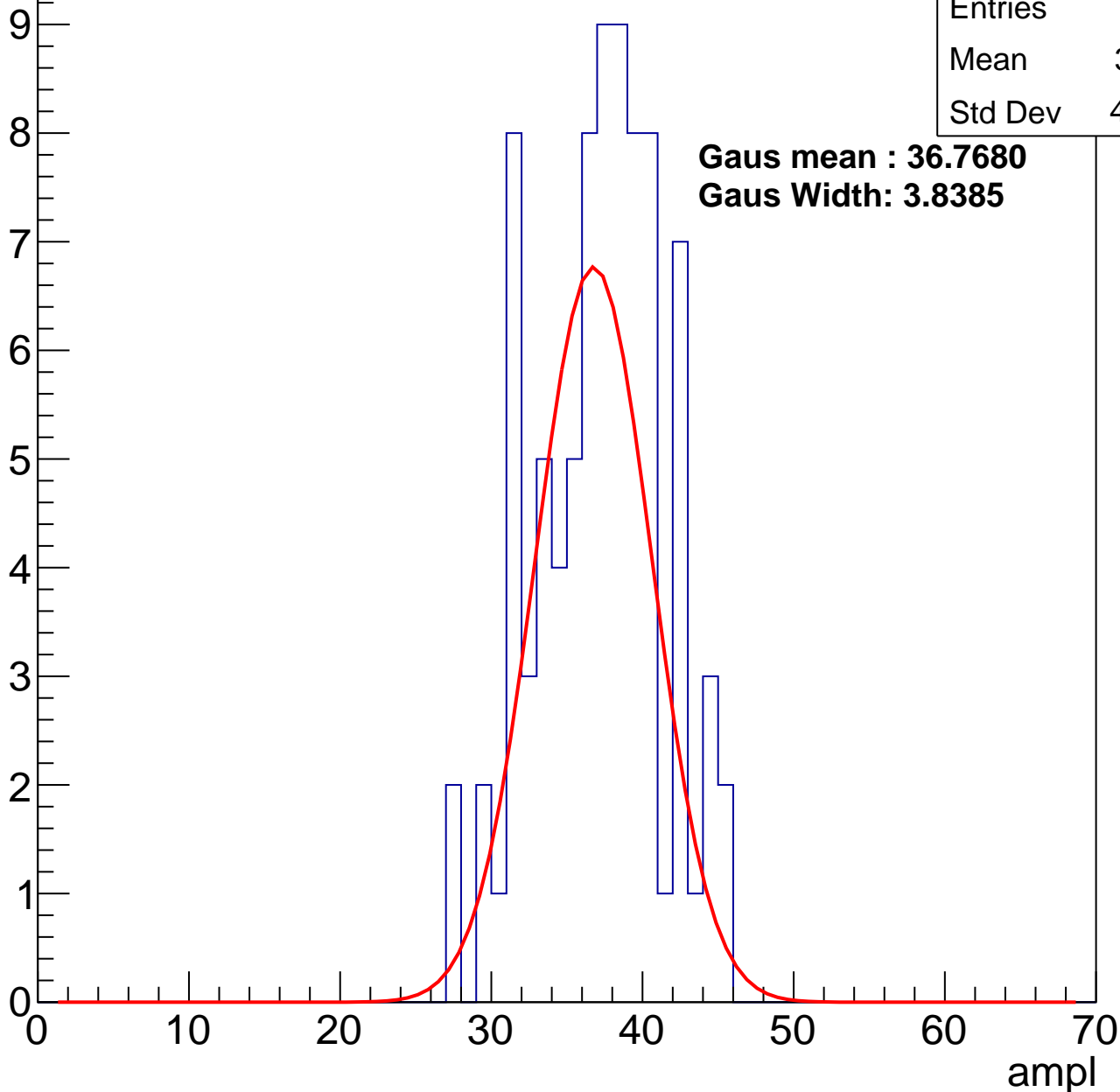
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	86
Mean	36.71
Std Dev	4.165

**Gaus mean : 36.7680**

**Gaus Width: 3.8385**



# B1L102S, U20-ch101, adc2

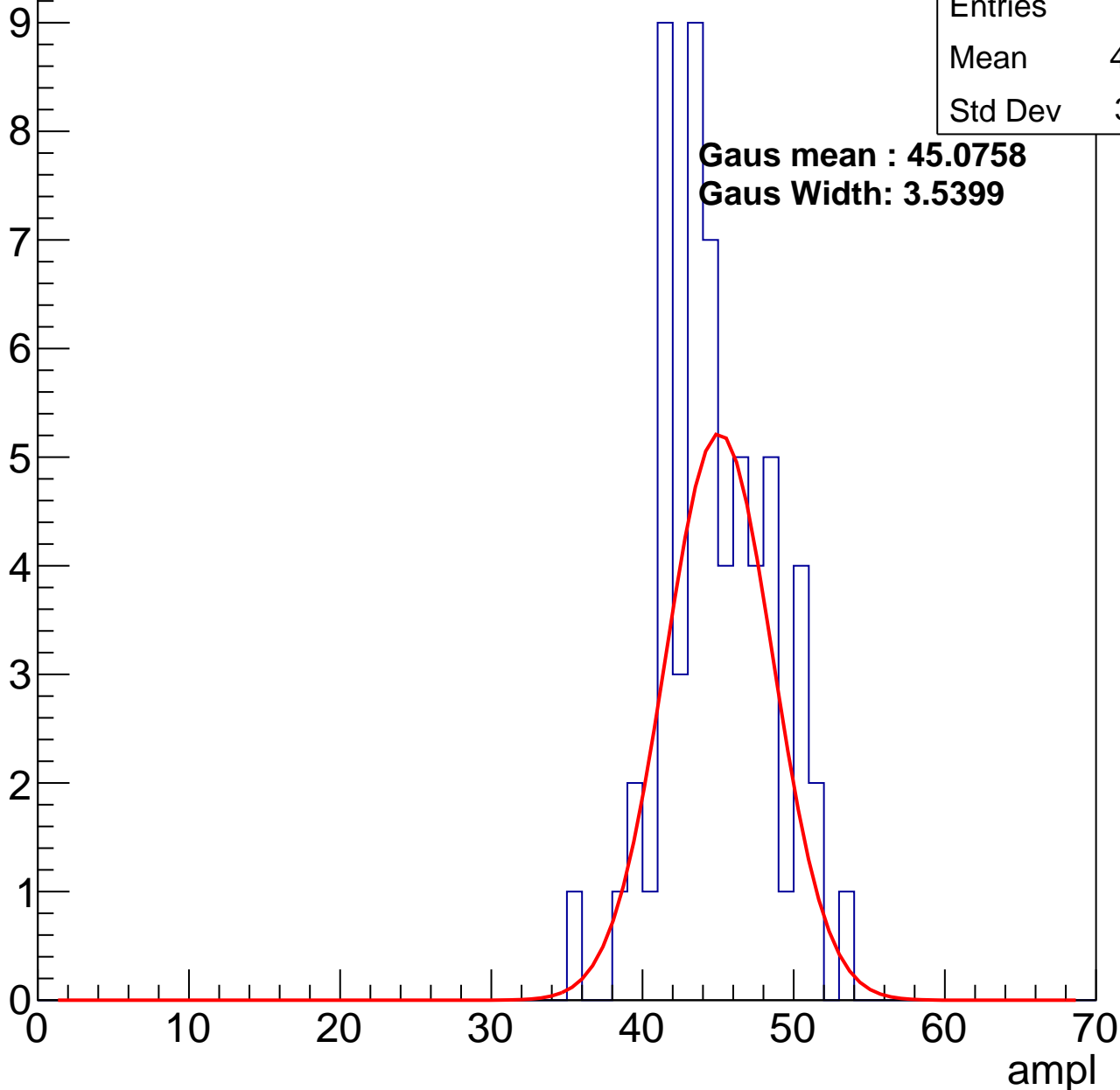
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	44.46
Std Dev	3.591

**Gaus mean : 45.0758**

**Gaus Width: 3.5399**

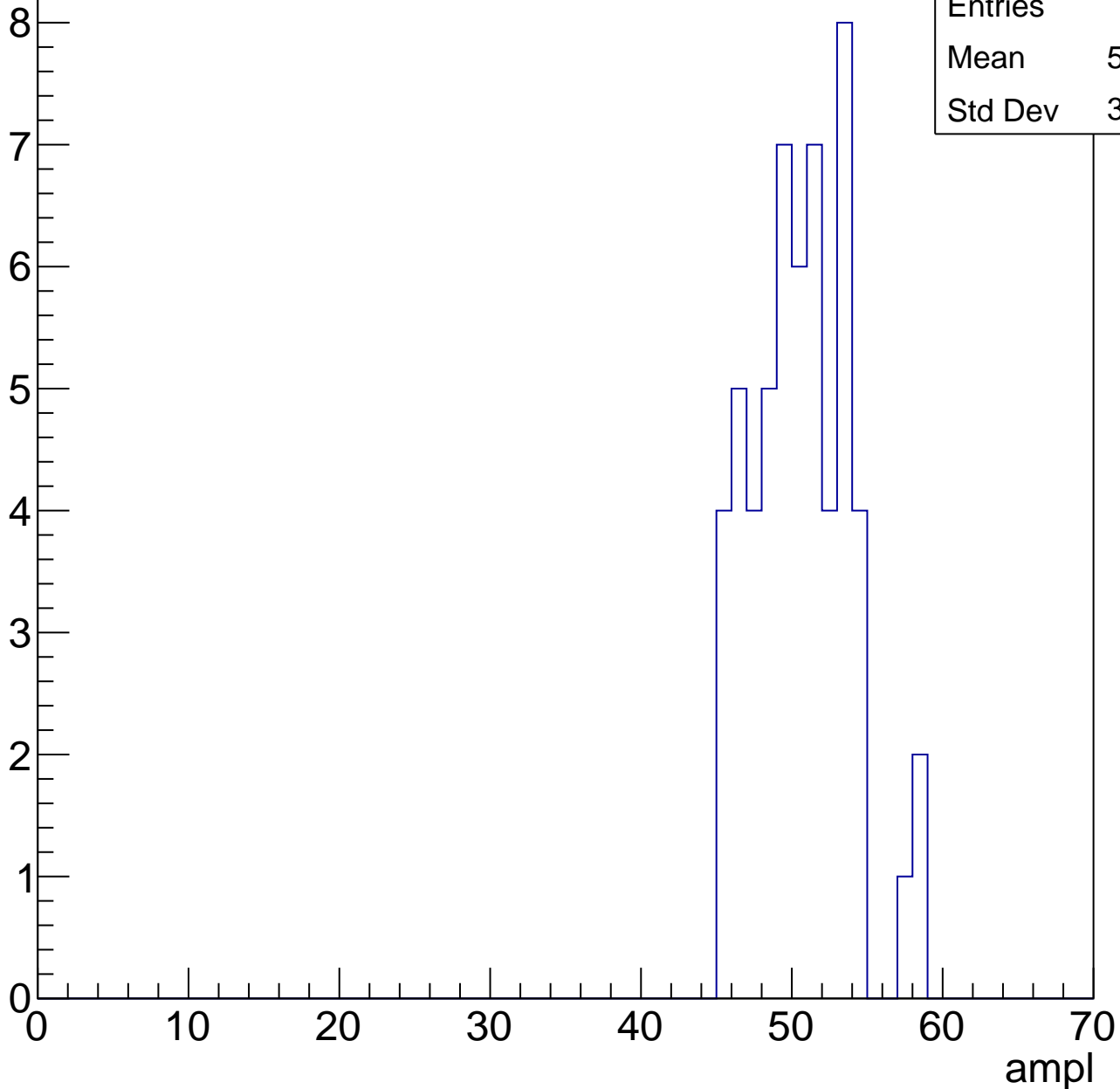


# B1L102S, U20-ch101, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	50.16
Std Dev	3.183

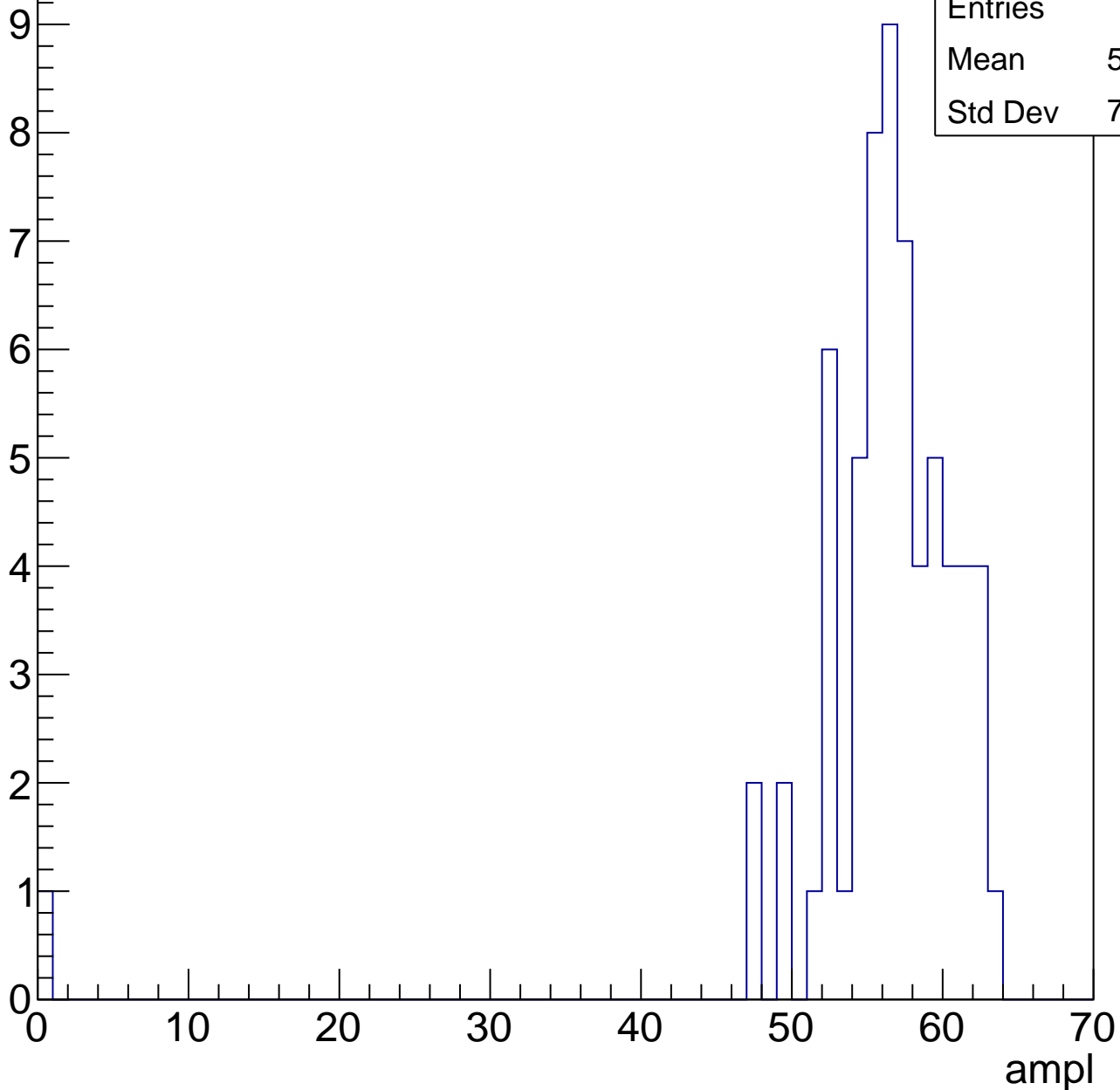


# B1L102S, U20-ch101, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	55.36
Std Dev	7.859

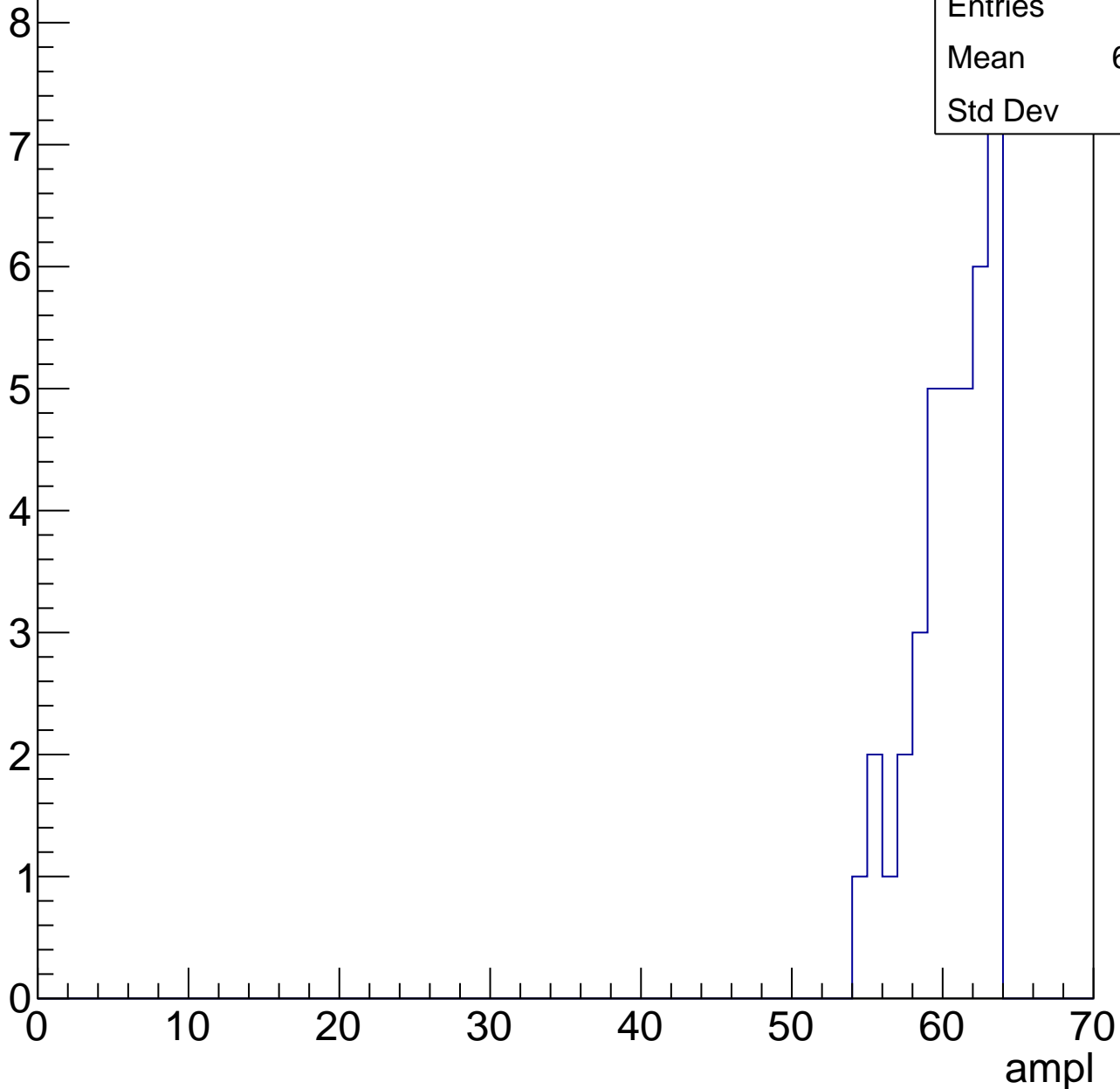


# B1L102S, U20-ch101, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	38
Mean	60.11
Std Dev	2.5



# B1L102S, U20-ch101, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries	4
Mean	60.5
Std Dev	1.803



# B1L102S, U20-ch101, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U20-ch102, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	87
Mean	28
Std Dev	3.991

**Gaus mean : 28.2284**

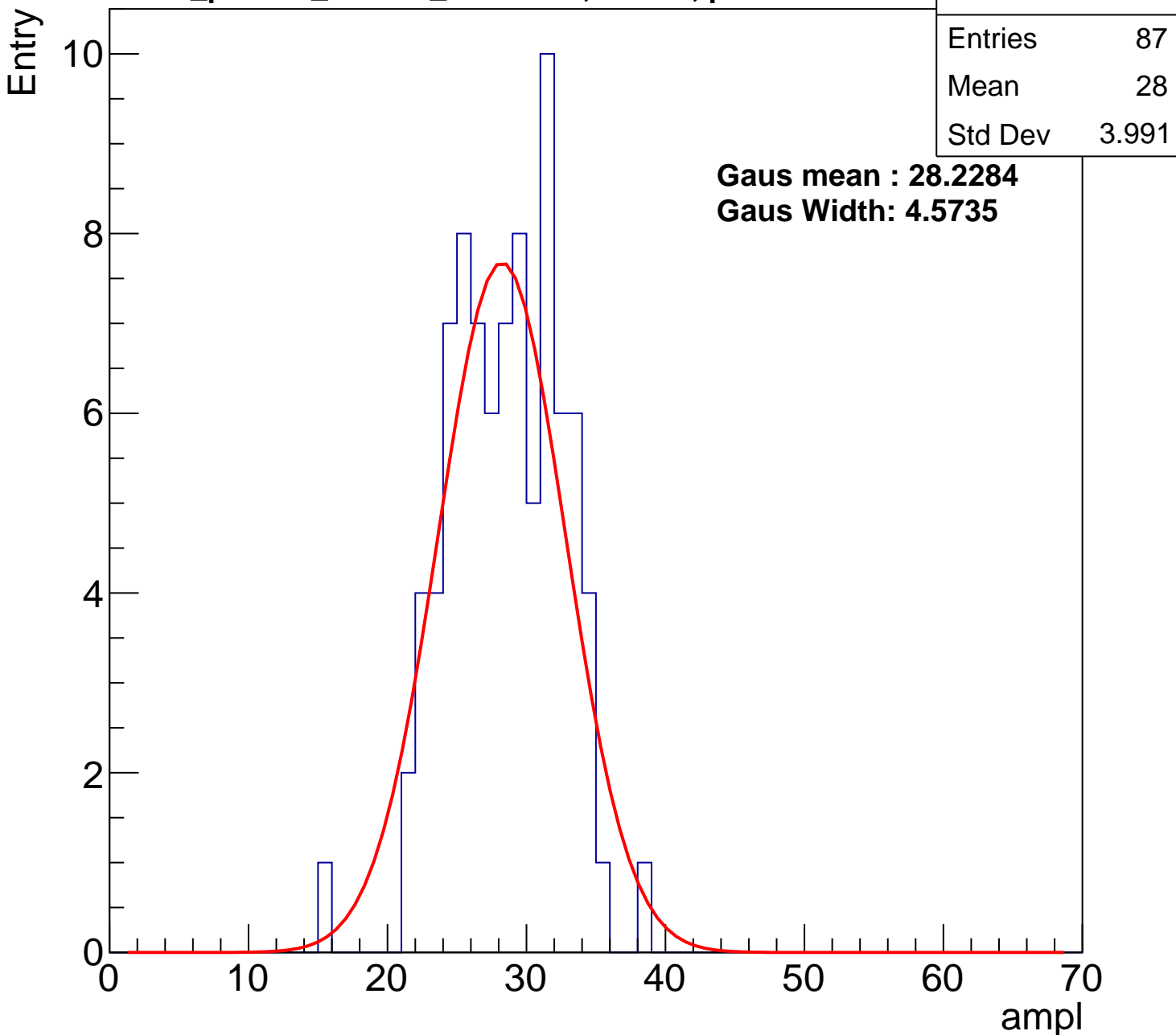
**Gaus Width: 4.5735**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U20-ch102, adc1

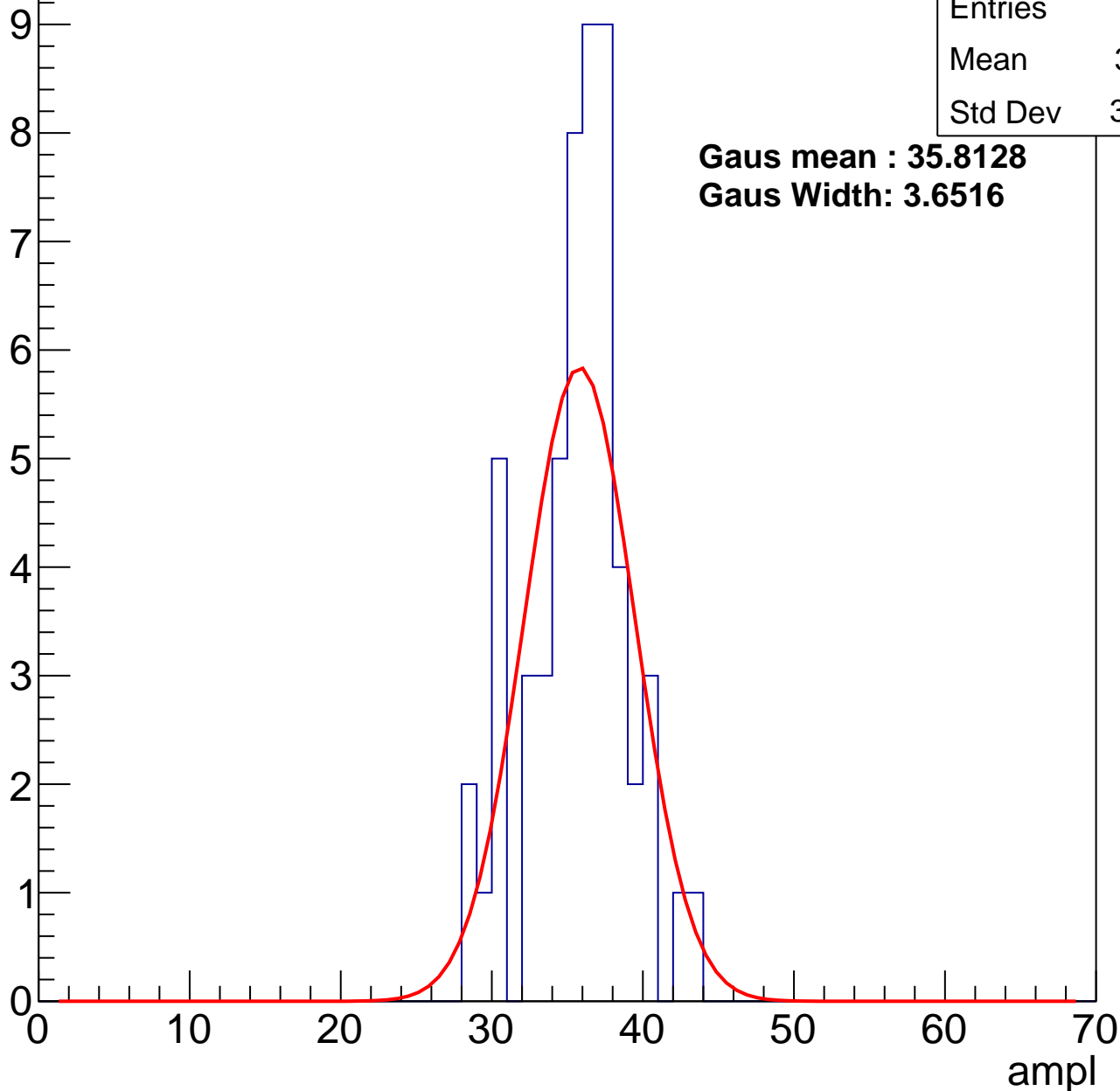
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	35.21
Std Dev	3.277

**Gaus mean : 35.8128**

**Gaus Width: 3.6516**



# B1L102S, U20-ch102, adc2

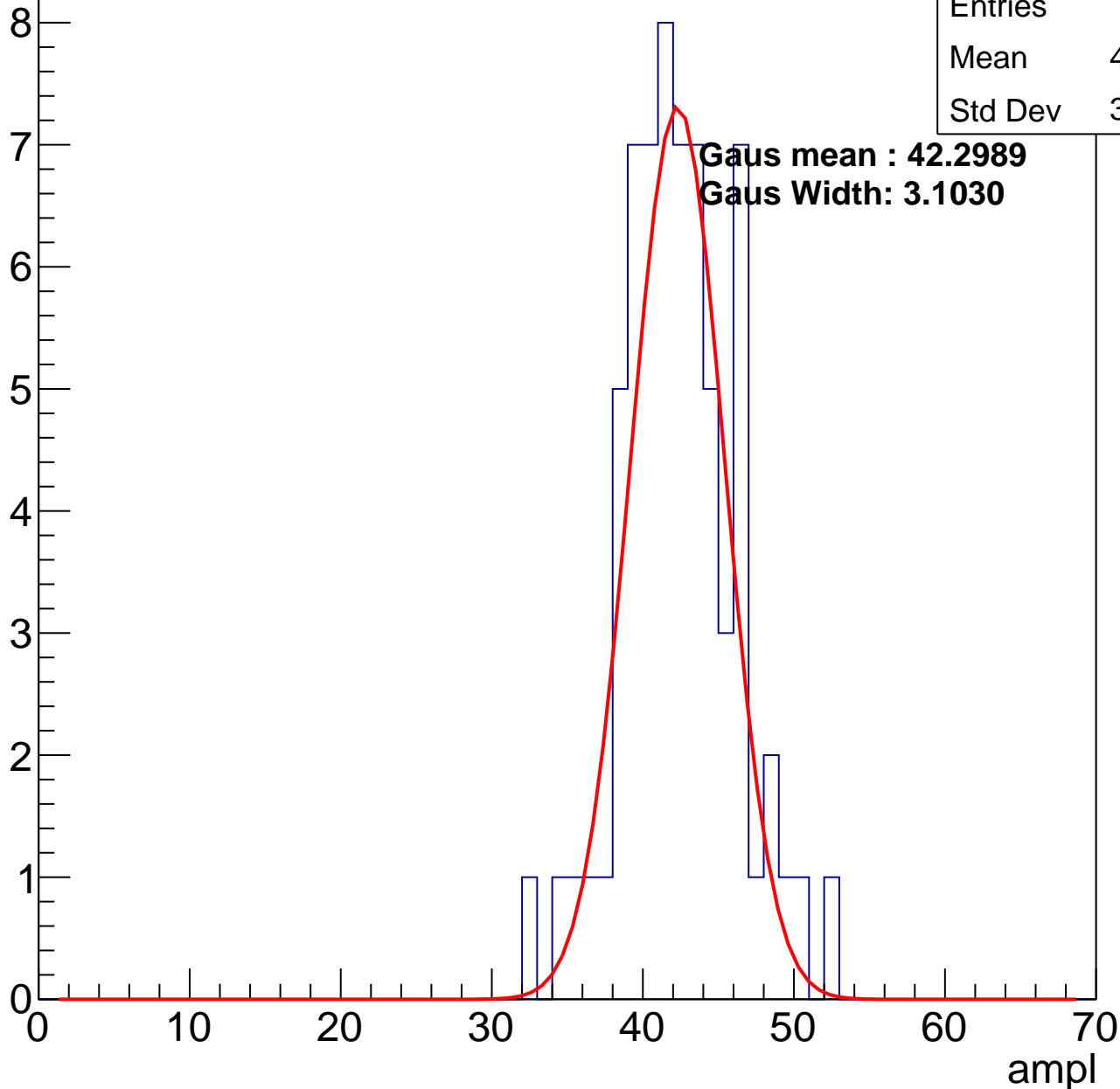
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	41.96
Std Dev	3.723

**Gaus mean : 42.2989**

**Gaus Width: 3.1030**

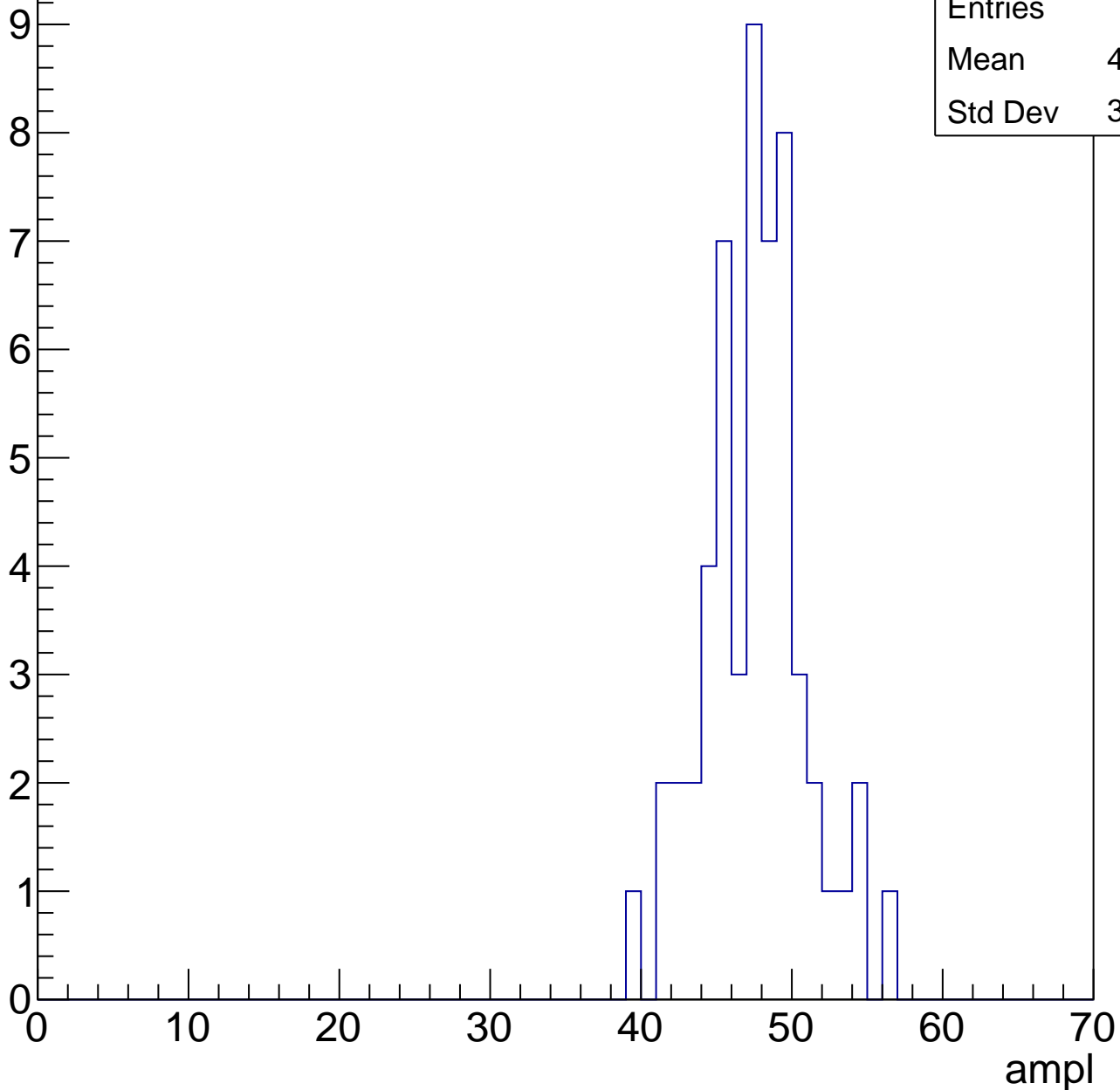


# B1L102S, U20-ch102, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	47.13
Std Dev	3.363

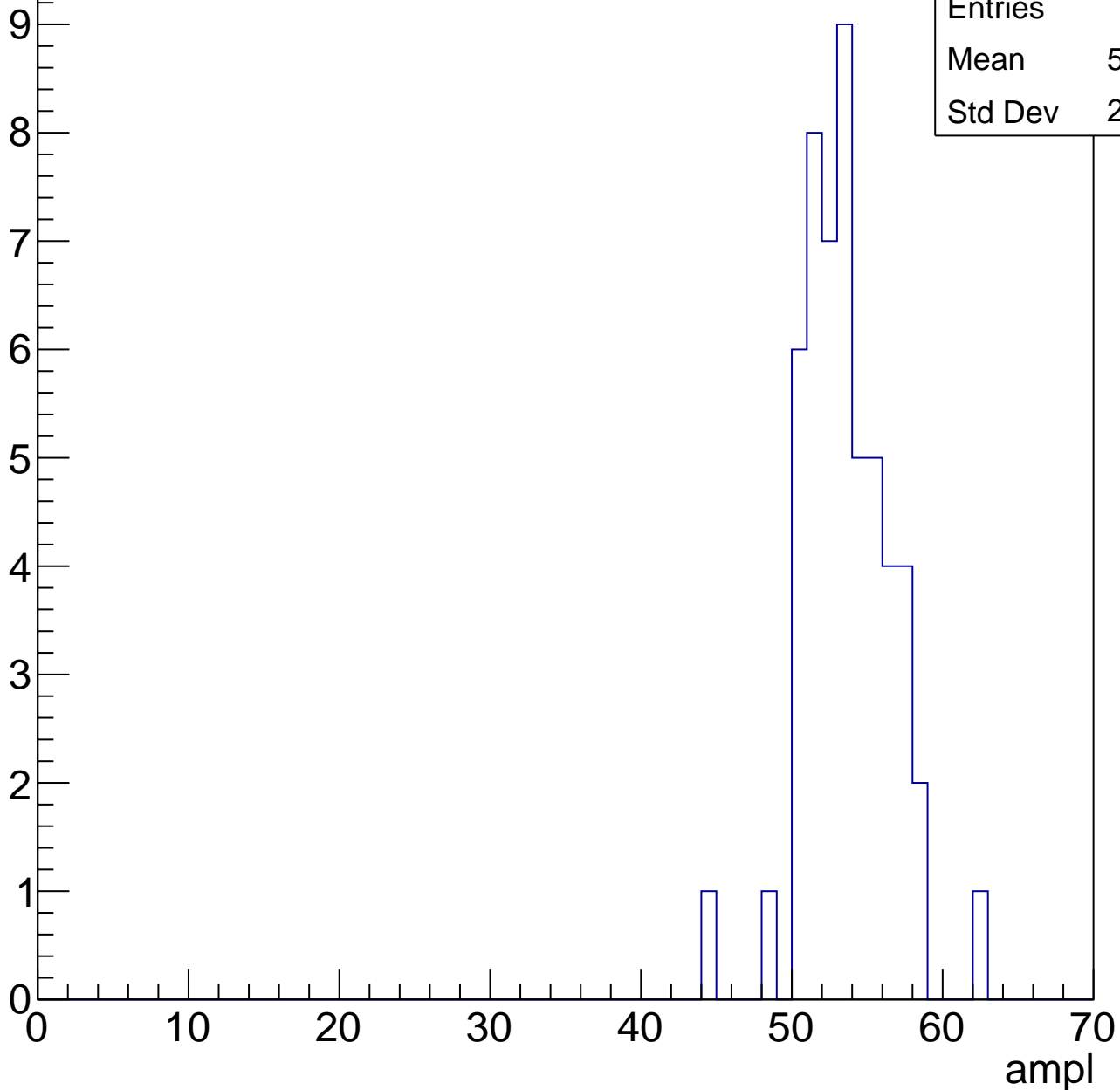


# B1L102S, U20-ch102, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	53.13
Std Dev	2.927

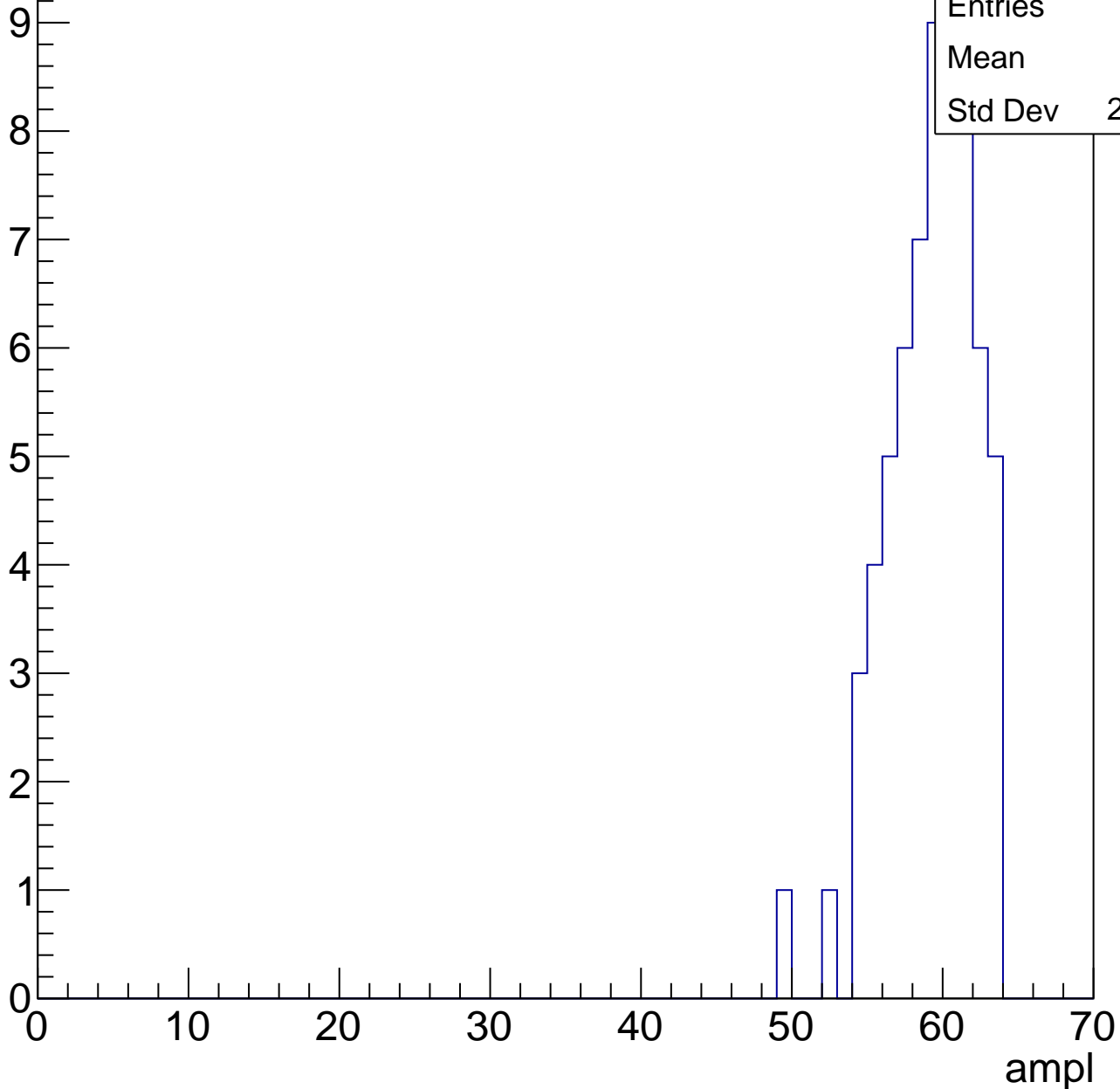


# B1L102S, U20-ch102, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	58.7
Std Dev	2.887

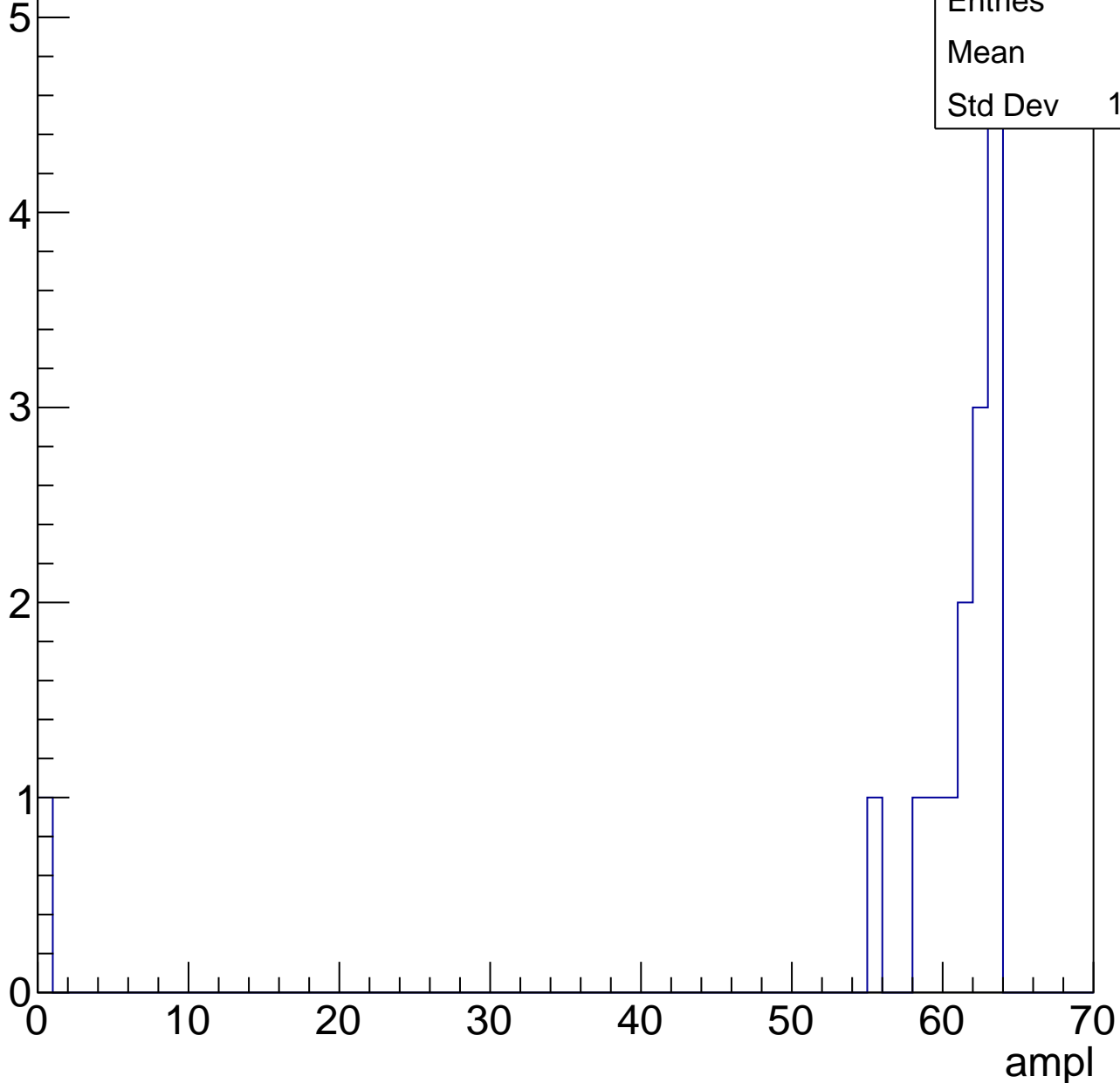


# B1L102S, U20-ch102, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	15
Mean	57
Std Dev	15.39





# B1L102S, U20-ch102, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	0
Std Dev	0

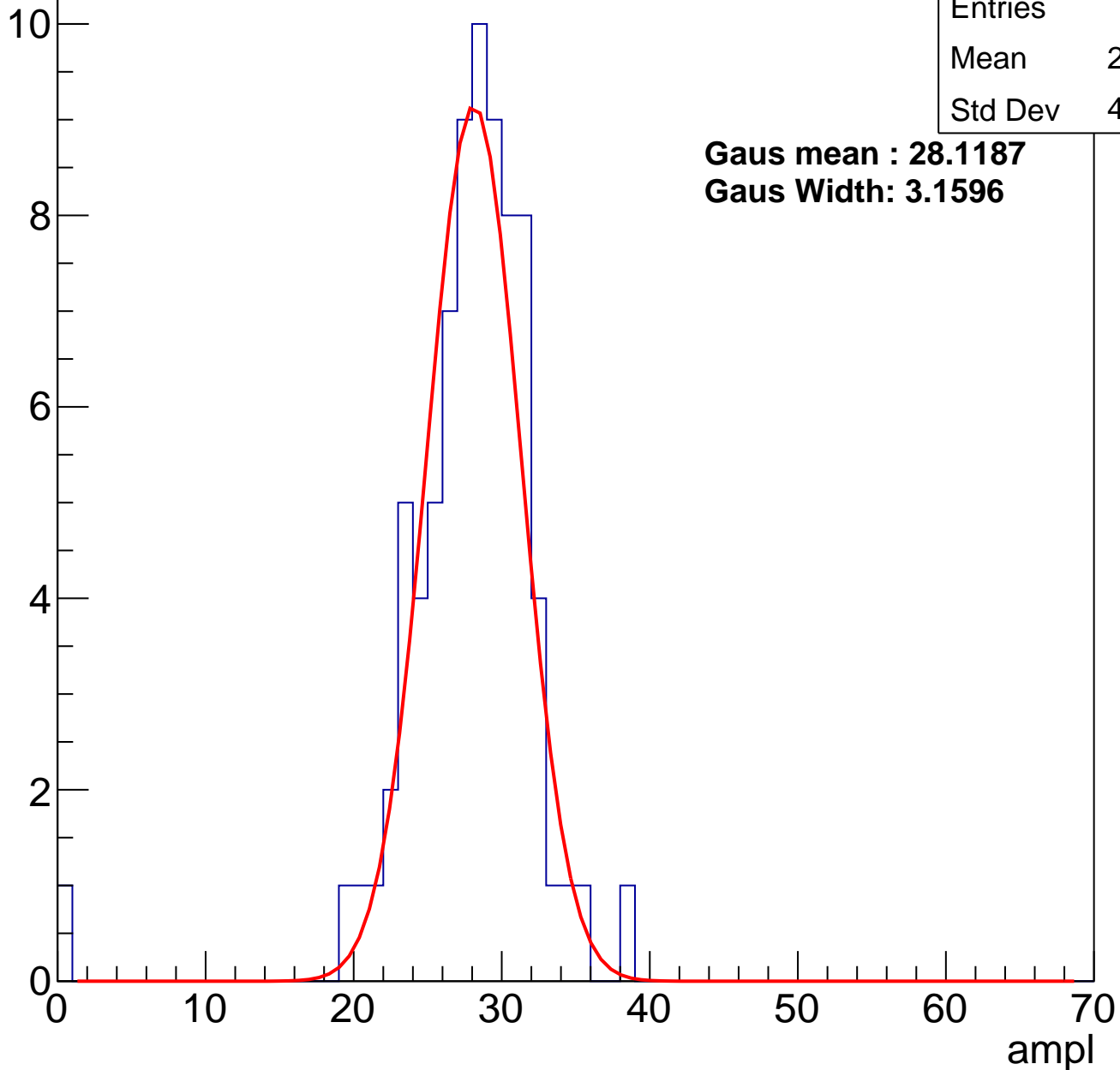
# B1L102S, U20-ch103, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	79
Mean	27.37
Std Dev	4.606

**Gaus mean : 28.1187**  
**Gaus Width: 3.1596**

Entry



# B1L102S, U20-ch103, adc1

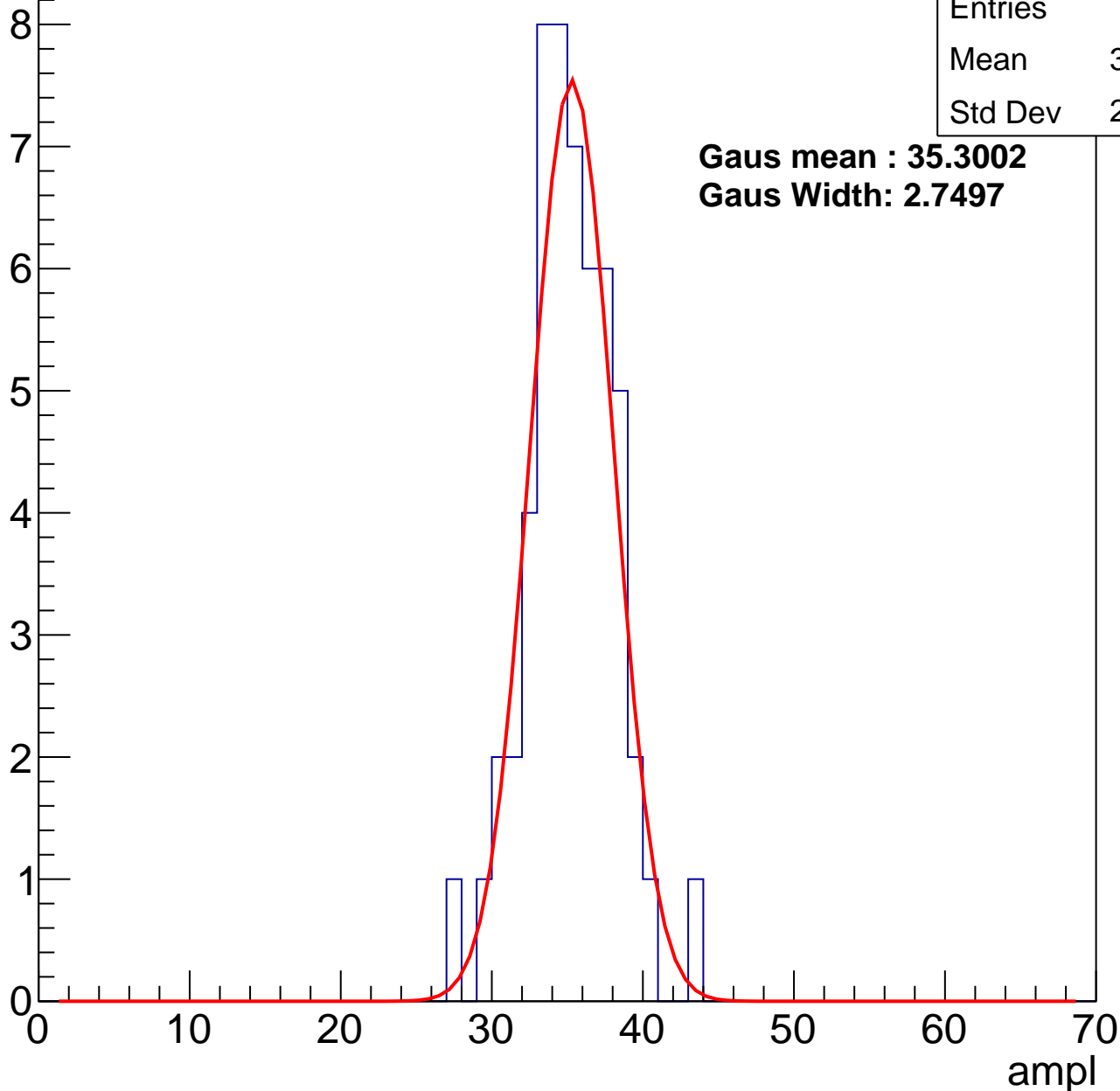
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	34.74
Std Dev	2.888

**Gaus mean : 35.3002**

**Gaus Width: 2.7497**



# B1L102S, U20-ch103, adc2

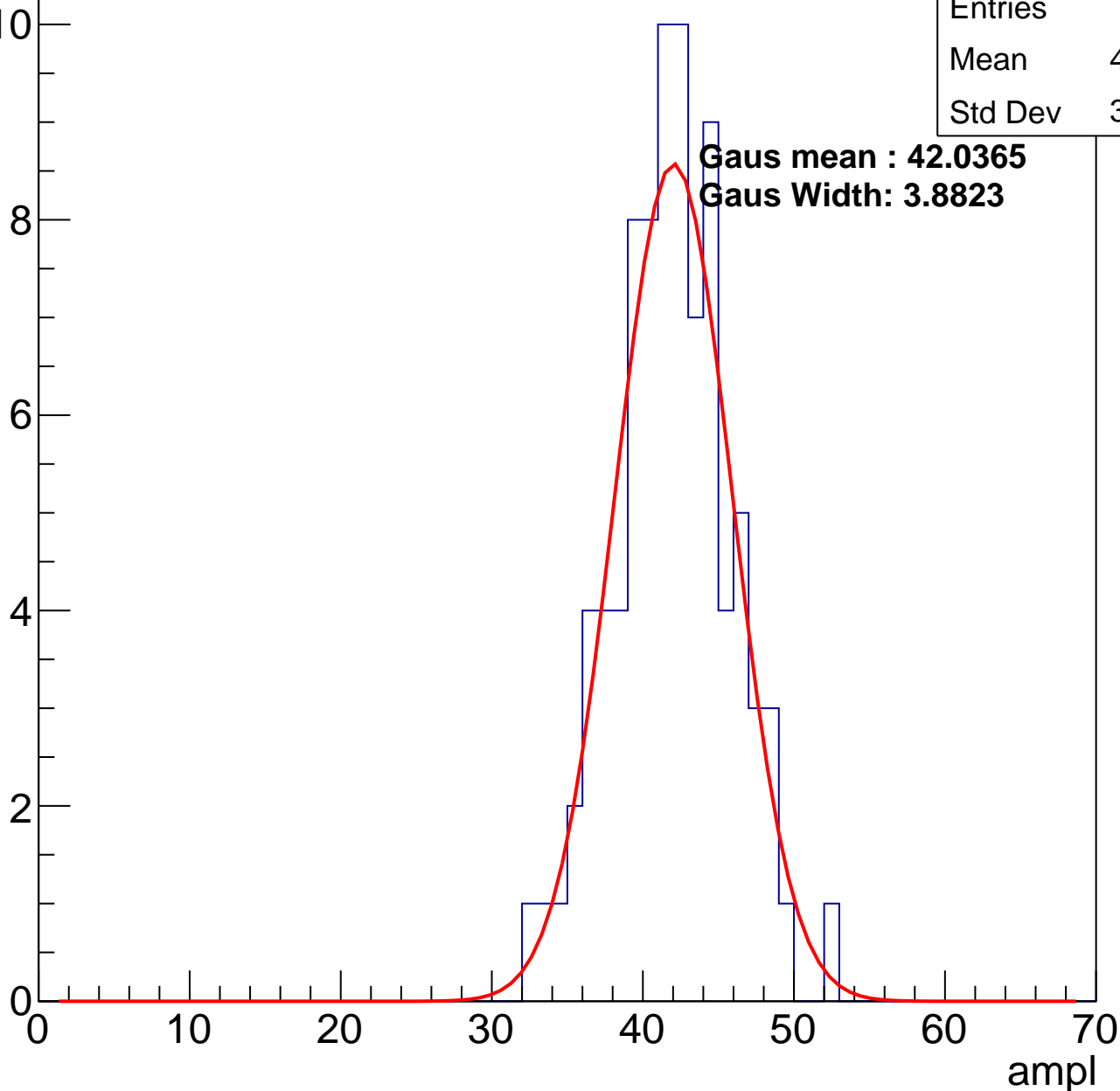
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	86
Mean	41.49
Std Dev	3.787

**Gaus mean : 42.0365**

**Gaus Width: 3.8823**

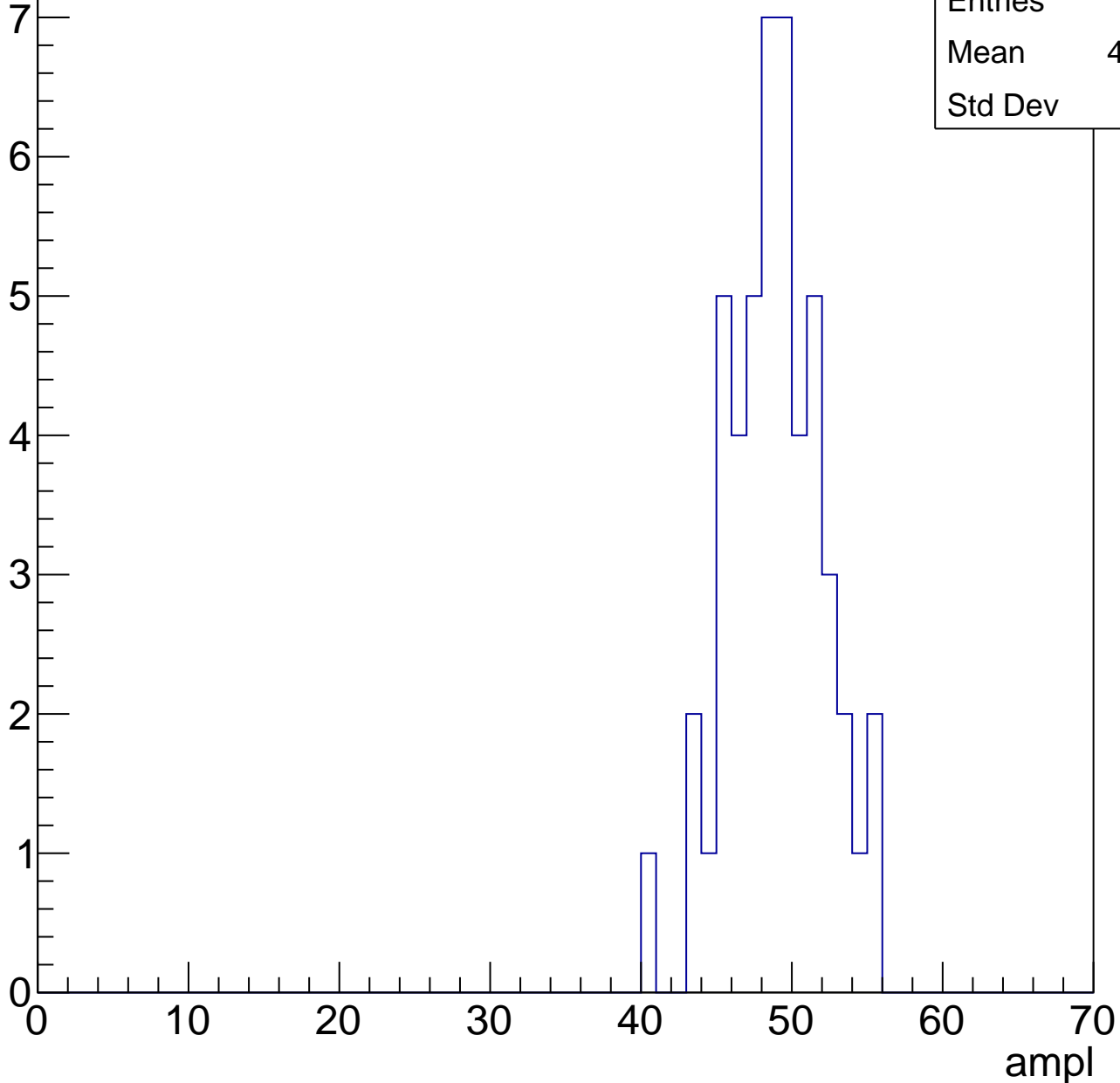


# B1L102S, U20-ch103, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	48.45
Std Dev	3.15

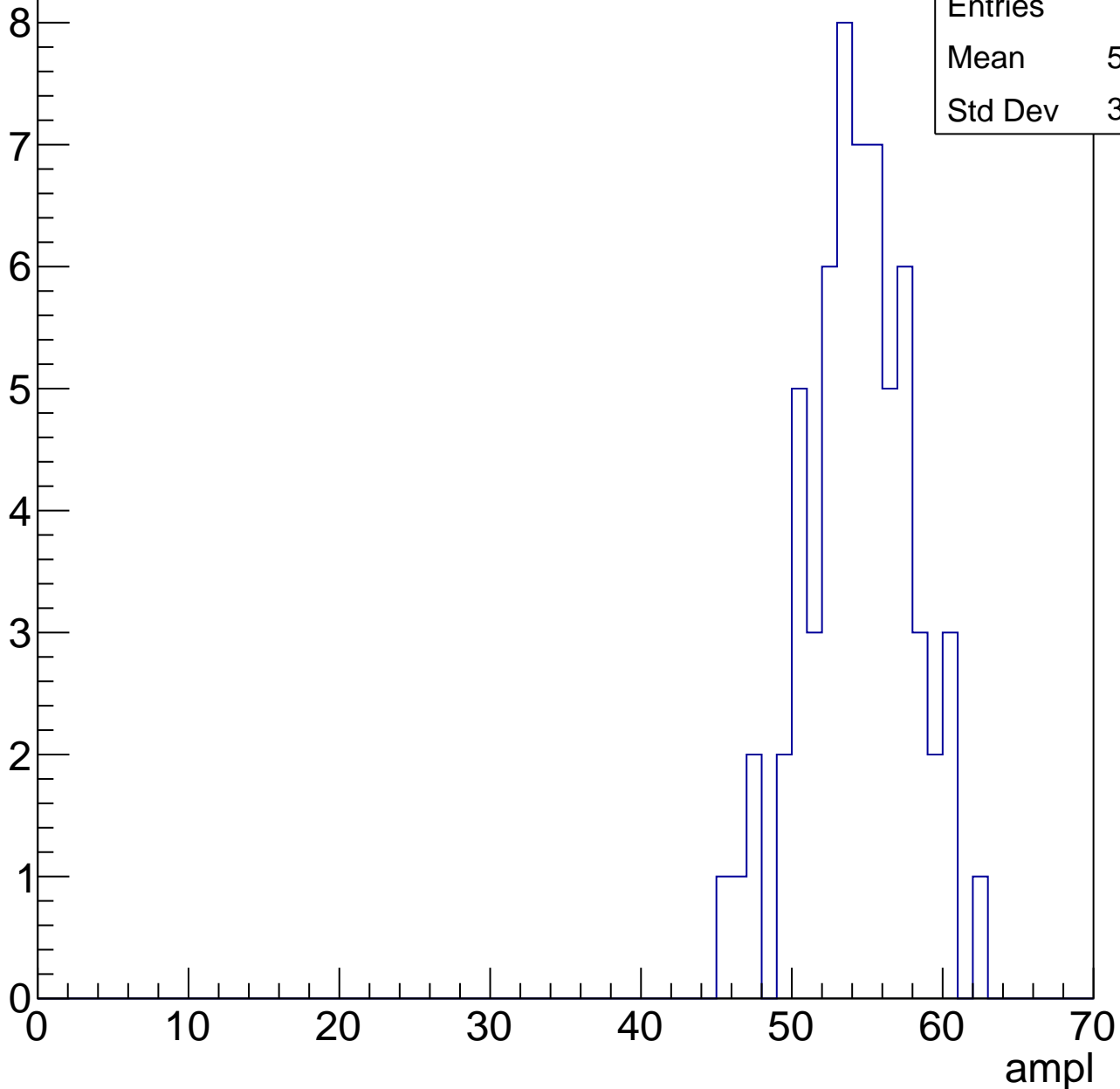


# B1L102S, U20-ch103, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	53.89
Std Dev	3.552

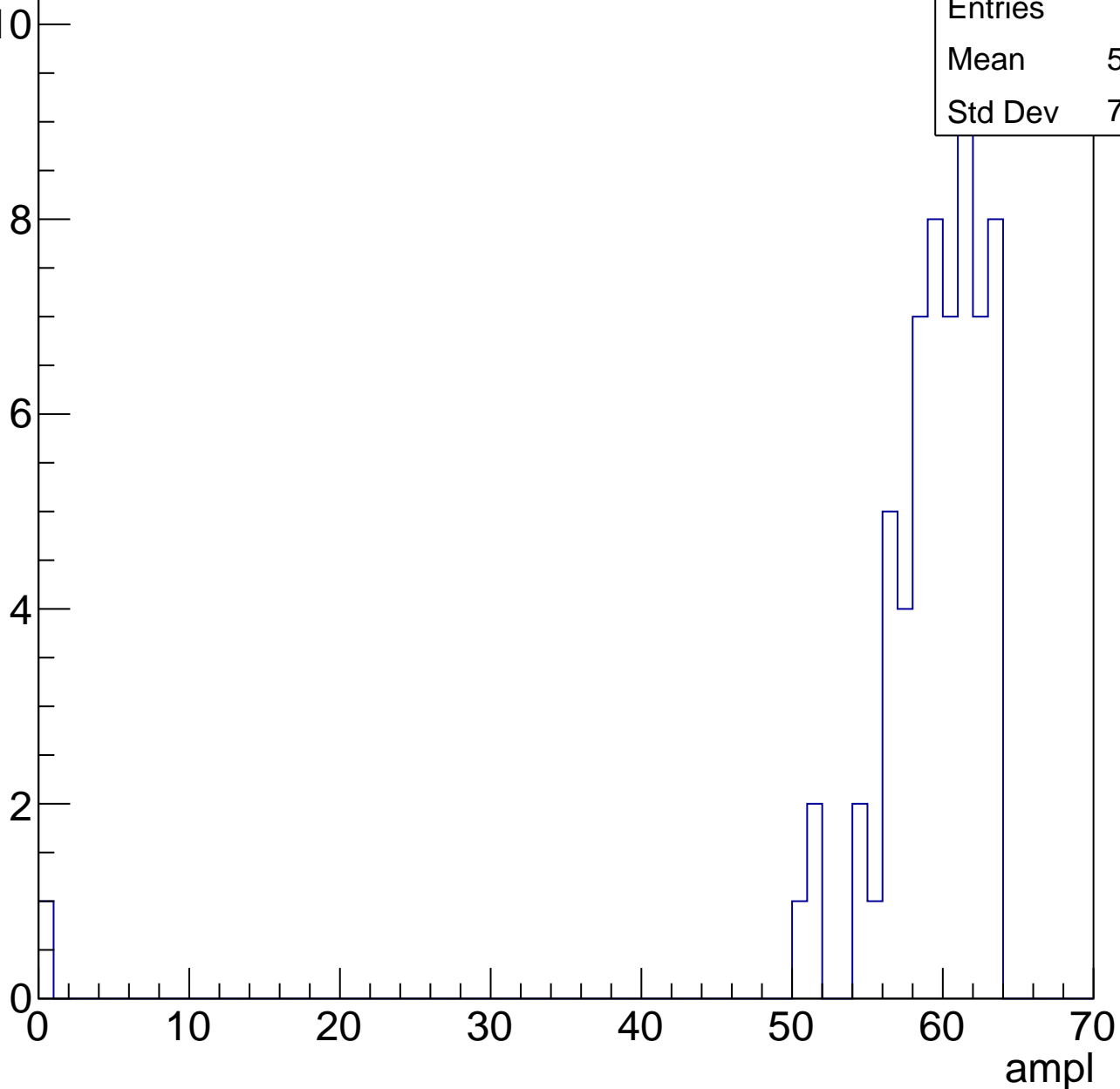


# B1L102S, U20-ch103, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	58.24
Std Dev	7.993



# B1L102S, U20-ch103, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U20-ch103, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	3
Mean	21
Std Dev	29.7

# B1L102S, U20-ch104, adc0

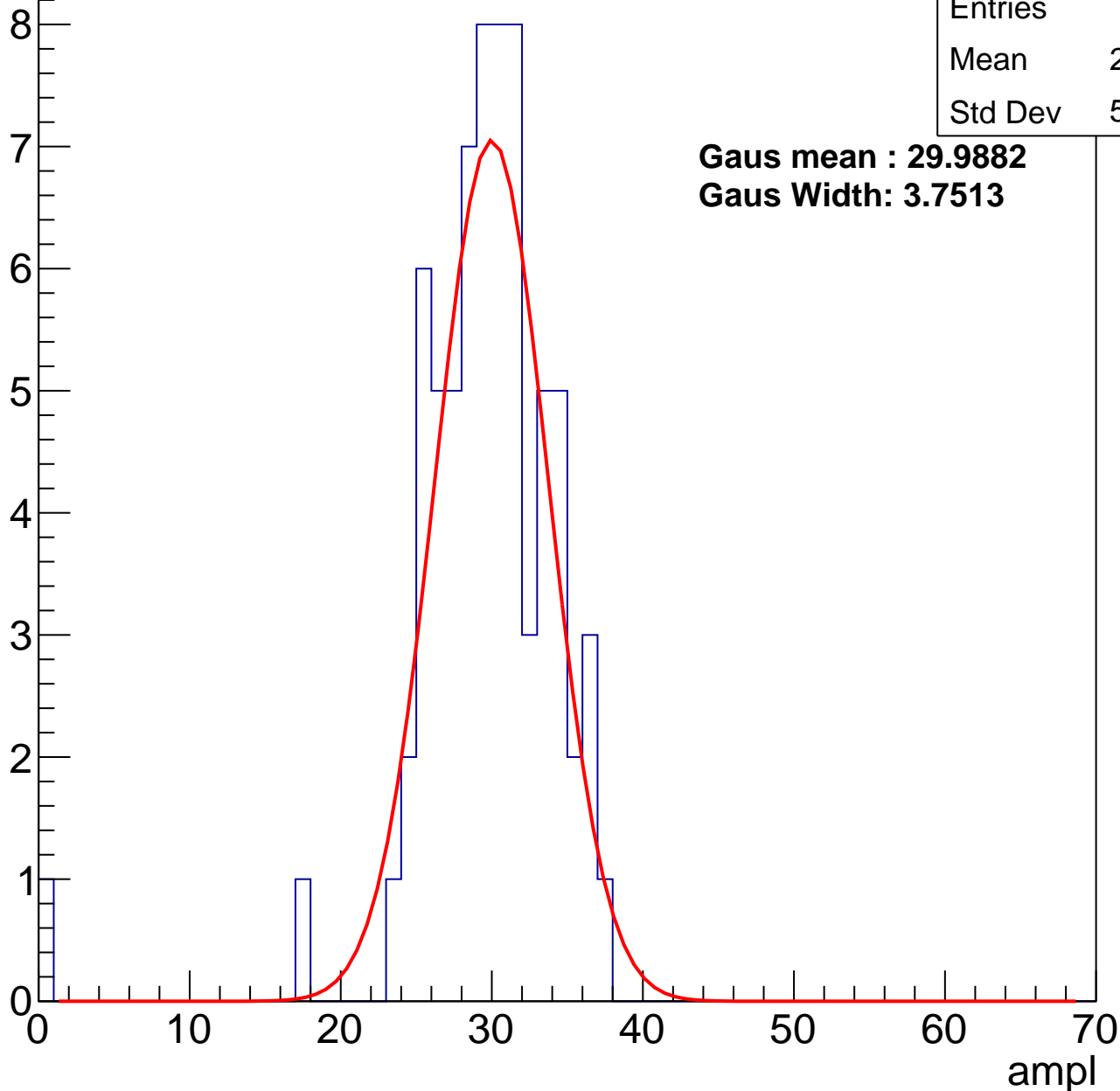
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	29.08
Std Dev	5.026

**Gaus mean : 29.9882**

**Gaus Width: 3.7513**



# B1L102S, U20-ch104, adc1

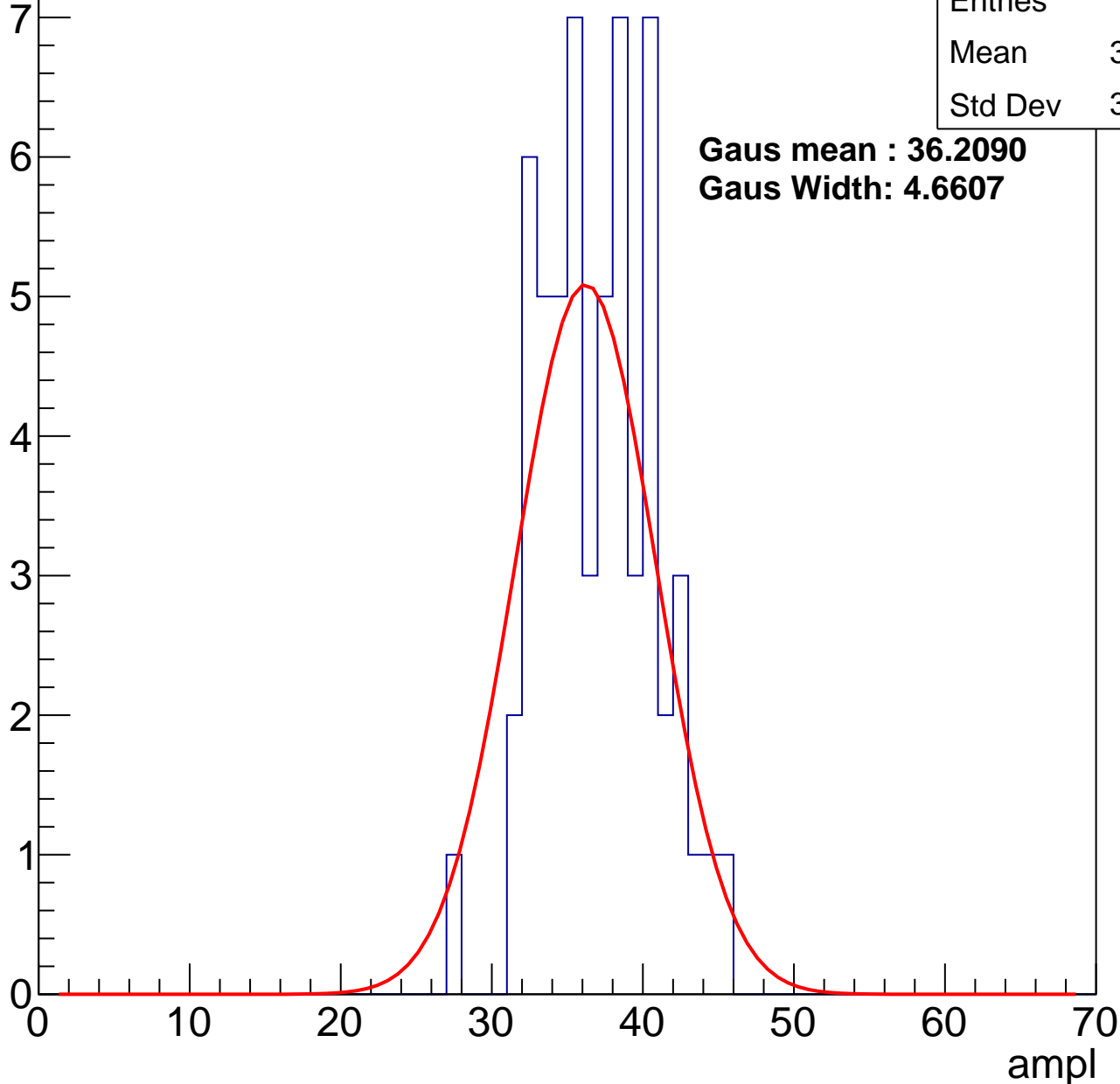
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	36.56
Std Dev	3.693

**Gaus mean : 36.2090**

**Gaus Width: 4.6607**



# B1L102S, U20-ch104, adc2

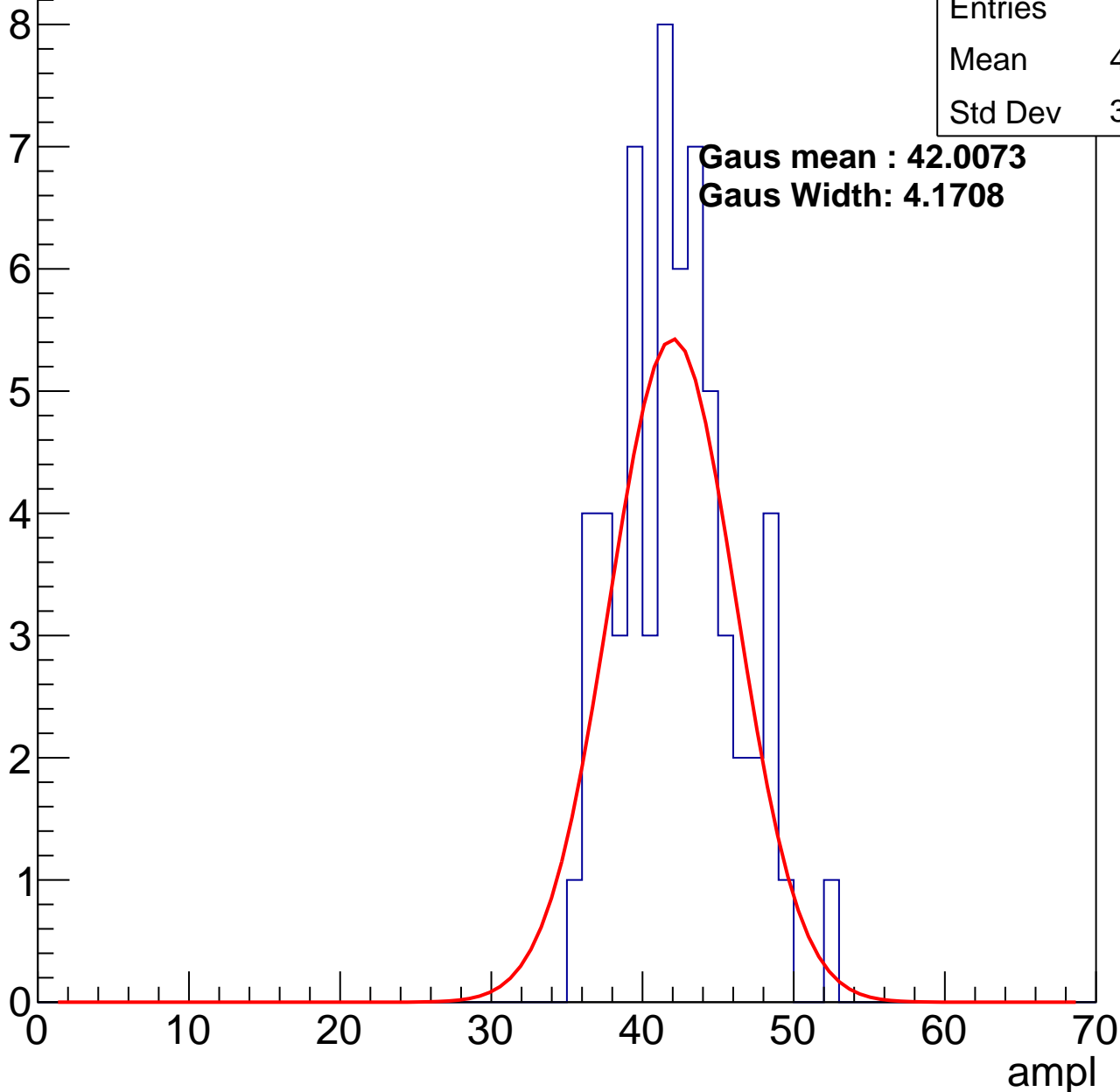
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	41.79
Std Dev	3.733

**Gaus mean : 42.0073**

**Gaus Width: 4.1708**

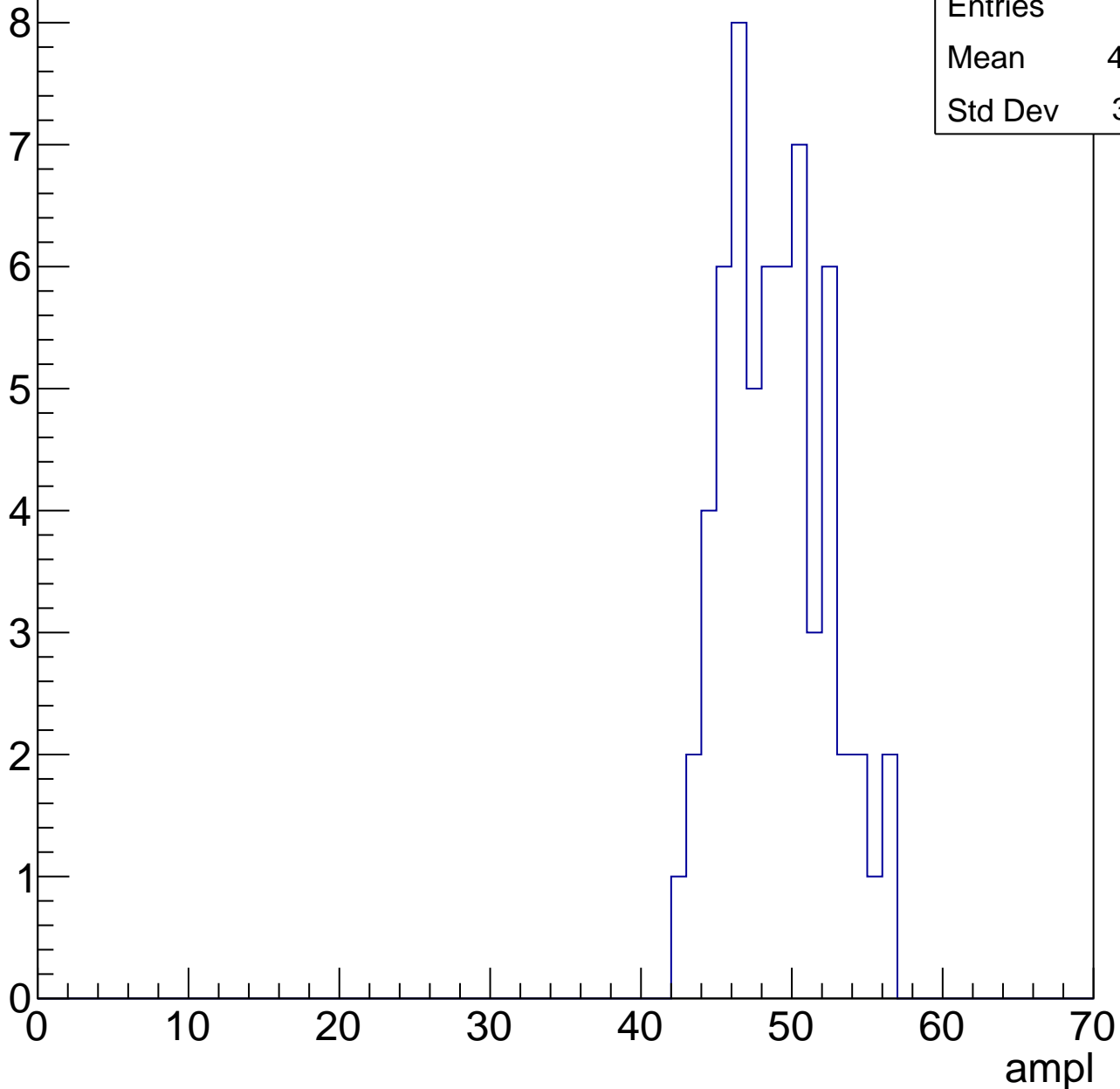


# B1L102S, U20-ch104, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	48.44
Std Dev	3.351

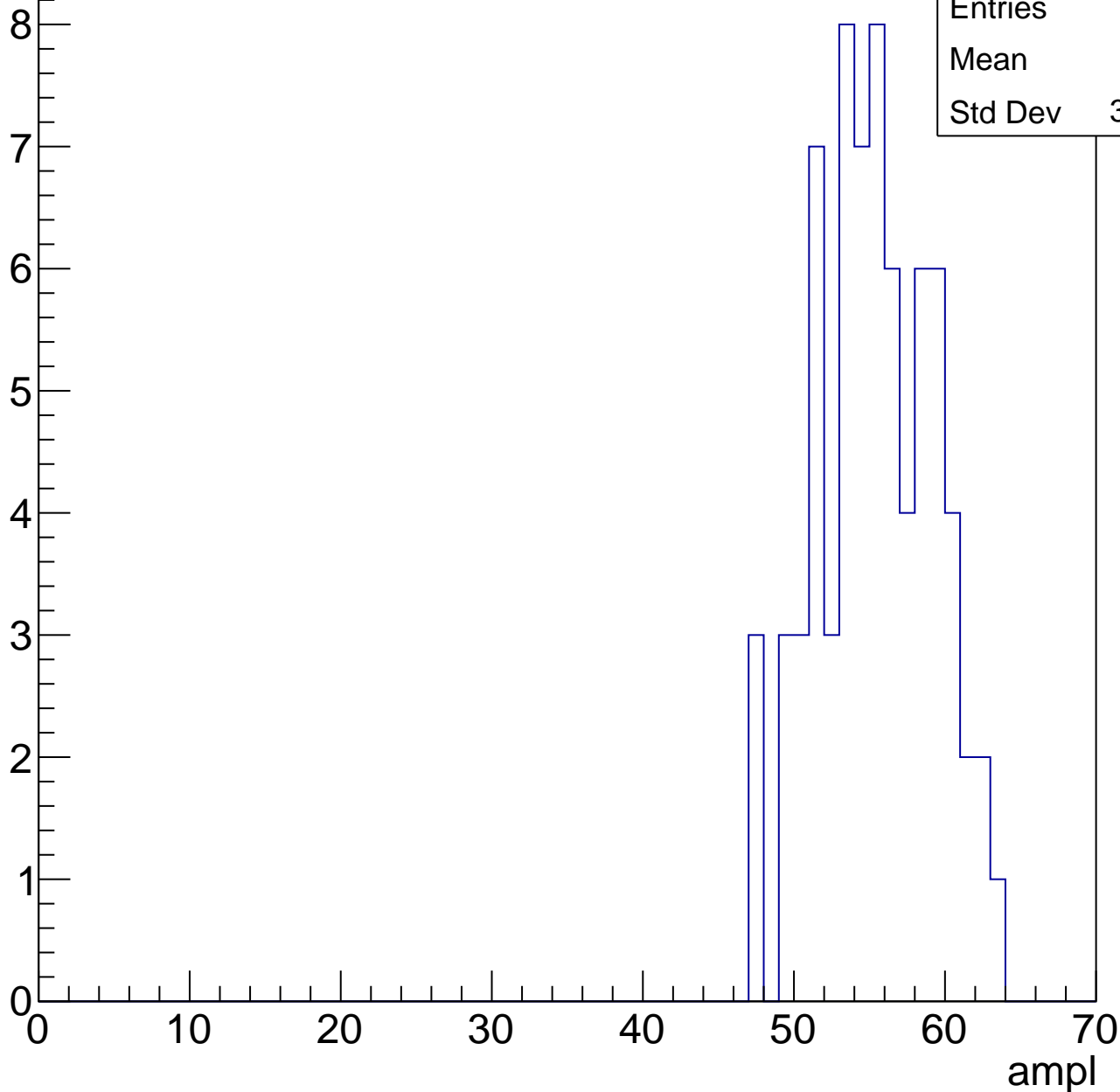


# B1L102S, U20-ch104, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	54.9
Std Dev	3.808

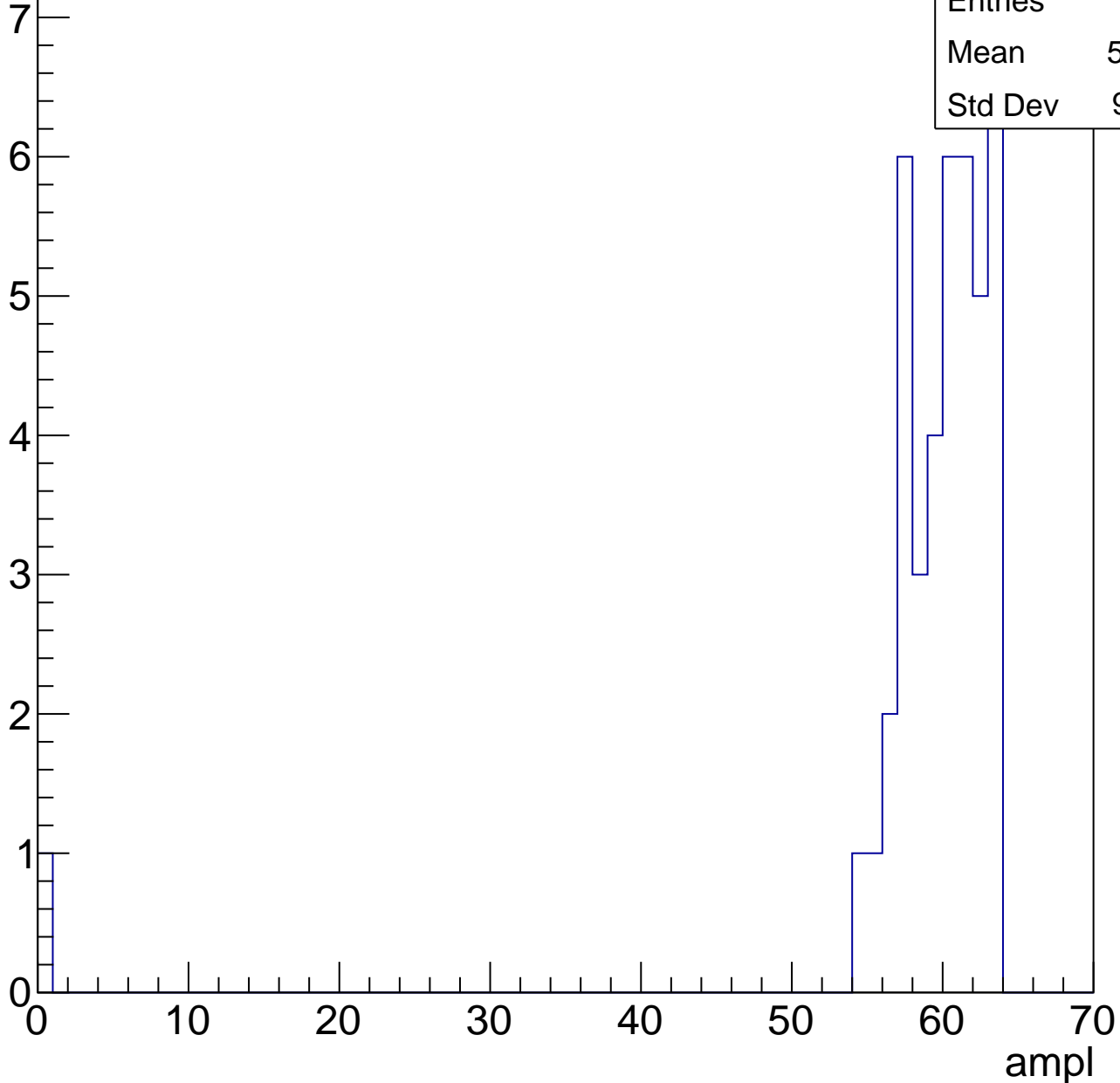


# B1L102S, U20-ch104, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

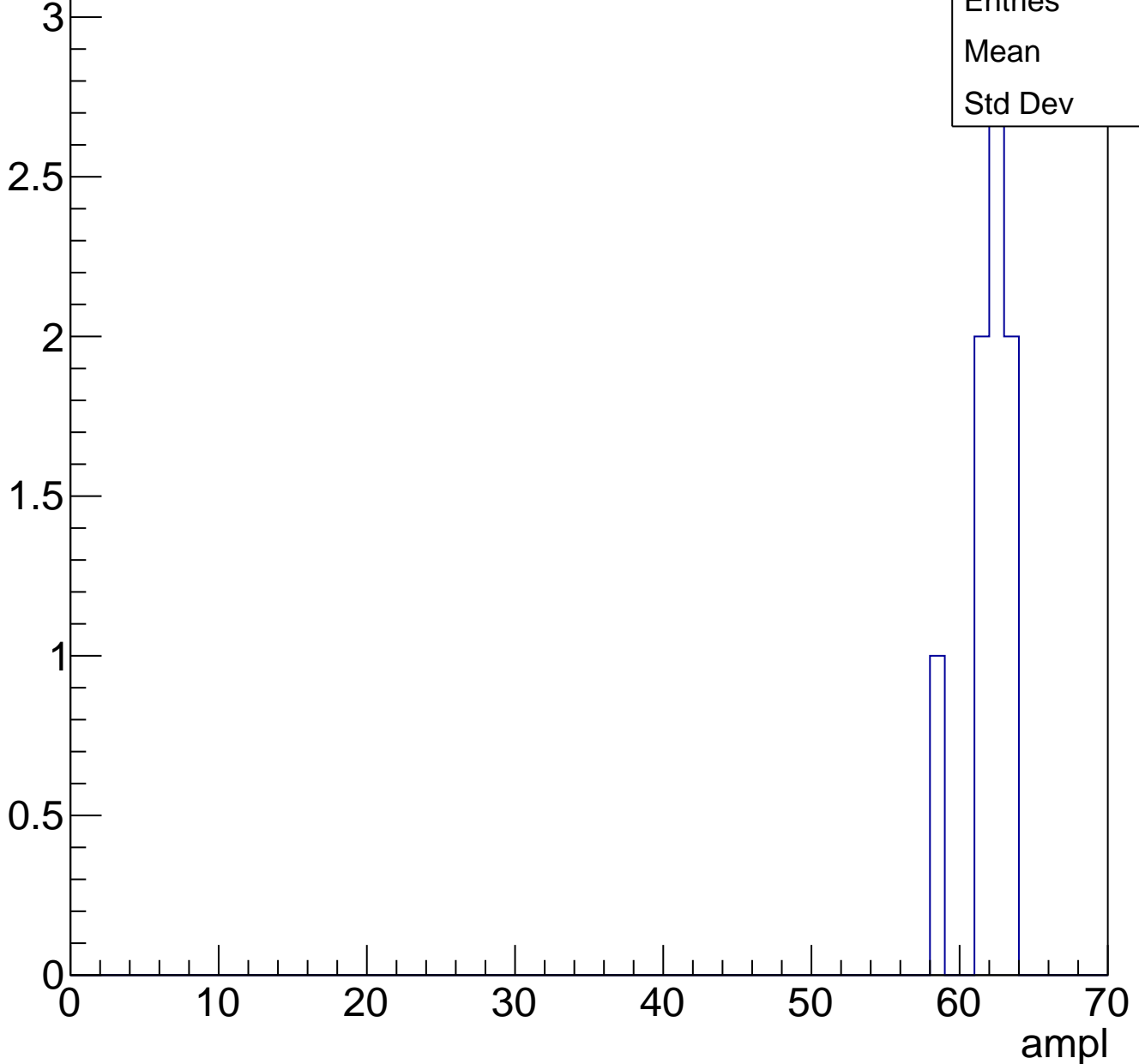
Entries	42
Mean	58.33
Std Dev	9.431



# B1L102S, U20-ch104, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U20-ch104, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U20-ch105, adc0

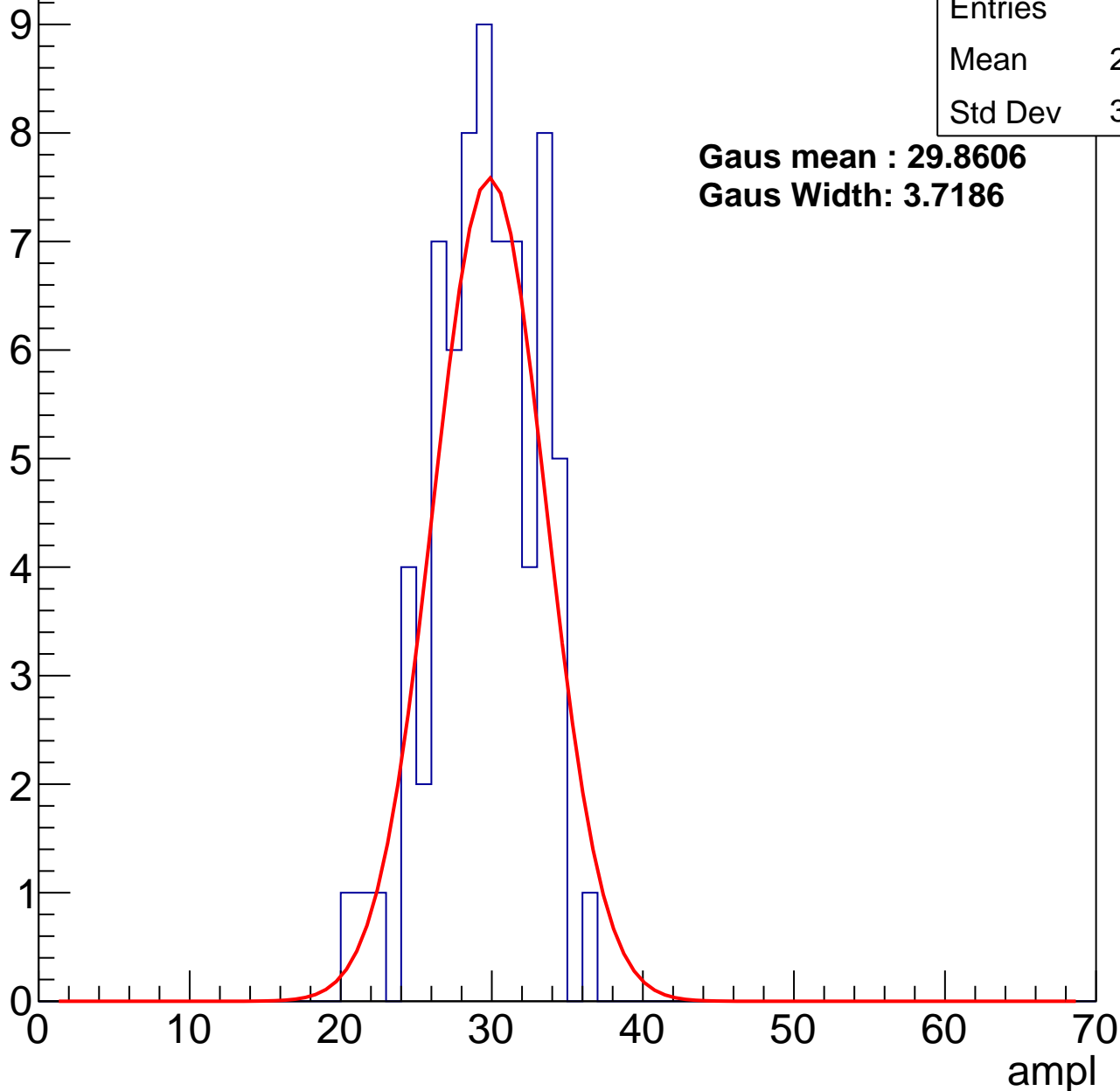
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	29.06
Std Dev	3.344

**Gaus mean : 29.8606**

**Gaus Width: 3.7186**



# B1L102S, U20-ch105, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	61
Mean	36
Std Dev	2.959

**Gaus mean : 36.6691**

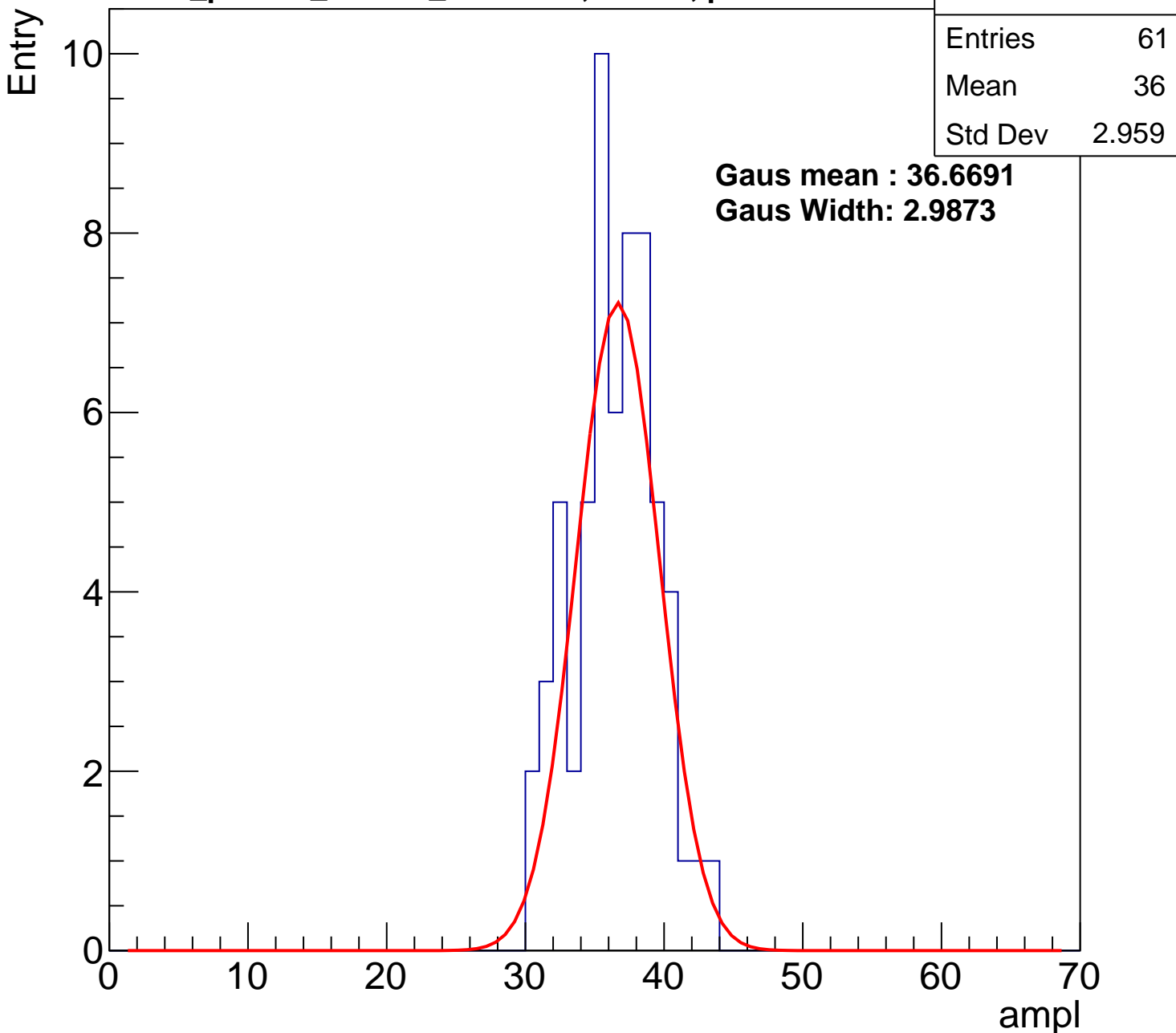
**Gaus Width: 2.9873**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U20-ch105, adc2

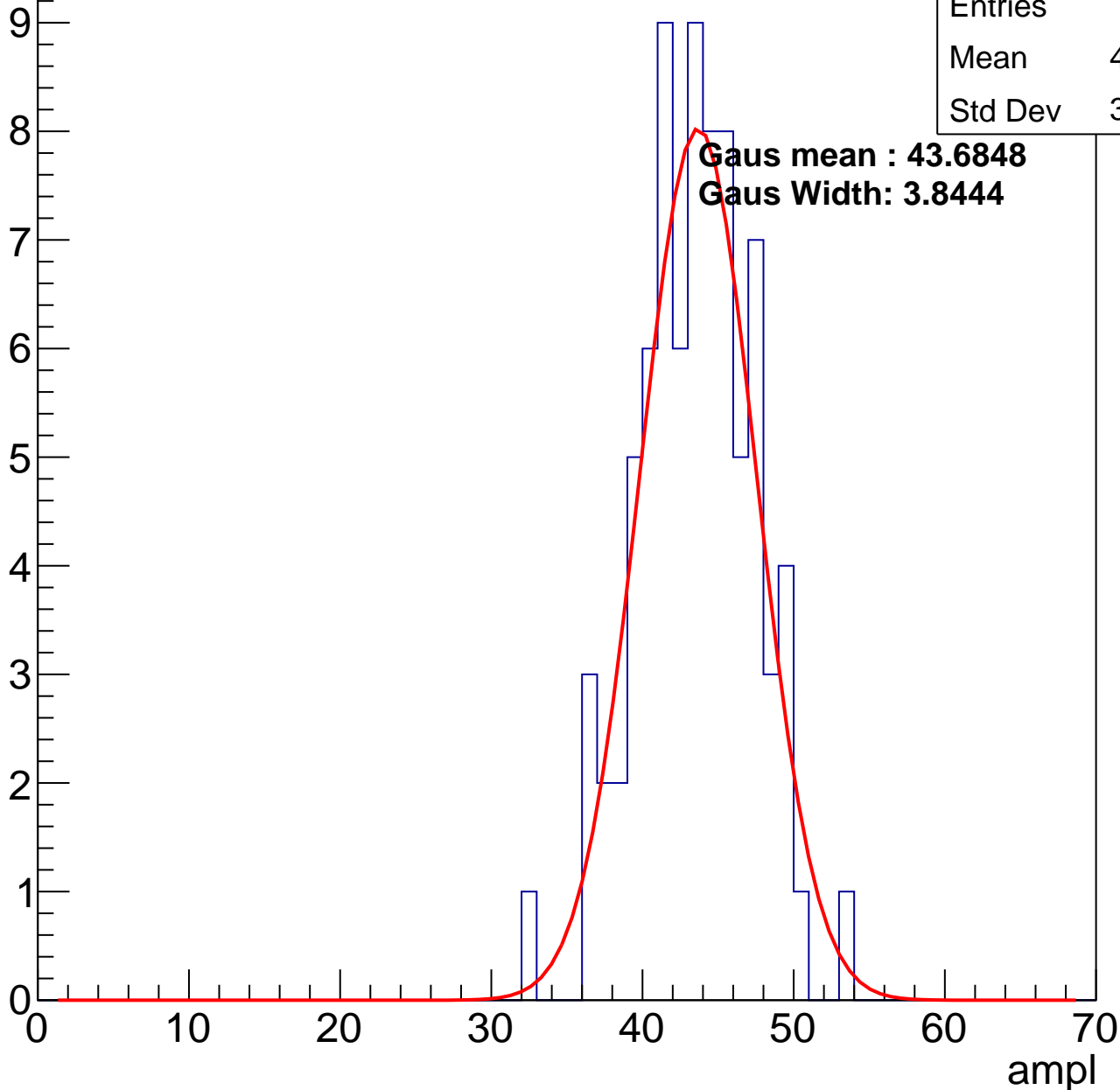
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	80
Mean	43.09
Std Dev	3.759

**Gaus mean : 43.6848**

**Gaus Width: 3.8444**



# B1L102S, U20-ch105, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

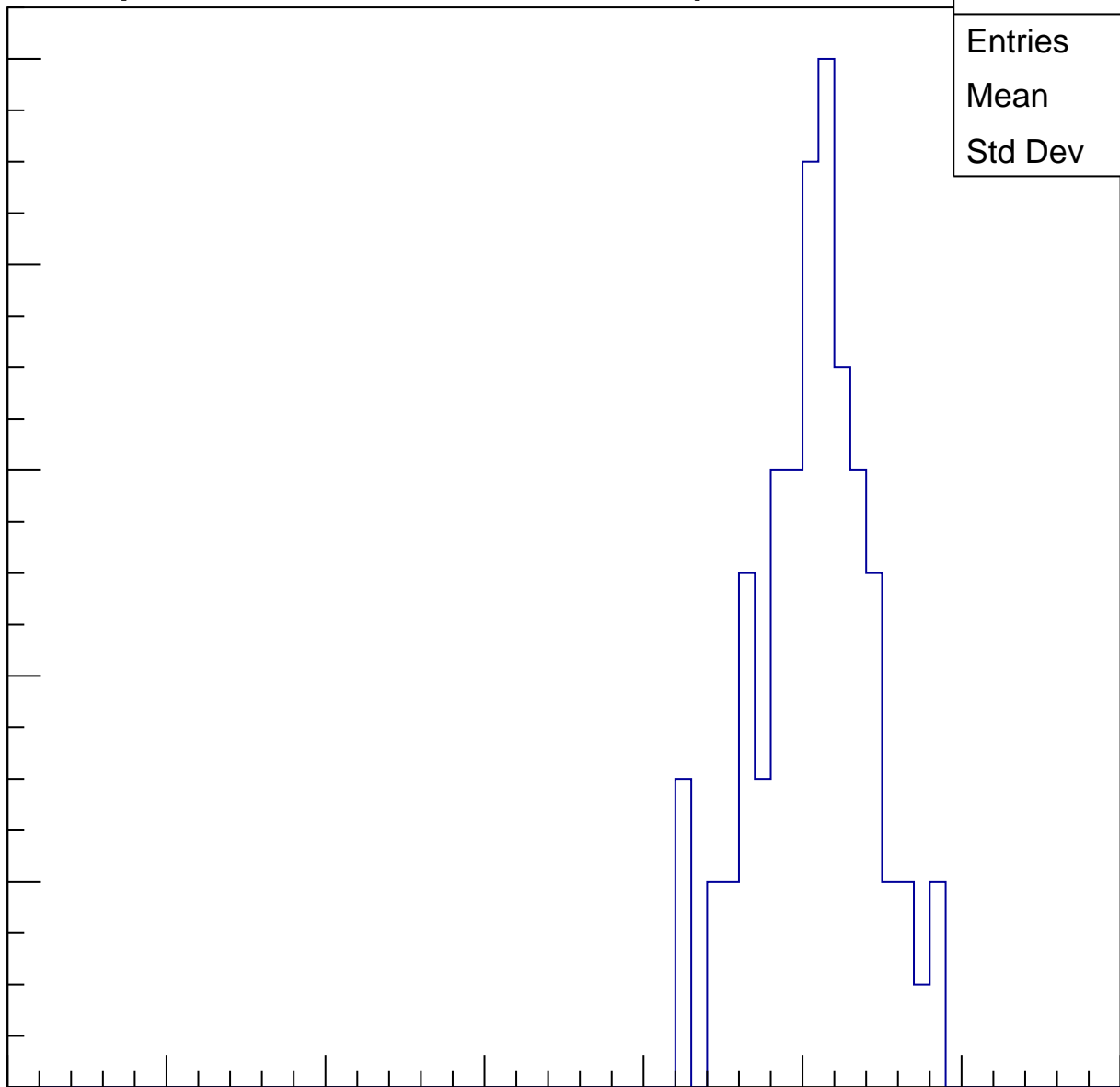
Entries	71
Mean	50.2
Std Dev	3.598

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

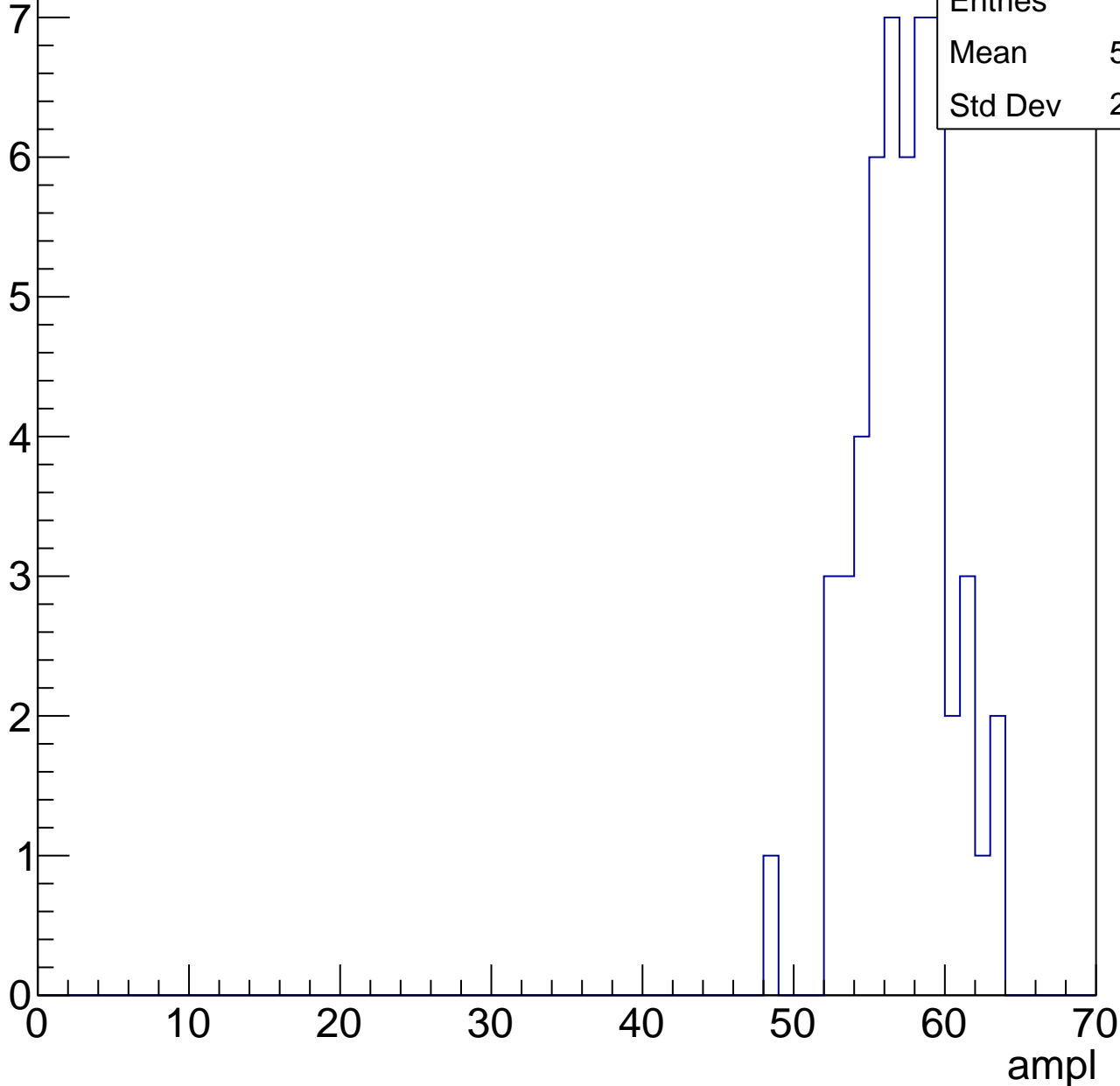


# B1L102S, U20-ch105, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	56.79
Std Dev	2.996



# B1L102S, U20-ch105, adc5

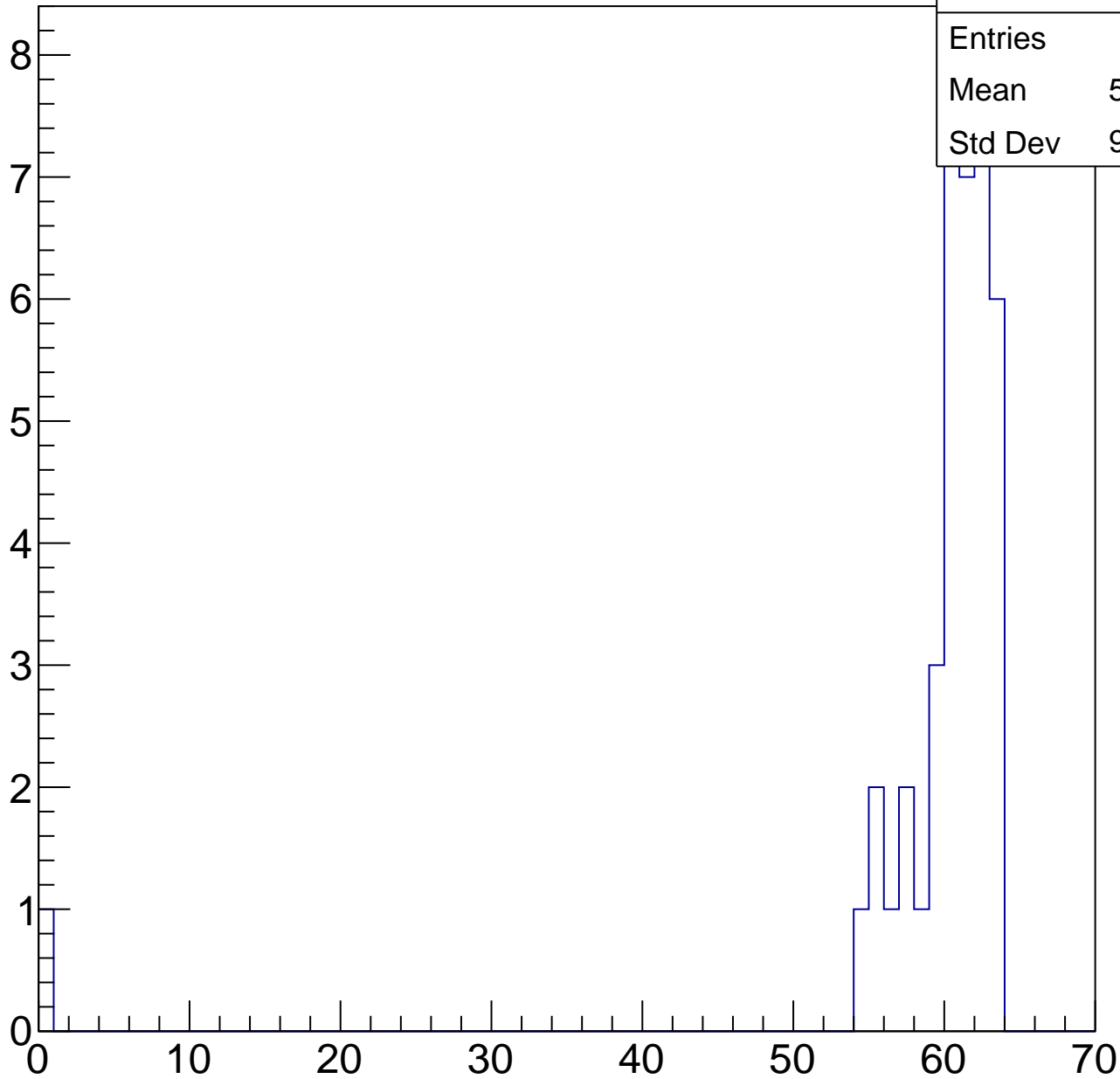
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	40
Mean	58.75
Std Dev	9.692

ampl



# B1L102S, U20-ch105, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

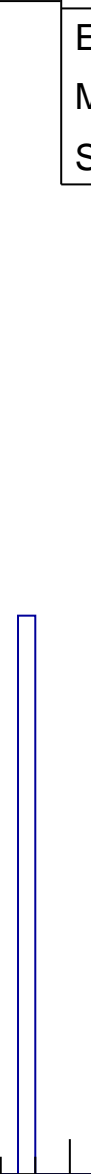
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	61.25
Std Dev	2.487

0 10 20 30 40 50 60 70

ampl





# B1L102S, U20-ch105, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U20-ch106, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	77
Mean	28.09
Std Dev	6.018

**Gaus mean : 29.4029**

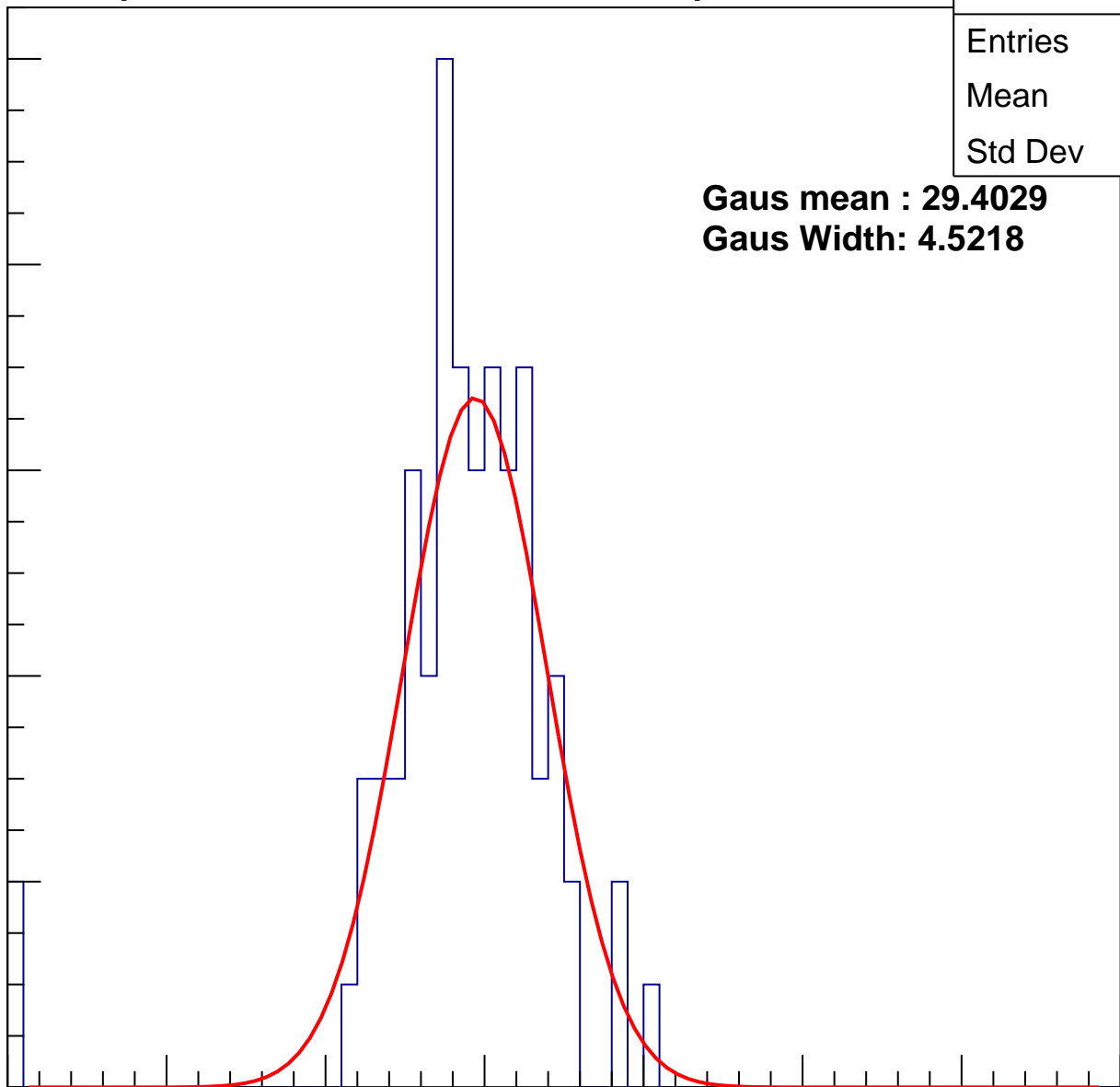
**Gaus Width: 4.5218**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U20-ch106, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	69
Mean	36.26
Std Dev	4.01

**Gaus mean : 36.4074**

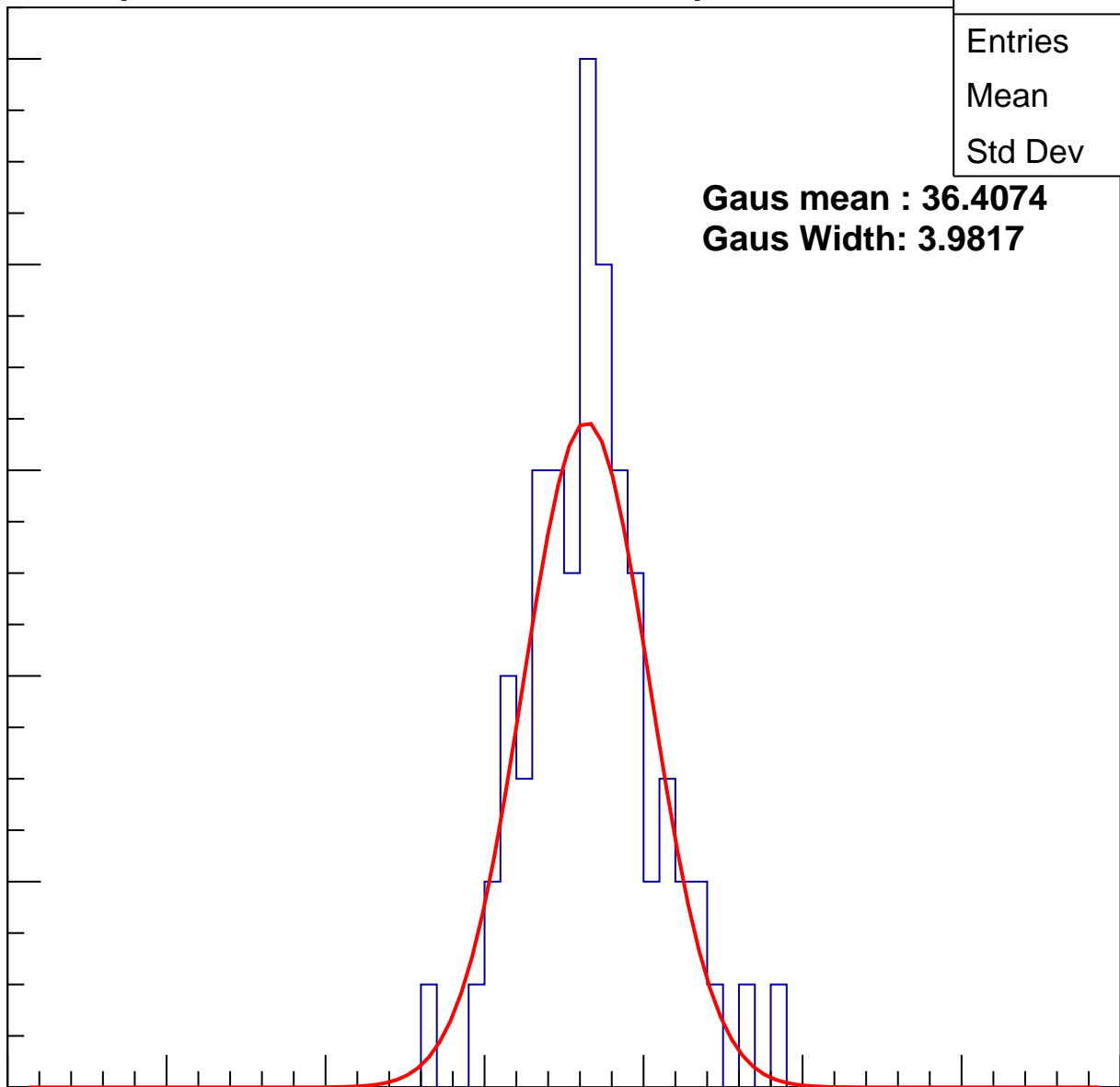
**Gaus Width: 3.9817**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U20-ch106, adc2

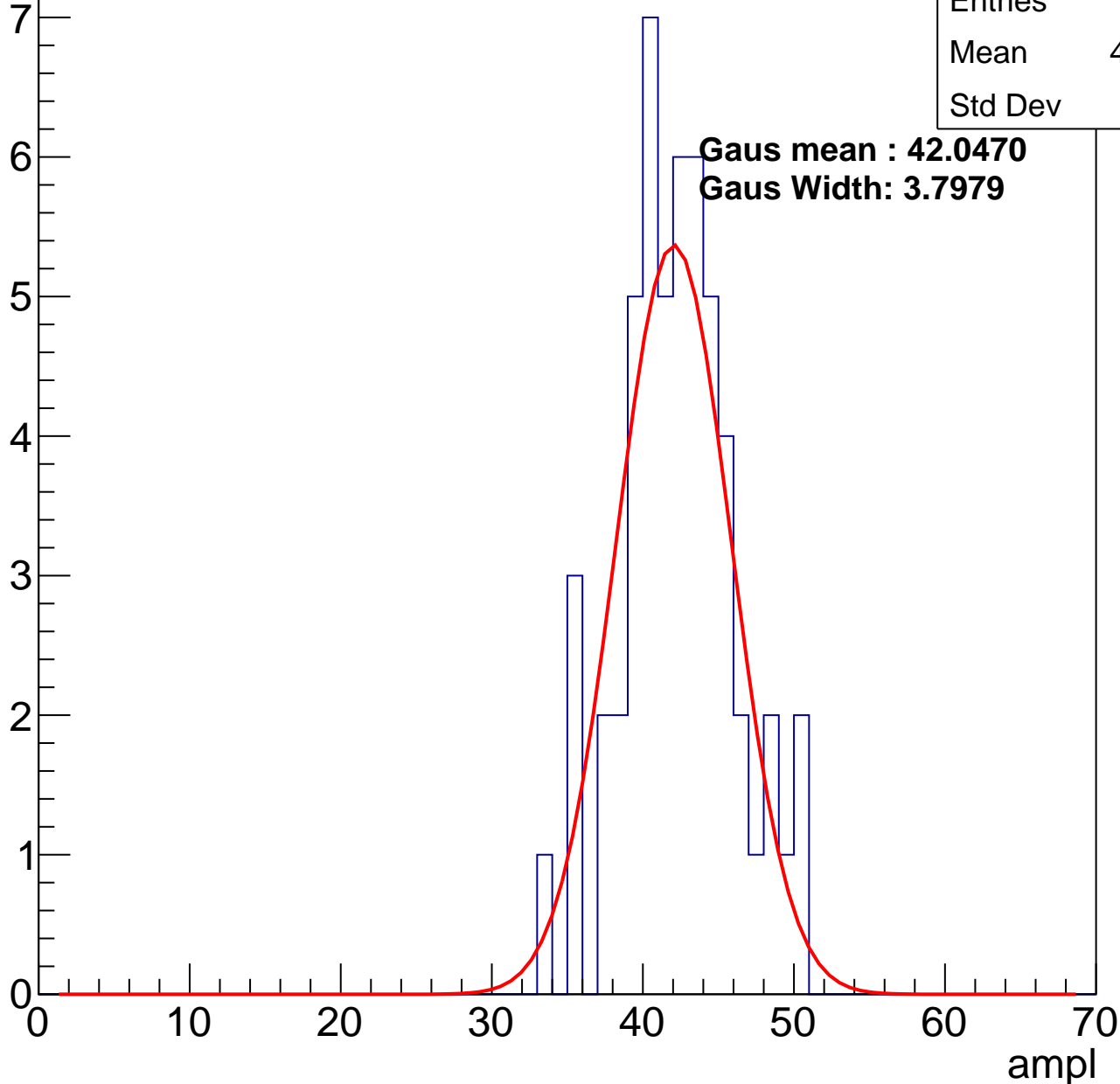
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	41.89
Std Dev	3.74

**Gaus mean : 42.0470**

**Gaus Width: 3.7979**

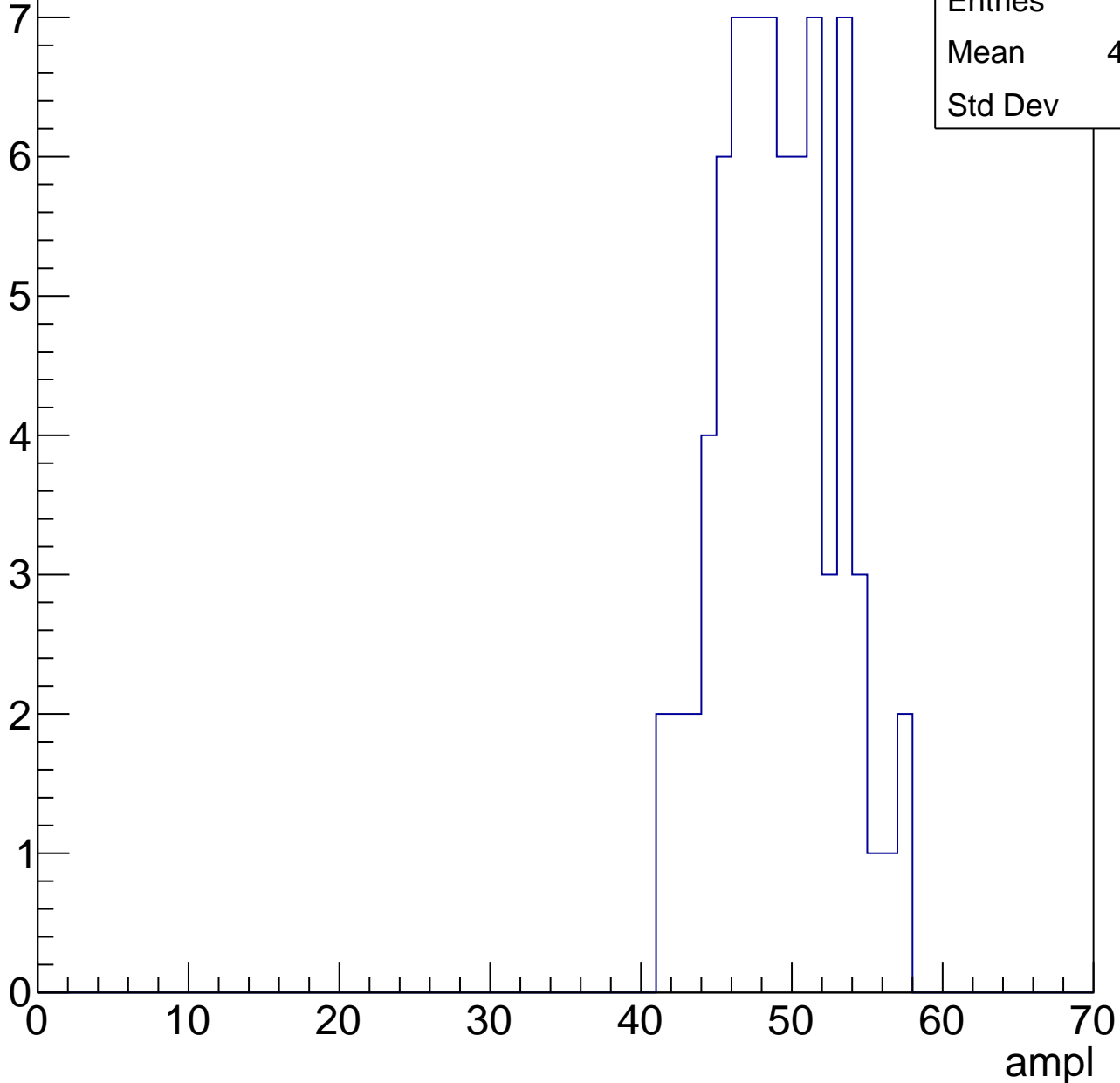


# B1L102S, U20-ch106, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	48.63
Std Dev	3.78

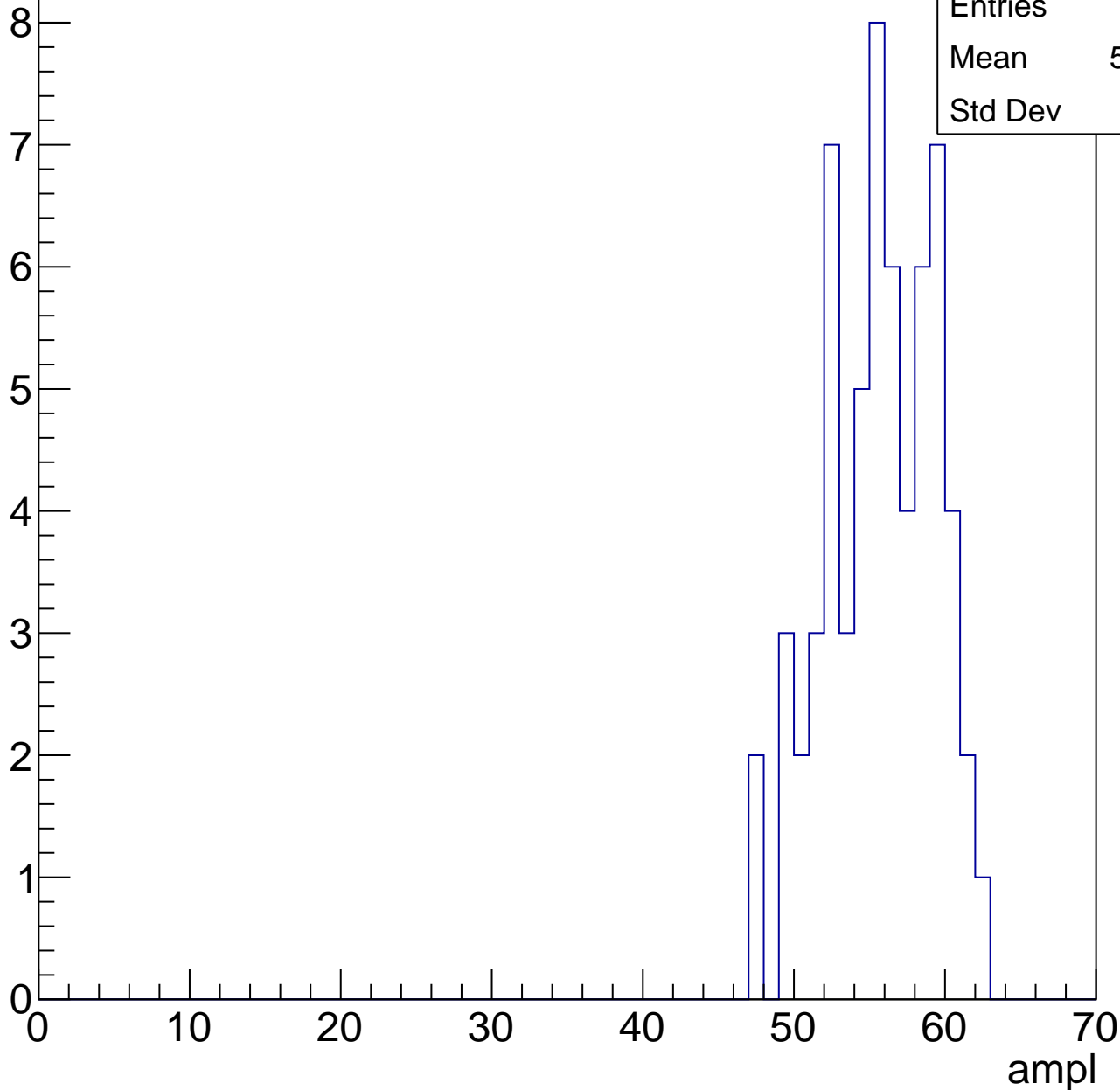


# B1L102S, U20-ch106, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	55.17
Std Dev	3.61

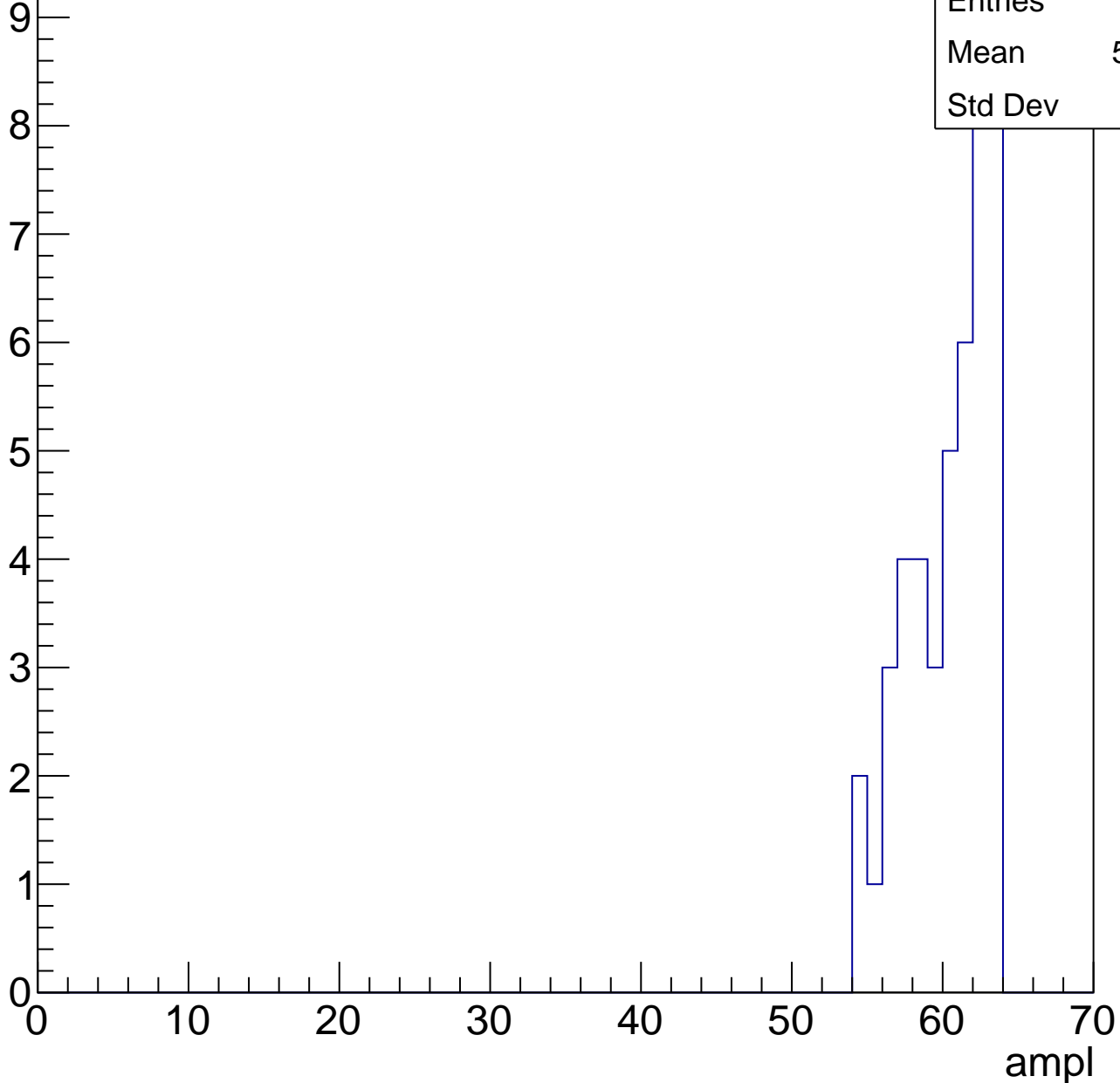


# B1L102S, U20-ch106, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	45
Mean	59.91
Std Dev	2.64



# B1L102S, U20-ch106, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	51.33
Std Dev	22.98

ampl

0 10 20 30 40 50 60 70



# B1L102S, U20-ch106, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L102S, U20-ch107, adc0

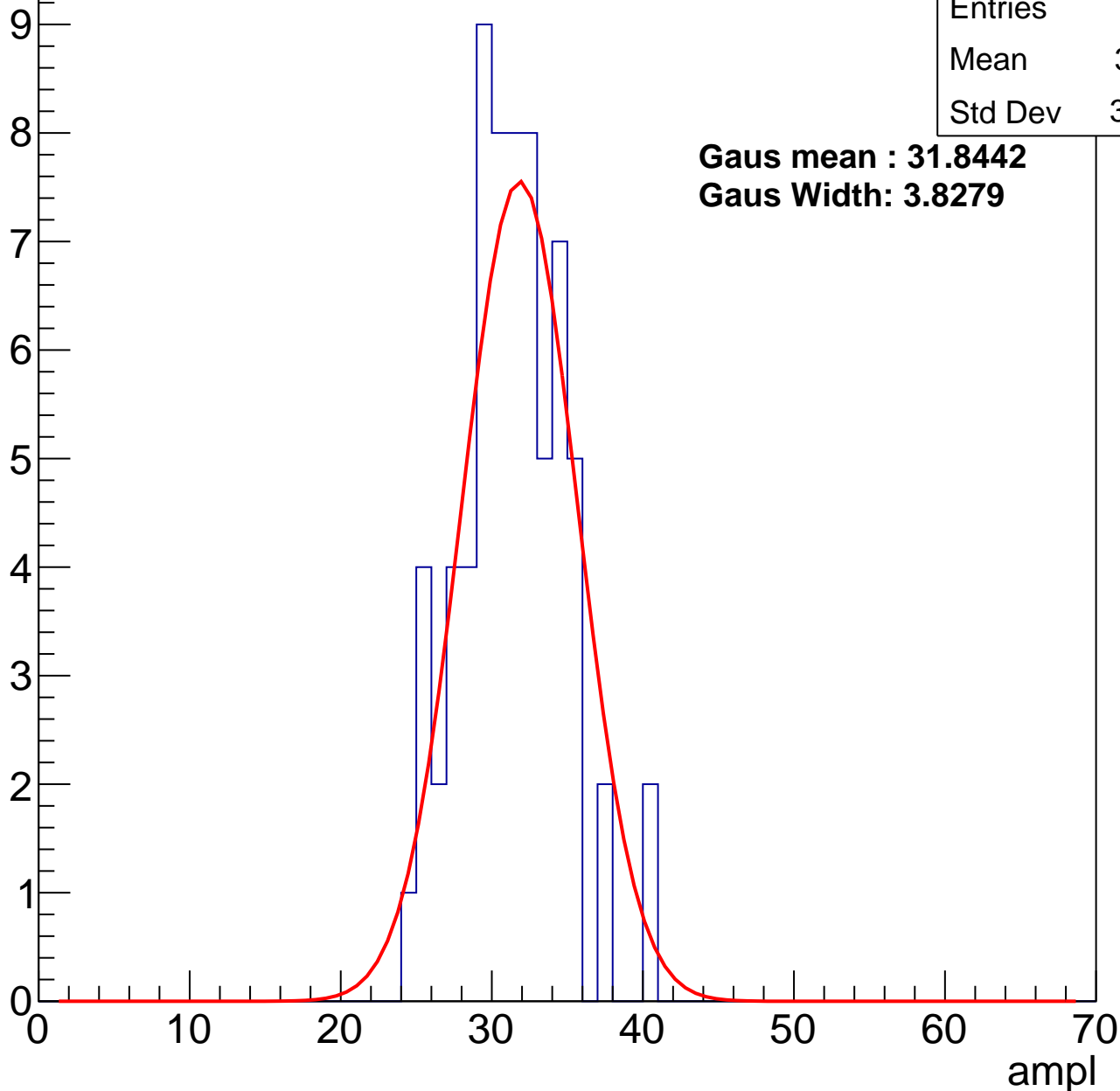
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	30.91
Std Dev	3.387

**Gaus mean : 31.8442**

**Gaus Width: 3.8279**



# B1L102S, U20-ch107, adc1

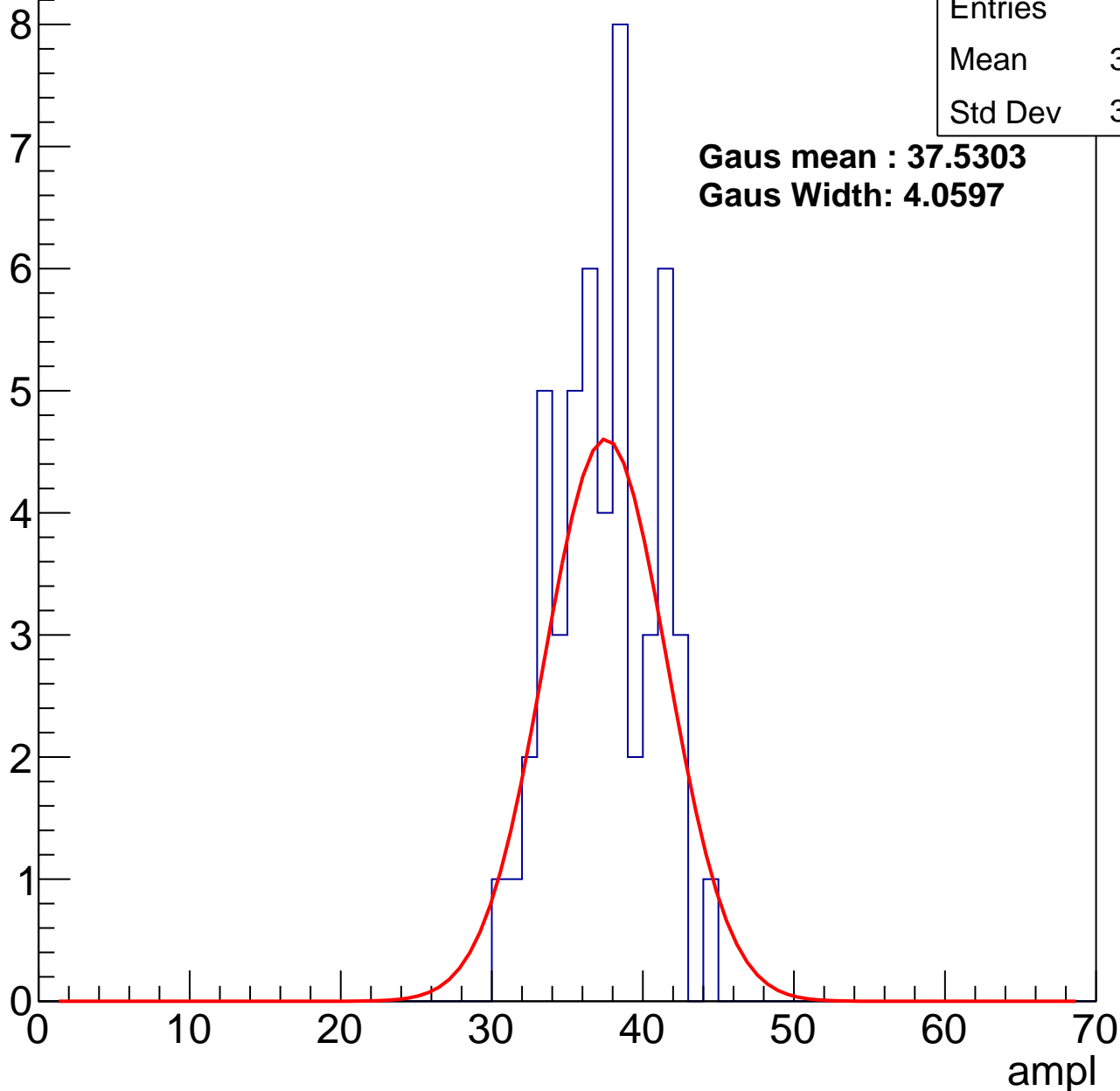
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	36.98
Std Dev	3.259

**Gaus mean : 37.5303**

**Gaus Width: 4.0597**



# B1L102S, U20-ch107, adc2

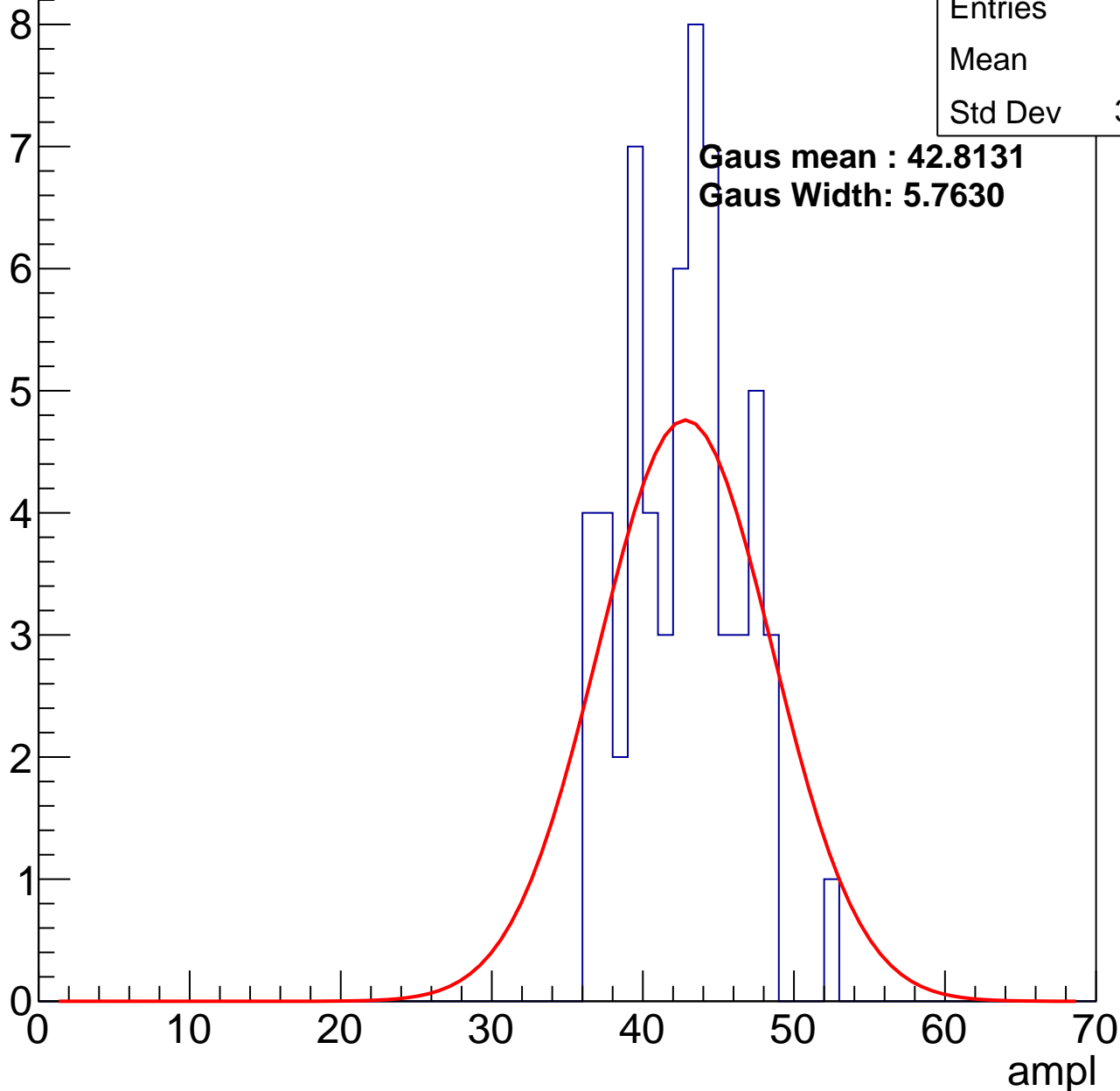
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	42.2
Std Dev	3.651

**Gaus mean : 42.8131**

**Gaus Width: 5.7630**



# B1L102S, U20-ch107, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

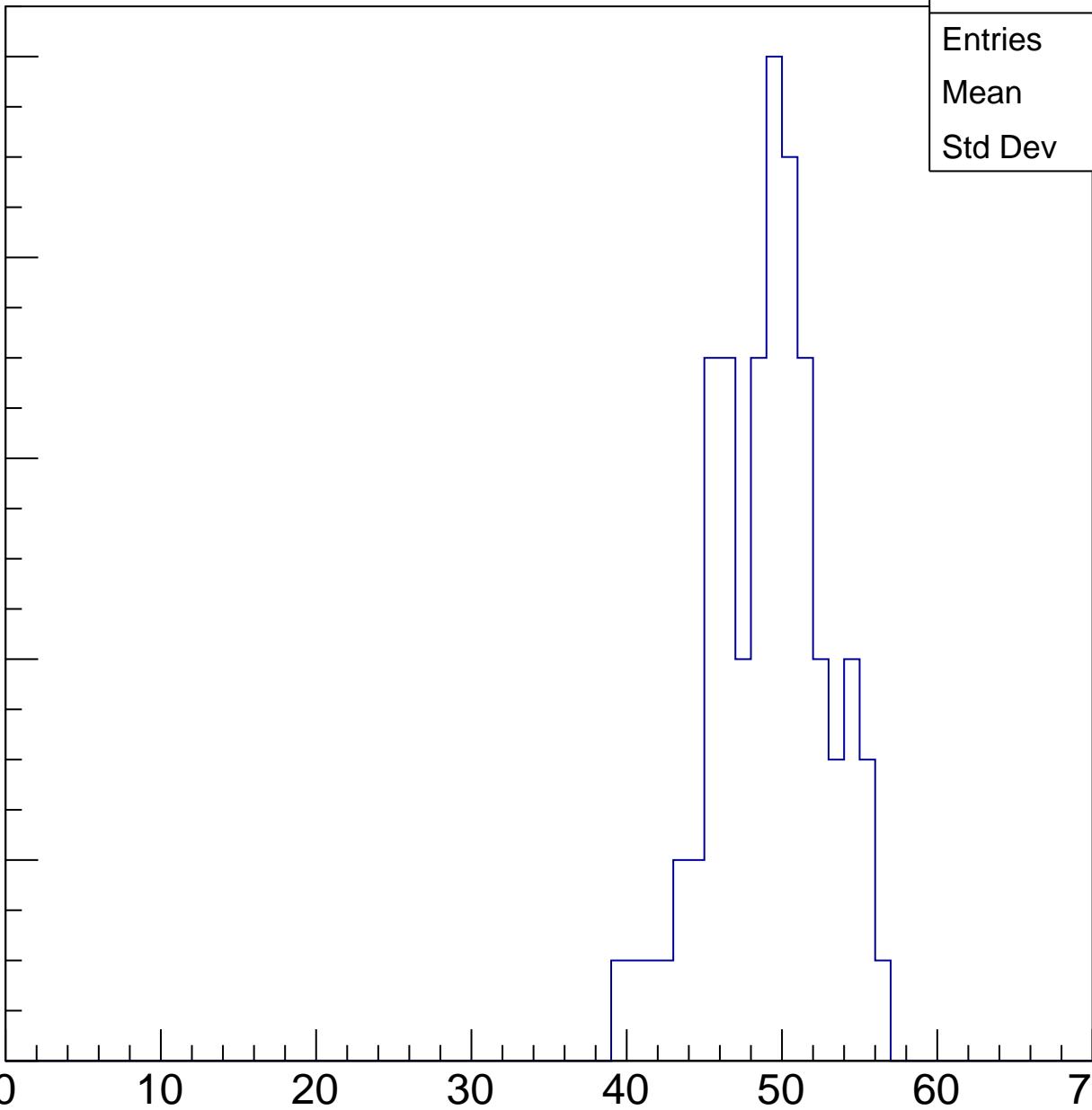
Entries	74
Mean	48.62
Std Dev	3.642

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

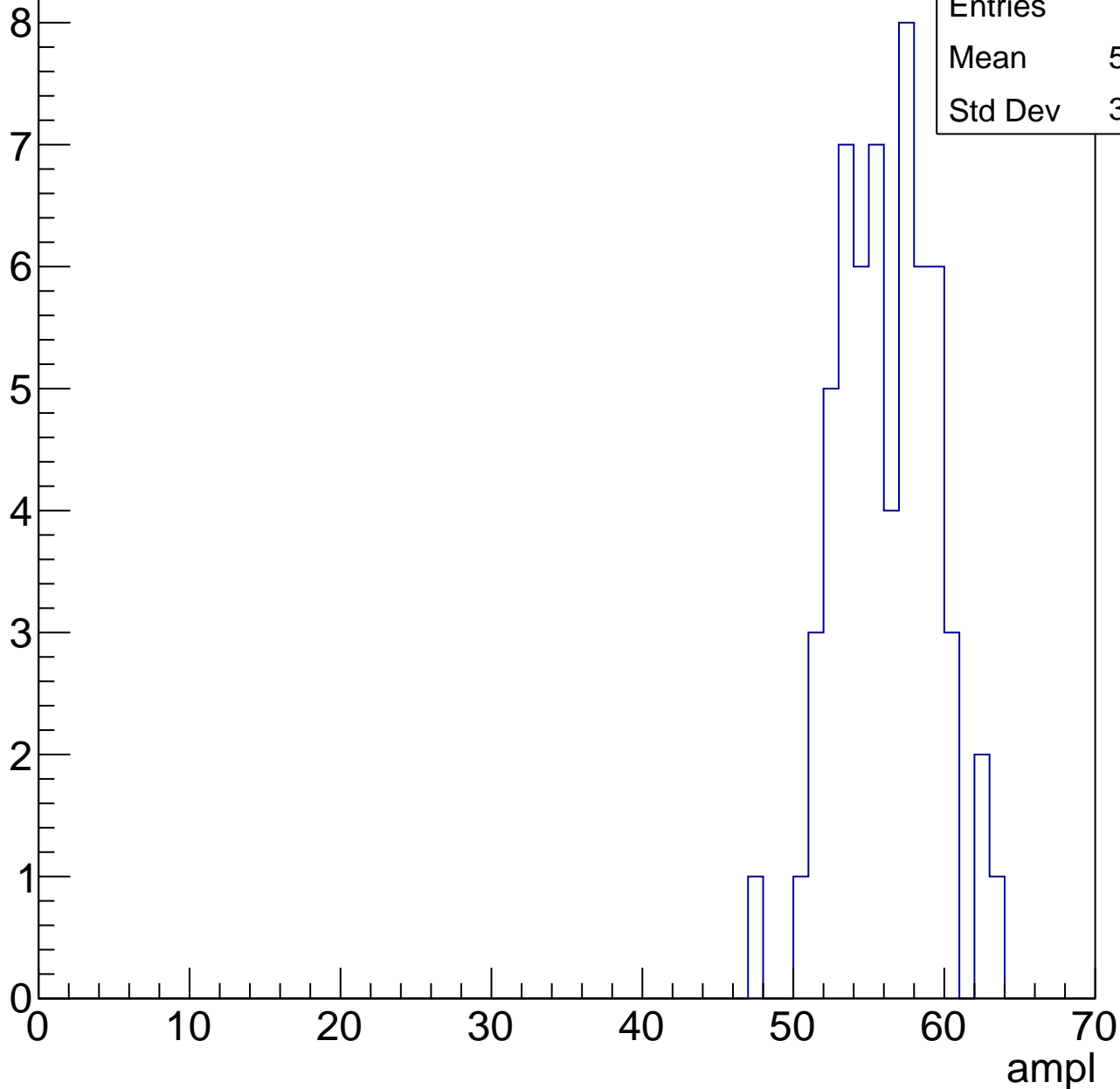


# B1L102S, U20-ch107, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	55.65
Std Dev	3.198

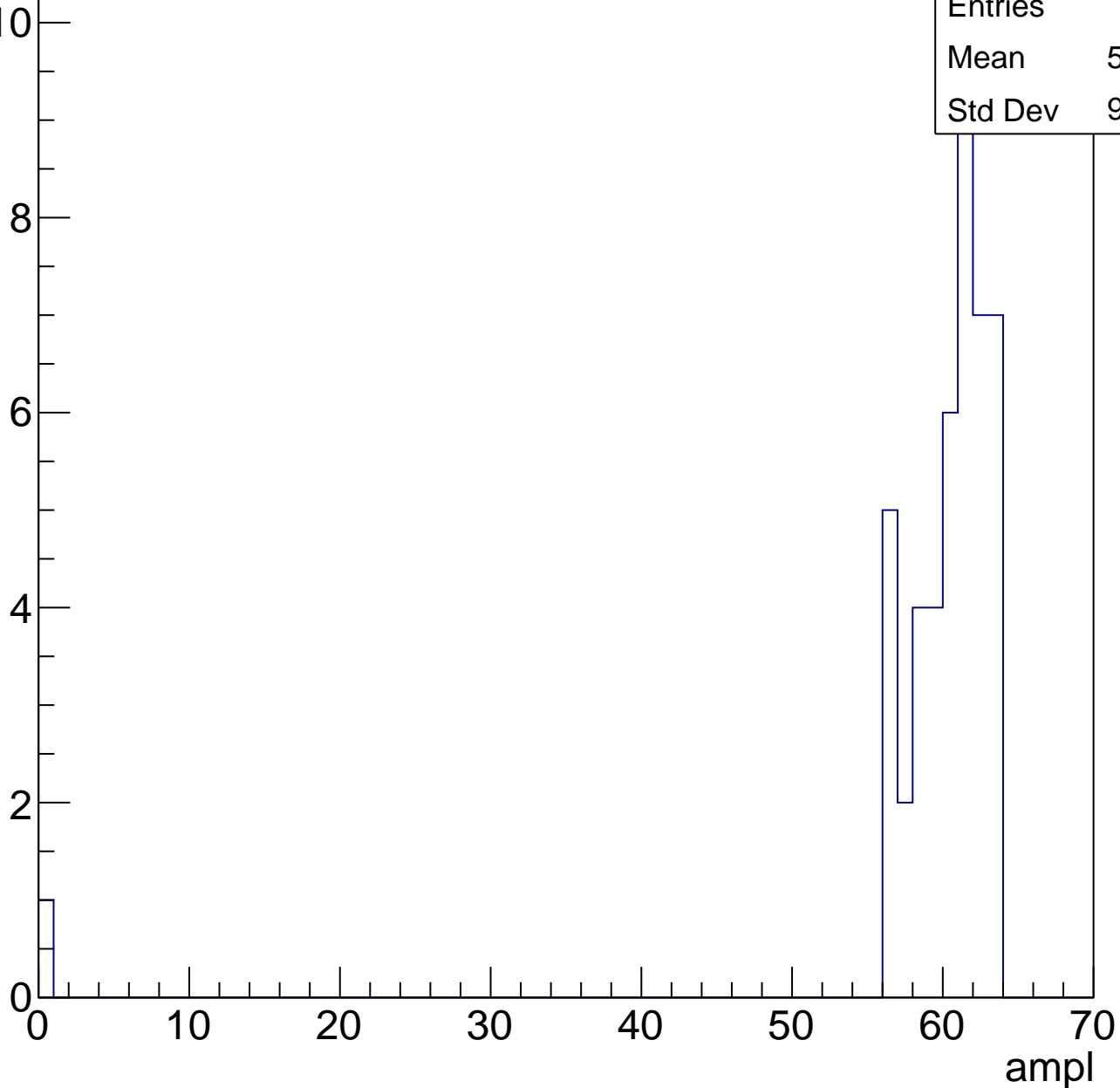


# B1L102S, U20-ch107, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	46
Mean	58.85
Std Dev	9.038



# B1L102S, U20-ch107, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	62
Std Dev	1.225

ampl

0 10 20 30 40 50 60 70



# B1L102S, U20-ch107, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch108, adc0

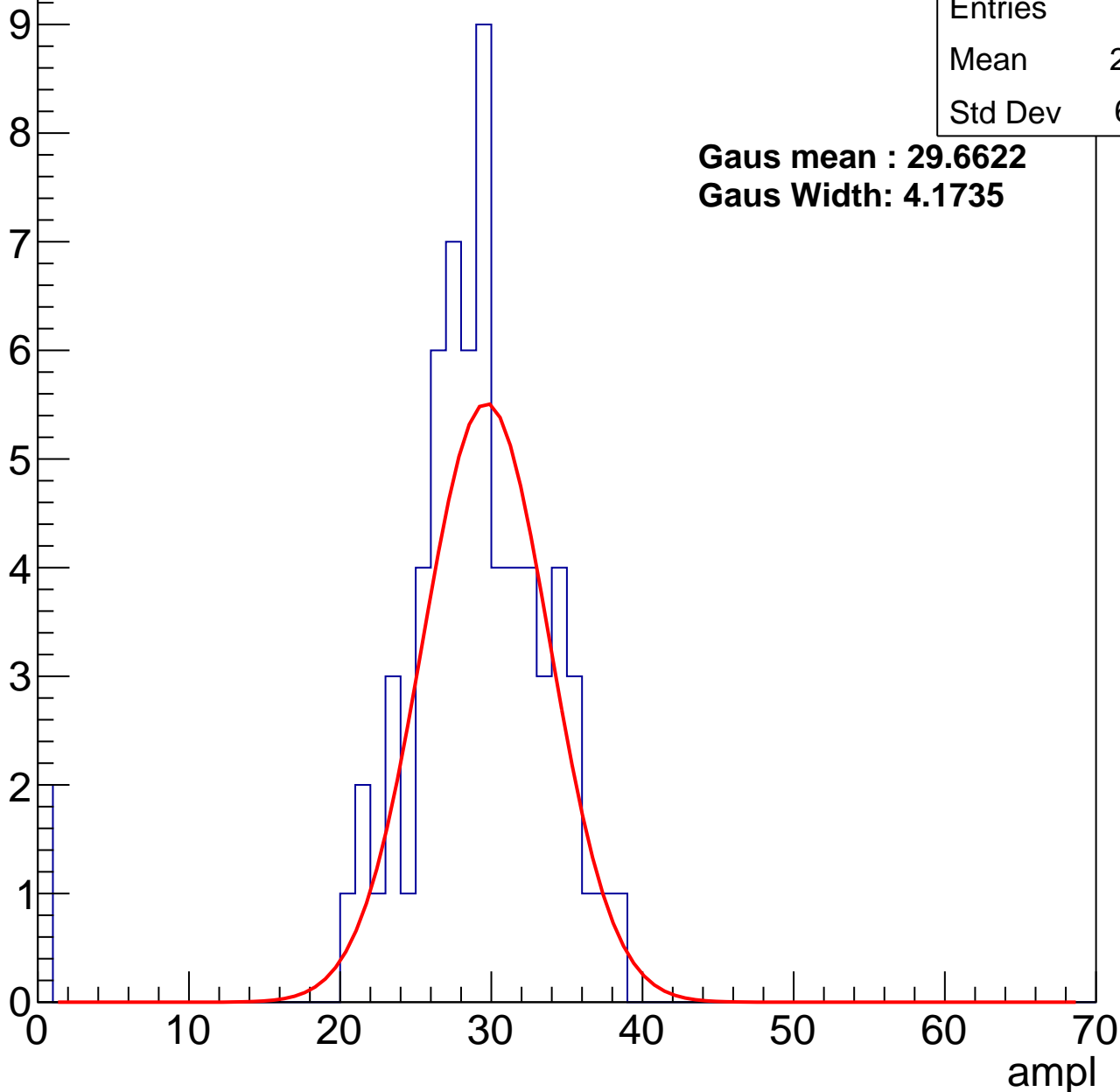
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	27.97
Std Dev	6.301

**Gaus mean : 29.6622**

**Gaus Width: 4.1735**



# B1L102S, U20-ch108, adc1

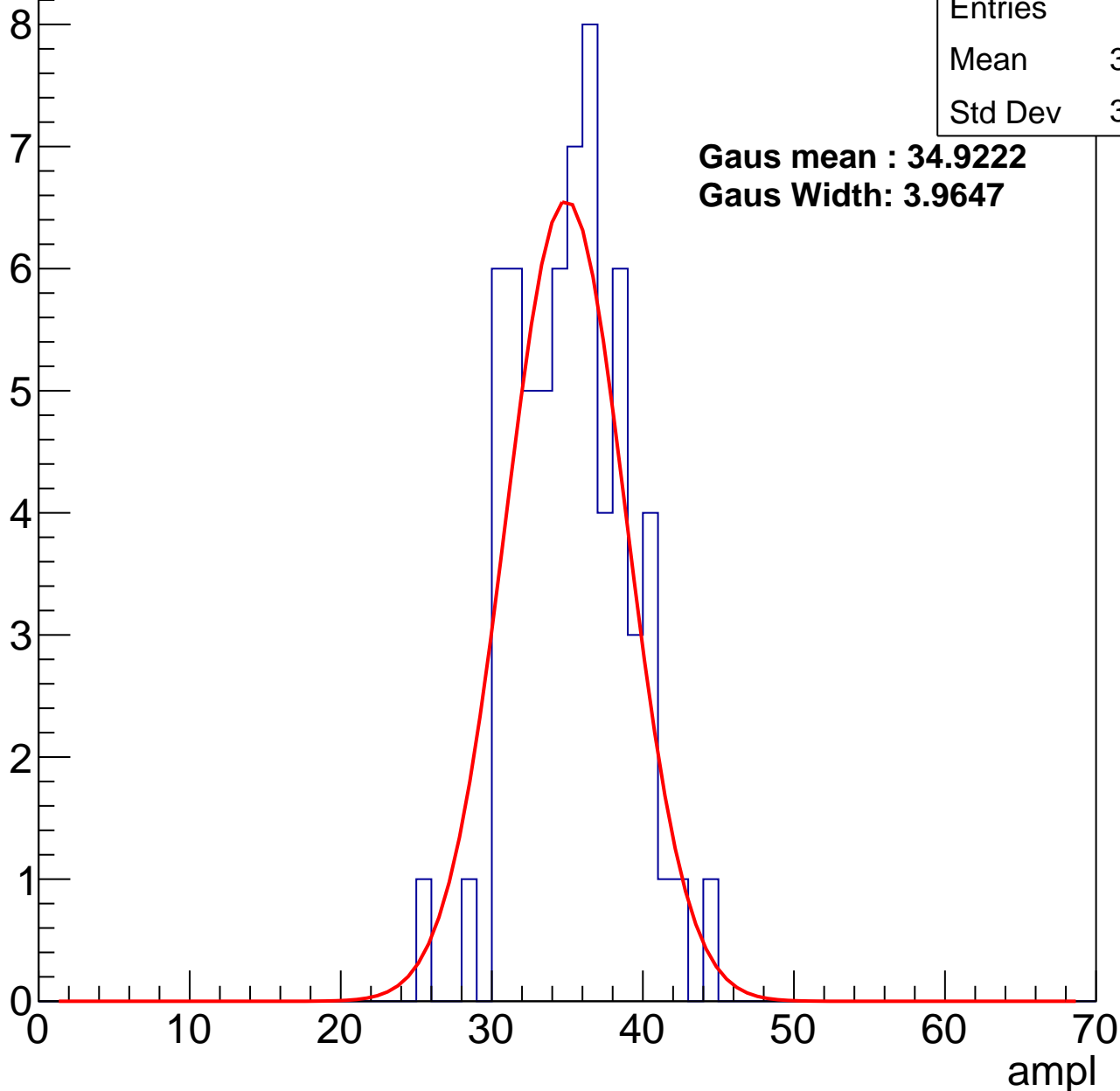
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	34.78
Std Dev	3.627

**Gaus mean : 34.9222**

**Gaus Width: 3.9647**



# B1L102S, U20-ch108, adc2

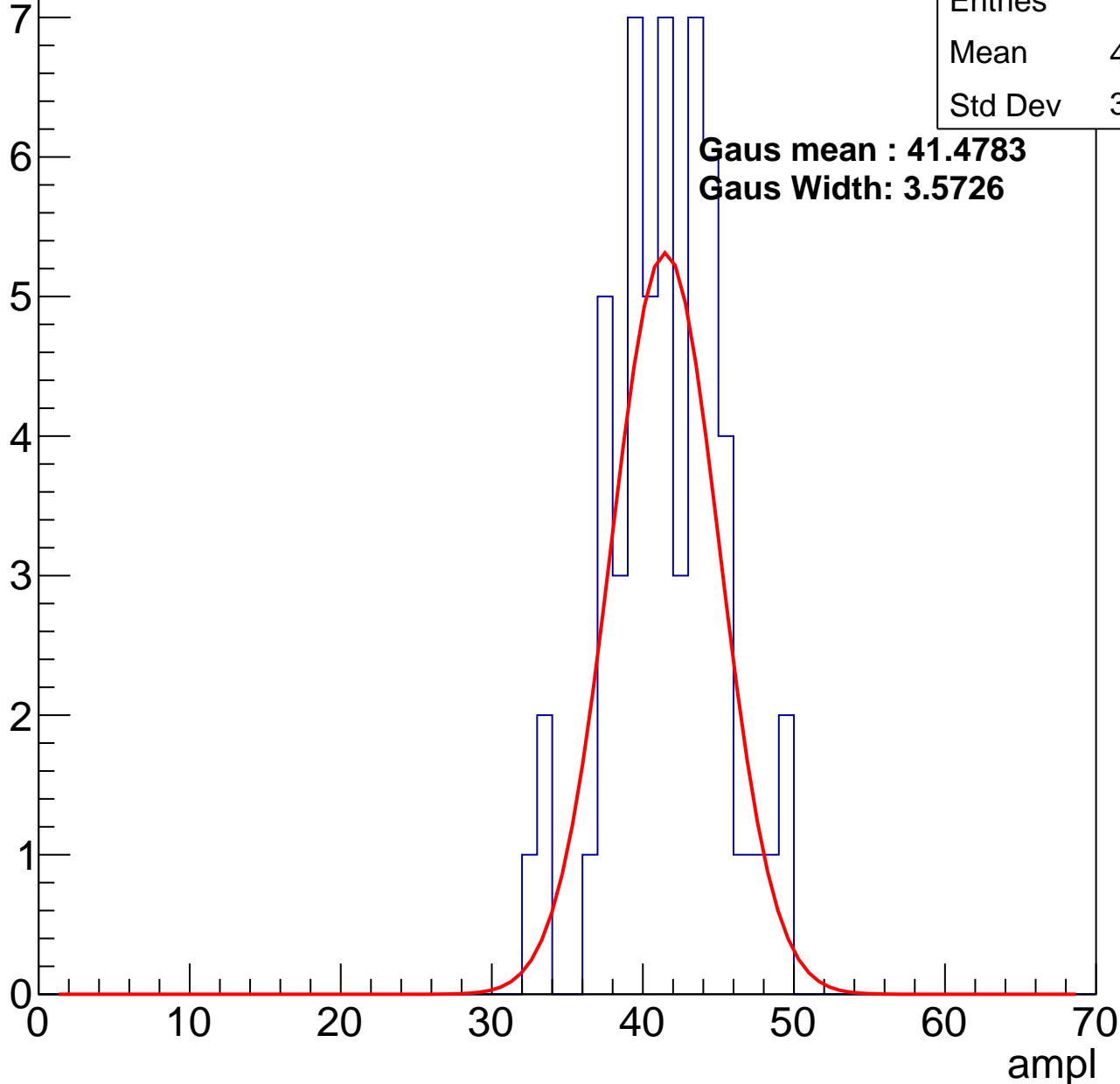
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	41.12
Std Dev	3.684

**Gaus mean : 41.4783**

**Gaus Width: 3.5726**

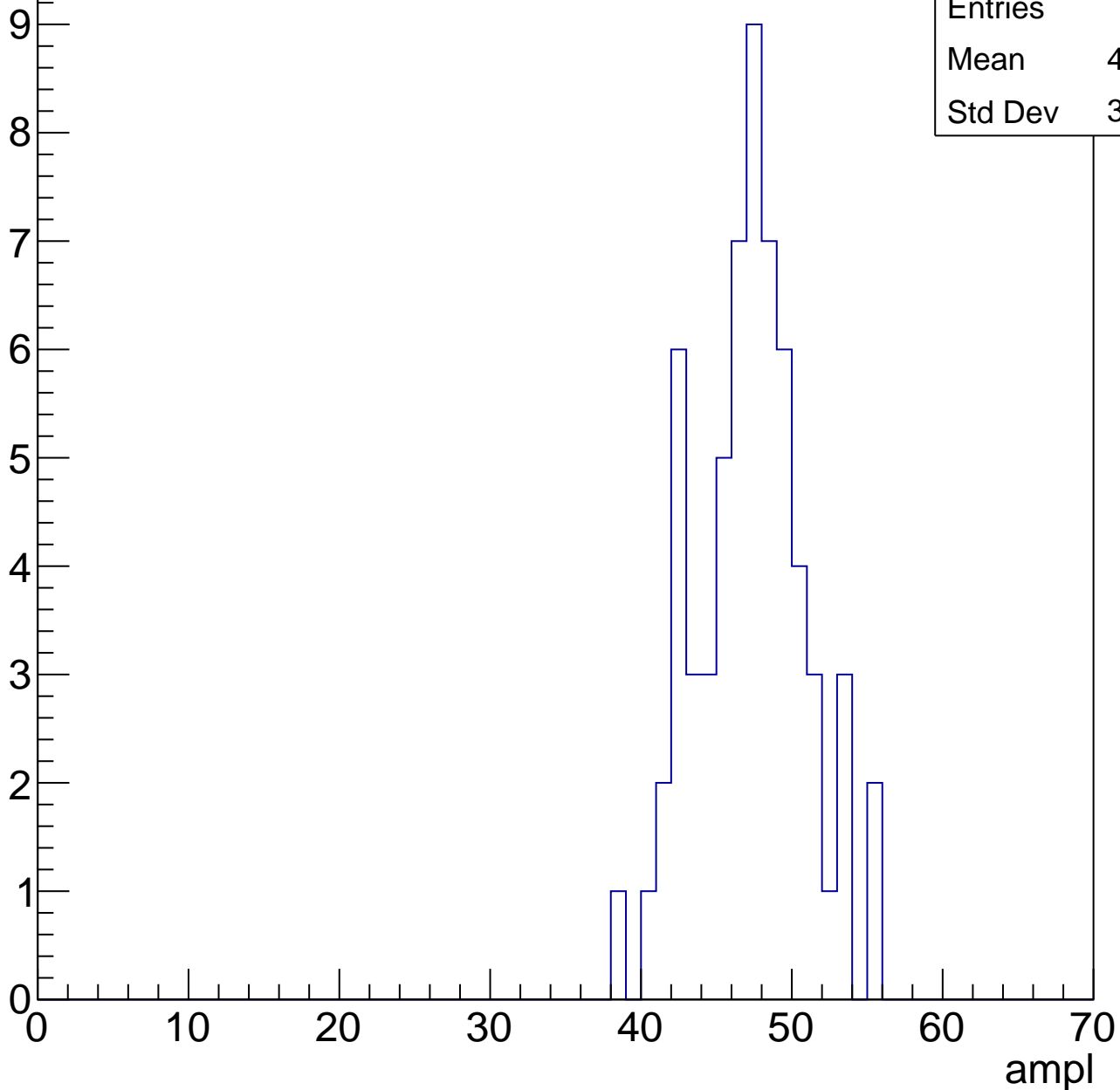


# B1L102S, U20-ch108, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	46.78
Std Dev	3.623

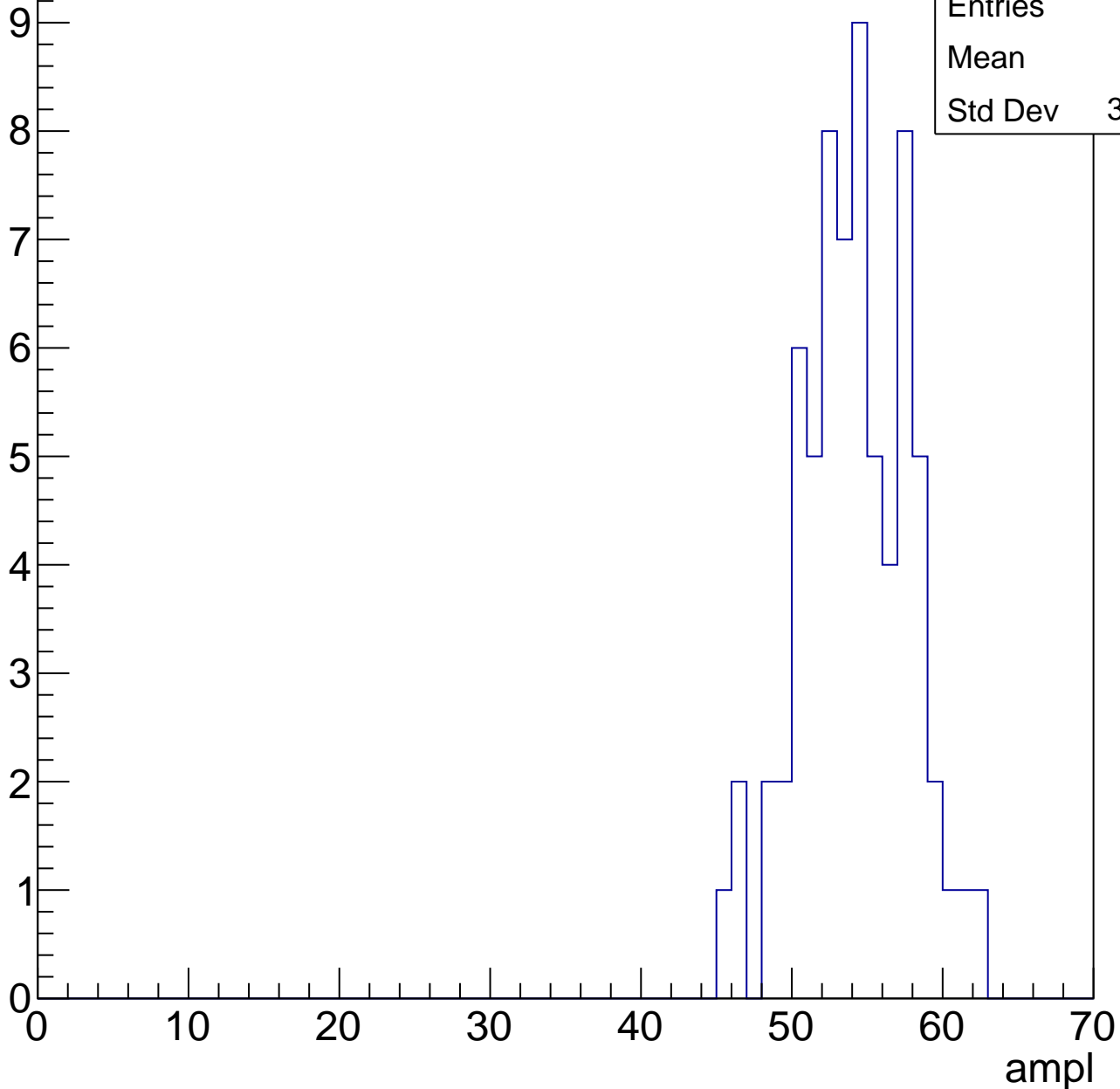


# B1L102S, U20-ch108, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	53.7
Std Dev	3.564

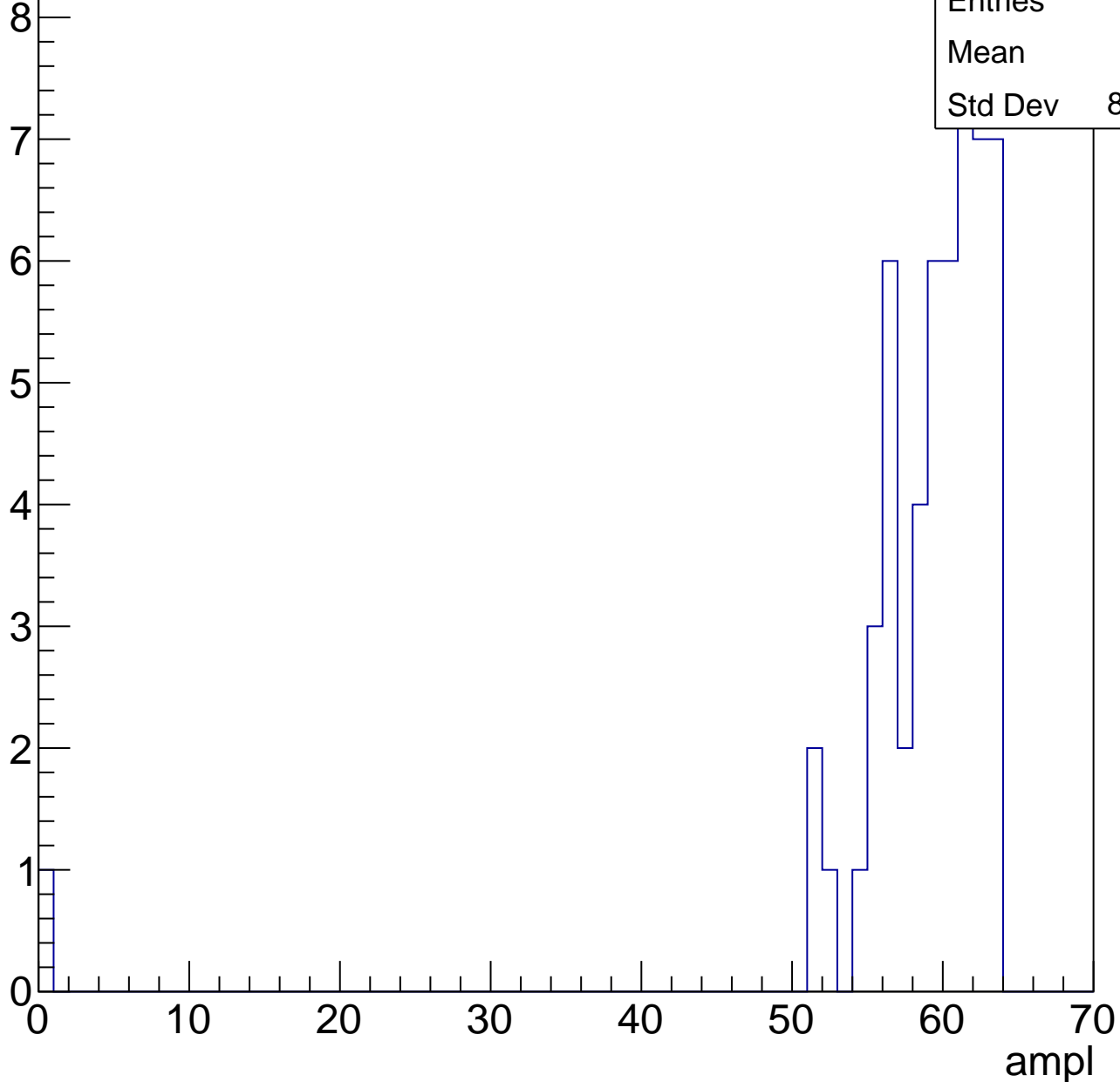


# B1L102S, U20-ch108, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	58
Std Dev	8.559



# B1L102S, U20-ch108, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries

11

Mean

60.73

Std Dev

1.71



# B1L102S, U20-ch108, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

1

Mean

62

Std Dev

0

# B1L102S, U20-ch109, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	73
Mean	27.93
Std Dev	5.624

**Gaus mean : 29.8448**

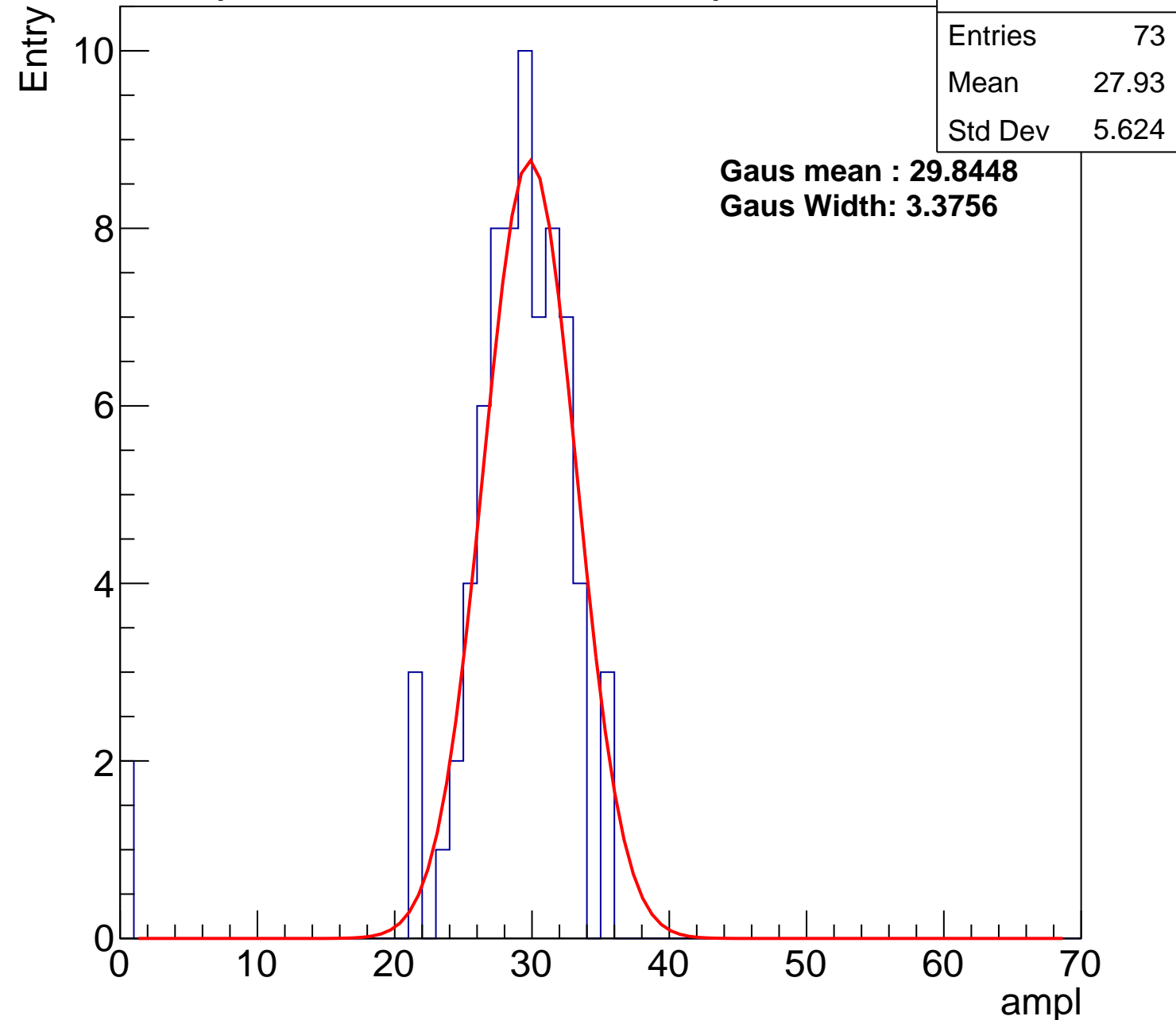
**Gaus Width: 3.3756**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U20-ch109, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	67
Mean	36.39
Std Dev	3.363

**Gaus mean : 36.8816**

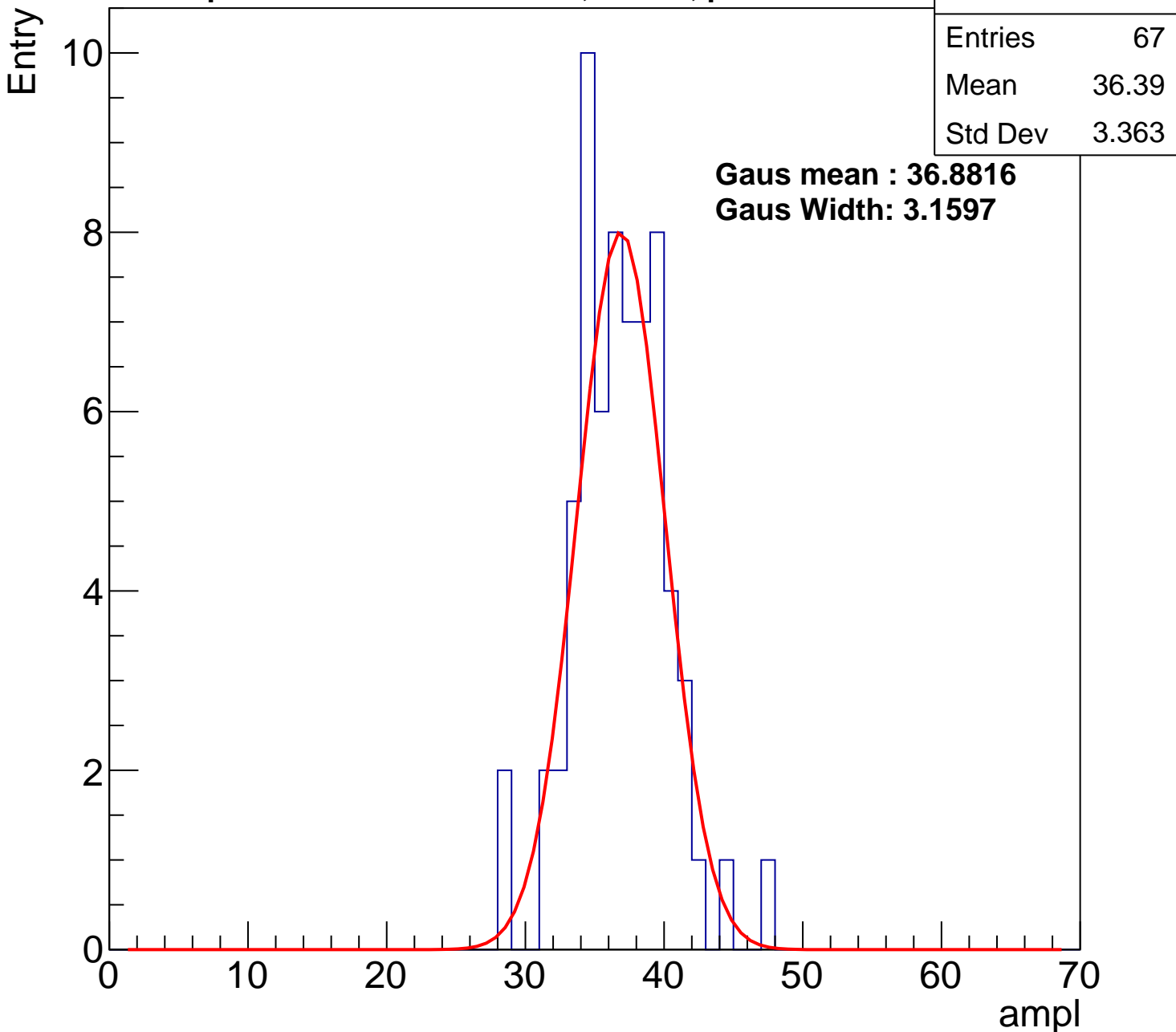
**Gaus Width: 3.1597**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U20-ch109, adc2

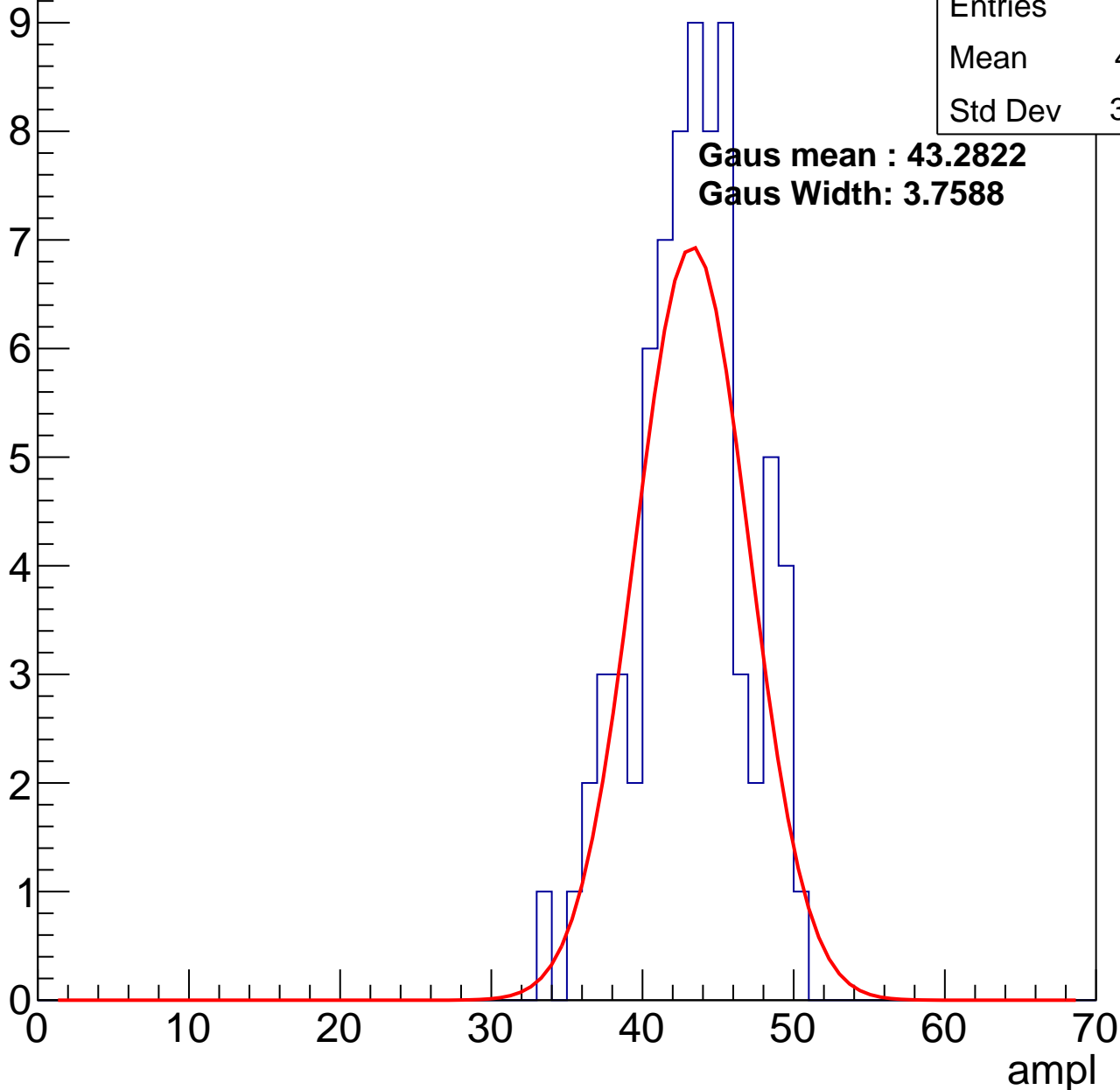
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	42.81
Std Dev	3.649

**Gaus mean : 43.2822**

**Gaus Width: 3.7588**

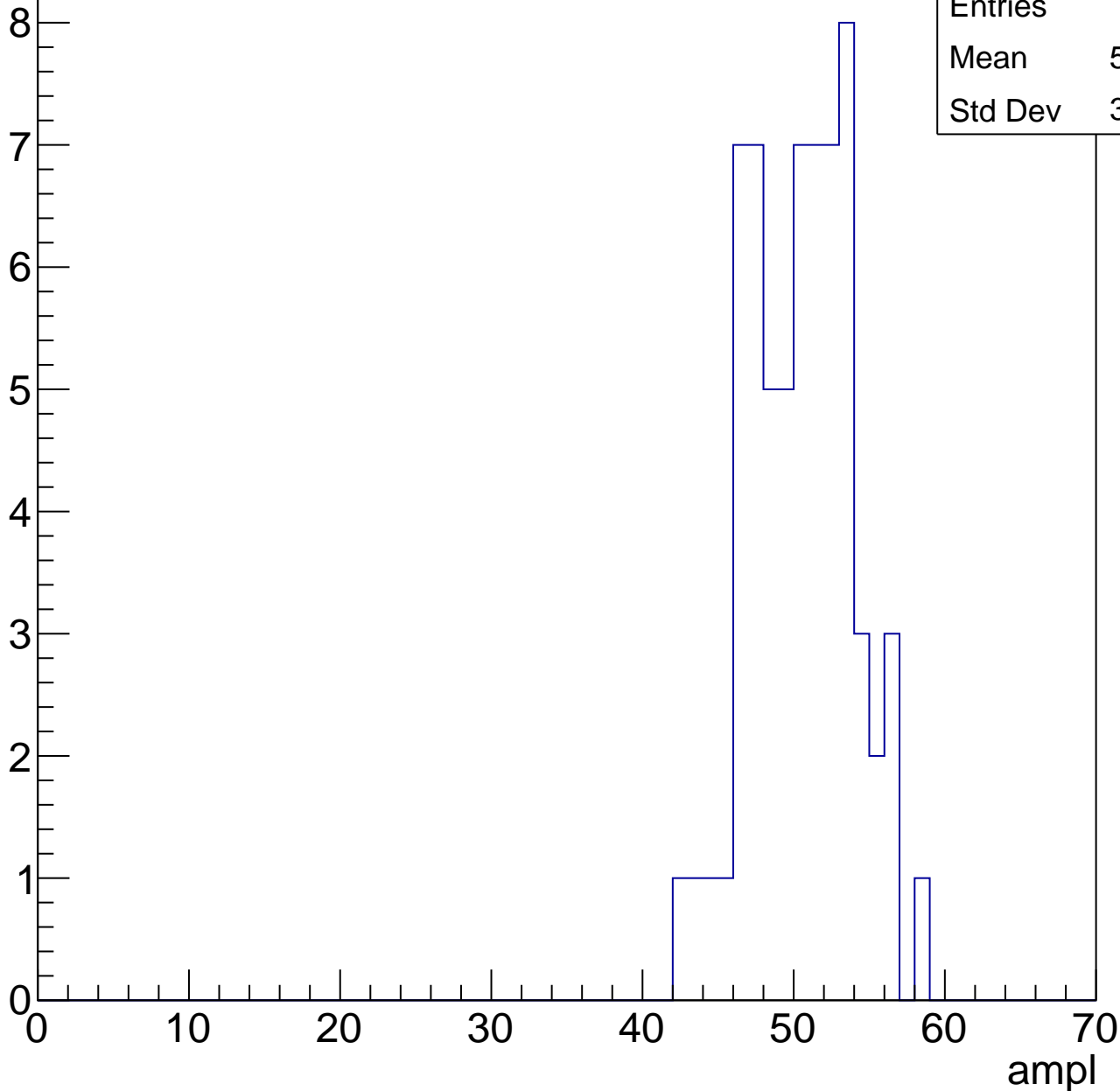


# B1L102S, U20-ch109, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	50.05
Std Dev	3.373

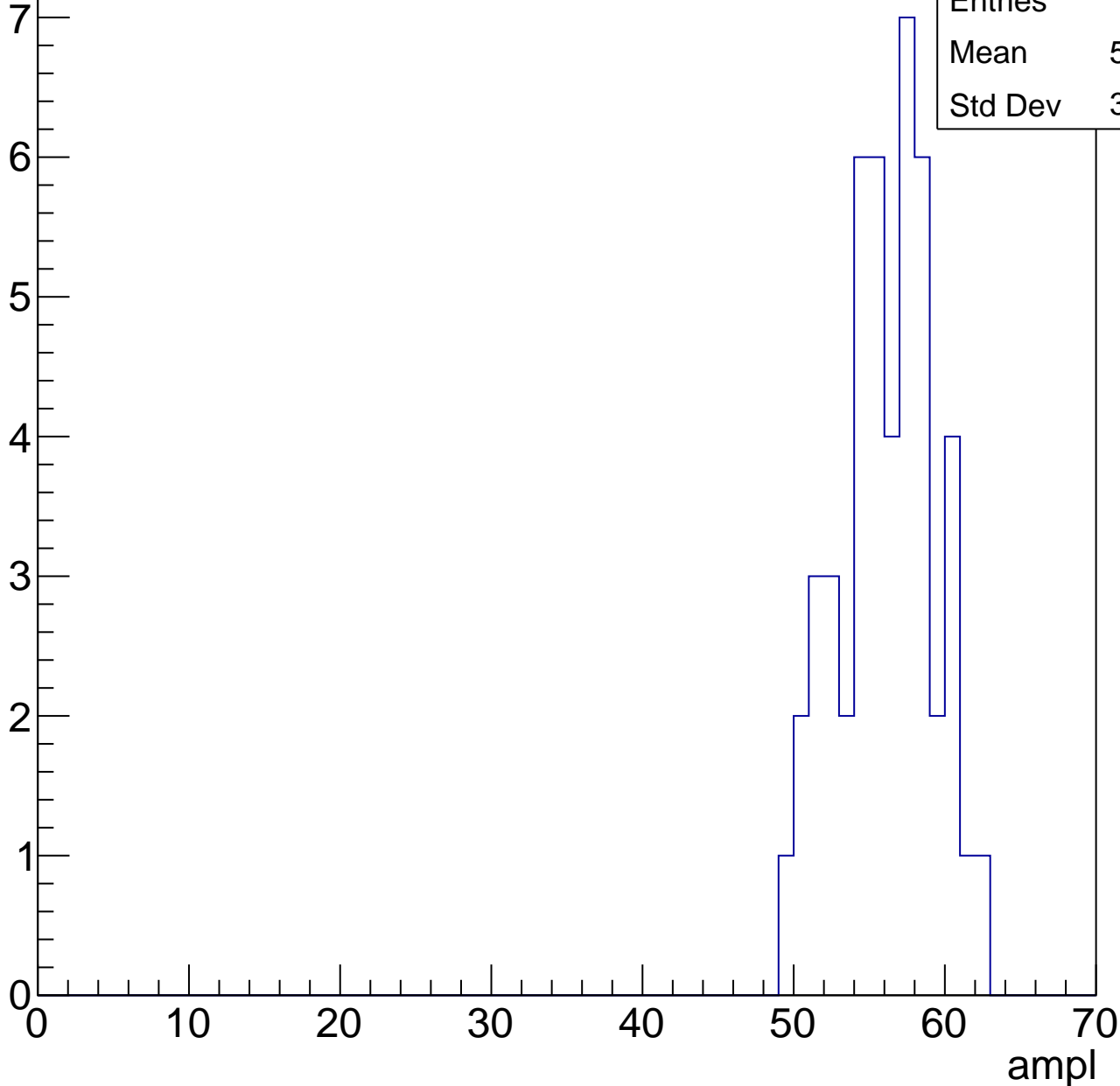


# B1L102S, U20-ch109, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

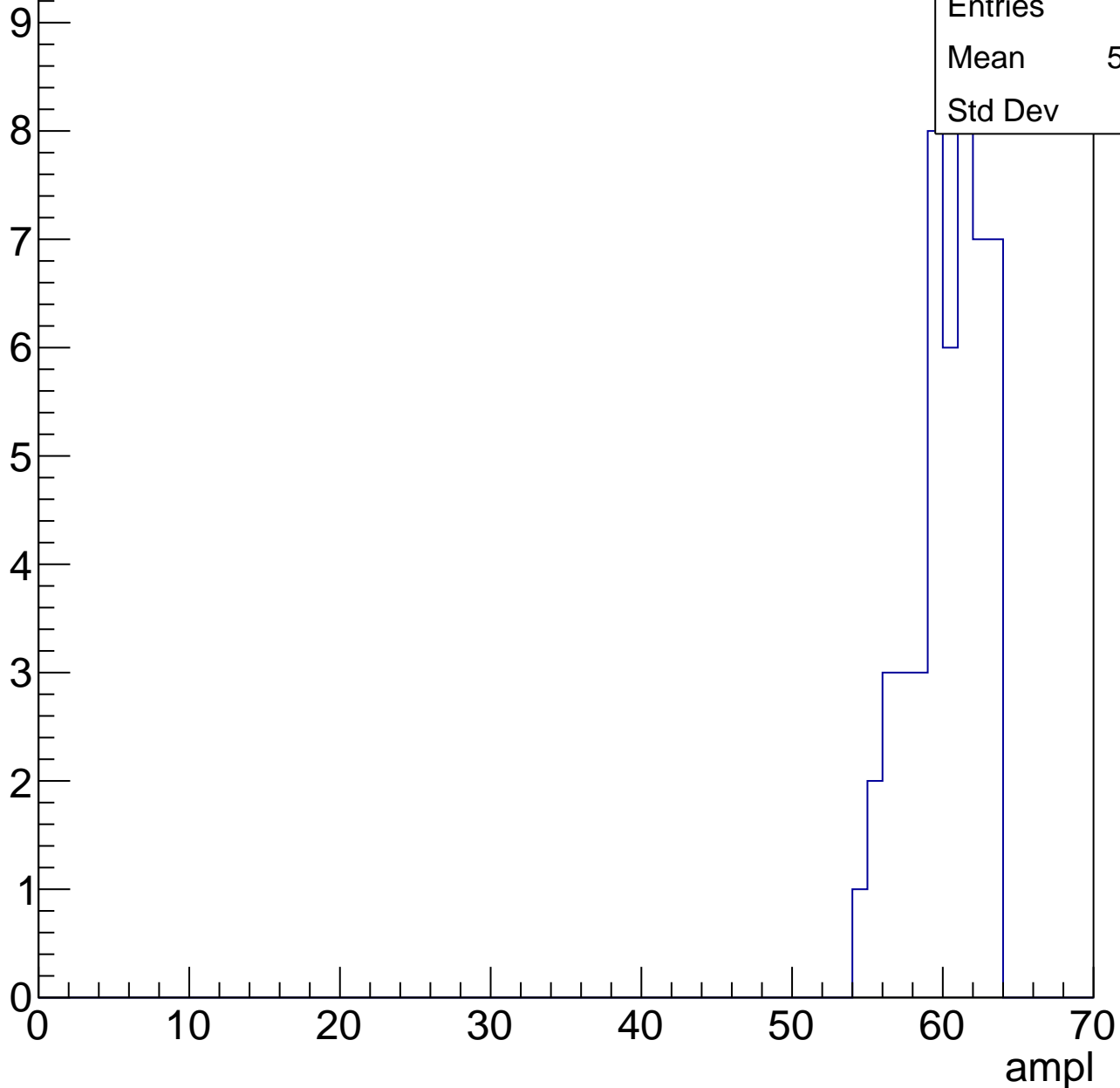
Entries	48
Mean	55.62
Std Dev	3.093



# B1L102S, U20-ch109, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

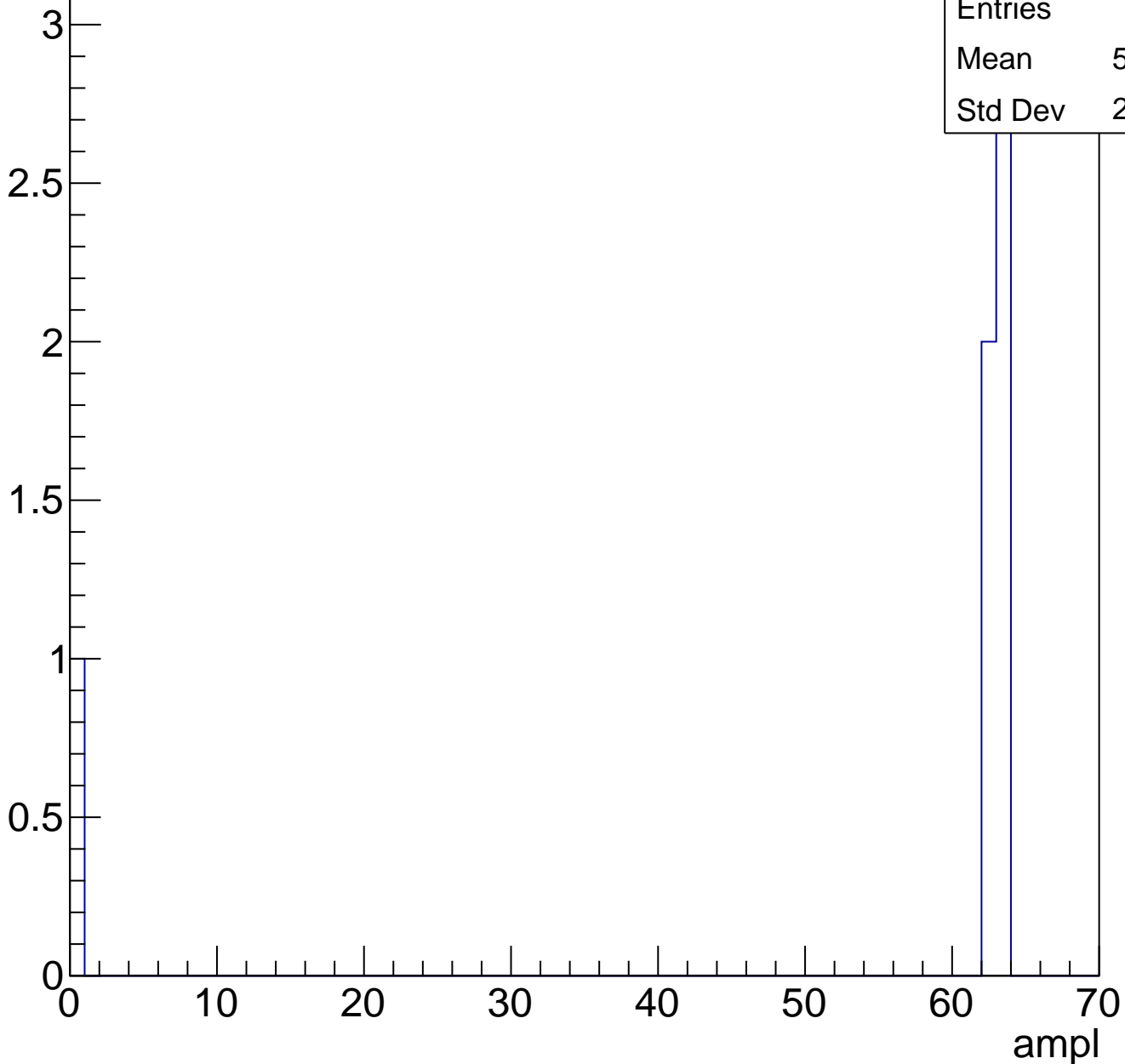
Entry



# B1L102S, U20-ch109, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U20-ch109, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch110, adc0

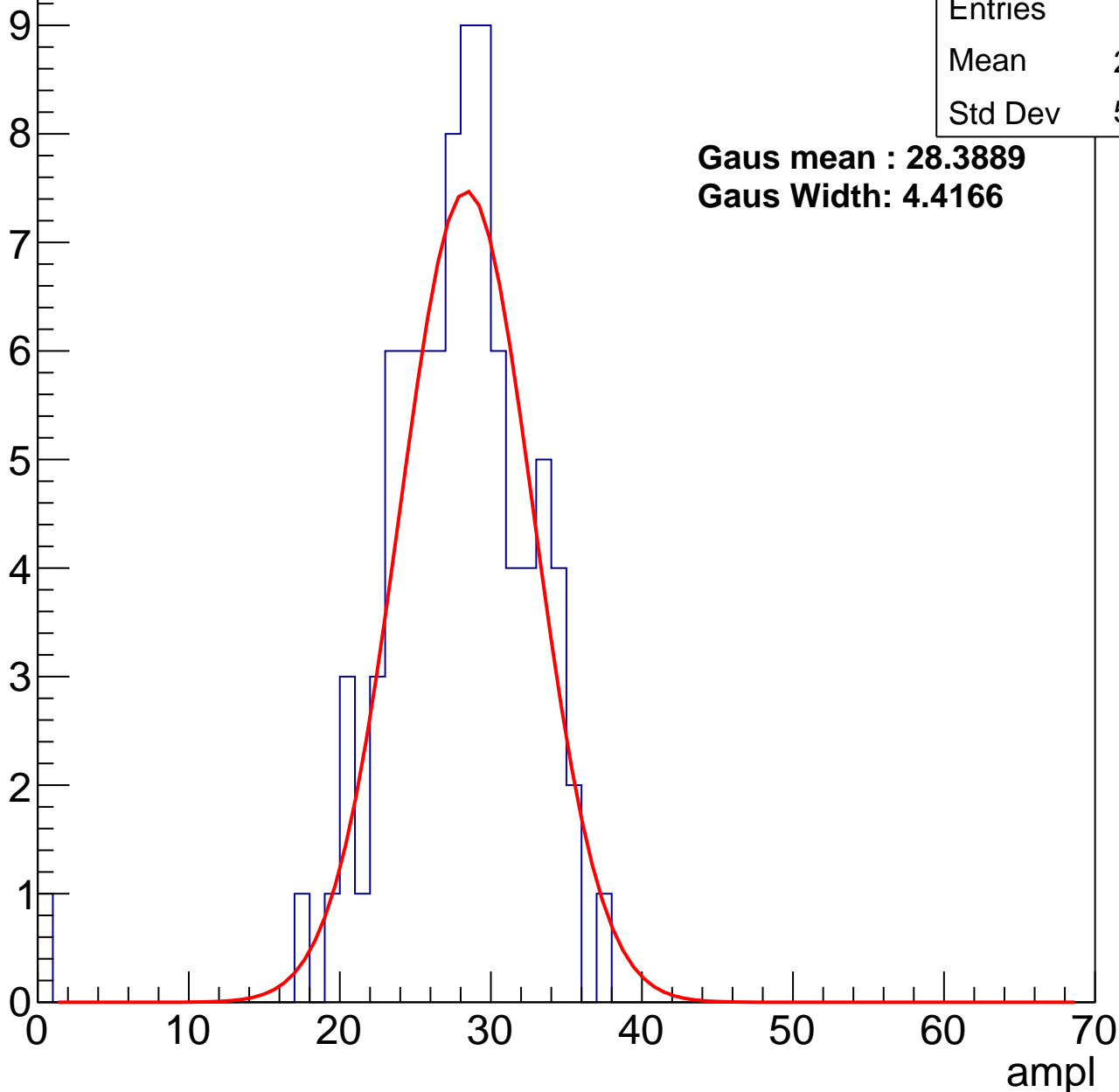
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	86
Mean	27.21
Std Dev	5.051

**Gaus mean : 28.3889**

**Gaus Width: 4.4166**



# B1L102S, U20-ch110, adc1

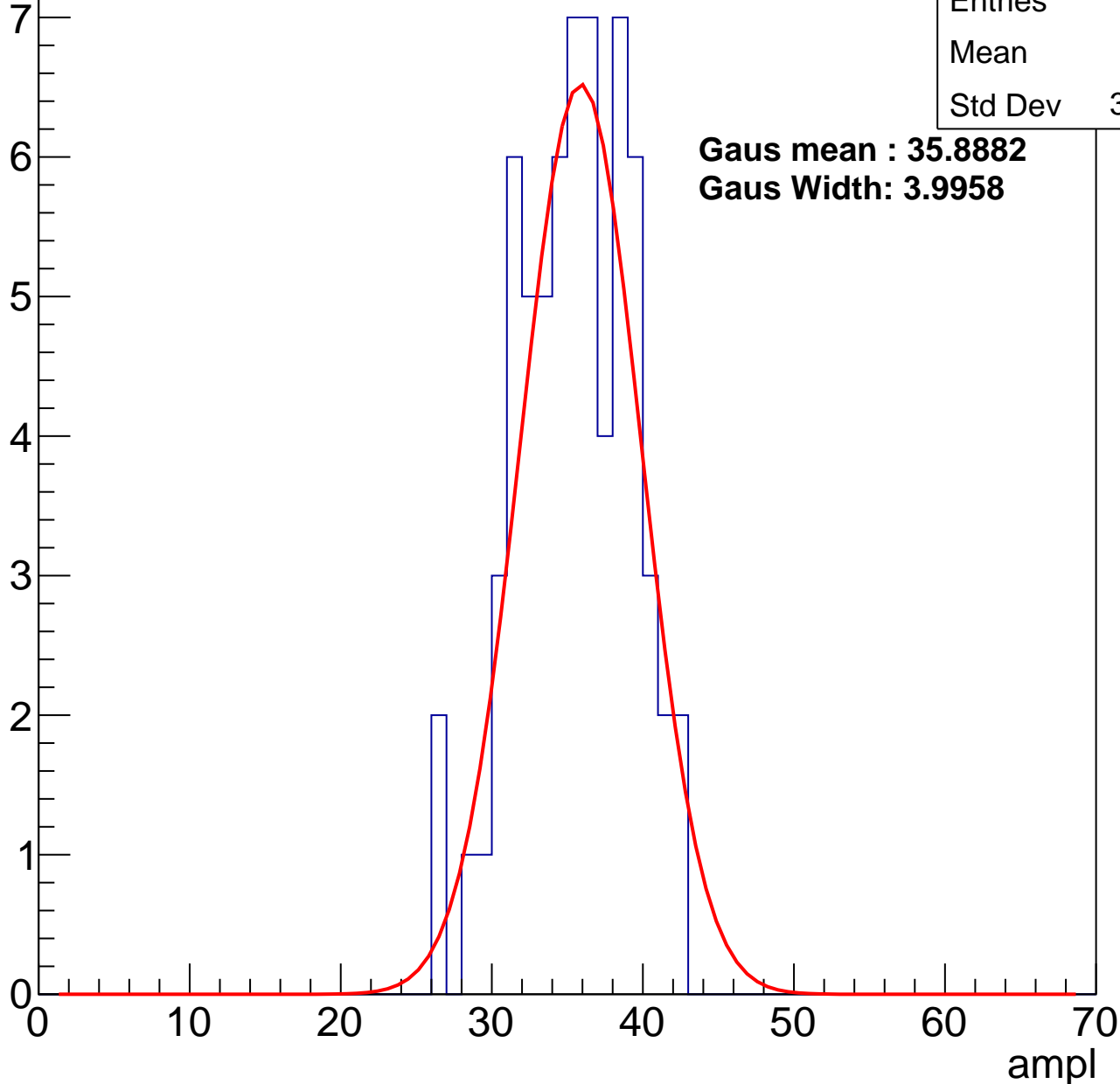
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	35
Std Dev	3.698

**Gaus mean : 35.8882**

**Gaus Width: 3.9958**



# B1L102S, U20-ch110, adc2

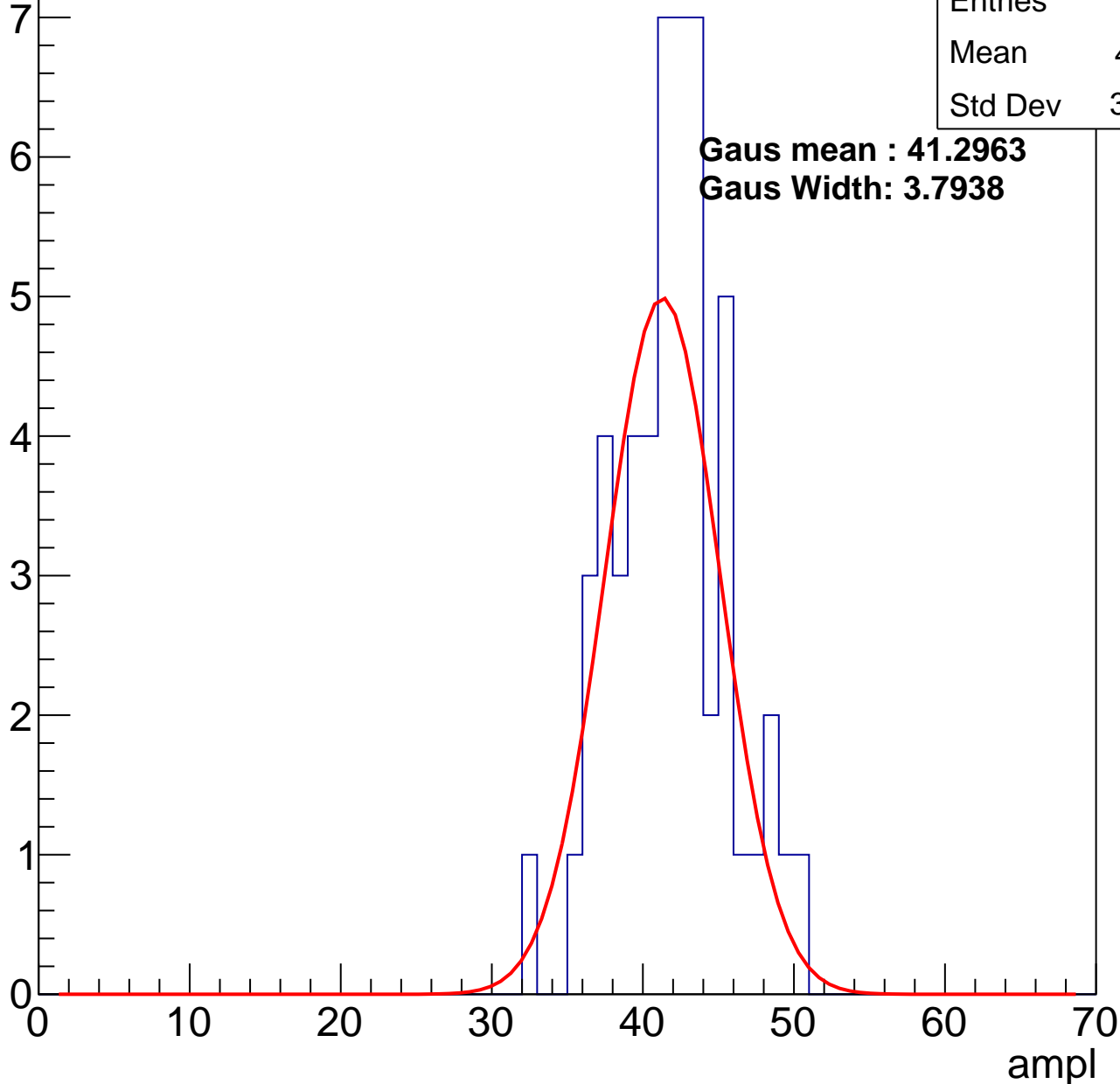
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	41.41
Std Dev	3.679

**Gaus mean : 41.2963**

**Gaus Width: 3.7938**

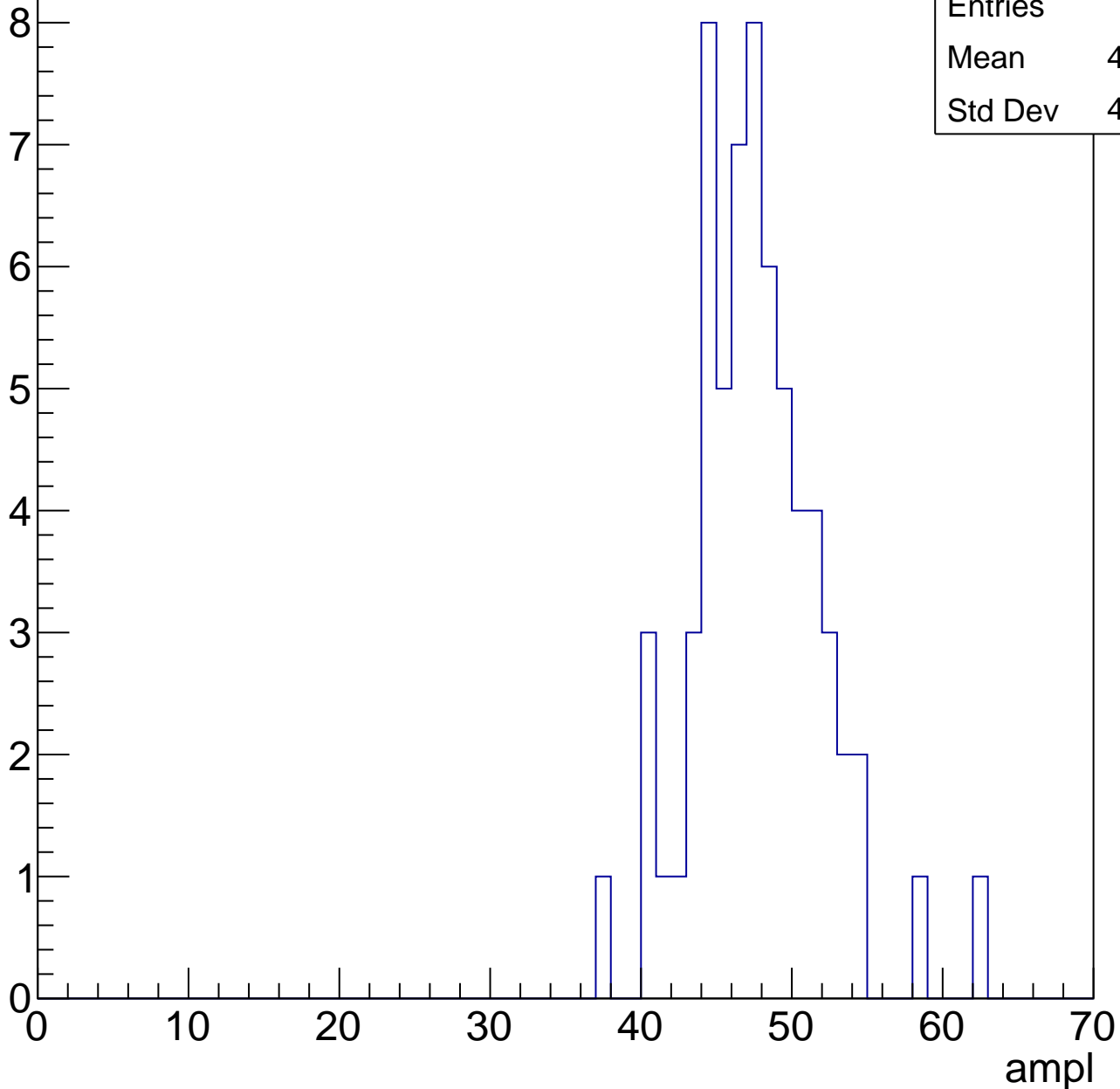


# B1L102S, U20-ch110, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	47.25
Std Dev	4.239

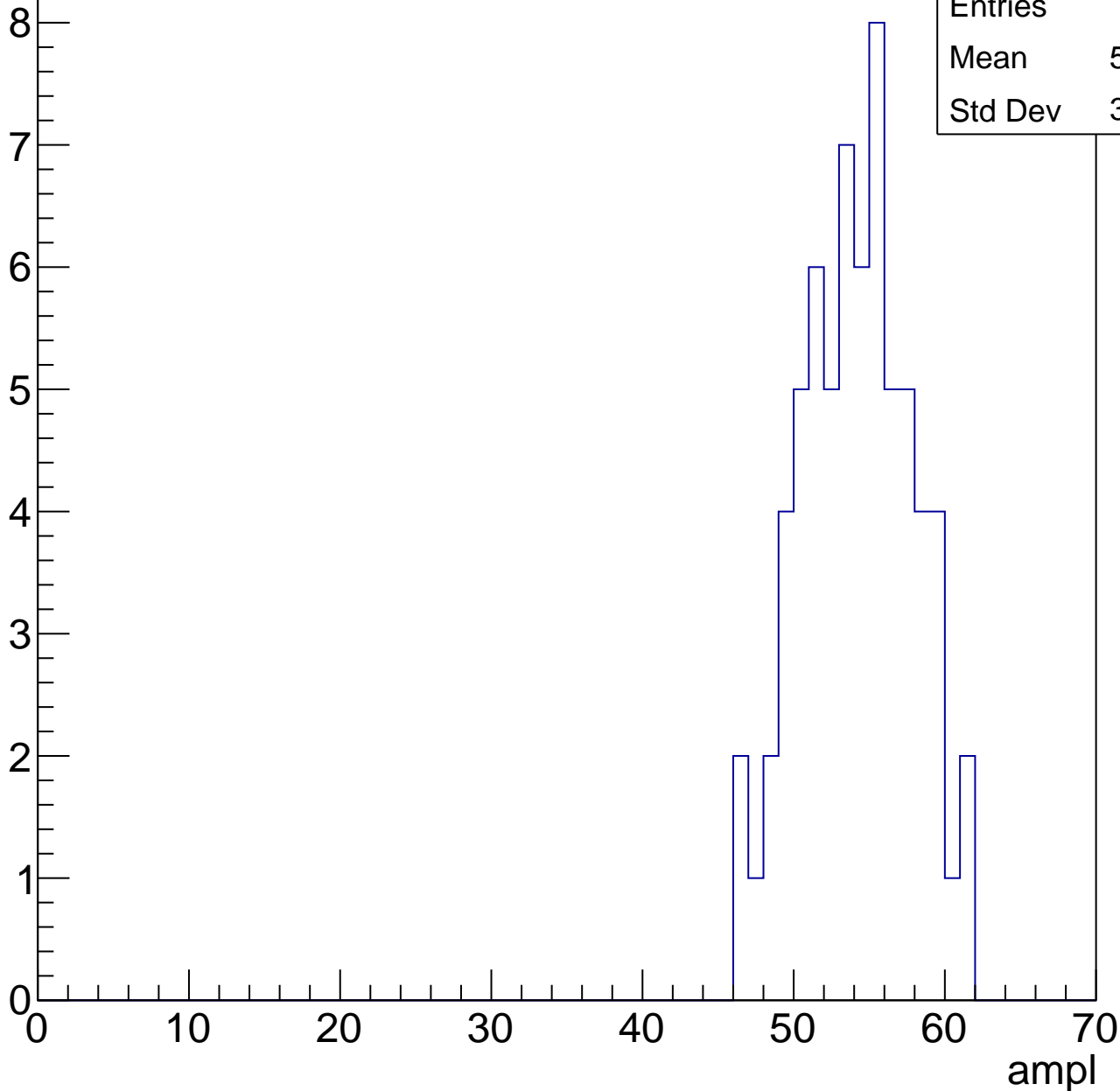


# B1L102S, U20-ch110, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	53.69
Std Dev	3.613

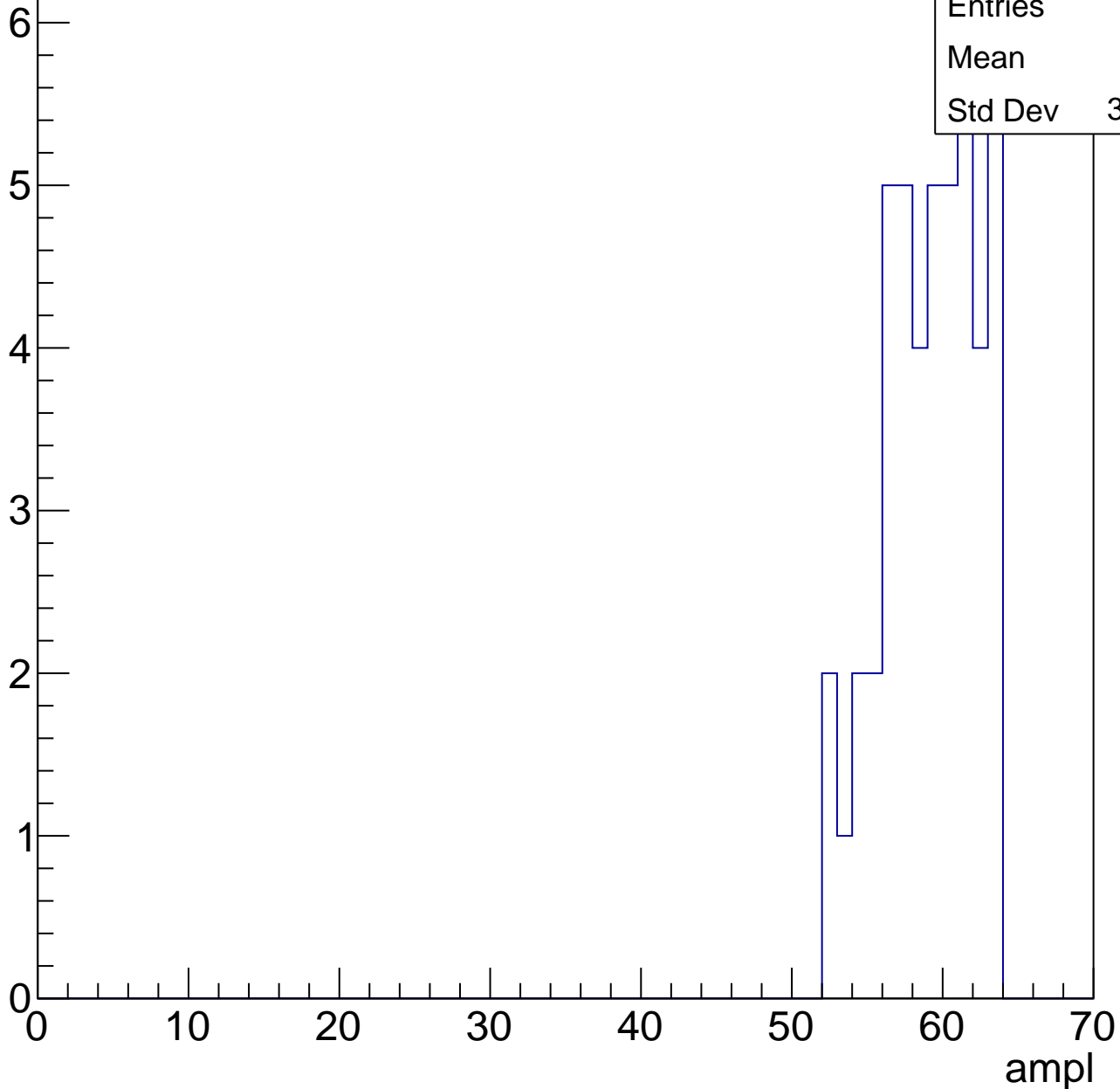


# B1L102S, U20-ch110, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	47
Mean	58.7
Std Dev	3.066

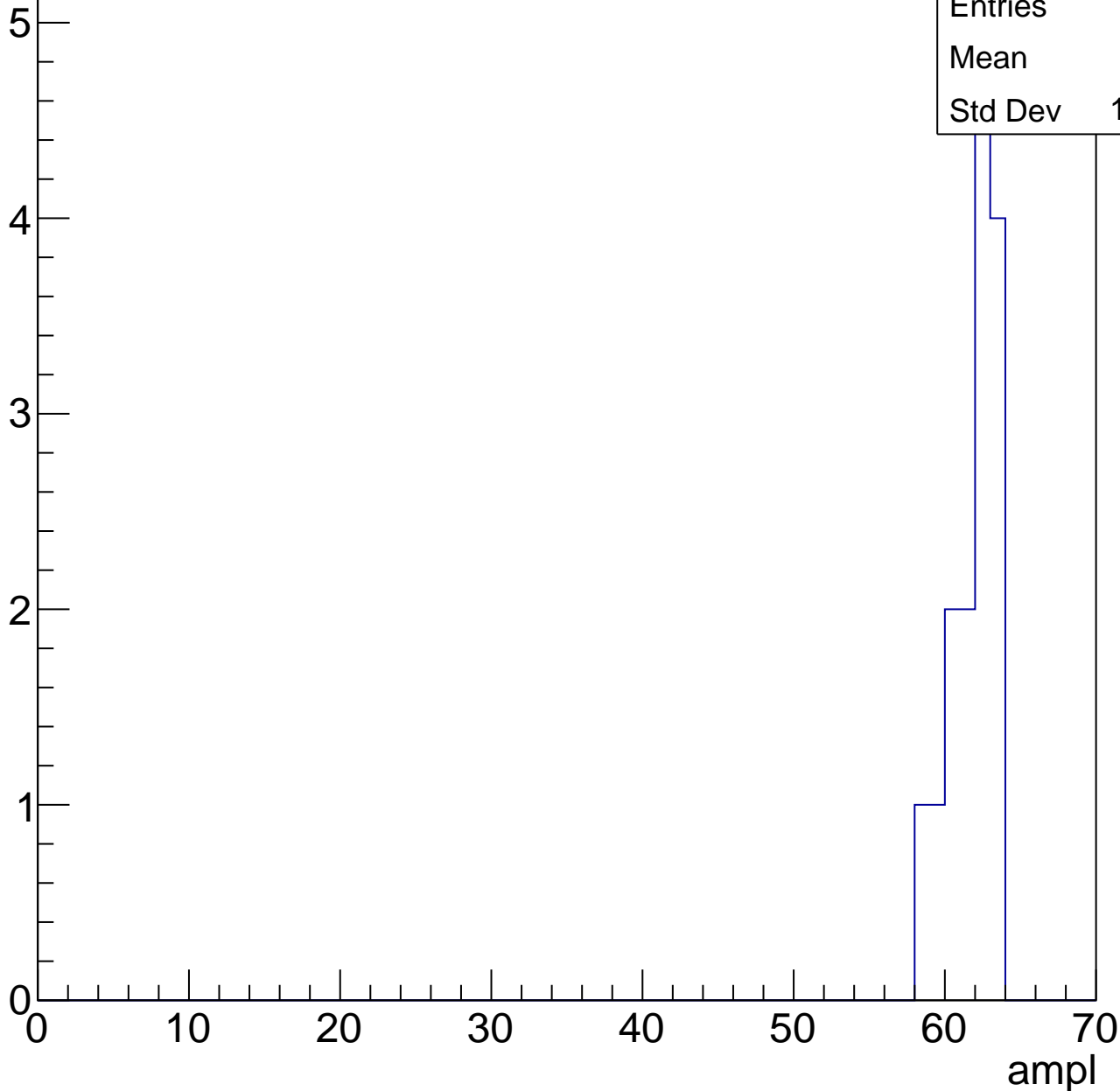


# B1L102S, U20-ch110, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	15
Mean	61.4
Std Dev	1.497

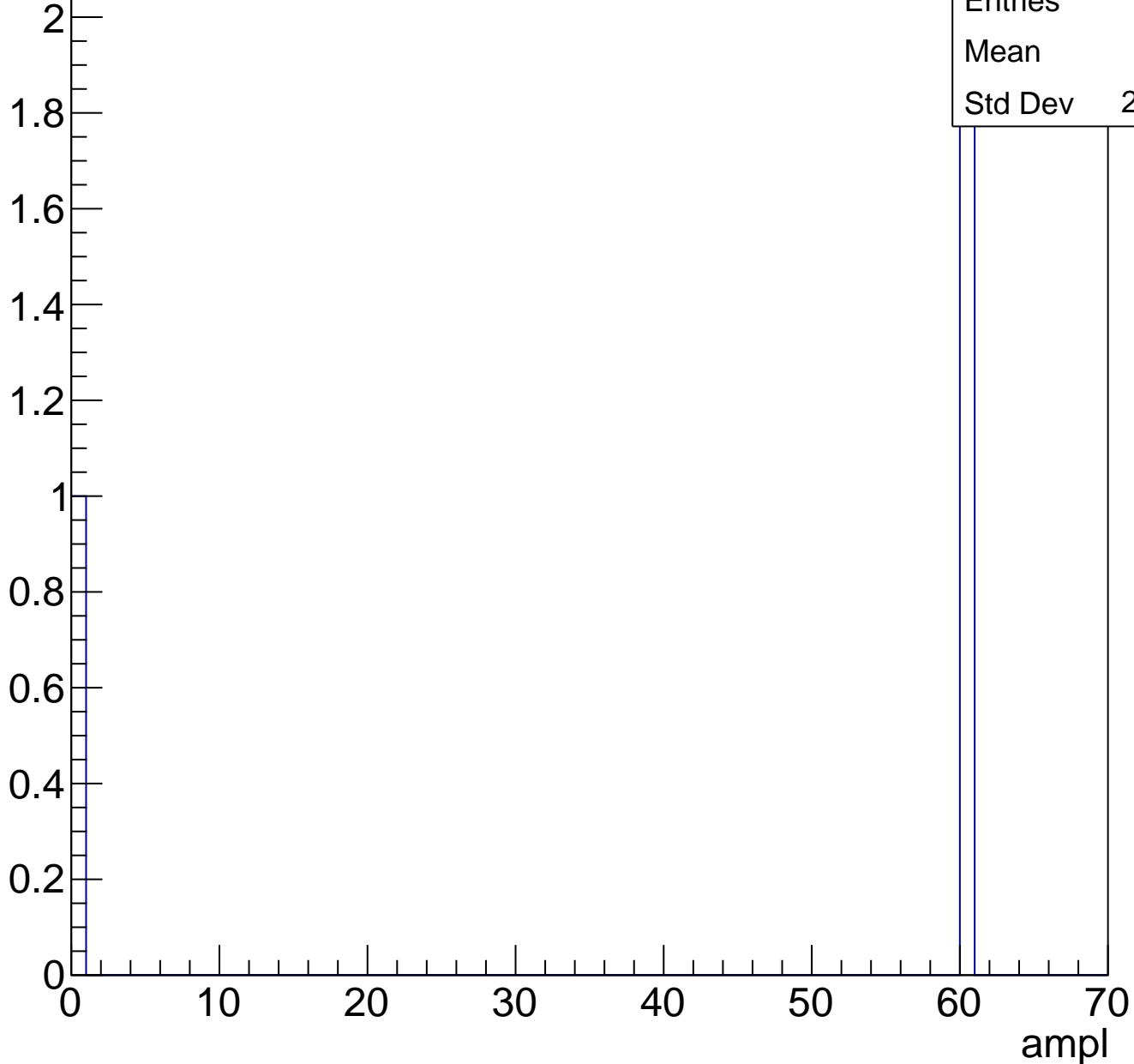




# B1L102S, U20-ch110, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch111, adc0

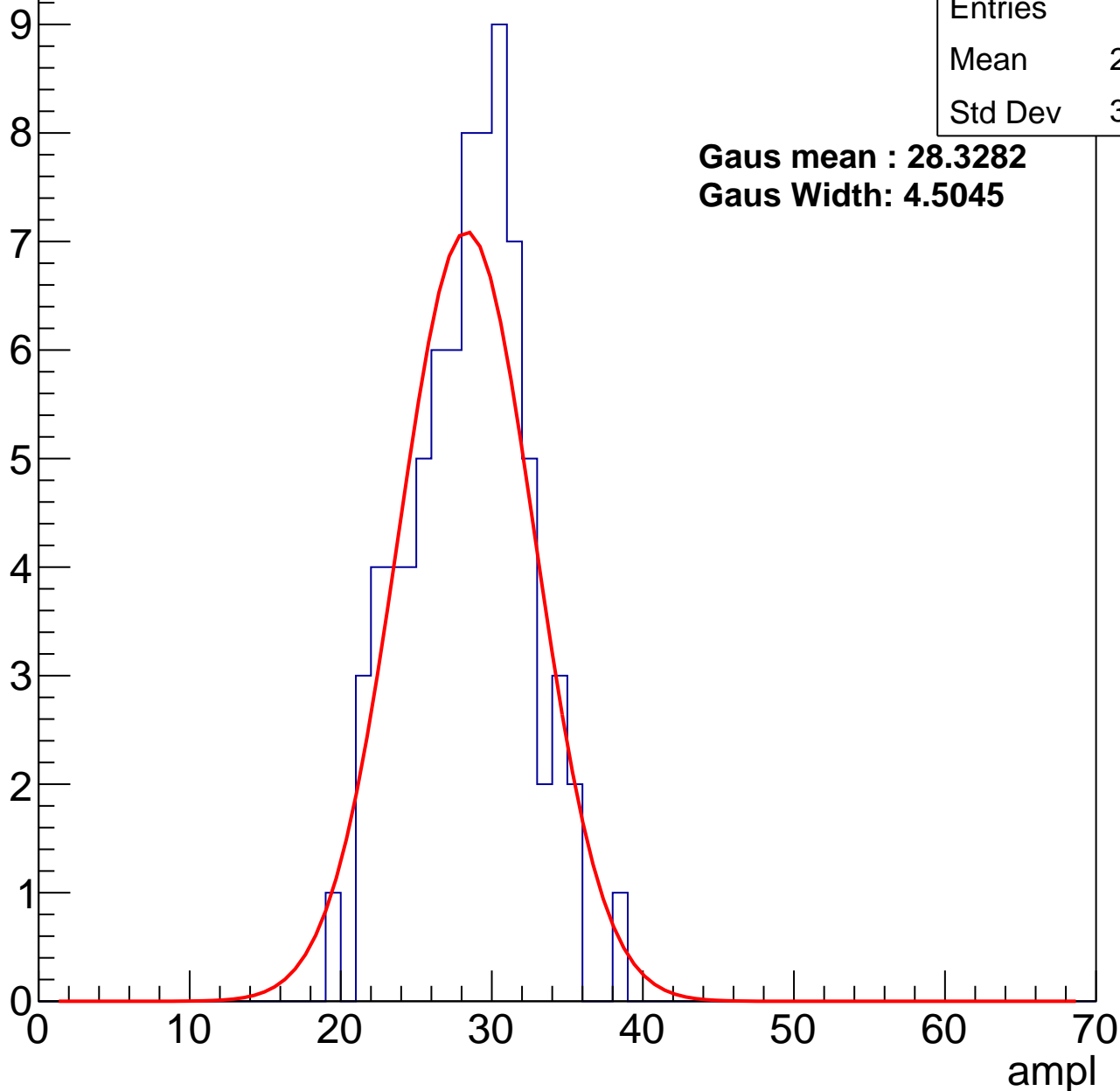
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	78
Mean	27.95
Std Dev	3.846

**Gaus mean : 28.3282**

**Gaus Width: 4.5045**



# B1L102S, U20-ch111, adc1

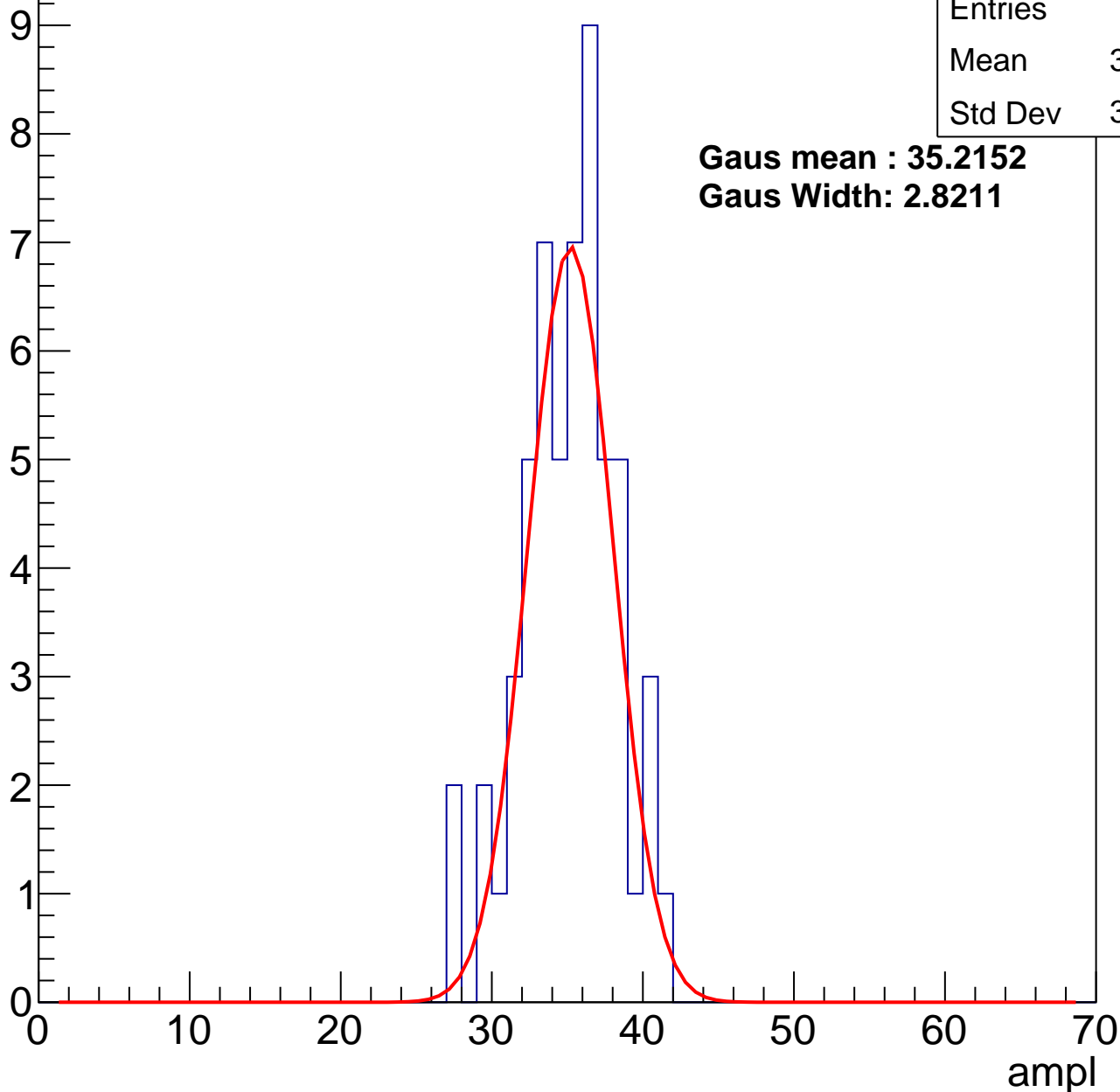
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	34.64
Std Dev	3.119

**Gaus mean : 35.2152**

**Gaus Width: 2.8211**



# B1L102S, U20-ch111, adc2

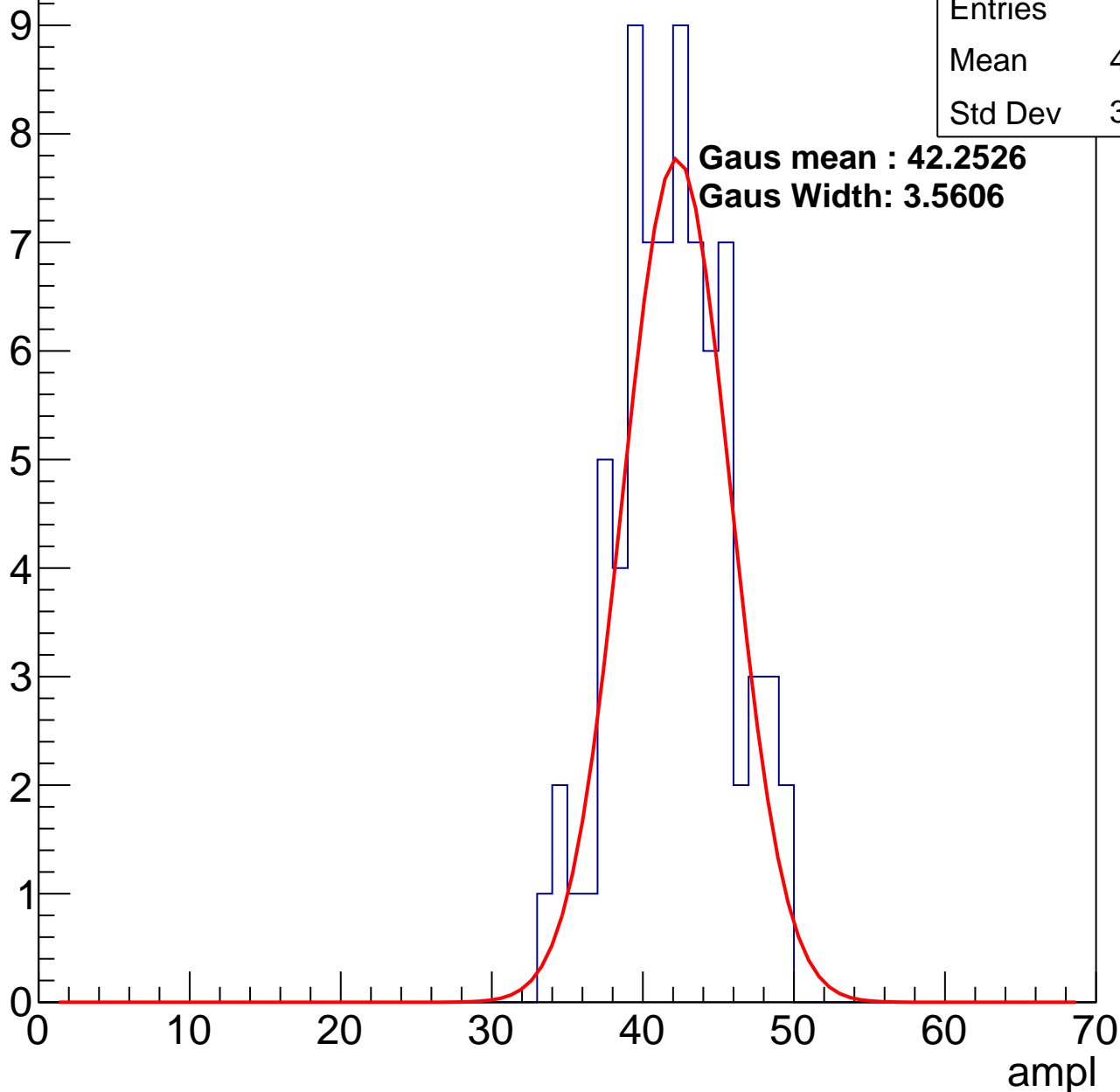
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	41.58
Std Dev	3.614

**Gaus mean : 42.2526**

**Gaus Width: 3.5606**

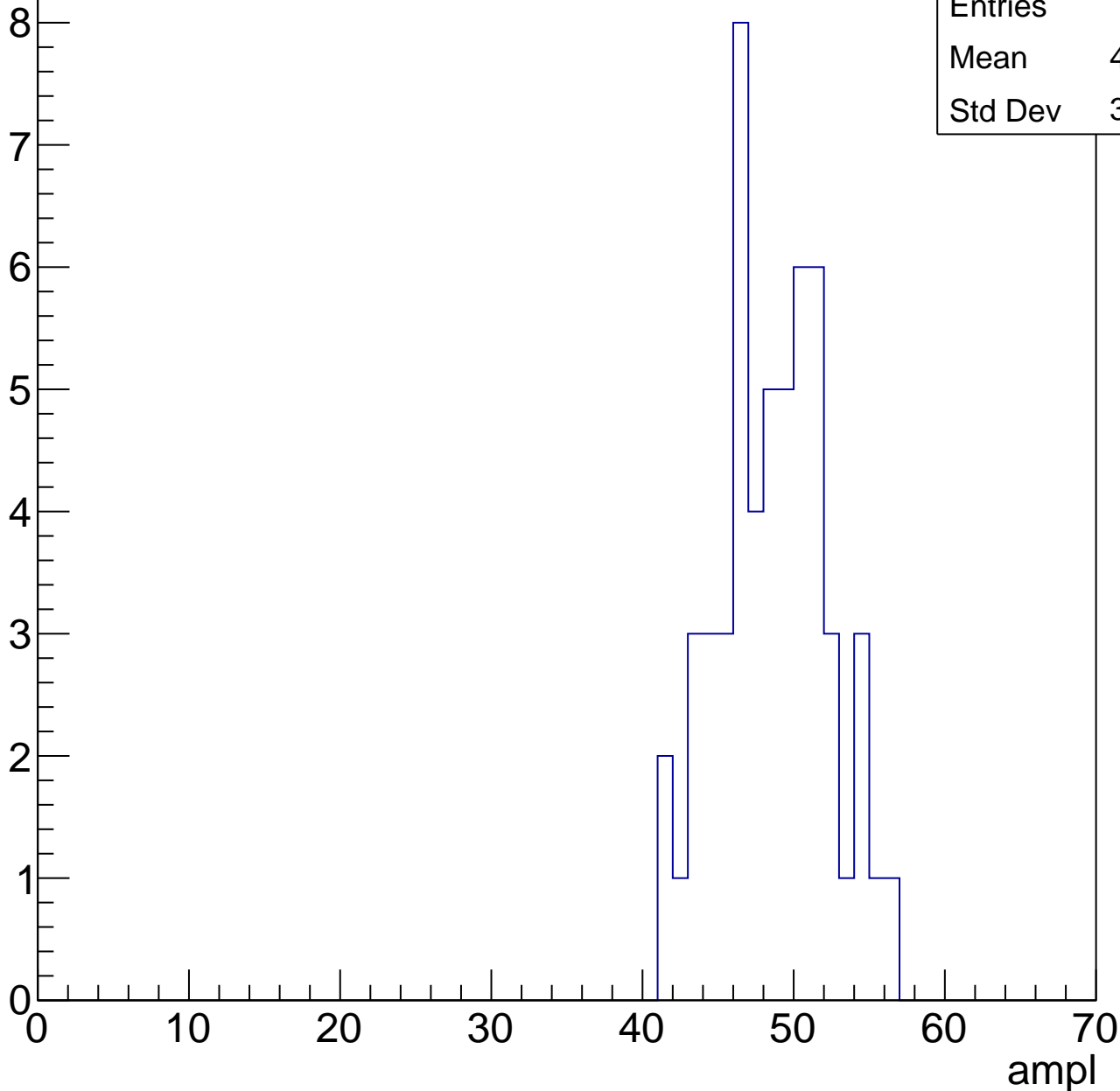


# B1L102S, U20-ch111, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	48.16
Std Dev	3.556

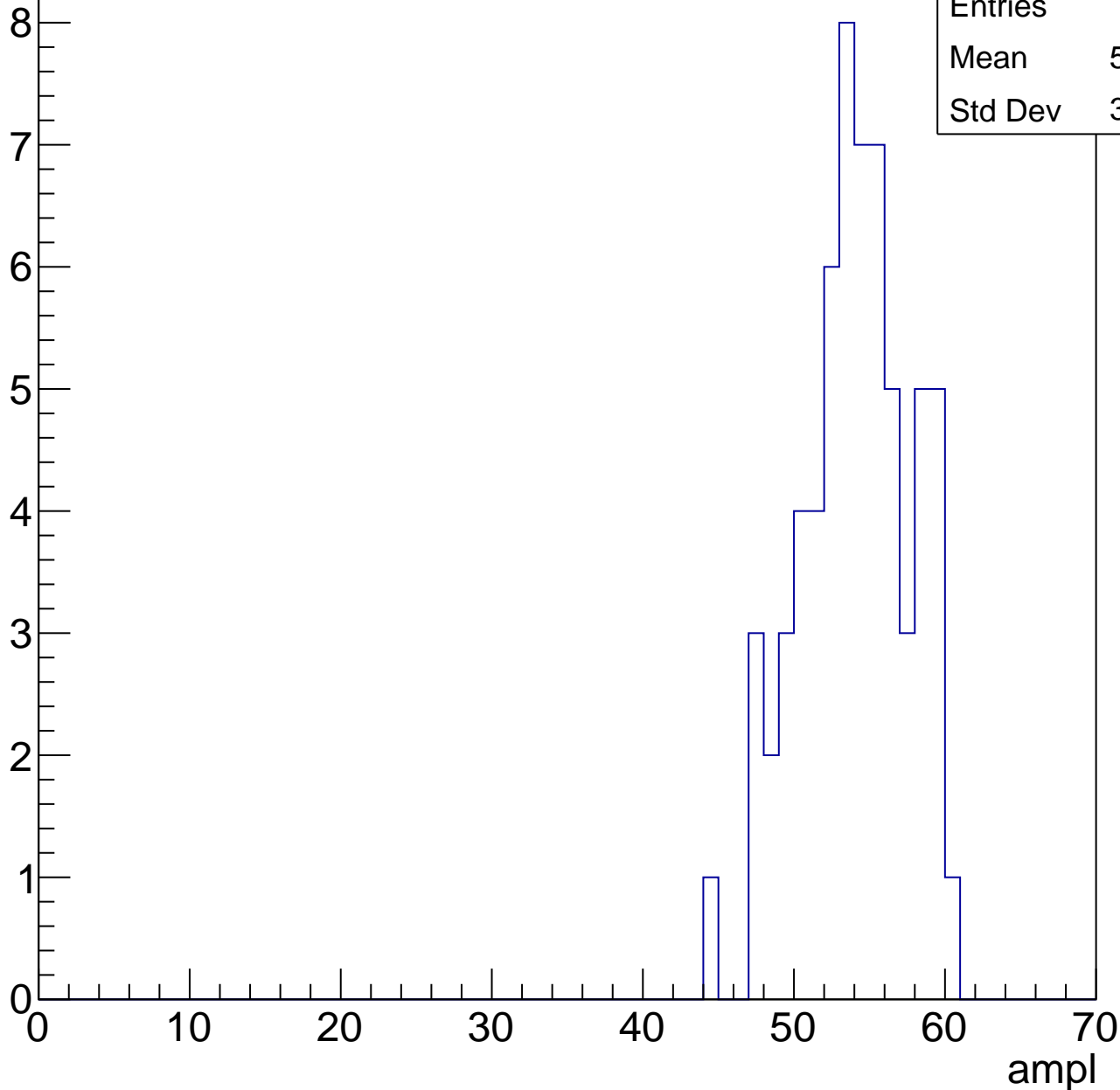


# B1L102S, U20-ch111, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	53.55
Std Dev	3.553

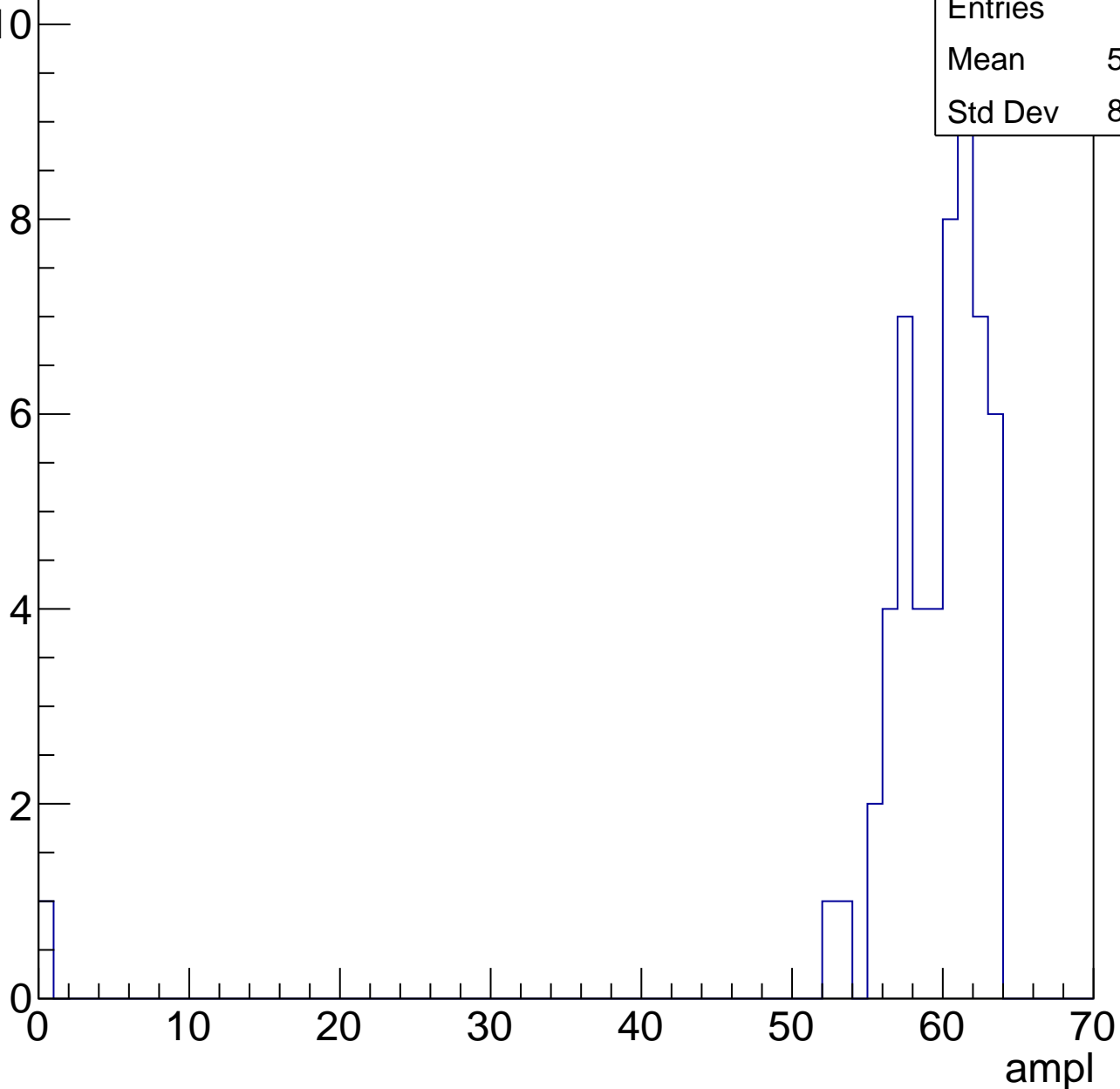


# B1L102S, U20-ch111, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

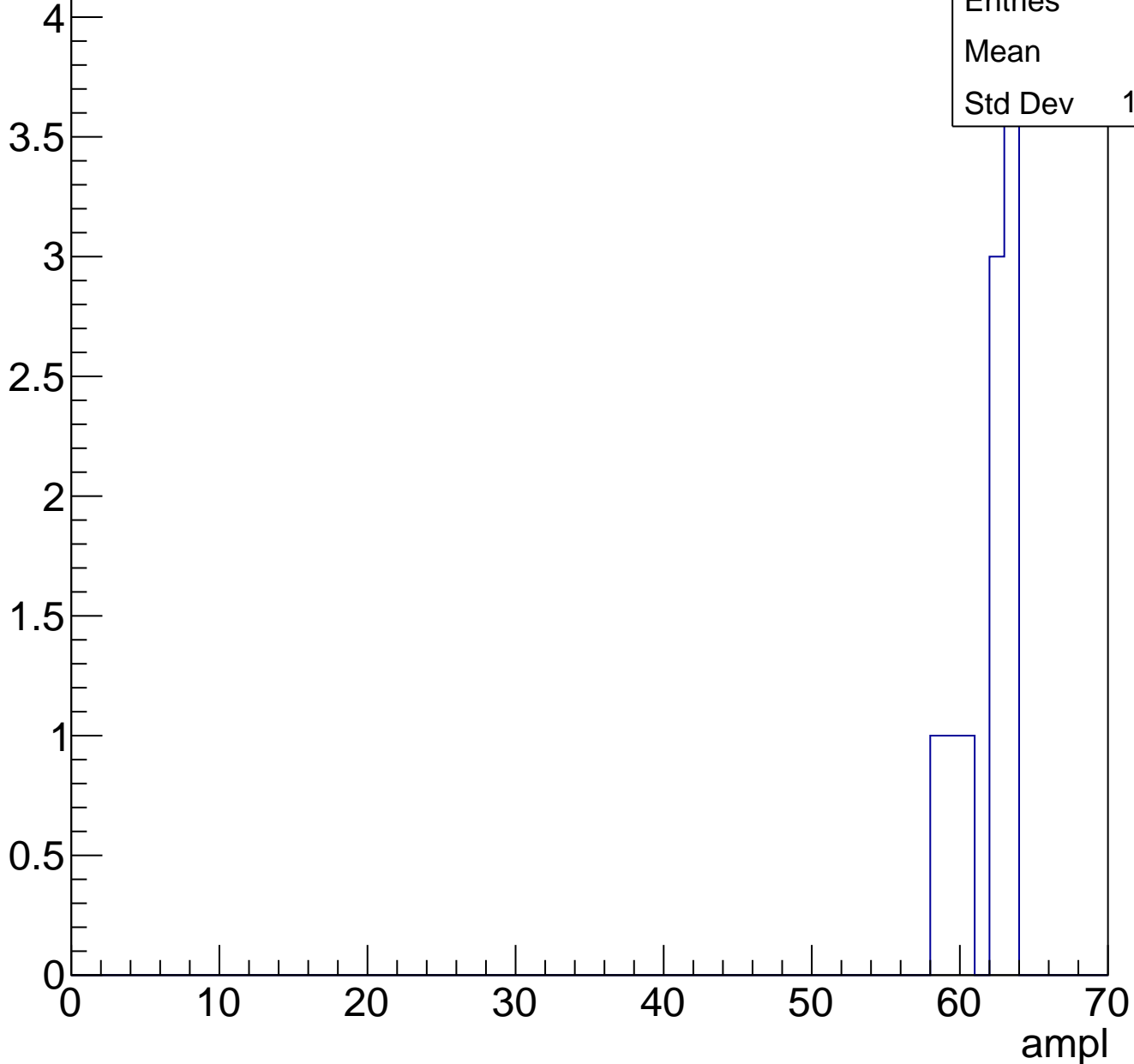
Entries	55
Mean	58.33
Std Dev	8.365



# B1L102S, U20-ch111, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U20-ch111, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U20-ch112, adc0

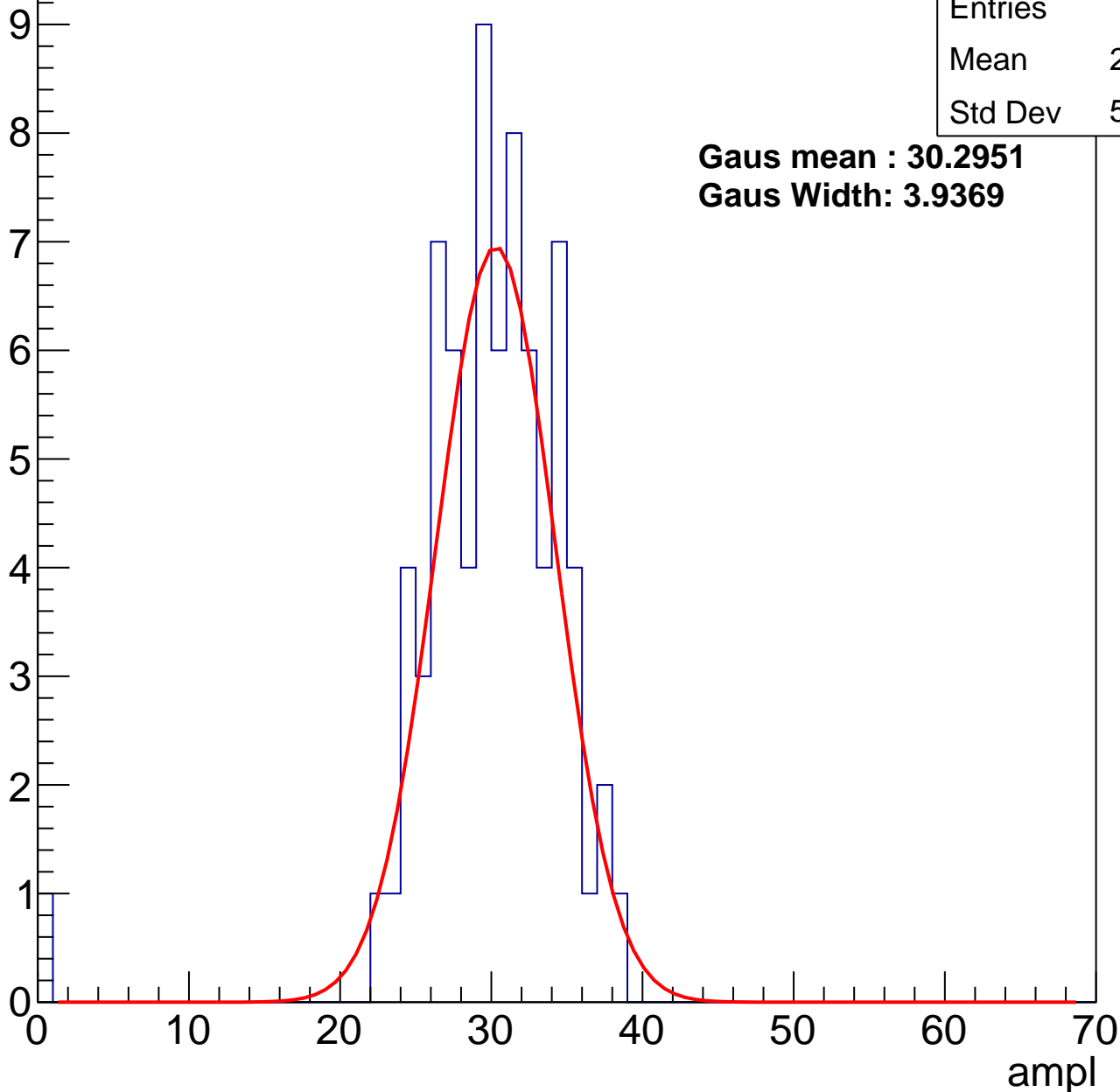
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	29.48
Std Dev	5.008

**Gaus mean : 30.2951**

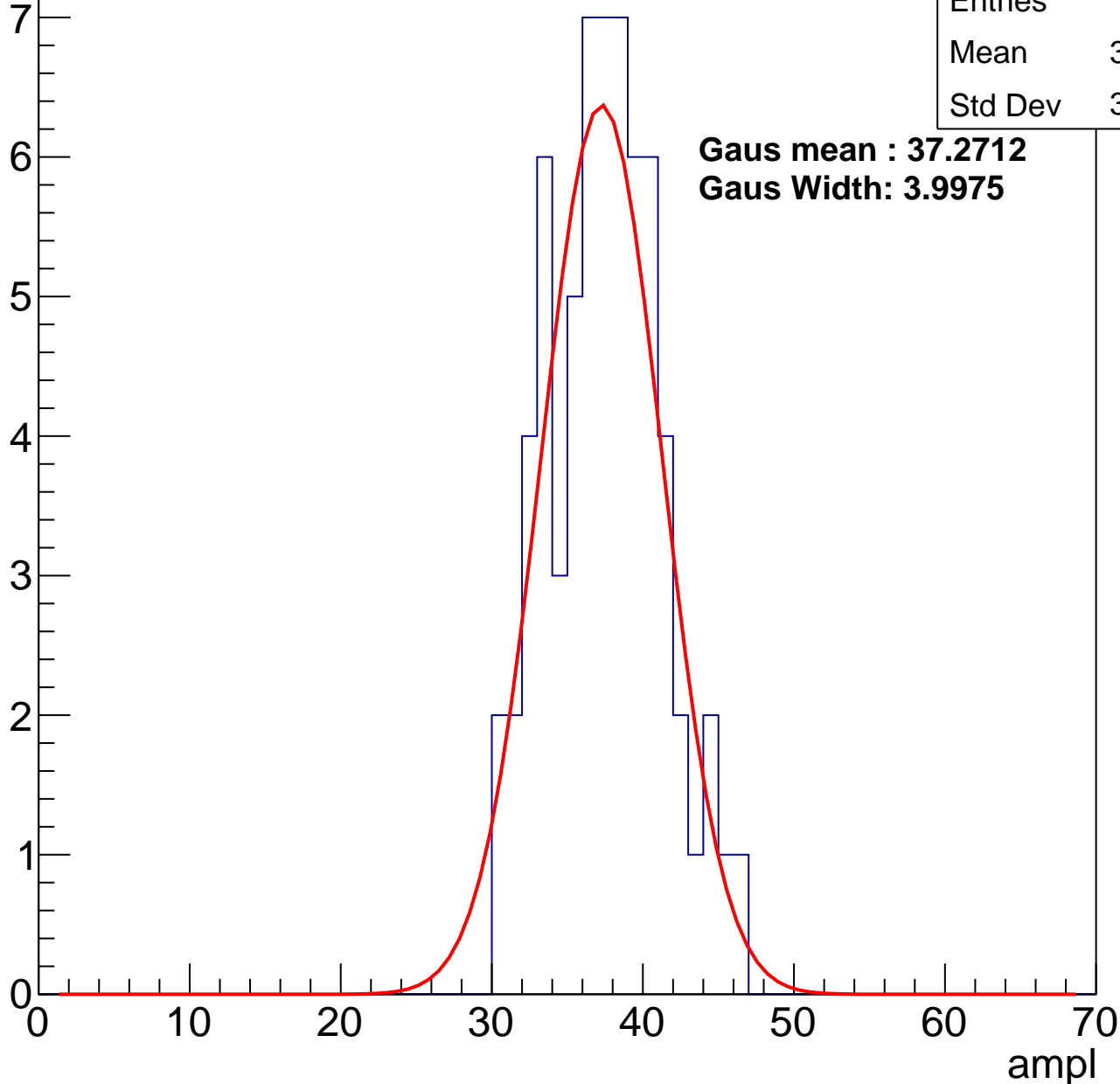
**Gaus Width: 3.9369**



# B1L102S, U20-ch112, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch112, adc2

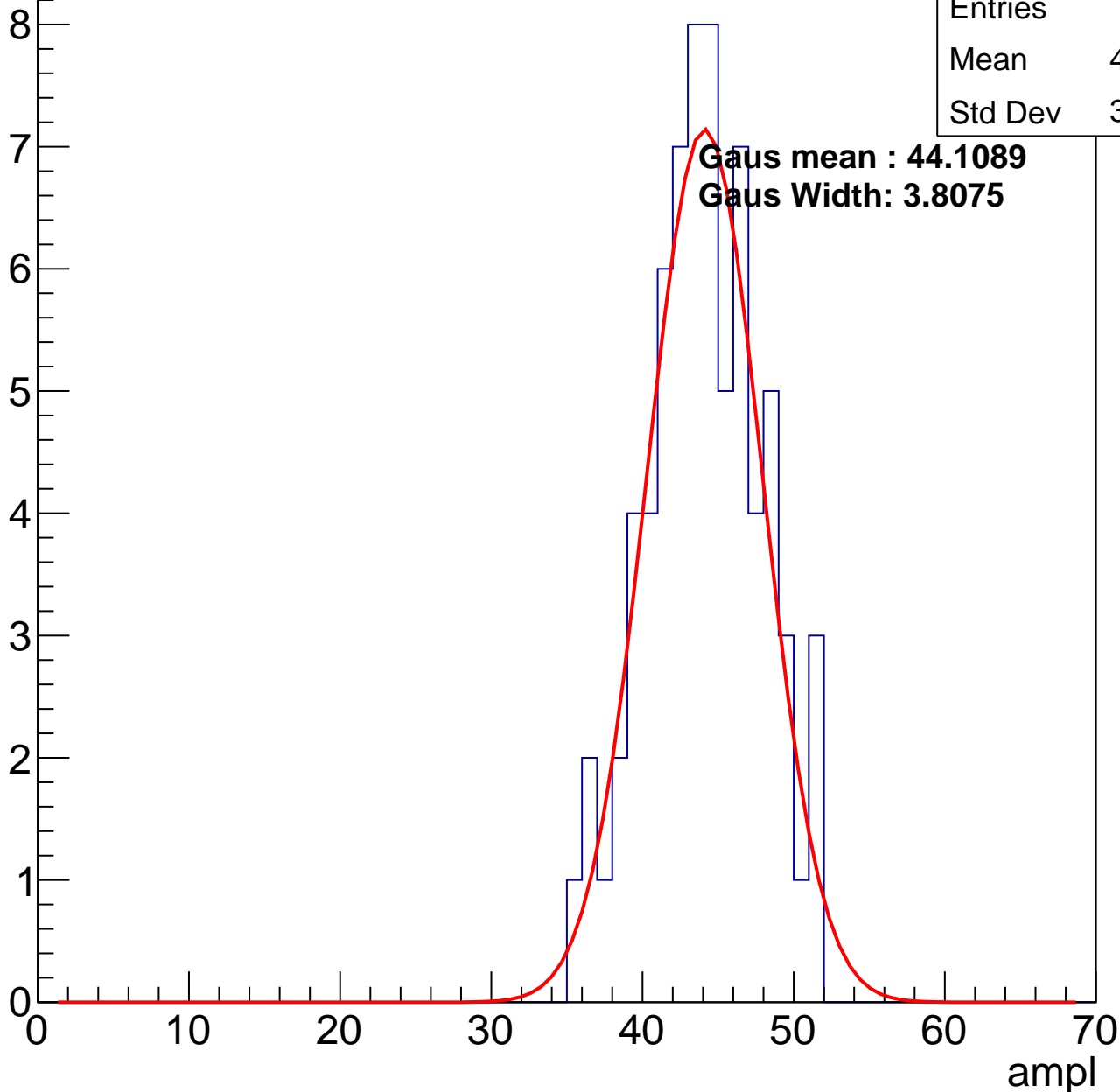
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	43.62
Std Dev	3.717

**Gaus mean : 44.1089**

**Gaus Width: 3.8075**

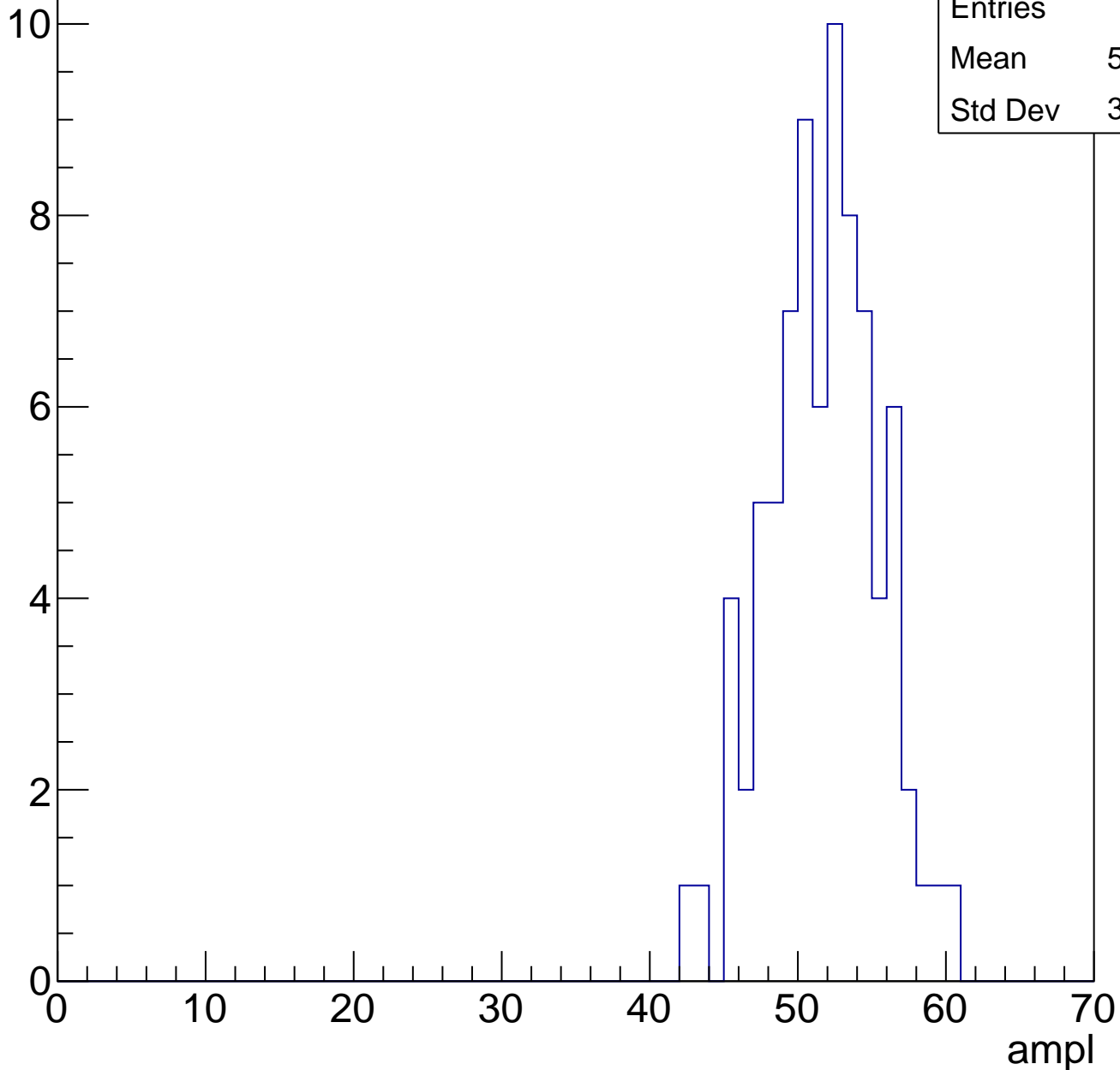


# B1L102S, U20-ch112, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	80
Mean	51.25
Std Dev	3.676

Entry

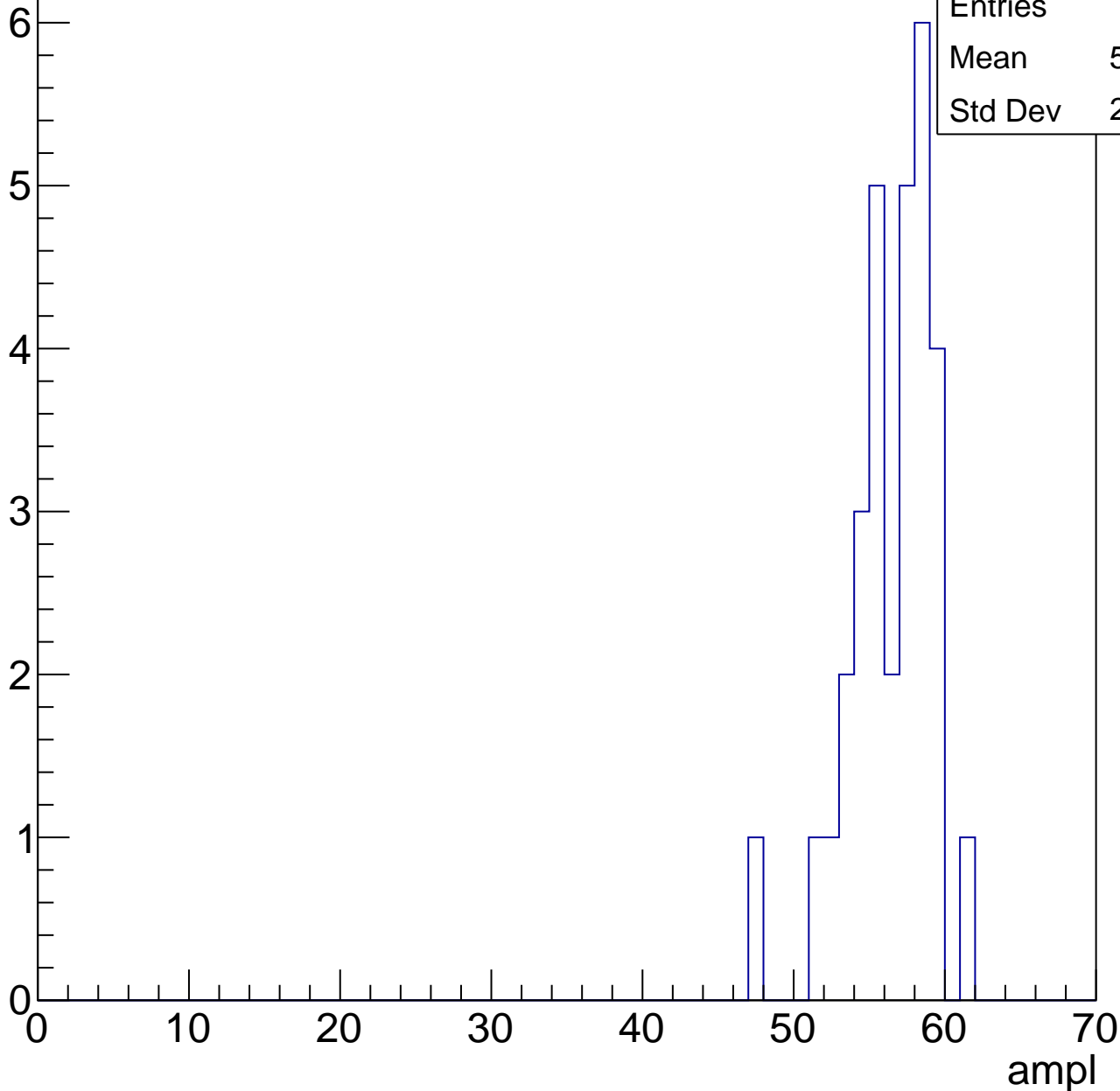


# B1L102S, U20-ch112, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	31
Mean	55.97
Std Dev	2.823

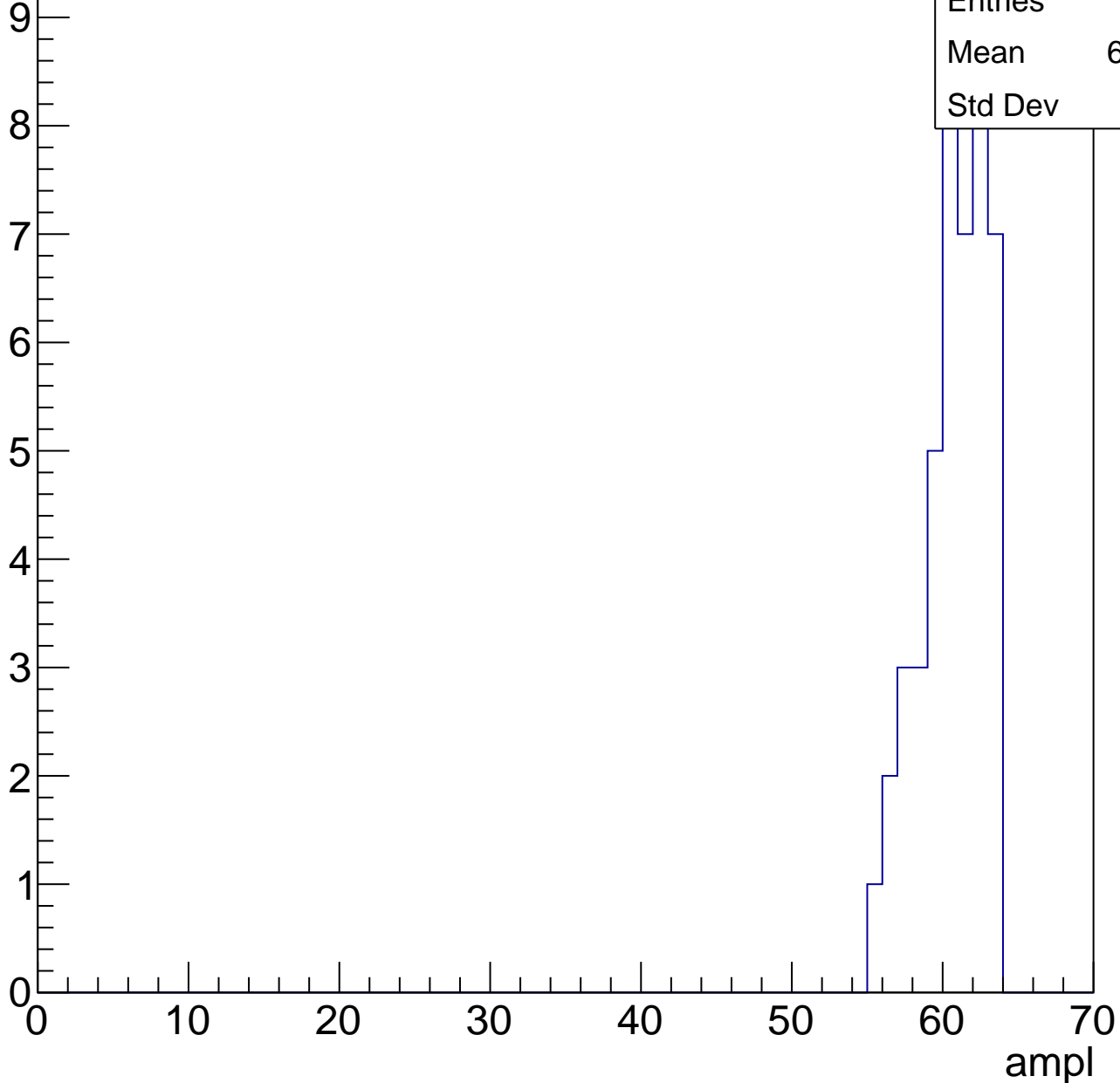


# B1L102S, U20-ch112, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

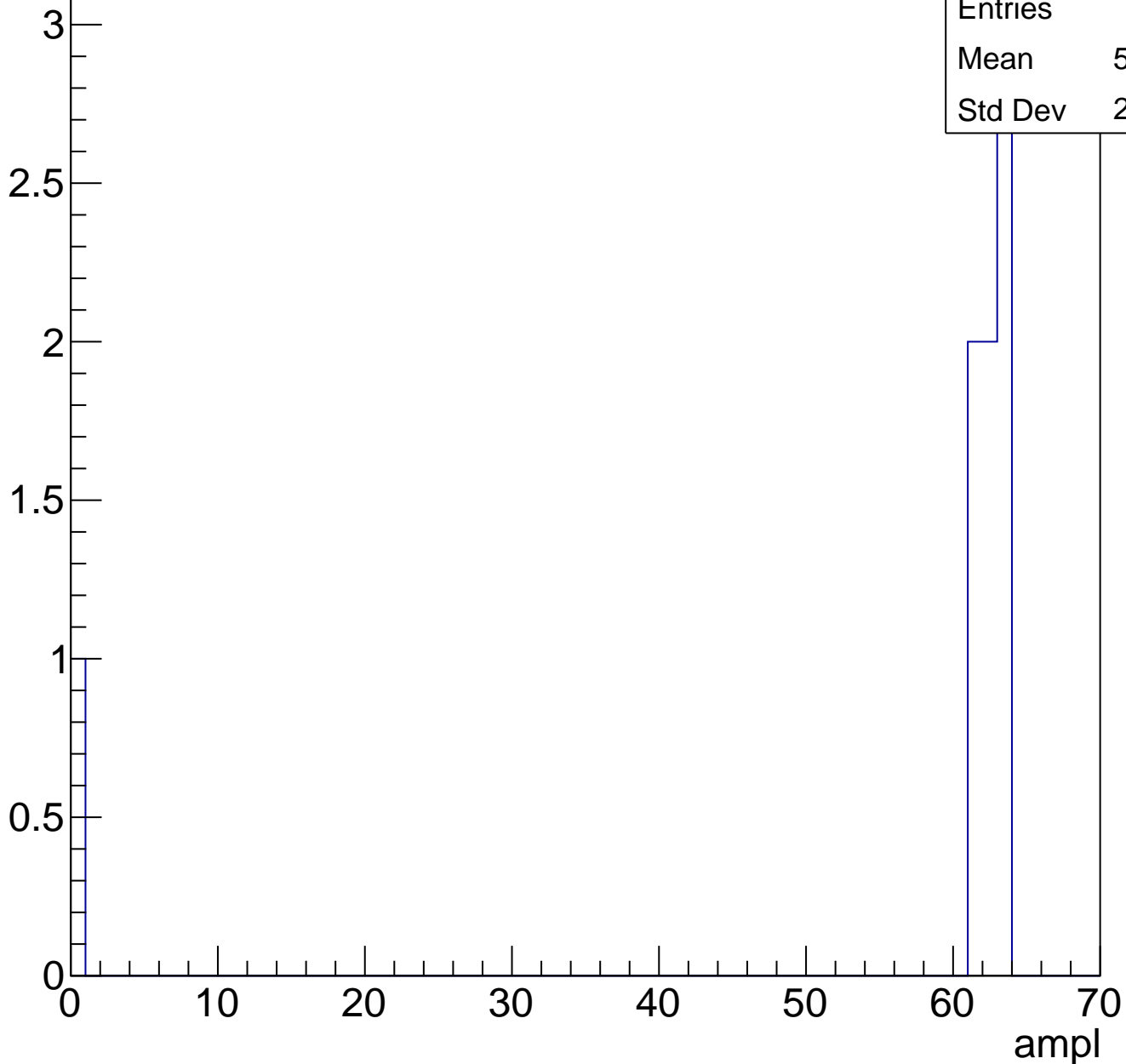
Entries	45
Mean	60.24
Std Dev	2.11



# B1L102S, U20-ch112, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

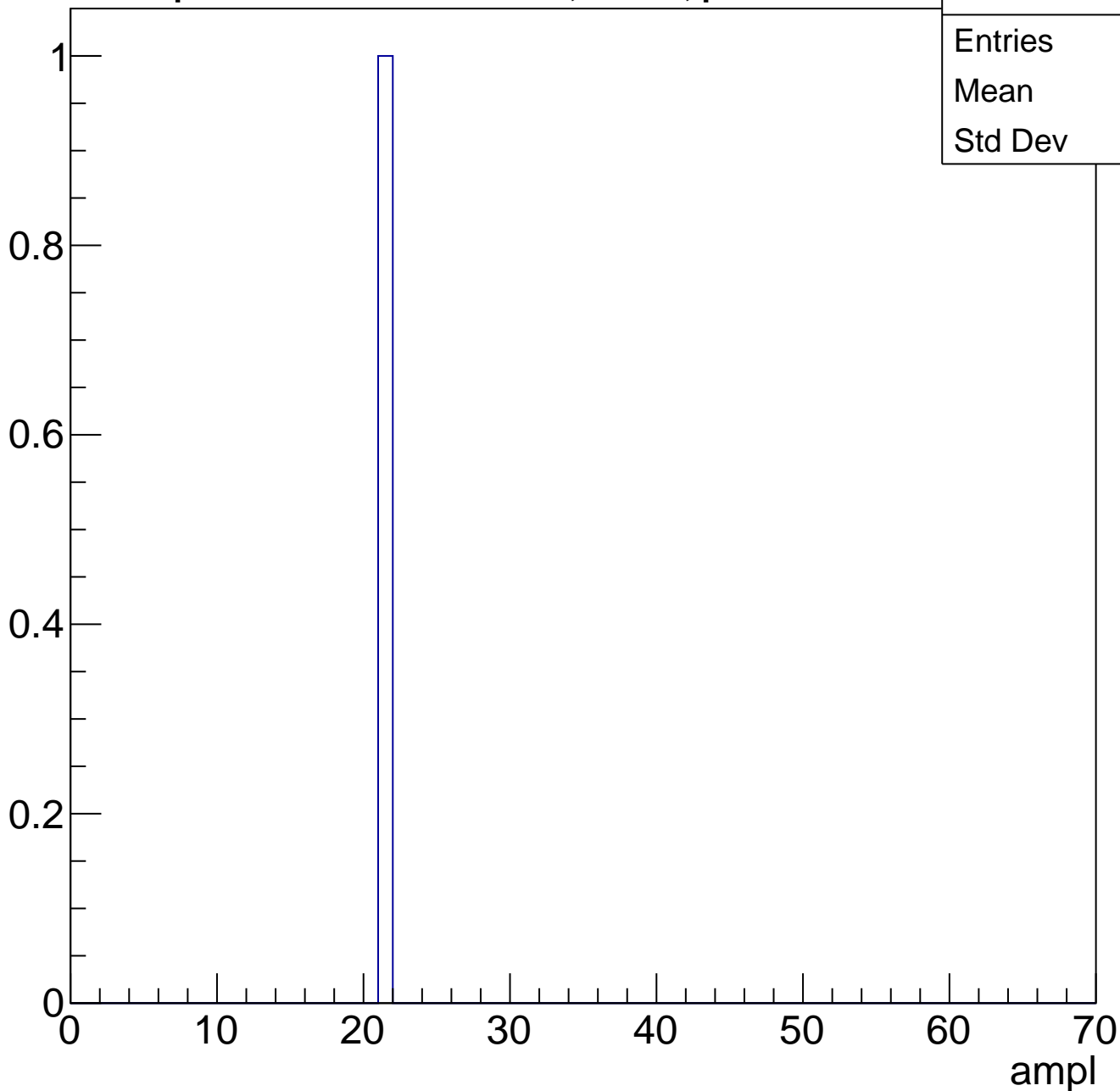




# B1L102S, U20-ch112, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch113, adc0

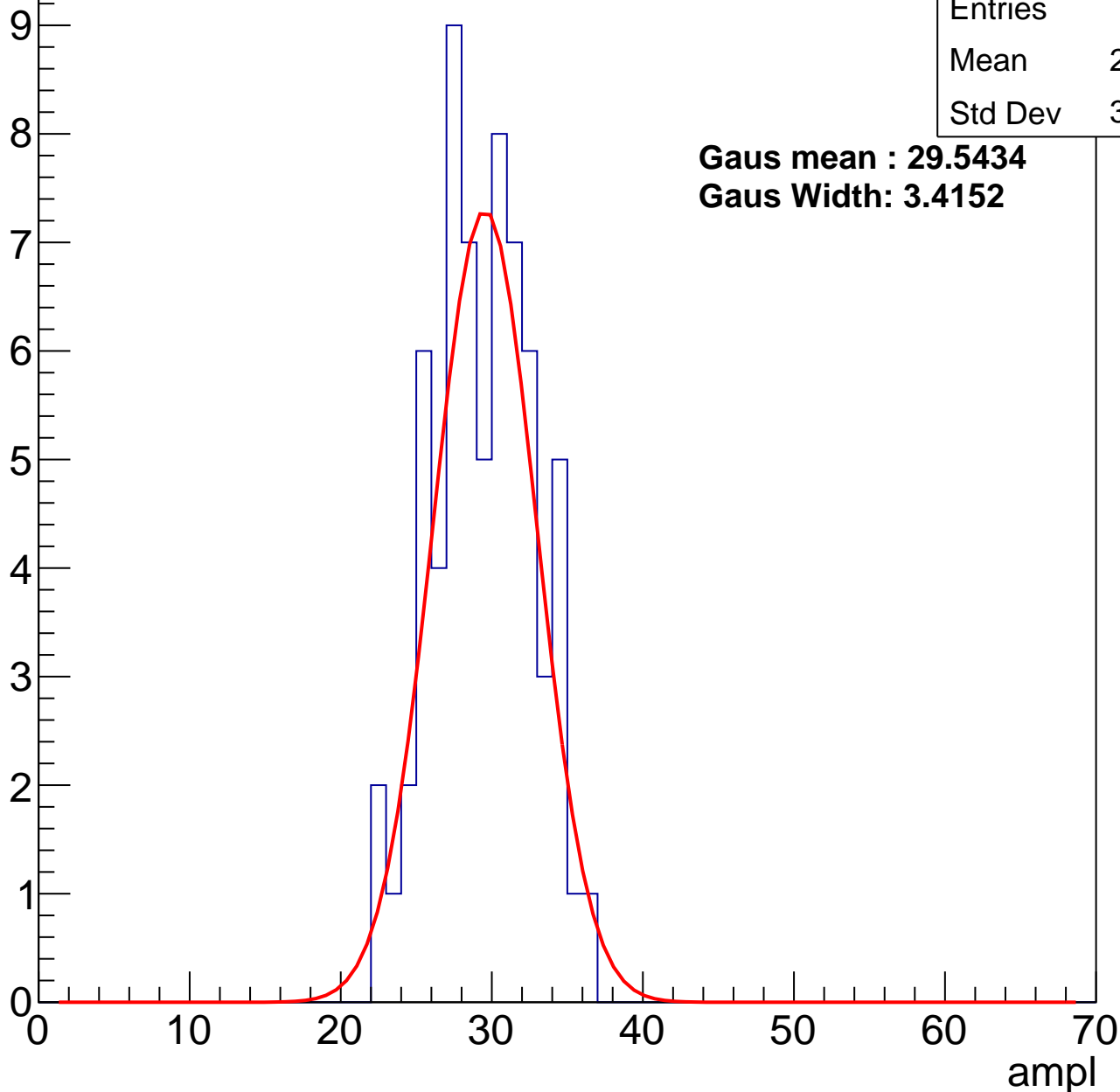
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	28.99
Std Dev	3.248

**Gaus mean : 29.5434**

**Gaus Width: 3.4152**



# B1L102S, U20-ch113, adc1

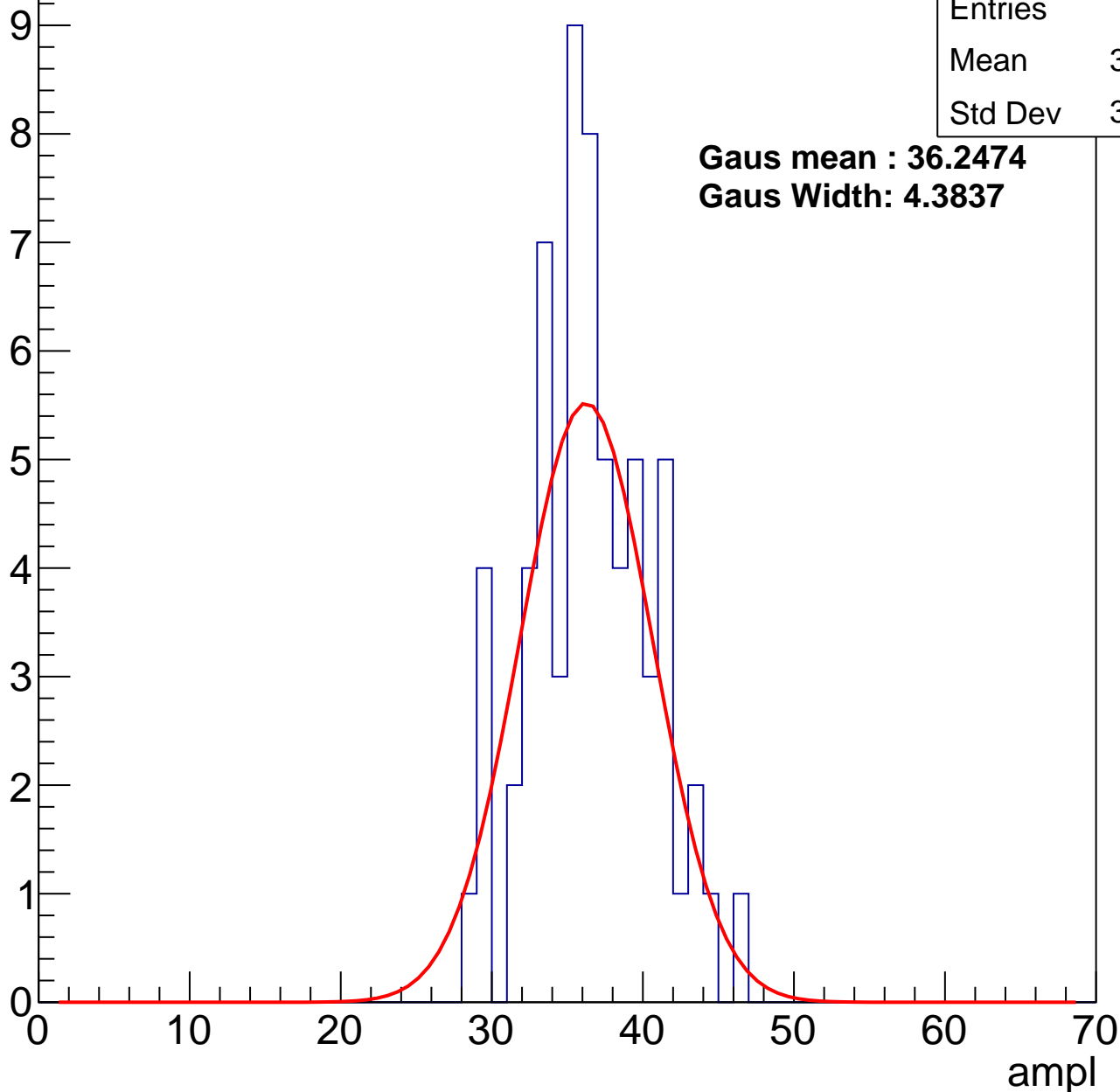
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	36.08
Std Dev	3.912

**Gaus mean : 36.2474**

**Gaus Width: 4.3837**



# B1L102S, U20-ch113, adc2

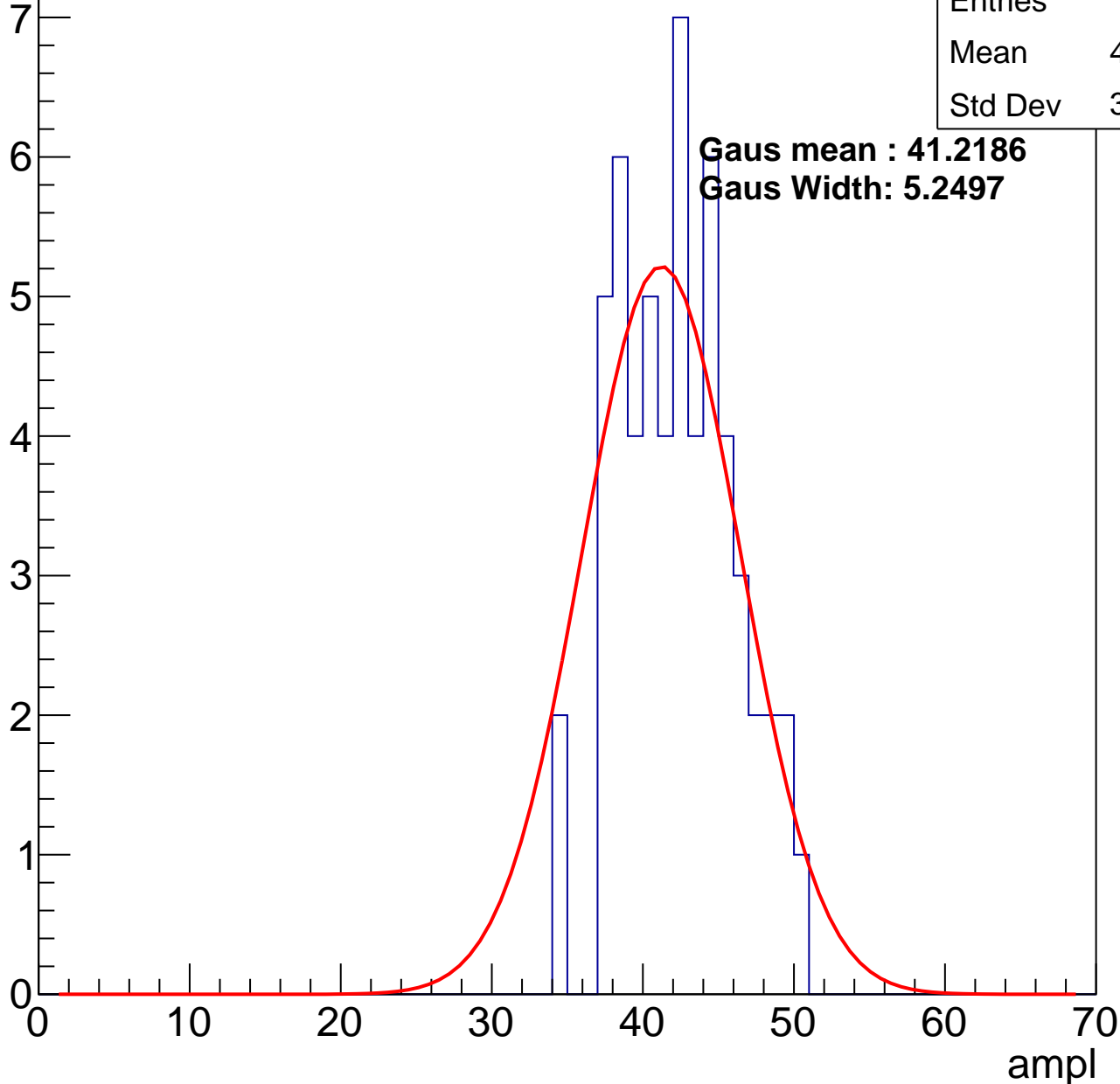
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	41.88
Std Dev	3.756

**Gaus mean : 41.2186**

**Gaus Width: 5.2497**

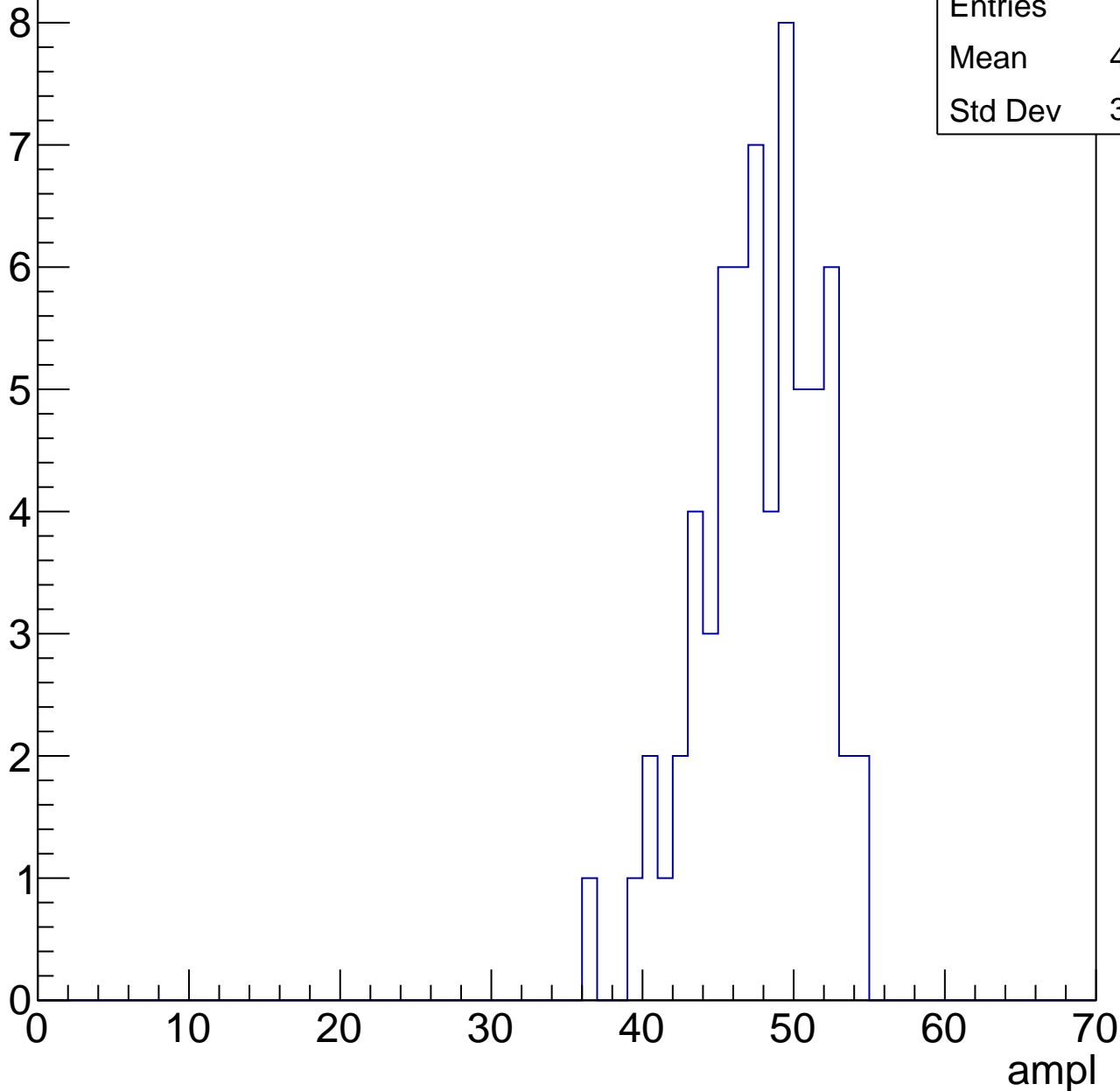


# B1L102S, U20-ch113, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	47.29
Std Dev	3.854



# B1L102S, U20-ch113, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

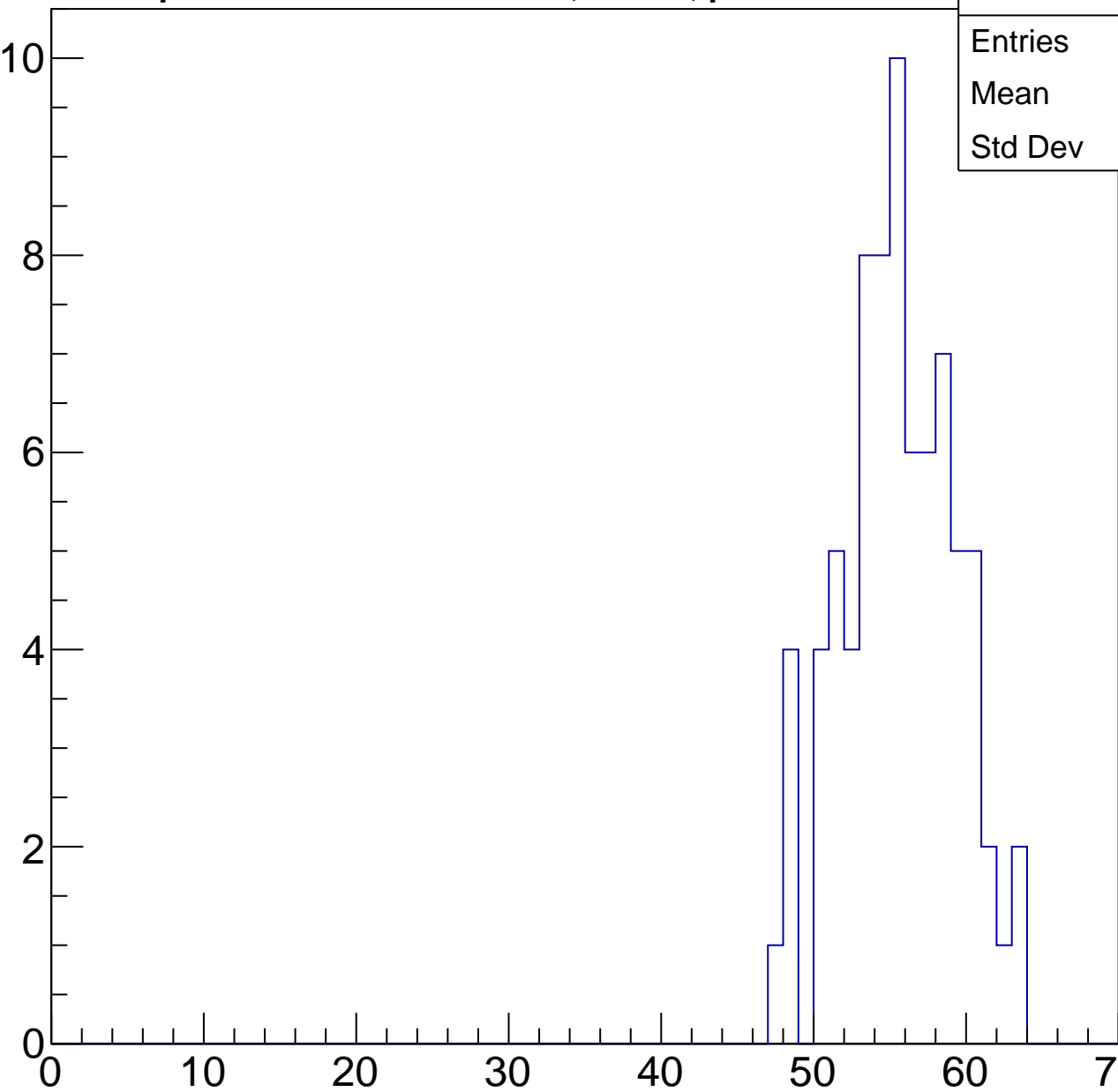
Entries	78
Mean	55.09
Std Dev	3.691

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

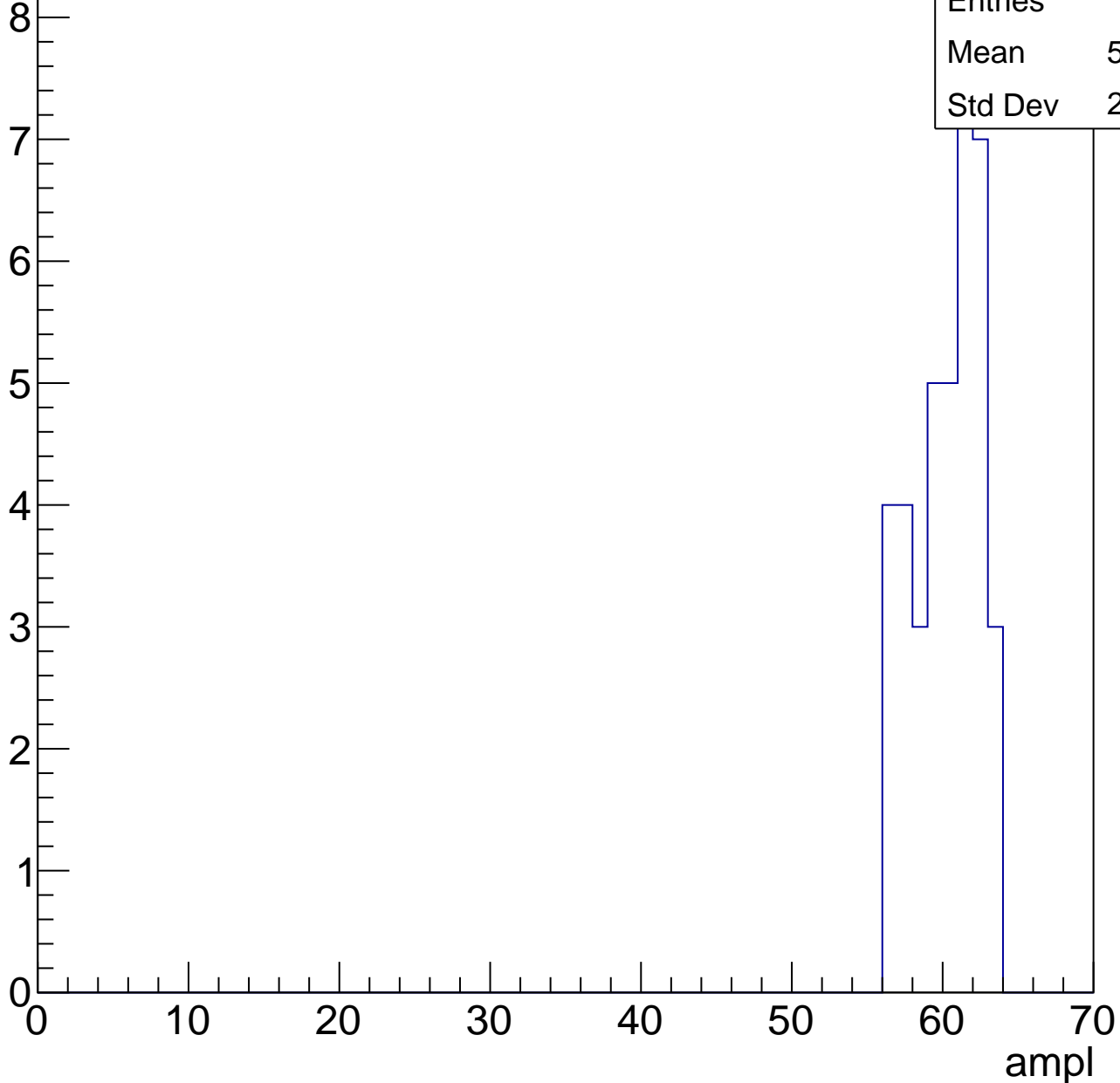


# B1L102S, U20-ch113, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	39
Mean	59.79
Std Dev	2.139

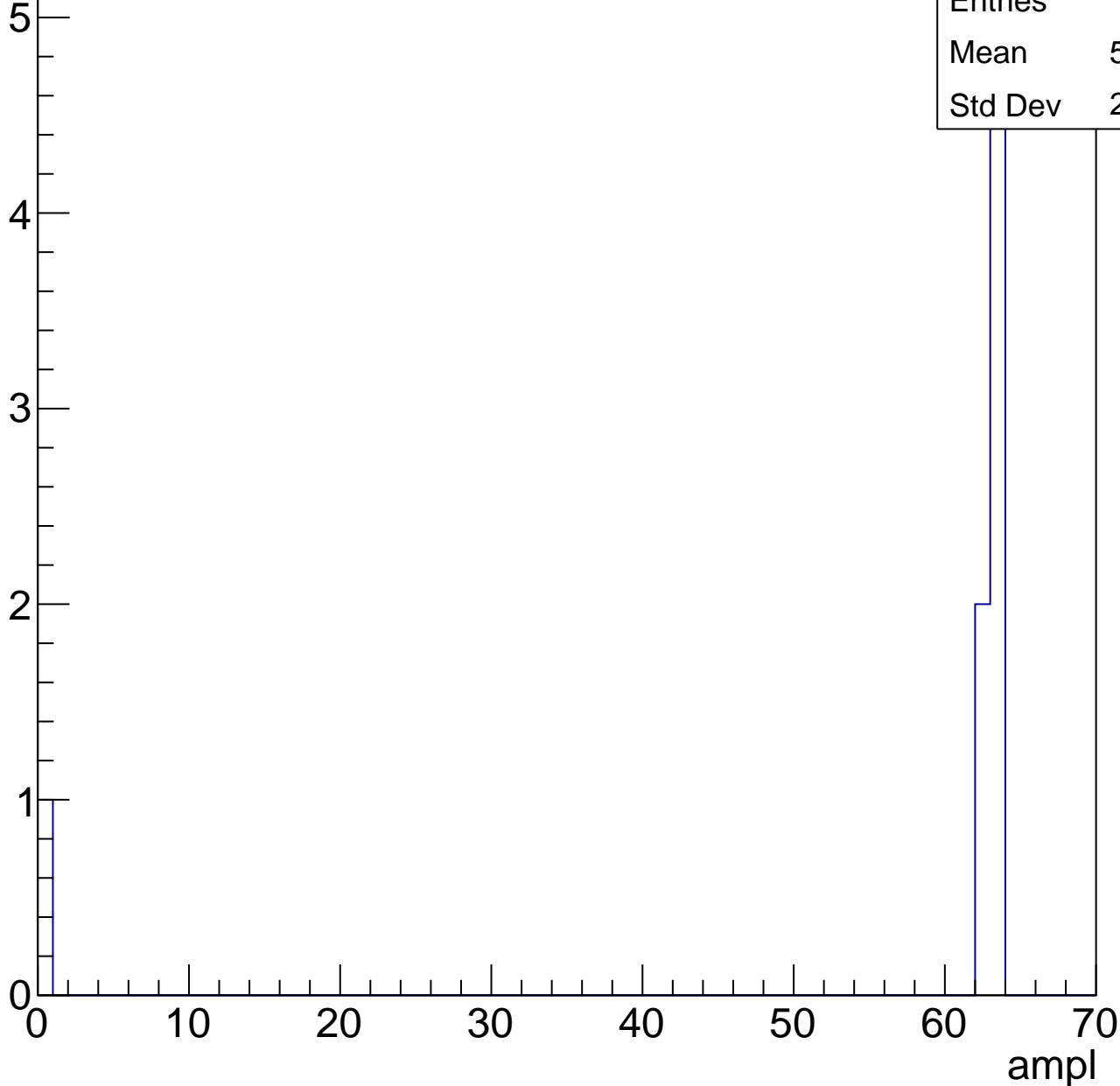


# B1L102S, U20-ch113, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	8
Mean	54.88
Std Dev	20.75





# B1L102S, U20-ch113, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch114, adc0

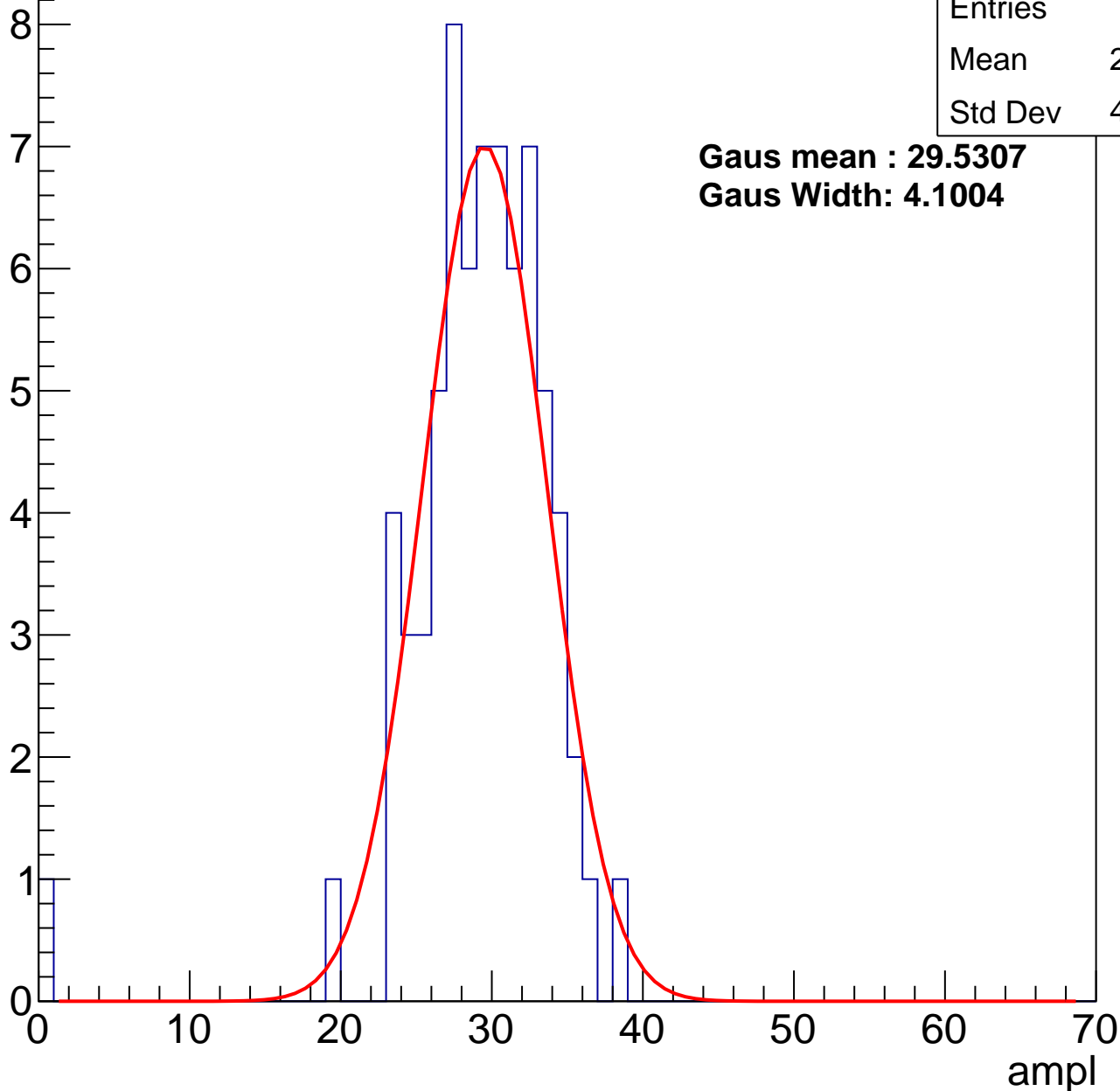
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	28.73
Std Dev	4.982

**Gaus mean : 29.5307**

**Gaus Width: 4.1004**



# B1L102S, U20-ch114, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	71
Mean	36.41
Std Dev	3.574

**Gaus mean : 36.7538**

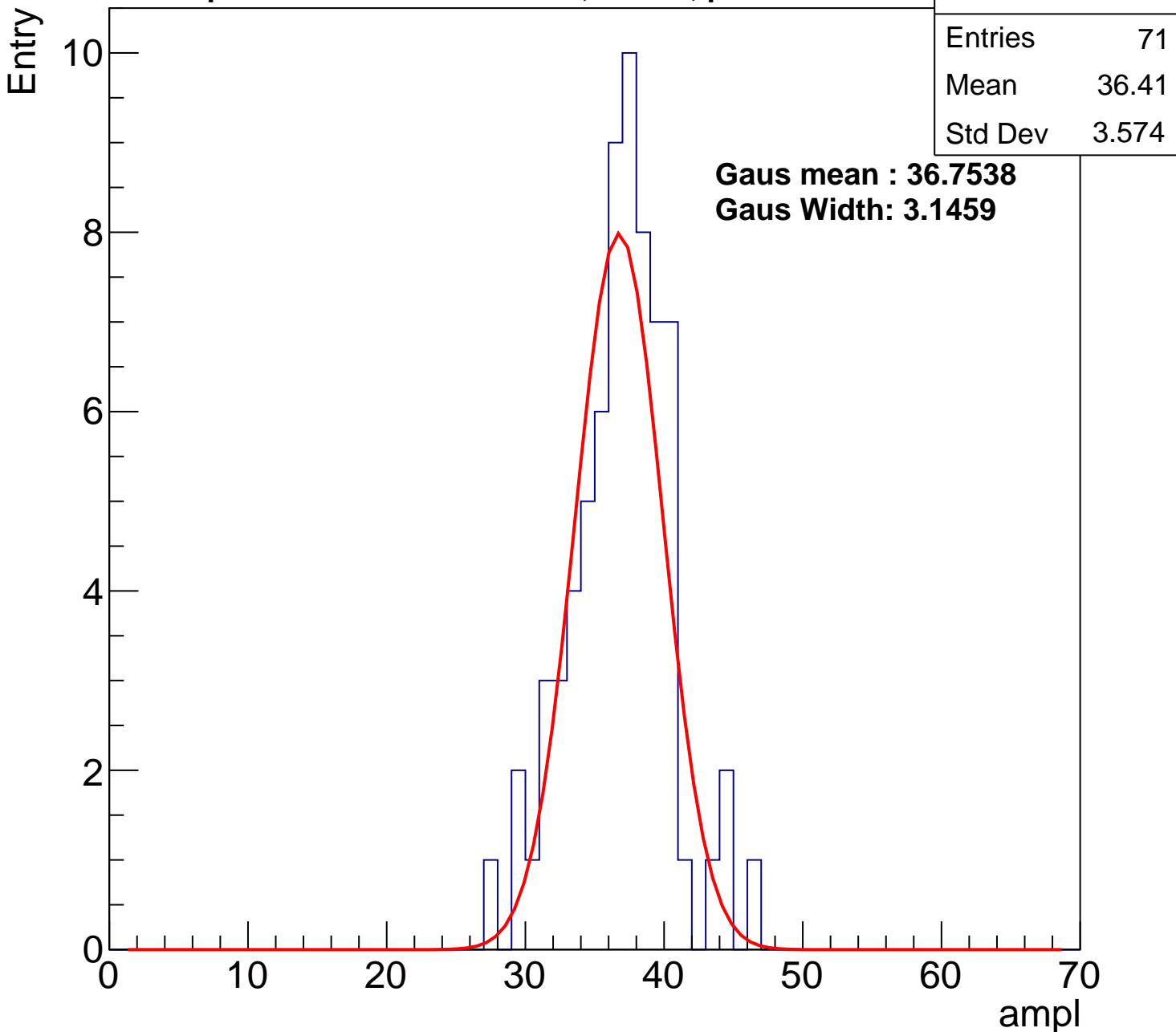
**Gaus Width: 3.1459**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U20-ch114, adc2

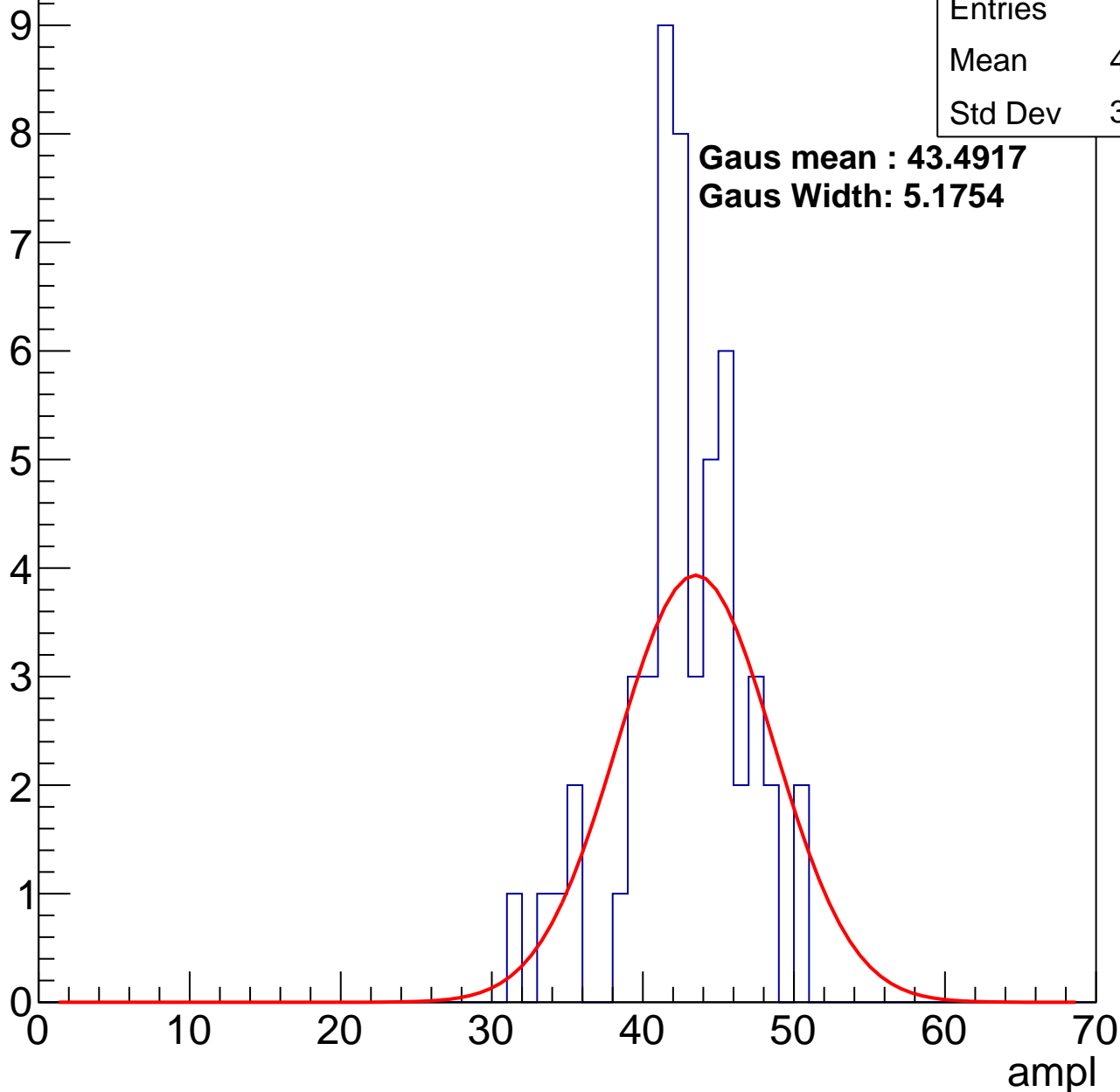
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	42.23
Std Dev	3.945

**Gaus mean : 43.4917**

**Gaus Width: 5.1754**

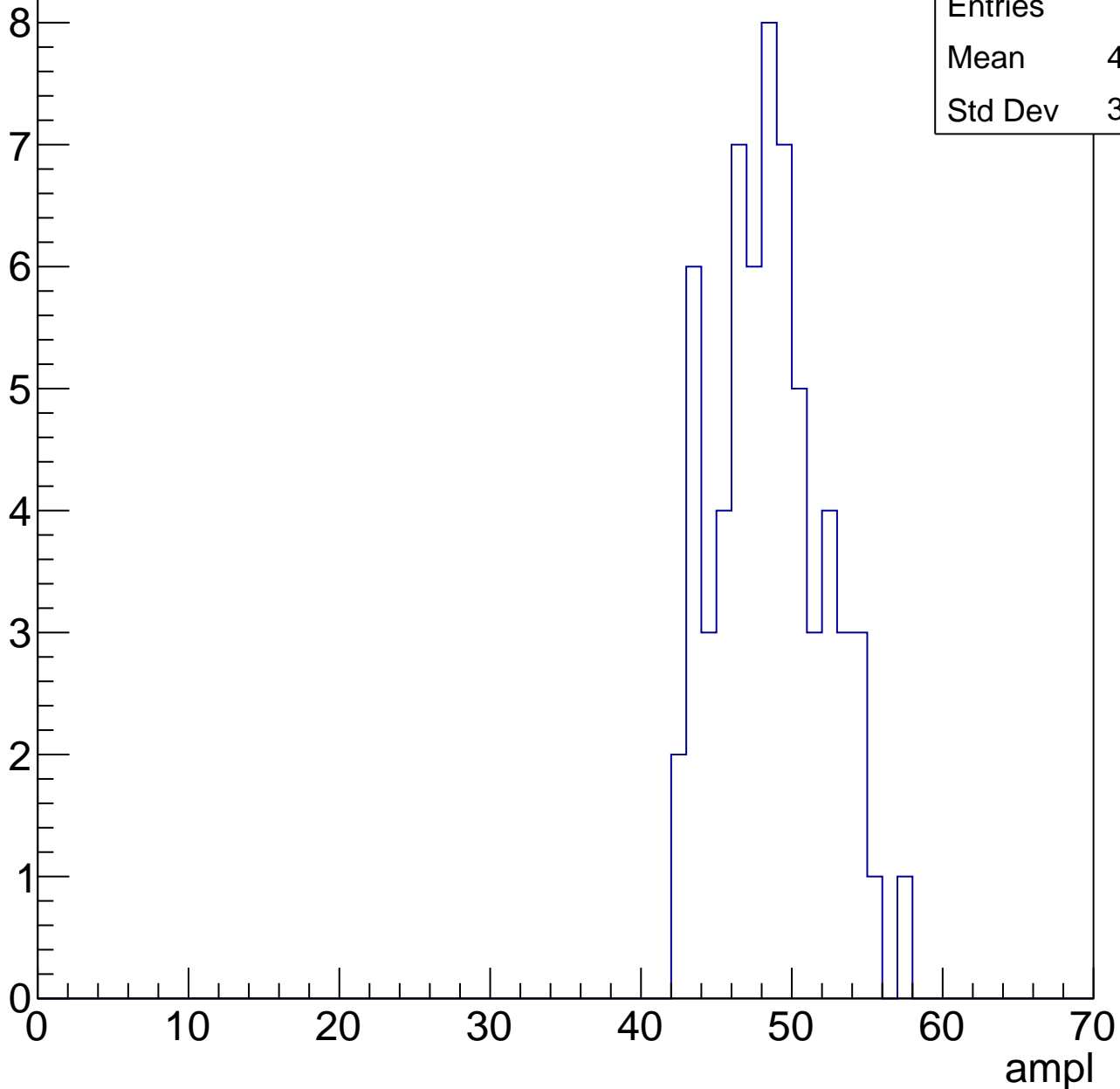


# B1L102S, U20-ch114, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	48.08
Std Dev	3.497

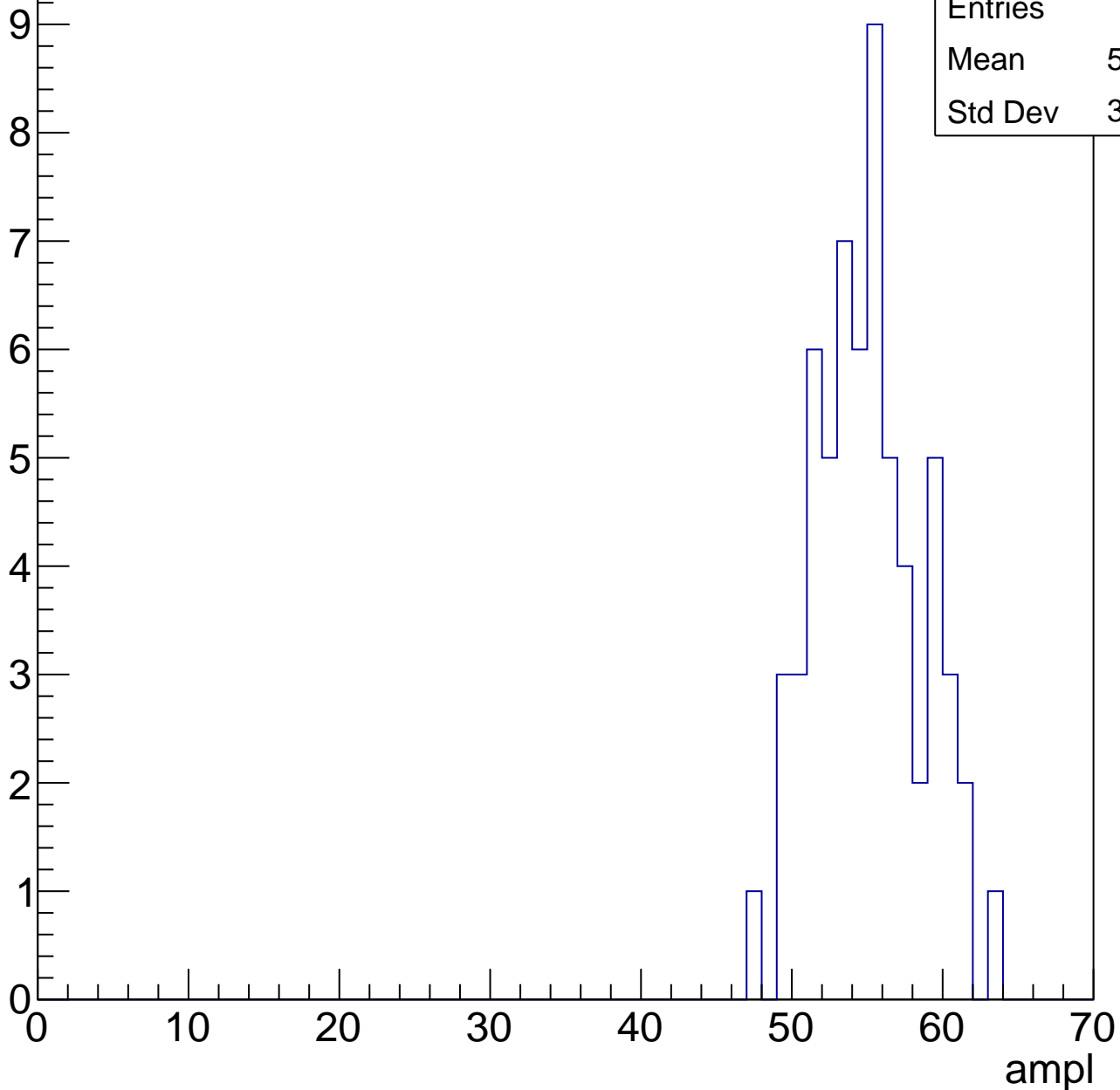


# B1L102S, U20-ch114, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	54.58
Std Dev	3.457

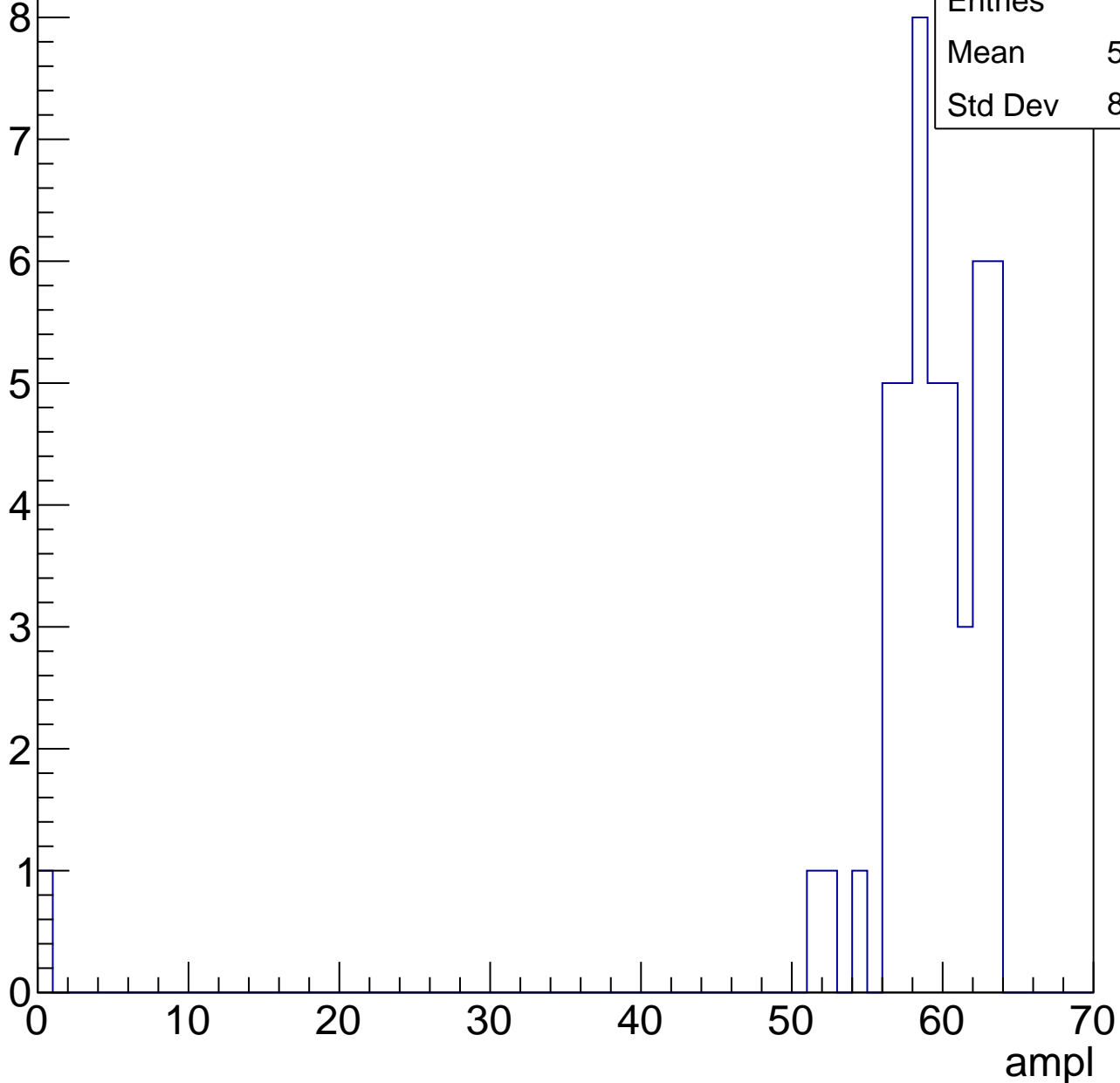


# B1L102S, U20-ch114, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	47
Mean	57.74
Std Dev	8.974

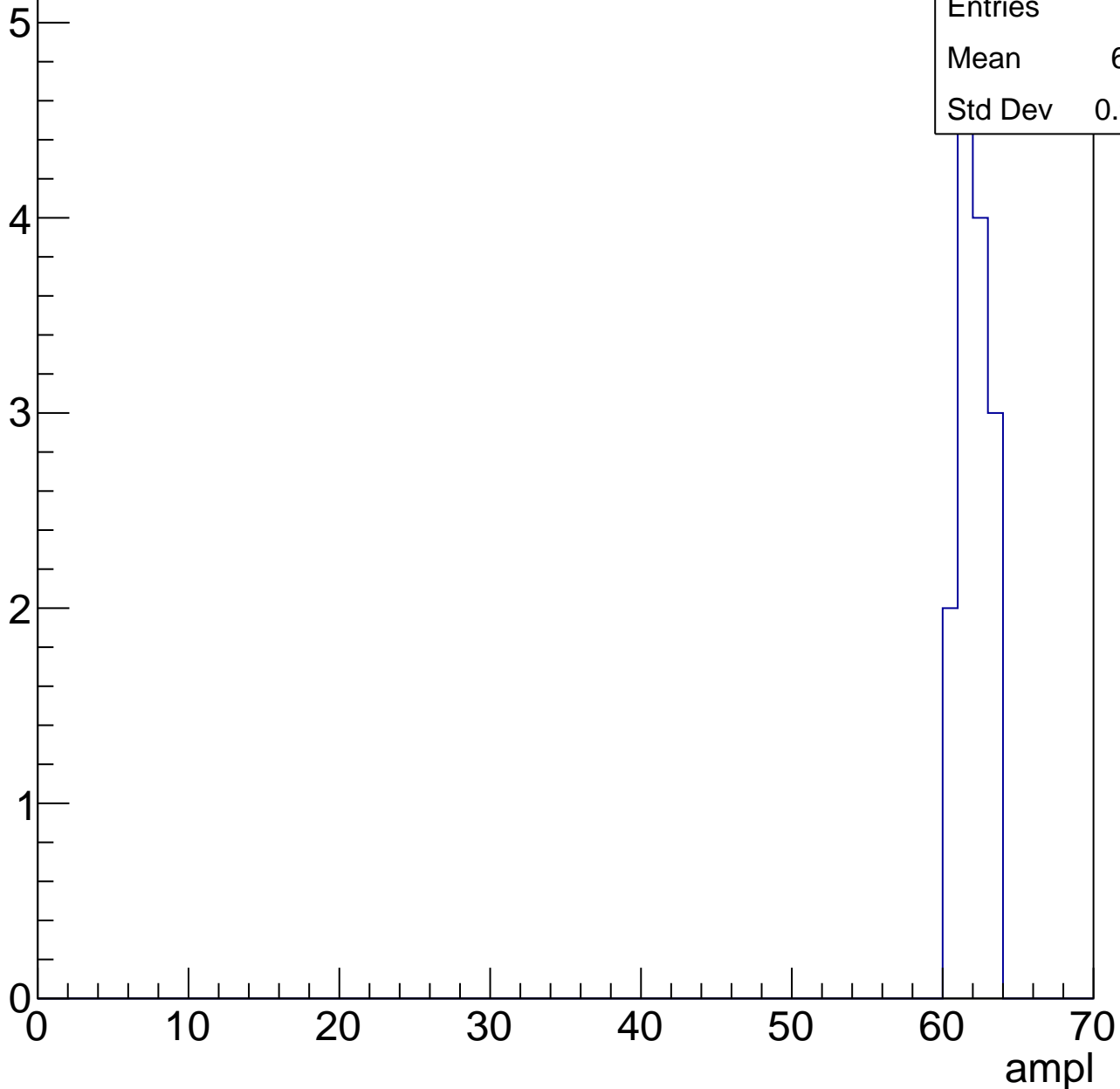


# B1L102S, U20-ch114, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	14
Mean	61.57
Std Dev	0.9794





# B1L102S, U20-ch114, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch115, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	71
Mean	30.42
Std Dev	3.372

**Gaus mean : 30.8944**

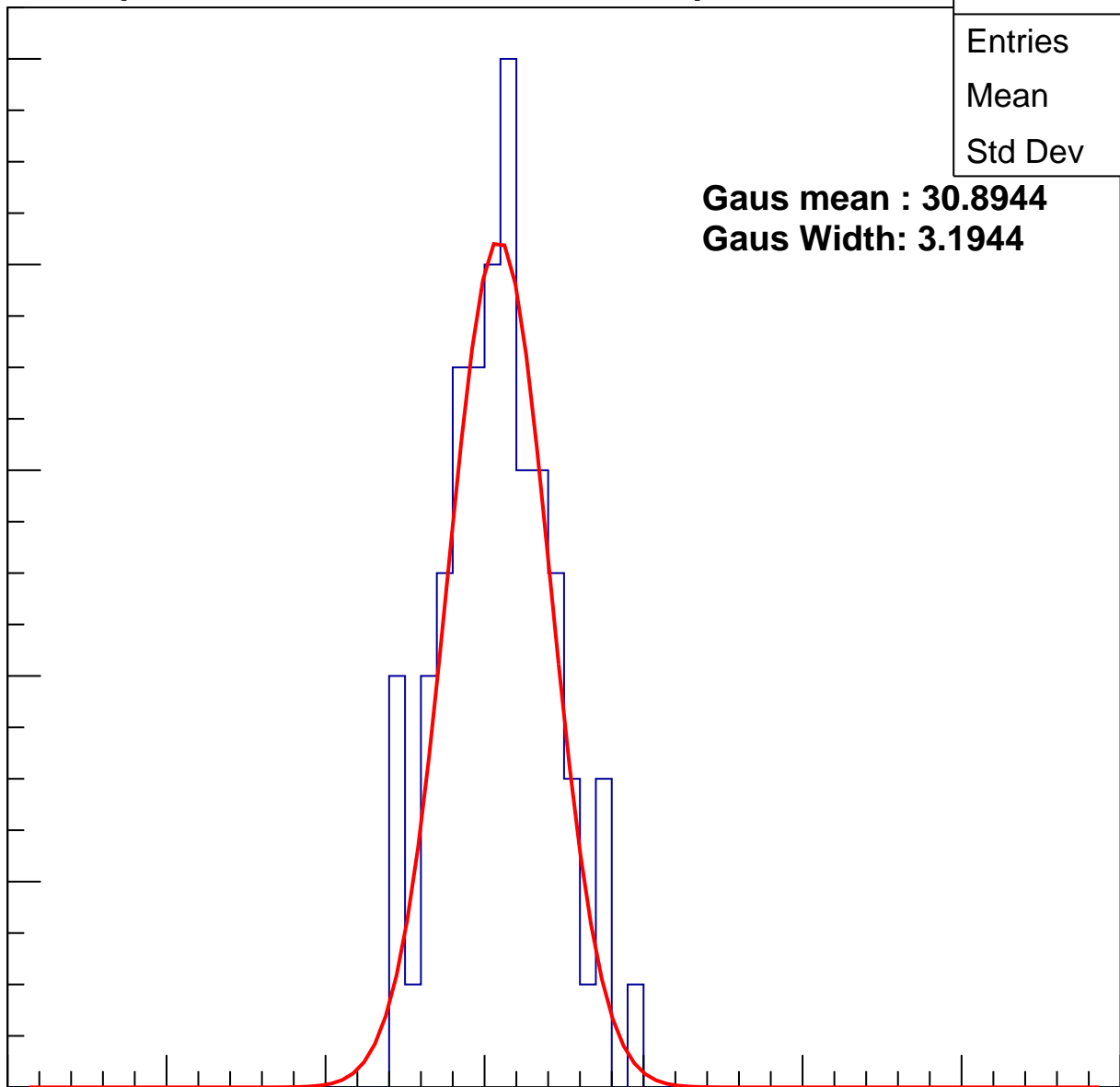
**Gaus Width: 3.1944**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U20-ch115, adc1

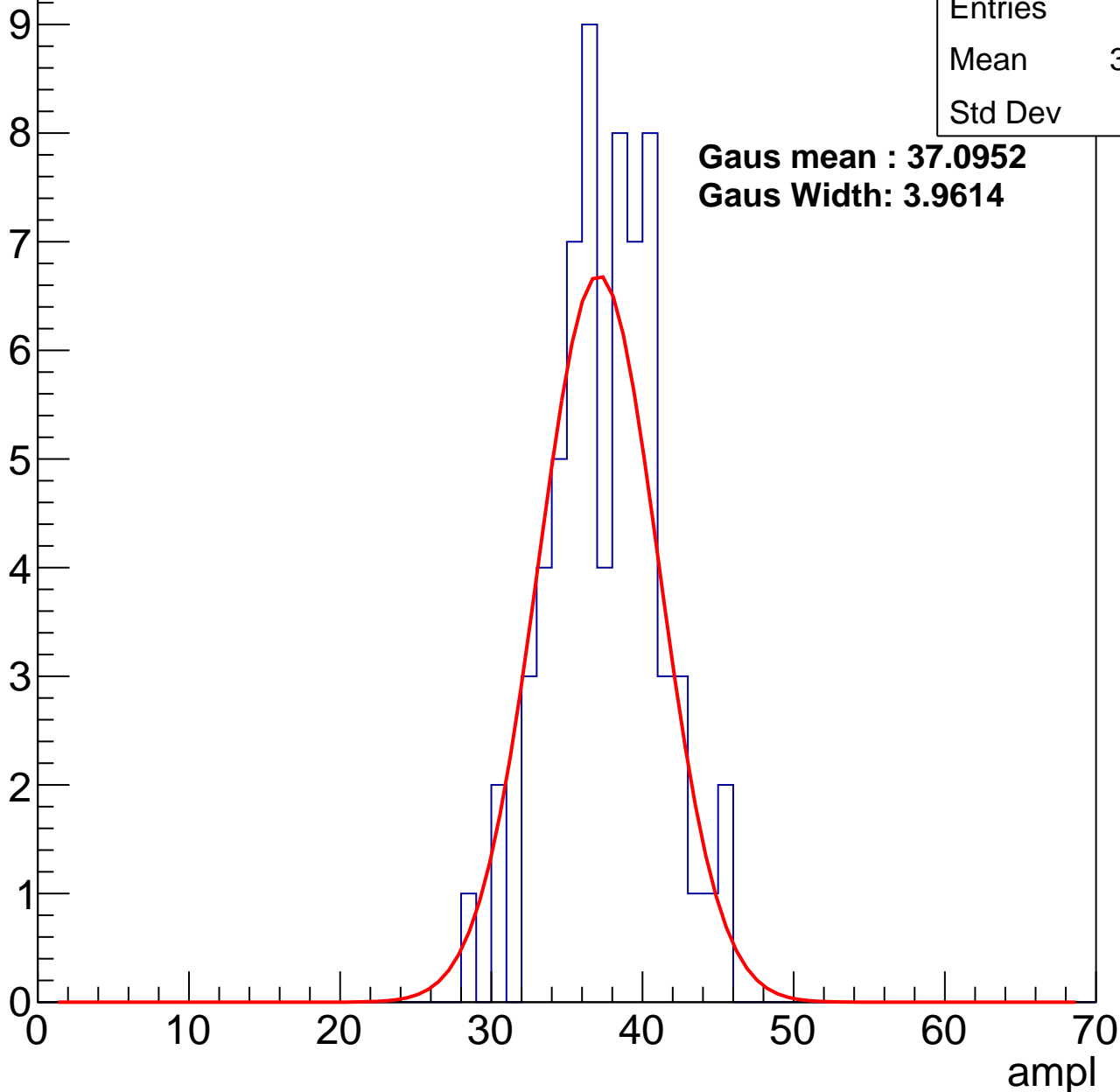
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	37.15
Std Dev	3.52

**Gaus mean : 37.0952**

**Gaus Width: 3.9614**



# B1L102S, U20-ch115, adc2

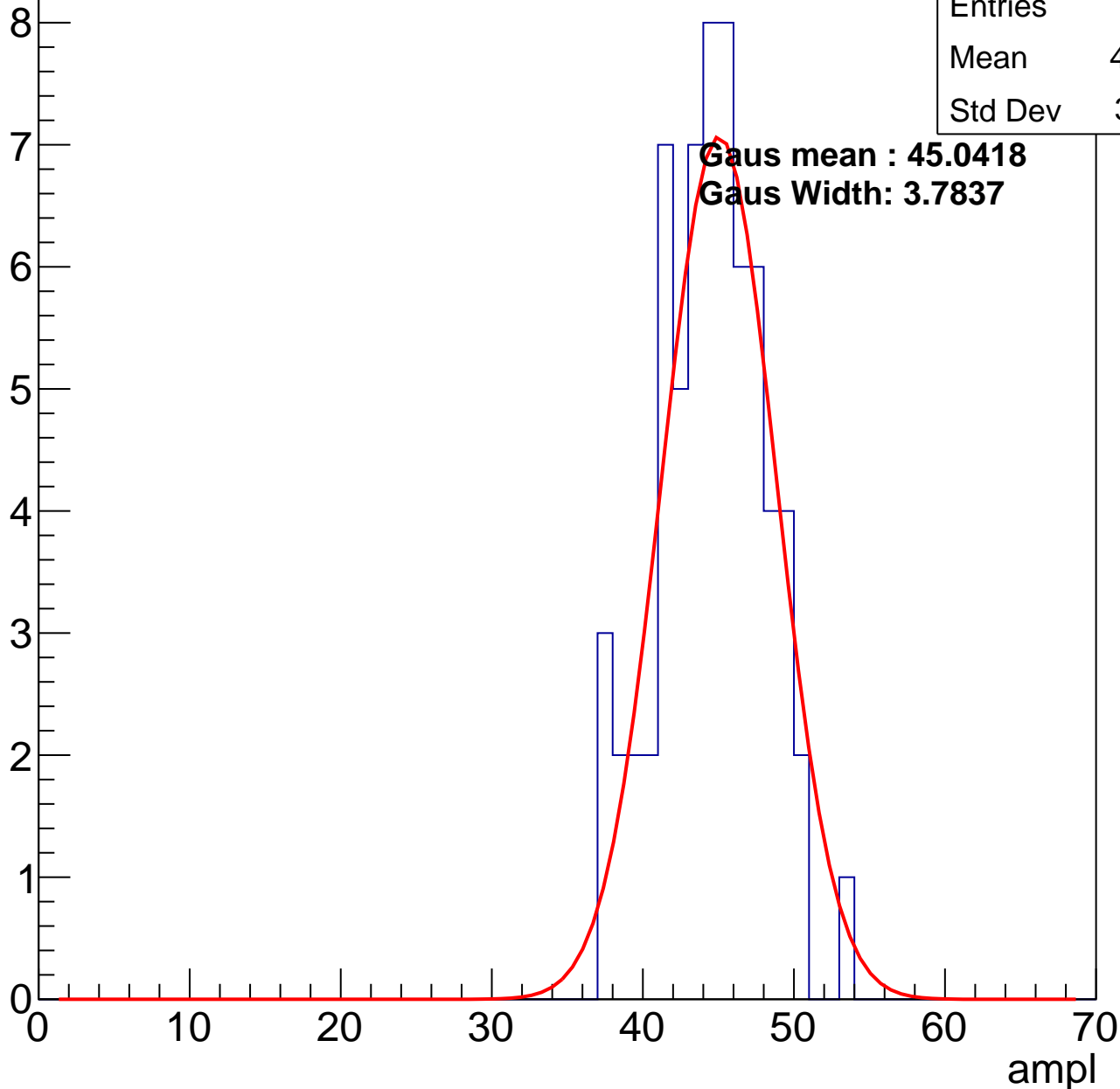
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	44.09
Std Dev	3.441

**Gaus mean : 45.0418**

**Gaus Width: 3.7837**

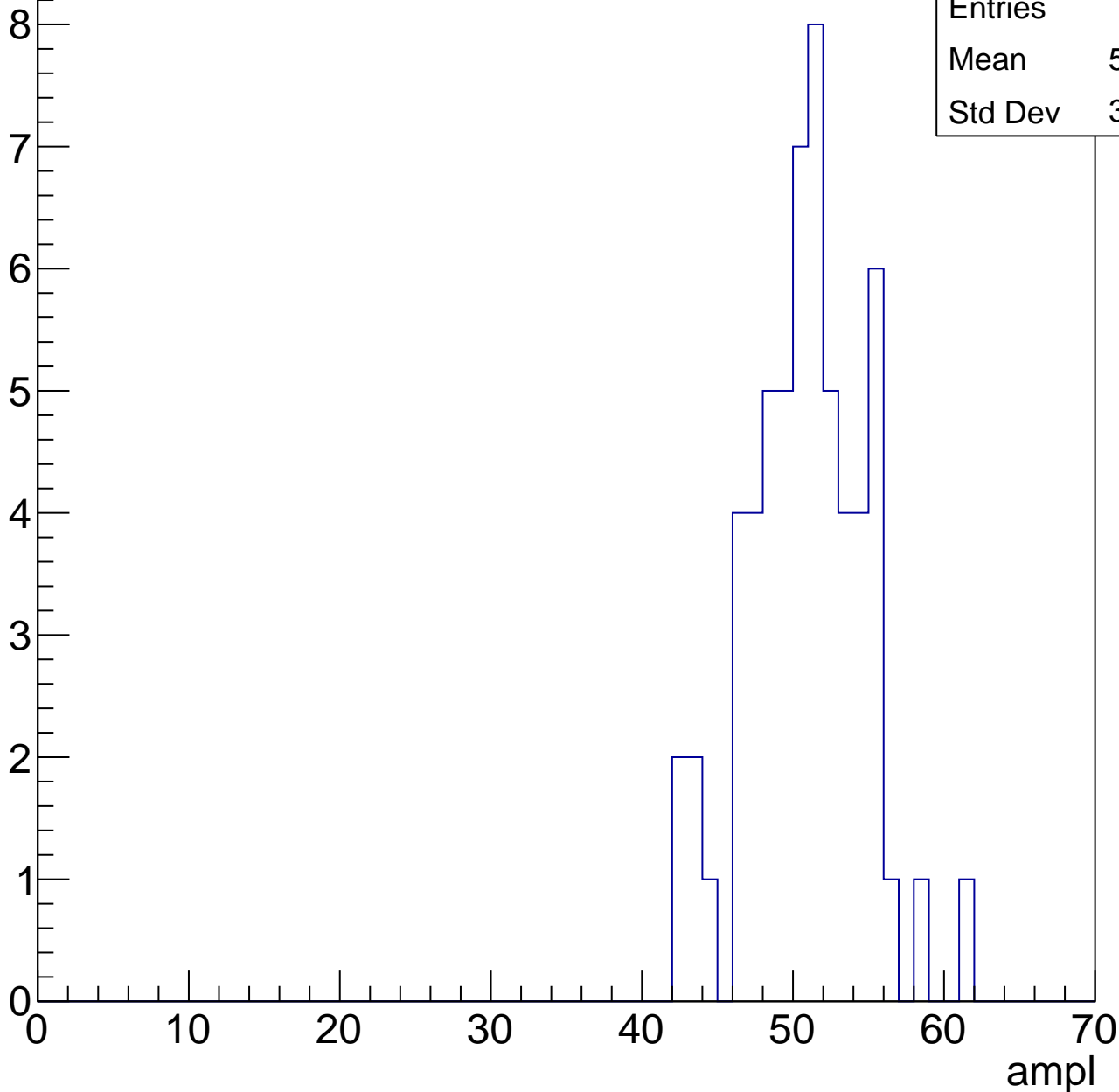


# B1L102S, U20-ch115, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	50.37
Std Dev	3.825

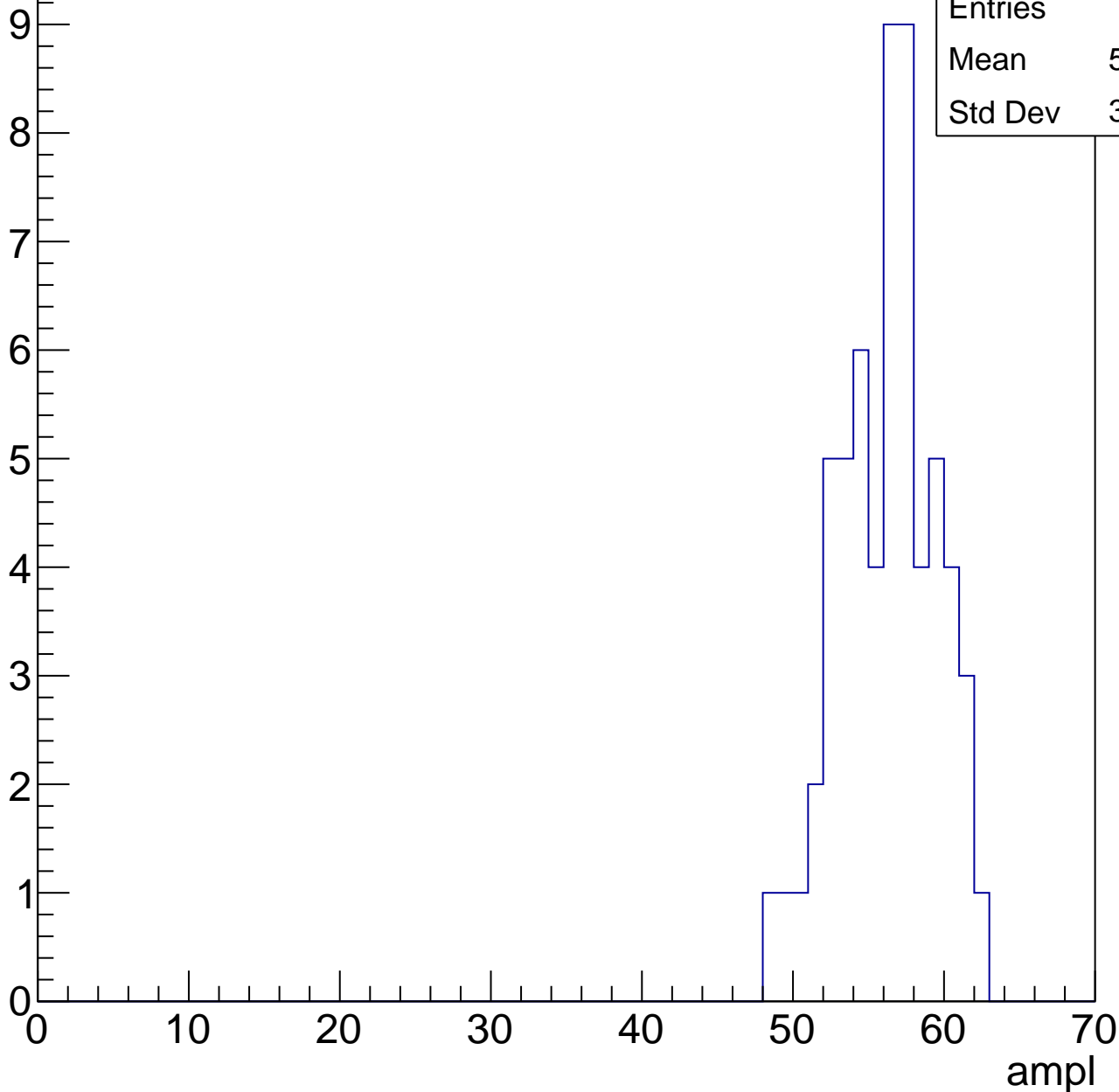


# B1L102S, U20-ch115, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	55.78
Std Dev	3.147

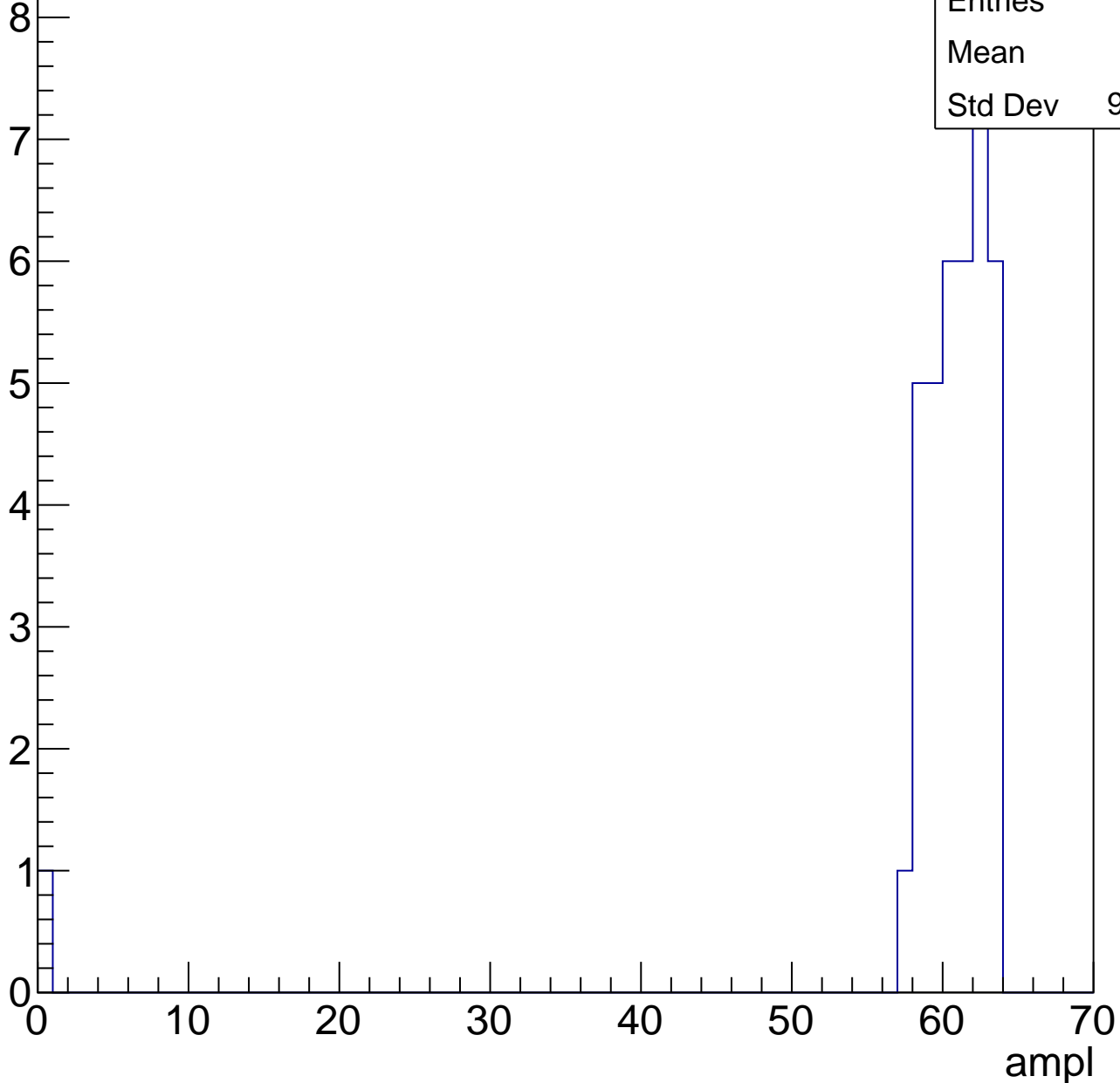


# B1L102S, U20-ch115, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	38
Mean	59
Std Dev	9.852



# B1L102S, U20-ch115, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



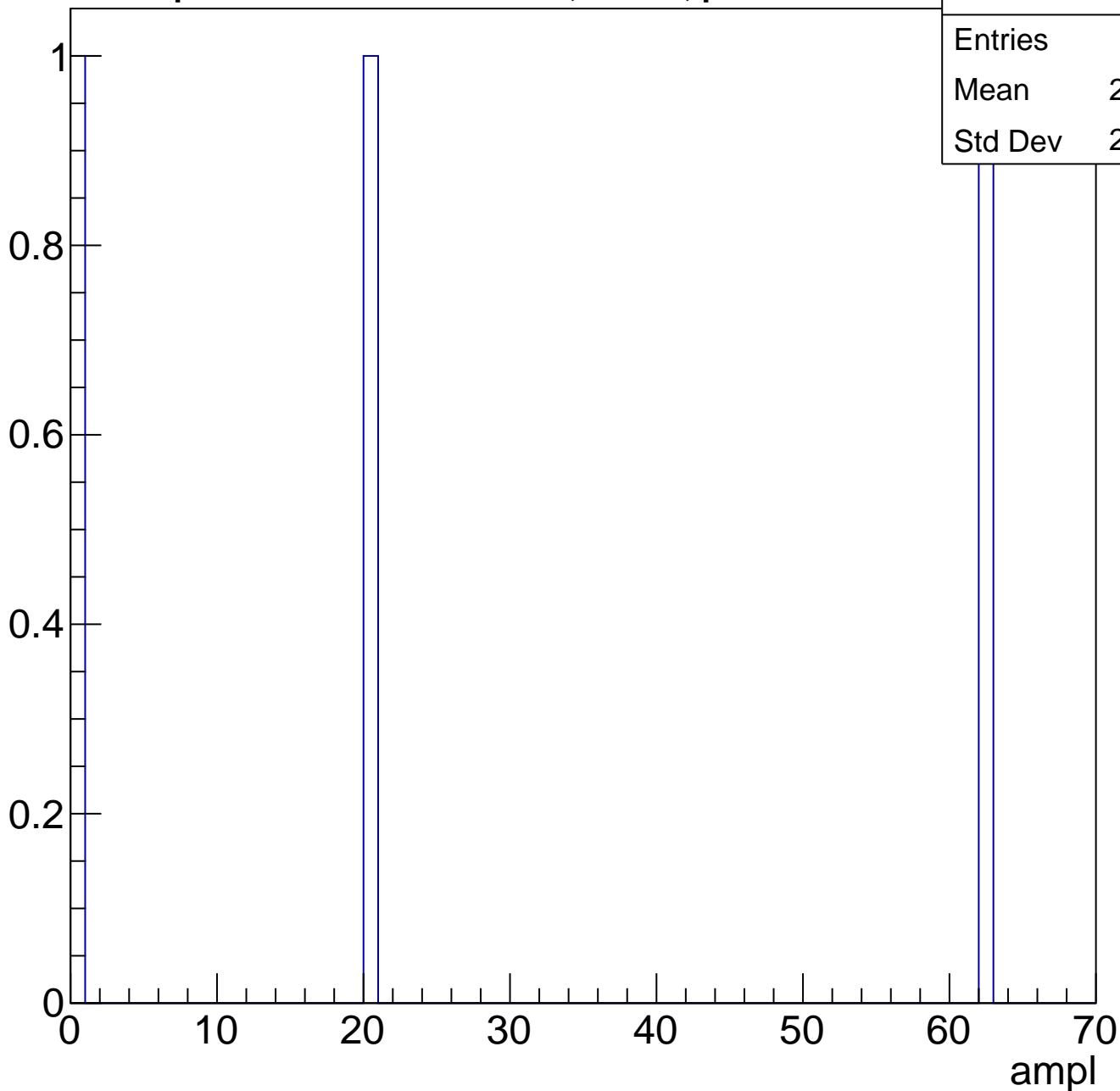
Entries	4
Mean	63
Std Dev	0



# B1L102S, U20-ch115, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	3
Mean	27.33
Std Dev	25.84

# B1L102S, U20-ch116, adc0

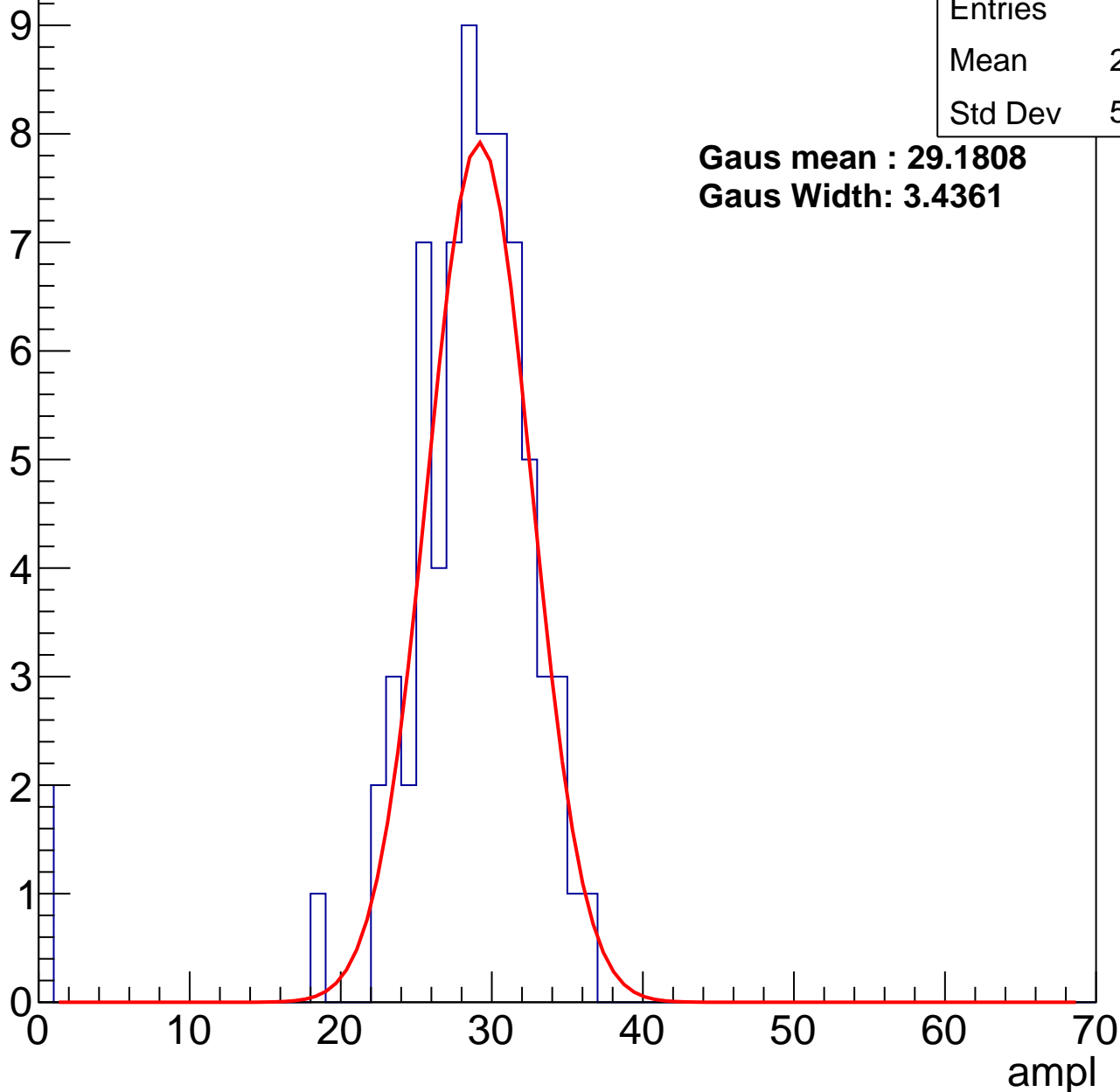
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	27.67
Std Dev	5.739

**Gaus mean : 29.1808**

**Gaus Width: 3.4361**



# B1L102S, U20-ch116, adc1

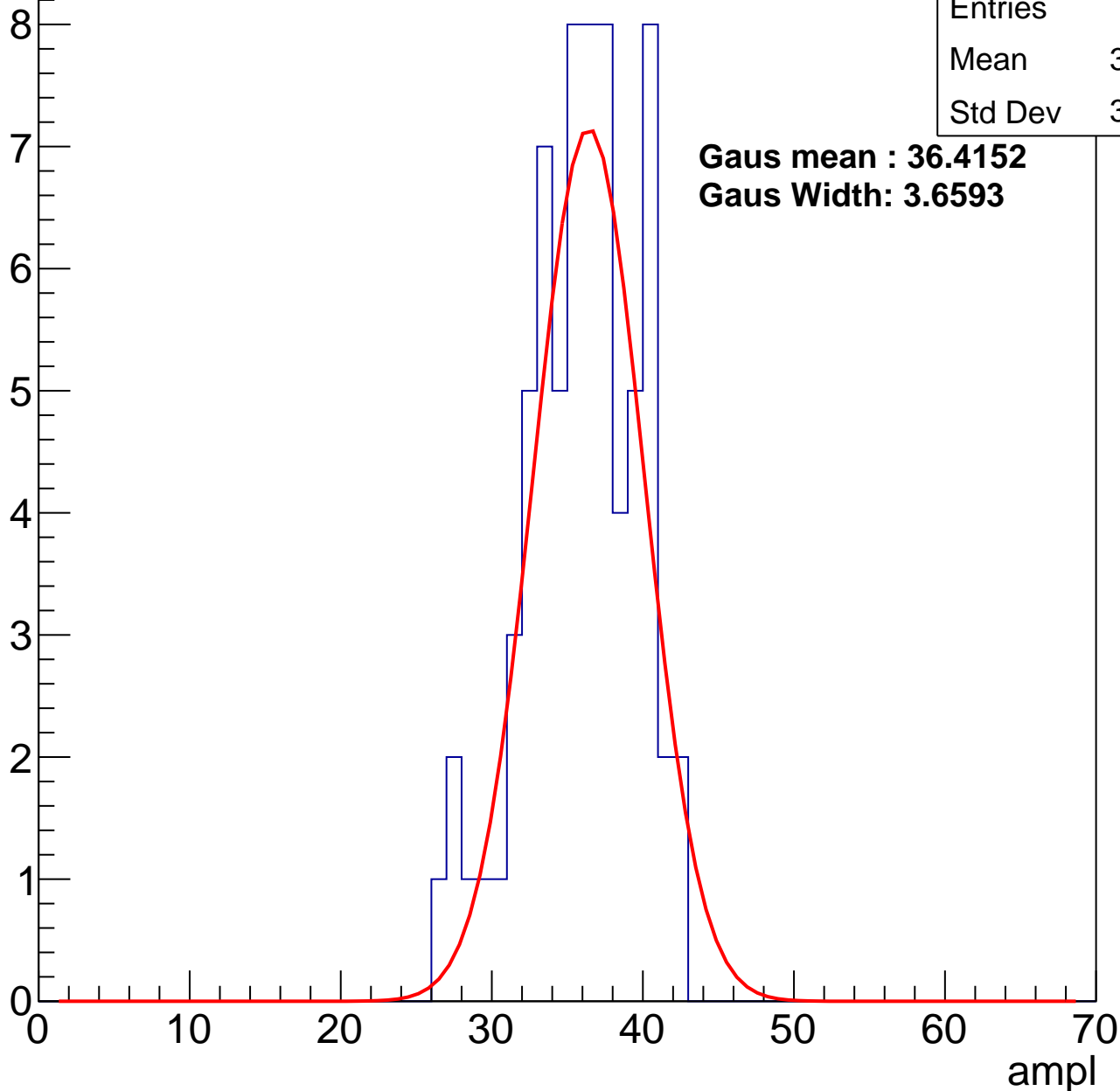
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	35.46
Std Dev	3.669

**Gaus mean : 36.4152**

**Gaus Width: 3.6593**



# B1L102S, U20-ch116, adc2

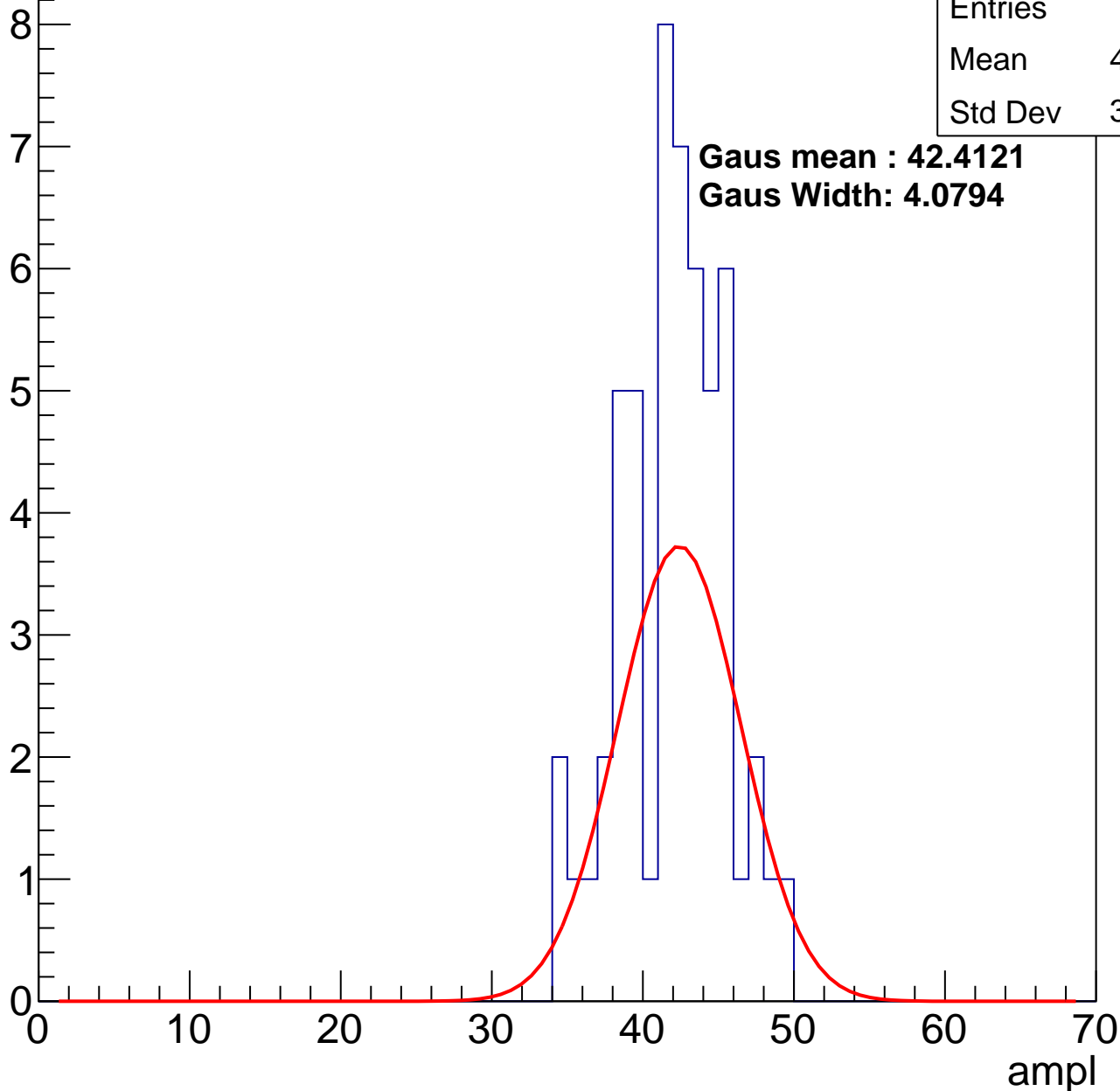
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	41.57
Std Dev	3.392

**Gaus mean : 42.4121**

**Gaus Width: 4.0794**

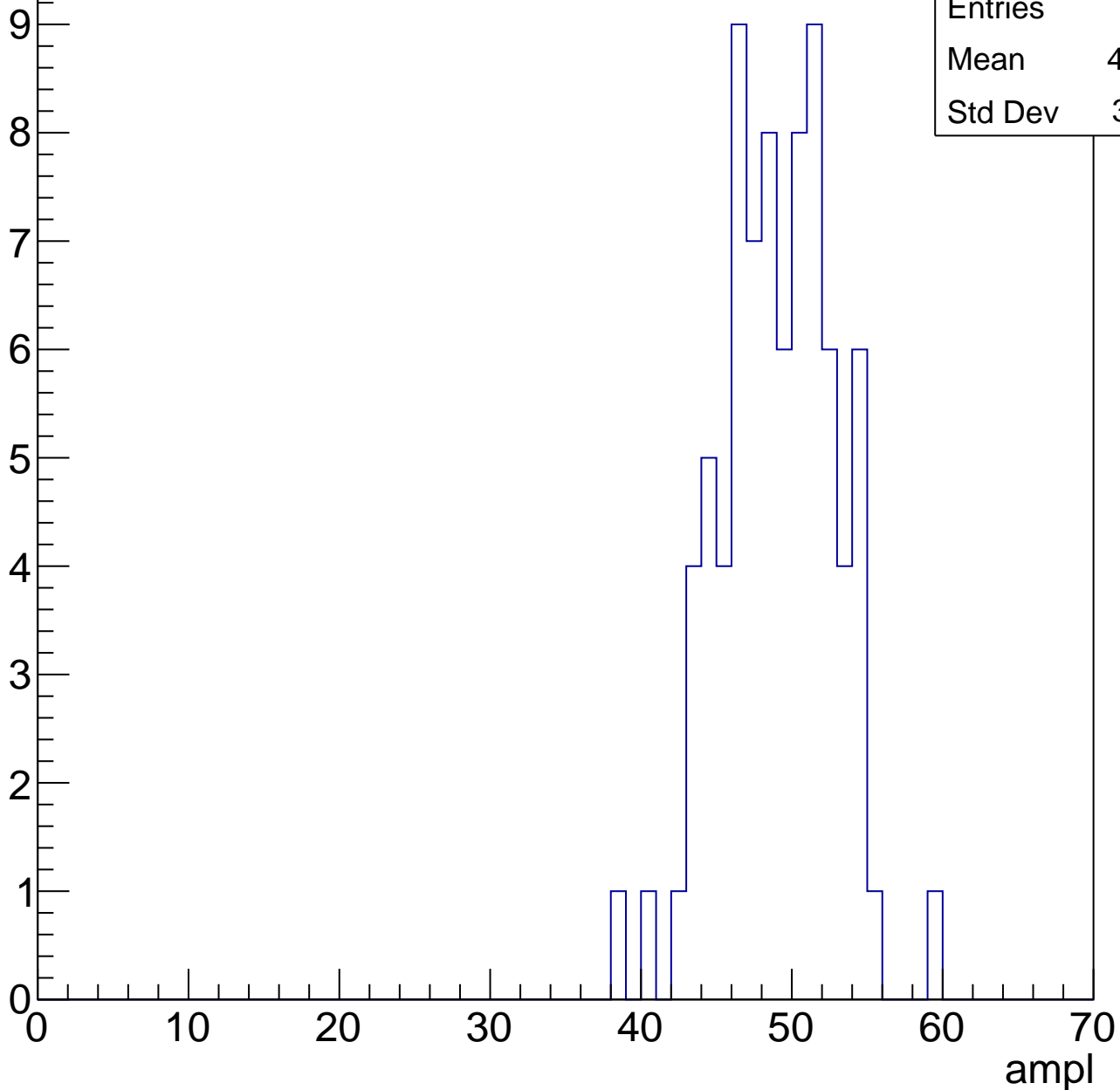


# B1L102S, U20-ch116, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	81
Mean	48.57
Std Dev	3.741

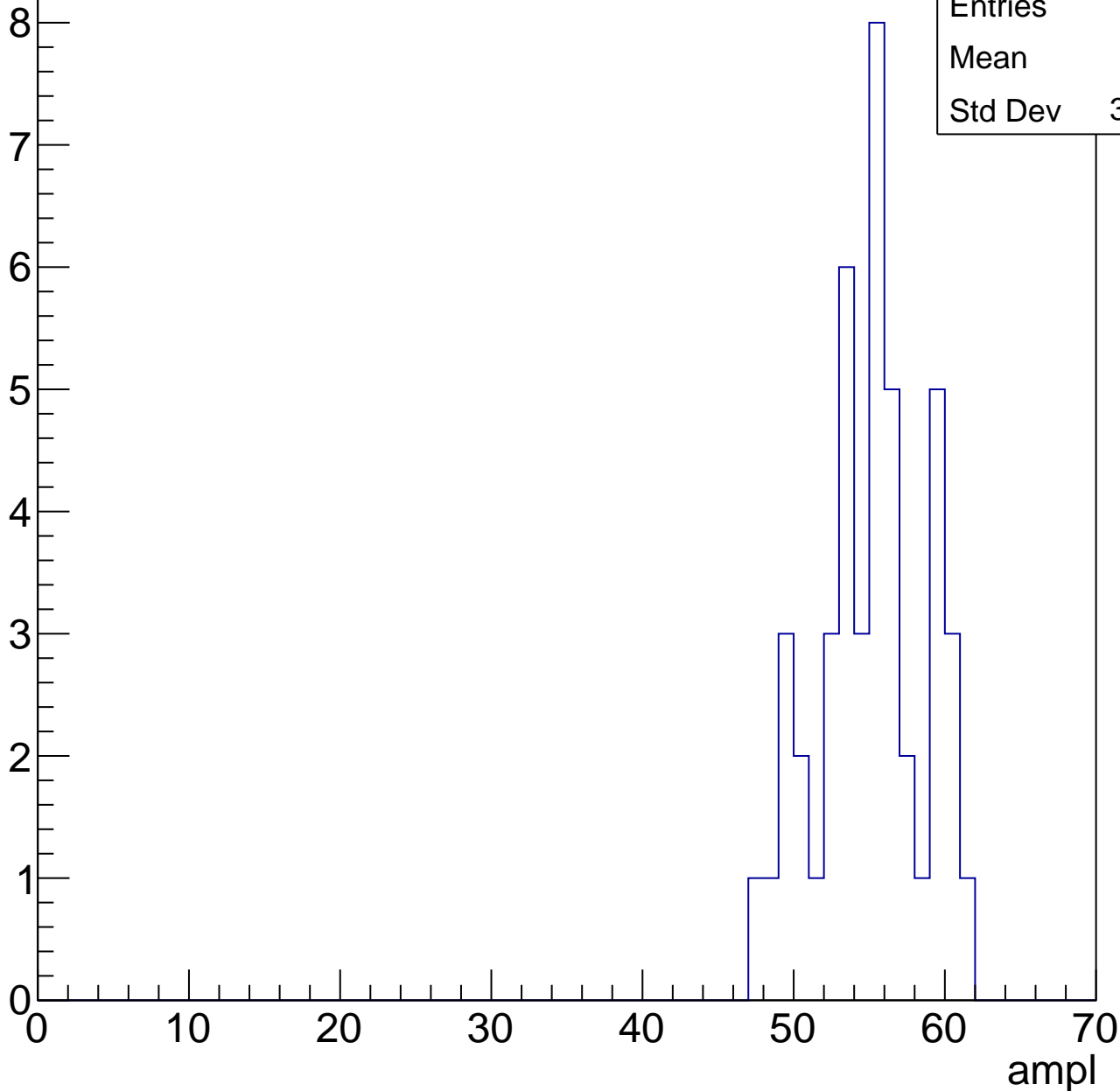


# B1L102S, U20-ch116, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

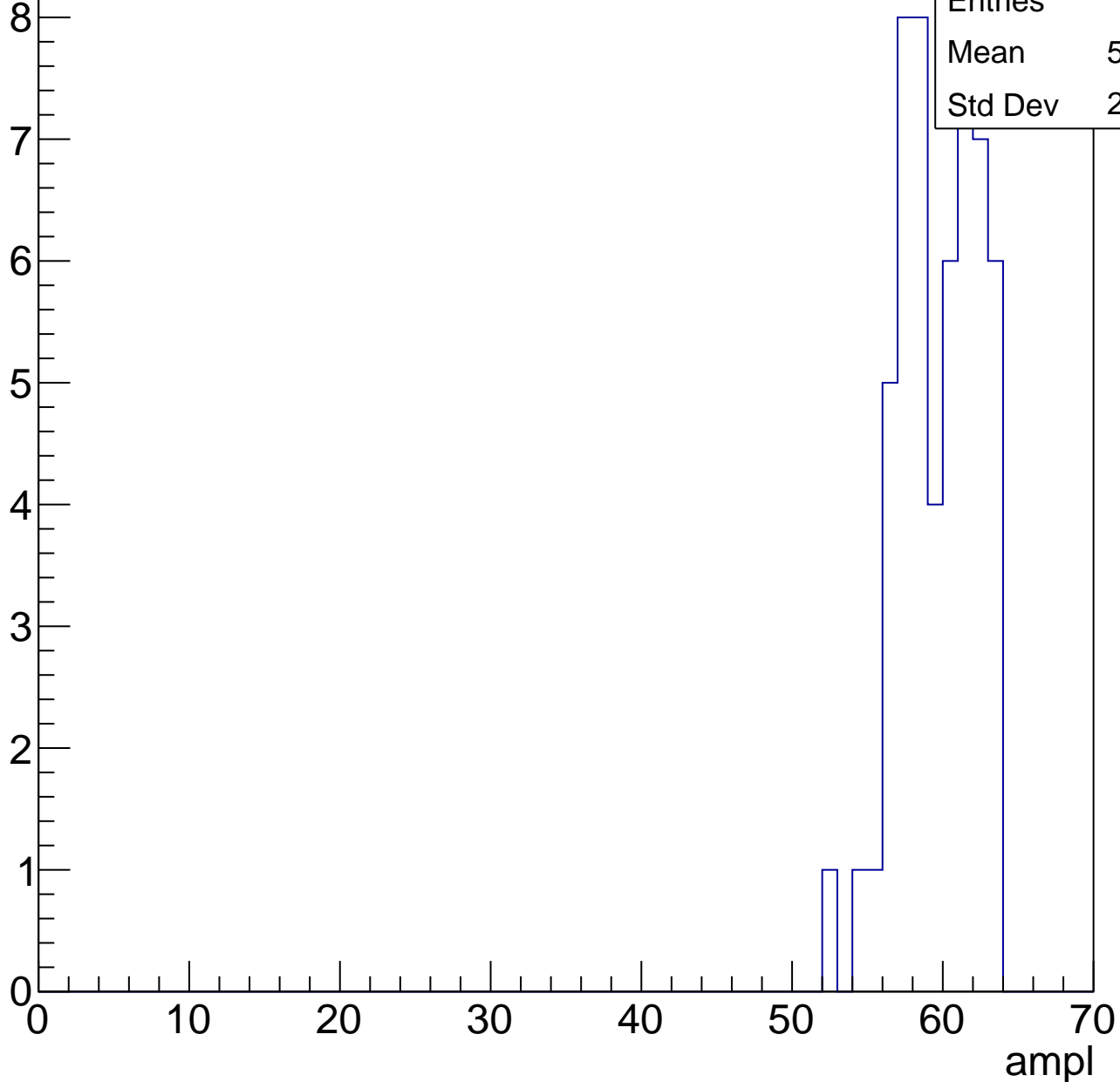
Entries	45
Mean	54.6
Std Dev	3.486



# B1L102S, U20-ch116, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

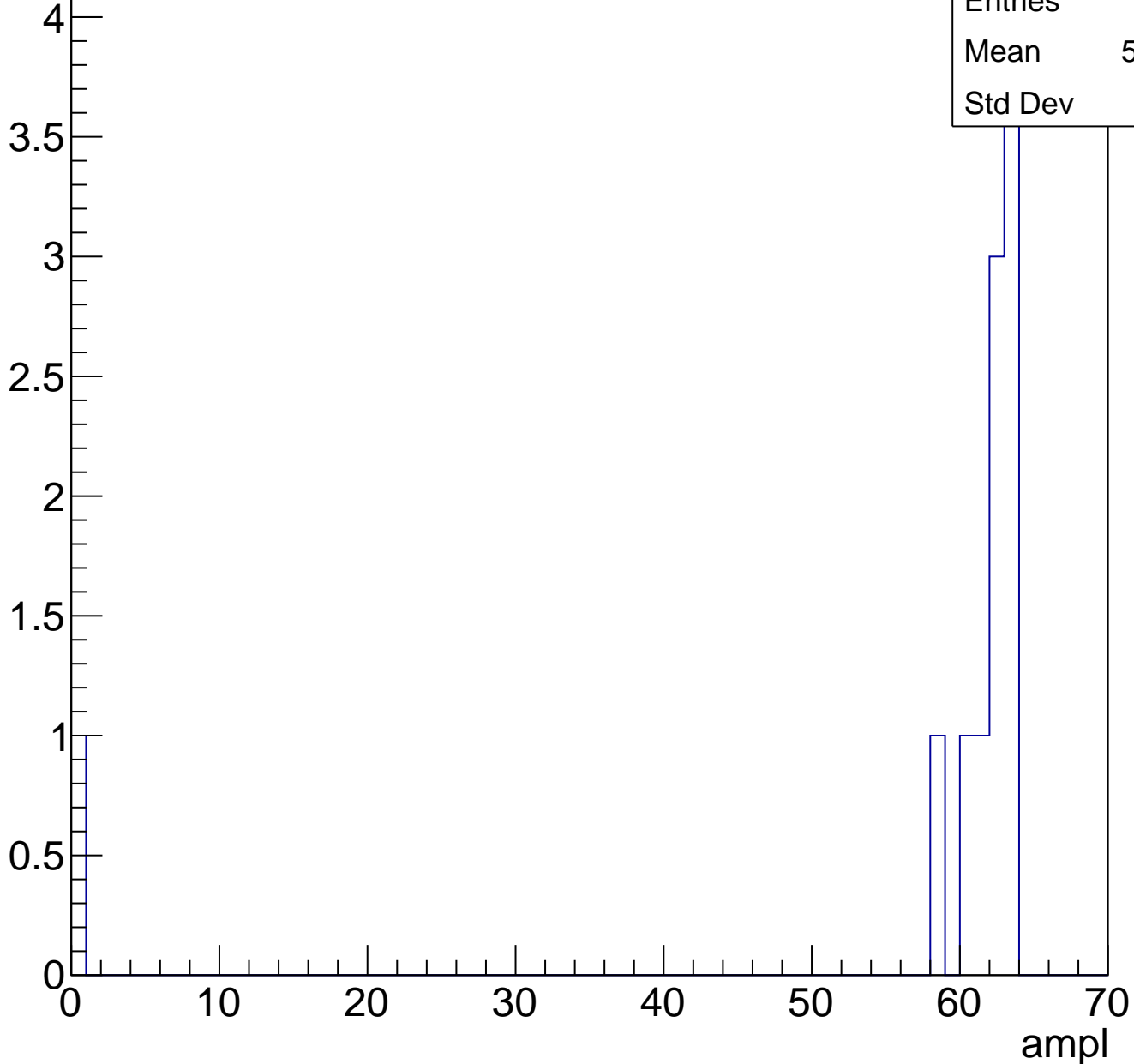
Entry



# B1L102S, U20-ch116, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U20-ch116, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch117, adc0

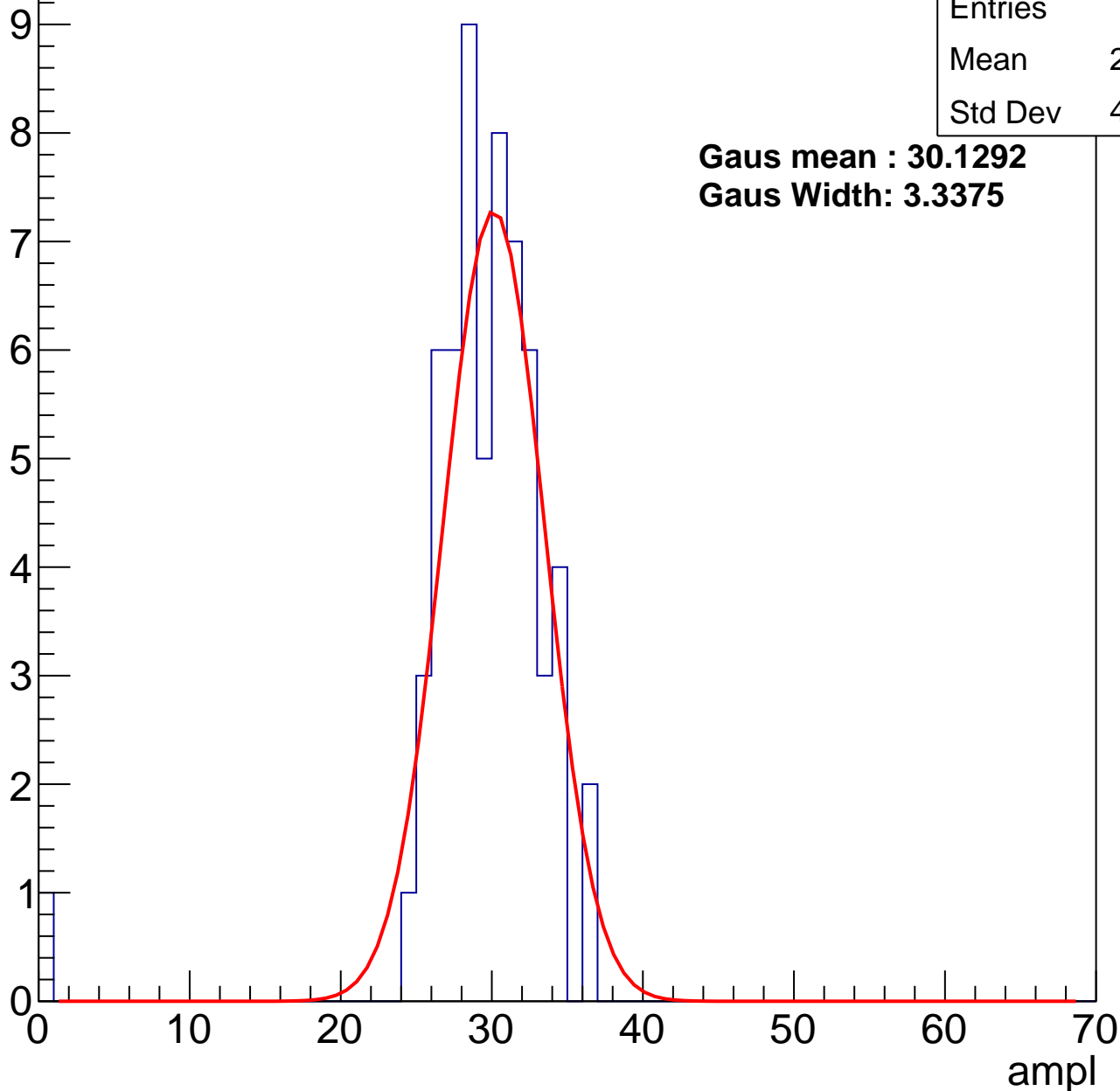
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	29.02
Std Dev	4.682

**Gaus mean : 30.1292**

**Gaus Width: 3.3375**



# B1L102S, U20-ch117, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	35.77
Std Dev	3.171

**Gaus mean : 36.3371**

**Gaus Width: 3.3741**

10

8

6

4

2

0

0

10

20

30

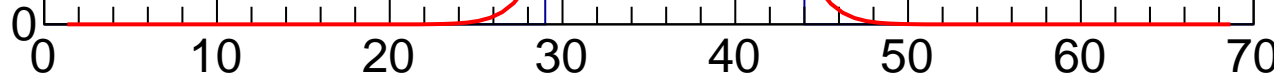
40

50

60

70

ampl



# B1L102S, U20-ch117, adc2

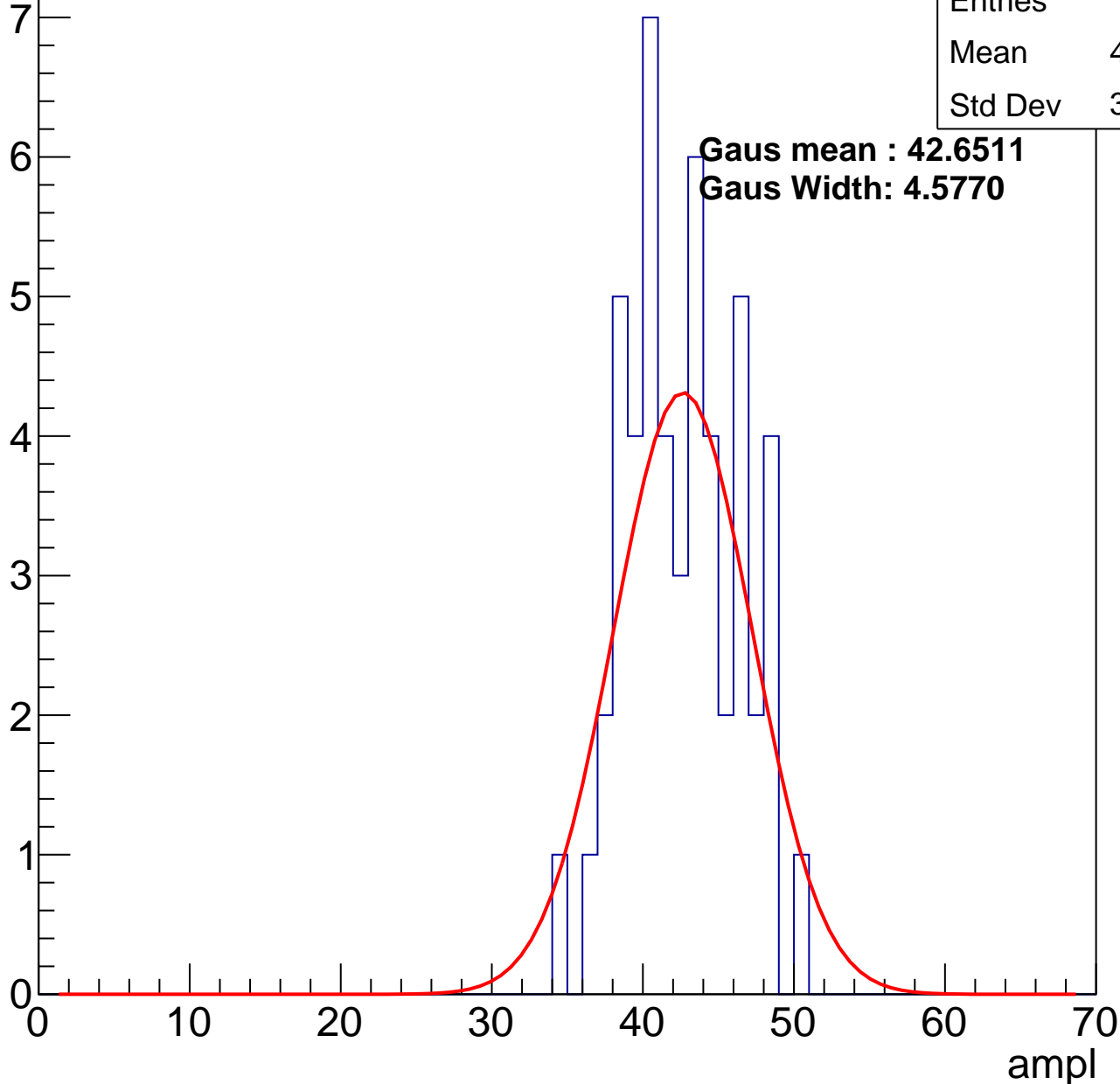
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	42.16
Std Dev	3.637

**Gaus mean : 42.6511**

**Gaus Width: 4.5770**

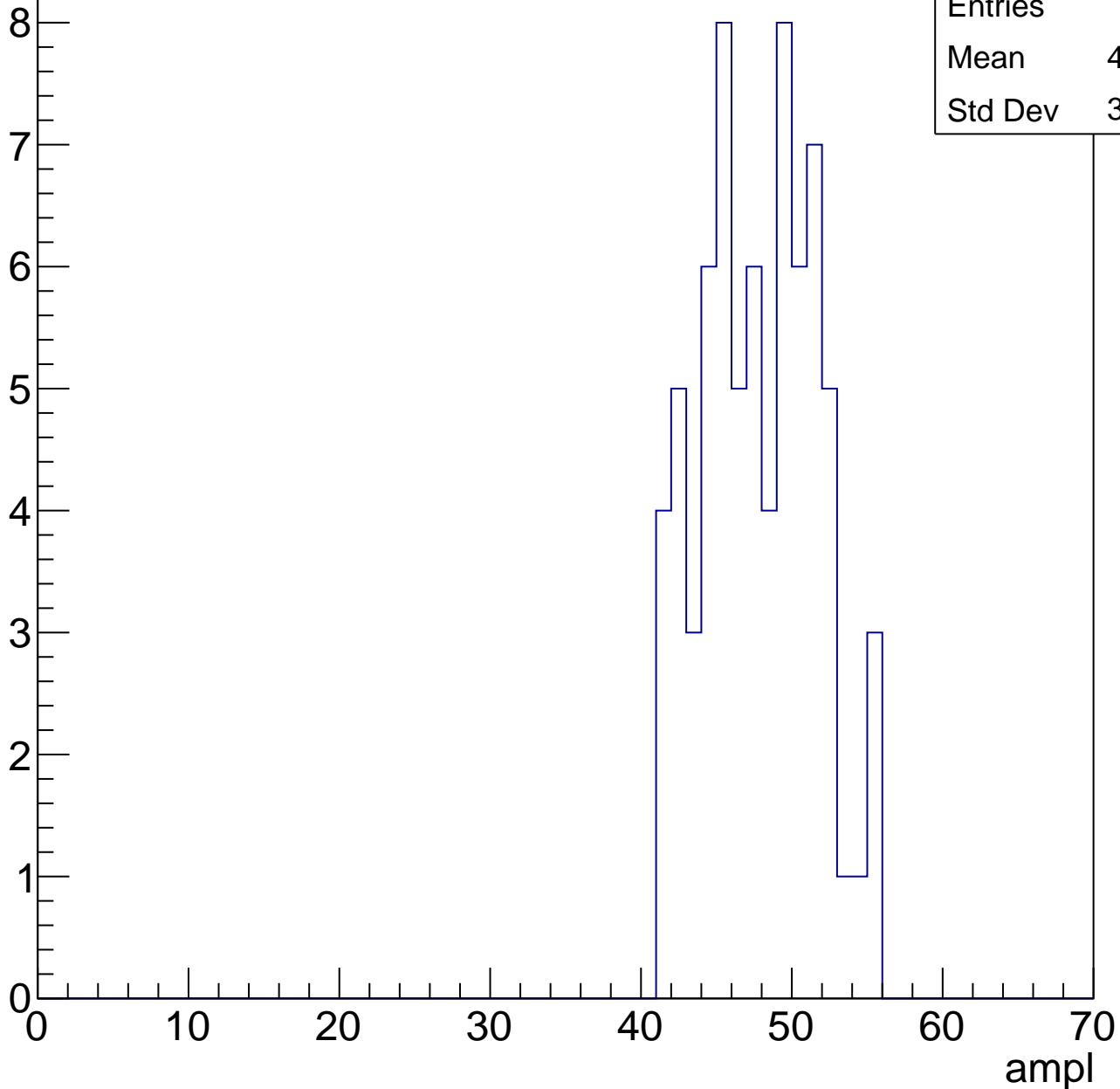


# B1L102S, U20-ch117, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

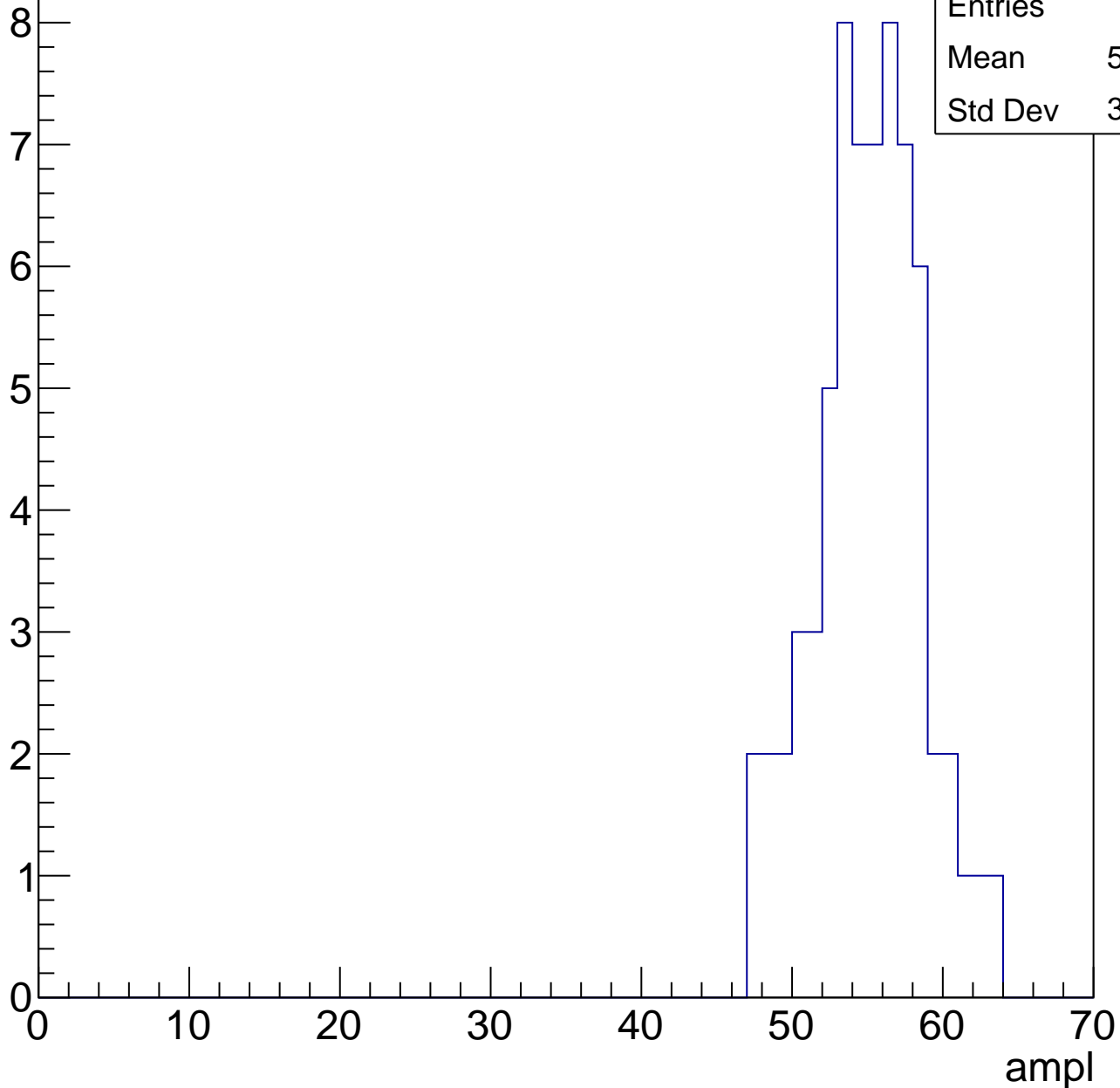
Entries	72
Mean	47.39
Std Dev	3.729



# B1L102S, U20-ch117, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

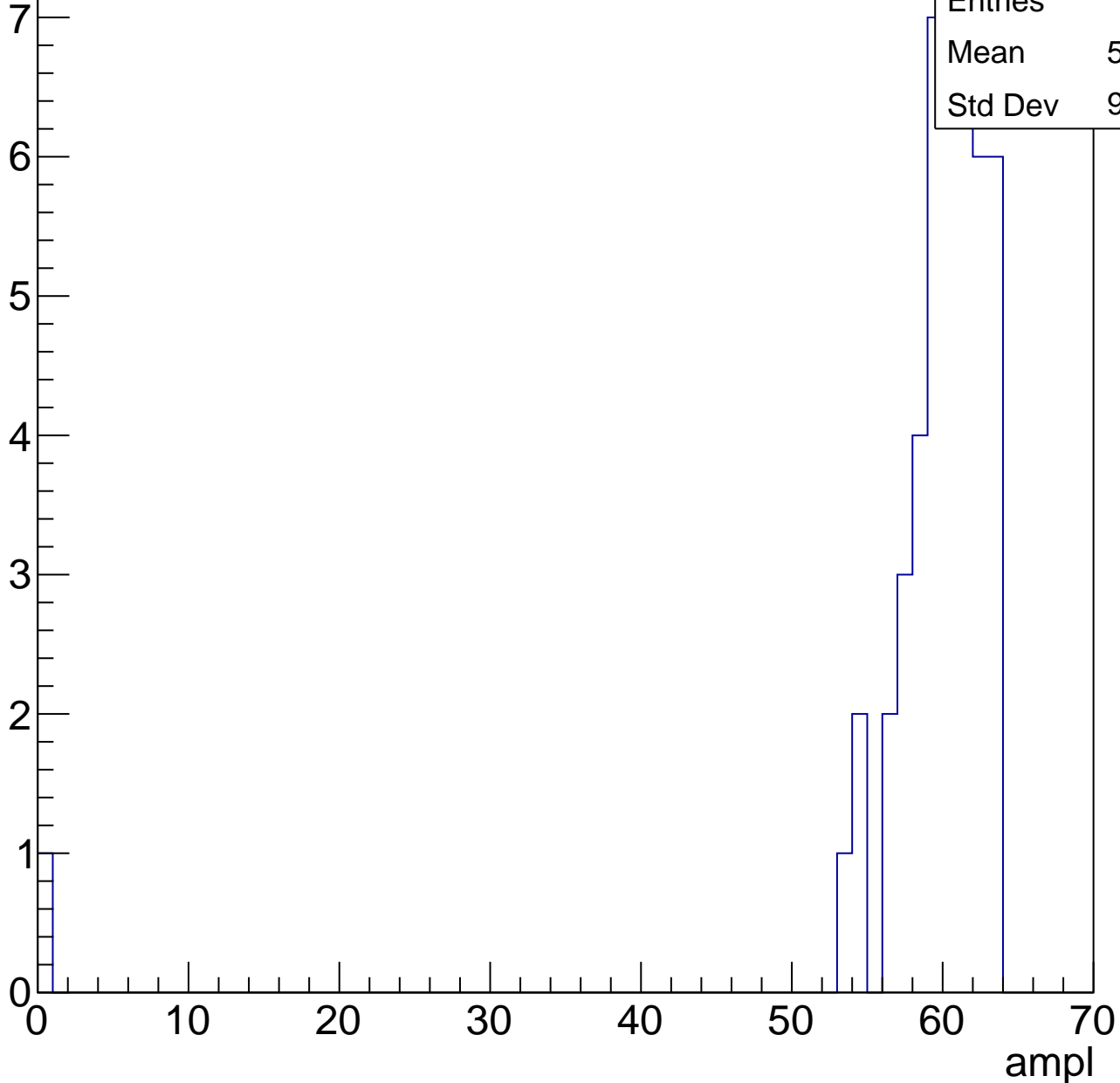


# B1L102S, U20-ch117, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

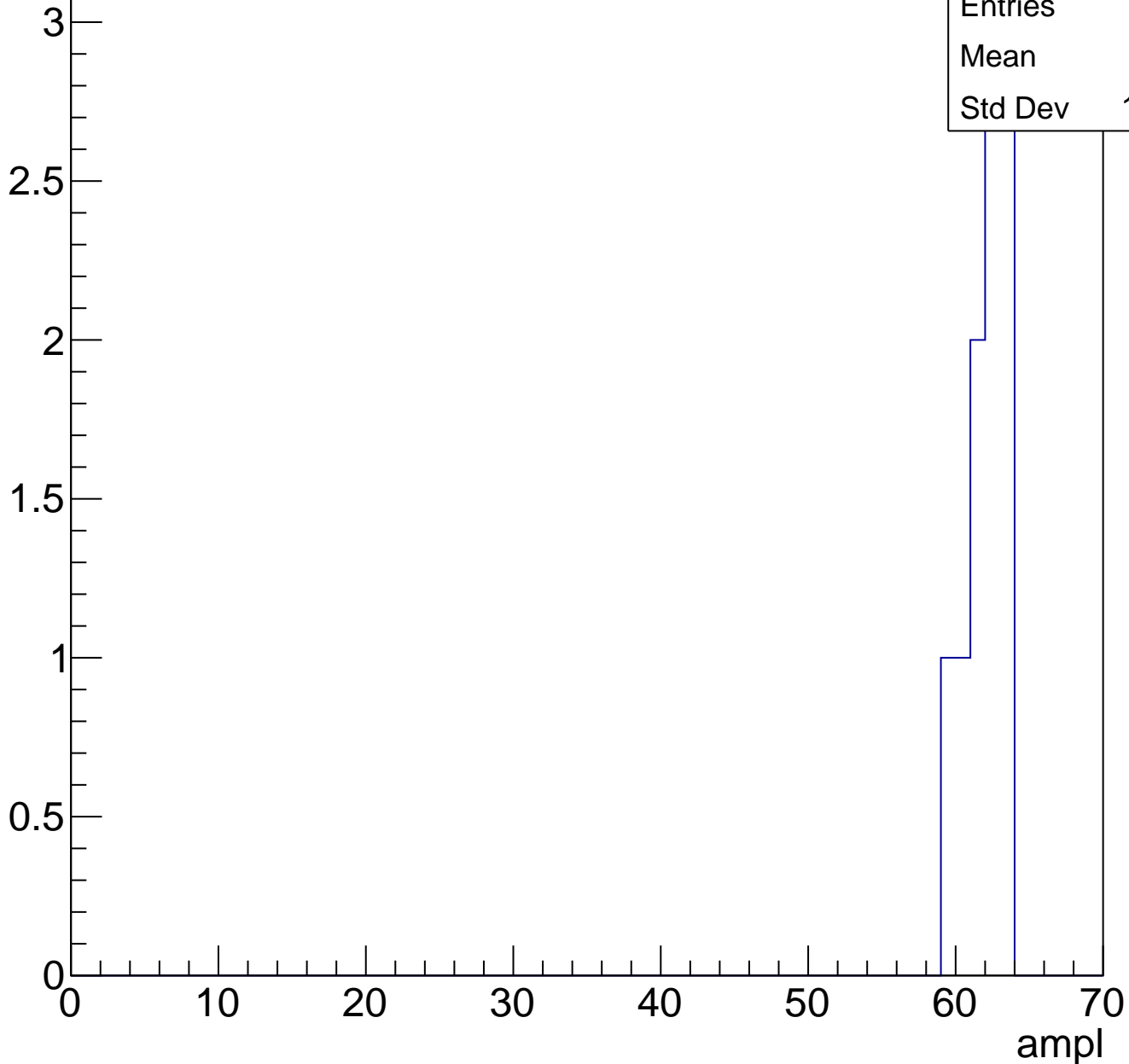
Entries	46
Mean	58.39
Std Dev	9.052



# B1L102S, U20-ch117, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	10
Mean	61.6
Std Dev	1.281



# B1L102S, U20-ch117, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U20-ch118, adc0

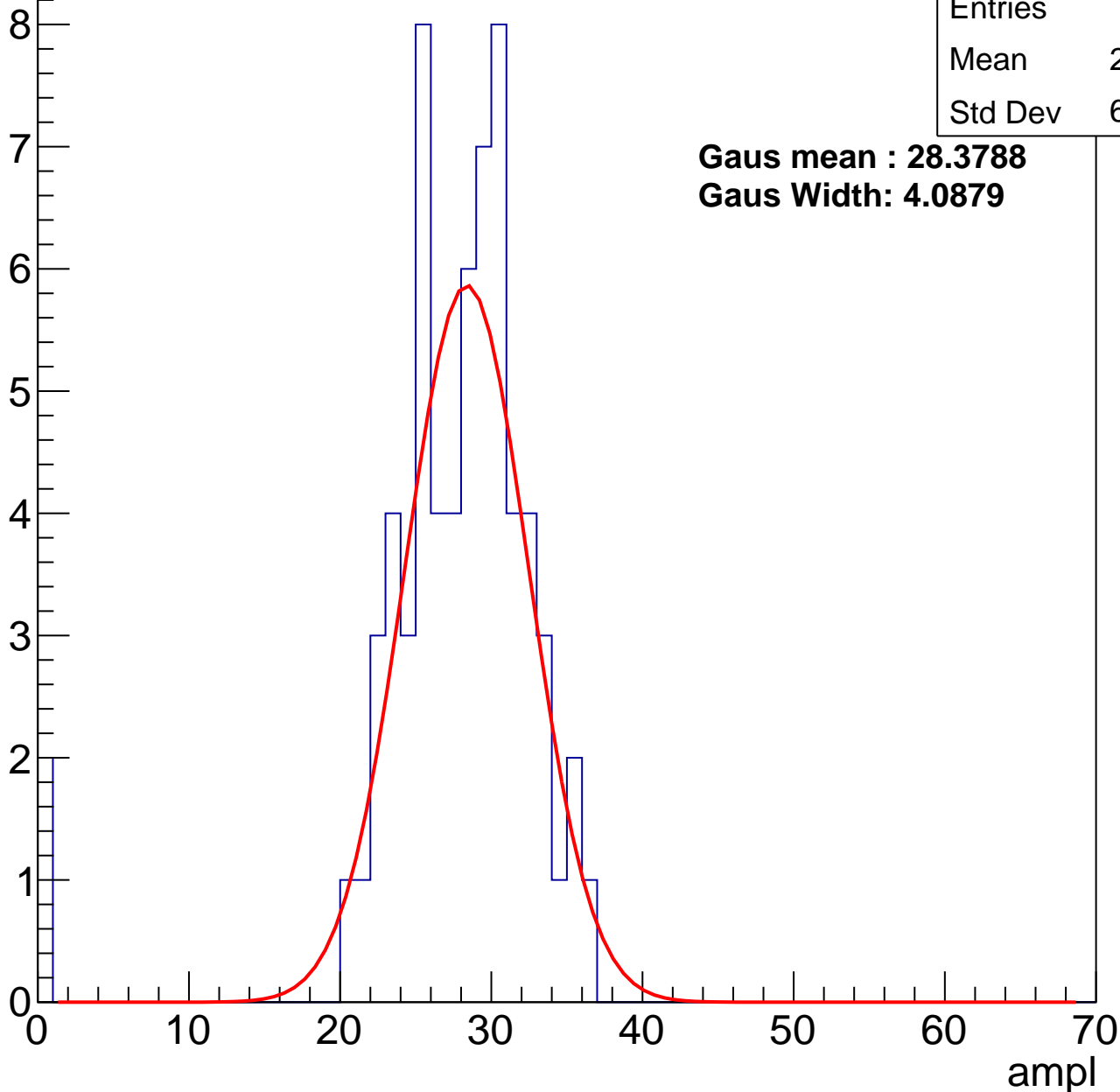
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	27.05
Std Dev	6.006

**Gaus mean : 28.3788**

**Gaus Width: 4.0879**



# B1L102S, U20-ch118, adc1

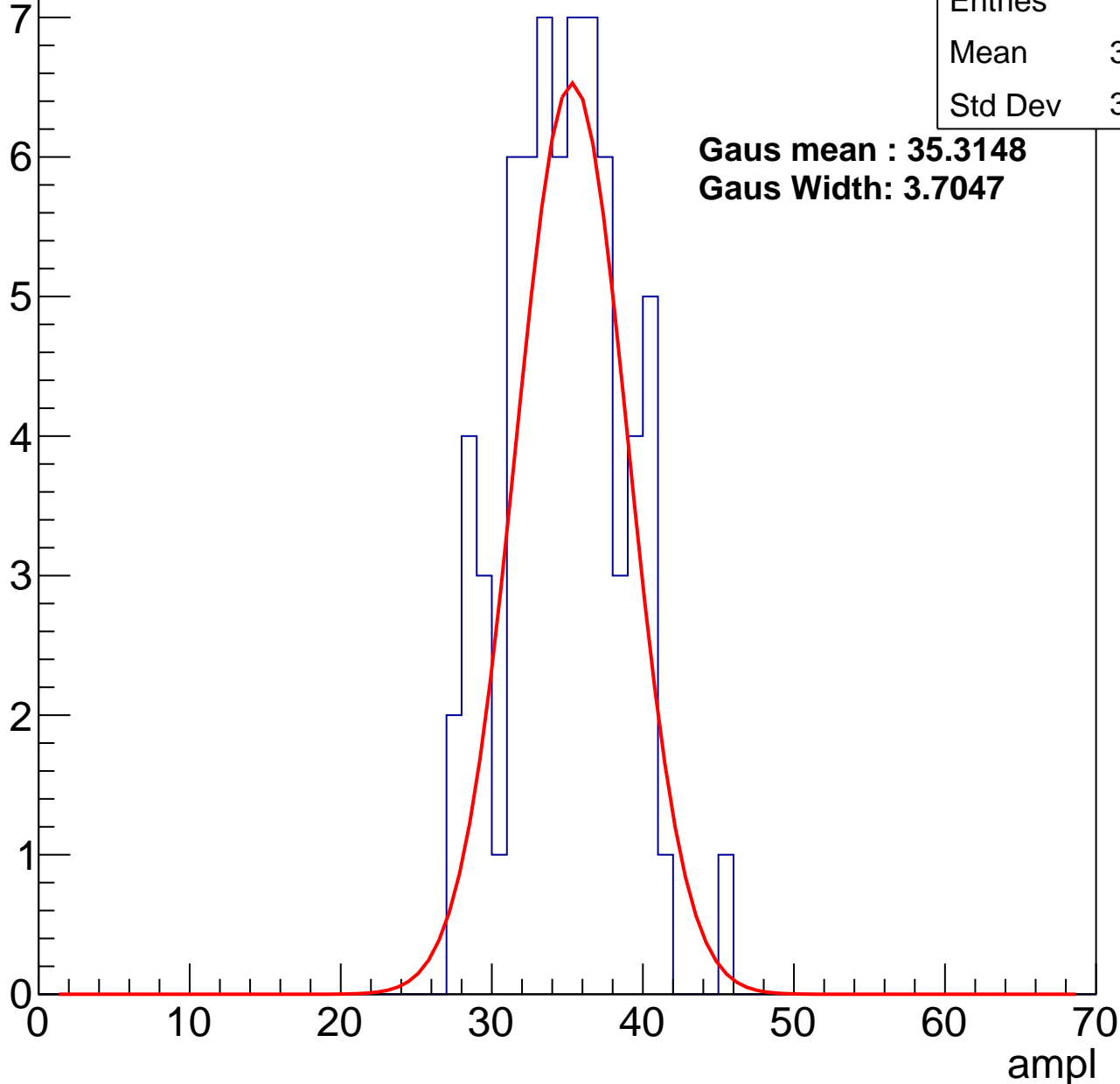
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	34.36
Std Dev	3.799

**Gaus mean : 35.3148**

**Gaus Width: 3.7047**



# B1L102S, U20-ch118, adc2

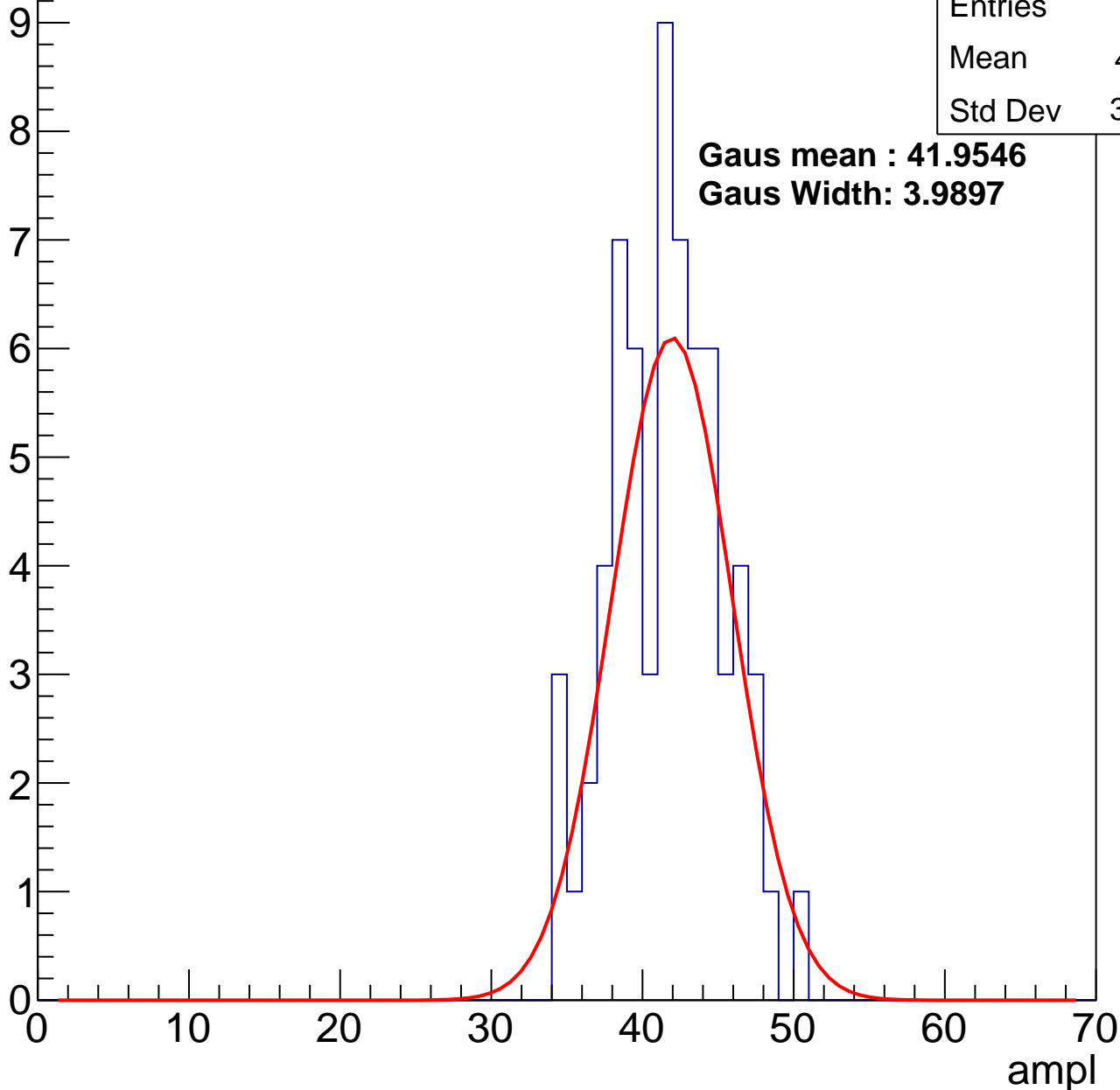
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	41.21
Std Dev	3.599

**Gaus mean : 41.9546**

**Gaus Width: 3.9897**

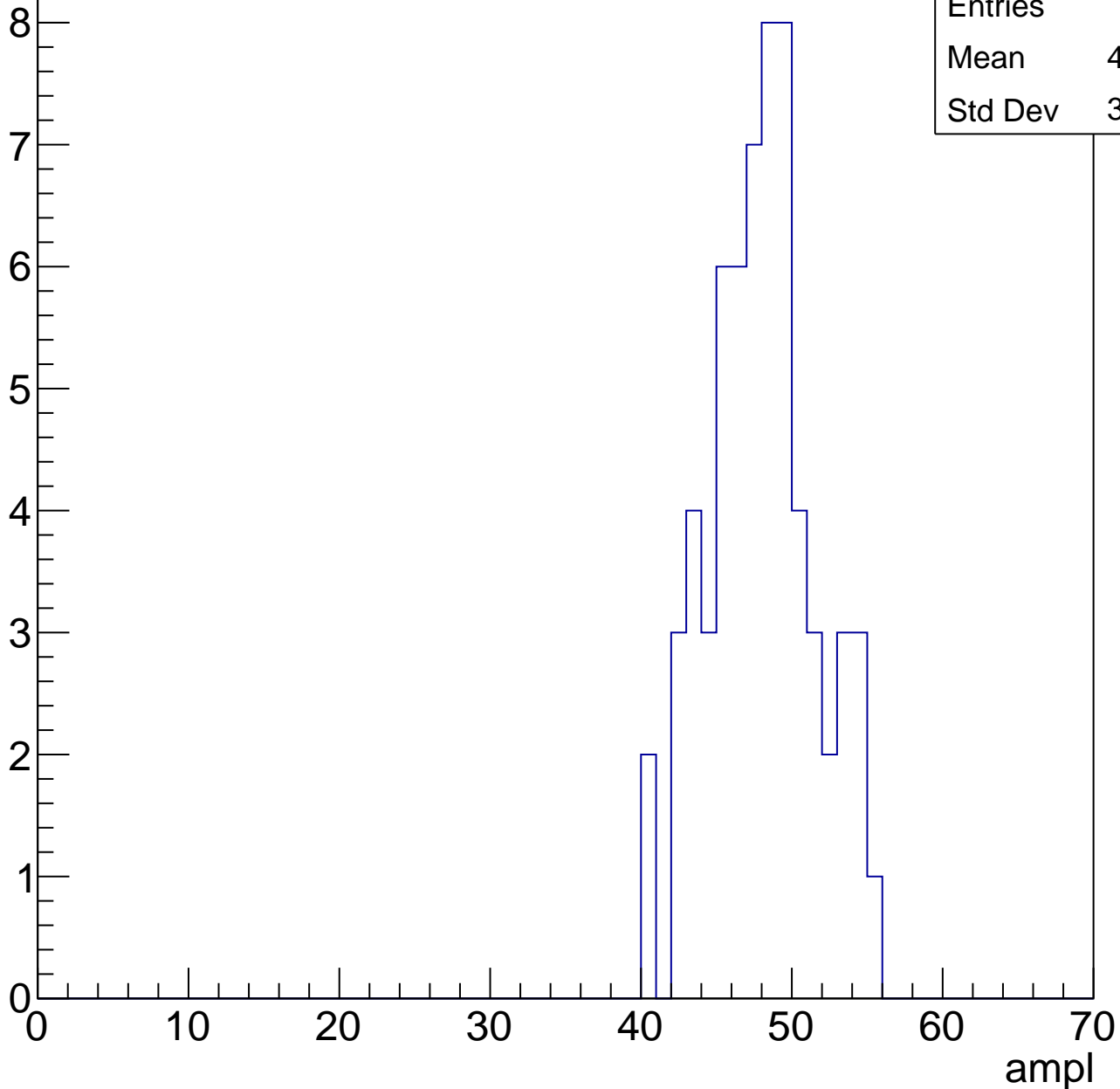


# B1L102S, U20-ch118, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	47.52
Std Dev	3.495

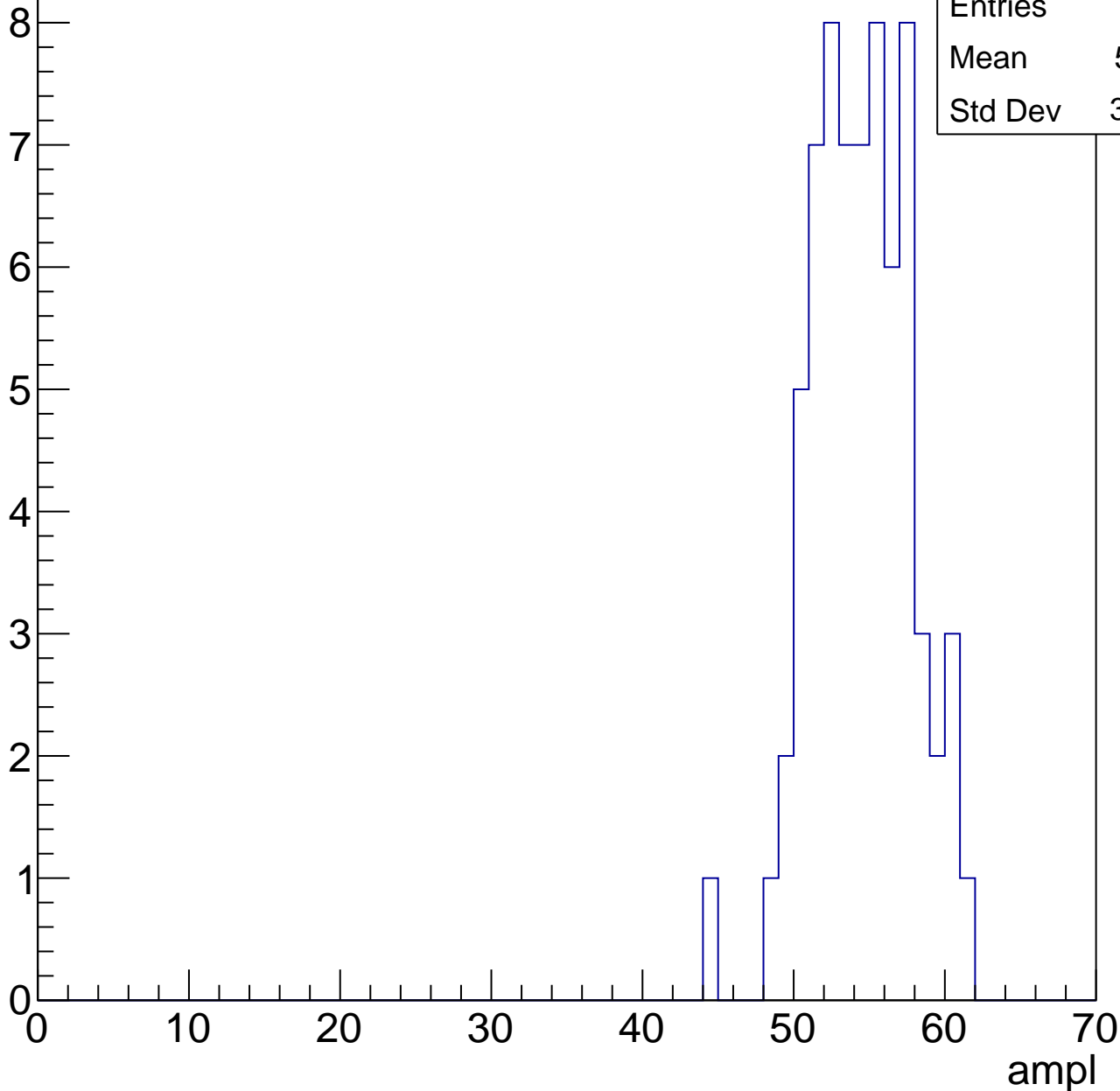


# B1L102S, U20-ch118, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

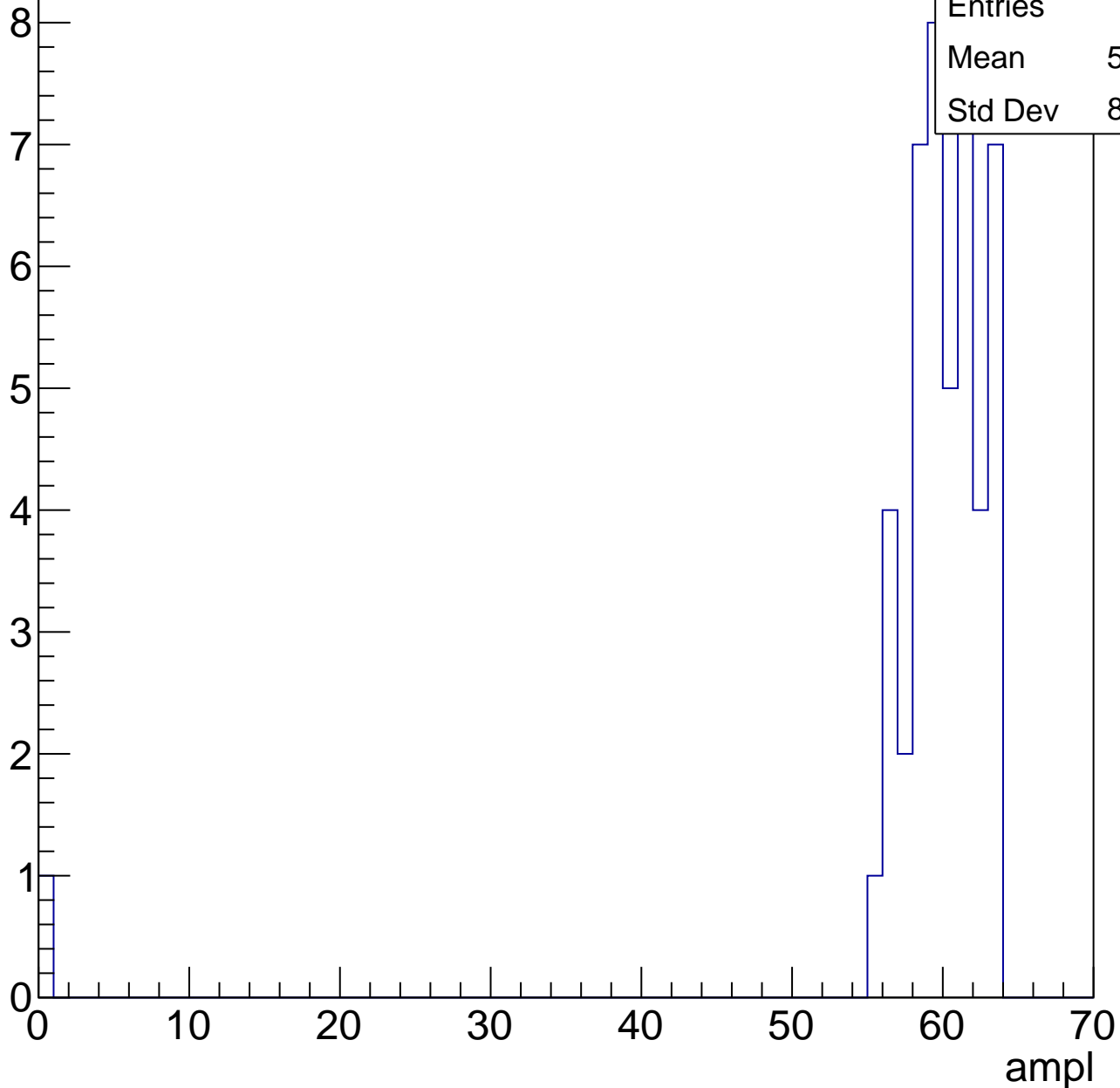
Entries	69
Mean	54.01
Std Dev	3.246



# B1L102S, U20-ch118, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

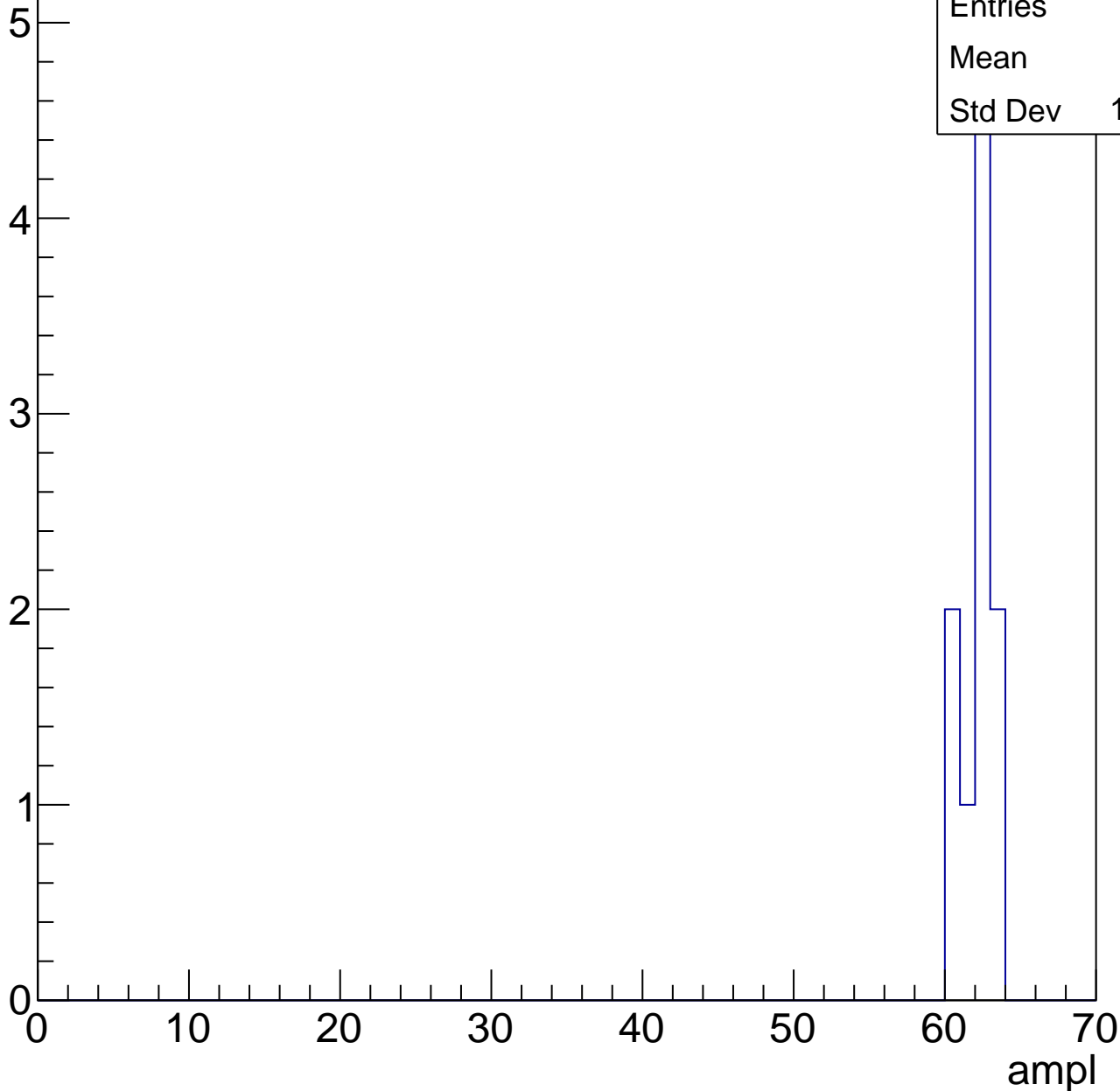


# B1L102S, U20-ch118, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	10
Mean	61.7
Std Dev	1.005





# B1L102S, U20-ch118, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch119, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	71
Mean	28.61
Std Dev	3.538

**Gaus mean : 28.9564**

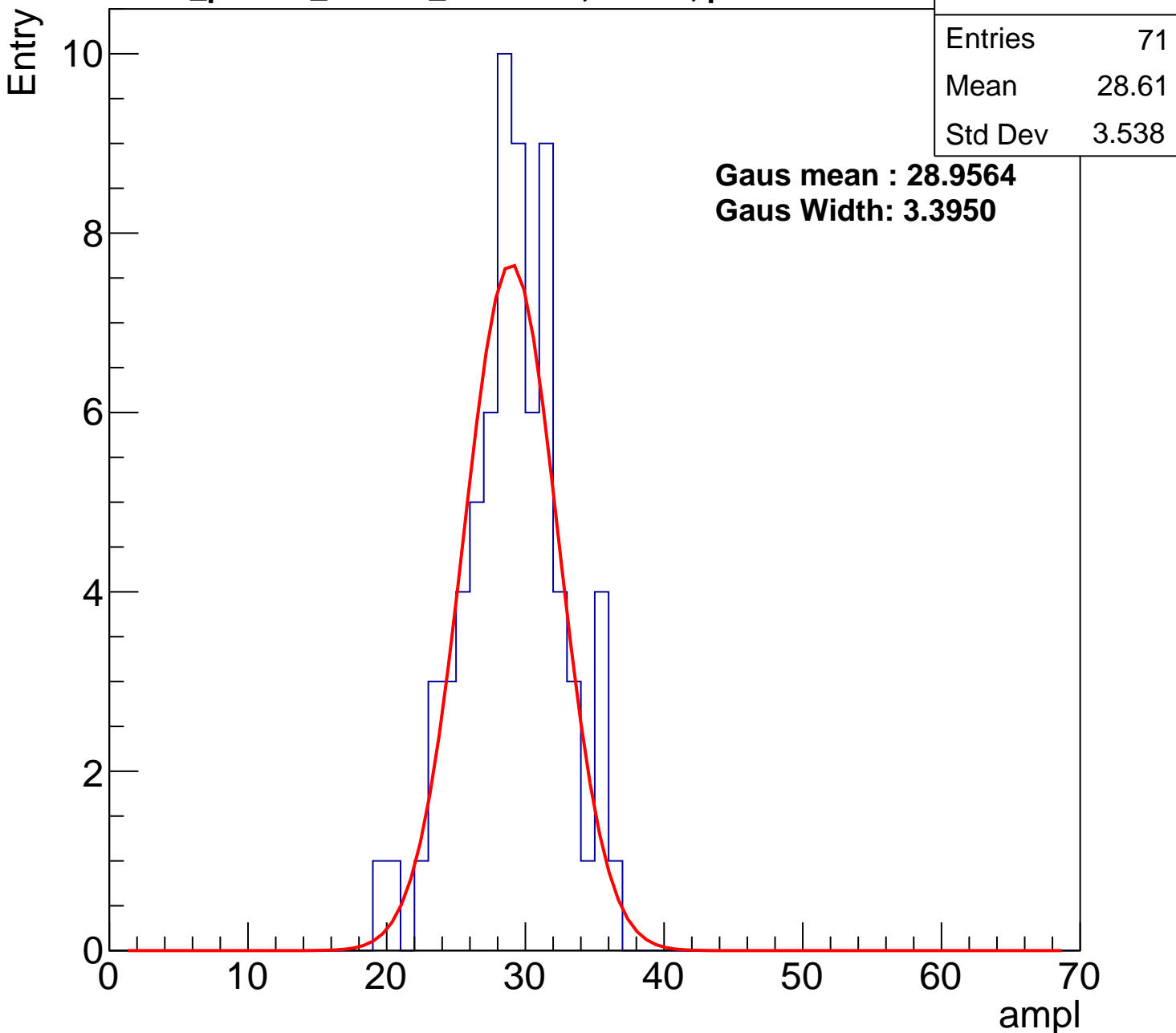
**Gaus Width: 3.3950**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U20-ch119, adc1

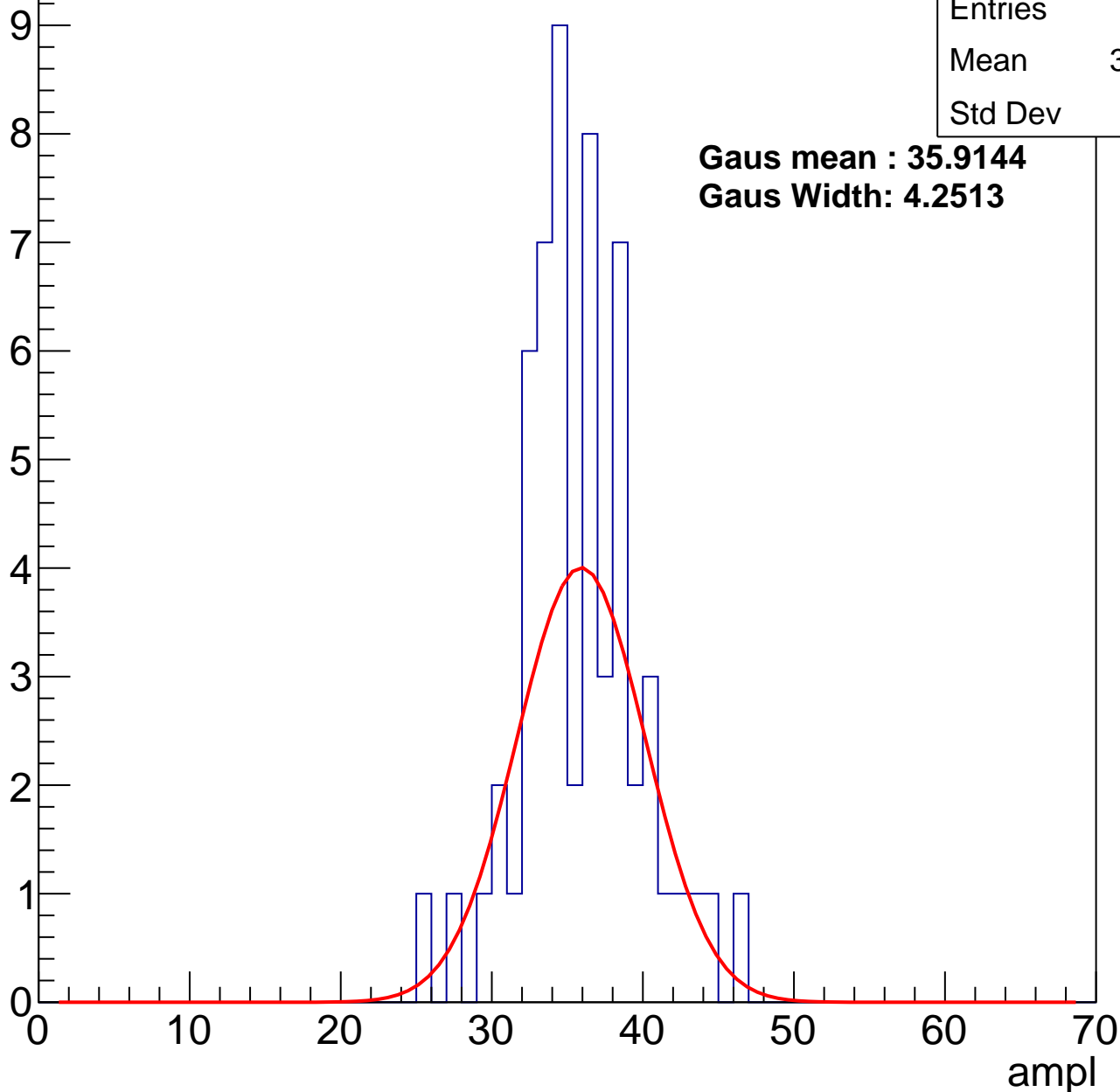
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	35.34
Std Dev	3.92

**Gaus mean : 35.9144**

**Gaus Width: 4.2513**



# B1L102S, U20-ch119, adc2

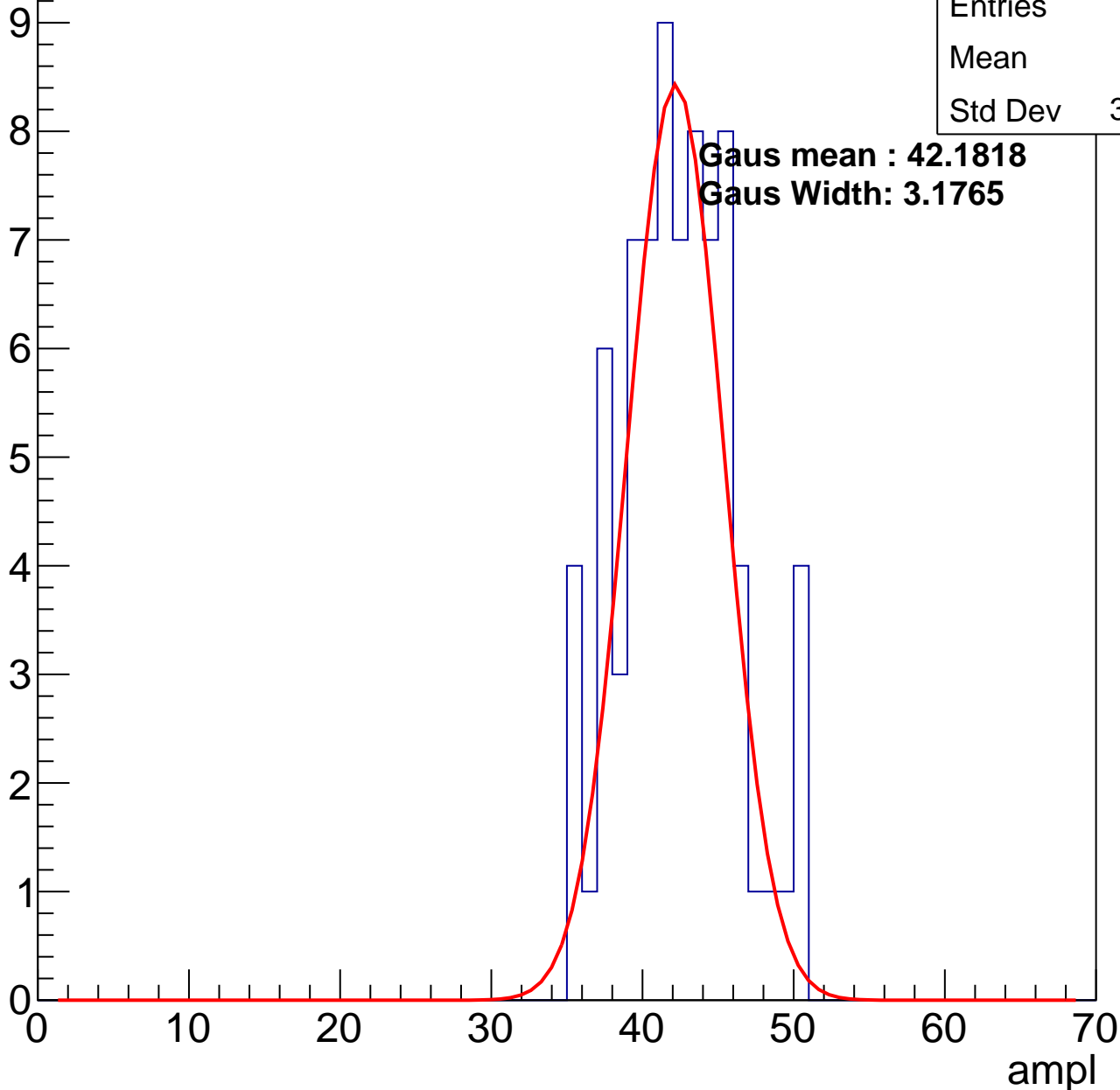
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	78
Mean	41.9
Std Dev	3.699

**Gaus mean : 42.1818**

**Gaus Width: 3.1765**

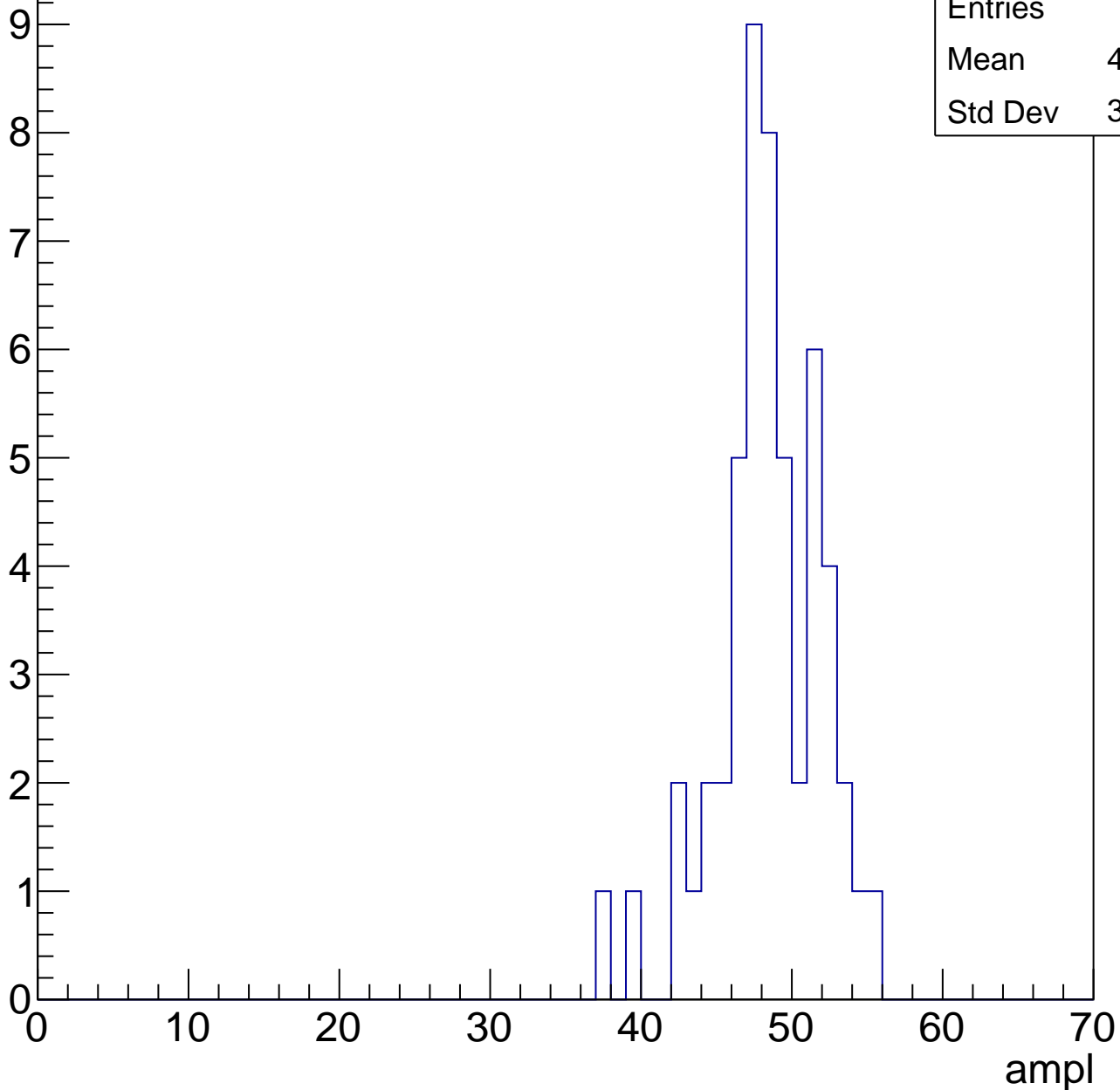


# B1L102S, U20-ch119, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	47.92
Std Dev	3.518

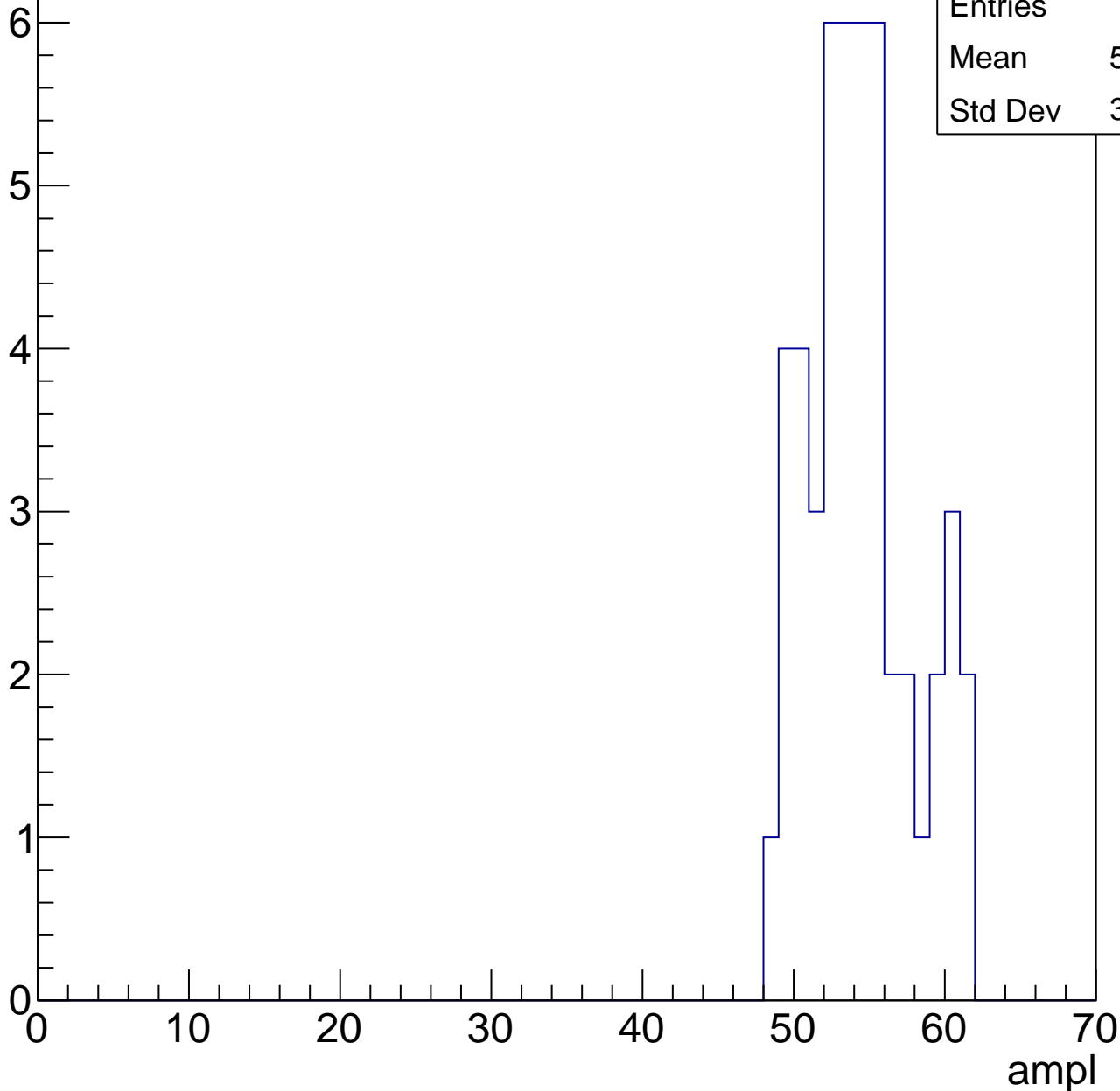


# B1L102S, U20-ch119, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	48
Mean	53.85
Std Dev	3.416

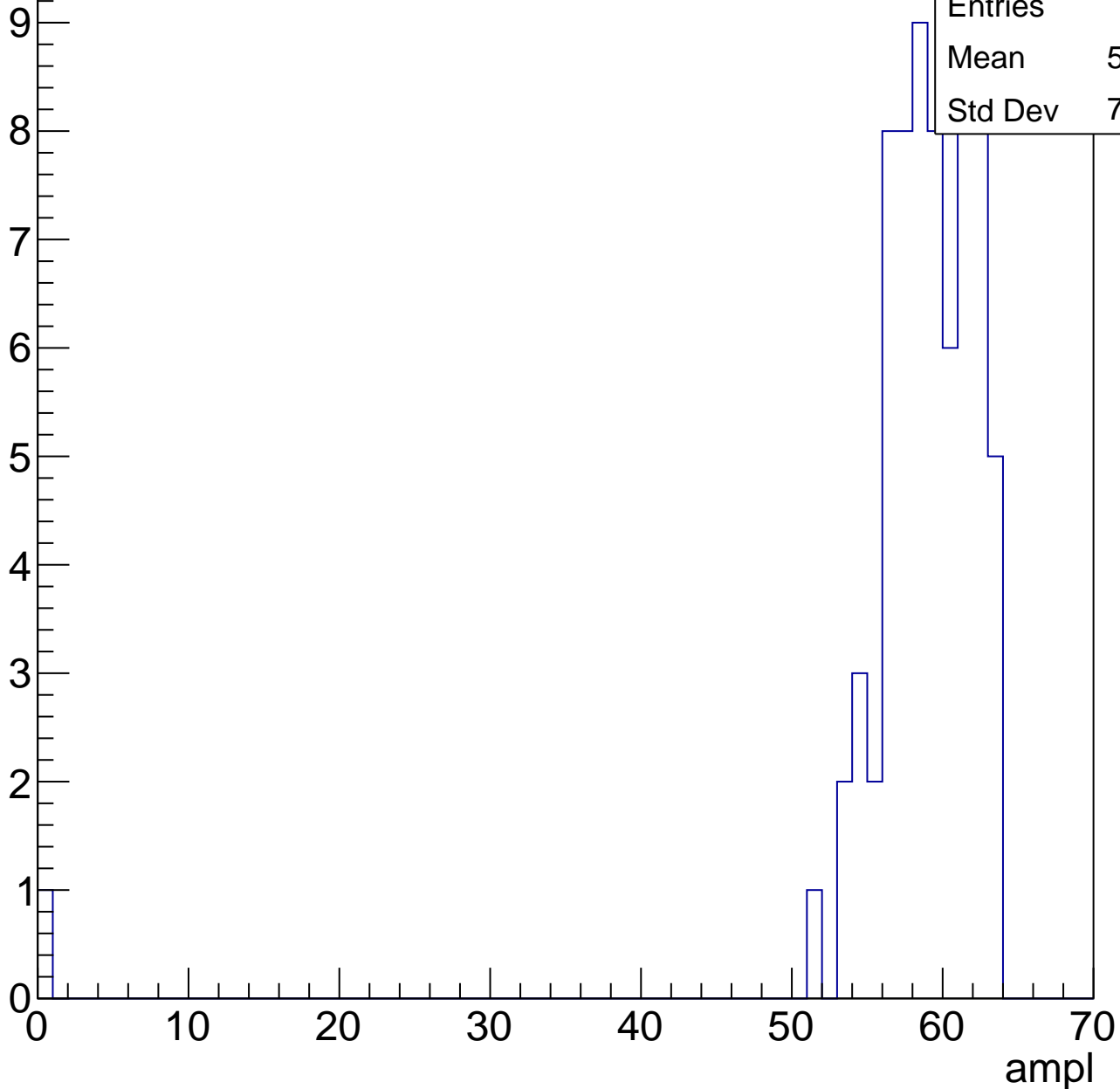


# B1L102S, U20-ch119, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	57.83
Std Dev	7.502

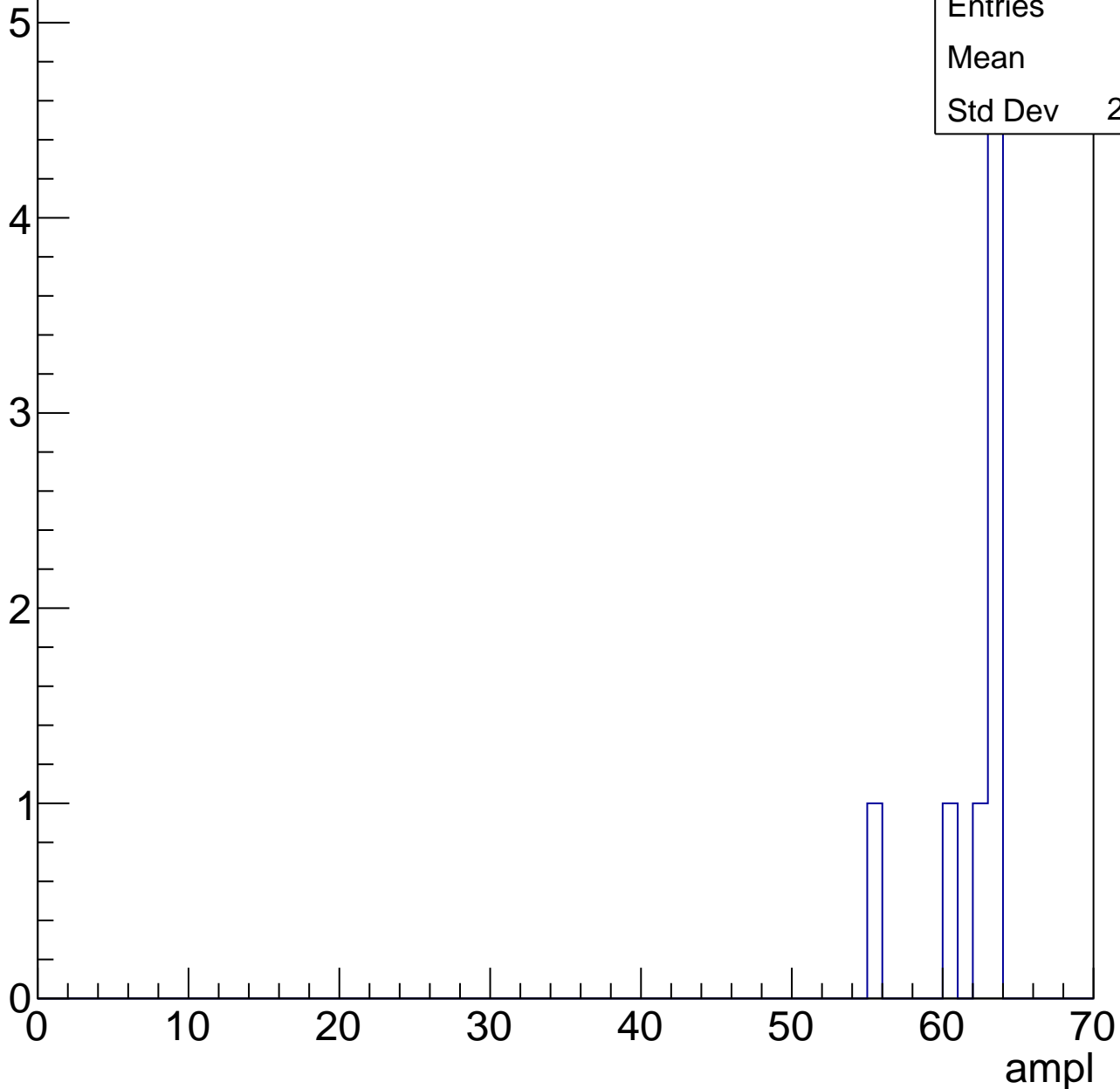


# B1L102S, U20-ch119, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	8
Mean	61.5
Std Dev	2.646





# B1L102S, U20-ch119, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L102S, U20-ch120, adc0

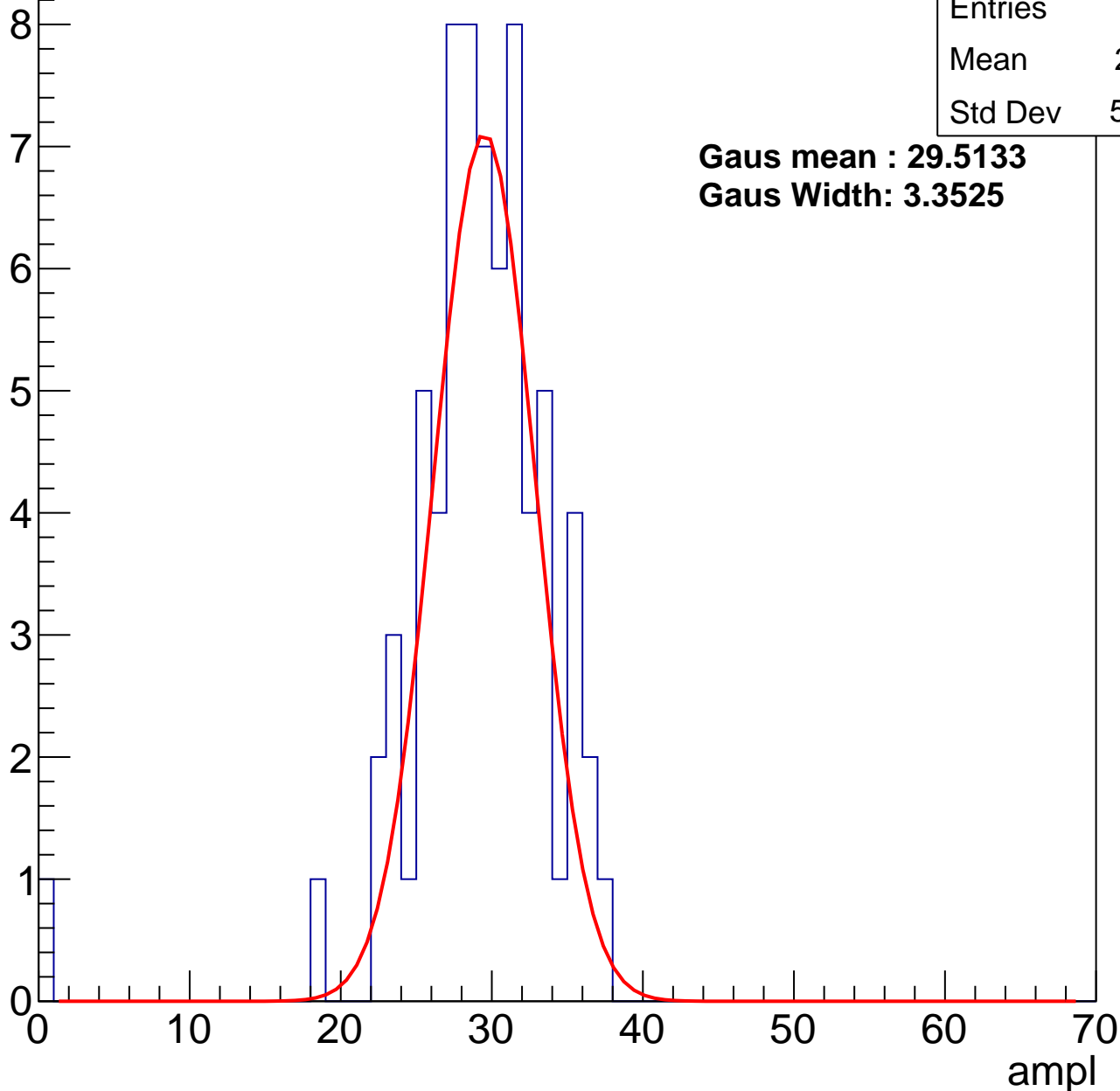
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	28.61
Std Dev	5.067

**Gaus mean : 29.5133**

**Gaus Width: 3.3525**



# B1L102S, U20-ch120, adc1

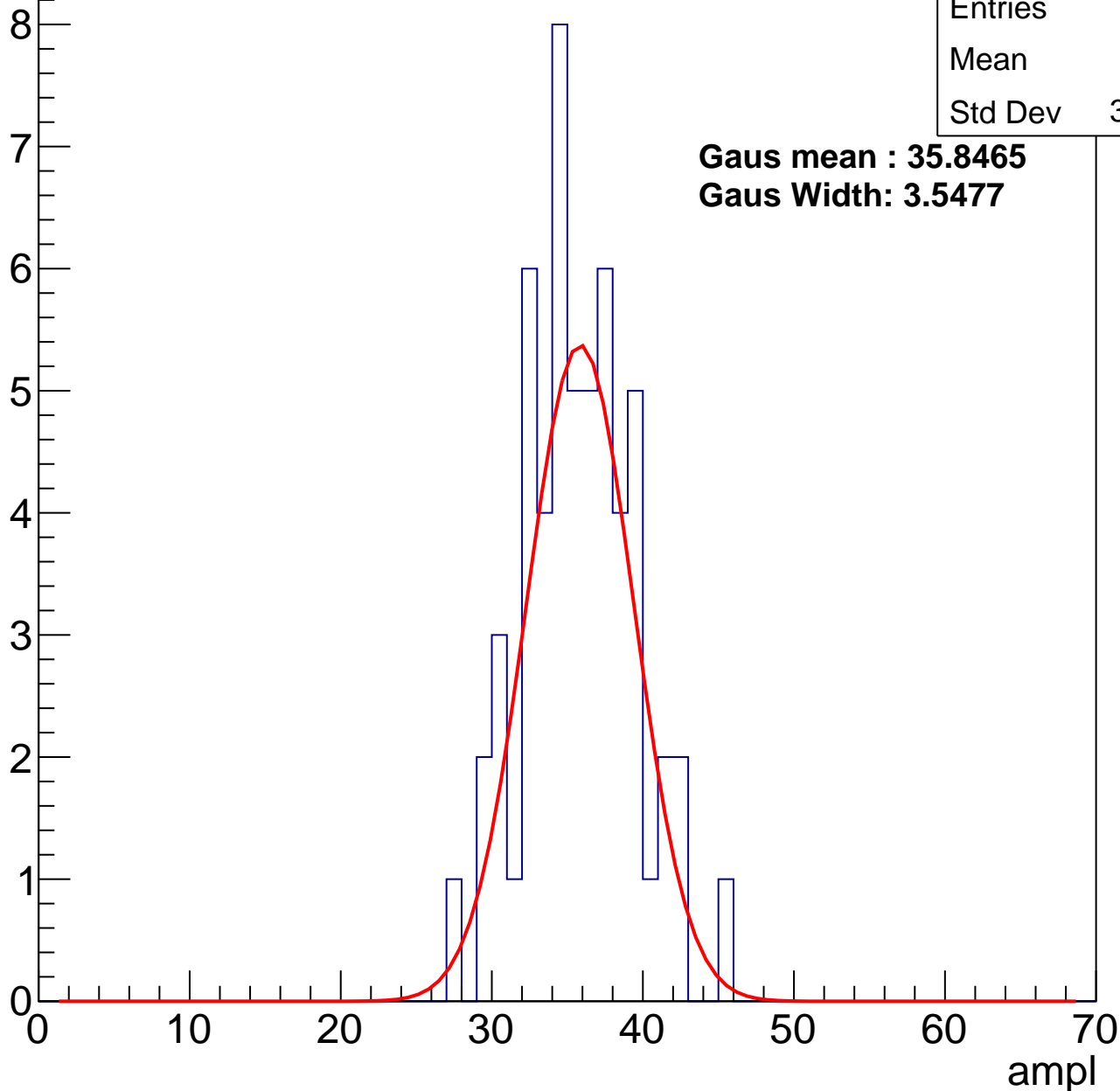
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	35.3
Std Dev	3.635

**Gaus mean : 35.8465**

**Gaus Width: 3.5477**



# B1L102S, U20-ch120, adc2

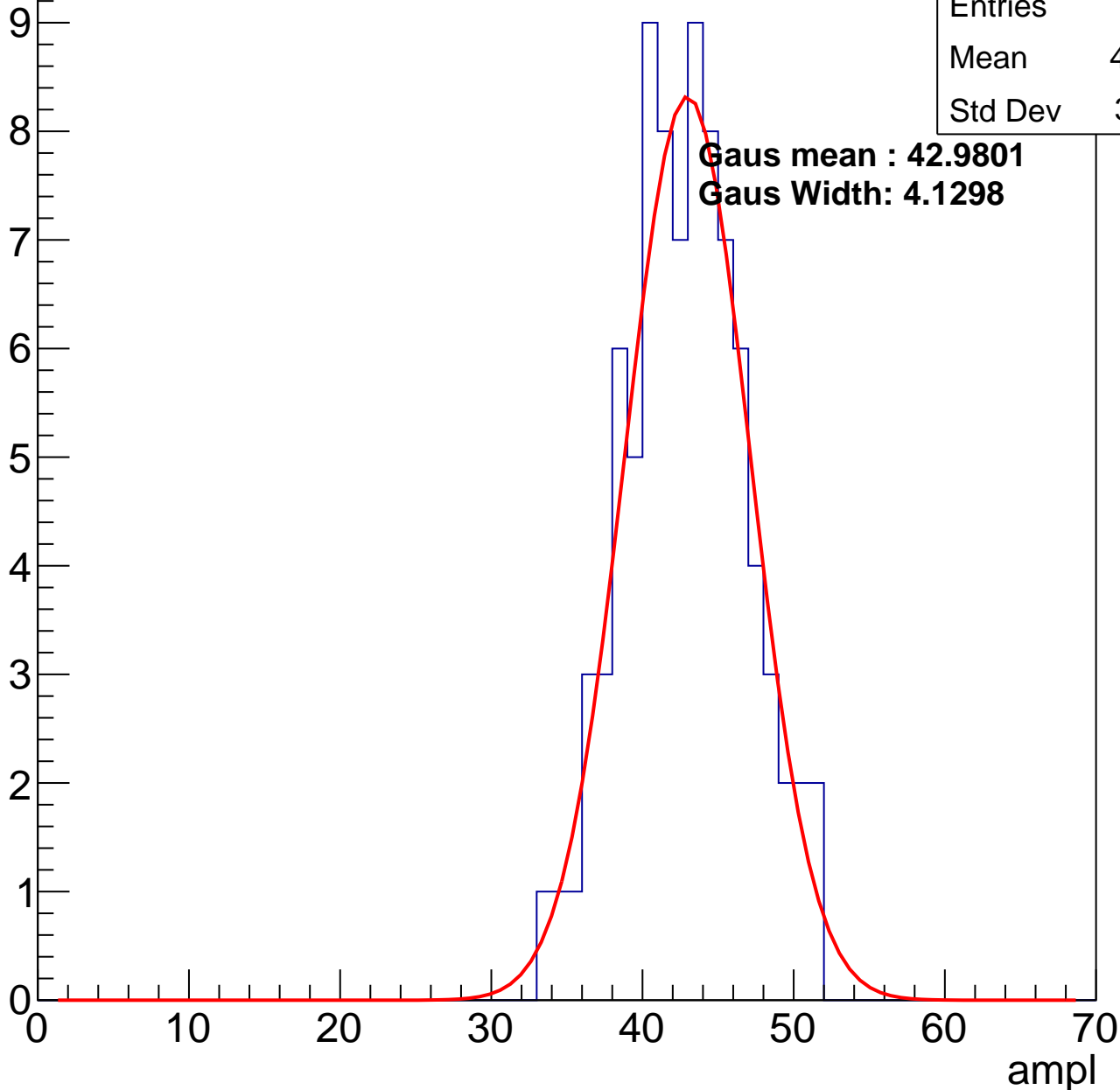
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	87
Mean	42.39
Std Dev	3.931

**Gaus mean : 42.9801**

**Gaus Width: 4.1298**

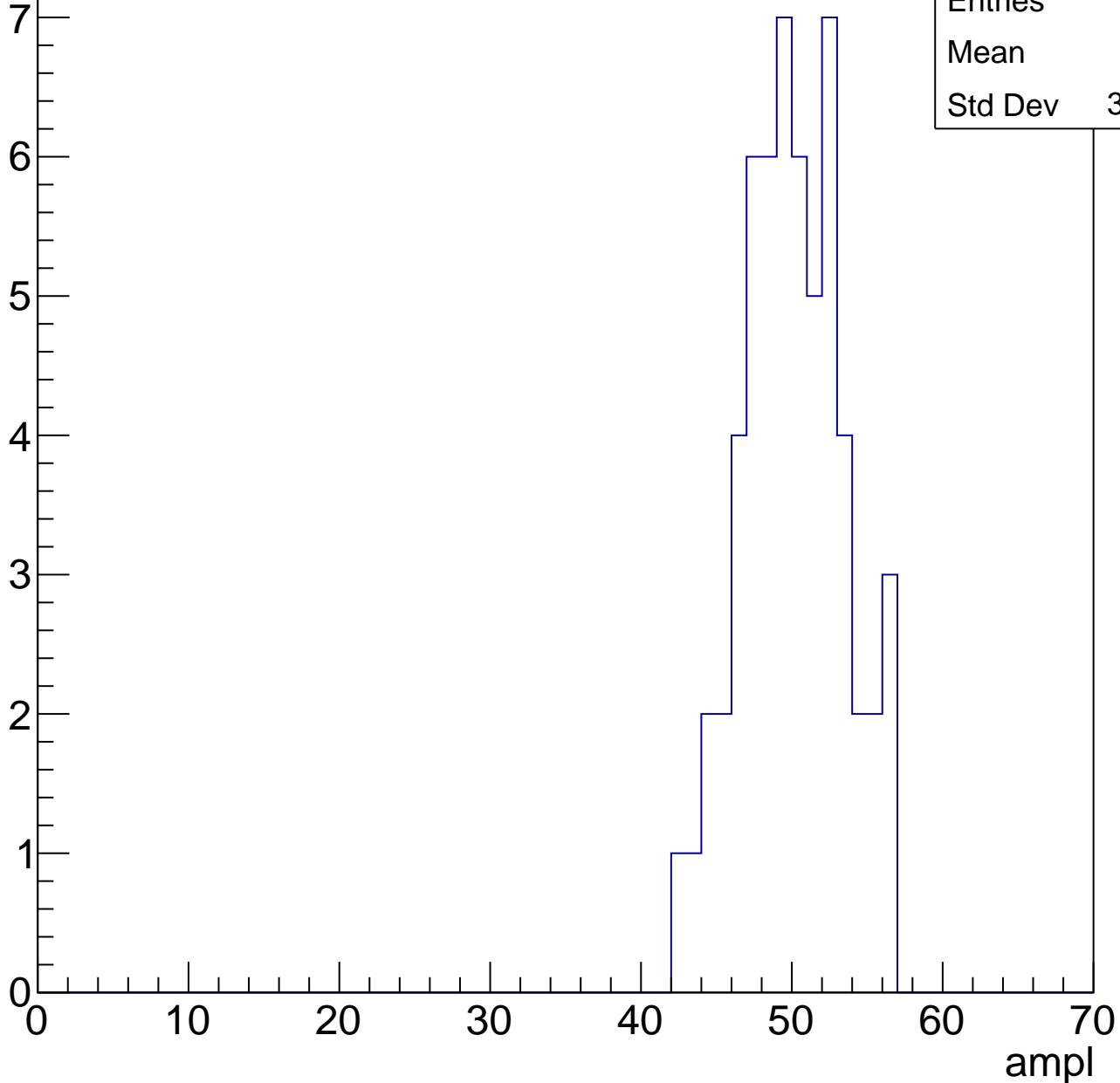


# B1L102S, U20-ch120, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	49.6
Std Dev	3.306

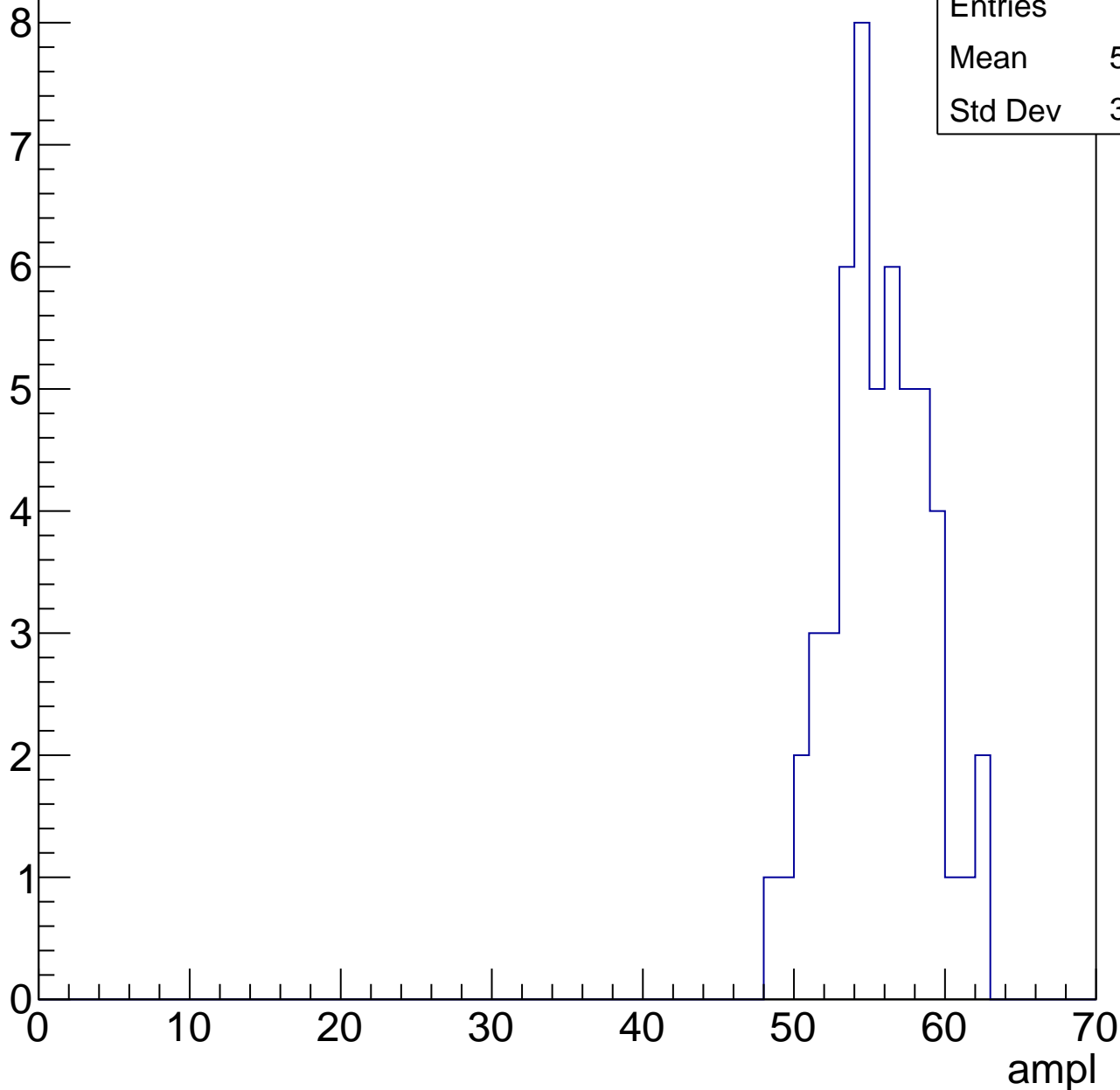


# B1L102S, U20-ch120, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	55.15
Std Dev	3.177

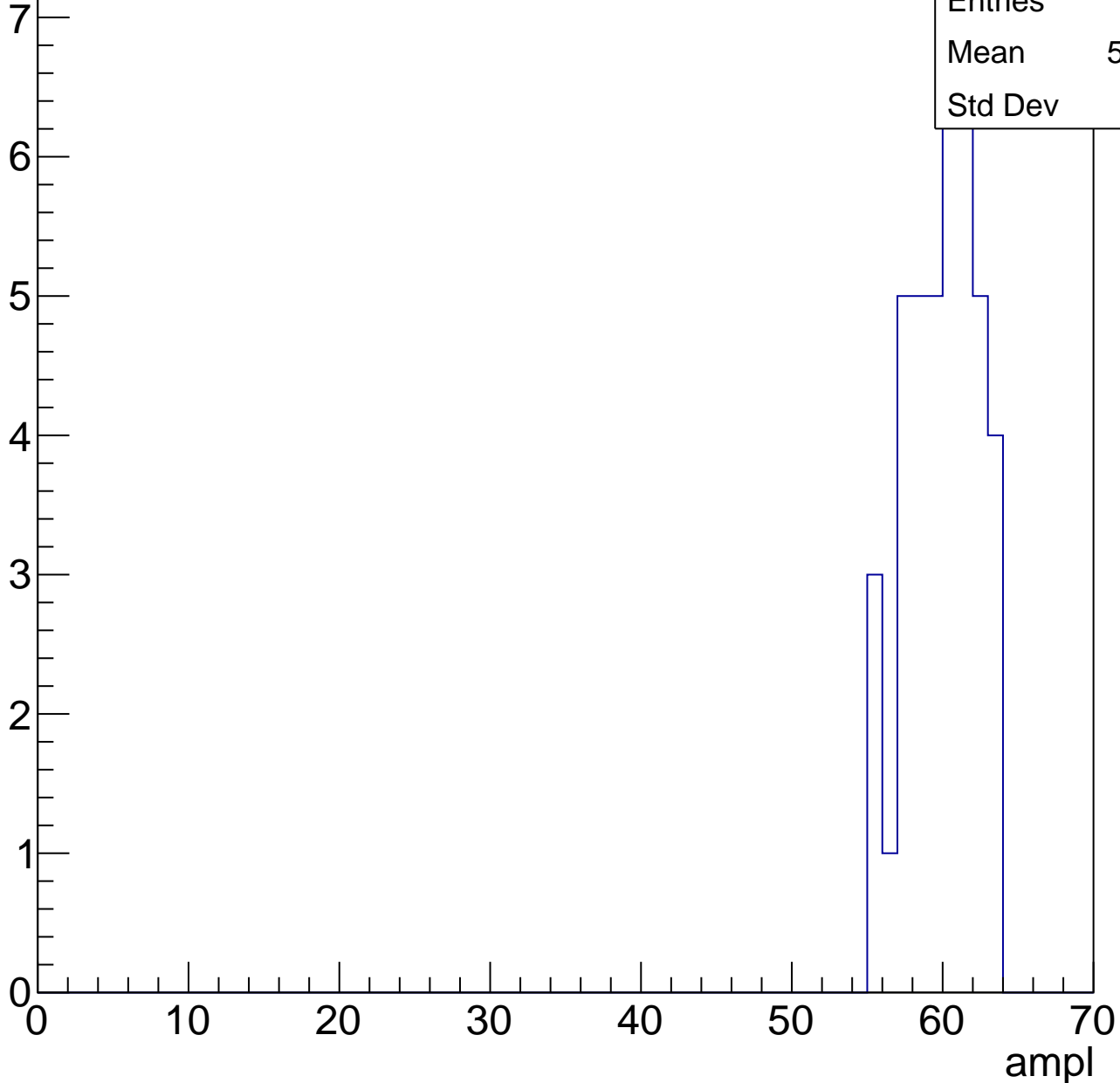


# B1L102S, U20-ch120, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	42
Mean	59.52
Std Dev	2.26

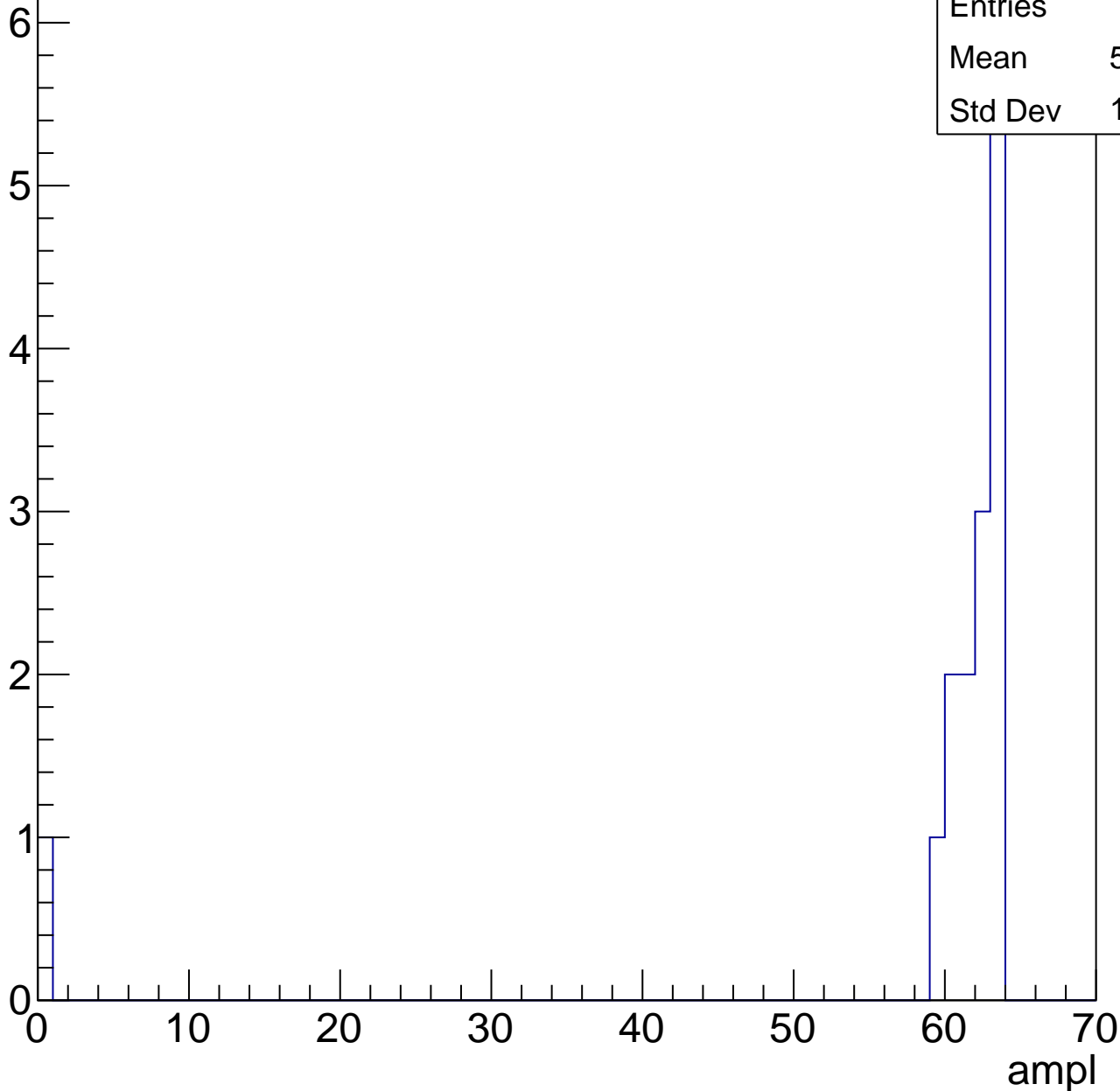


# B1L102S, U20-ch120, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	15
Mean	57.67
Std Dev	15.46

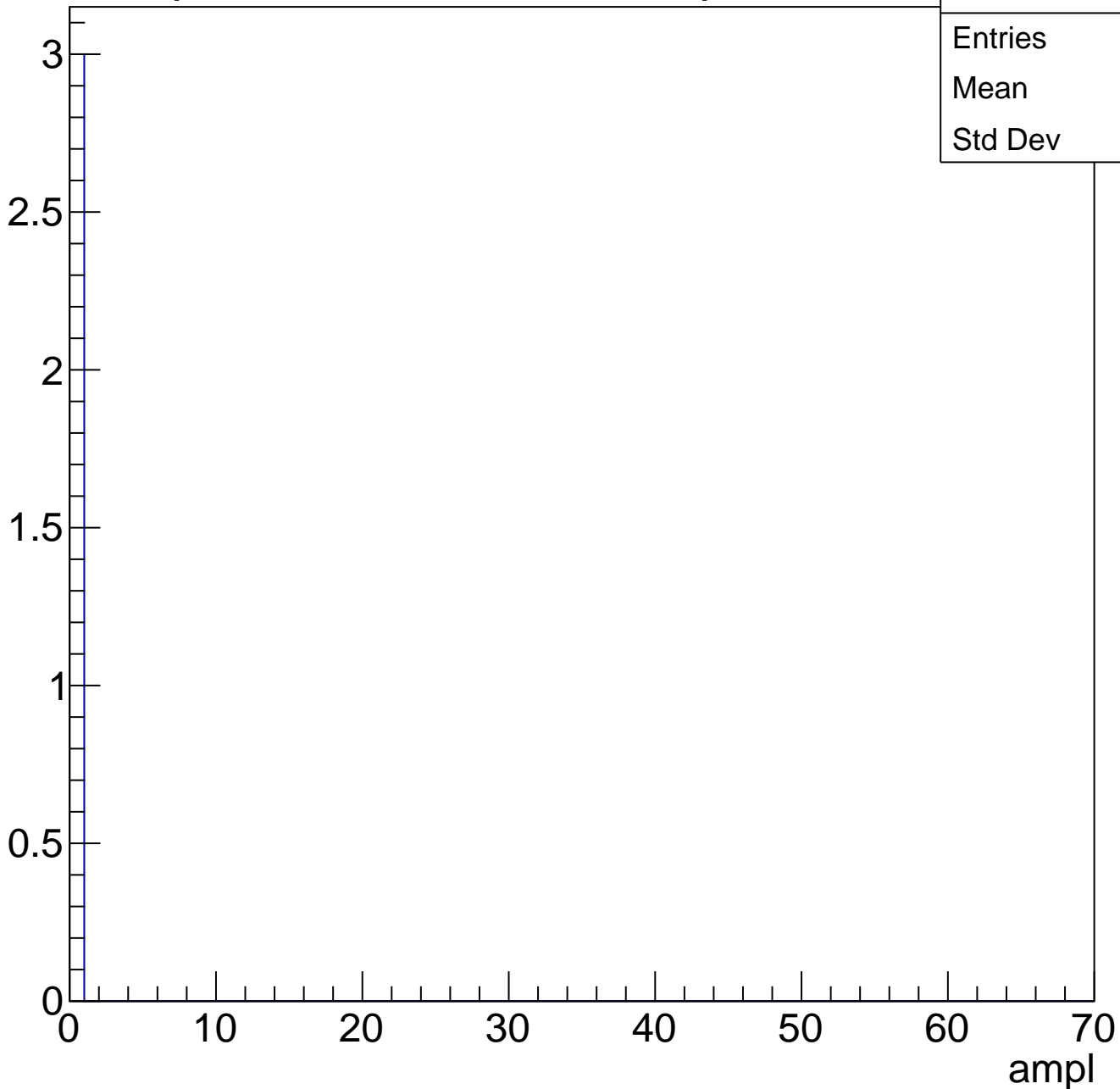




# B1L102S, U20-ch120, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L102S, U20-ch121, adc0

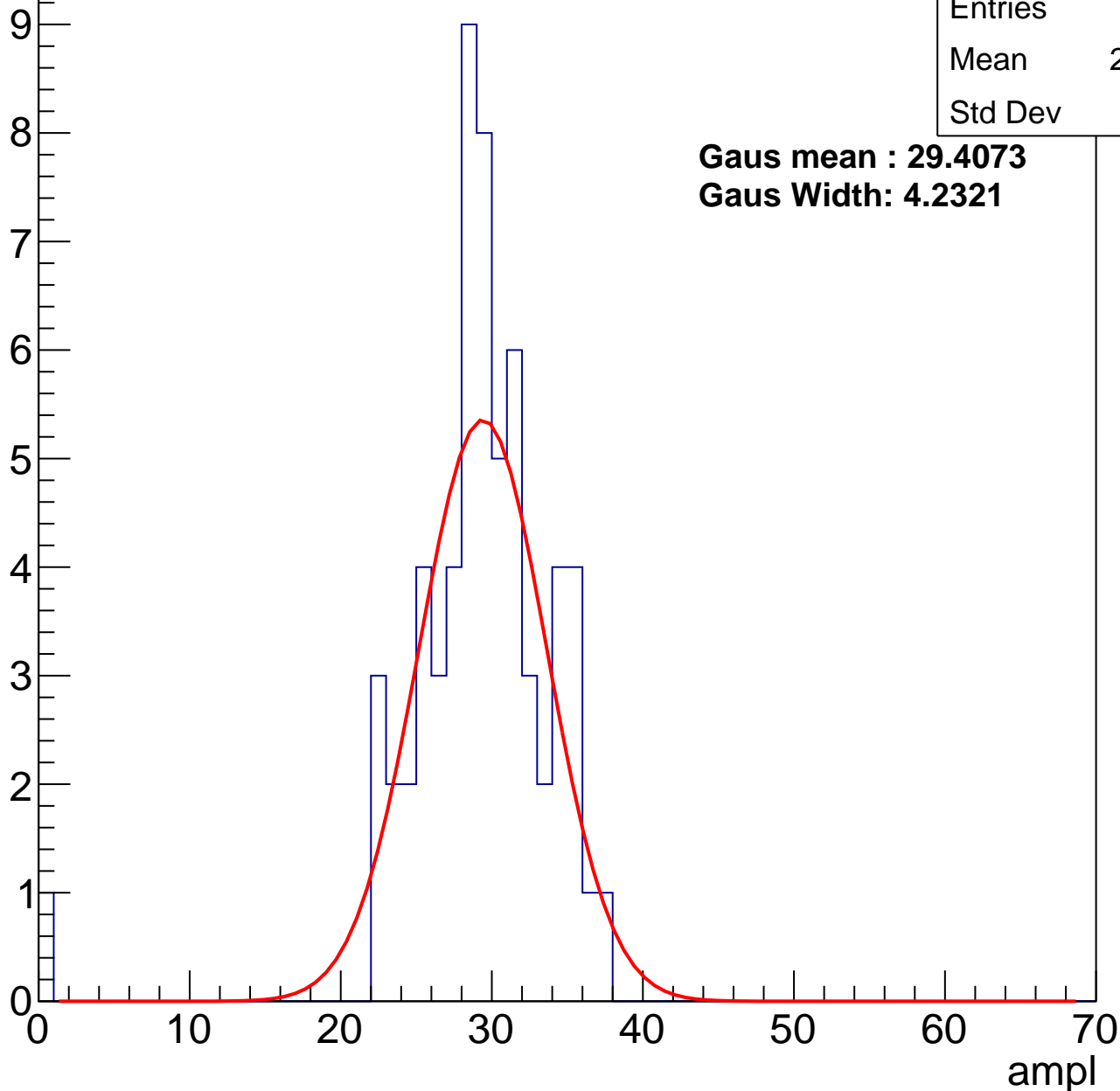
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	28.66
Std Dev	5.18

**Gaus mean : 29.4073**

**Gaus Width: 4.2321**



# B1L102S, U20-ch121, adc1

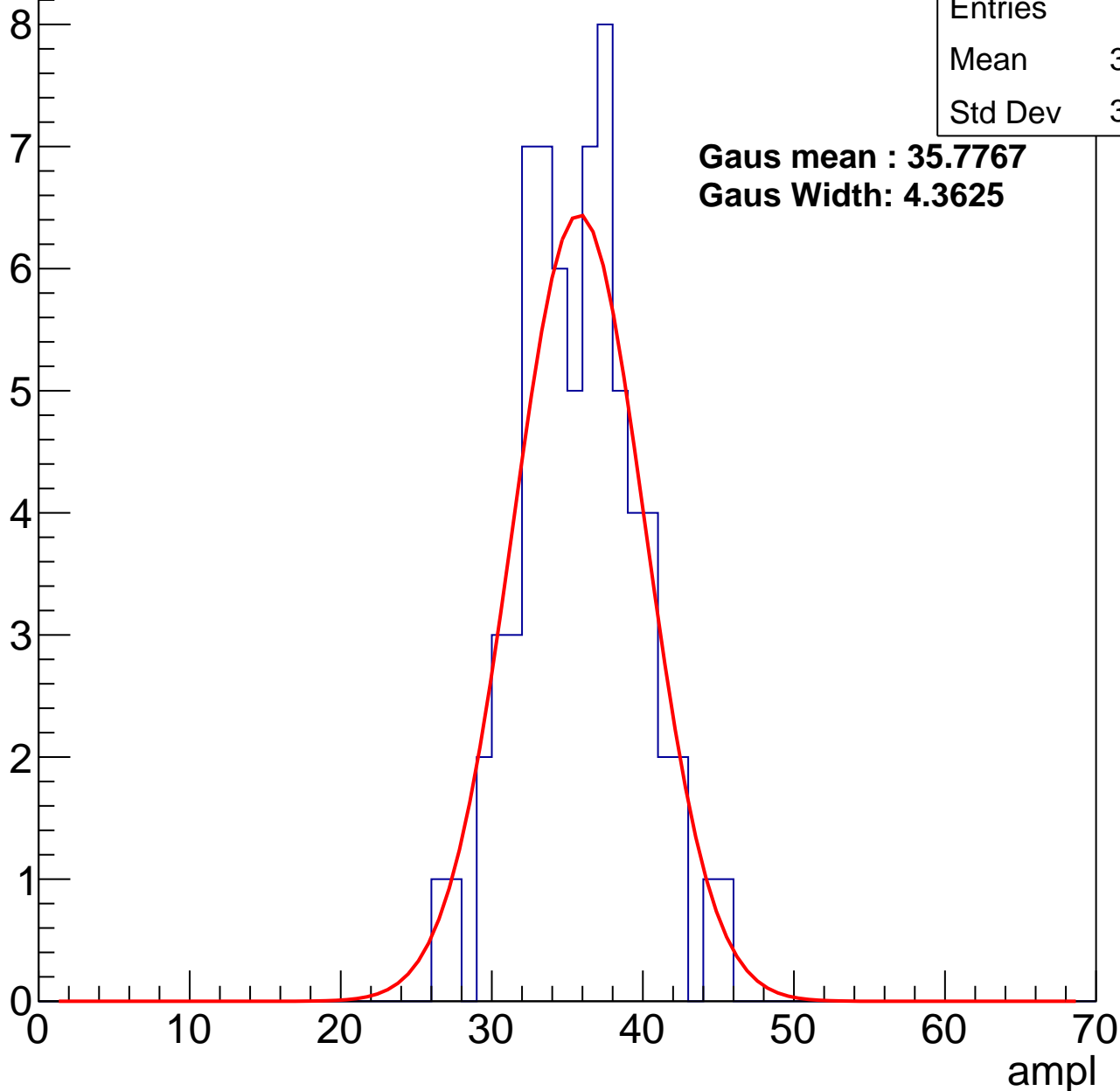
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	35.32
Std Dev	3.862

**Gaus mean : 35.7767**

**Gaus Width: 4.3625**



# B1L102S, U20-ch121, adc2

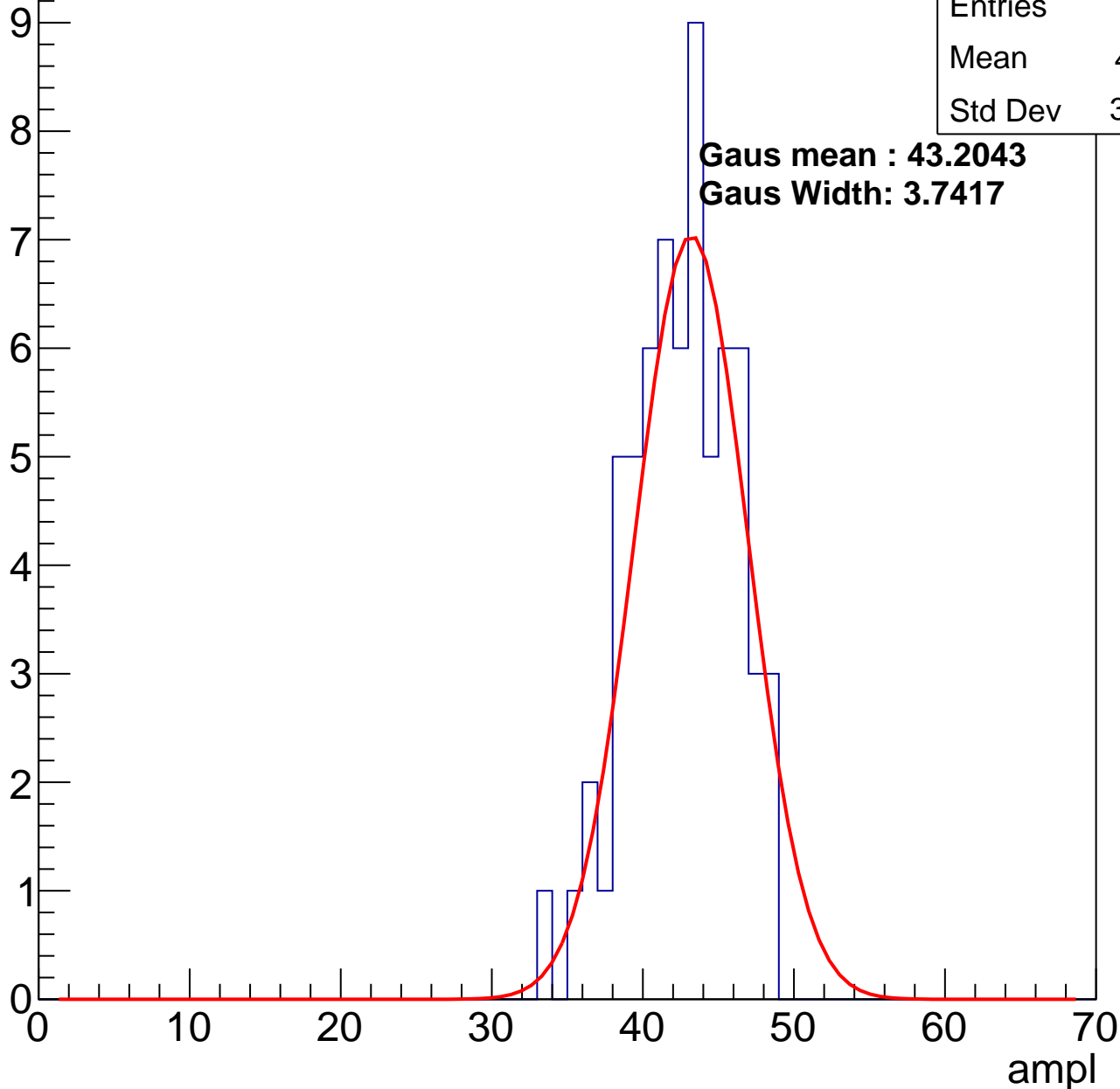
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	42.11
Std Dev	3.358

**Gaus mean : 43.2043**

**Gaus Width: 3.7417**

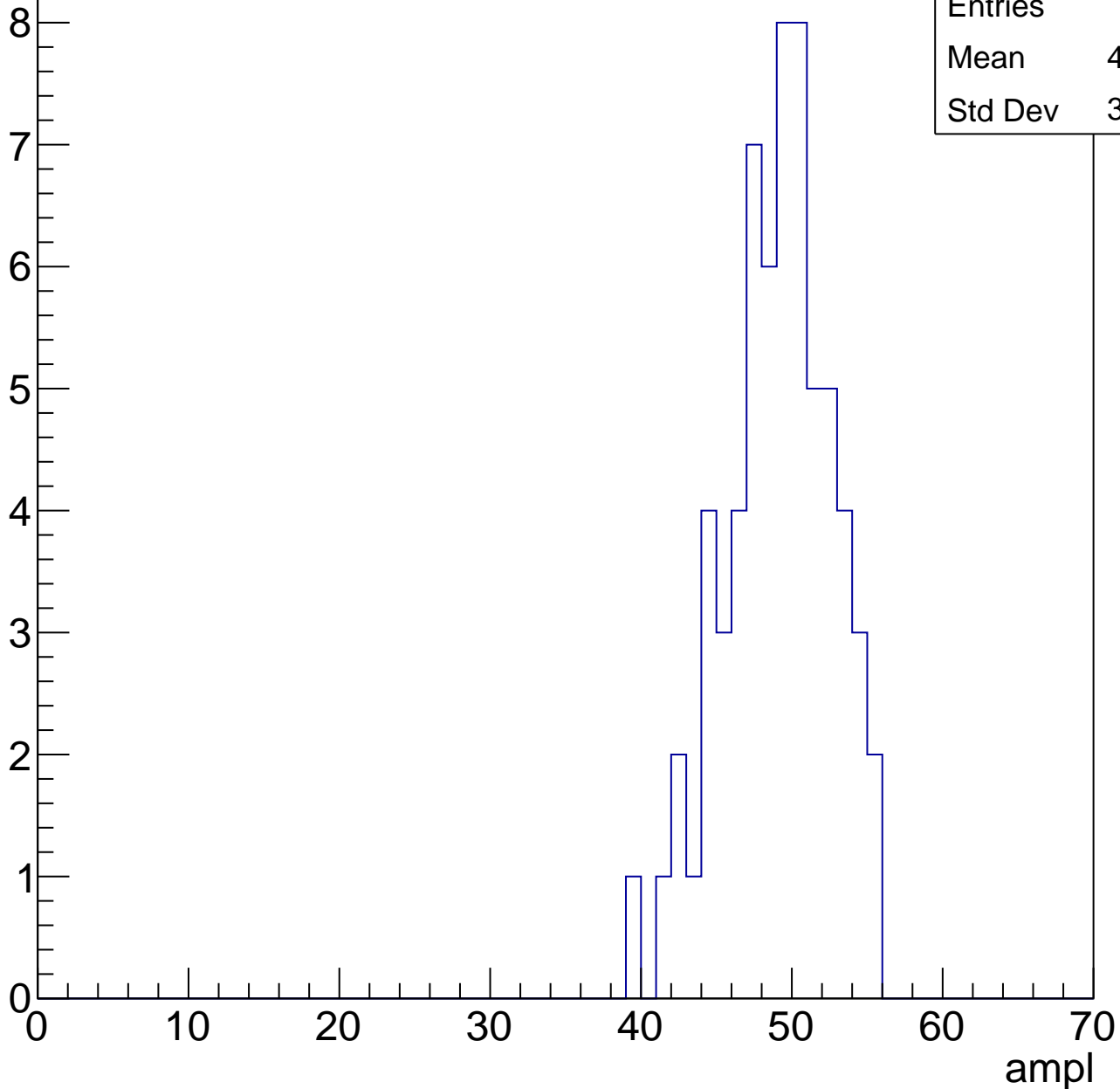


# B1L102S, U20-ch121, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	48.59
Std Dev	3.512

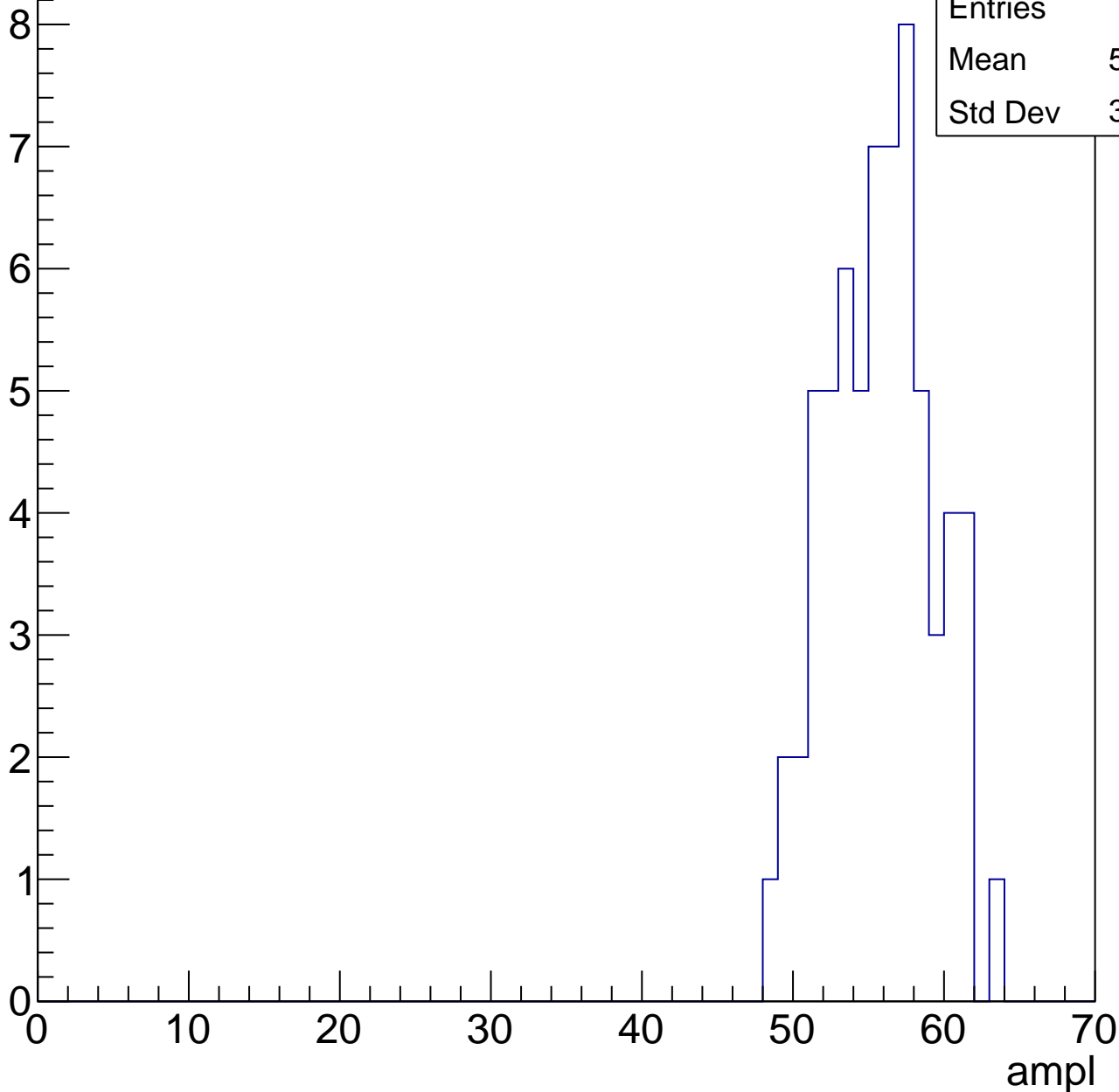


# B1L102S, U20-ch121, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	55.32
Std Dev	3.415

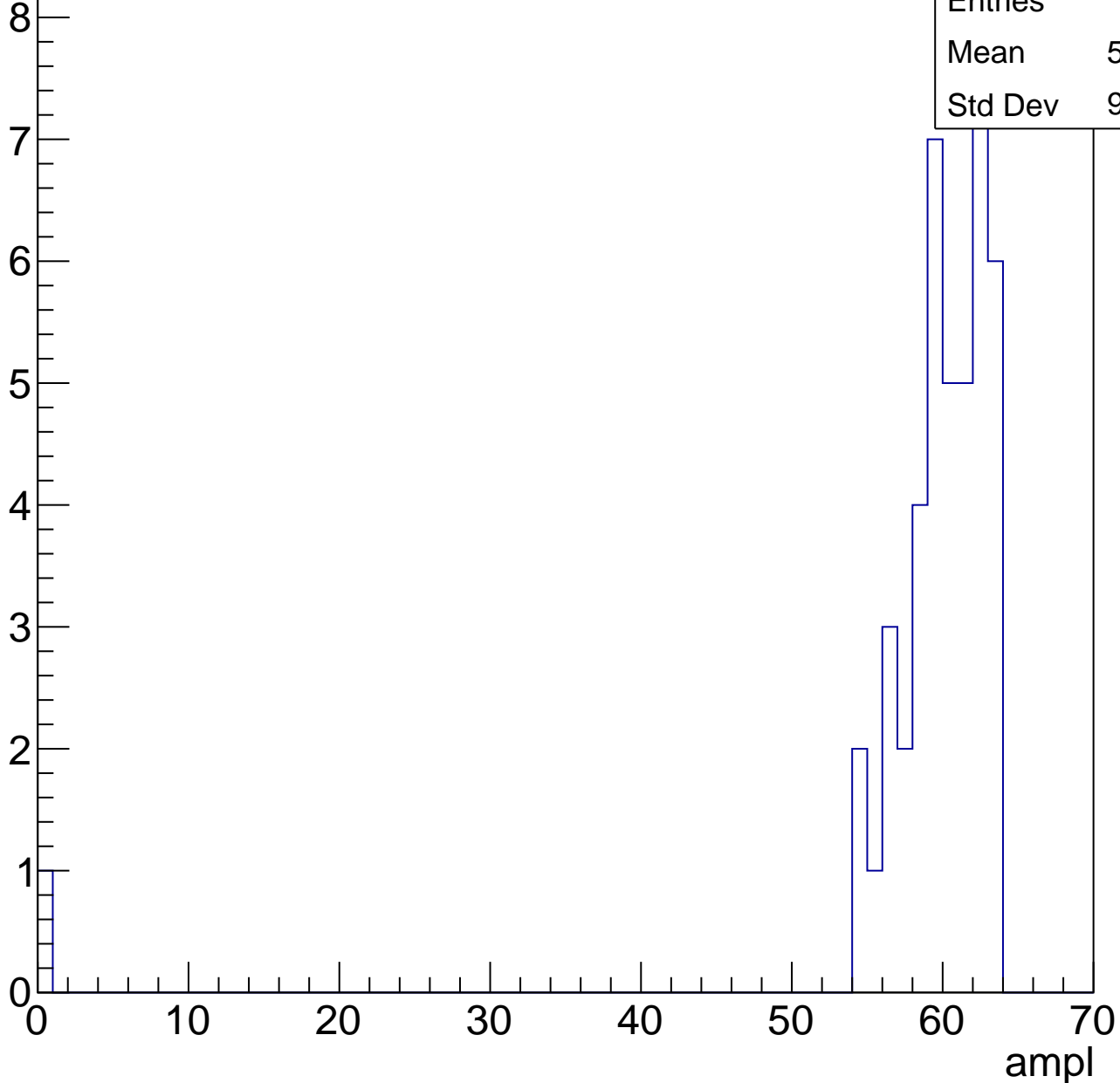


# B1L102S, U20-ch121, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

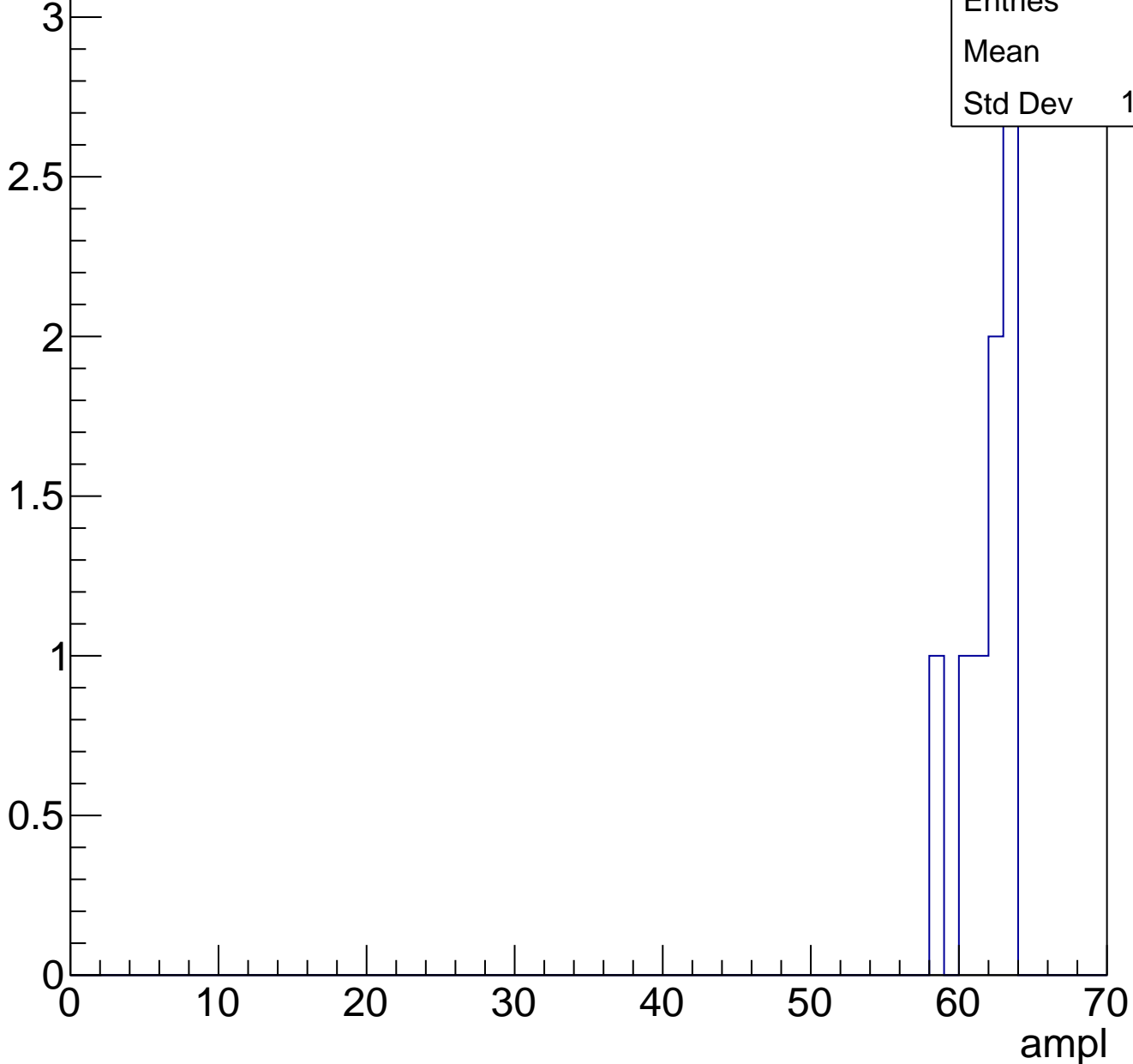
Entries	44
Mean	58.39
Std Dev	9.247



# B1L102S, U20-ch121, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U20-ch121, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch122, adc0

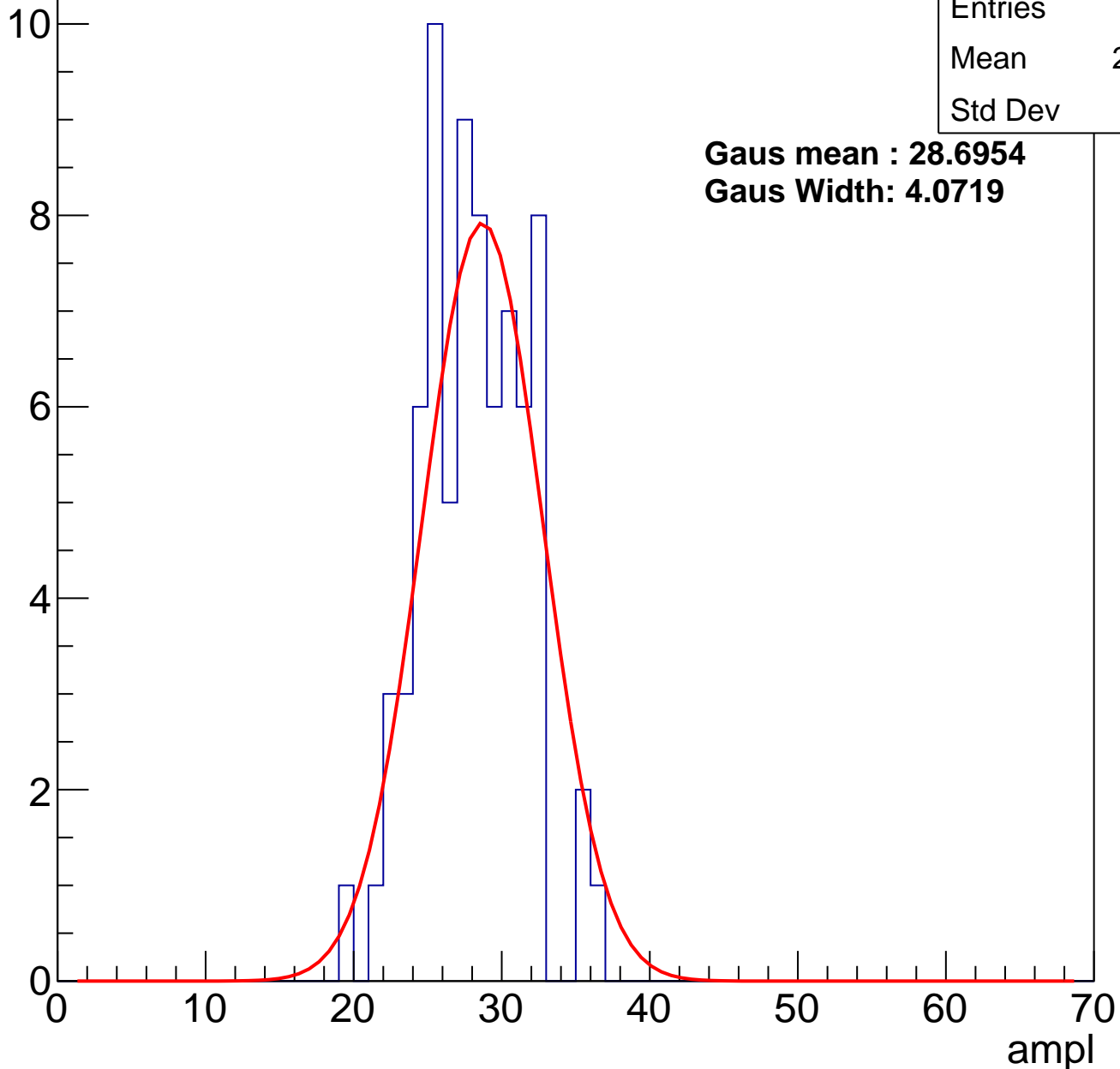
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	76
Mean	27.61
Std Dev	3.43

**Gaus mean : 28.6954**

**Gaus Width: 4.0719**

Entry



# B1L102S, U20-ch122, adc1

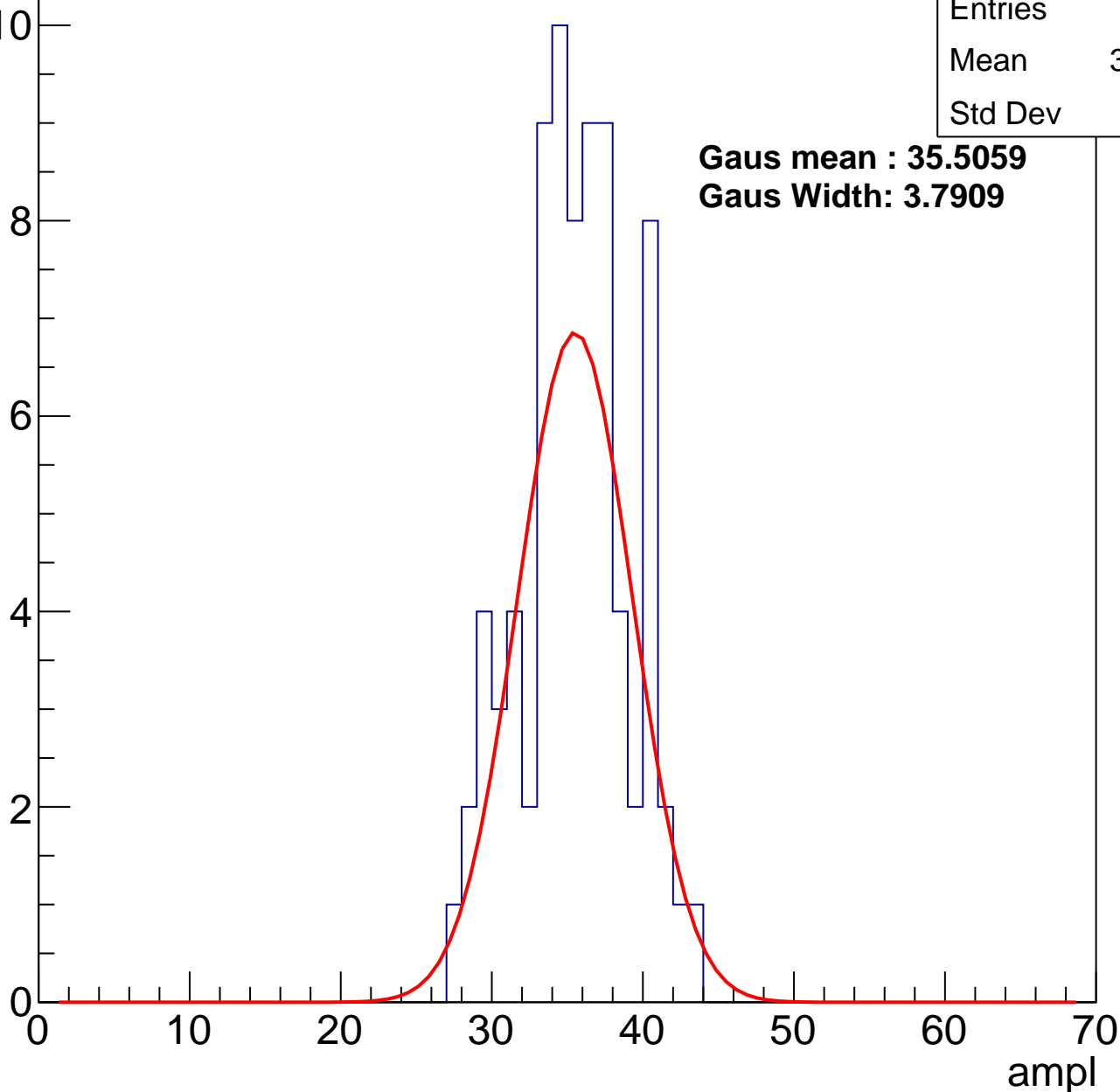
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	79
Mean	35.04
Std Dev	3.57

**Gaus mean : 35.5059**

**Gaus Width: 3.7909**



# B1L102S, U20-ch122, adc2

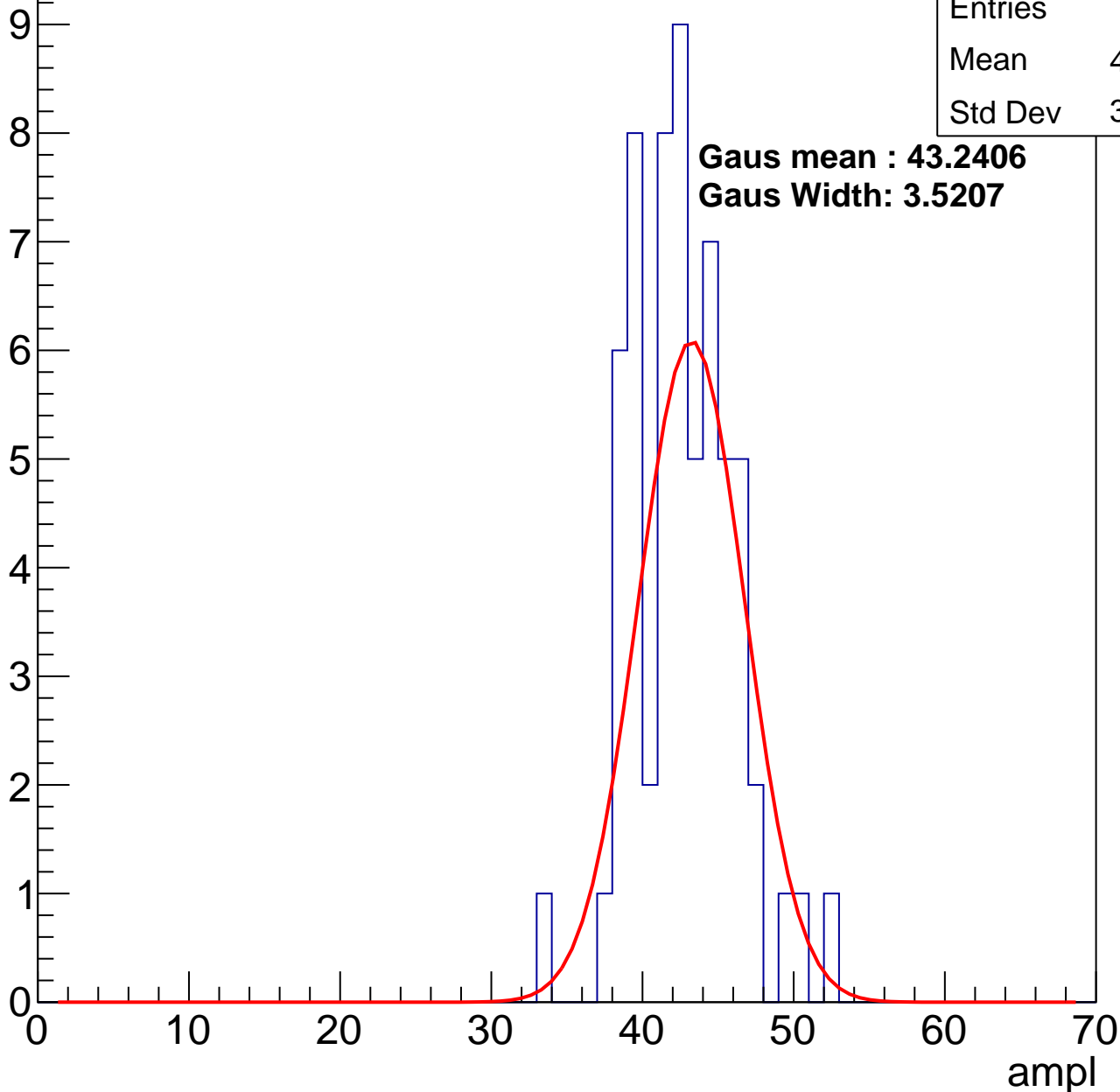
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	42.24
Std Dev	3.378

**Gaus mean : 43.2406**

**Gaus Width: 3.5207**

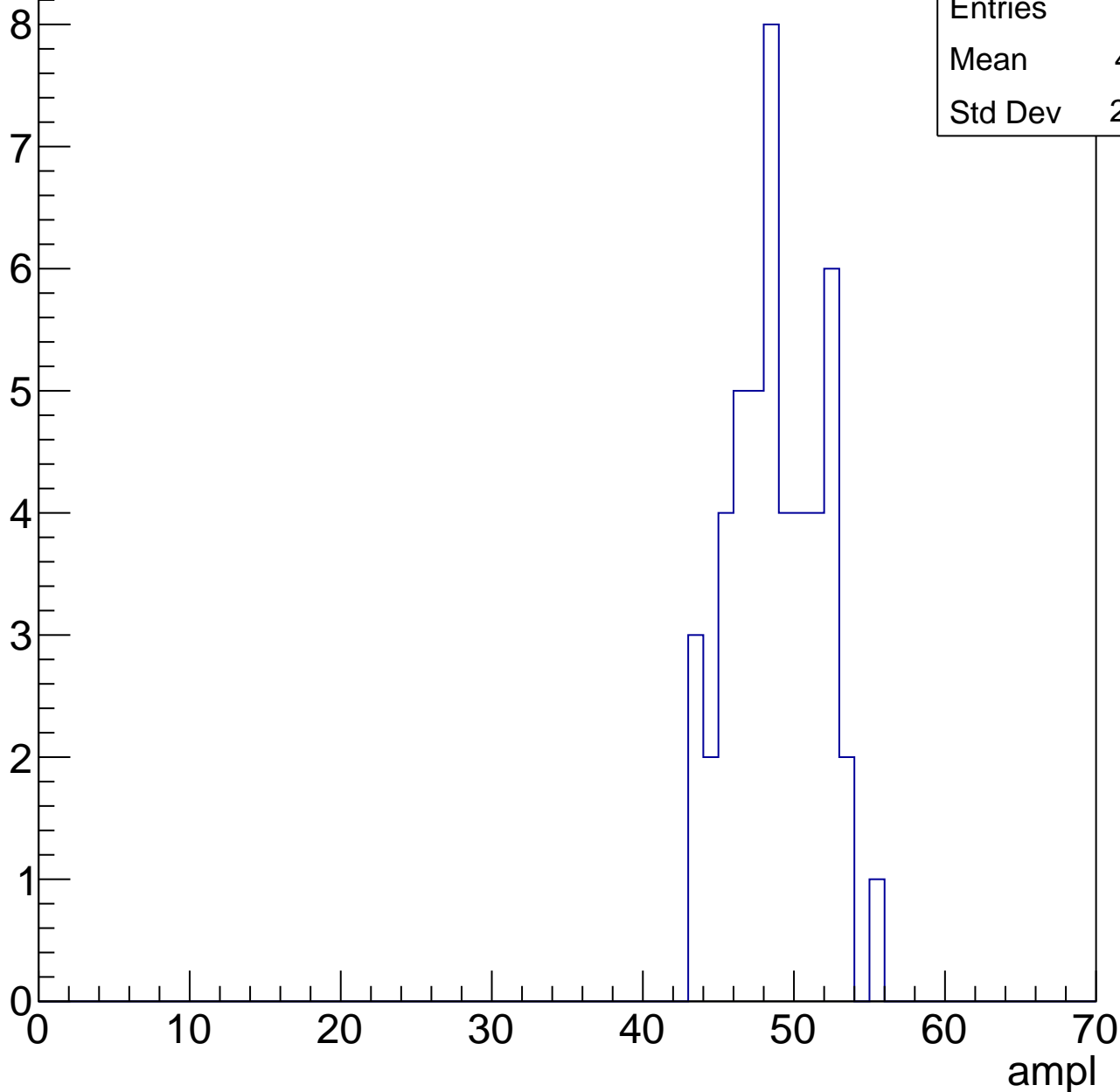


# B1L102S, U20-ch122, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	48
Mean	48.31
Std Dev	2.938

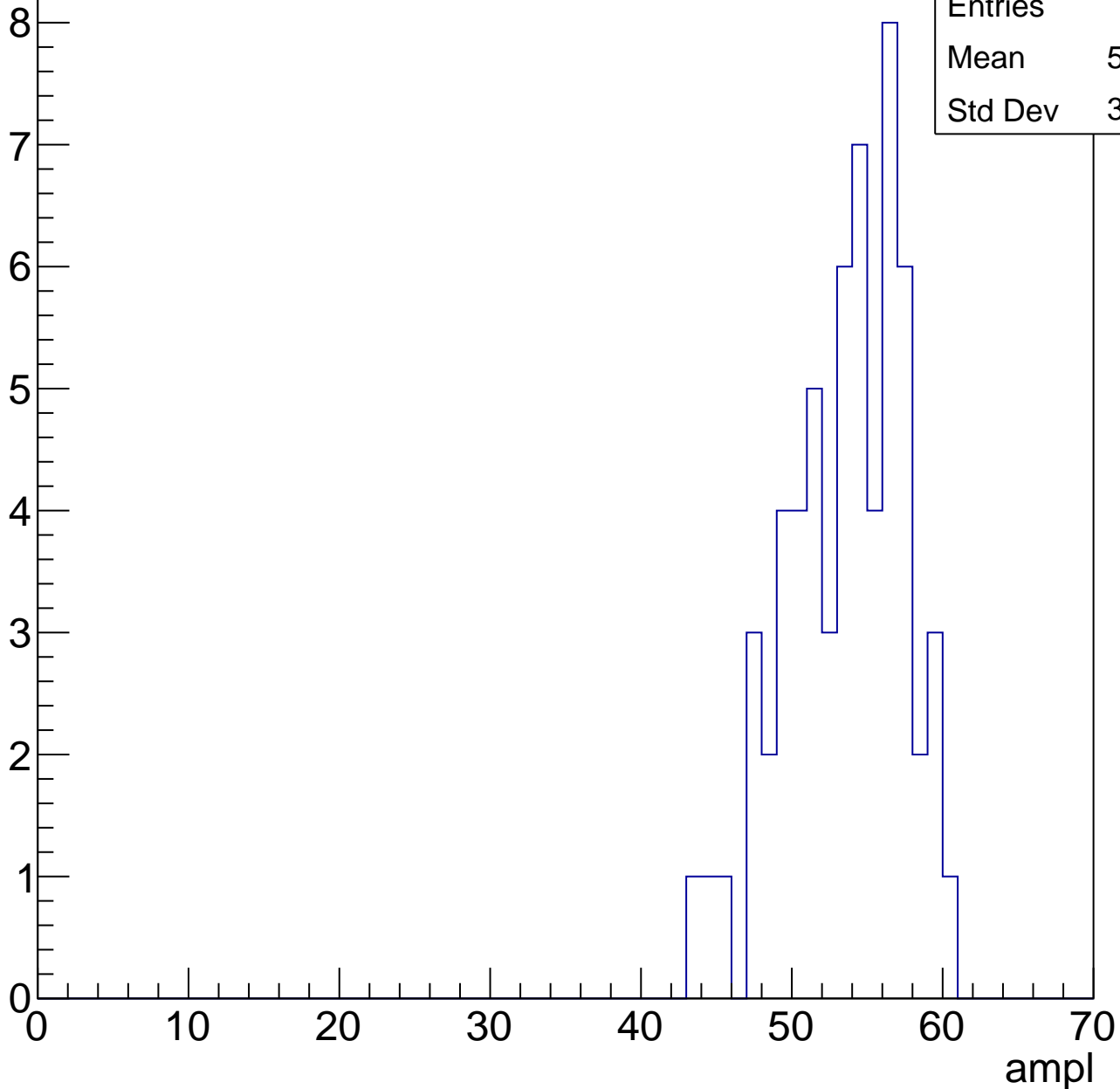


# B1L102S, U20-ch122, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	53.03
Std Dev	3.892

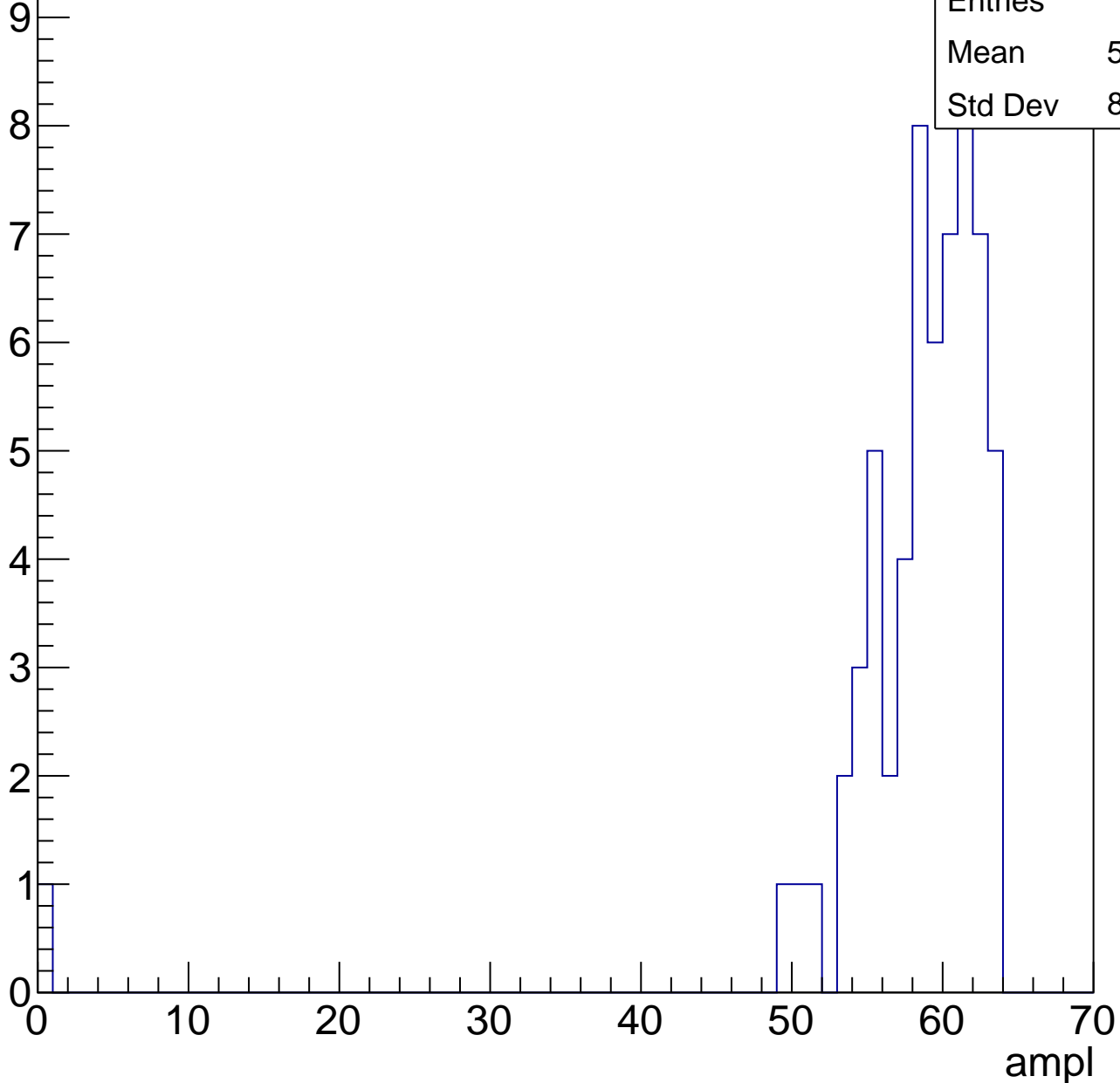


# B1L102S, U20-ch122, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	57.56
Std Dev	8.085

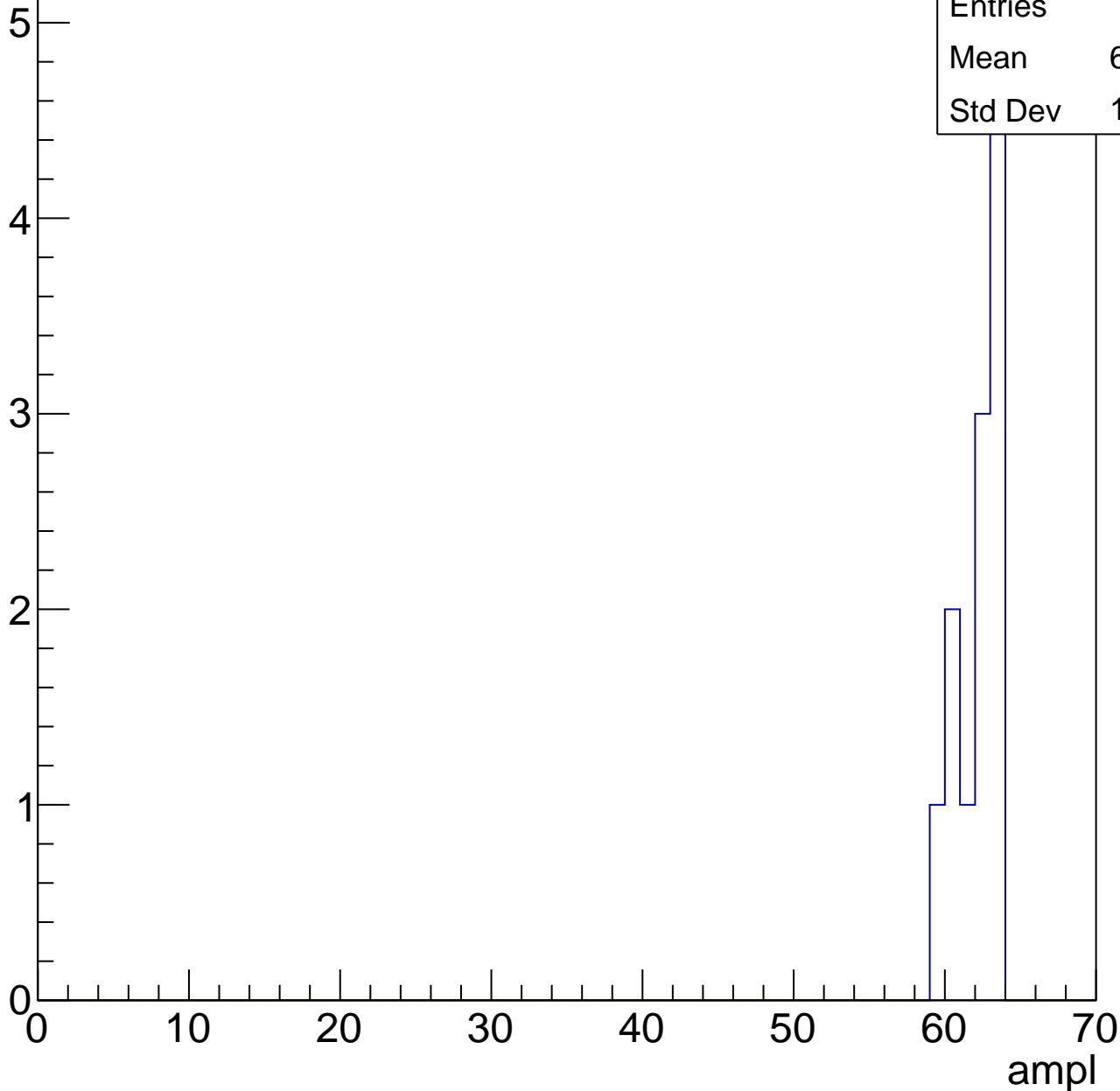


# B1L102S, U20-ch122, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	12
Mean	61.75
Std Dev	1.362





# B1L102S, U20-ch122, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U20-ch123, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	87
Mean	27.13
Std Dev	7.418

**Gaus mean : 29.4639**

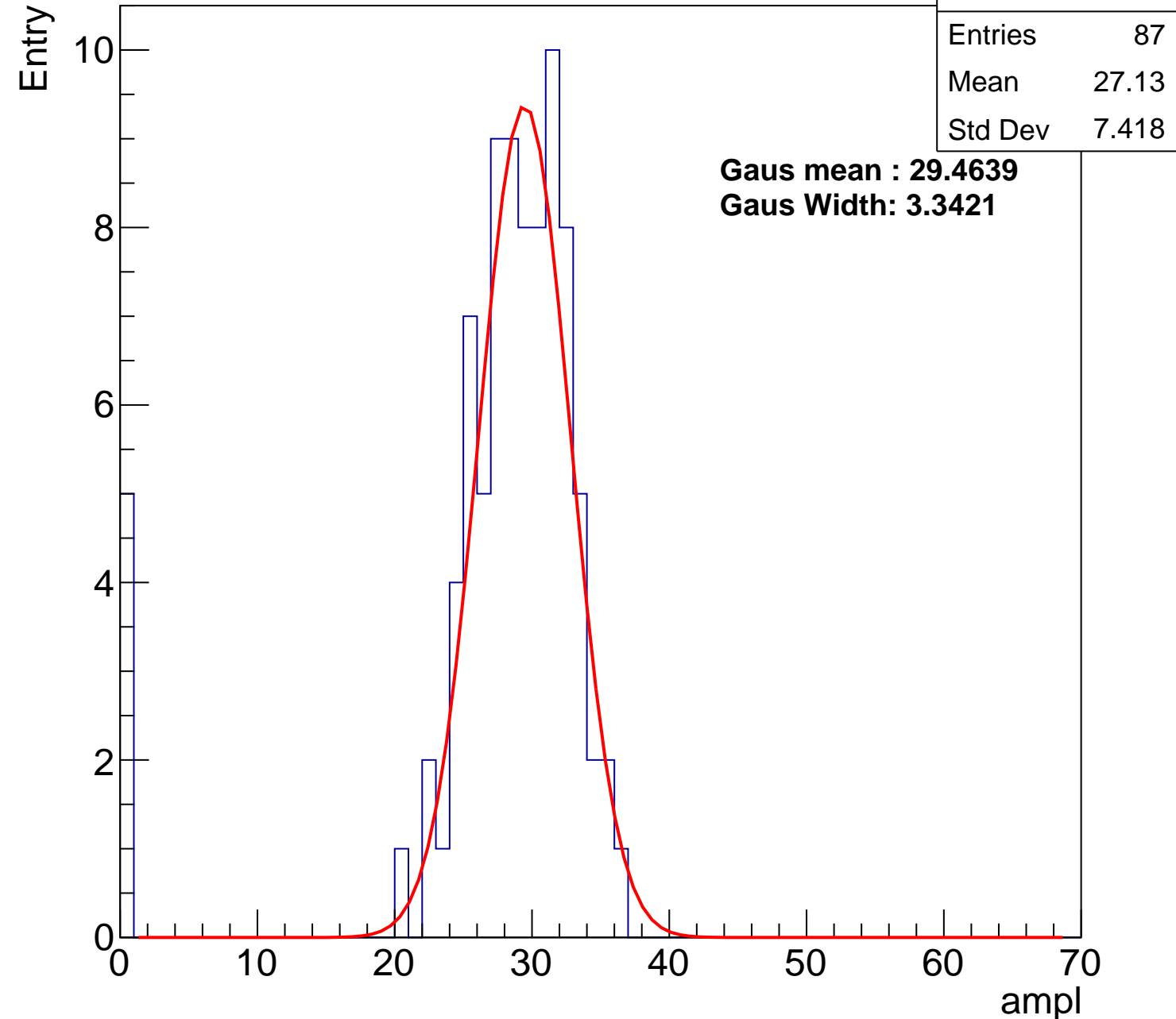
**Gaus Width: 3.3421**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U20-ch123, adc1

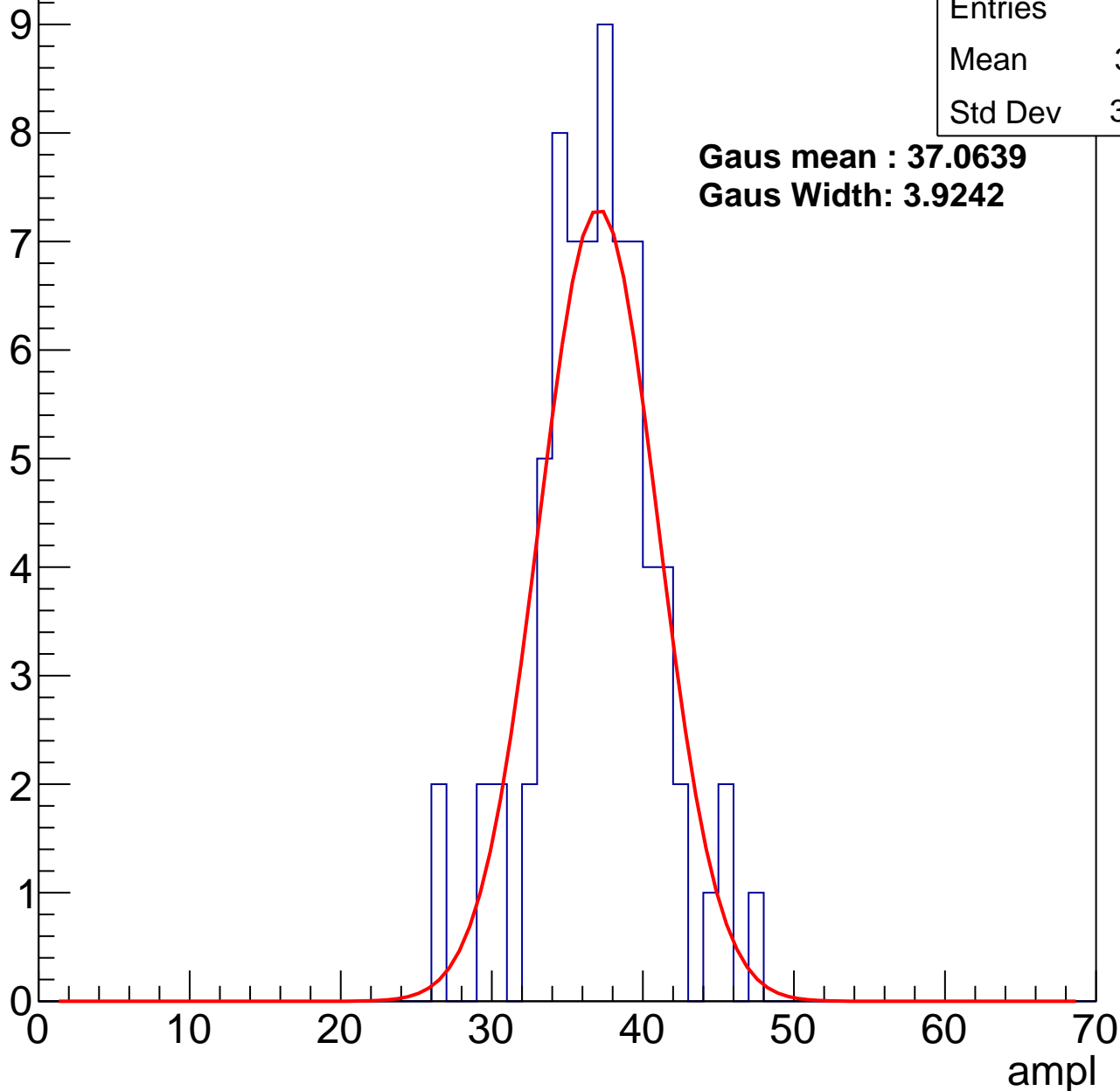
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	36.51
Std Dev	3.997

**Gaus mean : 37.0639**

**Gaus Width: 3.9242**



# B1L102S, U20-ch123, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	42.66
Std Dev	3.289

**Gaus mean : 43.2850**

**Gaus Width: 3.3869**

10

8

6

4

2

0

0

10

20

30

40

50

60

70

ampl

0

2

4

6

8

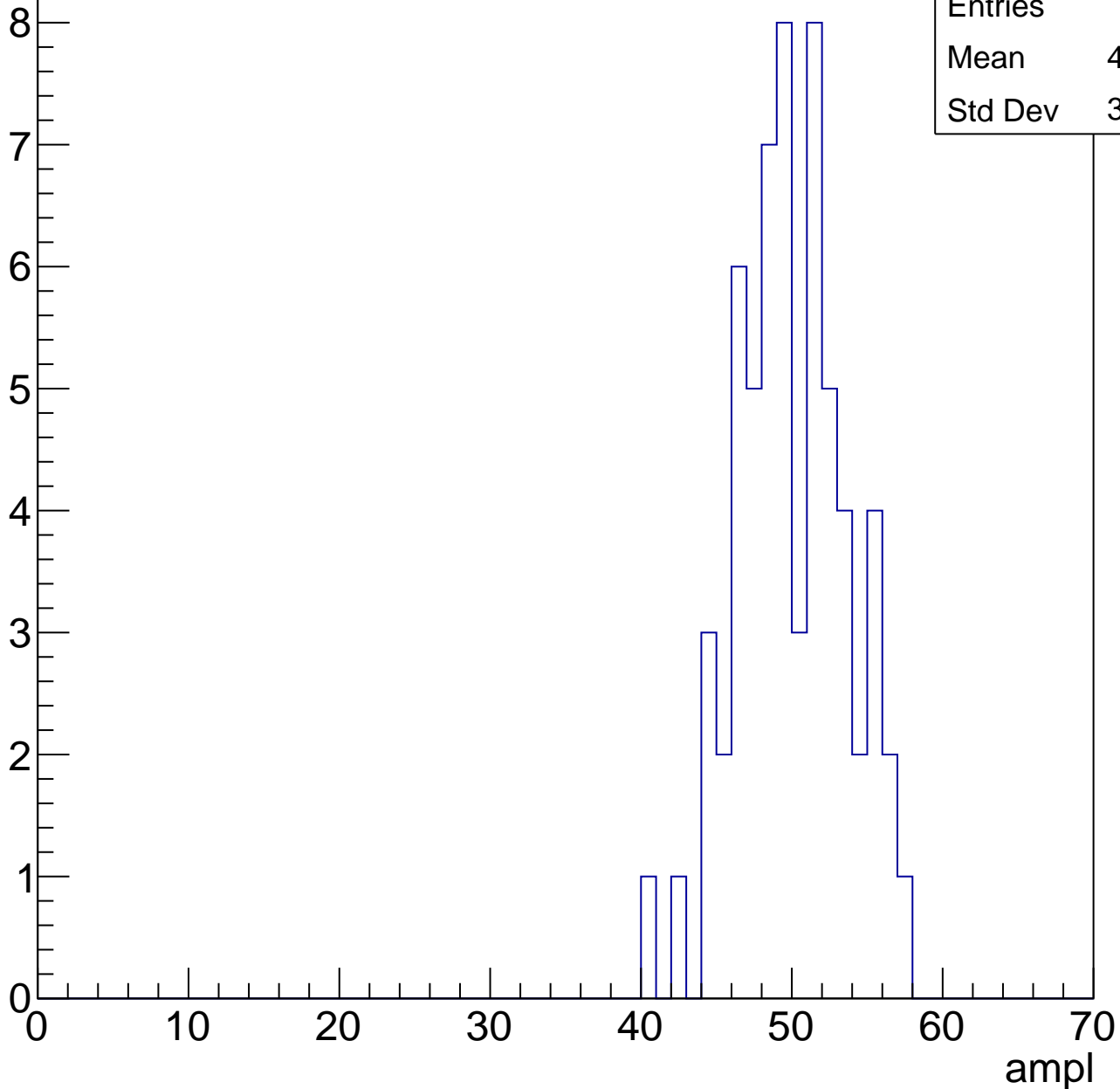
10

# B1L102S, U20-ch123, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	49.52
Std Dev	3.595

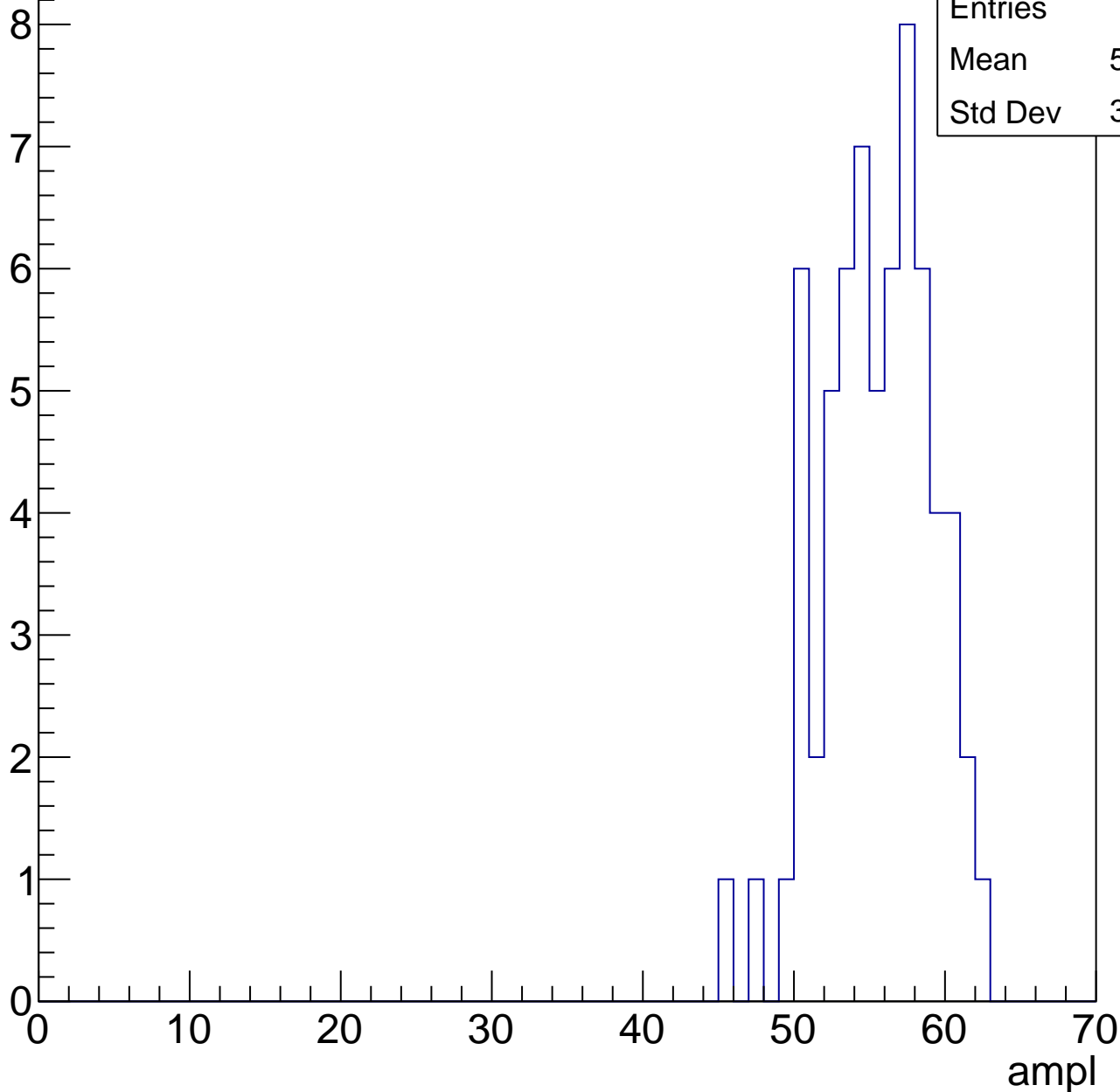


# B1L102S, U20-ch123, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	54.98
Std Dev	3.584

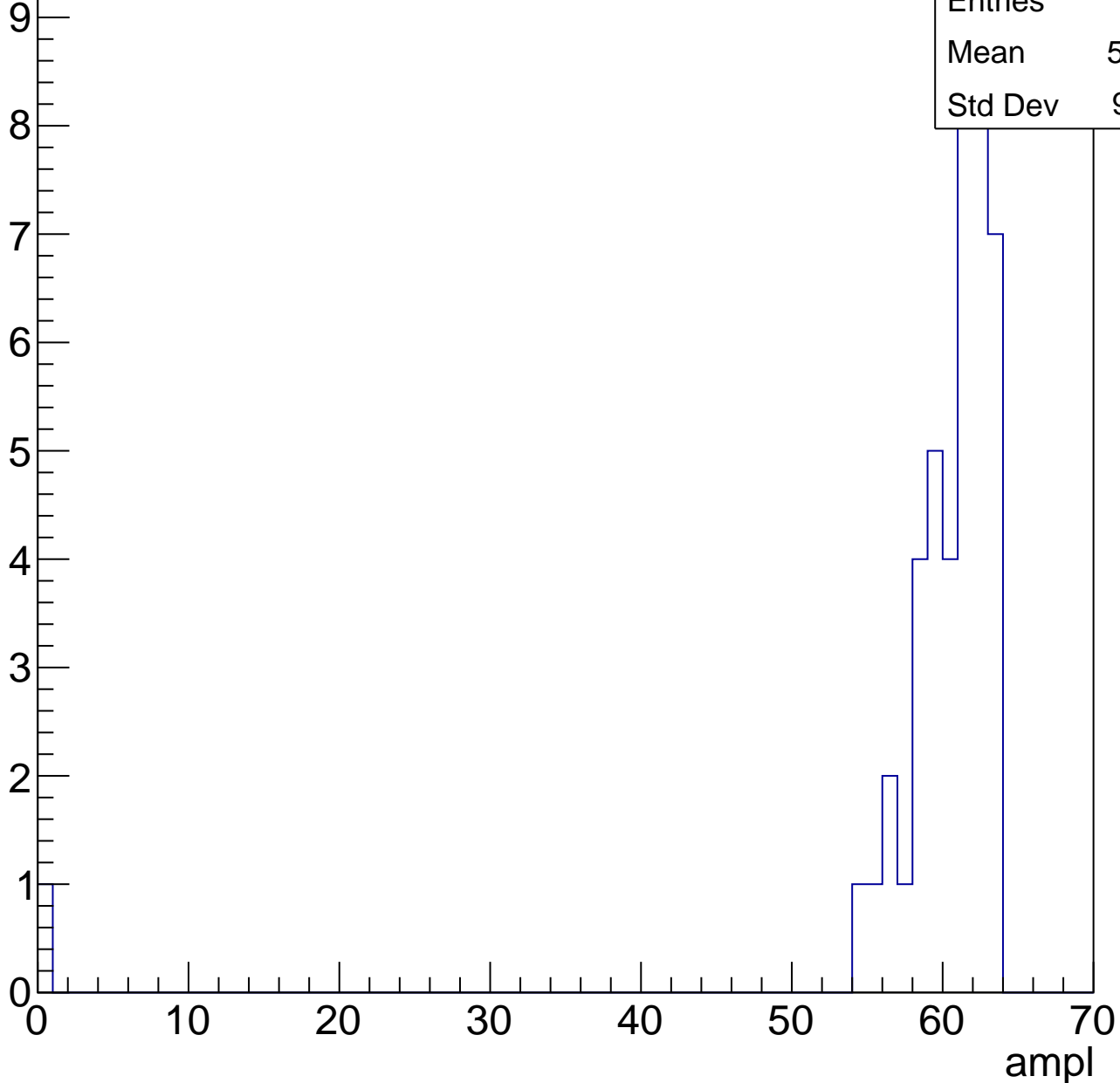


# B1L102S, U20-ch123, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	43
Mean	58.88
Std Dev	9.371



# B1L102S, U20-ch123, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	61
Std Dev	1.673

ampl

0 10 20 30 40 50 60 70



# B1L102S, U20-ch123, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch124, adc0

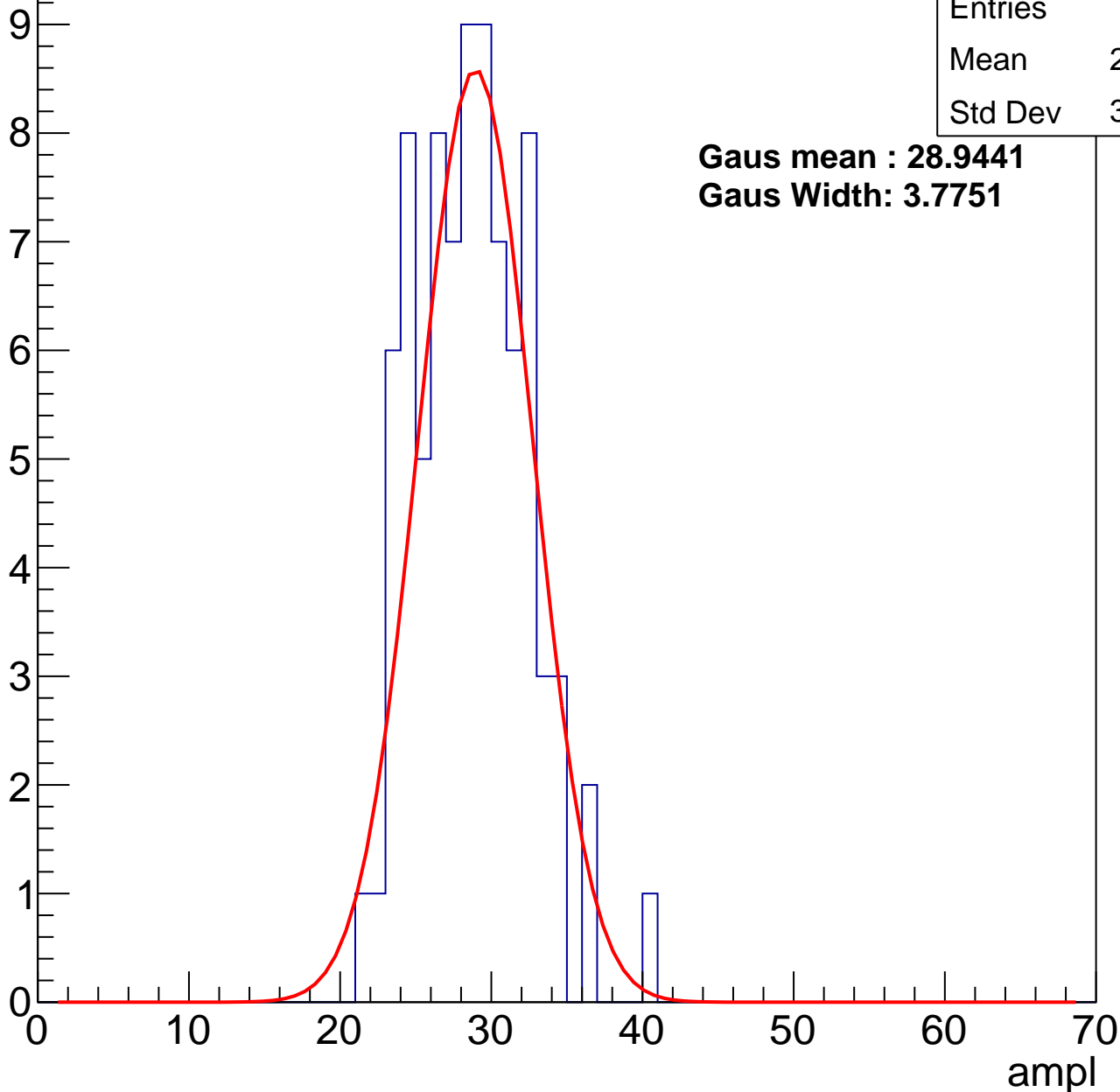
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	84
Mean	28.25
Std Dev	3.645

**Gaus mean : 28.9441**

**Gaus Width: 3.7751**



# B1L102S, U20-ch124, adc1

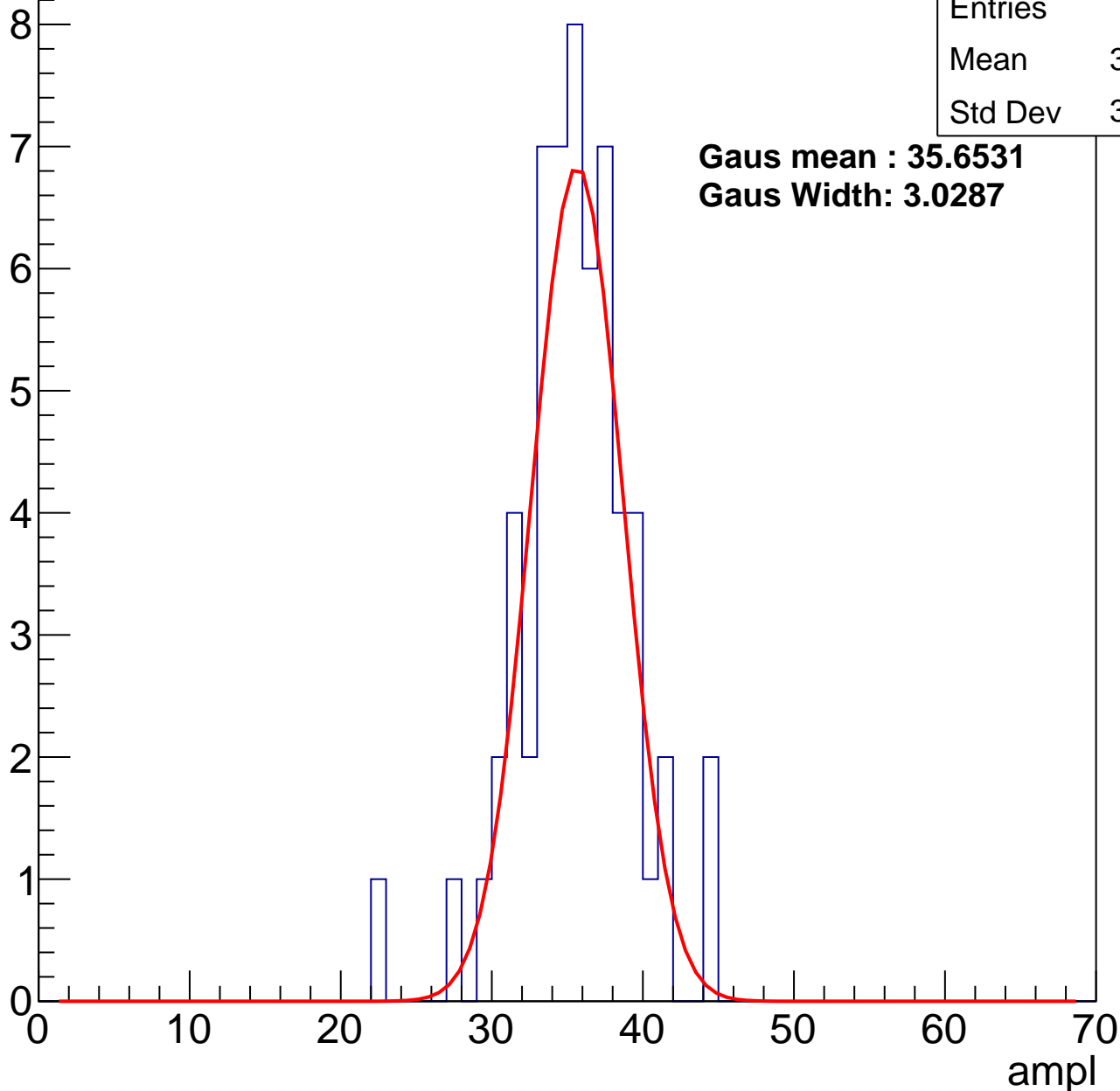
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	35.05
Std Dev	3.748

**Gaus mean : 35.6531**

**Gaus Width: 3.0287**



# B1L102S, U20-ch124, adc2

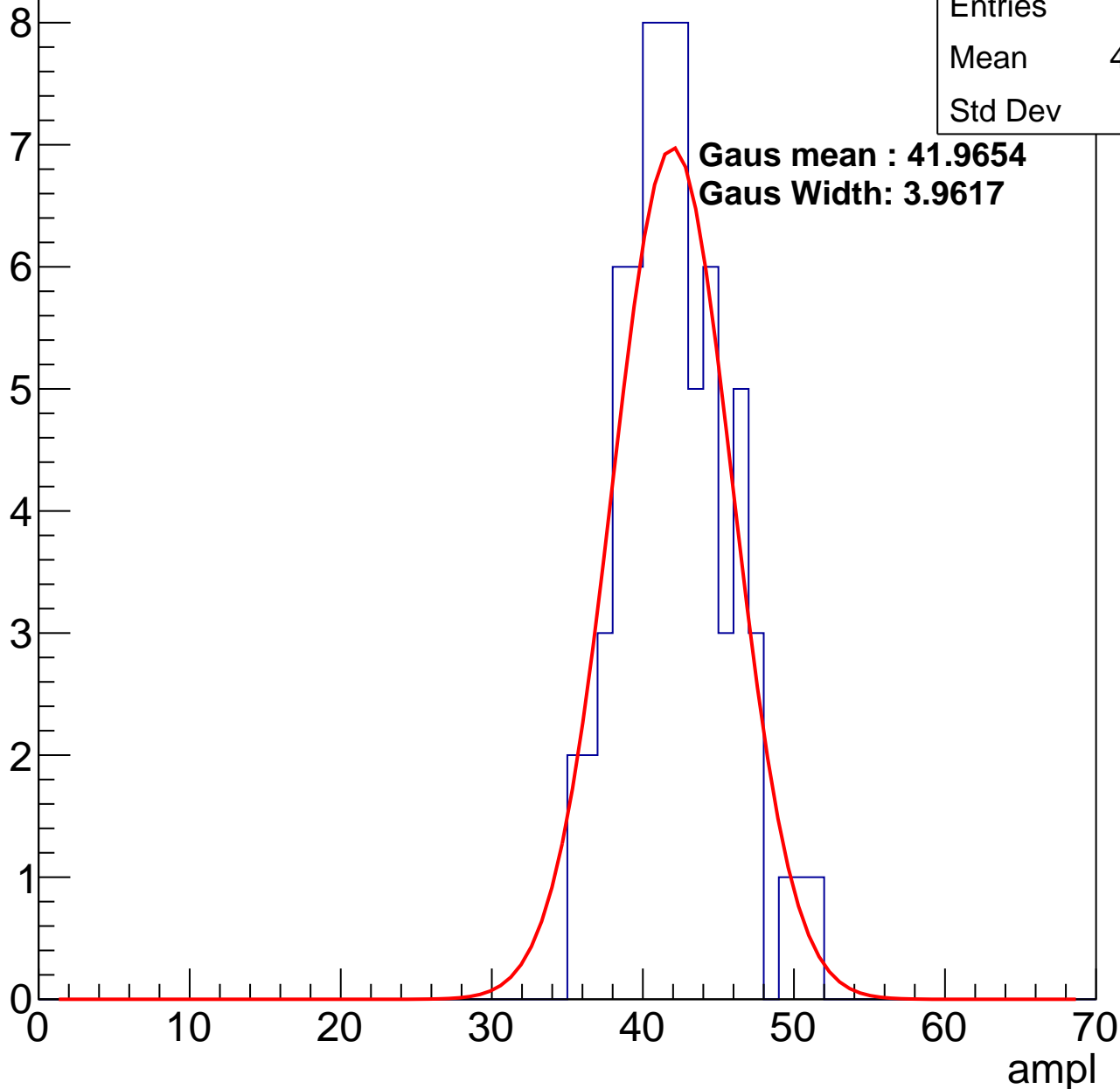
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	41.68
Std Dev	3.5

**Gaus mean : 41.9654**

**Gaus Width: 3.9617**

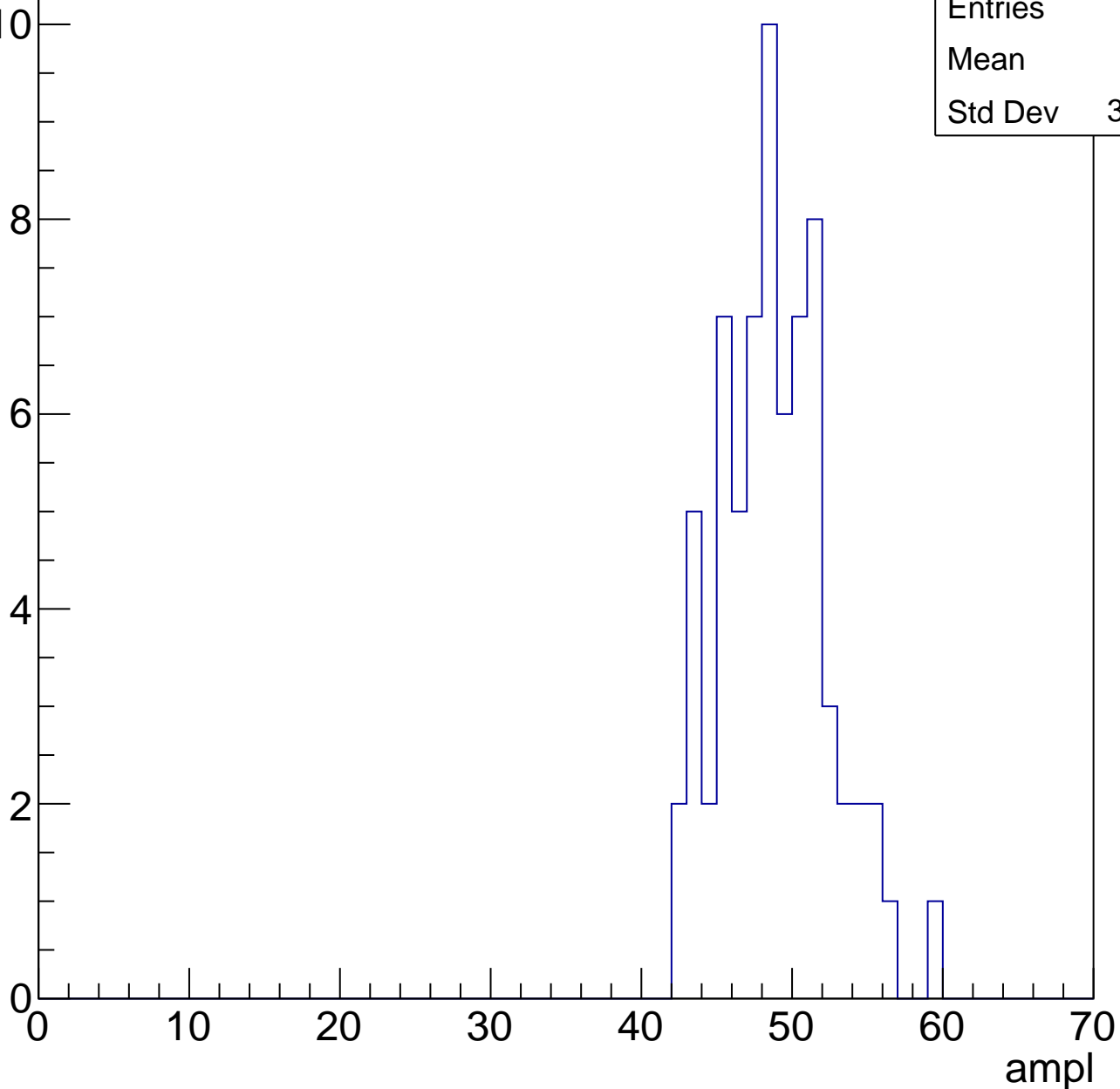


# B1L102S, U20-ch124, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	48.4
Std Dev	3.519

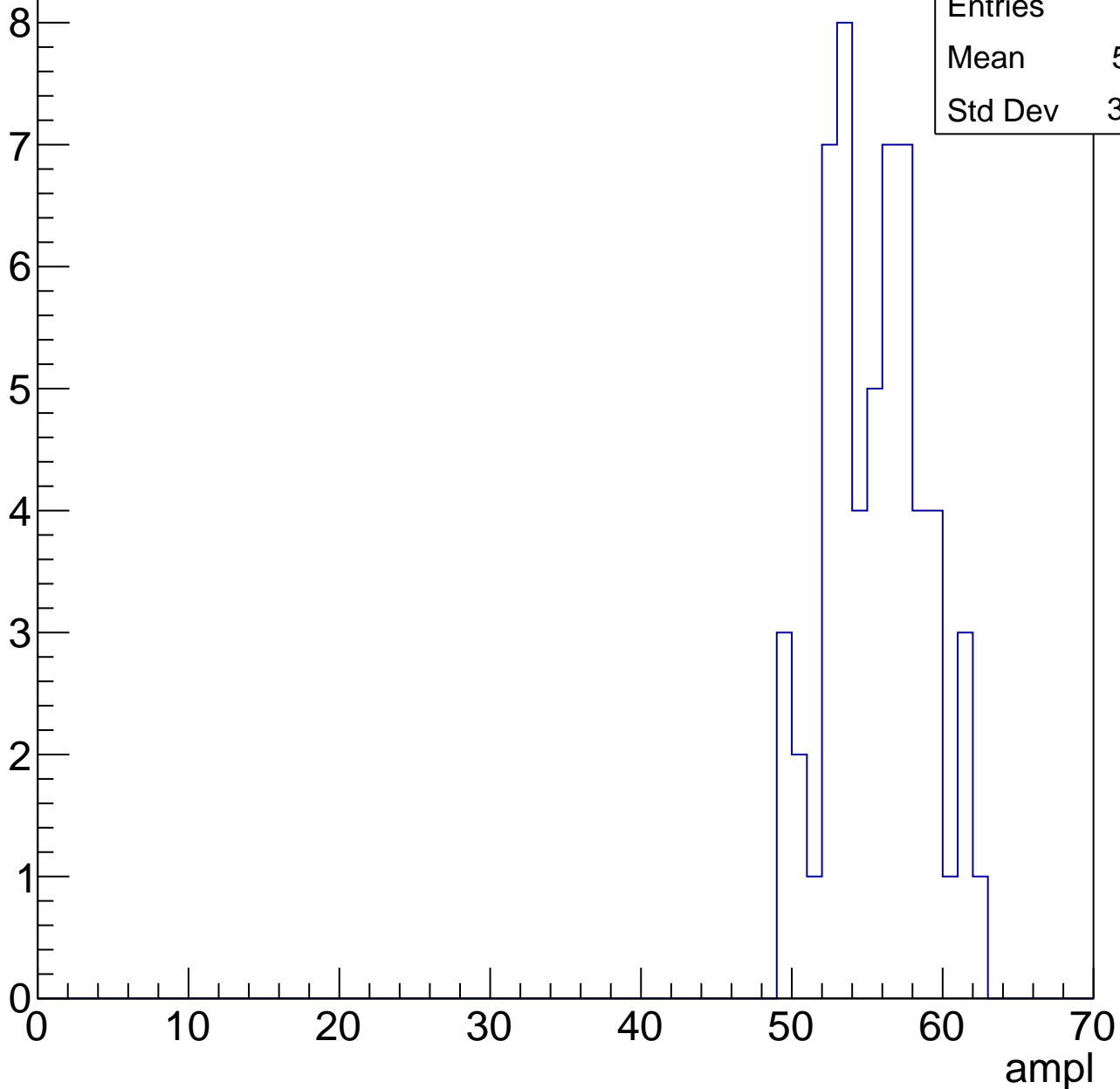


# B1L102S, U20-ch124, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	55.11
Std Dev	3.216

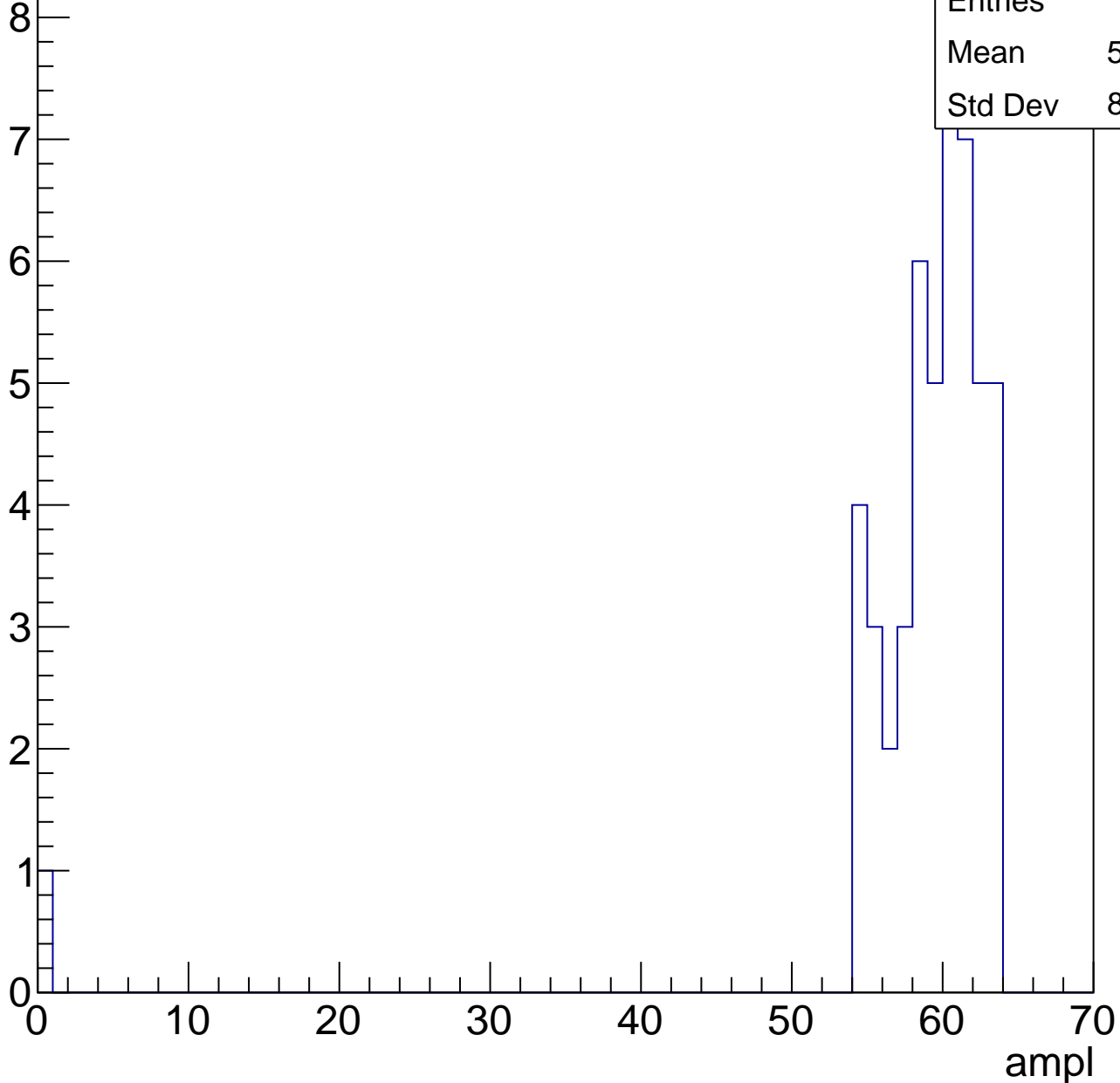


# B1L102S, U20-ch124, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

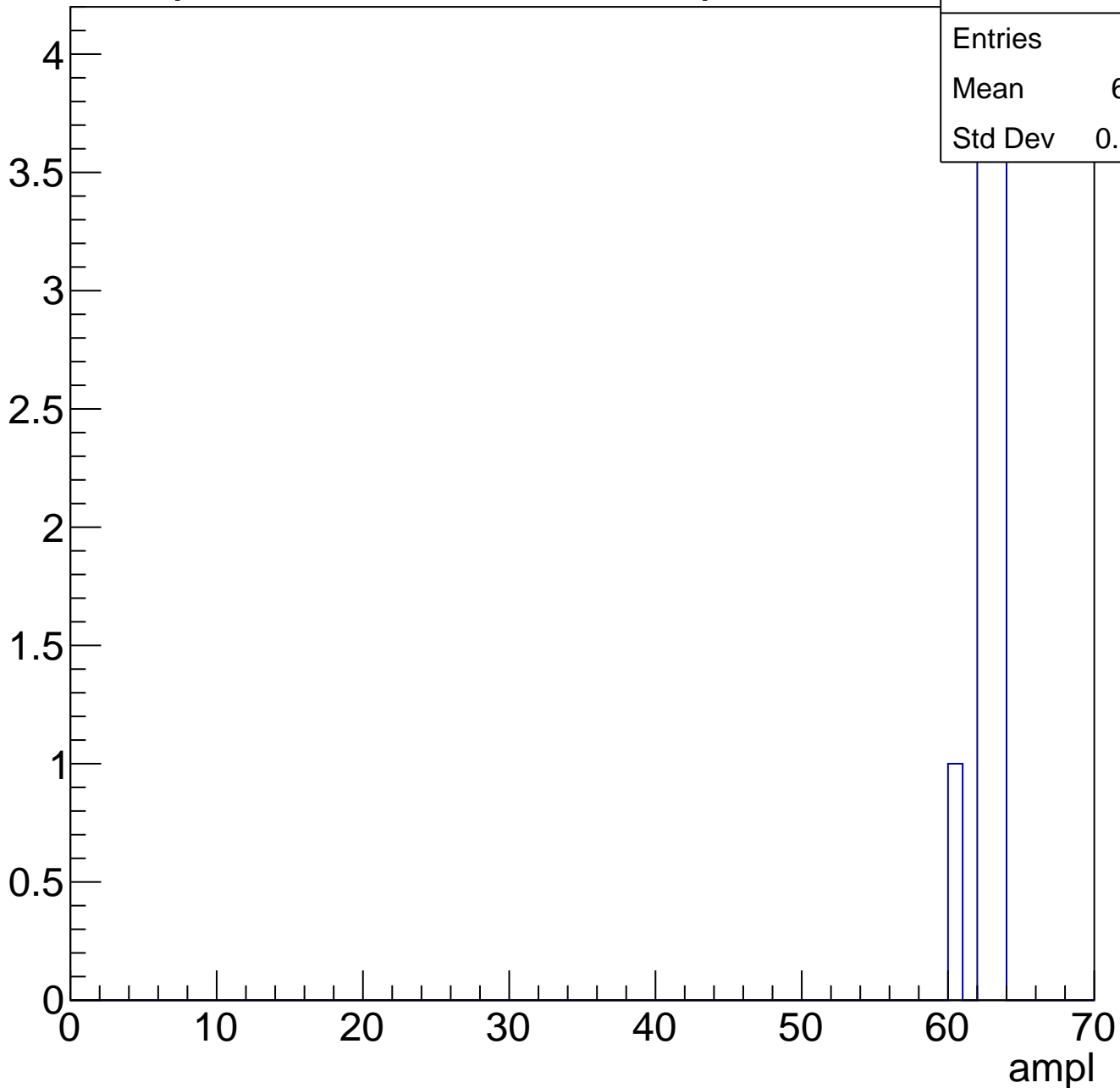
Entries	49
Mean	57.94
Std Dev	8.772



# B1L102S, U20-ch124, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

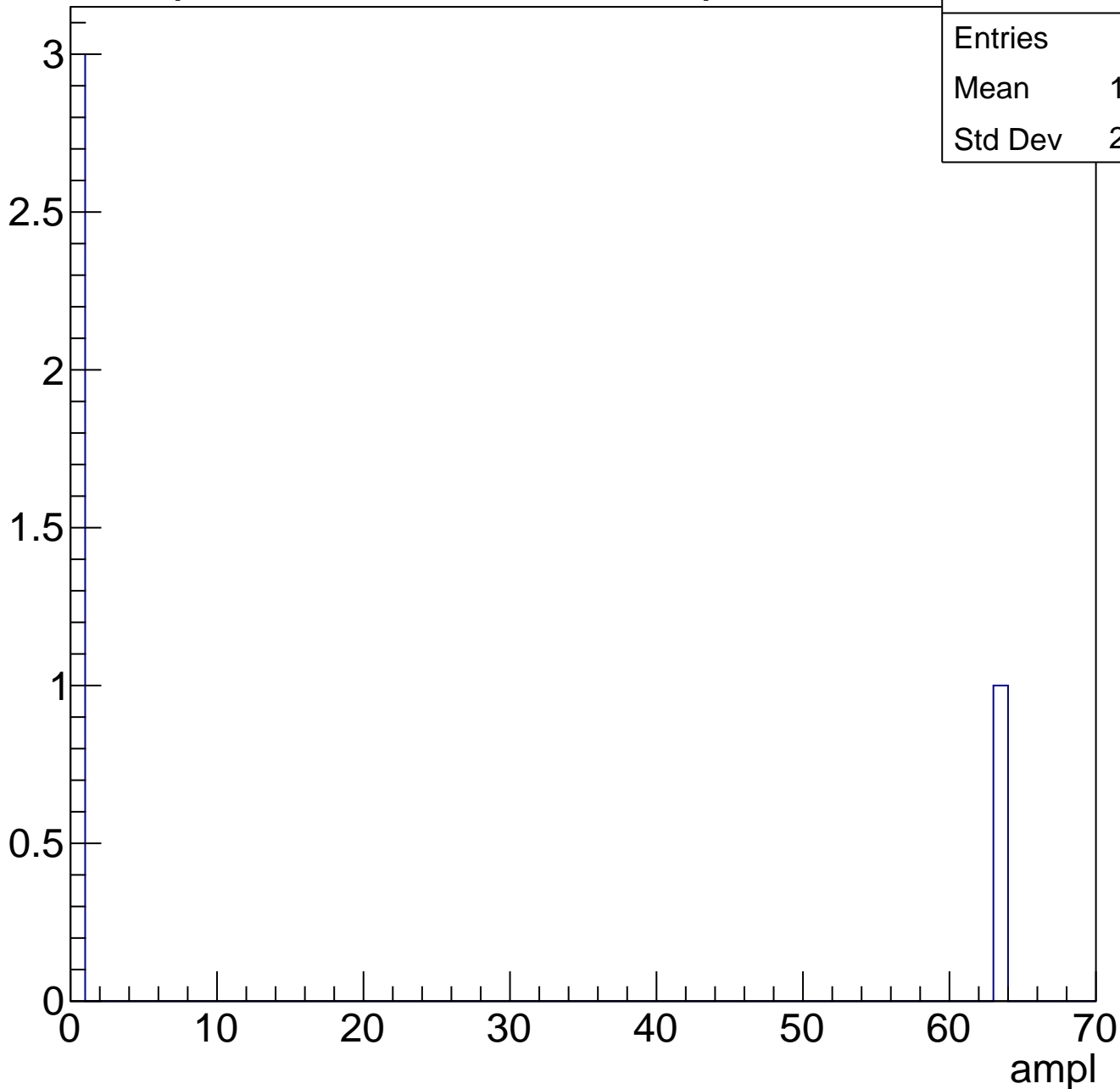




# B1L102S, U20-ch124, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U20-ch125, adc0

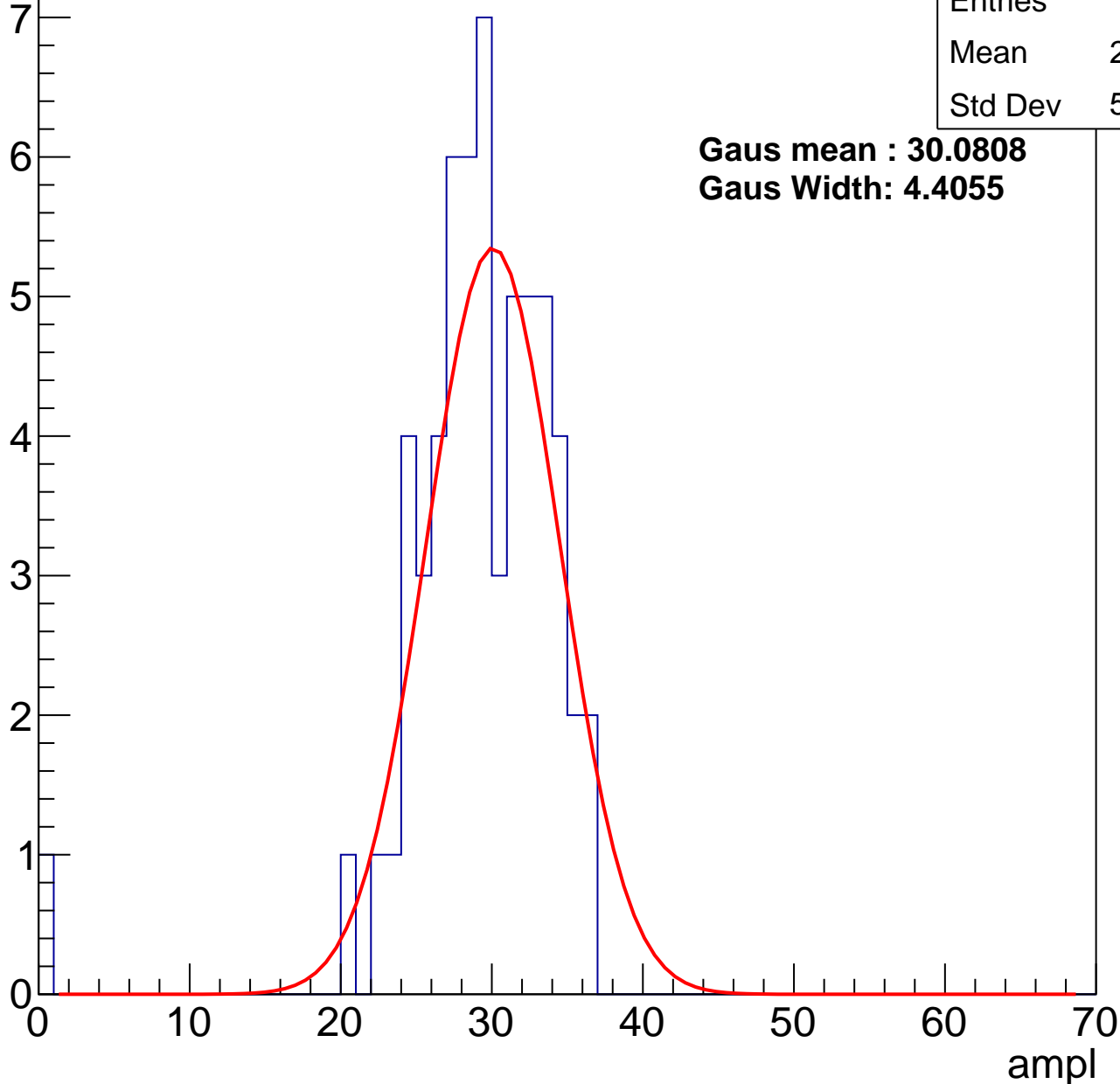
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	28.68
Std Dev	5.217

**Gaus mean : 30.0808**

**Gaus Width: 4.4055**



# B1L102S, U20-ch125, adc1

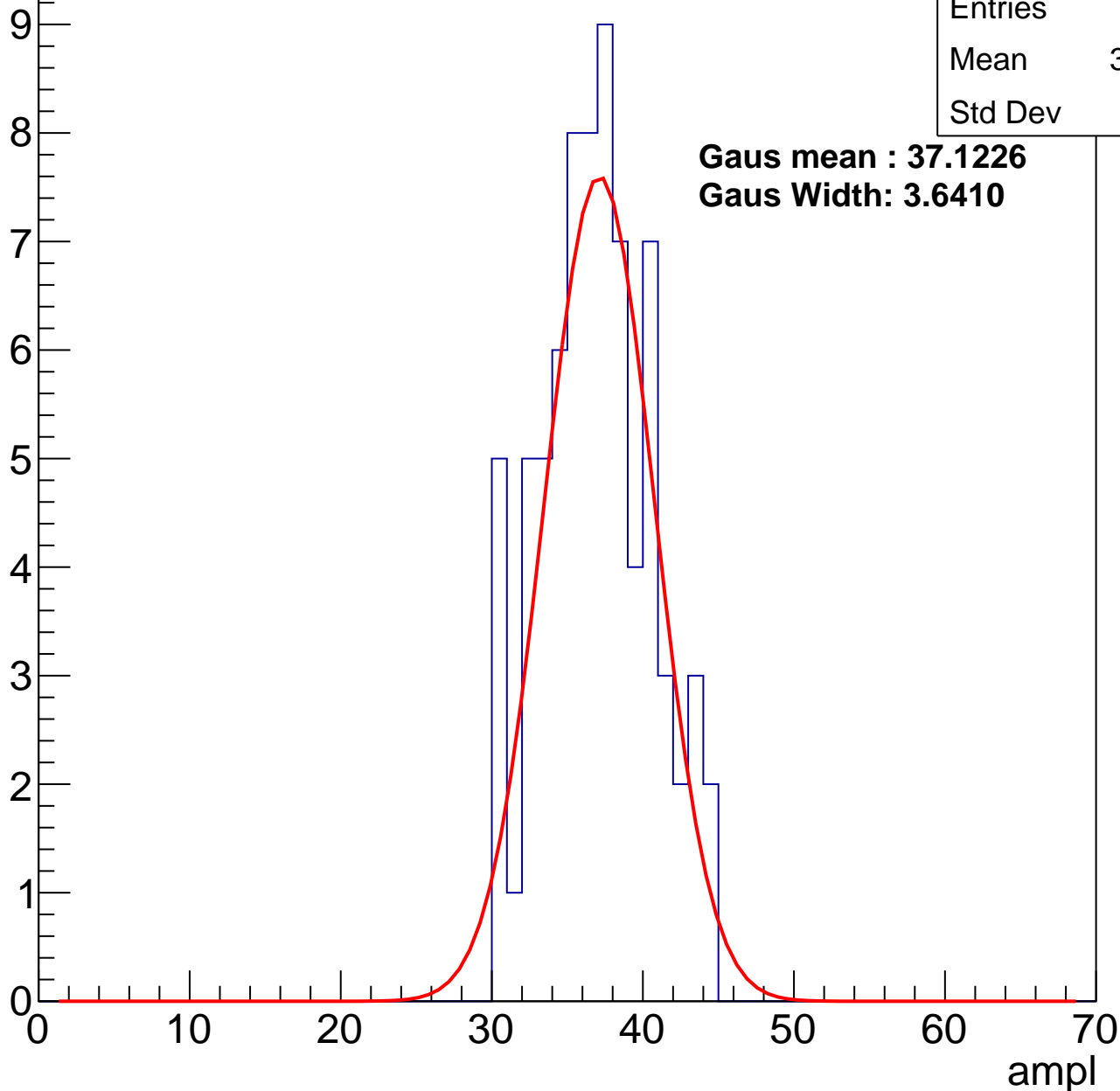
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	36.49
Std Dev	3.56

**Gaus mean : 37.1226**

**Gaus Width: 3.6410**



# B1L102S, U20-ch125, adc2

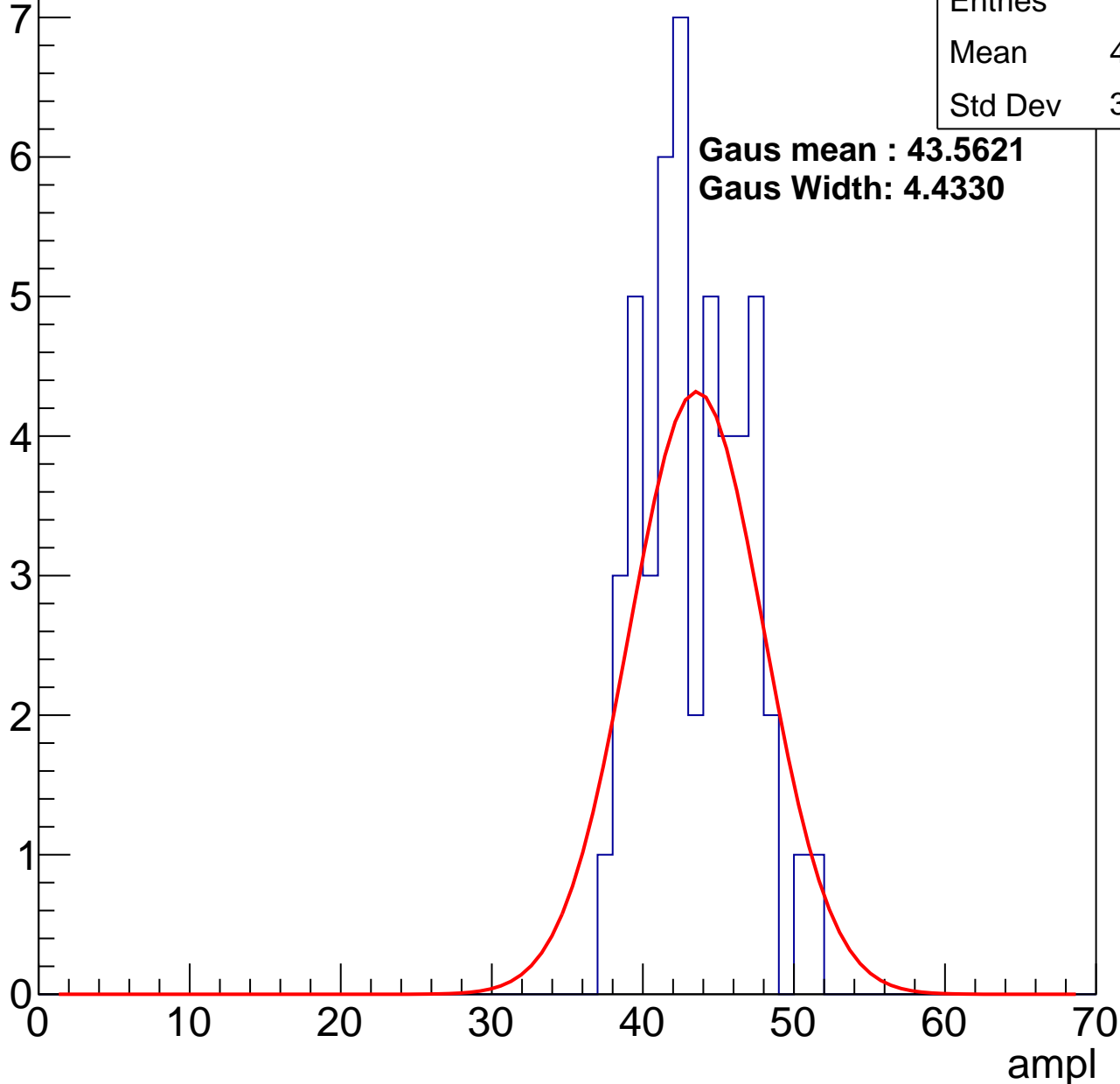
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	43.02
Std Dev	3.347

**Gaus mean : 43.5621**

**Gaus Width: 4.4330**

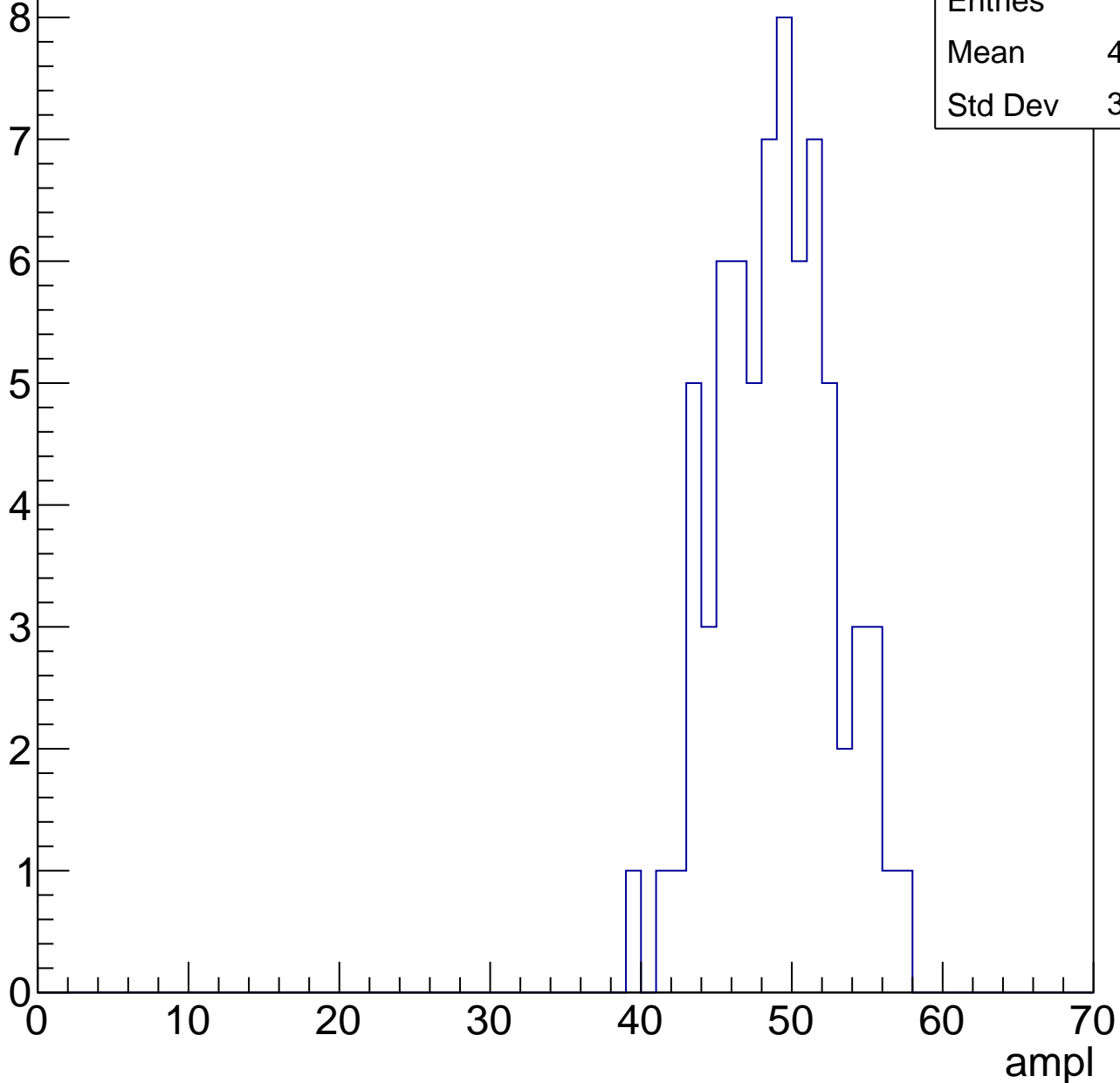


# B1L102S, U20-ch125, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	48.46
Std Dev	3.812

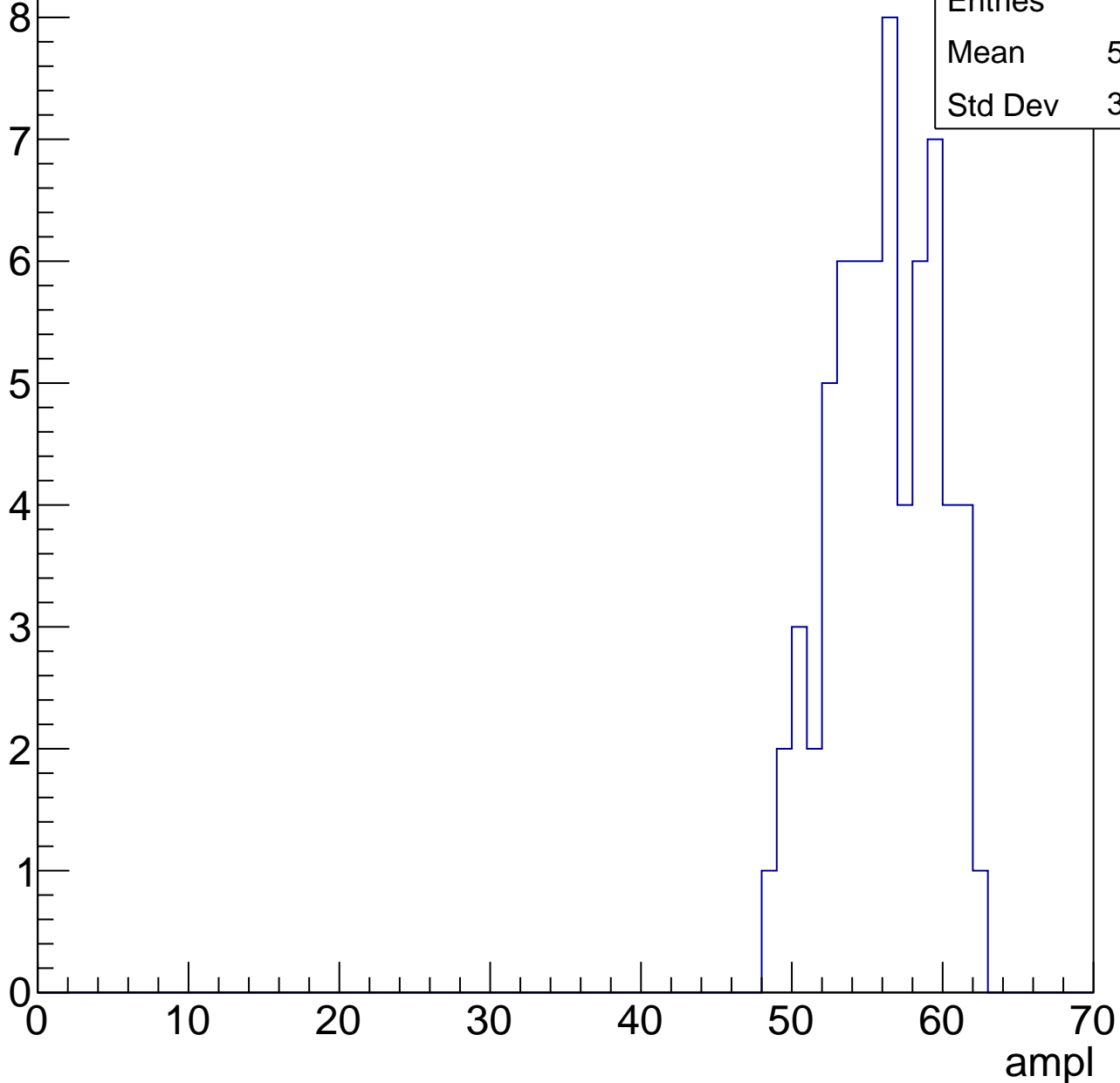


# B1L102S, U20-ch125, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	55.58
Std Dev	3.428

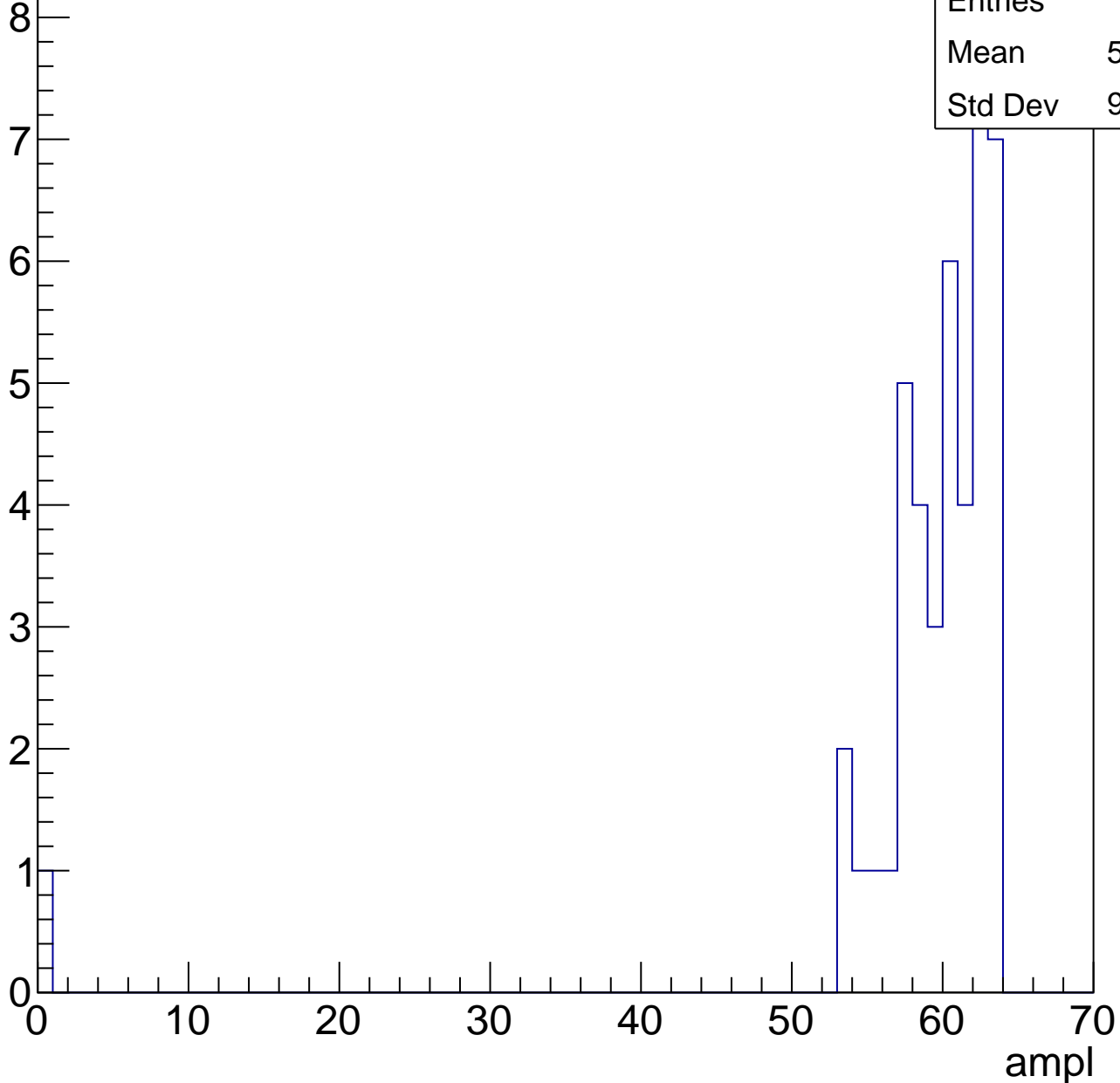


# B1L102S, U20-ch125, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	43
Mean	58.28
Std Dev	9.414



# B1L102S, U20-ch125, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U20-ch125, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

0

Mean

0

Std Dev

0

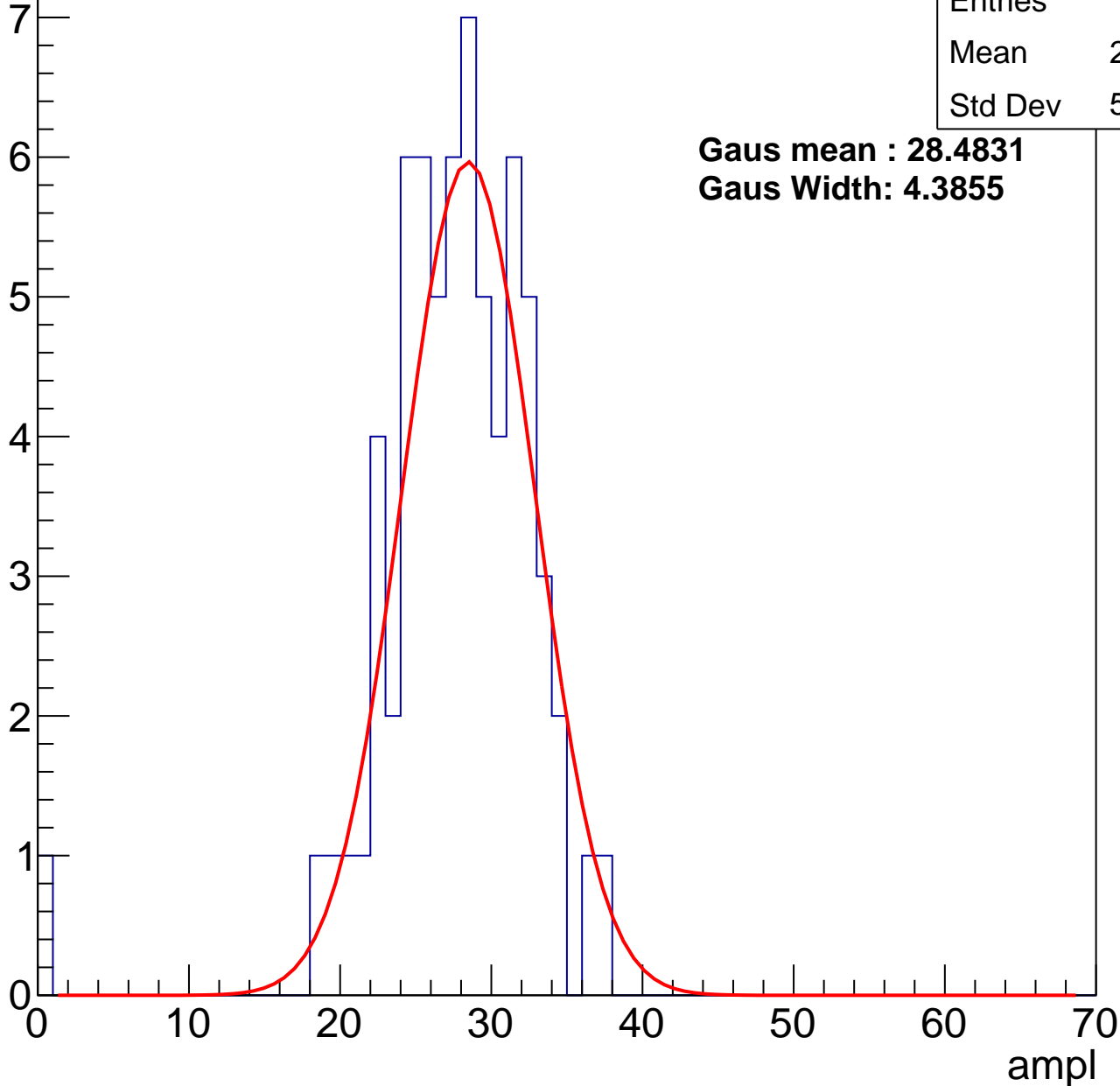
# B1L102S, U20-ch126, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	27.13
Std Dev	5.207

**Gaus mean : 28.4831**  
**Gaus Width: 4.3855**



# B1L102S, U20-ch126, adc1

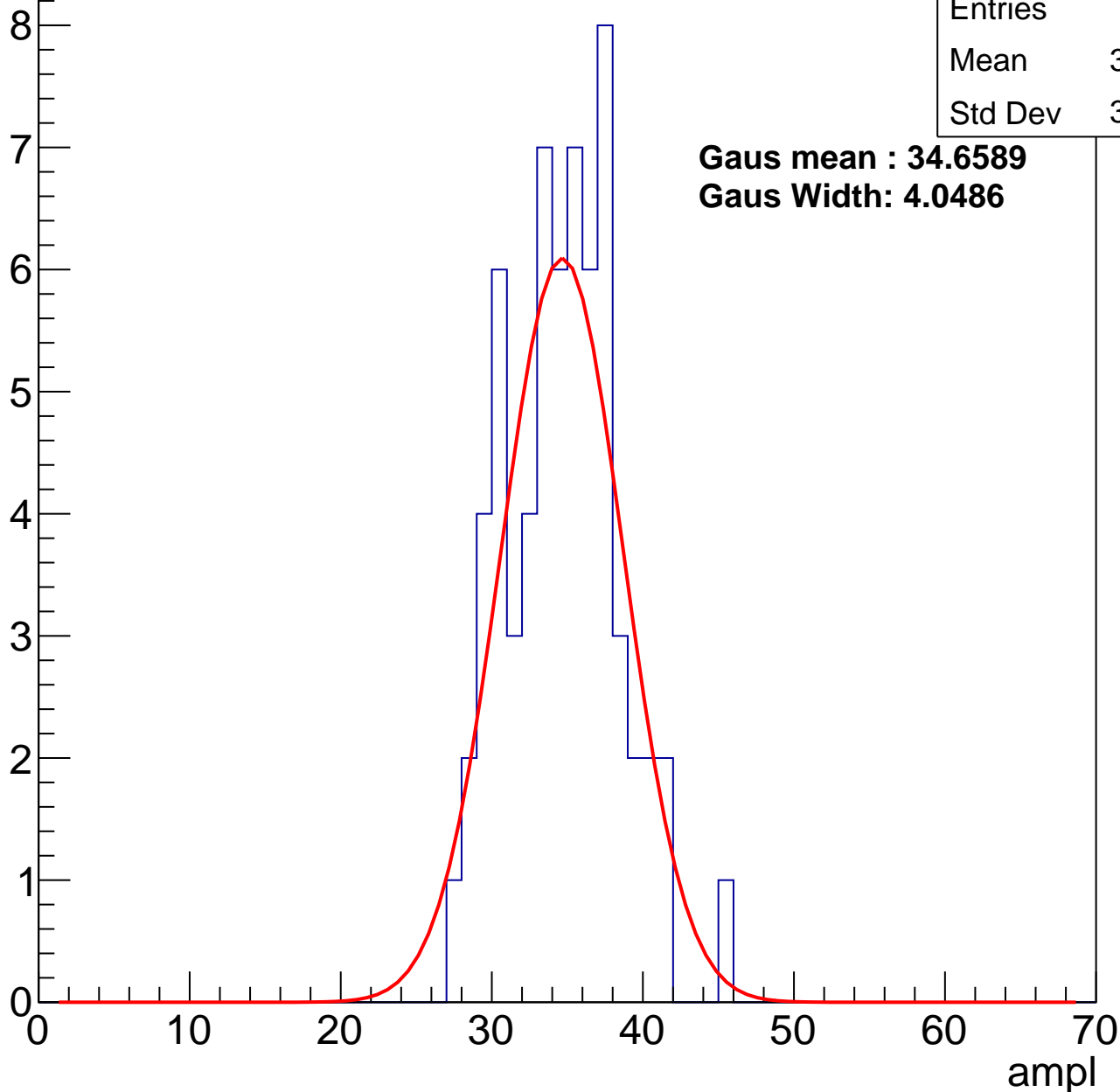
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	34.23
Std Dev	3.656

**Gaus mean : 34.6589**

**Gaus Width: 4.0486**



# B1L102S, U20-ch126, adc2

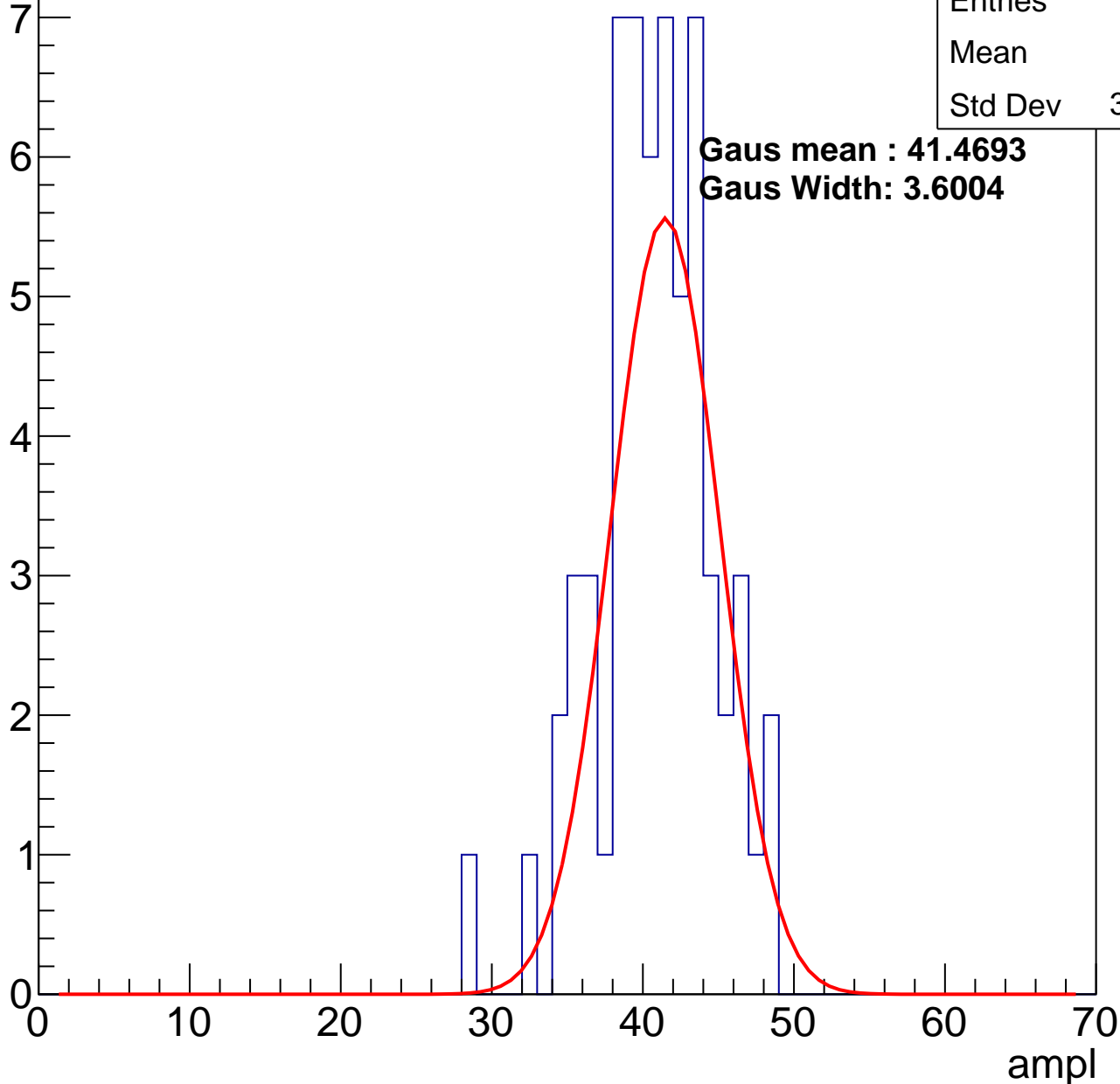
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	40.3
Std Dev	3.872

**Gaus mean : 41.4693**

**Gaus Width: 3.6004**

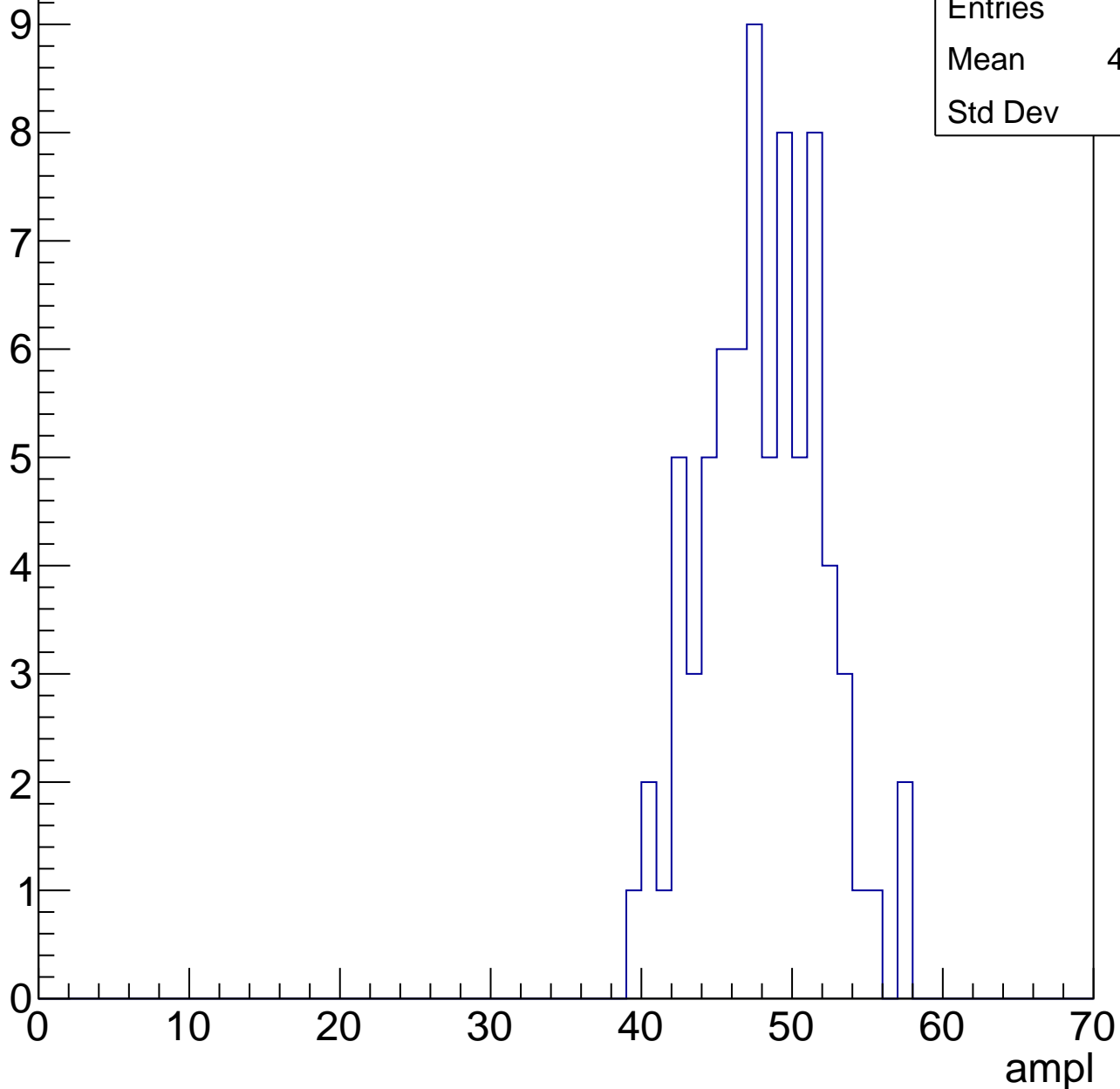


# B1L102S, U20-ch126, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	47.57
Std Dev	3.92

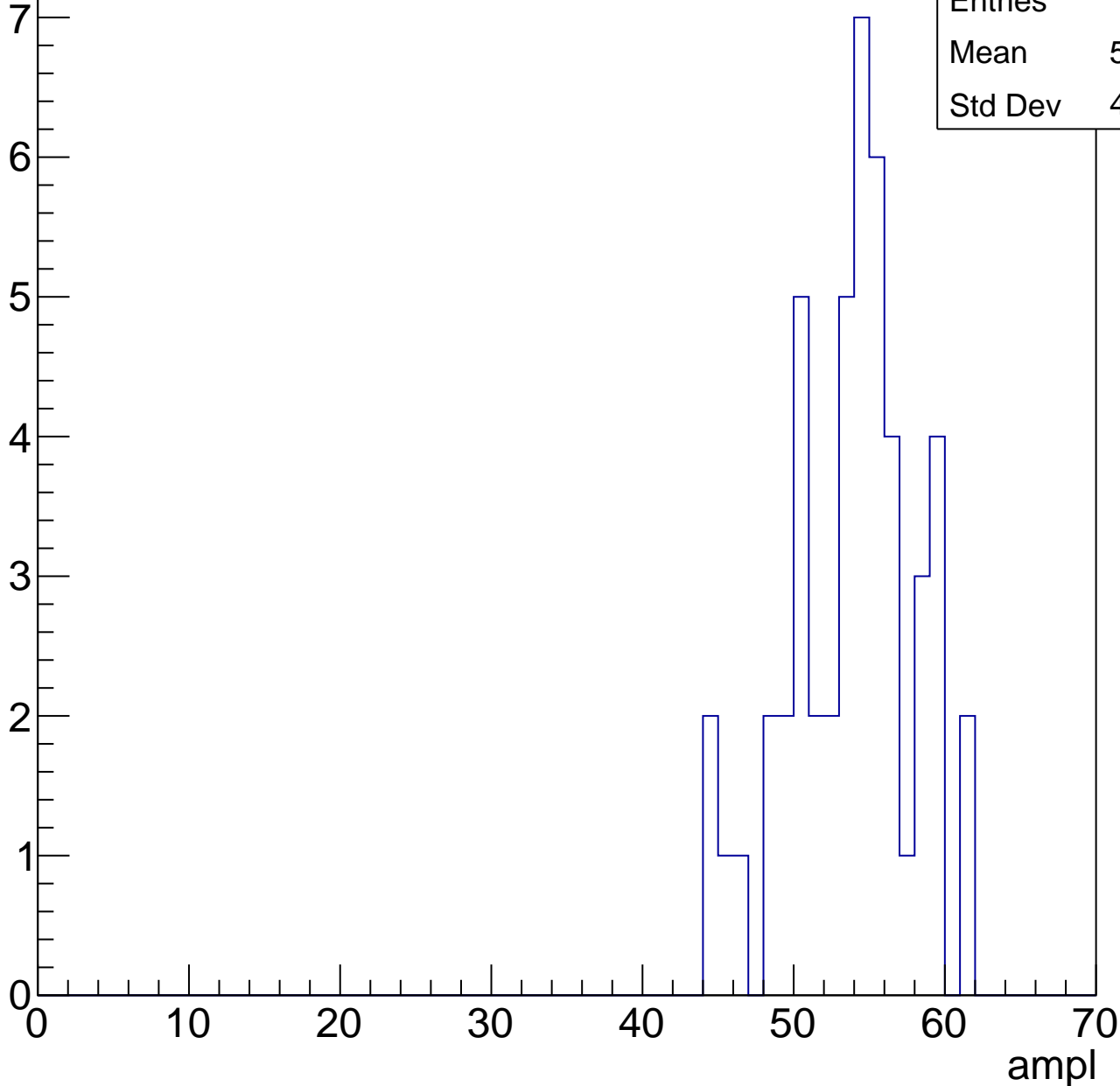


# B1L102S, U20-ch126, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	53.37
Std Dev	4.129

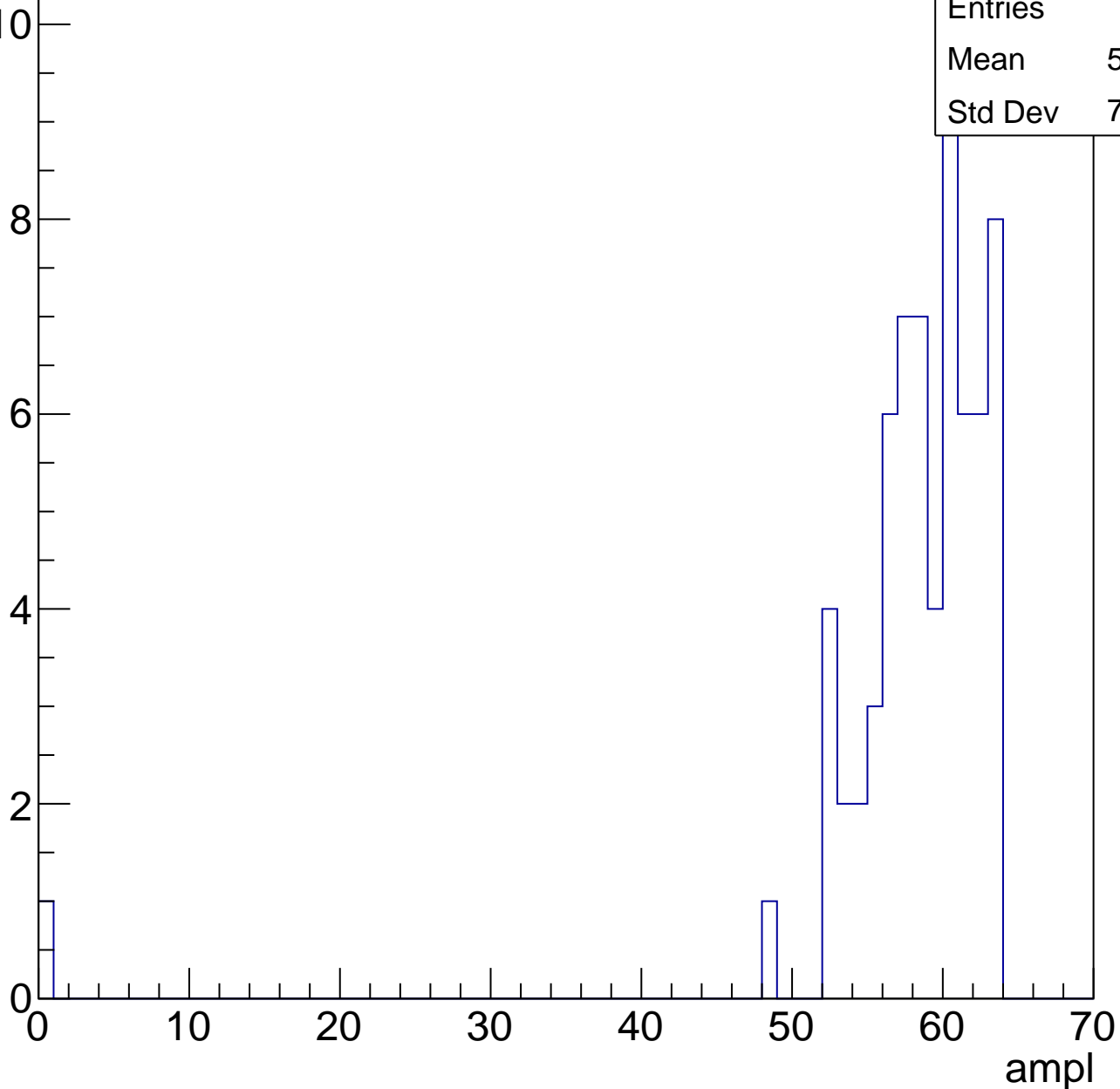


# B1L102S, U20-ch126, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

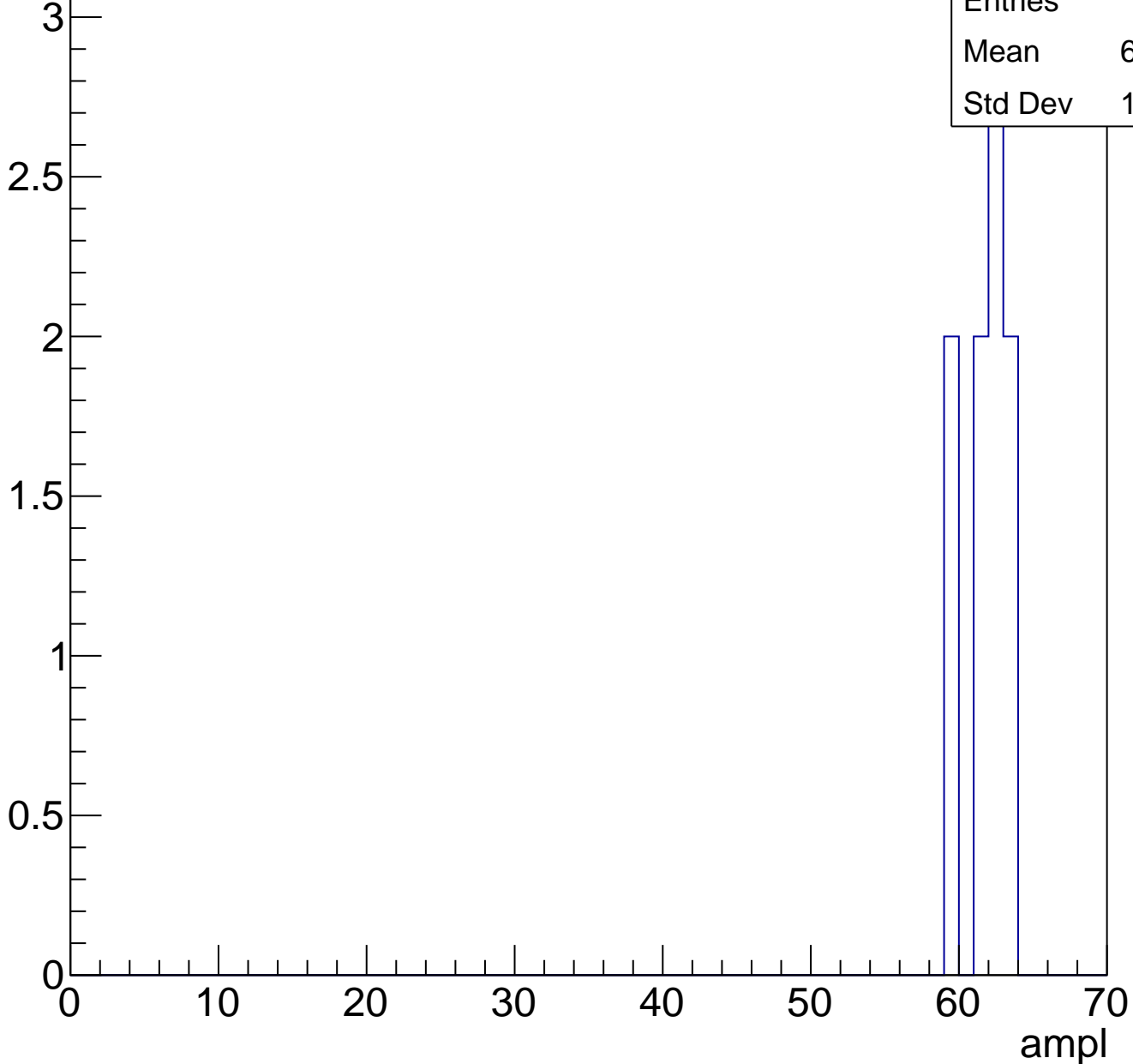
Entries	67
Mean	57.52
Std Dev	7.848



# B1L102S, U20-ch126, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

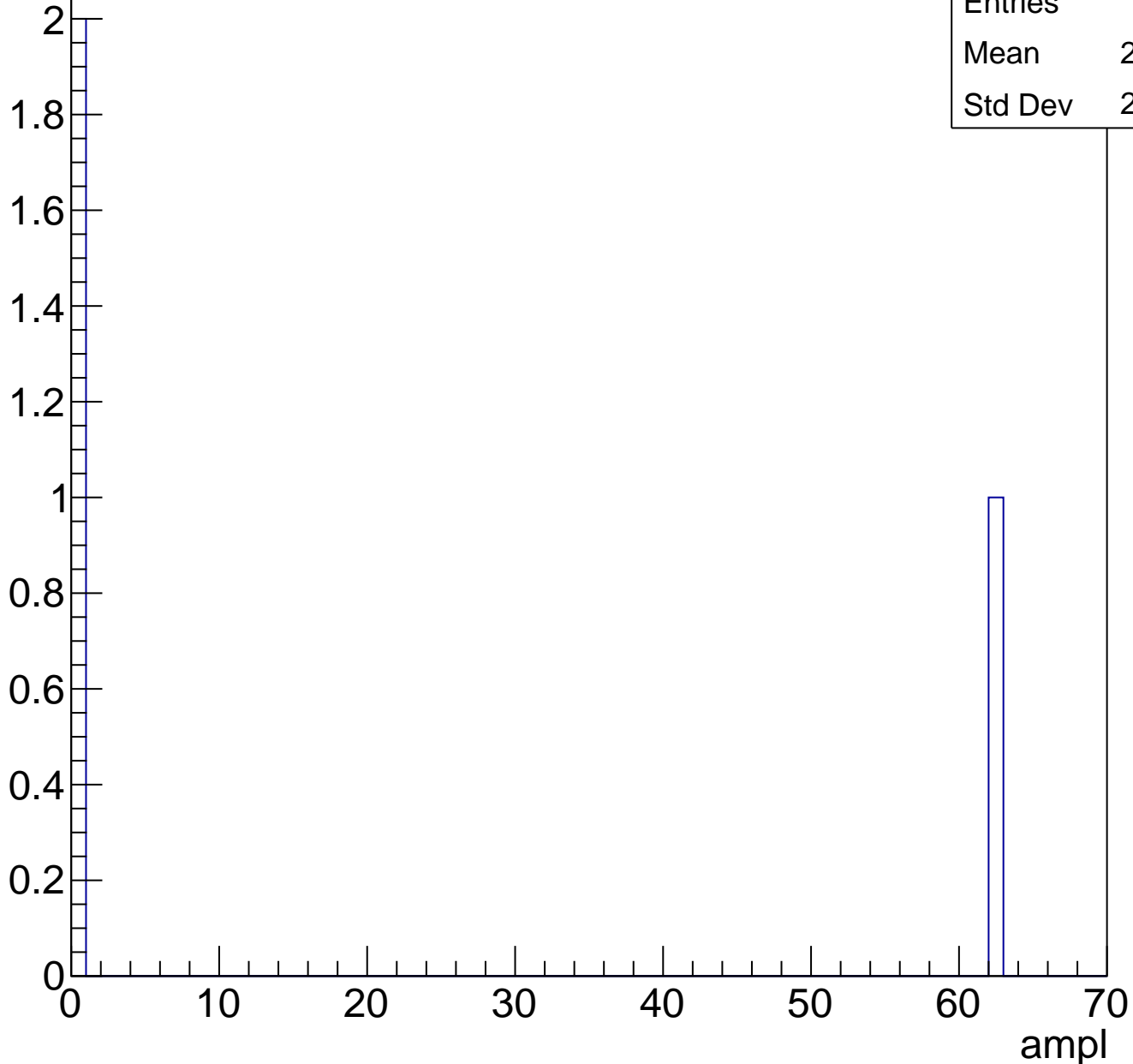




# B1L102S, U20-ch126, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	3
Mean	20.67
Std Dev	29.23

# B1L102S, U20-ch127, adc0

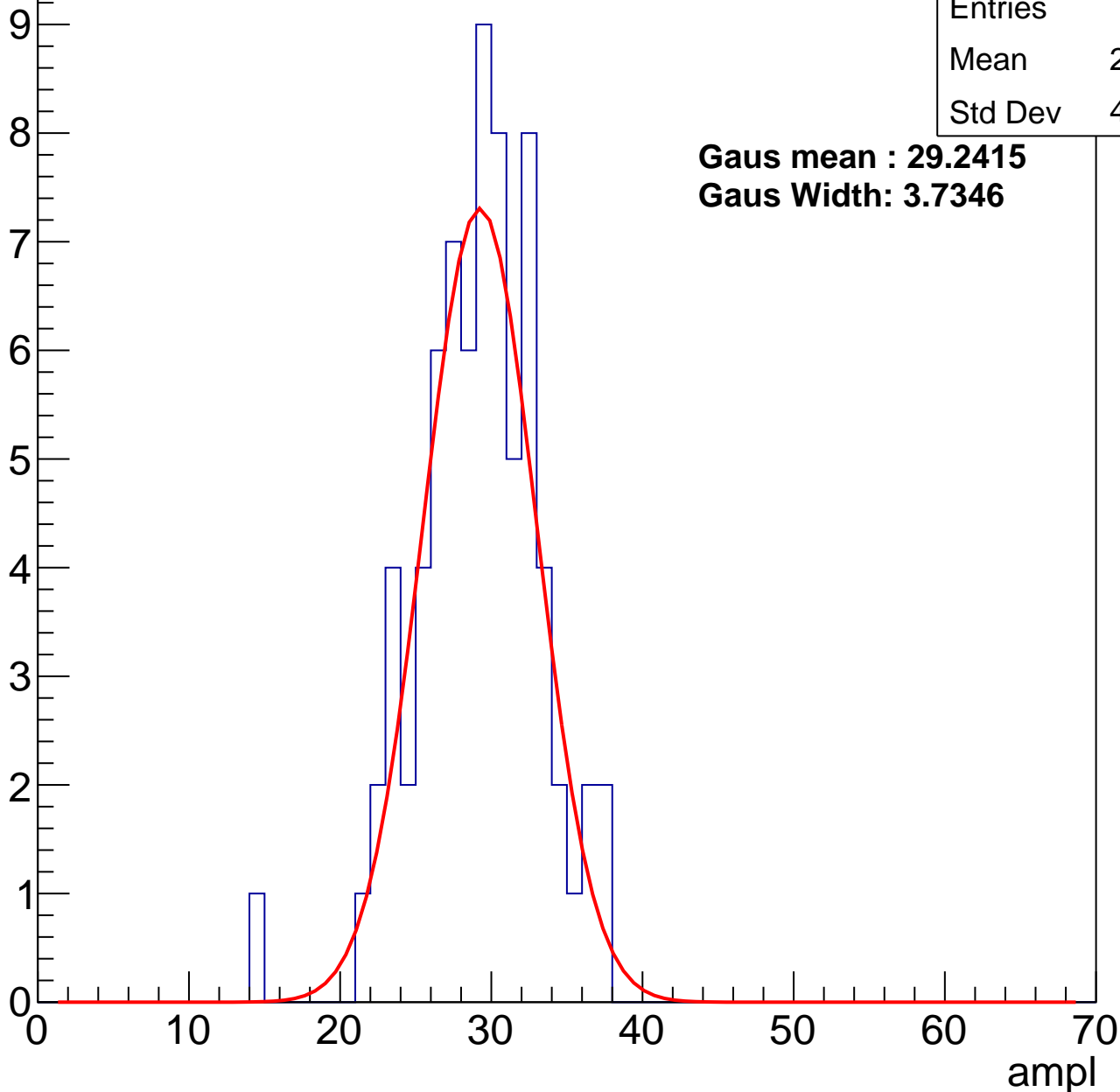
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	28.72
Std Dev	4.032

**Gaus mean : 29.2415**

**Gaus Width: 3.7346**



# B1L102S, U20-ch127, adc1

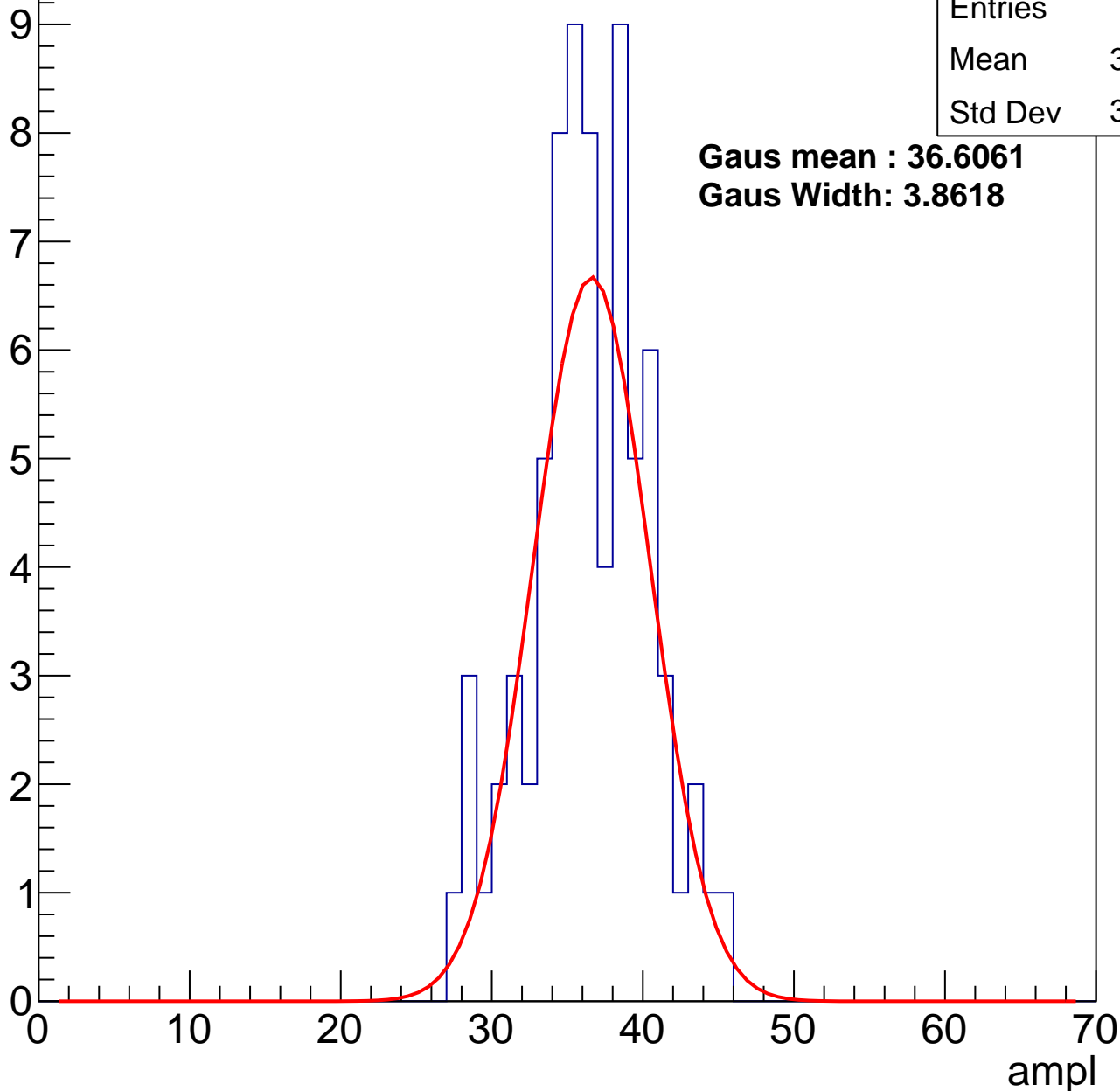
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	35.97
Std Dev	3.894

**Gaus mean : 36.6061**

**Gaus Width: 3.8618**



# B1L102S, U20-ch127, adc2

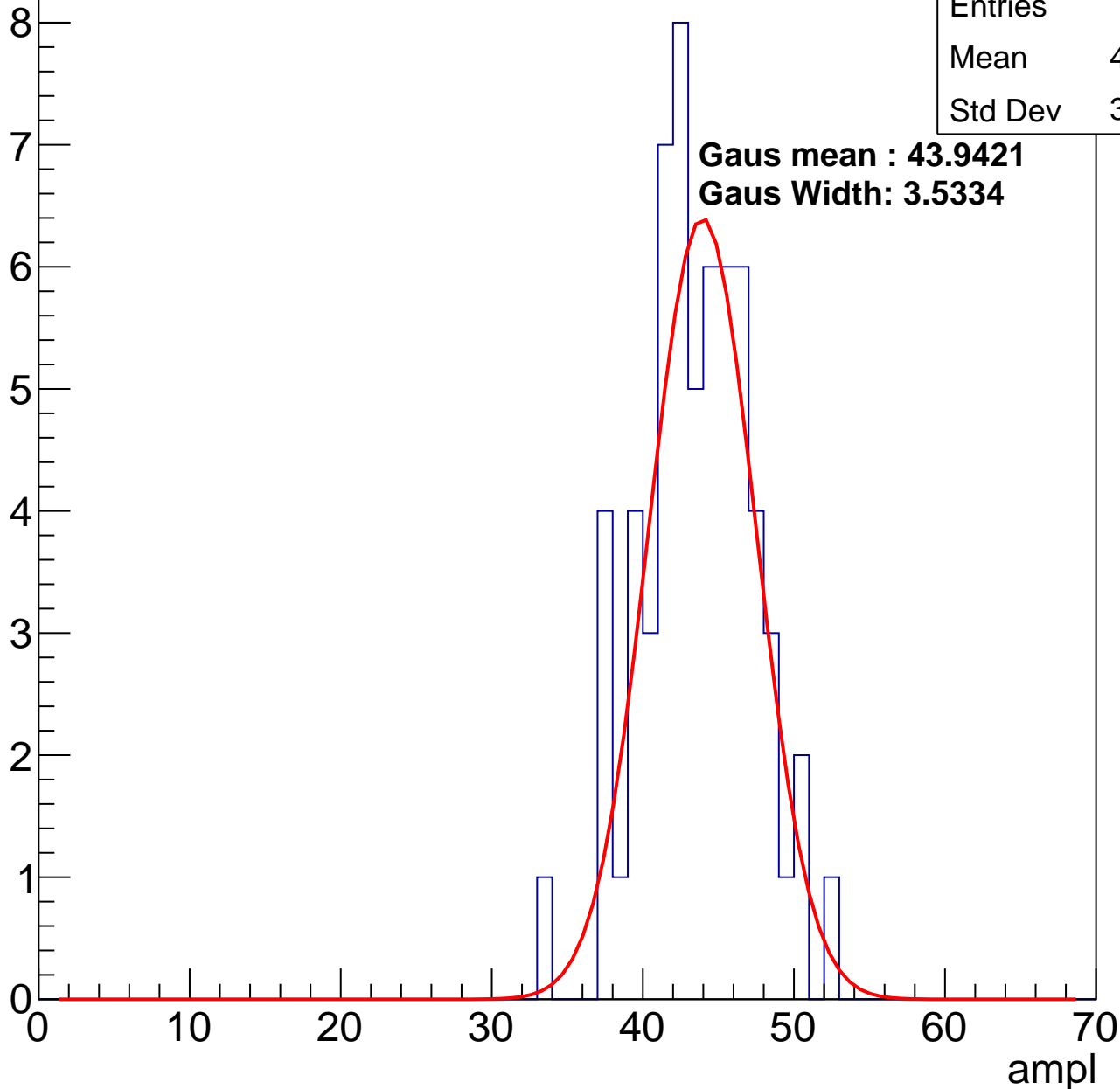
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	43.16
Std Dev	3.664

**Gaus mean : 43.9421**

**Gaus Width: 3.5334**

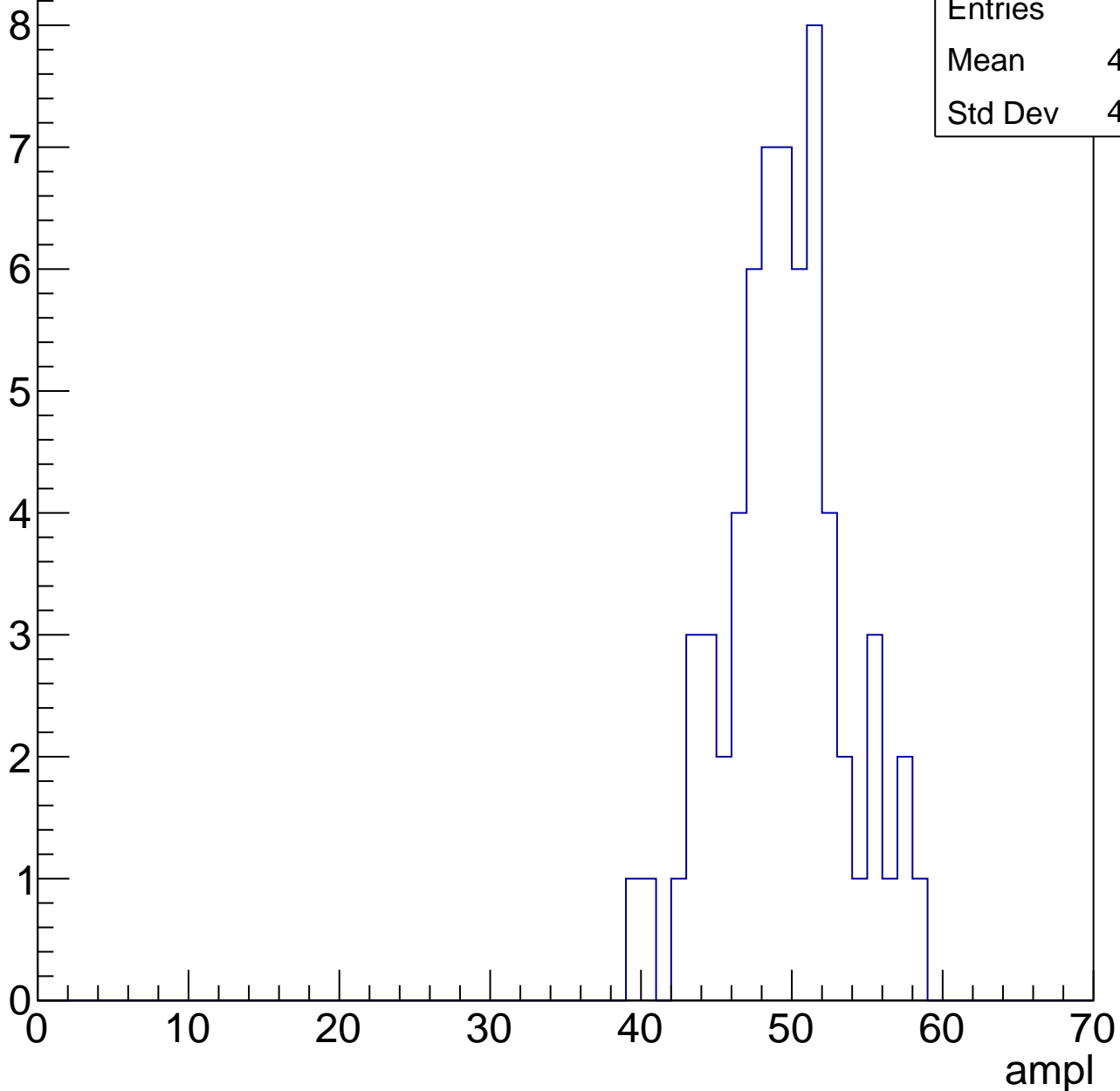


# B1L102S, U20-ch127, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	48.98
Std Dev	4.002

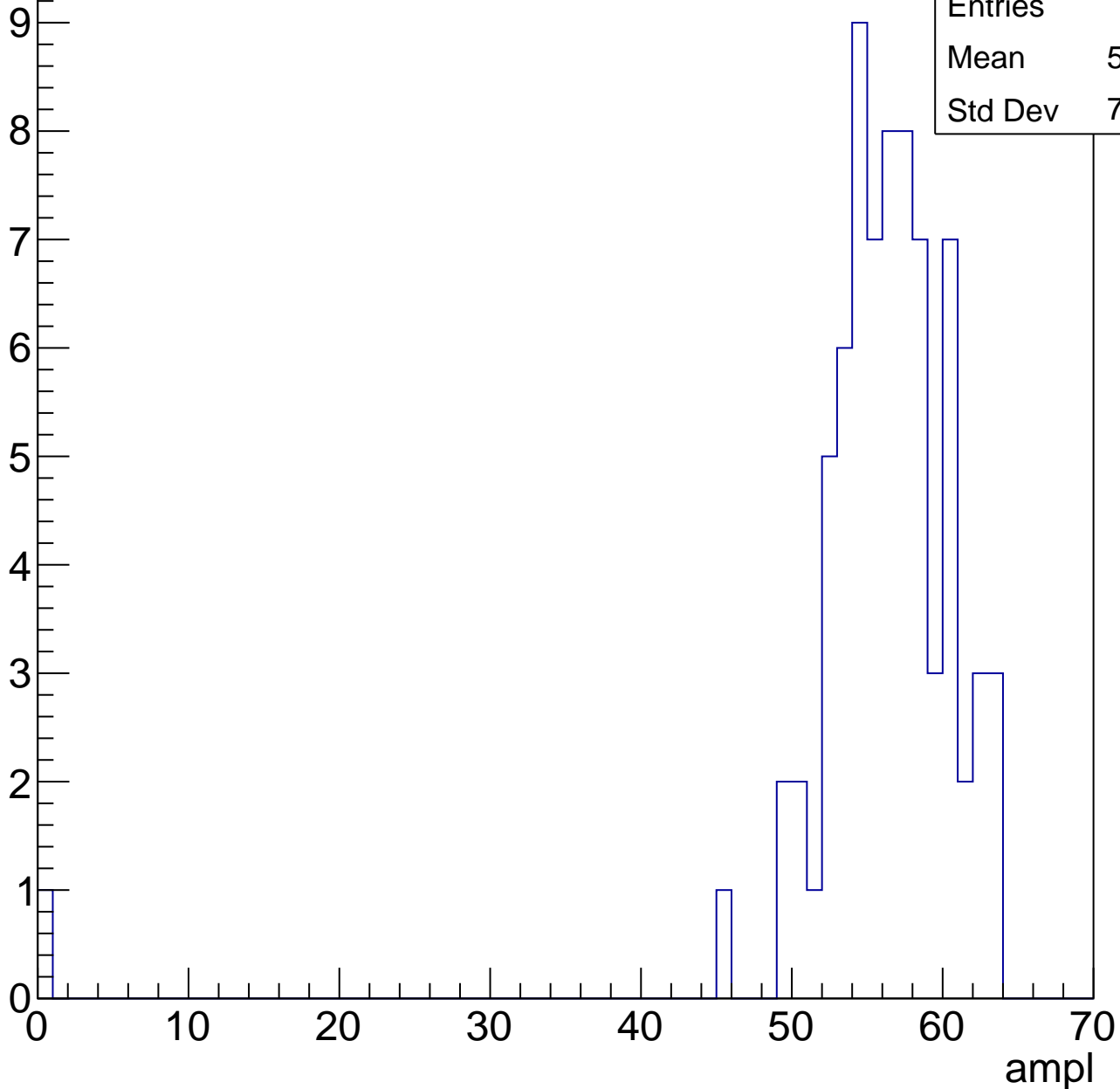


# B1L102S, U20-ch127, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	55.29
Std Dev	7.368

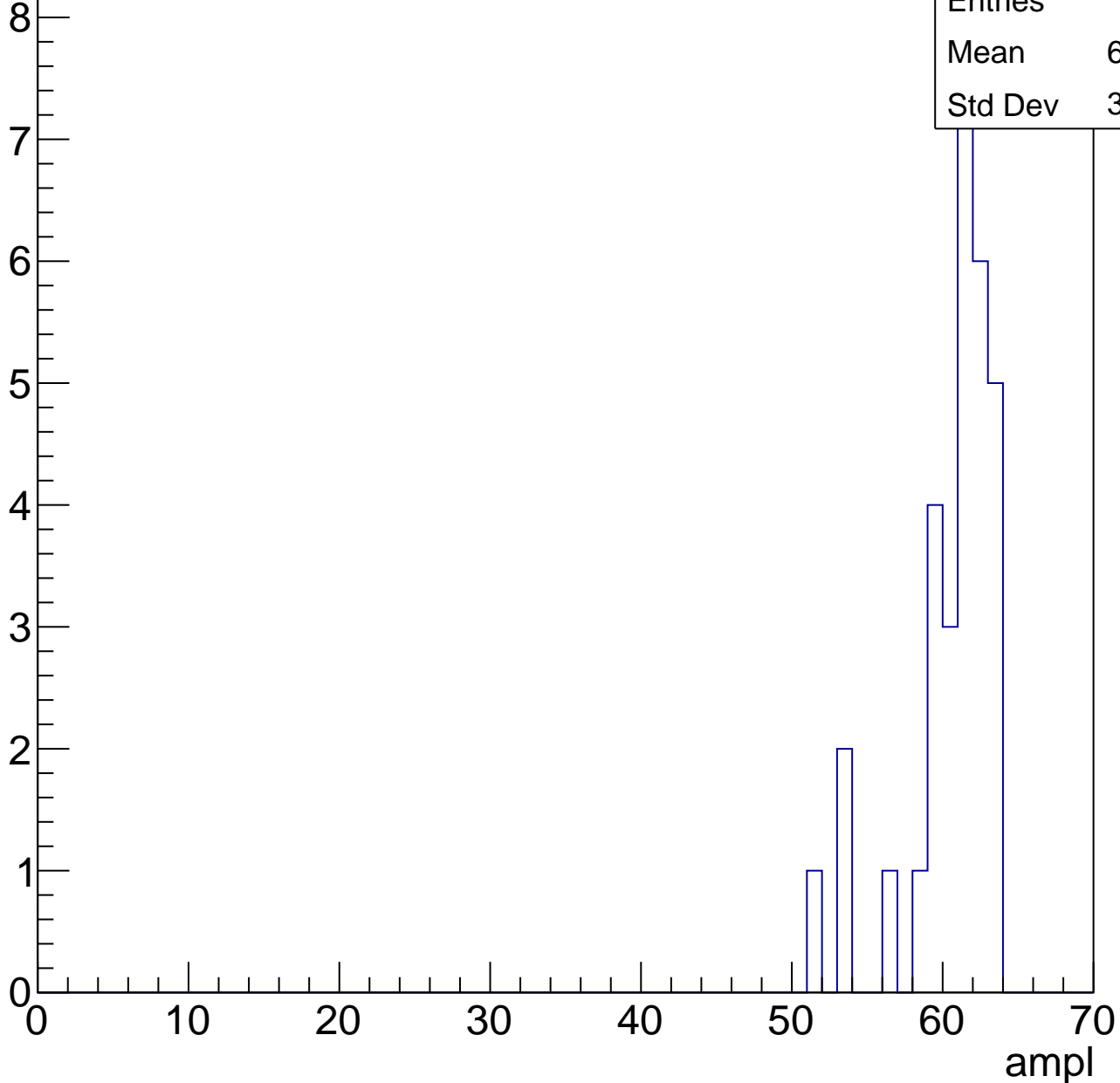


# B1L102S, U20-ch127, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

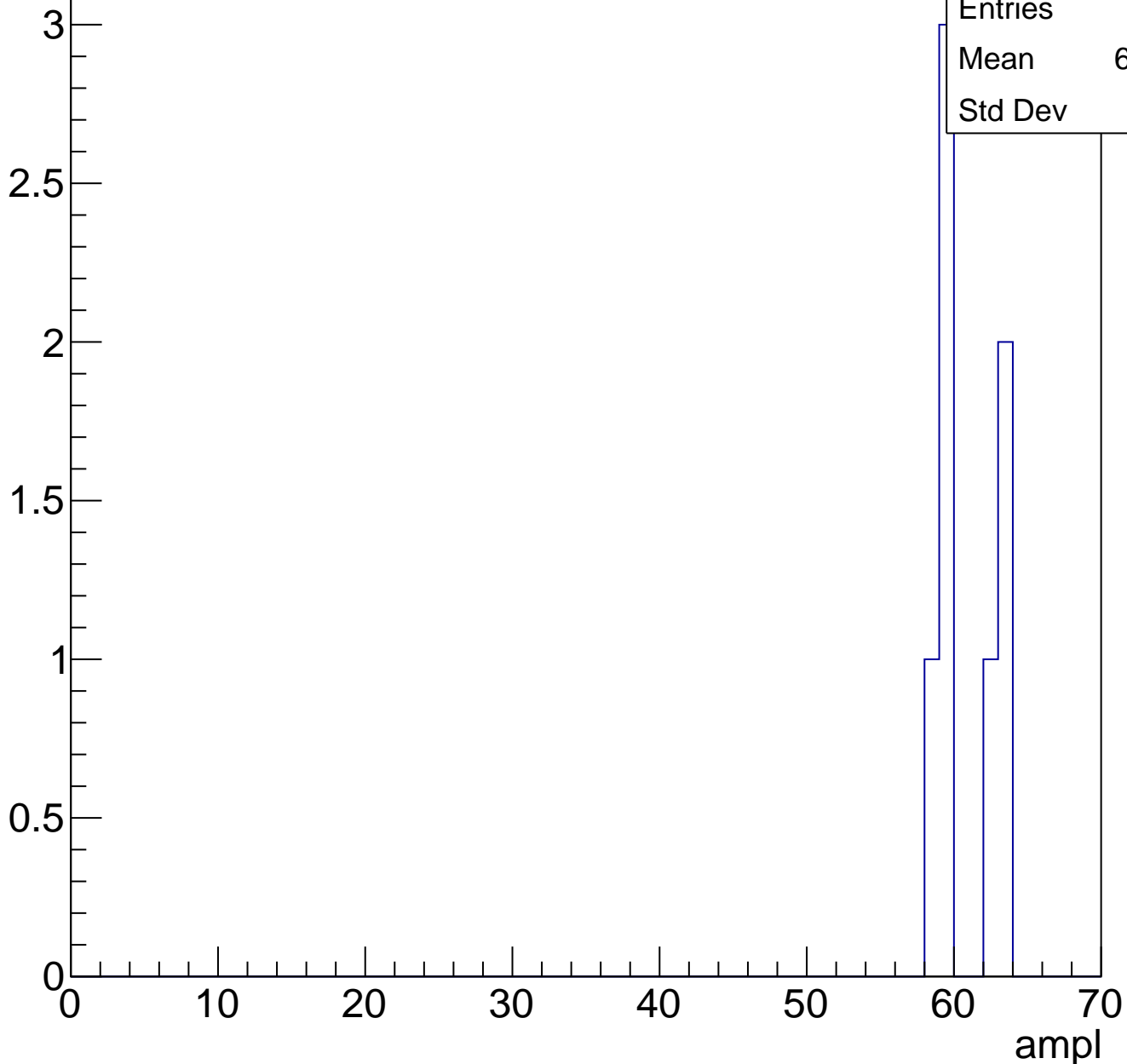
Entries	31
Mean	60.06
Std Dev	3.005



# B1L102S, U20-ch127, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

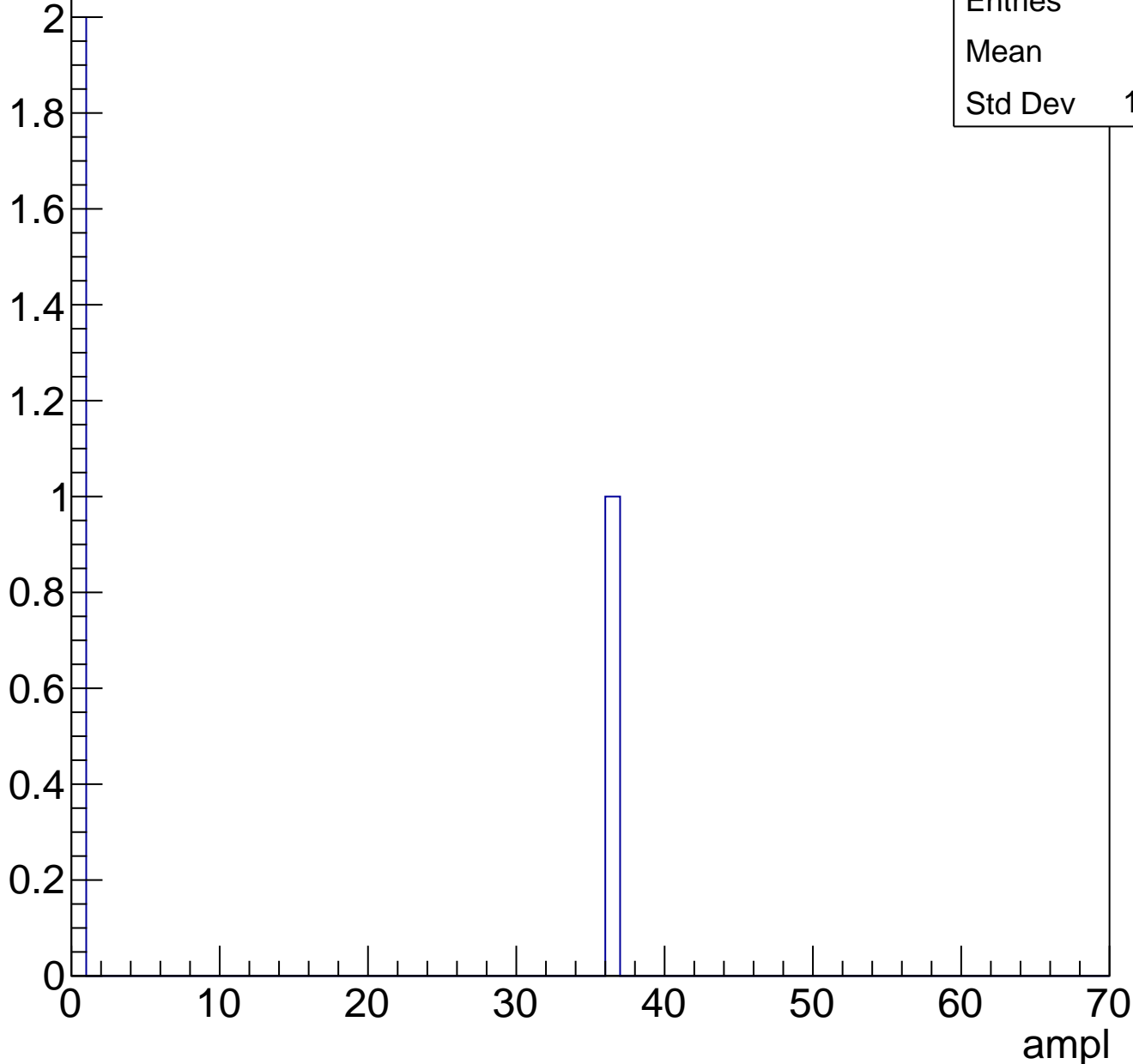




# B1L102S, U20-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

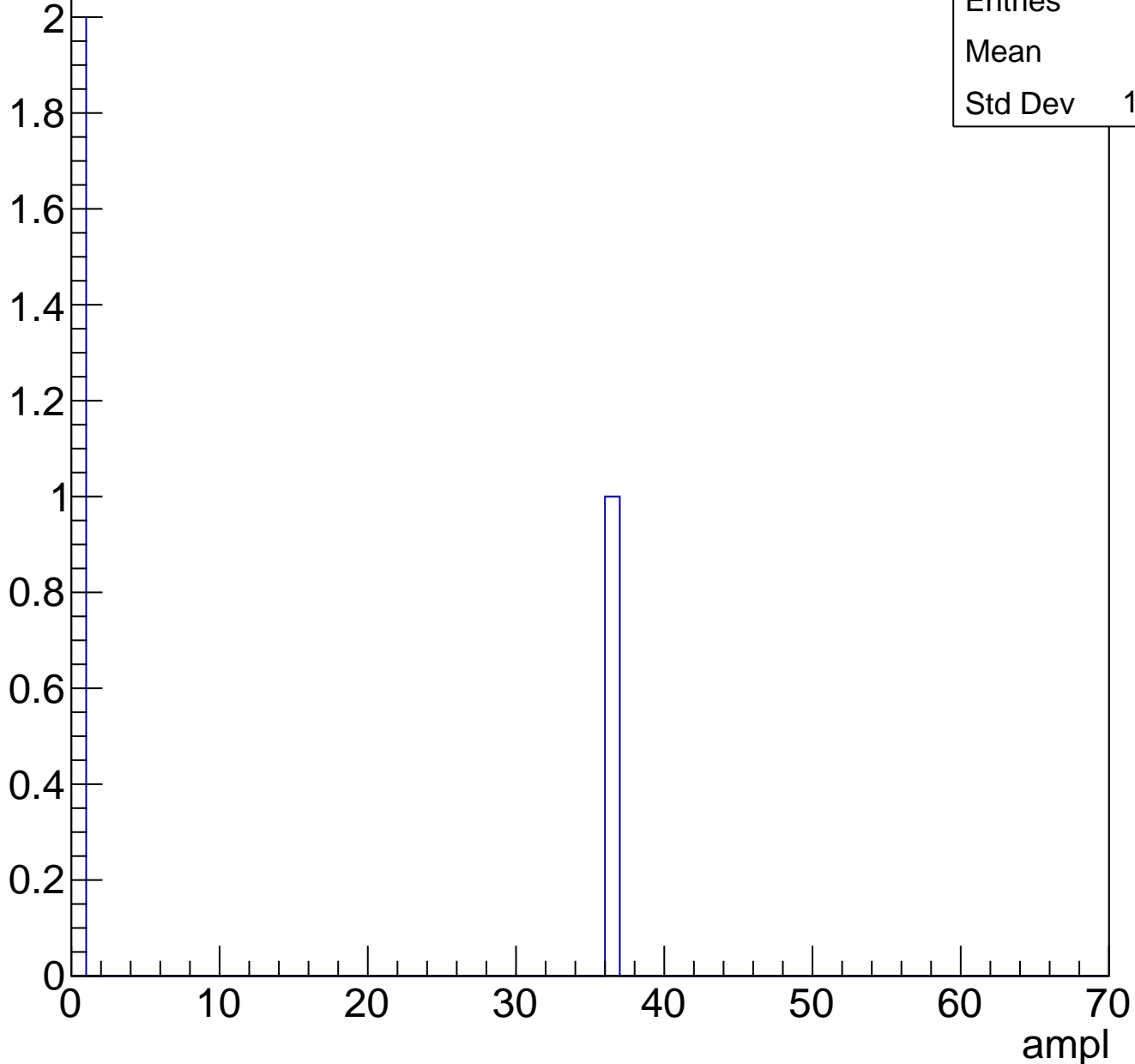


Entries	3
Mean	12
Std Dev	16.97

# B1L102S, U20-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	3
Mean	12
Std Dev	16.97