B1L101S, channel entry distribution (ampl > 54) calib_packv5_042523_0143.root, FC#0, port D2 **Entries** 3328 Mean 90.01 3000 Std Dev 0.1169 2500 2000 1500 1000 500

150

50

250

Channel entry

B1L002S, channel entry distribution (ampl > 54) calib_packv5_042523_0143.root, FC#10, port B3 **Entries** 3328 Mean 90.01 3000 Std Dev 0.09295 2500 2000 1500 1000 500

150

50

250

Channel entry

B1L102S, channel entry distribution (ampl > 54) calib_packv5_042523_0143.root, FC#11, port A2 **Entries** 3328 Mean 90.01 3000 Std Dev 0.07534 2500 2000 1500 1000 500

150

50

250

Channel entry

calib_packv5_042523_0143.root, FC#12, port B1 **Entries** 3328 Mean 90.03 3000 Std Dev 0.2147 2500 2000 1500 1000 500 100 250 50 150 200

Channel entry

B0L102S, channel entry distribution (ampl > 54)

B1L003S, channel entry distribution (ampl > 54) calib_packv5_042523_0143.root, FC#13, port D2 **Entries** 3328 Mean 86.54 3000 Std Dev 17.31 2500 2000 1500 1000 500

150

50

250

Channel entry

calib_packv5_042523_0143.root, FC#1, port C1 **Entries** Mean 90.11 Std Dev 90.05

Channel entry

B0L101S, channel entry distribution (ampl > 54)

B1L001S, channel entry distribution (ampl > 54) calib_packv5_042523_0143.root, FC#2, port C2 **Entries** Mean 90.01 Std Dev 90.01 Channel entry

B1L000S, channel entry distribution (ampl > 54) calib_packv5_042523_0143.root, FC#3, port B3 **Entries** 3328 Mean 90.01 3000 Std Dev 0.08976 2500 2000 1500 1000 500

150

50

250

Channel entry

B1L100S, channel entry distribution (ampl > 54) calib_packv5_042523_0143.root, FC#4, port A2 **Entries** 3328 Mean 90.01 3000 Std Dev 0.07334 2500 2000 1500 1000 500

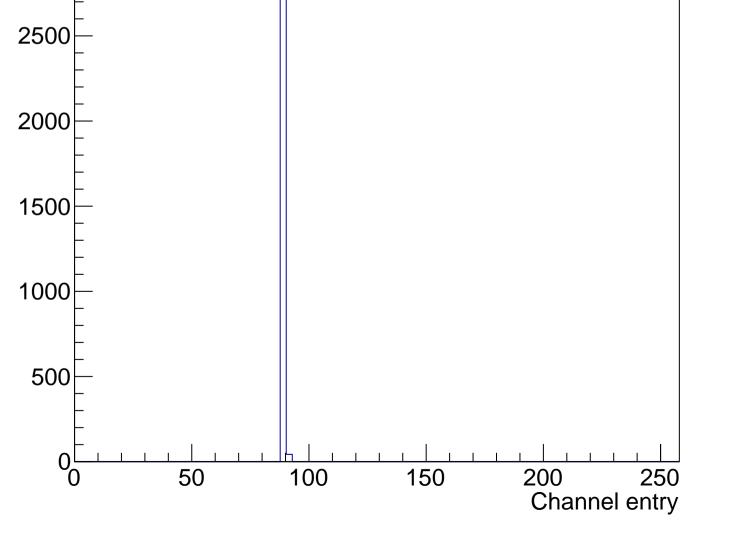
150

50

250

Channel entry

B0L000S, channel entry distribution (ampl > 54) calib_packv5_042523_0143.root, FC#5, port B1 **Entries** 3328 Mean 89.99 3000 Std Dev 1.565 2500 2000 1500 1000



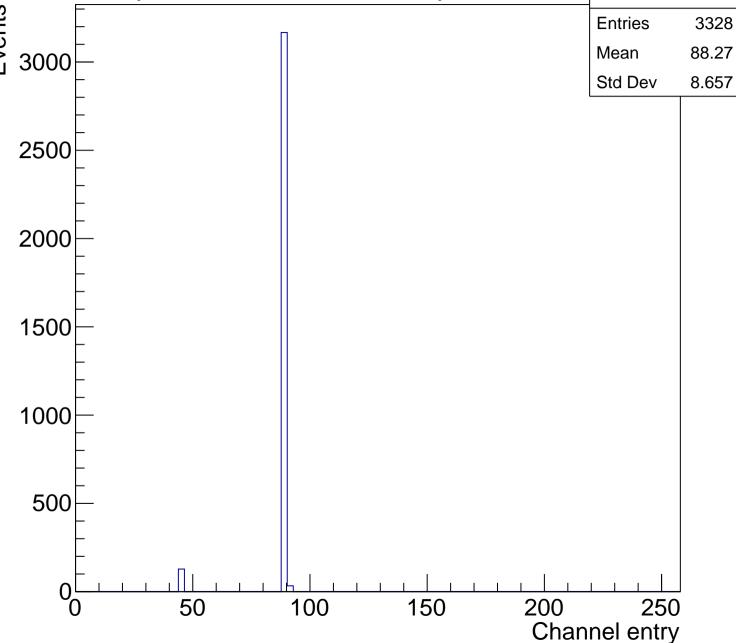
calib_packv5_042523_0143.root, FC#6, port A1 **Entries** 3328 0.4524 Mean 3000 5.413 Std Dev 2500 2000 1500 1000 500 100 250 50 150 200 Channel entry

B0L100S, channel entry distribution (ampl > 54)

B1L103S, channel entry distribution (ampl > 54)

calib_packv5_042523_0143.root, FC#7, port C2

Entrie



calib_packv5_042523_0143.root, FC#8, port C1 **Entries** Mean Std Dev 0.04897

Channel entry

B0L002S, channel entry distribution (ampl > 54)

B0L001S, channel entry distribution (ampl > 54) calib_packv5_042523_0143.root, FC#9, port A1 **Entries** 3328 Mean 90.01 3000 Std Dev 0.08971 2500 2000 1500 1000 500

100

150

50

250

Channel entry