

B1L102S, U7-ch0

calib_packv5_042523_0143.root, FC#11, port A2

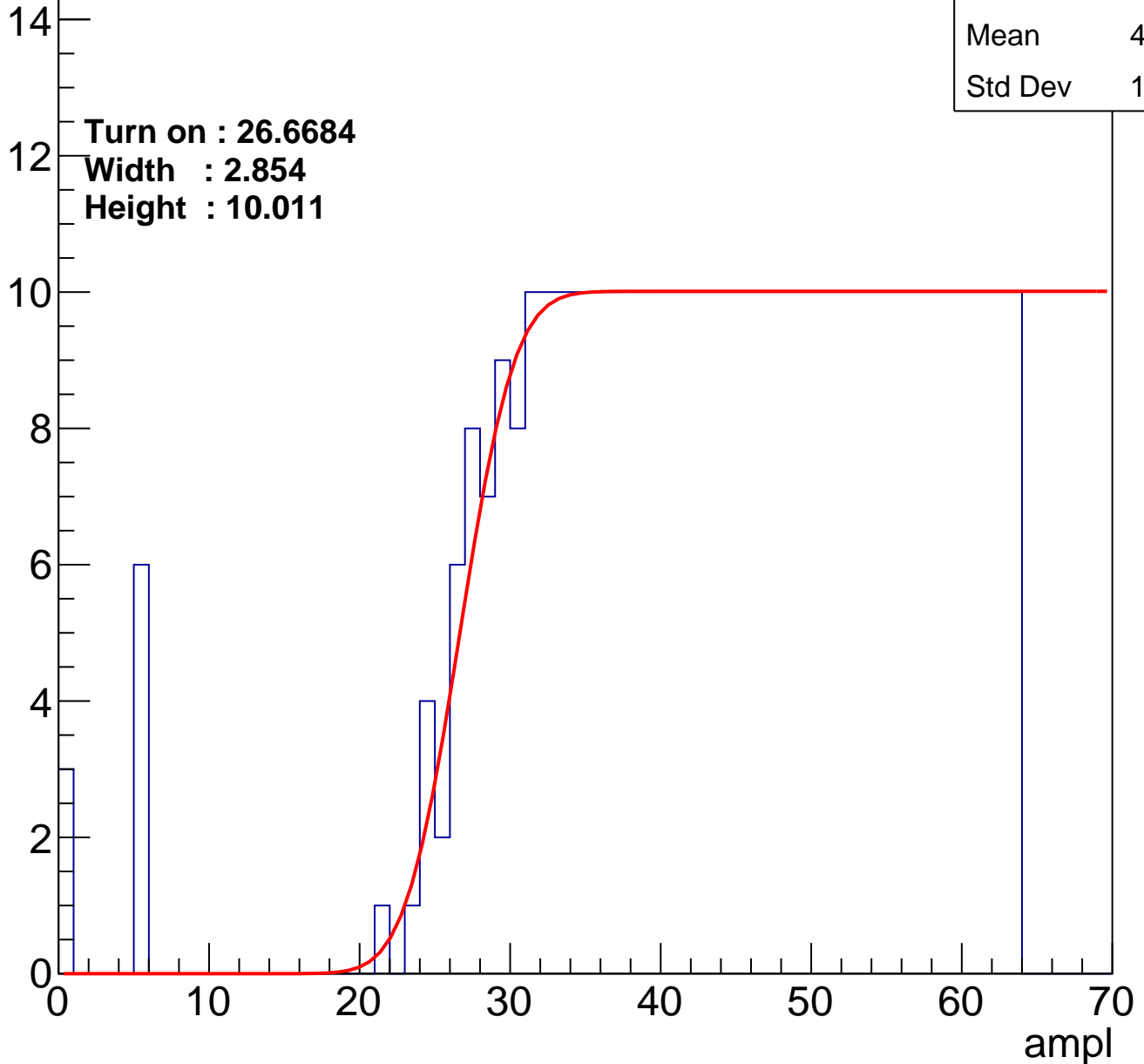
Entries	385
Mean	43.63
Std Dev	12.56

Turn on : 26.6684

Width : 2.854

Height : 10.011

Entry



B1L102S, U7-ch1

calib_packv5_042523_0143.root, FC#11, port A2

Entries	374
Mean	44.46
Std Dev	11.61

Turn on : 27.5526

Width : 3.683

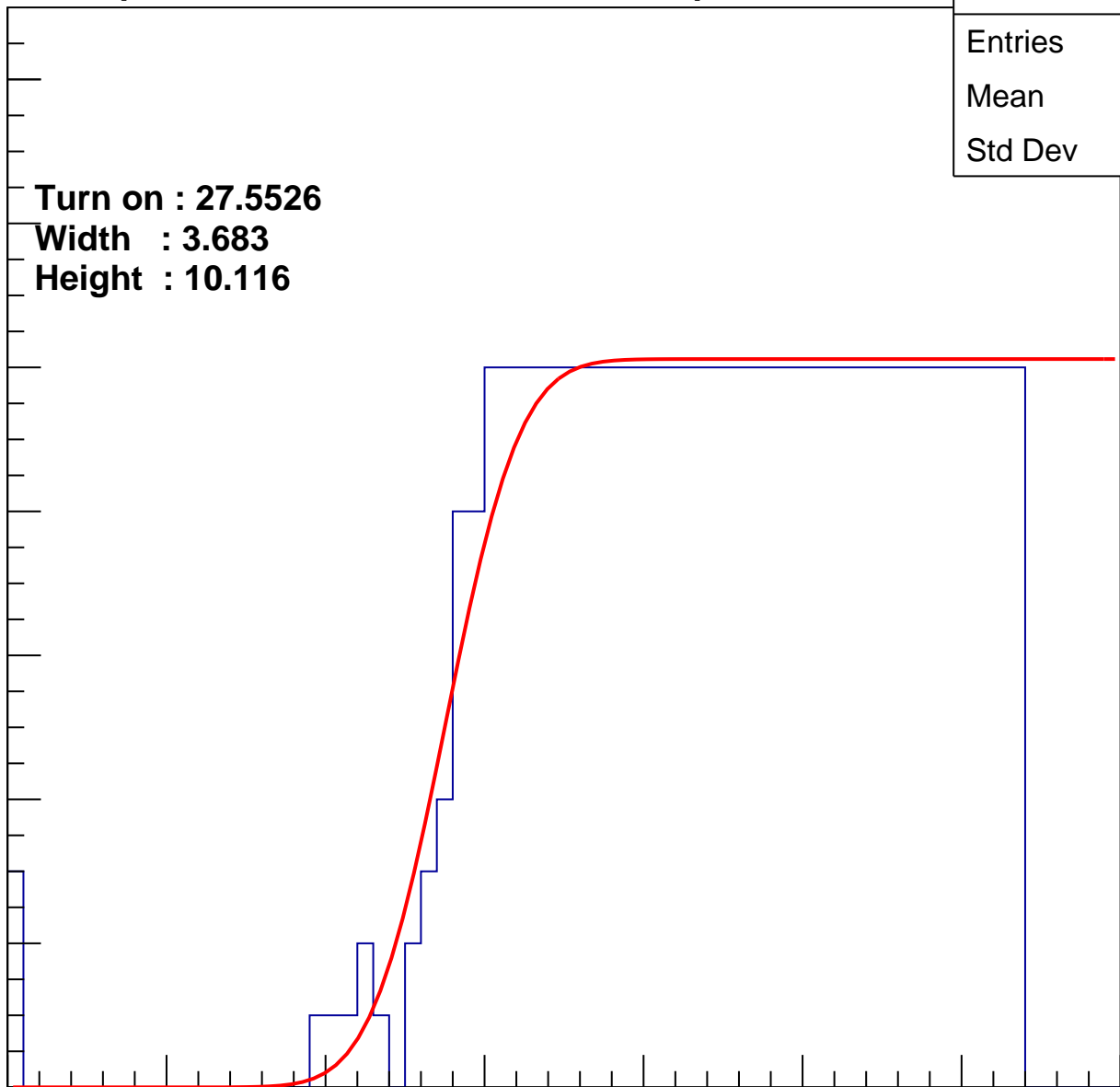
Height : 10.116

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L102S, U7-ch2

calib_packv5_042523_0143.root, FC#11, port A2

Entries	385
Mean	44.01
Std Dev	11.64

Turn on : 25.4085

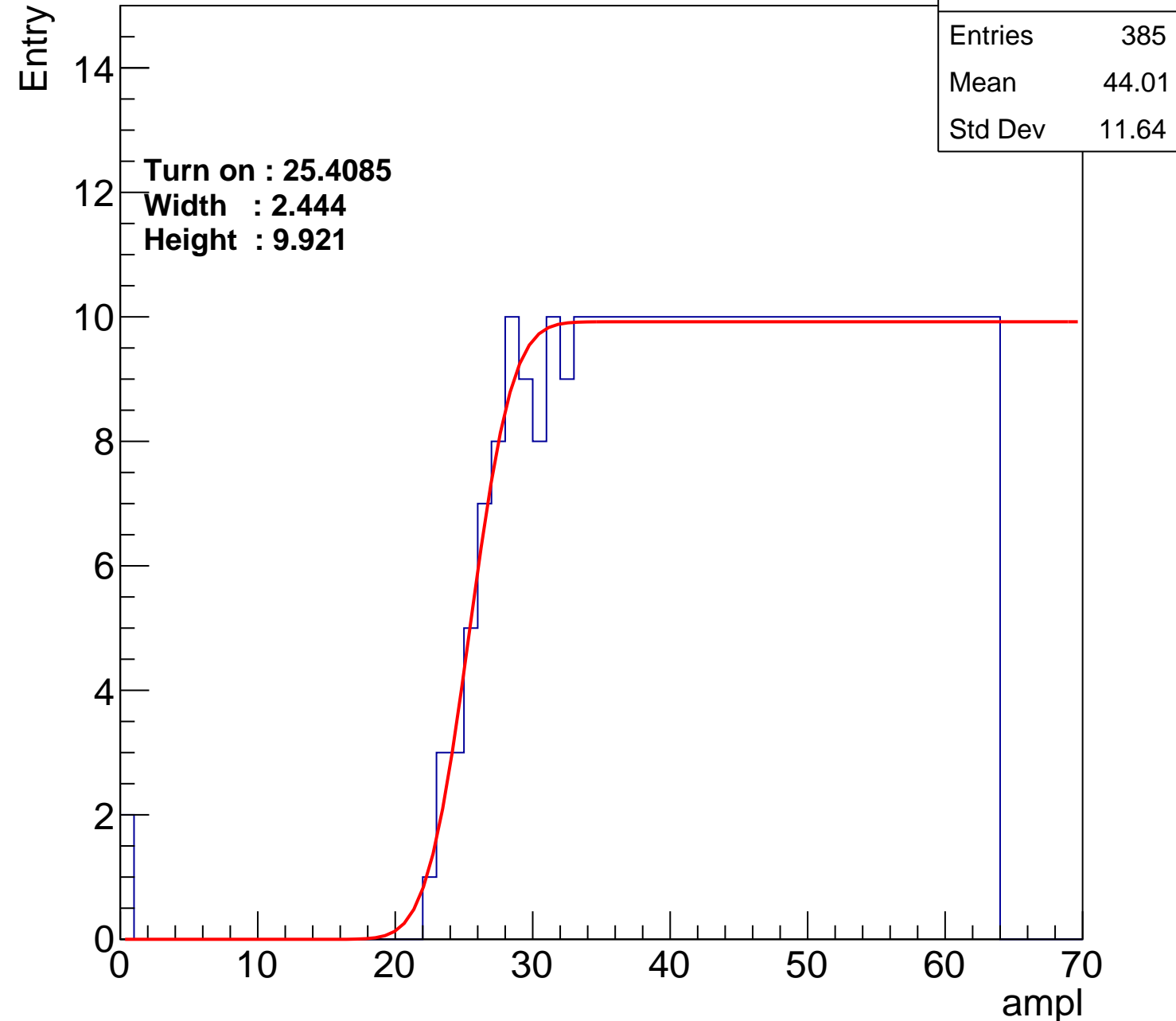
Width : 2.444

Height : 9.921

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch3

calib_packv5_042523_0143.root, FC#11, port A2

Entries	373
Mean	44.74
Std Dev	11.04

Turn on : 27.0617

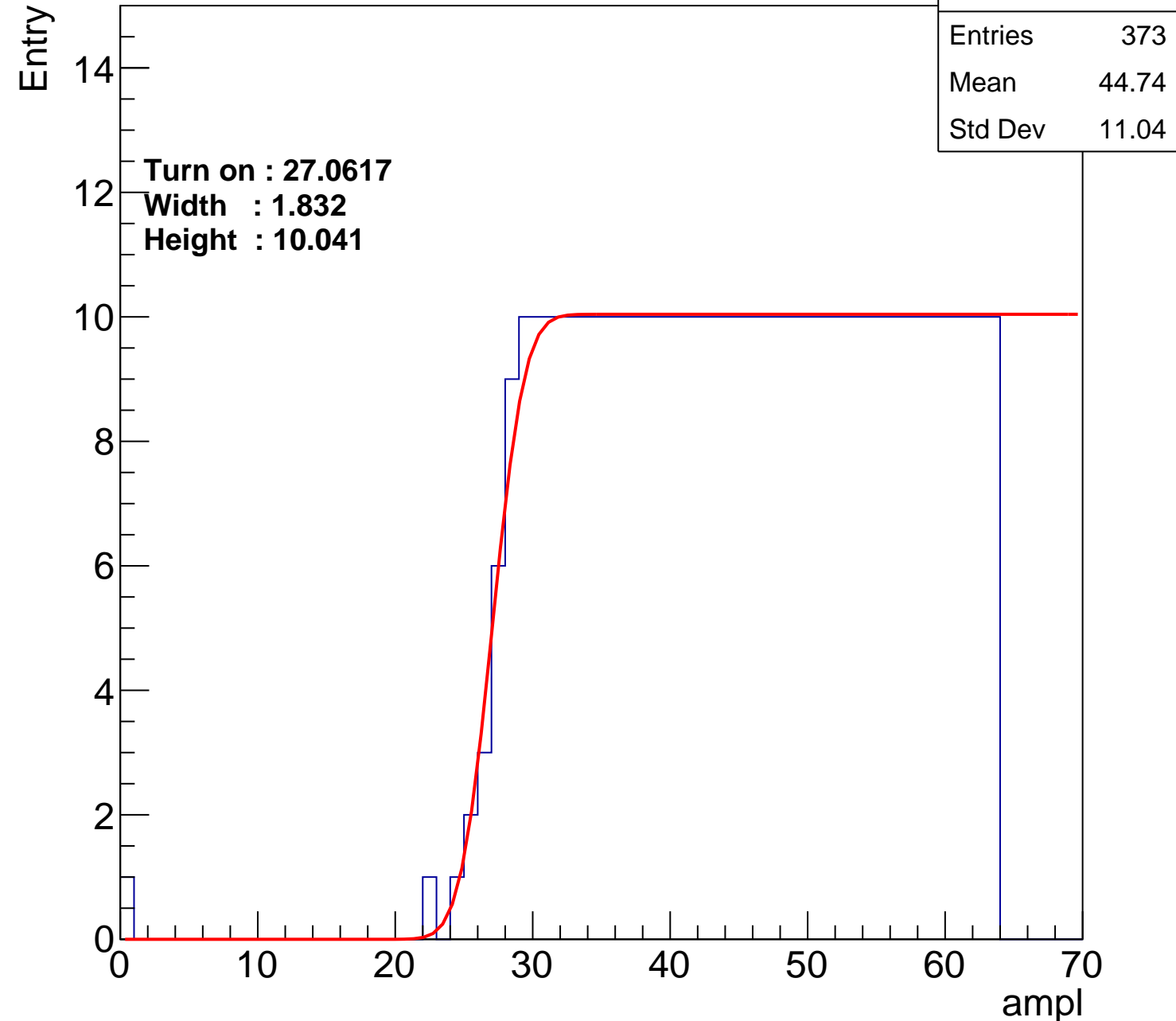
Width : 1.832

Height : 10.041

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch4

calib_packv5_042523_0143.root, FC#11, port A2

Entries	406
Mean	42.92
Std Dev	12.35

Turn on : 23.3241

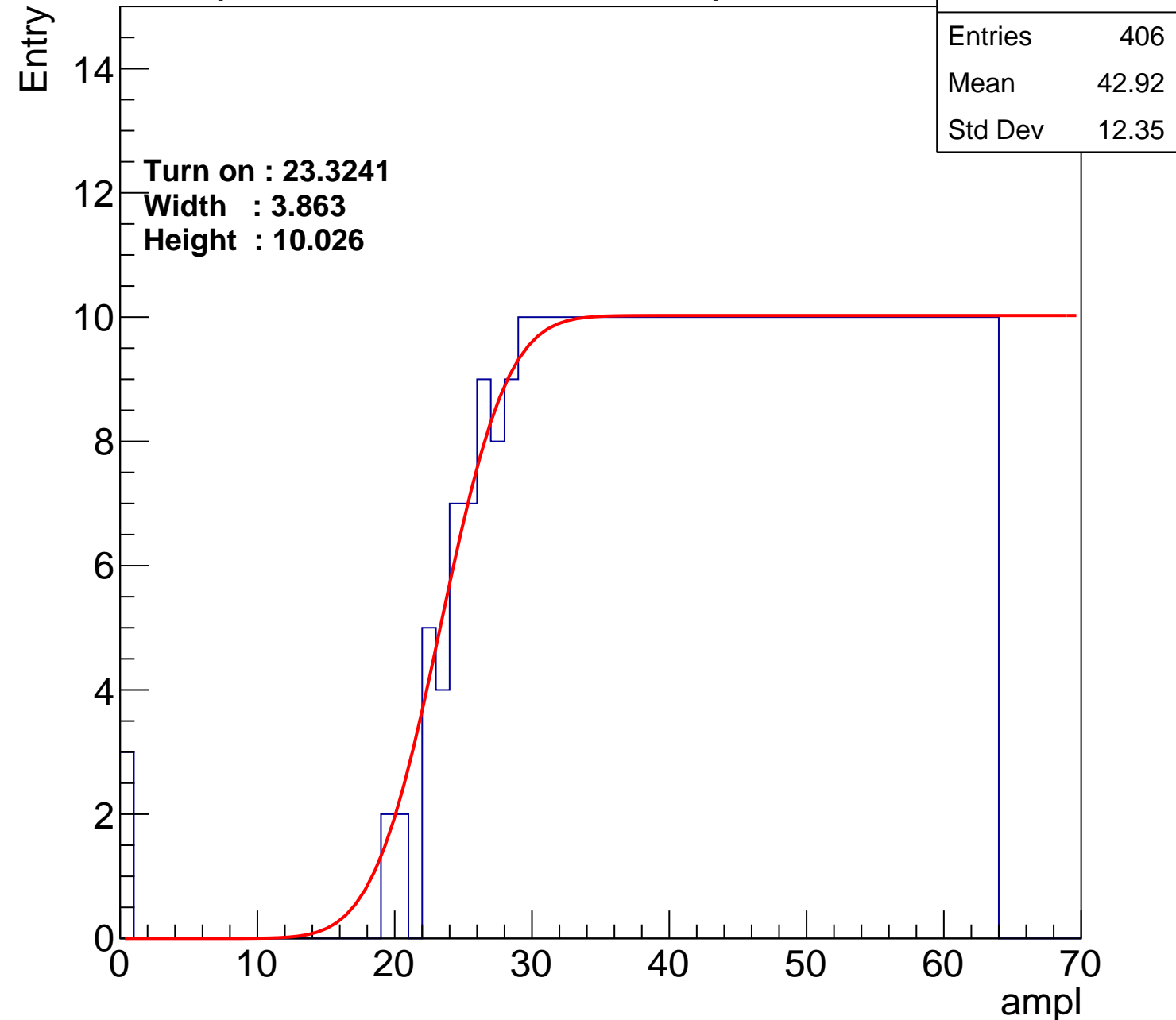
Width : 3.863

Height : 10.026

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch5

calib_packv5_042523_0143.root, FC#11, port A2

Entries	398
Mean	43.29
Std Dev	12.24

Turn on : 24.7978

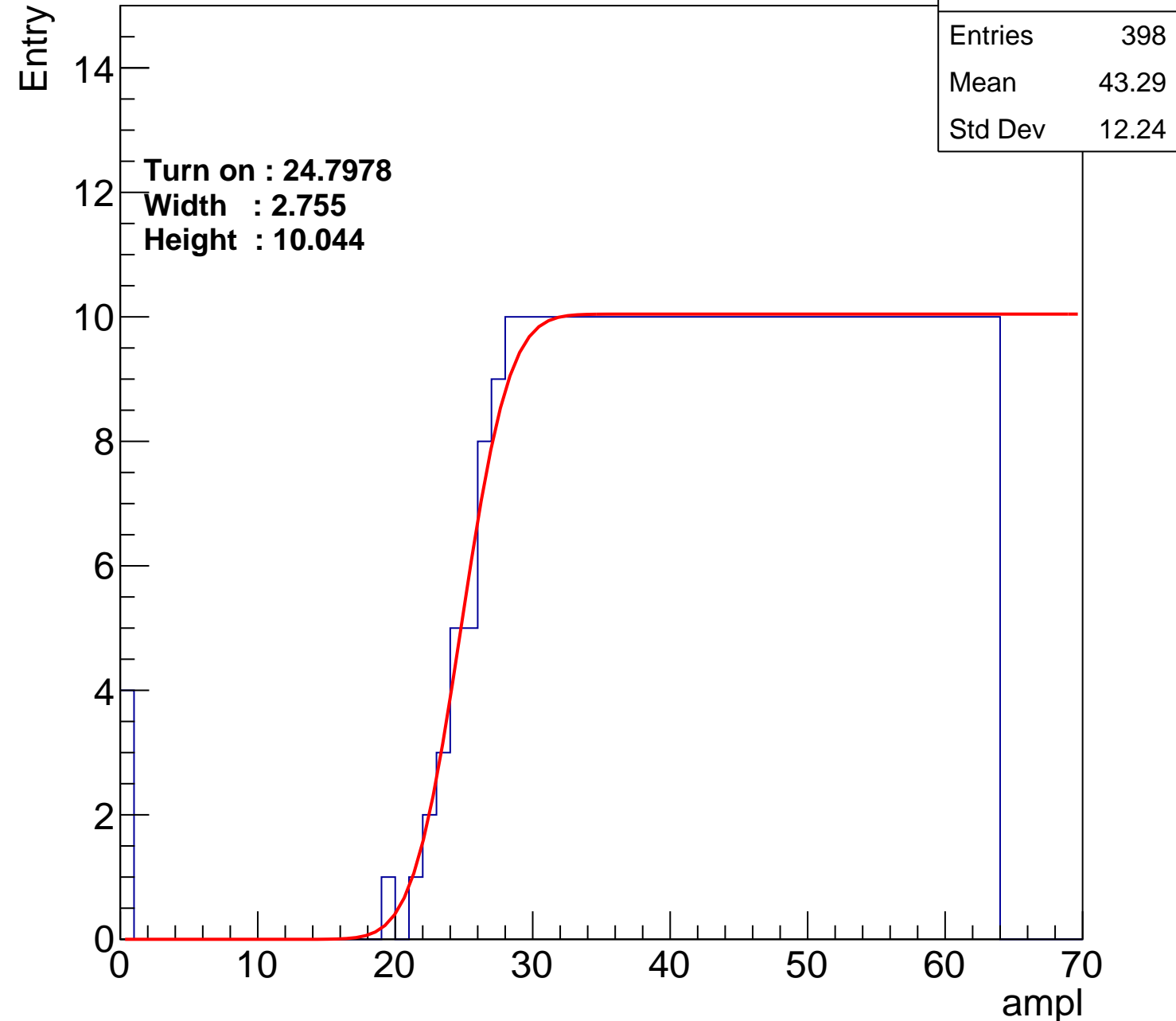
Width : 2.755

Height : 10.044

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch6

calib_packv5_042523_0143.root, FC#11, port A2

Entries	393
Mean	43.63
Std Dev	11.84

Turn on : 25.1695

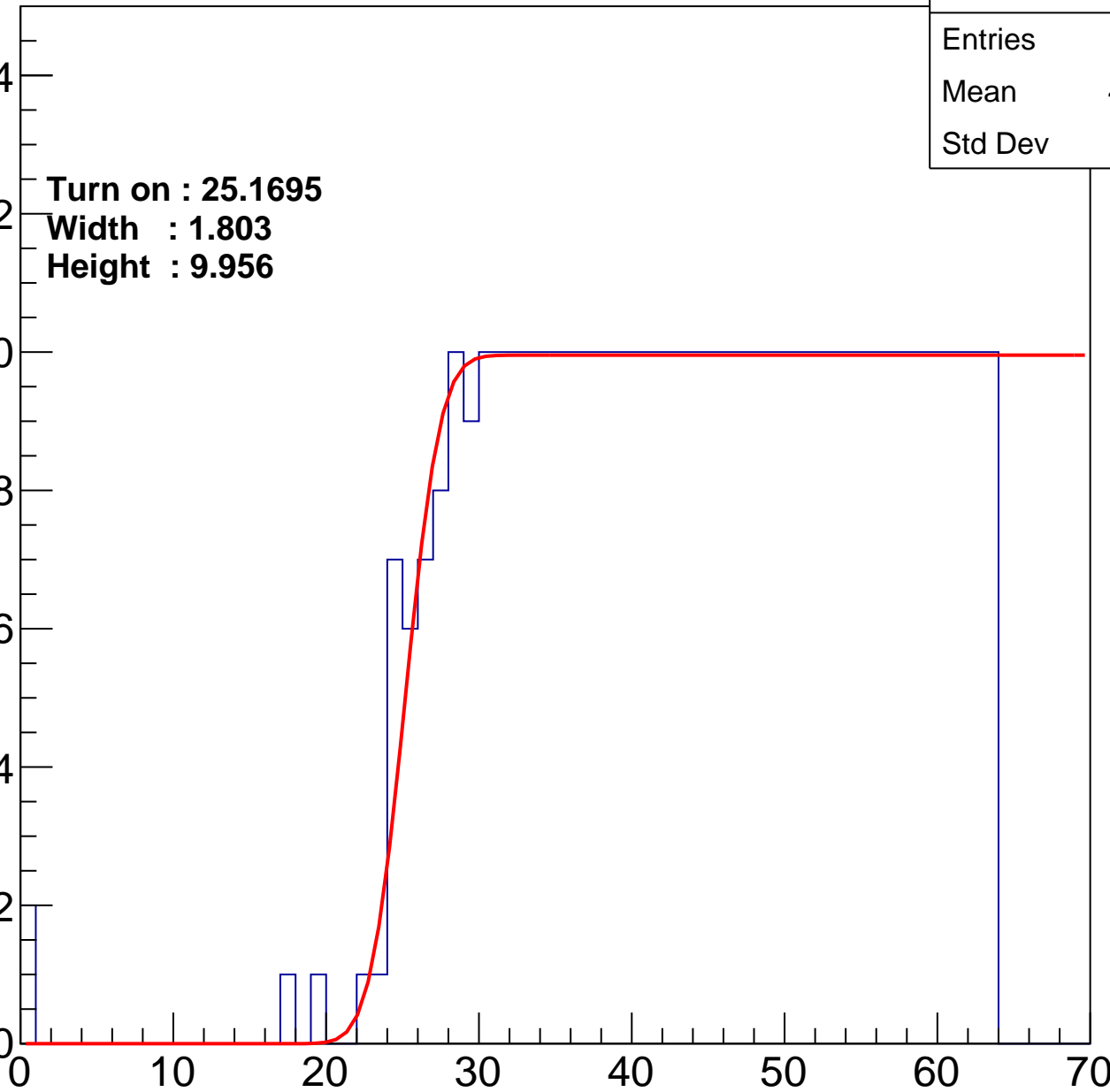
Width : 1.803

Height : 9.956

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch7

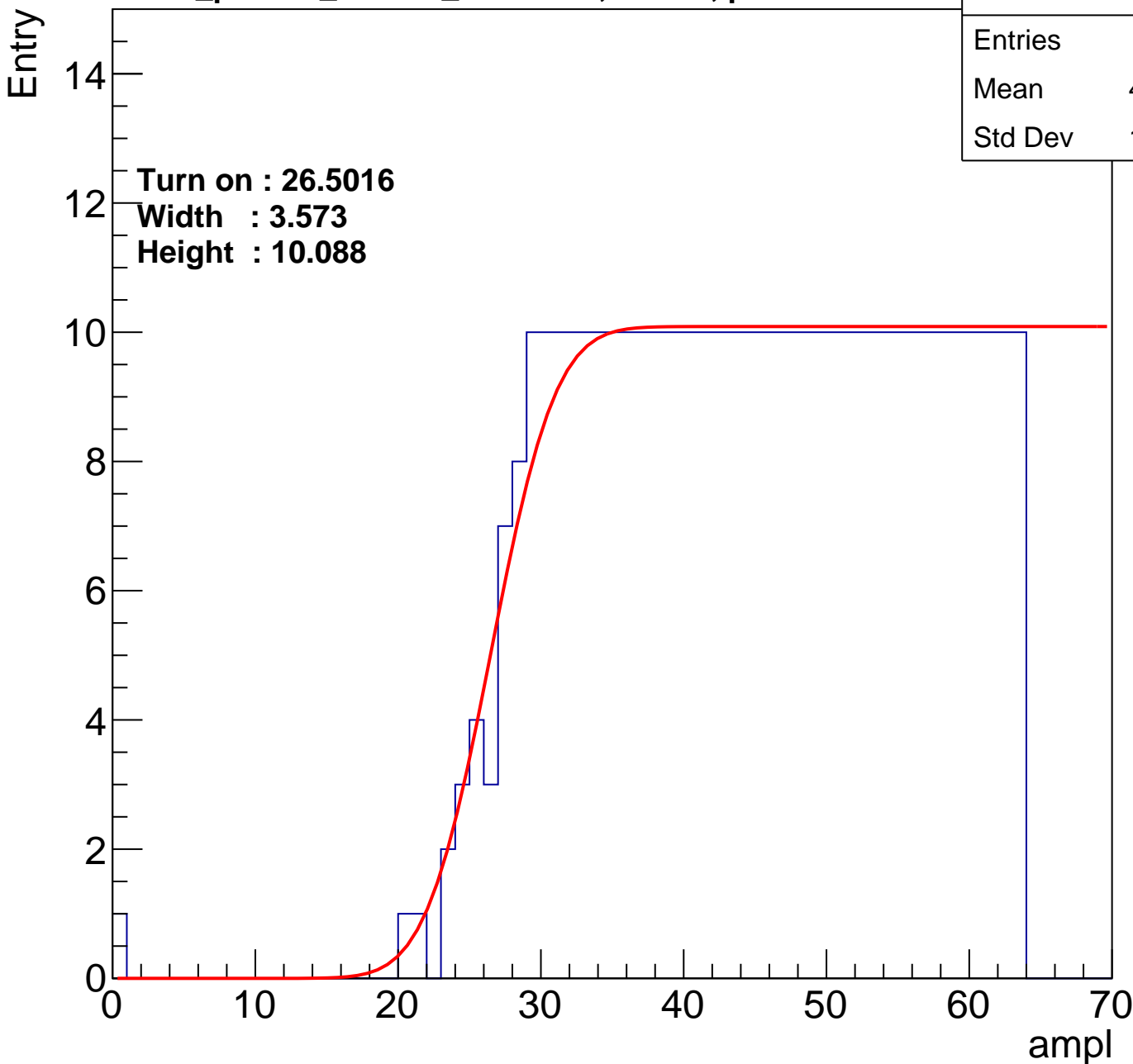
calib_packv5_042523_0143.root, FC#11, port A2

Entries	380
Mean	44.34
Std Dev	11.32

Turn on : 26.5016

Width : 3.573

Height : 10.088



B1L102S, U7-ch8

calib_packv5_042523_0143.root, FC#11, port A2

Entries	384
Mean	43.93
Std Dev	11.99

Turn on : 26.0878

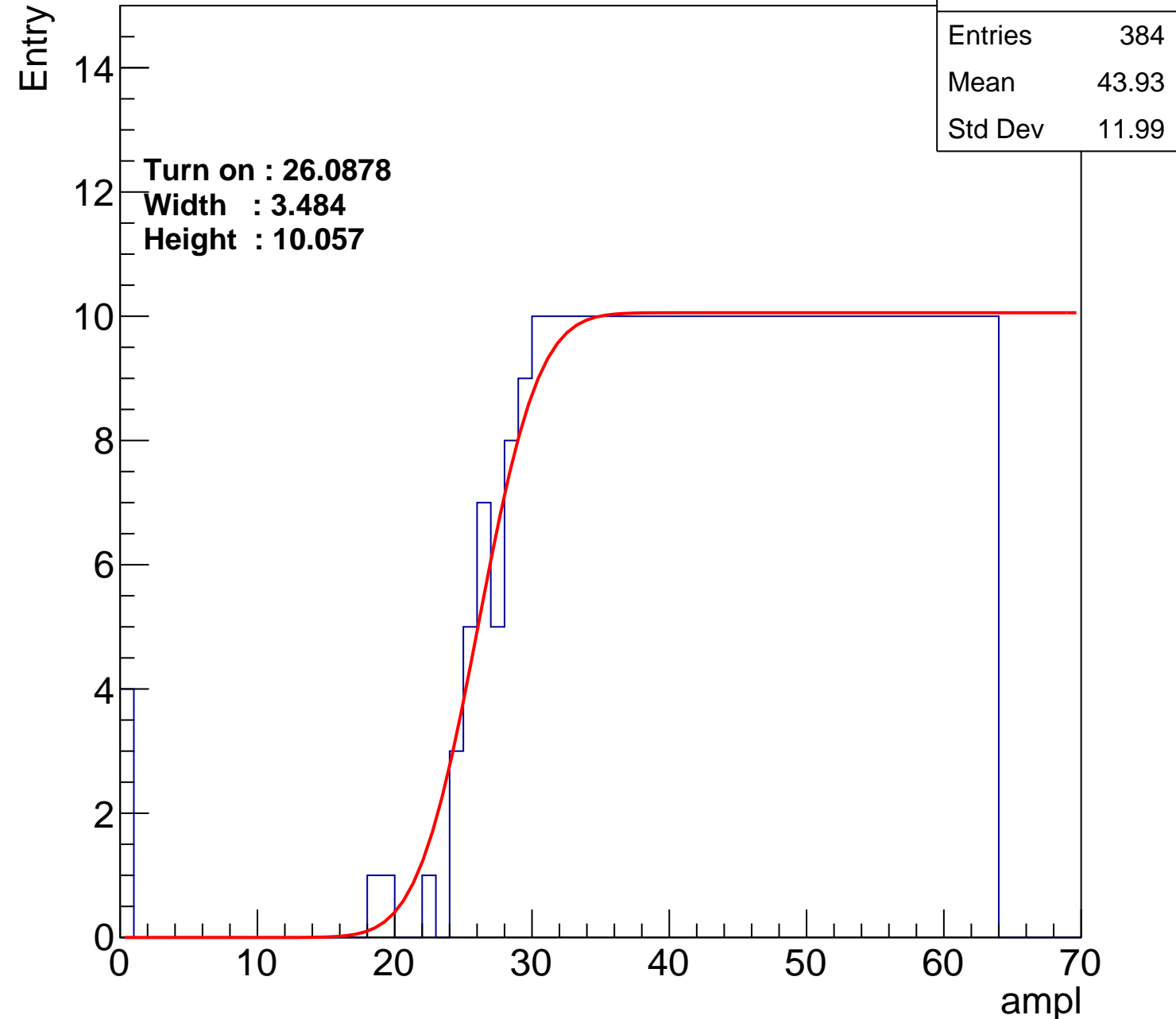
Width : 3.484

Height : 10.057

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch9

calib_packv5_042523_0143.root, FC#11, port A2

Entries	367
Mean	44.99
Std Dev	10.95

Turn on : 27.4757

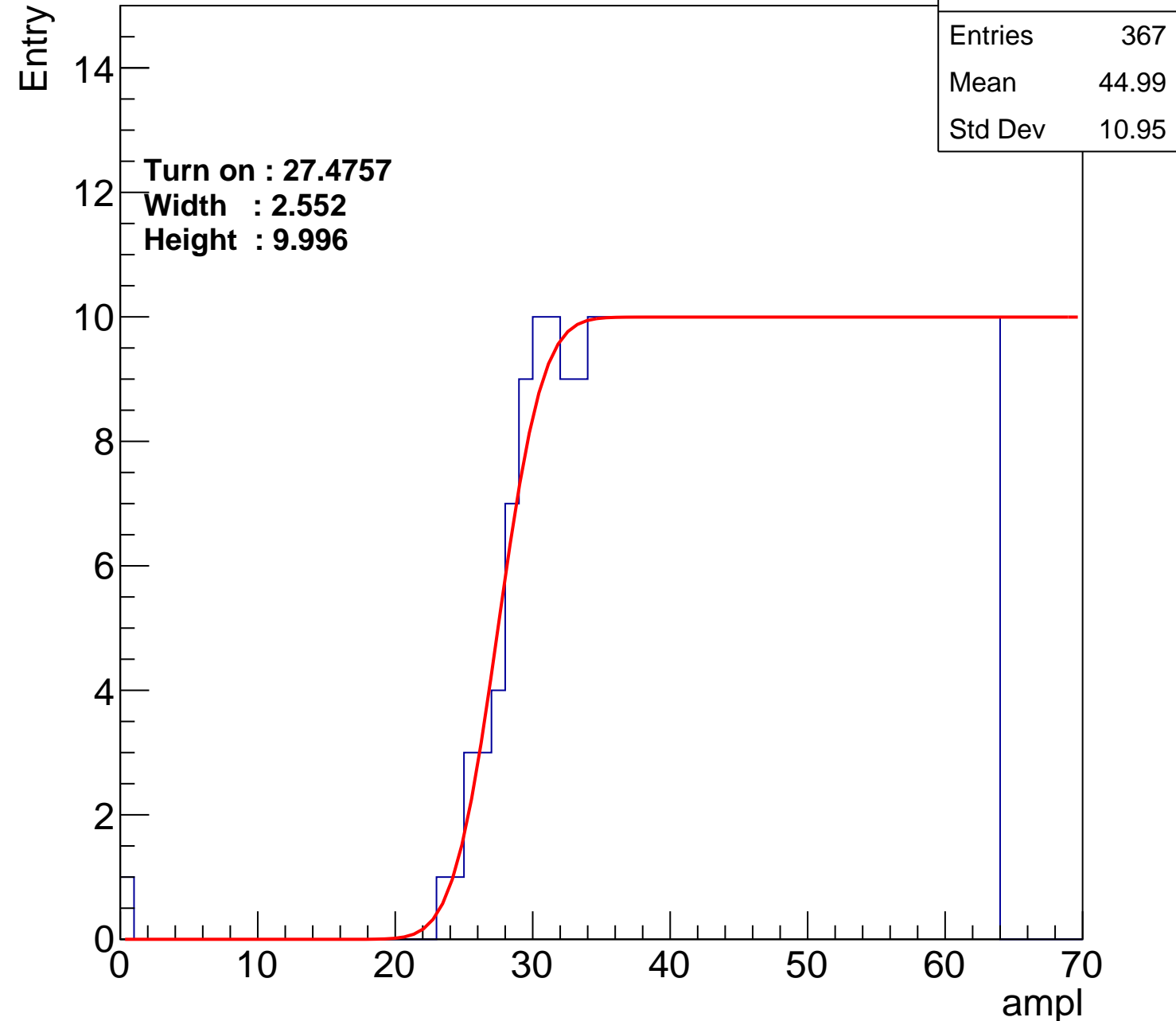
Width : 2.552

Height : 9.996

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch10

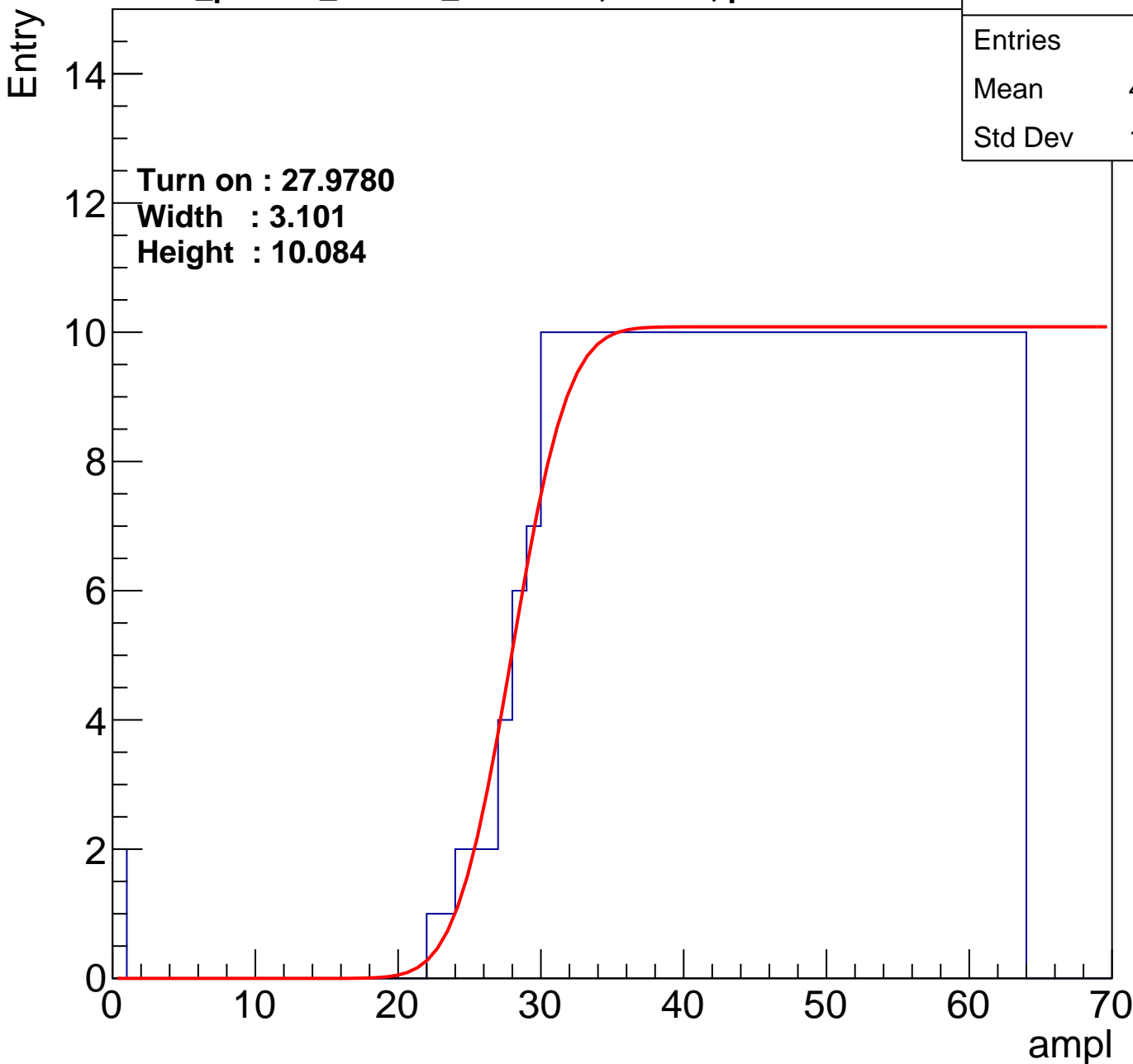
calib_packv5_042523_0143.root, FC#11, port A2

Turn on : 27.9780

Width : 3.101

Height : 10.084

Entries	367
Mean	44.92
Std Dev	11.17



B1L102S, U7-ch11

calib_packv5_042523_0143.root, FC#11, port A2

Entries	398
Mean	43.4
Std Dev	11.89

Turn on : 24.5499

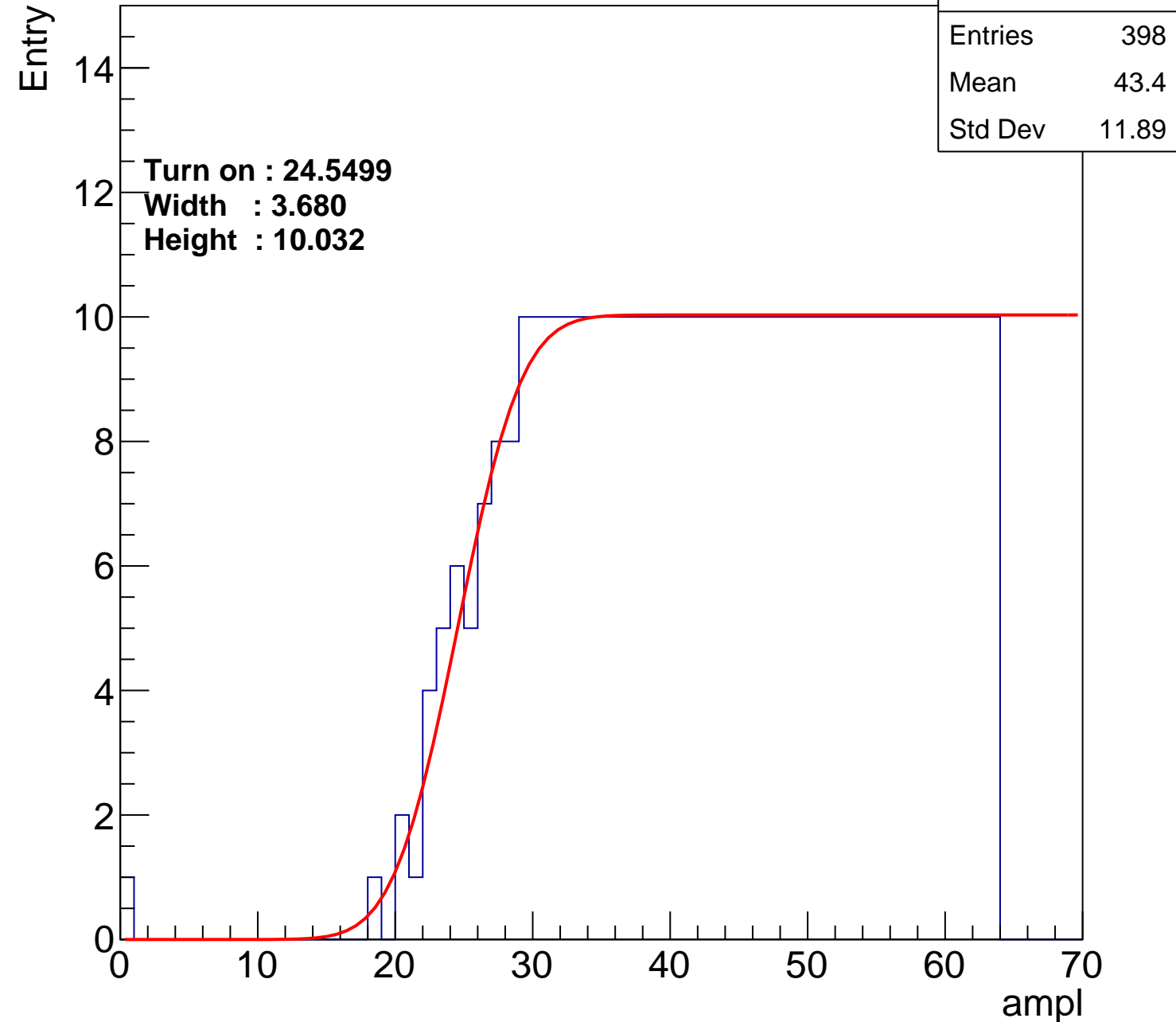
Width : 3.680

Height : 10.032

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch12

calib_packv5_042523_0143.root, FC#11, port A2

Entries	388
Mean	43.9
Std Dev	11.6

Turn on : 25.3255

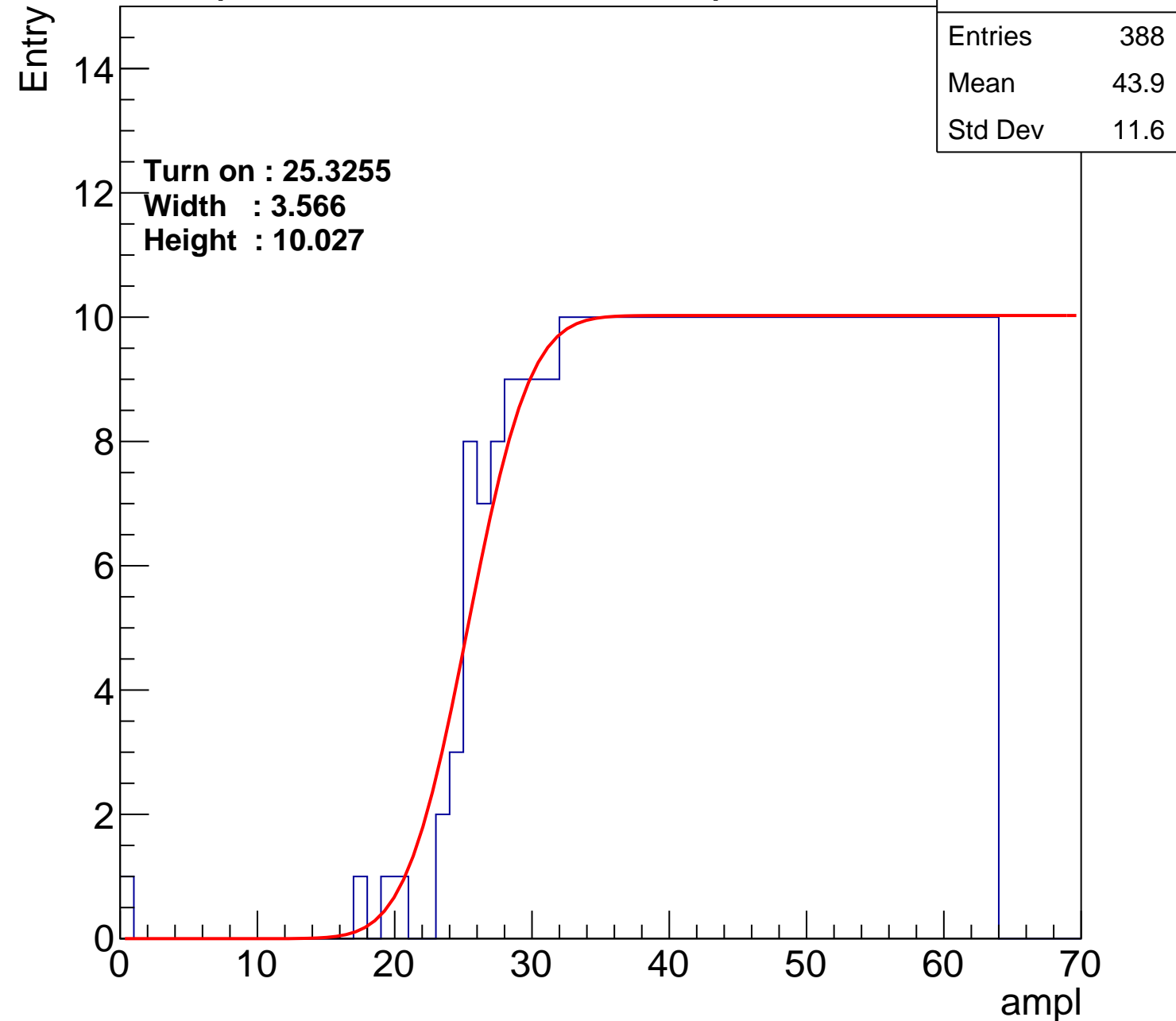
Width : 3.566

Height : 10.027

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch13

calib_packv5_042523_0143.root, FC#11, port A2

Entries	377
Mean	44.48
Std Dev	11.24

Turn on : 26.3561

Width : 3.504

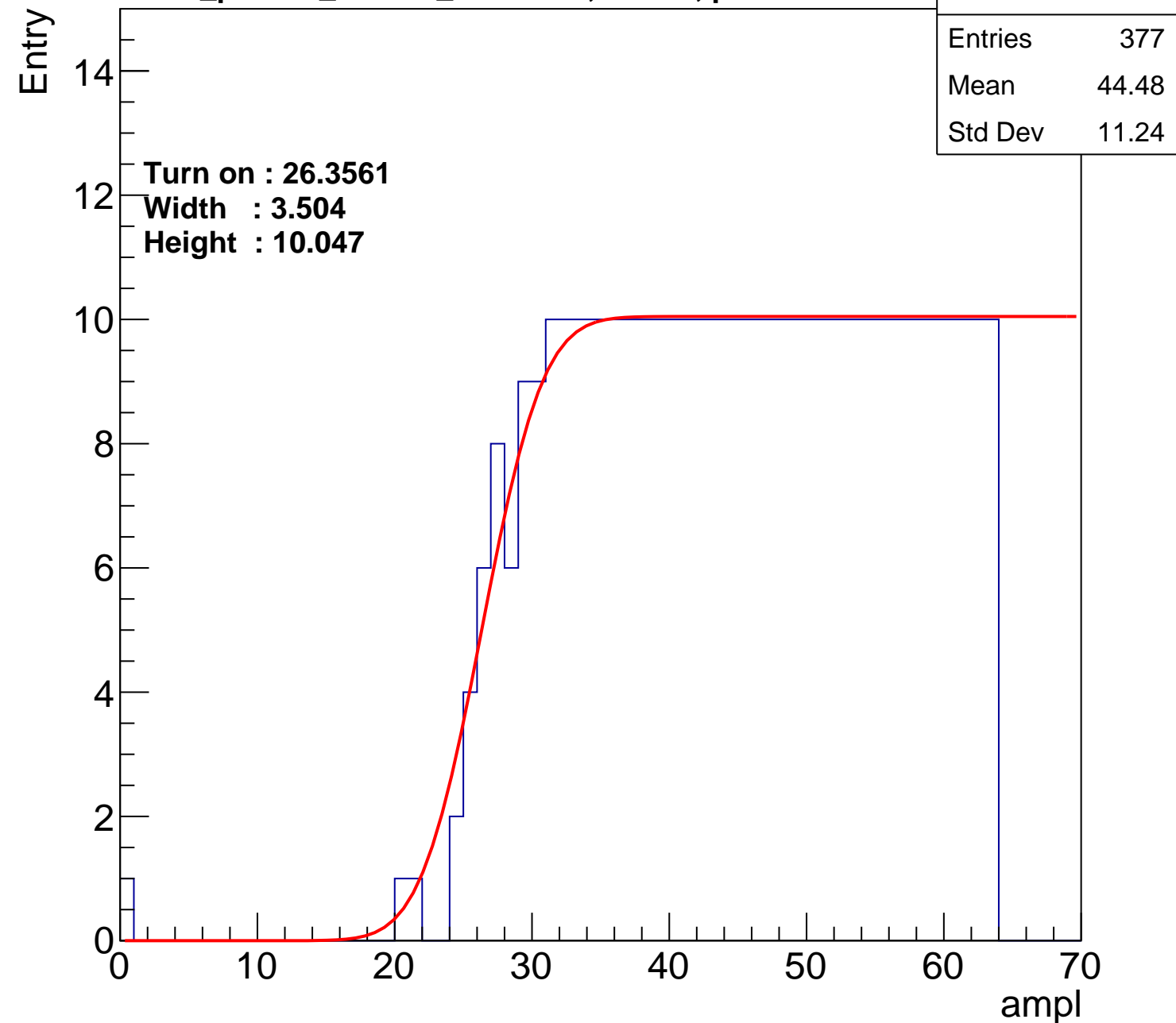
Height : 10.047

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L102S, U7-ch14

calib_packv5_042523_0143.root, FC#11, port A2

Entries	371
Mean	44.78
Std Dev	11.07

Turn on : 26.7137

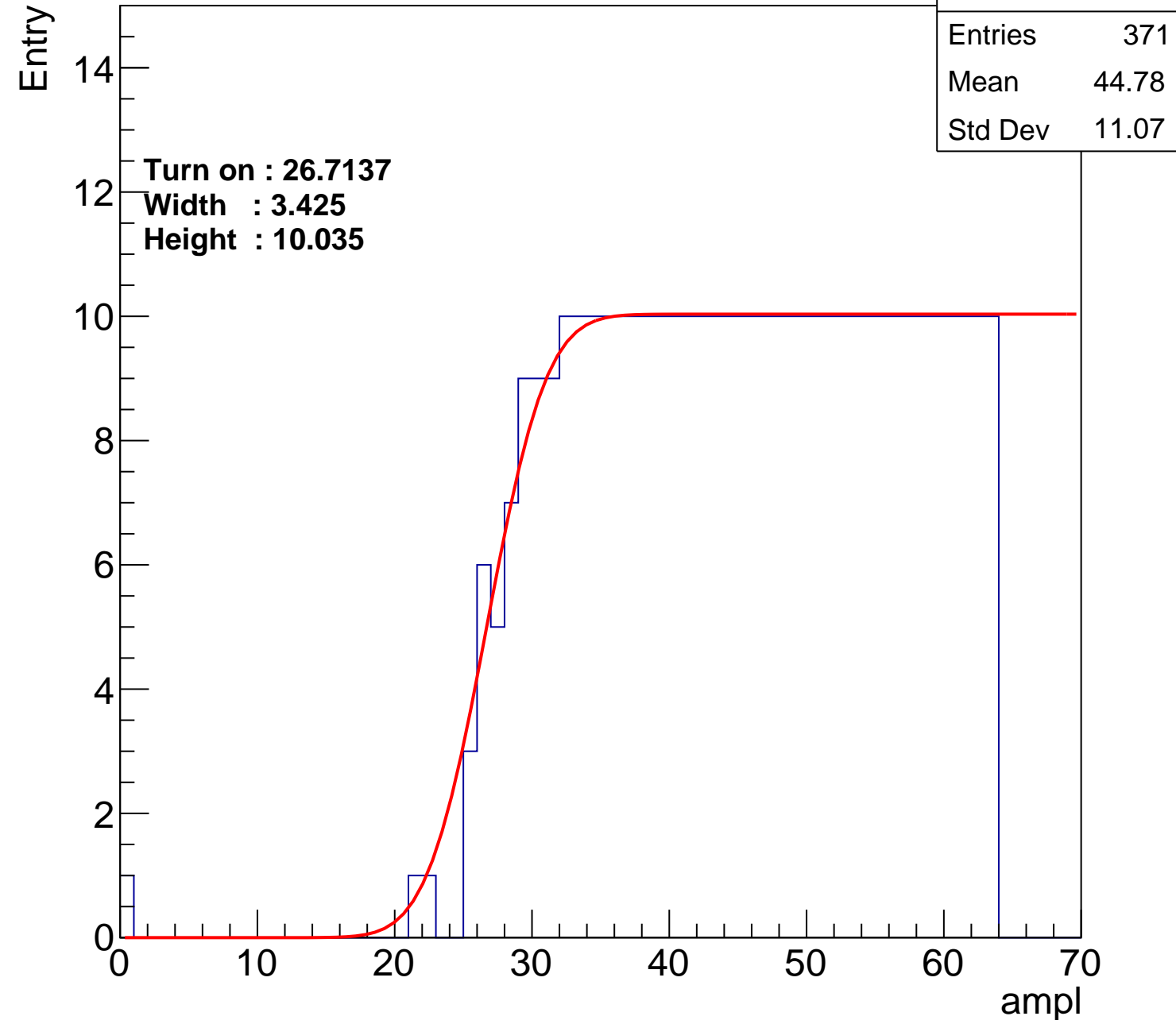
Width : 3.425

Height : 10.035

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch15

calib_packv5_042523_0143.root, FC#11, port A2

Entries	366
Mean	44.79
Std Dev	11.58

Turn on : 27.7971

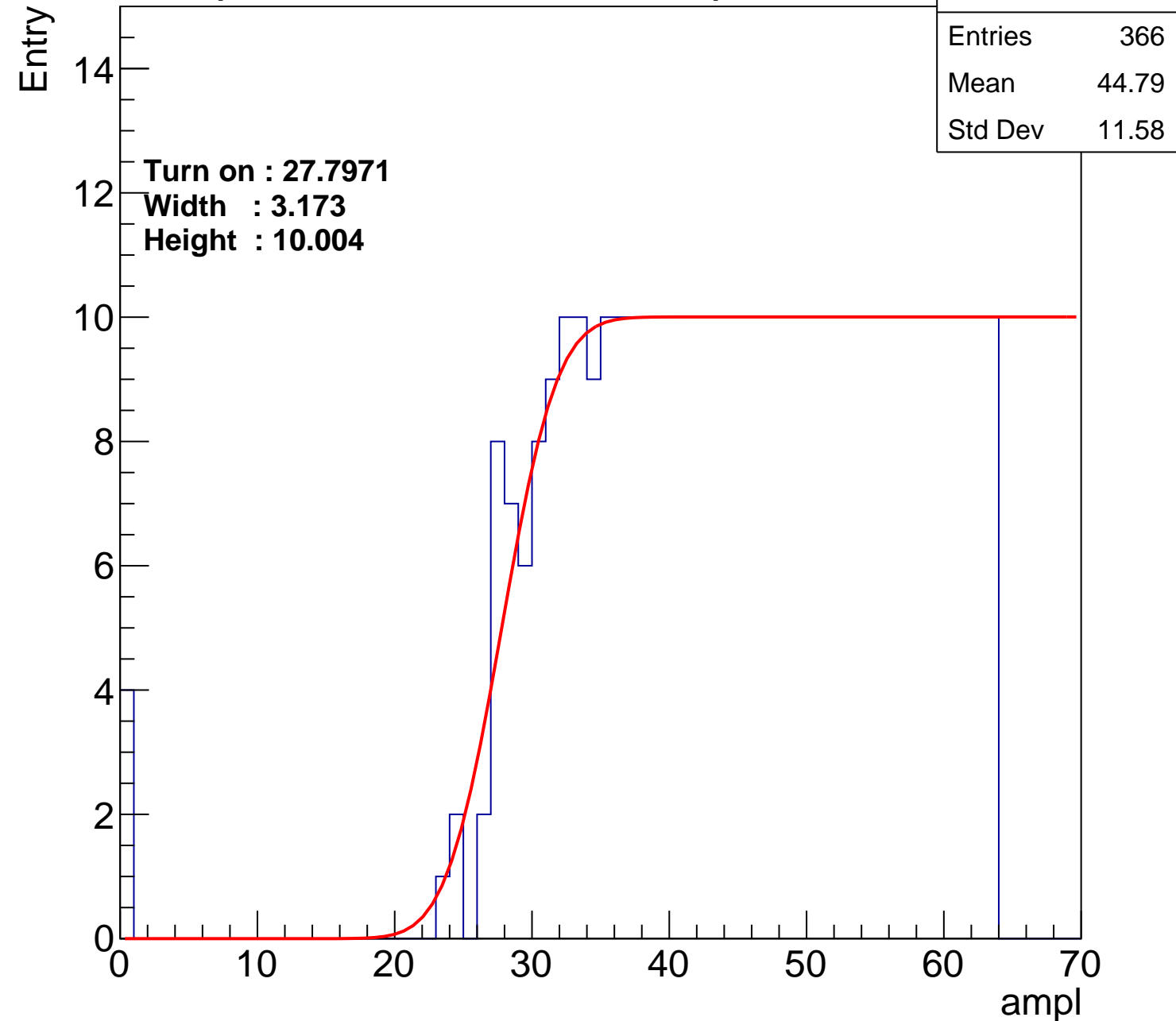
Width : 3.173

Height : 10.004

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch16

calib_packv5_042523_0143.root, FC#11, port A2

Entries	390
Mean	43.8
Std Dev	11.66

Turn on : 25.1094

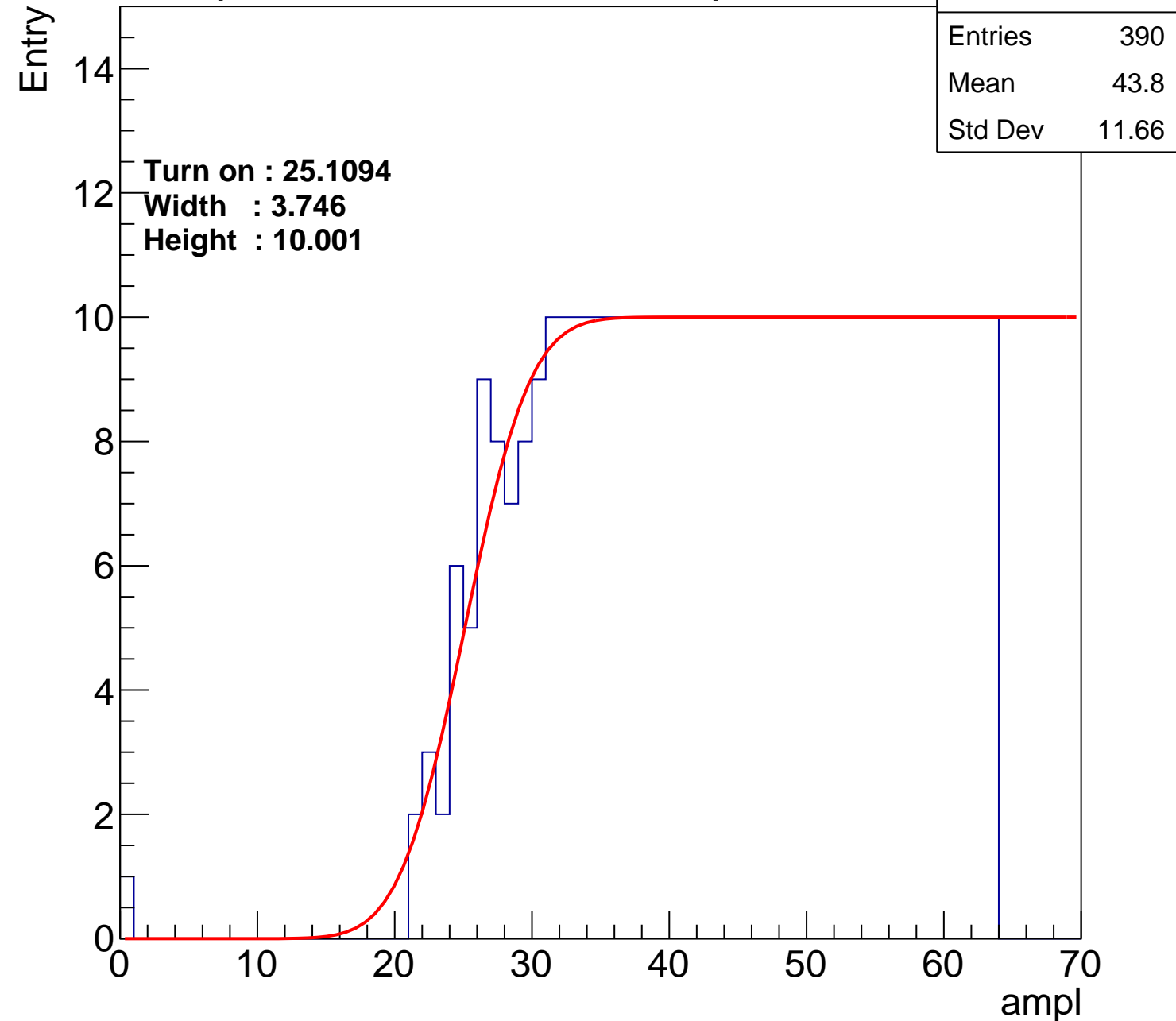
Width : 3.746

Height : 10.001

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch17

calib_packv5_042523_0143.root, FC#11, port A2

Entries	399
Mean	43.23
Std Dev	12.28

Turn on : 24.3463

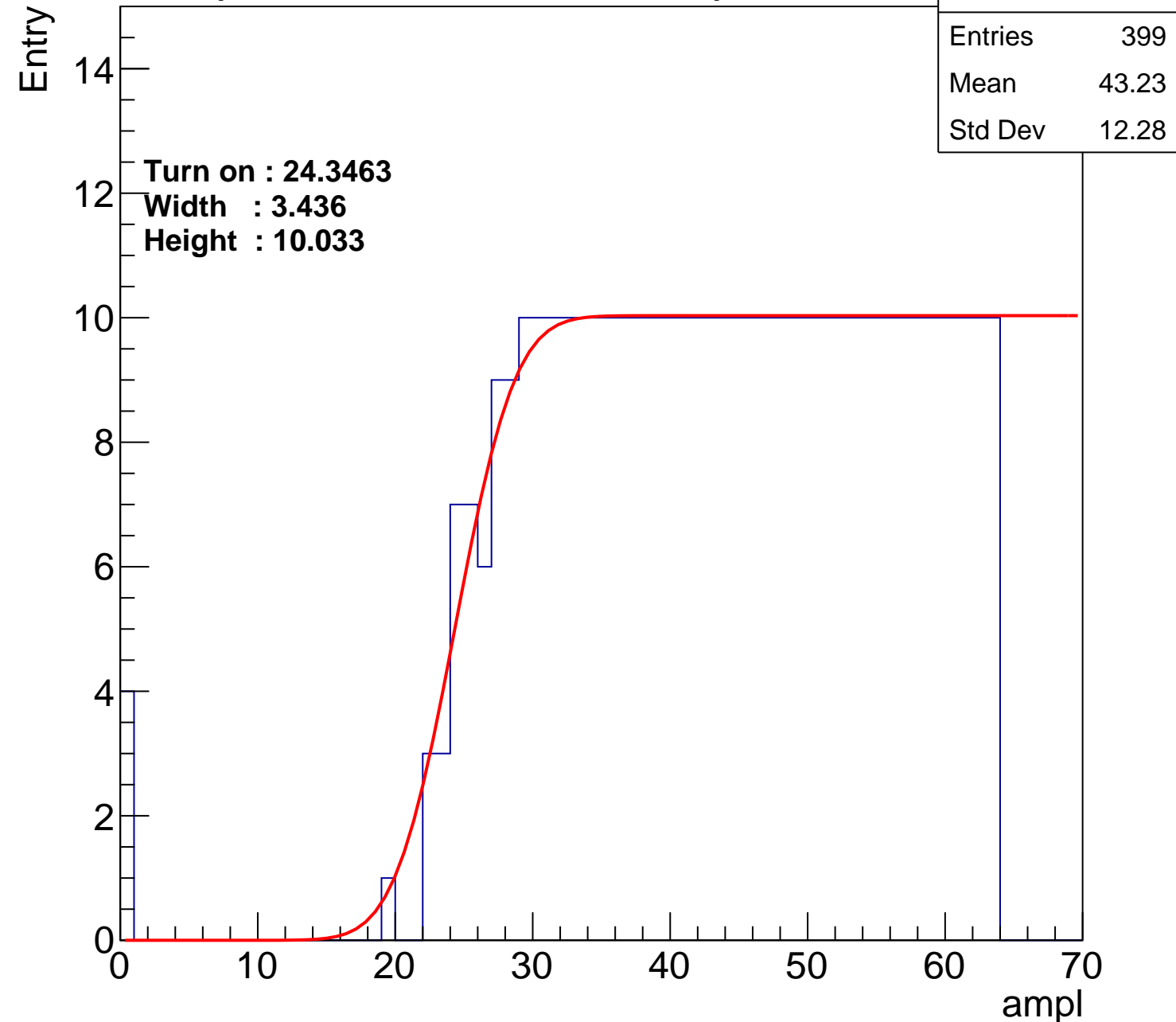
Width : 3.436

Height : 10.033

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch18

calib_packv5_042523_0143.root, FC#11, port A2

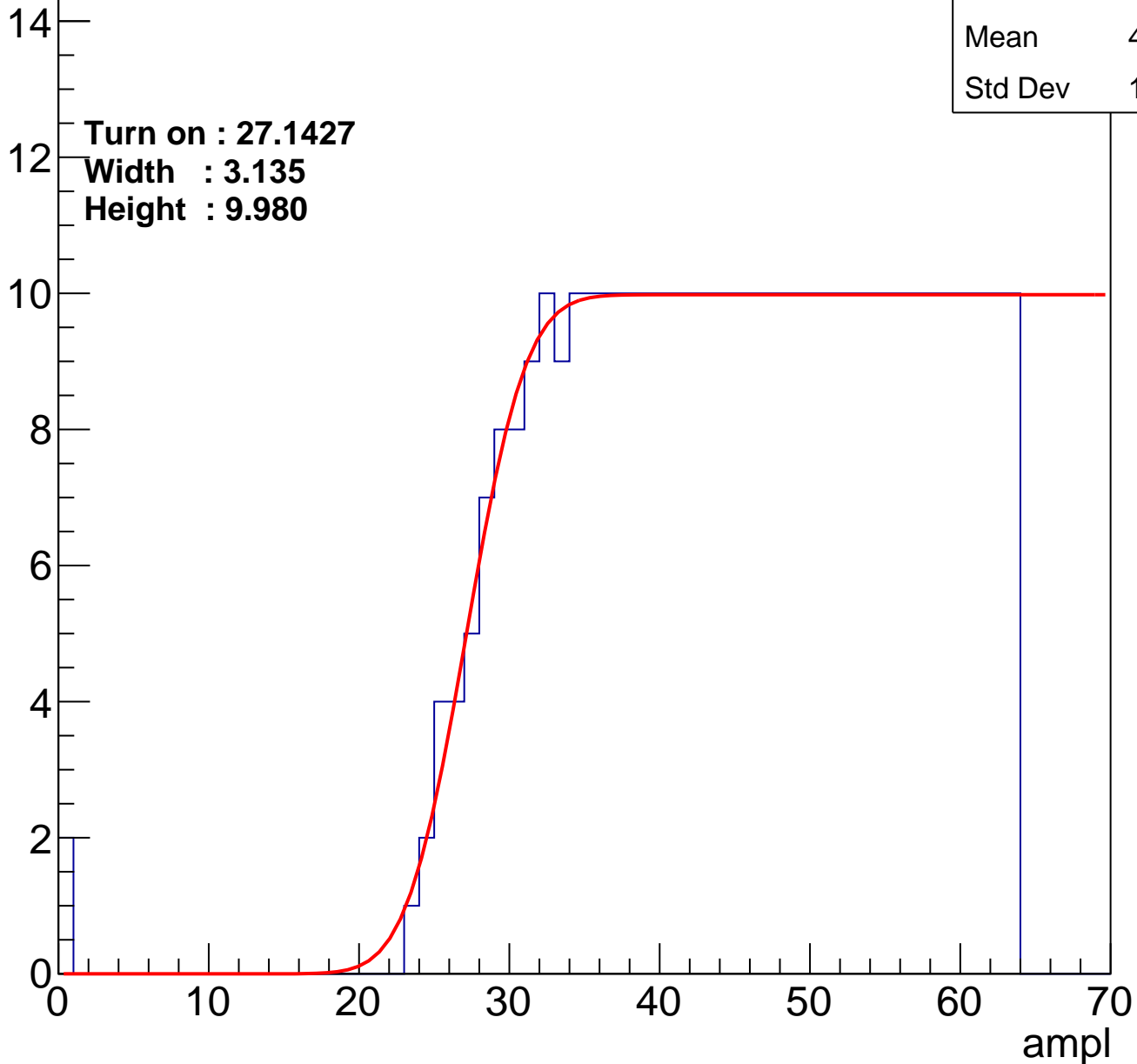
Entries	369
Mean	44.78
Std Dev	11.27

Turn on : 27.1427

Width : 3.135

Height : 9.980

Entry



B1L102S, U7-ch19

calib_packv5_042523_0143.root, FC#11, port A2

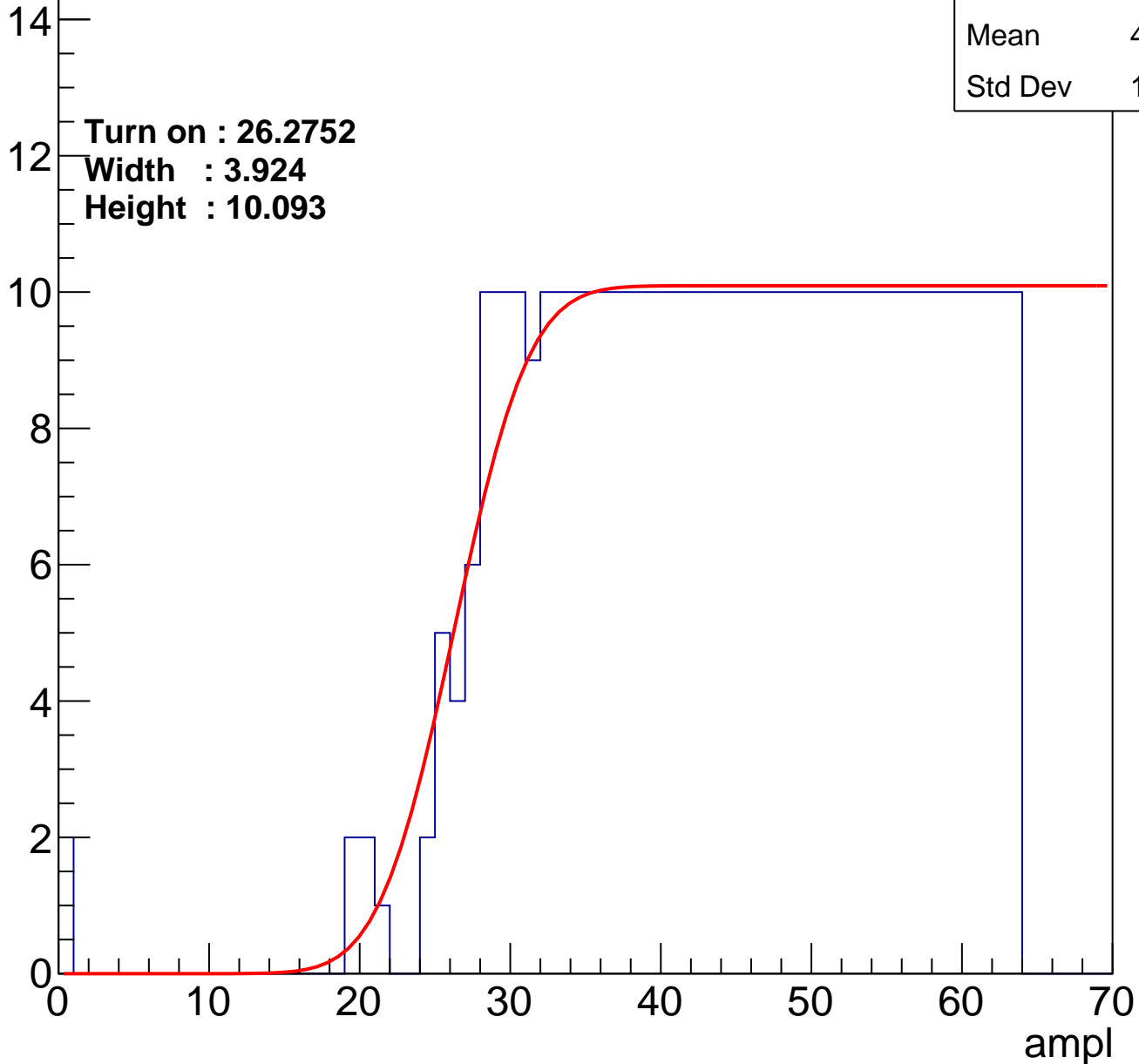
Entries	383
Mean	44.09
Std Dev	11.64

Turn on : 26.2752

Width : 3.924

Height : 10.093

Entry



B1L102S, U7-ch20

calib_packv5_042523_0143.root, FC#11, port A2

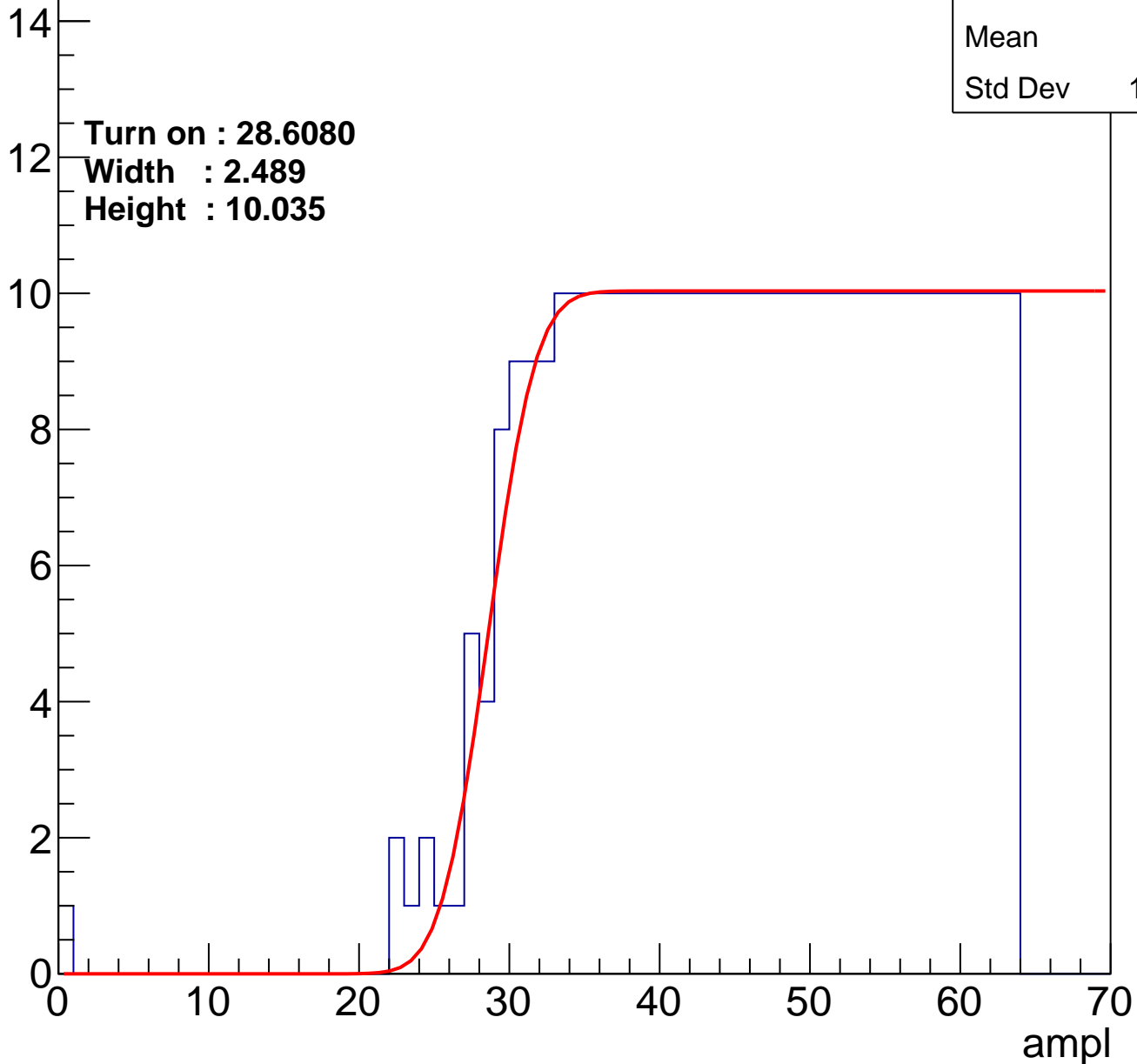
Entries	362
Mean	45.2
Std Dev	10.89

Turn on : 28.6080

Width : 2.489

Height : 10.035

Entry



B1L102S, U7-ch21

calib_packv5_042523_0143.root, FC#11, port A2

Entries	377
Mean	44.29
Std Dev	11.78

Turn on : 26.9384

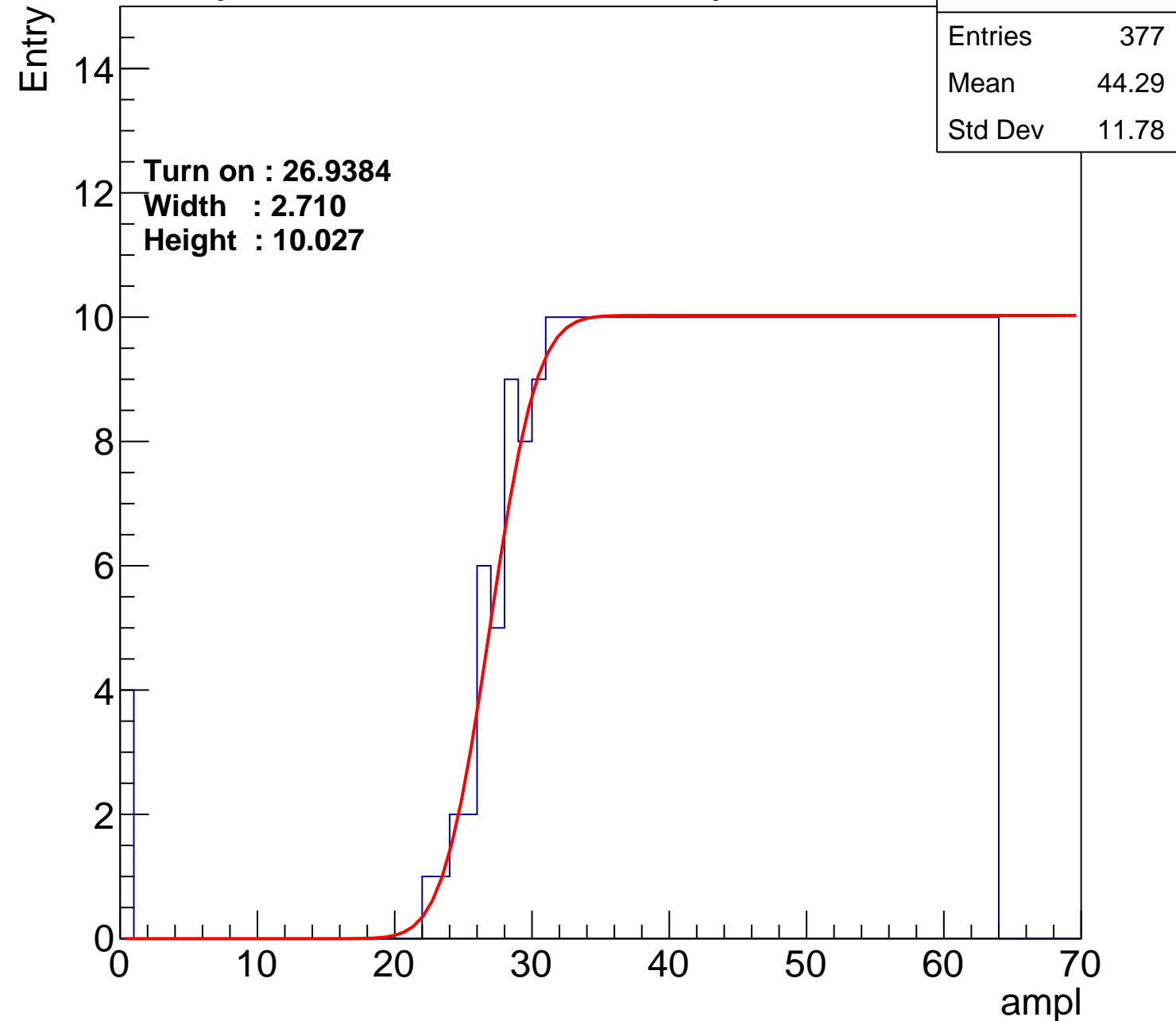
Width : 2.710

Height : 10.027

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch22

calib_packv5_042523_0143.root, FC#11, port A2

Entries	369
Mean	44.87
Std Dev	11.05

Turn on : 28.1941

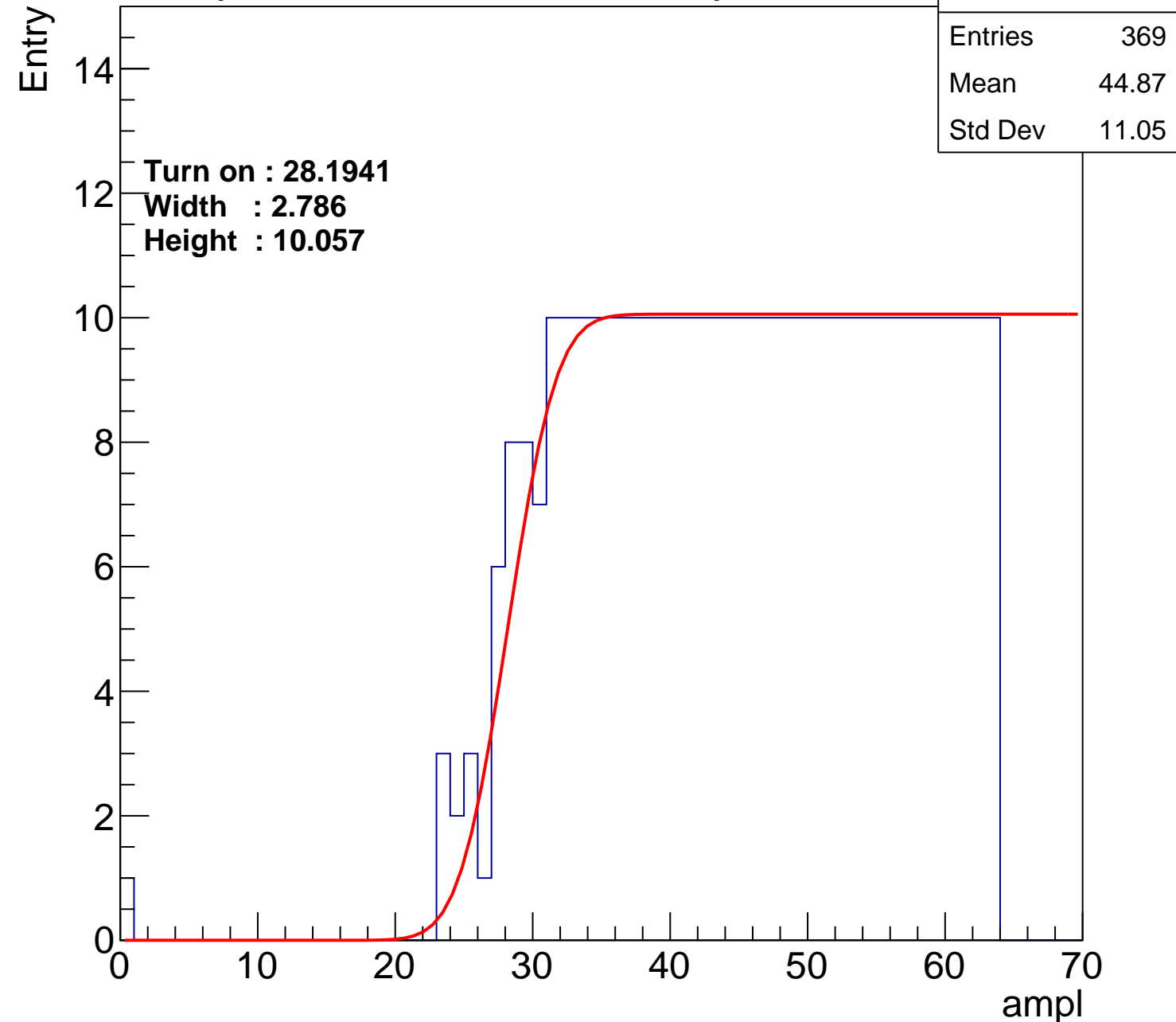
Width : 2.786

Height : 10.057

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch23

calib_packv5_042523_0143.root, FC#11, port A2

Entries	370
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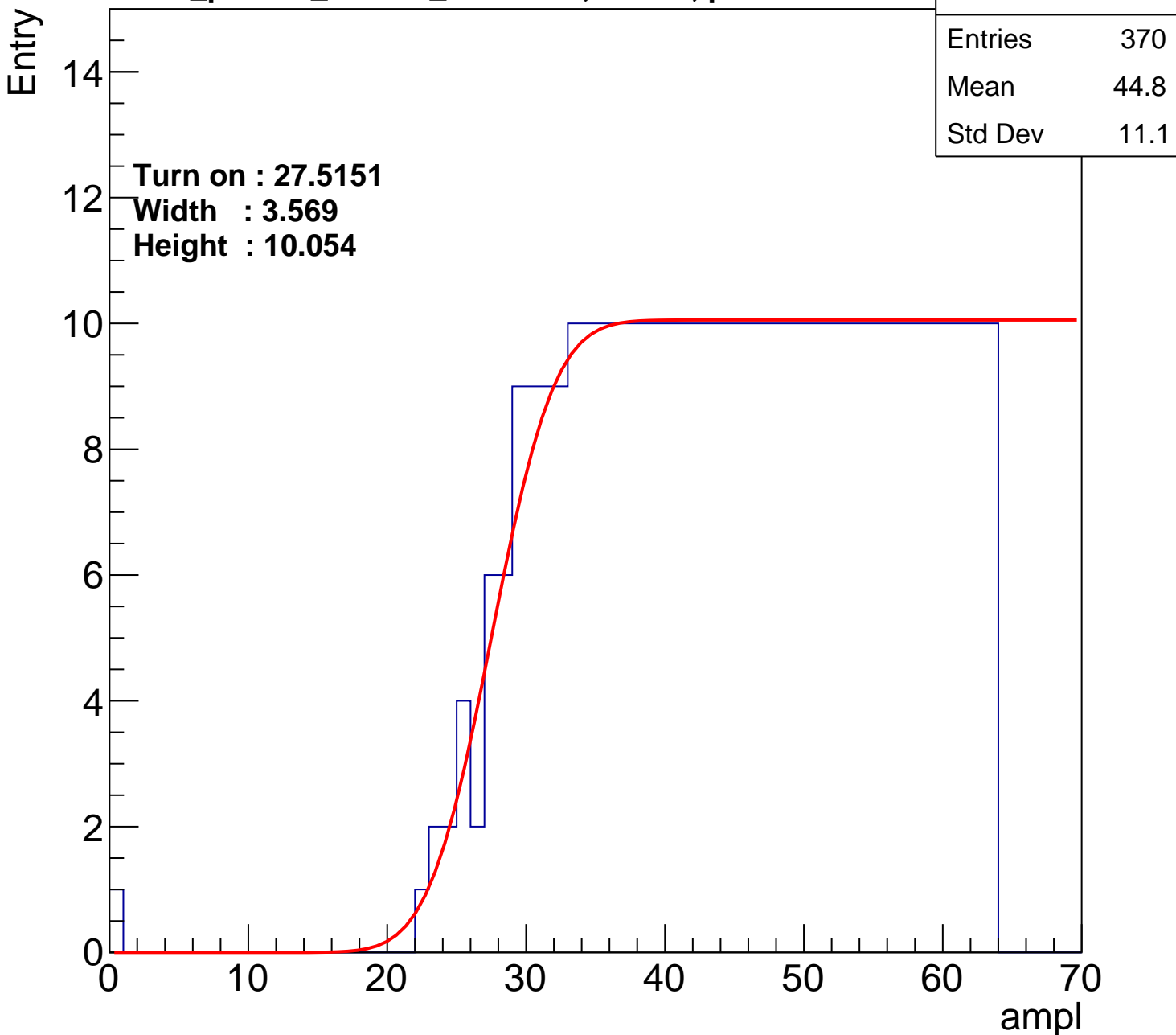
Mean	44.8
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Std Dev	11.1
---------	------

Turn on : 27.5151

Width : 3.569

Height : 10.054



B1L102S, U7-ch24

calib_packv5_042523_0143.root, FC#11, port A2

Entries	396
Mean	43.56
Std Dev	11.73

Turn on : 24.6247

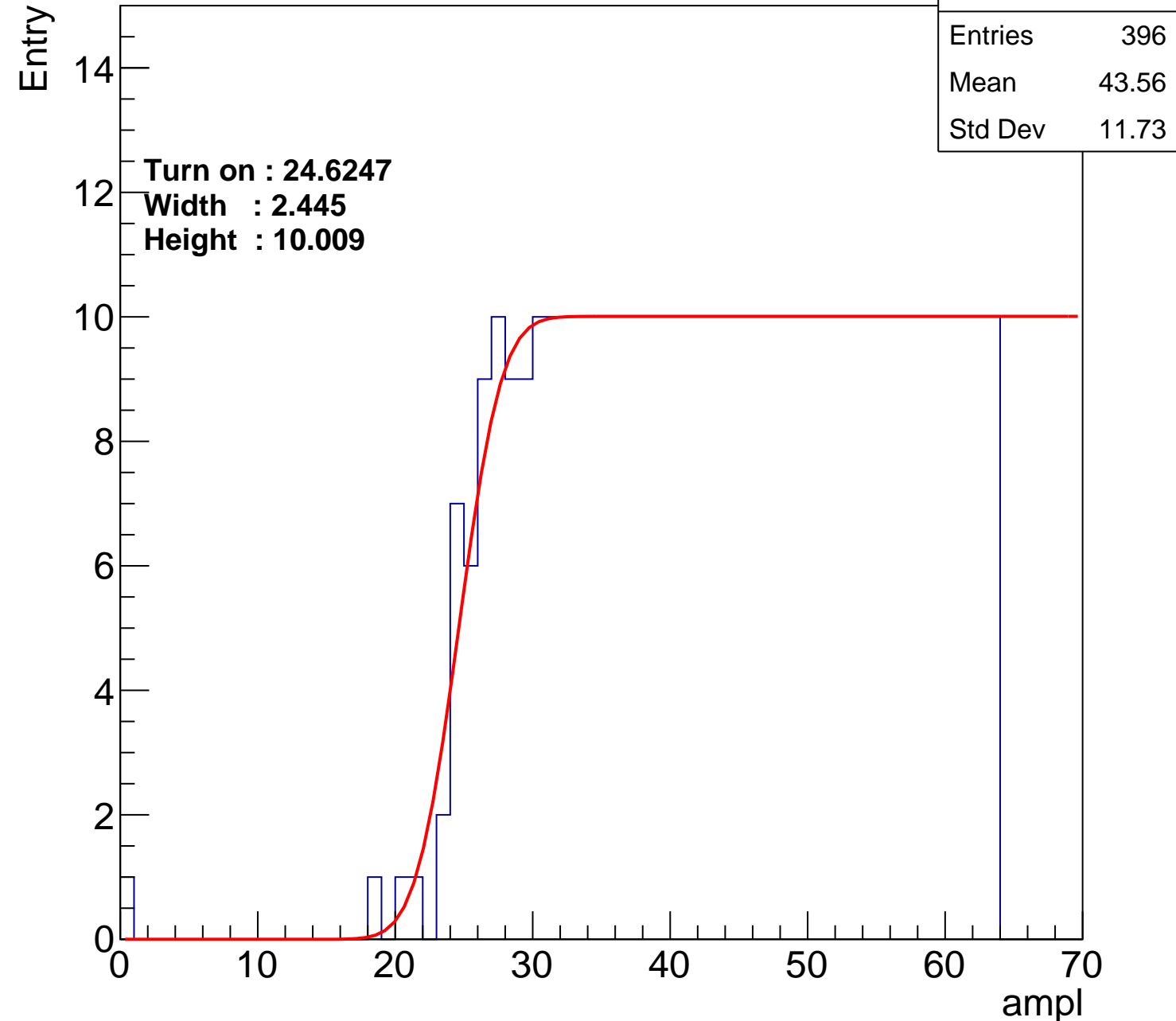
Width : 2.445

Height : 10.009

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch25

calib_packv5_042523_0143.root, FC#11, port A2

Entries	373
Mean	44.46
Std Dev	11.72

Turn on : 26.8624

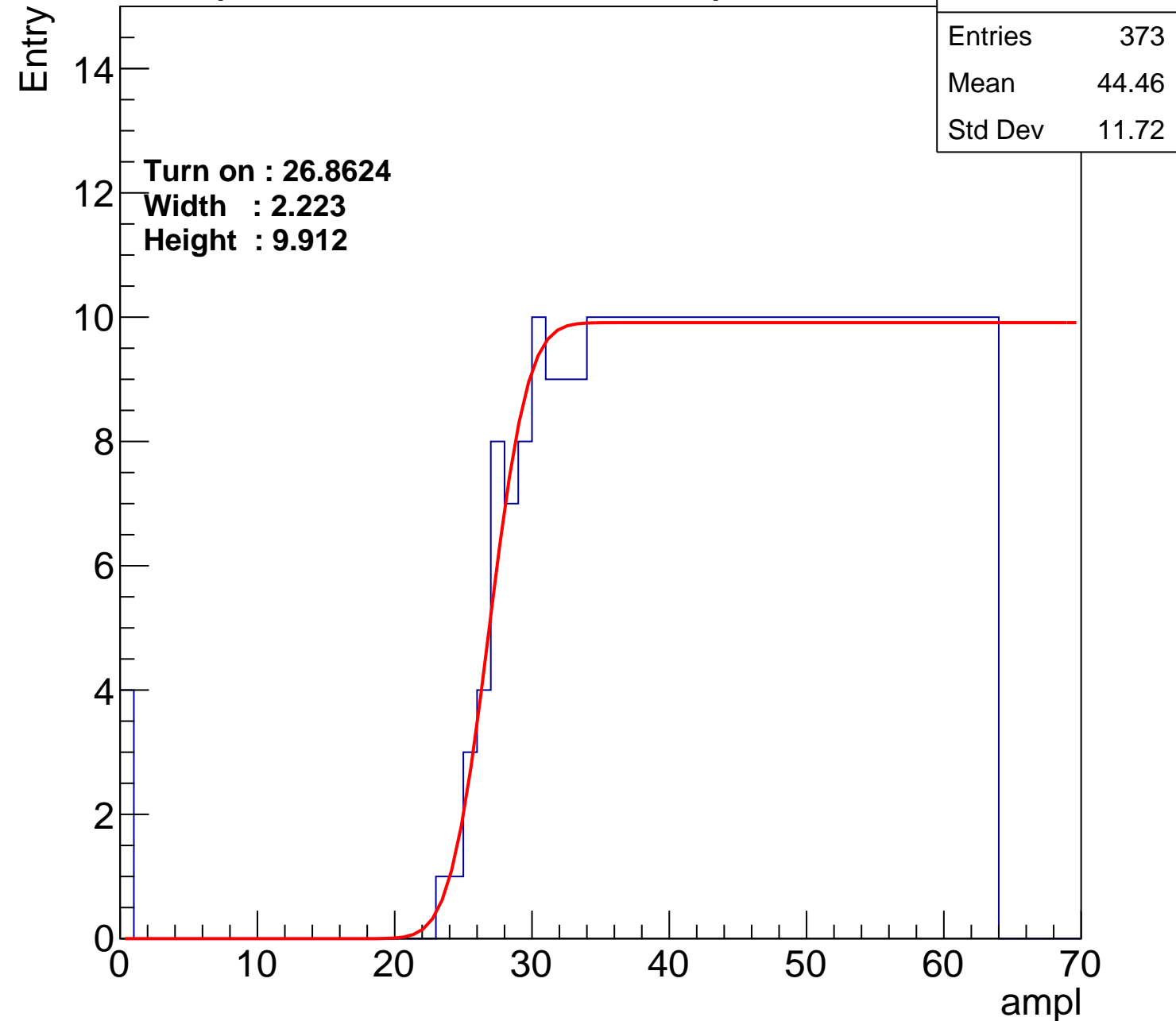
Width : 2.223

Height : 9.912

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch26

calib_packv5_042523_0143.root, FC#11, port A2

Entries	394
Mean	43.56
Std Dev	11.9

Turn on : 25.0547

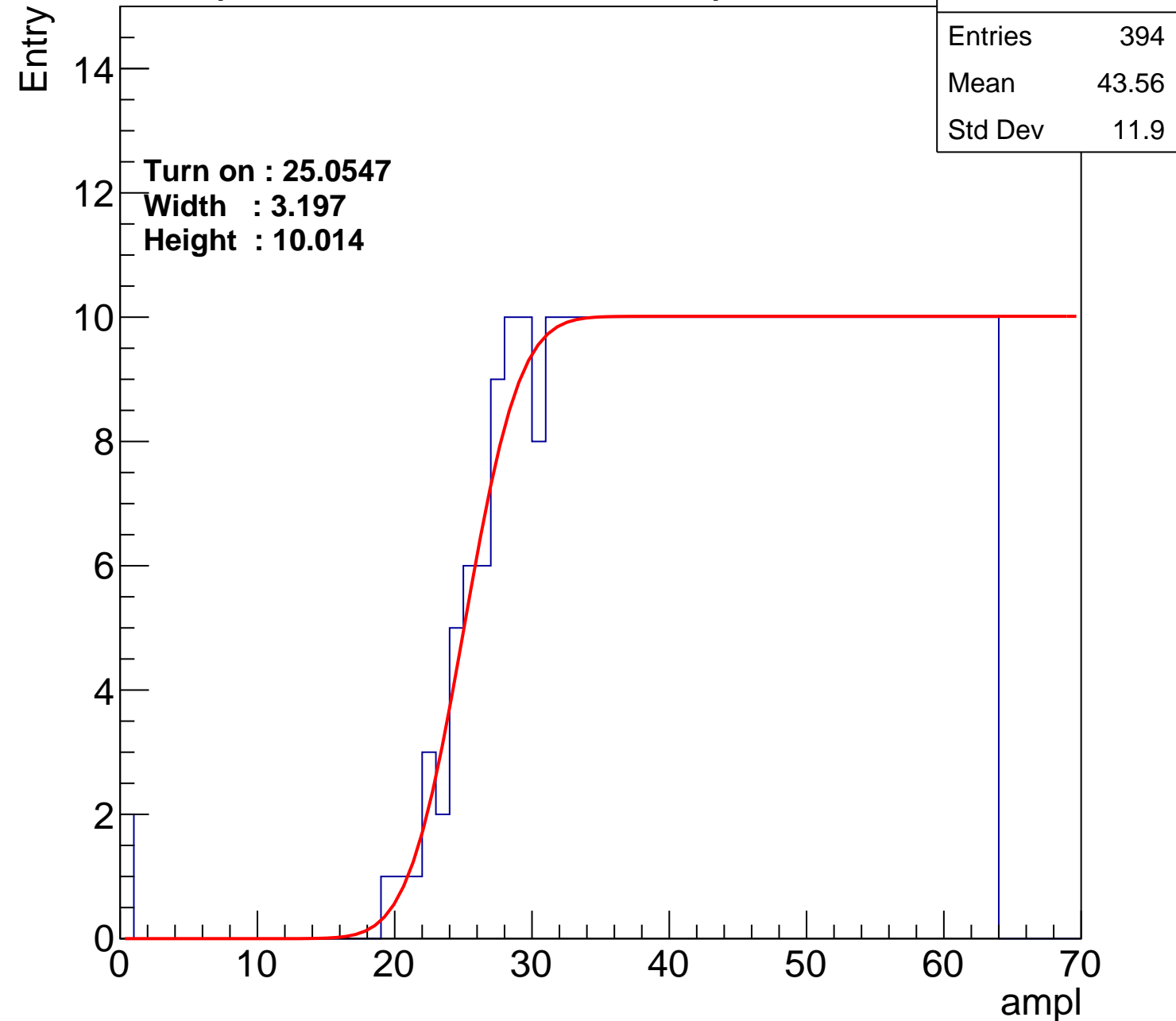
Width : 3.197

Height : 10.014

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch27

calib_packv5_042523_0143.root, FC#11, port A2

Entries	388
Mean	43.92
Std Dev	11.64

Turn on : 25.6171

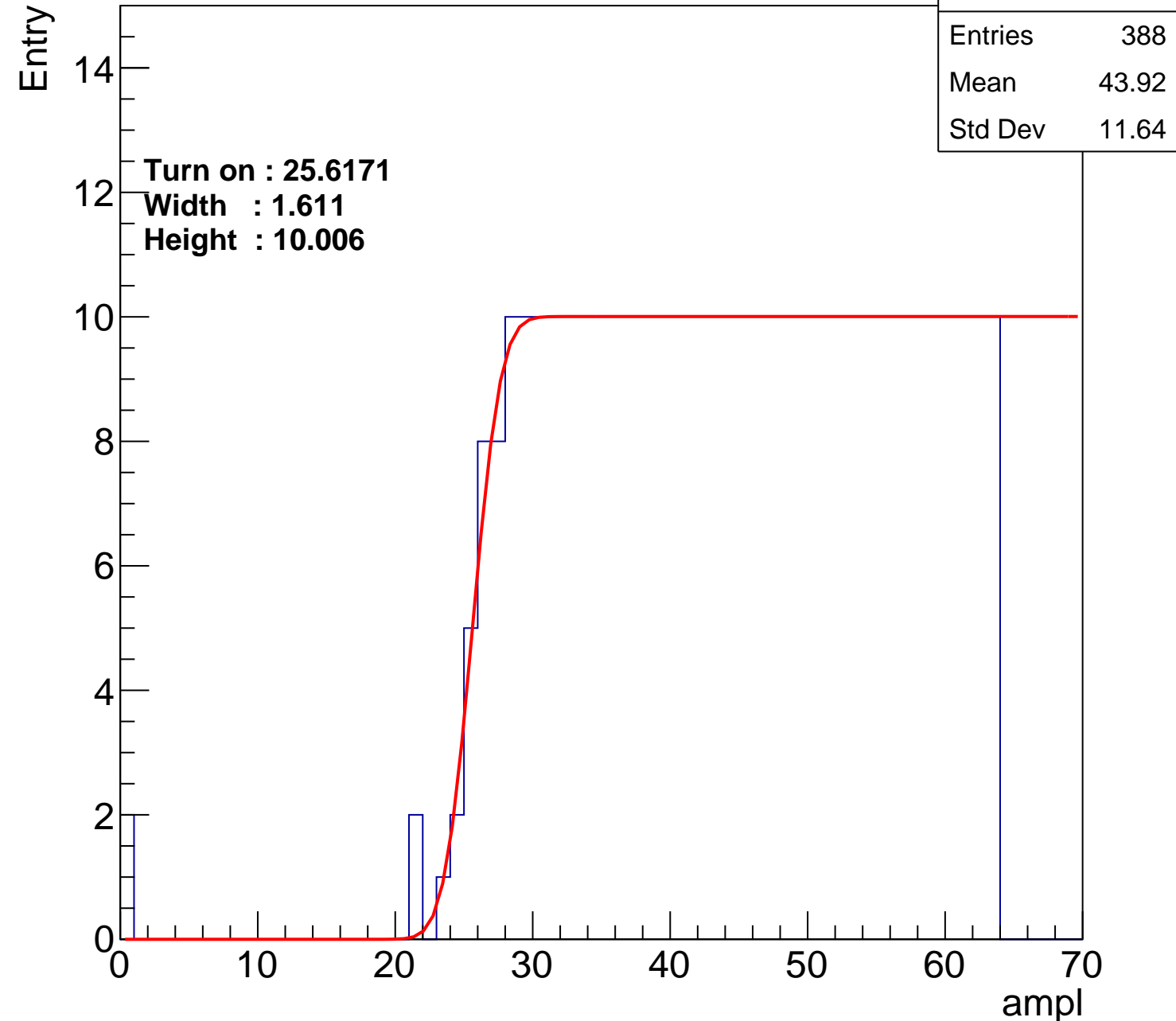
Width : 1.611

Height : 10.006

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch28

calib_packv5_042523_0143.root, FC#11, port A2

Entries	392
Mean	43.64
Std Dev	11.88

Turn on : 25.6105

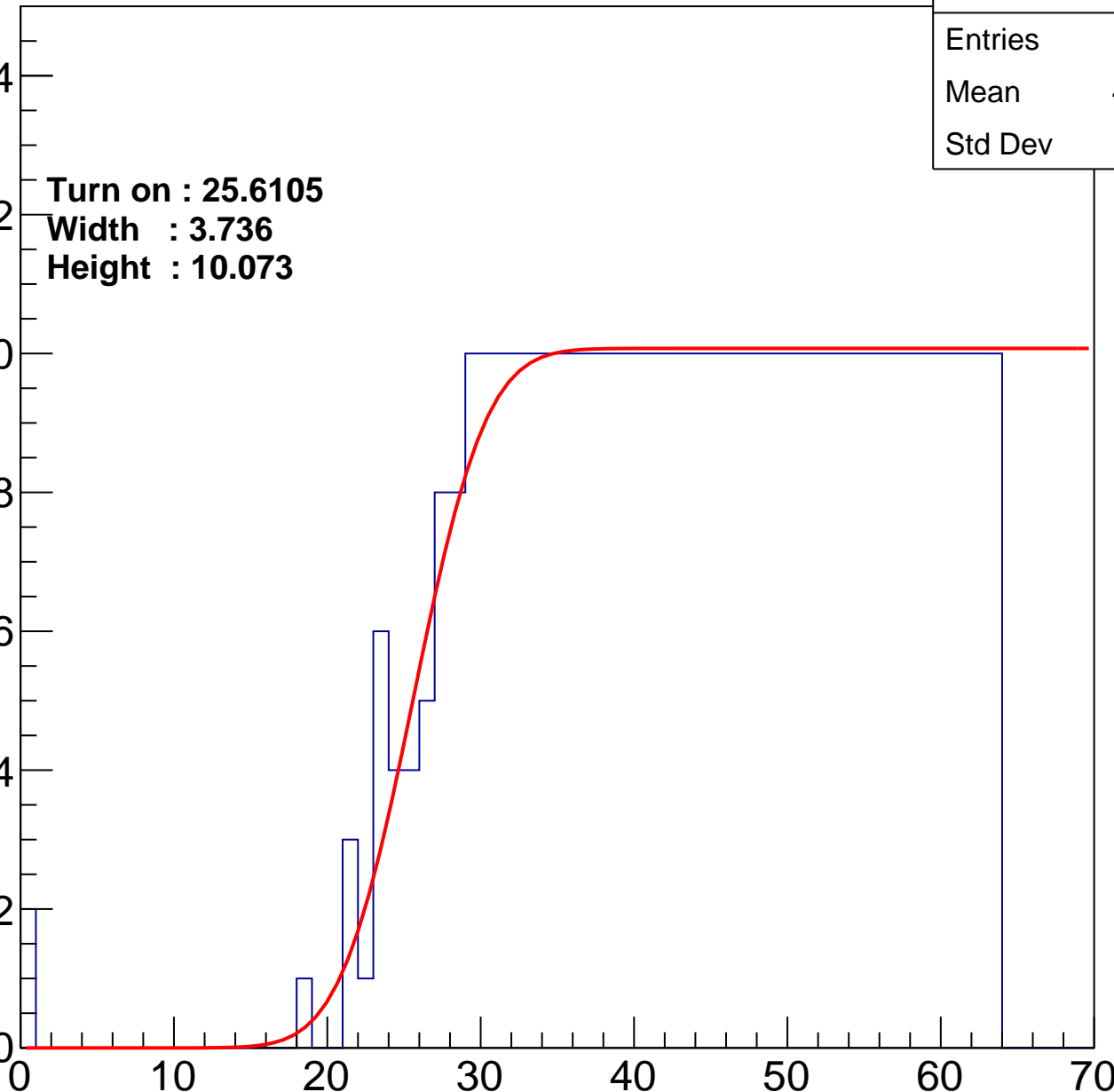
Width : 3.736

Height : 10.073

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch29

calib_packv5_042523_0143.root, FC#11, port A2

Entries	386
Mean	43.83
Std Dev	12.02

Turn on : 26.0142

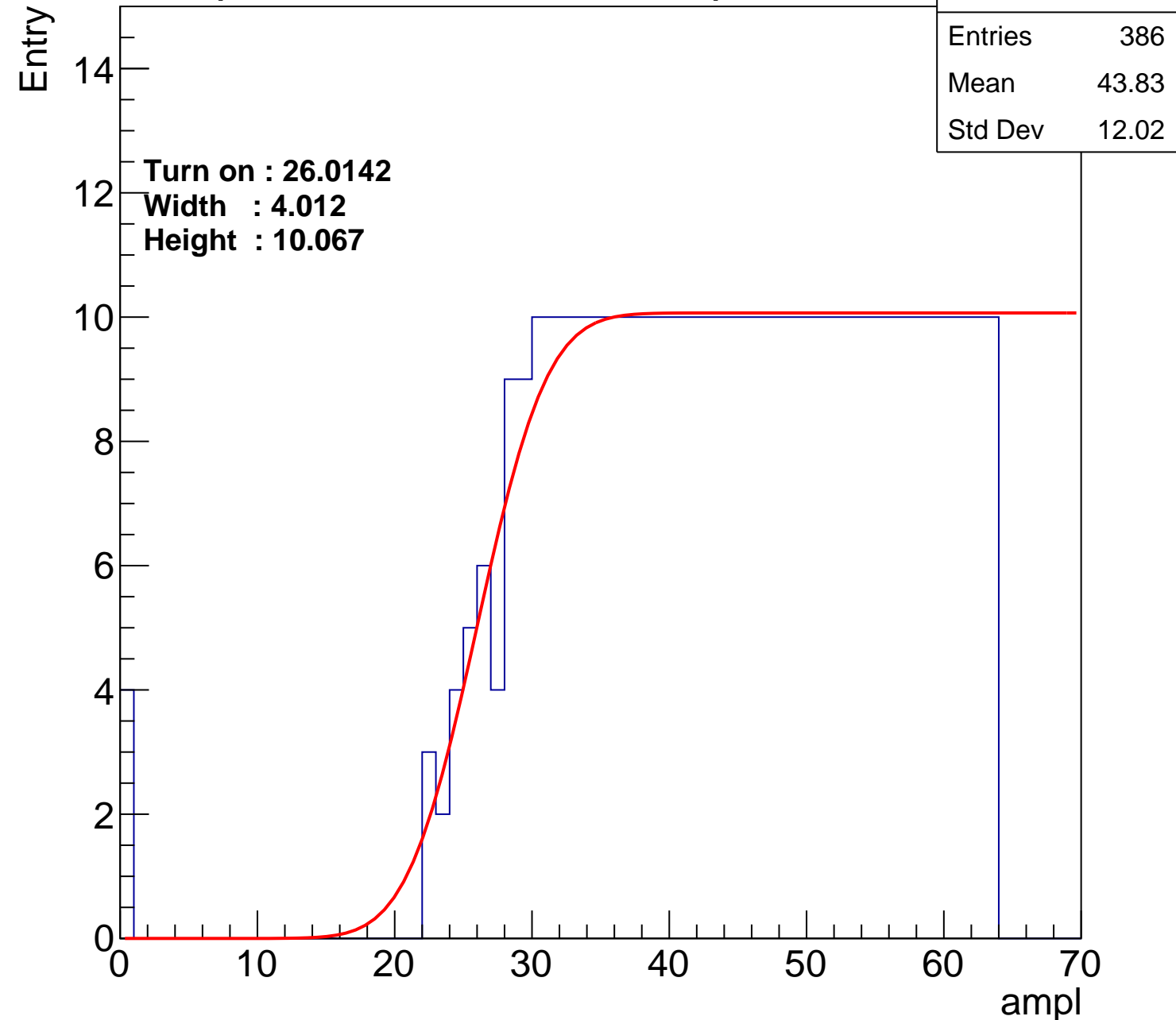
Width : 4.012

Height : 10.067

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch30

calib_packv5_042523_0143.root, FC#11, port A2

Entries	382
Mean	44.01
Std Dev	11.94

Turn on : 26.3565

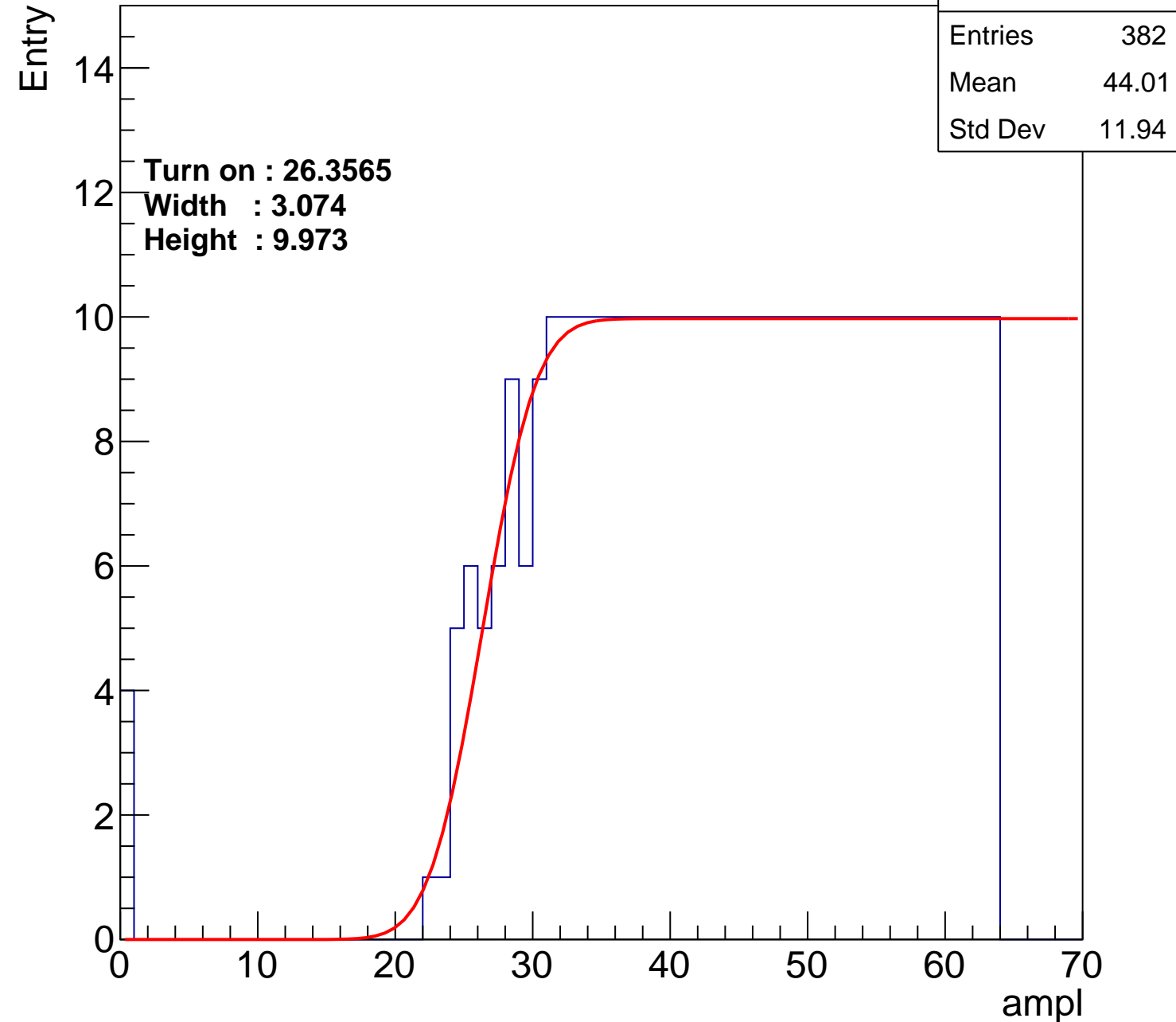
Width : 3.074

Height : 9.973

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch31

calib_packv5_042523_0143.root, FC#11, port A2

Entries	379
Mean	44.34
Std Dev	11.44

Turn on : 26.6267

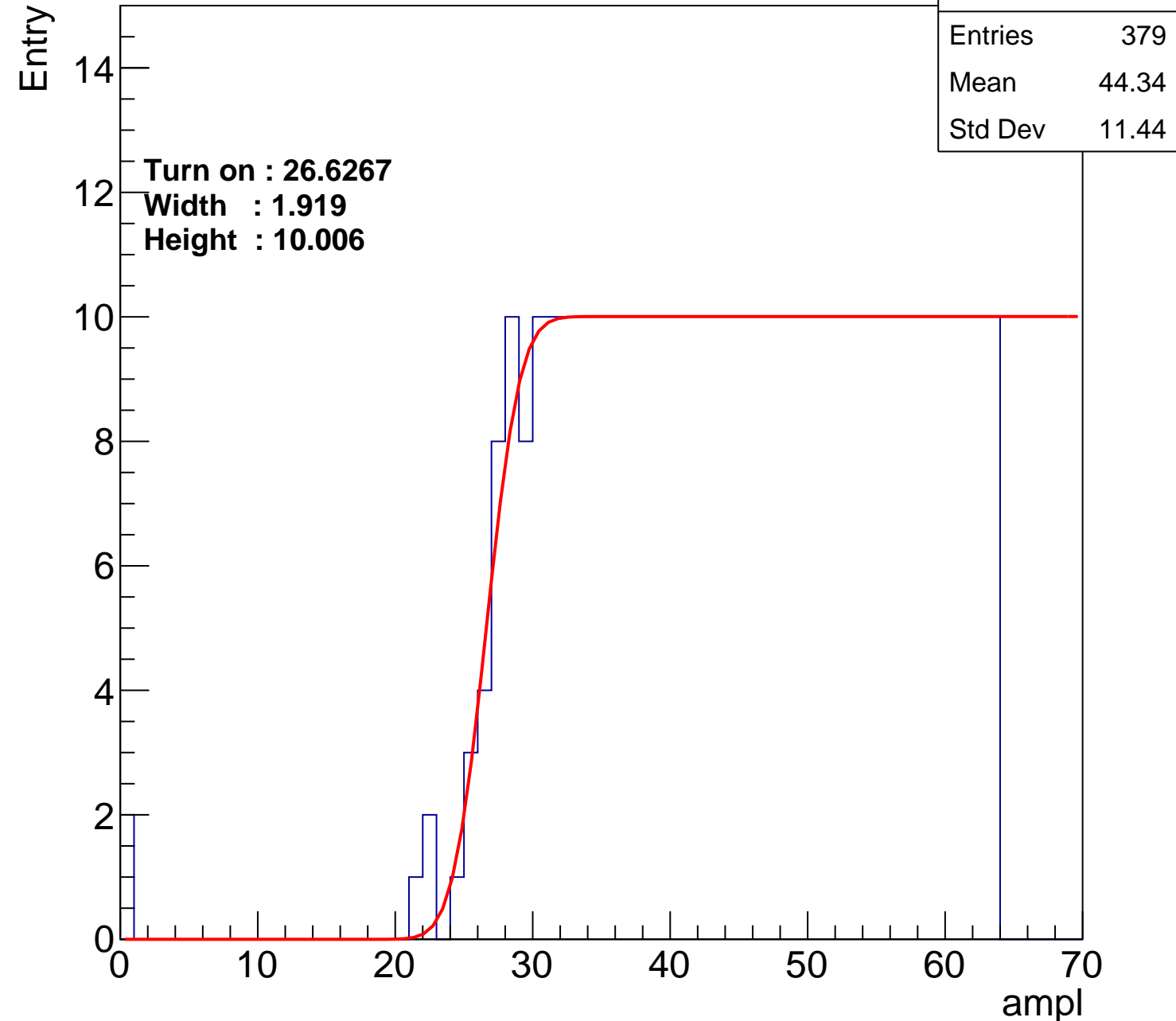
Width : 1.919

Height : 10.006

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch32

calib_packv5_042523_0143.root, FC#11, port A2

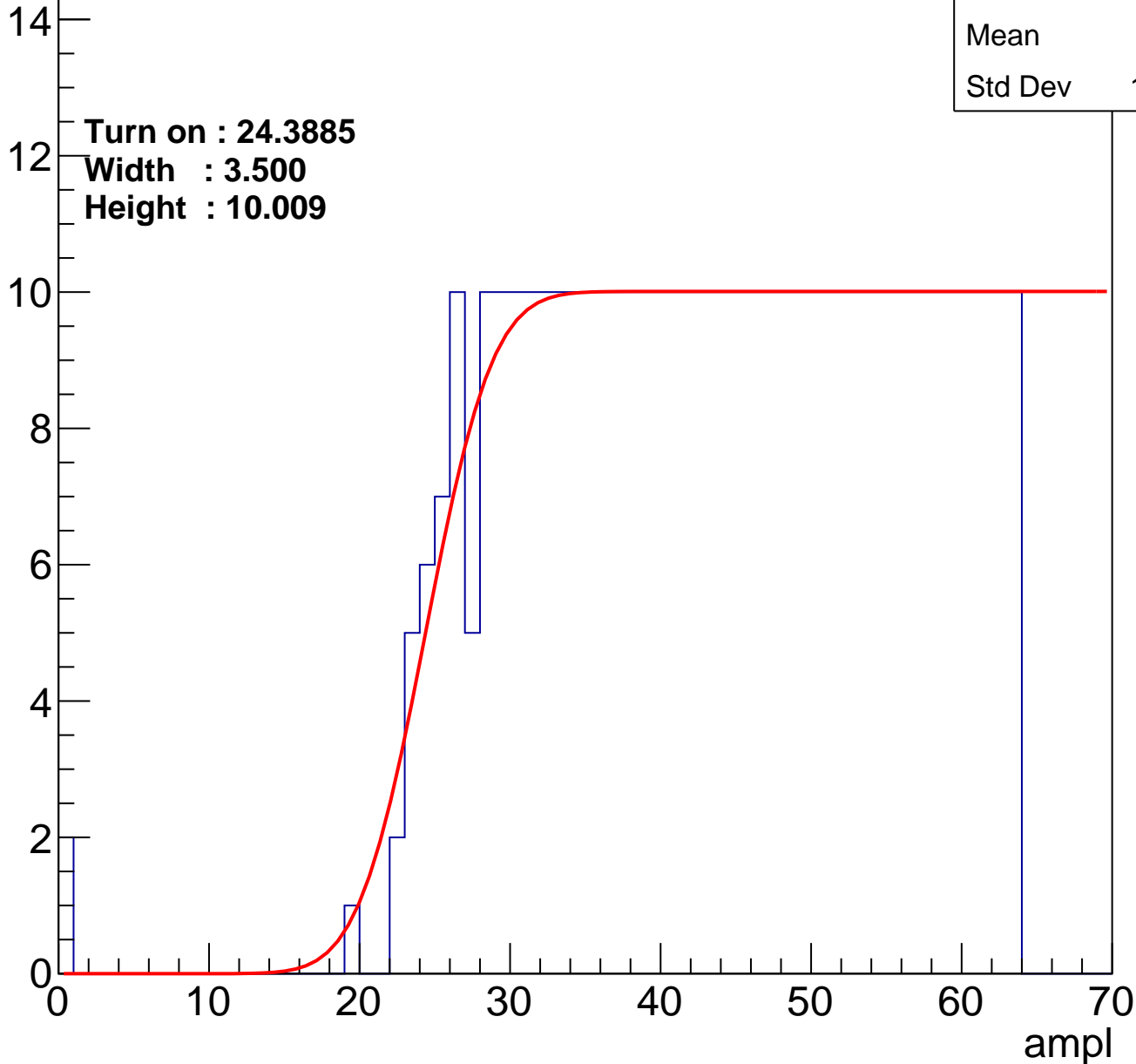
Entries	398
Mean	43.4
Std Dev	11.95

Turn on : 24.3885

Width : 3.500

Height : 10.009

Entry



B1L102S, U7-ch33

calib_packv5_042523_0143.root, FC#11, port A2

Entries	381
Mean	44.15
Std Dev	11.63

Turn on : 26.5796

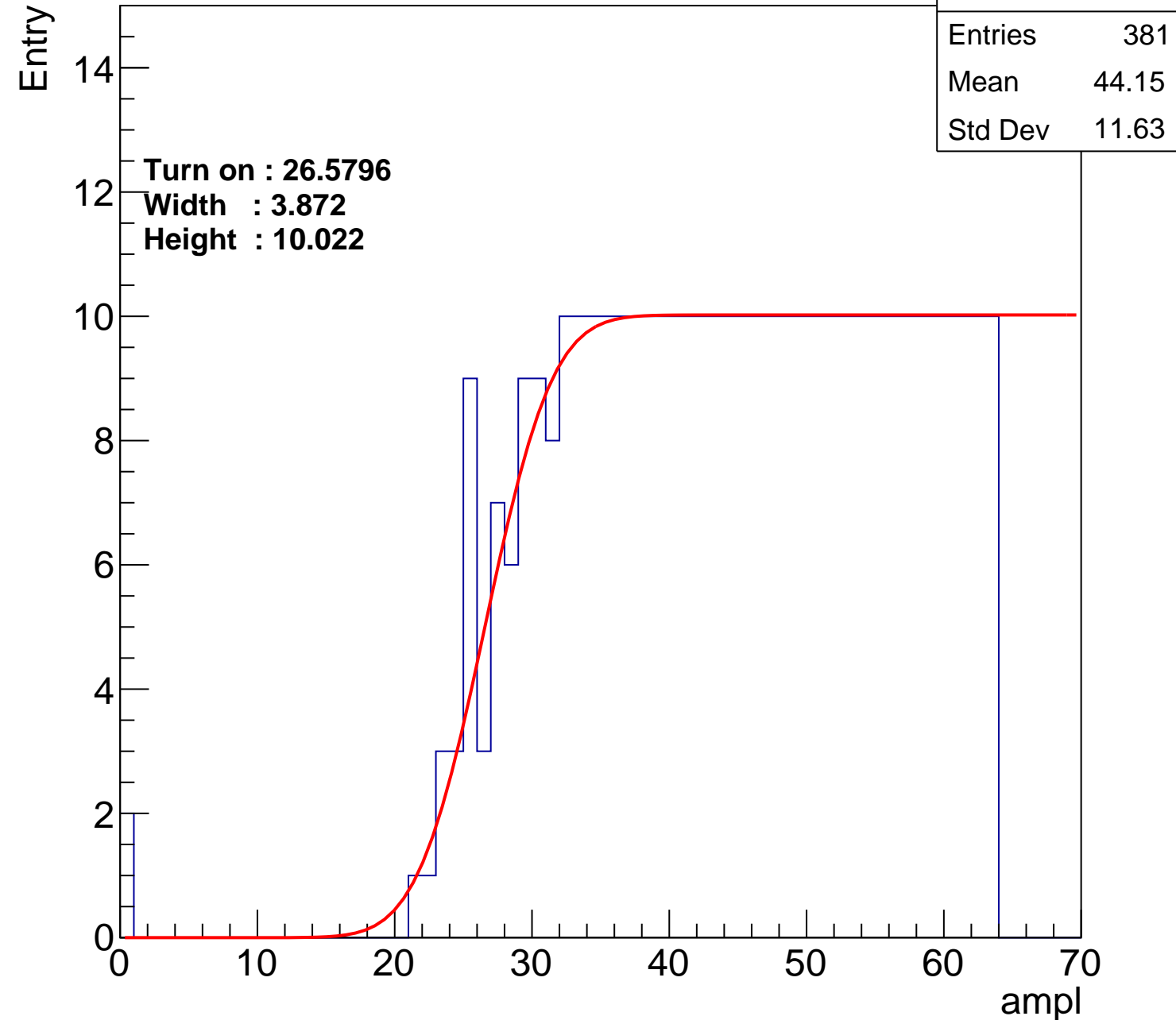
Width : 3.872

Height : 10.022

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch34

calib_packv5_042523_0143.root, FC#11, port A2

Entries	418
Mean	42.31
Std Dev	12.73

Turn on : 22.5952

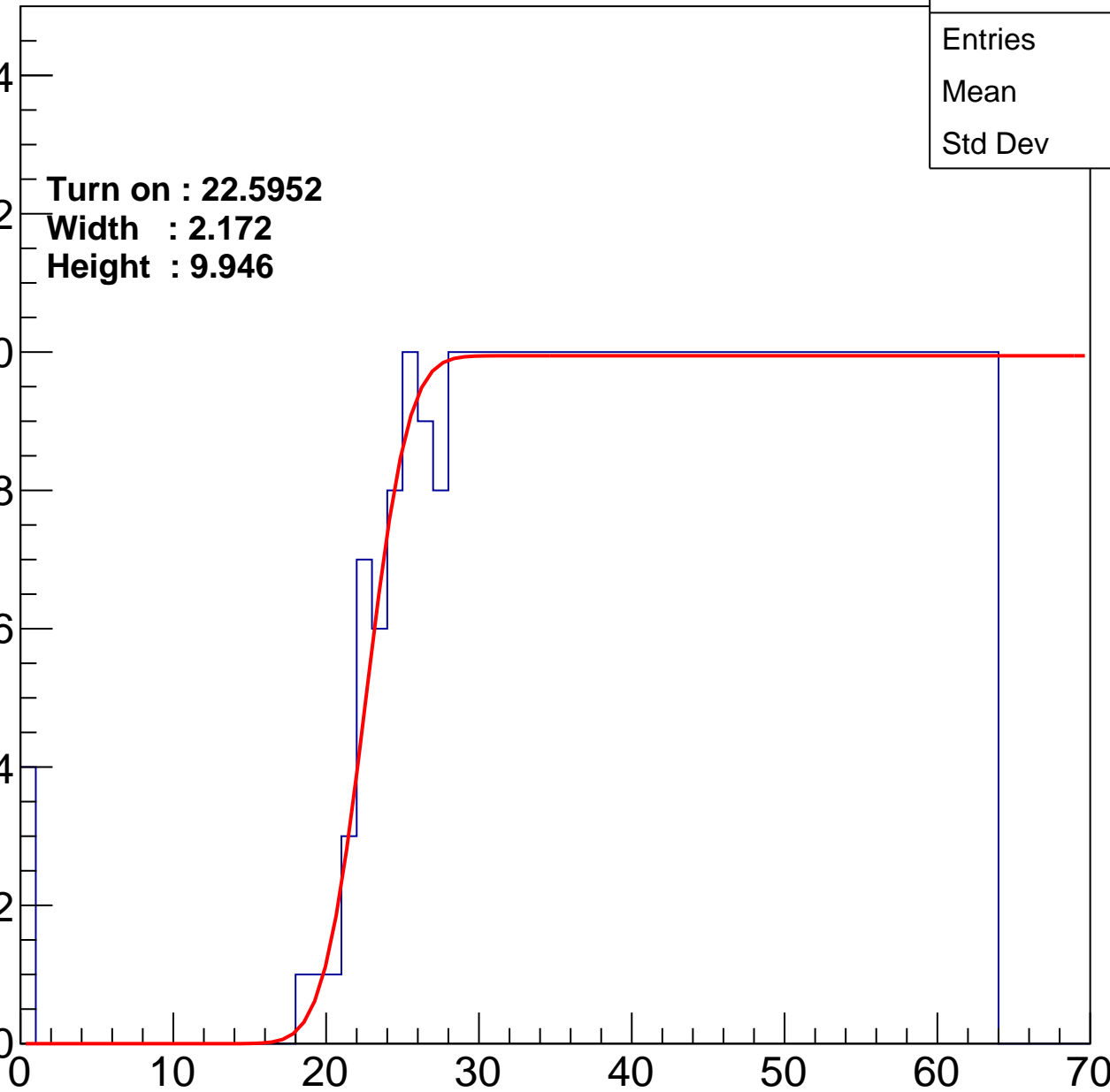
Width : 2.172

Height : 9.946

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch35

calib_packv5_042523_0143.root, FC#11, port A2

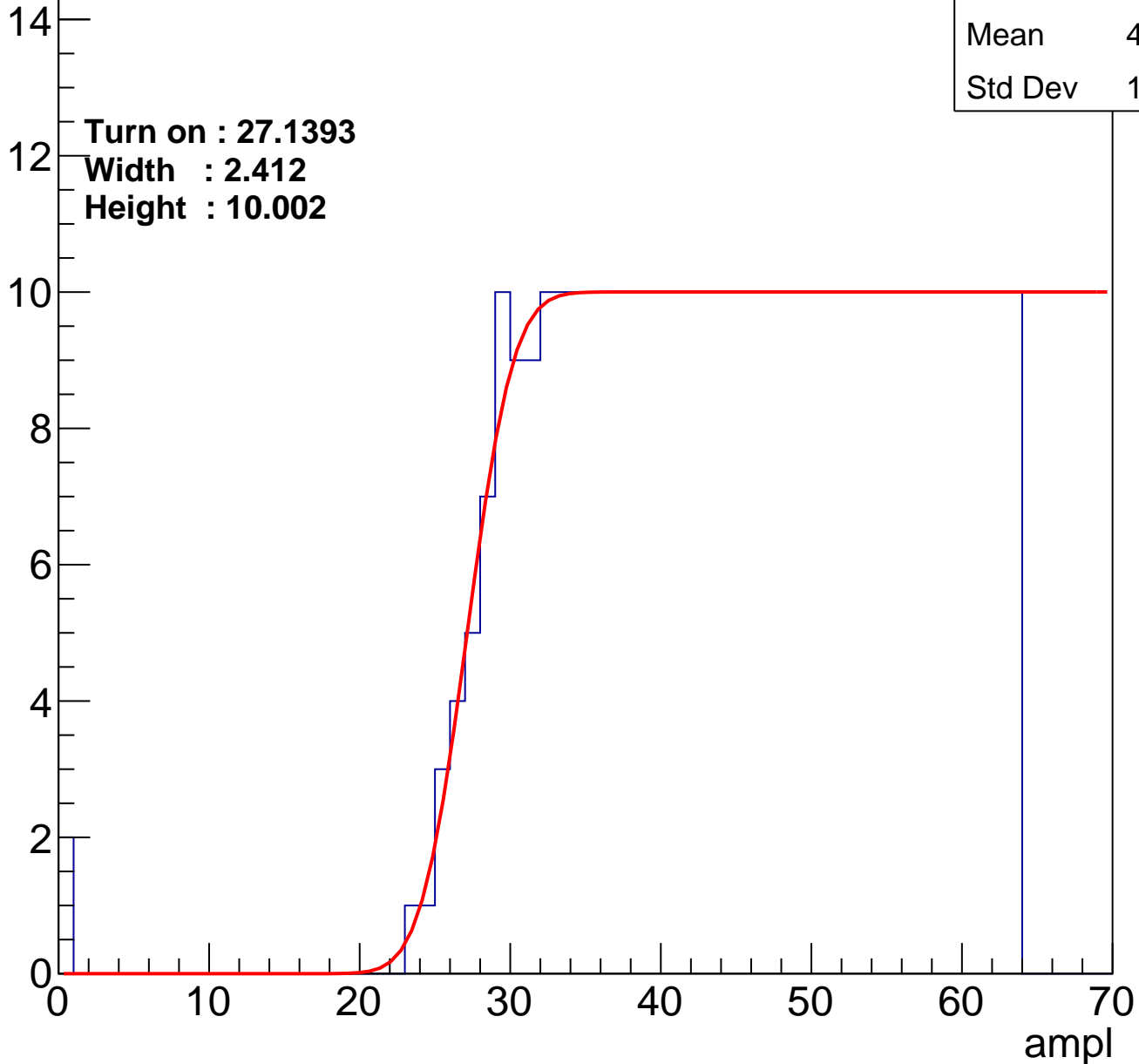
Entries	371
Mean	44.73
Std Dev	11.24

Turn on : 27.1393

Width : 2.412

Height : 10.002

Entry



B1L102S, U7-ch36

calib_packv5_042523_0143.root, FC#11, port A2

Entries	362
Mean	45.16
Std Dev	11.04

Turn on : 28.9170

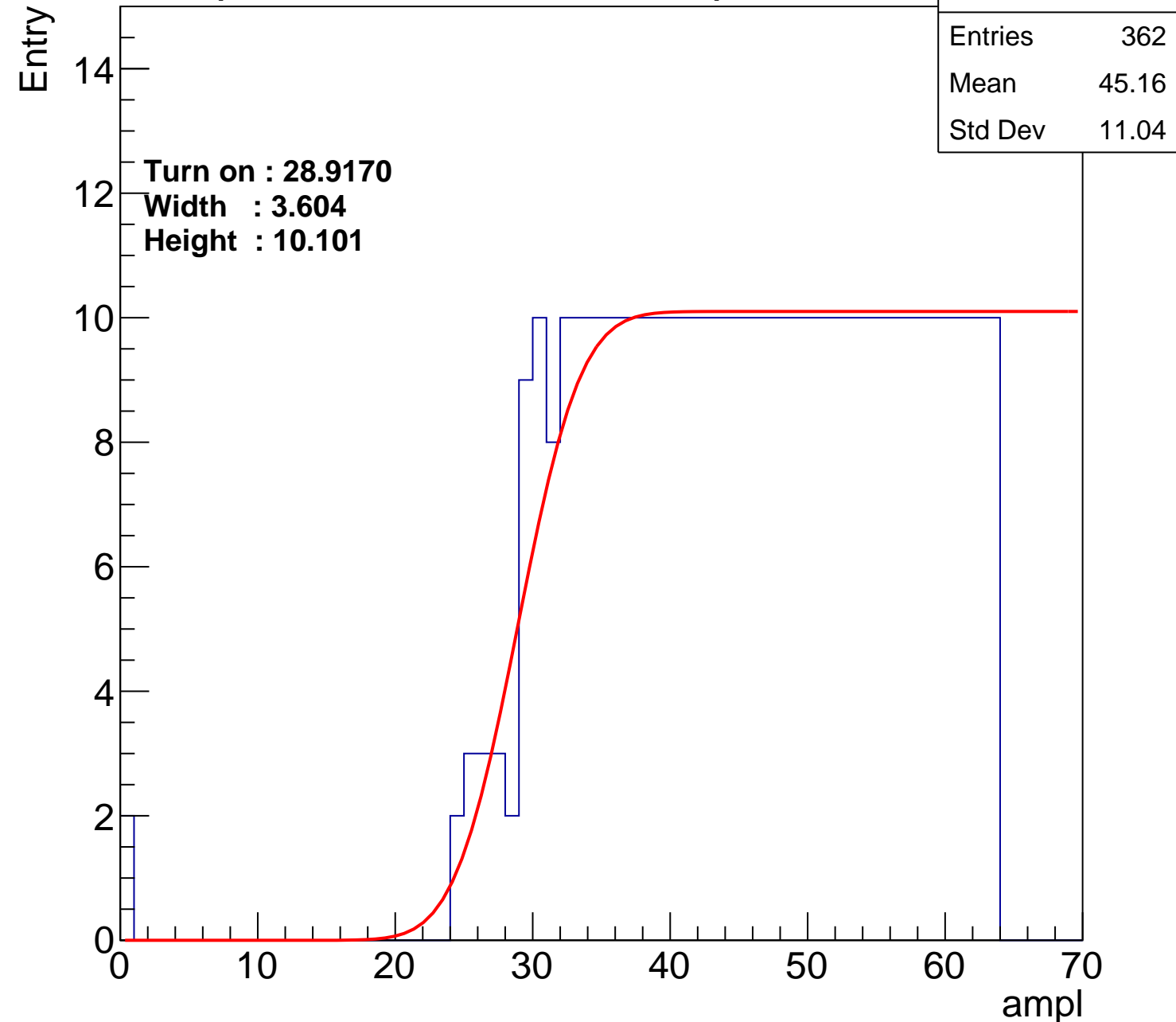
Width : 3.604

Height : 10.101

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch37

calib_packv5_042523_0143.root, FC#11, port A2

Entries	381
Mean	44.21
Std Dev	11.55

Turn on : 26.4462

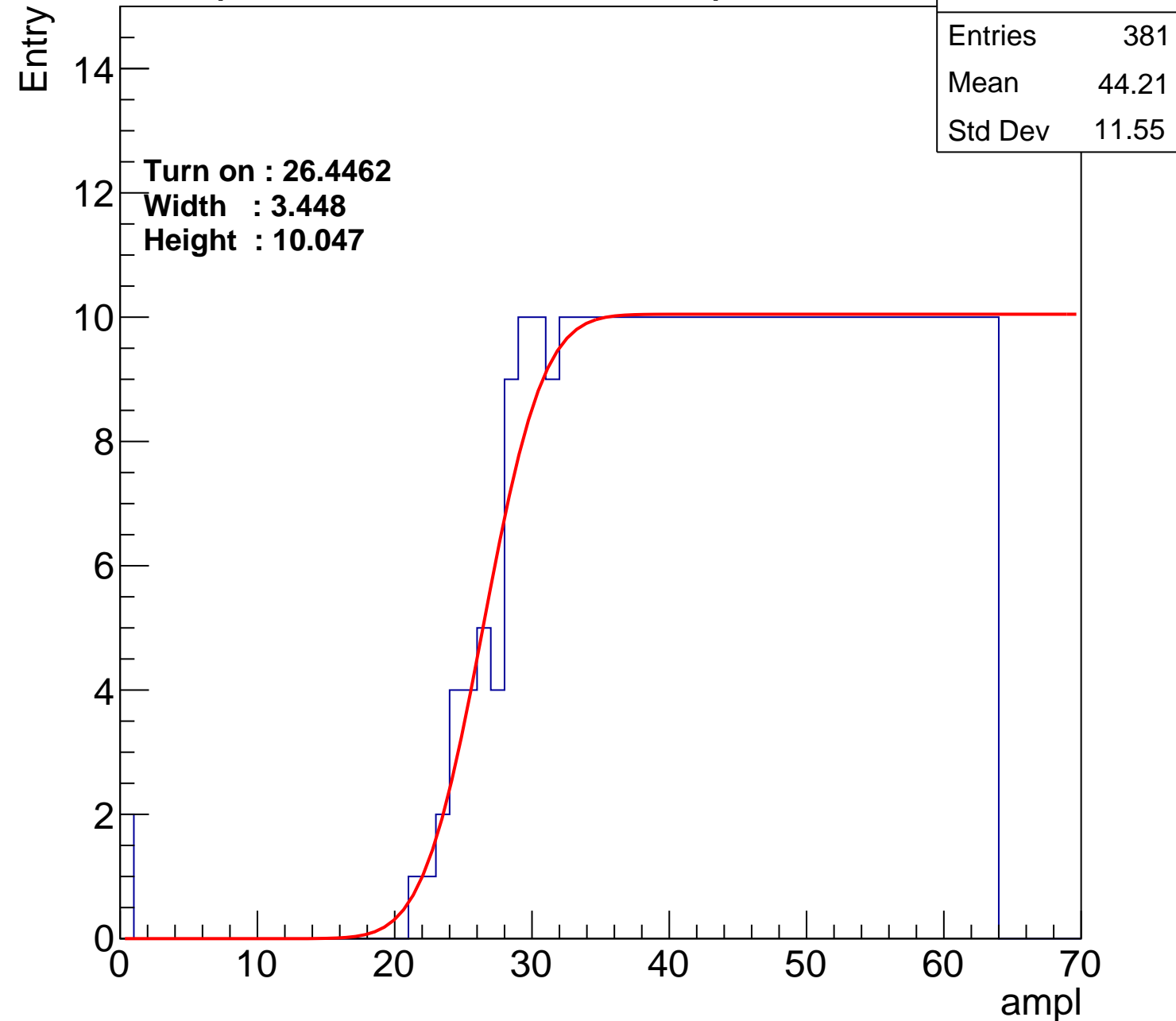
Width : 3.448

Height : 10.047

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch38

calib_packv5_042523_0143.root, FC#11, port A2

Entries	381
Mean	44.11
Std Dev	11.78

Turn on : 26.5525

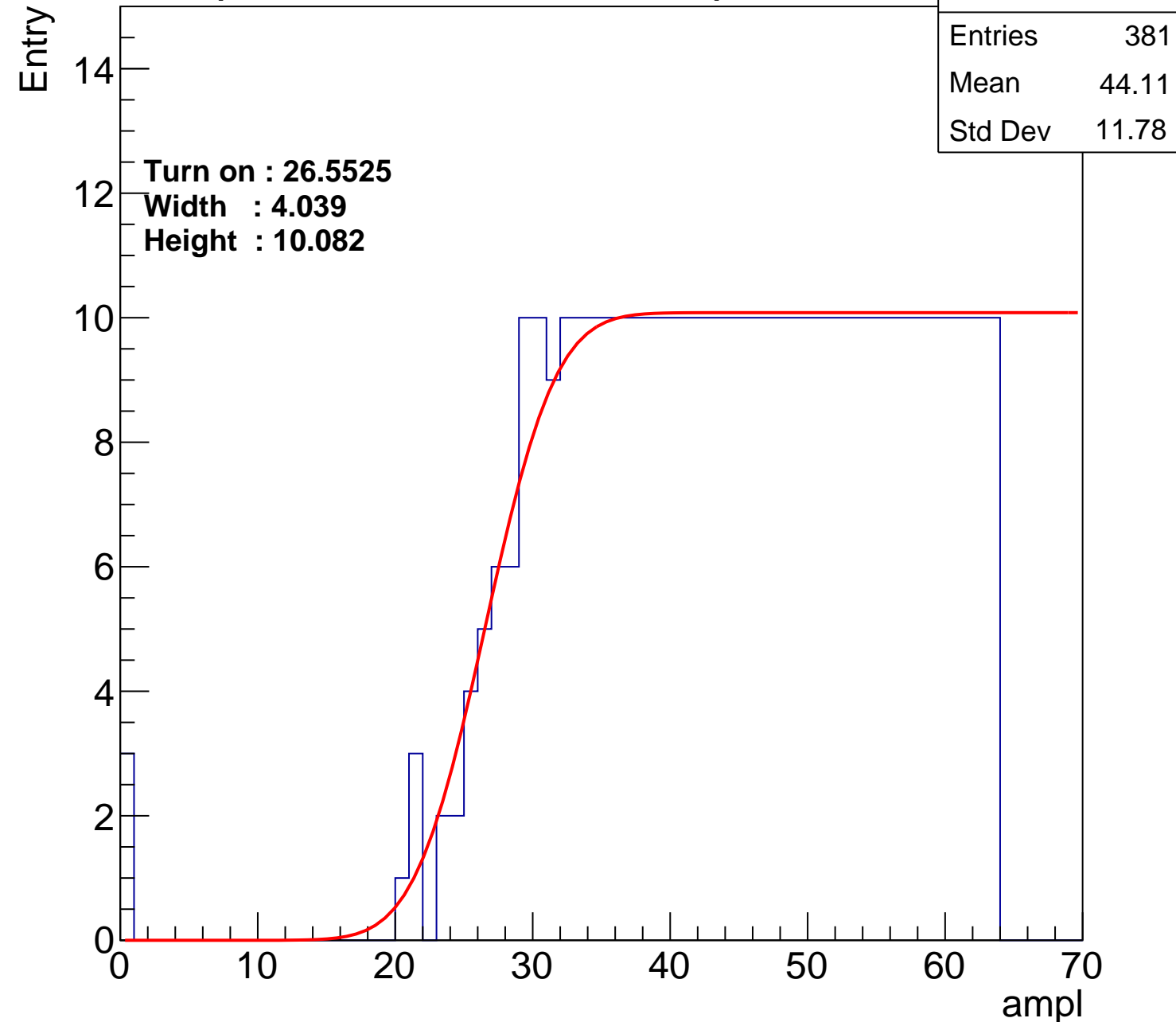
Width : 4.039

Height : 10.082

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch39

calib_packv5_042523_0143.root, FC#11, port A2

Entries	387
Mean	43.83
Std Dev	11.89

Turn on : 25.6159

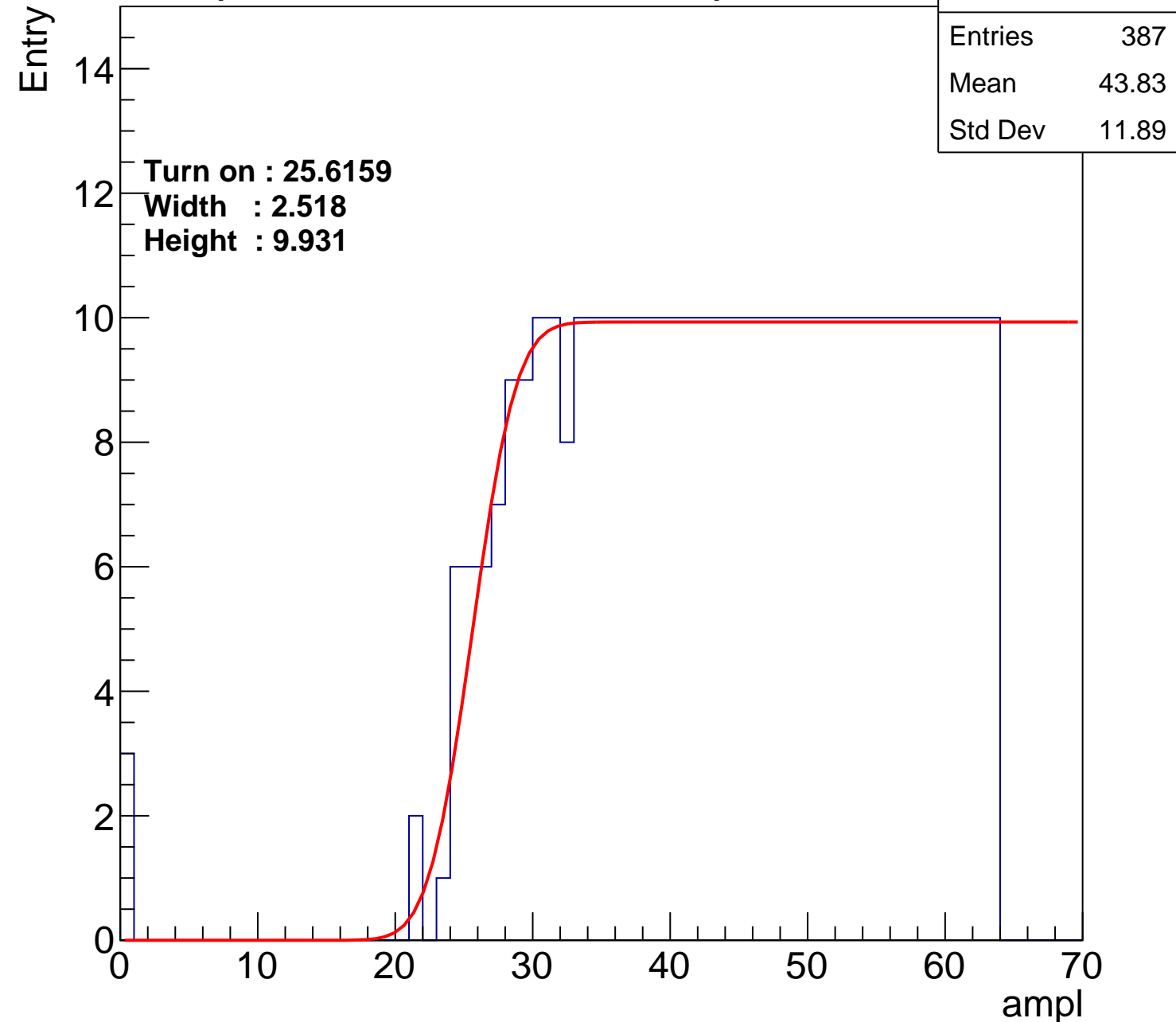
Width : 2.518

Height : 9.931

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch40

calib_packv5_042523_0143.root, FC#11, port A2

Entries	384
Mean	44.14
Std Dev	11.42

Turn on : 25.8280

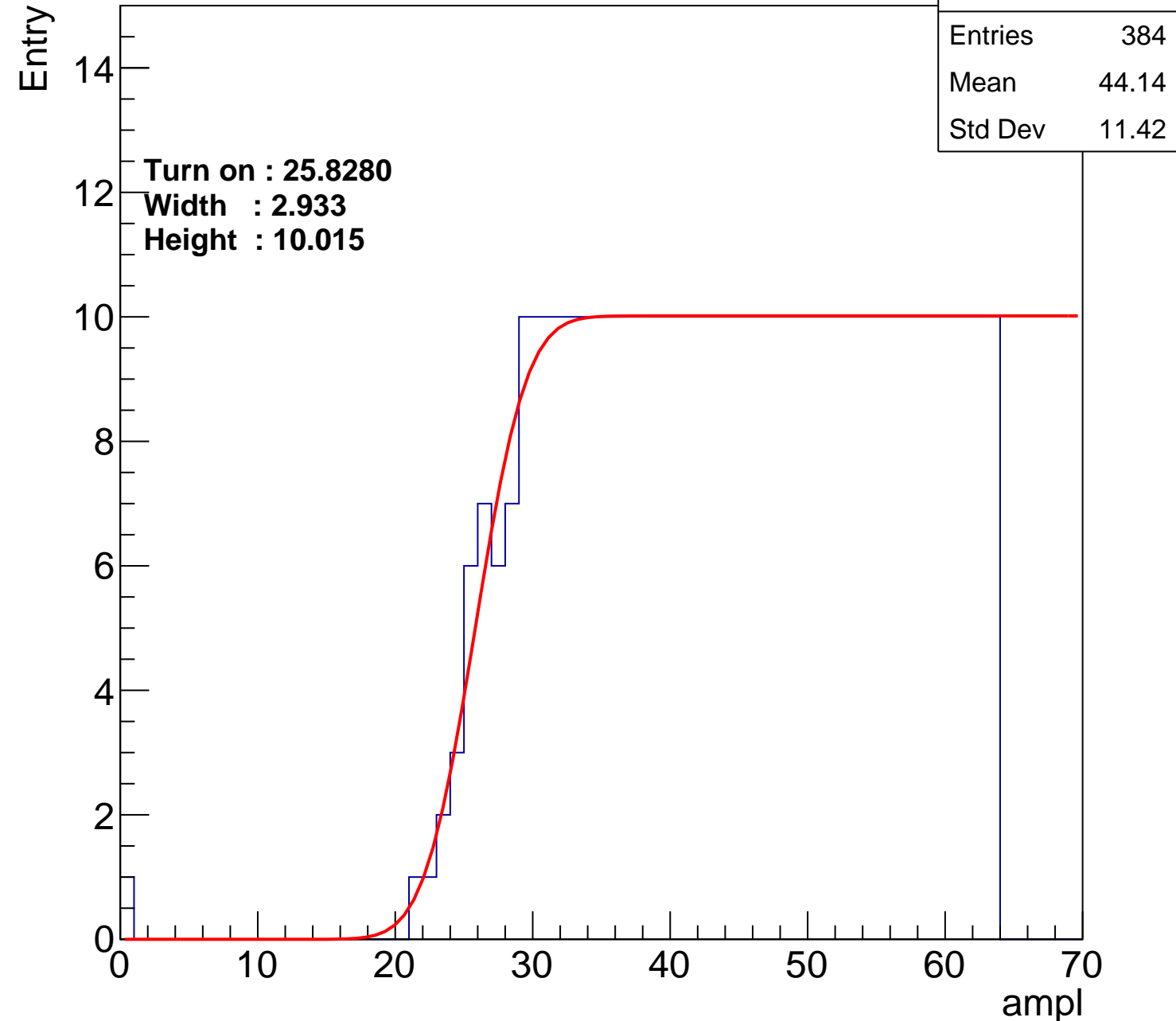
Width : 2.933

Height : 10.015

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch41

calib_packv5_042523_0143.root, FC#11, port A2

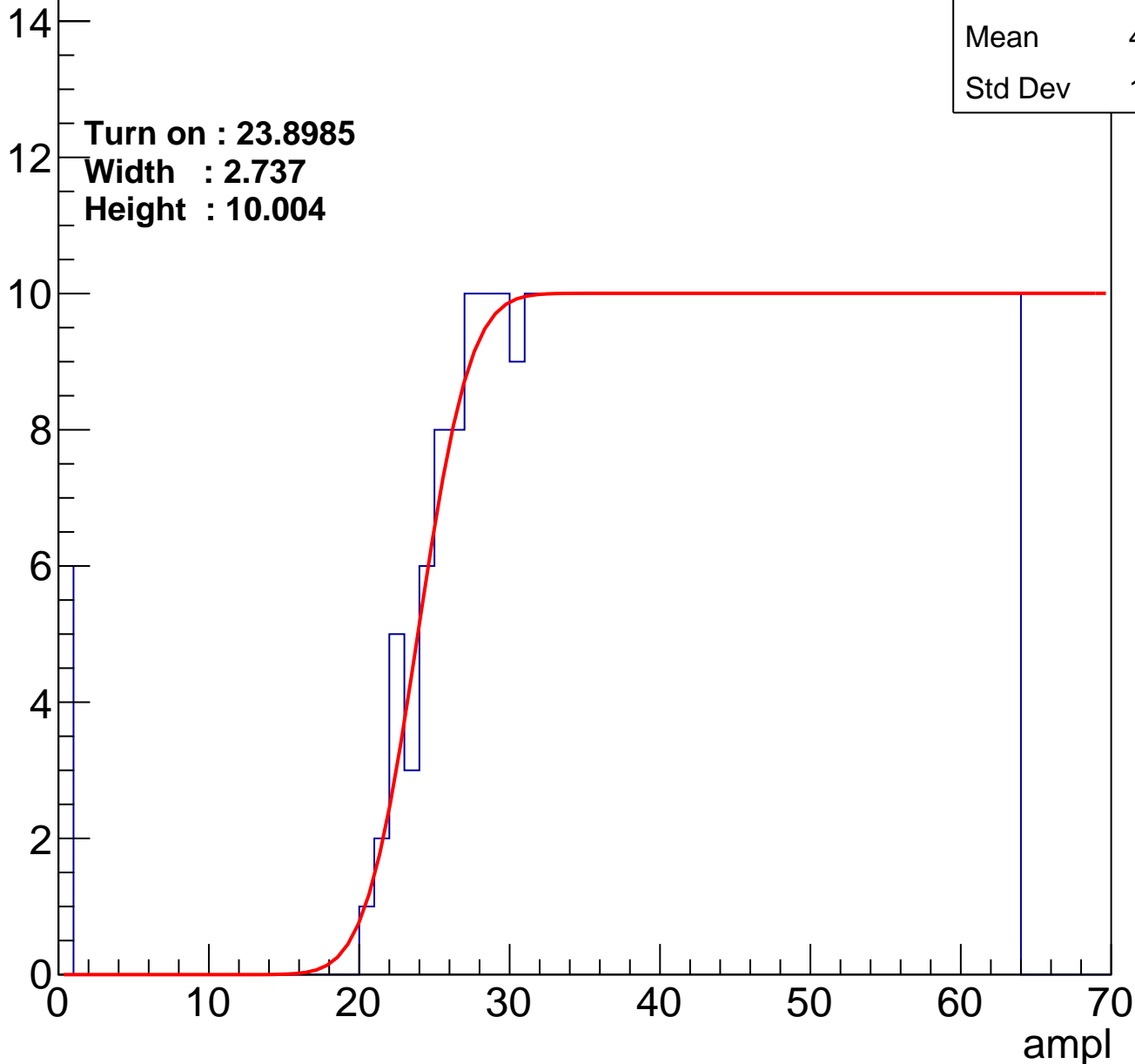
Entries	408
Mean	42.68
Std Dev	12.77

Turn on : 23.8985

Width : 2.737

Height : 10.004

Entry



B1L102S, U7-ch42

calib_packv5_042523_0143.root, FC#11, port A2

Entries	389
Mean	43.82
Std Dev	11.74

Turn on : 25.4811

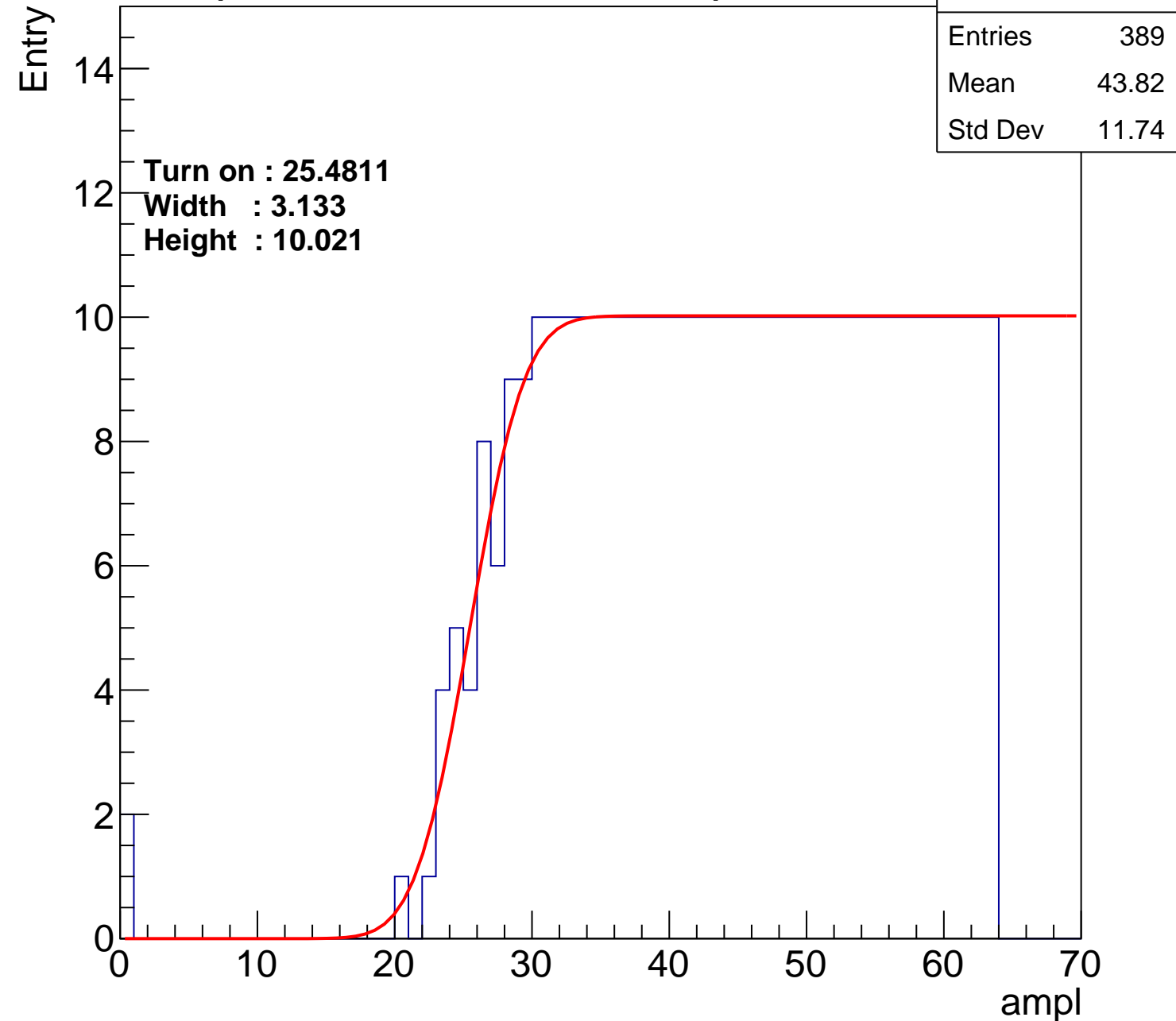
Width : 3.133

Height : 10.021

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch43

calib_packv5_042523_0143.root, FC#11, port A2

Entries	372
Mean	44.55
Std Dev	11.65

Turn on : 27.1953

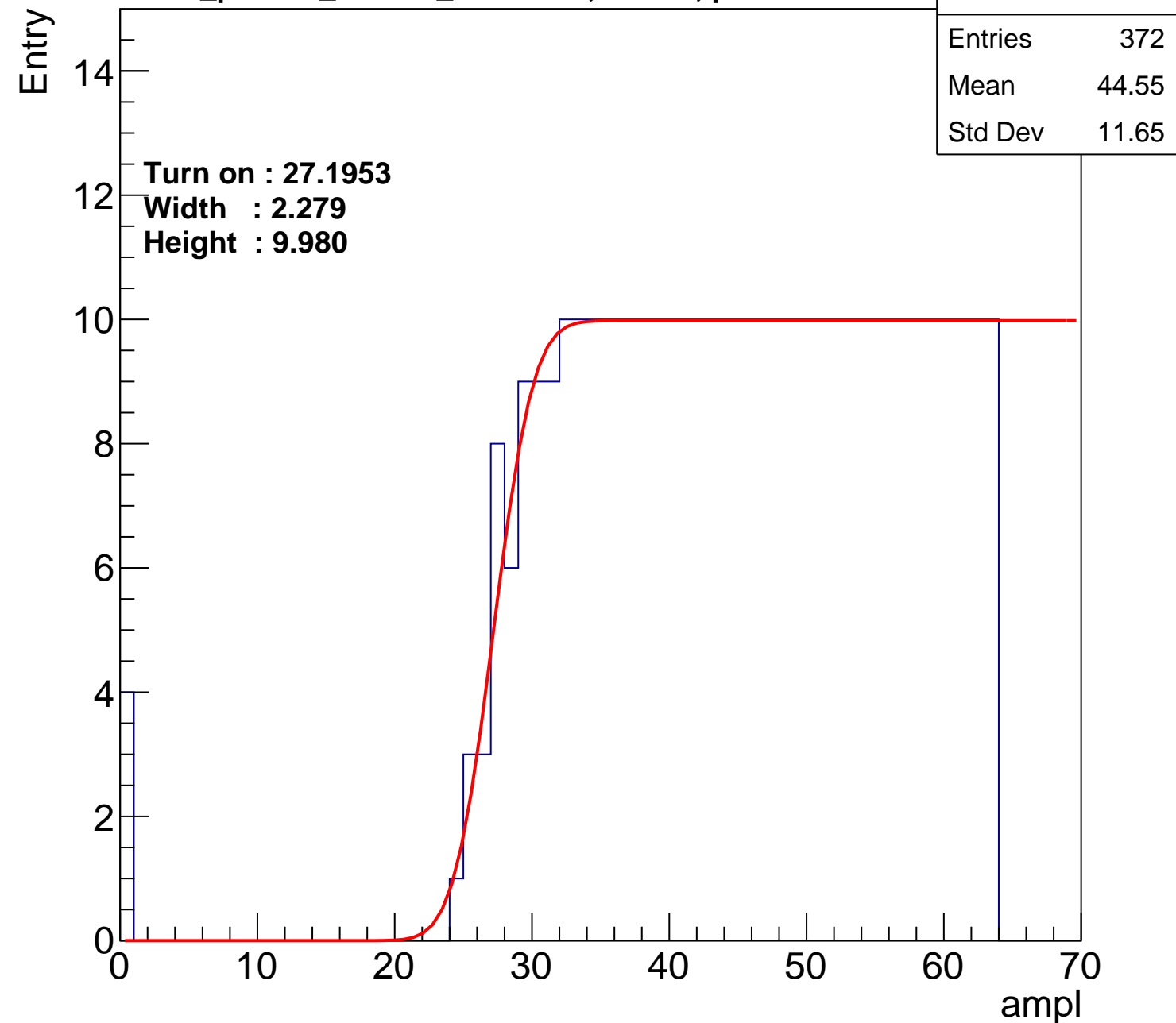
Width : 2.279

Height : 9.980

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch44

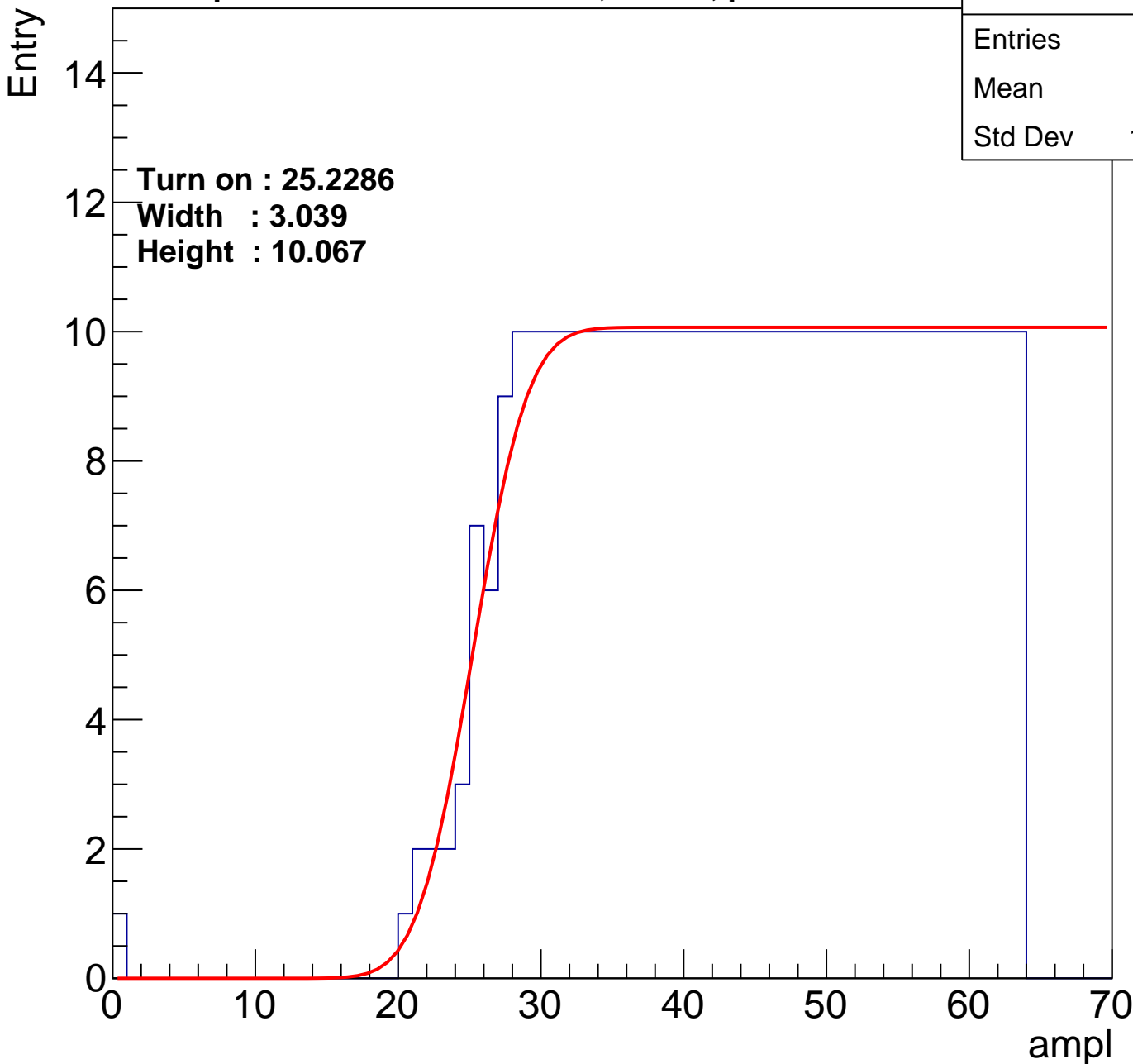
calib_packv5_042523_0143.root, FC#11, port A2

Entries	393
Mean	43.71
Std Dev	11.65

Turn on : 25.2286

Width : 3.039

Height : 10.067



B1L102S, U7-ch45

calib_packv5_042523_0143.root, FC#11, port A2

Entries	367
Mean	44.96
Std Dev	10.99

Turn on : 27.4818

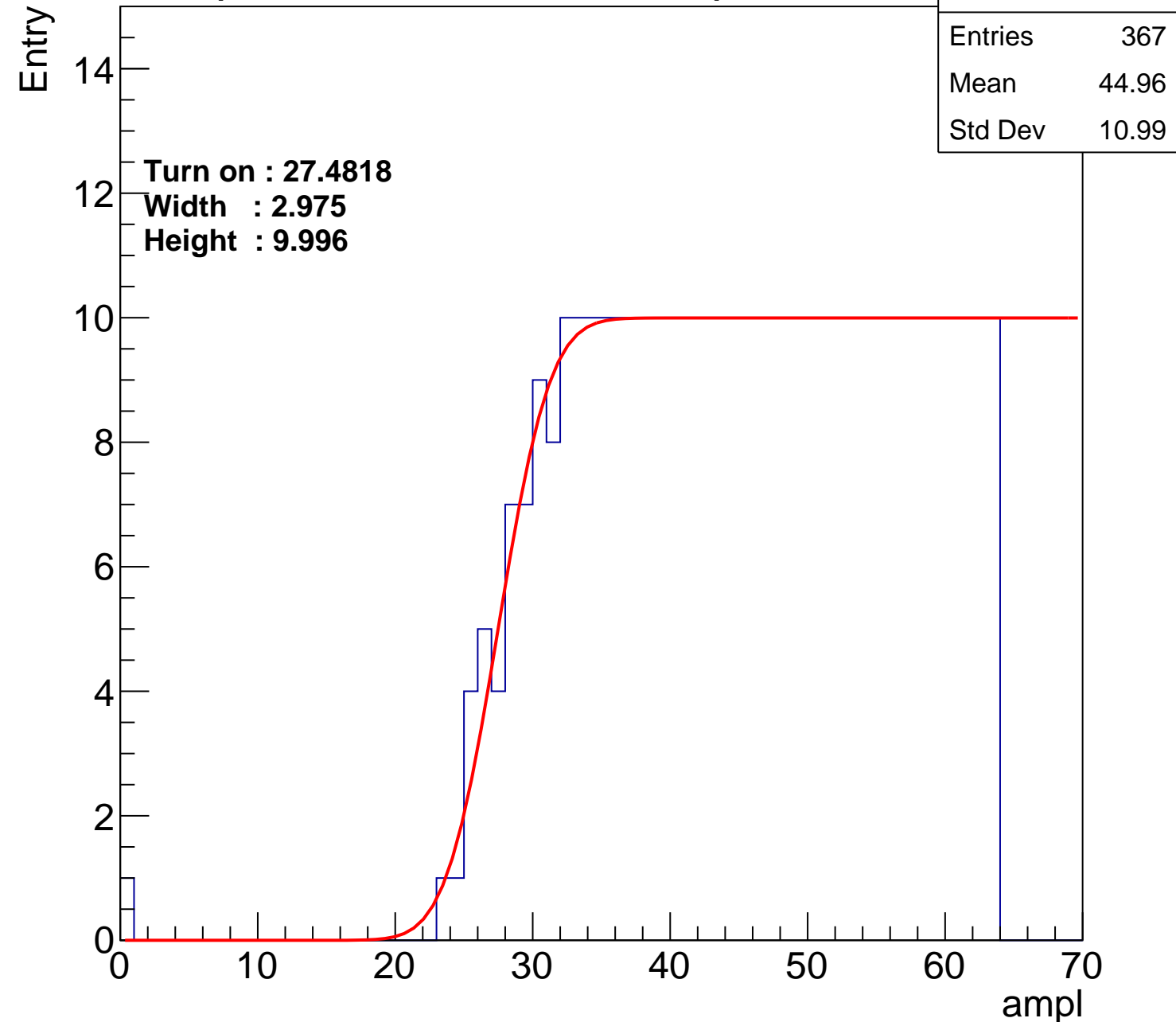
Width : 2.975

Height : 9.996

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch46

calib_packv5_042523_0143.root, FC#11, port A2

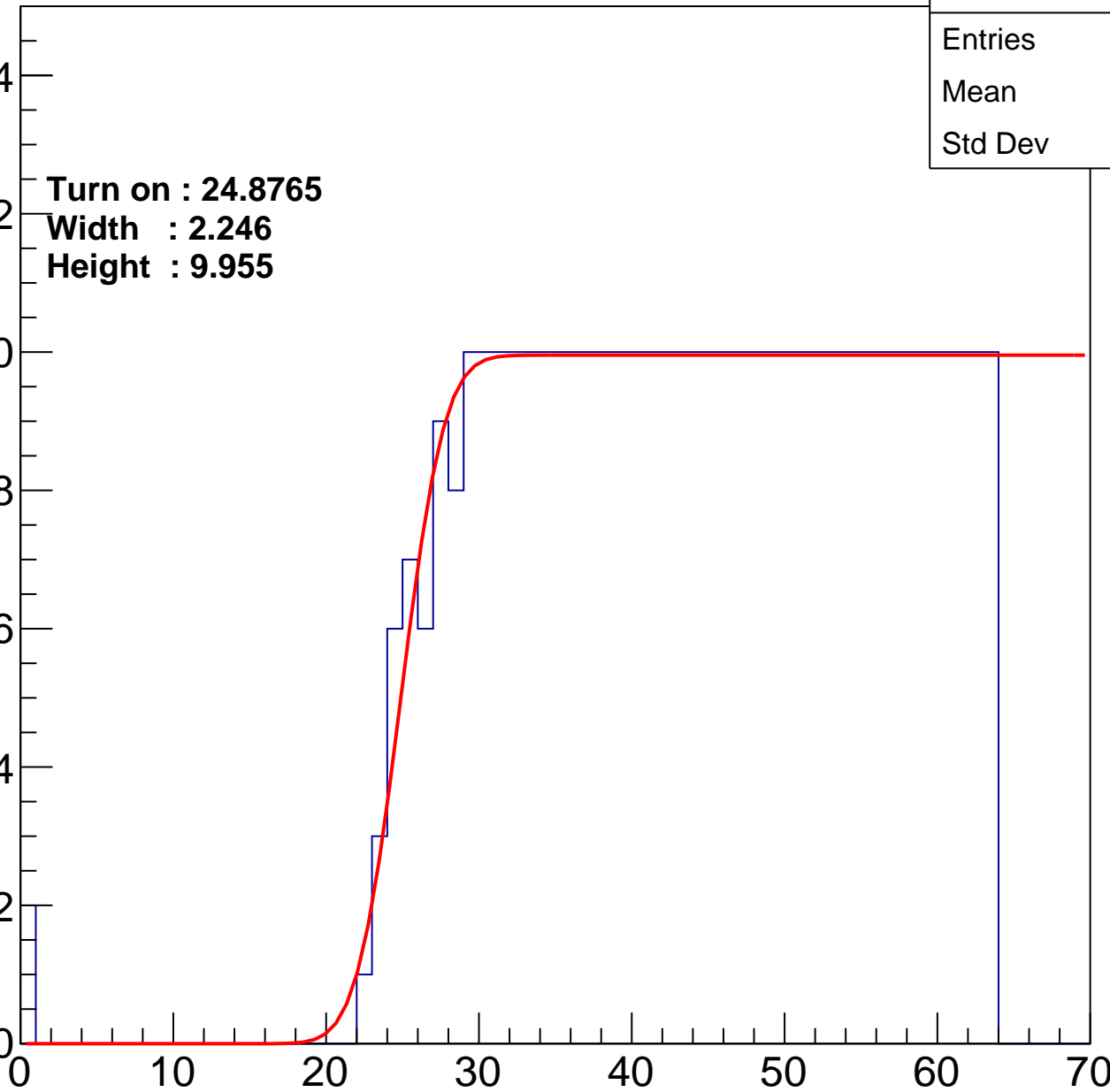
Entry

14
12
10
8
6
4
2
0

Turn on : 24.8765
Width : 2.246
Height : 9.955

Entries	392
Mean	43.71
Std Dev	11.77

ampl



B1L102S, U7-ch47

calib_packv5_042523_0143.root, FC#11, port A2

Entries	390
Mean	43.67
Std Dev	12.06

Turn on : 25.5714

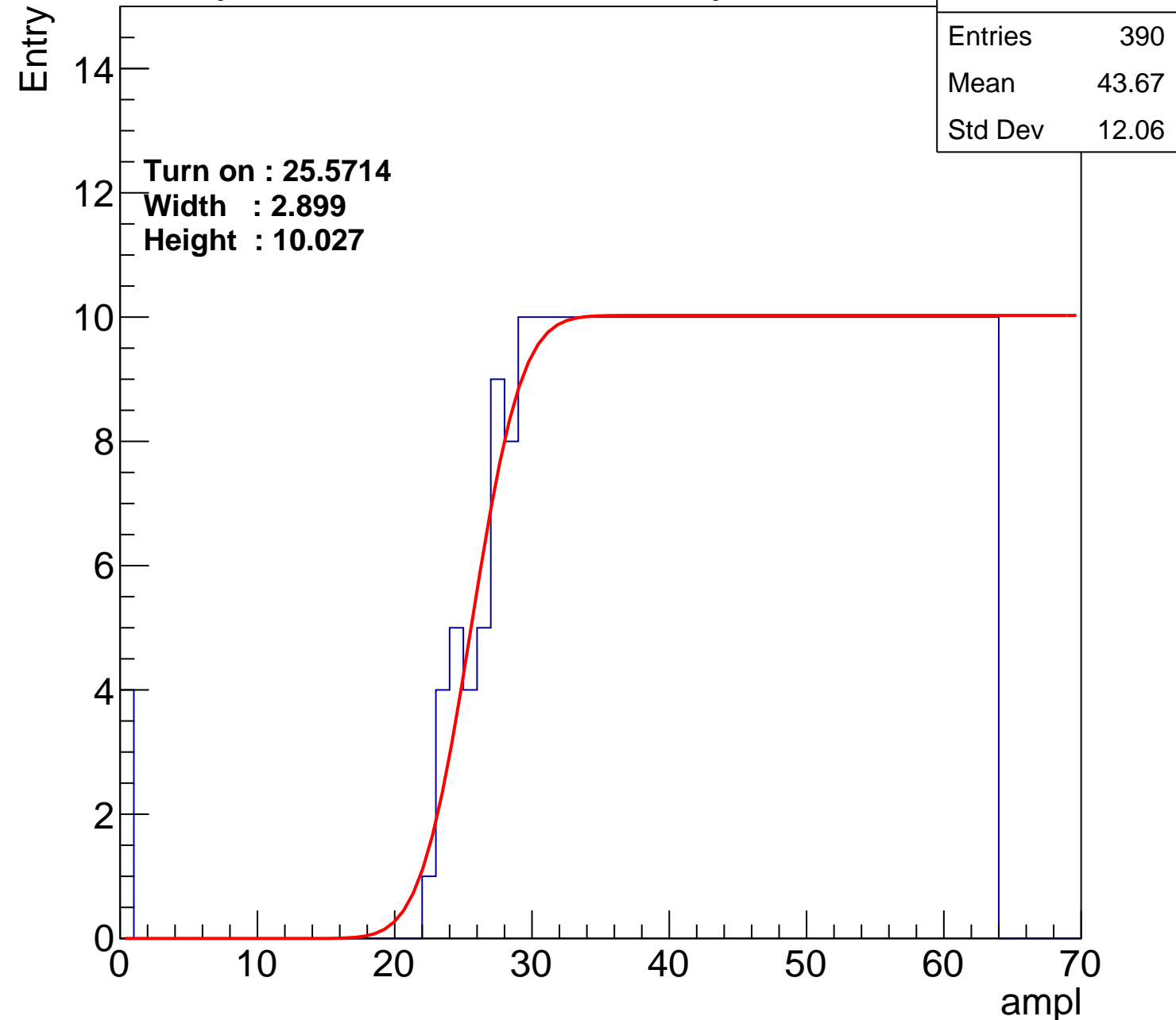
Width : 2.899

Height : 10.027

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch48

calib_packv5_042523_0143.root, FC#11, port A2

Entries	390
Mean	43.75
Std Dev	11.88

Turn on : 25.4912

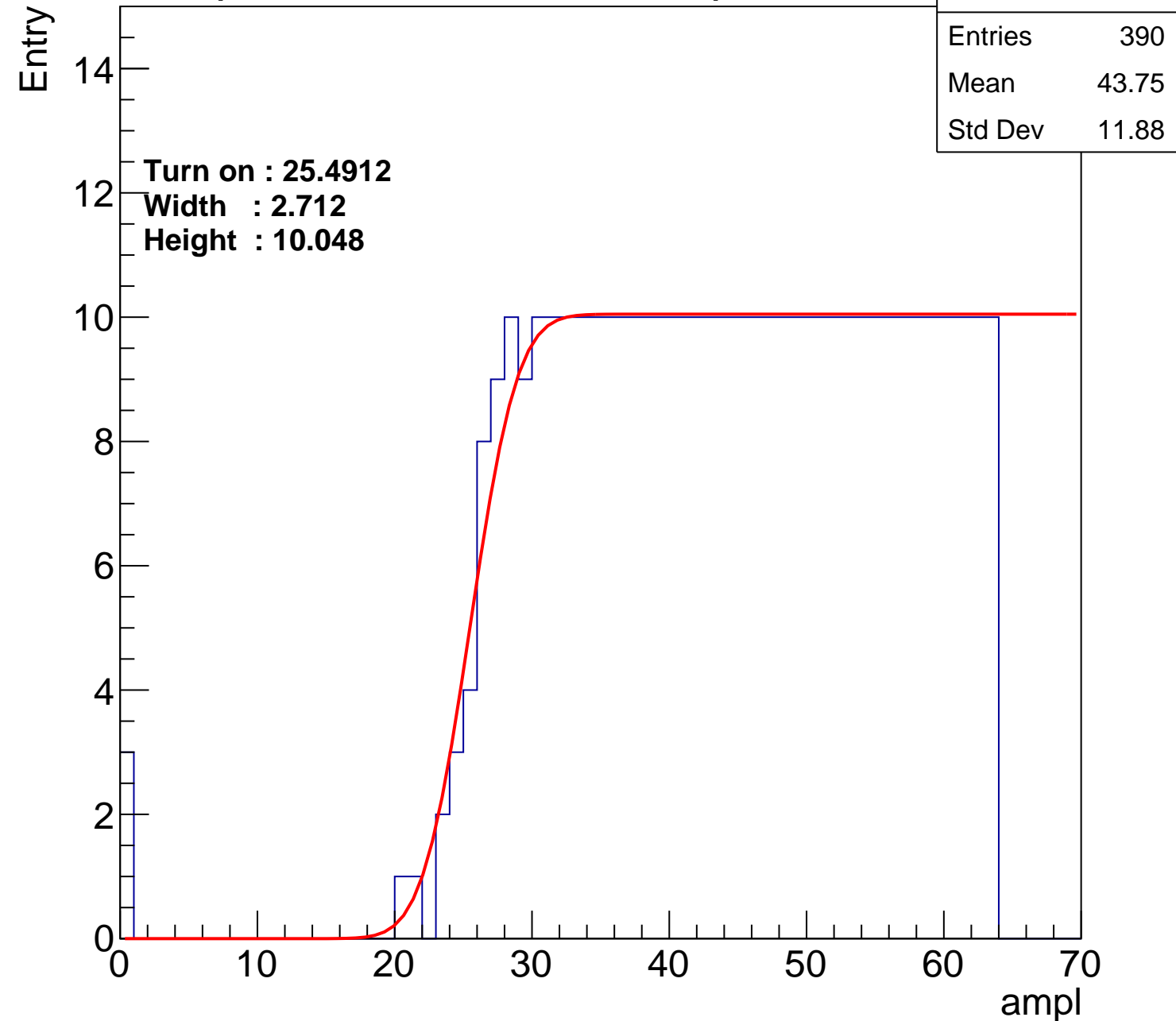
Width : 2.712

Height : 10.048

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch49

calib_packv5_042523_0143.root, FC#11, port A2

Entries	372
Mean	44.74
Std Dev	11.09

Turn on : 26.9393

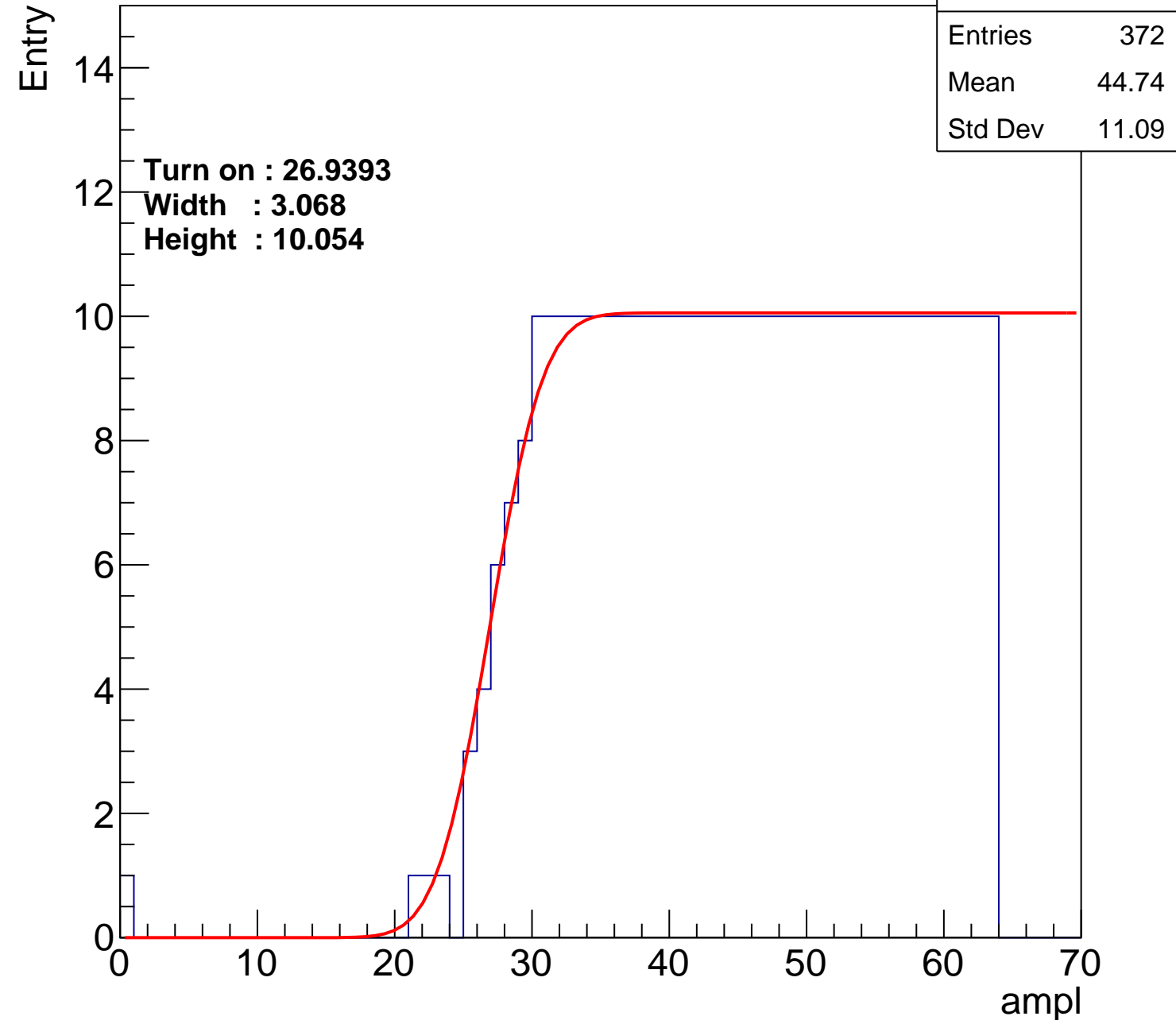
Width : 3.068

Height : 10.054

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch50

calib_packv5_042523_0143.root, FC#11, port A2

Entries	393
Mean	43.69
Std Dev	11.68

Turn on : 24.6150

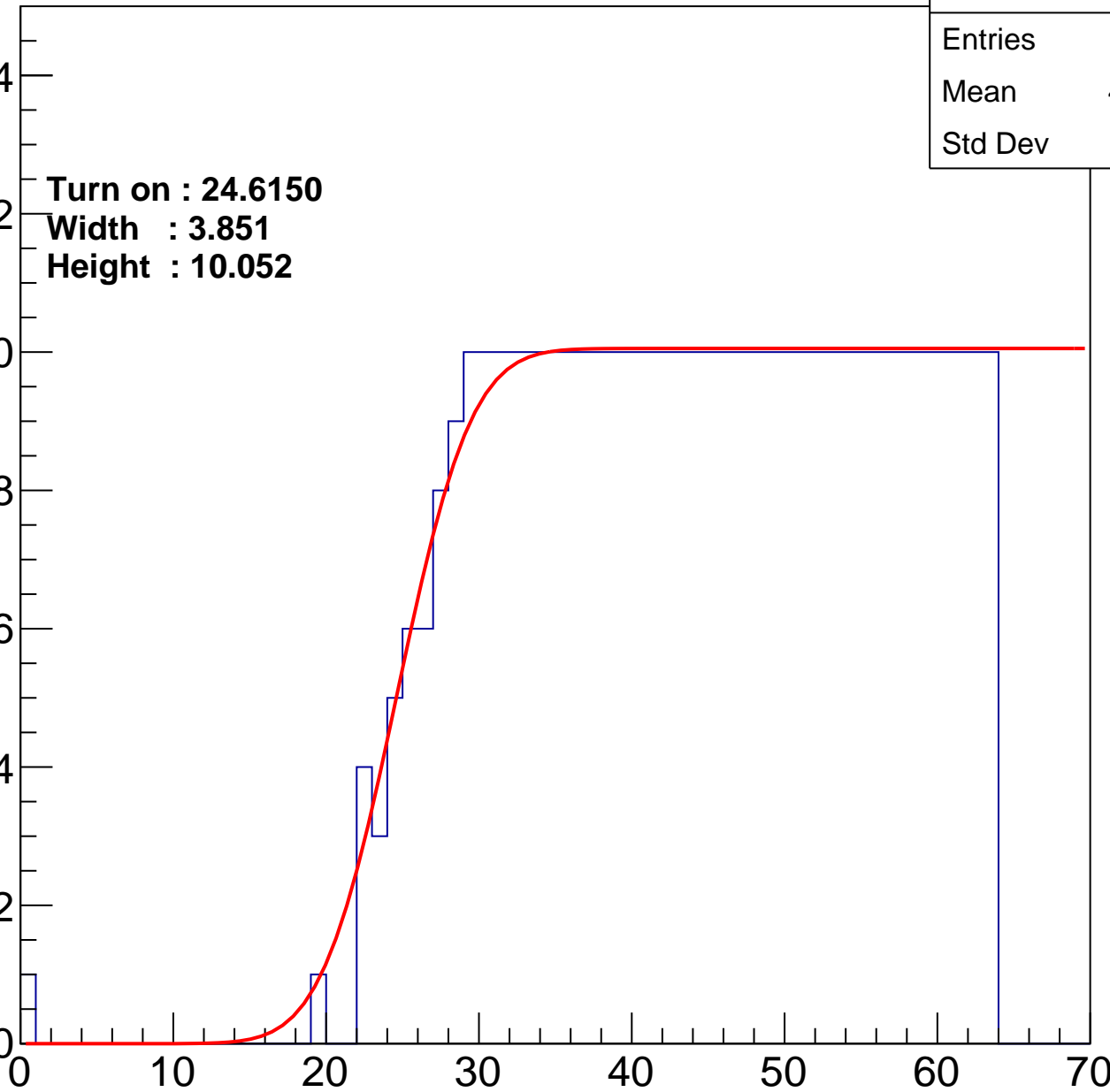
Width : 3.851

Height : 10.052

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch51

calib_packv5_042523_0143.root, FC#11, port A2

Entries	375
Mean	44.46
Std Dev	11.56

Turn on : 27.5073

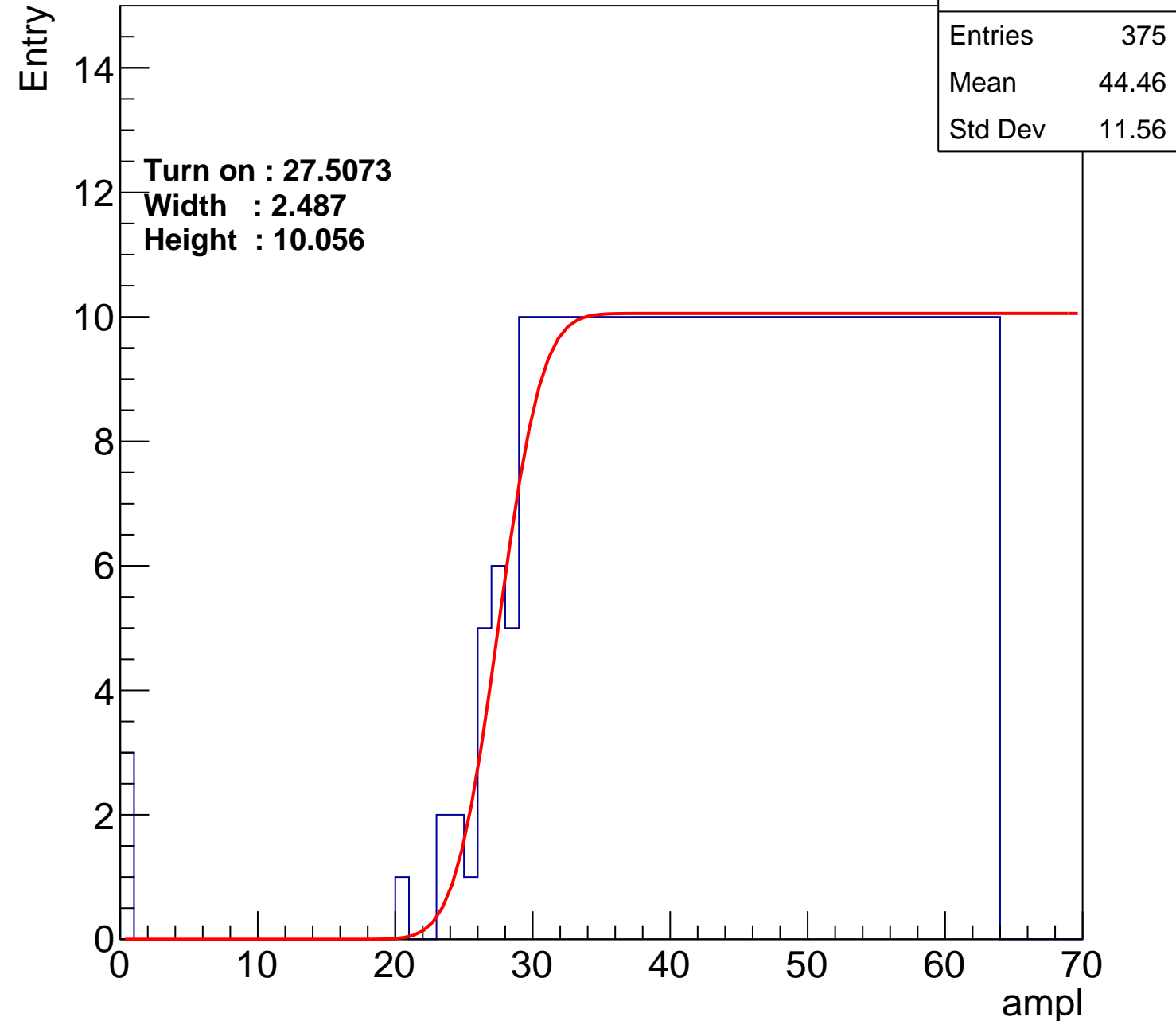
Width : 2.487

Height : 10.056

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch52

calib_packv5_042523_0143.root, FC#11, port A2

Entries	377
Mean	44.47
Std Dev	11.25

Turn on : 26.2106

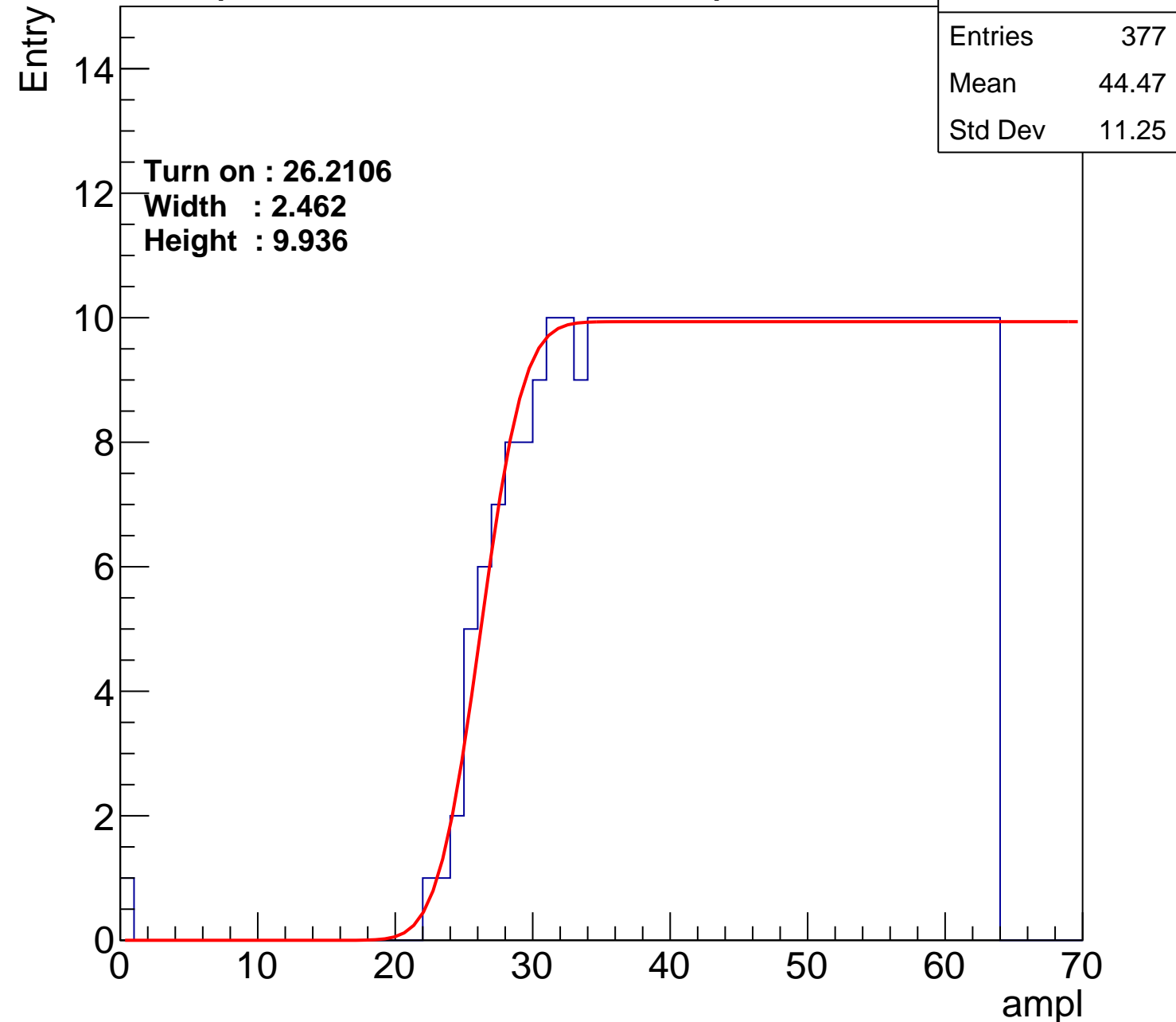
Width : 2.462

Height : 9.936

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch53

calib_packv5_042523_0143.root, FC#11, port A2

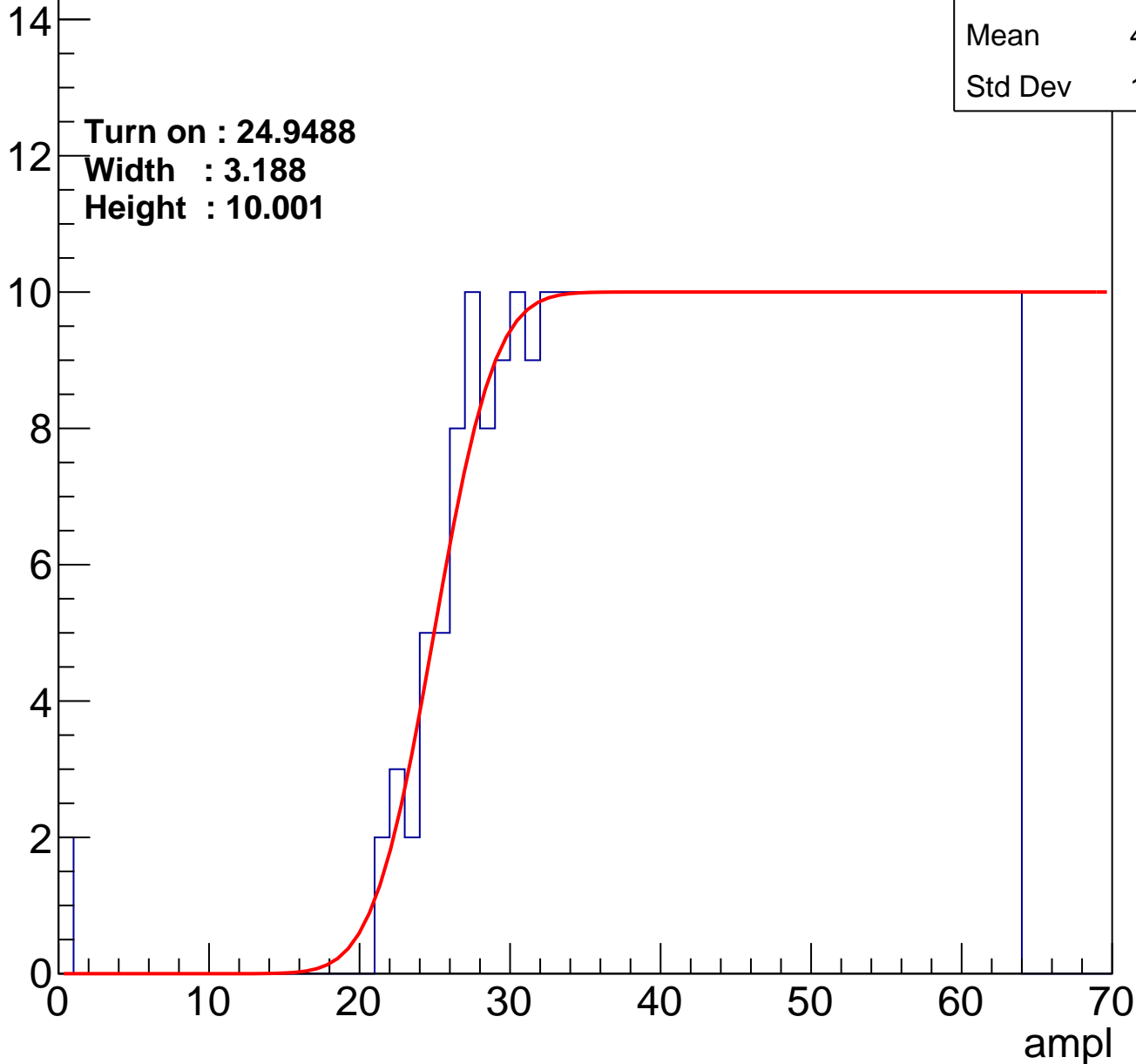
Entries	393
Mean	43.62
Std Dev	11.86

Turn on : 24.9488

Width : 3.188

Height : 10.001

Entry



B1L102S, U7-ch54

calib_packv5_042523_0143.root, FC#11, port A2

Entries	398
Mean	43.4
Std Dev	11.95

Turn on : 24.5044

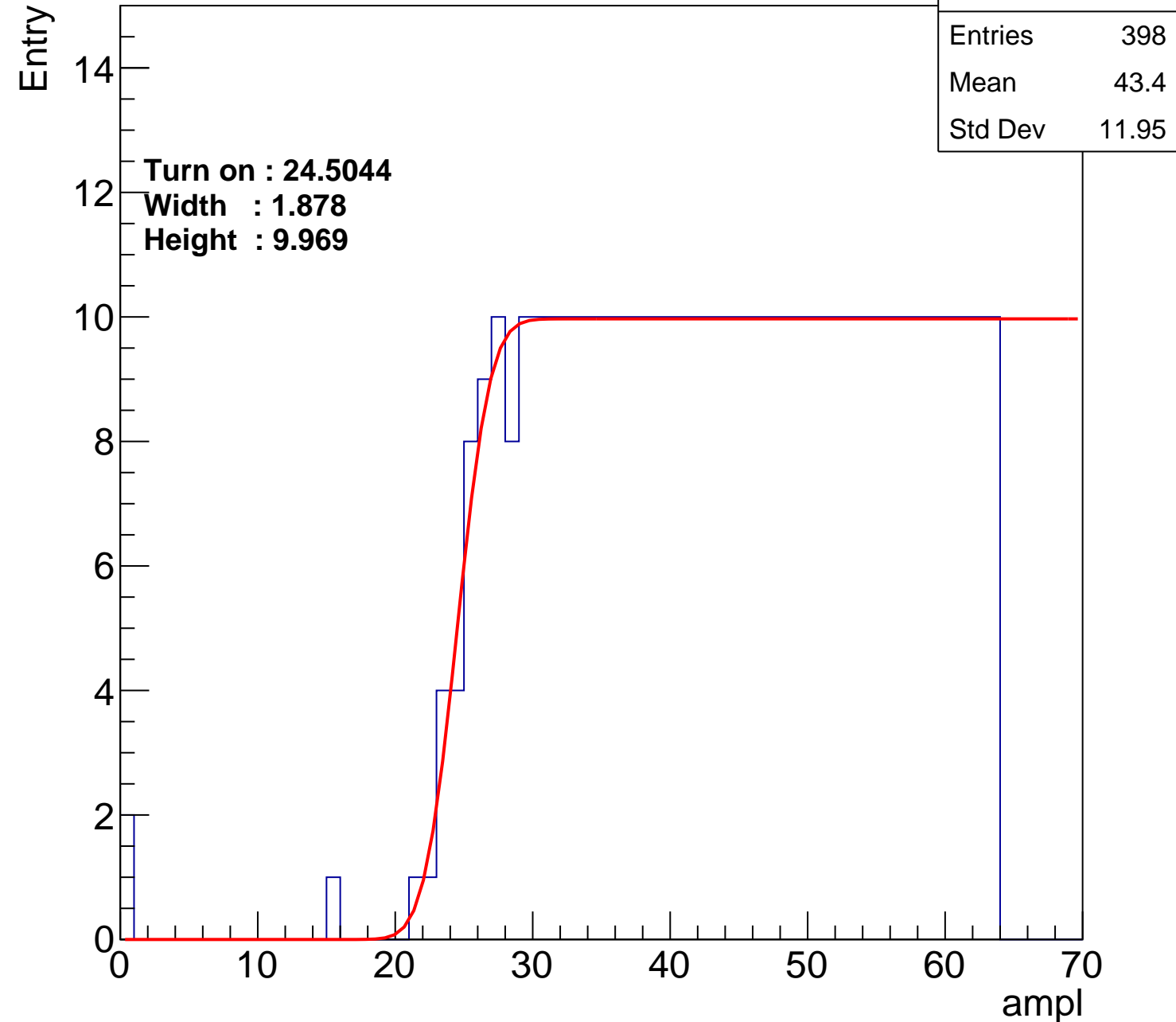
Width : 1.878

Height : 9.969

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch55

calib_packv5_042523_0143.root, FC#11, port A2

Entries	373
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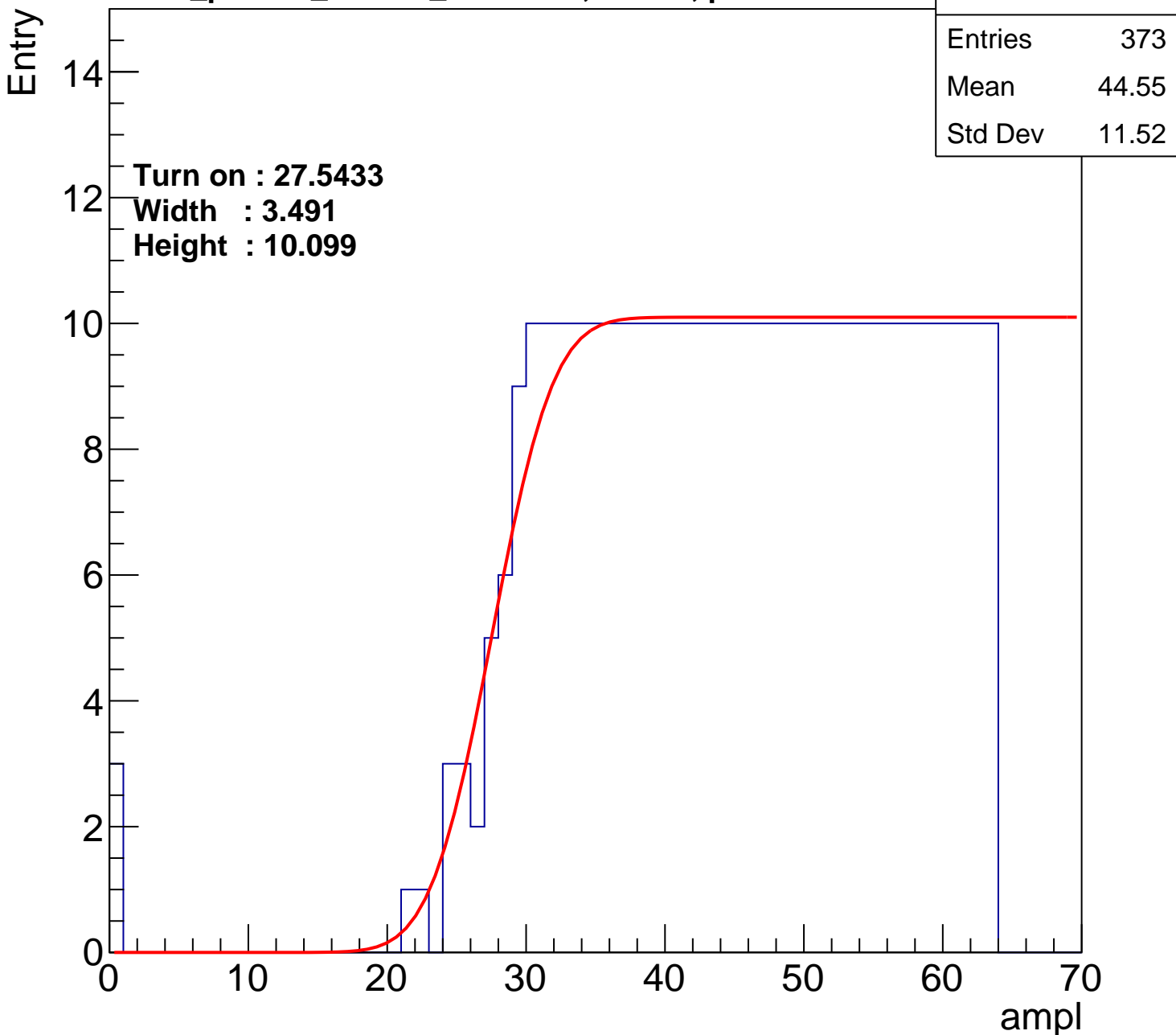
Mean	44.55
------	-------

Std Dev	11.52
---------	-------

Turn on : 27.5433

Width : 3.491

Height : 10.099



B1L102S, U7-ch56

calib_packv5_042523_0143.root, FC#11, port A2

Entries	403
Mean	43.18
Std Dev	11.98

Turn on : 24.1594

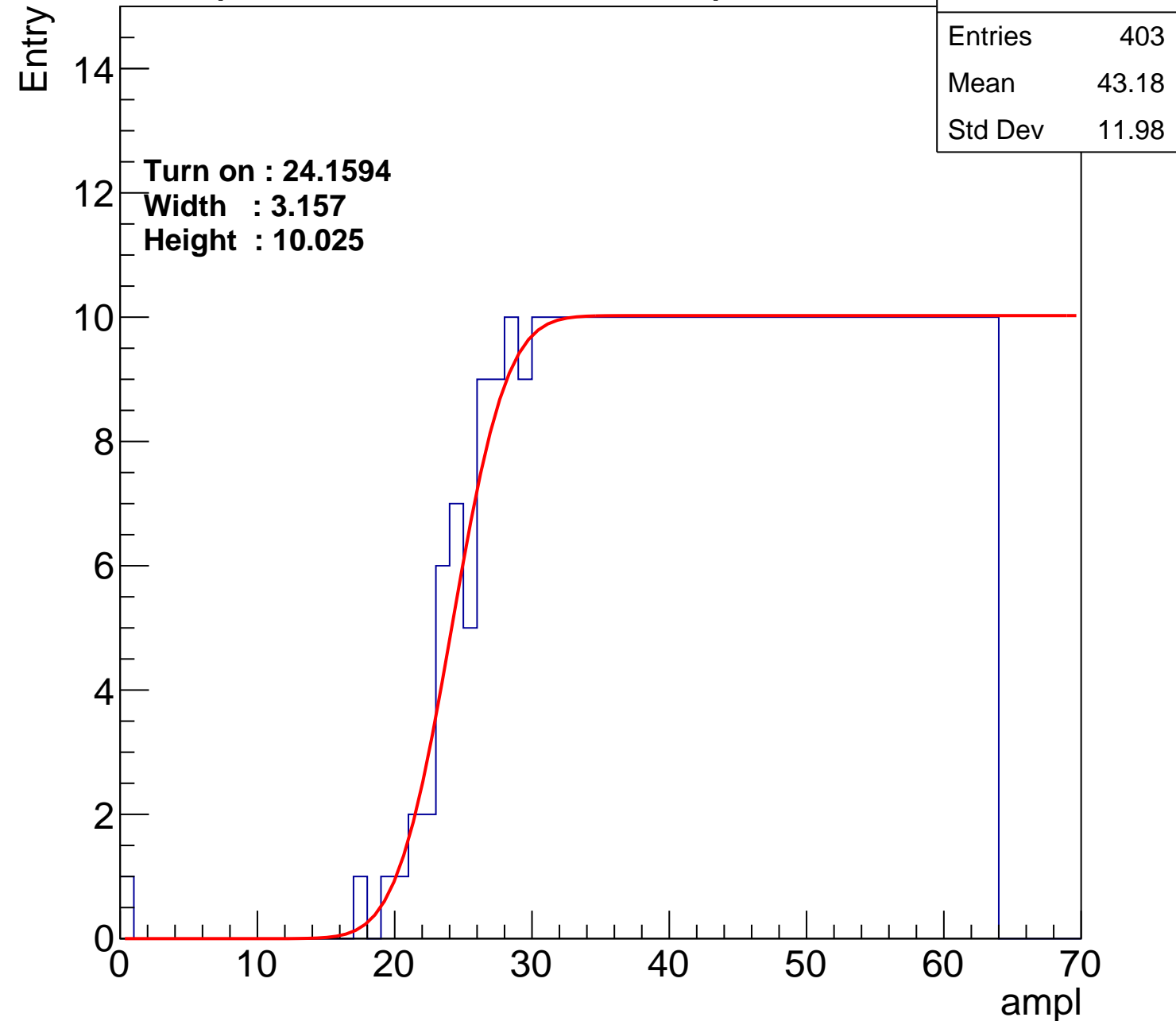
Width : 3.157

Height : 10.025

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch57

calib_packv5_042523_0143.root, FC#11, port A2

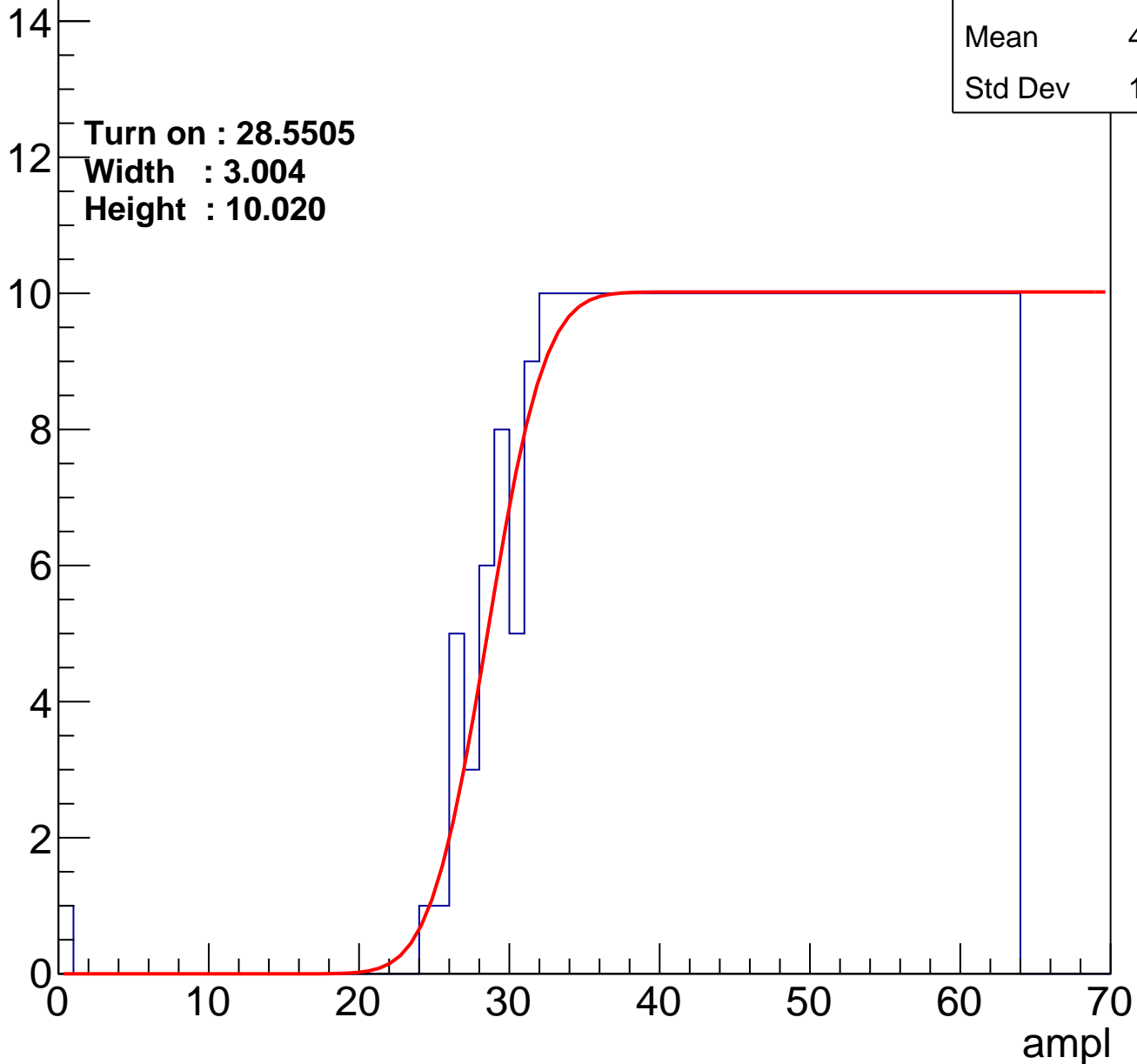
Entry

Entries	359
Mean	45.37
Std Dev	10.76

Turn on : 28.5505

Width : 3.004

Height : 10.020



B1L102S, U7-ch58

calib_packv5_042523_0143.root, FC#11, port A2

Entries	377
Mean	44.38
Std Dev	11.49

Turn on : 27.2453

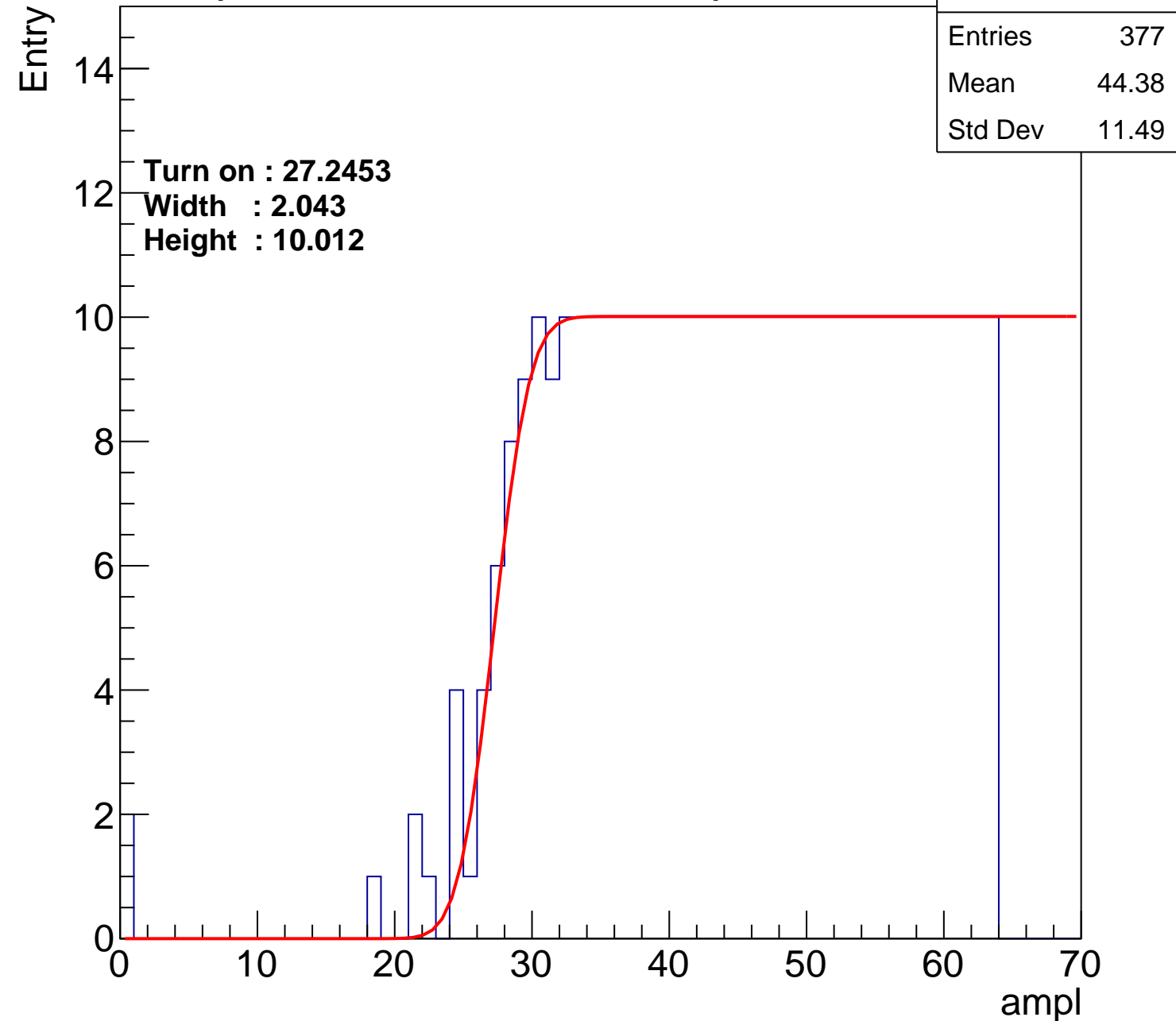
Width : 2.043

Height : 10.012

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch59

calib_packv5_042523_0143.root, FC#11, port A2

Entries	396
Mean	43.49
Std Dev	11.9

Turn on : 25.0224

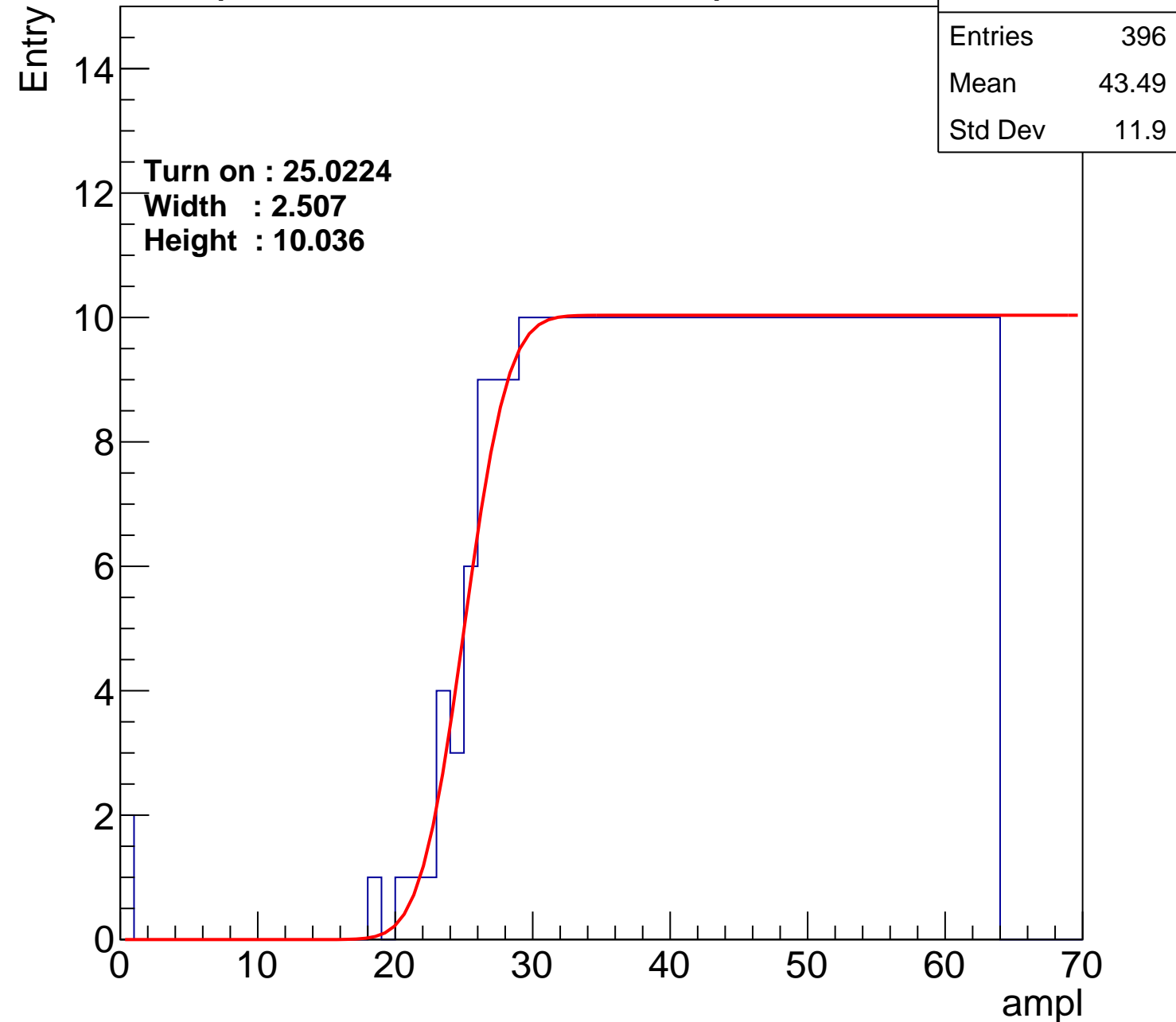
Width : 2.507

Height : 10.036

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch60

calib_packv5_042523_0143.root, FC#11, port A2

Entries	387
Mean	43.91
Std Dev	11.7

Turn on : 25.7060

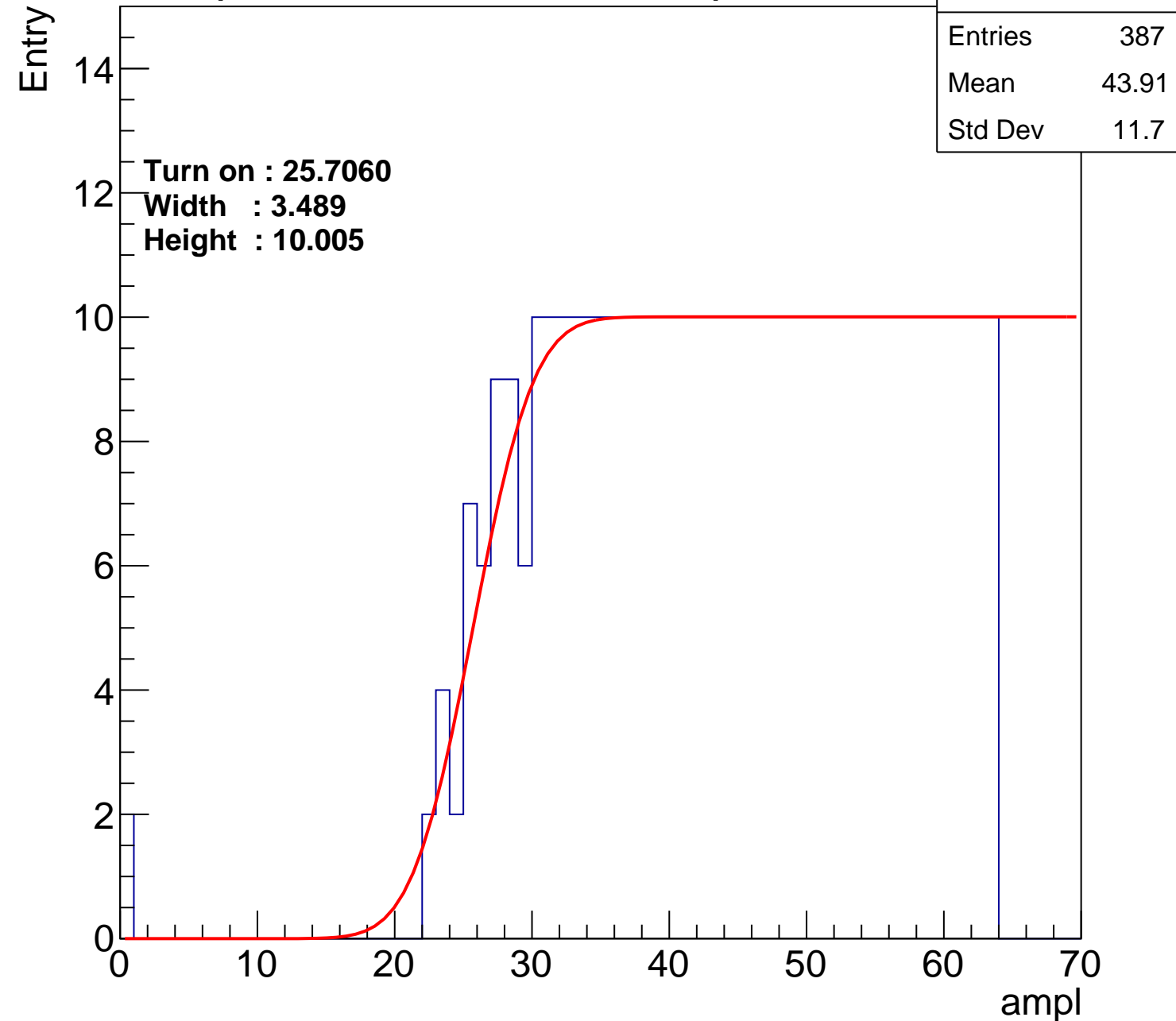
Width : 3.489

Height : 10.005

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch61

calib_packv5_042523_0143.root, FC#11, port A2

Entries	381
Mean	44.28
Std Dev	11.35

Turn on : 26.2164

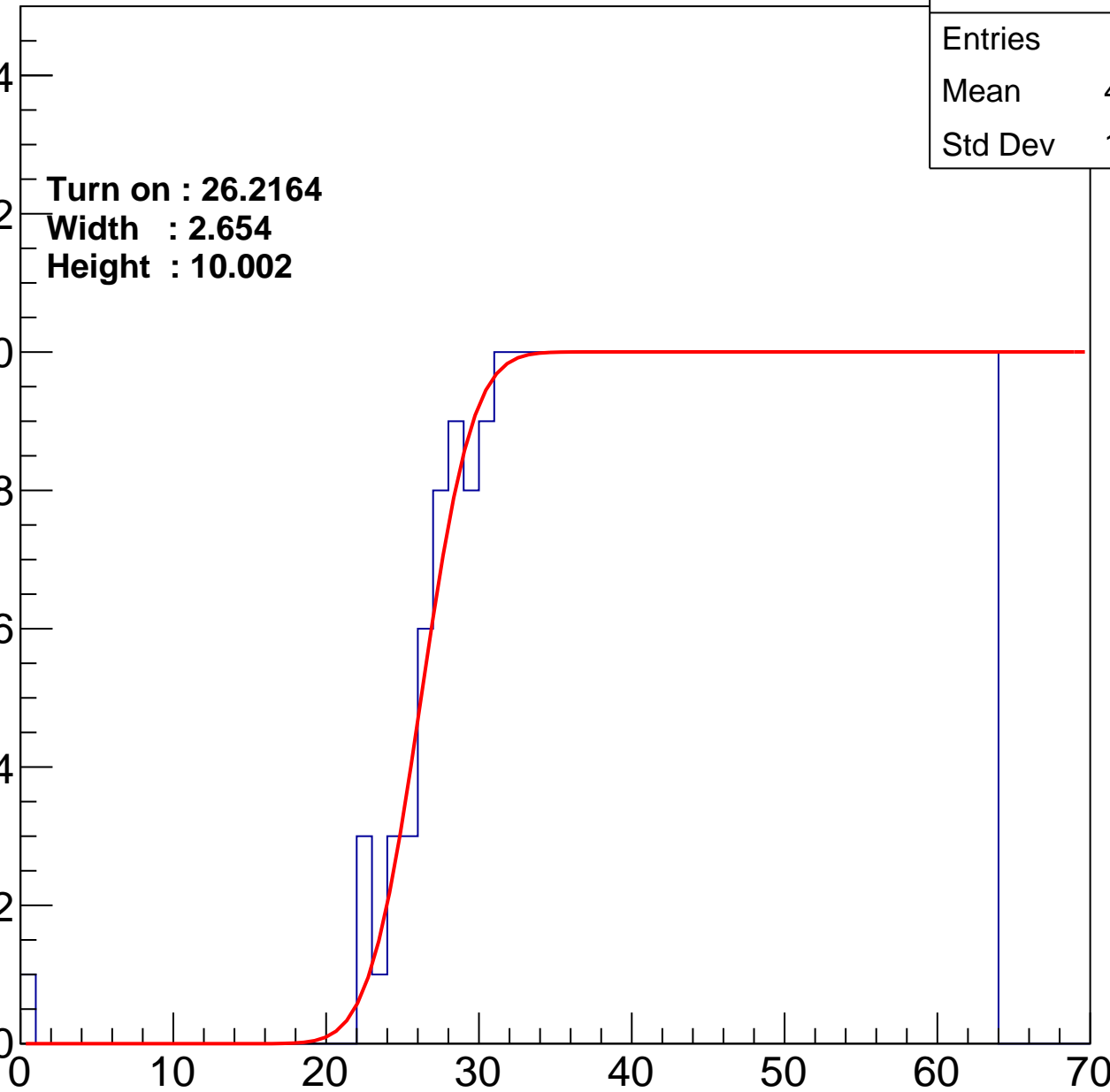
Width : 2.654

Height : 10.002

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch62

calib_packv5_042523_0143.root, FC#11, port A2

Entries	386
Mean	43.87
Std Dev	11.91

Turn on : 26.1937

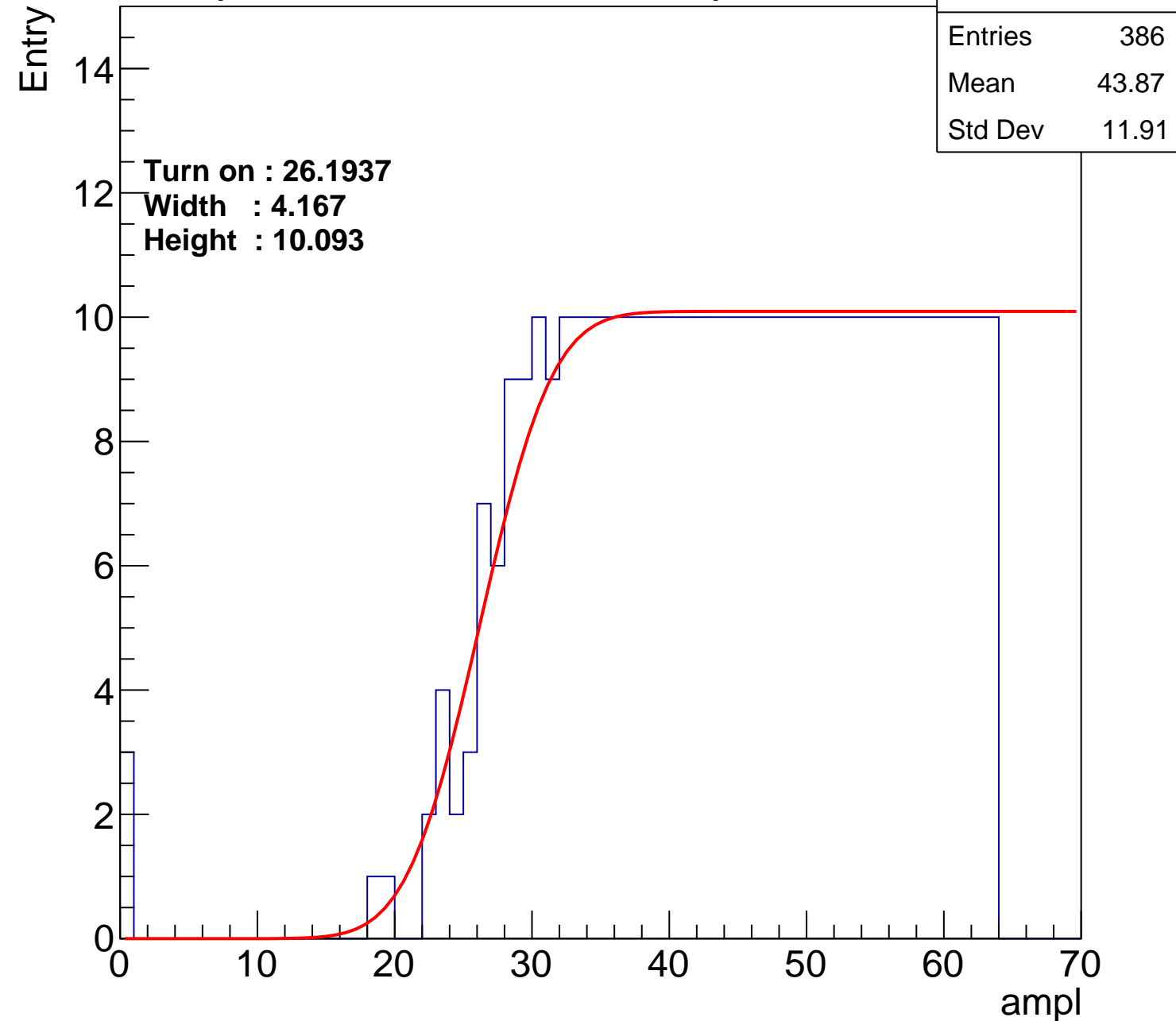
Width : 4.167

Height : 10.093

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch63

calib_packv5_042523_0143.root, FC#11, port A2

Entries	386
Mean	43.97
Std Dev	11.67

Turn on : 27.0209

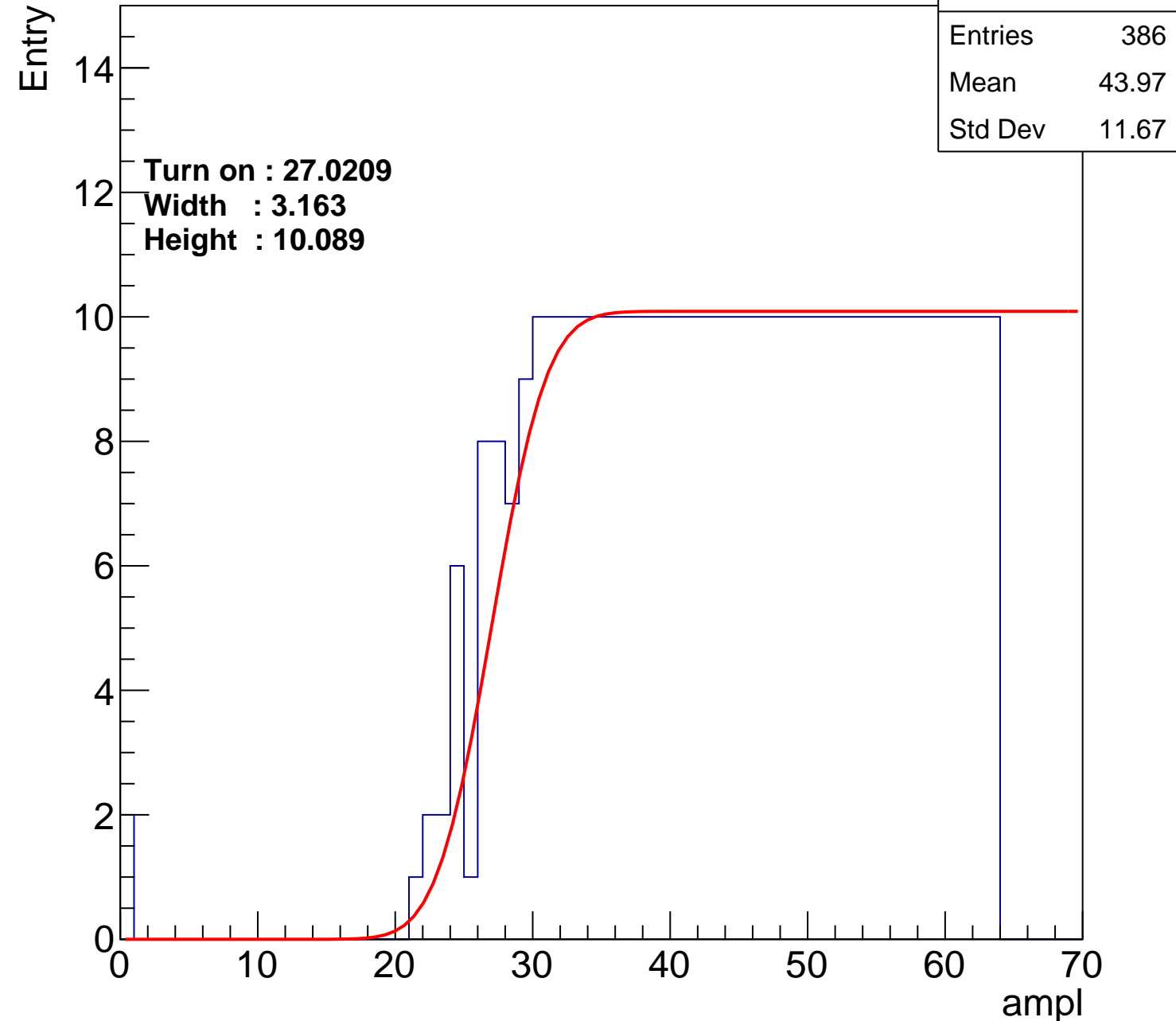
Width : 3.163

Height : 10.089

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch64

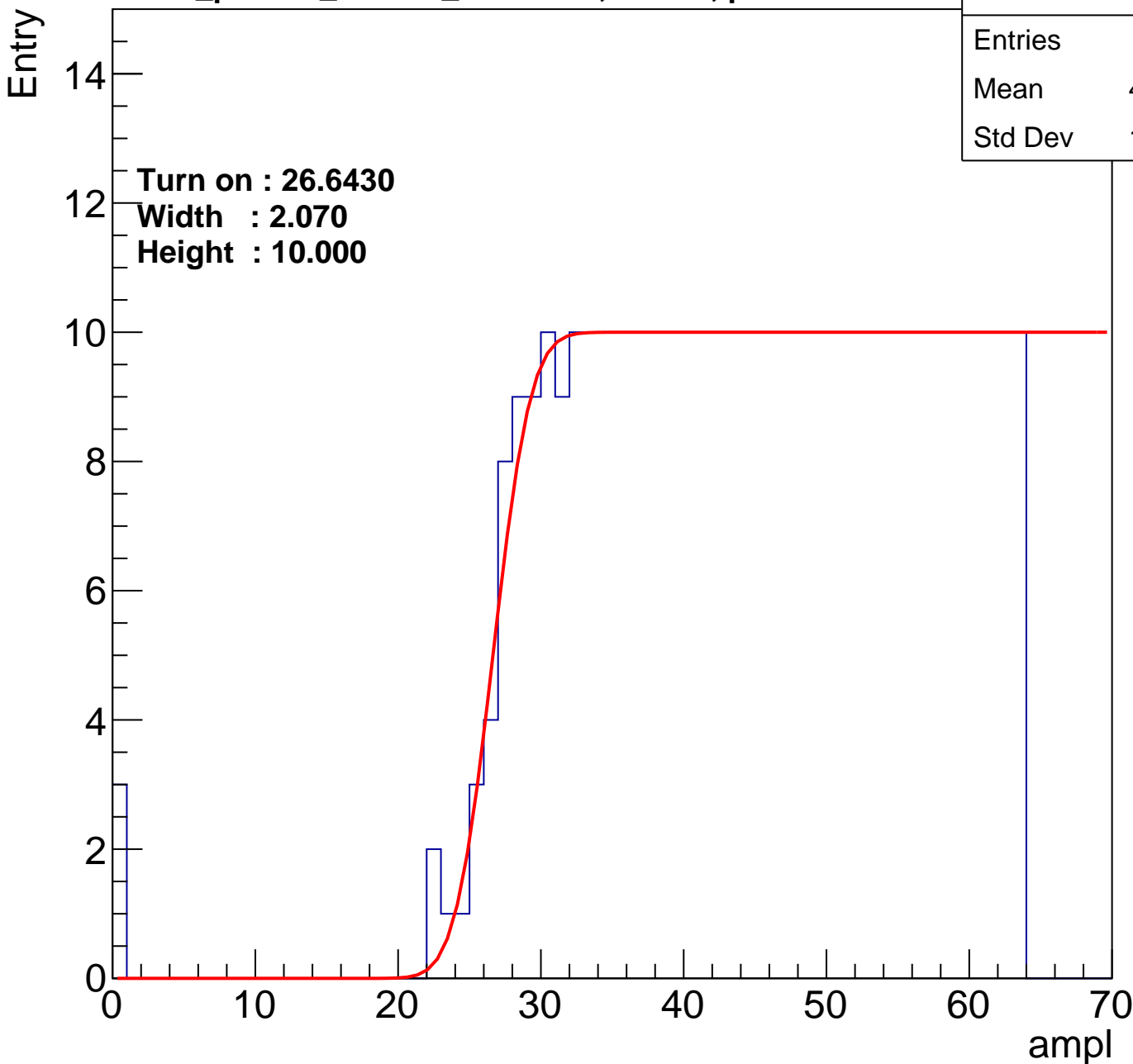
calib_packv5_042523_0143.root, FC#11, port A2

Entries	379
Mean	44.27
Std Dev	11.63

Turn on : 26.6430

Width : 2.070

Height : 10.000



B1L102S, U7-ch65

calib_packv5_042523_0143.root, FC#11, port A2

Entries	377
Mean	44.4
Std Dev	11.45

Turn on : 26.9283

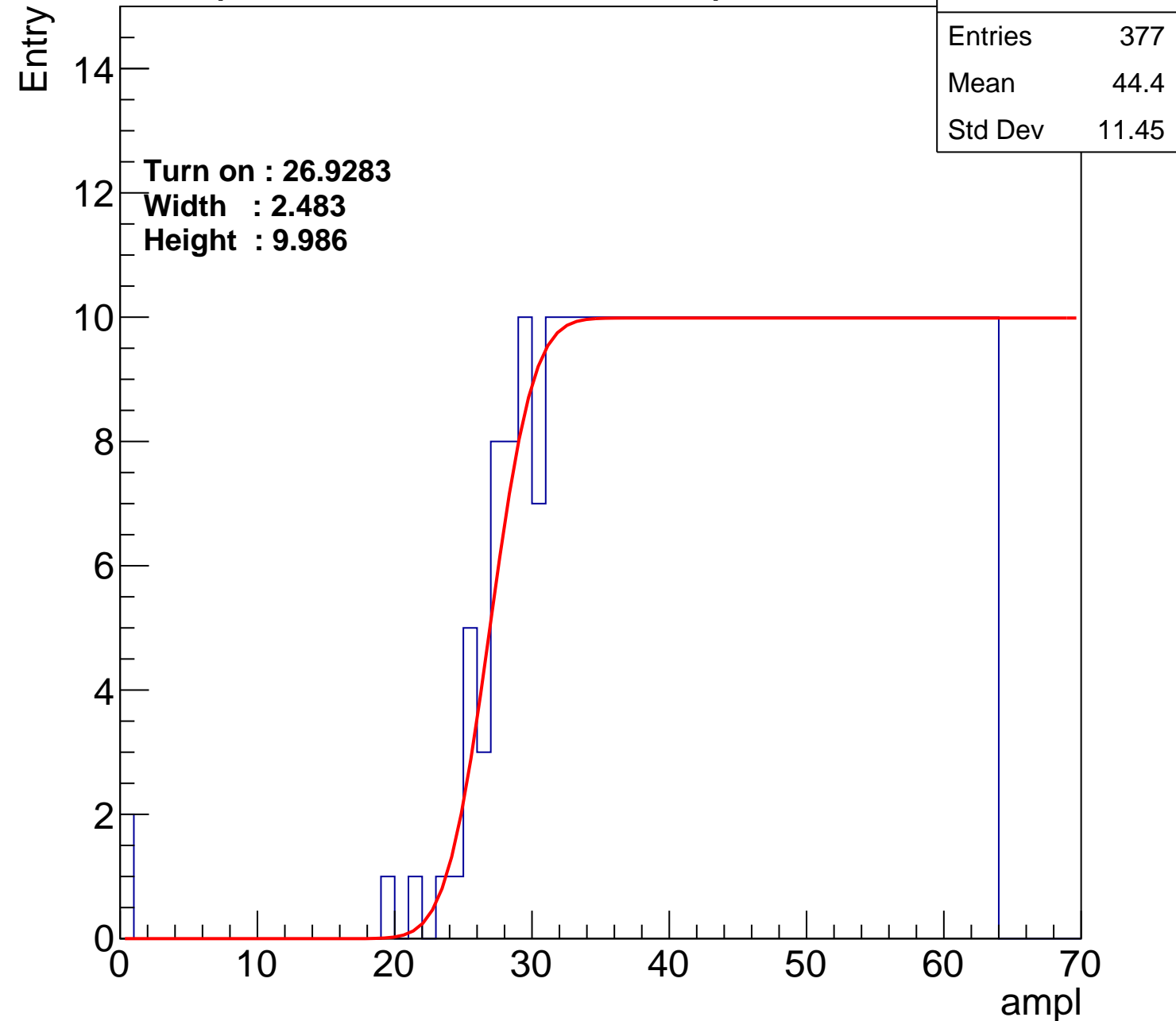
Width : 2.483

Height : 9.986

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch66

calib_packv5_042523_0143.root, FC#11, port A2

Entries	398
Mean	43.35
Std Dev	12.01

Turn on : 24.2645

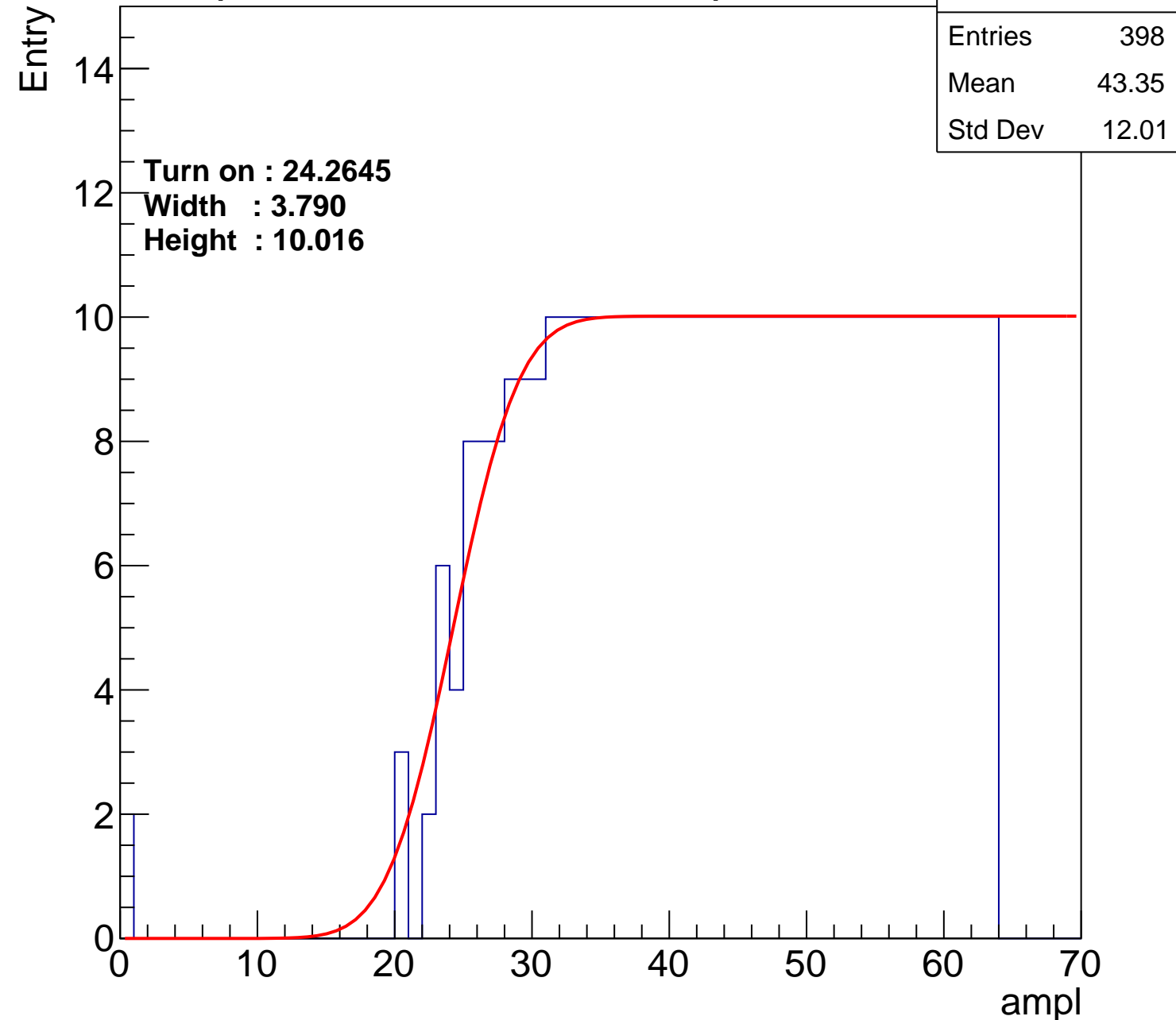
Width : 3.790

Height : 10.016

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch67

calib_packv5_042523_0143.root, FC#11, port A2

Entries	382
Mean	44.19
Std Dev	11.53

Turn on : 26.3154

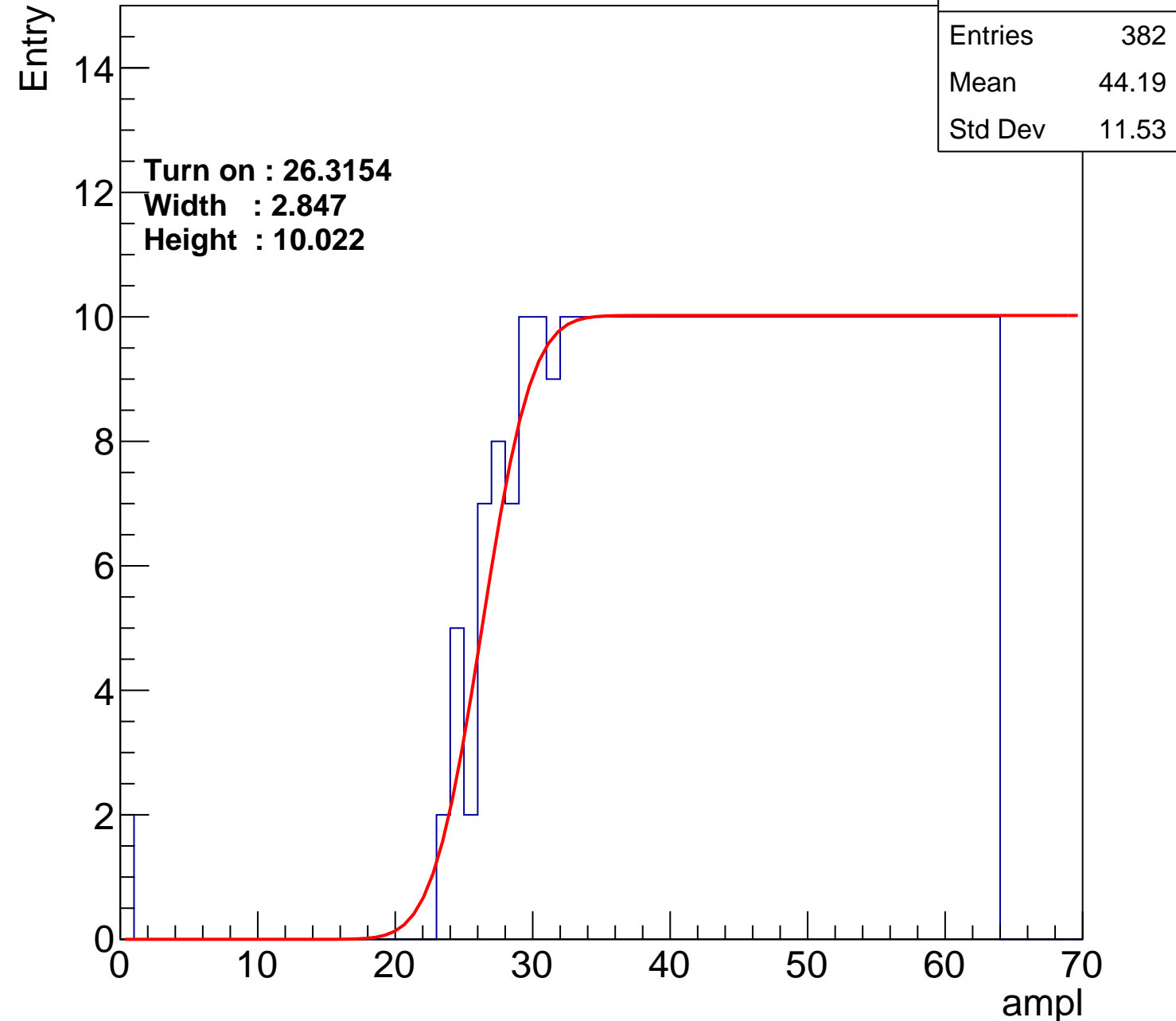
Width : 2.847

Height : 10.022

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch68

calib_packv5_042523_0143.root, FC#11, port A2

Entries	385
Mean	43.92
Std Dev	11.86

Turn on : 26.9655

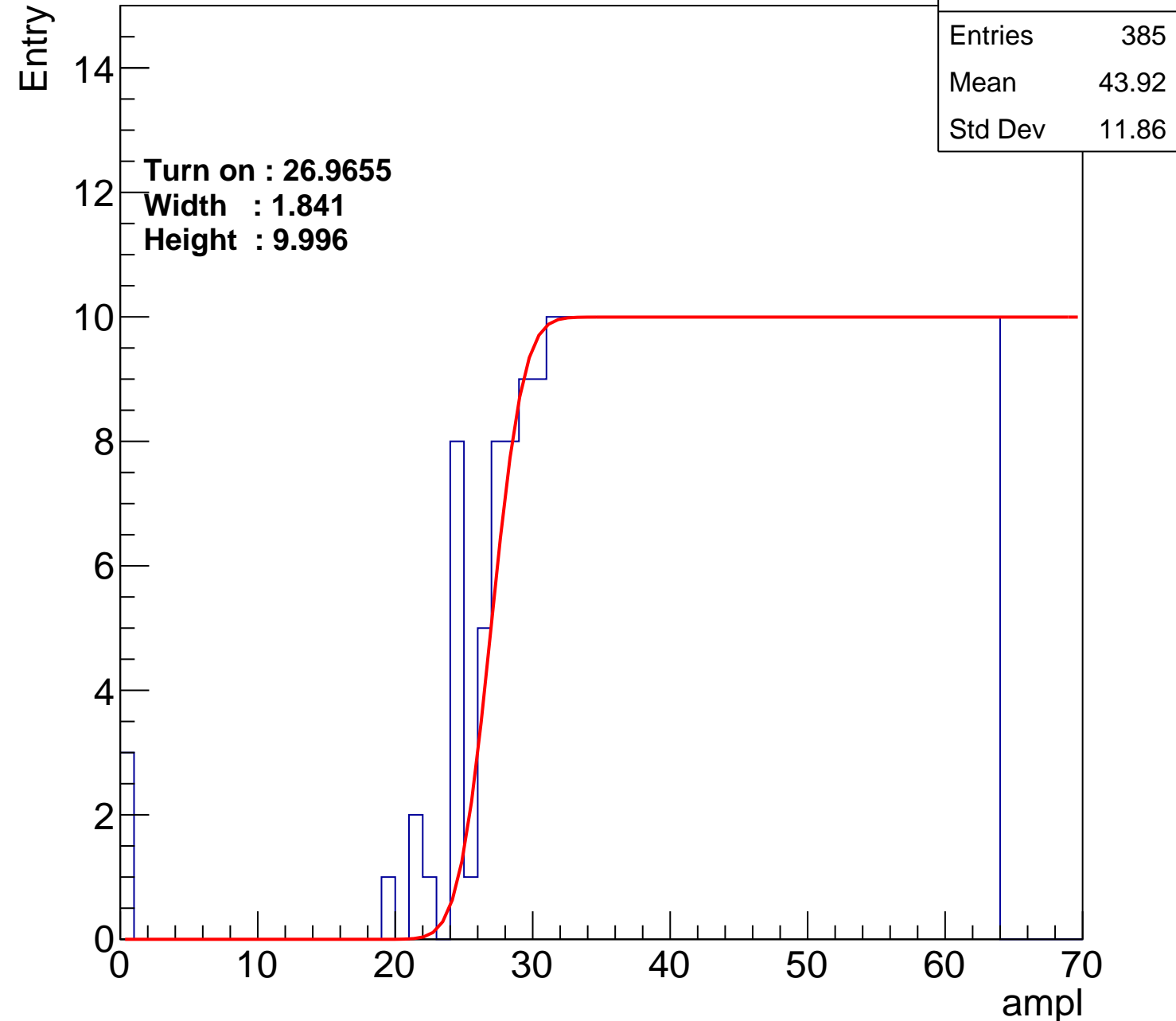
Width : 1.841

Height : 9.996

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch69

calib_packv5_042523_0143.root, FC#11, port A2

Entries	385
Mean	43.96
Std Dev	11.81

Turn on : 25.9366

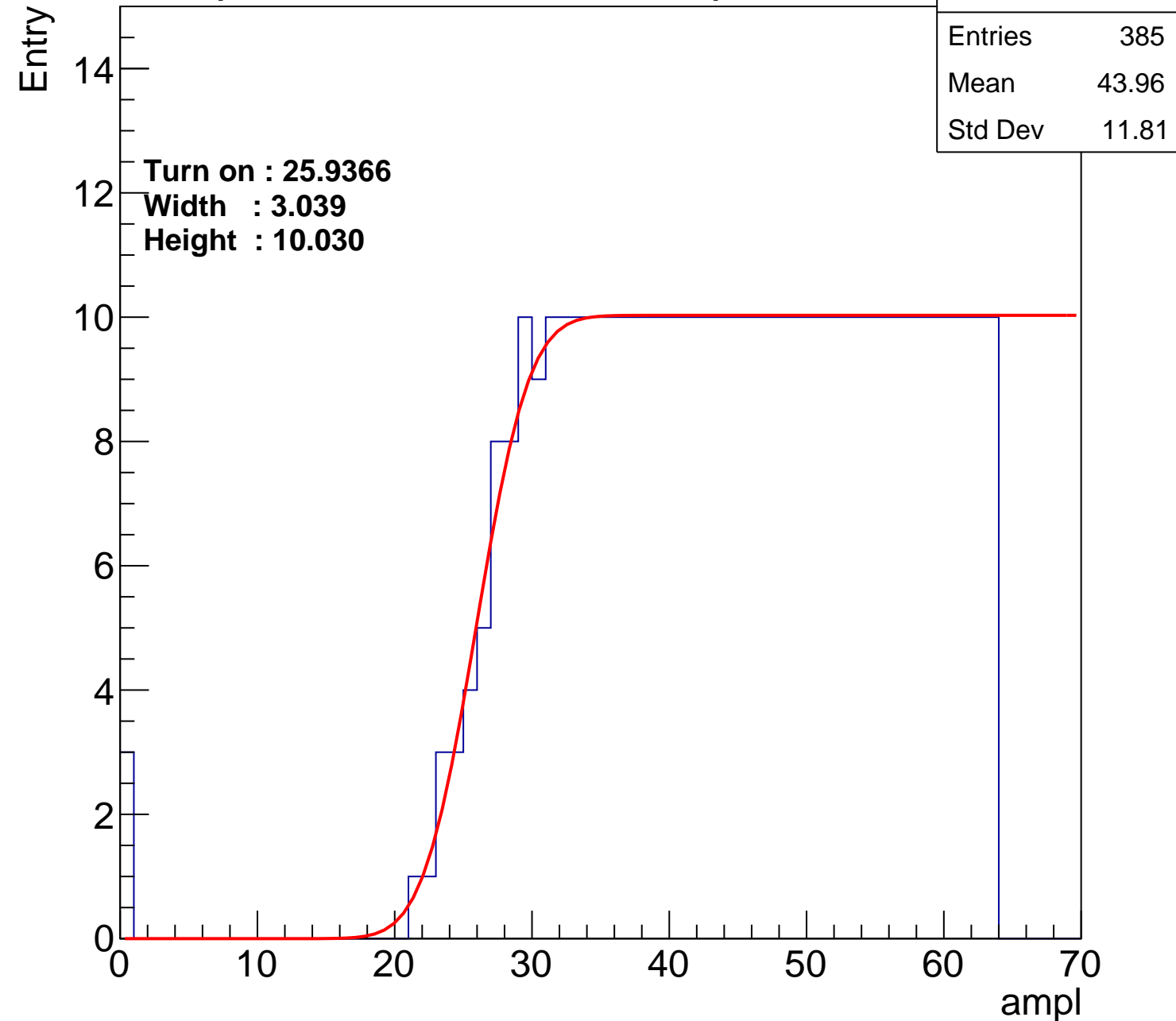
Width : 3.039

Height : 10.030

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch70

calib_packv5_042523_0143.root, FC#11, port A2

Entries	365
Mean	44.94
Std Dev	11.22

Turn on : 28.7929

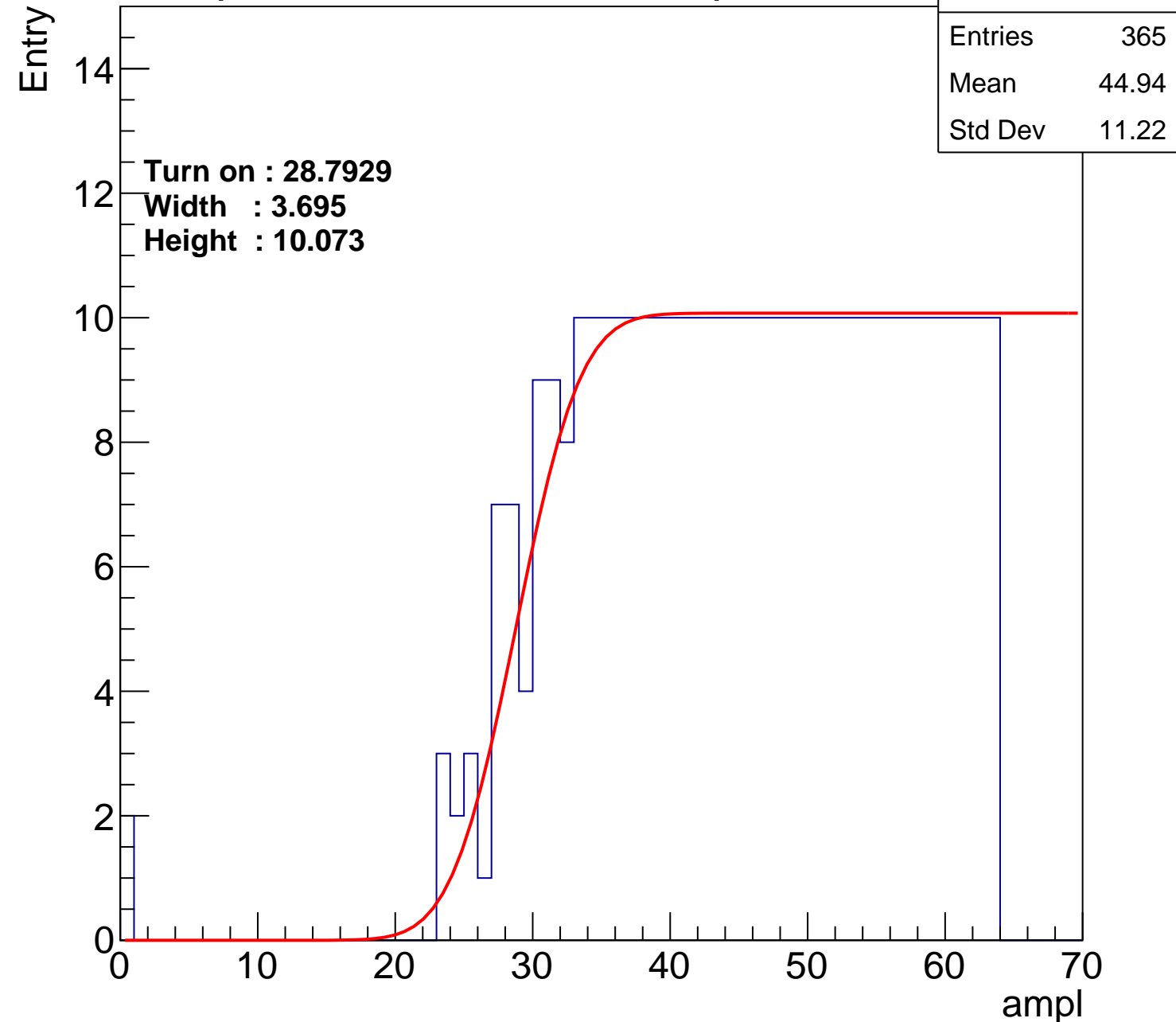
Width : 3.695

Height : 10.073

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch71

calib_packv5_042523_0143.root, FC#11, port A2

Entries	396
Mean	43.45
Std Dev	11.97

Turn on : 24.8609

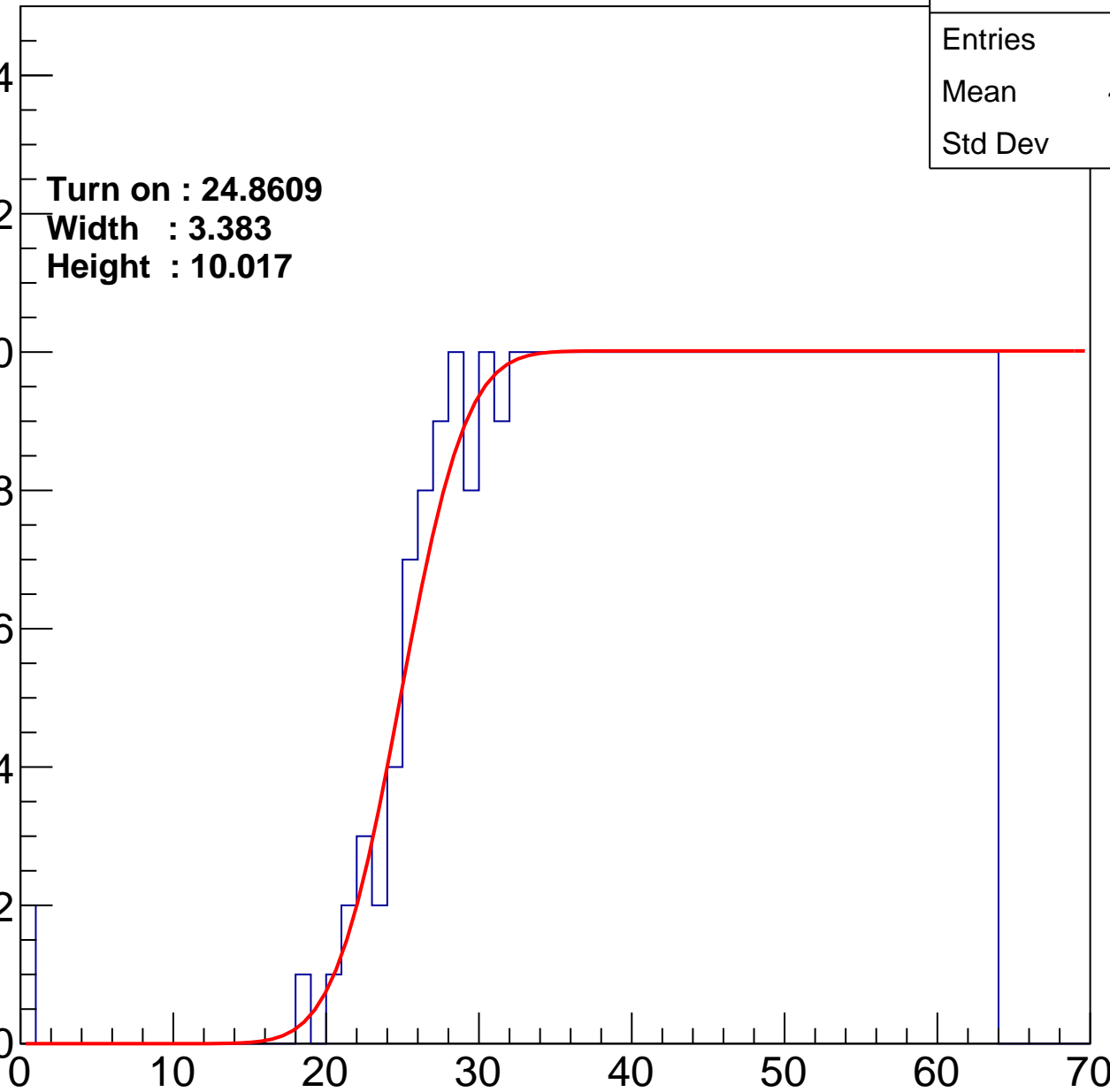
Width : 3.383

Height : 10.017

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch72

calib_packv5_042523_0143.root, FC#11, port A2

Entries	367
Mean	44.94
Std Dev	11.04

Turn on : 27.8391

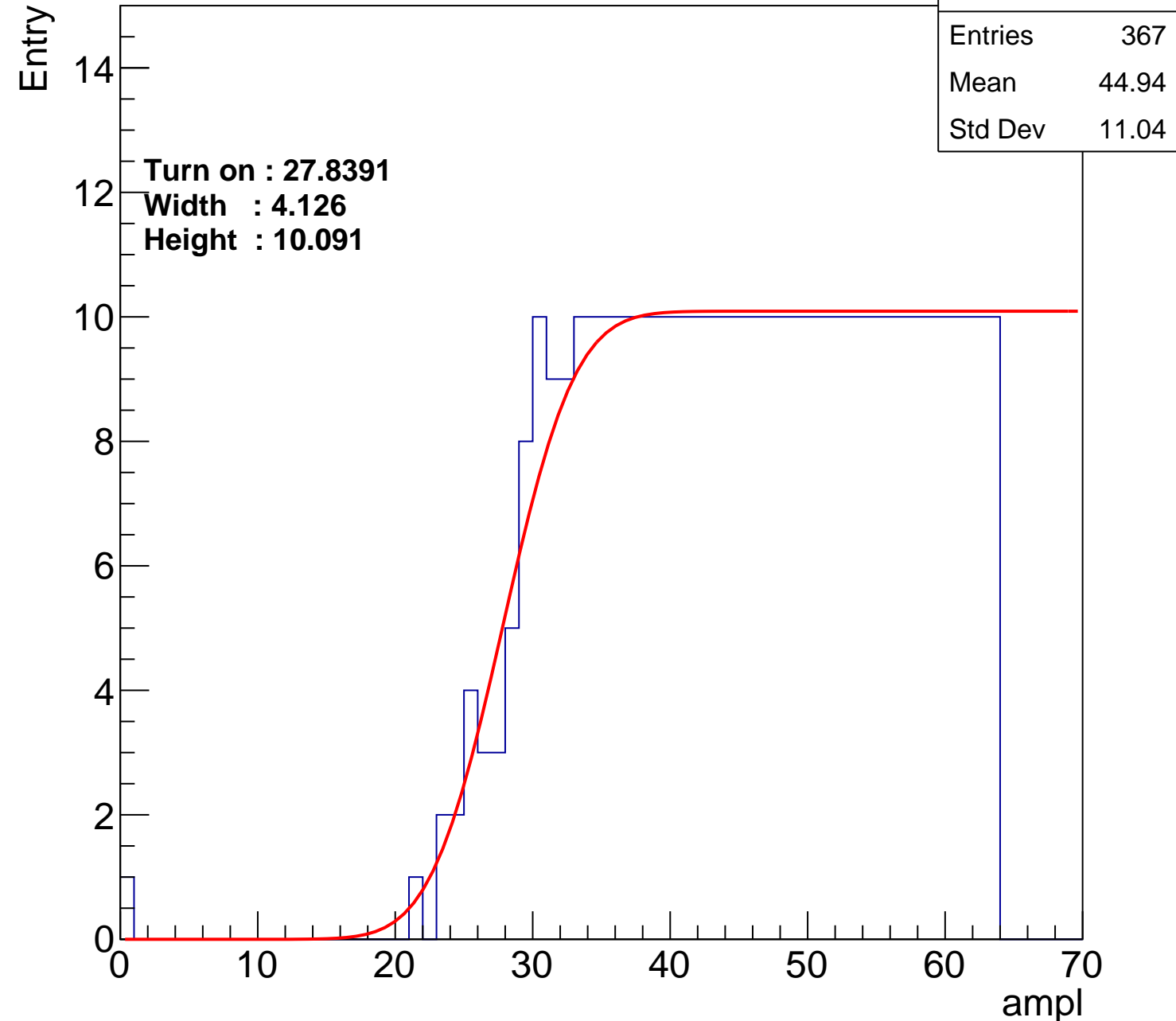
Width : 4.126

Height : 10.091

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch73

calib_packv5_042523_0143.root, FC#11, port A2

Entries	371
Mean	44.61
Std Dev	11.53

Turn on : 28.1595

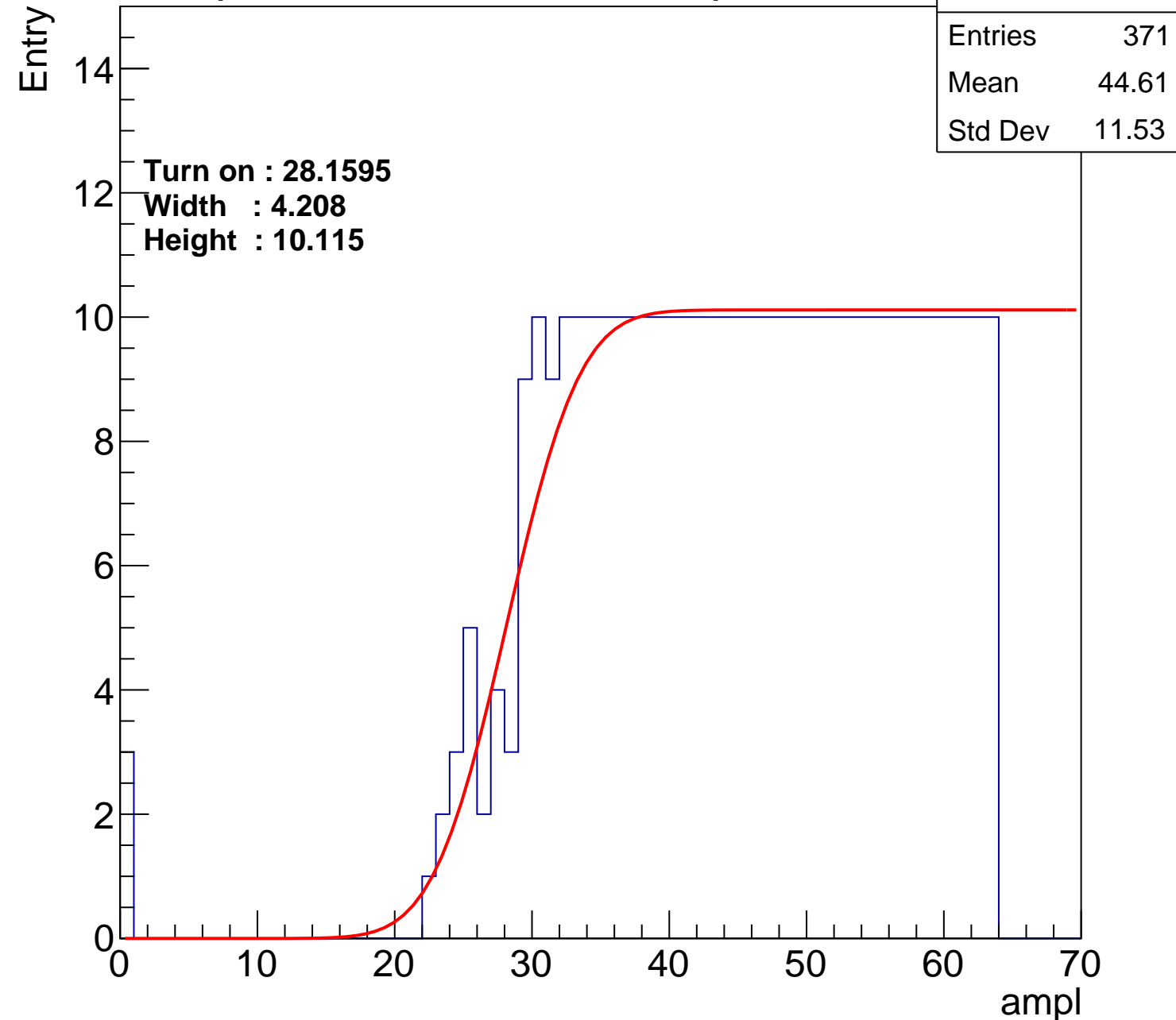
Width : 4.208

Height : 10.115

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch74

calib_packv5_042523_0143.root, FC#11, port A2

Entries	388
Mean	43.94
Std Dev	11.54

Turn on : 25.9743

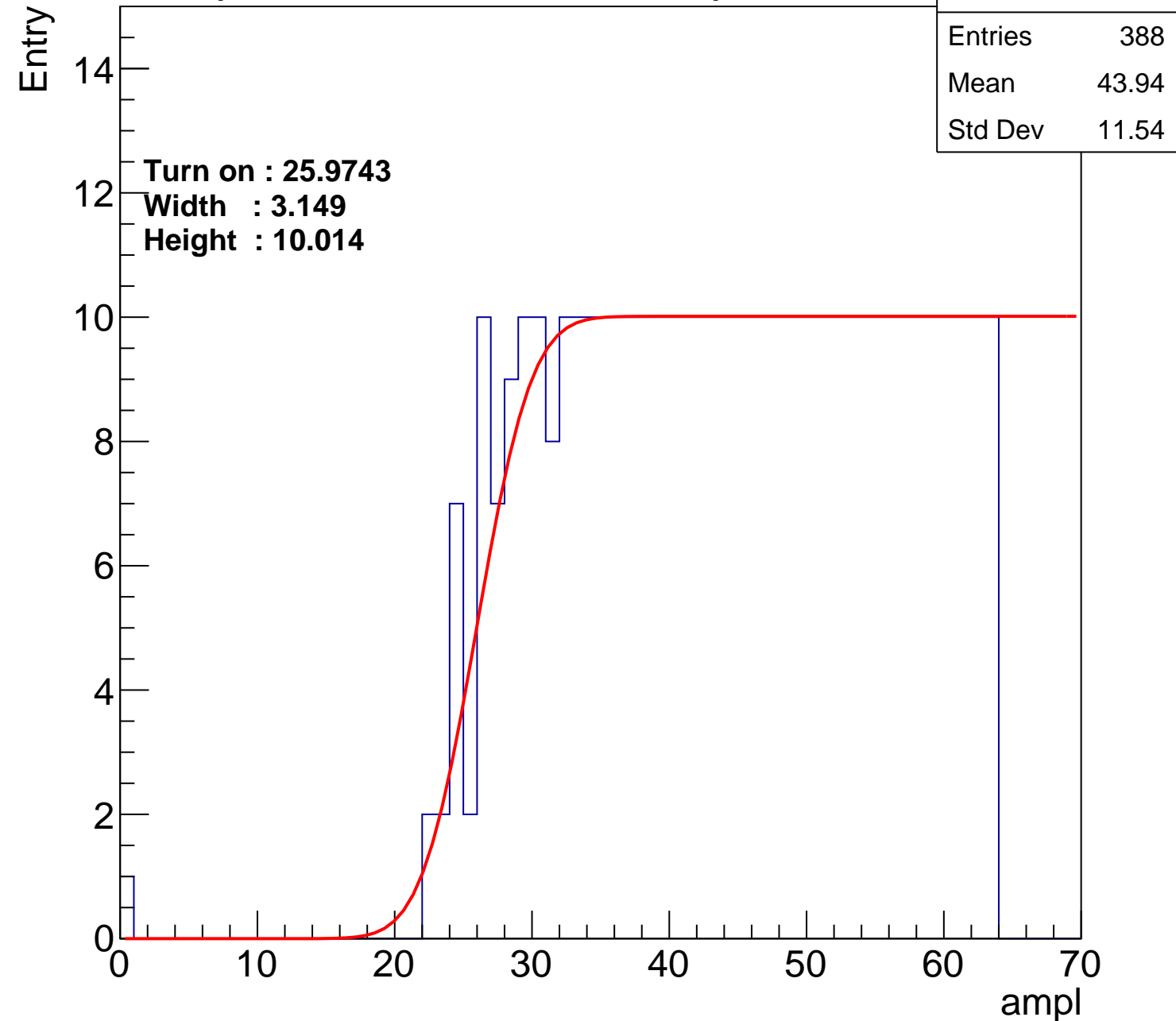
Width : 3.149

Height : 10.014

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch75

calib_packv5_042523_0143.root, FC#11, port A2

Entries	384
Mean	44.07
Std Dev	11.61

Turn on : 25.9356

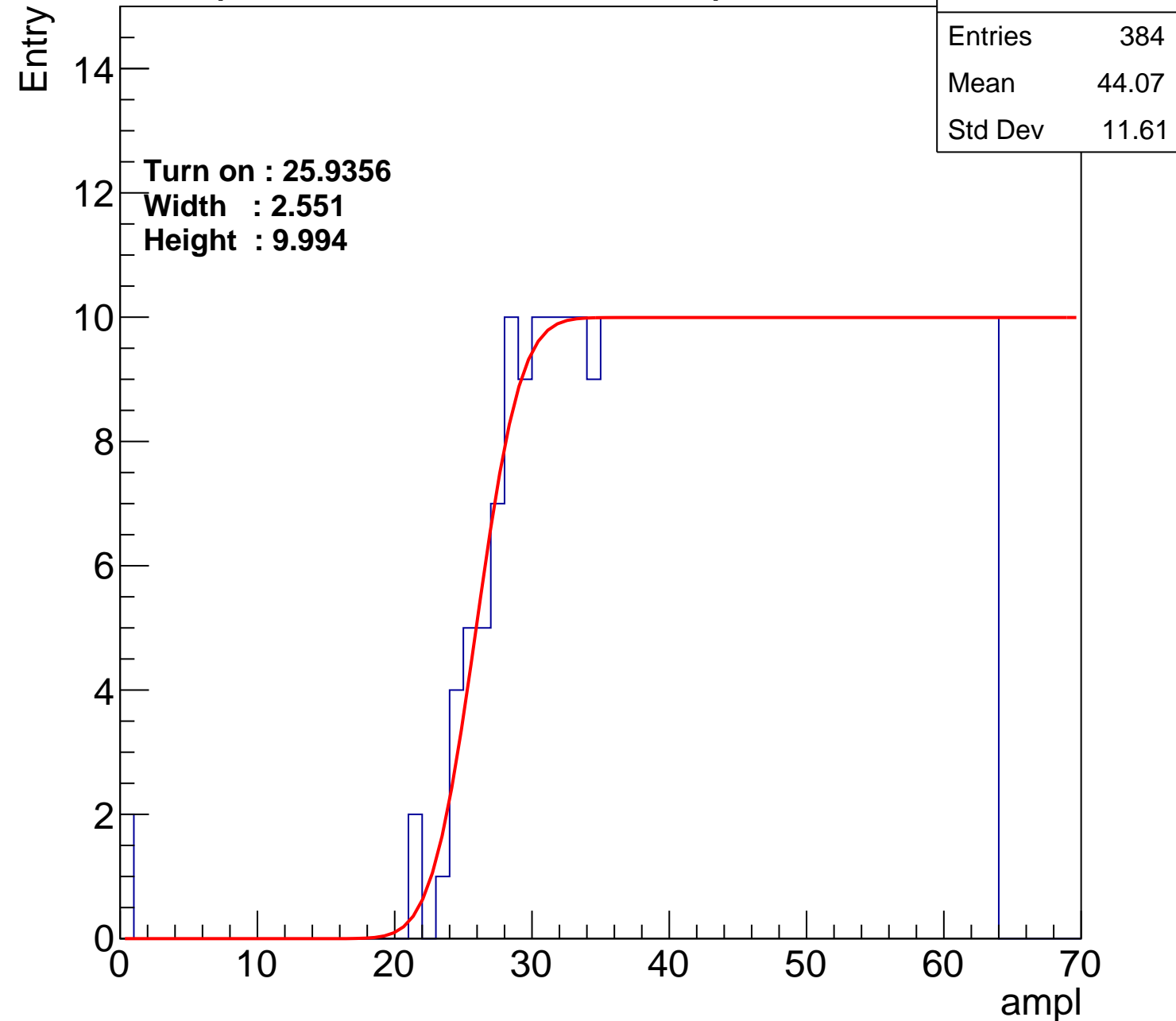
Width : 2.551

Height : 9.994

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch76

calib_packv5_042523_0143.root, FC#11, port A2

Entries	383
Mean	44.16
Std Dev	11.46

Turn on : 26.5382

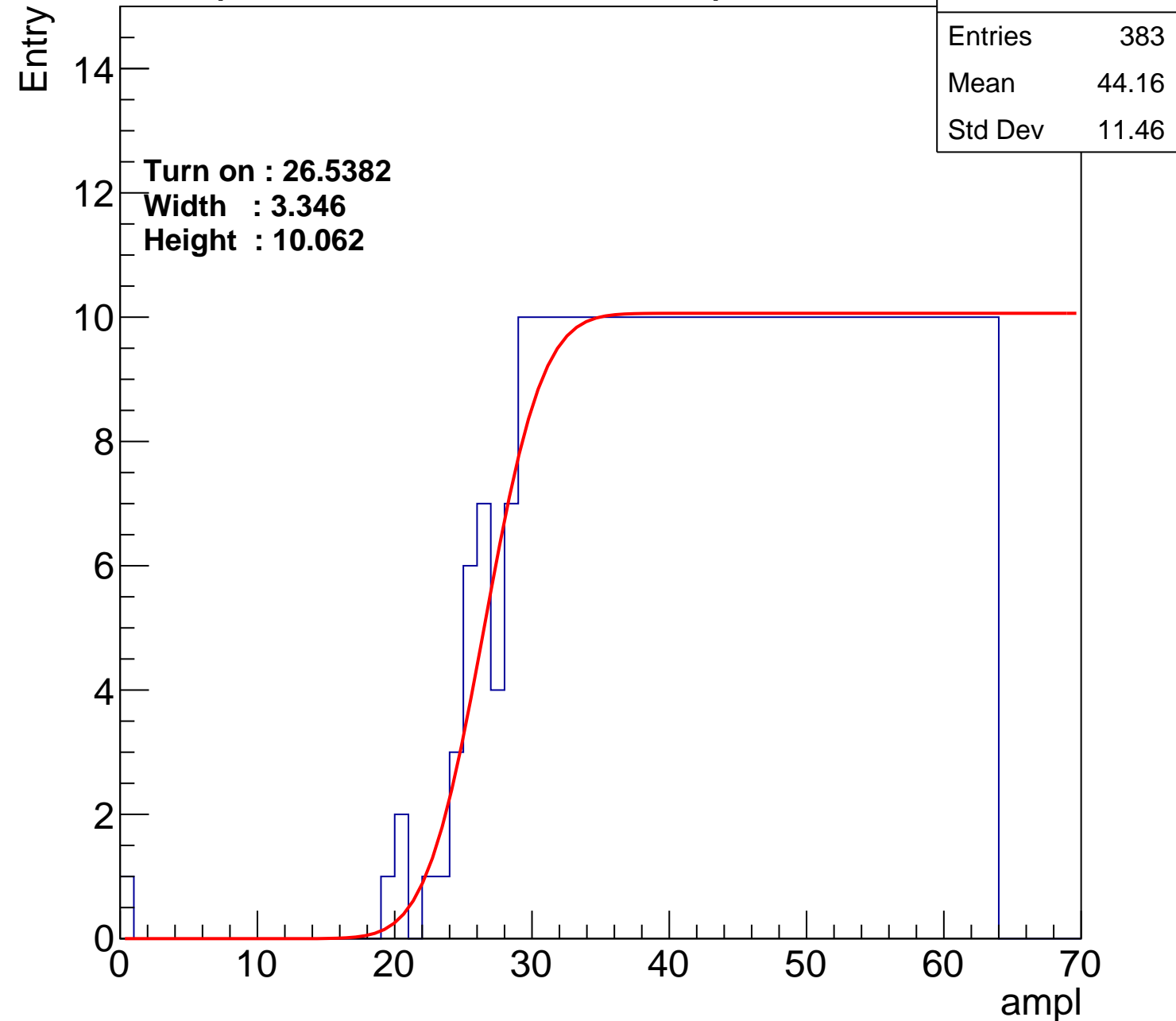
Width : 3.346

Height : 10.062

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch77

calib_packv5_042523_0143.root, FC#11, port A2

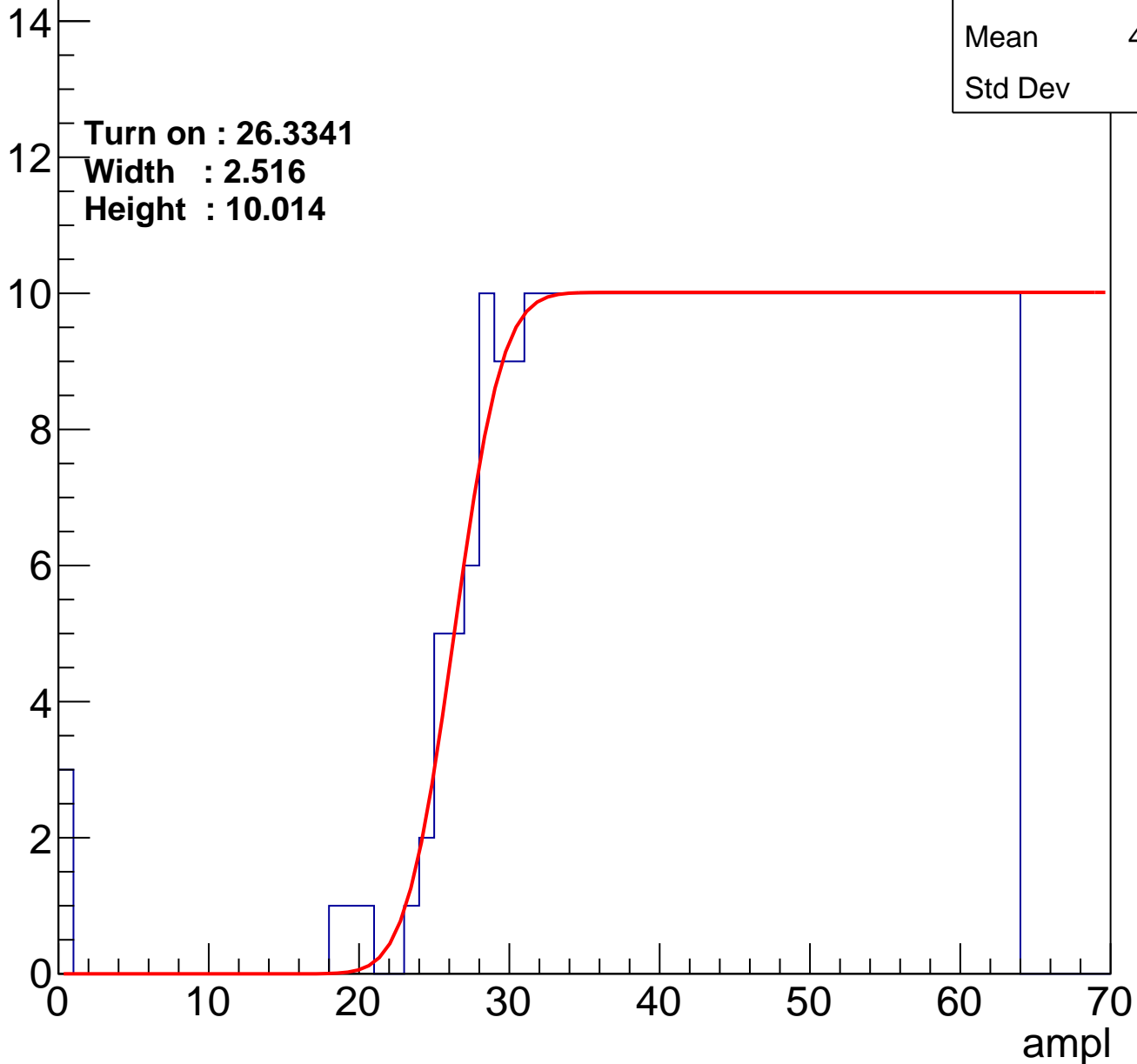
Entries	383
Mean	44.04
Std Dev	11.8

Turn on : 26.3341

Width : 2.516

Height : 10.014

Entry



B1L102S, U7-ch78

calib_packv5_042523_0143.root, FC#11, port A2

Entries	387
Mean	43.9
Std Dev	11.72

Turn on : 25.7711

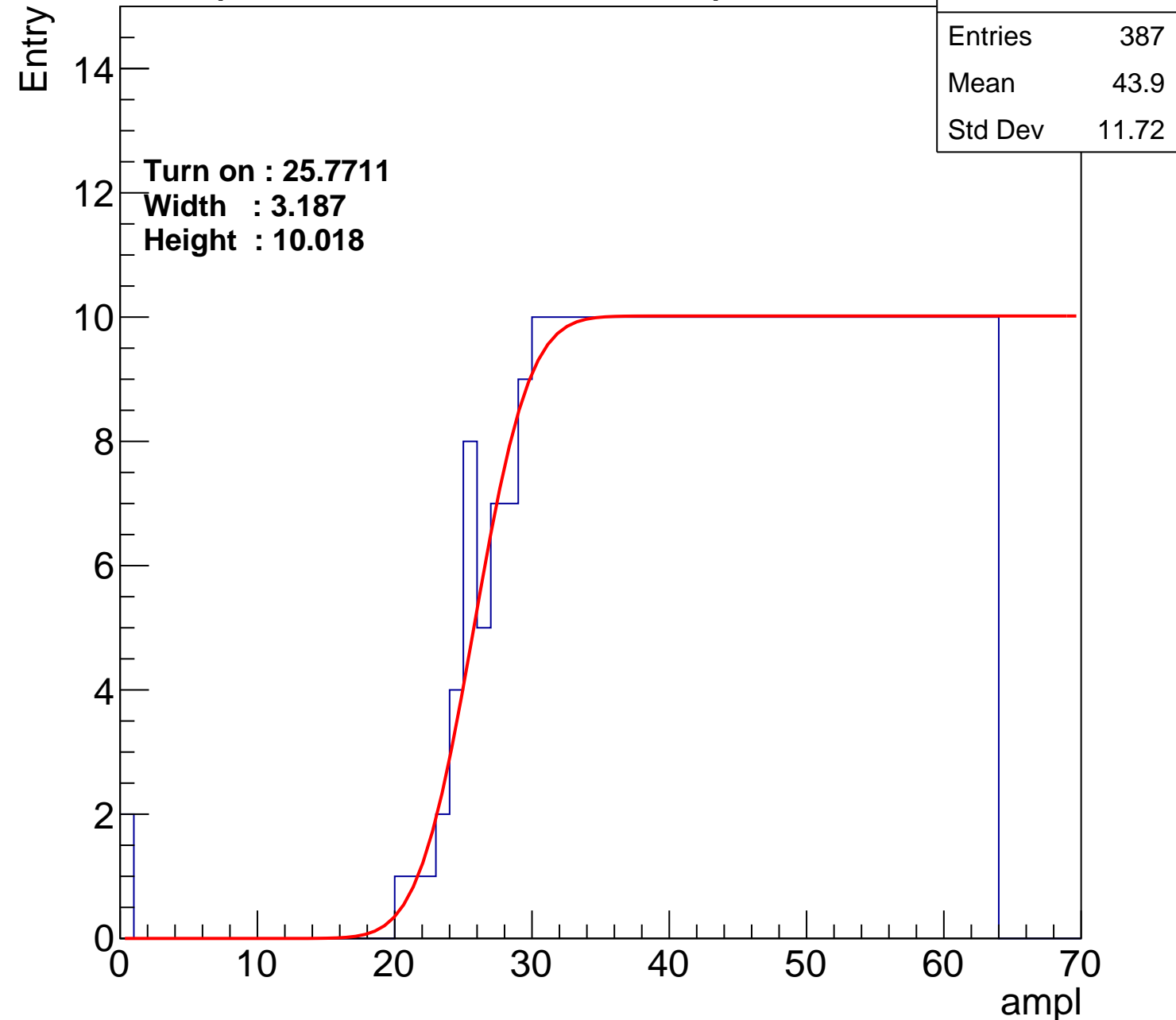
Width : 3.187

Height : 10.018

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch79

calib_packv5_042523_0143.root, FC#11, port A2

Entries	384
Mean	44.11
Std Dev	11.55

Turn on : 26.1787

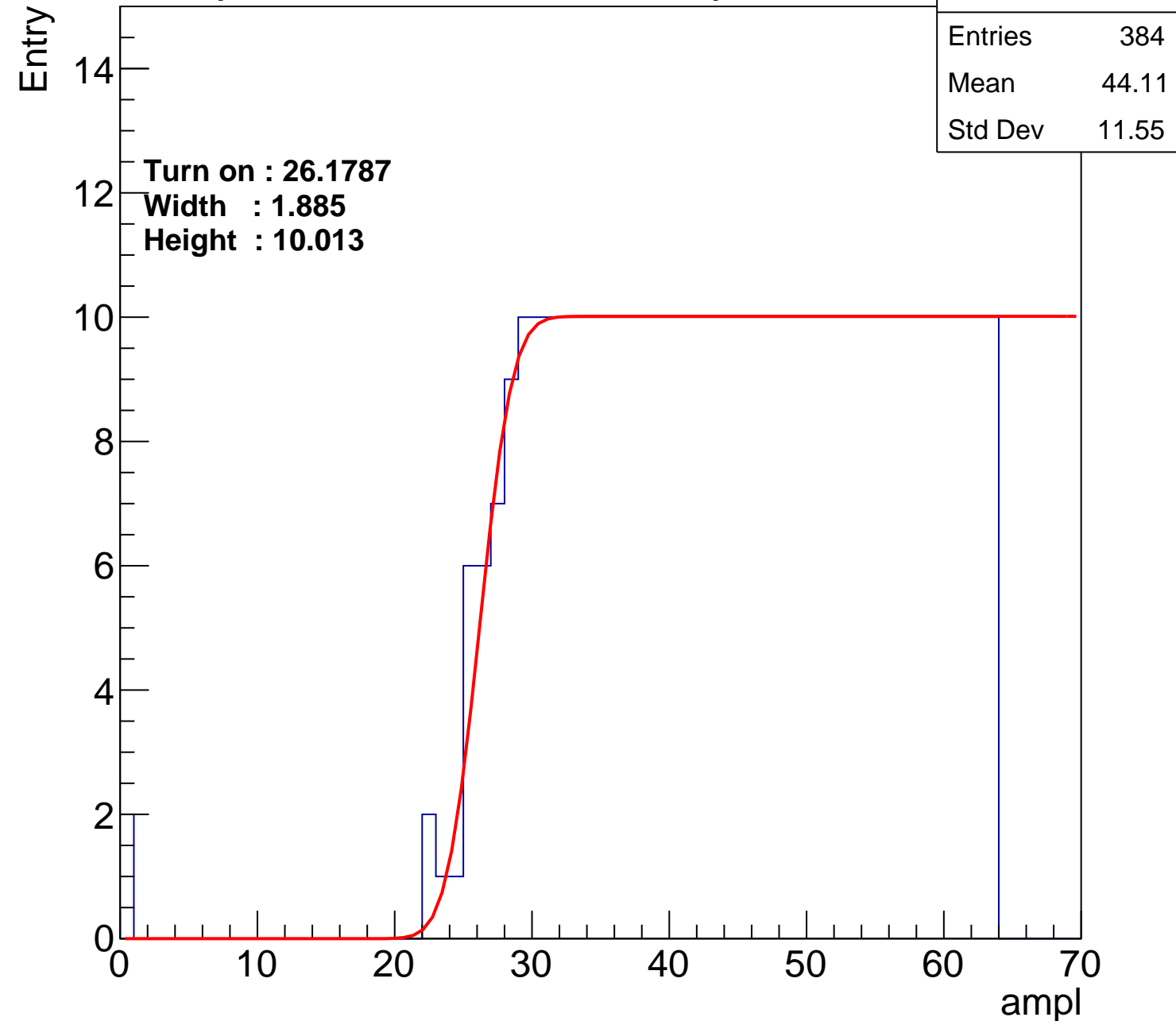
Width : 1.885

Height : 10.013

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch80

calib_packv5_042523_0143.root, FC#11, port A2

Entries	396
Mean	43.49
Std Dev	11.84

Turn on : 24.9396

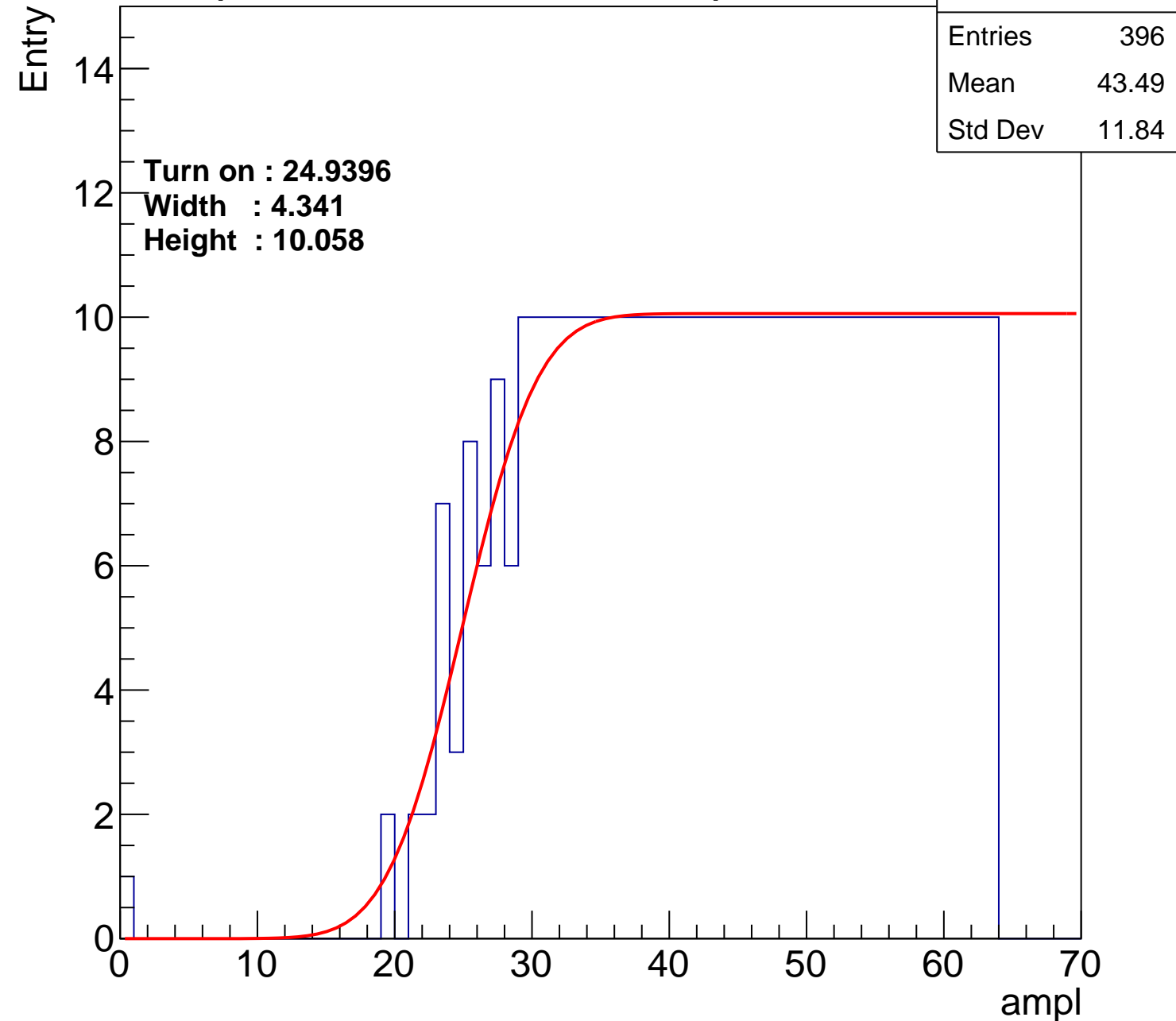
Width : 4.341

Height : 10.058

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch81

calib_packv5_042523_0143.root, FC#11, port A2

Entries	363
Mean	45.06
Std Dev	11.15

Turn on : 28.3482

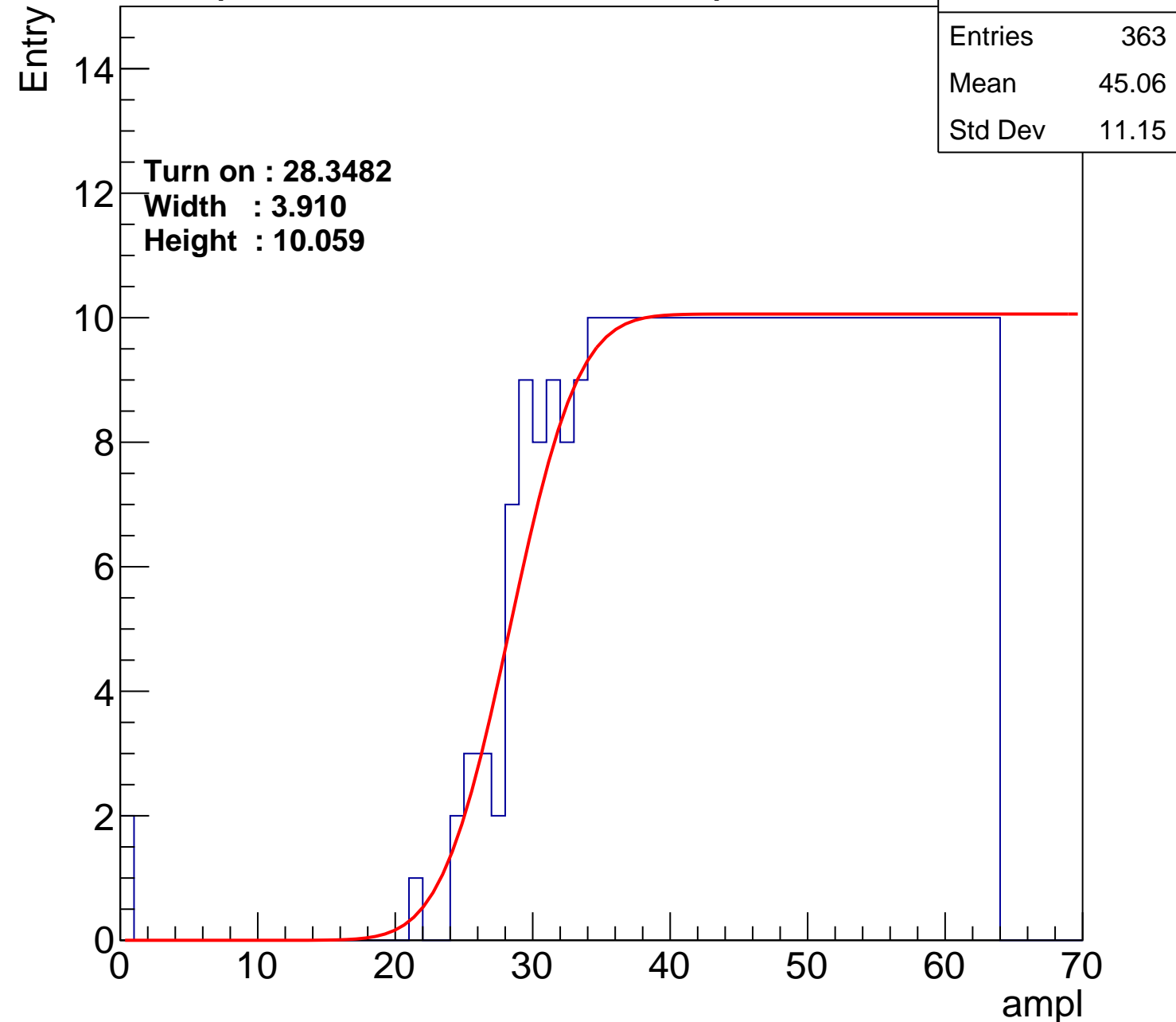
Width : 3.910

Height : 10.059

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch82

calib_packv5_042523_0143.root, FC#11, port A2

Entries	406
Mean	42.99
Std Dev	12.18

Turn on : 23.9223

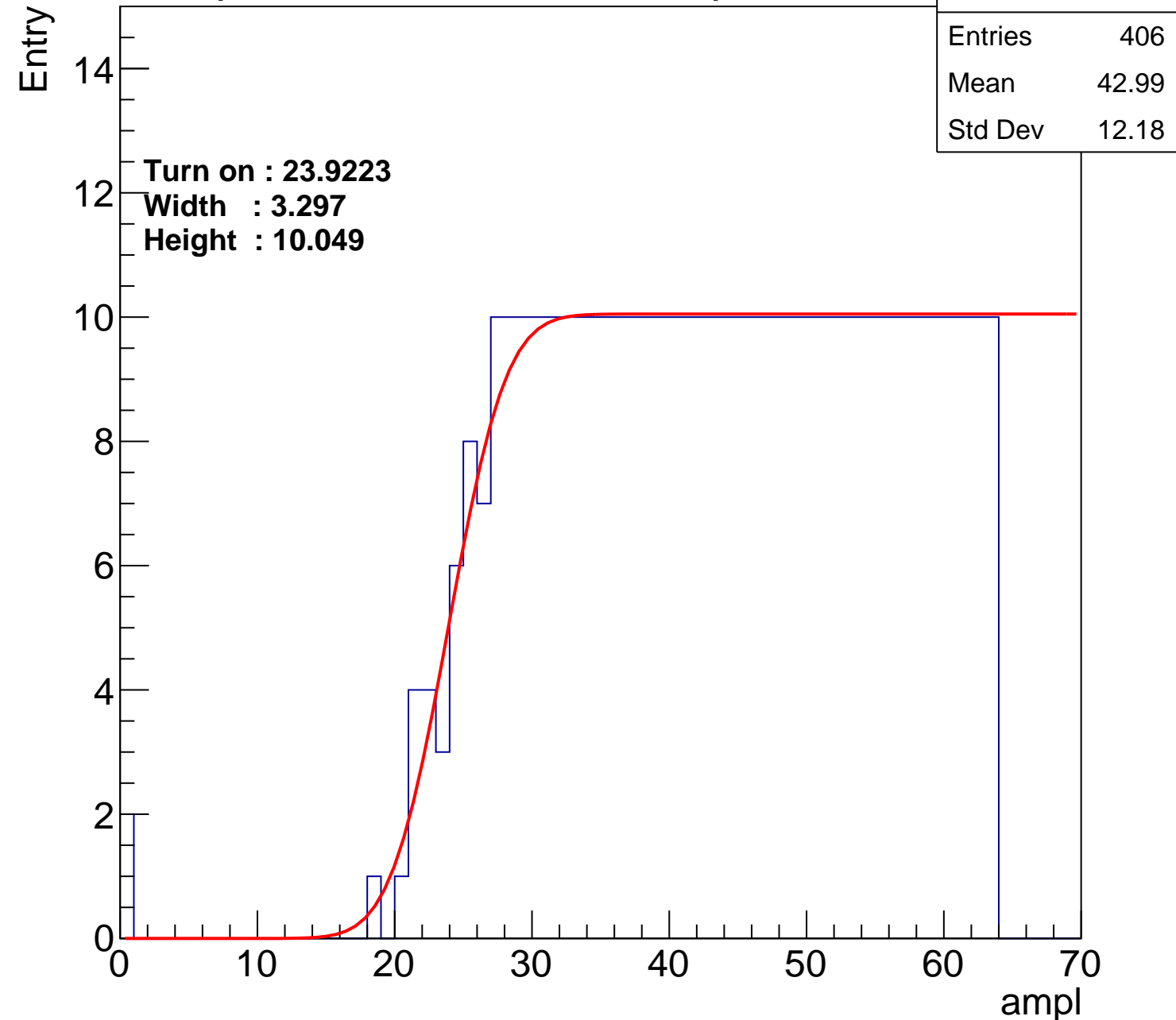
Width : 3.297

Height : 10.049

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch83

calib_packv5_042523_0143.root, FC#11, port A2

Entries	393
Mean	43.63
Std Dev	11.83

Turn on : 24.5834

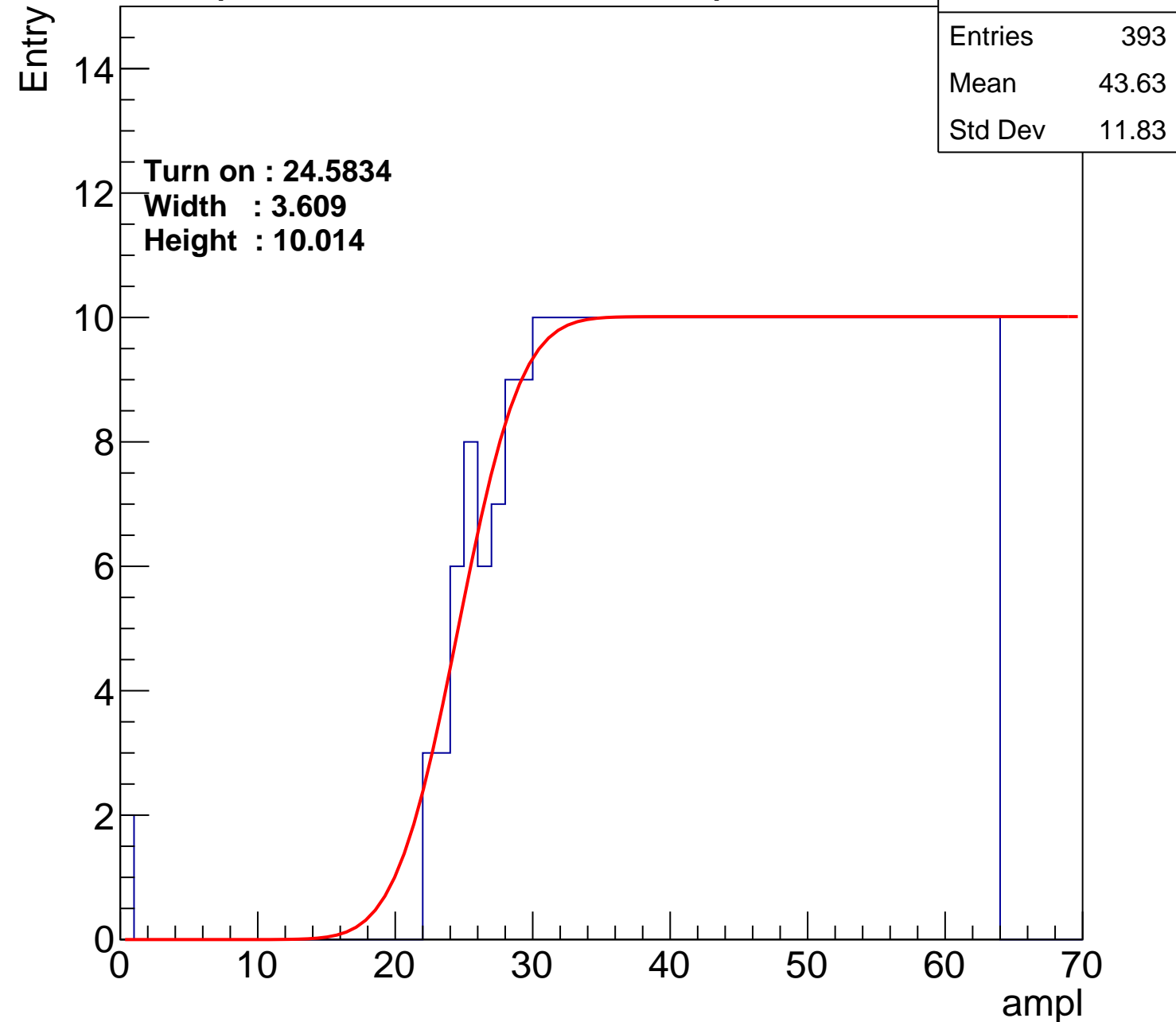
Width : 3.609

Height : 10.014

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch84

calib_packv5_042523_0143.root, FC#11, port A2

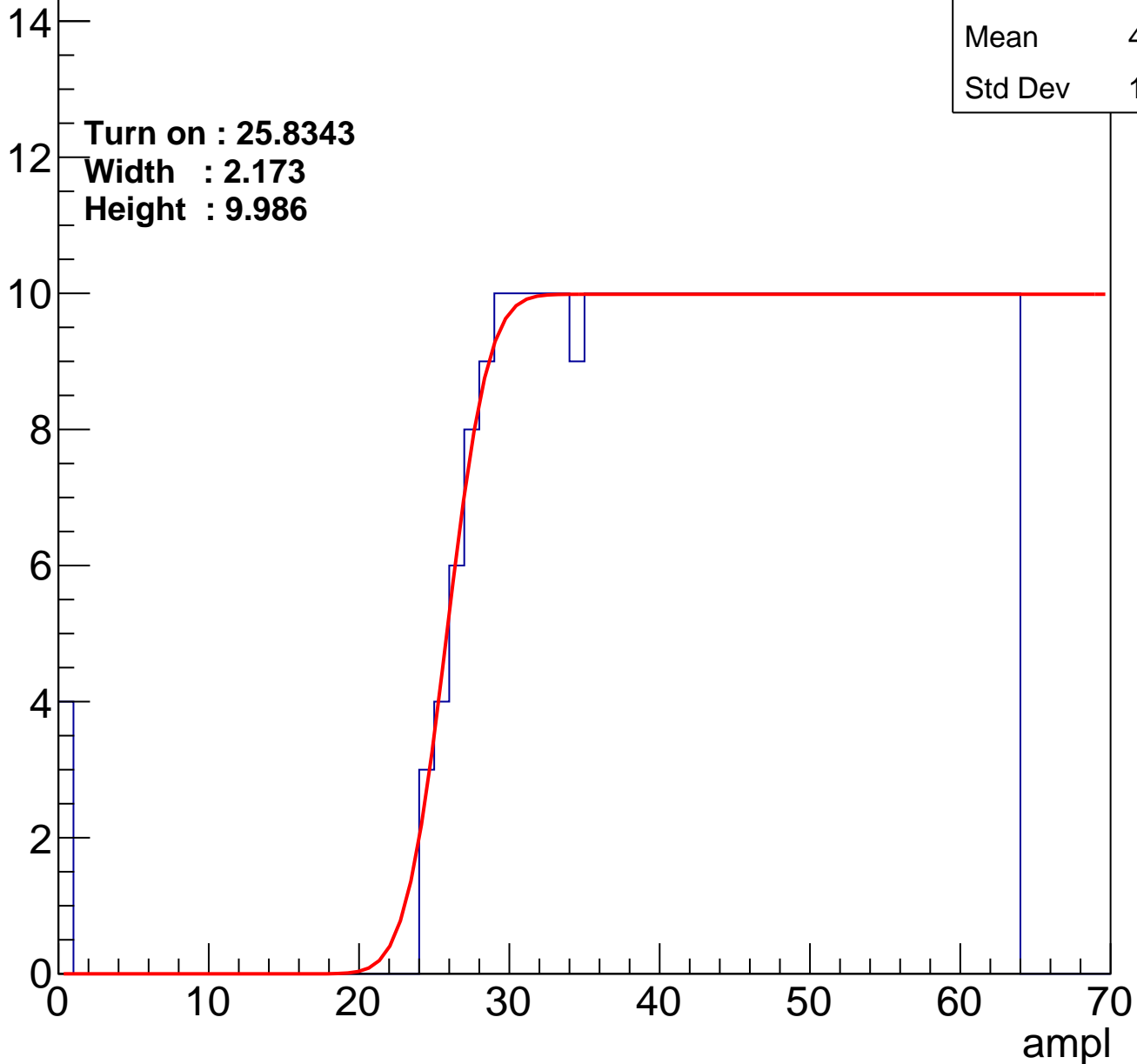
Entries	383
Mean	44.03
Std Dev	11.87

Turn on : 25.8343

Width : 2.173

Height : 9.986

Entry



B1L102S, U7-ch85

calib_packv5_042523_0143.root, FC#11, port A2

Entries	376
Mean	44.38
Std Dev	11.61

Turn on : 26.4053

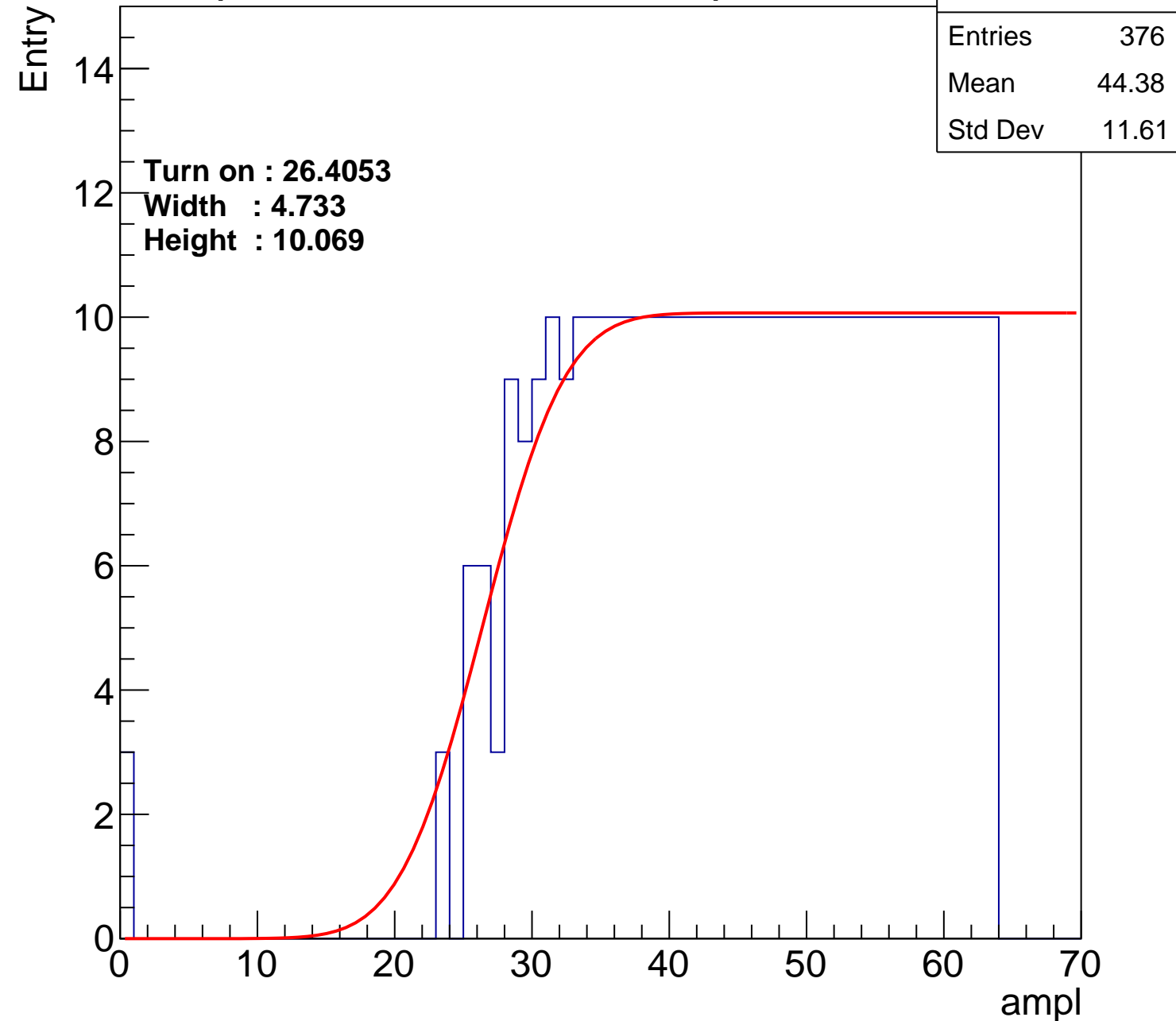
Width : 4.733

Height : 10.069

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch86

calib_packv5_042523_0143.root, FC#11, port A2

Entries	386
Mean	43.85
Std Dev	11.91

Turn on : 25.9829

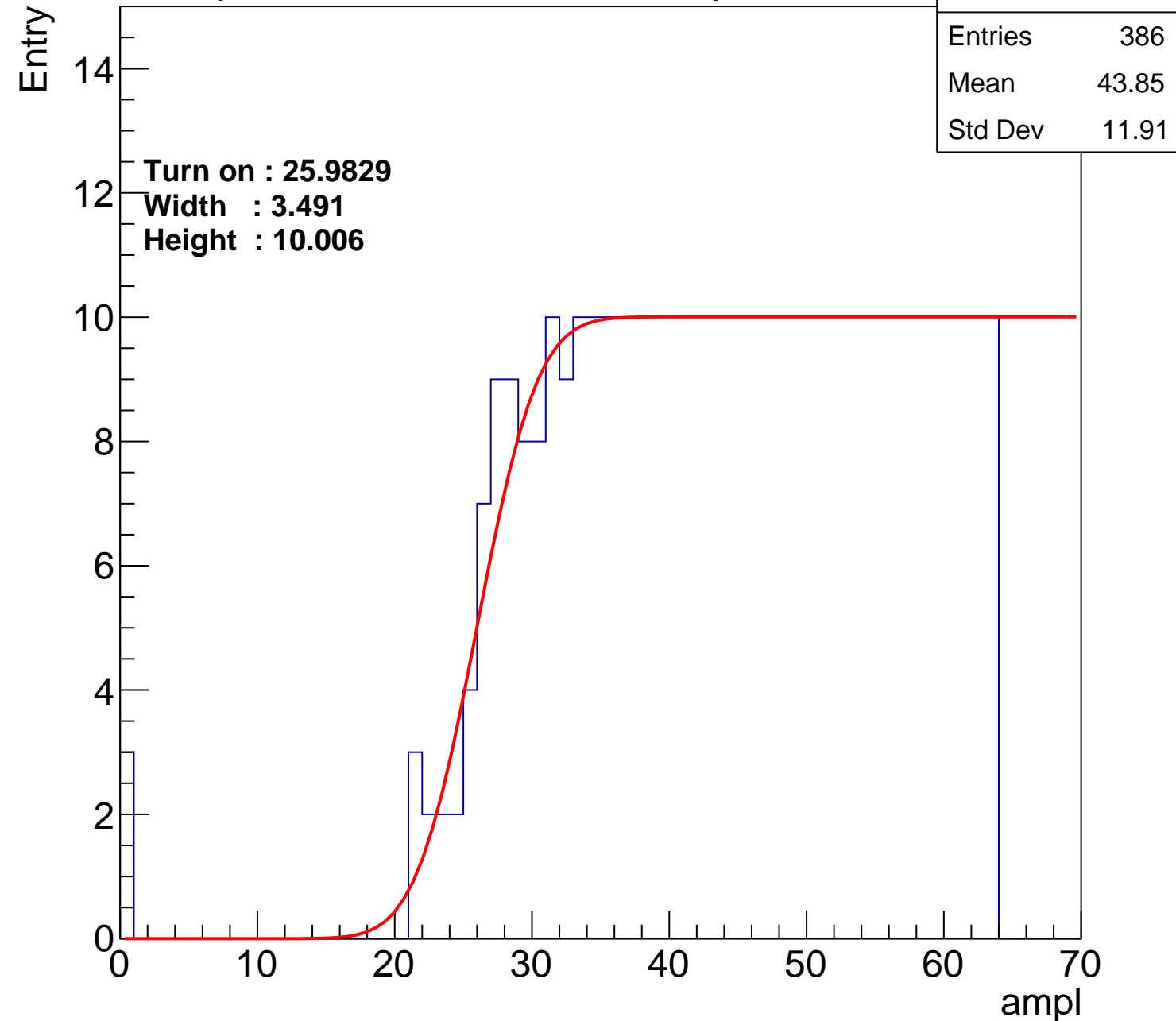
Width : 3.491

Height : 10.006

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch87

calib_packv5_042523_0143.root, FC#11, port A2

Entries	374
Mean	44.69
Std Dev	11.35

Turn on : 28.2091

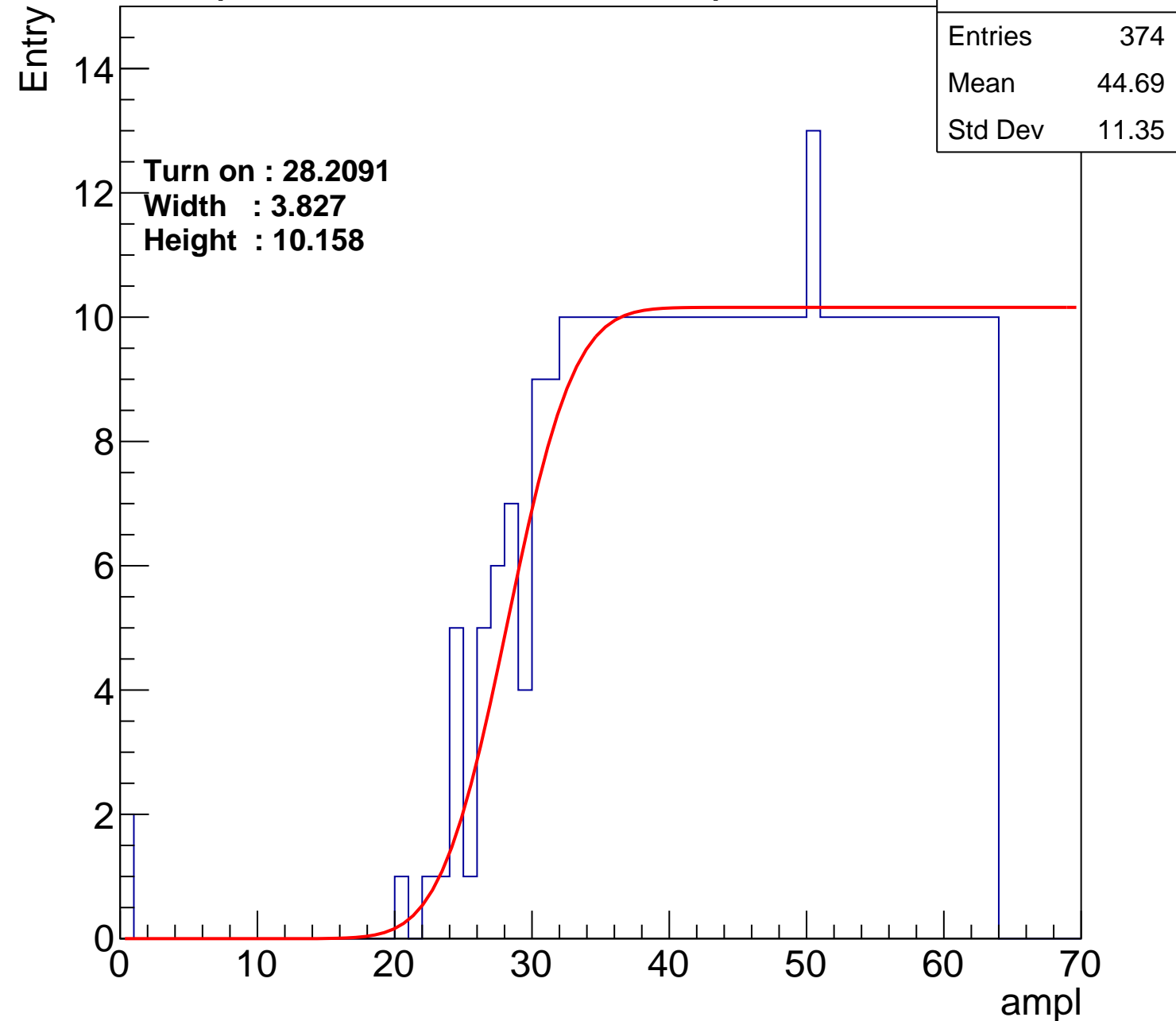
Width : 3.827

Height : 10.158

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch88

calib_packv5_042523_0143.root, FC#11, port A2

Entries	394
Mean	43.58
Std Dev	11.85

Turn on : 25.1735

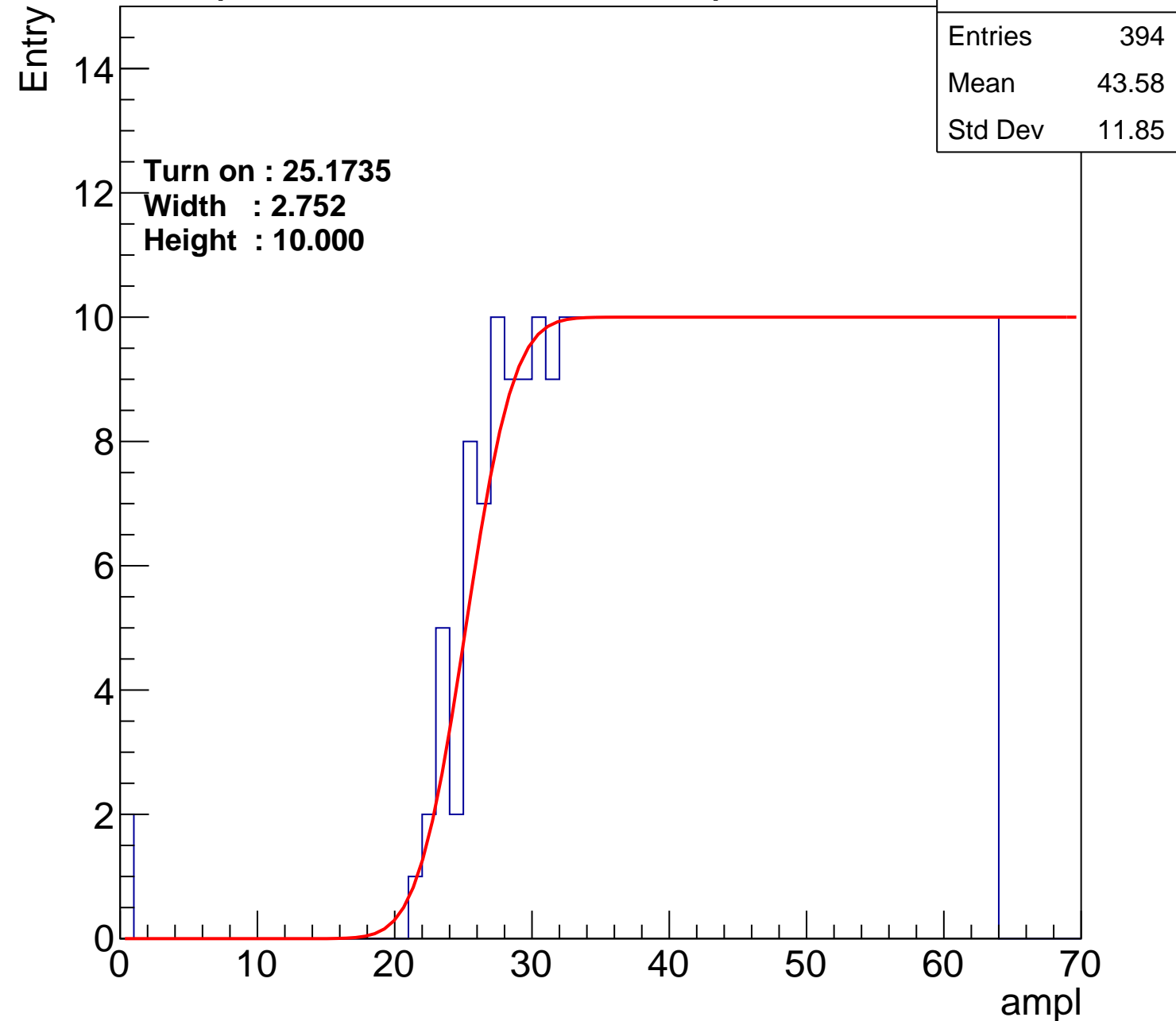
Width : 2.752

Height : 10.000

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch89

calib_packv5_042523_0143.root, FC#11, port A2

Entries	396
Mean	43.36
Std Dev	12.23

Turn on : 24.3865

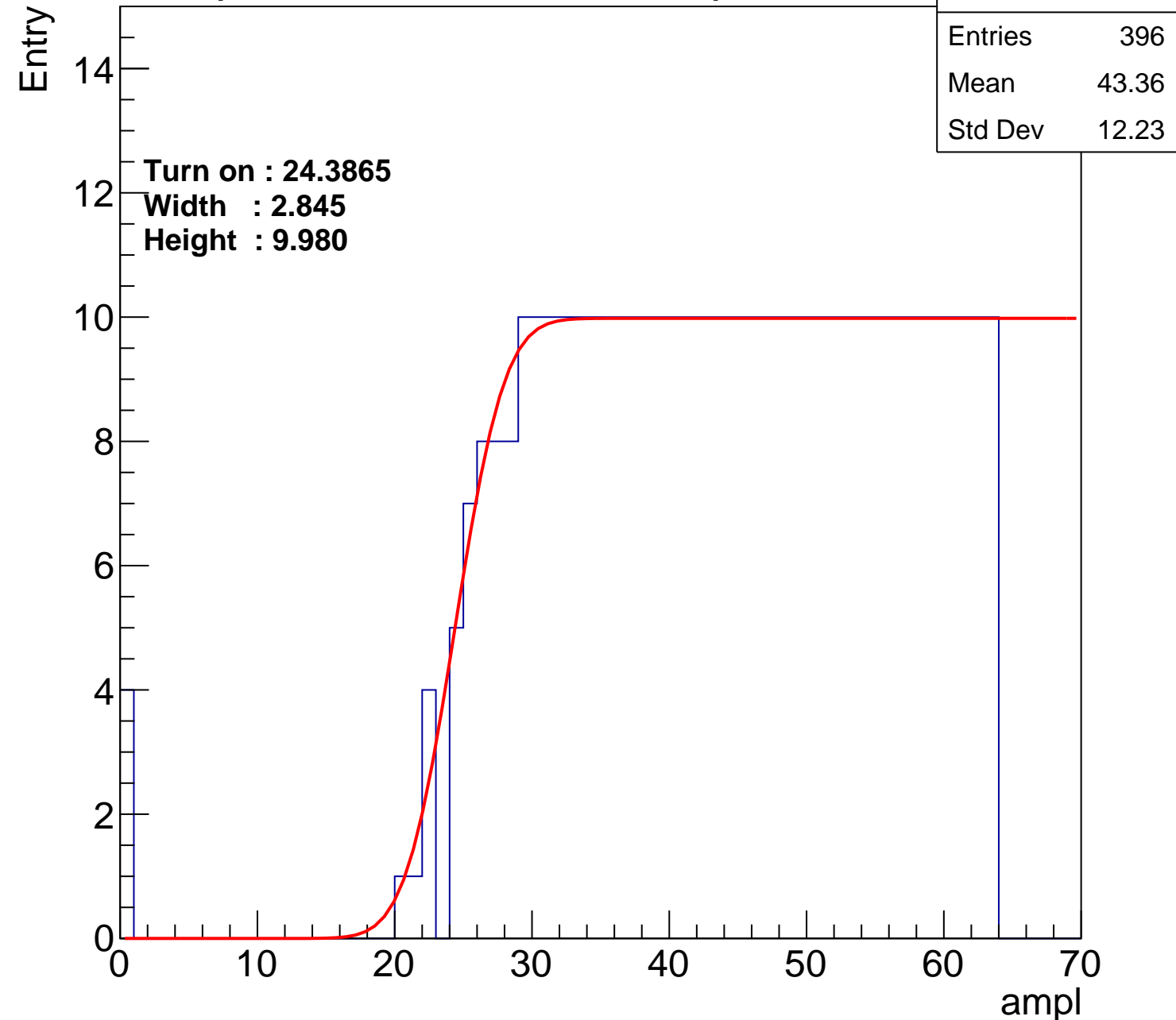
Width : 2.845

Height : 9.980

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch90

calib_packv5_042523_0143.root, FC#11, port A2

Entries	372
Mean	44.34
Std Dev	12.06

Turn on : 28.0552

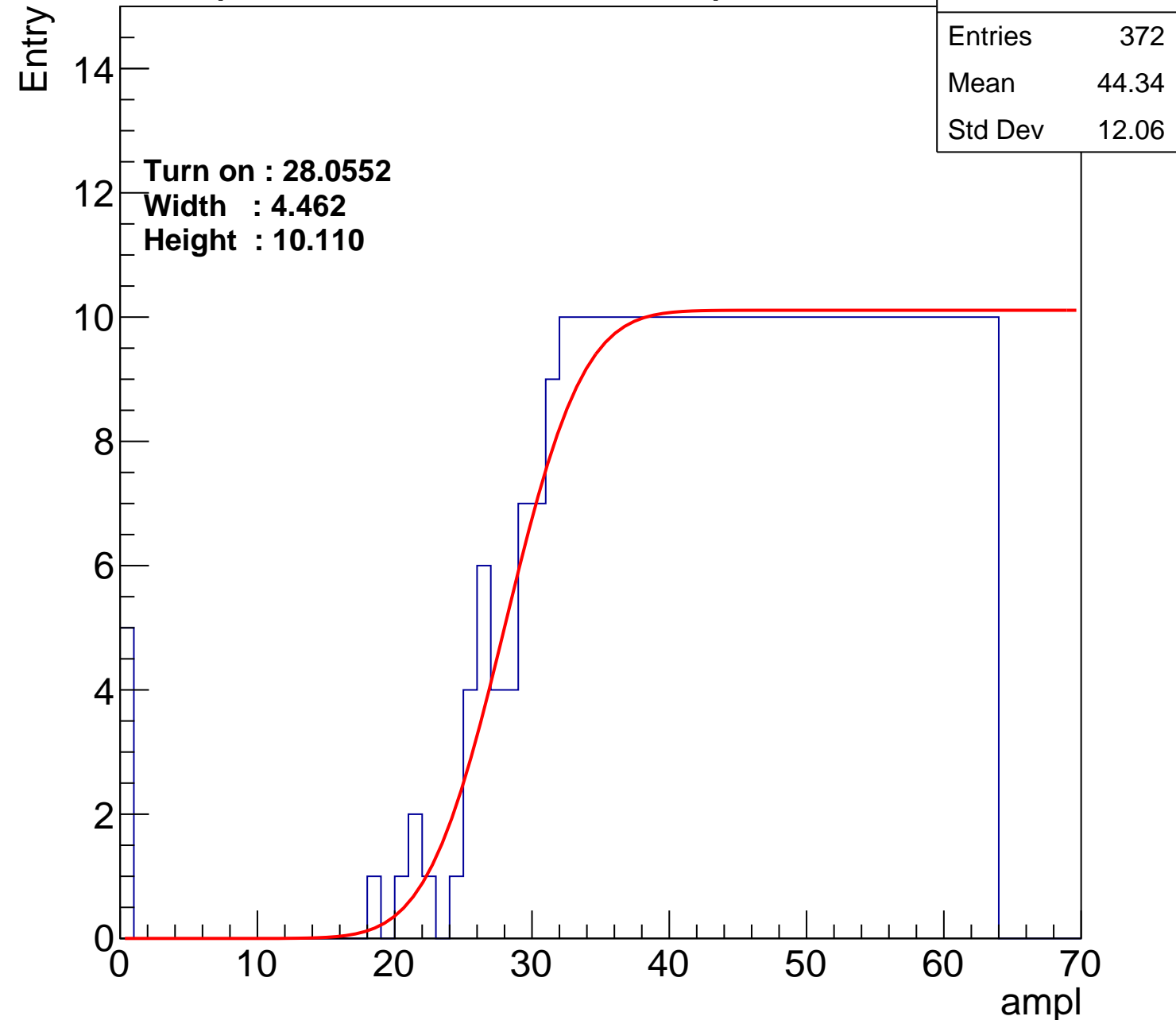
Width : 4.462

Height : 10.110

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch91

calib_packv5_042523_0143.root, FC#11, port A2

Entries	381
Mean	44.19
Std Dev	11.58

Turn on : 26.4617

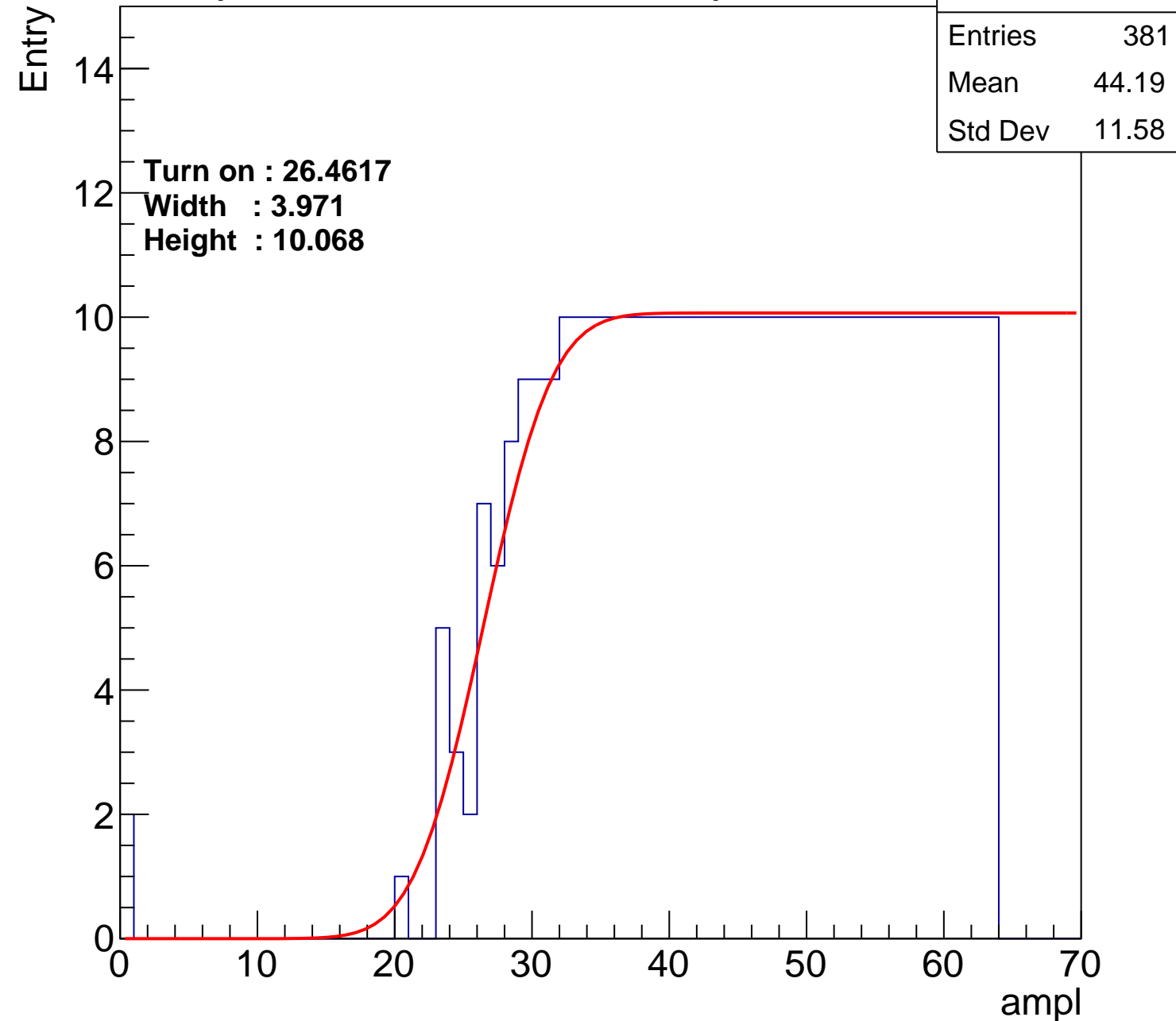
Width : 3.971

Height : 10.068

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch92

calib_packv5_042523_0143.root, FC#11, port A2

Entries	377
Mean	44.49
Std Dev	11.23

Turn on : 26.6399

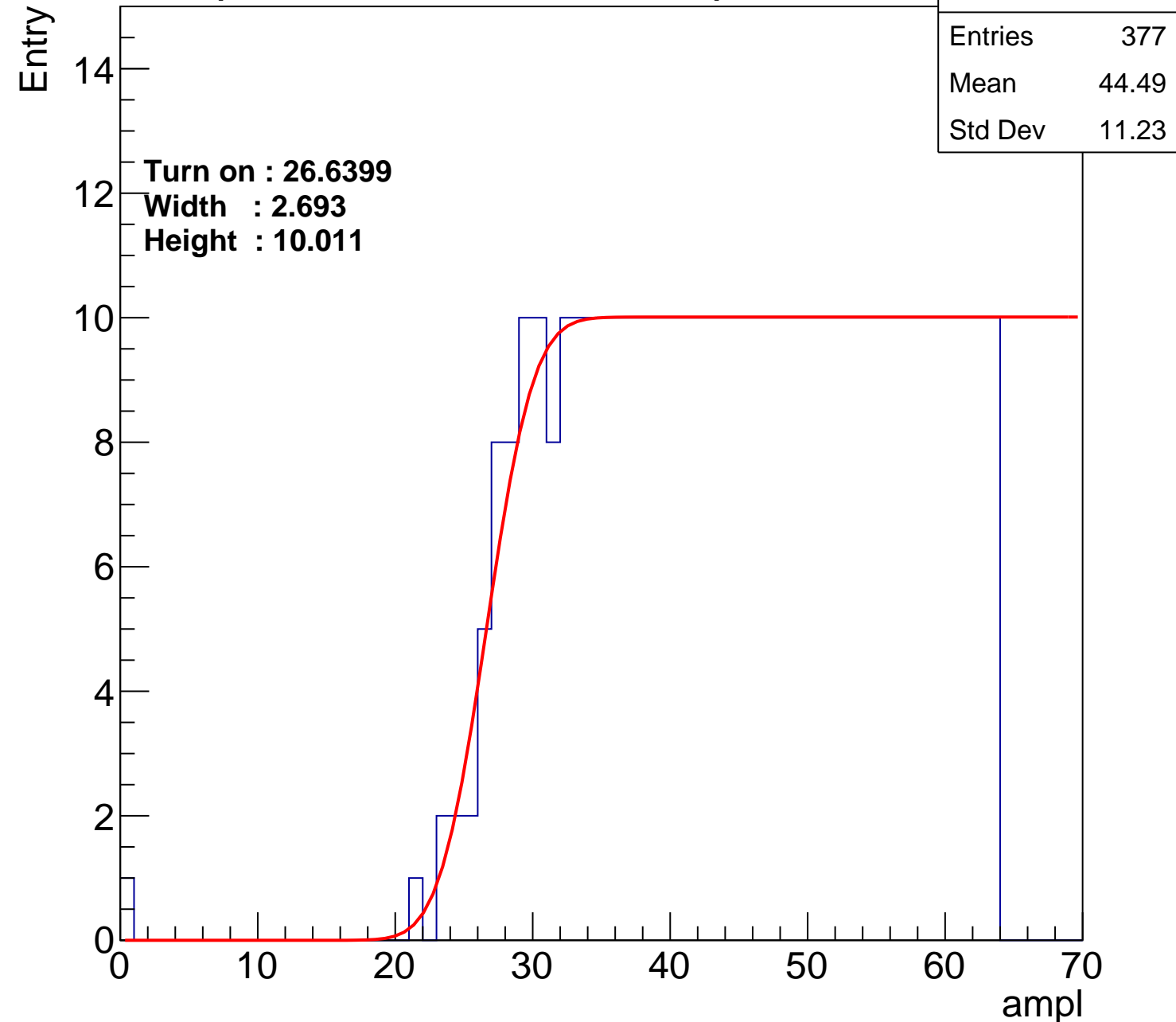
Width : 2.693

Height : 10.011

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch93

calib_packv5_042523_0143.root, FC#11, port A2

Entries	380
Mean	44.17
Std Dev	11.74

Turn on : 26.7206

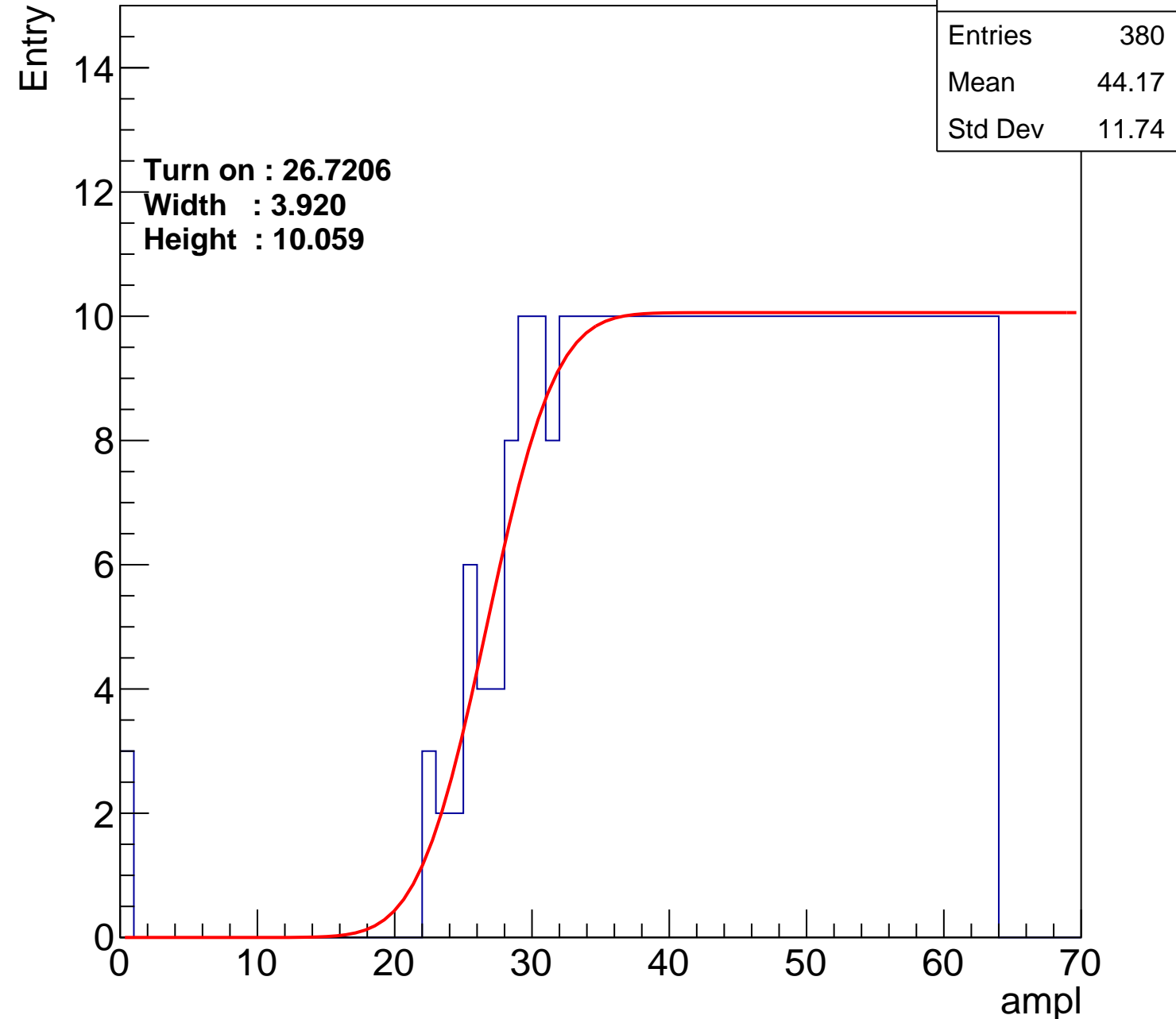
Width : 3.920

Height : 10.059

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch94

calib_packv5_042523_0143.root, FC#11, port A2

Entries	392
Mean	43.65
Std Dev	11.86

Turn on : 25.3150

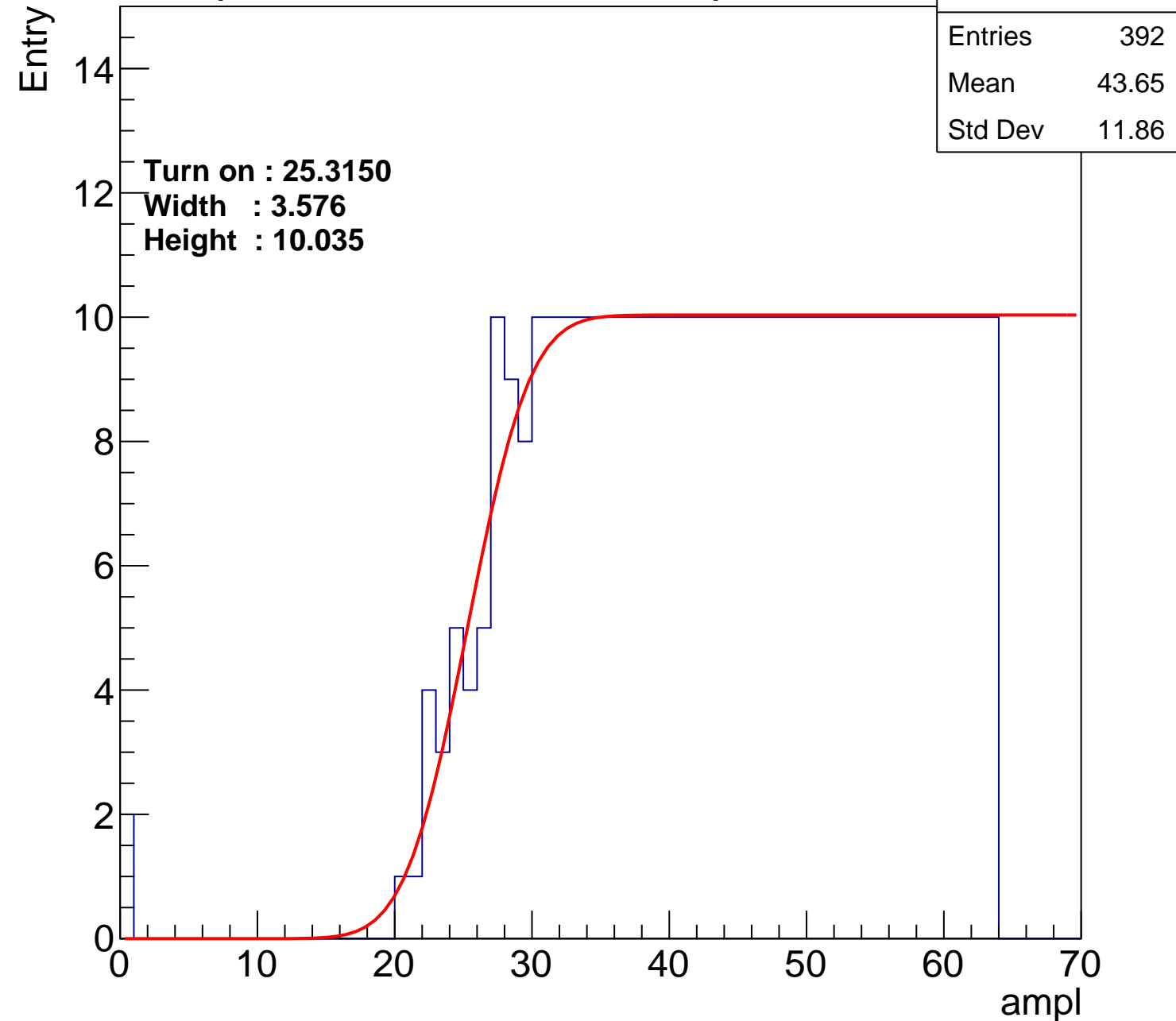
Width : 3.576

Height : 10.035

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch95

calib_packv5_042523_0143.root, FC#11, port A2

Entries	385
Mean	43.9
Std Dev	11.97

Turn on : 26.3056

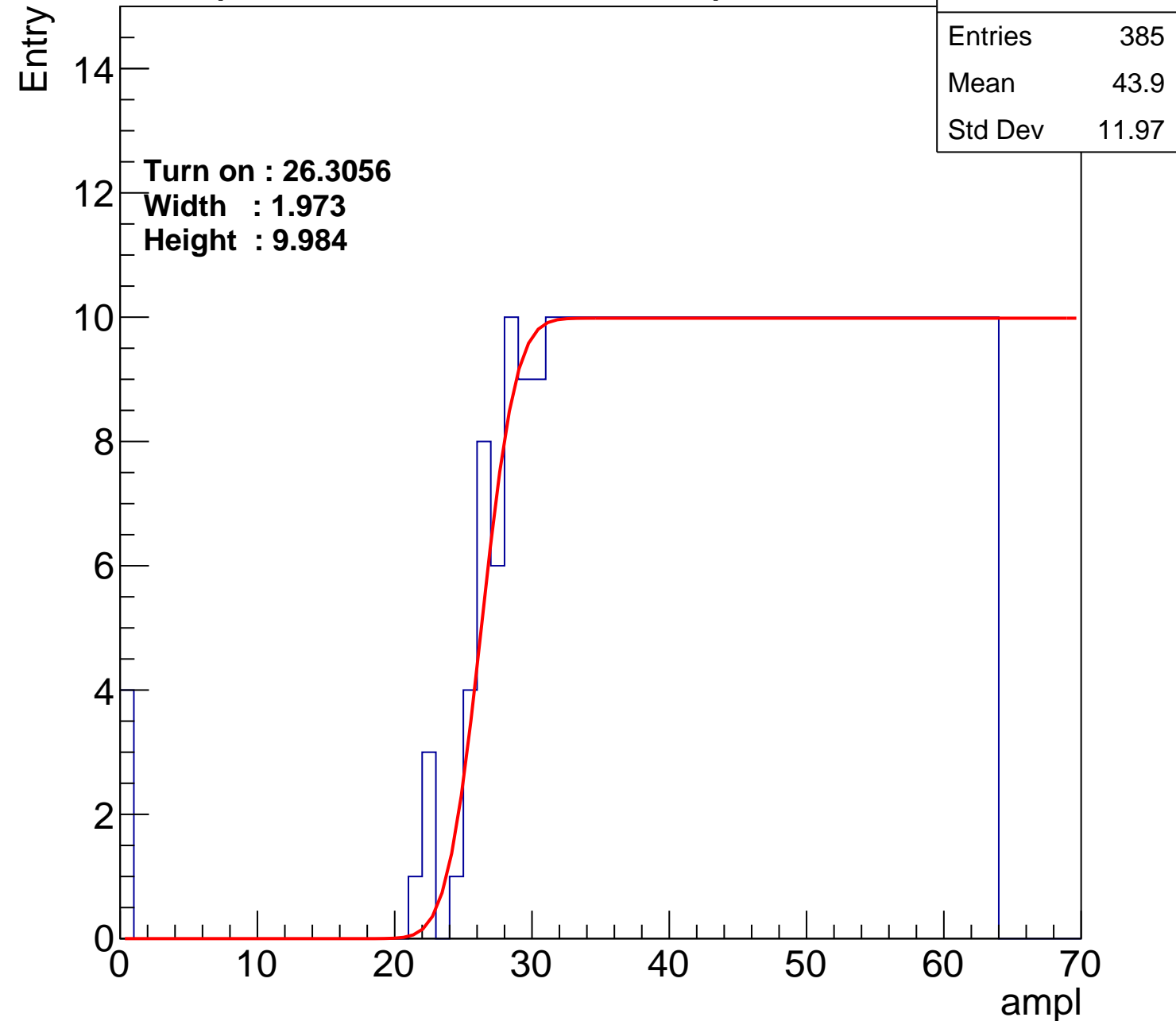
Width : 1.973

Height : 9.984

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch96

calib_packv5_042523_0143.root, FC#11, port A2

Entries	374
Mean	44.57
Std Dev	11.35

Turn on : 27.2770

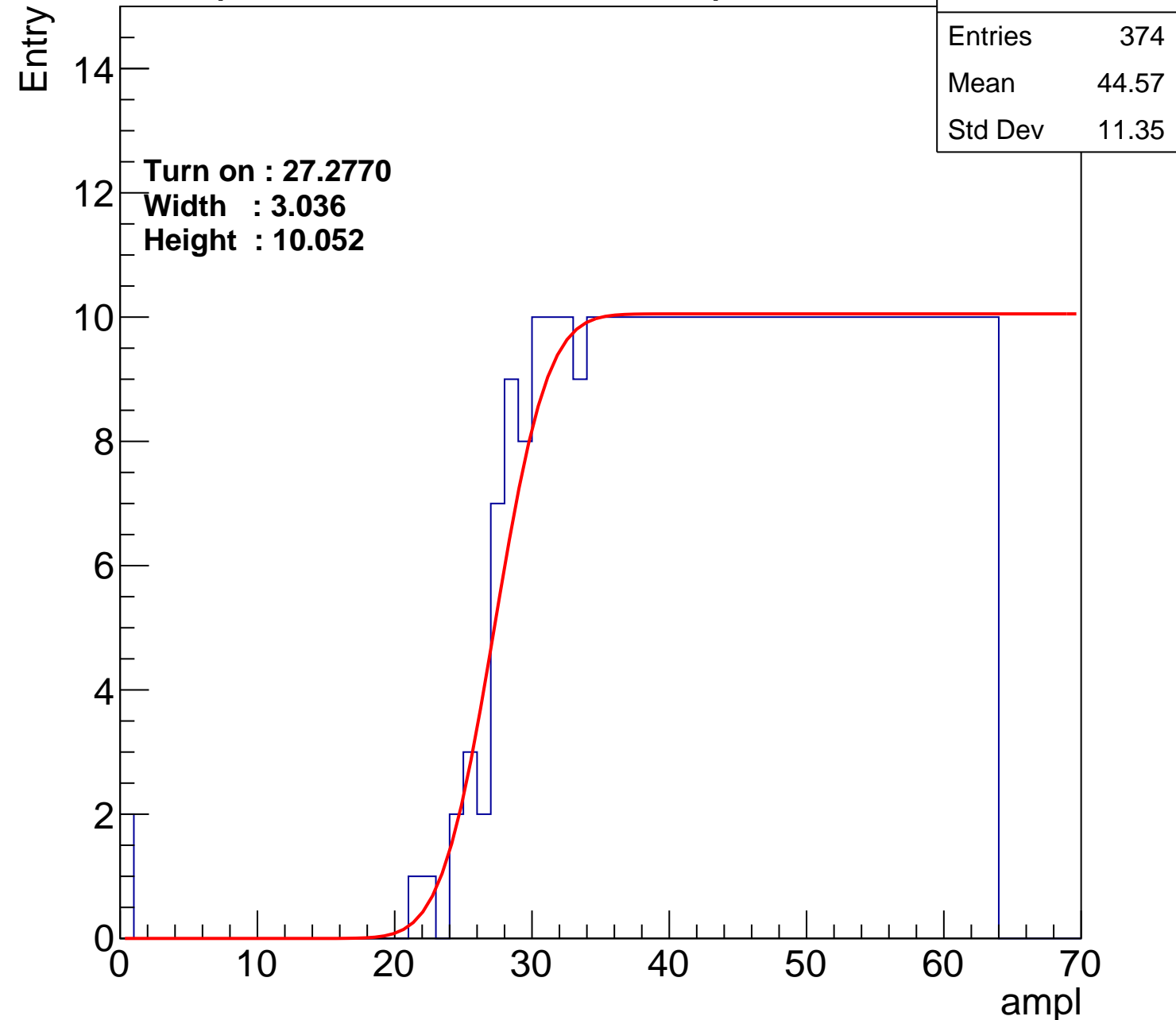
Width : 3.036

Height : 10.052

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch97

calib_packv5_042523_0143.root, FC#11, port A2

Entries	396
Mean	43.5
Std Dev	11.89

Turn on : 24.5868

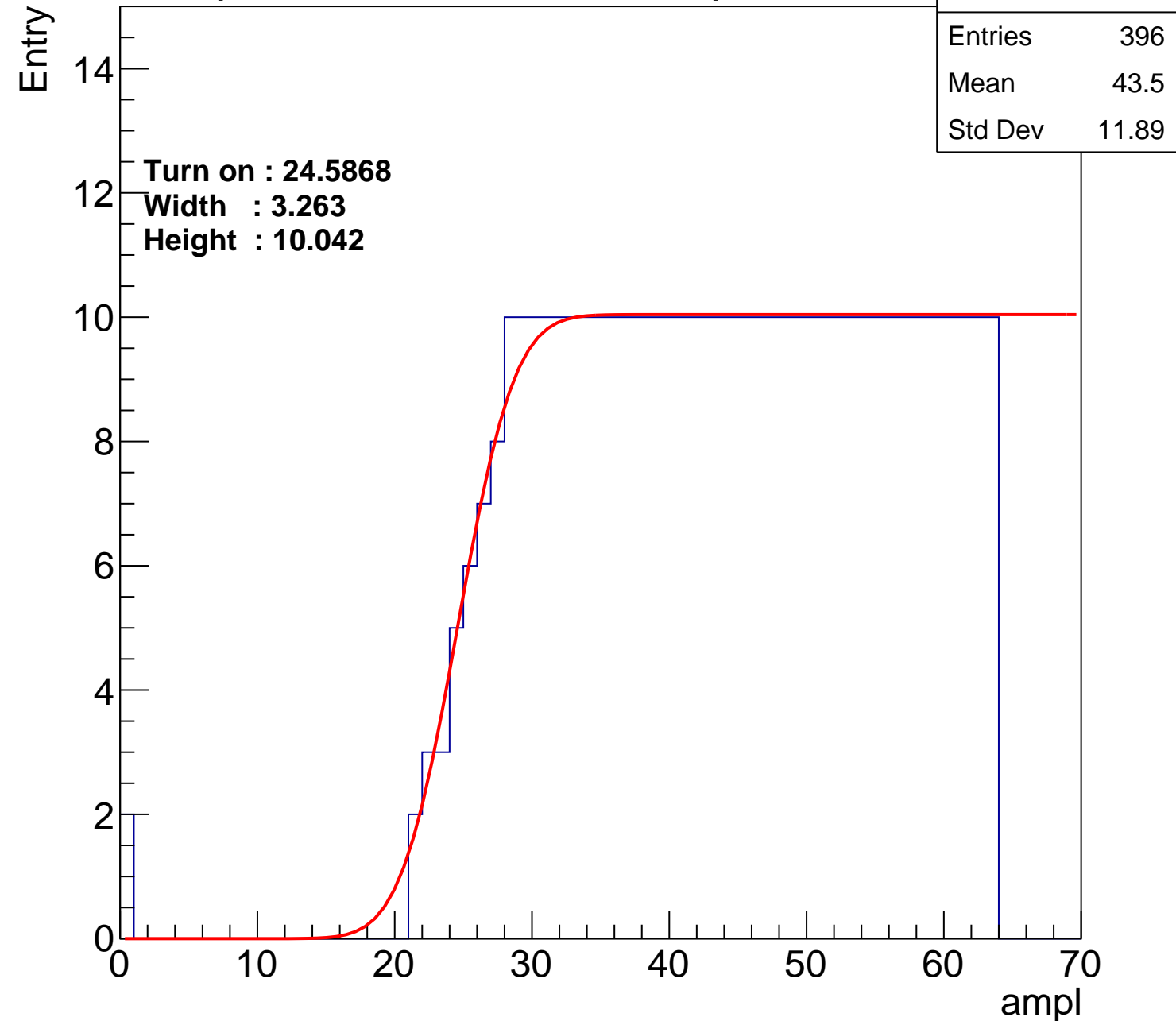
Width : 3.263

Height : 10.042

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch98

calib_packv5_042523_0143.root, FC#11, port A2

Entries	383
Mean	44.04
Std Dev	11.79

Turn on : 26.7778

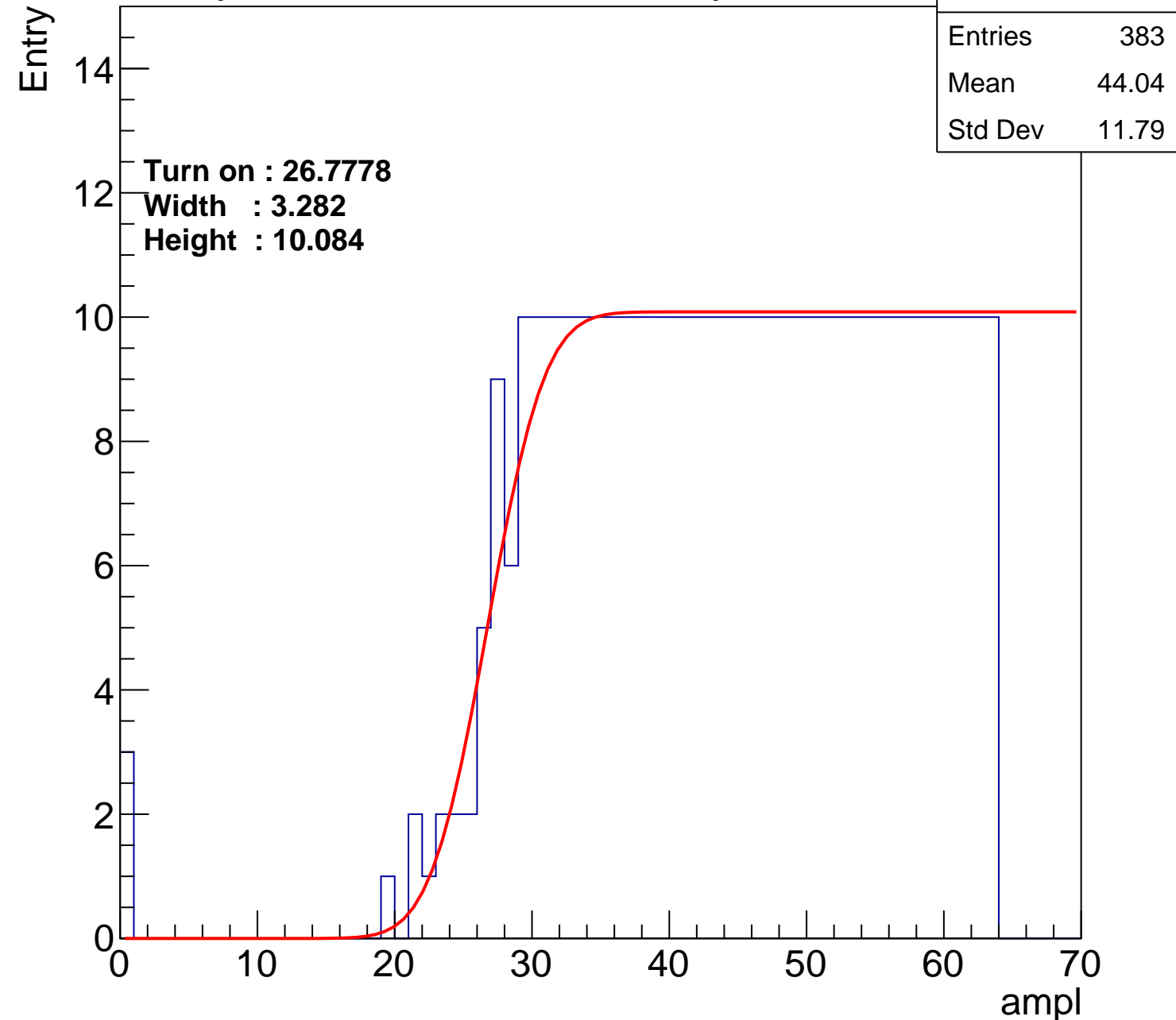
Width : 3.282

Height : 10.084

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch99

calib_packv5_042523_0143.root, FC#11, port A2

Entries	400
Mean	43.17
Std Dev	12.32

Turn on : 24.0834

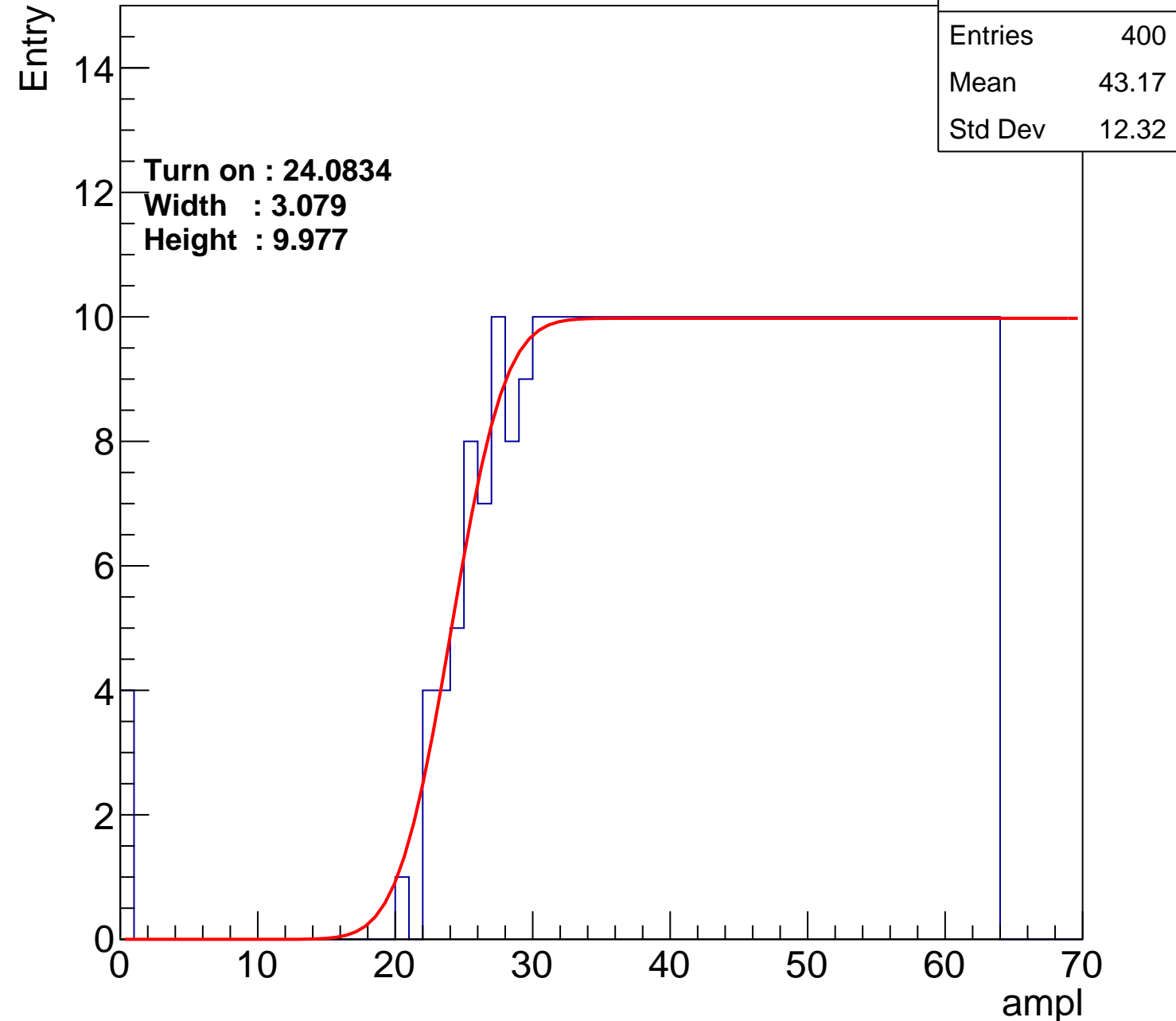
Width : 3.079

Height : 9.977

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch100

calib_packv5_042523_0143.root, FC#11, port A2

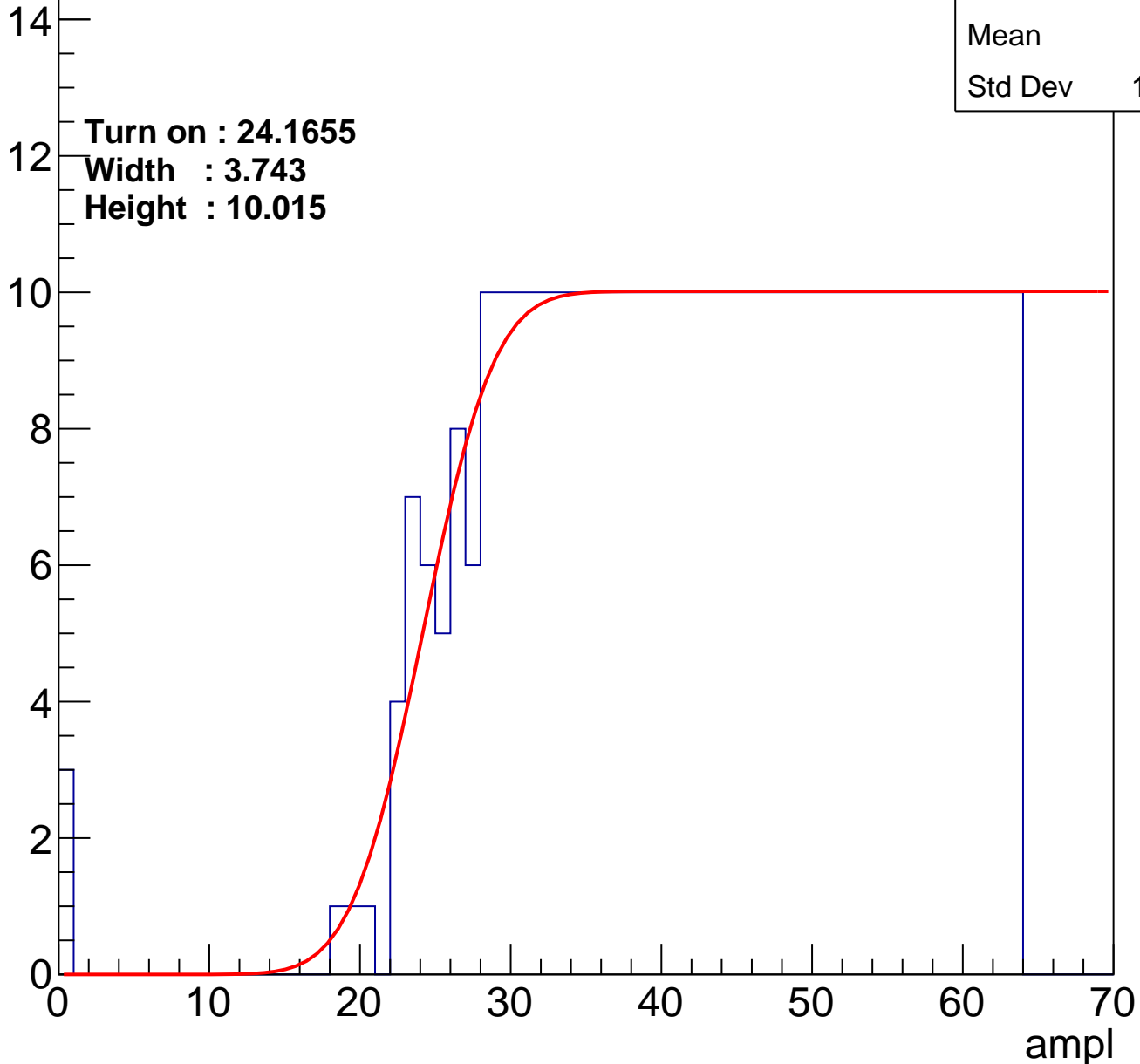
Entries	402
Mean	43.1
Std Dev	12.27

Turn on : 24.1655

Width : 3.743

Height : 10.015

Entry



B1L102S, U7-ch101

calib_packv5_042523_0143.root, FC#11, port A2

Entries	398
Mean	43.29
Std Dev	12.18

Turn on : 24.8432

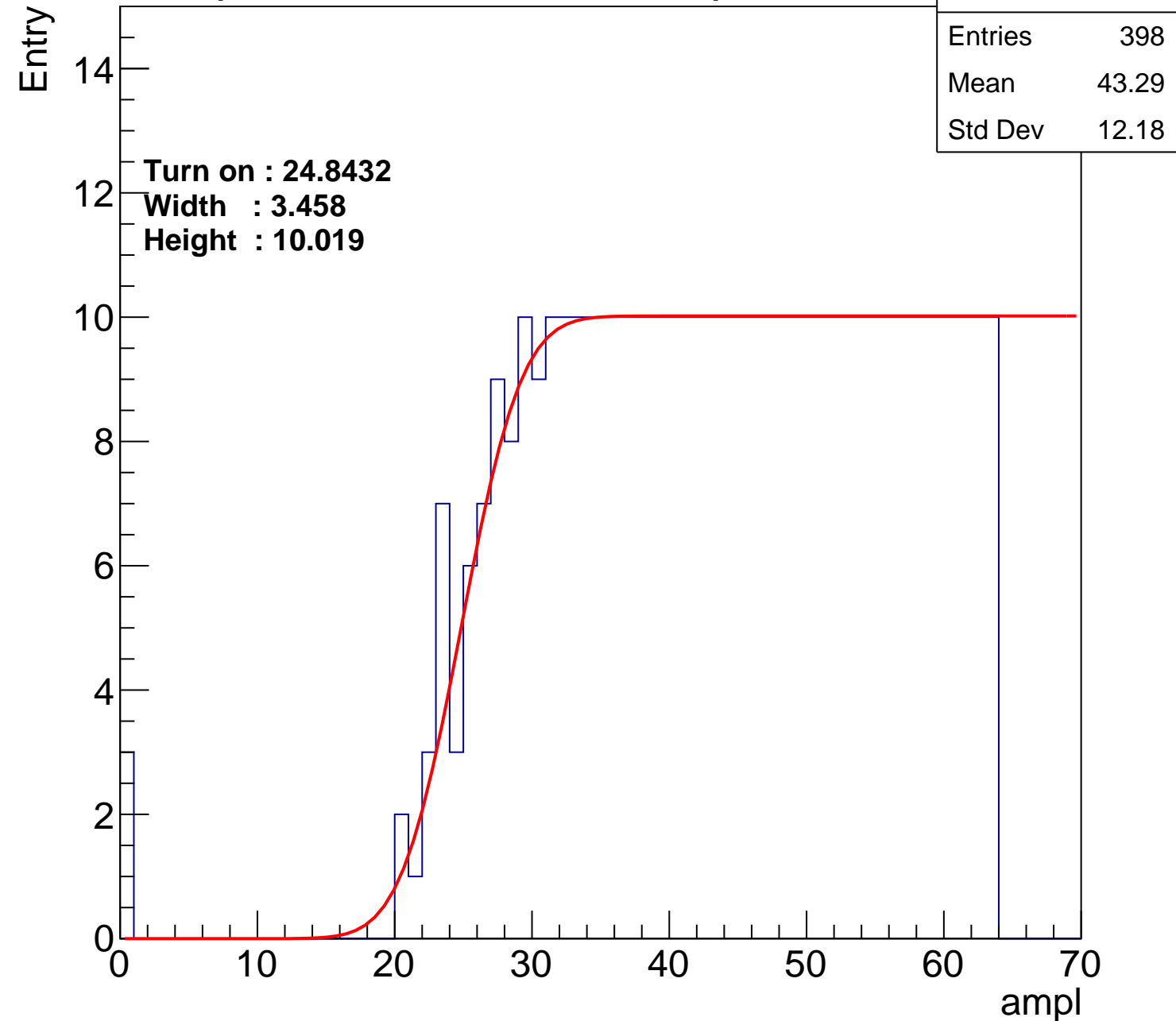
Width : 3.458

Height : 10.019

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch102

calib_packv5_042523_0143.root, FC#11, port A2

Entries	369
Mean	44.72
Std Dev	11.46

Turn on : 26.9926

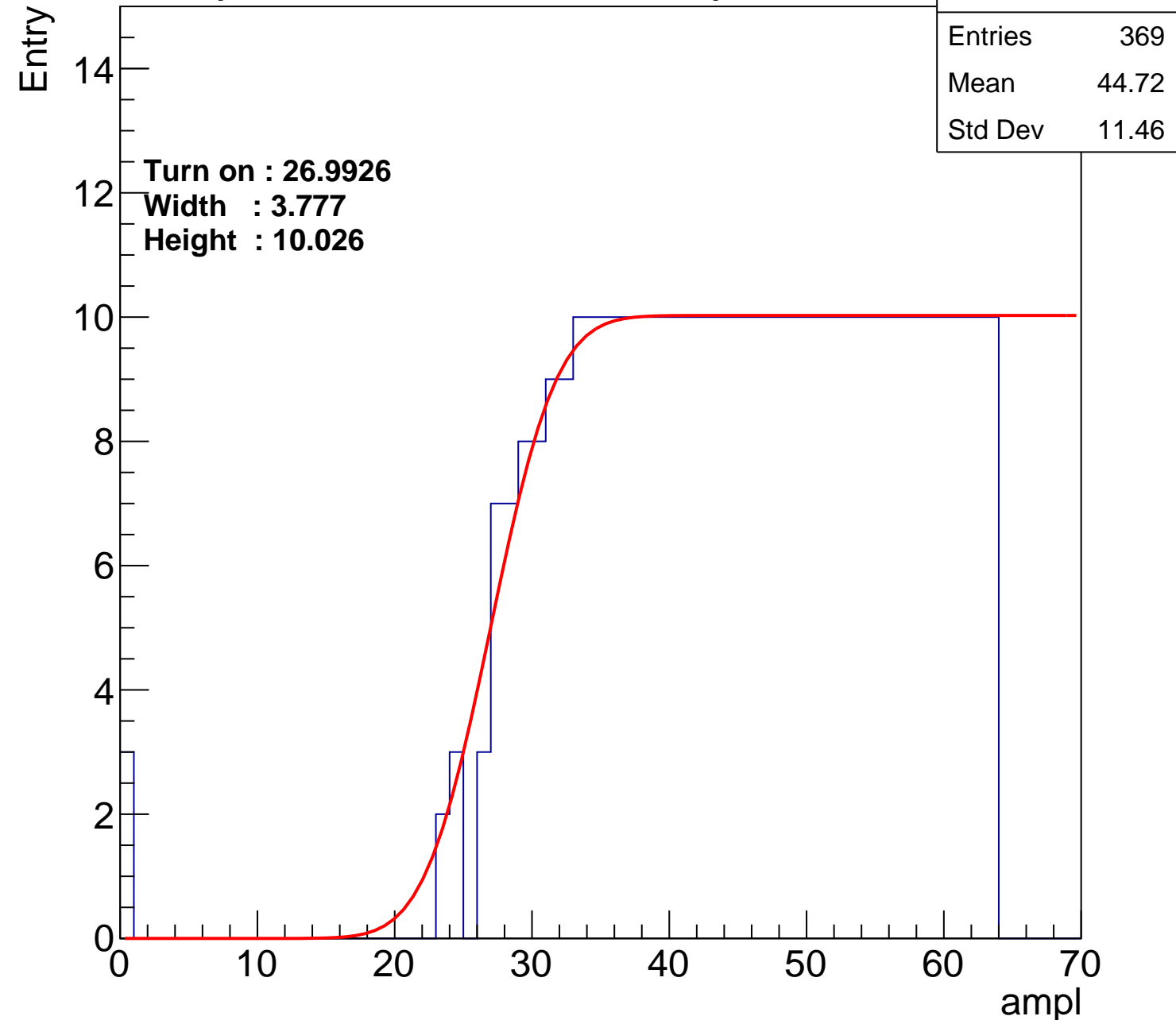
Width : 3.777

Height : 10.026

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch103

calib_packv5_042523_0143.root, FC#11, port A2

Entries	396
Mean	43.33
Std Dev	12.26

Turn on : 25.0594

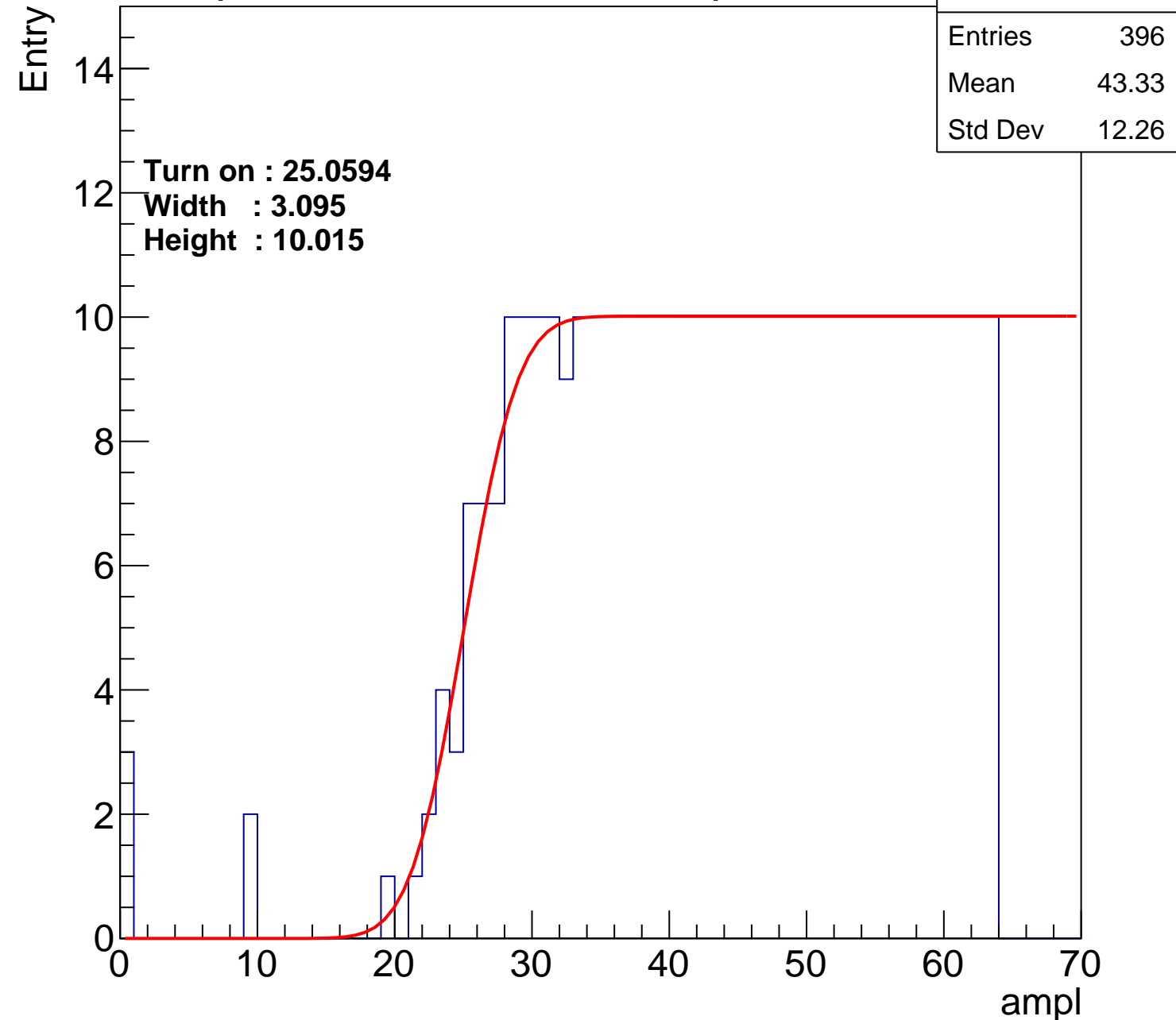
Width : 3.095

Height : 10.015

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch104

calib_packv5_042523_0143.root, FC#11, port A2

Entries	399
Mean	43.13
Std Dev	12.45

Turn on : 24.8388

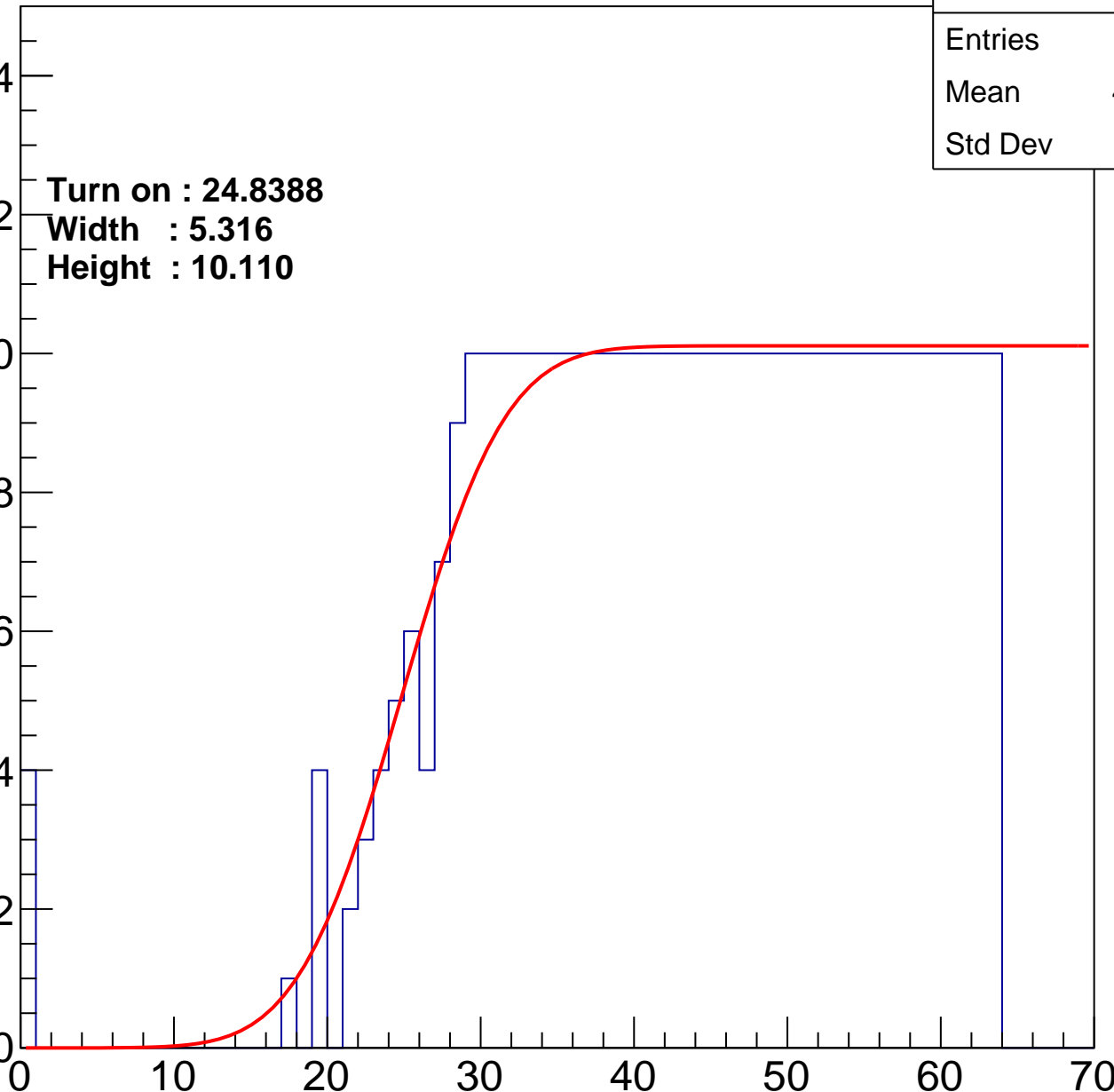
Width : 5.316

Height : 10.110

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch105

calib_packv5_042523_0143.root, FC#11, port A2

Entries	390
Mean	43.71
Std Dev	11.94

Turn on : 25.6407

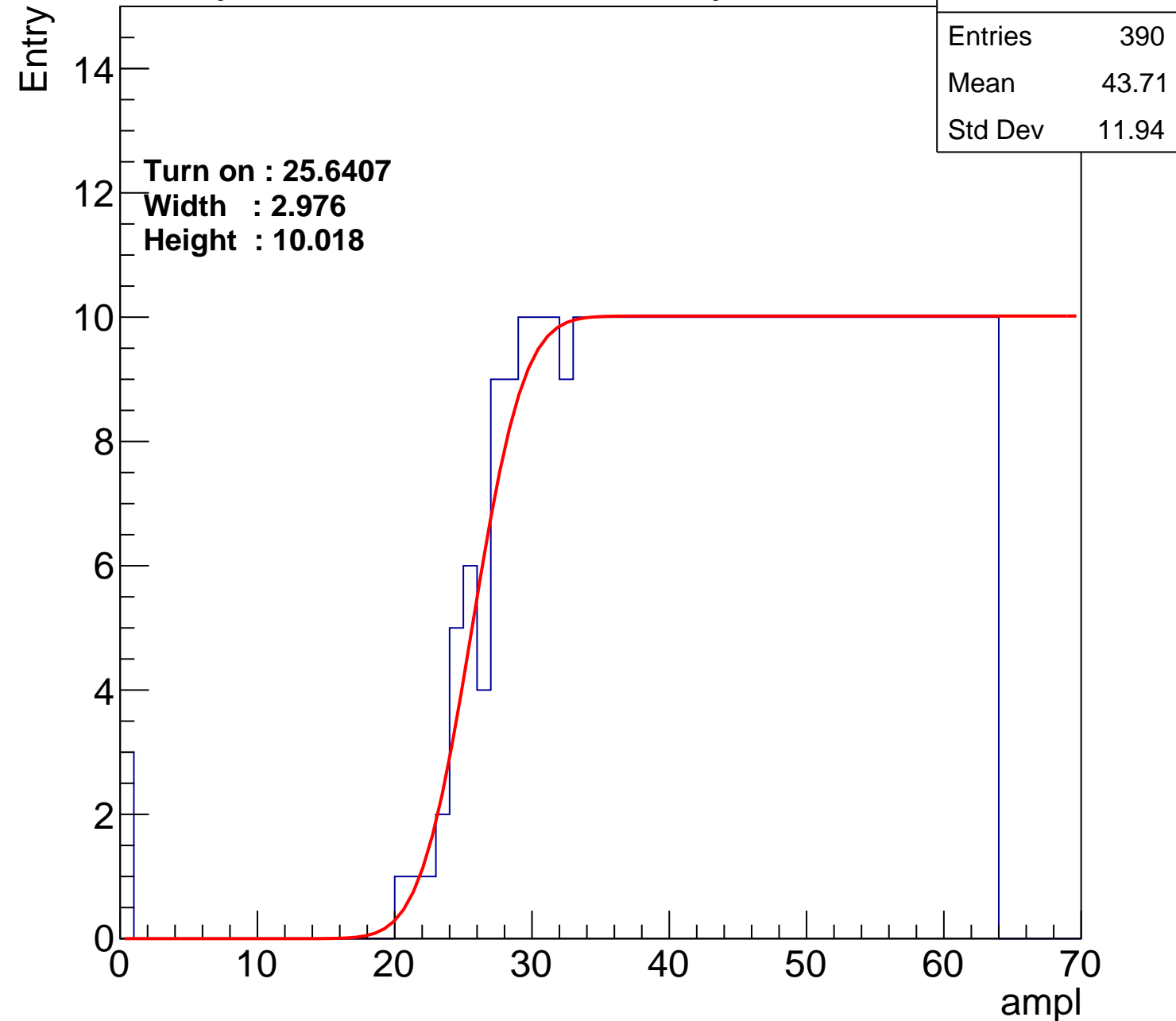
Width : 2.976

Height : 10.018

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch106

calib_packv5_042523_0143.root, FC#11, port A2

Entries	396
Mean	43.3
Std Dev	12.31

Turn on : 24.3957

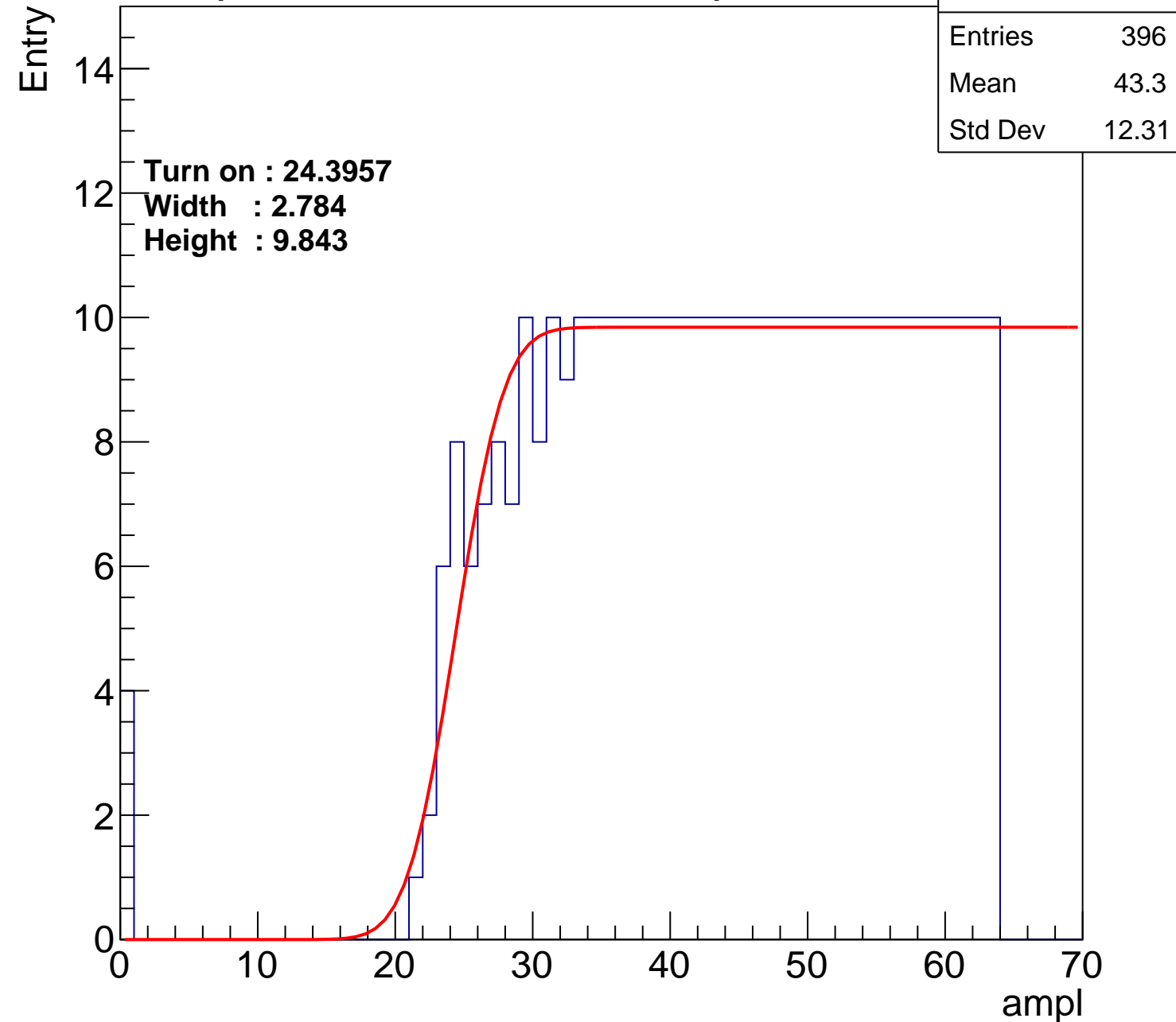
Width : 2.784

Height : 9.843

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch107

calib_packv5_042523_0143.root, FC#11, port A2

Entries	385
Mean	43.81
Std Dev	12.09

Turn on : 25.2950

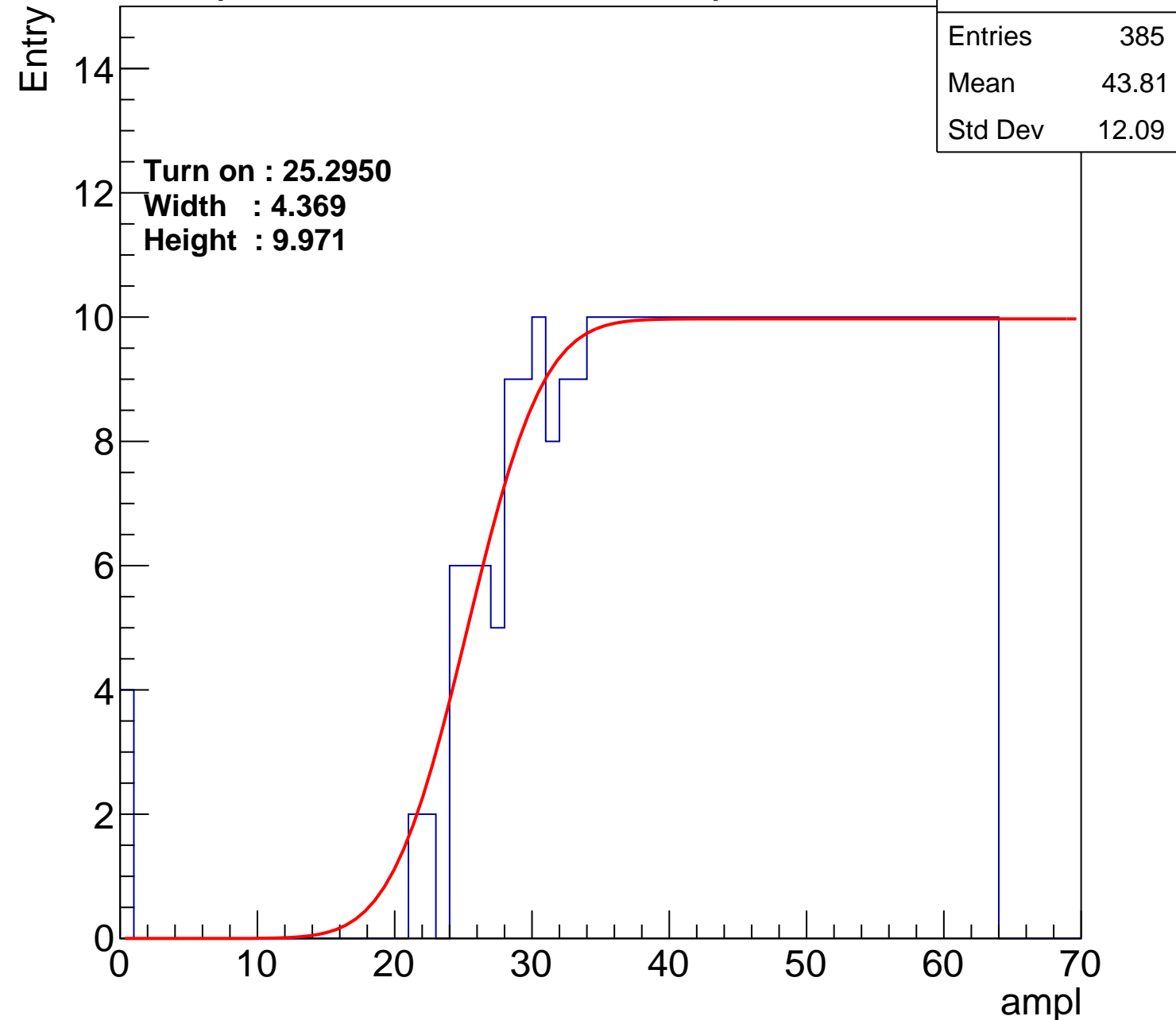
Width : 4.369

Height : 9.971

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch108

calib_packv5_042523_0143.root, FC#11, port A2

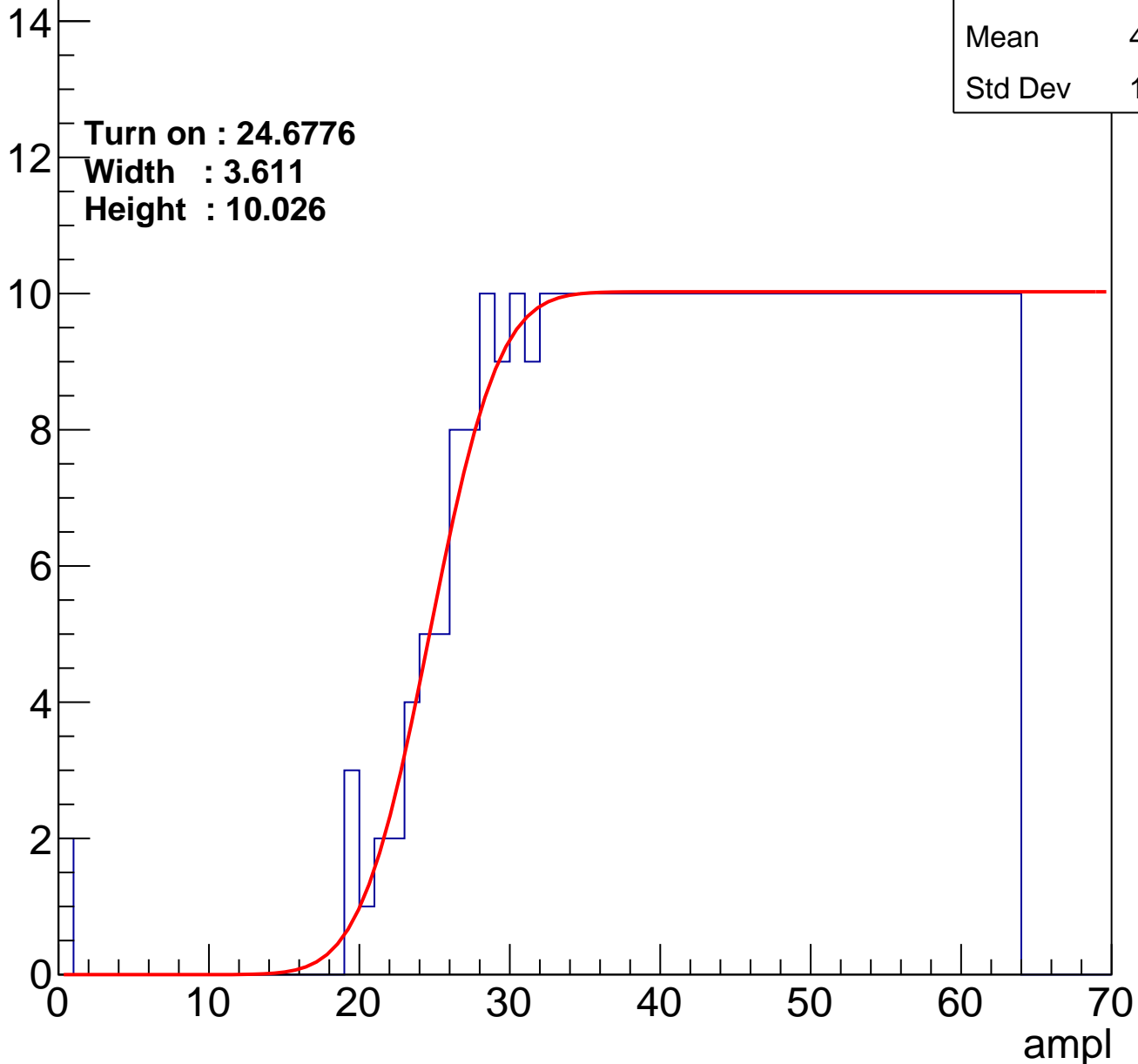
Entries	398
Mean	43.33
Std Dev	12.06

Turn on : 24.6776

Width : 3.611

Height : 10.026

Entry



B1L102S, U7-ch109

calib_packv5_042523_0143.root, FC#11, port A2

Entries	405
Mean	42.94
Std Dev	12.36

Turn on : 23.8837

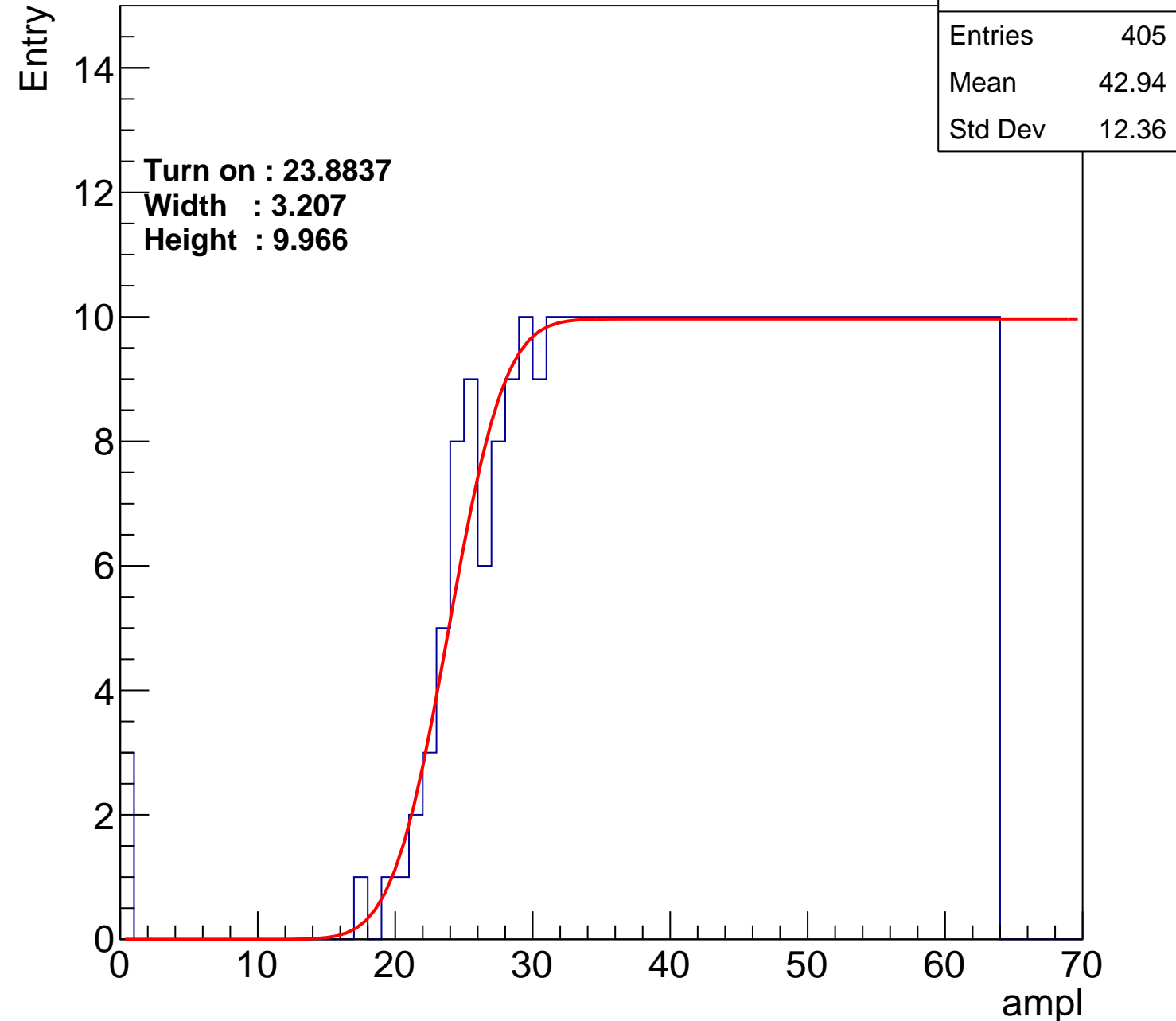
Width : 3.207

Height : 9.966

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch110

calib_packv5_042523_0143.root, FC#11, port A2

Entries	399
Mean	43.28
Std Dev	12.14

Turn on : 25.3443

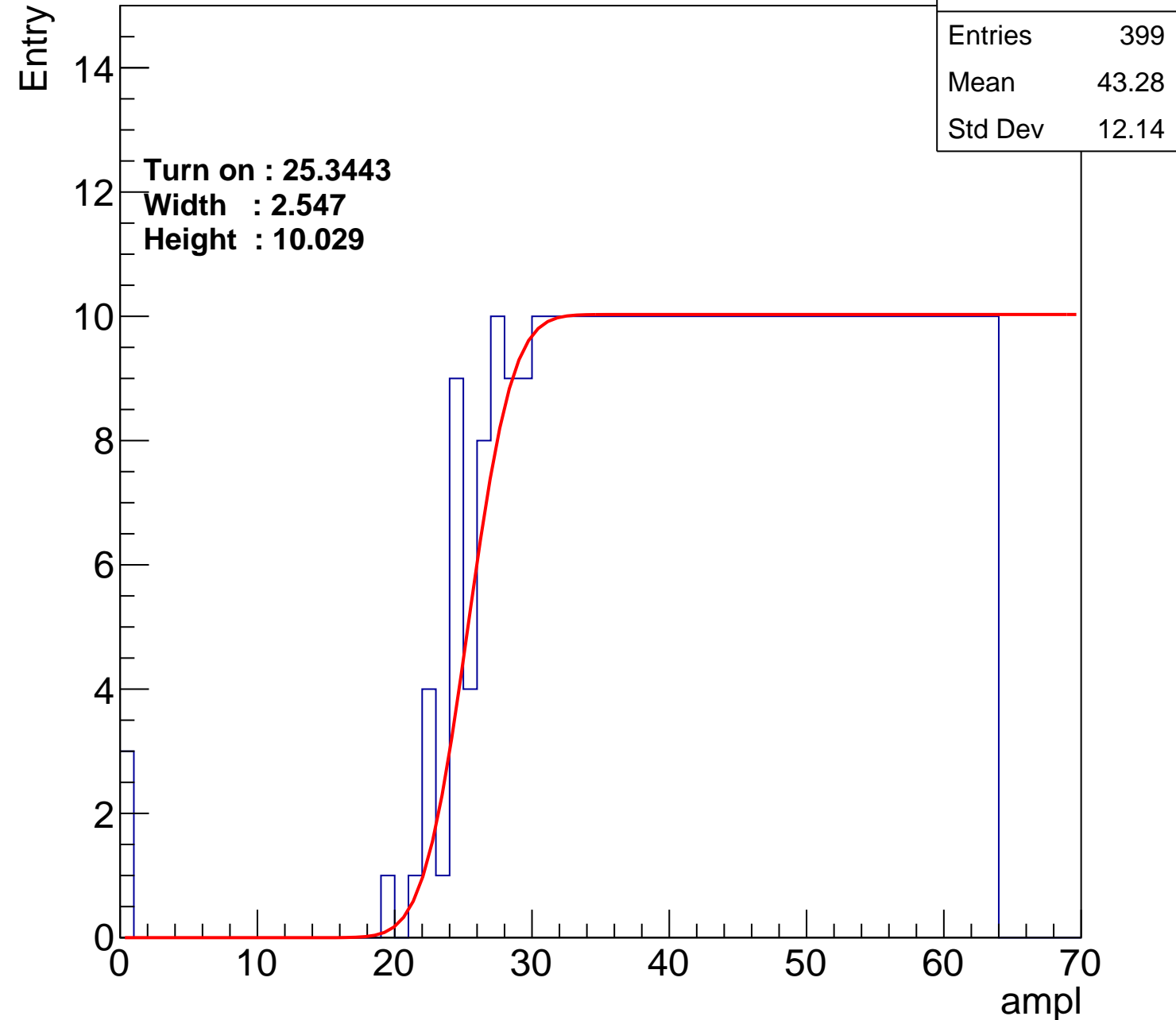
Width : 2.547

Height : 10.029

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch111

calib_packv5_042523_0143.root, FC#11, port A2

Entries	383
Mean	43.92
Std Dev	12.11

Turn on : 26.3628

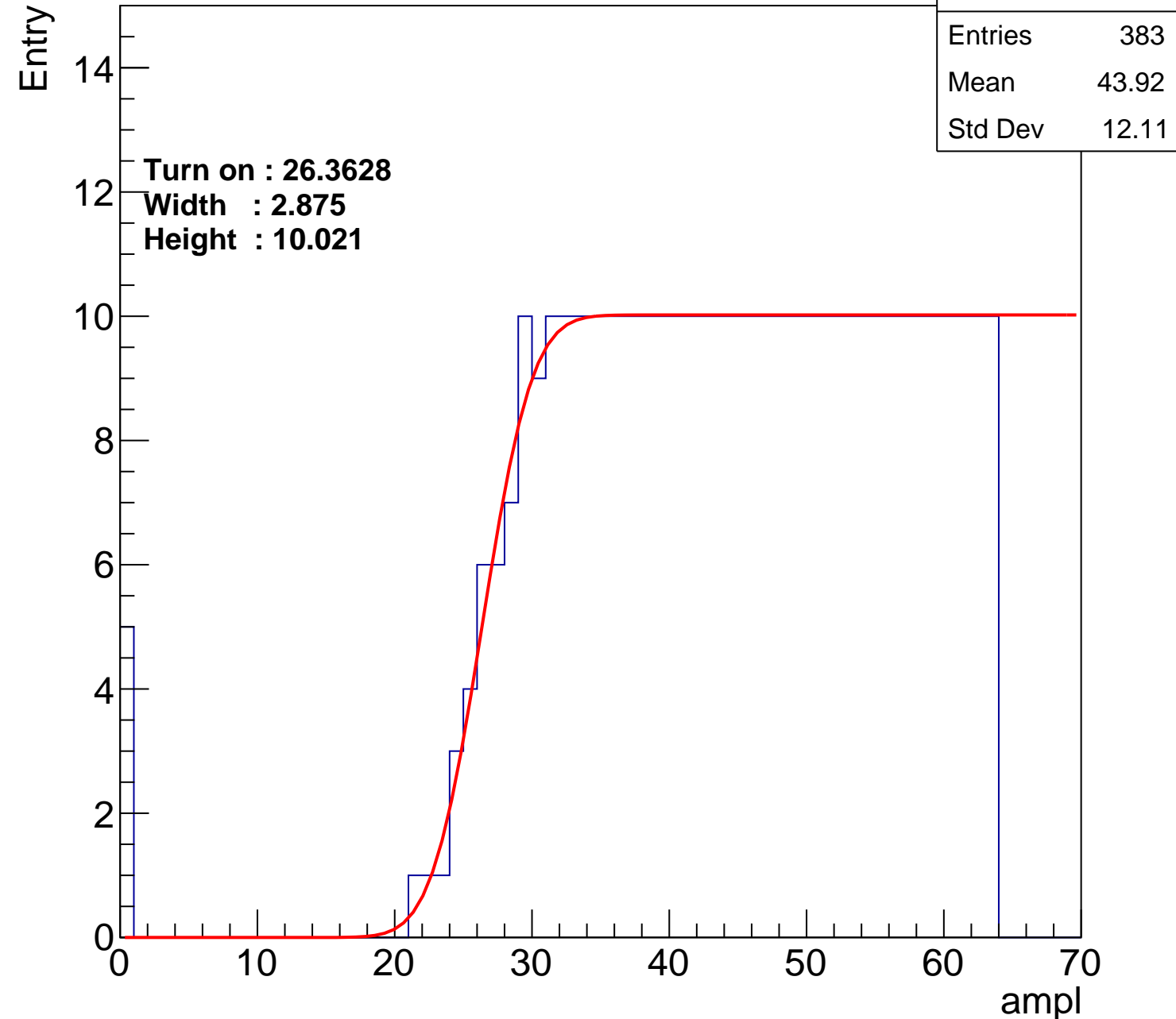
Width : 2.875

Height : 10.021

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch112

calib_packv5_042523_0143.root, FC#11, port A2

Entries	388
Mean	43.79
Std Dev	11.91

Turn on : 25.4478

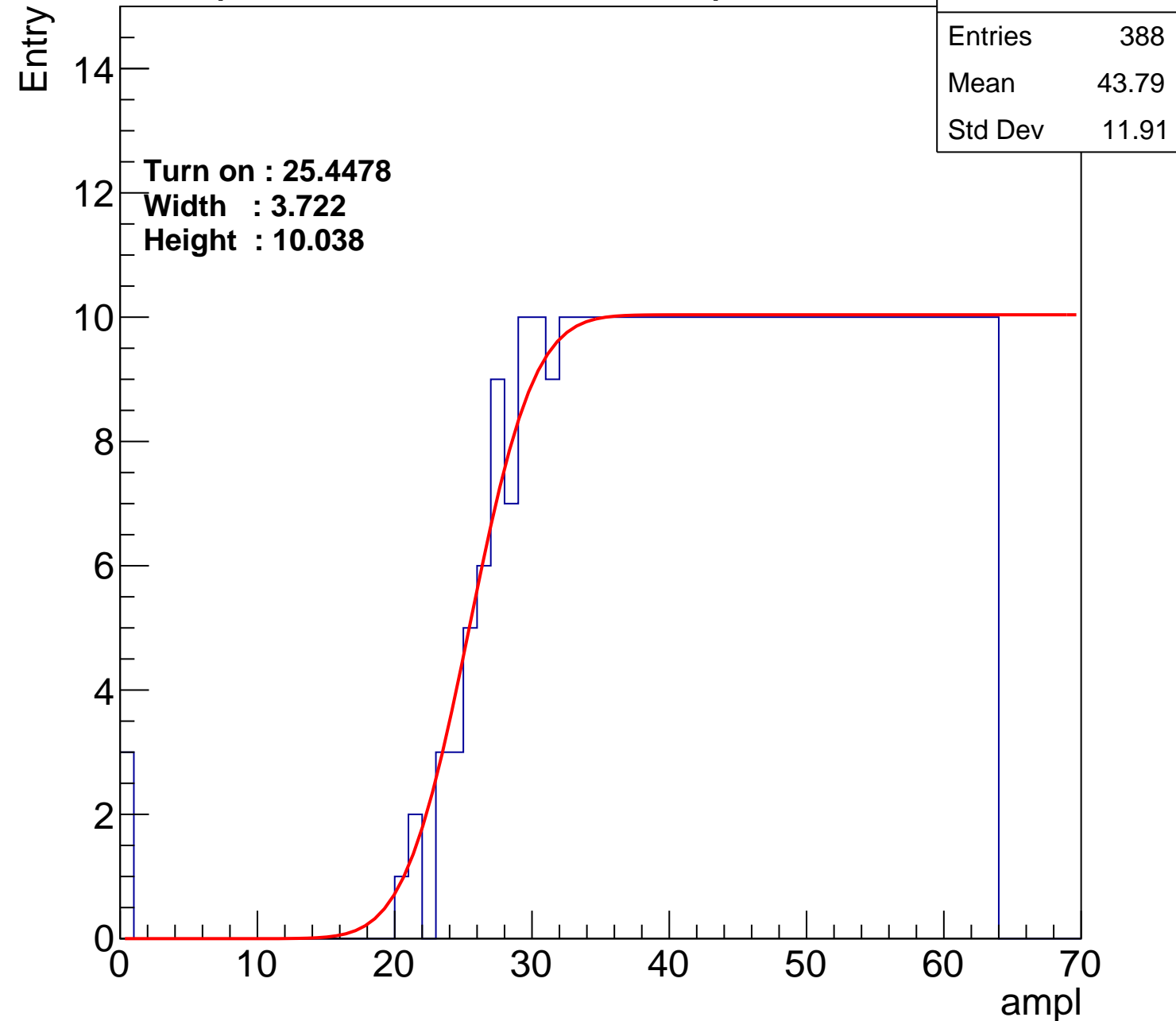
Width : 3.722

Height : 10.038

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch113

calib_packv5_042523_0143.root, FC#11, port A2

Entries	380
Mean	44.33
Std Dev	11.33

Turn on : 25.7996

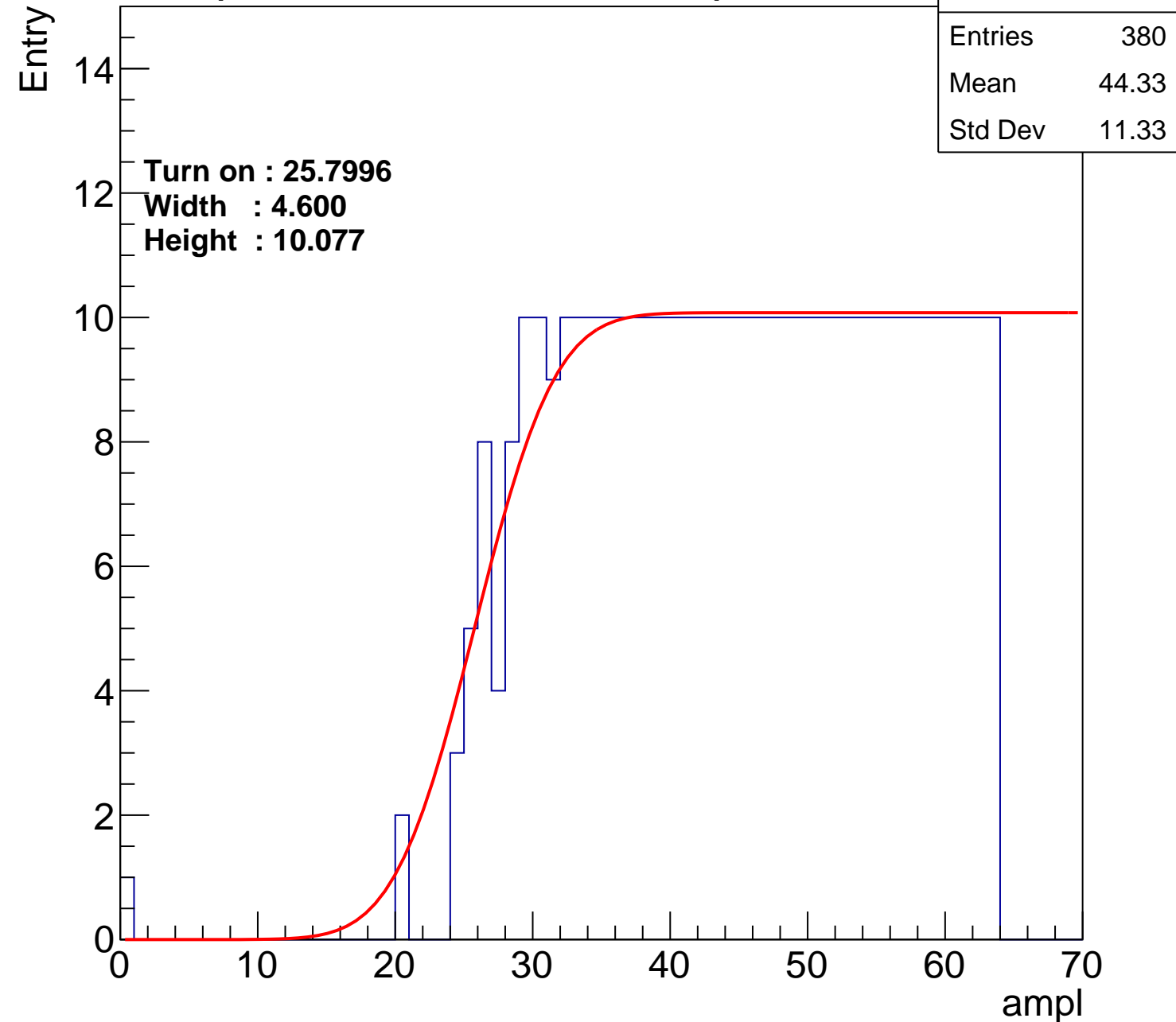
Width : 4.600

Height : 10.077

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch114

calib_packv5_042523_0143.root, FC#11, port A2

Entries	395
Mean	43.5
Std Dev	11.94

Turn on : 25.4703

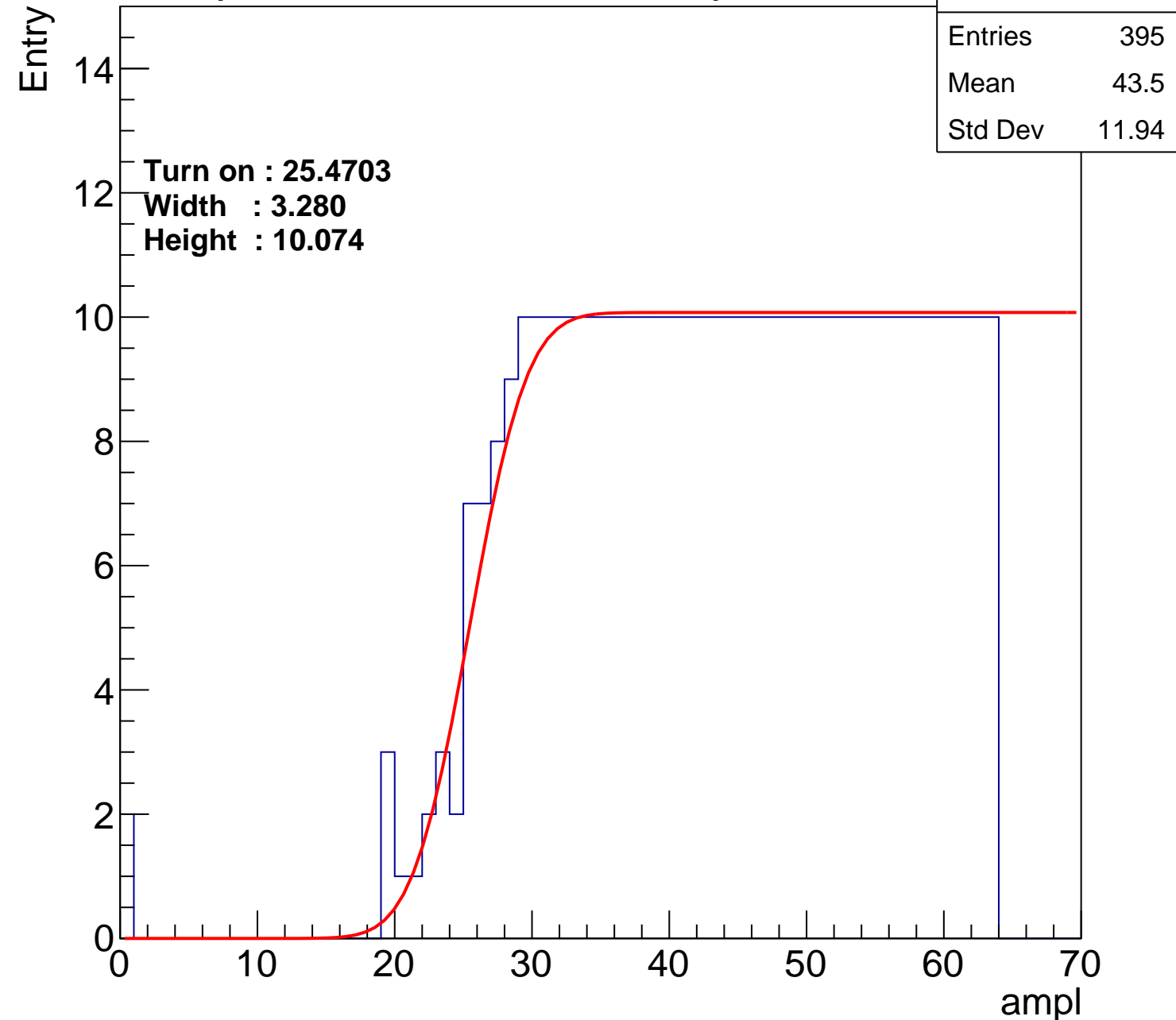
Width : 3.280

Height : 10.074

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch115

calib_packv5_042523_0143.root, FC#11, port A2

Entries	380
Mean	44.33
Std Dev	11.32

Turn on : 26.3745

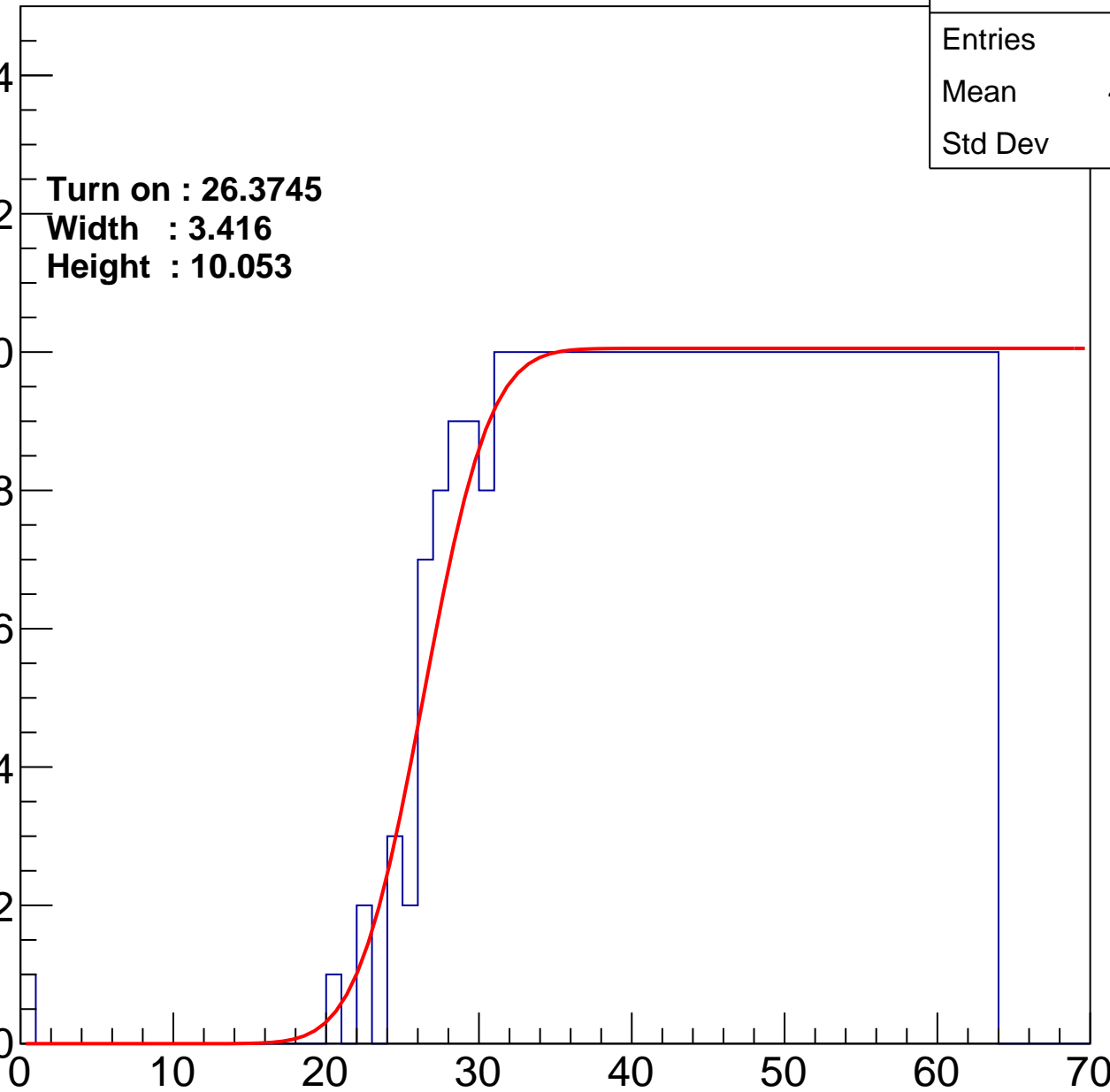
Width : 3.416

Height : 10.053

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch116

calib_packv5_042523_0143.root, FC#11, port A2

Entries	401
Mean	43.29
Std Dev	11.9

Turn on : 24.3365

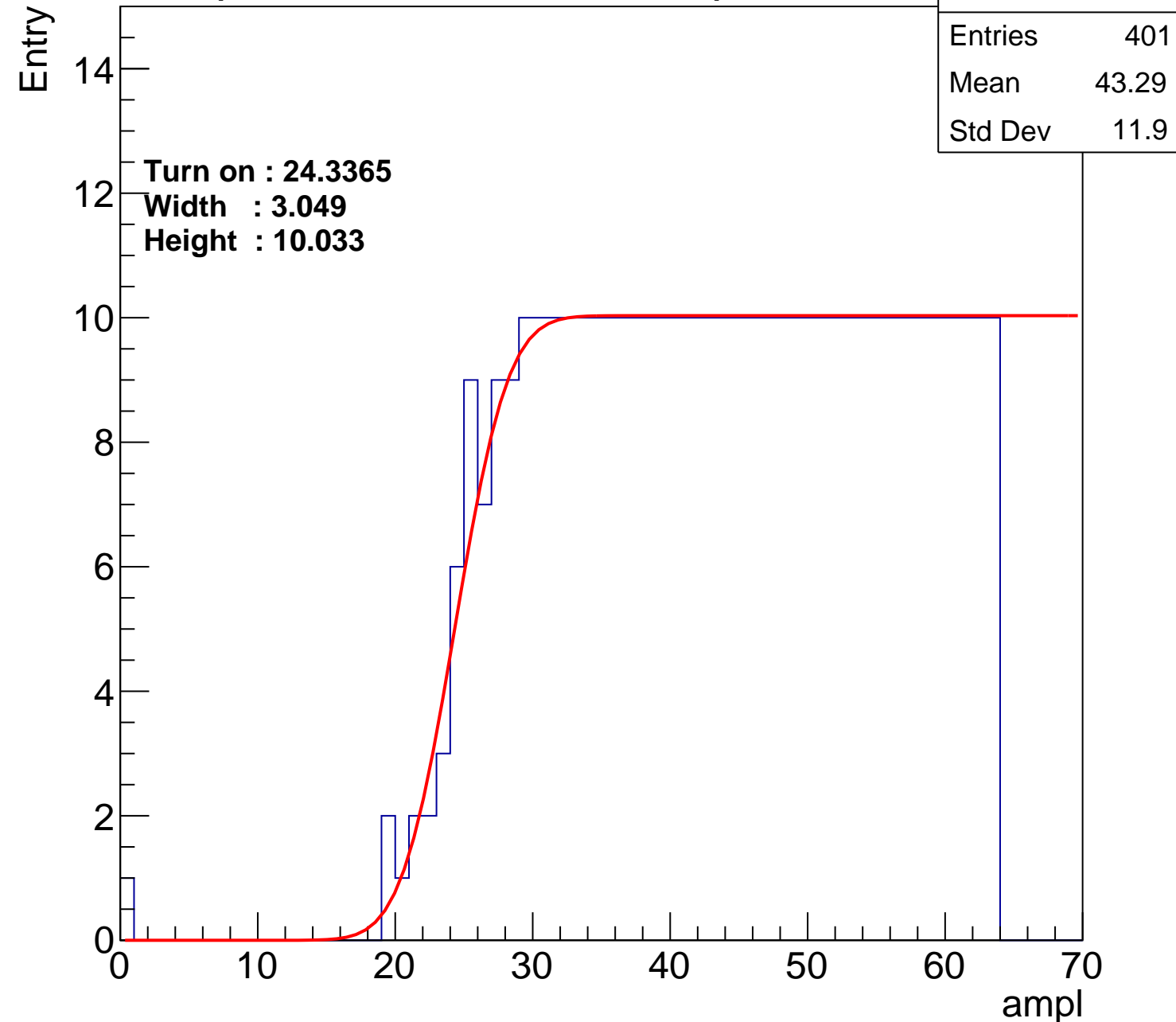
Width : 3.049

Height : 10.033

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch117

calib_packv5_042523_0143.root, FC#11, port A2

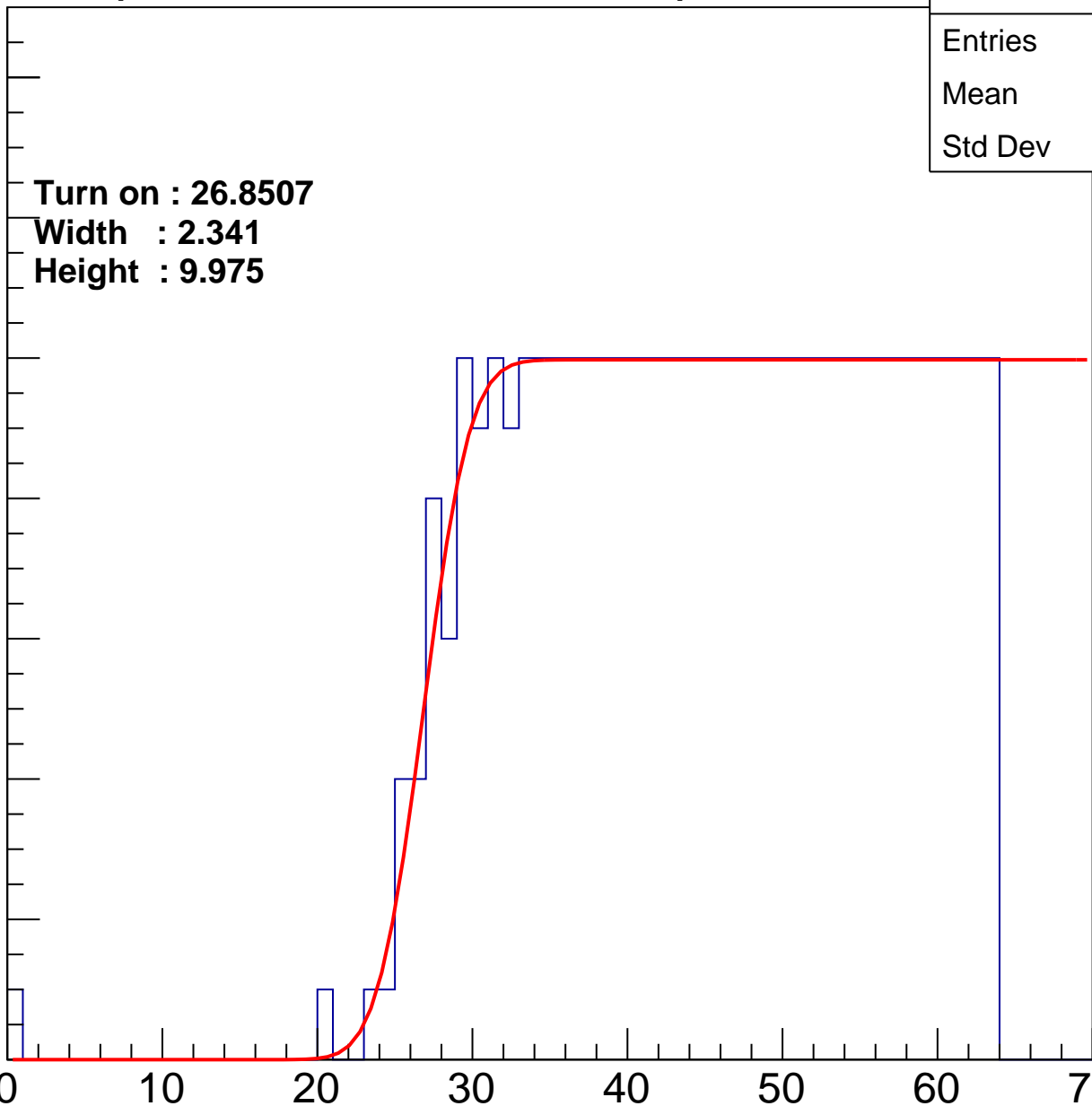
Entry

14
12
10
8
6
4
2
0

Turn on : 26.8507
Width : 2.341
Height : 9.975

Entries	374
Mean	44.63
Std Dev	11.16

ampl



B1L102S, U7-ch118

calib_packv5_042523_0143.root, FC#11, port A2

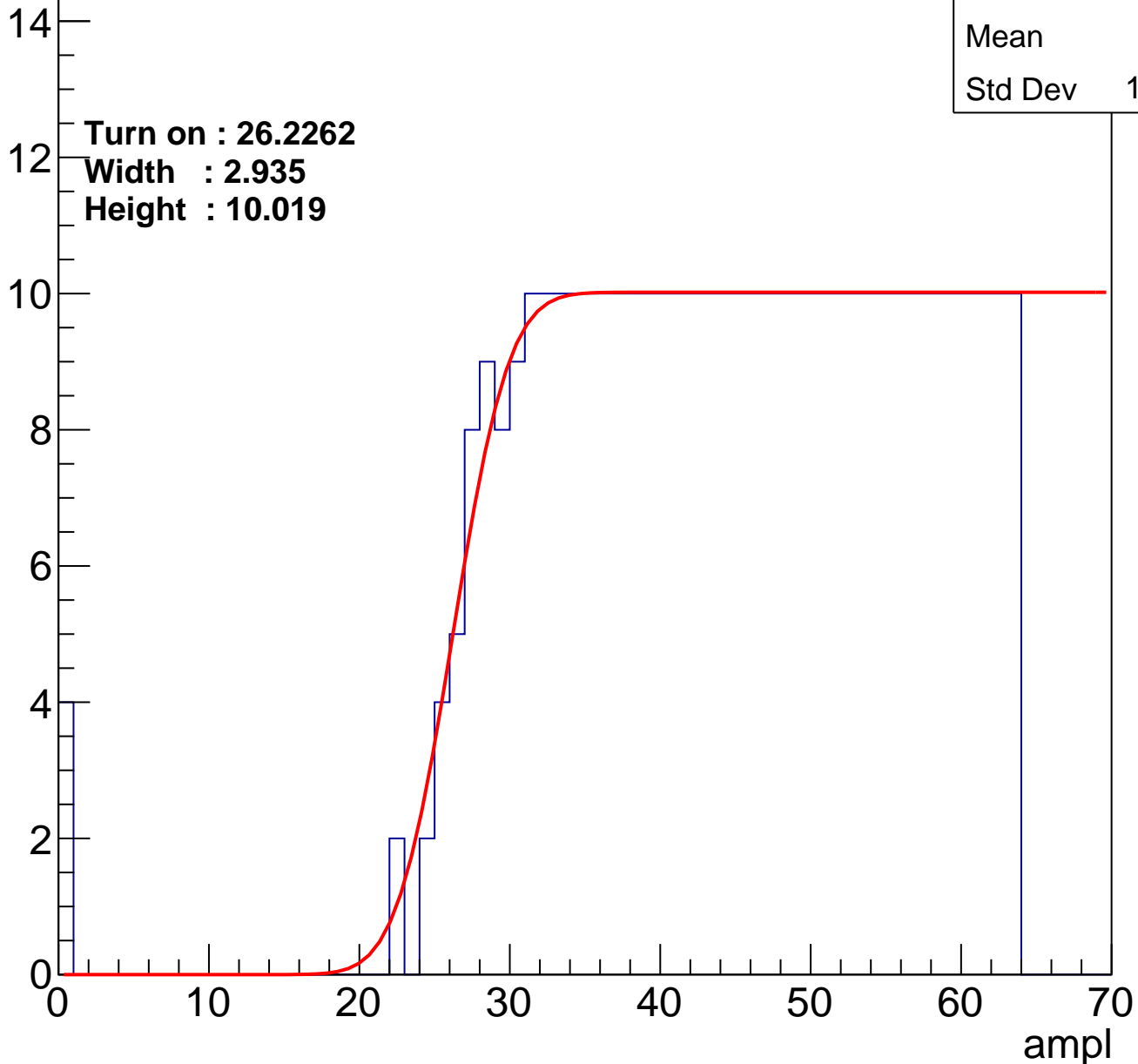
Entries	381
Mean	44.1
Std Dev	11.87

Turn on : 26.2262

Width : 2.935

Height : 10.019

Entry



B1L102S, U7-ch119

calib_packv5_042523_0143.root, FC#11, port A2

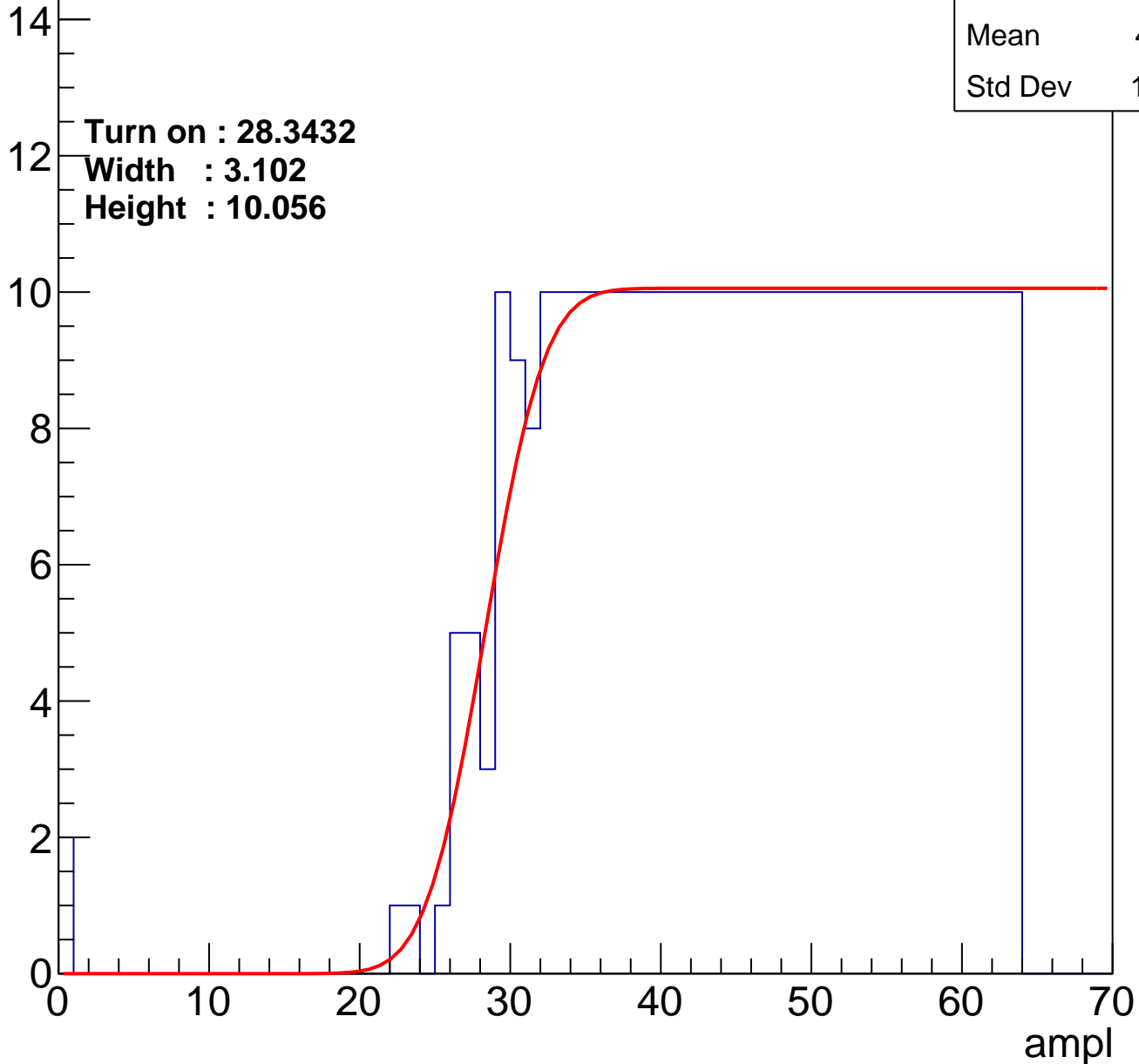
Entries	365
Mean	45.01
Std Dev	11.13

Turn on : 28.3432

Width : 3.102

Height : 10.056

Entry



B1L102S, U7-ch120

calib_packv5_042523_0143.root, FC#11, port A2

Entries	392
Mean	43.62
Std Dev	11.98

Turn on : 25.4378

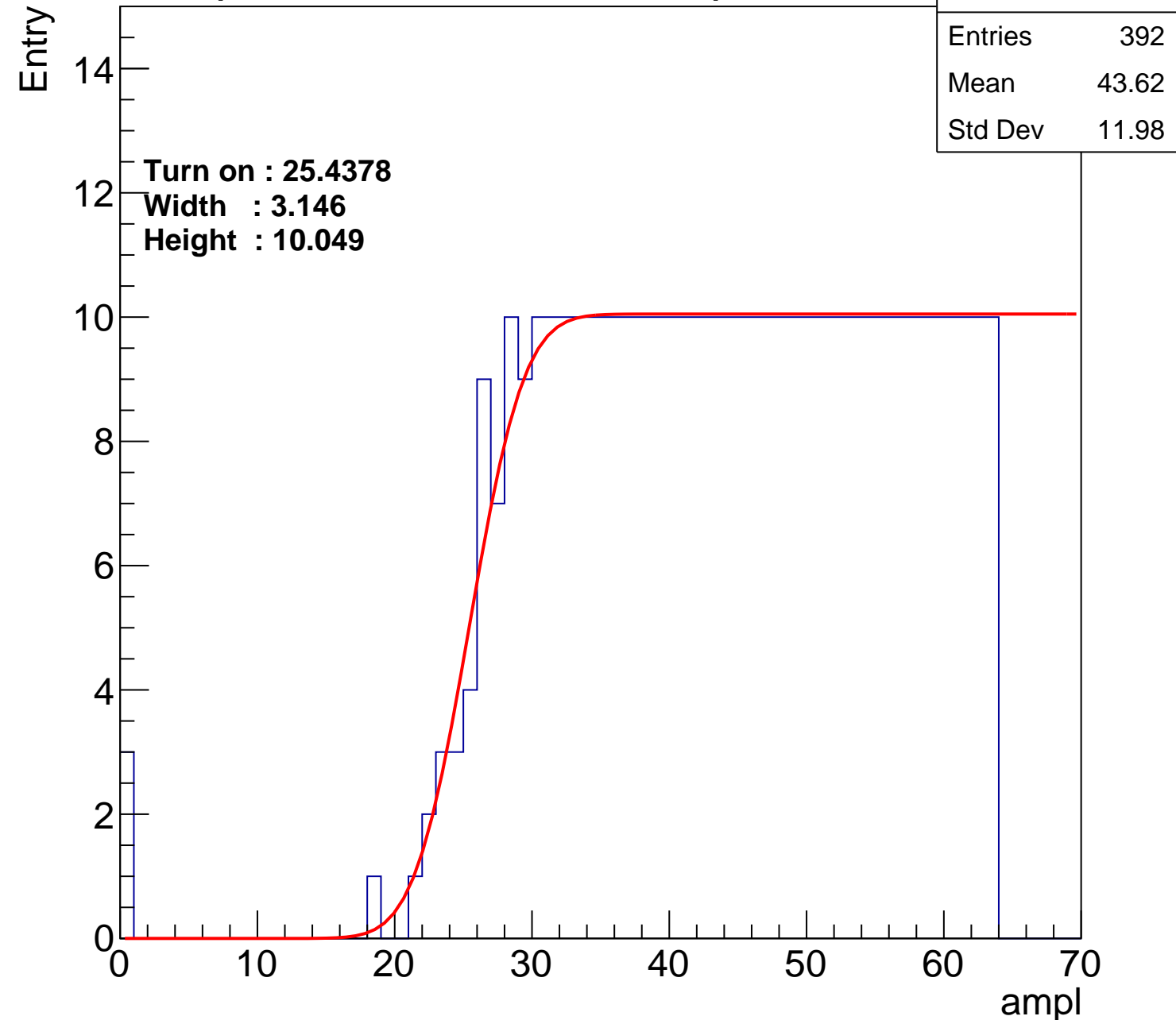
Width : 3.146

Height : 10.049

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch121

calib_packv5_042523_0143.root, FC#11, port A2

Entries	378
Mean	44.34
Std Dev	11.51

Turn on : 26.6268

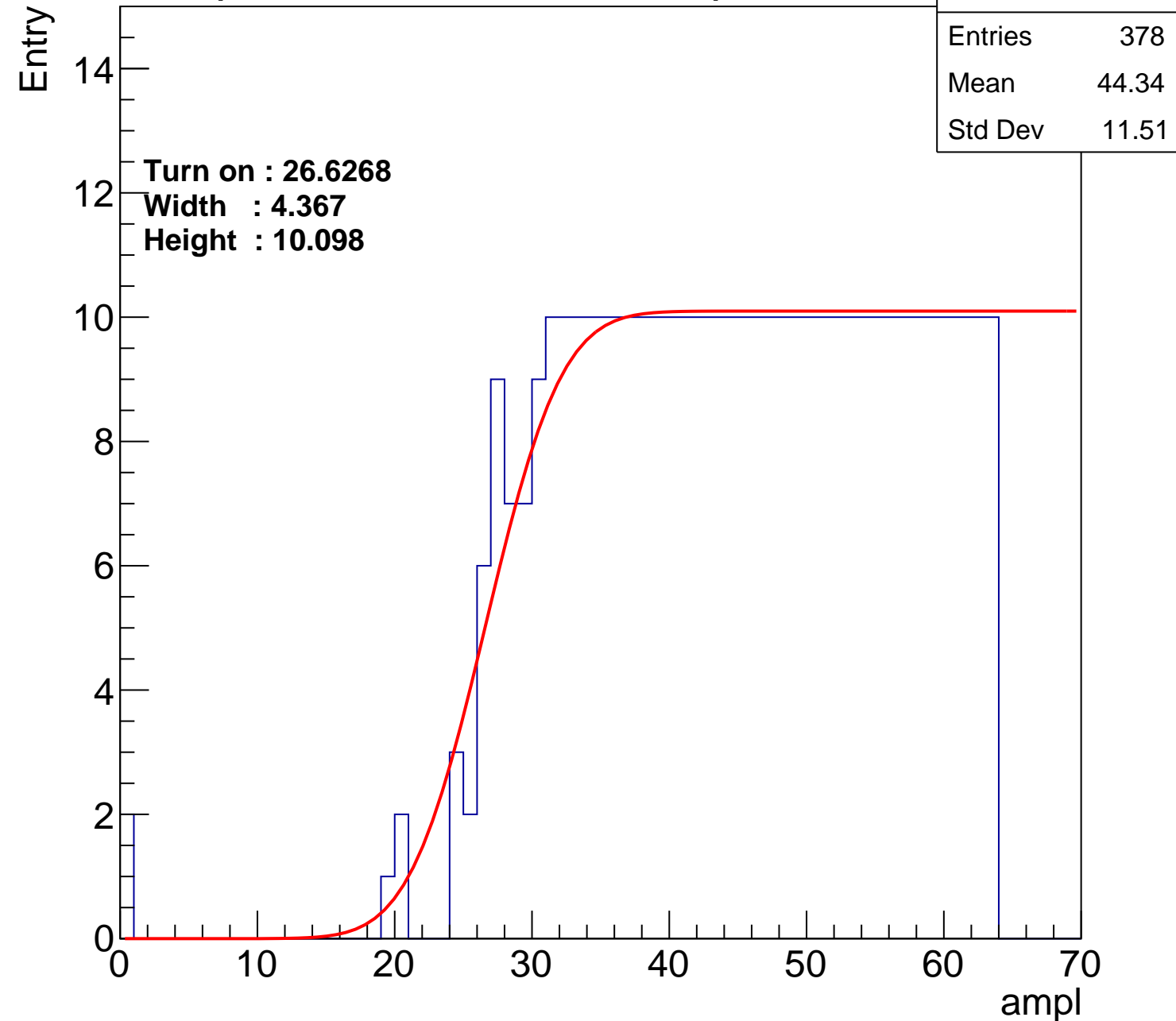
Width : 4.367

Height : 10.098

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch122

calib_packv5_042523_0143.root, FC#11, port A2

Entries	379
Mean	43.92
Std Dev	12.48

Turn on : 27.2425

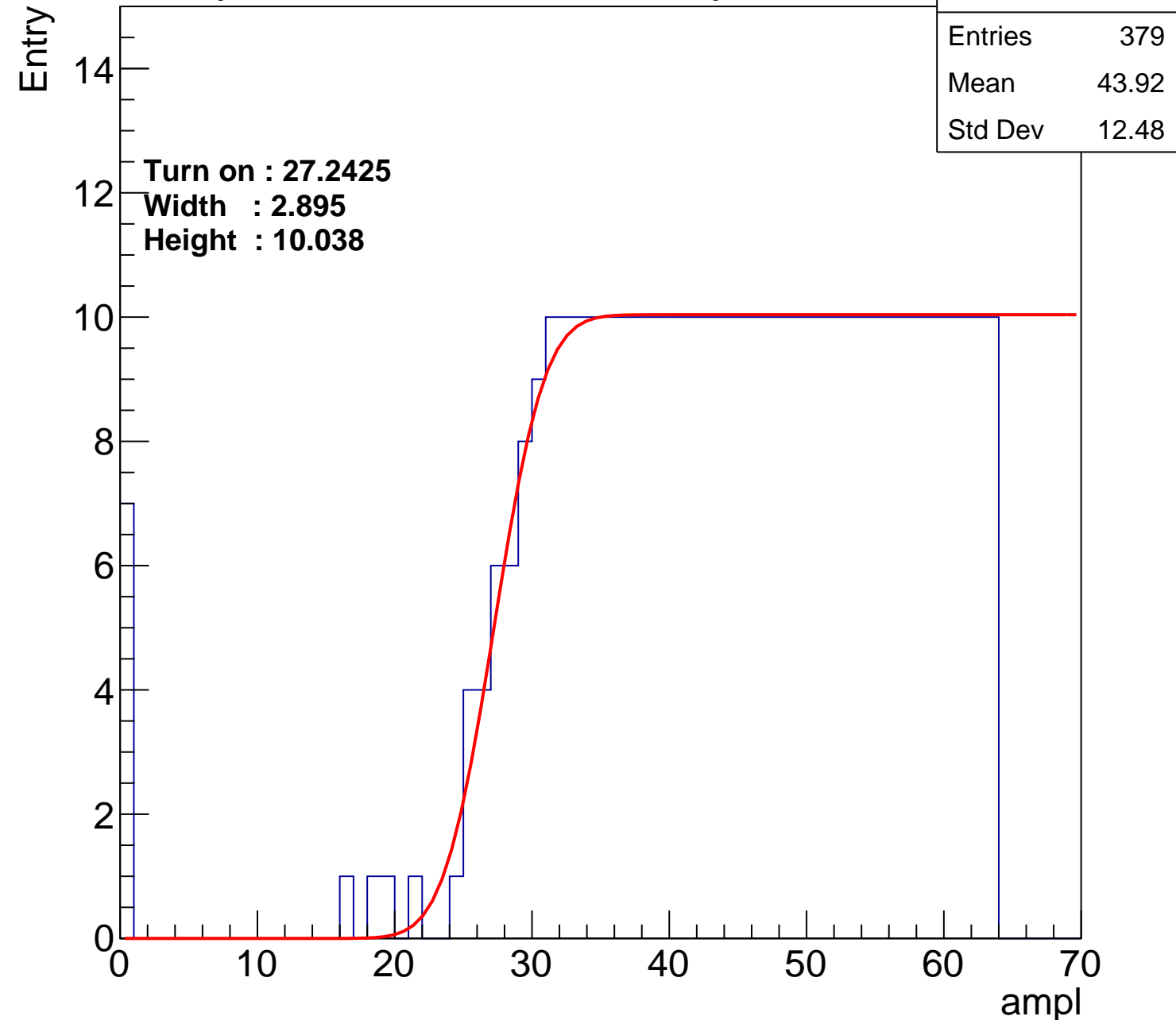
Width : 2.895

Height : 10.038

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch123

calib_packv5_042523_0143.root, FC#11, port A2

Entries	396
Mean	43.33
Std Dev	12.28

Turn on : 25.2807

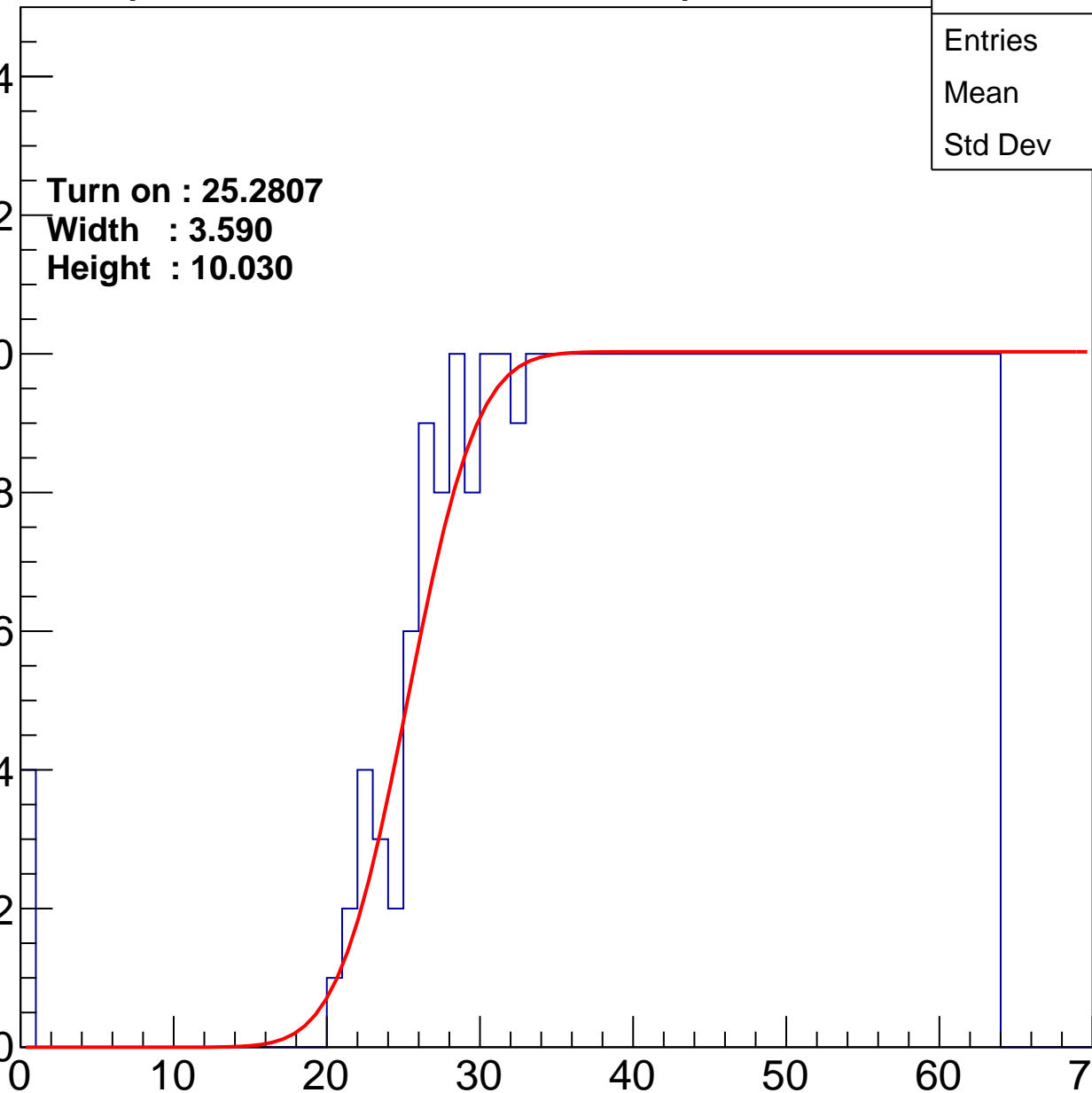
Width : 3.590

Height : 10.030

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch124

calib_packv5_042523_0143.root, FC#11, port A2

Entries	393
Mean	43.49
Std Dev	12.19

Turn on : 26.2392

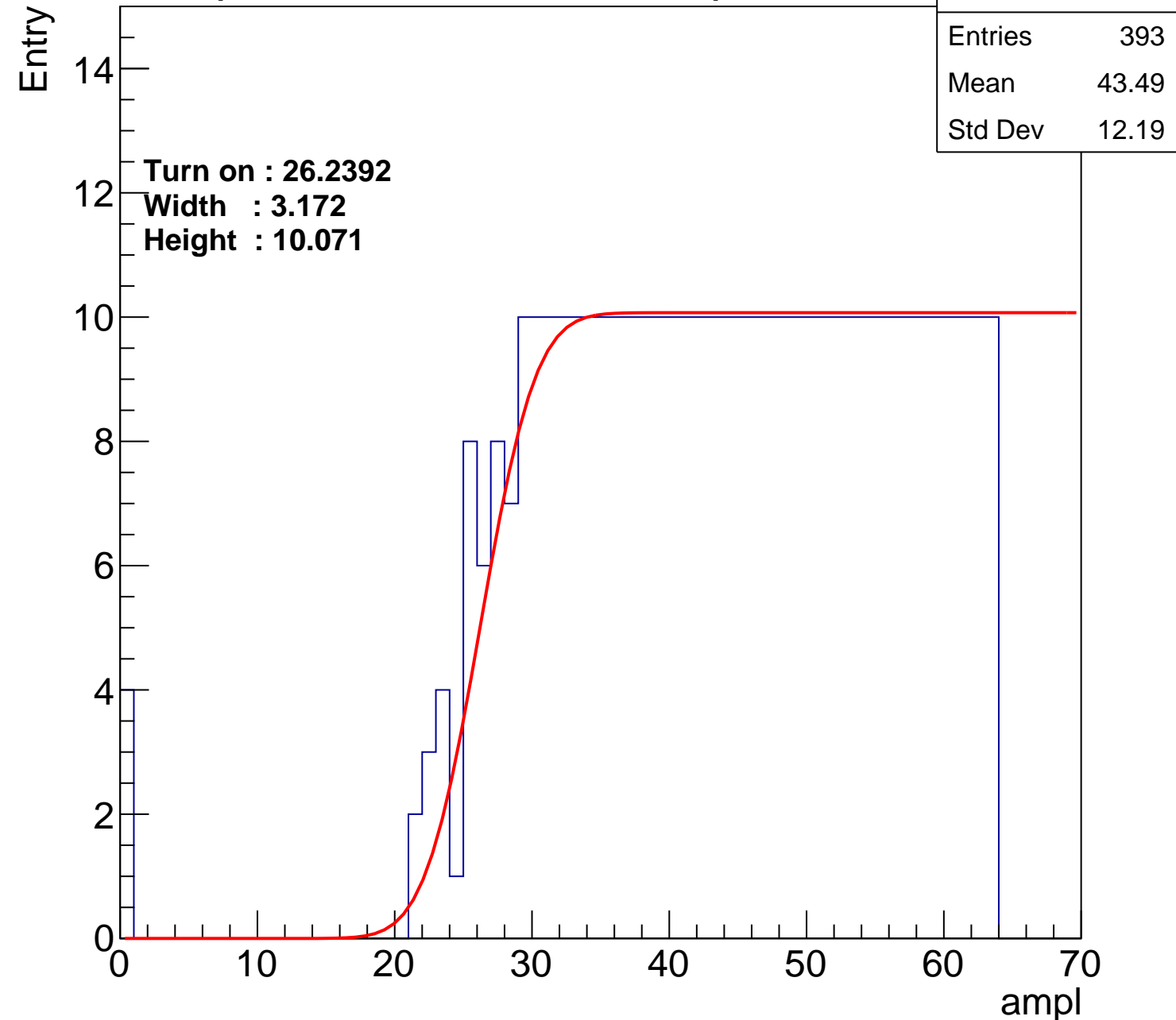
Width : 3.172

Height : 10.071

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch125

calib_packv5_042523_0143.root, FC#11, port A2

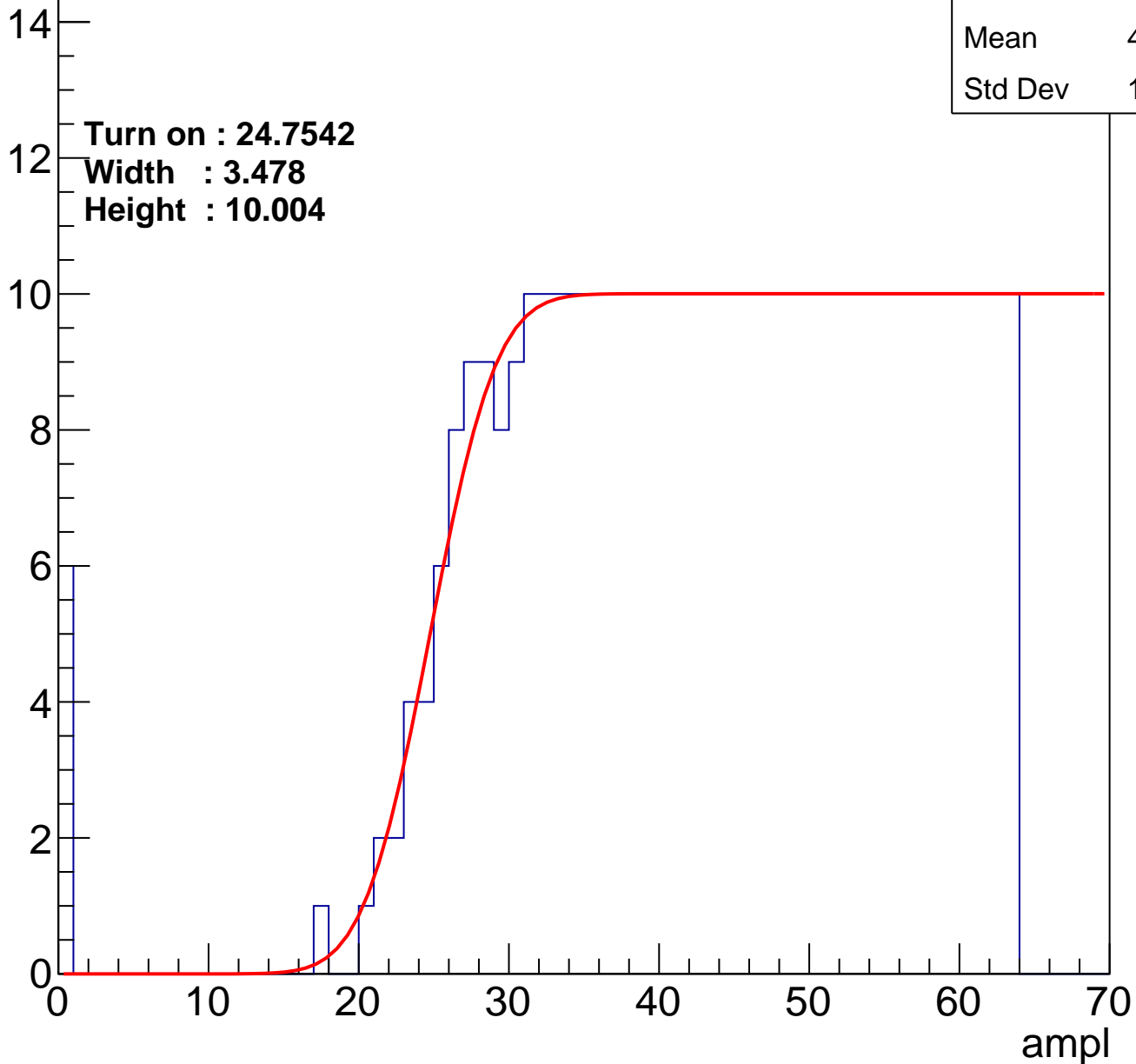
Entries	399
Mean	43.05
Std Dev	12.67

Turn on : 24.7542

Width : 3.478

Height : 10.004

Entry



B1L102S, U7-ch126

calib_packv5_042523_0143.root, FC#11, port A2

Entries	395
Mean	43.58
Std Dev	11.75

Turn on : 25.8254

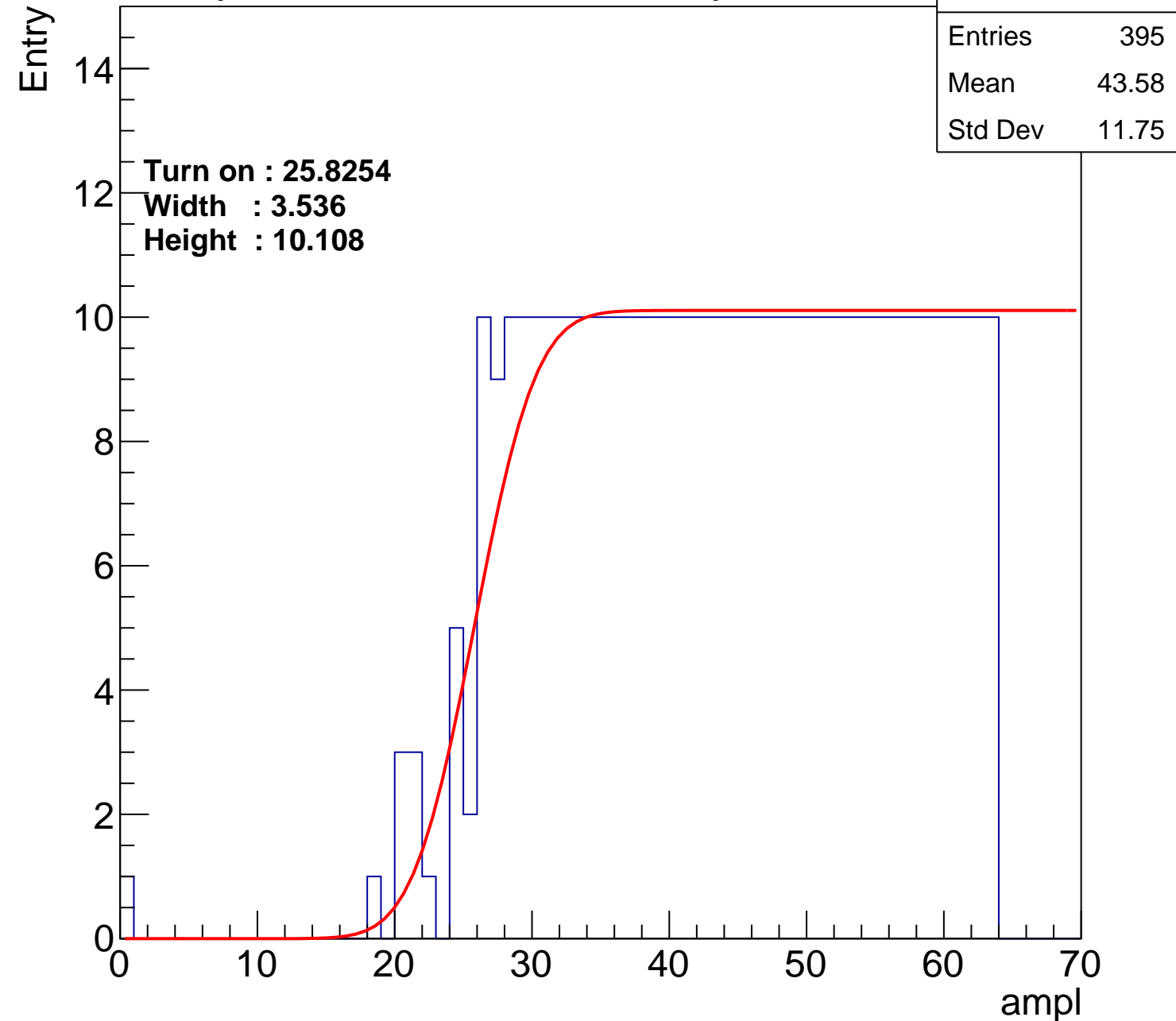
Width : 3.536

Height : 10.108

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch127

calib_packv5_042523_0143.root, FC#11, port A2

Entries	394
Mean	43.3
Std Dev	12.55

Turn on : 25.3027

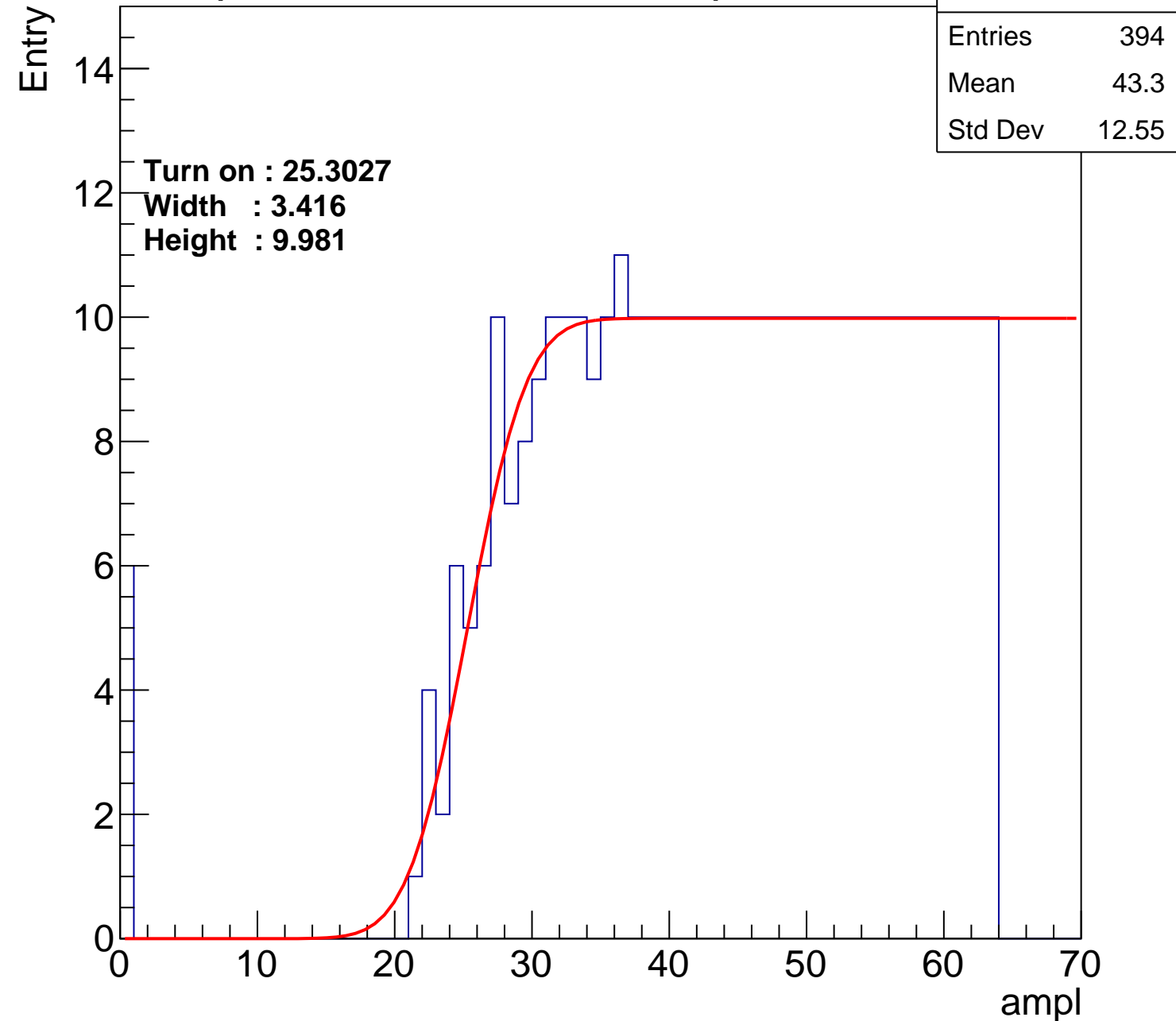
Width : 3.416

Height : 9.981

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U7-ch127

calib_packv5_042523_0143.root, FC#11, port A2

Entries	394
Mean	43.3
Std Dev	12.55

Turn on : 25.3027

Width : 3.416

Height : 9.981

Entry

14
12
10
8
6
4
2
0

ampl

