



# B1L003S, U3-ch0, adc0

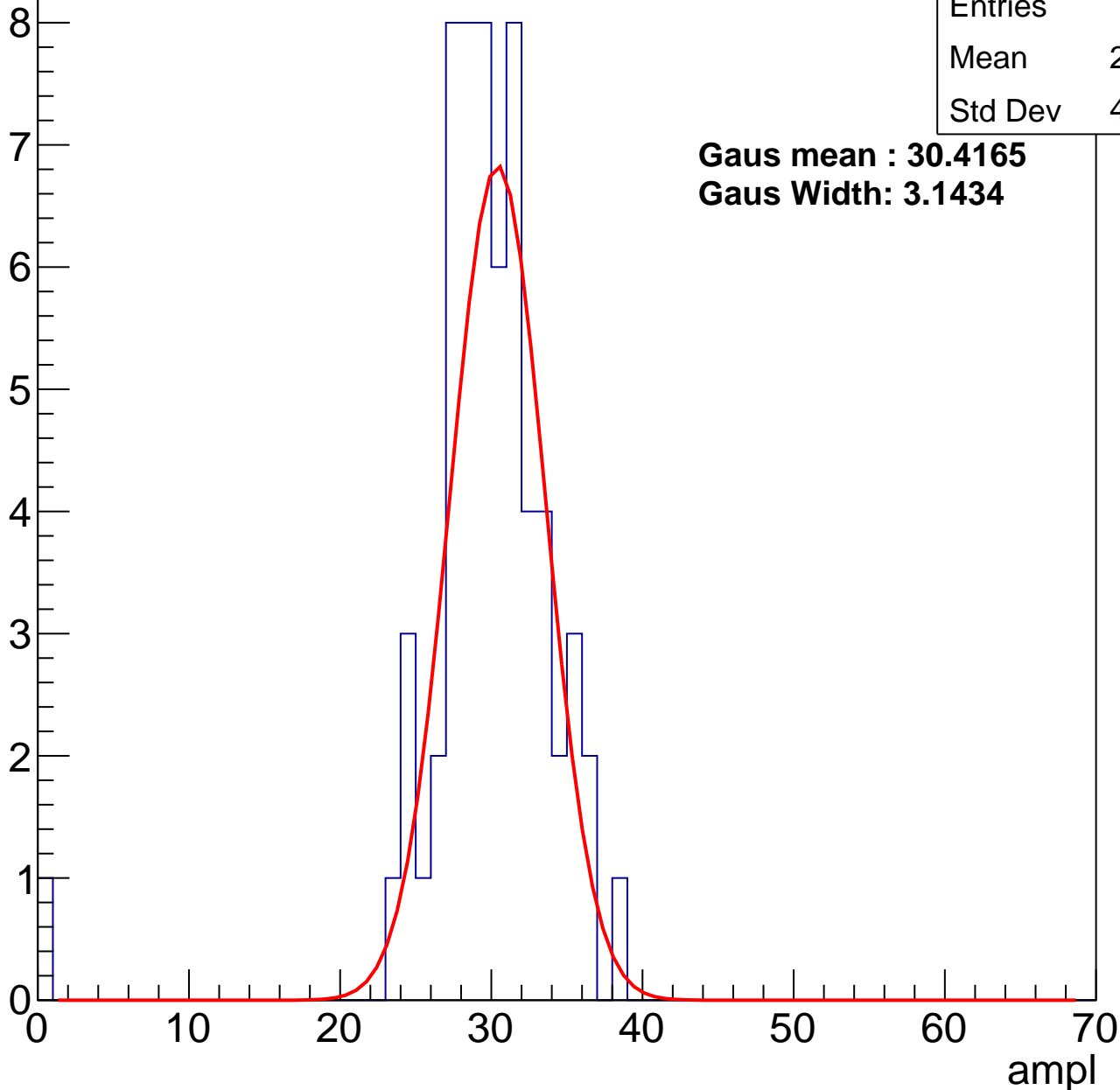
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	29.27
Std Dev	4.913

**Gaus mean : 30.4165**

**Gaus Width: 3.1434**



# B1L003S, U3-ch0, adc1

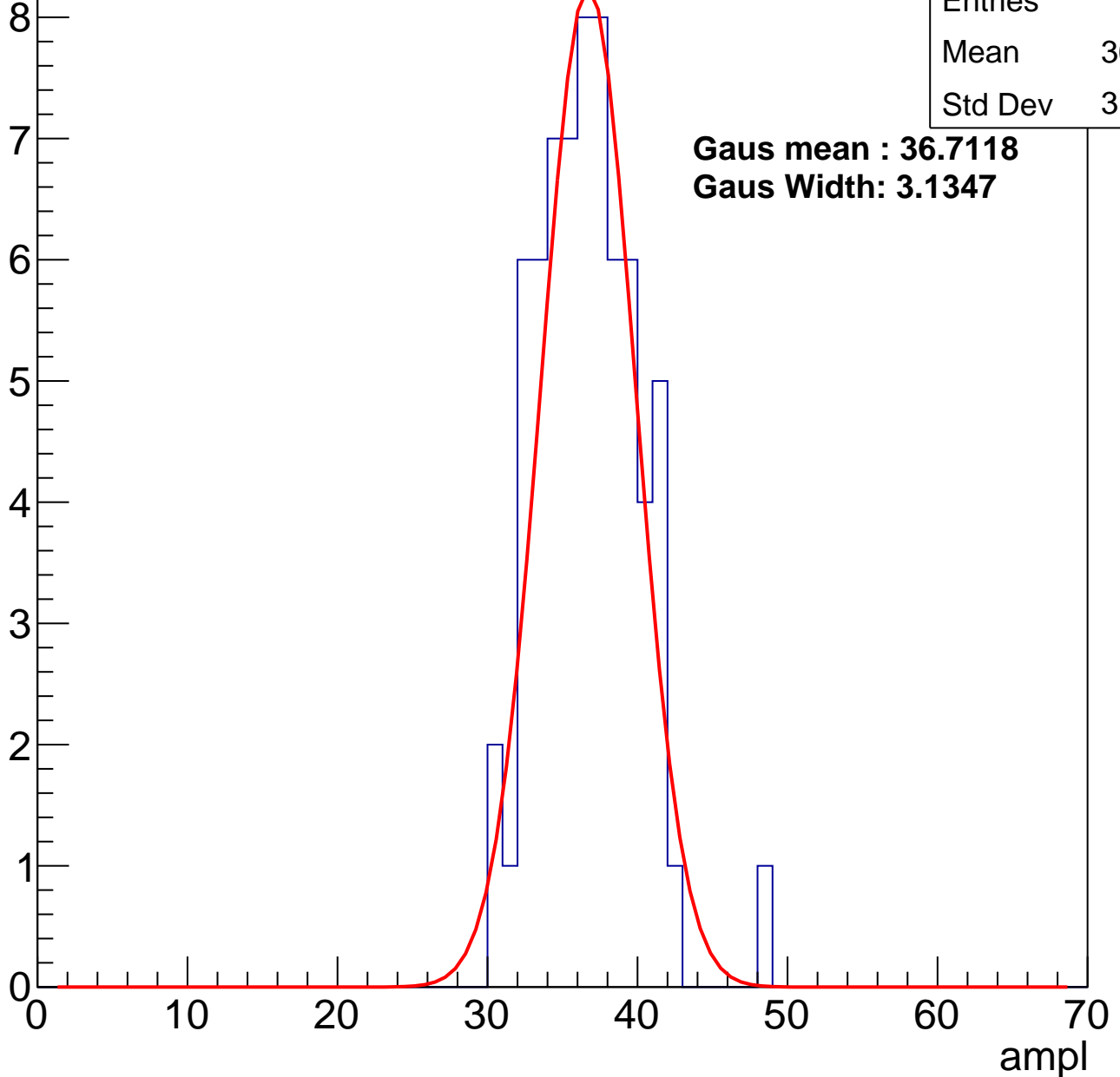
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	36.25
Std Dev	3.283

**Gaus mean : 36.7118**

**Gaus Width: 3.1347**



# B1L003S, U3-ch0, adc2

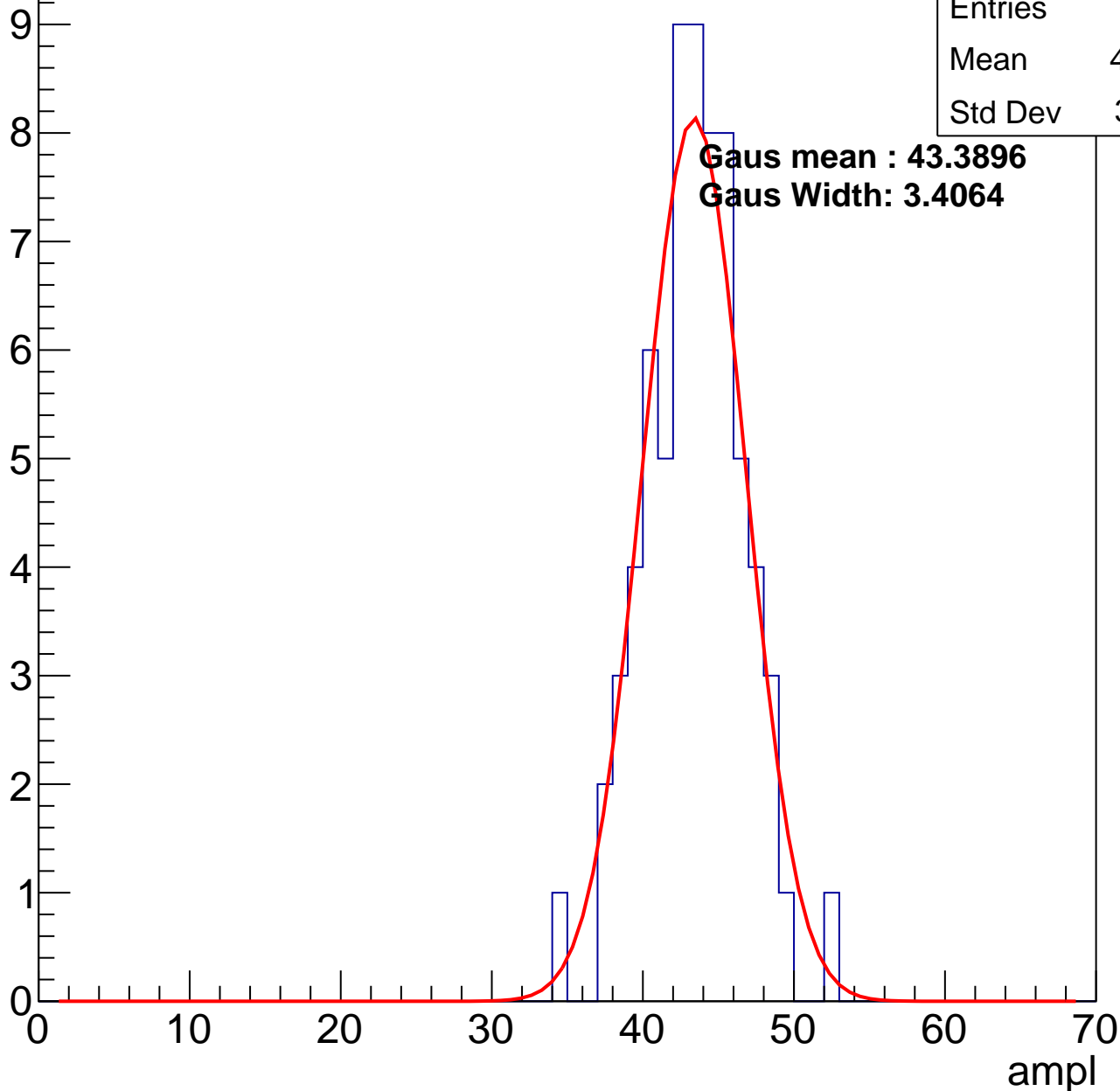
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	42.94
Std Dev	3.221

**Gaus mean : 43.3896**

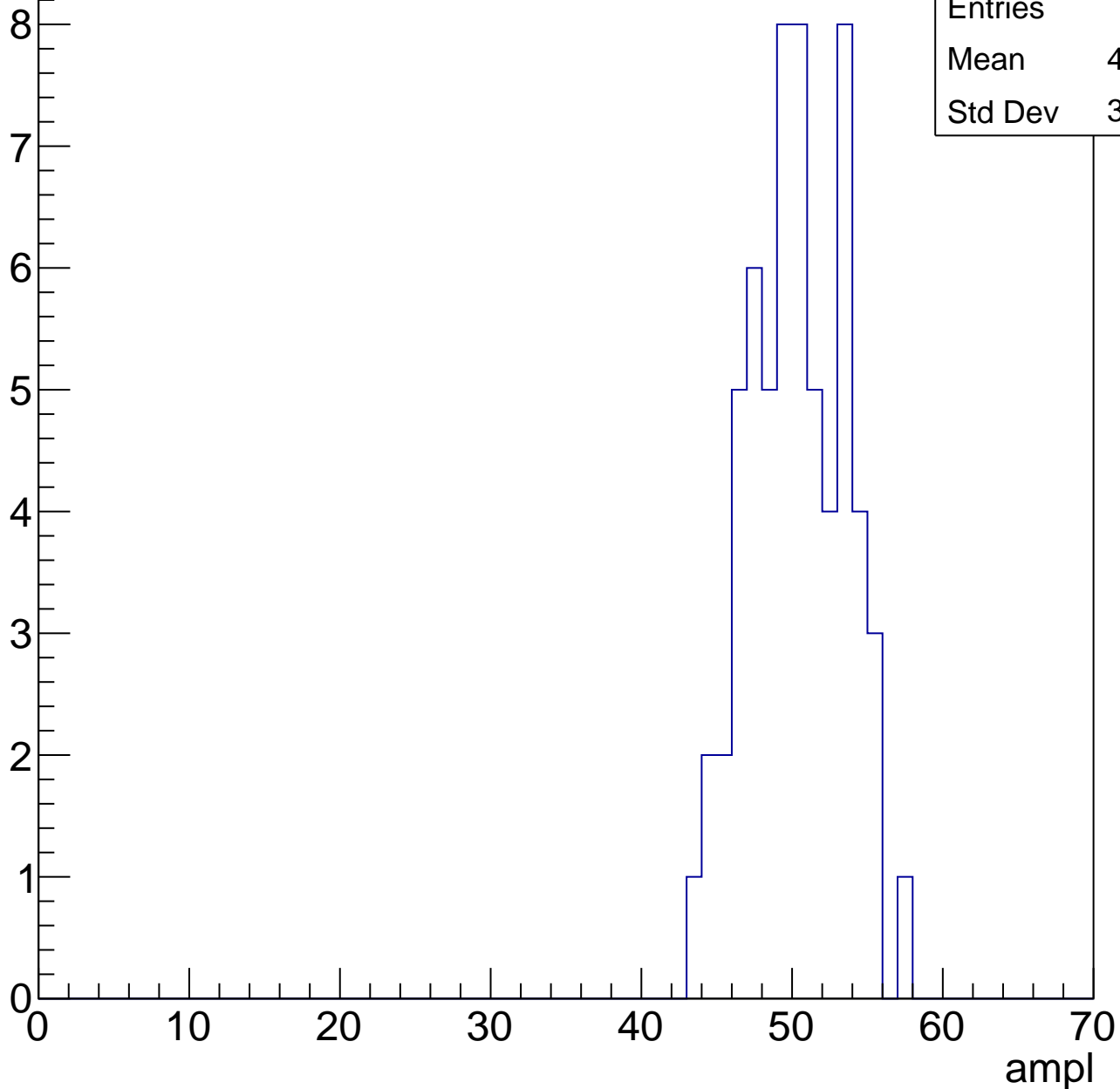
**Gaus Width: 3.4064**



# B1L003S, U3-ch0, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

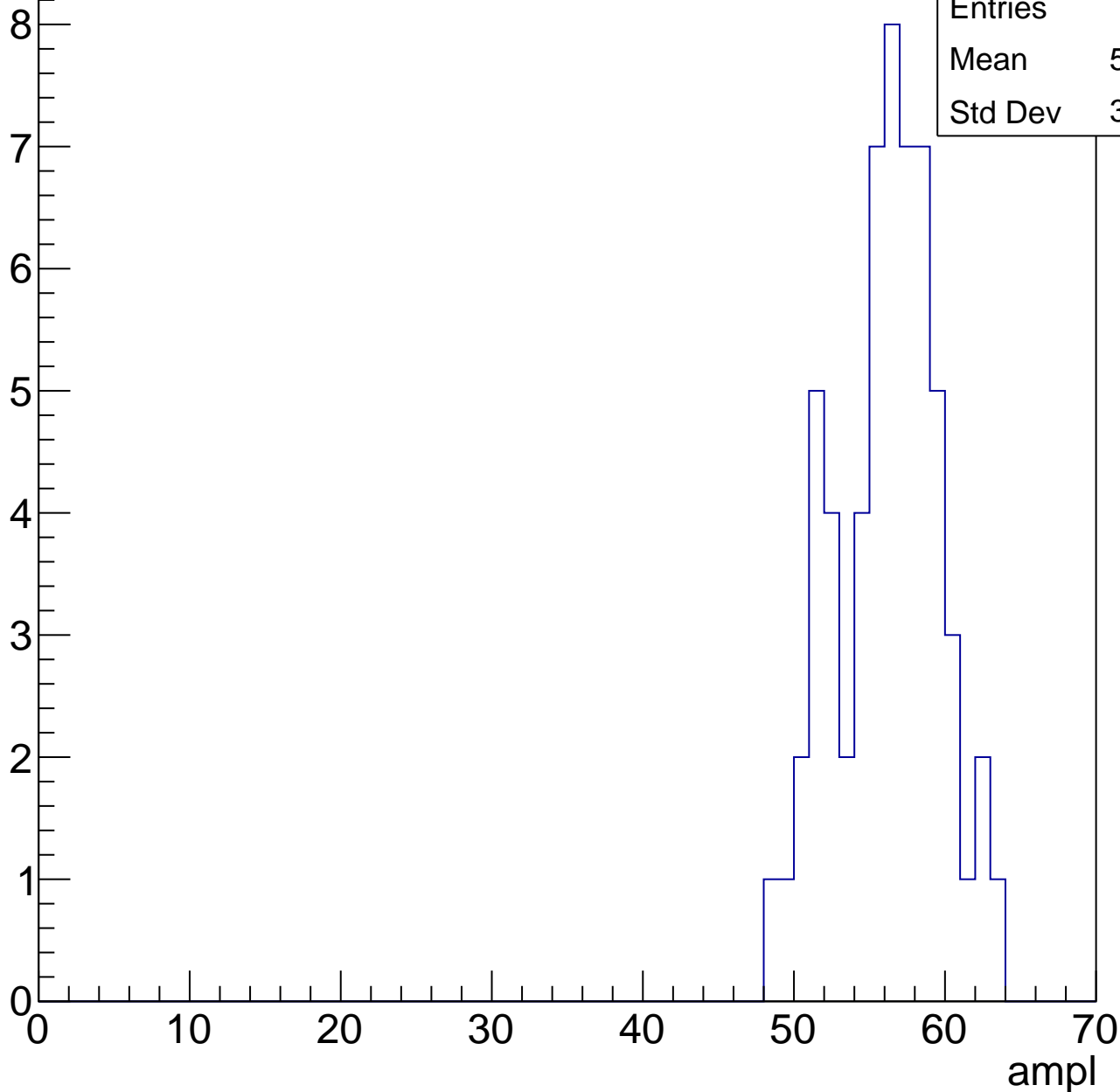


# B1L003S, U3-ch0, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	55.72
Std Dev	3.377

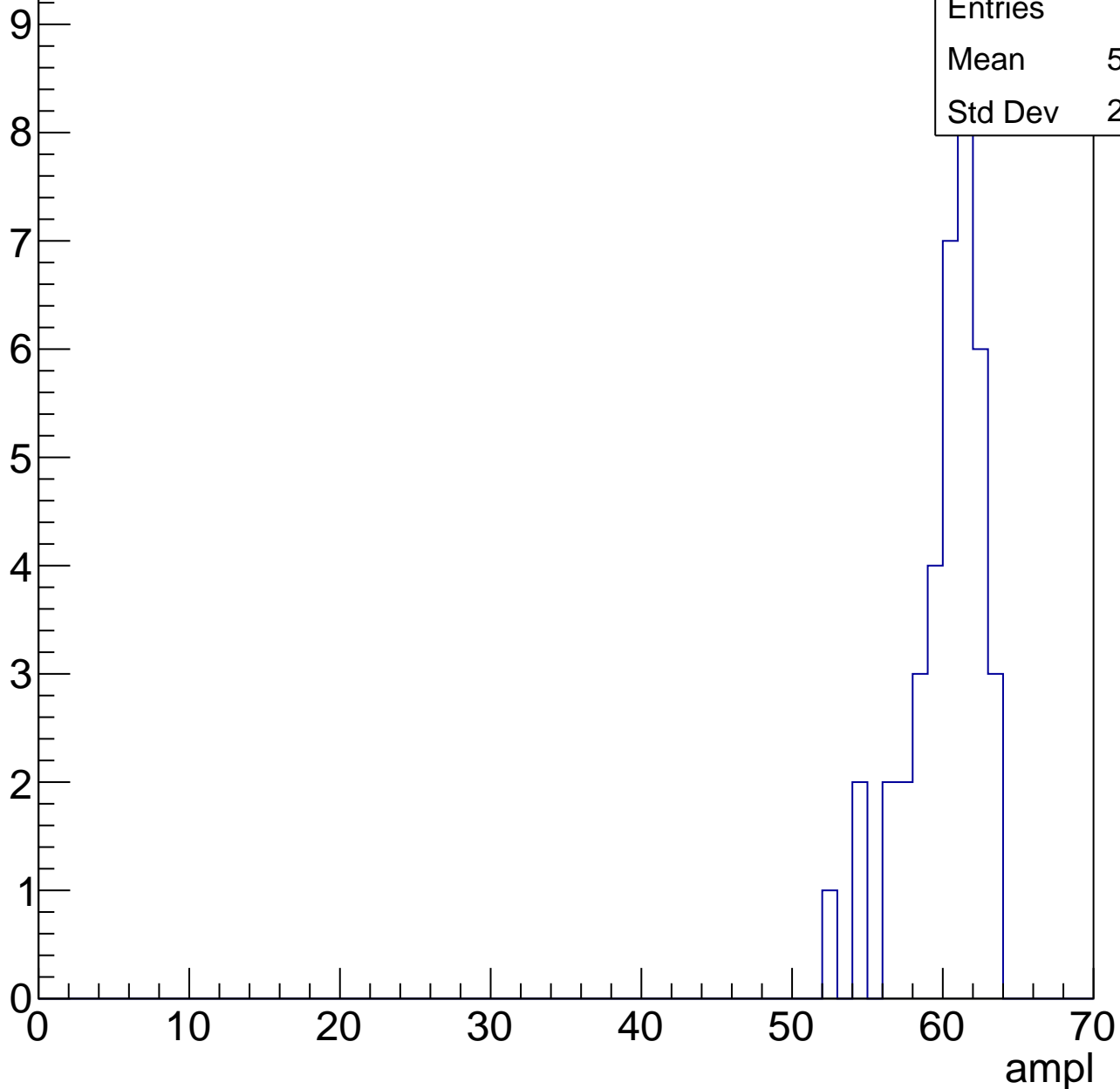


# B1L003S, U3-ch0, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	39
Mean	59.64
Std Dev	2.567

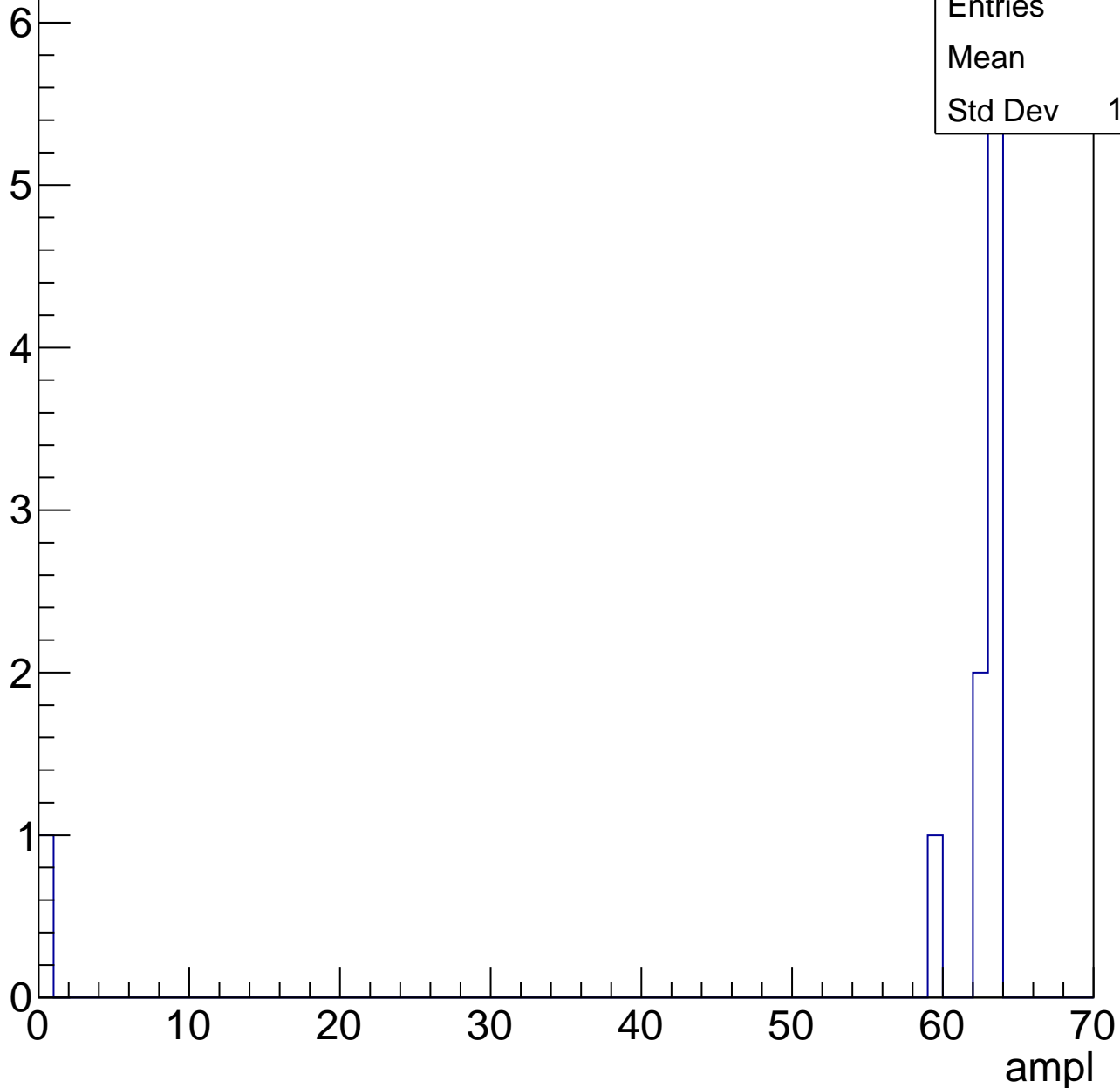


# B1L003S, U3-ch0, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	10
Mean	56.1
Std Dev	18.74





# B1L003S, U3-ch0, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U3-ch1, adc0

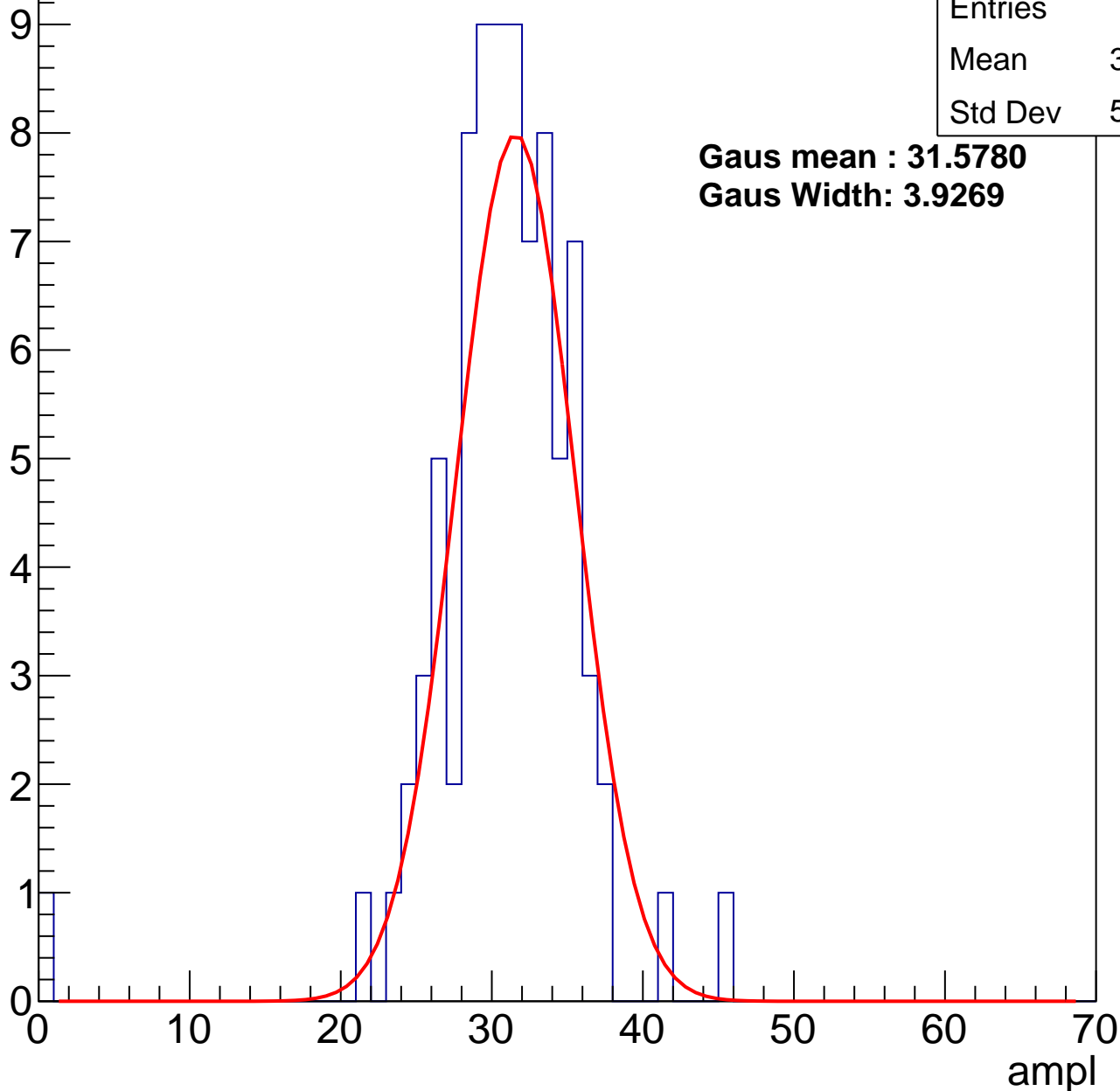
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	84
Mean	30.43
Std Dev	5.137

**Gaus mean : 31.5780**

**Gaus Width: 3.9269**



# B1L003S, U3-ch1, adc1

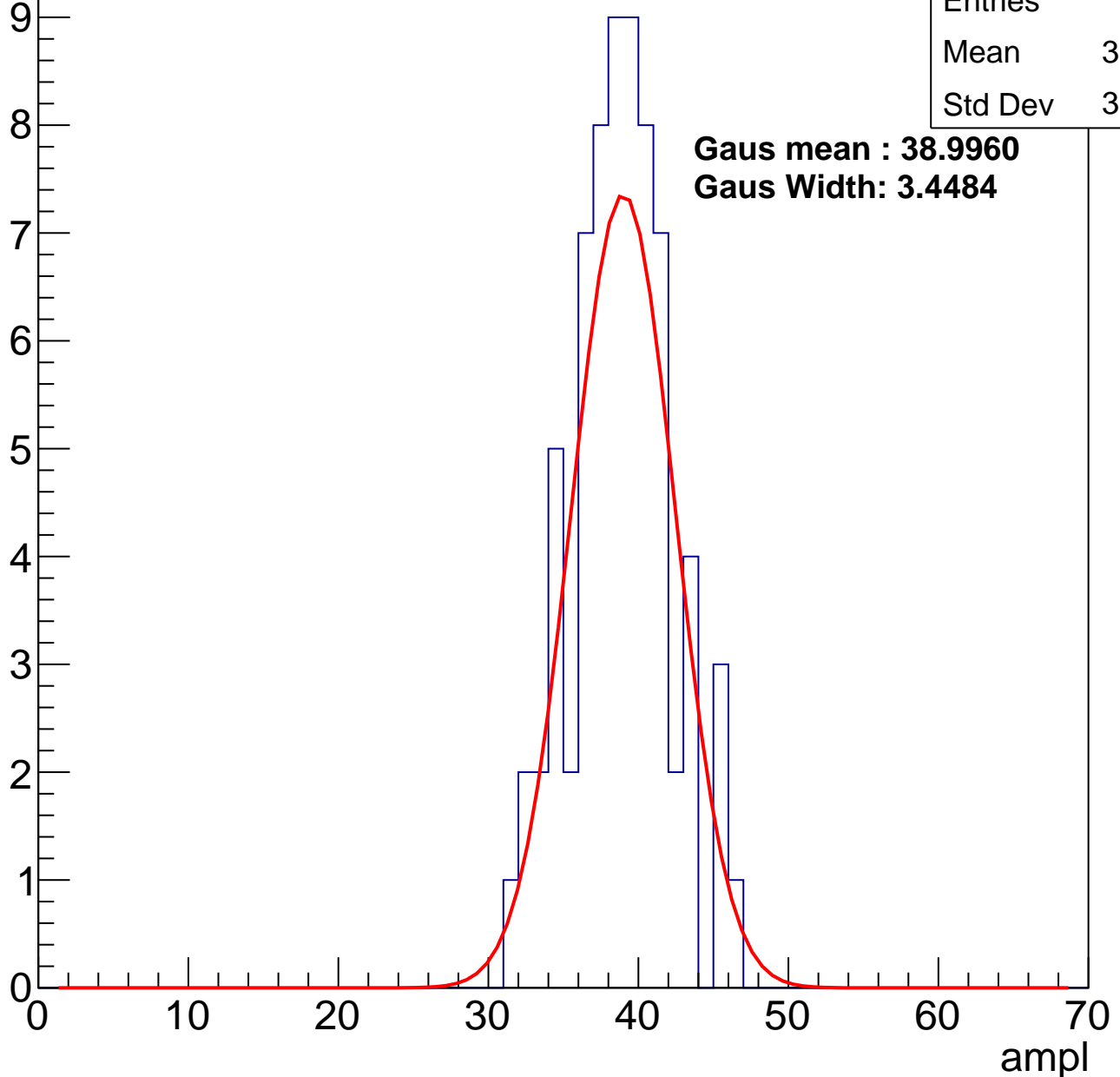
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	38.37
Std Dev	3.257

**Gaus mean : 38.9960**

**Gaus Width: 3.4484**



# B1L003S, U3-ch1, adc2

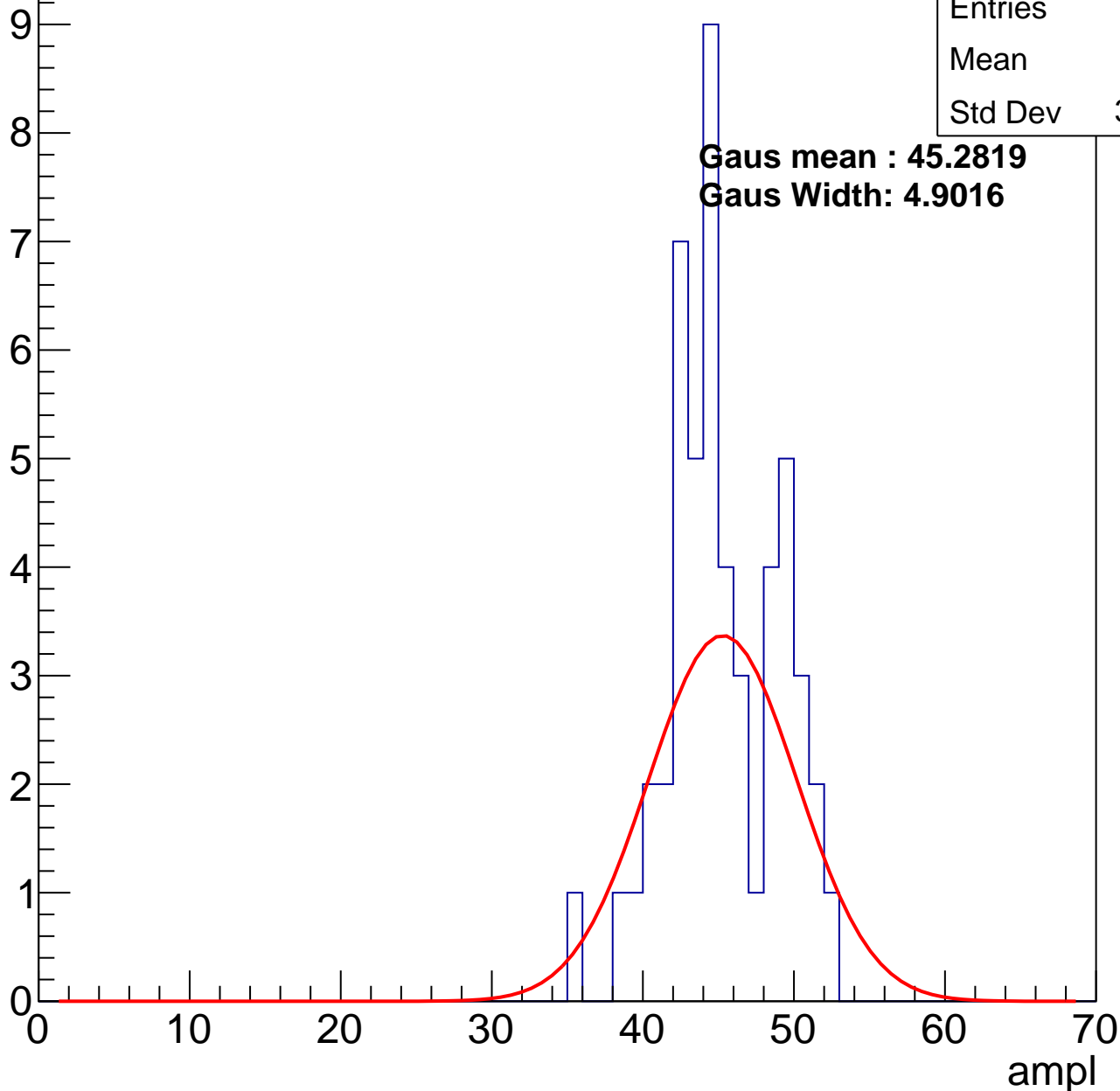
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	51
Mean	44.8
Std Dev	3.641

**Gaus mean : 45.2819**

**Gaus Width: 4.9016**

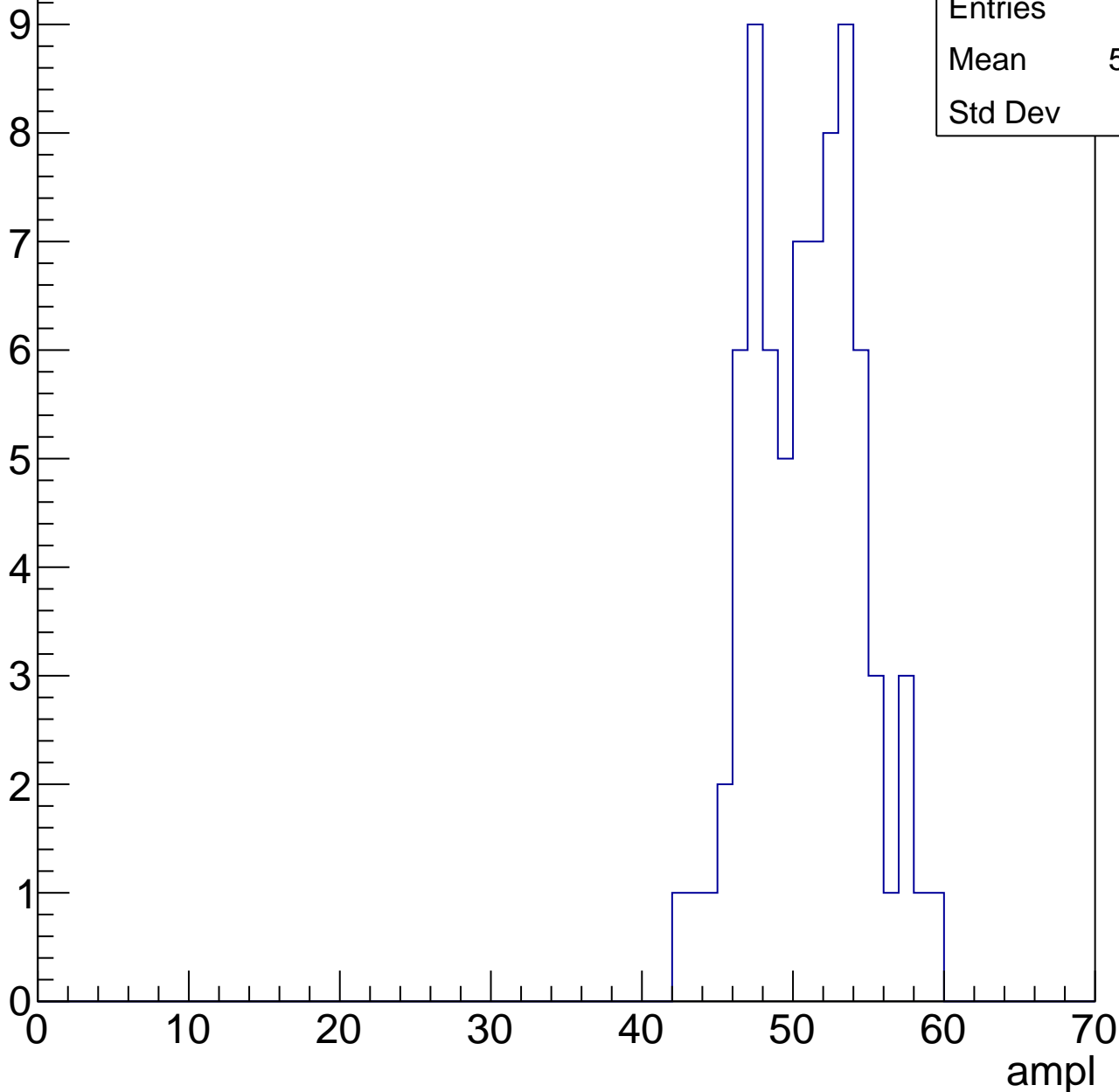


# B1L003S, U3-ch1, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

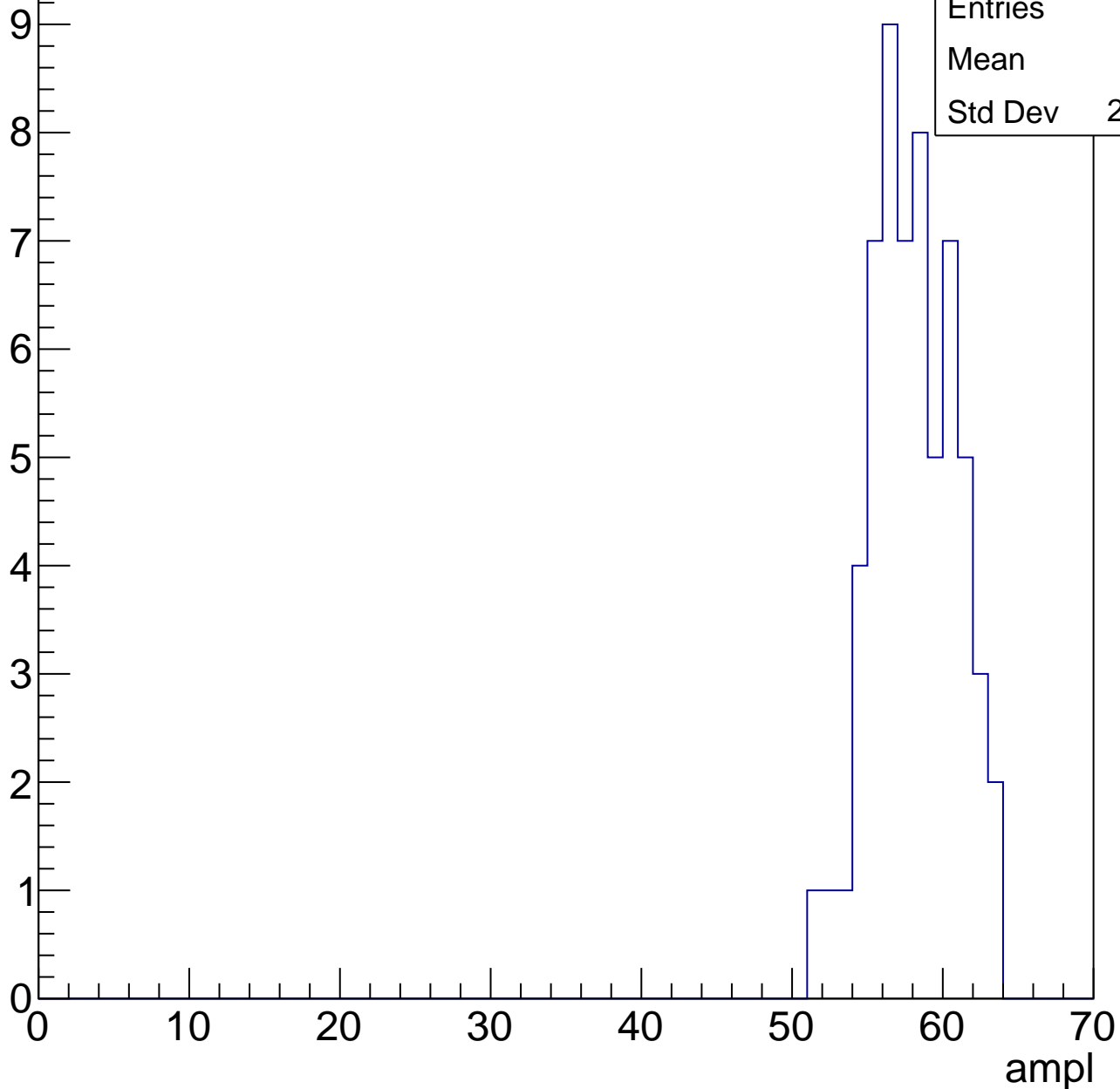
Entries	77
Mean	50.44
Std Dev	3.62



# B1L003S, U3-ch1, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

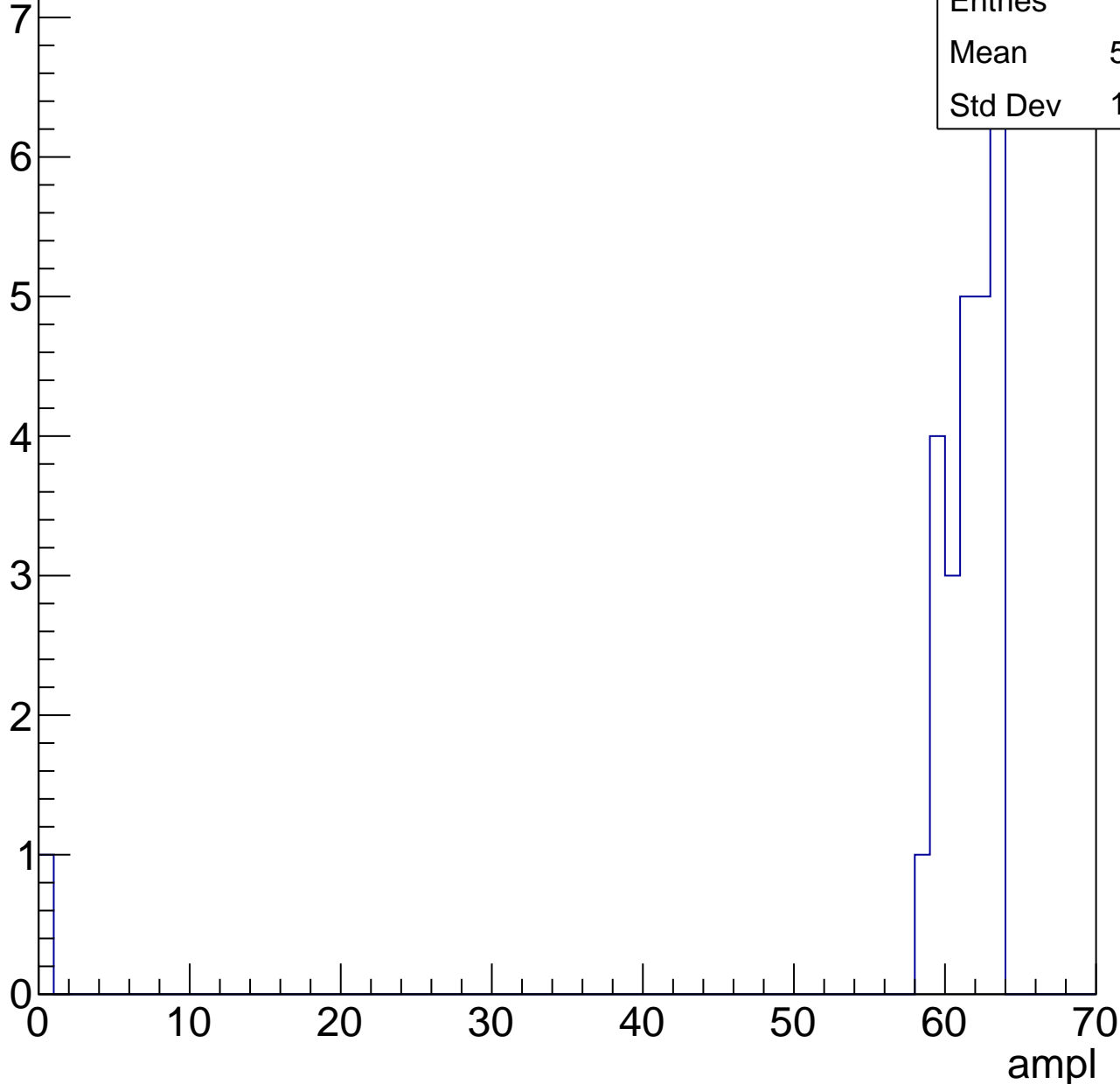


# B1L003S, U3-ch1, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	26
Mean	58.85
Std Dev	11.87



# B1L003S, U3-ch1, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

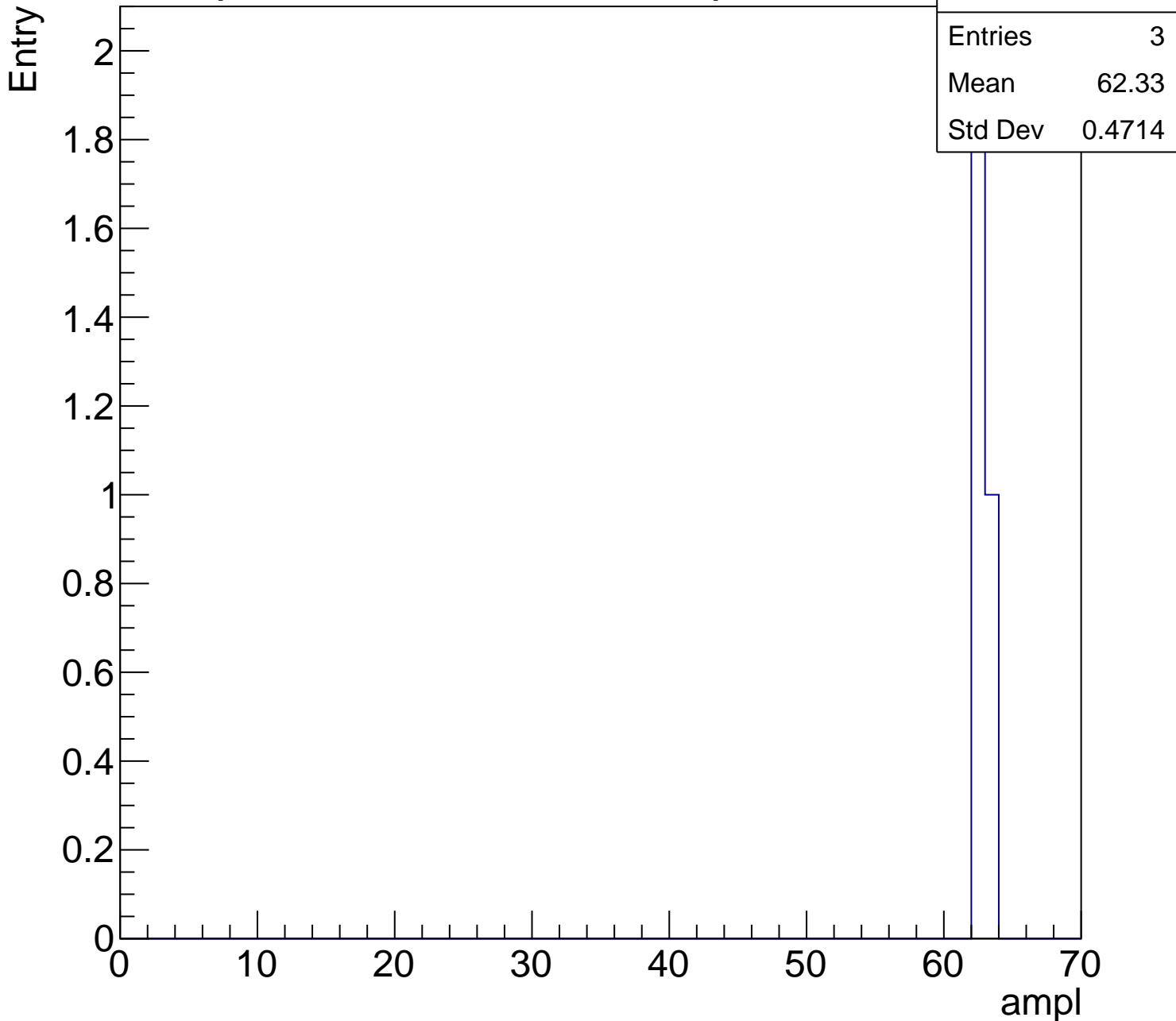
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.33
Std Dev	0.4714

0 10 20 30 40 50 60 70

ampl





# B1L003S, U3-ch1, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U3-ch2, adc0

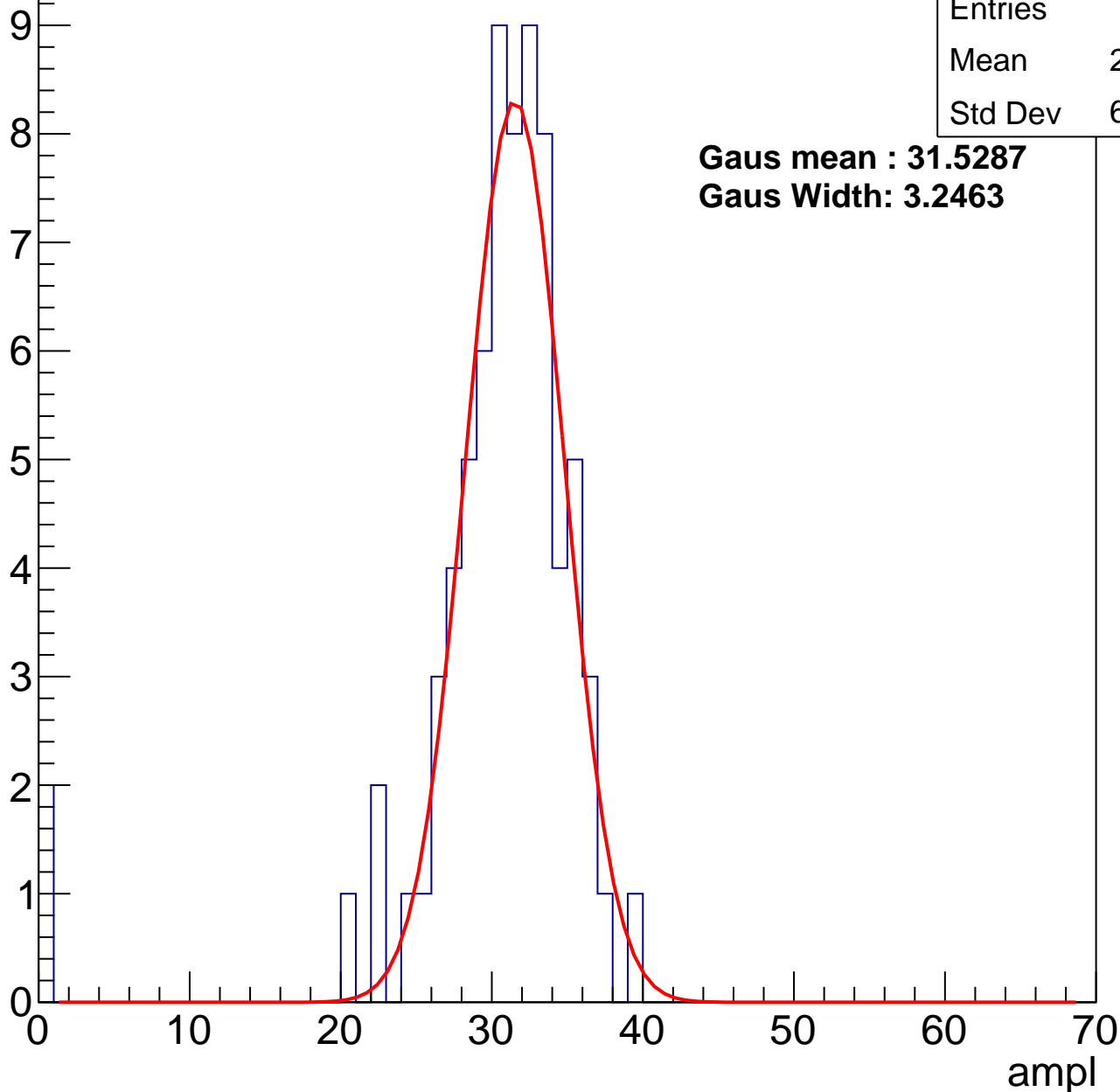
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	73
Mean	29.84
Std Dev	6.127

**Gaus mean : 31.5287**

**Gaus Width: 3.2463**



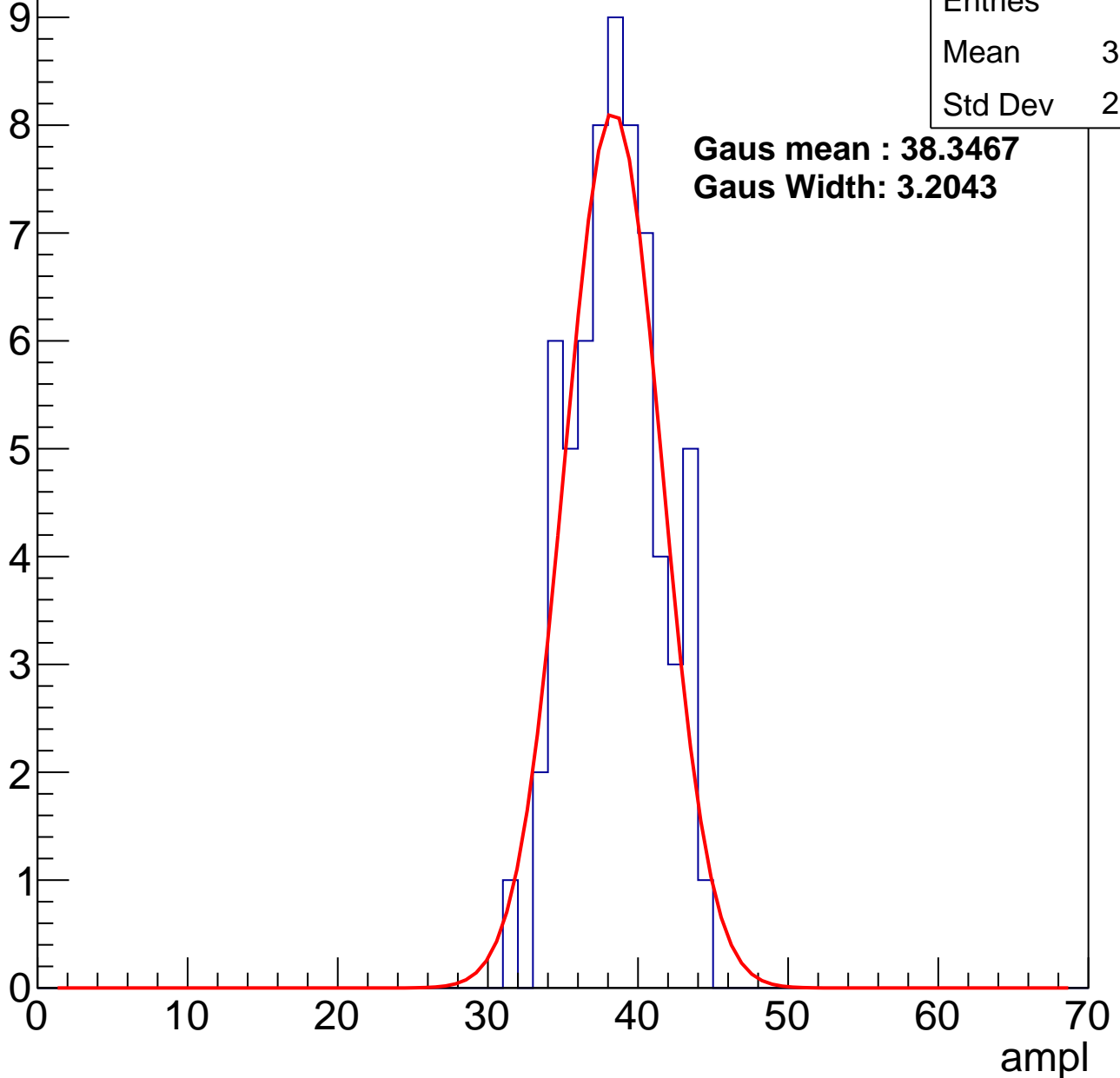
# B1L003S, U3-ch2, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	38.02
Std Dev	2.917

**Gaus mean : 38.3467**  
**Gaus Width: 3.2043**



# B1L003S, U3-ch2, adc2

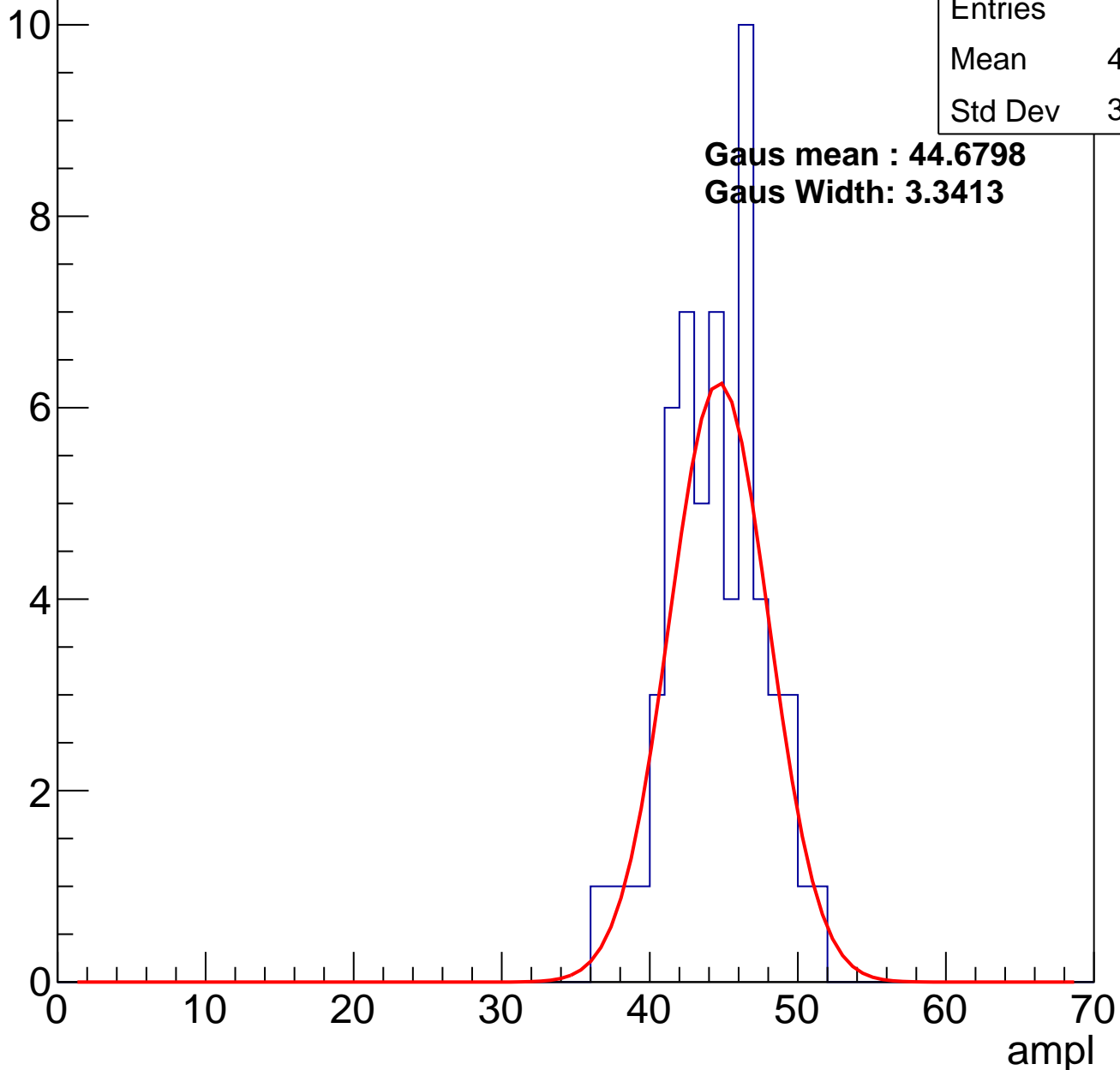
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	58
Mean	44.02
Std Dev	3.208

**Gaus mean : 44.6798**

**Gaus Width: 3.3413**

Entry

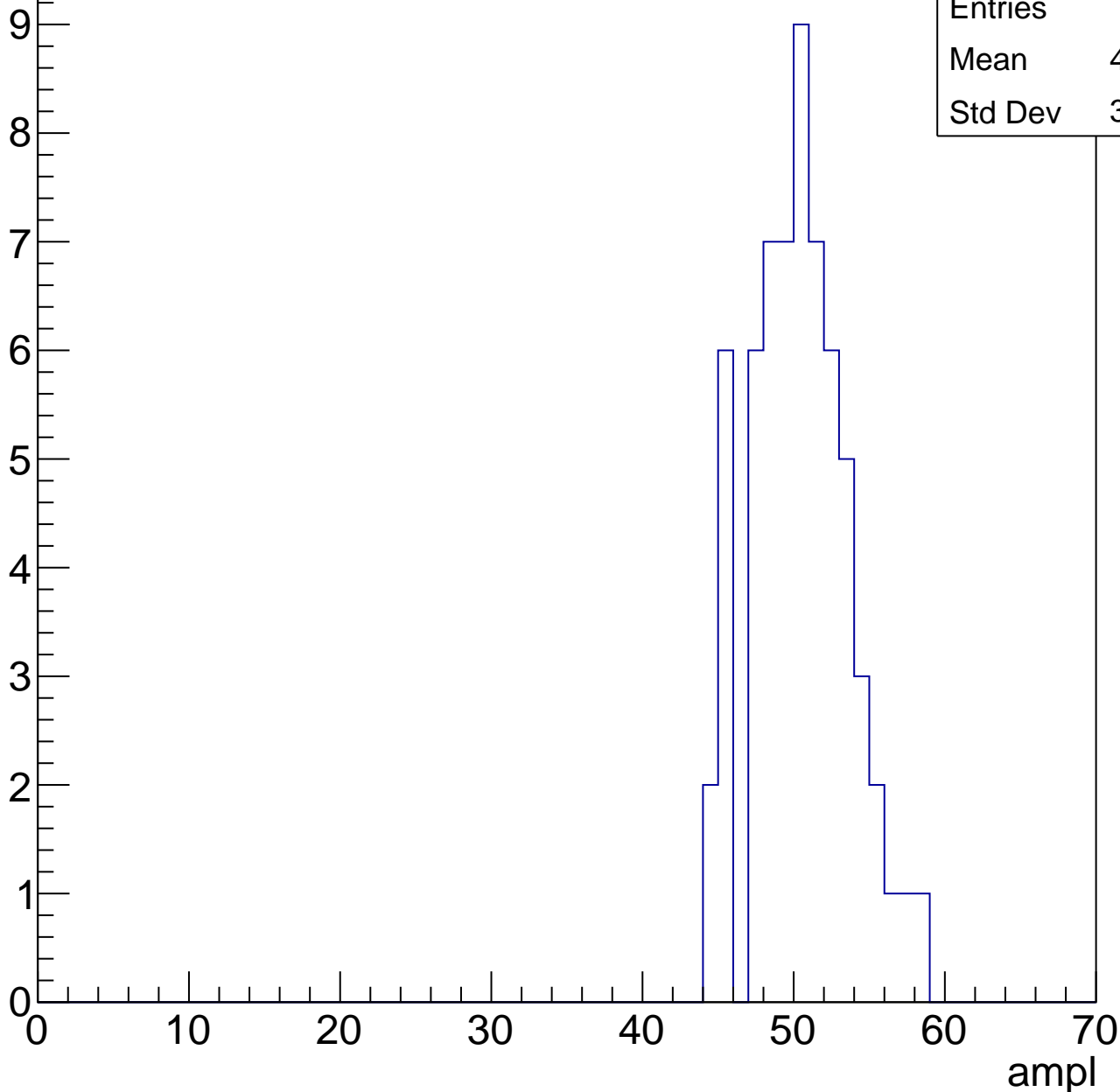


# B1L003S, U3-ch2, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	49.94
Std Dev	3.172

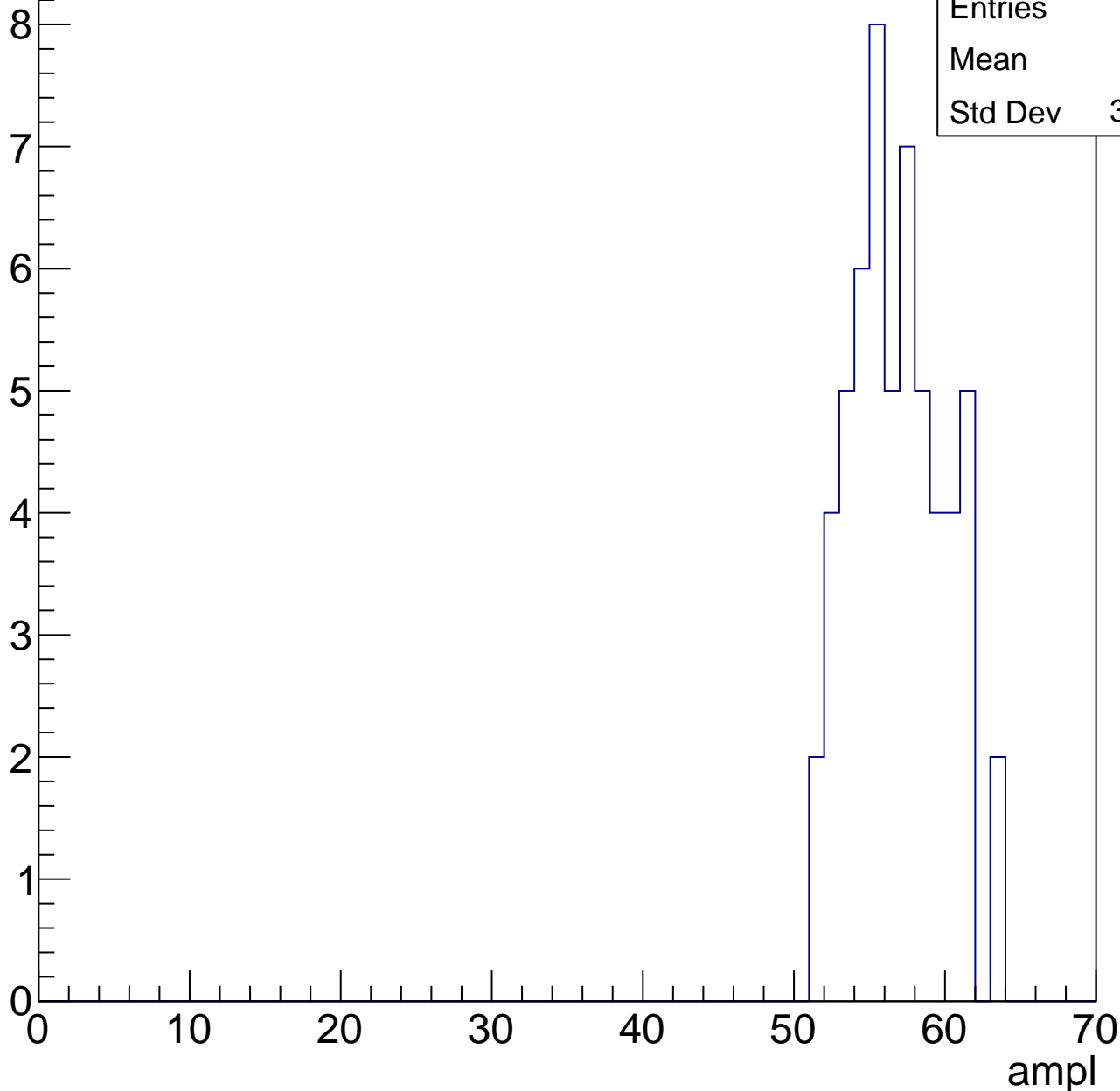


# B1L003S, U3-ch2, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	56.4
Std Dev	3.054



# B1L003S, U3-ch2, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

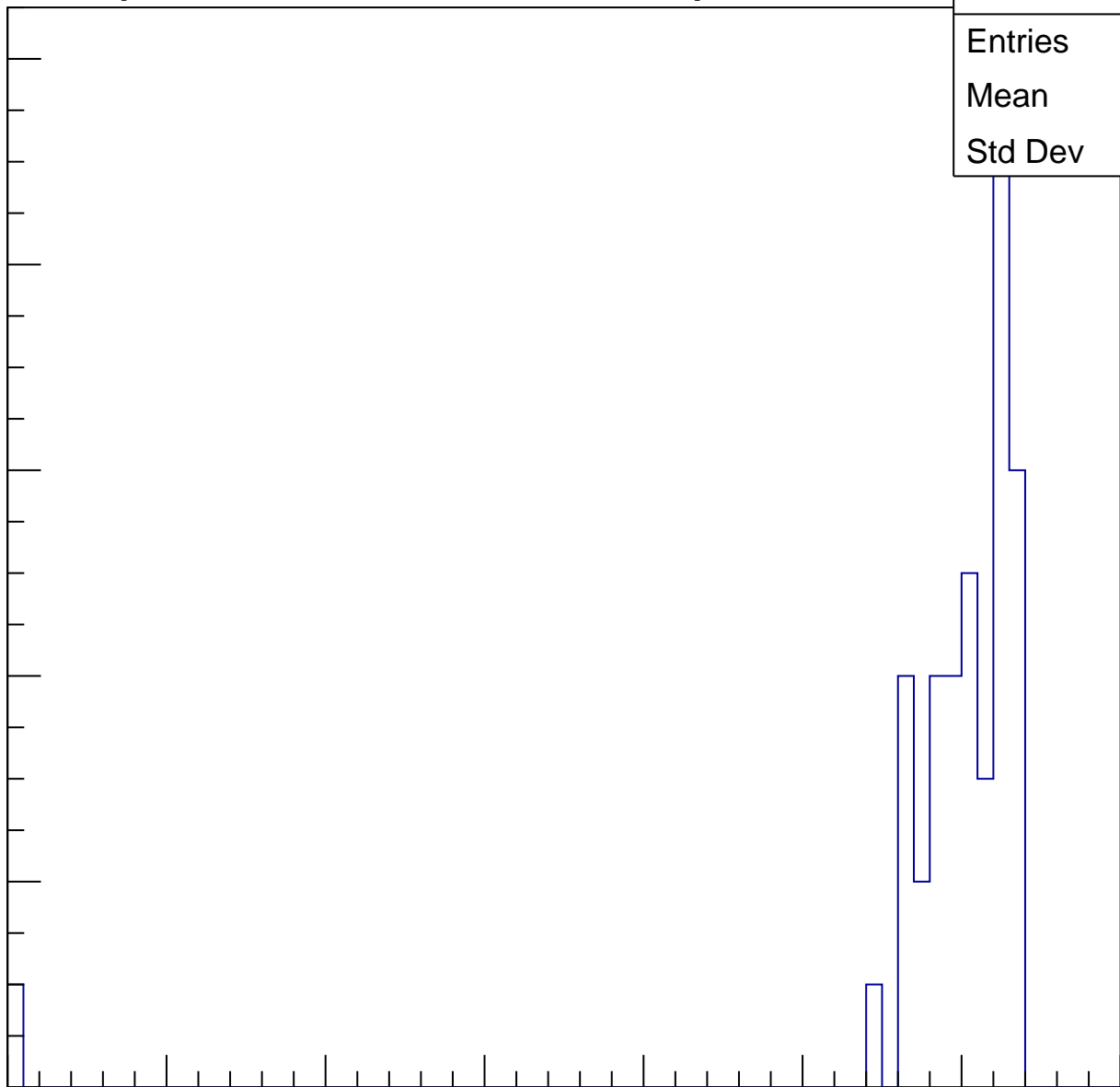
Entries	40
Mean	58.52
Std Dev	9.68

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

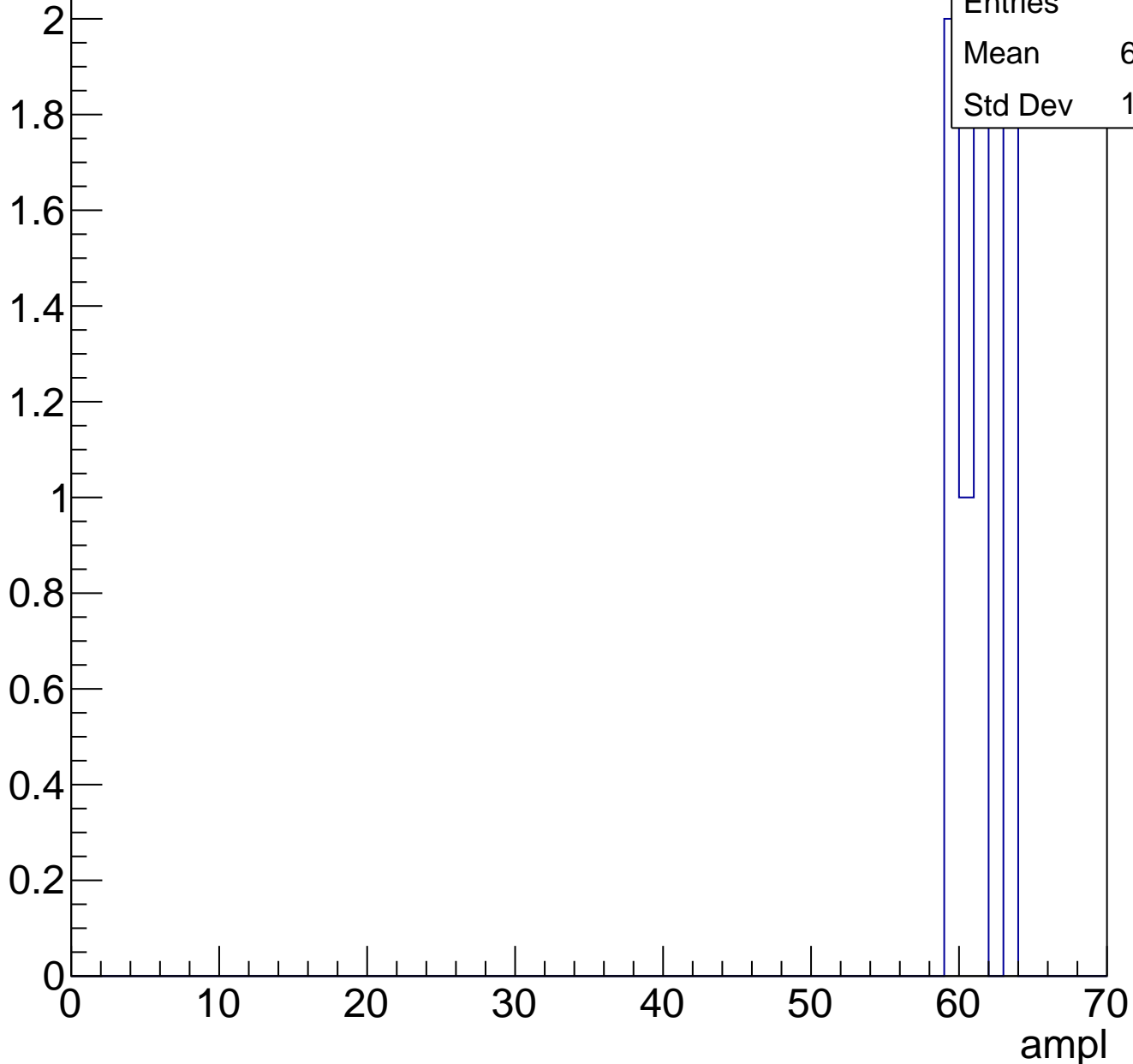
ampl



# B1L003S, U3-ch2, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch2, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U3-ch3, adc0

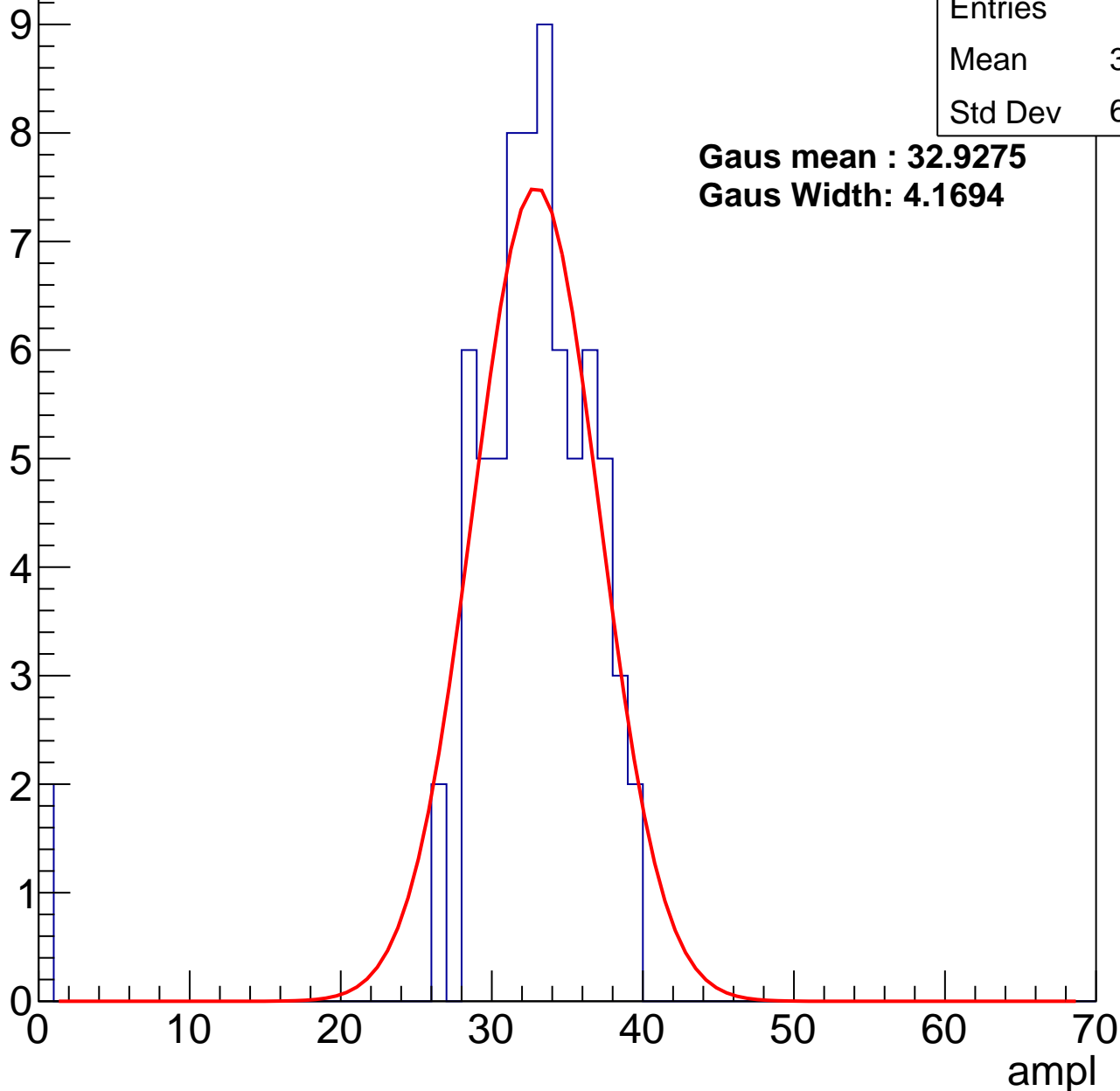
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	72
Mean	31.78
Std Dev	6.225

**Gaus mean : 32.9275**

**Gaus Width: 4.1694**



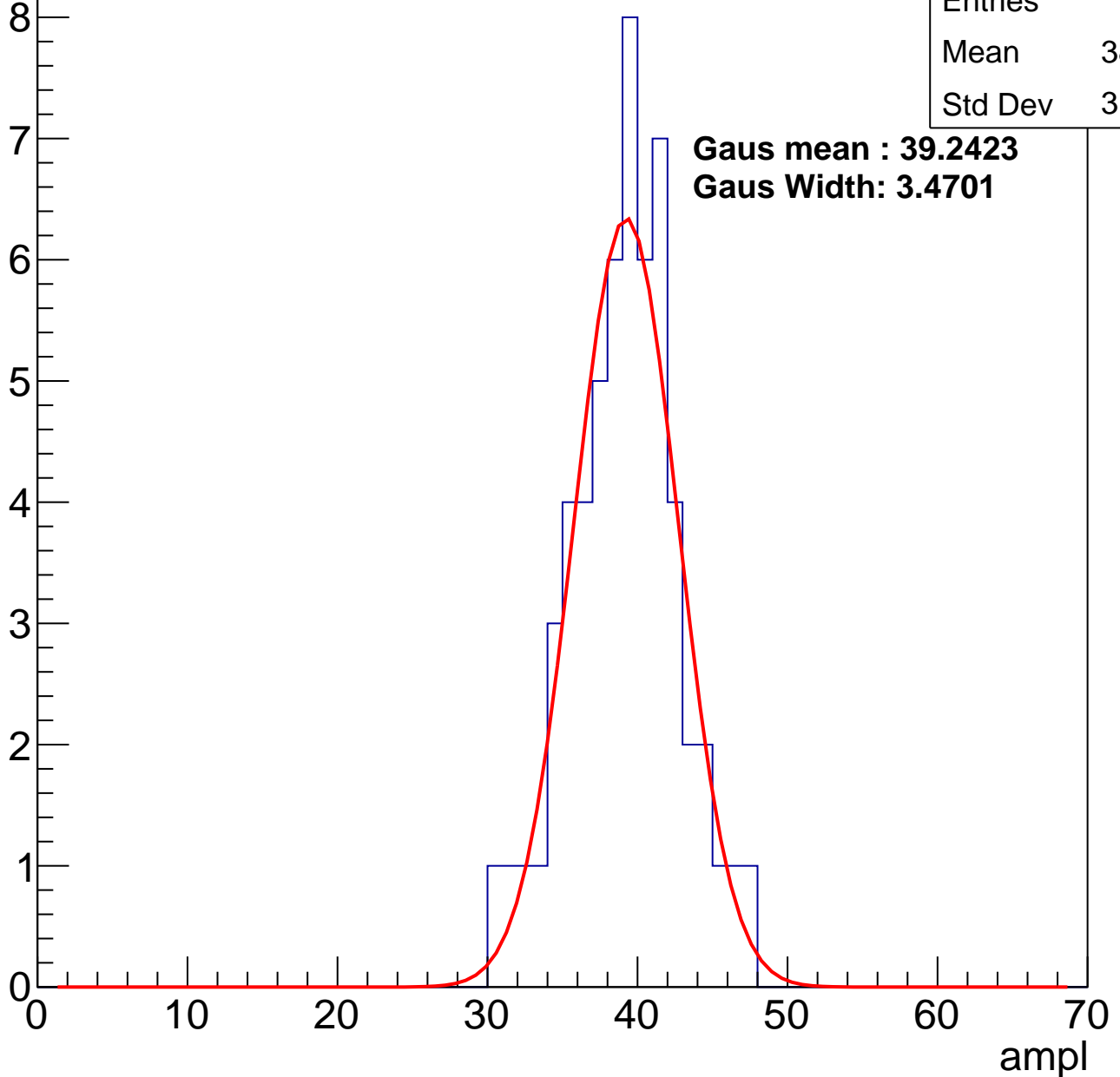
# B1L003S, U3-ch3, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	38.69
Std Dev	3.539

**Gaus mean : 39.2423**  
**Gaus Width: 3.4701**



# B1L003S, U3-ch3, adc2

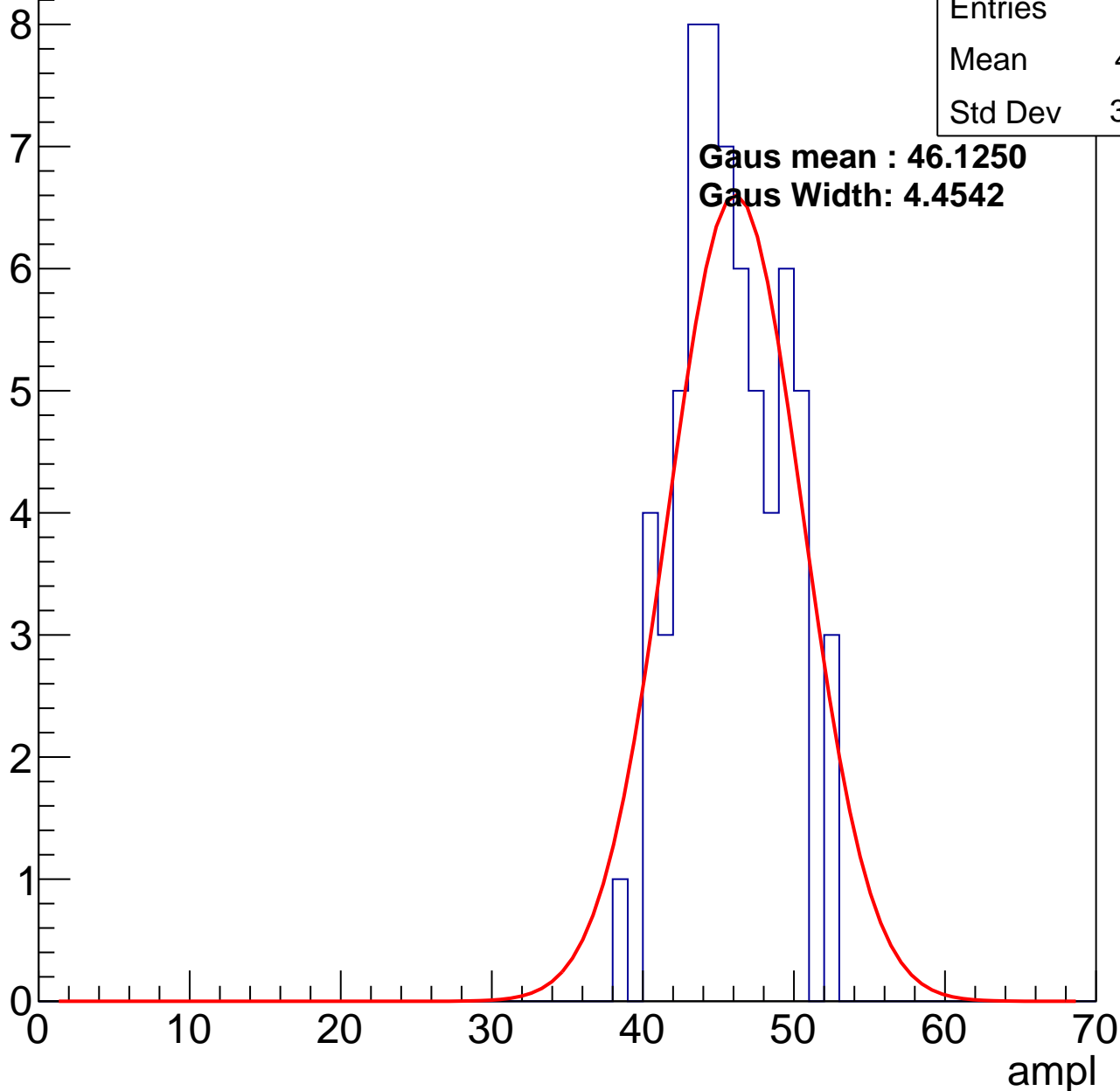
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	45.31
Std Dev	3.295

**Gaus mean : 46.1250**

**Gaus Width: 4.4542**

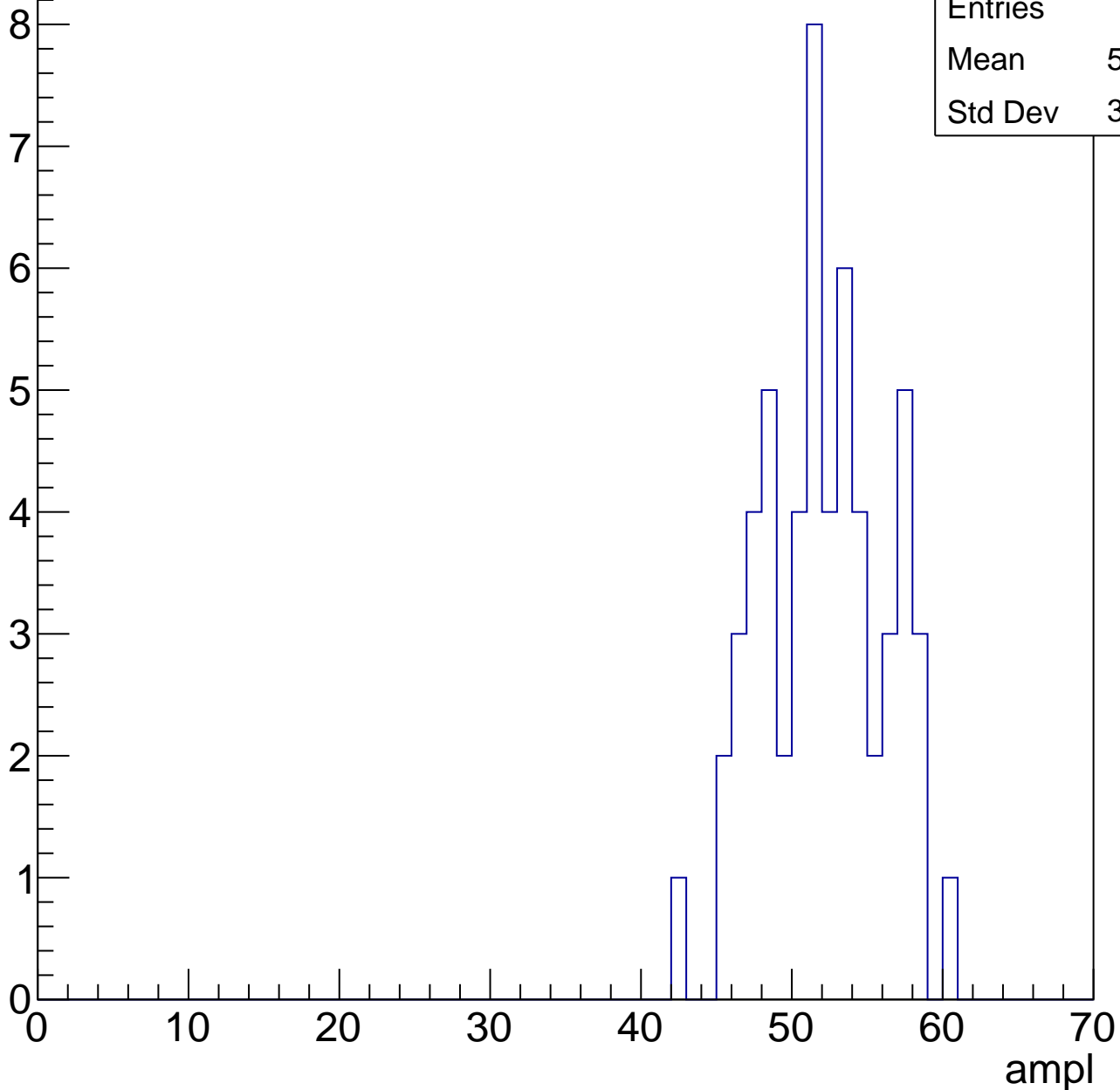


# B1L003S, U3-ch3, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

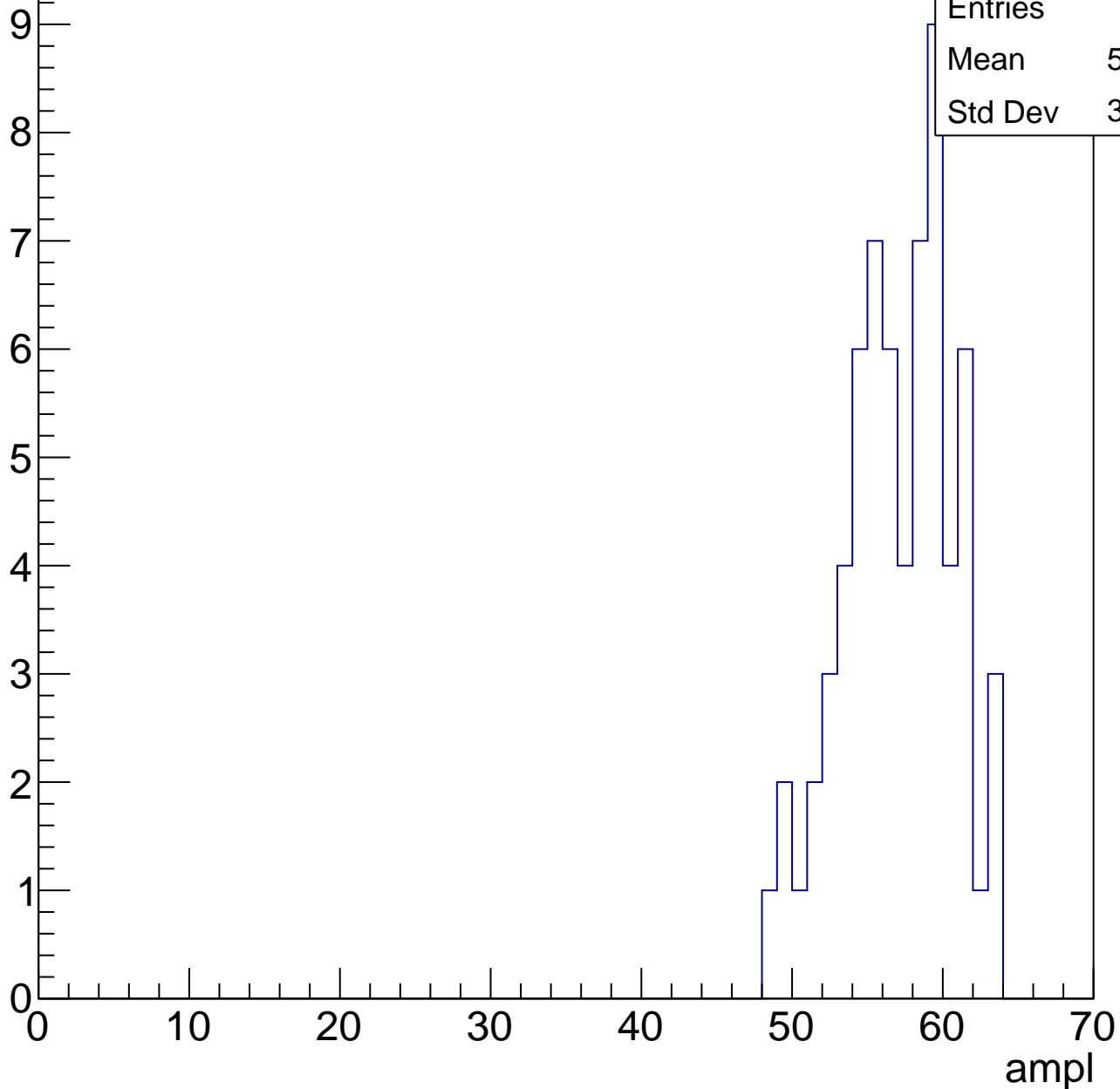
Entries	57
Mean	51.63
Std Dev	3.985



# B1L003S, U3-ch3, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

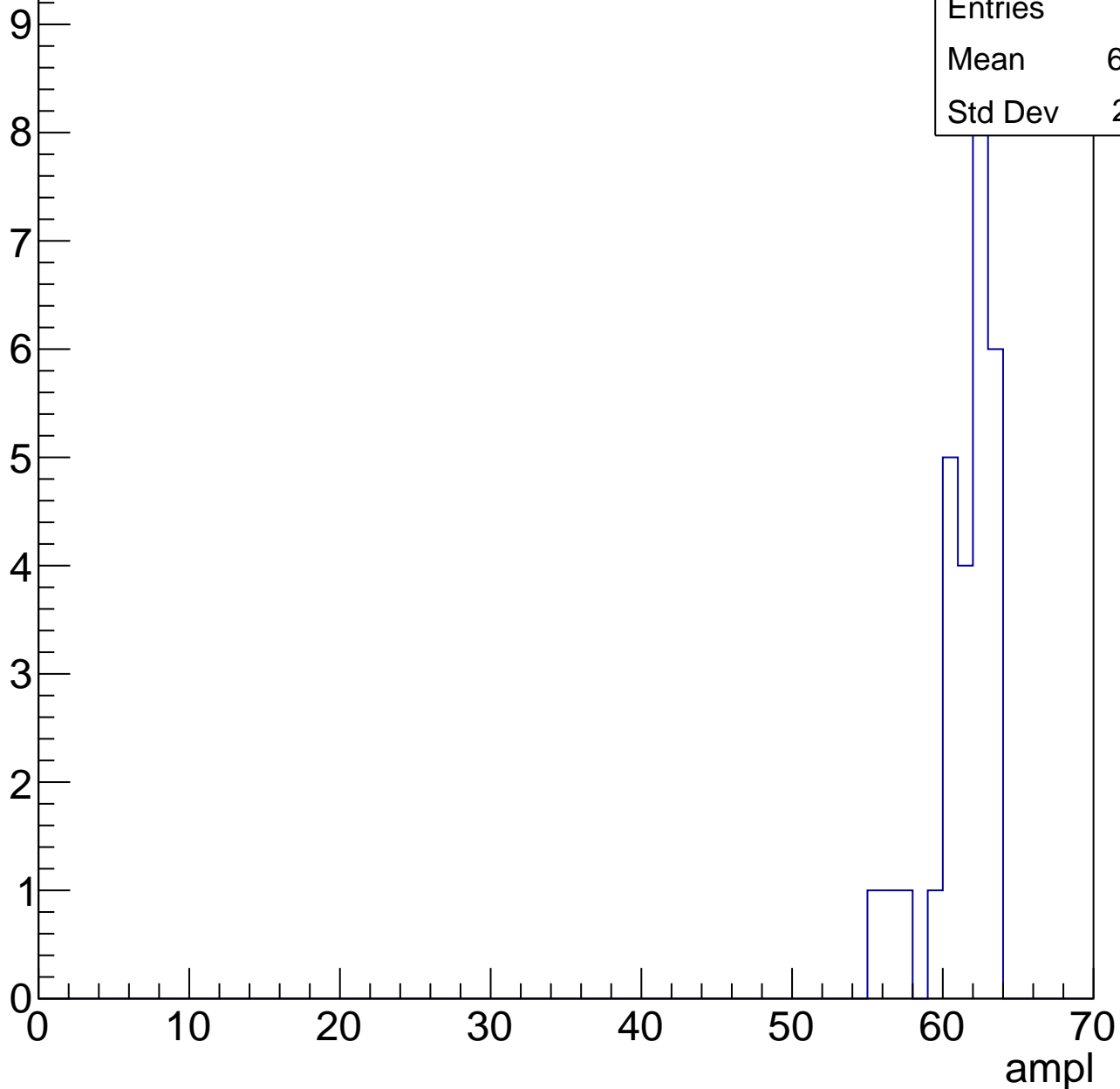


# B1L003S, U3-ch3, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

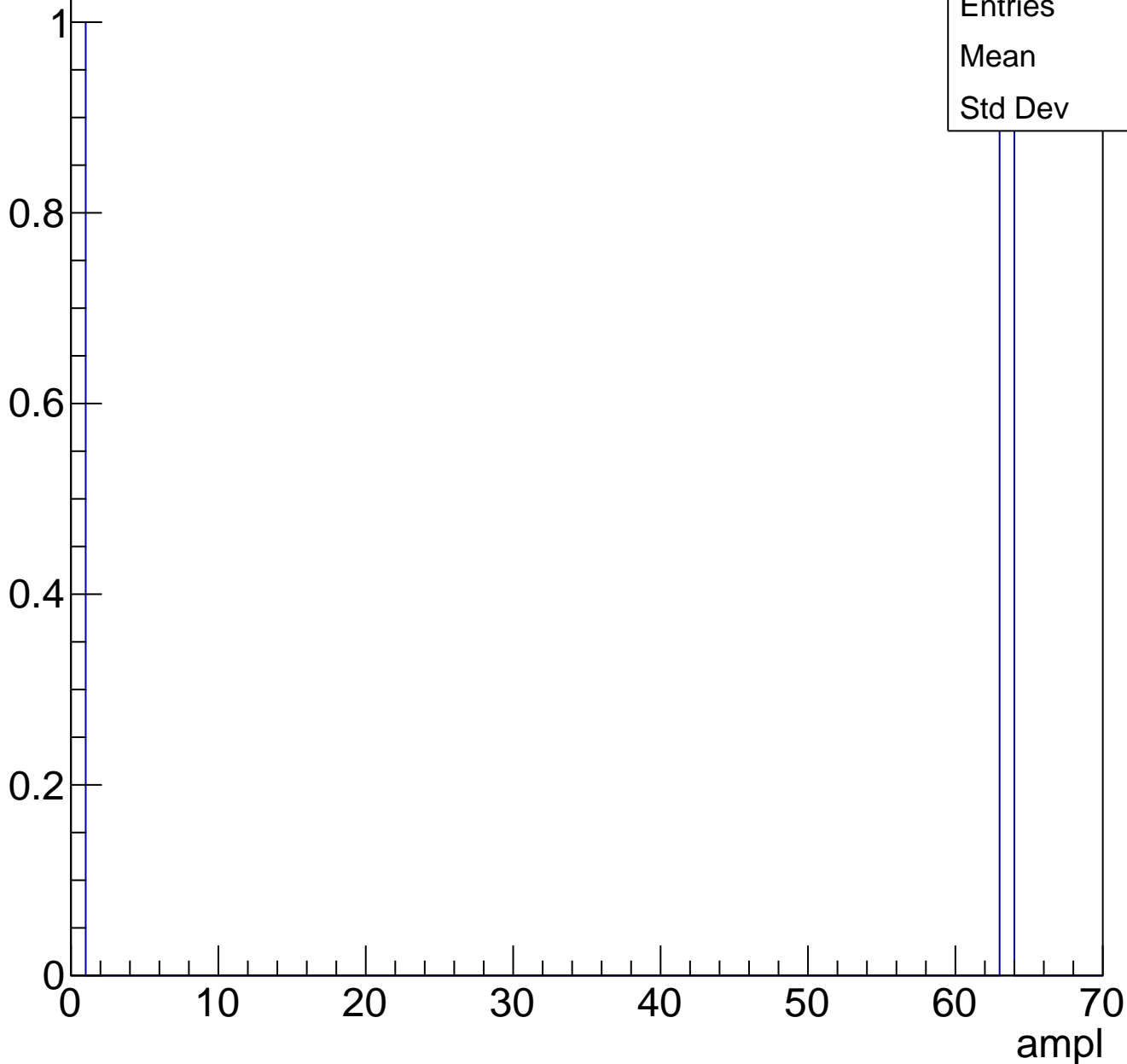
Entries	28
Mean	60.96
Std Dev	2.061



# B1L003S, U3-ch3, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch3, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L003S, U3-ch4, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	87
Mean	32.08
Std Dev	3.73

**Gaus mean : 33.1235**

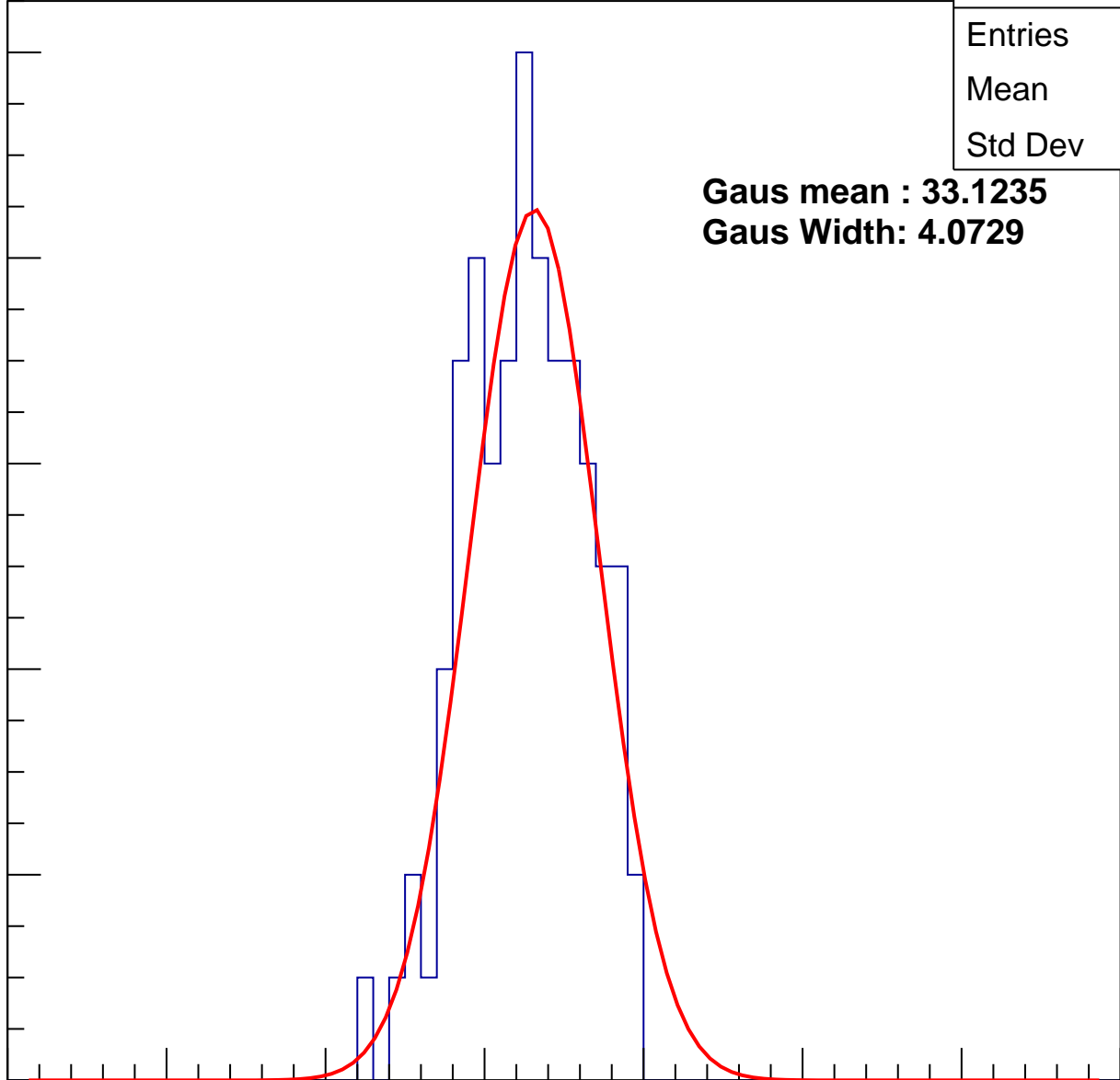
**Gaus Width: 4.0729**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U3-ch4, adc1

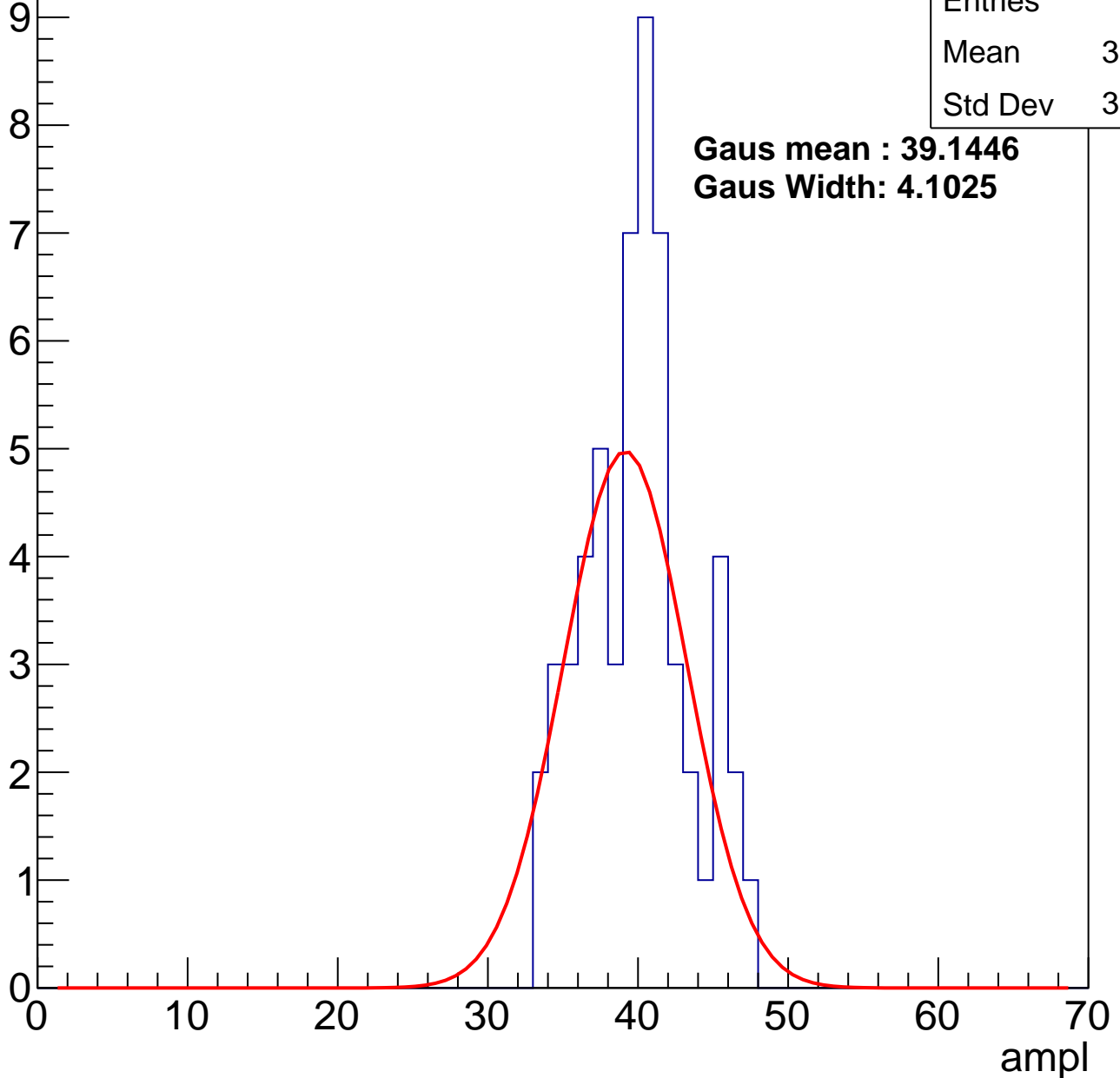
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	39.48
Std Dev	3.454

**Gaus mean : 39.1446**

**Gaus Width: 4.1025**



# B1L003S, U3-ch4, adc2

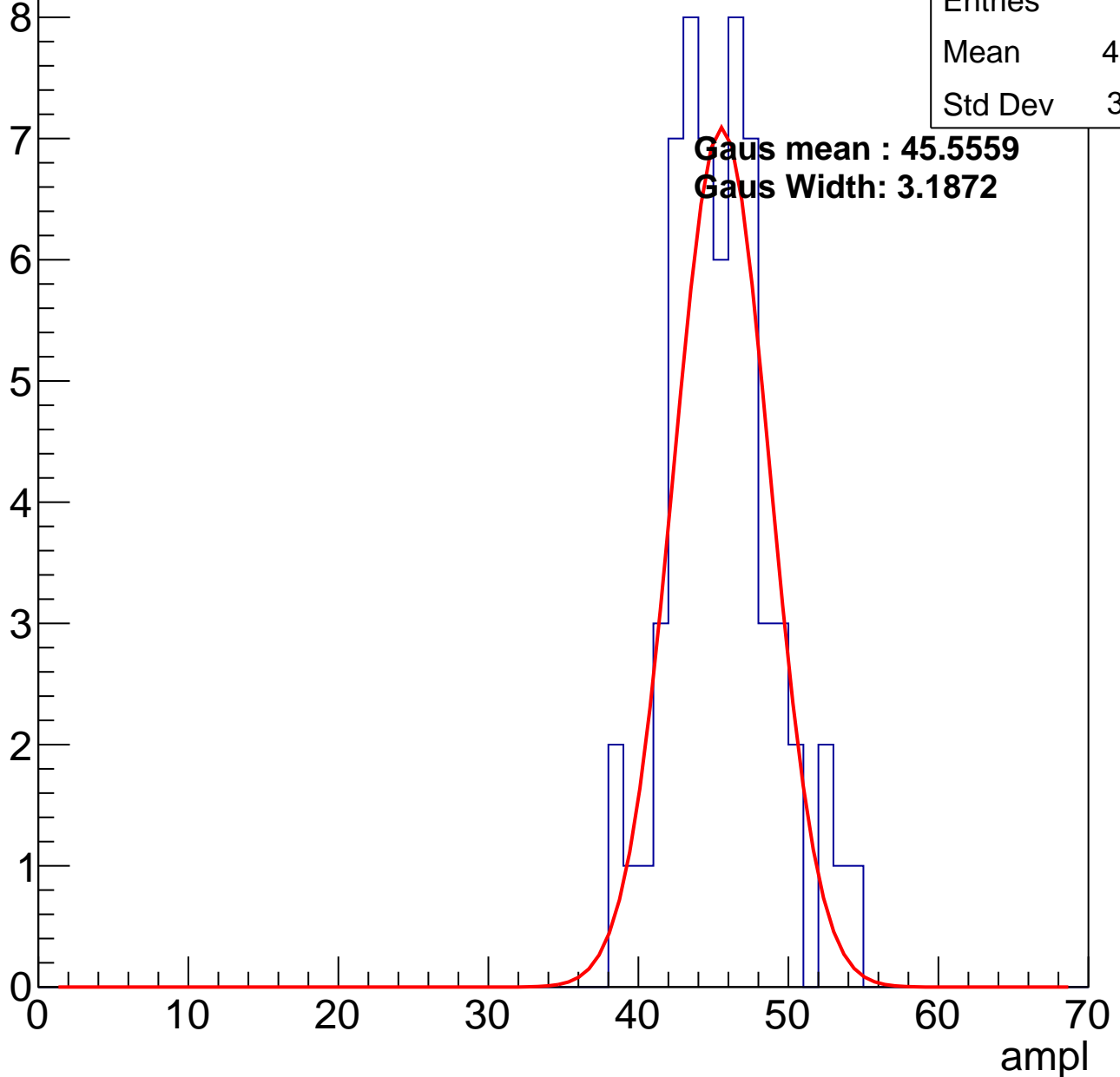
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	45.05
Std Dev	3.391

**Gaus mean : 45.5559**

**Gaus Width: 3.1872**

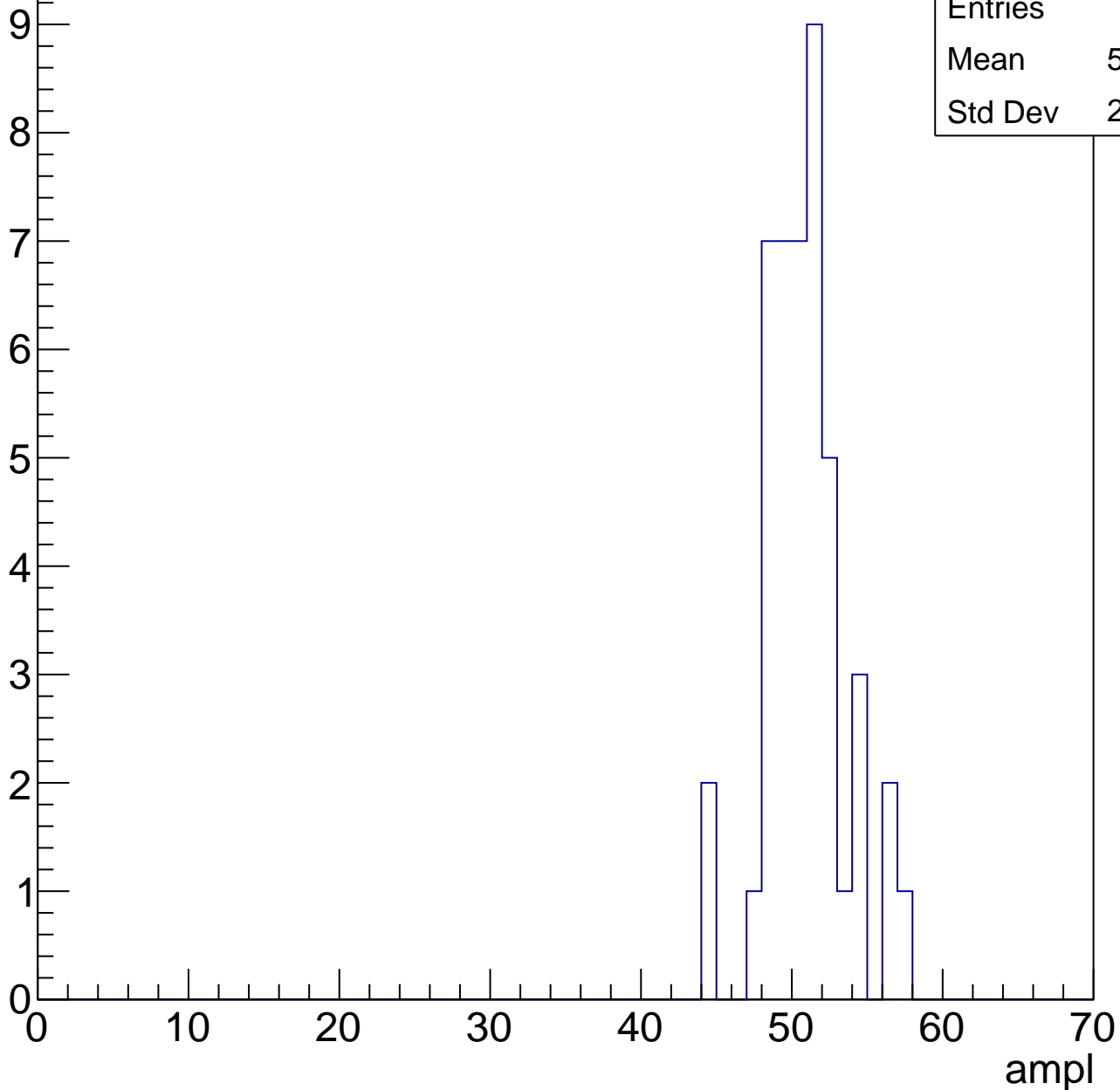


# B1L003S, U3-ch4, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	45
Mean	50.38
Std Dev	2.652



# B1L003S, U3-ch4, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

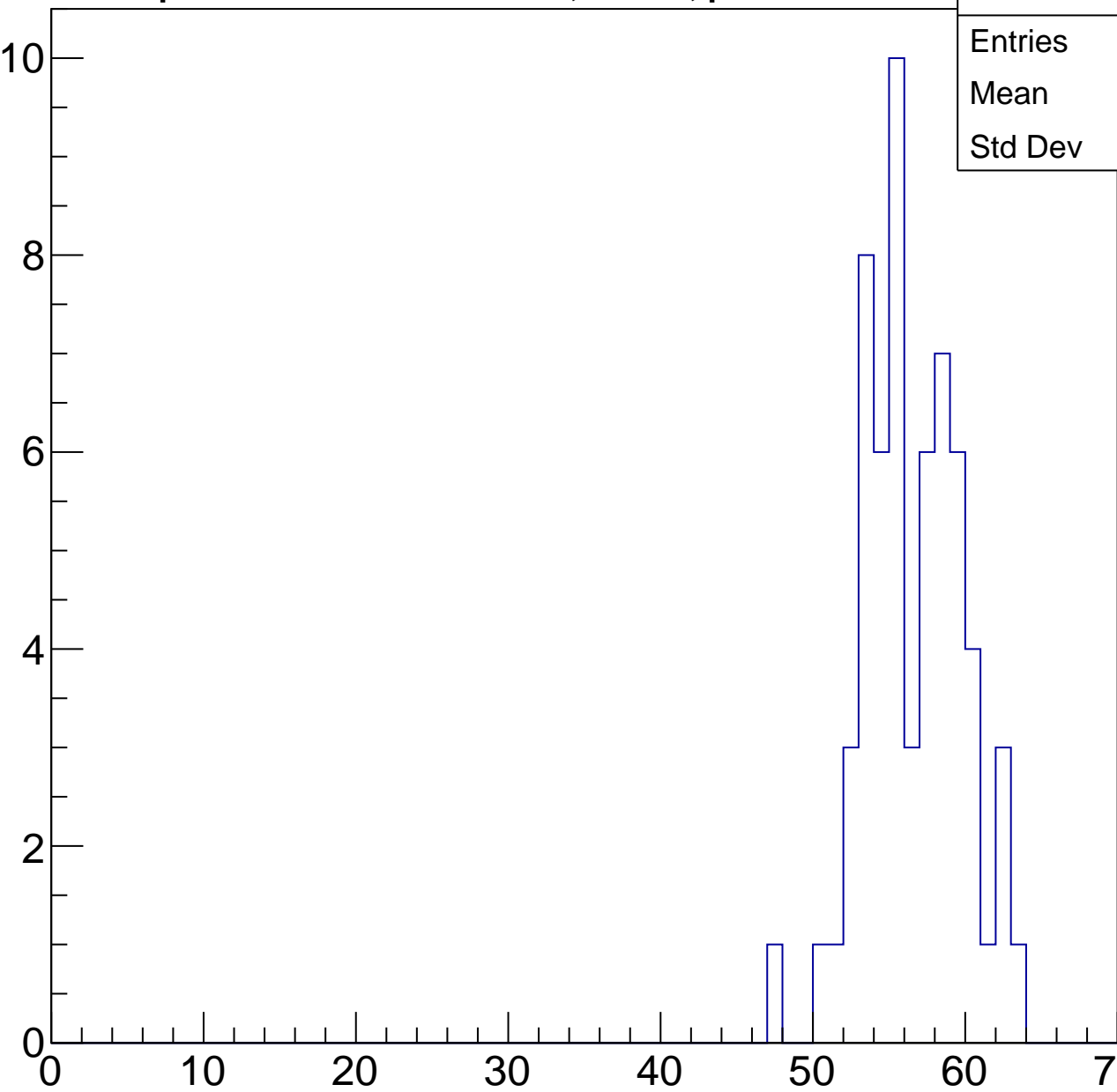
Entries	61
Mean	56.1
Std Dev	3.212

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

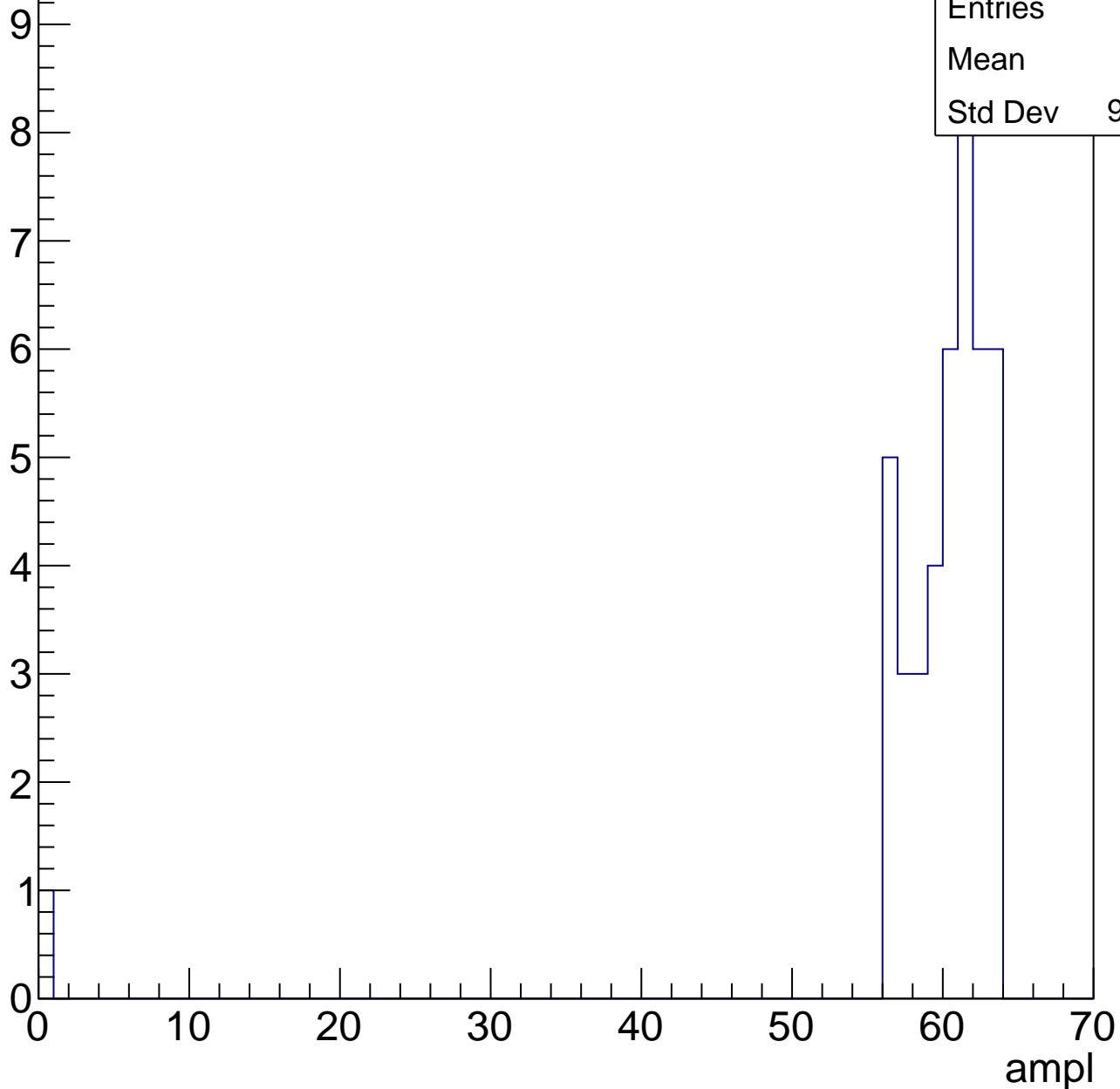
ampl



# B1L003S, U3-ch4, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U3-ch4, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch4, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U3-ch5, adc0

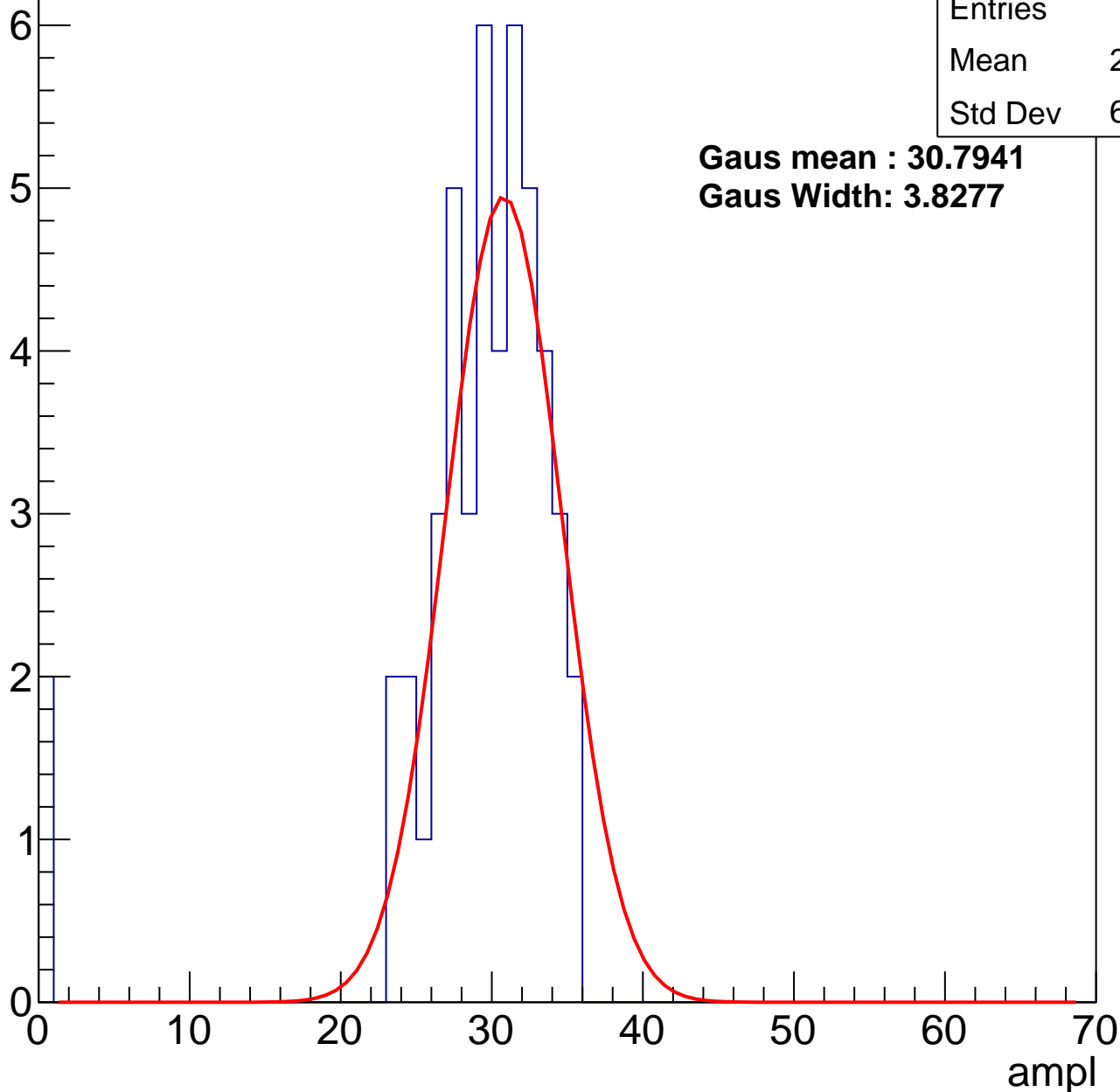
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	48
Mean	28.33
Std Dev	6.666

**Gaus mean : 30.7941**

**Gaus Width: 3.8277**



# B1L003S, U3-ch5, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	91
Mean	36.62
Std Dev	3.788

**Gaus mean : 37.1180**

**Gaus Width: 4.0126**

Entry

10

8

6

4

2

0

0

10

20

30

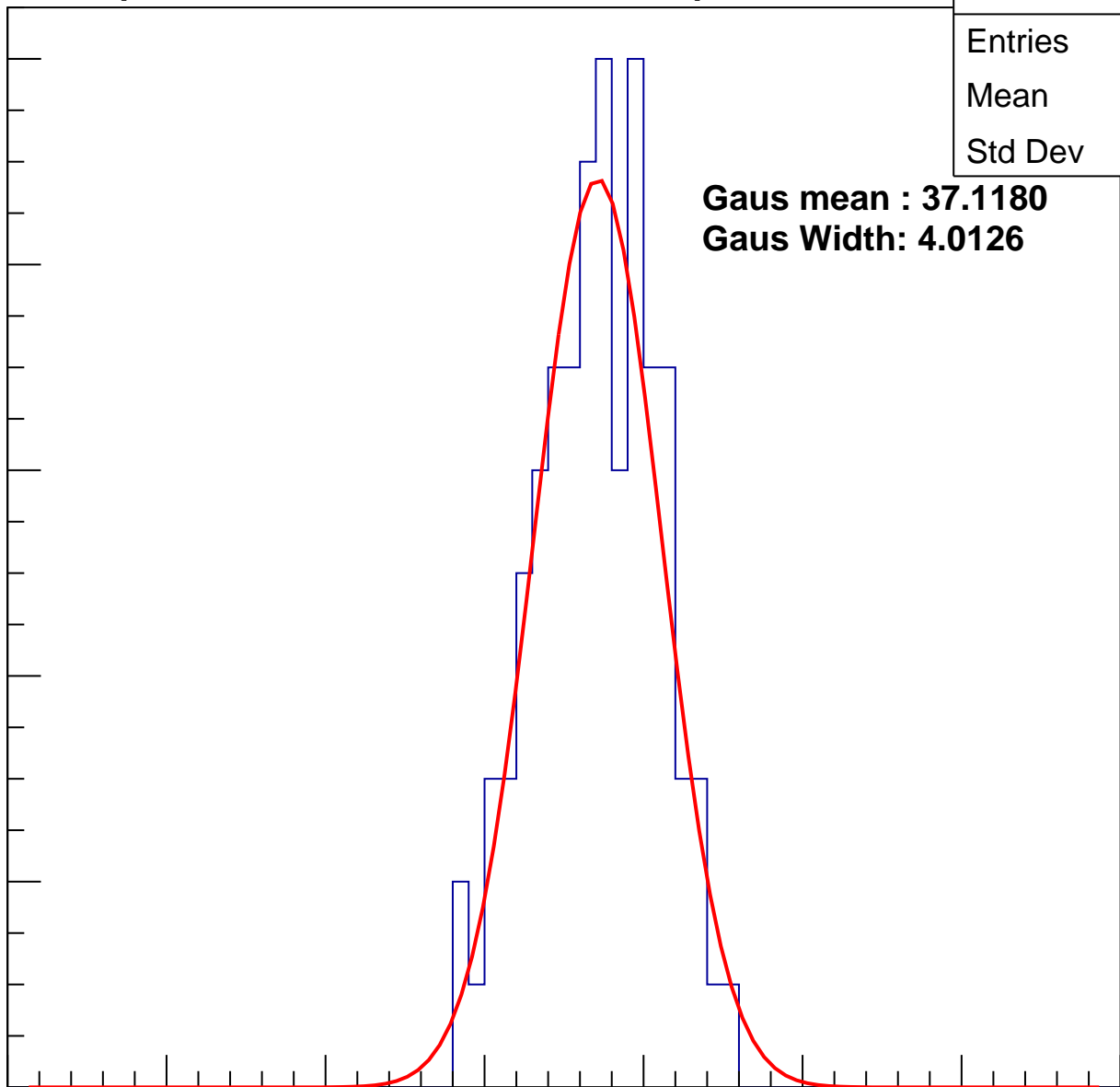
40

50

60

70

ampl



# B1L003S, U3-ch5, adc2

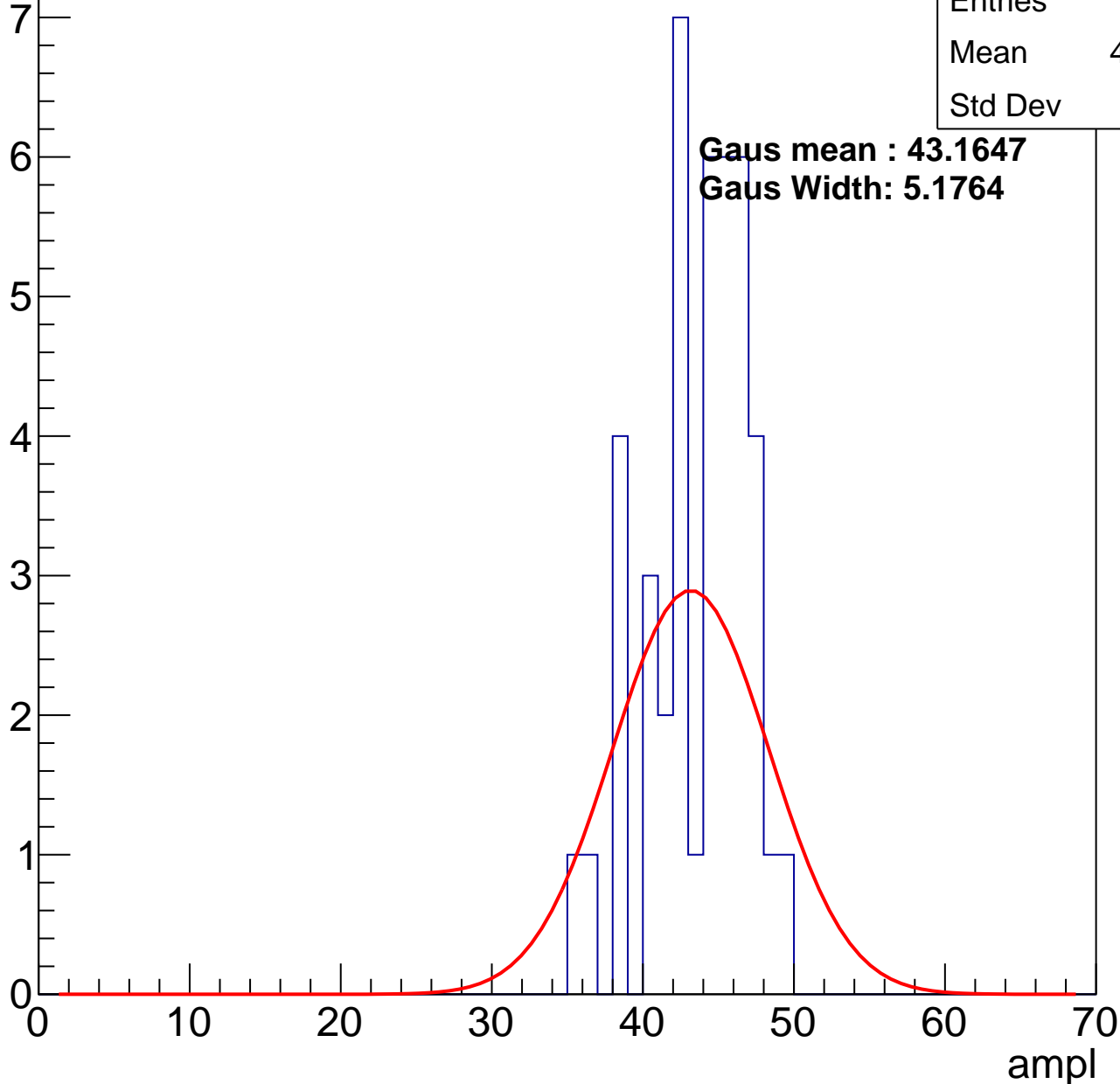
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	43
Mean	43.19
Std Dev	3.28

**Gaus mean : 43.1647**

**Gaus Width: 5.1764**

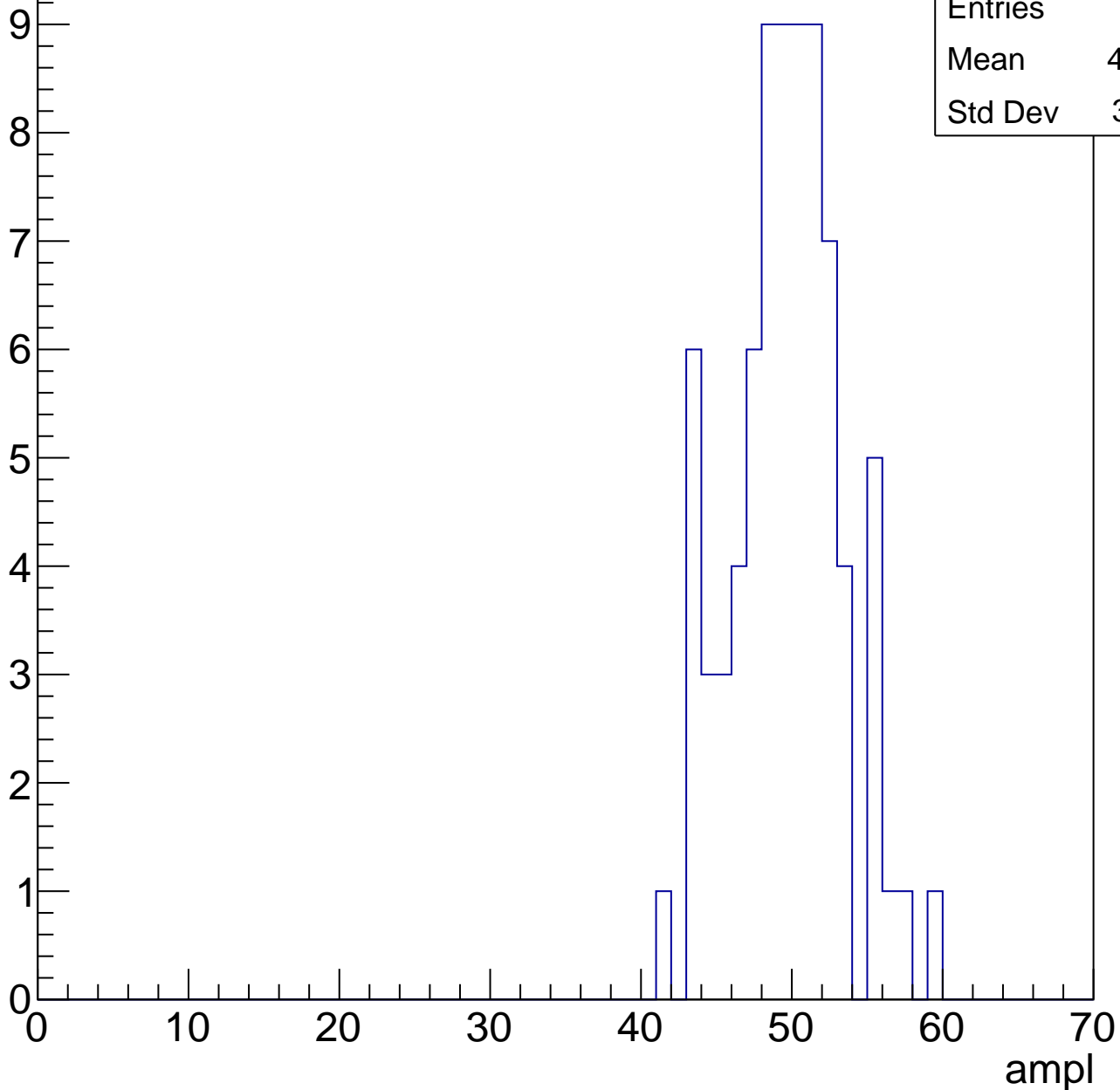


# B1L003S, U3-ch5, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	78
Mean	49.19
Std Dev	3.641



# B1L003S, U3-ch5, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	67
Mean	56.54
Std Dev	2.994

Entry

10

8

6

4

2

0

0

10

20

30

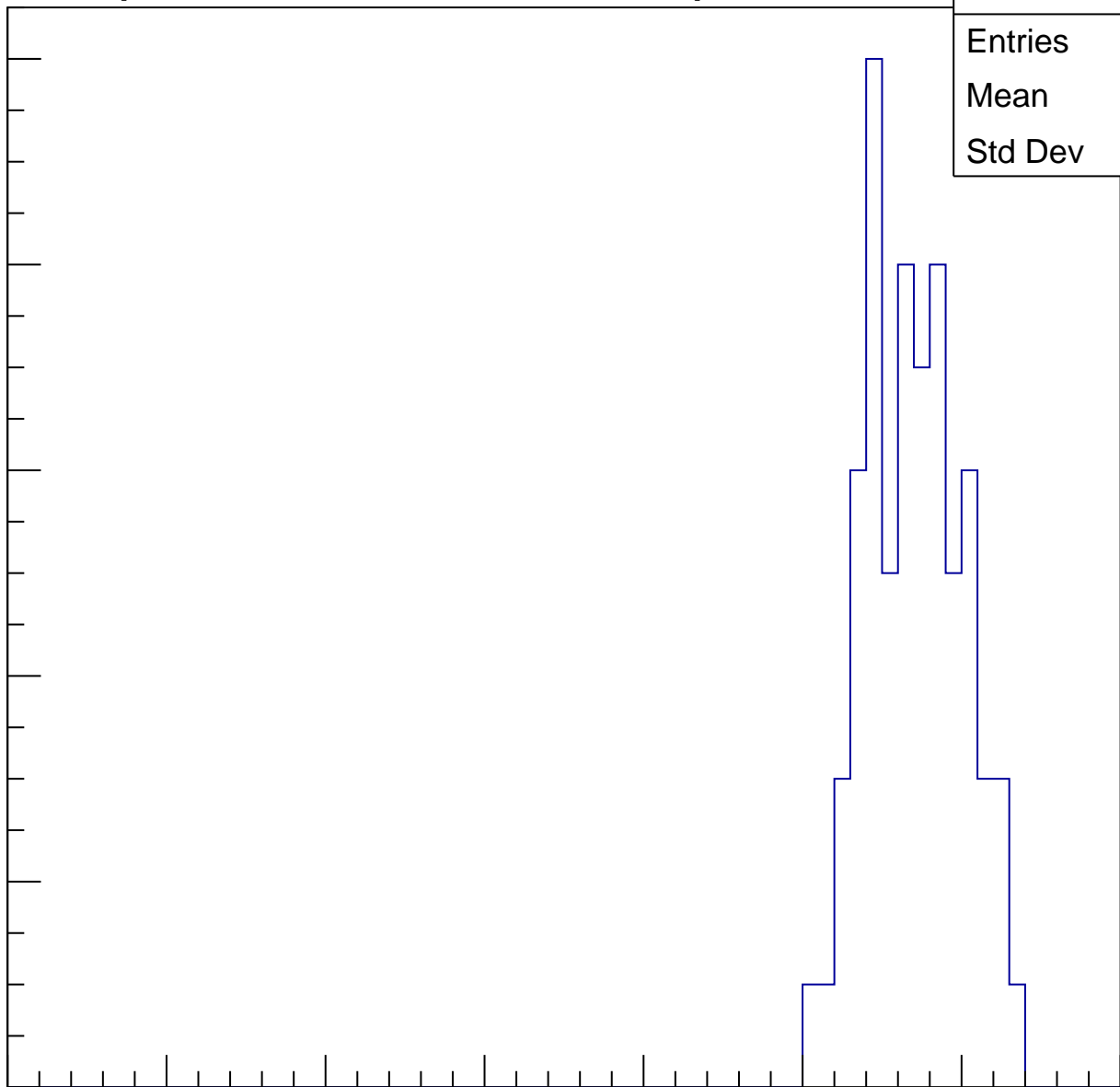
40

50

60

70

ampl

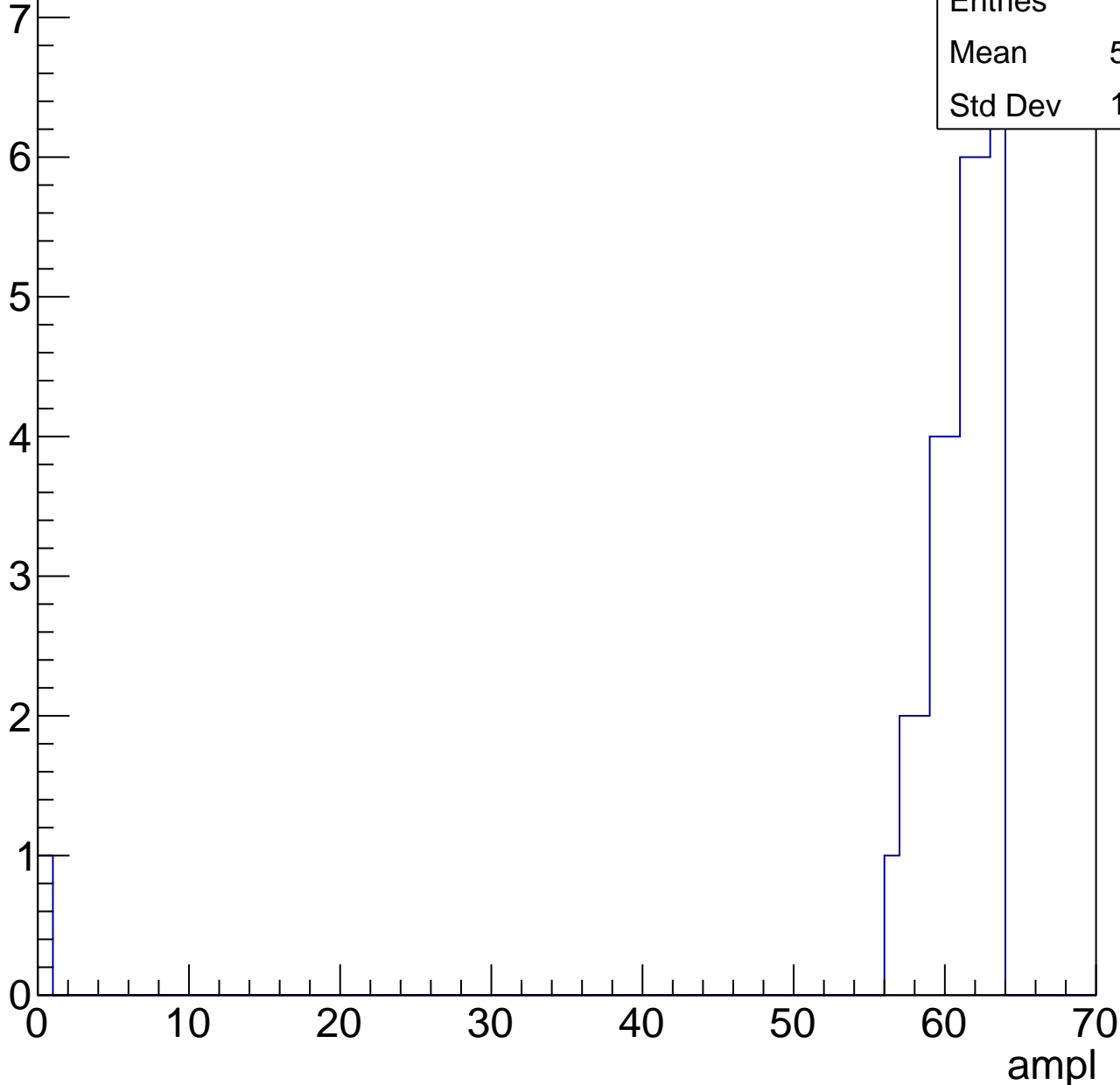


# B1L003S, U3-ch5, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	33
Mean	58.82
Std Dev	10.58



# B1L003S, U3-ch5, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch5, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U3-ch6, adc0

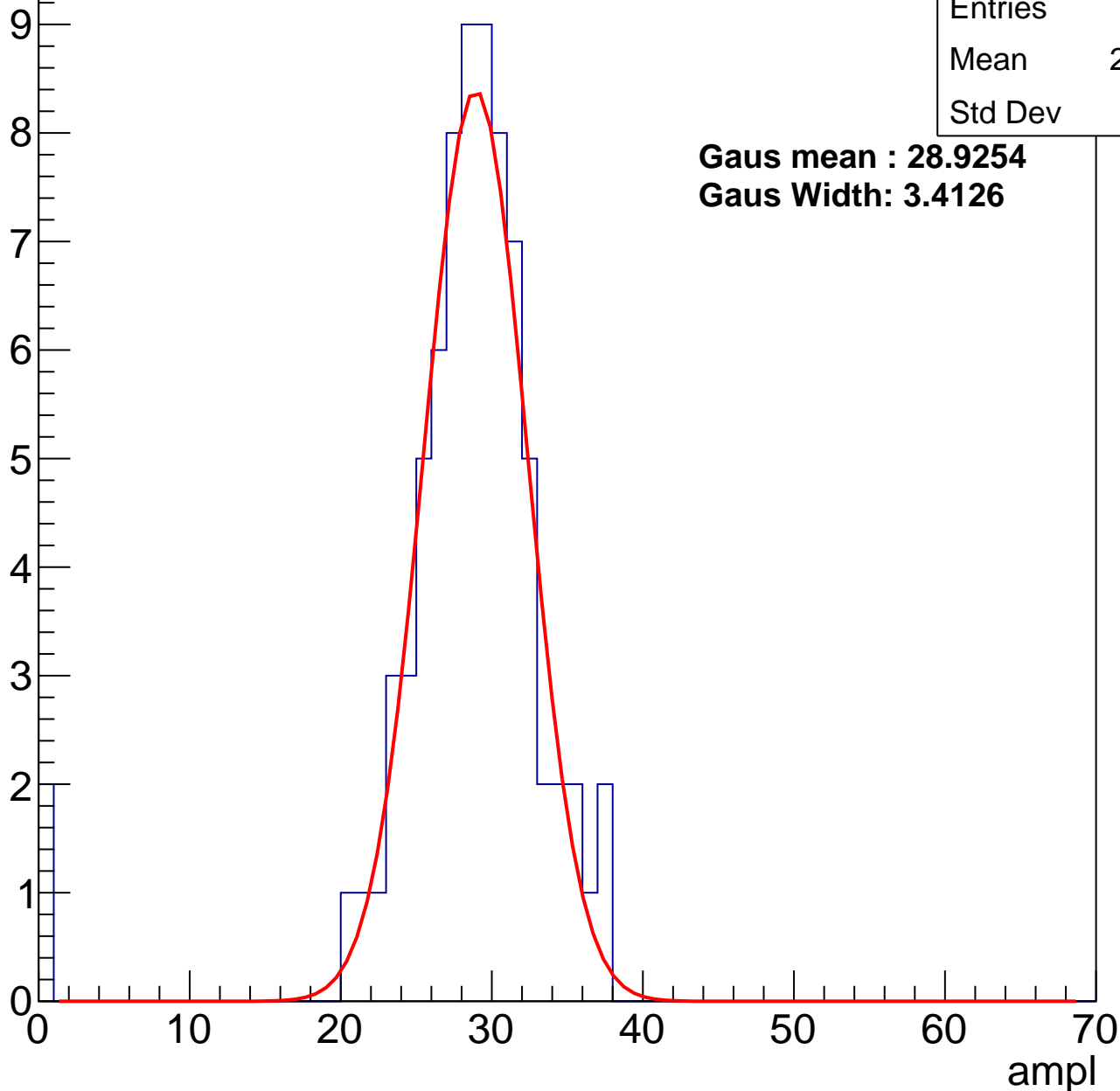
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	77
Mean	27.86
Std Dev	5.75

**Gaus mean : 28.9254**

**Gaus Width: 3.4126**



# B1L003S, U3-ch6, adc1

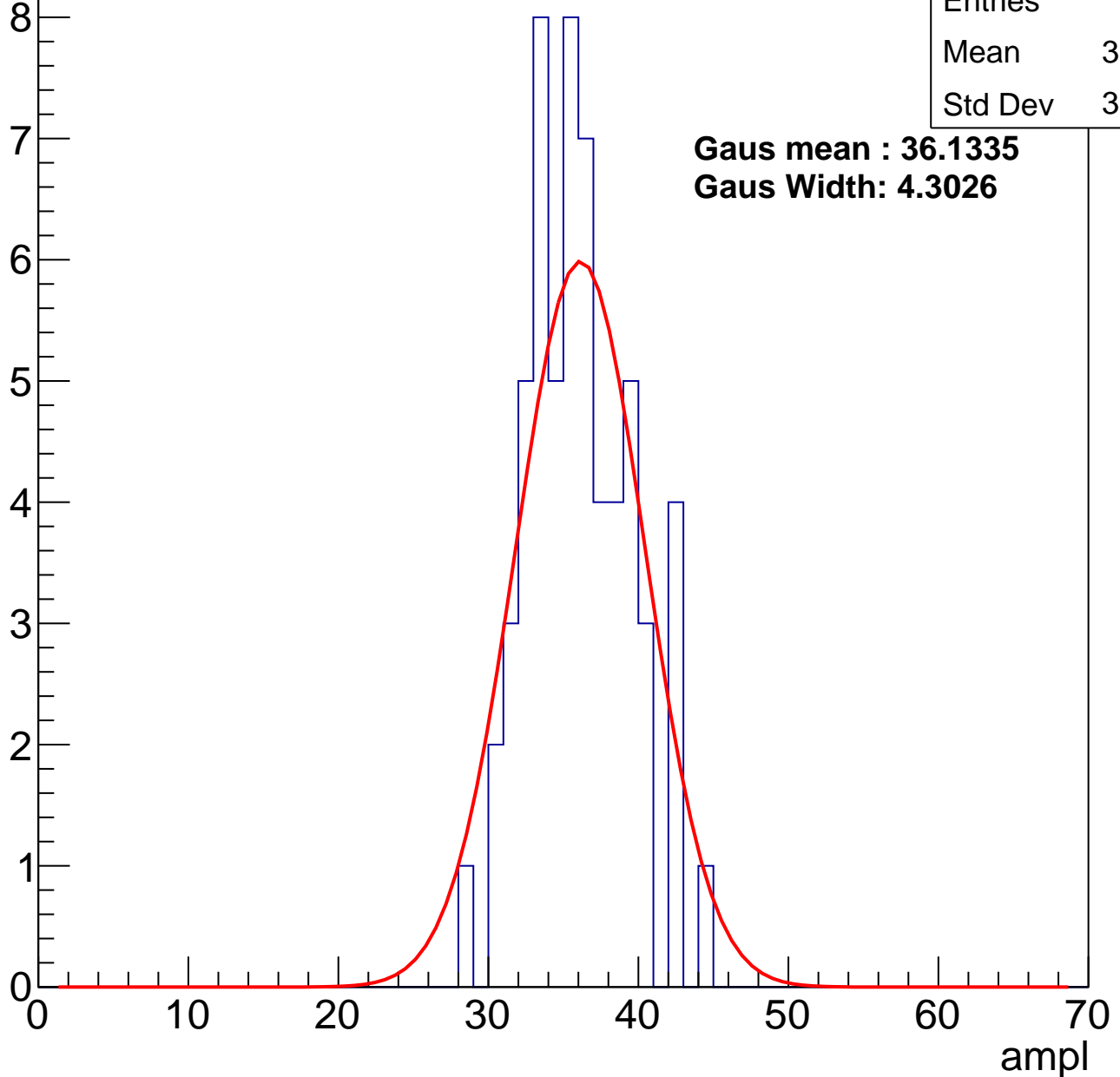
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	35.57
Std Dev	3.417

**Gaus mean : 36.1335**

**Gaus Width: 4.3026**



# B1L003S, U3-ch6, adc2

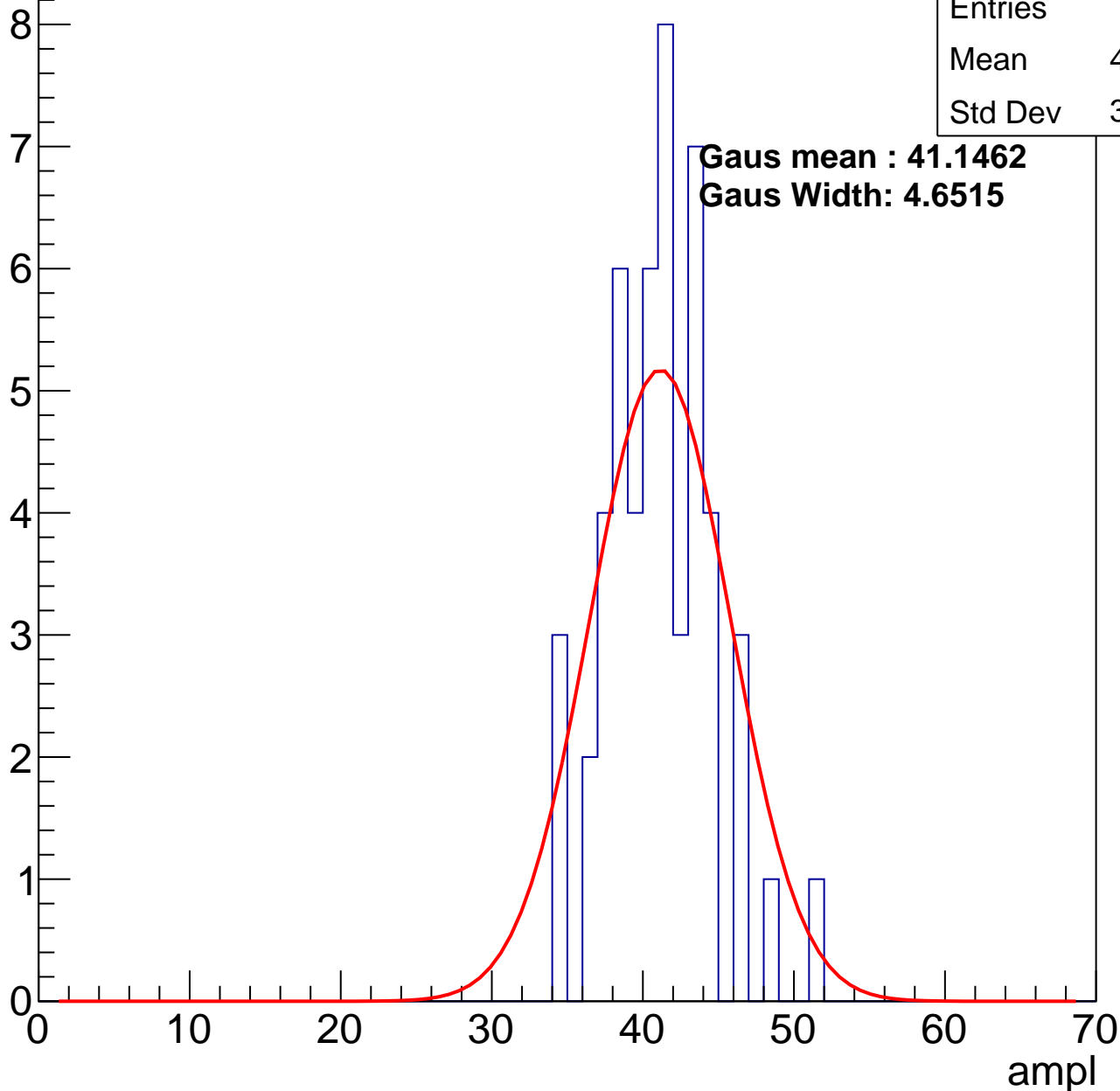
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	52
Mean	40.65
Std Dev	3.458

**Gaus mean : 41.1462**

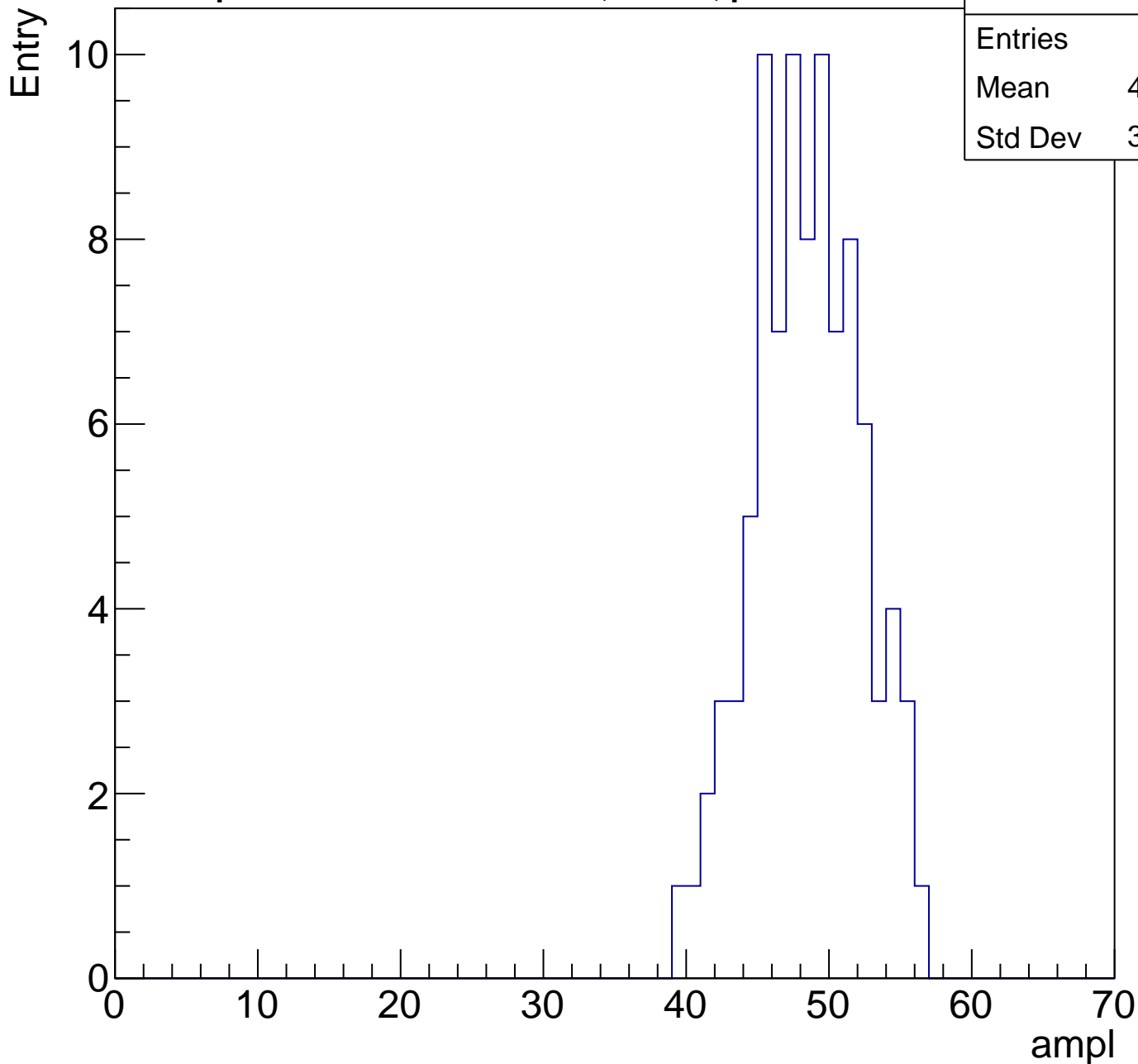
**Gaus Width: 4.6515**



# B1L003S, U3-ch6, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	92
Mean	48.02
Std Dev	3.715

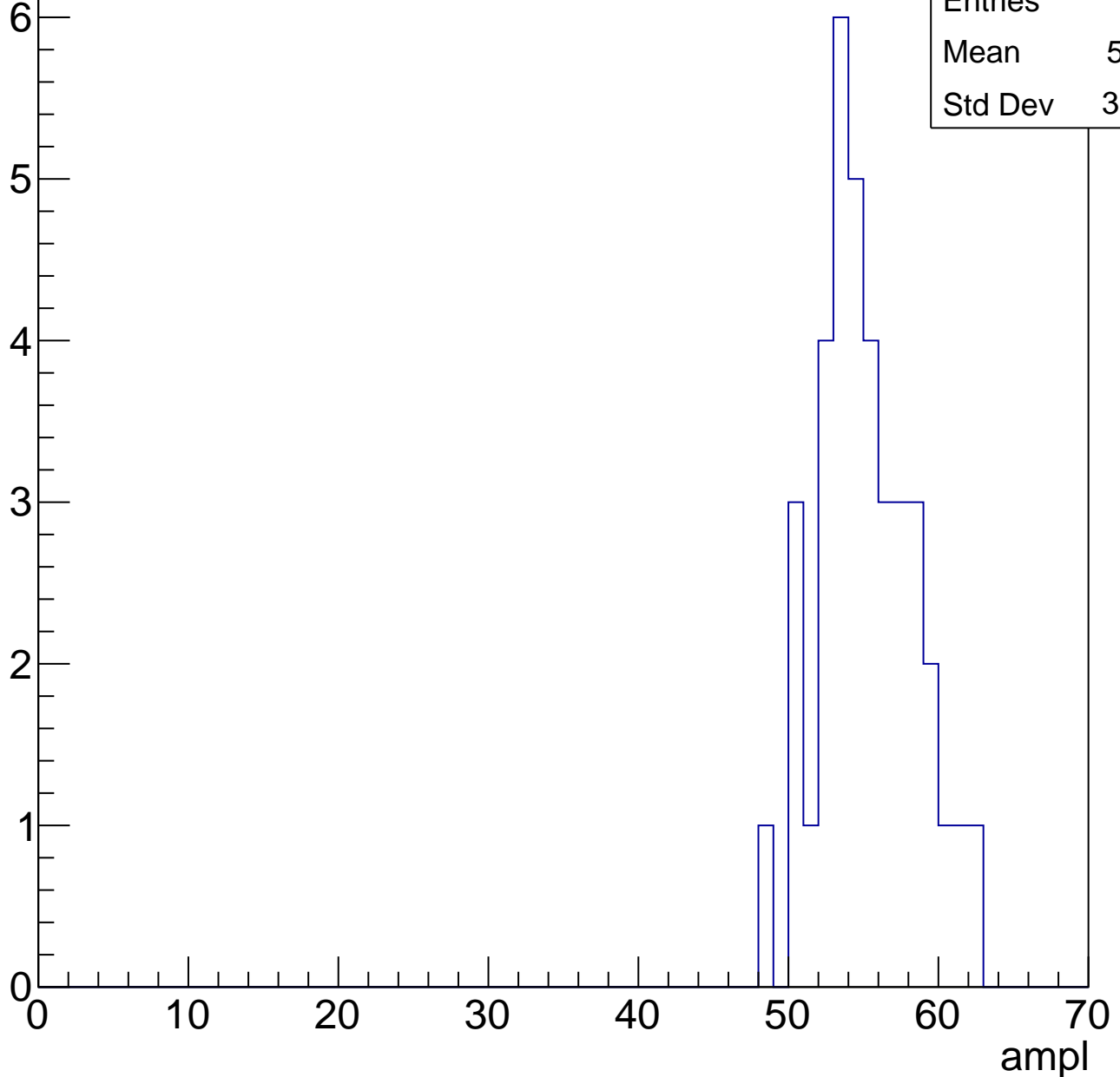


# B1L003S, U3-ch6, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	38
Mean	54.71
Std Dev	3.186

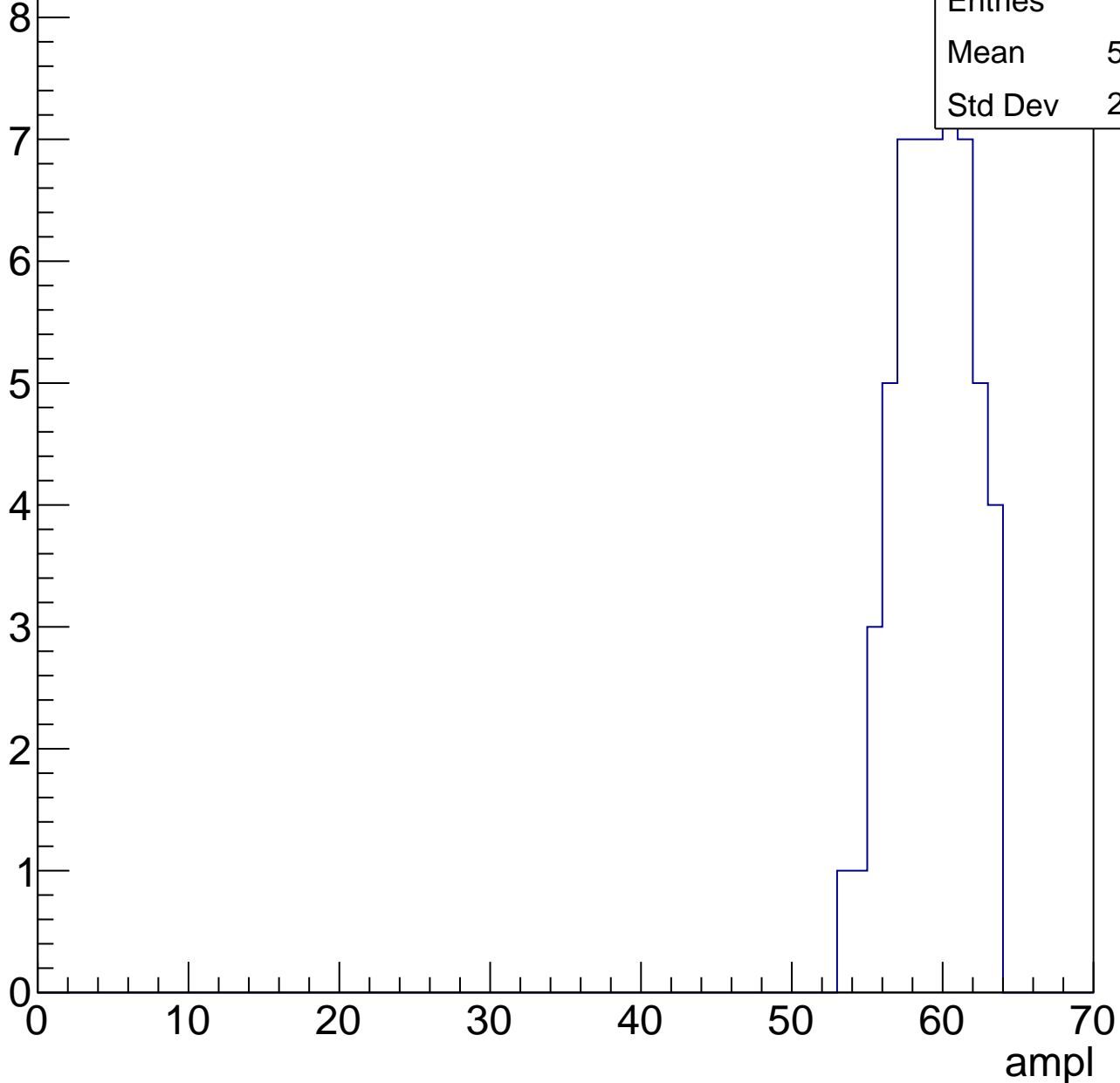


# B1L003S, U3-ch6, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	58.89
Std Dev	2.462

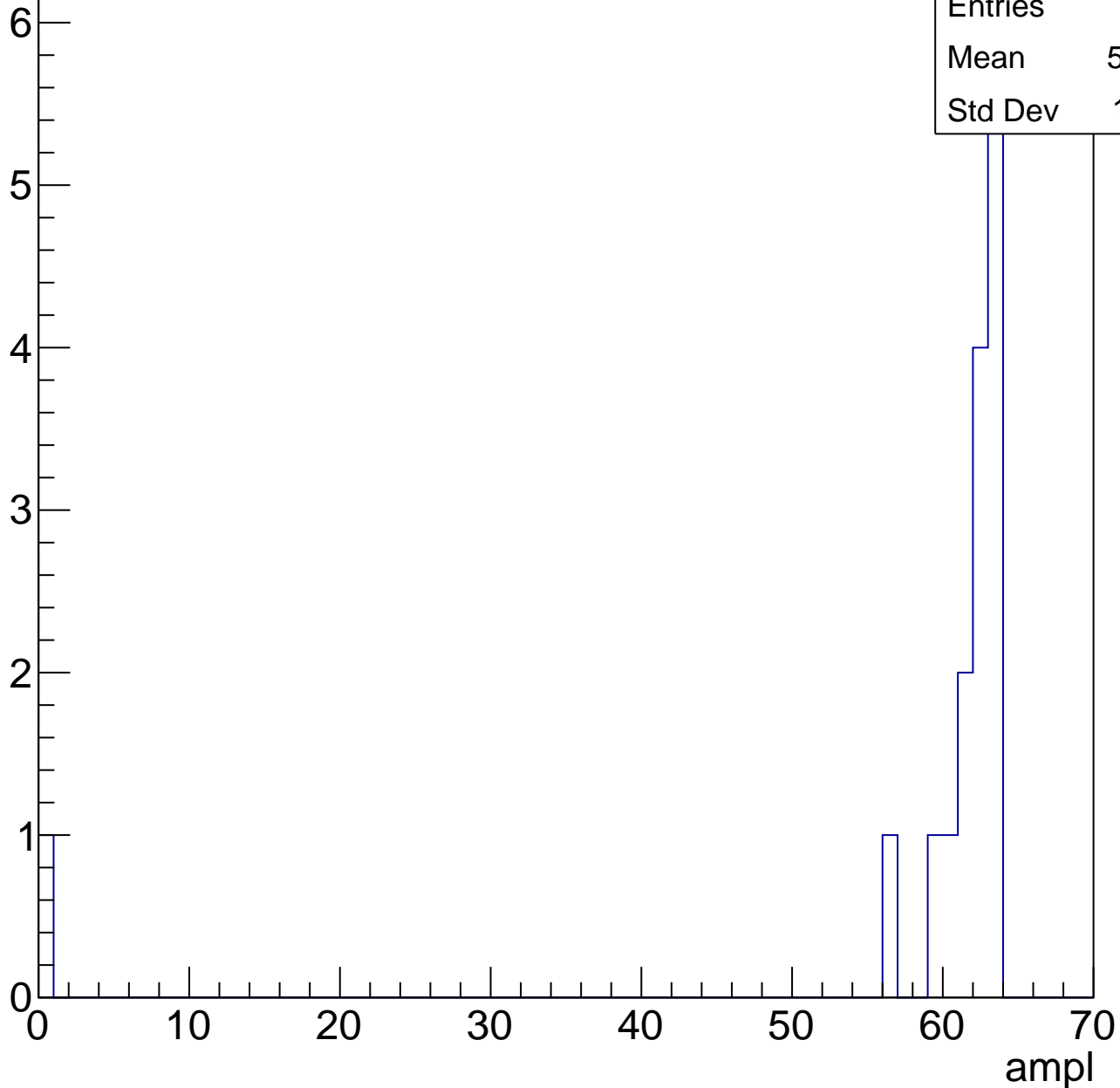


# B1L003S, U3-ch6, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	16
Mean	57.69
Std Dev	15.01





# B1L003S, U3-ch6, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L003S, U3-ch7, adc0

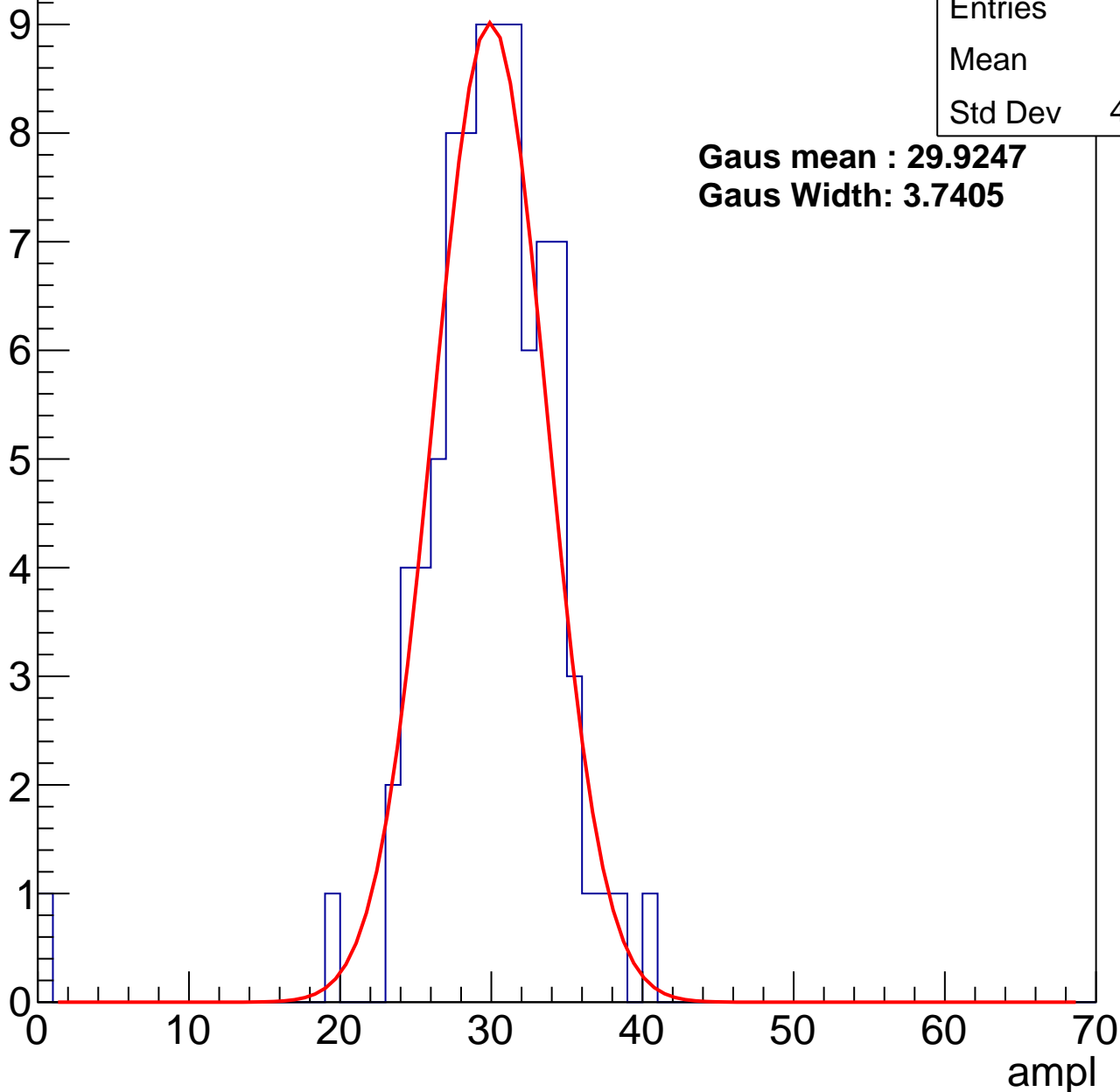
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	87
Mean	29.4
Std Dev	4.862

**Gaus mean : 29.9247**

**Gaus Width: 3.7405**



# B1L003S, U3-ch7, adc1

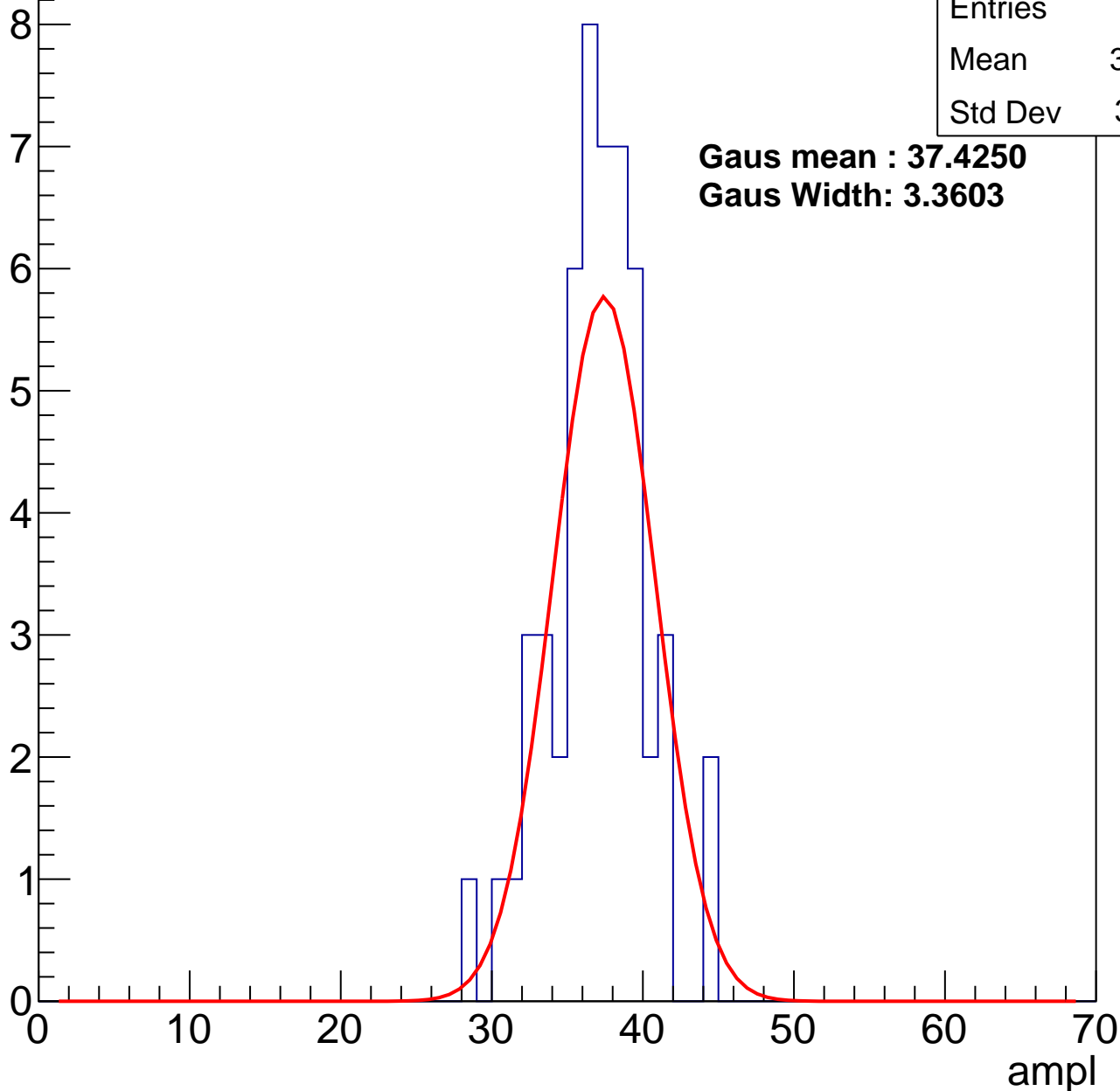
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	52
Mean	36.54
Std Dev	3.171

**Gaus mean : 37.4250**

**Gaus Width: 3.3603**



# B1L003S, U3-ch7, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	72
Mean	42.49
Std Dev	3.551

**Gaus mean : 43.1924**

**Gaus Width: 3.3228**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

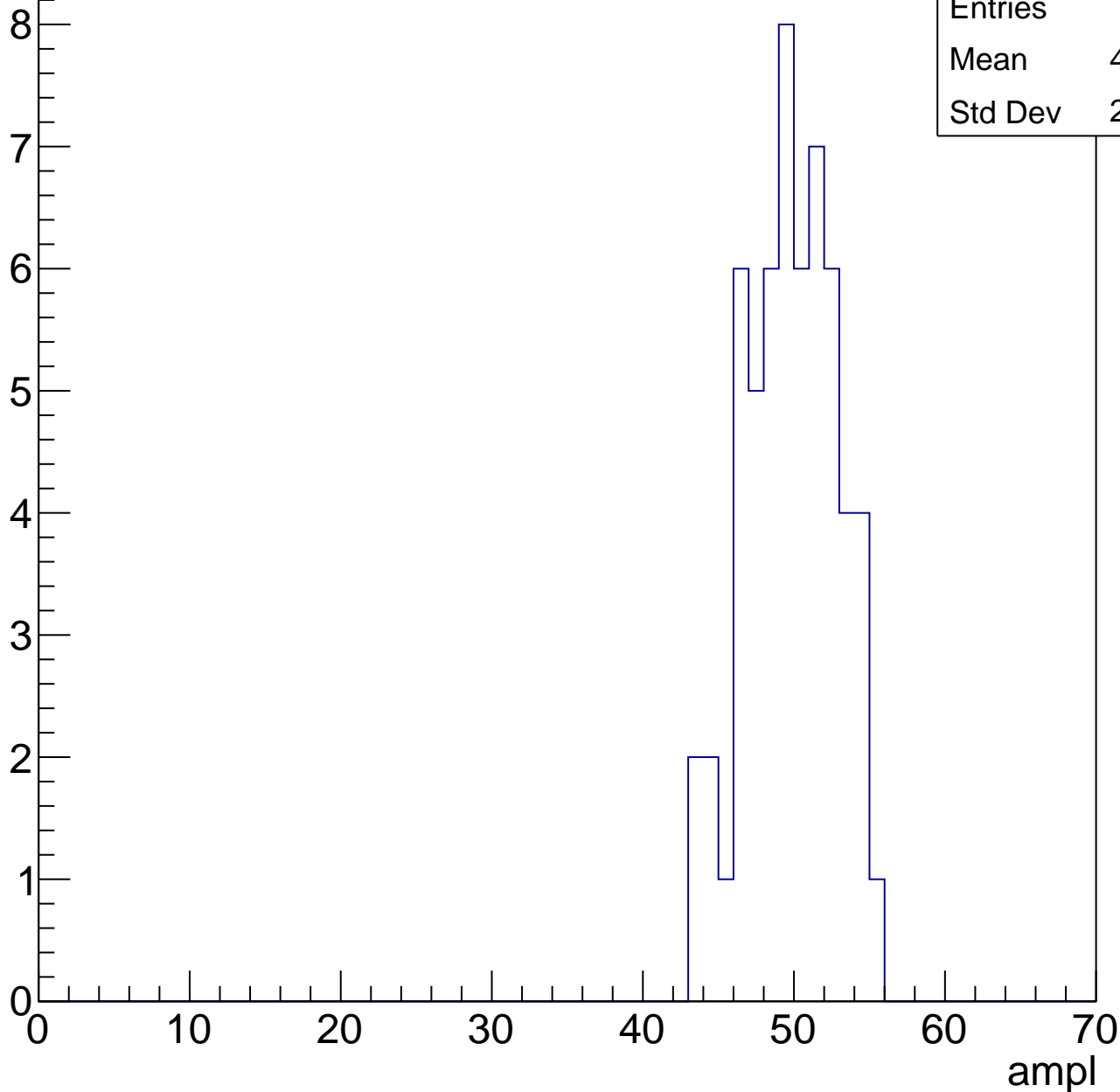


# B1L003S, U3-ch7, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	49.34
Std Dev	2.933

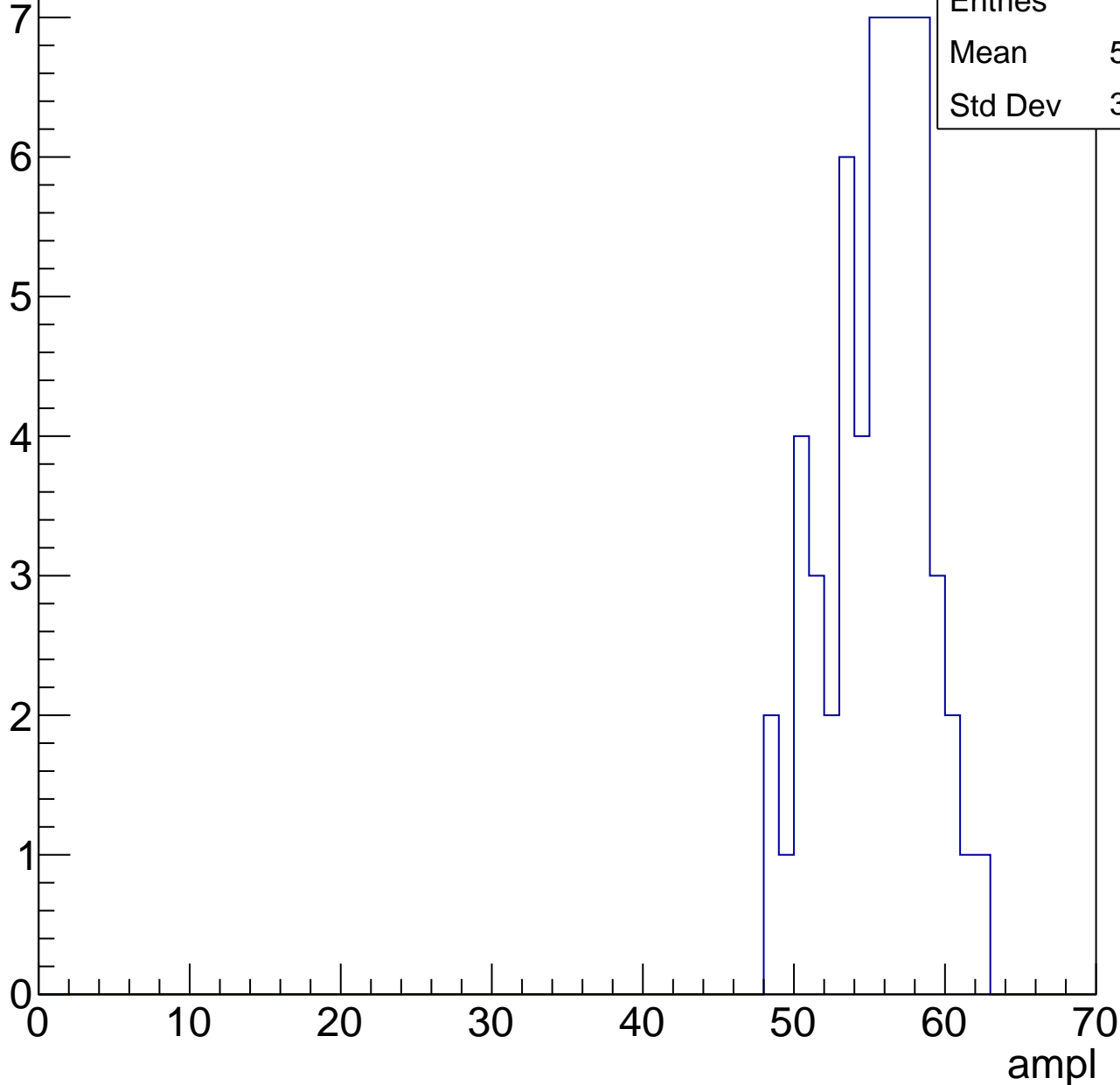


# B1L003S, U3-ch7, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	55.05
Std Dev	3.268

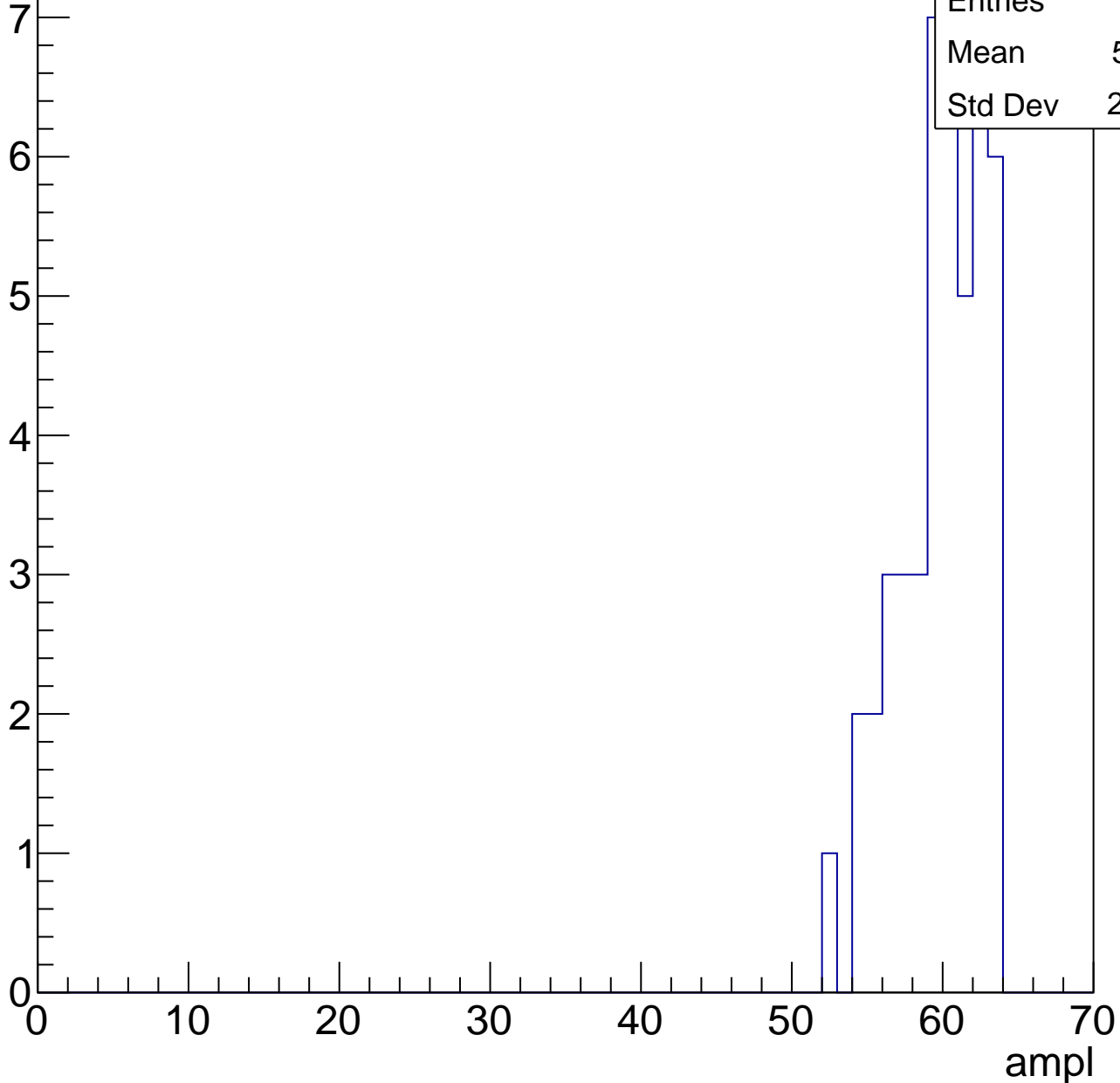


# B1L003S, U3-ch7, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

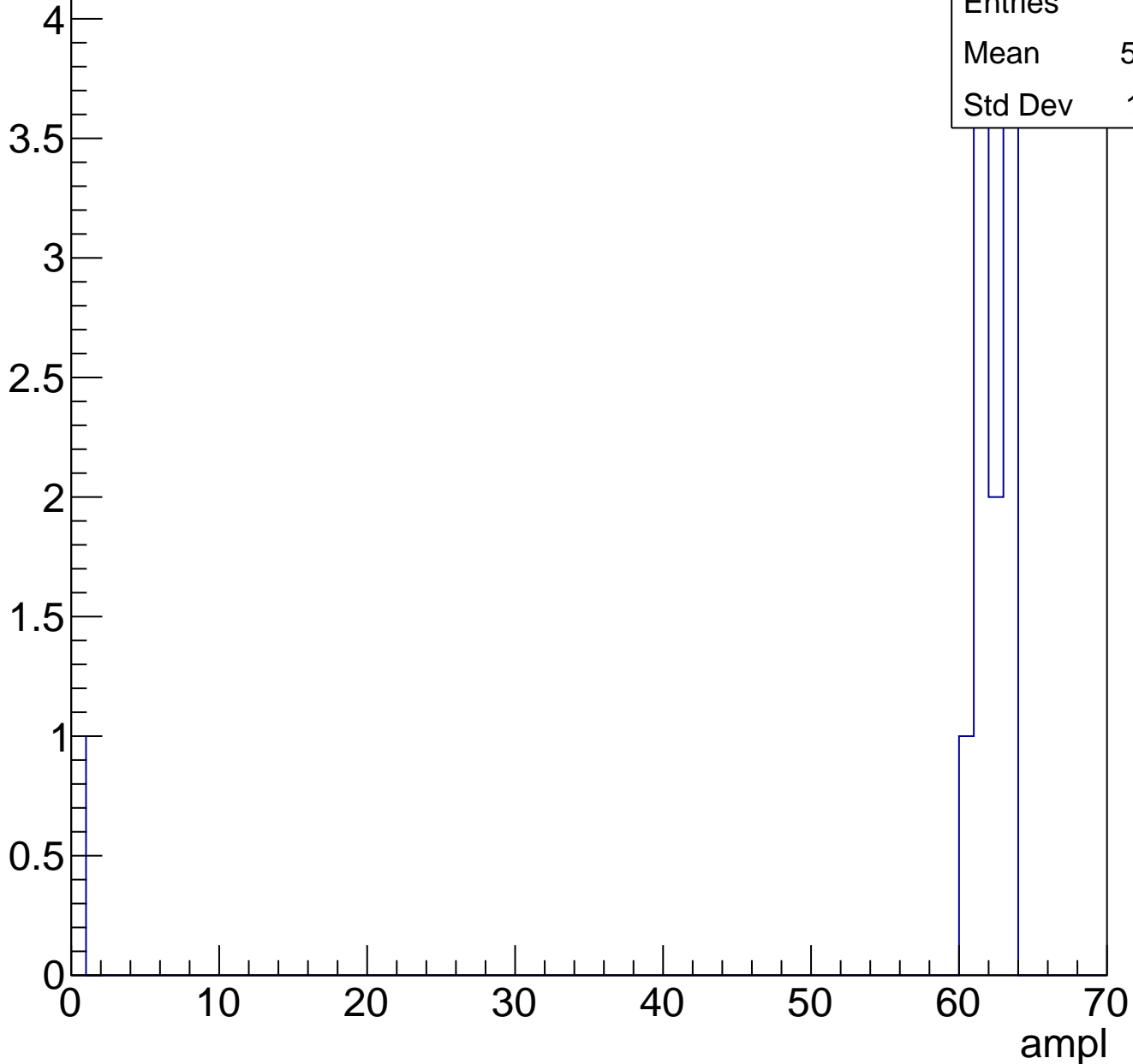
Entries	46
Mean	59.41
Std Dev	2.763



# B1L003S, U3-ch7, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch7, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L003S, U3-ch8, adc0

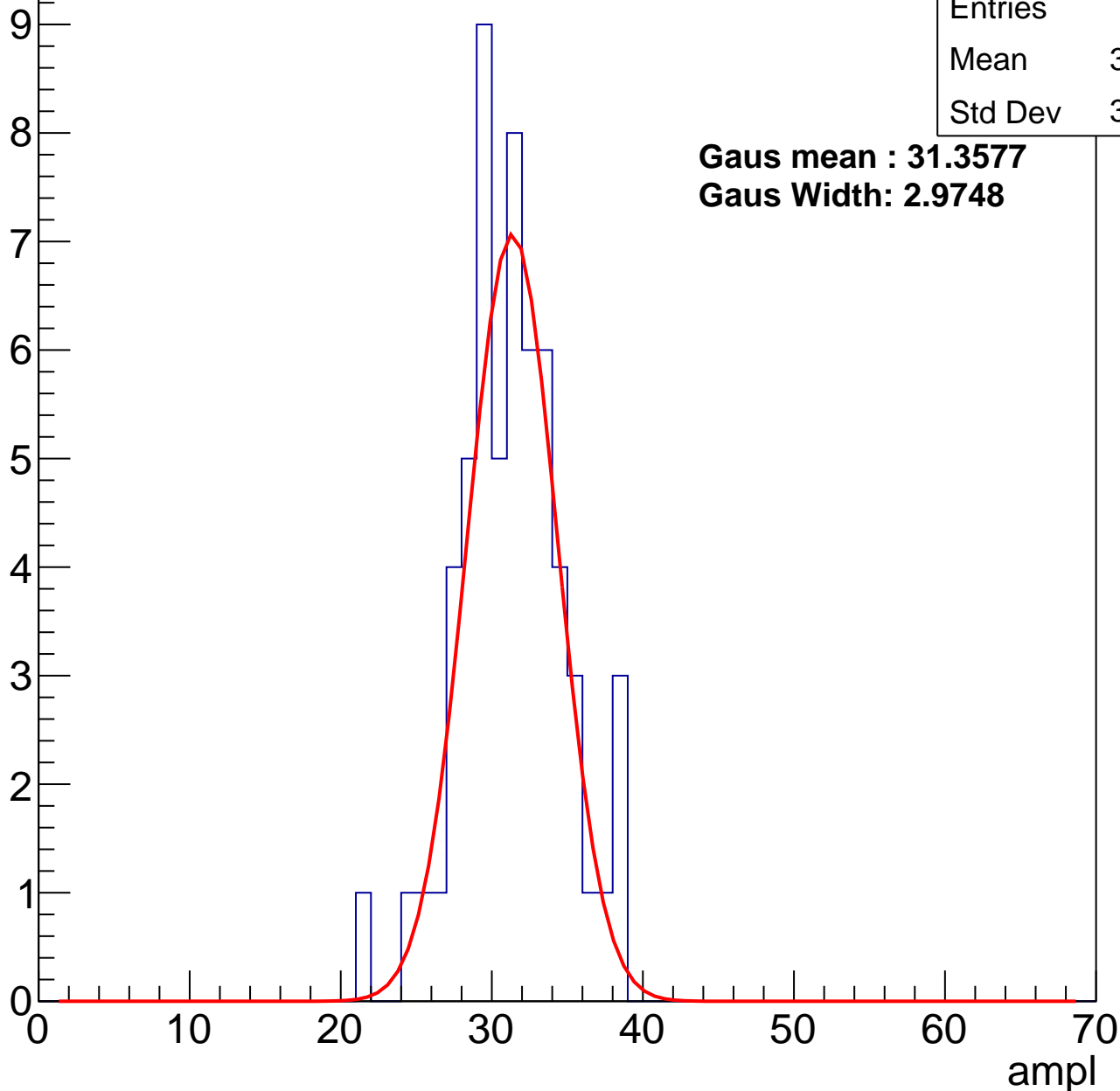
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	30.86
Std Dev	3.397

**Gaus mean : 31.3577**

**Gaus Width: 2.9748**



# B1L003S, U3-ch8, adc1

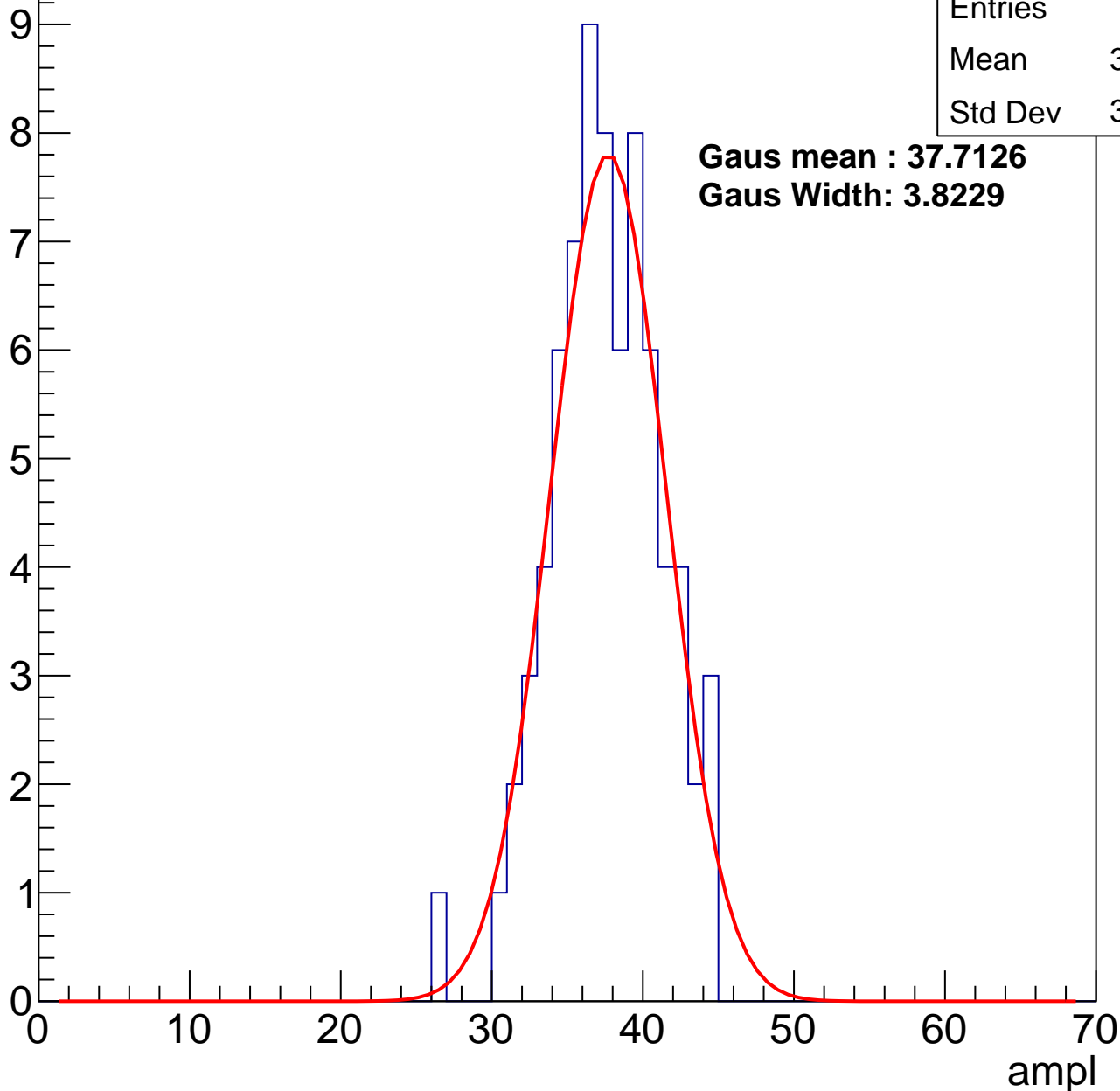
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	74
Mean	37.09
Std Dev	3.576

**Gaus mean : 37.7126**

**Gaus Width: 3.8229**



# B1L003S, U3-ch8, adc2

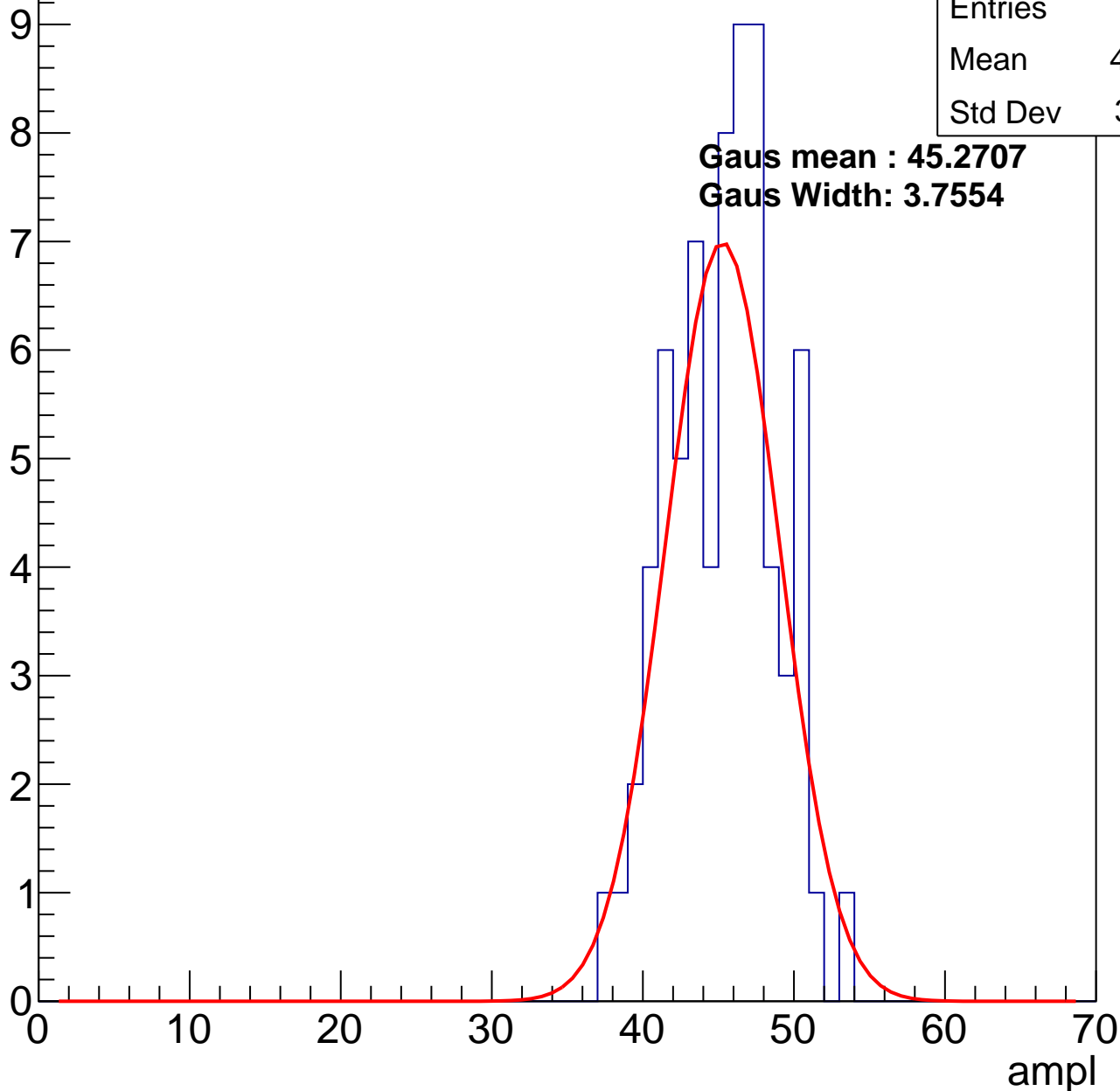
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	71
Mean	44.87
Std Dev	3.431

**Gaus mean : 45.2707**

**Gaus Width: 3.7554**

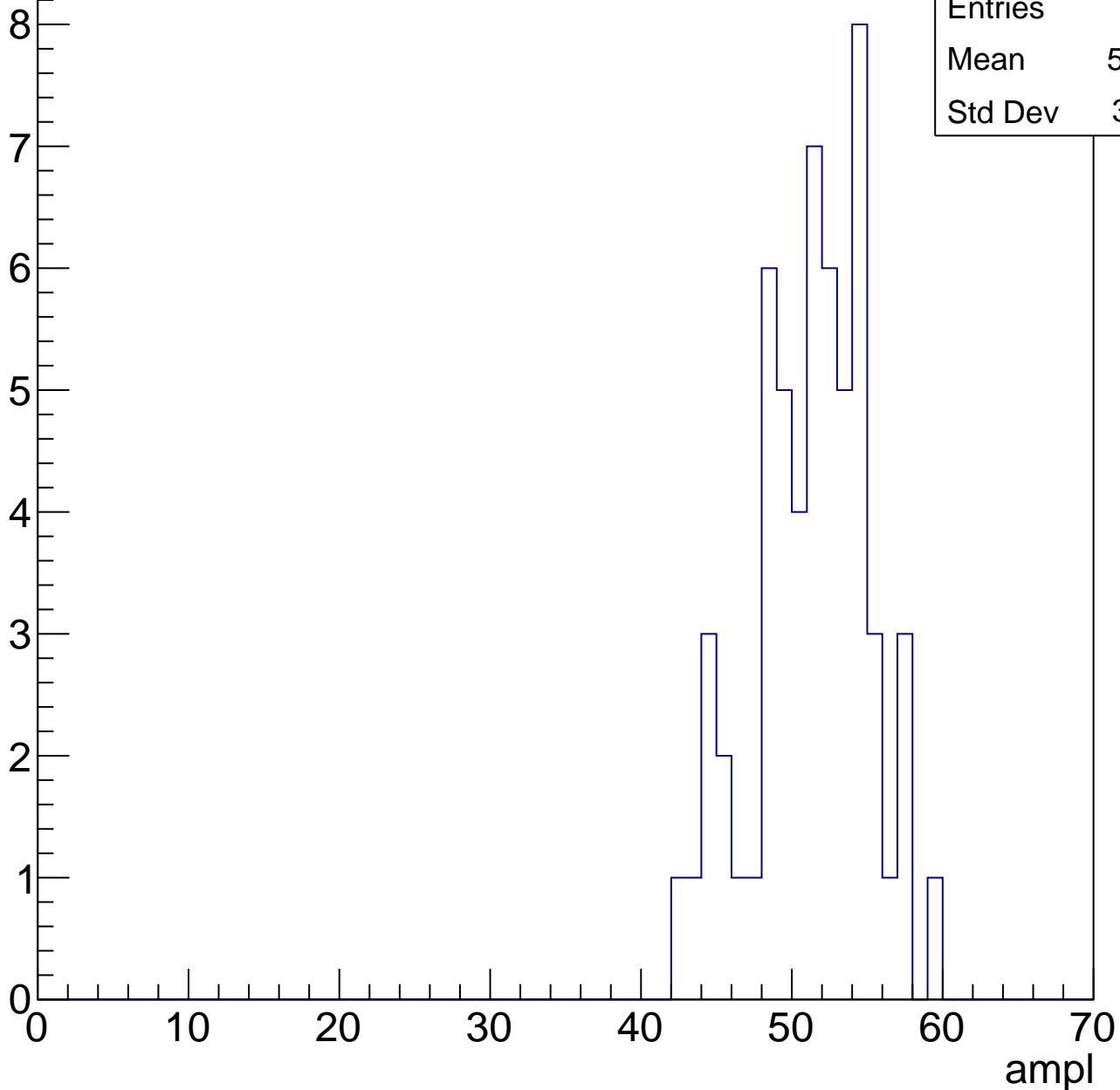


# B1L003S, U3-ch8, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	50.86
Std Dev	3.771

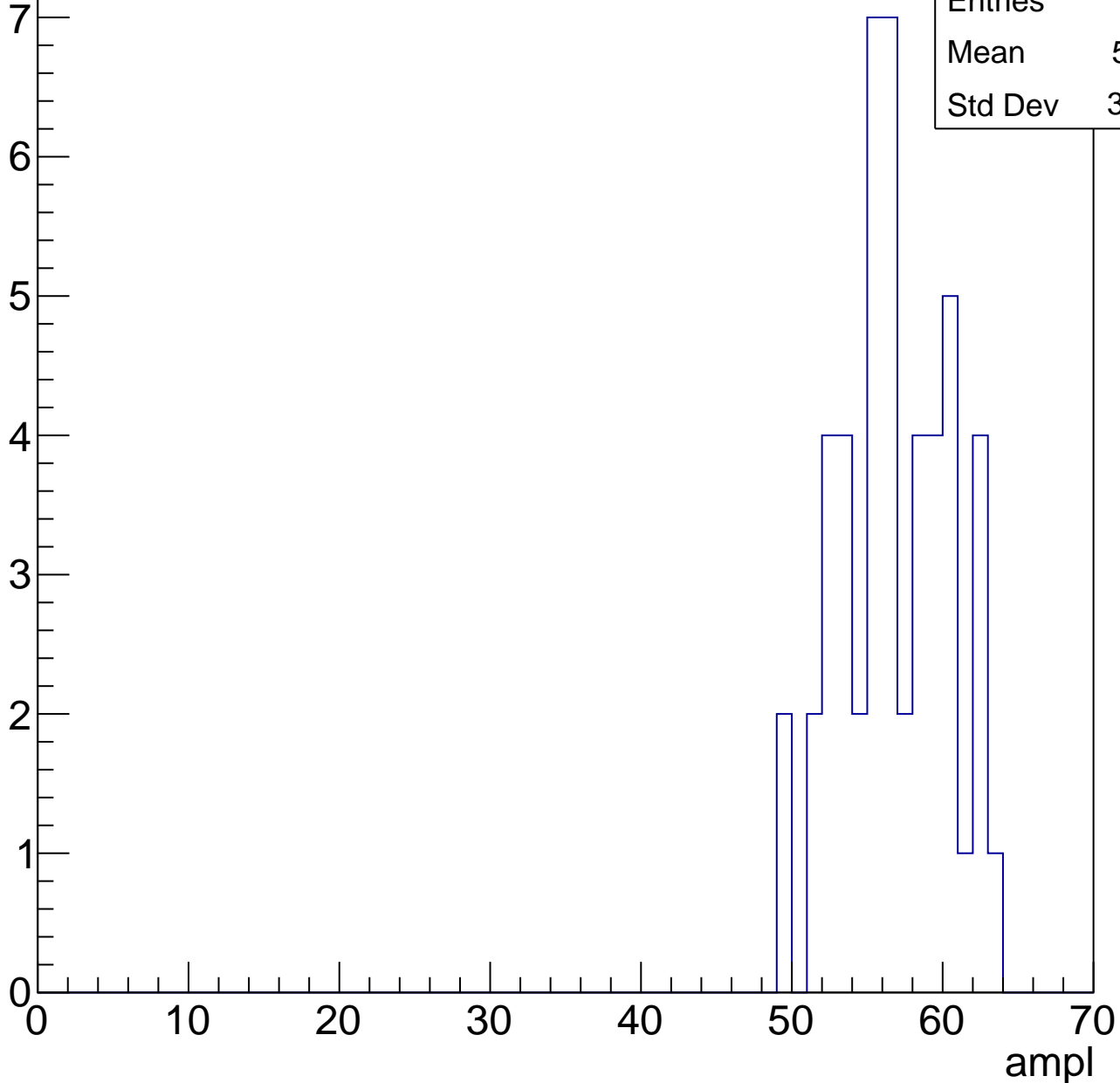


# B1L003S, U3-ch8, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	49
Mean	56.31
Std Dev	3.529

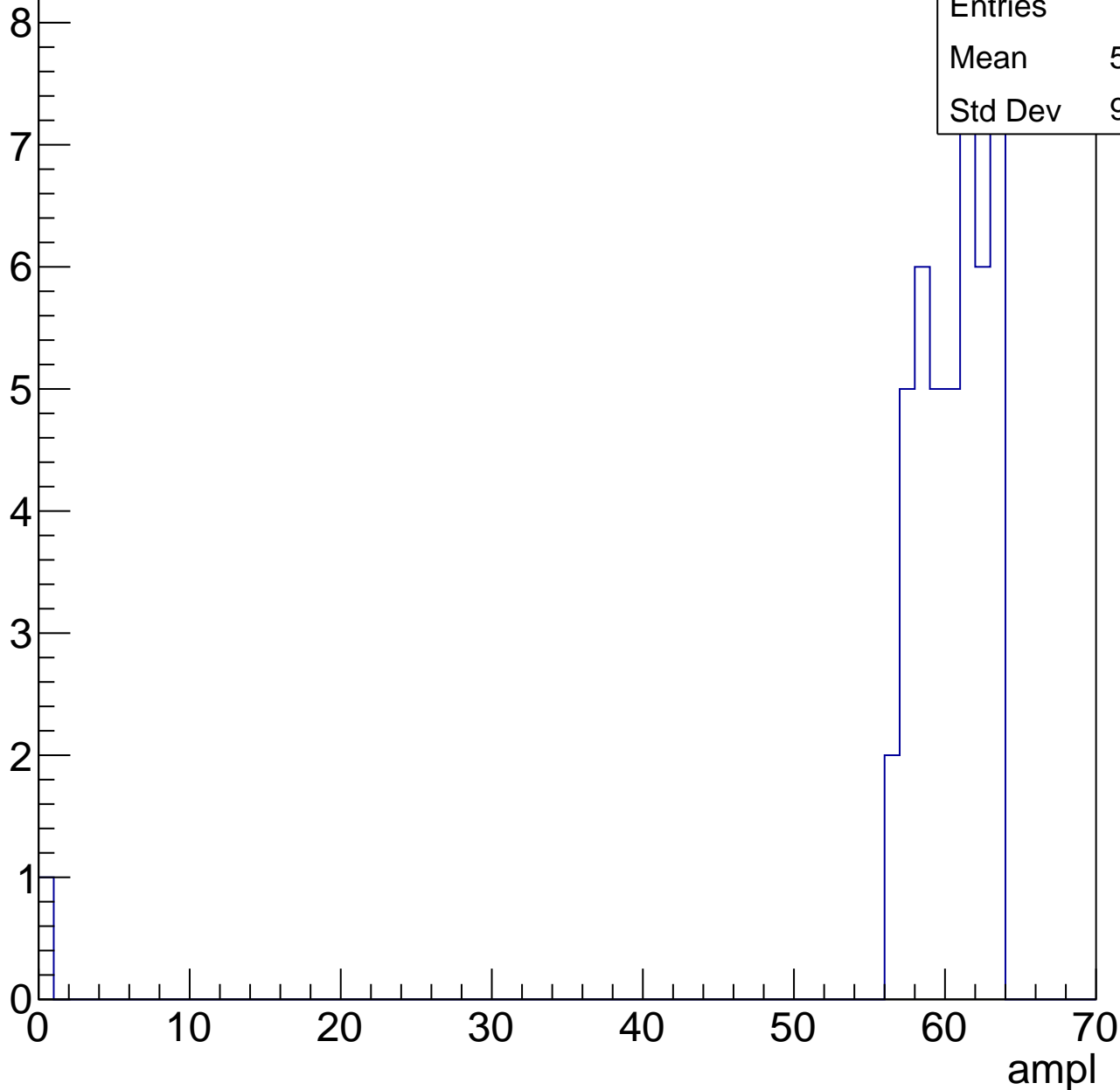


# B1L003S, U3-ch8, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	46
Mean	58.78
Std Dev	9.019



# B1L003S, U3-ch8, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch8, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U3-ch9, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	89
Mean	29.12
Std Dev	4.635

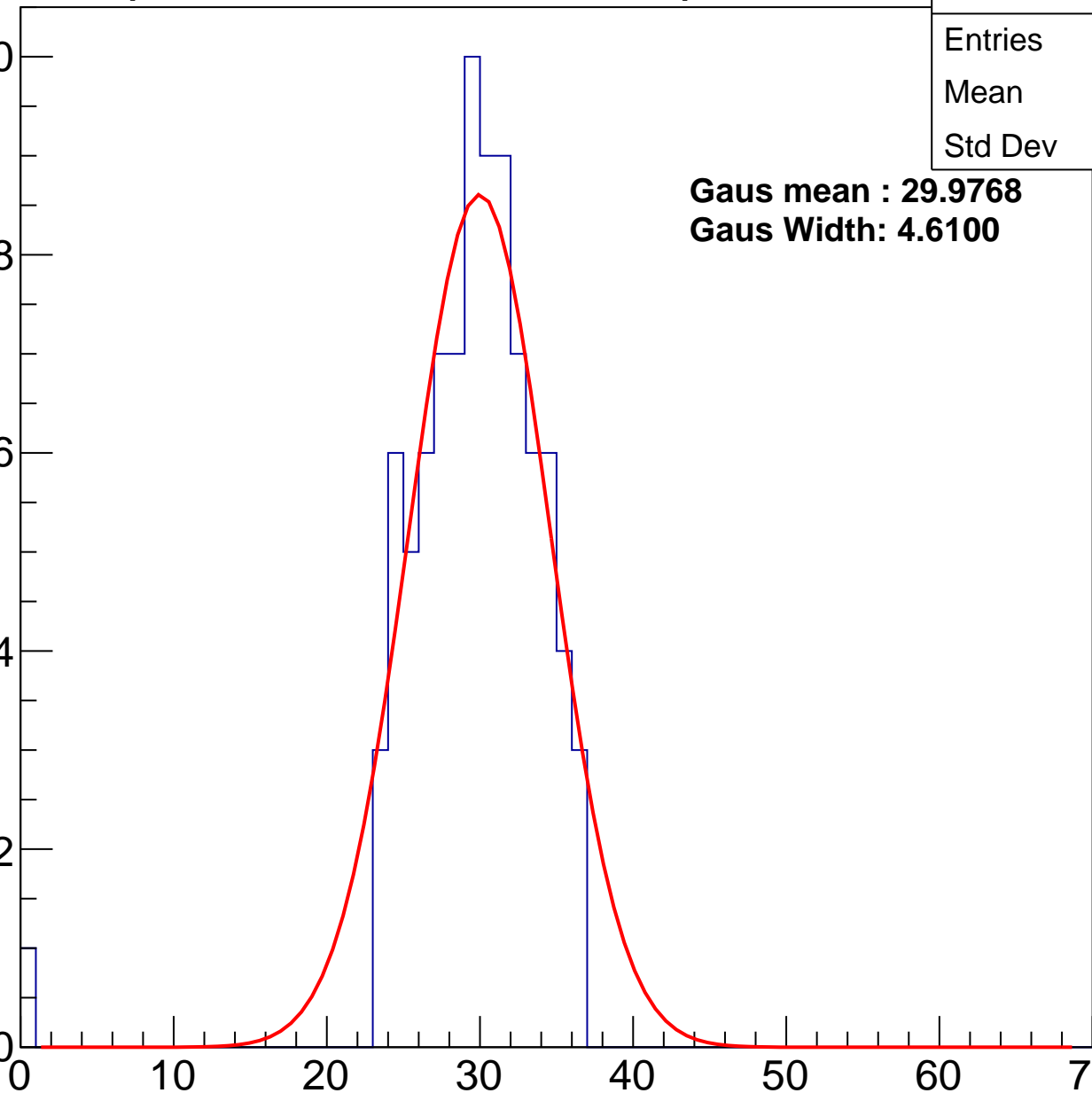
**Gaus mean : 29.9768**

**Gaus Width: 4.6100**

Entry

10  
8  
6  
4  
2  
0

ampl



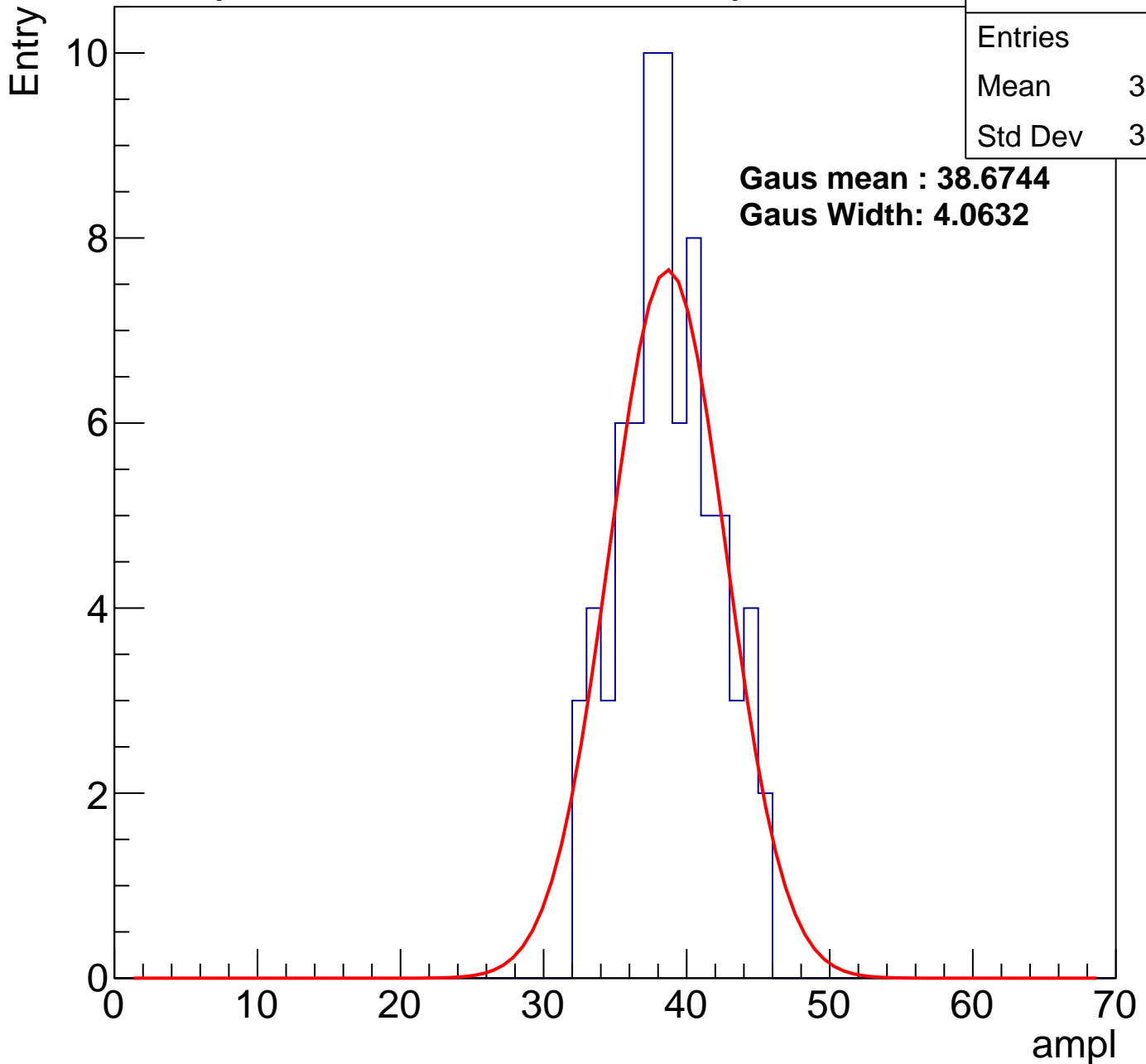
# B1L003S, U3-ch9, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	75
Mean	38.27
Std Dev	3.304

**Gaus mean : 38.6744**

**Gaus Width: 4.0632**



# B1L003S, U3-ch9, adc2

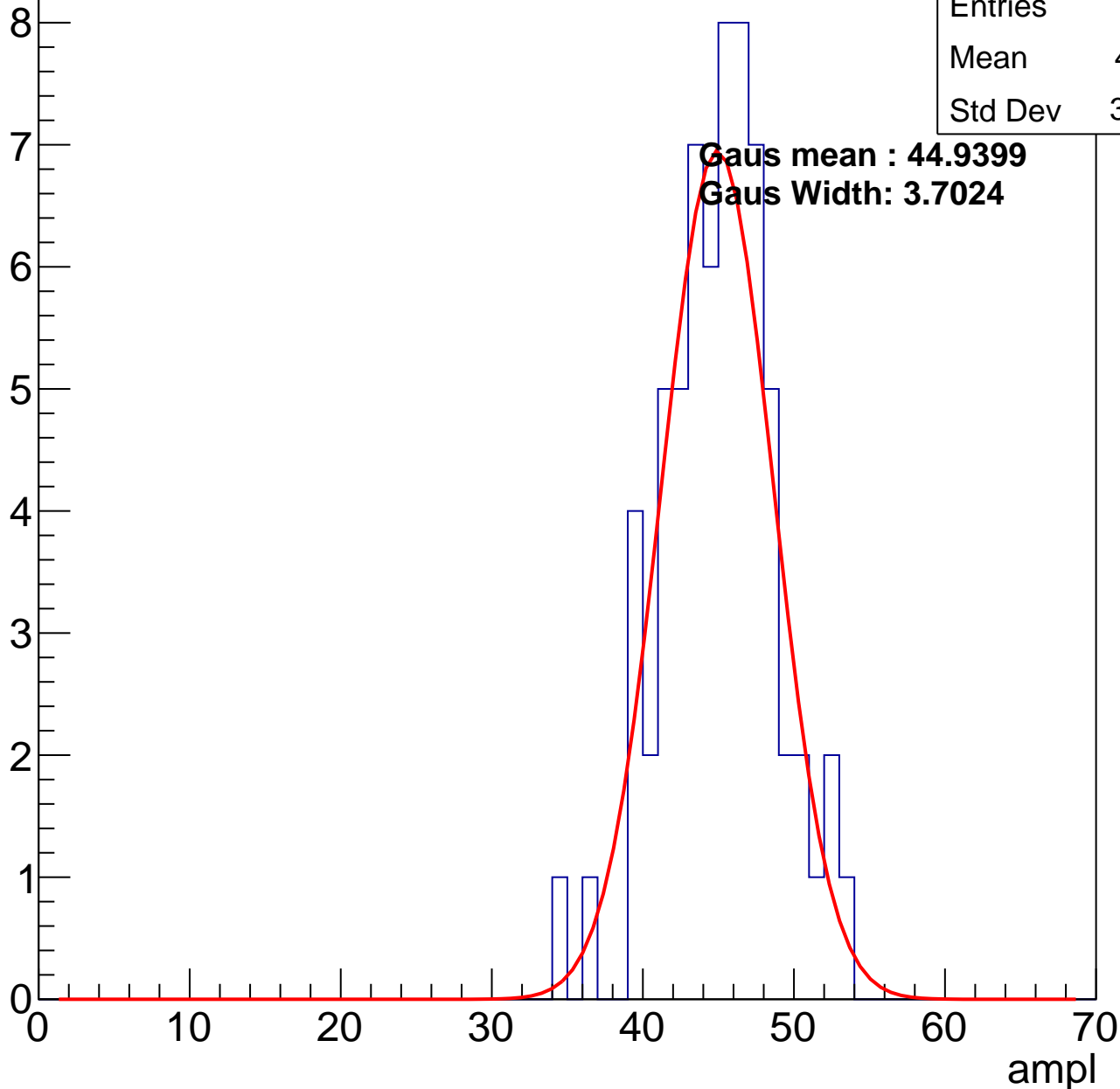
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	44.61
Std Dev	3.677

**Gaus mean : 44.9399**

**Gaus Width: 3.7024**

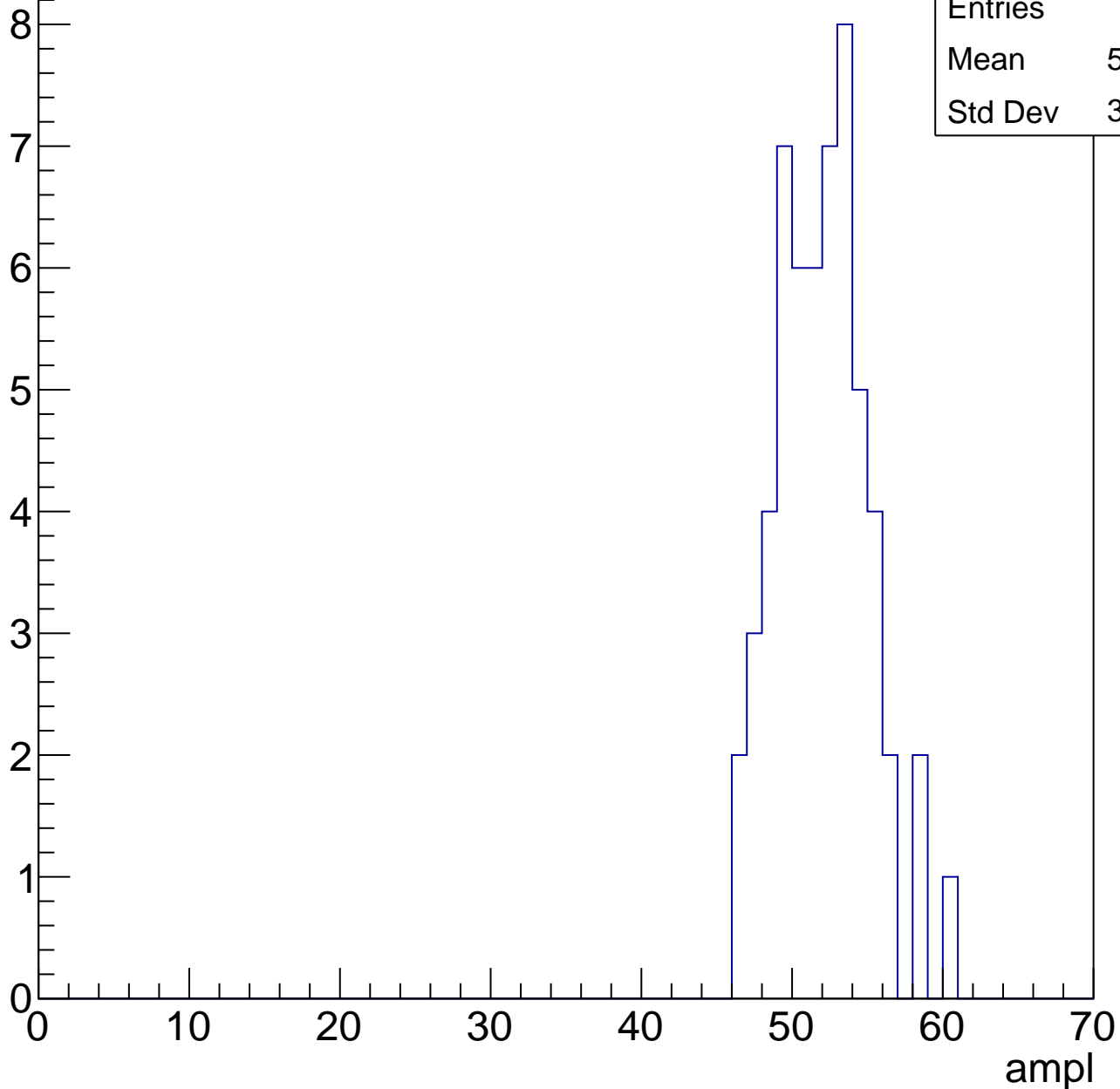


# B1L003S, U3-ch9, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	51.58
Std Dev	3.037

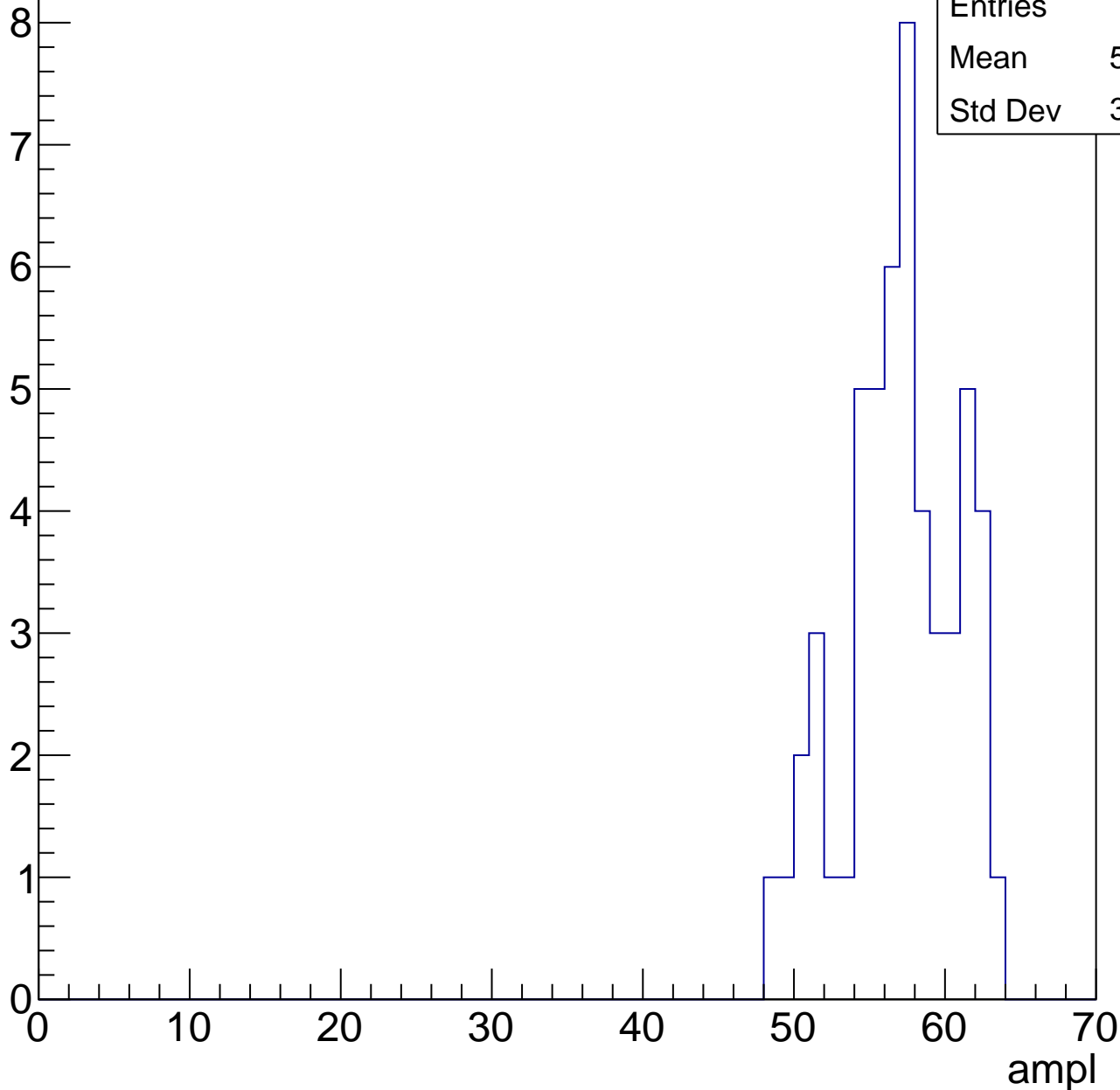


# B1L003S, U3-ch9, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	56.55
Std Dev	3.663

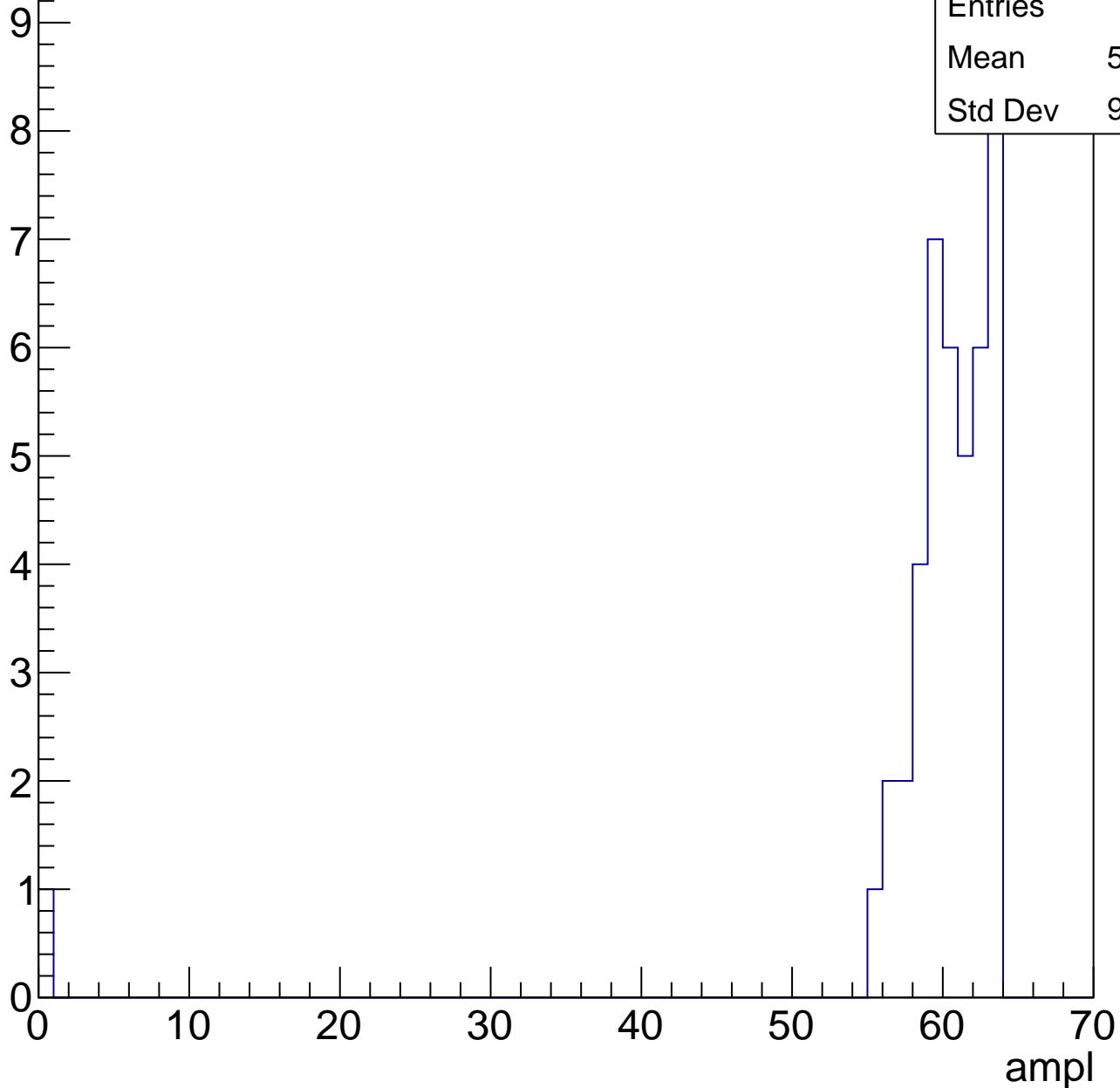


# B1L003S, U3-ch9, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	43
Mean	58.84
Std Dev	9.338



# B1L003S, U3-ch9, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L003S, U3-ch9, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U3-ch10, adc0

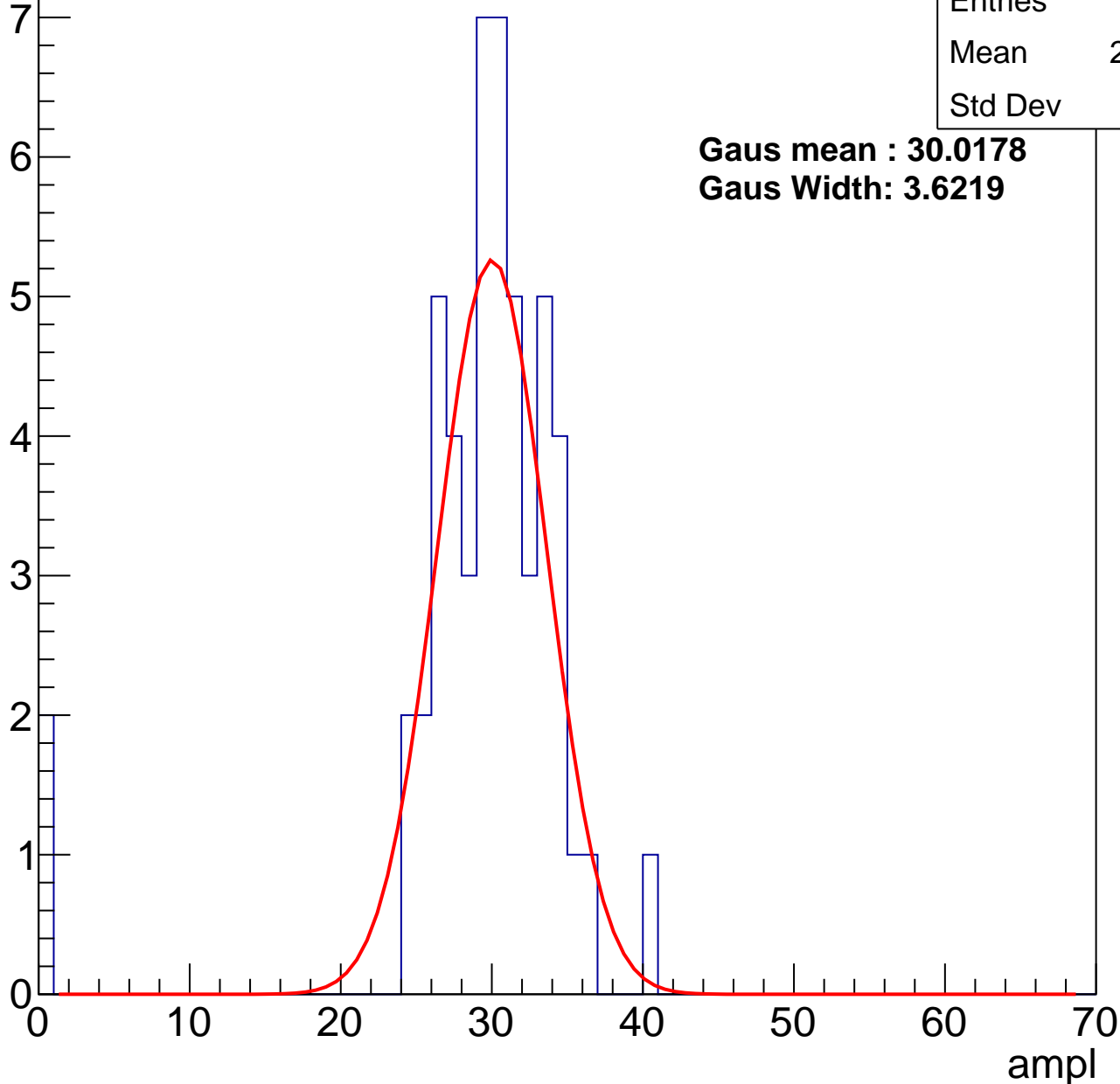
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	52
Mean	28.77
Std Dev	6.6

**Gaus mean : 30.0178**

**Gaus Width: 3.6219**



# B1L003S, U3-ch10, adc1

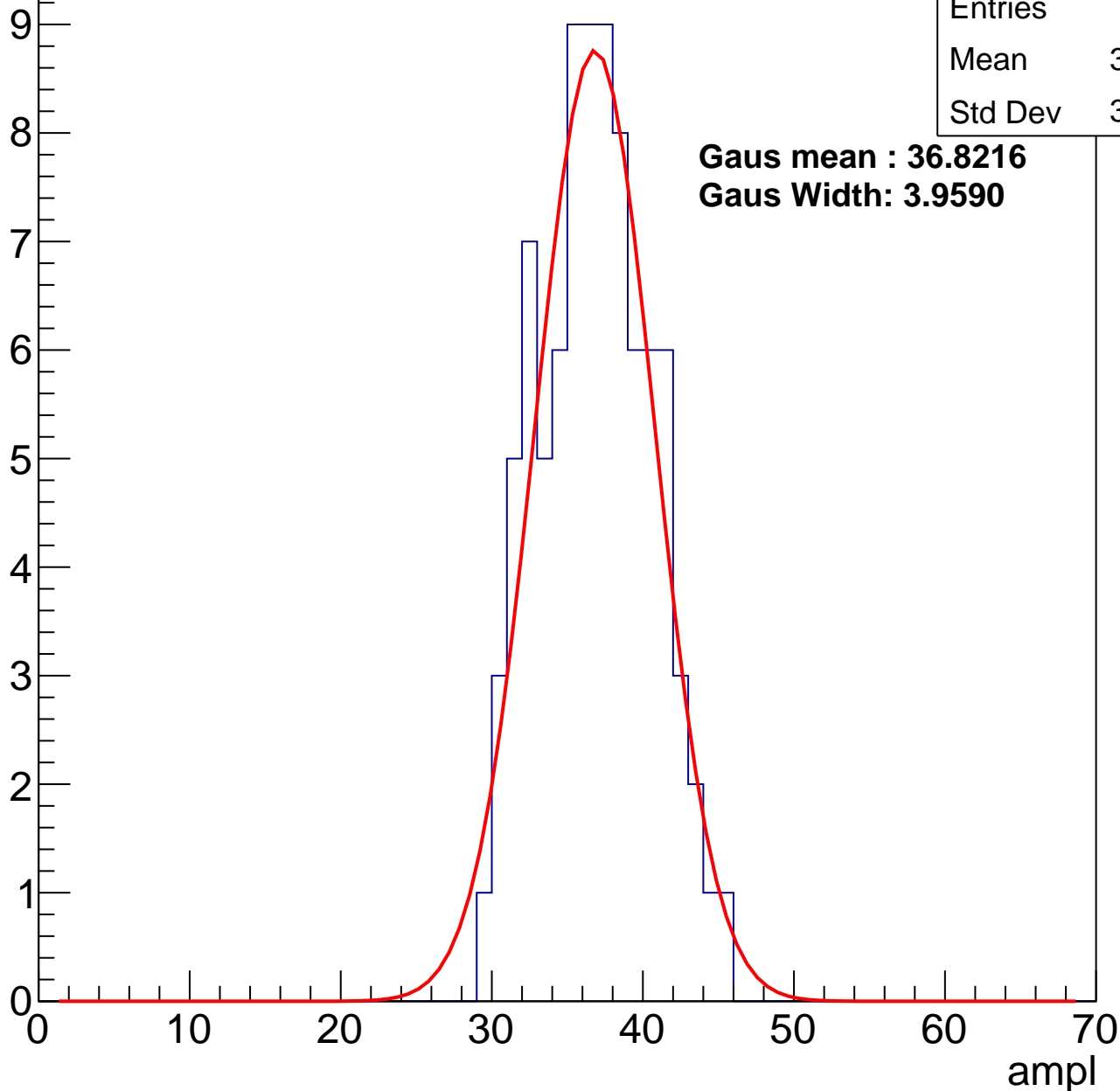
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	87
Mean	36.37
Std Dev	3.639

**Gaus mean : 36.8216**

**Gaus Width: 3.9590**



# B1L003S, U3-ch10, adc2

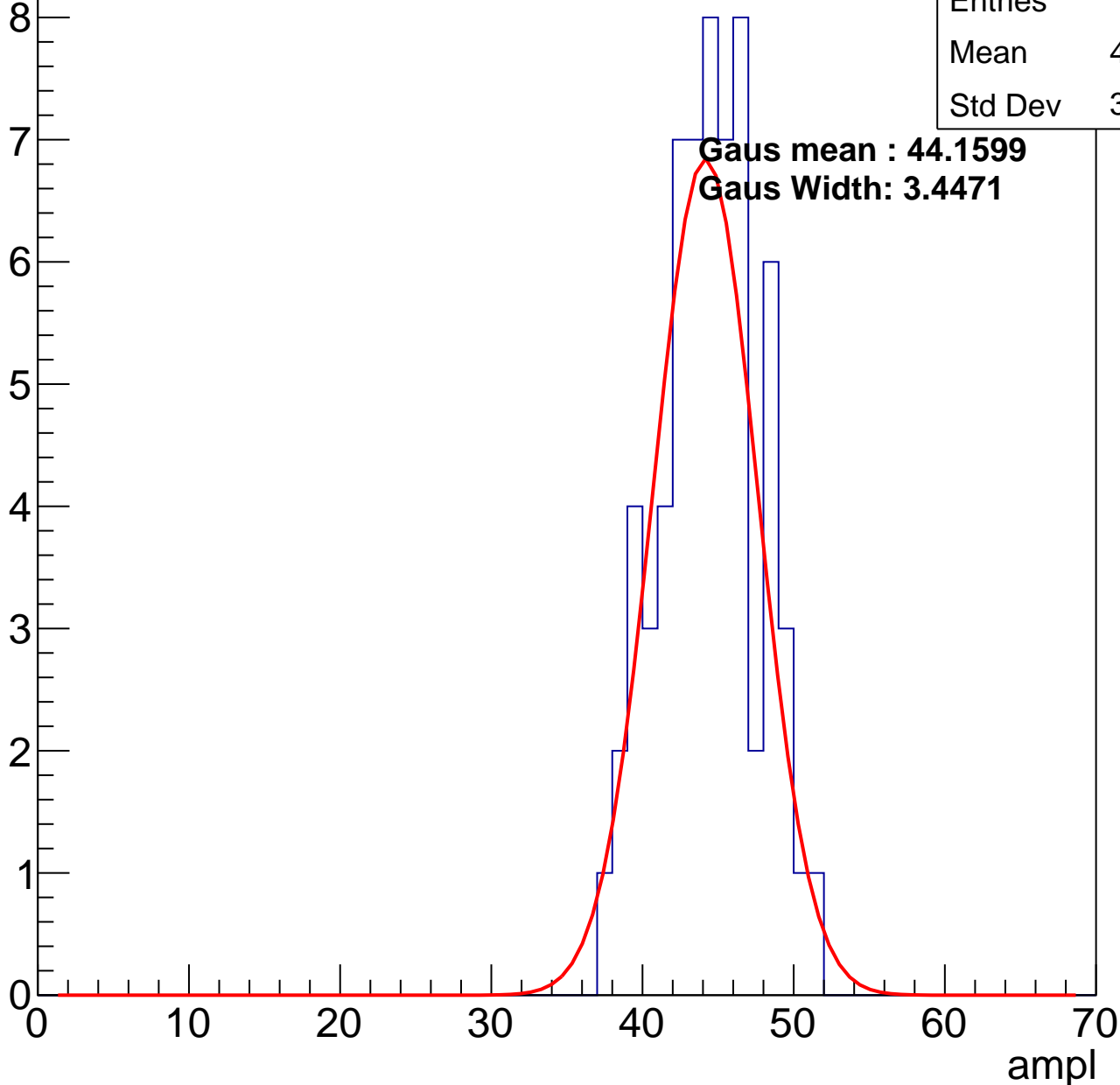
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	43.95
Std Dev	3.194

**Gaus mean : 44.1599**

**Gaus Width: 3.4471**

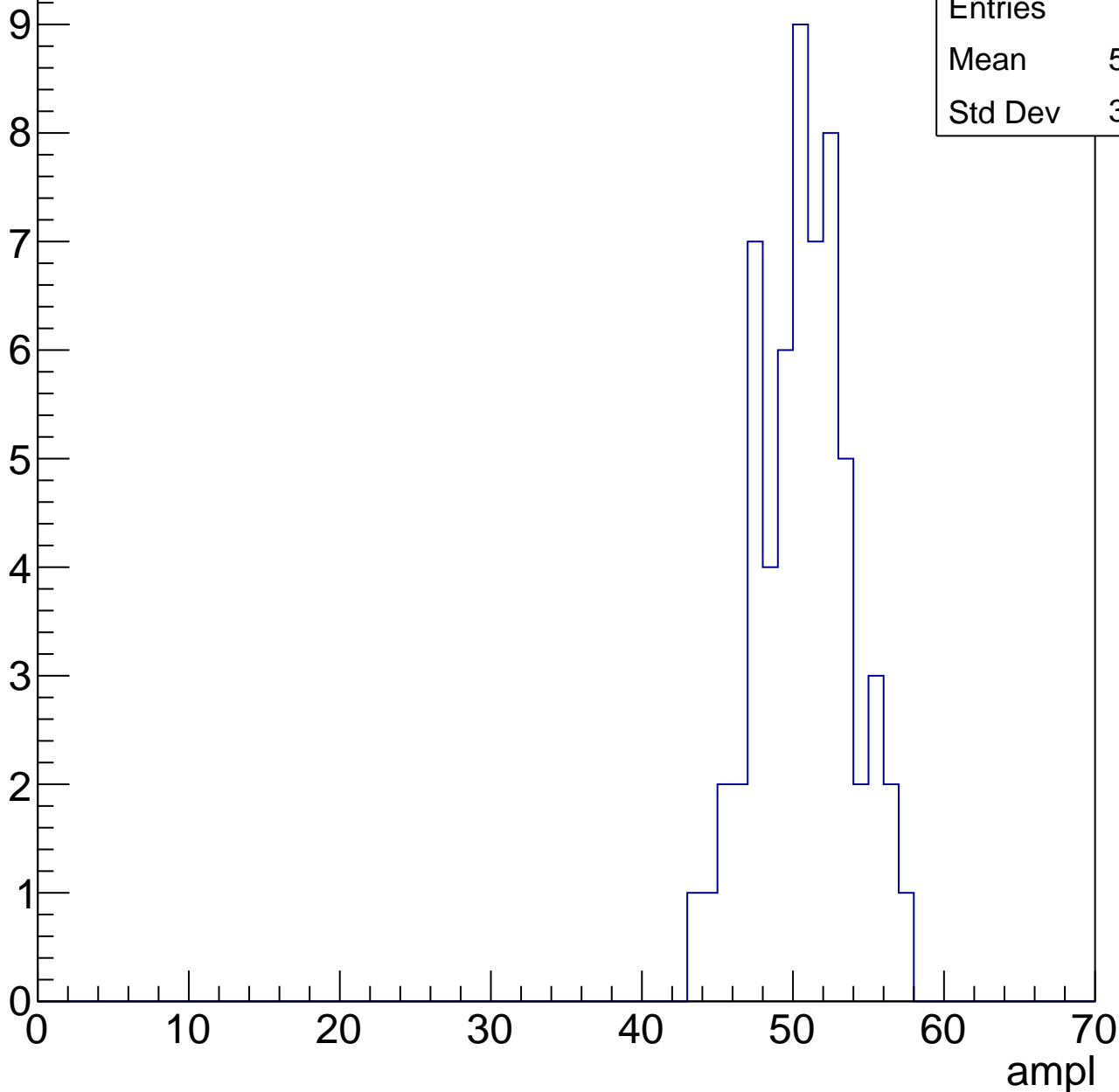


# B1L003S, U3-ch10, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	50.23
Std Dev	3.057

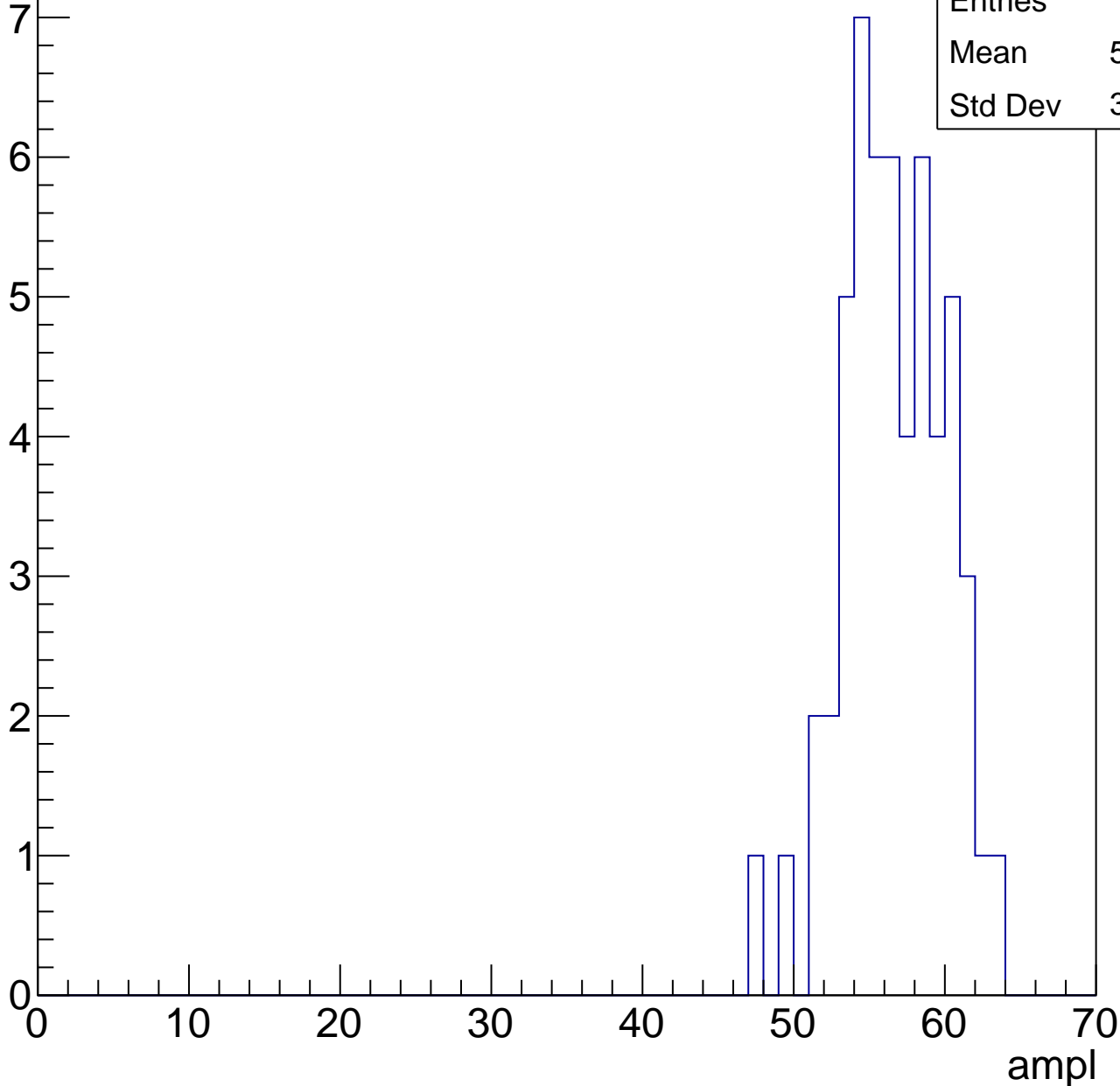


# B1L003S, U3-ch10, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	54
Mean	56.13
Std Dev	3.317

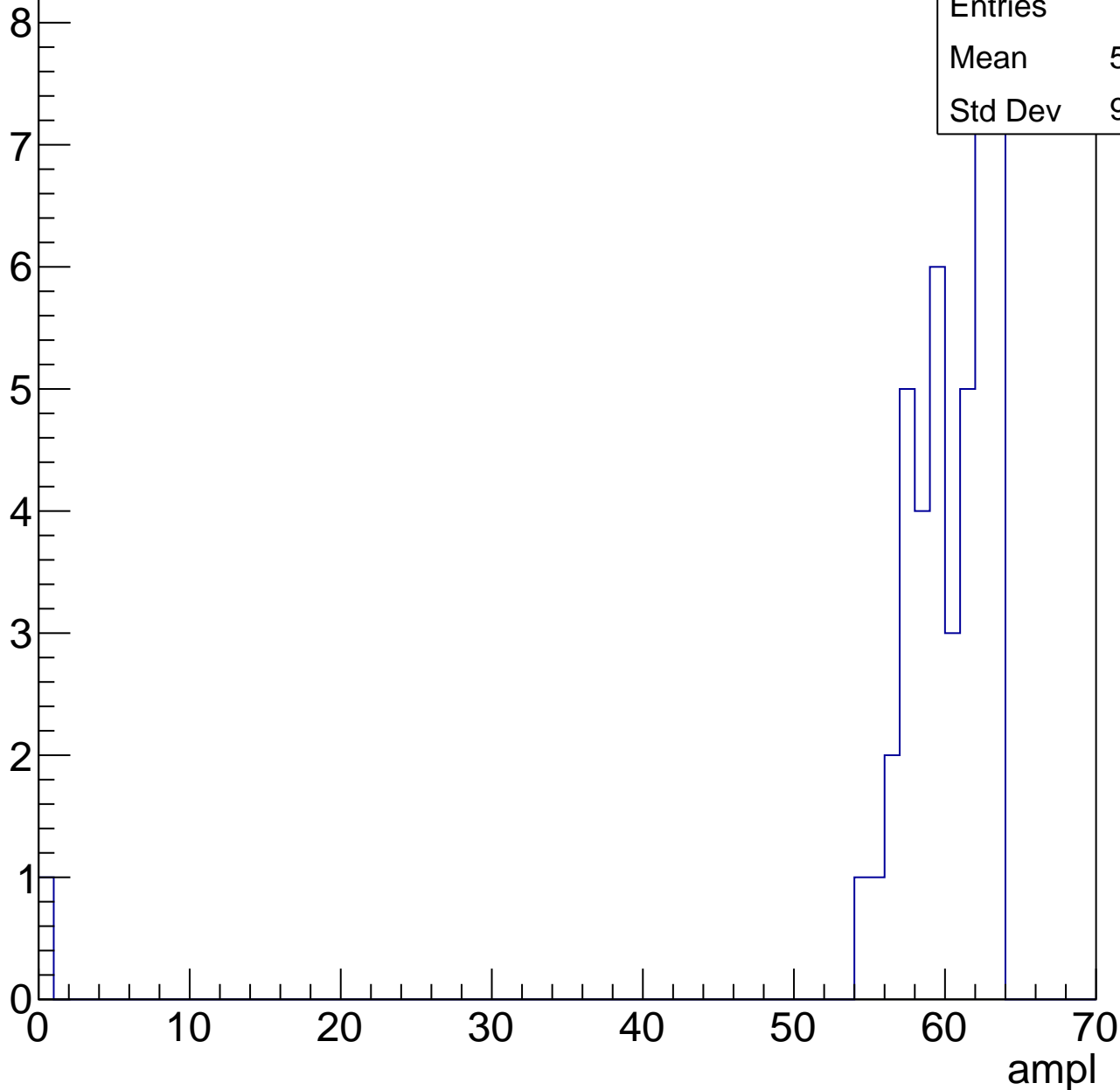


# B1L003S, U3-ch10, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	44
Mean	58.57
Std Dev	9.267



# B1L003S, U3-ch10, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

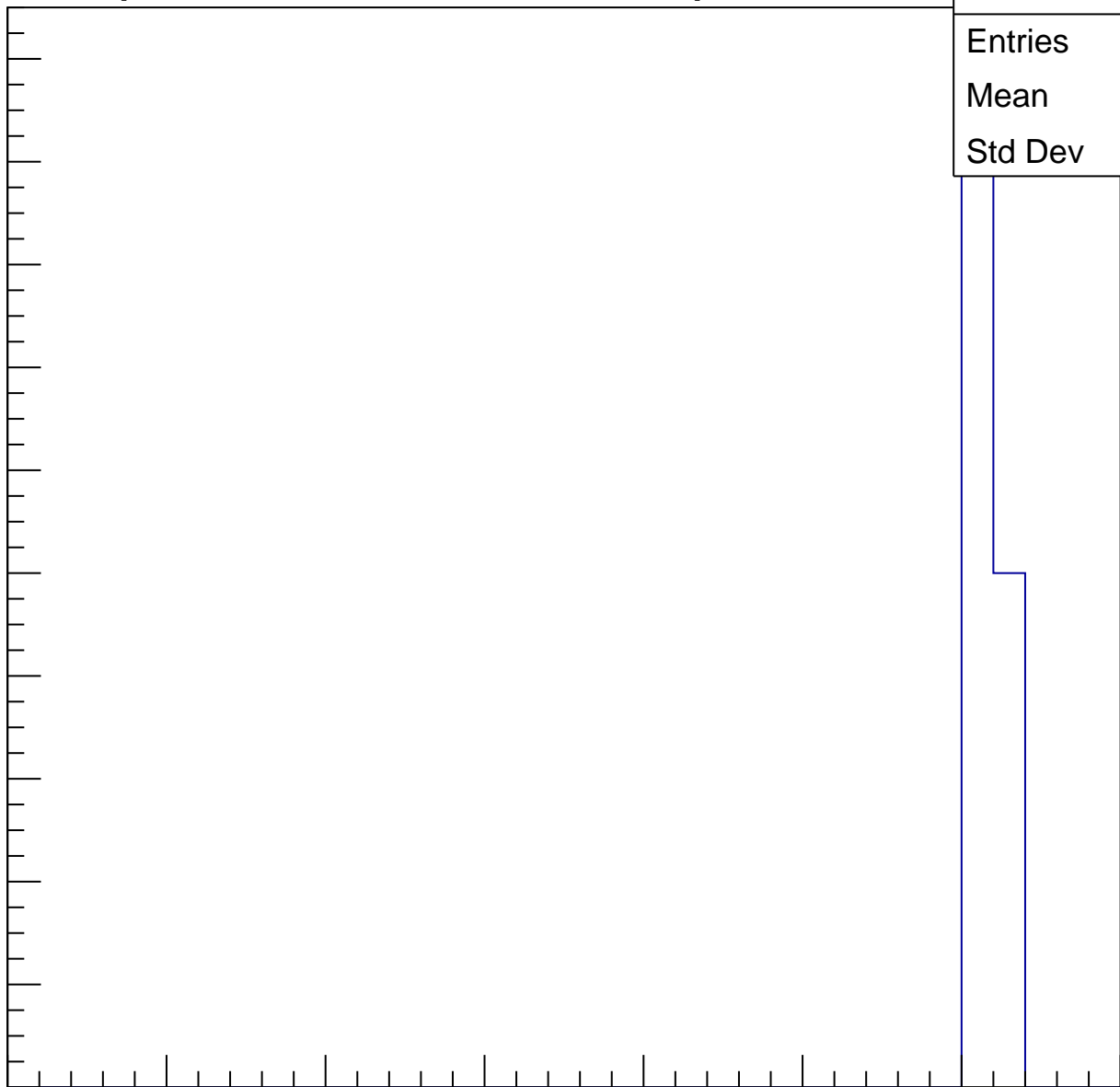
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	61.17
Std Dev	1.067

0 10 20 30 40 50 60 70

ampl

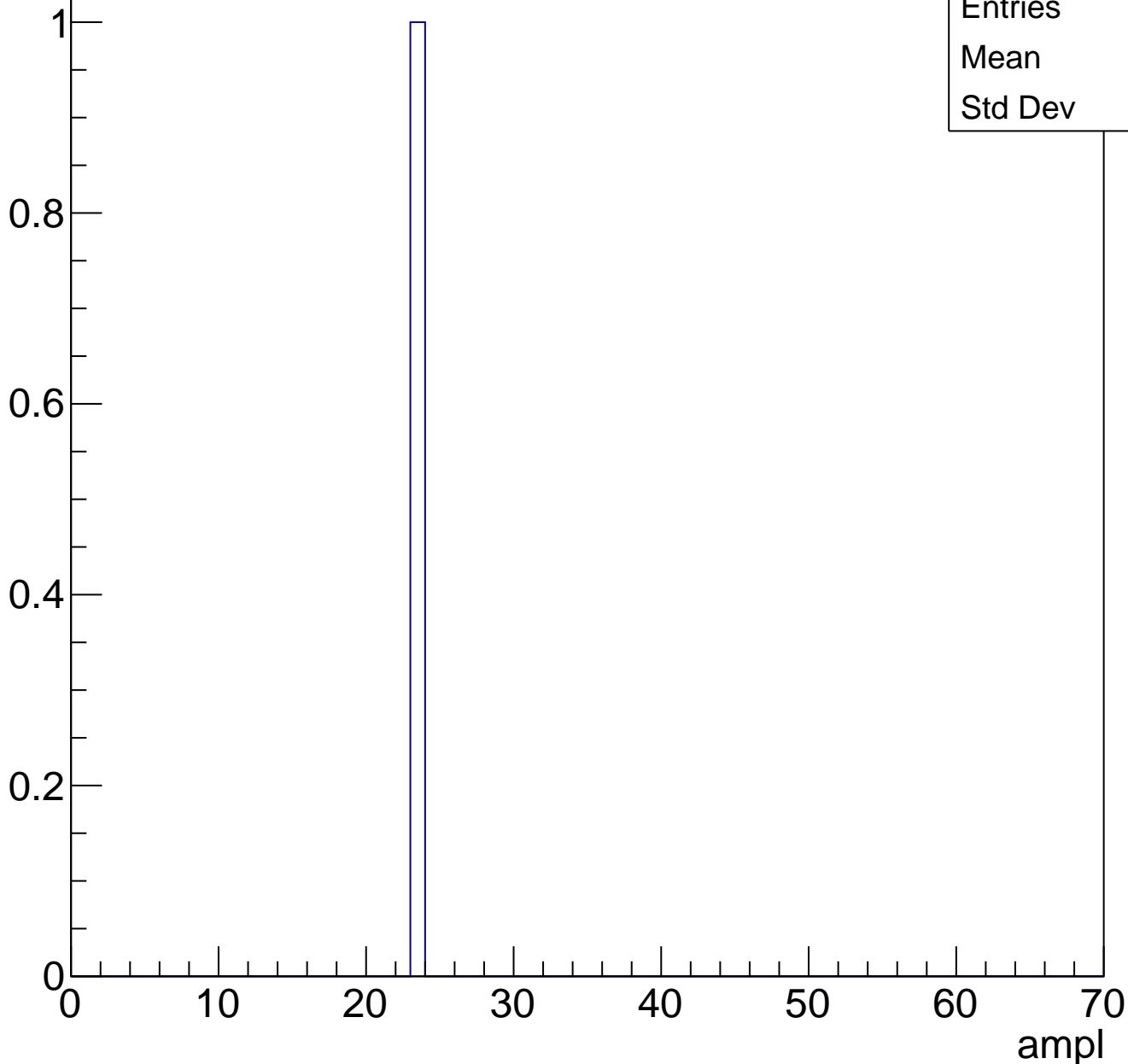




# B1L003S, U3-ch10, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U3-ch11, adc0

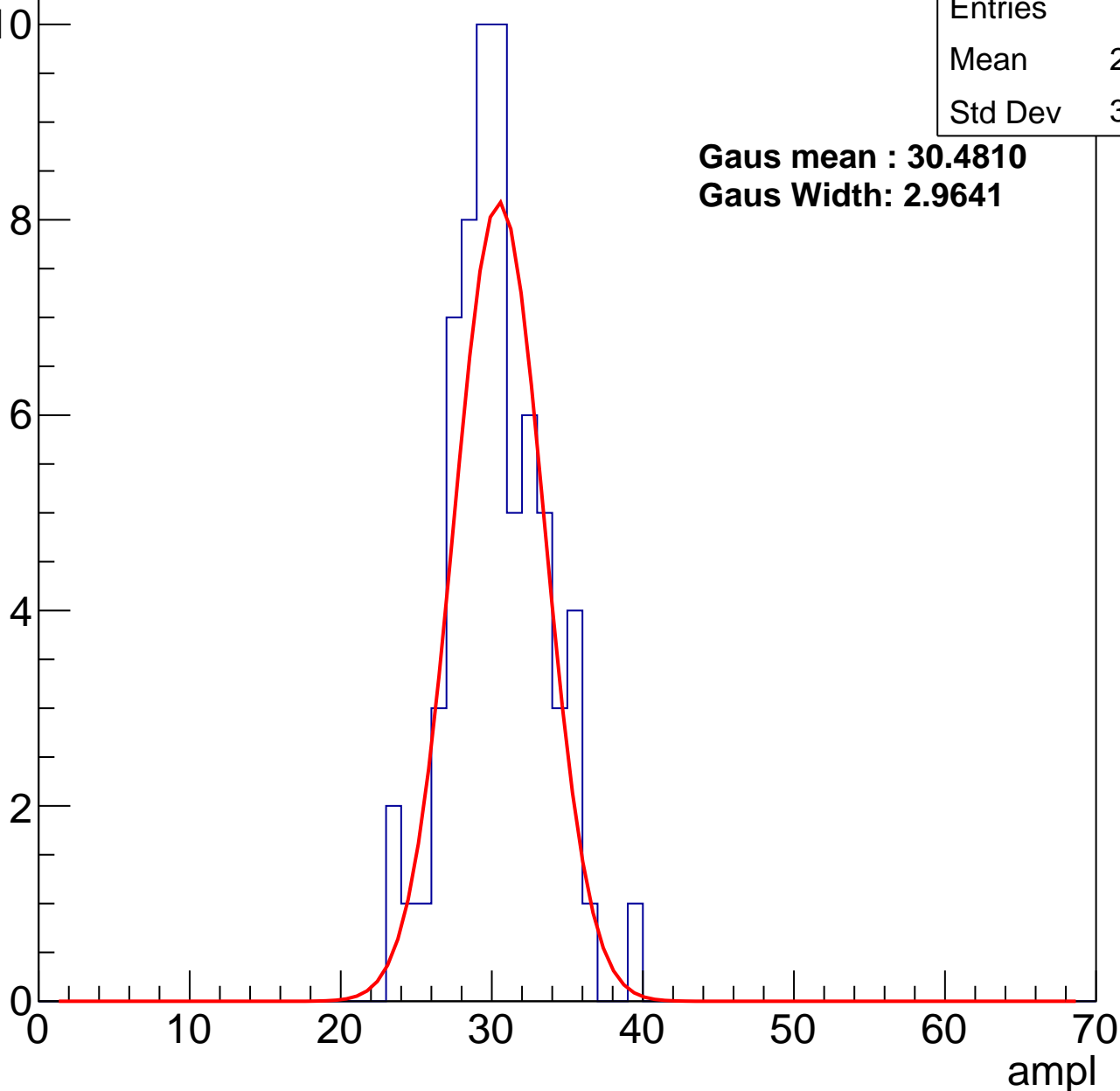
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	29.93
Std Dev	3.116

**Gaus mean : 30.4810**

**Gaus Width: 2.9641**



# B1L003S, U3-ch11, adc1

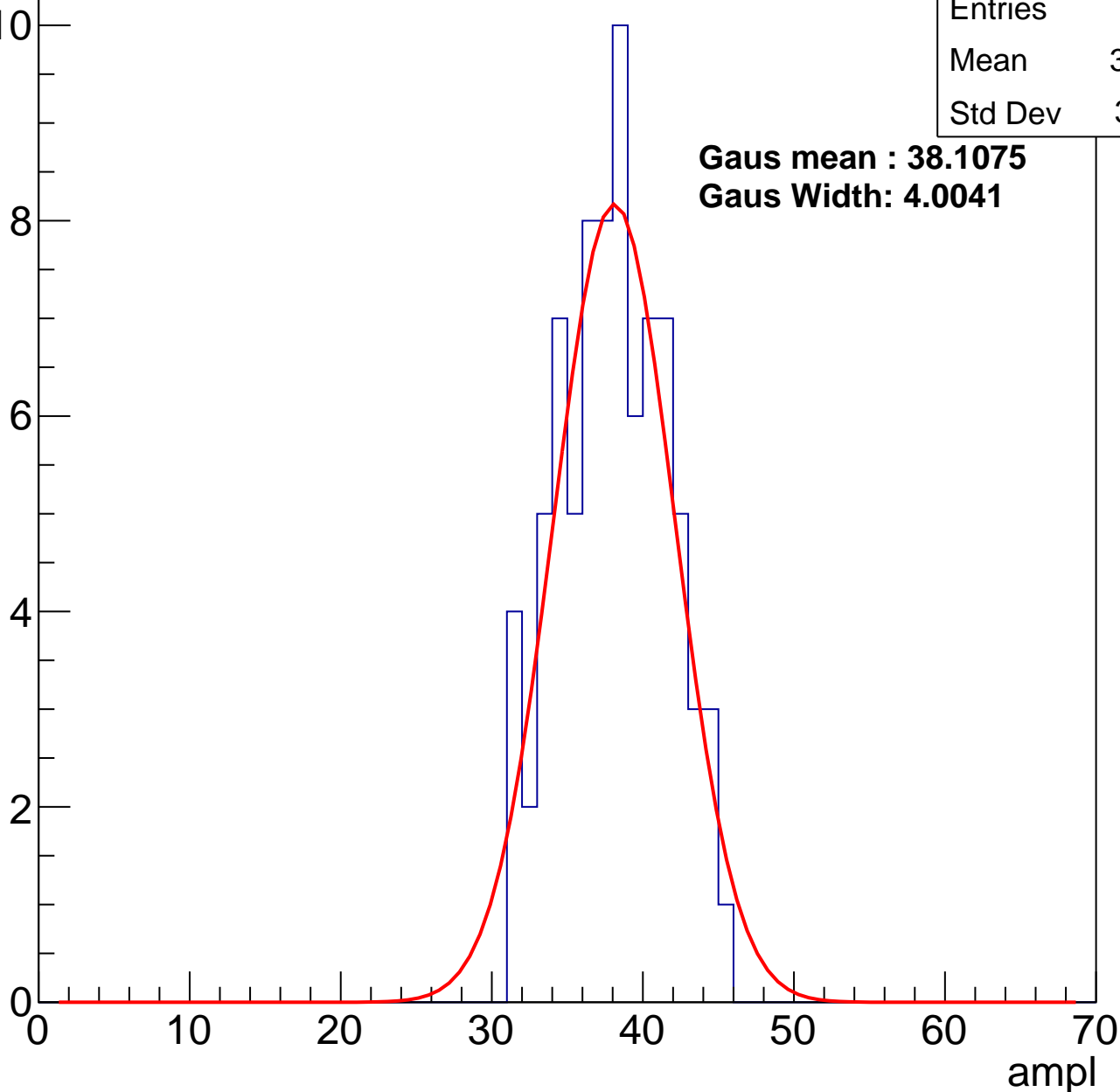
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	81
Mean	37.62
Std Dev	3.491

**Gaus mean : 38.1075**

**Gaus Width: 4.0041**



# B1L003S, U3-ch11, adc2

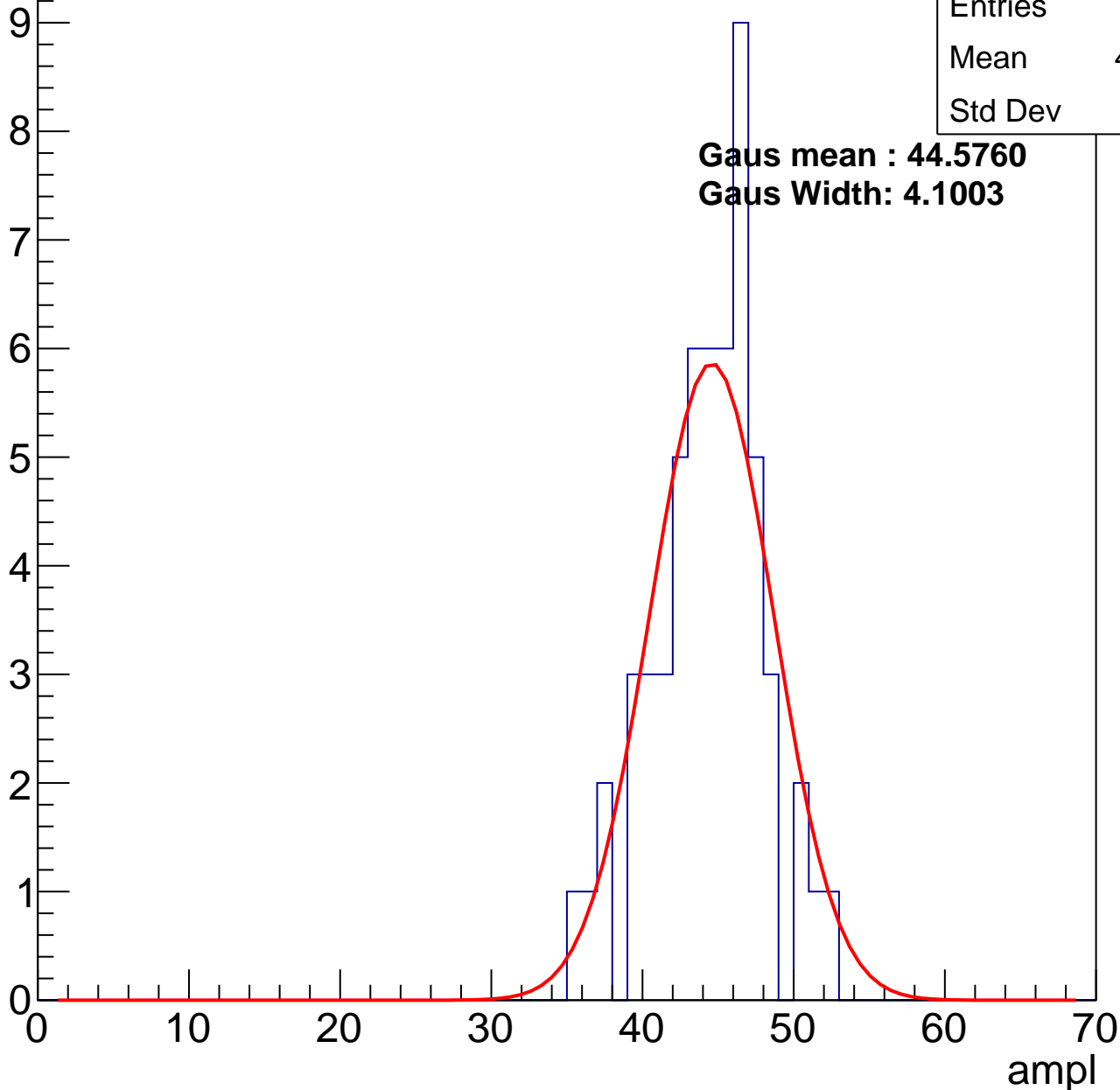
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	43.91
Std Dev	3.6

**Gaus mean : 44.5760**

**Gaus Width: 4.1003**

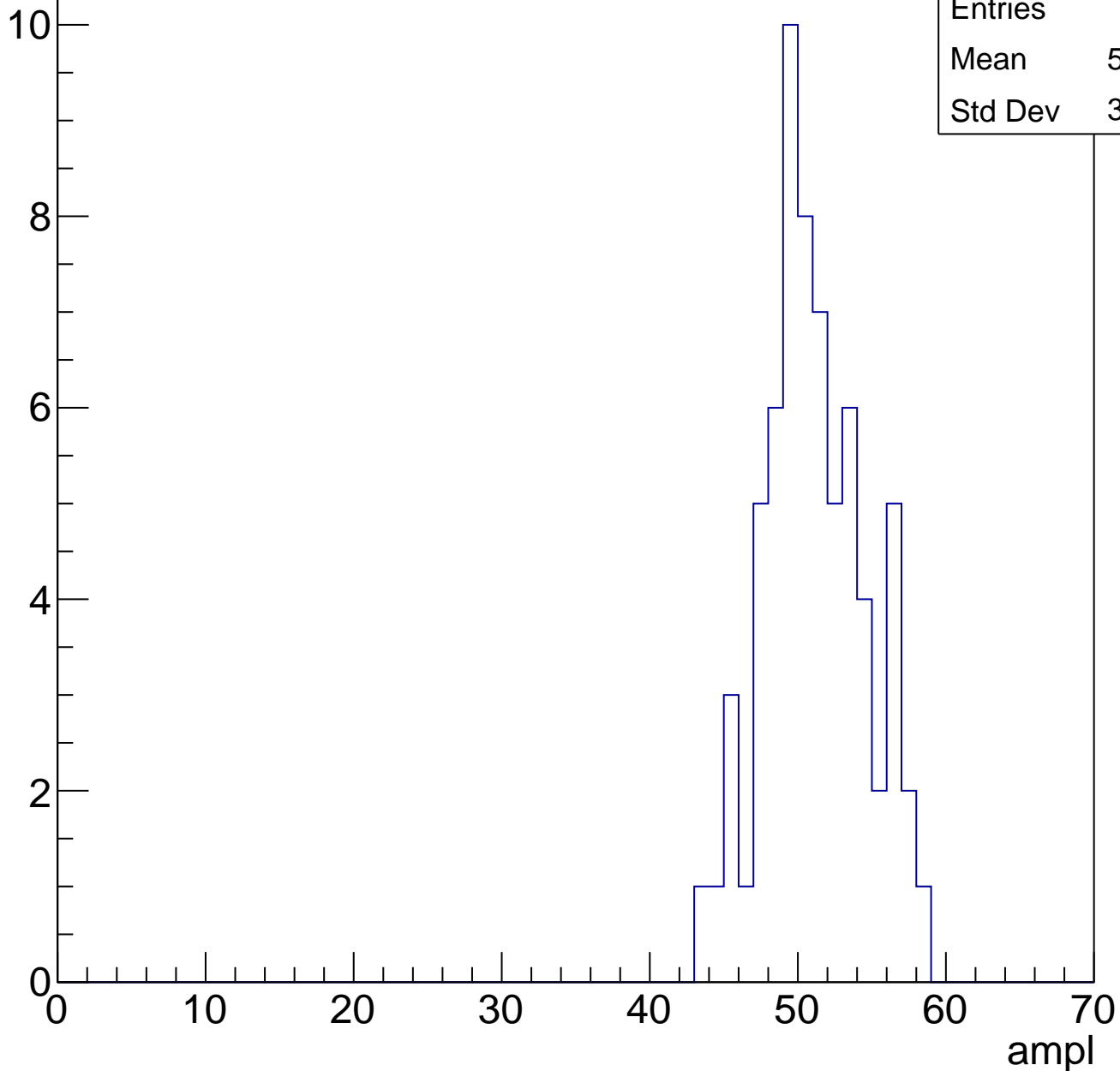


# B1L003S, U3-ch11, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	67
Mean	50.66
Std Dev	3.375

Entry

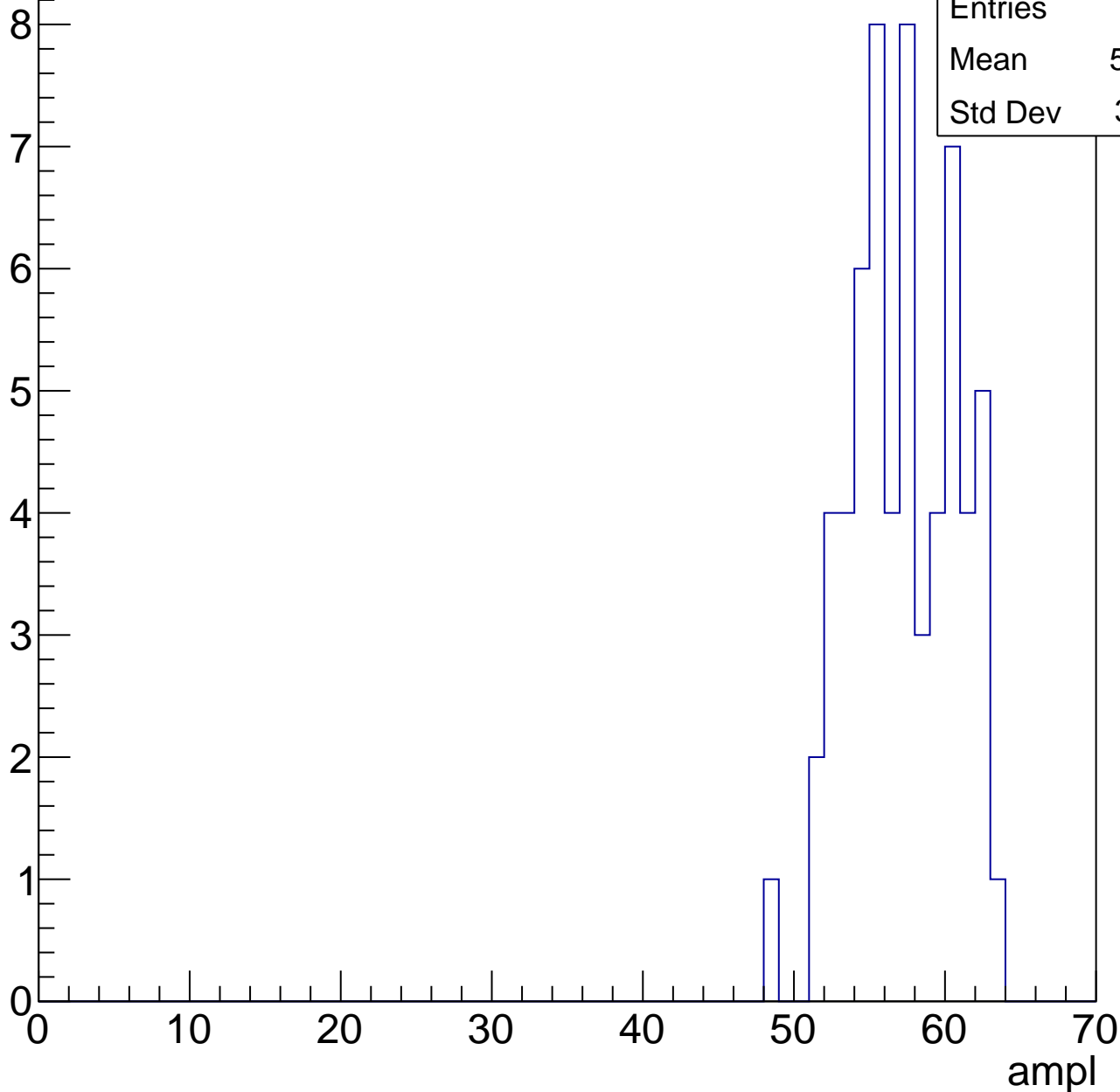


# B1L003S, U3-ch11, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	56.74
Std Dev	3.411

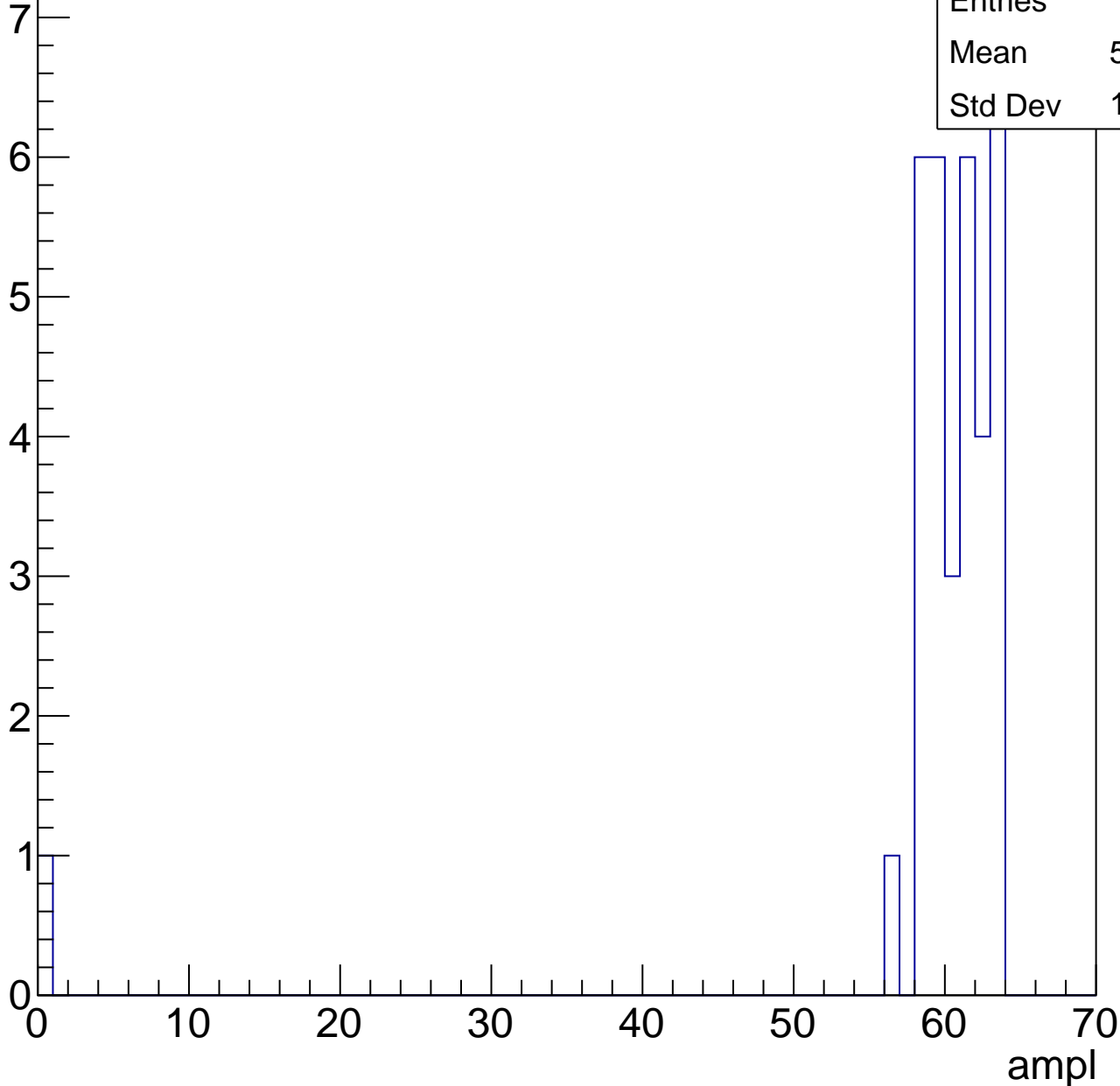


# B1L003S, U3-ch11, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	34
Mean	58.62
Std Dev	10.38



# B1L003S, U3-ch11, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch11, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U3-ch12, adc0

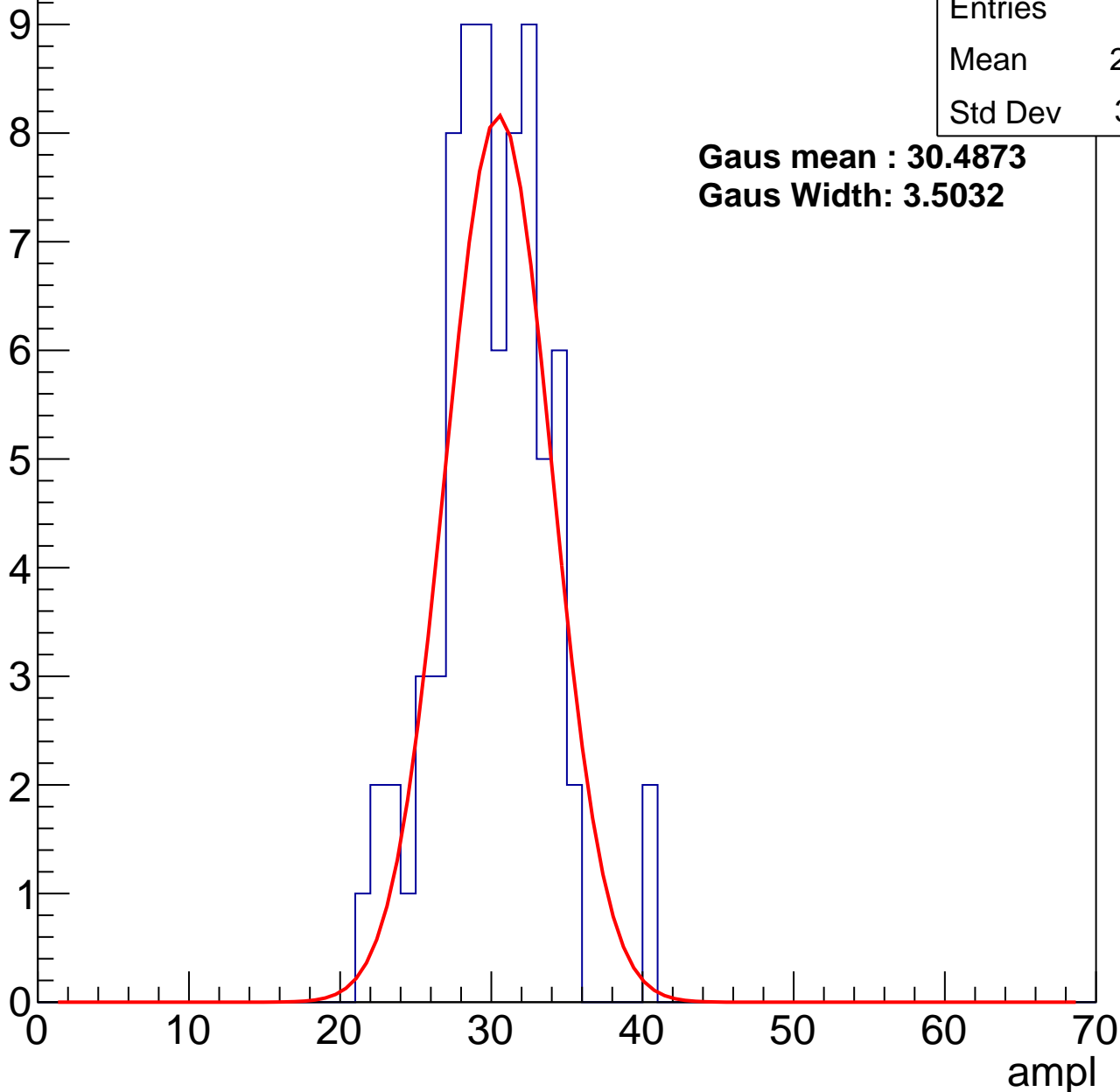
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	76
Mean	29.63
Std Dev	3.641

**Gaus mean : 30.4873**

**Gaus Width: 3.5032**



# B1L003S, U3-ch12, adc1

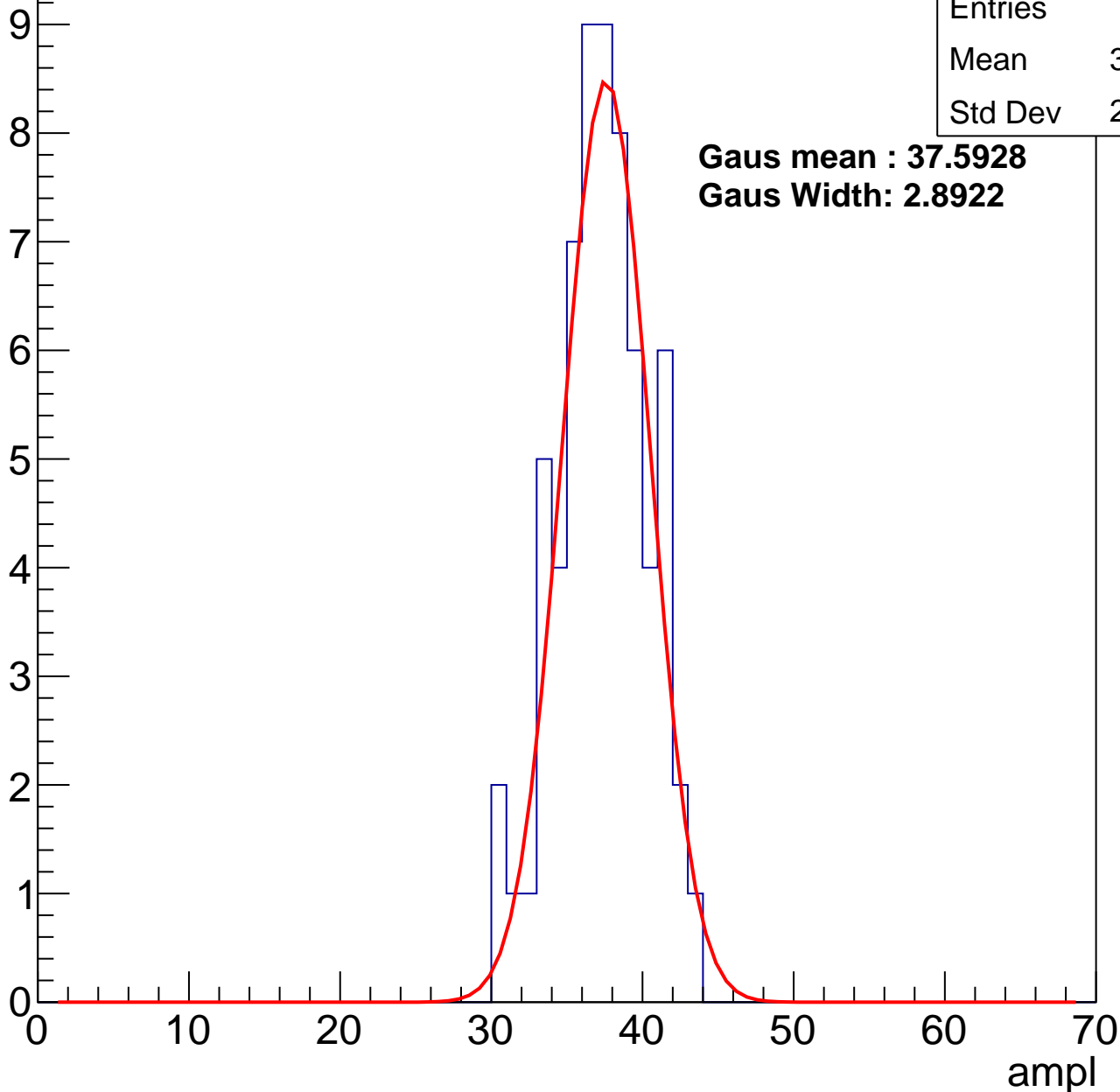
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	36.88
Std Dev	2.938

**Gaus mean : 37.5928**

**Gaus Width: 2.8922**



# B1L003S, U3-ch12, adc2

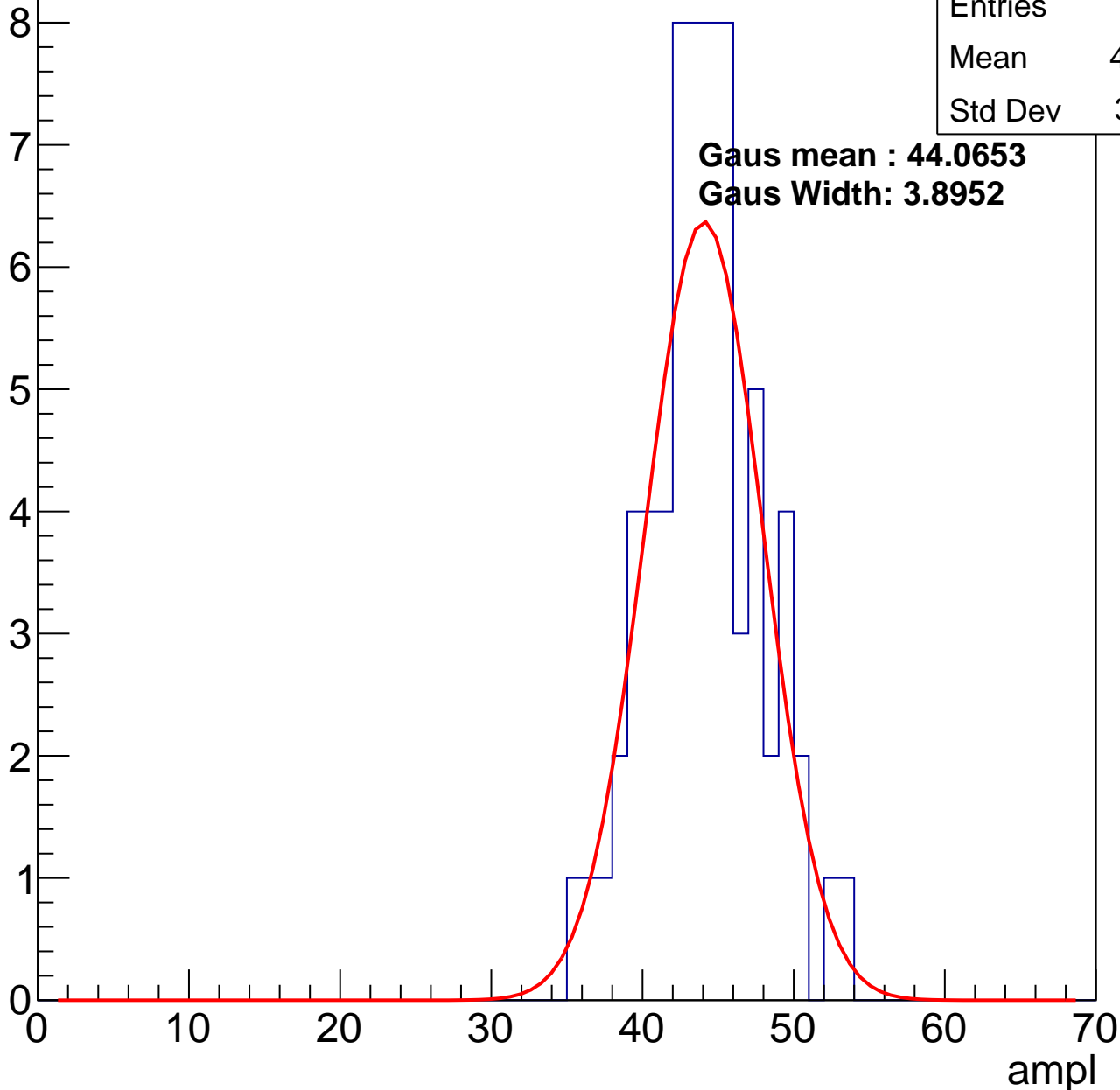
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	43.67
Std Dev	3.691

**Gaus mean : 44.0653**

**Gaus Width: 3.8952**

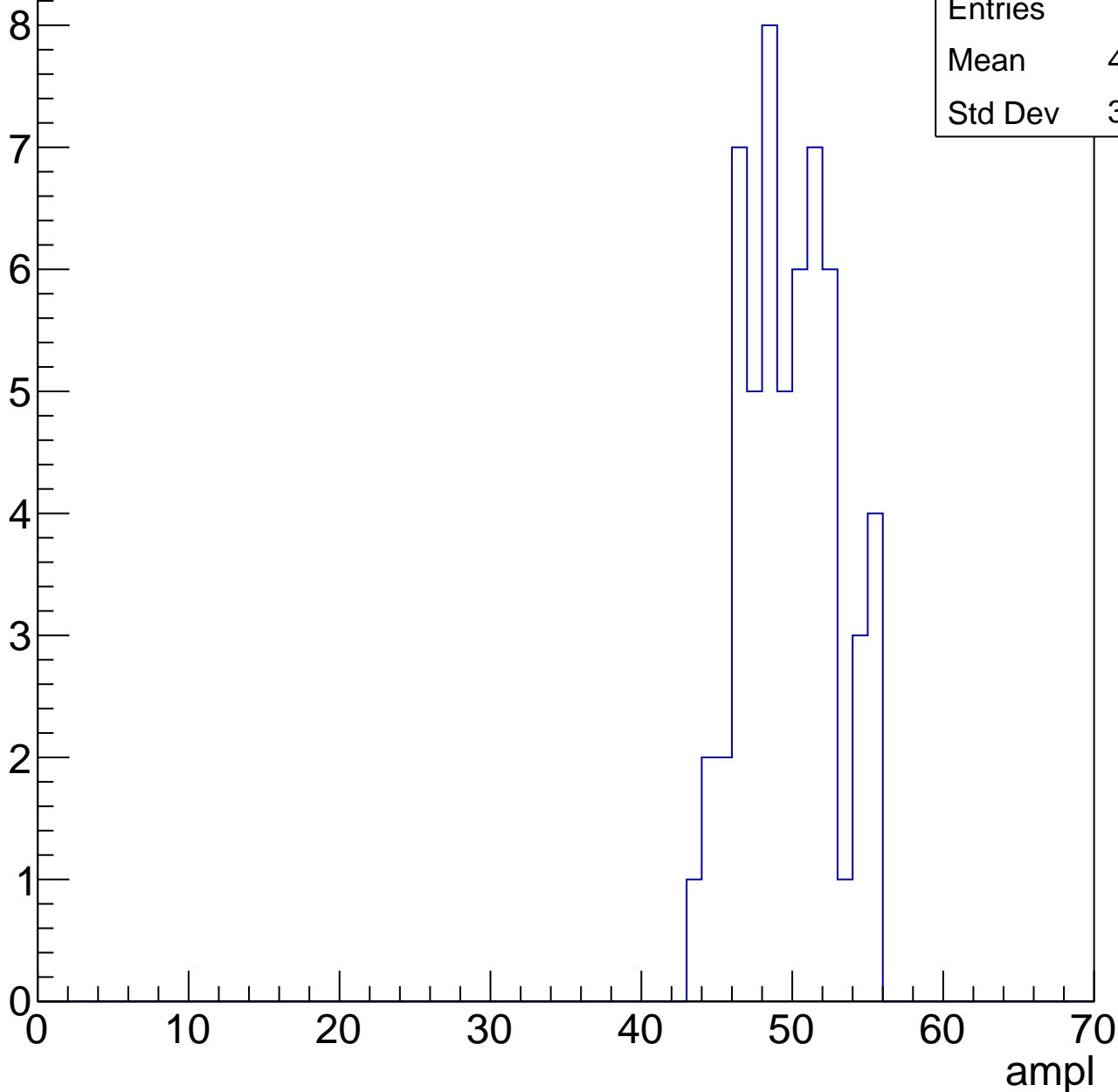


# B1L003S, U3-ch12, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

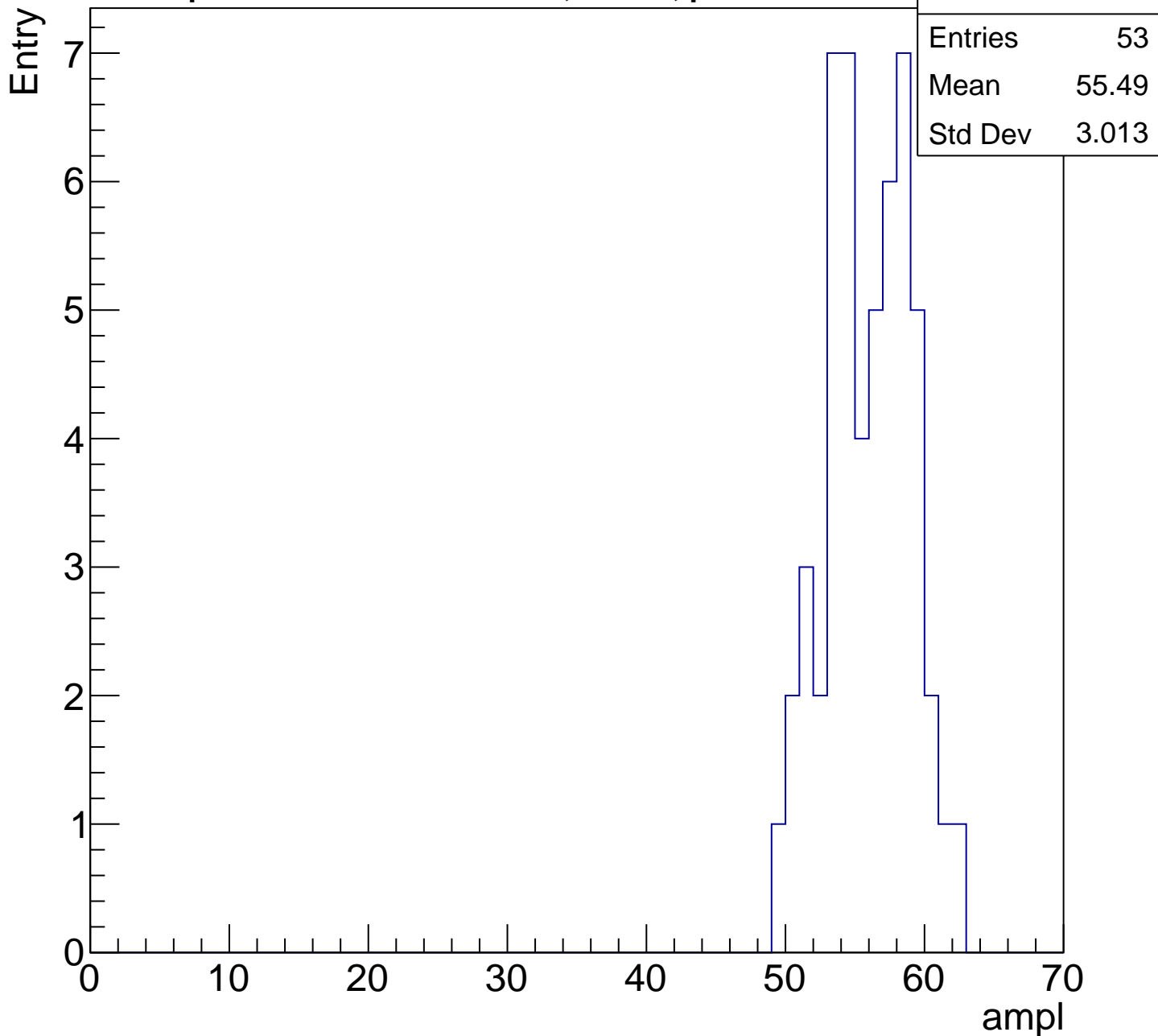
Entry

Entries	57
Mean	49.32
Std Dev	3.039



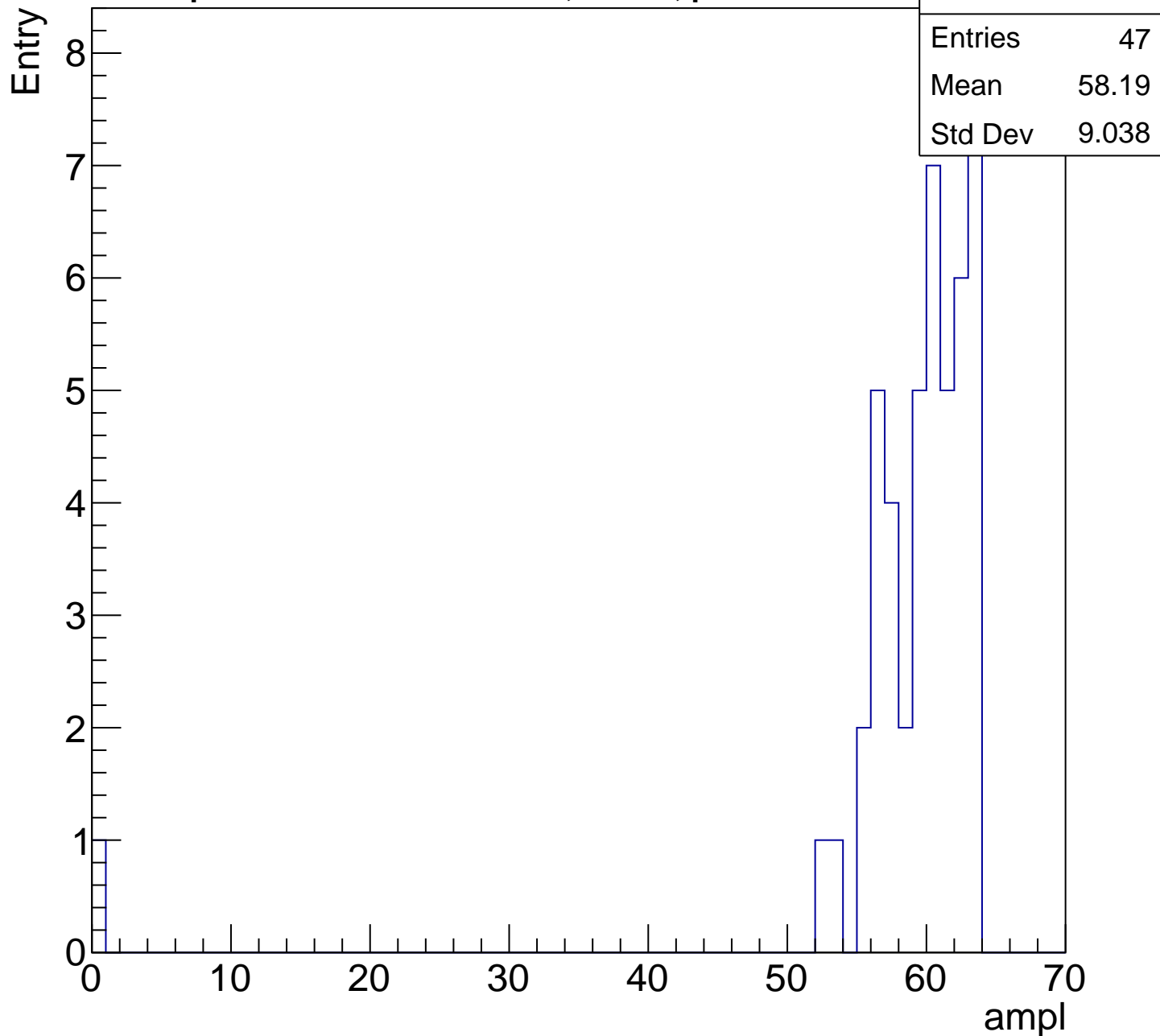
# B1L003S, U3-ch12, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2



# B1L003S, U3-ch12, adc5

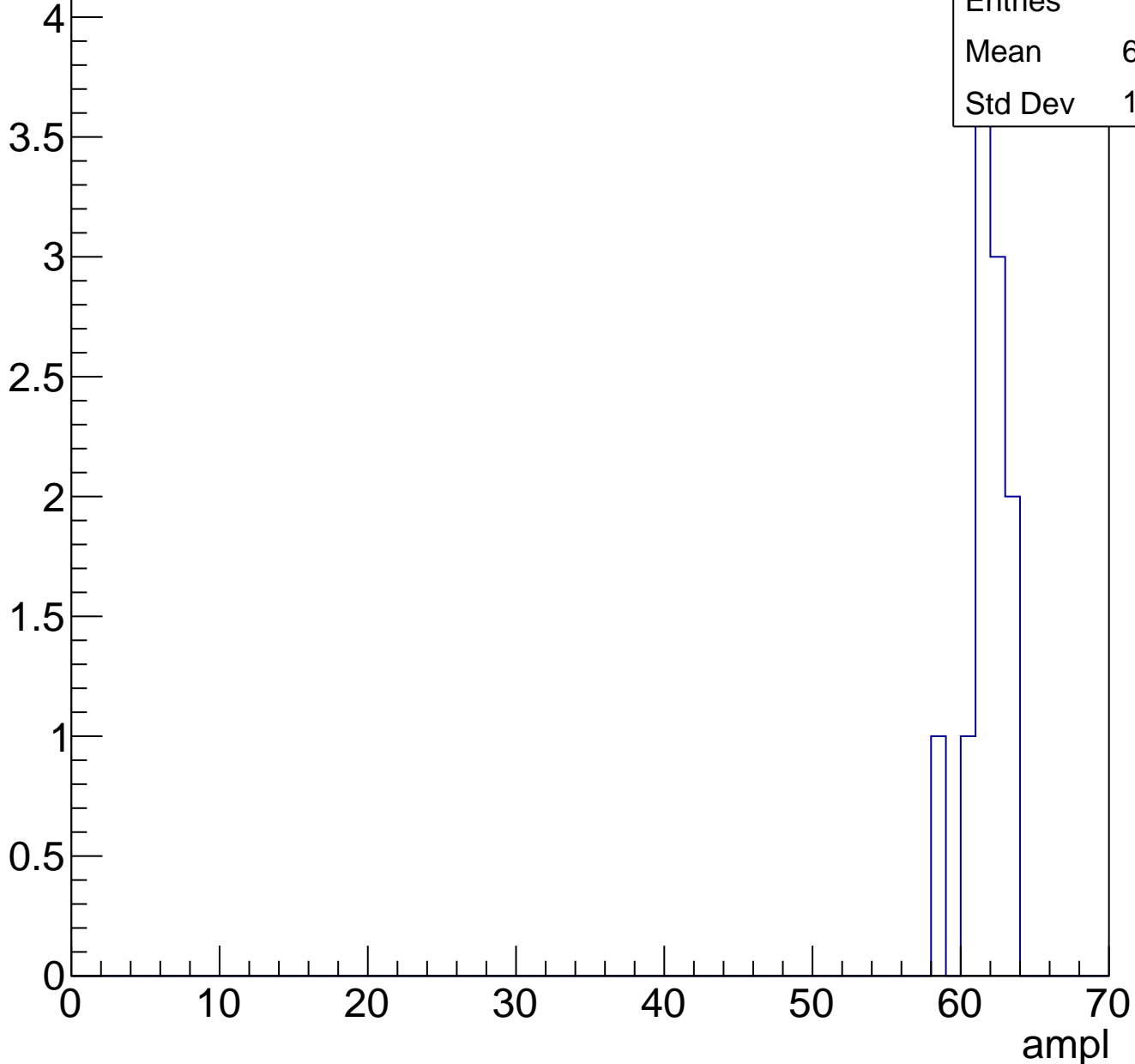
calib\_packv5\_042523\_0143.root, FC#13, port D2



# B1L003S, U3-ch12, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch12, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U3-ch13, adc0

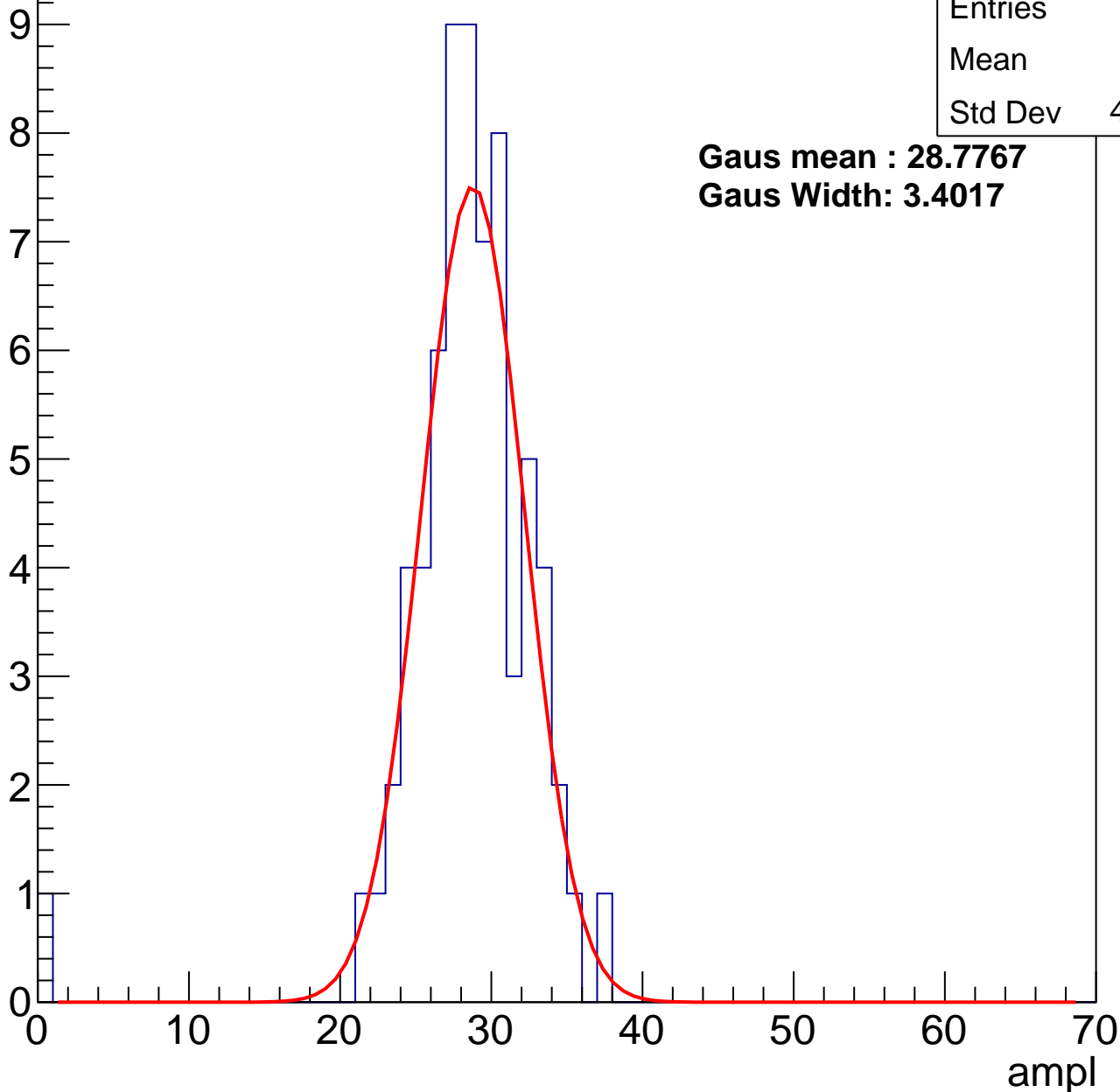
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	28
Std Dev	4.697

**Gaus mean : 28.7767**

**Gaus Width: 3.4017**



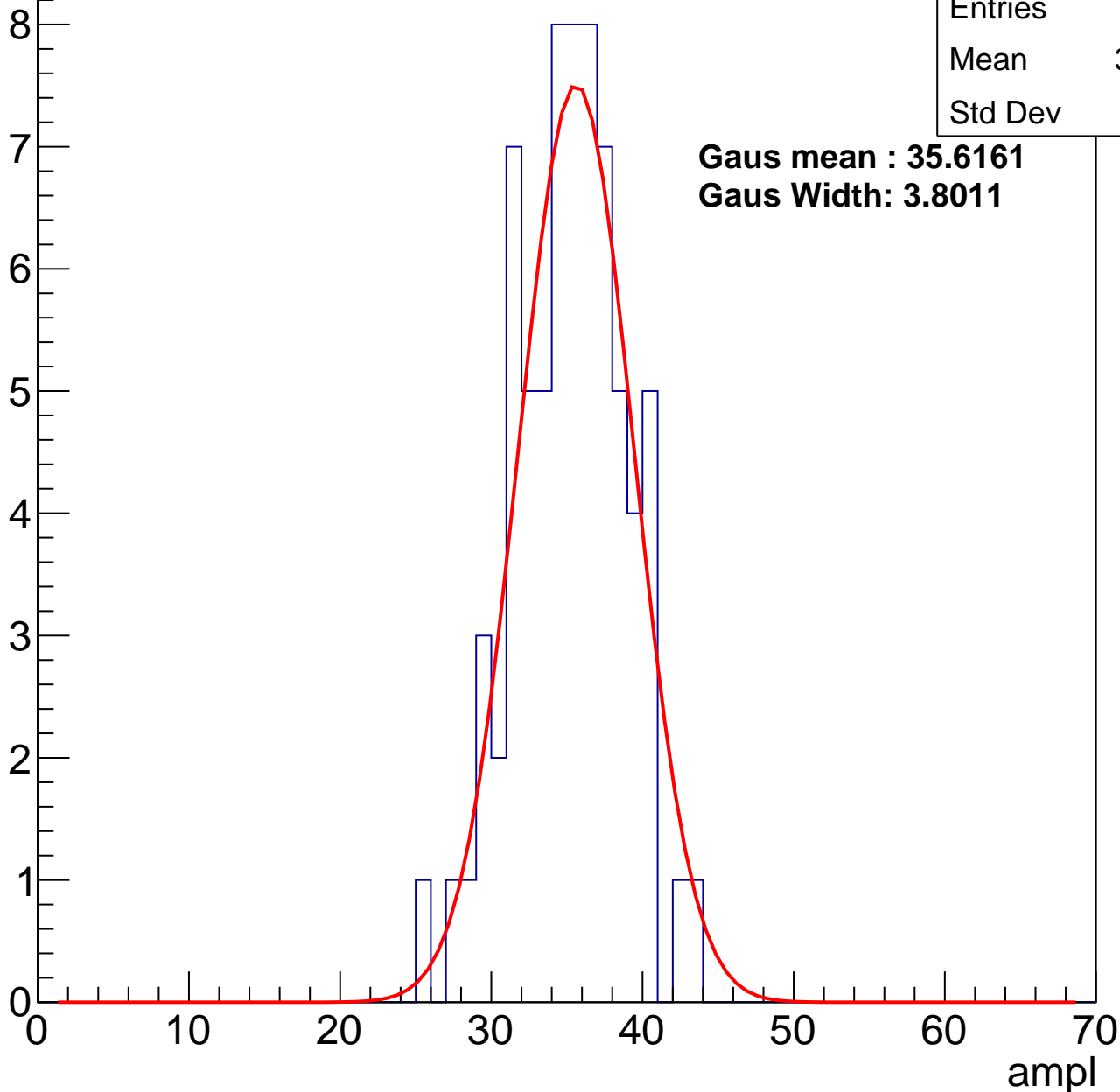
# B1L003S, U3-ch13, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	72
Mean	34.71
Std Dev	3.6

**Gaus mean : 35.6161**  
**Gaus Width: 3.8011**



# B1L003S, U3-ch13, adc2

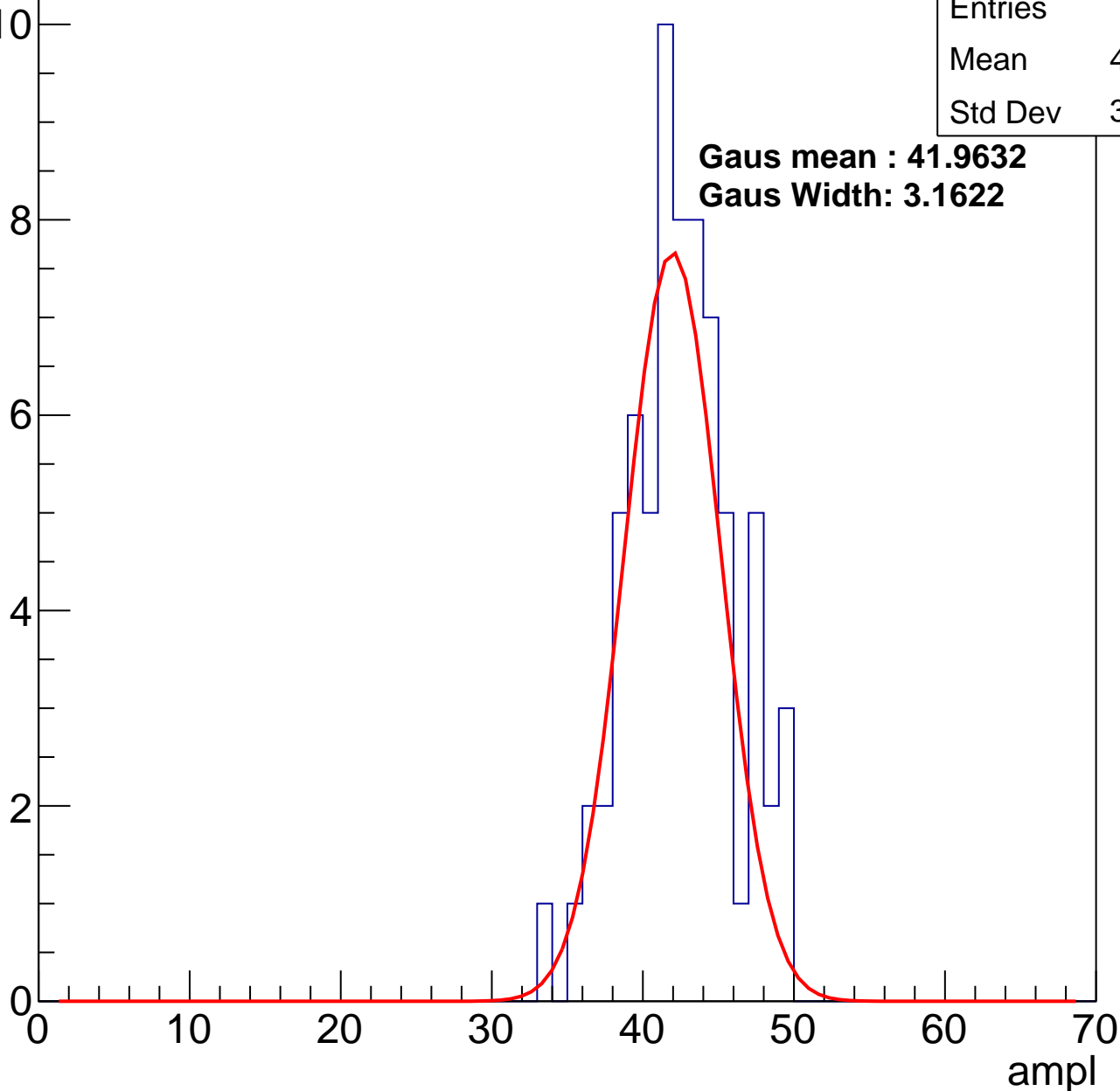
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	71
Mean	42.04
Std Dev	3.474

**Gaus mean : 41.9632**

**Gaus Width: 3.1622**

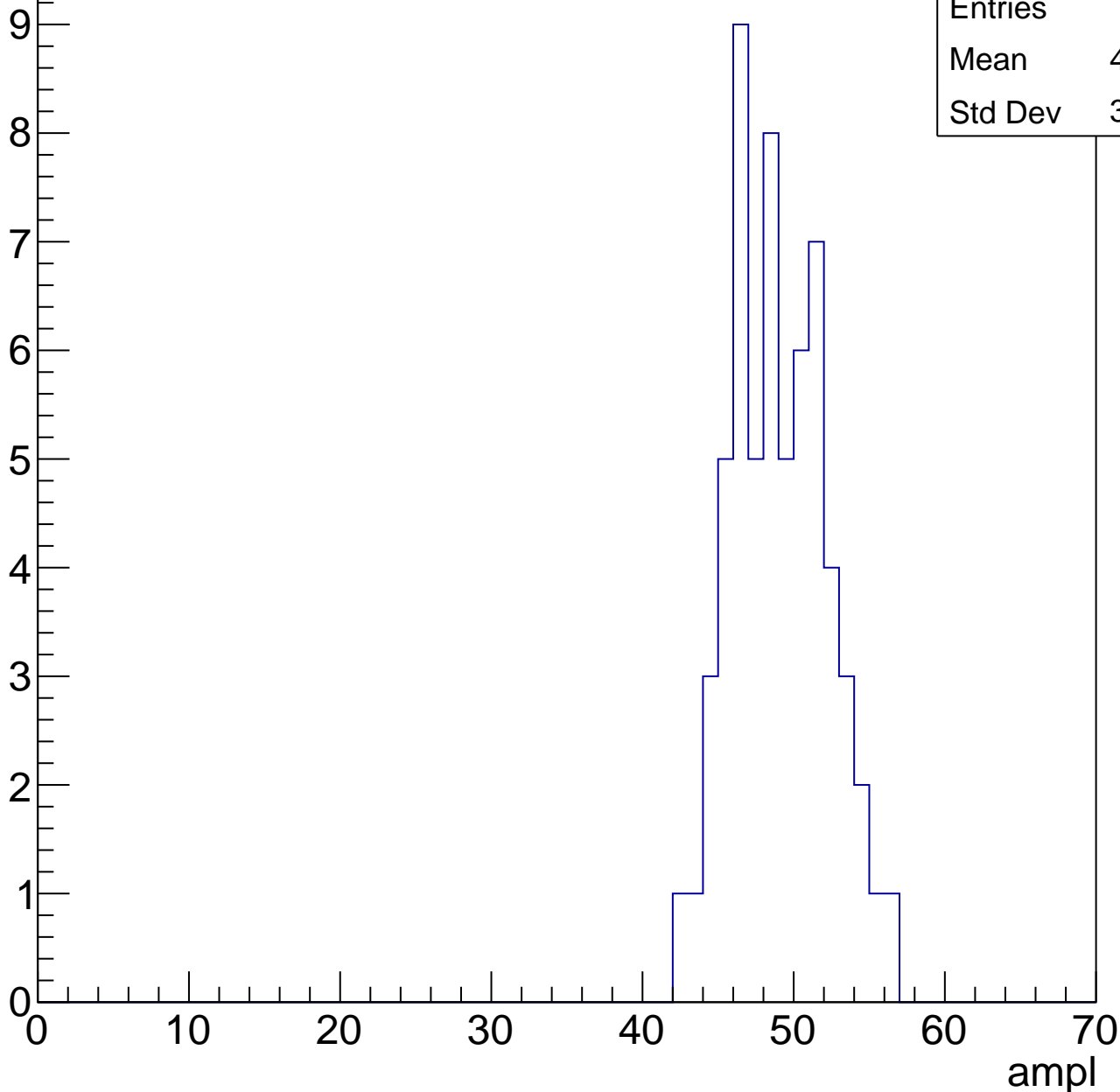


# B1L003S, U3-ch13, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

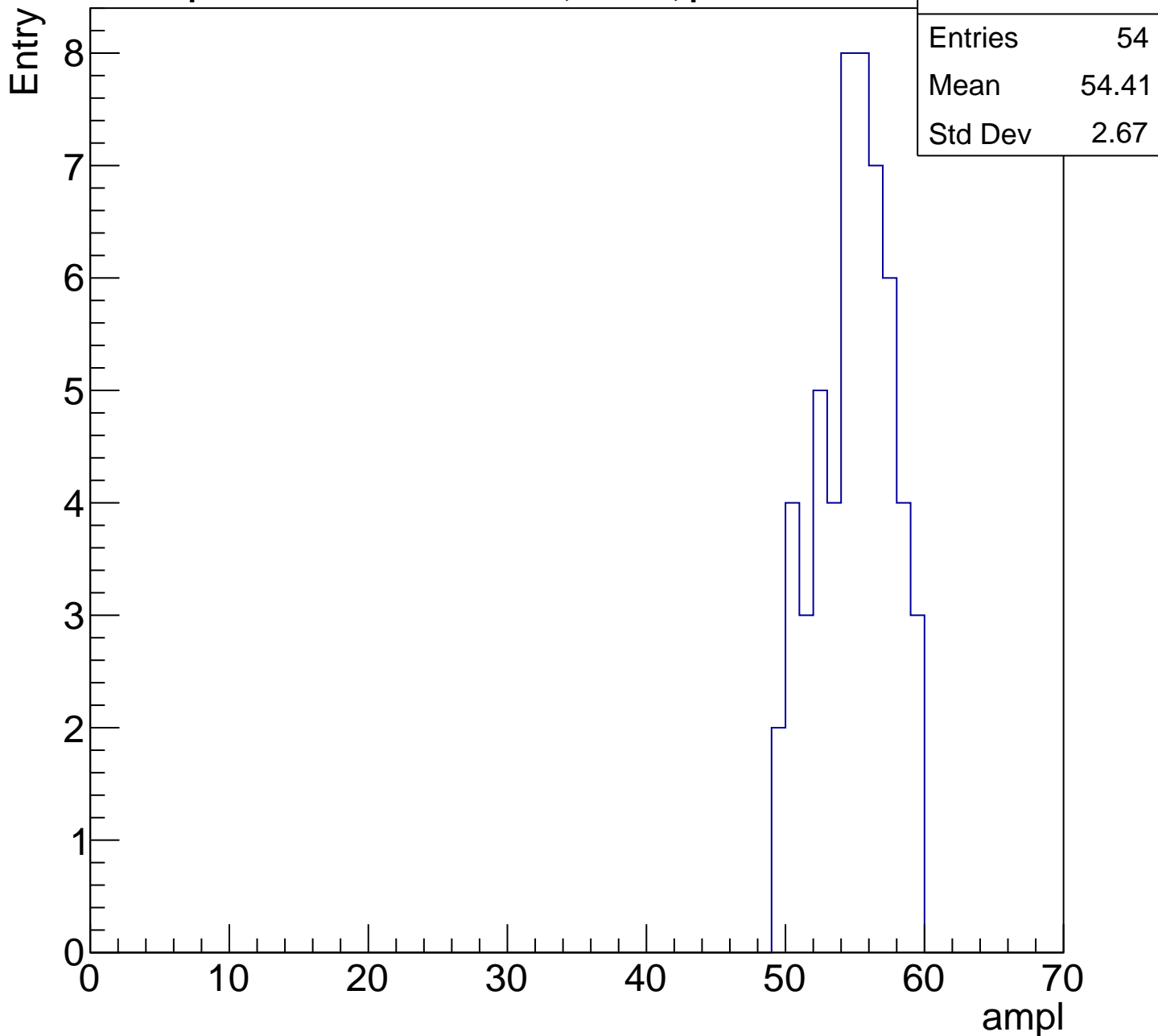
Entry

Entries	61
Mean	48.57
Std Dev	3.112



# B1L003S, U3-ch13, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2



# B1L003S, U3-ch13, adc5

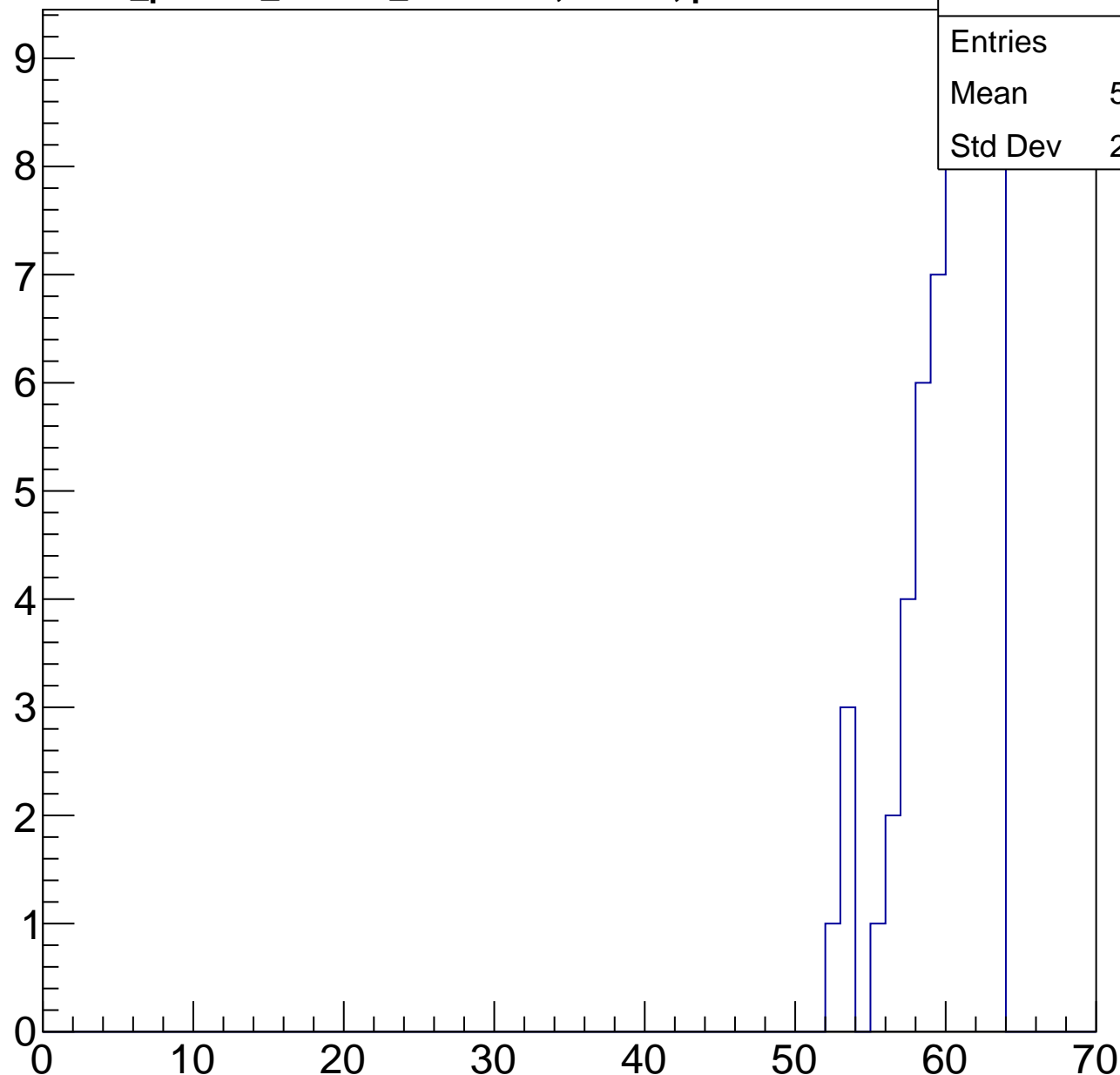
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	59
Mean	59.68
Std Dev	2.777

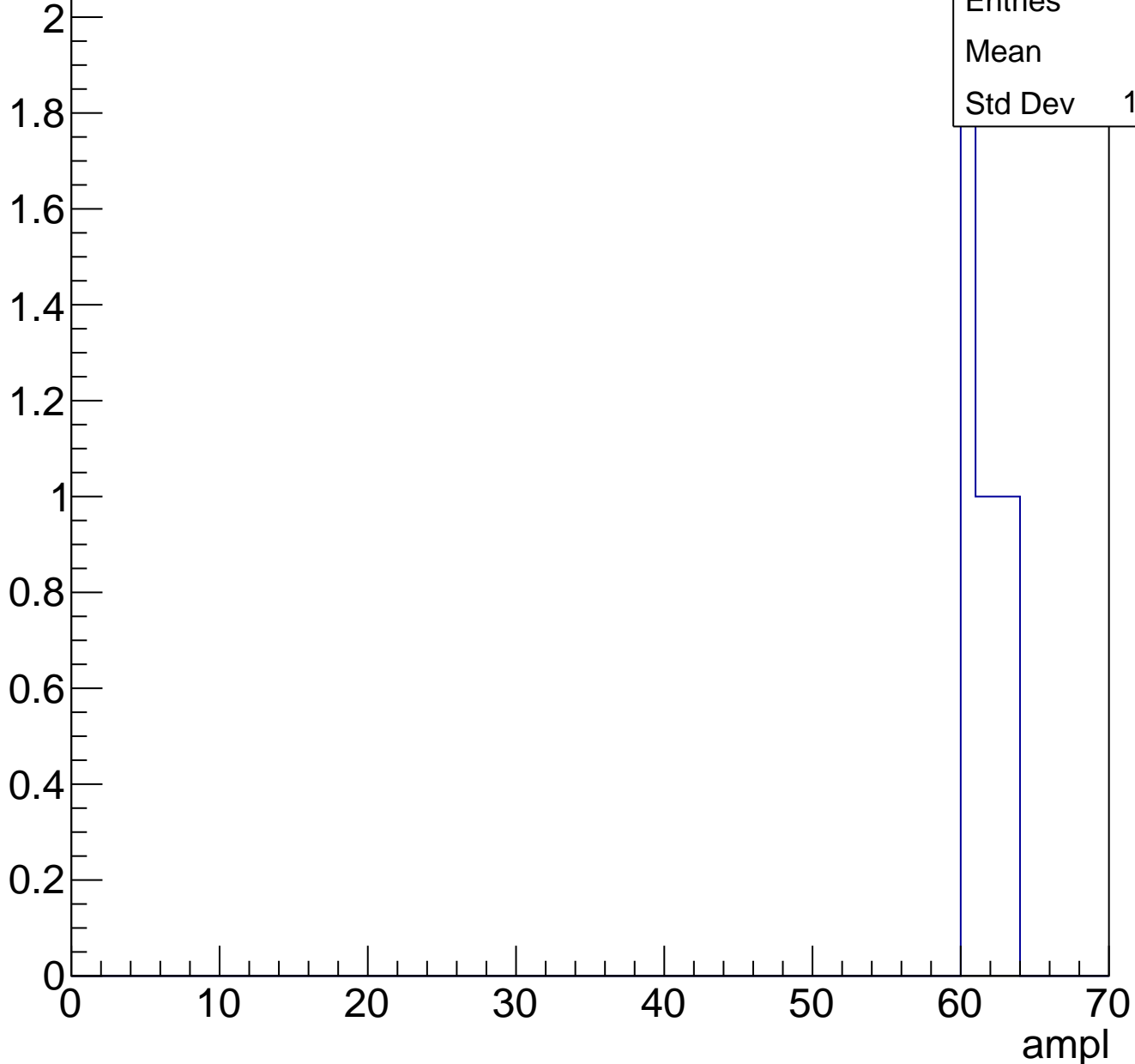
ampl



# B1L003S, U3-ch13, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	5
Mean	61.2
Std Dev	1.166



# B1L003S, U3-ch13, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U3-ch14, adc0

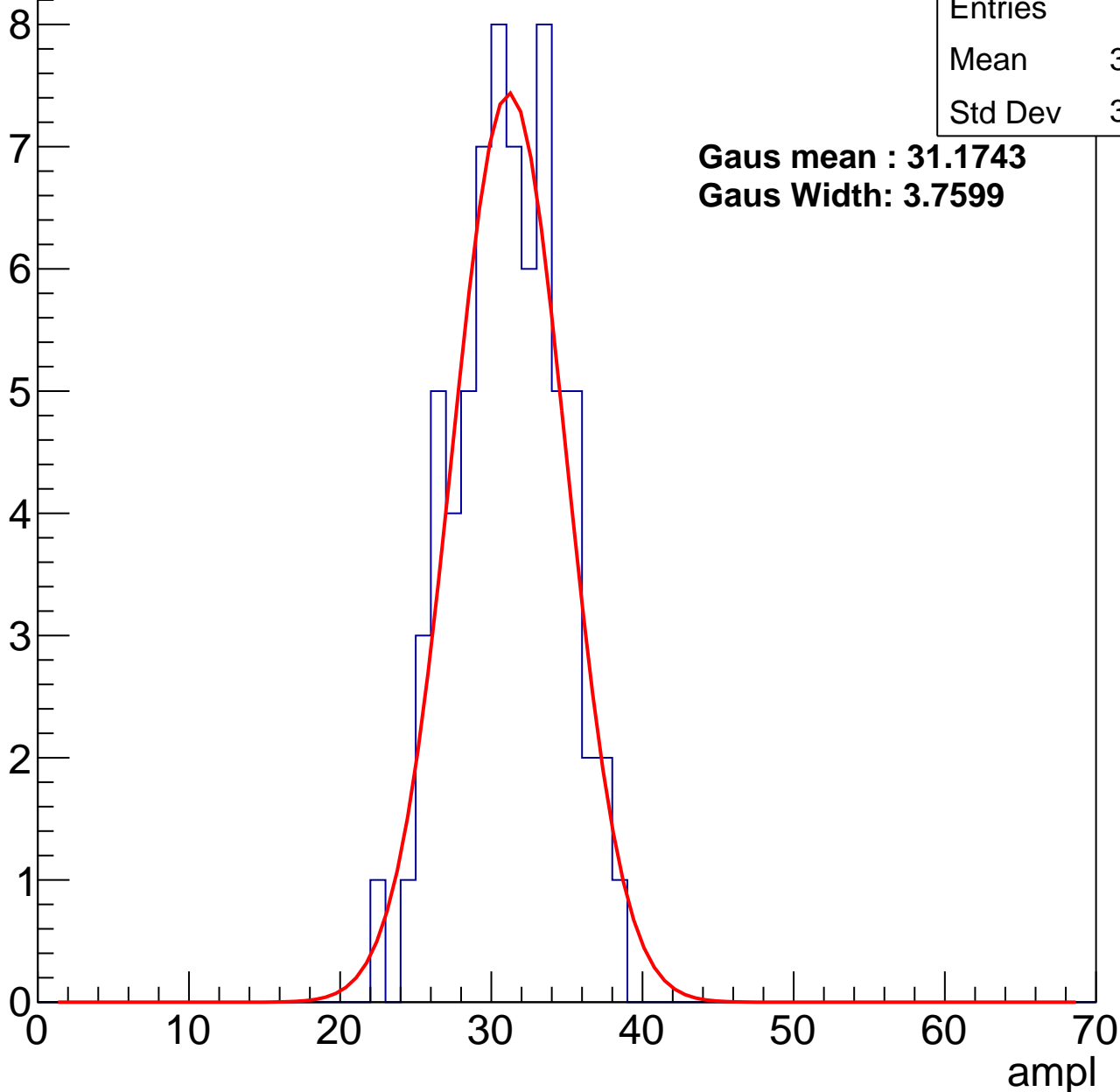
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	30.63
Std Dev	3.448

**Gaus mean : 31.1743**

**Gaus Width: 3.7599**



# B1L003S, U3-ch14, adc1

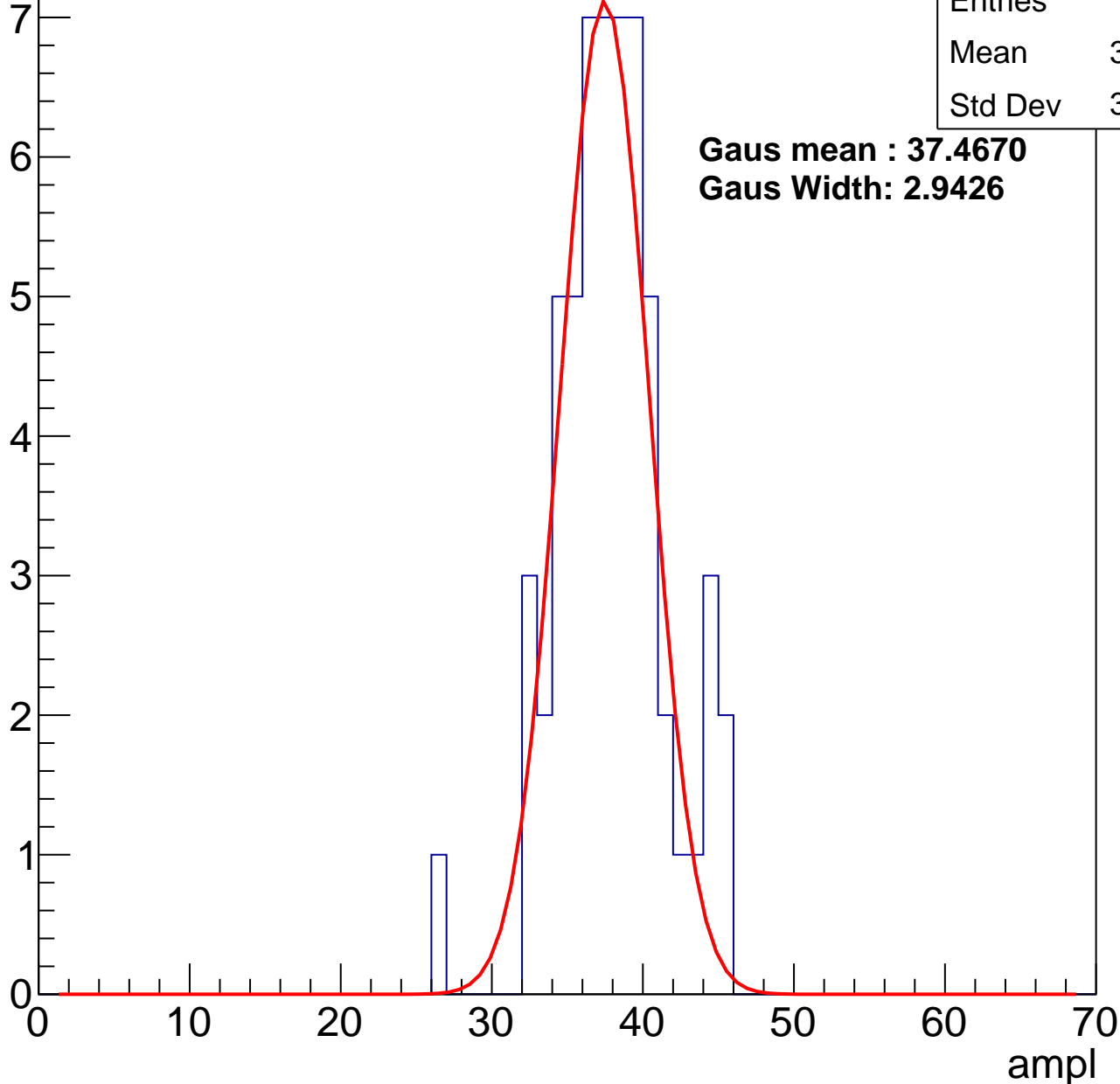
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	37.45
Std Dev	3.563

**Gaus mean : 37.4670**

**Gaus Width: 2.9426**



# B1L003S, U3-ch14, adc2

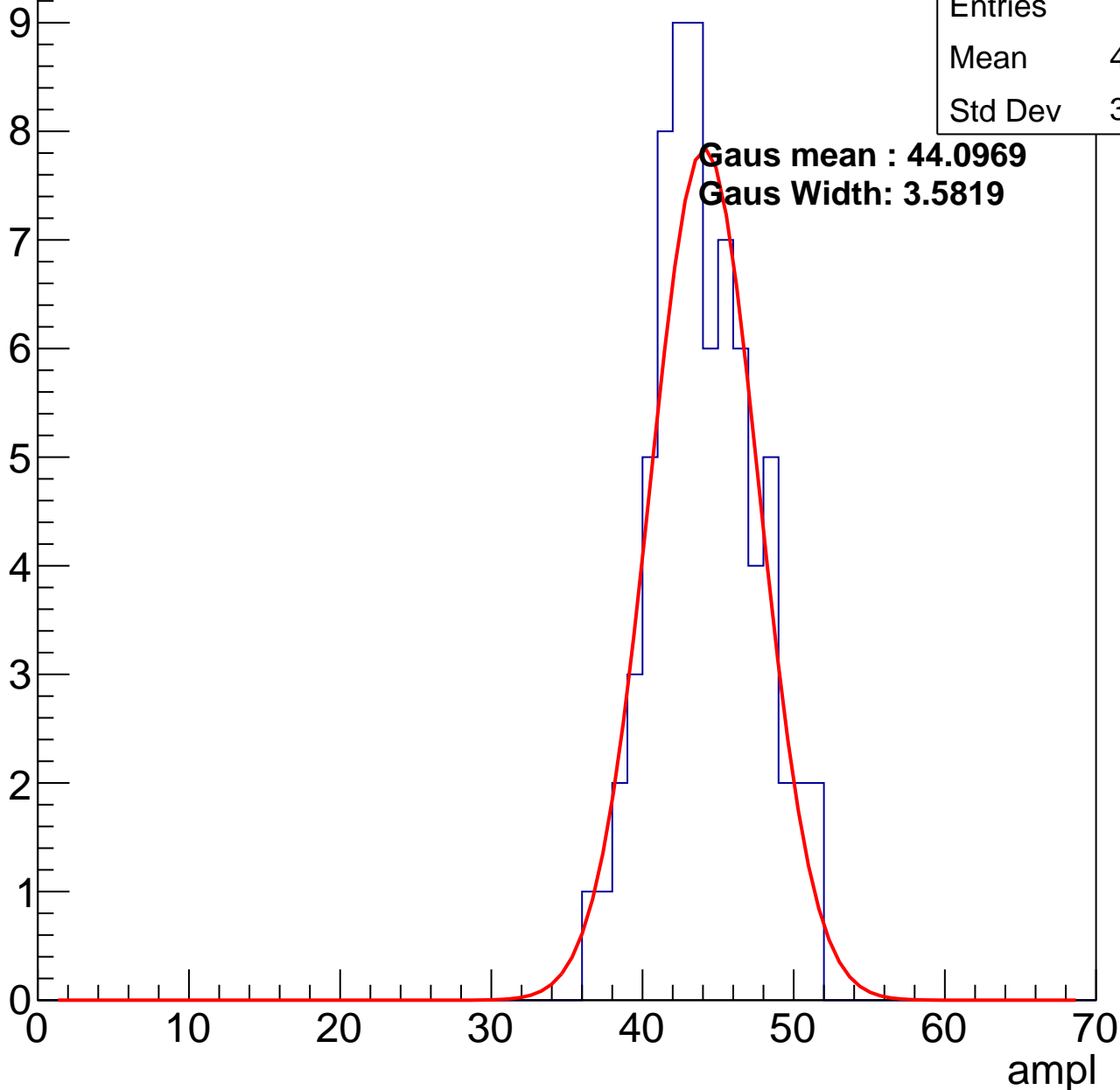
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	72
Mean	43.64
Std Dev	3.364

**Gaus mean : 44.0969**

**Gaus Width: 3.5819**

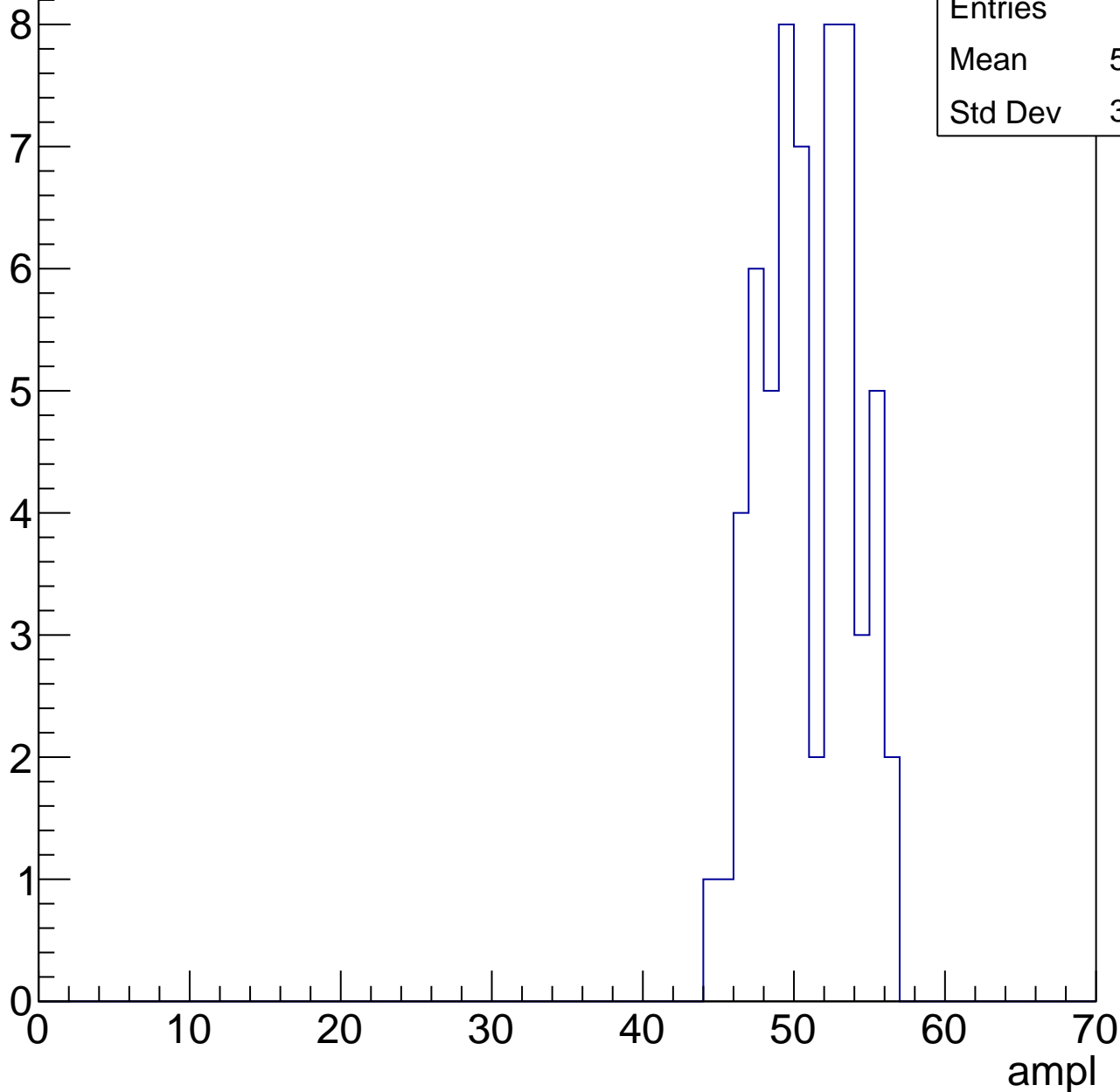


# B1L003S, U3-ch14, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

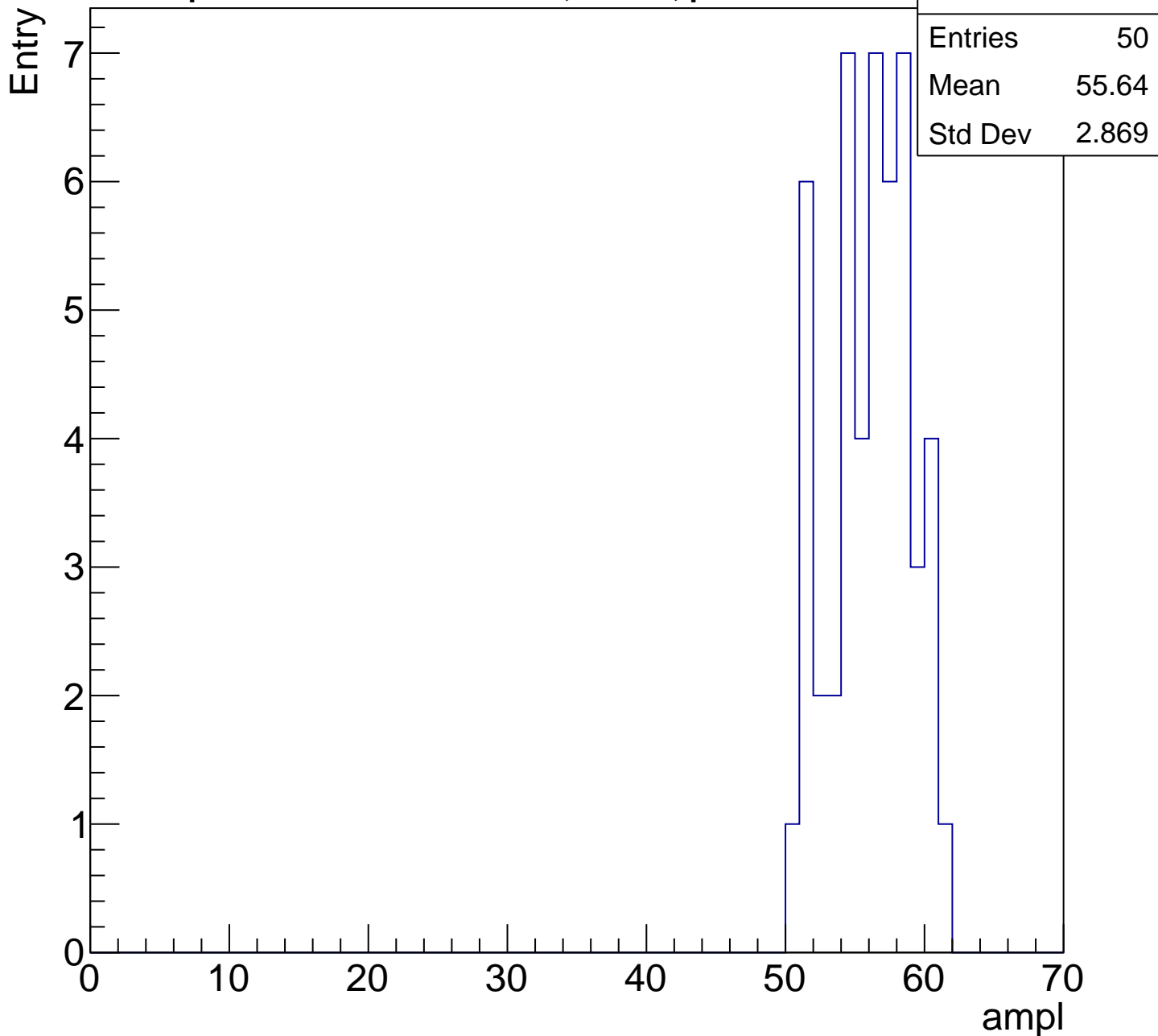
Entry

Entries	60
Mean	50.47
Std Dev	3.014



# B1L003S, U3-ch14, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

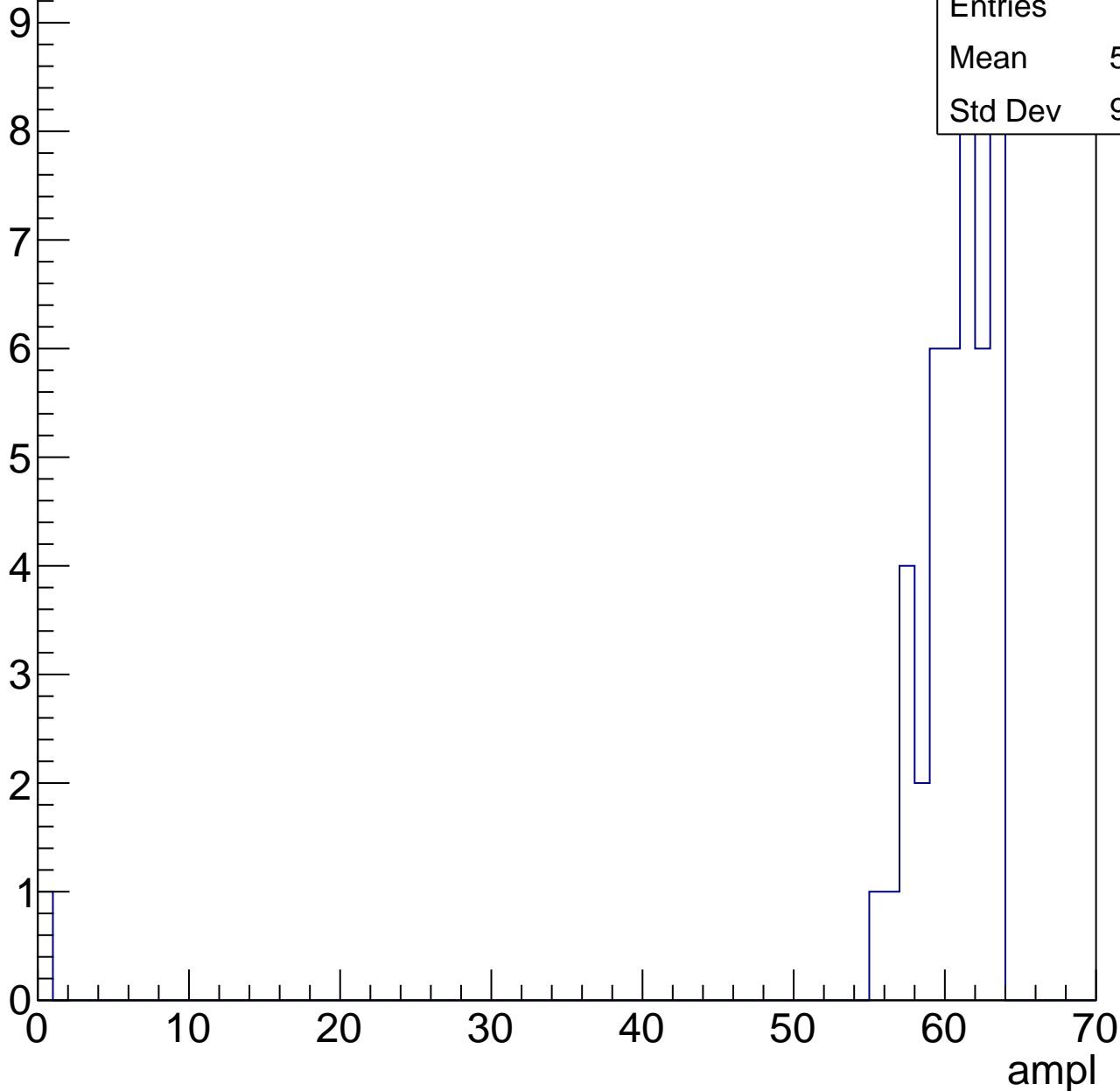


# B1L003S, U3-ch14, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

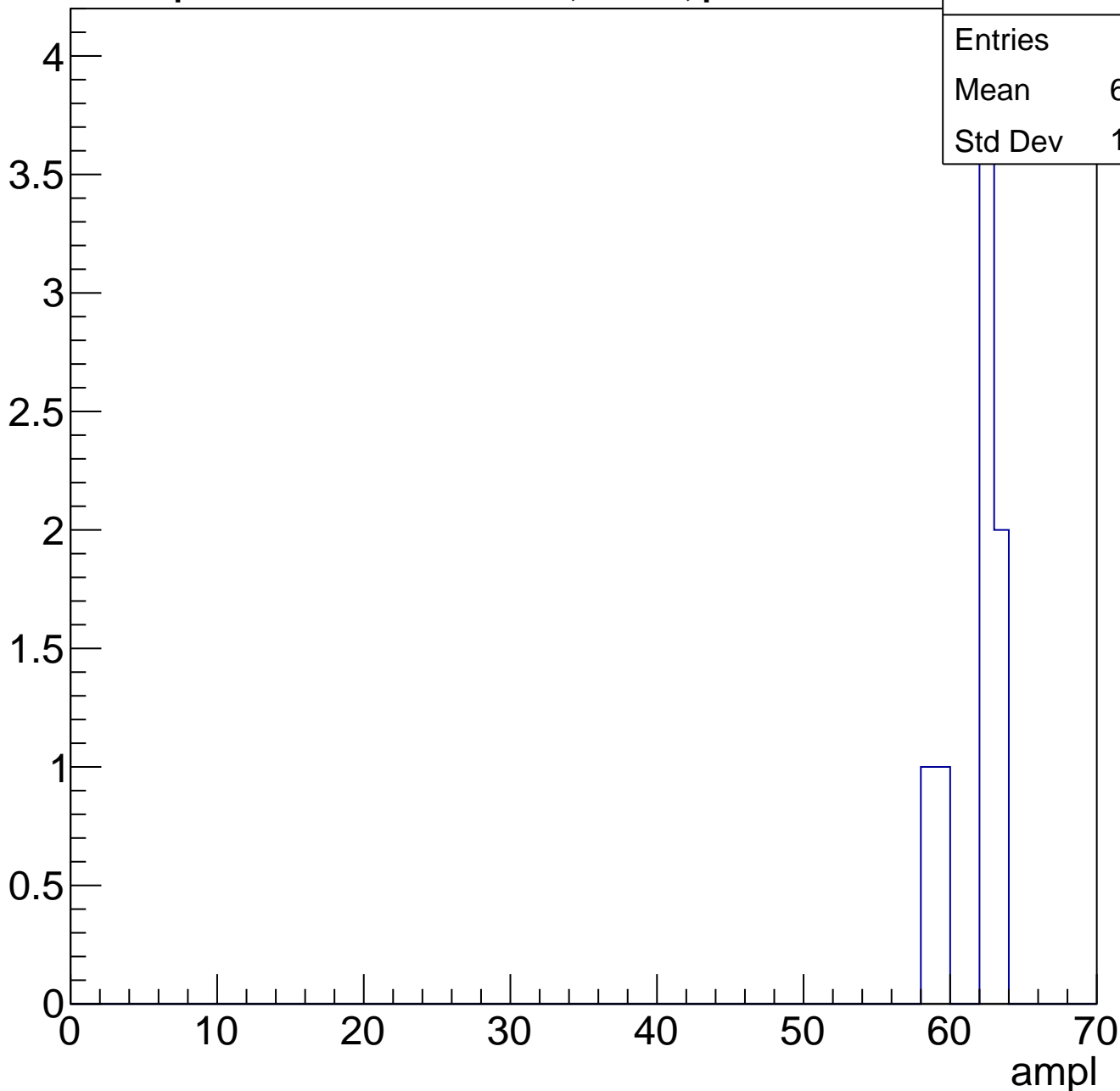
Entries	44
Mean	58.95
Std Dev	9.229



# B1L003S, U3-ch14, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

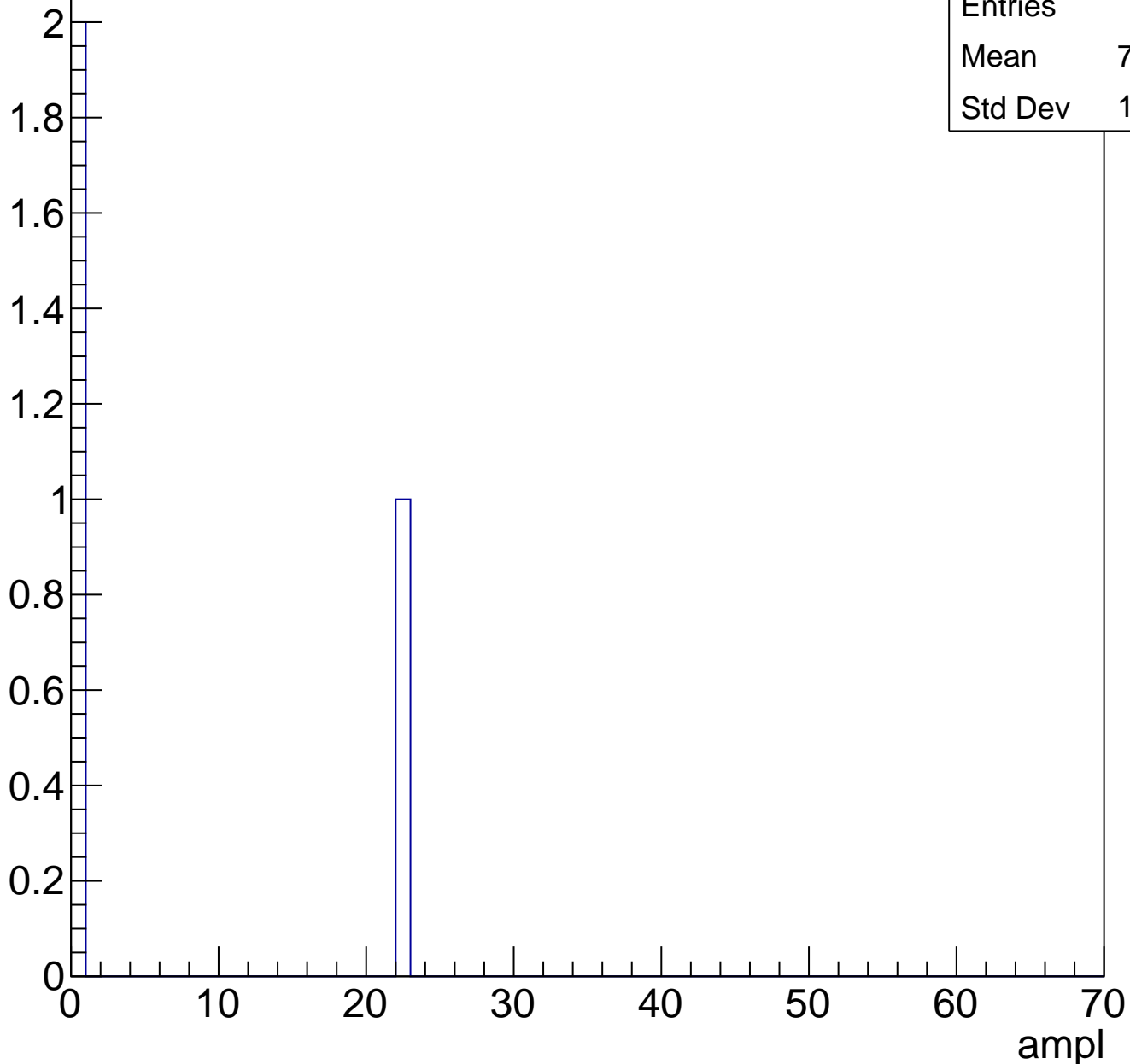




# B1L003S, U3-ch14, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	3
Mean	7.333
Std Dev	10.37

# B1L003S, U3-ch15, adc0

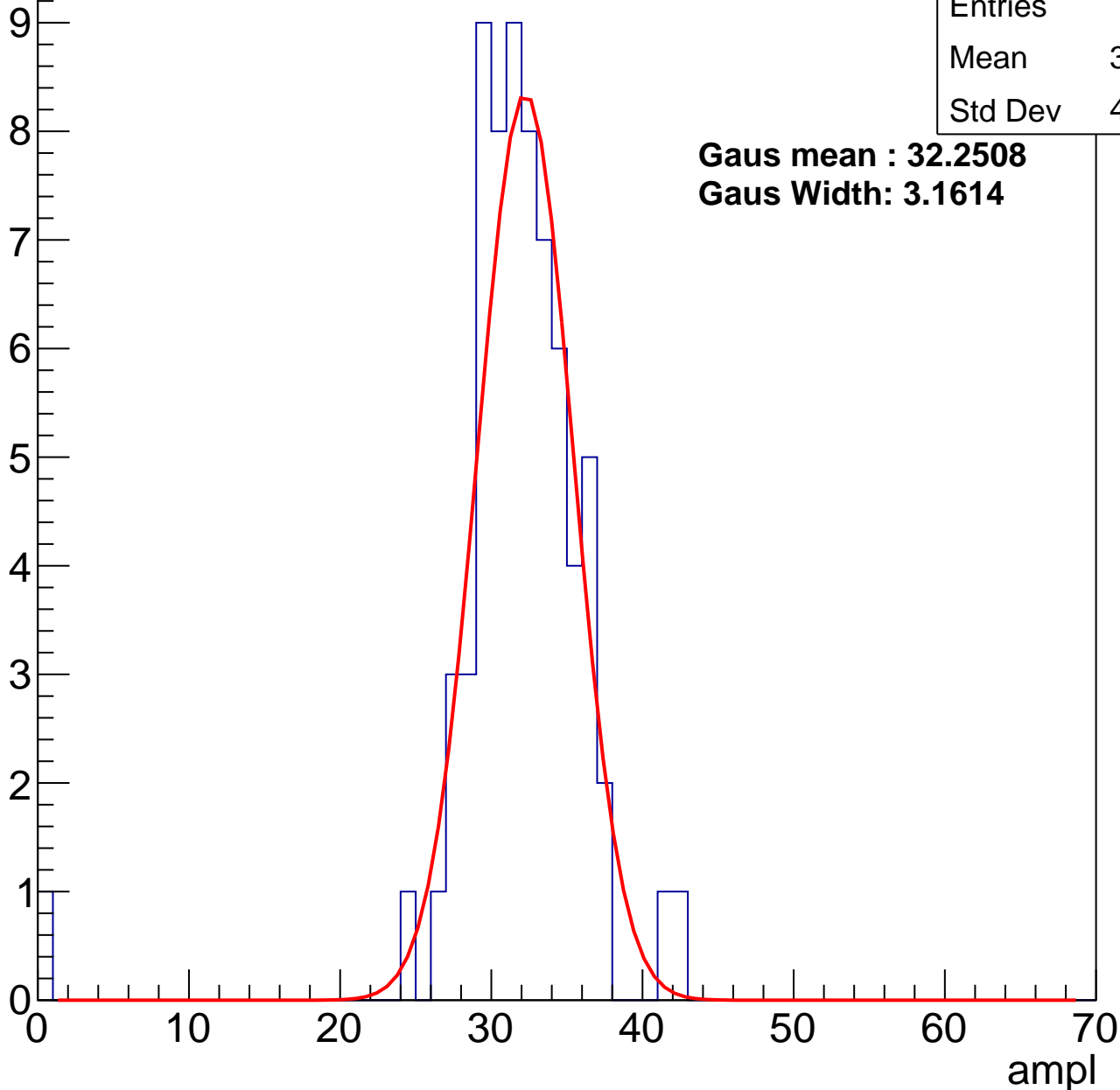
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	31.35
Std Dev	4.989

**Gaus mean : 32.2508**

**Gaus Width: 3.1614**



# B1L003S, U3-ch15, adc1

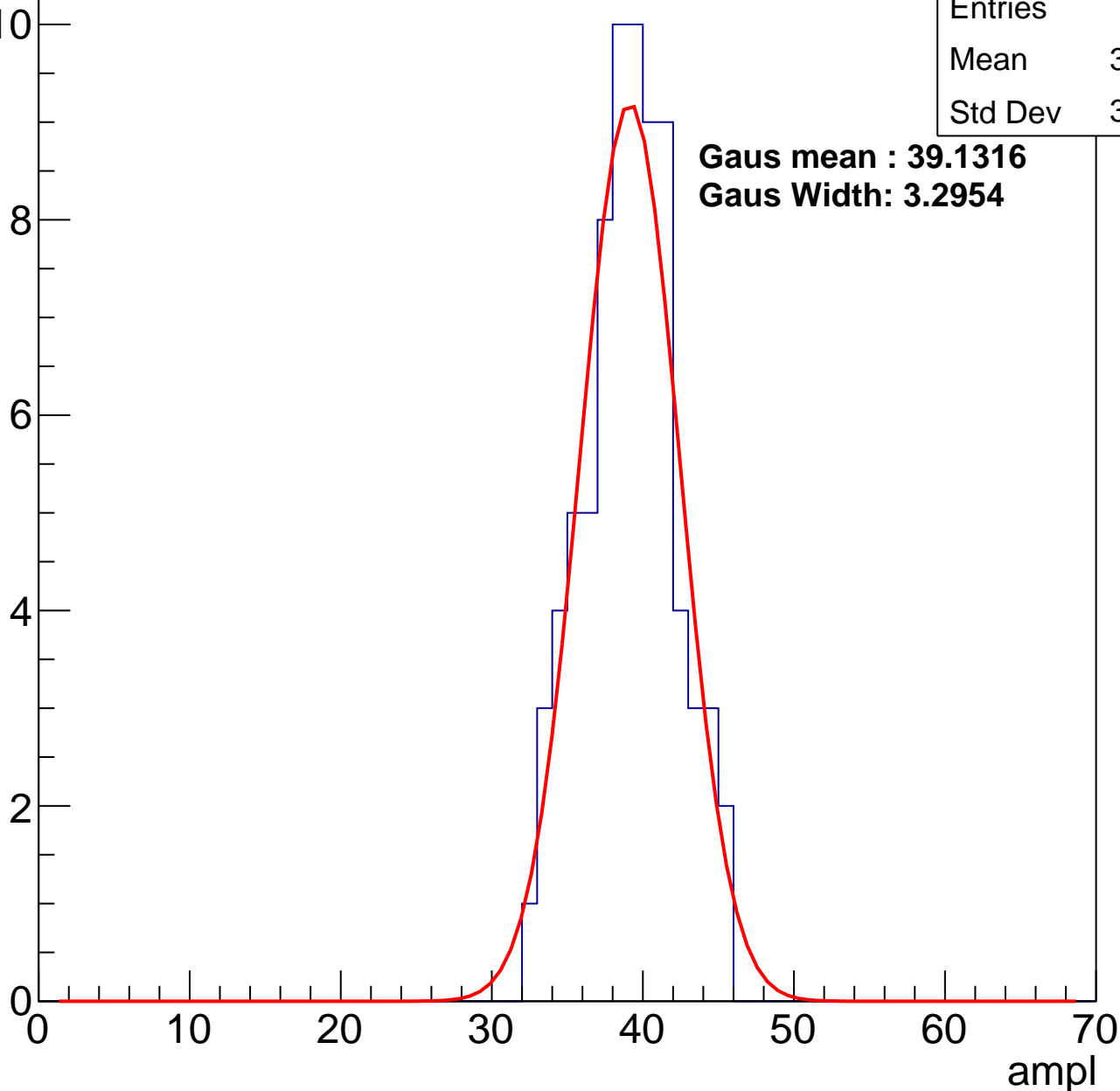
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	76
Mean	38.63
Std Dev	3.012

**Gaus mean : 39.1316**

**Gaus Width: 3.2954**



# B1L003S, U3-ch15, adc2

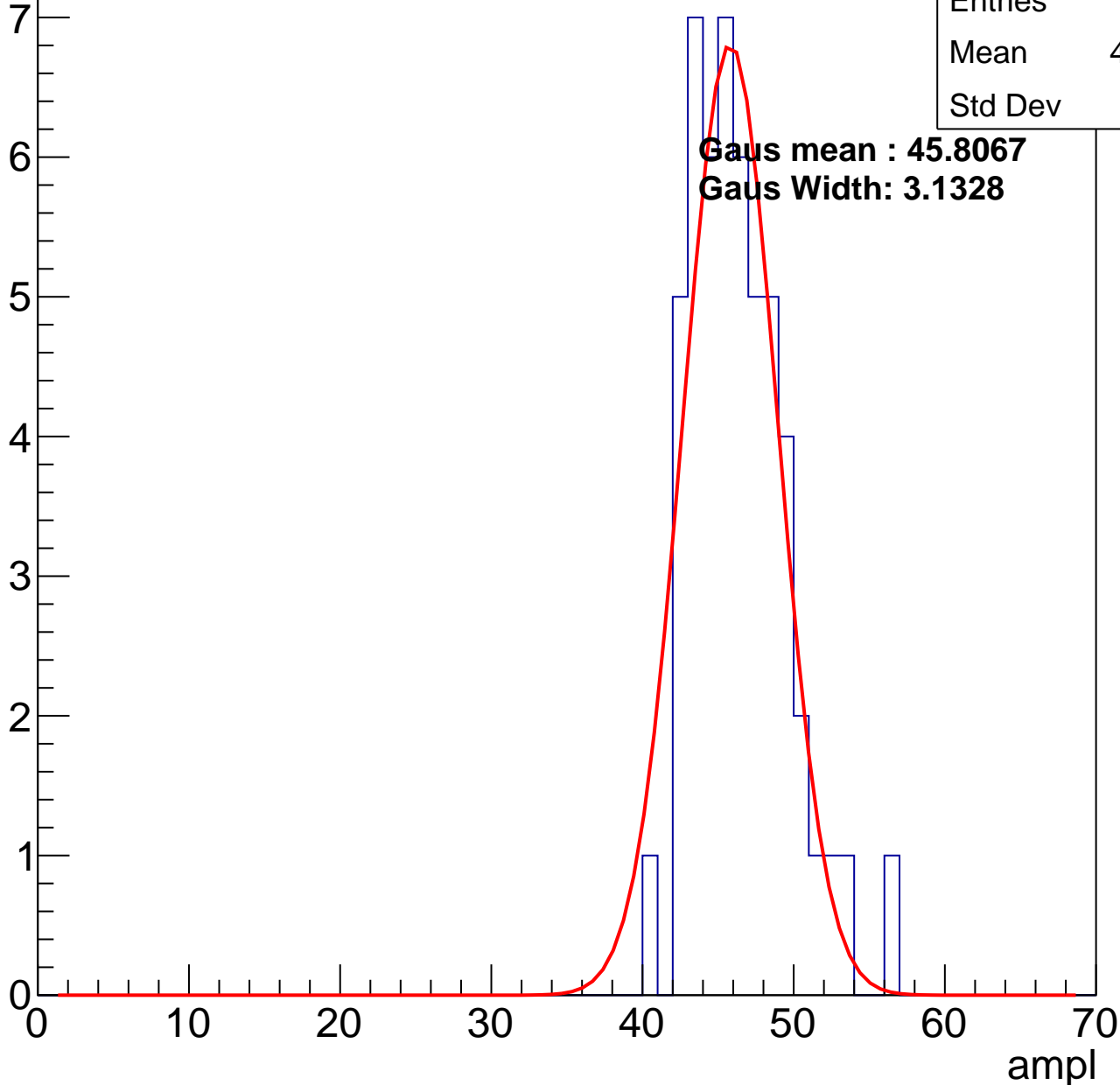
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	52
Mean	45.94
Std Dev	3.14

**Gaus mean : 45.8067**

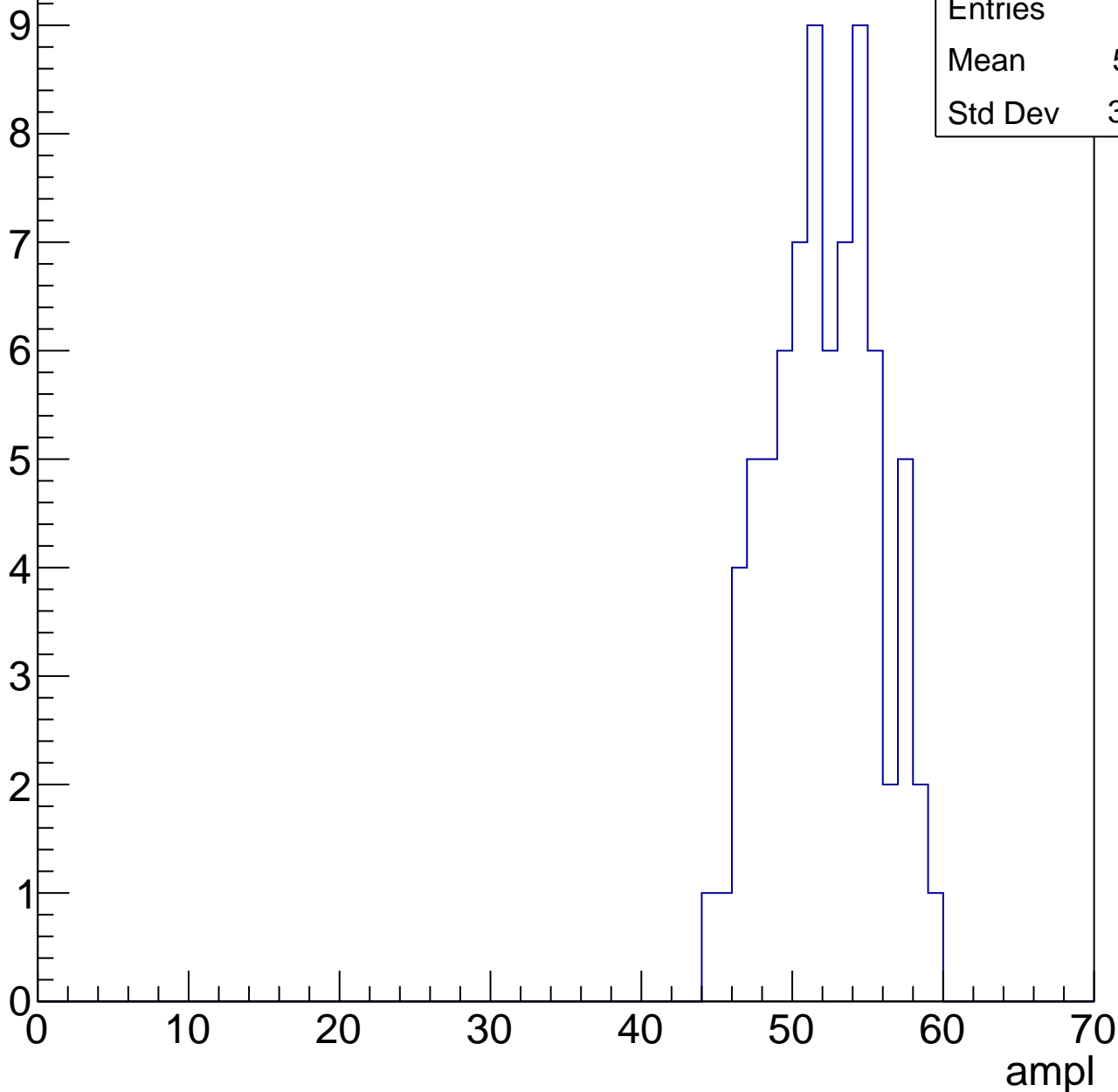
**Gaus Width: 3.1328**



# B1L003S, U3-ch15, adc3

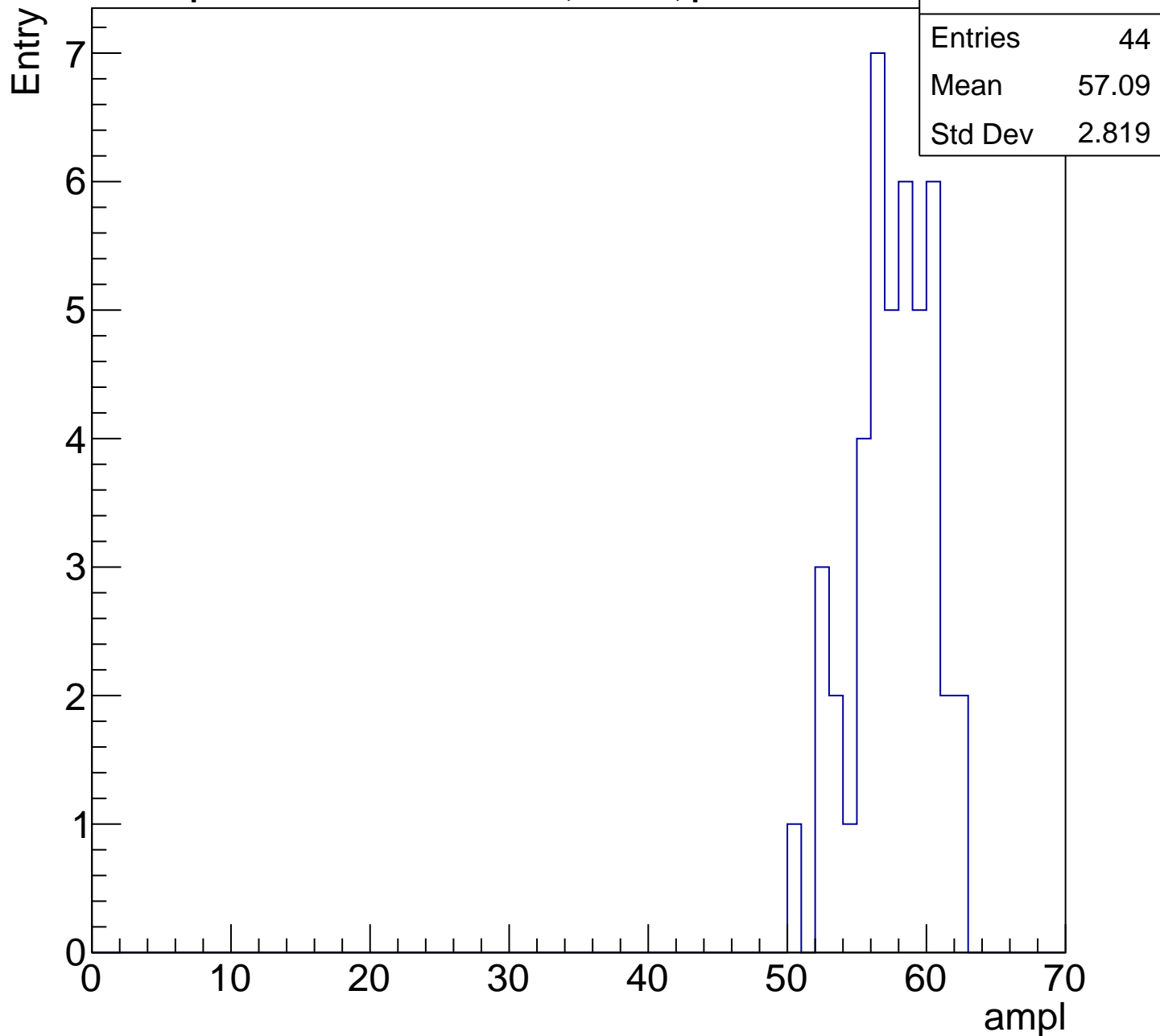
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U3-ch15, adc4

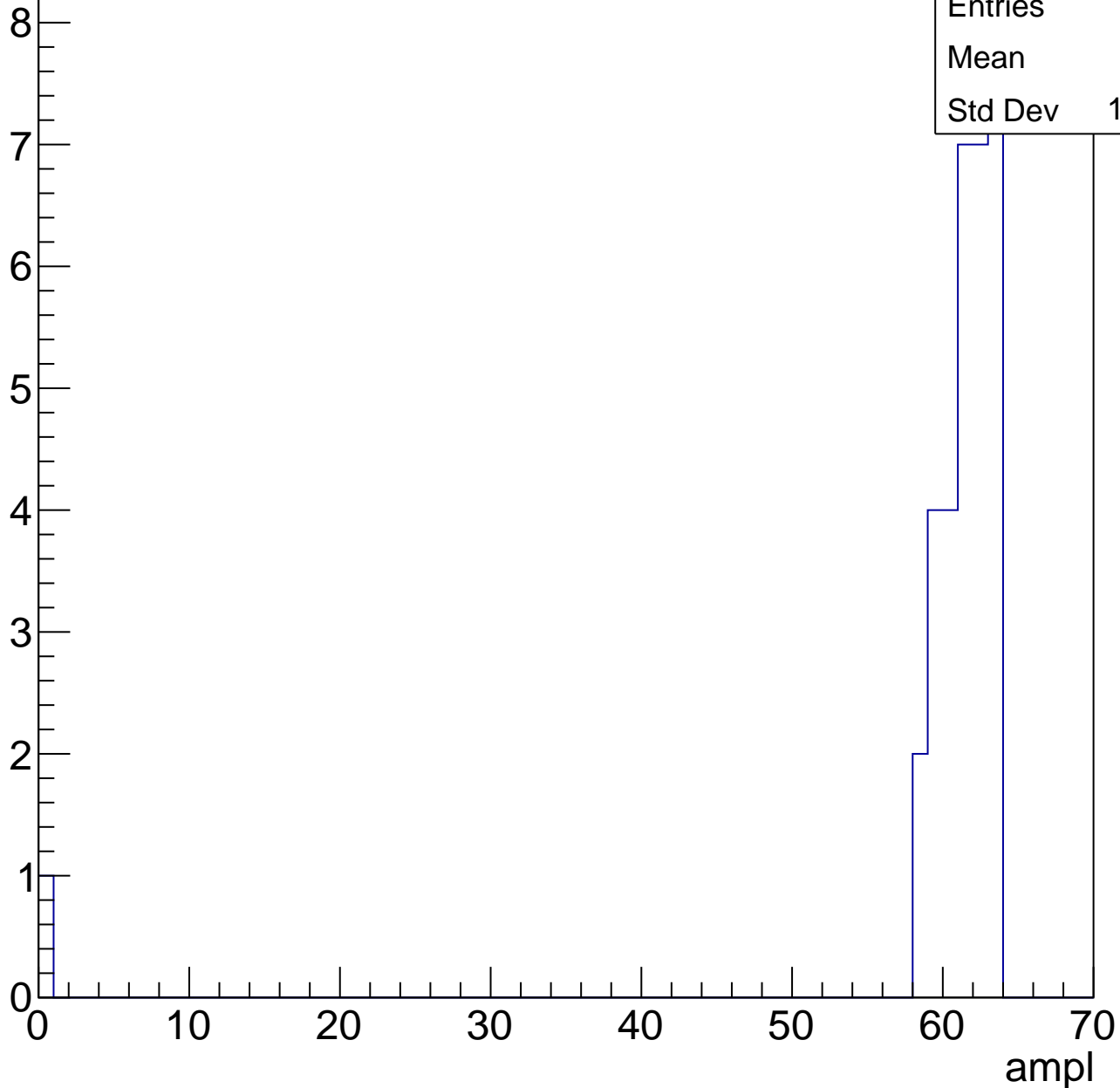
calib\_packv5\_042523\_0143.root, FC#13, port D2



# B1L003S, U3-ch15, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U3-ch15, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch15, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U3-ch16, adc0

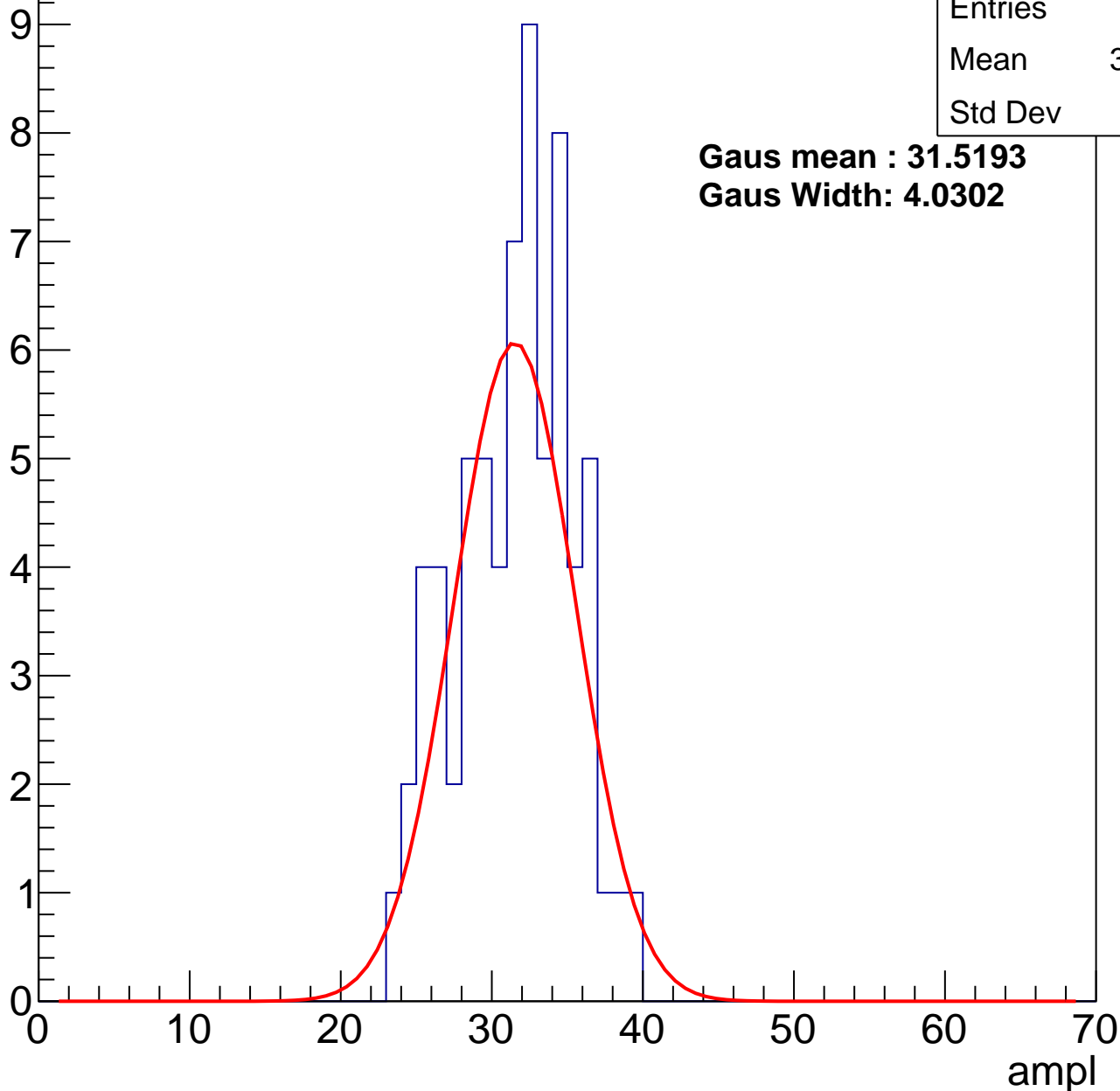
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	31.03
Std Dev	3.73

**Gaus mean : 31.5193**

**Gaus Width: 4.0302**



# B1L003S, U3-ch16, adc1

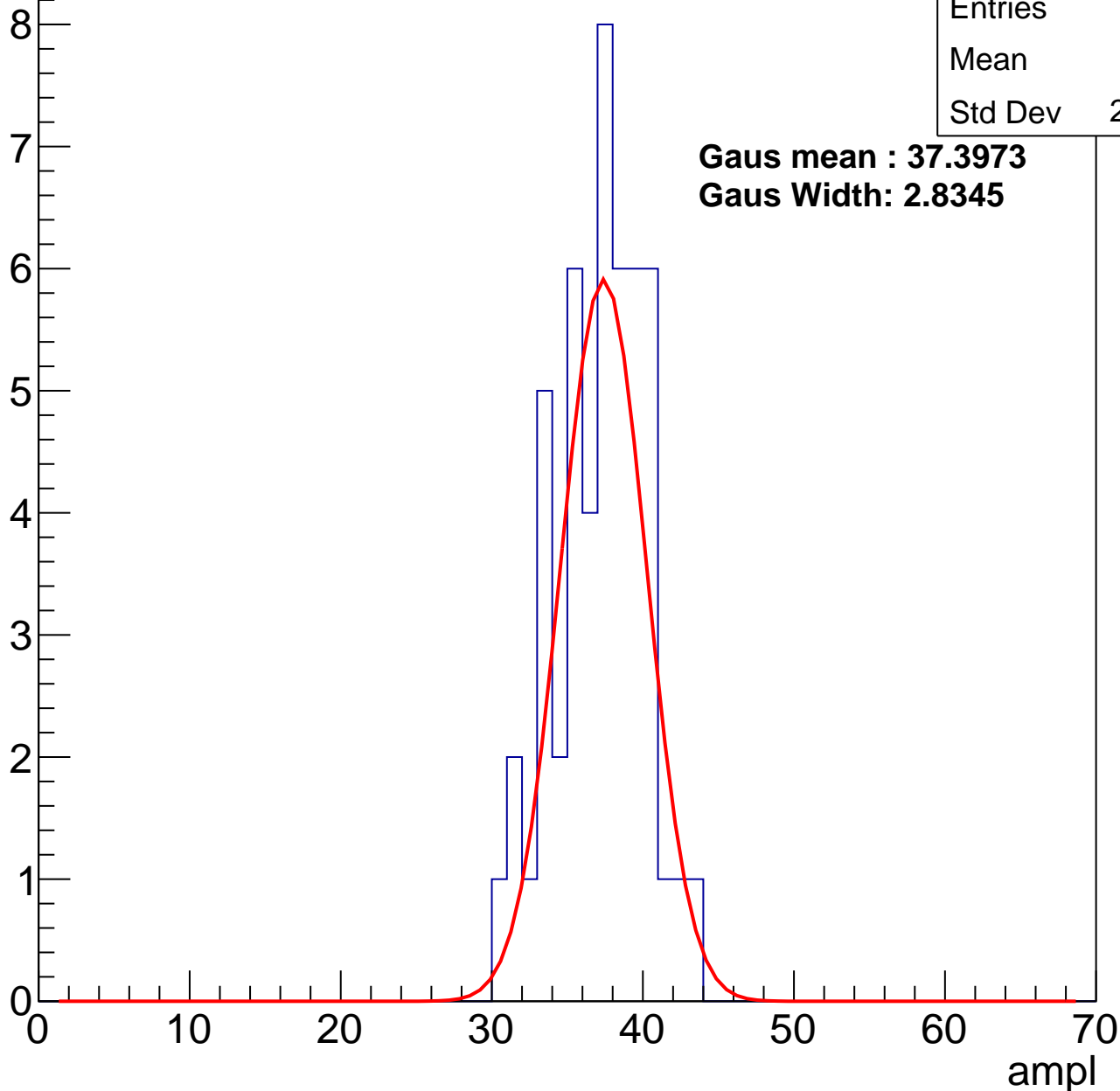
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	50
Mean	36.7
Std Dev	2.927

**Gaus mean : 37.3973**

**Gaus Width: 2.8345**



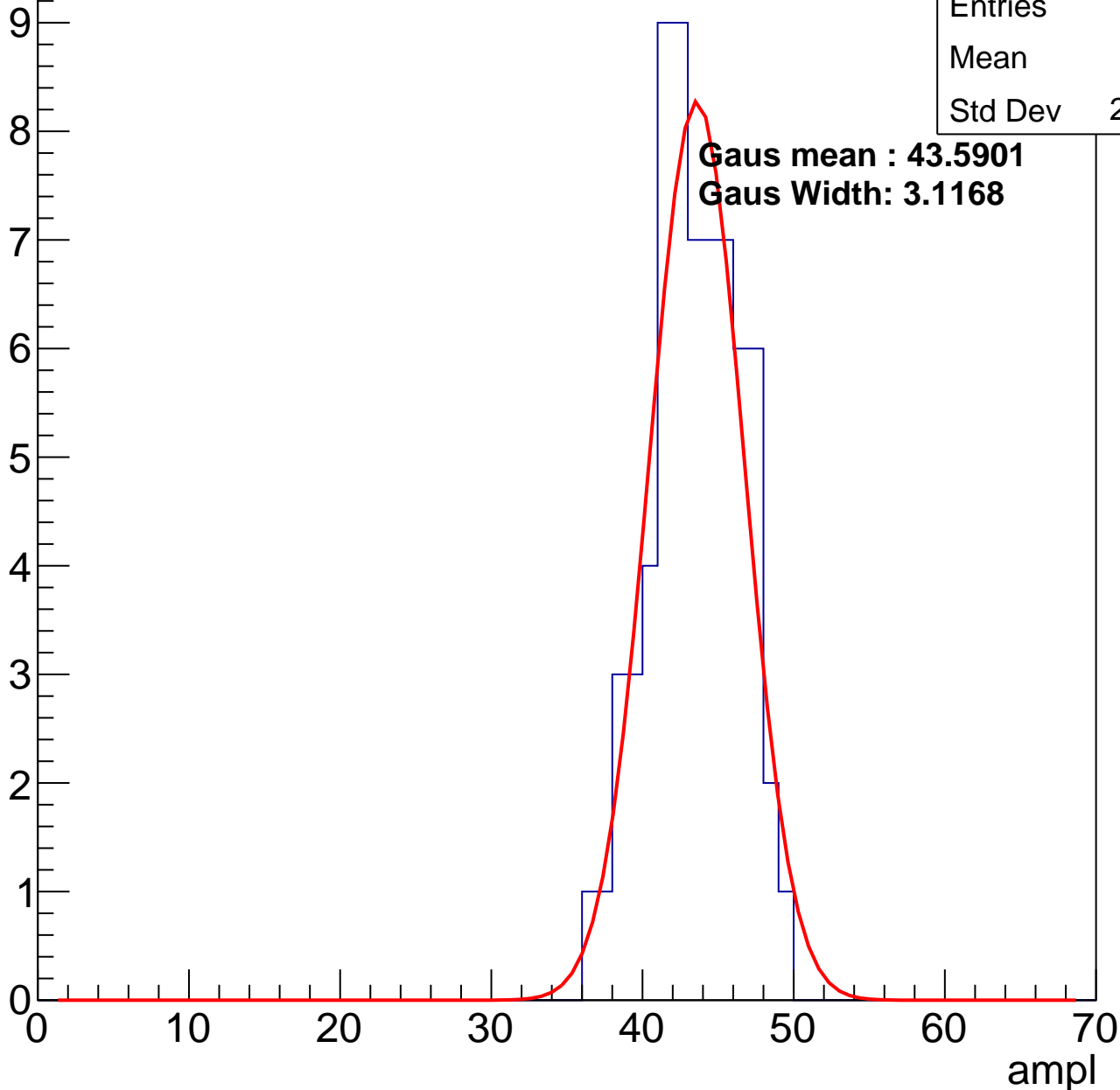
# B1L003S, U3-ch16, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	43
Std Dev	2.913

**Gaus mean : 43.5901**  
**Gaus Width: 3.1168**



# B1L003S, U3-ch16, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	79
Mean	50.35
Std Dev	3.6

Entry

10

8

6

4

2

0

0

10

20

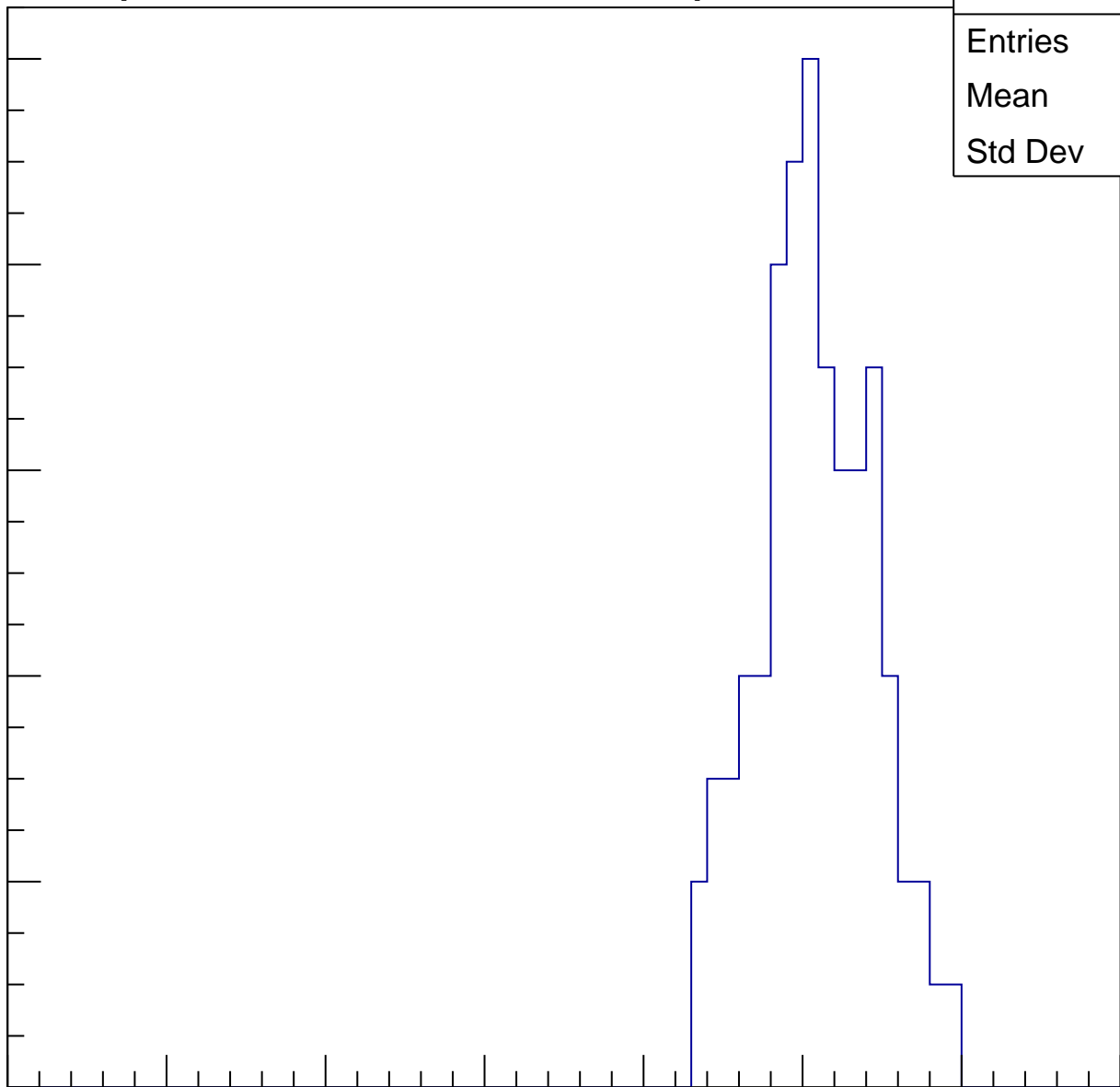
30

40

50

60

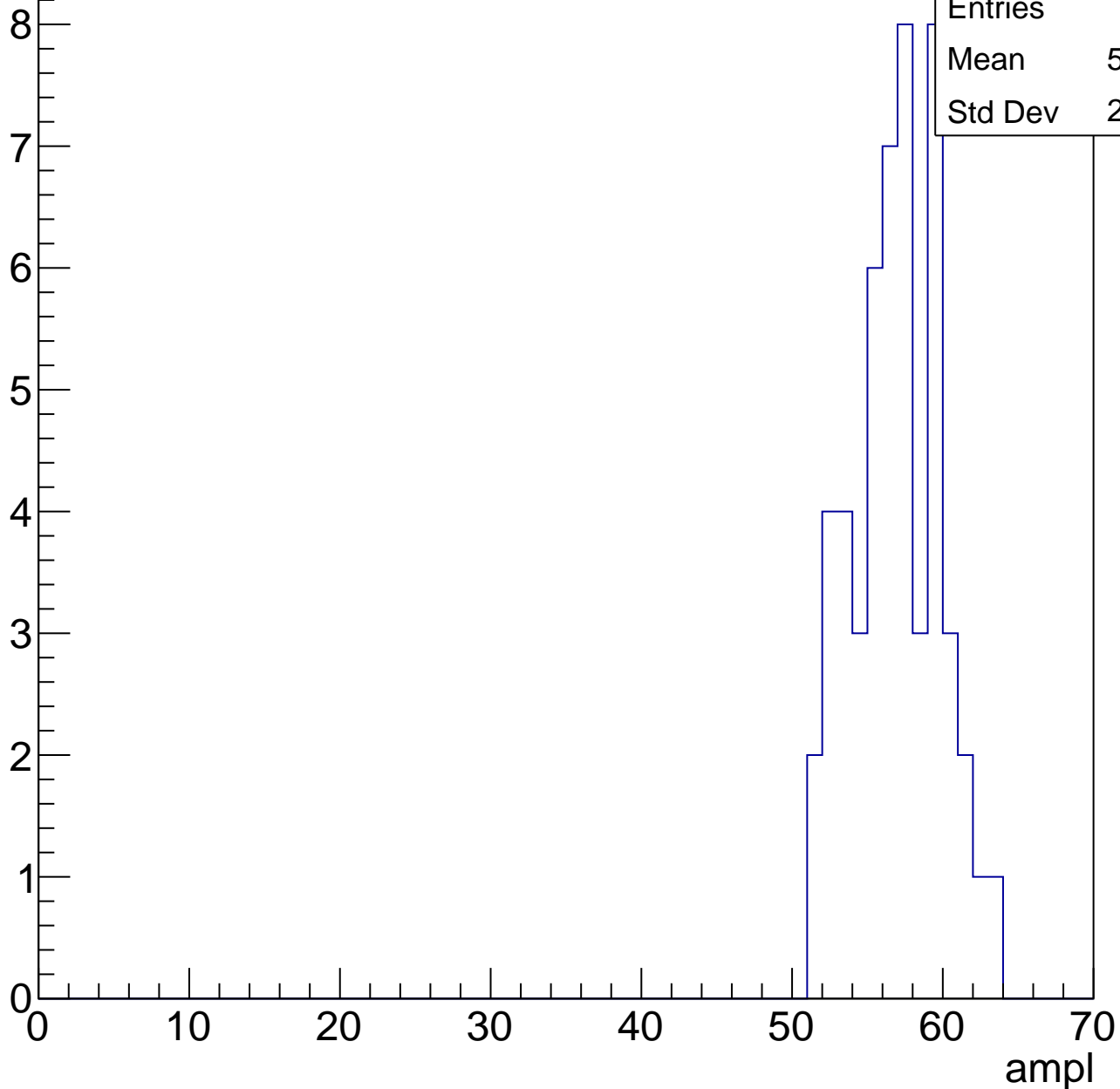
ampl



# B1L003S, U3-ch16, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



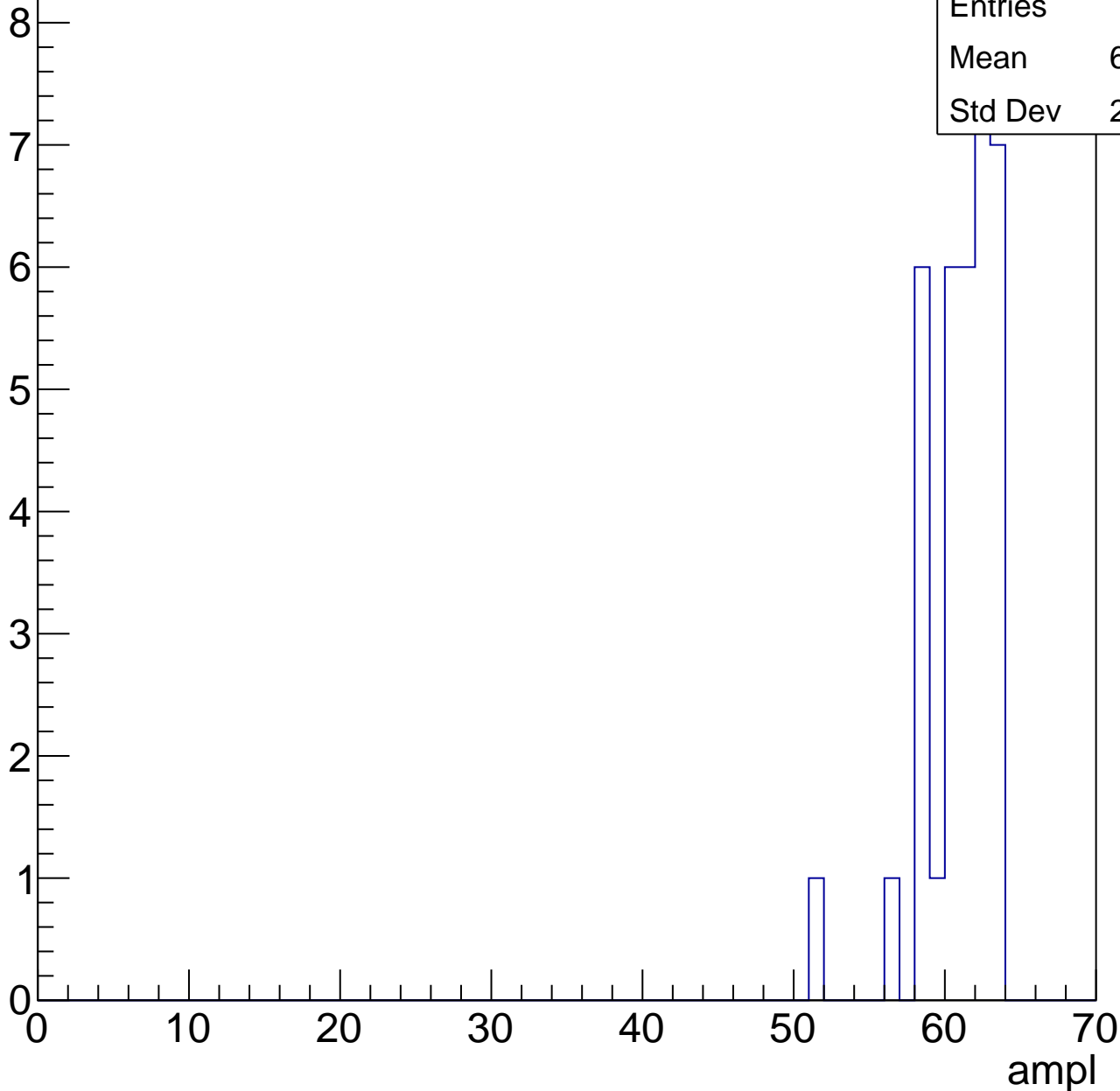
Entries	52
Mean	56.44
Std Dev	2.885

# B1L003S, U3-ch16, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	36
Mean	60.47
Std Dev	2.444



# B1L003S, U3-ch16, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

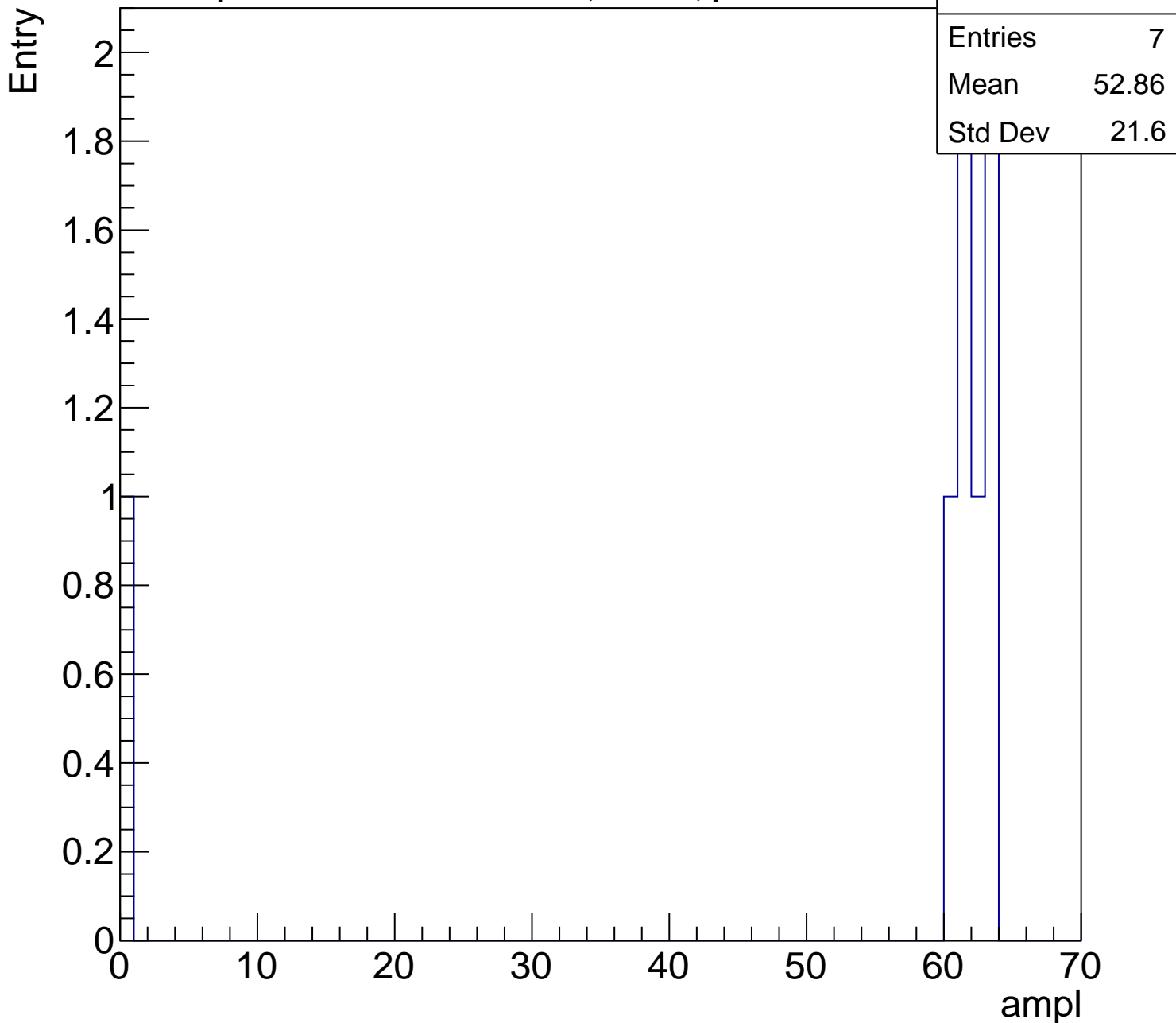
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	7
Mean	52.86
Std Dev	21.6

0 10 20 30 40 50 60 70

ampl





# B1L003S, U3-ch16, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L003S, U3-ch17, adc0

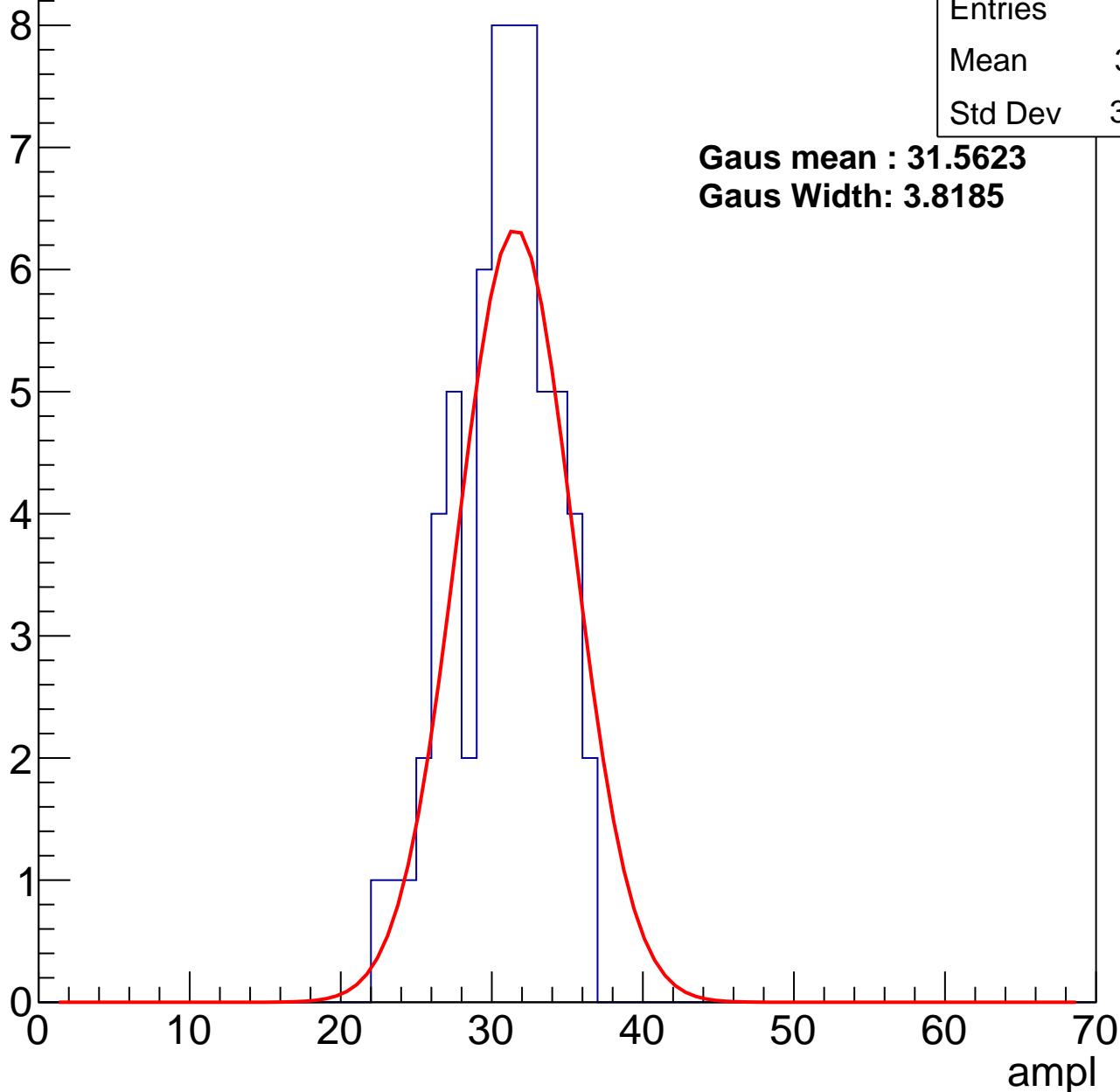
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	30.31
Std Dev	3.246

**Gaus mean : 31.5623**

**Gaus Width: 3.8185**



# B1L003S, U3-ch17, adc1

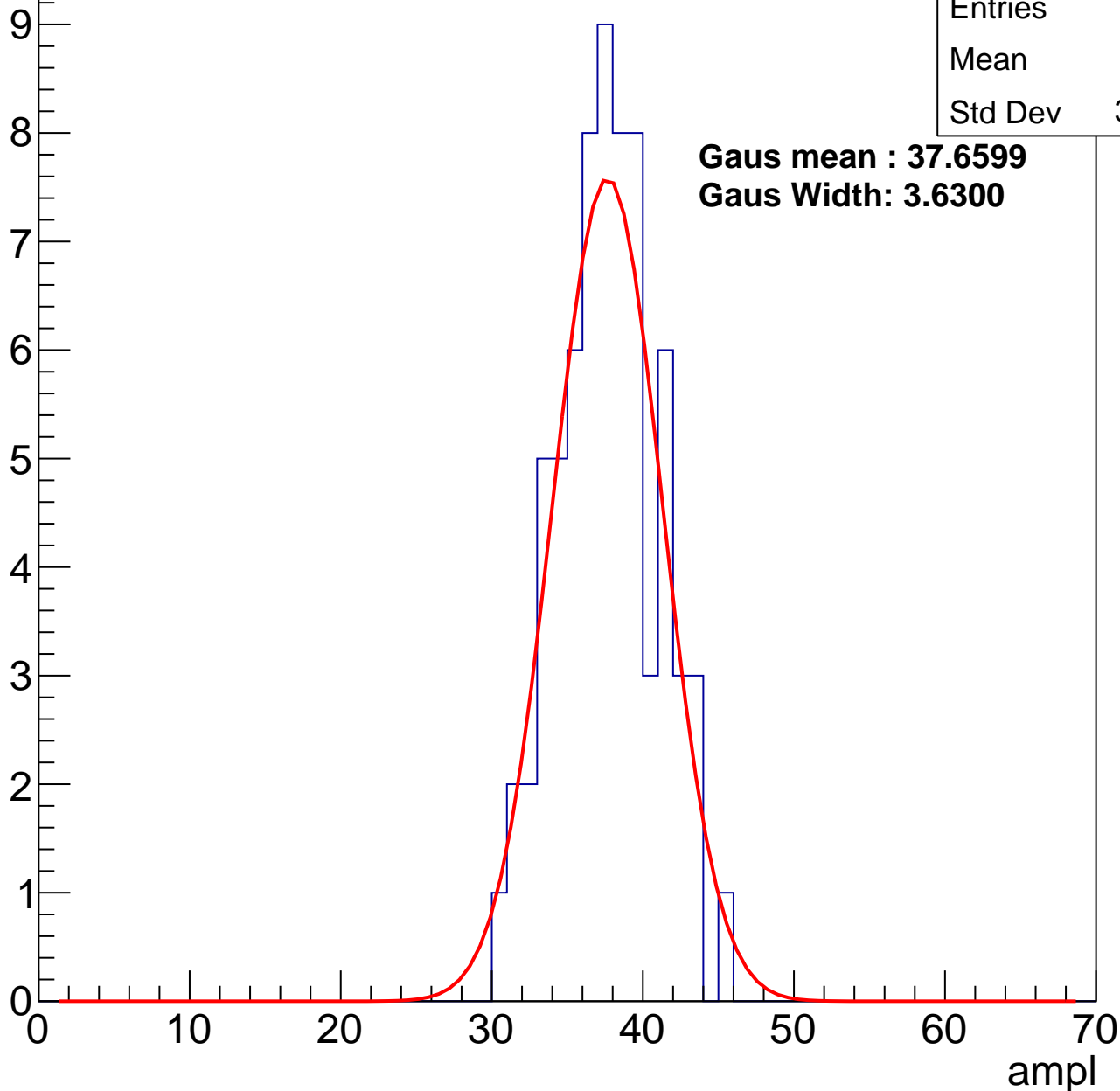
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	37.2
Std Dev	3.241

**Gaus mean : 37.6599**

**Gaus Width: 3.6300**



# B1L003S, U3-ch17, adc2

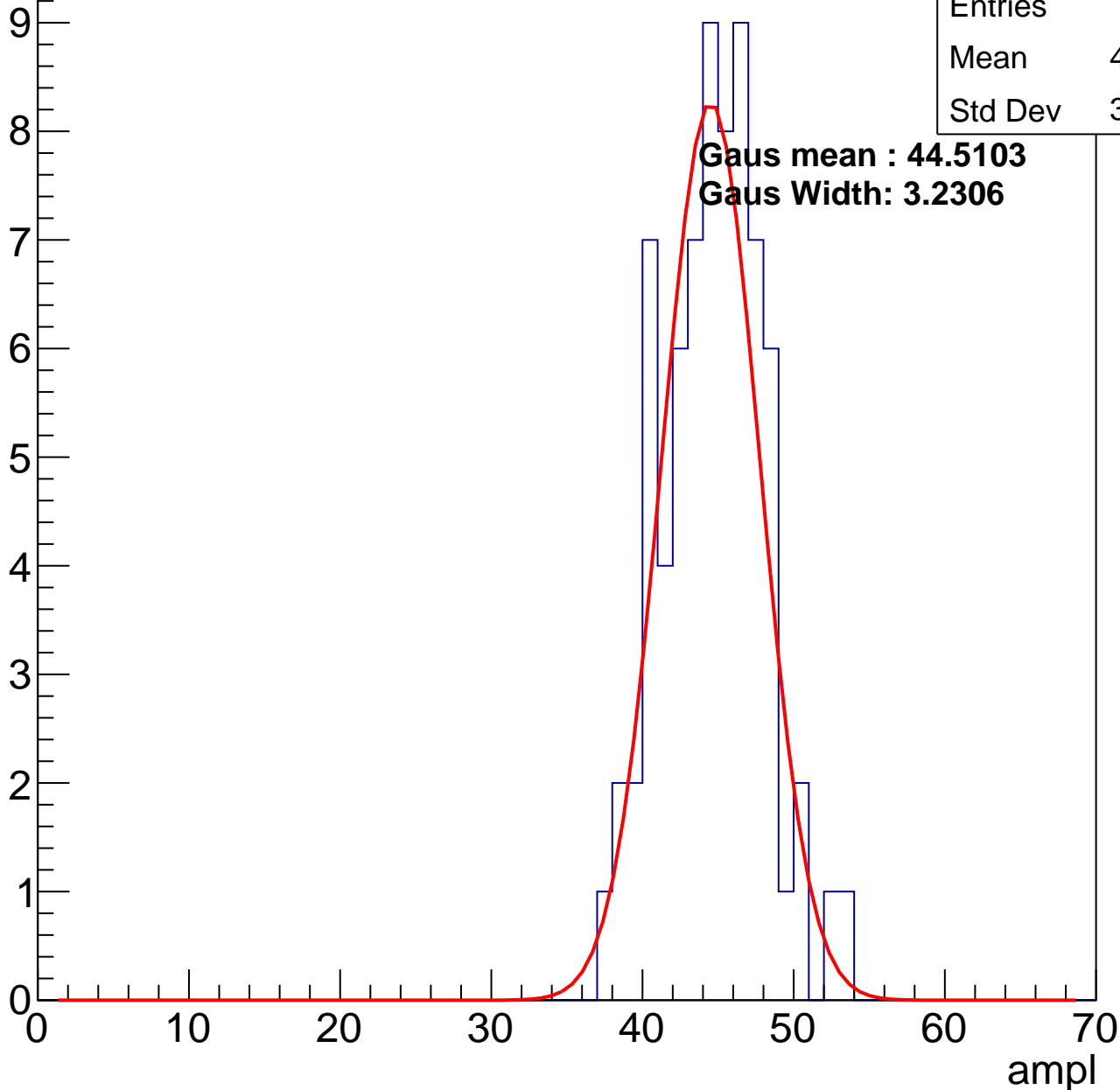
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	73
Mean	44.23
Std Dev	3.292

**Gaus mean : 44.5103**

**Gaus Width: 3.2306**

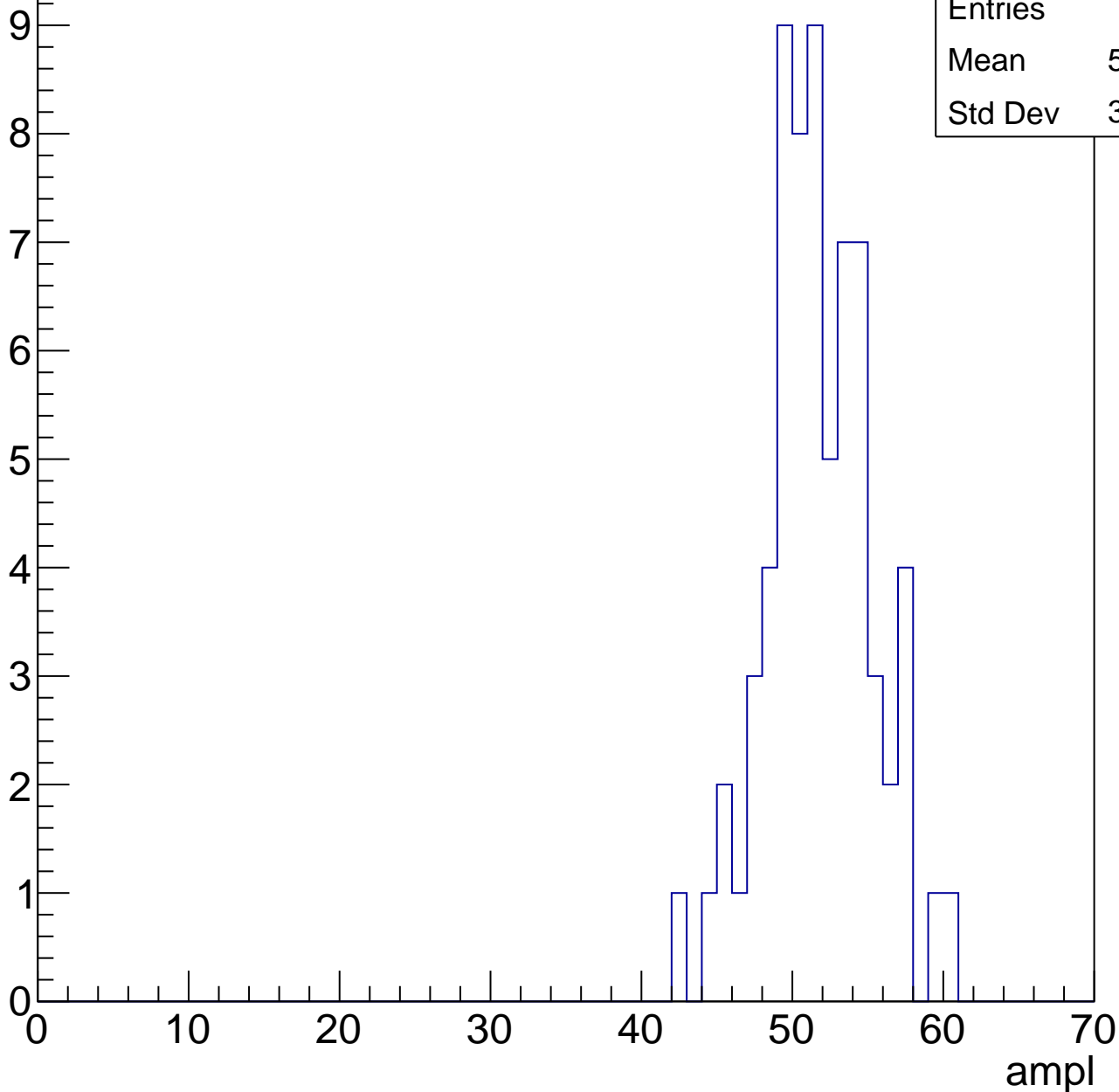


# B1L003S, U3-ch17, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	51.29
Std Dev	3.498

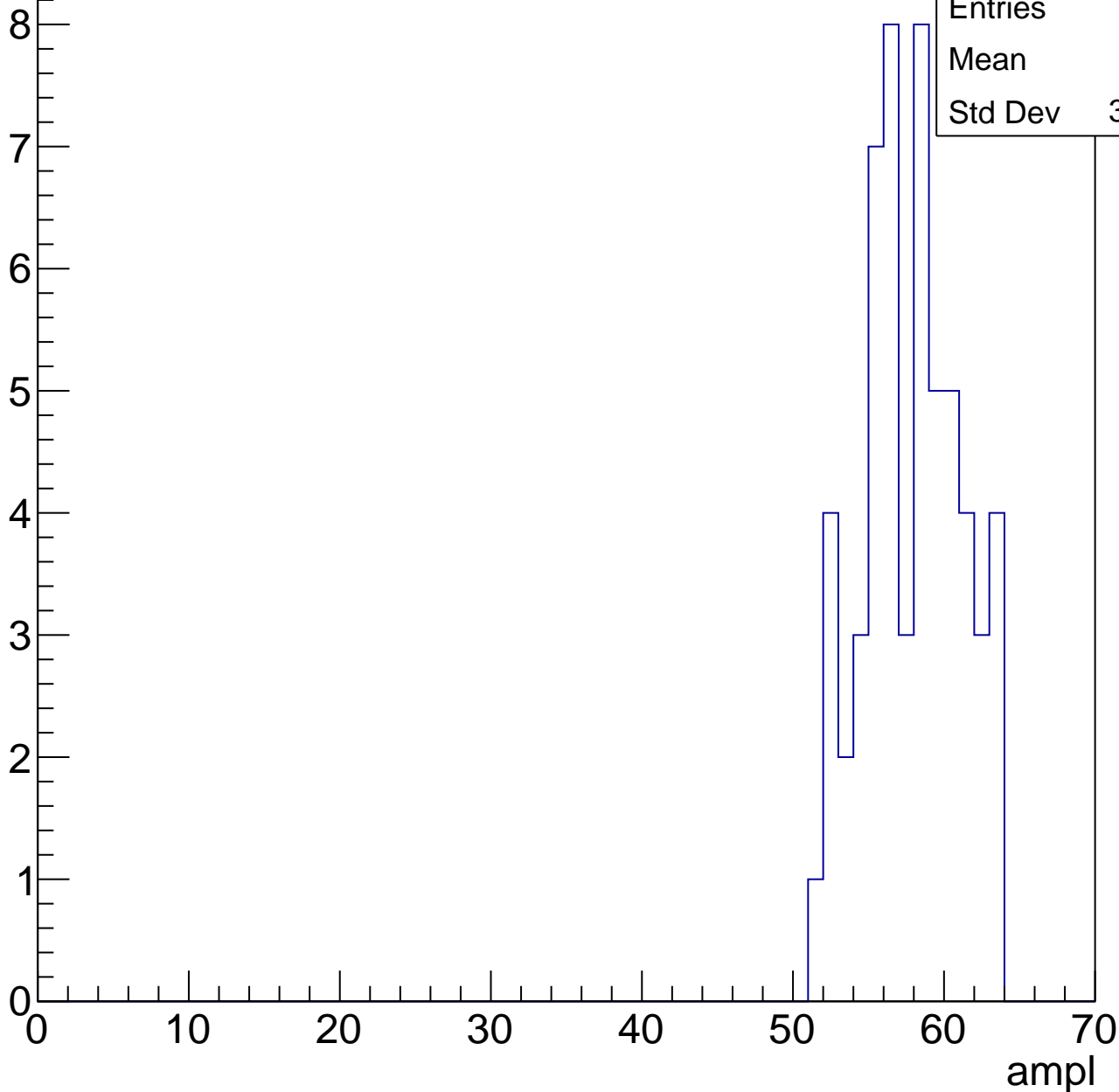


# B1L003S, U3-ch17, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	57.4
Std Dev	3.184

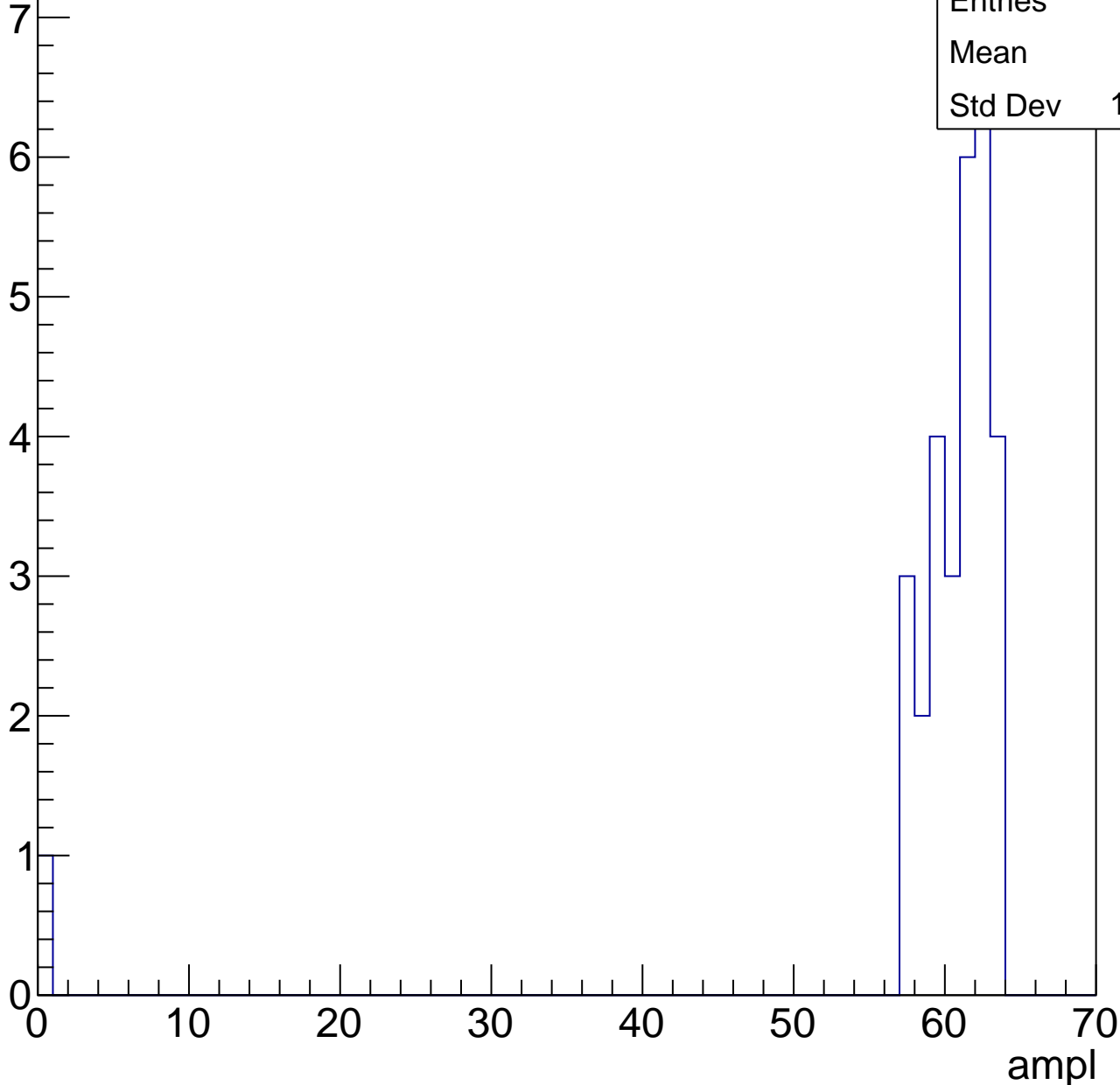


# B1L003S, U3-ch17, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	30
Mean	58.5
Std Dev	11.02



# B1L003S, U3-ch17, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch17, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U3-ch18, adc0

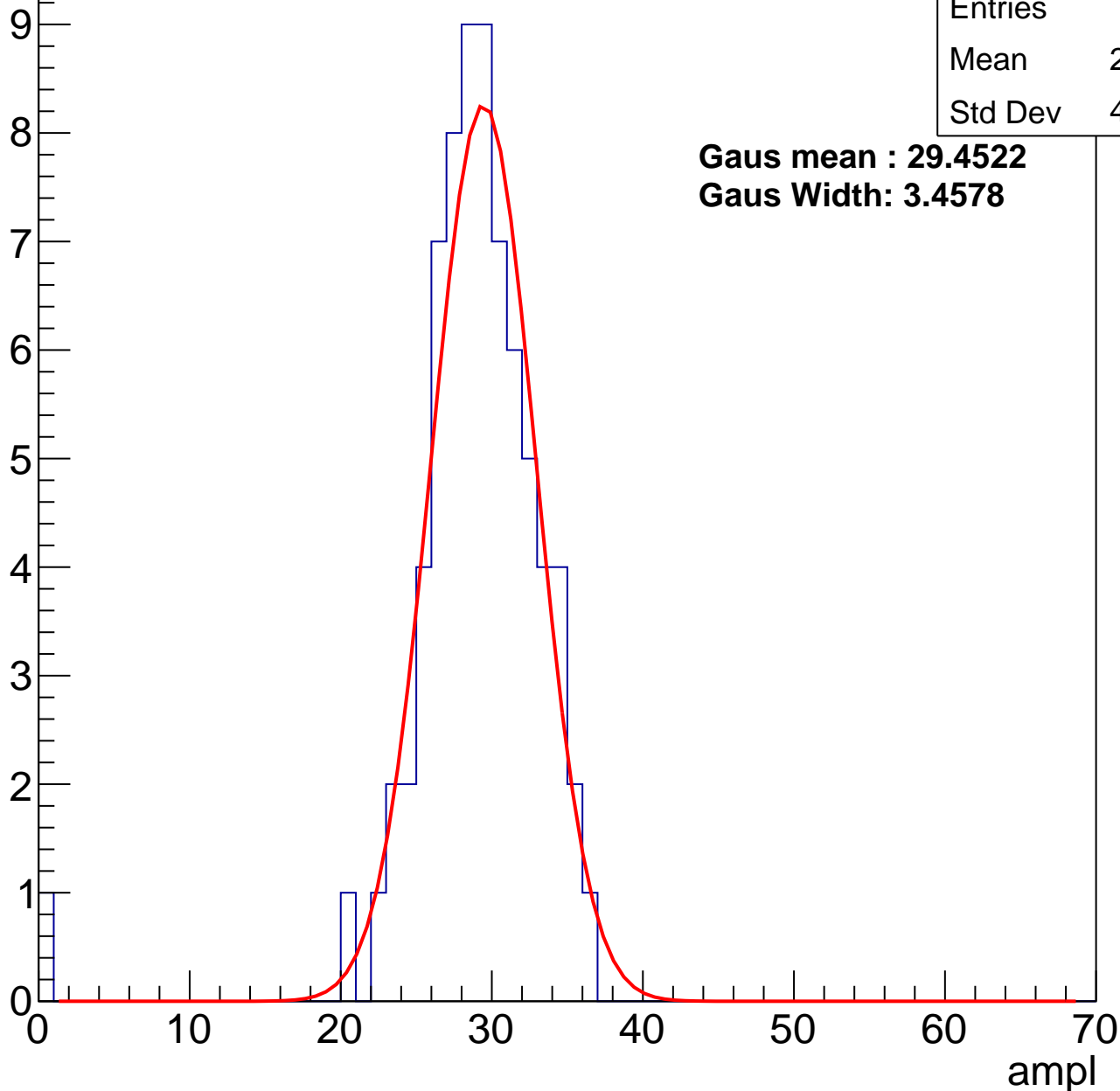
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	73
Mean	28.45
Std Dev	4.682

**Gaus mean : 29.4522**

**Gaus Width: 3.4578**



# B1L003S, U3-ch18, adc1

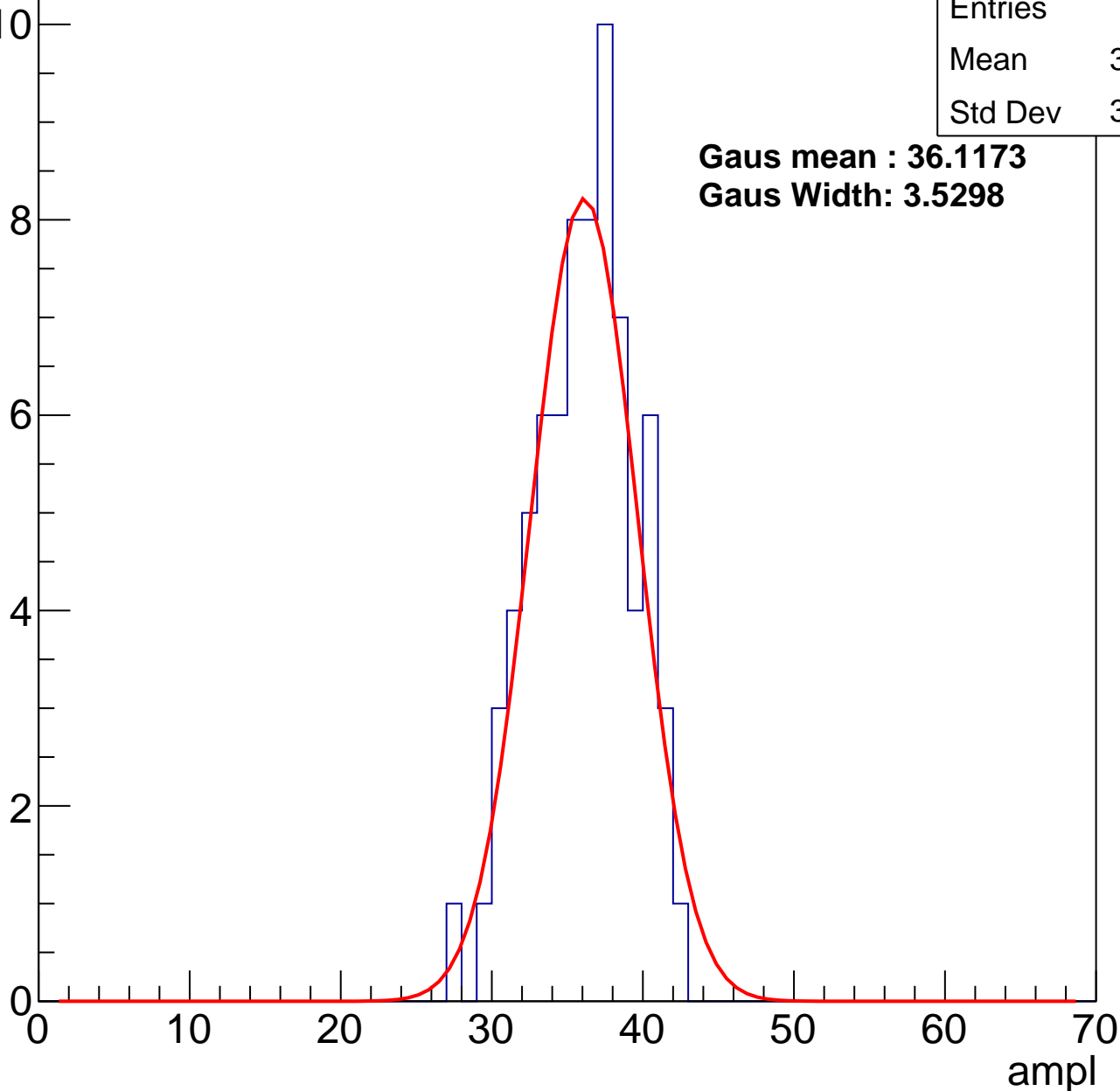
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	73
Mean	35.58
Std Dev	3.252

**Gaus mean : 36.1173**

**Gaus Width: 3.5298**



# B1L003S, U3-ch18, adc2

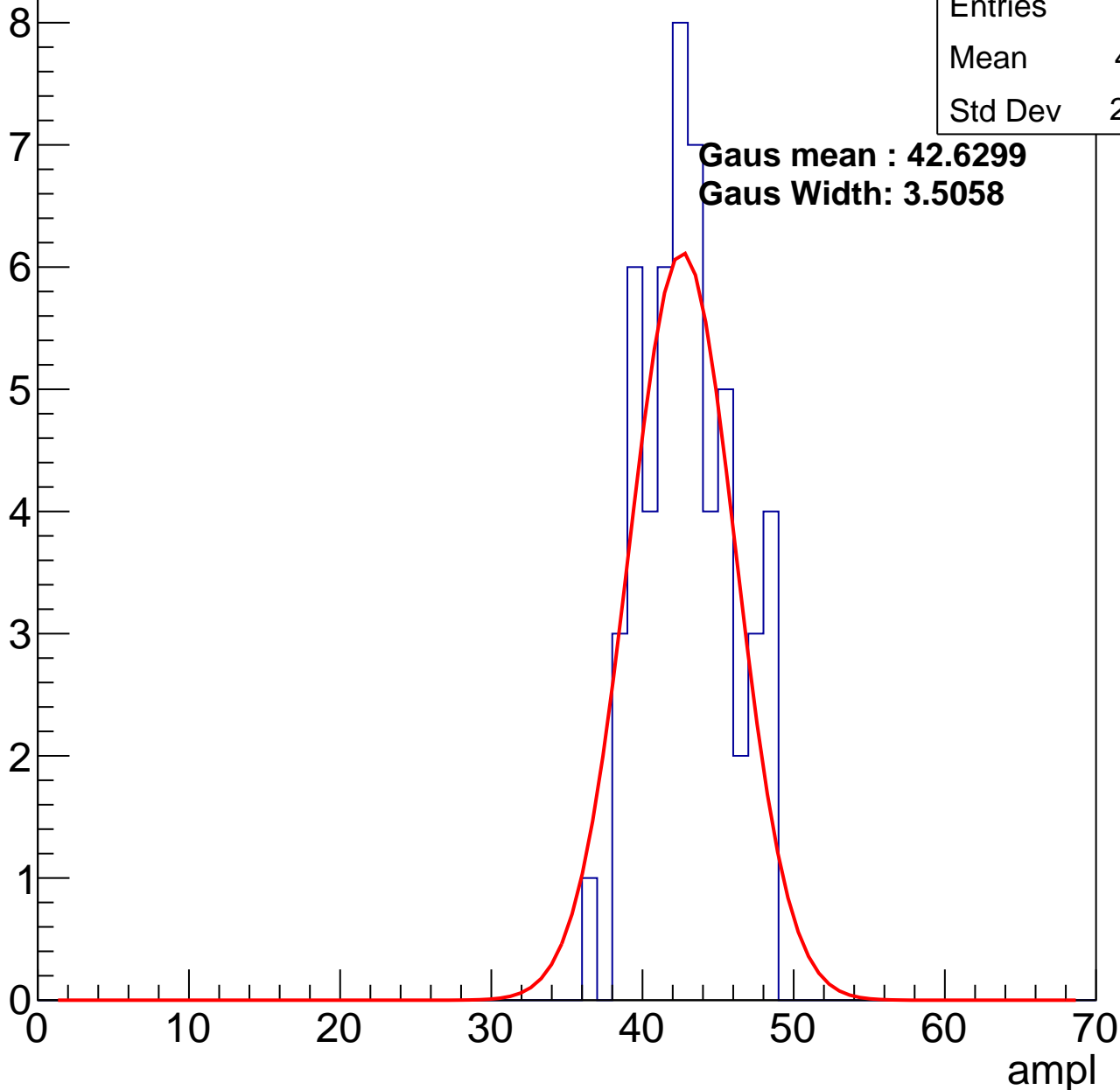
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	42.51
Std Dev	2.963

**Gaus mean : 42.6299**

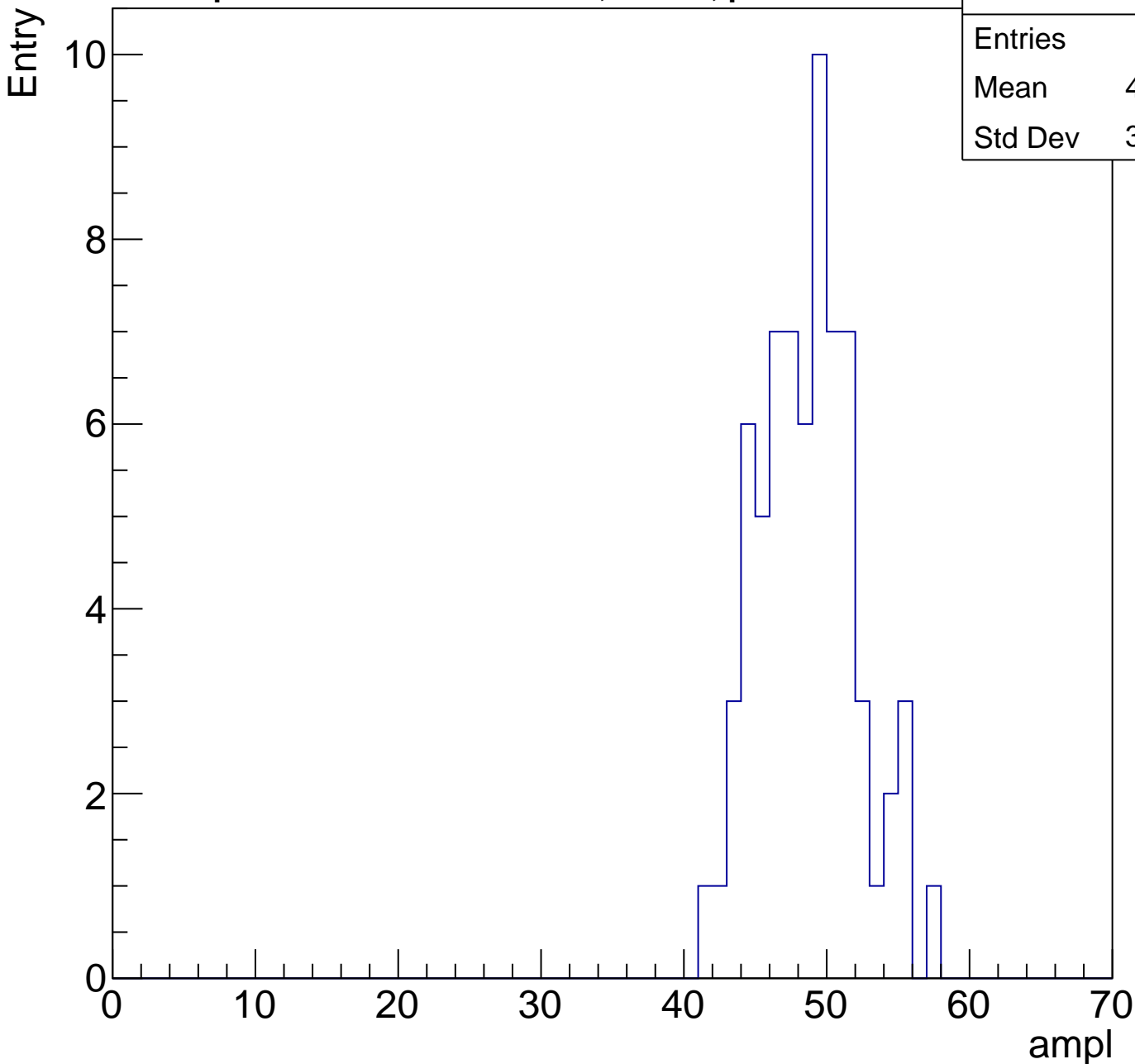
**Gaus Width: 3.5058**



# B1L003S, U3-ch18, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	70
Mean	48.23
Std Dev	3.394

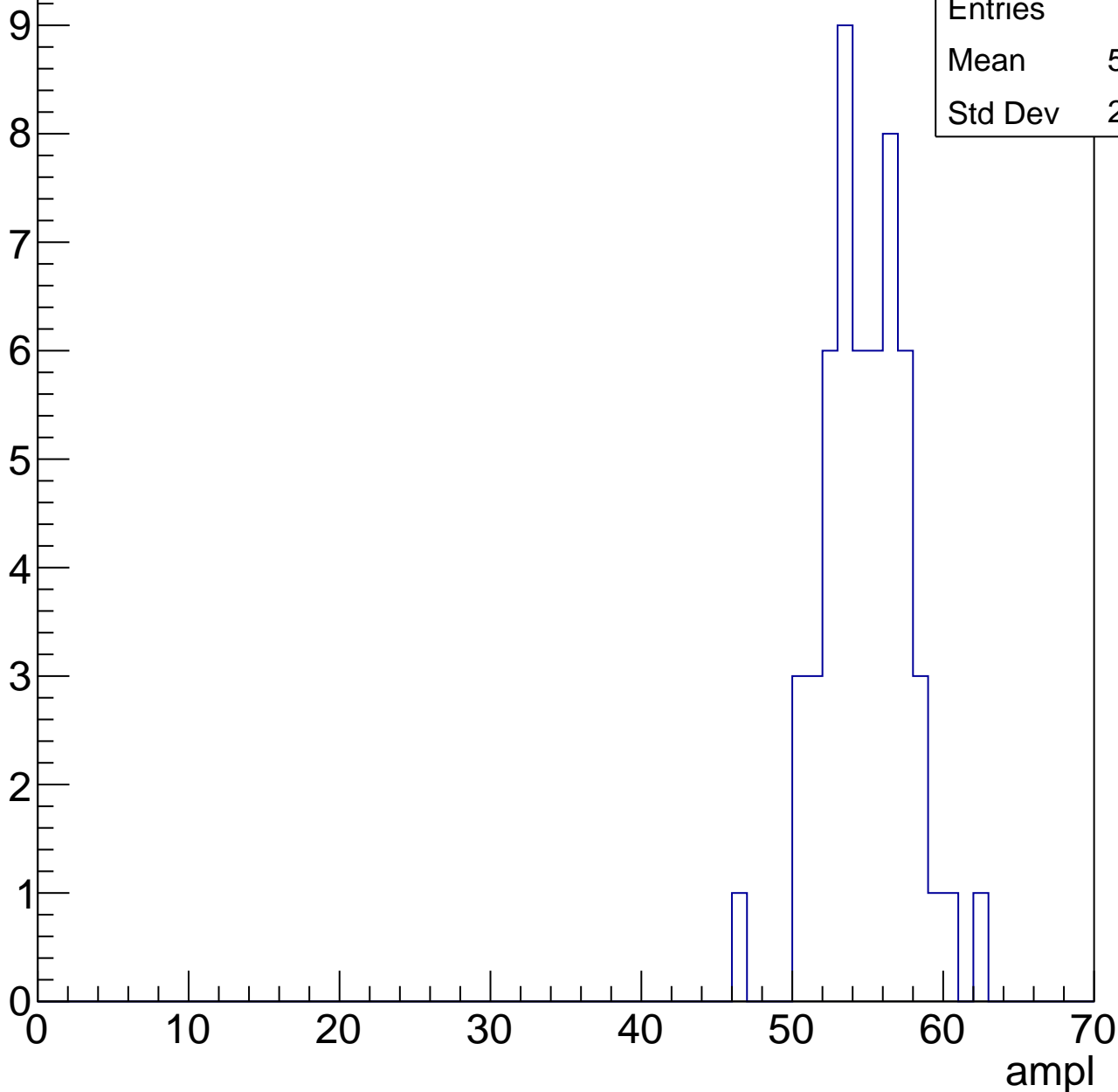


# B1L003S, U3-ch18, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	54
Mean	54.39
Std Dev	2.818



# B1L003S, U3-ch18, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

10

8

6

4

2

0

0

10

20

30

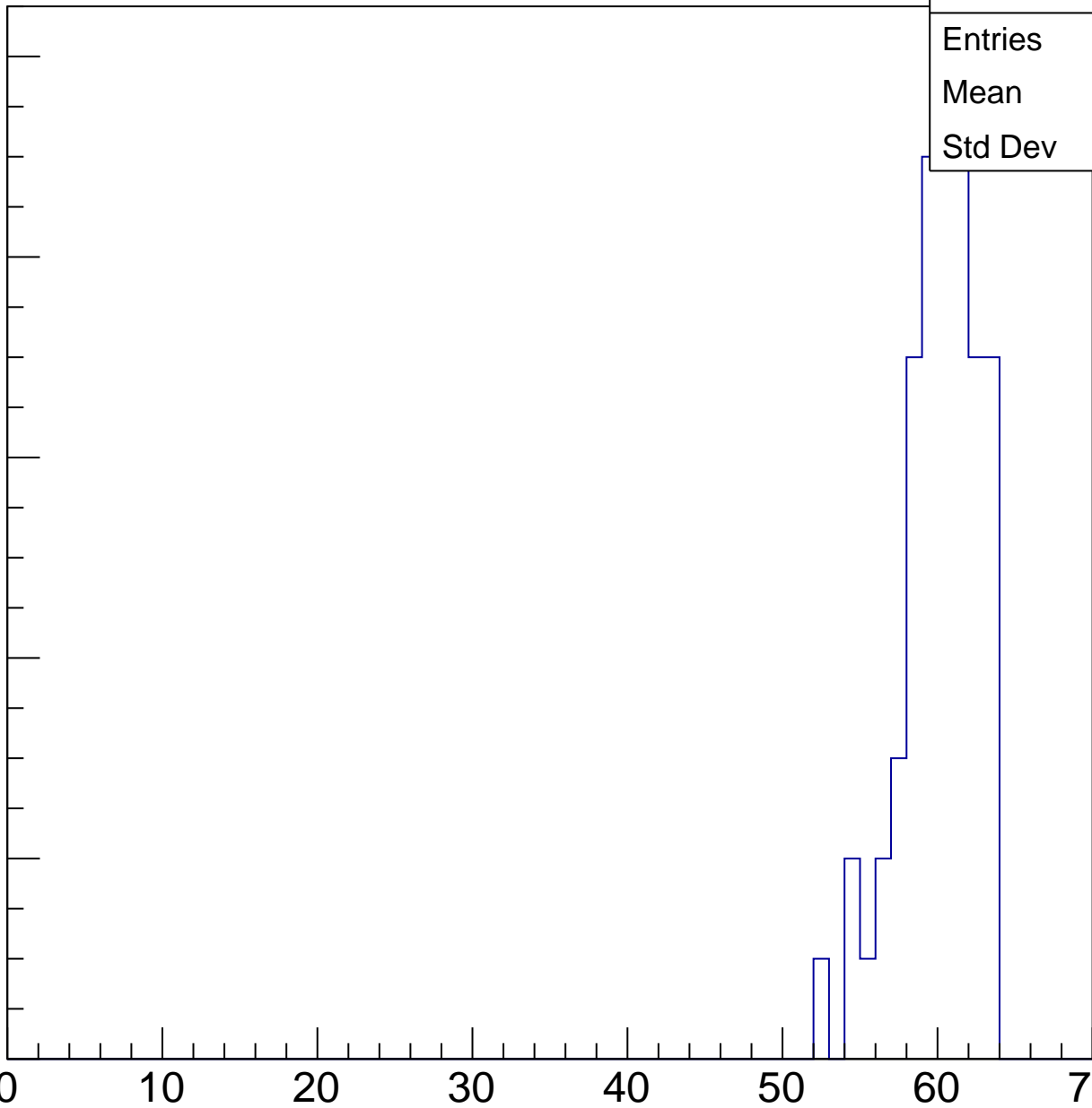
40

50

60

ampl

Entries	58
Mean	59.66
Std Dev	2.46



# B1L003S, U3-ch18, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

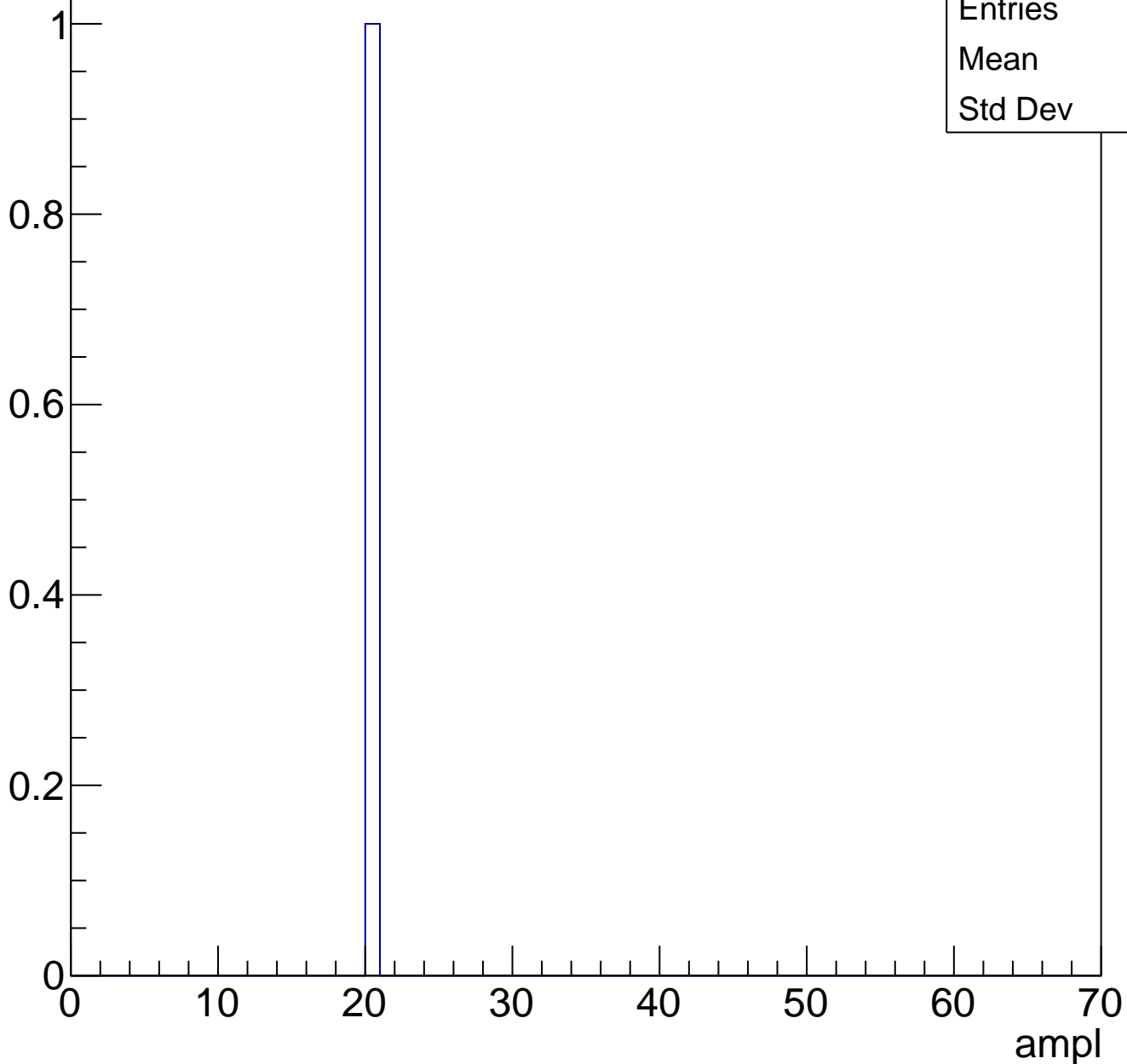




# B1L003S, U3-ch18, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	20
Std Dev	0

# B1L003S, U3-ch19, adc0

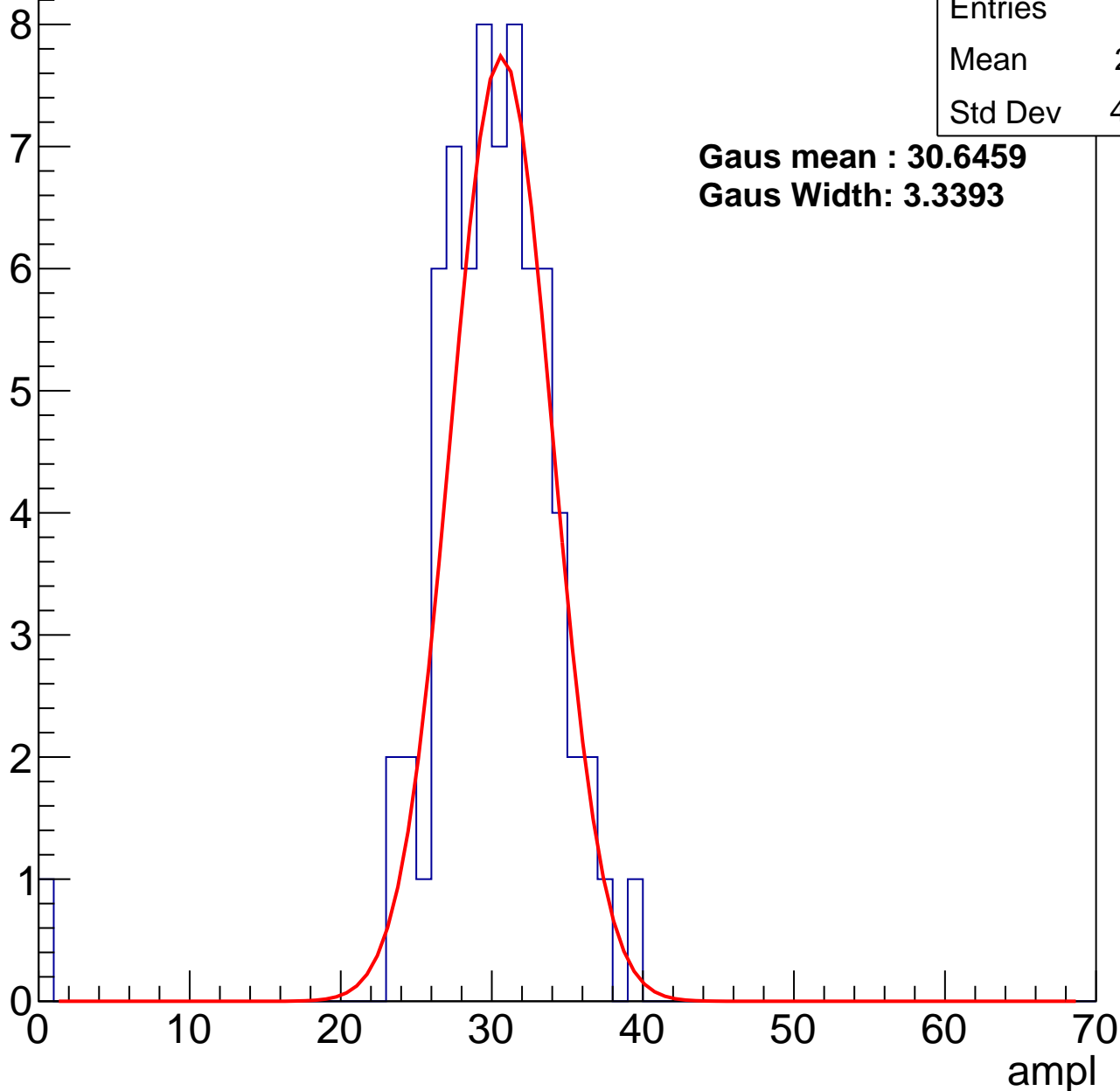
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	29.51
Std Dev	4.887

**Gaus mean : 30.6459**

**Gaus Width: 3.3393**



# B1L003S, U3-ch19, adc1

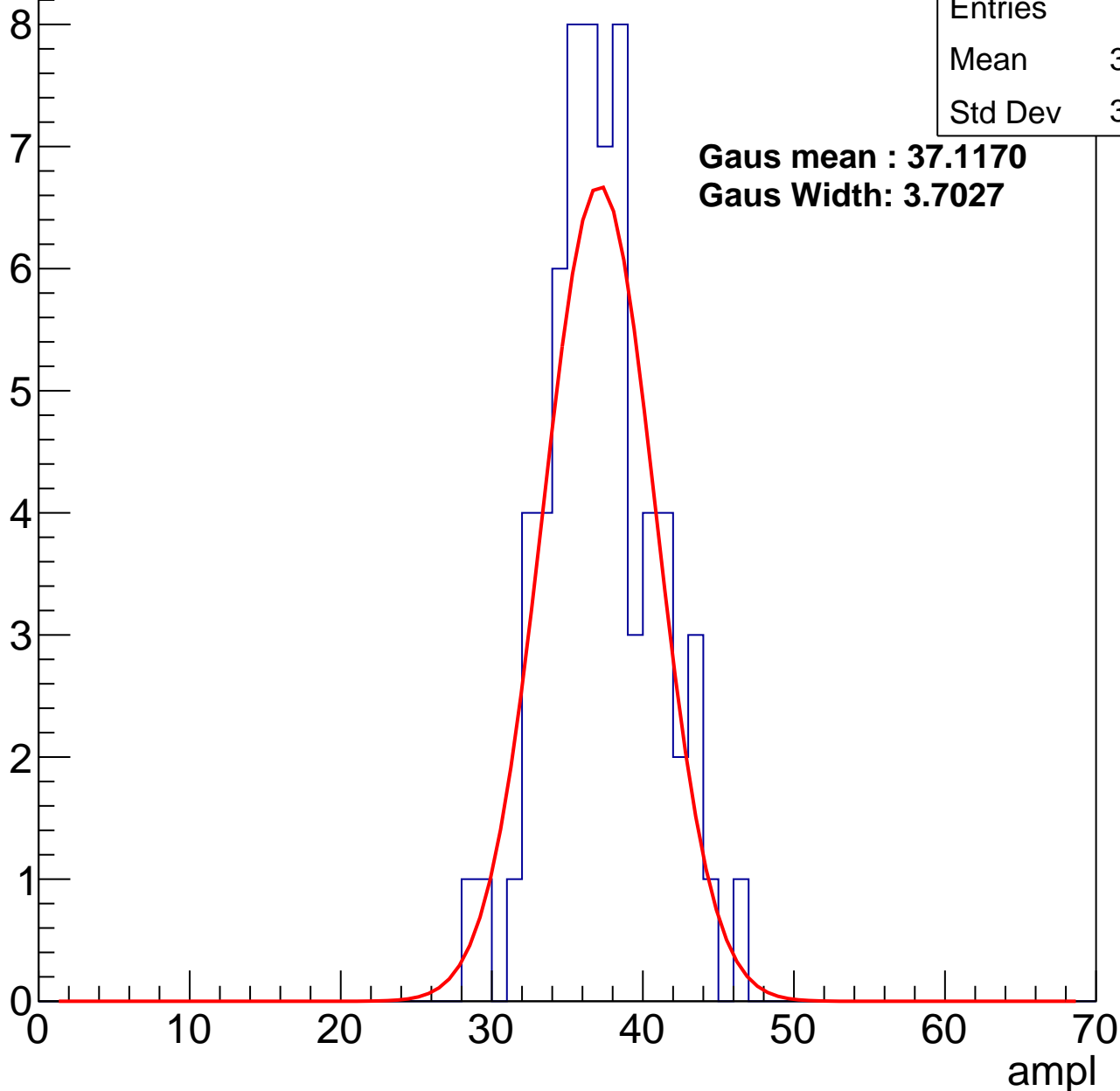
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	36.77
Std Dev	3.575

**Gaus mean : 37.1170**

**Gaus Width: 3.7027**



# B1L003S, U3-ch19, adc2

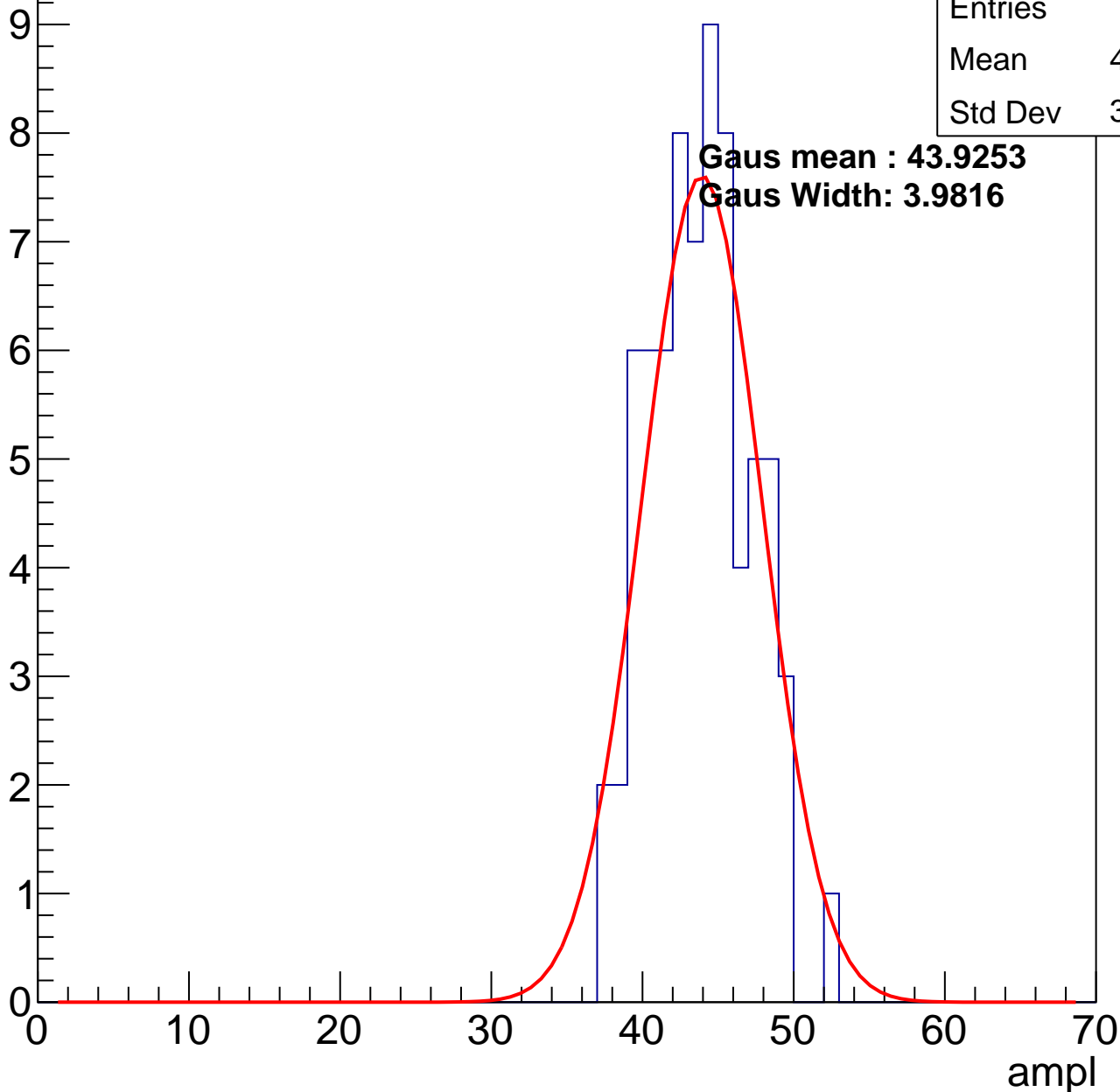
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	72
Mean	43.35
Std Dev	3.262

**Gaus mean : 43.9253**

**Gaus Width: 3.9816**

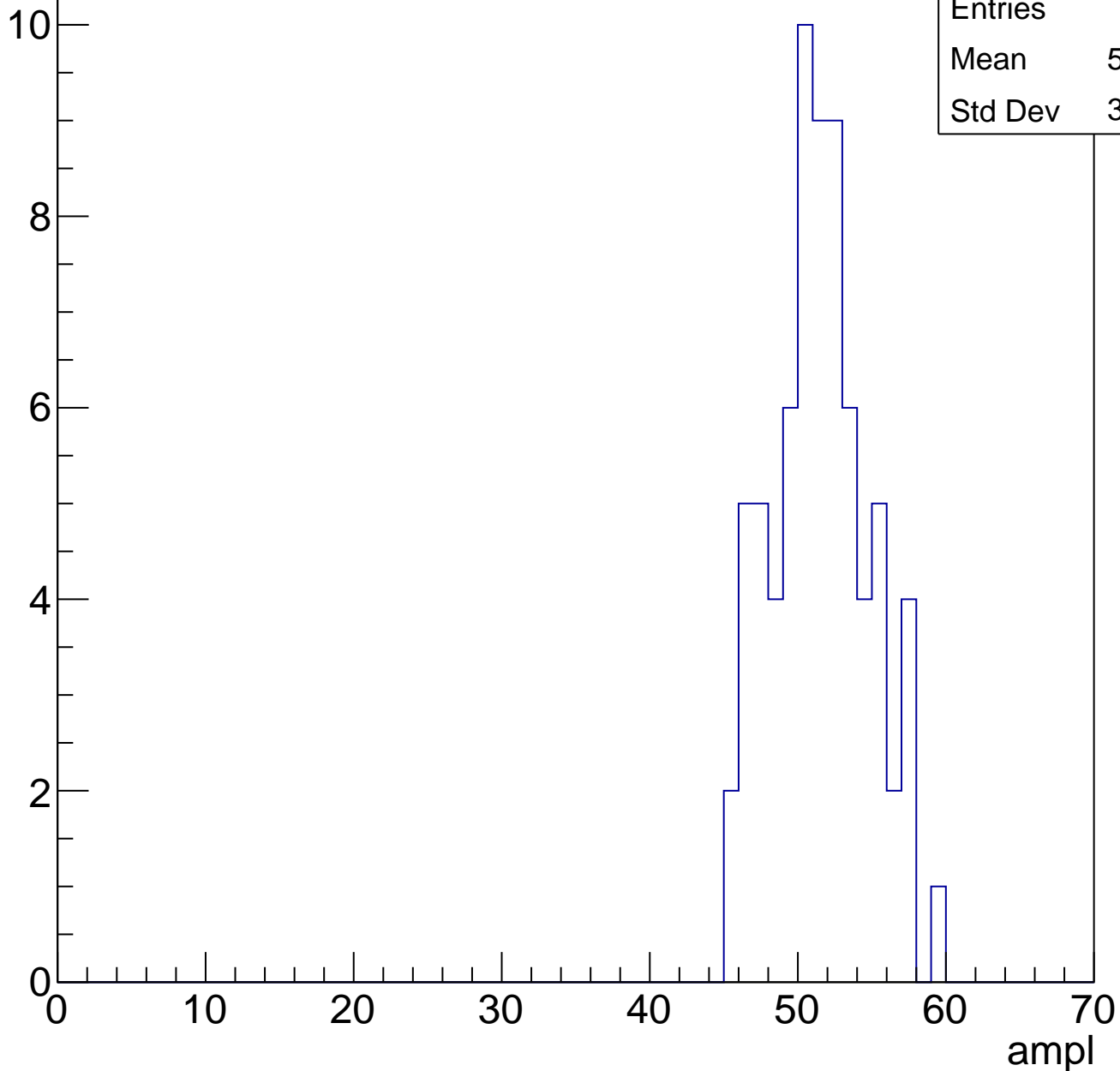


# B1L003S, U3-ch19, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	72
Mean	51.06
Std Dev	3.236

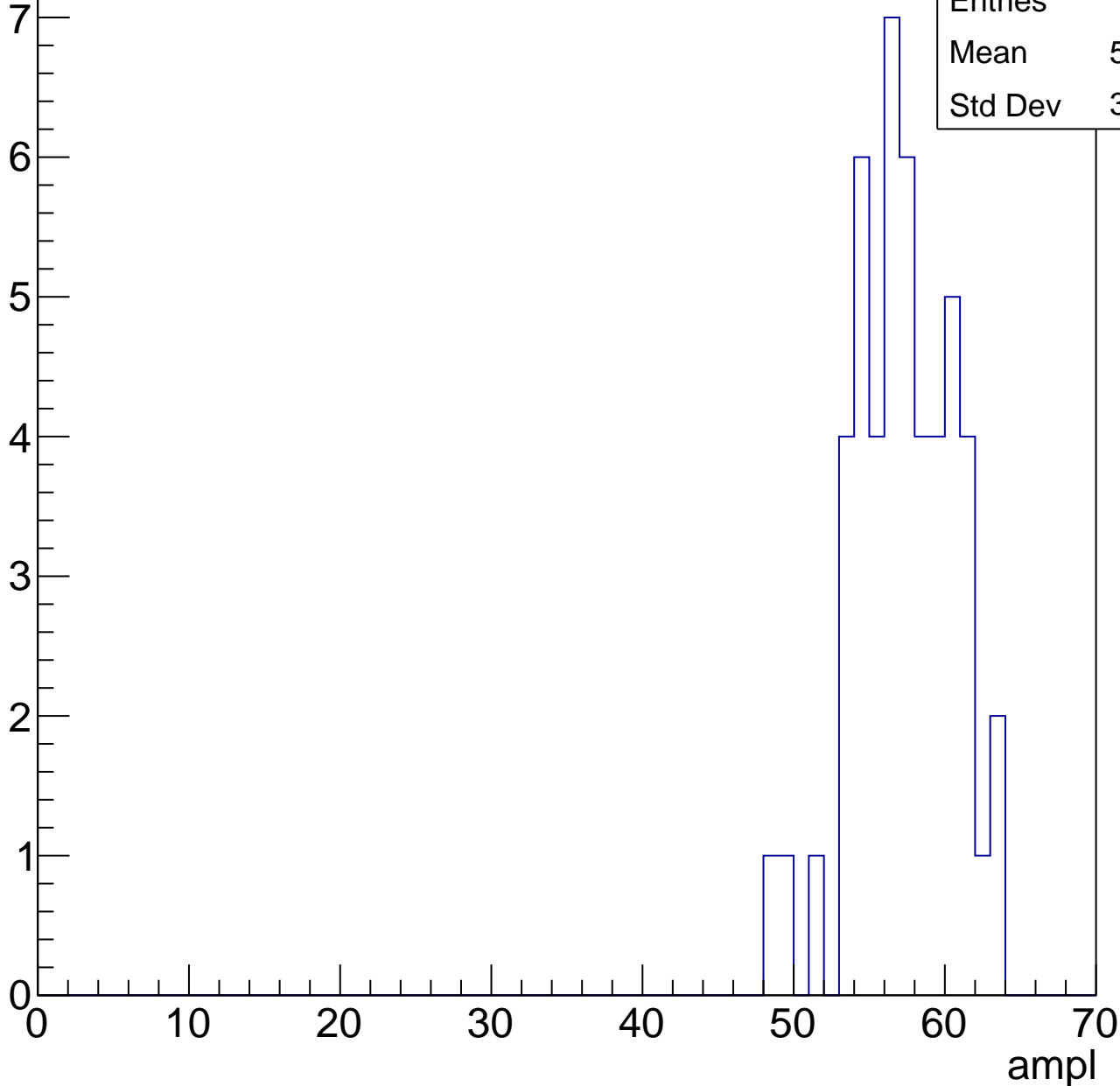


# B1L003S, U3-ch19, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	50
Mean	56.76
Std Dev	3.302

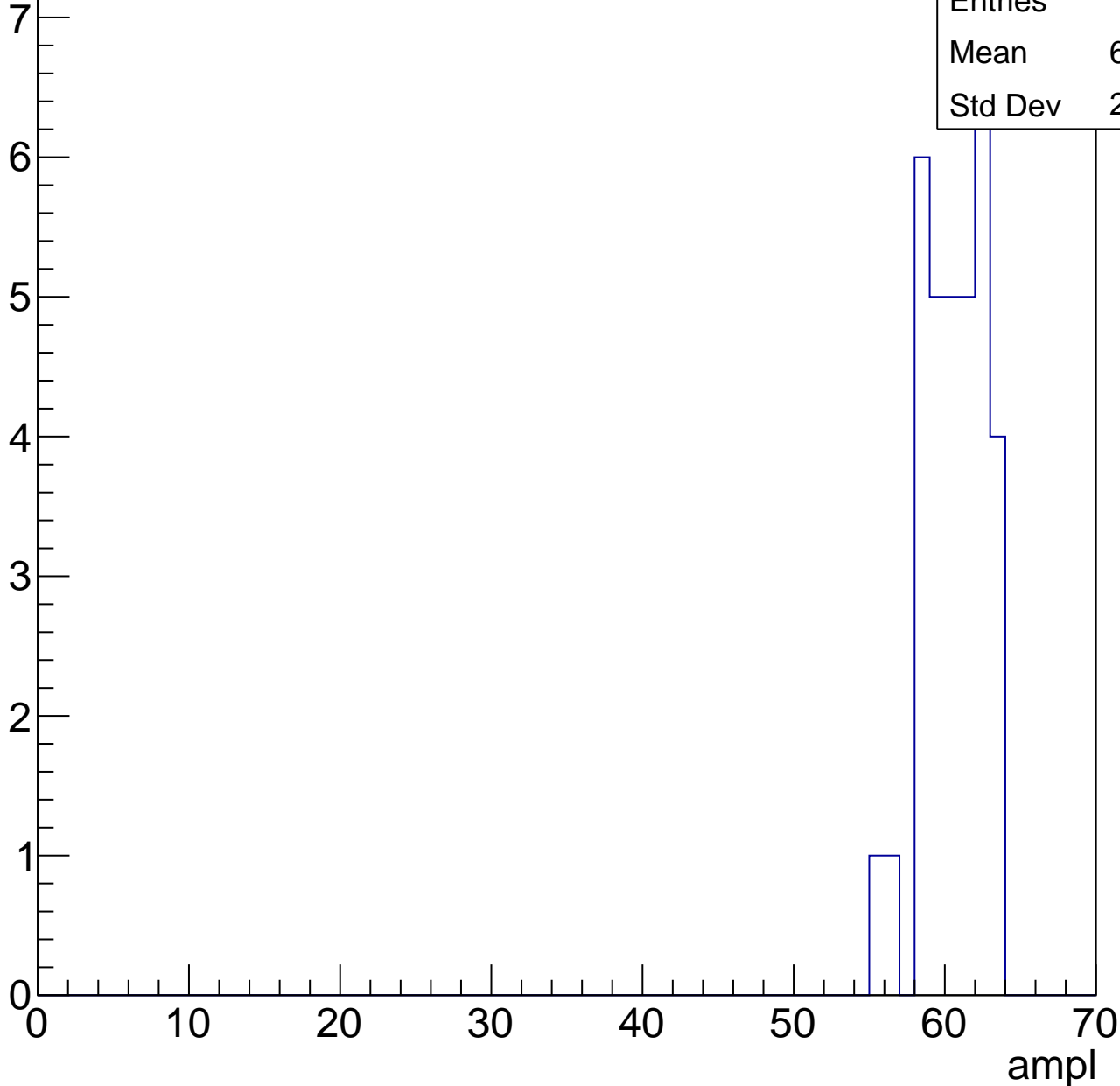


# B1L003S, U3-ch19, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

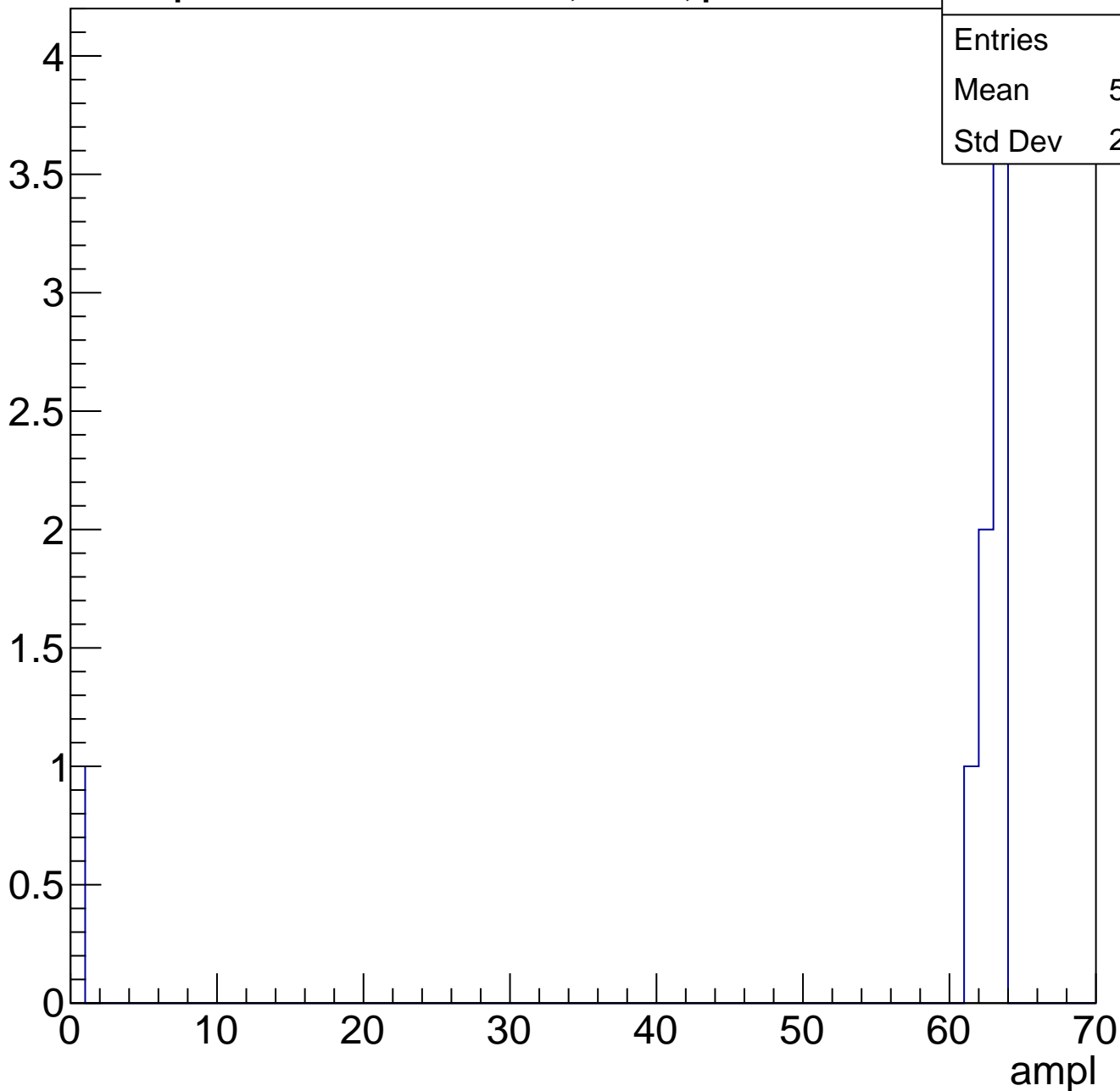
Entries	34
Mean	60.15
Std Dev	2.017



# B1L003S, U3-ch19, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch19, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U3-ch20, adc0

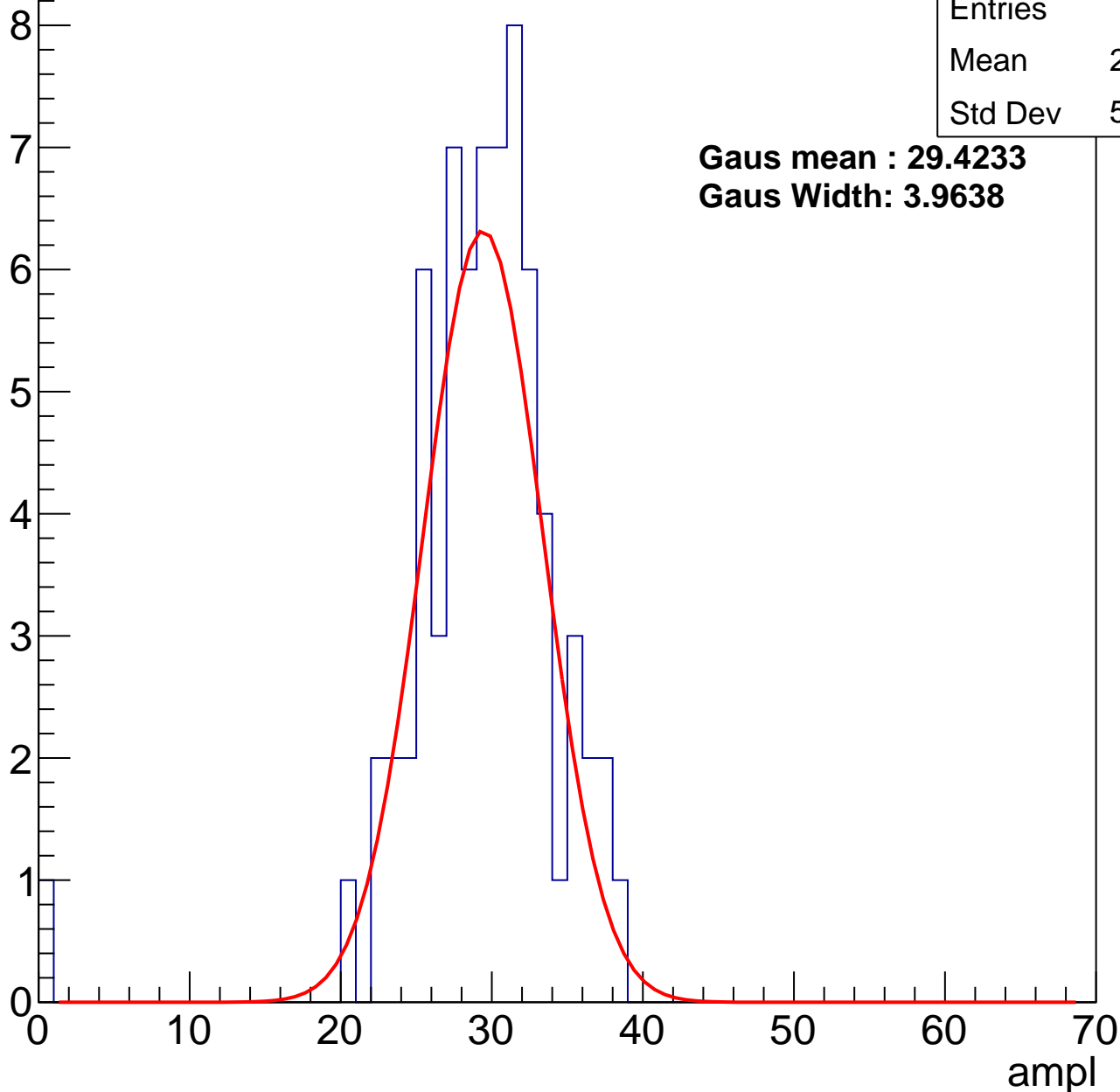
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	71
Mean	28.89
Std Dev	5.166

**Gaus mean : 29.4233**

**Gaus Width: 3.9638**



# B1L003S, U3-ch20, adc1

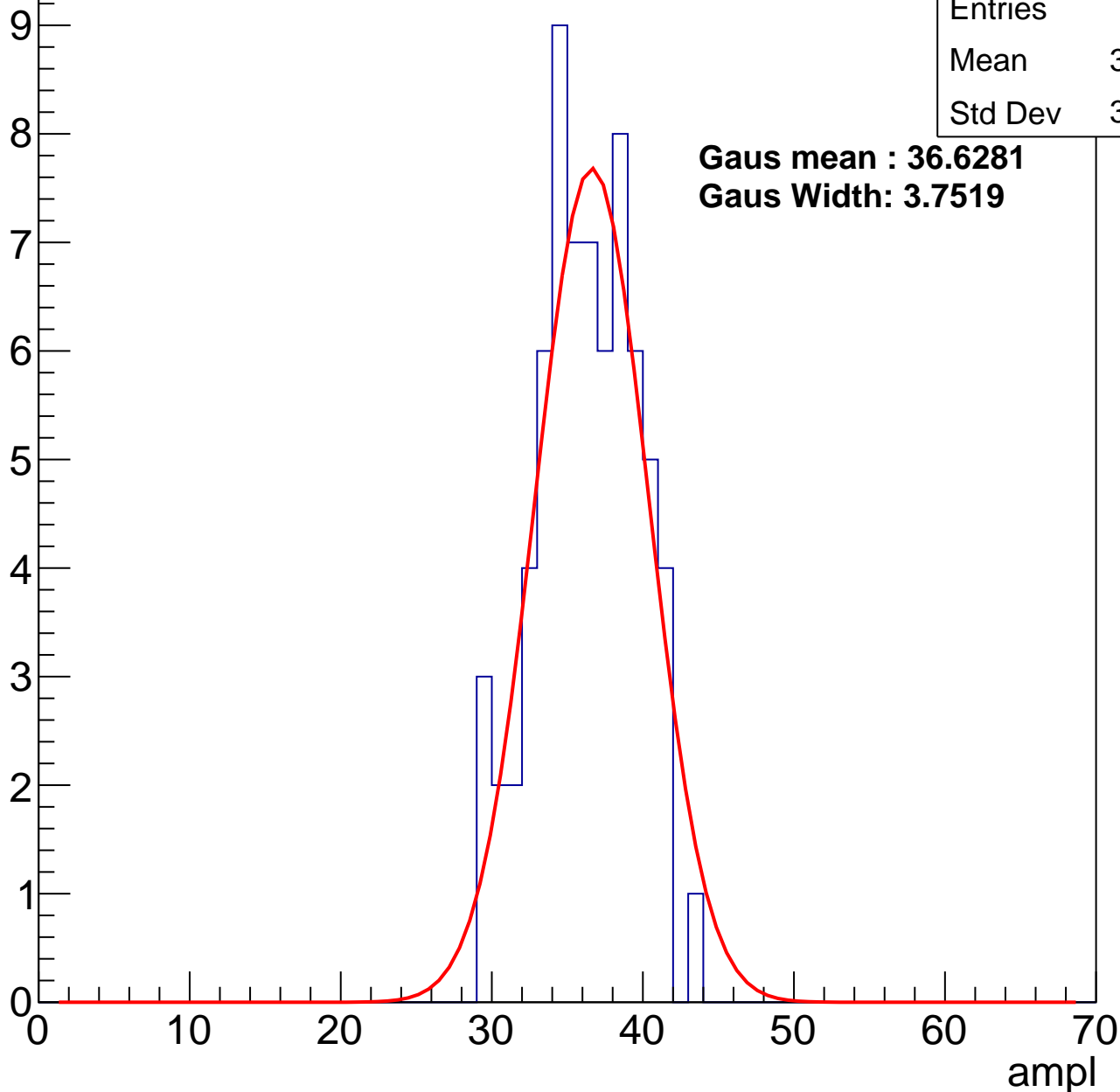
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	35.79
Std Dev	3.268

**Gaus mean : 36.6281**

**Gaus Width: 3.7519**



# B1L003S, U3-ch20, adc2

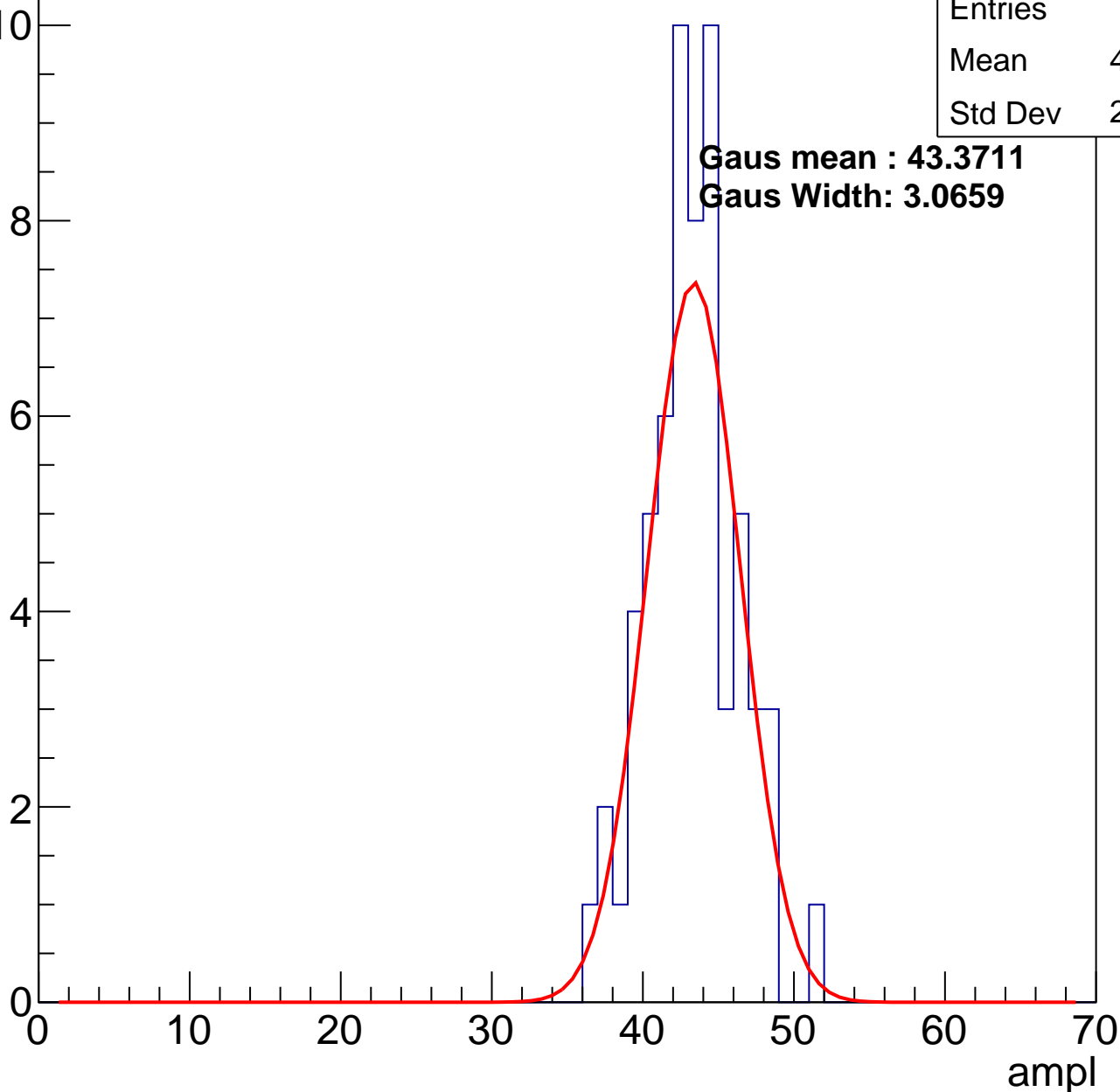
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	42.82
Std Dev	2.954

**Gaus mean : 43.3711**

**Gaus Width: 3.0659**

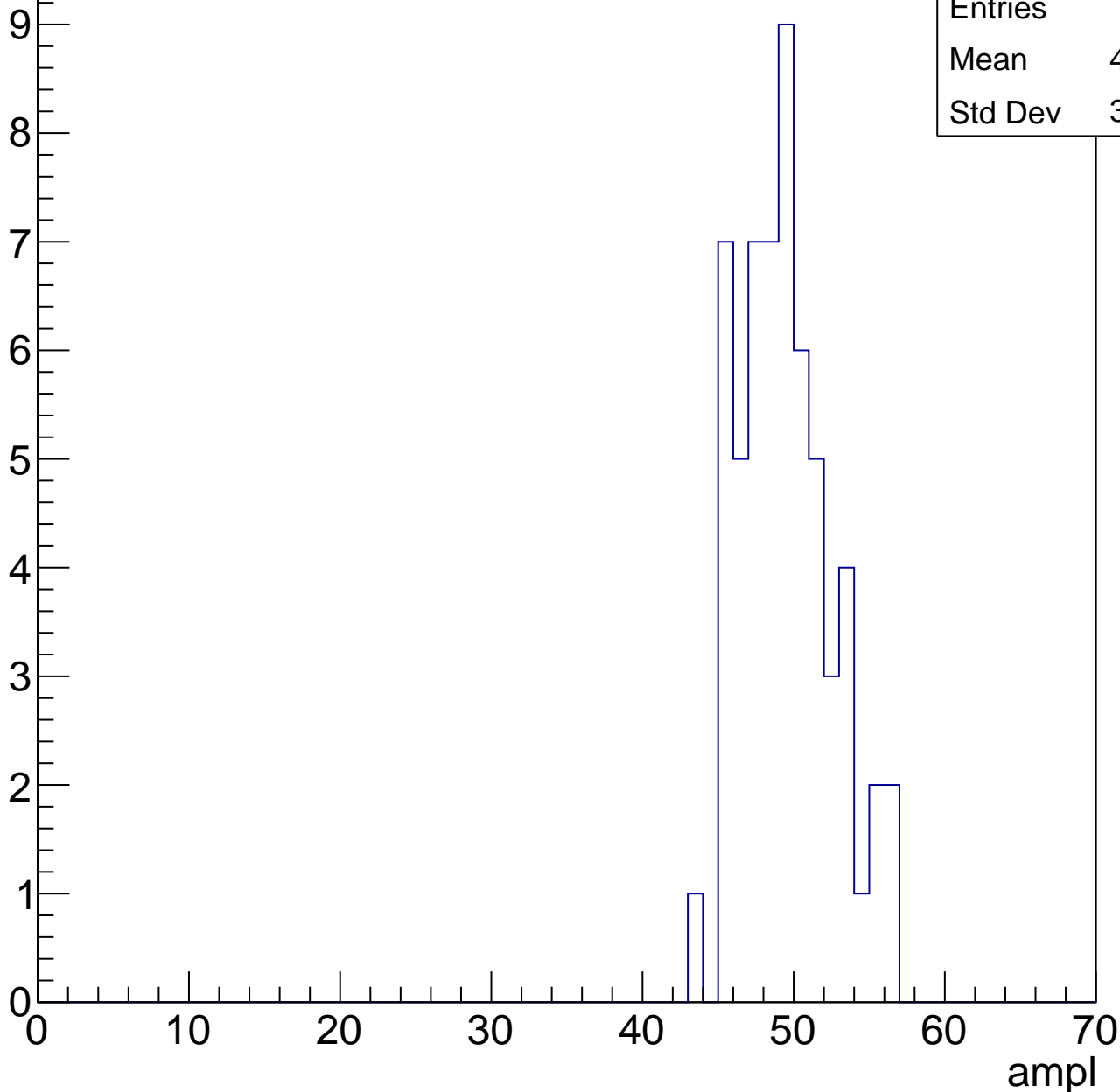


# B1L003S, U3-ch20, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	49.03
Std Dev	3.025

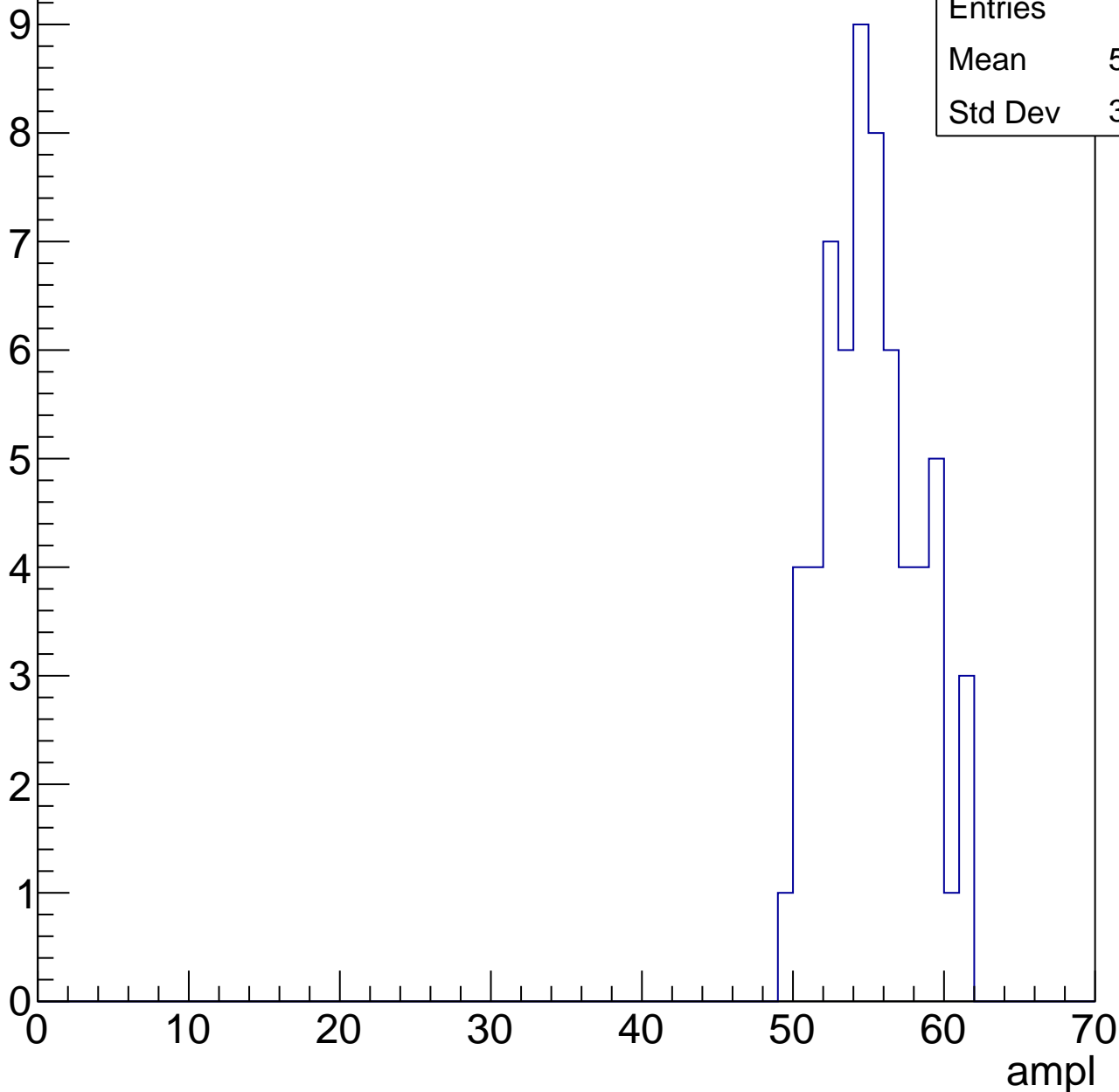


# B1L003S, U3-ch20, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	54.76
Std Dev	3.014



# B1L003S, U3-ch20, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

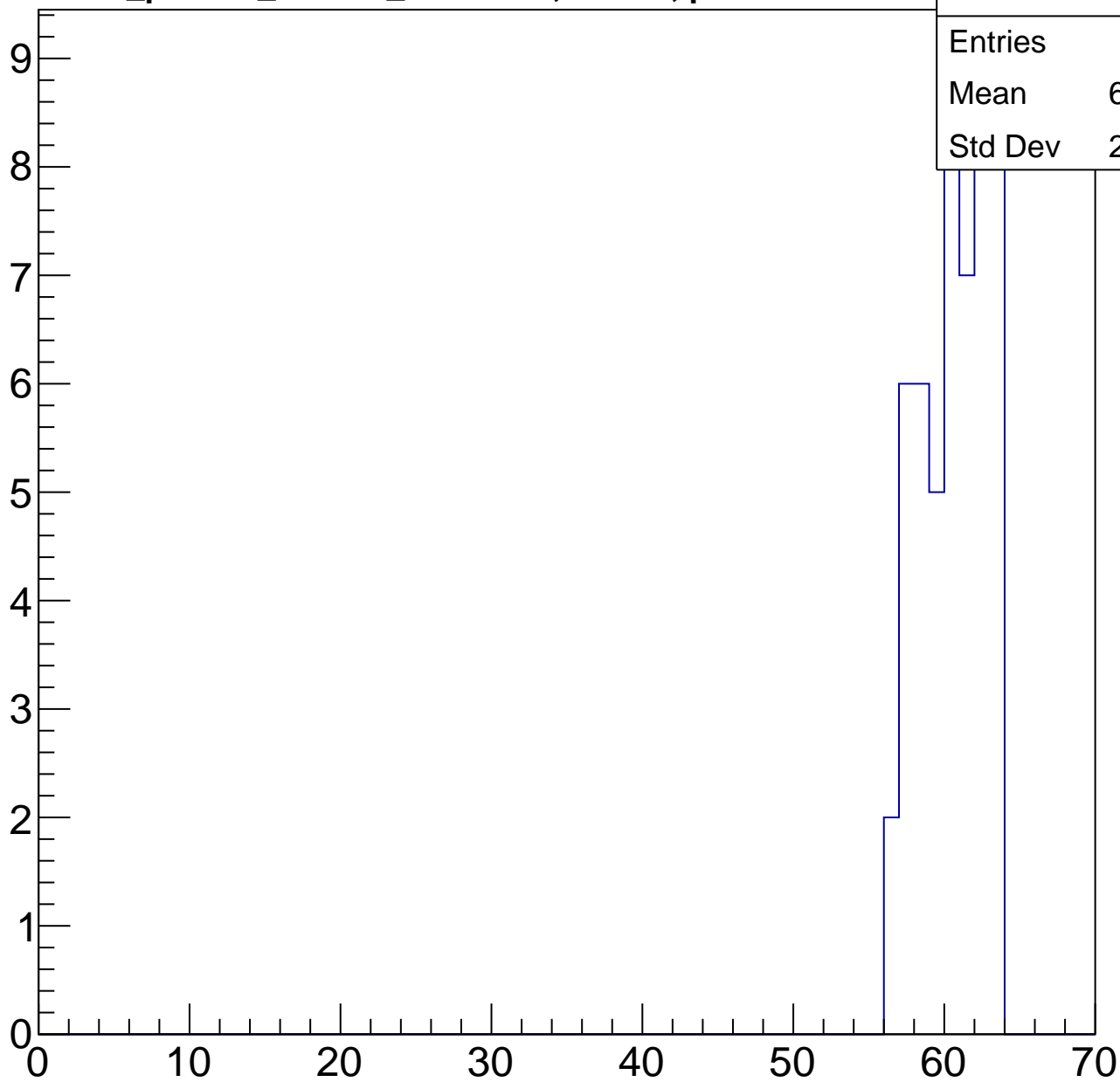
Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	53
Mean	60.17
Std Dev	2.117

ampl

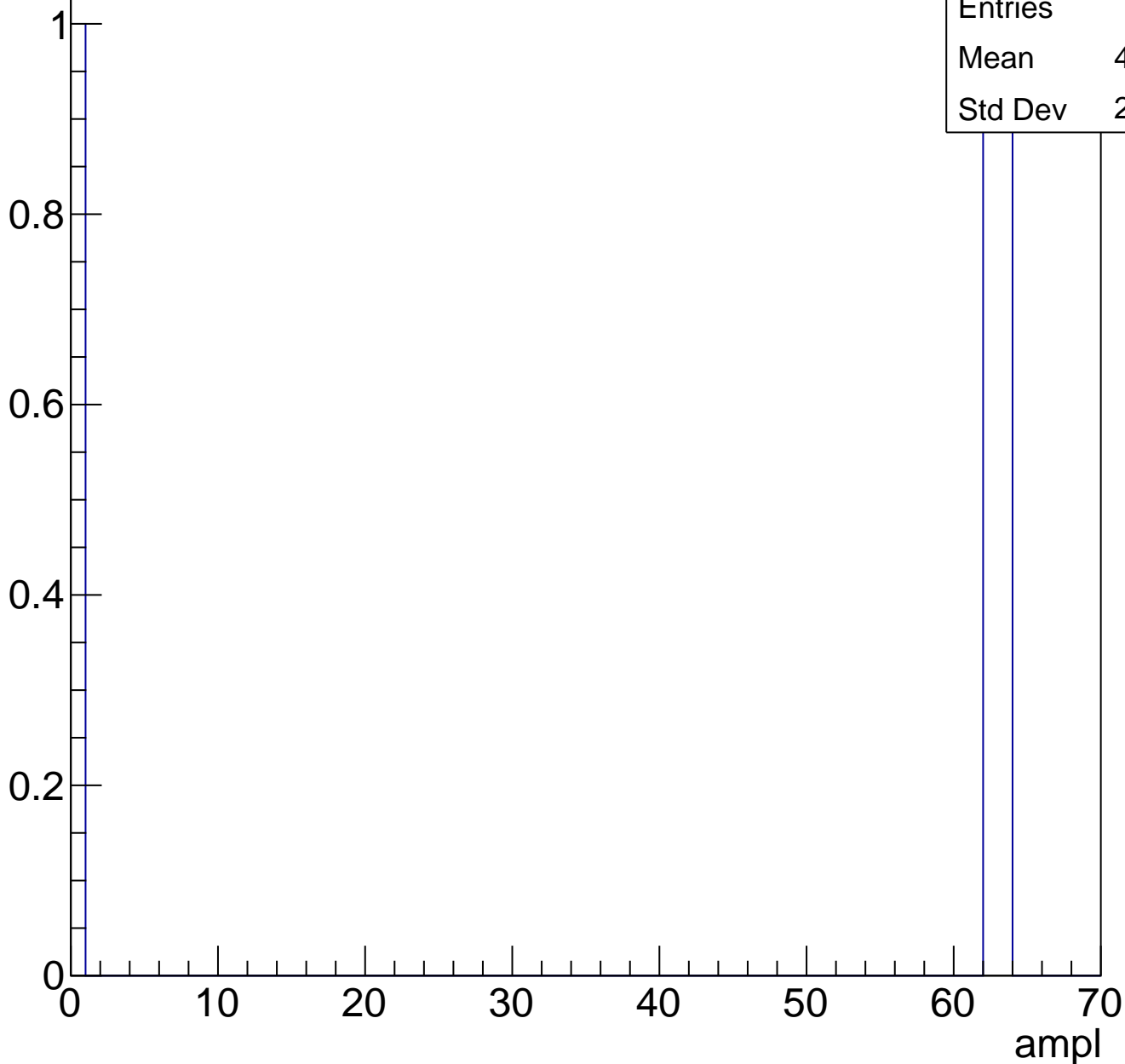
0 10 20 30 40 50 60 70



# B1L003S, U3-ch20, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch20, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U3-ch21, adc0

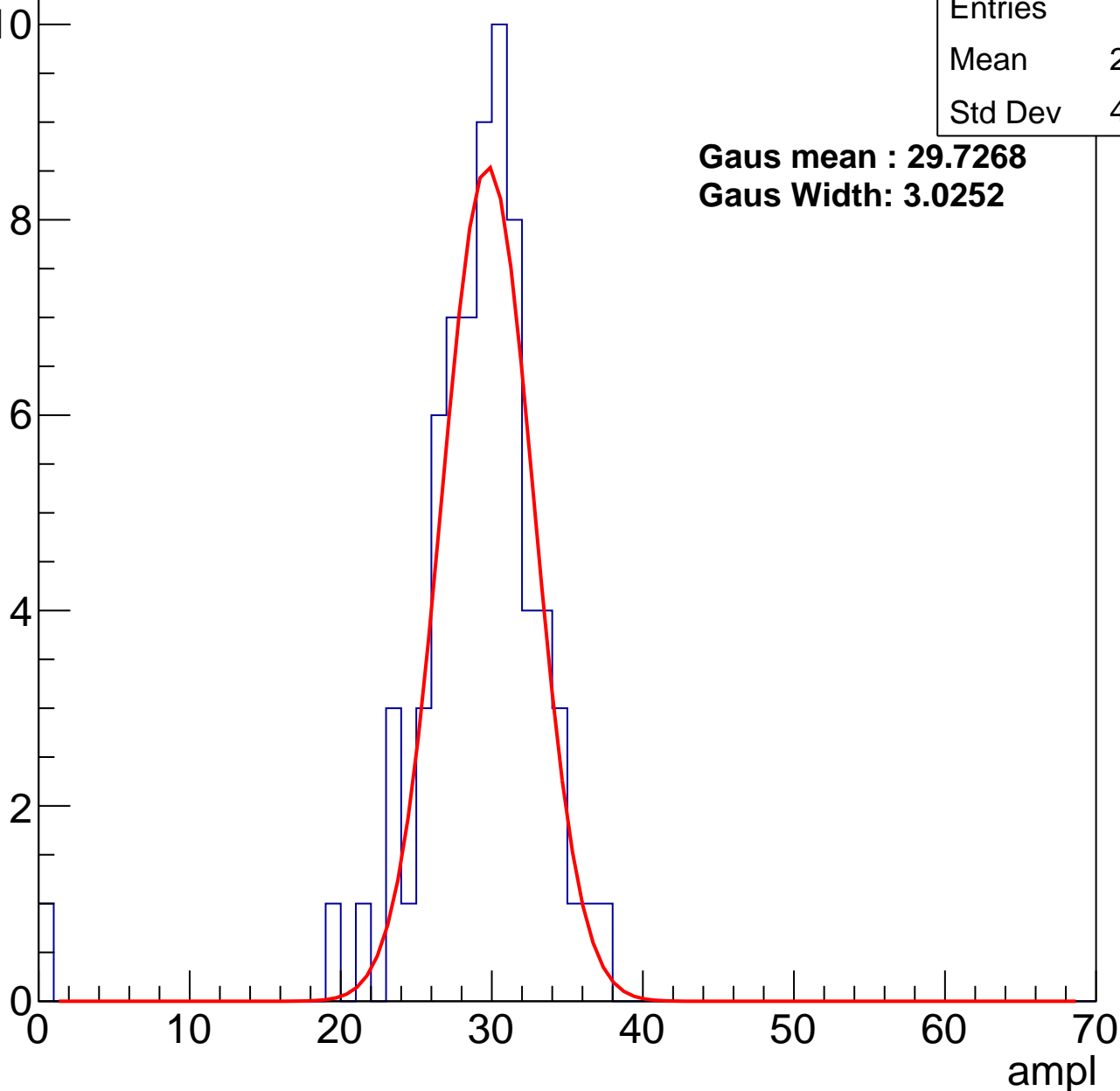
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	71
Mean	28.56
Std Dev	4.788

**Gaus mean : 29.7268**

**Gaus Width: 3.0252**



# B1L003S, U3-ch21, adc1

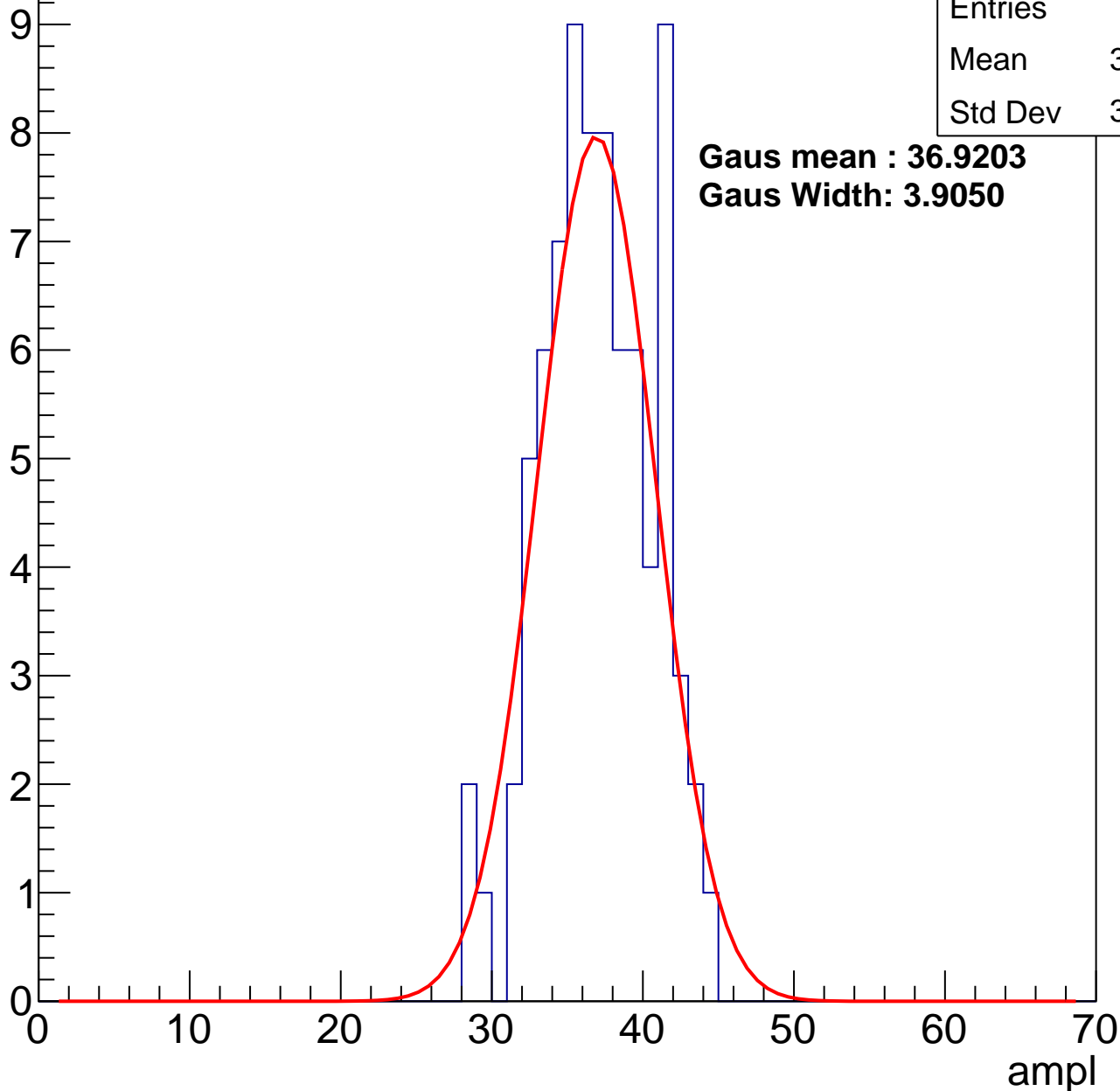
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	79
Mean	36.57
Std Dev	3.589

**Gaus mean : 36.9203**

**Gaus Width: 3.9050**



# B1L003S, U3-ch21, adc2

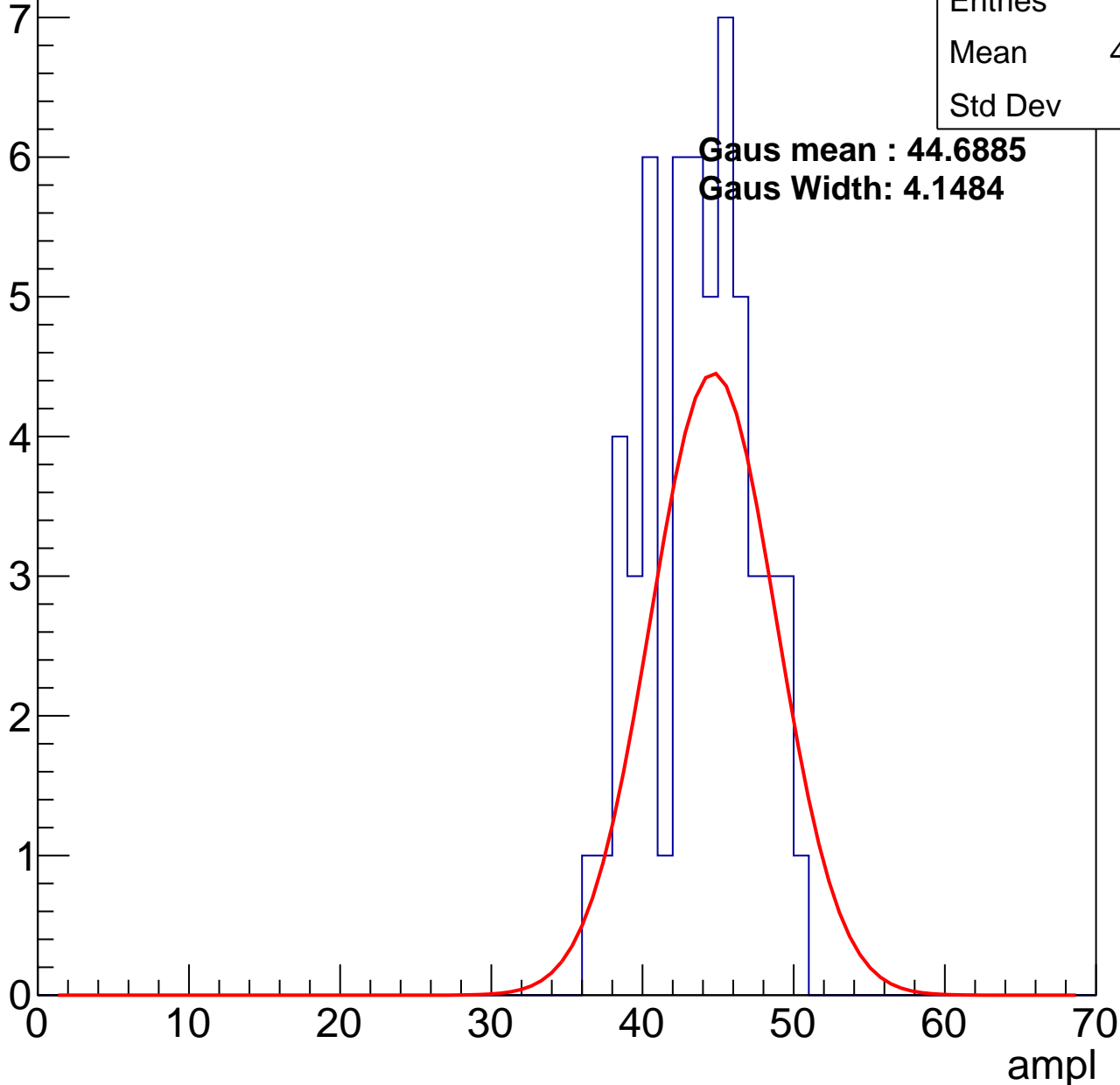
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	43.27
Std Dev	3.44

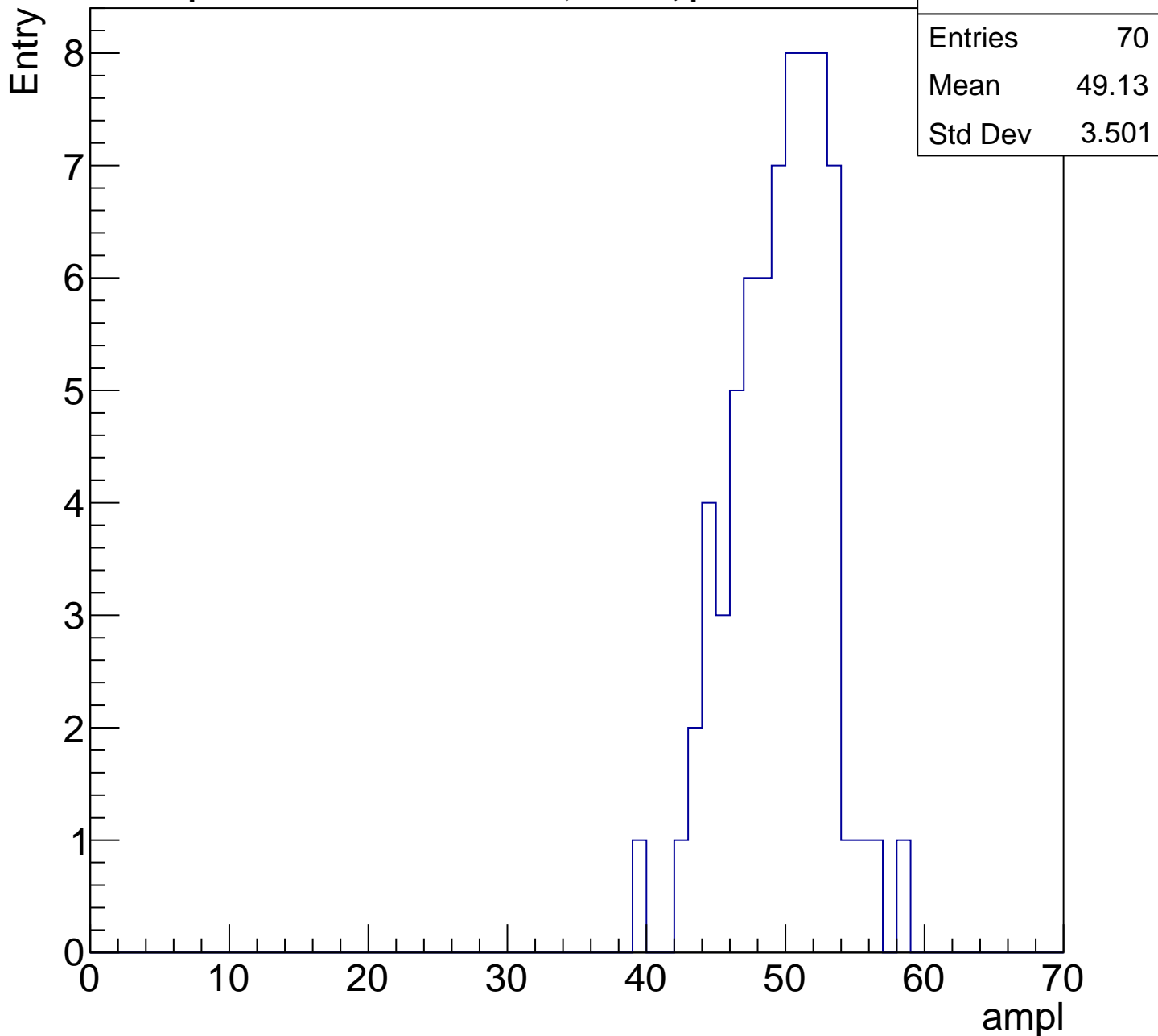
**Gaus mean : 44.6885**

**Gaus Width: 4.1484**



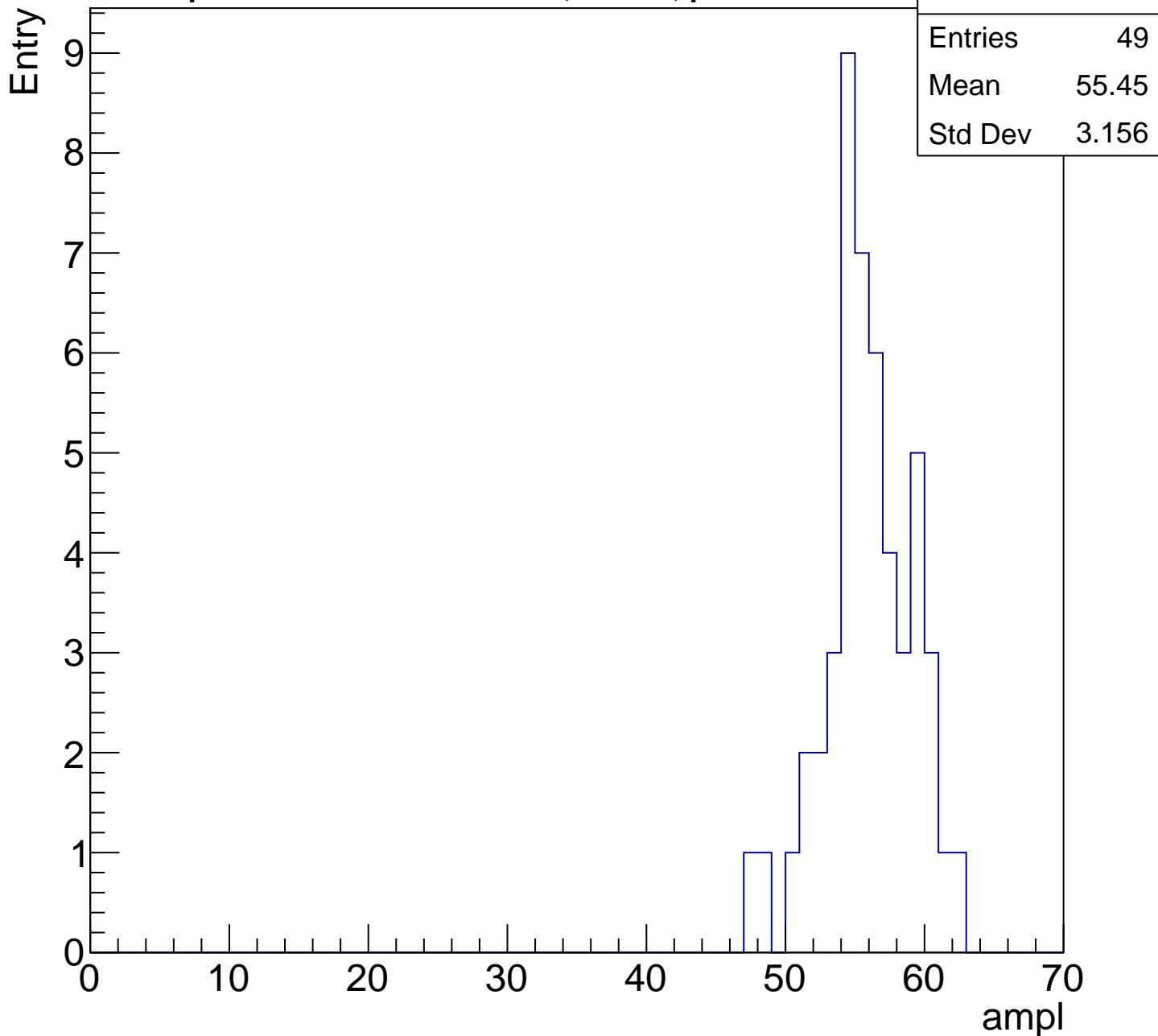
# B1L003S, U3-ch21, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2



# B1L003S, U3-ch21, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

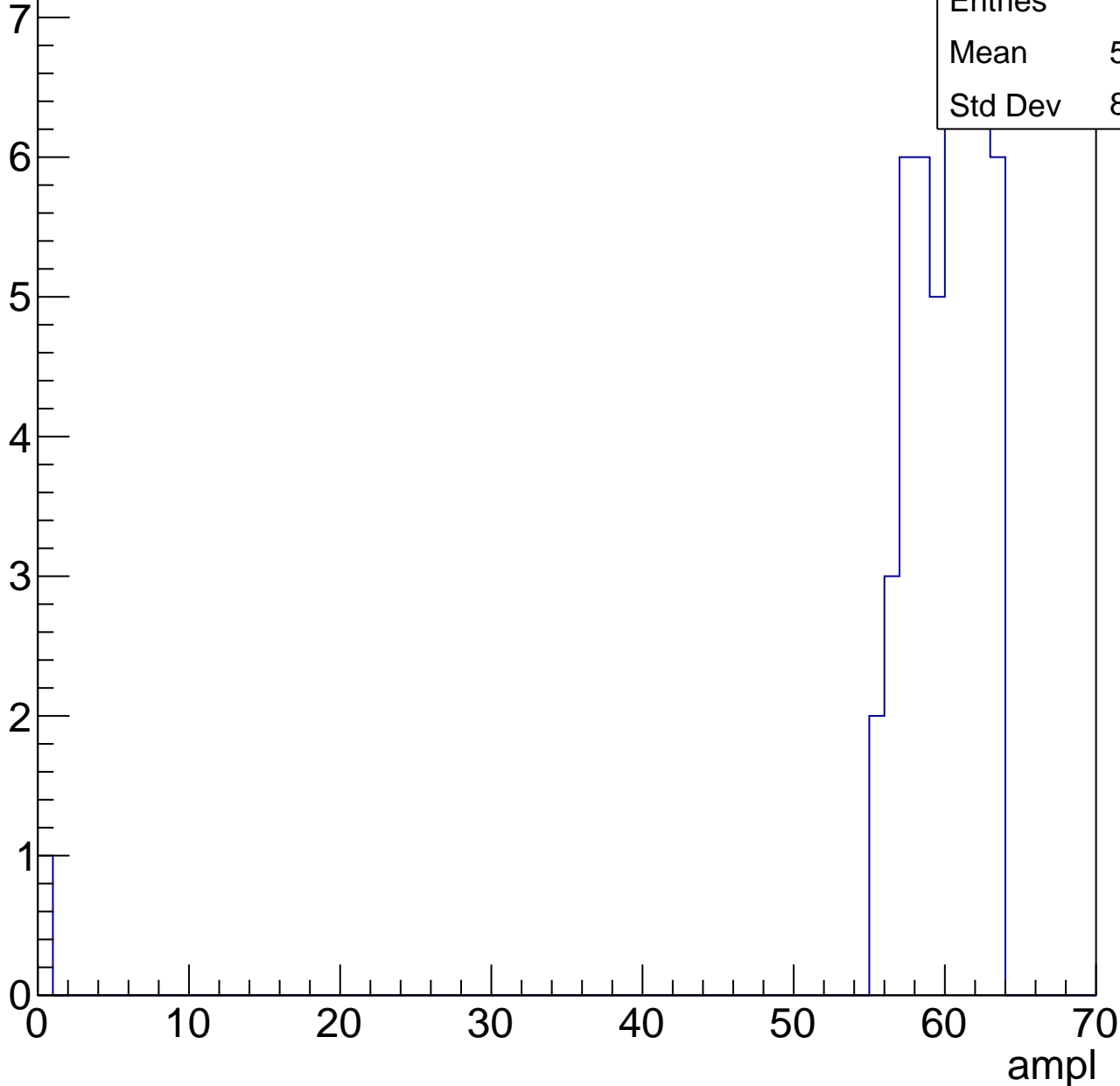


# B1L003S, U3-ch21, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

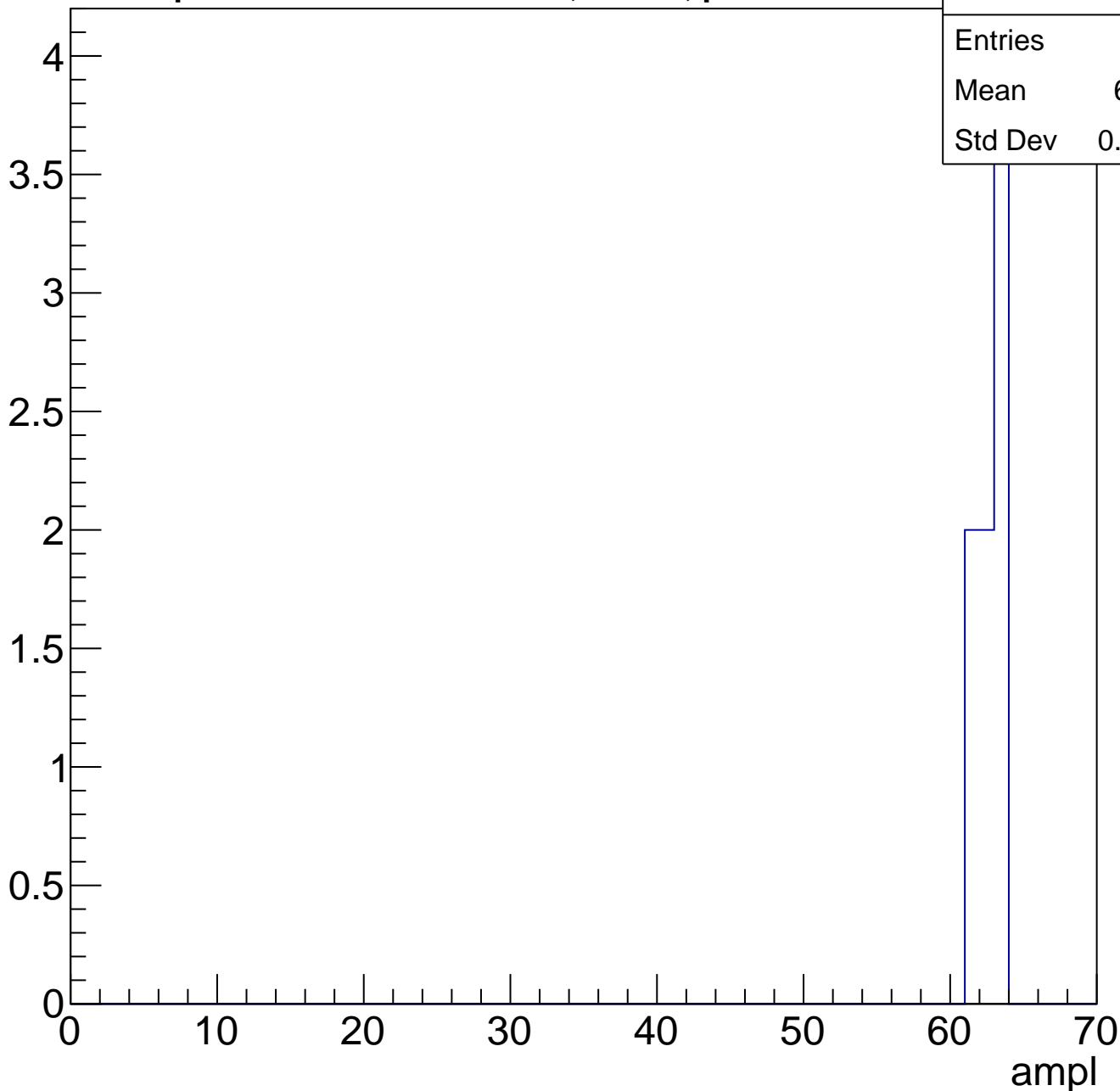
Entries	50
Mean	58.44
Std Dev	8.658



# B1L003S, U3-ch21, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch21, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U3-ch22, adc0

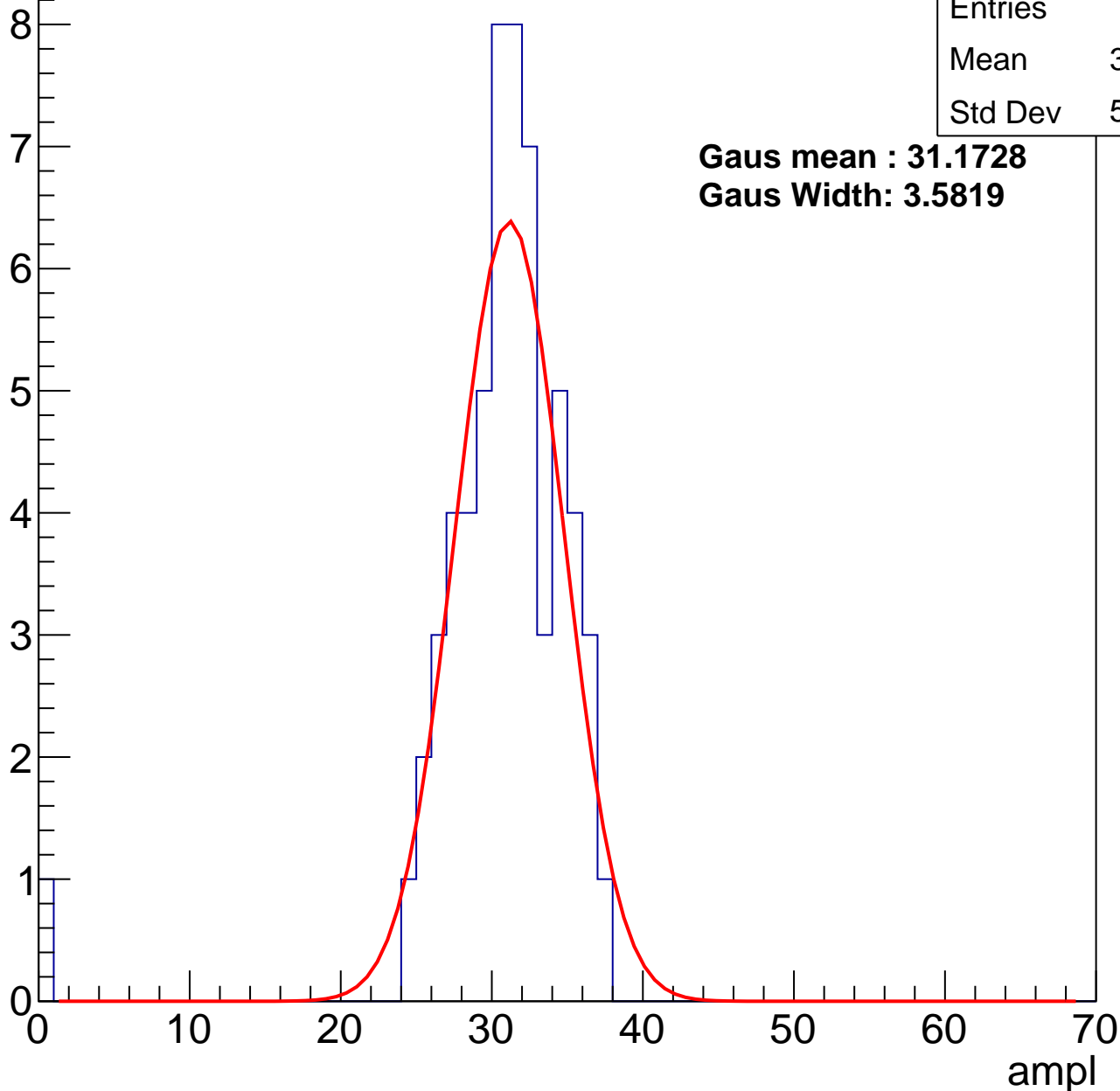
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	30.22
Std Dev	5.022

**Gaus mean : 31.1728**

**Gaus Width: 3.5819**



# B1L003S, U3-ch22, adc1

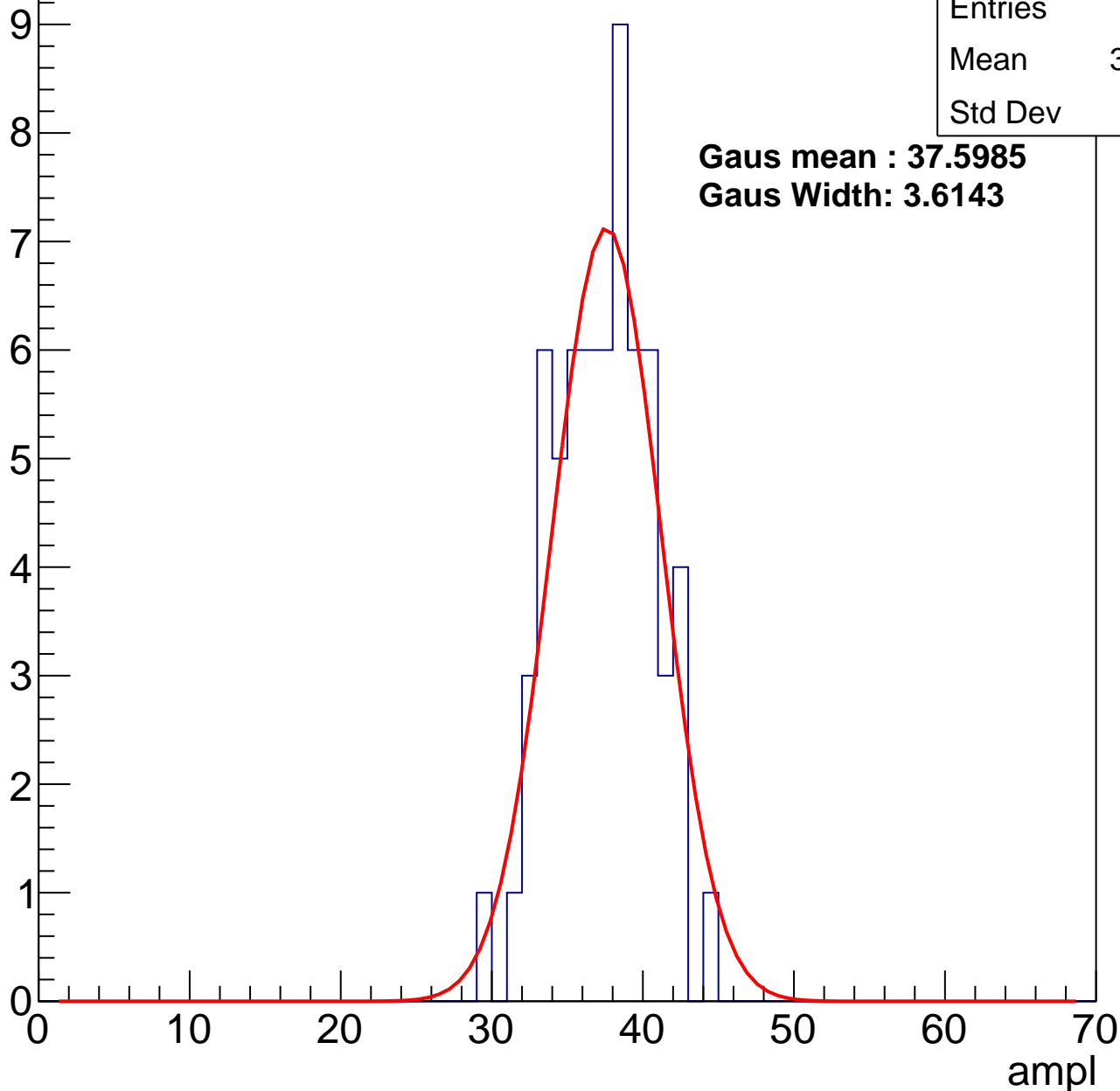
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	36.87
Std Dev	3.16

**Gaus mean : 37.5985**

**Gaus Width: 3.6143**



# B1L003S, U3-ch22, adc2

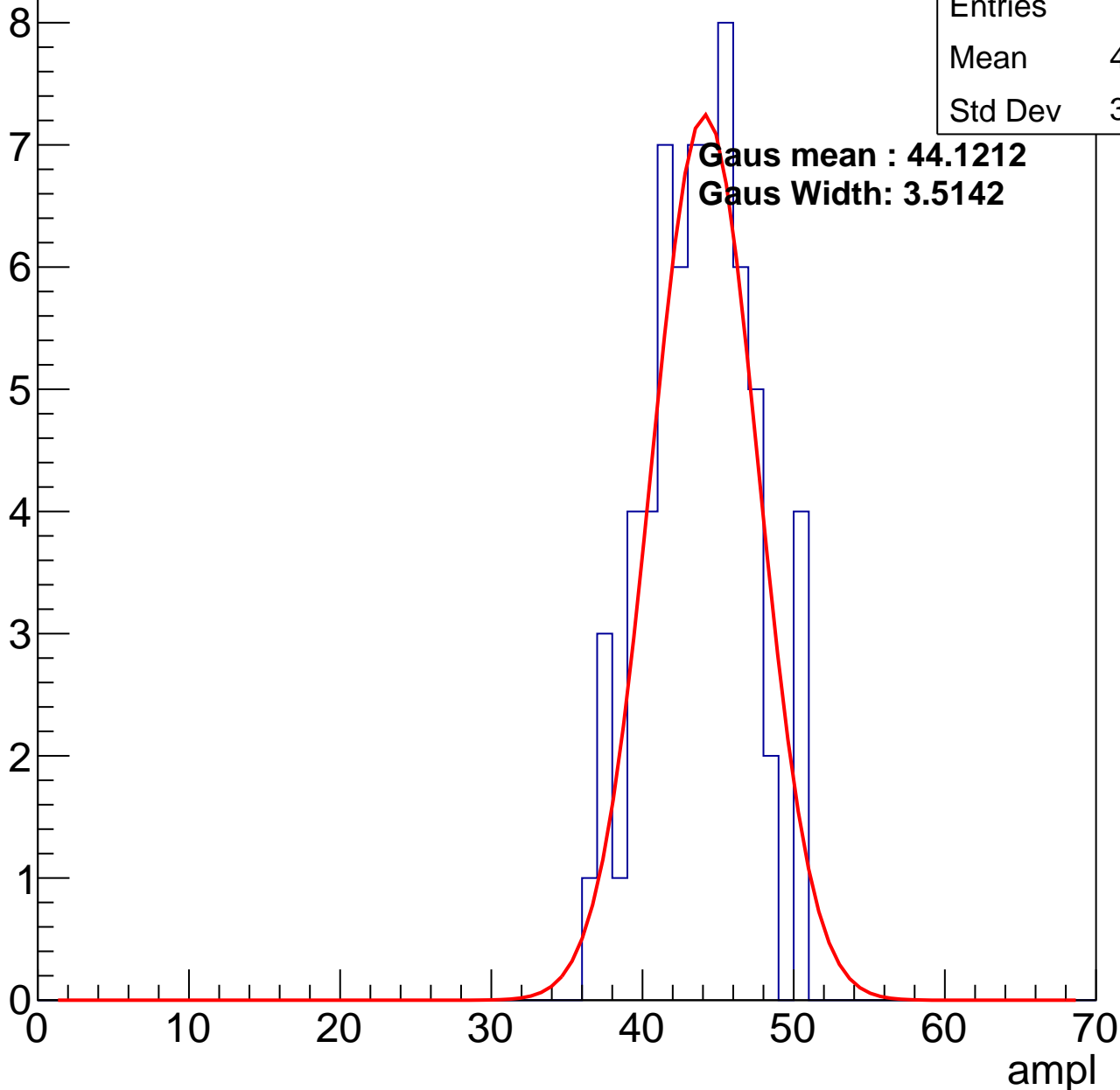
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	43.32
Std Dev	3.347

**Gaus mean : 44.1212**

**Gaus Width: 3.5142**



# B1L003S, U3-ch22, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	78
Mean	50.36
Std Dev	3.534

Entry

10

8

6

4

2

0

0

10

20

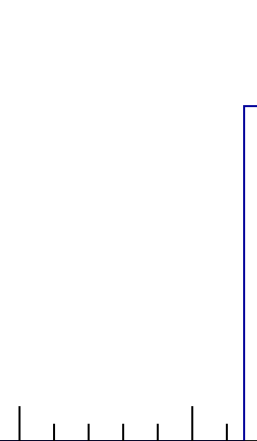
30

40

50

60

ampl

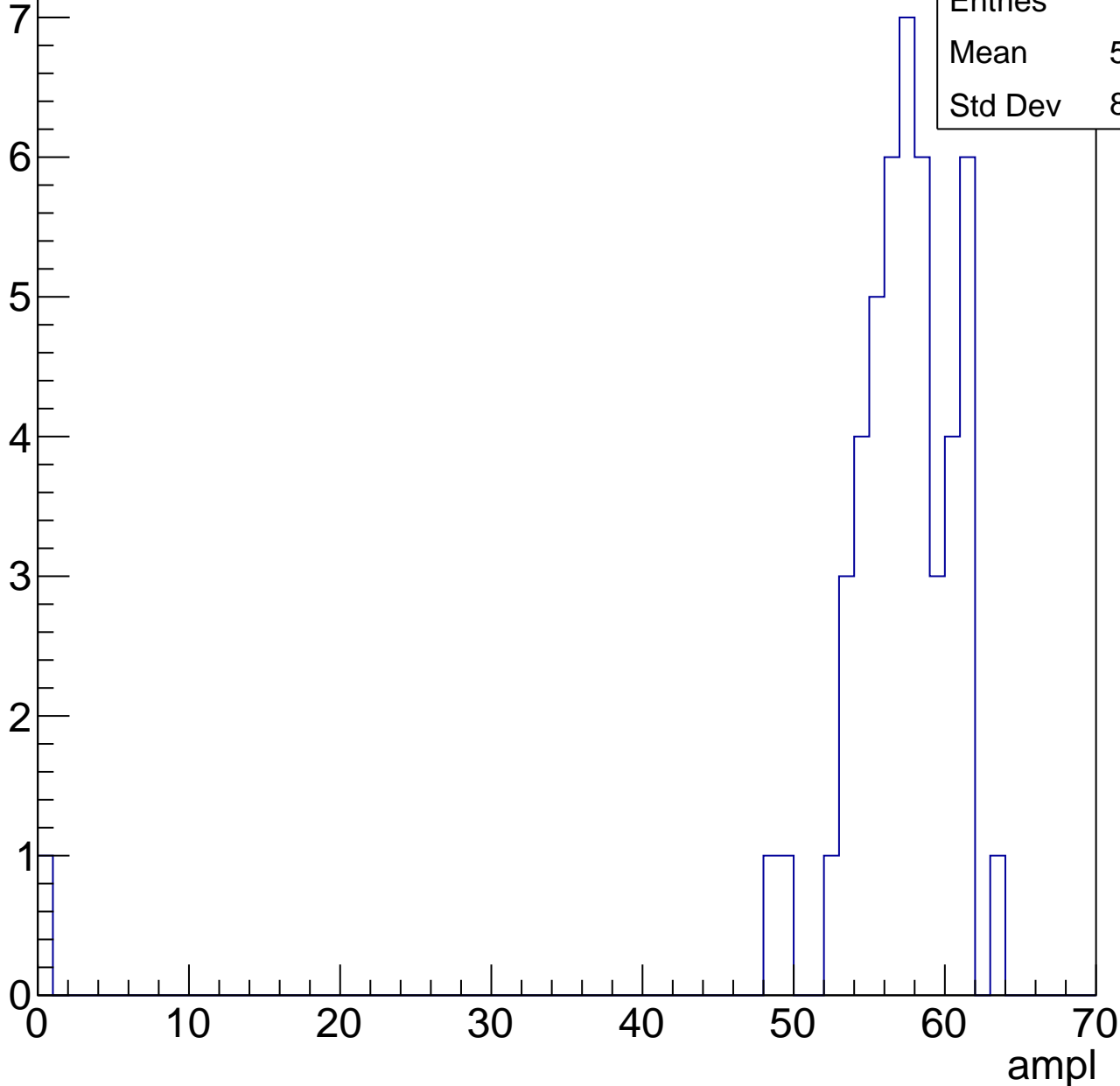


# B1L003S, U3-ch22, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	49
Mean	55.67
Std Dev	8.606

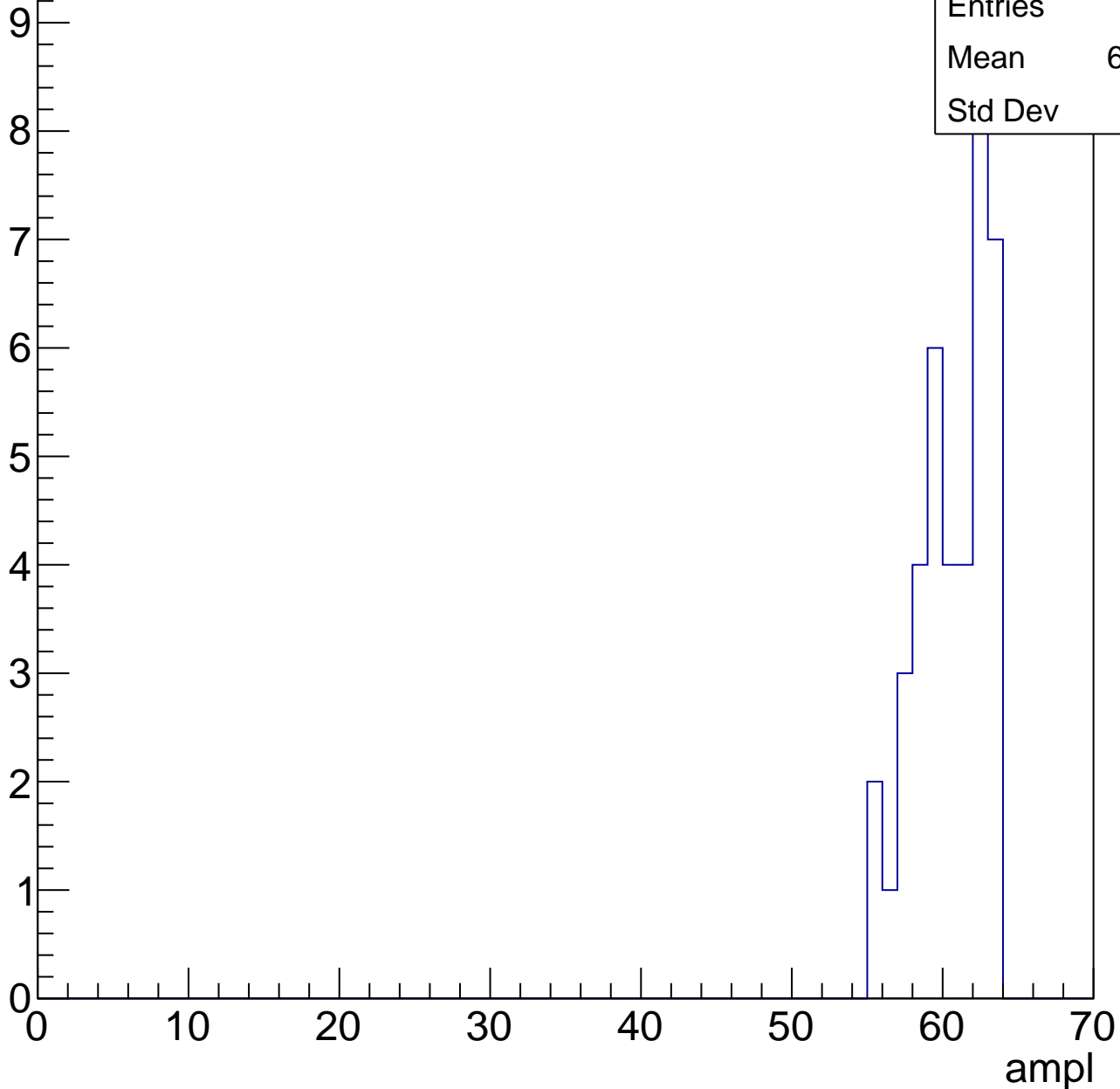


# B1L003S, U3-ch22, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	40
Mean	60.15
Std Dev	2.33



# B1L003S, U3-ch22, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch22, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U3-ch23, adc0

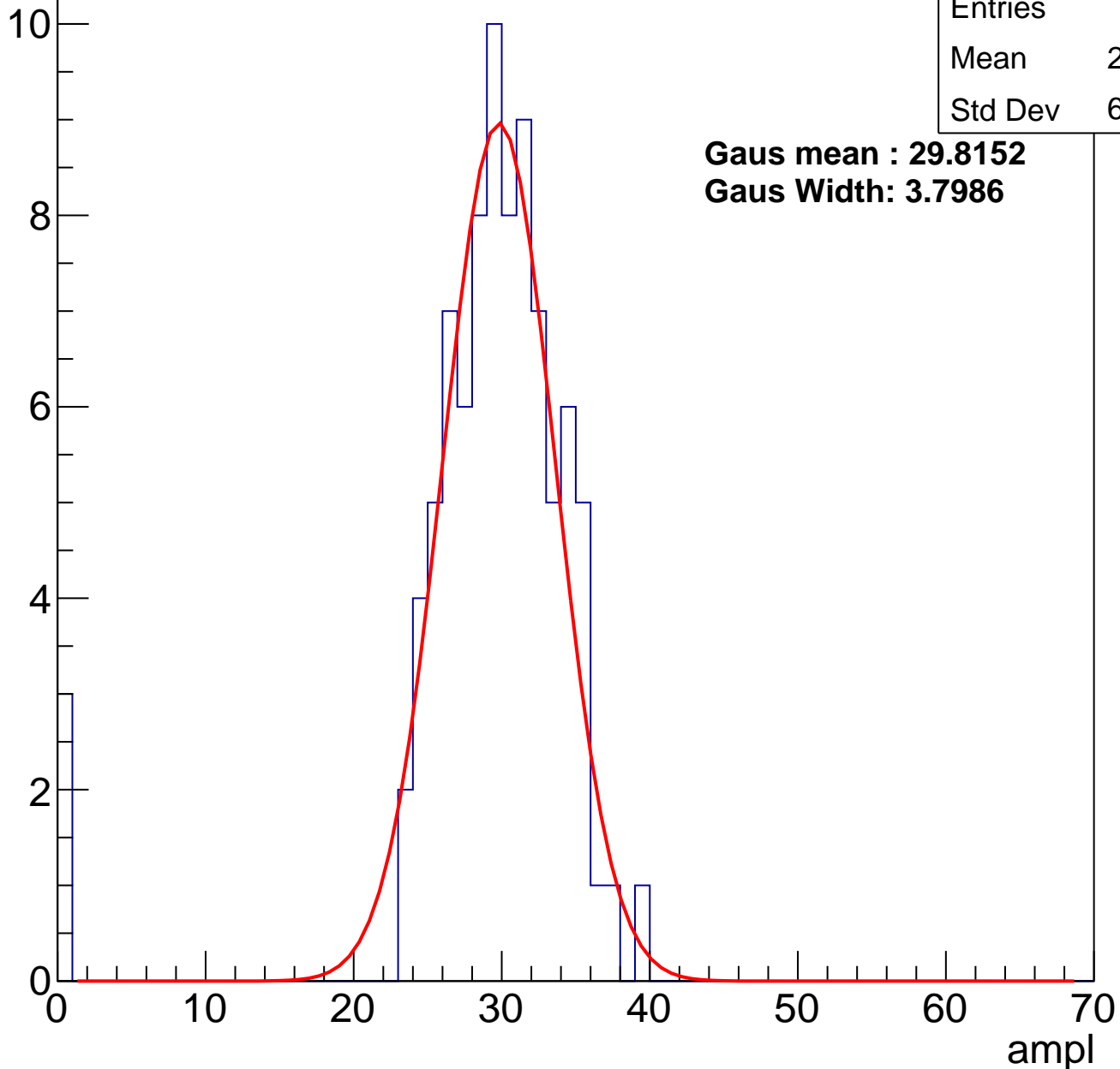
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	88
Mean	28.68
Std Dev	6.388

**Gaus mean : 29.8152**

**Gaus Width: 3.7986**

Entry



# B1L003S, U3-ch23, adc1

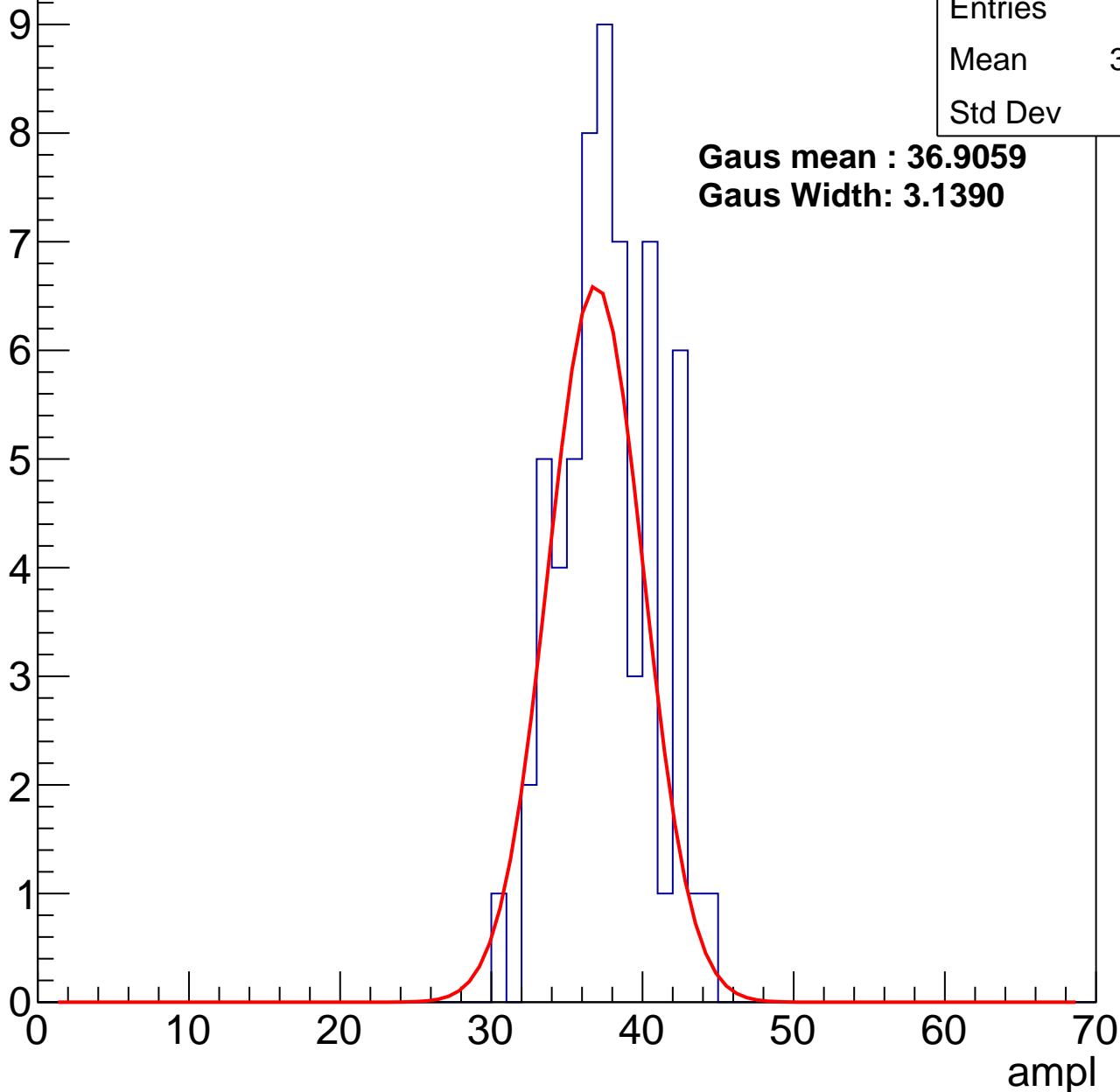
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	37.23
Std Dev	3.09

**Gaus mean : 36.9059**

**Gaus Width: 3.1390**



# B1L003S, U3-ch23, adc2

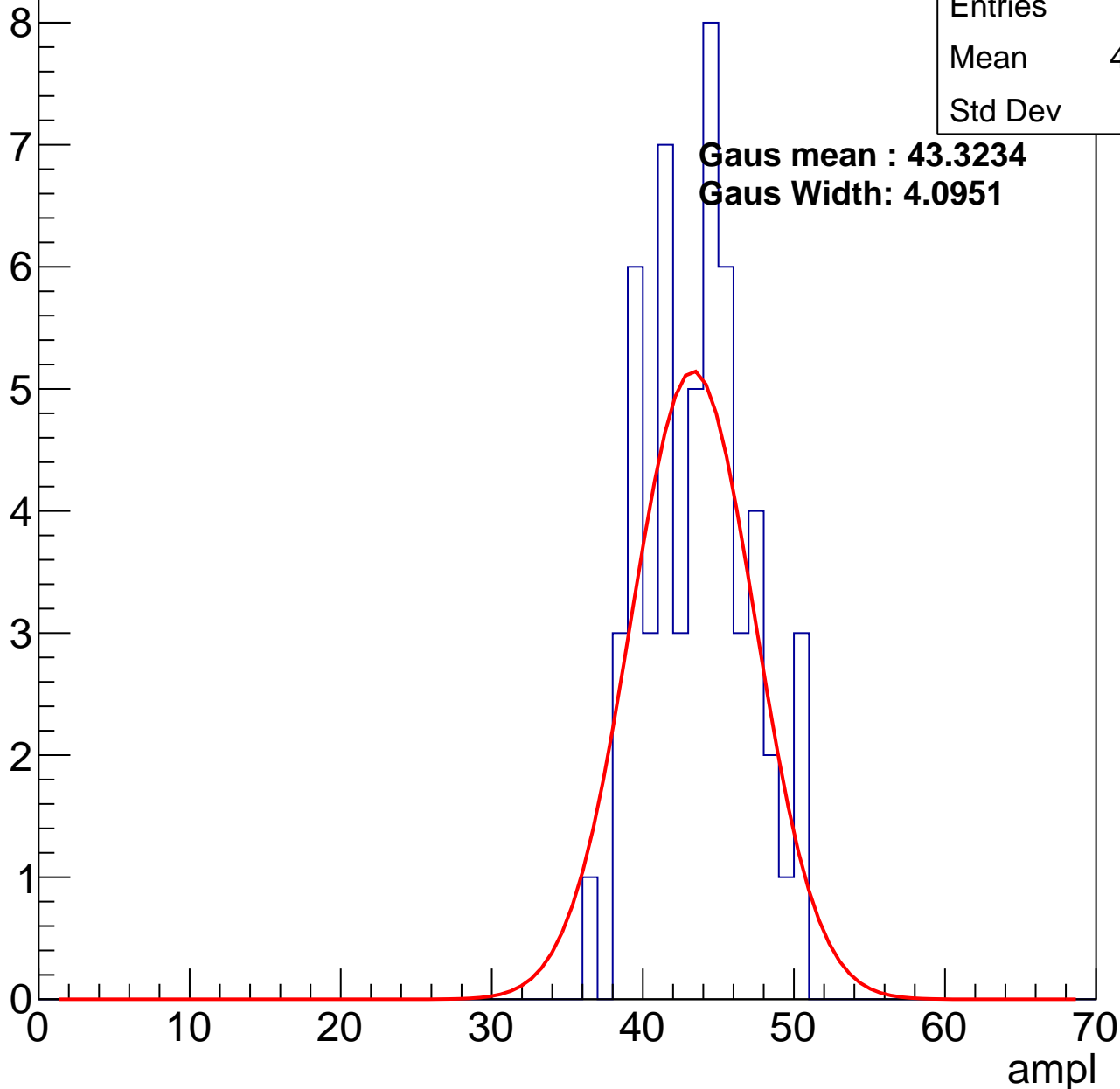
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	43.18
Std Dev	3.39

**Gaus mean : 43.3234**

**Gaus Width: 4.0951**

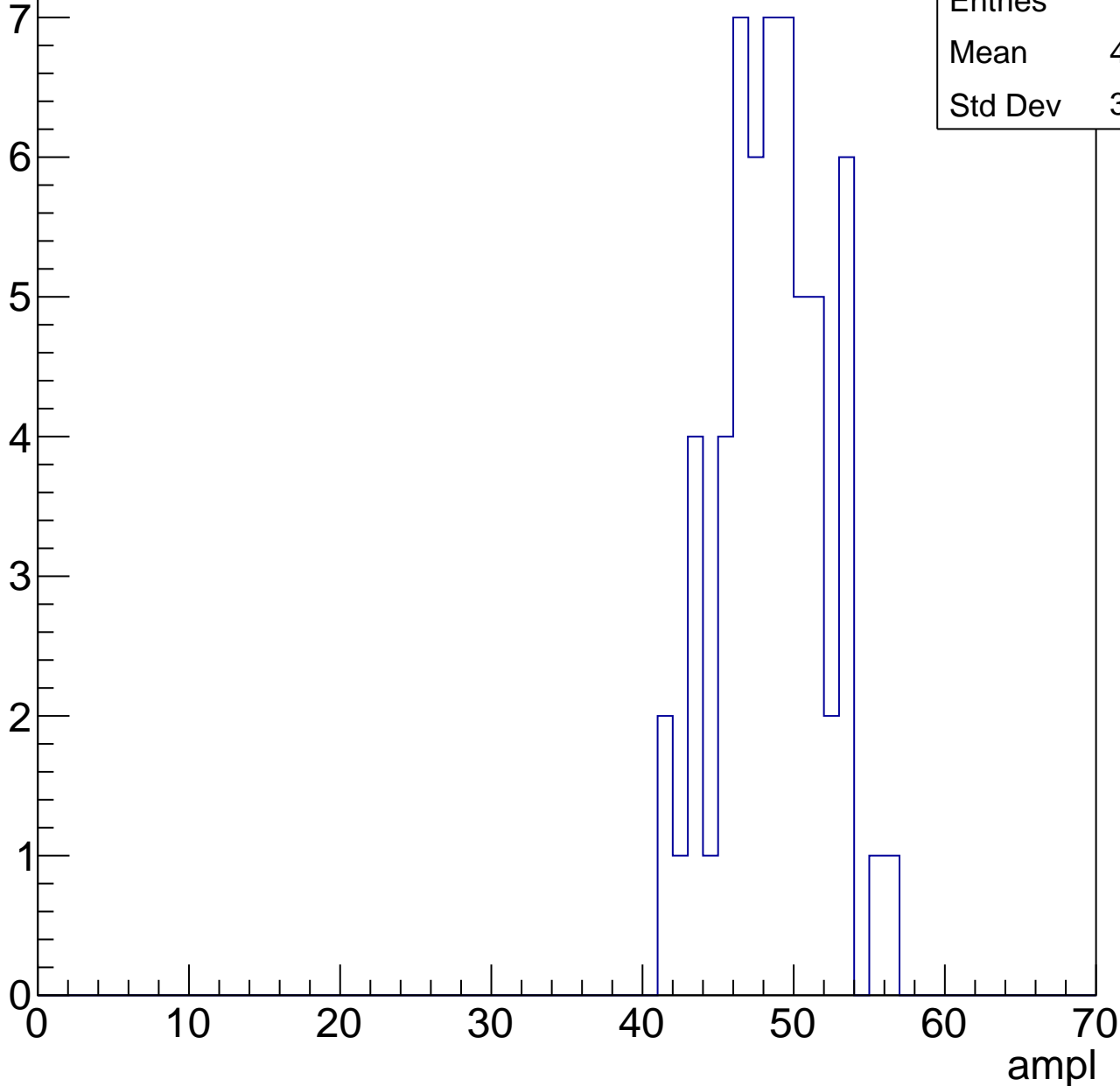


# B1L003S, U3-ch23, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

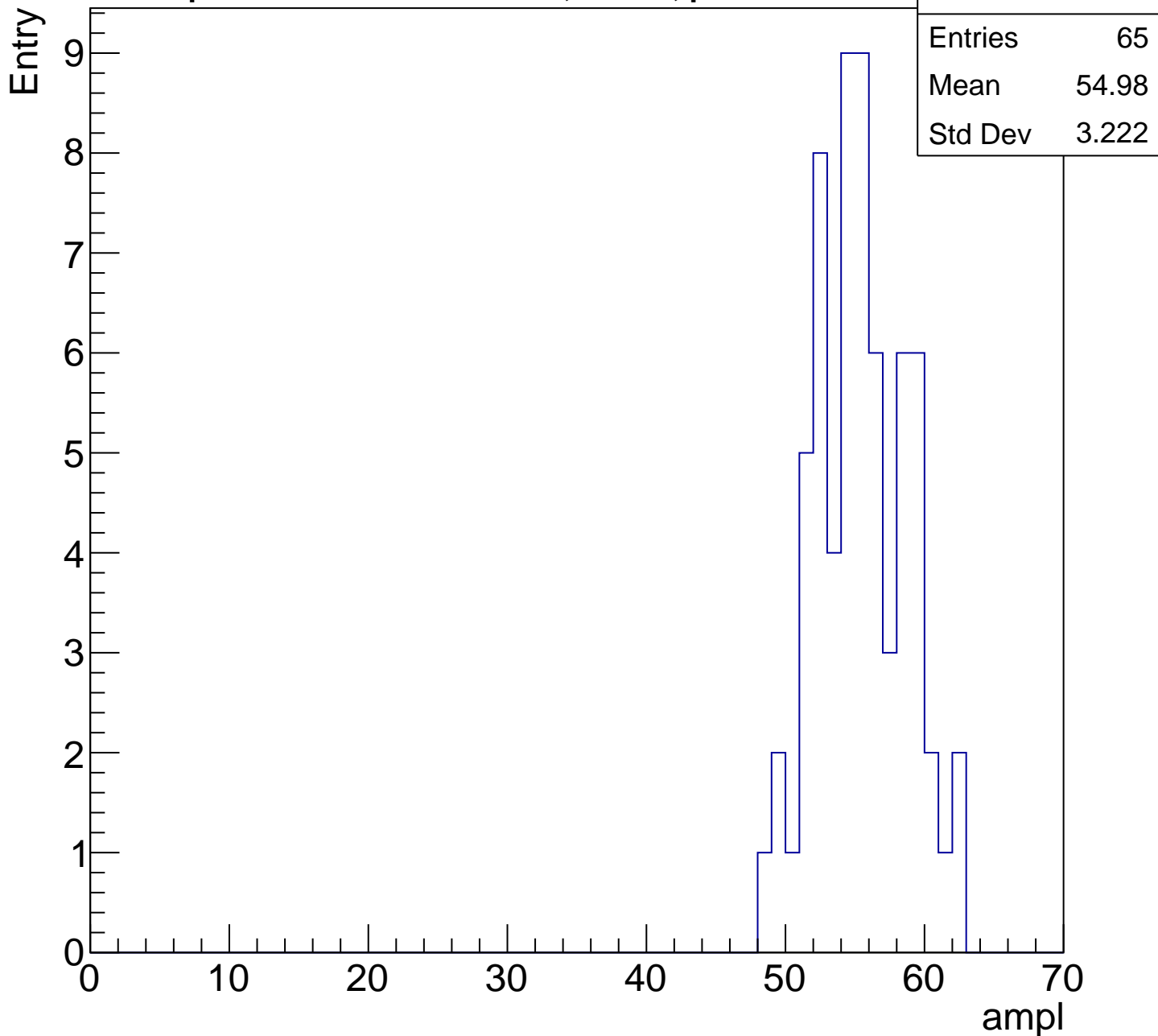
Entry

Entries	59
Mean	48.15
Std Dev	3.409



# B1L003S, U3-ch23, adc4

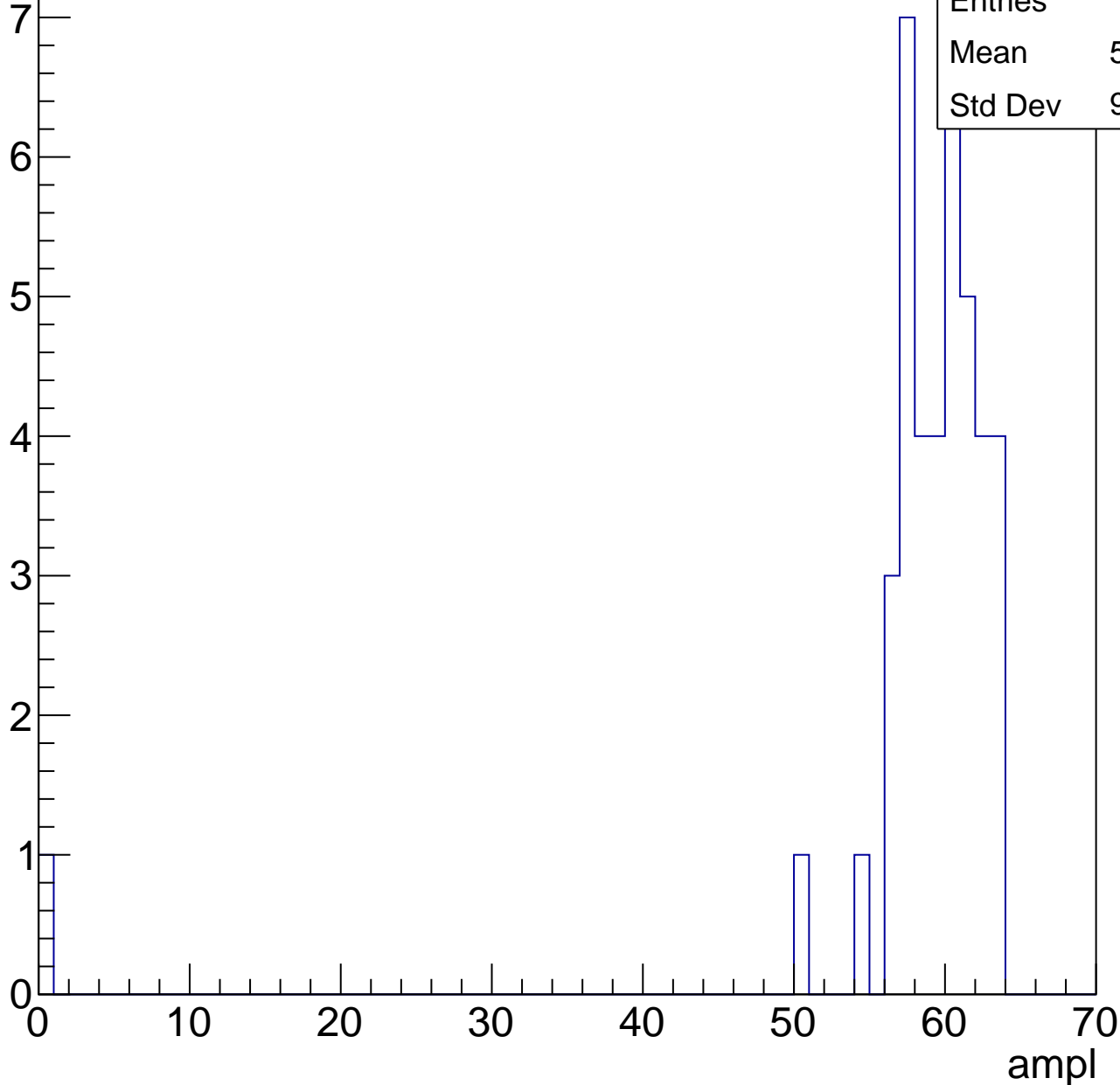
calib\_packv5\_042523\_0143.root, FC#13, port D2



# B1L003S, U3-ch23, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

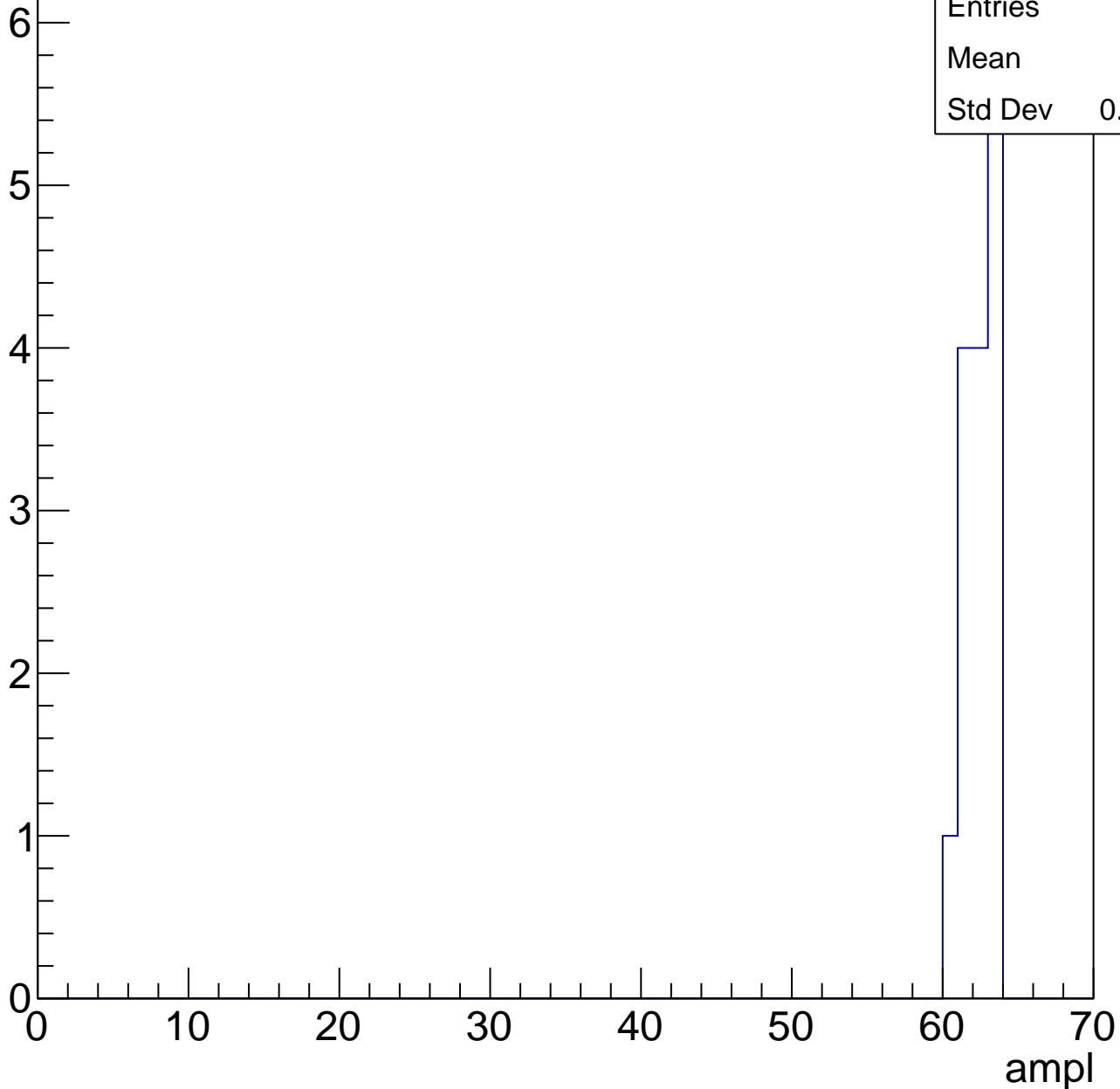


# B1L003S, U3-ch23, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	15
Mean	62
Std Dev	0.9661





# B1L003S, U3-ch23, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U3-ch24, adc0

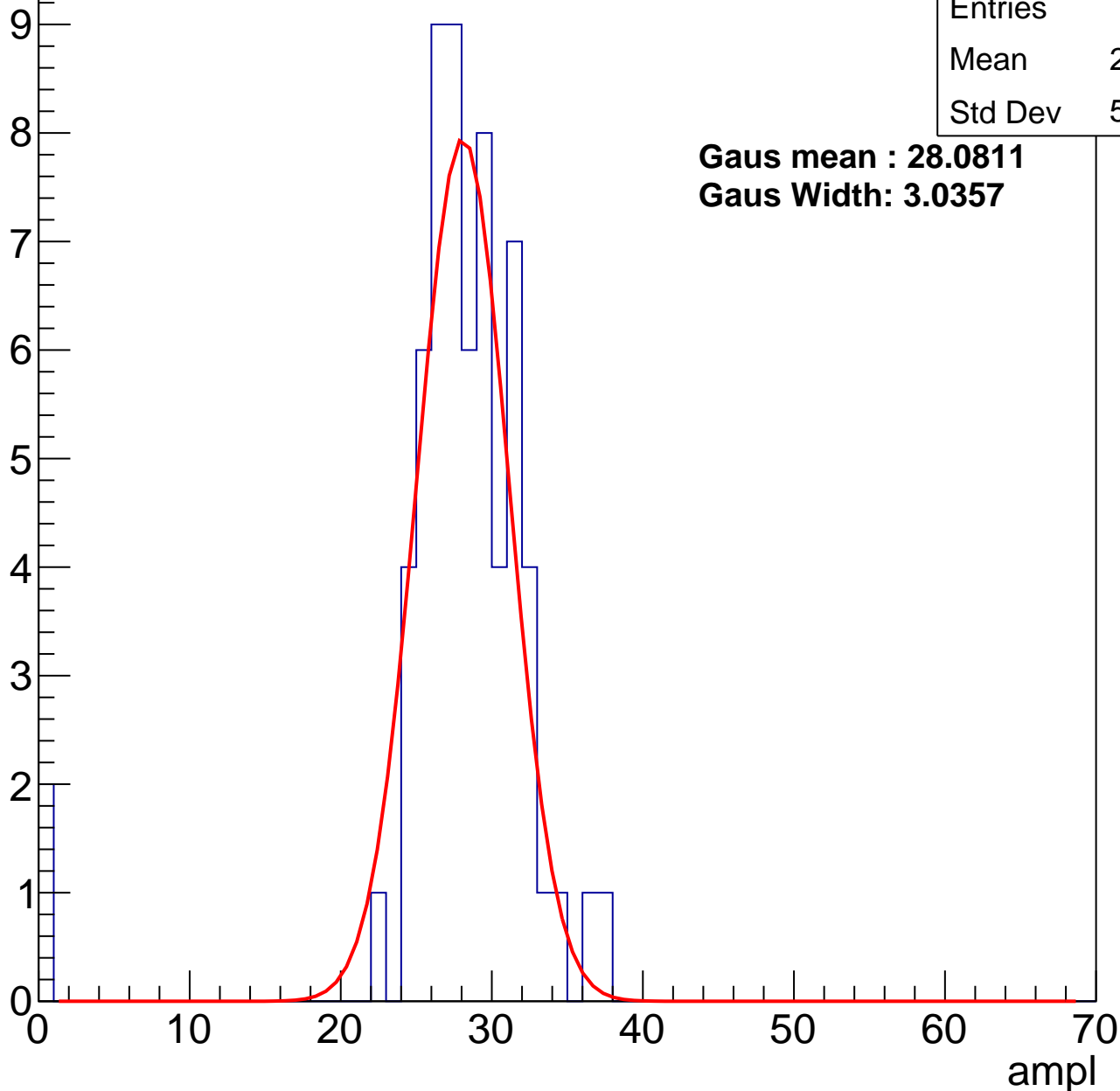
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	27.34
Std Dev	5.723

**Gaus mean : 28.0811**

**Gaus Width: 3.0357**



# B1L003S, U3-ch24, adc1

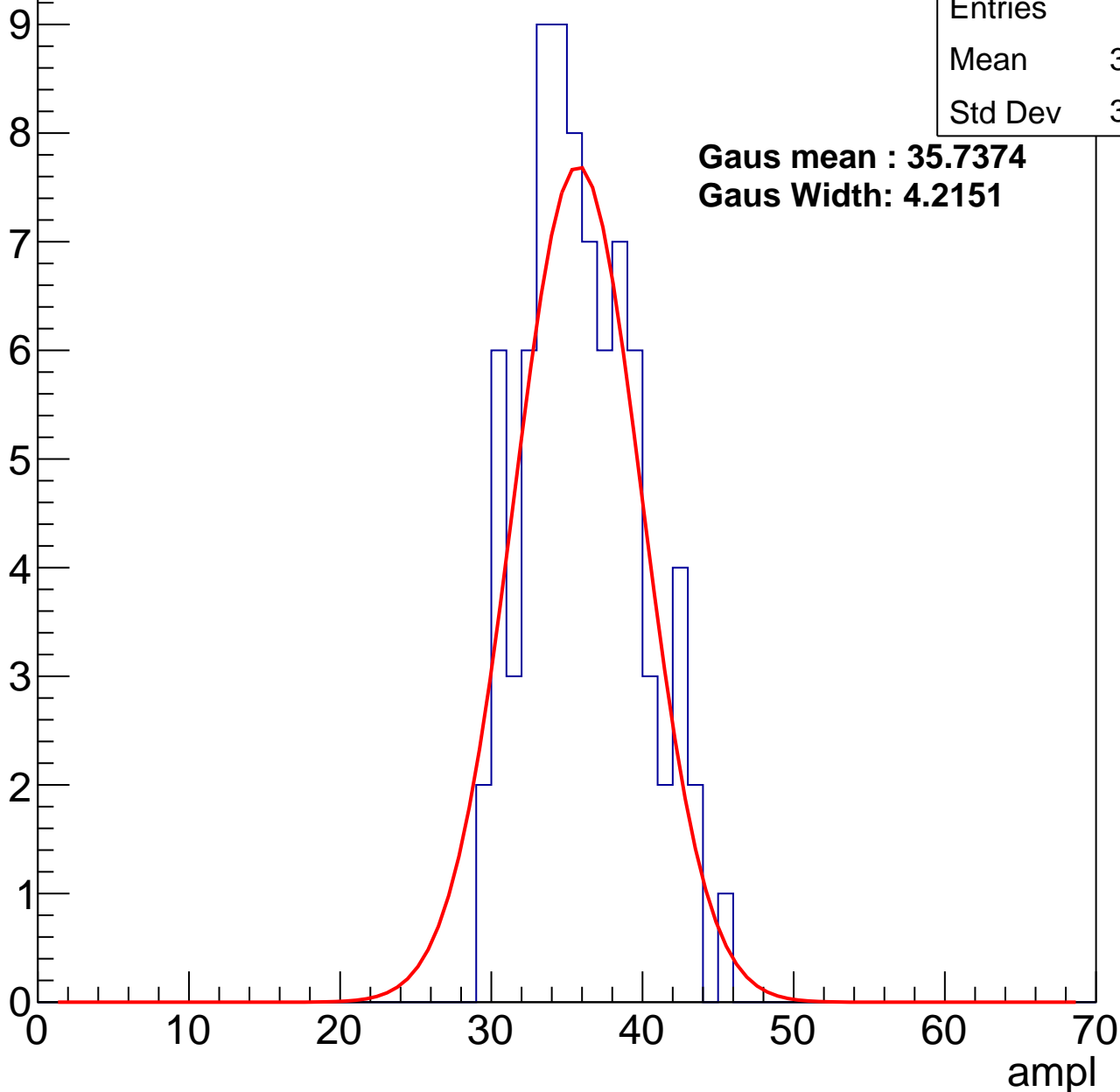
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	81
Mean	35.57
Std Dev	3.692

**Gaus mean : 35.7374**

**Gaus Width: 4.2151**

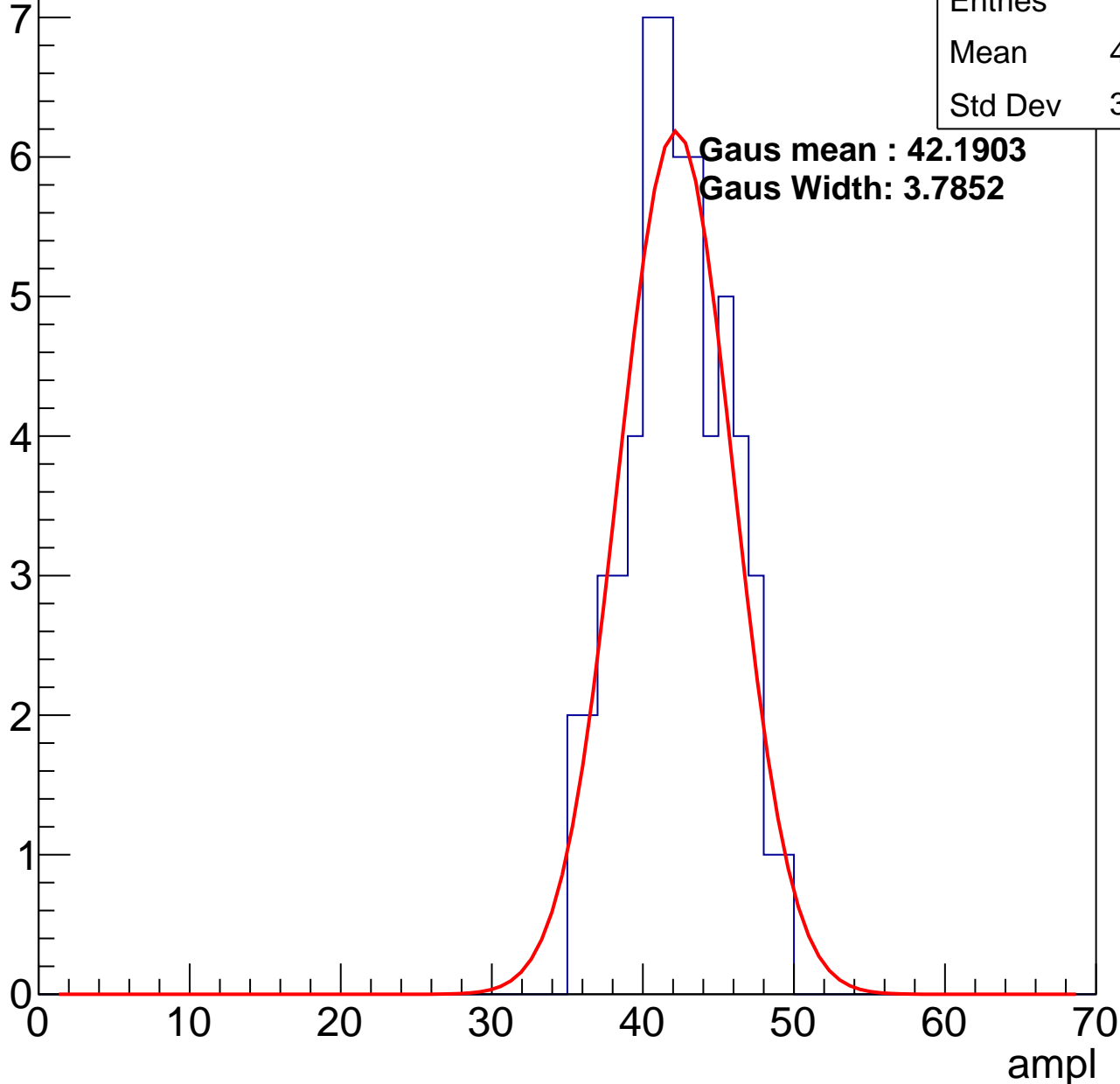


# B1L003S, U3-ch24, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	41.78
Std Dev	3.353

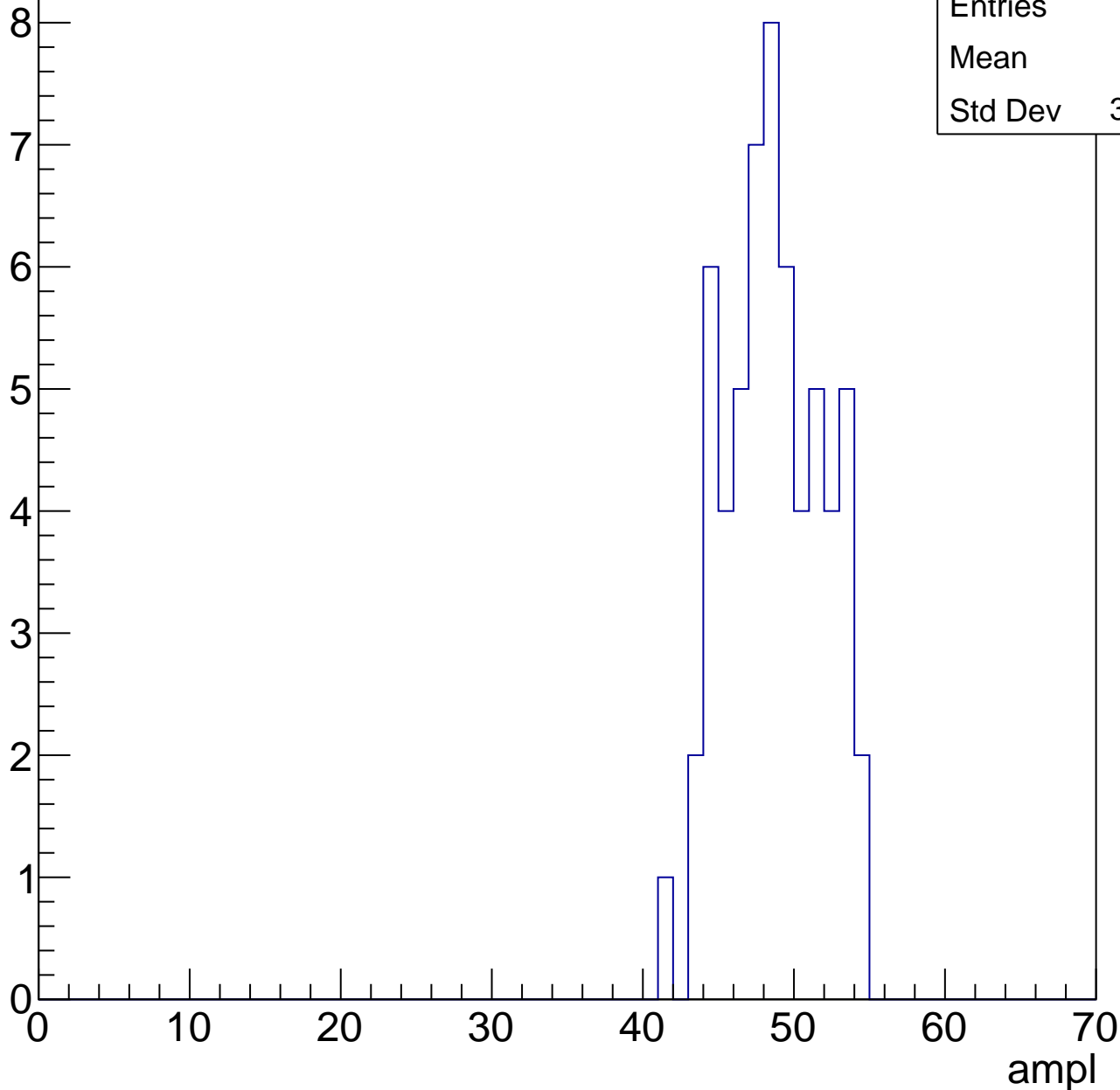


# B1L003S, U3-ch24, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	48.2
Std Dev	3.145

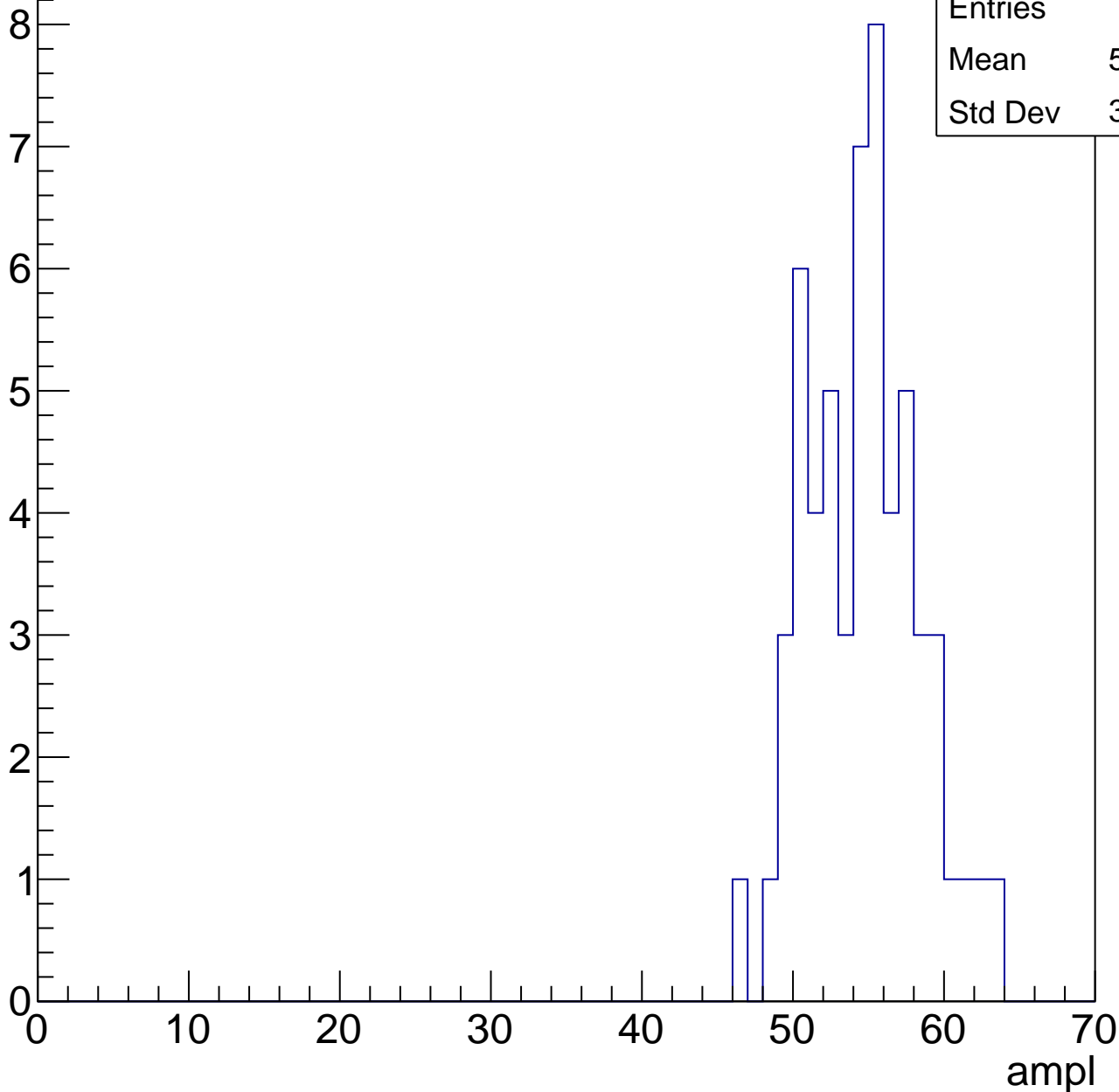


# B1L003S, U3-ch24, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	54.18
Std Dev	3.628

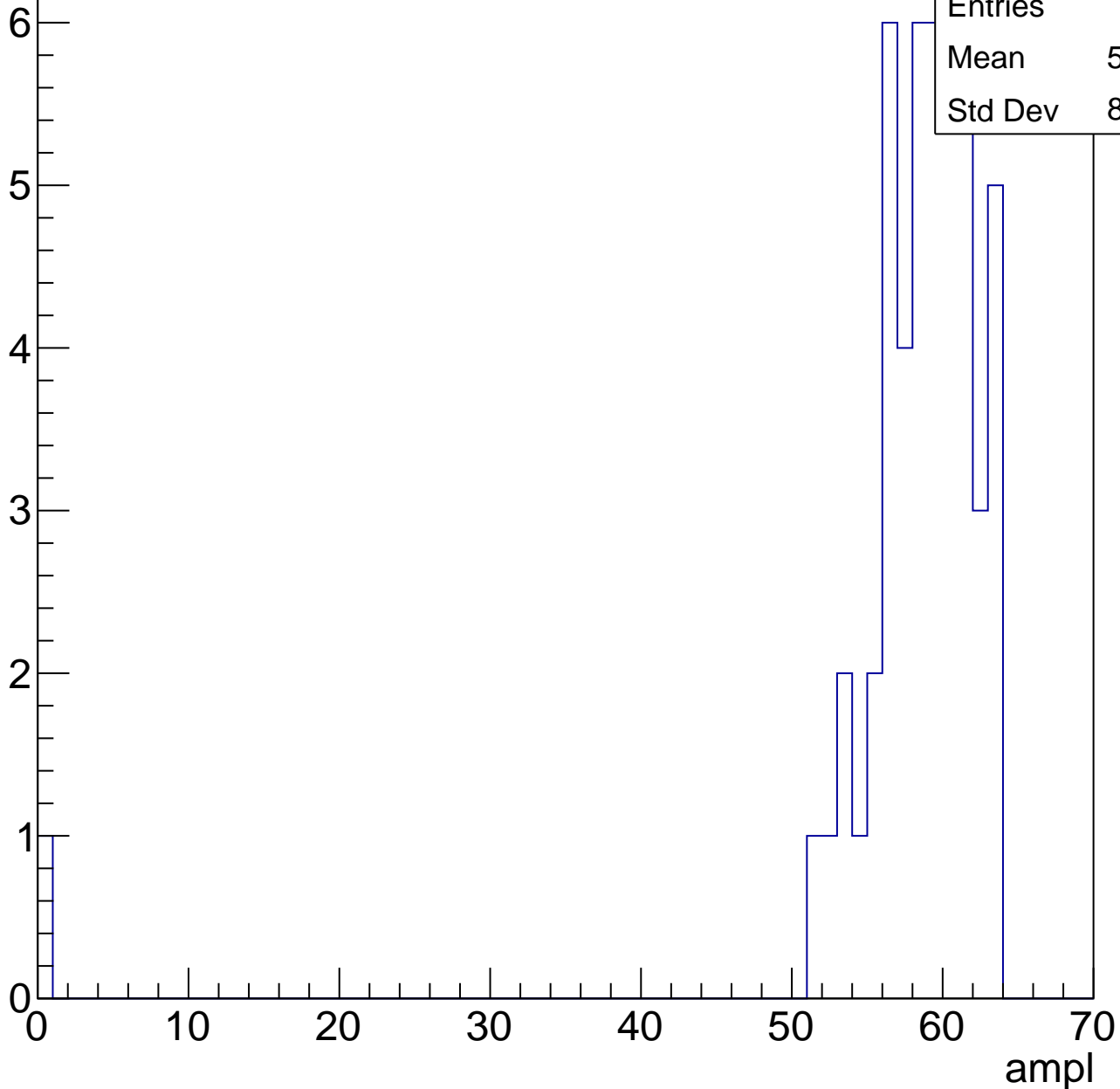


# B1L003S, U3-ch24, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	50
Mean	57.32
Std Dev	8.712

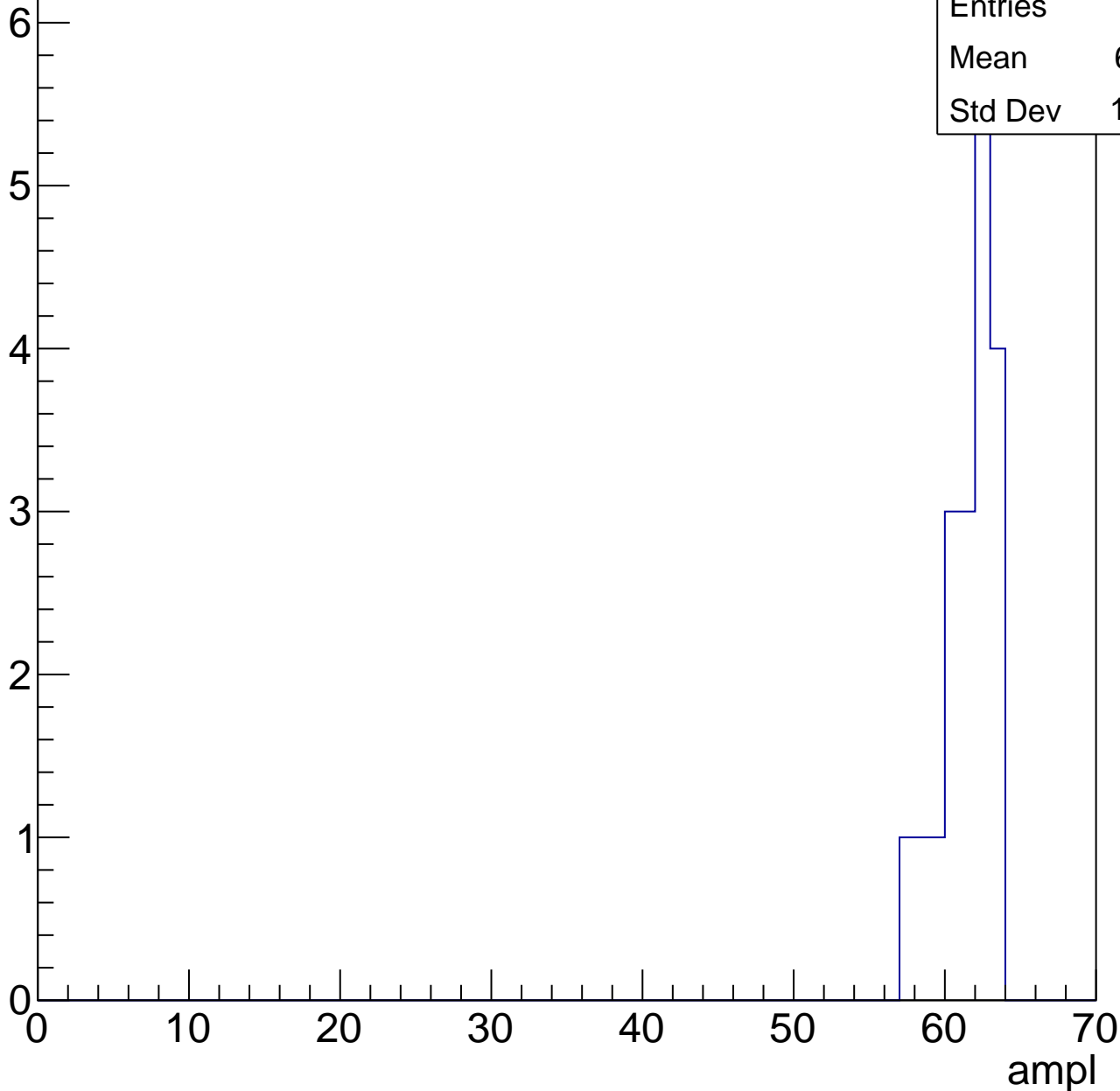


# B1L003S, U3-ch24, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	19
Mean	61.11
Std Dev	1.683





# B1L003S, U3-ch24, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U3-ch25, adc0

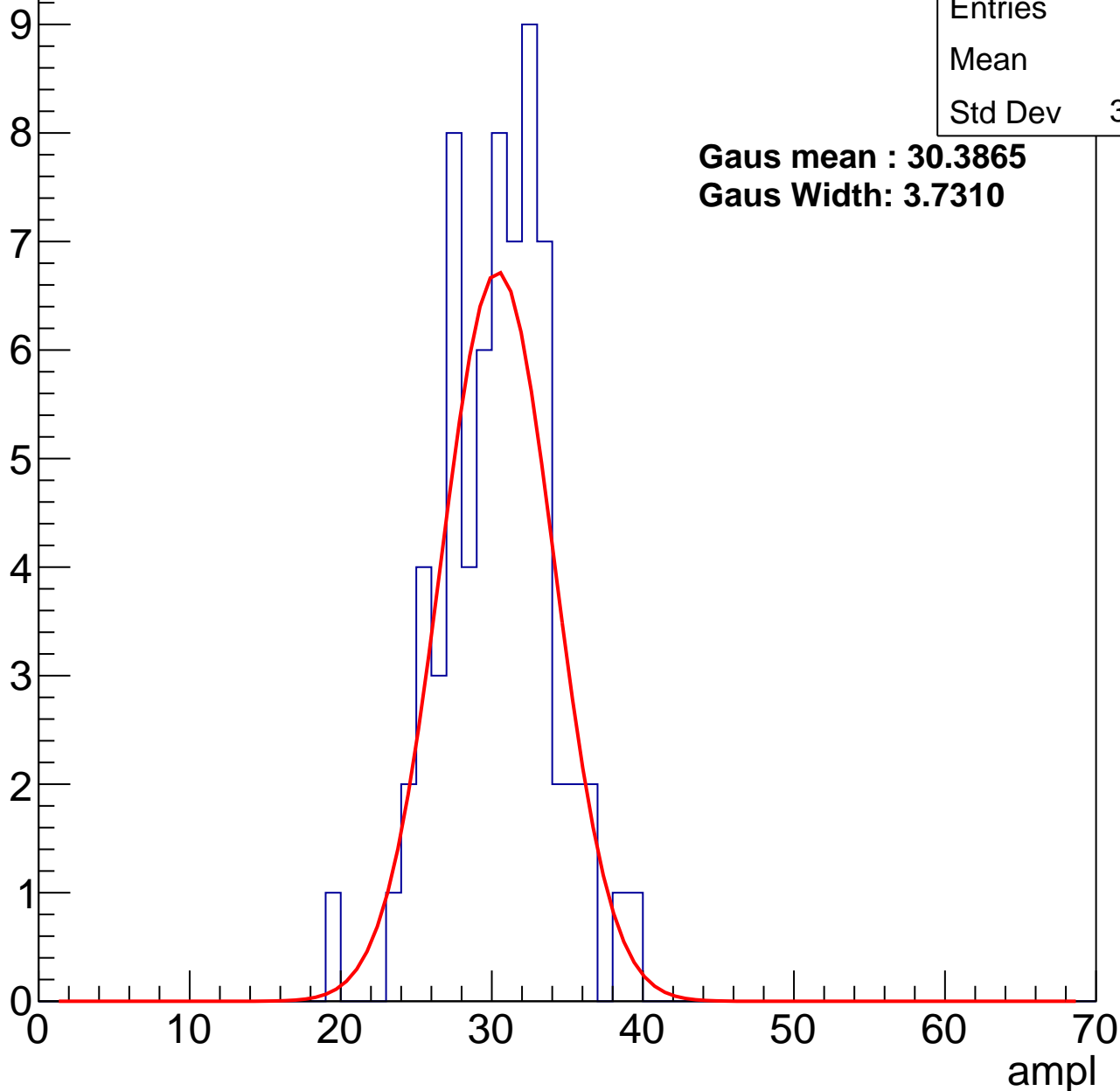
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	29.9
Std Dev	3.614

**Gaus mean : 30.3865**

**Gaus Width: 3.7310**



# B1L003S, U3-ch25, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	66
Mean	37.33
Std Dev	3.461

**Gaus mean : 37.5614**

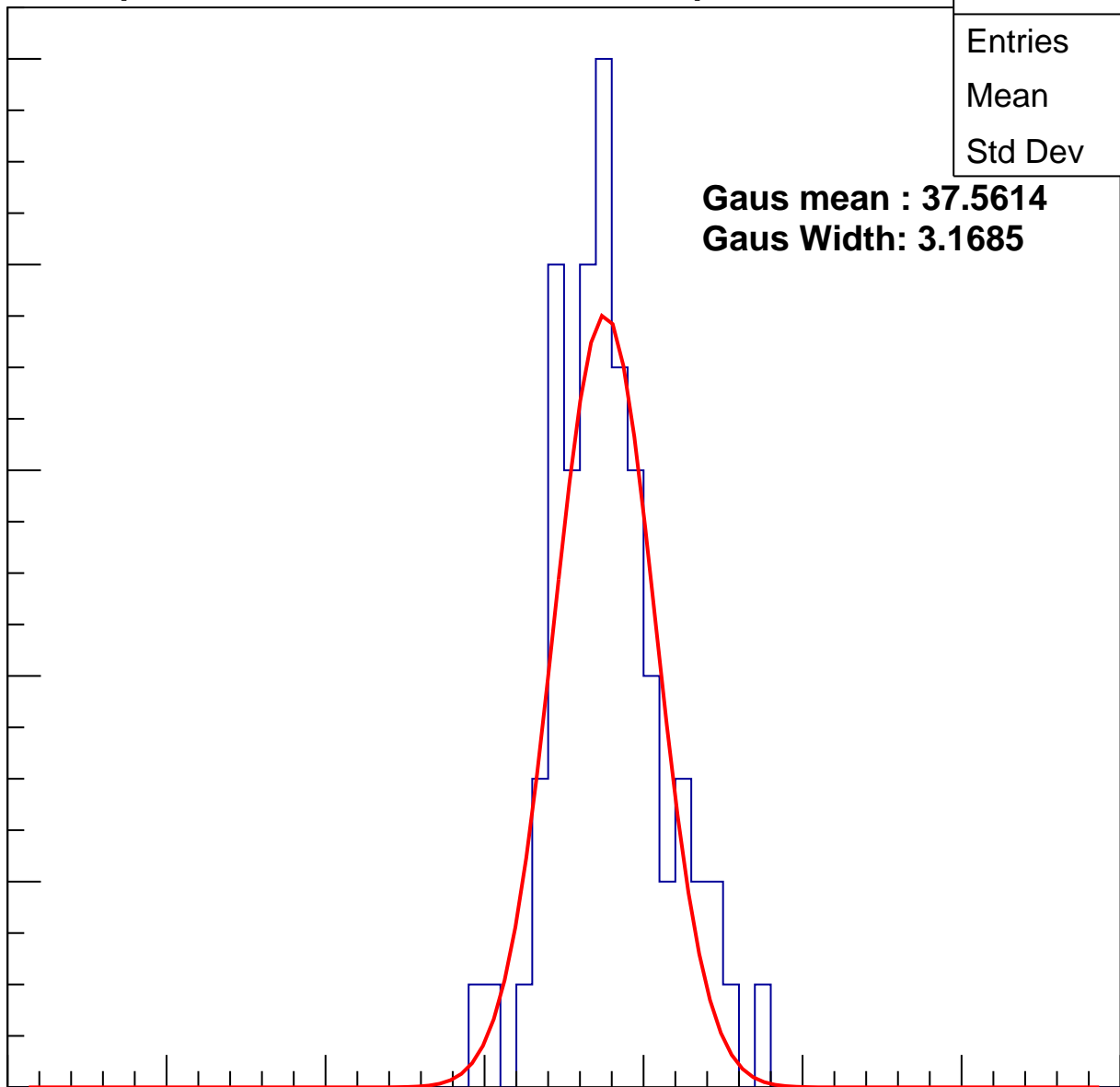
**Gaus Width: 3.1685**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L003S, U3-ch25, adc2

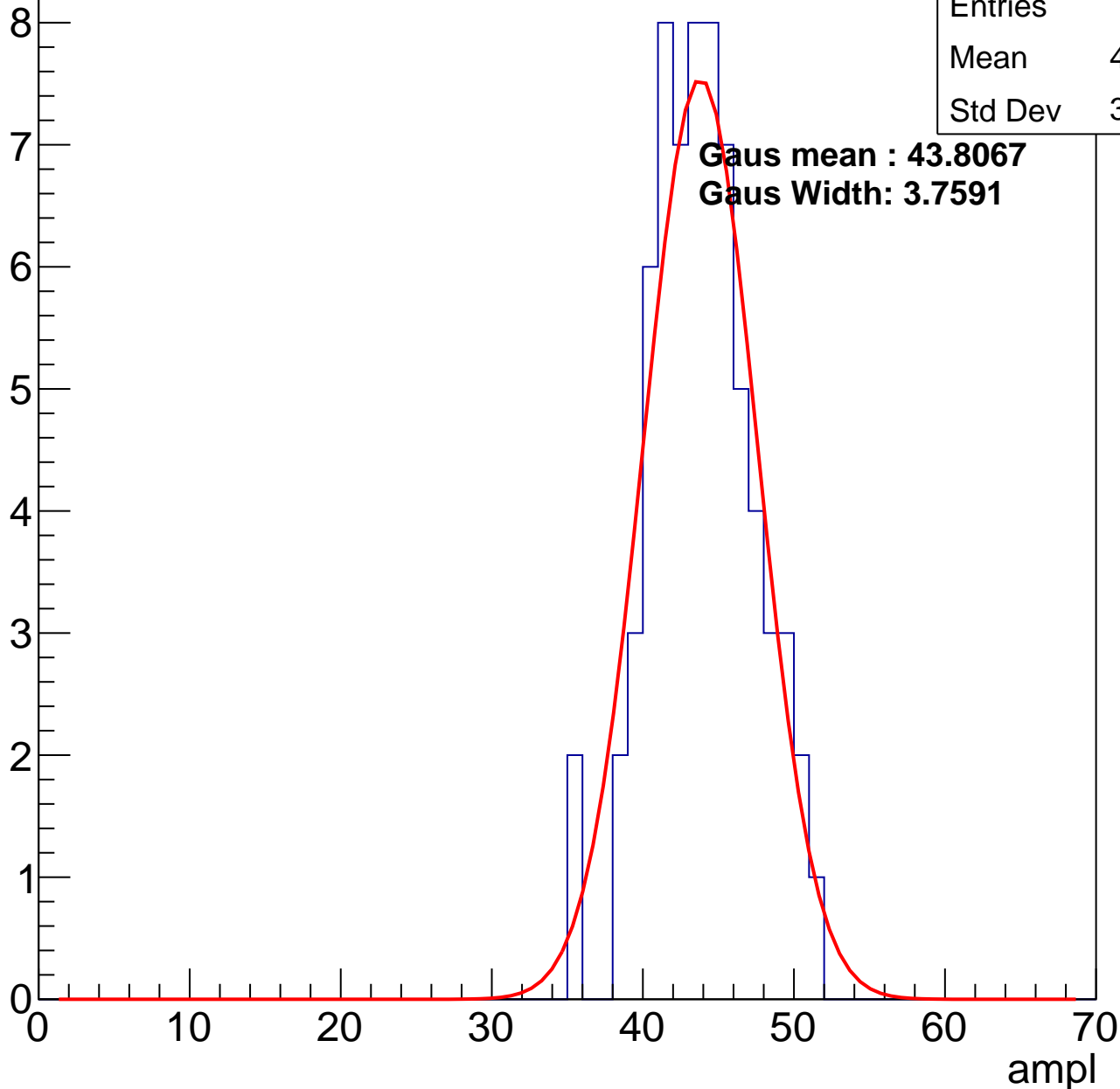
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	43.42
Std Dev	3.398

**Gaus mean : 43.8067**

**Gaus Width: 3.7591**

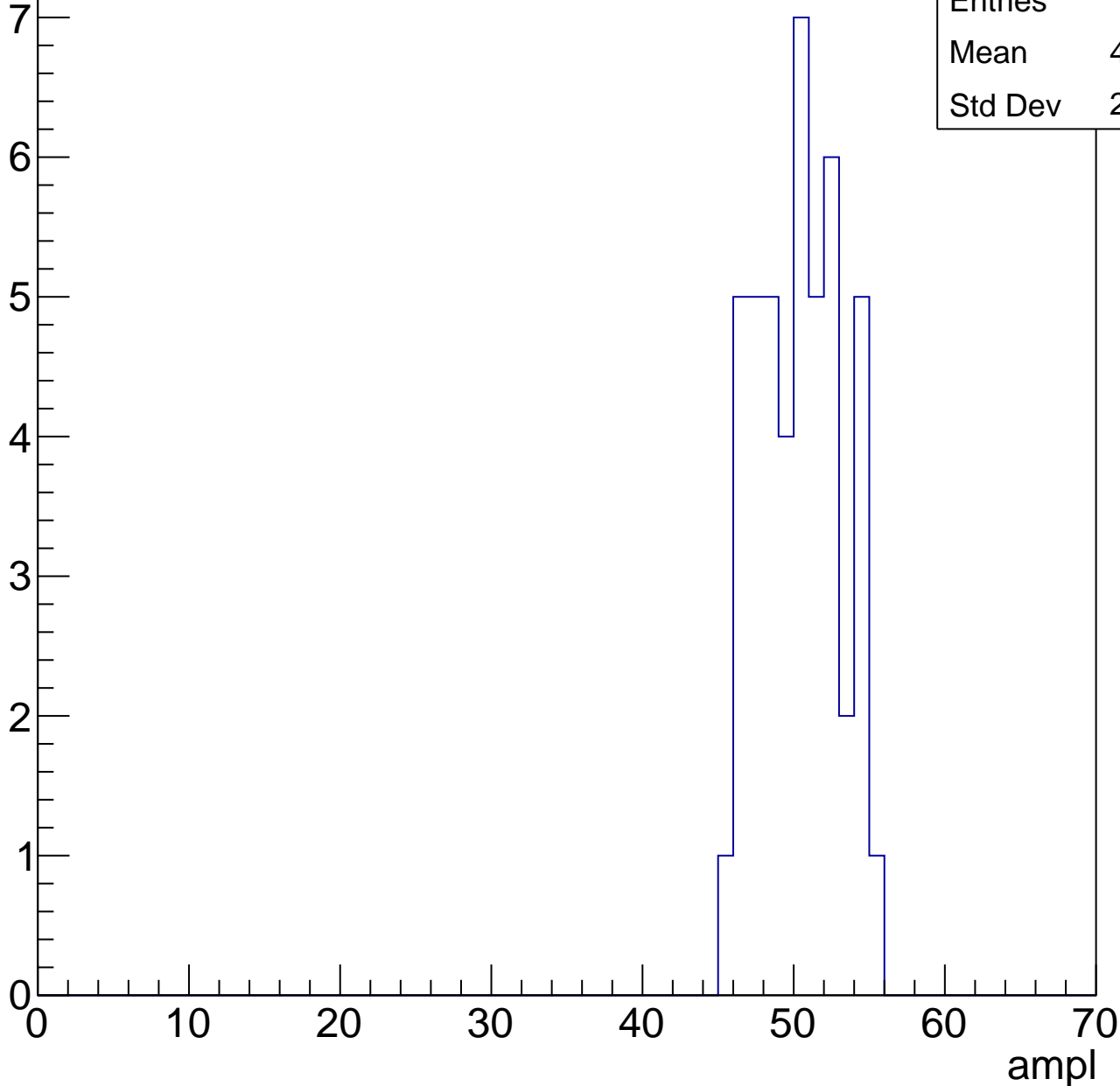


# B1L003S, U3-ch25, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	46
Mean	49.87
Std Dev	2.659

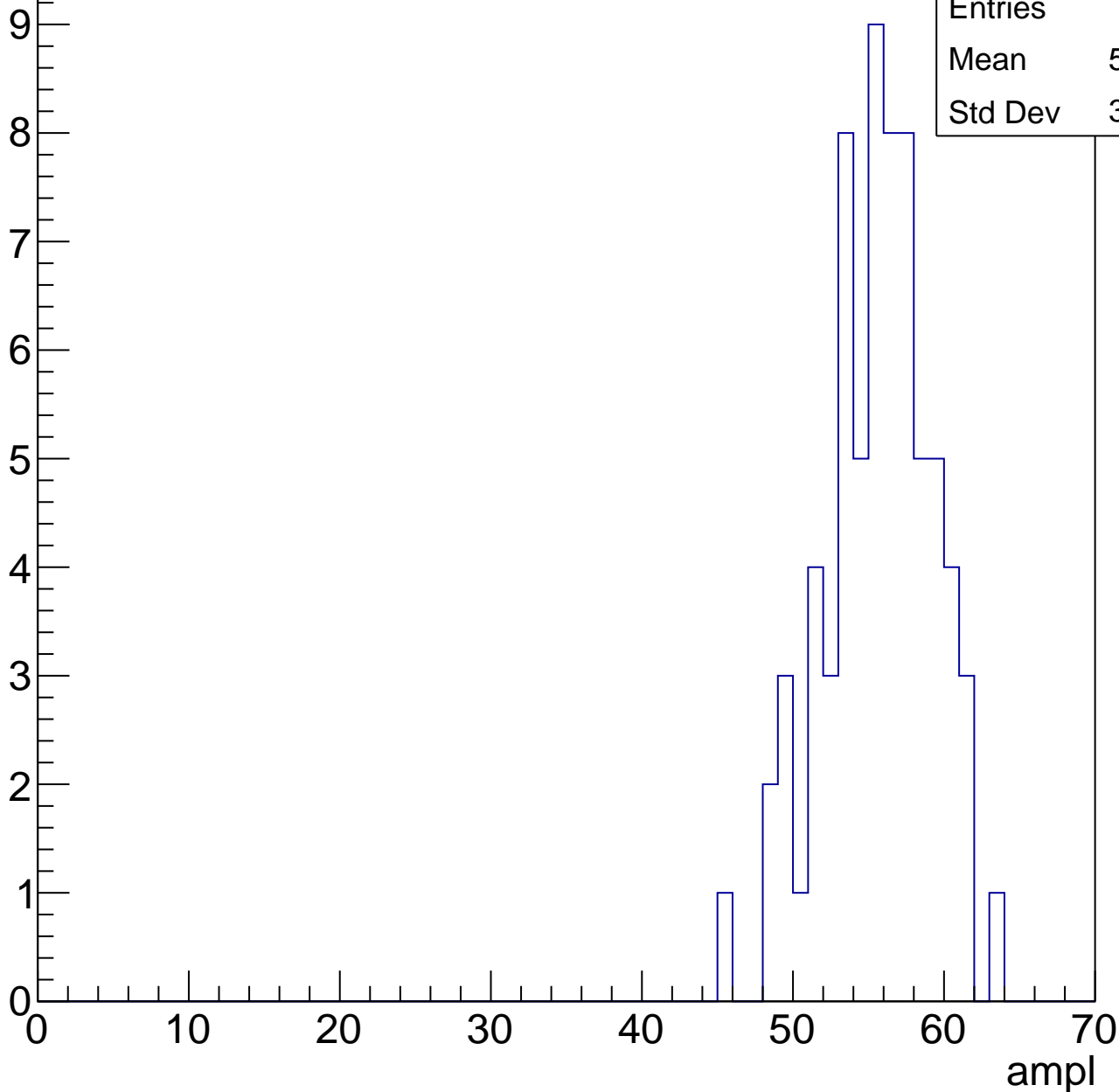


# B1L003S, U3-ch25, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	55.17
Std Dev	3.574

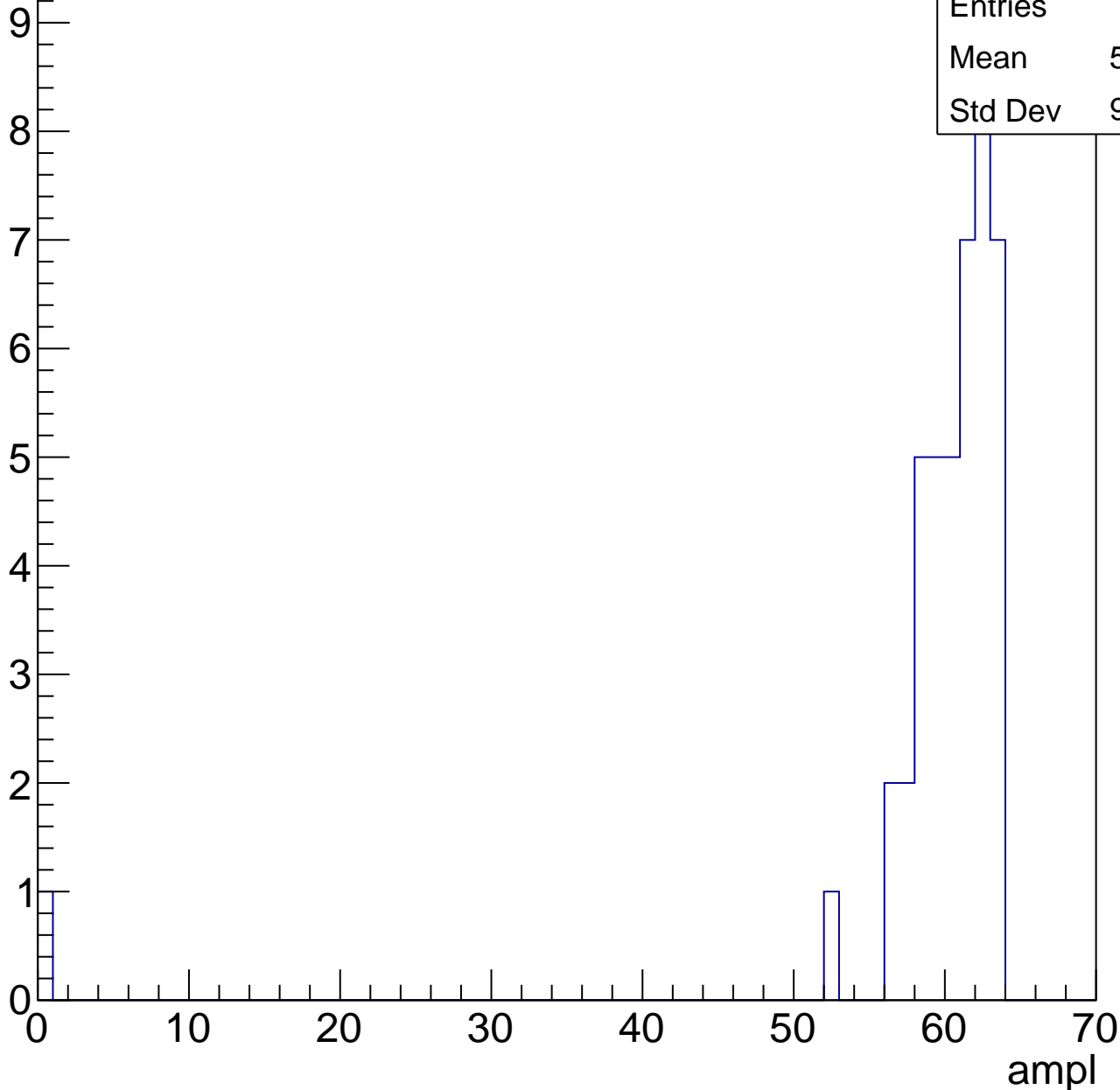


# B1L003S, U3-ch25, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	44
Mean	58.84
Std Dev	9.276



# B1L003S, U3-ch25, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch25, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U3-ch26, adc0

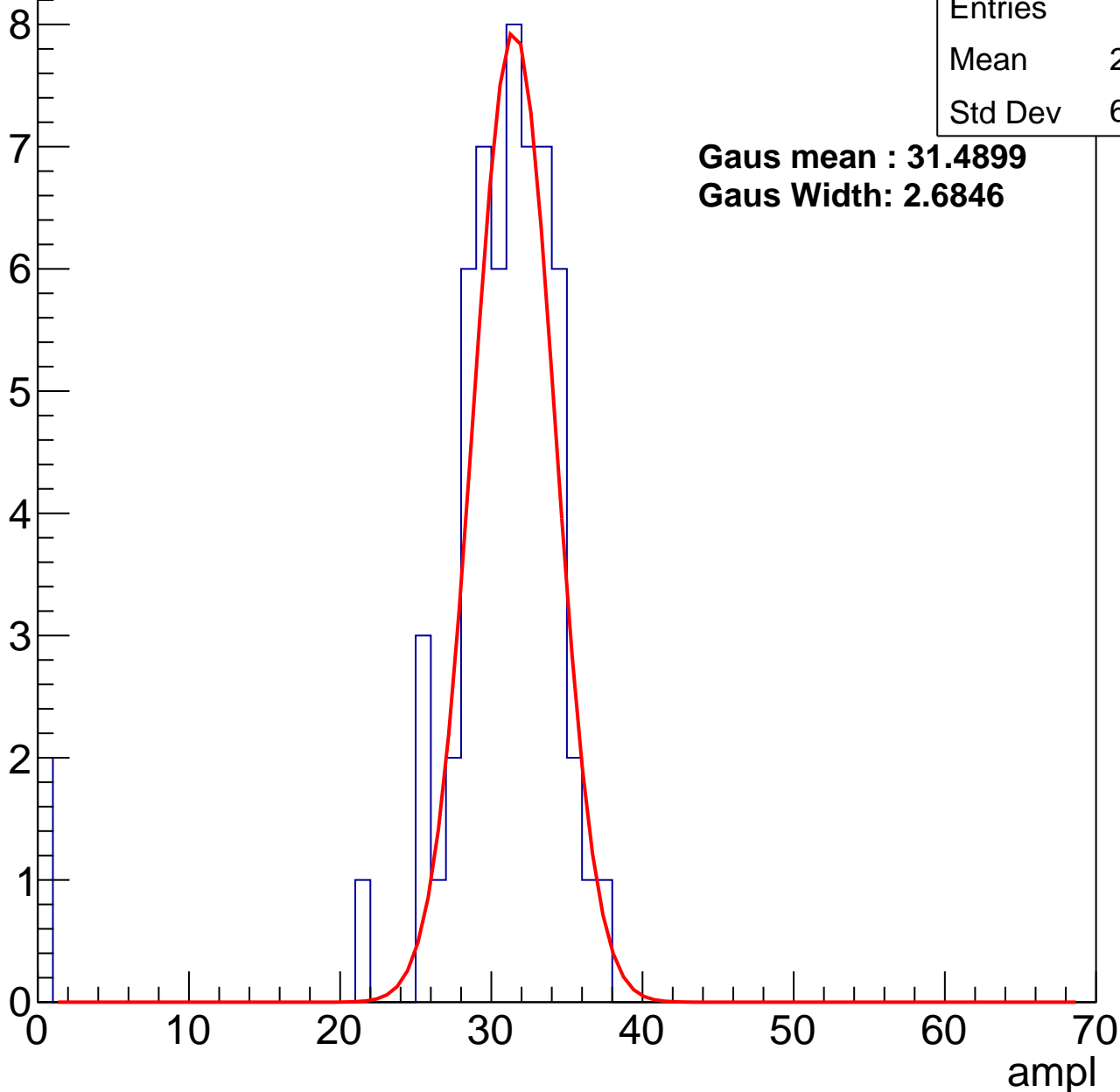
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	29.62
Std Dev	6.248

**Gaus mean : 31.4899**

**Gaus Width: 2.6846**



# B1L003S, U3-ch26, adc1

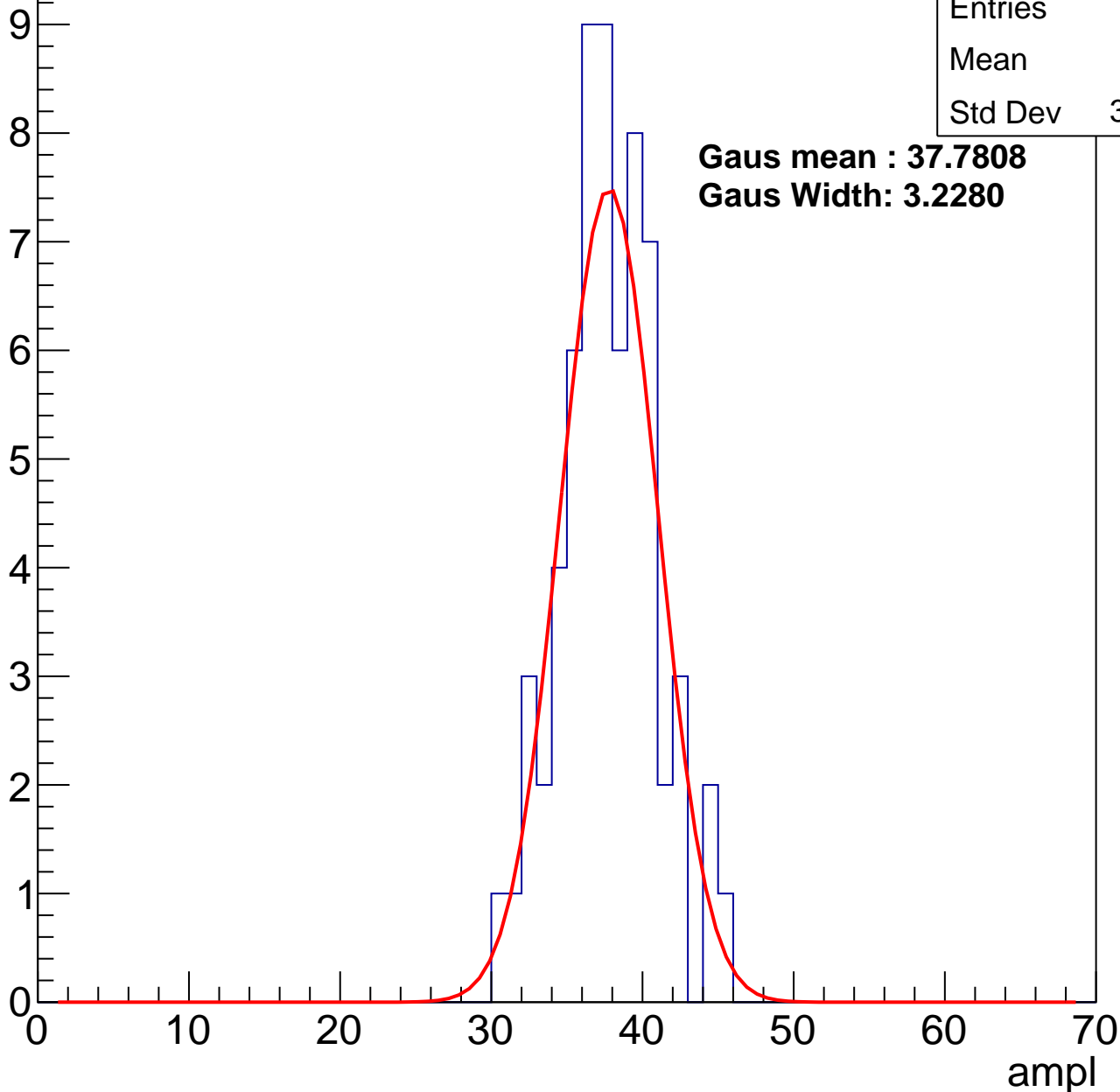
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	37.3
Std Dev	3.126

**Gaus mean : 37.7808**

**Gaus Width: 3.2280**



# B1L003S, U3-ch26, adc2

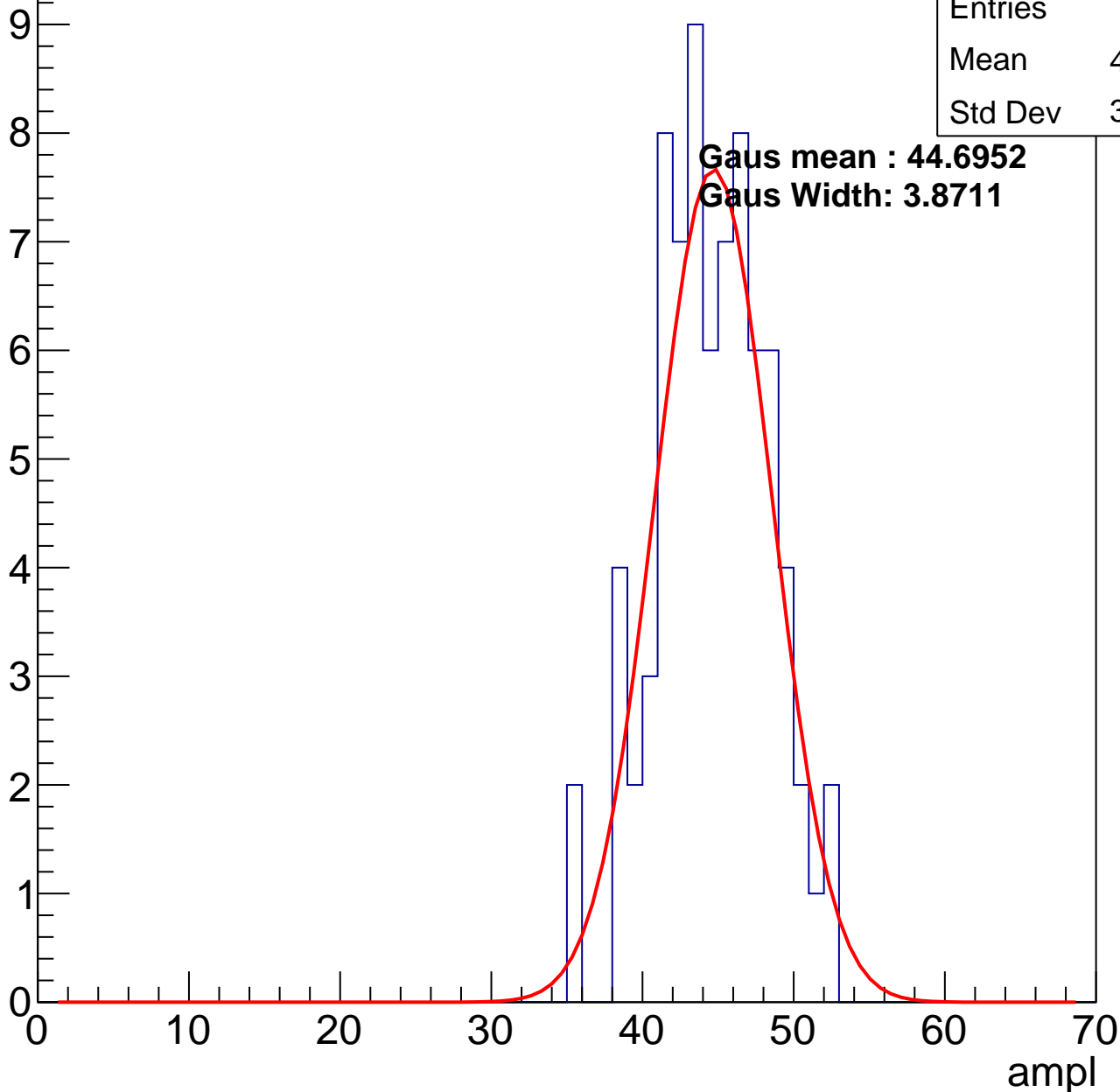
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	77
Mean	44.12
Std Dev	3.693

**Gaus mean : 44.6952**

**Gaus Width: 3.8711**

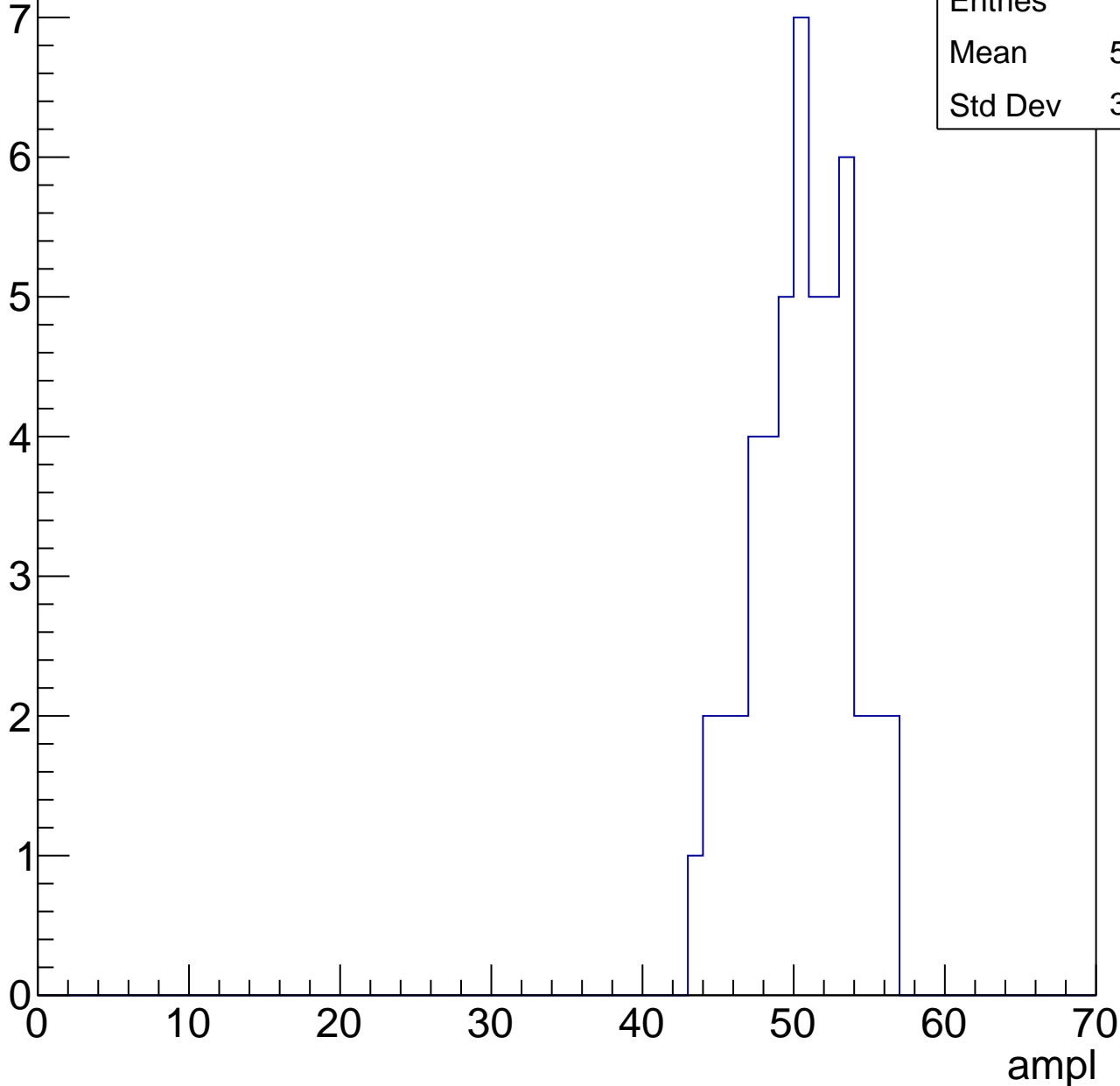


# B1L003S, U3-ch26, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

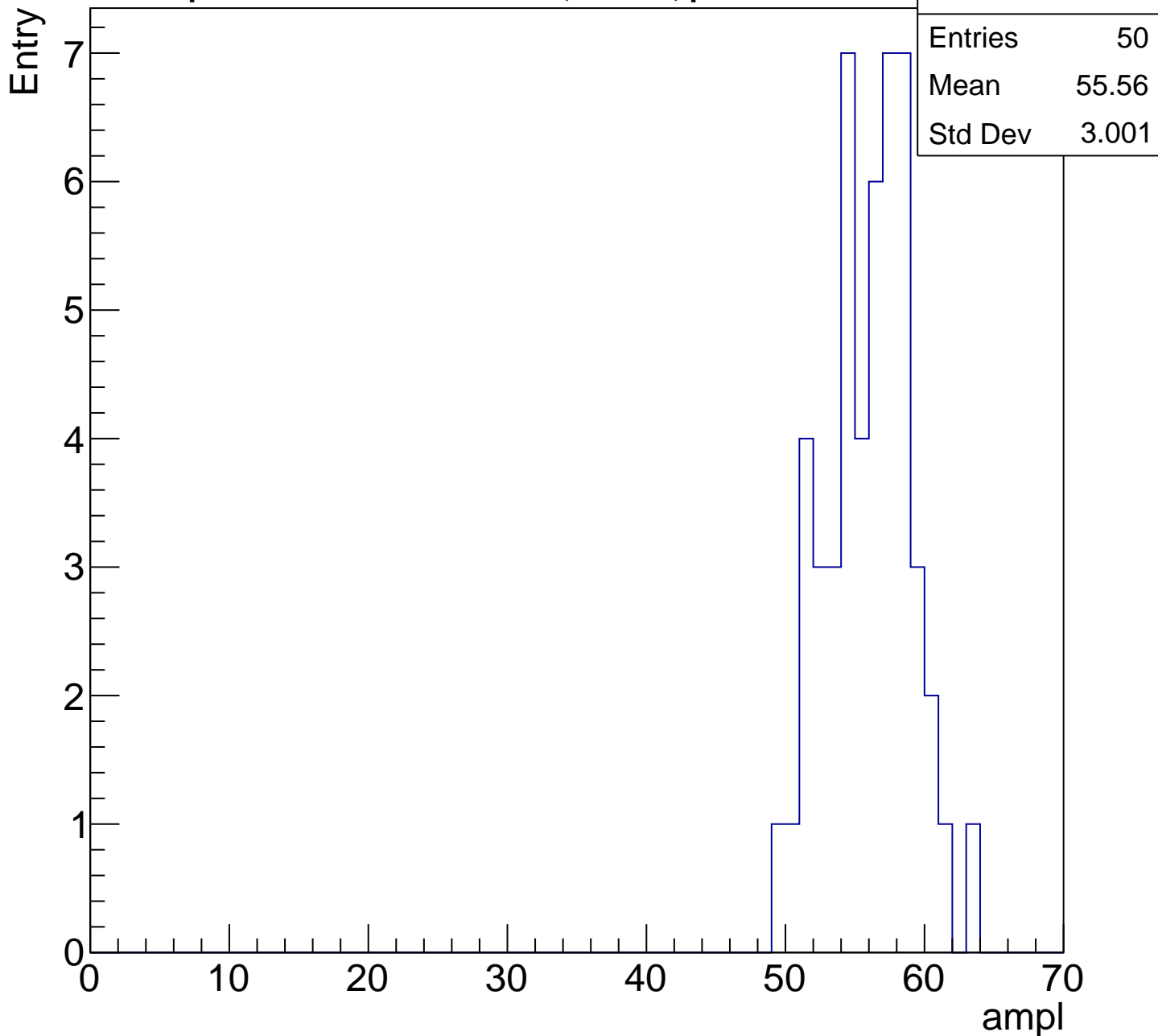
Entry

Entries	49
Mean	50.02
Std Dev	3.172



# B1L003S, U3-ch26, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

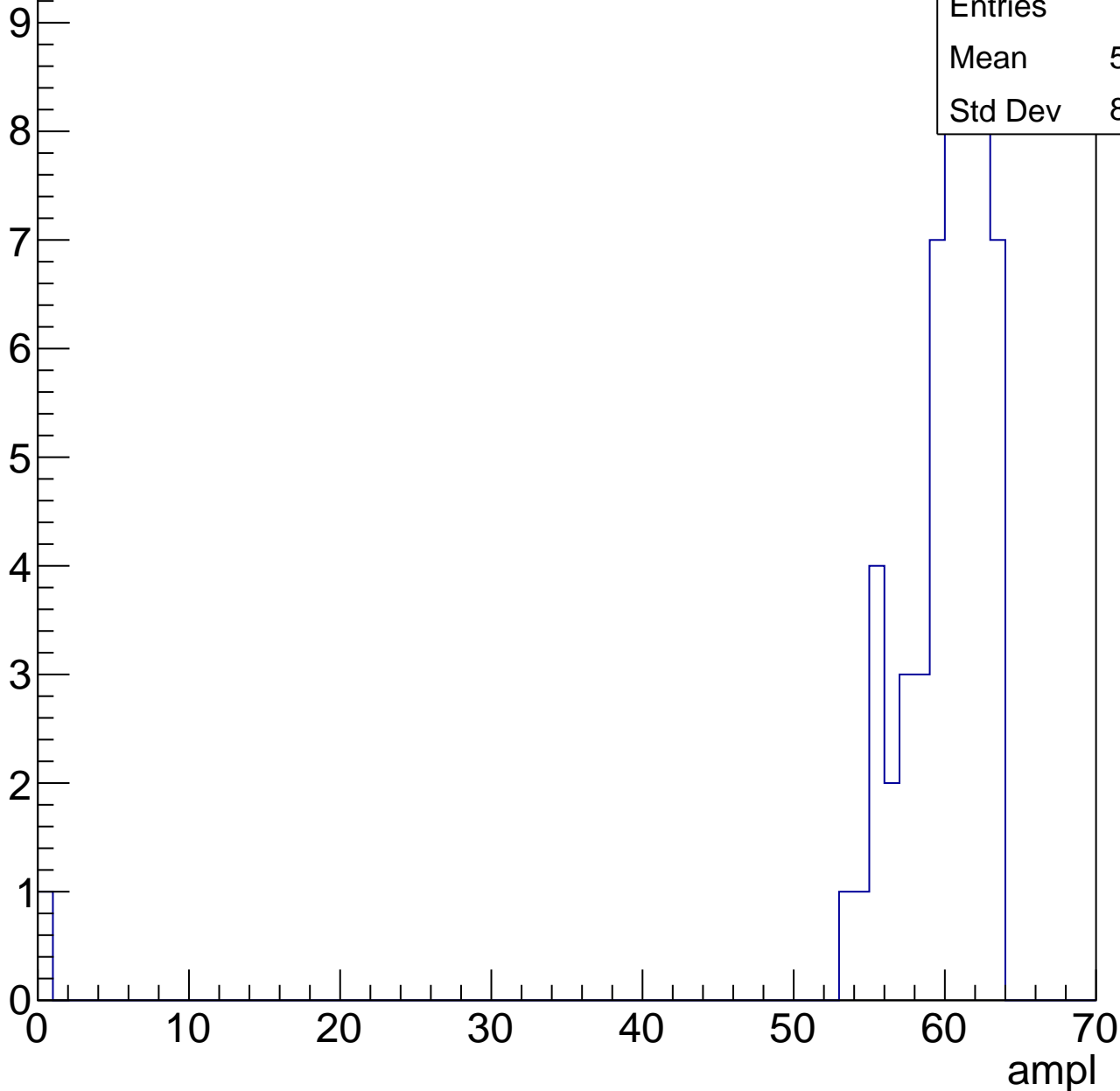


# B1L003S, U3-ch26, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	58.64
Std Dev	8.387



# B1L003S, U3-ch26, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch26, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	4
Mean	0
Std Dev	0

# B1L003S, U3-ch27, adc0

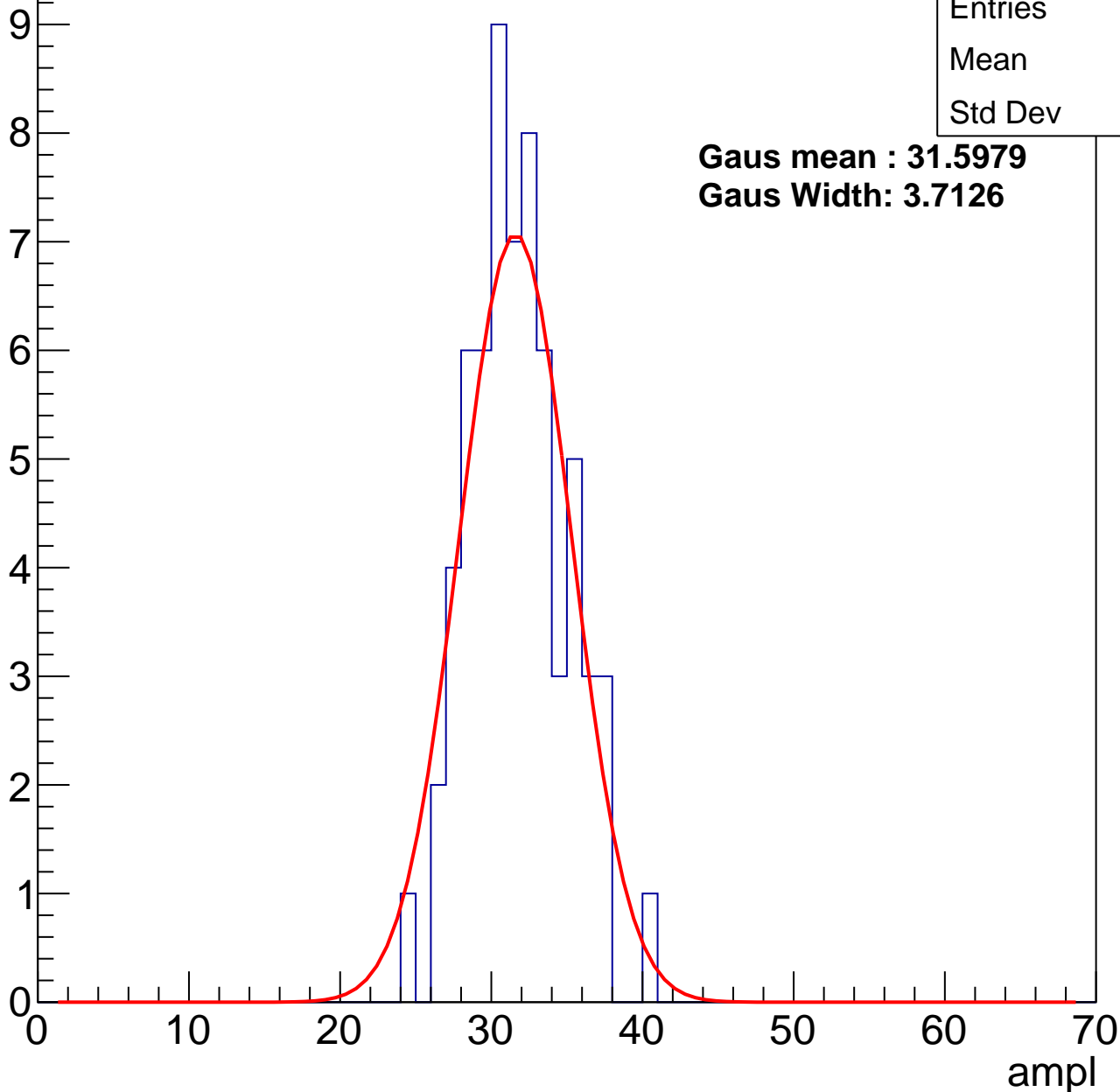
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	31.3
Std Dev	3.18

**Gaus mean : 31.5979**

**Gaus Width: 3.7126**



# B1L003S, U3-ch27, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	72
Mean	37.42
Std Dev	3.624

**Gaus mean : 38.1248**

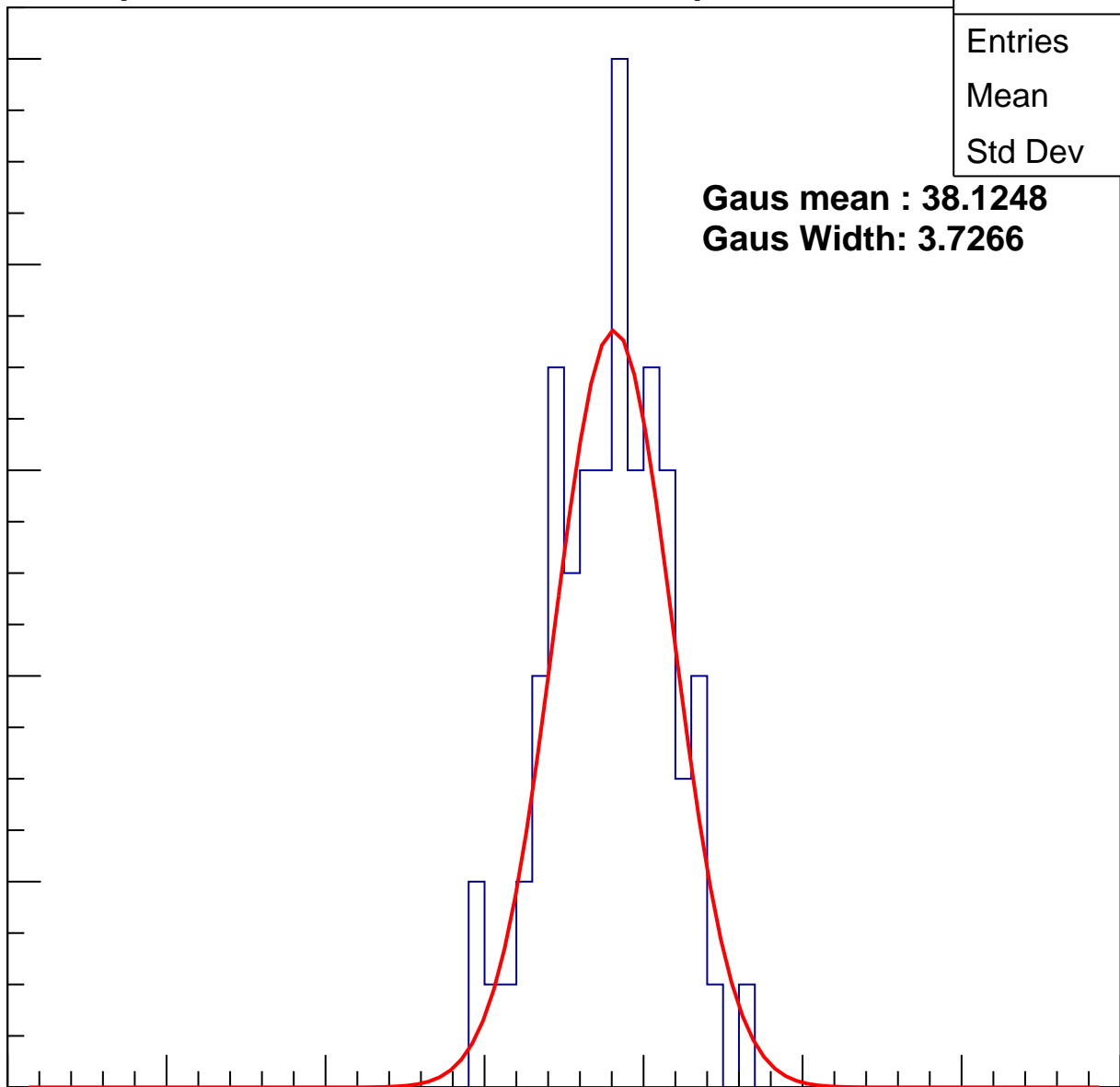
**Gaus Width: 3.7266**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



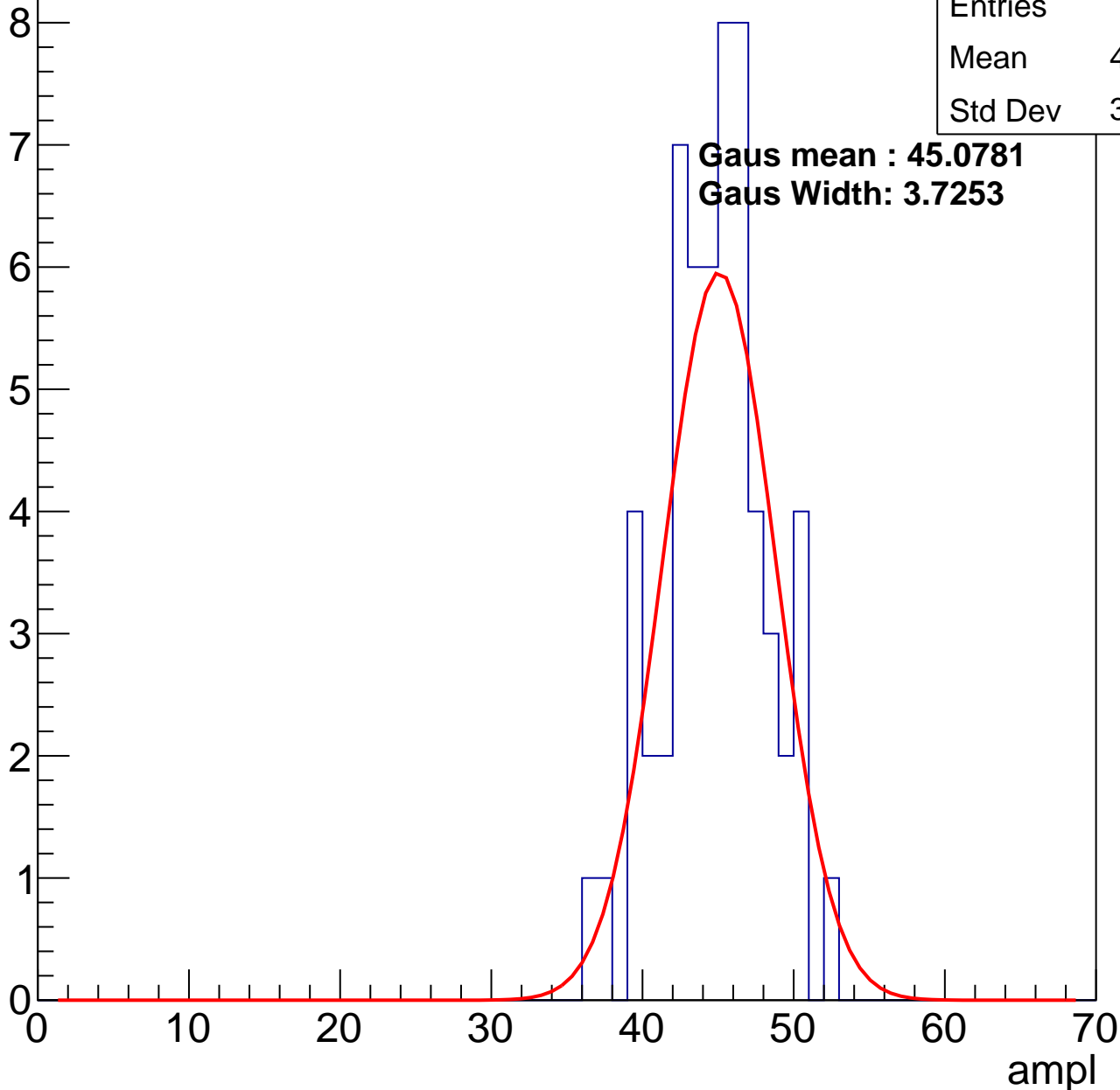
# B1L003S, U3-ch27, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	44.36
Std Dev	3.374

**Gaus mean : 45.0781**  
**Gaus Width: 3.7253**

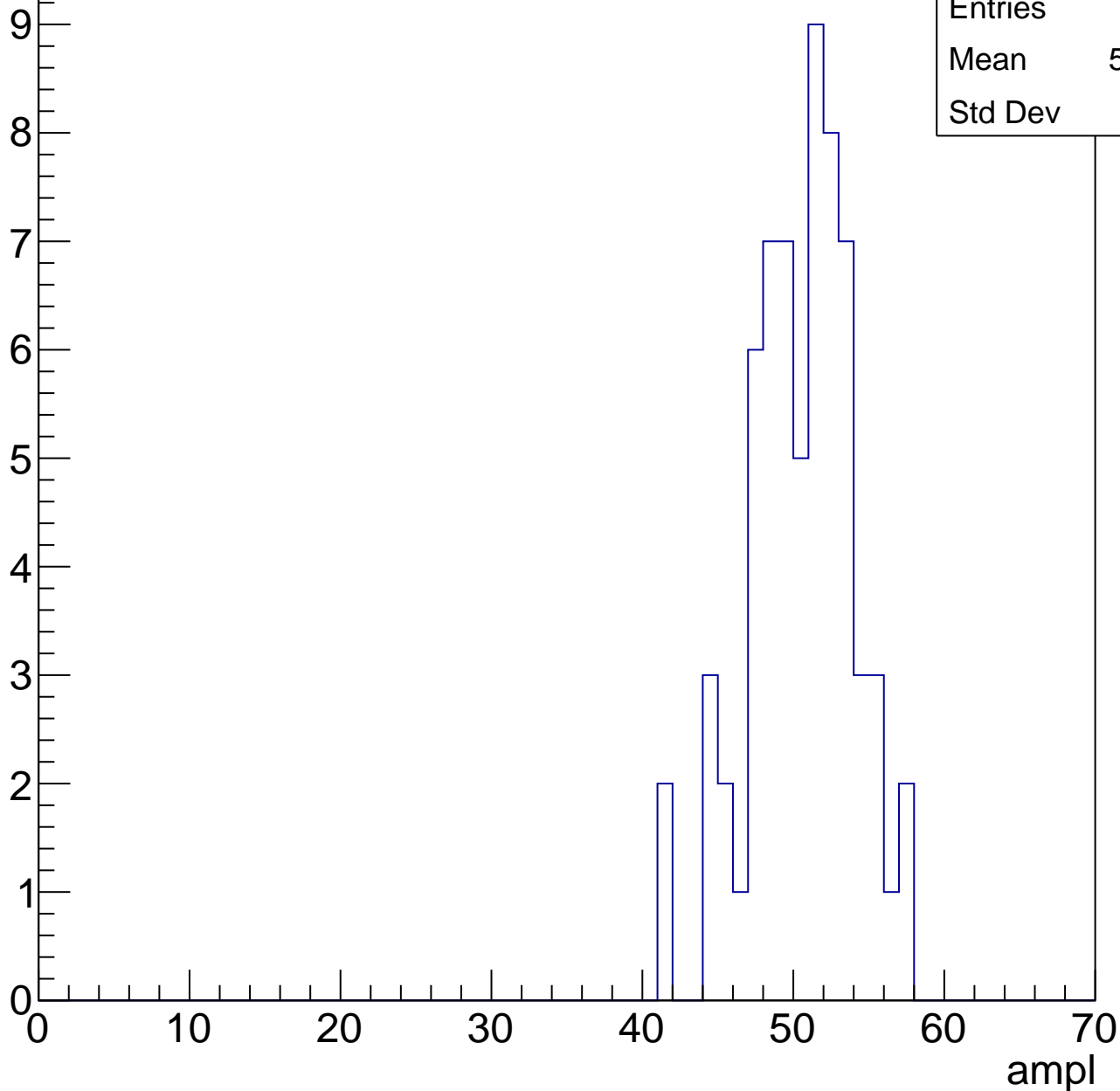


# B1L003S, U3-ch27, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

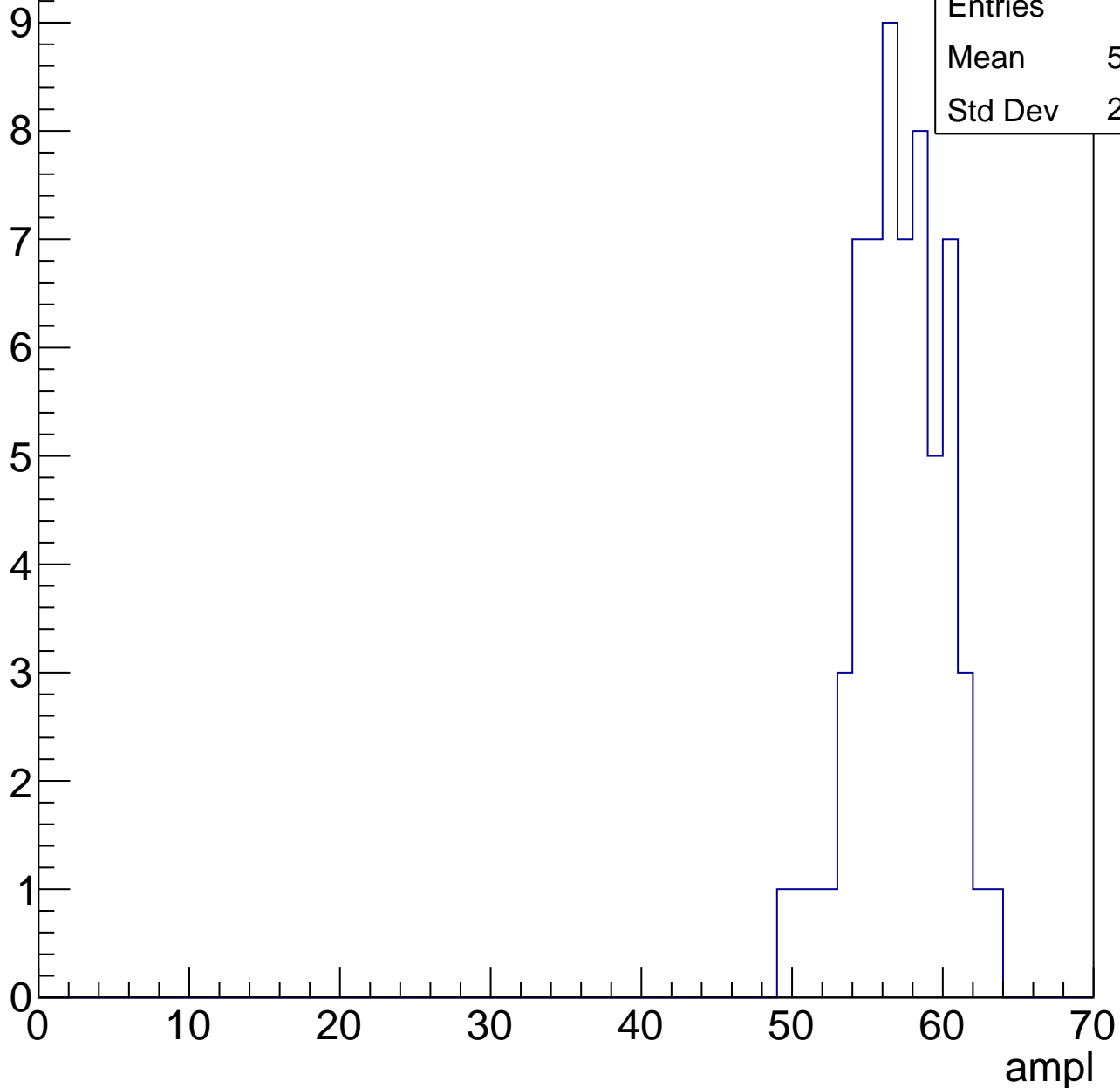
Entries	66
Mean	50.06
Std Dev	3.45



# B1L003S, U3-ch27, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

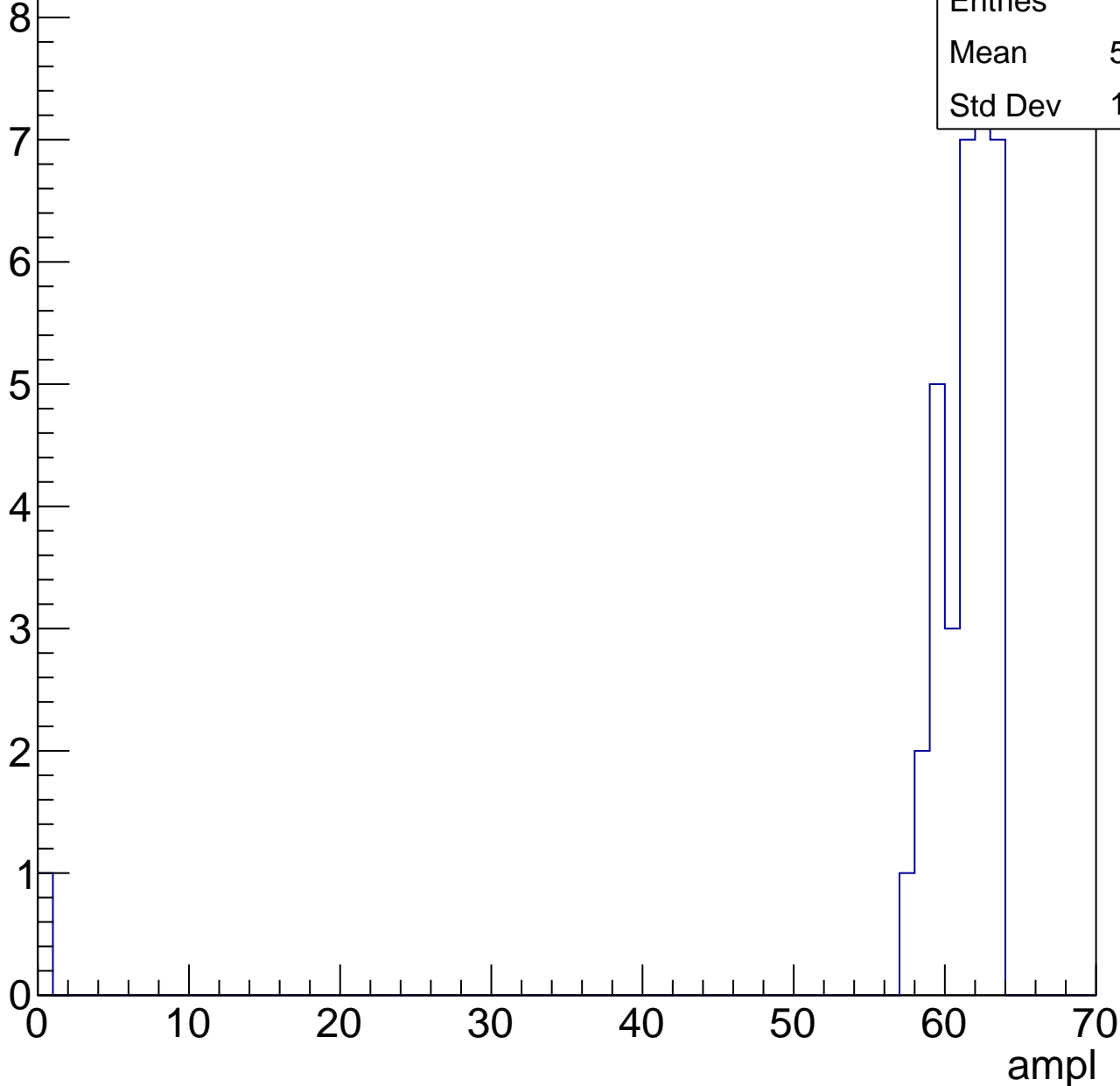


# B1L003S, U3-ch27, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

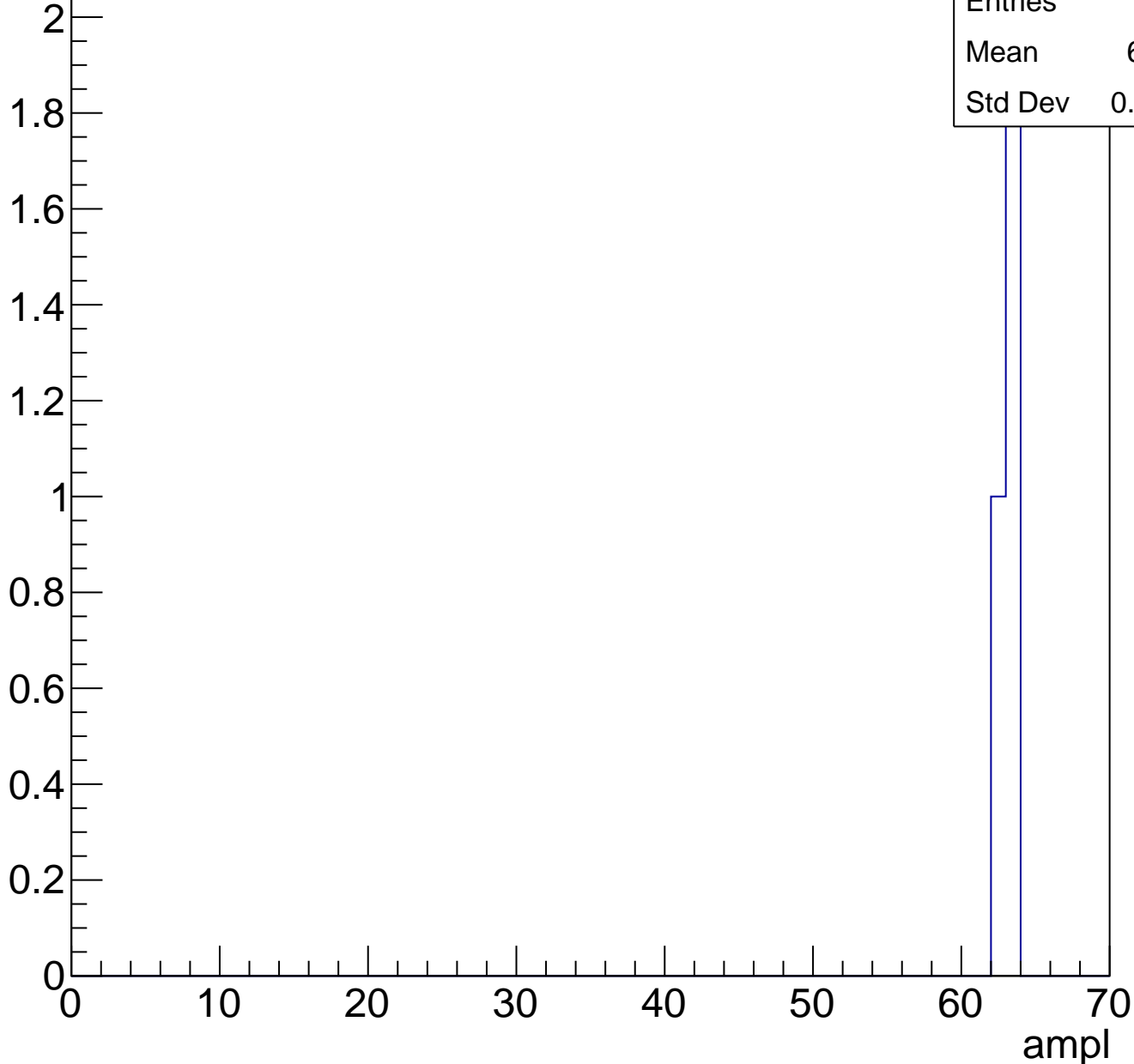
Entries	34
Mean	59.18
Std Dev	10.43



# B1L003S, U3-ch27, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

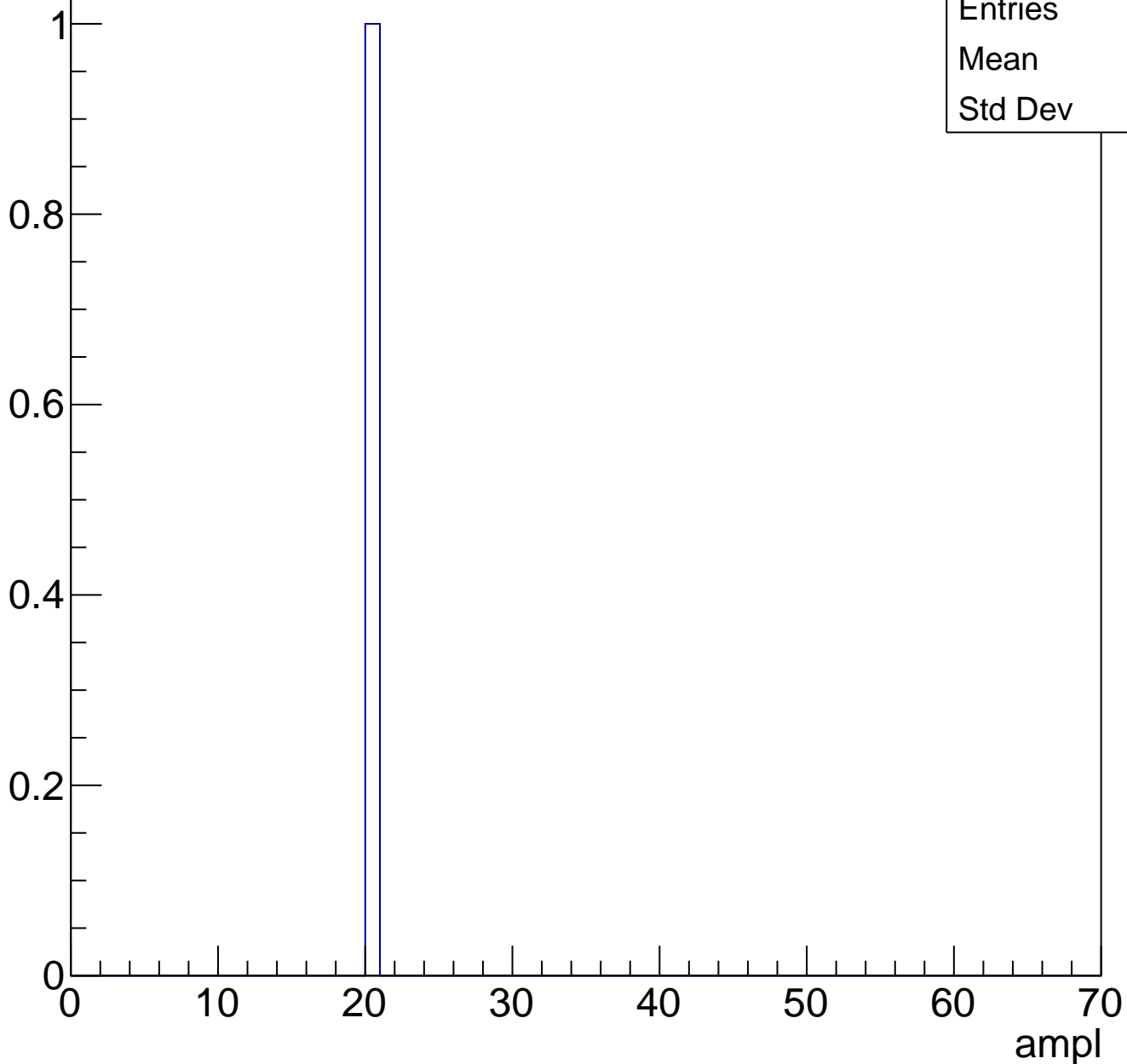




# B1L003S, U3-ch27, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	20
Std Dev	0

# B1L003S, U3-ch28, adc0

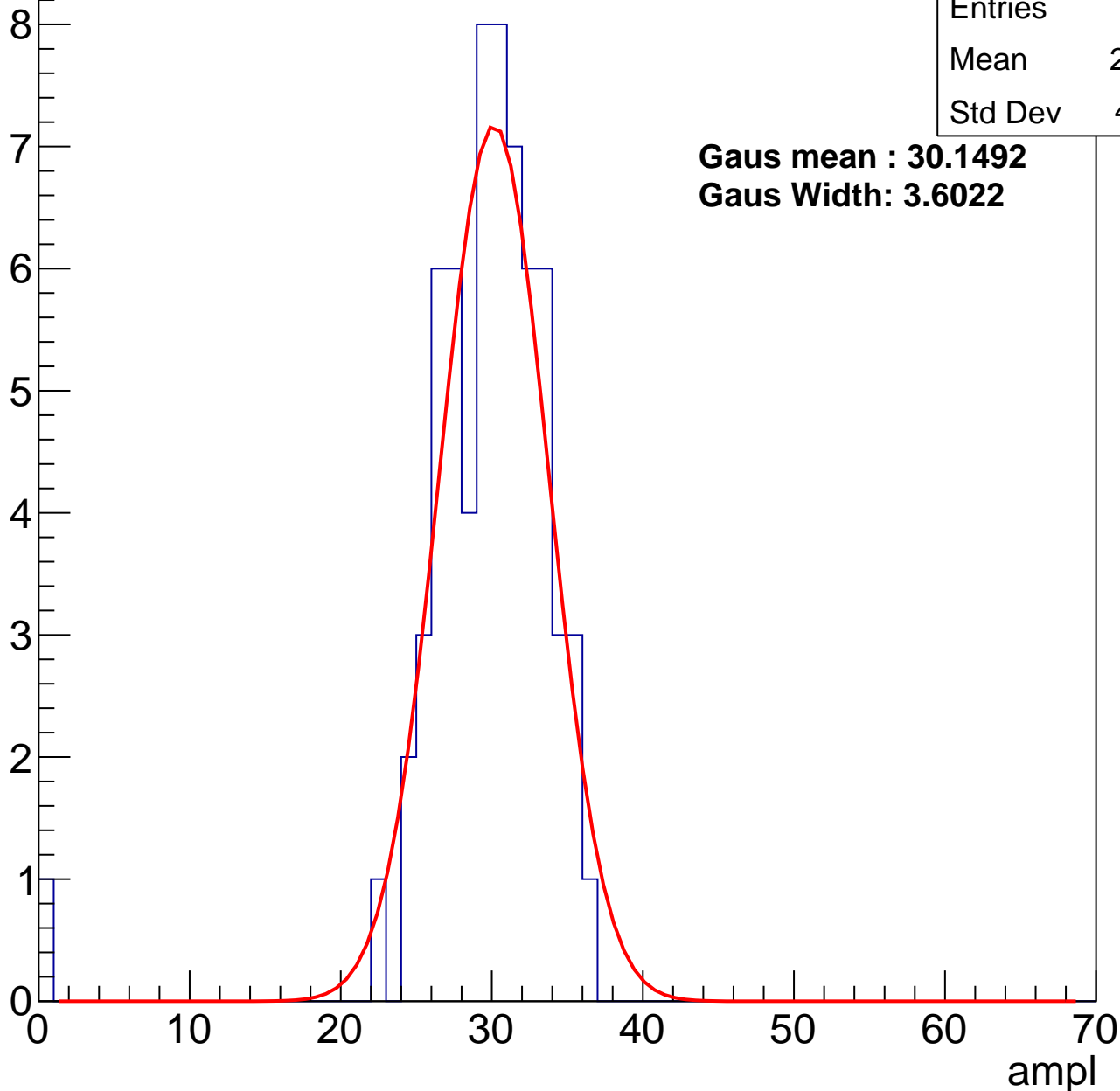
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	29.18
Std Dev	4.781

**Gaus mean : 30.1492**

**Gaus Width: 3.6022**

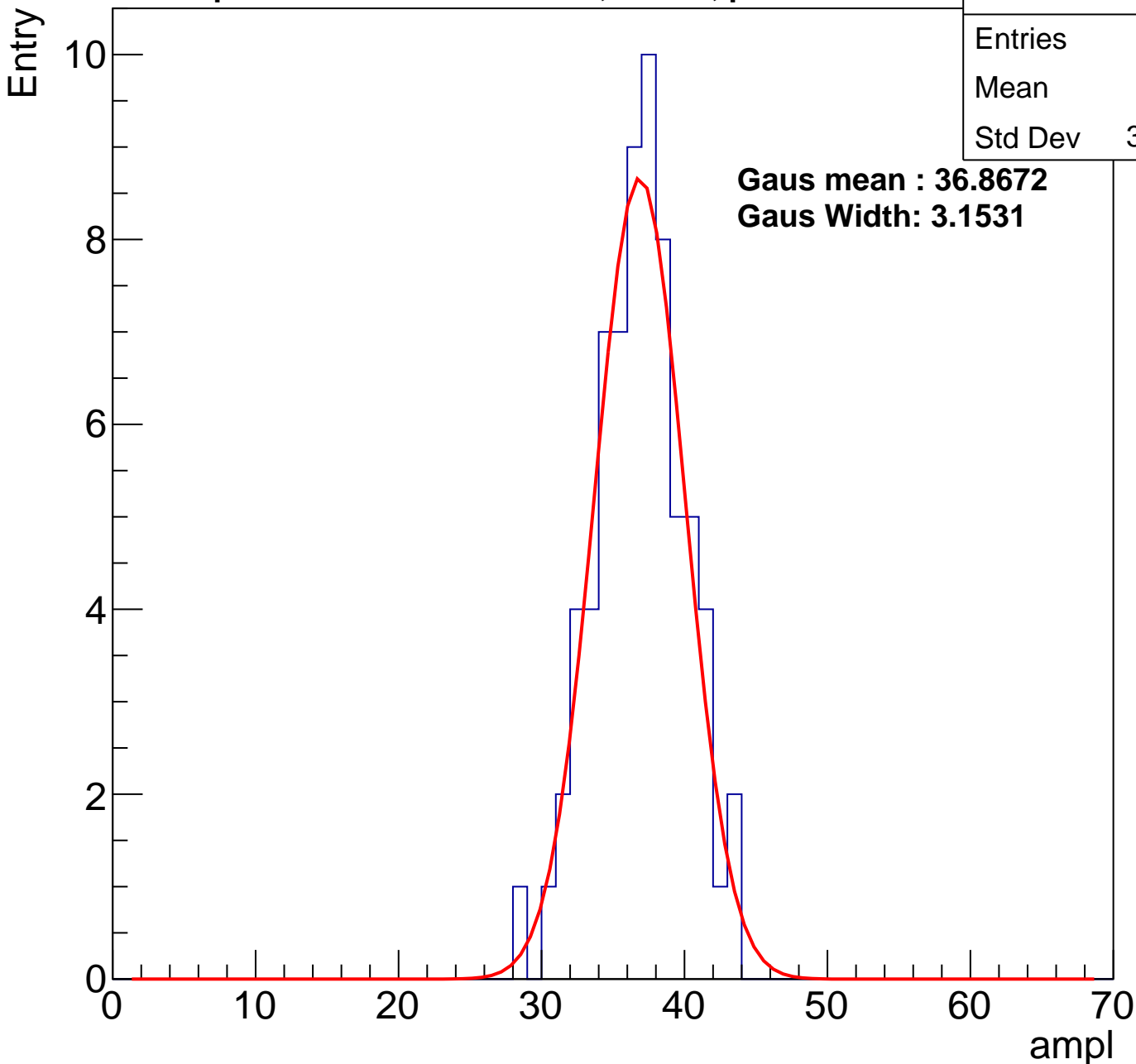


# B1L003S, U3-ch28, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	70
Mean	36.4
Std Dev	3.105

**Gaus mean : 36.8672**  
**Gaus Width: 3.1531**



# B1L003S, U3-ch28, adc2

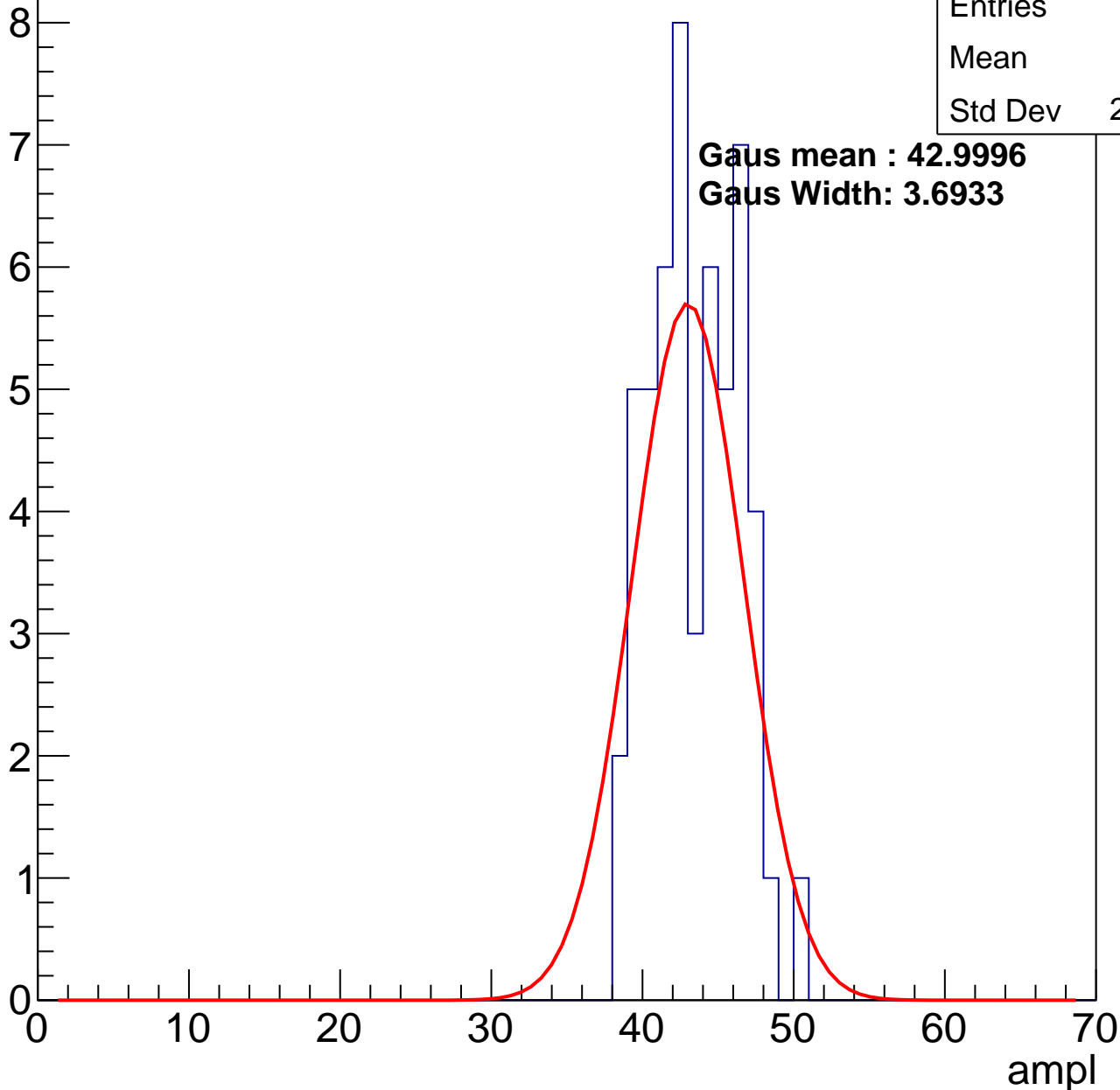
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	43
Std Dev	2.862

**Gaus mean : 42.9996**

**Gaus Width: 3.6933**

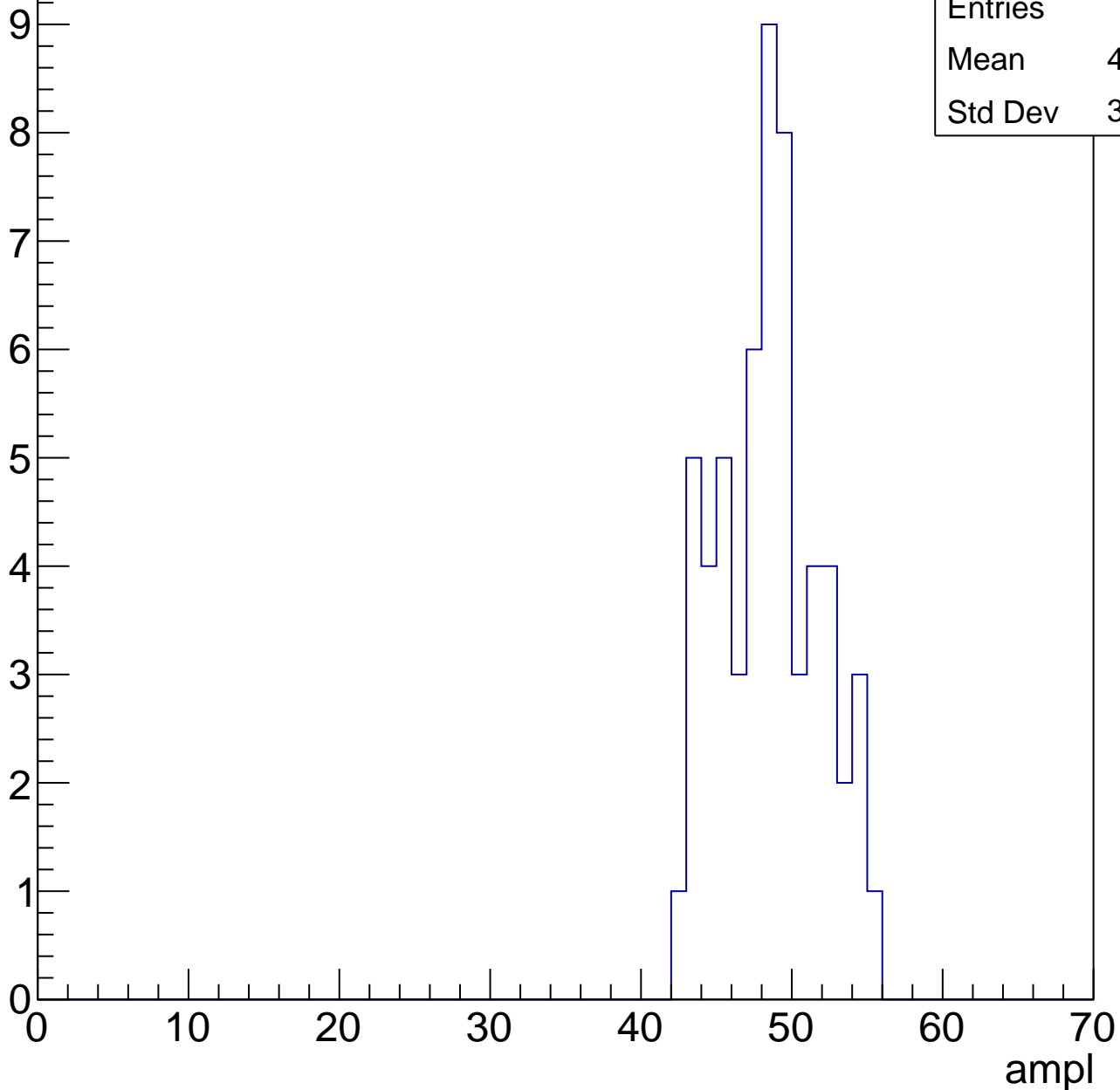


# B1L003S, U3-ch28, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

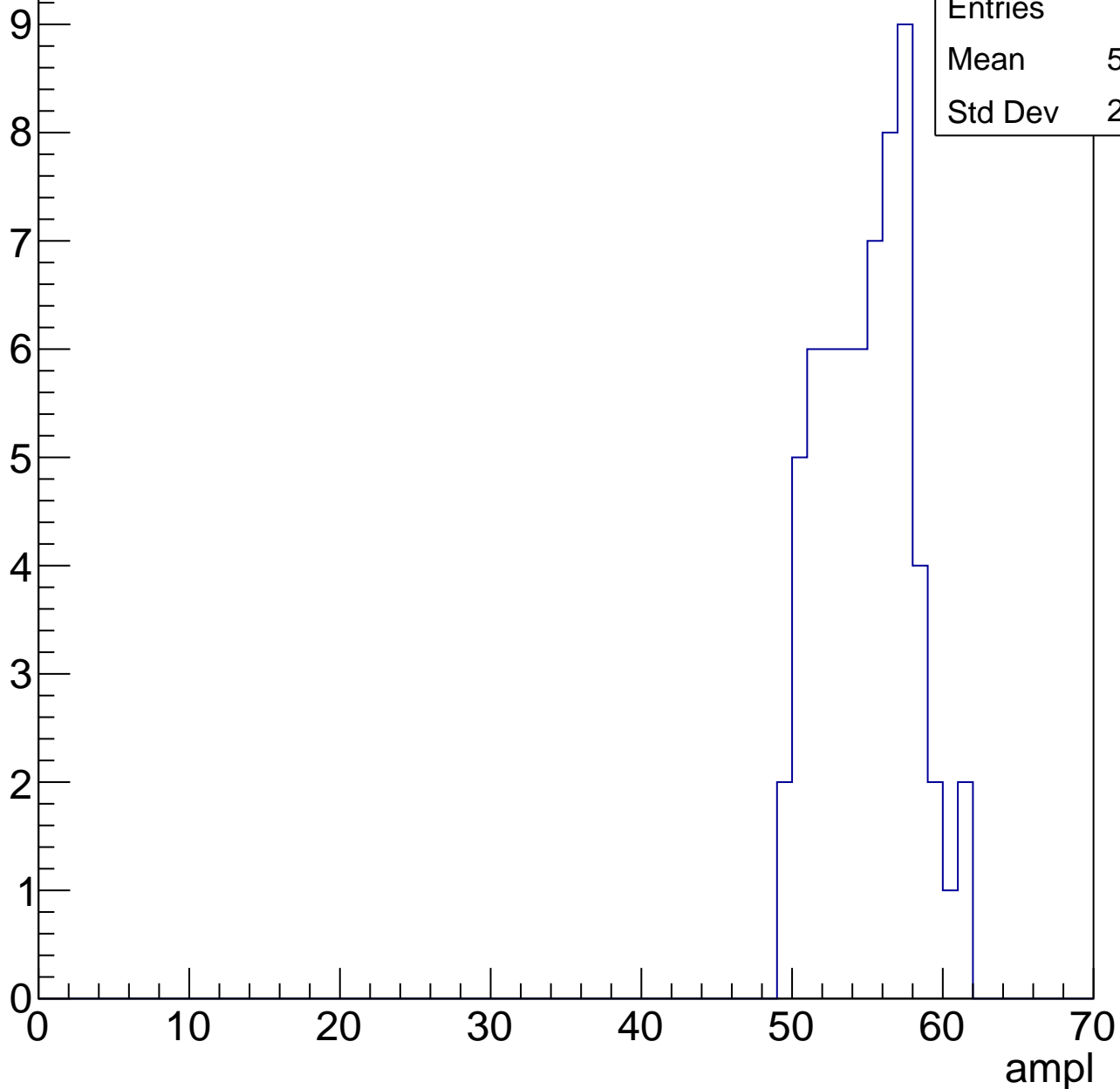
Entries	58
Mean	48.05
Std Dev	3.256



# B1L003S, U3-ch28, adc4

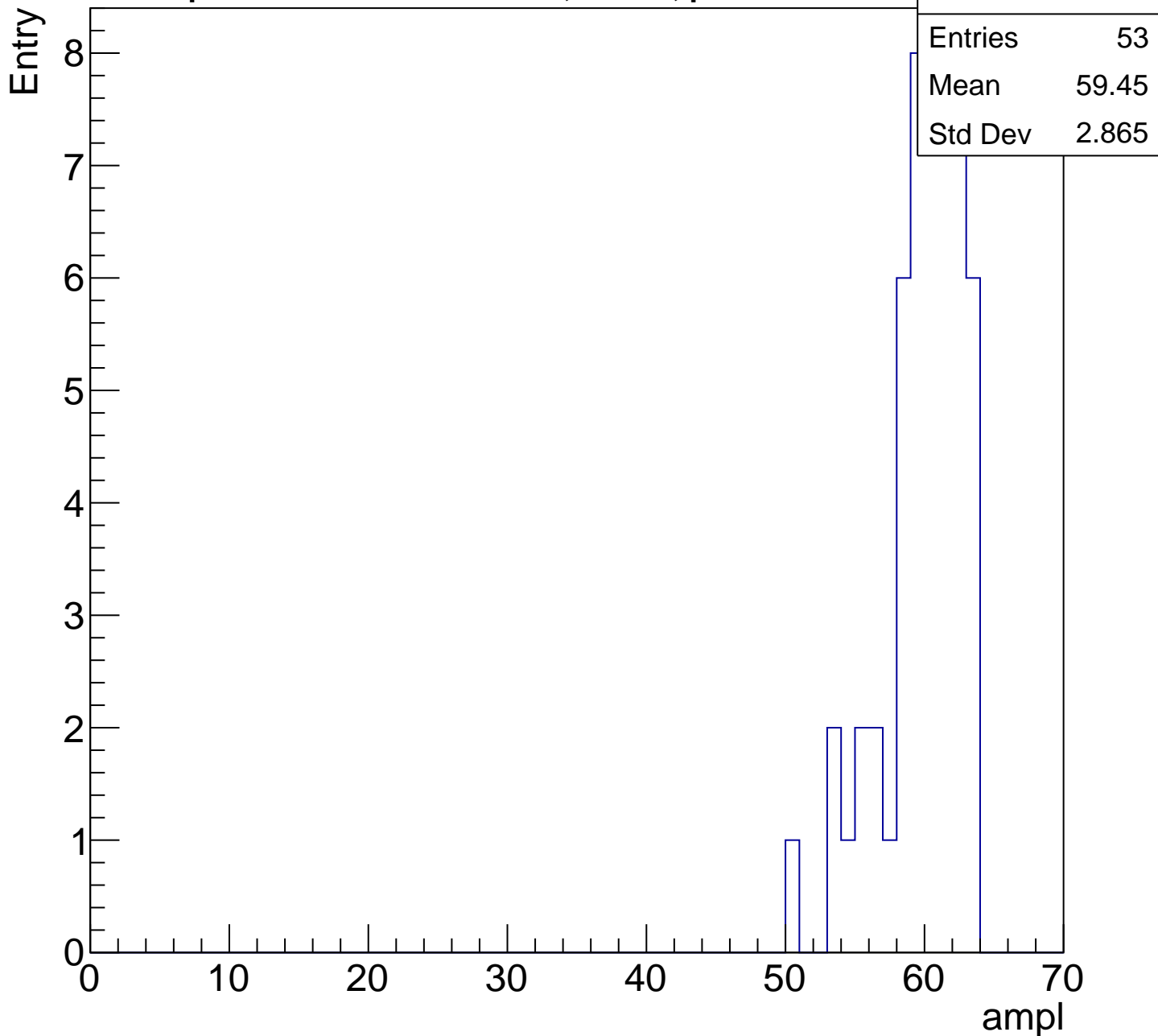
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U3-ch28, adc5

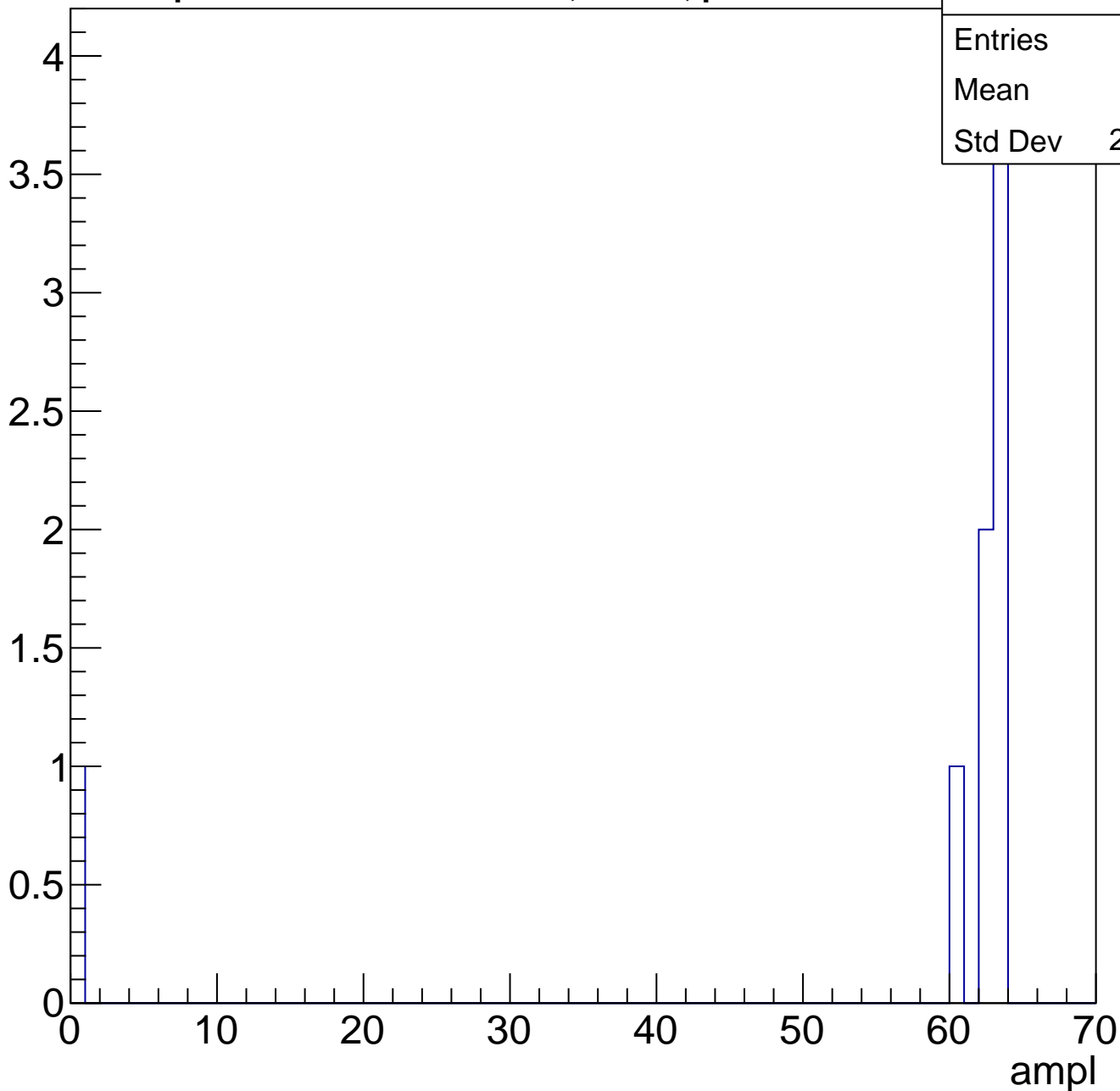
calib\_packv5\_042523\_0143.root, FC#13, port D2



# B1L003S, U3-ch28, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch28, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U3-ch29, adc0

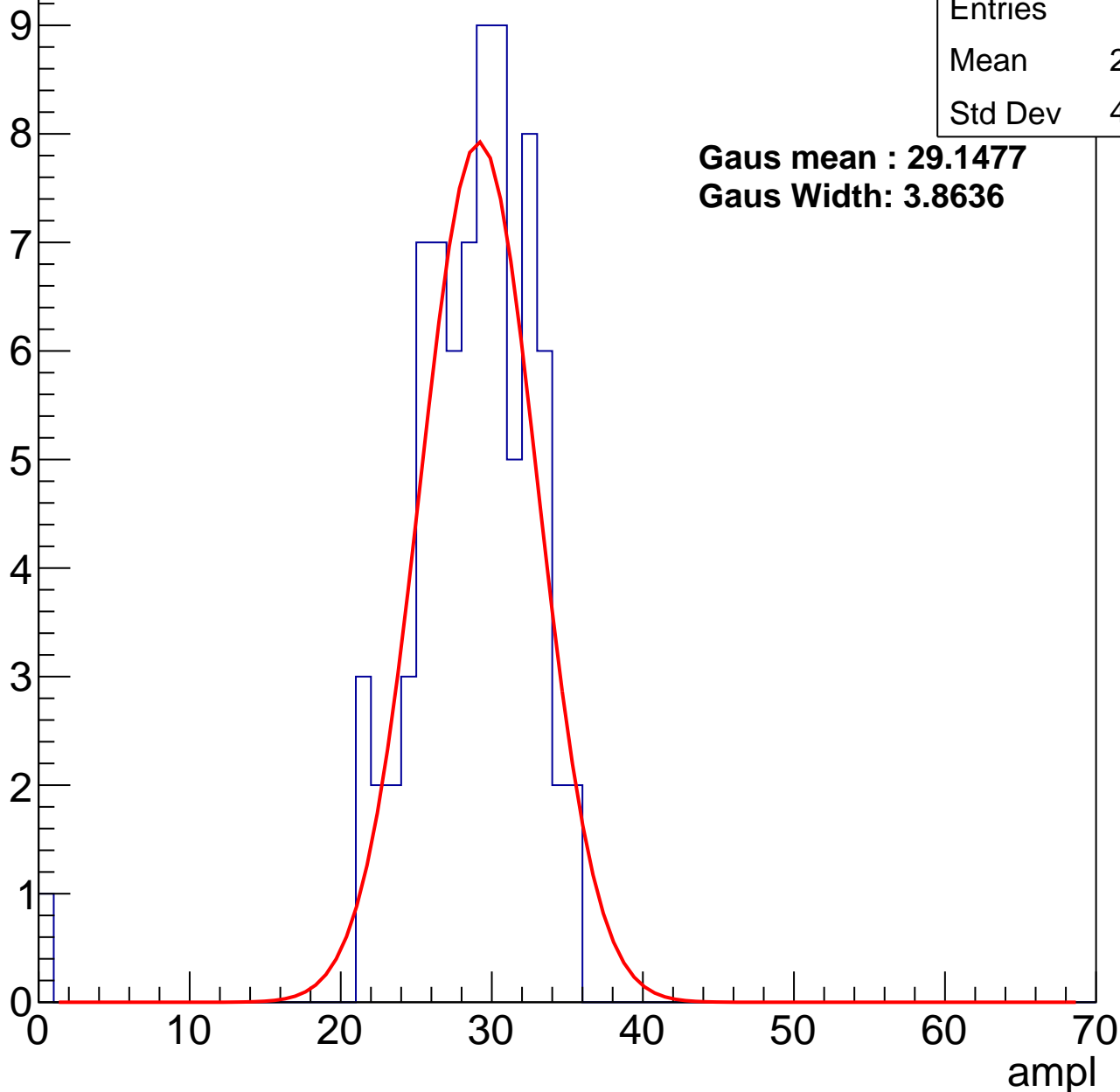
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	79
Mean	28.08
Std Dev	4.687

**Gaus mean : 29.1477**

**Gaus Width: 3.8636**



# B1L003S, U3-ch29, adc1

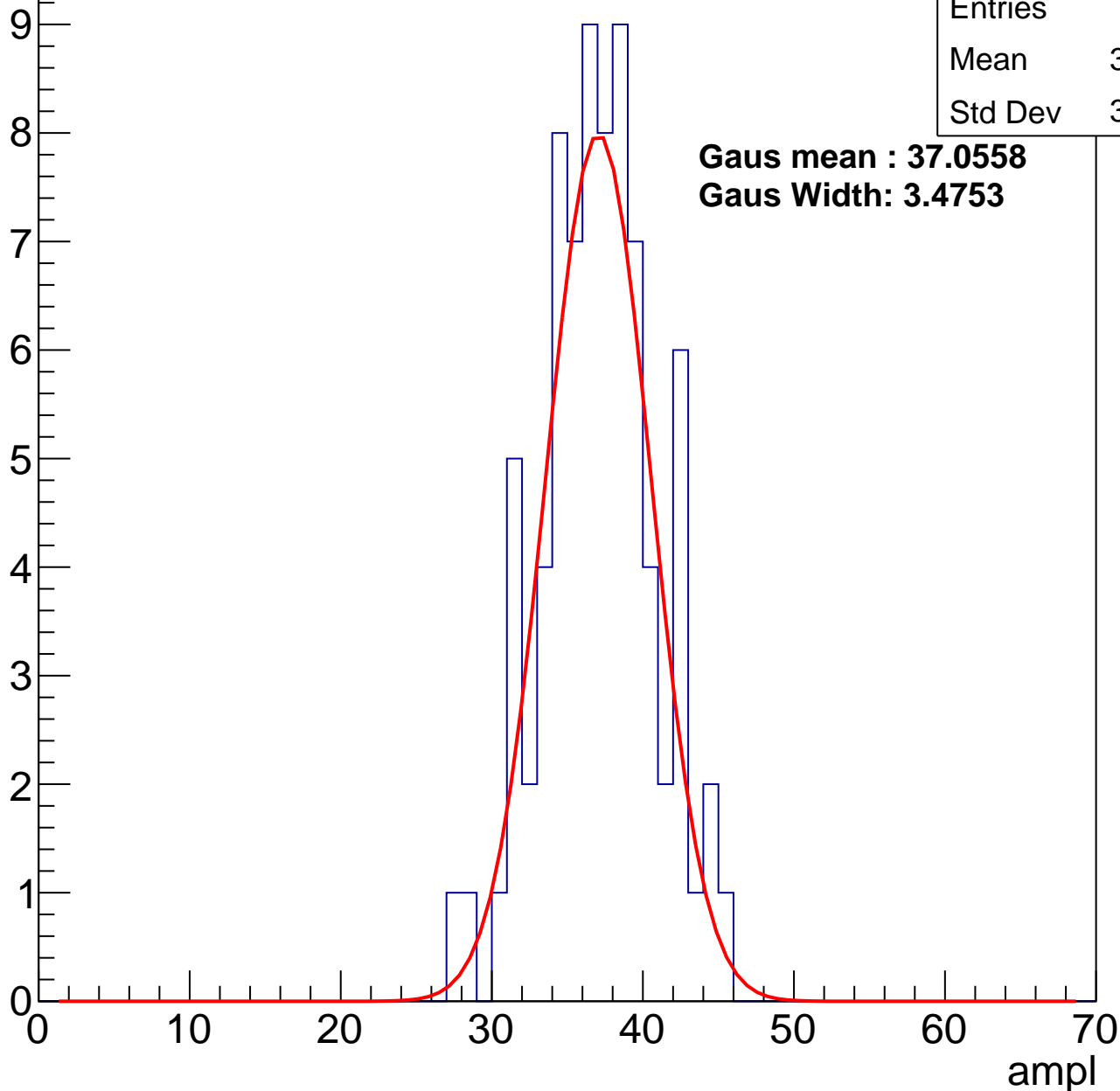
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	78
Mean	36.64
Std Dev	3.714

**Gaus mean : 37.0558**

**Gaus Width: 3.4753**



# B1L003S, U3-ch29, adc2

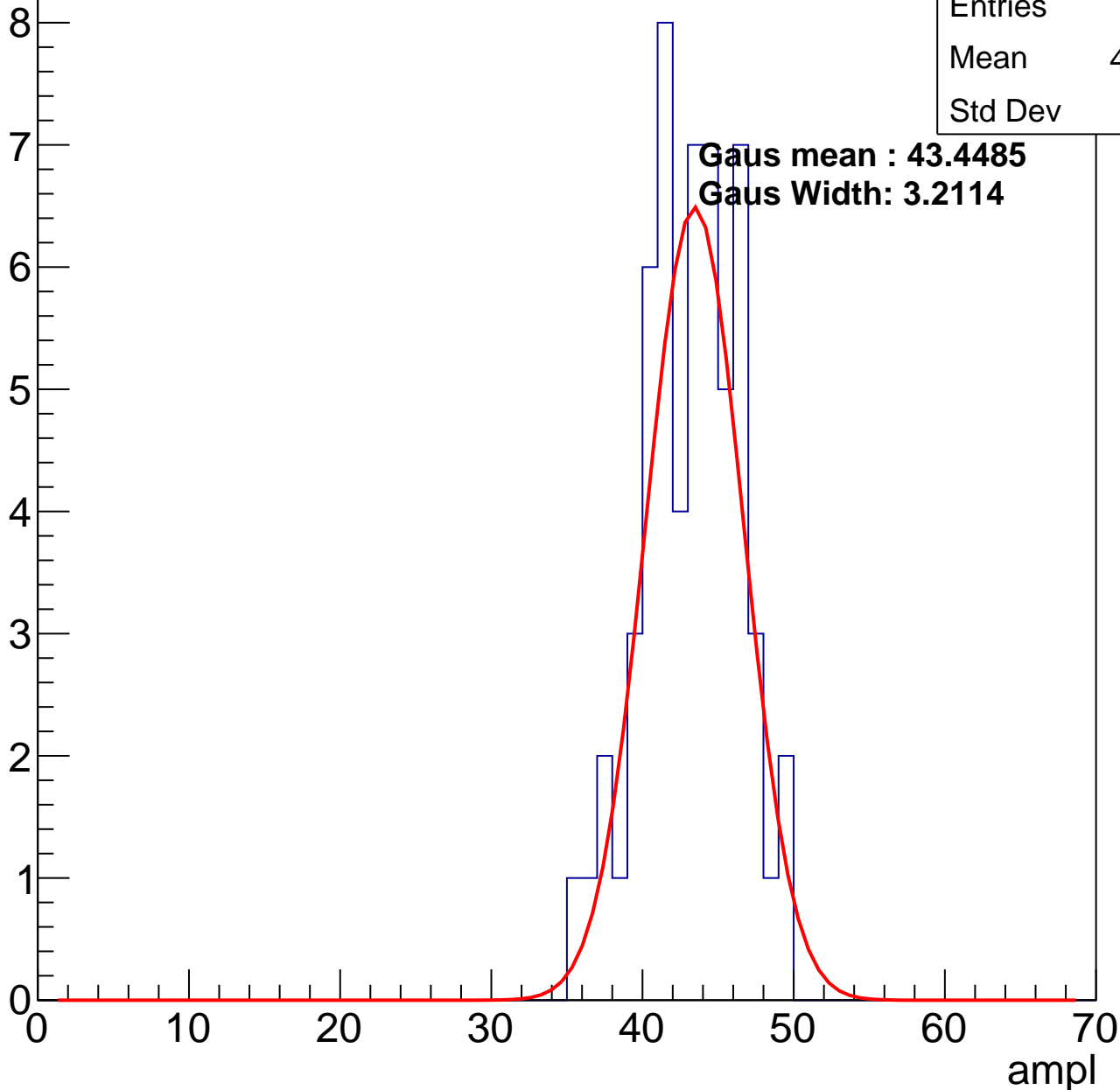
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	42.74
Std Dev	3.16

**Gaus mean : 43.4485**

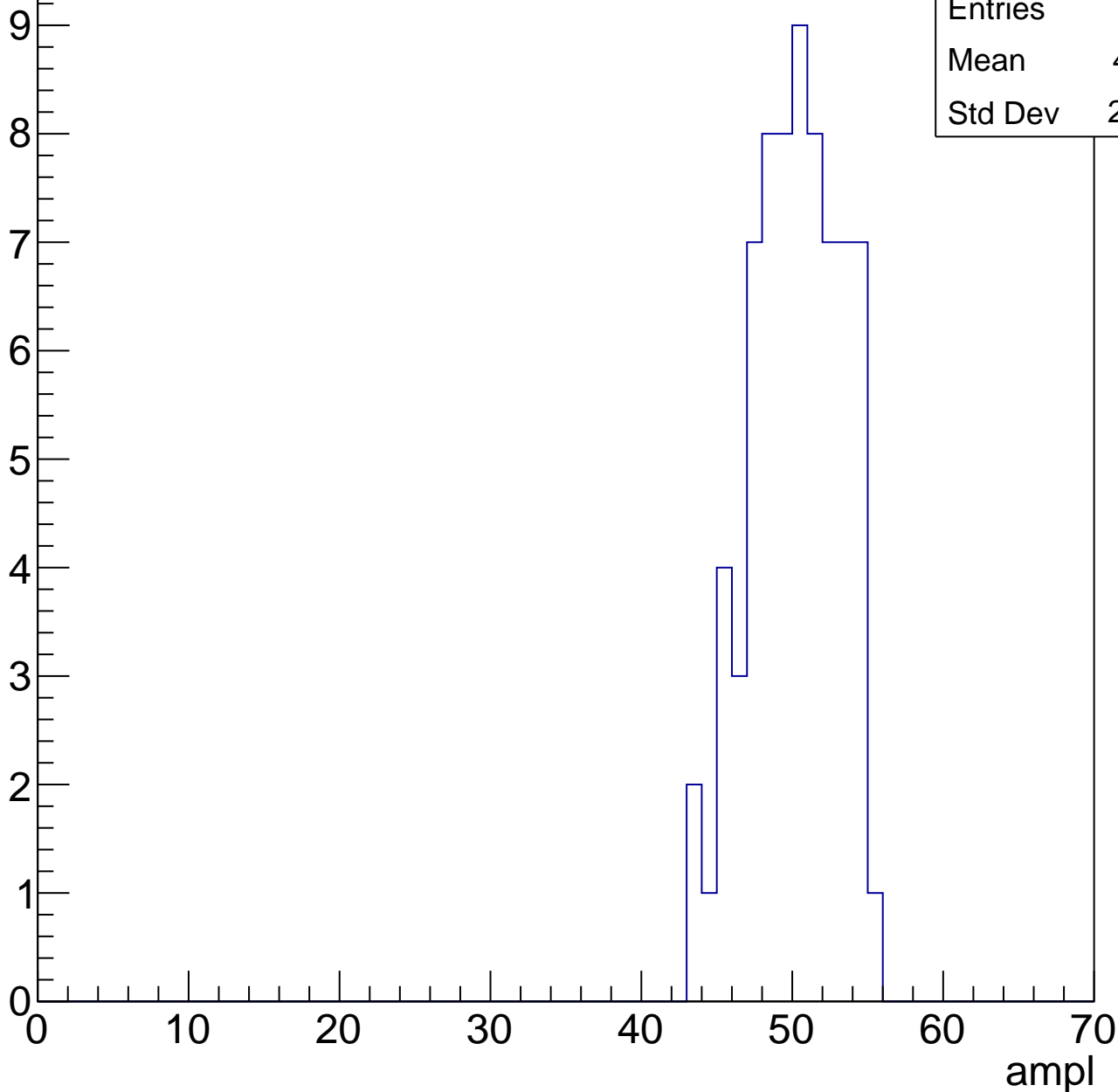
**Gaus Width: 3.2114**



# B1L003S, U3-ch29, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

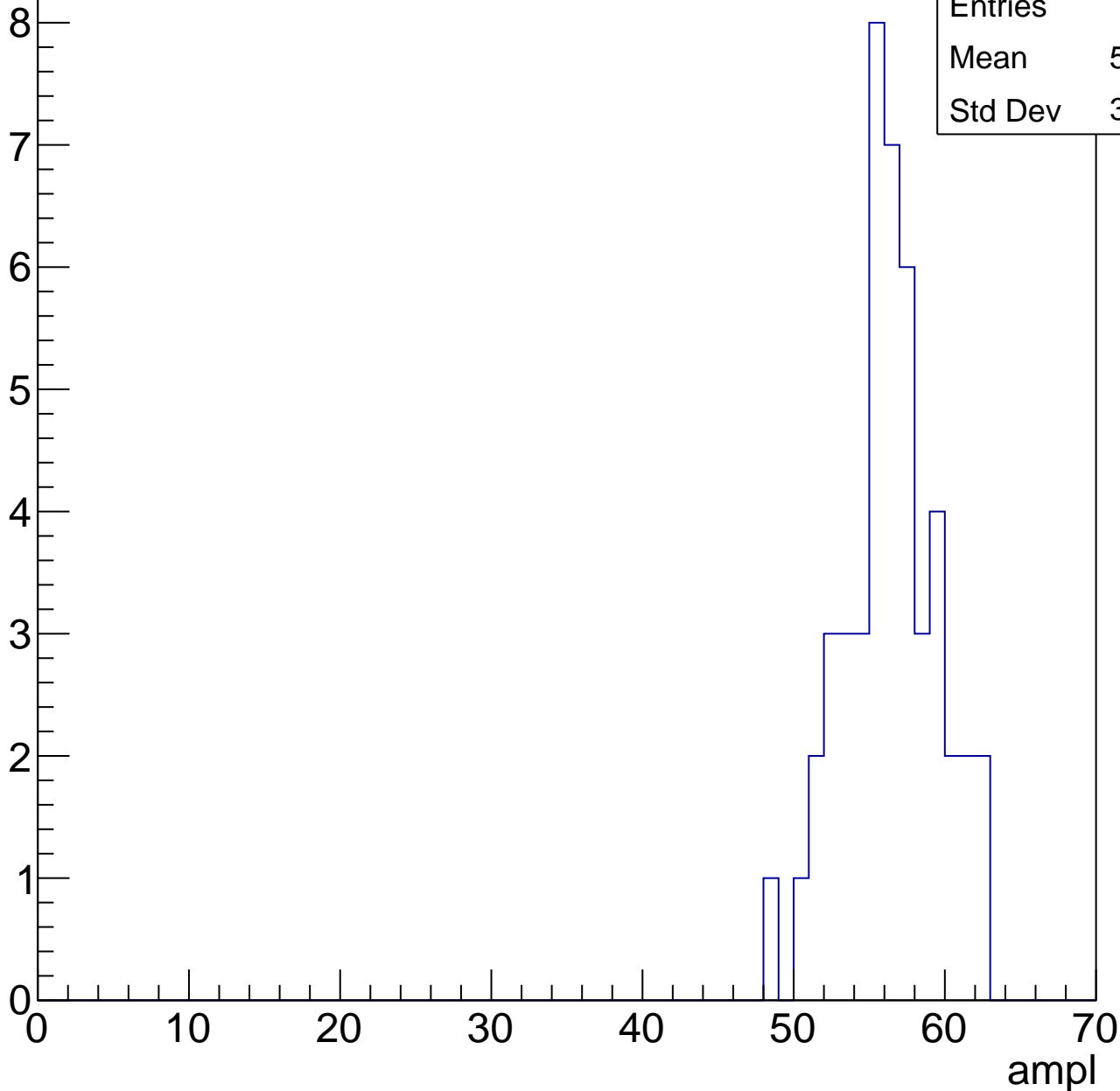


# B1L003S, U3-ch29, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	47
Mean	55.89
Std Dev	3.103



# B1L003S, U3-ch29, adc5

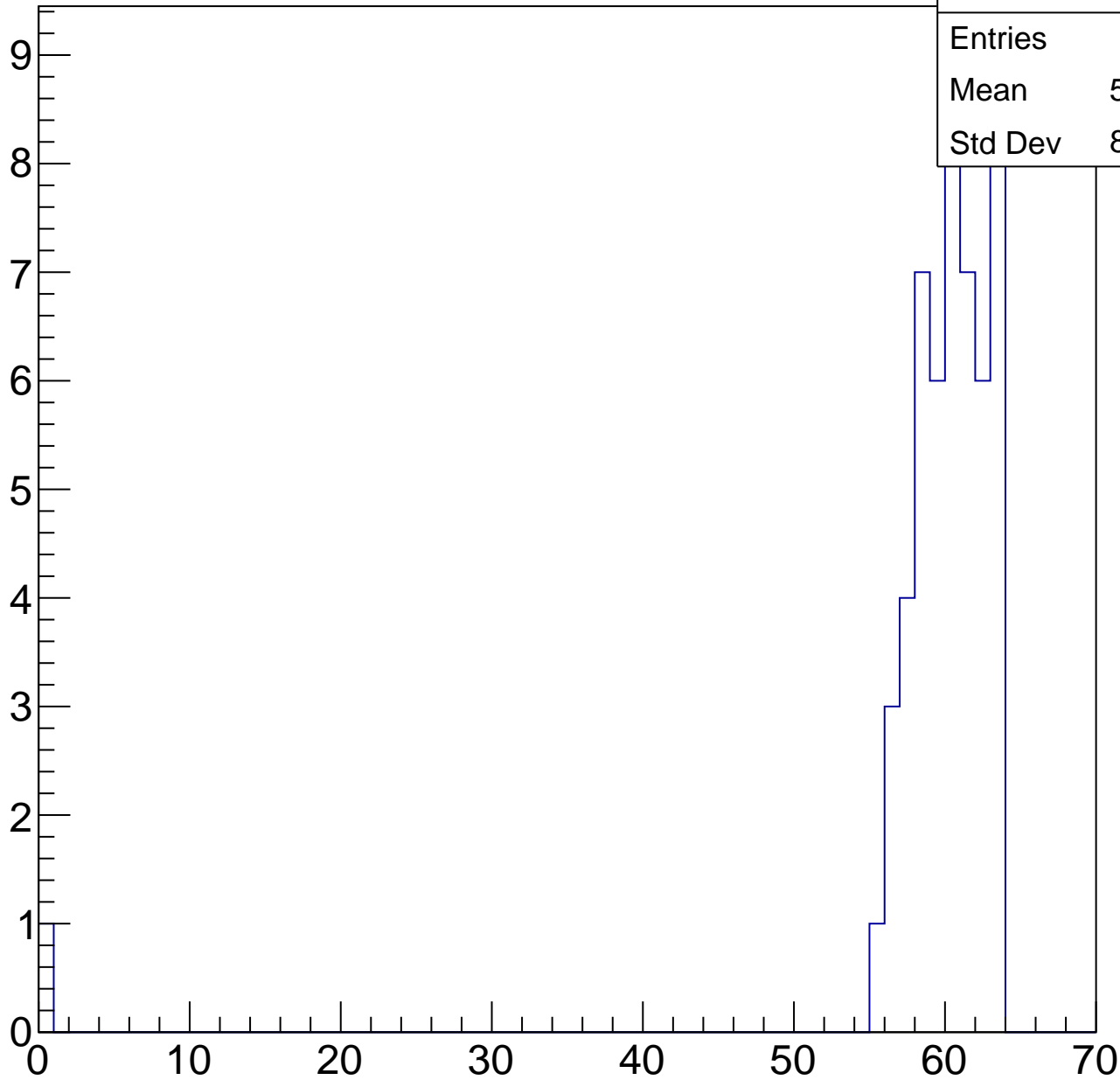
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	52
Mean	58.79
Std Dev	8.524

ampl



# B1L003S, U3-ch29, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

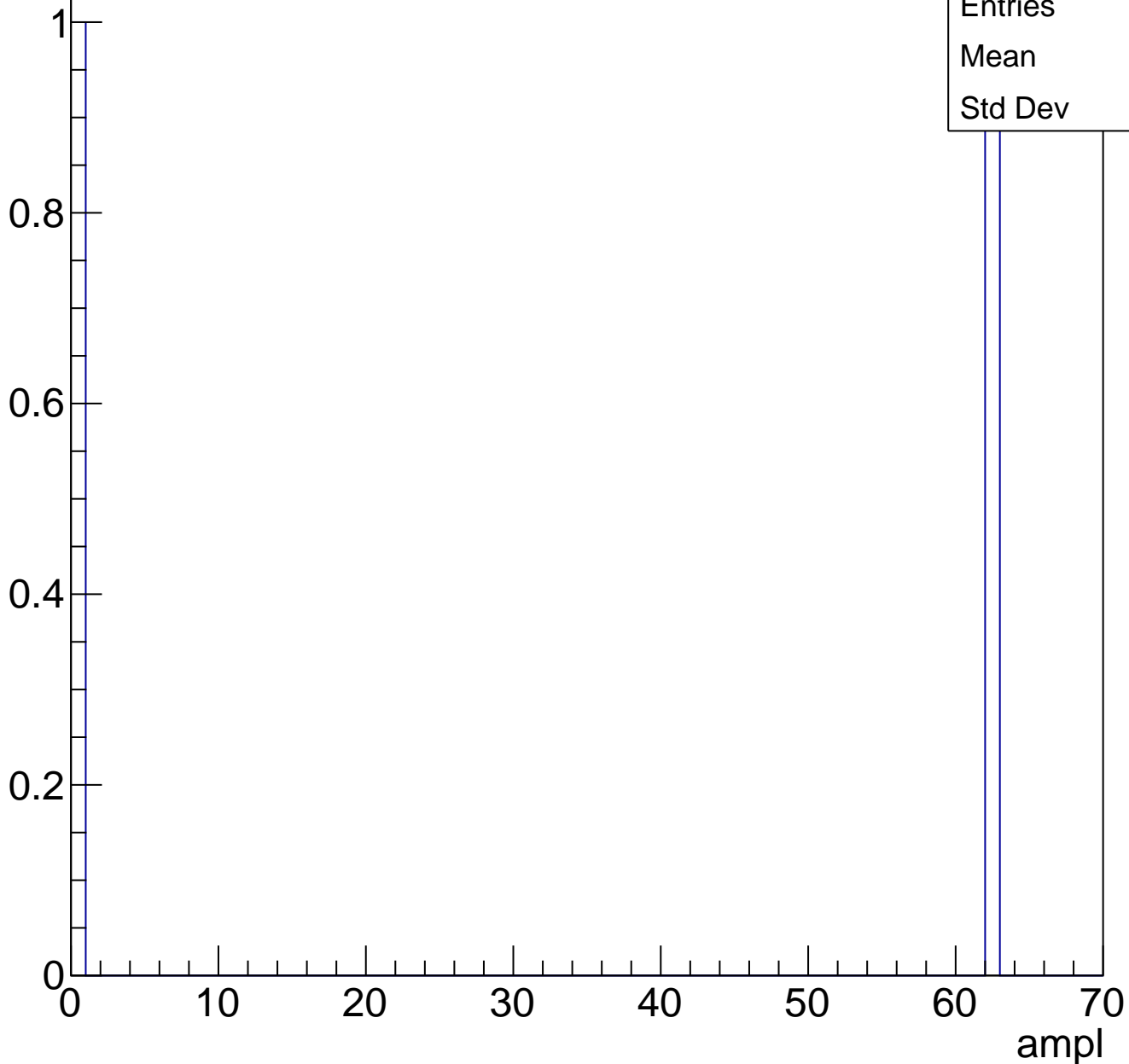




# B1L003S, U3-ch29, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U3-ch30, adc0

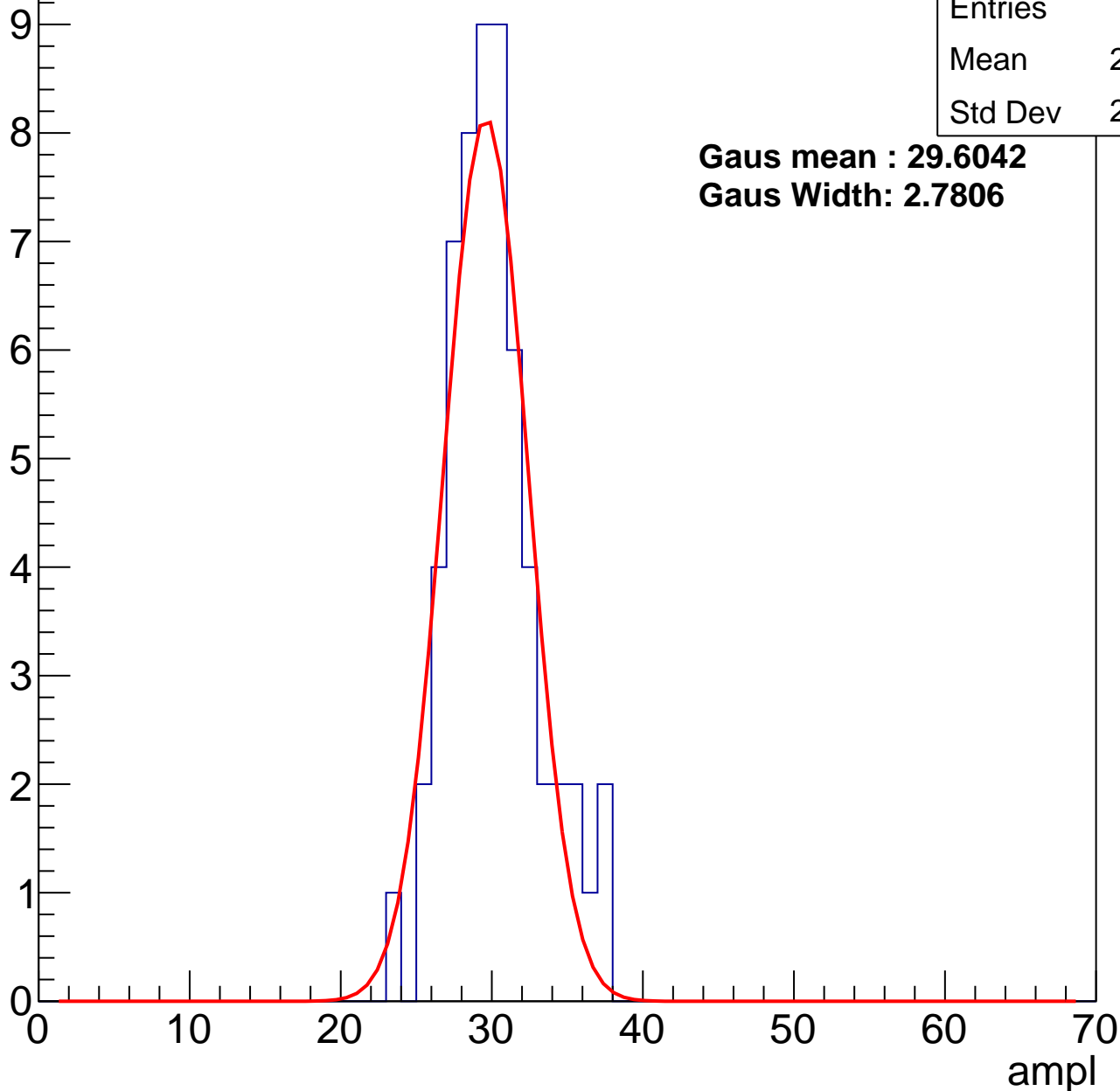
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	29.64
Std Dev	2.956

**Gaus mean : 29.6042**

**Gaus Width: 2.7806**



# B1L003S, U3-ch30, adc1

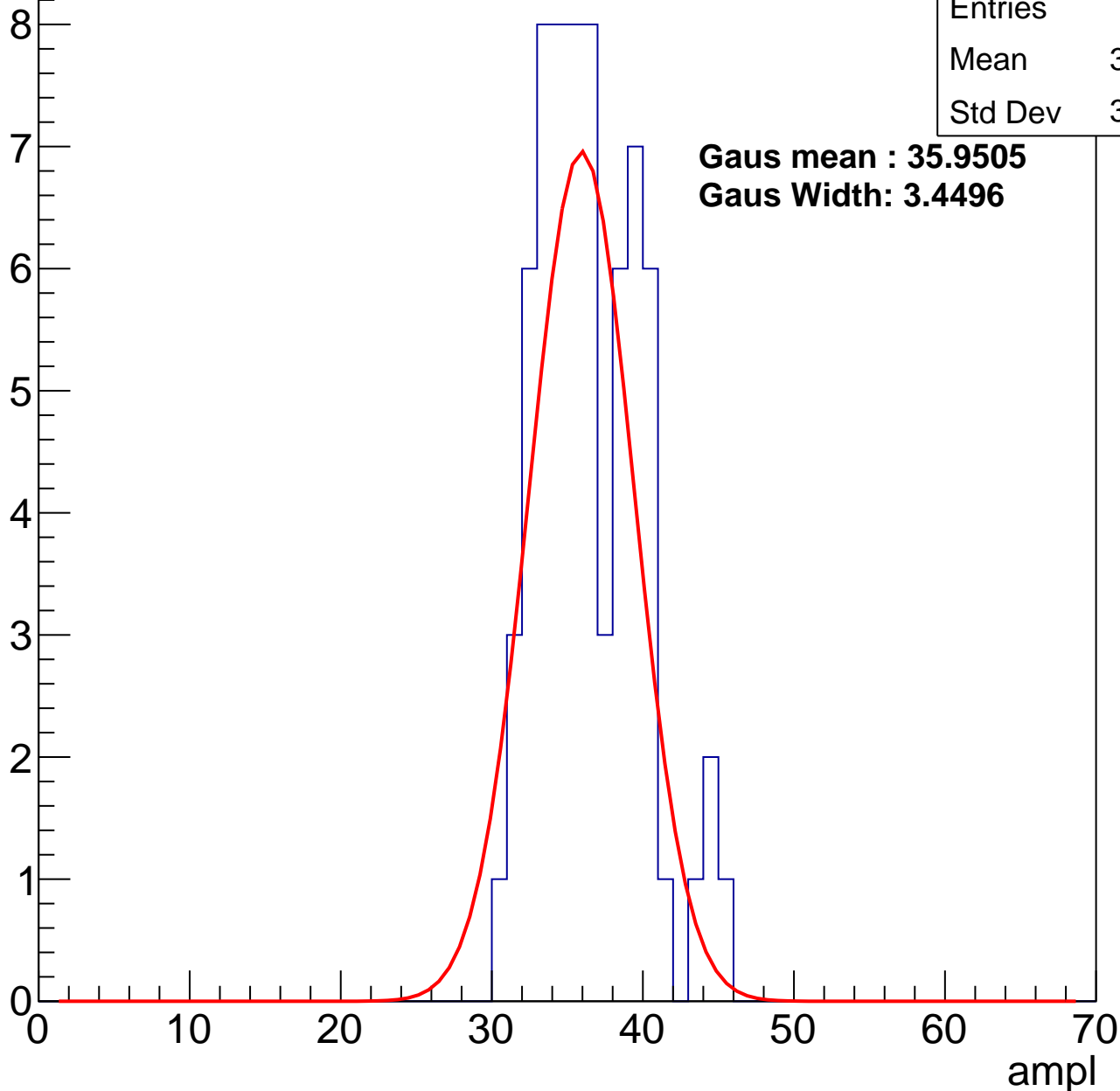
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	36.06
Std Dev	3.379

**Gaus mean : 35.9505**

**Gaus Width: 3.4496**



# B1L003S, U3-ch30, adc2

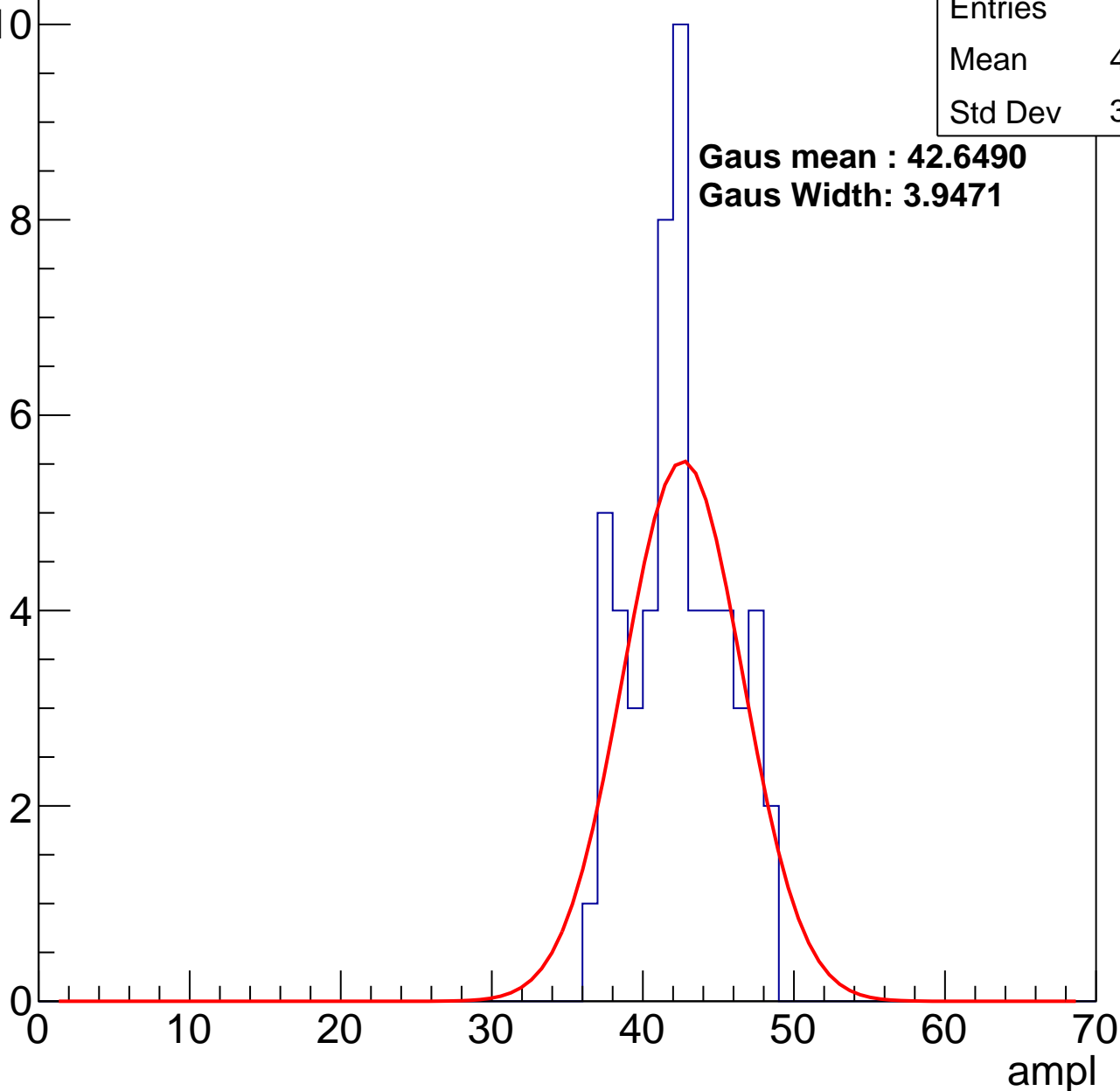
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	41.93
Std Dev	3.139

**Gaus mean : 42.6490**

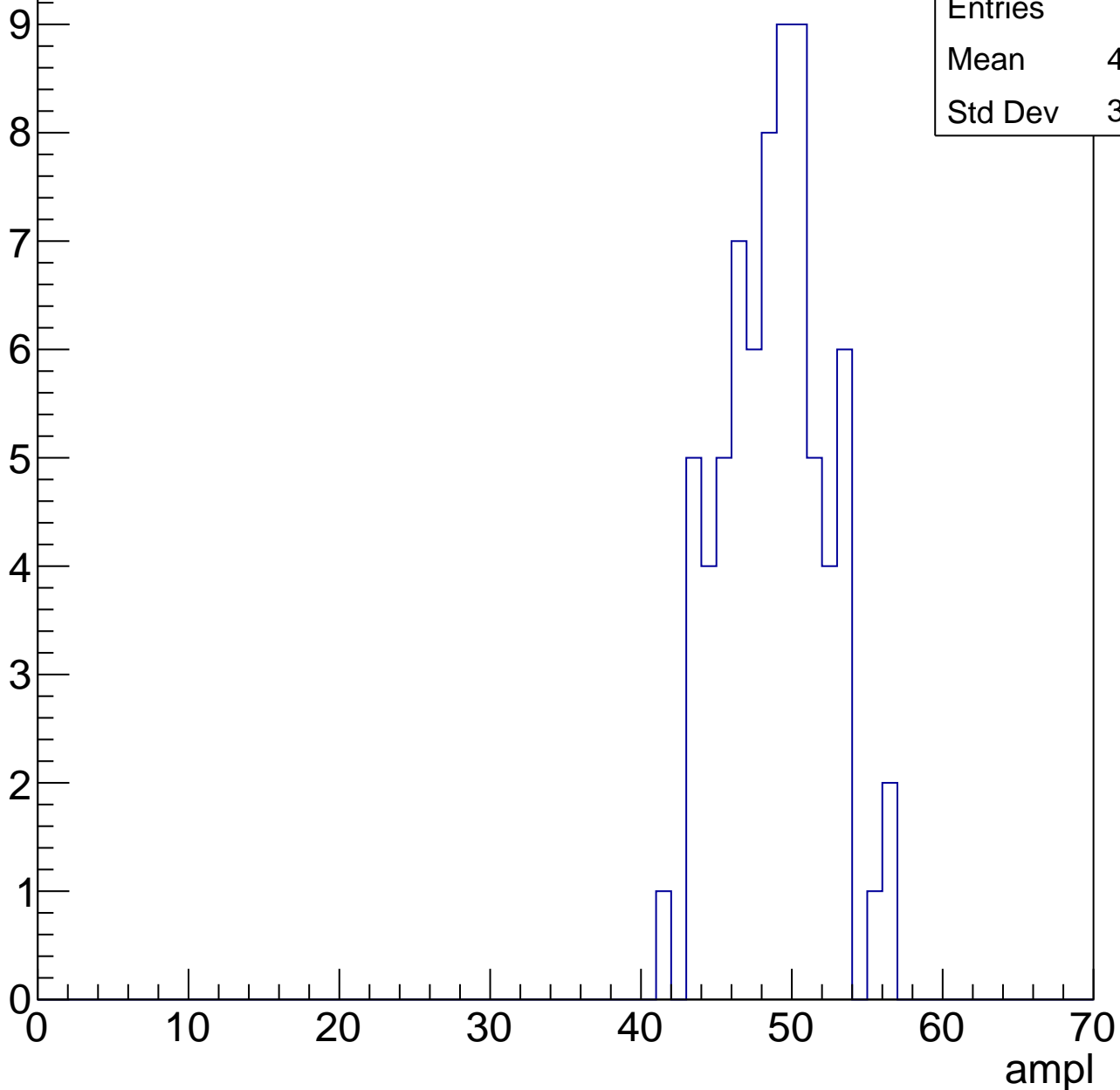
**Gaus Width: 3.9471**



# B1L003S, U3-ch30, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



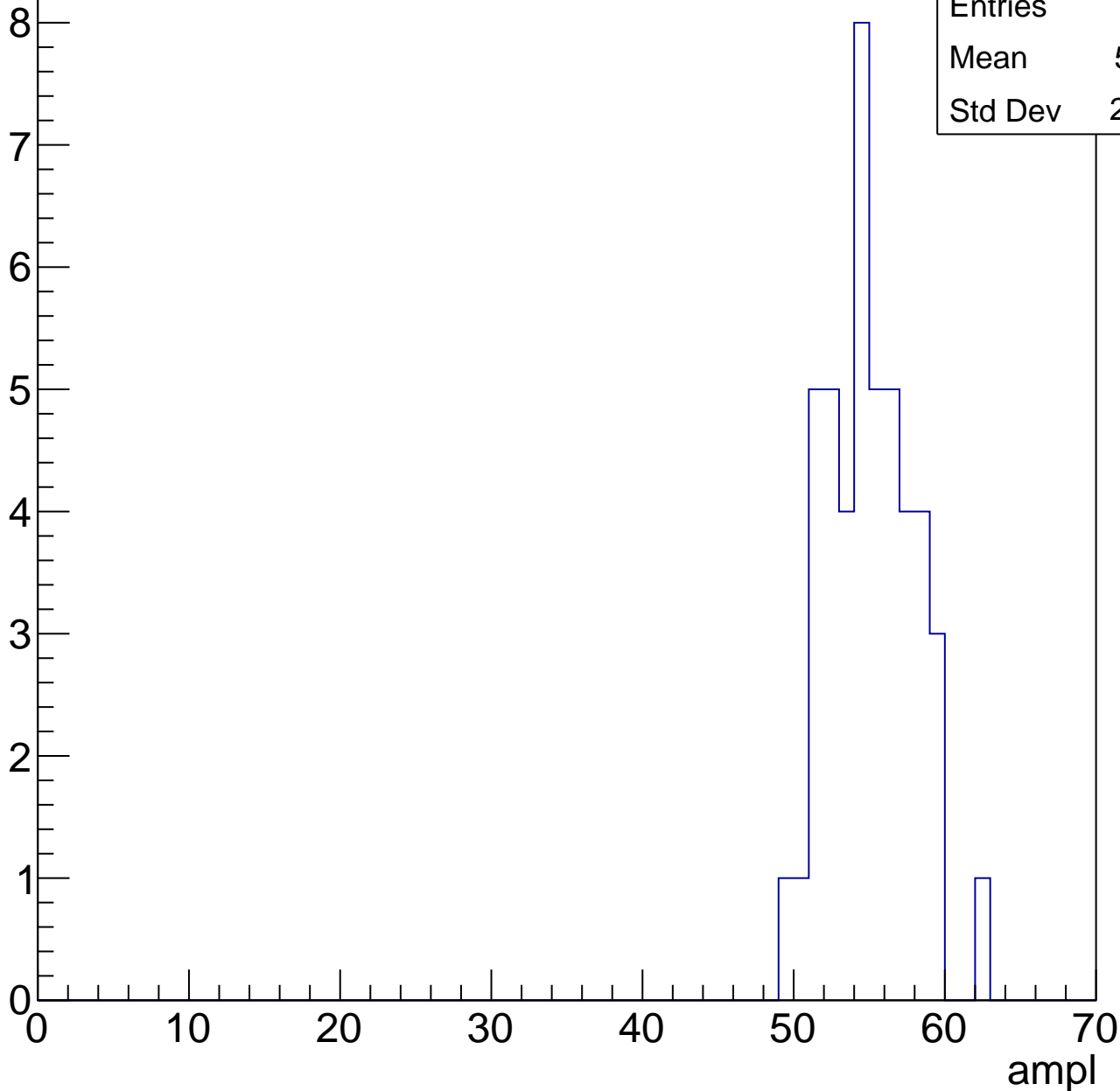
Entries	72
Mean	48.39
Std Dev	3.306

# B1L003S, U3-ch30, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	46
Mean	54.61
Std Dev	2.786

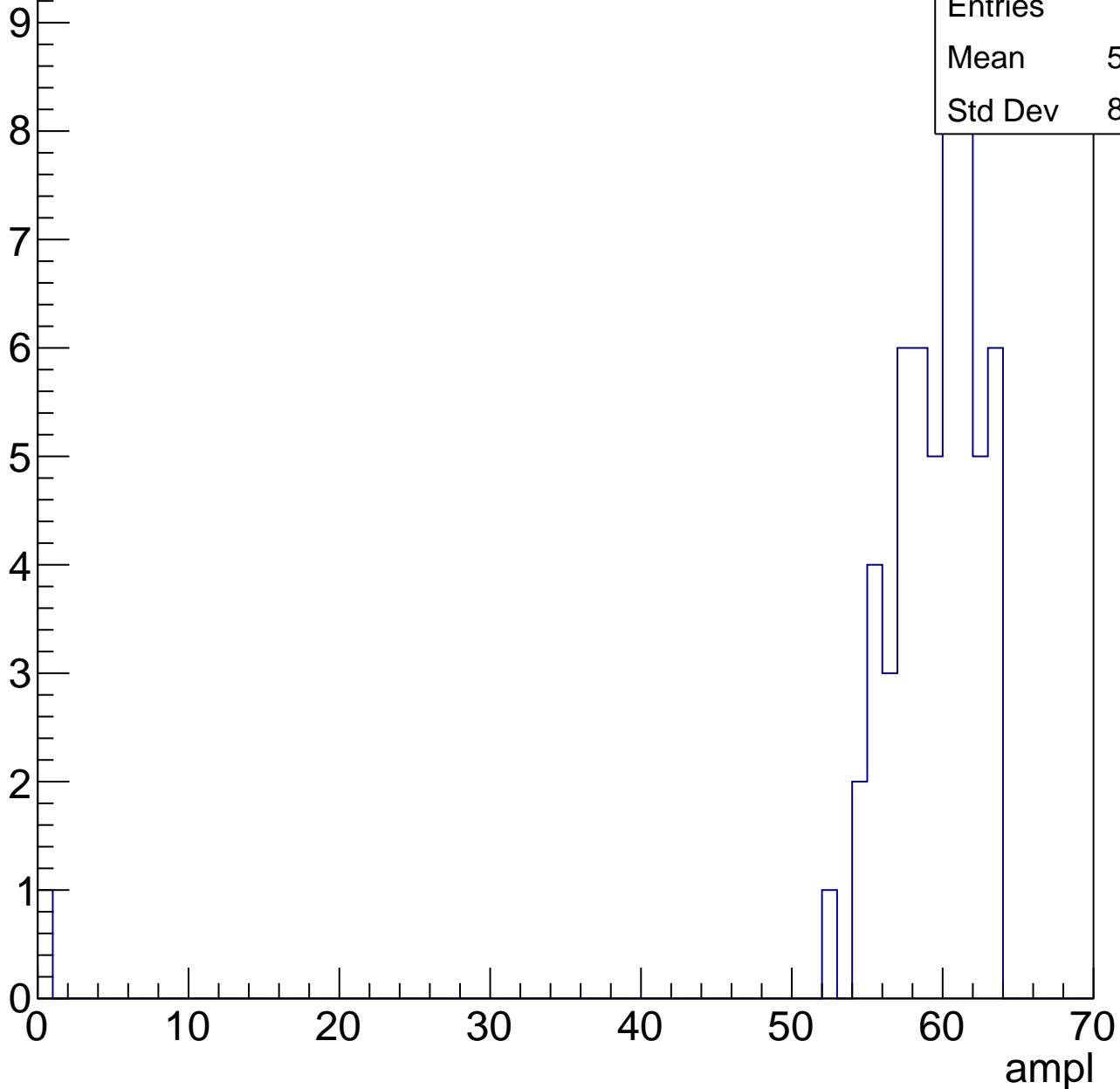


# B1L003S, U3-ch30, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

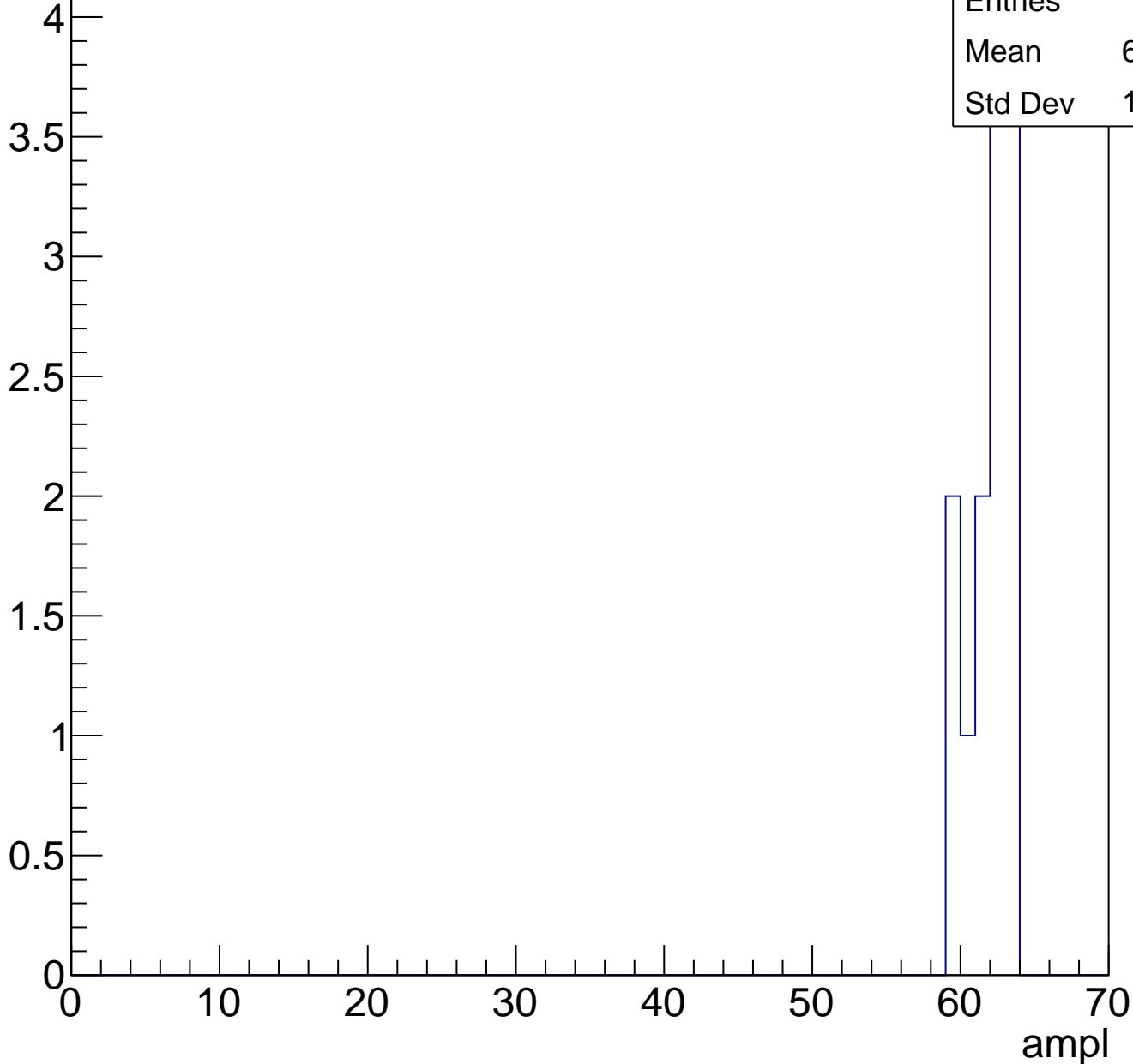
Entries	56
Mean	58.02
Std Dev	8.269



# B1L003S, U3-ch30, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch30, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U3-ch31, adc0

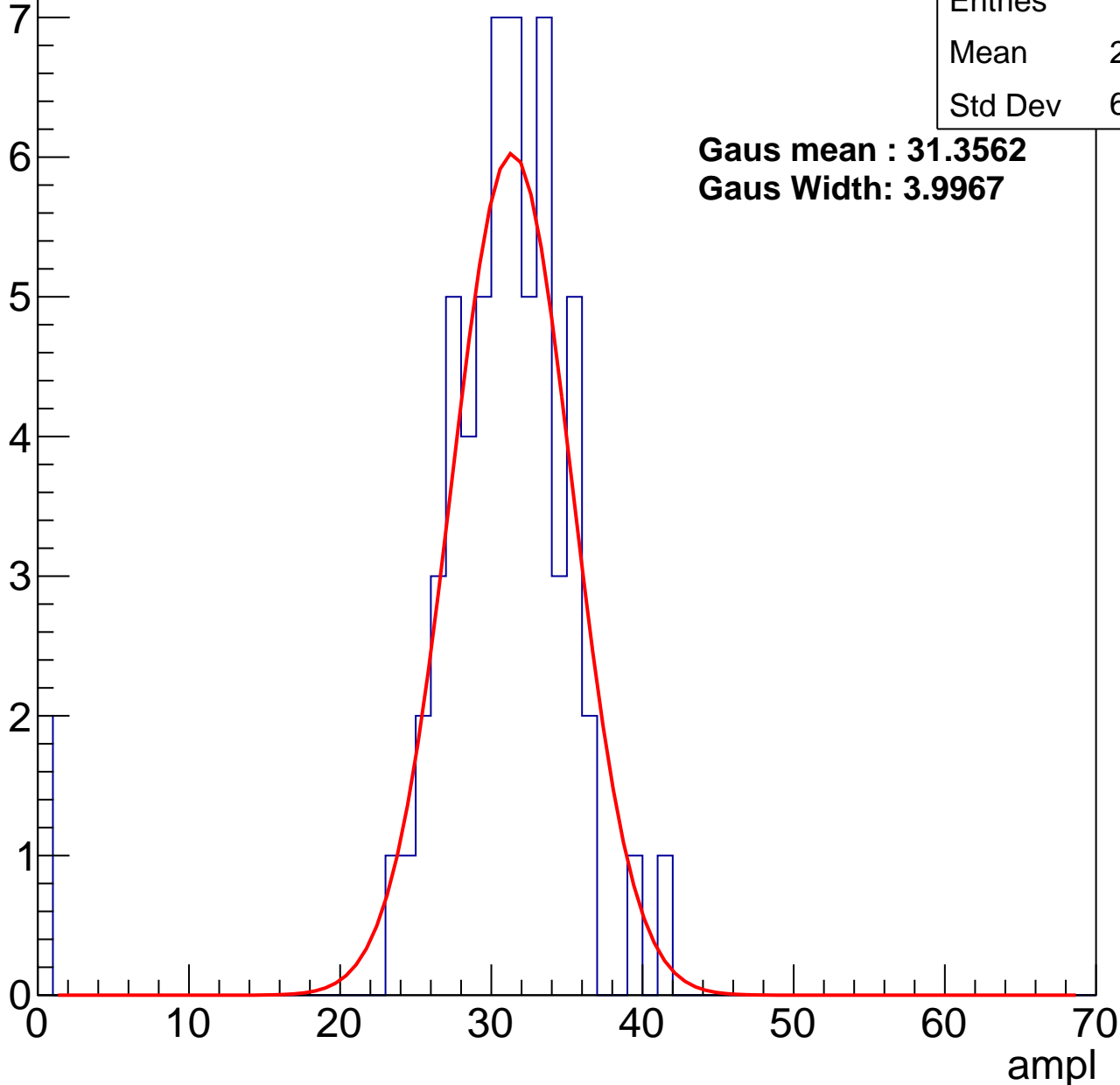
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	29.74
Std Dev	6.506

**Gaus mean : 31.3562**

**Gaus Width: 3.9967**



# B1L003S, U3-ch31, adc1

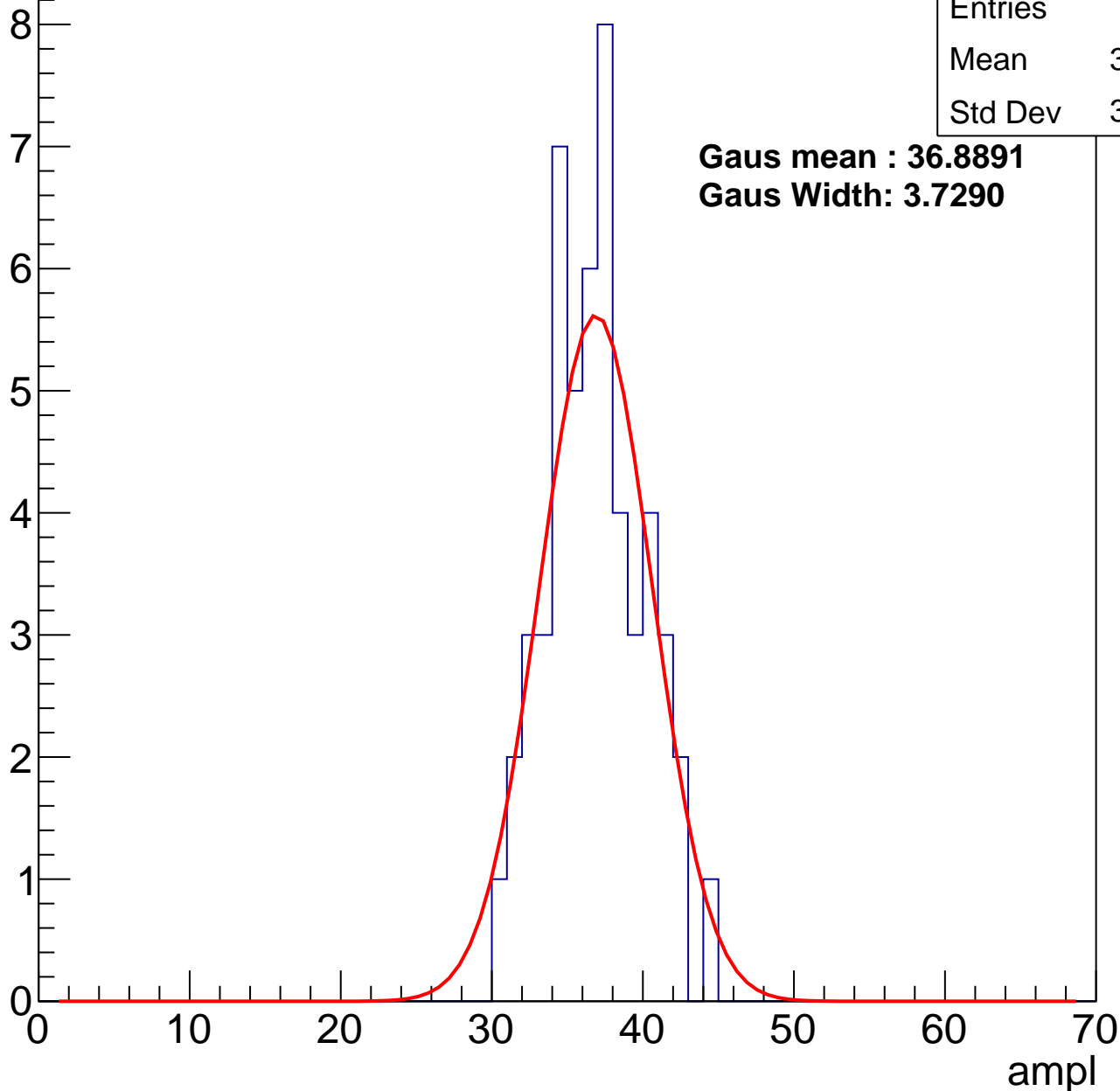
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	52
Mean	36.38
Std Dev	3.139

**Gaus mean : 36.8891**

**Gaus Width: 3.7290**



# B1L003S, U3-ch31, adc2

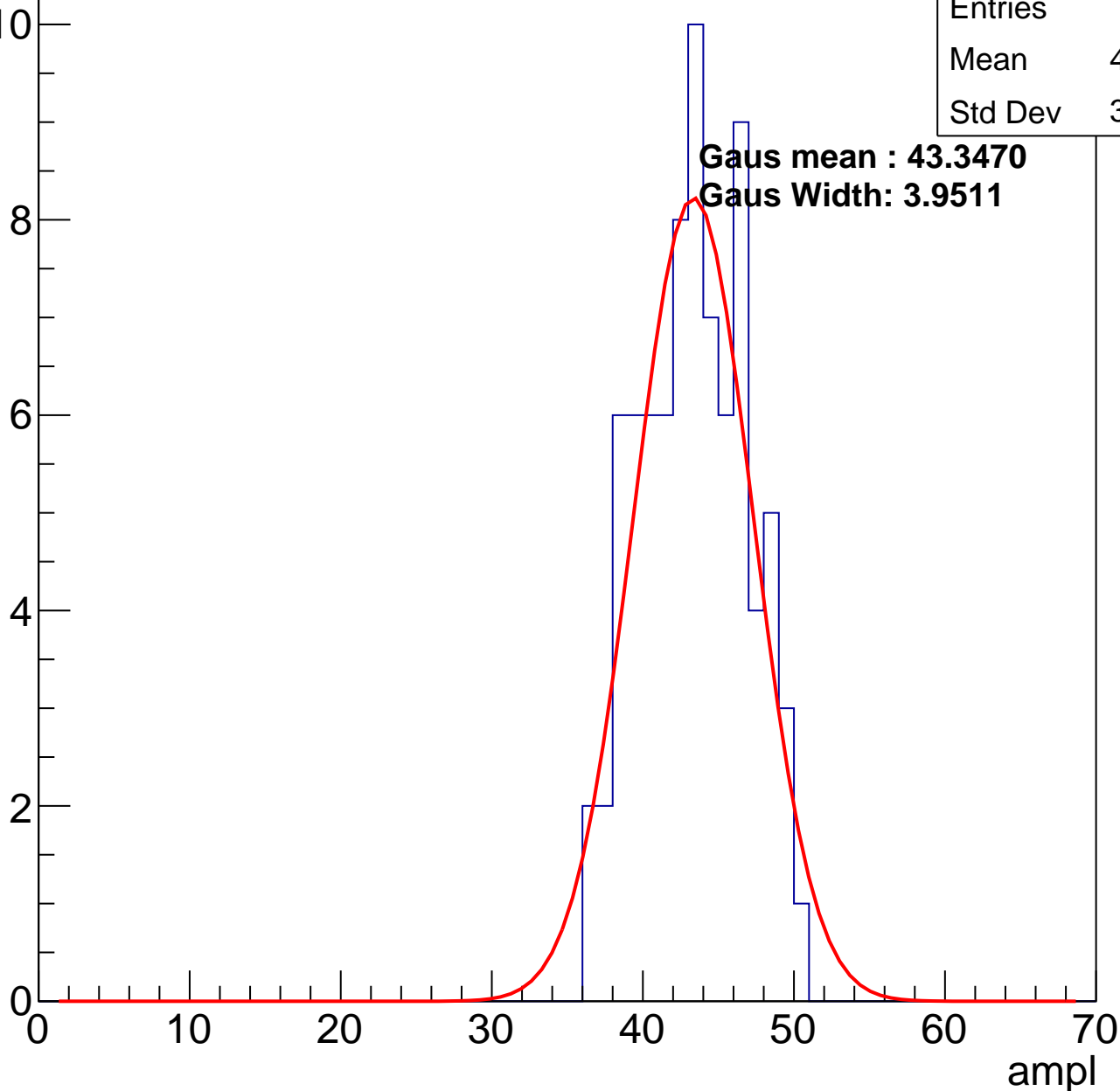
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	81
Mean	42.93
Std Dev	3.442

**Gaus mean : 43.3470**

**Gaus Width: 3.9511**

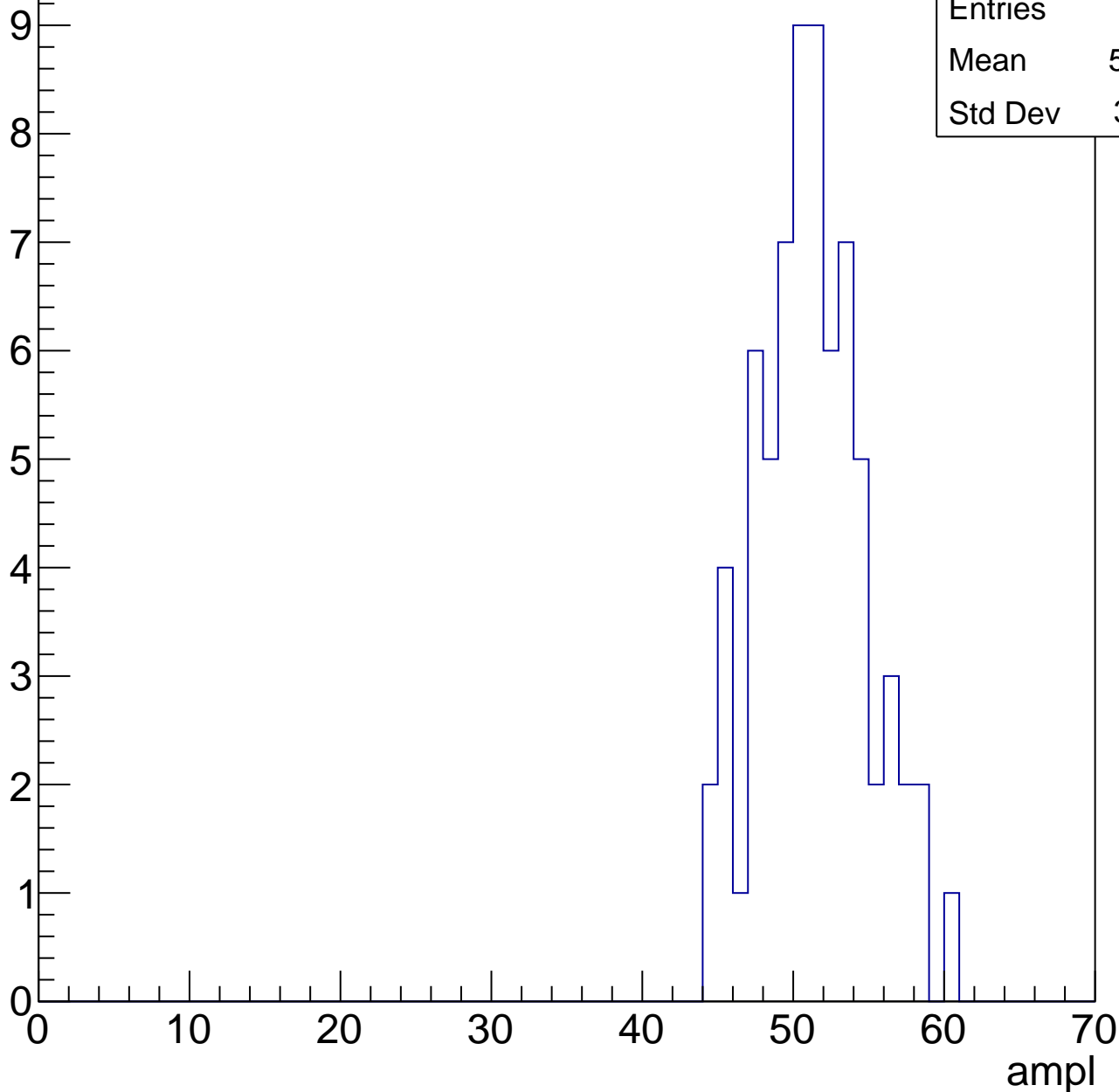


# B1L003S, U3-ch31, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	71
Mean	50.83
Std Dev	3.521

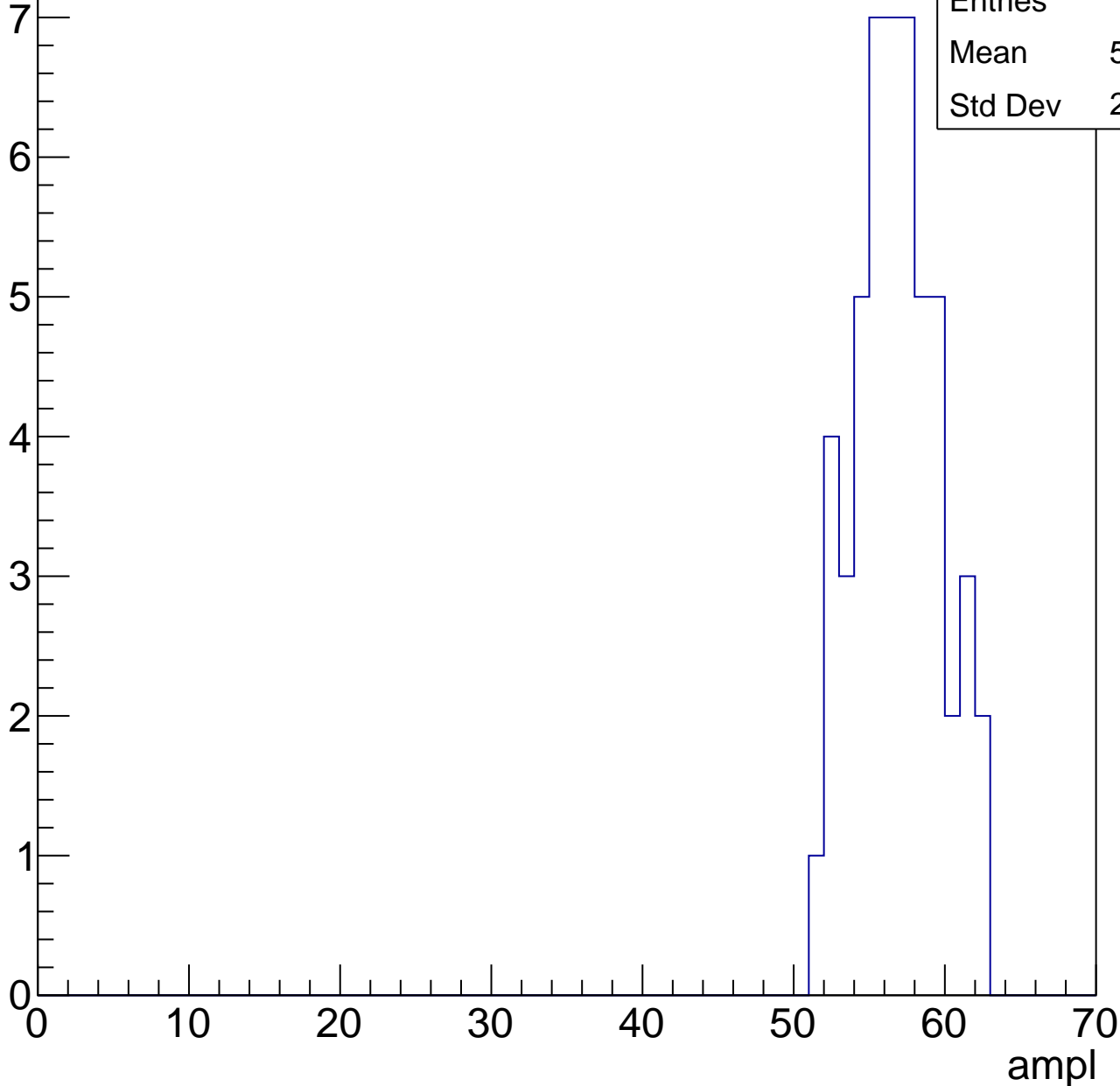


# B1L003S, U3-ch31, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	51
Mean	56.39
Std Dev	2.752

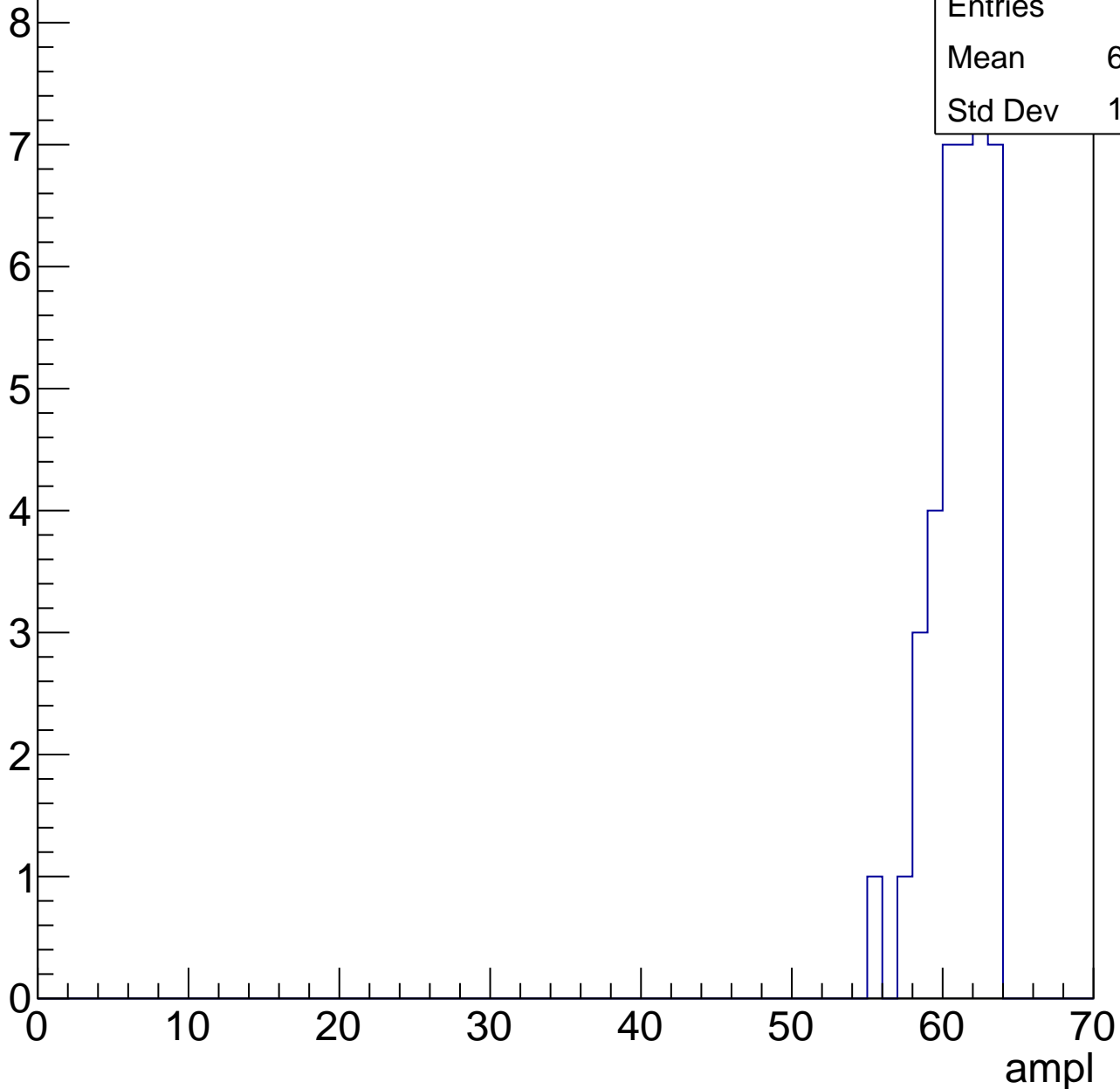


# B1L003S, U3-ch31, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

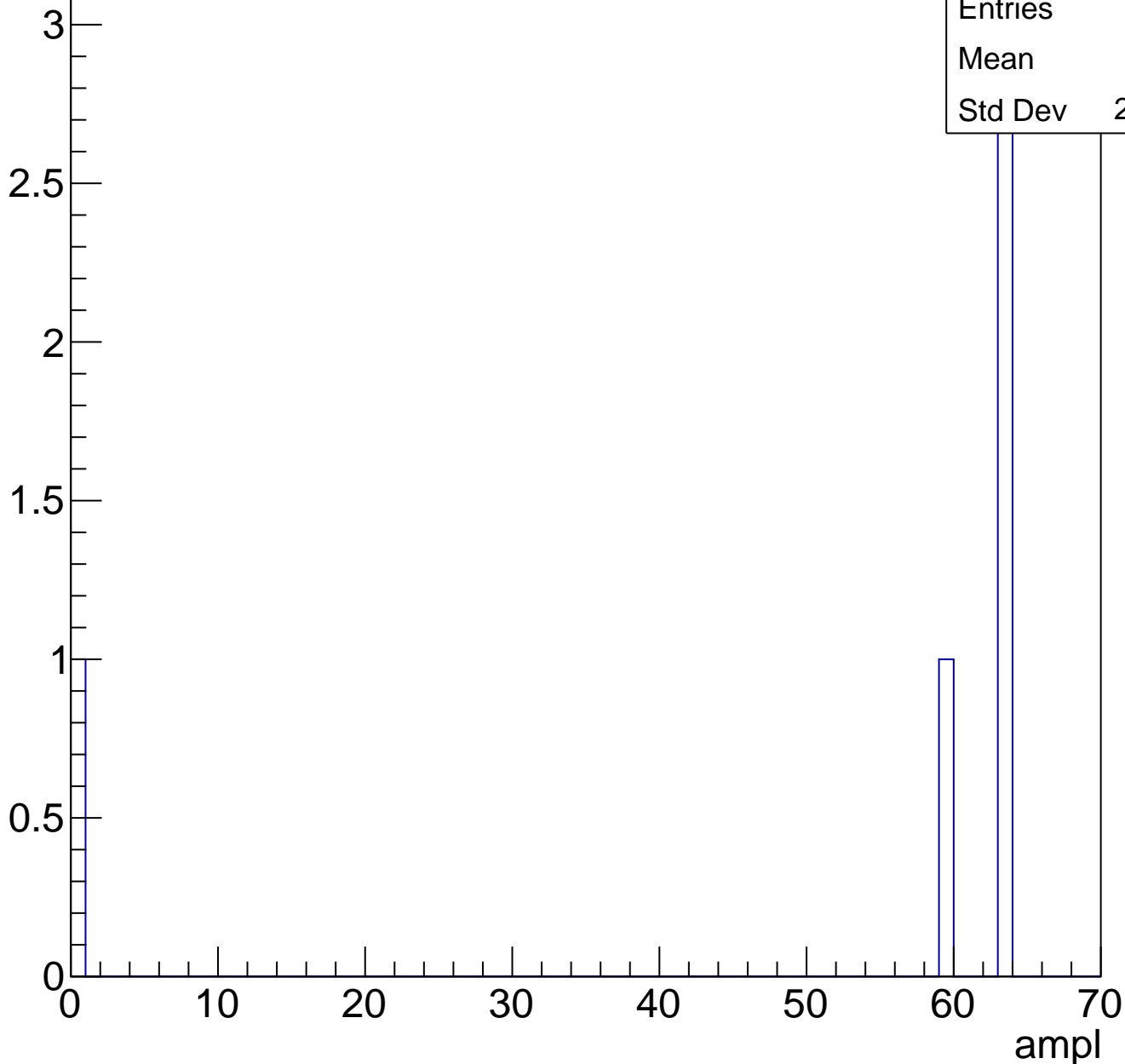
Entries	38
Mean	60.68
Std Dev	1.879



# B1L003S, U3-ch31, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch31, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U3-ch32, adc0

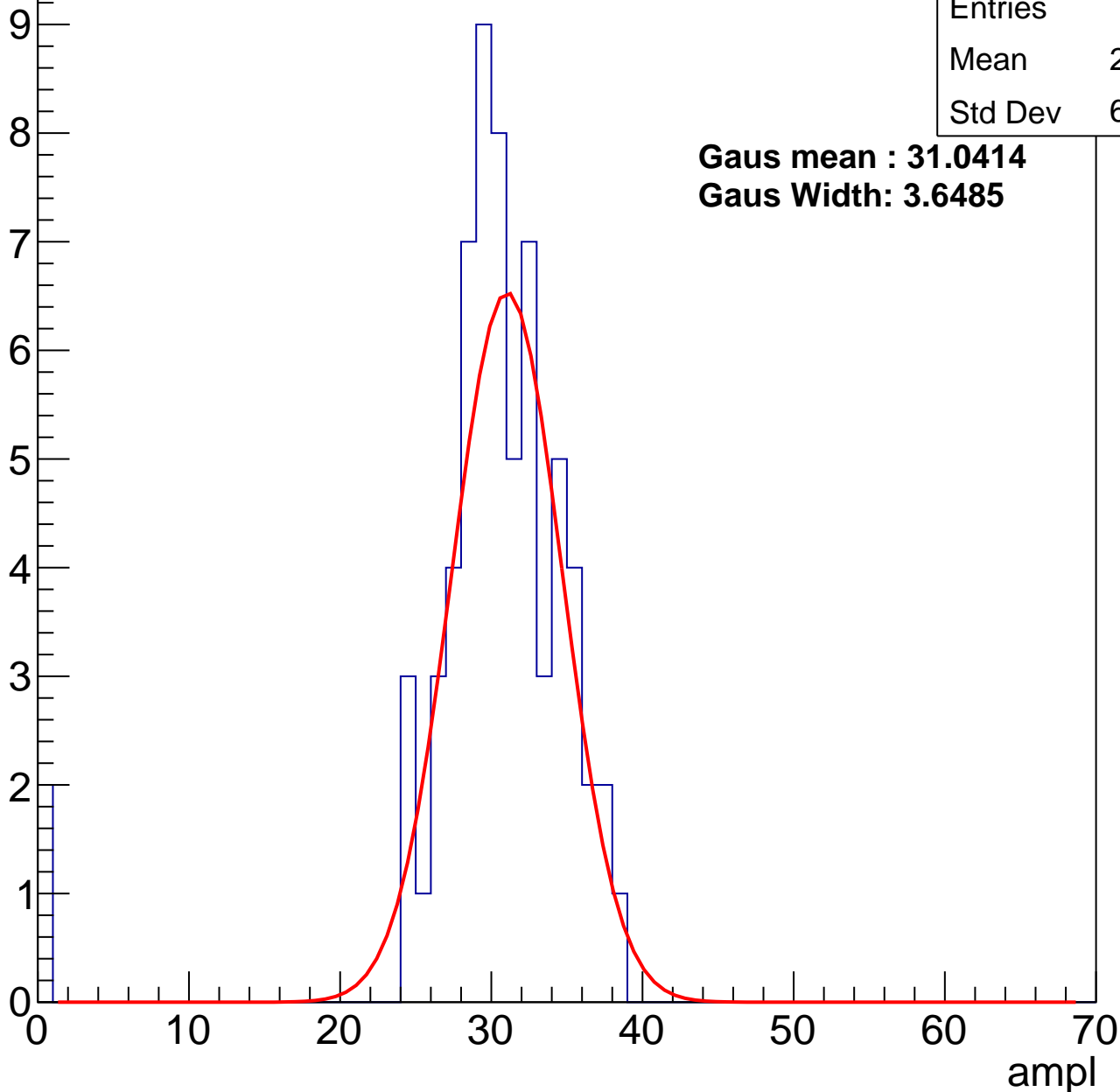
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	29.58
Std Dev	6.174

**Gaus mean : 31.0414**

**Gaus Width: 3.6485**



# B1L003S, U3-ch32, adc1

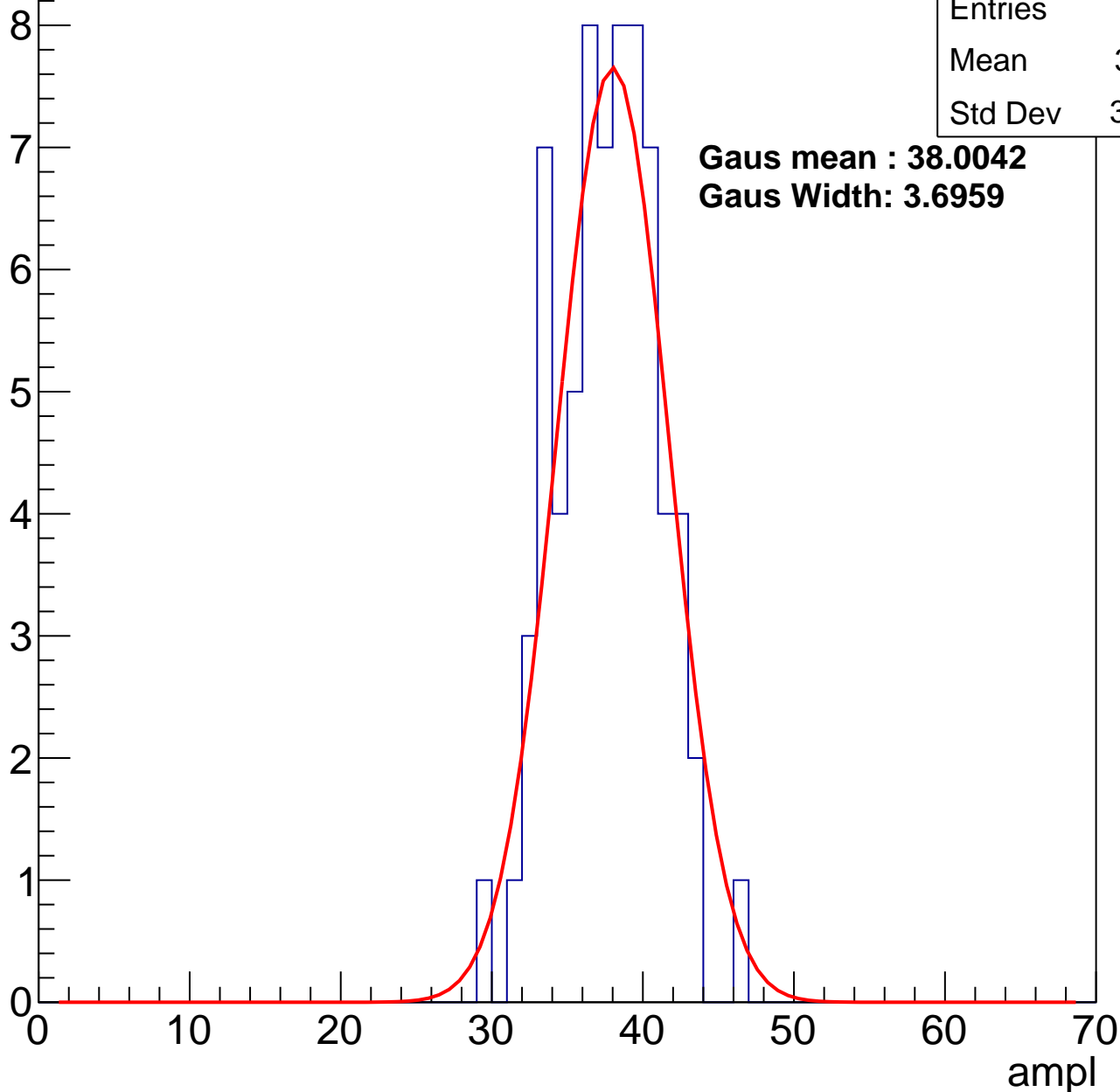
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	37.21
Std Dev	3.312

**Gaus mean : 38.0042**

**Gaus Width: 3.6959**



# B1L003S, U3-ch32, adc2

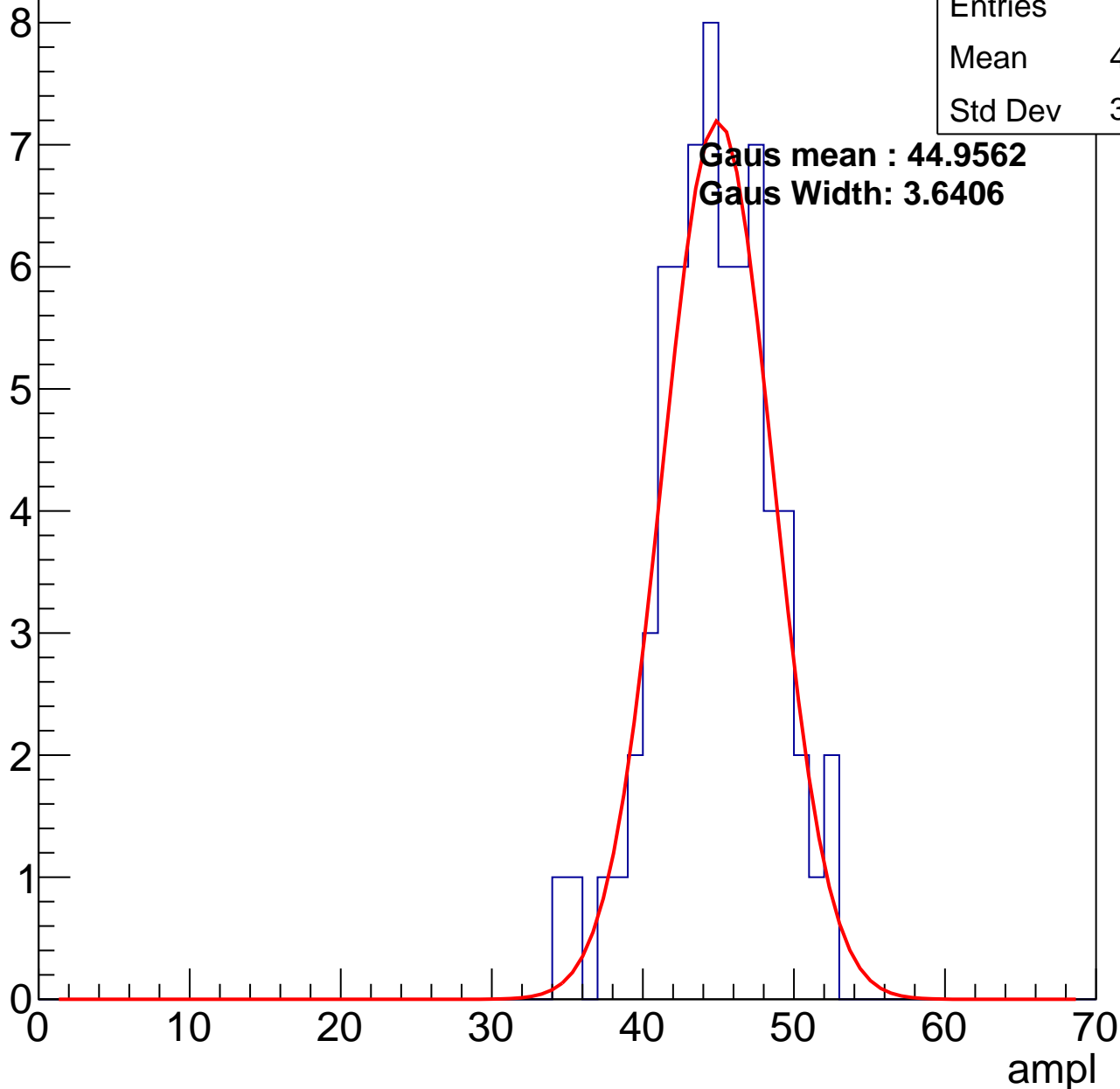
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	44.28
Std Dev	3.737

**Gaus mean : 44.9562**

**Gaus Width: 3.6406**

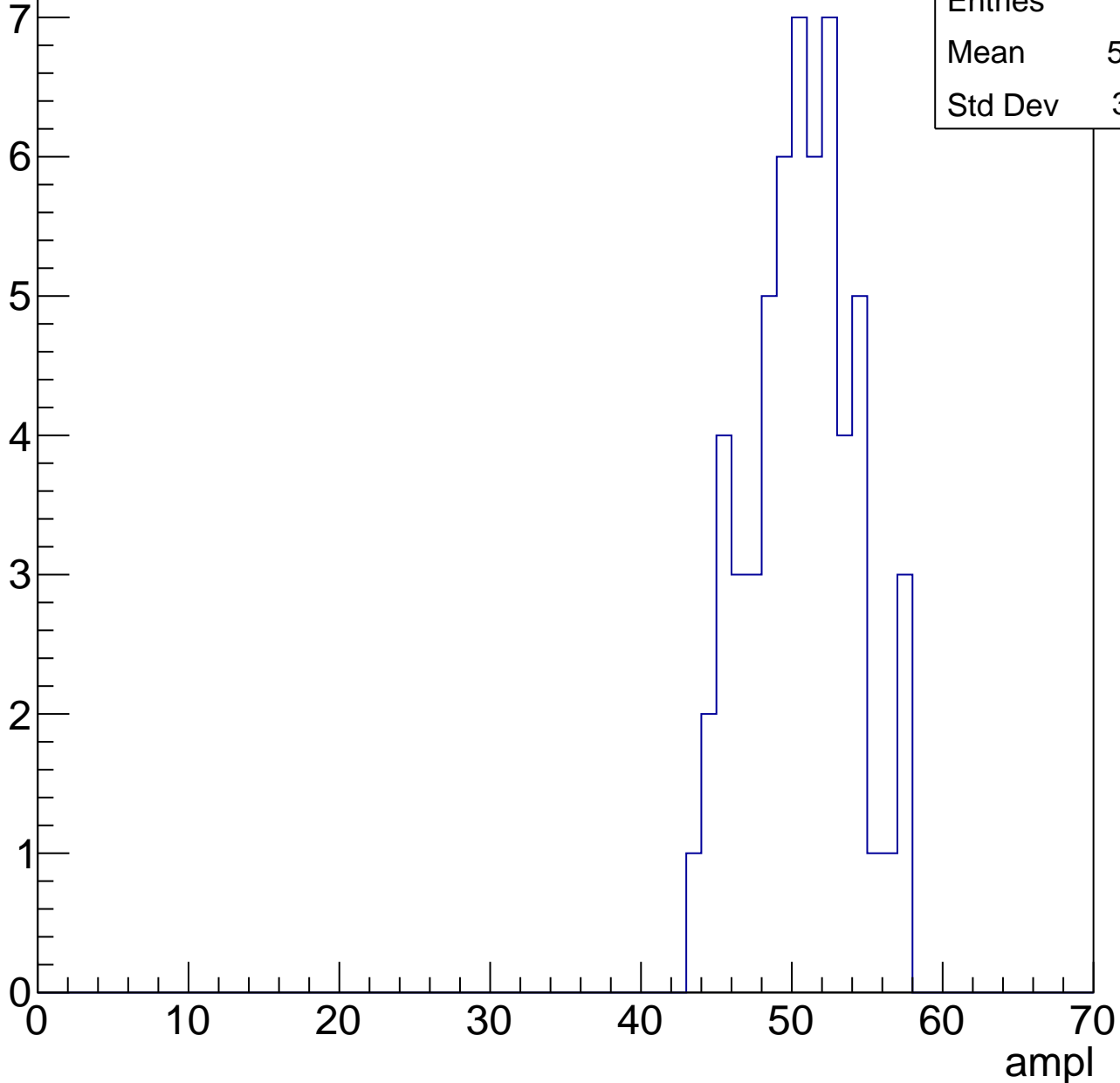


# B1L003S, U3-ch32, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	50.14
Std Dev	3.421

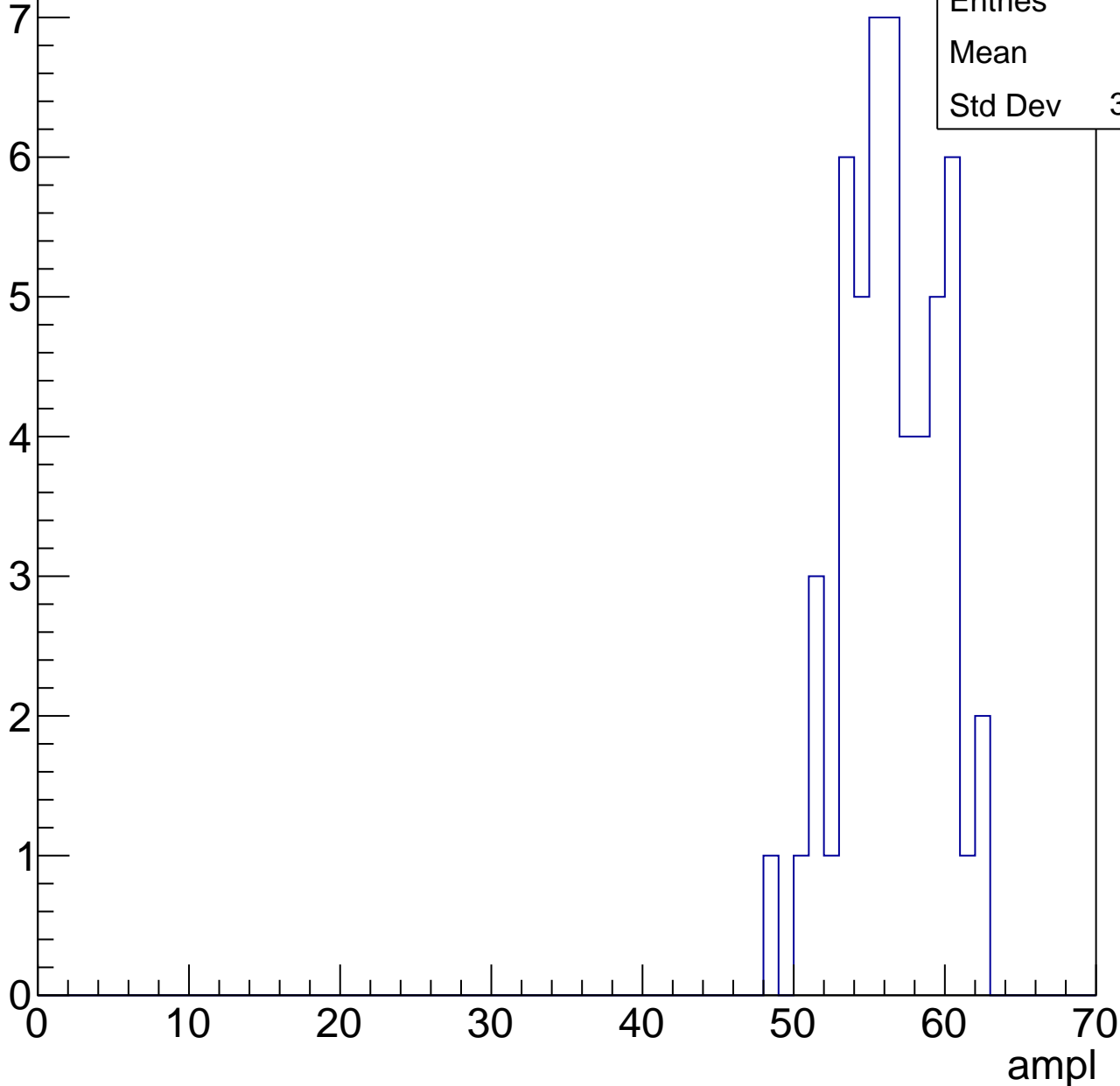


# B1L003S, U3-ch32, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

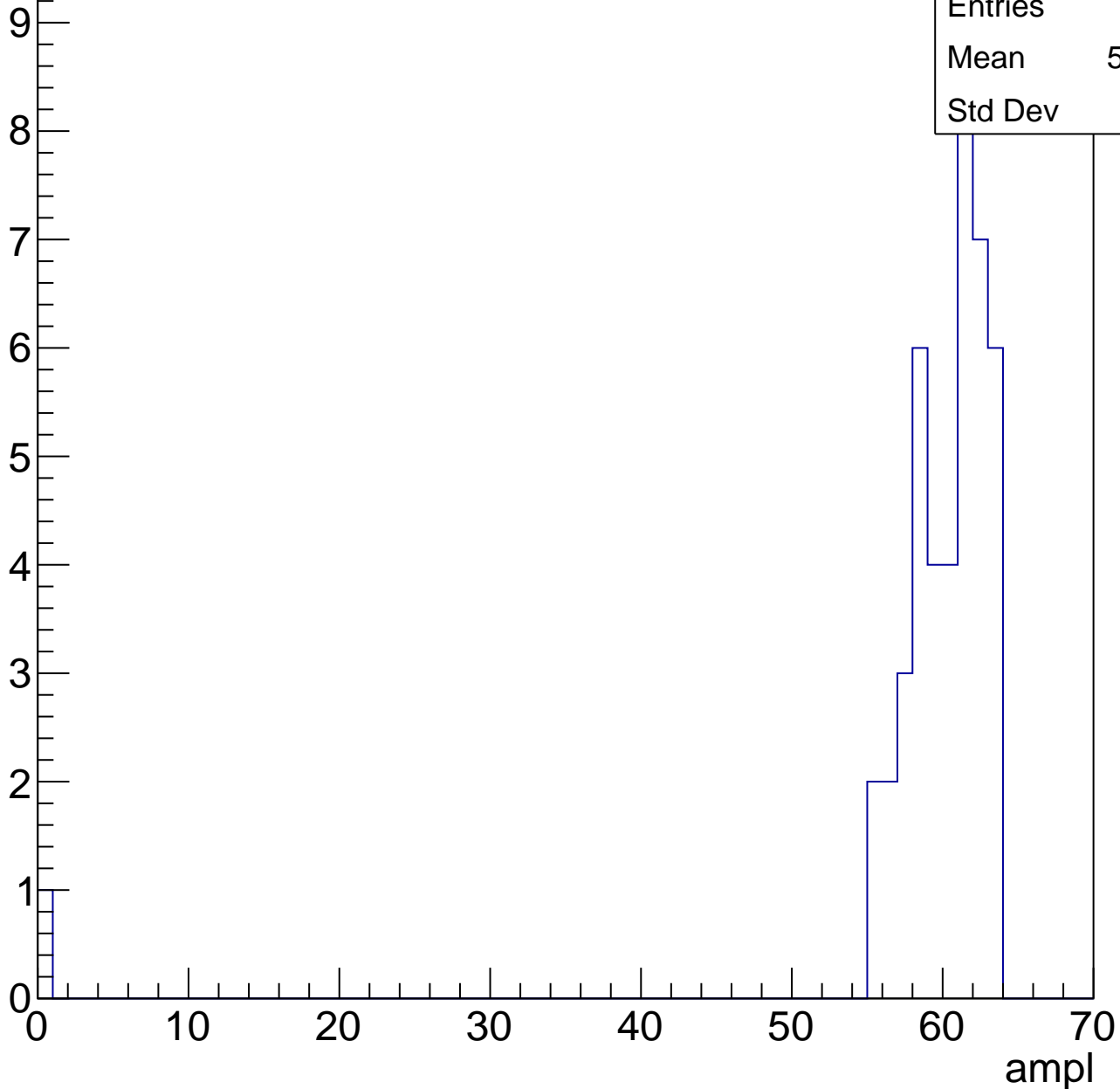
Entries	53
Mean	56
Std Dev	3.162



# B1L003S, U3-ch32, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

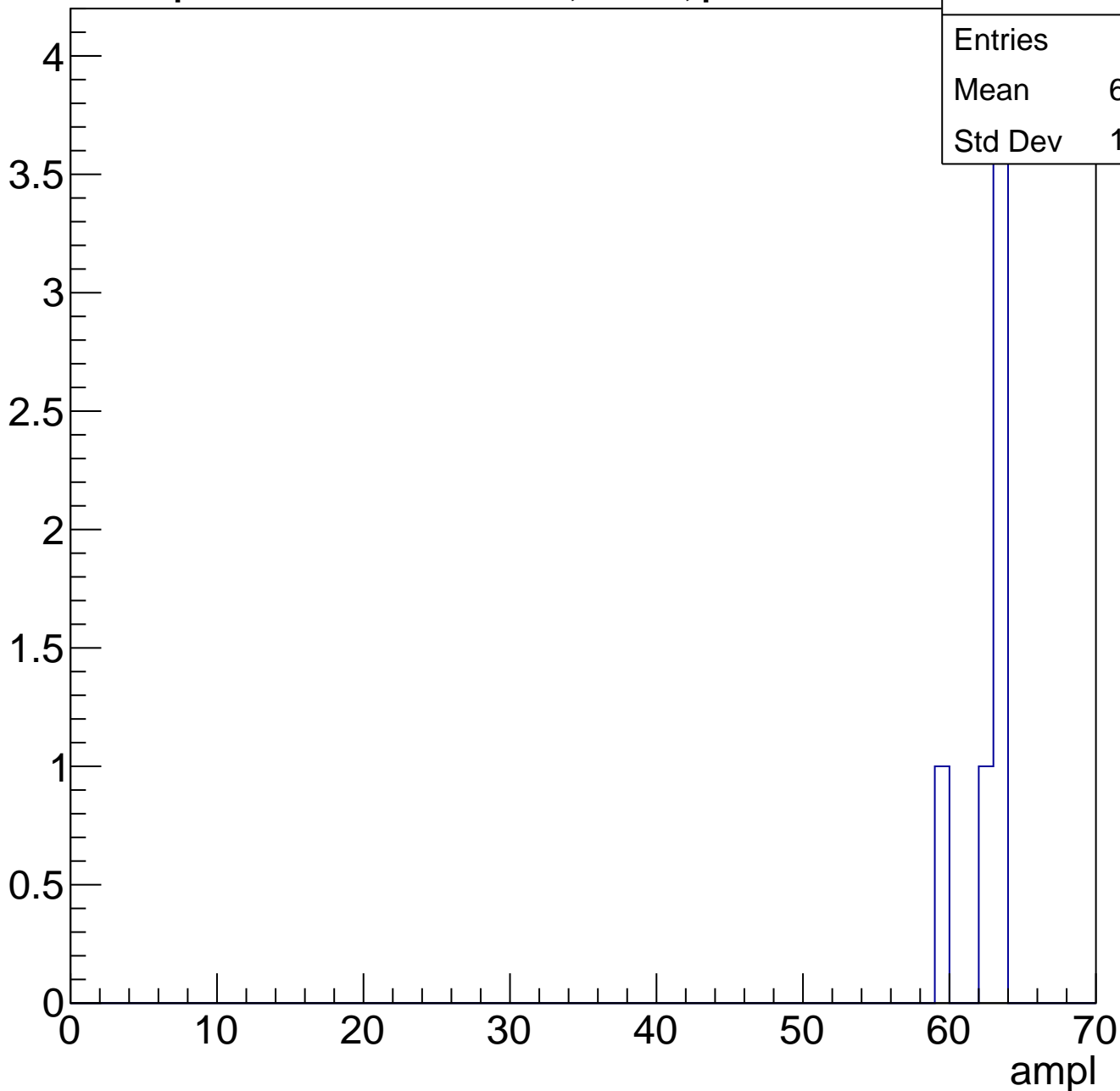


Entries	44
Mean	58.59
Std Dev	9.22

# B1L003S, U3-ch32, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch32, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U3-ch33, adc0

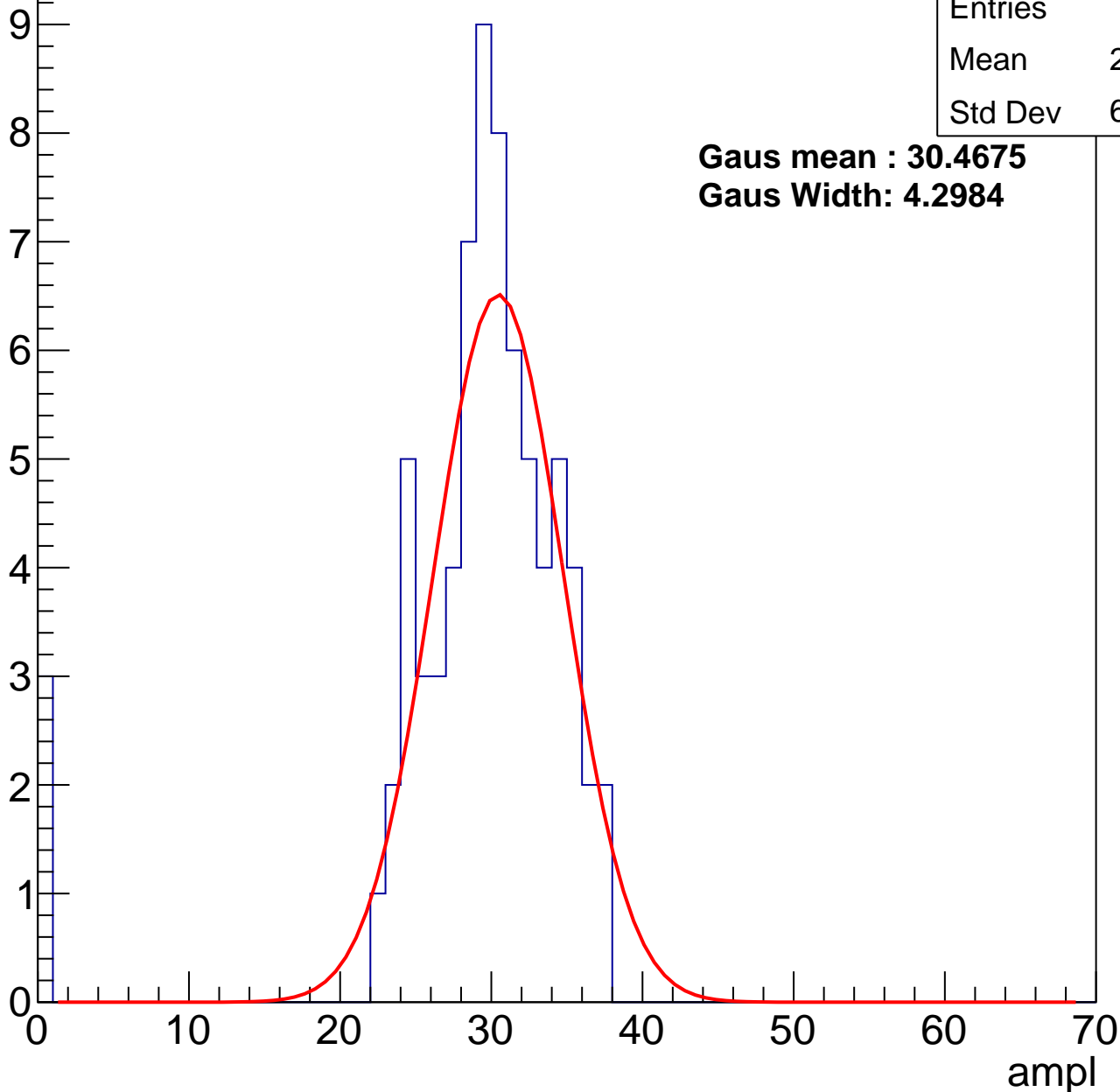
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	73
Mean	28.49
Std Dev	6.909

**Gaus mean : 30.4675**

**Gaus Width: 4.2984**



# B1L003S, U3-ch33, adc1

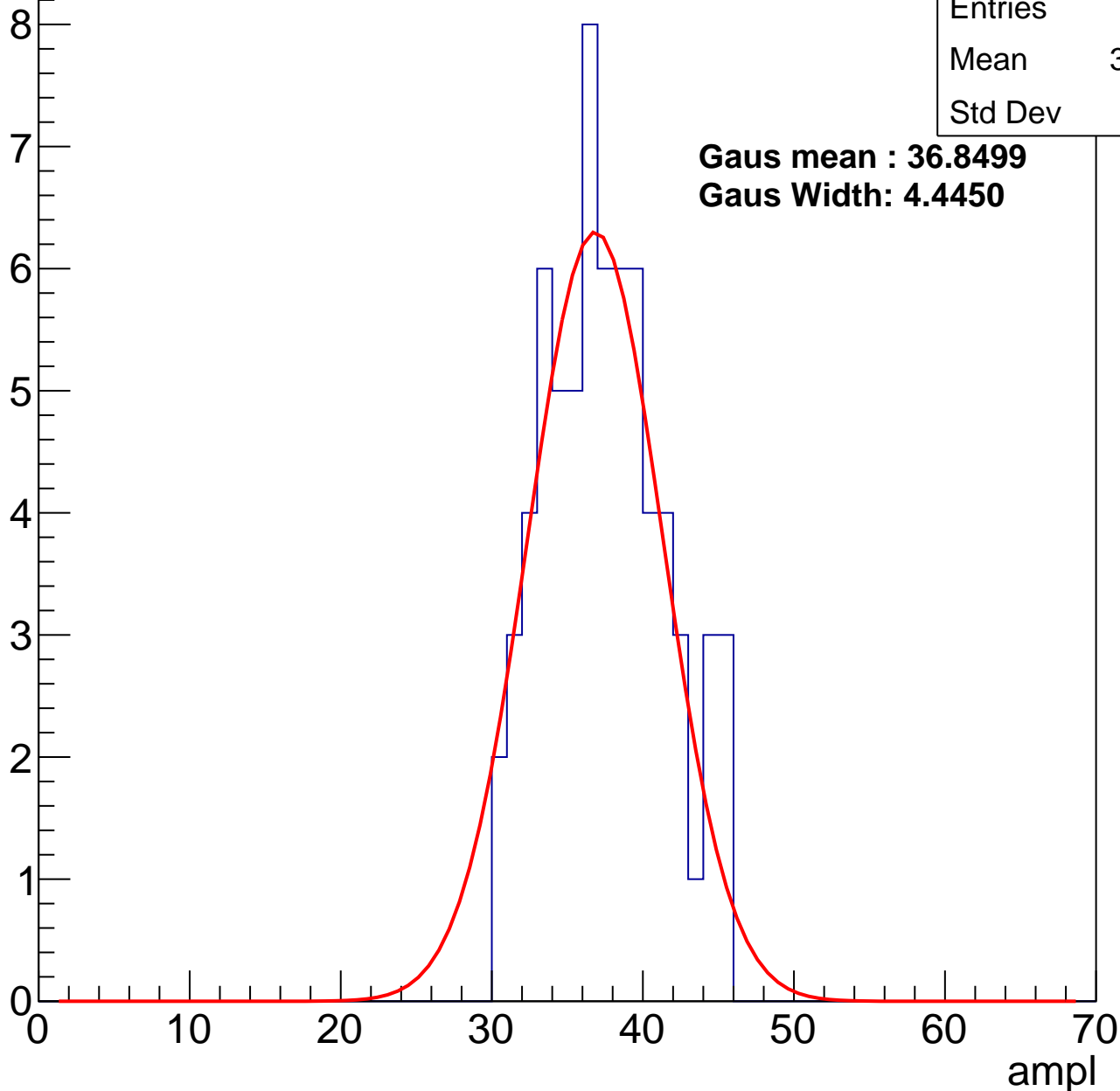
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	37.04
Std Dev	3.91

**Gaus mean : 36.8499**

**Gaus Width: 4.4450**



# B1L003S, U3-ch33, adc2

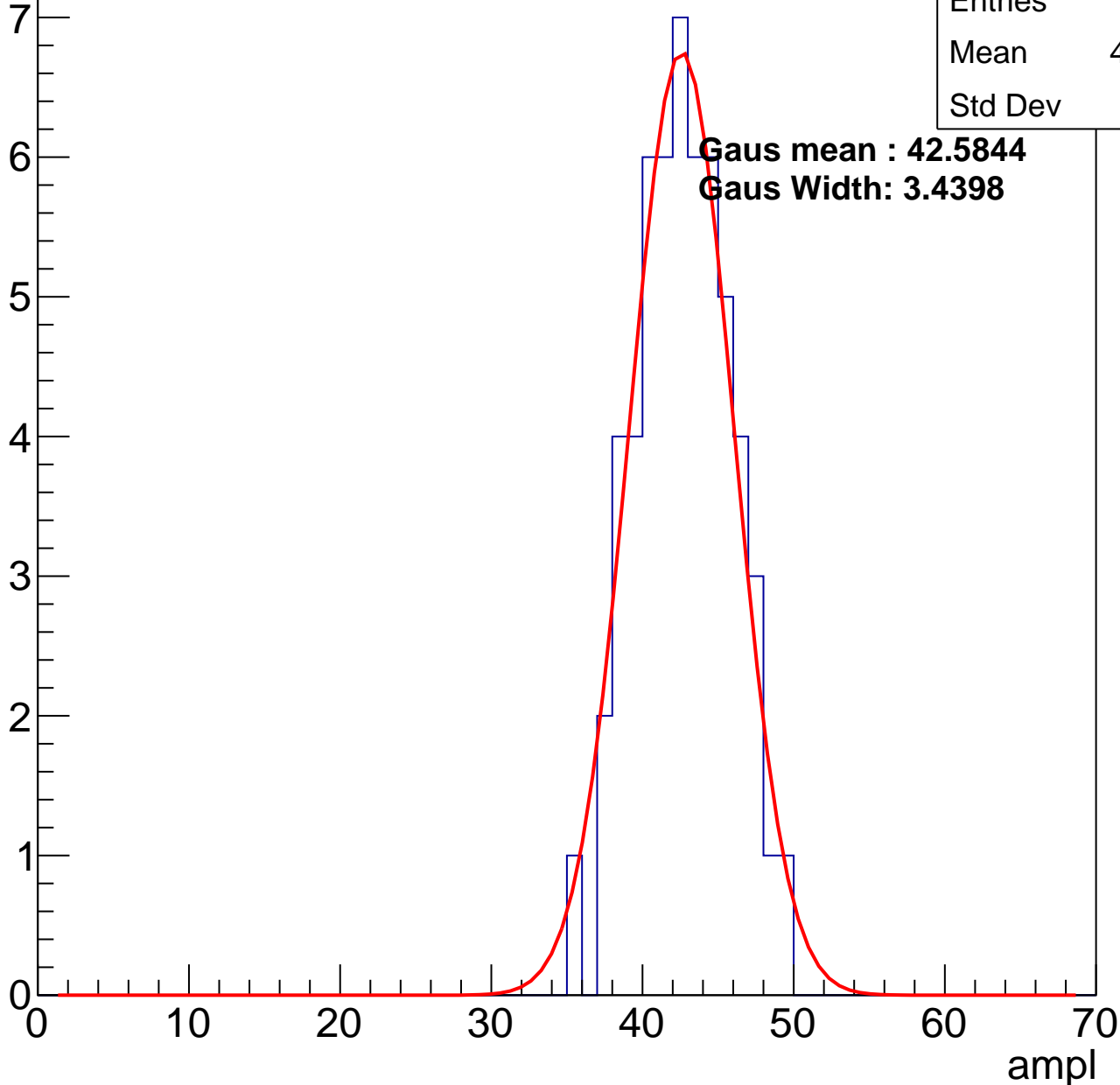
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	42.25
Std Dev	3.06

**Gaus mean : 42.5844**

**Gaus Width: 3.4398**

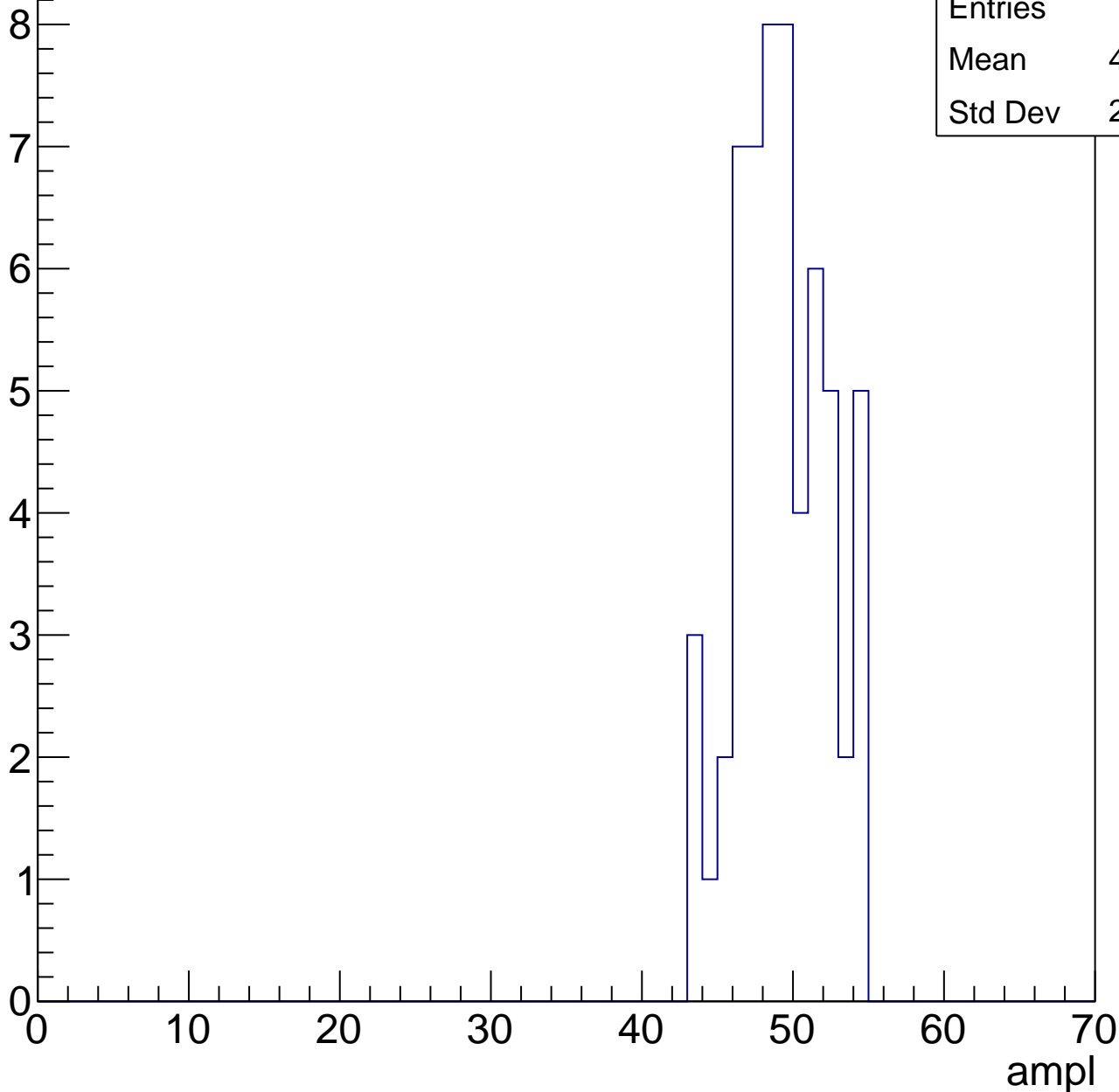


# B1L003S, U3-ch33, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	48.83
Std Dev	2.913

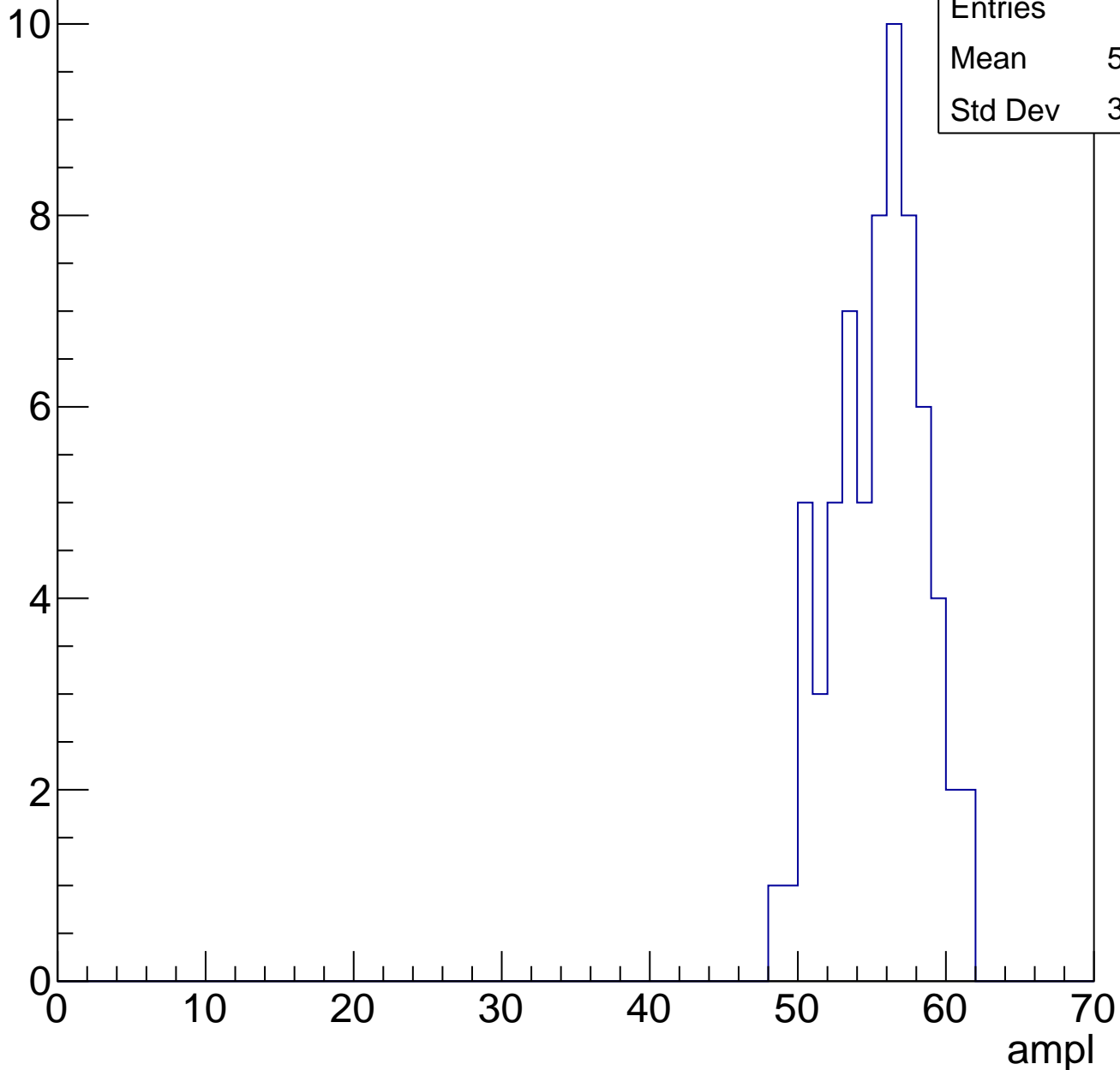


# B1L003S, U3-ch33, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	67
Mean	54.97
Std Dev	3.037

Entry

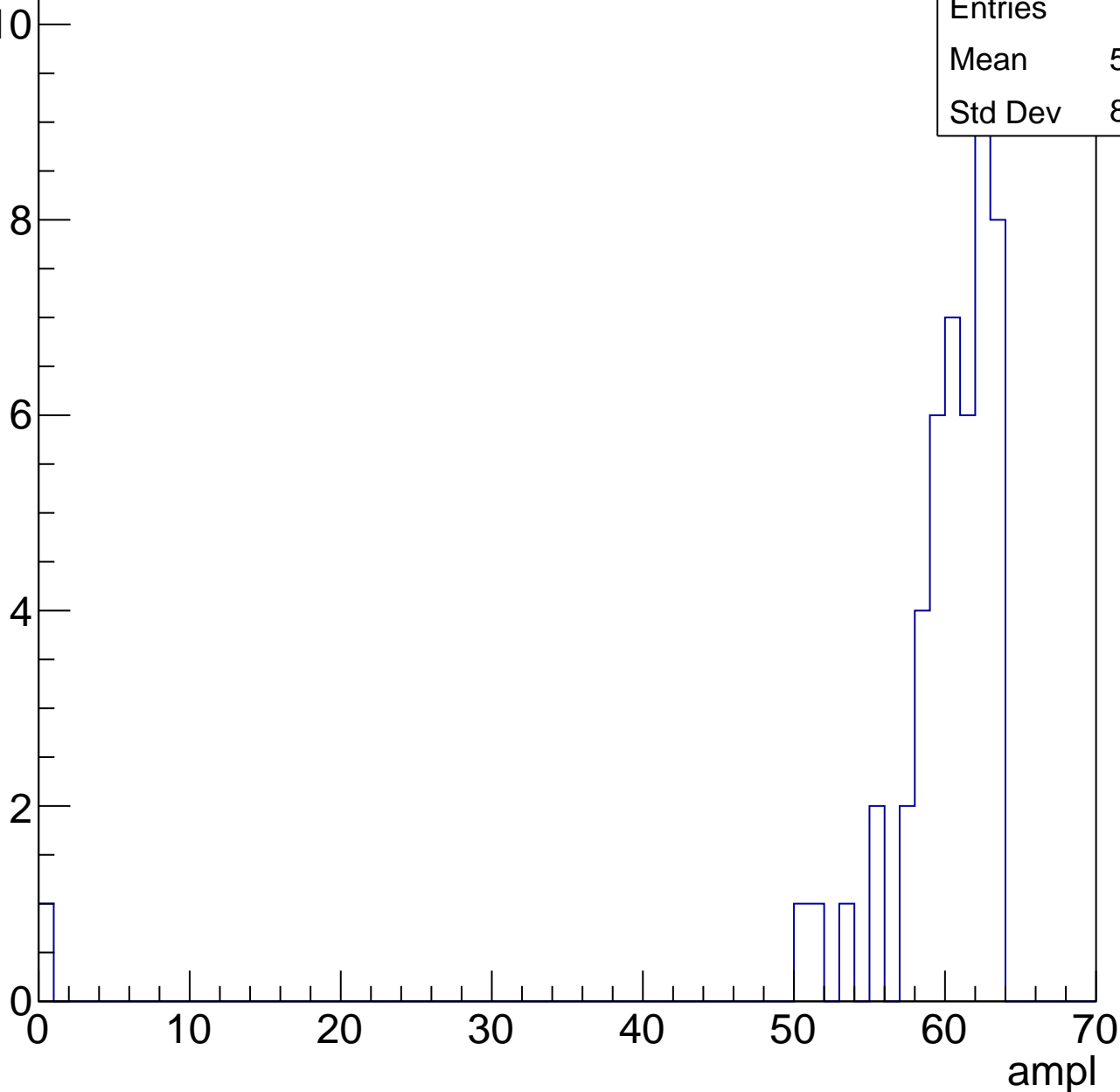


# B1L003S, U3-ch33, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	49
Mean	58.65
Std Dev	8.977



# B1L003S, U3-ch33, adc6

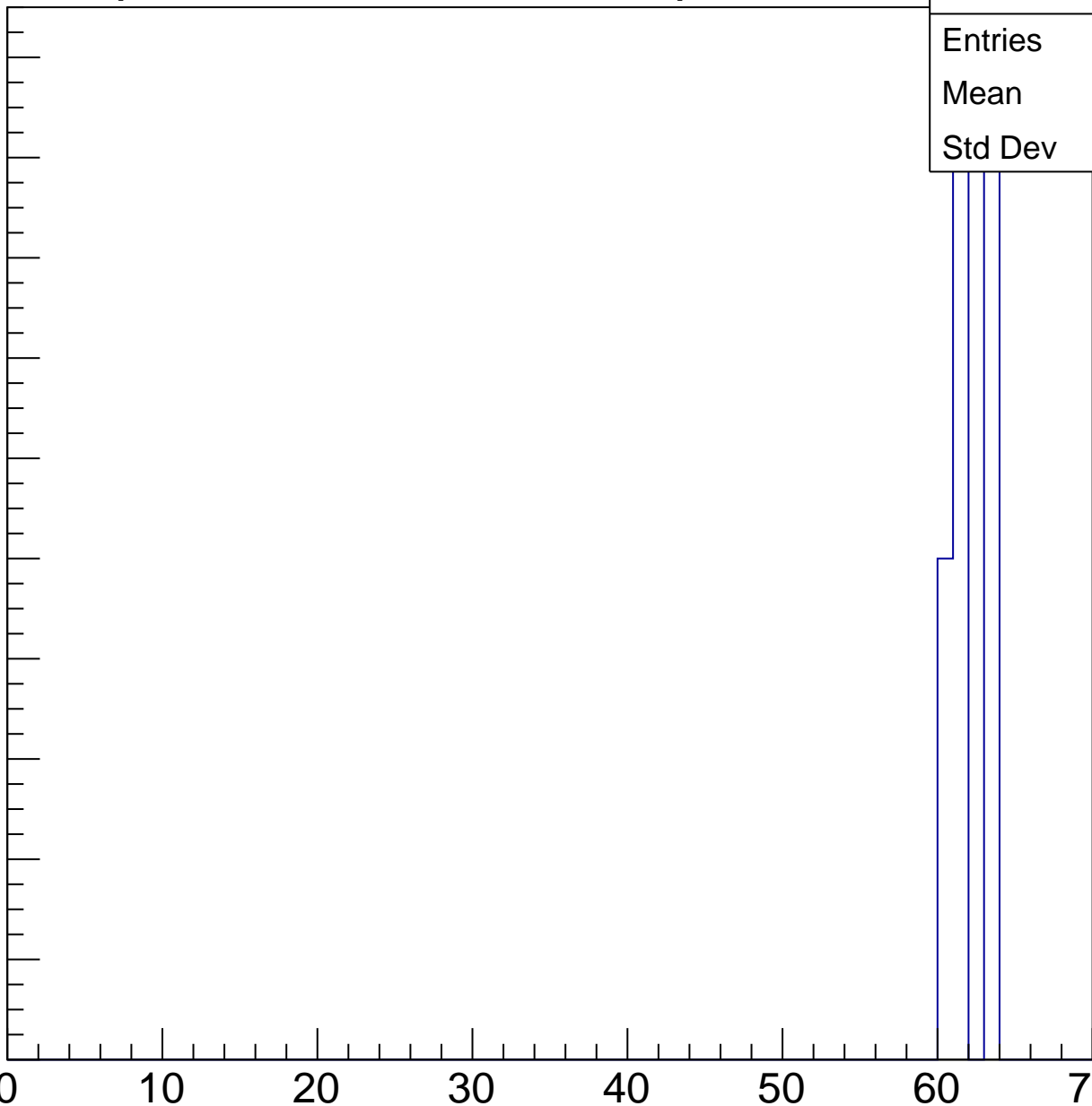
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	61.6
Std Dev	1.2

ampl





# B1L003S, U3-ch33, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U3-ch34, adc0

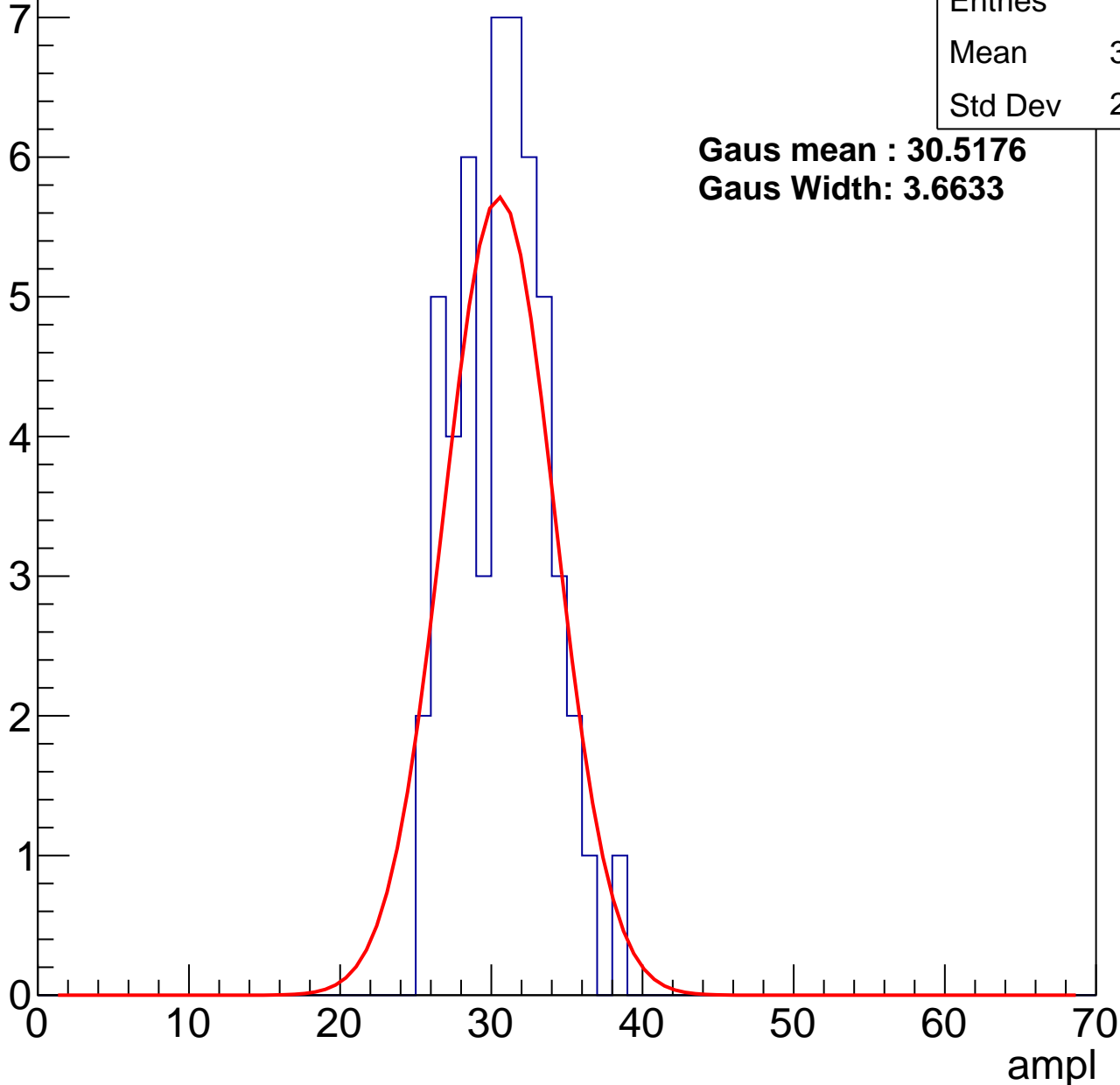
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	52
Mean	30.25
Std Dev	2.986

**Gaus mean : 30.5176**

**Gaus Width: 3.6633**



# B1L003S, U3-ch34, adc1

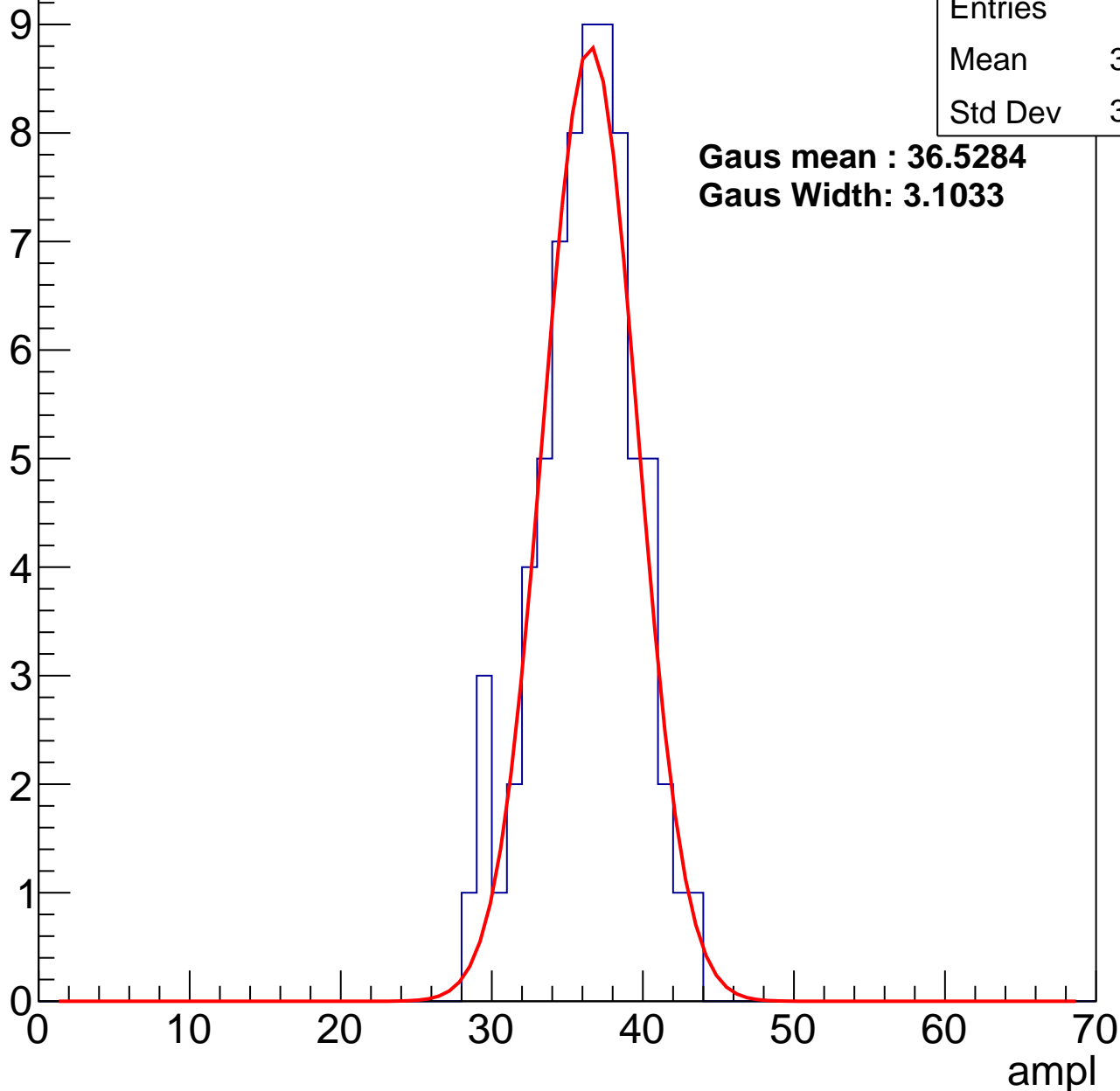
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	71
Mean	35.79
Std Dev	3.228

**Gaus mean : 36.5284**

**Gaus Width: 3.1033**



# B1L003S, U3-ch34, adc2

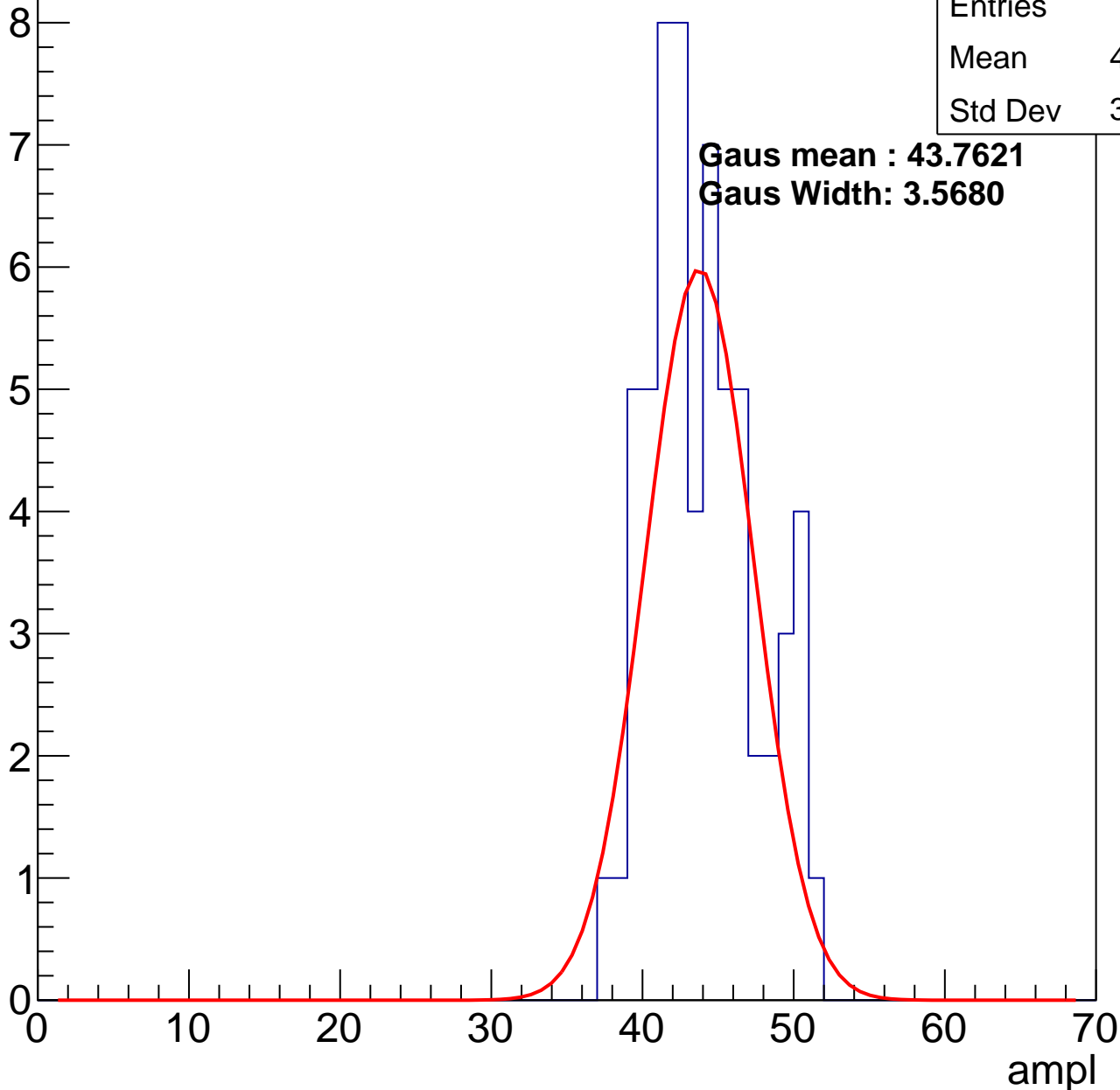
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	43.56
Std Dev	3.457

**Gaus mean : 43.7621**

**Gaus Width: 3.5680**

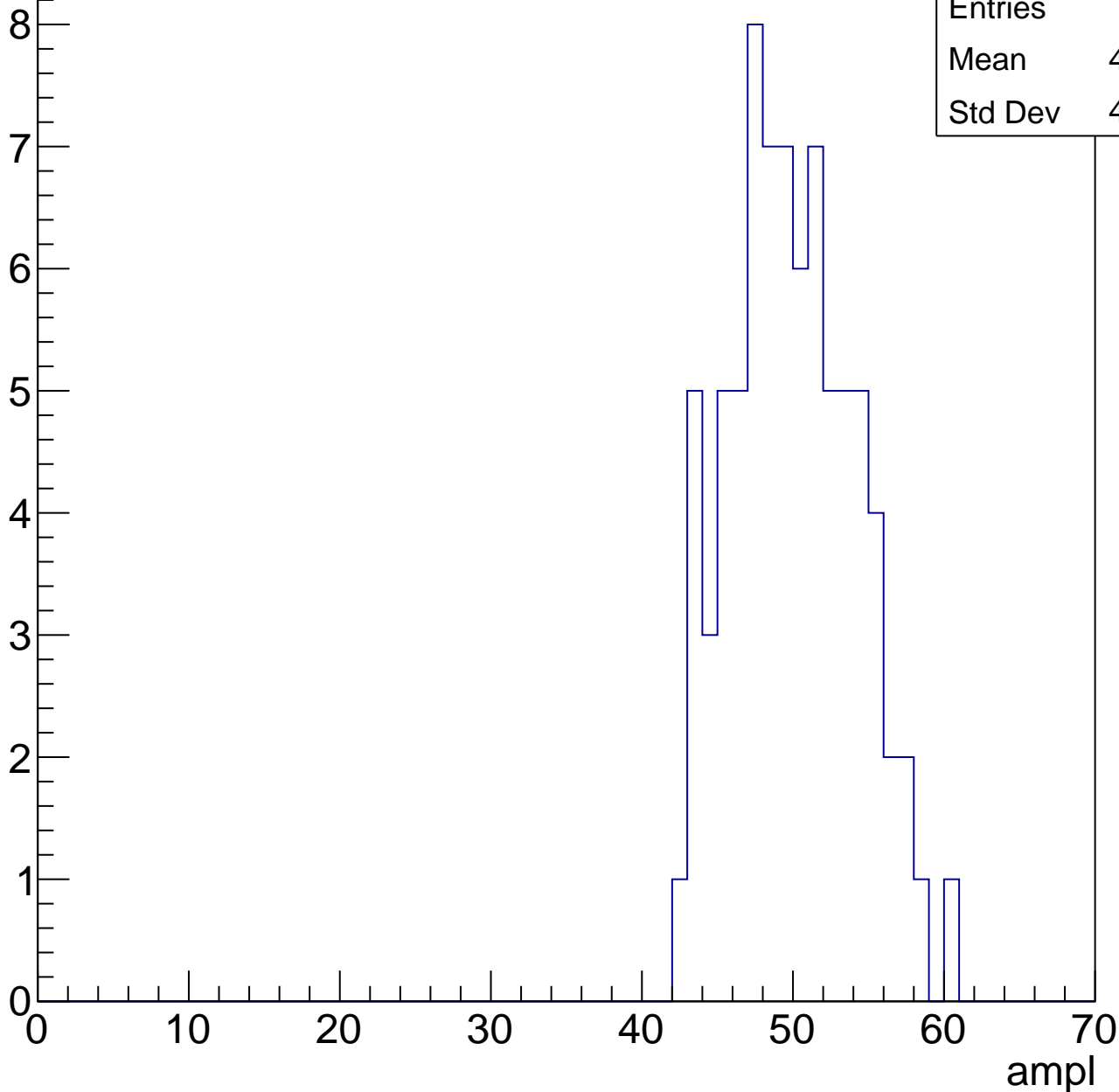


# B1L003S, U3-ch34, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	79
Mean	49.56
Std Dev	4.056

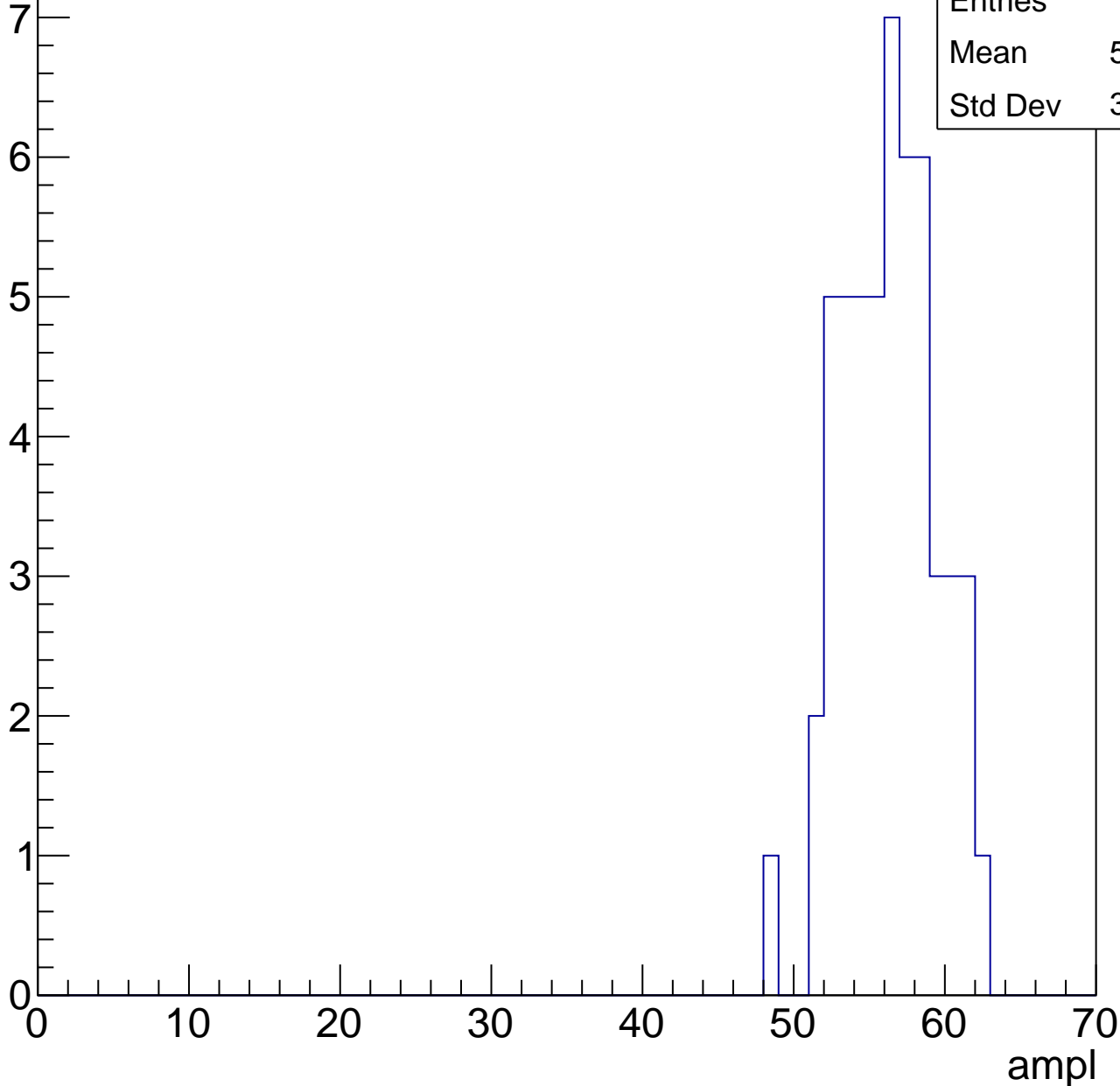


# B1L003S, U3-ch34, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	52
Mean	55.85
Std Dev	3.034



# B1L003S, U3-ch34, adc5

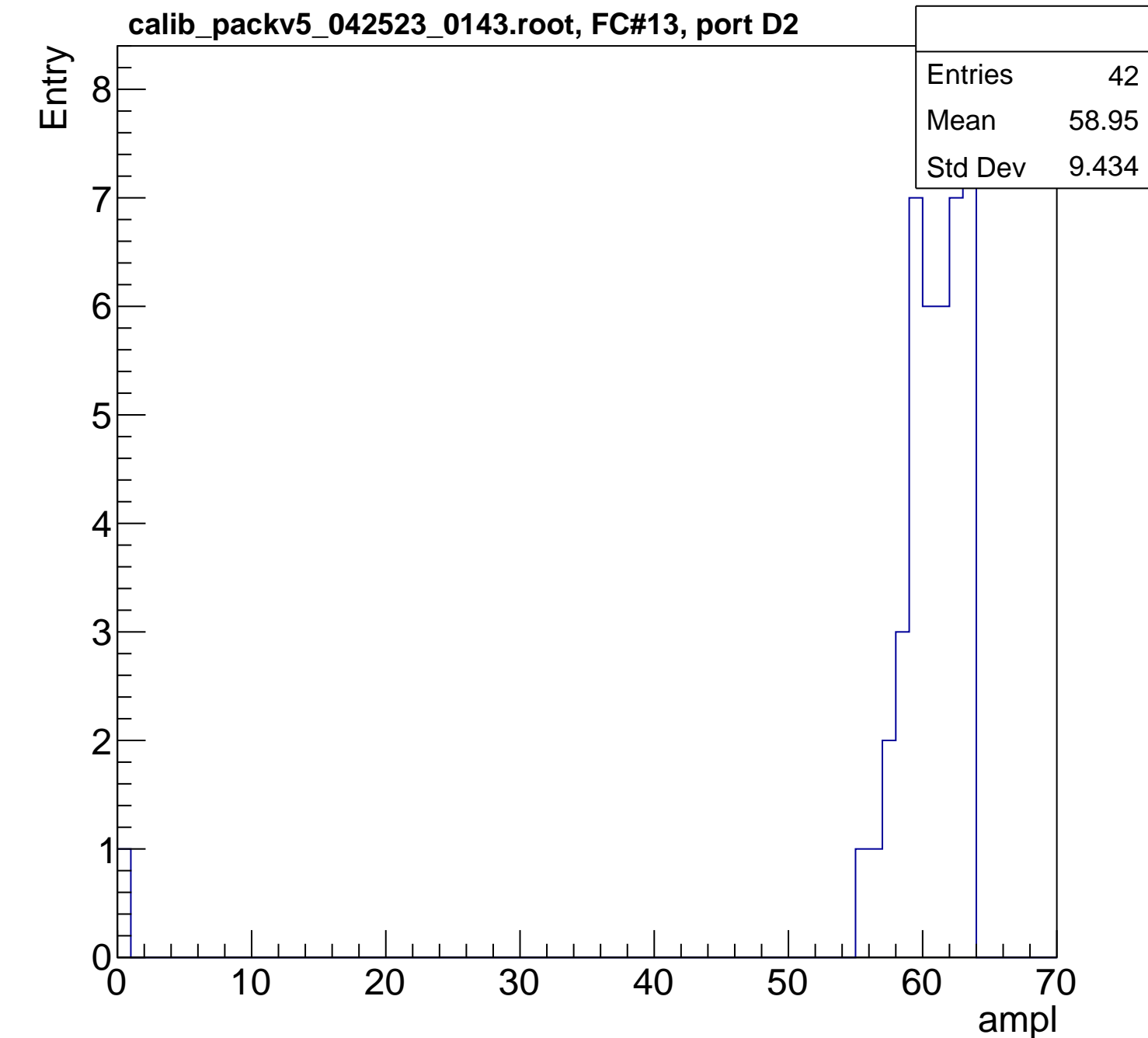
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	42
Mean	58.95
Std Dev	9.434

ampl



# B1L003S, U3-ch34, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

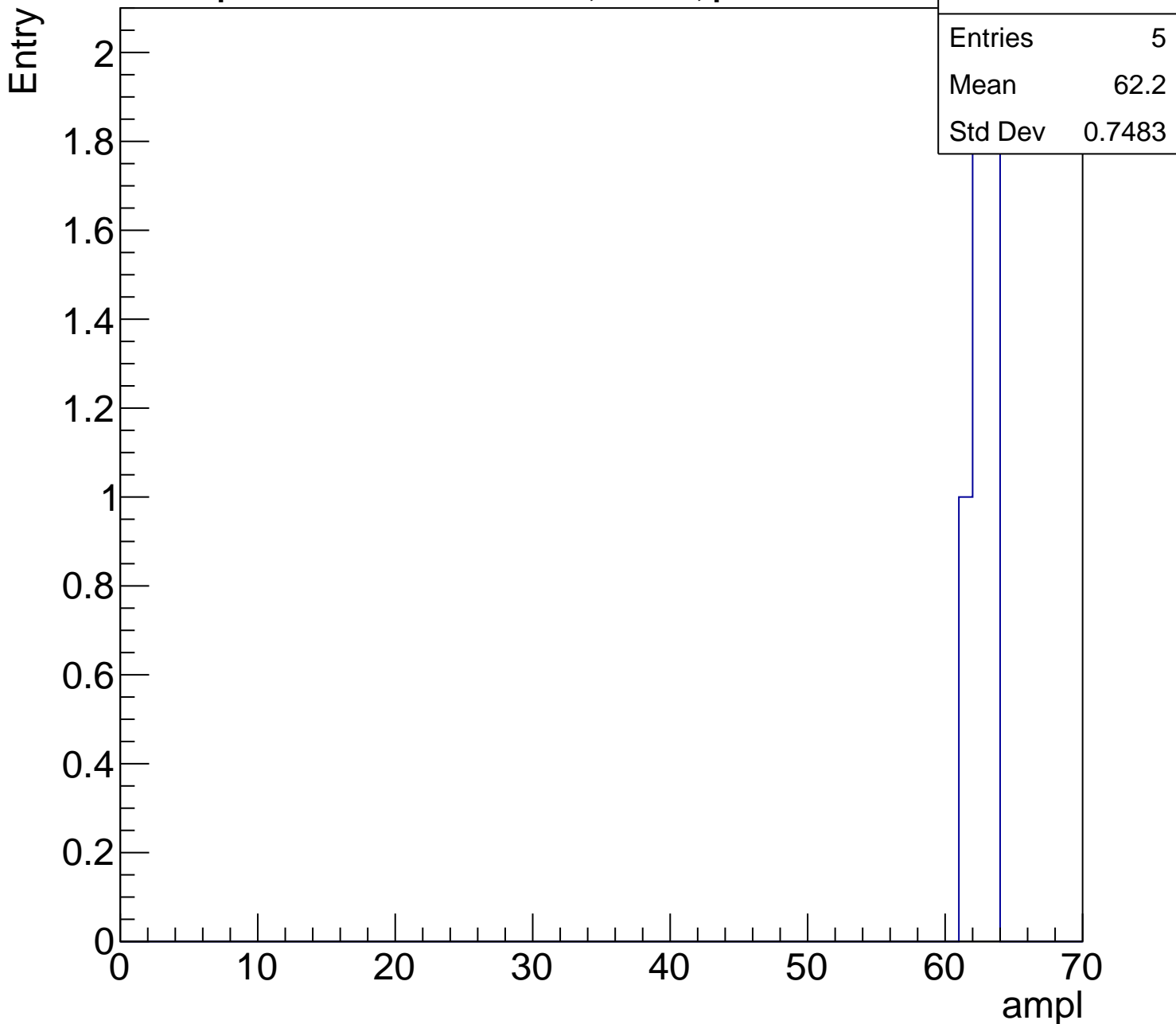
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	62.2
Std Dev	0.7483

0 10 20 30 40 50 60 70

ampl





# B1L003S, U3-ch34, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U3-ch35, adc0

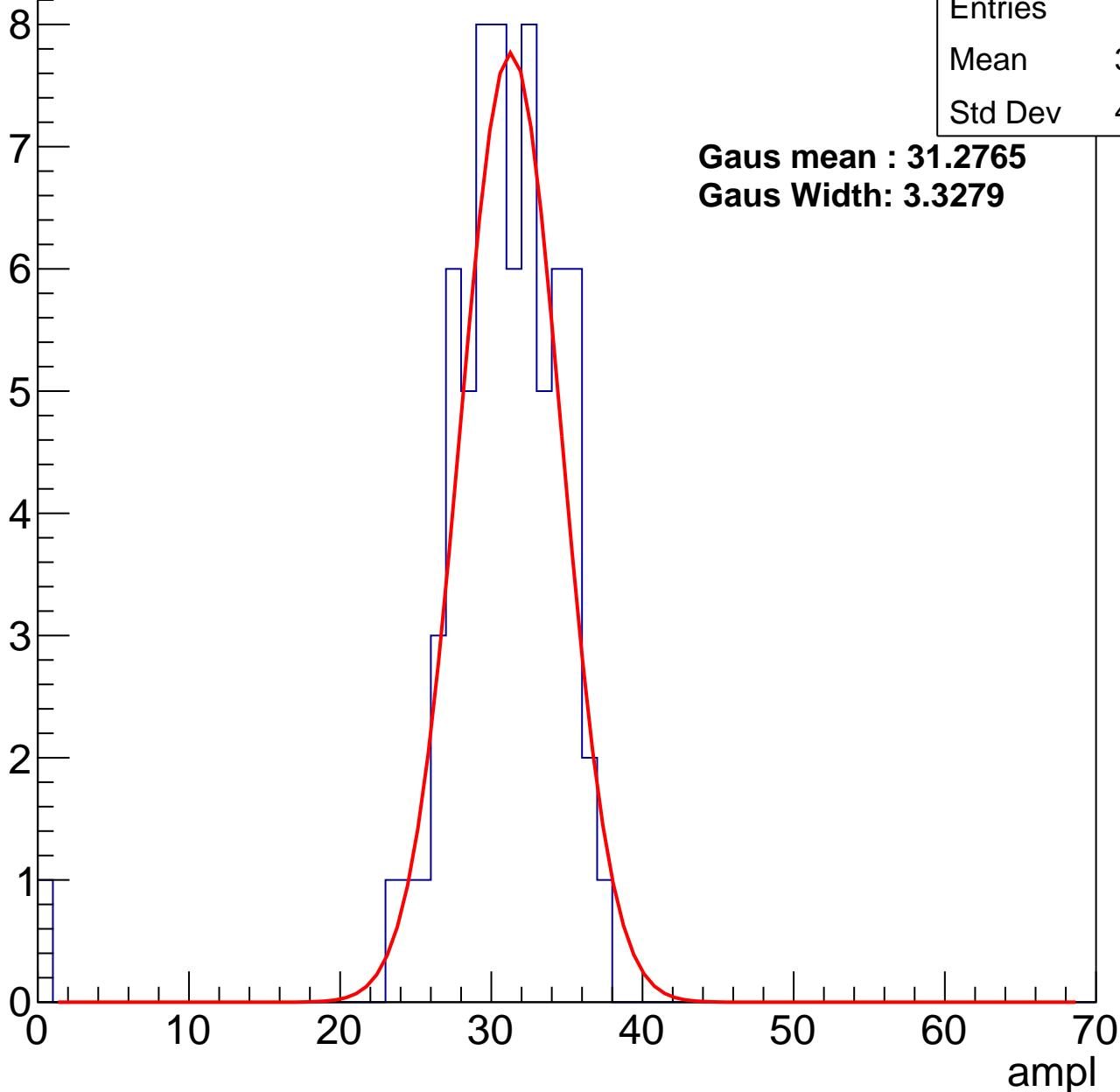
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	30.21
Std Dev	4.831

**Gaus mean : 31.2765**

**Gaus Width: 3.3279**



# B1L003S, U3-ch35, adc1

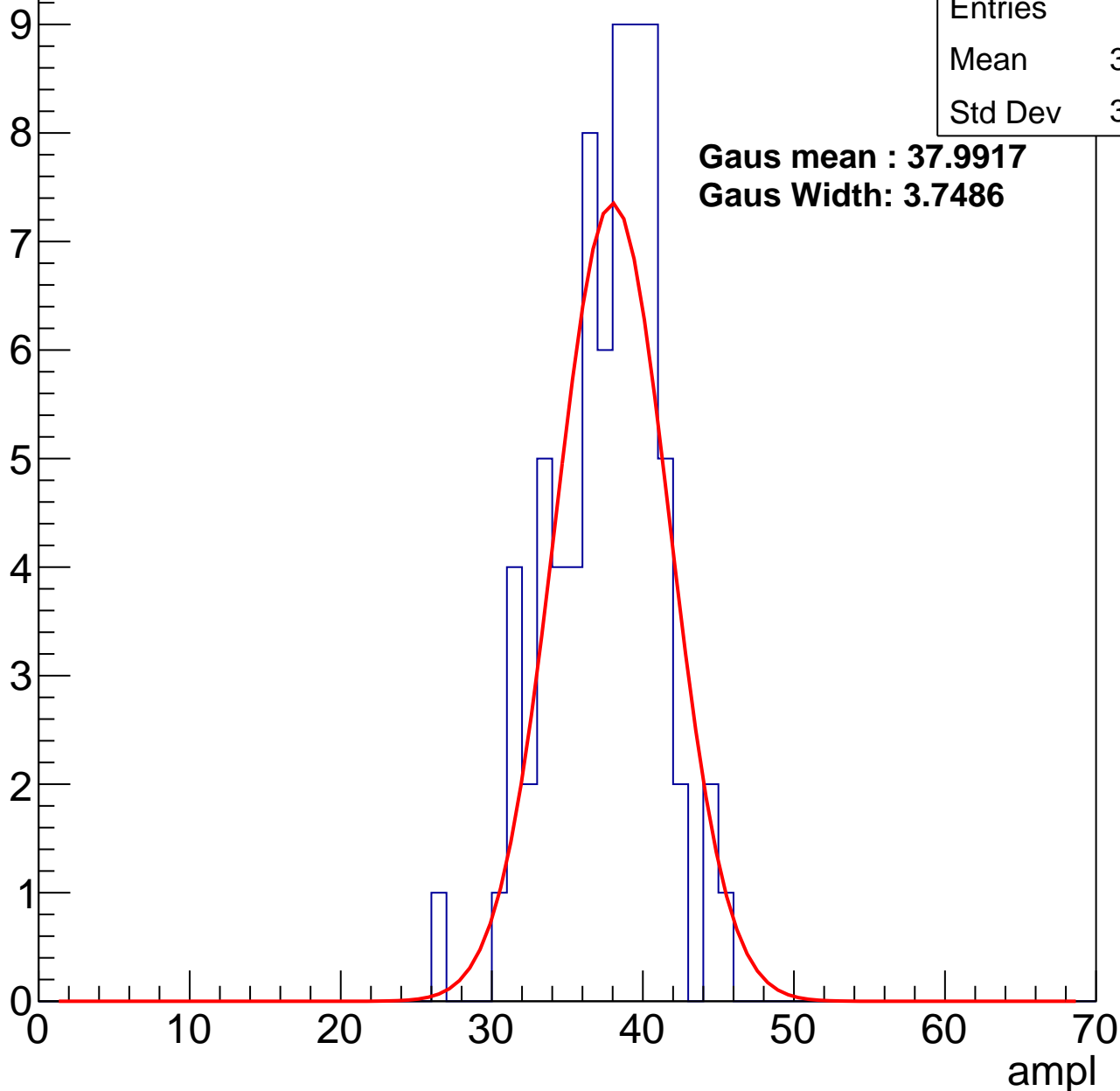
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	72
Mean	37.08
Std Dev	3.578

**Gaus mean : 37.9917**

**Gaus Width: 3.7486**



# B1L003S, U3-ch35, adc2

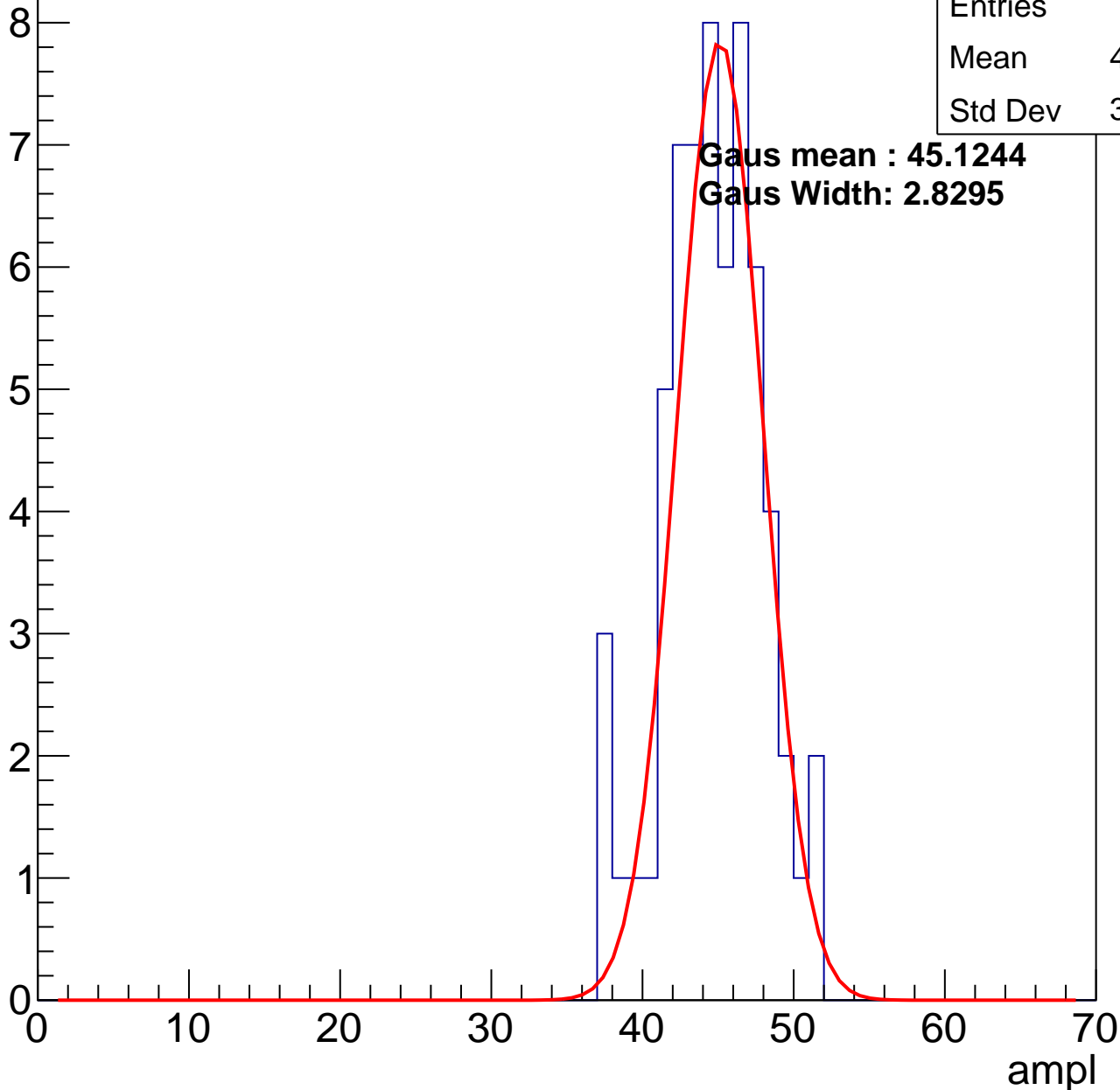
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	44.23
Std Dev	3.215

**Gaus mean : 45.1244**

**Gaus Width: 2.8295**

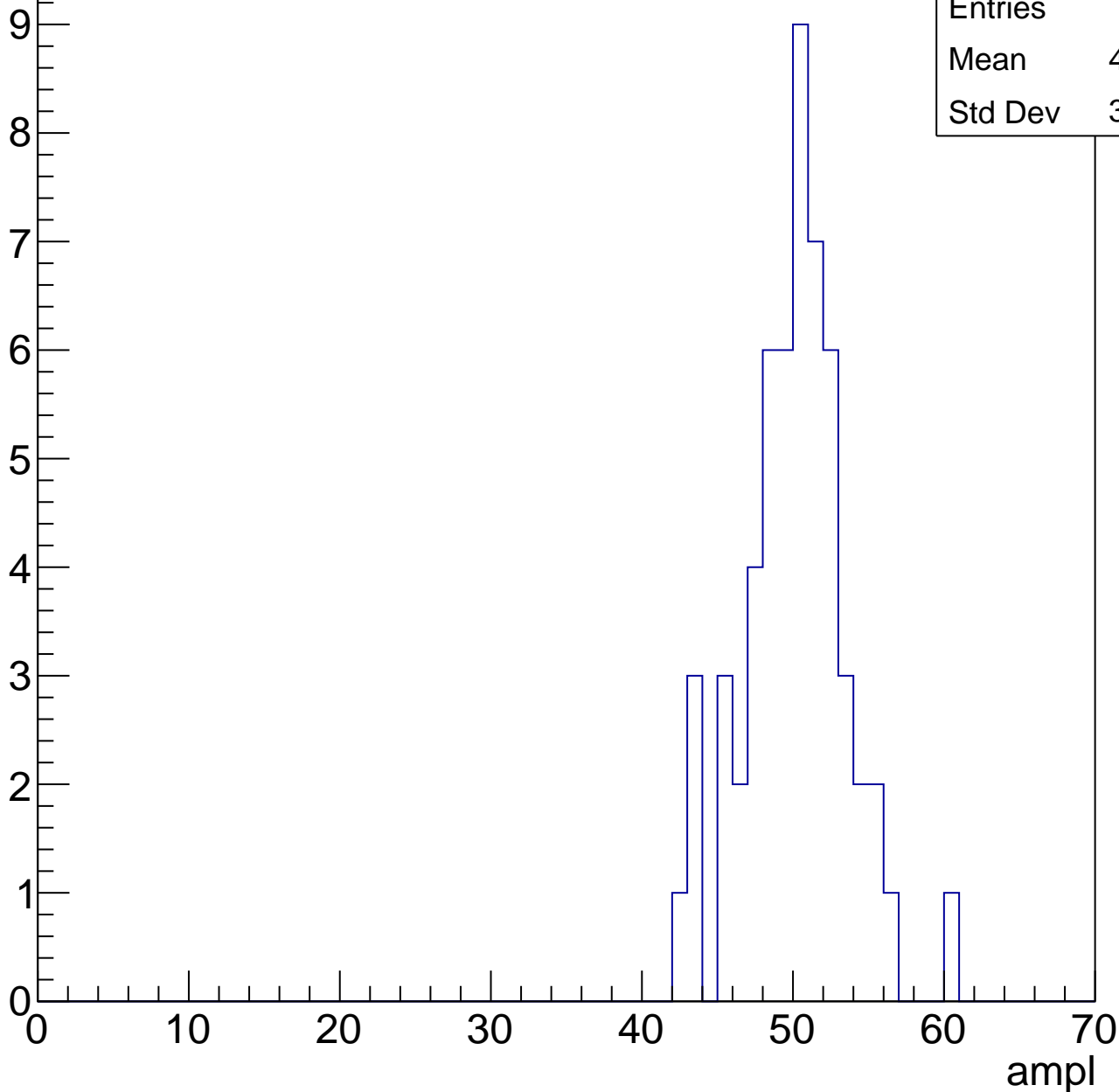


# B1L003S, U3-ch35, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	49.64
Std Dev	3.414

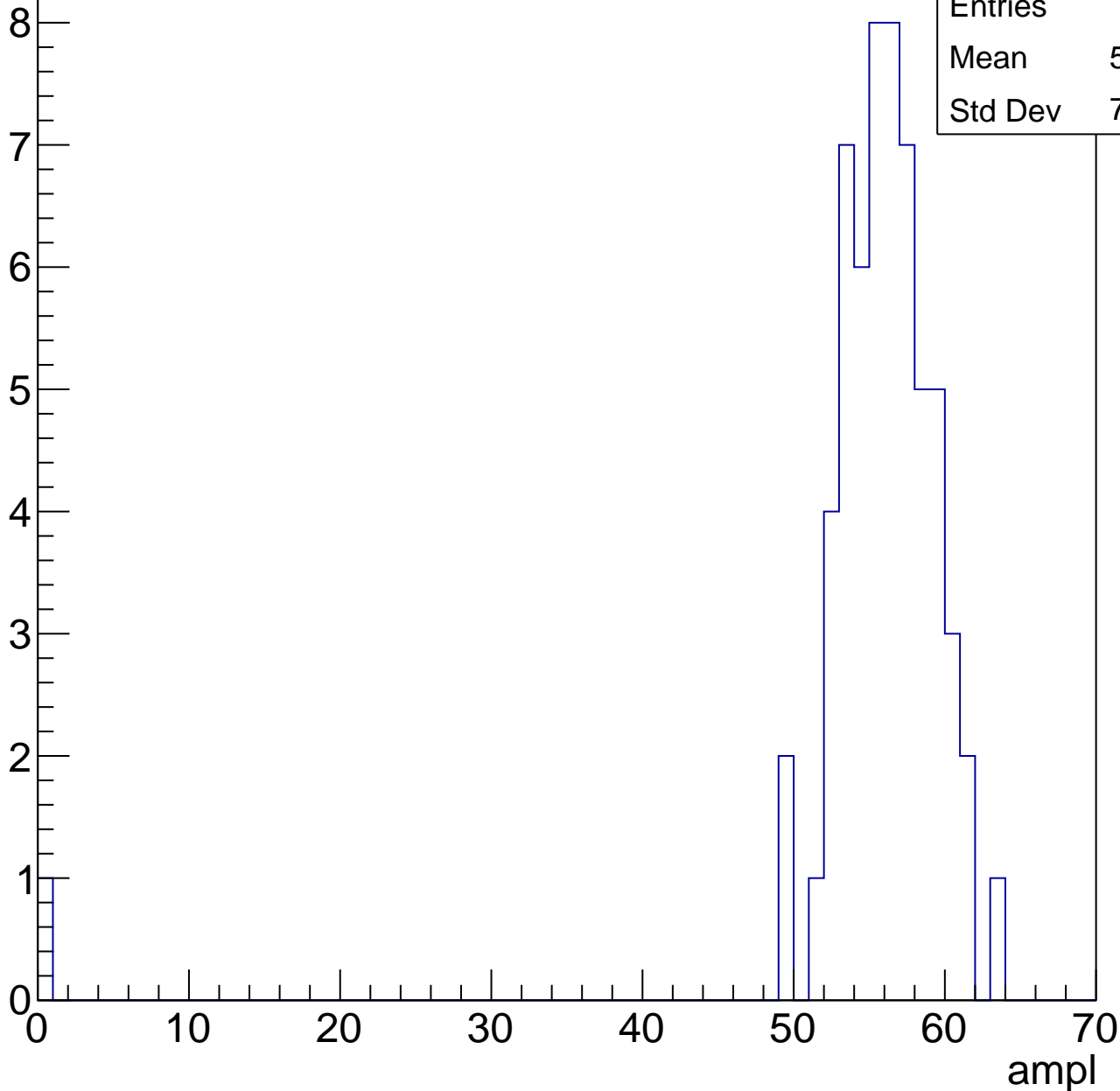


# B1L003S, U3-ch35, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	54.82
Std Dev	7.695

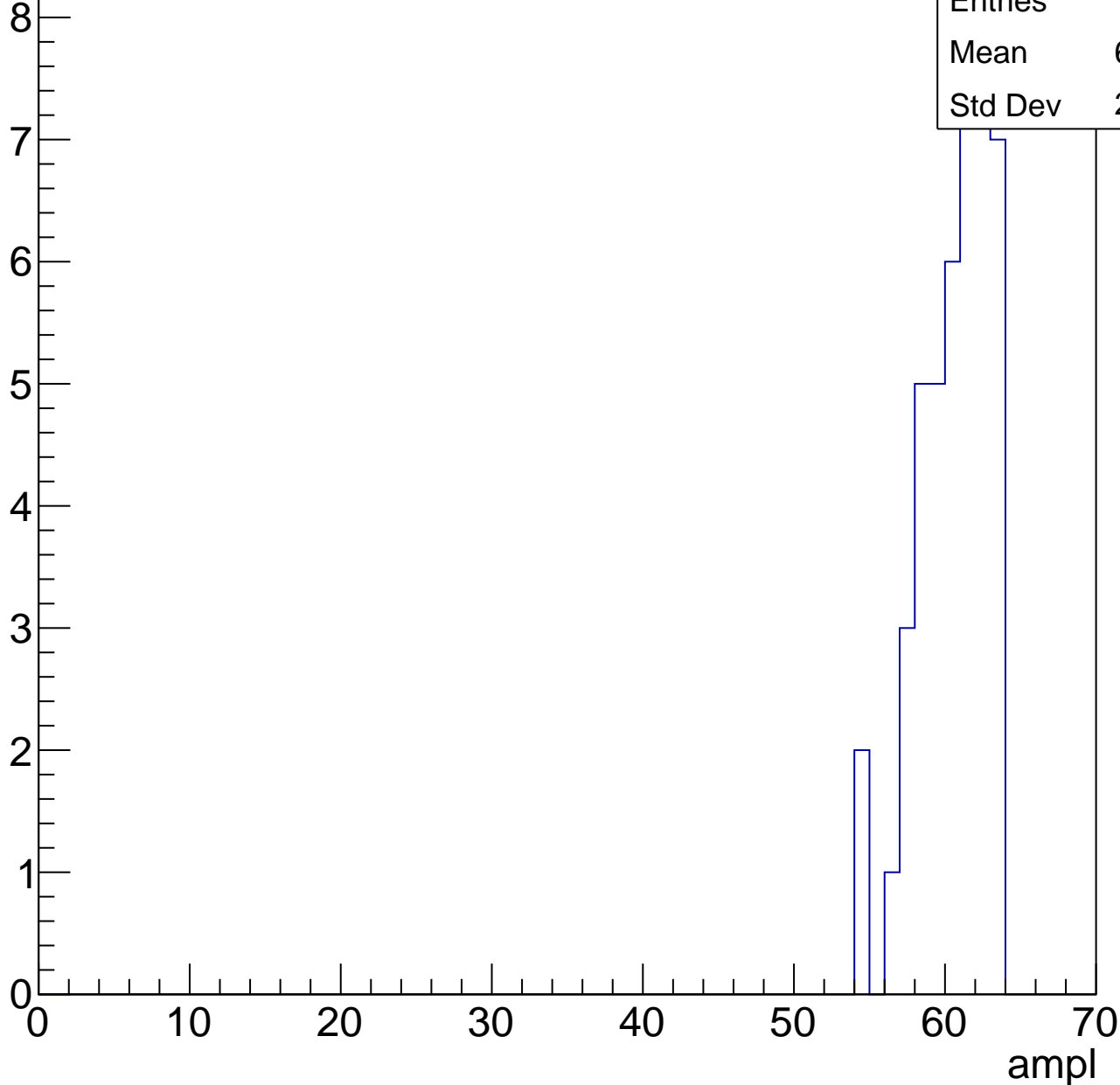


# B1L003S, U3-ch35, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	45
Mean	60.11
Std Dev	2.321



# B1L003S, U3-ch35, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch35, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U3-ch36, adc0

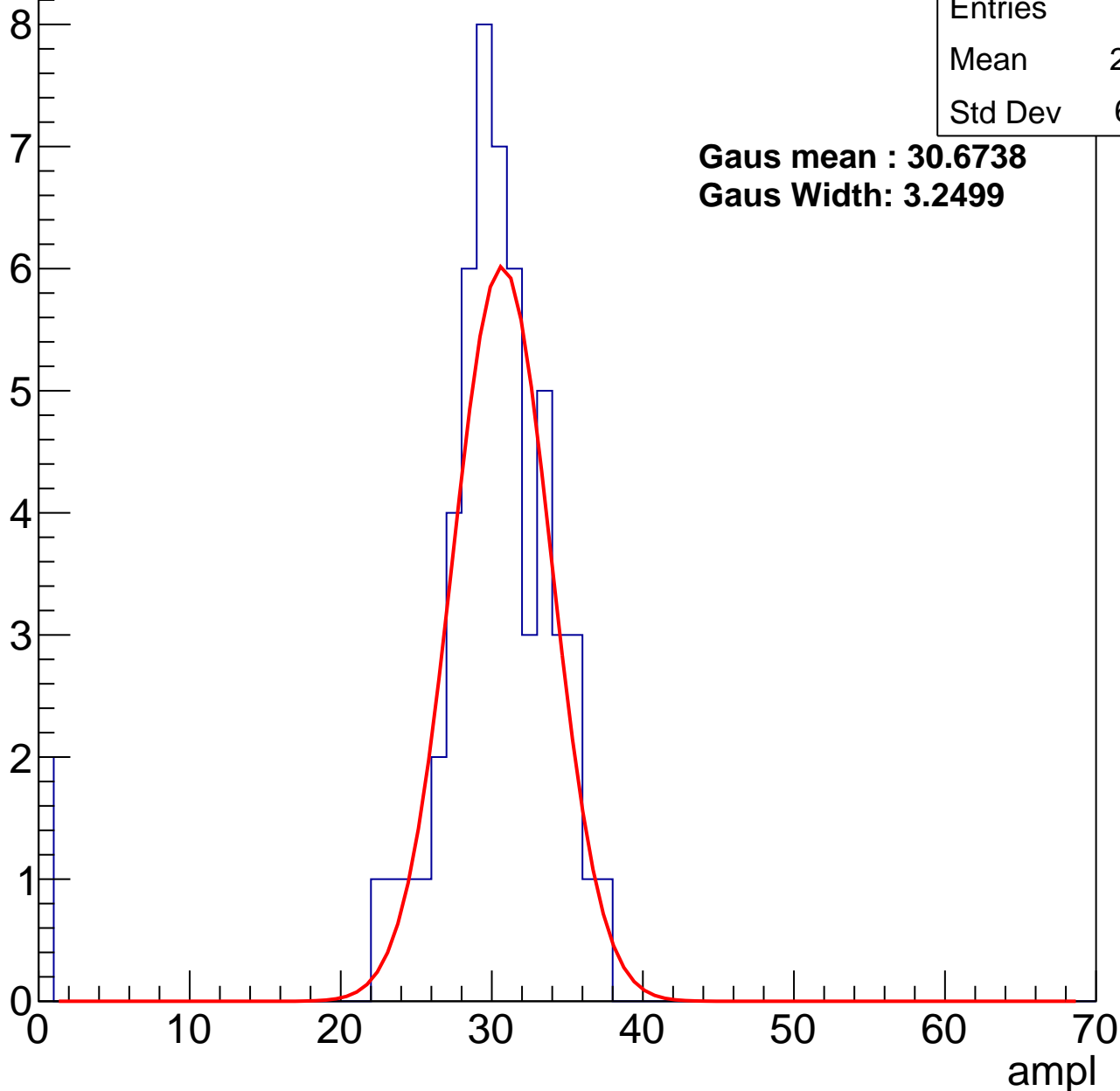
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	28.93
Std Dev	6.441

**Gaus mean : 30.6738**

**Gaus Width: 3.2499**



# B1L003S, U3-ch36, adc1

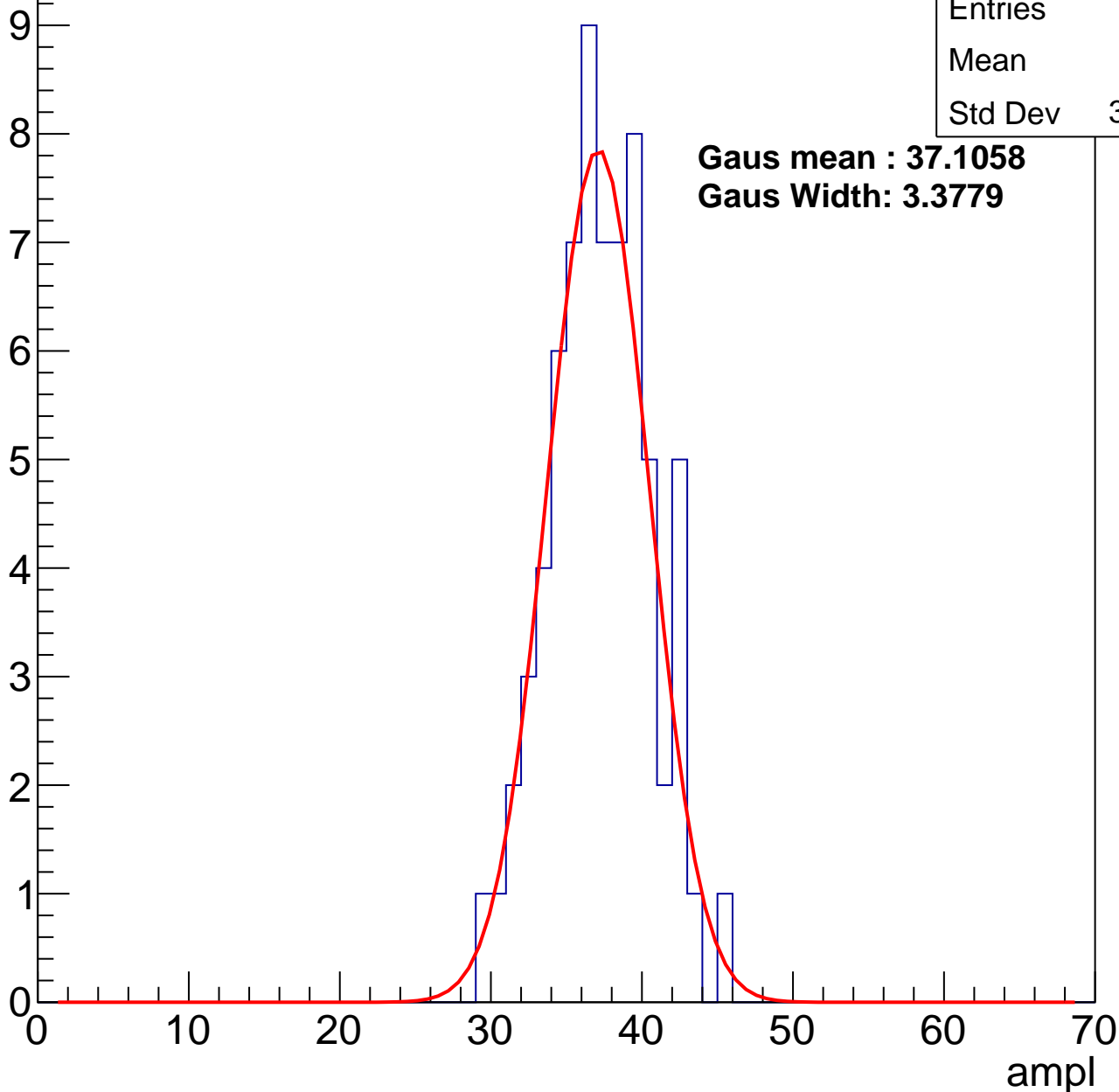
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	36.8
Std Dev	3.304

**Gaus mean : 37.1058**

**Gaus Width: 3.3779**



# B1L003S, U3-ch36, adc2

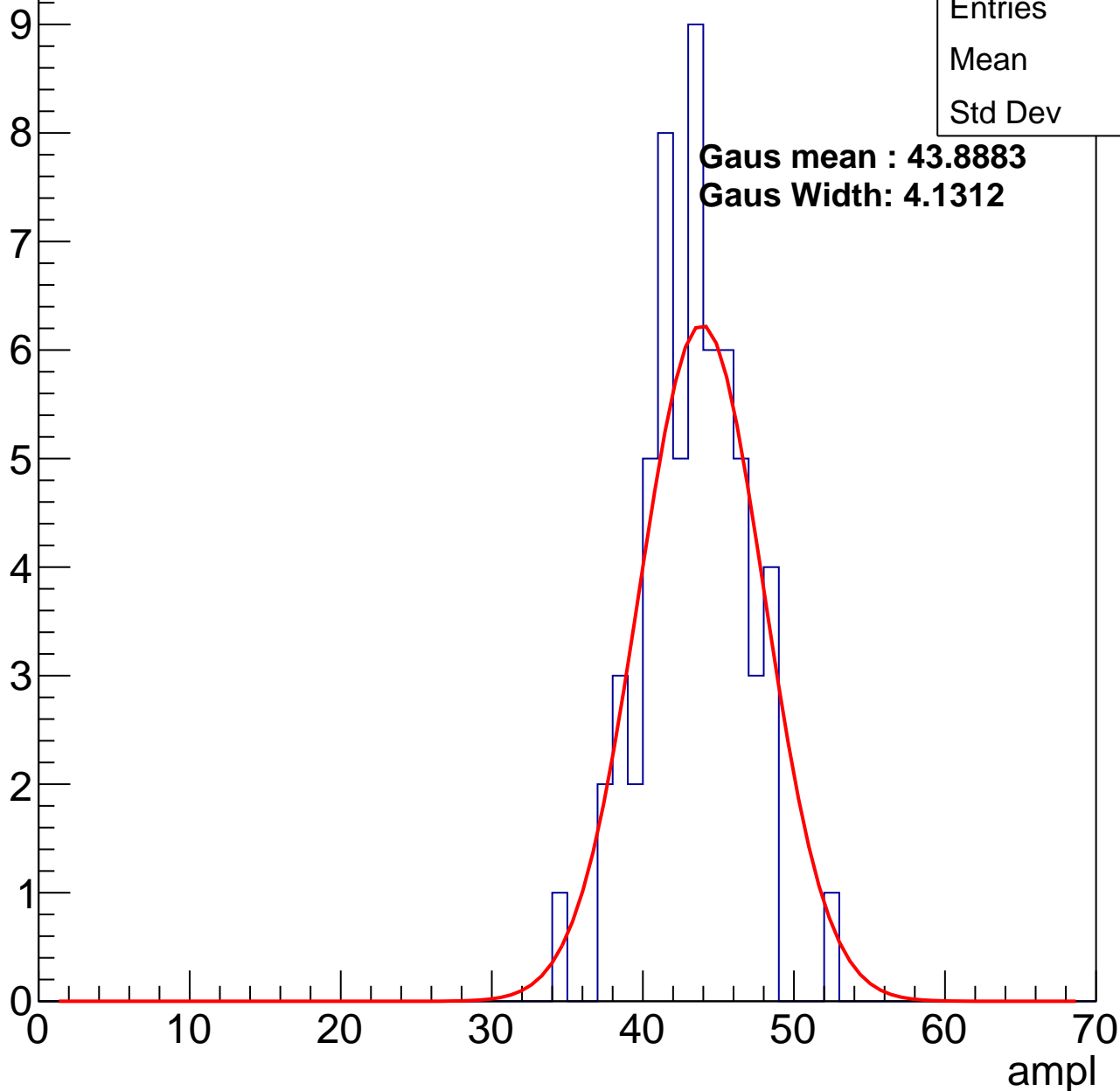
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	42.9
Std Dev	3.28

**Gaus mean : 43.8883**

**Gaus Width: 4.1312**

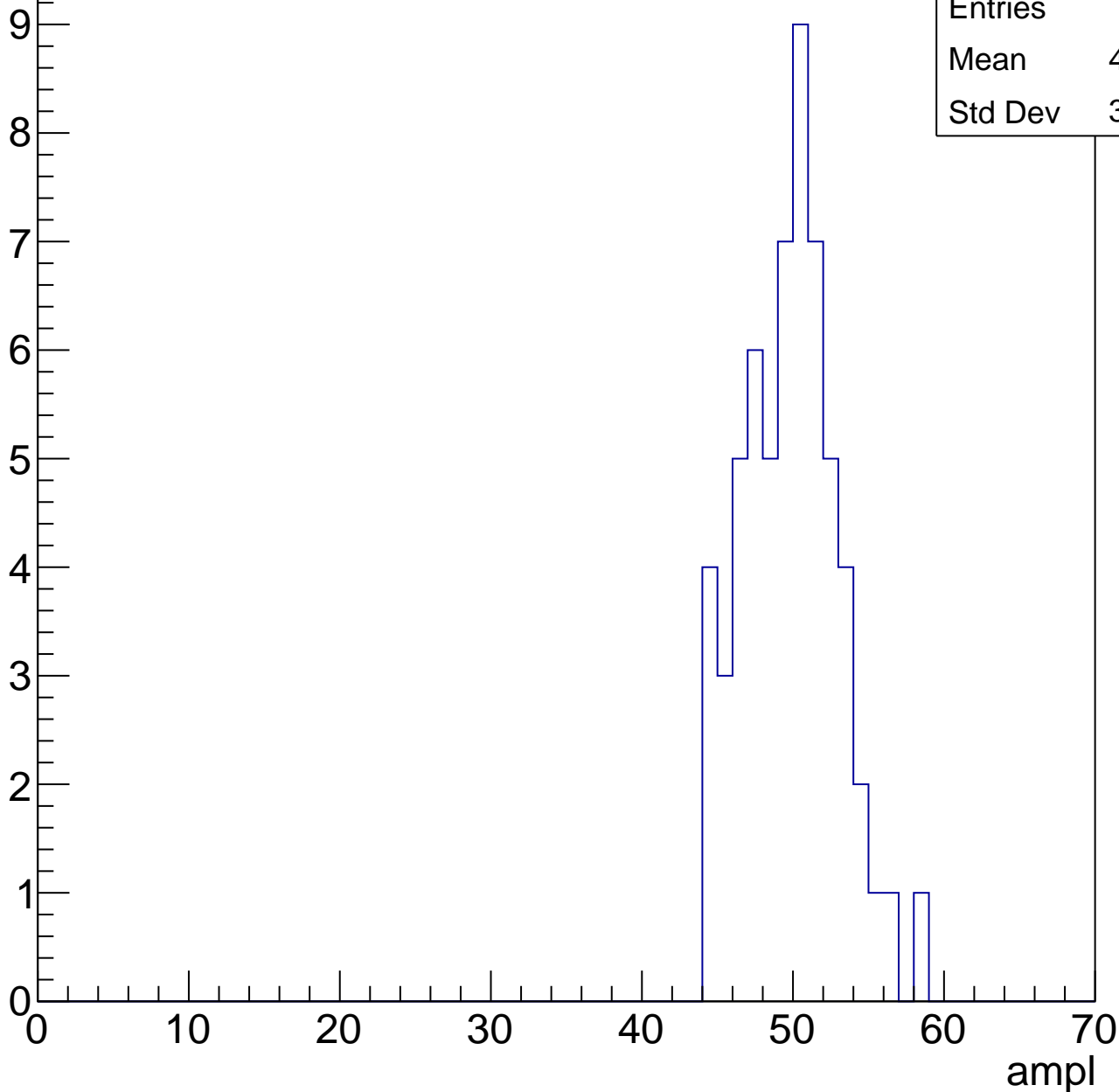


# B1L003S, U3-ch36, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	49.37
Std Dev	3.098

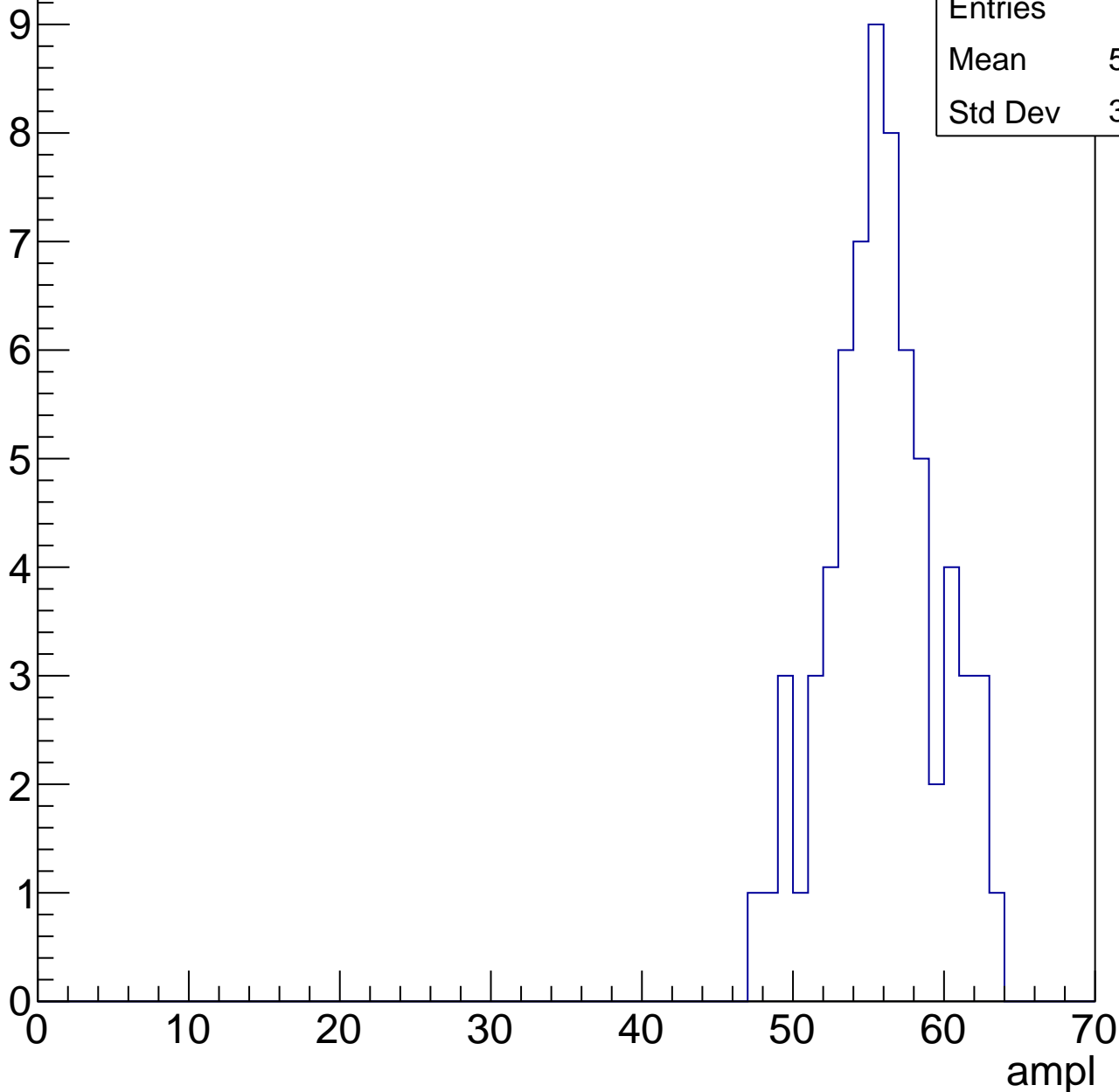


# B1L003S, U3-ch36, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	55.43
Std Dev	3.617



# B1L003S, U3-ch36, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	40
Mean	60.08
Std Dev	2.317

ampl

0 10 20 30 40 50 60 70

0

1

2

3

4

5

6

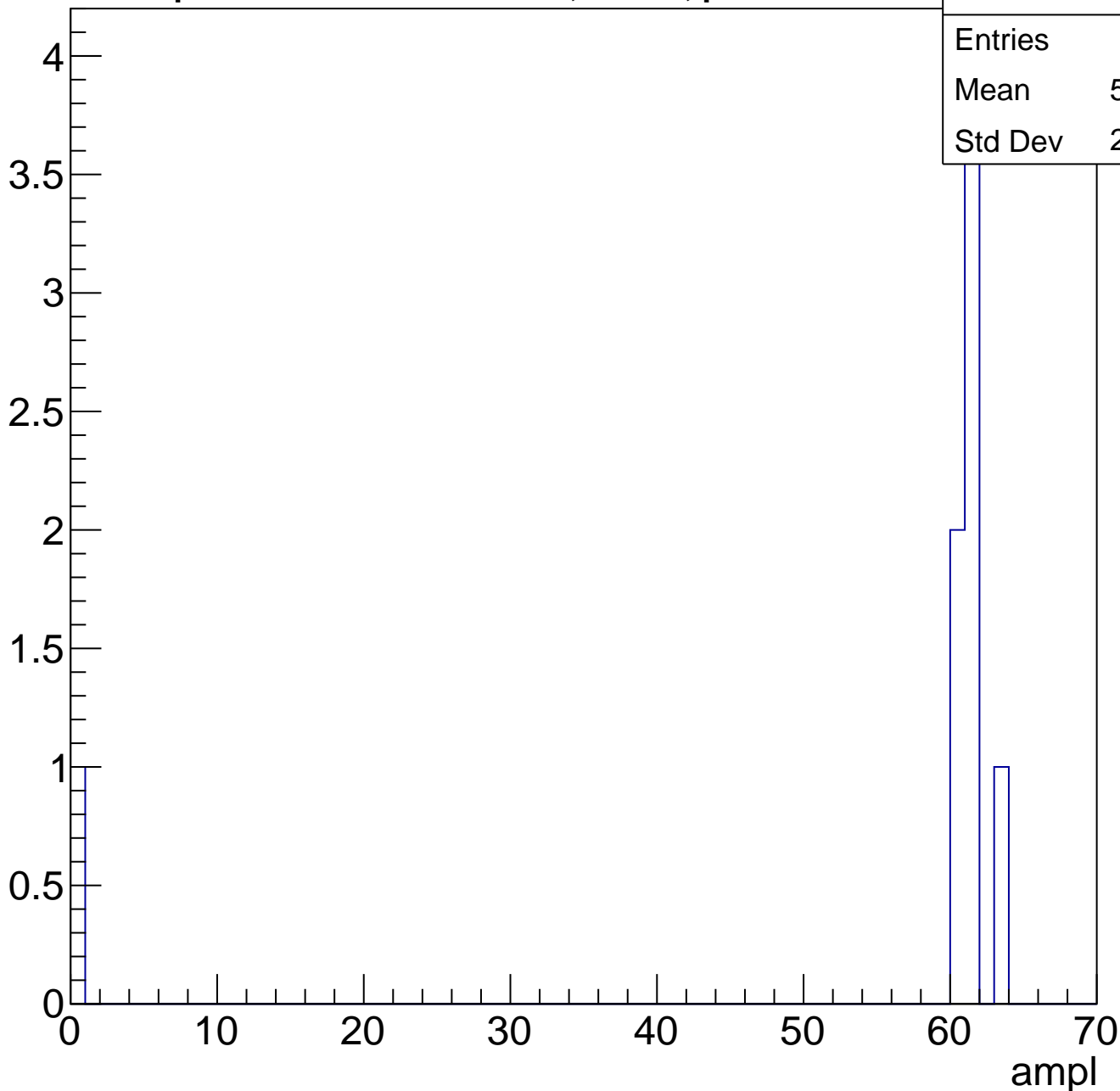
7

8

# B1L003S, U3-ch36, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	8
Mean	53.38
Std Dev	20.19



# B1L003S, U3-ch36, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U3-ch37, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	76
Mean	28.33
Std Dev	5.634

**Gaus mean : 29.1156**

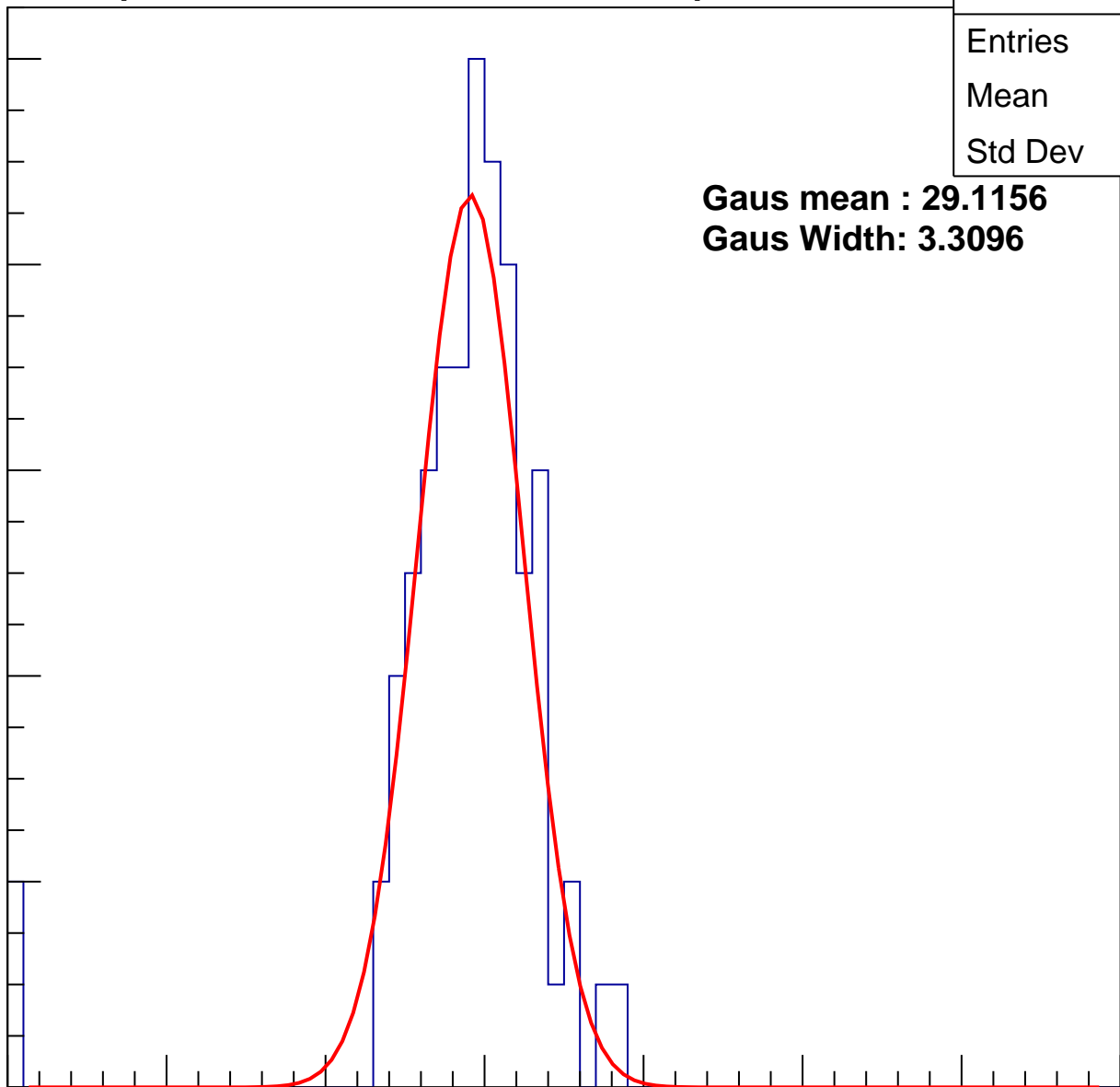
**Gaus Width: 3.3096**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U3-ch37, adc1

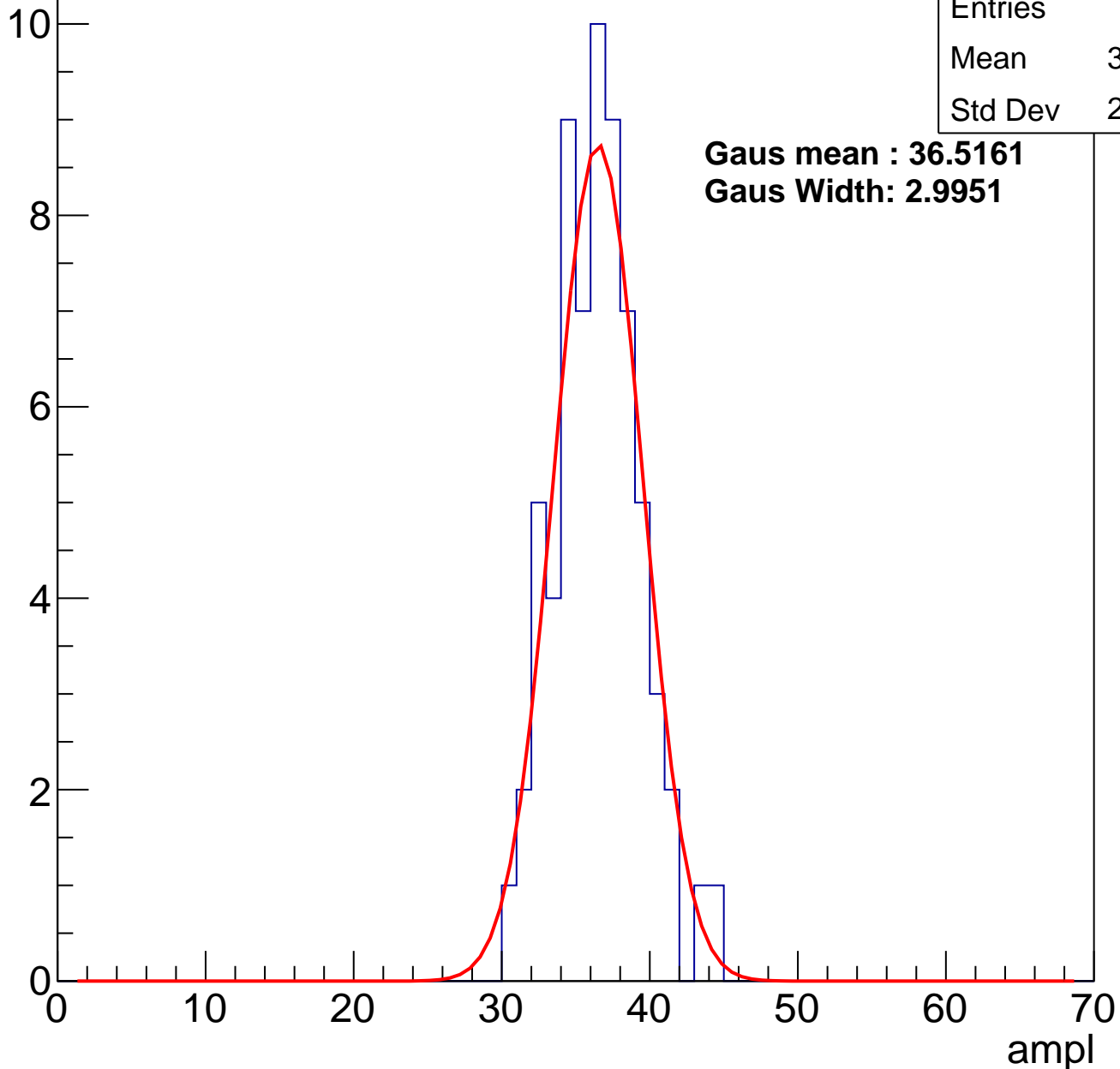
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	66
Mean	36.03
Std Dev	2.855

**Gaus mean : 36.5161**

**Gaus Width: 2.9951**

Entry



# B1L003S, U3-ch37, adc2

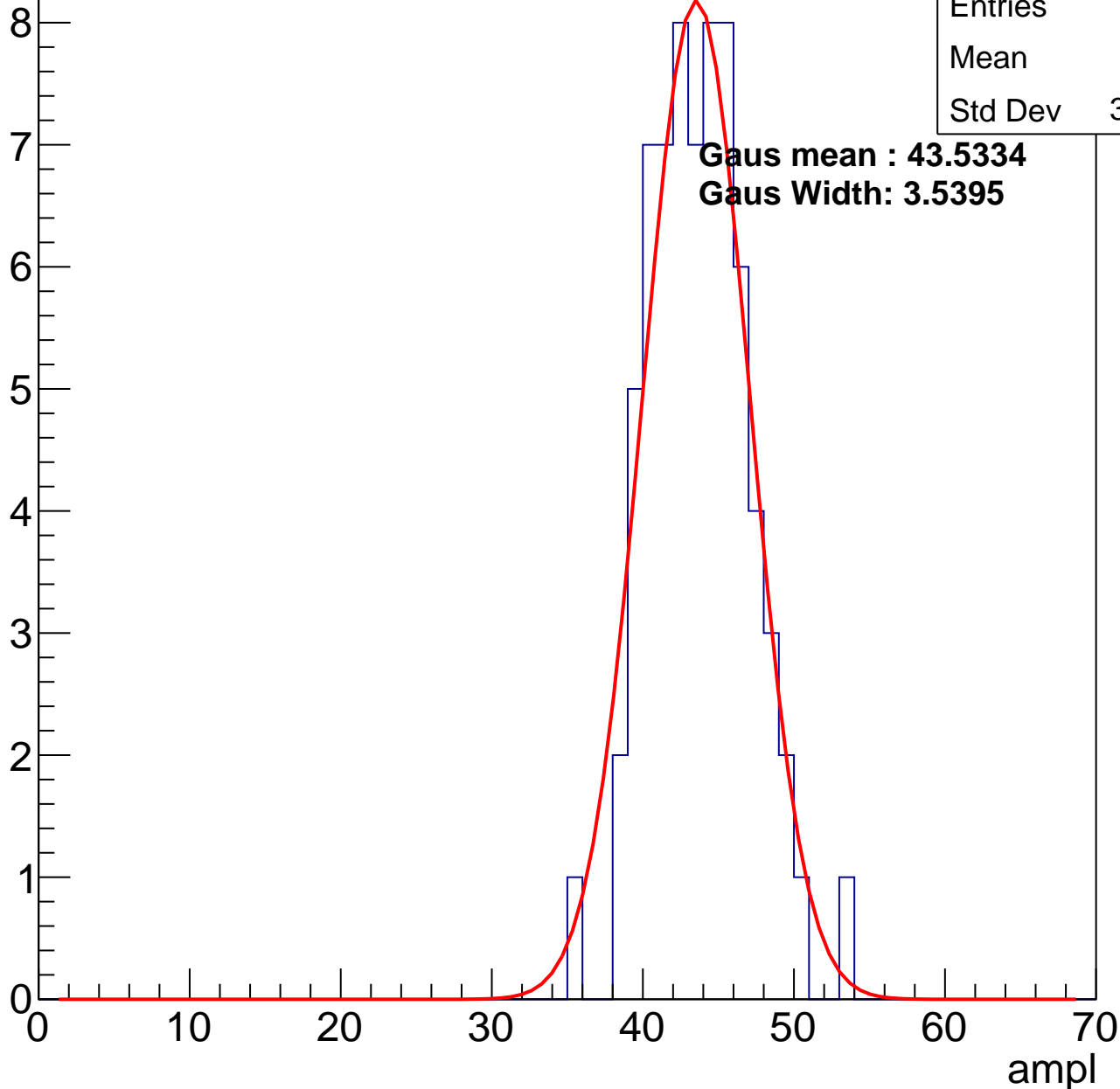
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	43.3
Std Dev	3.253

**Gaus mean : 43.5334**

**Gaus Width: 3.5395**

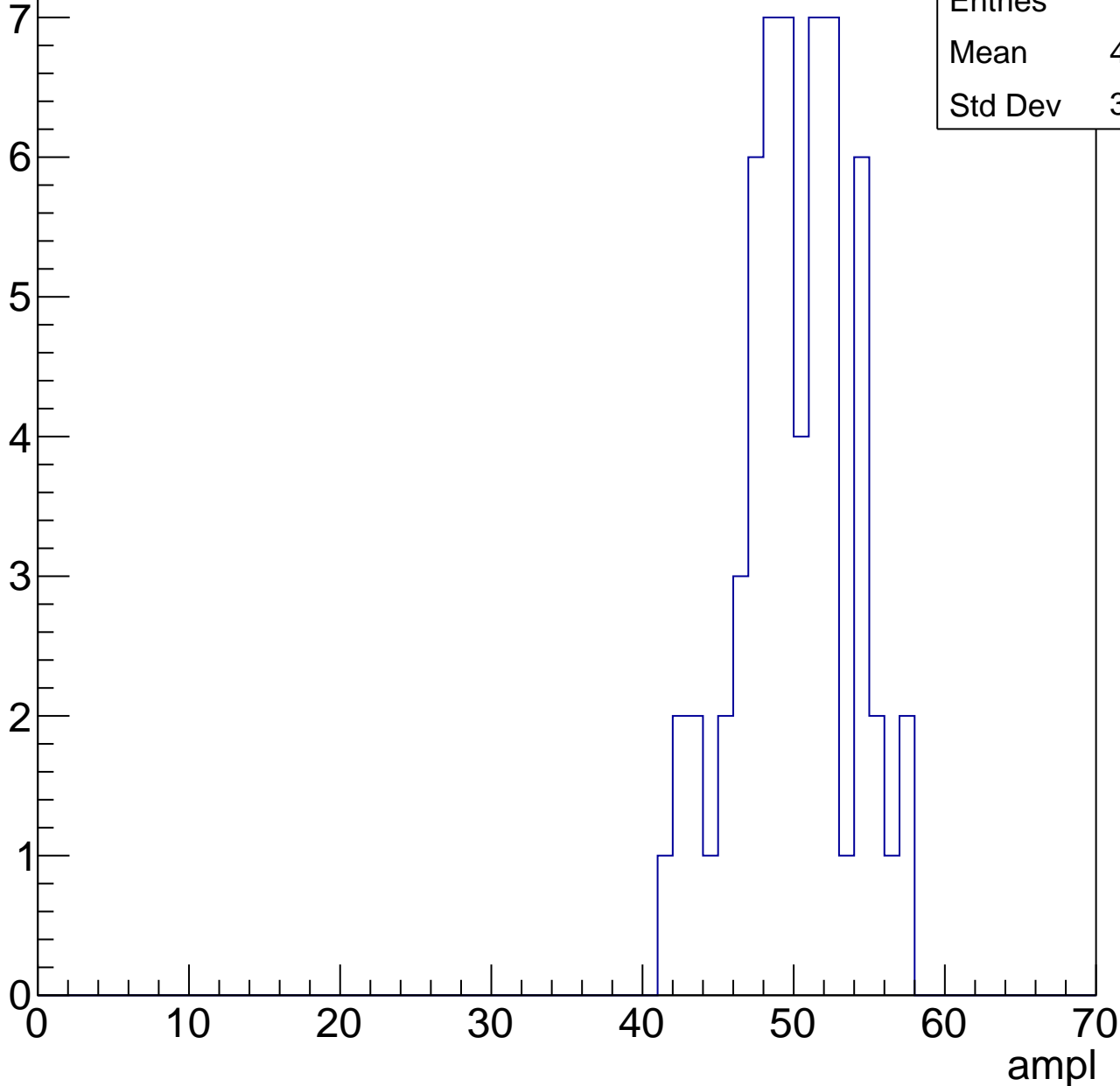


# B1L003S, U3-ch37, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	49.54
Std Dev	3.713

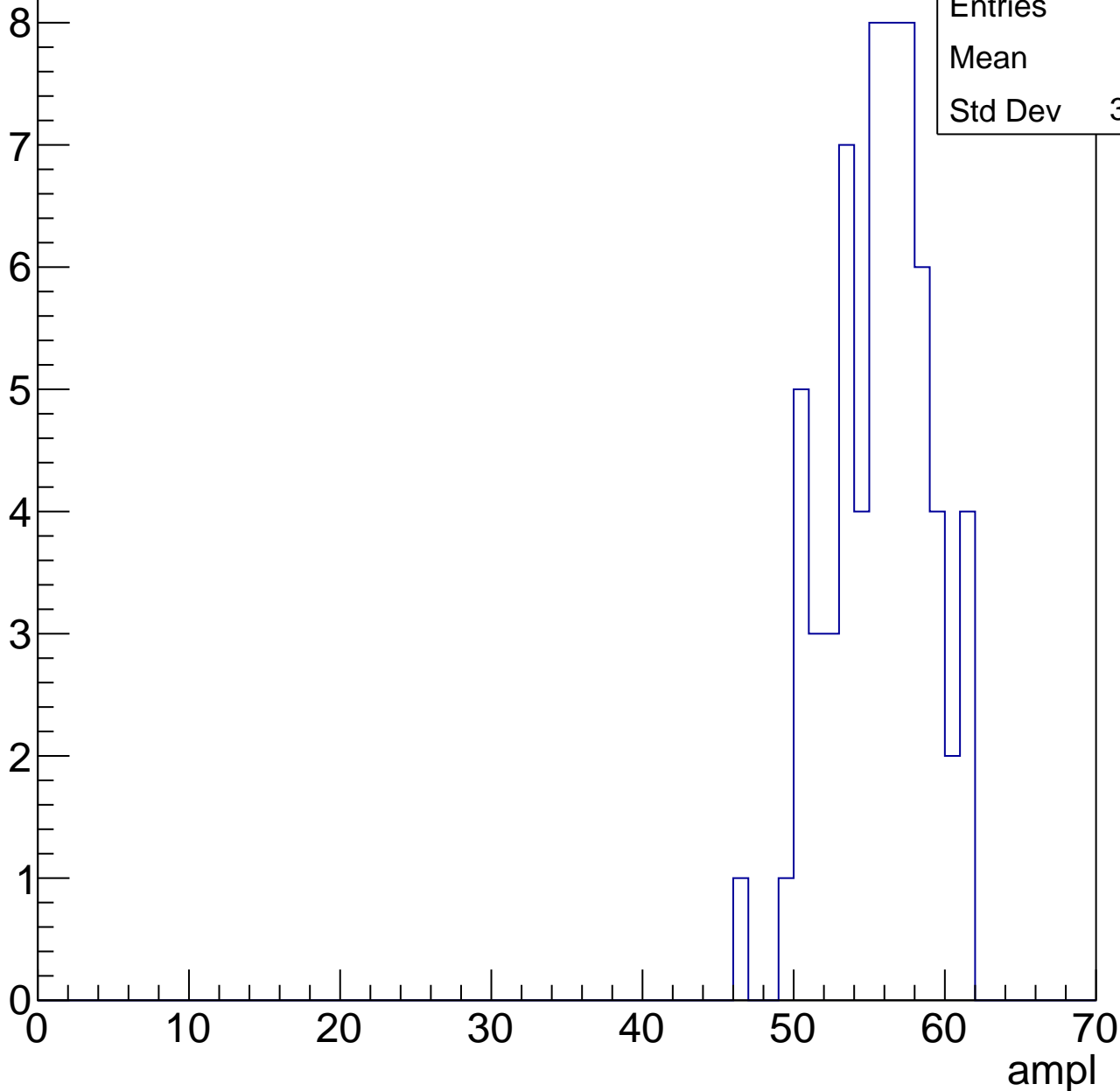


# B1L003S, U3-ch37, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	55.2
Std Dev	3.303

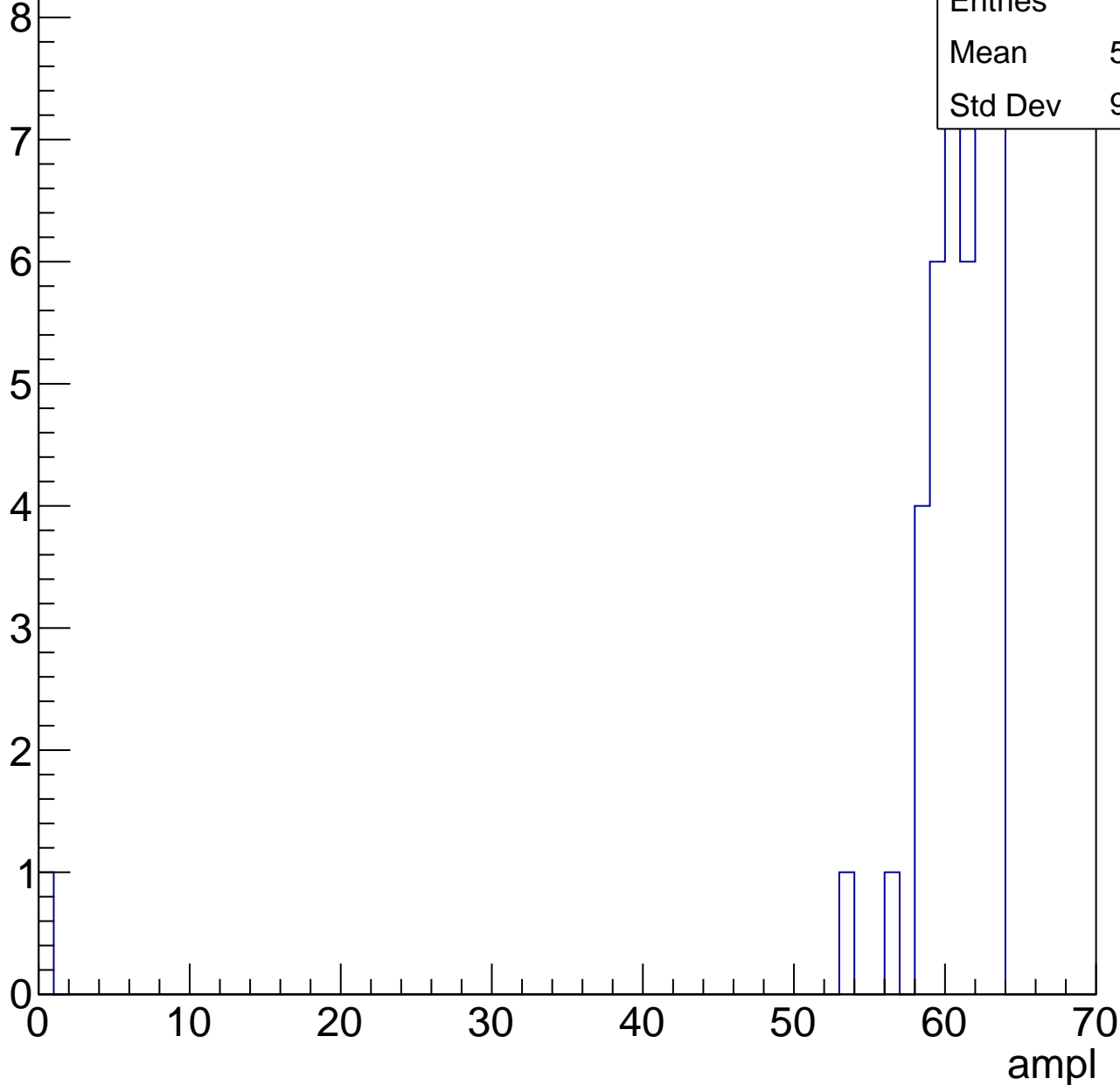


# B1L003S, U3-ch37, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	43
Mean	59.09
Std Dev	9.353



# B1L003S, U3-ch37, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

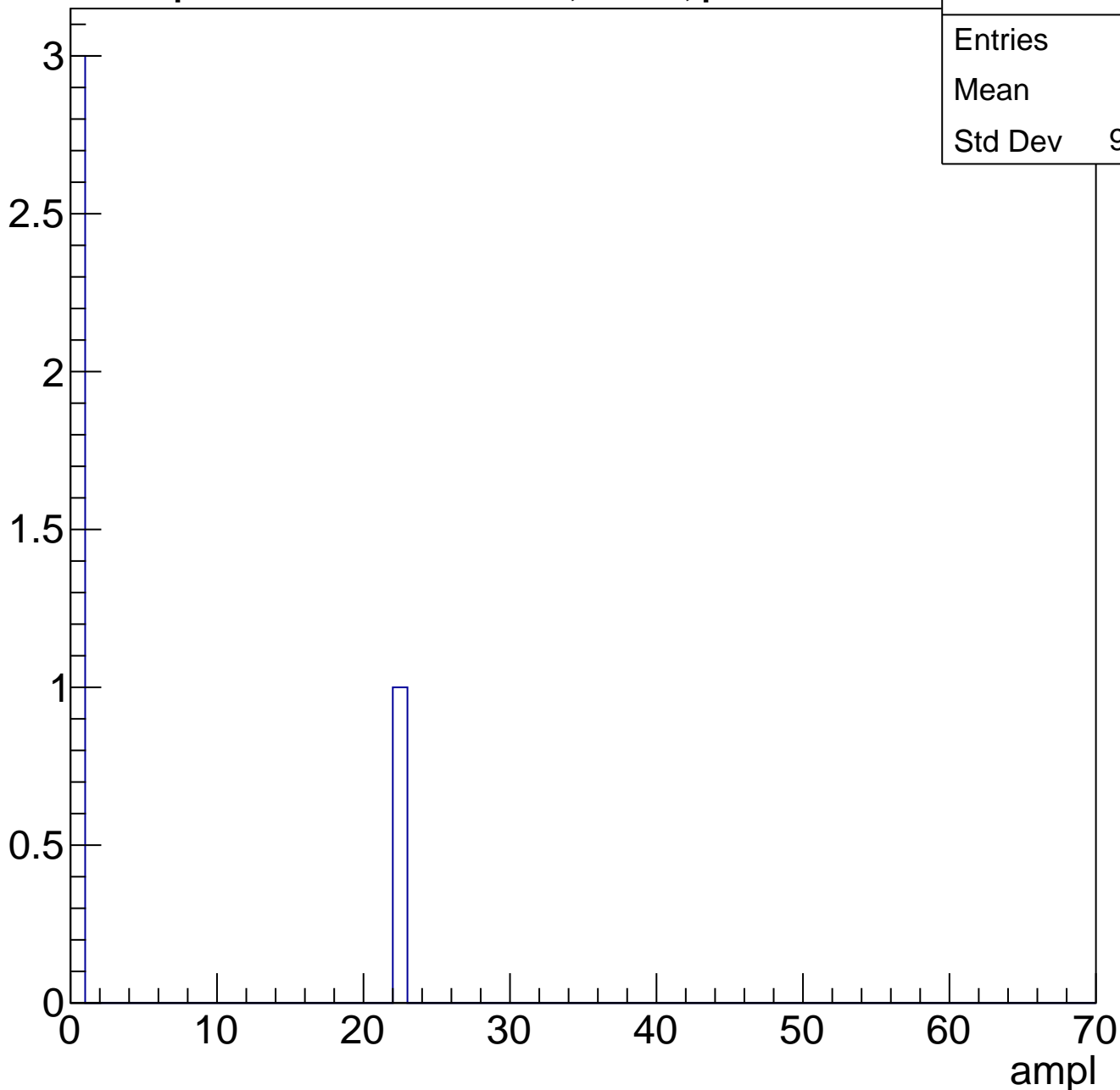




# B1L003S, U3-ch37, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	4
Mean	5.5
Std Dev	9.526

# B1L003S, U3-ch38, adc0

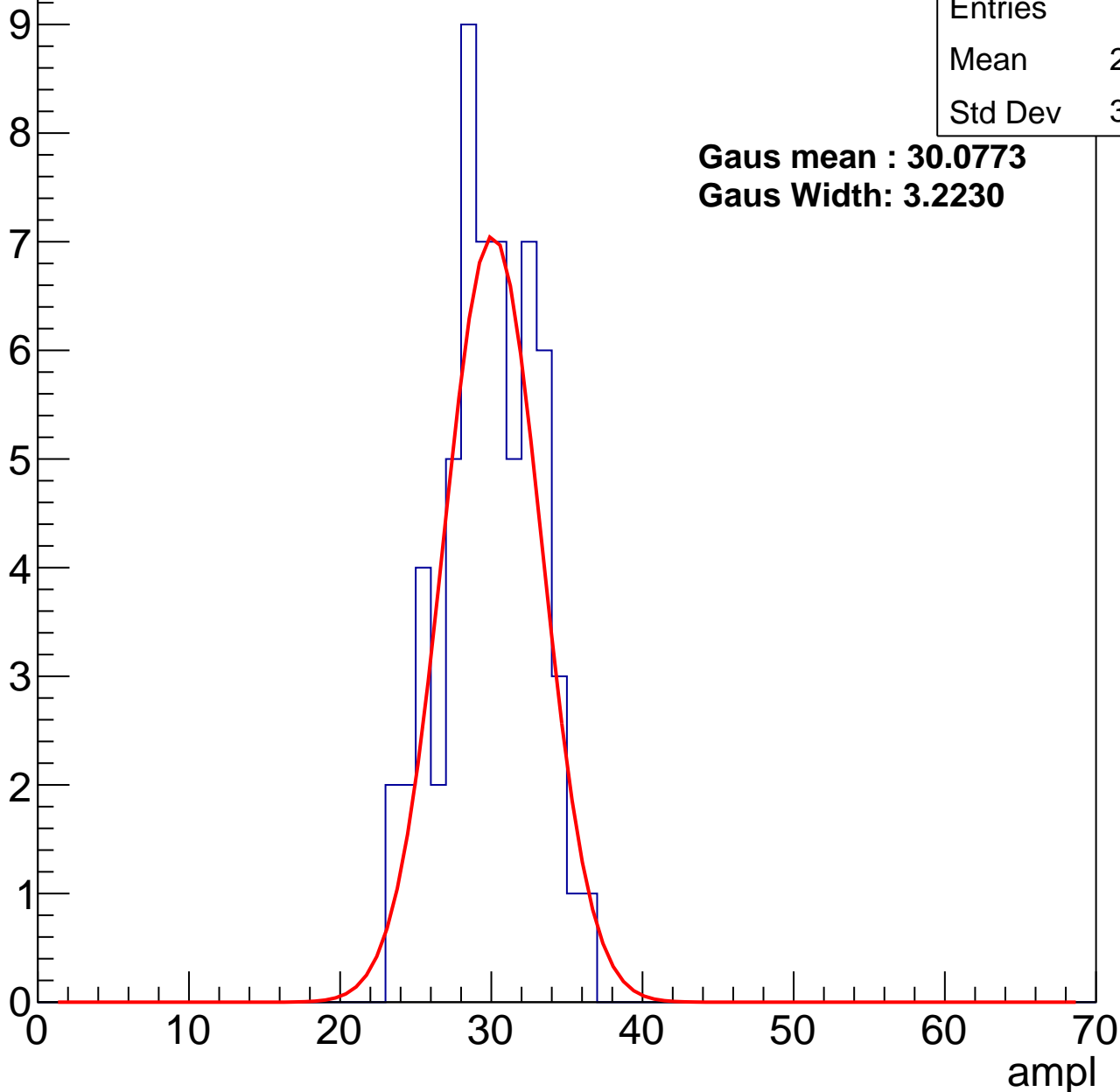
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	29.44
Std Dev	3.049

**Gaus mean : 30.0773**

**Gaus Width: 3.2230**



# B1L003S, U3-ch38, adc1

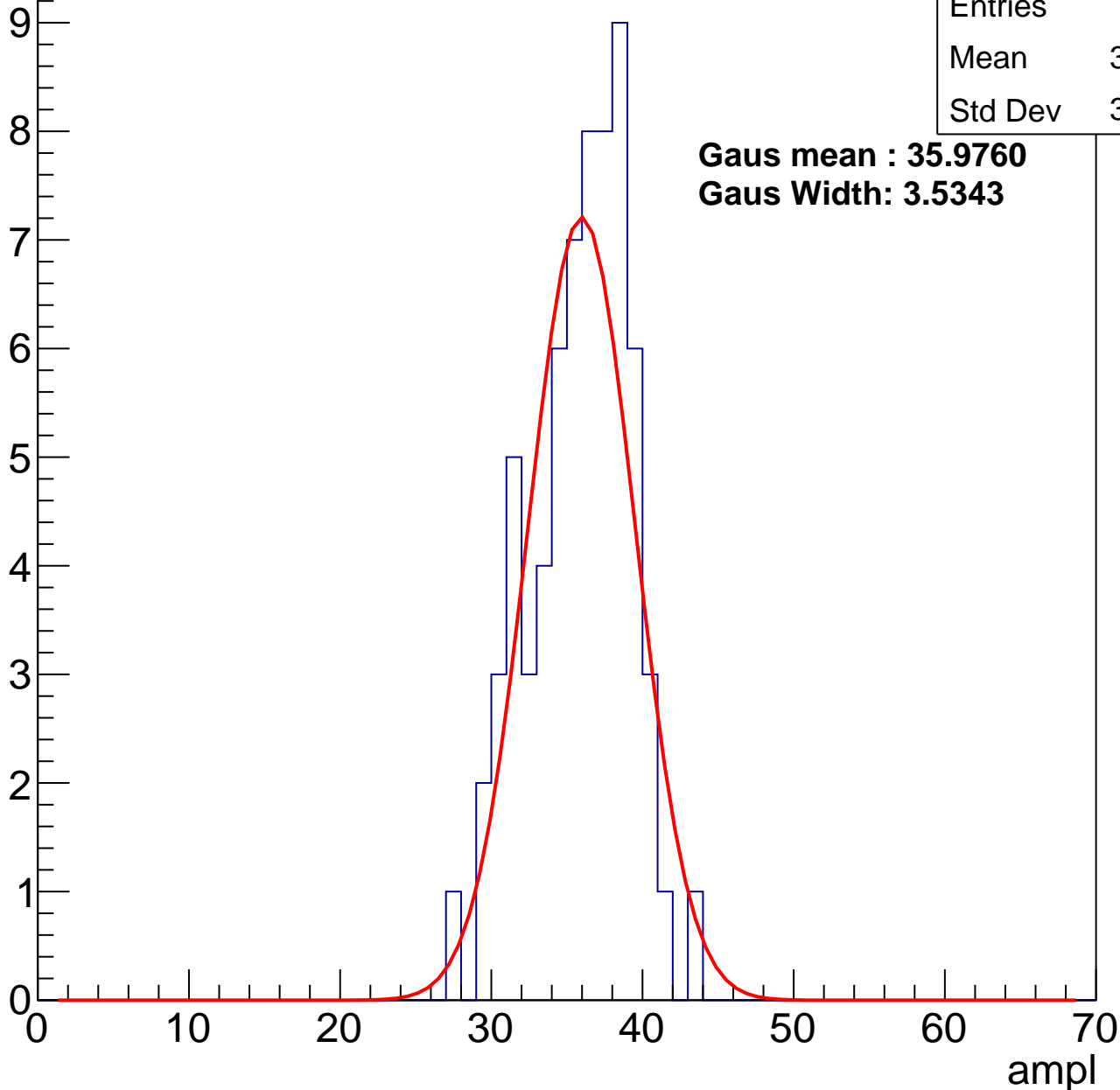
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	35.39
Std Dev	3.282

**Gaus mean : 35.9760**

**Gaus Width: 3.5343**



# B1L003S, U3-ch38, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	74
Mean	42.85
Std Dev	3.623

**Gaus mean : 43.8850**

**Gaus Width: 3.5215**

Entry

10

8

6

4

2

0

0

10

20

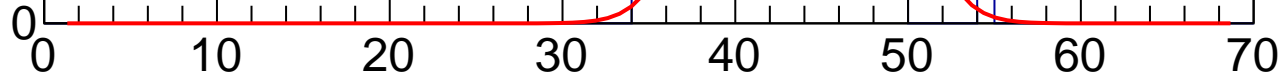
30

40

50

60

ampl

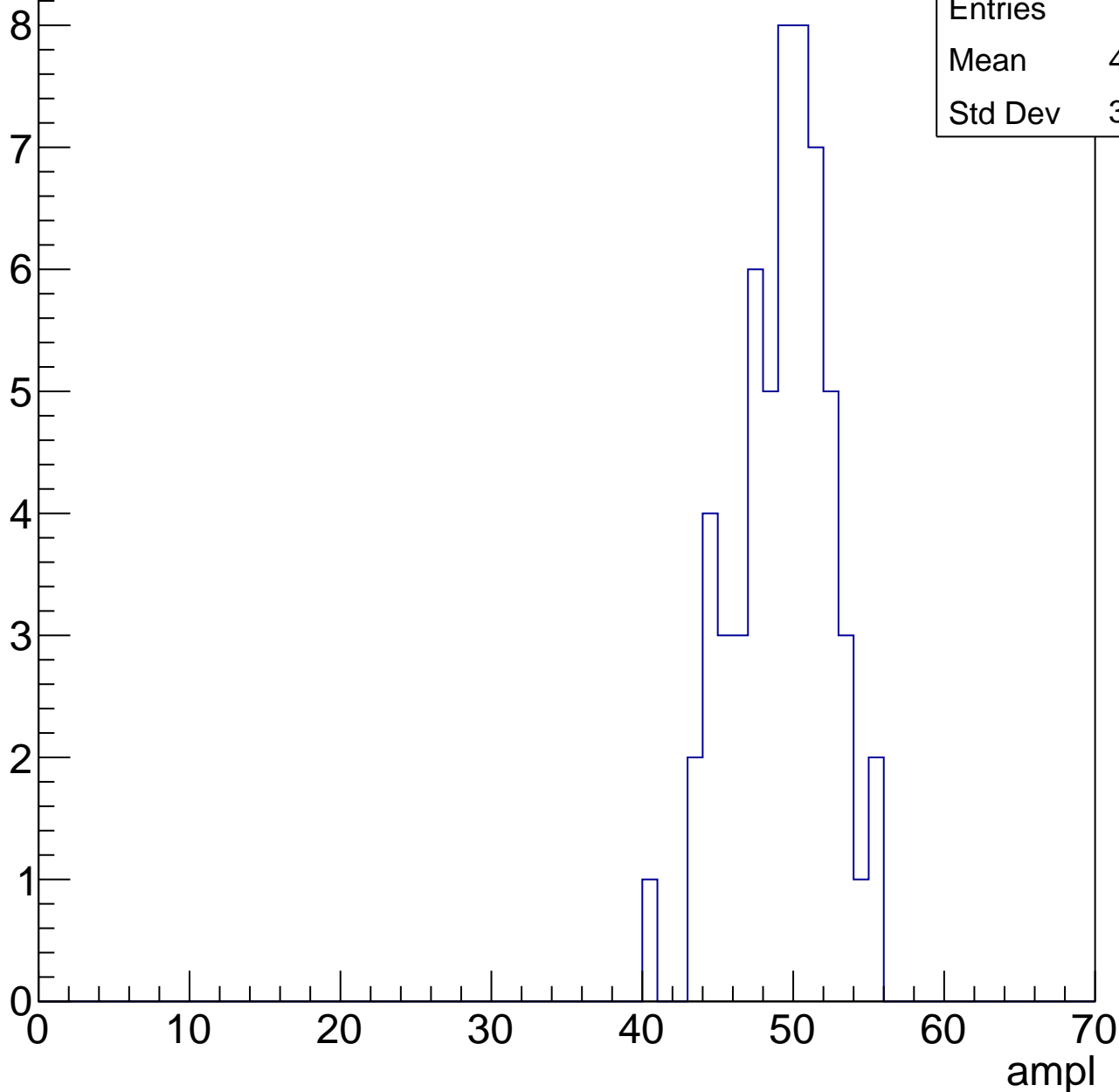


# B1L003S, U3-ch38, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	48.78
Std Dev	3.163

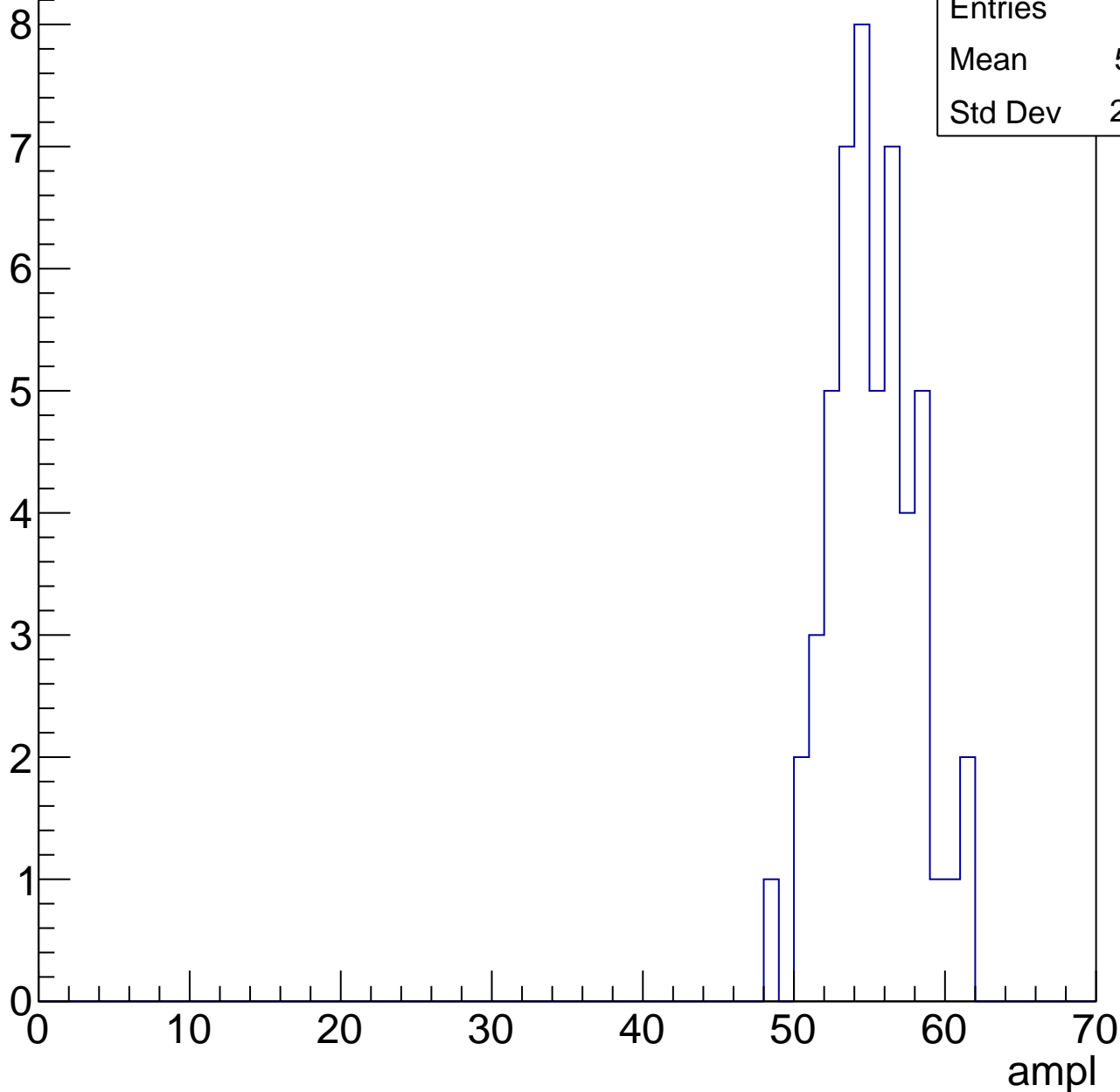


# B1L003S, U3-ch38, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	51
Mean	54.71
Std Dev	2.817

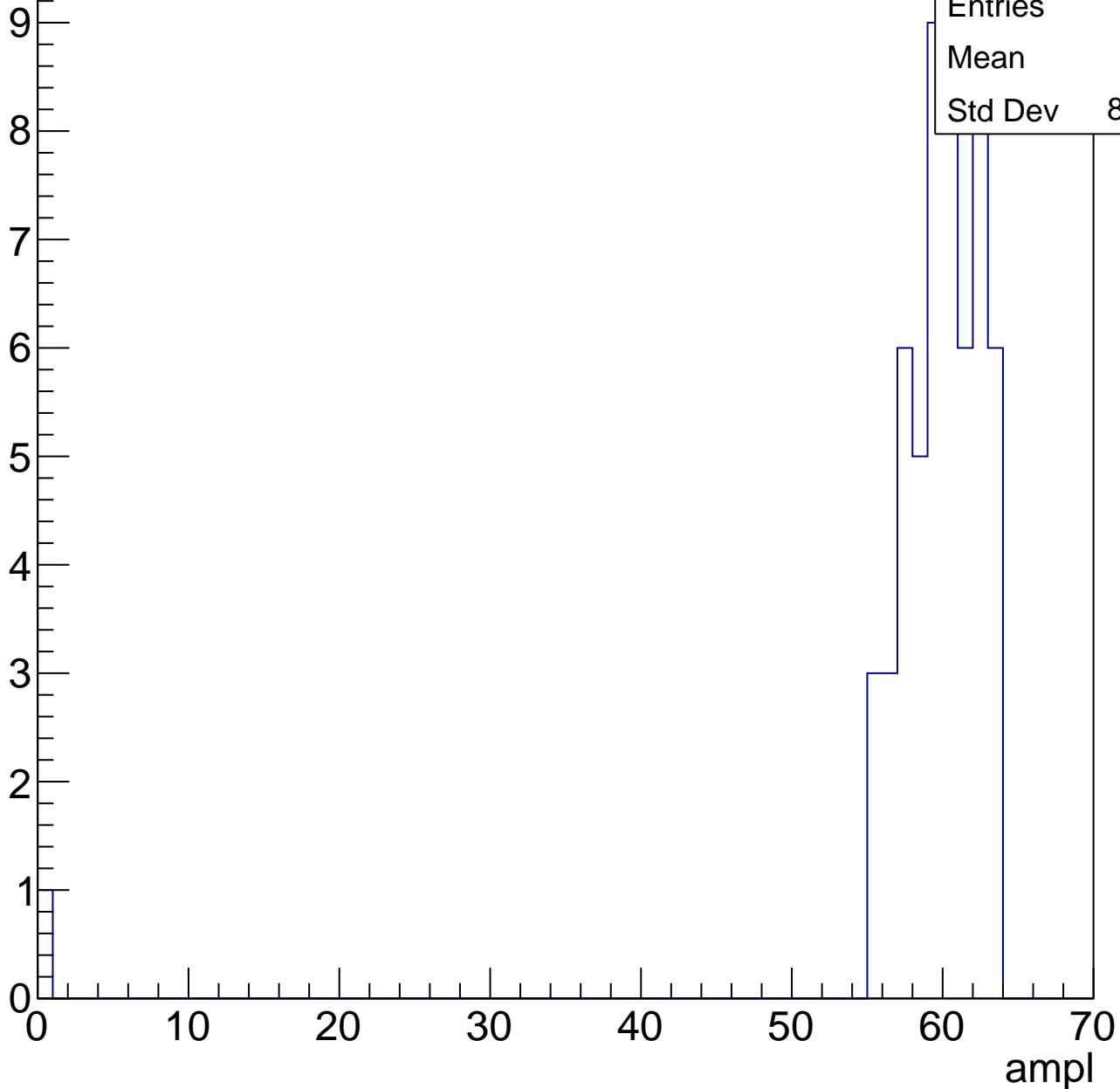


# B1L003S, U3-ch38, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	58.5
Std Dev	8.207



# B1L003S, U3-ch38, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch38, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L003S, U3-ch39, adc0

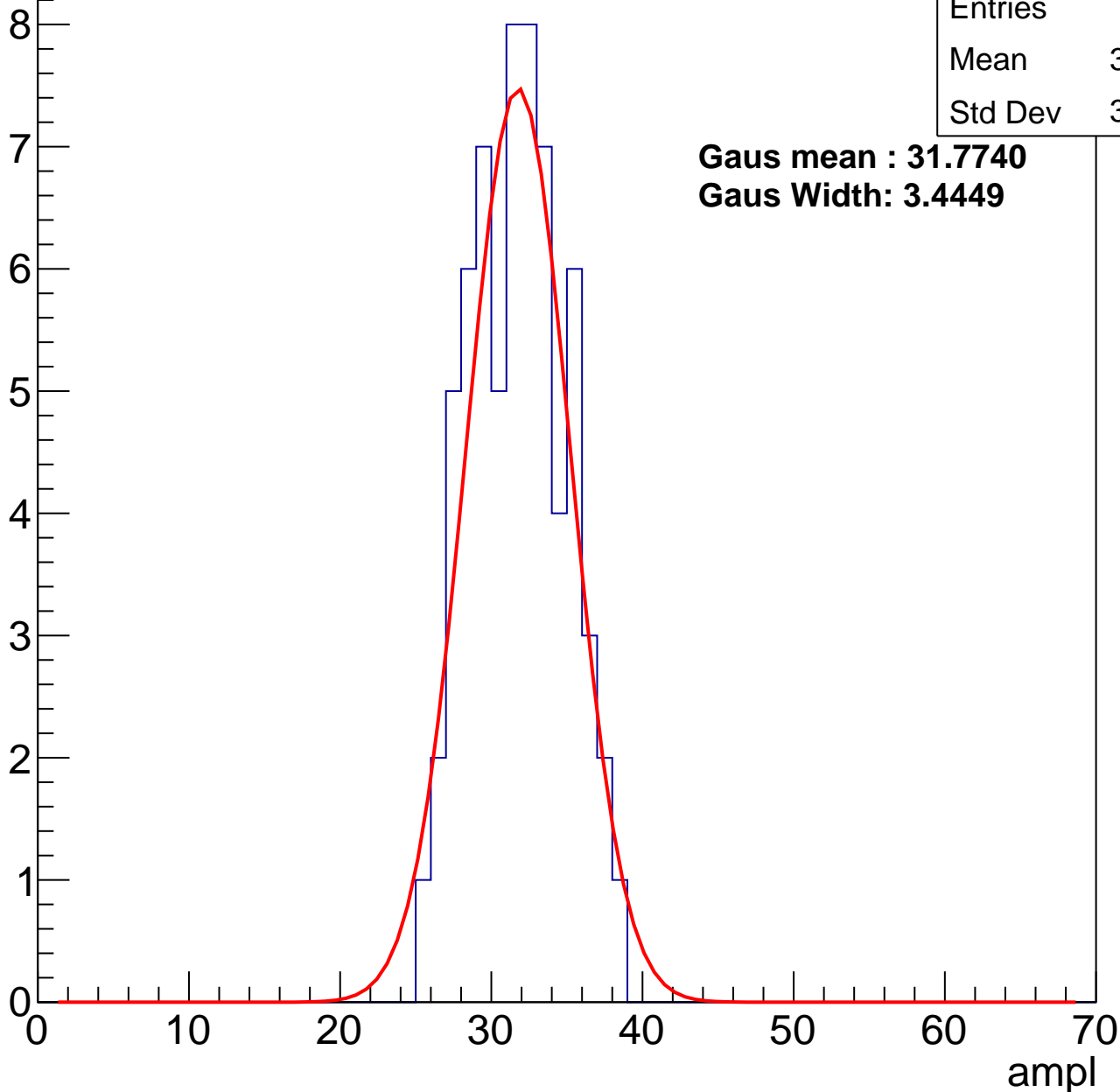
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	31.29
Std Dev	3.067

**Gaus mean : 31.7740**

**Gaus Width: 3.4449**



# B1L003S, U3-ch39, adc1

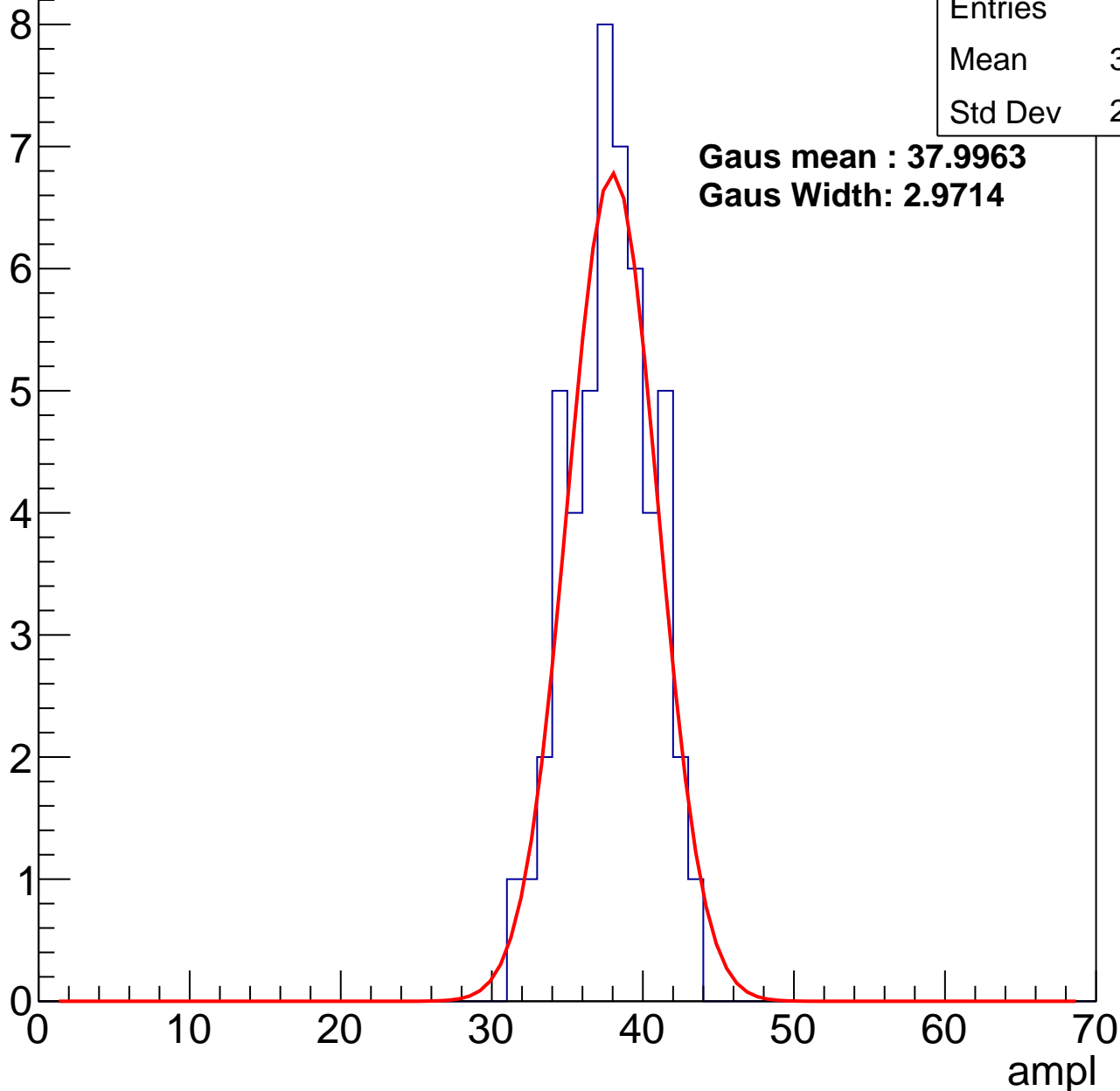
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	51
Mean	37.39
Std Dev	2.745

**Gaus mean : 37.9963**

**Gaus Width: 2.9714**



# B1L003S, U3-ch39, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	55
Mean	42.95
Std Dev	3.06

**Gaus mean : 43.0955**

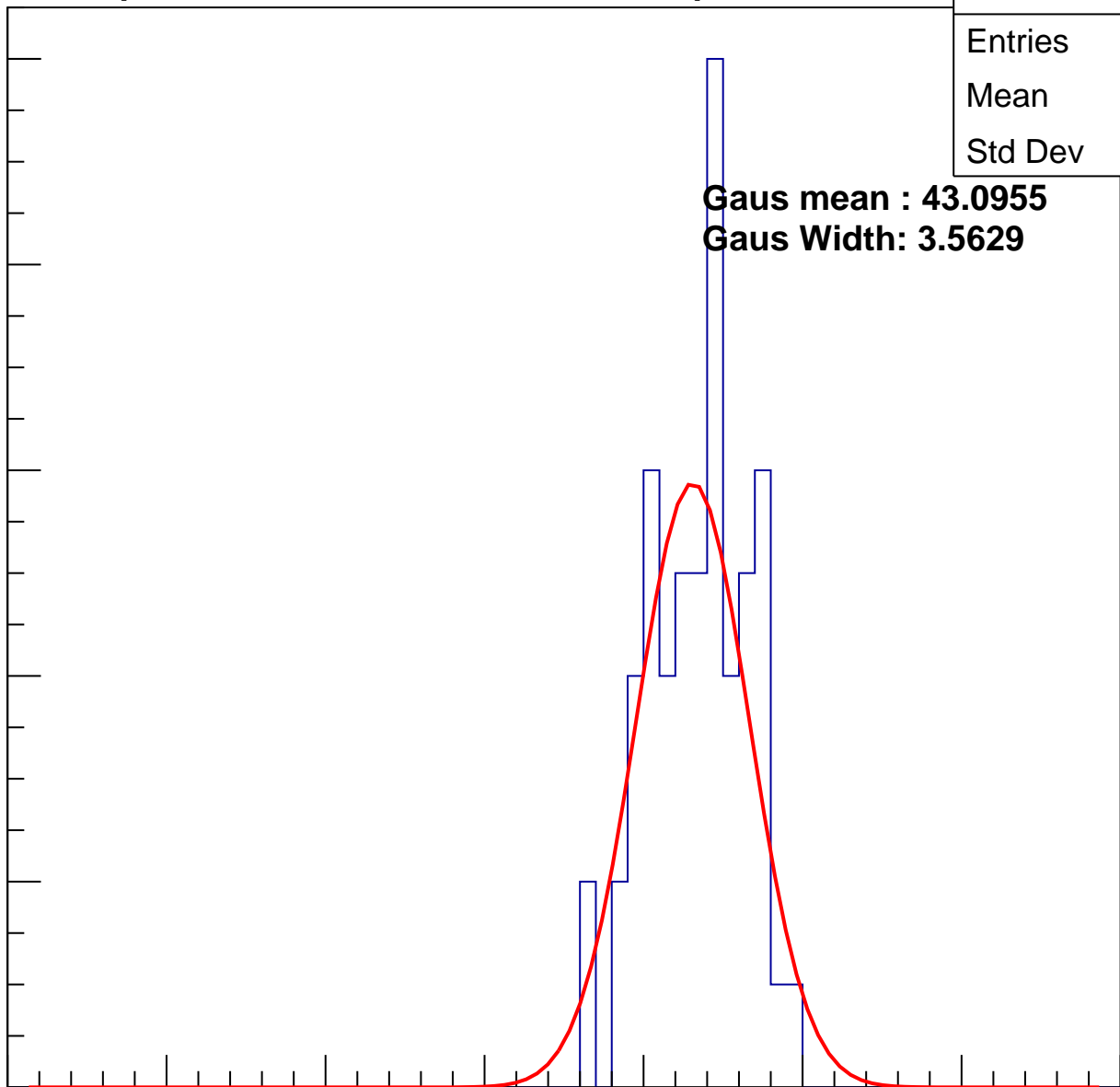
**Gaus Width: 3.5629**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

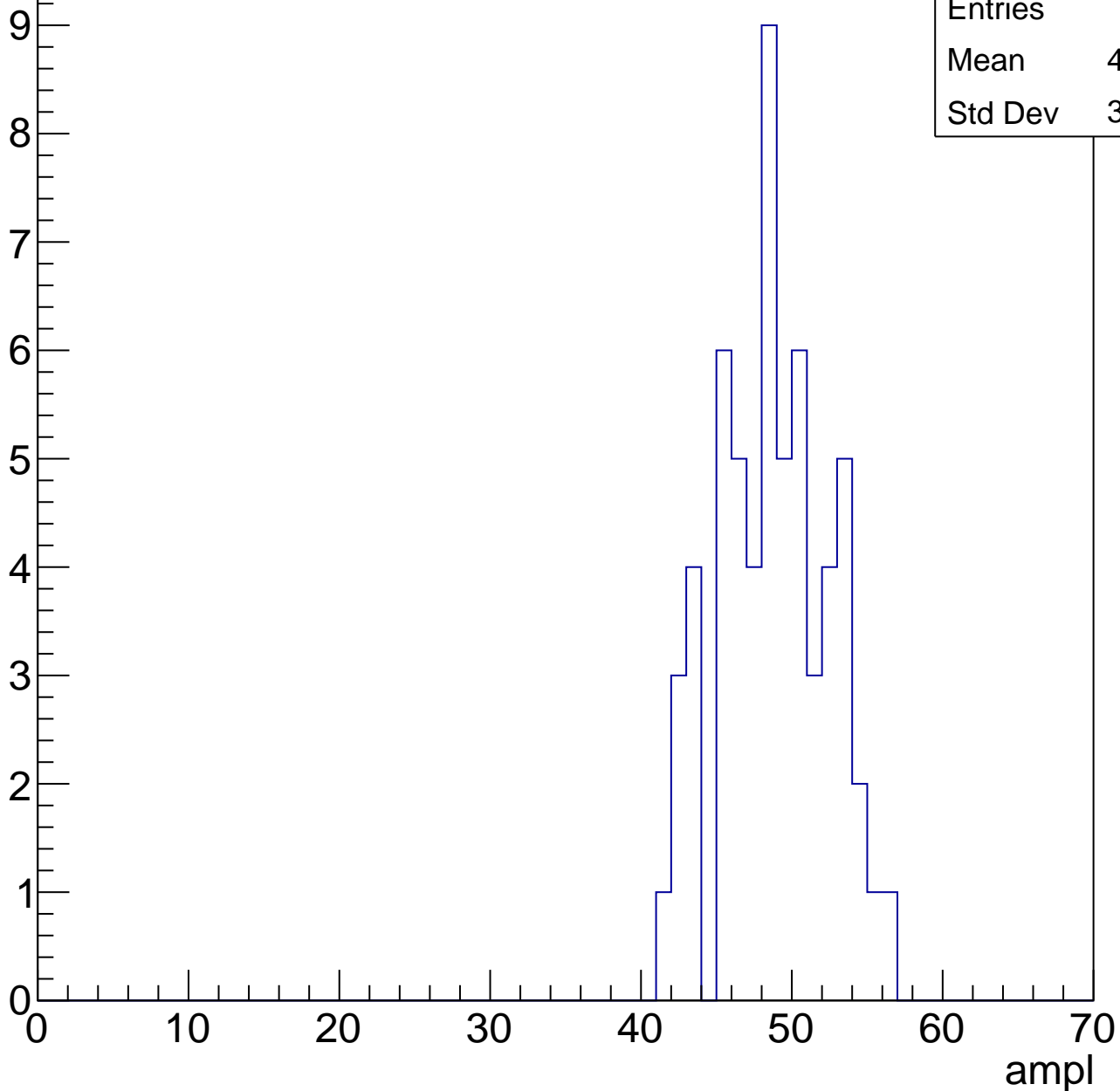


# B1L003S, U3-ch39, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

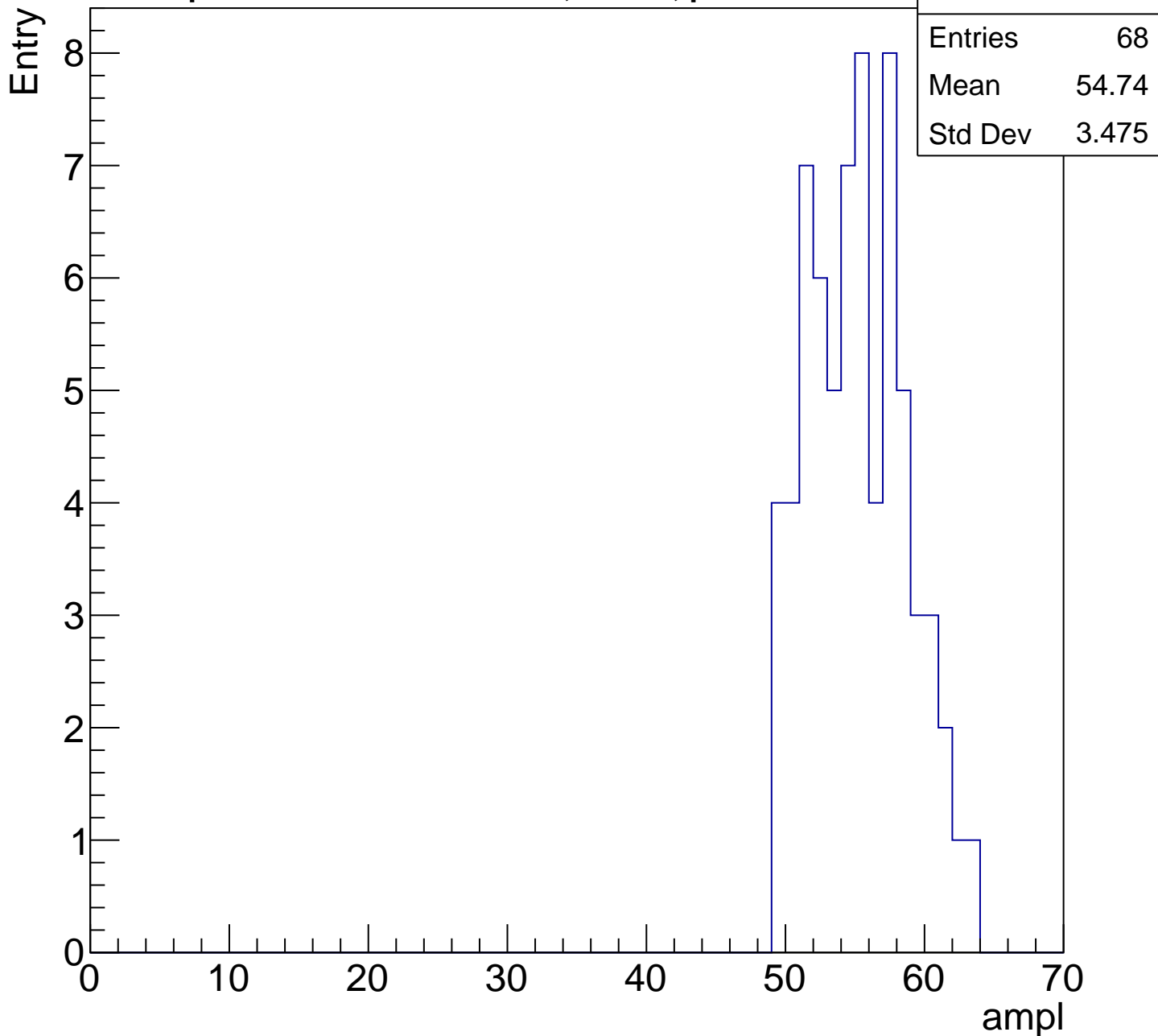
Entry

Entries	59
Mean	48.29
Std Dev	3.589



# B1L003S, U3-ch39, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

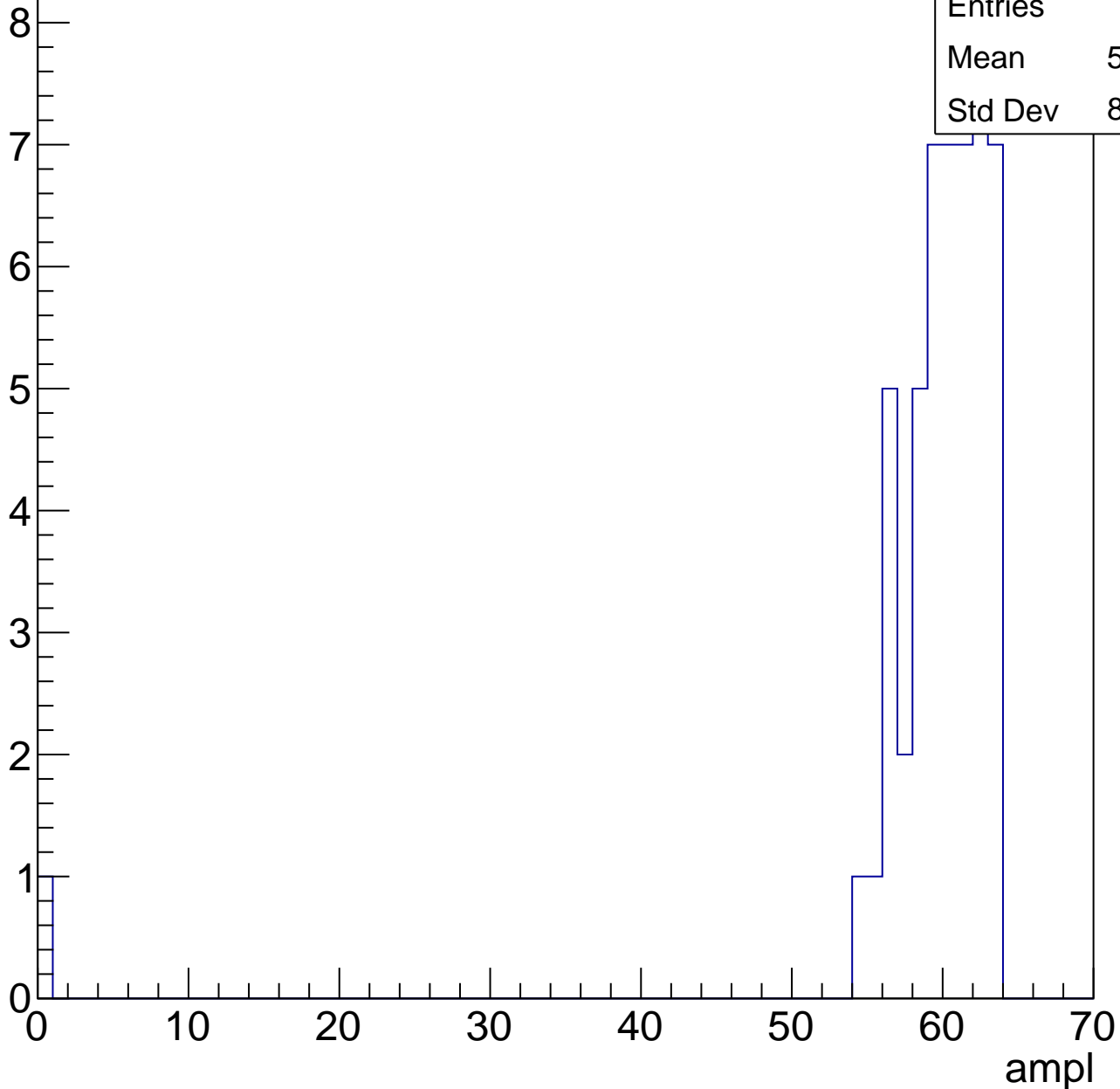


# B1L003S, U3-ch39, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	51
Mean	58.63
Std Dev	8.623



# B1L003S, U3-ch39, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch39, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U3-ch40, adc0

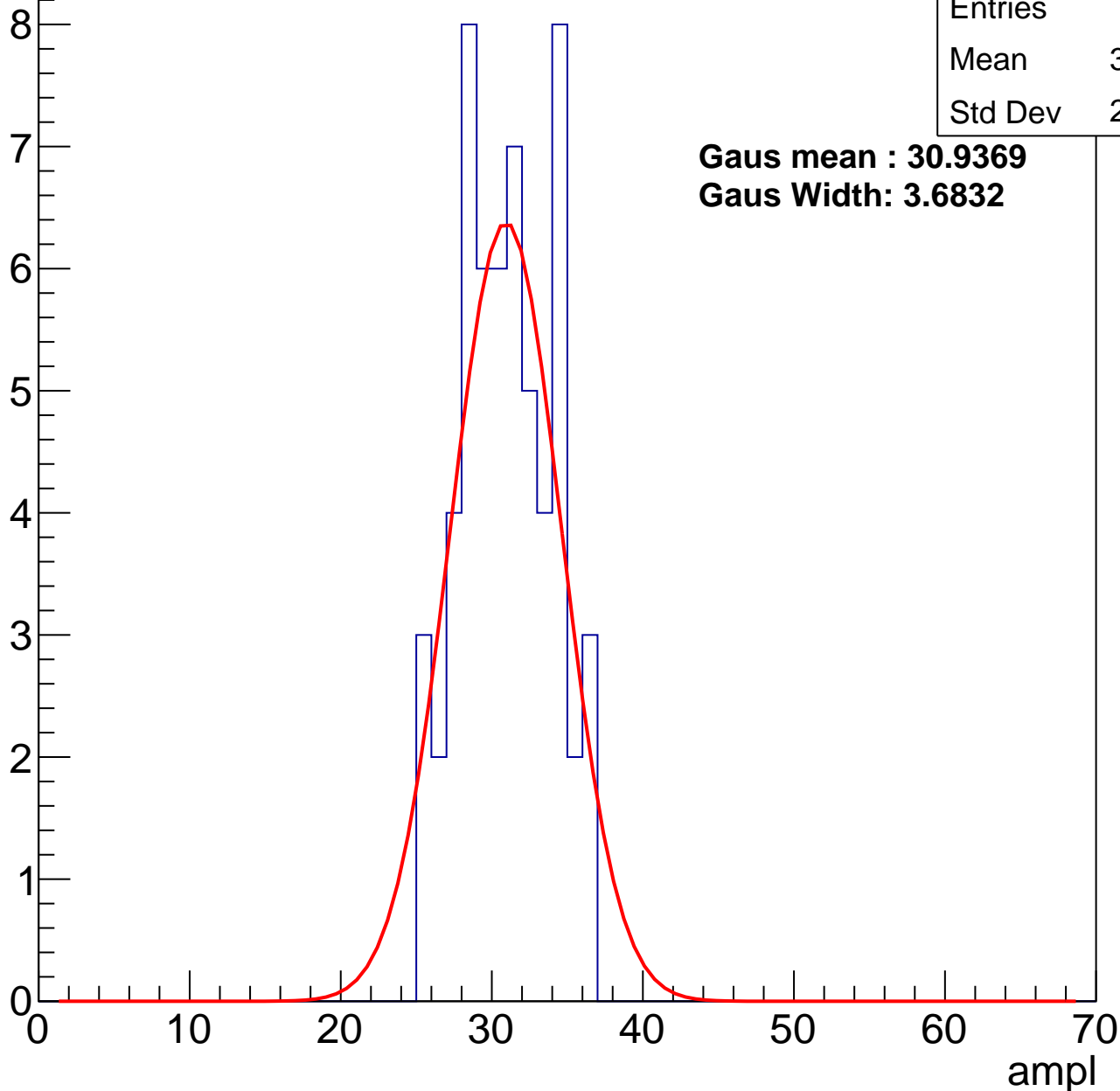
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	30.55
Std Dev	2.972

**Gaus mean : 30.9369**

**Gaus Width: 3.6832**



# B1L003S, U3-ch40, adc1

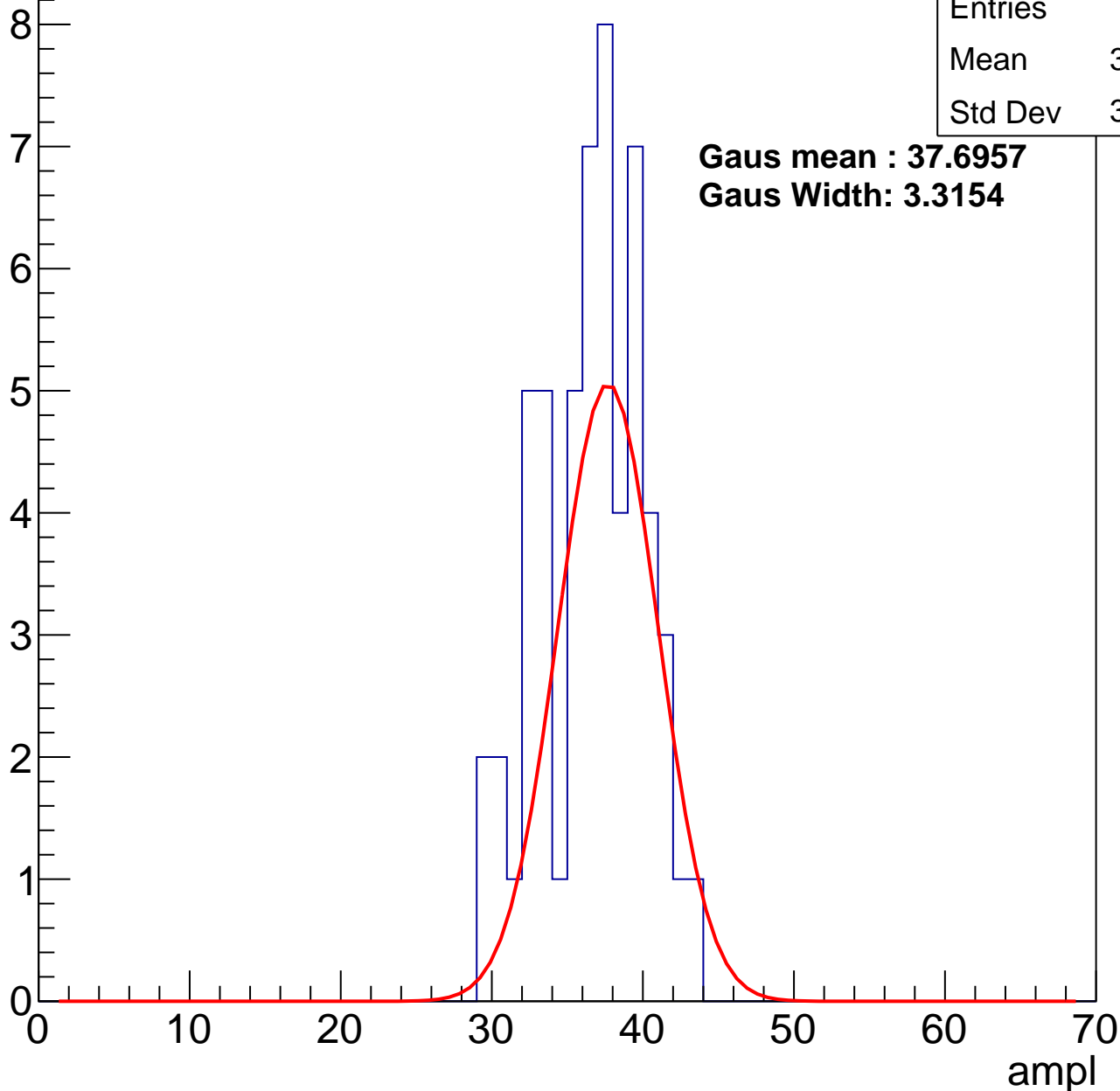
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	36.14
Std Dev	3.378

**Gaus mean : 37.6957**

**Gaus Width: 3.3154**



# B1L003S, U3-ch40, adc2

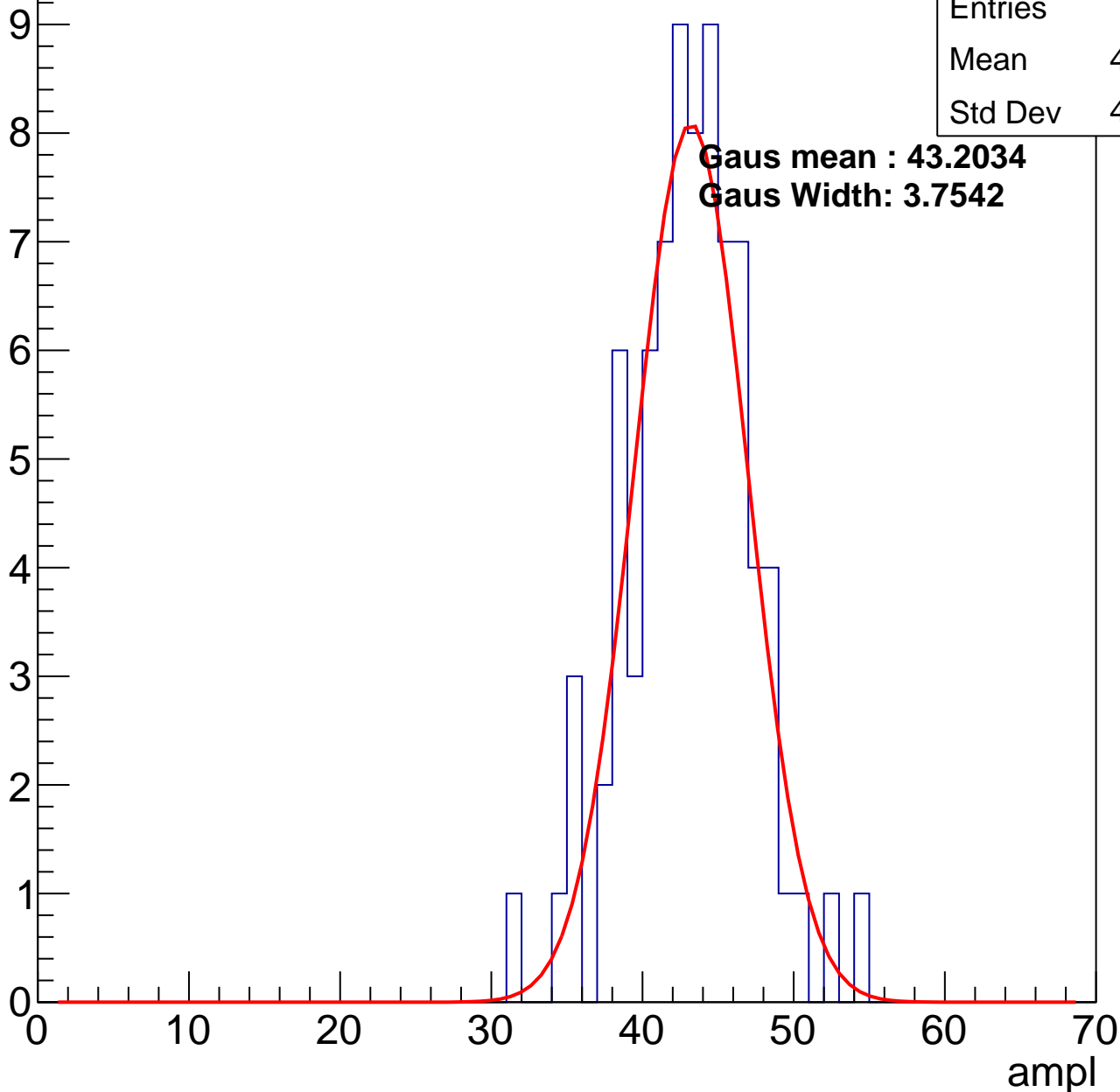
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	81
Mean	42.67
Std Dev	4.037

**Gaus mean : 43.2034**

**Gaus Width: 3.7542**

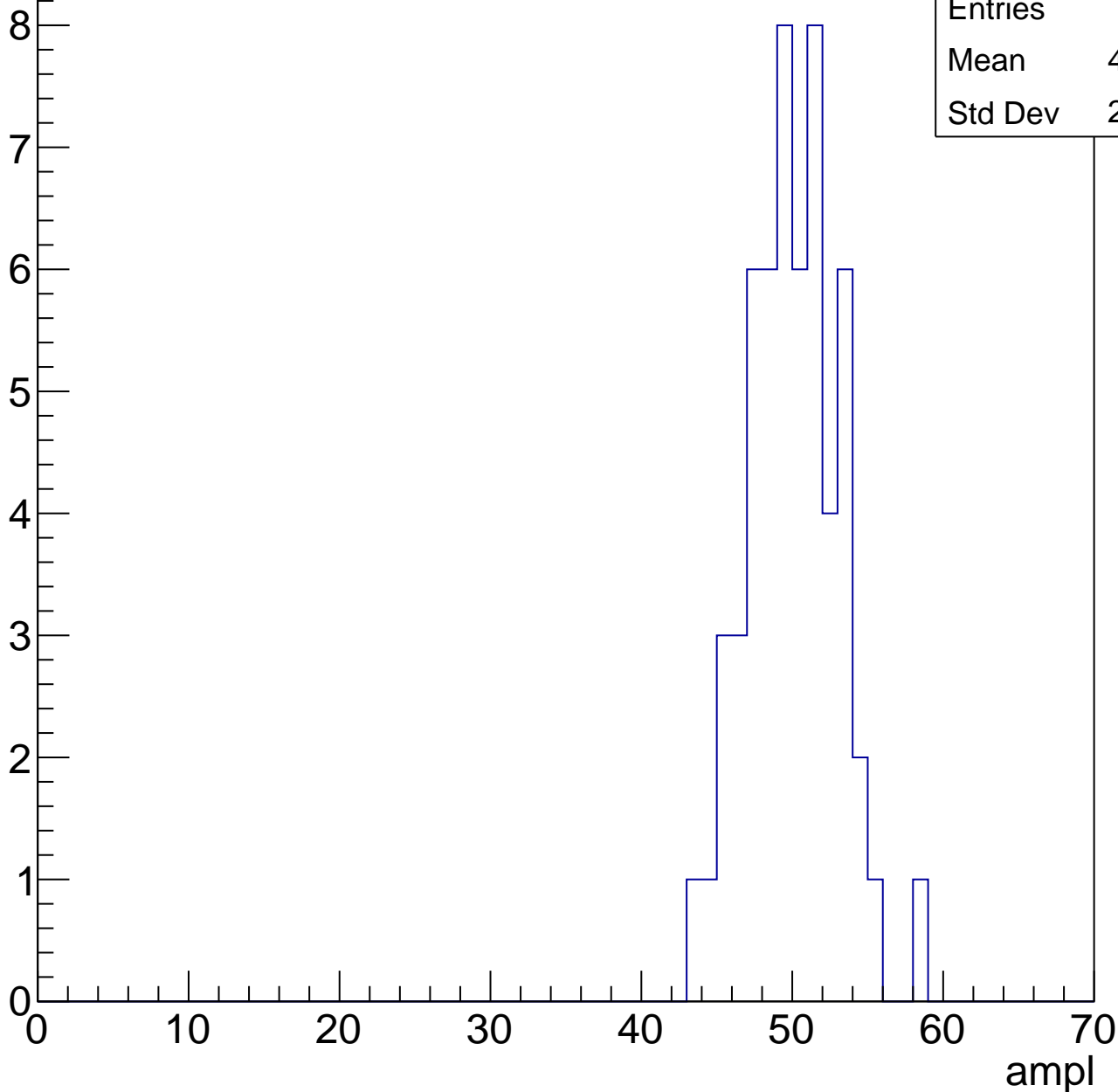


# B1L003S, U3-ch40, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	49.59
Std Dev	2.939

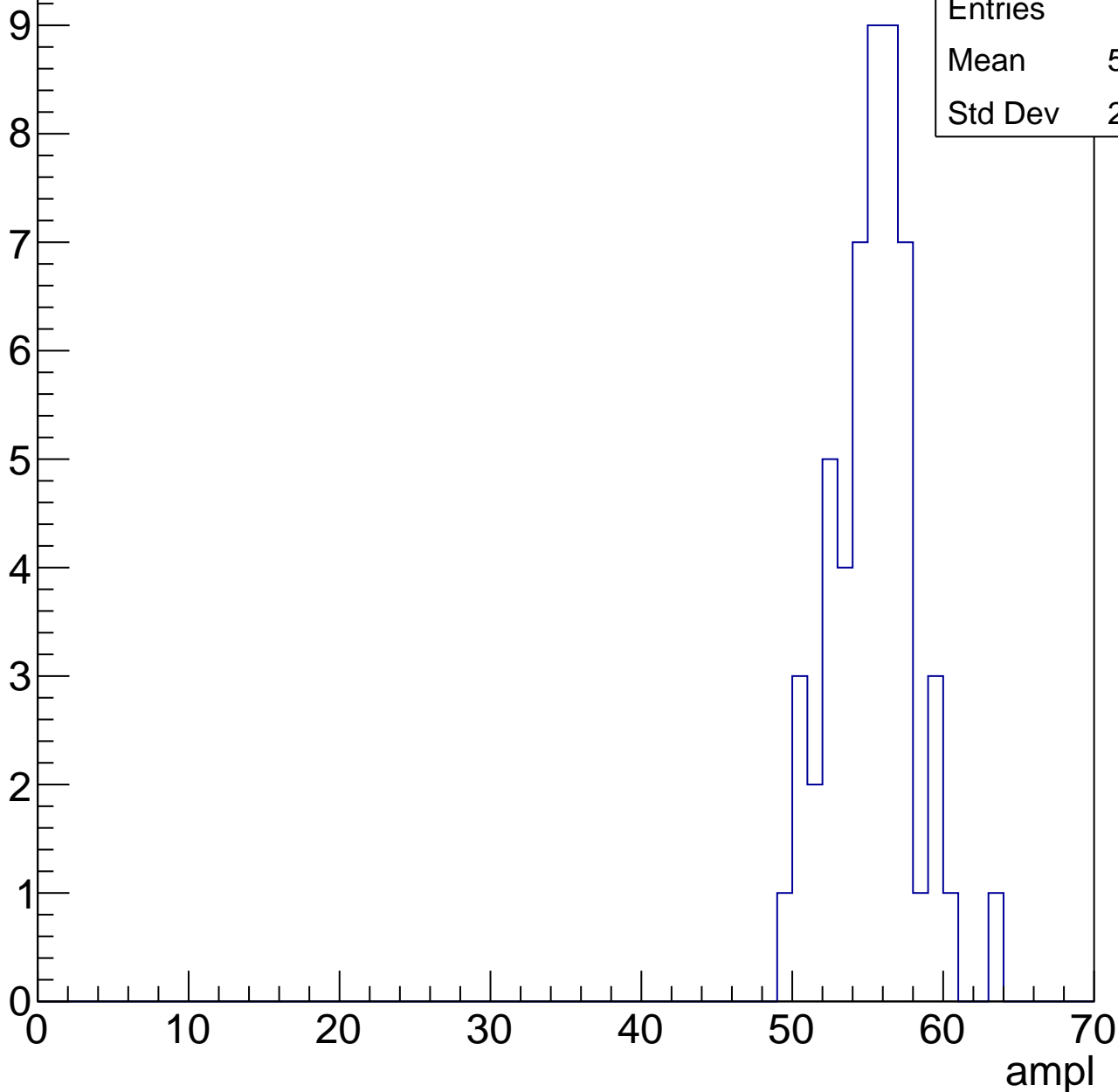


# B1L003S, U3-ch40, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	54.85
Std Dev	2.722



# B1L003S, U3-ch40, adc5

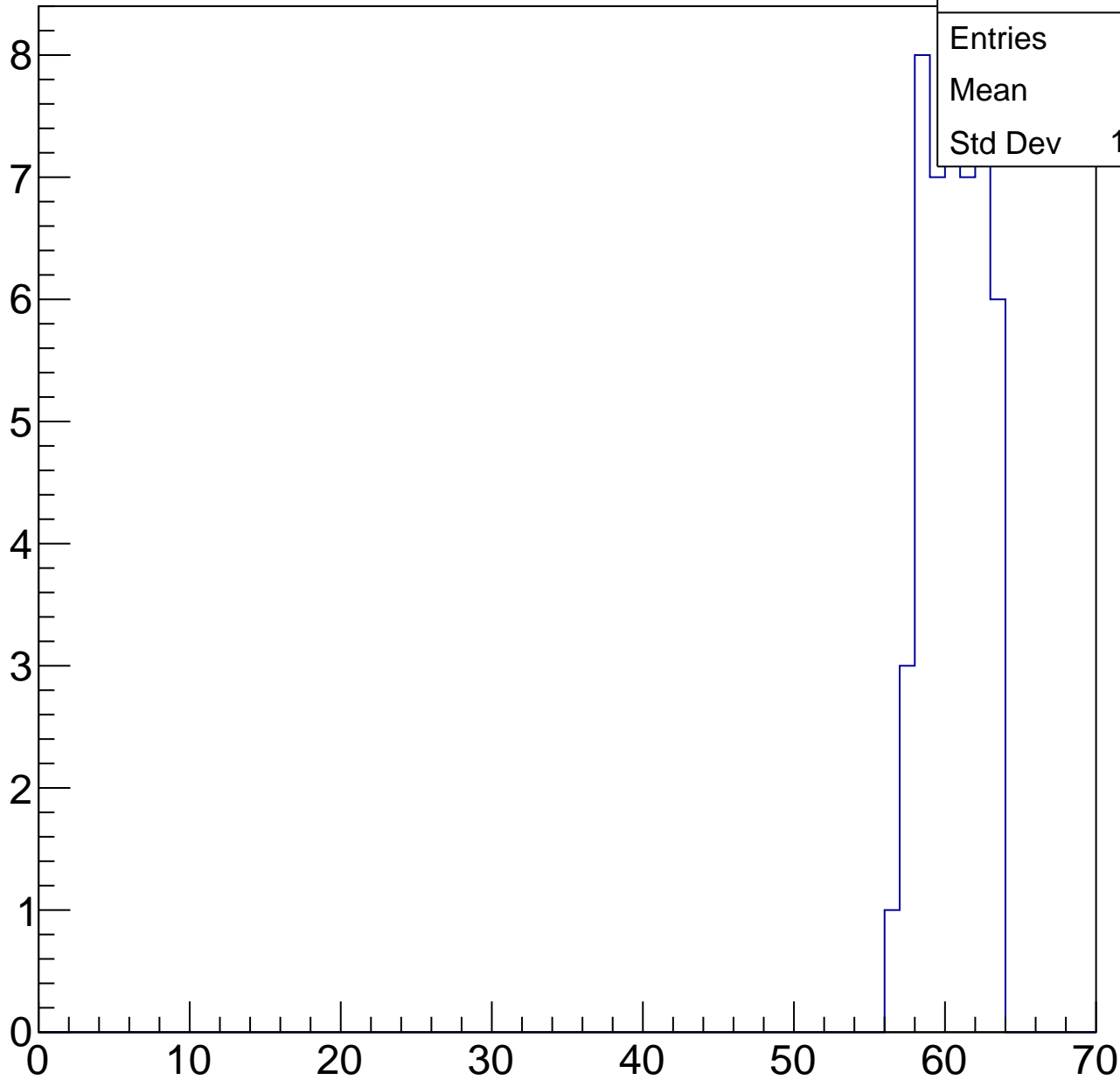
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	48
Mean	60.1
Std Dev	1.907

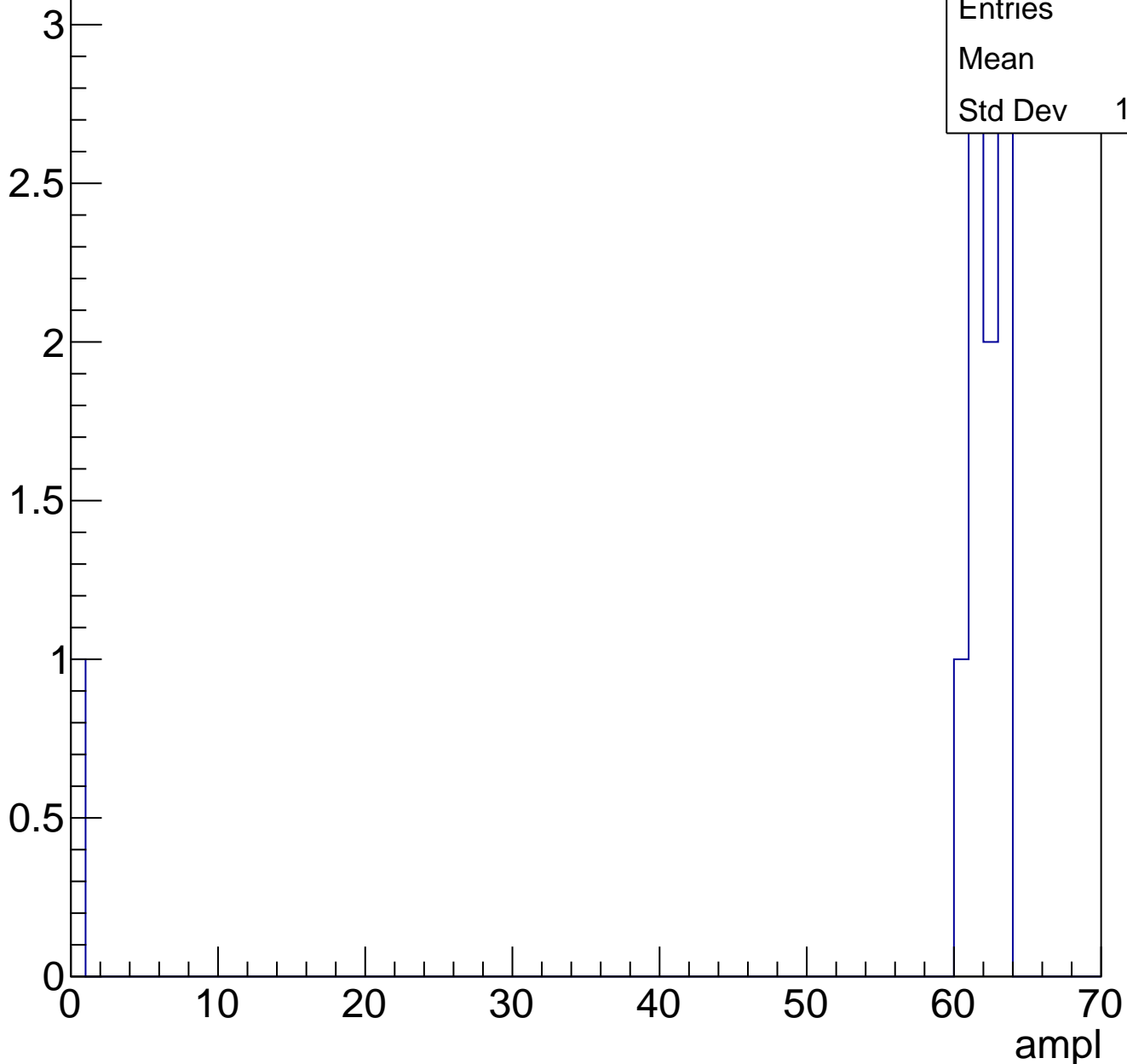
ampl



# B1L003S, U3-ch40, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch40, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U3-ch41, adc0

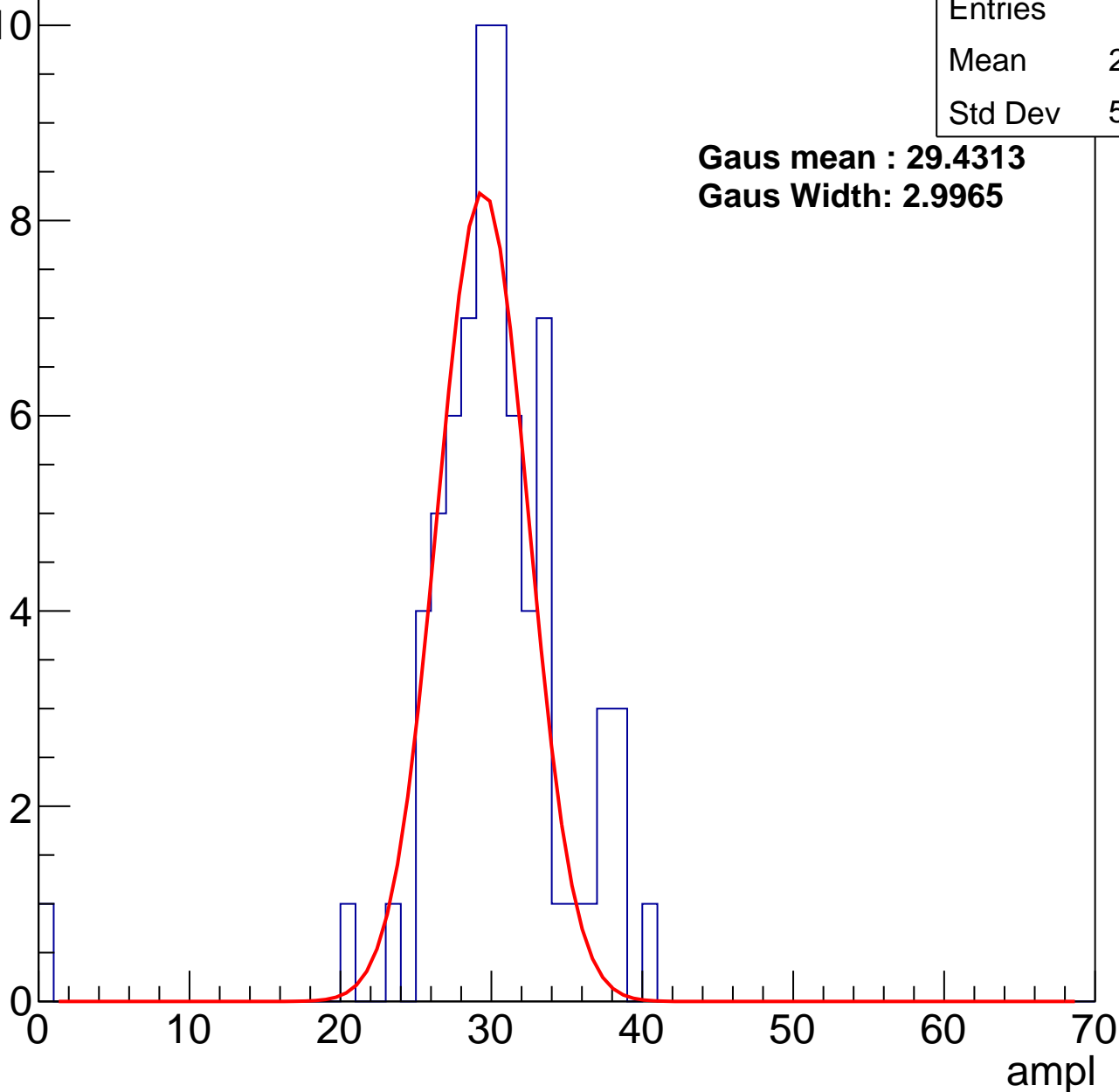
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	72
Mean	29.67
Std Dev	5.156

**Gaus mean : 29.4313**

**Gaus Width: 2.9965**



# B1L003S, U3-ch41, adc1

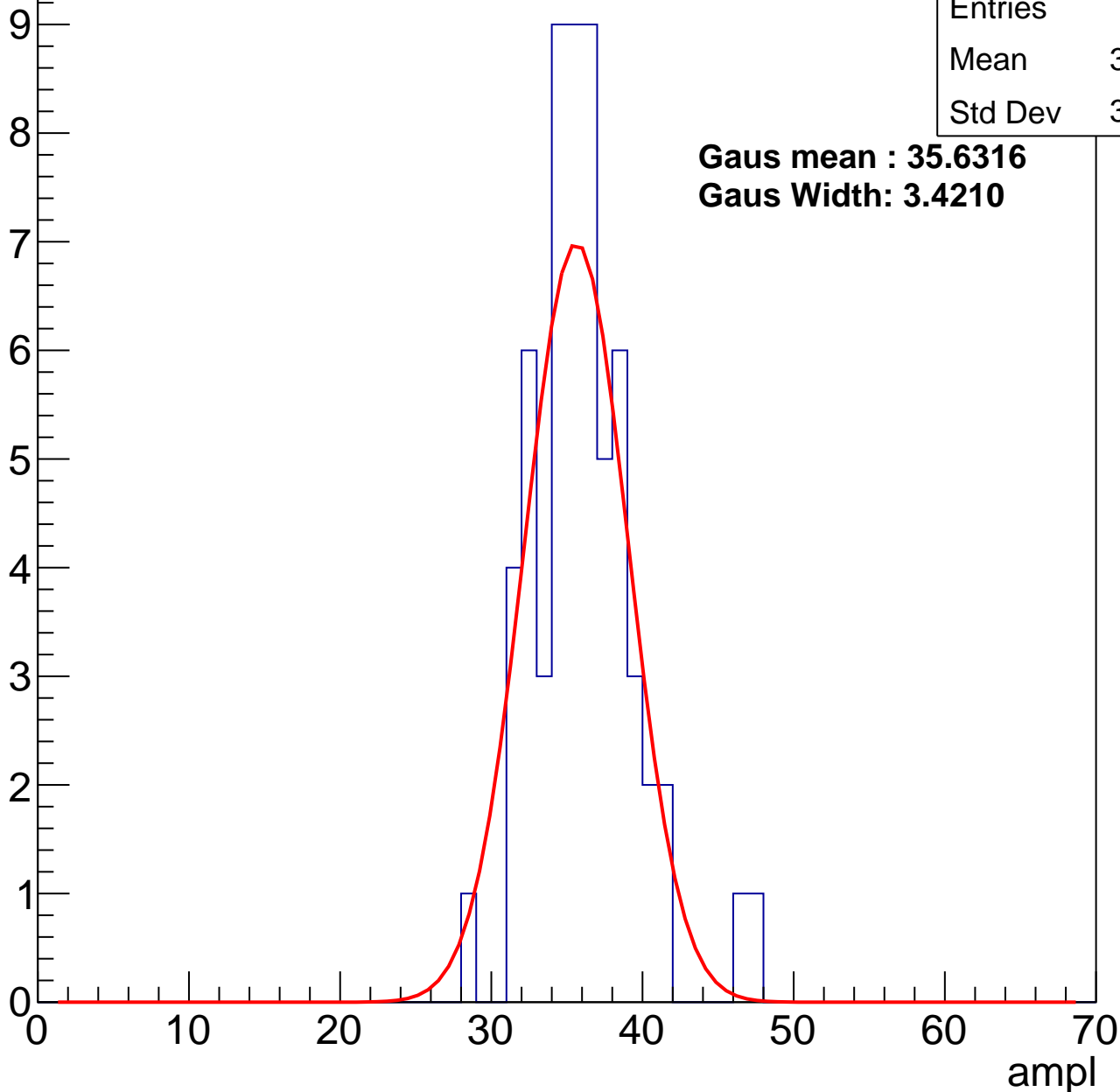
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	35.62
Std Dev	3.345

**Gaus mean : 35.6316**

**Gaus Width: 3.4210**



# B1L003S, U3-ch41, adc2

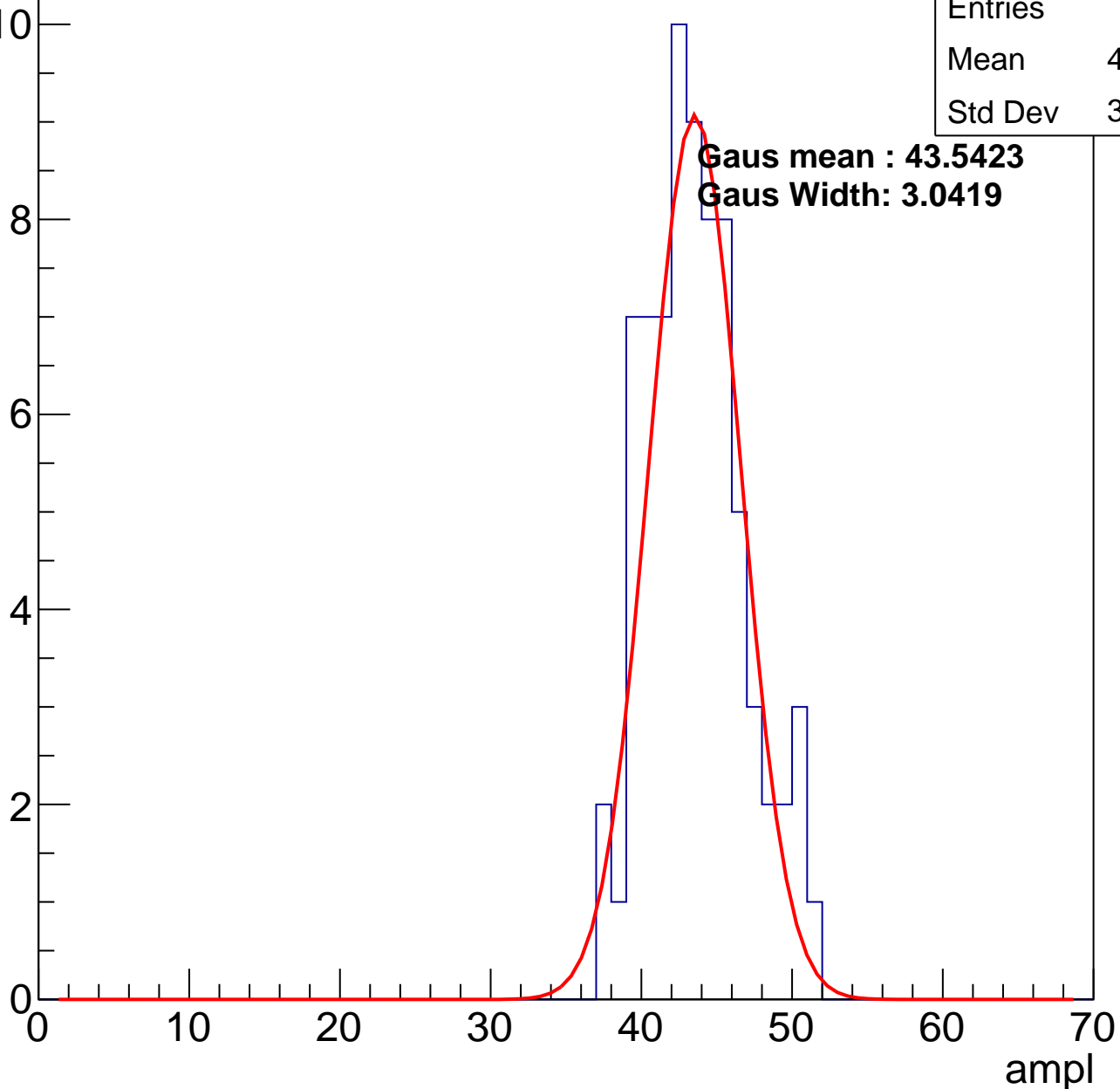
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	75
Mean	43.16
Std Dev	3.213

**Gaus mean : 43.5423**

**Gaus Width: 3.0419**

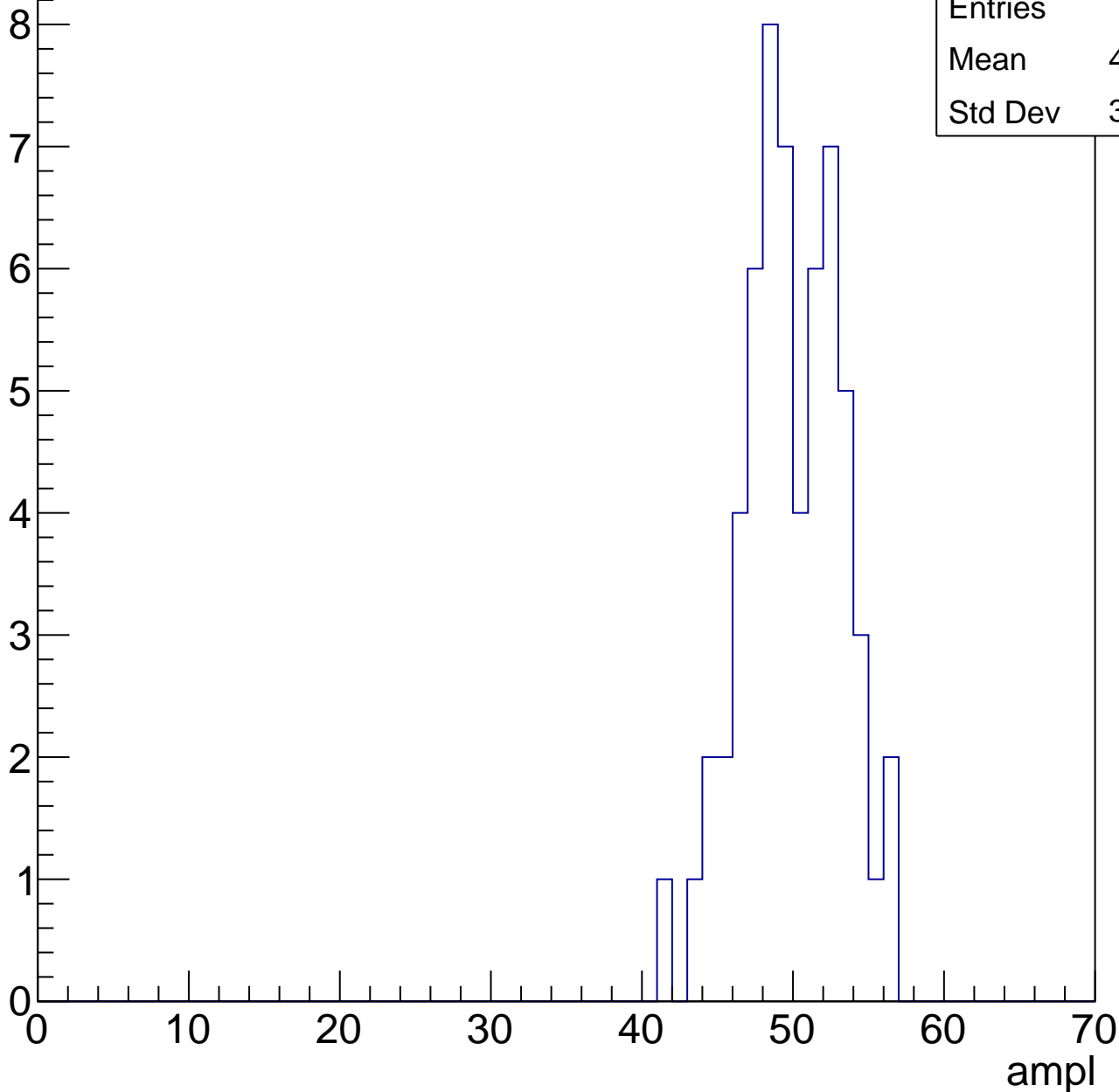


# B1L003S, U3-ch41, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	49.47
Std Dev	3.233



# B1L003S, U3-ch41, adc4

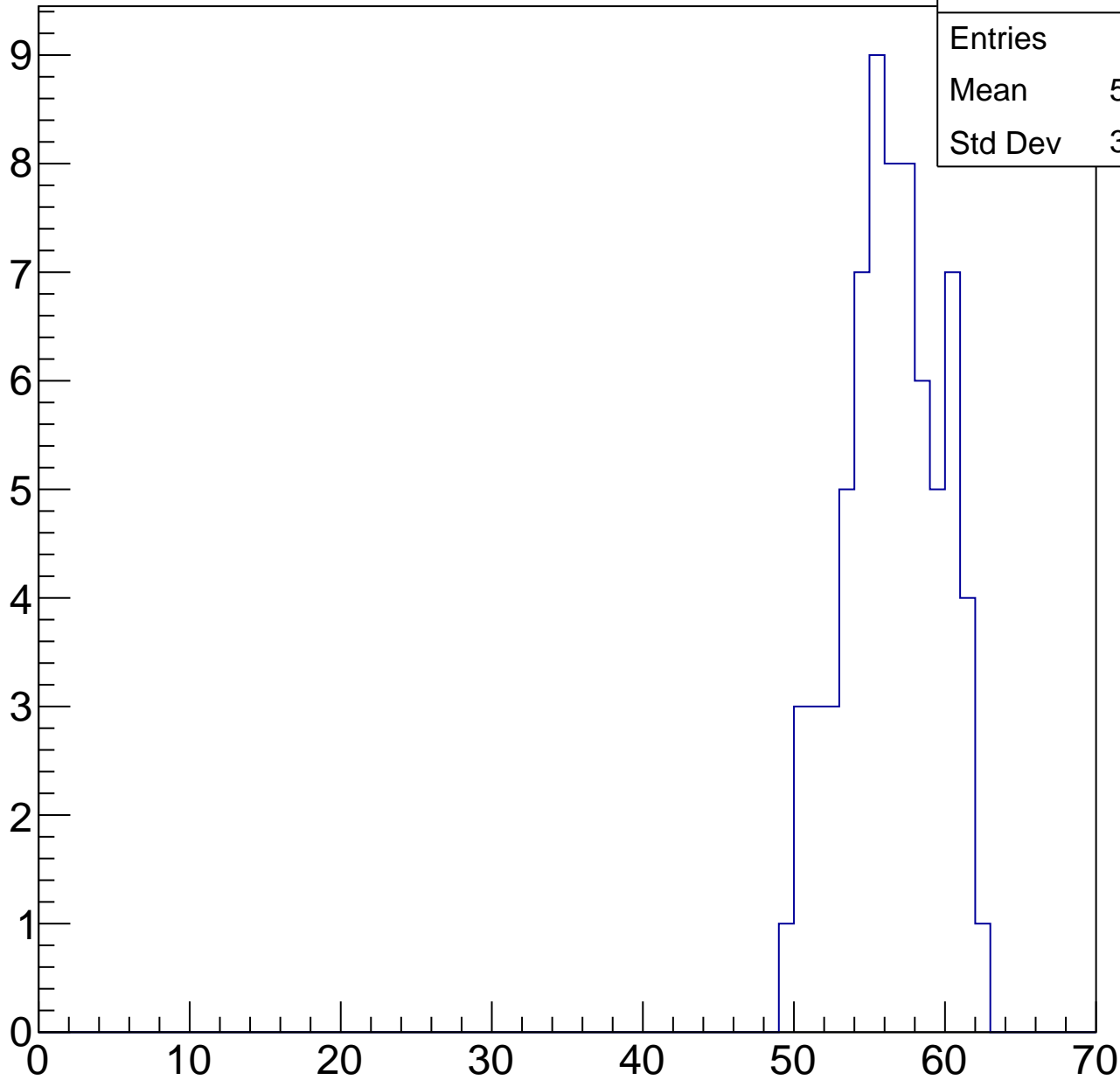
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	70
Mean	55.99
Std Dev	3.133

ampl

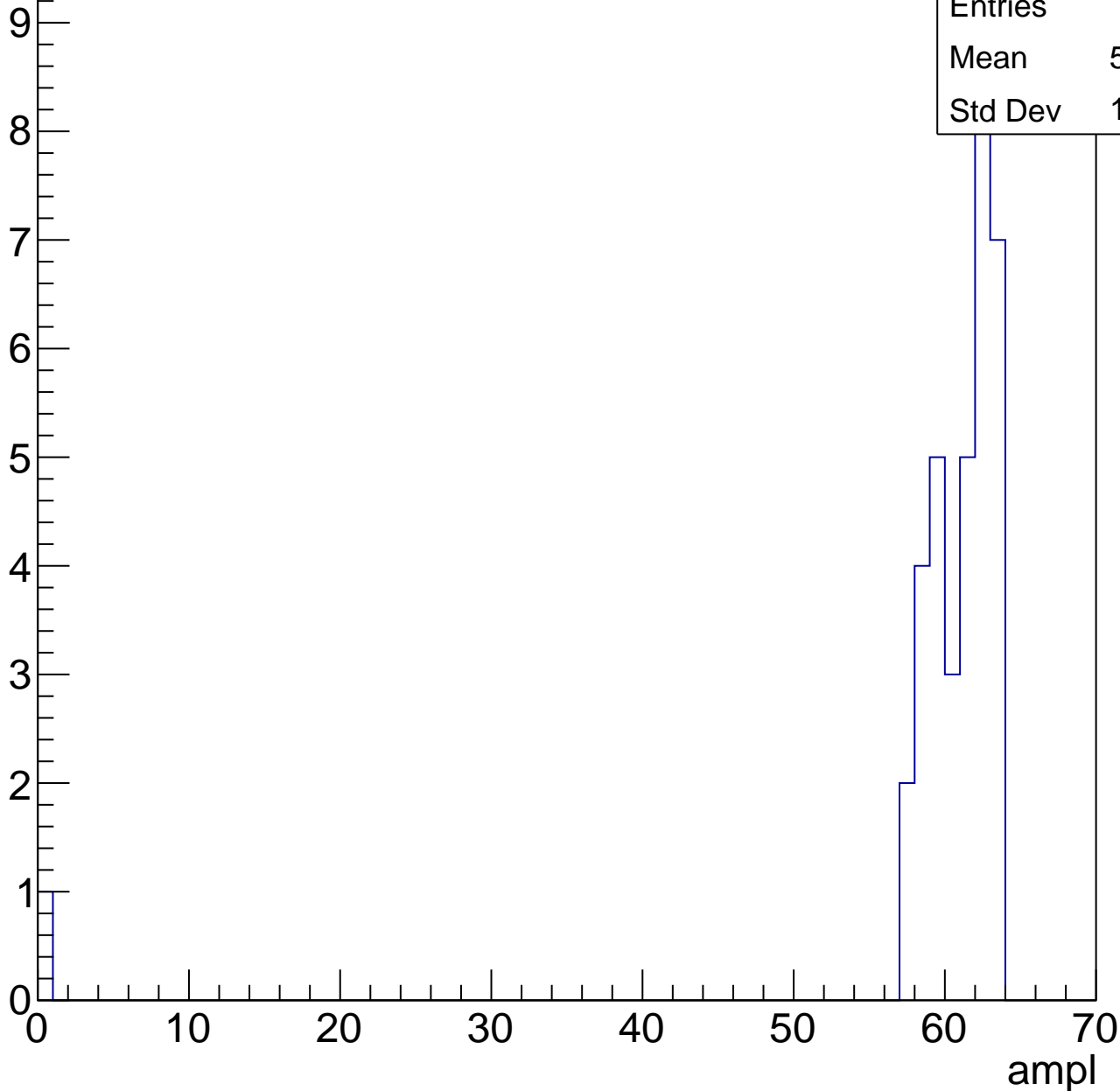


# B1L003S, U3-ch41, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	36
Mean	59.03
Std Dev	10.15



# B1L003S, U3-ch41, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch41, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U3-ch42, adc0

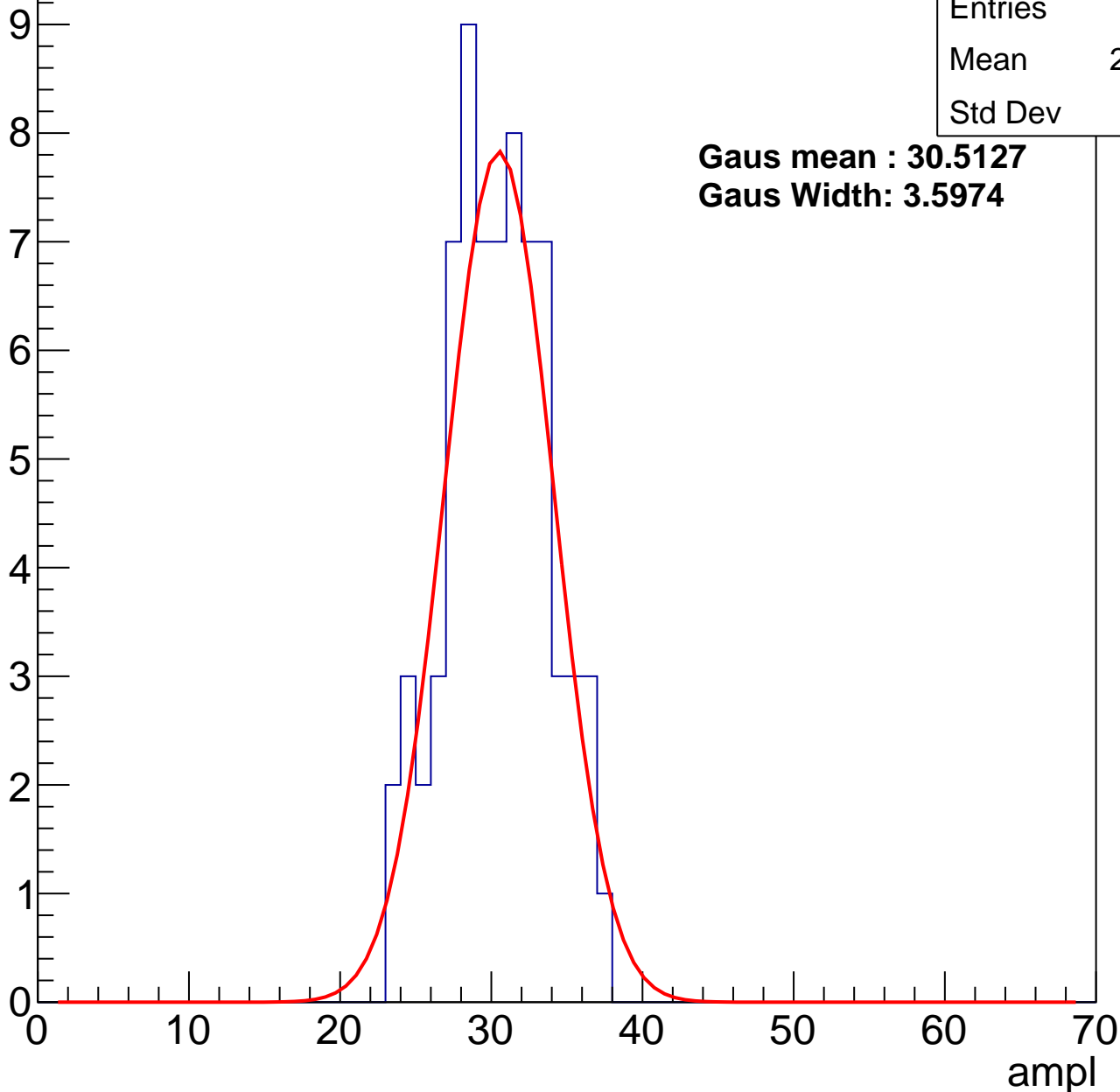
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	72
Mean	29.93
Std Dev	3.31

**Gaus mean : 30.5127**

**Gaus Width: 3.5974**



# B1L003S, U3-ch42, adc1

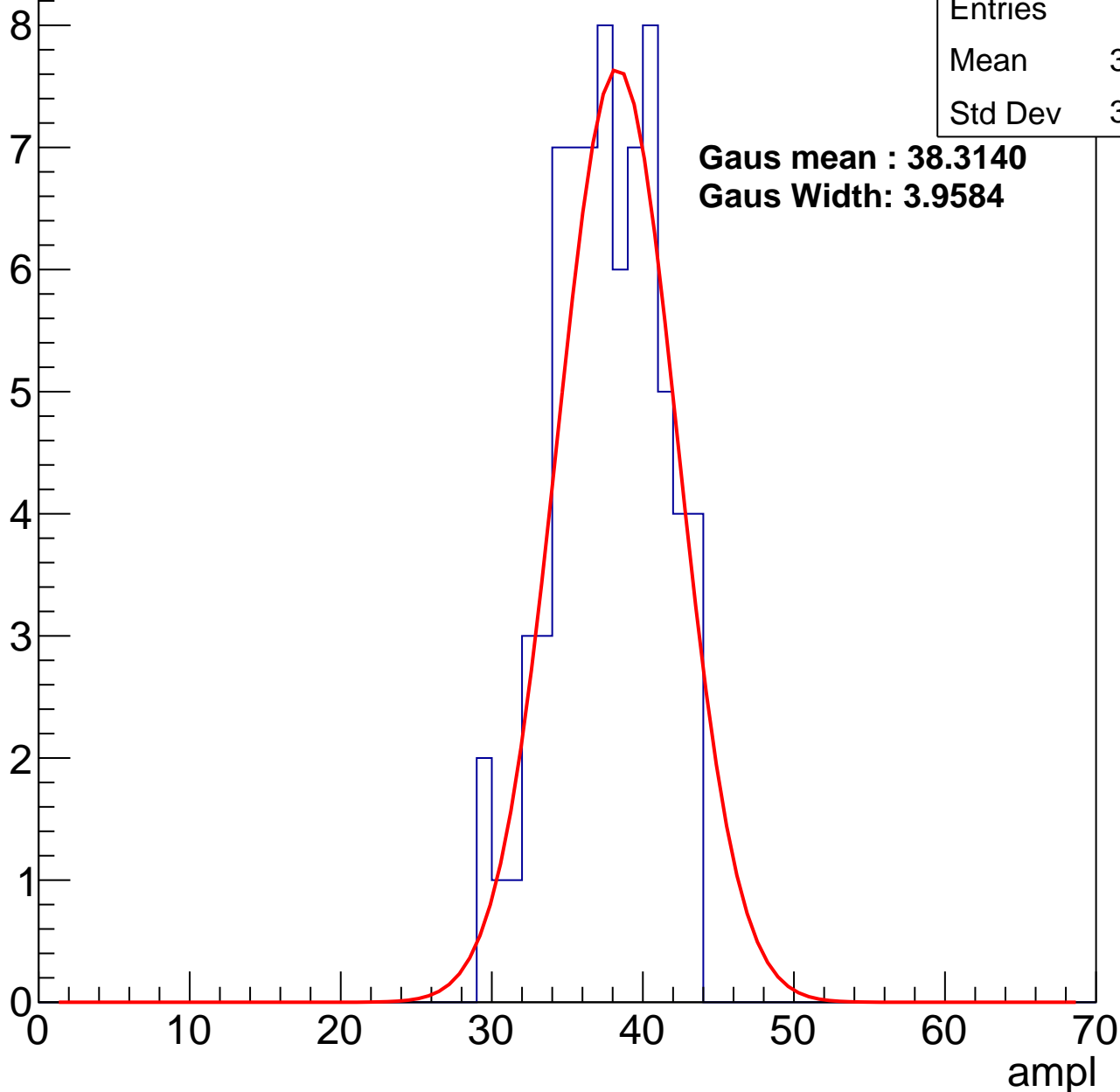
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	73
Mean	37.14
Std Dev	3.438

**Gaus mean : 38.3140**

**Gaus Width: 3.9584**



# B1L003S, U3-ch42, adc2

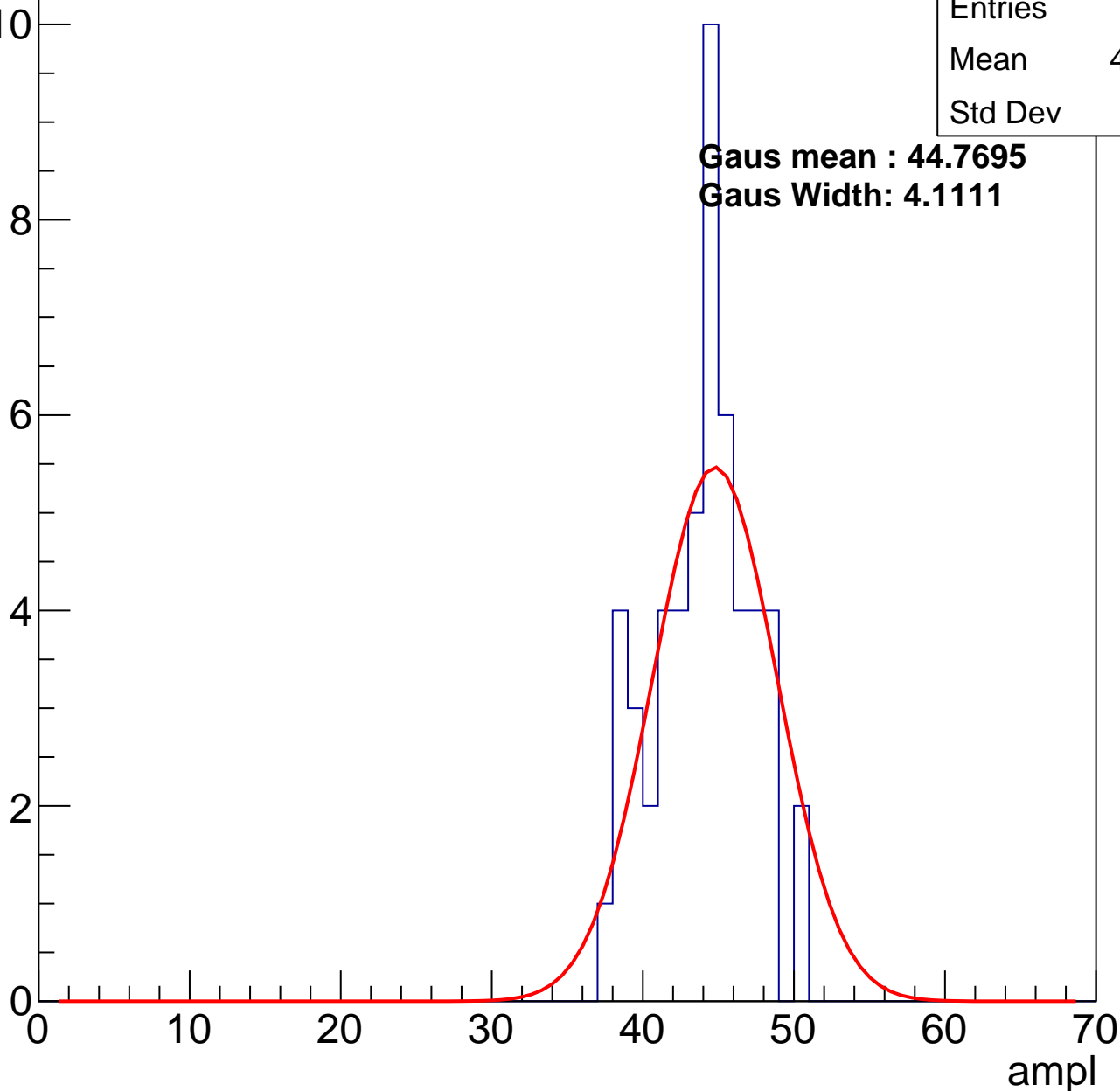
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	43.53
Std Dev	3.19

**Gaus mean : 44.7695**

**Gaus Width: 4.1111**



# B1L003S, U3-ch42, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

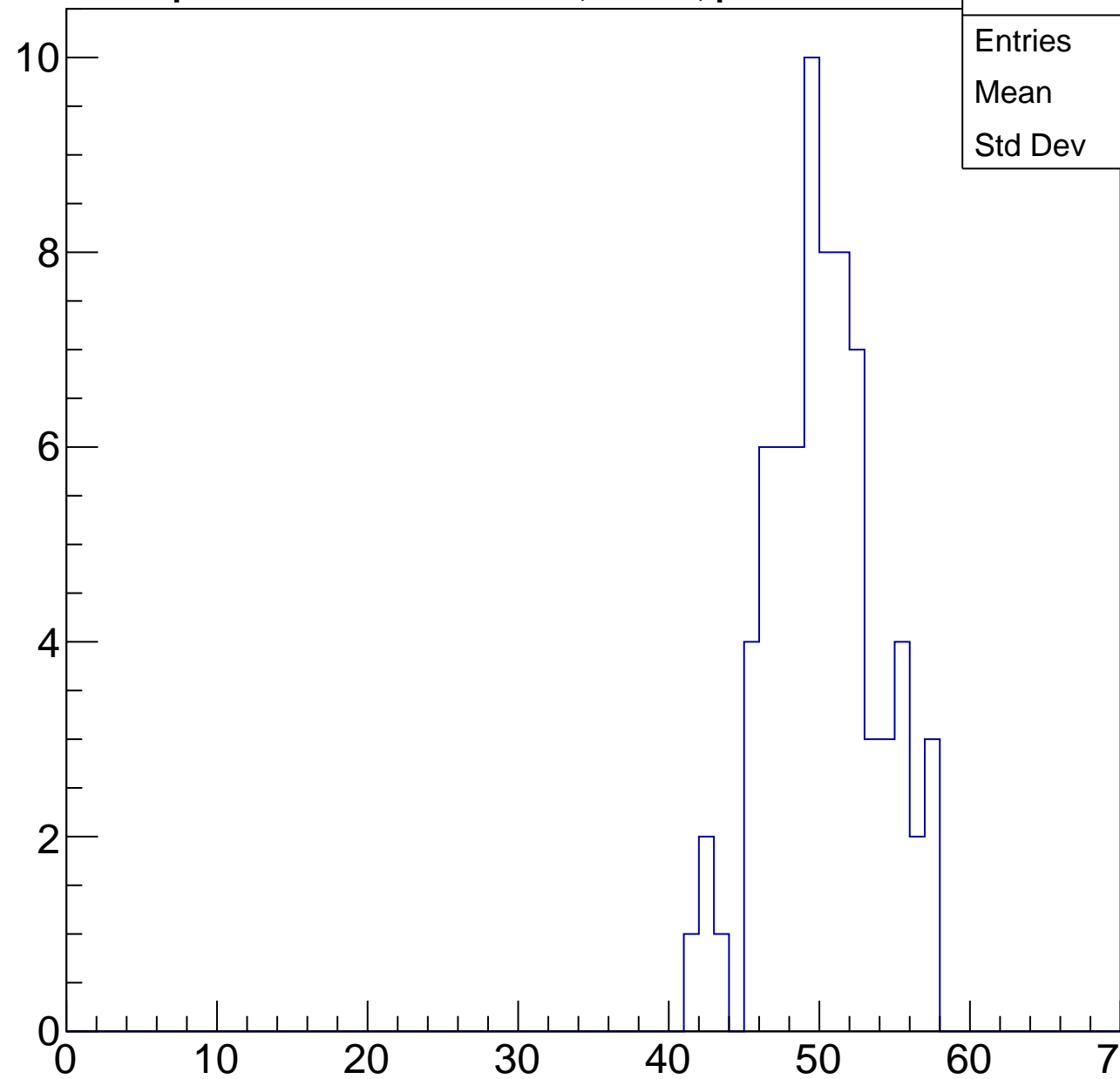
Entries	74
Mean	49.73
Std Dev	3.614

Entry

10  
8  
6  
4  
2  
0

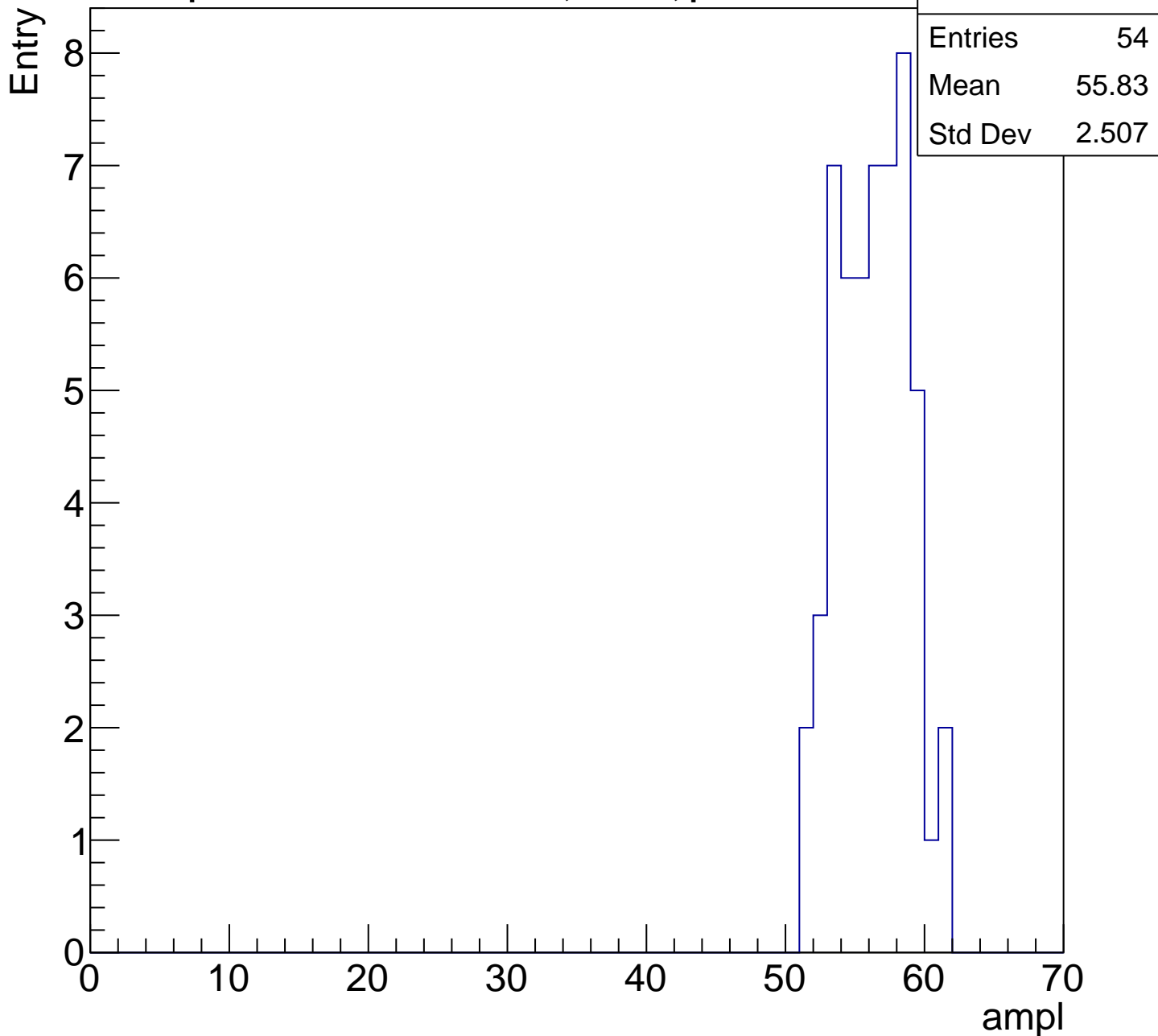
0 10 20 30 40 50 60 70

ampl



# B1L003S, U3-ch42, adc4

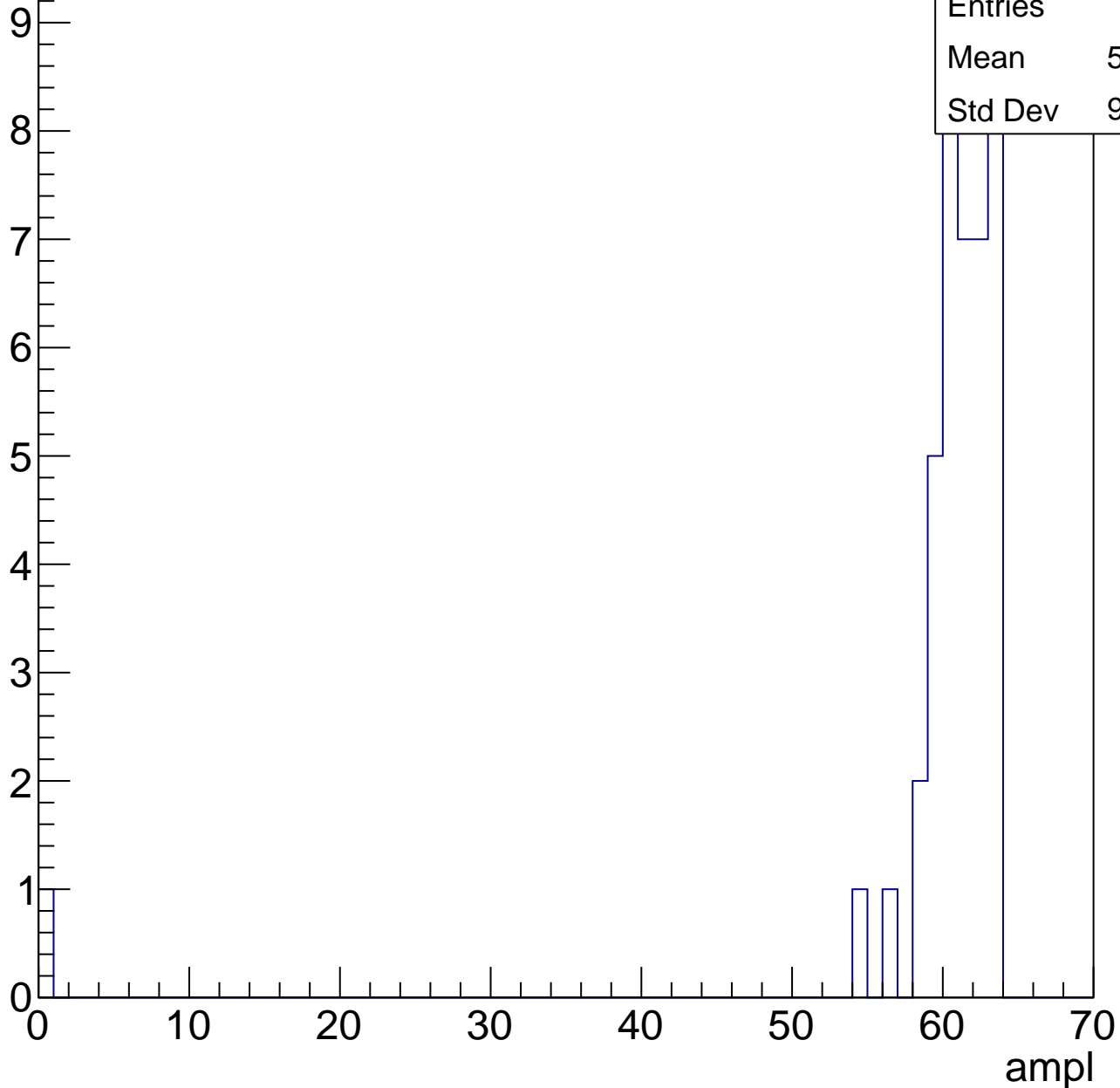
calib\_packv5\_042523\_0143.root, FC#13, port D2



# B1L003S, U3-ch42, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U3-ch42, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch42, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U3-ch43, adc0

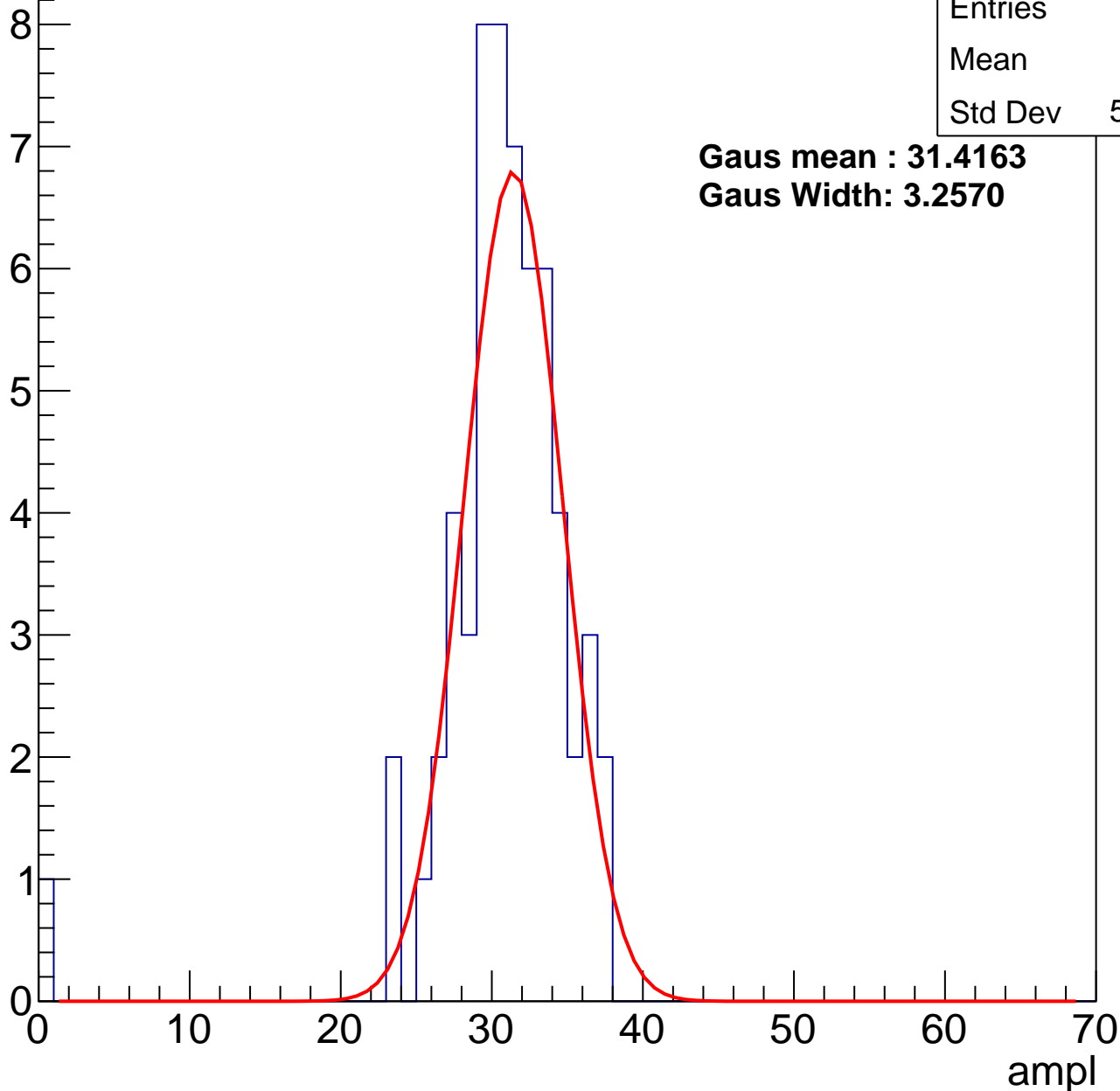
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	30.2
Std Dev	5.065

**Gaus mean : 31.4163**

**Gaus Width: 3.2570**



# B1L003S, U3-ch43, adc1

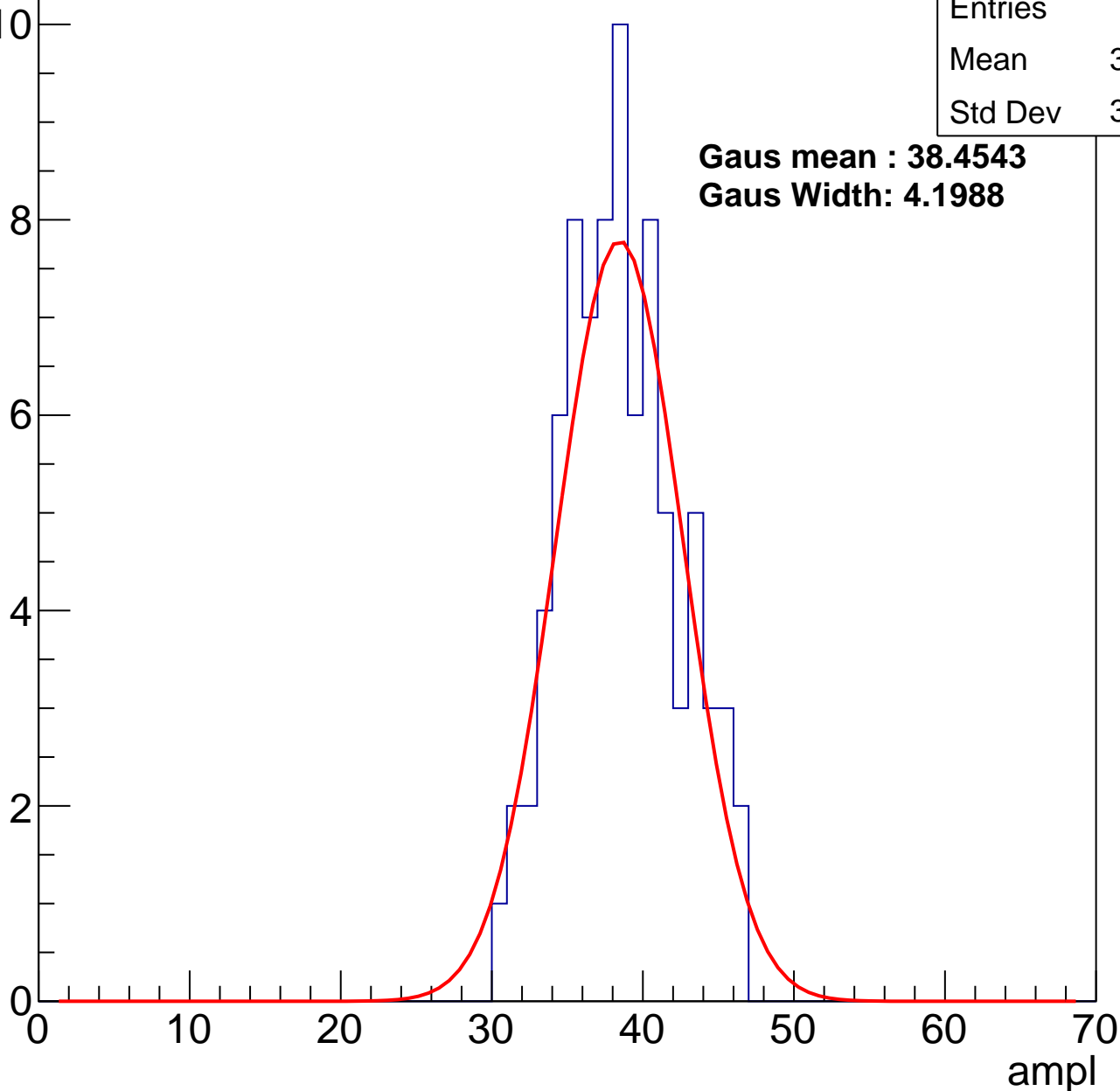
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	83
Mean	38.06
Std Dev	3.765

**Gaus mean : 38.4543**

**Gaus Width: 4.1988**



# B1L003S, U3-ch43, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	67
Mean	45.13
Std Dev	3.472

**Gaus mean : 45.0971**

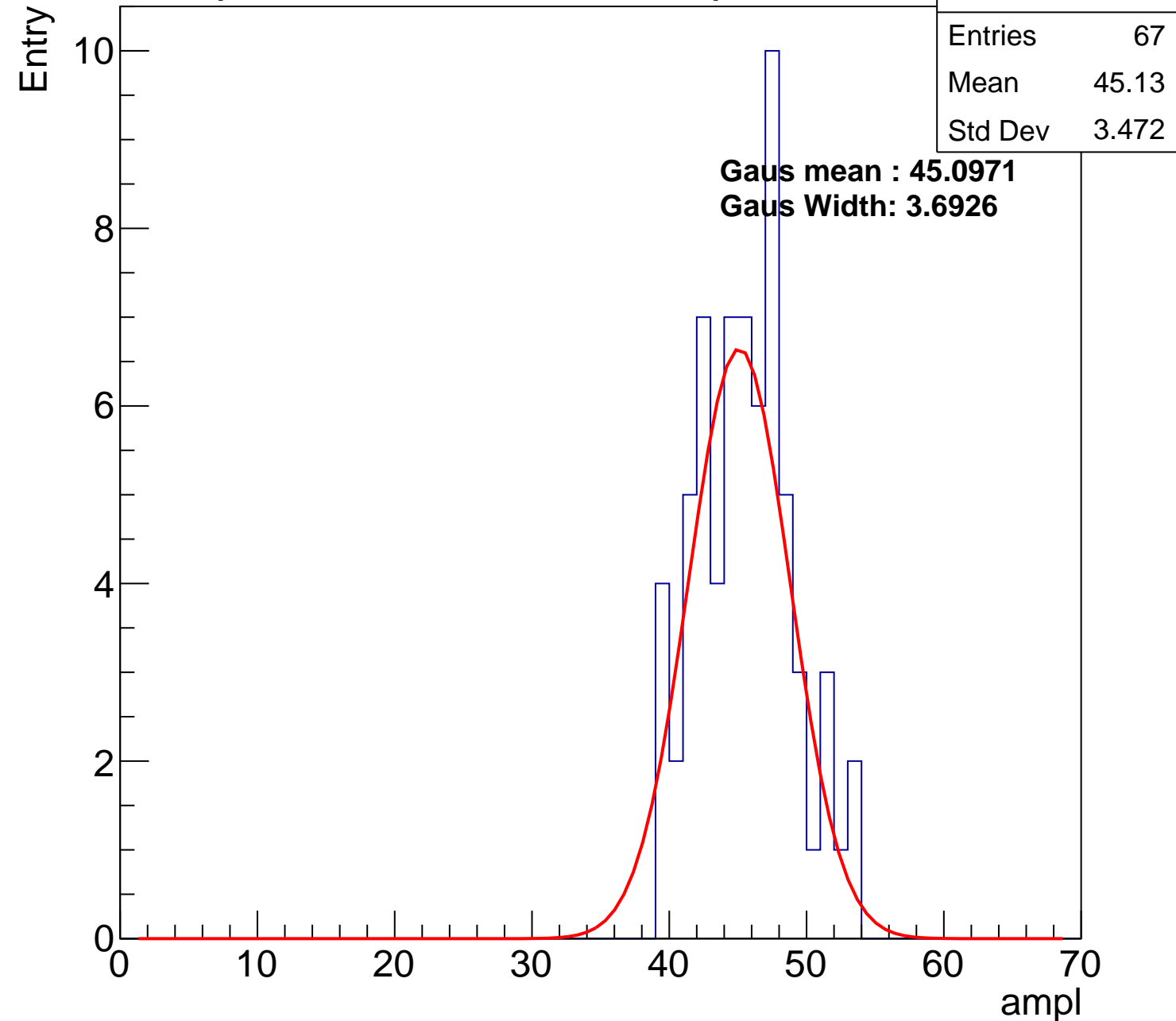
**Gaus Width: 3.6926**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

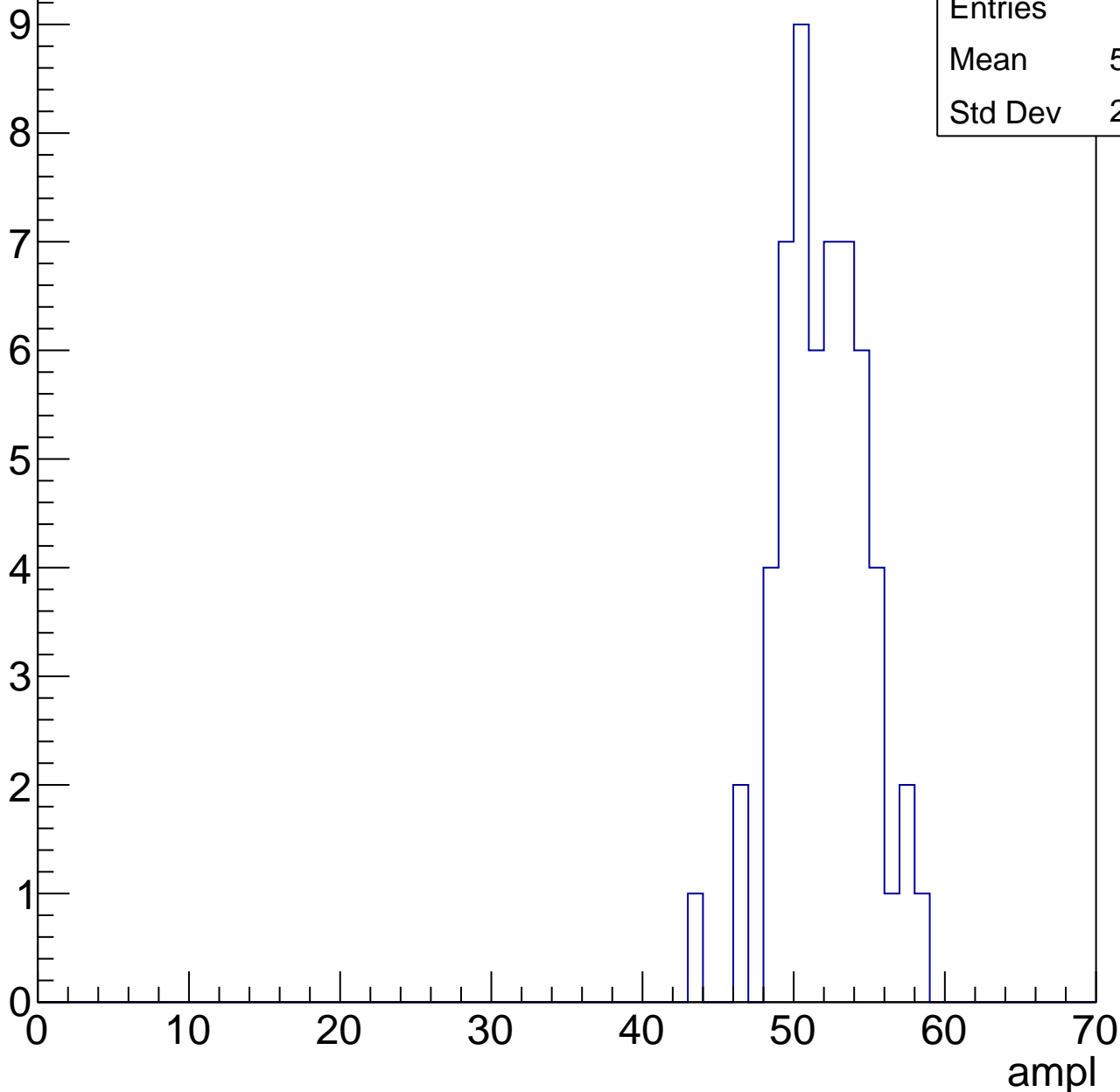


# B1L003S, U3-ch43, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	51.46
Std Dev	2.884

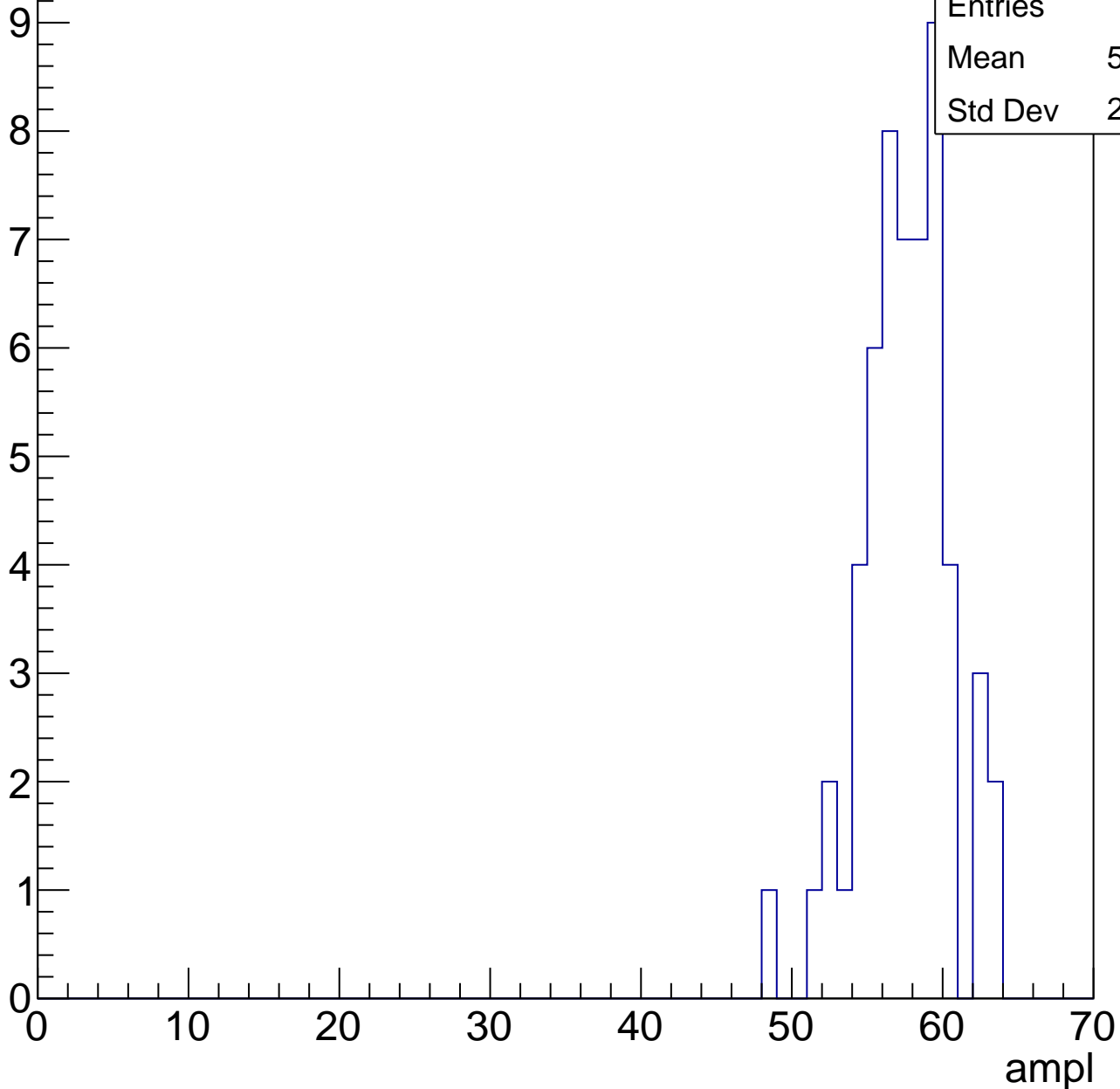


# B1L003S, U3-ch43, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	57.05
Std Dev	2.944

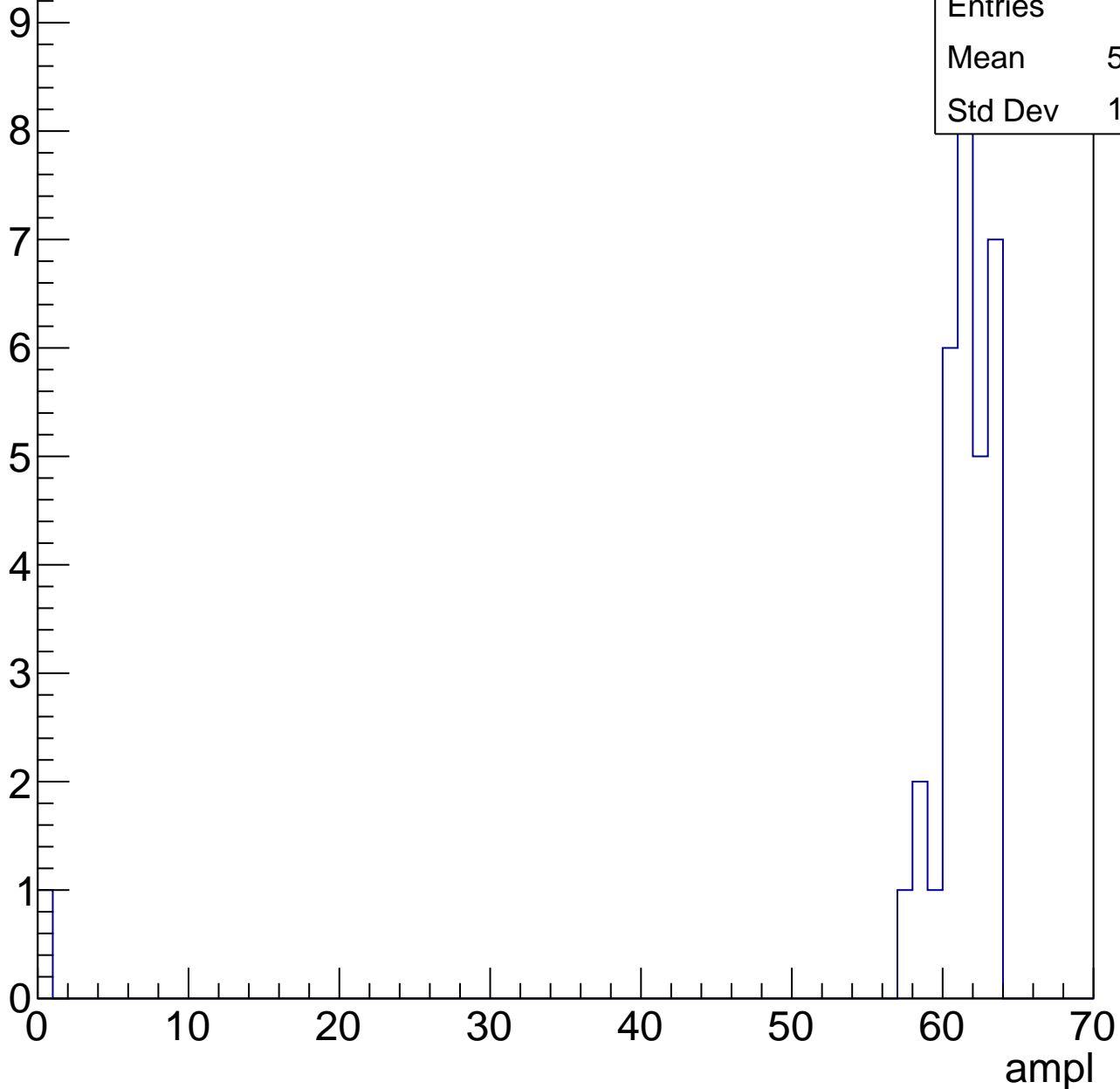


# B1L003S, U3-ch43, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

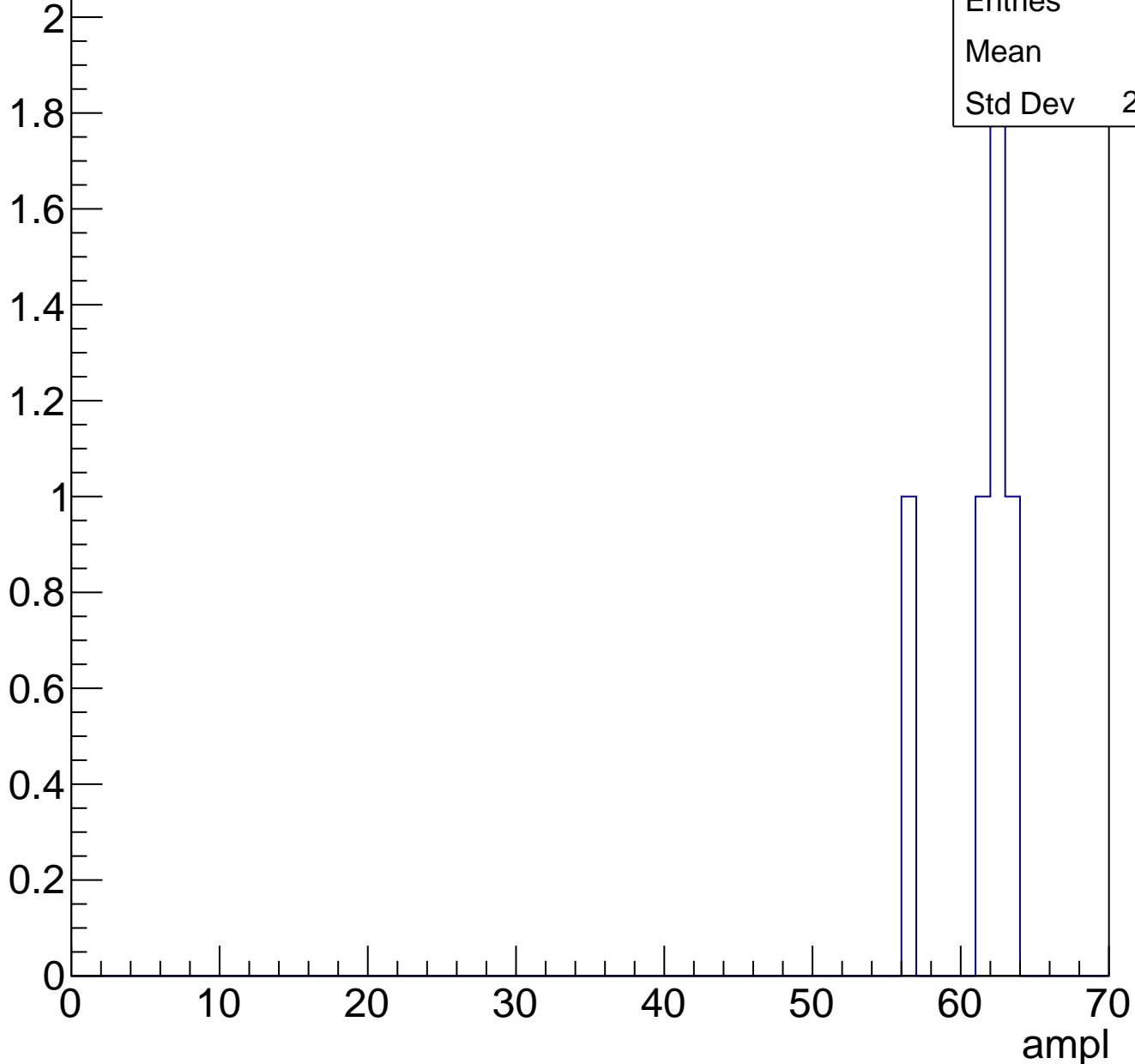
Entries	32
Mean	59.12
Std Dev	10.73



# B1L003S, U3-ch43, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch43, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U3-ch44, adc0

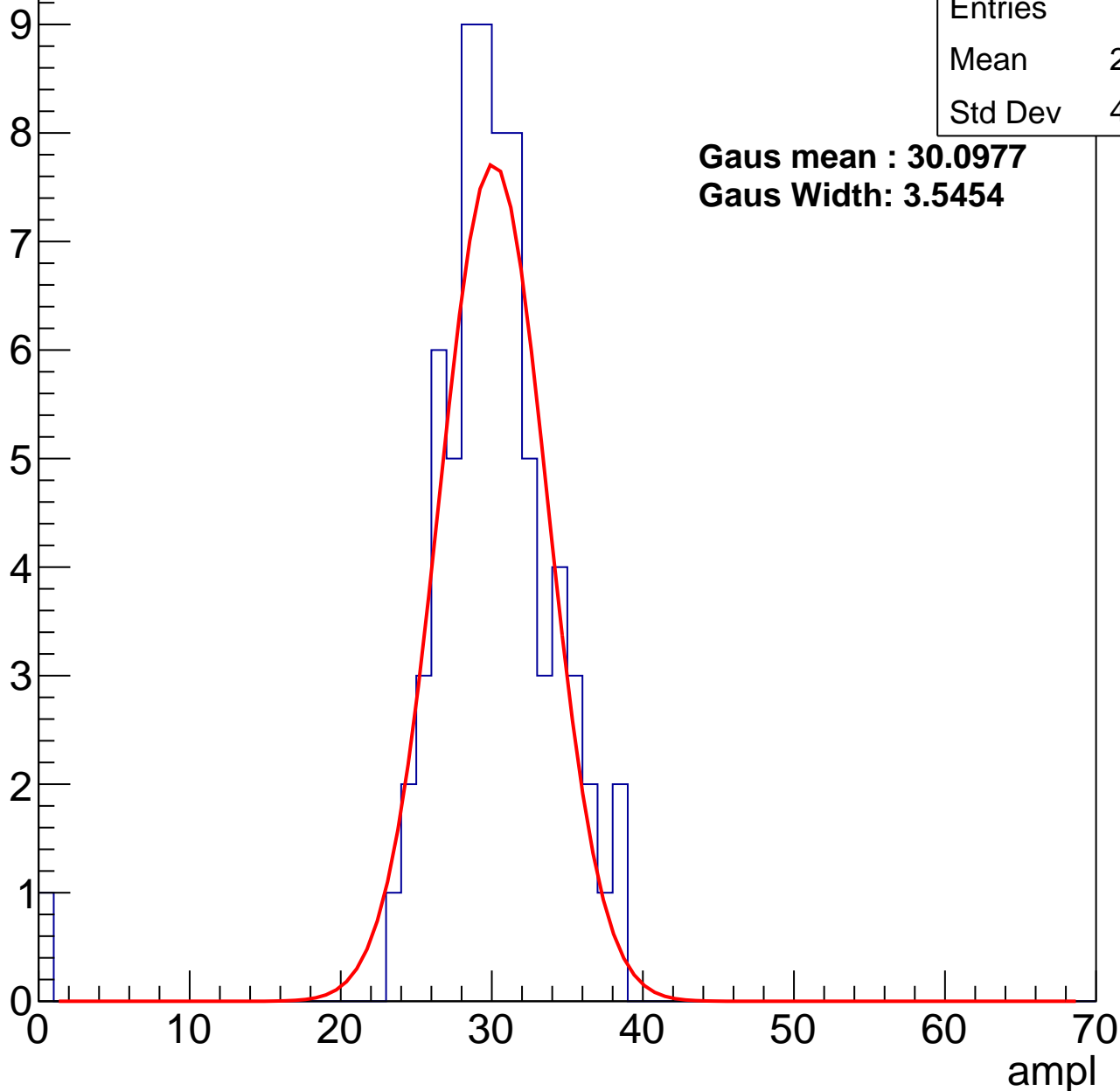
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	72
Mean	29.49
Std Dev	4.868

**Gaus mean : 30.0977**

**Gaus Width: 3.5454**



# B1L003S, U3-ch44, adc1

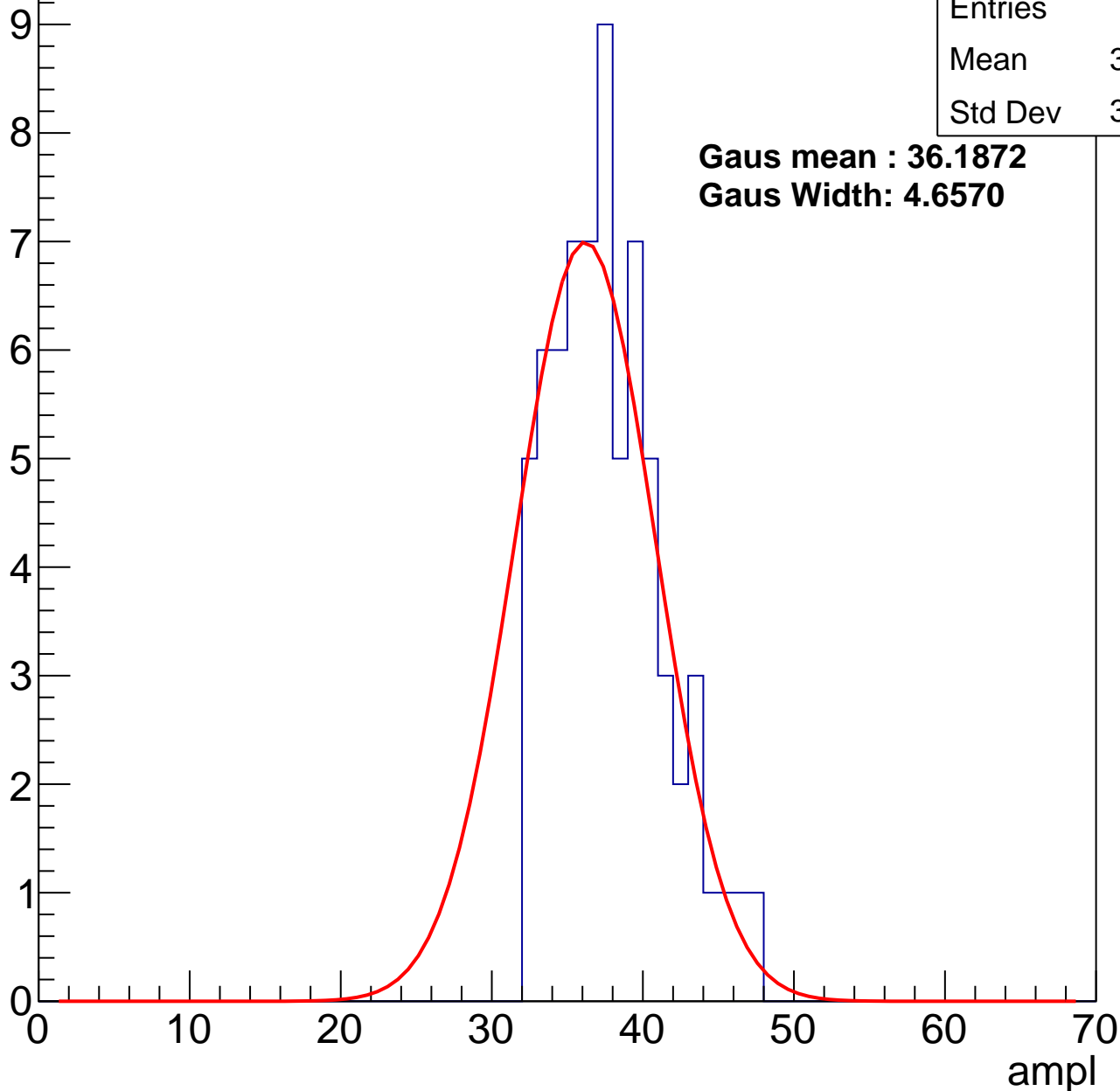
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	37.29
Std Dev	3.576

**Gaus mean : 36.1872**

**Gaus Width: 4.6570**



# B1L003S, U3-ch44, adc2

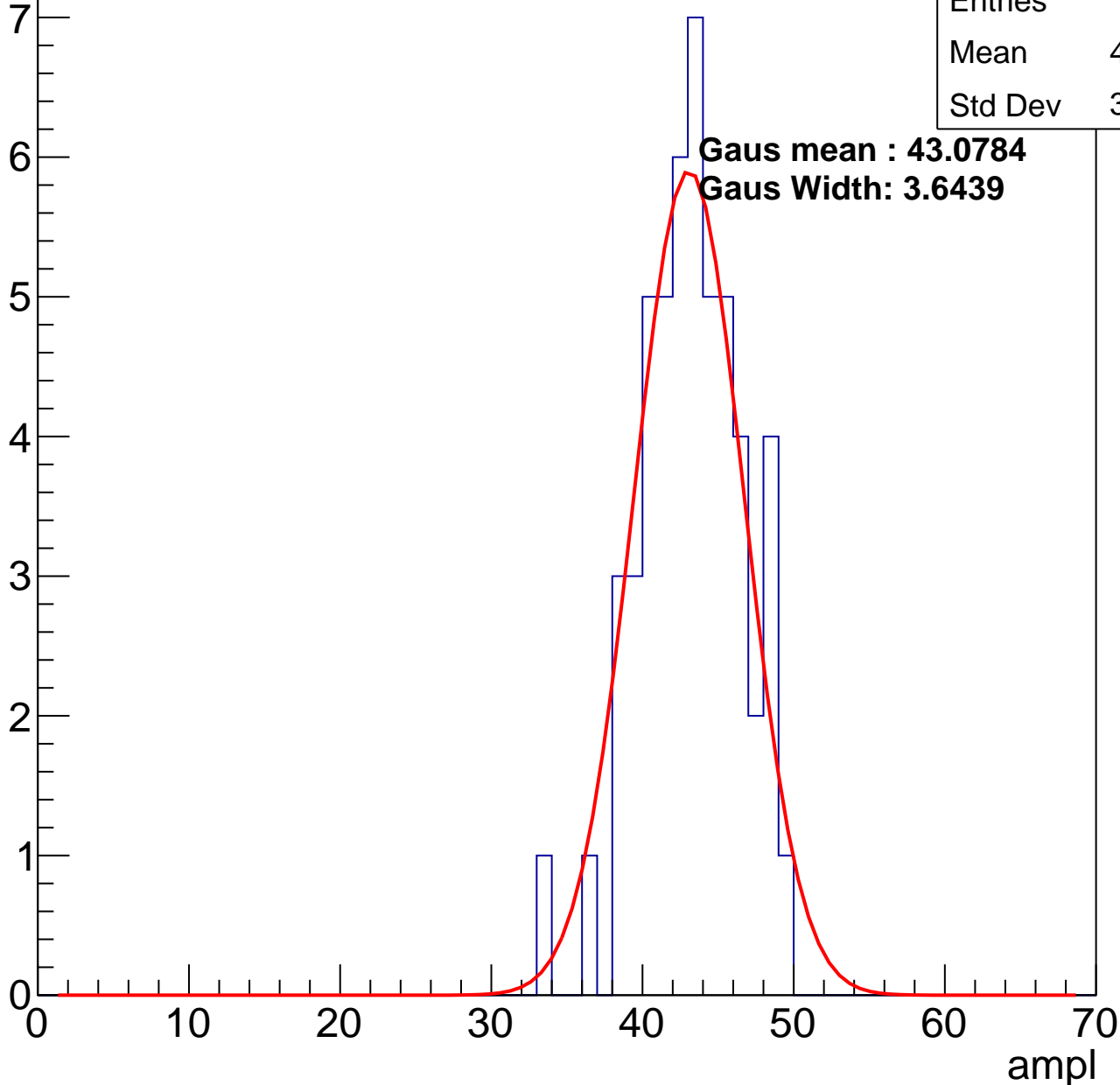
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	52
Mean	42.73
Std Dev	3.306

**Gaus mean : 43.0784**

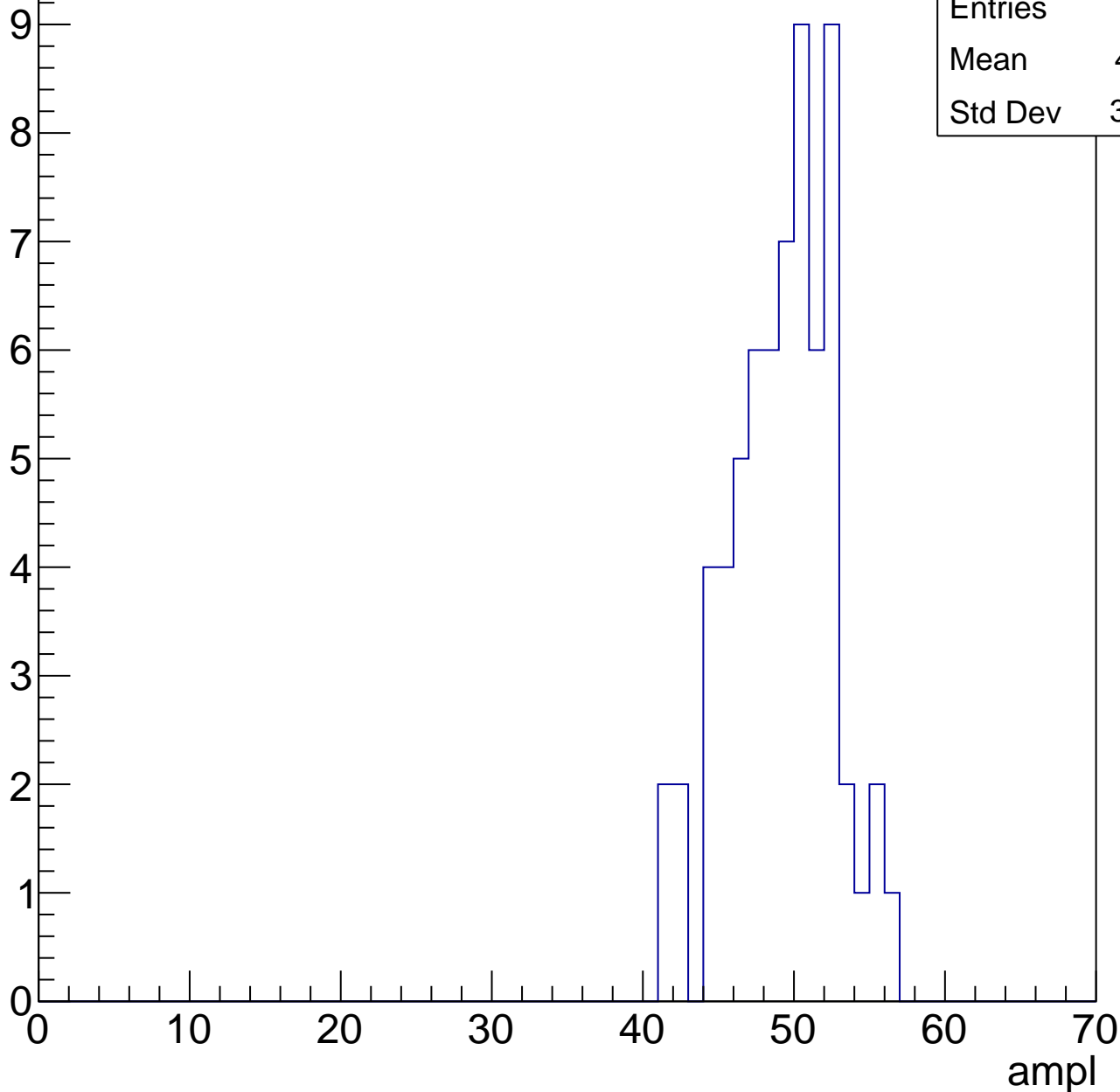
**Gaus Width: 3.6439**



# B1L003S, U3-ch44, adc3

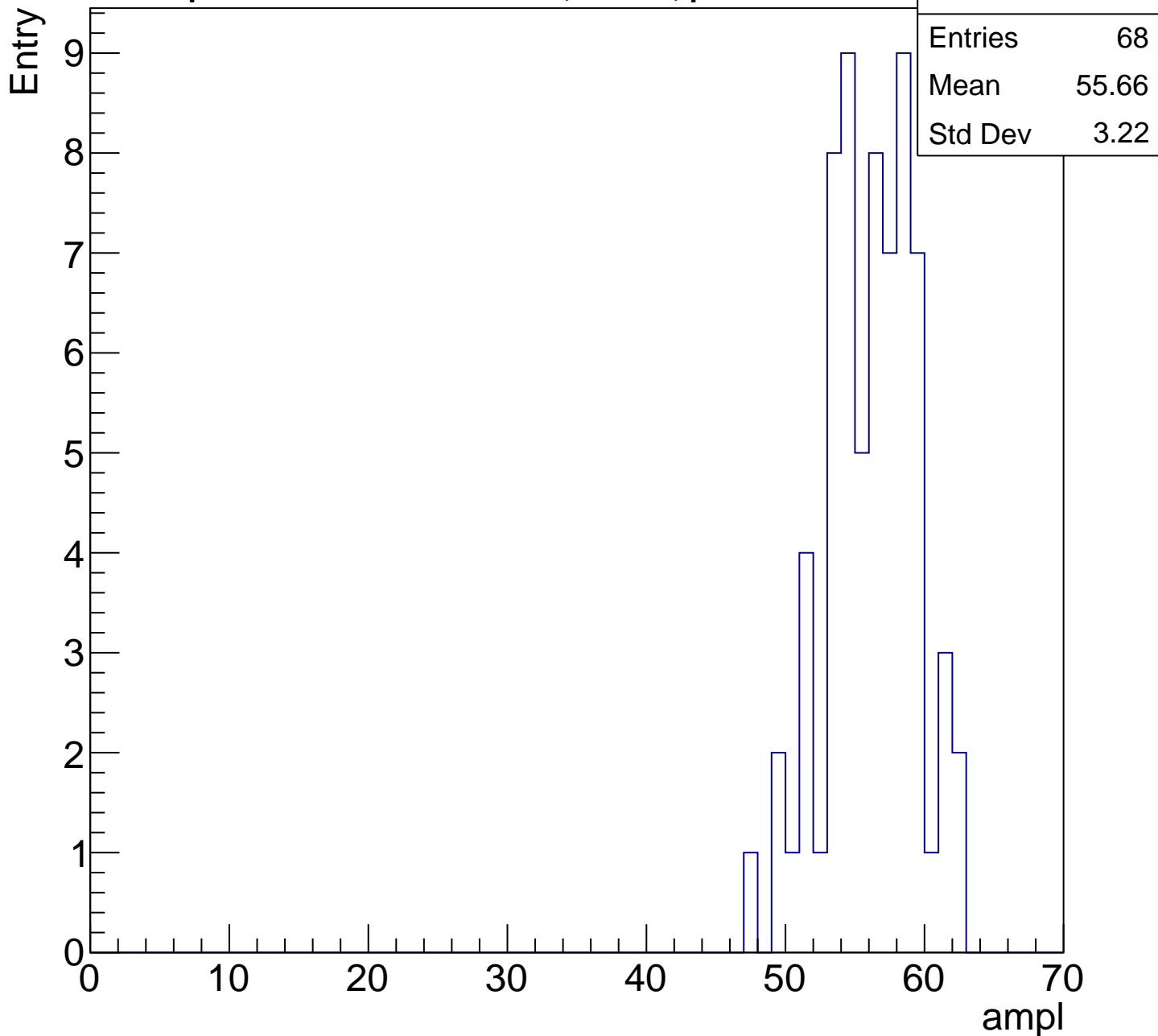
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U3-ch44, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2



# B1L003S, U3-ch44, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	43
Mean	58.88
Std Dev	9.374

ampl

0

10

20

30

40

50

60

70

# B1L003S, U3-ch44, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch44, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	23
Std Dev	0

ampl

# B1L003S, U3-ch45, adc0

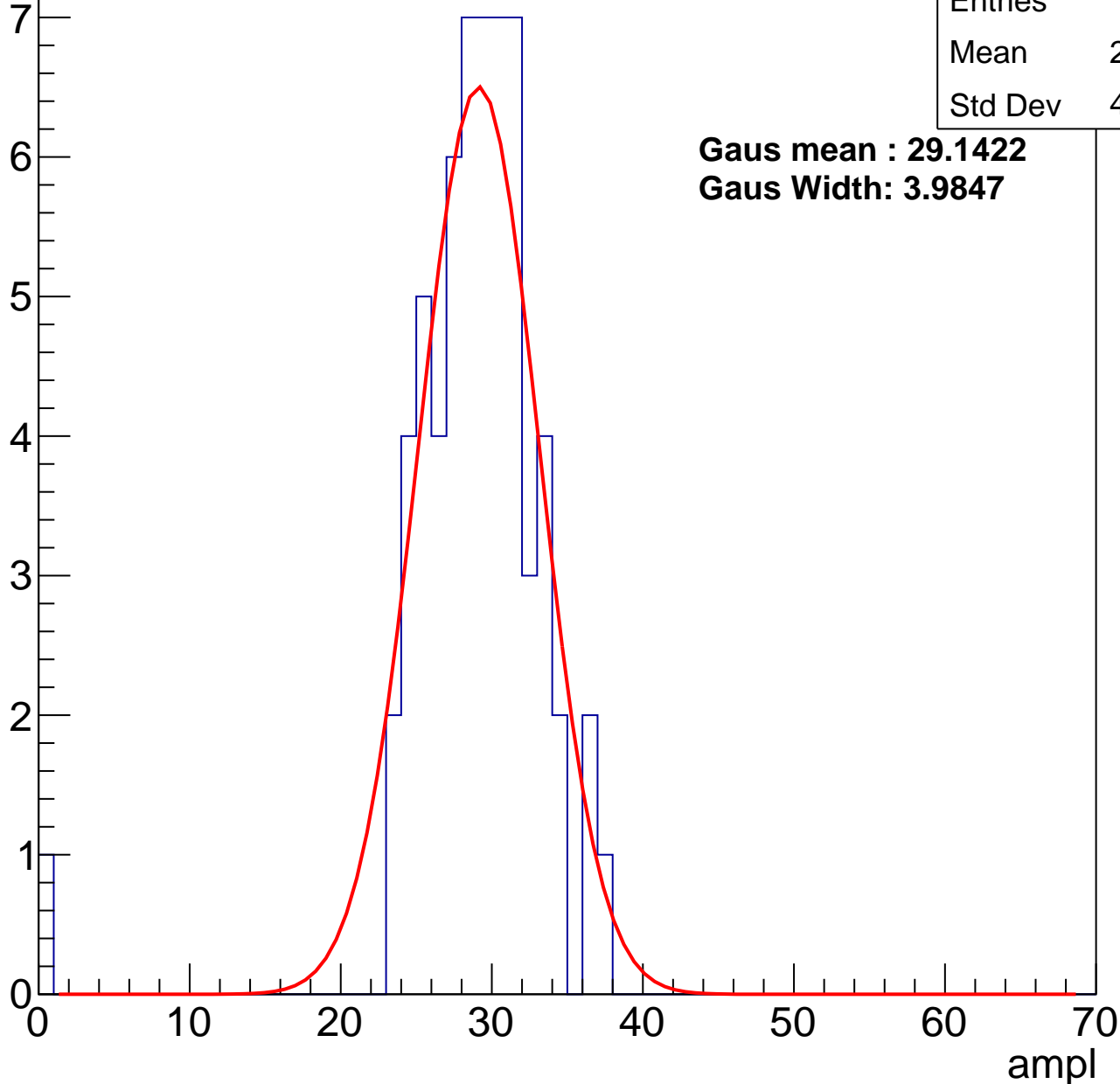
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	28.45
Std Dev	4.885

**Gaus mean : 29.1422**

**Gaus Width: 3.9847**



# B1L003S, U3-ch45, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	76
Mean	36.04
Std Dev	3.559

**Gaus mean : 36.4754**

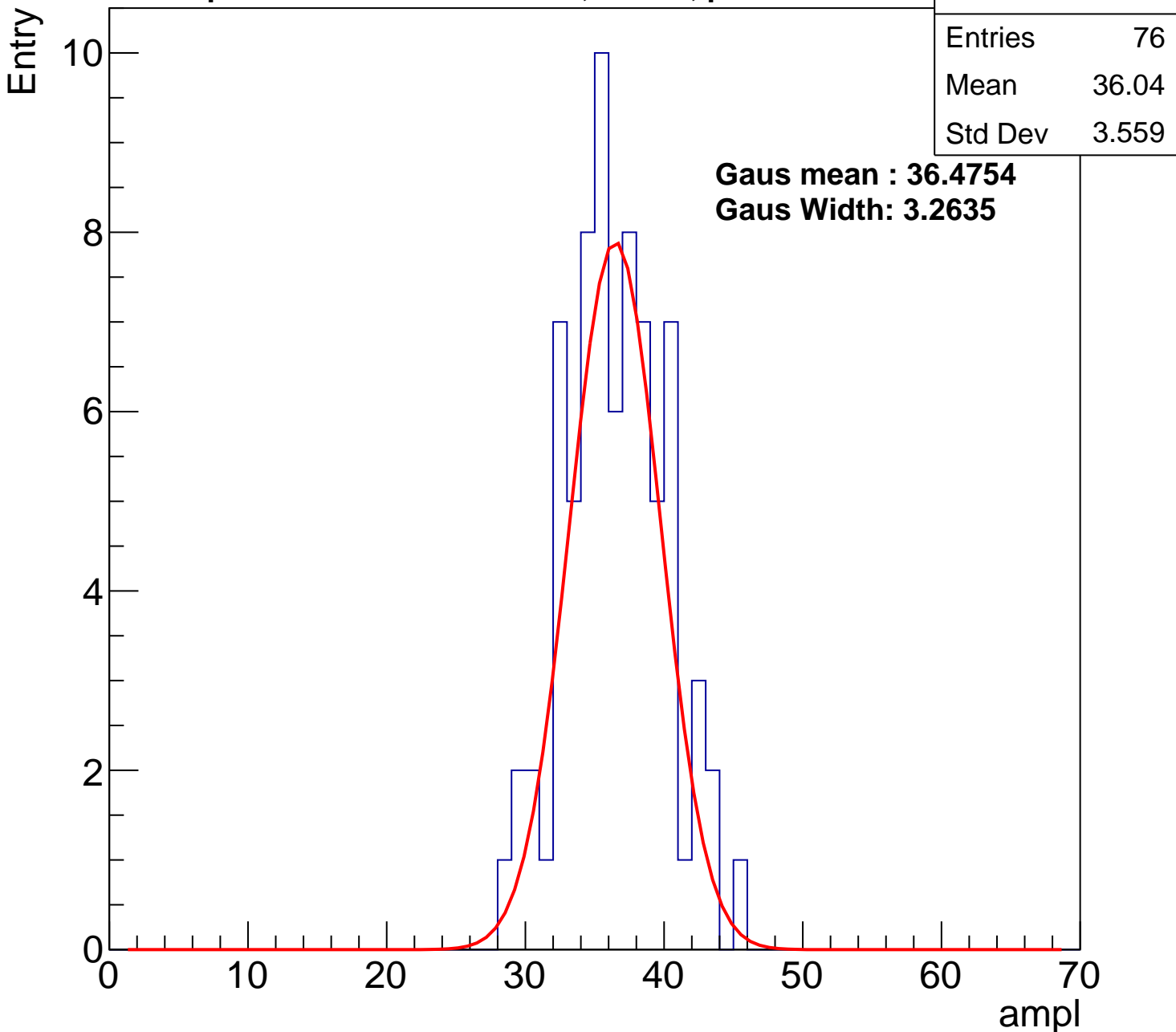
**Gaus Width: 3.2635**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L003S, U3-ch45, adc2

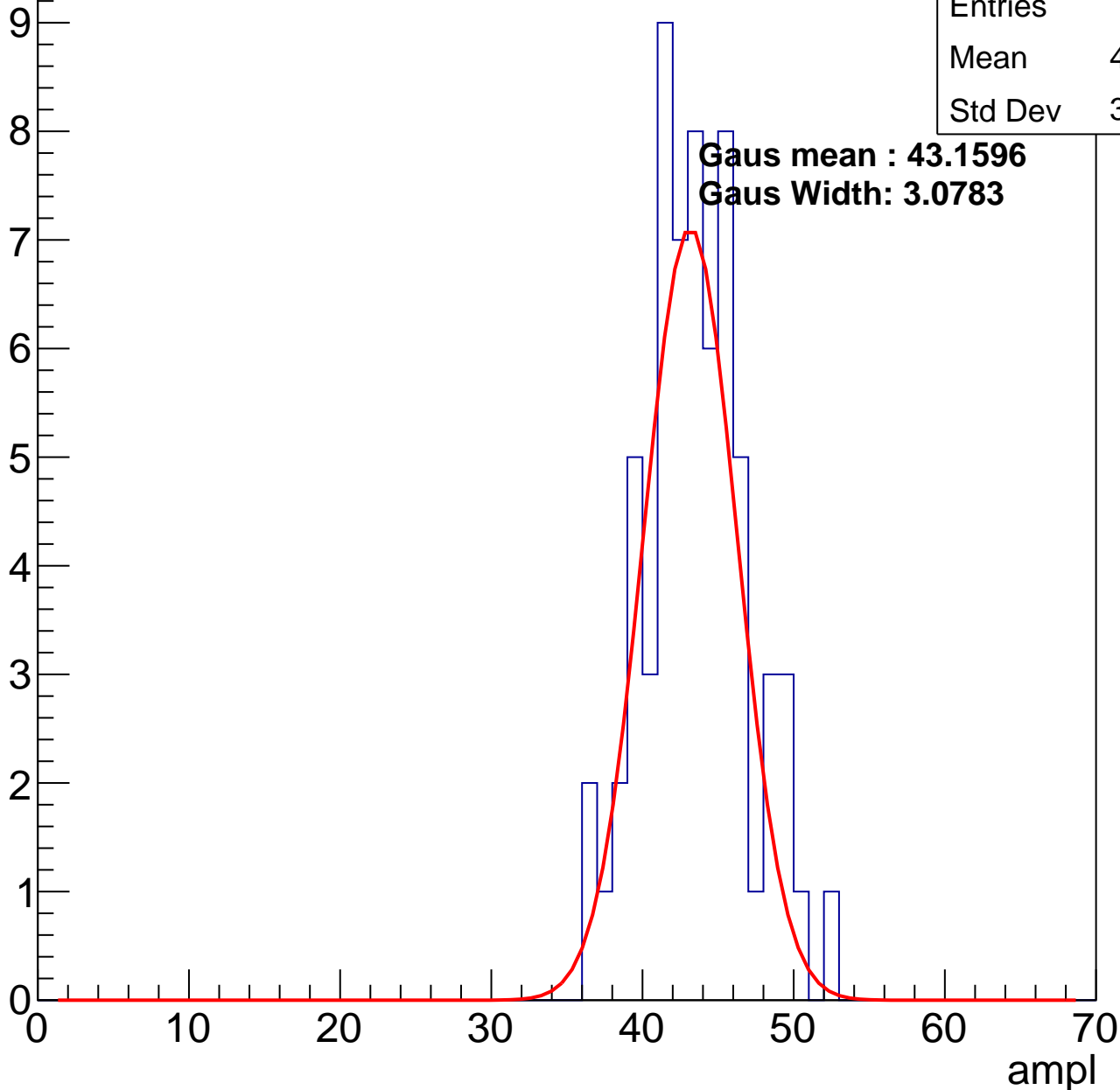
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	43.09
Std Dev	3.387

**Gaus mean : 43.1596**

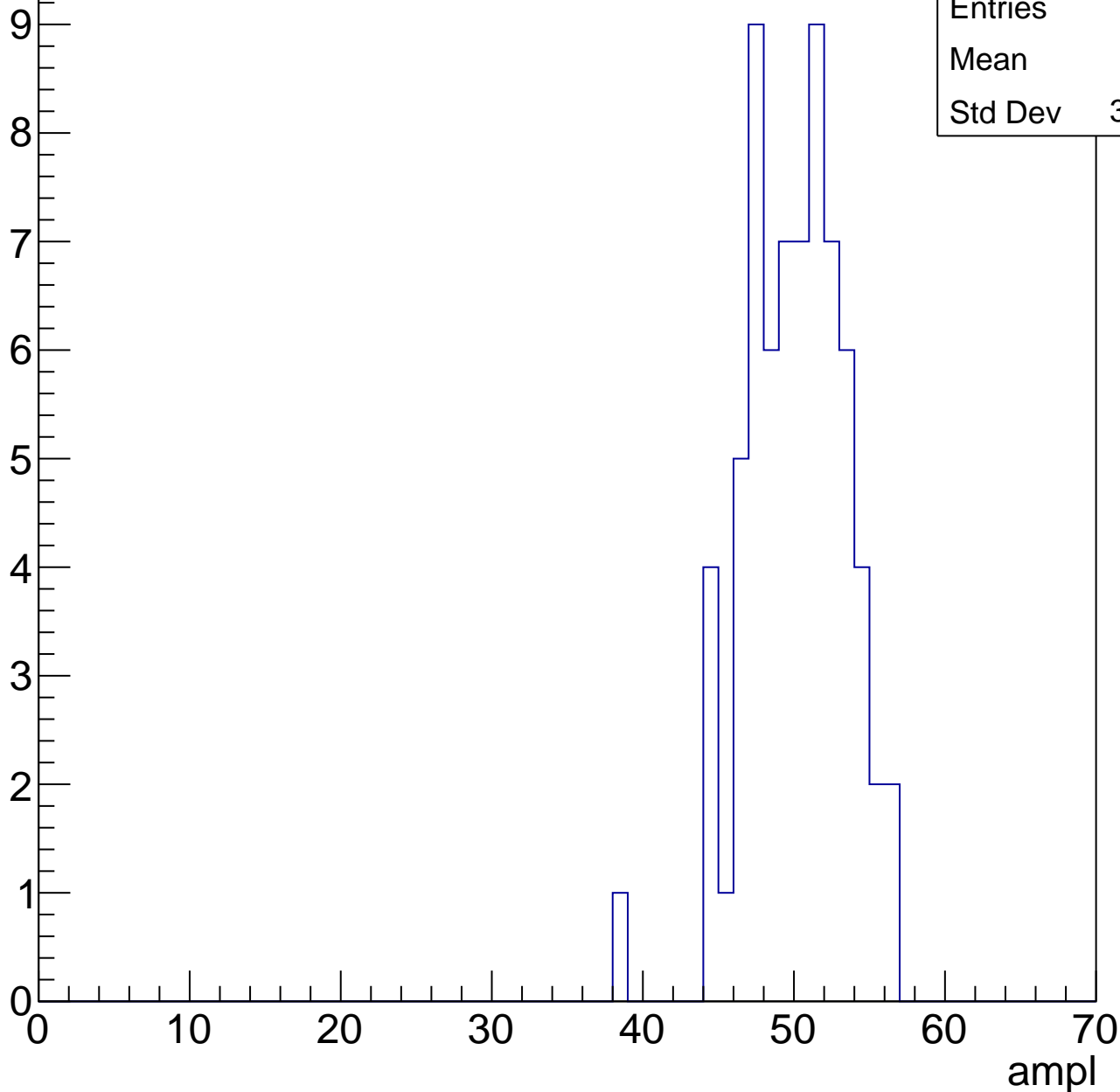
**Gaus Width: 3.0783**



# B1L003S, U3-ch45, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

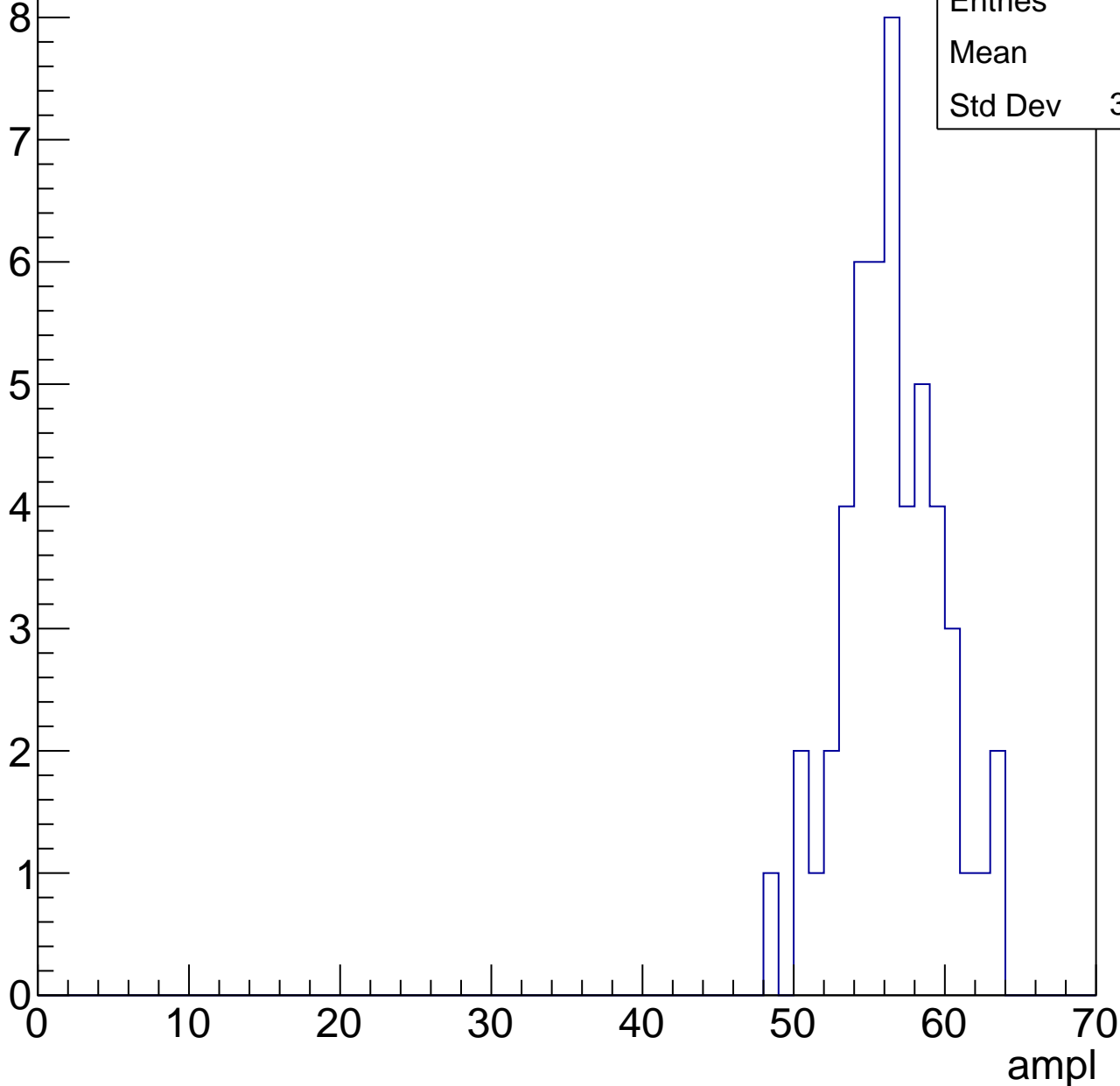


# B1L003S, U3-ch45, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	50
Mean	56
Std Dev	3.243

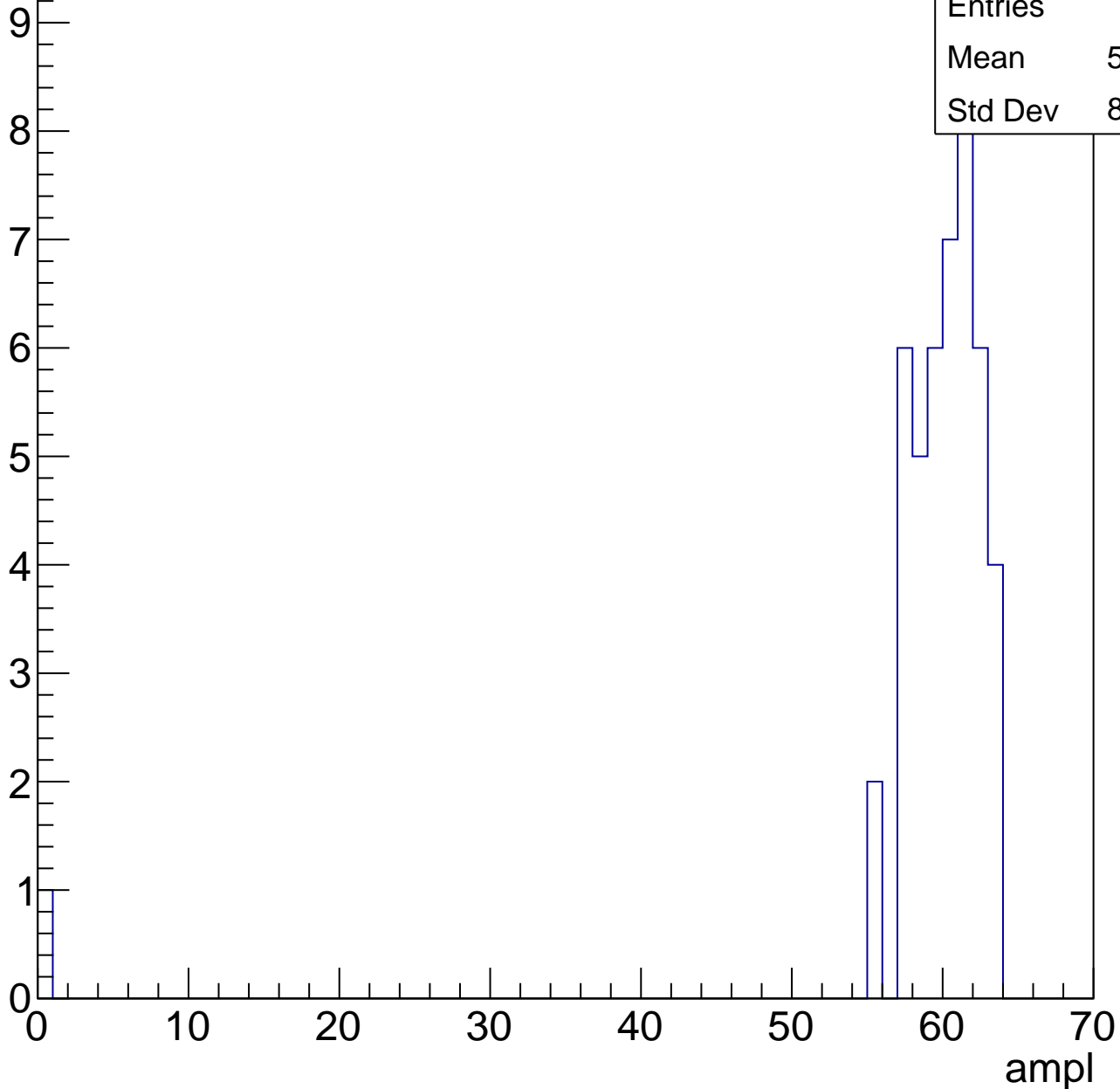


# B1L003S, U3-ch45, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

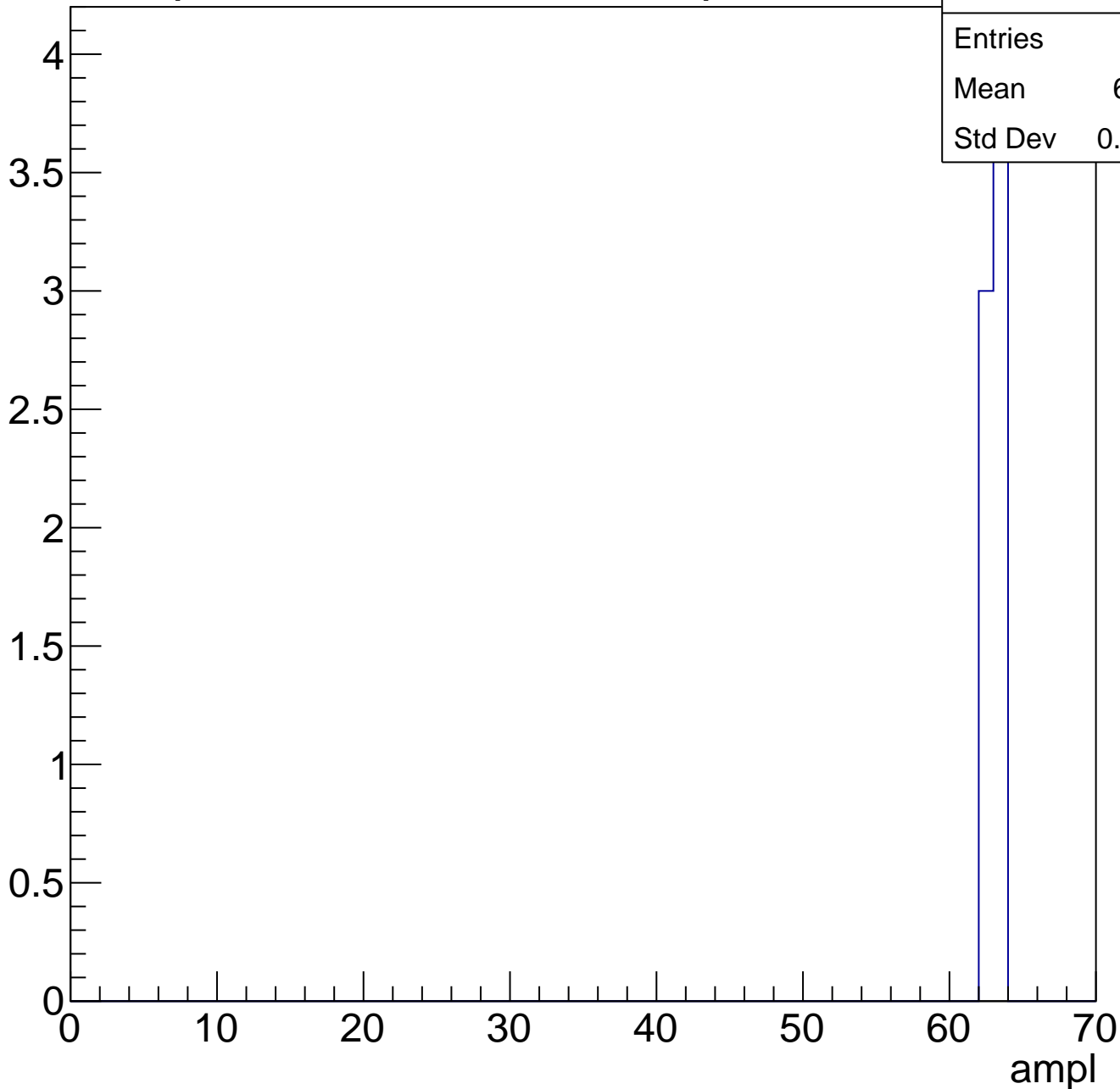
Entries	46
Mean	58.46
Std Dev	8.956



# B1L003S, U3-ch45, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch45, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	3
Mean	7.333
Std Dev	10.37

# B1L003S, U3-ch46, adc0

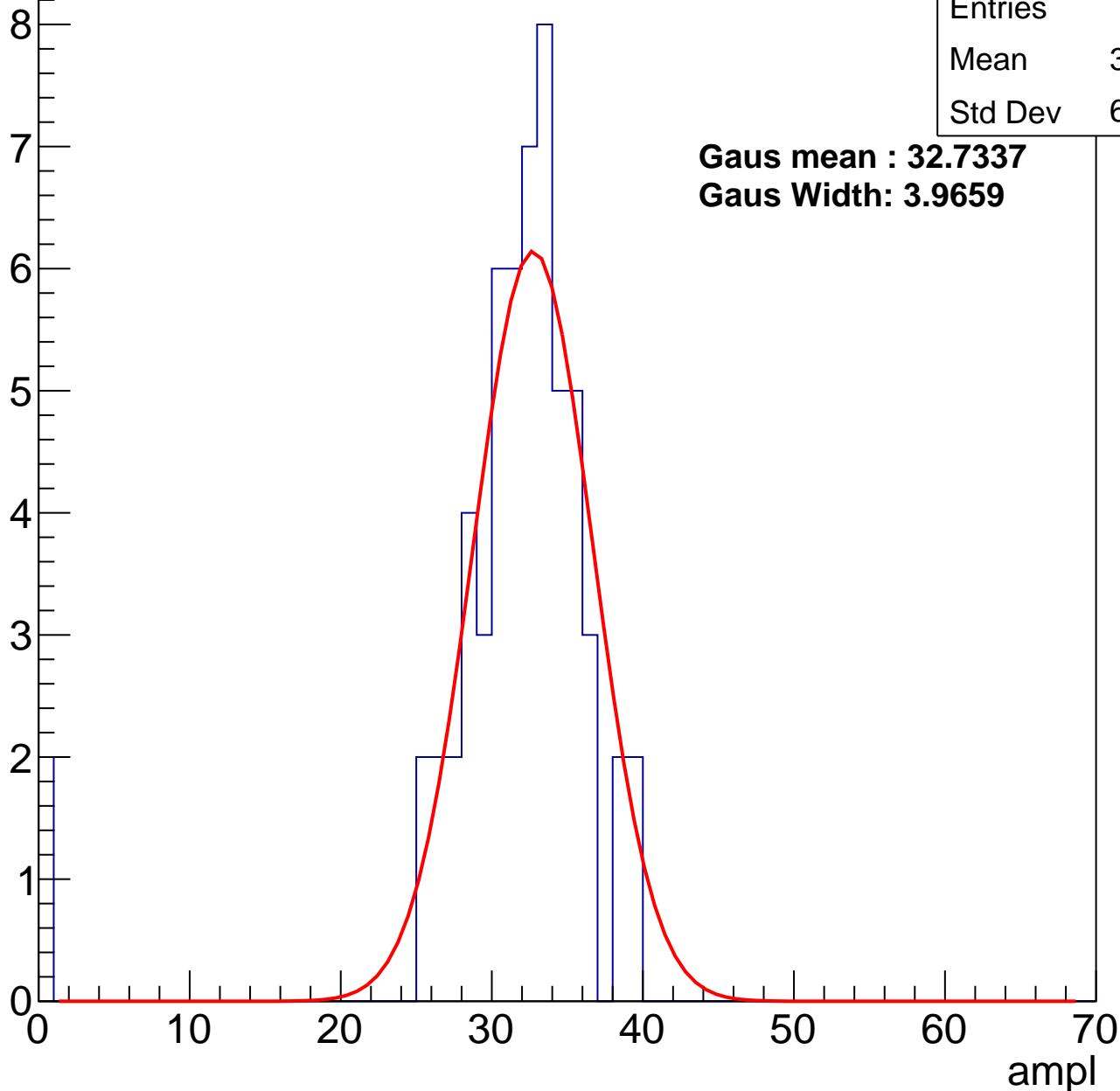
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	30.78
Std Dev	6.628

**Gaus mean : 32.7337**

**Gaus Width: 3.9659**



# B1L003S, U3-ch46, adc1

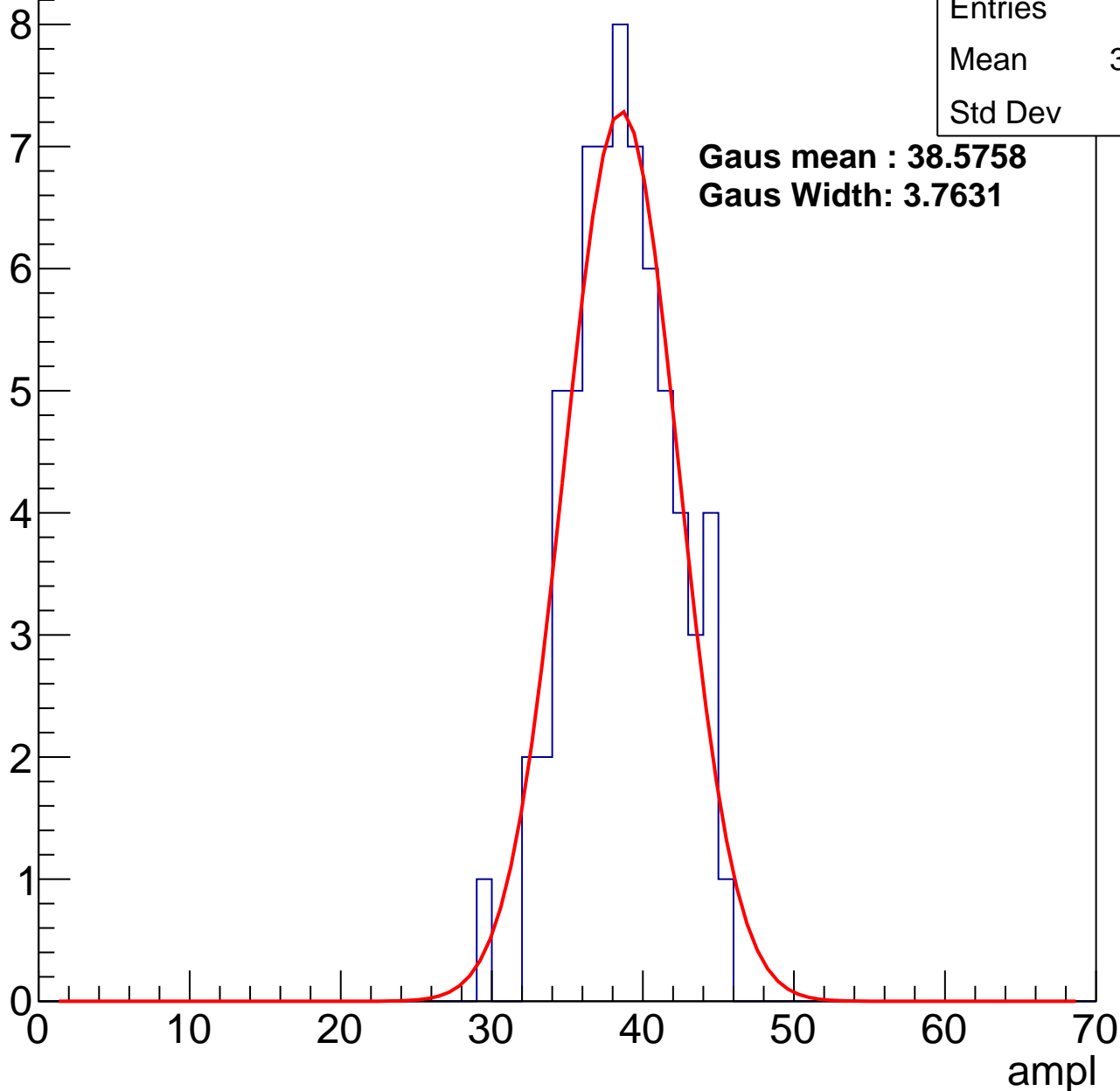
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	38.13
Std Dev	3.39

**Gaus mean : 38.5758**

**Gaus Width: 3.7631**



# B1L003S, U3-ch46, adc2

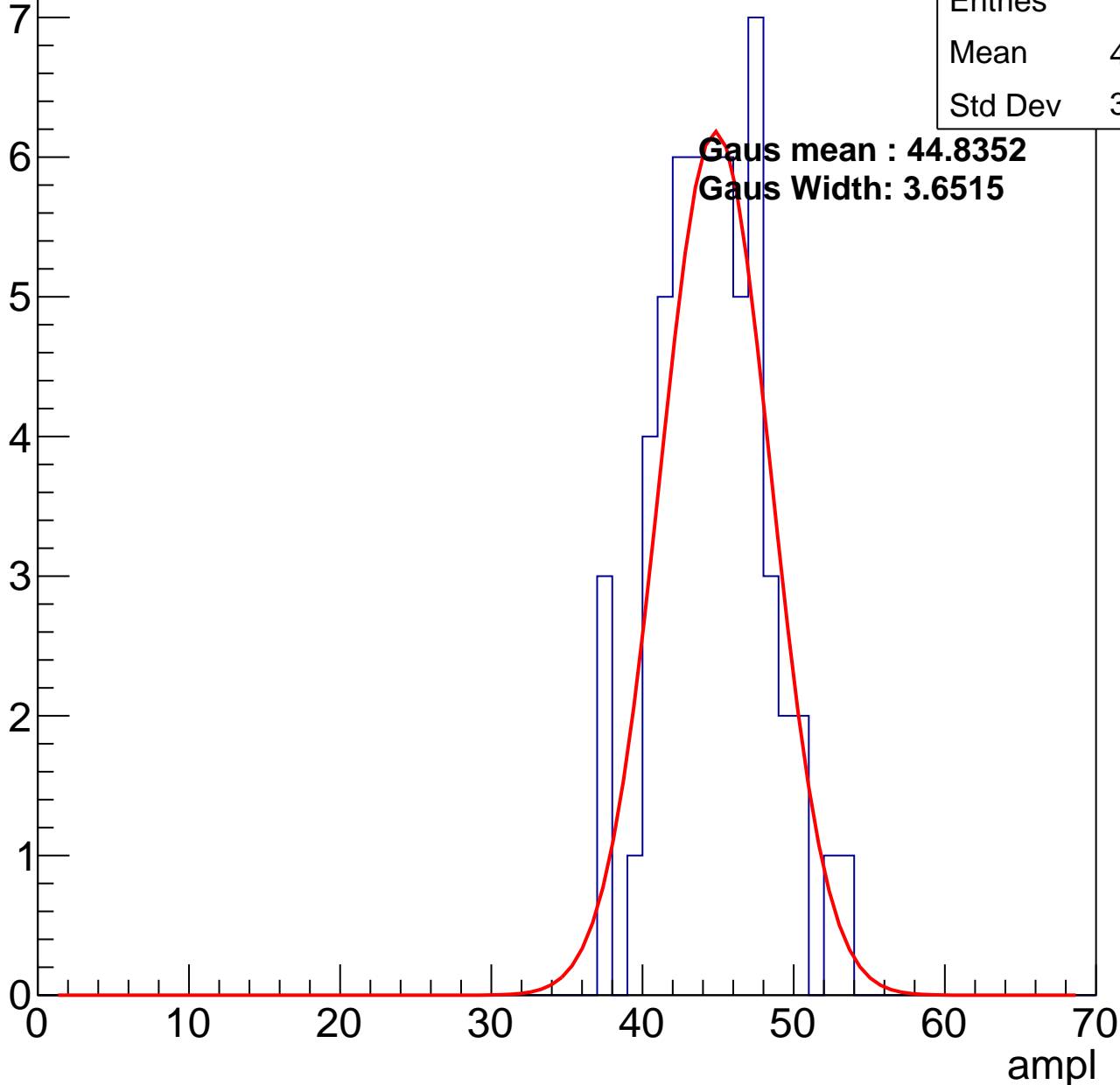
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	44.22
Std Dev	3.504

**Gaus mean : 44.8352**

**Gaus Width: 3.6515**

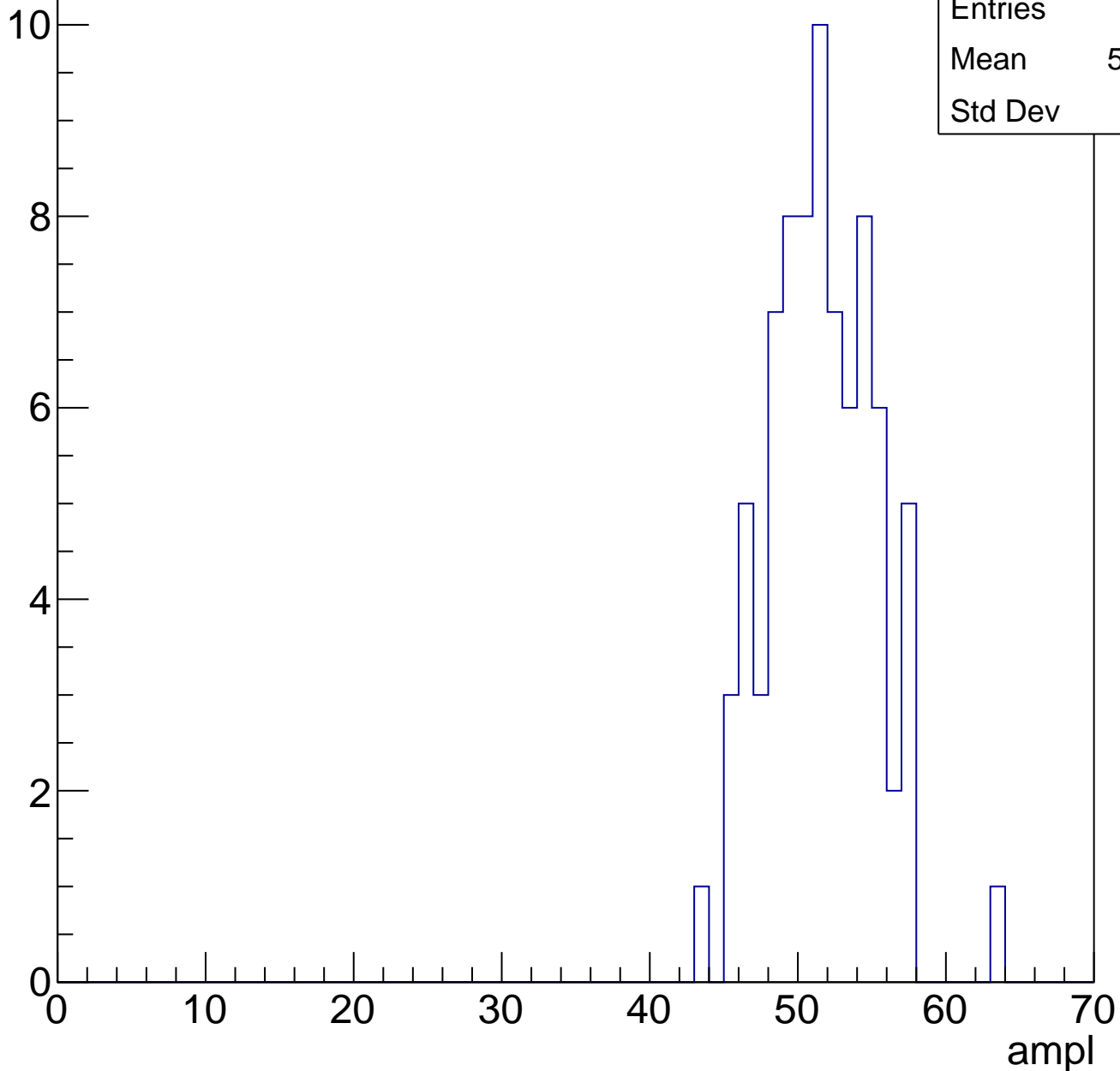


# B1L003S, U3-ch46, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

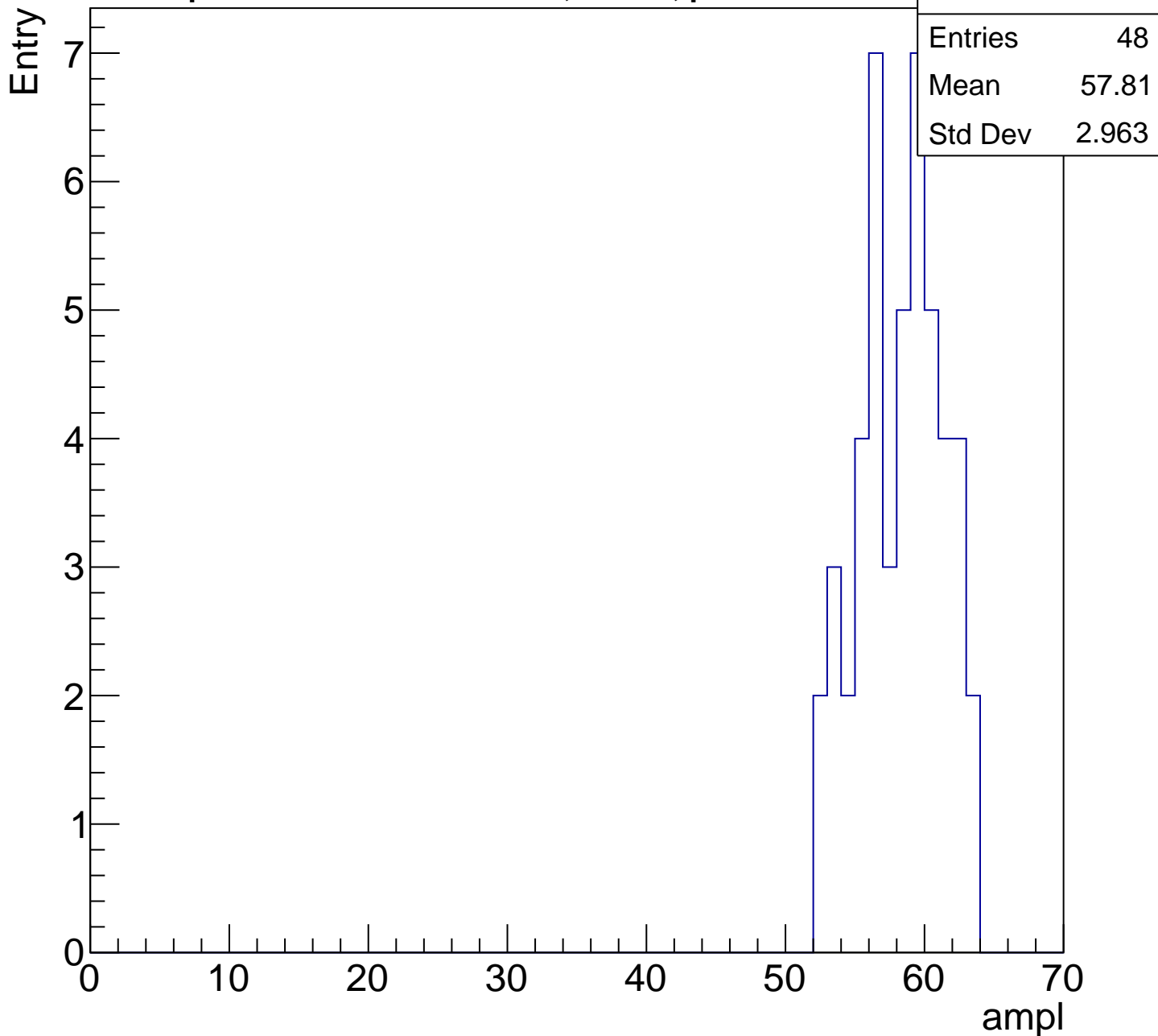
Entries	80
Mean	51.14
Std Dev	3.57

Entry



# B1L003S, U3-ch46, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

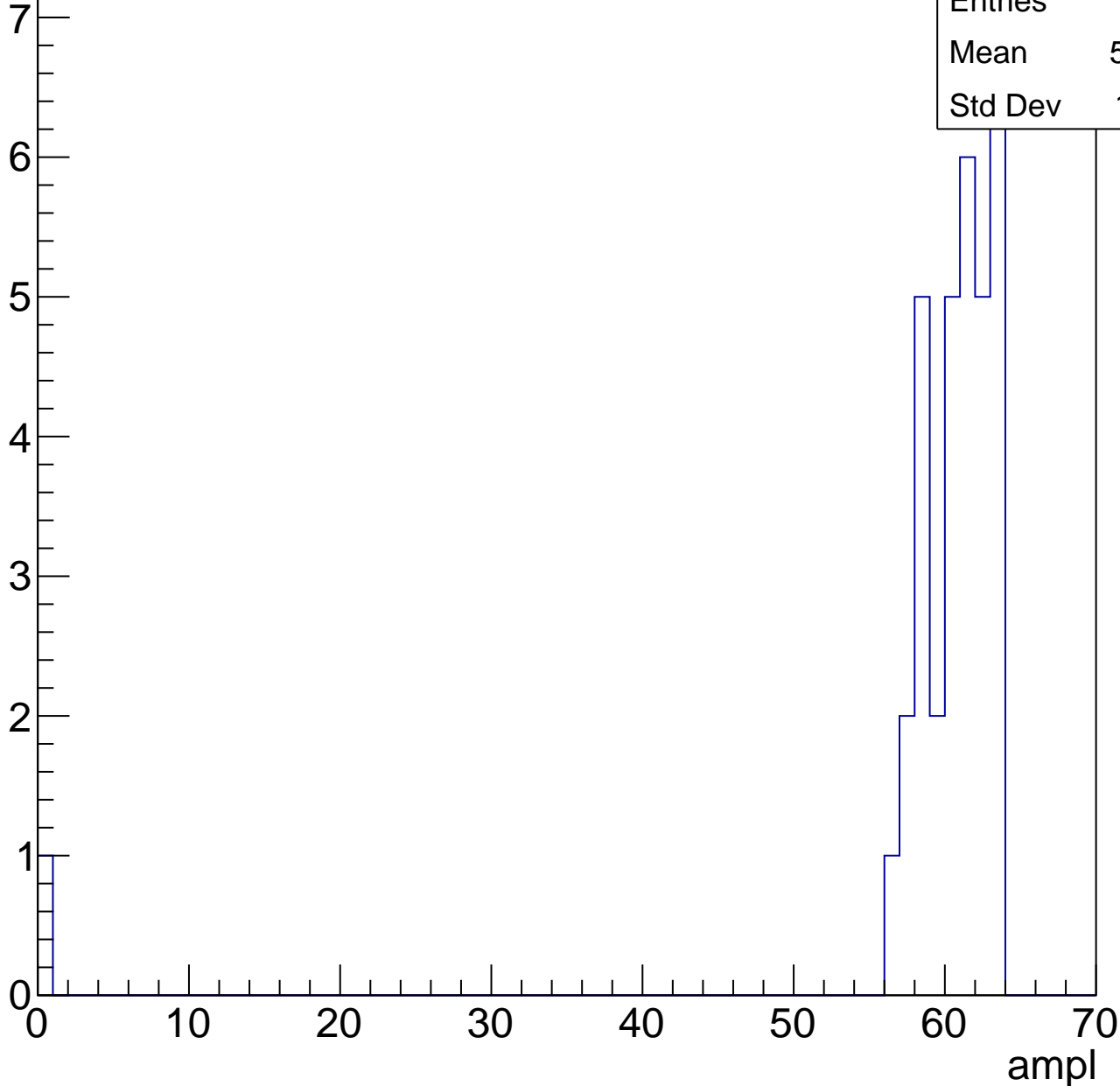


# B1L003S, U3-ch46, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	34
Mean	58.68
Std Dev	10.41



# B1L003S, U3-ch46, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries	2
Mean	60.5
Std Dev	1.5



# B1L003S, U3-ch46, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U3-ch47, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	92
Mean	29.32
Std Dev	4.802

**Gaus mean : 30.5990**

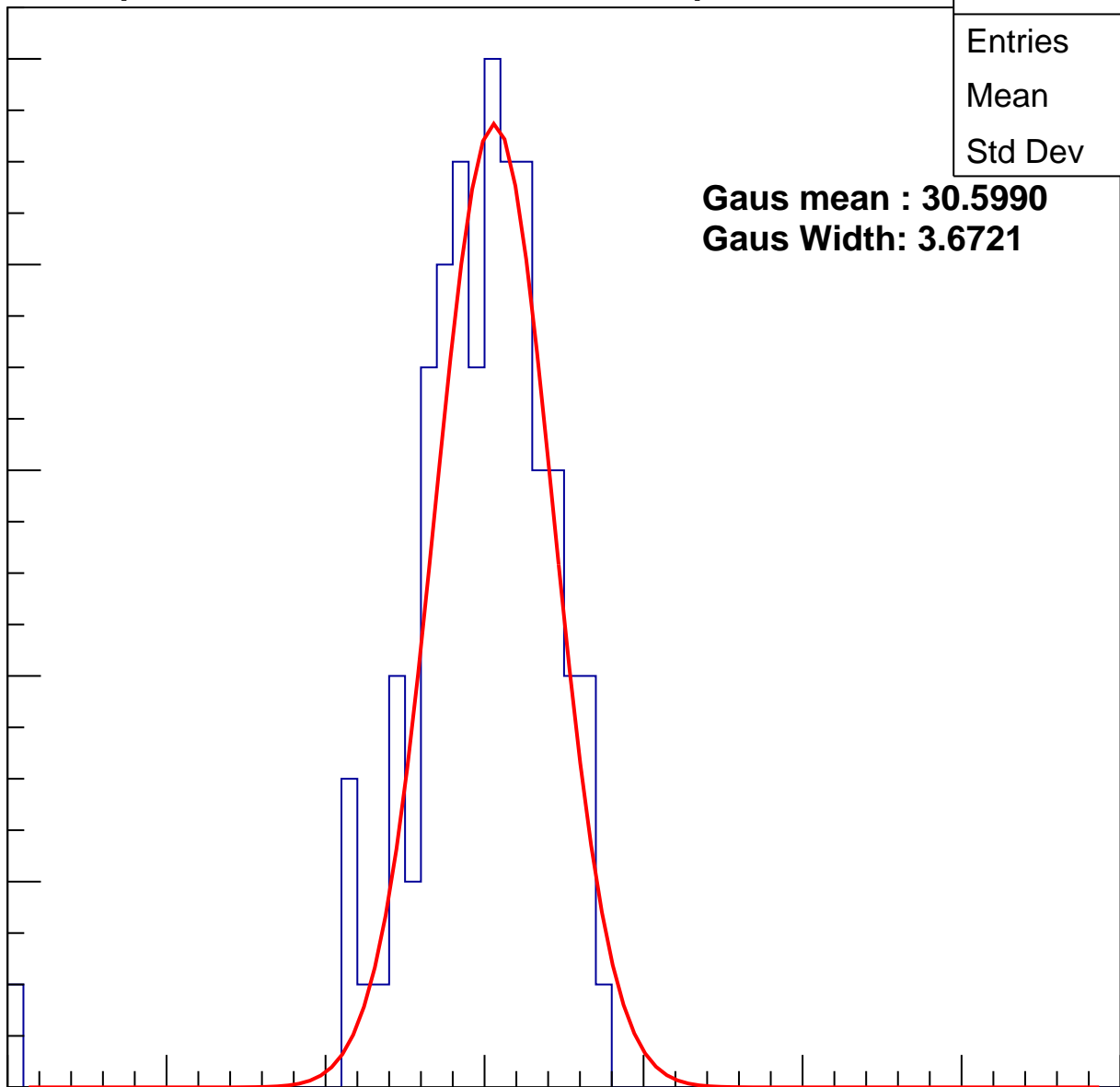
**Gaus Width: 3.6721**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U3-ch47, adc1

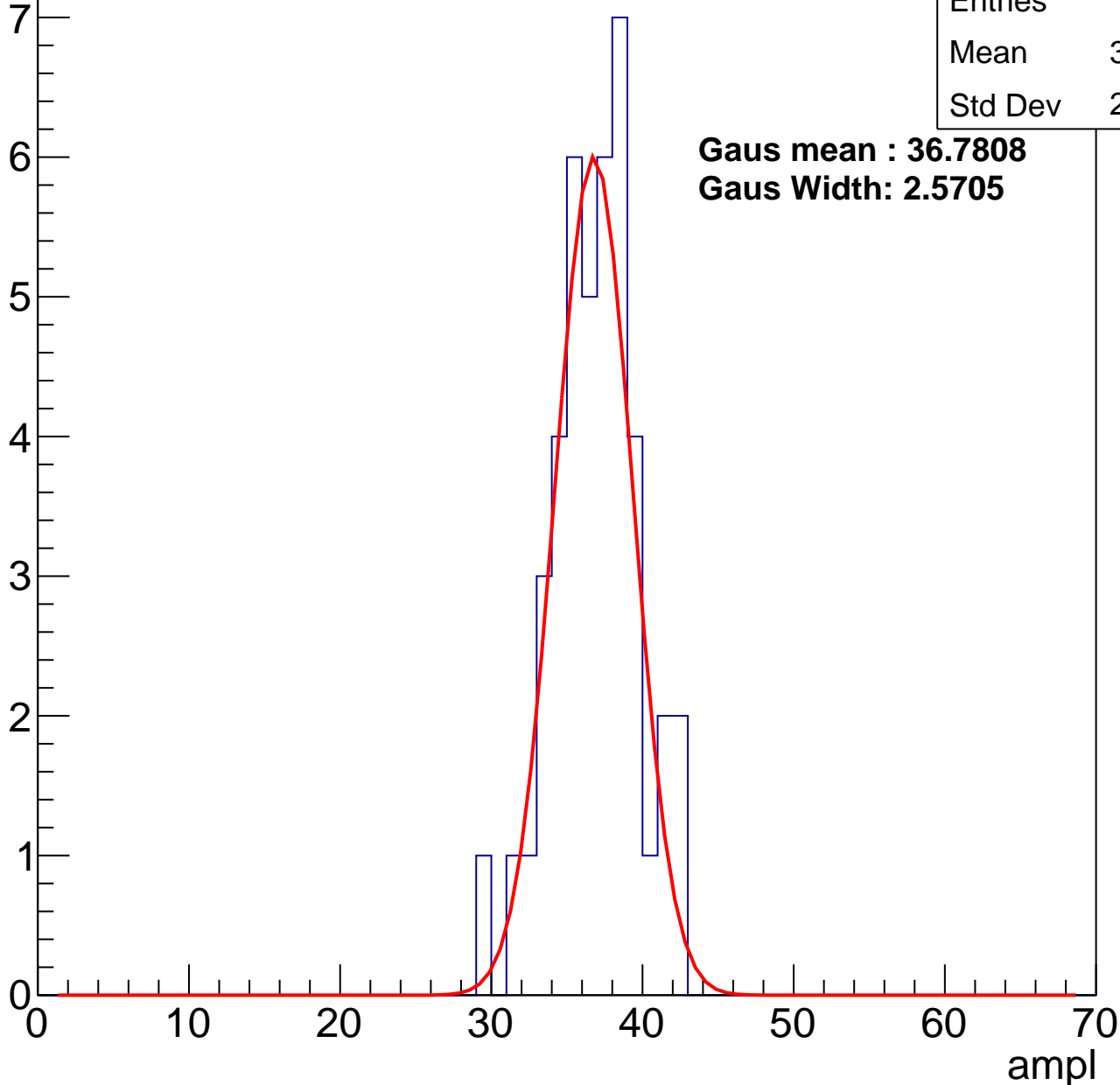
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	43
Mean	36.44
Std Dev	2.806

**Gaus mean : 36.7808**

**Gaus Width: 2.5705**



# B1L003S, U3-ch47, adc2

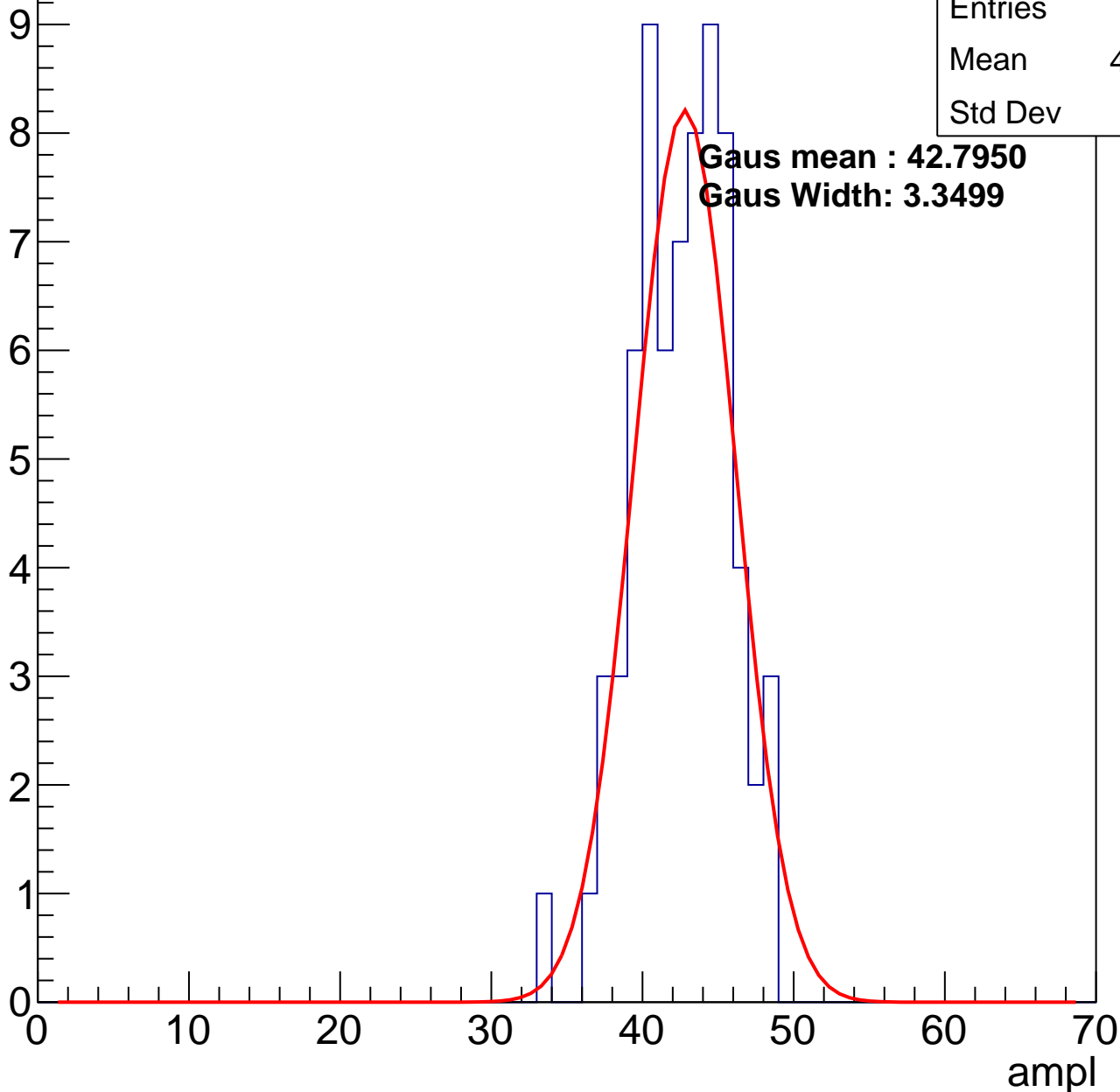
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	42.14
Std Dev	3.1

**Gaus mean : 42.7950**

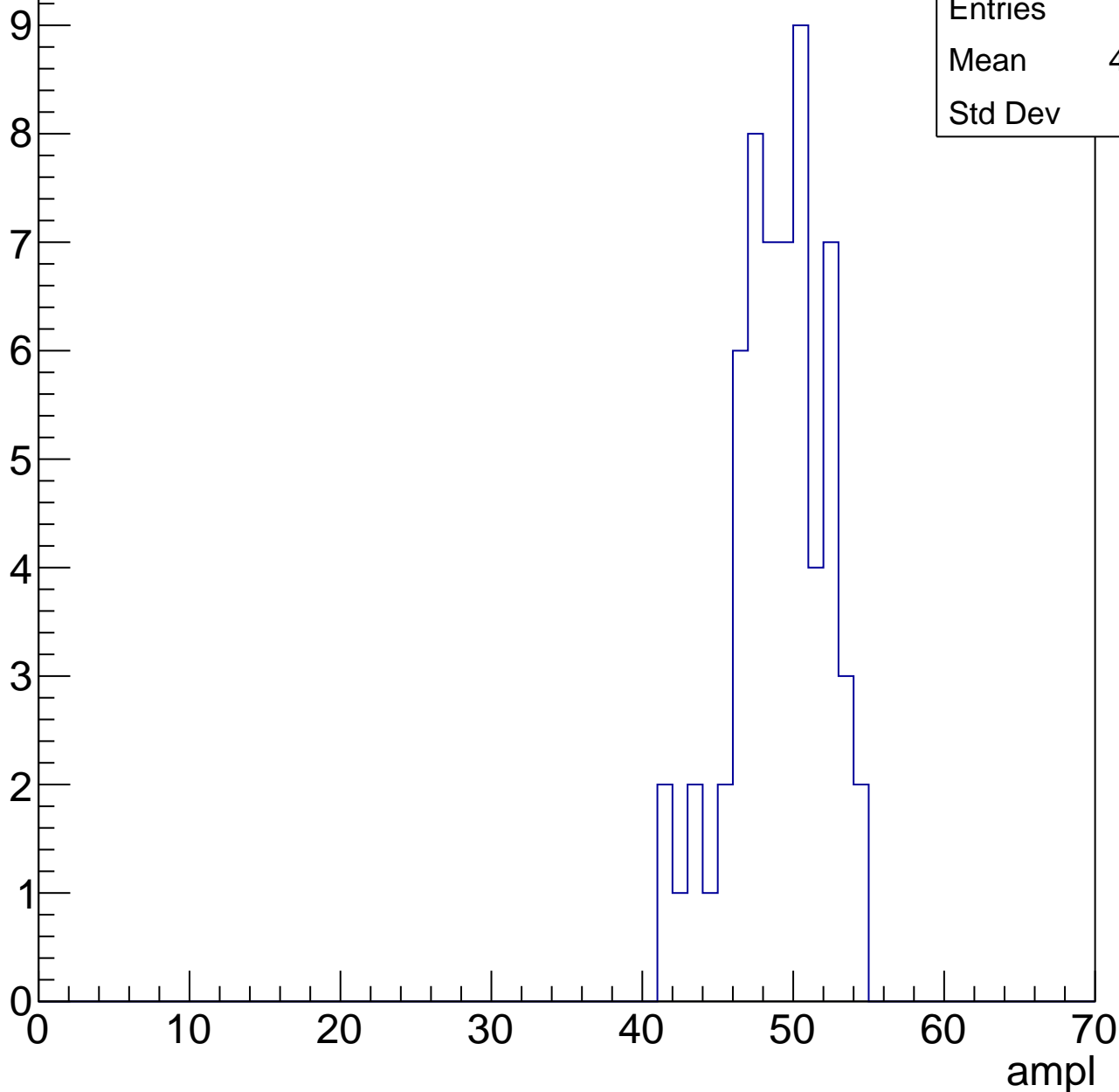
**Gaus Width: 3.3499**



# B1L003S, U3-ch47, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U3-ch47, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

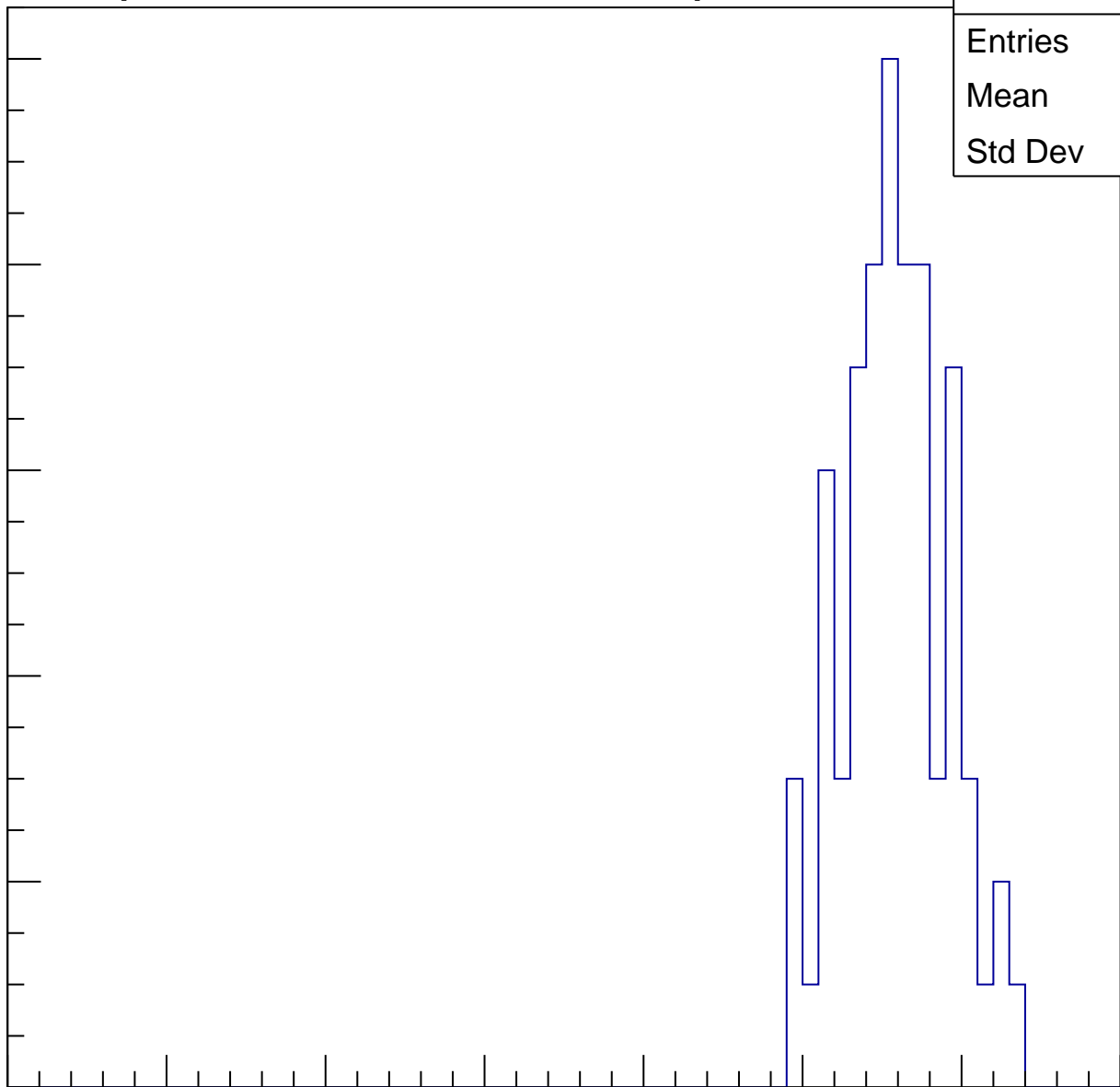
Entries	71
Mean	55.37
Std Dev	3.216

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

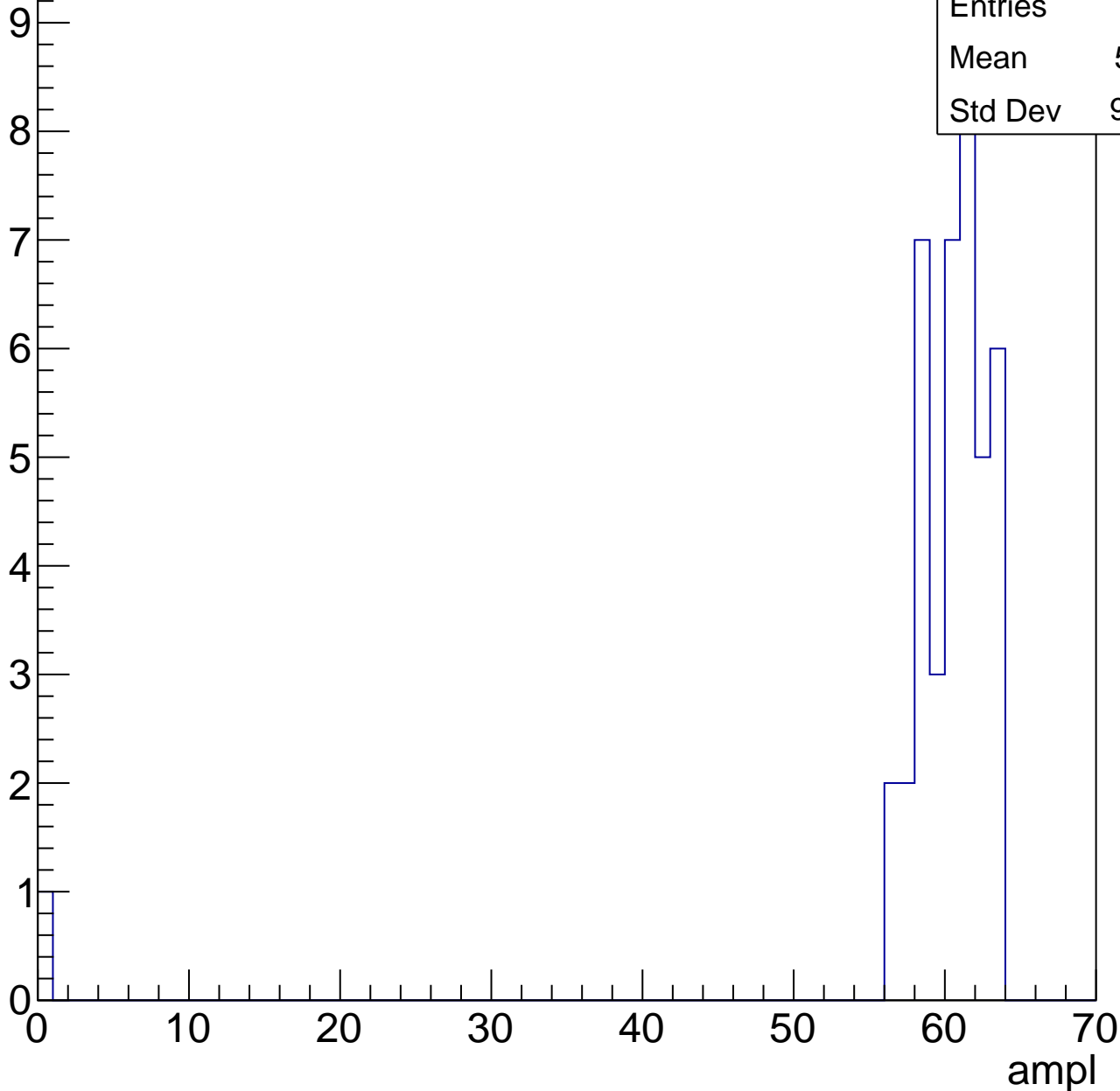


# B1L003S, U3-ch47, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	42
Mean	58.71
Std Dev	9.379



# B1L003S, U3-ch47, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch47, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U3-ch48, adc0

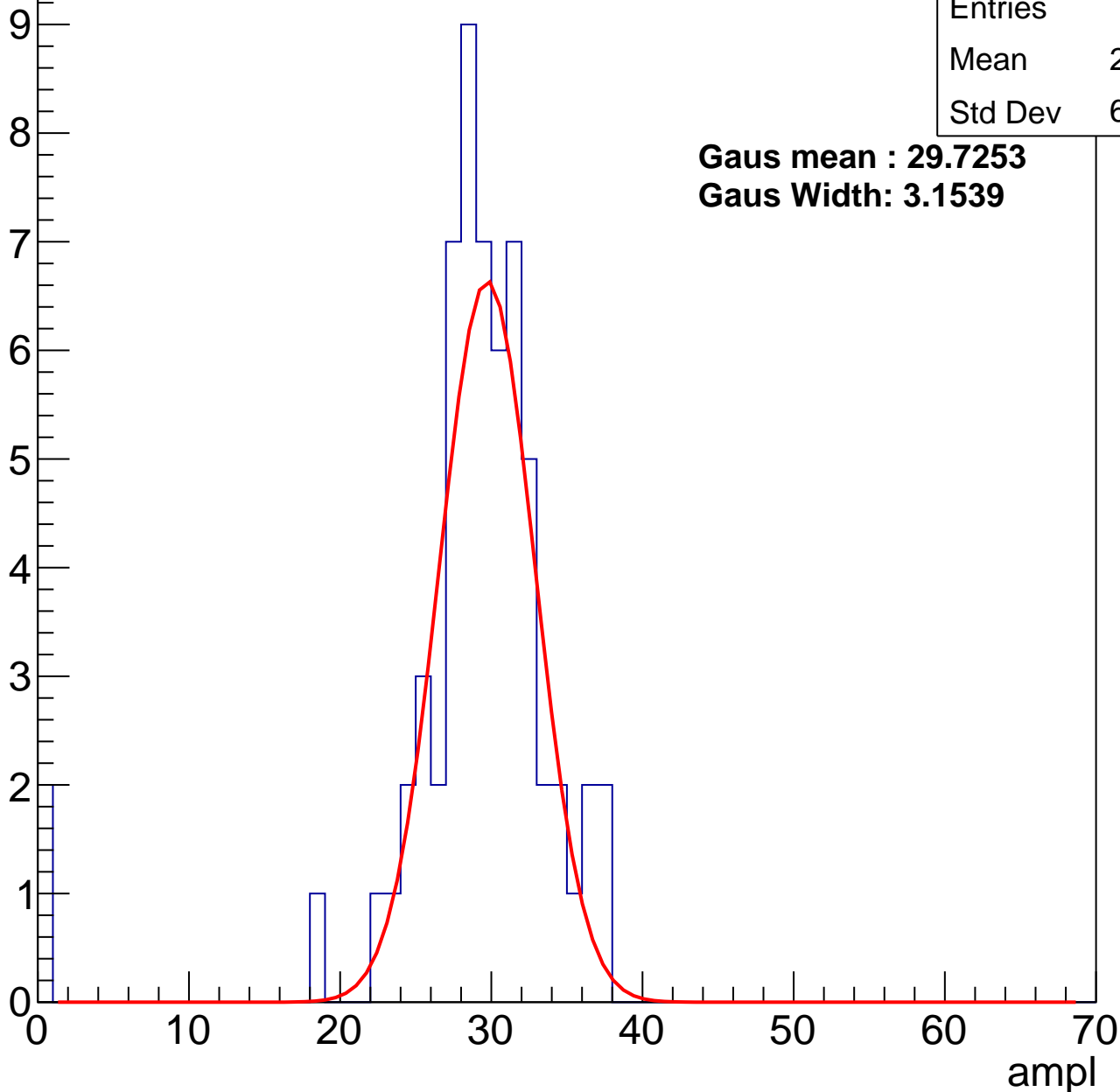
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	28.29
Std Dev	6.264

**Gaus mean : 29.7253**

**Gaus Width: 3.1539**



# B1L003S, U3-ch48, adc1

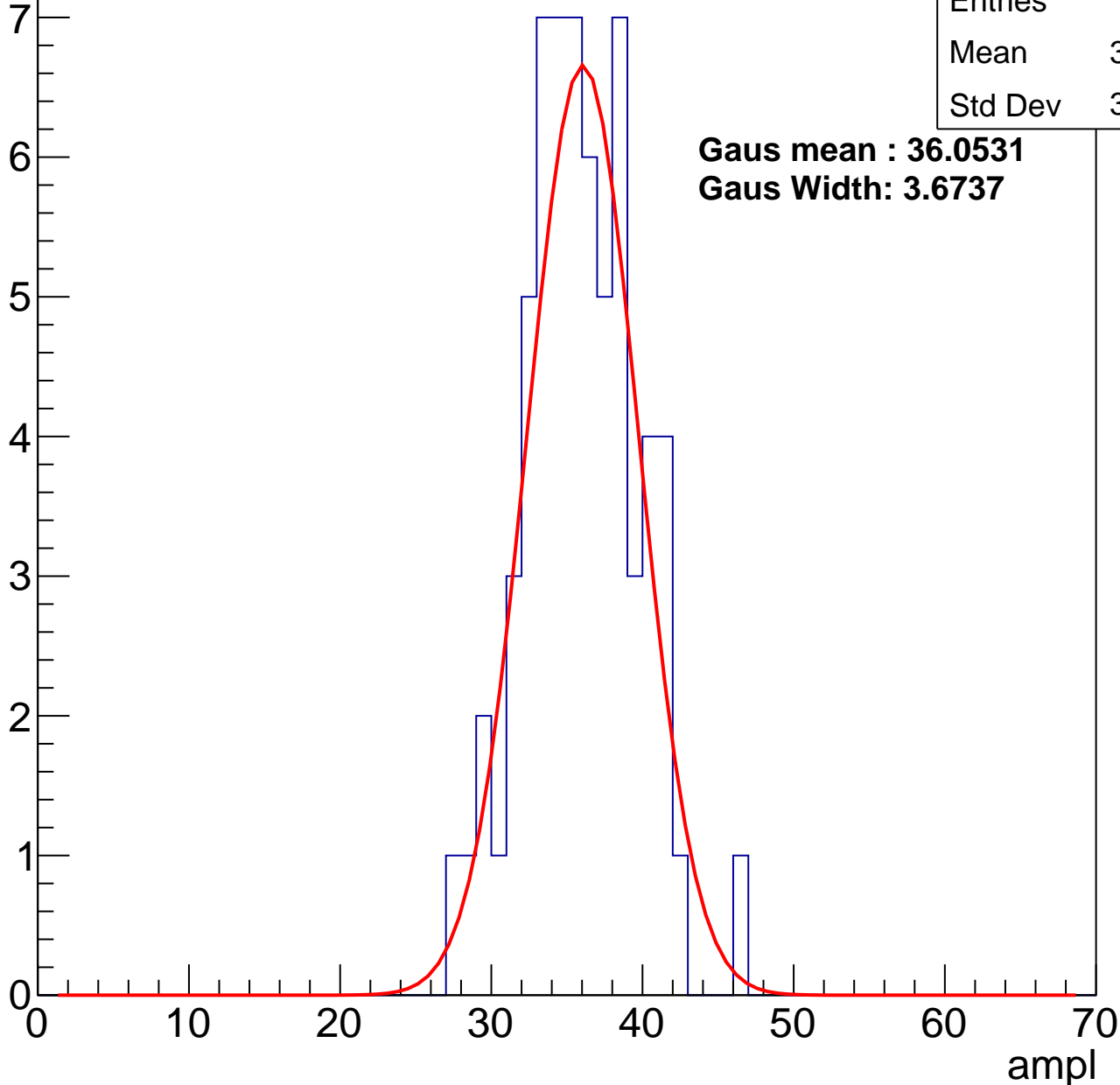
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	35.48
Std Dev	3.667

**Gaus mean : 36.0531**

**Gaus Width: 3.6737**



# B1L003S, U3-ch48, adc2

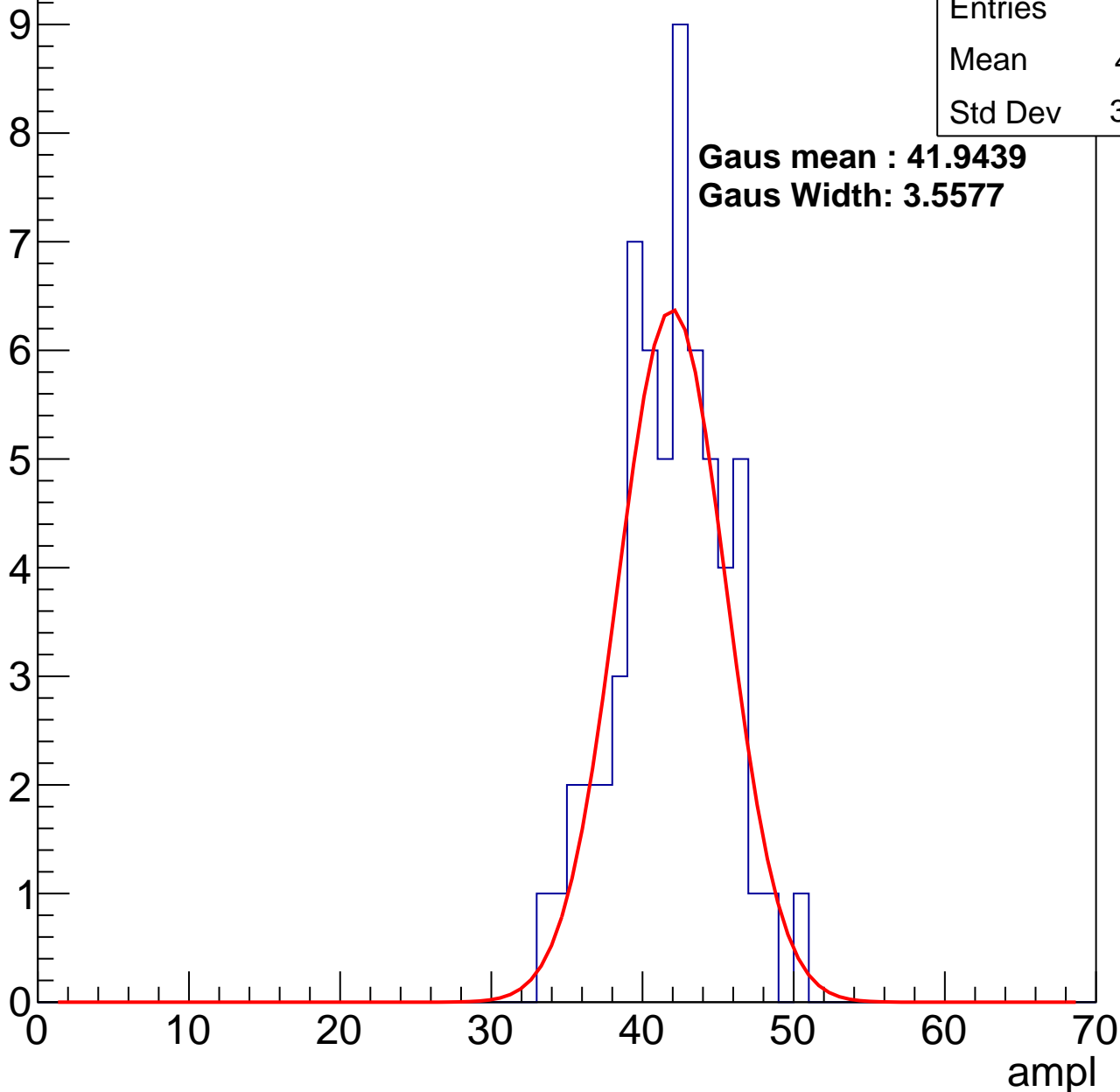
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	41.41
Std Dev	3.508

**Gaus mean : 41.9439**

**Gaus Width: 3.5577**

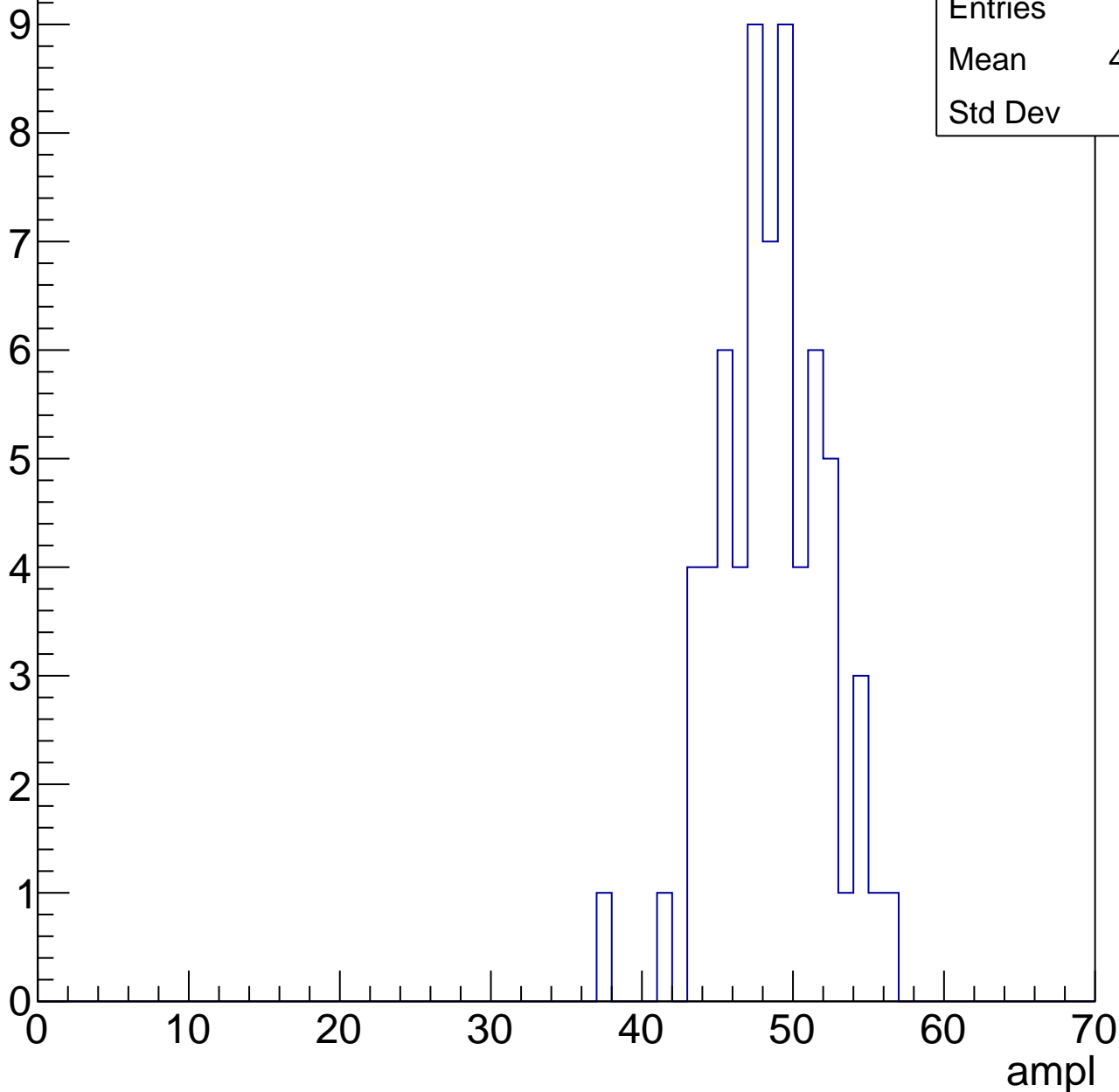


# B1L003S, U3-ch48, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	48.06
Std Dev	3.52

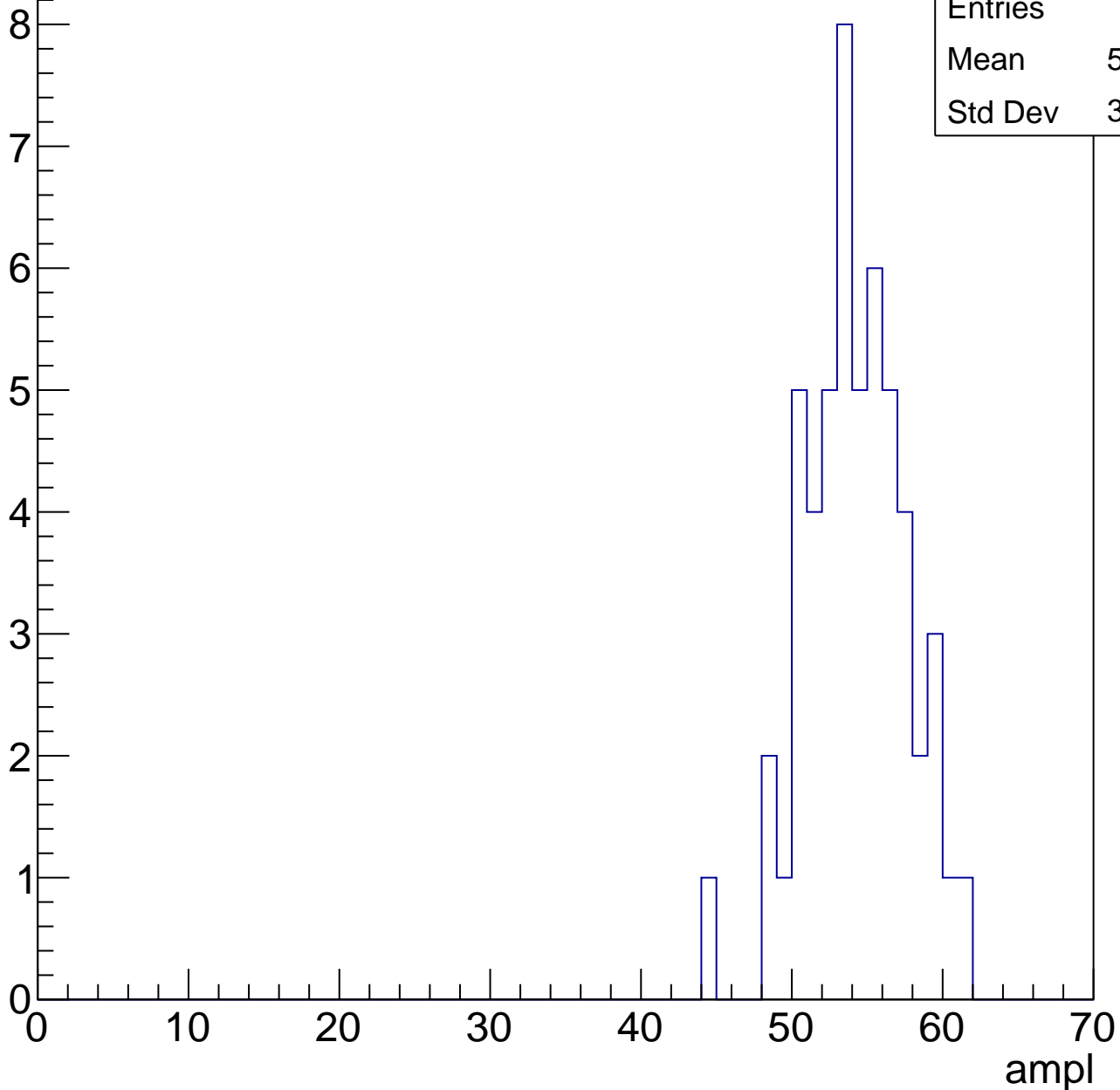


# B1L003S, U3-ch48, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	53.75
Std Dev	3.342



# B1L003S, U3-ch48, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

7

6

5

4

3

2

1

0

Entries 51

Mean 58.84

Std Dev 2.562

ampl

0

10

20

30

40

50

60

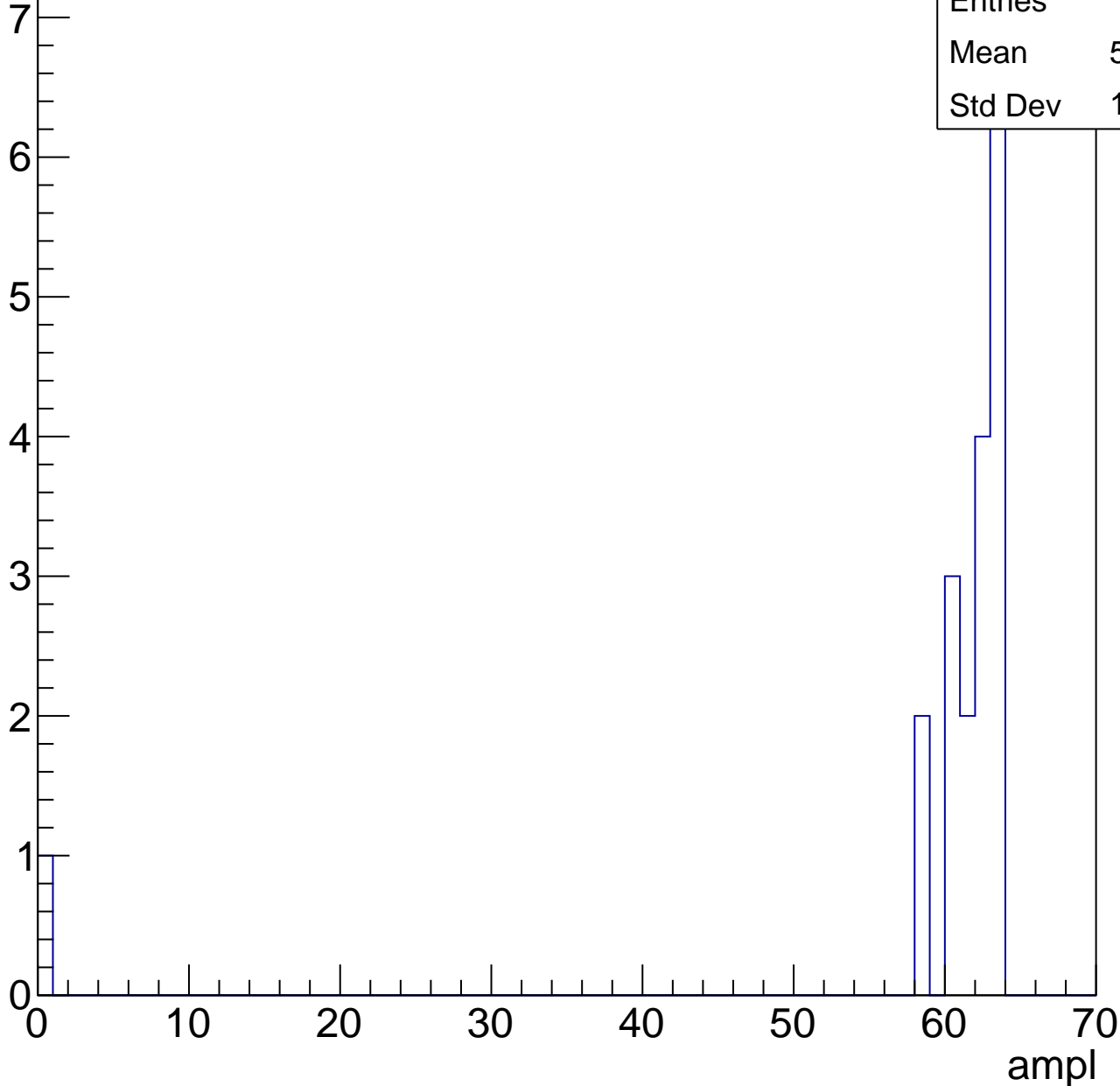
70

# B1L003S, U3-ch48, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	19
Mean	58.26
Std Dev	13.83





# B1L003S, U3-ch48, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L003S, U3-ch49, adc0

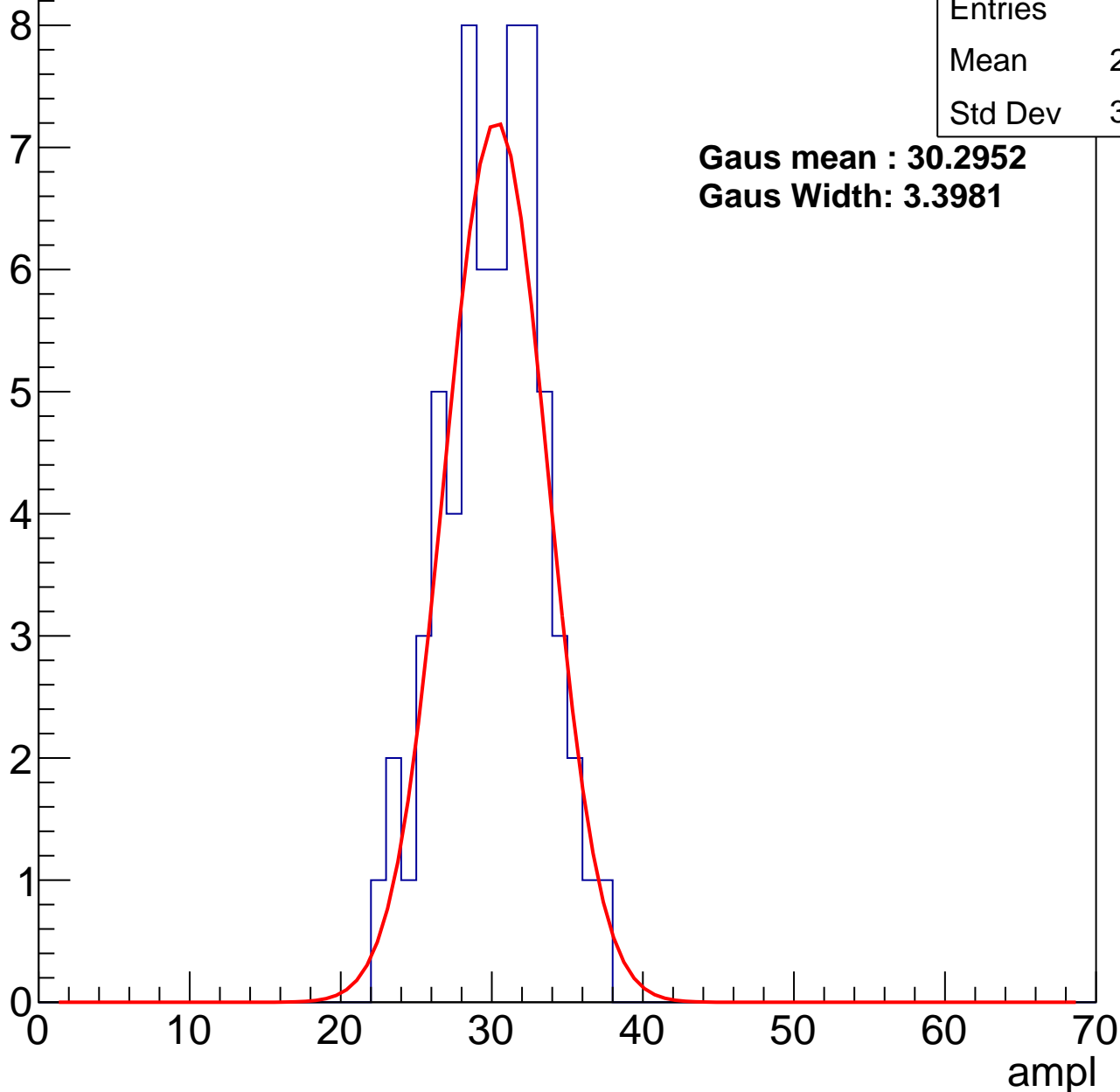
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	29.64
Std Dev	3.276

**Gaus mean : 30.2952**

**Gaus Width: 3.3981**



# B1L003S, U3-ch49, adc1

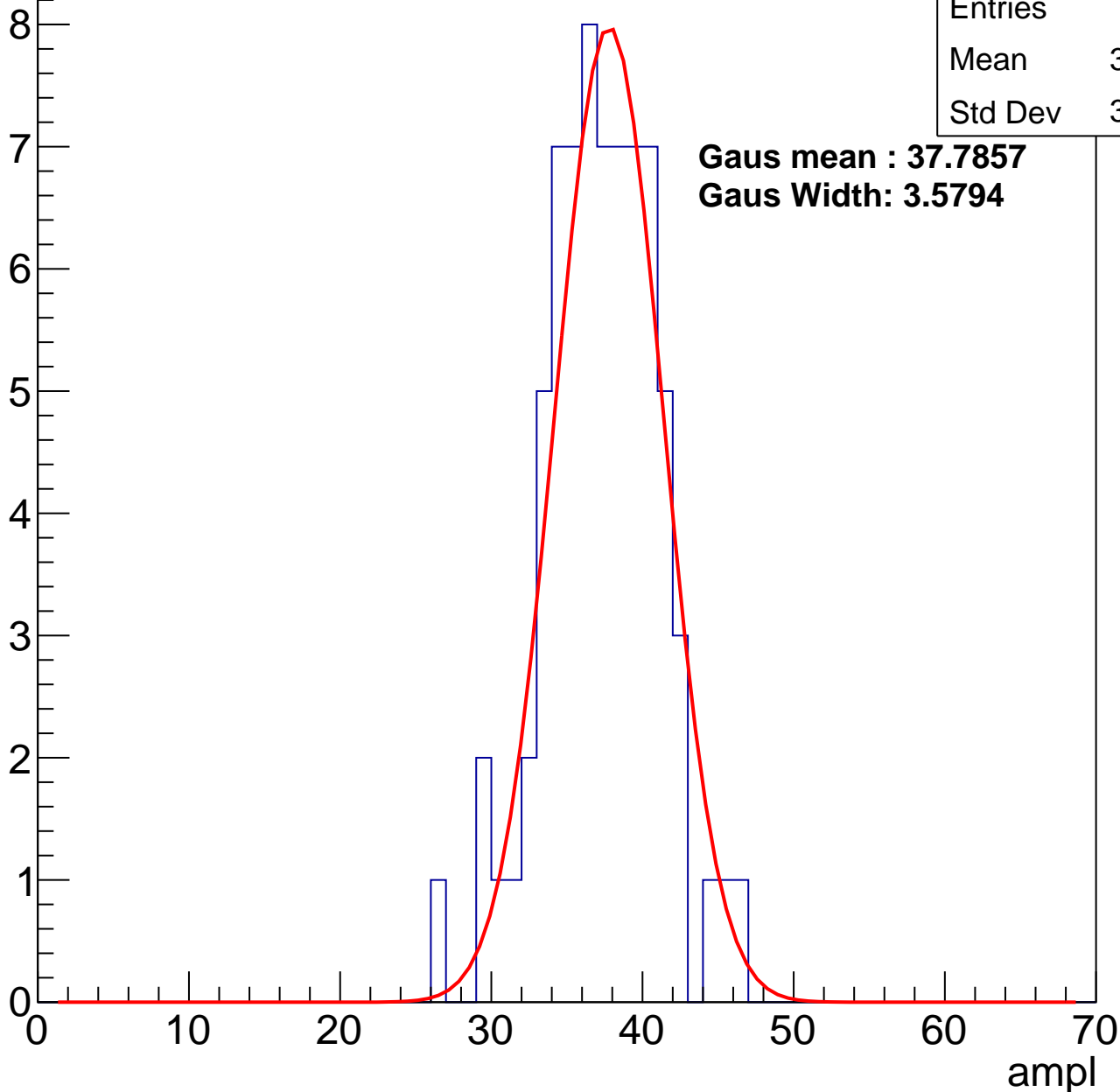
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	73
Mean	36.84
Std Dev	3.716

**Gaus mean : 37.7857**

**Gaus Width: 3.5794**



# B1L003S, U3-ch49, adc2

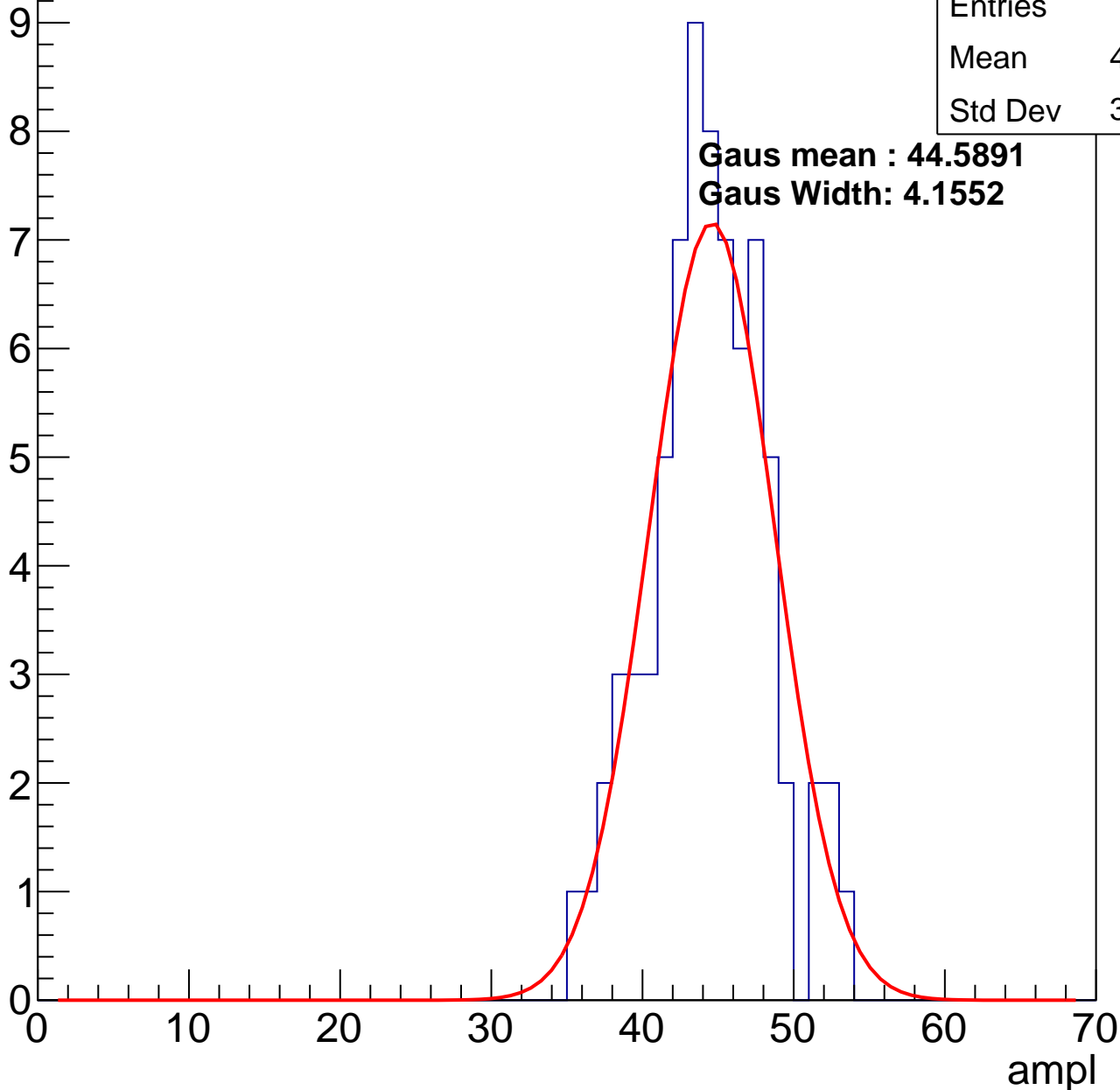
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	74
Mean	43.93
Std Dev	3.832

**Gaus mean : 44.5891**

**Gaus Width: 4.1552**

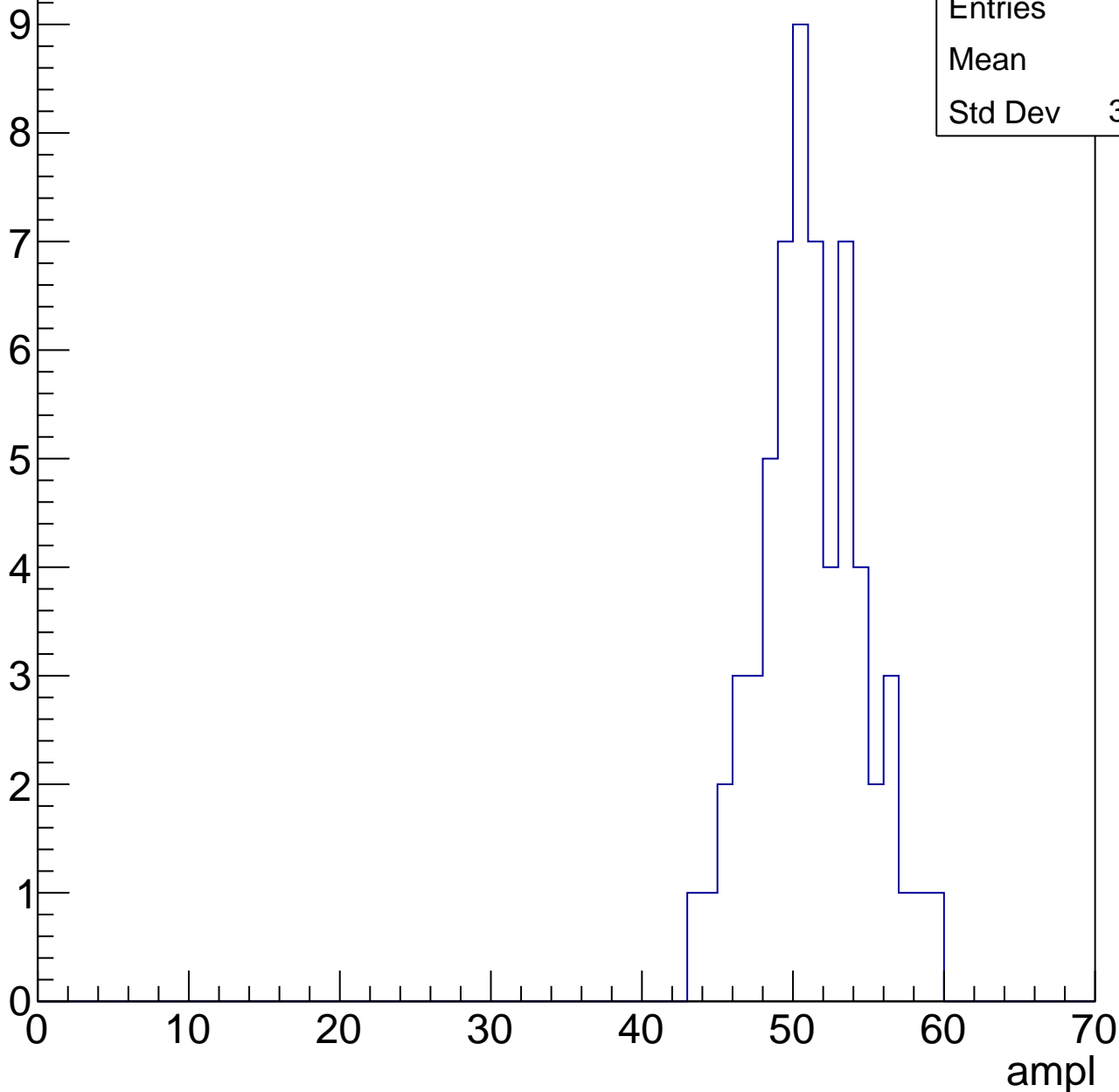


# B1L003S, U3-ch49, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	50.7
Std Dev	3.408

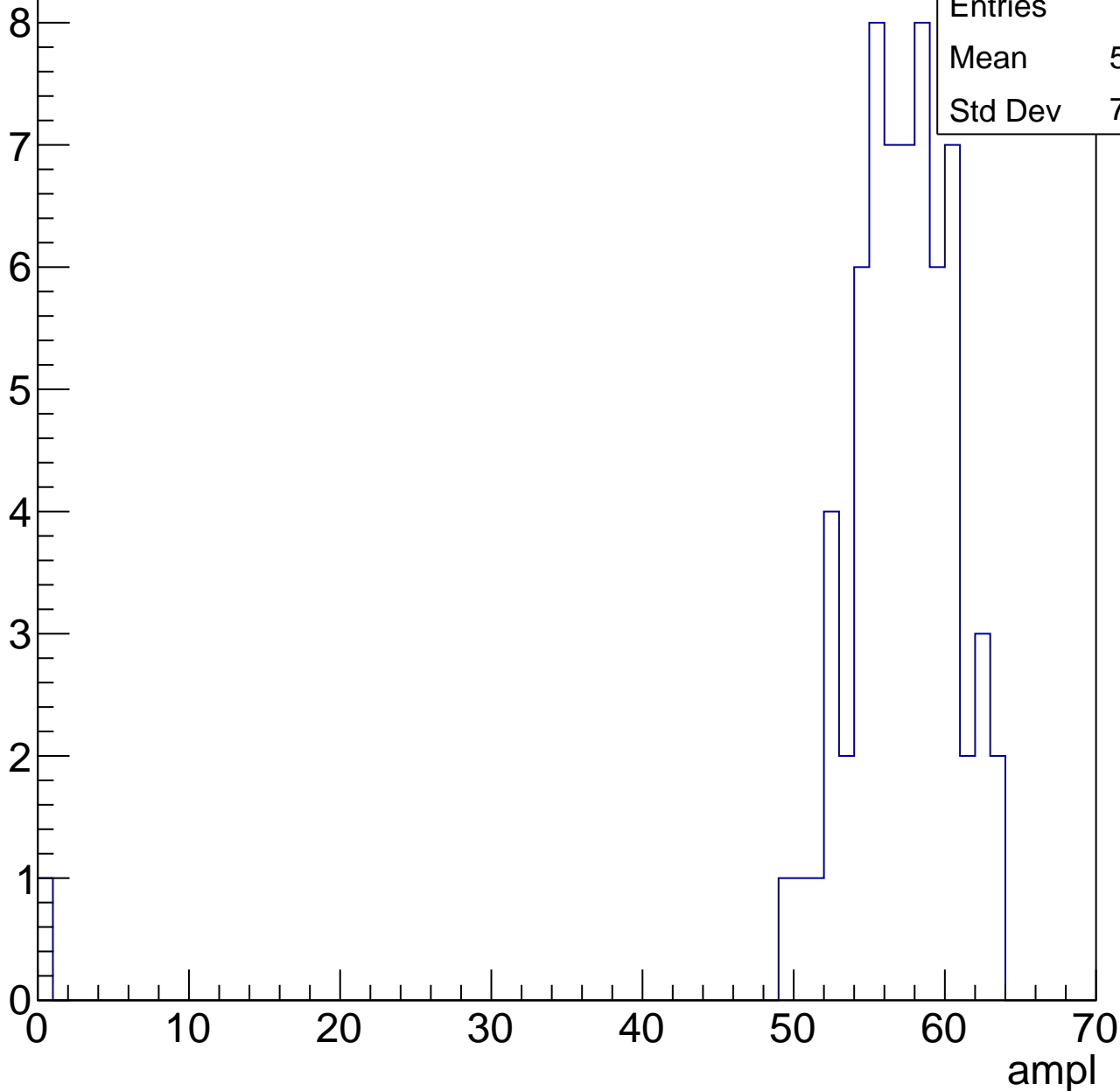


# B1L003S, U3-ch49, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	55.92
Std Dev	7.608

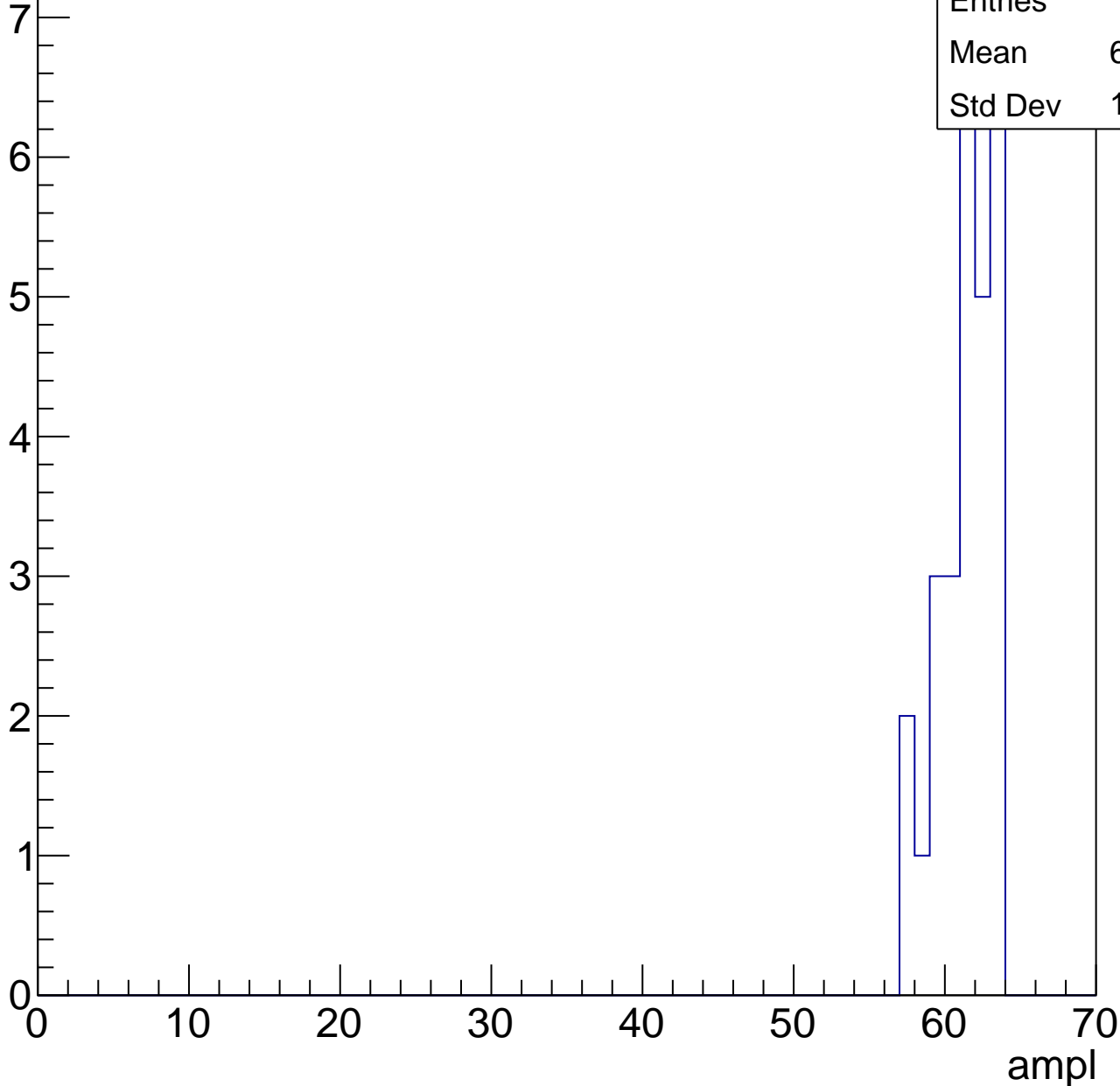


# B1L003S, U3-ch49, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	28
Mean	60.96
Std Dev	1.782



# B1L003S, U3-ch49, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch49, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U3-ch50, adc0

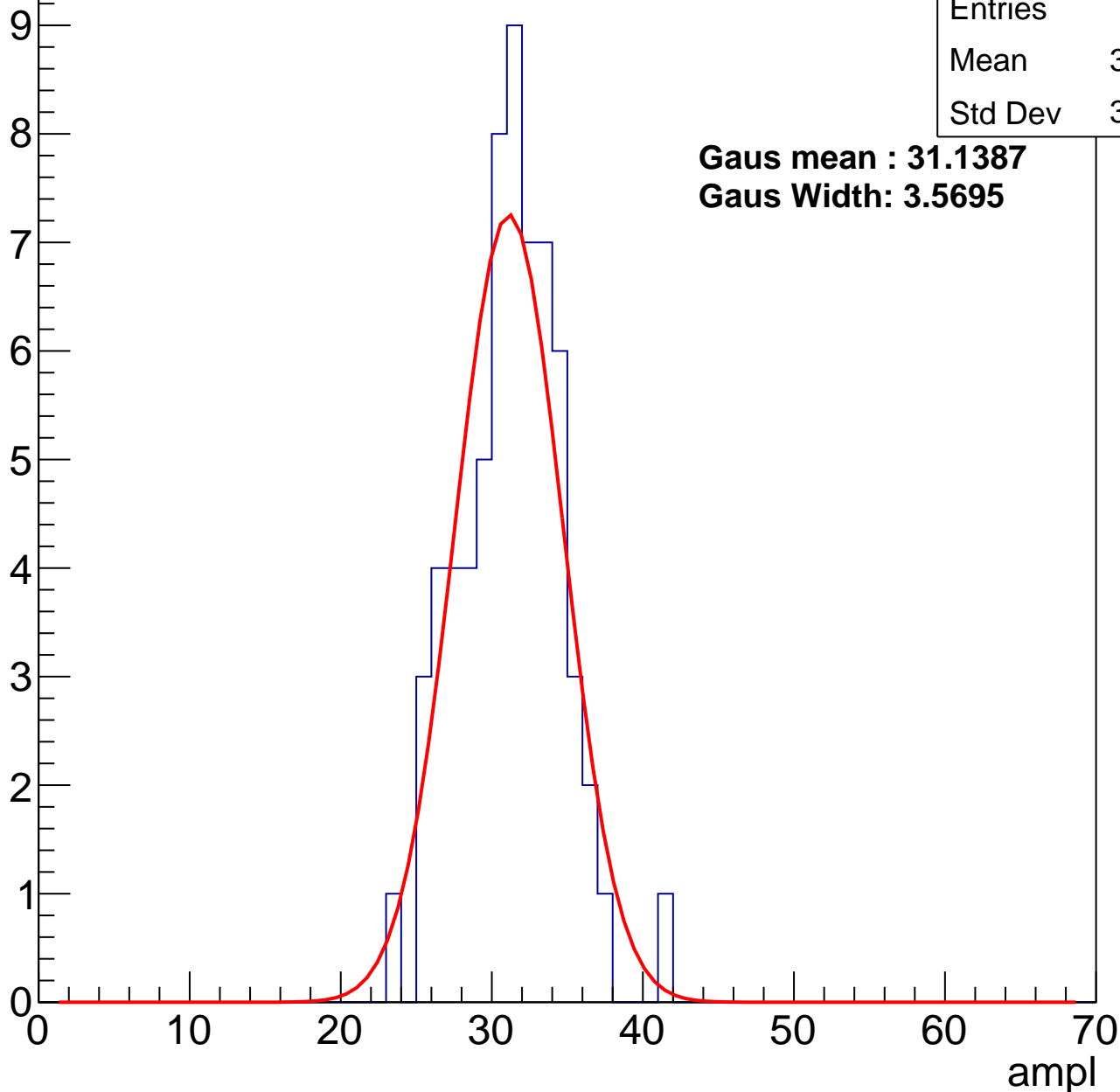
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	30.77
Std Dev	3.327

**Gaus mean : 31.1387**

**Gaus Width: 3.5695**



# B1L003S, U3-ch50, adc1

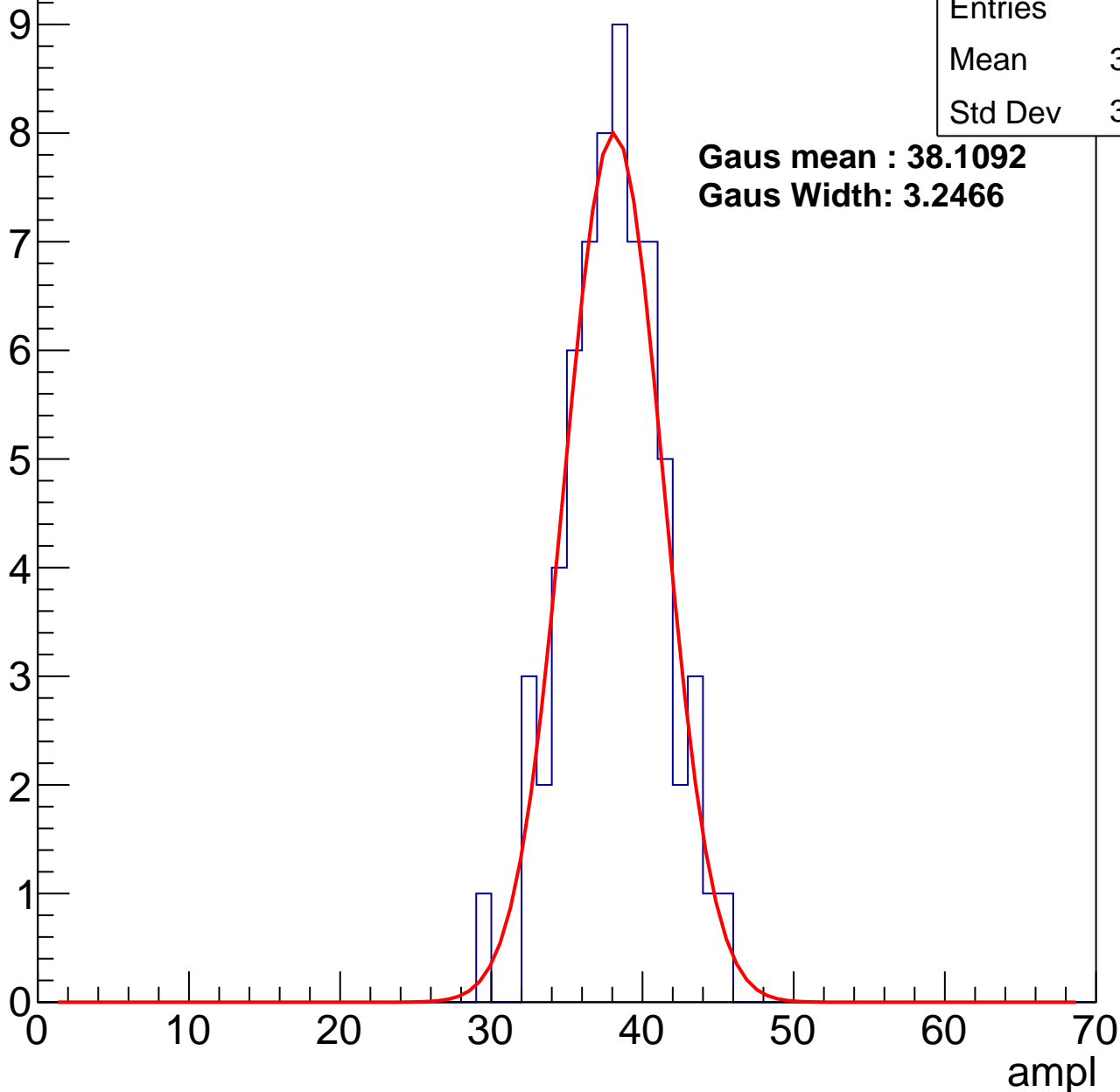
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	37.68
Std Dev	3.158

**Gaus mean : 38.1092**

**Gaus Width: 3.2466**



# B1L003S, U3-ch50, adc2

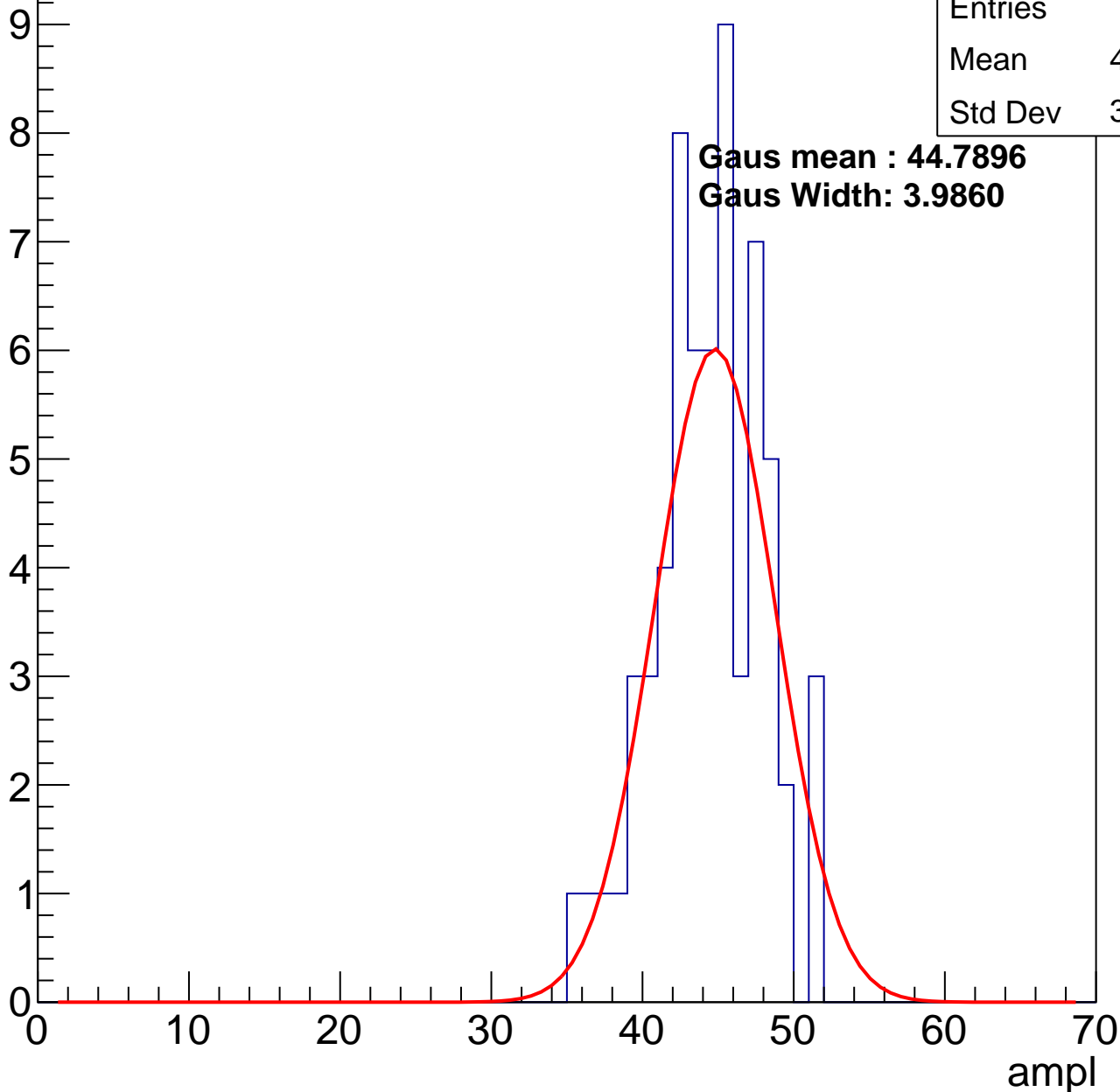
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	43.94
Std Dev	3.536

**Gaus mean : 44.7896**

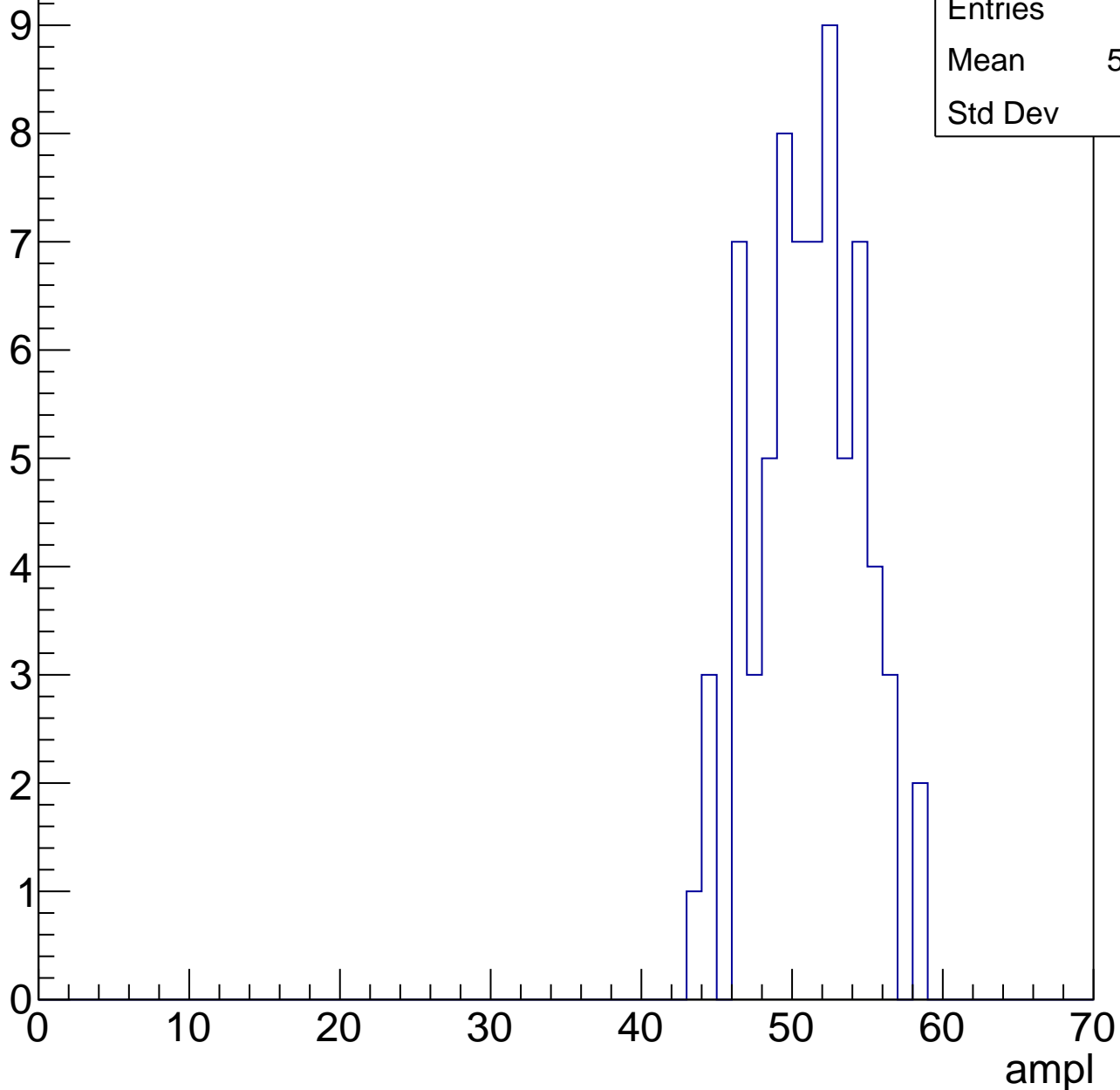
**Gaus Width: 3.9860**



# B1L003S, U3-ch50, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



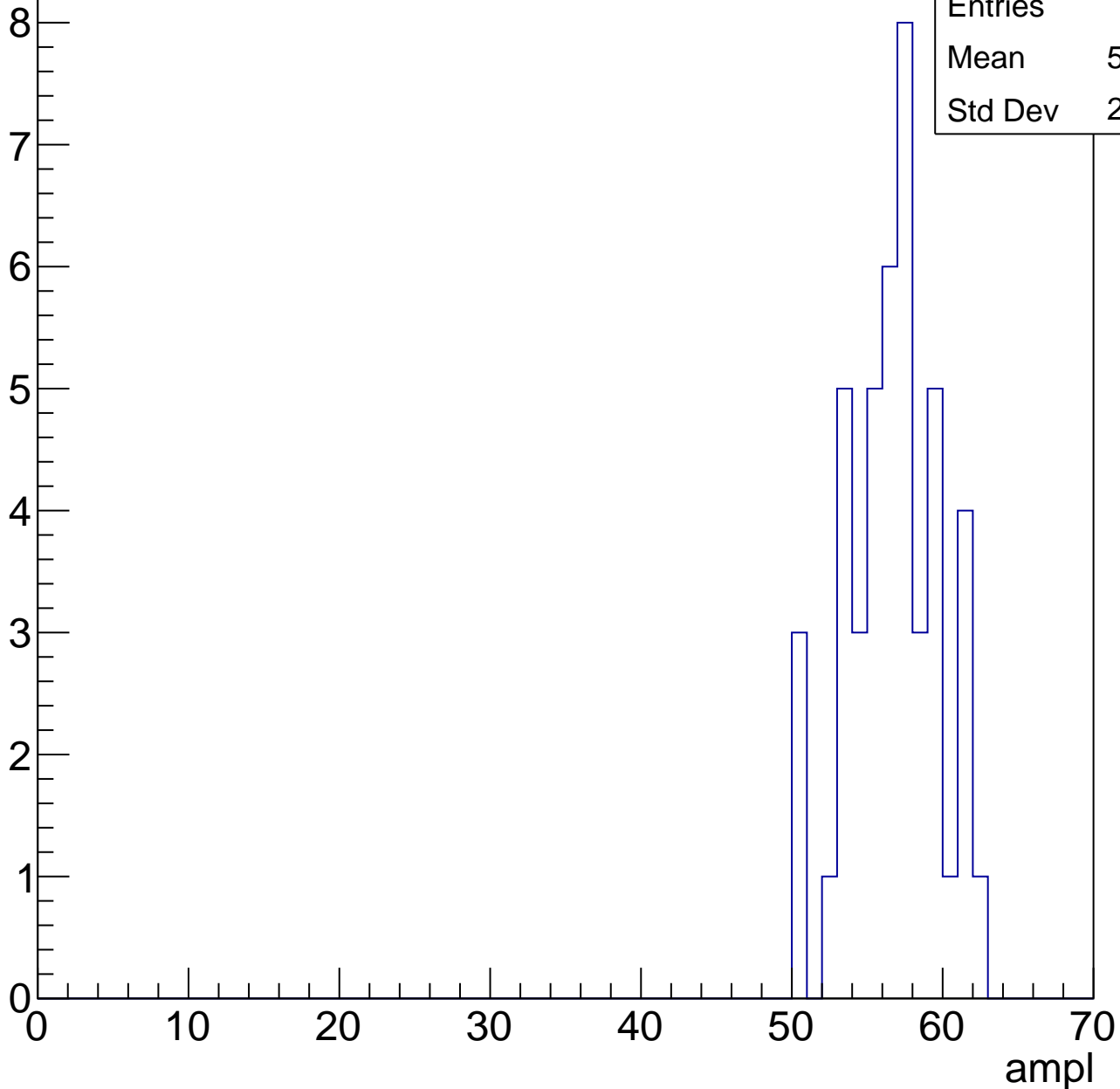
Entries	71
Mean	50.59
Std Dev	3.43

# B1L003S, U3-ch50, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	45
Mean	56.24
Std Dev	2.983



# B1L003S, U3-ch50, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

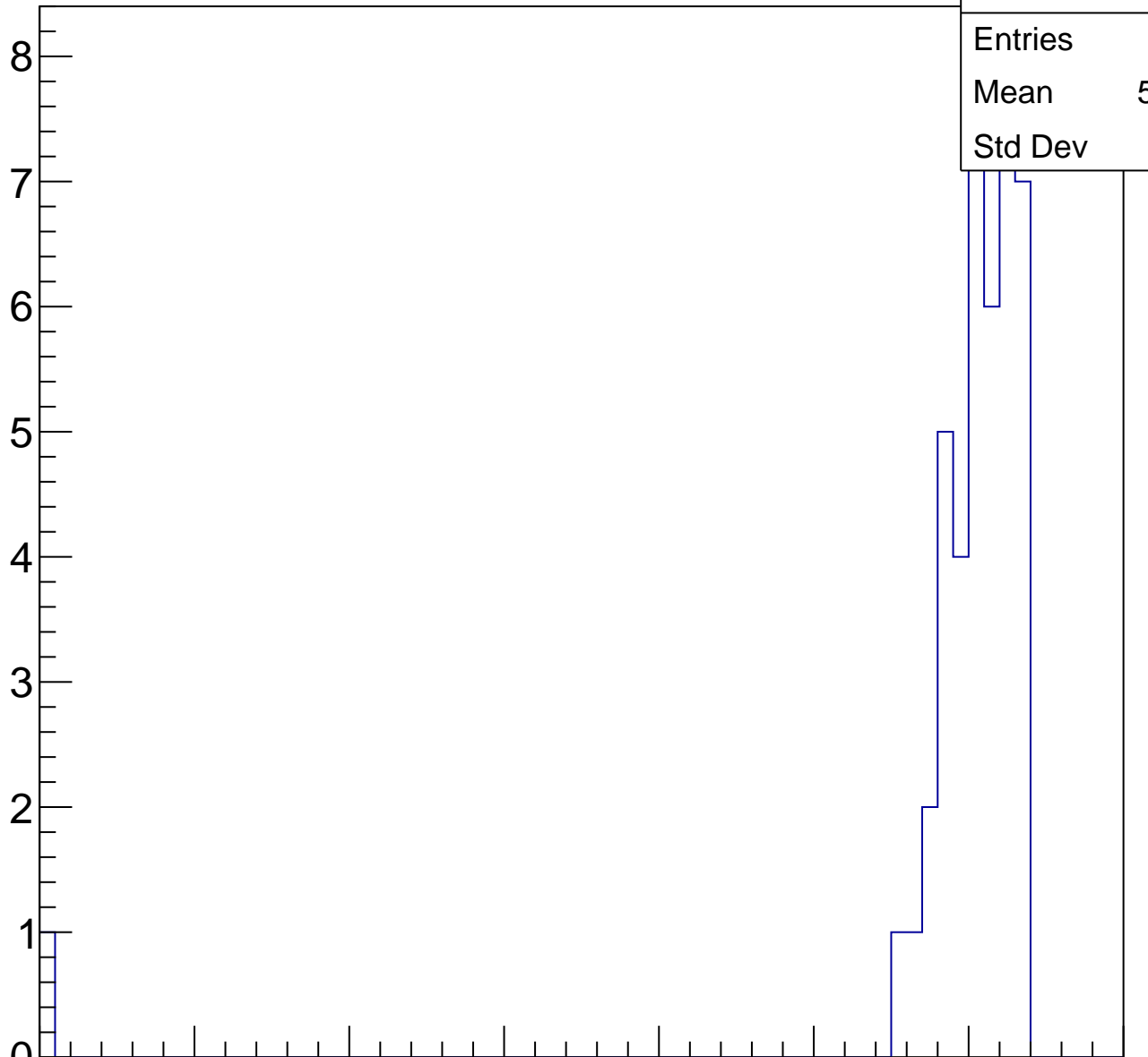
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	43
Mean	58.93
Std Dev	9.32

ampl

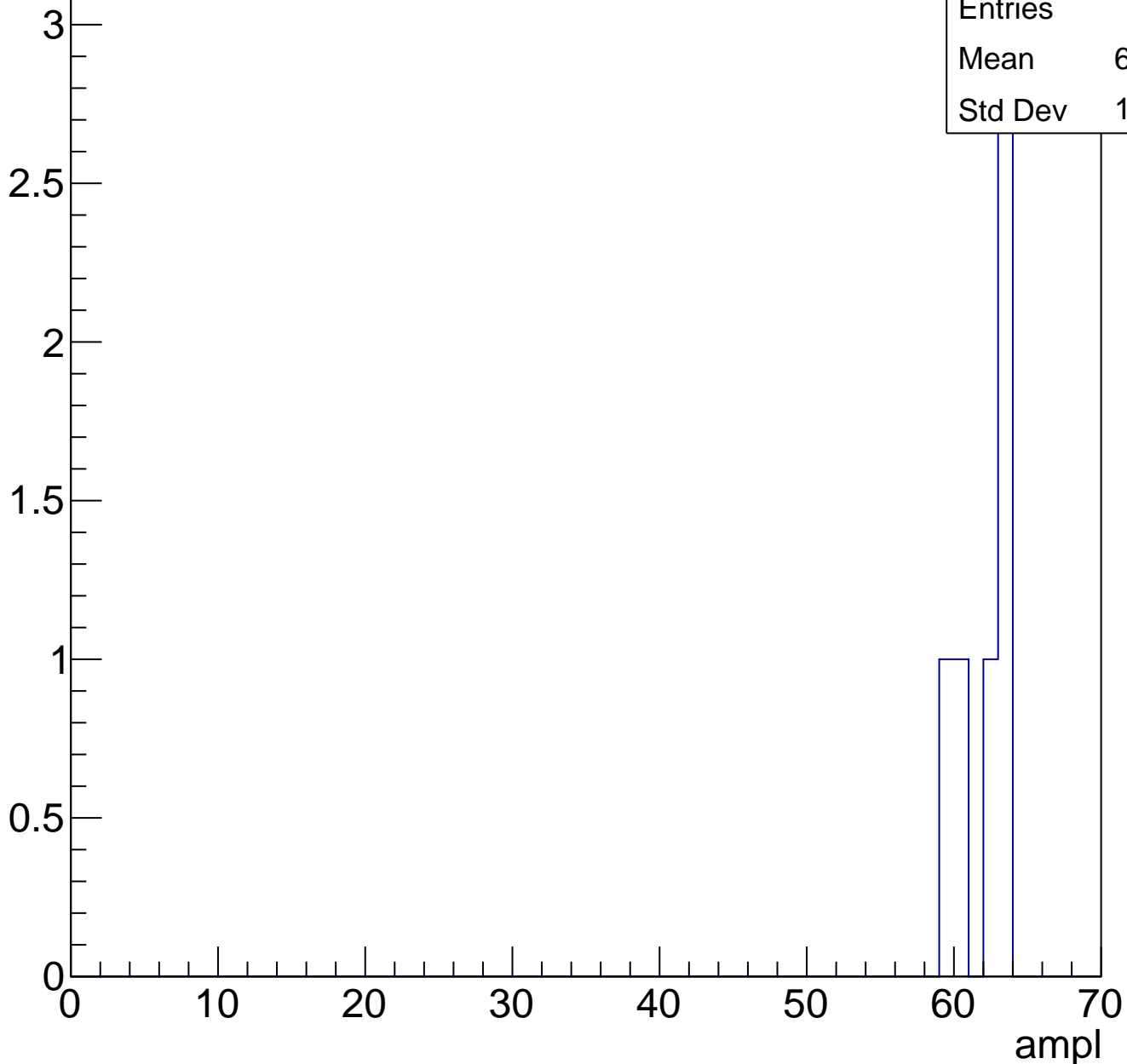
0 10 20 30 40 50 60 70



# B1L003S, U3-ch50, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch50, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U3-ch51, adc0

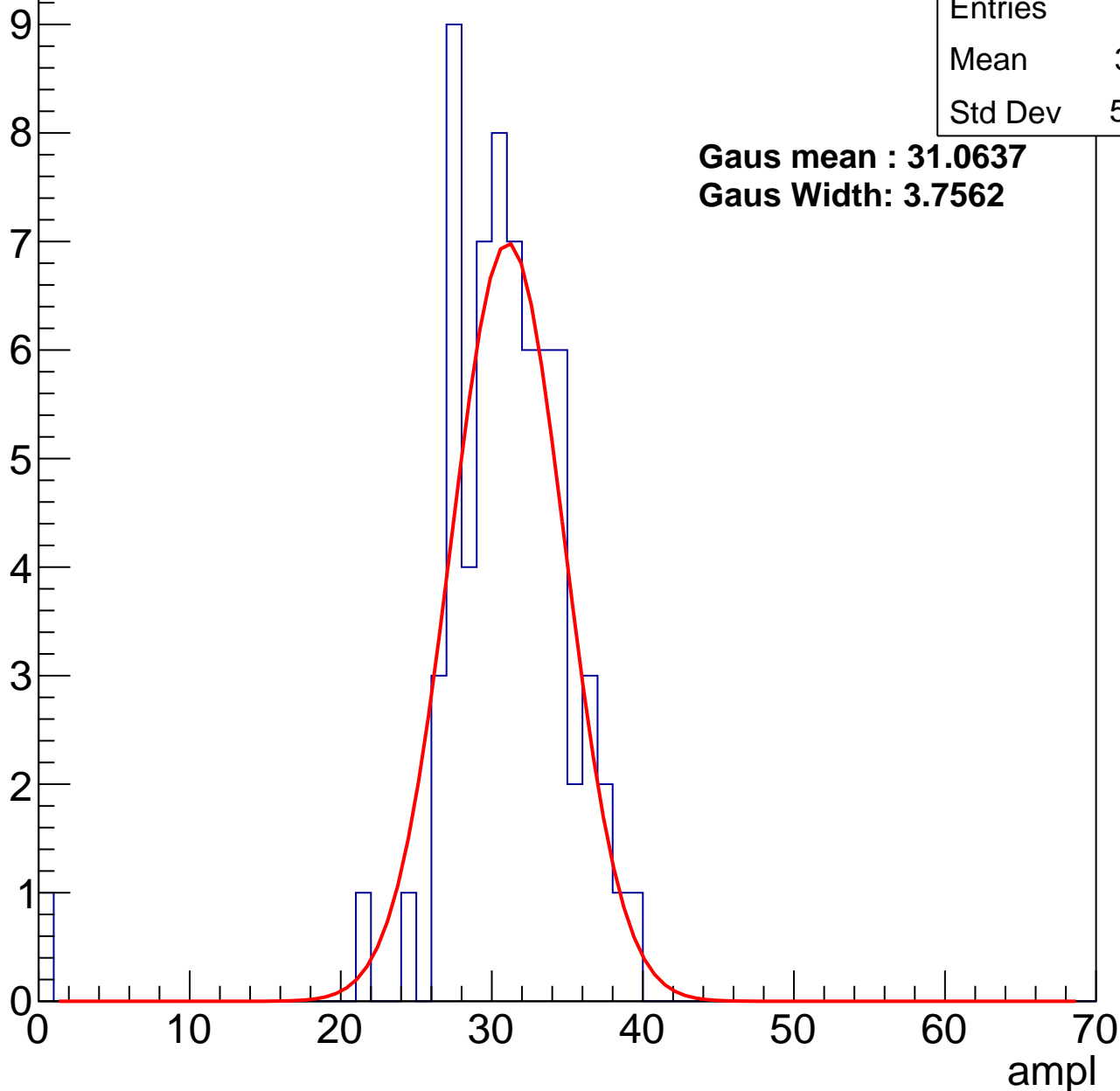
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	30.31
Std Dev	5.065

**Gaus mean : 31.0637**

**Gaus Width: 3.7562**



# B1L003S, U3-ch51, adc1

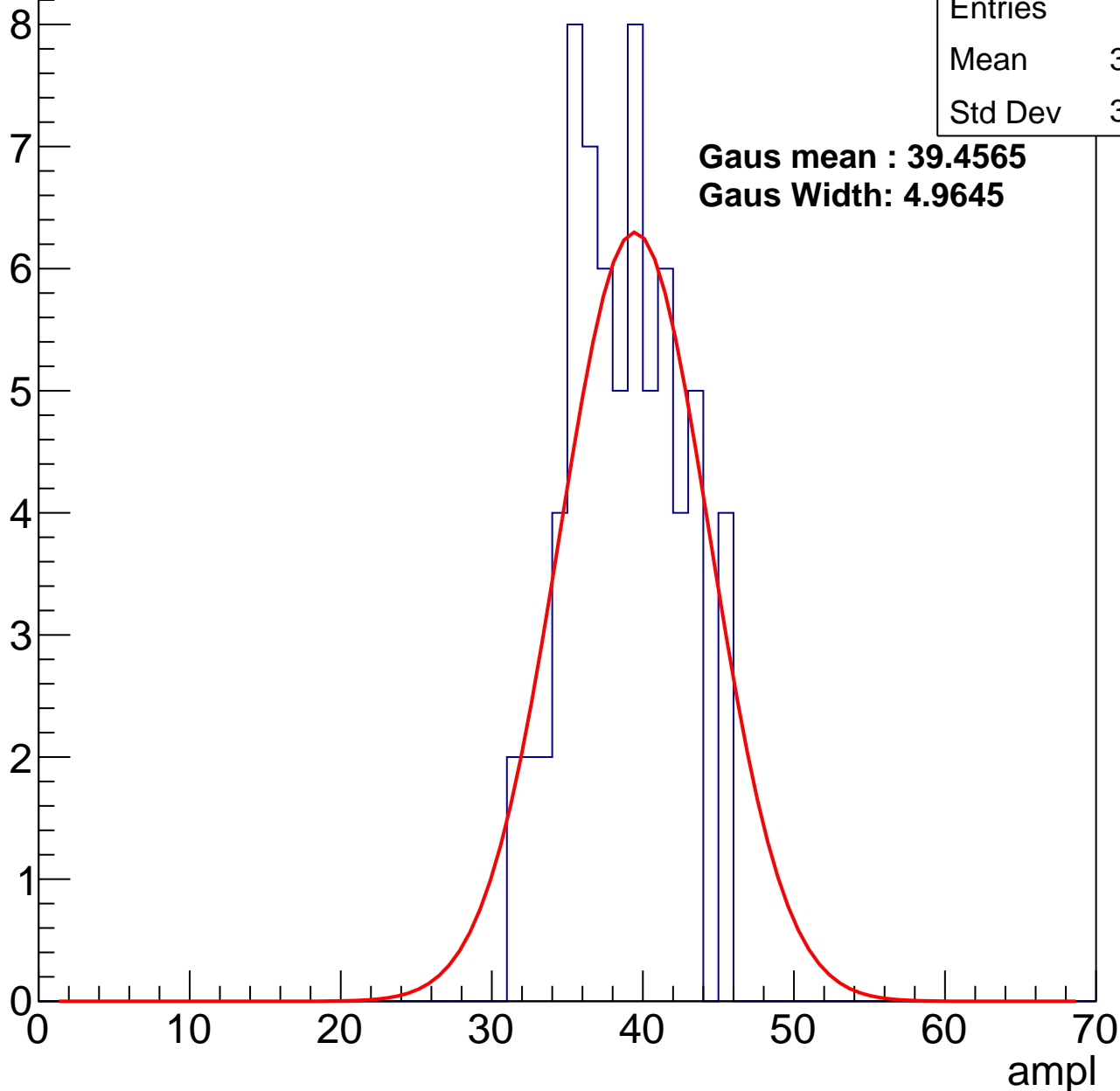
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	38.13
Std Dev	3.548

**Gaus mean : 39.4565**

**Gaus Width: 4.9645**



# B1L003S, U3-ch51, adc2

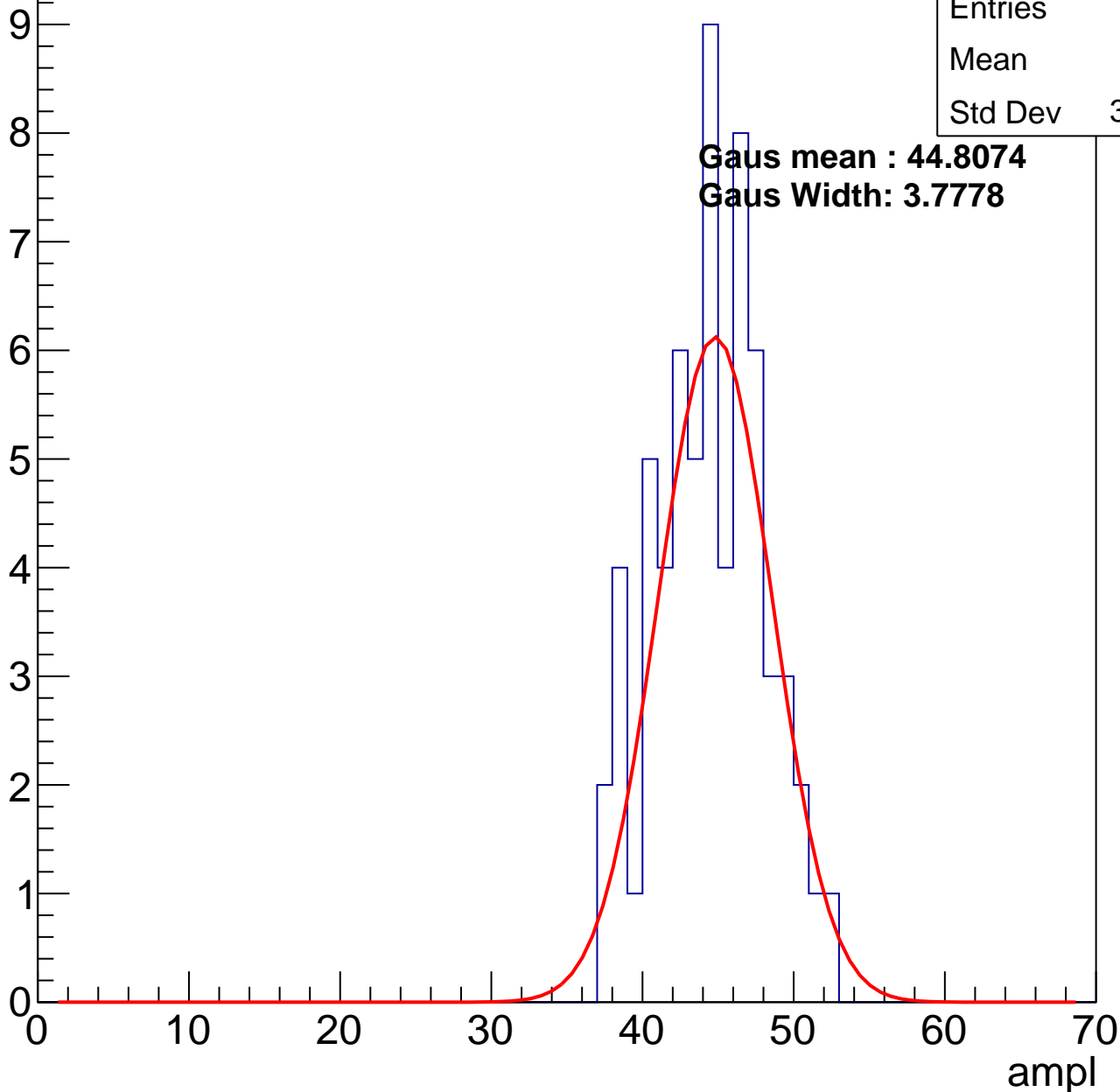
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	44
Std Dev	3.558

**Gaus mean : 44.8074**

**Gaus Width: 3.7778**

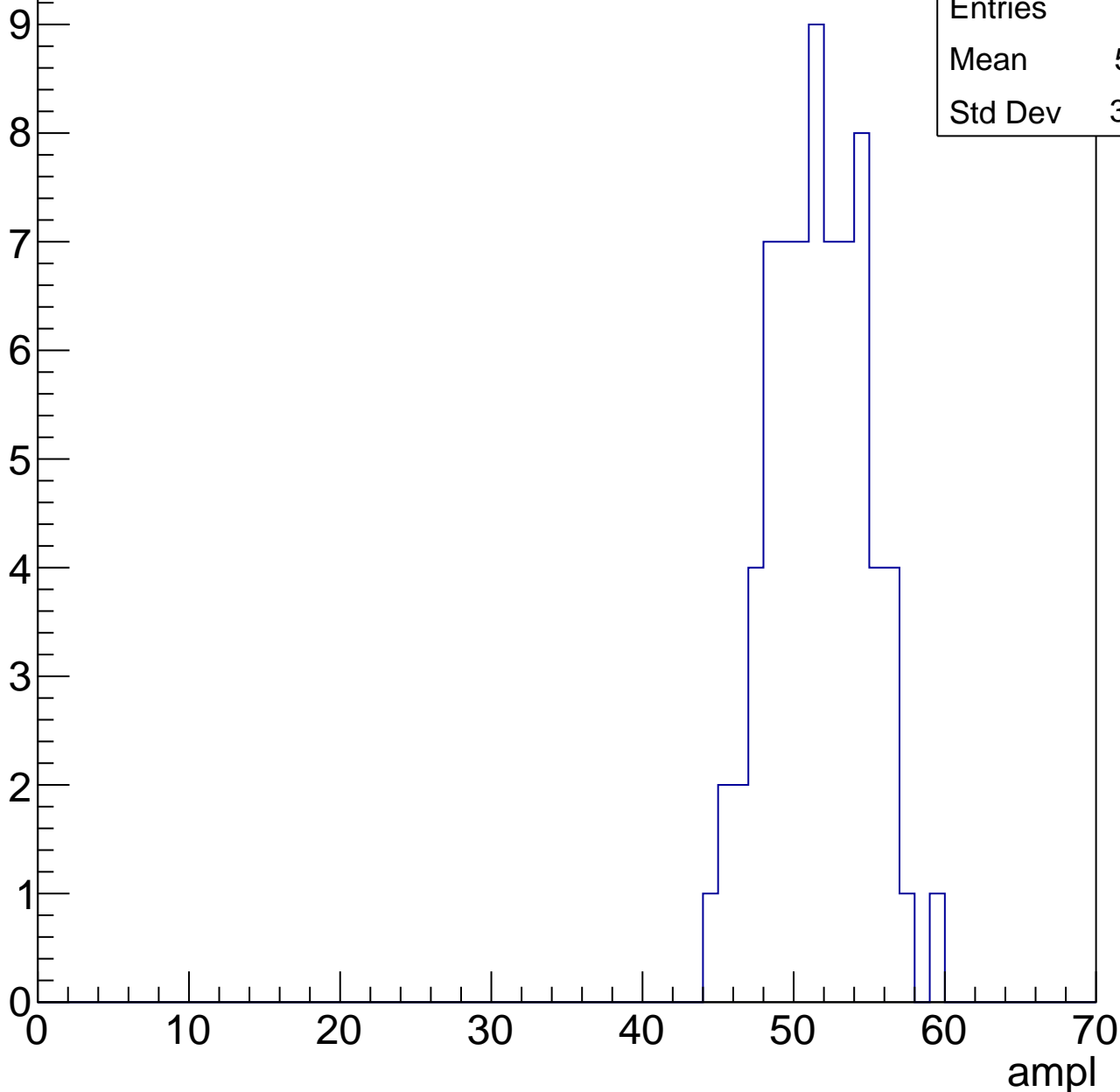


# B1L003S, U3-ch51, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	71
Mean	51.11
Std Dev	3.147

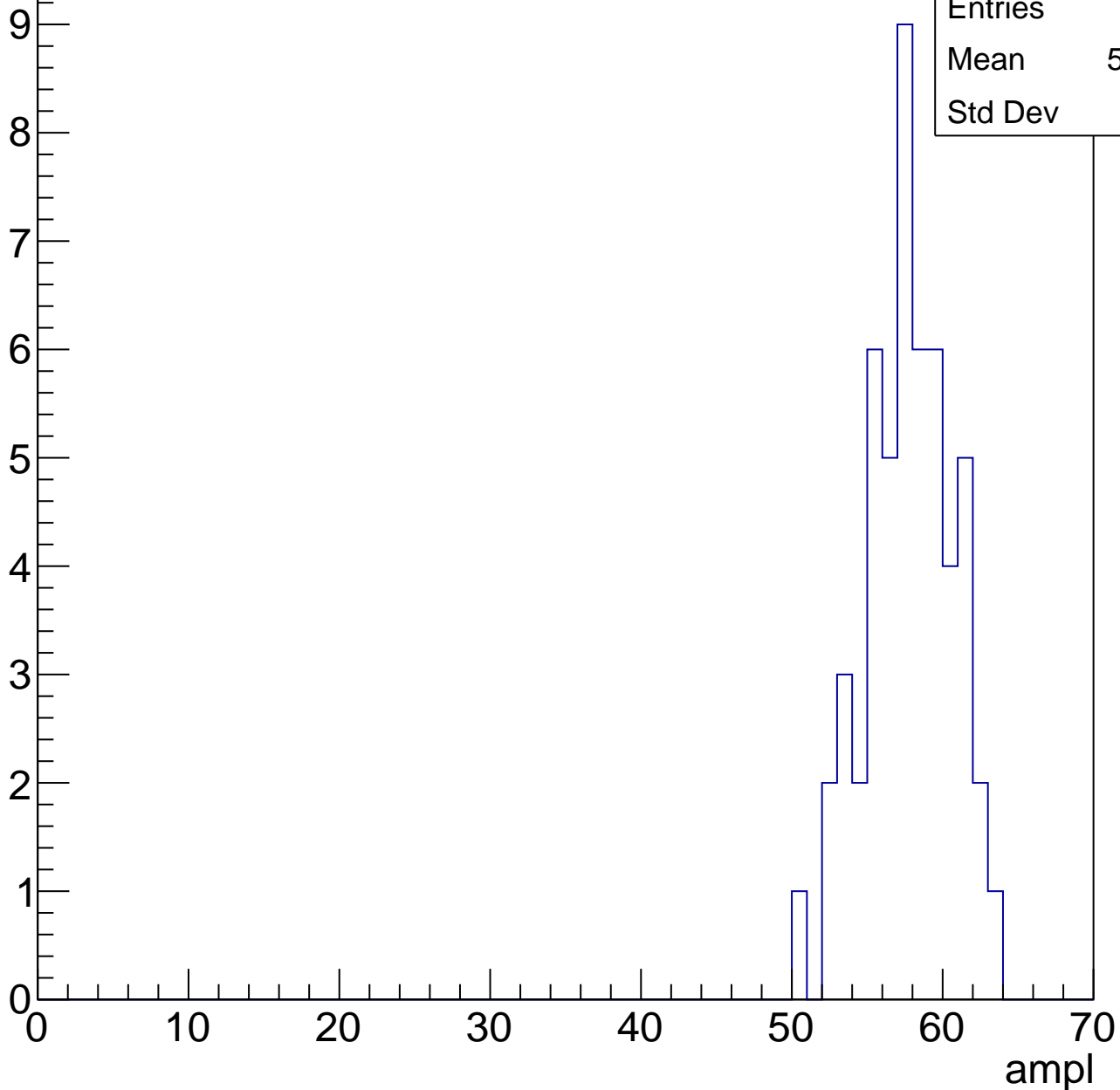


# B1L003S, U3-ch51, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	52
Mean	57.27
Std Dev	2.85

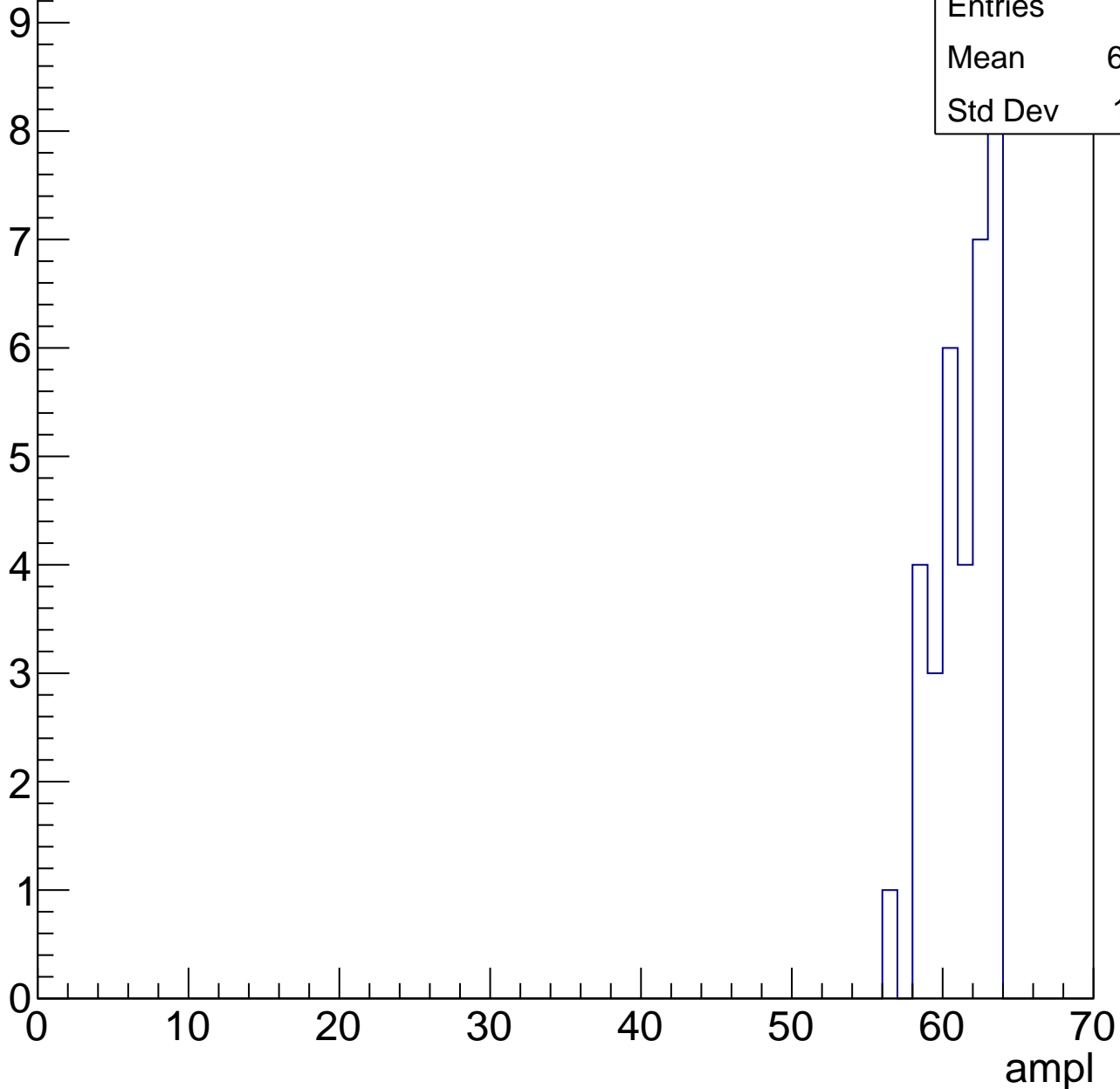


# B1L003S, U3-ch51, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

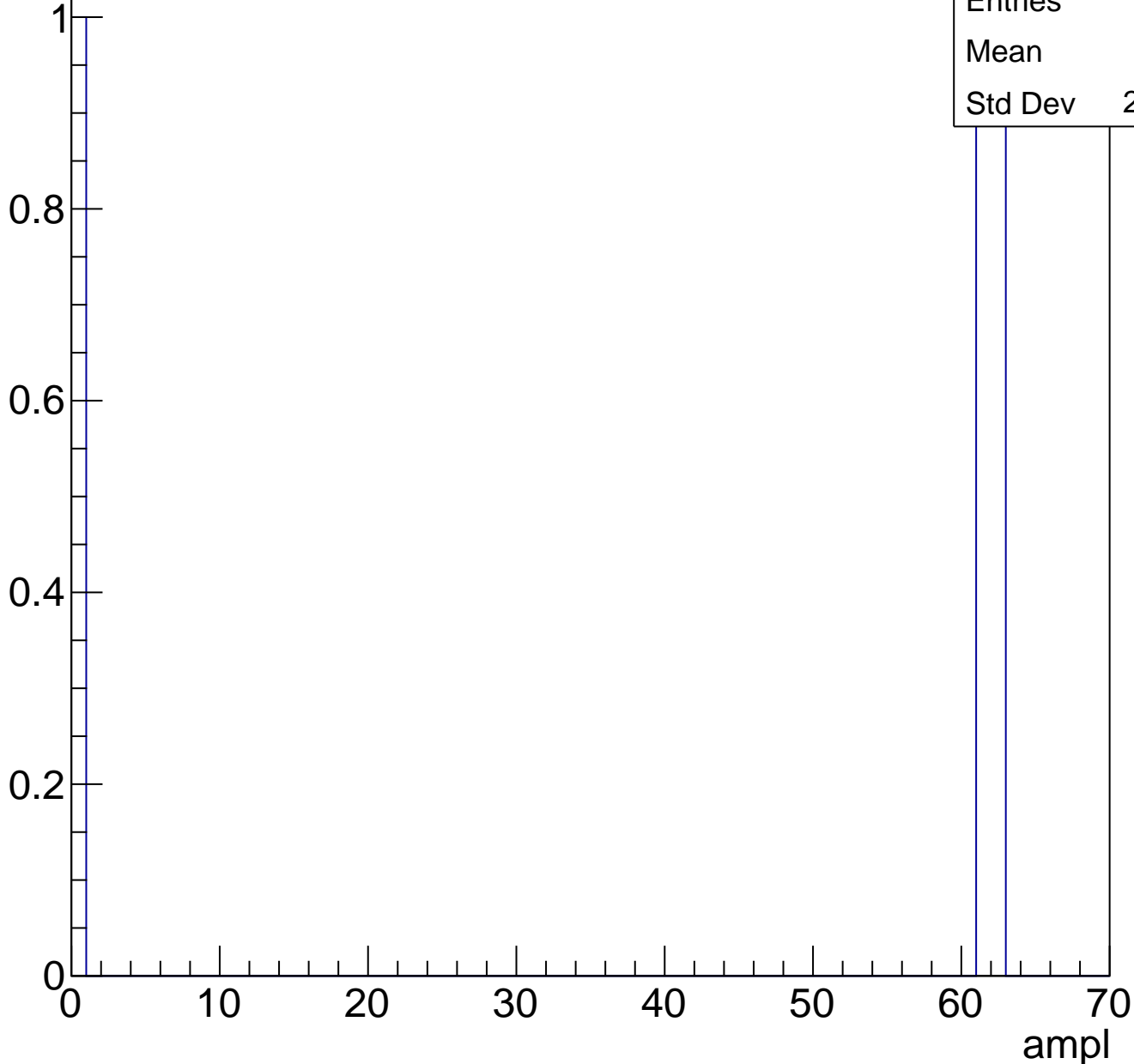
Entries	34
Mean	60.88
Std Dev	1.891



# B1L003S, U3-ch51, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch51, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U3-ch52, adc0

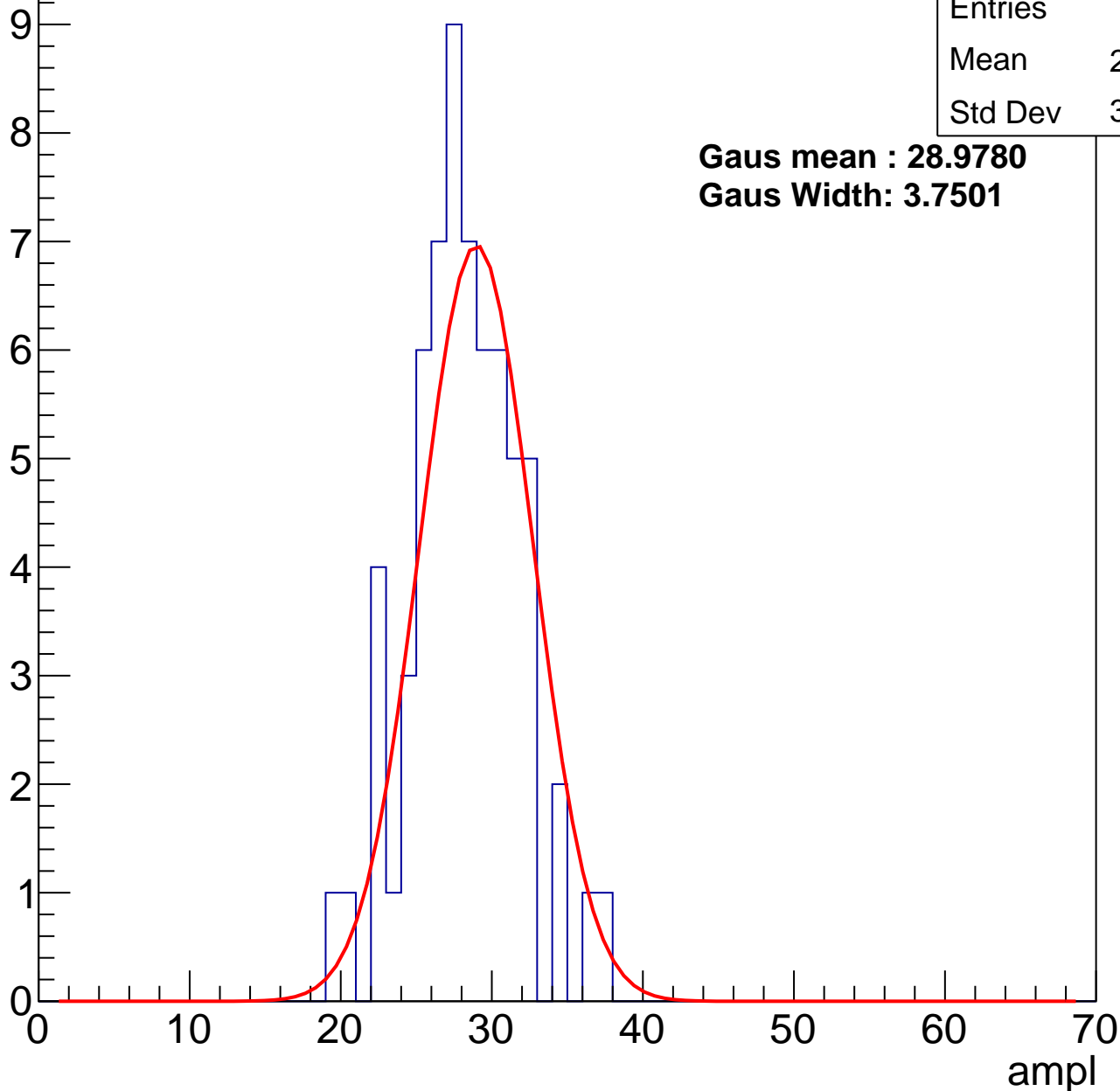
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	27.74
Std Dev	3.553

**Gaus mean : 28.9780**

**Gaus Width: 3.7501**



# B1L003S, U3-ch52, adc1

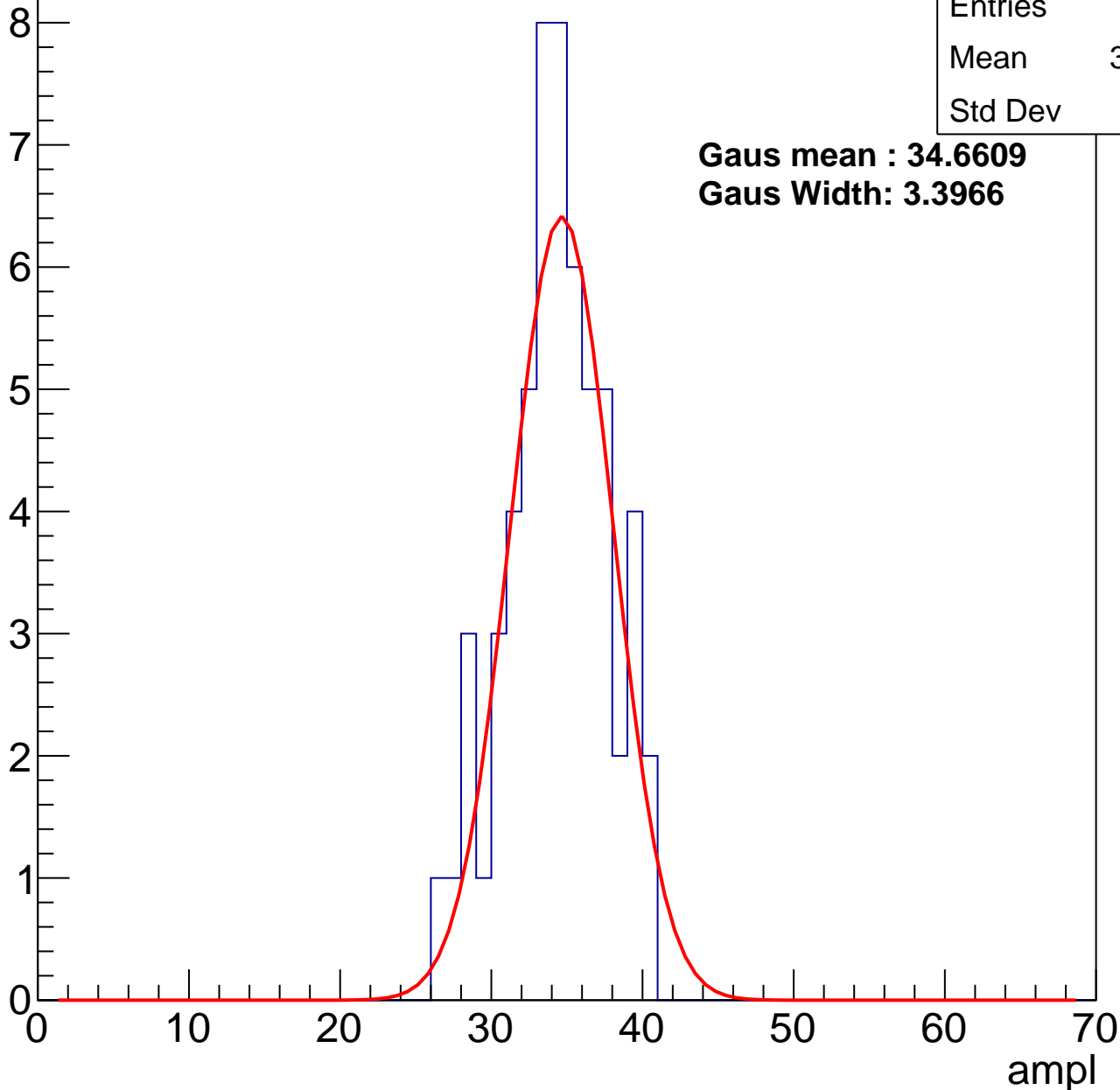
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	33.84
Std Dev	3.3

**Gaus mean : 34.6609**

**Gaus Width: 3.3966**



# B1L003S, U3-ch52, adc2

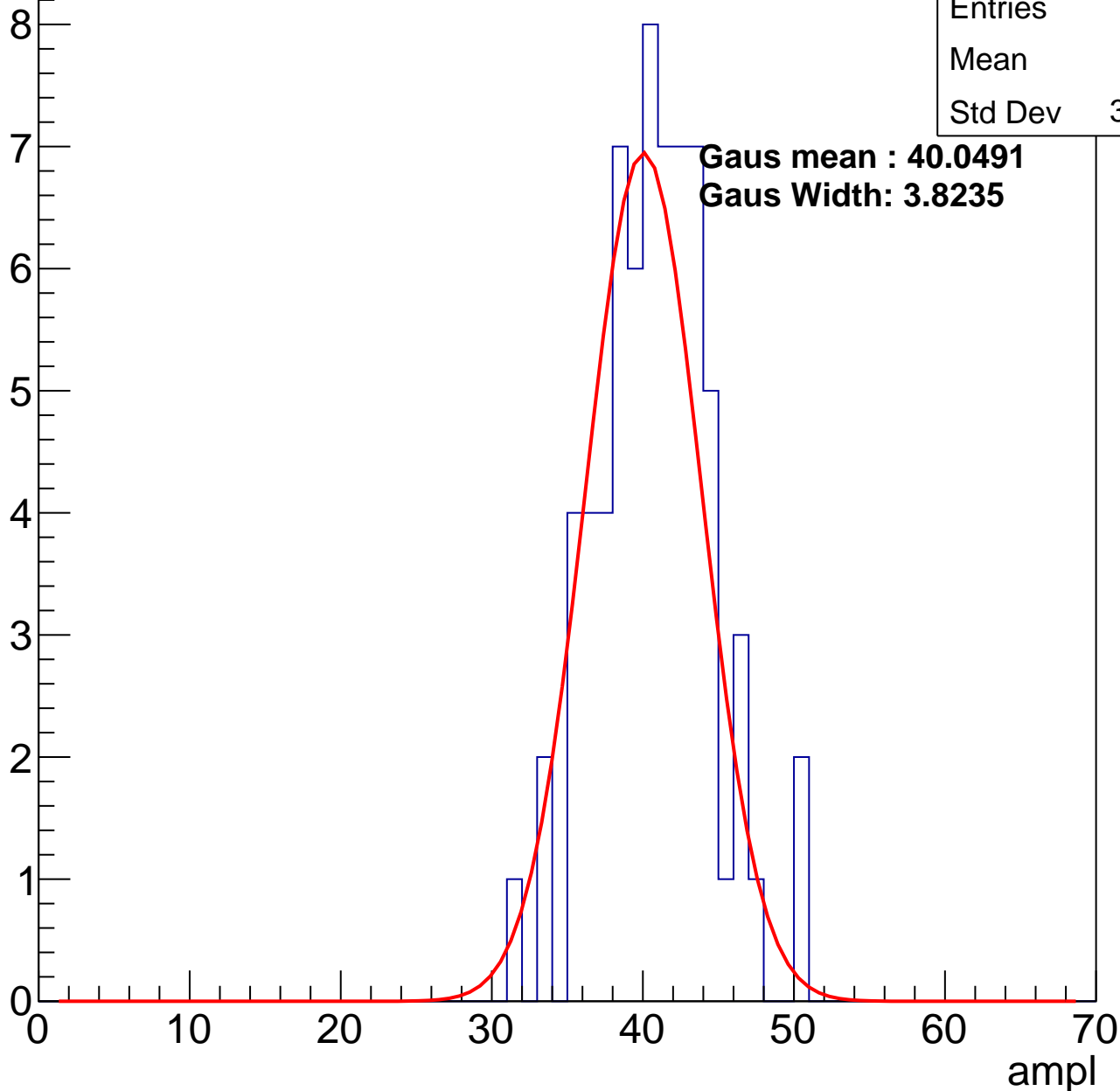
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	40.3
Std Dev	3.743

**Gaus mean : 40.0491**

**Gaus Width: 3.8235**

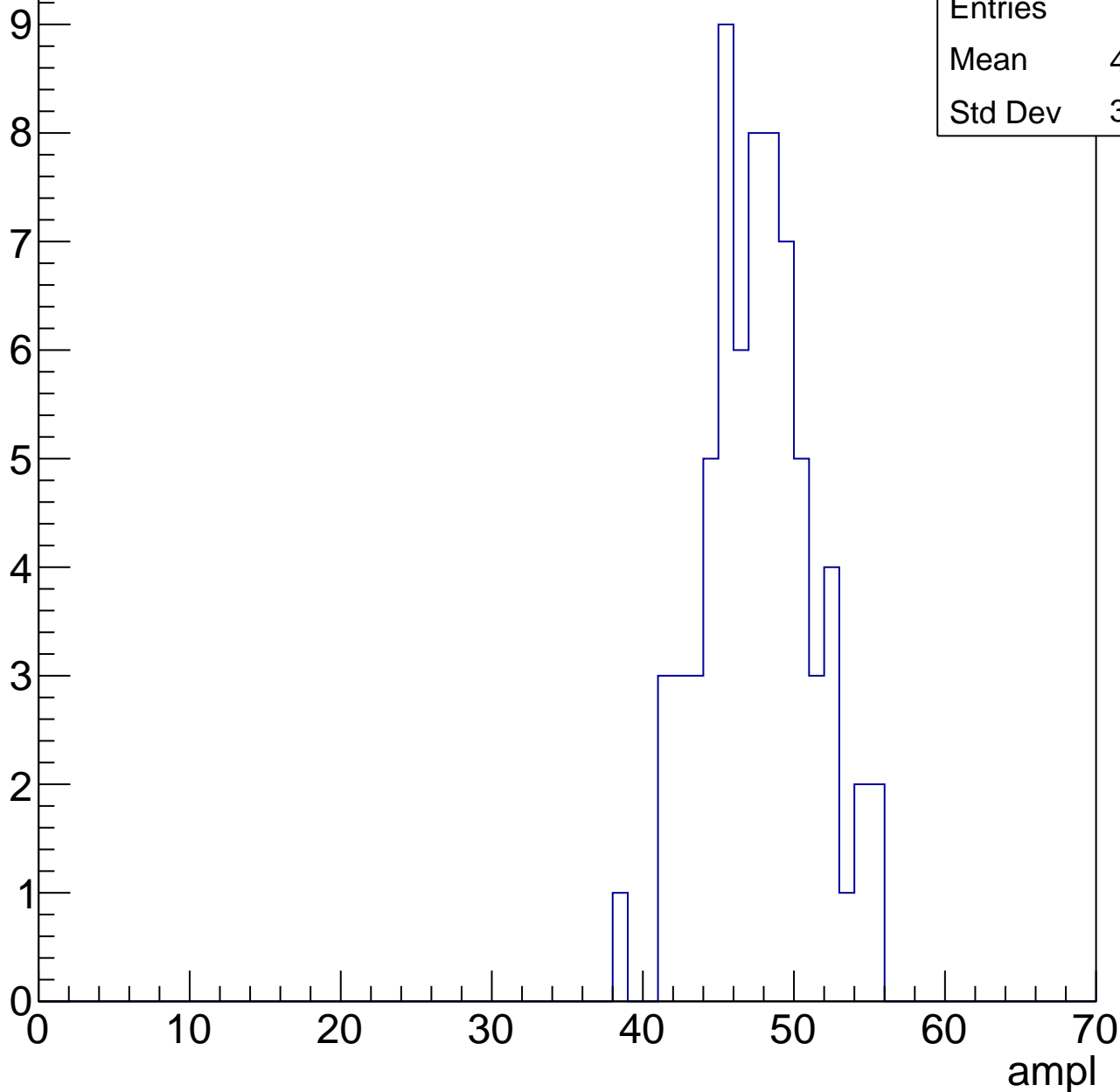


# B1L003S, U3-ch52, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	47.17
Std Dev	3.562

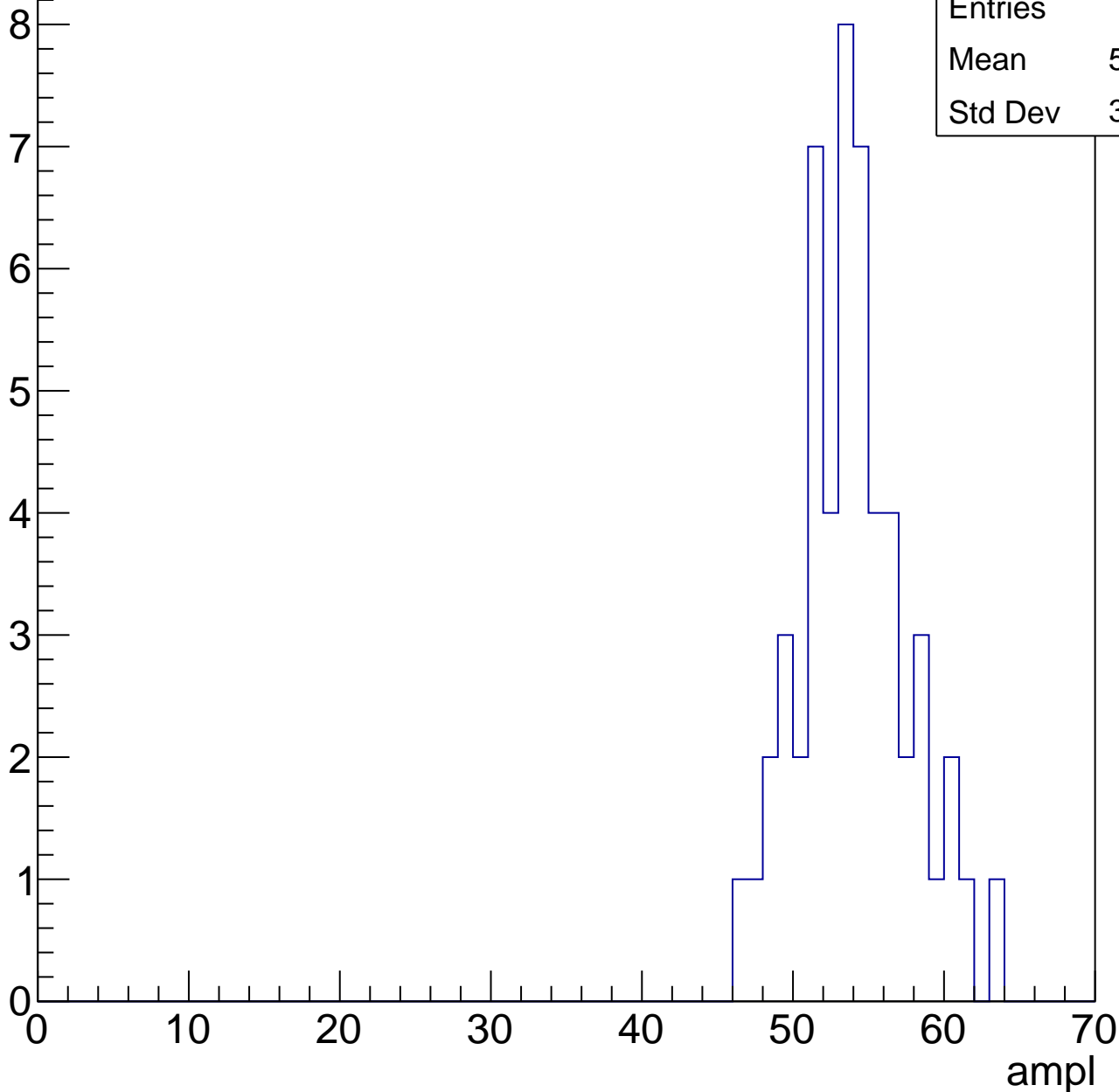


# B1L003S, U3-ch52, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

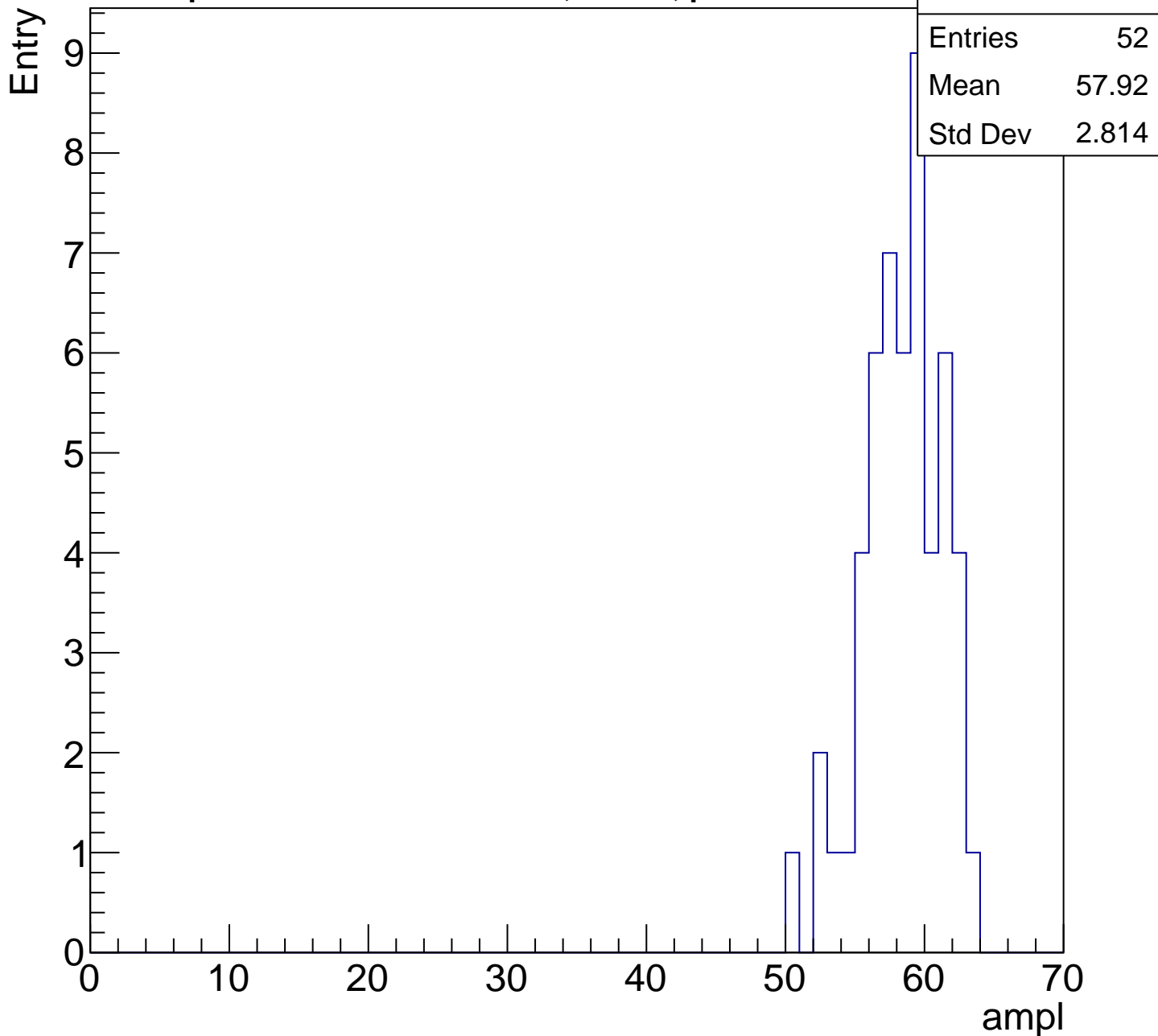
Entry

Entries	53
Mean	53.55
Std Dev	3.585



# B1L003S, U3-ch52, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

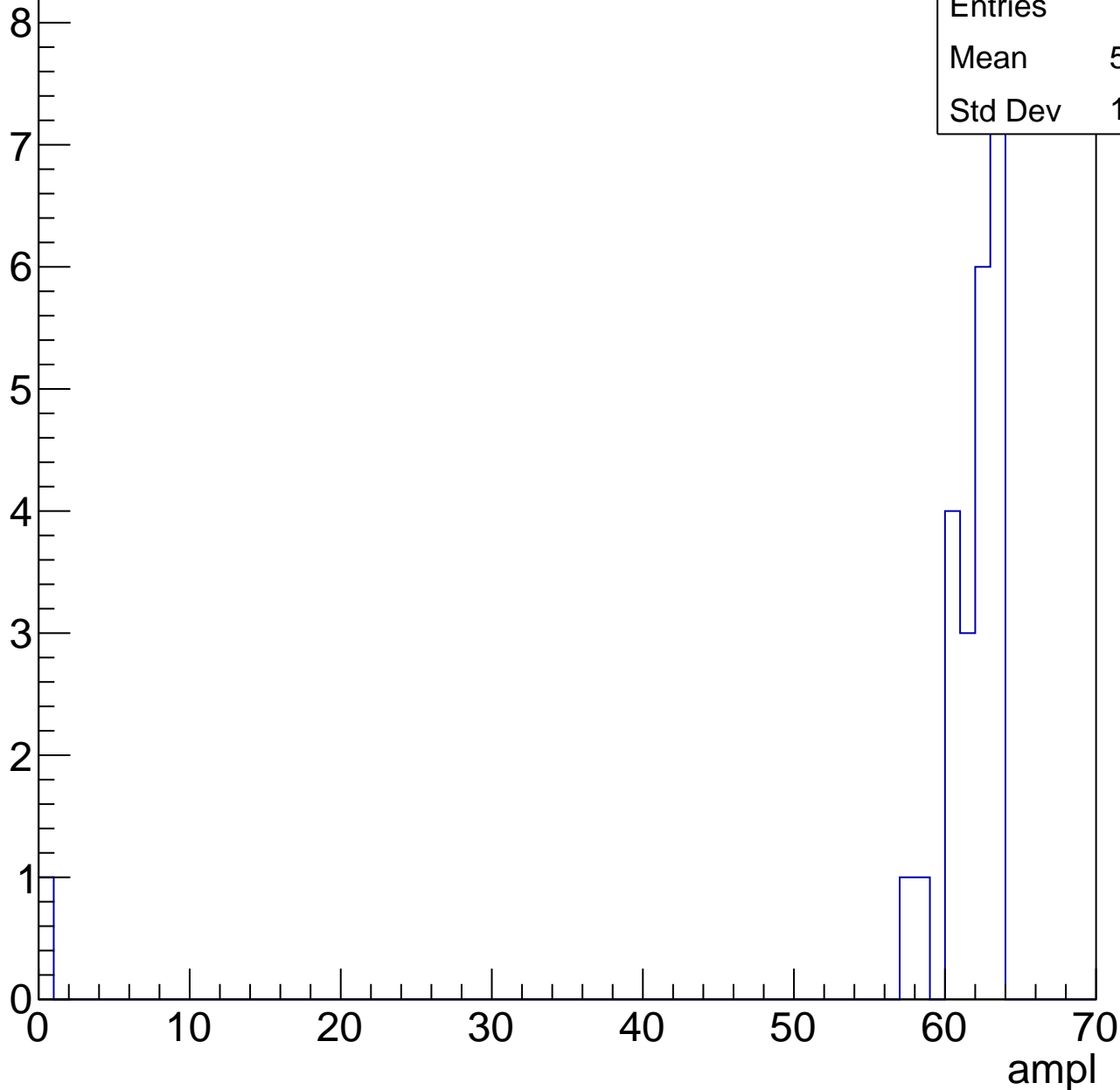


# B1L003S, U3-ch52, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	24
Mean	58.92
Std Dev	12.39





# B1L003S, U3-ch52, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U3-ch53, adc0

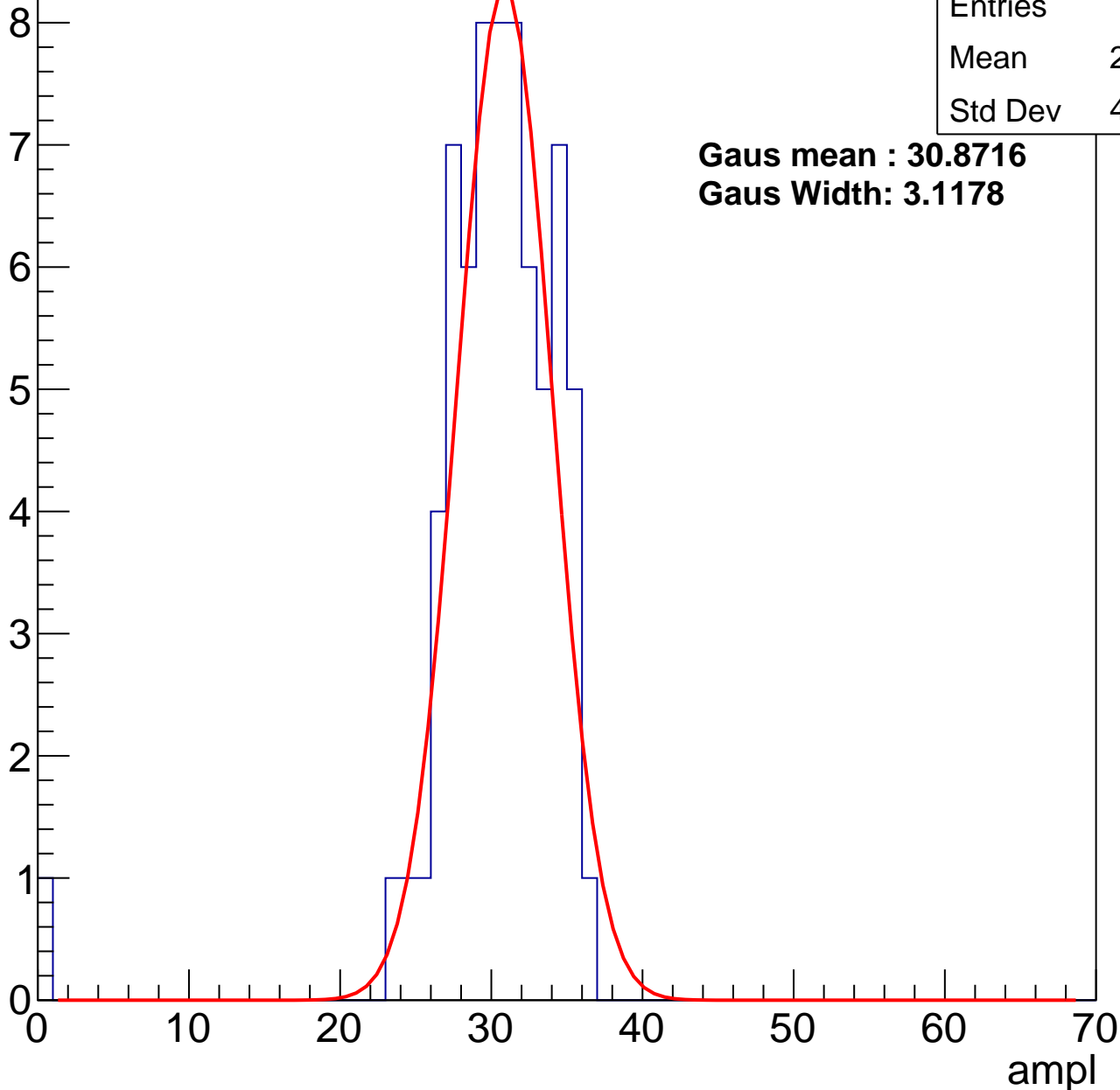
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	29.84
Std Dev	4.689

**Gaus mean : 30.8716**

**Gaus Width: 3.1178**



# B1L003S, U3-ch53, adc1

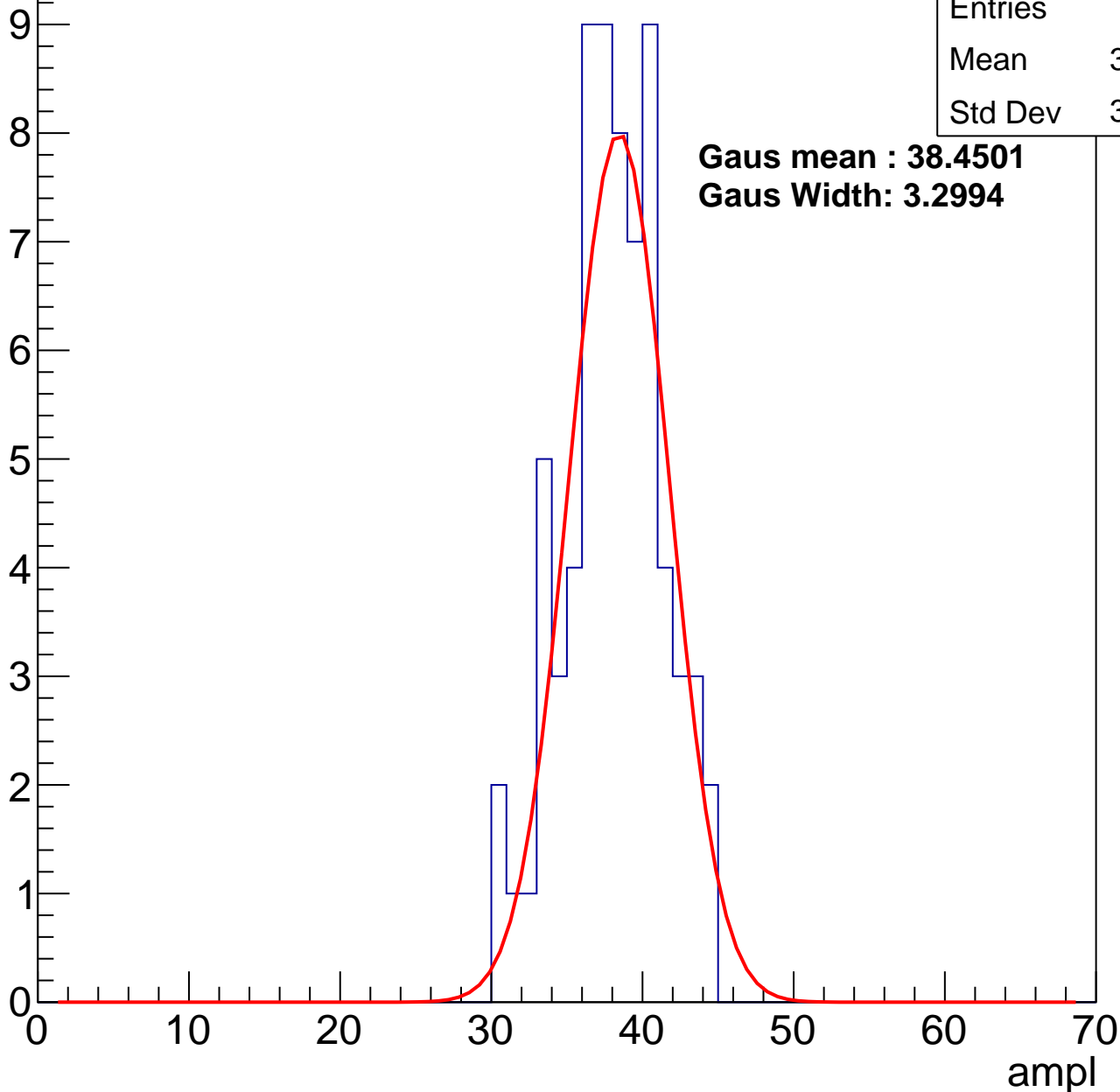
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	37.59
Std Dev	3.227

**Gaus mean : 38.4501**

**Gaus Width: 3.2994**

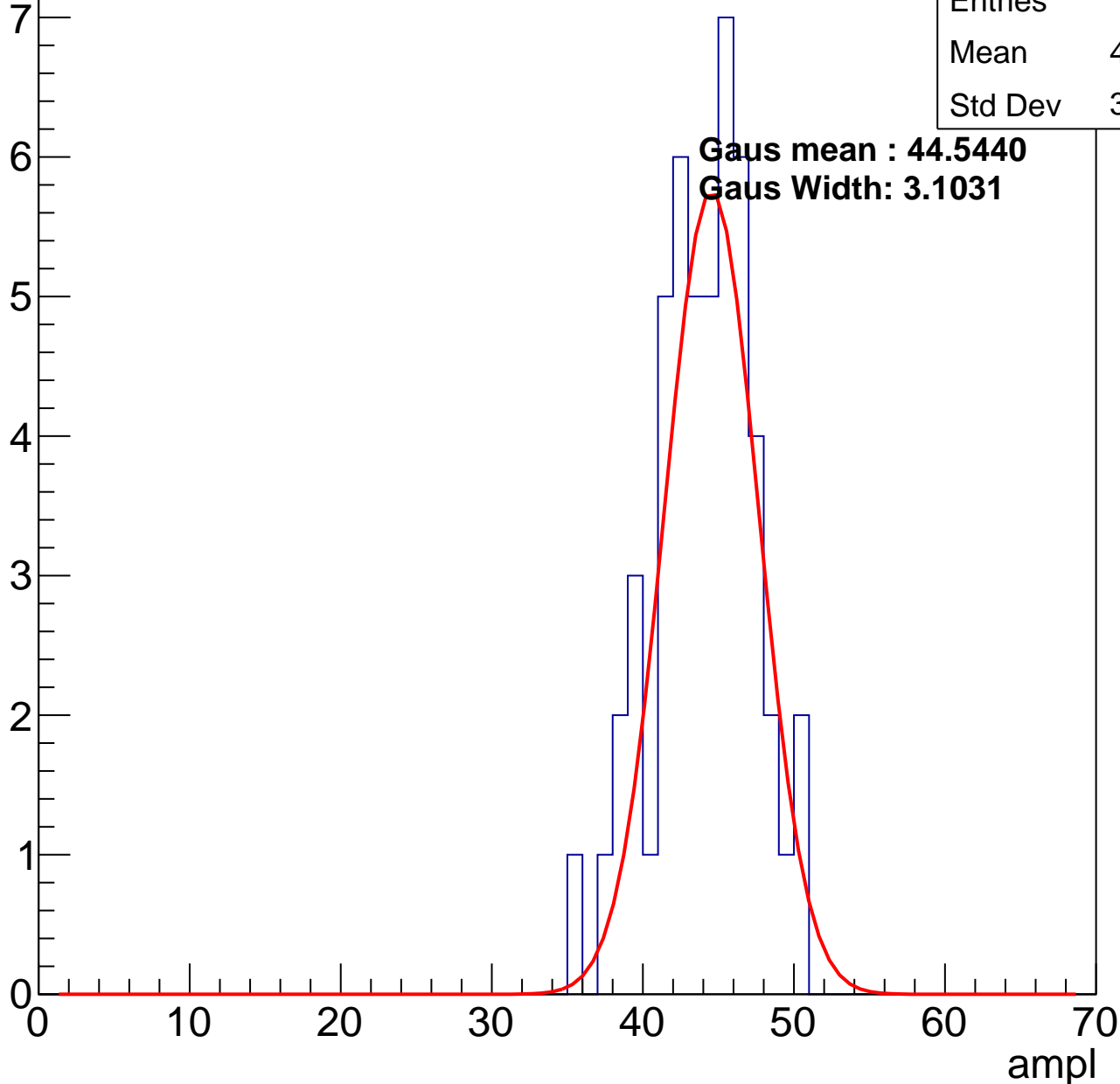


# B1L003S, U3-ch53, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	51
Mean	43.55
Std Dev	3.292

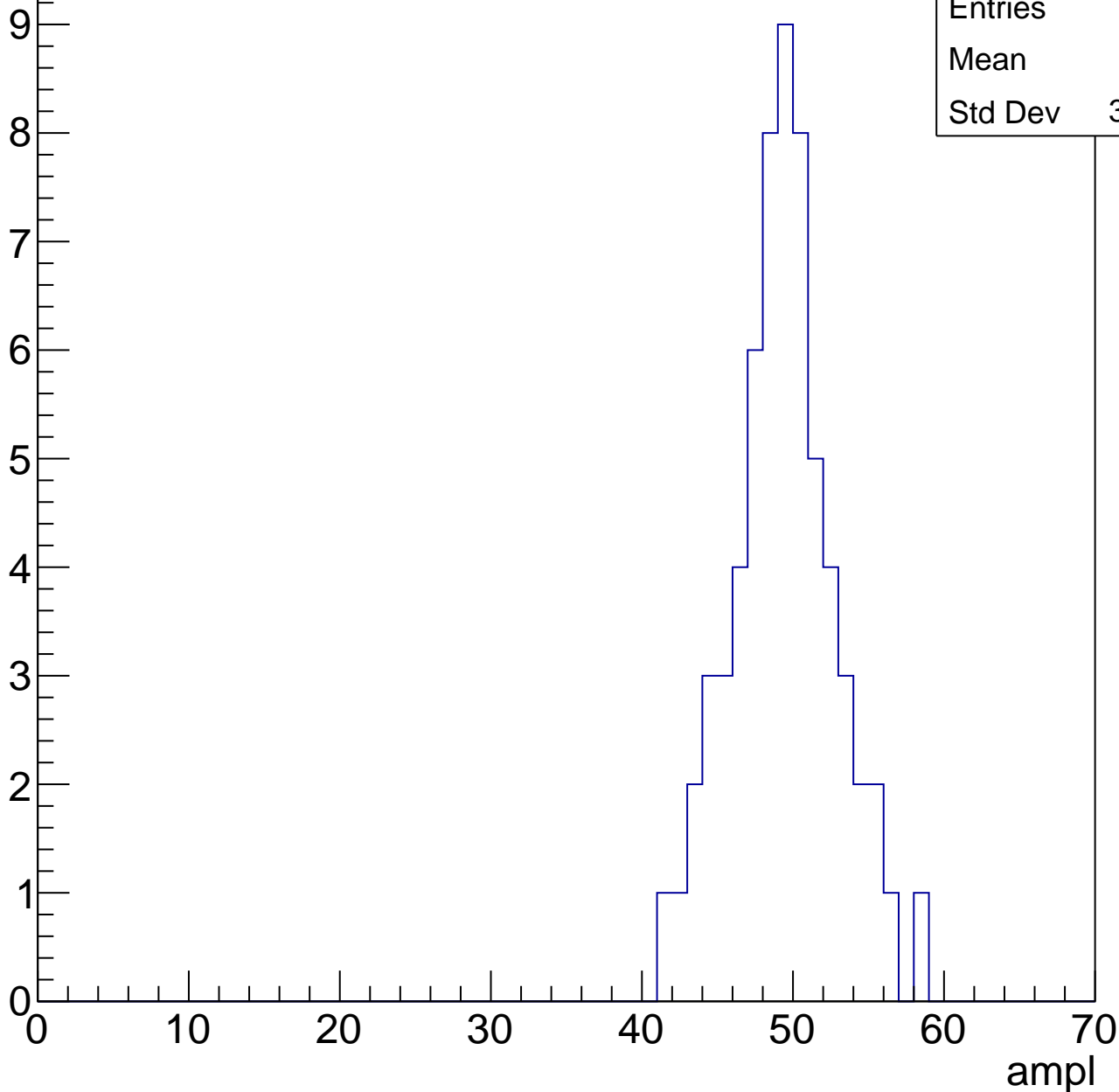


# B1L003S, U3-ch53, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	48.9
Std Dev	3.426

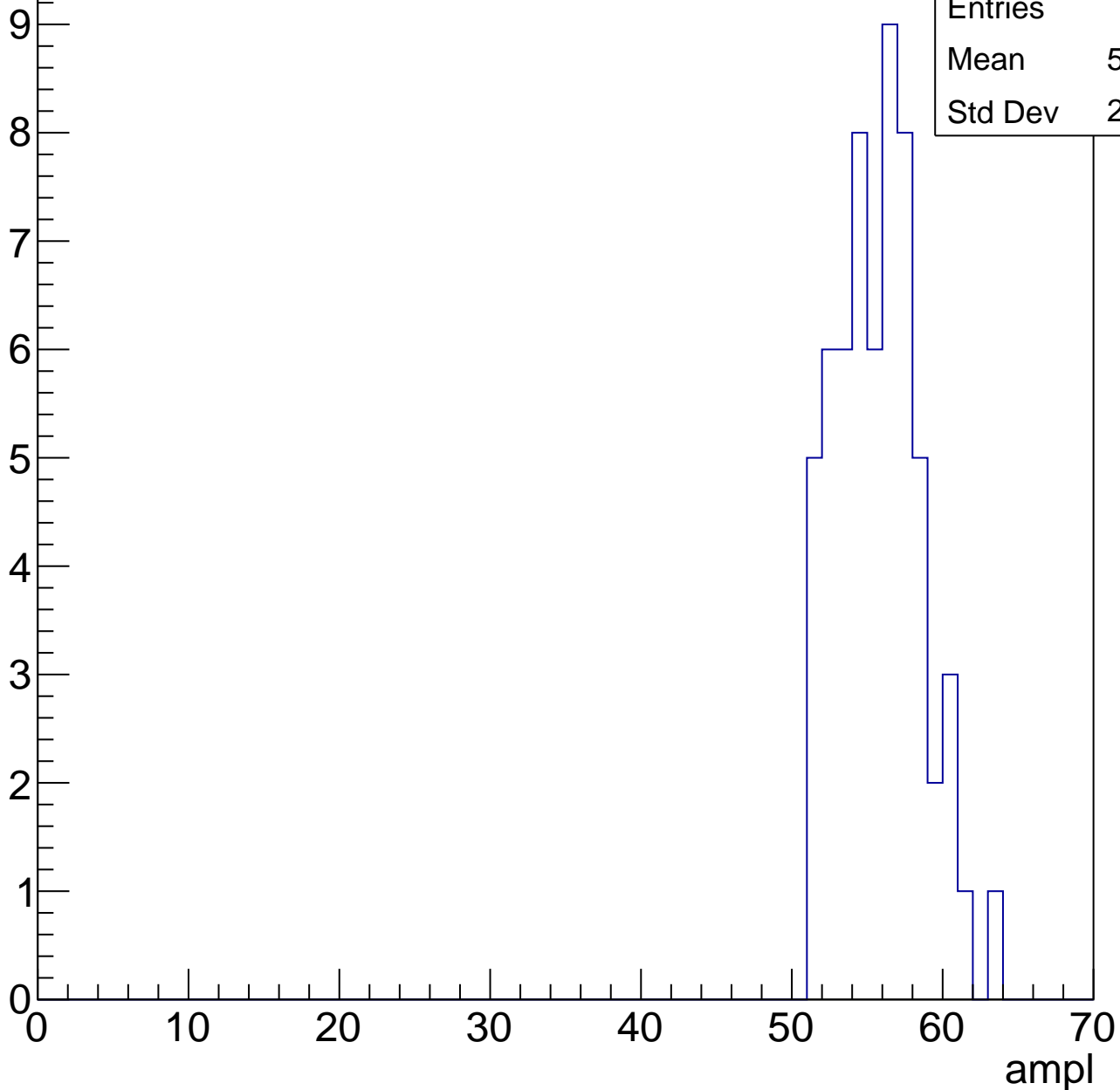


# B1L003S, U3-ch53, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

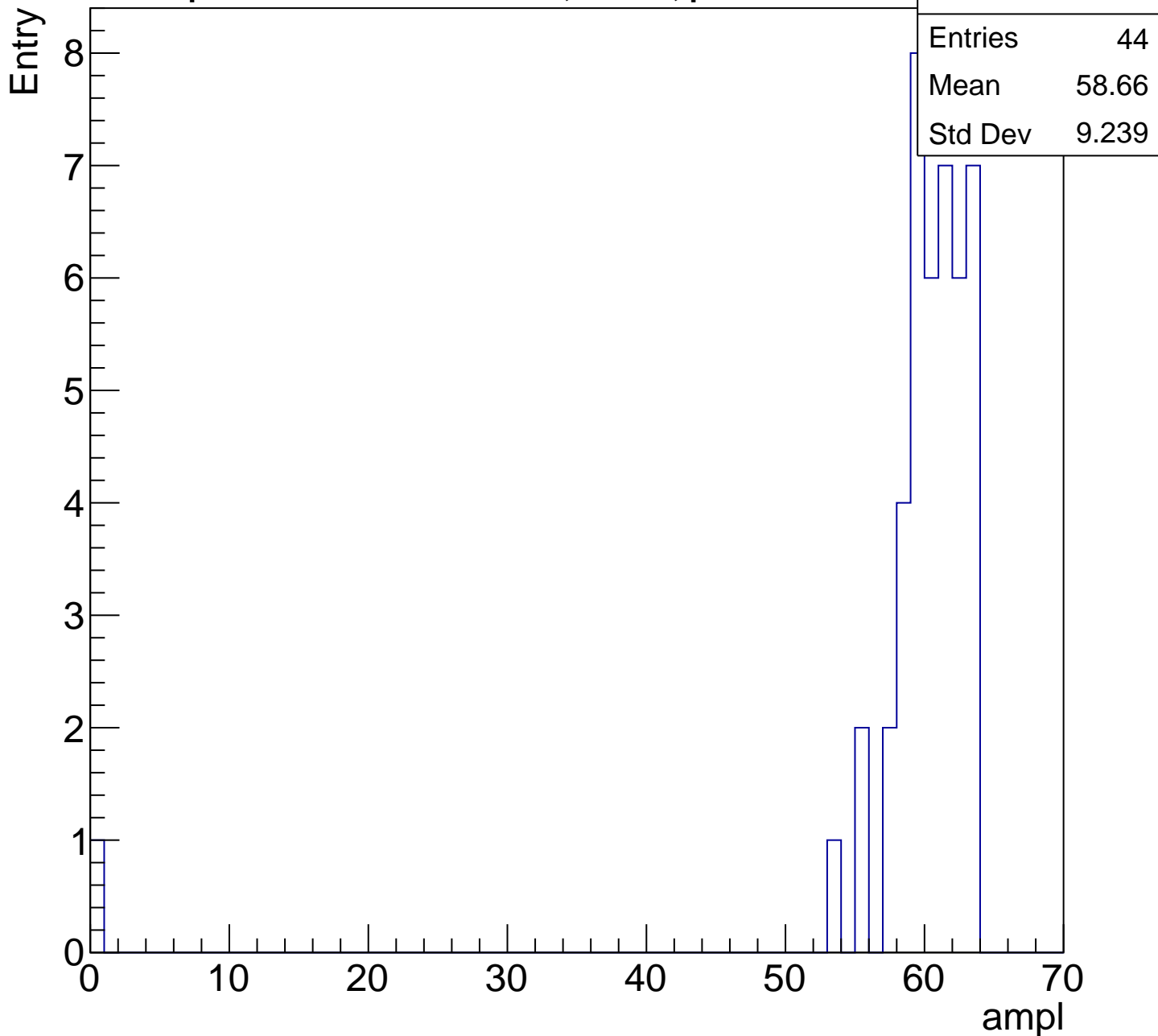
Entry

Entries	60
Mean	55.32
Std Dev	2.748



# B1L003S, U3-ch53, adc5

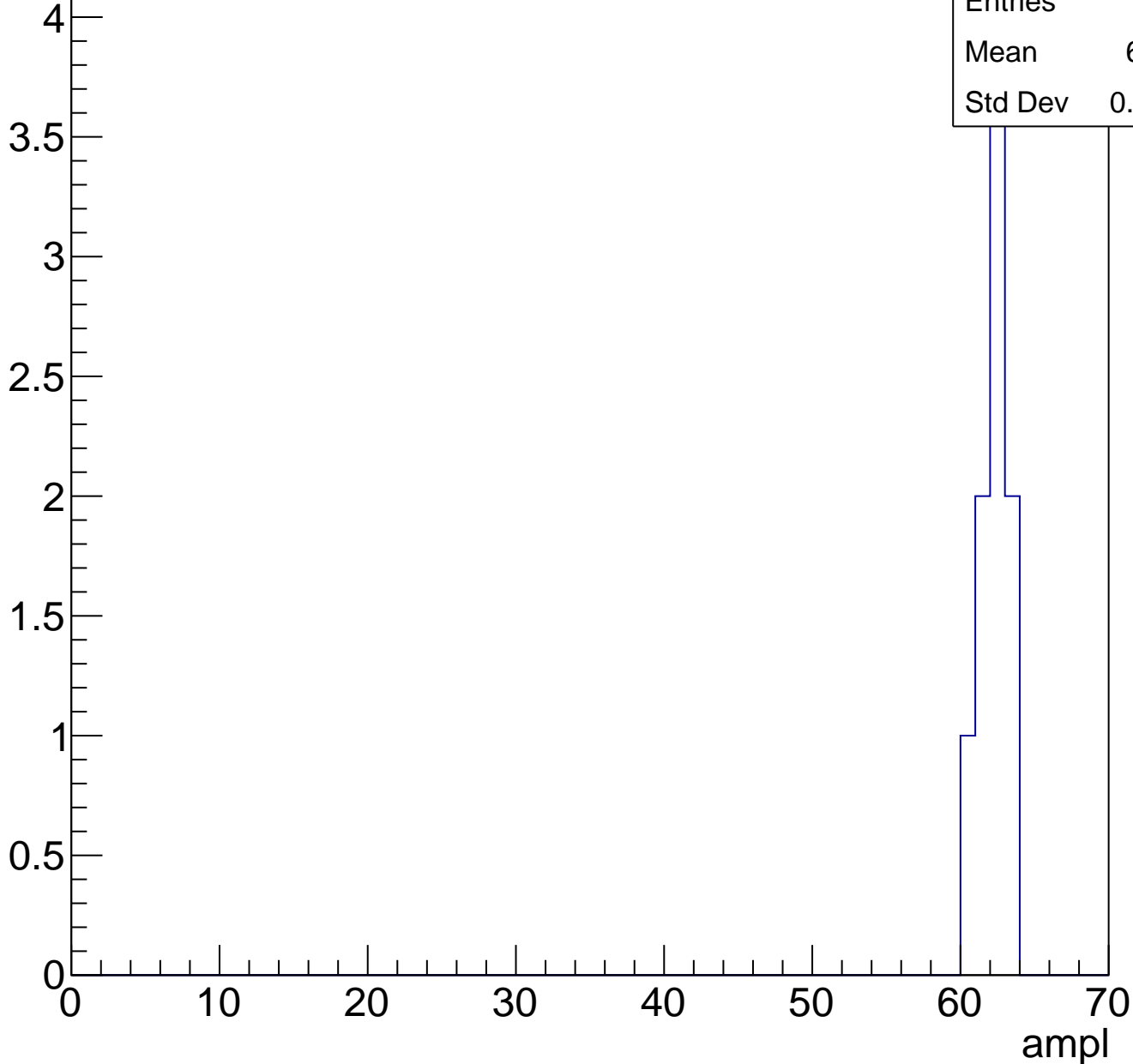
calib\_packv5\_042523\_0143.root, FC#13, port D2



# B1L003S, U3-ch53, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

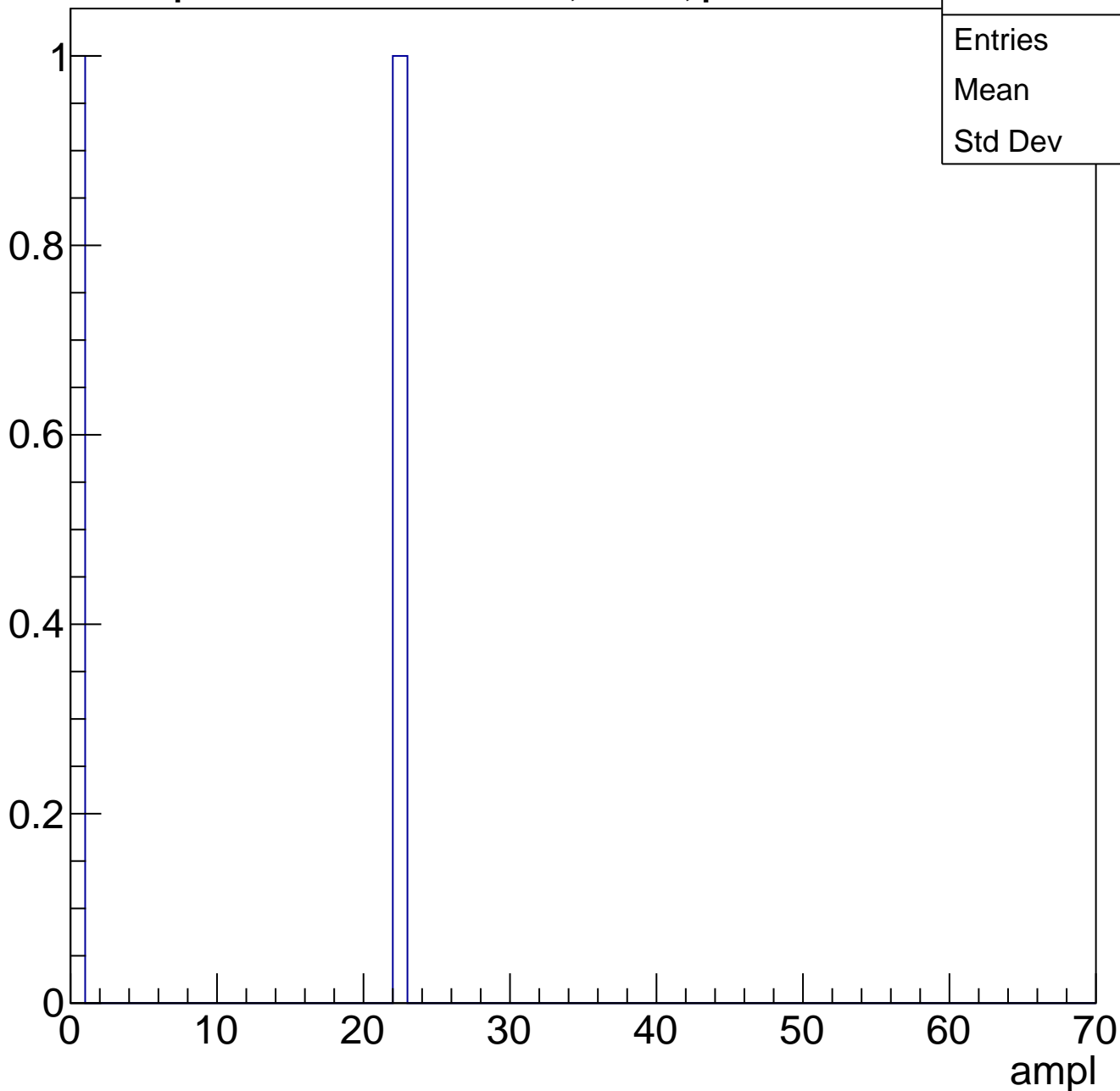




# B1L003S, U3-ch53, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	11
Std Dev	11

# B1L003S, U3-ch54, adc0

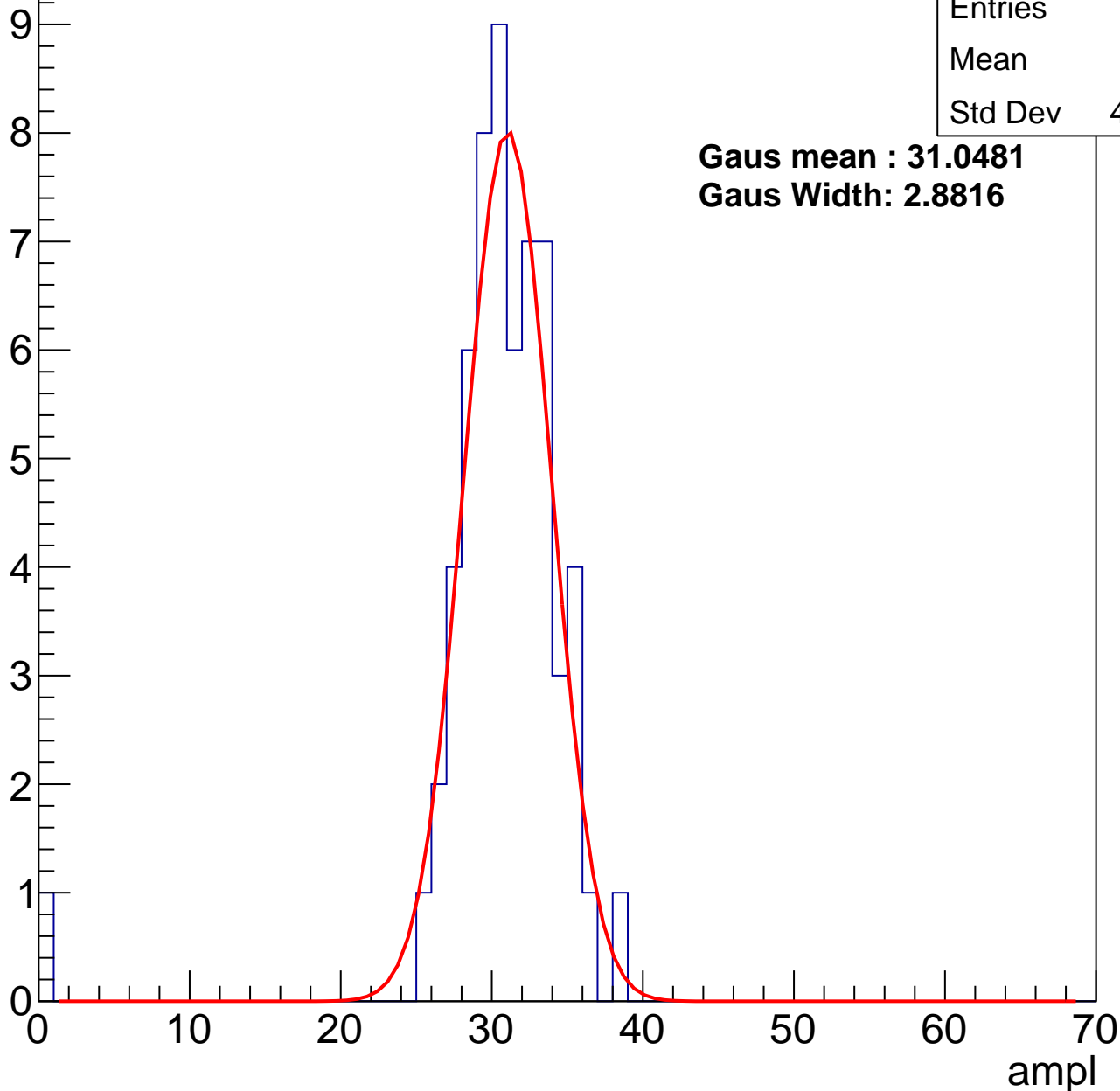
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	30.2
Std Dev	4.774

**Gaus mean : 31.0481**

**Gaus Width: 2.8816**



# B1L003S, U3-ch54, adc1

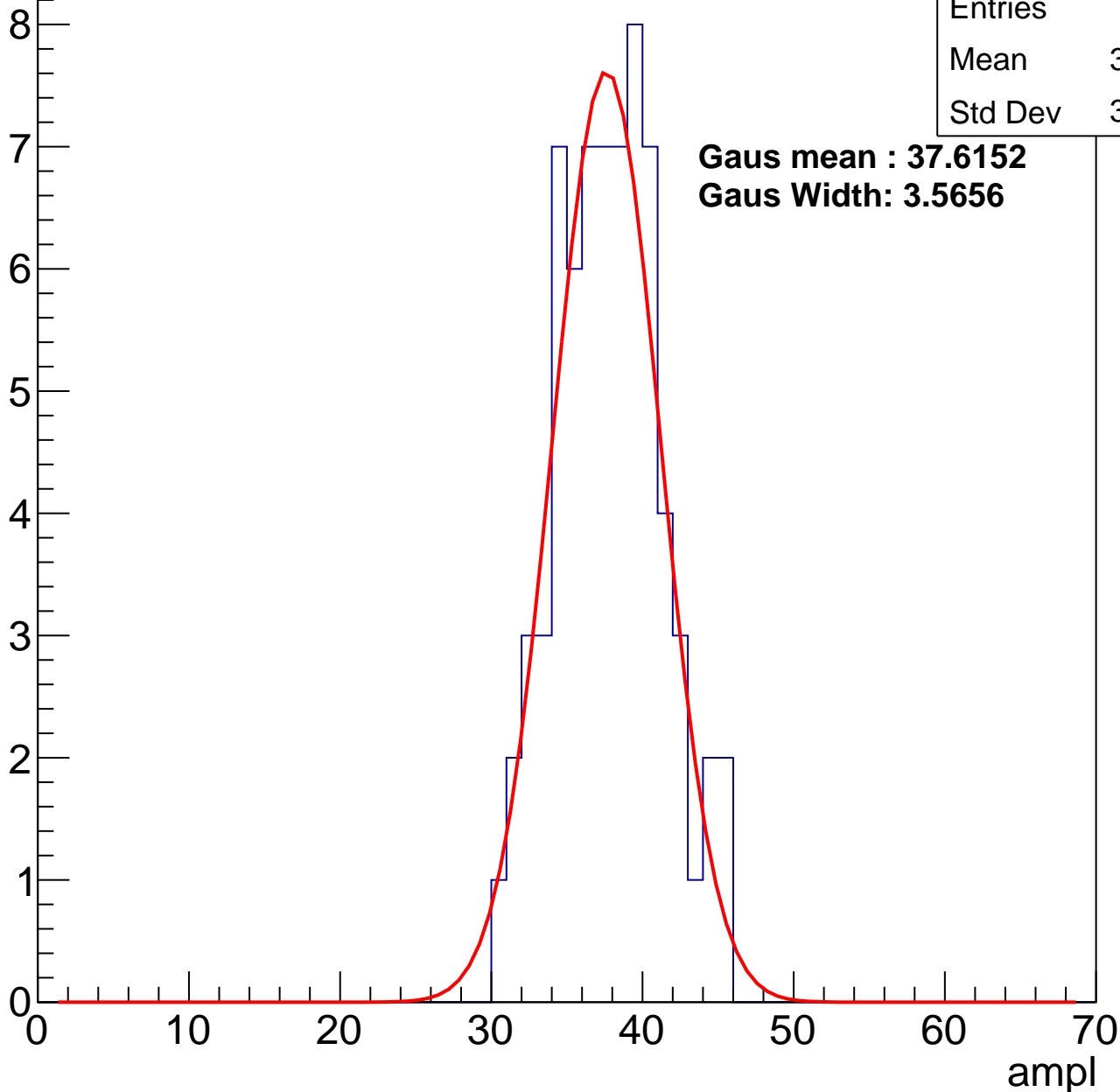
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	37.36
Std Dev	3.448

**Gaus mean : 37.6152**

**Gaus Width: 3.5656**



# B1L003S, U3-ch54, adc2

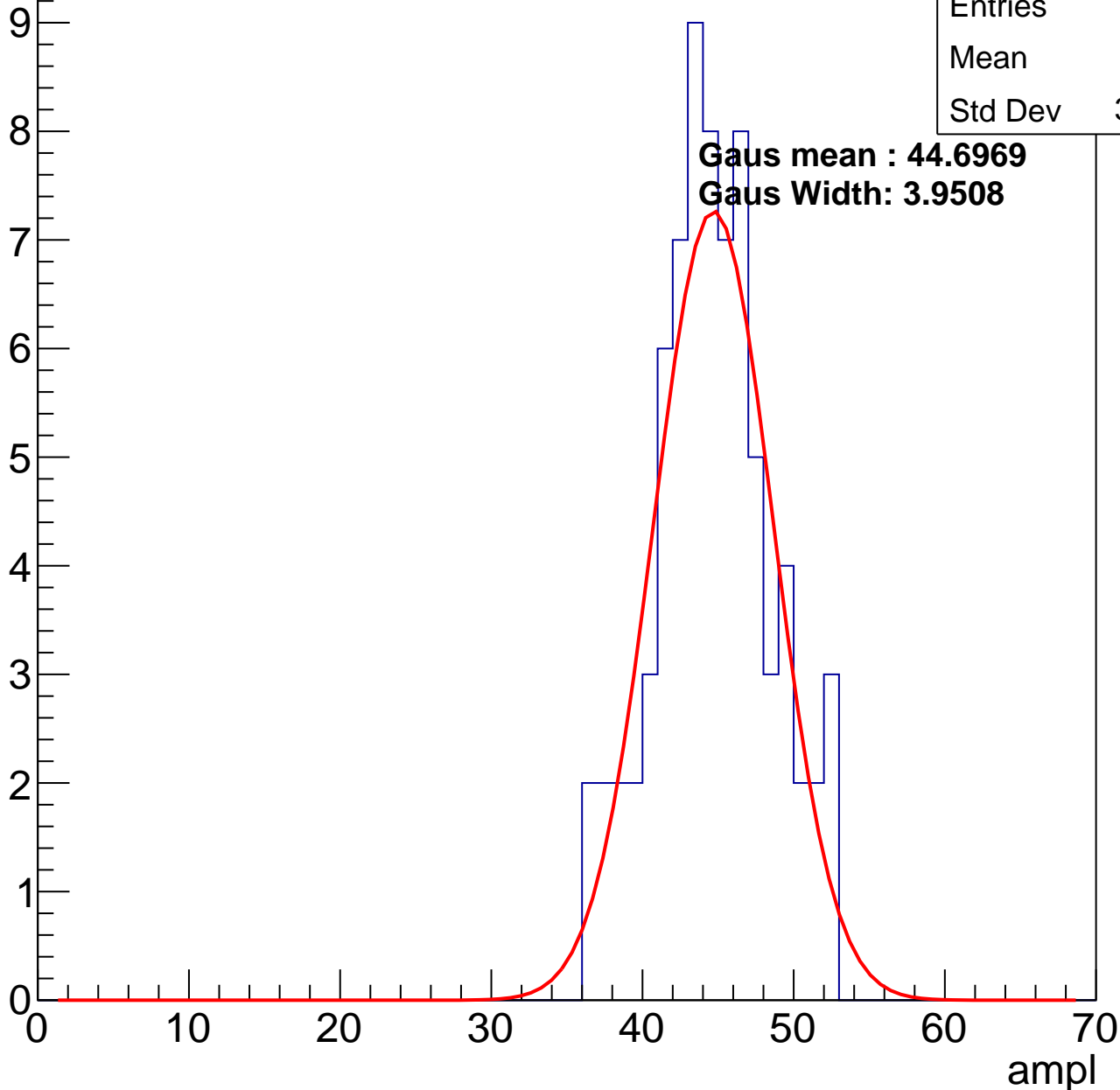
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	75
Mean	44.2
Std Dev	3.791

**Gaus mean : 44.6969**

**Gaus Width: 3.9508**

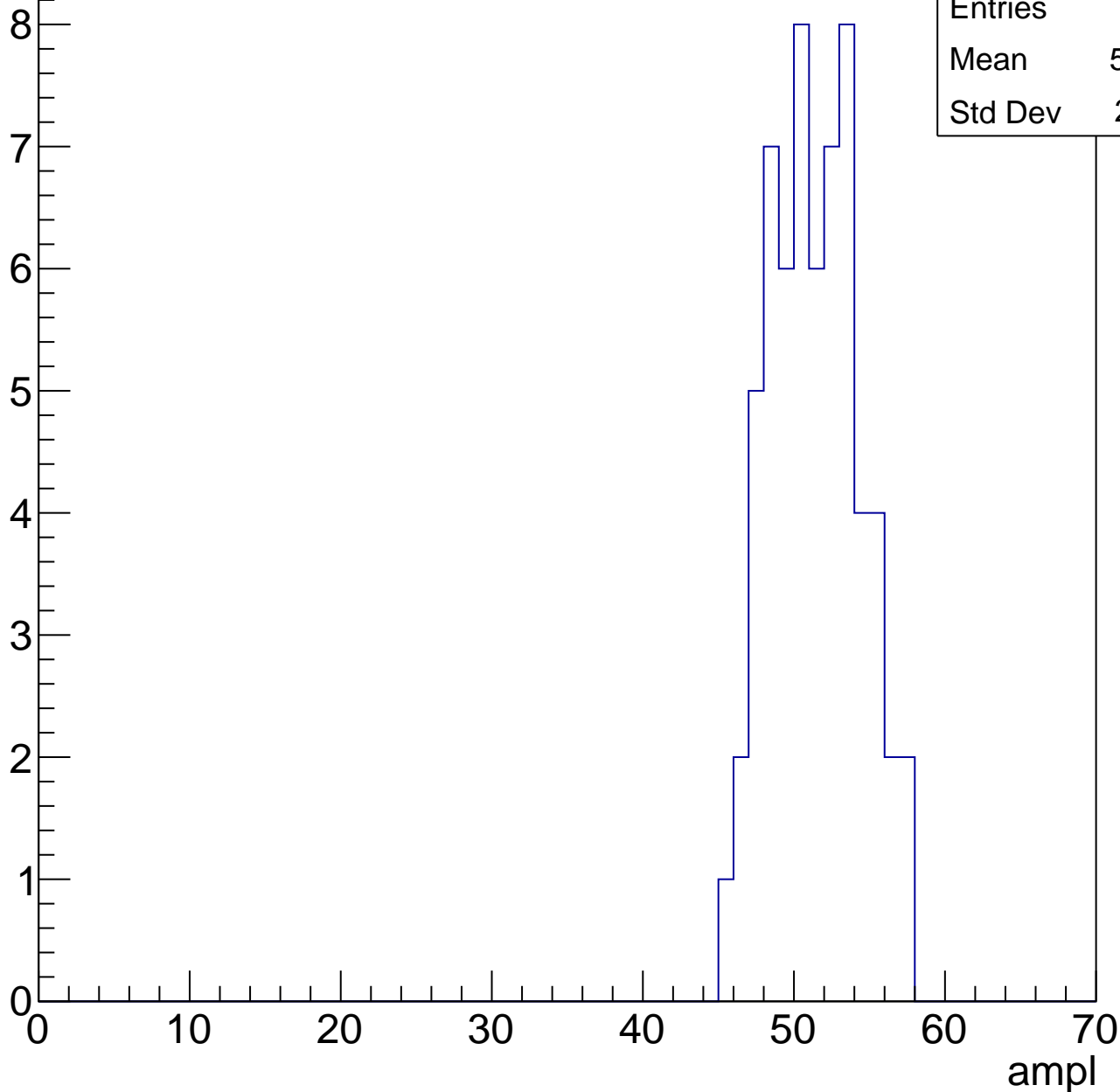


# B1L003S, U3-ch54, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

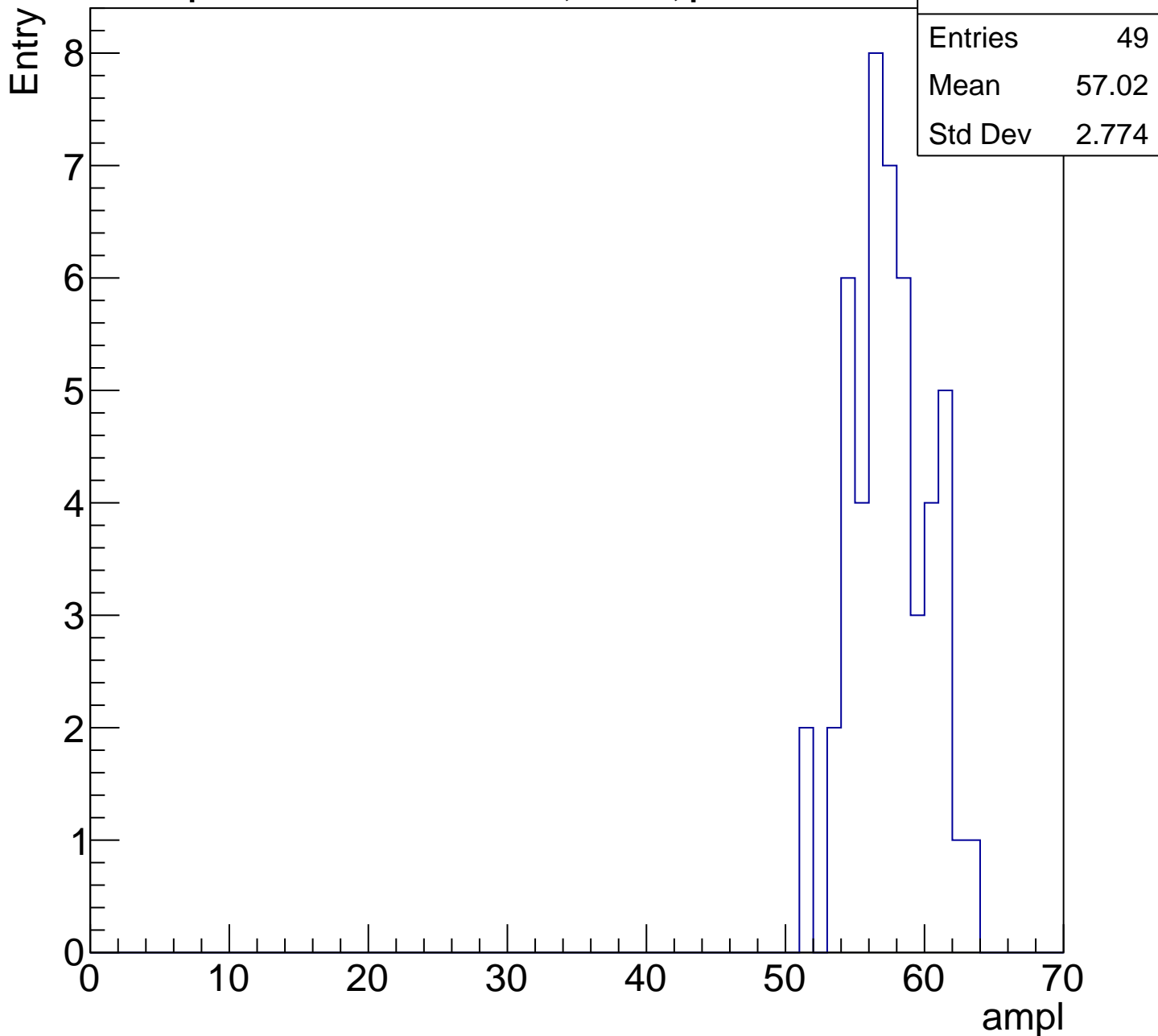
Entry

Entries	62
Mean	50.94
Std Dev	2.901



# B1L003S, U3-ch54, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

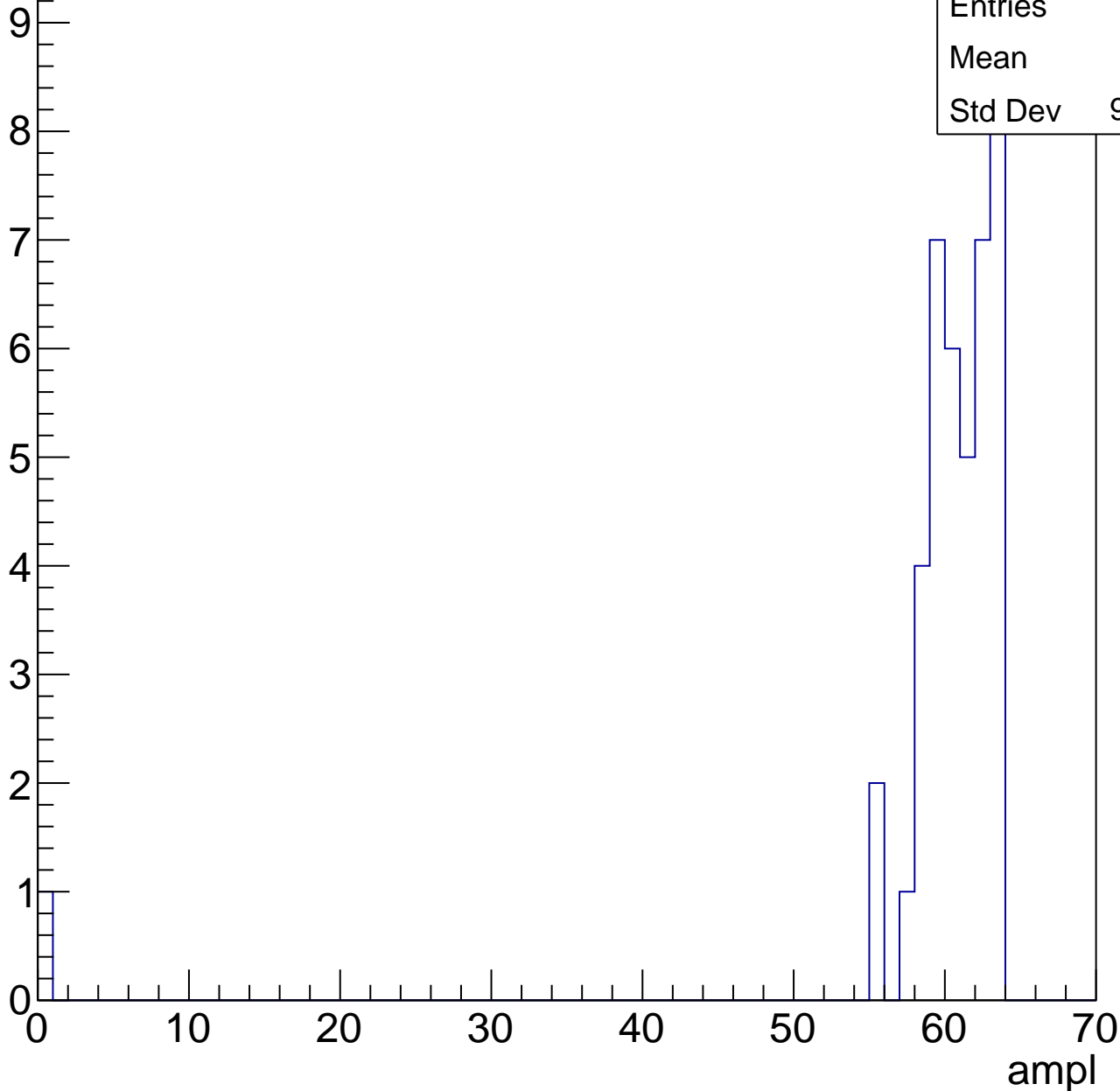


# B1L003S, U3-ch54, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	42
Mean	59
Std Dev	9.454



# B1L003S, U3-ch54, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

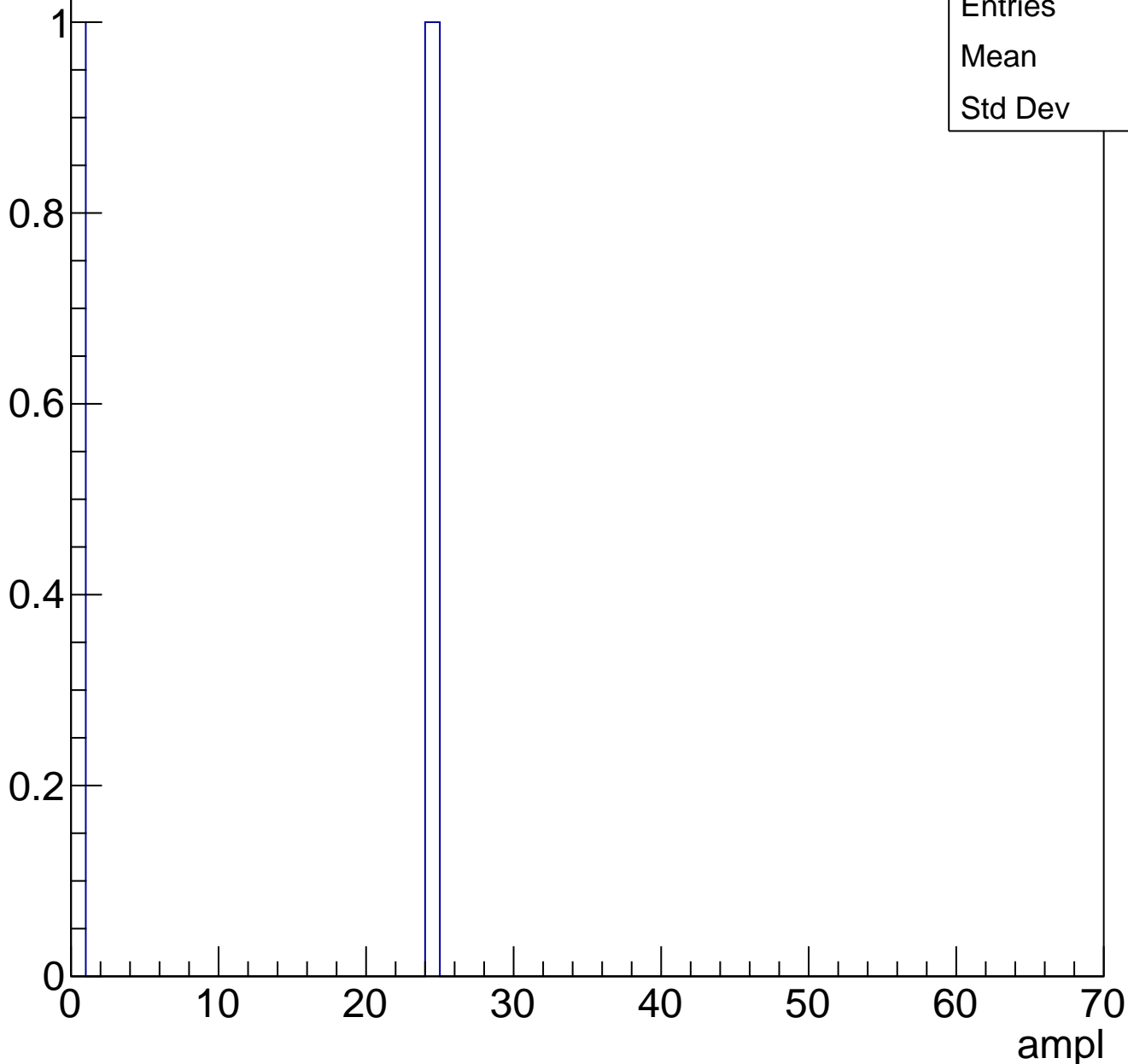




# B1L003S, U3-ch54, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U3-ch55, adc0

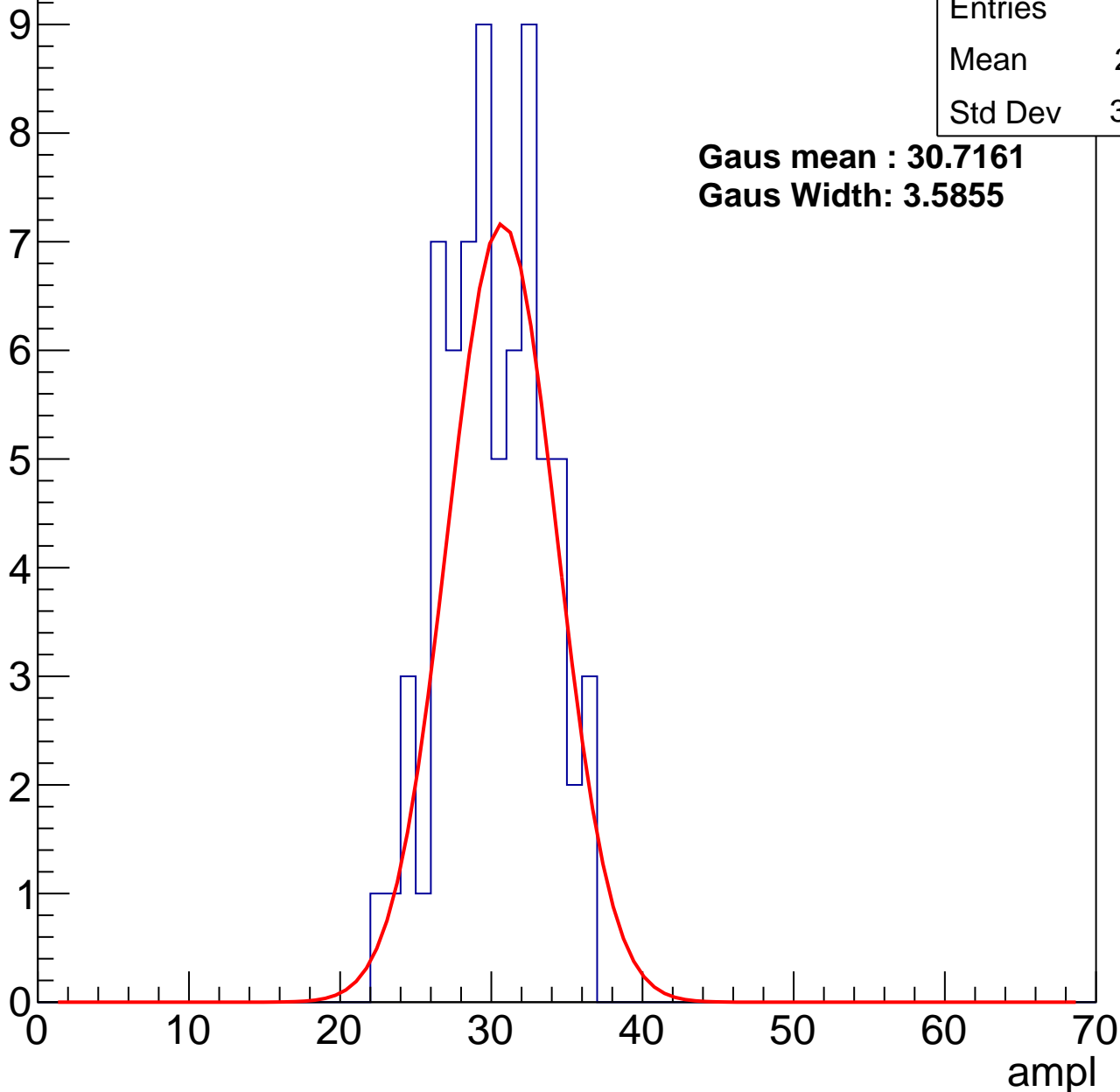
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	29.71
Std Dev	3.313

**Gaus mean : 30.7161**

**Gaus Width: 3.5855**



# B1L003S, U3-ch55, adc1

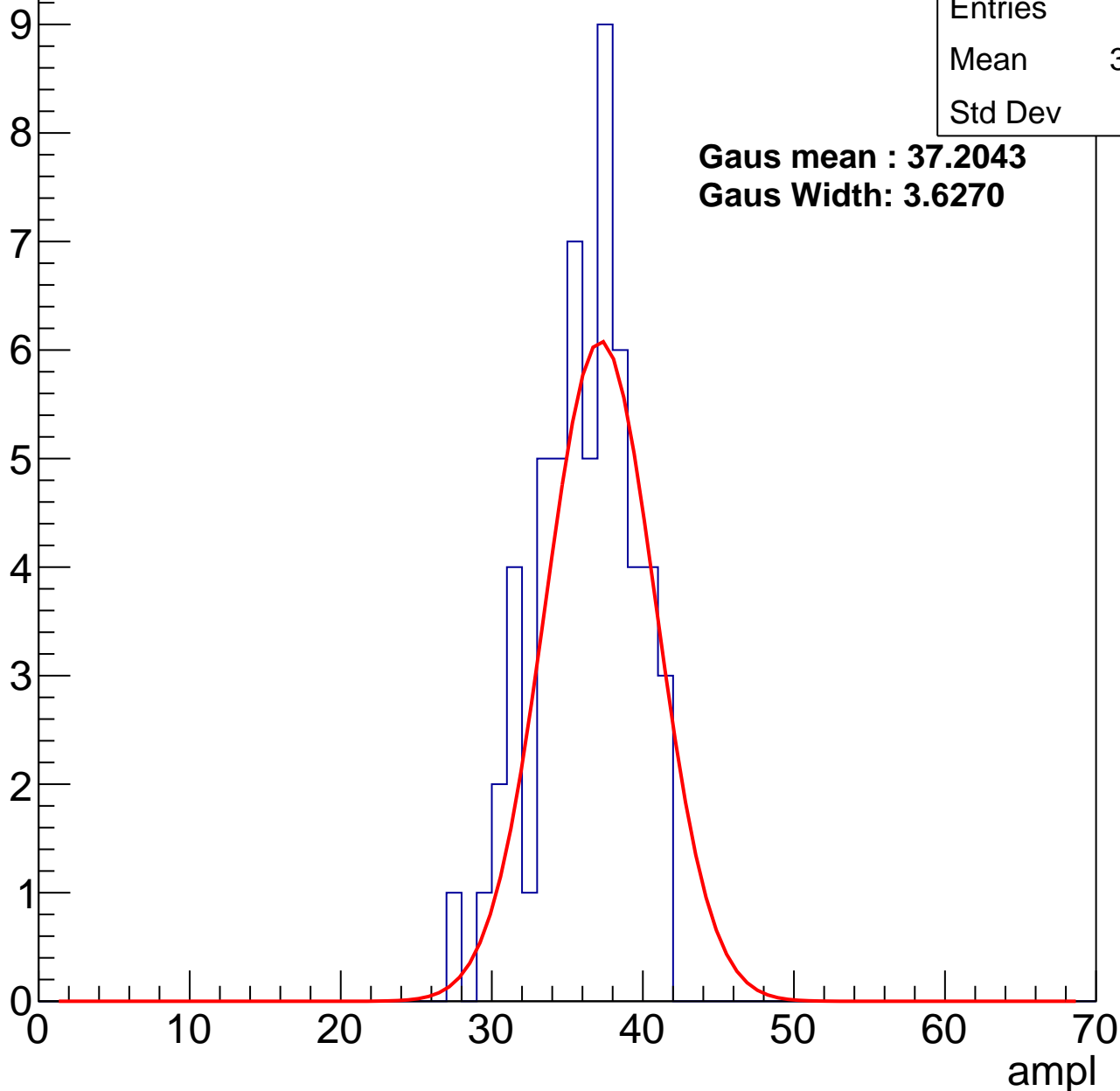
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	35.65
Std Dev	3.22

**Gaus mean : 37.2043**

**Gaus Width: 3.6270**



# B1L003S, U3-ch55, adc2

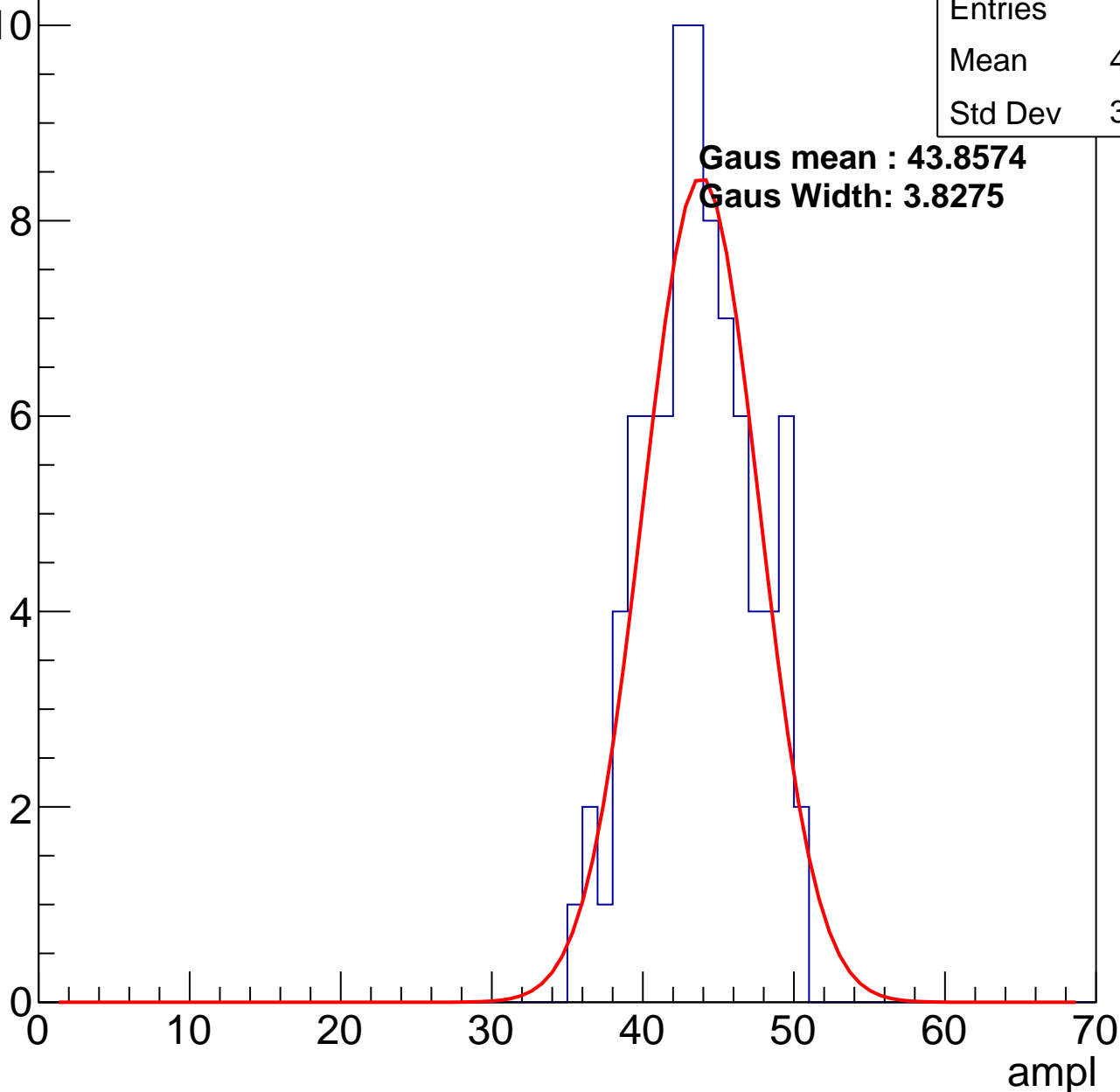
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	83
Mean	43.17
Std Dev	3.553

**Gaus mean : 43.8574**

**Gaus Width: 3.8275**

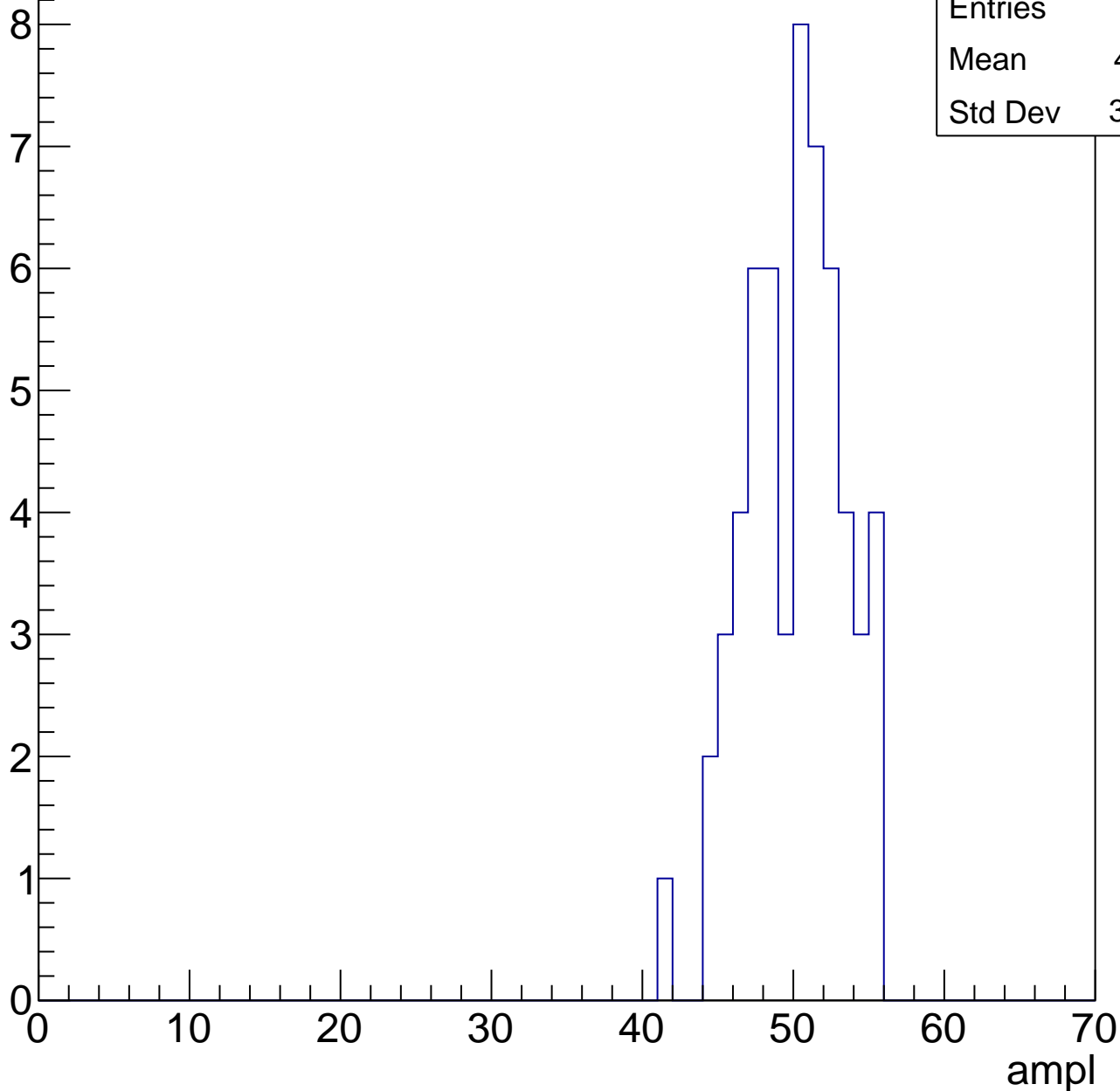


# B1L003S, U3-ch55, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	49.61
Std Dev	3.189

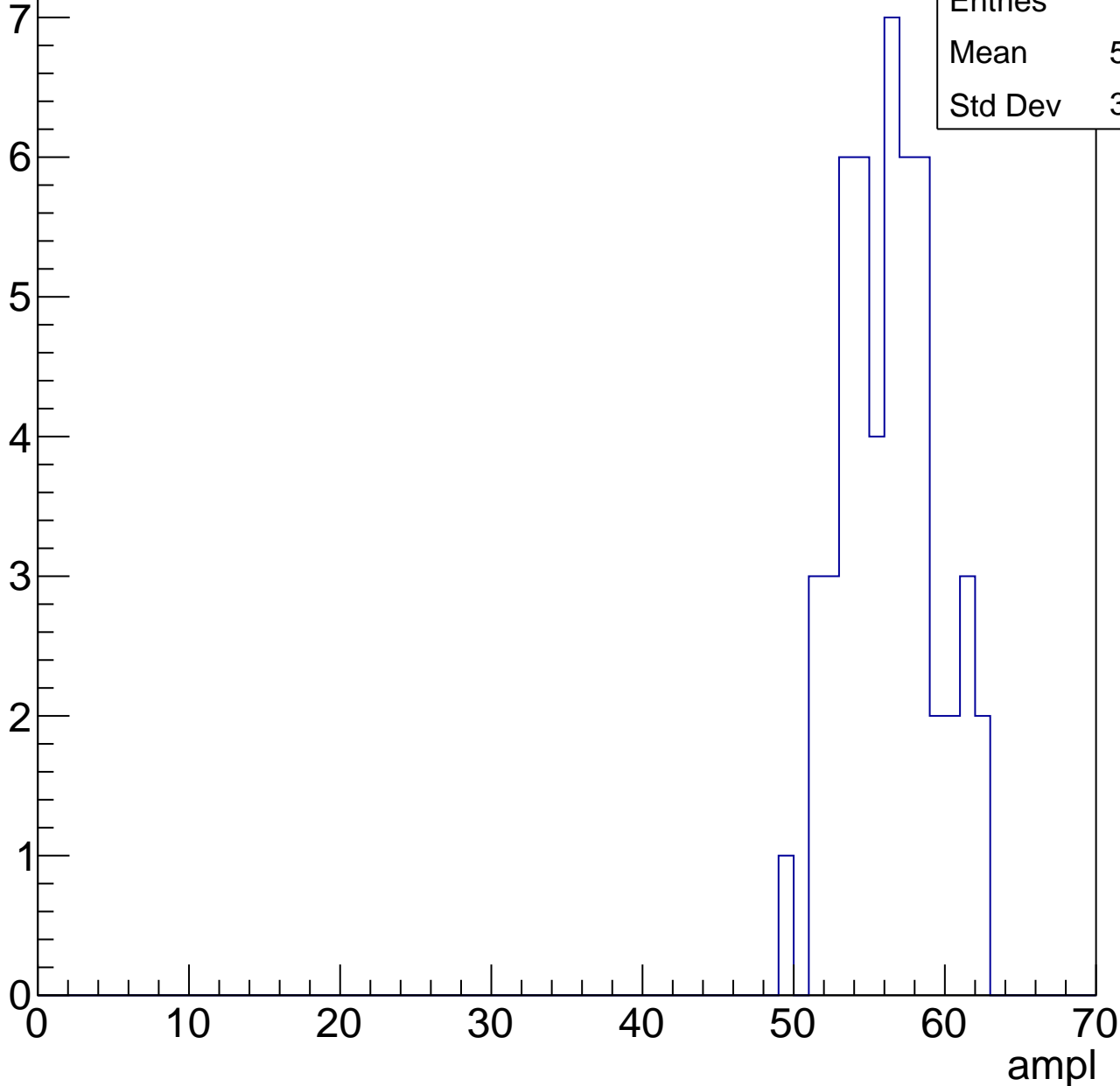


# B1L003S, U3-ch55, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

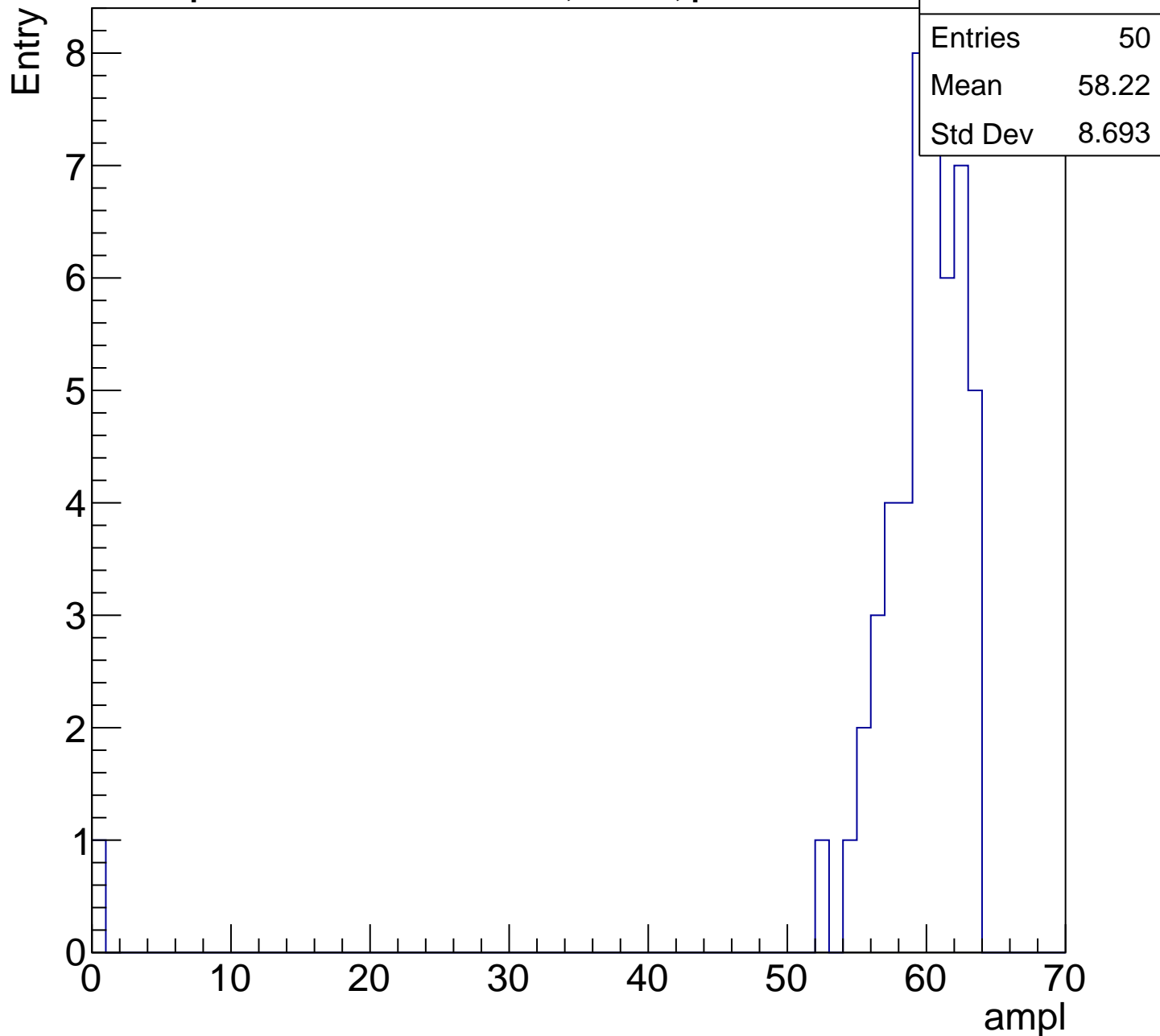
Entry

Entries	51
Mean	55.82
Std Dev	3.066



# B1L003S, U3-ch55, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

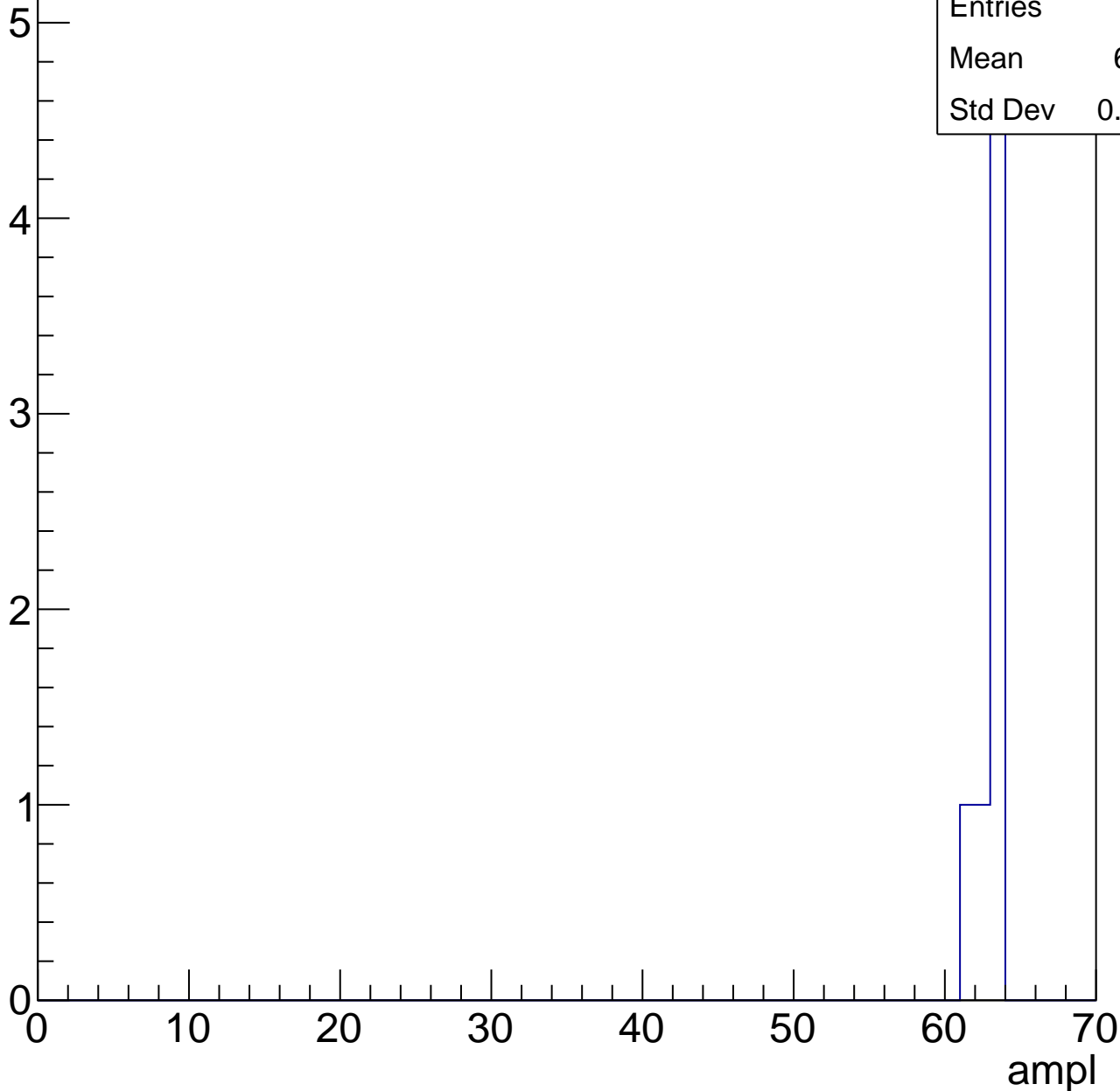


# B1L003S, U3-ch55, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	7
Mean	62.57
Std Dev	0.7284





# B1L003S, U3-ch55, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U3-ch56, adc0

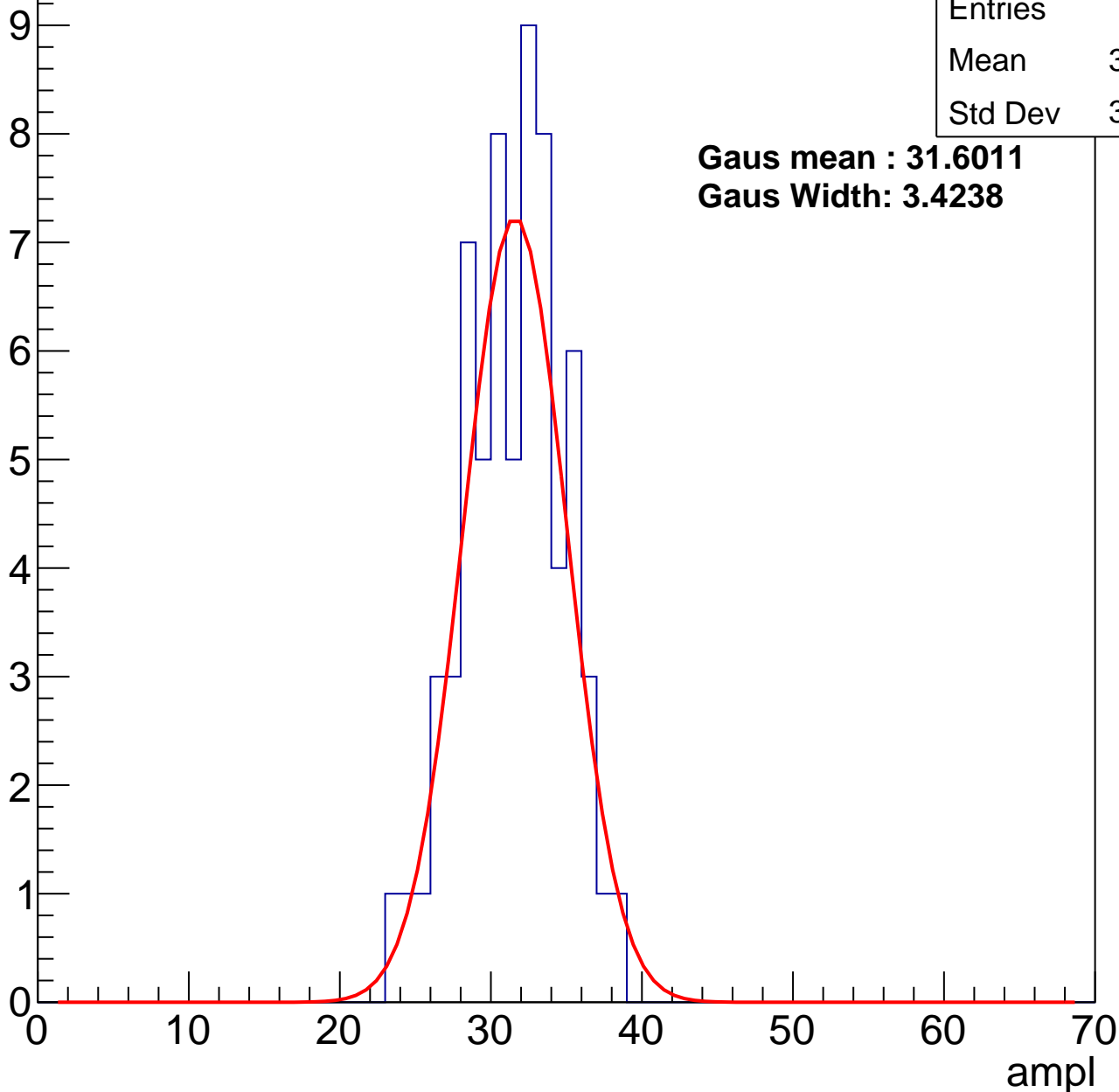
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	31.03
Std Dev	3.247

**Gaus mean : 31.6011**

**Gaus Width: 3.4238**



# B1L003S, U3-ch56, adc1

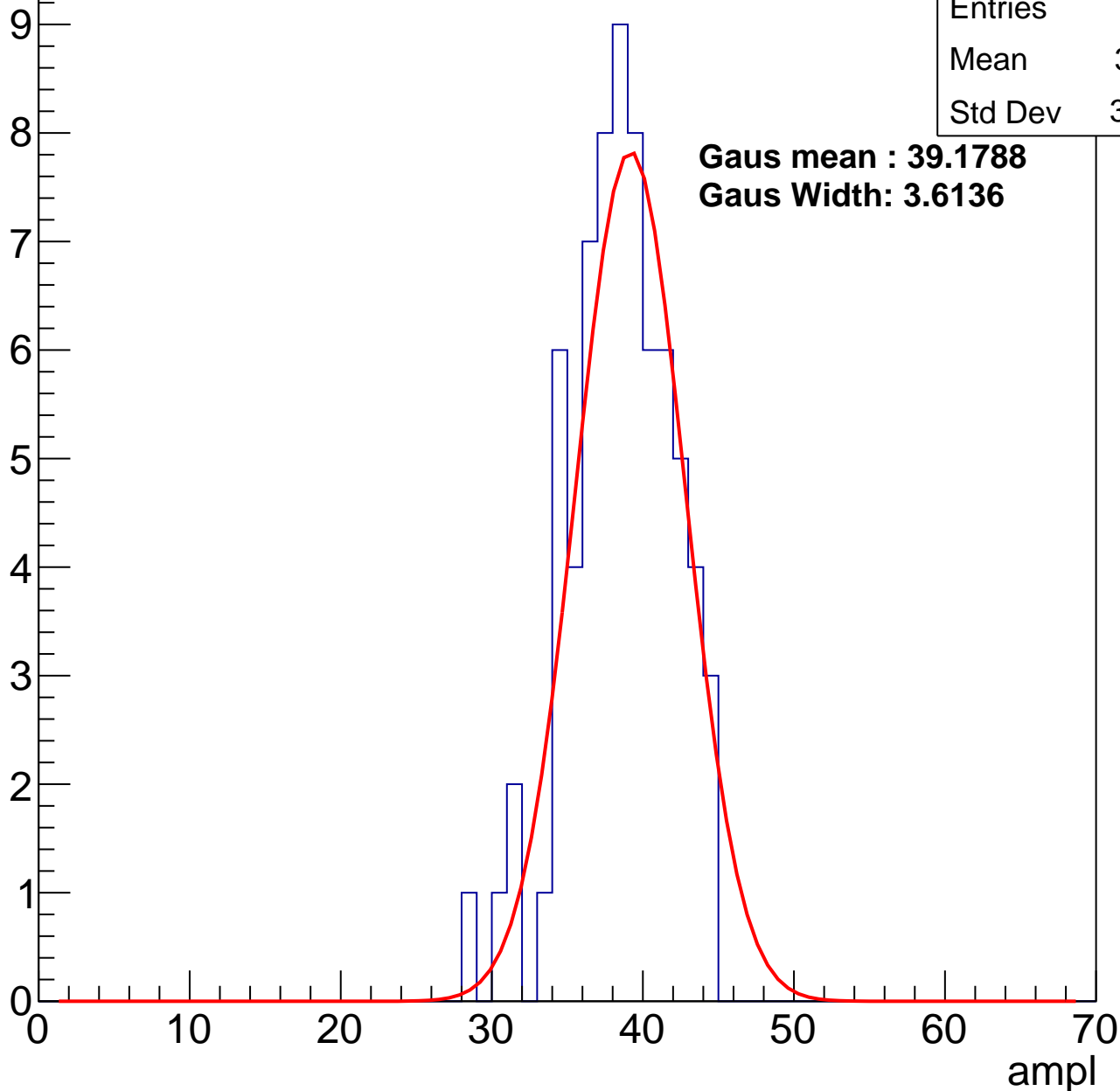
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	71
Mean	38.01
Std Dev	3.417

**Gaus mean : 39.1788**

**Gaus Width: 3.6136**



# B1L003S, U3-ch56, adc2

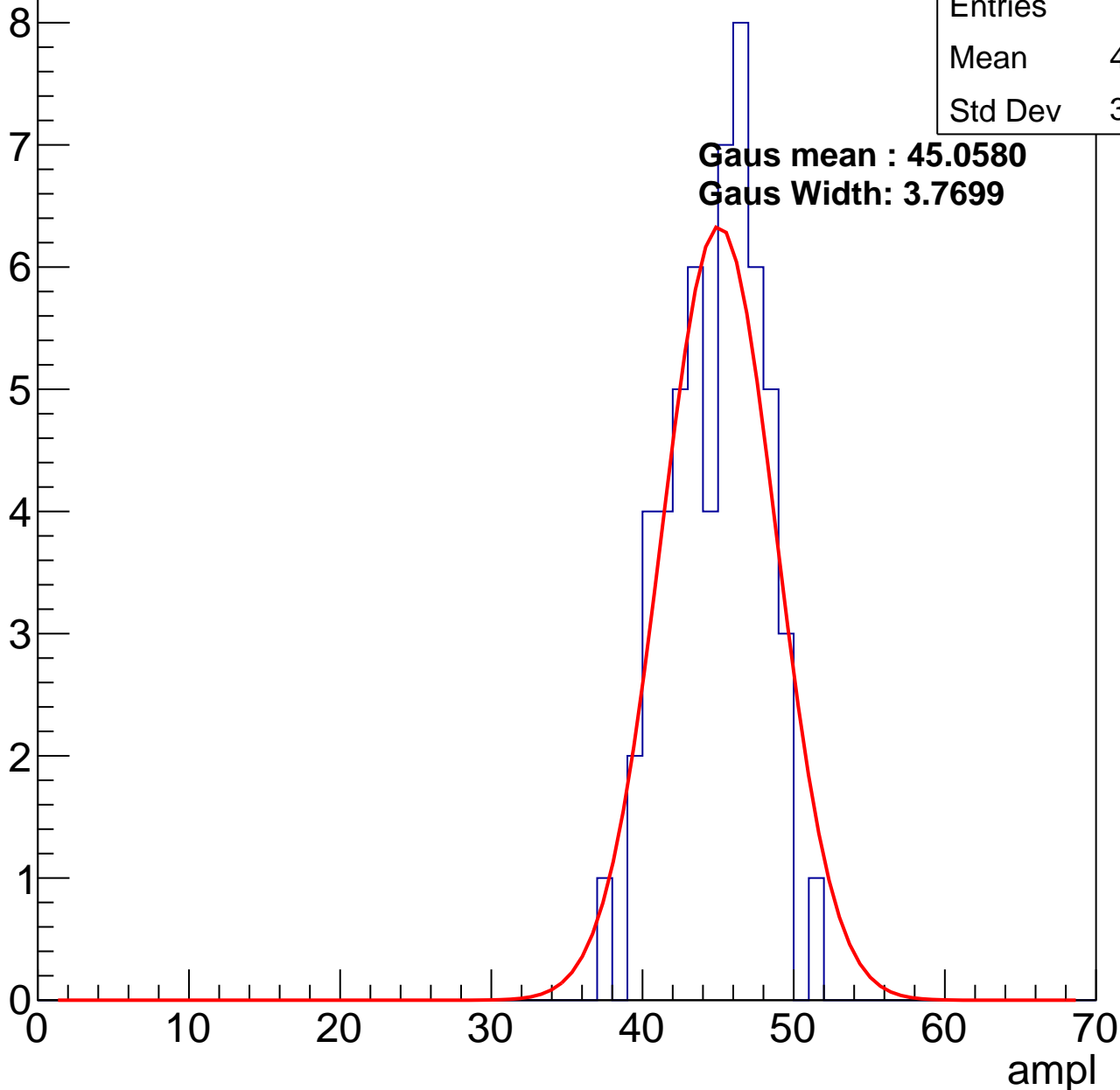
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	44.39
Std Dev	3.028

**Gaus mean : 45.0580**

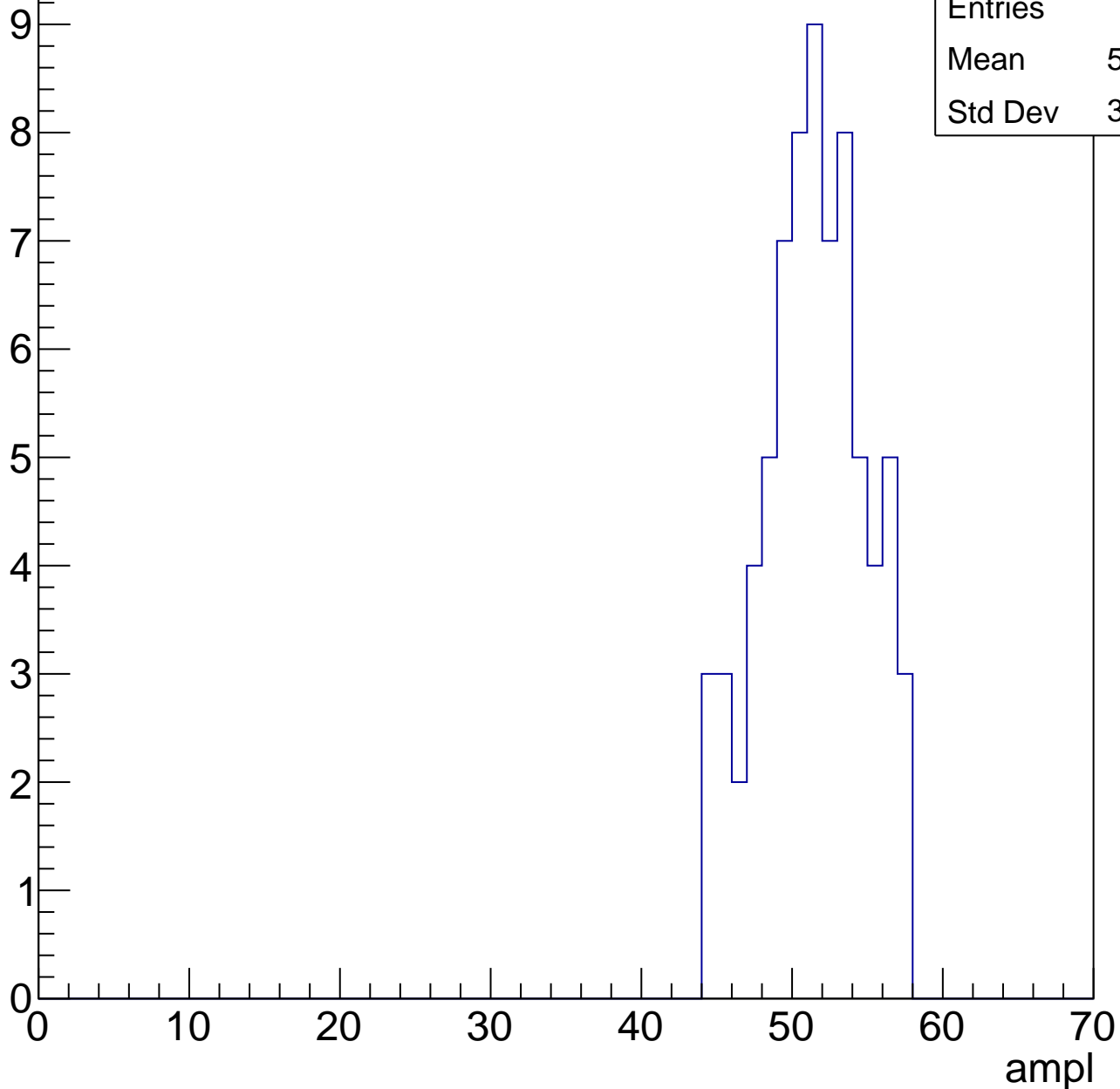
**Gaus Width: 3.7699**



# B1L003S, U3-ch56, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

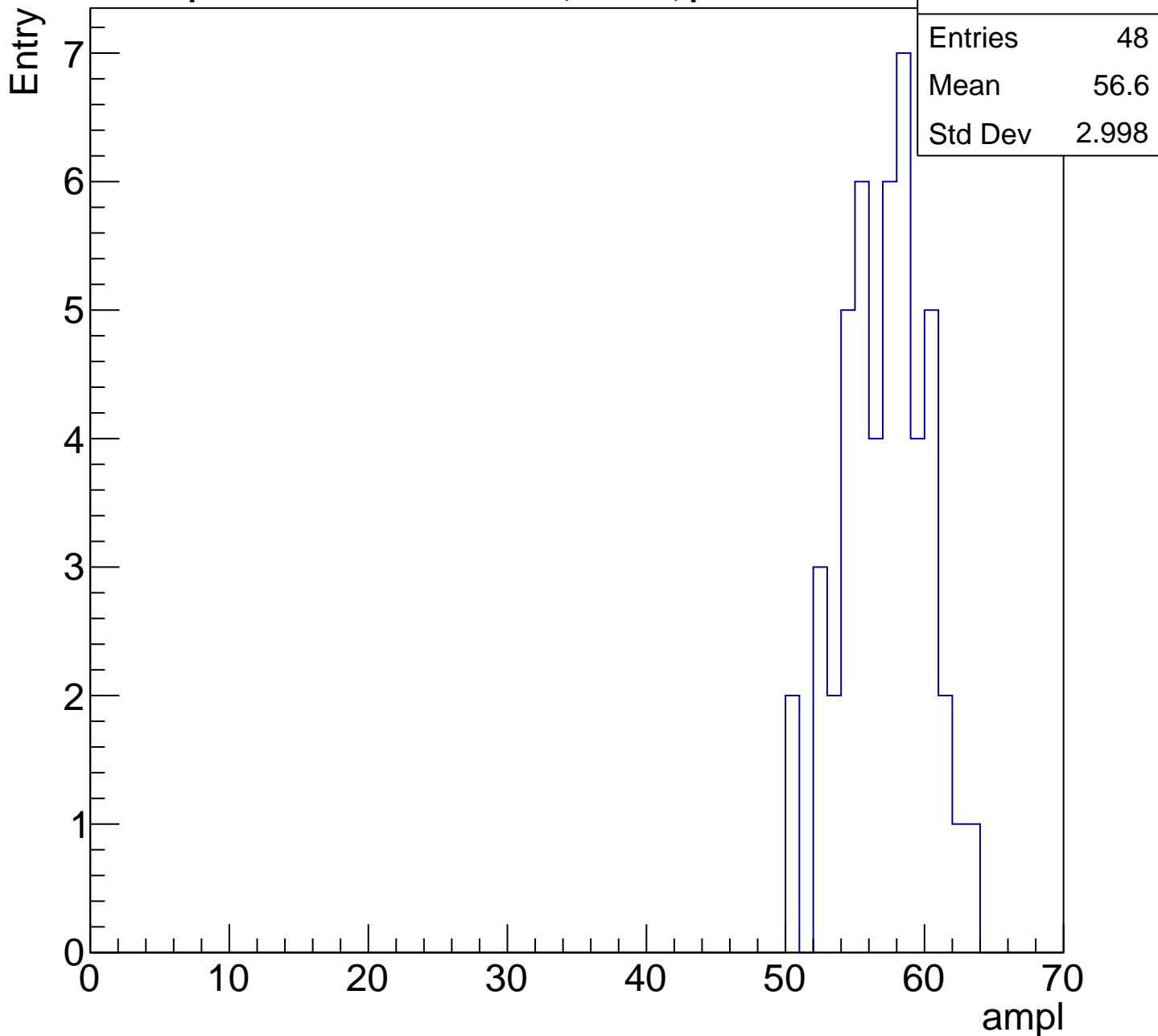
Entry



Entries	73
Mean	50.93
Std Dev	3.373

# B1L003S, U3-ch56, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

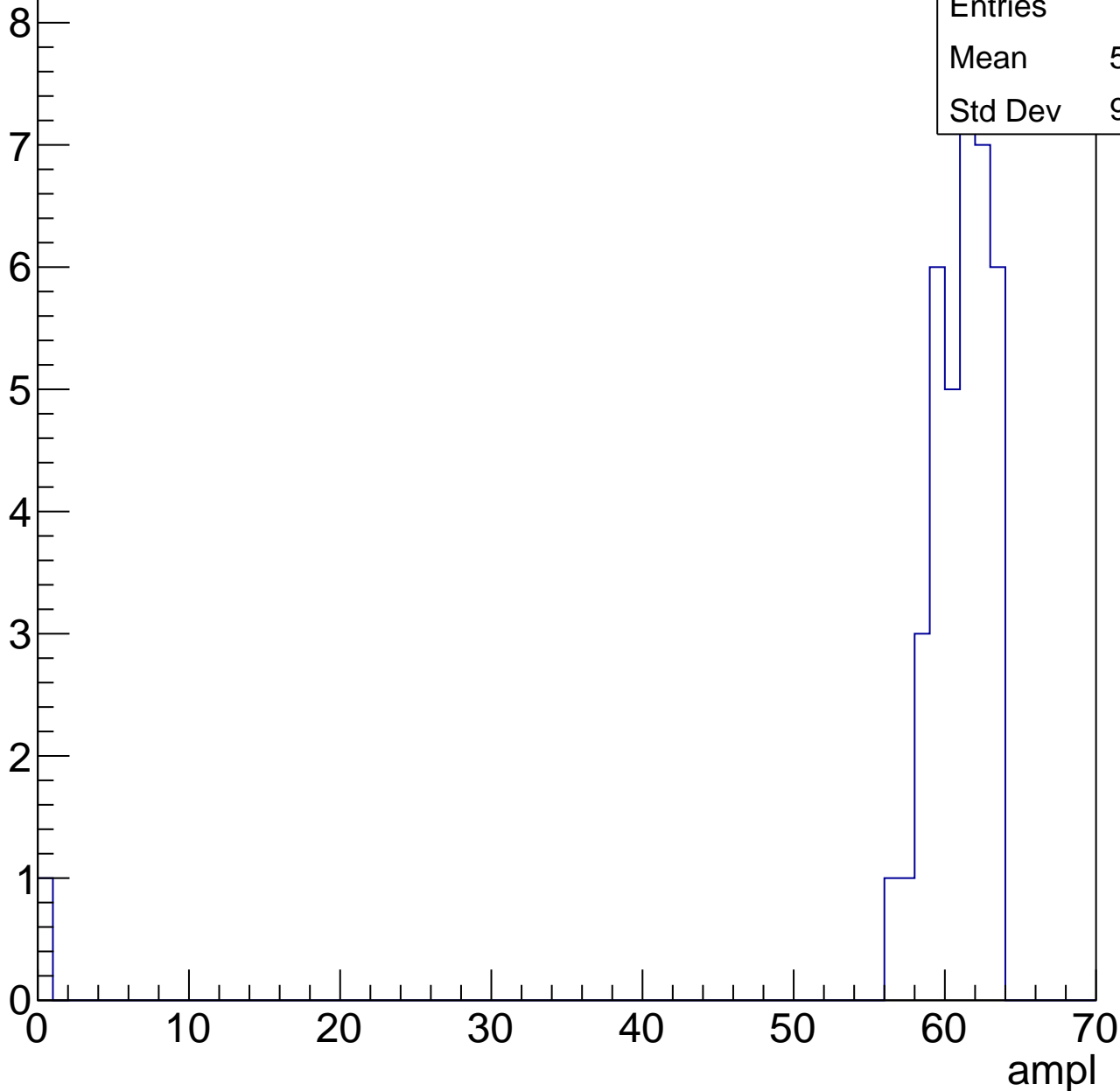


# B1L003S, U3-ch56, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	38
Mean	58.97
Std Dev	9.858



# B1L003S, U3-ch56, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

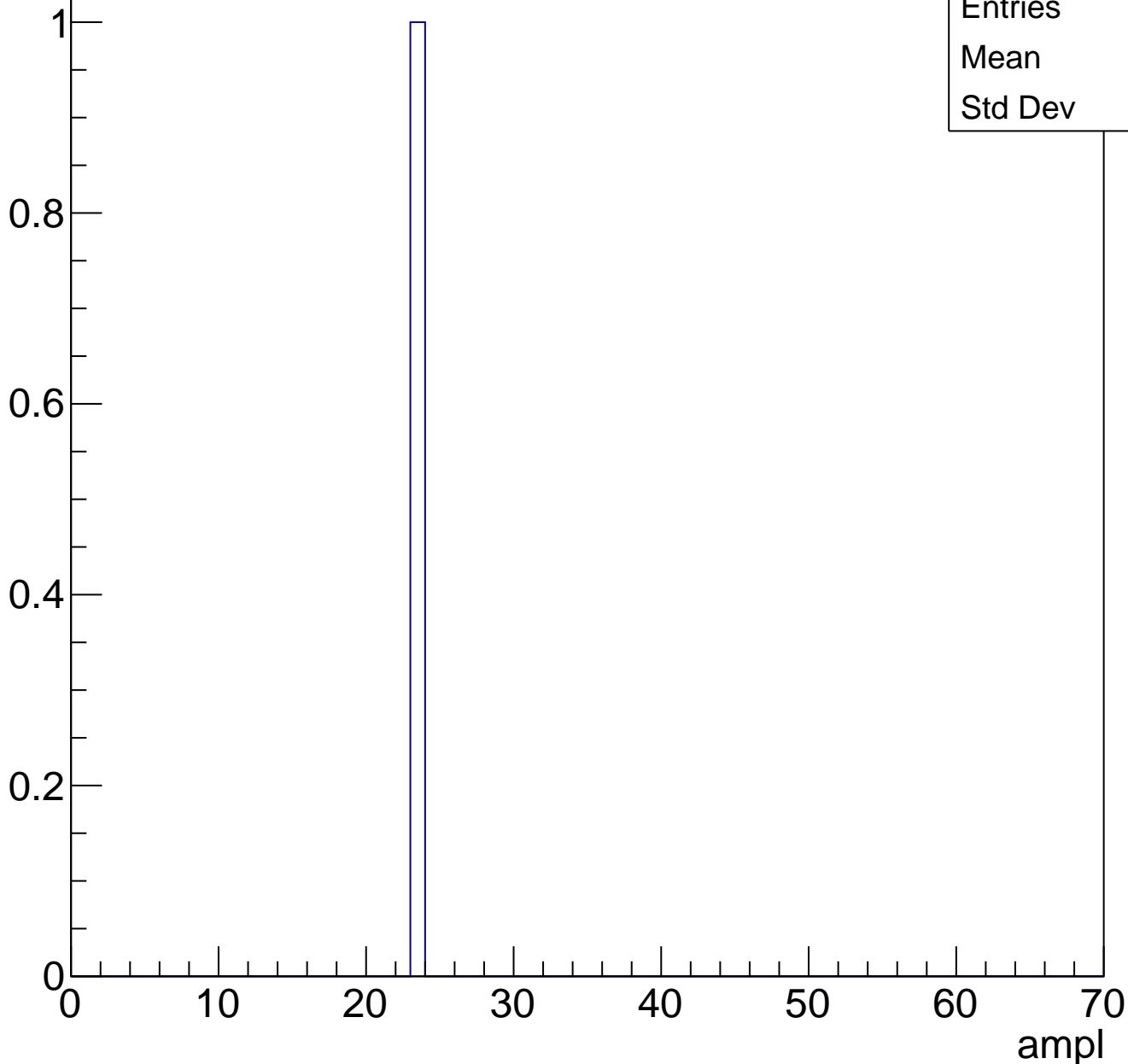




# B1L003S, U3-ch56, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U3-ch57, adc0

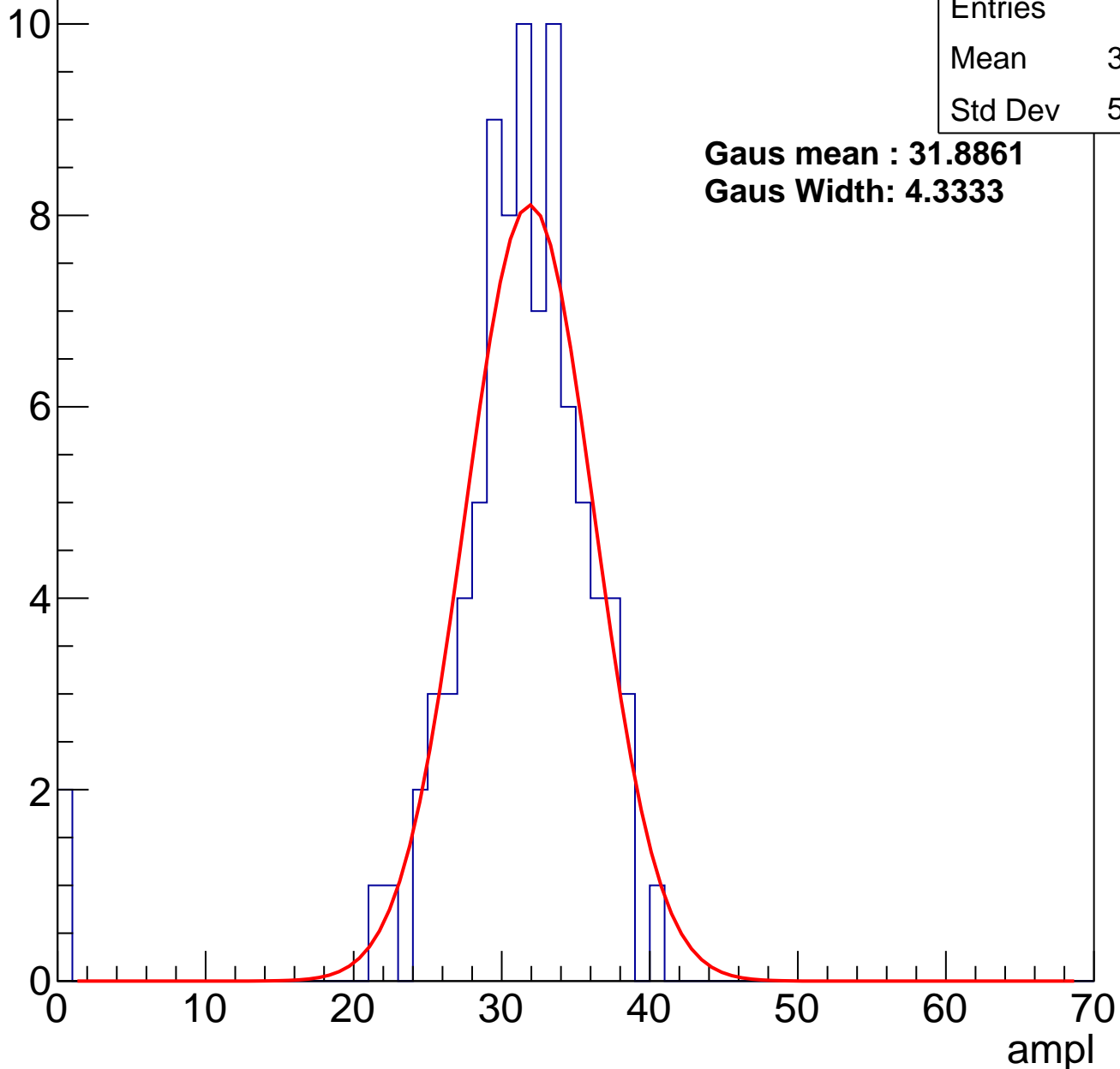
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	88
Mean	30.48
Std Dev	5.998

**Gaus mean : 31.8861**

**Gaus Width: 4.3333**

Entry



# B1L003S, U3-ch57, adc1

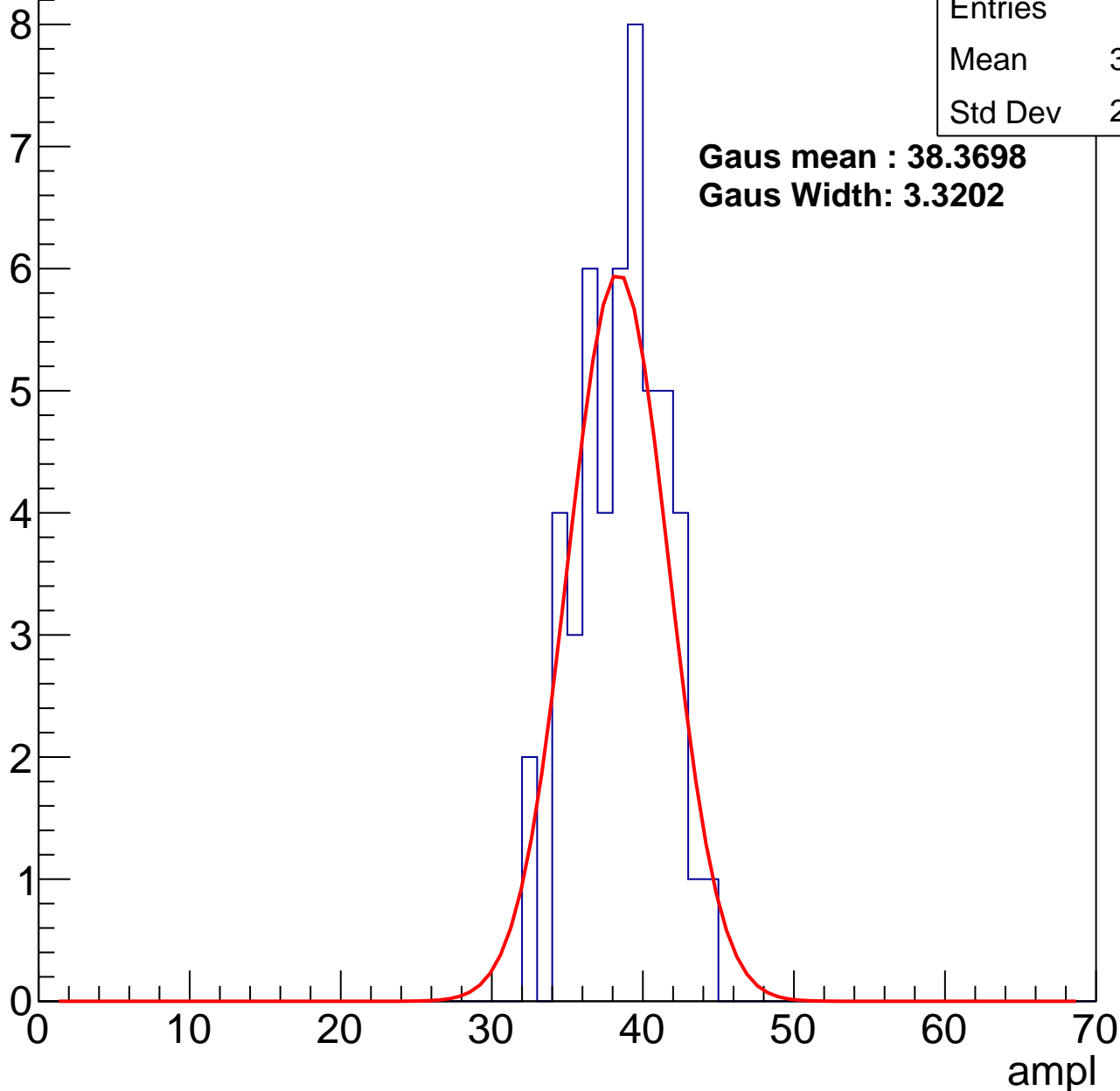
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	49
Mean	38.14
Std Dev	2.814

**Gaus mean : 38.3698**

**Gaus Width: 3.3202**



# B1L003S, U3-ch57, adc2

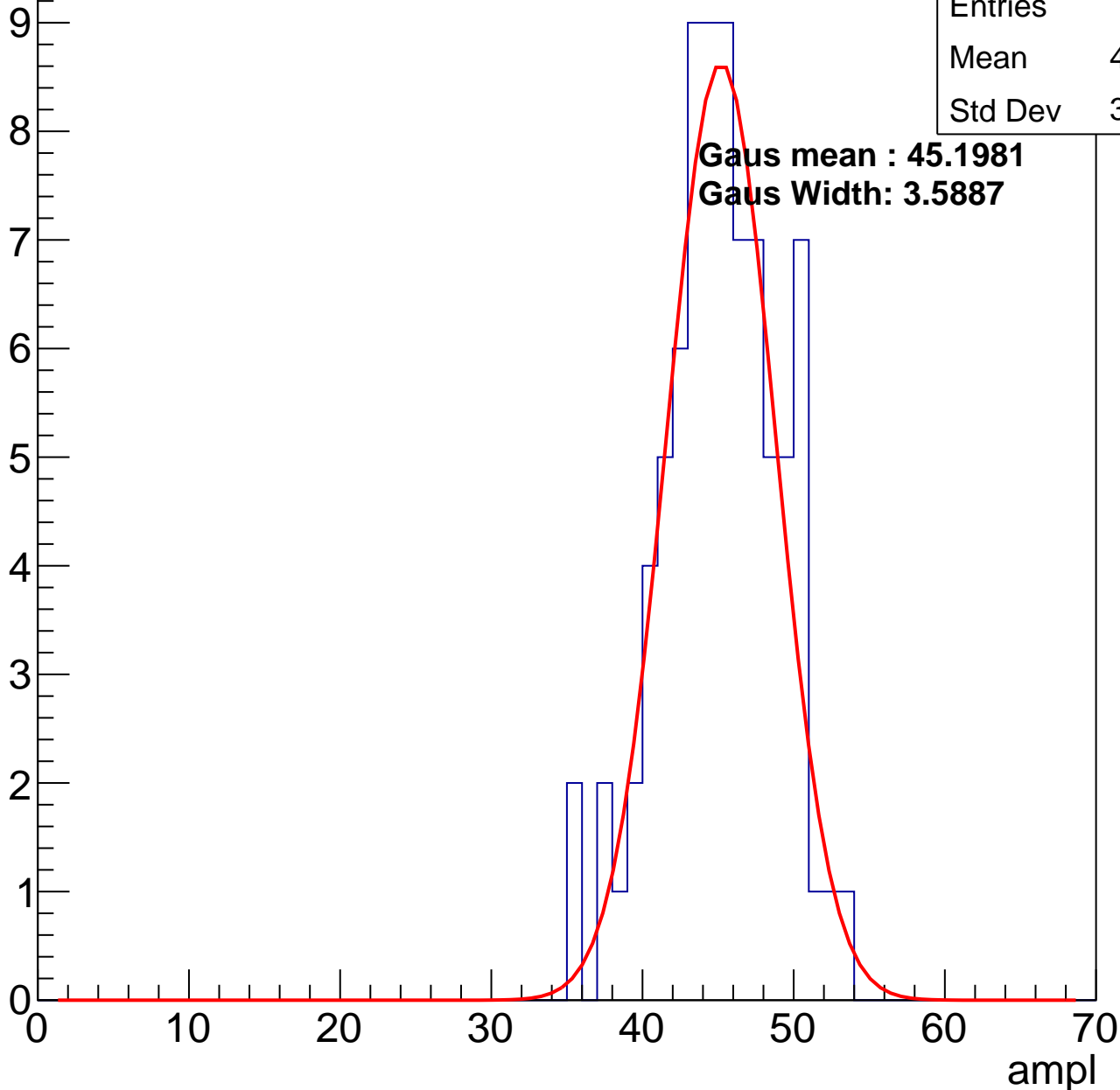
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	83
Mean	44.66
Std Dev	3.806

**Gaus mean : 45.1981**

**Gaus Width: 3.5887**

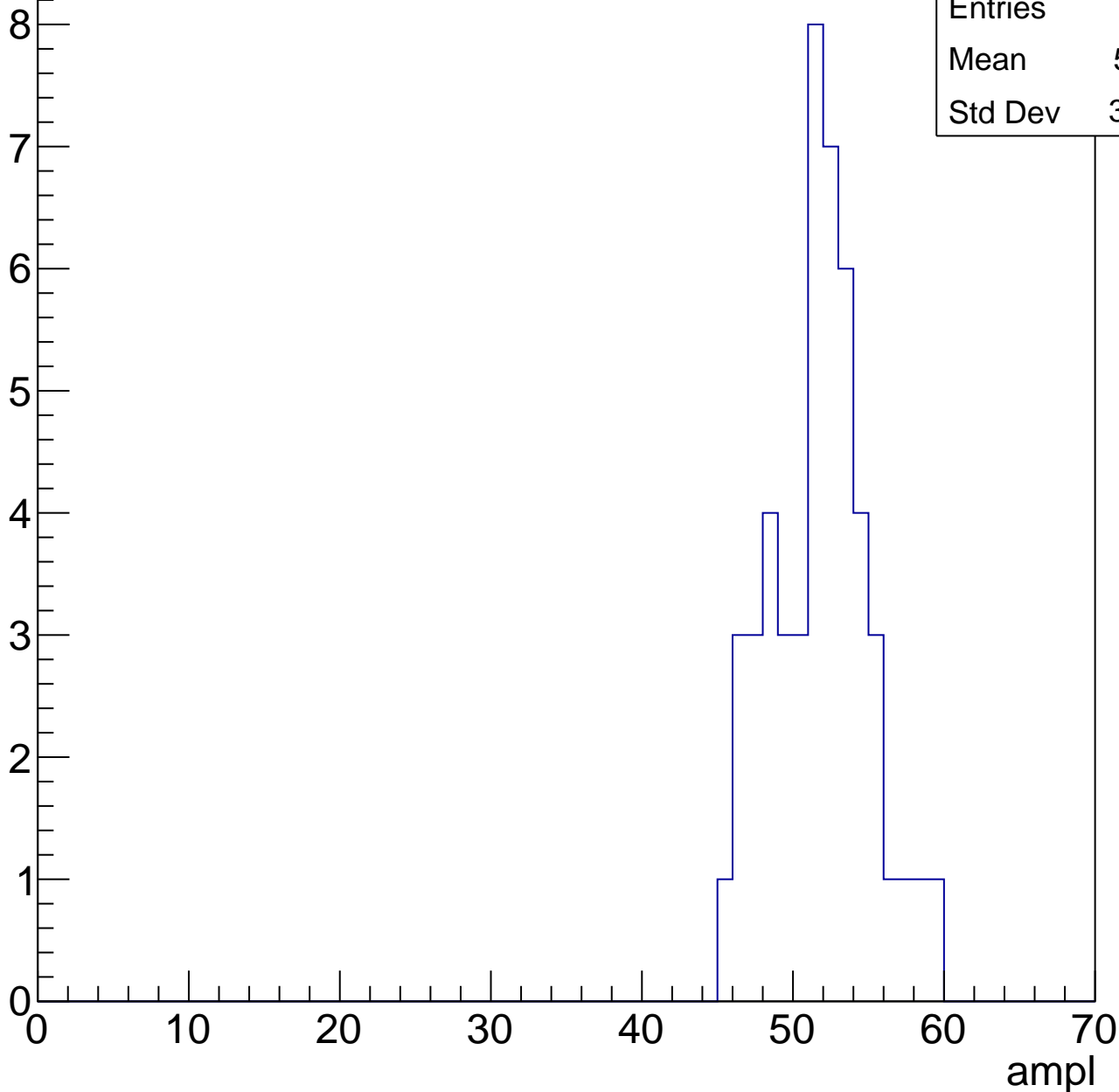


# B1L003S, U3-ch57, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	49
Mean	51.31
Std Dev	3.176

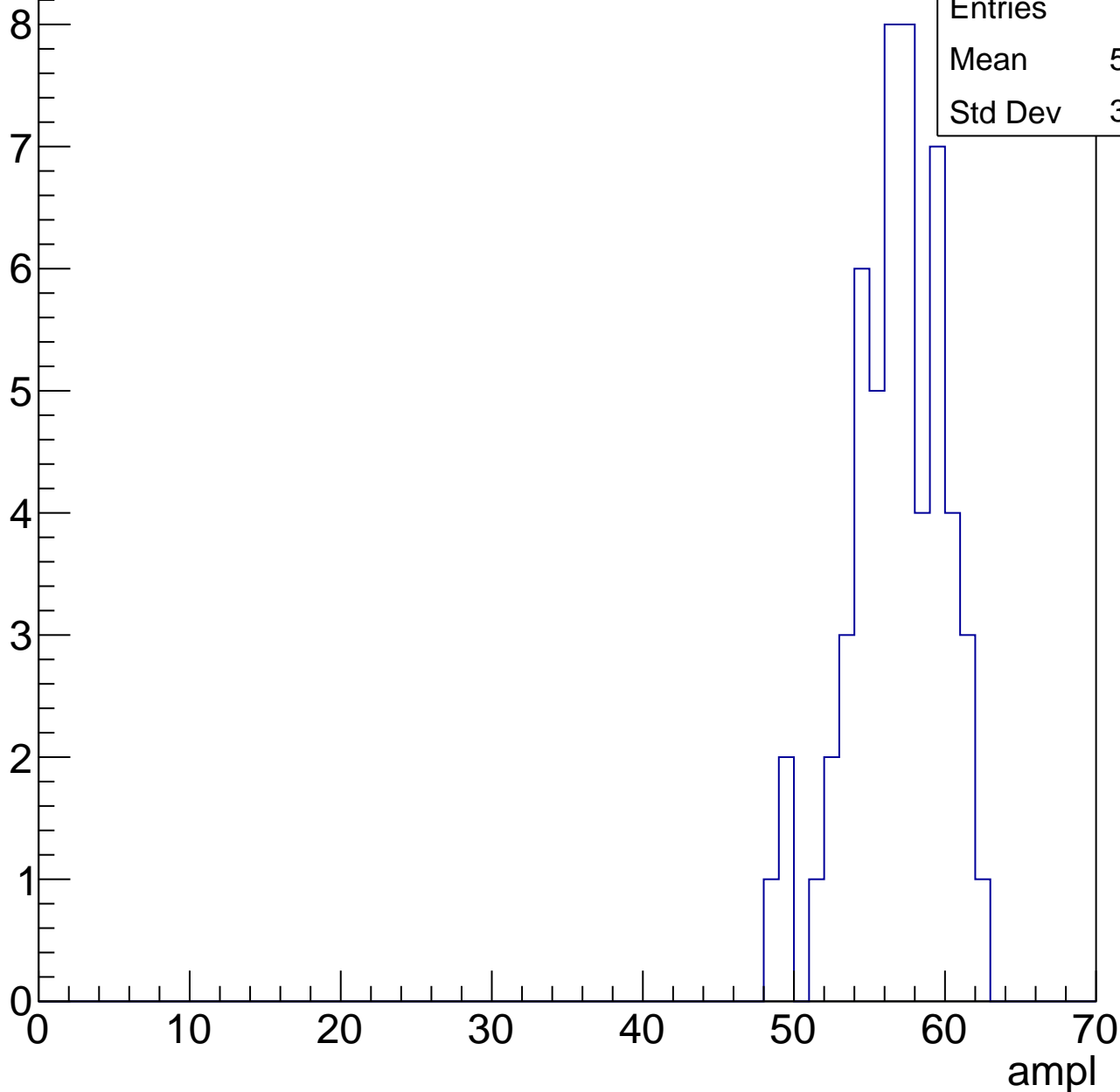


# B1L003S, U3-ch57, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	56.24
Std Dev	3.116

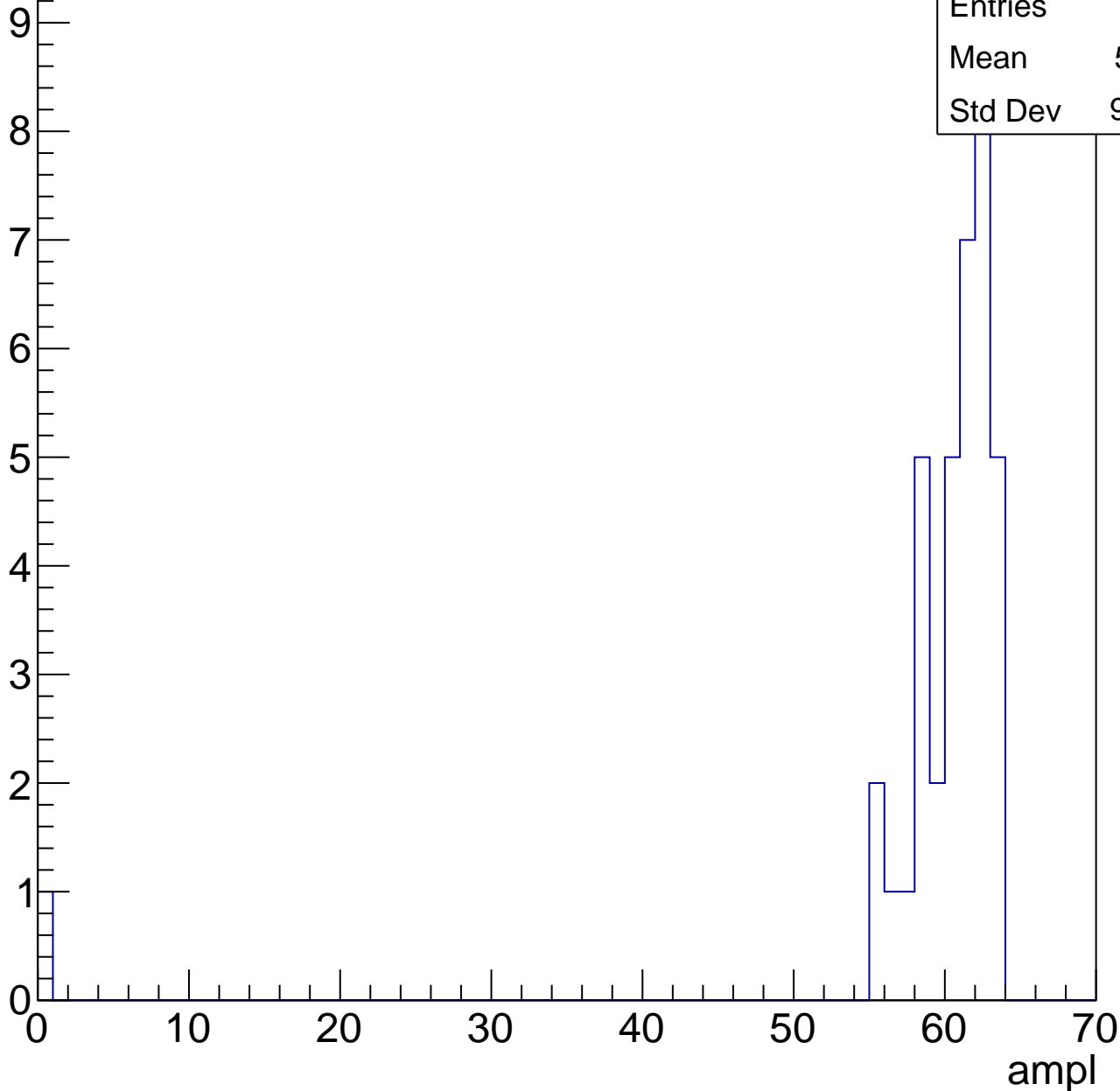


# B1L003S, U3-ch57, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	38
Mean	58.71
Std Dev	9.897

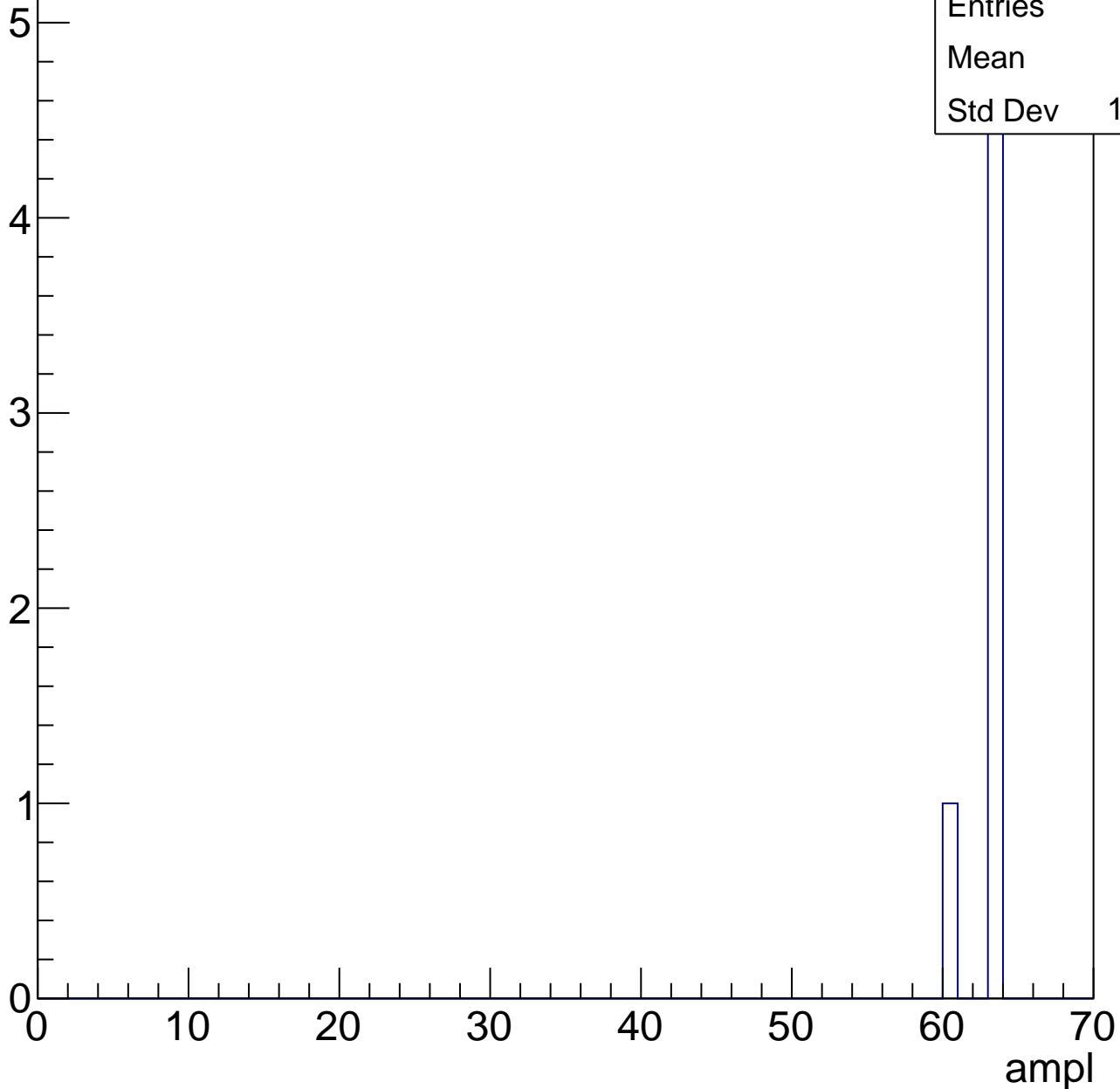


# B1L003S, U3-ch57, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	6
Mean	62.5
Std Dev	1.118





# B1L003S, U3-ch57, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U3-ch58, adc0

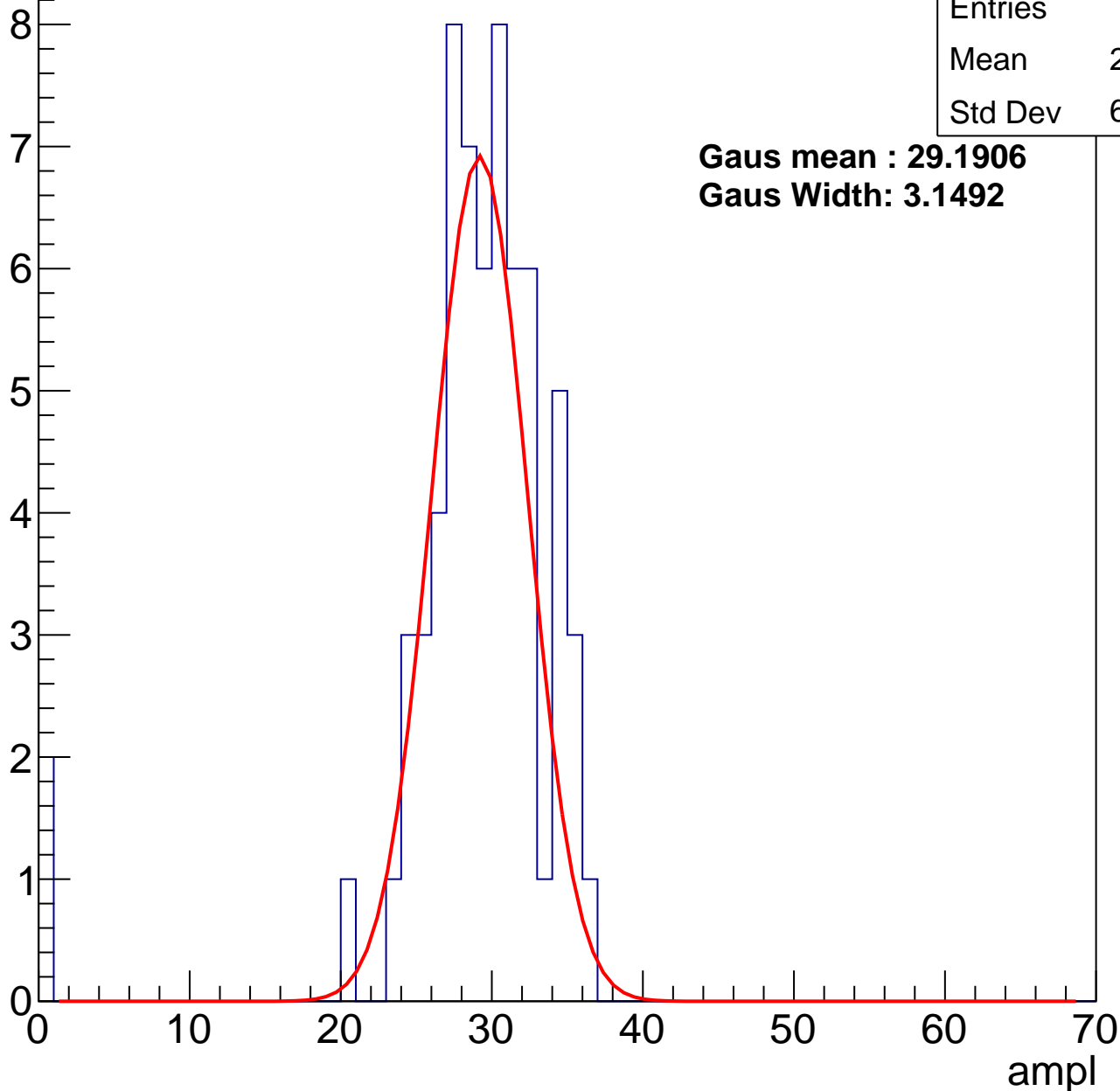
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	28.34
Std Dev	6.016

**Gaus mean : 29.1906**

**Gaus Width: 3.1492**



# B1L003S, U3-ch58, adc1

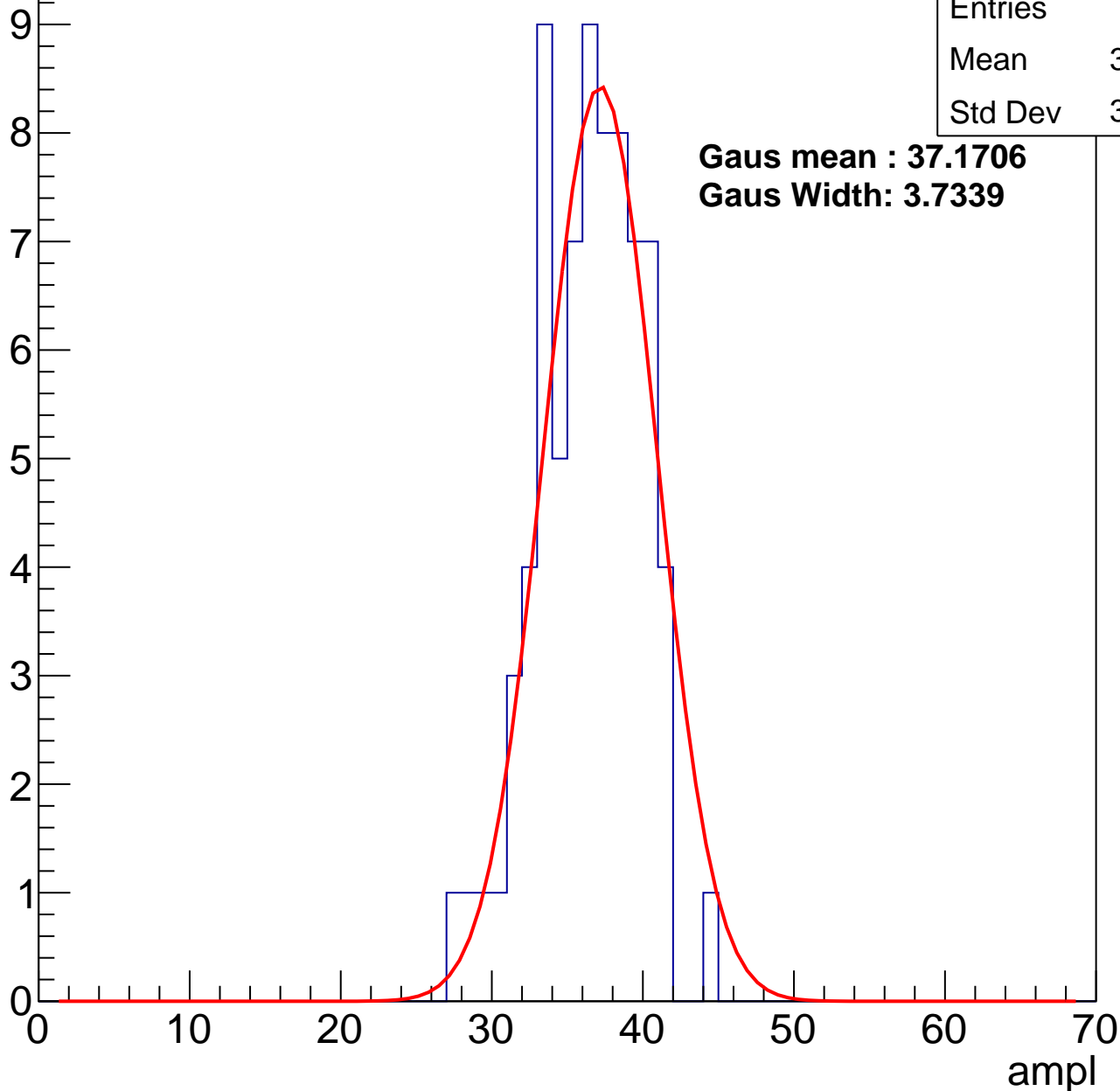
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	76
Mean	35.95
Std Dev	3.356

**Gaus mean : 37.1706**

**Gaus Width: 3.7339**



# B1L003S, U3-ch58, adc2

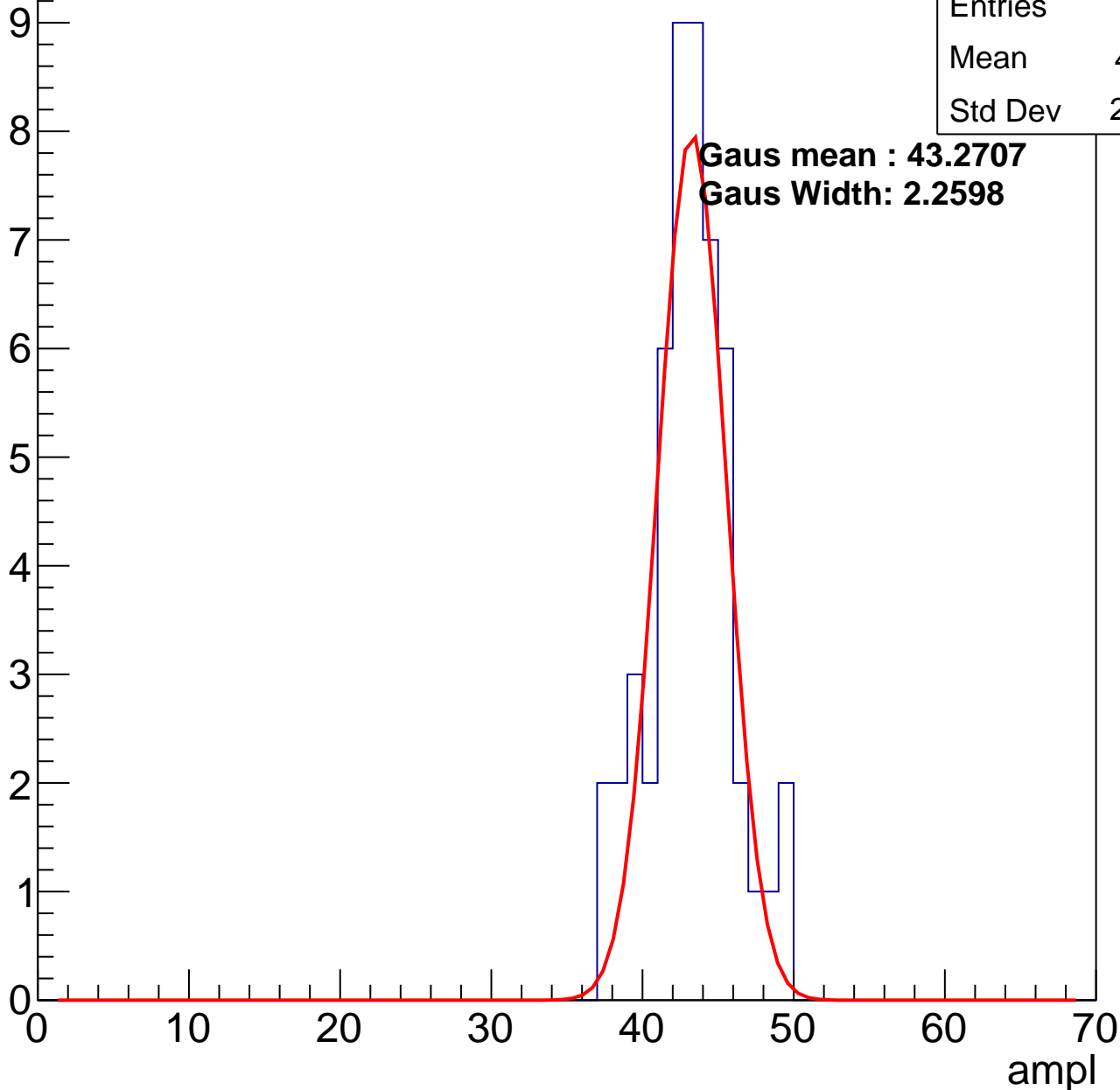
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	52
Mean	42.71
Std Dev	2.699

**Gaus mean : 43.2707**

**Gaus Width: 2.2598**



# B1L003S, U3-ch58, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

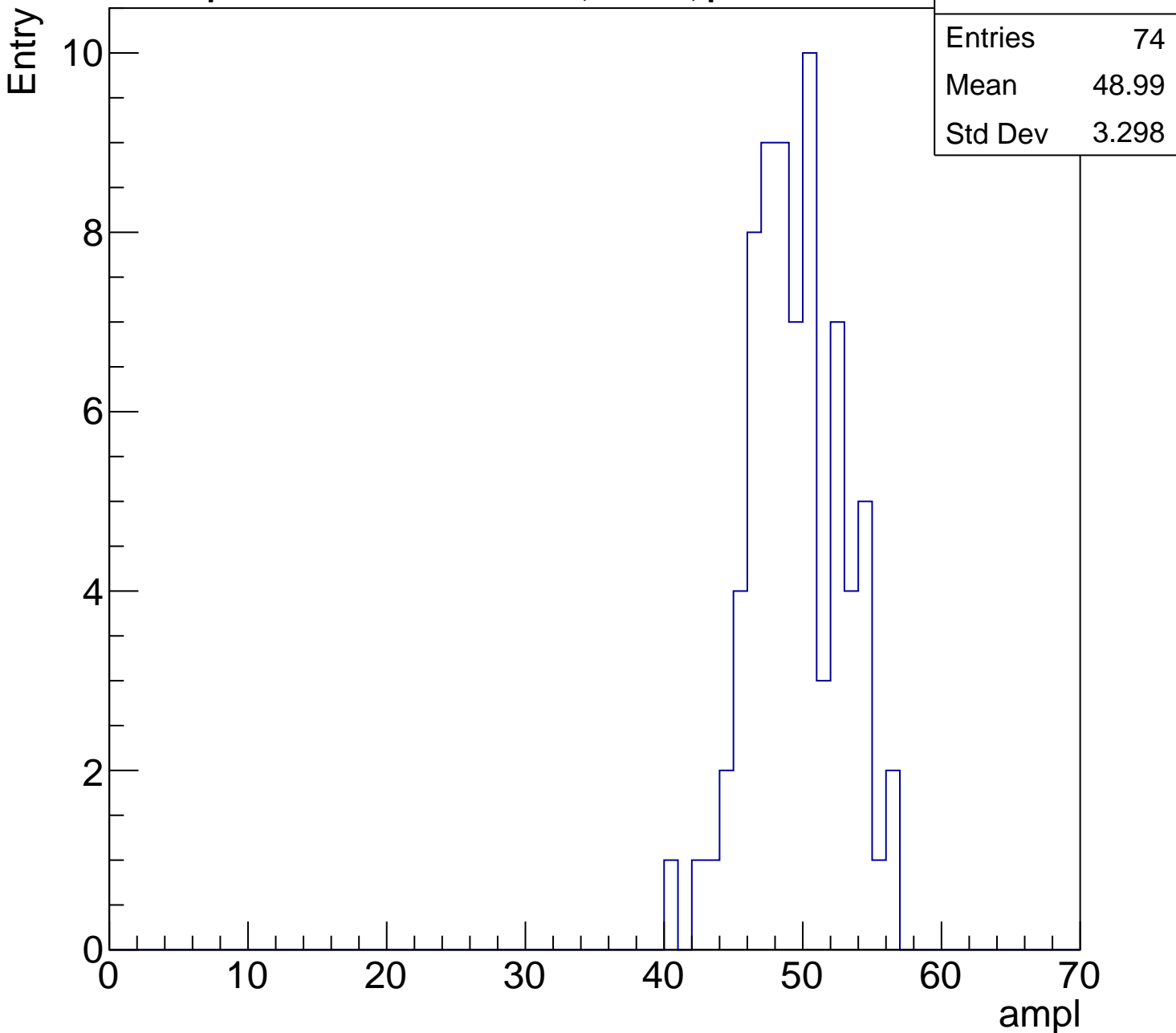
Entries	74
Mean	48.99
Std Dev	3.298

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

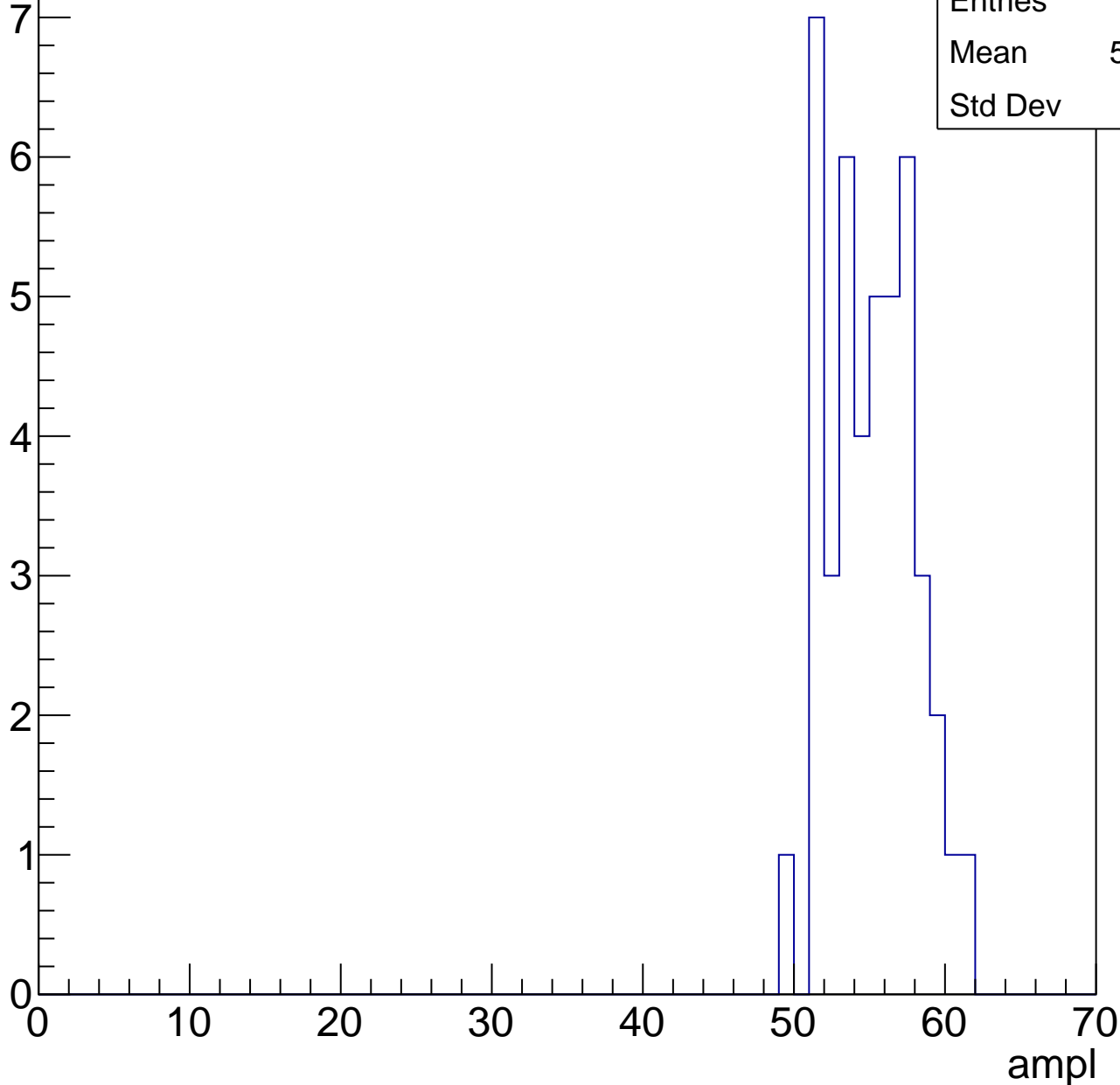


# B1L003S, U3-ch58, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	44
Mean	54.68
Std Dev	2.81

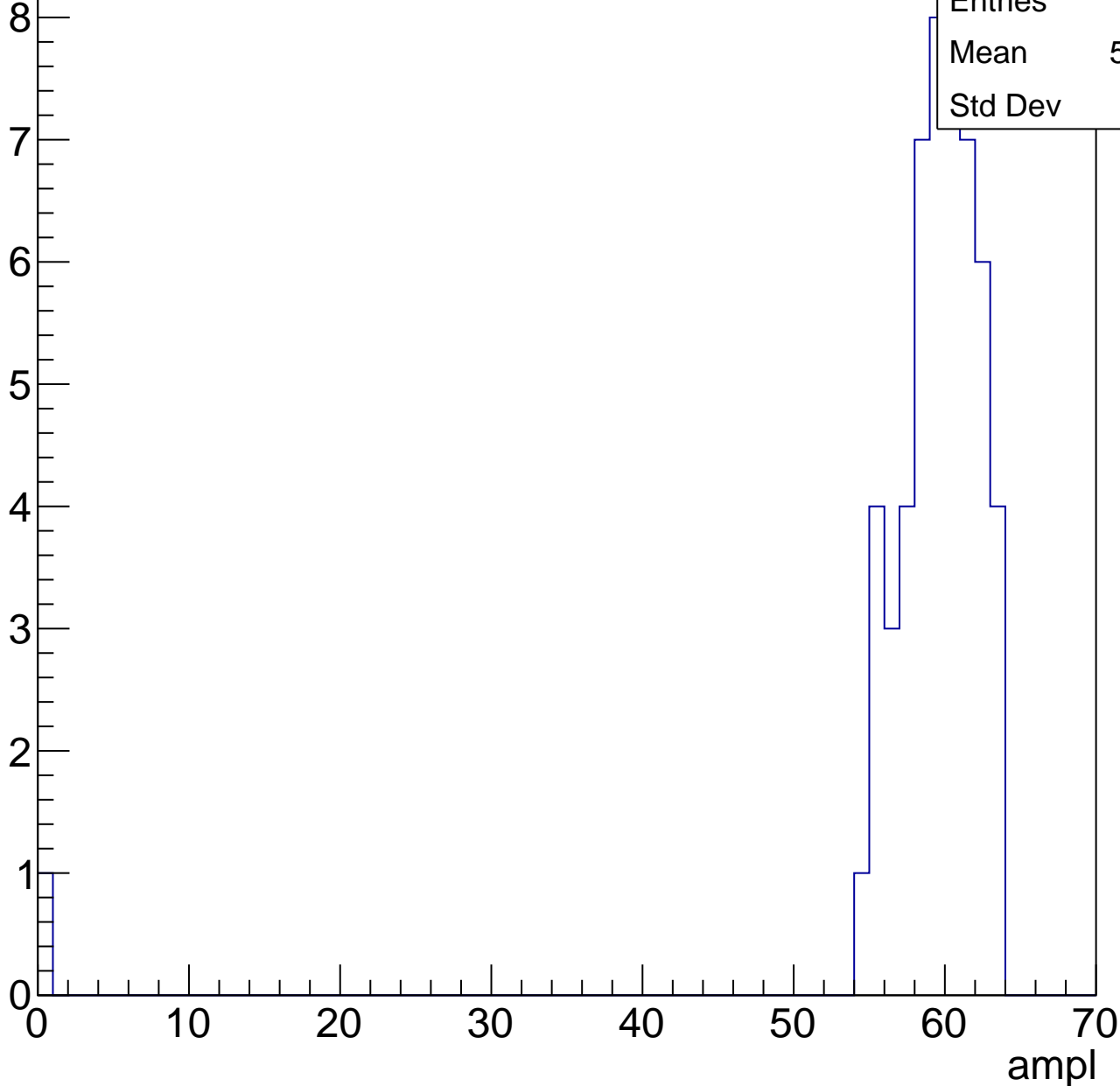


# B1L003S, U3-ch58, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	58.09
Std Dev	8.39

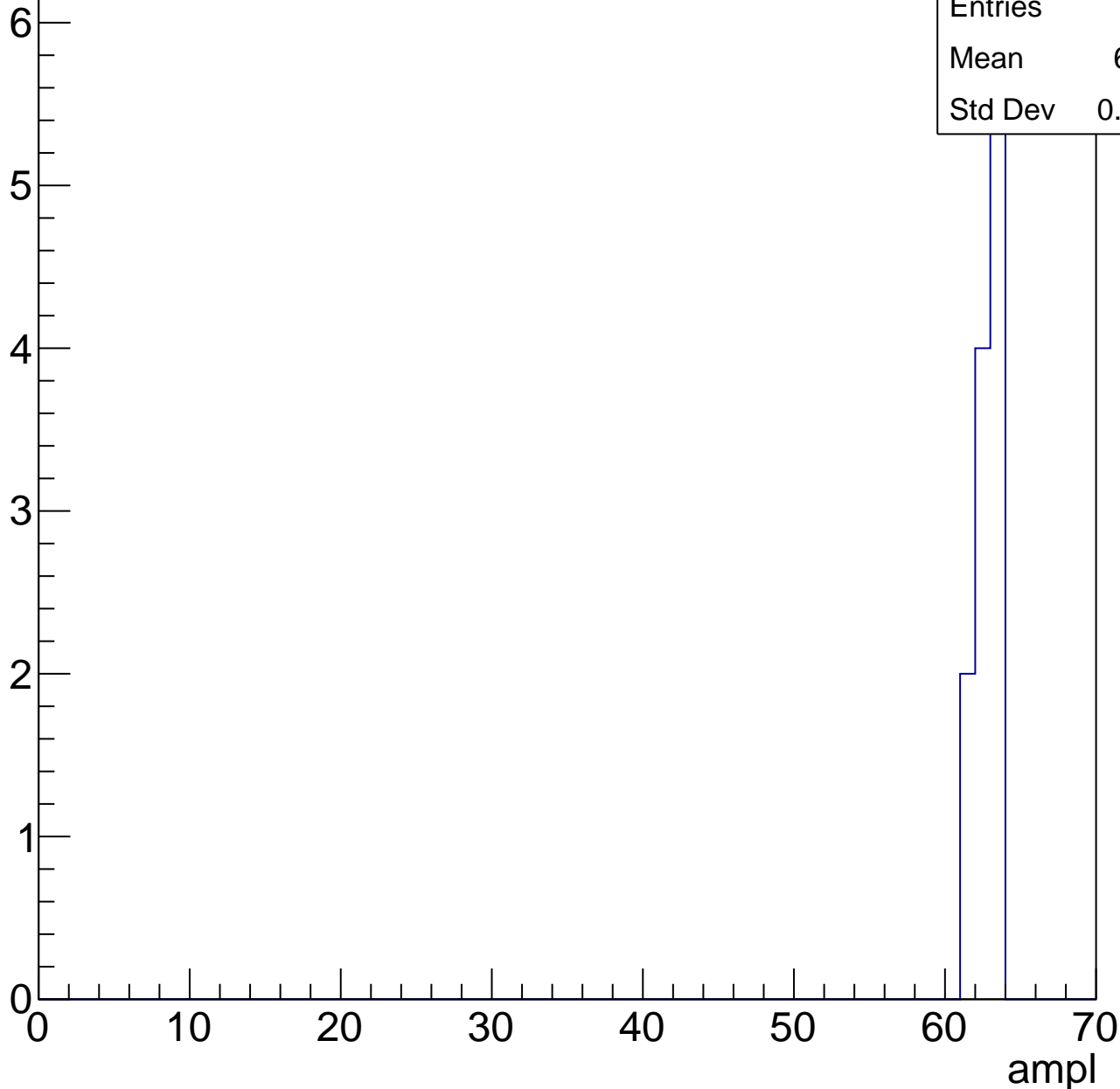


# B1L003S, U3-ch58, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	12
Mean	62.33
Std Dev	0.7454





# B1L003S, U3-ch58, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U3-ch59, adc0

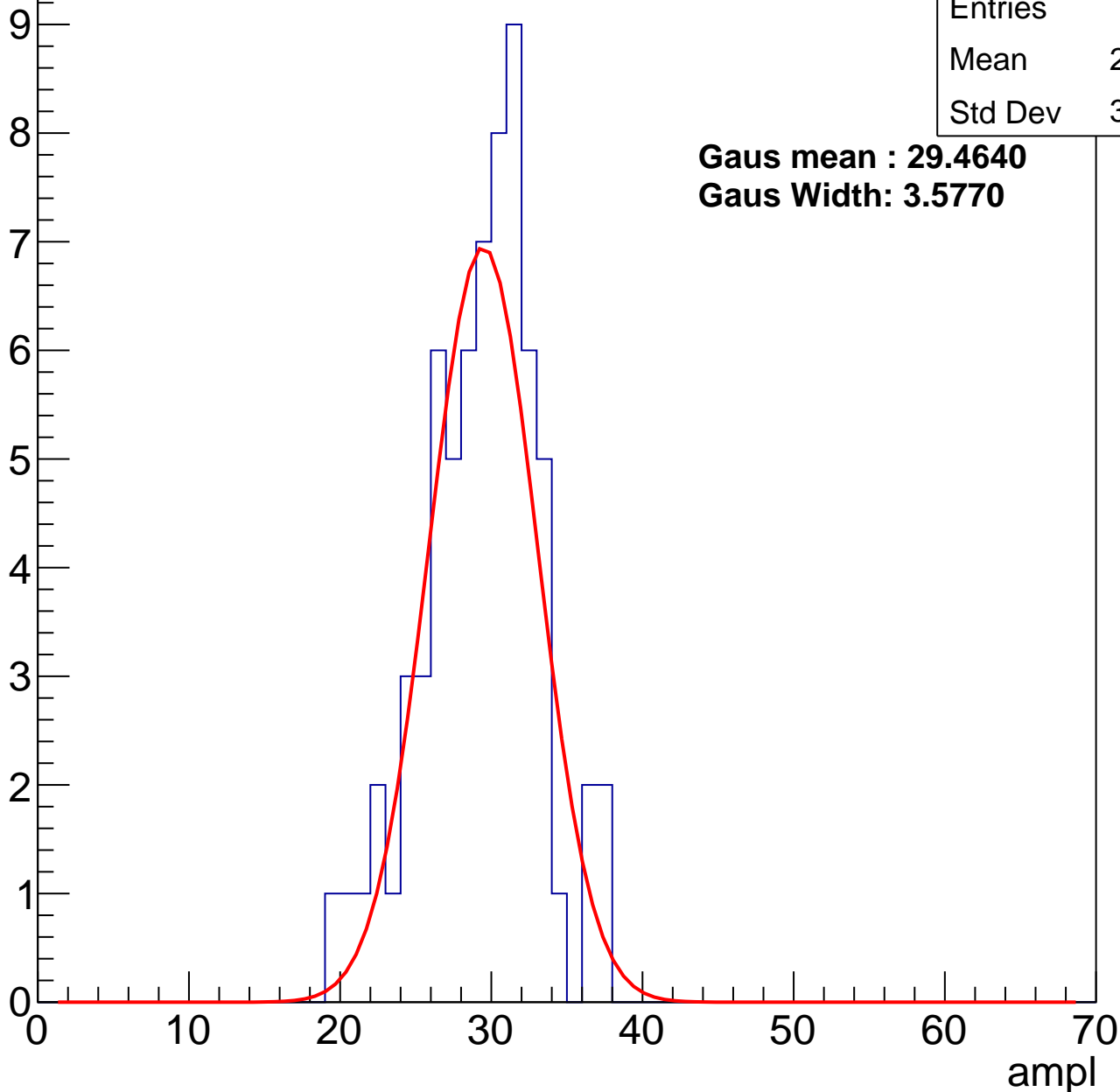
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	28.87
Std Dev	3.826

**Gaus mean : 29.4640**

**Gaus Width: 3.5770**



# B1L003S, U3-ch59, adc1

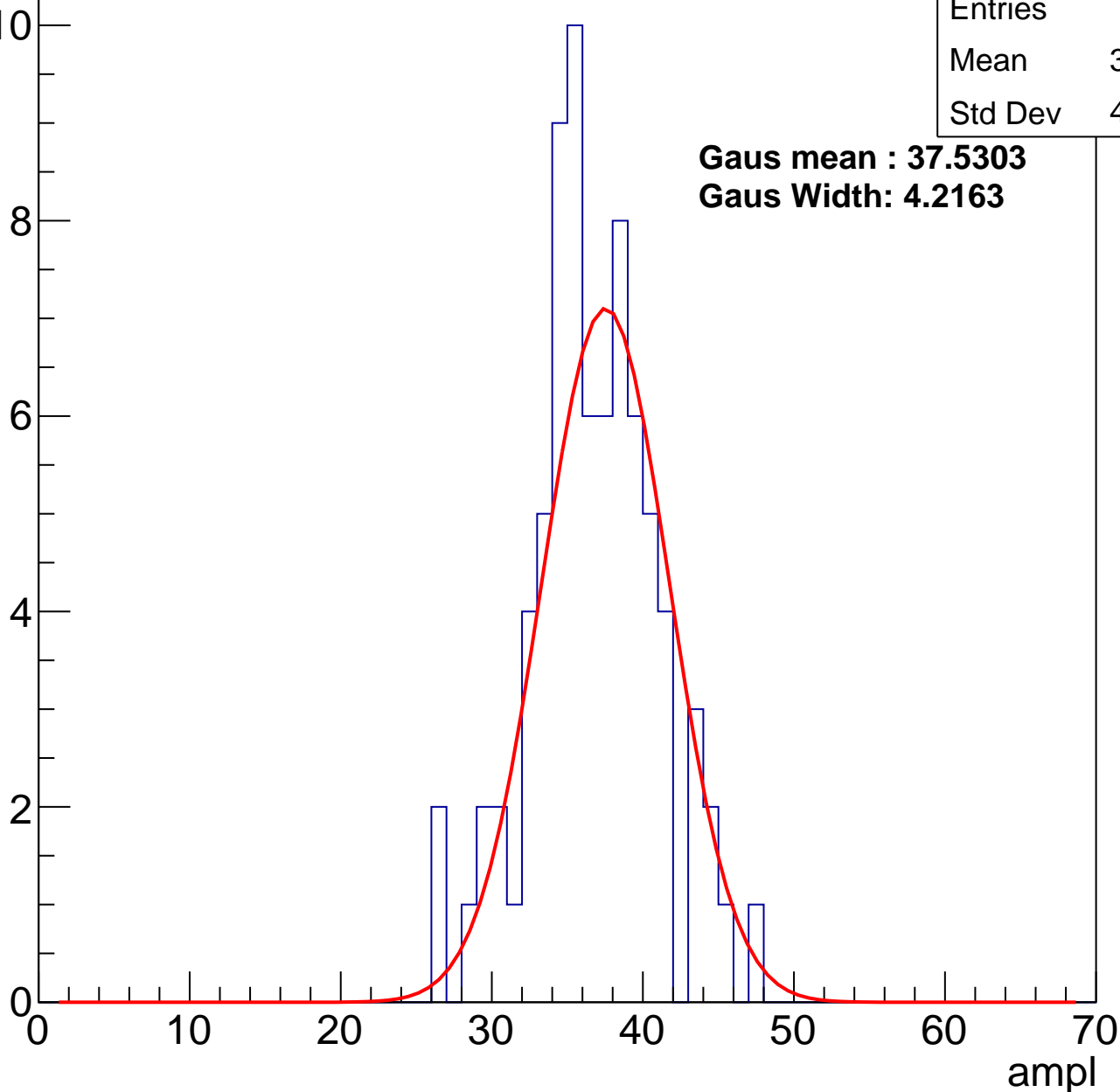
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	78
Mean	36.24
Std Dev	4.173

**Gaus mean : 37.5303**

**Gaus Width: 4.2163**



# B1L003S, U3-ch59, adc2

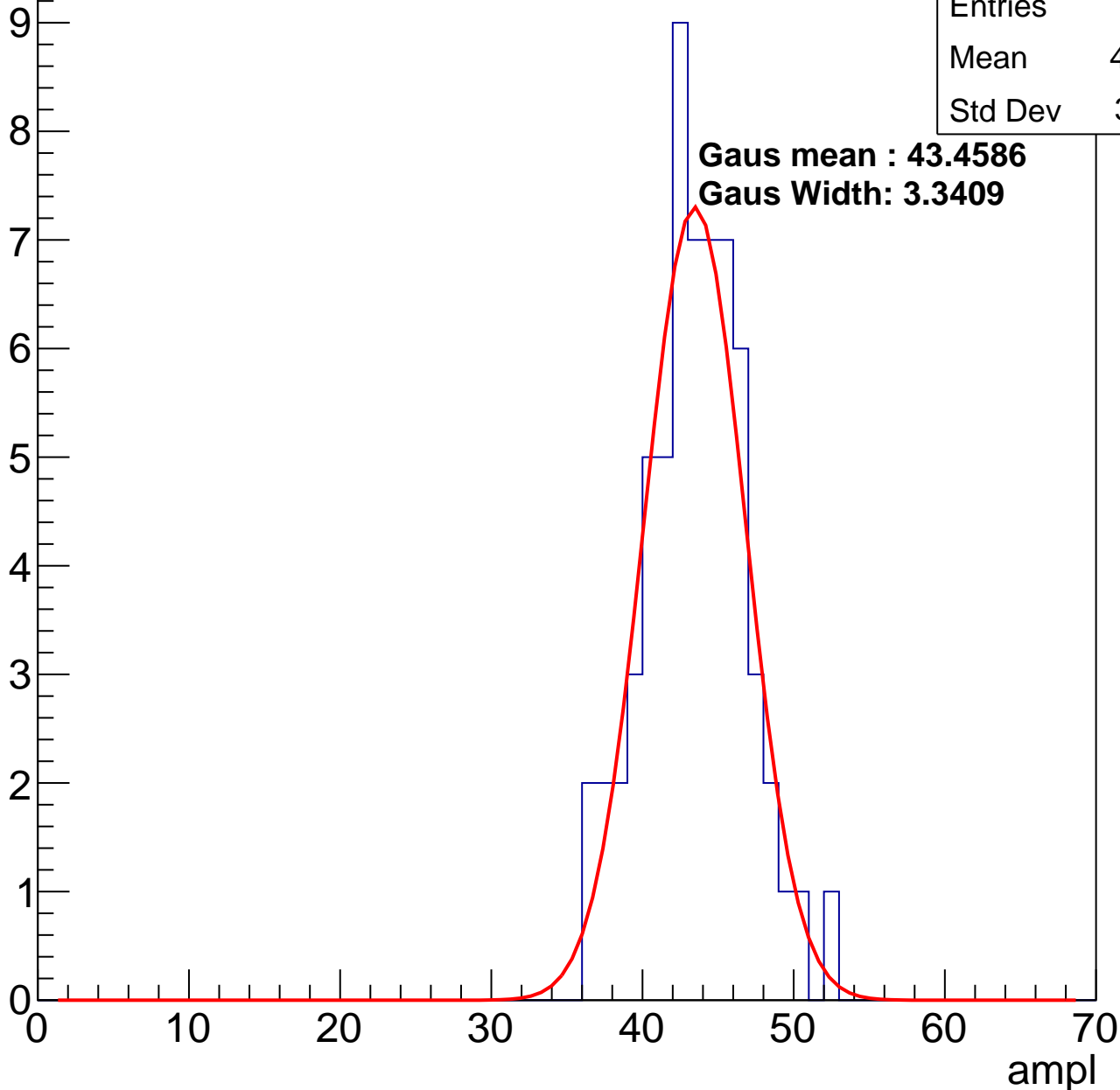
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	43.02
Std Dev	3.321

**Gaus mean : 43.4586**

**Gaus Width: 3.3409**

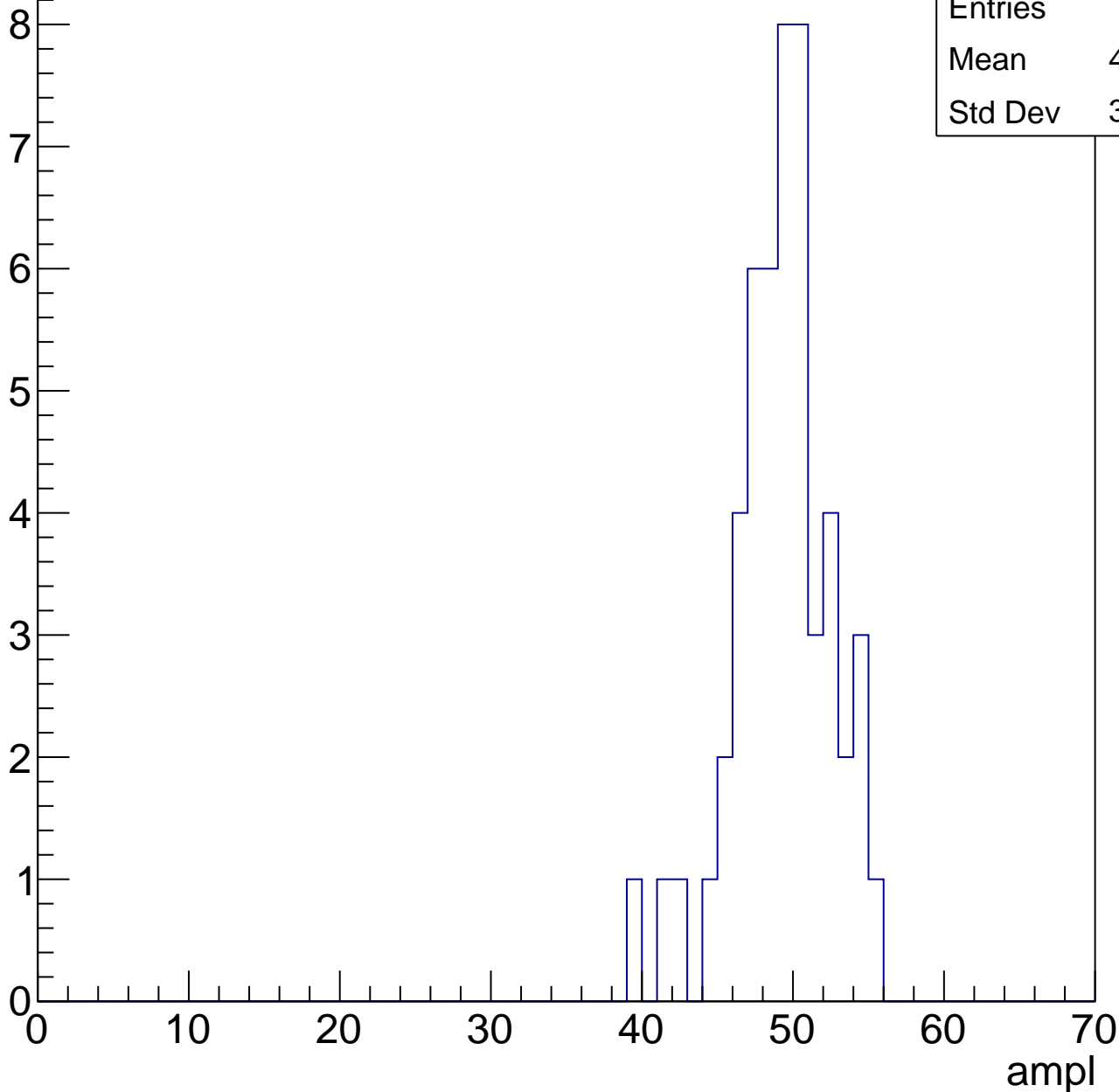


# B1L003S, U3-ch59, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	51
Mean	48.75
Std Dev	3.229

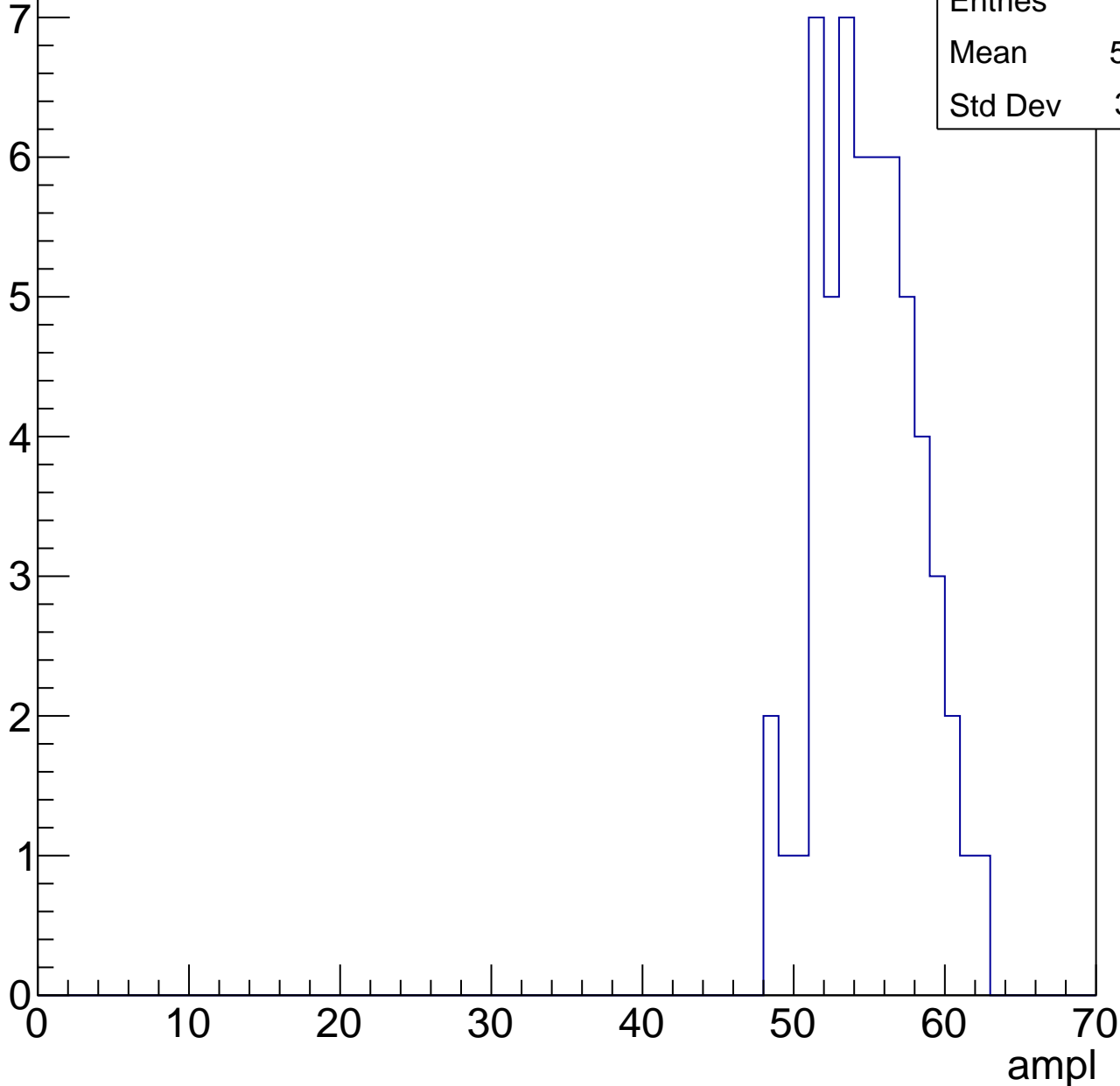


# B1L003S, U3-ch59, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	54.56
Std Dev	3.201

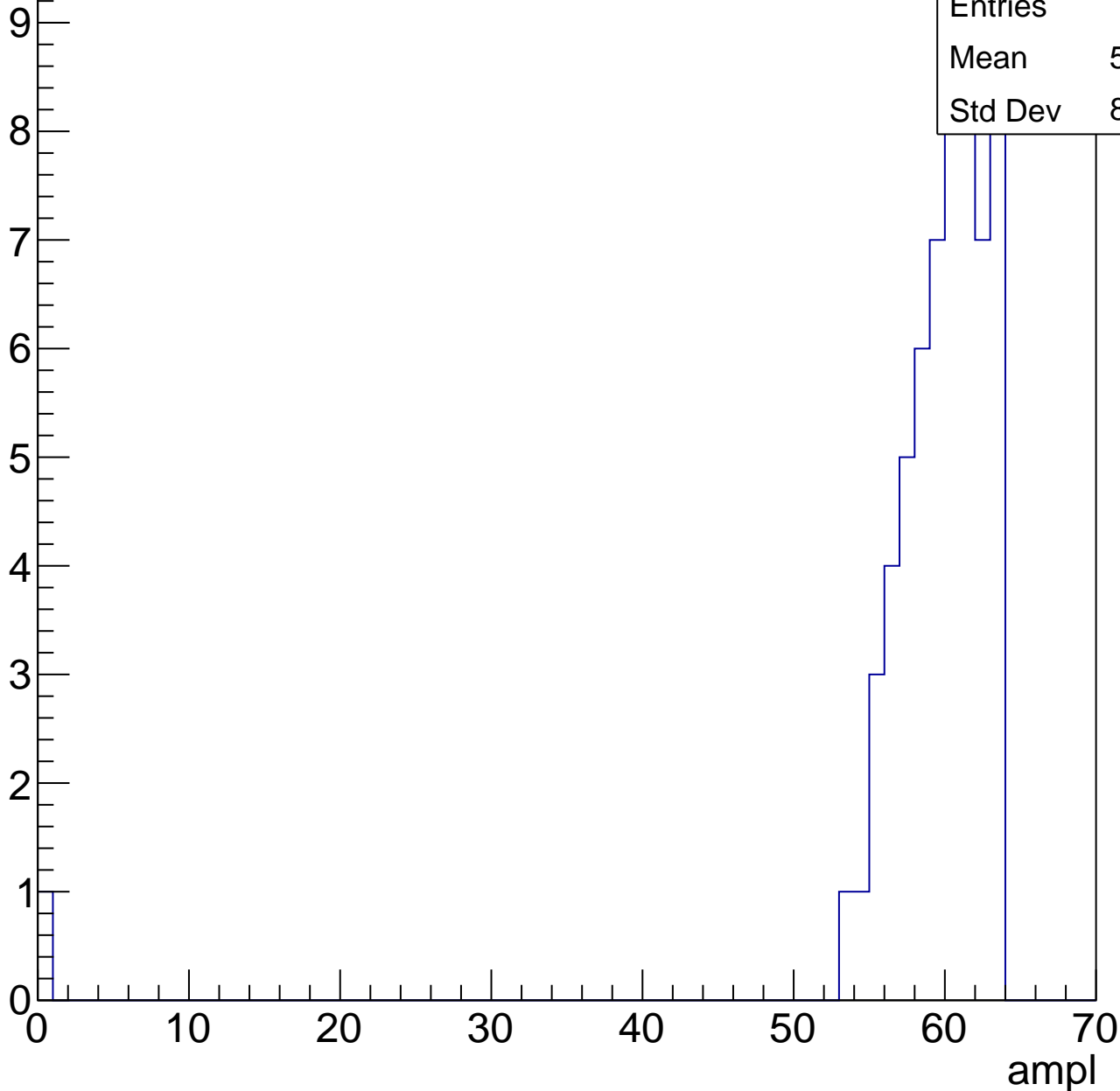


# B1L003S, U3-ch59, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	58.52
Std Dev	8.047



# B1L003S, U3-ch59, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

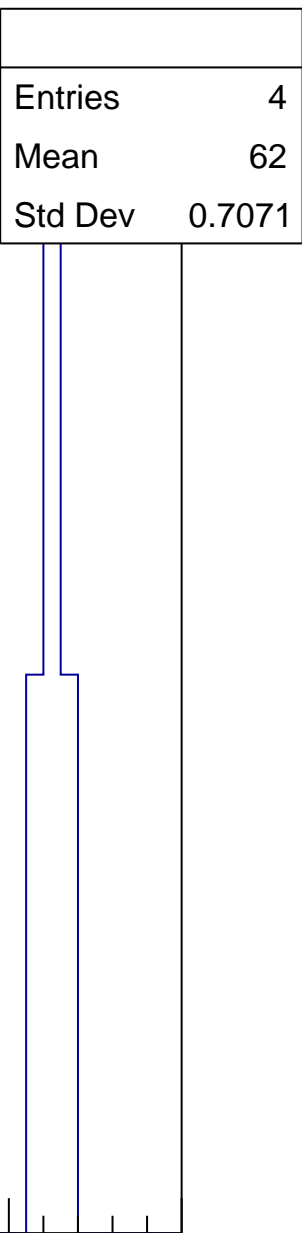
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	62
Std Dev	0.7071

0 10 20 30 40 50 60 70

ampl





# B1L003S, U3-ch59, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U3-ch60, adc0

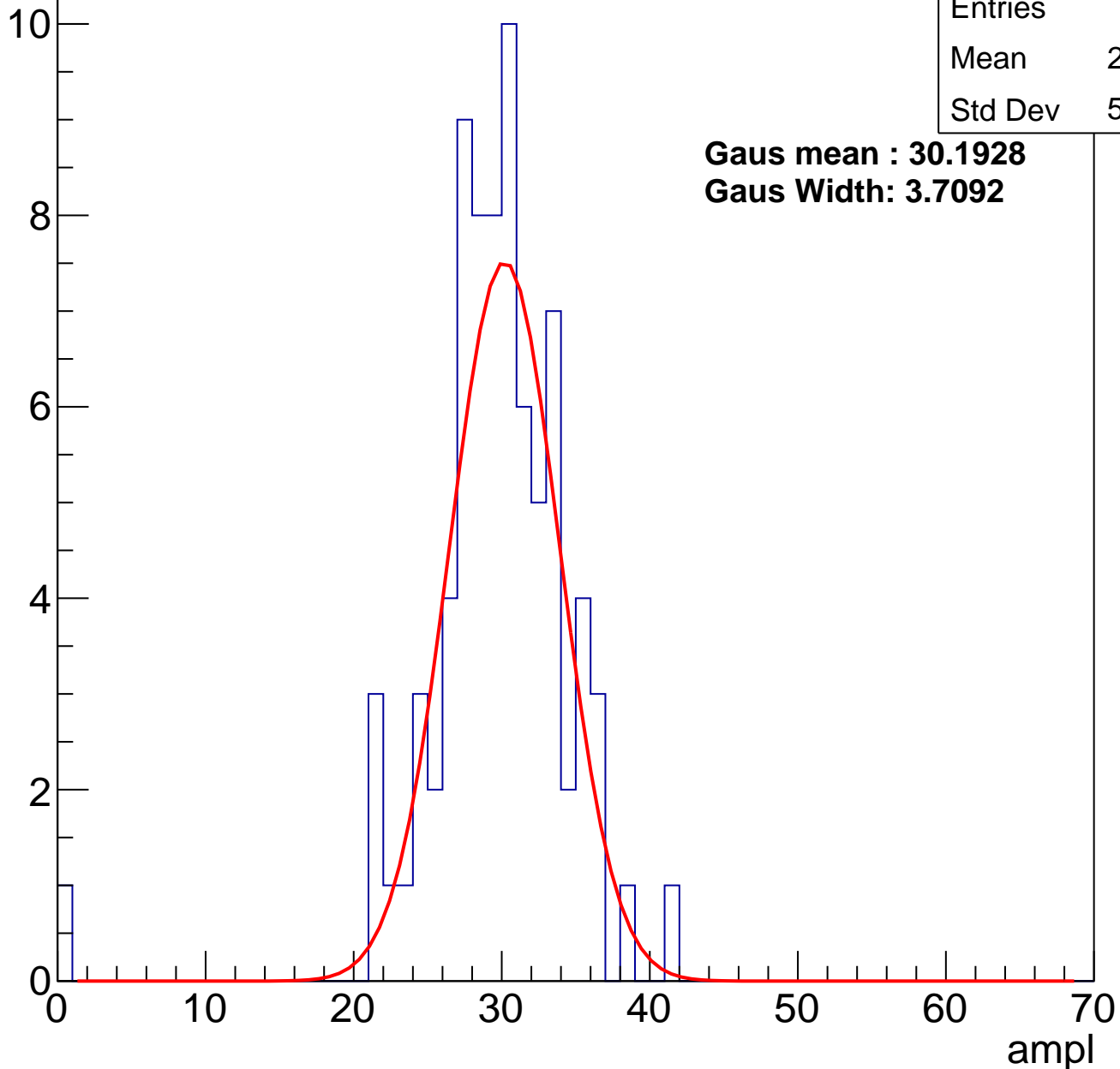
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	79
Mean	29.18
Std Dev	5.106

**Gaus mean : 30.1928**

**Gaus Width: 3.7092**

Entry



# B1L003S, U3-ch60, adc1

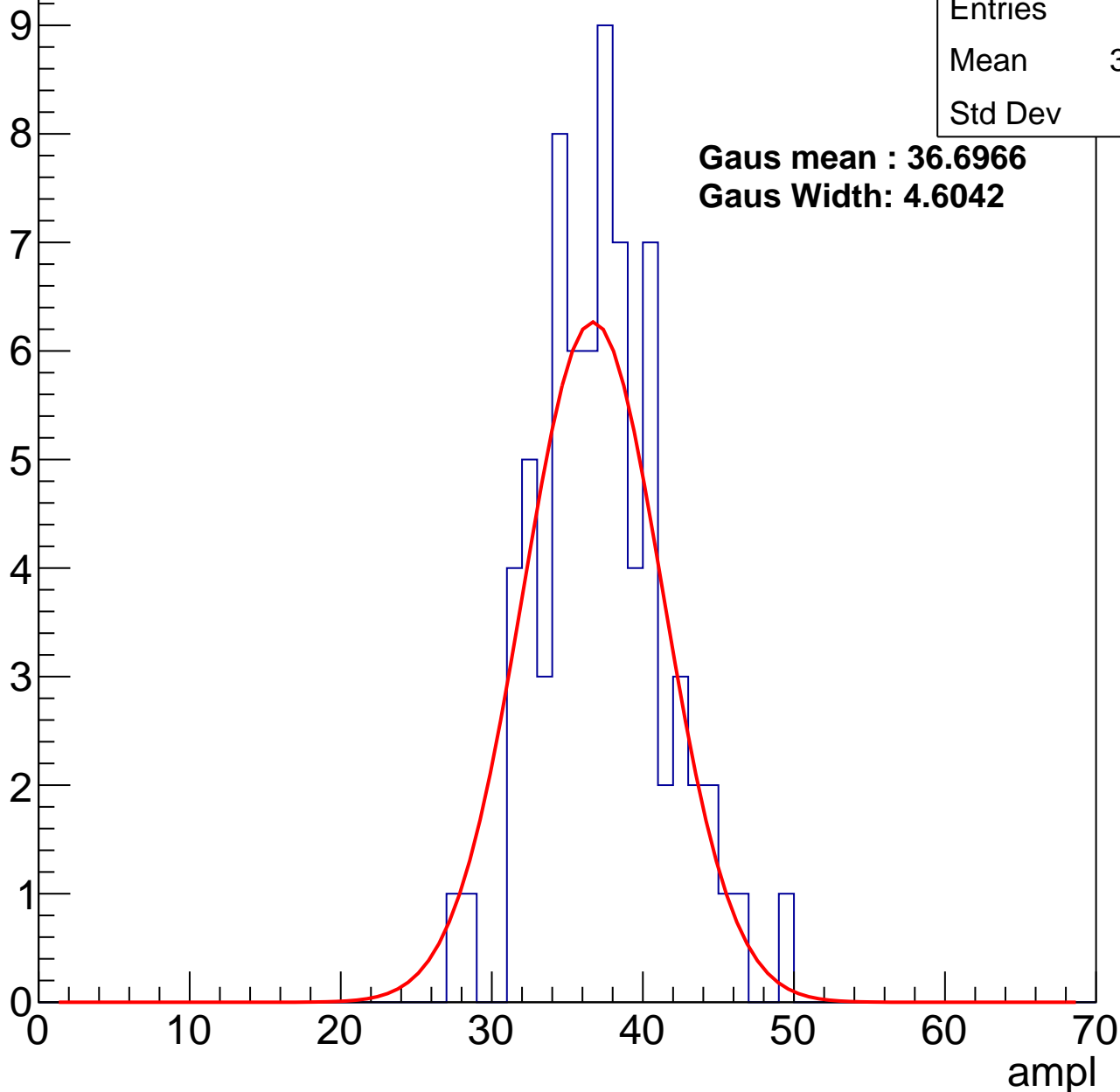
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	73
Mean	36.89
Std Dev	4.14

**Gaus mean : 36.6966**

**Gaus Width: 4.6042**



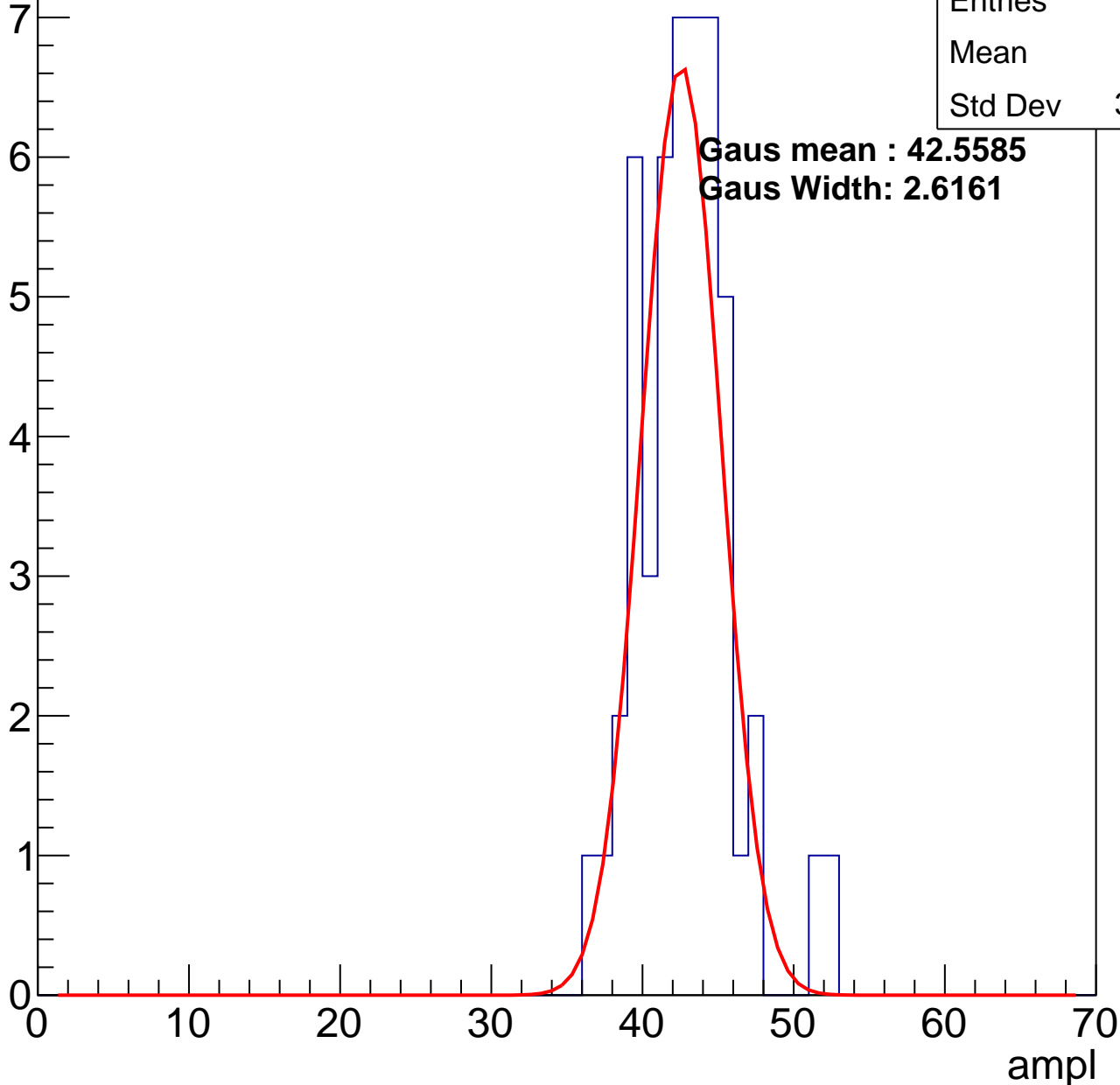
# B1L003S, U3-ch60, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	50
Mean	42.4
Std Dev	3.111

**Gaus mean : 42.5585**  
**Gaus Width: 2.6161**

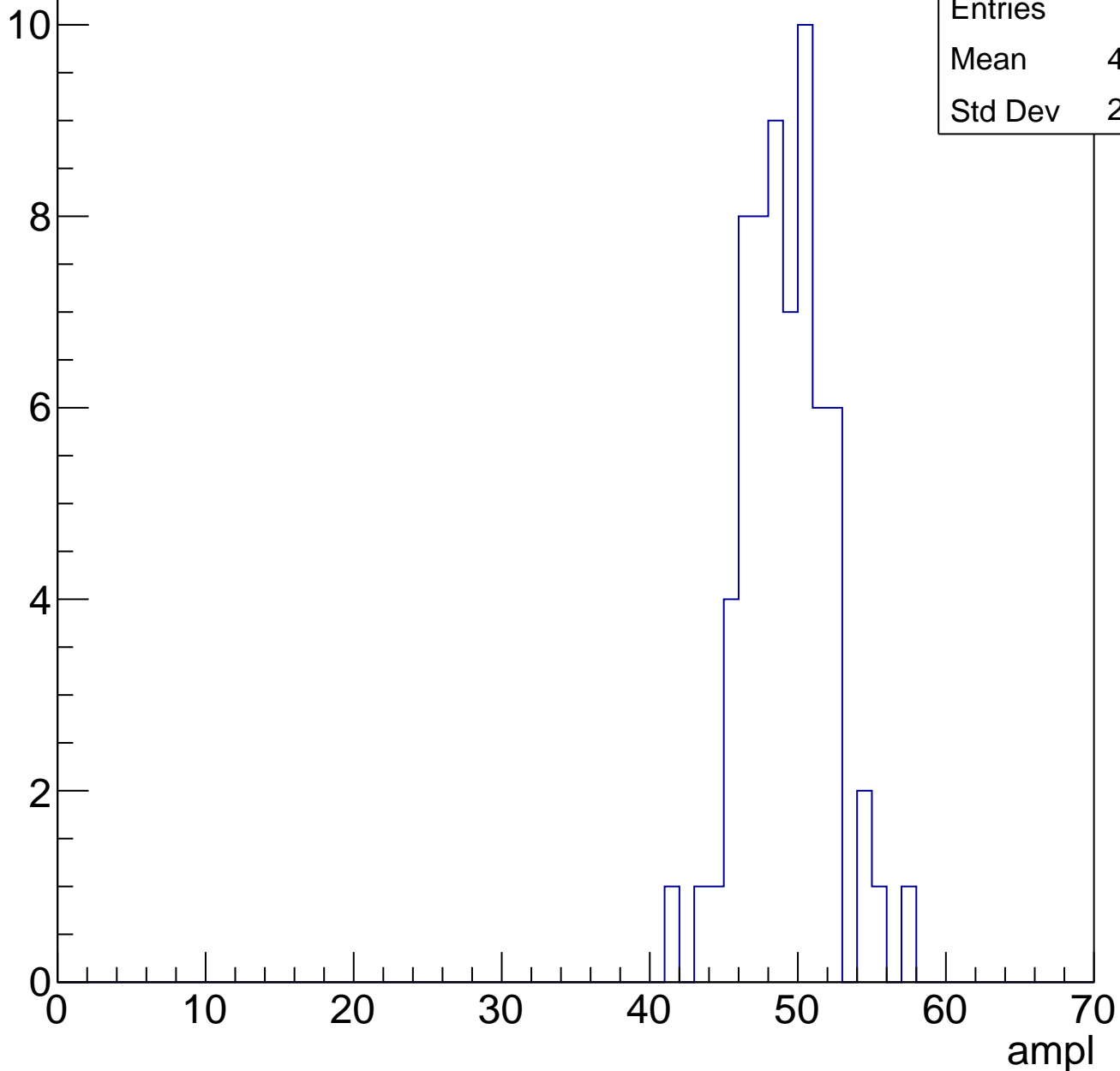


# B1L003S, U3-ch60, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	65
Mean	48.69
Std Dev	2.866

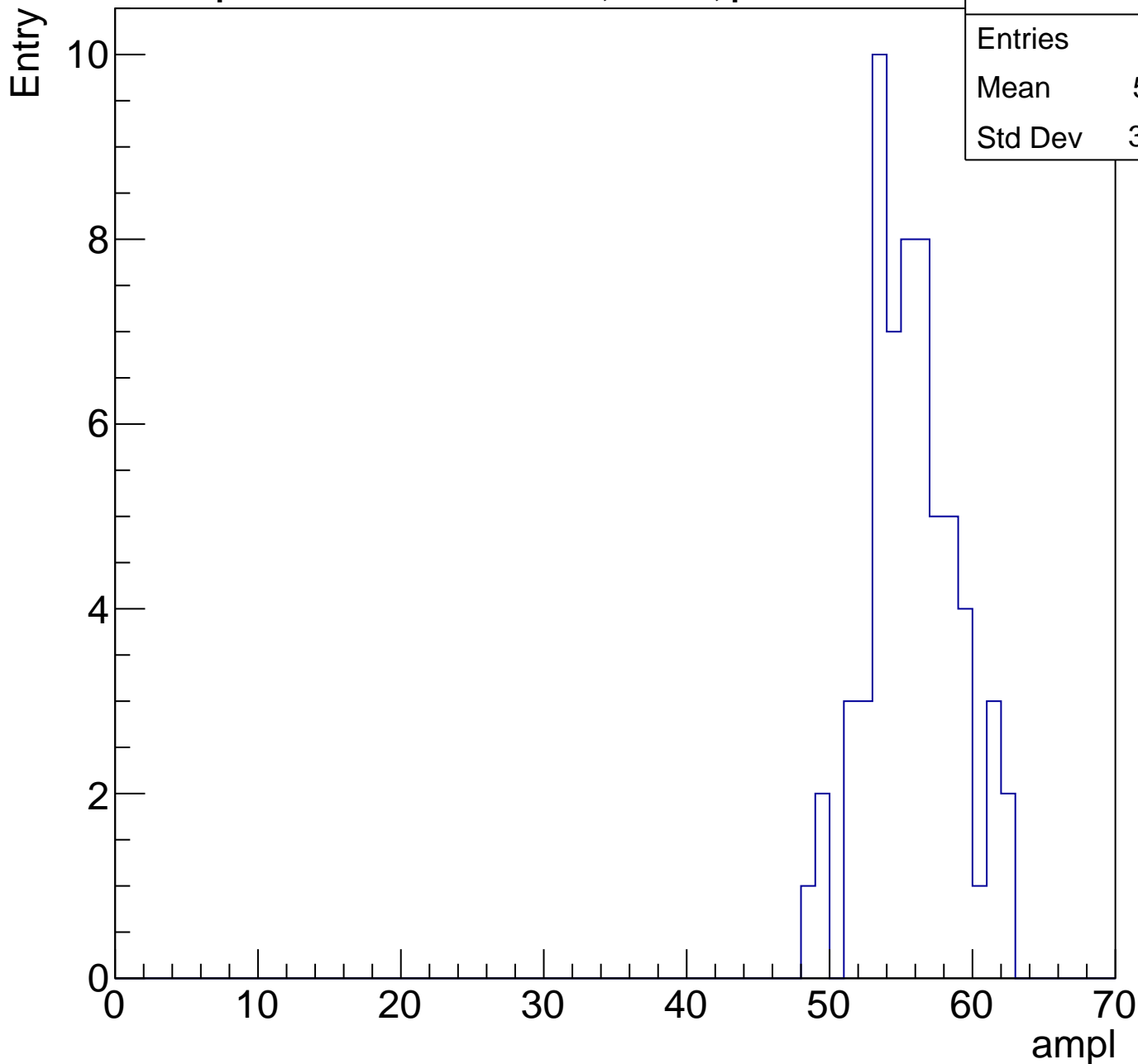
Entry



# B1L003S, U3-ch60, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	62
Mean	55.31
Std Dev	3.124



# B1L003S, U3-ch60, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

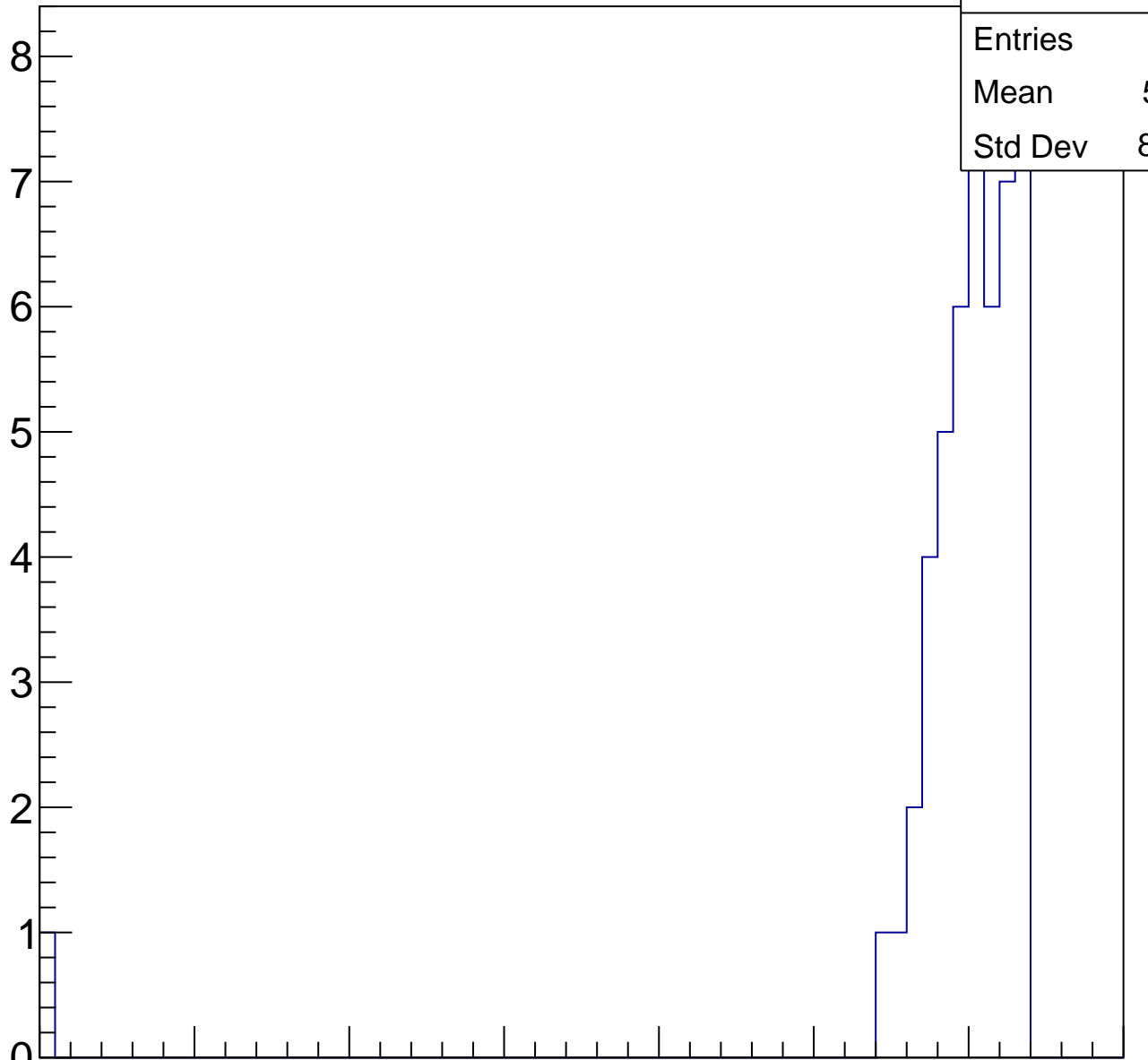
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	49
Mean	58.71
Std Dev	8.783

ampl

0 10 20 30 40 50 60 70



# B1L003S, U3-ch60, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

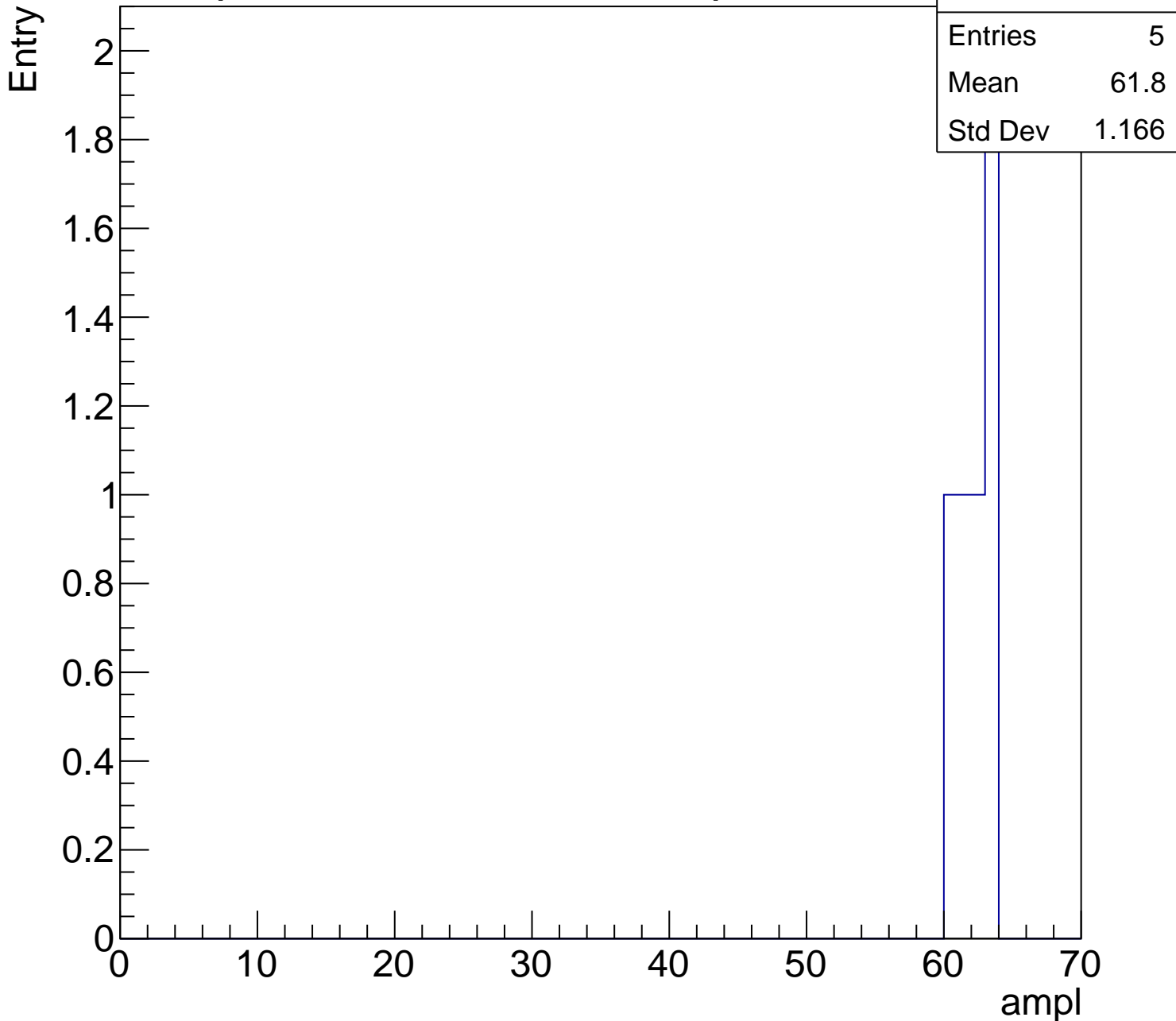
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	61.8
Std Dev	1.166

0 10 20 30 40 50 60 70

ampl





# B1L003S, U3-ch60, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L003S, U3-ch61, adc0

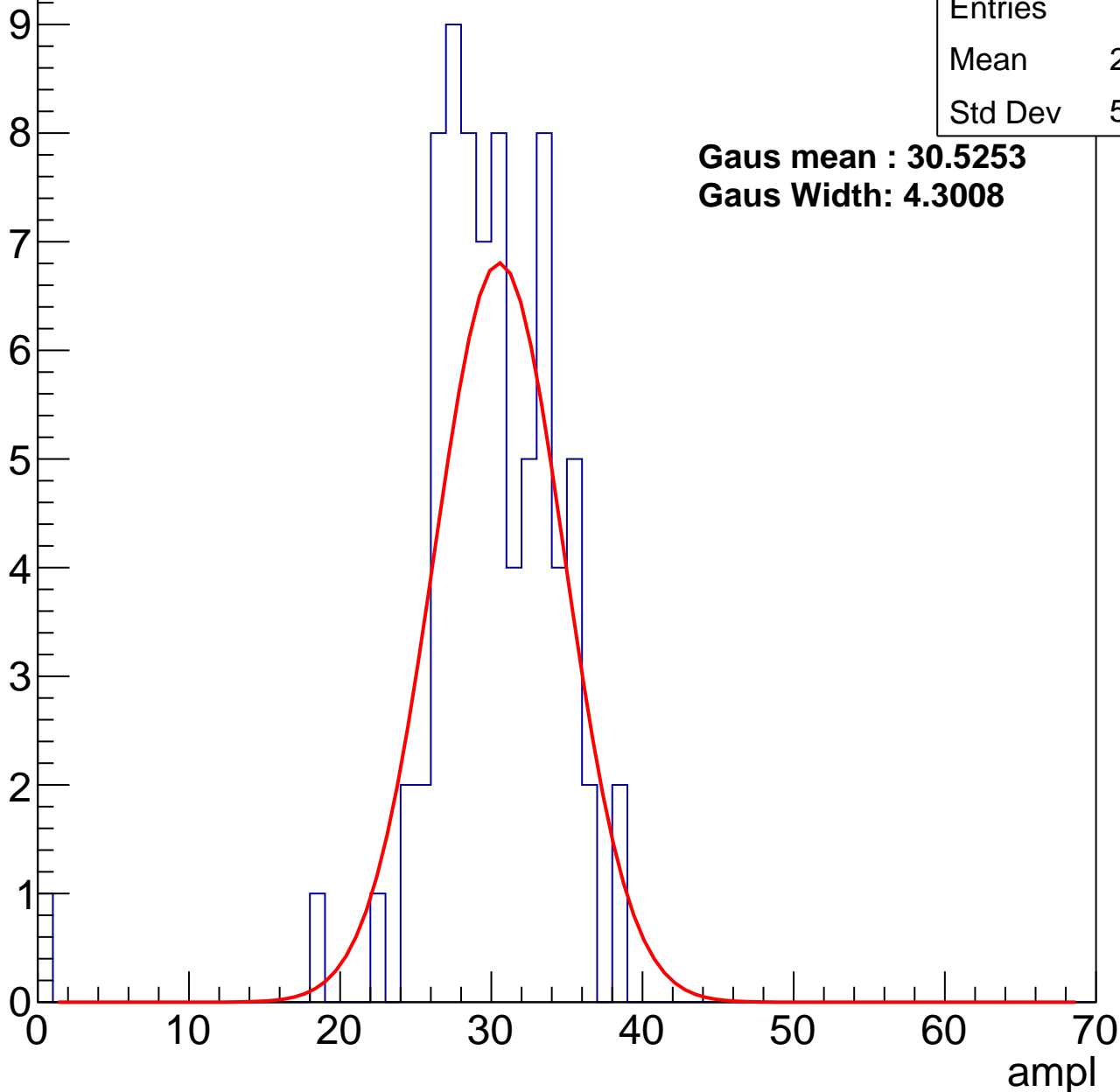
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	77
Mean	29.39
Std Dev	5.012

**Gaus mean : 30.5253**

**Gaus Width: 4.3008**



# B1L003S, U3-ch61, adc1

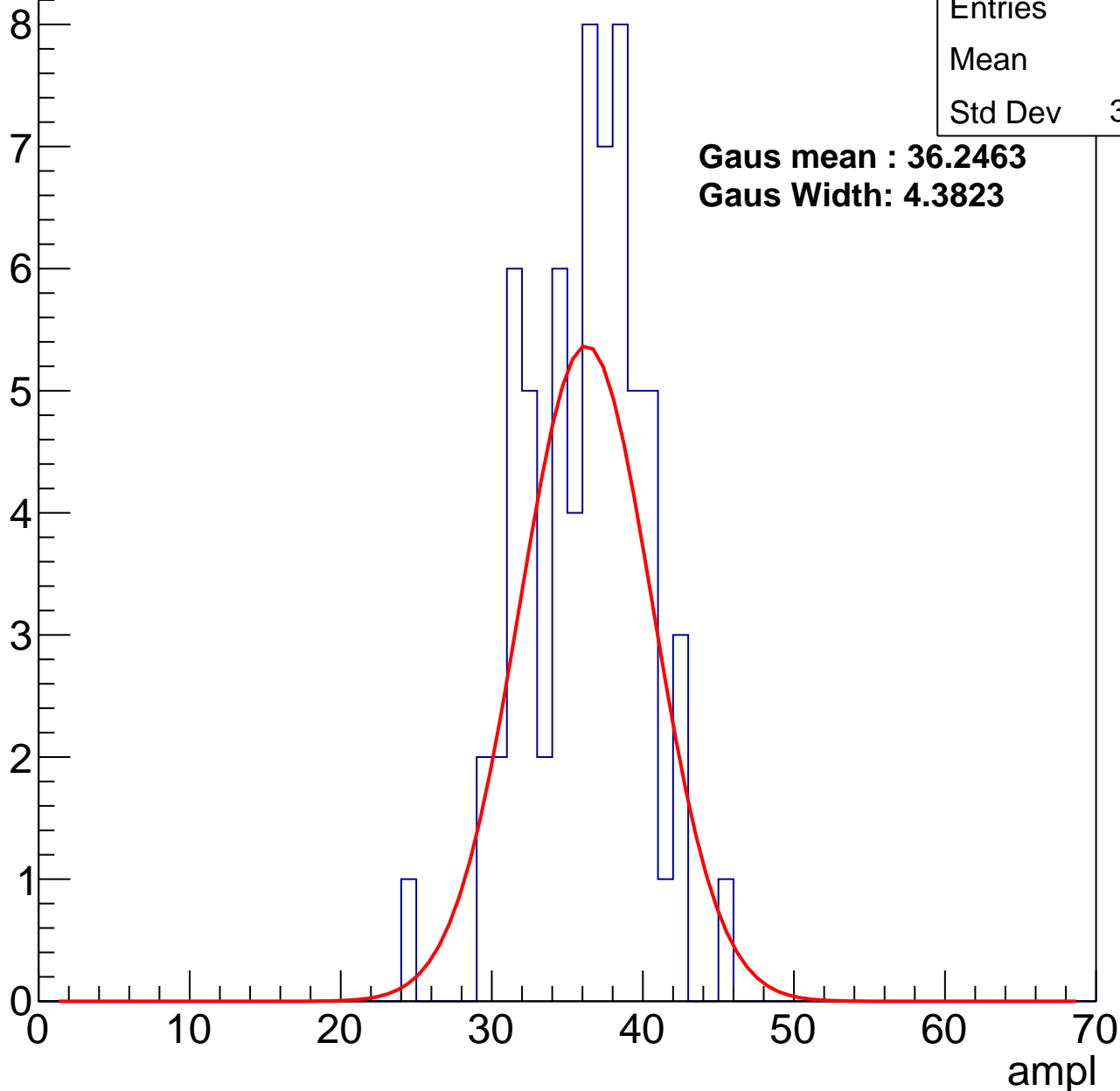
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	35.7
Std Dev	3.818

**Gaus mean : 36.2463**

**Gaus Width: 4.3823**



# B1L003S, U3-ch61, adc2

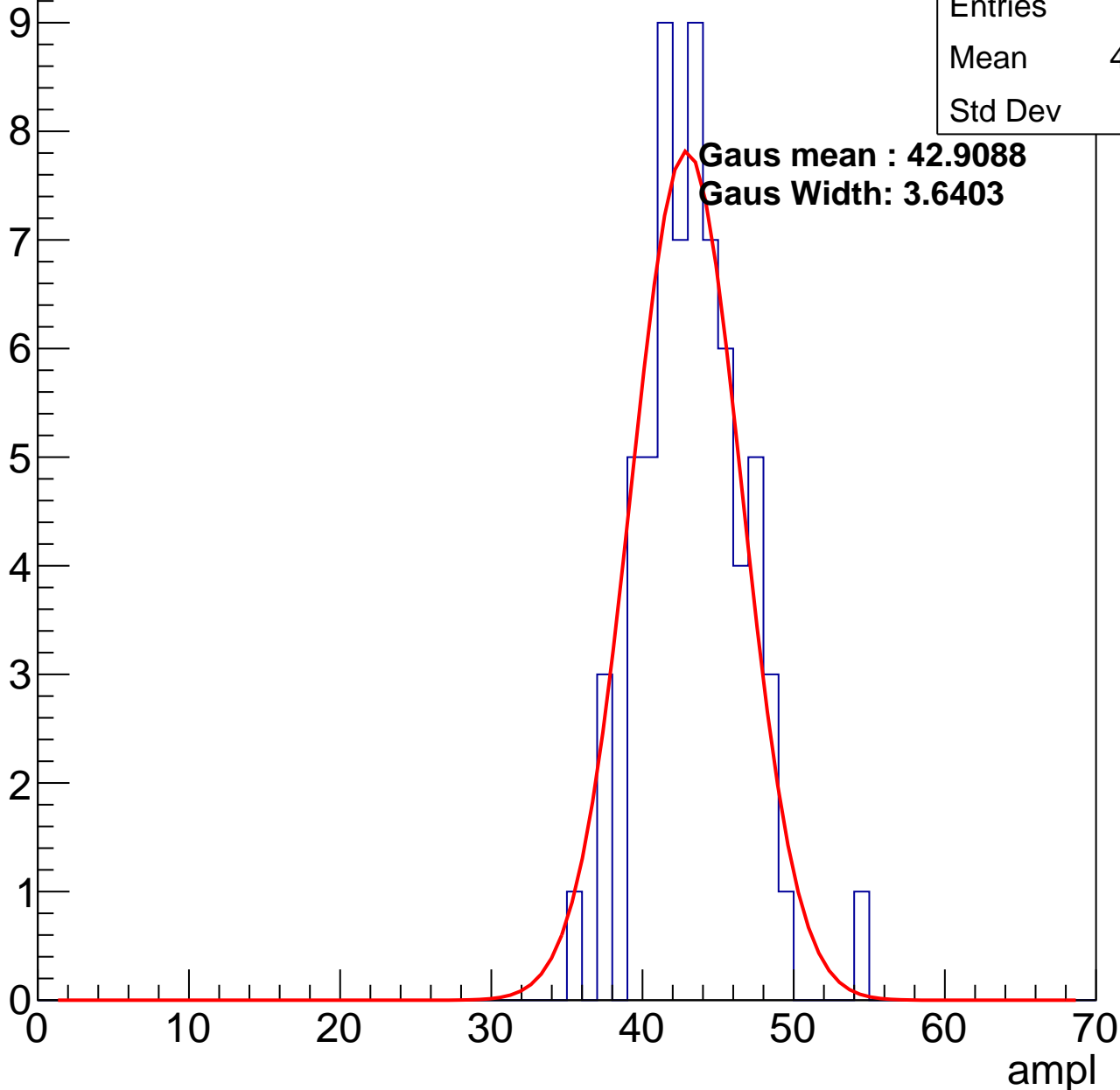
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	42.95
Std Dev	3.3

**Gaus mean : 42.9088**

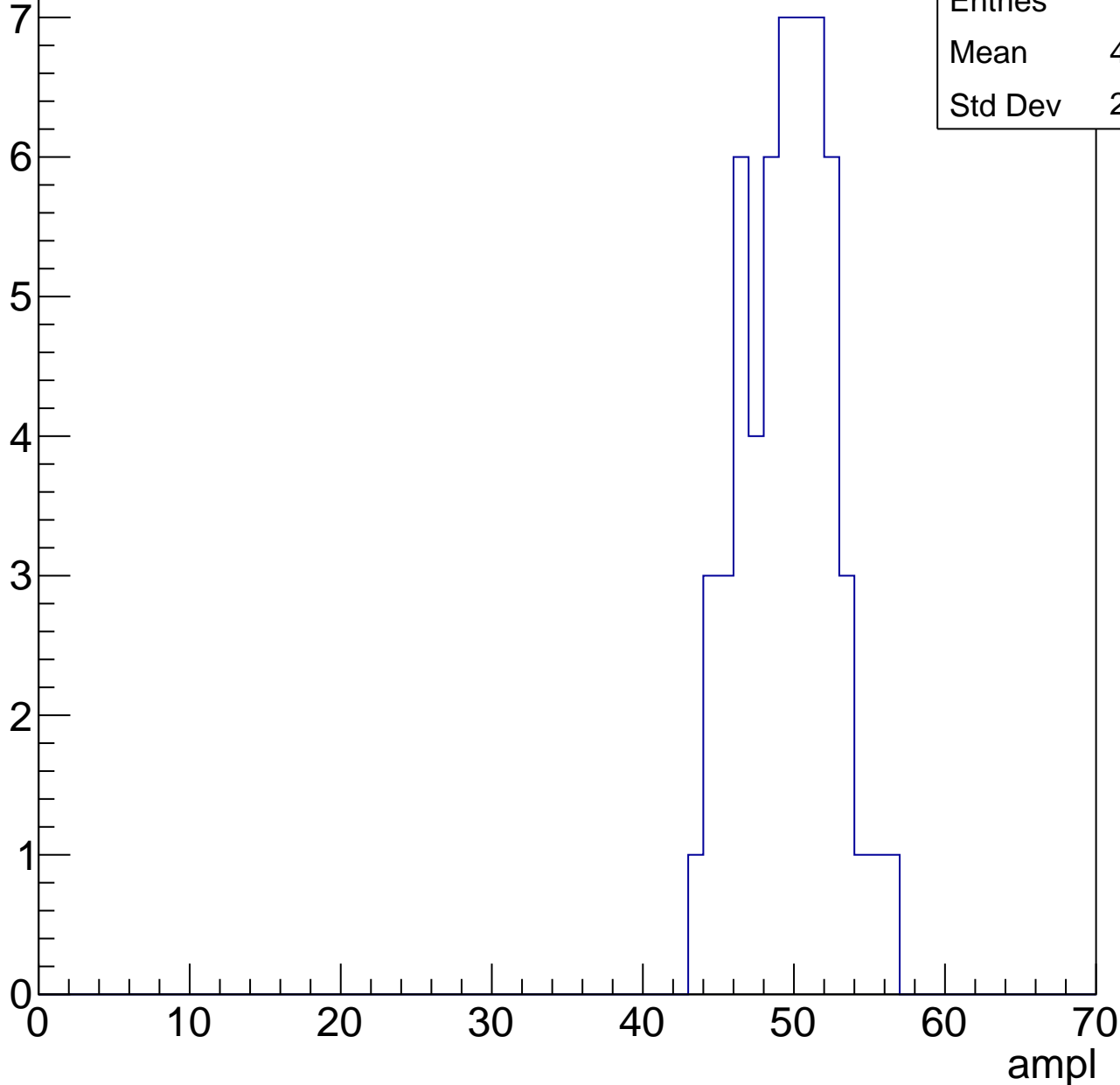
**Gaus Width: 3.6403**



# B1L003S, U3-ch61, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



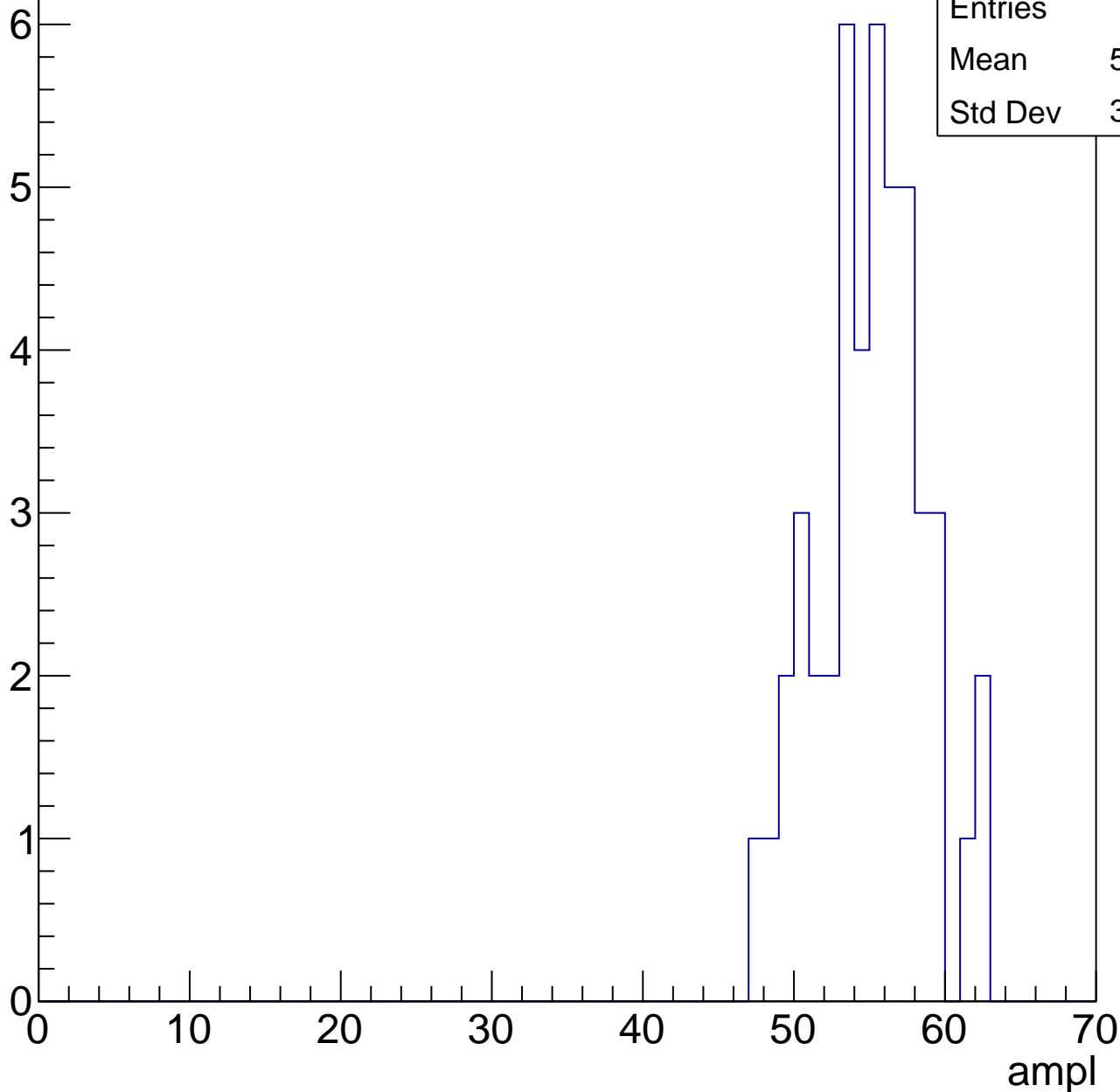
Entries	56
Mean	49.07
Std Dev	2.933

# B1L003S, U3-ch61, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

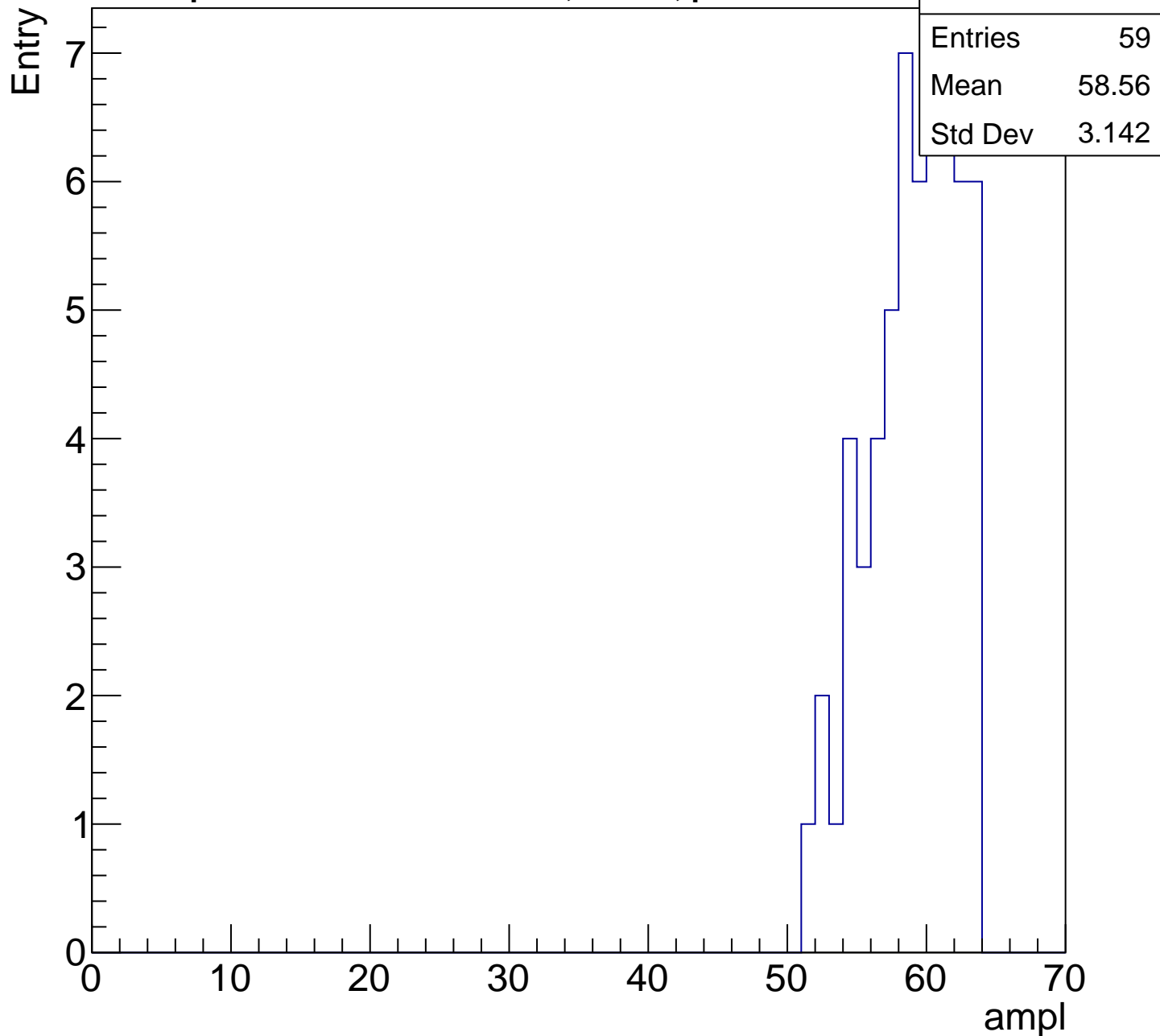
Entry

Entries	46
Mean	54.65
Std Dev	3.509



# B1L003S, U3-ch61, adc5

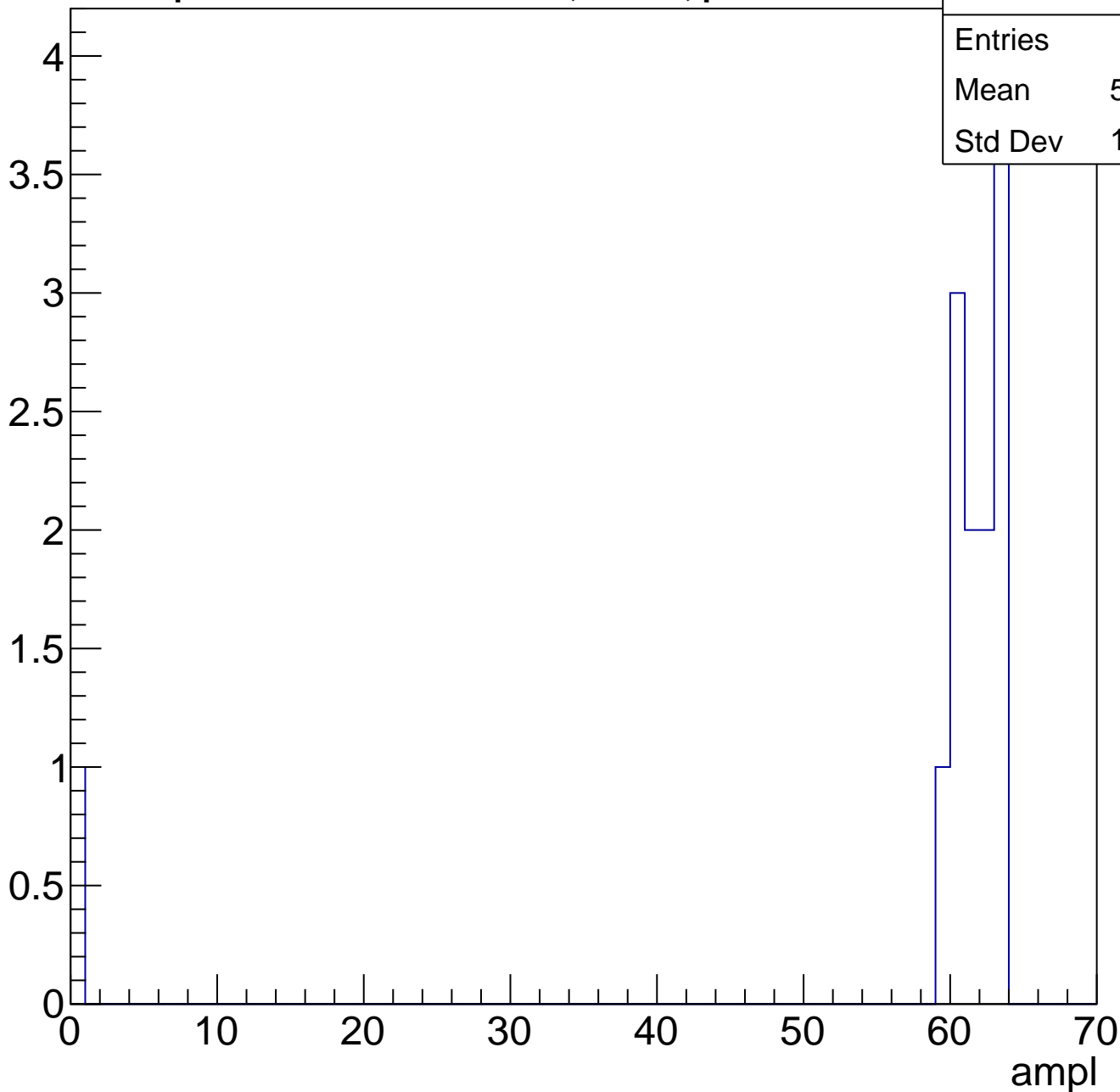
calib\_packv5\_042523\_0143.root, FC#13, port D2



# B1L003S, U3-ch61, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch61, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U3-ch62, adc0

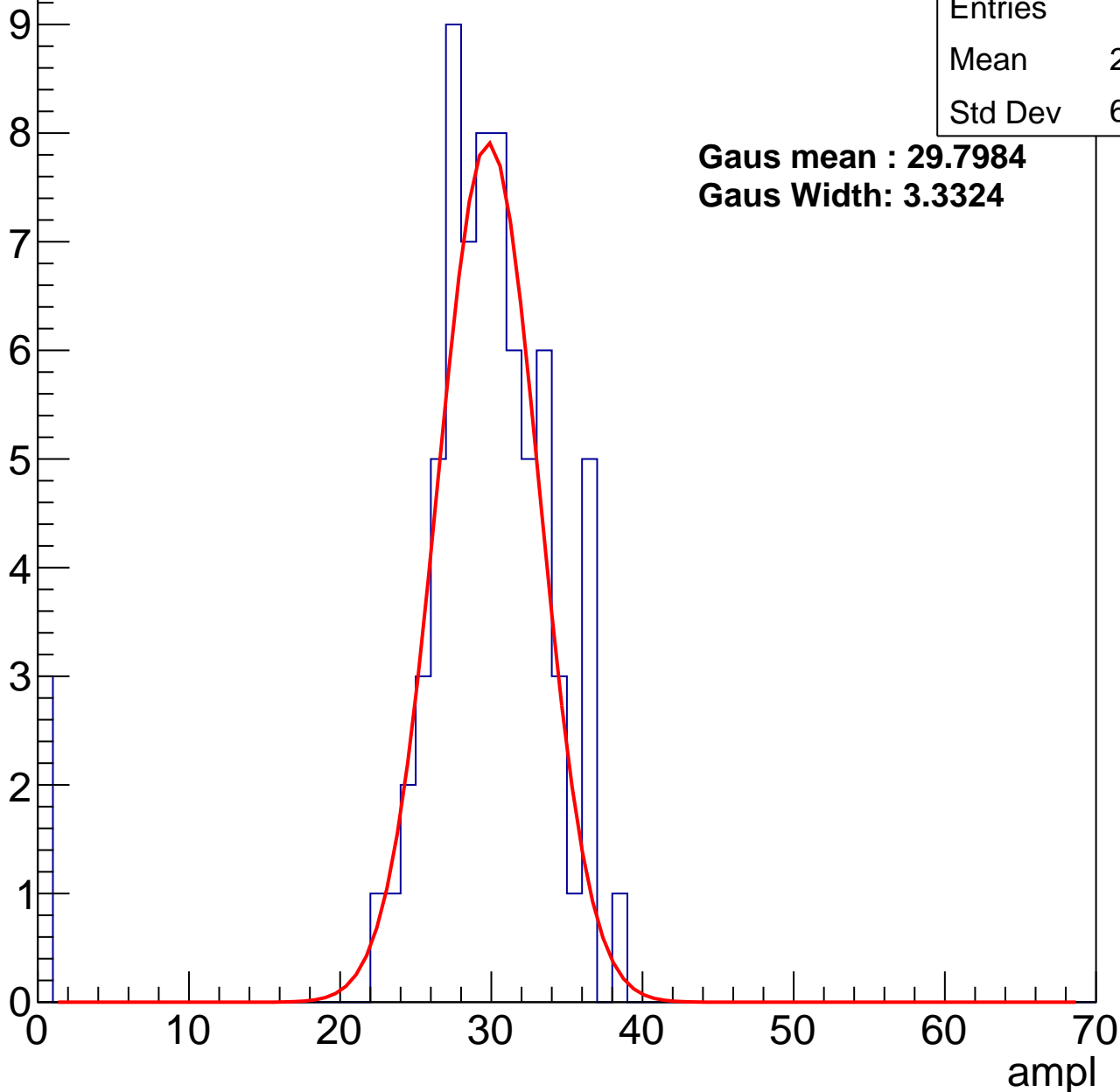
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	74
Mean	28.49
Std Dev	6.763

**Gaus mean : 29.7984**

**Gaus Width: 3.3324**



# B1L003S, U3-ch62, adc1

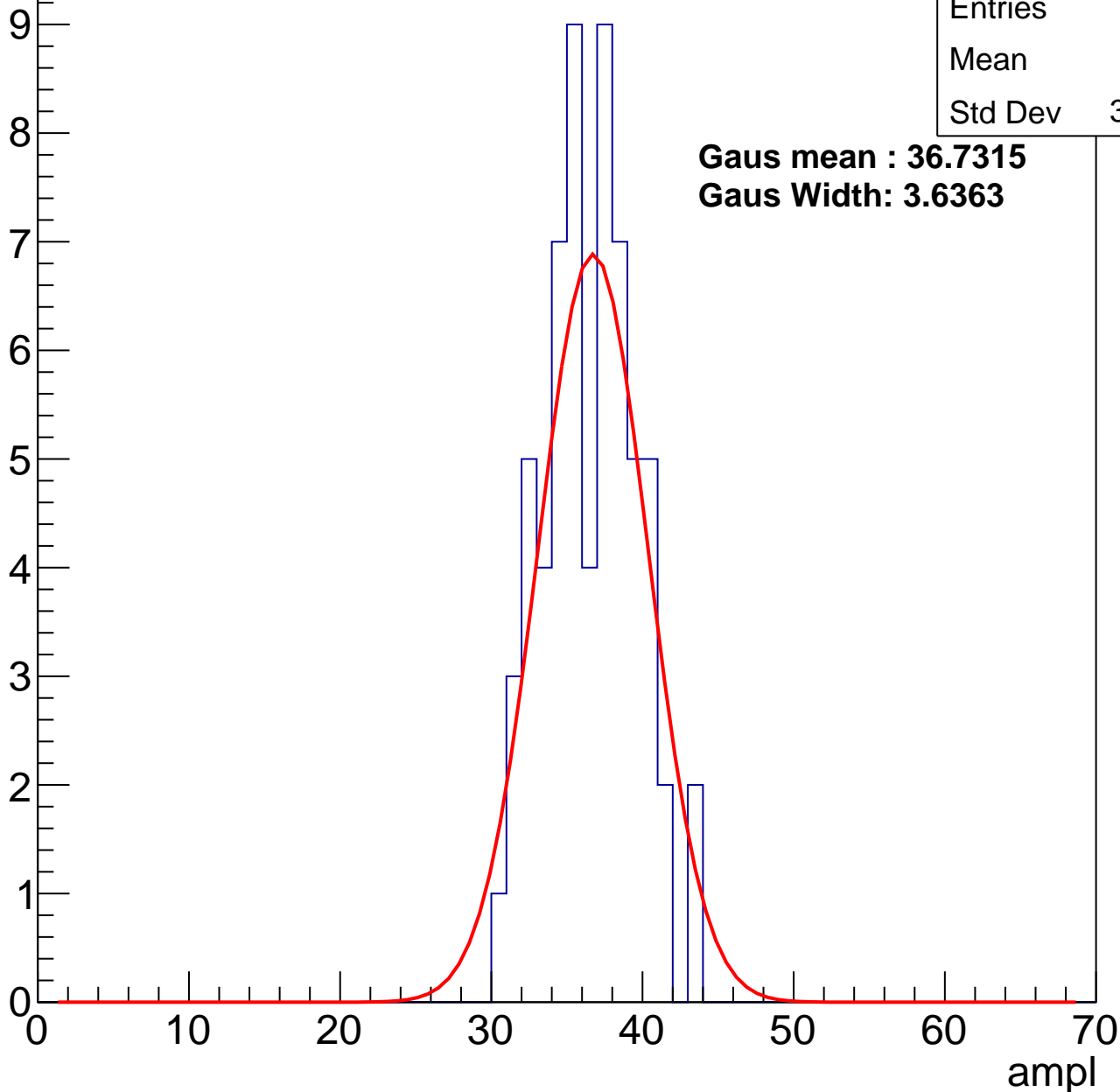
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	36.1
Std Dev	3.017

**Gaus mean : 36.7315**

**Gaus Width: 3.6363**



# B1L003S, U3-ch62, adc2

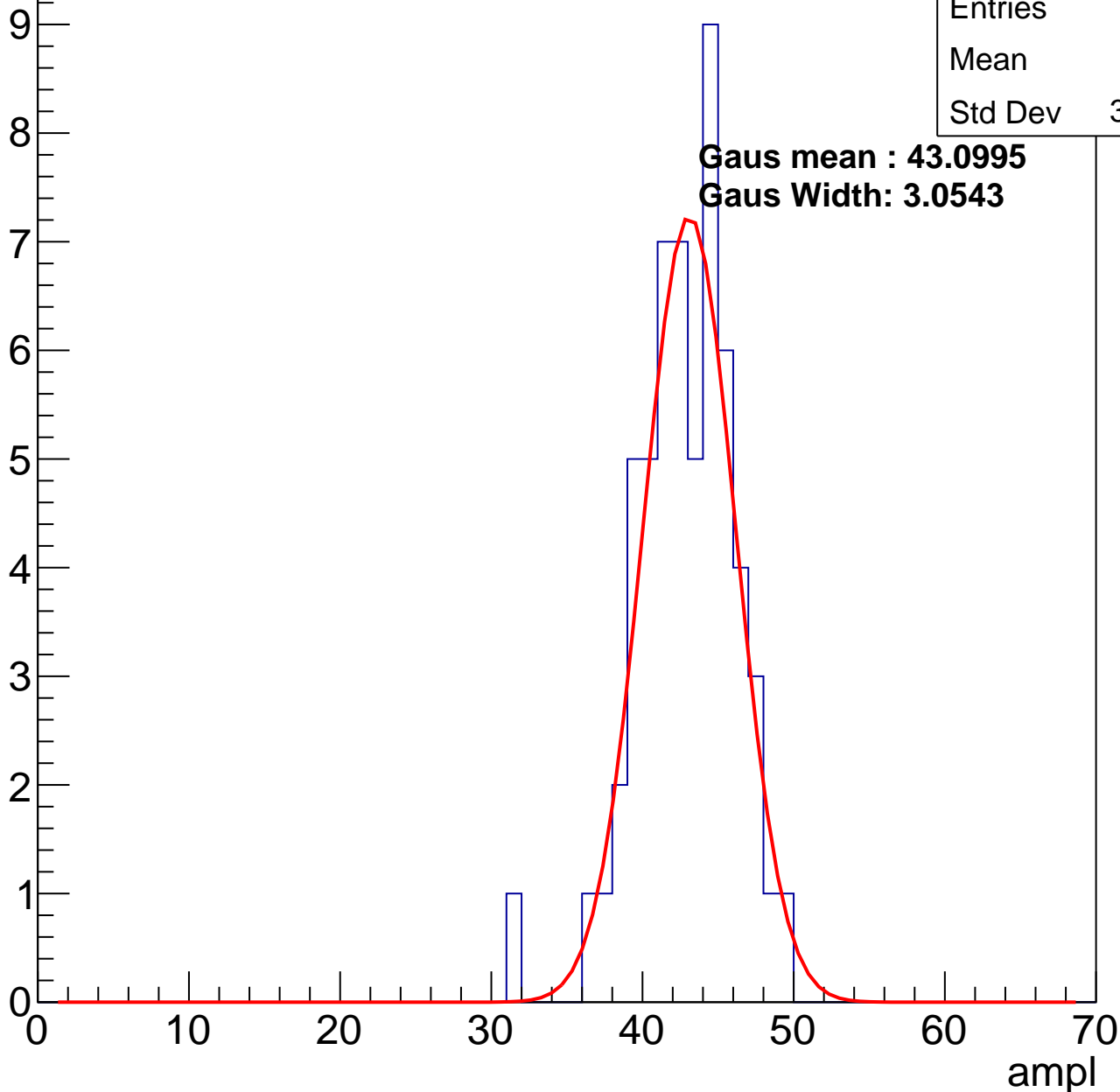
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	42.4
Std Dev	3.205

**Gaus mean : 43.0995**

**Gaus Width: 3.0543**

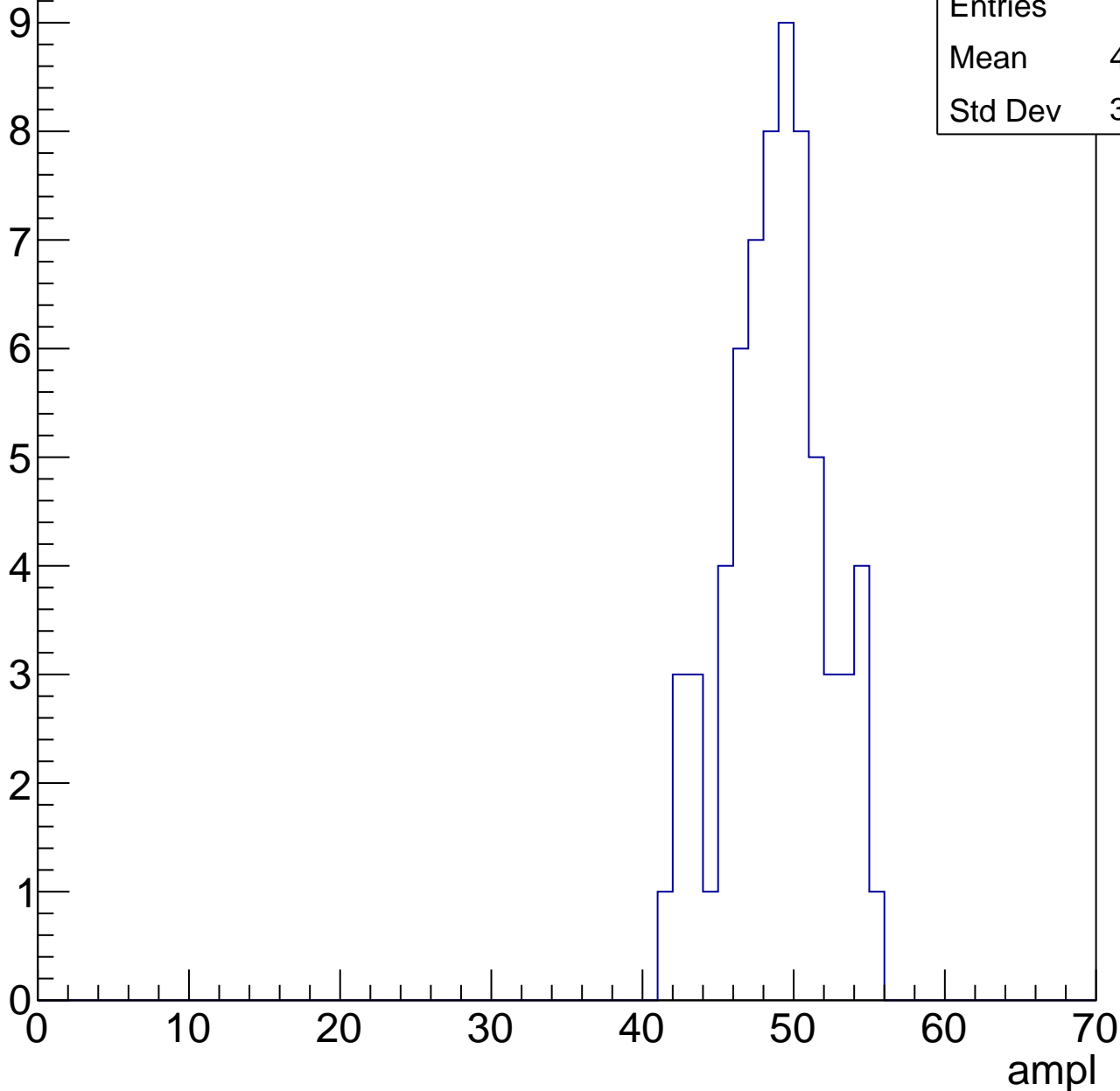


# B1L003S, U3-ch62, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	48.35
Std Dev	3.278

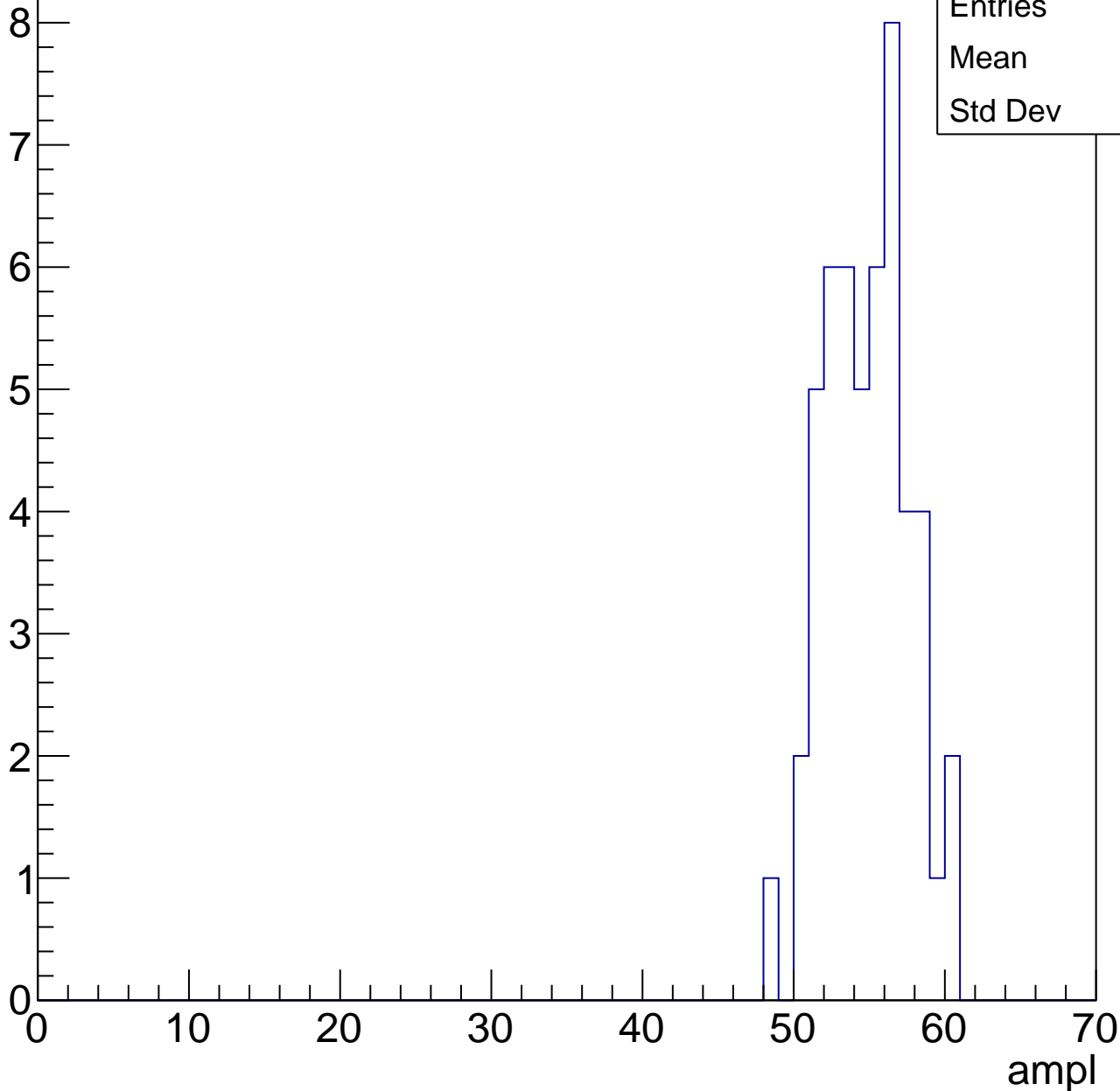


# B1L003S, U3-ch62, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	50
Mean	54.4
Std Dev	2.72

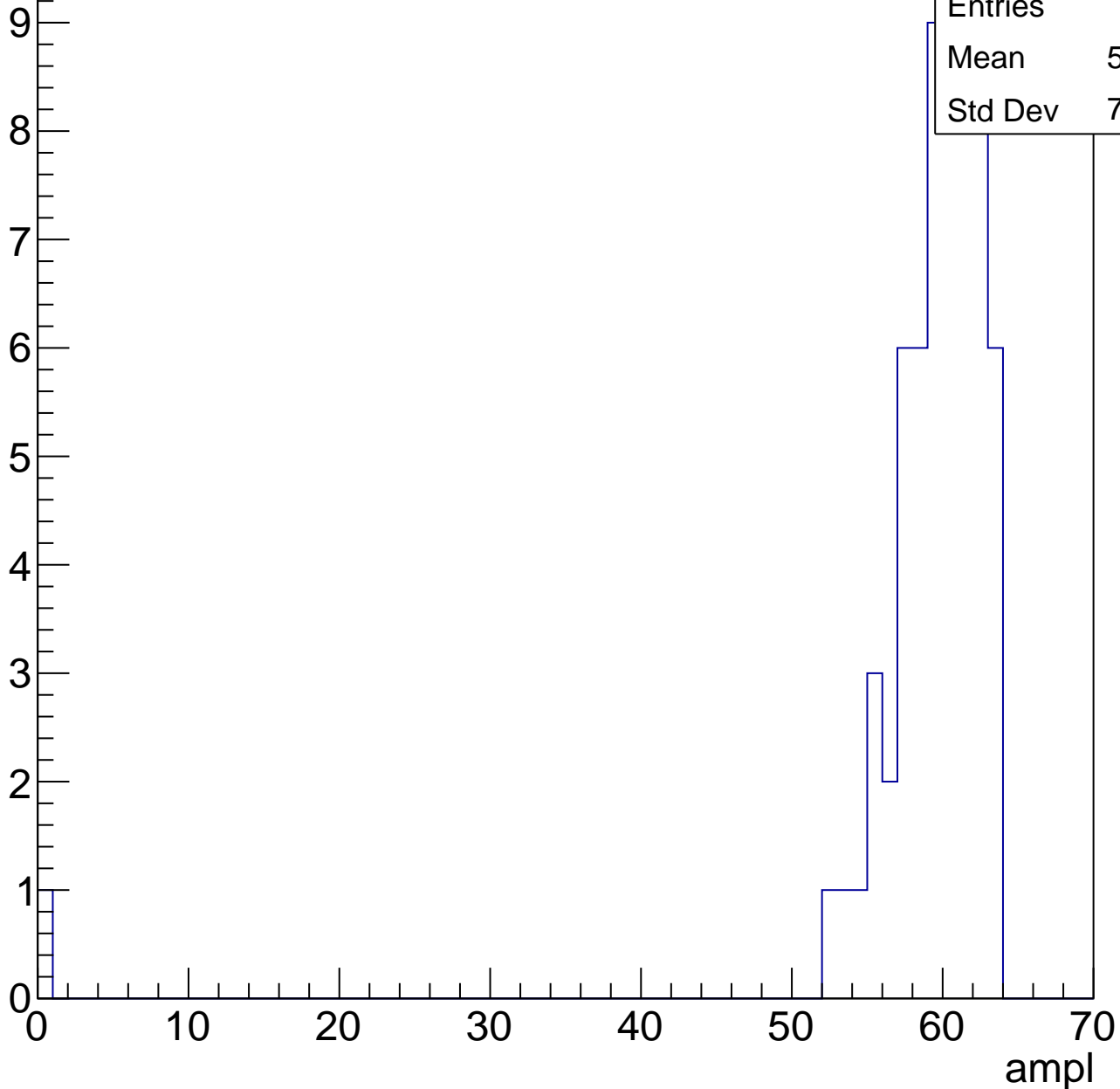


# B1L003S, U3-ch62, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

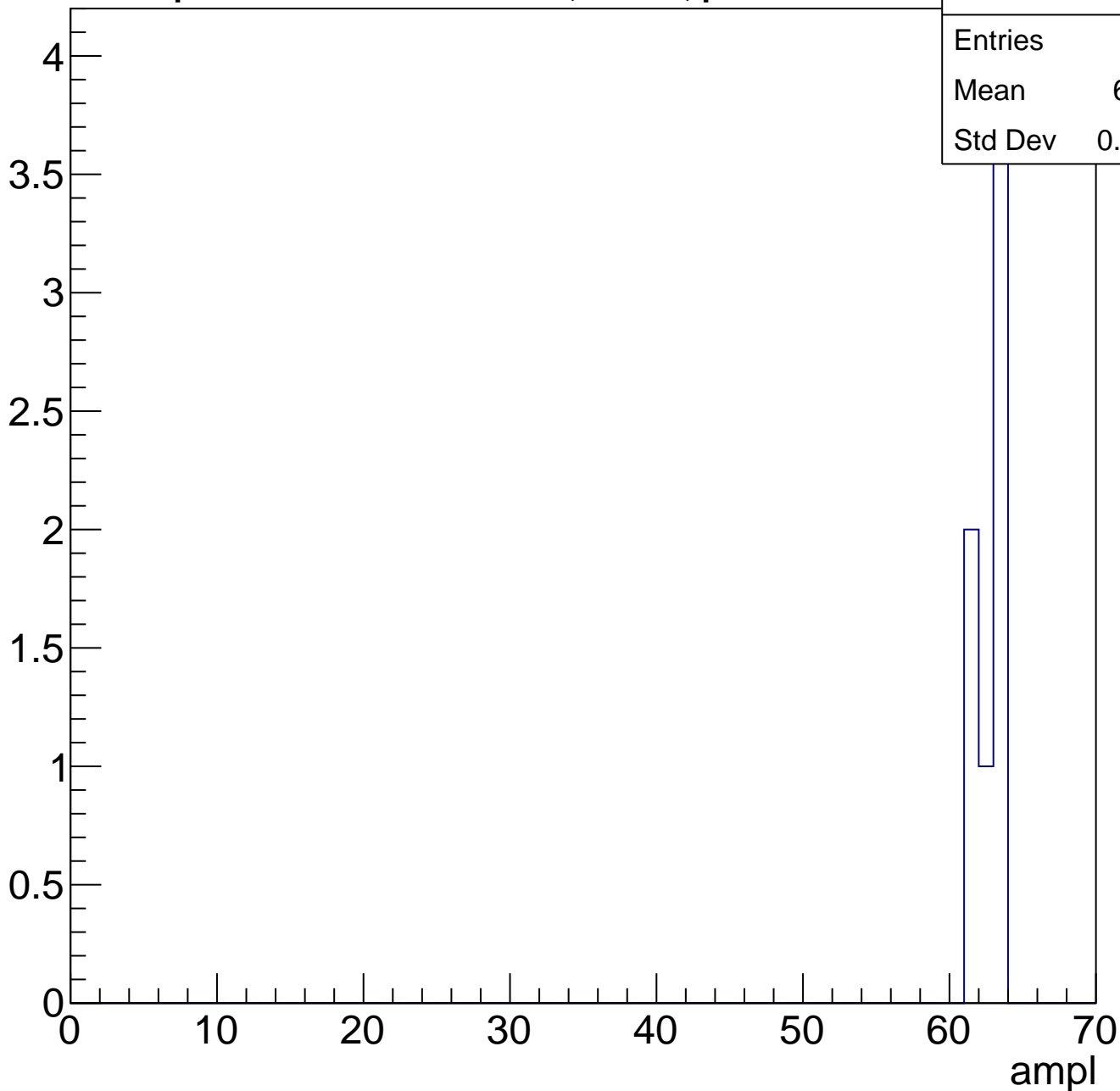
Entries	61
Mean	58.38
Std Dev	7.976



# B1L003S, U3-ch62, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch62, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	22
Std Dev	0

# B1L003S, U3-ch63, adc0

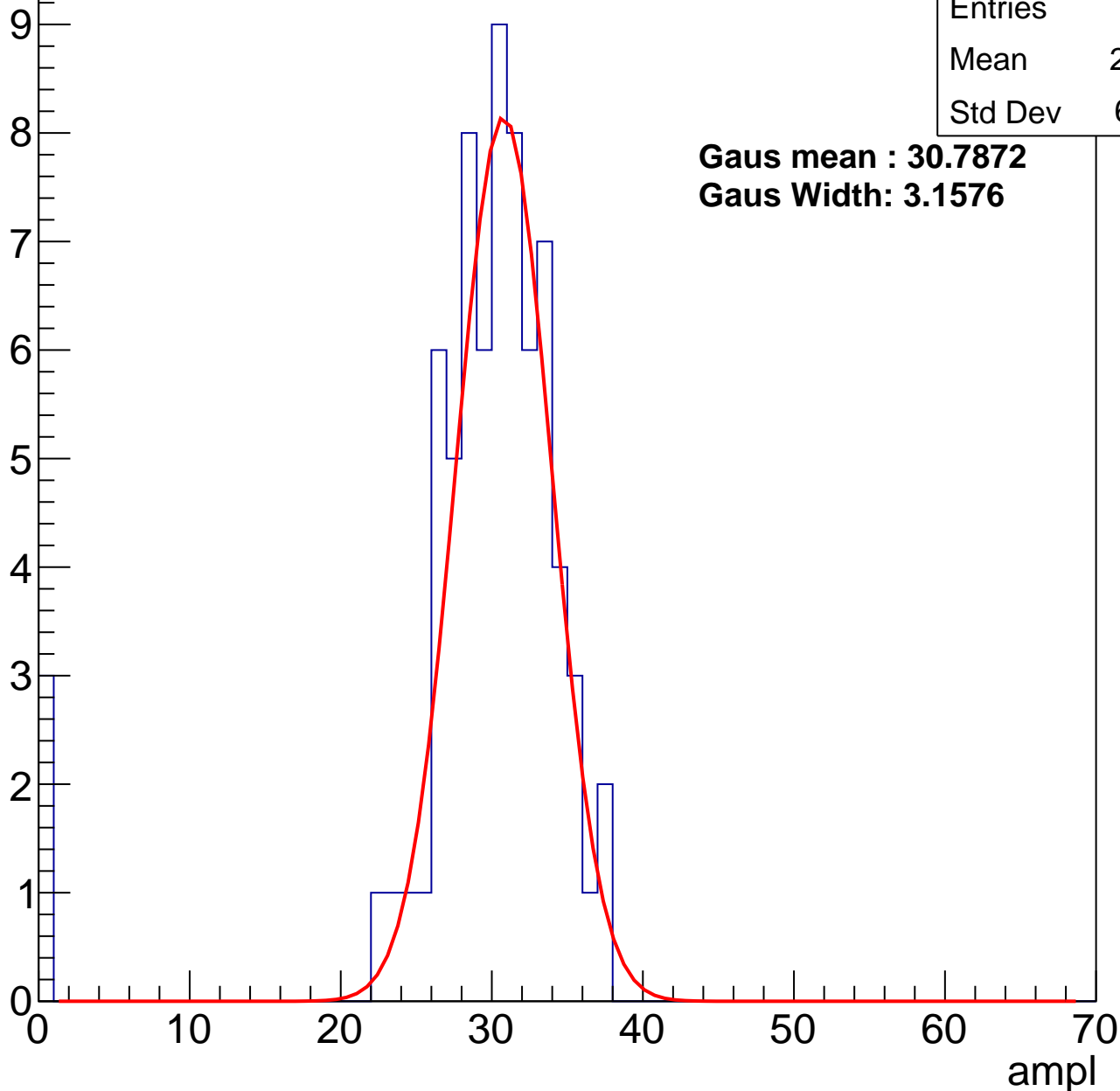
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	72
Mean	28.82
Std Dev	6.791

**Gaus mean : 30.7872**

**Gaus Width: 3.1576**



# B1L003S, U3-ch63, adc1

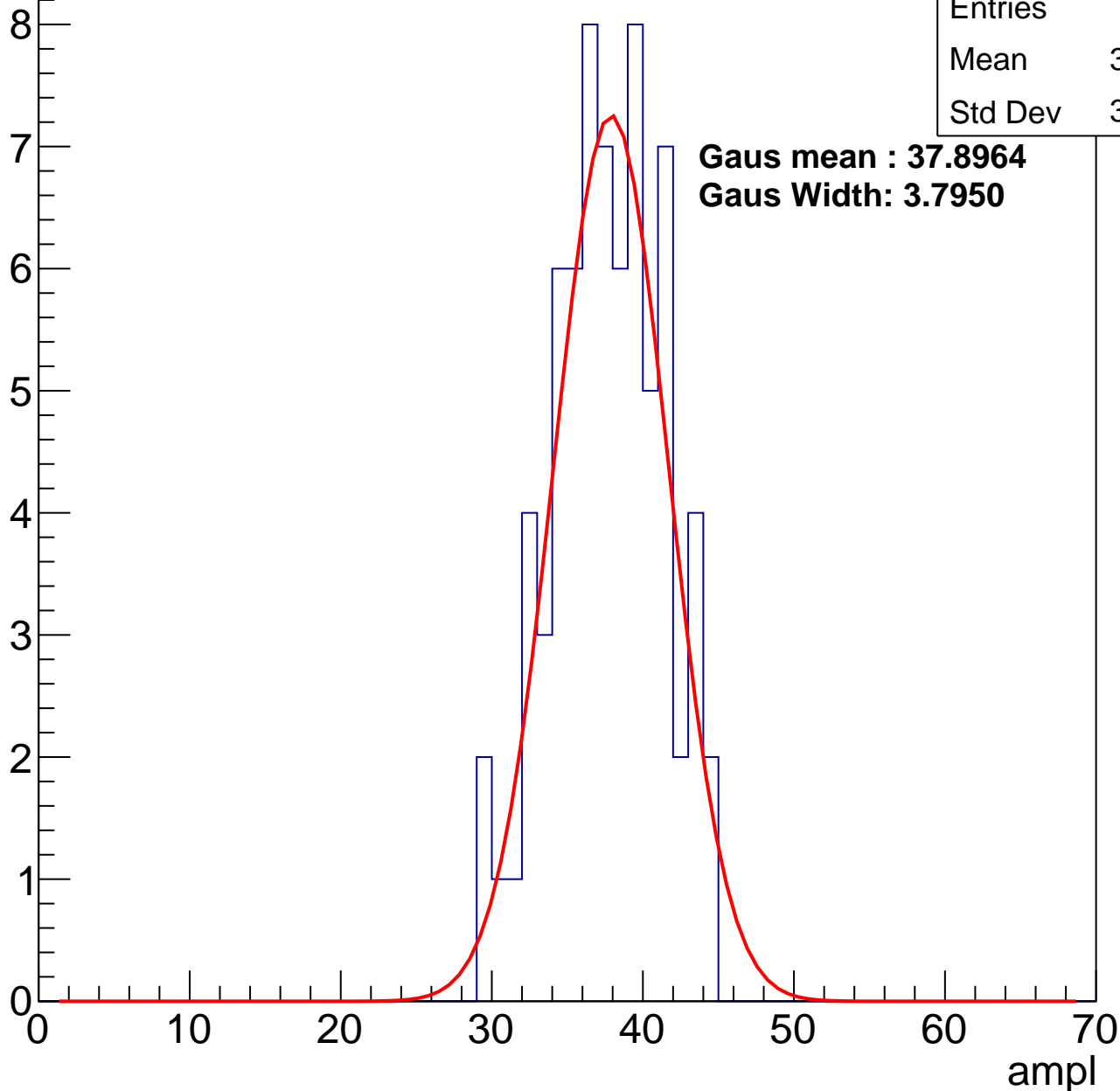
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	72
Mean	37.19
Std Dev	3.596

**Gaus mean : 37.8964**

**Gaus Width: 3.7950**



# B1L003S, U3-ch63, adc2

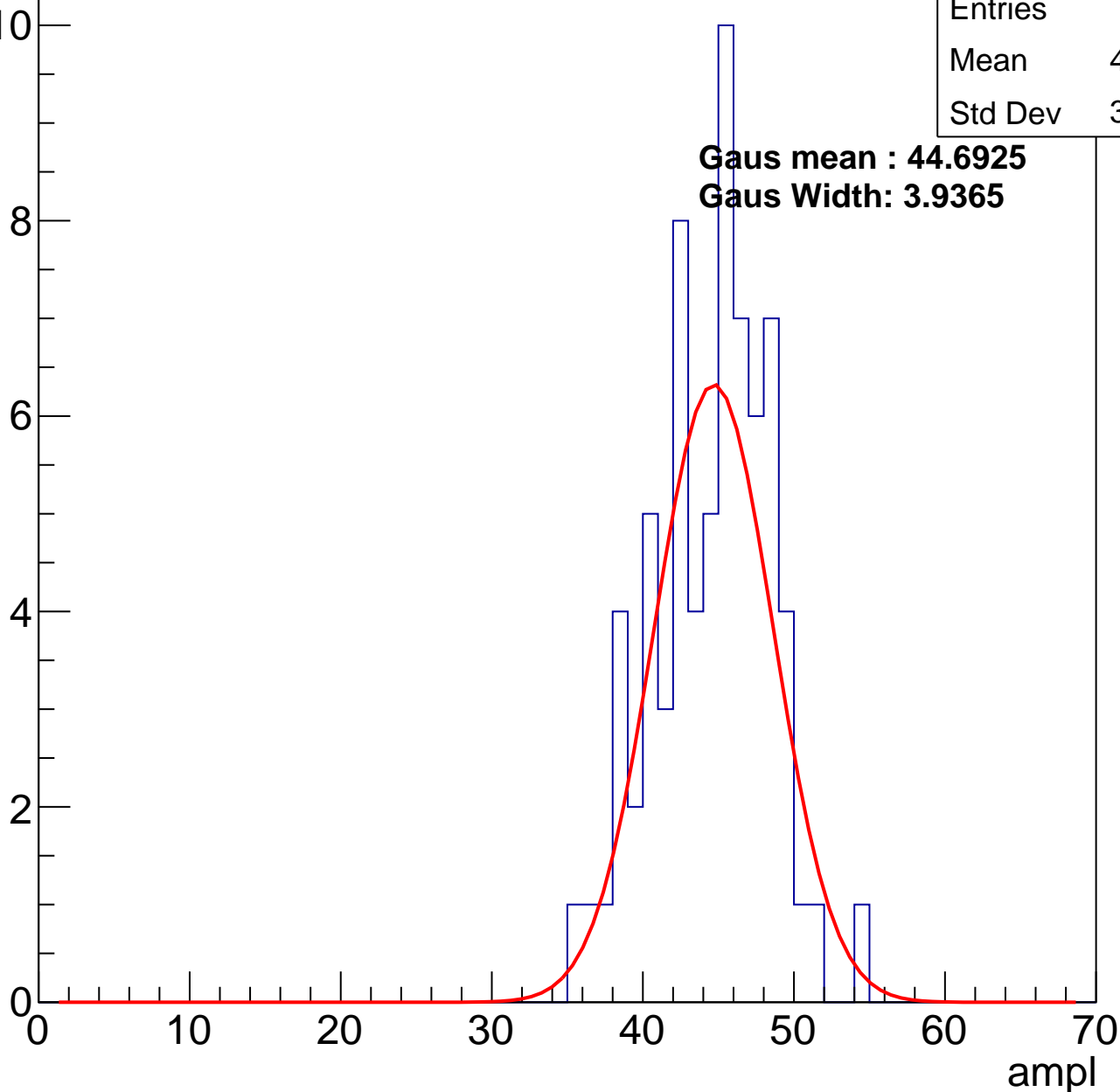
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	71
Mean	44.08
Std Dev	3.789

**Gaus mean : 44.6925**

**Gaus Width: 3.9365**

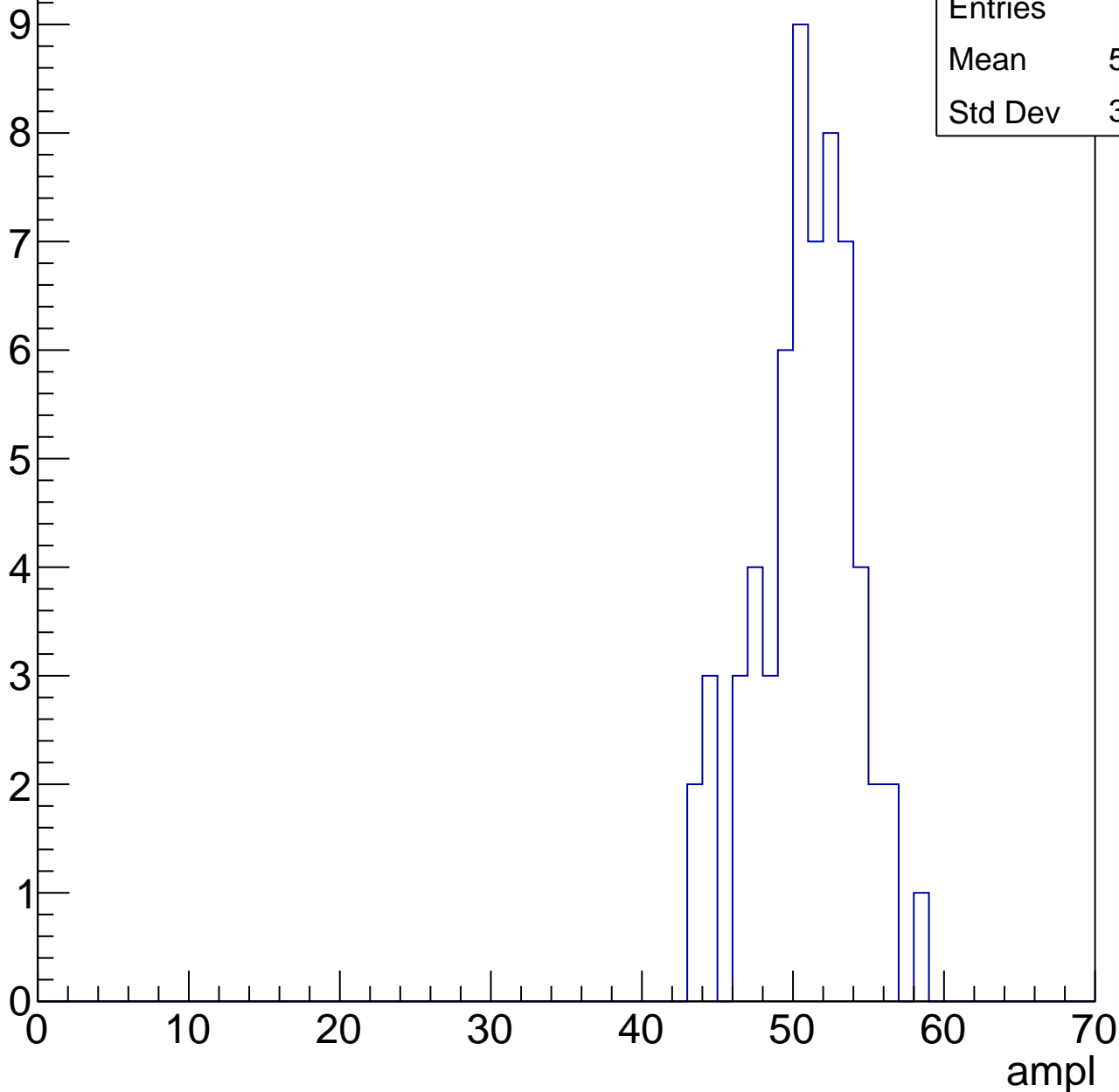


# B1L003S, U3-ch63, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

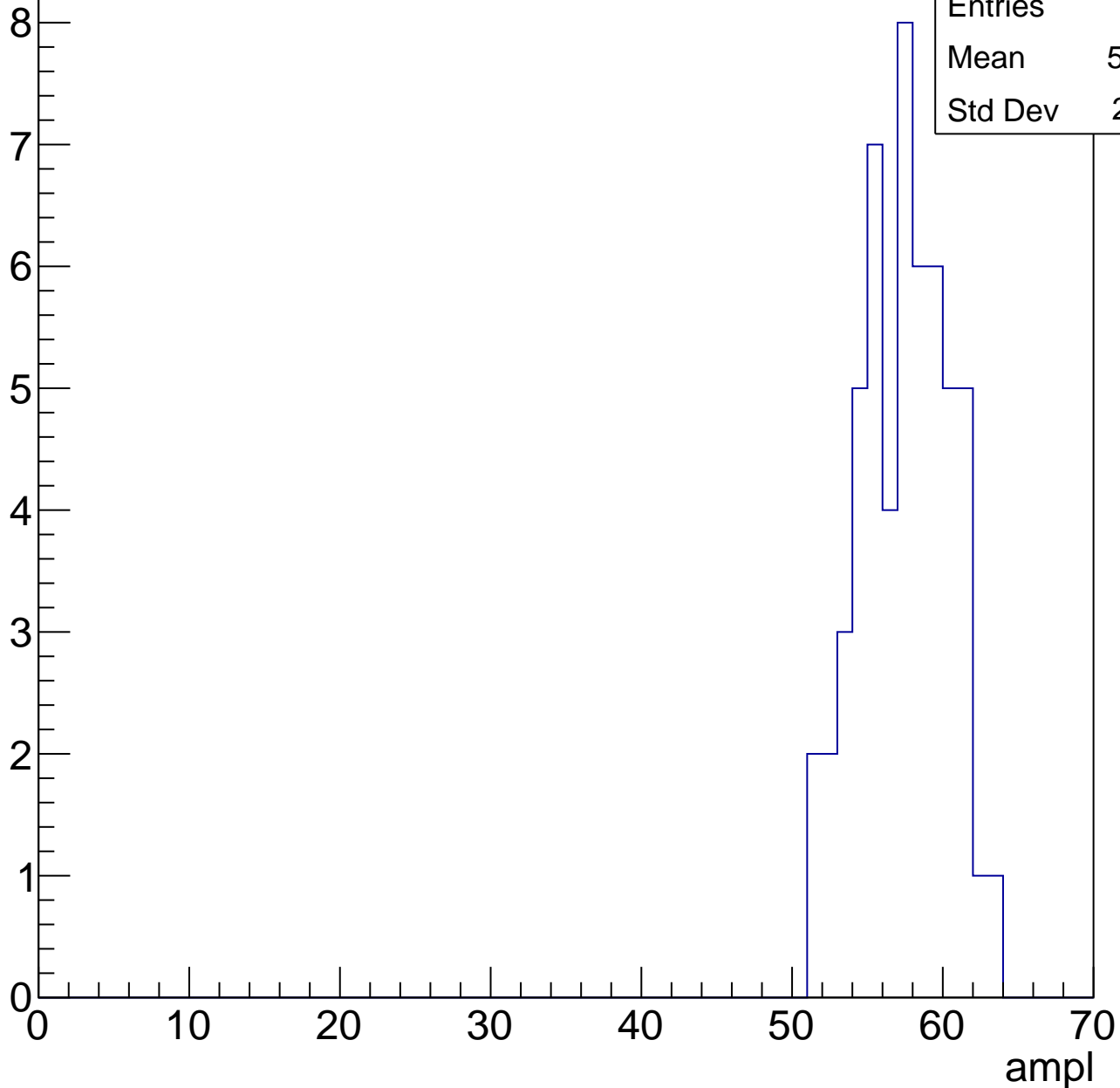
Entries	61
Mean	50.36
Std Dev	3.269



# B1L003S, U3-ch63, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

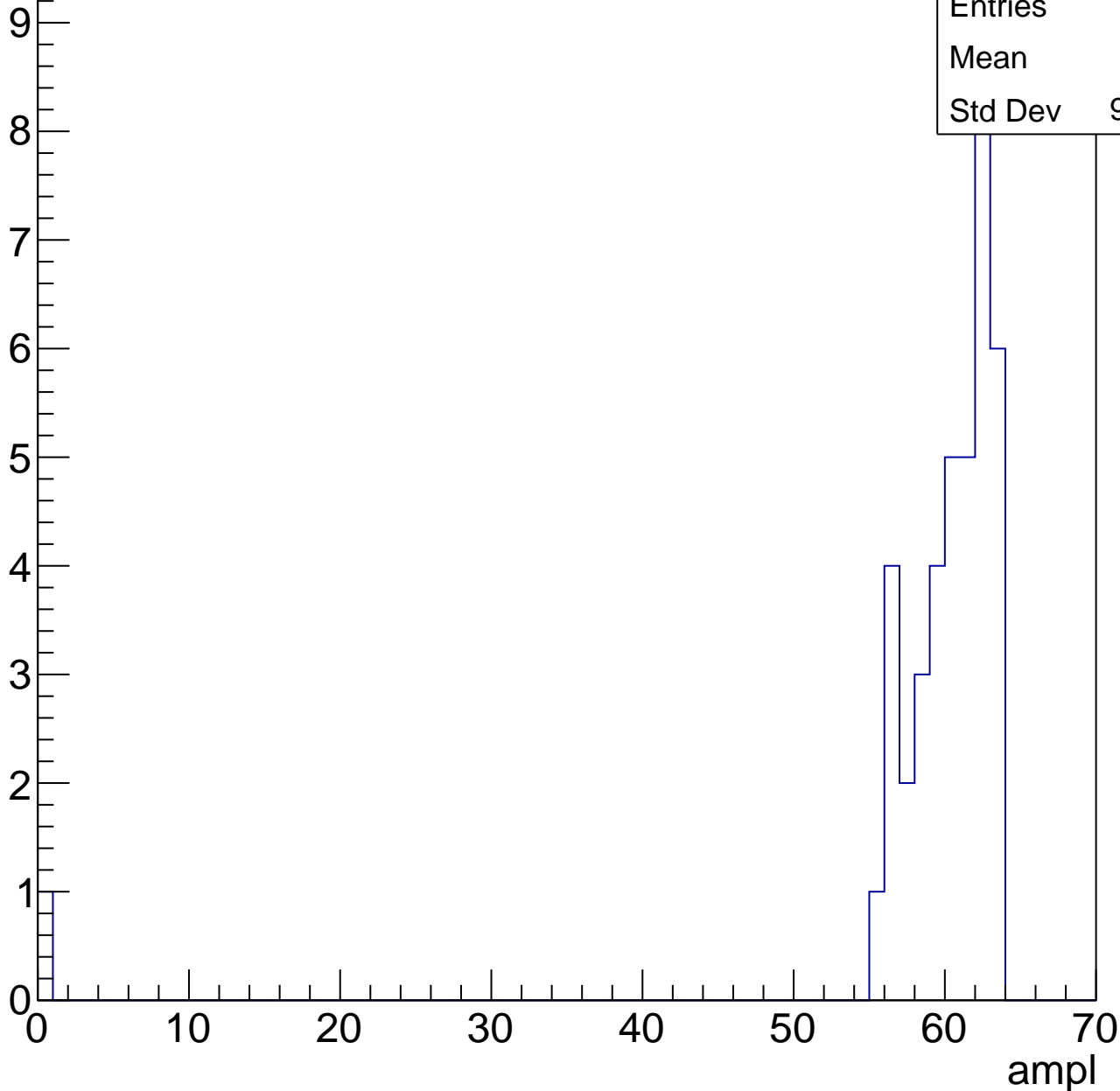


# B1L003S, U3-ch63, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	40
Mean	58.6
Std Dev	9.669



# B1L003S, U3-ch63, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch63, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U3-ch64, adc0

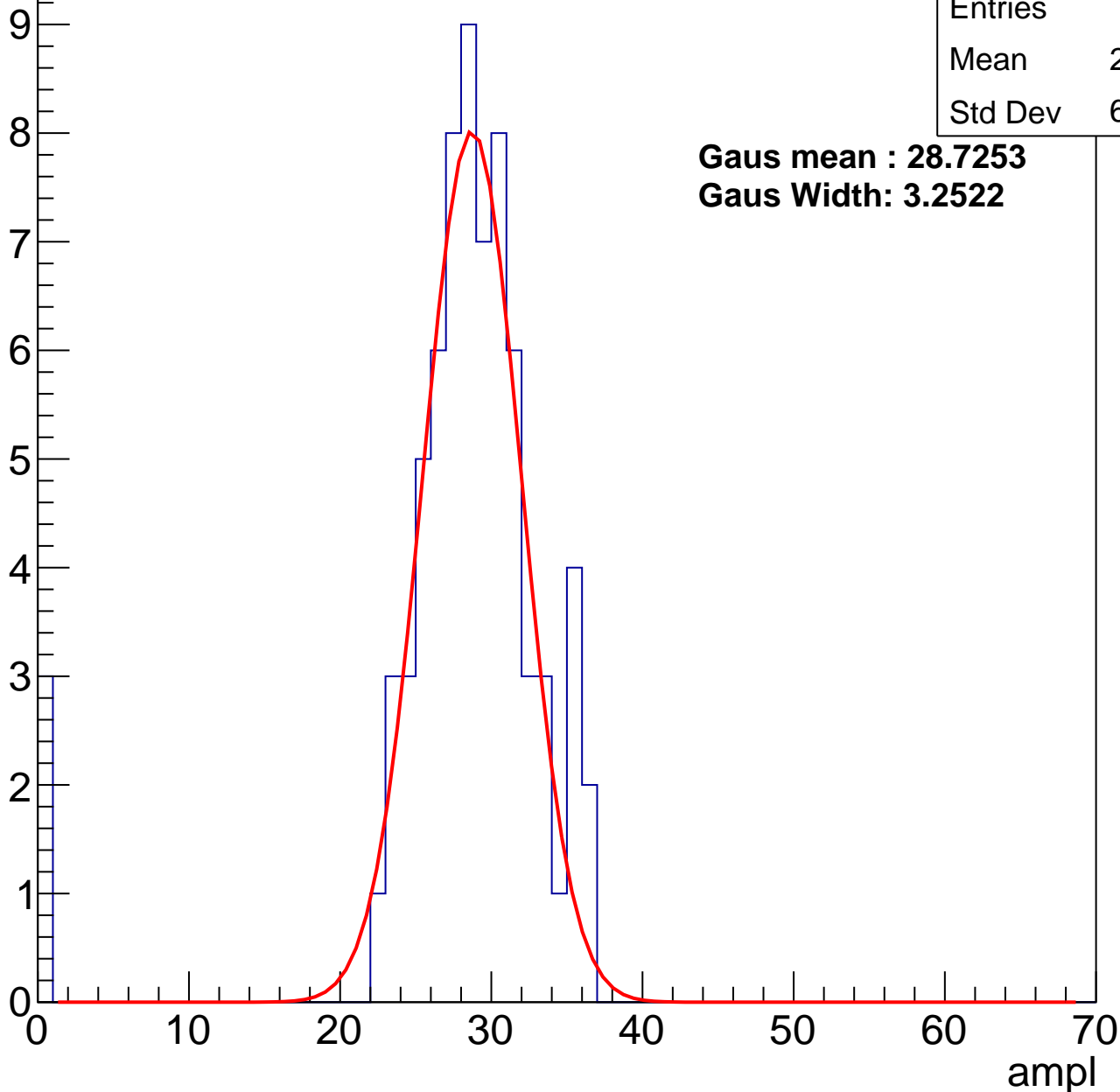
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	72
Mean	27.53
Std Dev	6.612

**Gaus mean : 28.7253**

**Gaus Width: 3.2522**



# B1L003S, U3-ch64, adc1

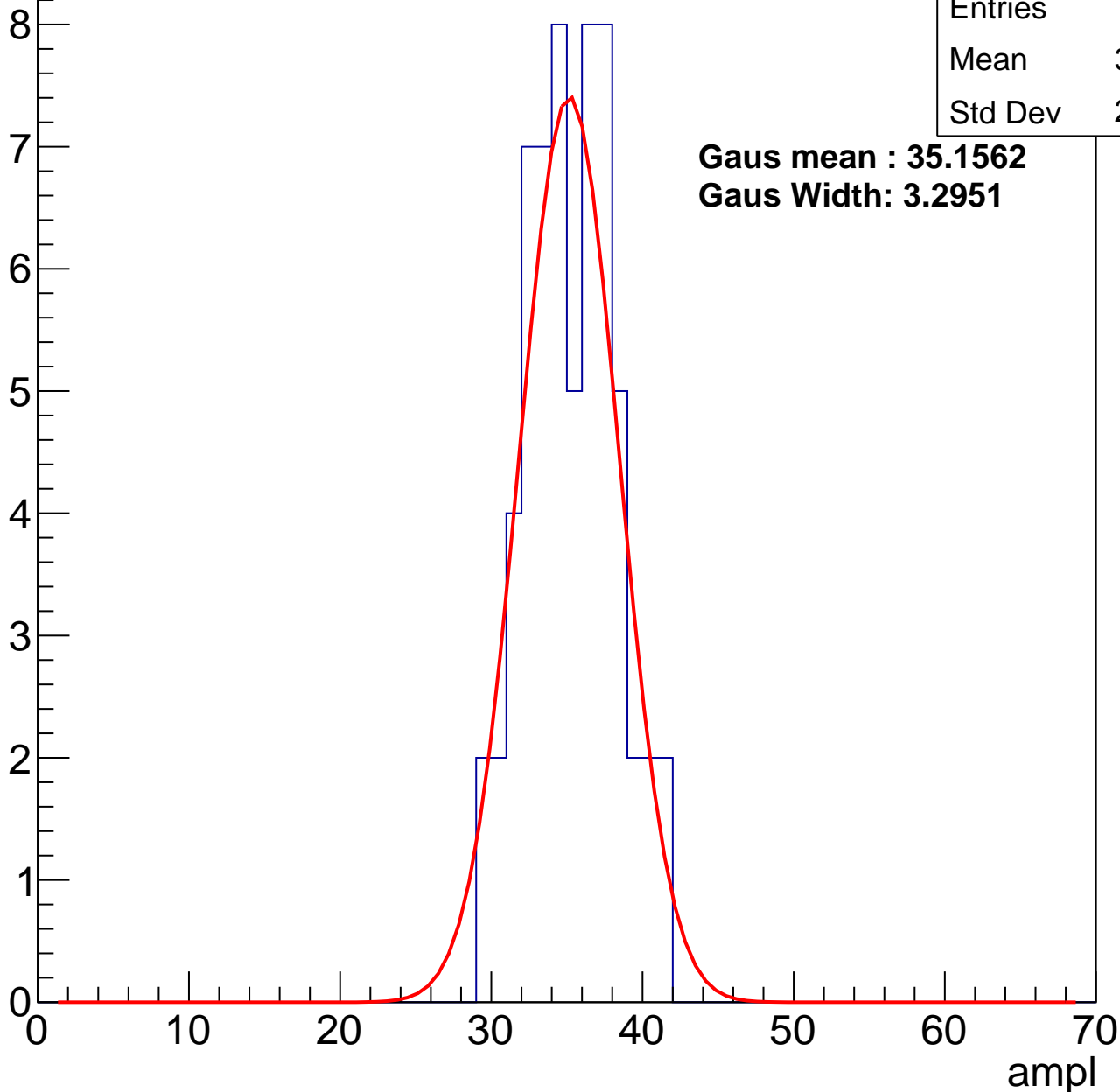
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	34.81
Std Dev	2.901

**Gaus mean : 35.1562**

**Gaus Width: 3.2951**



# B1L003S, U3-ch64, adc2

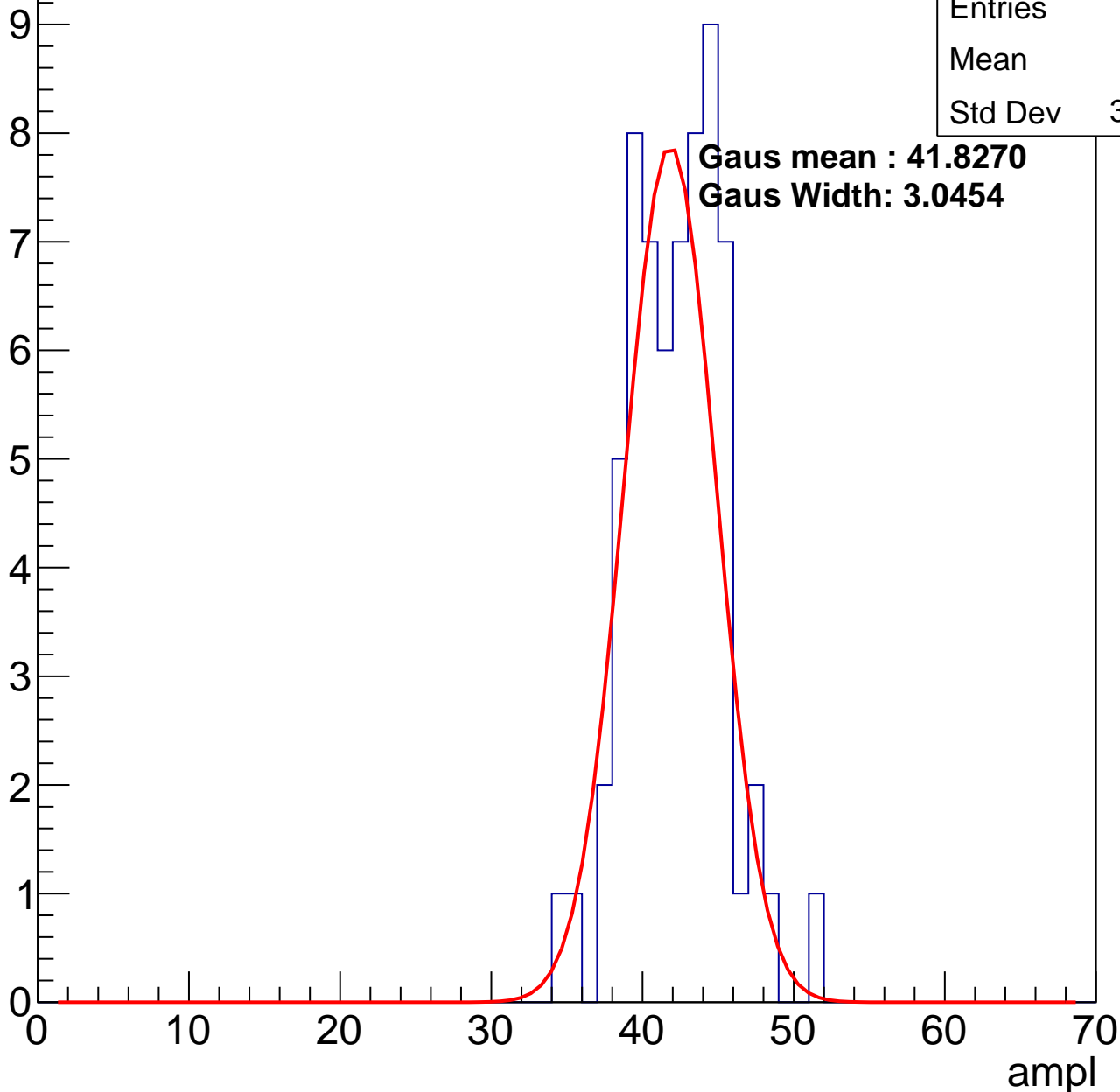
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	41.8
Std Dev	3.105

**Gaus mean : 41.8270**

**Gaus Width: 3.0454**

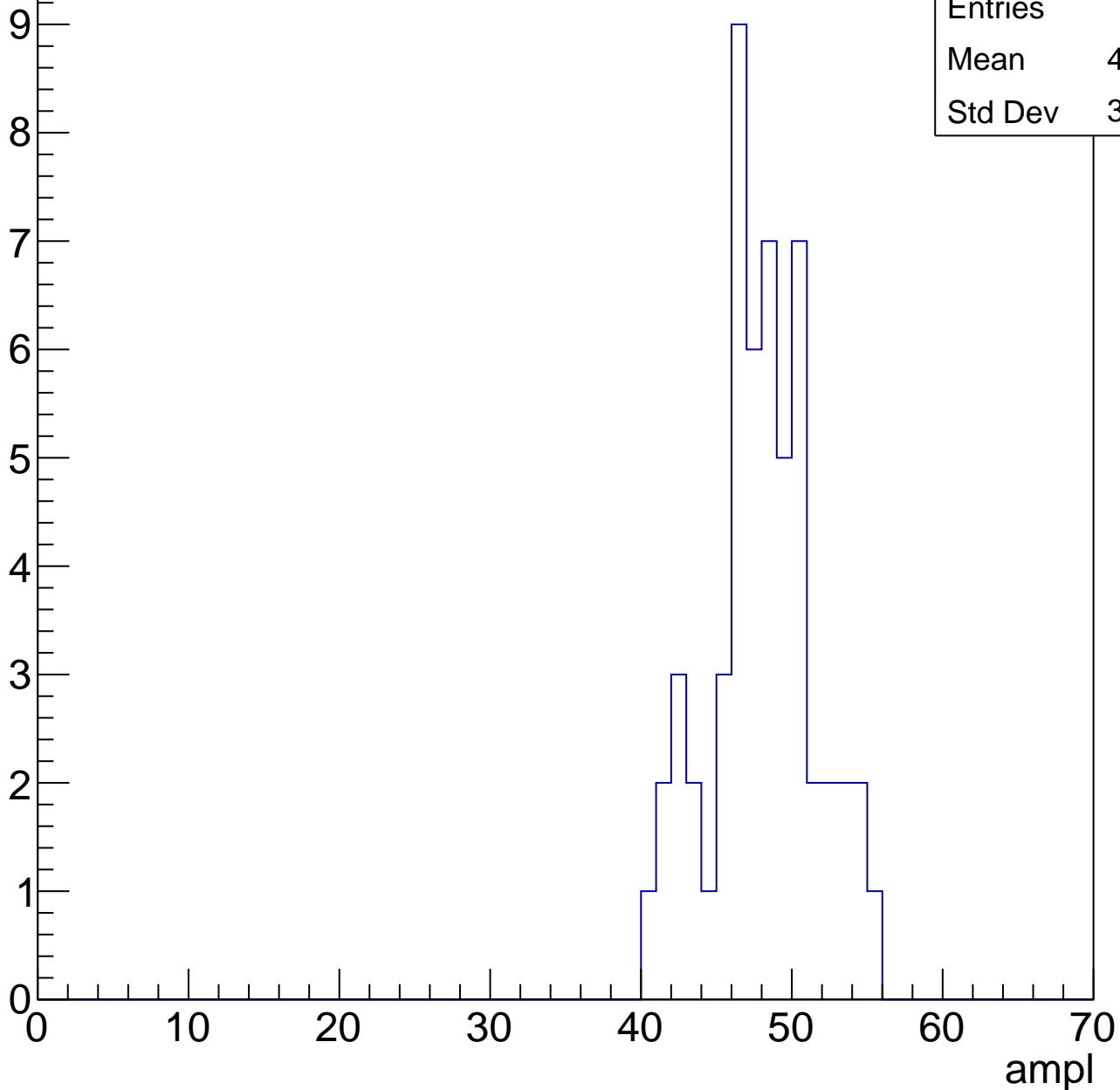


# B1L003S, U3-ch64, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

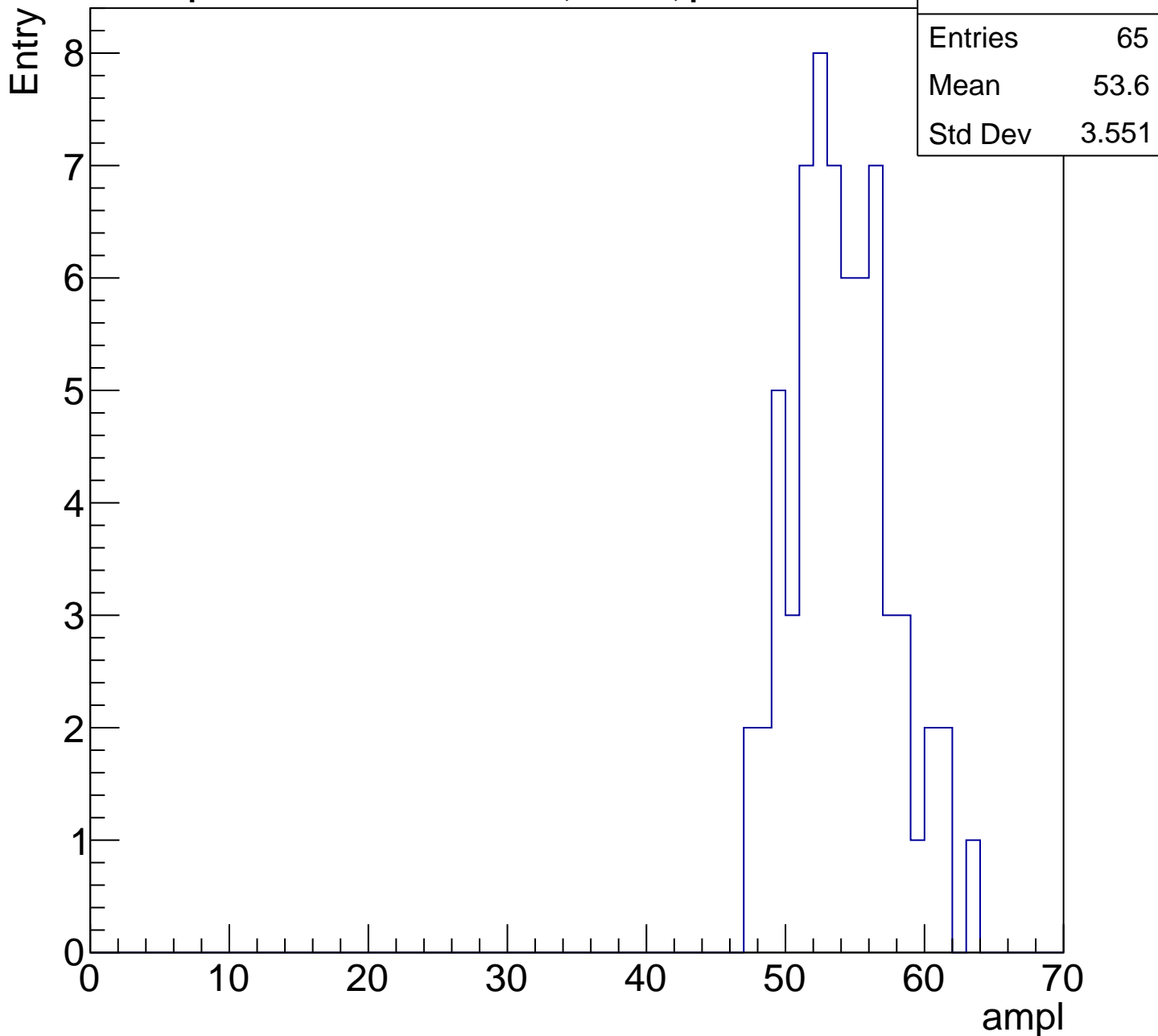
Entry

Entries	55
Mean	47.55
Std Dev	3.432



# B1L003S, U3-ch64, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

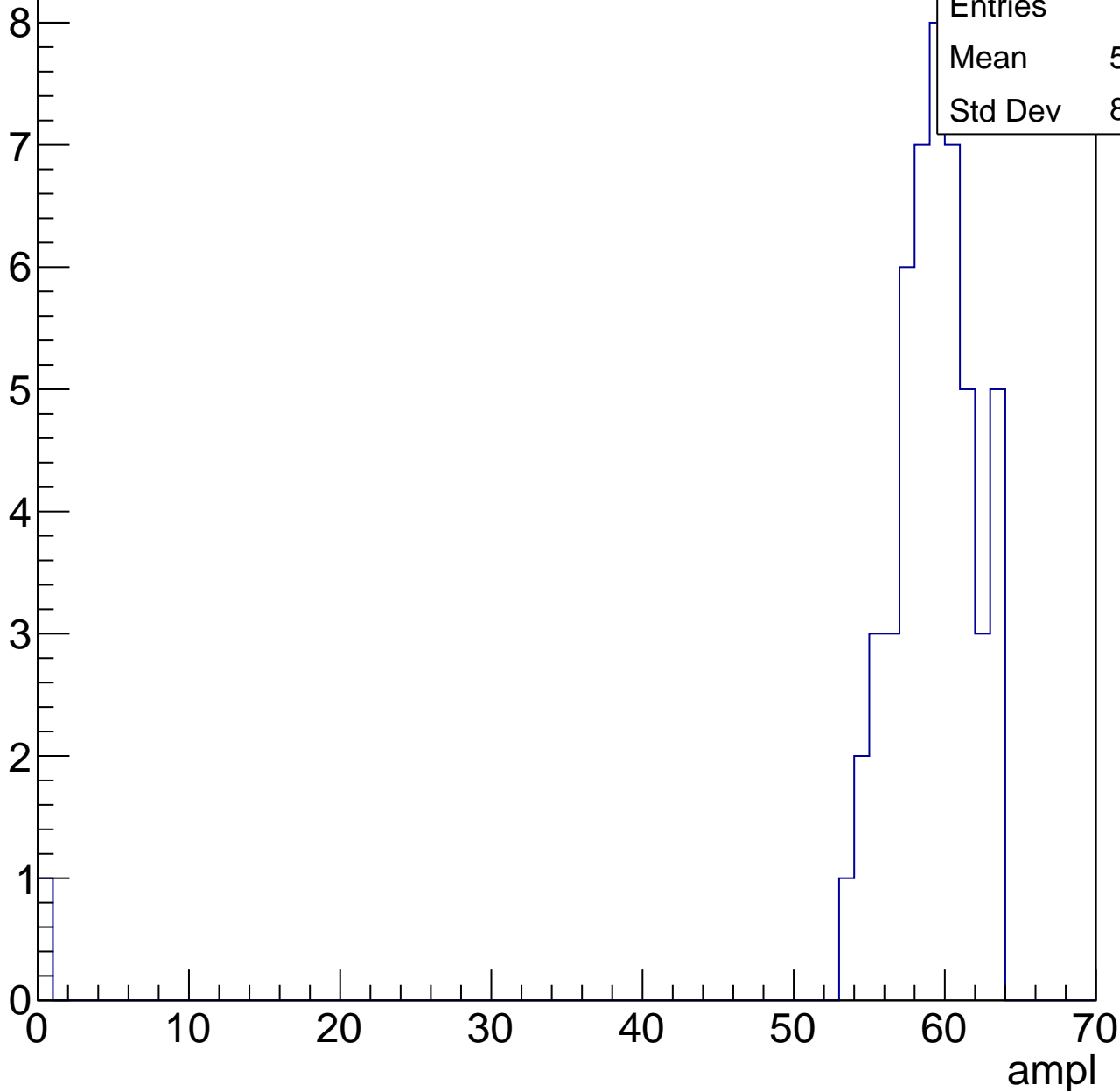


# B1L003S, U3-ch64, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	51
Mean	57.65
Std Dev	8.533

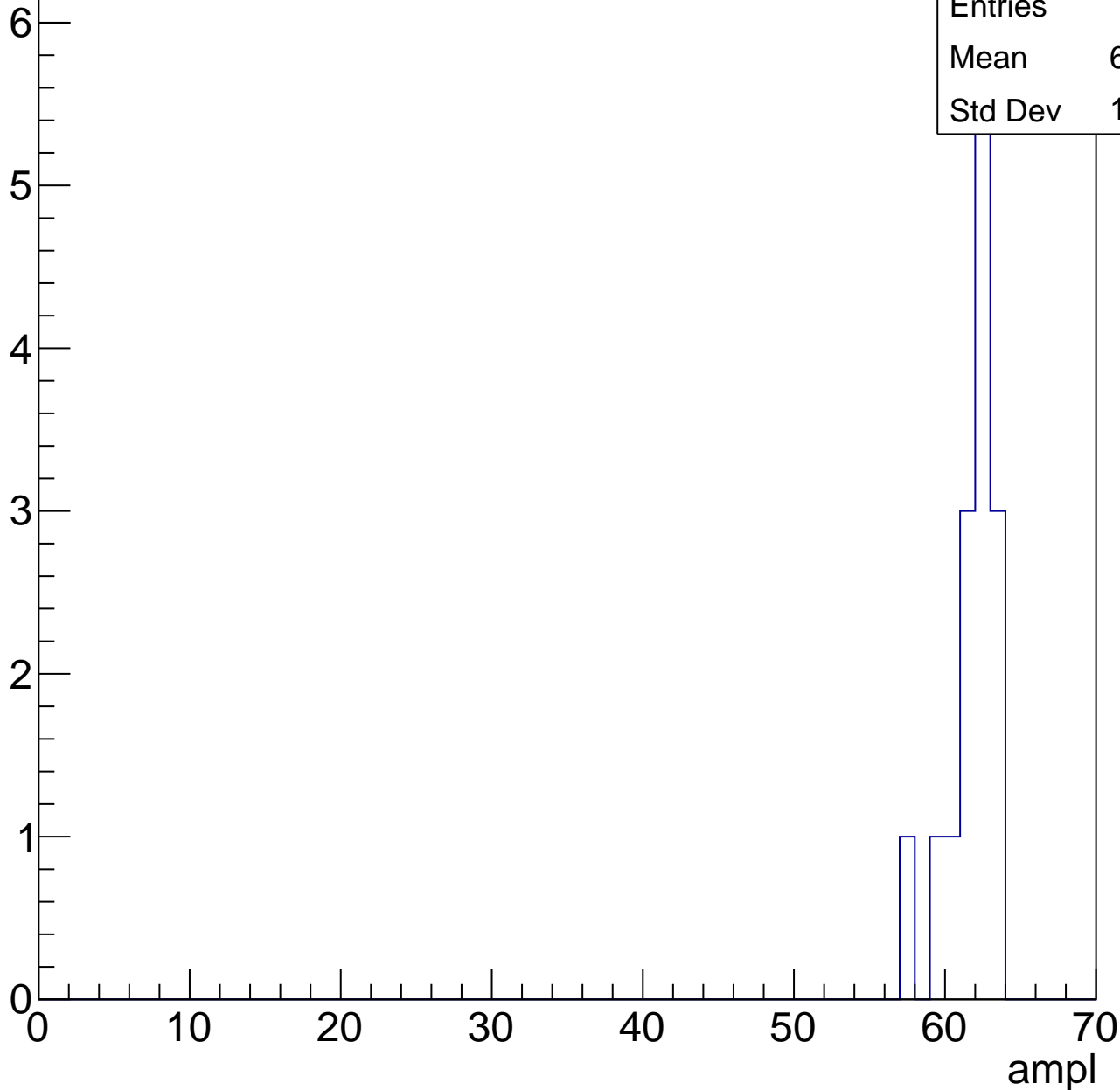


# B1L003S, U3-ch64, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	15
Mean	61.33
Std Dev	1.578

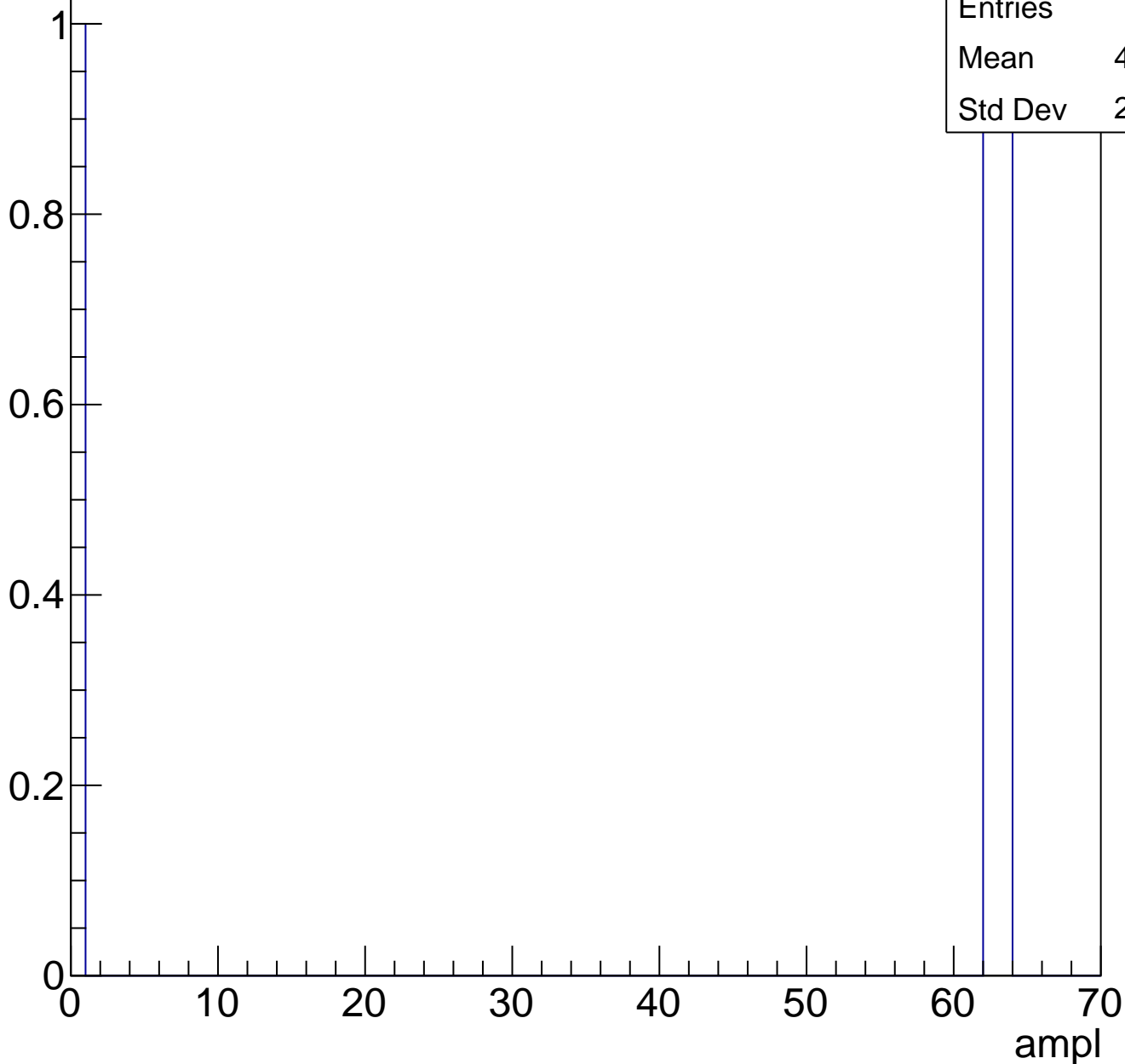




# B1L003S, U3-ch64, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U3-ch65, adc0

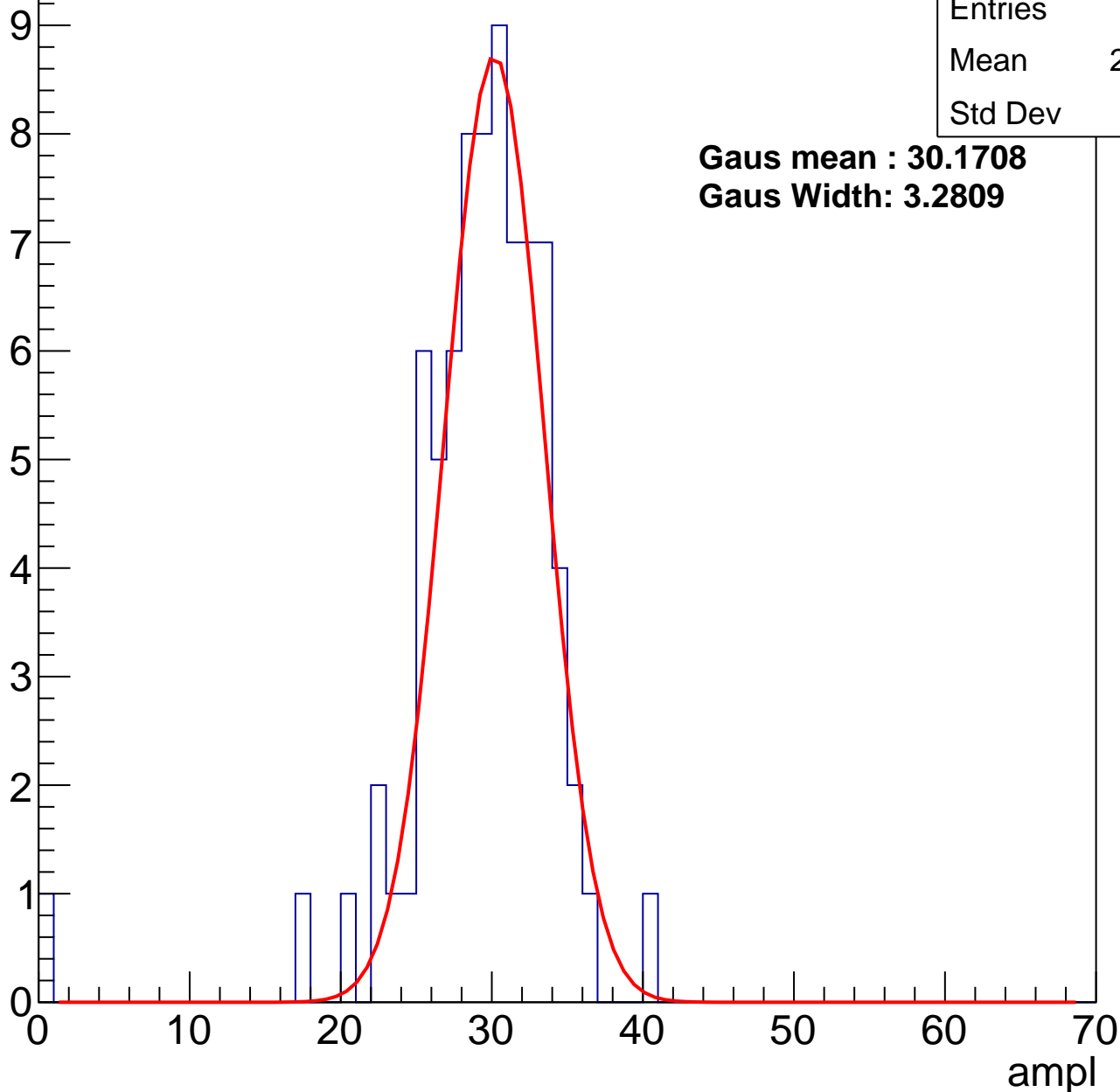
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	78
Mean	28.85
Std Dev	5

**Gaus mean : 30.1708**

**Gaus Width: 3.2809**



# B1L003S, U3-ch65, adc1

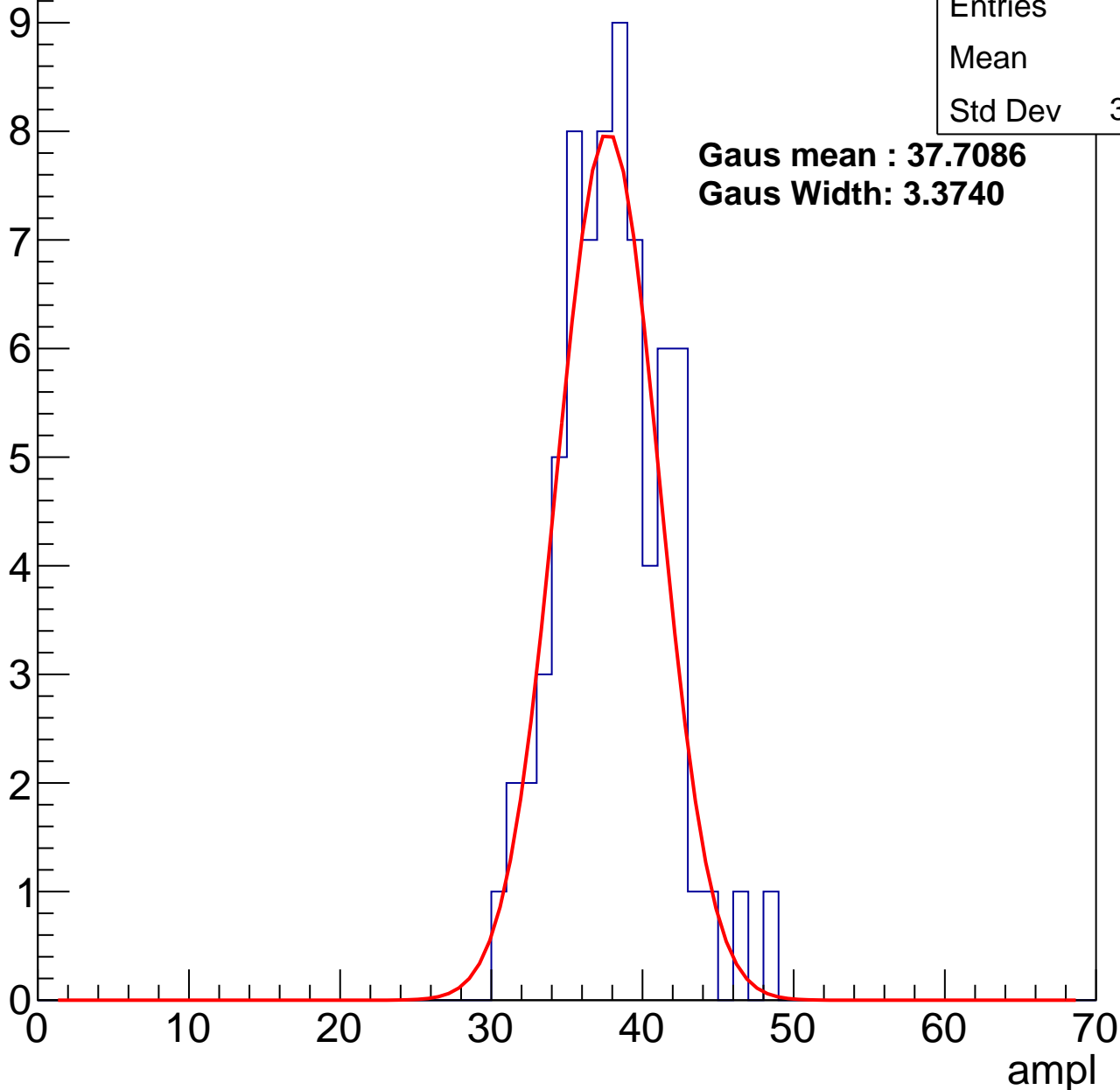
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	72
Mean	37.6
Std Dev	3.503

**Gaus mean : 37.7086**

**Gaus Width: 3.3740**



# B1L003S, U3-ch65, adc2

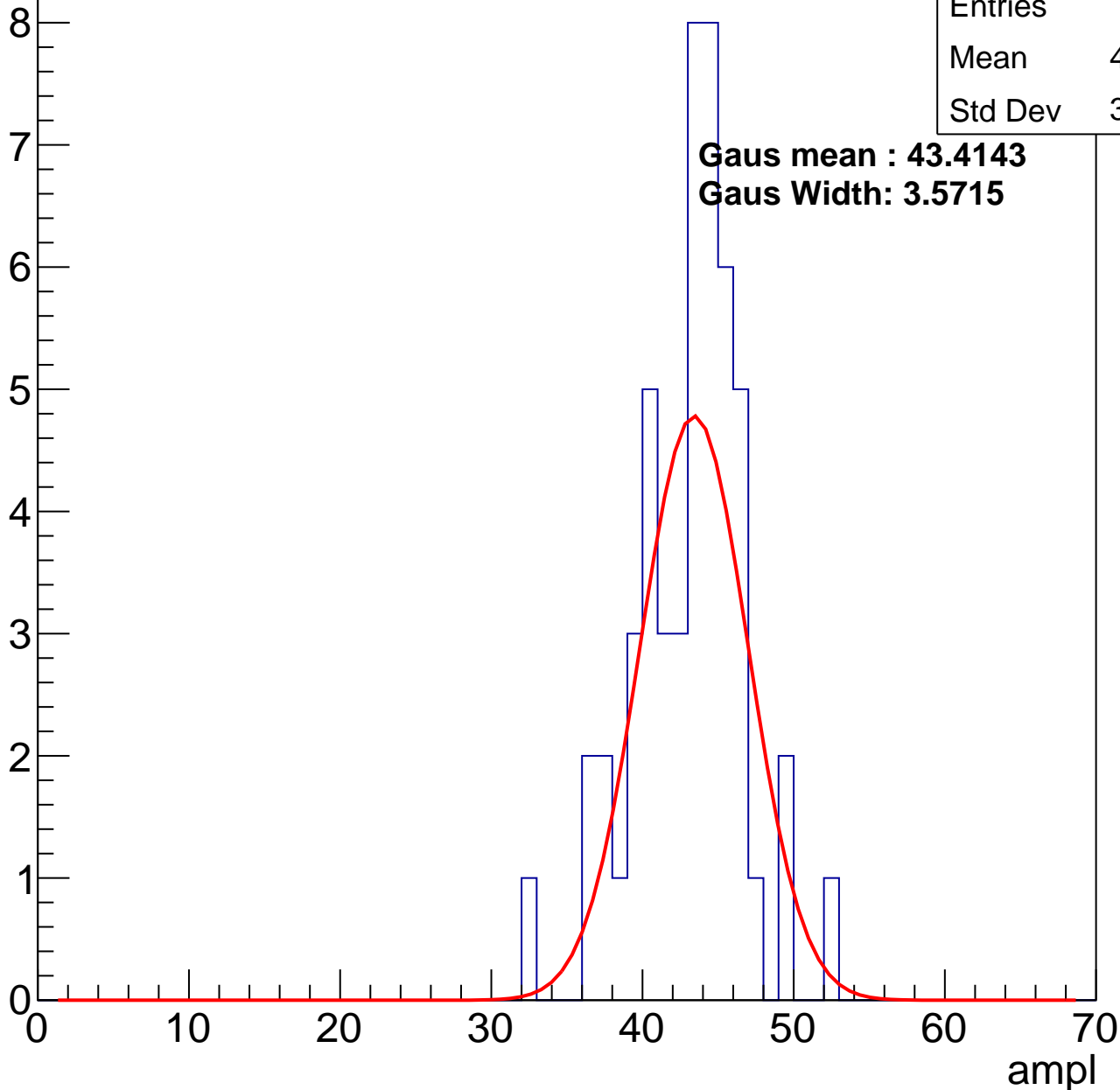
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	51
Mean	42.65
Std Dev	3.607

**Gaus mean : 43.4143**

**Gaus Width: 3.5715**



# B1L003S, U3-ch65, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

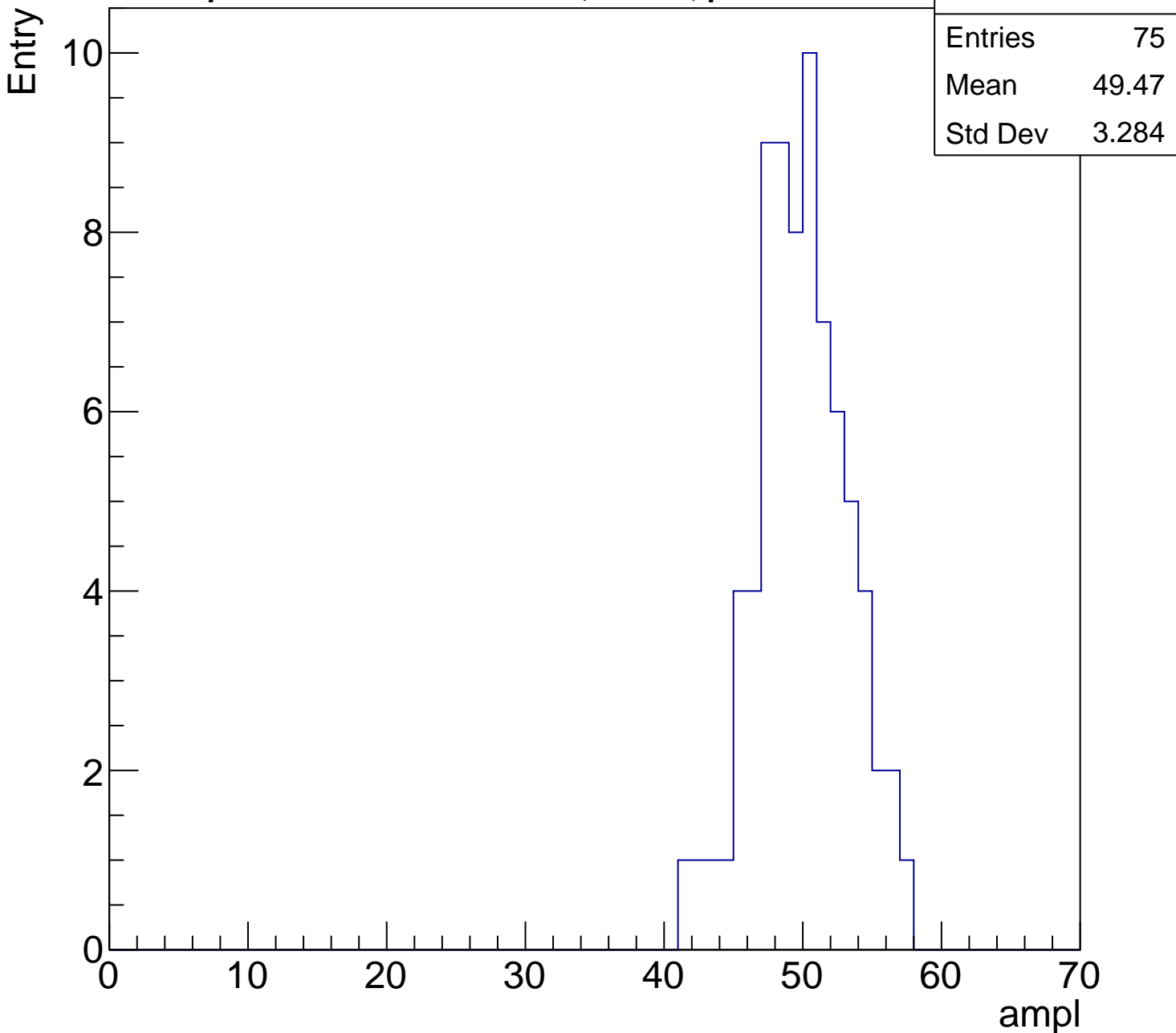
Entries	75
Mean	49.47
Std Dev	3.284

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

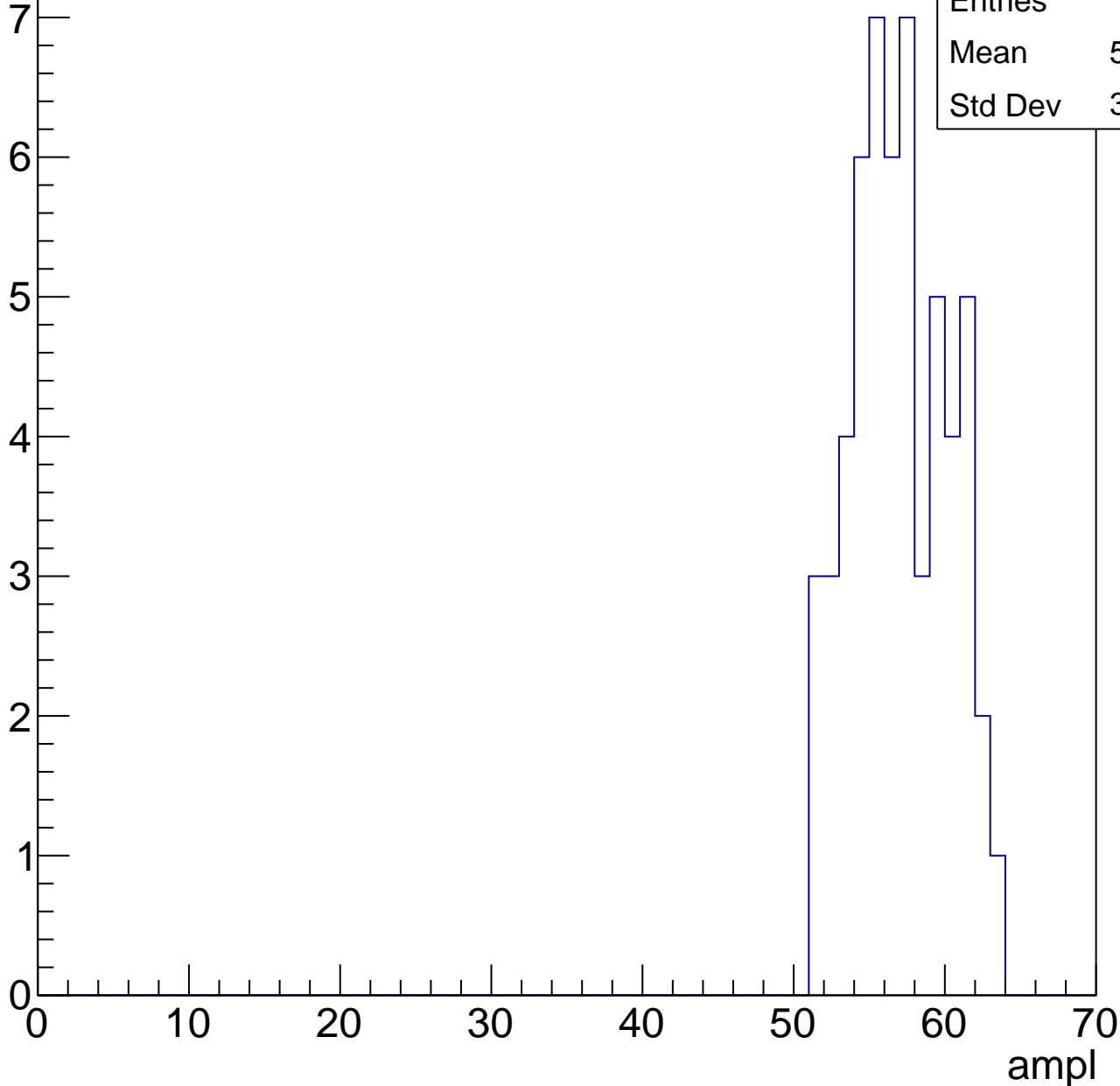


# B1L003S, U3-ch65, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	56.54
Std Dev	3.128

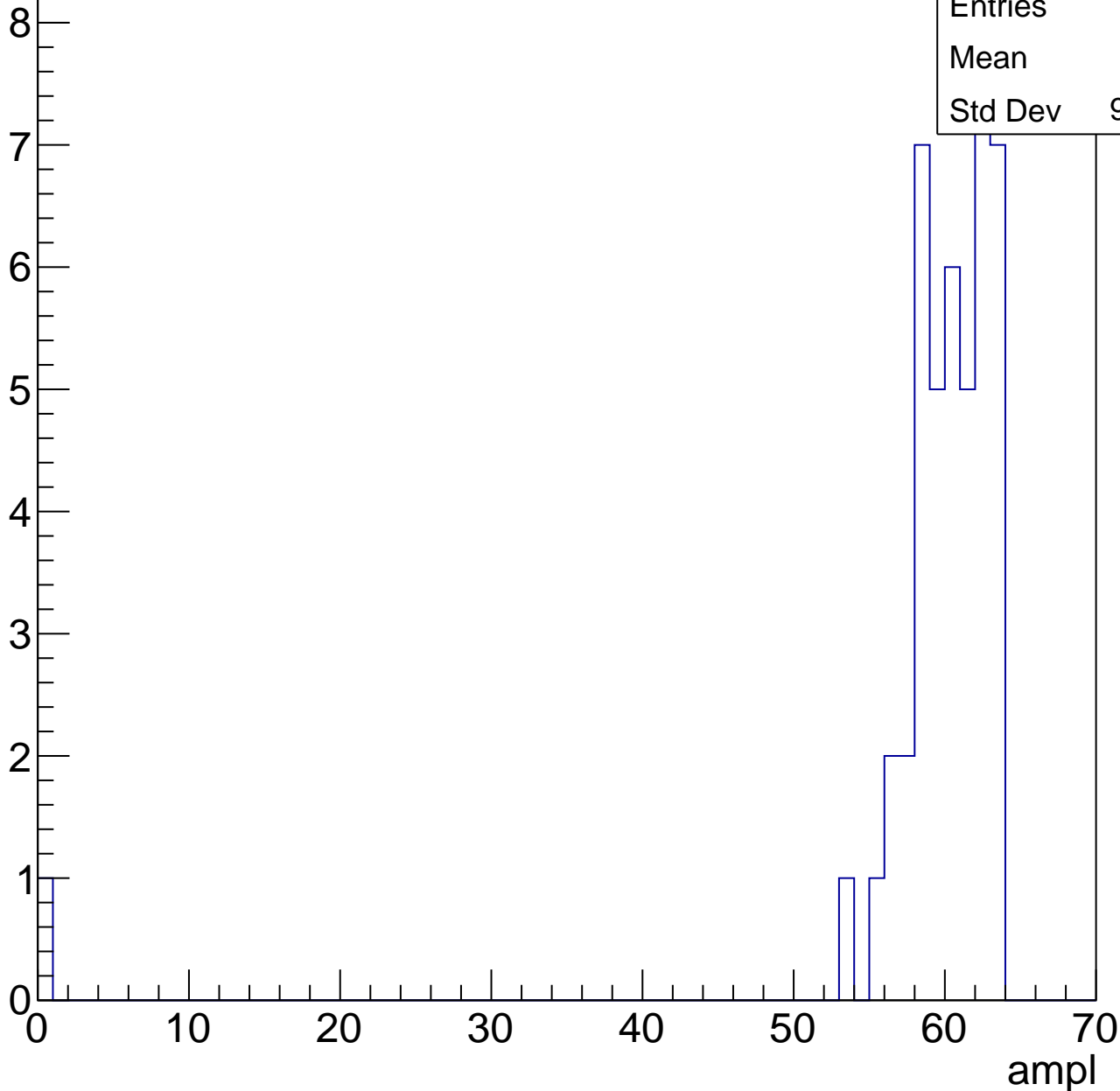


# B1L003S, U3-ch65, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	45
Mean	58.6
Std Dev	9.152



# B1L003S, U3-ch65, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch65, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U3-ch66, adc0

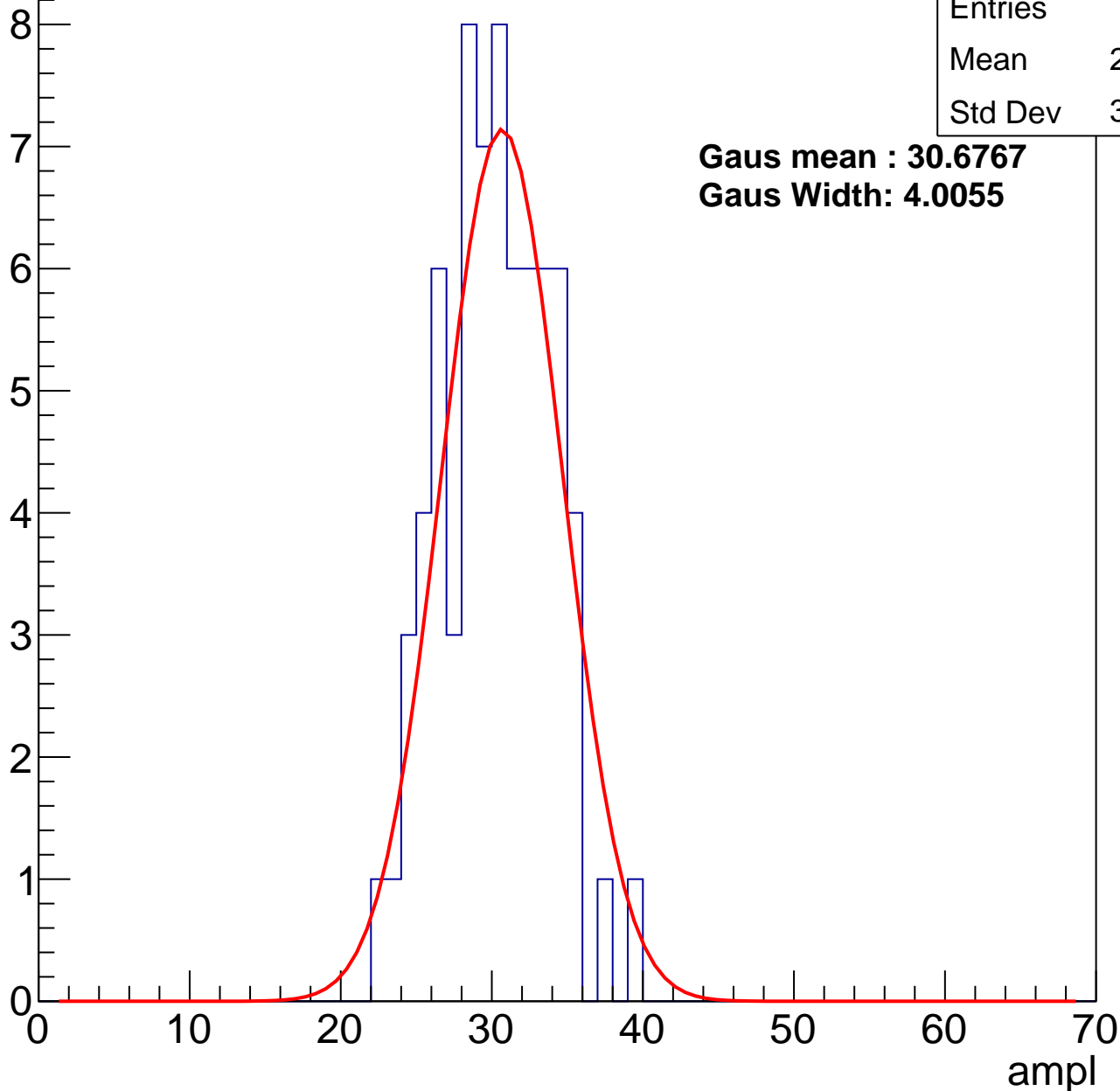
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	71
Mean	29.82
Std Dev	3.542

**Gaus mean : 30.6767**

**Gaus Width: 4.0055**



# B1L003S, U3-ch66, adc1

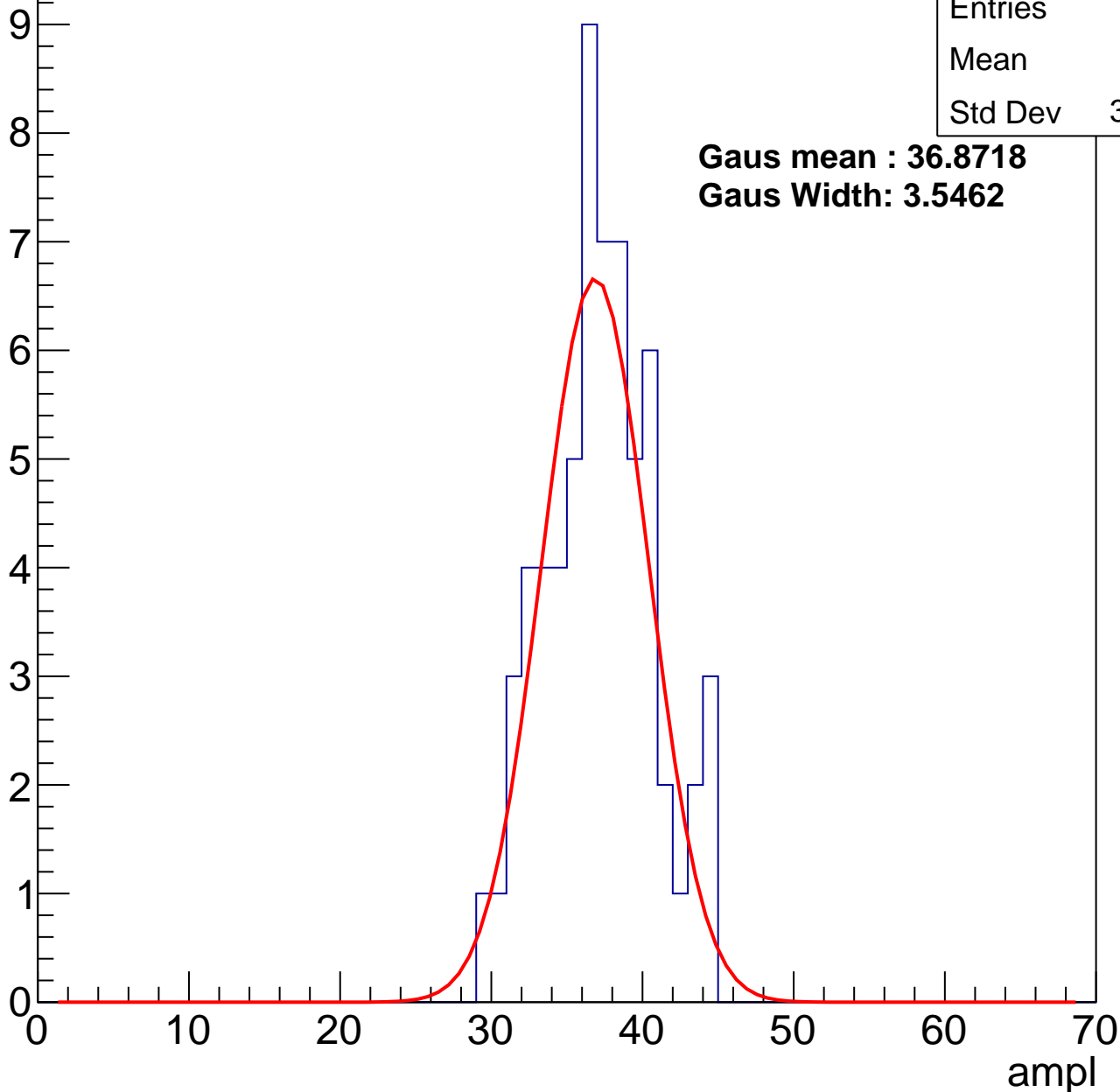
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	36.7
Std Dev	3.539

**Gaus mean : 36.8718**

**Gaus Width: 3.5462**



# B1L003S, U3-ch66, adc2

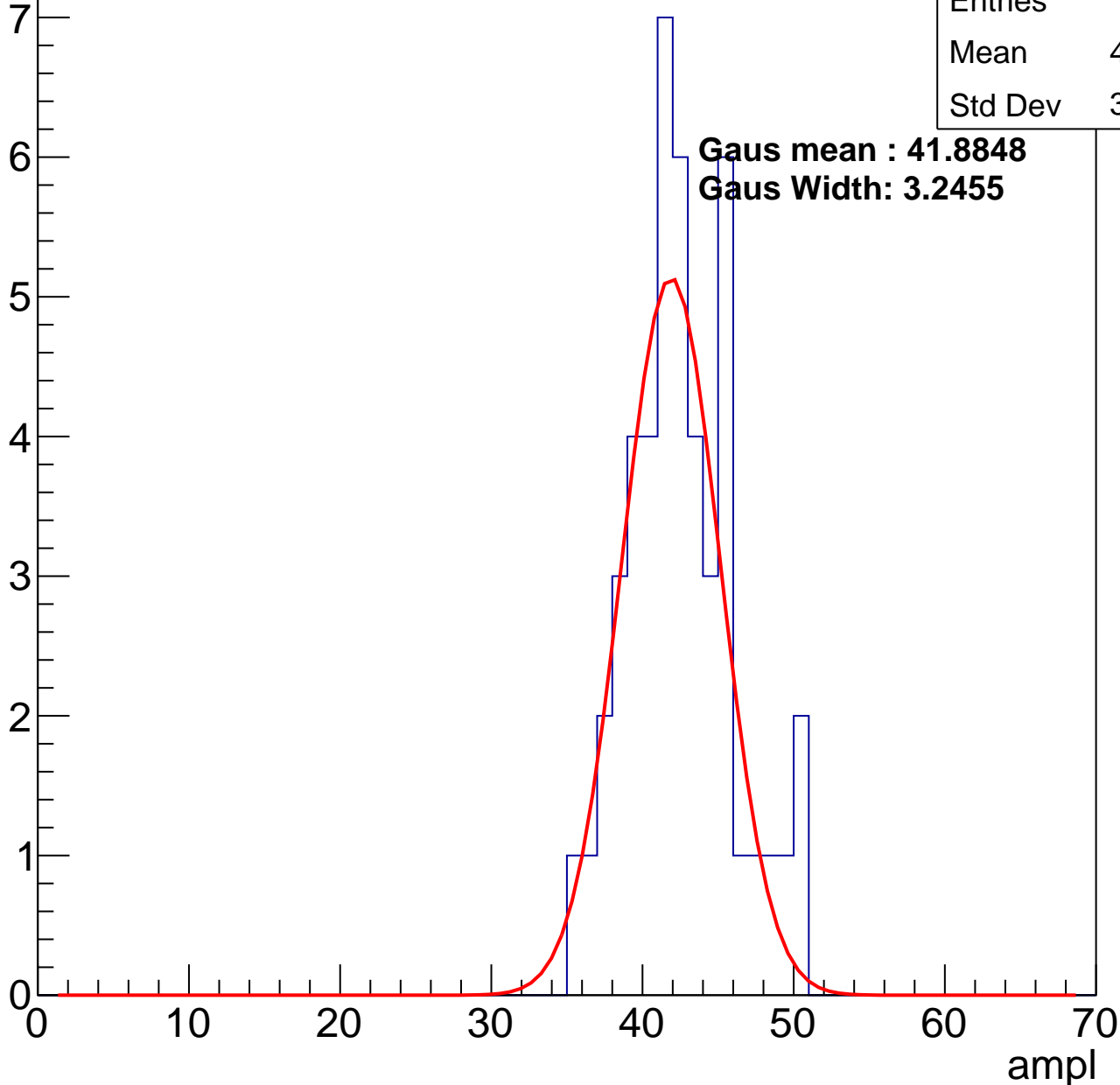
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	47
Mean	42.09
Std Dev	3.469

**Gaus mean : 41.8848**

**Gaus Width: 3.2455**

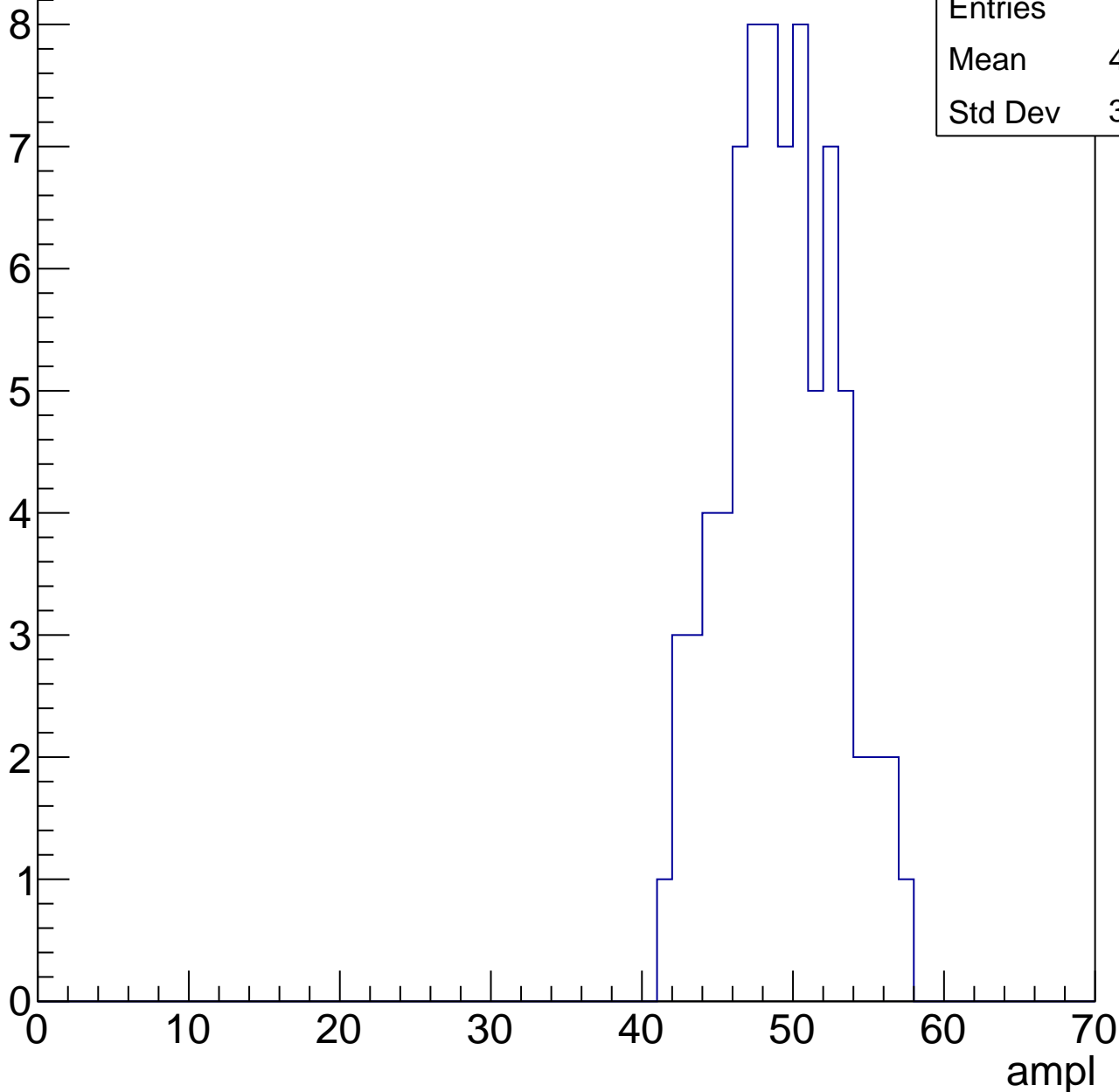


# B1L003S, U3-ch66, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

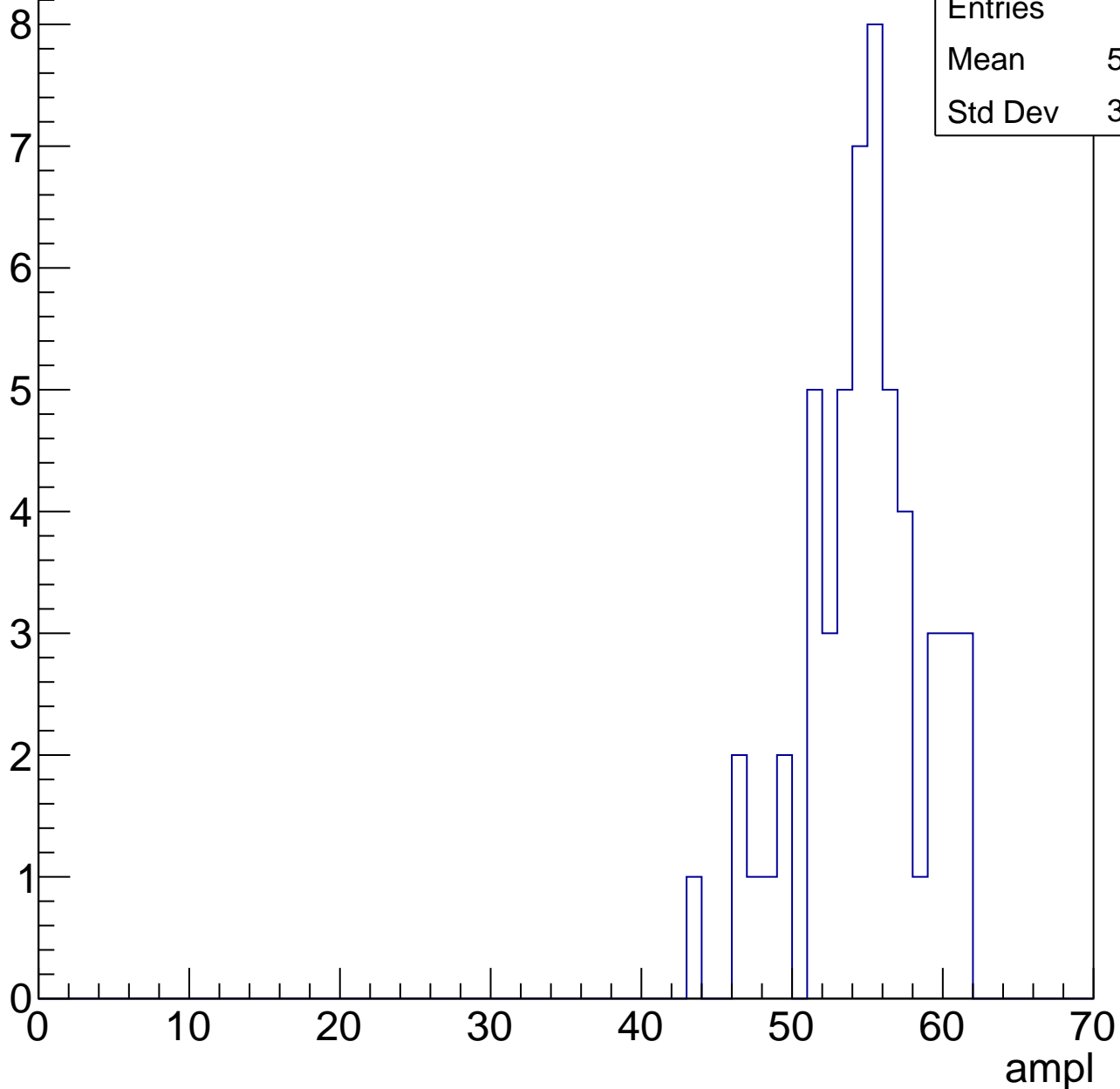
Entries	77
Mean	48.68
Std Dev	3.663



# B1L003S, U3-ch66, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

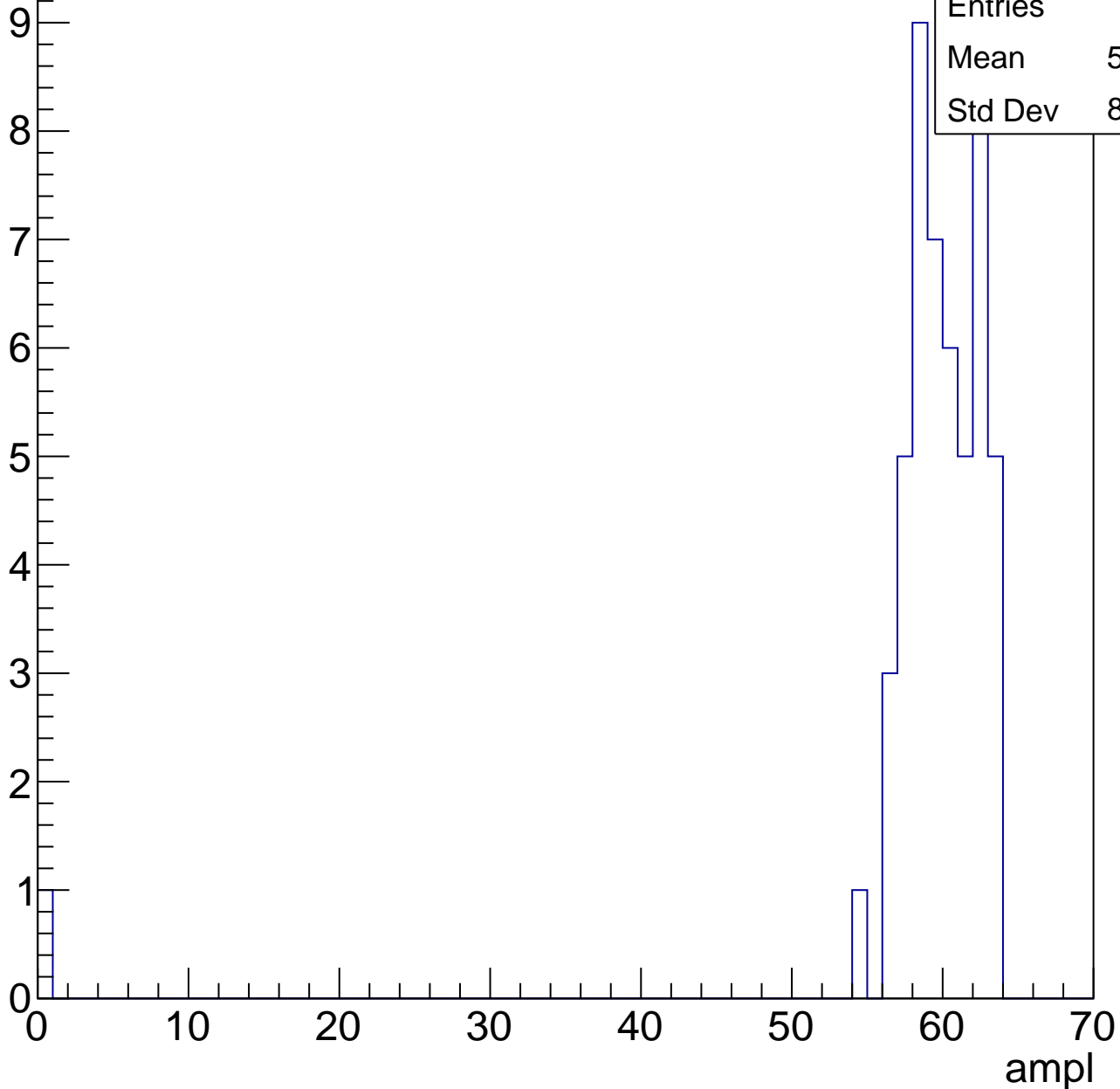


# B1L003S, U3-ch66, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	50
Mean	58.36
Std Dev	8.625

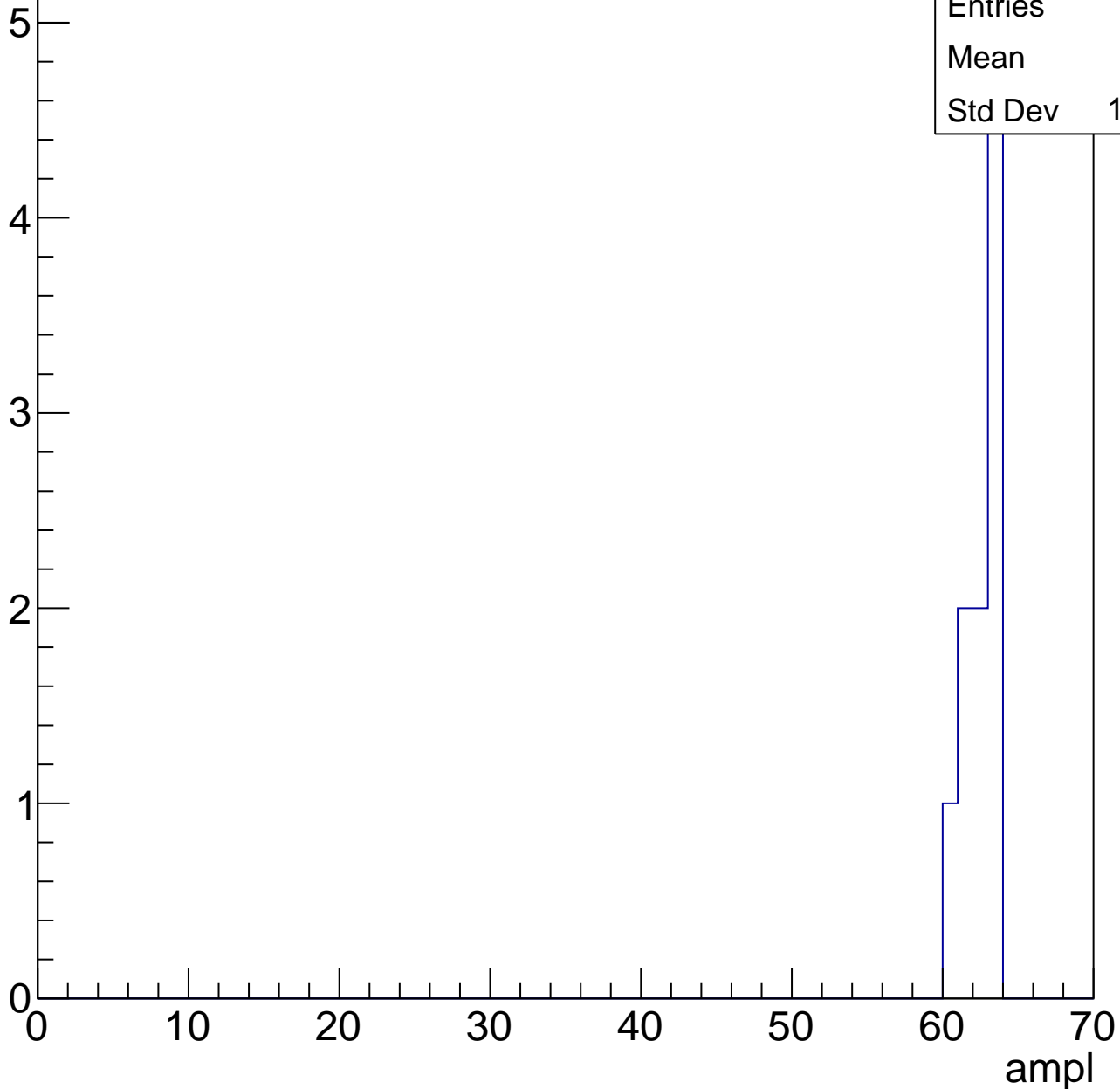


# B1L003S, U3-ch66, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	10
Mean	62.1
Std Dev	1.044





# B1L003S, U3-ch66, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	10.5
Std Dev	10.5

# B1L003S, U3-ch67, adc0

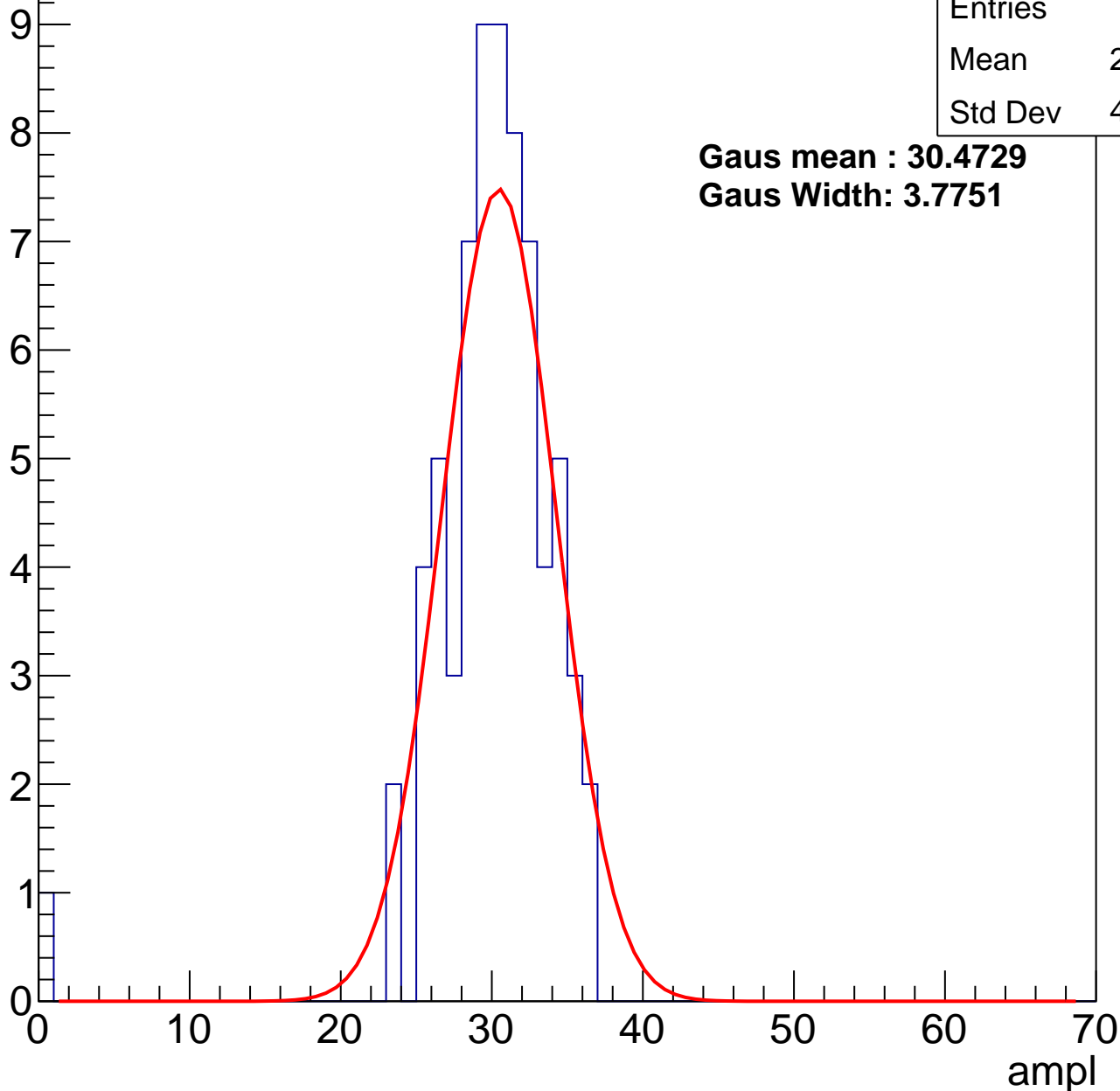
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	29.49
Std Dev	4.699

**Gaus mean : 30.4729**

**Gaus Width: 3.7751**



# B1L003S, U3-ch67, adc1

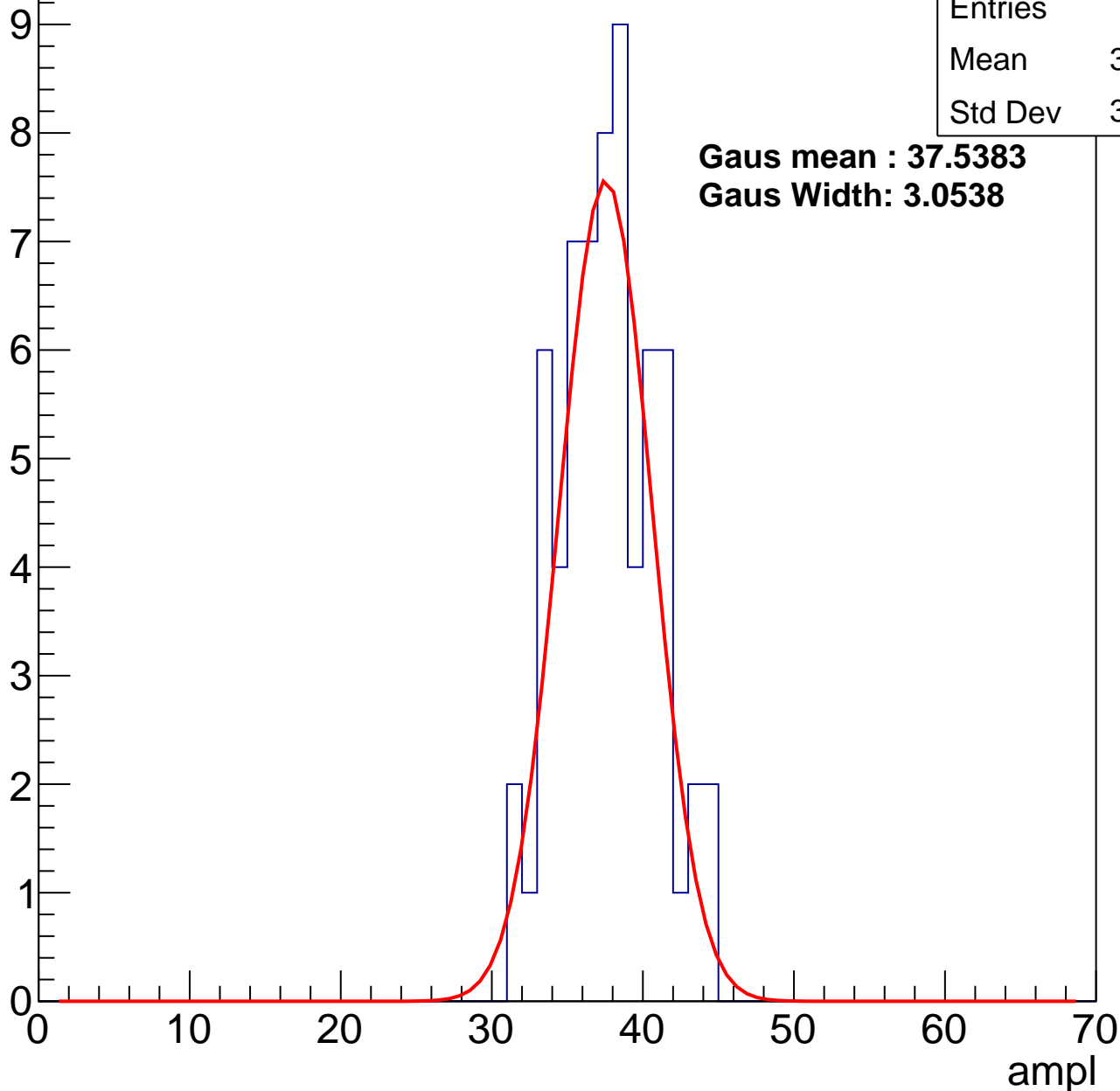
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	37.25
Std Dev	3.113

**Gaus mean : 37.5383**

**Gaus Width: 3.0538**



# B1L003S, U3-ch67, adc2

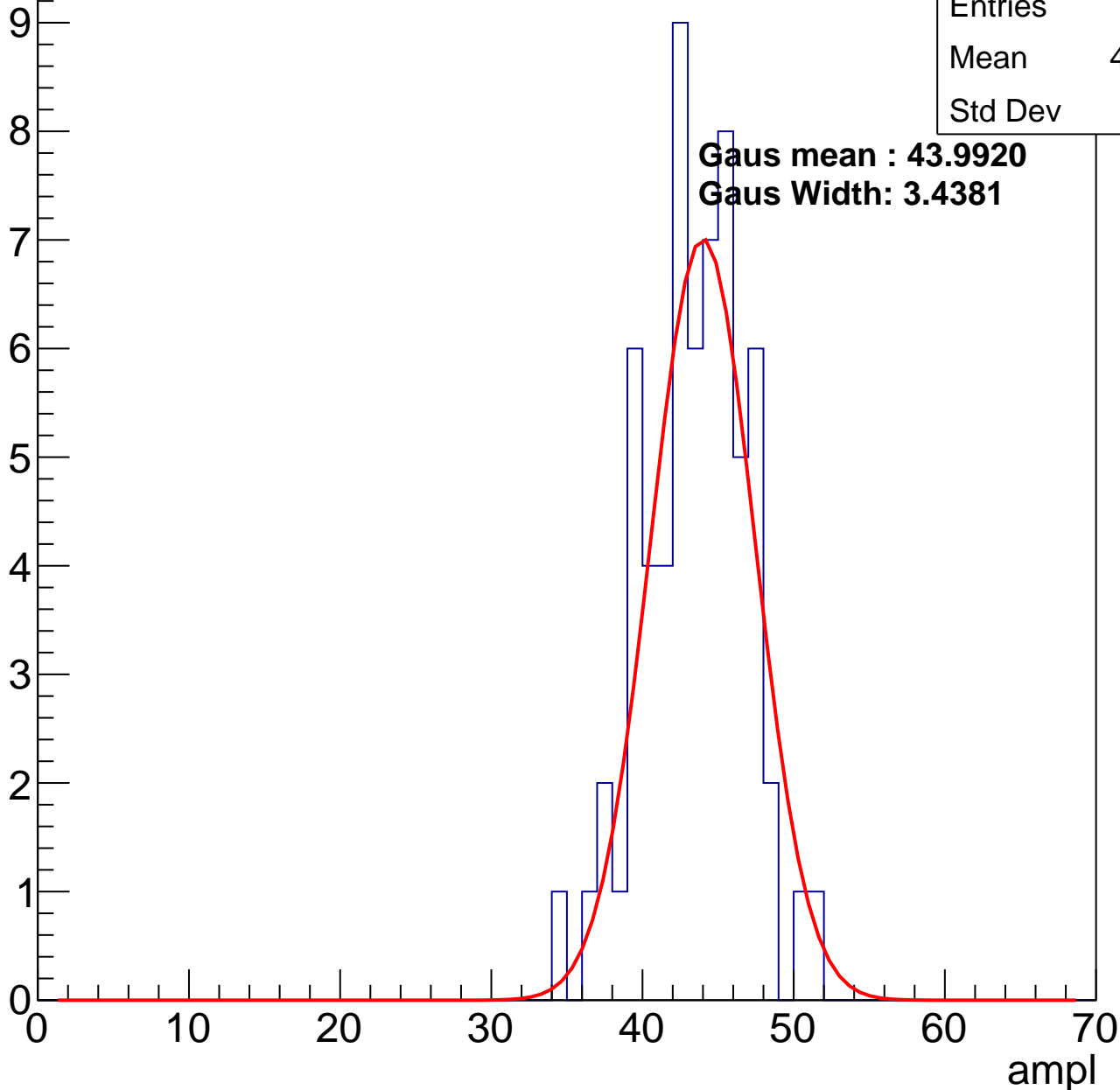
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	43.02
Std Dev	3.37

**Gaus mean : 43.9920**

**Gaus Width: 3.4381**

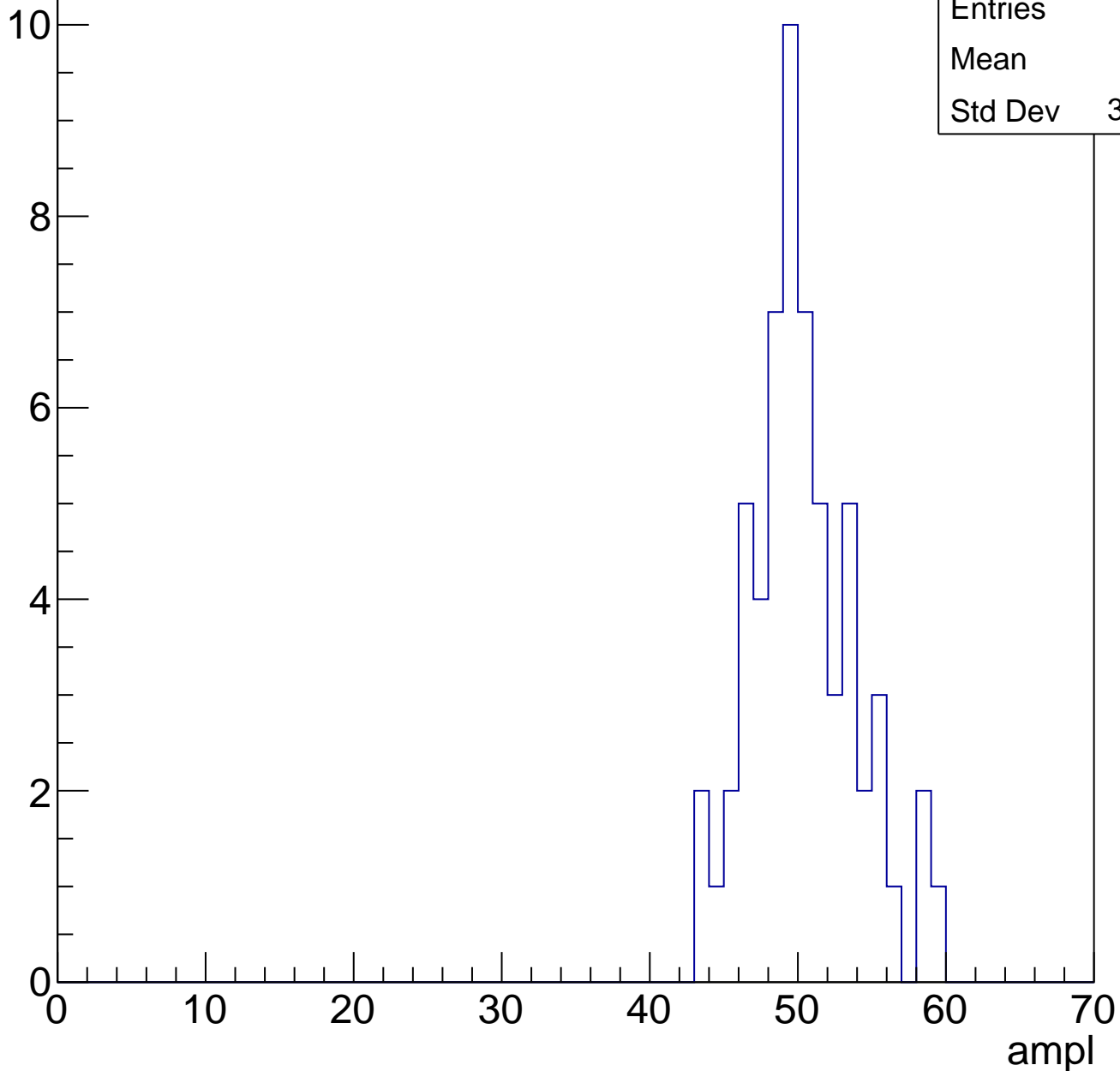


# B1L003S, U3-ch67, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	60
Mean	49.9
Std Dev	3.539

Entry

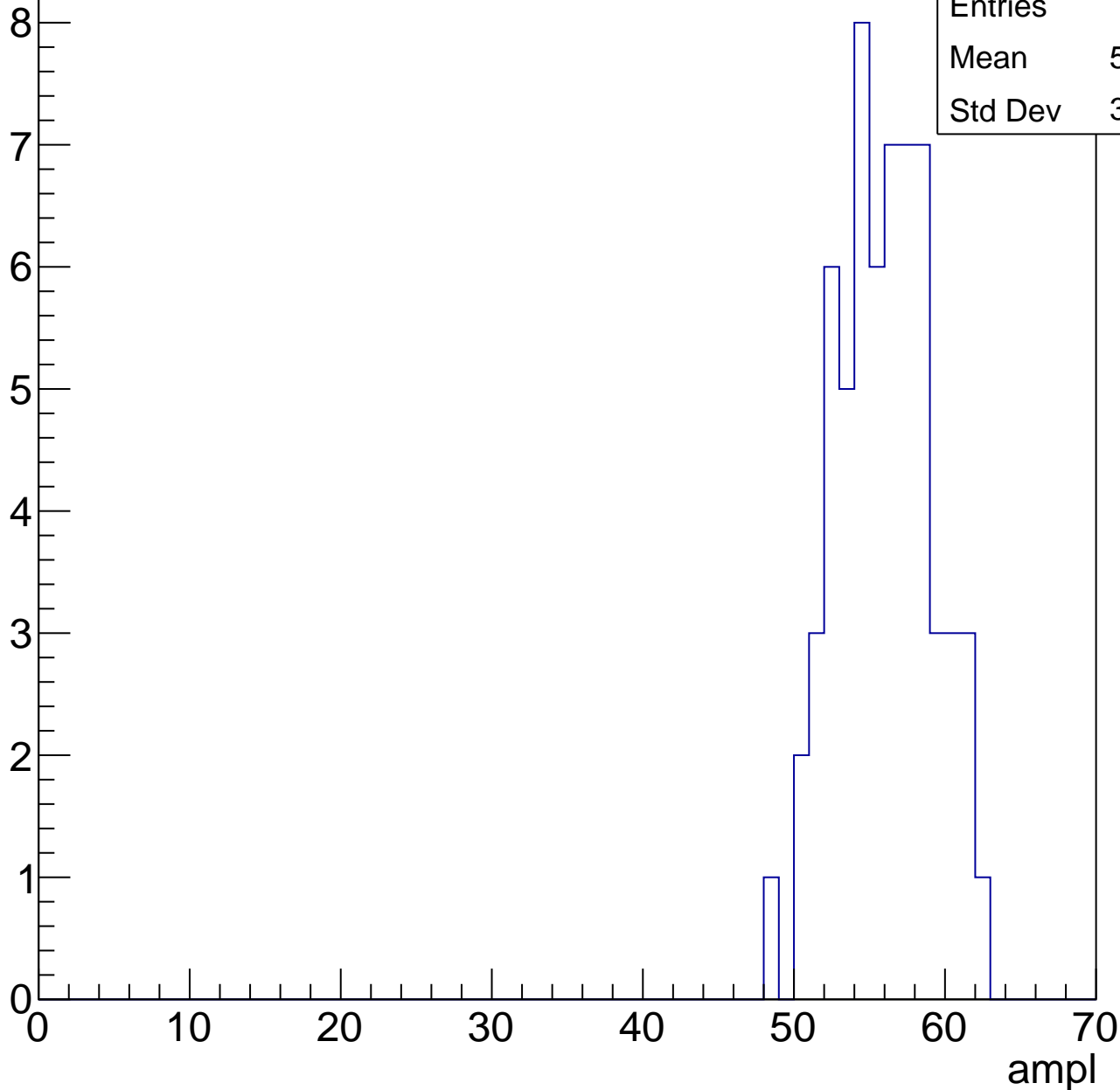


# B1L003S, U3-ch67, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	55.47
Std Dev	3.094

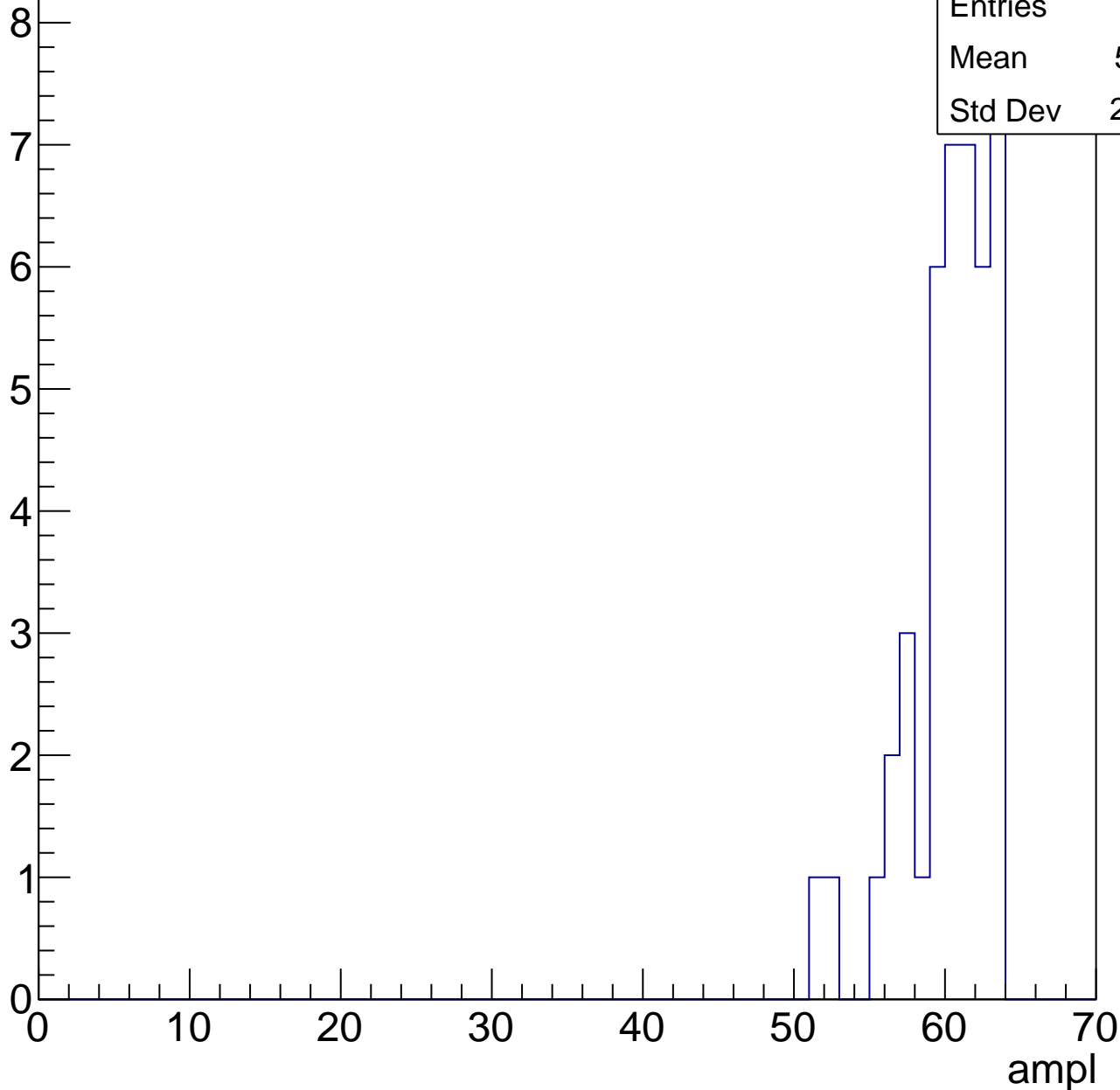


# B1L003S, U3-ch67, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	43
Mean	59.91
Std Dev	2.819



# B1L003S, U3-ch67, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	5
Mean	50
Std Dev	25



# B1L003S, U3-ch67, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U3-ch68, adc0

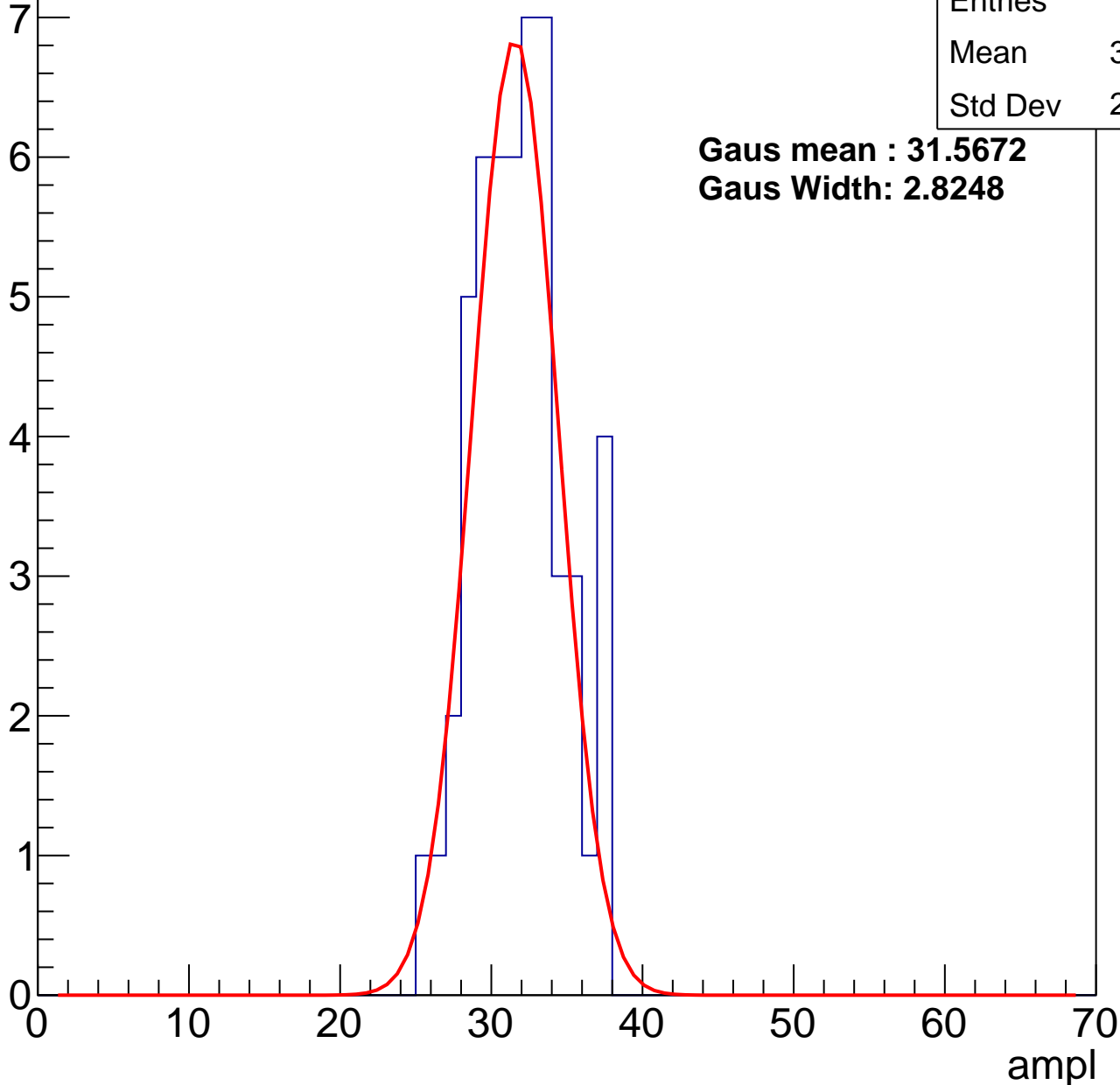
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	52
Mean	31.37
Std Dev	2.909

**Gaus mean : 31.5672**

**Gaus Width: 2.8248**



# B1L003S, U3-ch68, adc1

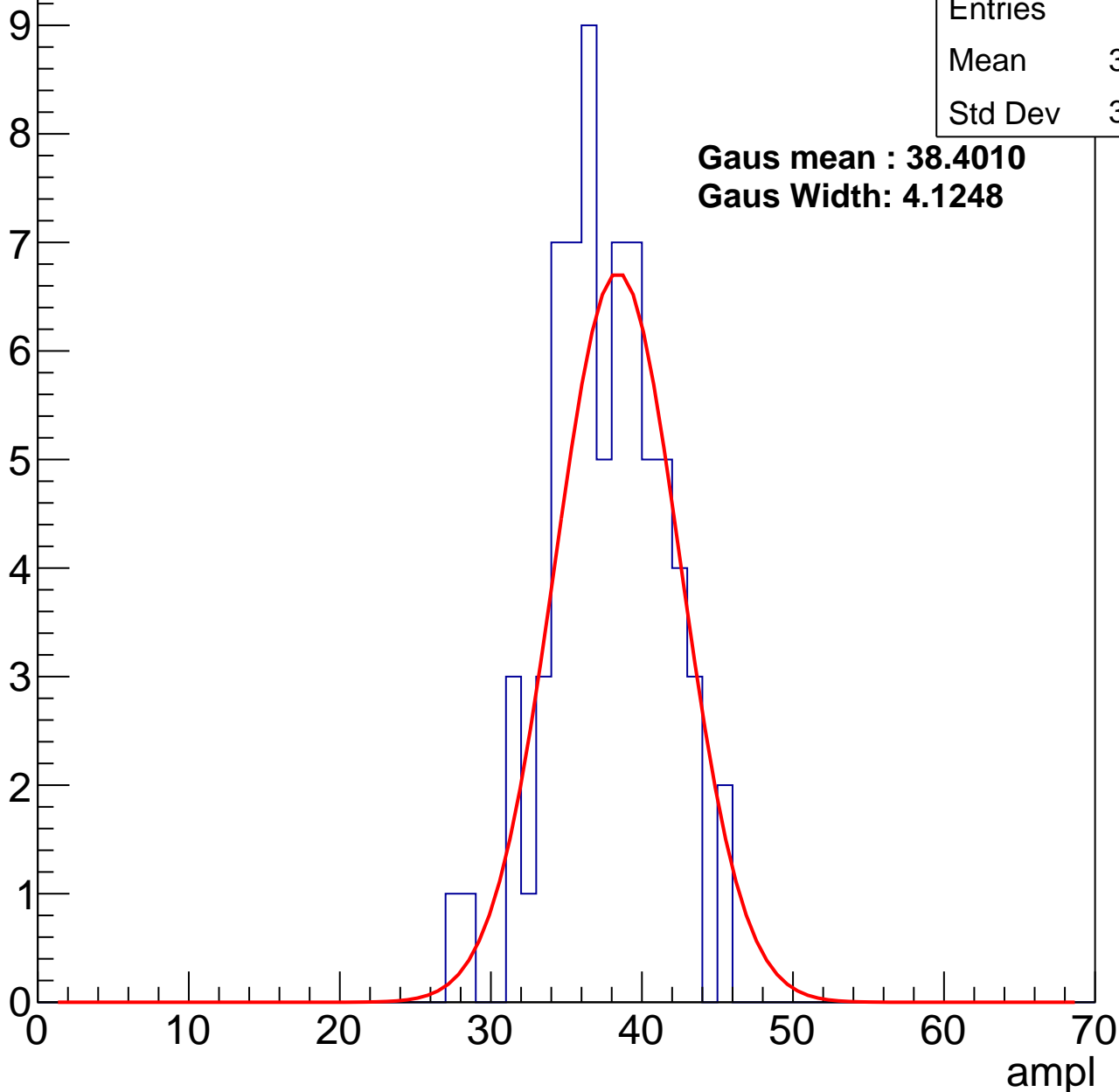
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	37.17
Std Dev	3.695

**Gaus mean : 38.4010**

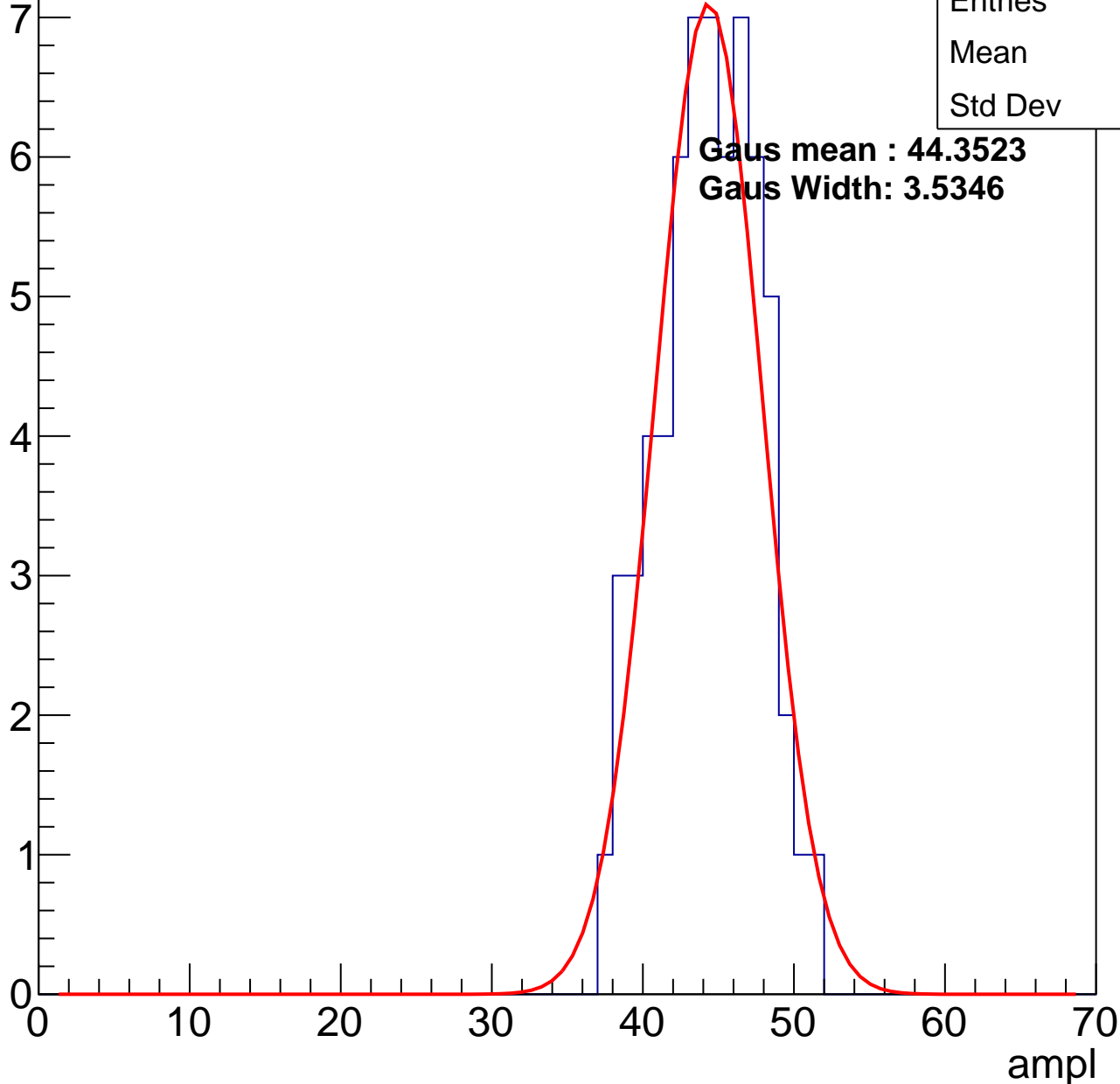
**Gaus Width: 4.1248**



# B1L003S, U3-ch68, adc2

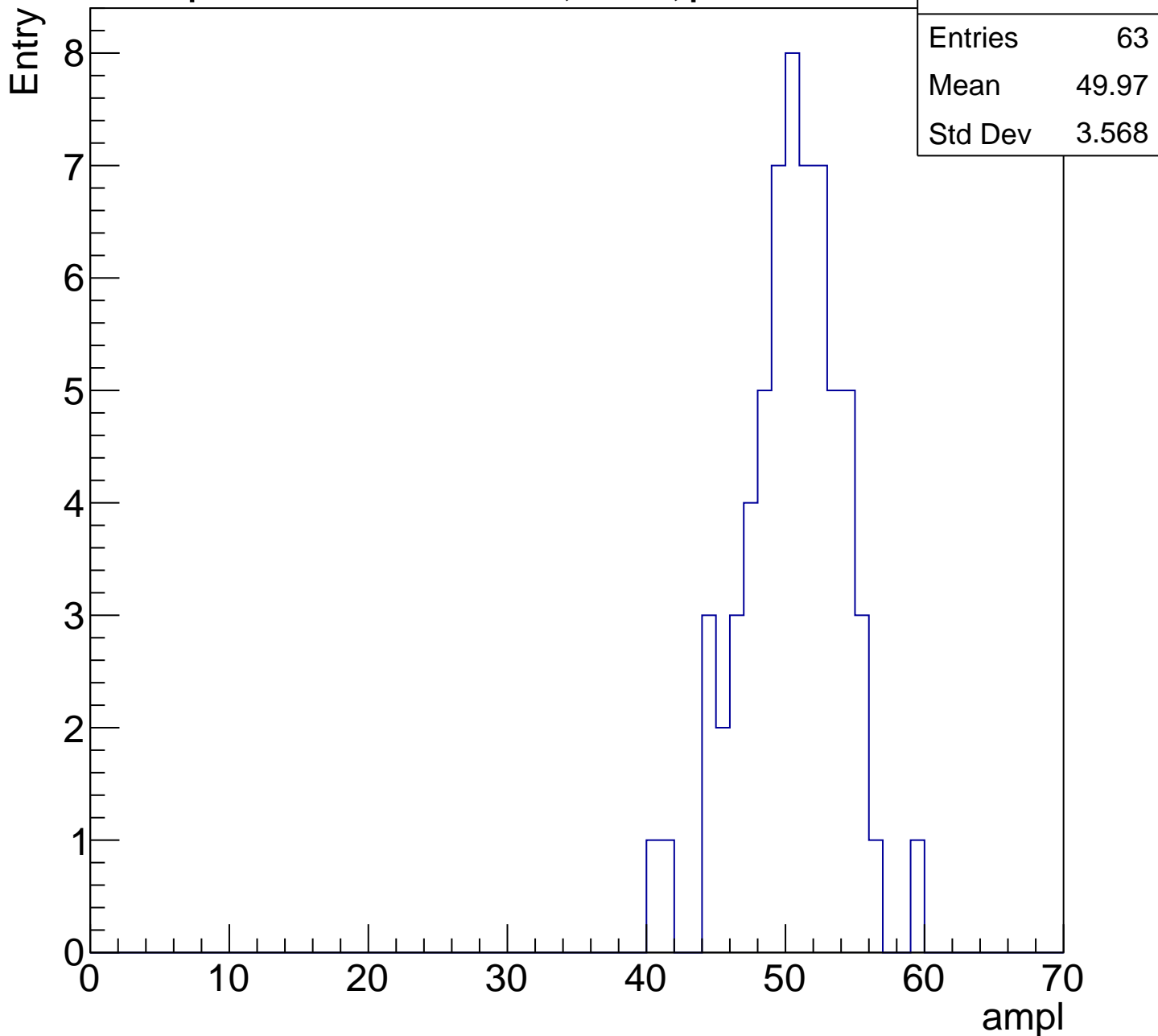
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U3-ch68, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

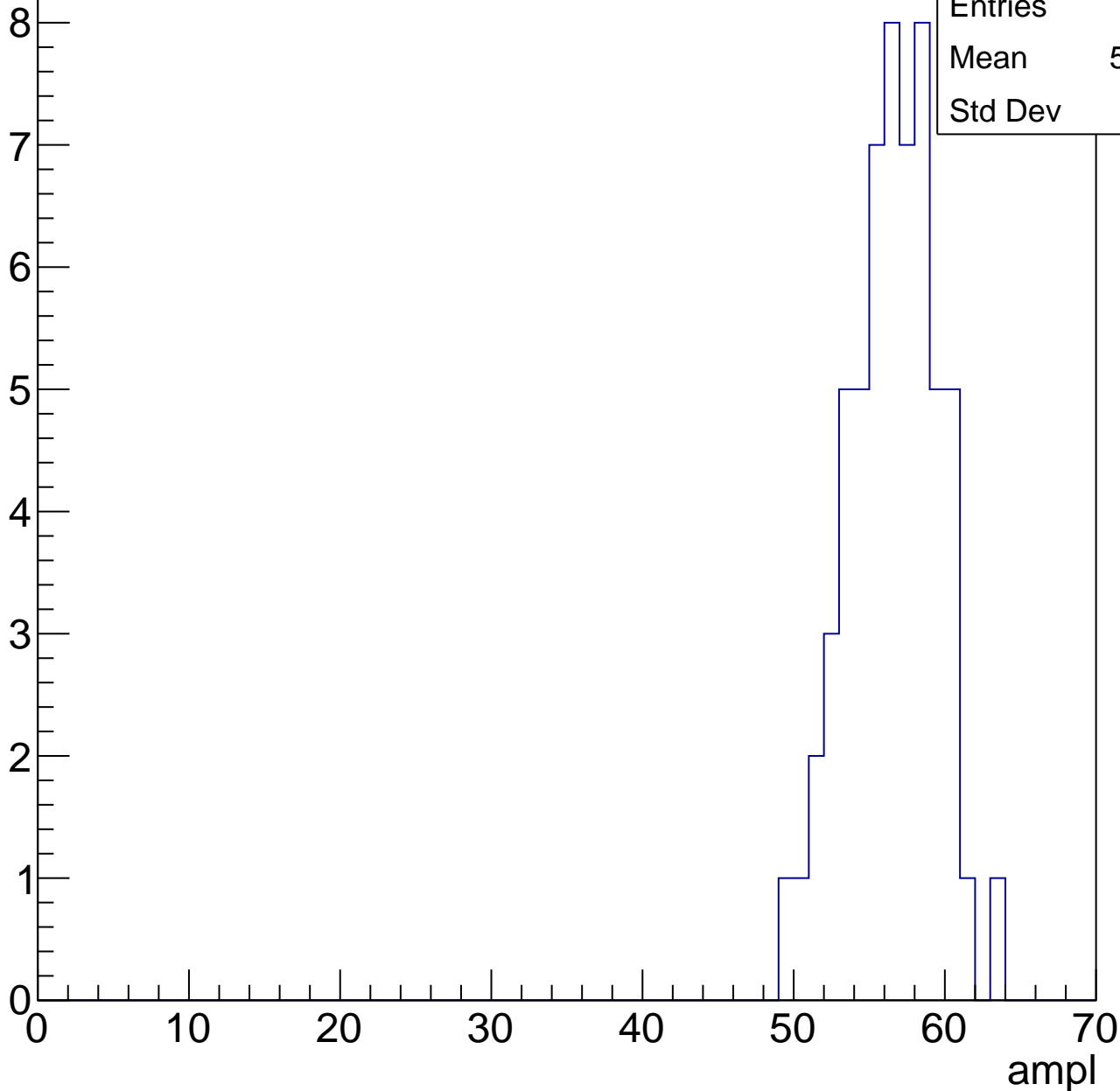


# B1L003S, U3-ch68, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

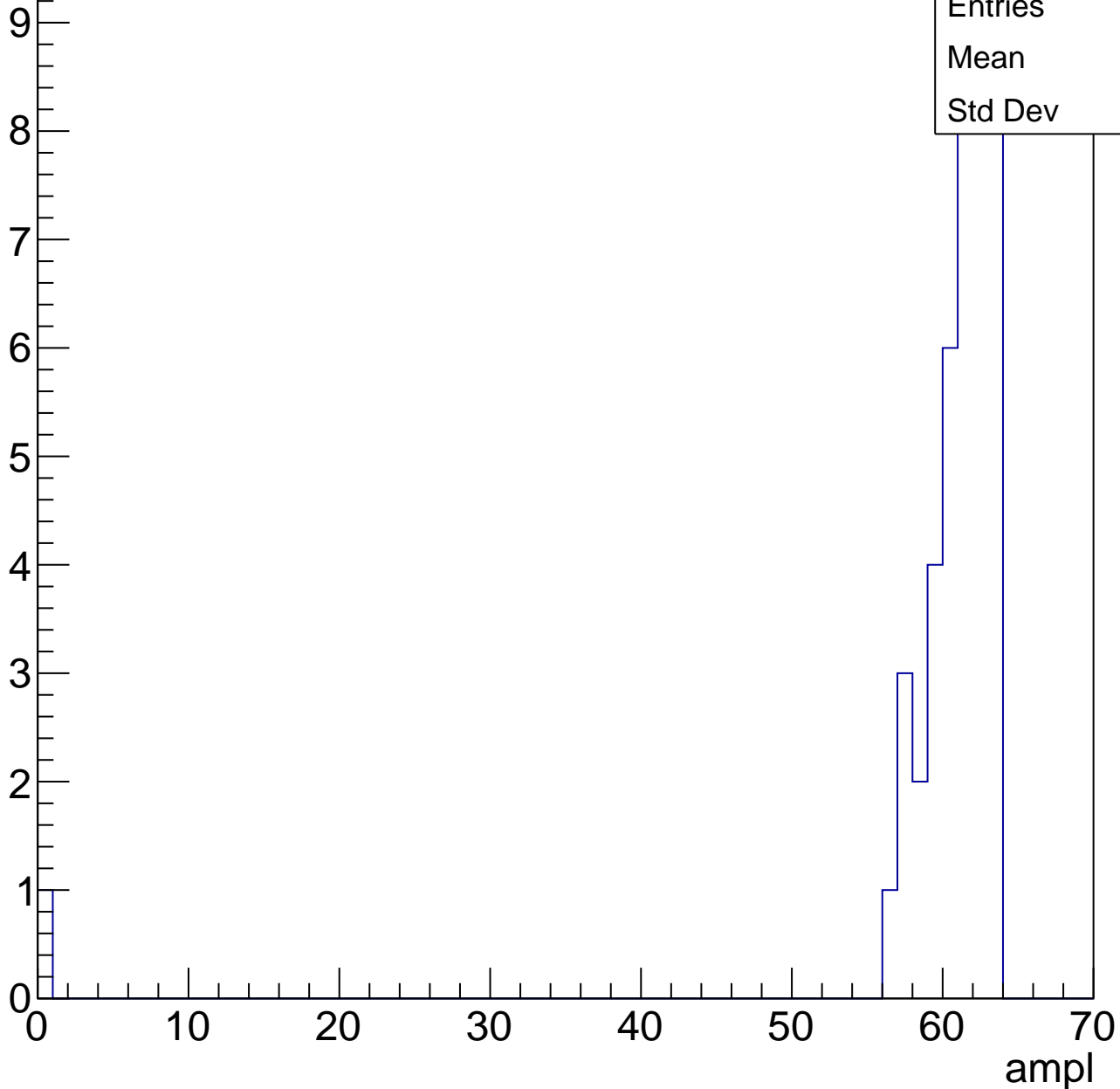
Entries	59
Mean	56.05
Std Dev	2.89



# B1L003S, U3-ch68, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U3-ch68, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch68, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U3-ch69, adc0

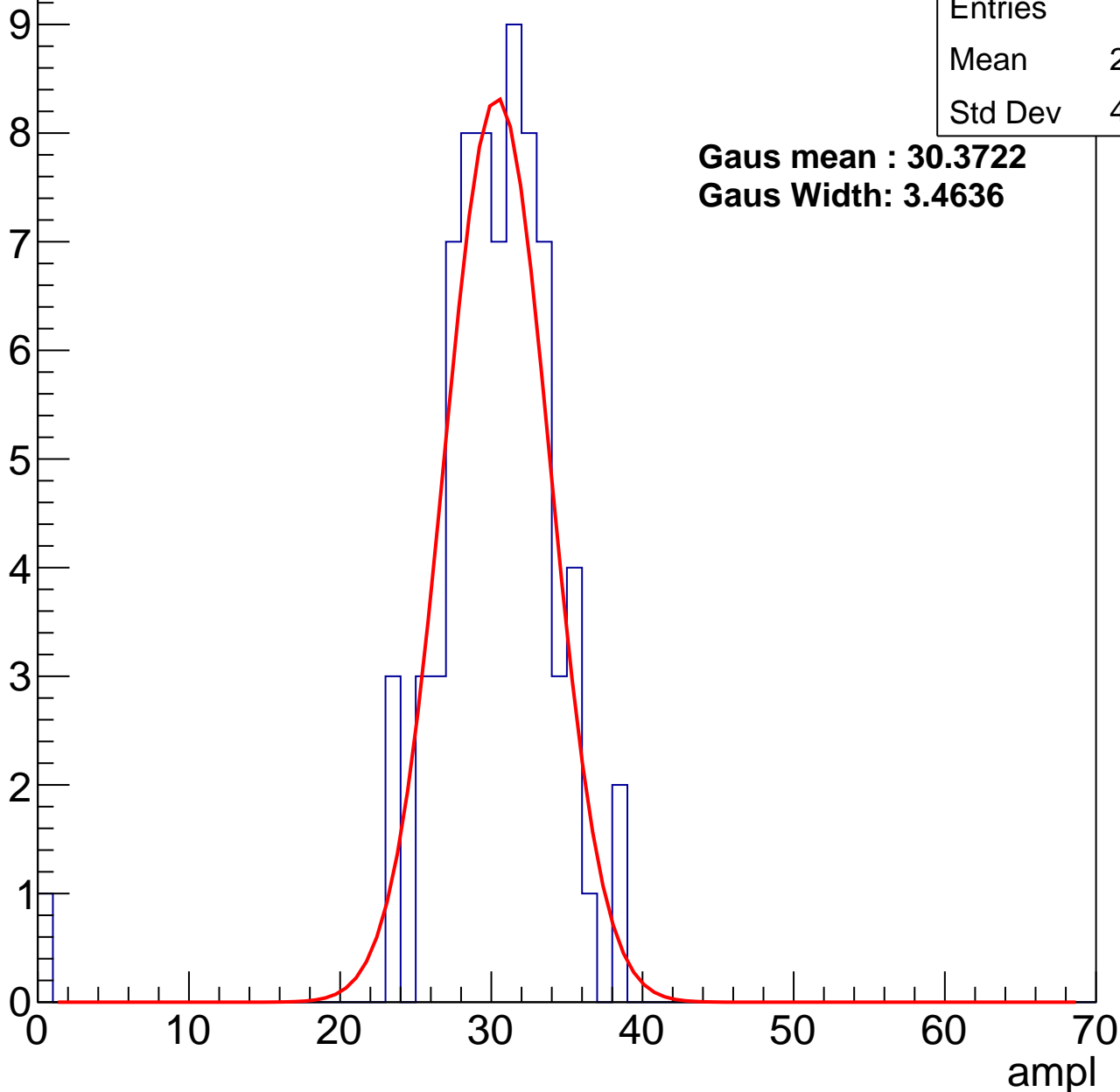
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	74
Mean	29.69
Std Dev	4.767

**Gaus mean : 30.3722**

**Gaus Width: 3.4636**



# B1L003S, U3-ch69, adc1

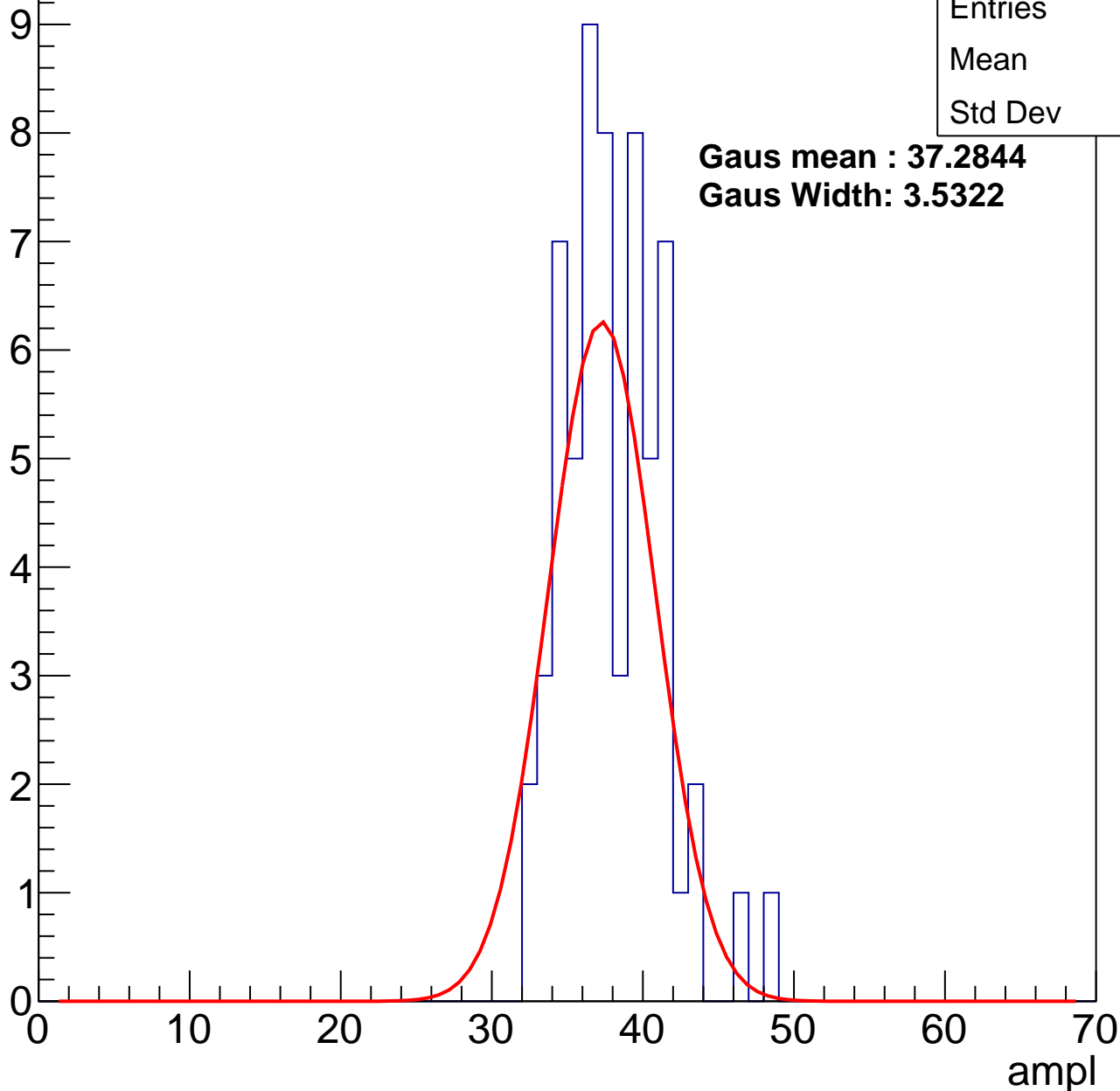
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	37.6
Std Dev	3.26

**Gaus mean : 37.2844**

**Gaus Width: 3.5322**



# B1L003S, U3-ch69, adc2

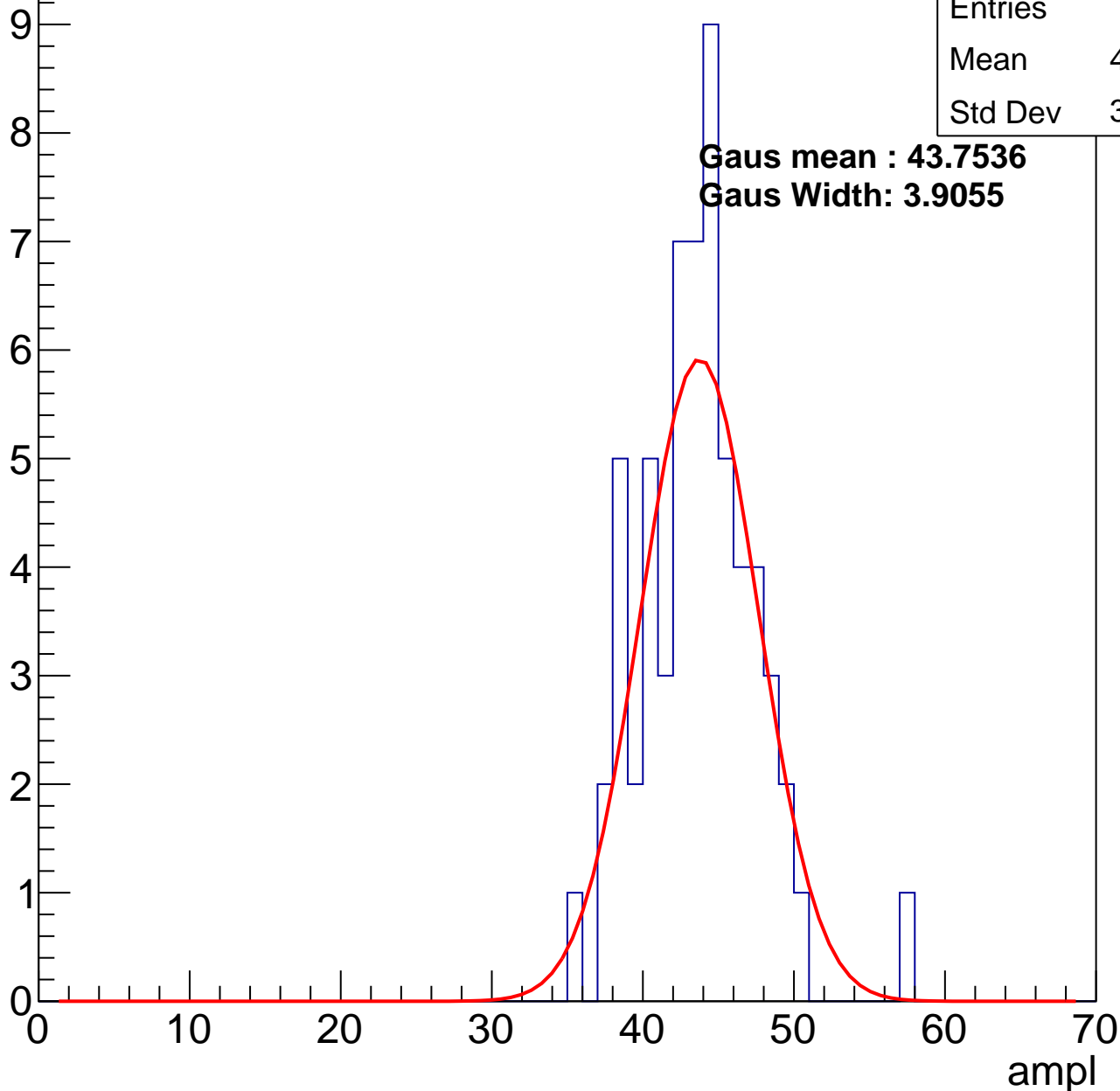
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	43.23
Std Dev	3.787

**Gaus mean : 43.7536**

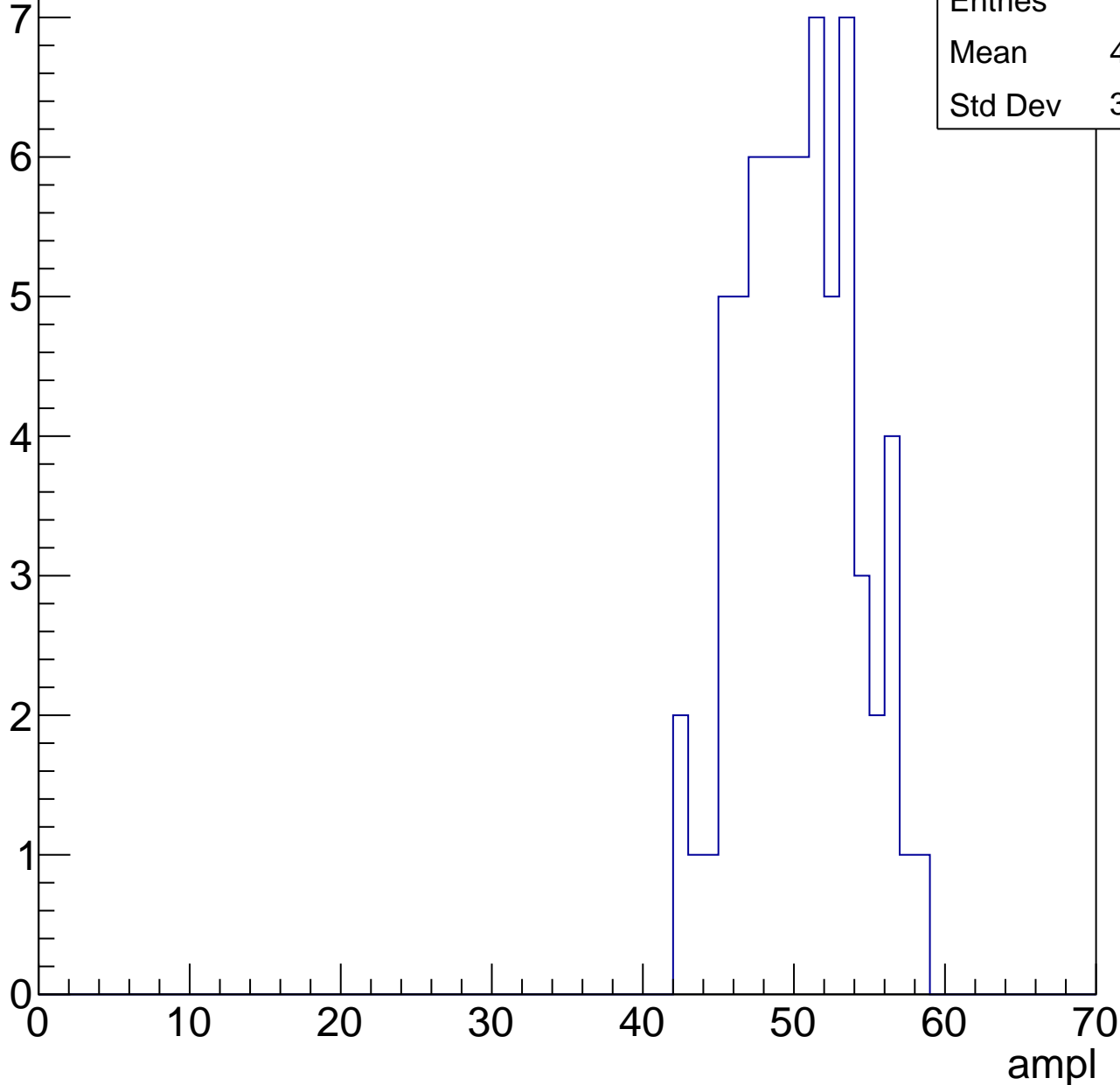
**Gaus Width: 3.9055**



# B1L003S, U3-ch69, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



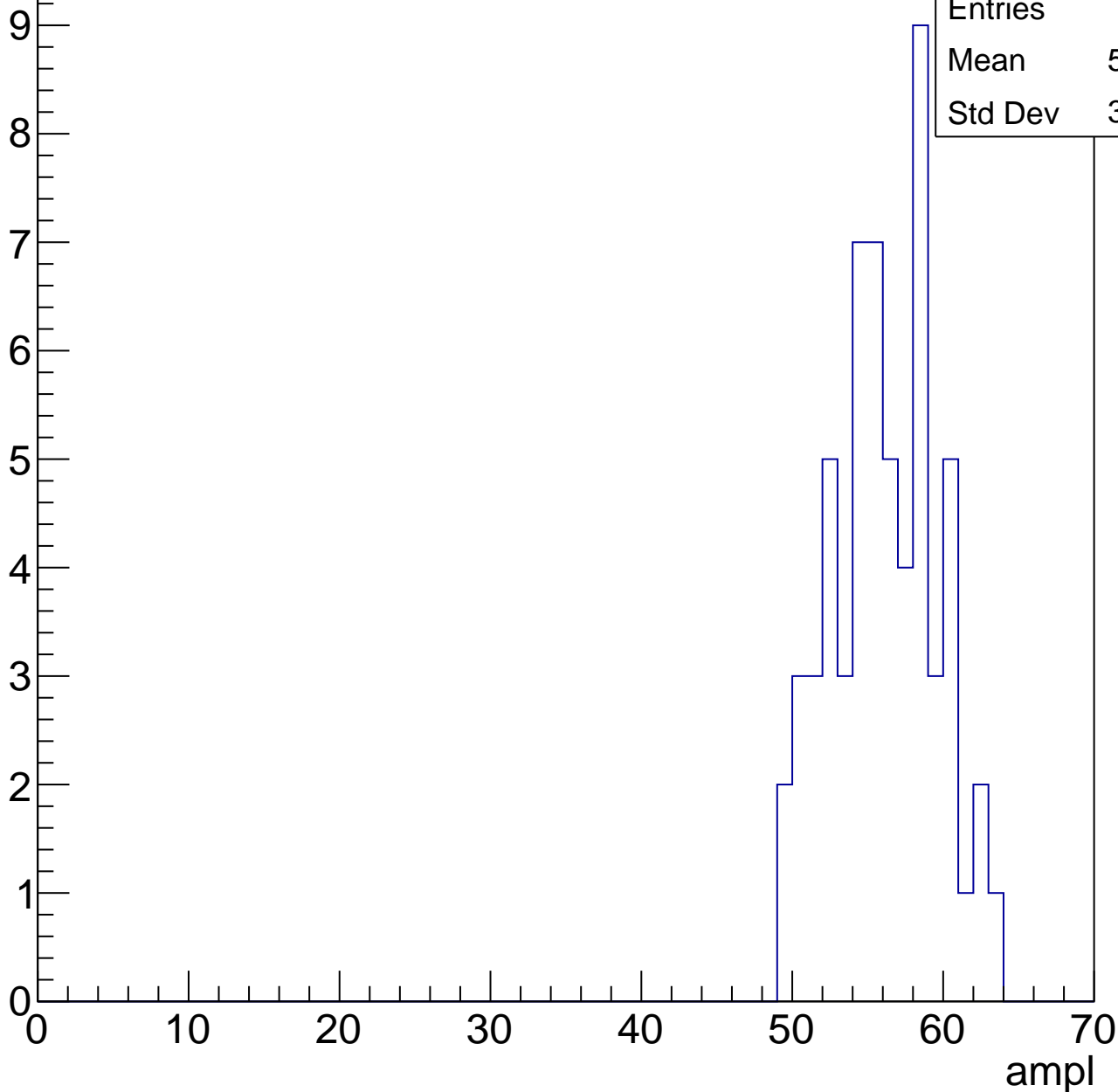
Entries	68
Mean	49.84
Std Dev	3.728

# B1L003S, U3-ch69, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	55.63
Std Dev	3.435

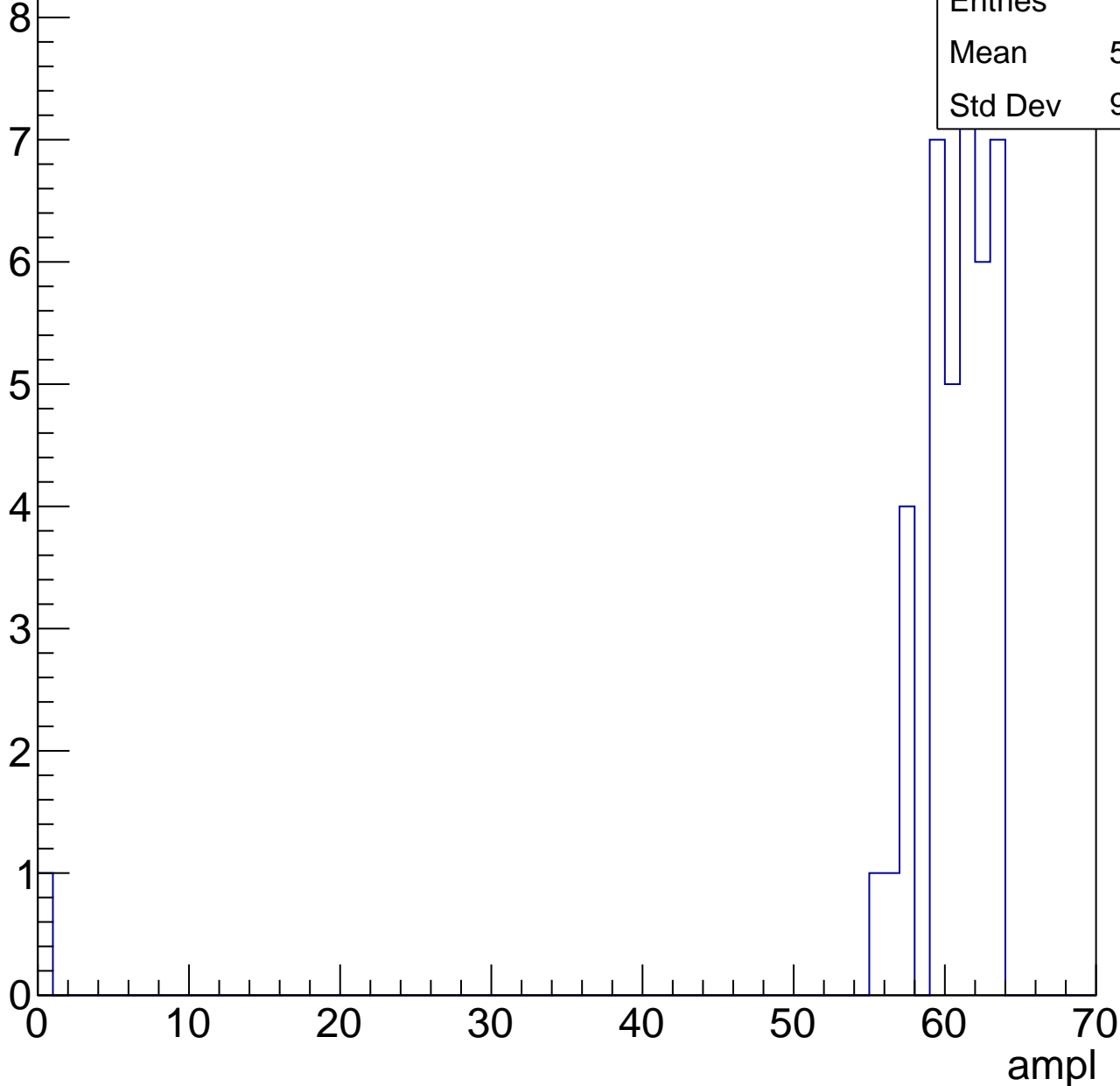


# B1L003S, U3-ch69, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	40
Mean	58.83
Std Dev	9.649



# B1L003S, U3-ch69, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch69, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U3-ch70, adc0

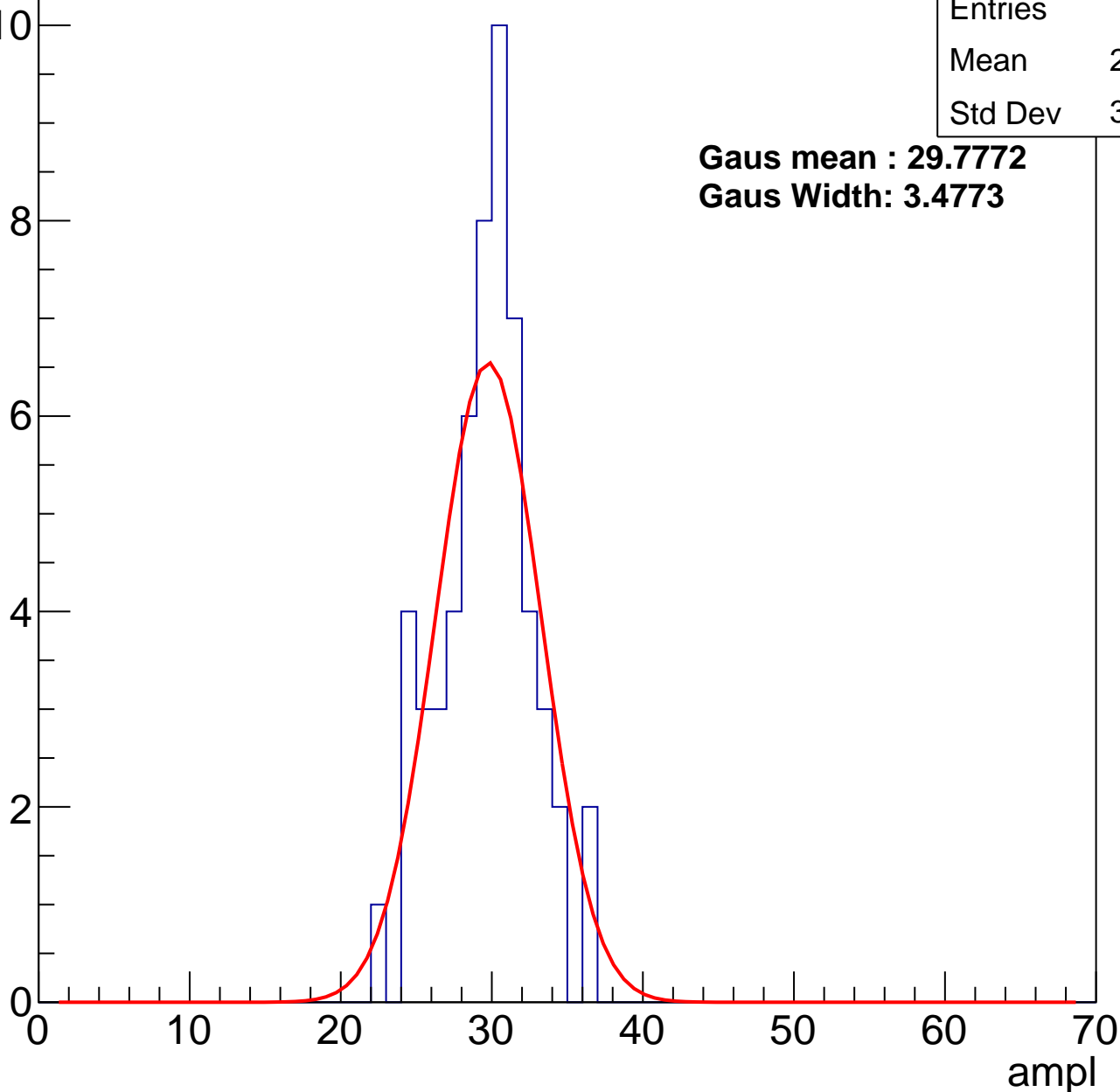
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	29.18
Std Dev	3.004

**Gaus mean : 29.7772**

**Gaus Width: 3.4773**



# B1L003S, U3-ch70, adc1

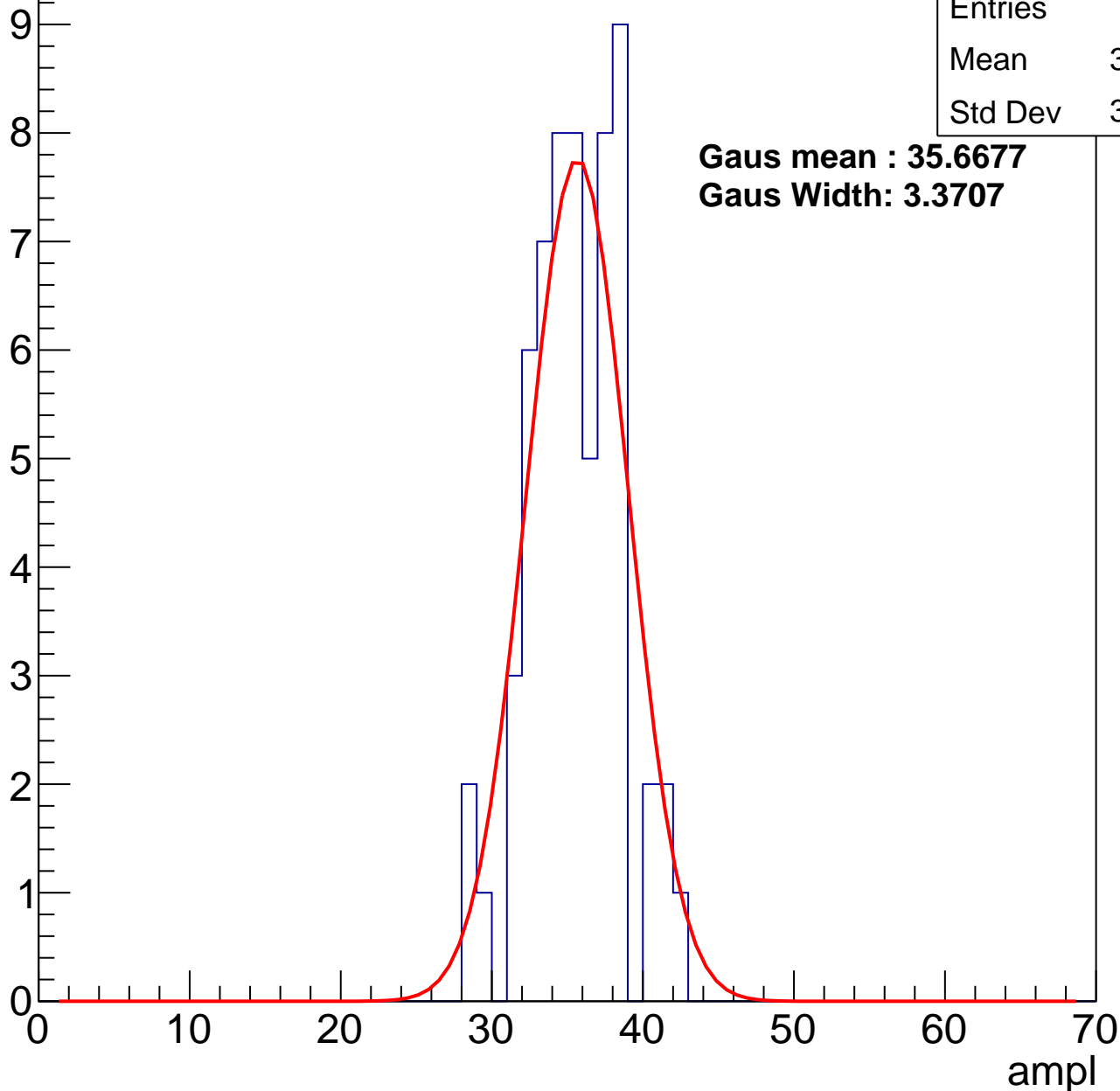
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	35.08
Std Dev	3.007

**Gaus mean : 35.6677**

**Gaus Width: 3.3707**



# B1L003S, U3-ch70, adc2

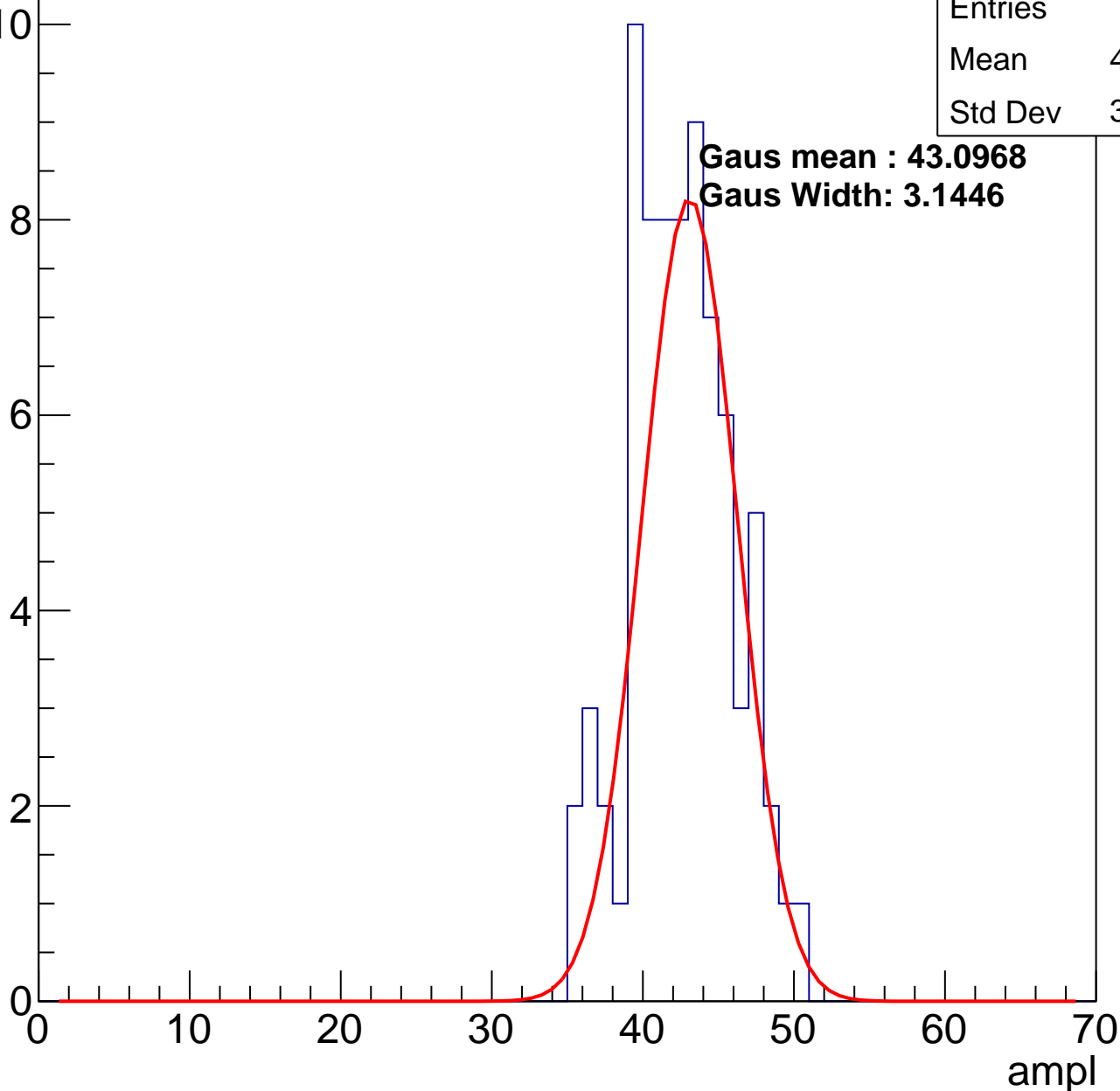
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	76
Mean	42.07
Std Dev	3.346

**Gaus mean : 43.0968**

**Gaus Width: 3.1446**

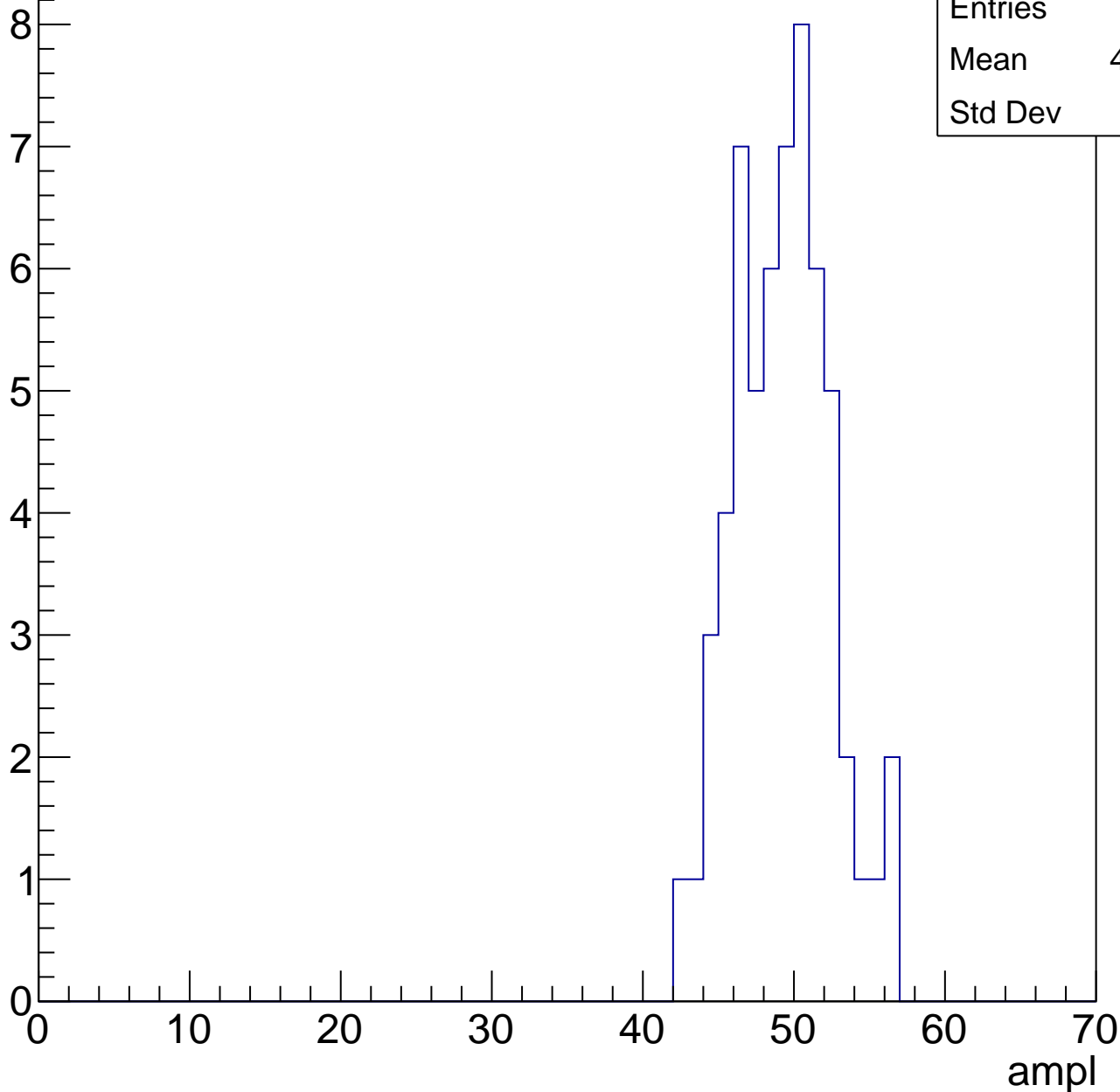


# B1L003S, U3-ch70, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	48.78
Std Dev	3.13

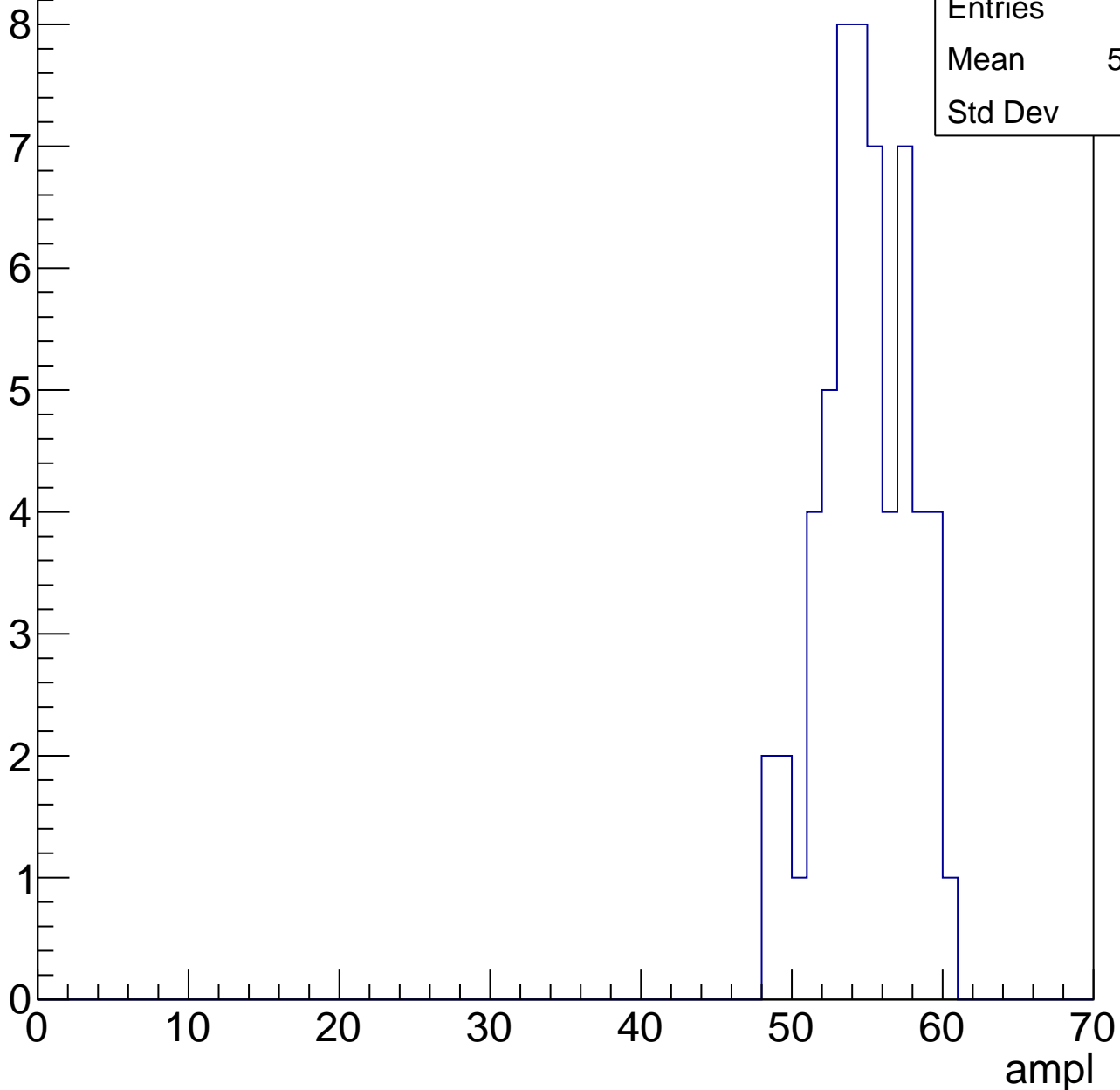


# B1L003S, U3-ch70, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	54.39
Std Dev	2.9

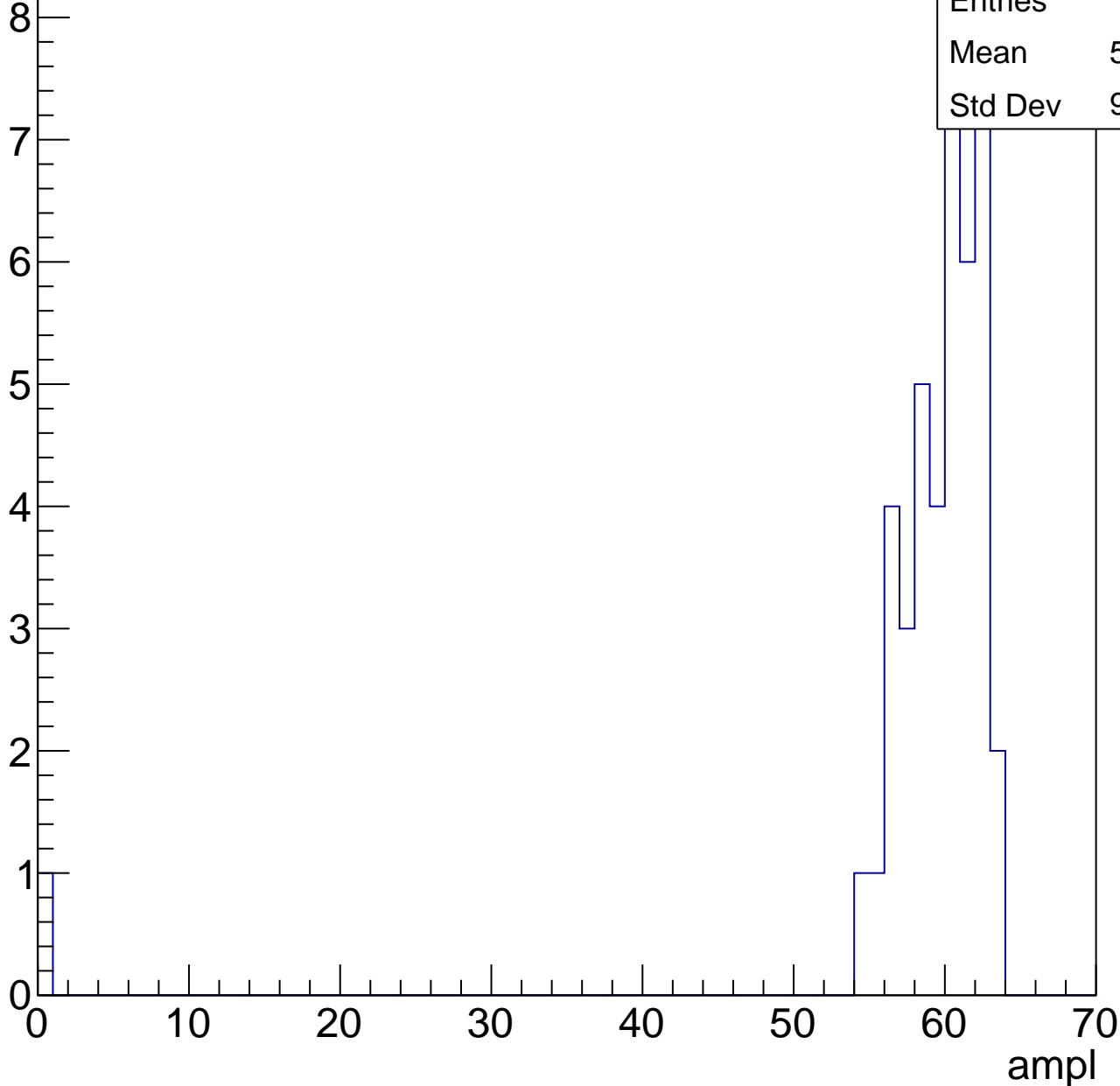


# B1L003S, U3-ch70, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	43
Mean	58.09
Std Dev	9.246

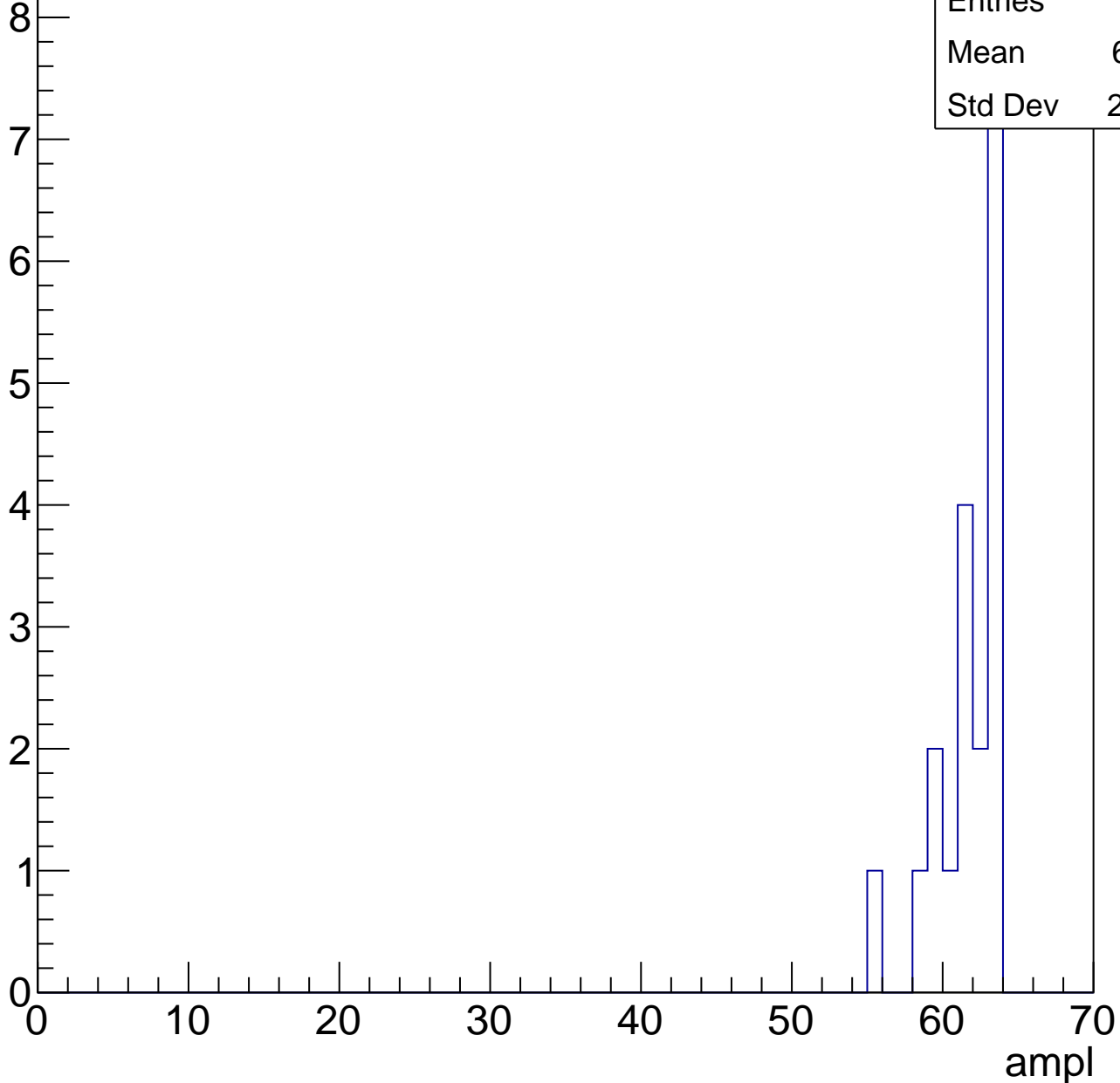


# B1L003S, U3-ch70, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	19
Mean	61.21
Std Dev	2.142

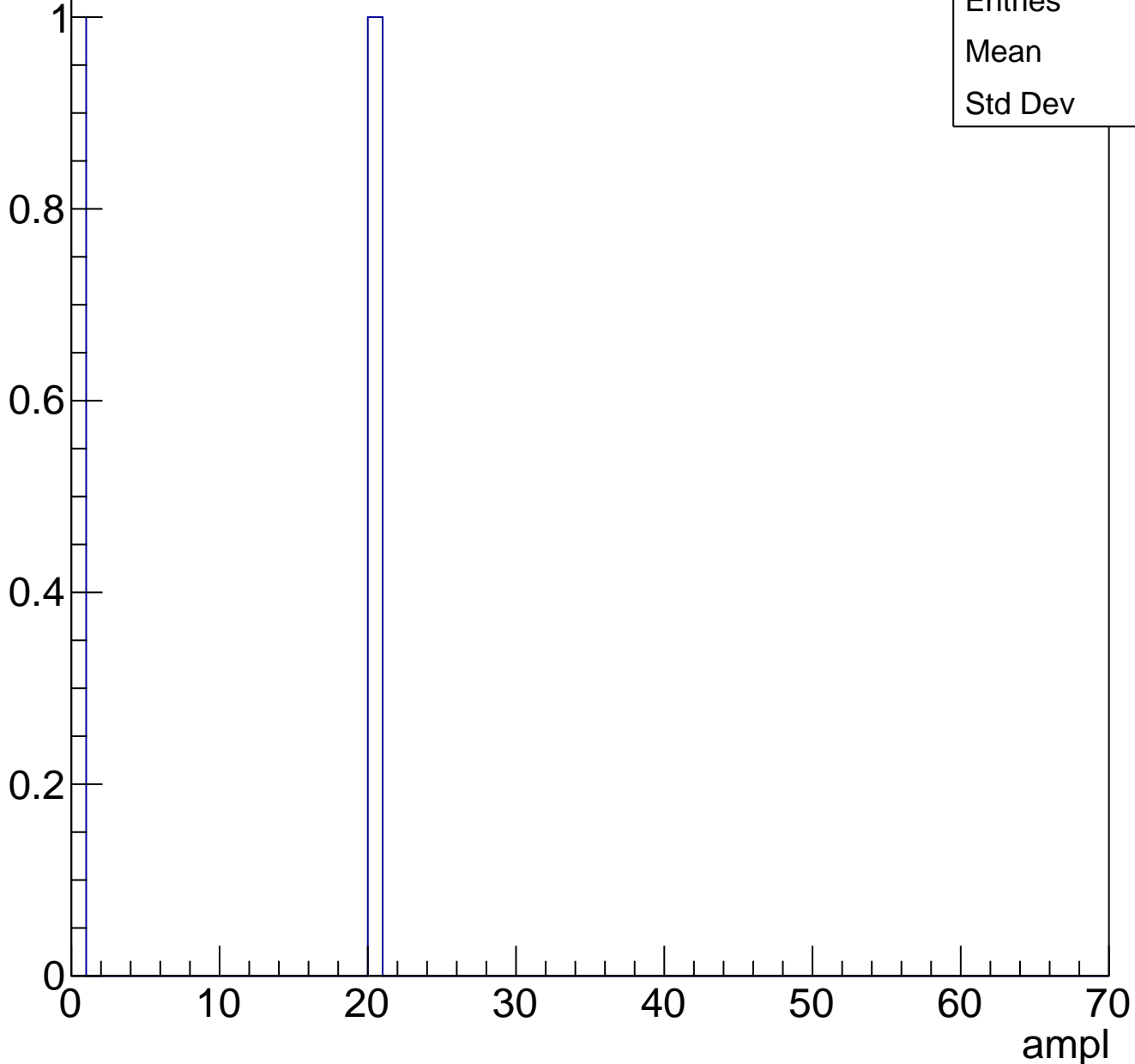




# B1L003S, U3-ch70, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	10
Std Dev	10

# B1L003S, U3-ch71, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	83
Mean	28.3
Std Dev	5.762

**Gaus mean : 29.5842**

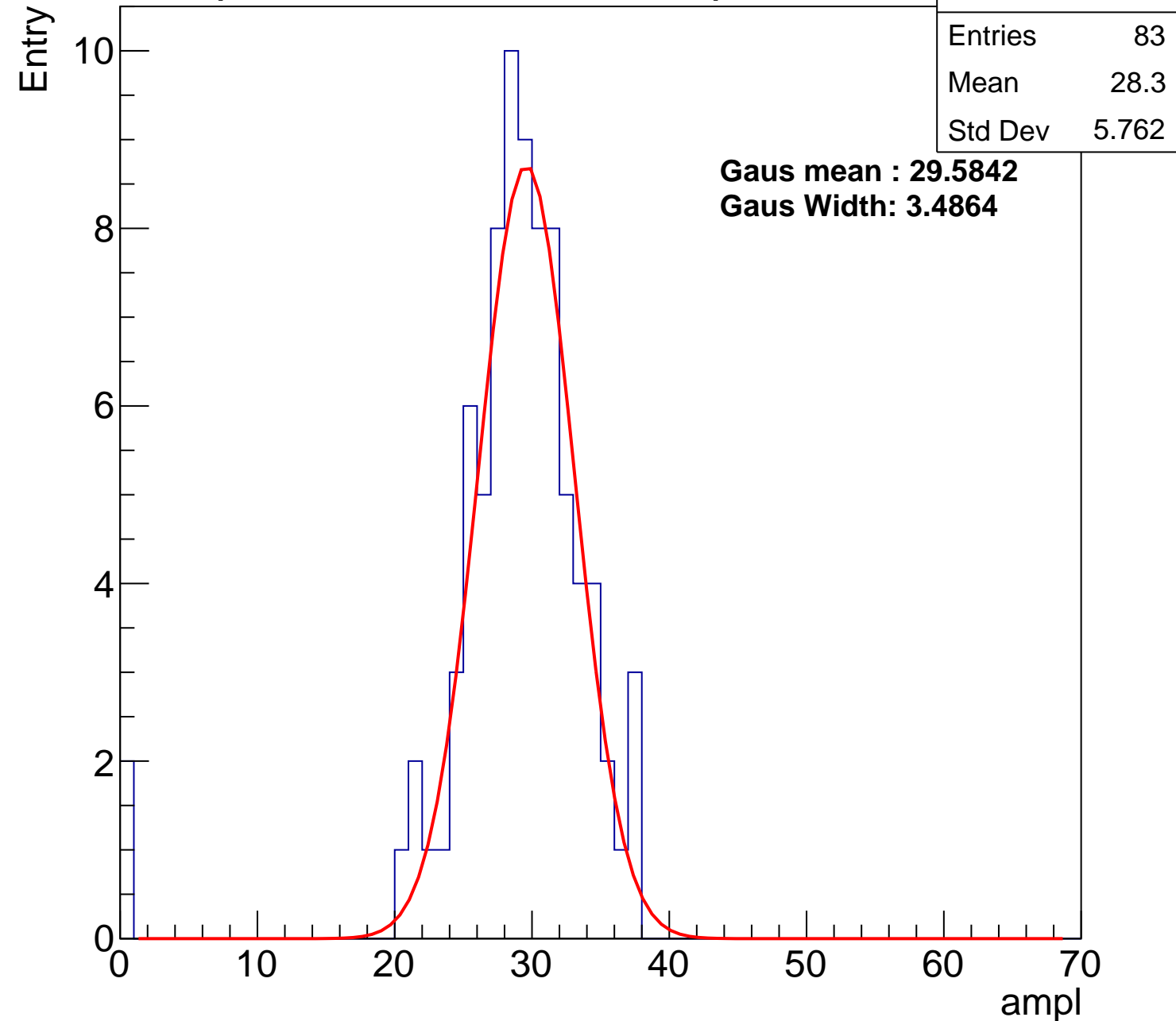
**Gaus Width: 3.4864**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U3-ch71, adc1

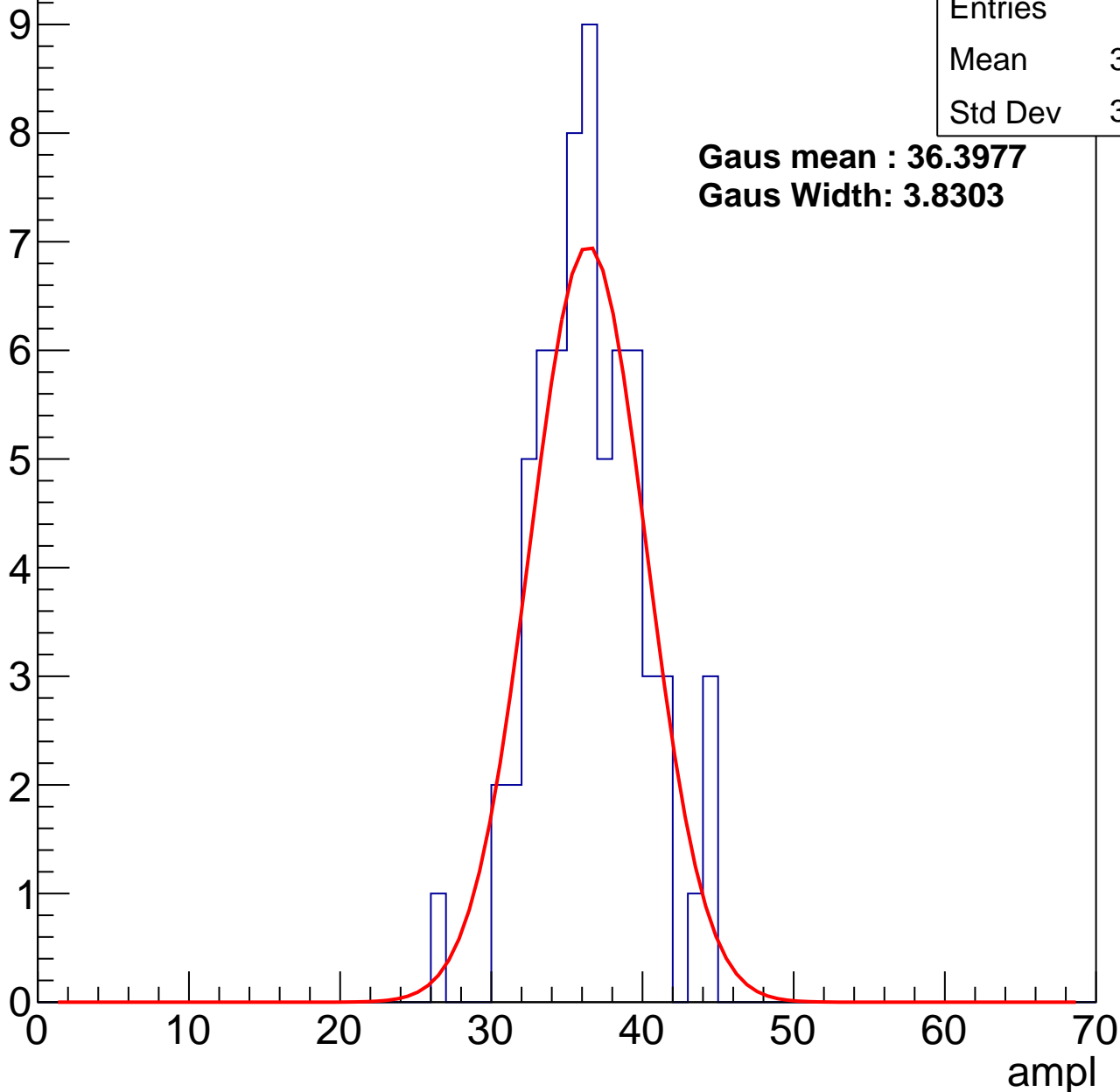
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	36.05
Std Dev	3.557

**Gaus mean : 36.3977**

**Gaus Width: 3.8303**



# B1L003S, U3-ch71, adc2

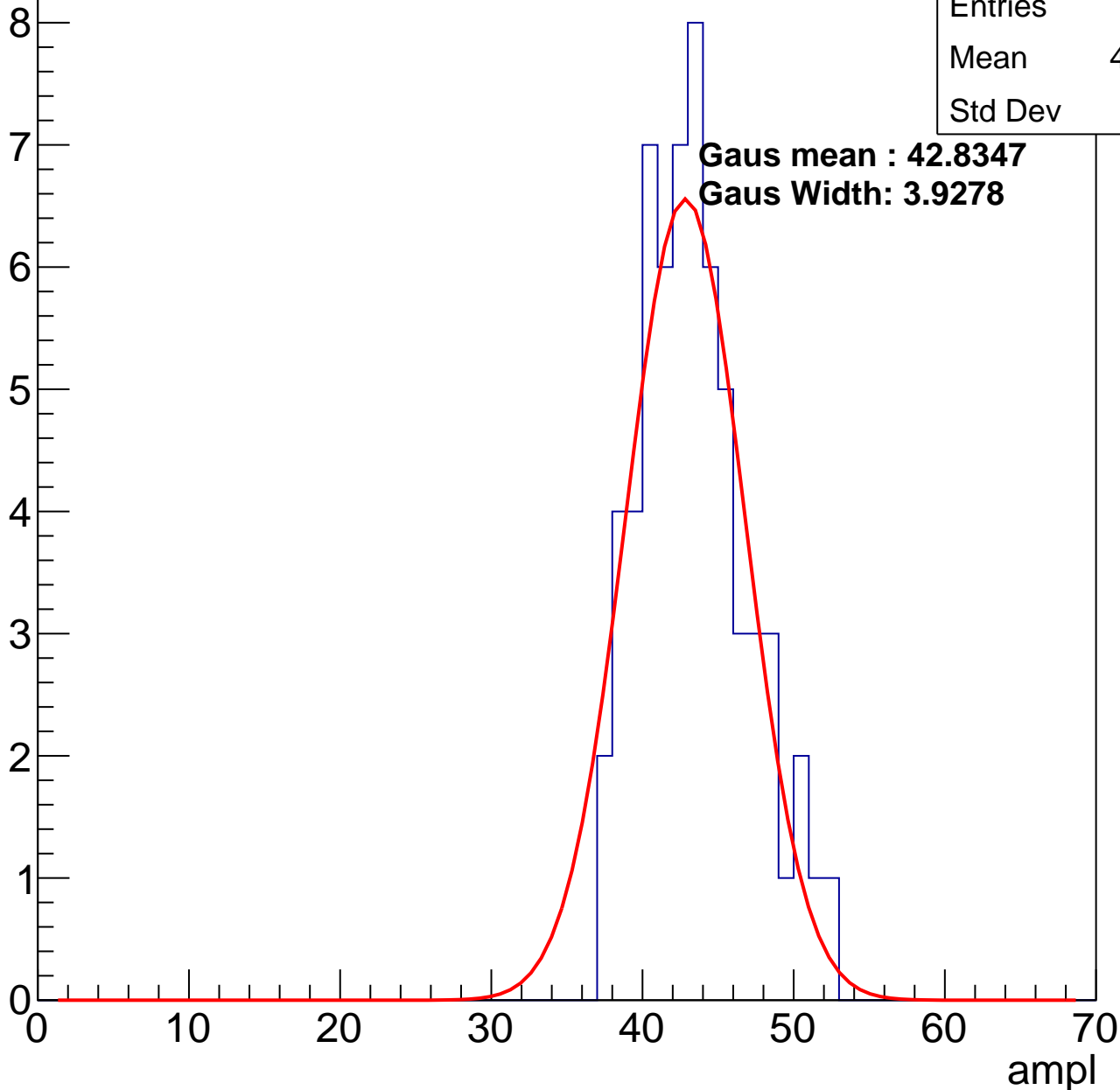
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	43.02
Std Dev	3.53

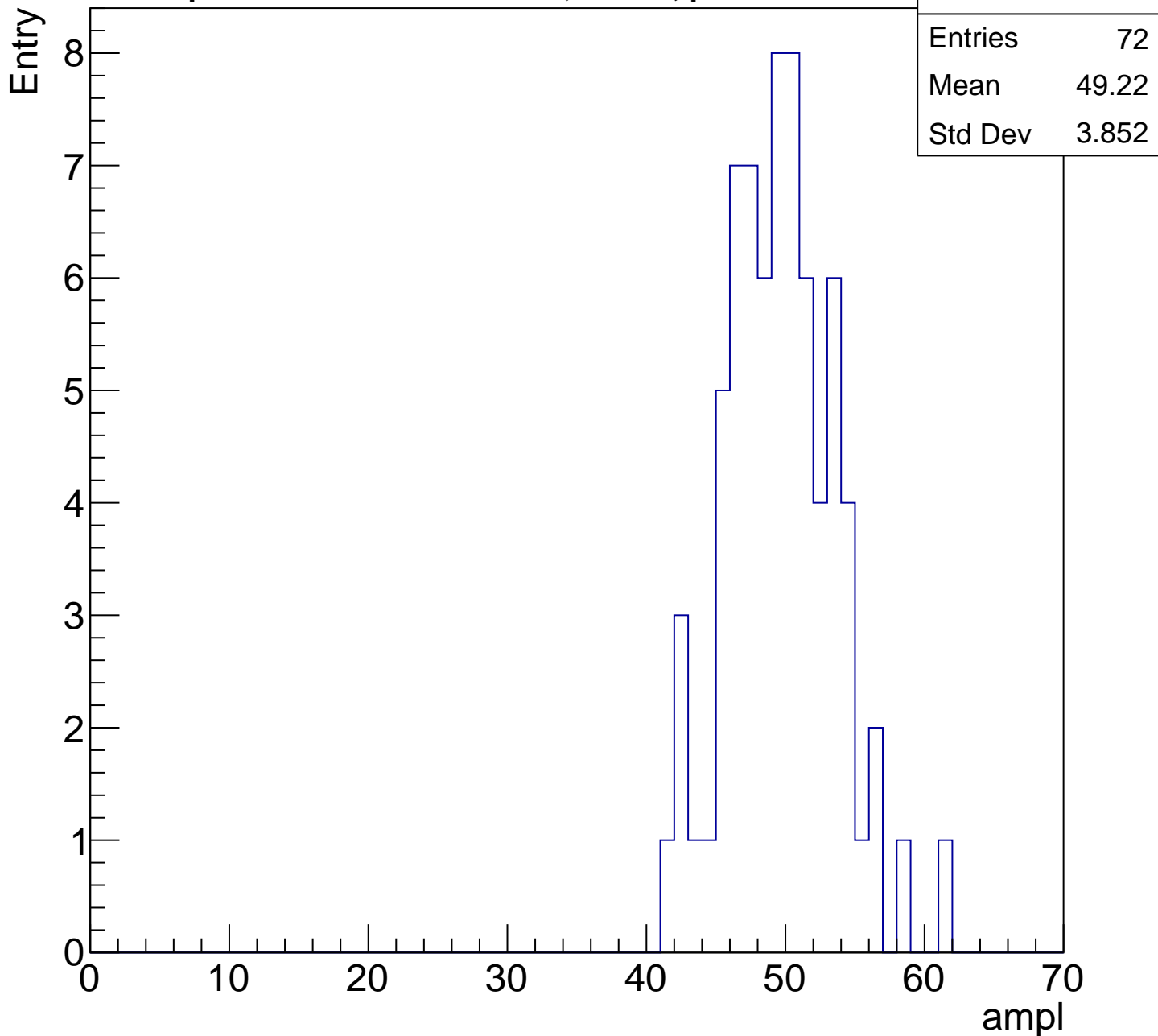
**Gaus mean : 42.8347**

**Gaus Width: 3.9278**



# B1L003S, U3-ch71, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

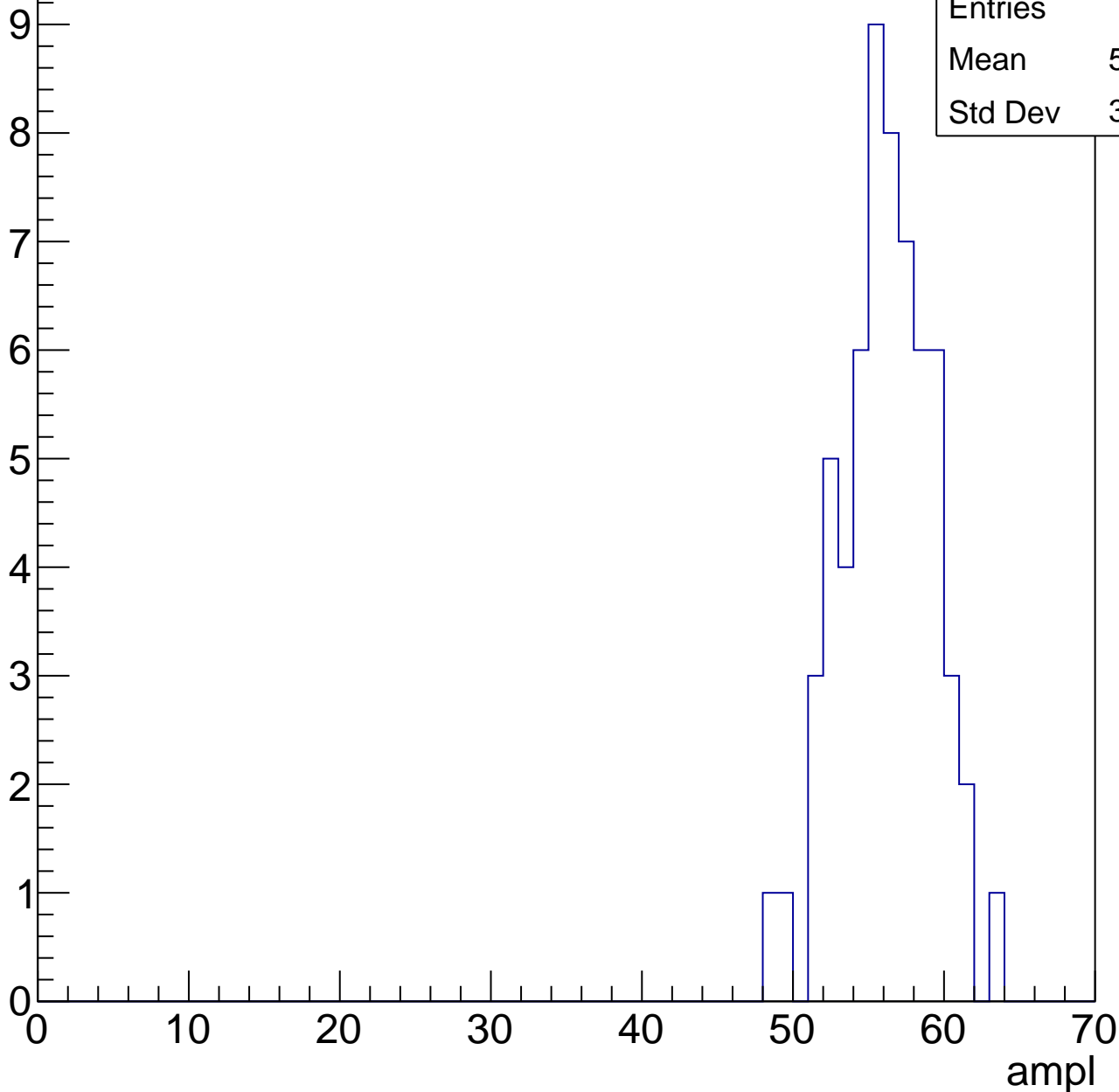


# B1L003S, U3-ch71, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	55.73
Std Dev	3.017



# B1L003S, U3-ch71, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

7

6

5

4

3

2

1

0

Entries	36
Mean	60.58
Std Dev	1.816

ampl

10

20

30

40

50

60

70

# B1L003S, U3-ch71, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

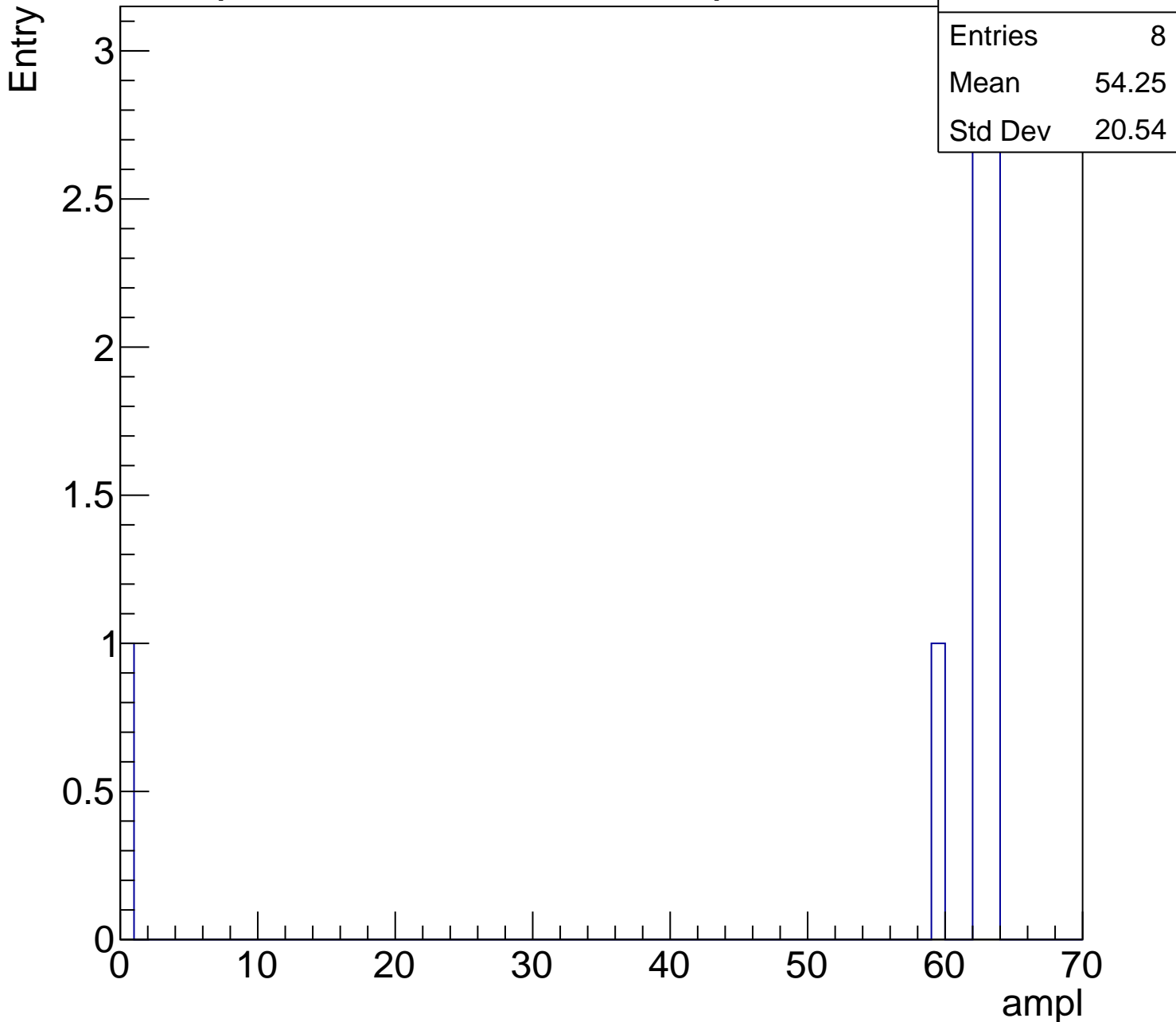
50

60

70

ampl

Entries	8
Mean	54.25
Std Dev	20.54





# B1L003S, U3-ch71, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U3-ch72, adc0

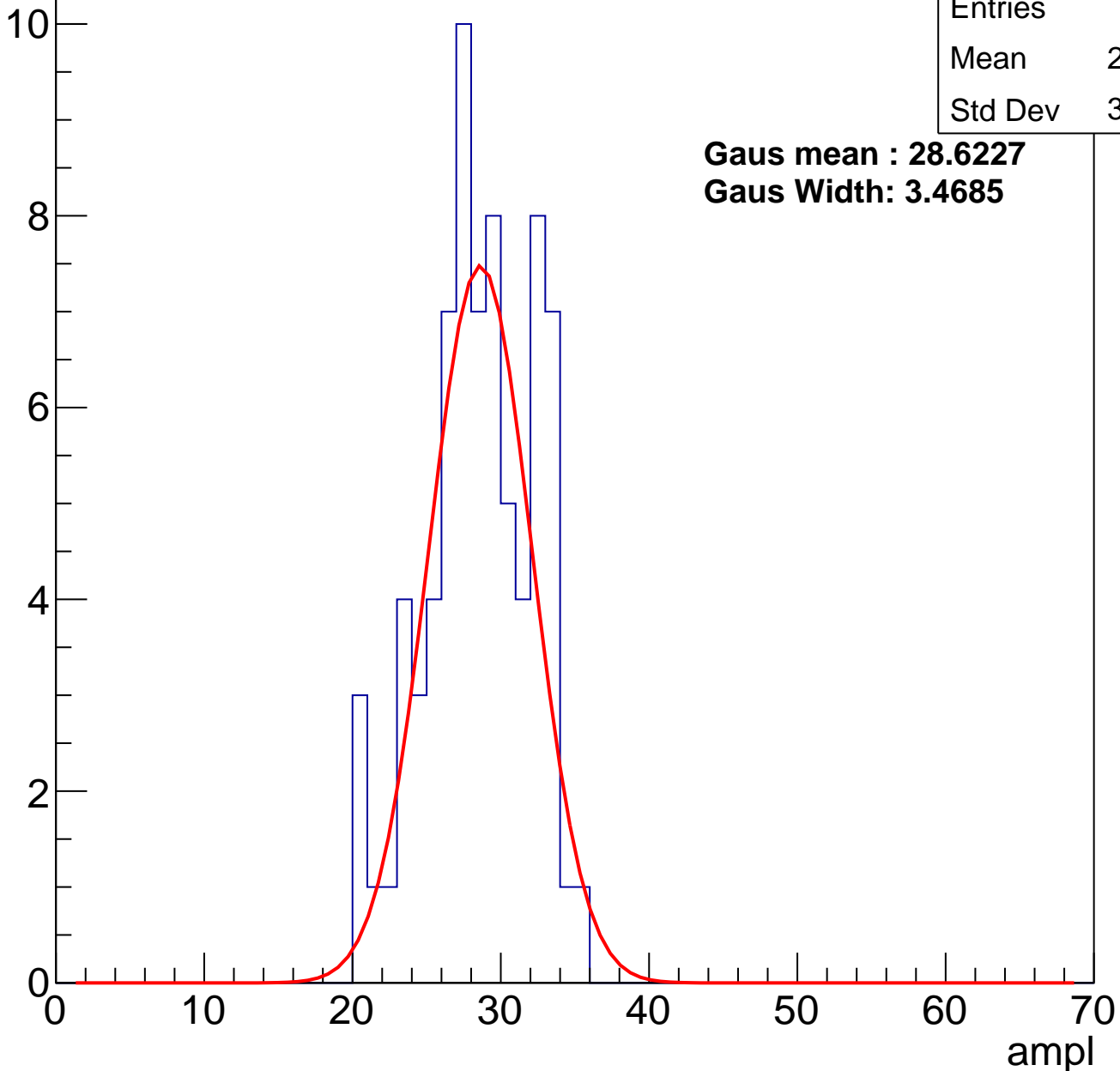
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	74
Mean	28.07
Std Dev	3.584

**Gaus mean : 28.6227**

**Gaus Width: 3.4685**

Entry



# B1L003S, U3-ch72, adc1

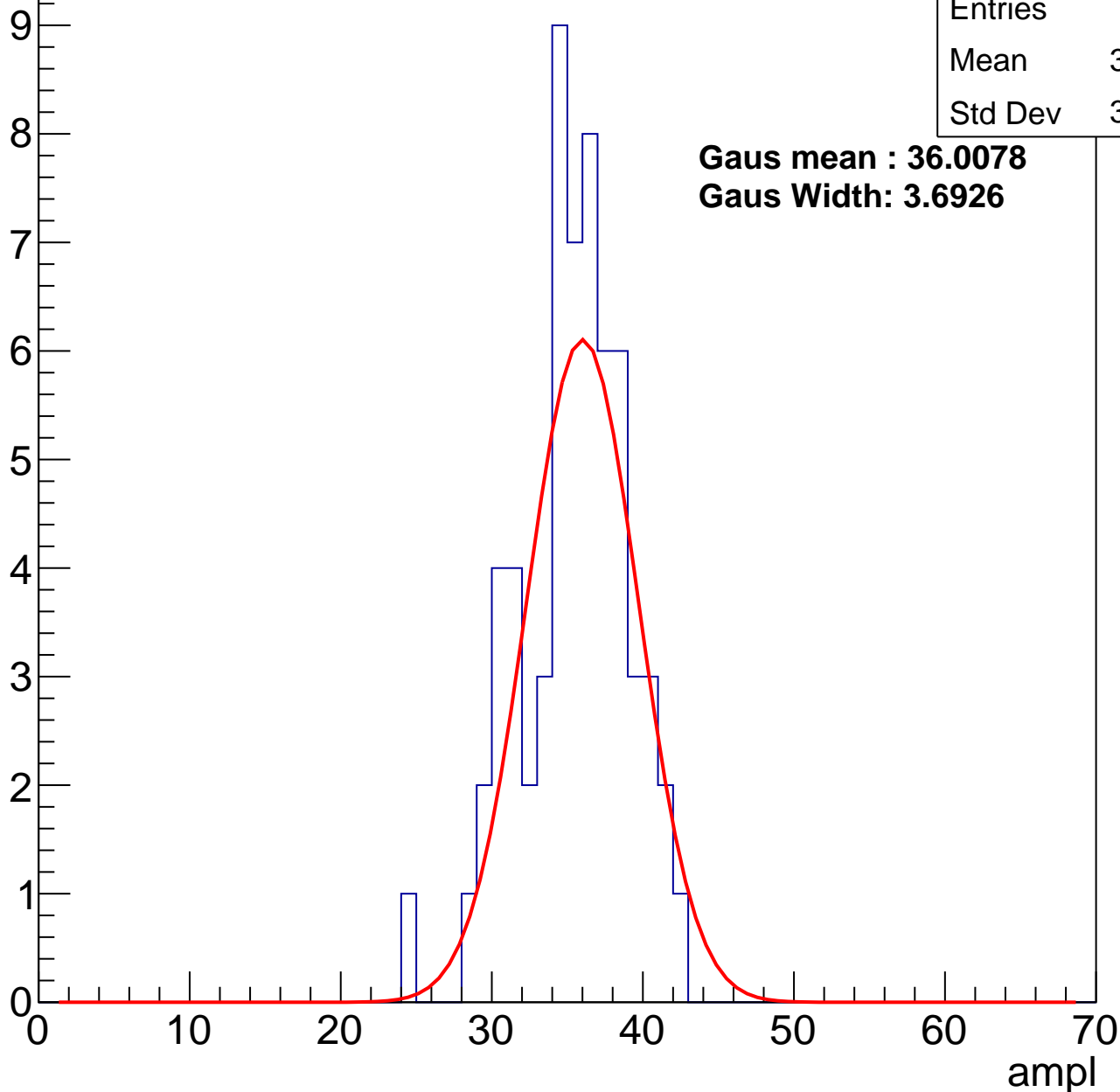
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	34.95
Std Dev	3.535

**Gaus mean : 36.0078**

**Gaus Width: 3.6926**



# B1L003S, U3-ch72, adc2

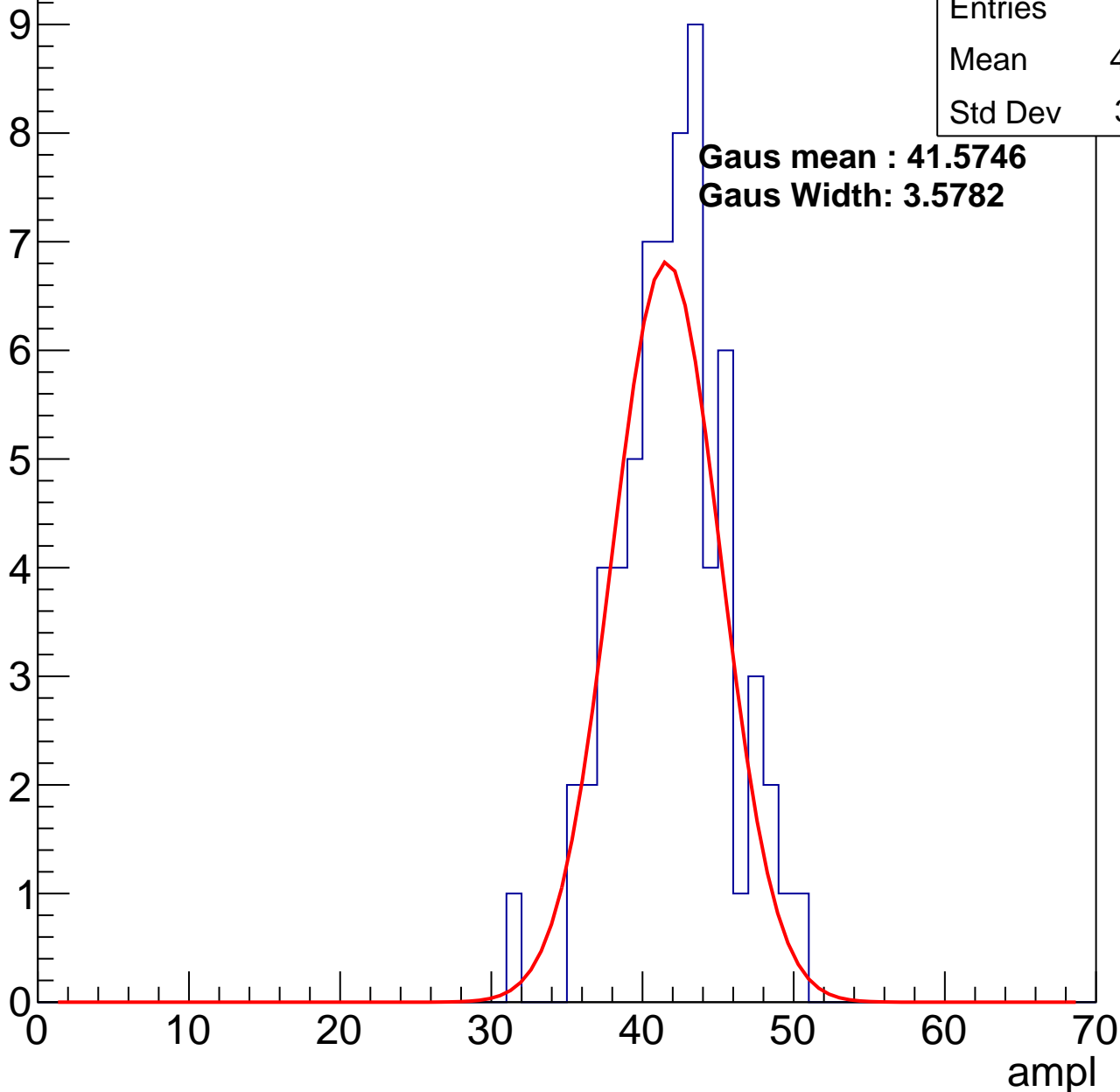
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	41.58
Std Dev	3.621

**Gaus mean : 41.5746**

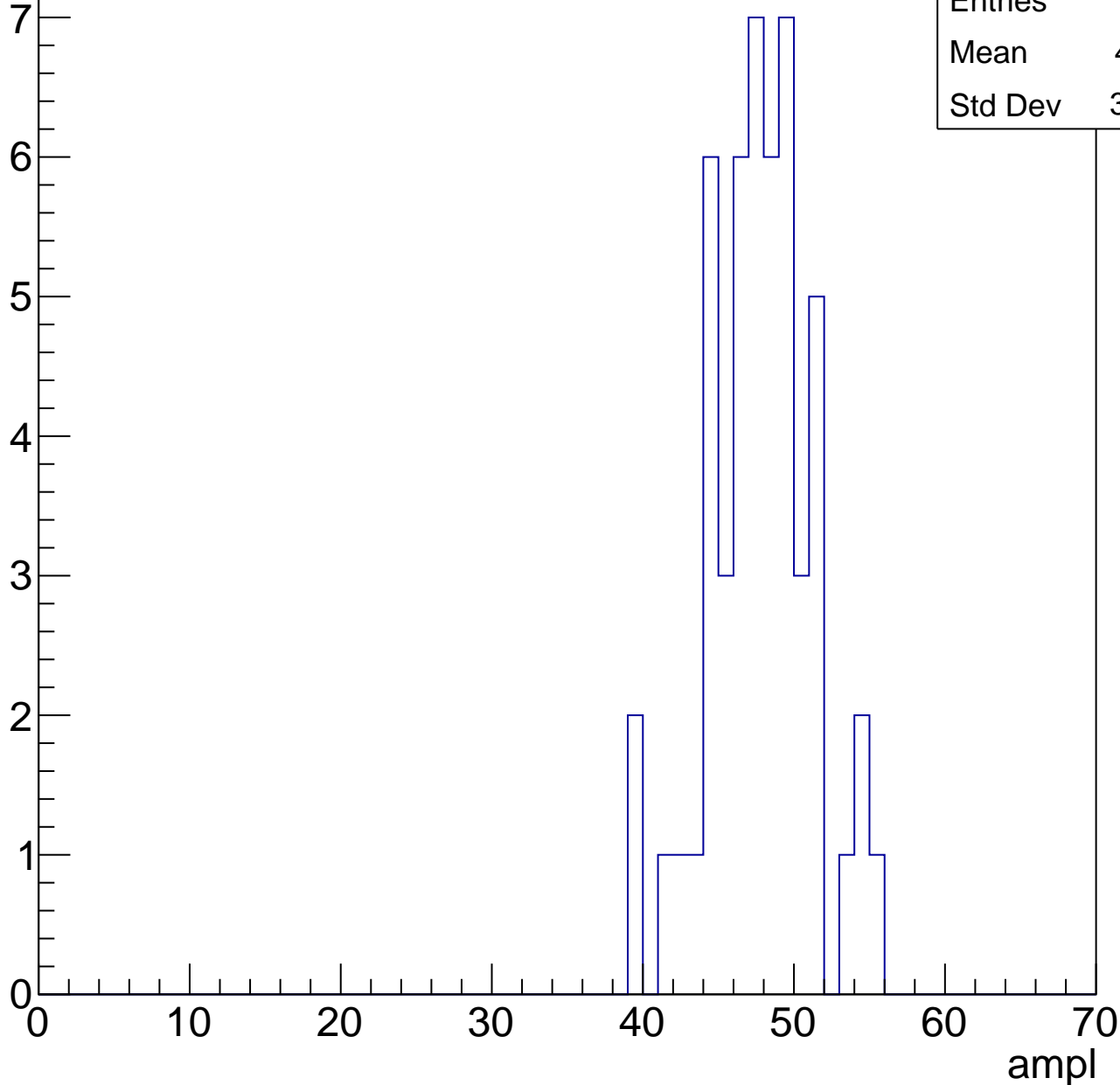
**Gaus Width: 3.5782**



# B1L003S, U3-ch72, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

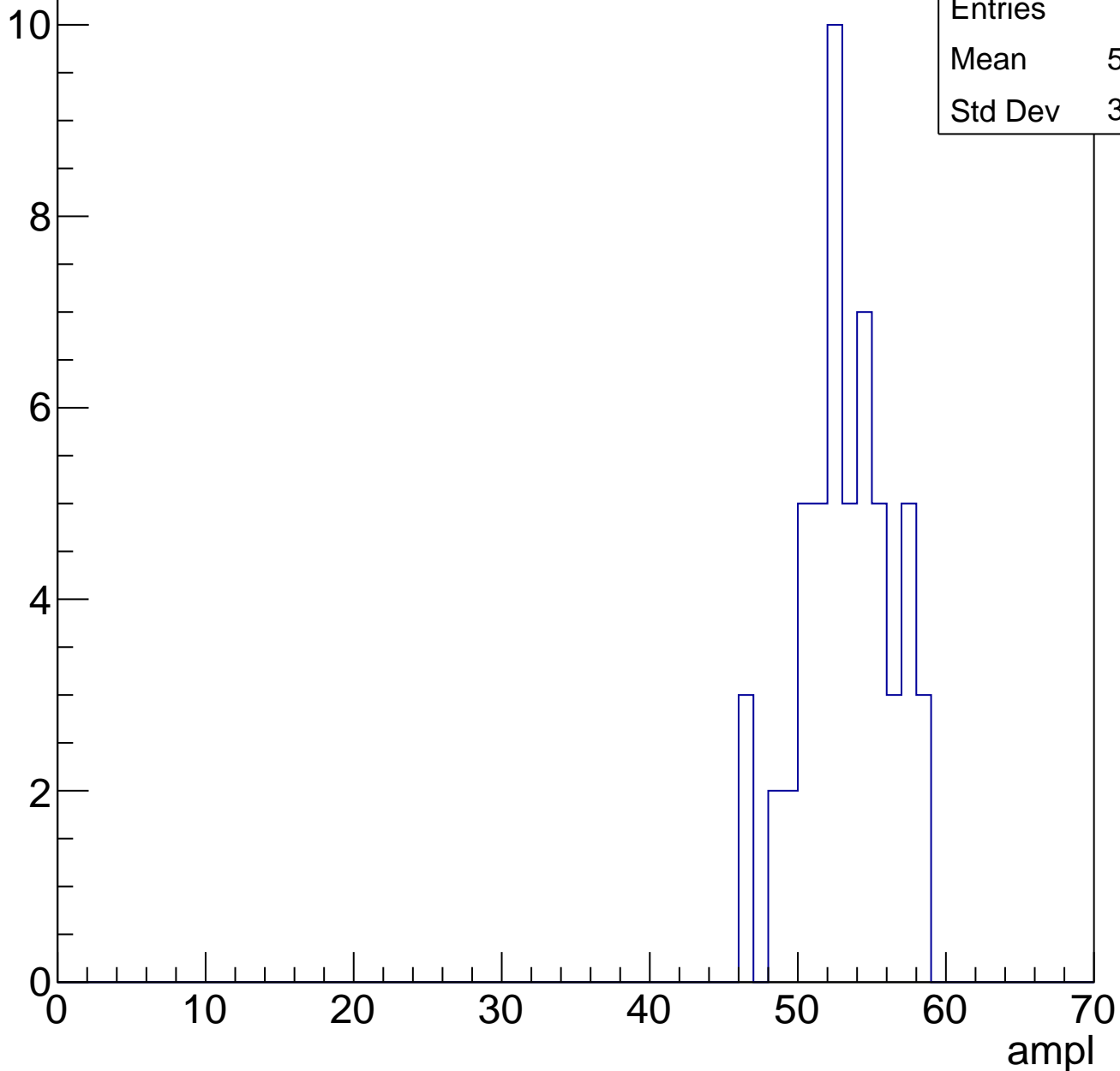


# B1L003S, U3-ch72, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	55
Mean	52.76
Std Dev	3.045

Entry

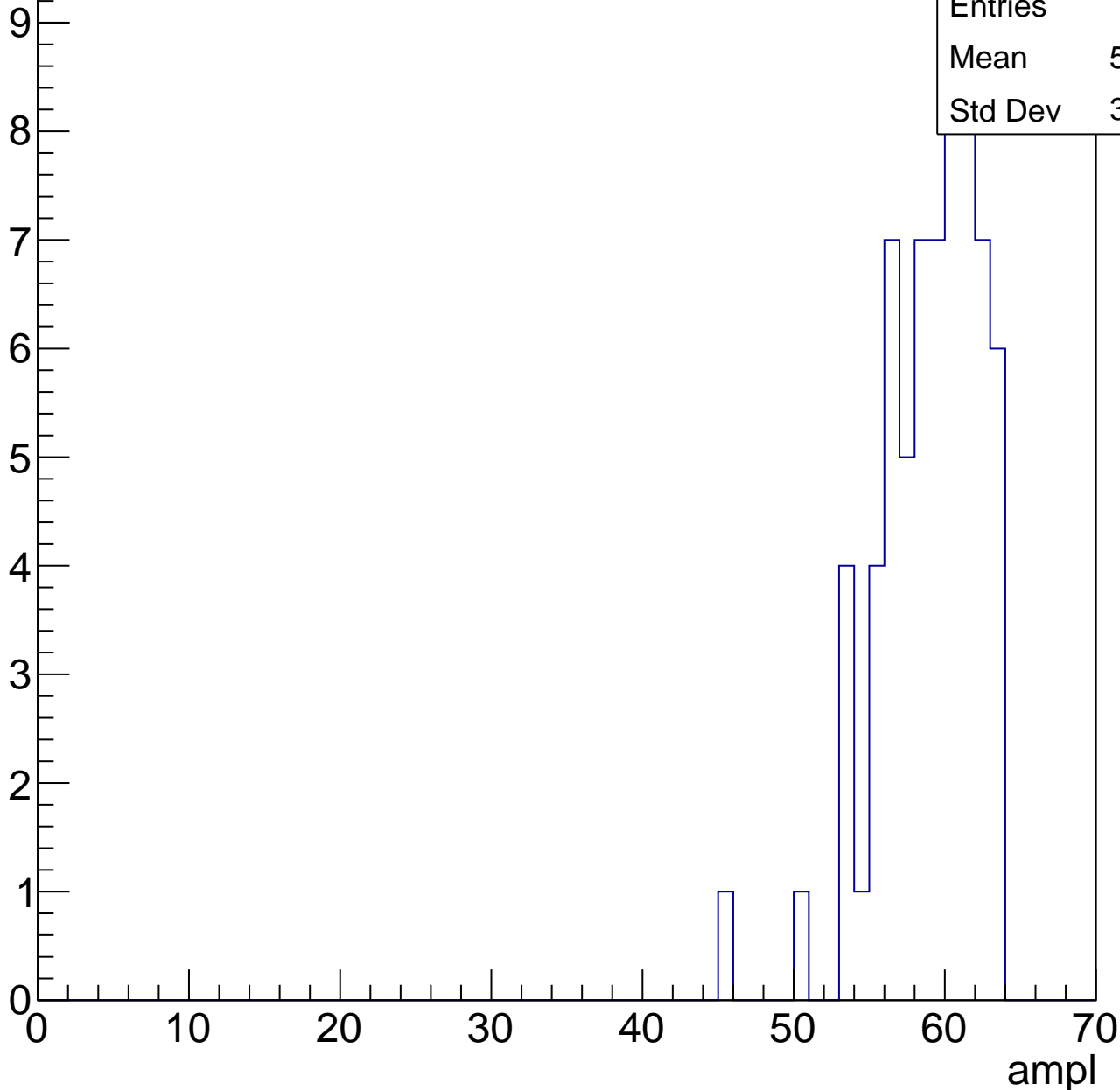


# B1L003S, U3-ch72, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	58.46
Std Dev	3.413



# B1L003S, U3-ch72, adc6

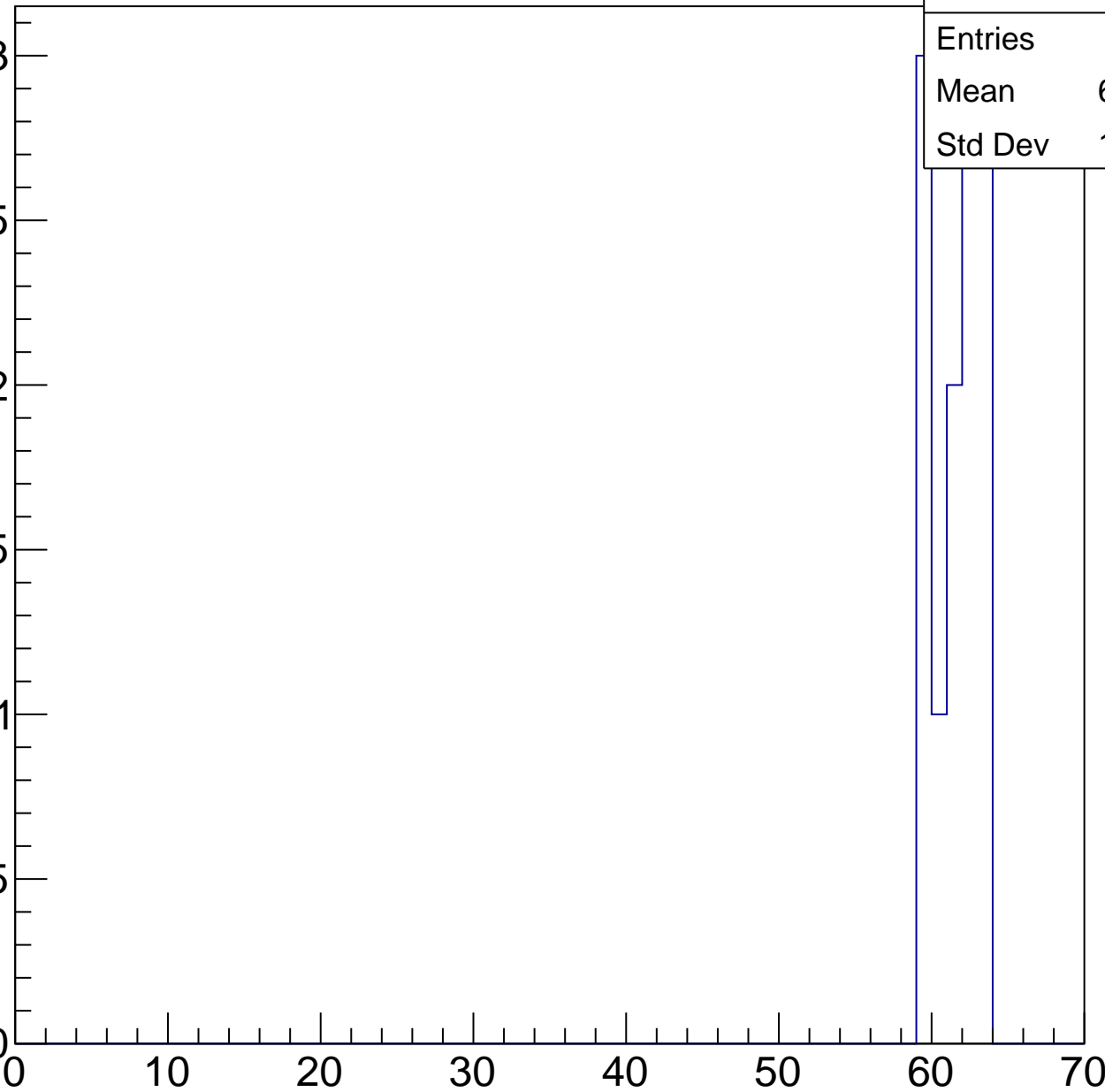
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

3  
2.5  
2  
1.5  
1  
0.5  
0

Entries	12
Mean	61.17
Std Dev	1.518

ampl

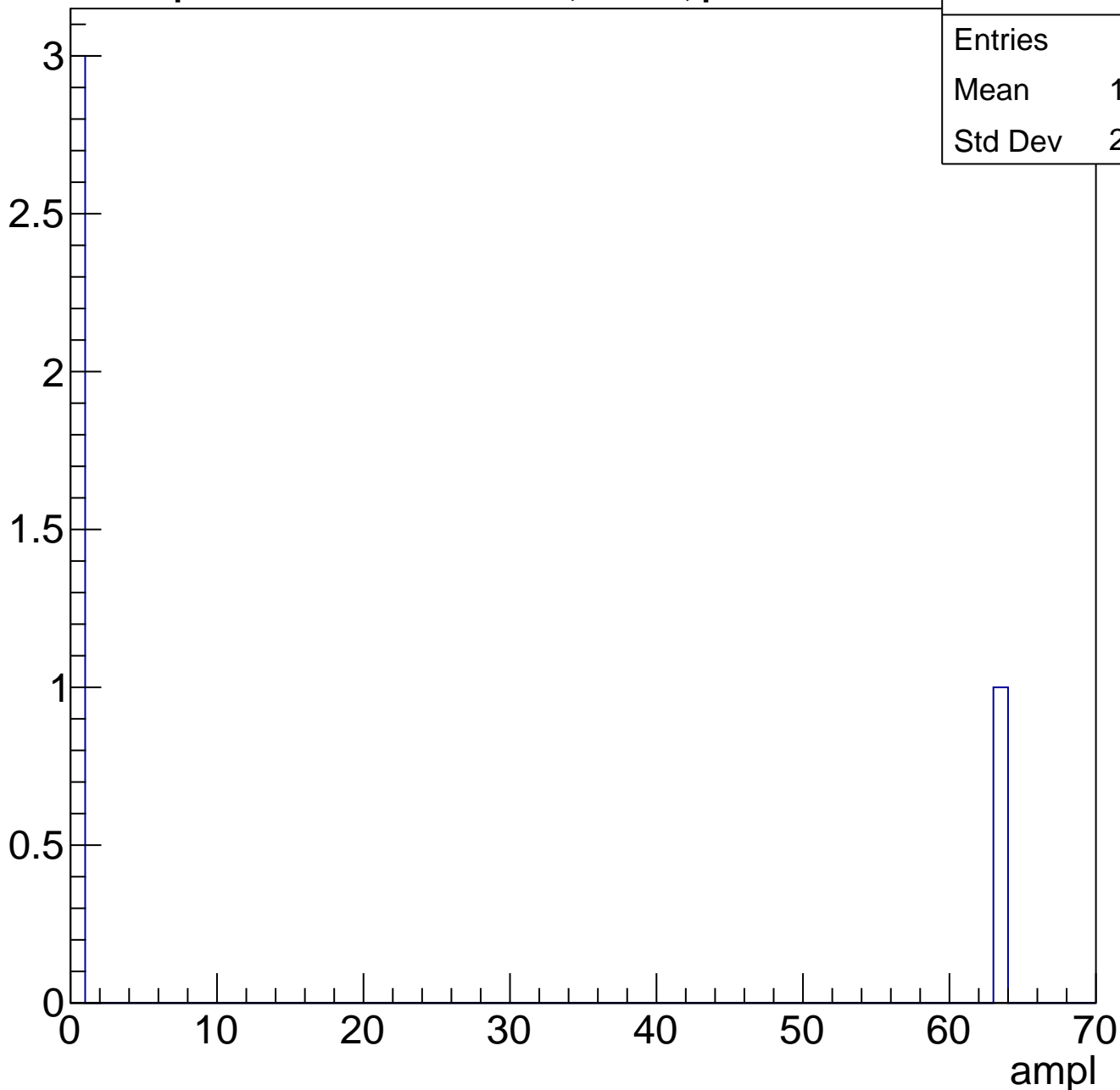




# B1L003S, U3-ch72, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U3-ch73, adc0

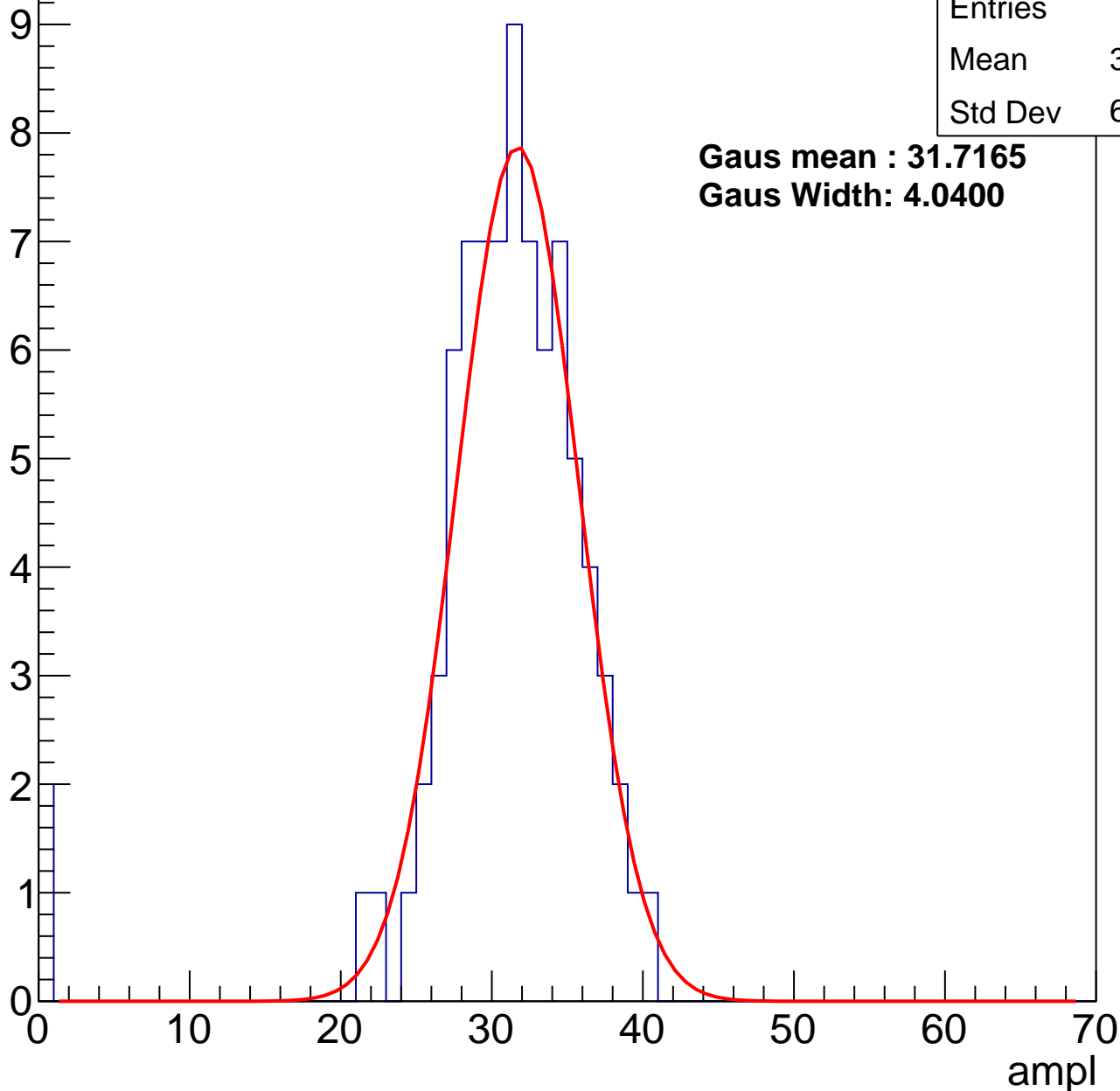
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	82
Mean	30.37
Std Dev	6.134

**Gaus mean : 31.7165**

**Gaus Width: 4.0400**



# B1L003S, U3-ch73, adc1

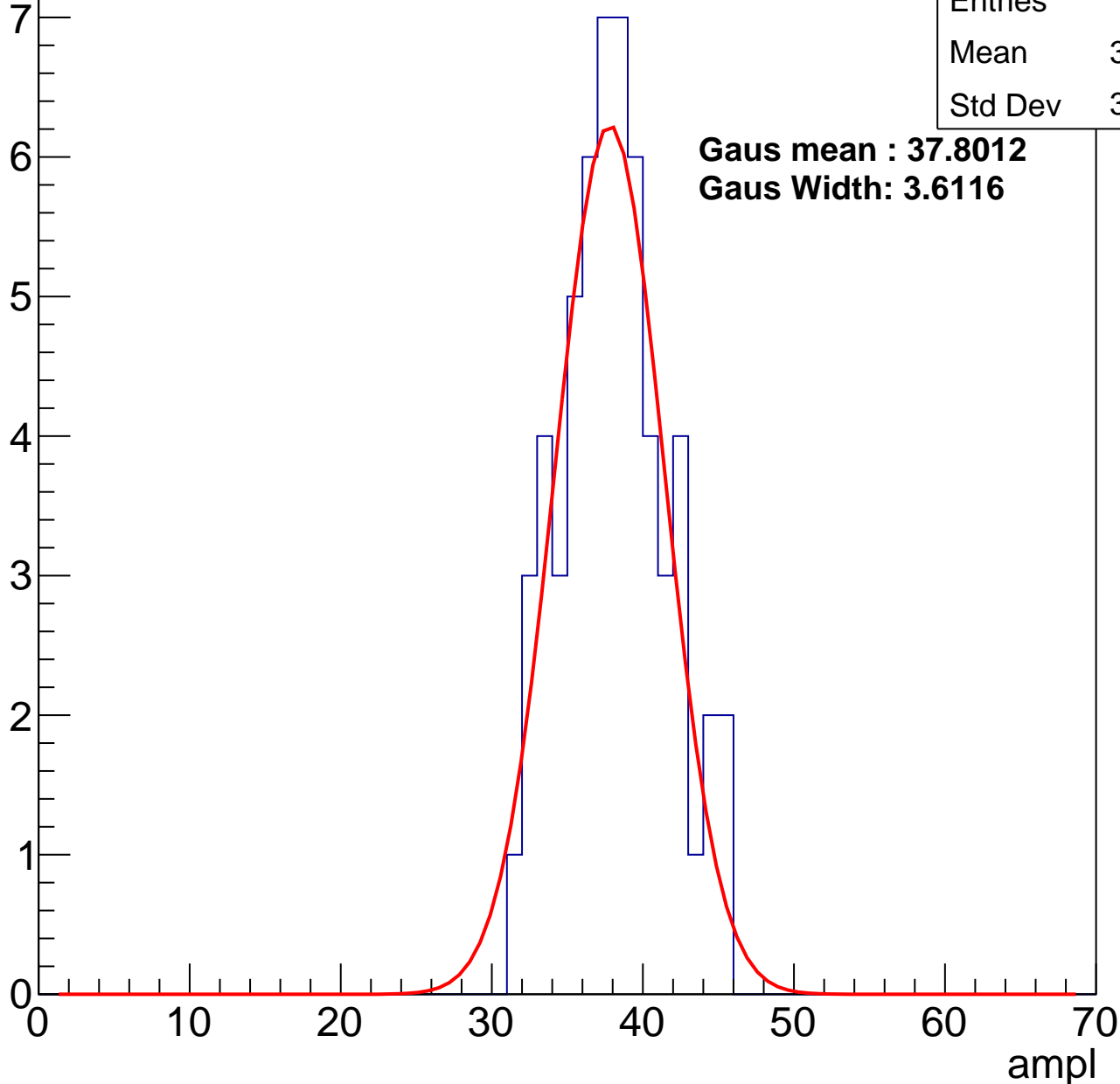
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	37.64
Std Dev	3.428

**Gaus mean : 37.8012**

**Gaus Width: 3.6116**



# B1L003S, U3-ch73, adc2

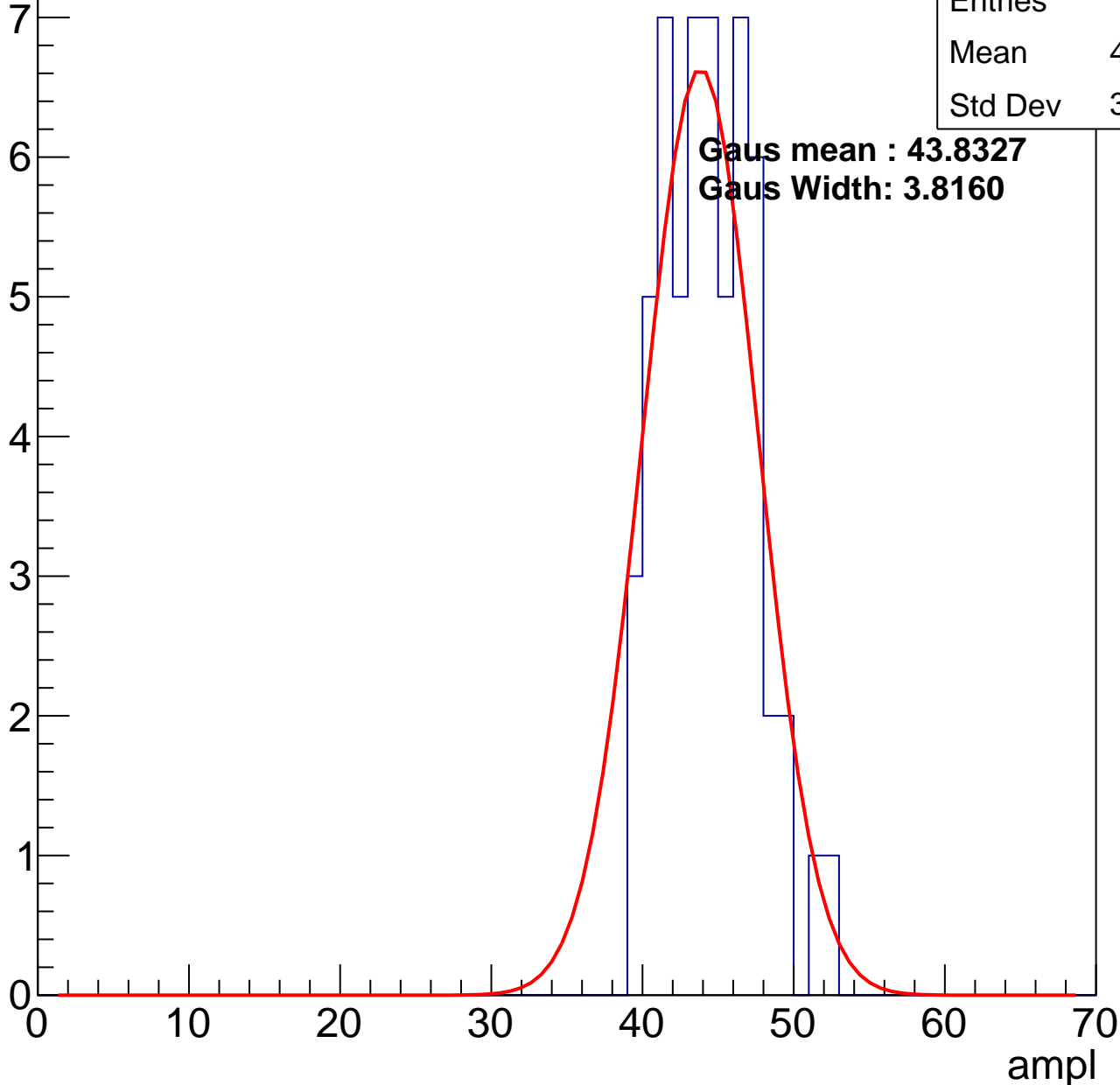
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	43.95
Std Dev	3.014

**Gaus mean : 43.8327**

**Gaus Width: 3.8160**

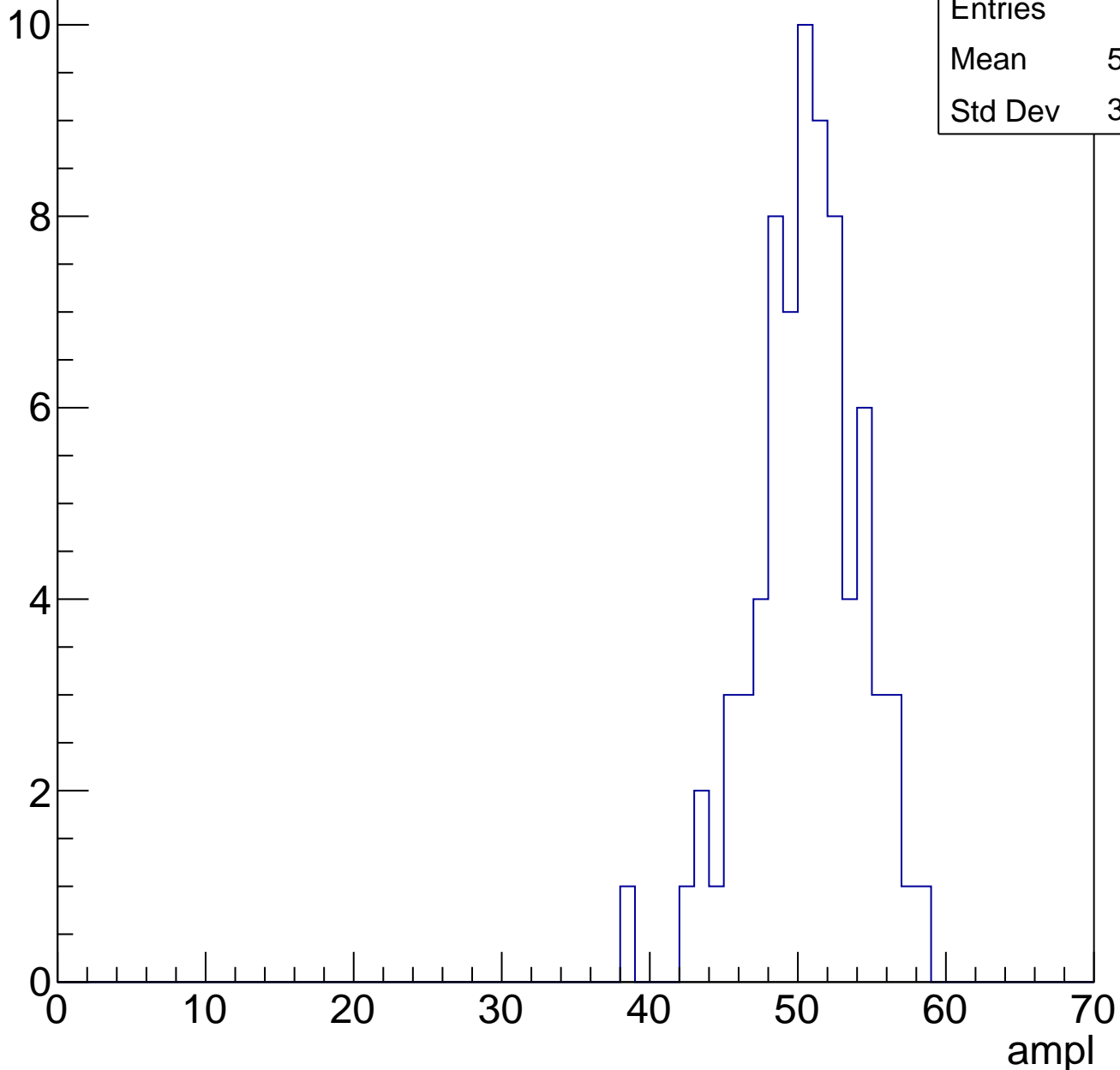


# B1L003S, U3-ch73, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	75
Mean	50.09
Std Dev	3.667



# B1L003S, U3-ch73, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

6

5

4

3

2

1

0

Entries 44

Mean 56.32

Std Dev 2.592

ampl

0

10

20

30

40

50

60

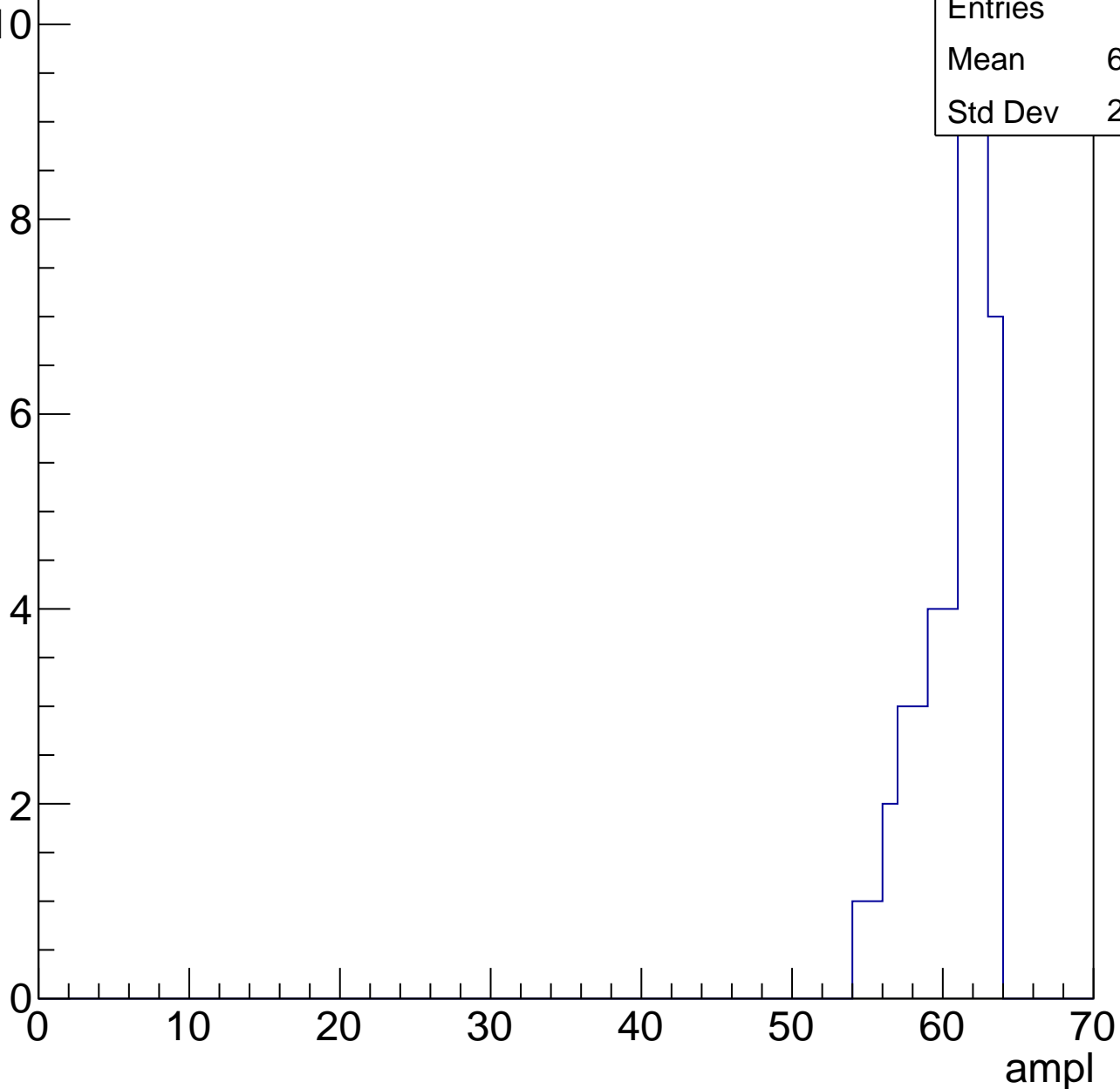
70

# B1L003S, U3-ch73, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

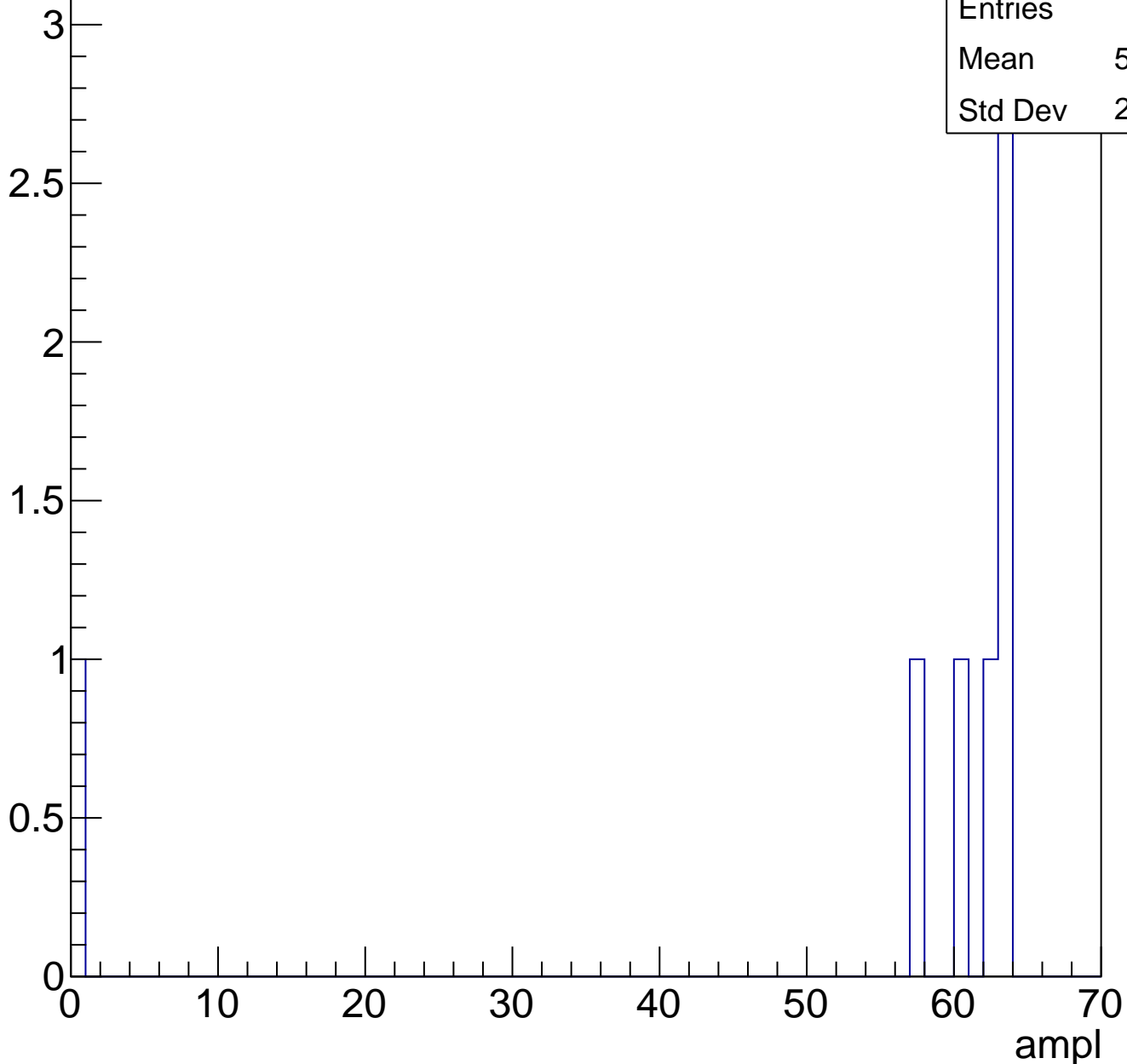
Entries	44
Mean	60.25
Std Dev	2.346



# B1L003S, U3-ch73, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch73, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U3-ch74, adc0

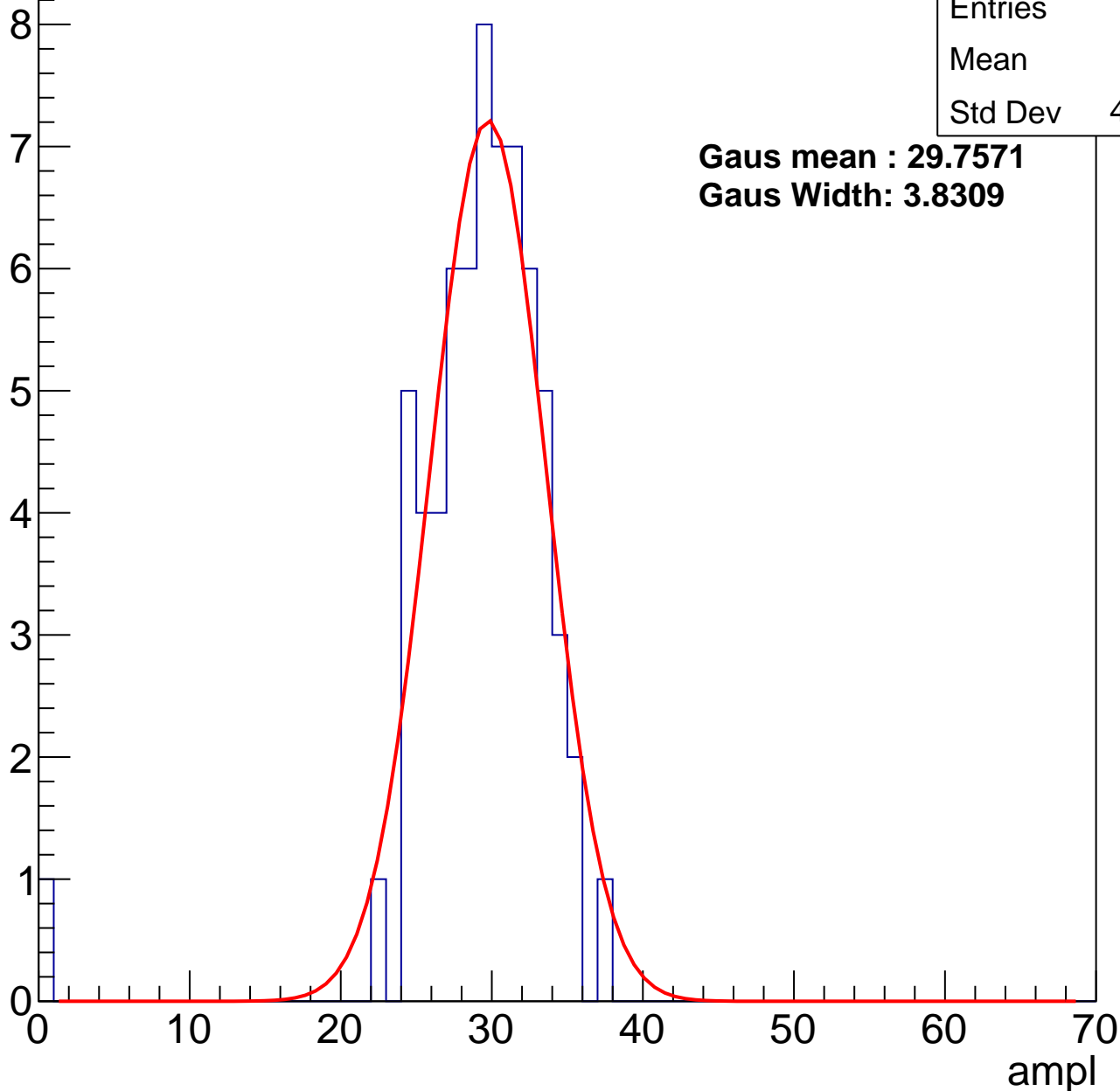
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	28.8
Std Dev	4.803

**Gaus mean : 29.7571**

**Gaus Width: 3.8309**



# B1L003S, U3-ch74, adc1

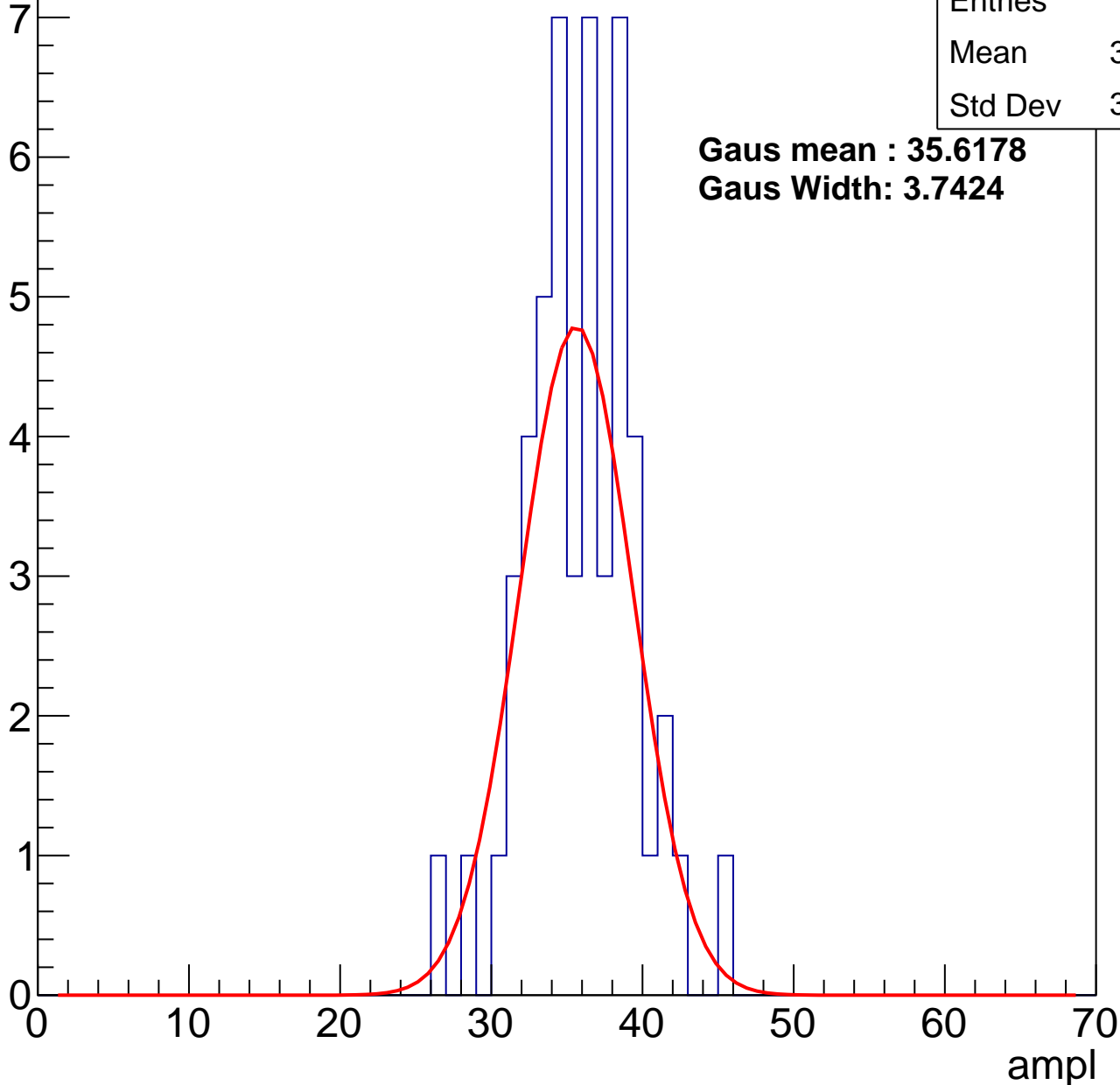
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	51
Mean	35.43
Std Dev	3.566

**Gaus mean : 35.6178**

**Gaus Width: 3.7424**



# B1L003S, U3-ch74, adc2

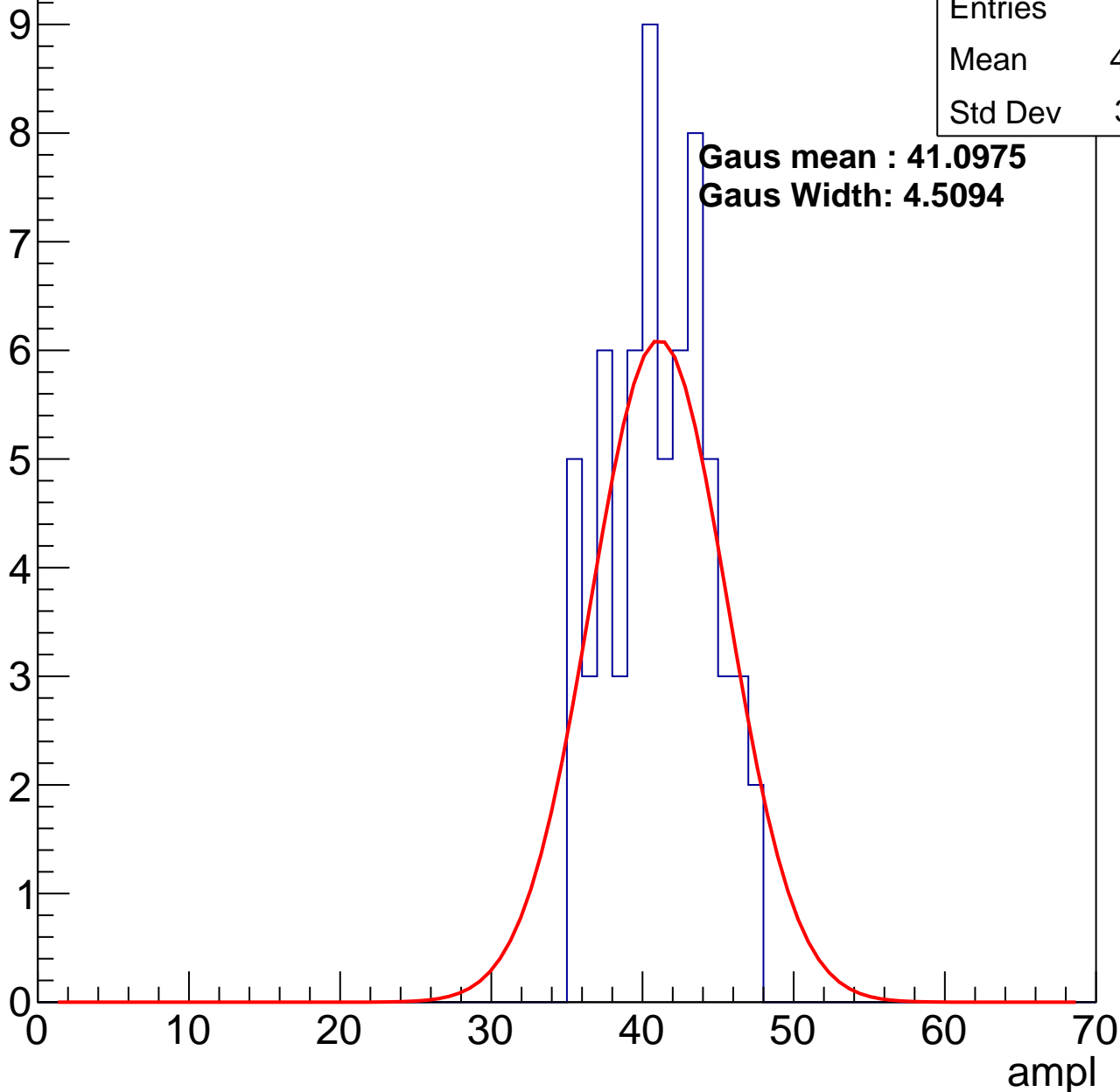
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	40.64
Std Dev	3.261

**Gaus mean : 41.0975**

**Gaus Width: 4.5094**

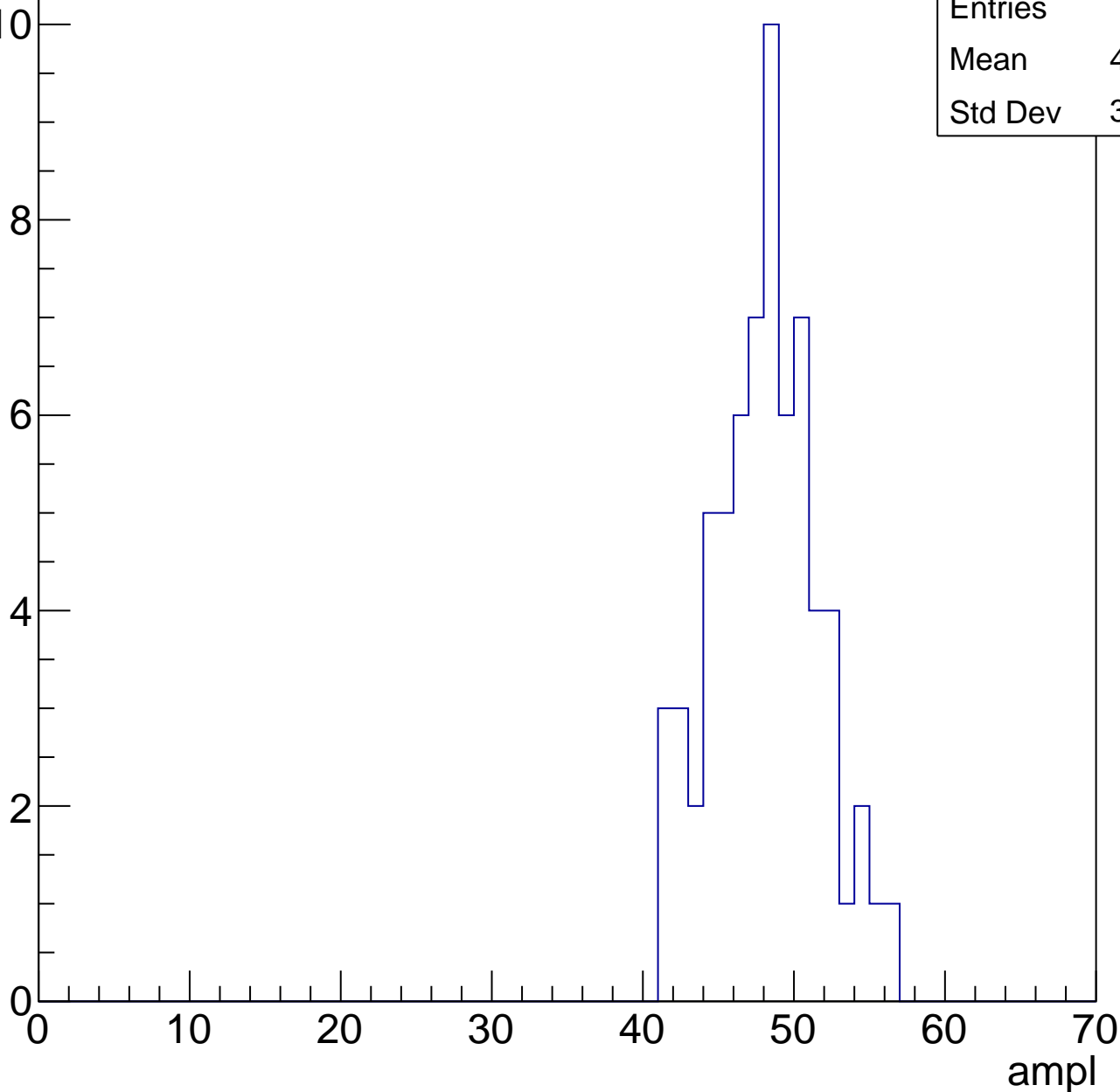


# B1L003S, U3-ch74, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	47.66
Std Dev	3.449

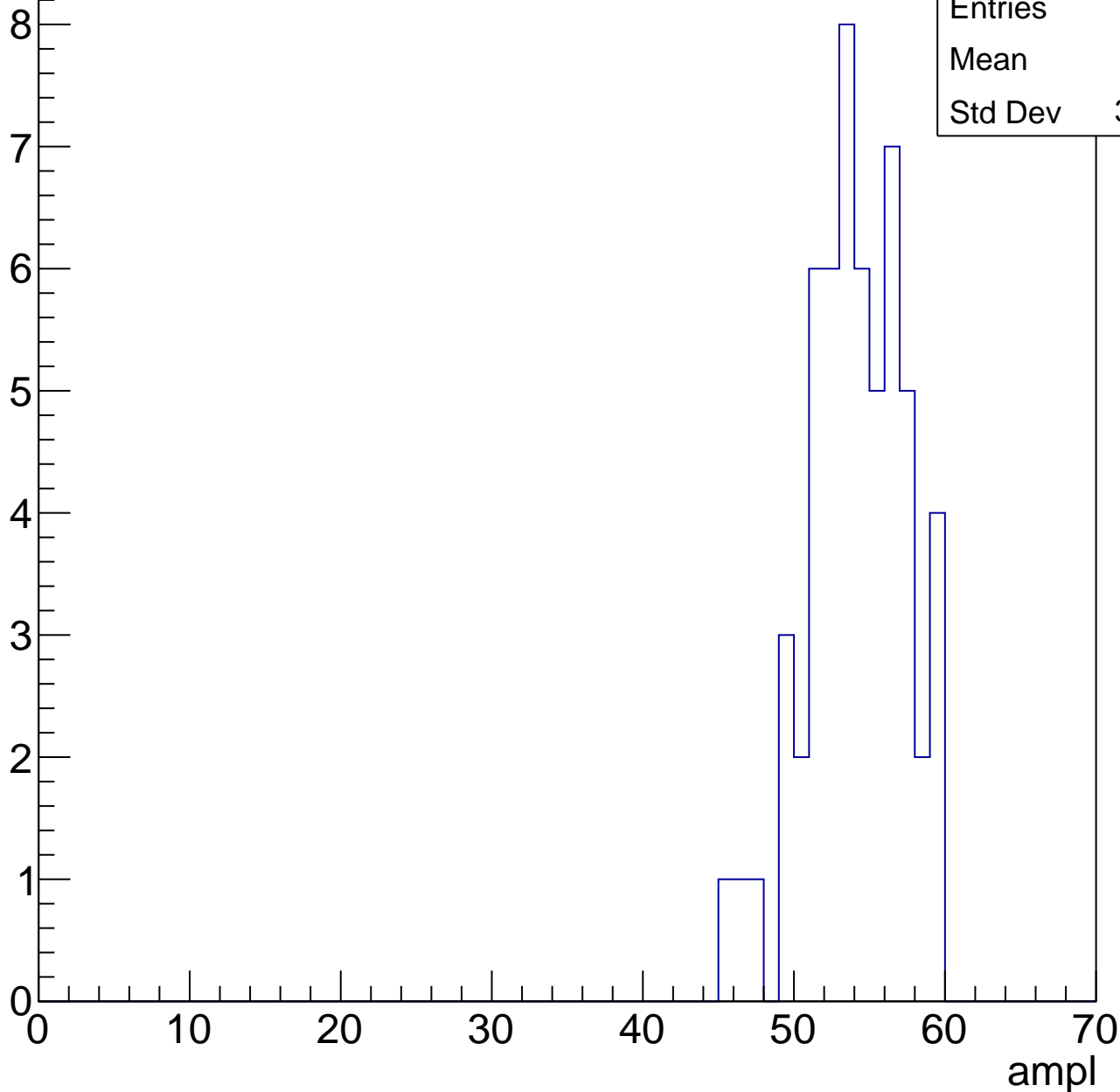


# B1L003S, U3-ch74, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	53.6
Std Dev	3.211

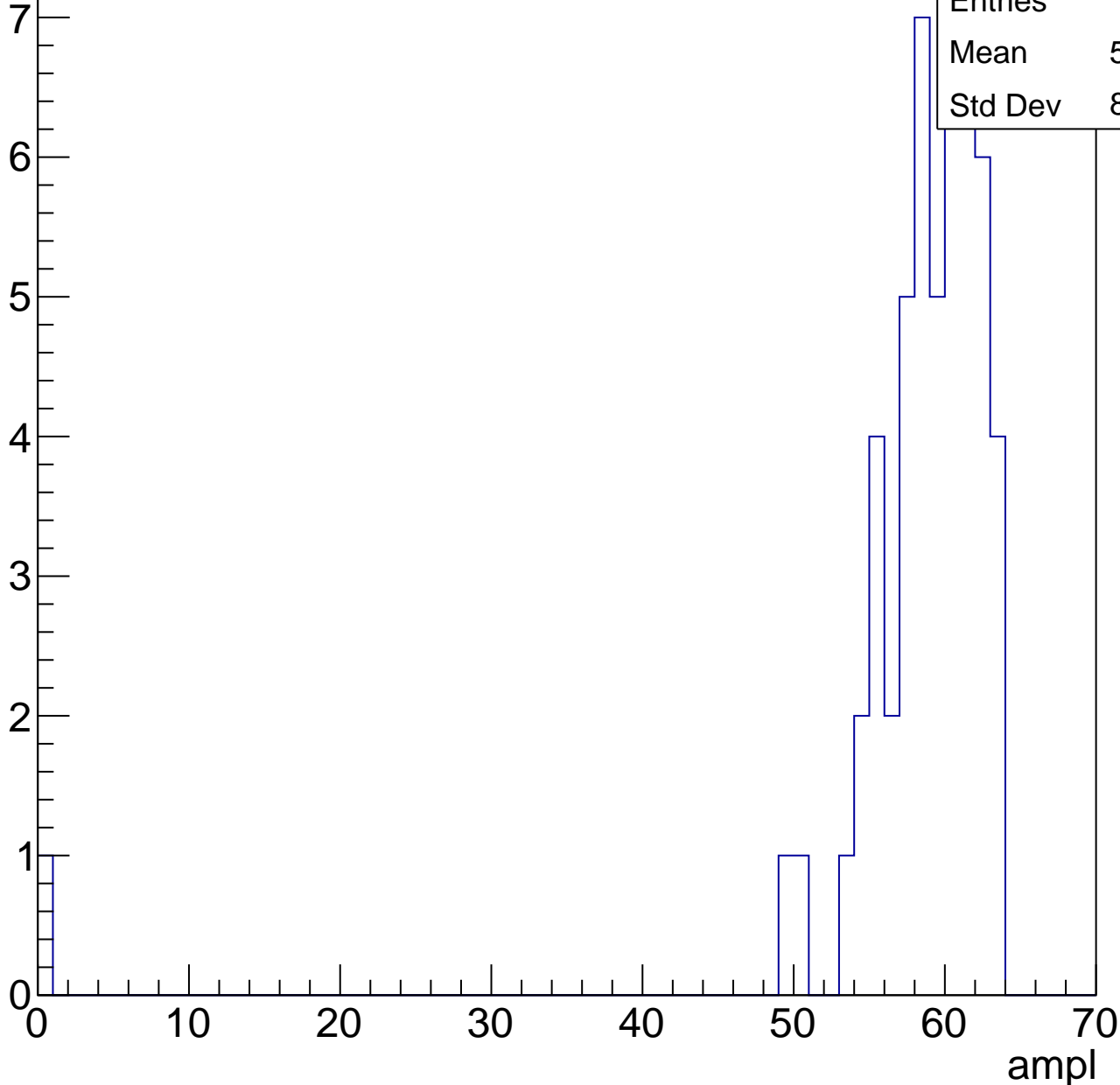


# B1L003S, U3-ch74, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	57.53
Std Dev	8.573

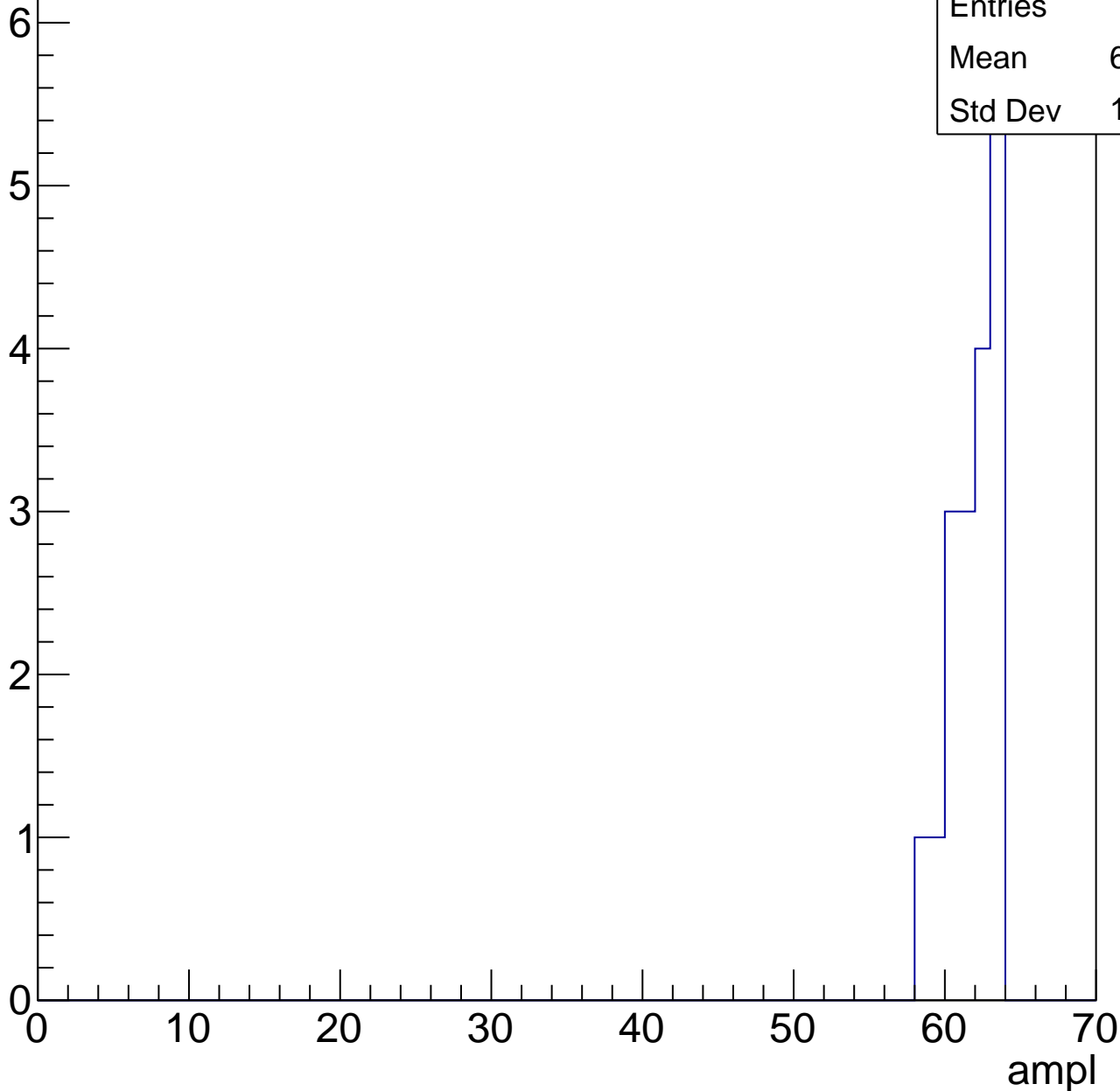


# B1L003S, U3-ch74, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	18
Mean	61.44
Std Dev	1.499





# B1L003S, U3-ch74, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U3-ch75, adc0

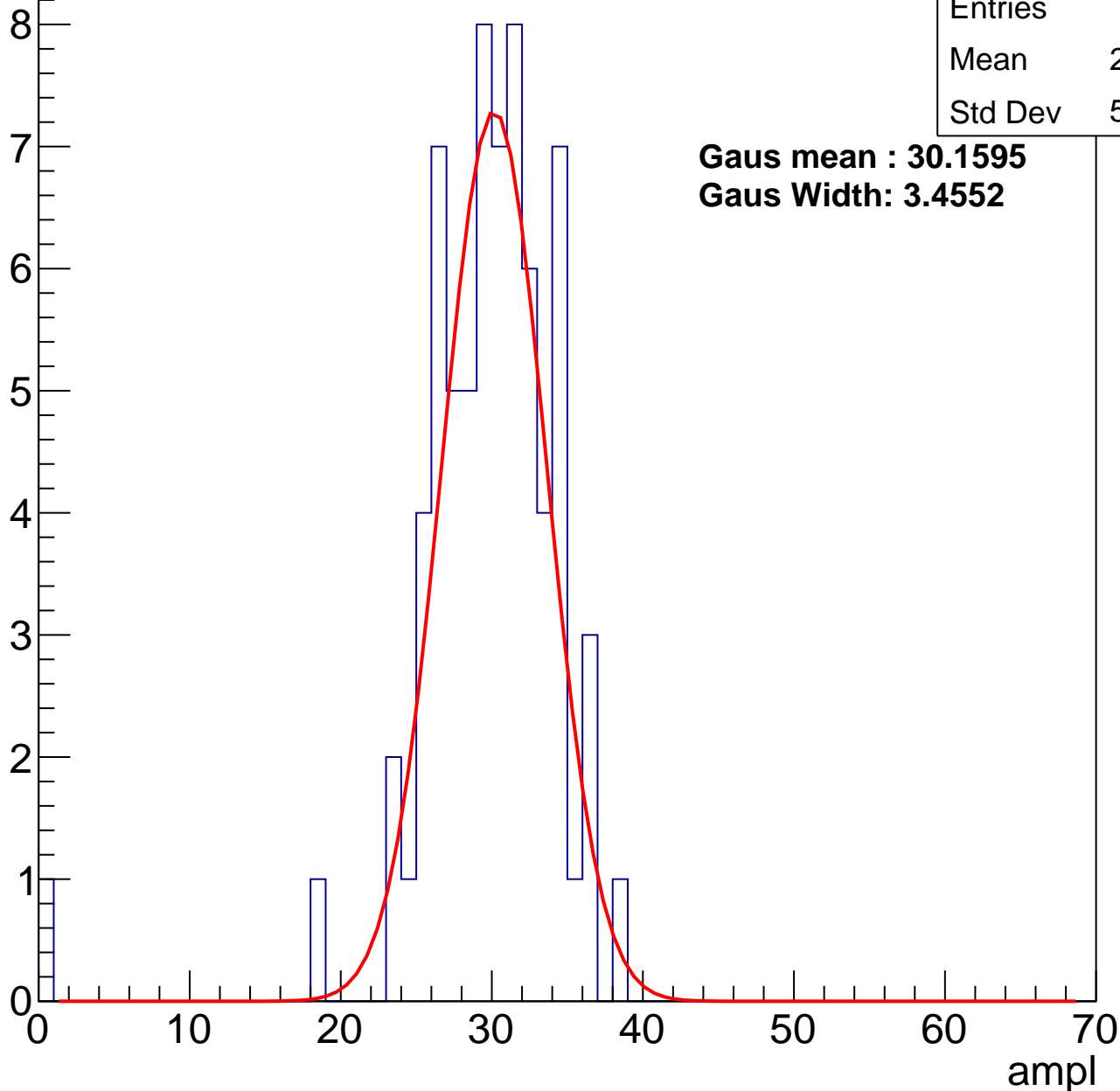
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	71
Mean	29.27
Std Dev	5.038

**Gaus mean : 30.1595**

**Gaus Width: 3.4552**



# B1L003S, U3-ch75, adc1

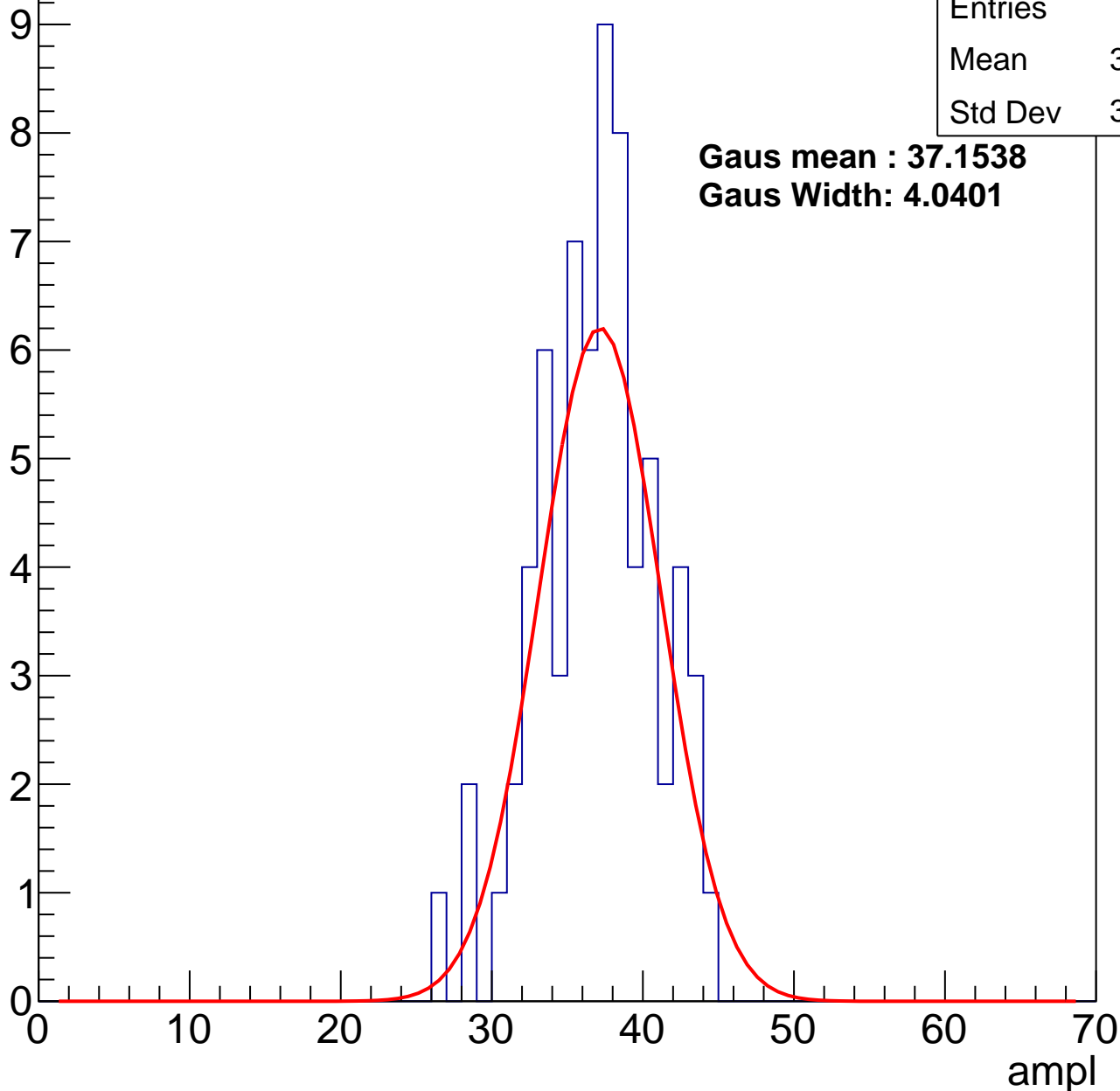
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	36.46
Std Dev	3.833

**Gaus mean : 37.1538**

**Gaus Width: 4.0401**



# B1L003S, U3-ch75, adc2

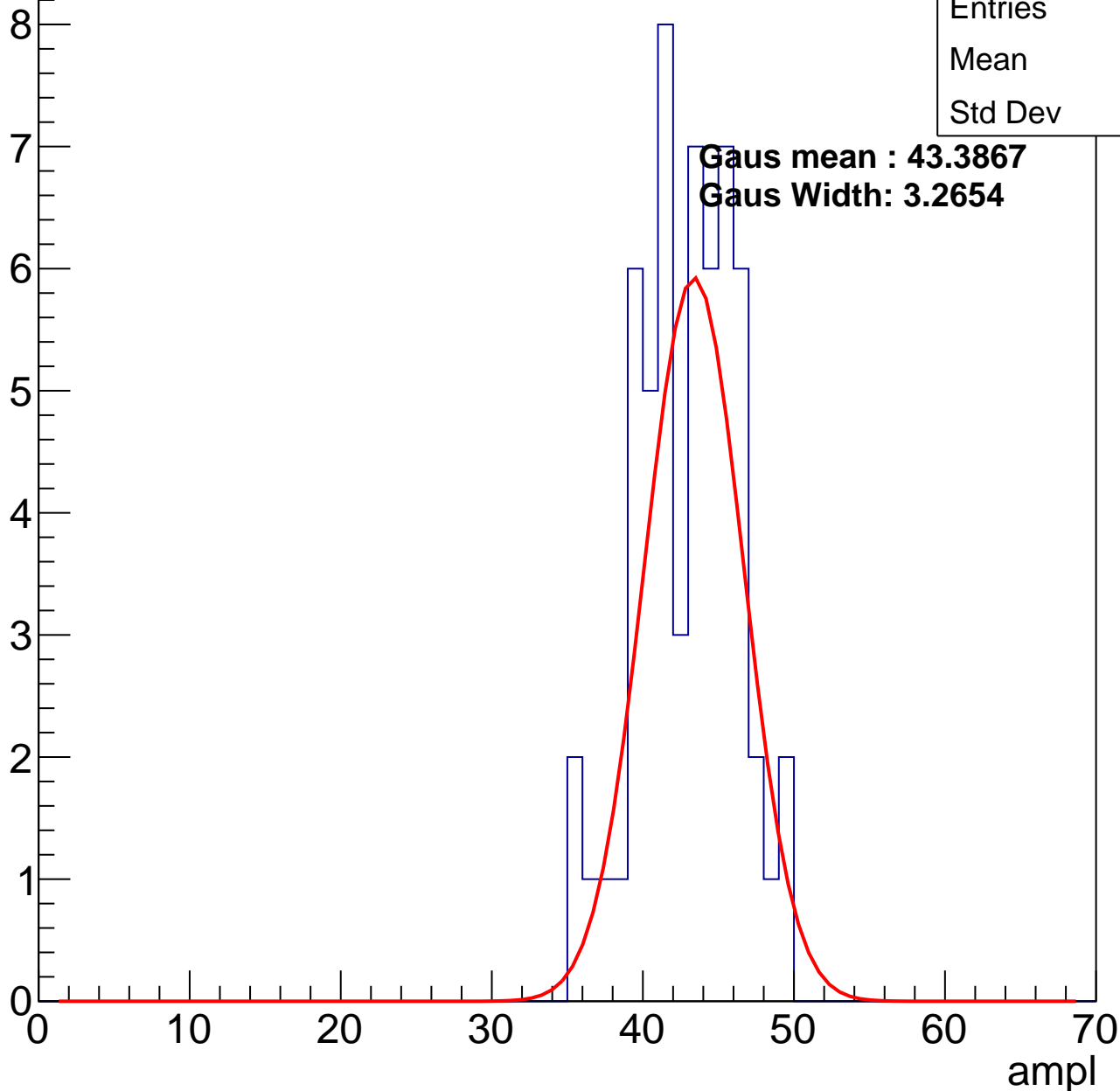
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	42.5
Std Dev	3.26

**Gaus mean : 43.3867**

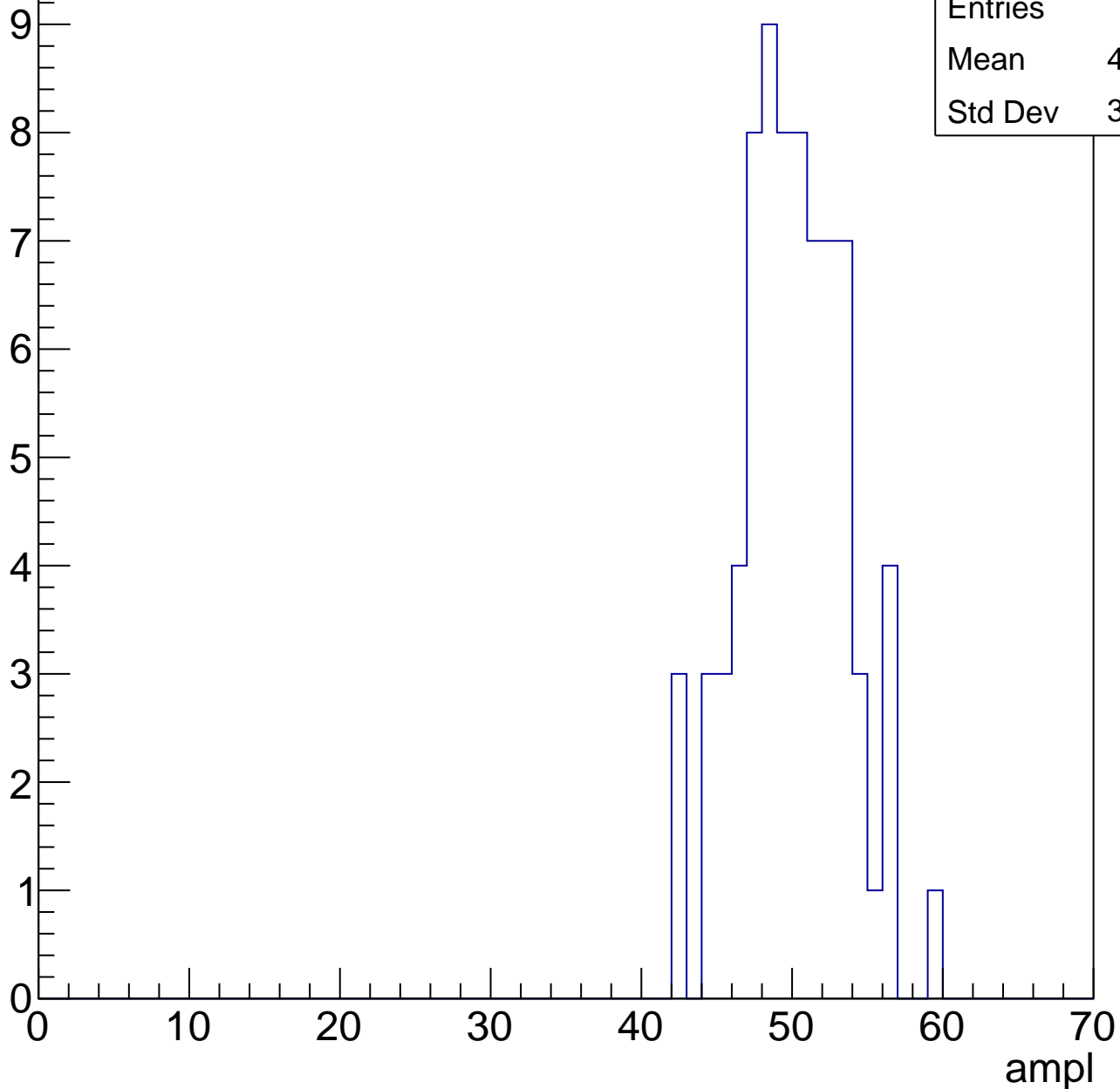
**Gaus Width: 3.2654**



# B1L003S, U3-ch75, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



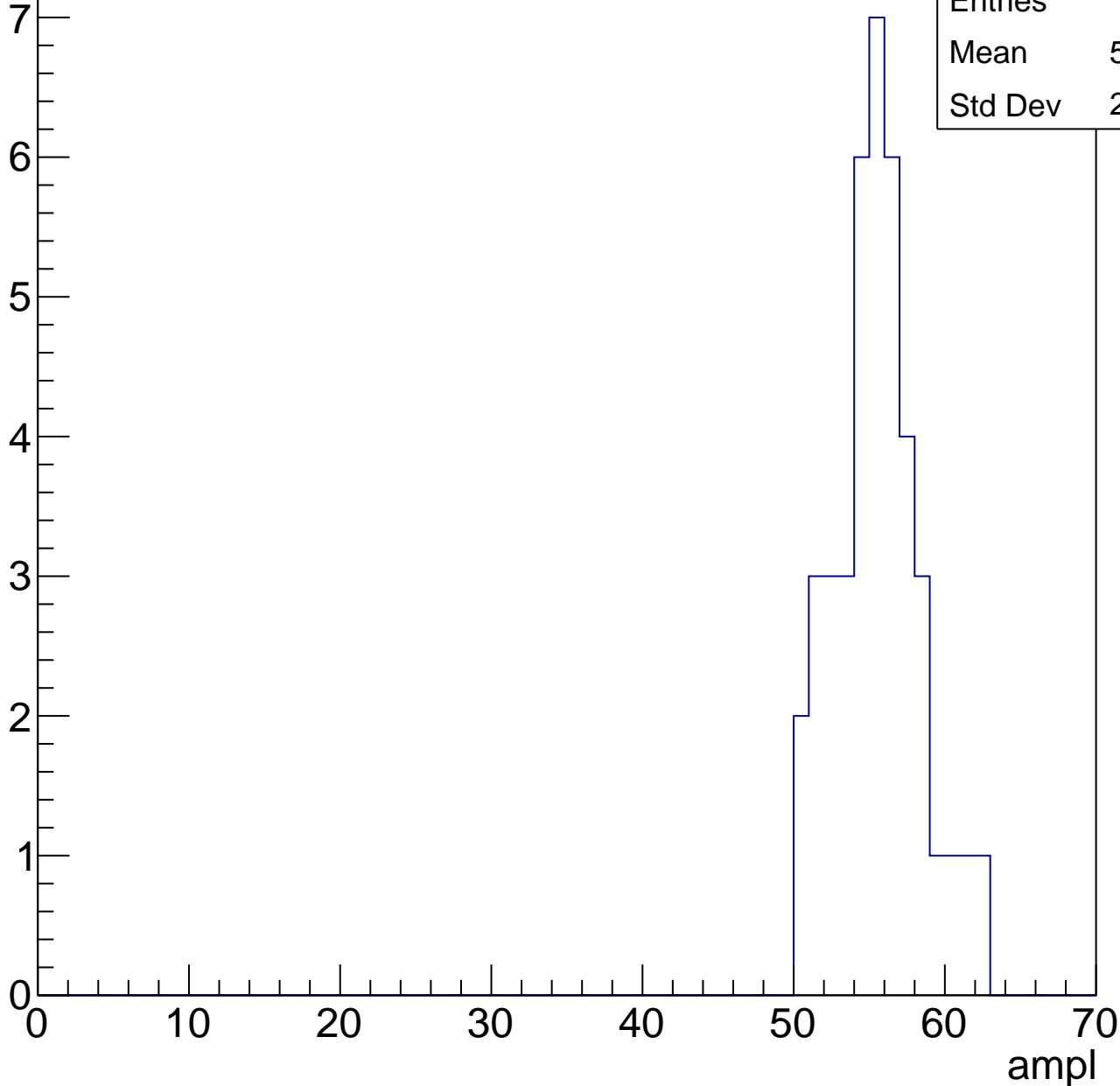
Entries	76
Mean	49.59
Std Dev	3.514

# B1L003S, U3-ch75, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	41
Mean	55.05
Std Dev	2.785

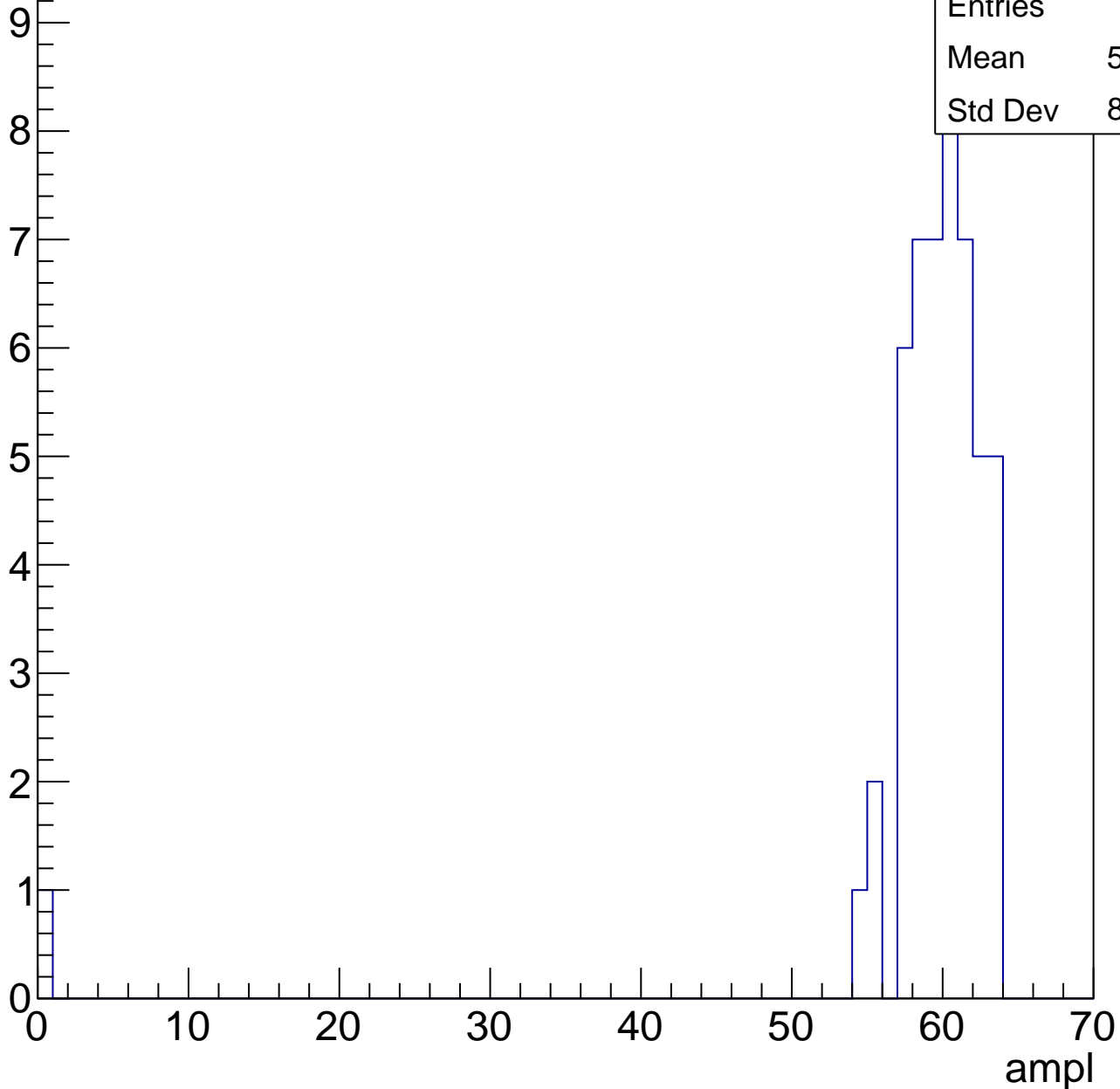


# B1L003S, U3-ch75, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	50
Mean	58.34
Std Dev	8.613

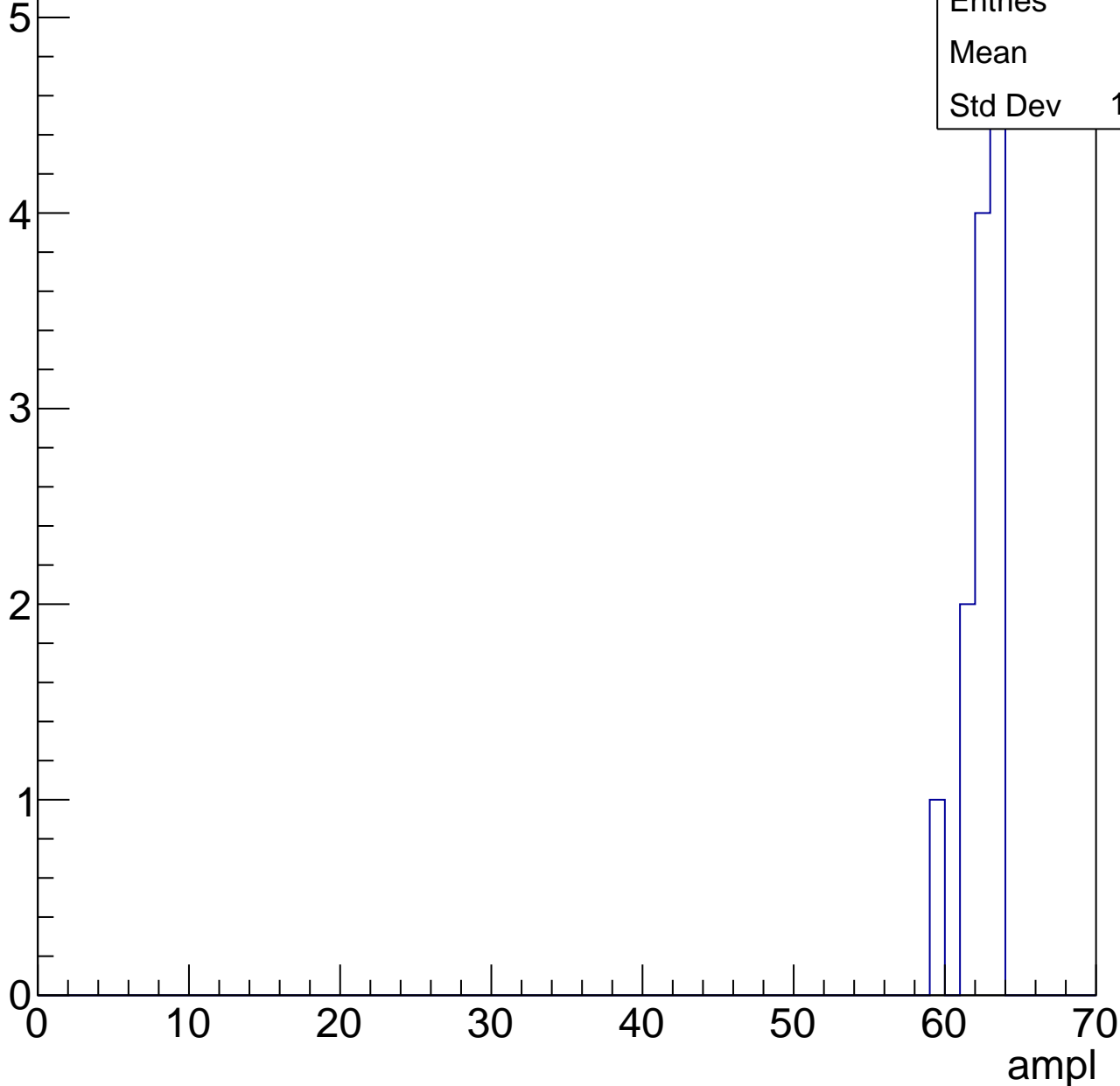


# B1L003S, U3-ch75, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	12
Mean	62
Std Dev	1.155





# B1L003S, U3-ch75, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U3-ch76, adc0

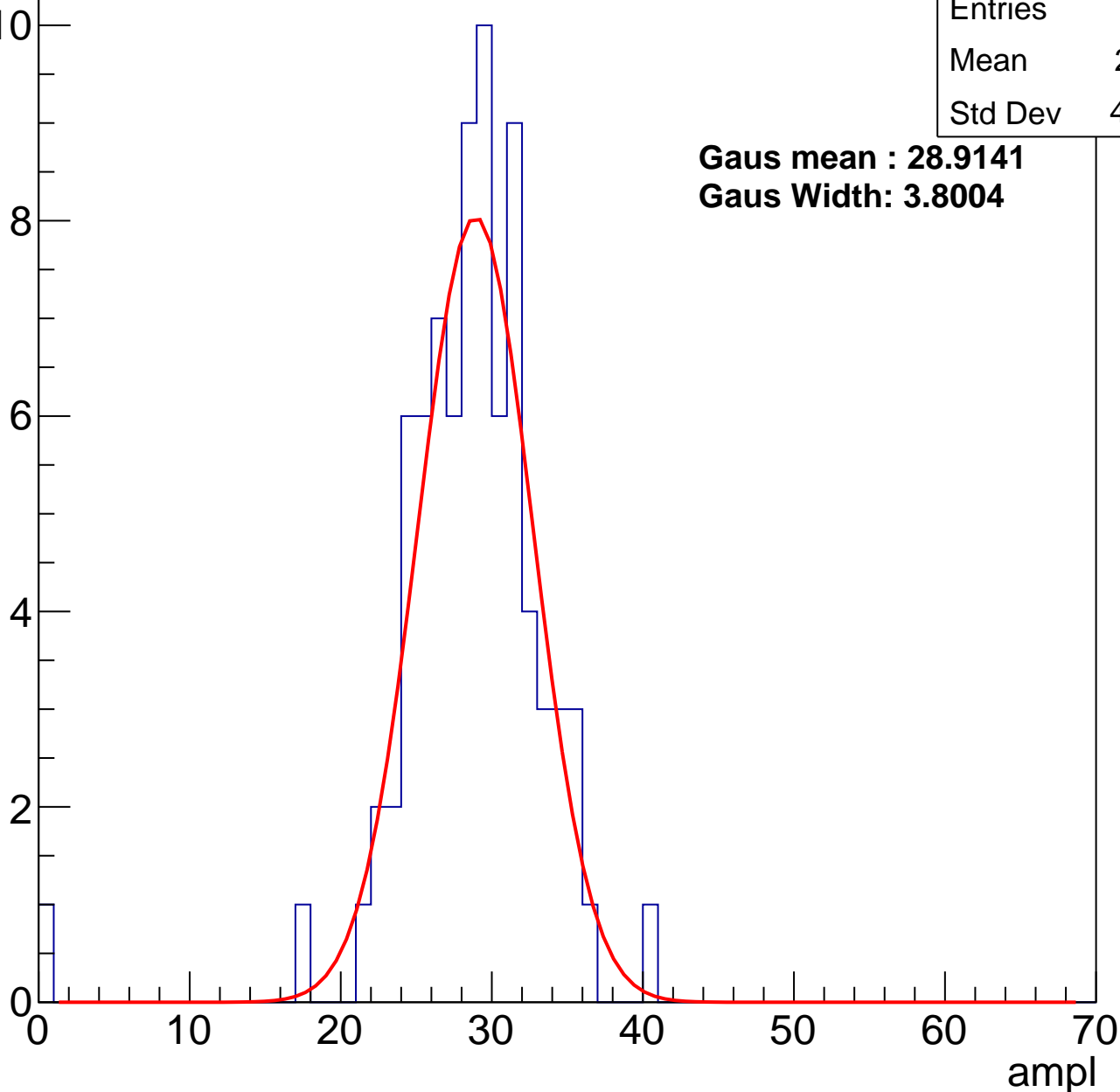
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	81
Mean	28.11
Std Dev	4.939

**Gaus mean : 28.9141**

**Gaus Width: 3.8004**



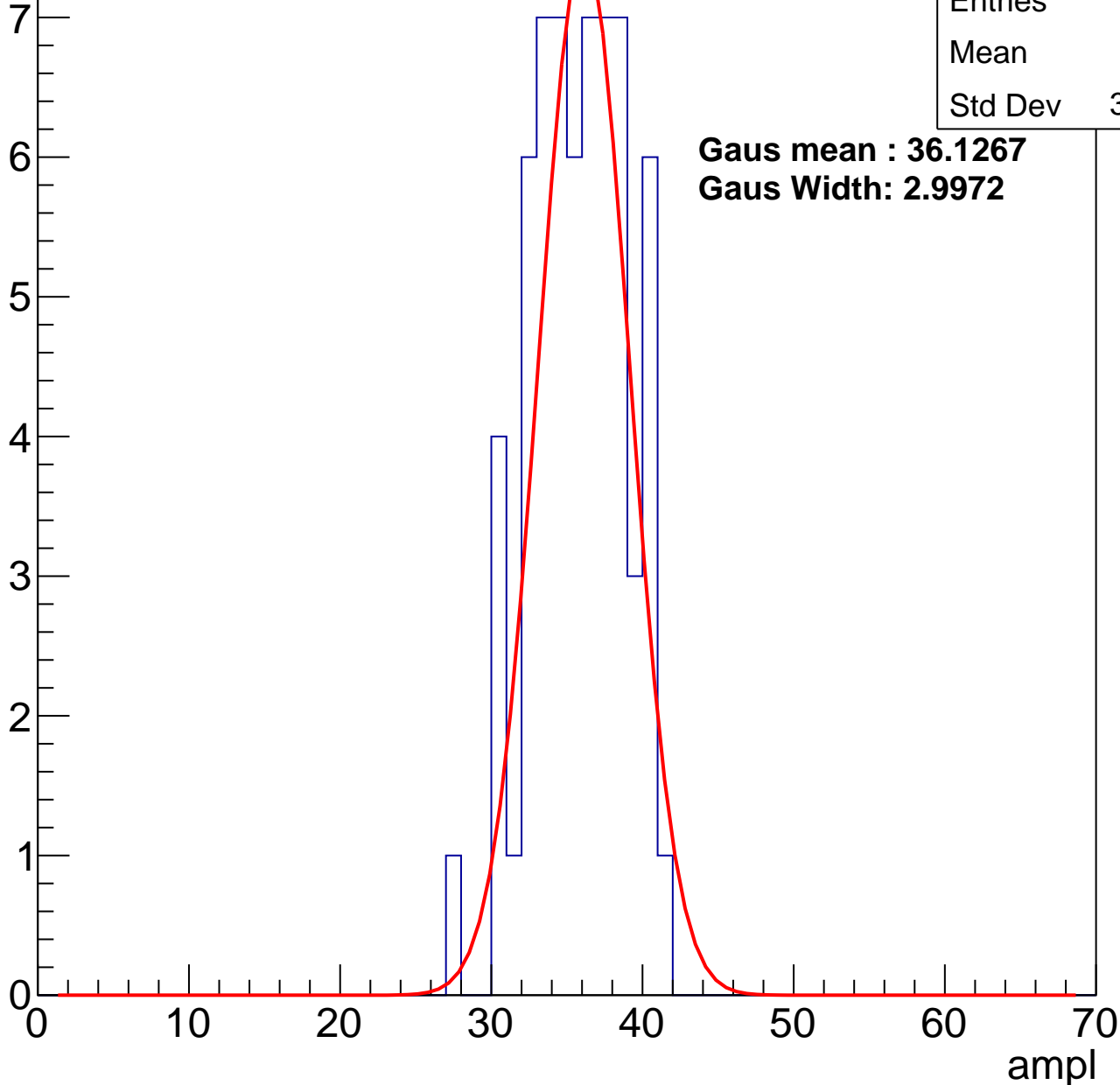
# B1L003S, U3-ch76, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	35.3
Std Dev	3.074

**Gaus mean : 36.1267**  
**Gaus Width: 2.9972**



# B1L003S, U3-ch76, adc2

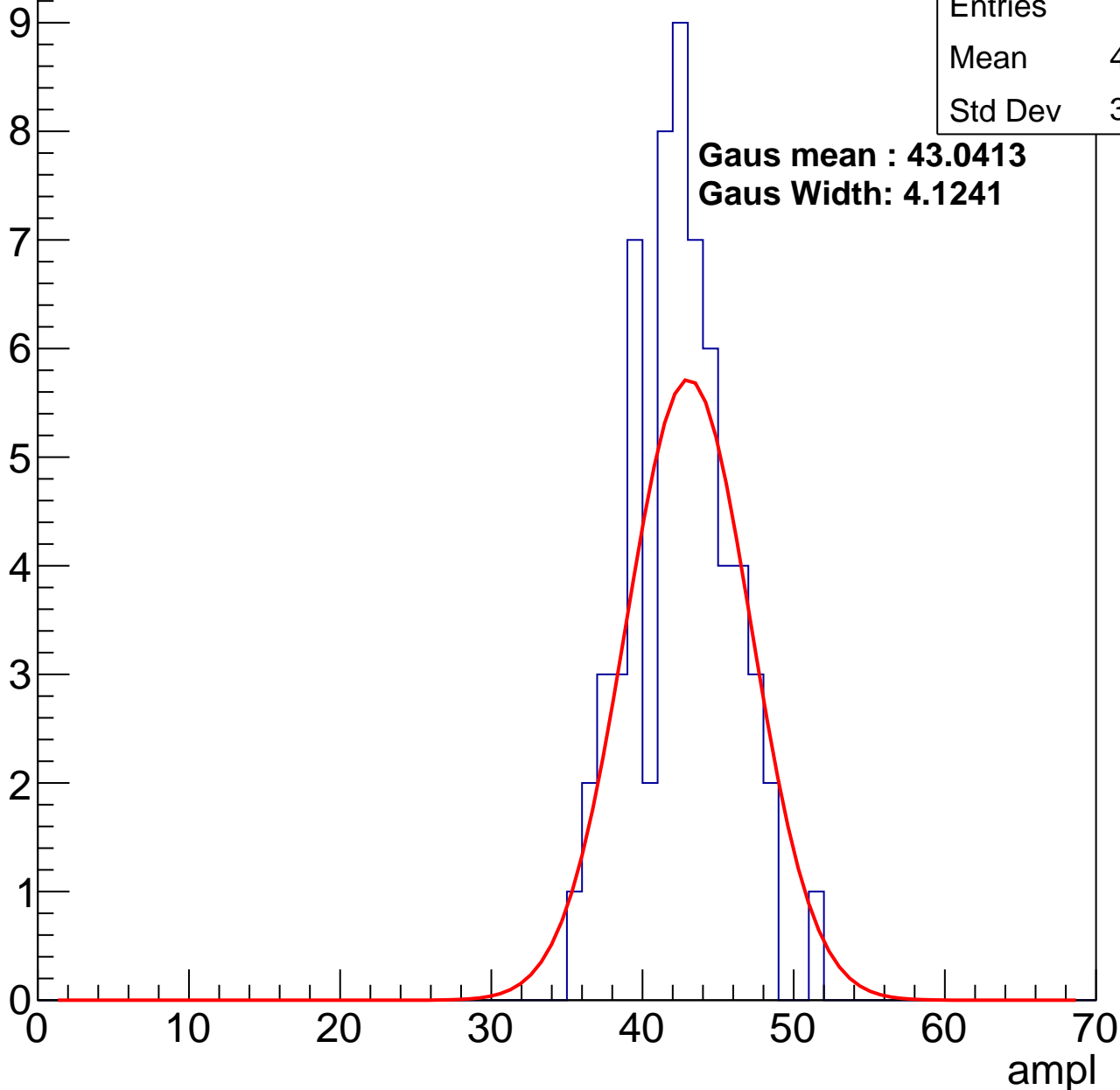
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	42.06
Std Dev	3.316

**Gaus mean : 43.0413**

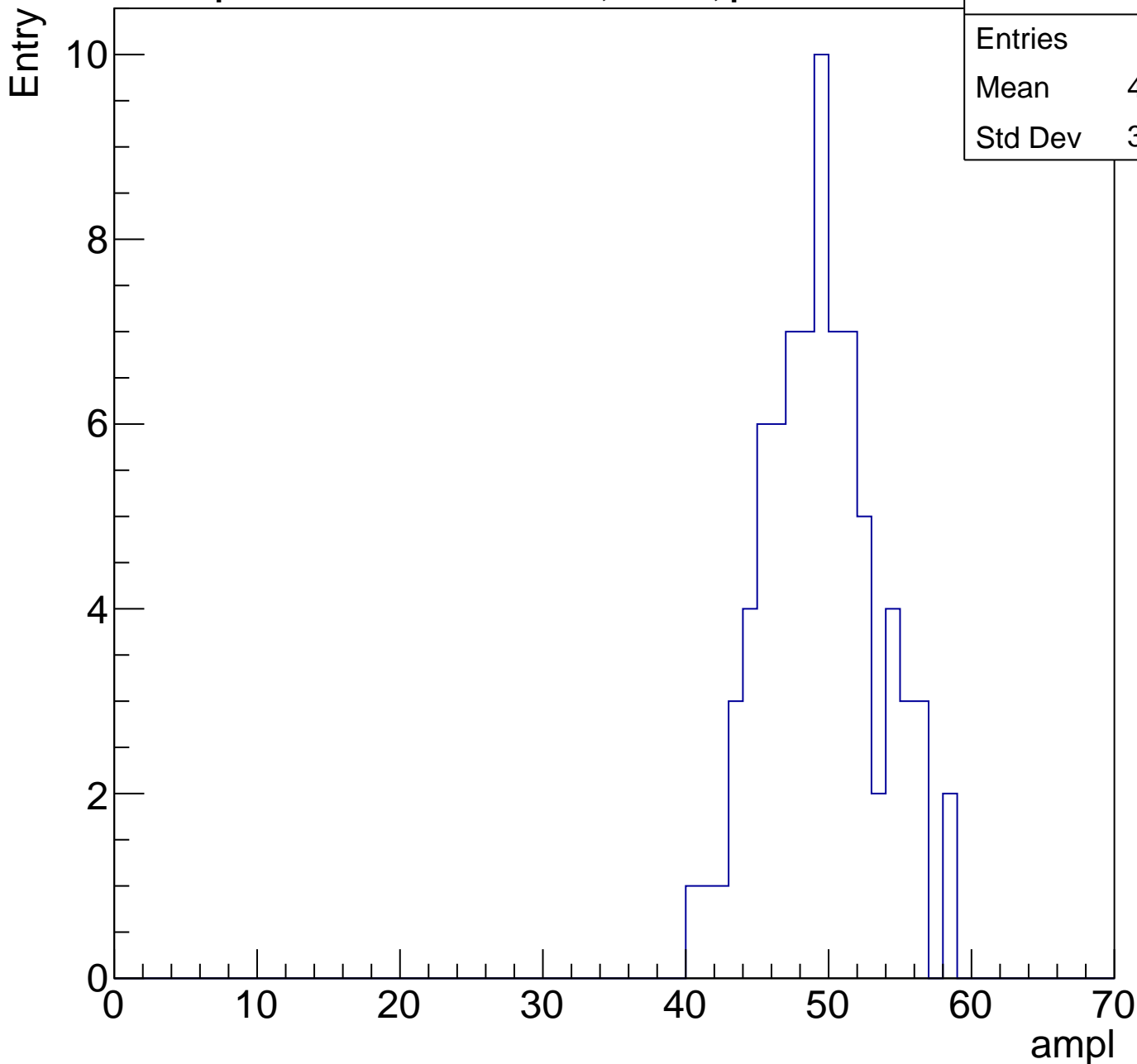
**Gaus Width: 4.1241**



# B1L003S, U3-ch76, adc3

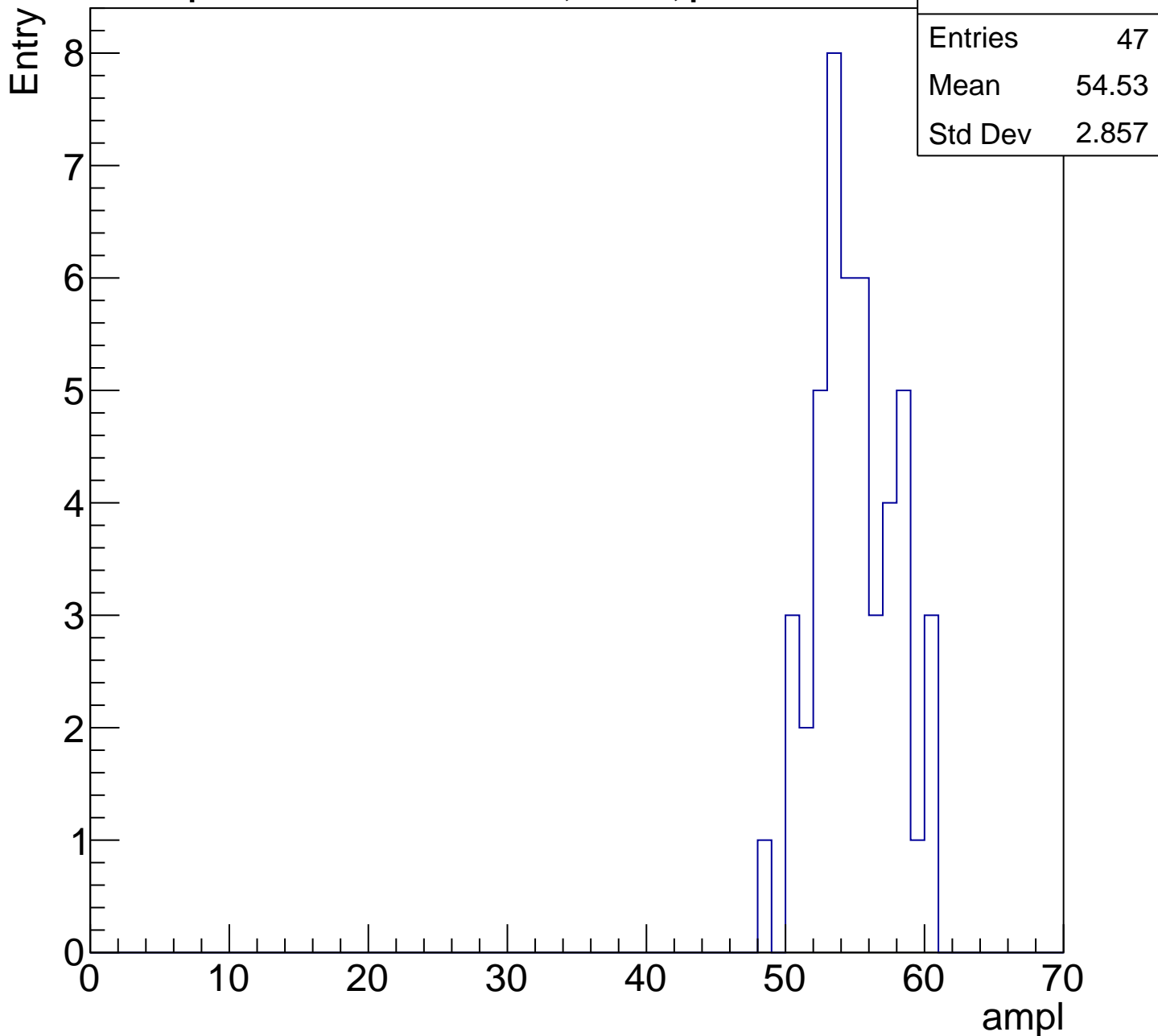
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	79
Mean	48.95
Std Dev	3.923



# B1L003S, U3-ch76, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2



# B1L003S, U3-ch76, adc5

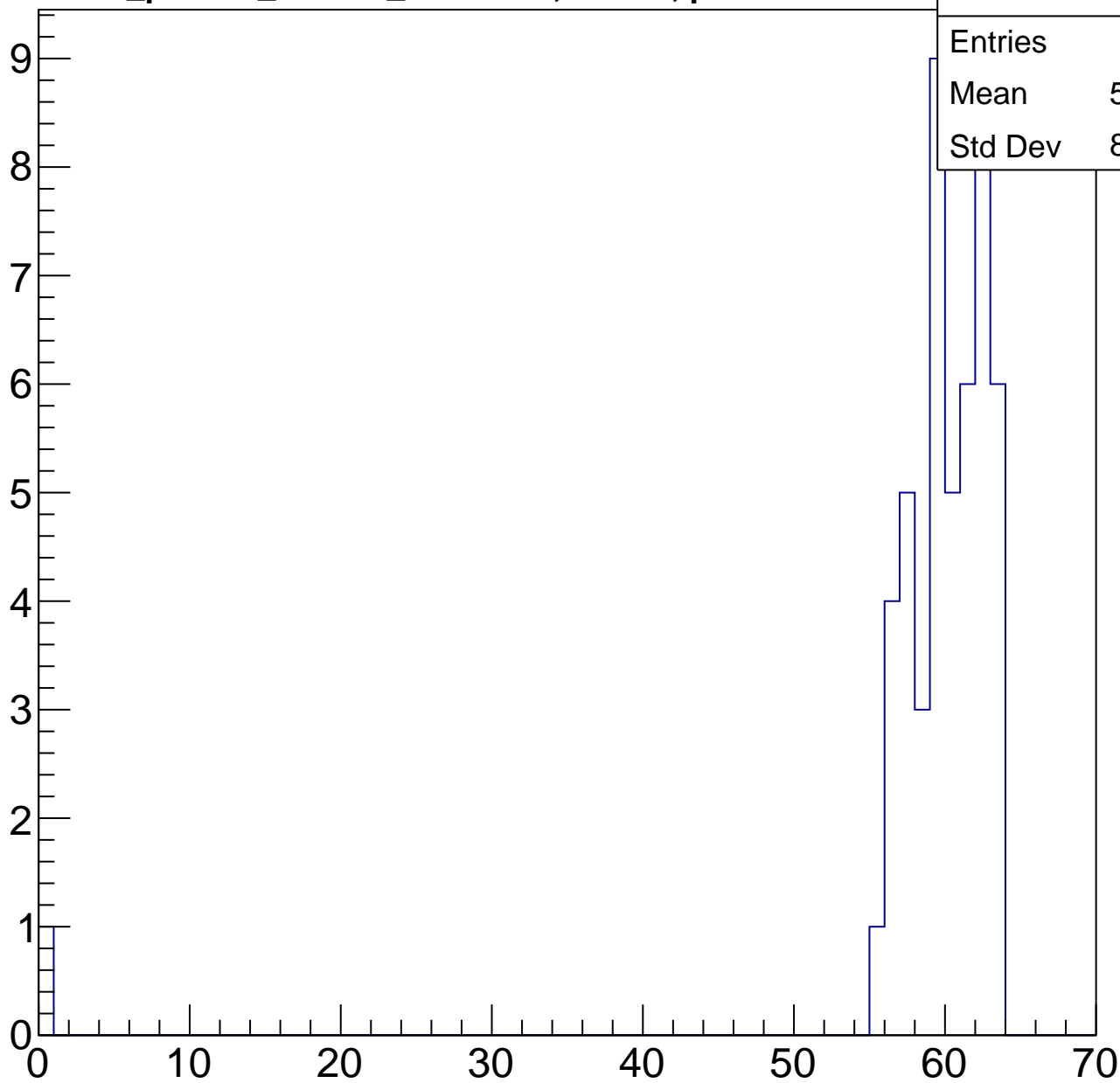
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	48
Mean	58.52
Std Dev	8.829

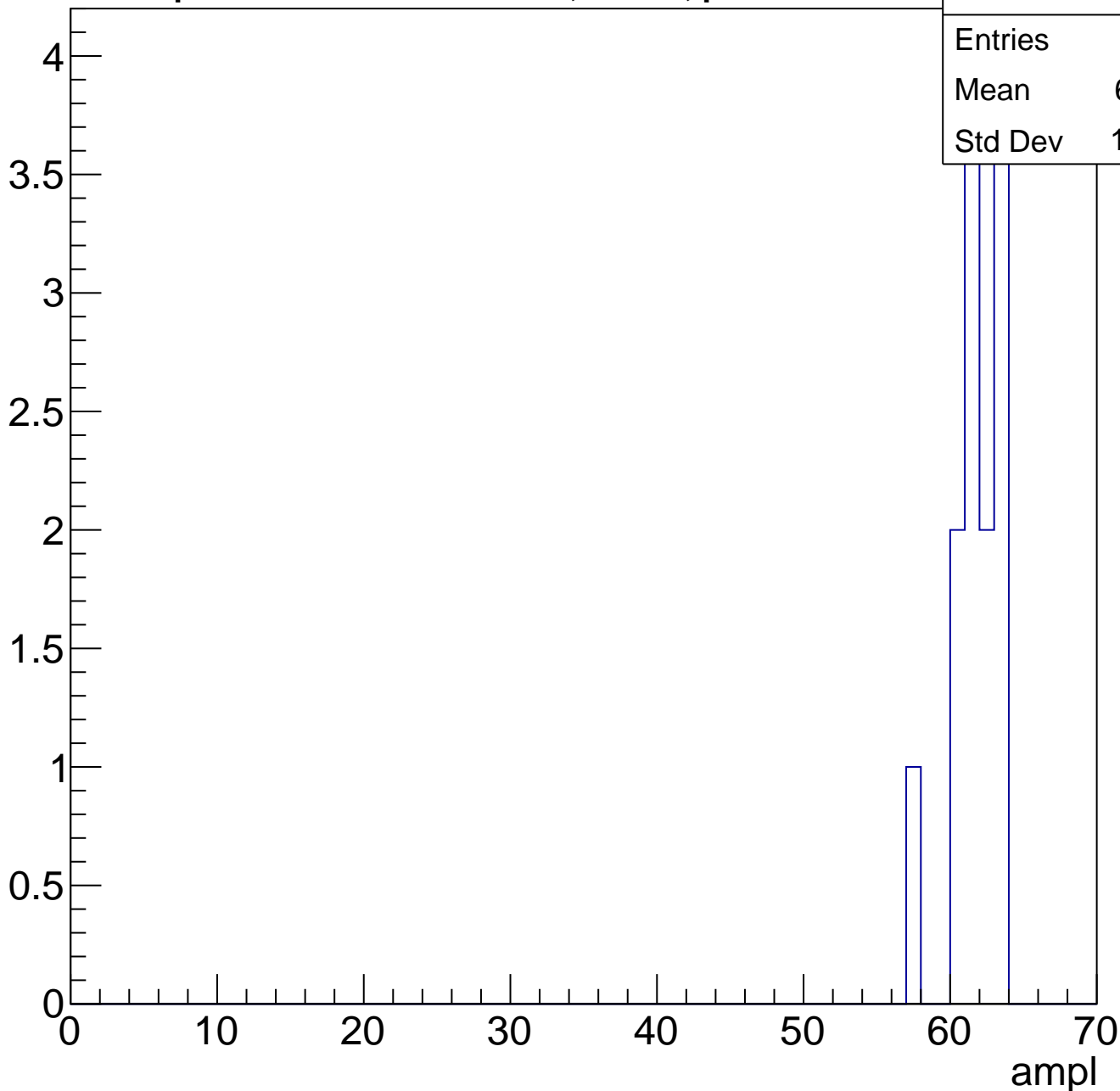
ampl



# B1L003S, U3-ch76, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	13
Mean	61.31
Std Dev	1.635



# B1L003S, U3-ch76, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U3-ch77, adc0

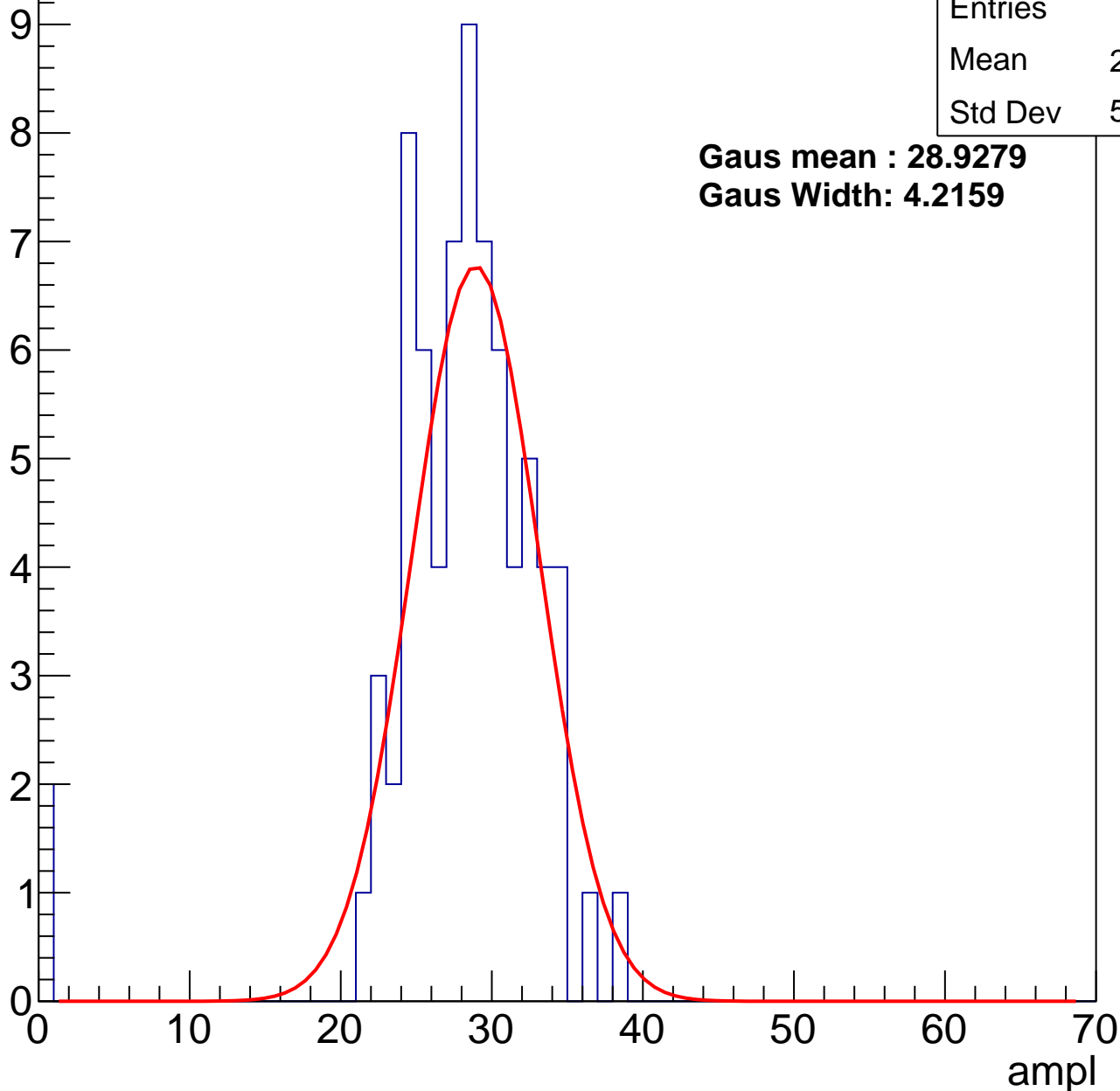
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	74
Mean	27.42
Std Dev	5.824

**Gaus mean : 28.9279**

**Gaus Width: 4.2159**



# B1L003S, U3-ch77, adc1

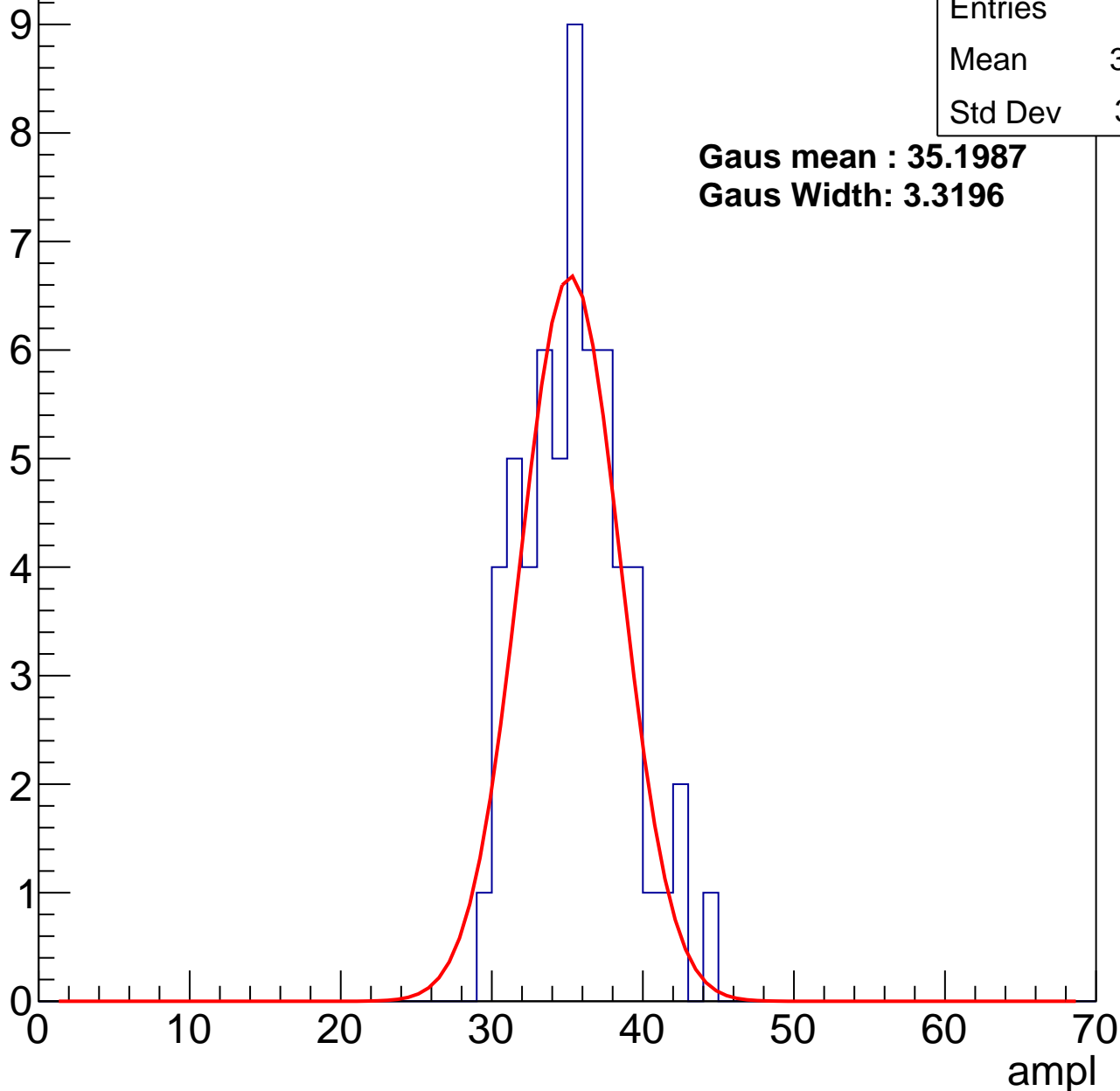
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	35.08
Std Dev	3.321

**Gaus mean : 35.1987**

**Gaus Width: 3.3196**



# B1L003S, U3-ch77, adc2

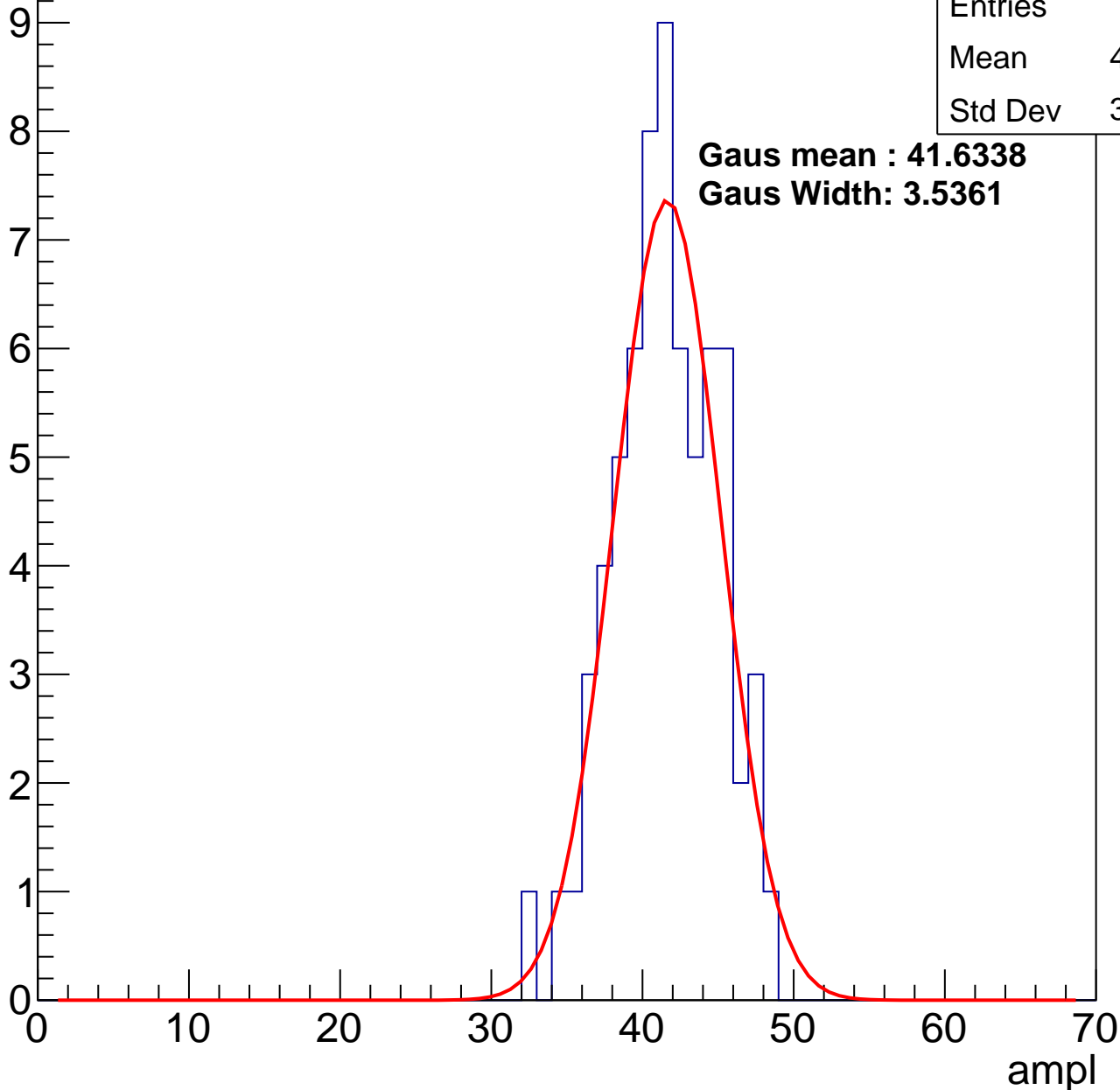
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	41.07
Std Dev	3.378

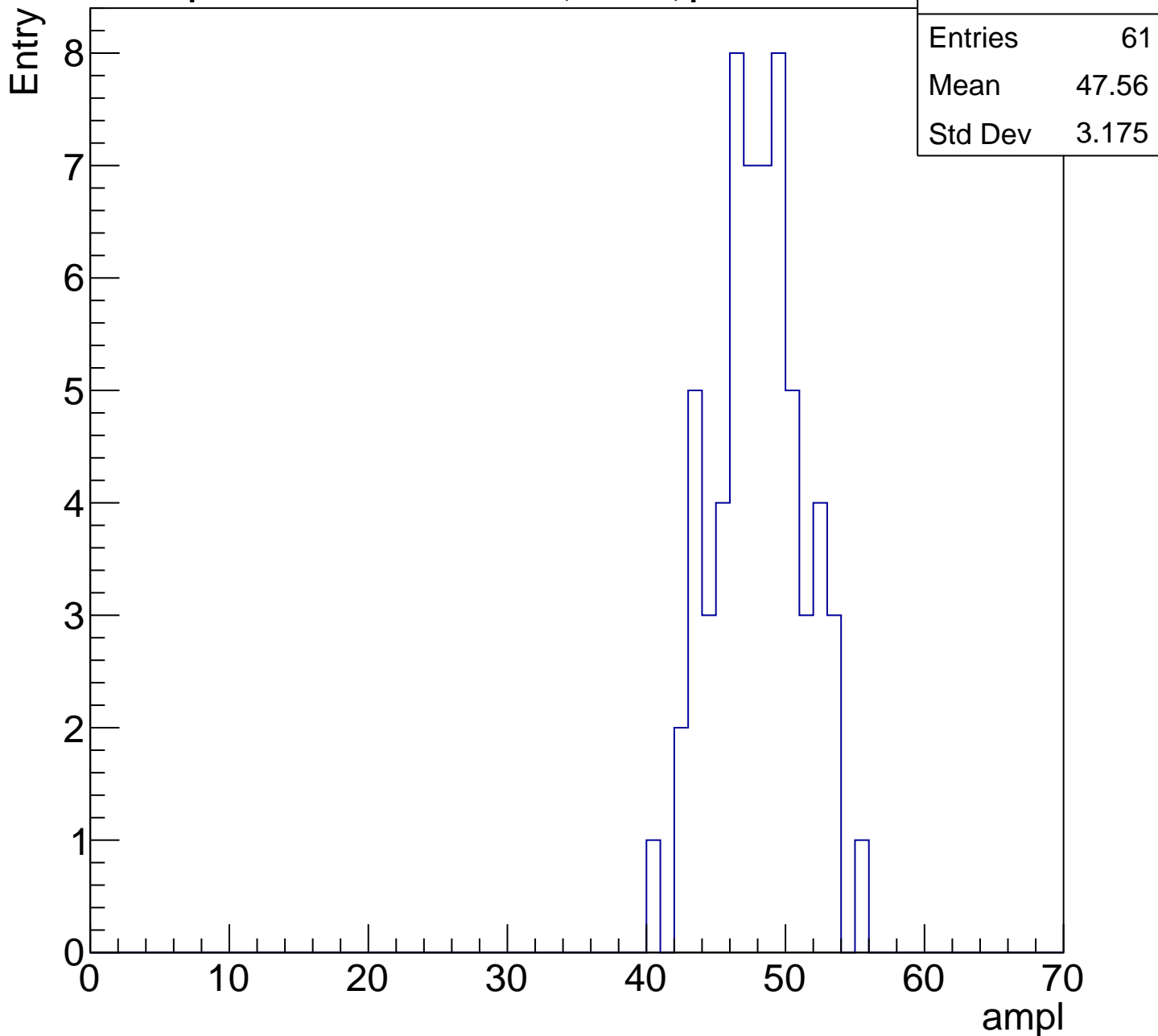
**Gaus mean : 41.6338**

**Gaus Width: 3.5361**



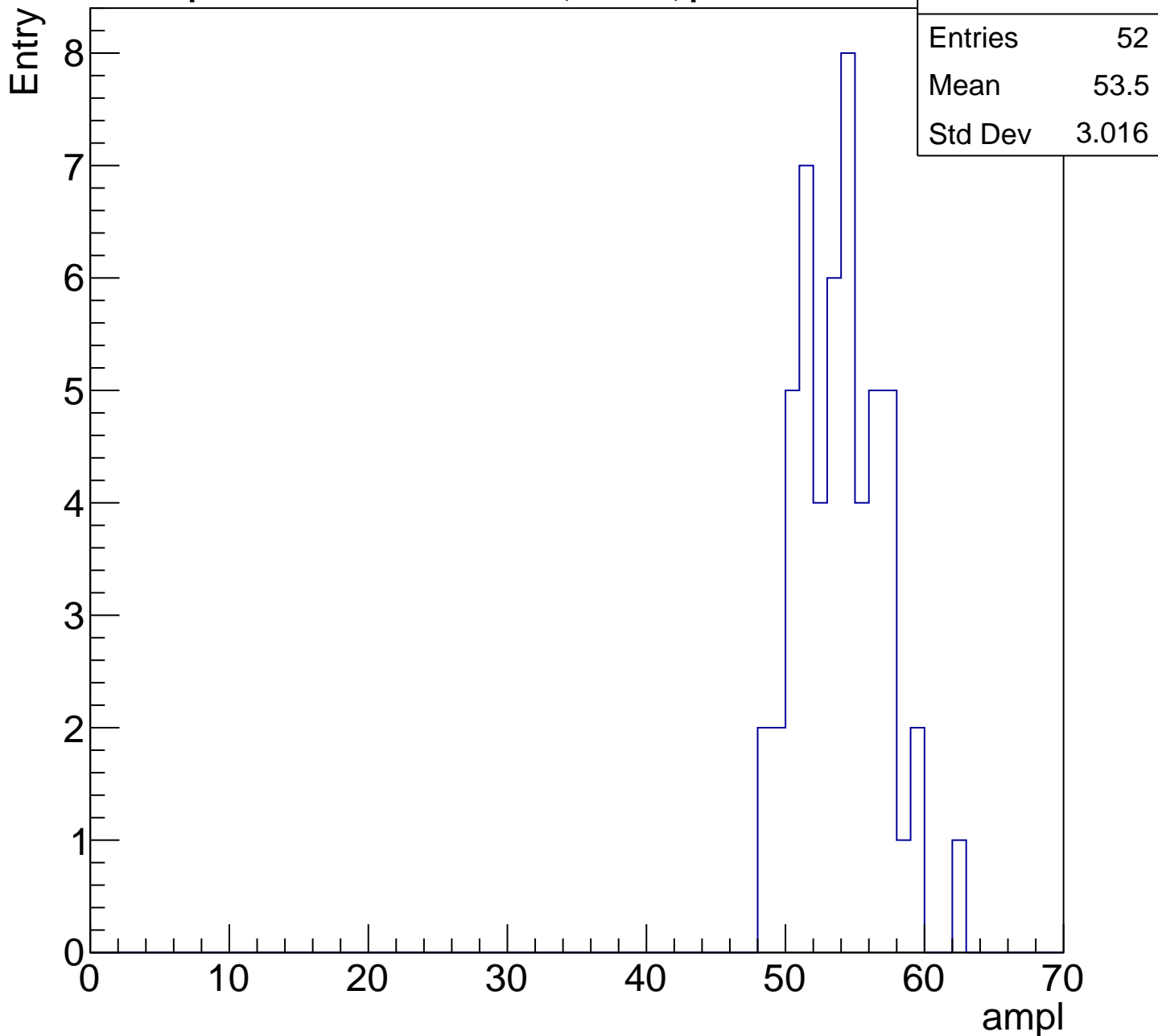
# B1L003S, U3-ch77, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2



# B1L003S, U3-ch77, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

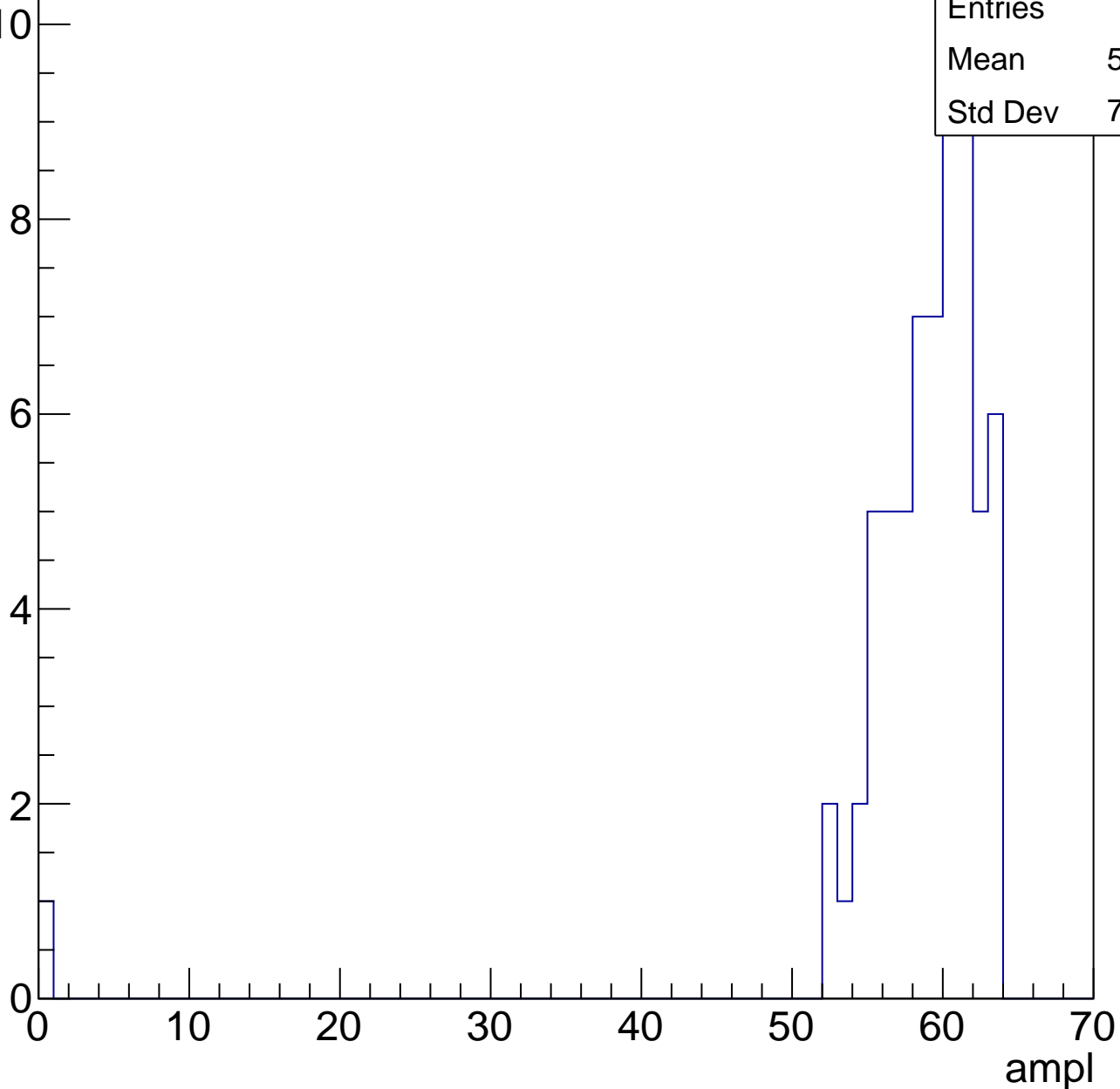


# B1L003S, U3-ch77, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

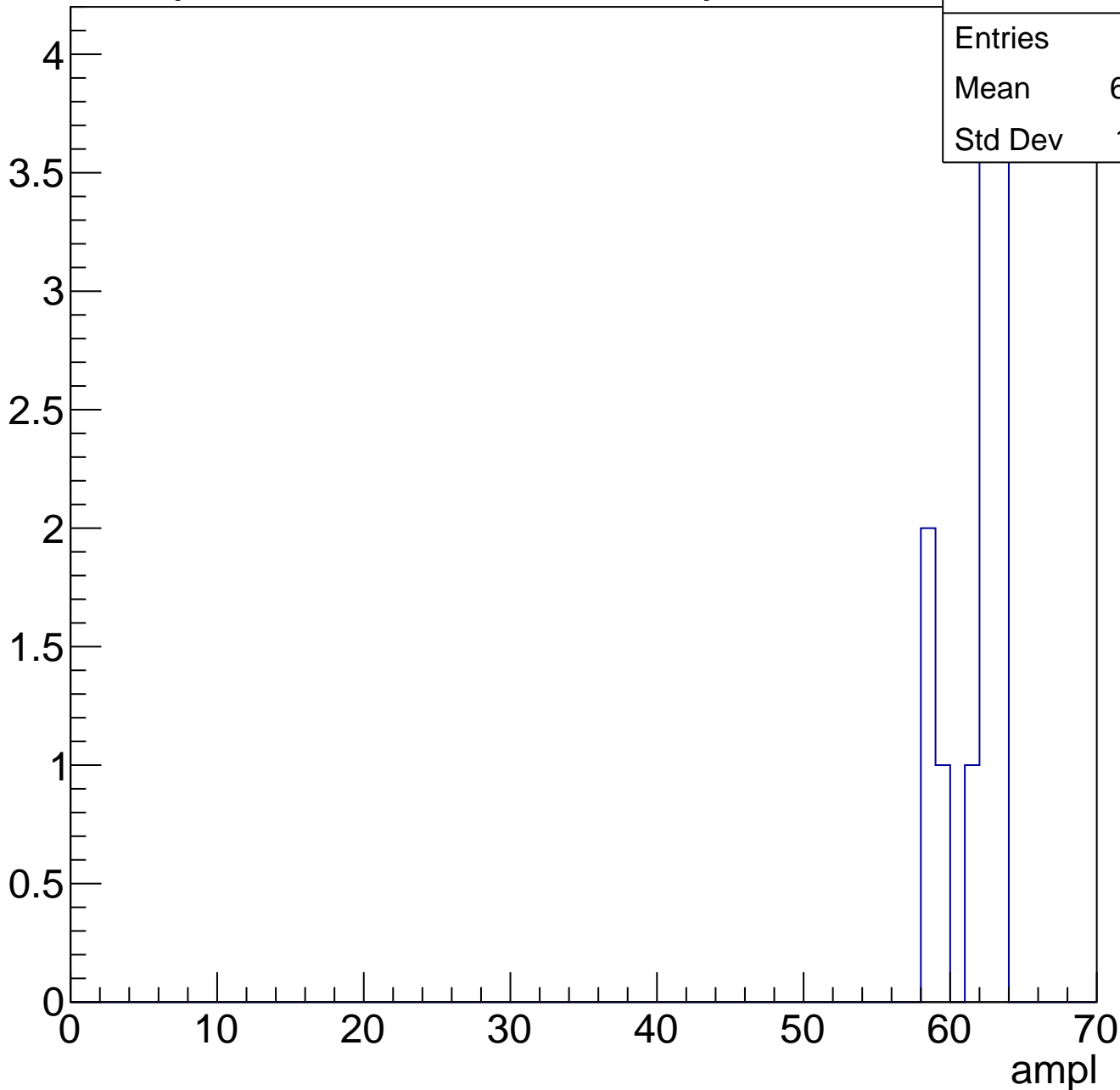
Entries	65
Mean	57.86
Std Dev	7.766



# B1L003S, U3-ch77, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch77, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U3-ch78, adc0

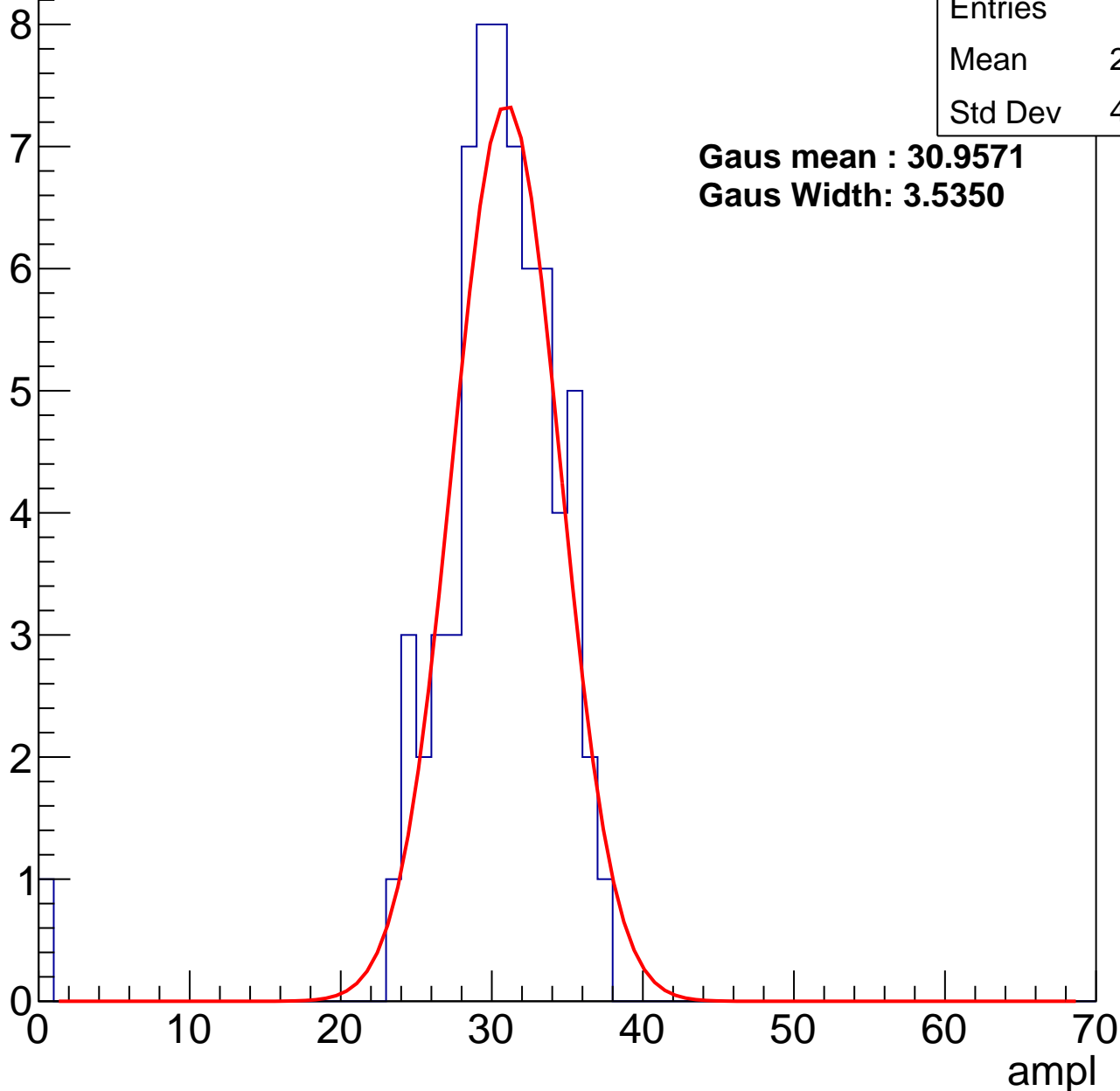
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	29.84
Std Dev	4.904

**Gaus mean : 30.9571**

**Gaus Width: 3.5350**



# B1L003S, U3-ch78, adc1

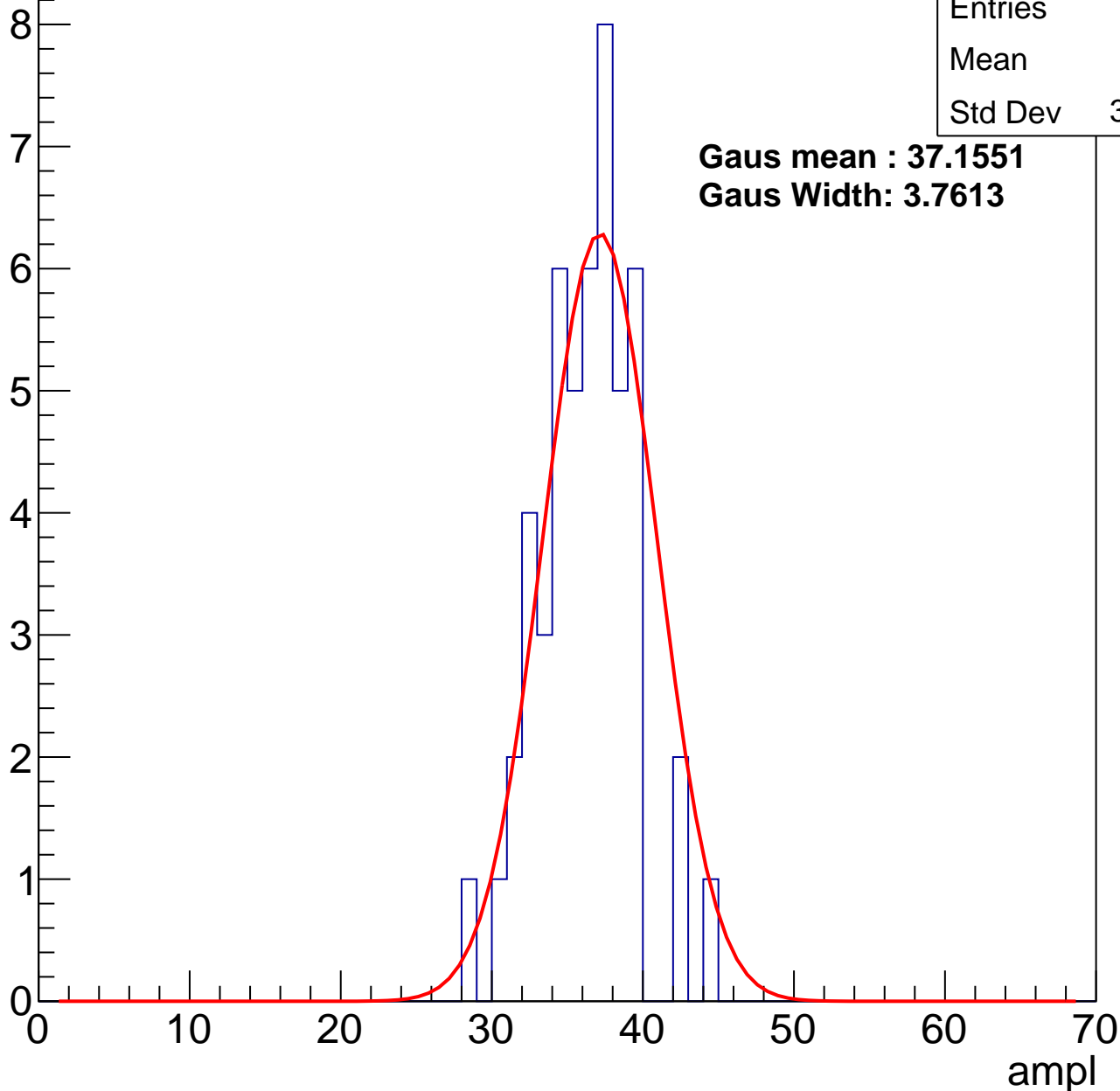
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	50
Mean	35.8
Std Dev	3.118

**Gaus mean : 37.1551**

**Gaus Width: 3.7613**



# B1L003S, U3-ch78, adc2

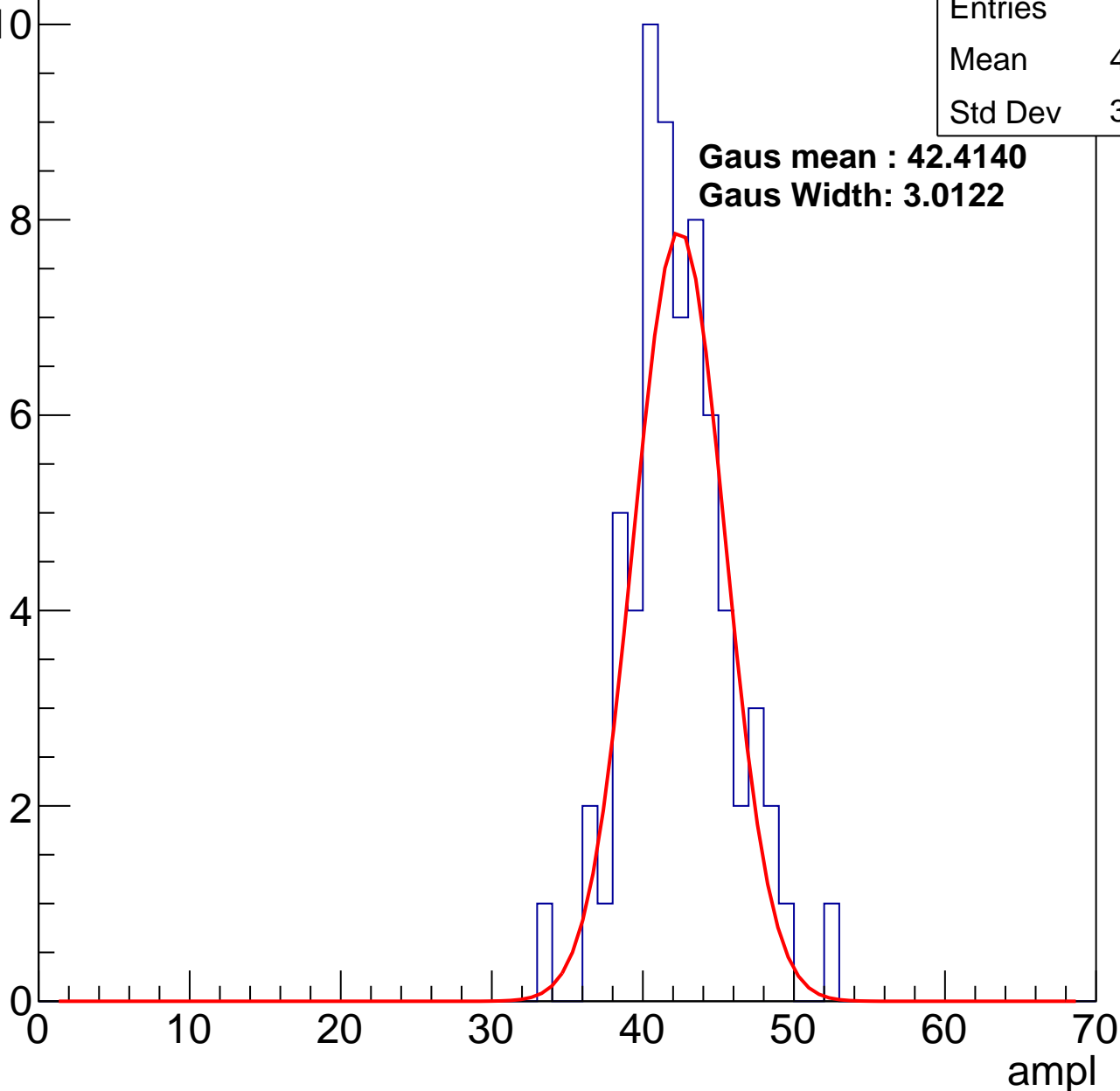
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	41.95
Std Dev	3.346

**Gaus mean : 42.4140**

**Gaus Width: 3.0122**

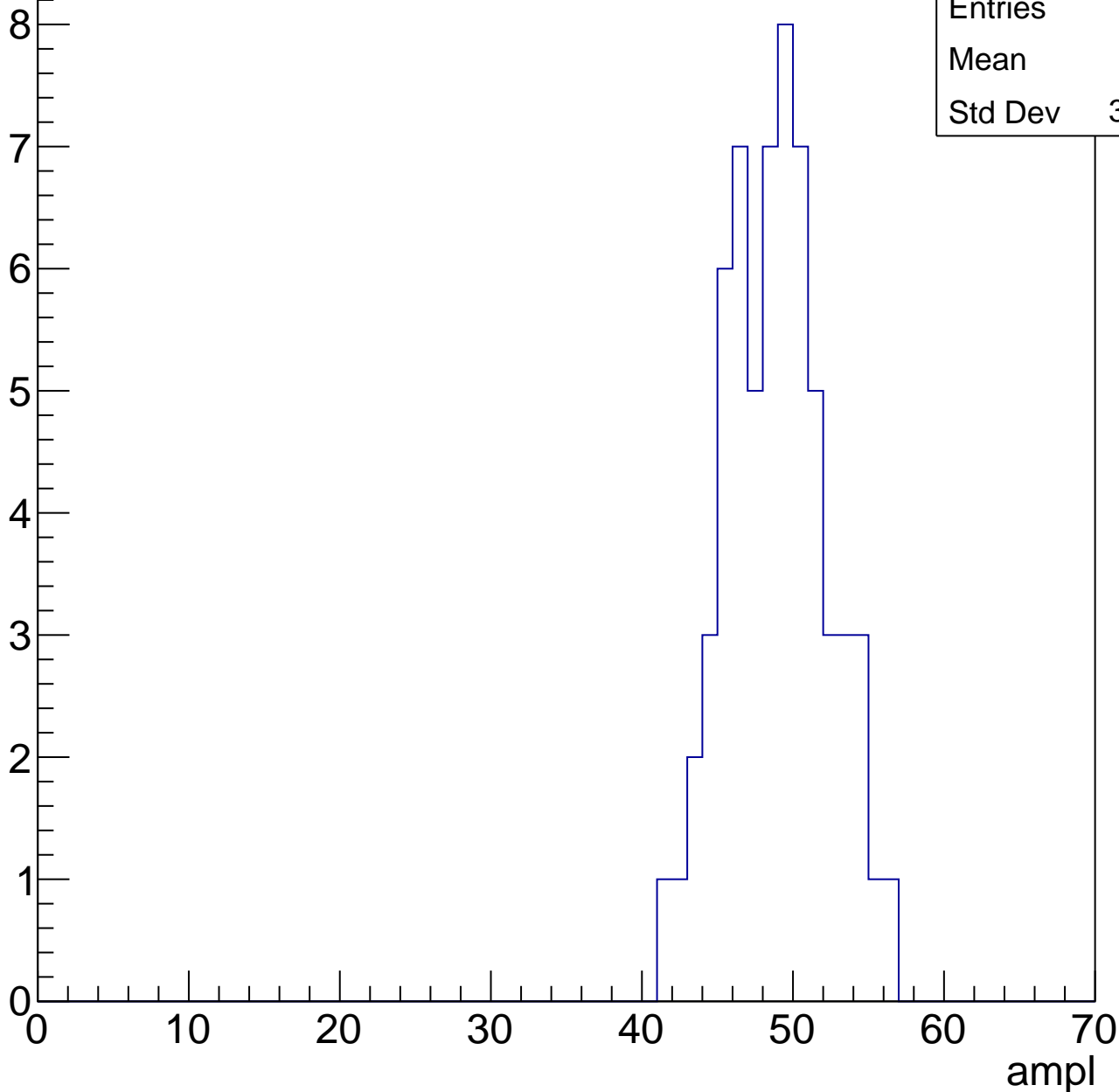


# B1L003S, U3-ch78, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

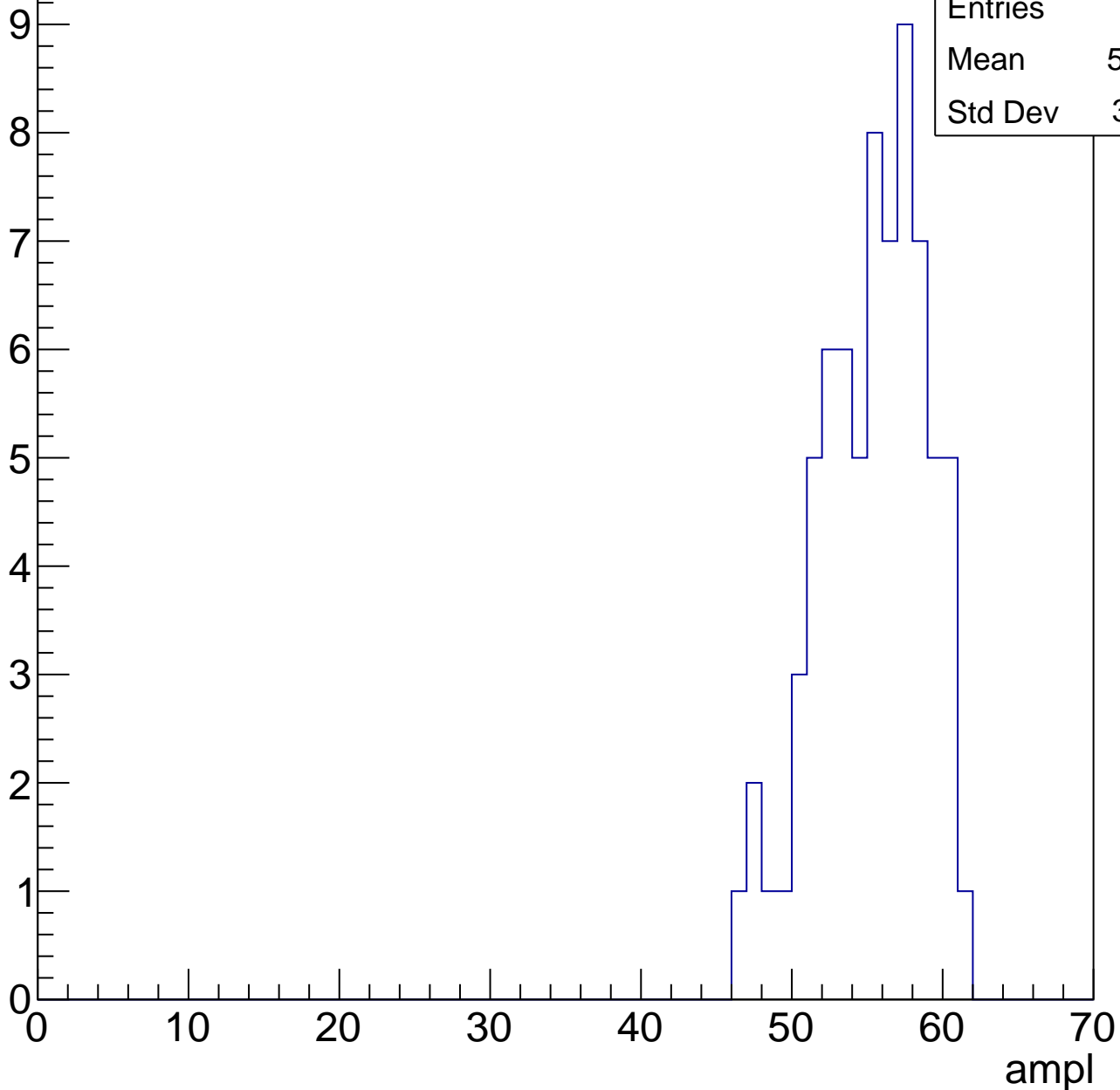
Entries	63
Mean	48.4
Std Dev	3.298



# B1L003S, U3-ch78, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U3-ch78, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

5

4

3

2

1

0

Entries 30

Mean 59.53

Std Dev 2.884

ampl

0

10

20

30

40

50

60

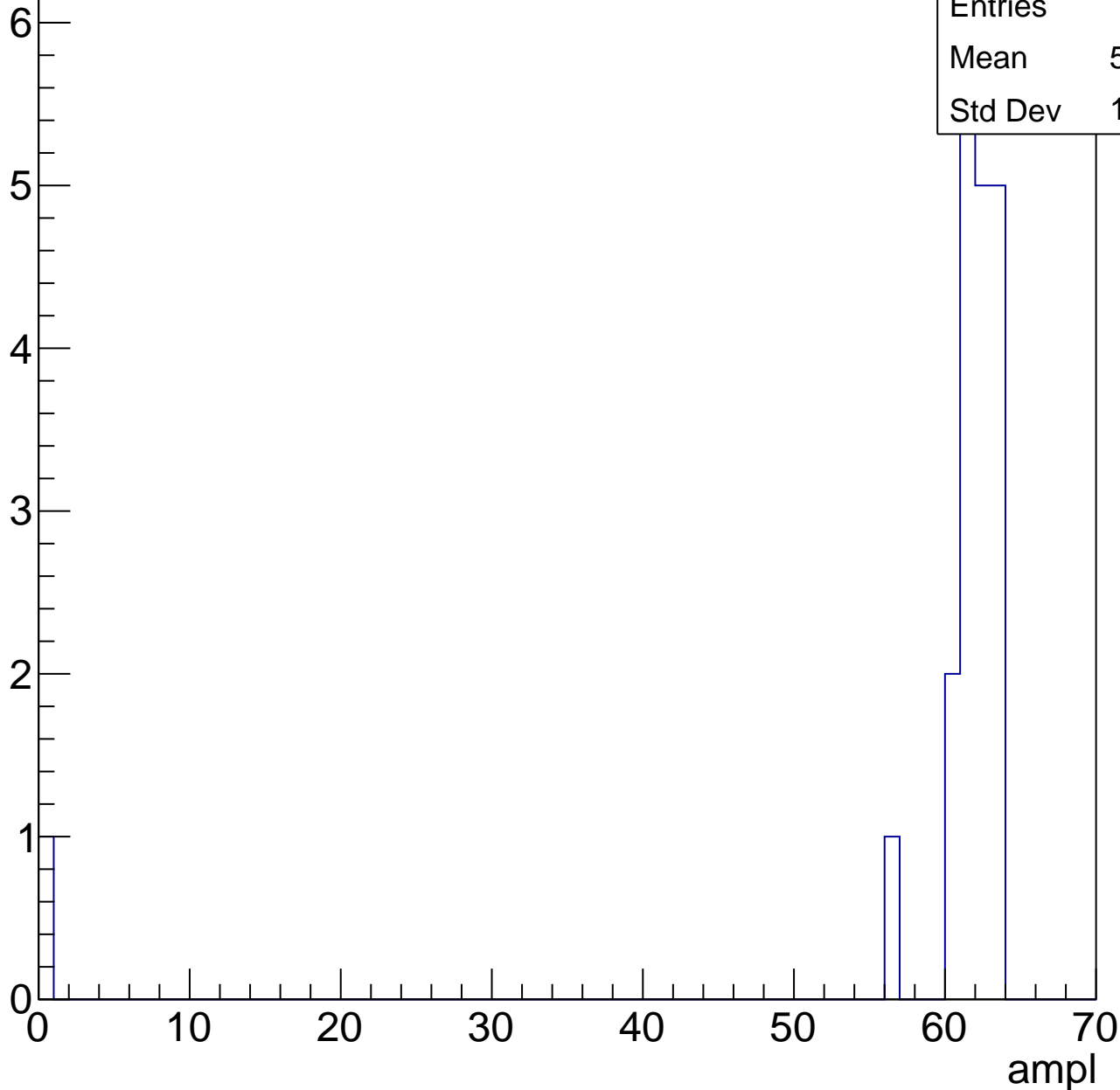
70

# B1L003S, U3-ch78, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	20
Mean	58.35
Std Dev	13.48





# B1L003S, U3-ch78, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L003S, U3-ch79, adc0

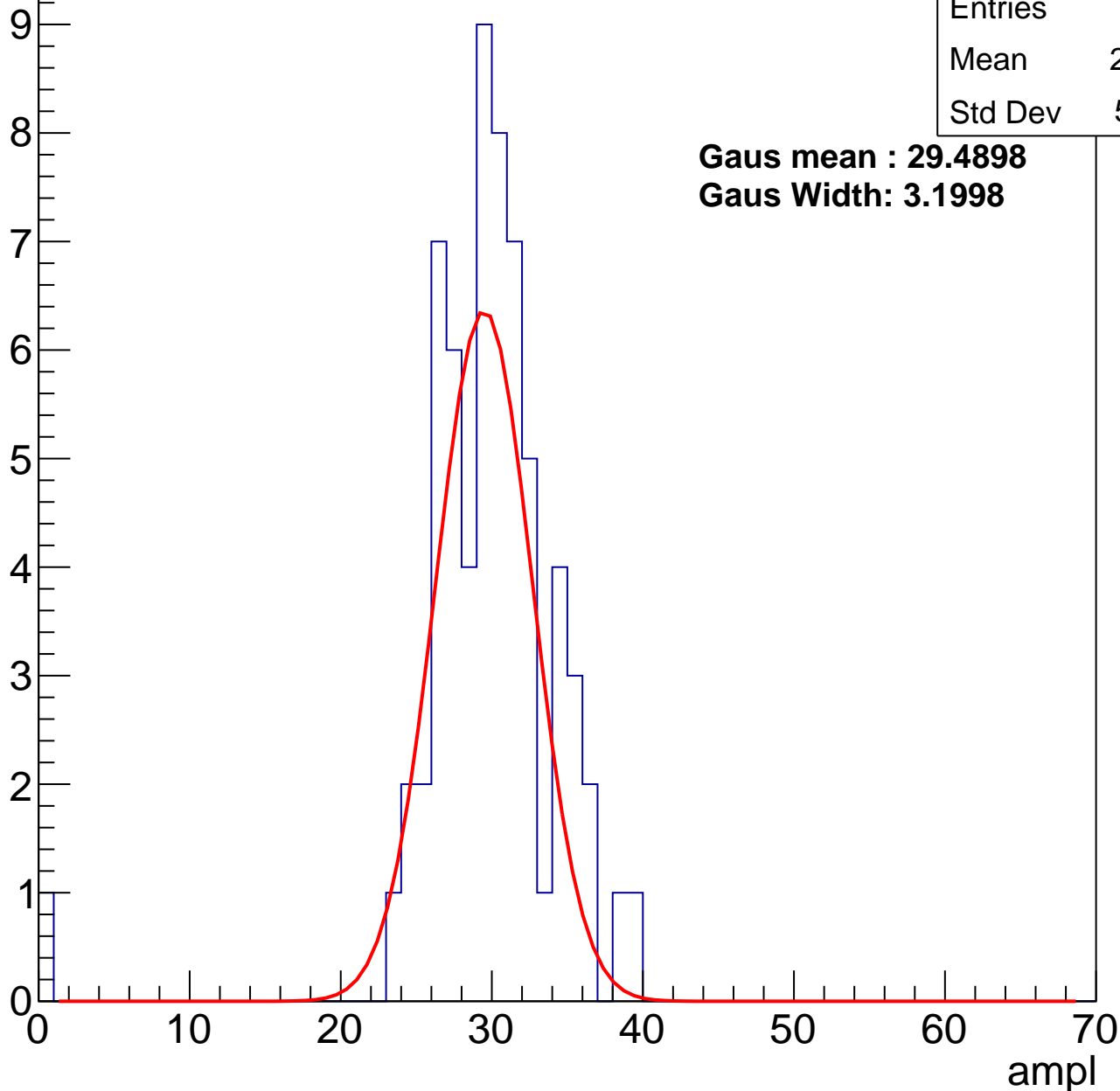
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	29.34
Std Dev	5.041

**Gaus mean : 29.4898**

**Gaus Width: 3.1998**



# B1L003S, U3-ch79, adc1

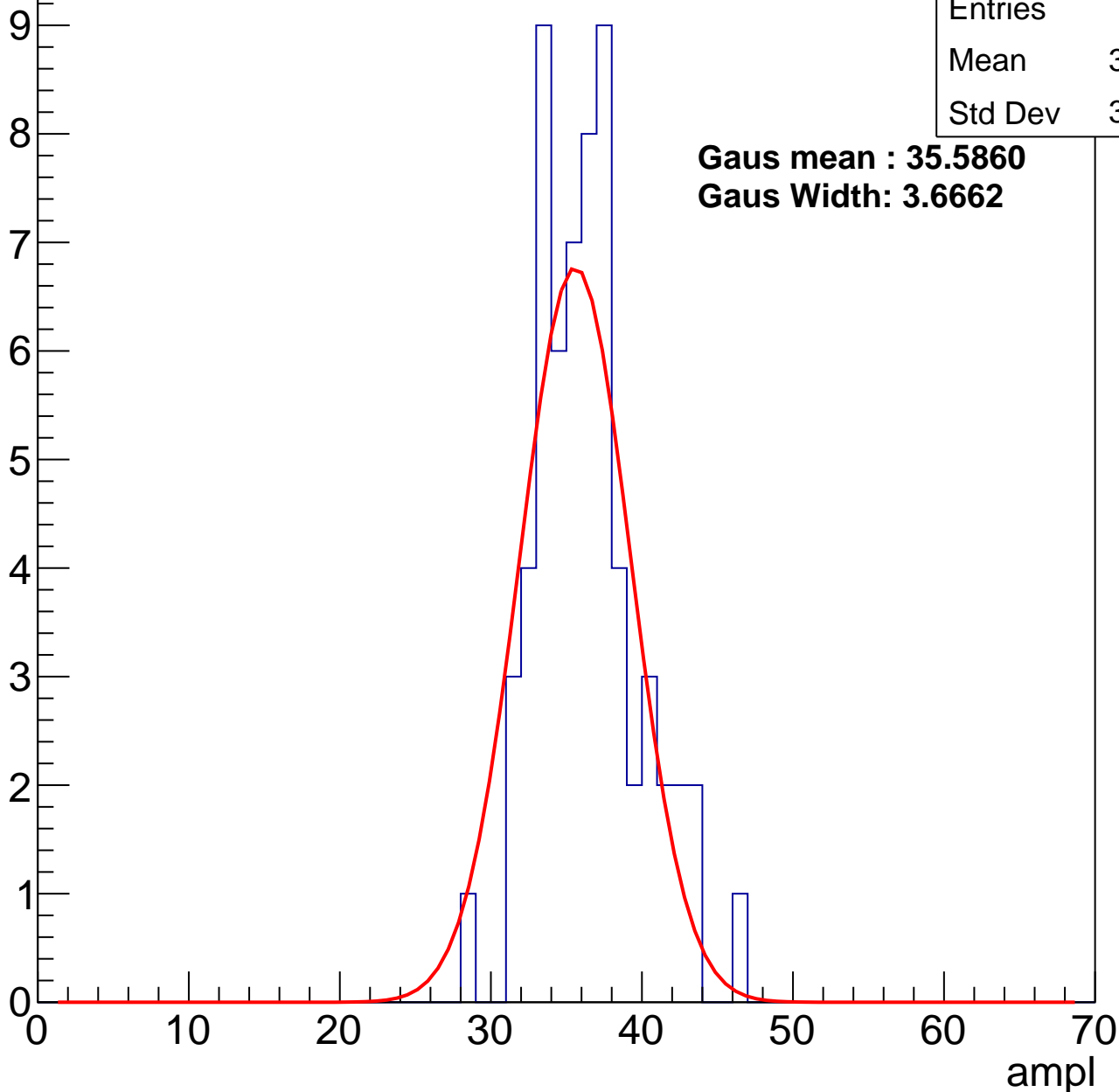
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	35.94
Std Dev	3.394

**Gaus mean : 35.5860**

**Gaus Width: 3.6662**



# B1L003S, U3-ch79, adc2

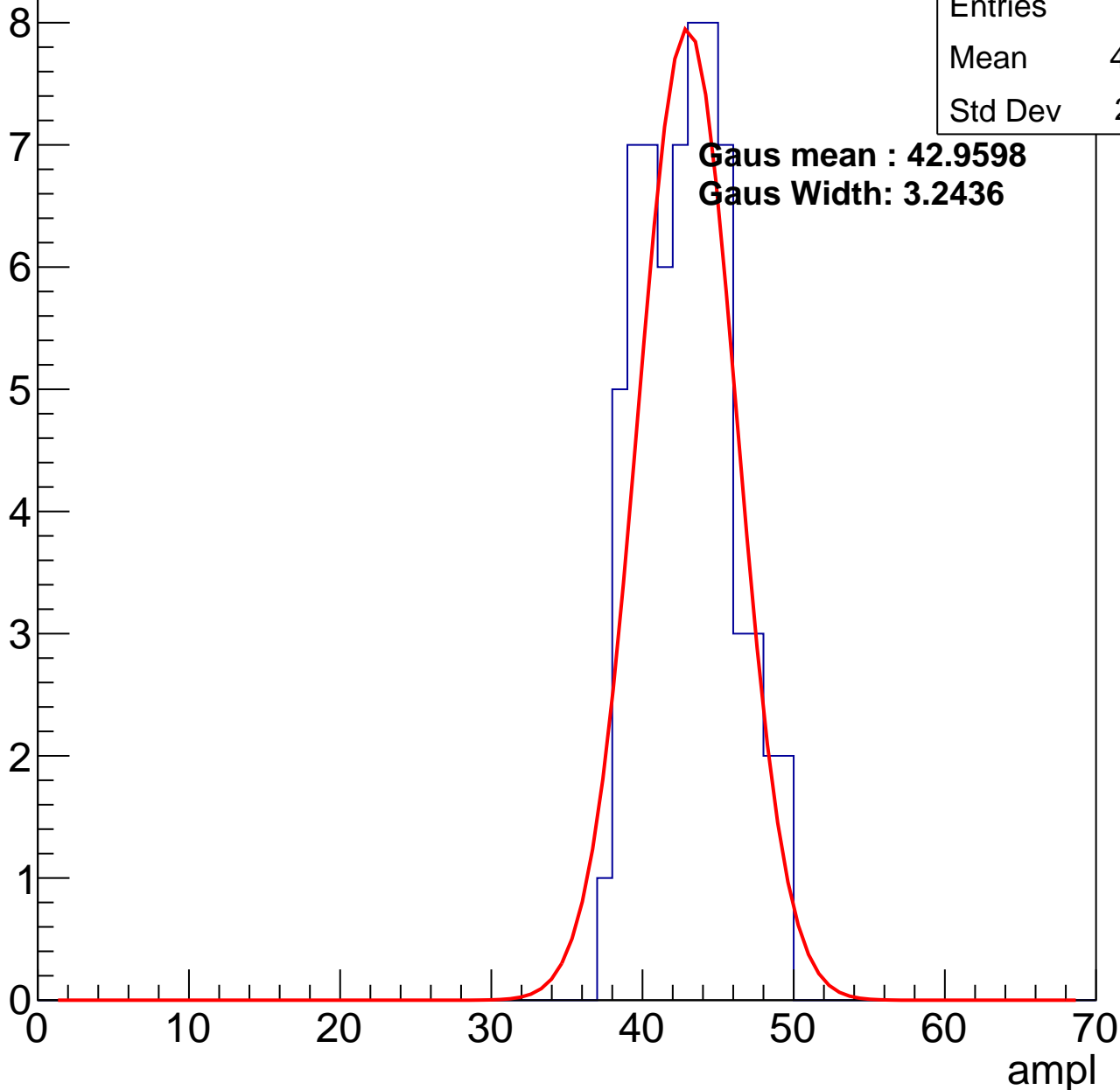
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	42.48
Std Dev	2.971

**Gaus mean : 42.9598**

**Gaus Width: 3.2436**

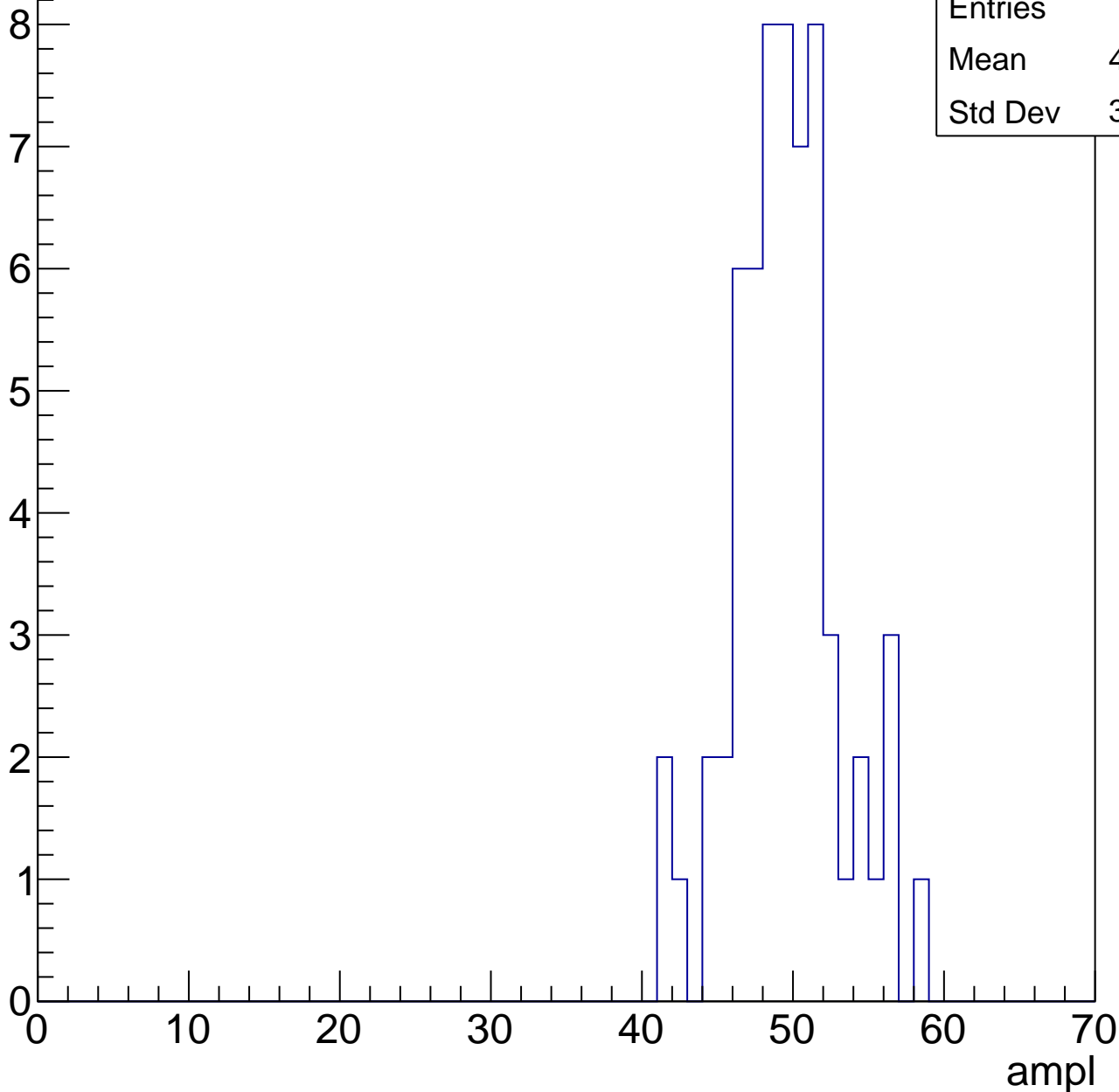


# B1L003S, U3-ch79, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

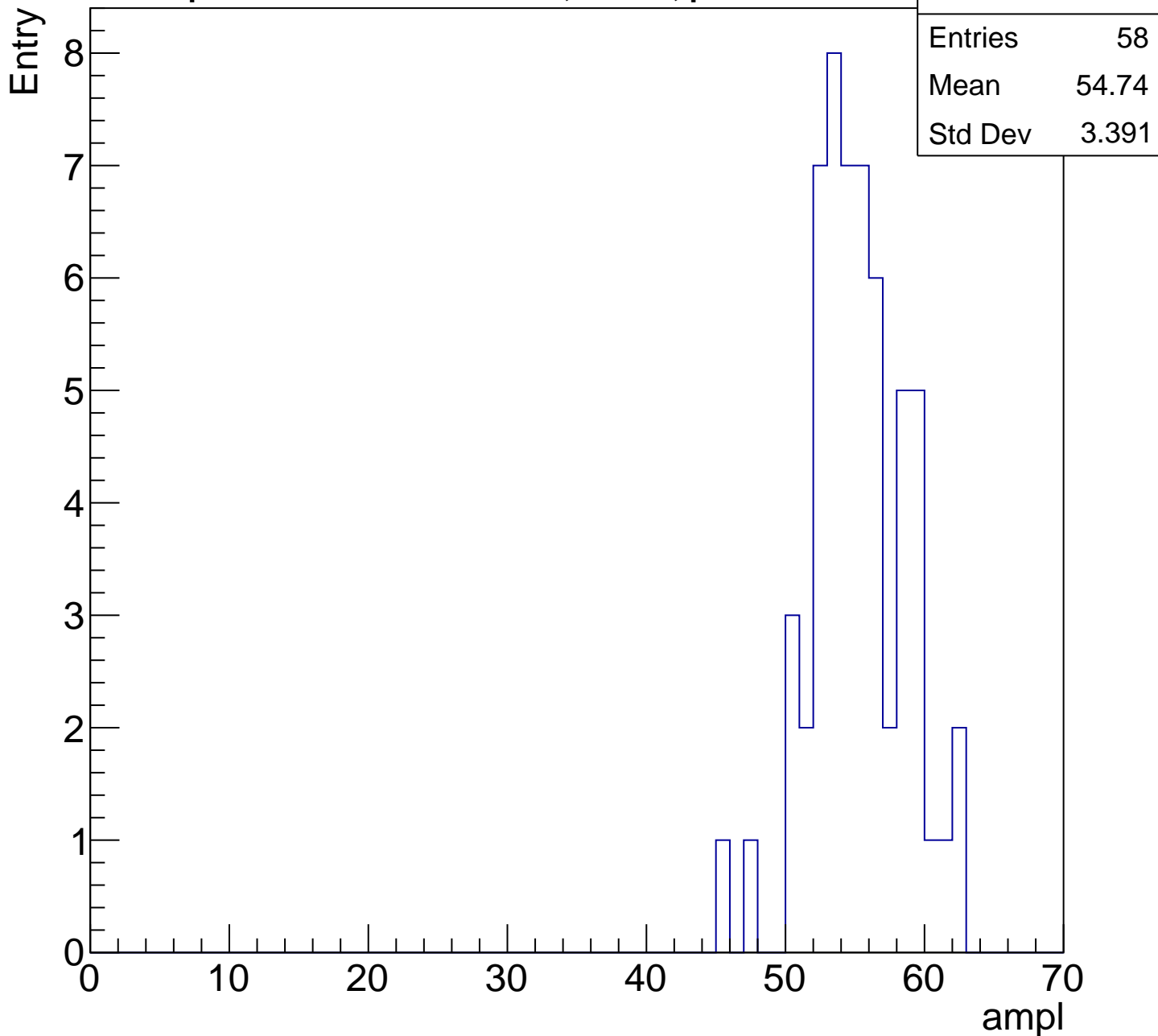
Entry

Entries	61
Mean	49.05
Std Dev	3.485



# B1L003S, U3-ch79, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

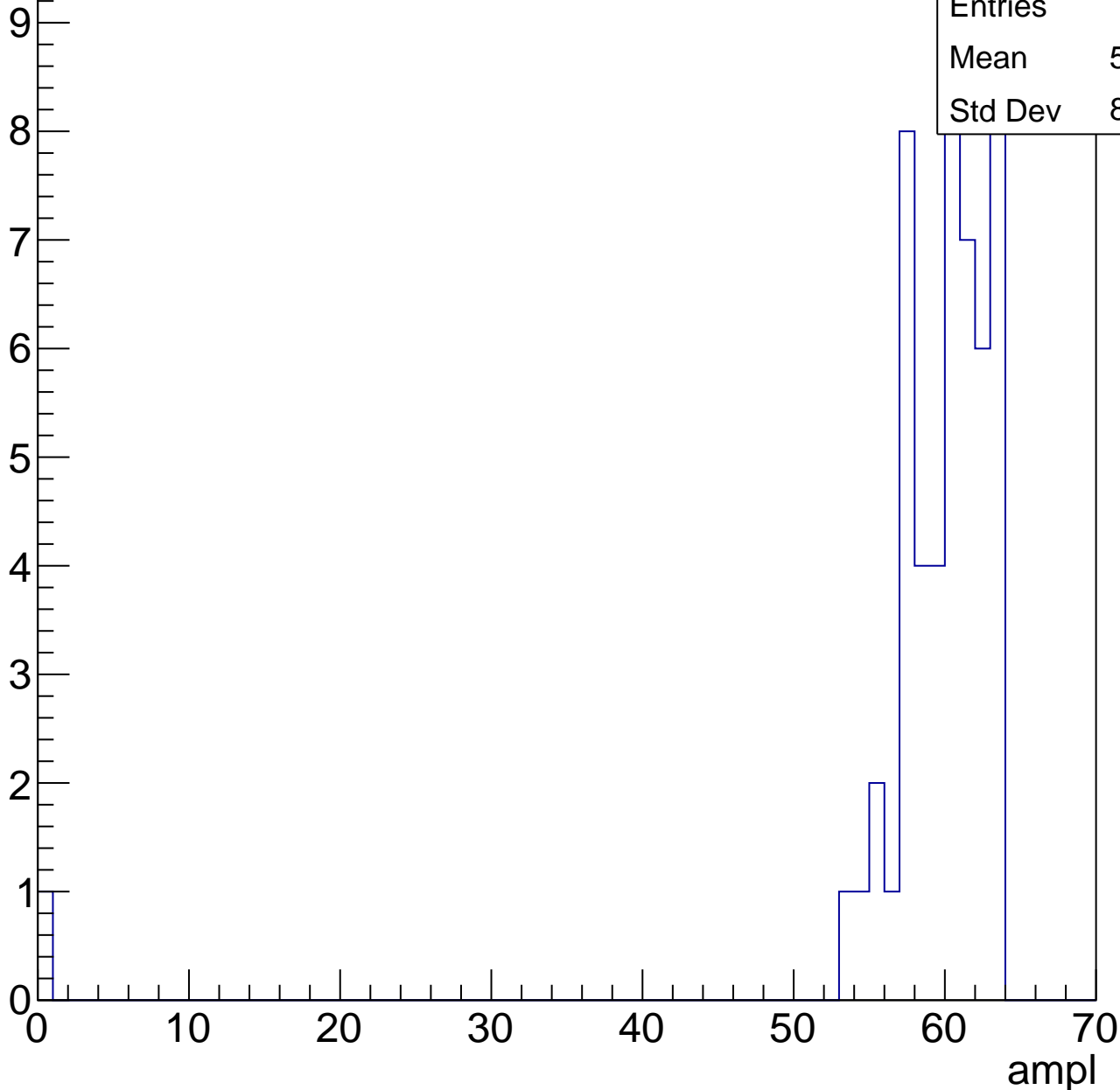


# B1L003S, U3-ch79, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

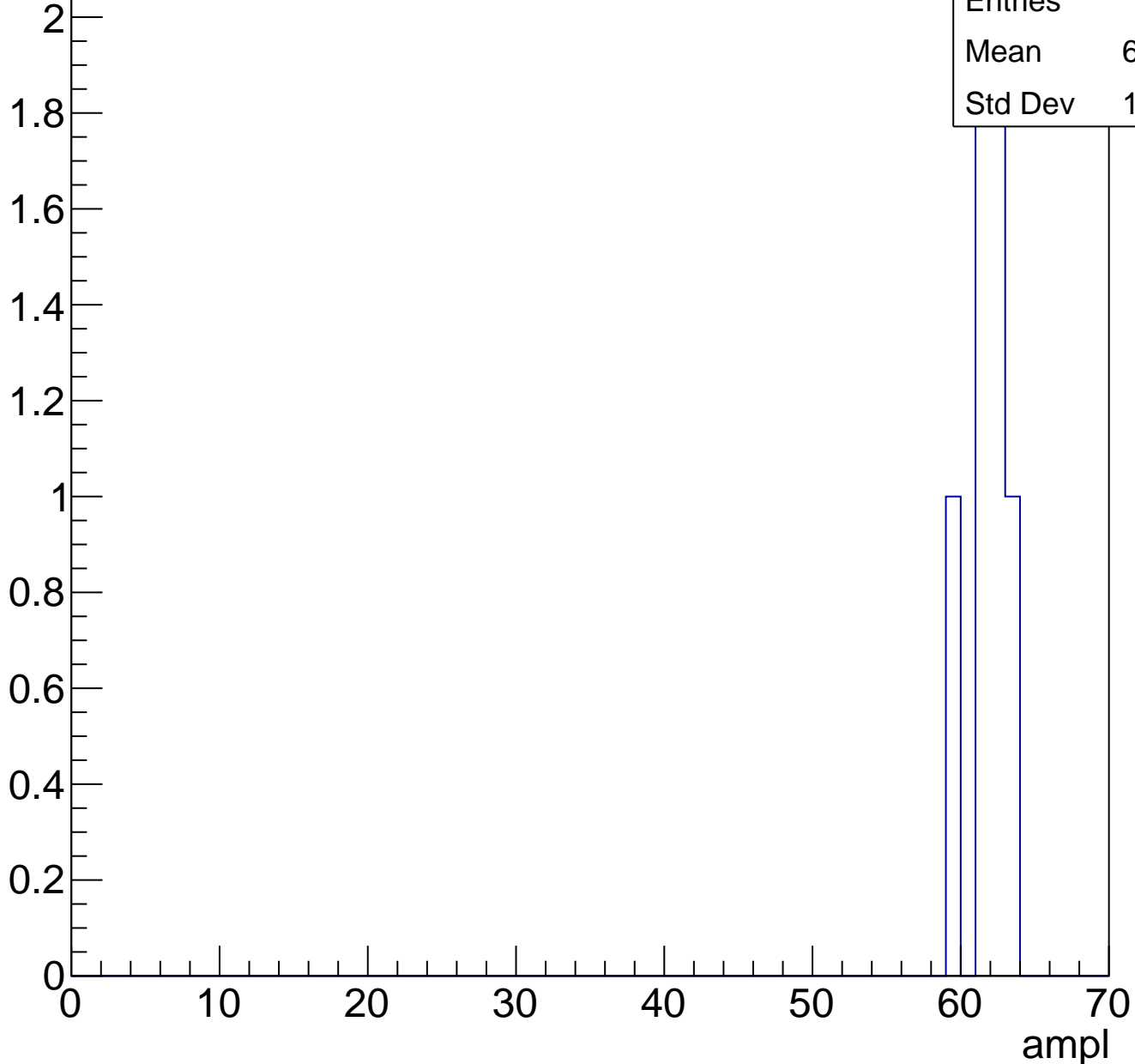
Entries	53
Mean	58.55
Std Dev	8.515



# B1L003S, U3-ch79, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch79, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L003S, U3-ch80, adc0

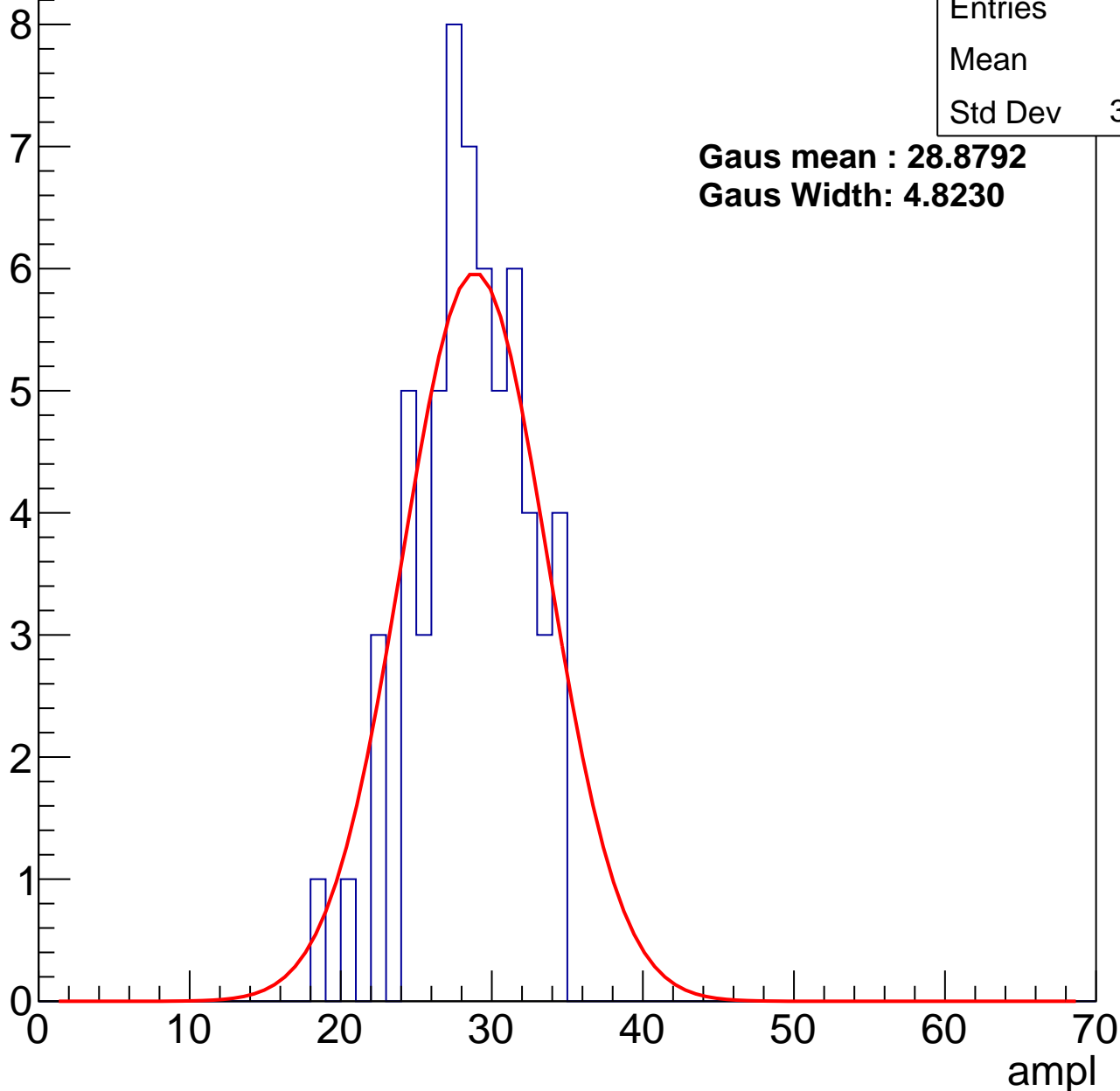
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	28.1
Std Dev	3.552

**Gaus mean : 28.8792**

**Gaus Width: 4.8230**



# B1L003S, U3-ch80, adc1

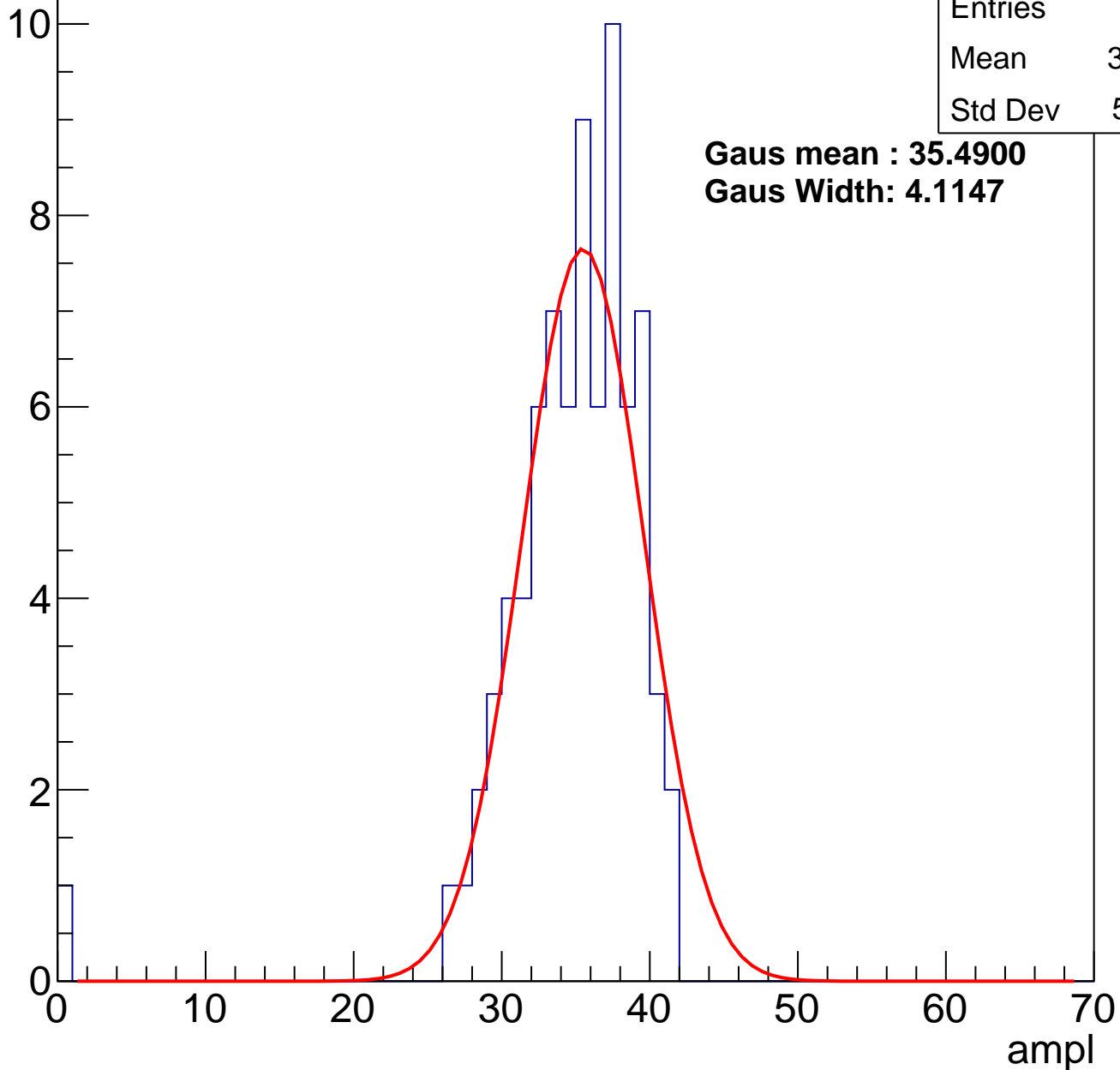
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	78
Mean	34.24
Std Dev	5.241

**Gaus mean : 35.4900**

**Gaus Width: 4.1147**

Entry



# B1L003S, U3-ch80, adc2

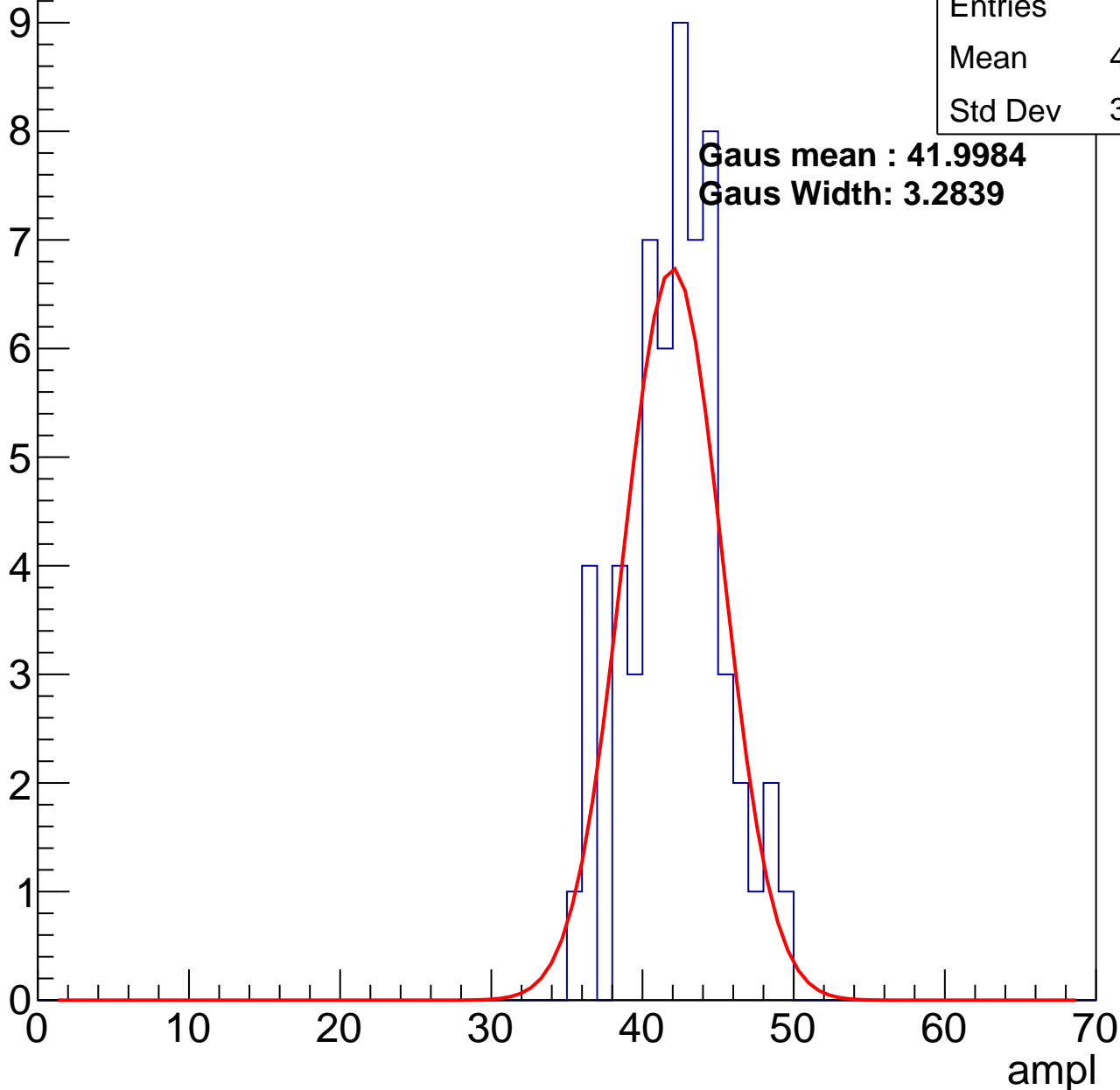
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	41.79
Std Dev	3.106

**Gaus mean : 41.9984**

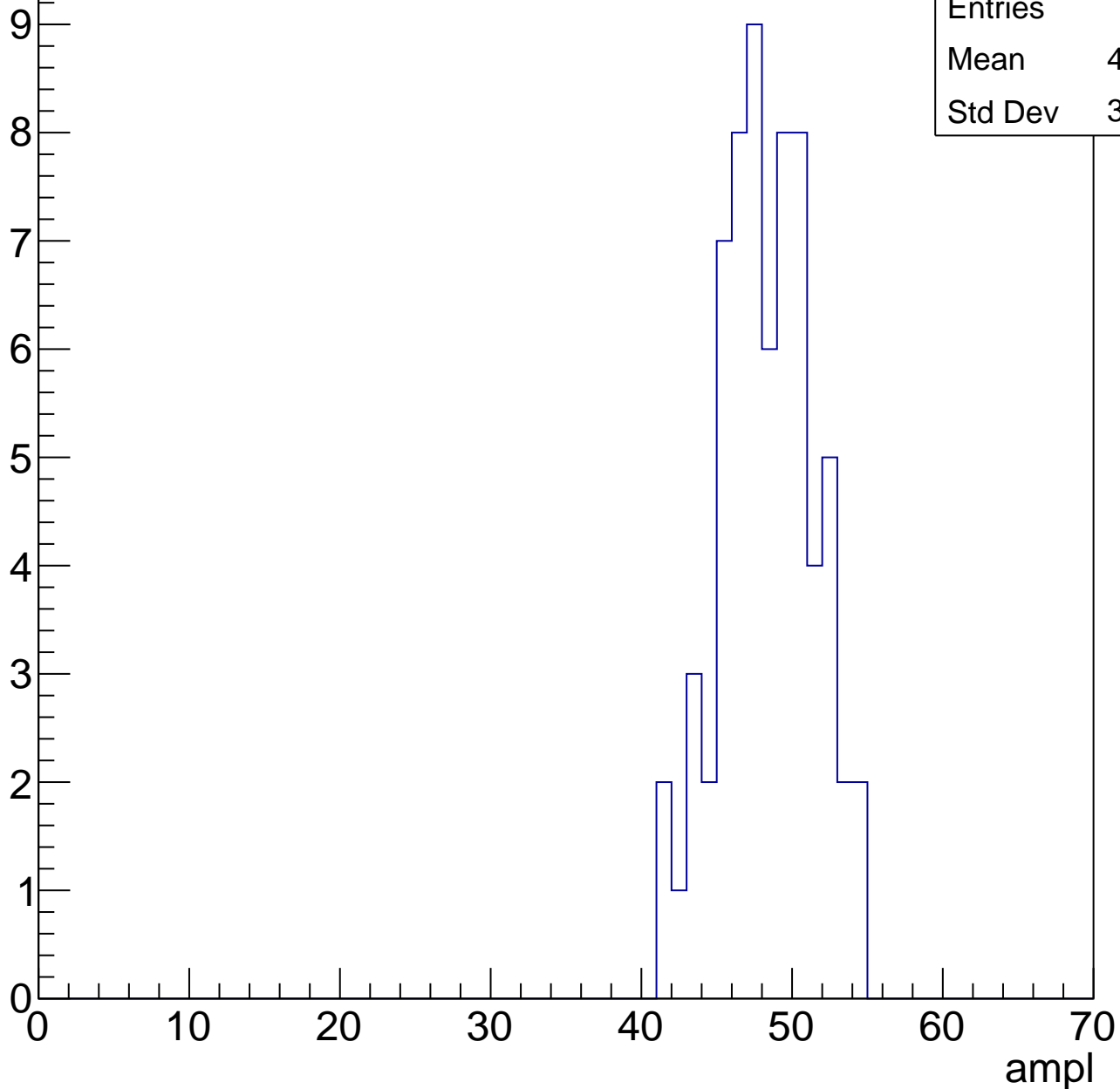
**Gaus Width: 3.2839**



# B1L003S, U3-ch80, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



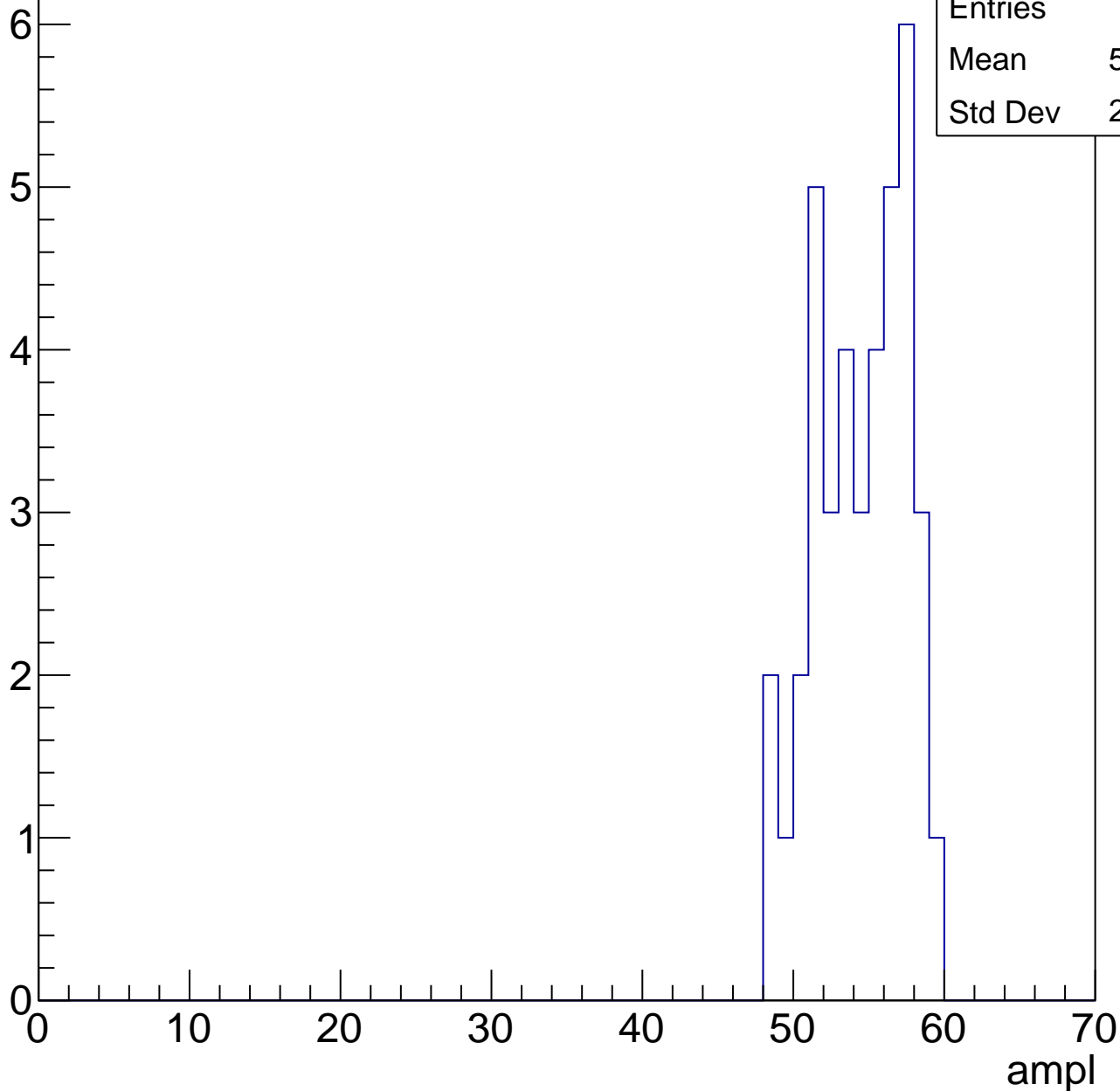
Entries	67
Mean	47.84
Std Dev	3.045

# B1L003S, U3-ch80, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	39
Mean	53.97
Std Dev	2.957

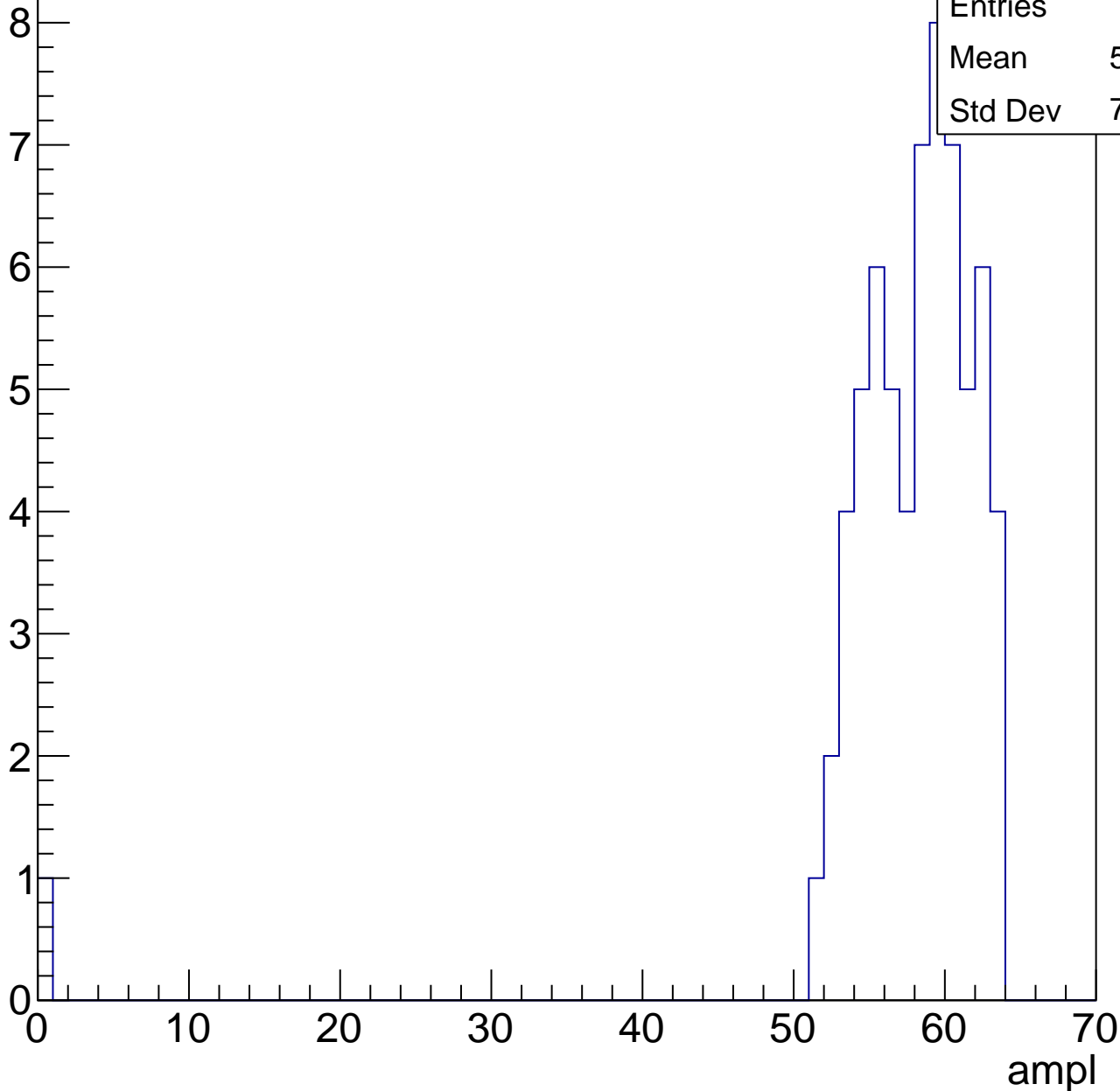


# B1L003S, U3-ch80, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	56.95
Std Dev	7.794

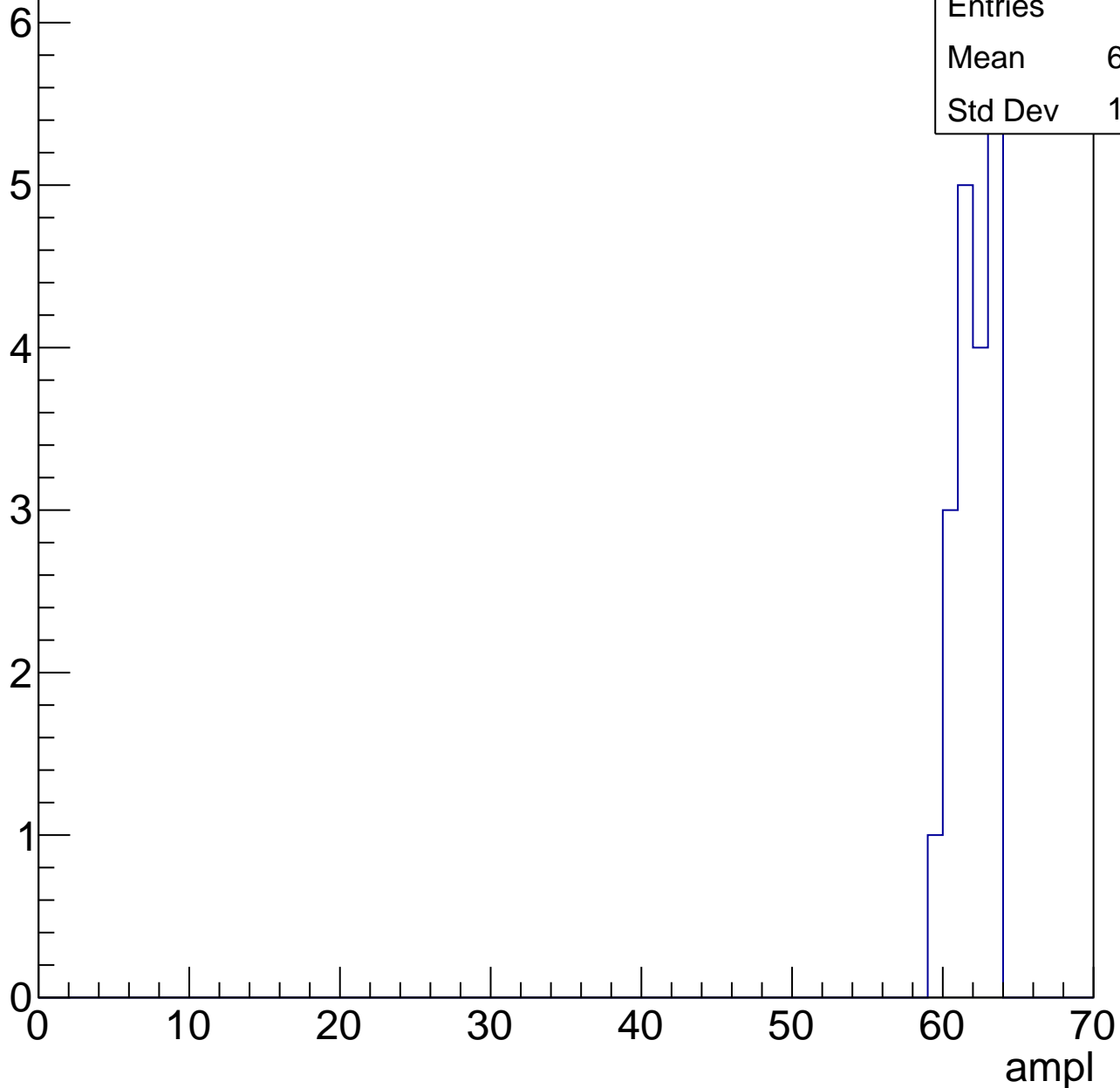


# B1L003S, U3-ch80, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	19
Mean	61.58
Std Dev	1.228





# B1L003S, U3-ch80, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U3-ch81, adc0

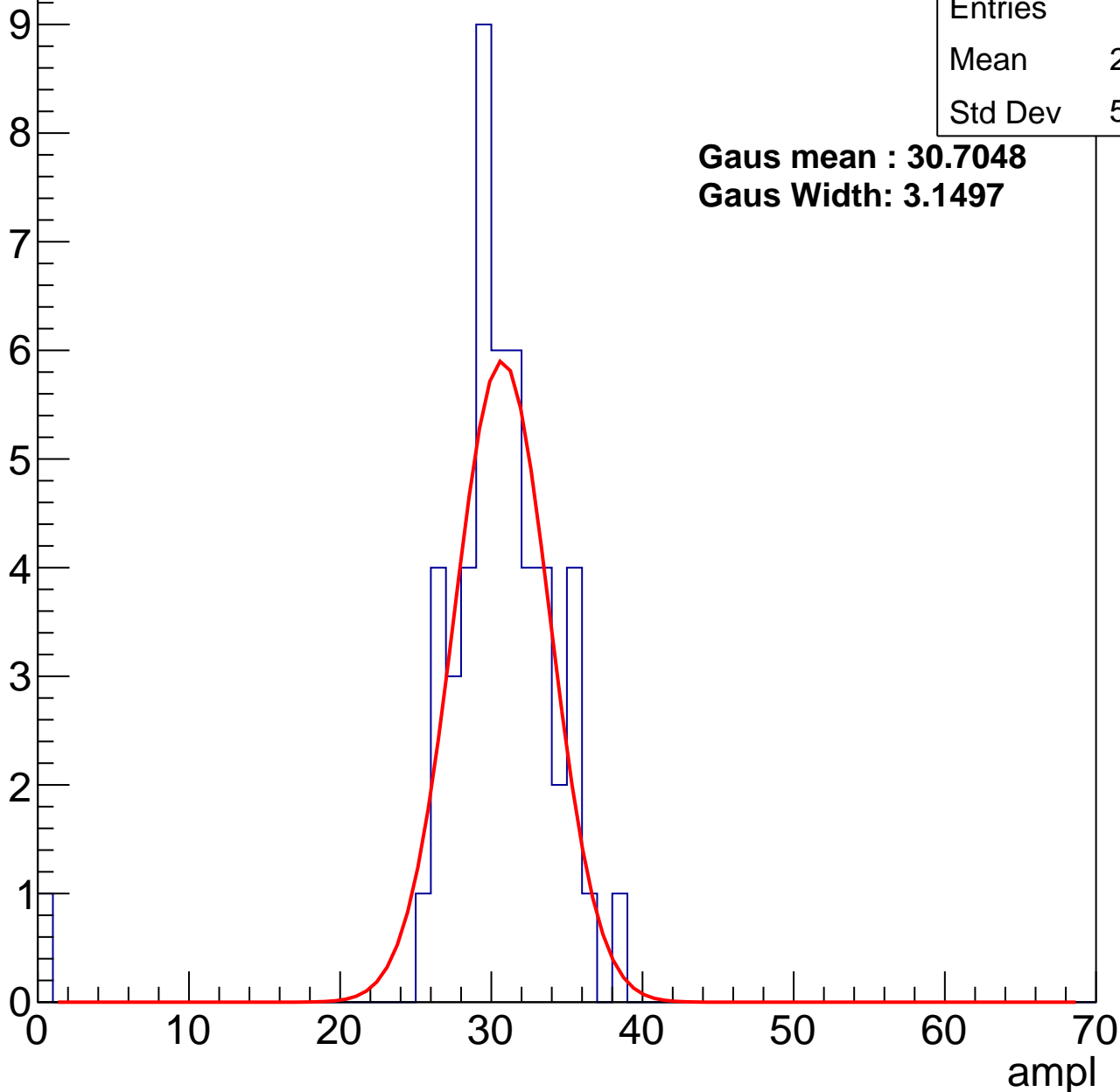
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	50
Mean	29.82
Std Dev	5.156

**Gaus mean : 30.7048**

**Gaus Width: 3.1497**



# B1L003S, U3-ch81, adc1

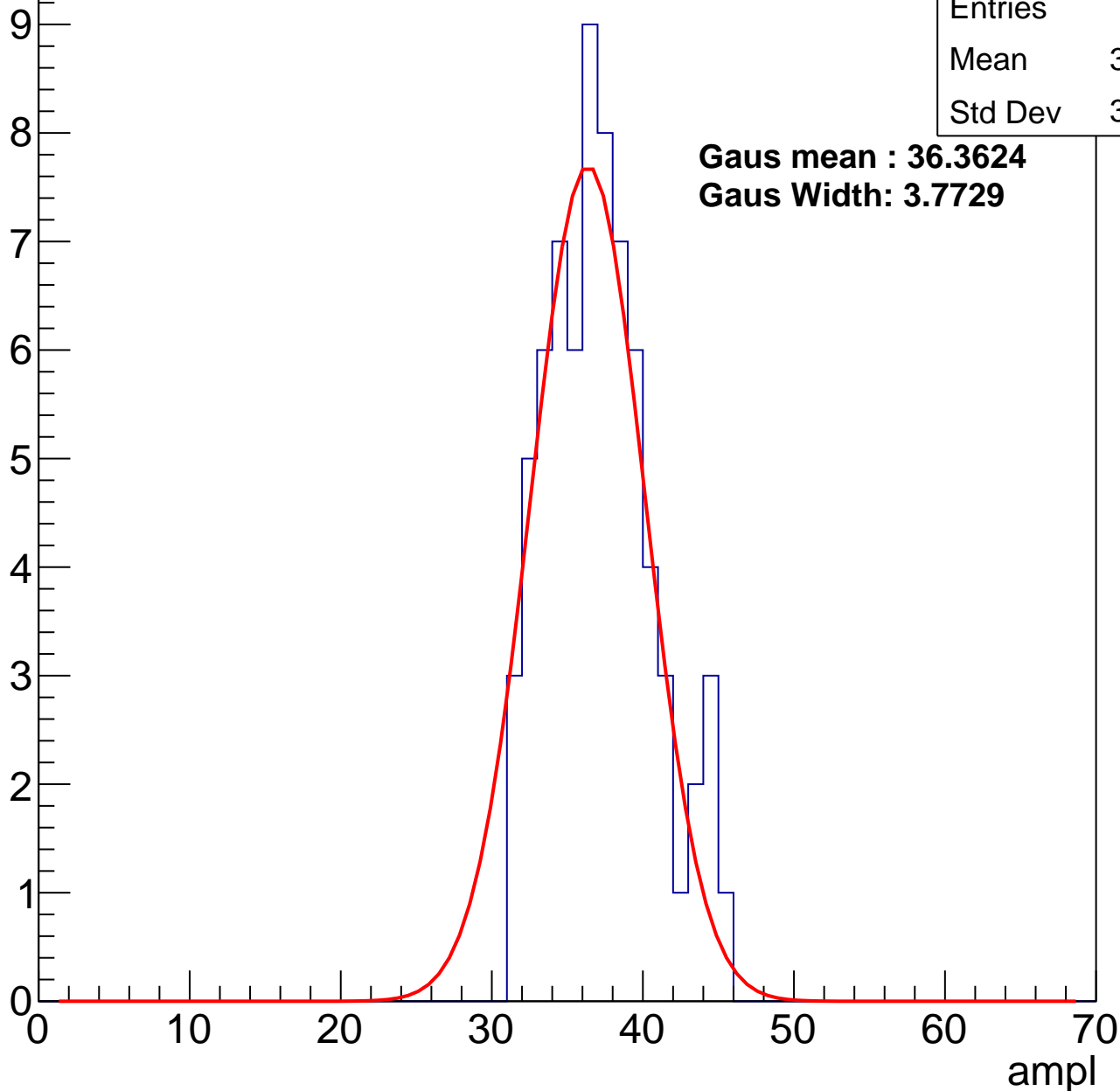
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	71
Mean	36.72
Std Dev	3.444

**Gaus mean : 36.3624**

**Gaus Width: 3.7729**



# B1L003S, U3-ch81, adc2

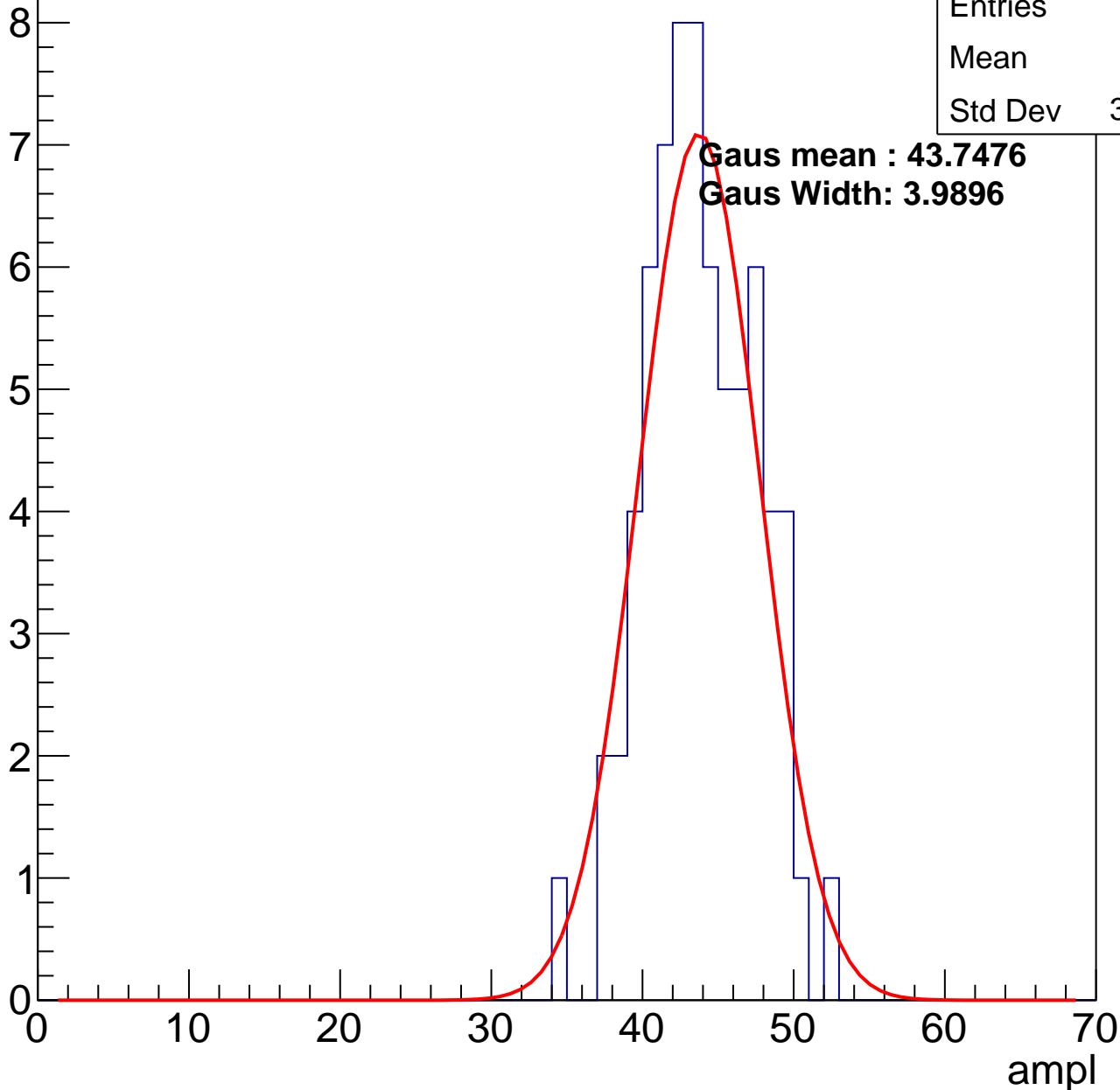
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	43.4
Std Dev	3.559

**Gaus mean : 43.7476**

**Gaus Width: 3.9896**

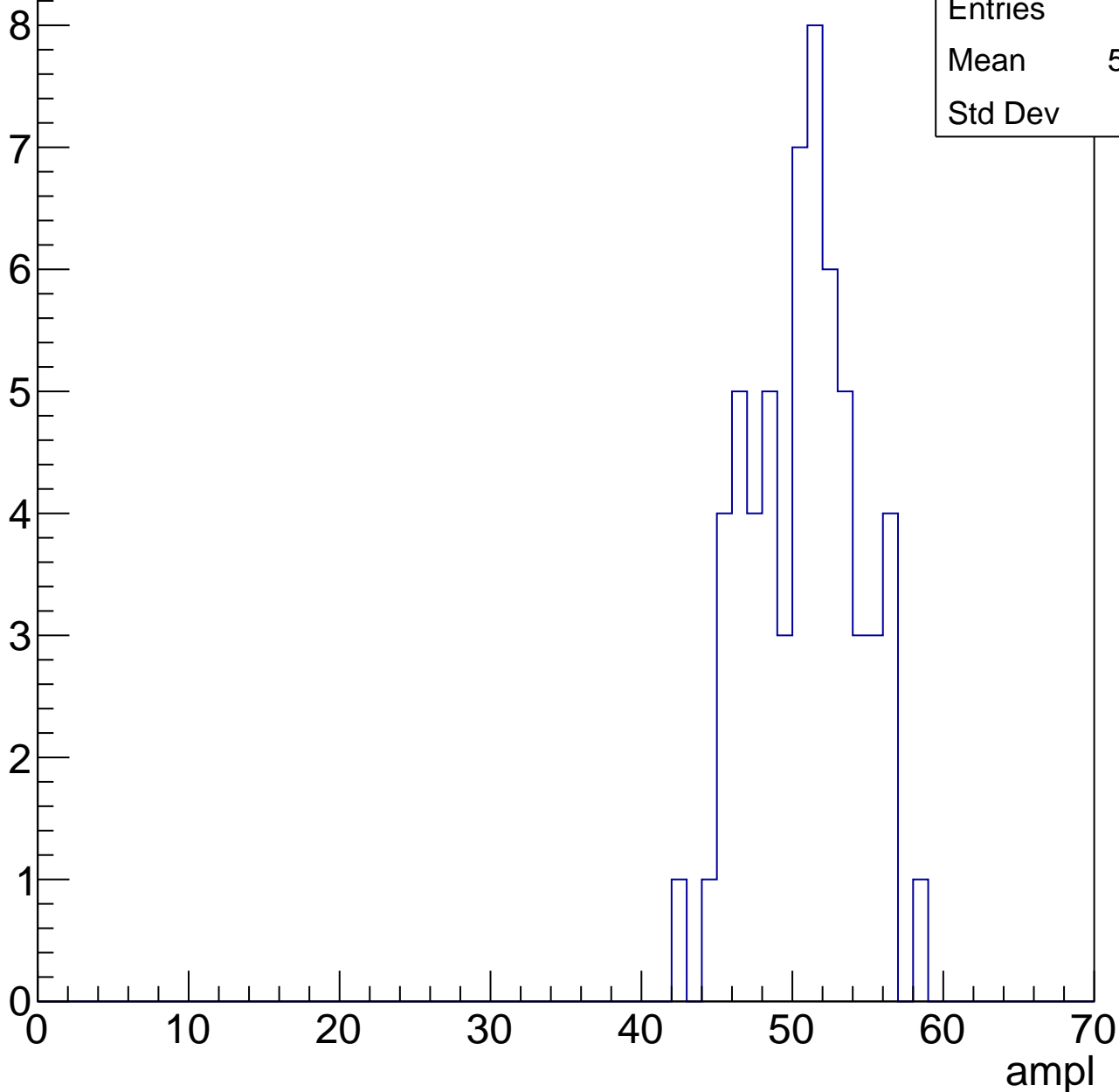


# B1L003S, U3-ch81, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	50.25
Std Dev	3.52



# B1L003S, U3-ch81, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

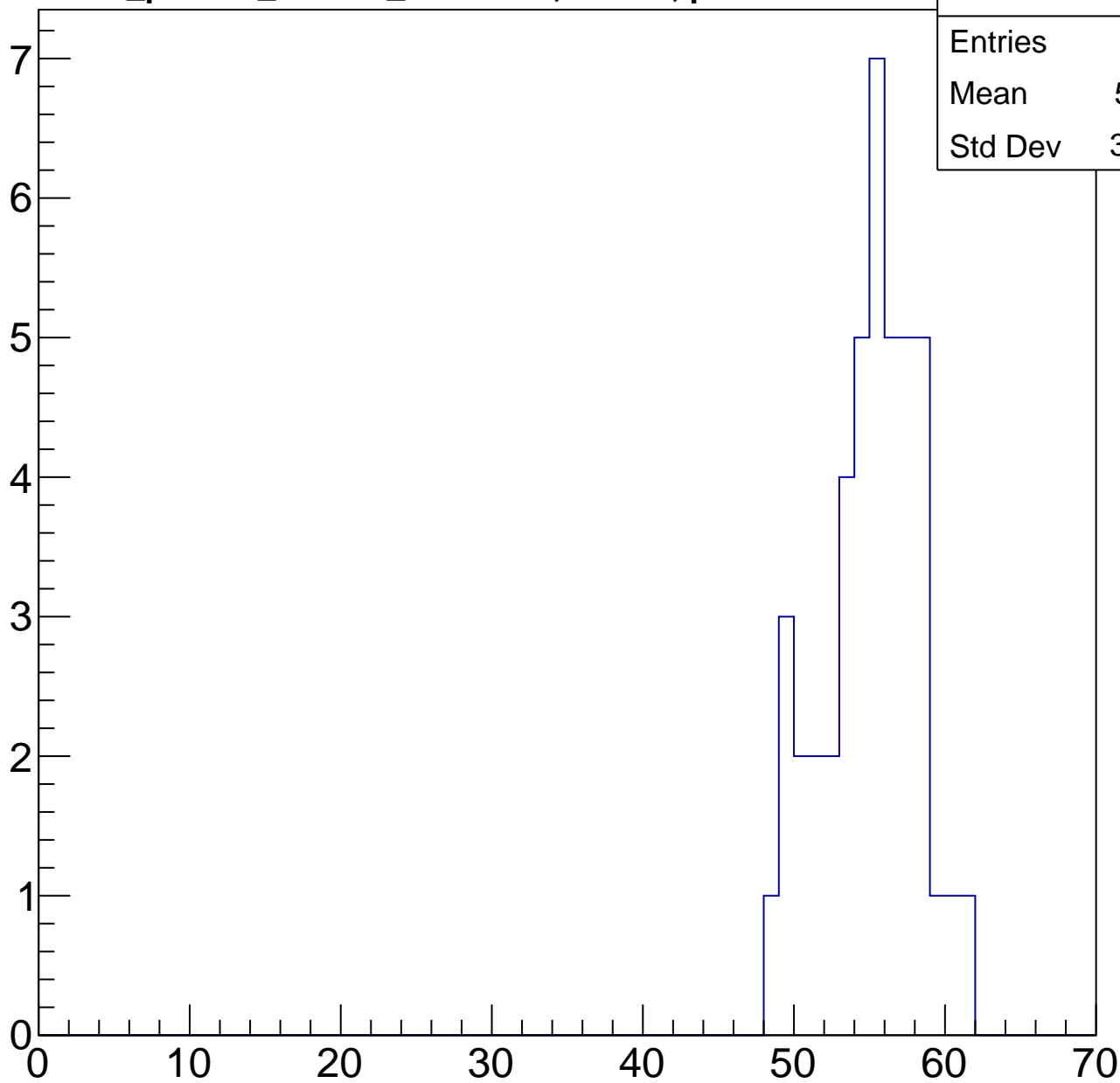
Entry

7  
6  
5  
4  
3  
2  
1  
0

Entries	44
Mean	54.61
Std Dev	3.084

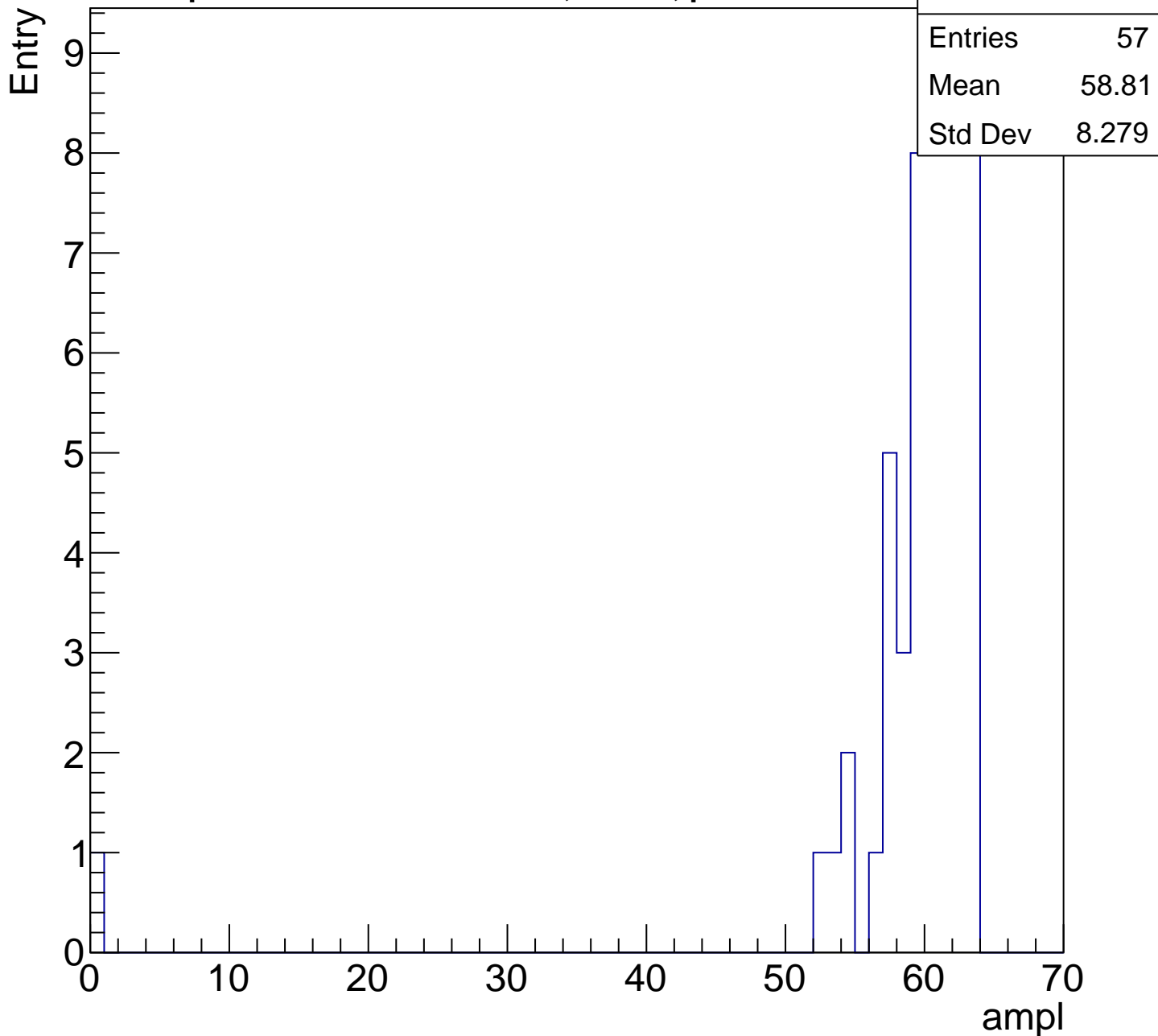
ampl

0 10 20 30 40 50 60 70



# B1L003S, U3-ch81, adc5

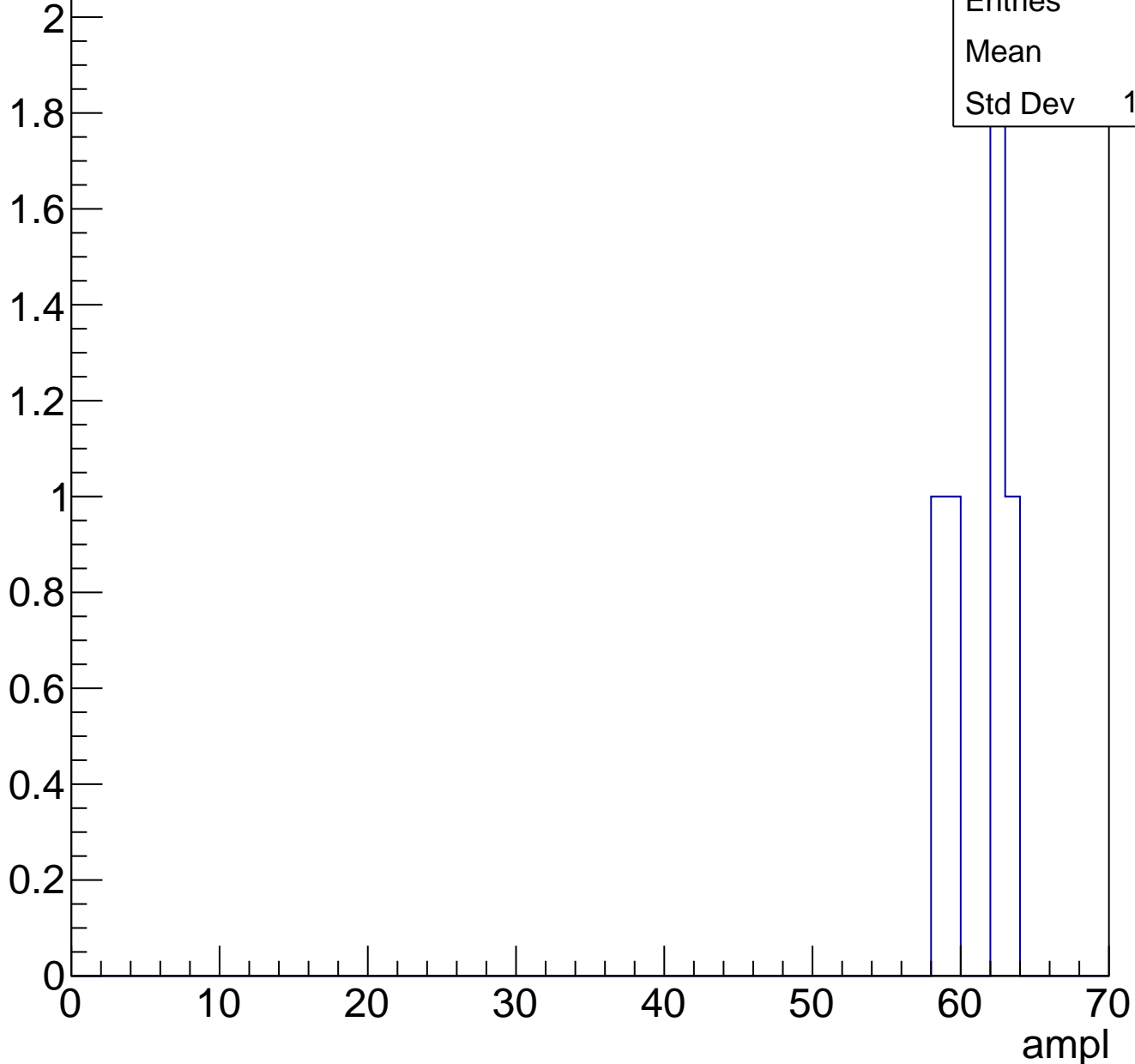
calib\_packv5\_042523\_0143.root, FC#13, port D2



# B1L003S, U3-ch81, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch81, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U3-ch82, adc0

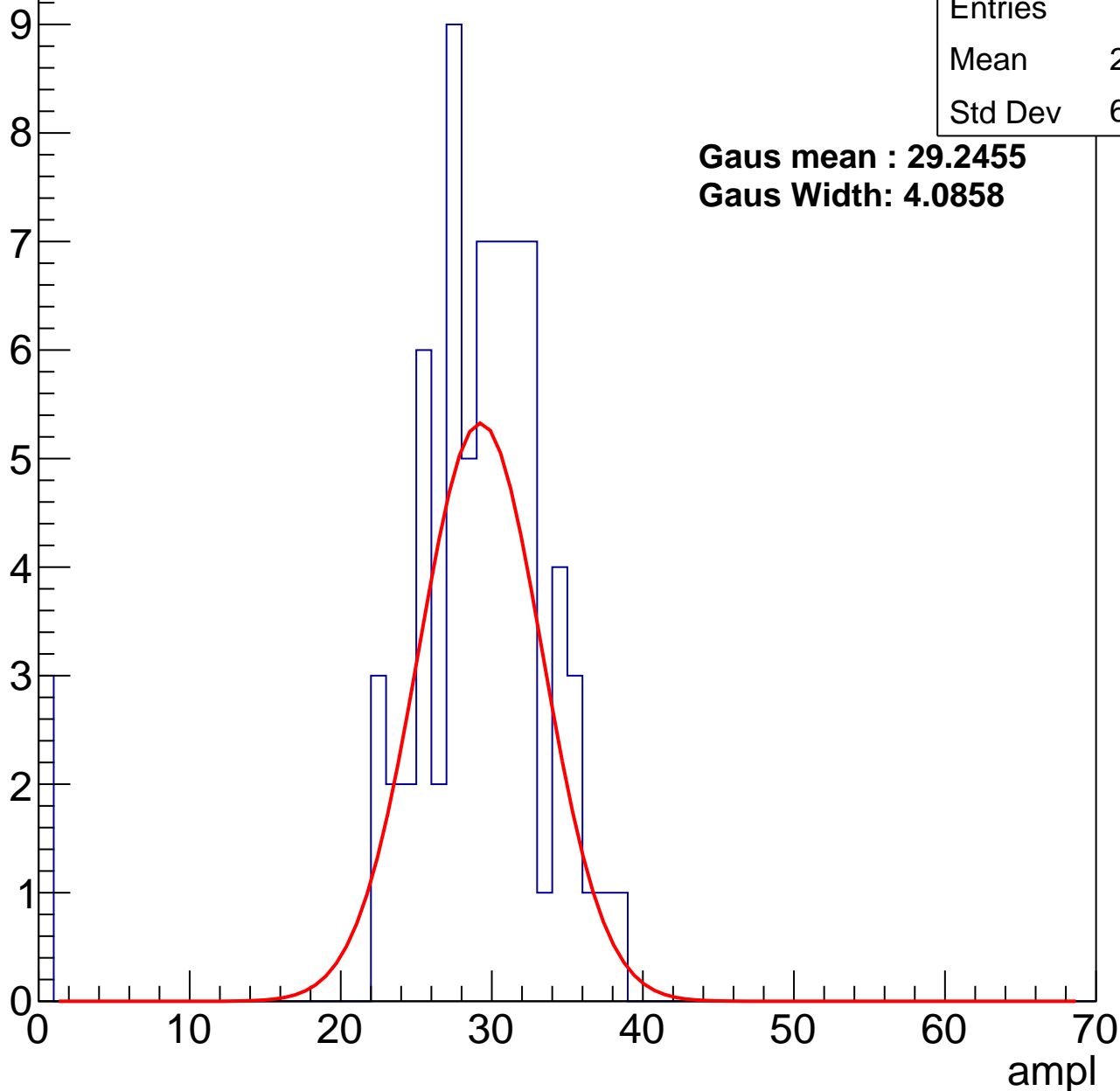
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	71
Mean	27.94
Std Dev	6.904

**Gaus mean : 29.2455**

**Gaus Width: 4.0858**



# B1L003S, U3-ch82, adc1

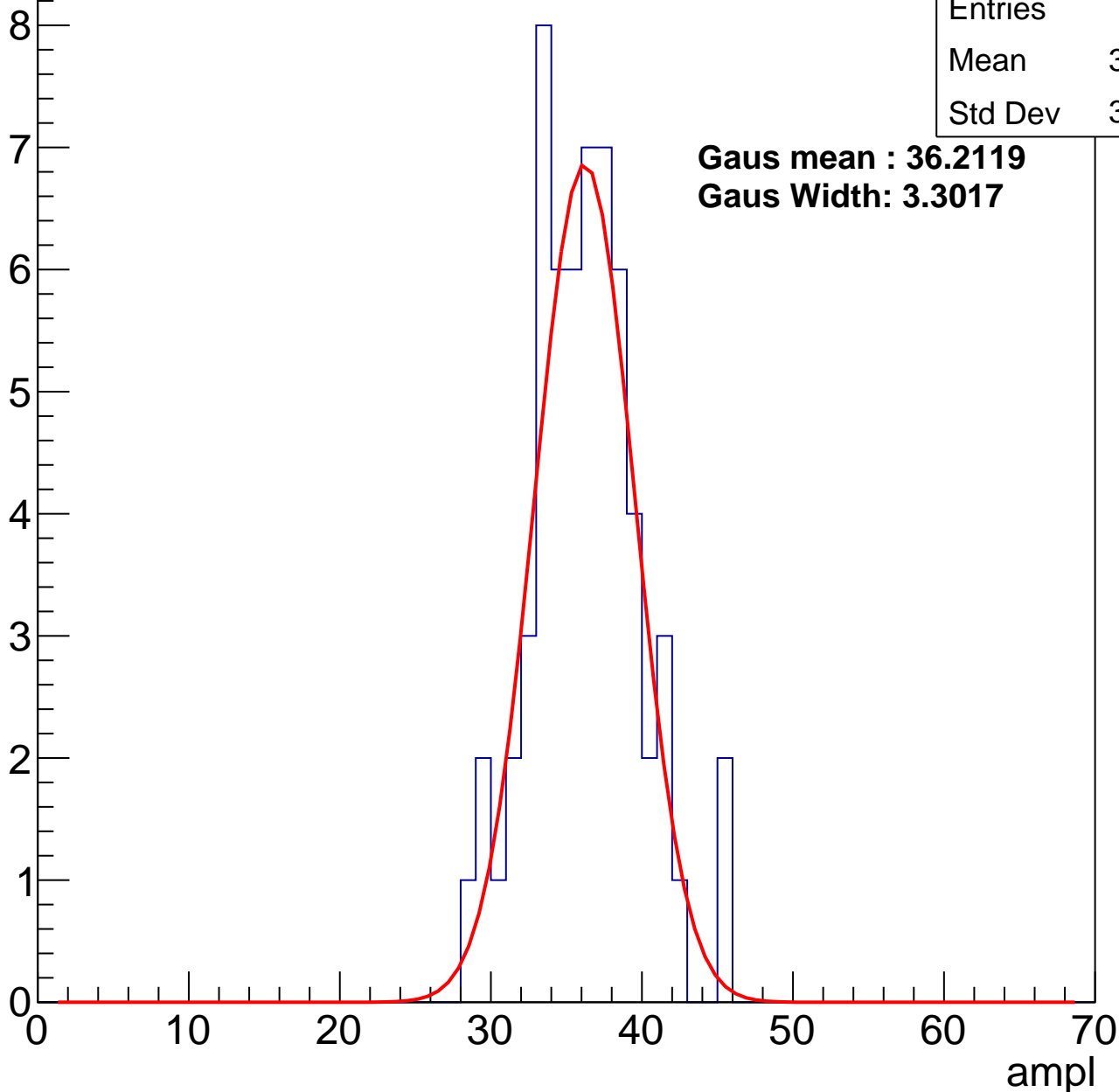
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	35.77
Std Dev	3.545

**Gaus mean : 36.2119**

**Gaus Width: 3.3017**



# B1L003S, U3-ch82, adc2

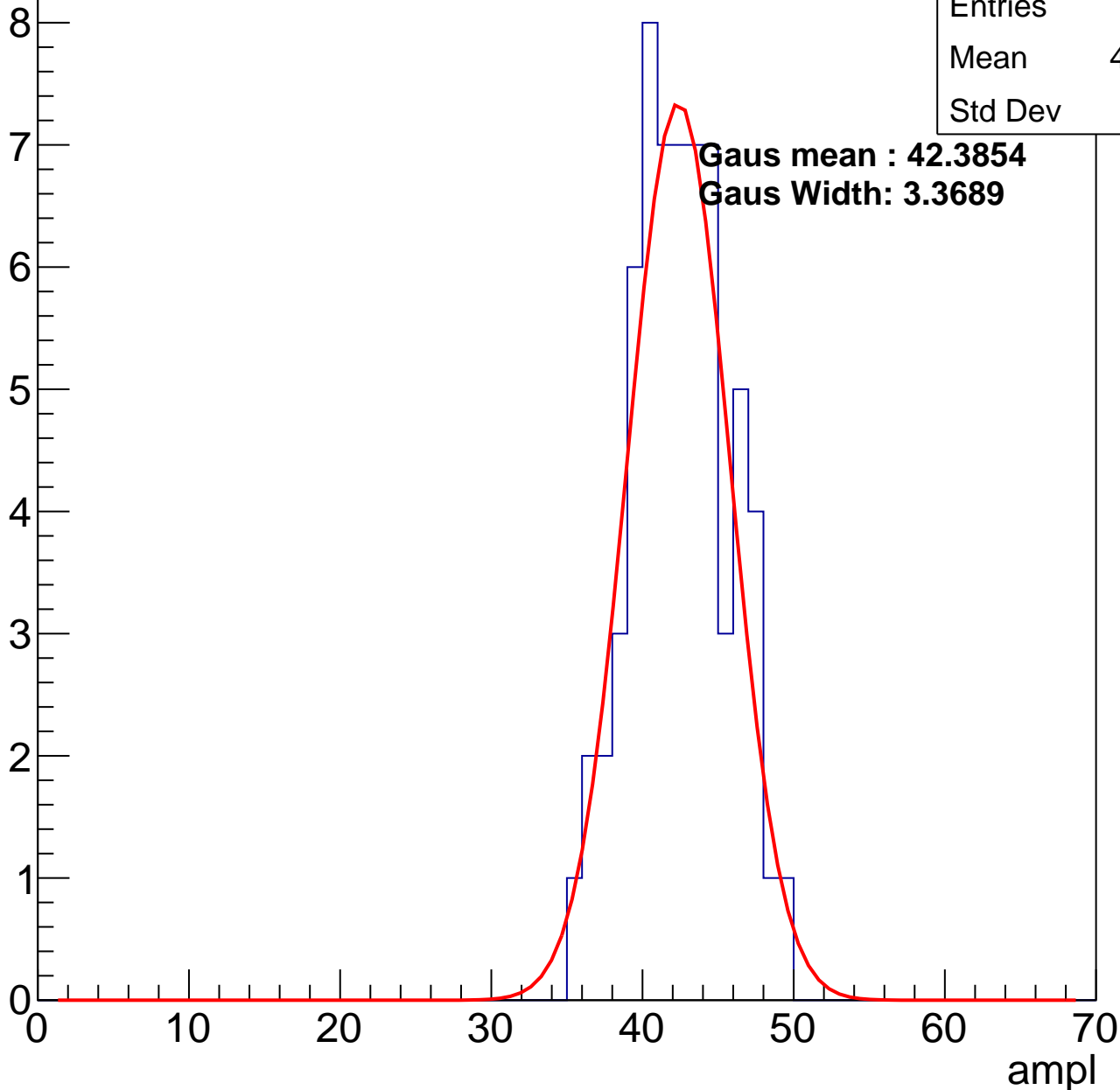
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	42.02
Std Dev	3.16

**Gaus mean : 42.3854**

**Gaus Width: 3.3689**

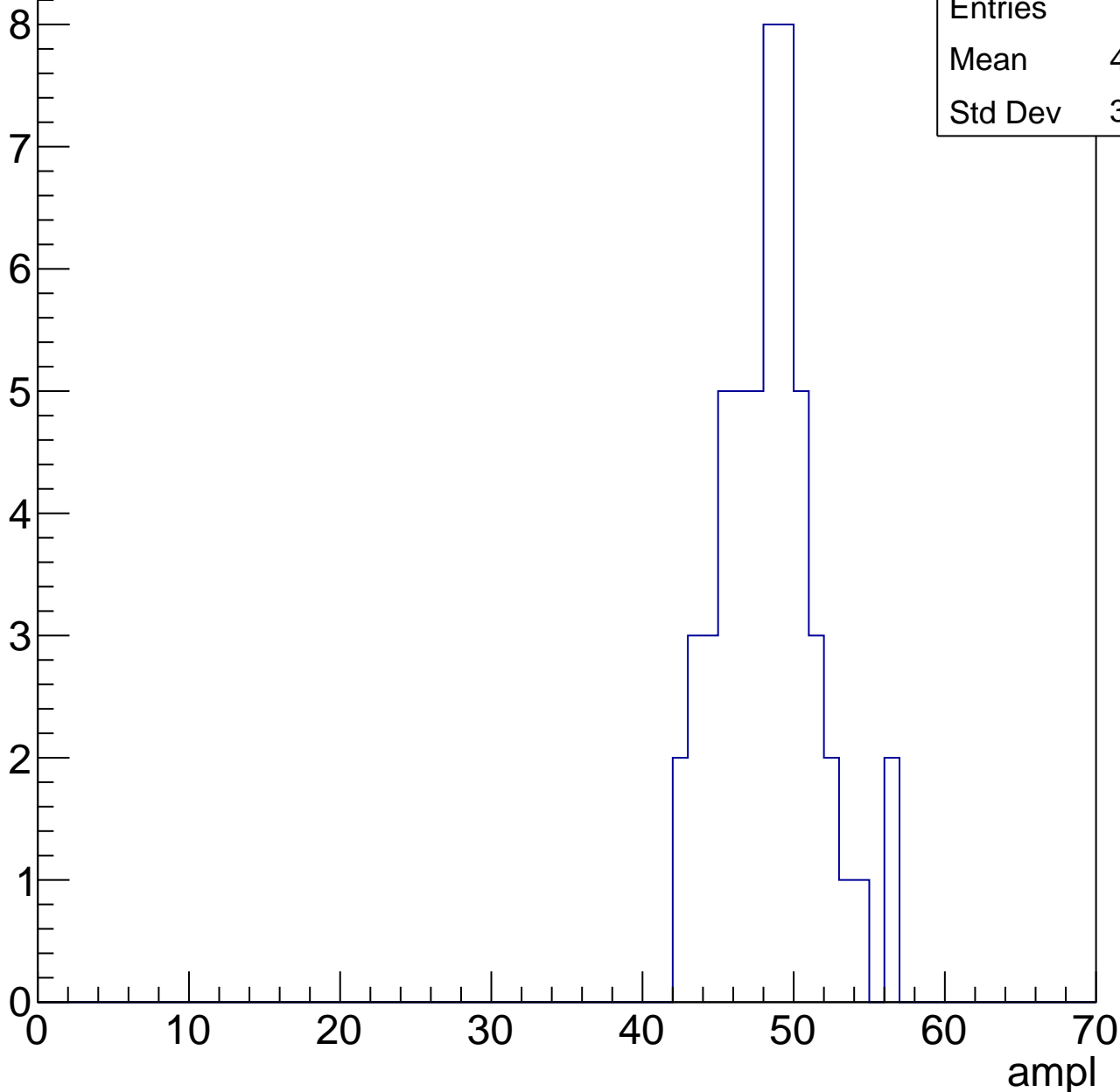


# B1L003S, U3-ch82, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

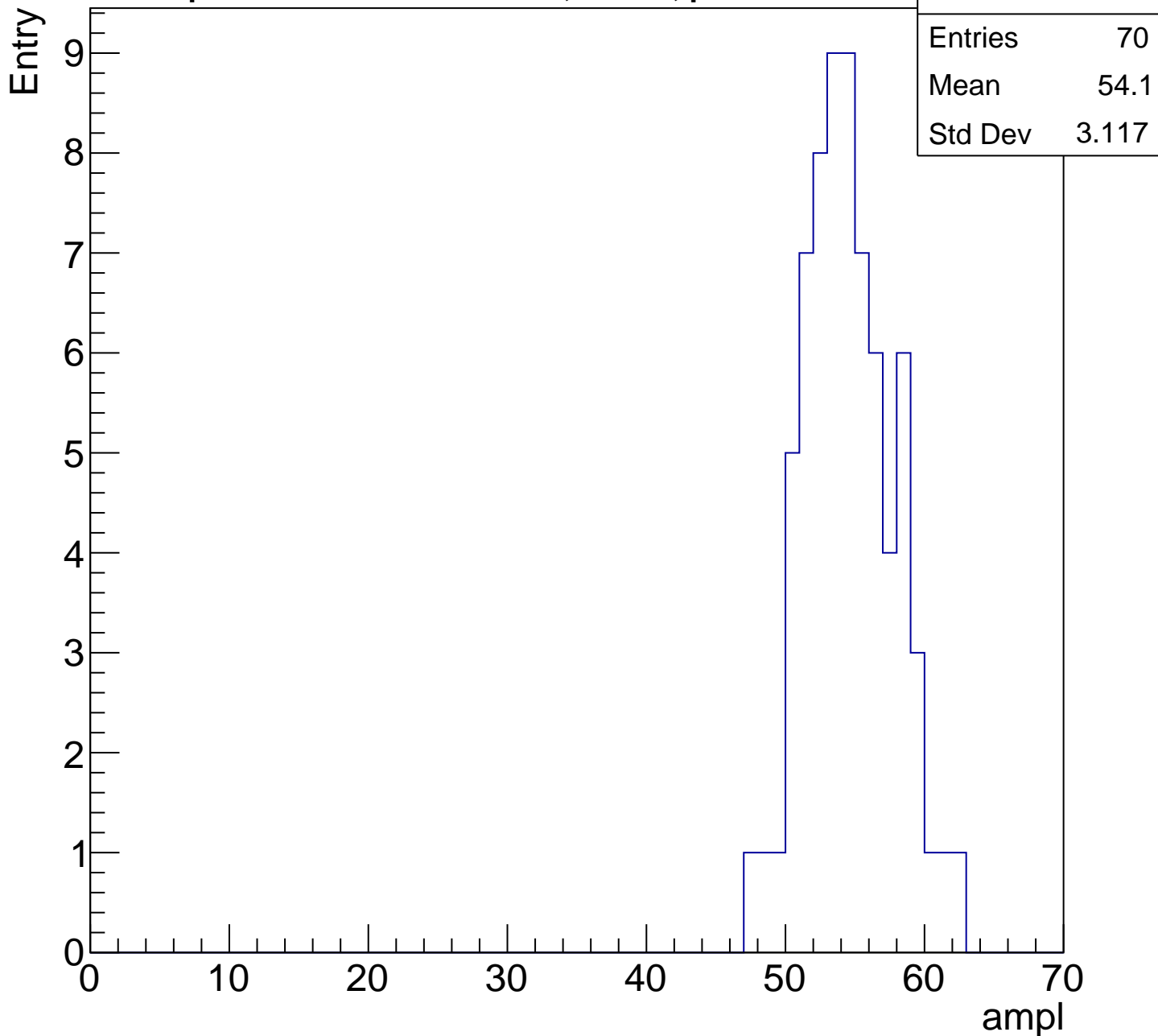
Entry

Entries	53
Mean	47.87
Std Dev	3.192



# B1L003S, U3-ch82, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2



# B1L003S, U3-ch82, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

7

6

5

4

3

2

1

0

Entries	41
Mean	59.34
Std Dev	2.364

ampl

10

20

30

40

50

60

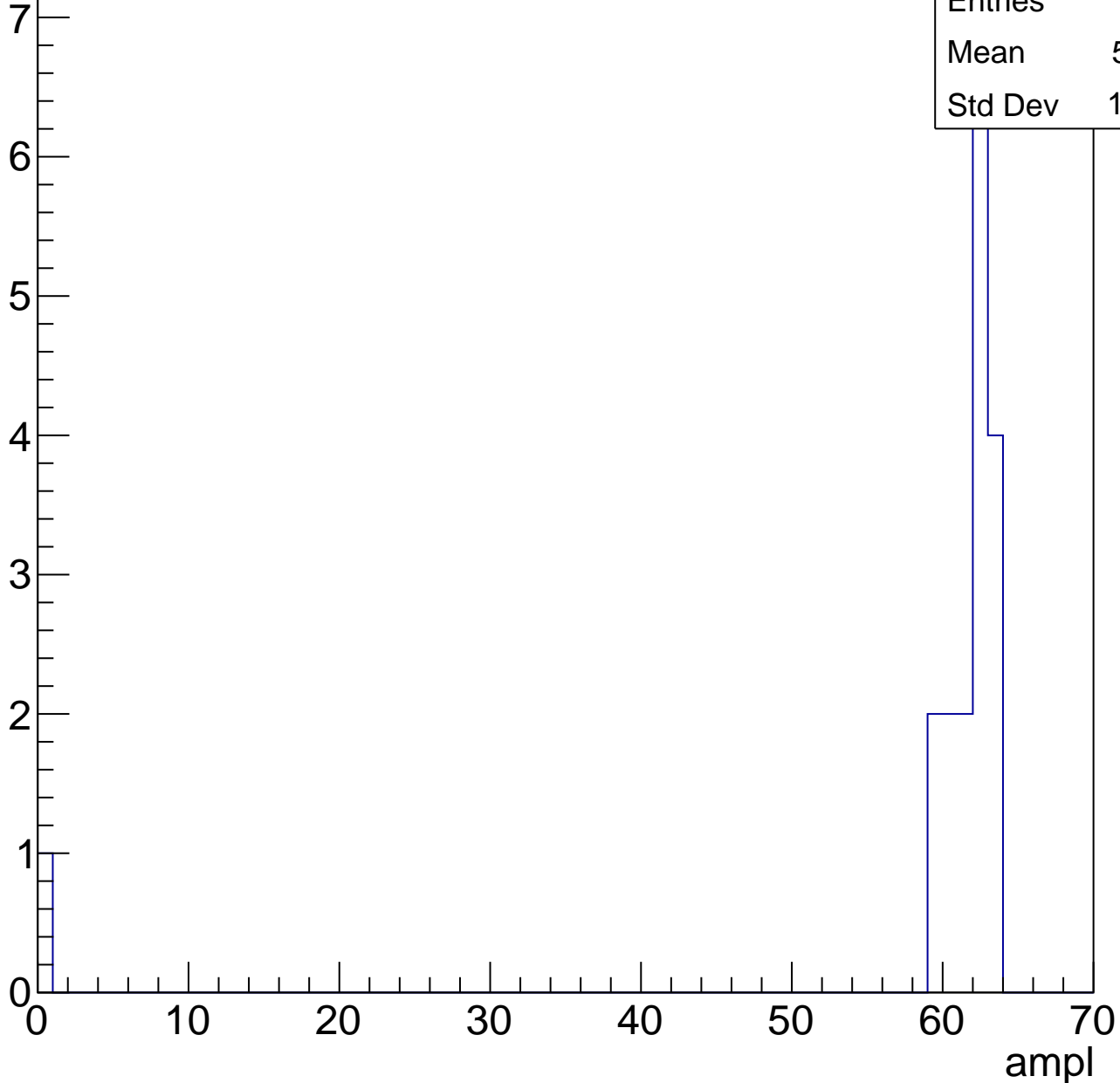
70

# B1L003S, U3-ch82, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	18
Mean	58.11
Std Dev	14.15

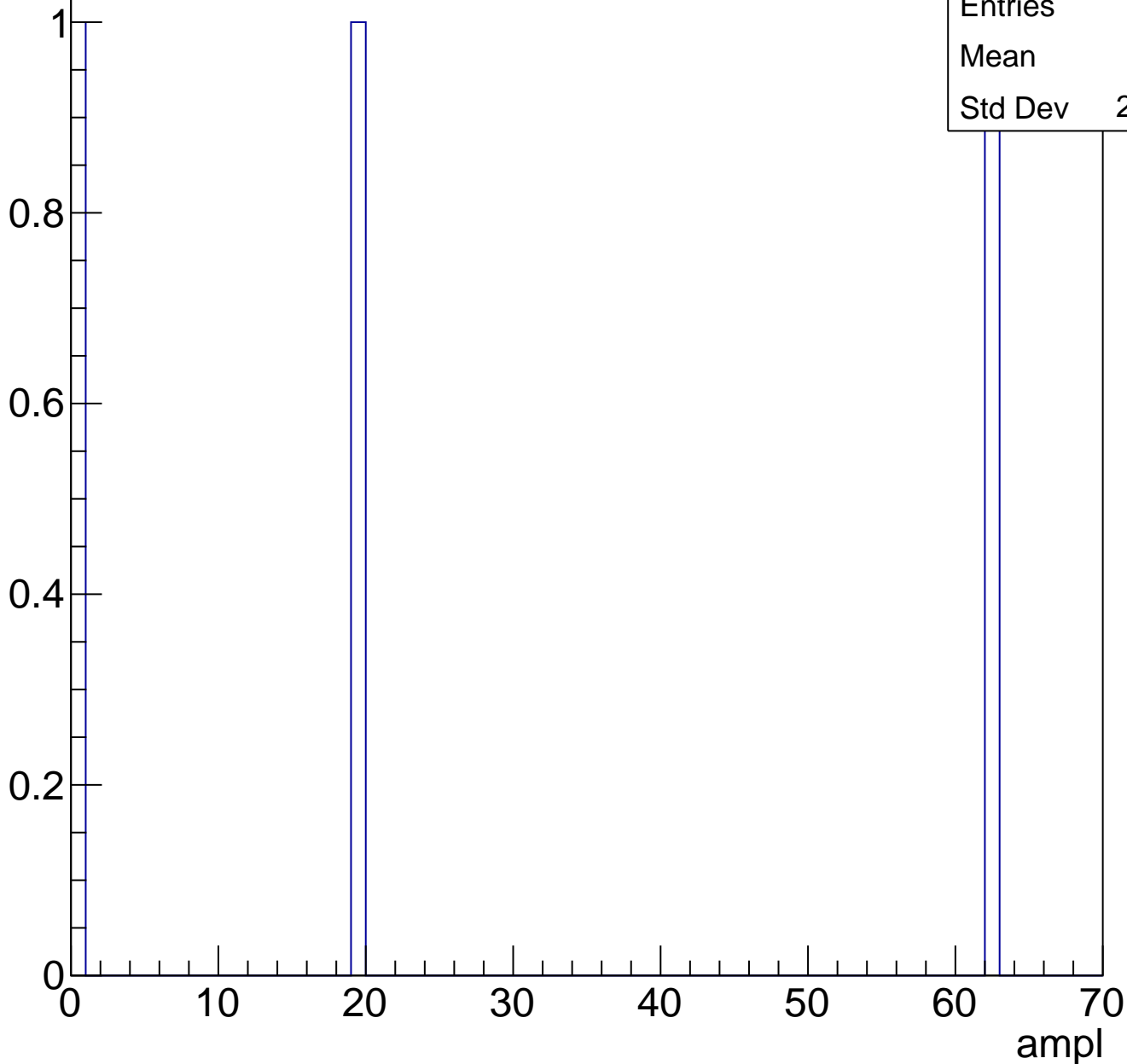




# B1L003S, U3-ch82, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U3-ch83, adc0

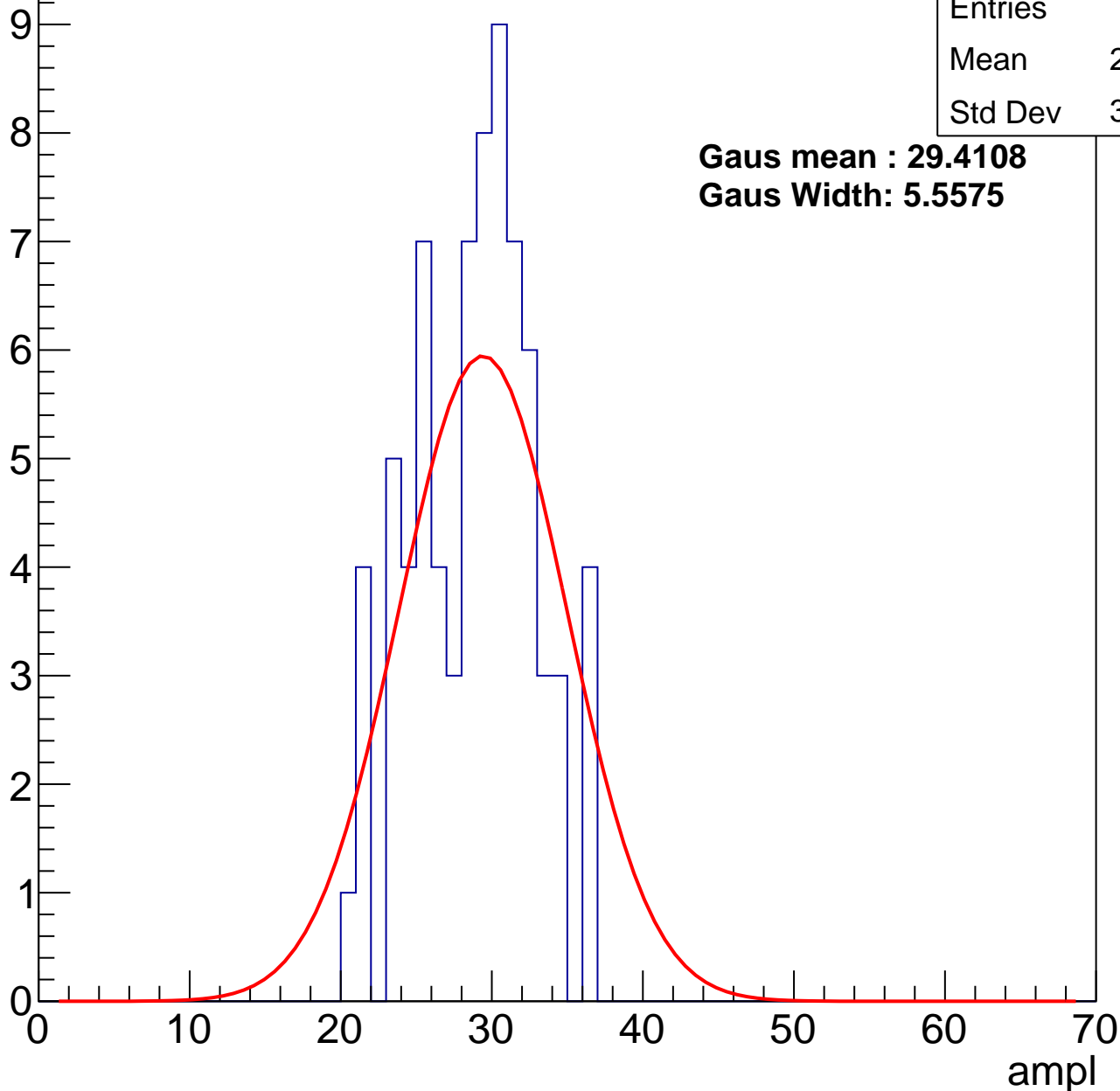
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	75
Mean	28.36
Std Dev	3.938

**Gaus mean : 29.4108**

**Gaus Width: 5.5575**



# B1L003S, U3-ch83, adc1

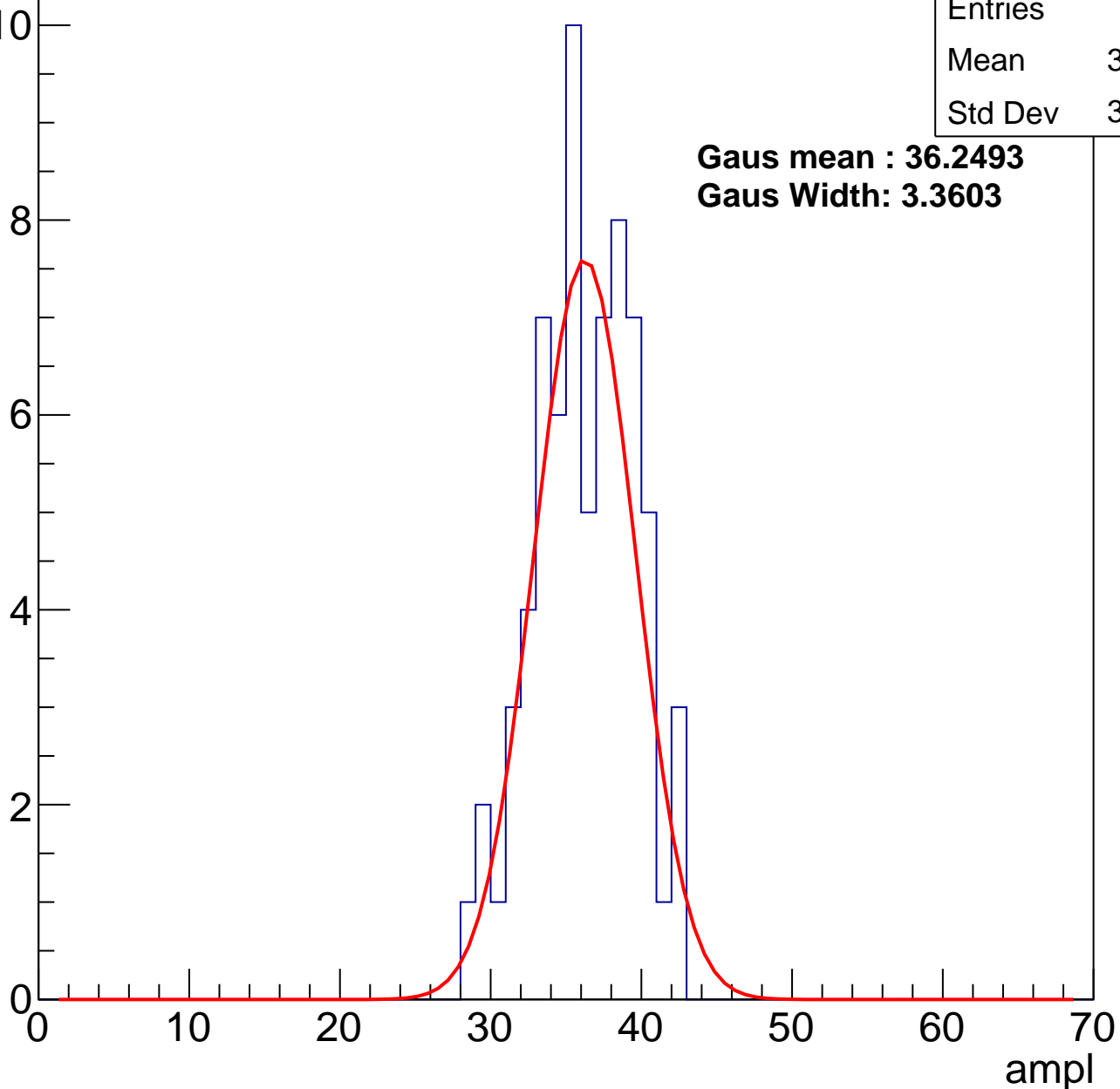
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	35.79
Std Dev	3.264

**Gaus mean : 36.2493**

**Gaus Width: 3.3603**



# B1L003S, U3-ch83, adc2

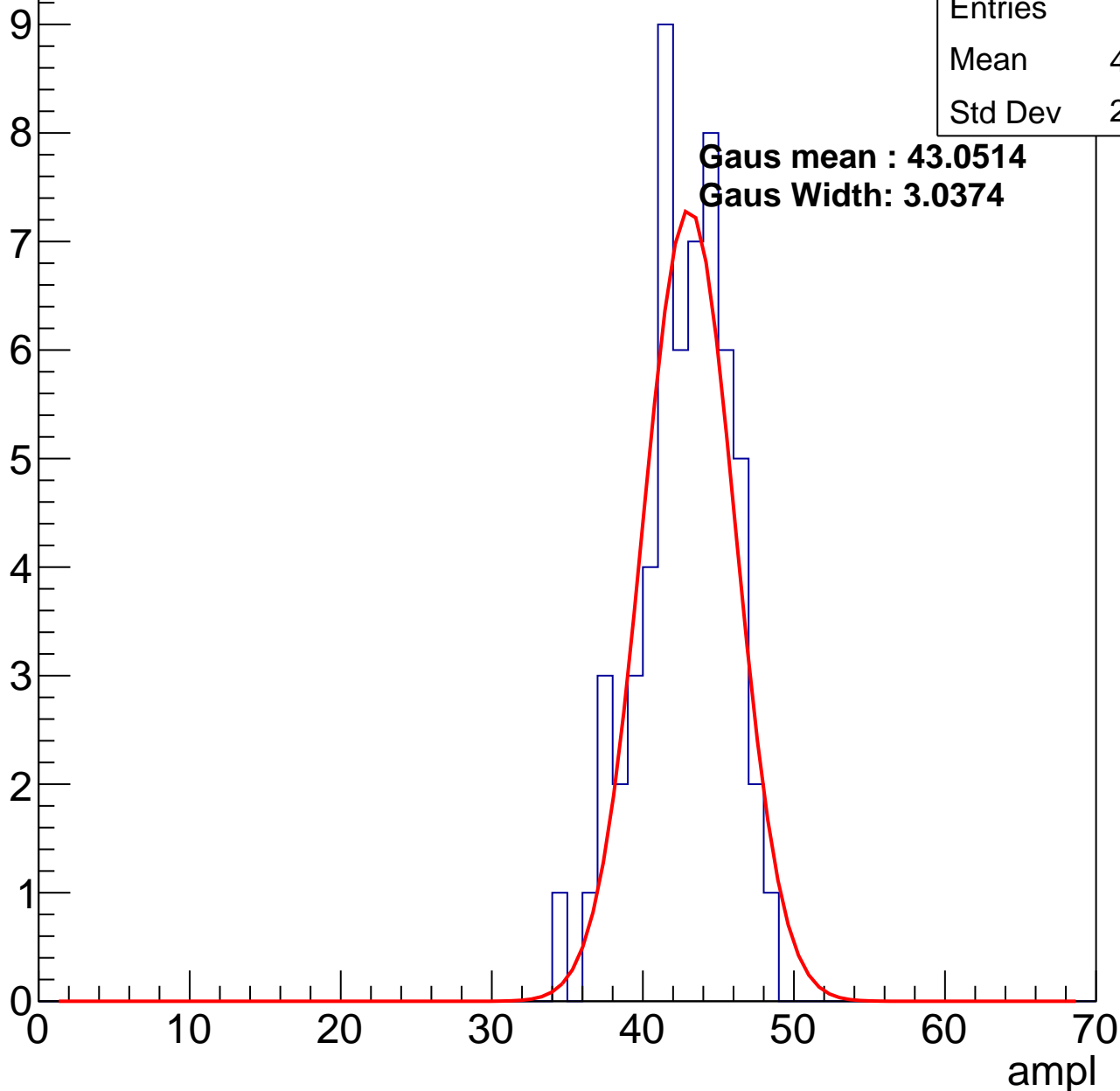
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	42.24
Std Dev	2.979

**Gaus mean : 43.0514**

**Gaus Width: 3.0374**

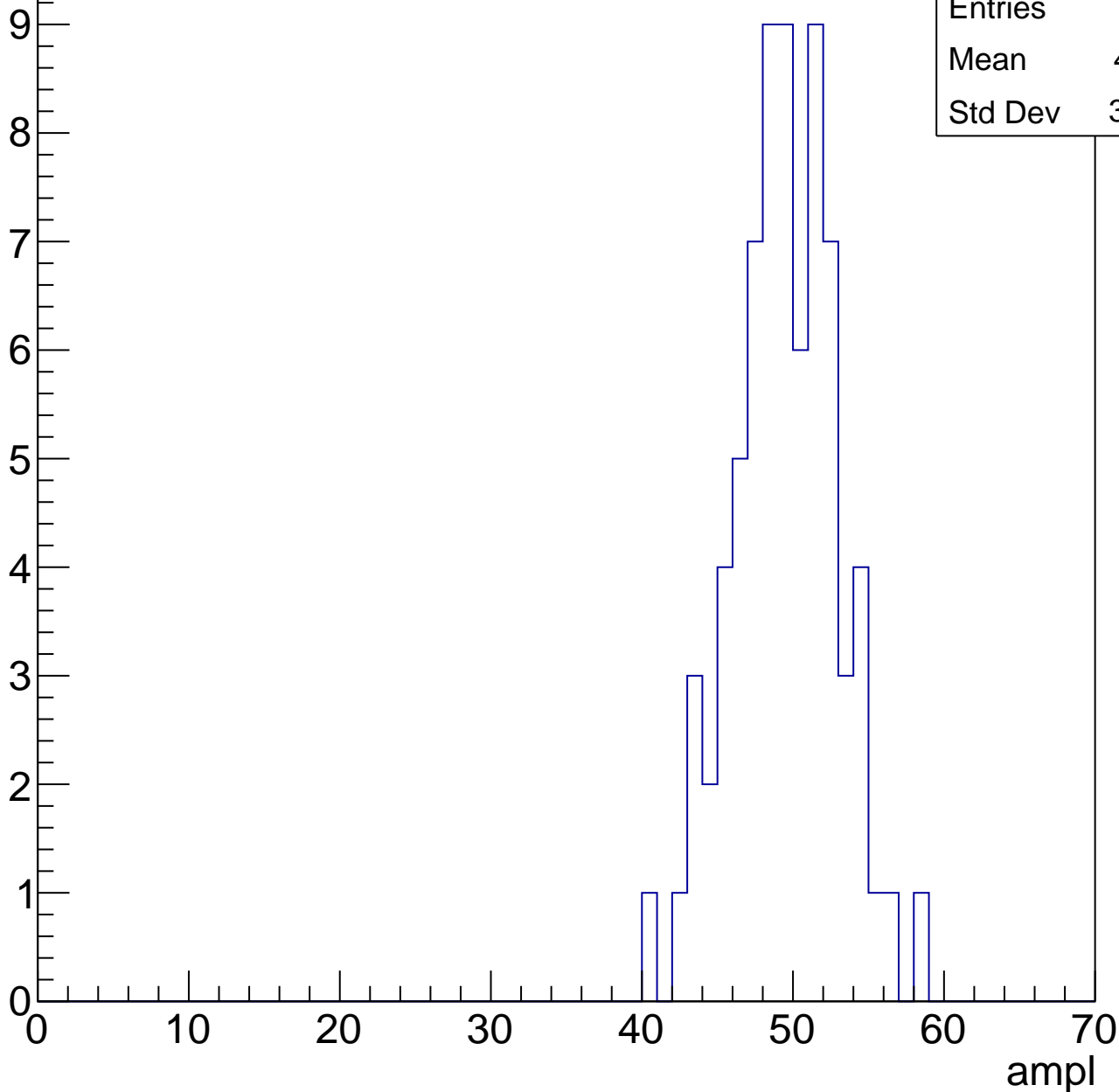


# B1L003S, U3-ch83, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	73
Mean	49.01
Std Dev	3.418

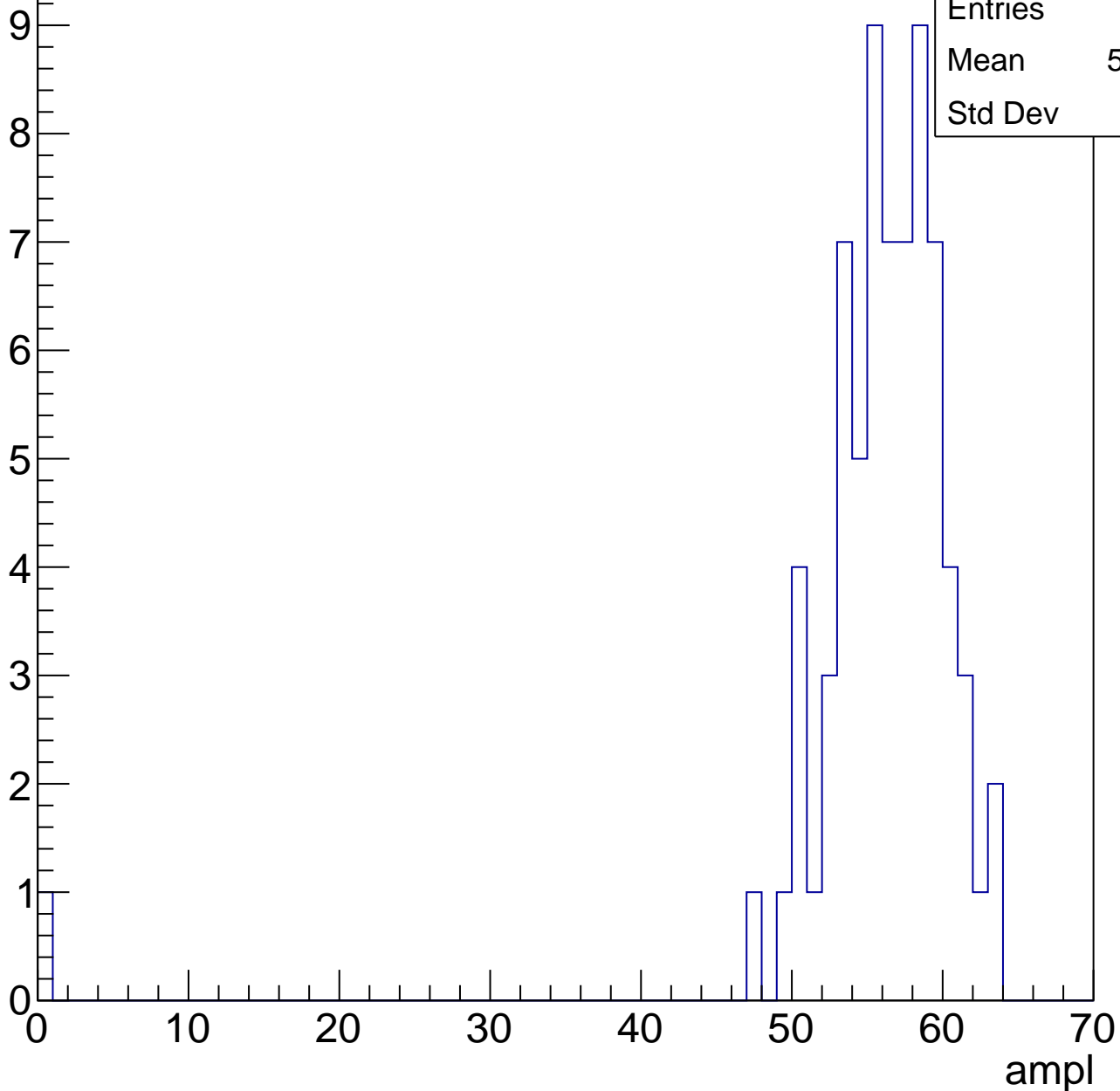


# B1L003S, U3-ch83, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	72
Mean	55.22
Std Dev	7.37

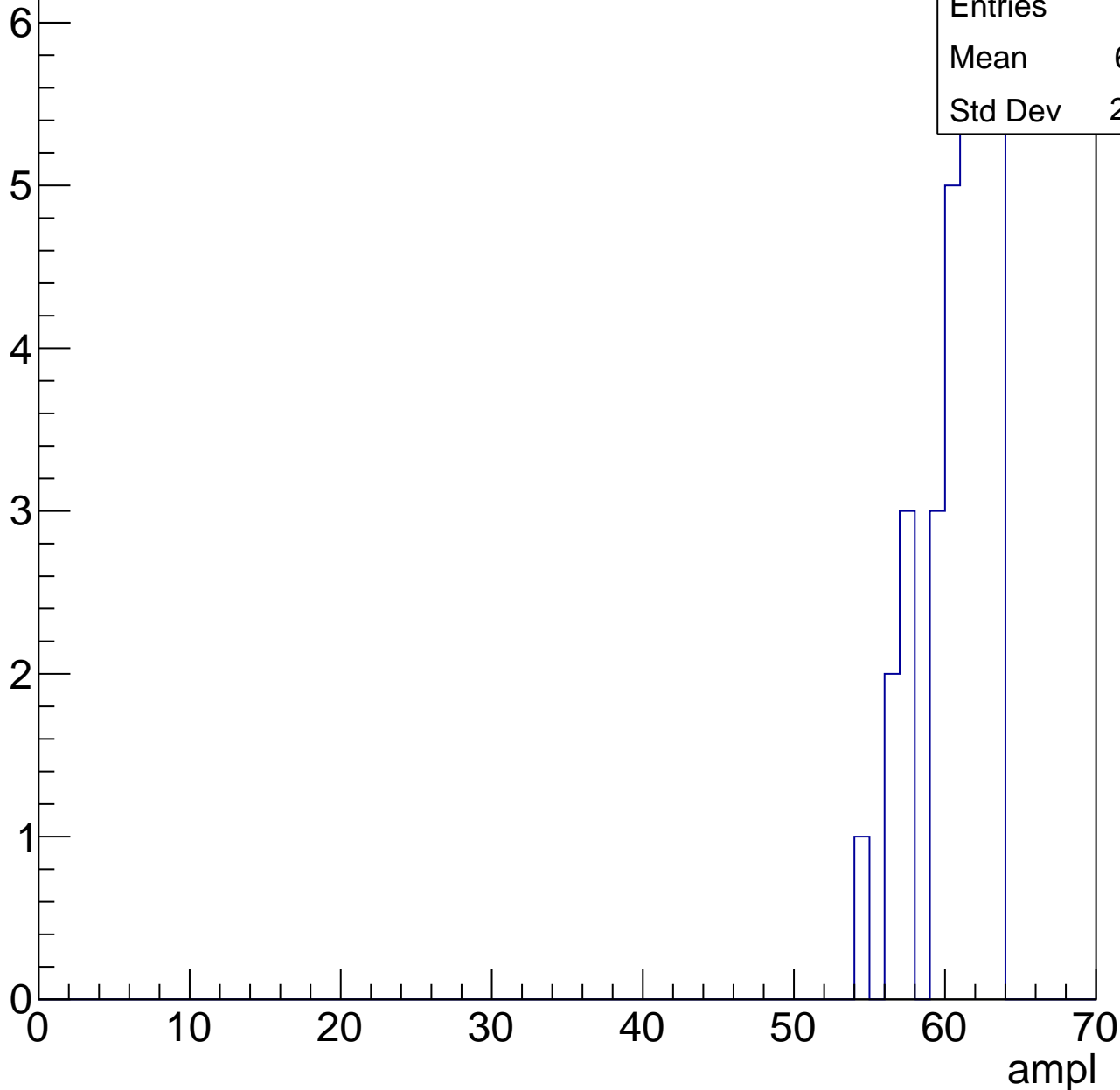


# B1L003S, U3-ch83, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

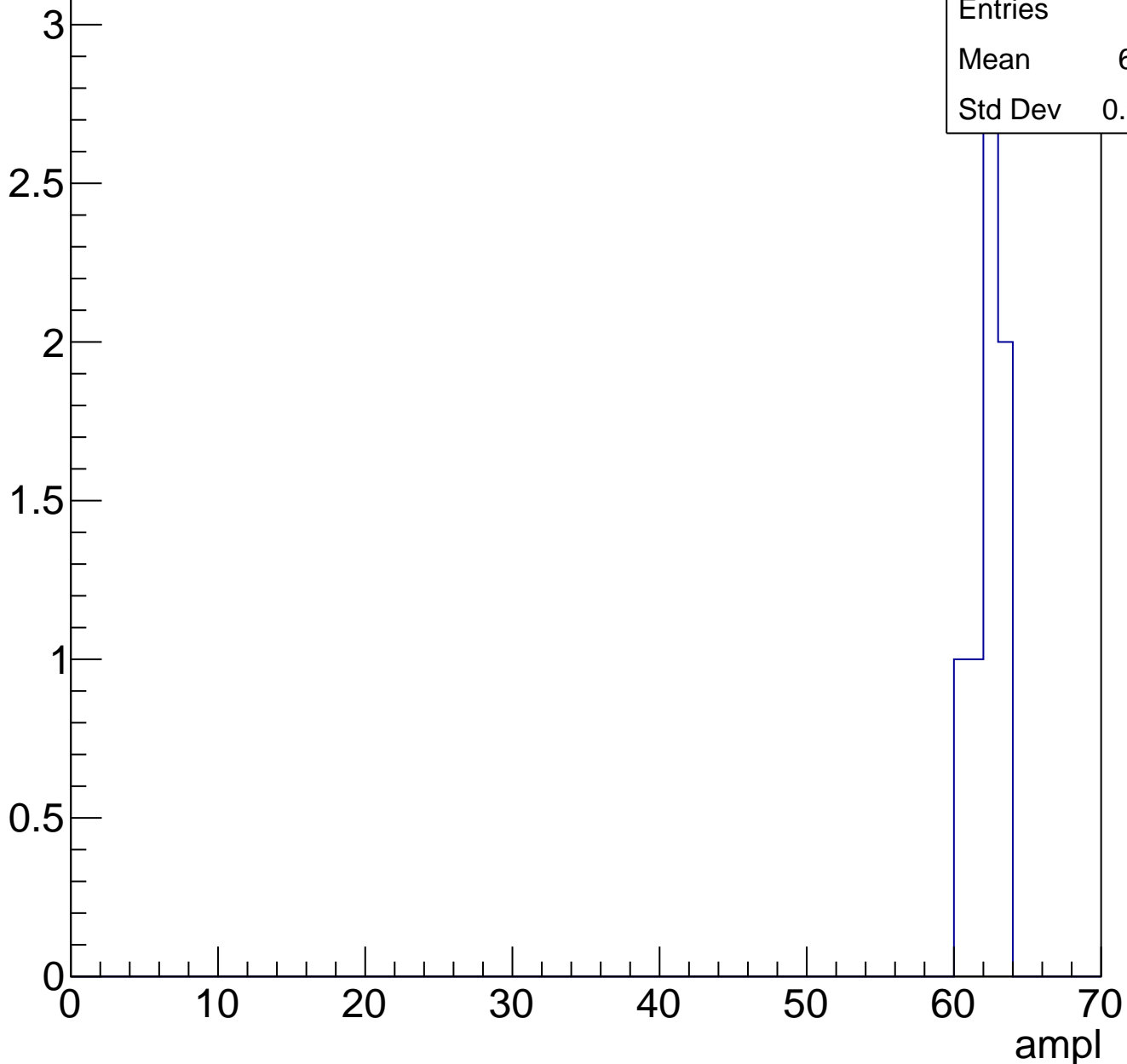
Entries	32
Mean	60.31
Std Dev	2.364



# B1L003S, U3-ch83, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch83, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U3-ch84, adc0

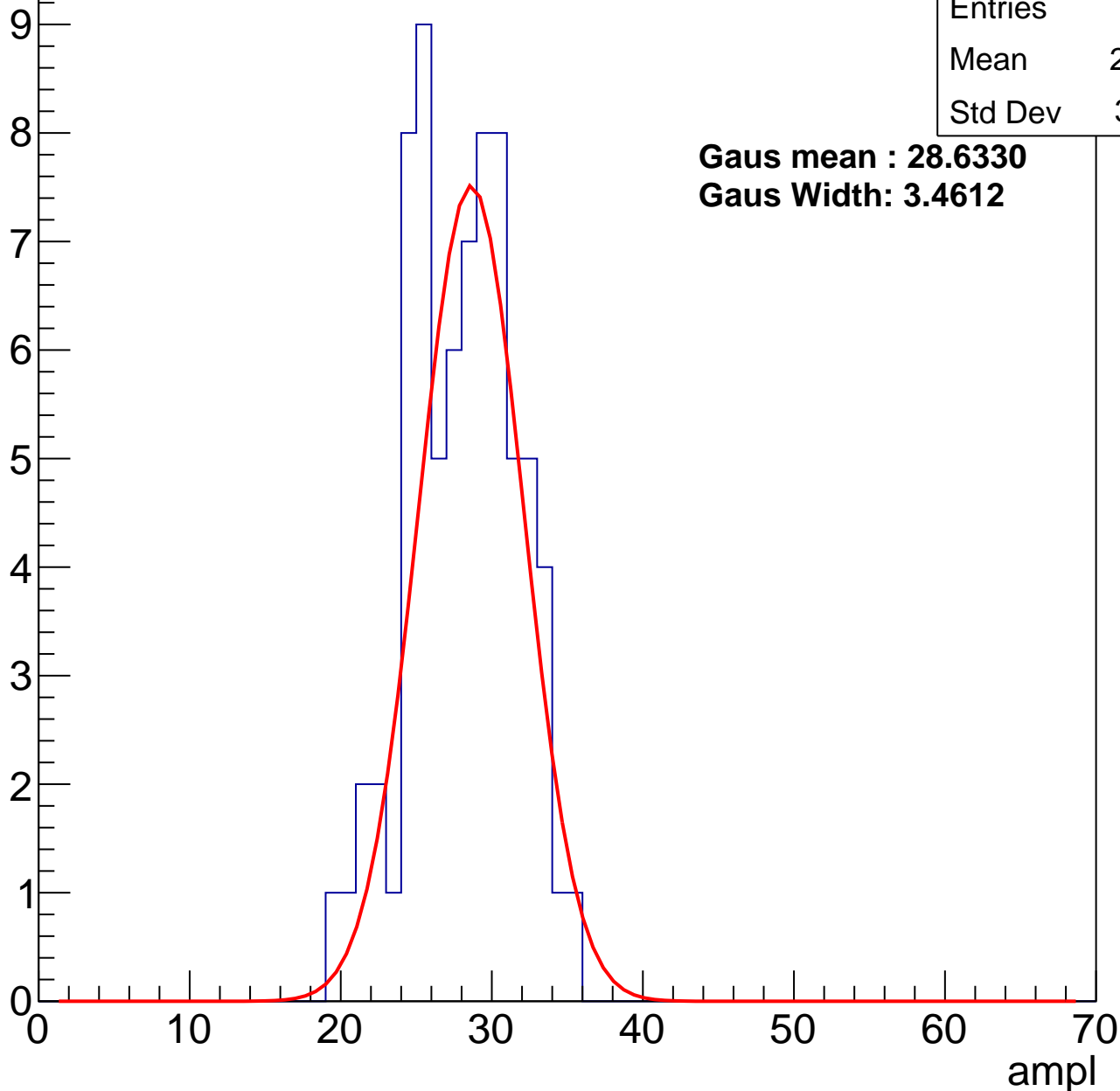
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	74
Mean	27.58
Std Dev	3.511

**Gaus mean : 28.6330**

**Gaus Width: 3.4612**



# B1L003S, U3-ch84, adc1

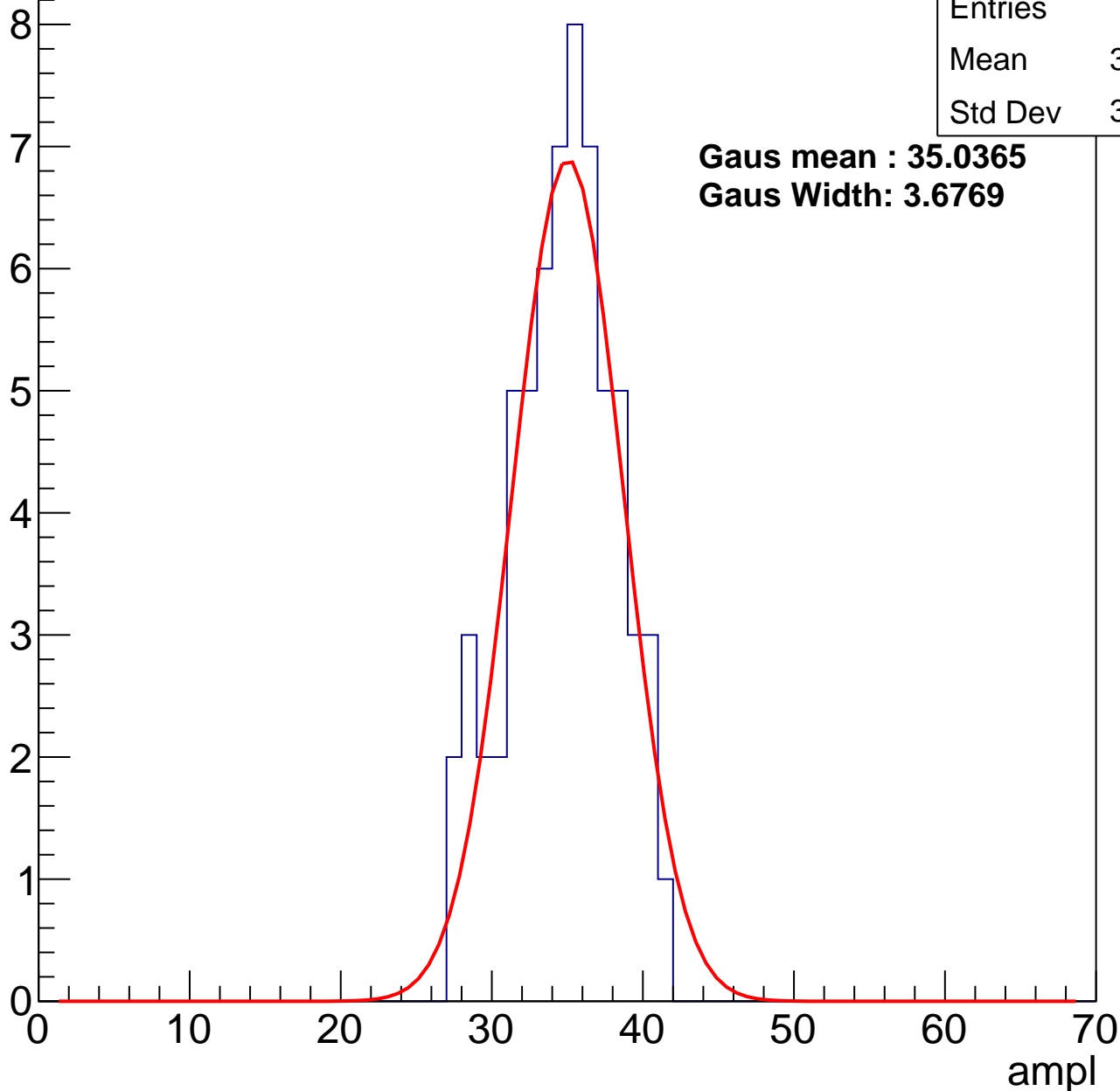
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	34.25
Std Dev	3.419

**Gaus mean : 35.0365**

**Gaus Width: 3.6769**



# B1L003S, U3-ch84, adc2

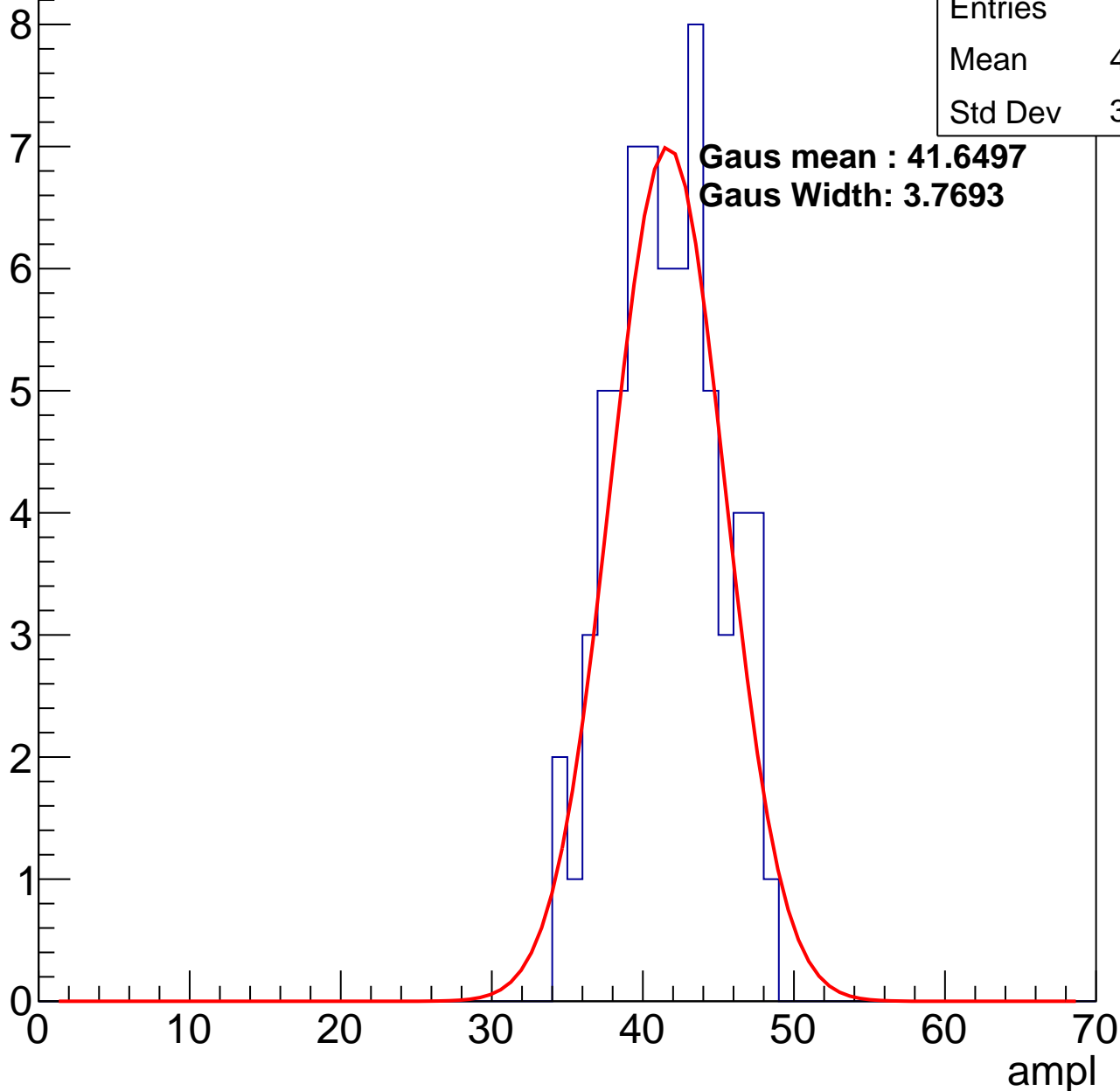
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	41.13
Std Dev	3.438

**Gaus mean : 41.6497**

**Gaus Width: 3.7693**

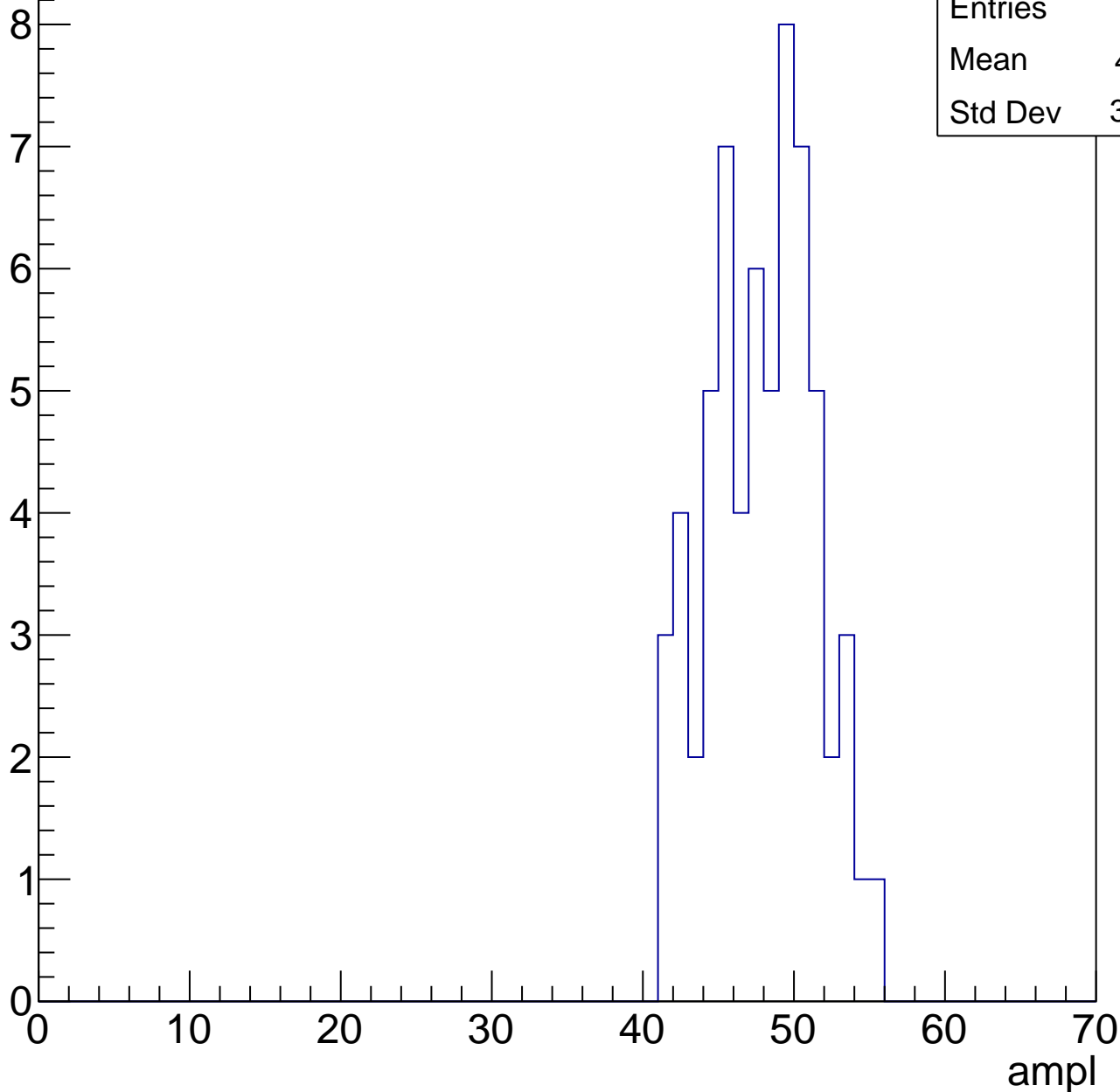


# B1L003S, U3-ch84, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	47.41
Std Dev	3.467

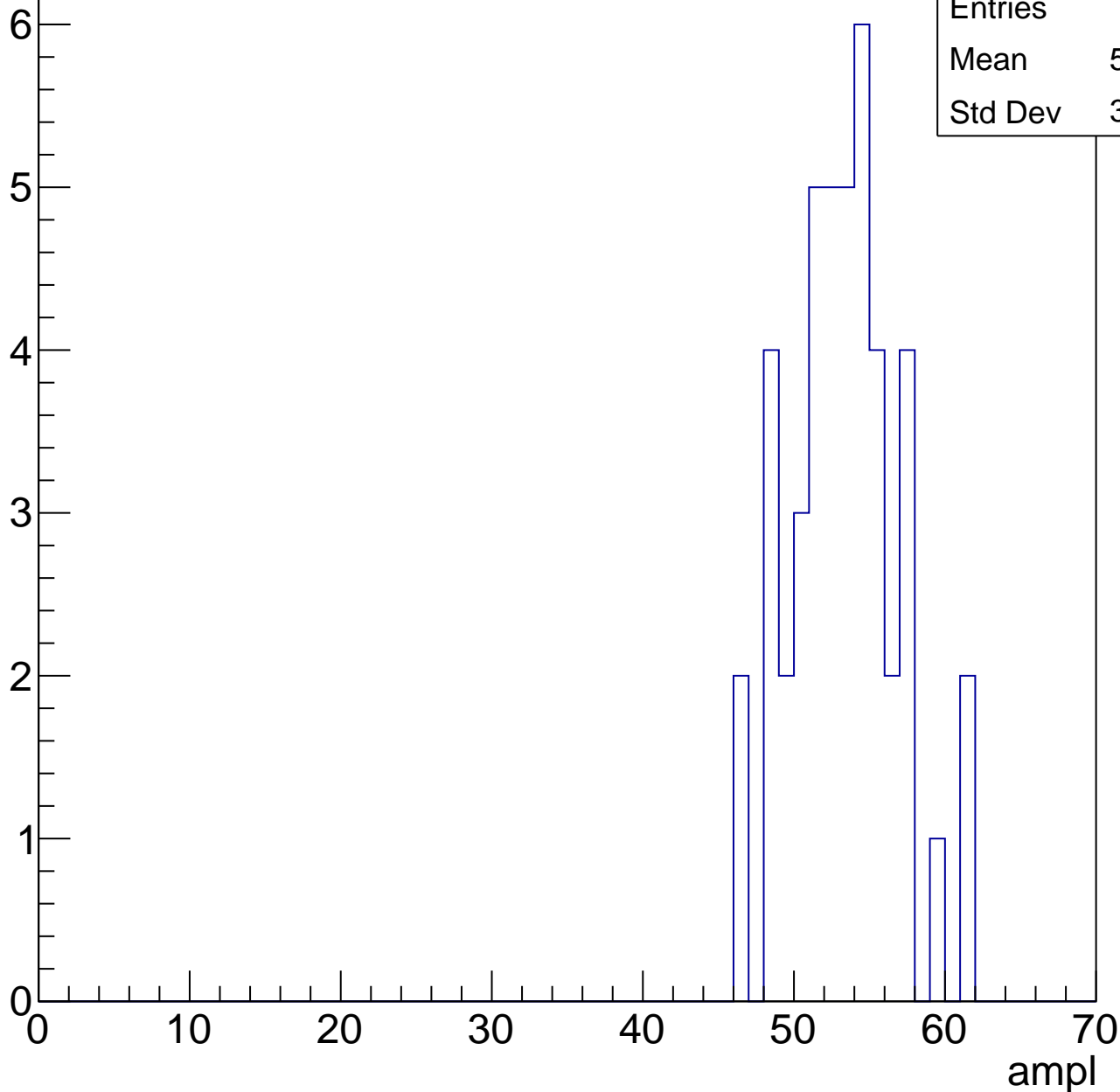


# B1L003S, U3-ch84, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

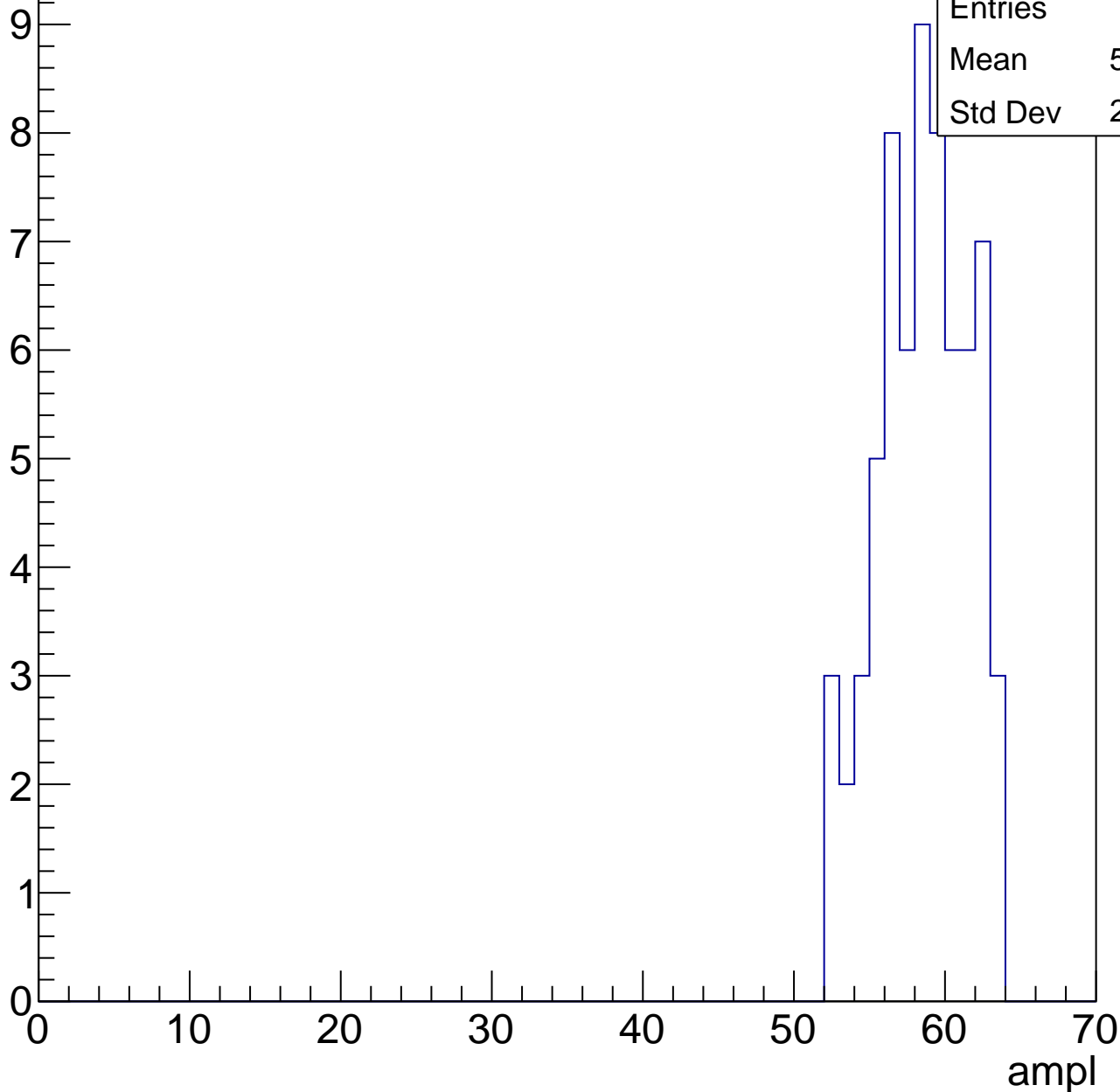
Entries	45
Mean	52.82
Std Dev	3.492



# B1L003S, U3-ch84, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

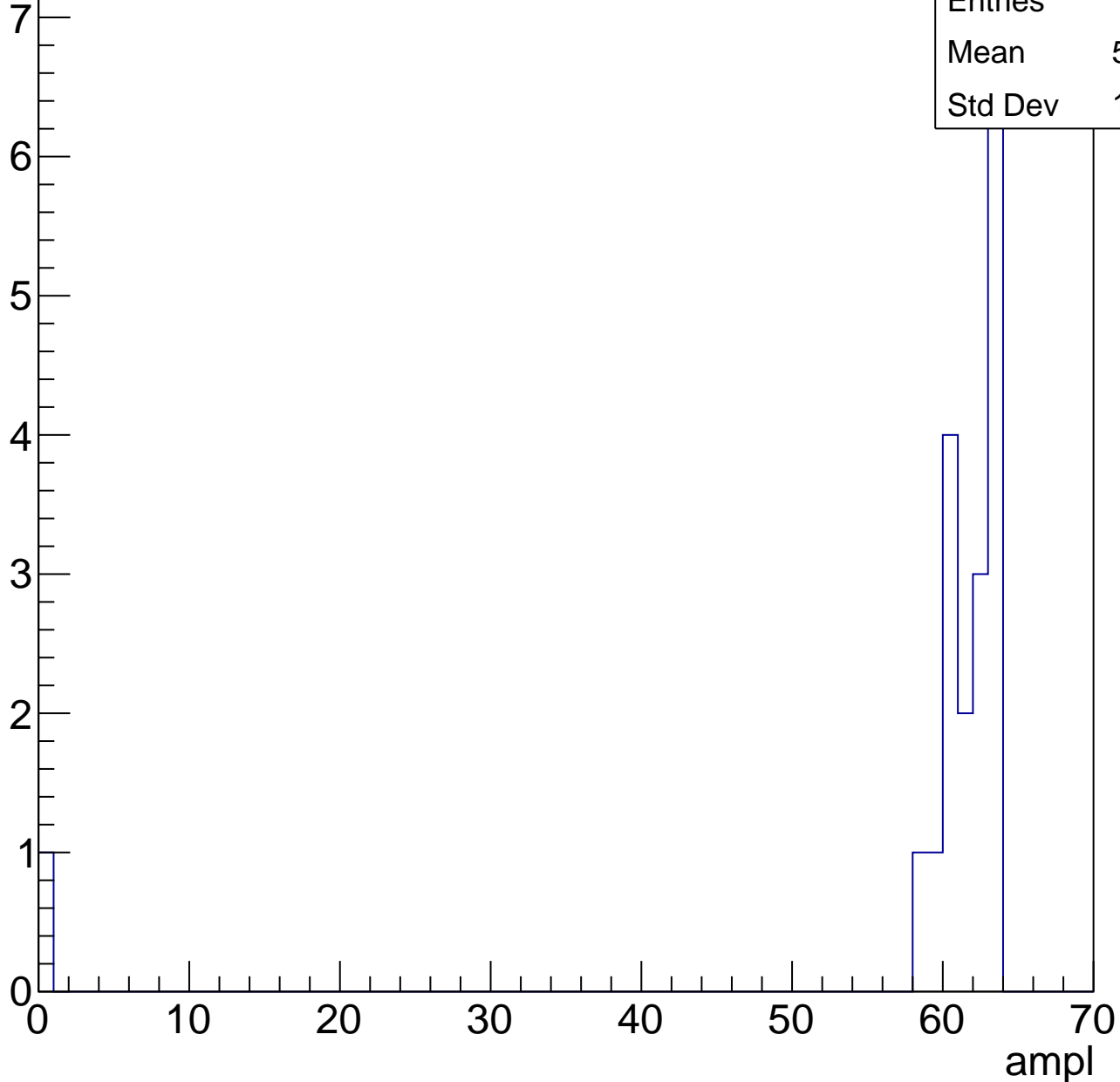


# B1L003S, U3-ch84, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	19
Mean	58.21
Std Dev	13.81





# B1L003S, U3-ch84, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U3-ch85, adc0

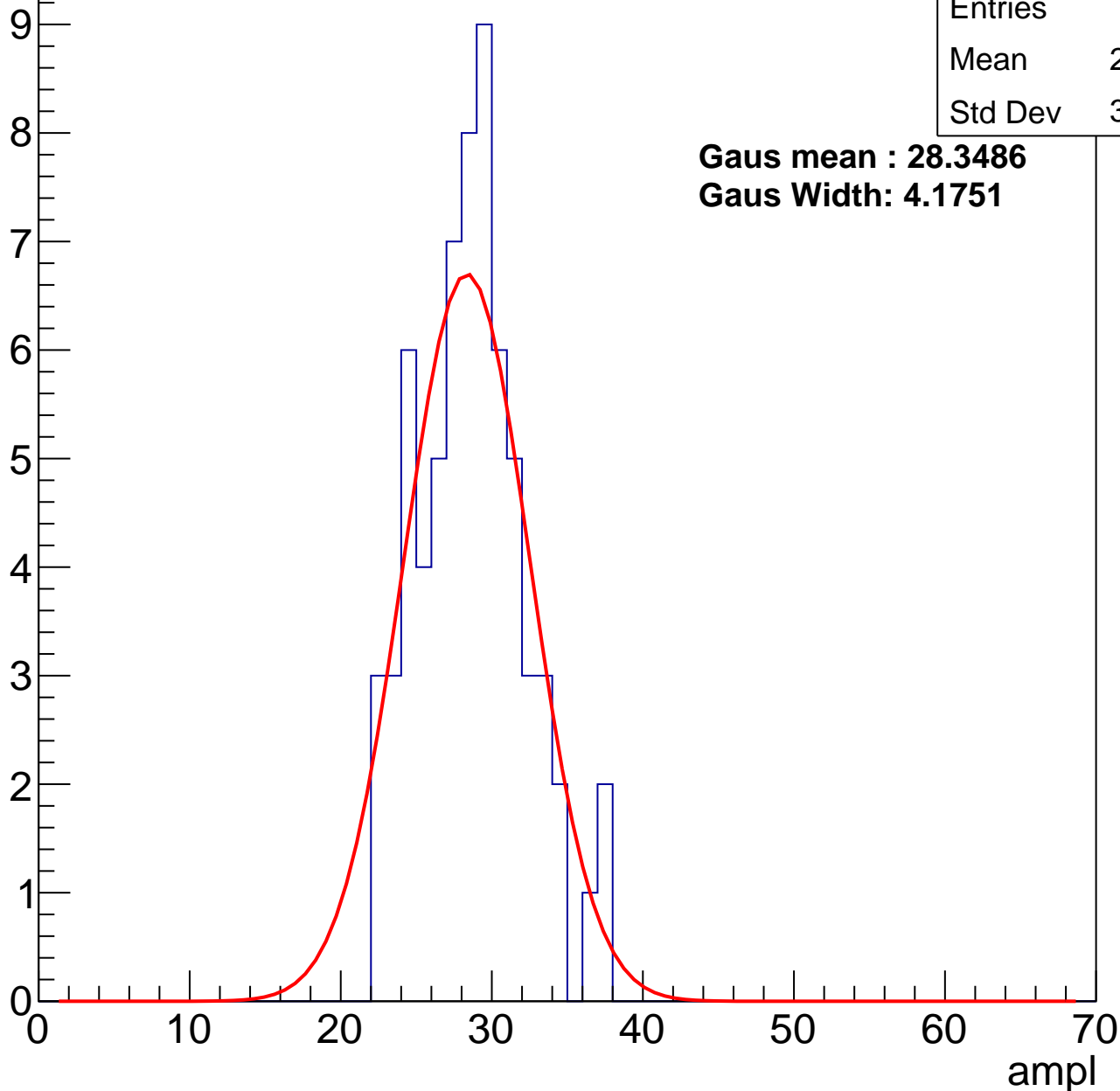
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	28.22
Std Dev	3.536

**Gaus mean : 28.3486**

**Gaus Width: 4.1751**



# B1L003S, U3-ch85, adc1

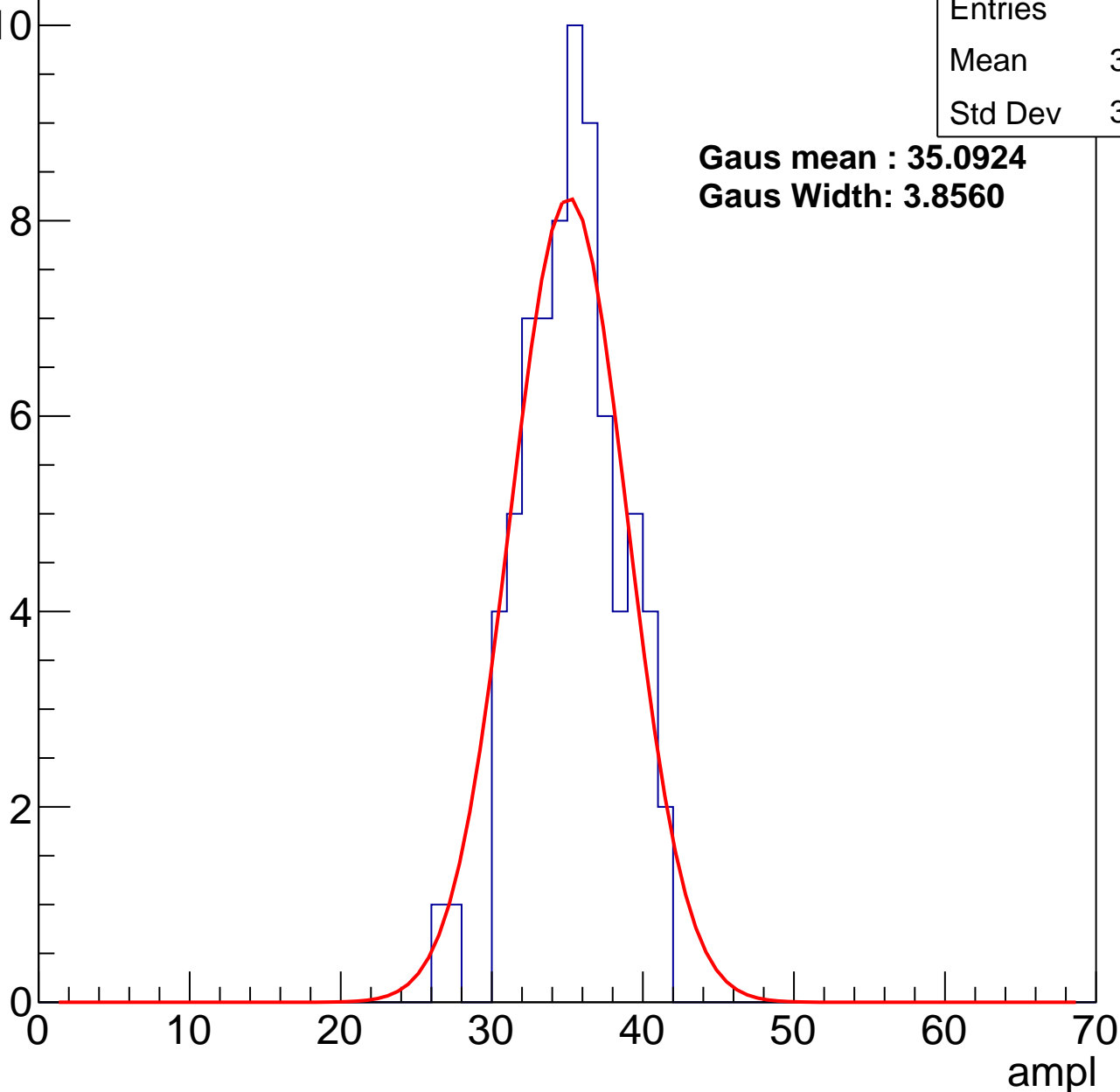
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	73
Mean	34.79
Std Dev	3.188

**Gaus mean : 35.0924**

**Gaus Width: 3.8560**

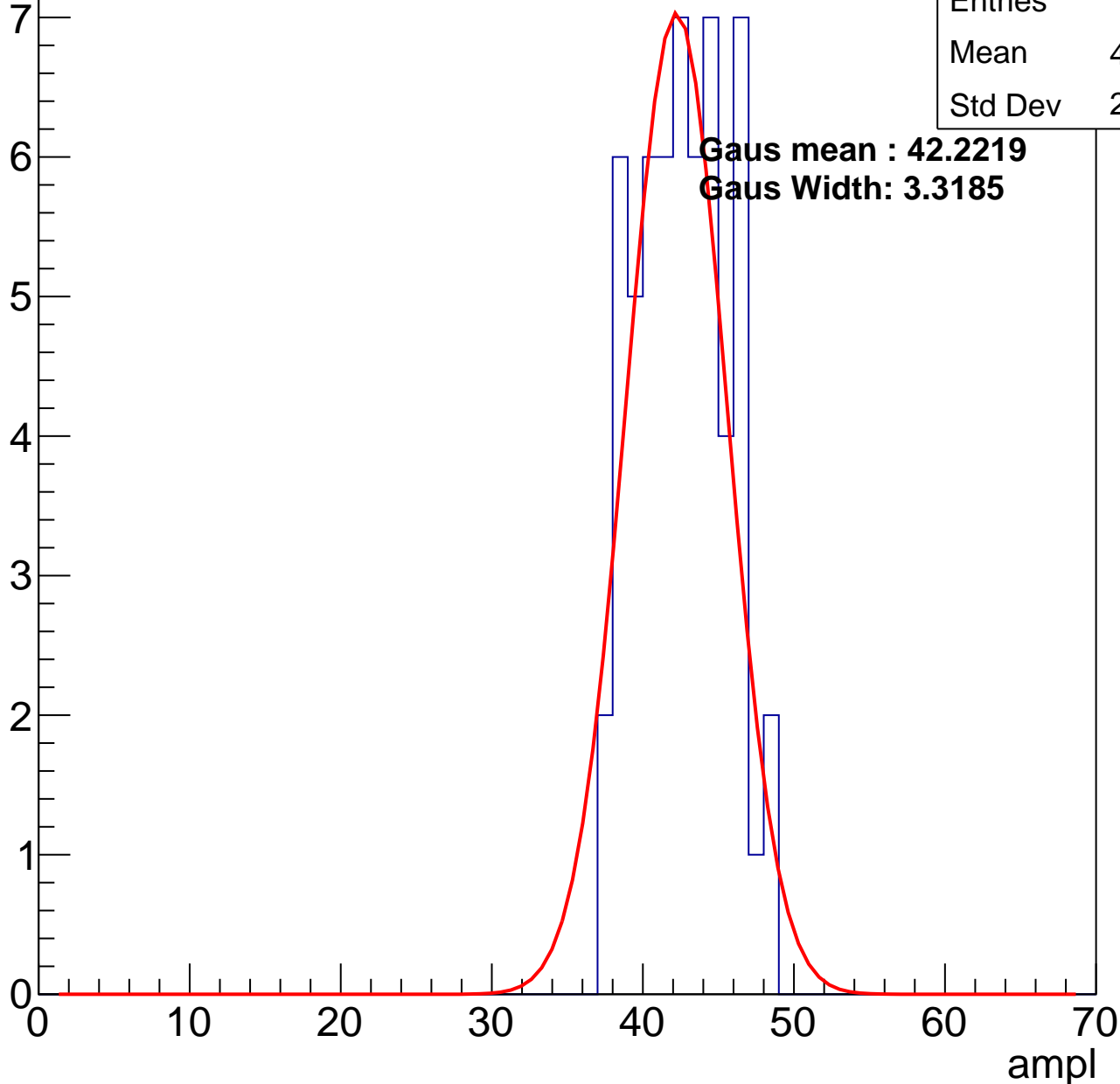


# B1L003S, U3-ch85, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	42.17
Std Dev	2.906



# B1L003S, U3-ch85, adc3

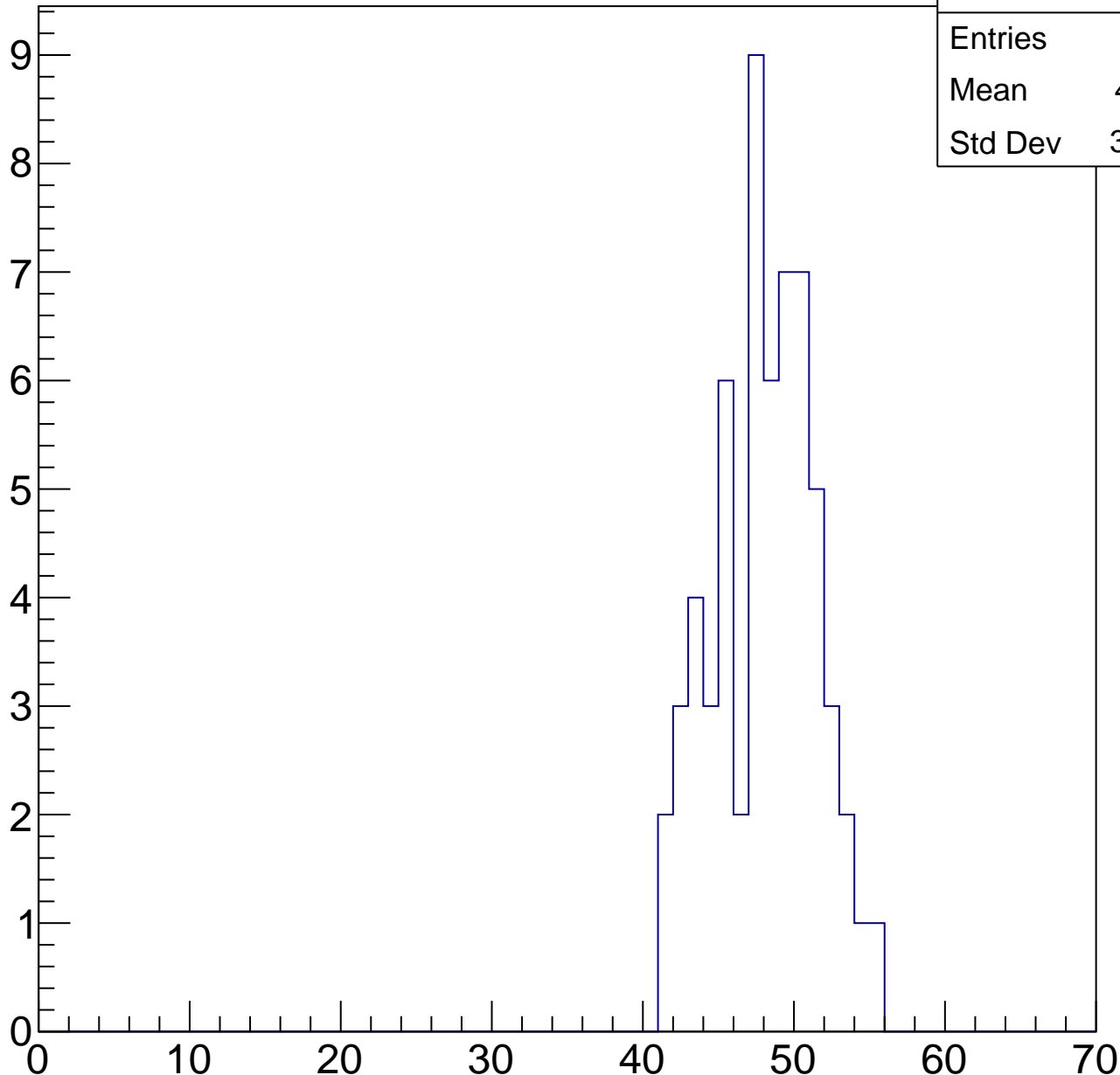
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	61
Mean	47.61
Std Dev	3.335

ampl

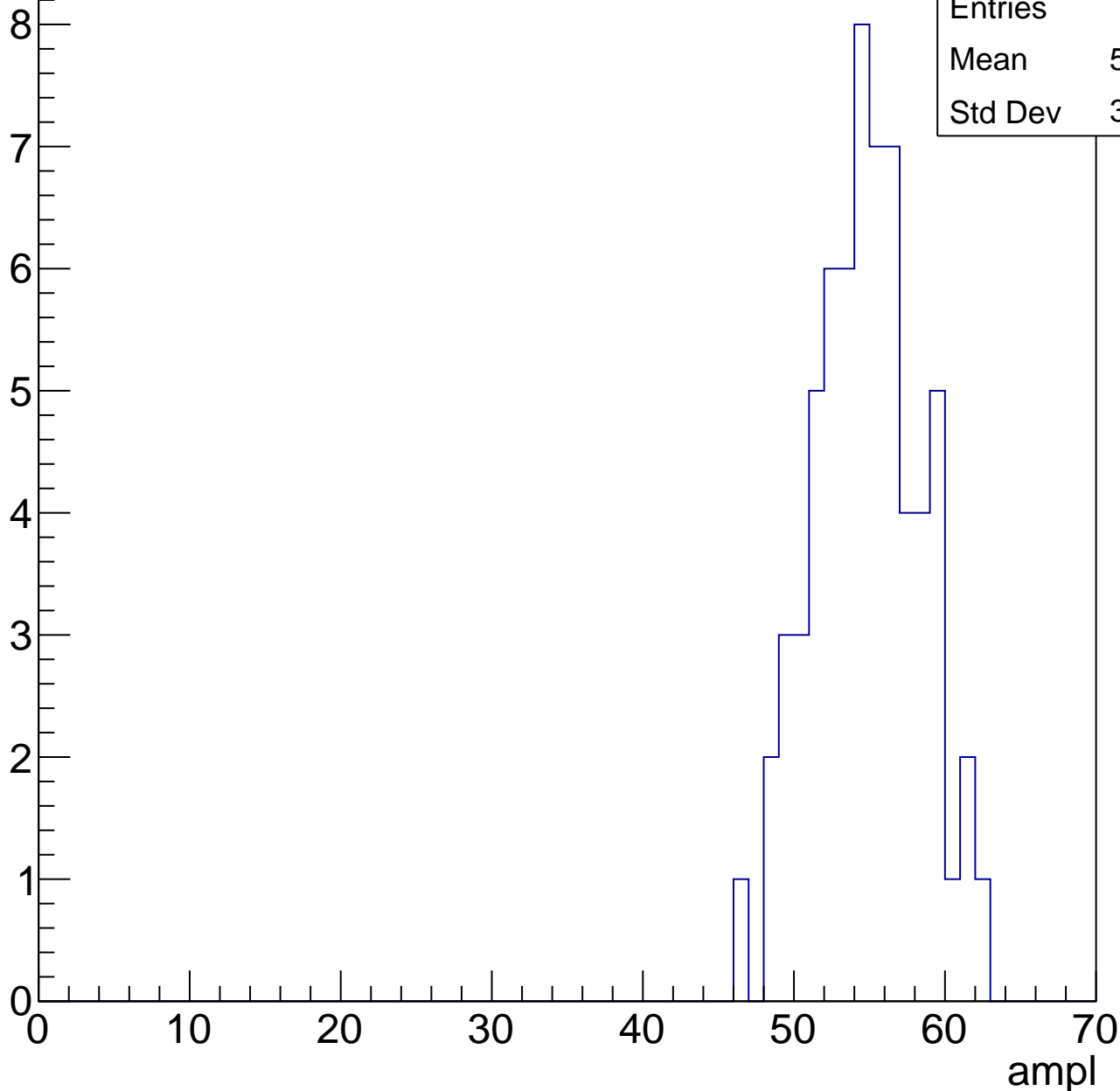


# B1L003S, U3-ch85, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

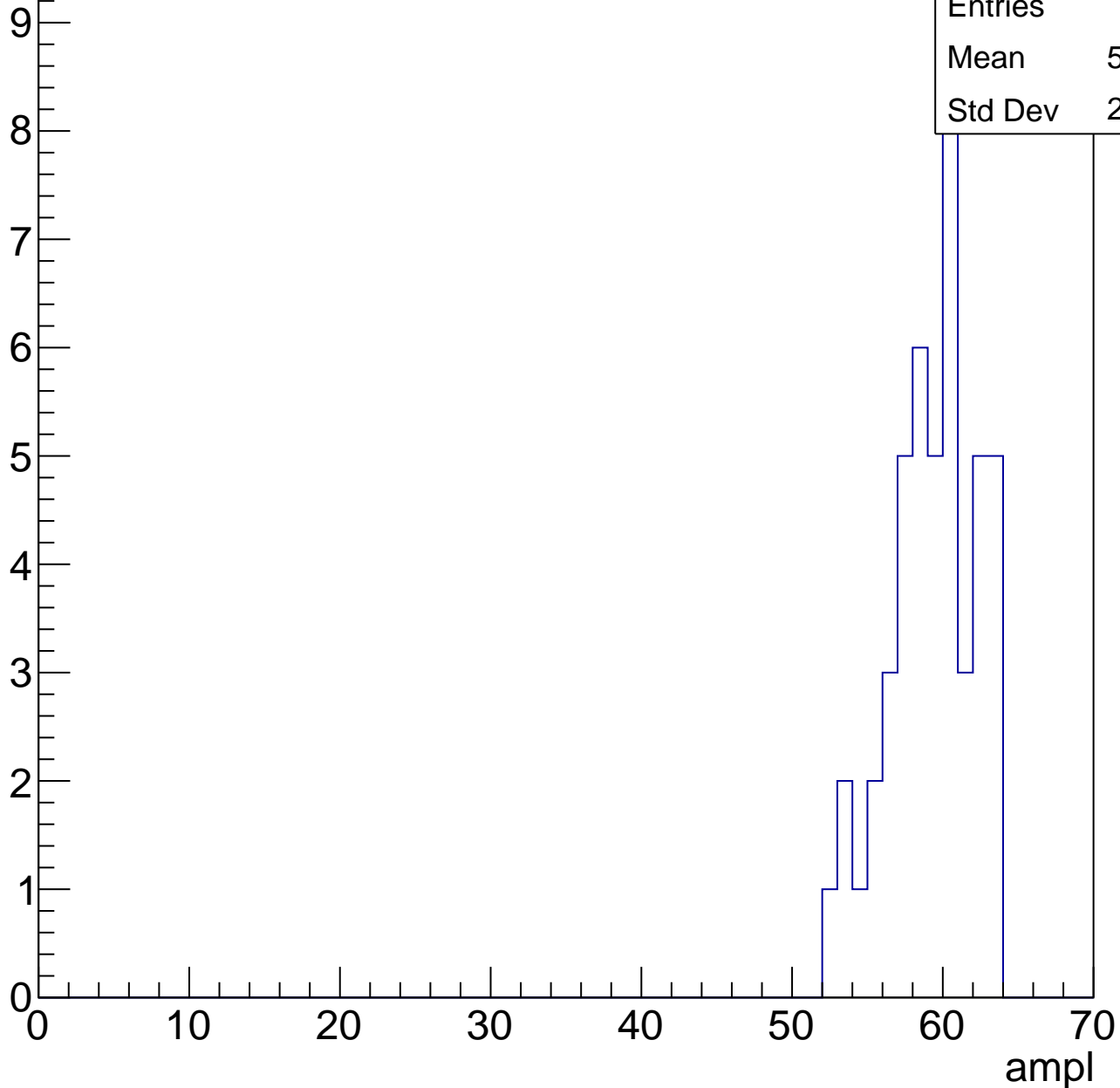
Entries	65
Mean	54.34
Std Dev	3.474



# B1L003S, U3-ch85, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

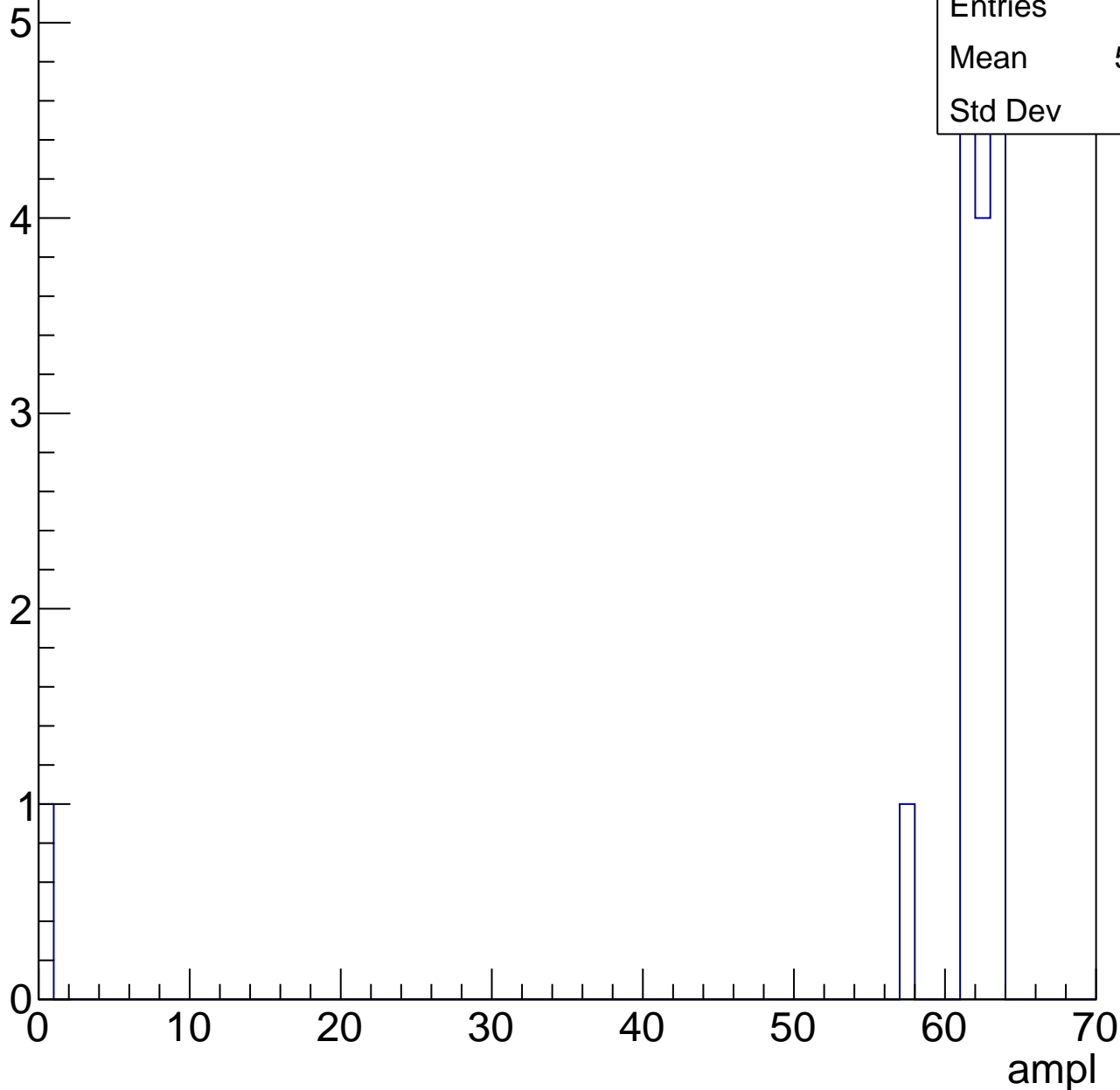


# B1L003S, U3-ch85, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	16
Mean	57.81
Std Dev	15





# B1L003S, U3-ch85, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U3-ch86, adc0

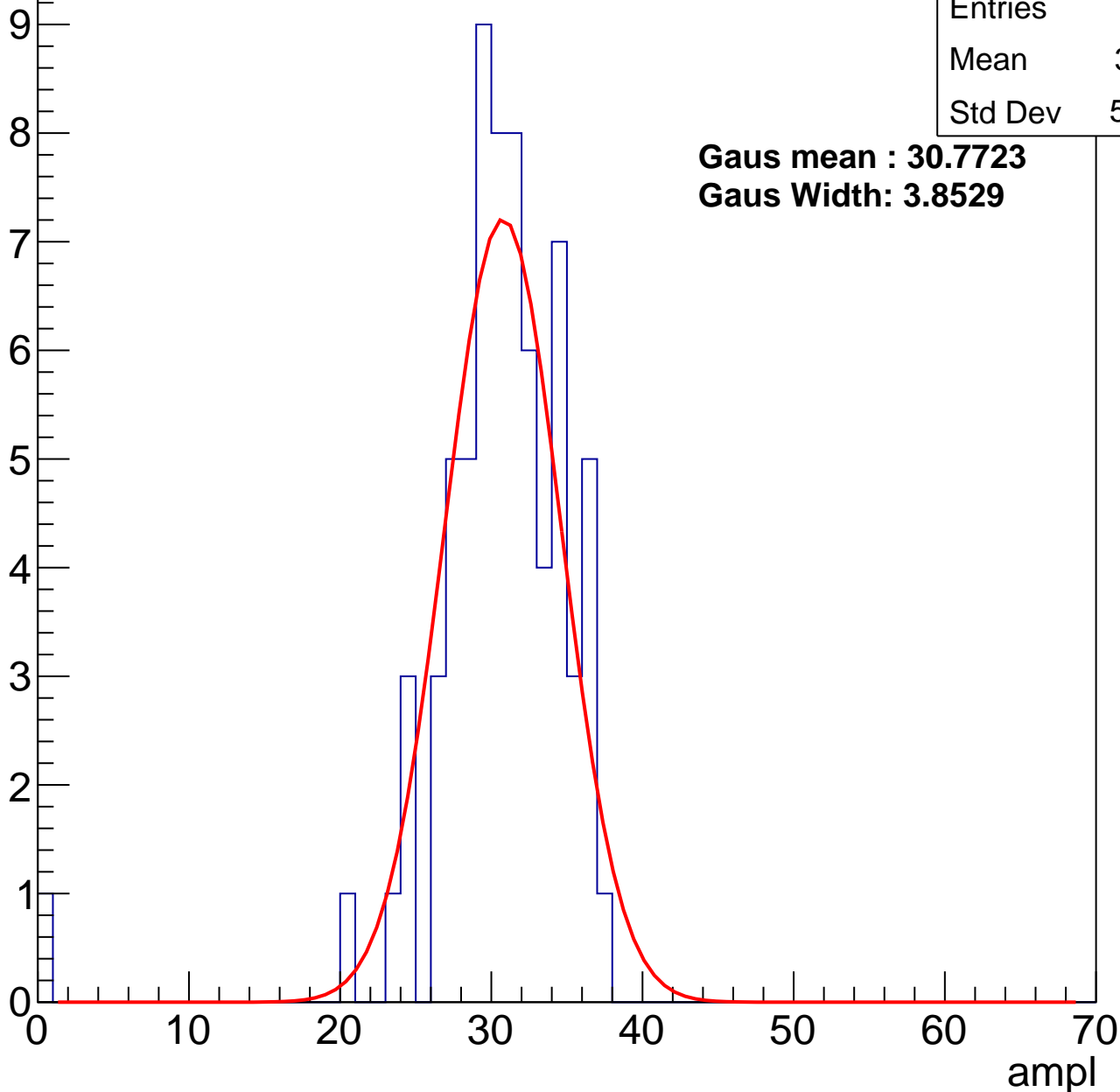
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	30.01
Std Dev	5.019

**Gaus mean : 30.7723**

**Gaus Width: 3.8529**



# B1L003S, U3-ch86, adc1

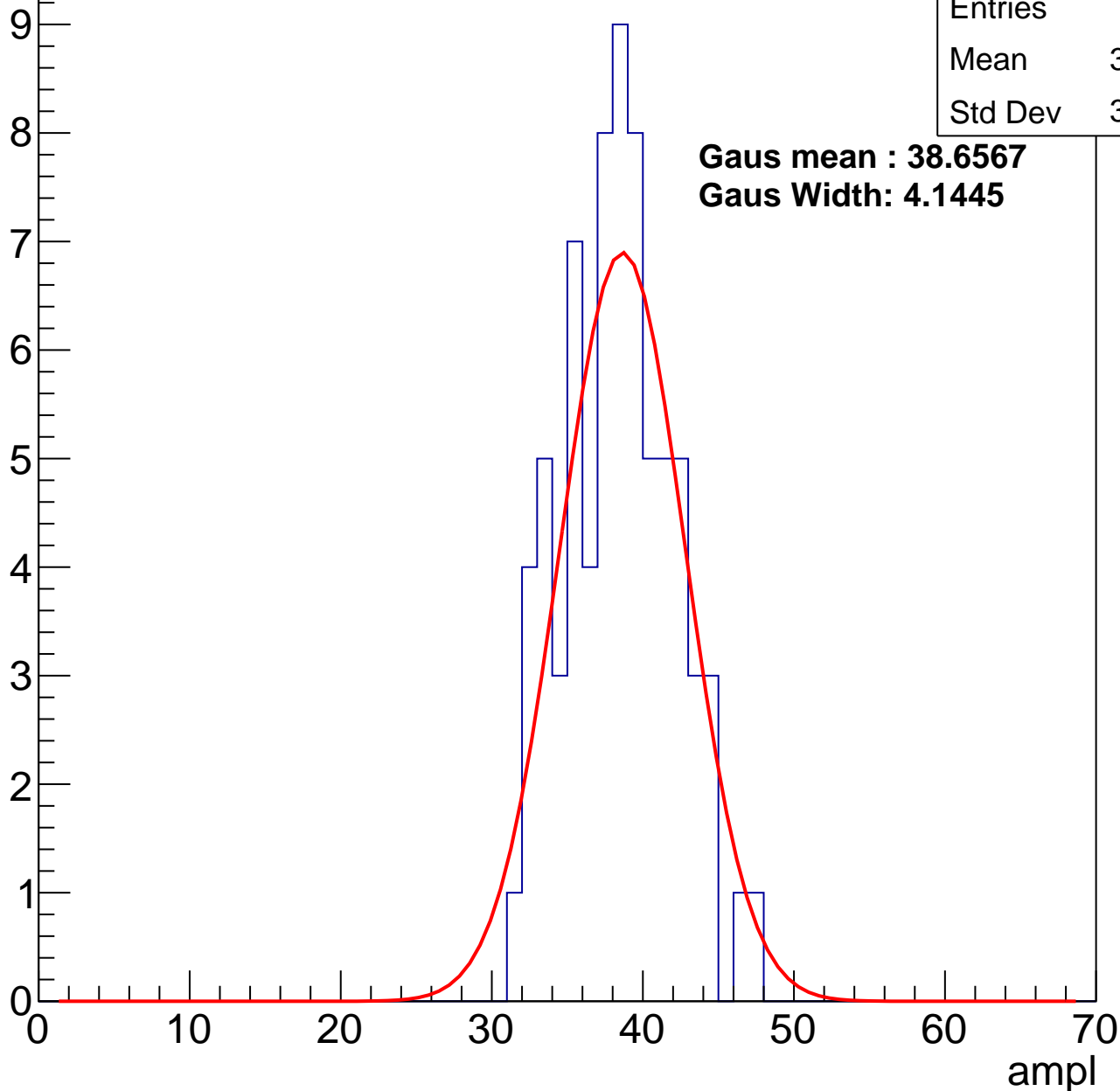
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	72
Mean	37.97
Std Dev	3.602

**Gaus mean : 38.6567**

**Gaus Width: 4.1445**



# B1L003S, U3-ch86, adc2

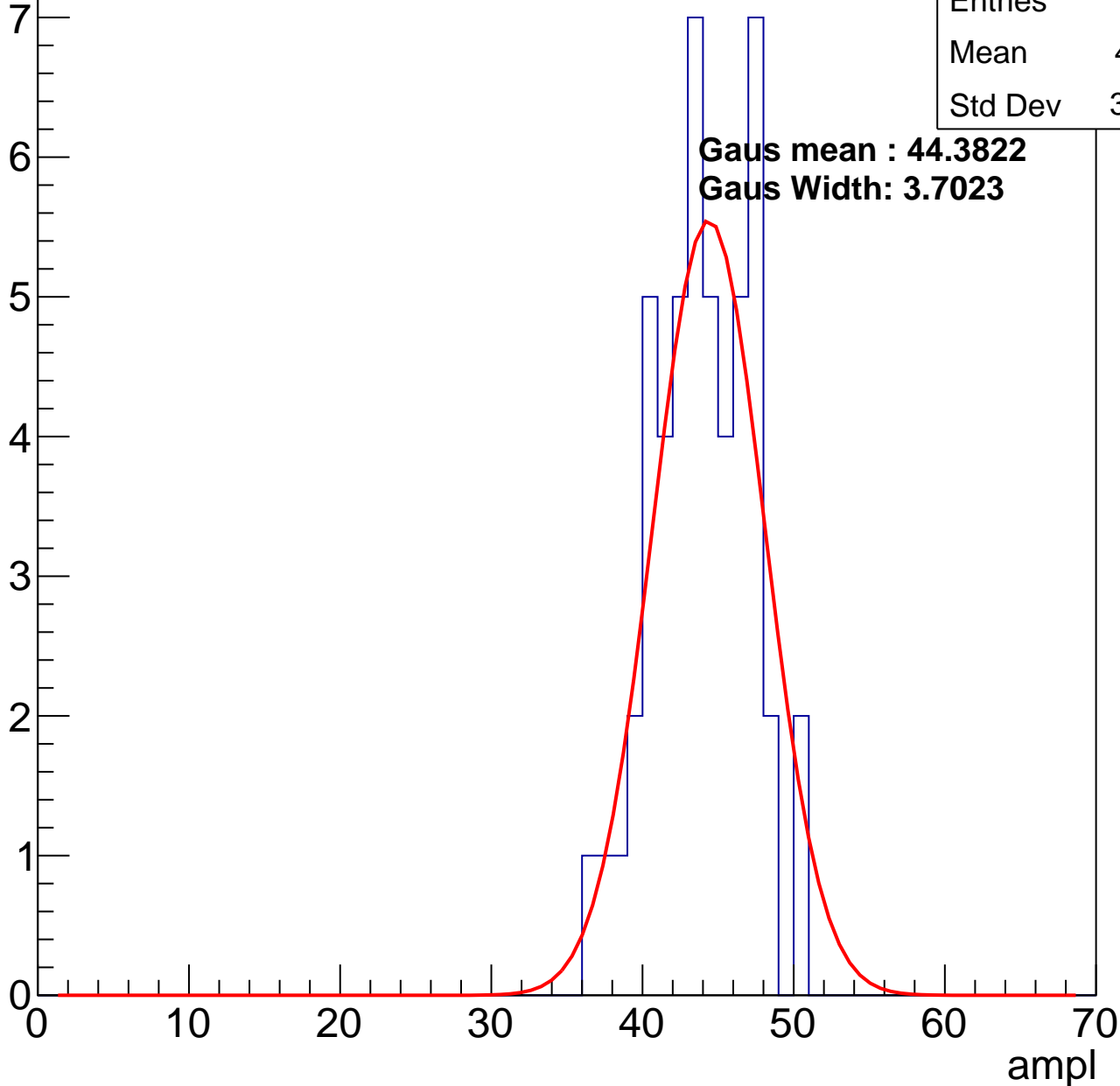
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	51
Mean	43.51
Std Dev	3.195

**Gaus mean : 44.3822**

**Gaus Width: 3.7023**

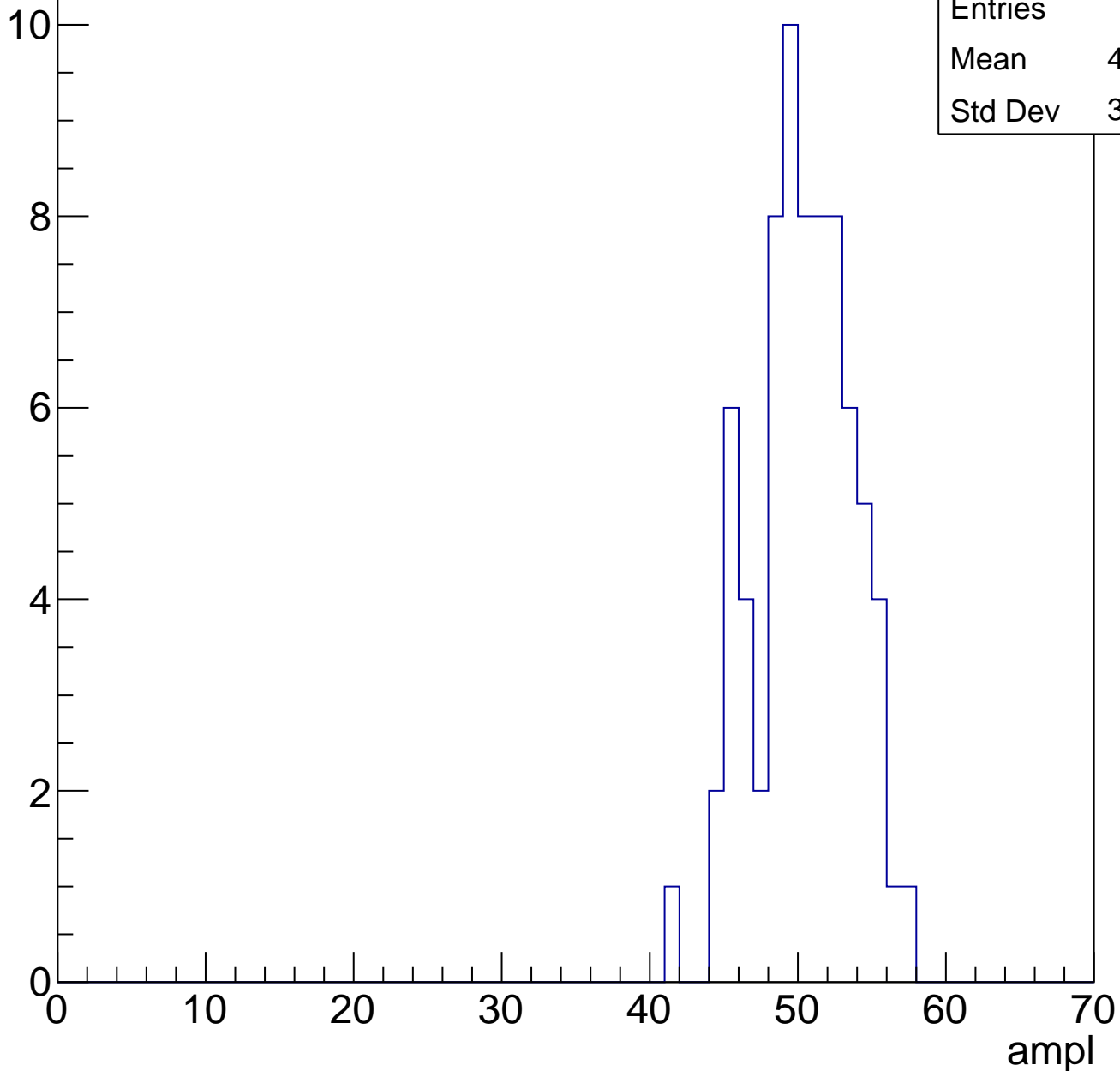


# B1L003S, U3-ch86, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	74
Mean	49.95
Std Dev	3.259

Entry

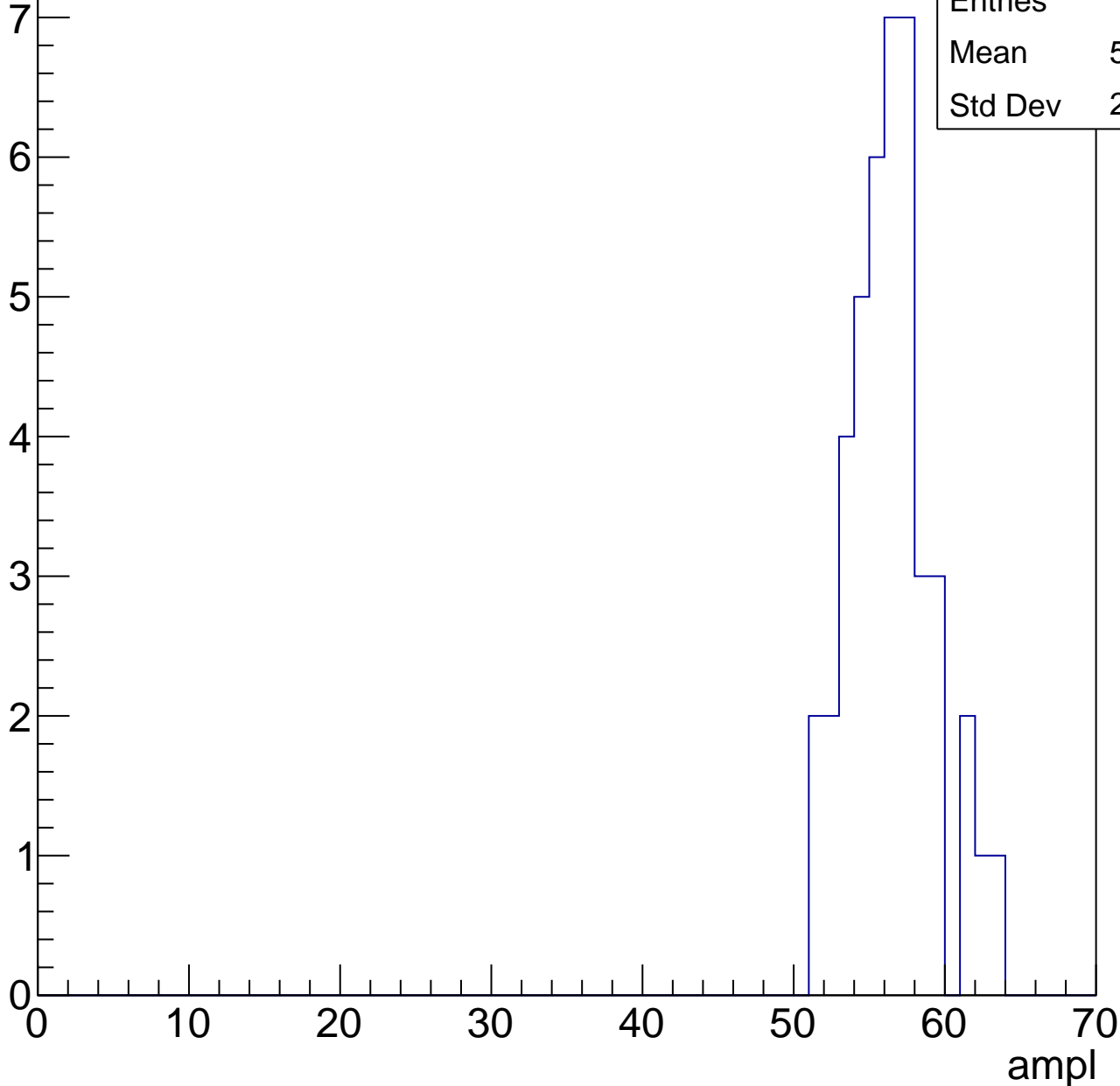


# B1L003S, U3-ch86, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	43
Mean	55.98
Std Dev	2.749

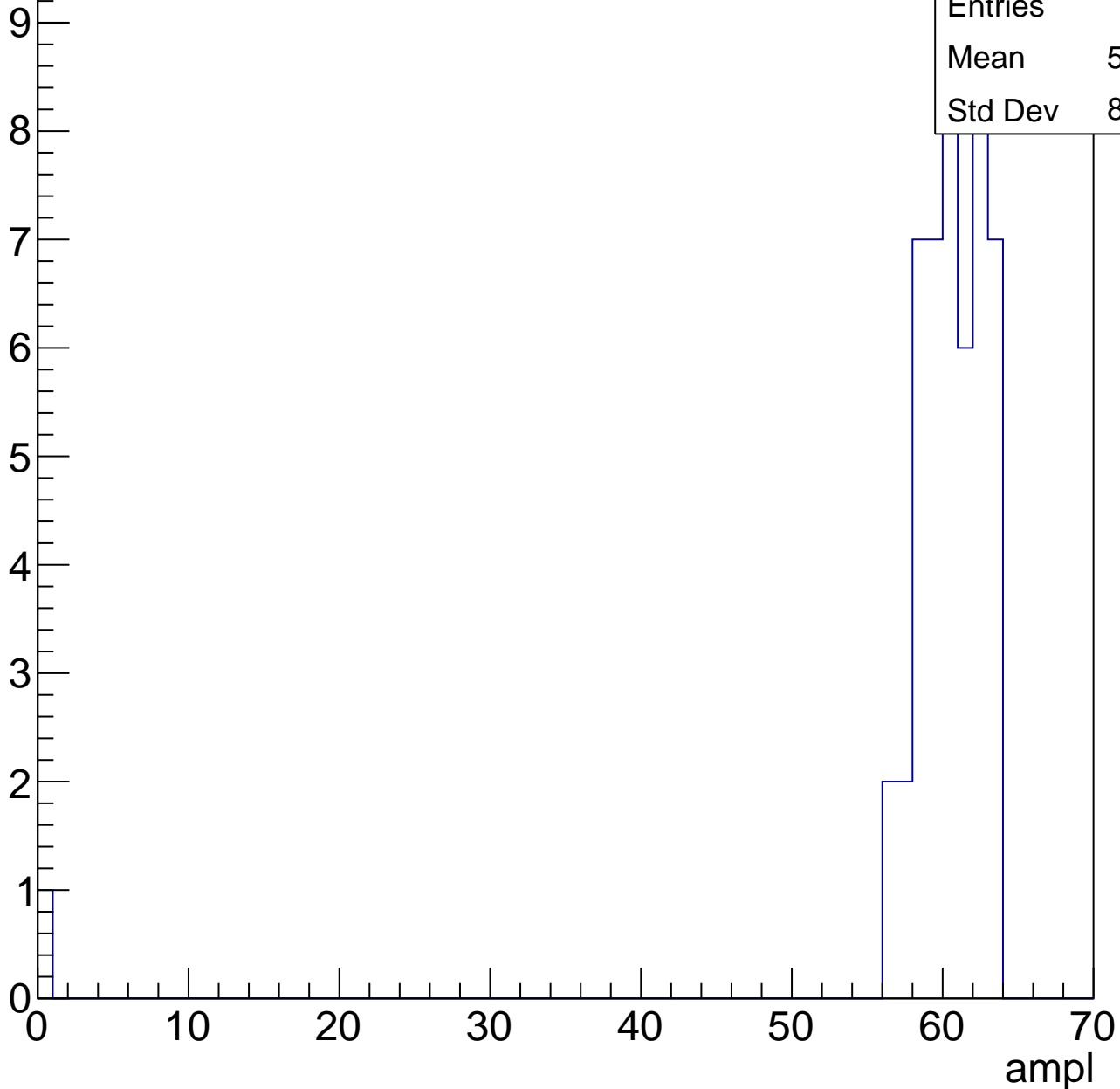


# B1L003S, U3-ch86, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	49
Mean	58.94
Std Dev	8.726



# B1L003S, U3-ch86, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

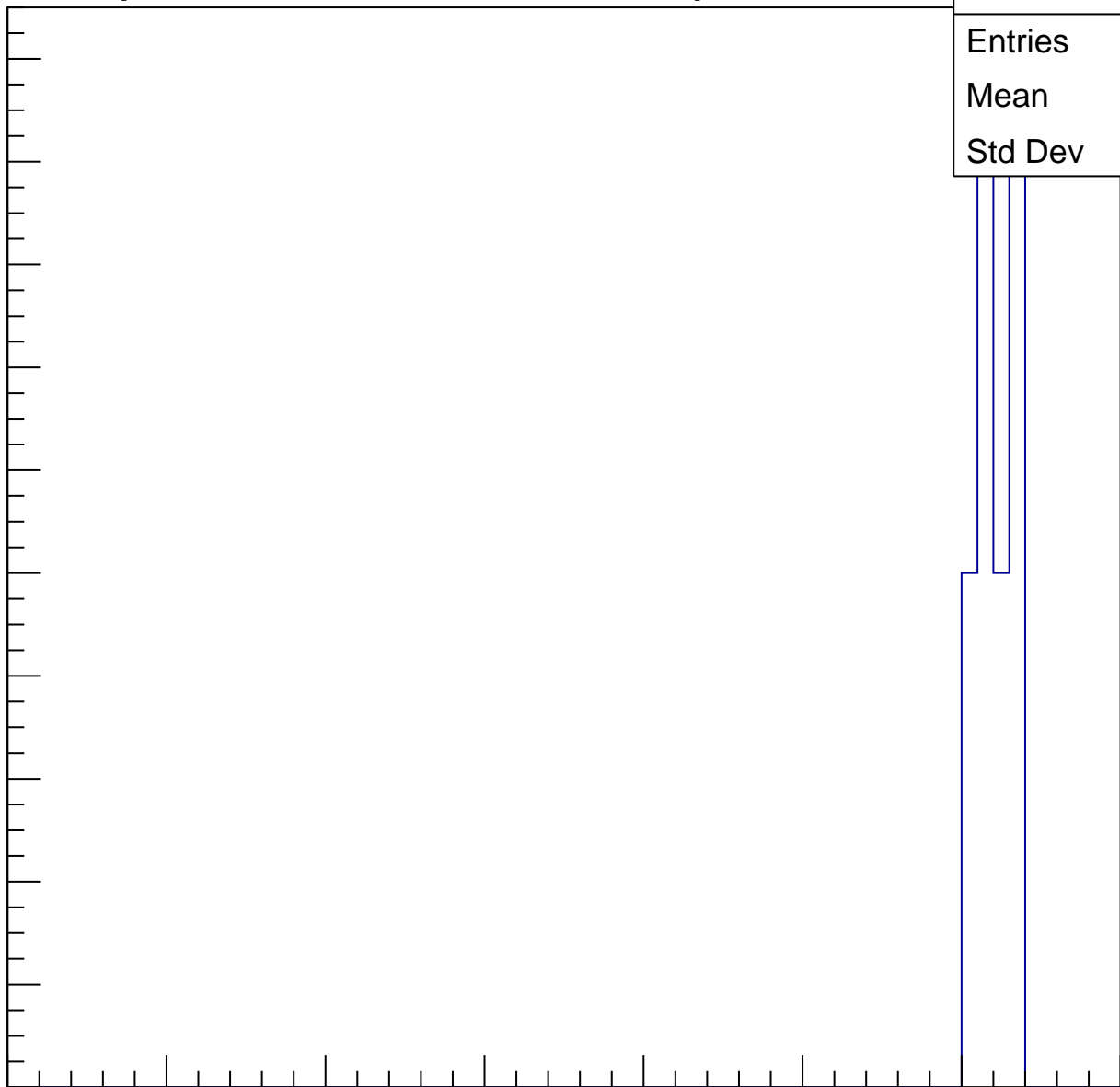
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	61.67
Std Dev	1.106

0 10 20 30 40 50 60 70

ampl





# B1L003S, U3-ch86, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U3-ch87, adc0

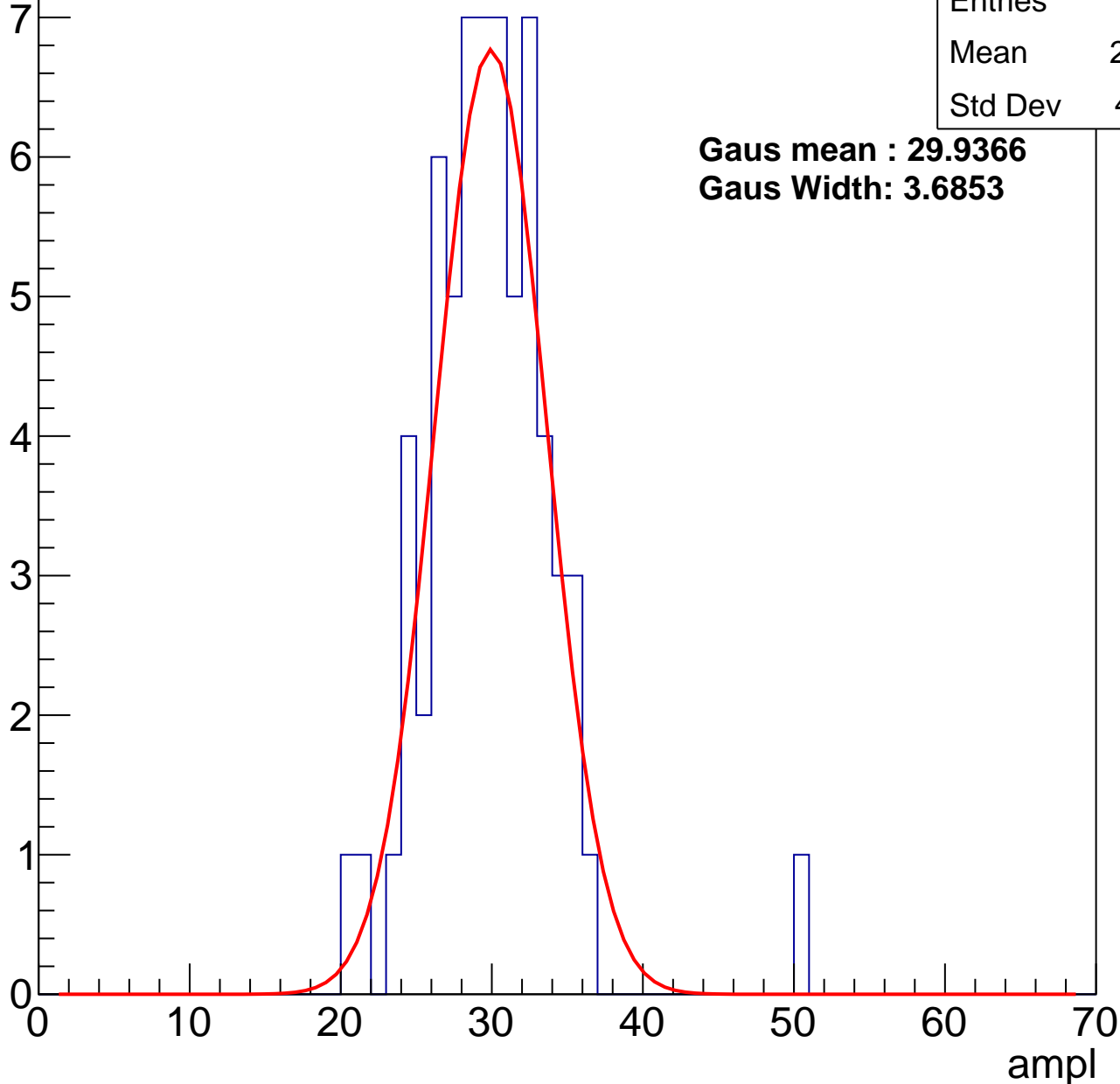
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	29.45
Std Dev	4.311

**Gaus mean : 29.9366**

**Gaus Width: 3.6853**



# B1L003S, U3-ch87, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	82
Mean	36.61
Std Dev	3.622

**Gaus mean : 37.2125**

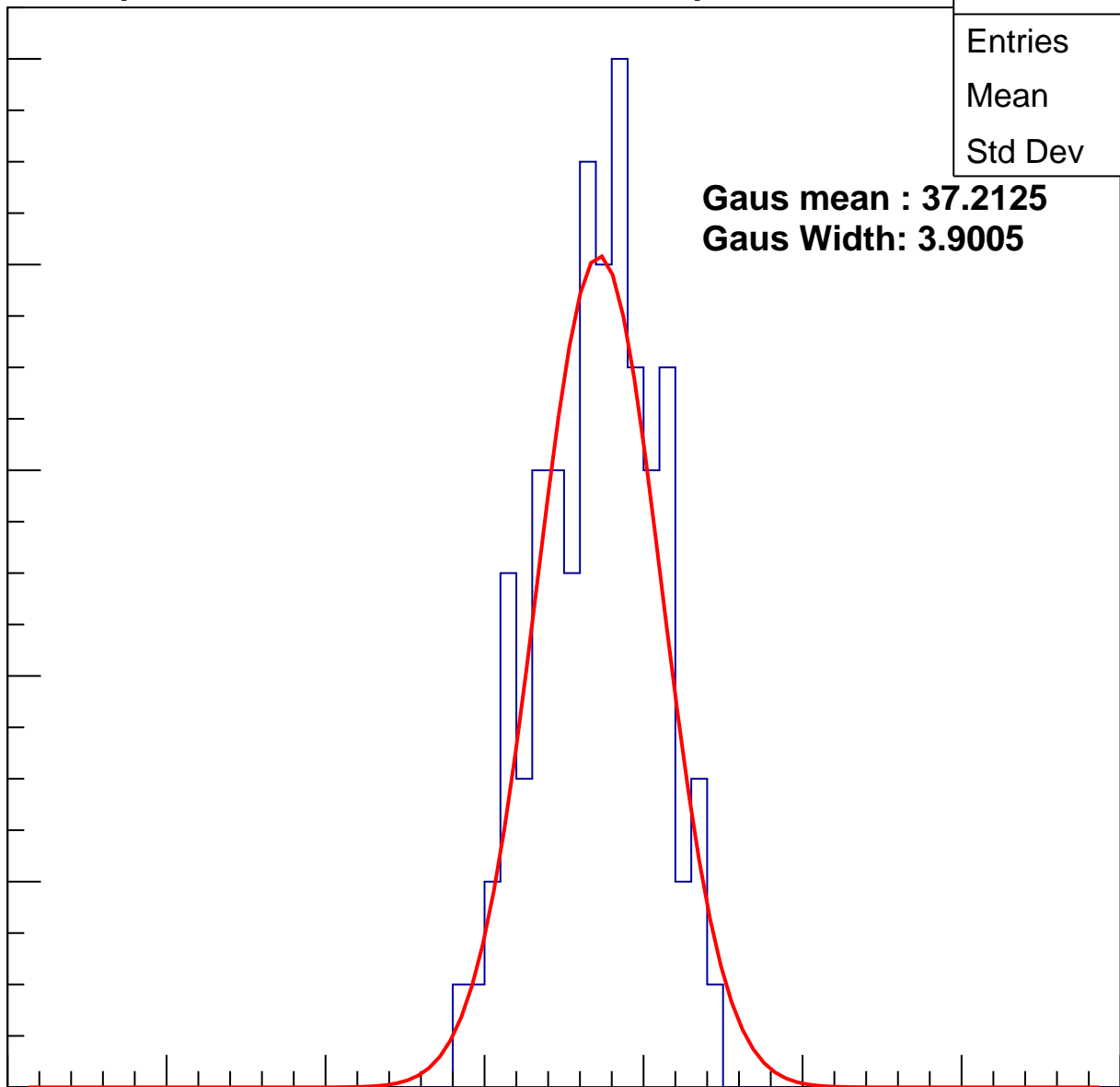
**Gaus Width: 3.9005**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L003S, U3-ch87, adc2

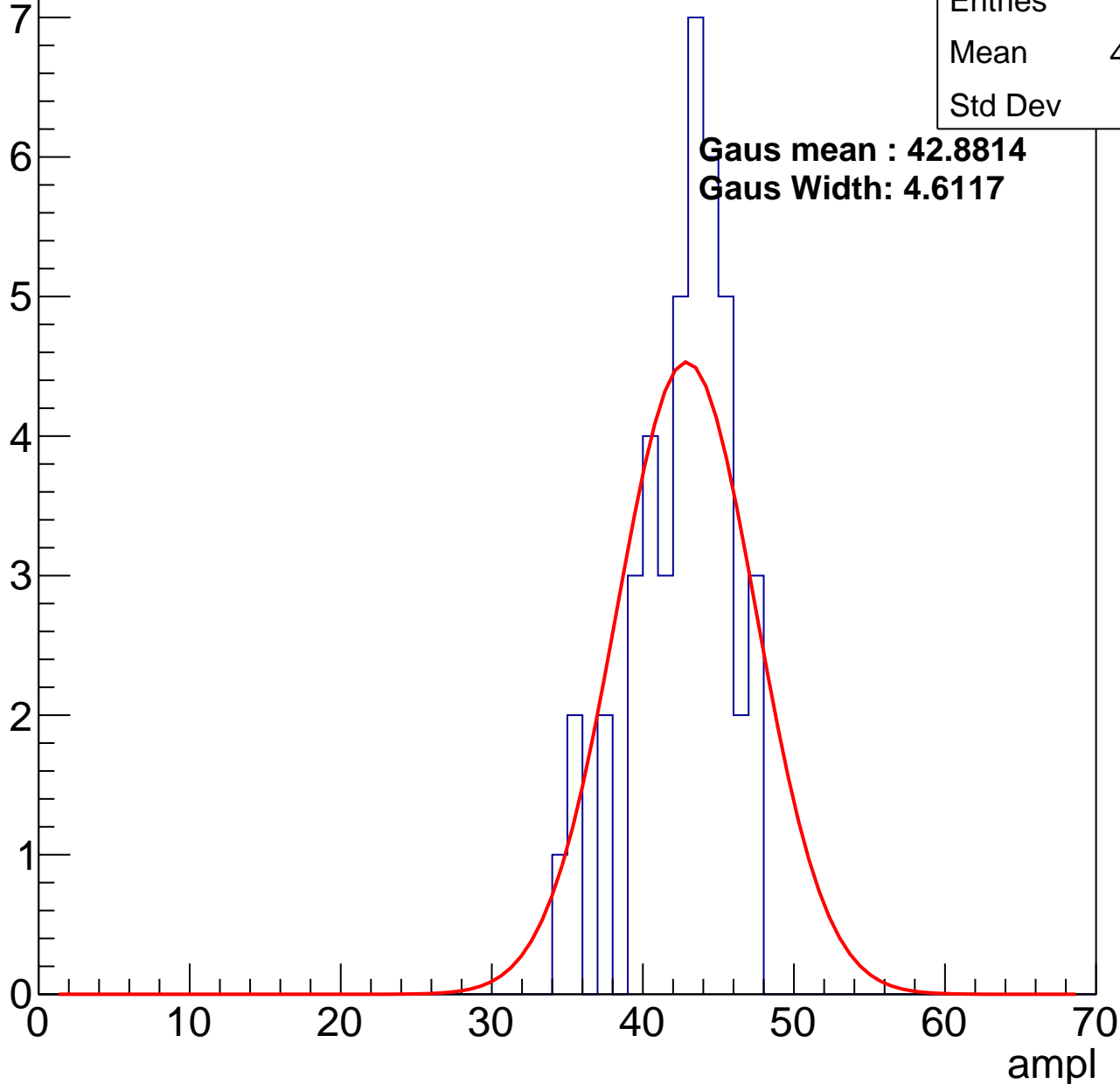
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	43
Mean	42.12
Std Dev	3.2

**Gaus mean : 42.8814**

**Gaus Width: 4.6117**



# B1L003S, U3-ch87, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

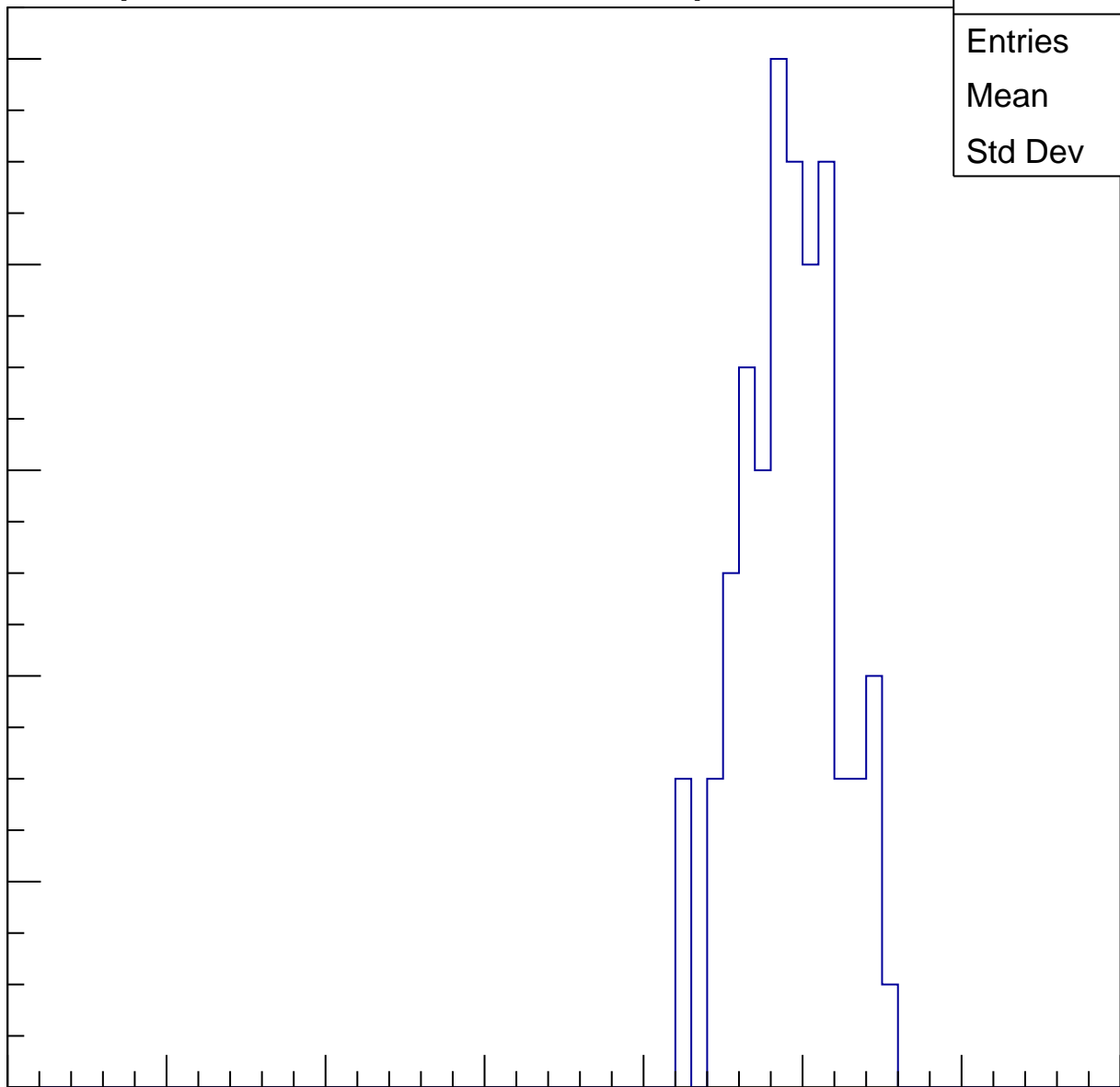
Entries	71
Mean	48.63
Std Dev	3.013

Entry

10  
8  
6  
4  
2  
0

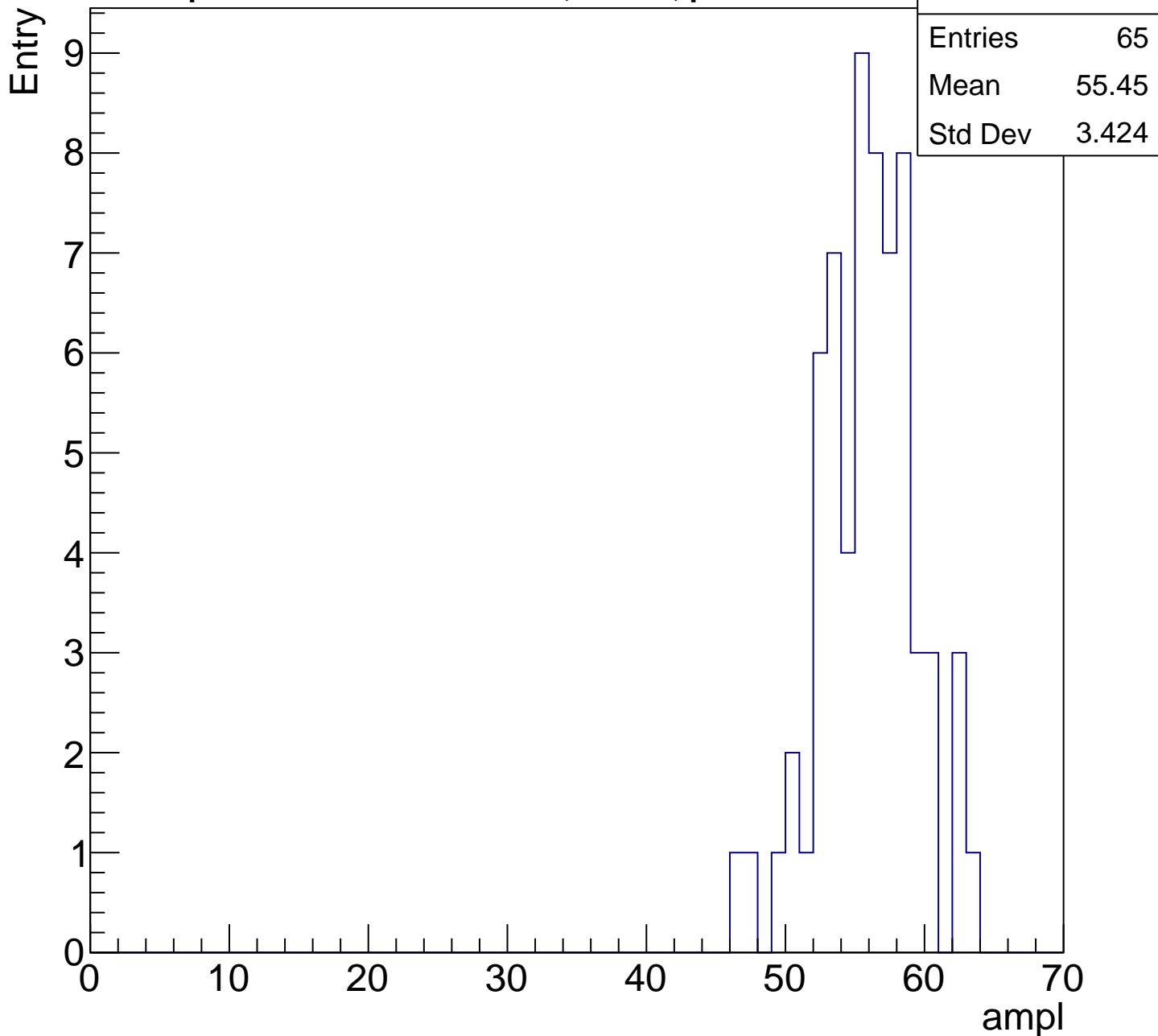
0 10 20 30 40 50 60 70

ampl



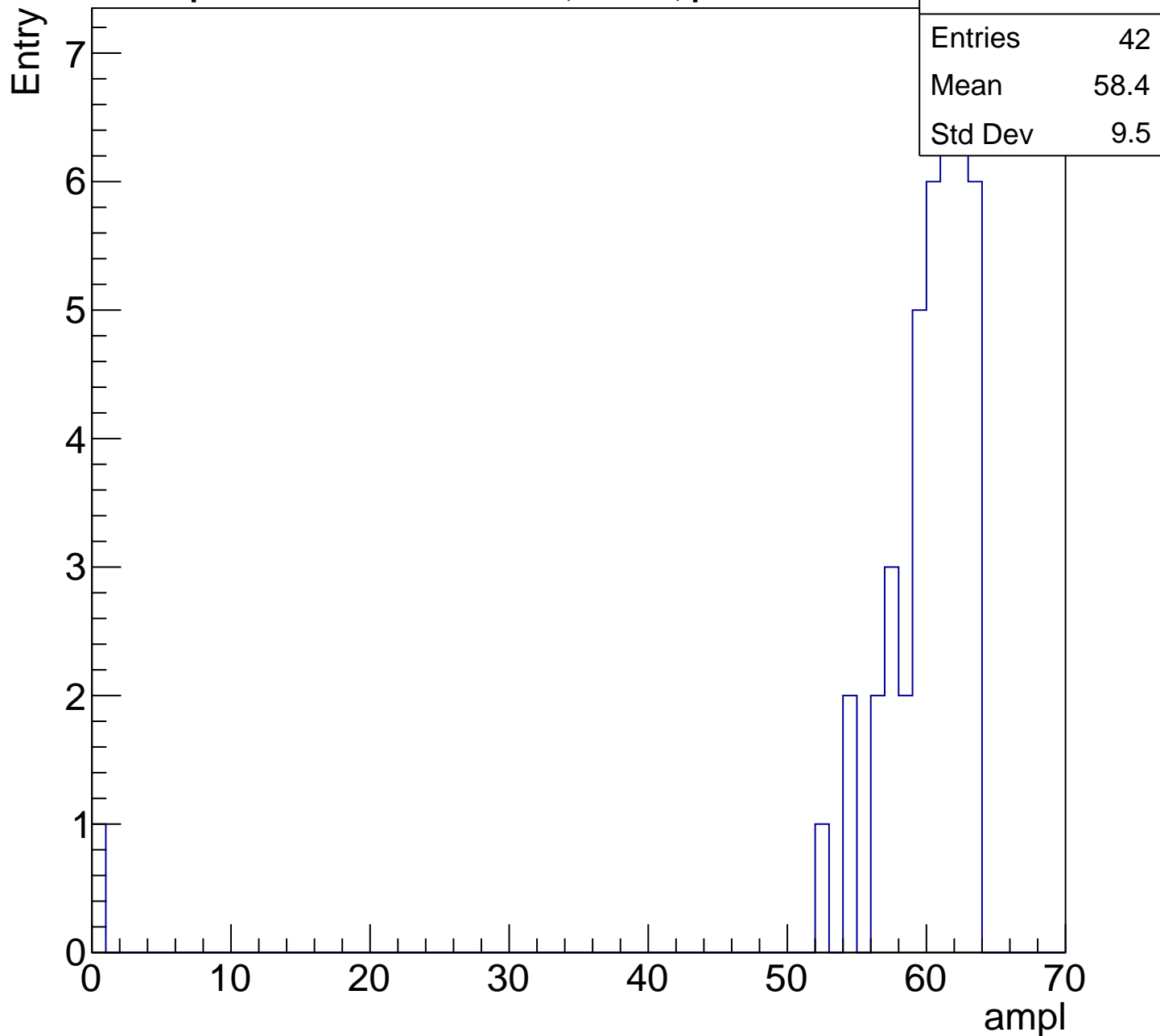
# B1L003S, U3-ch87, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2



# B1L003S, U3-ch87, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2



# B1L003S, U3-ch87, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries

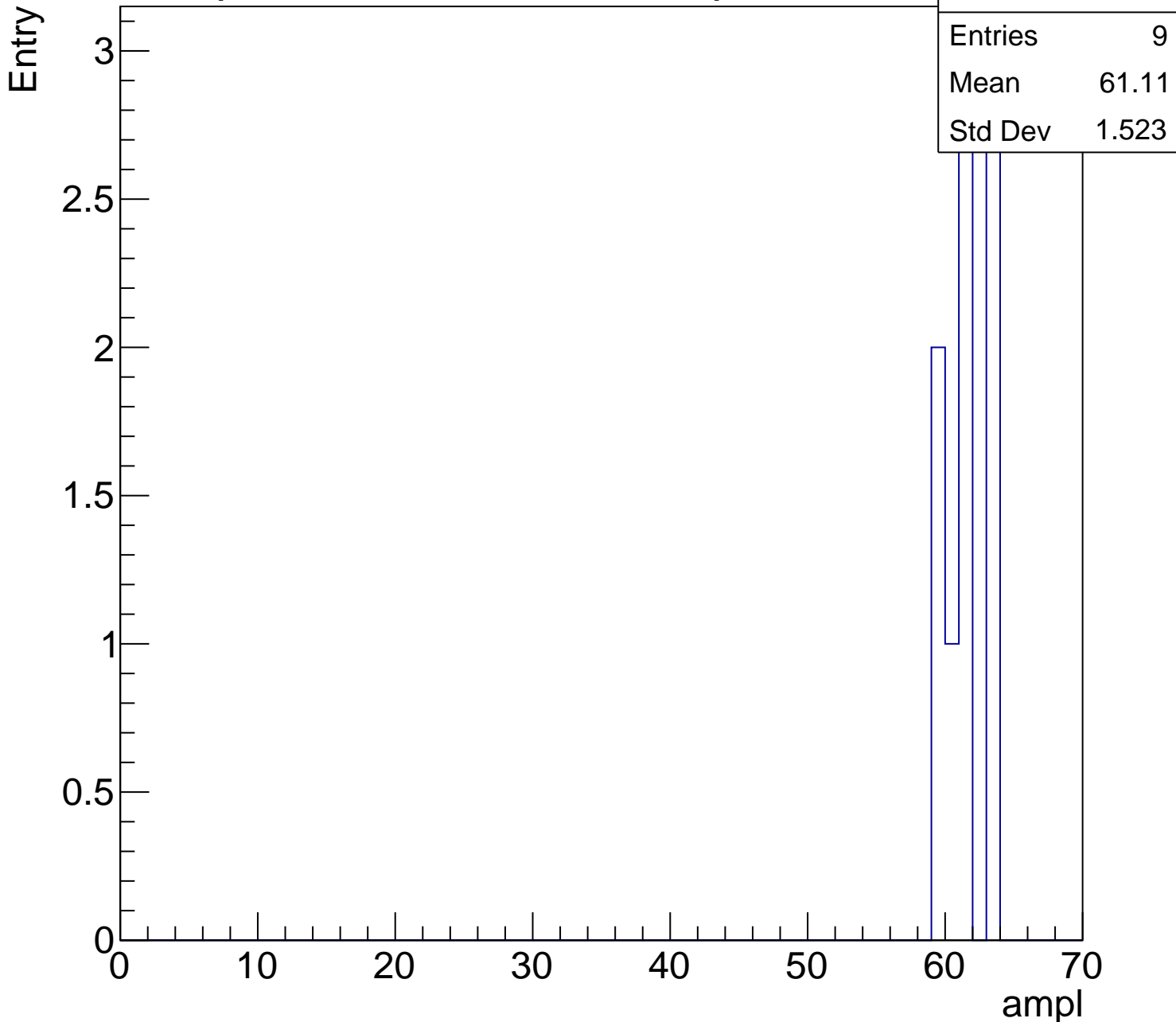
9

Mean

61.11

Std Dev

1.523

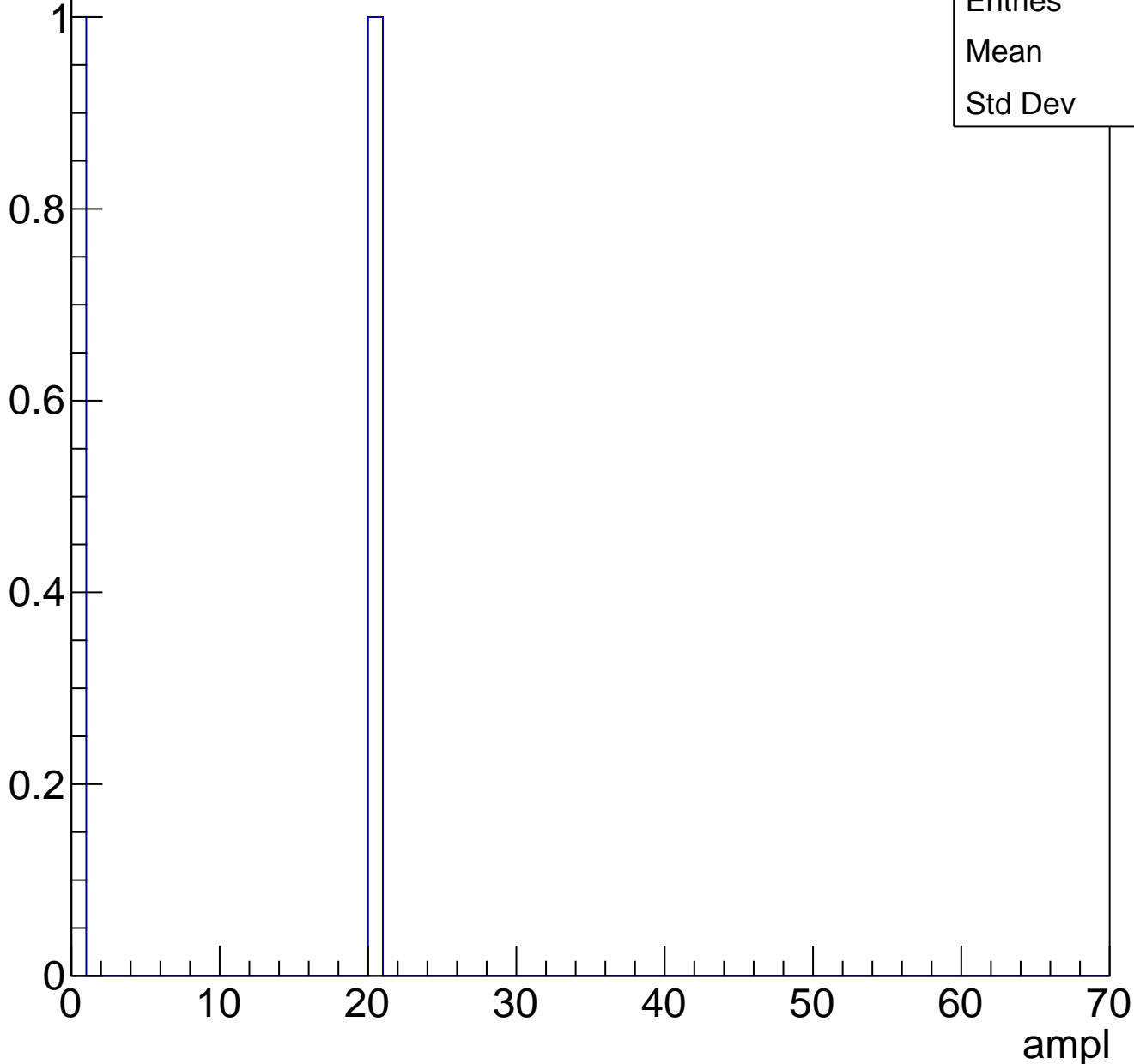




# B1L003S, U3-ch87, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U3-ch88, adc0

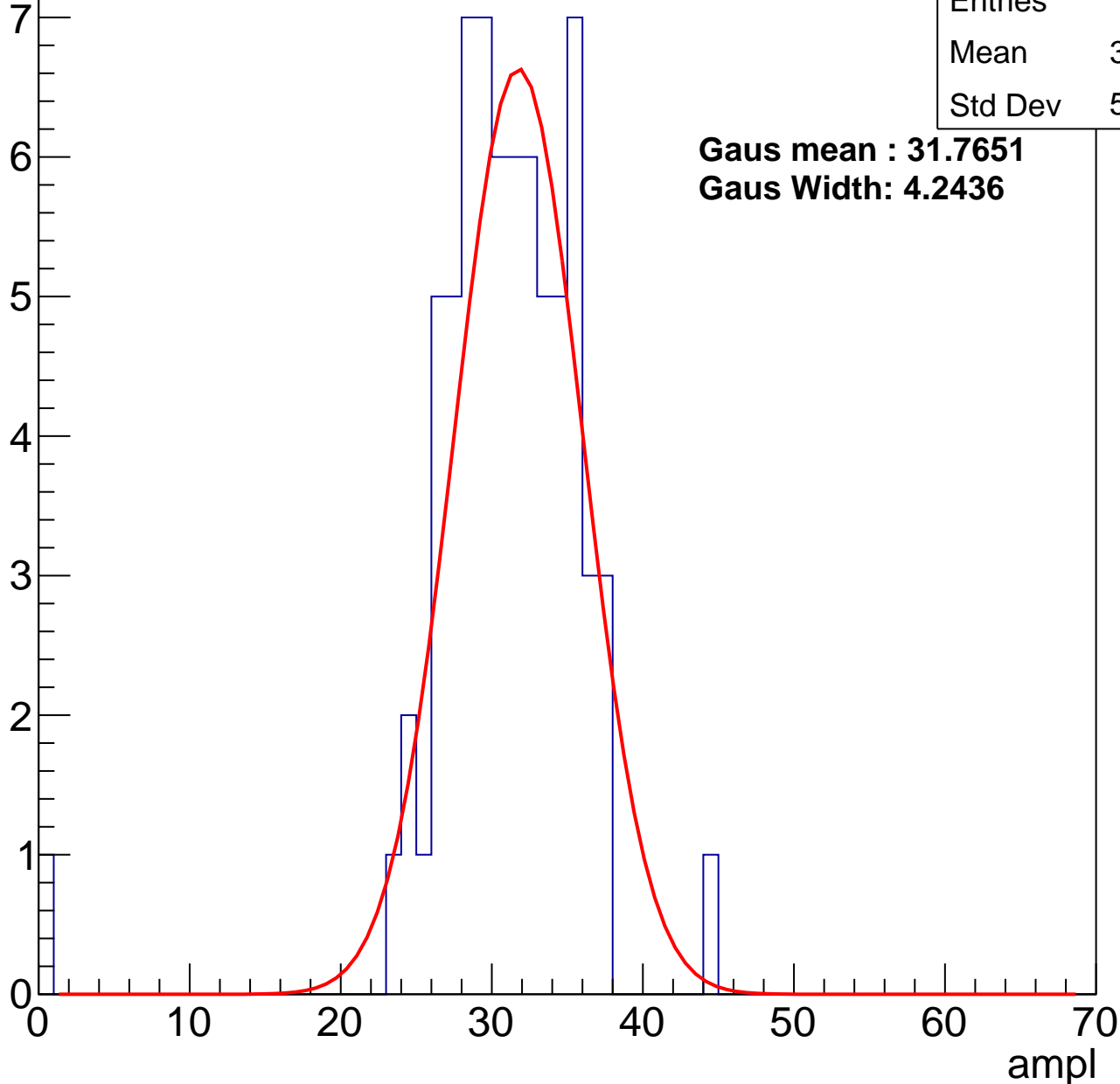
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	71
Mean	30.44
Std Dev	5.272

**Gaus mean : 31.7651**

**Gaus Width: 4.2436**



# B1L003S, U3-ch88, adc1

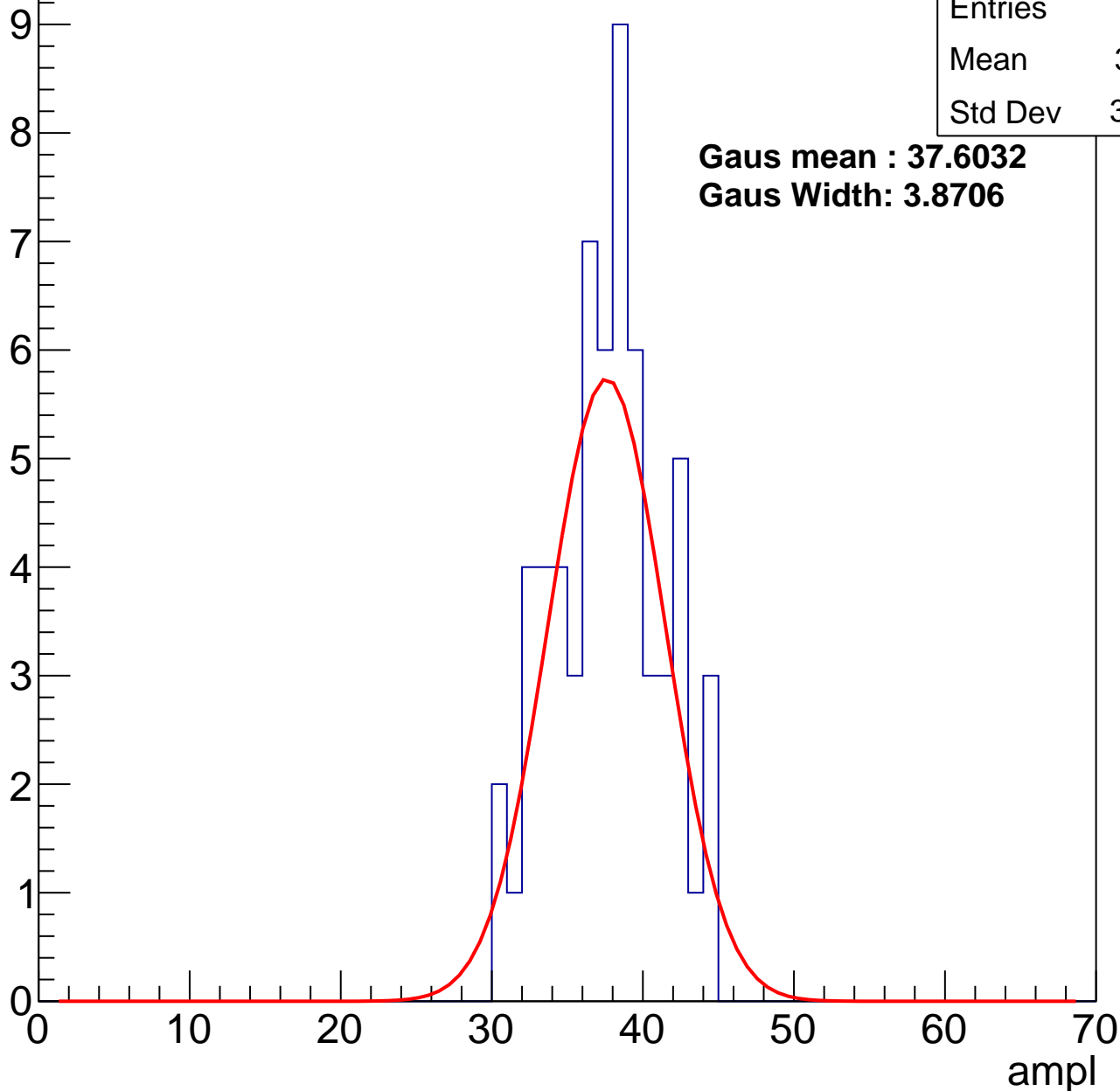
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	37.21
Std Dev	3.544

**Gaus mean : 37.6032**

**Gaus Width: 3.8706**



# B1L003S, U3-ch88, adc2

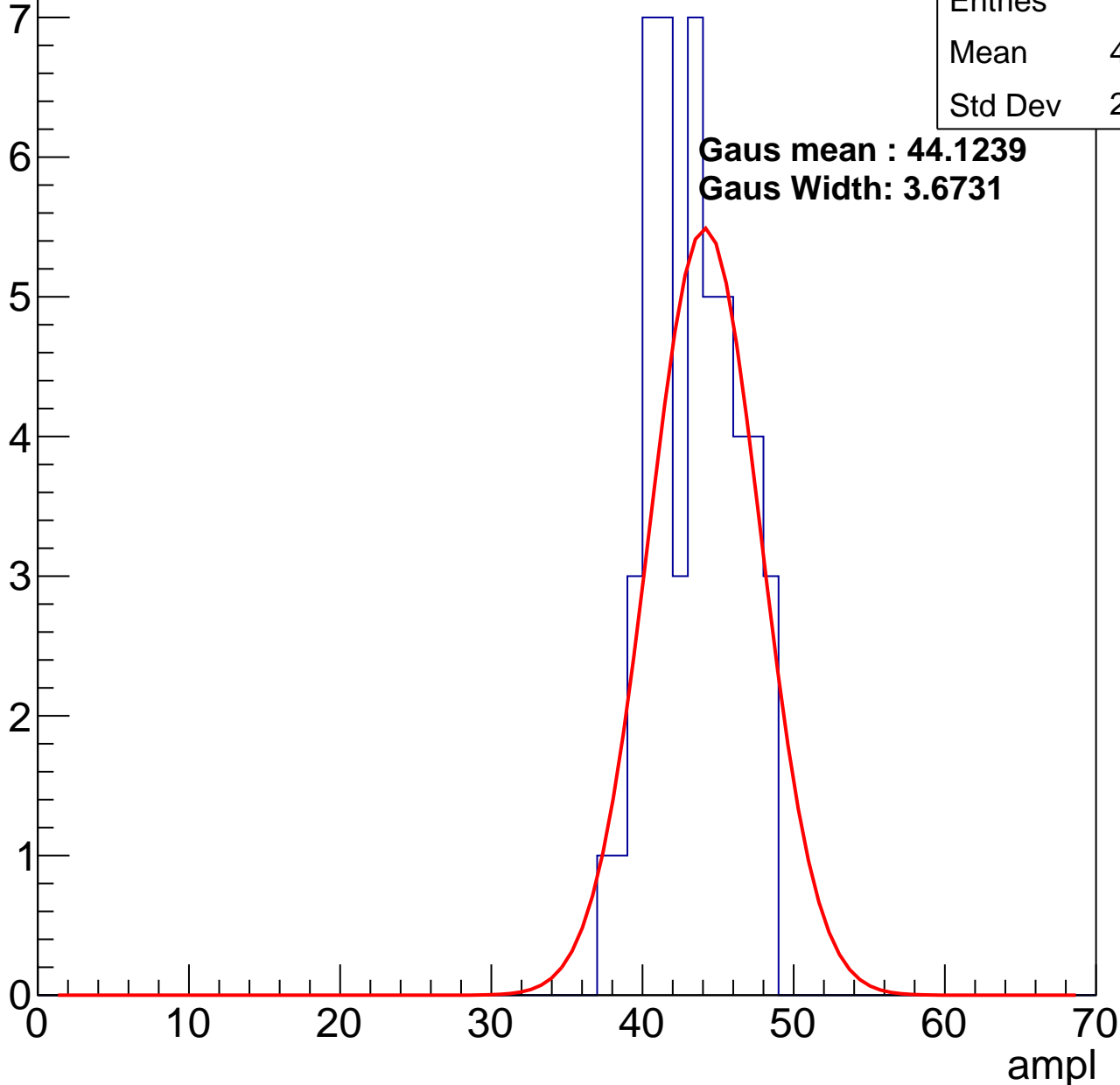
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	50
Mean	42.94
Std Dev	2.838

**Gaus mean : 44.1239**

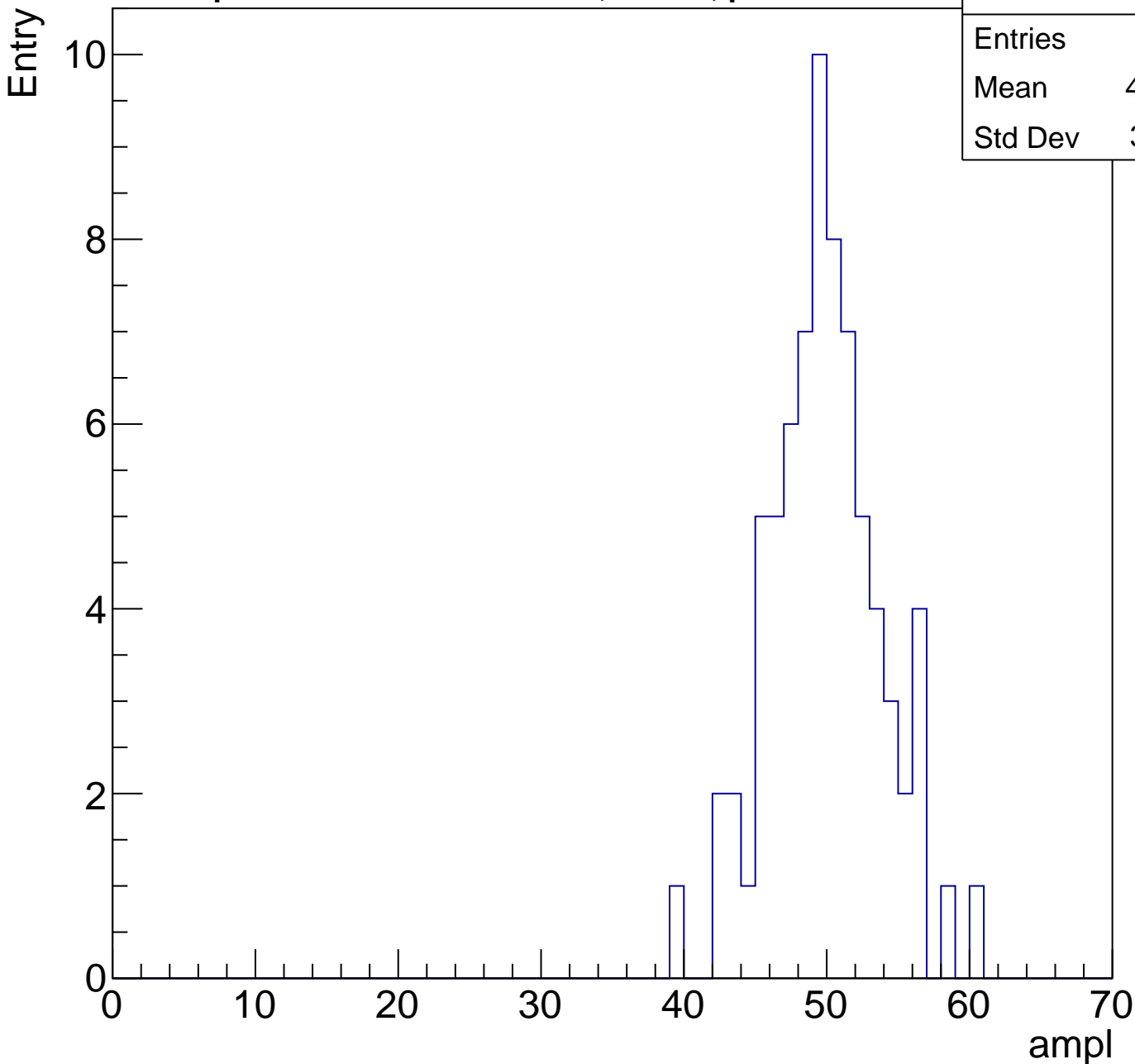
**Gaus Width: 3.6731**



# B1L003S, U3-ch88, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	74
Mean	49.45
Std Dev	3.901

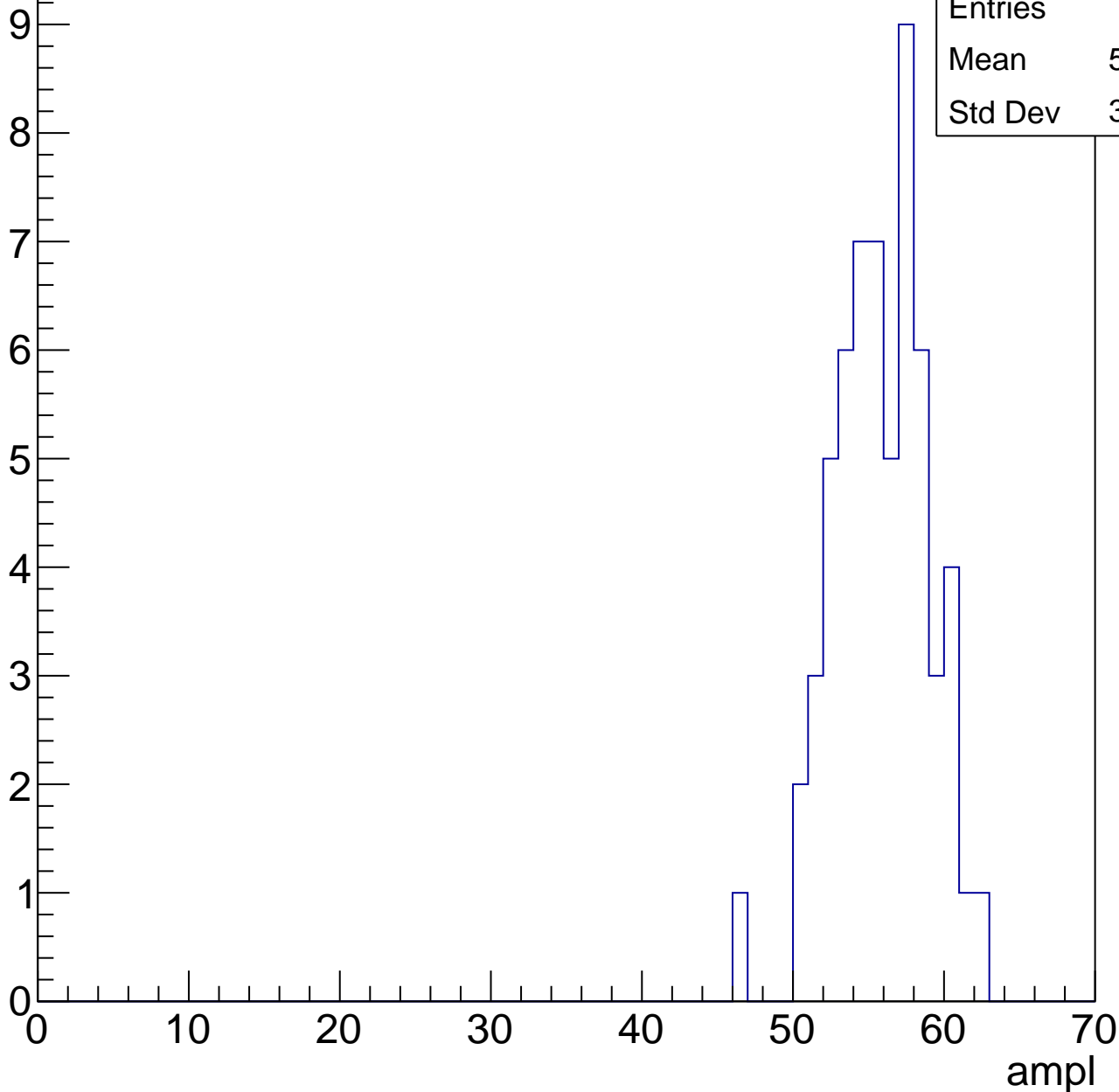


# B1L003S, U3-ch88, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	55.35
Std Dev	3.097

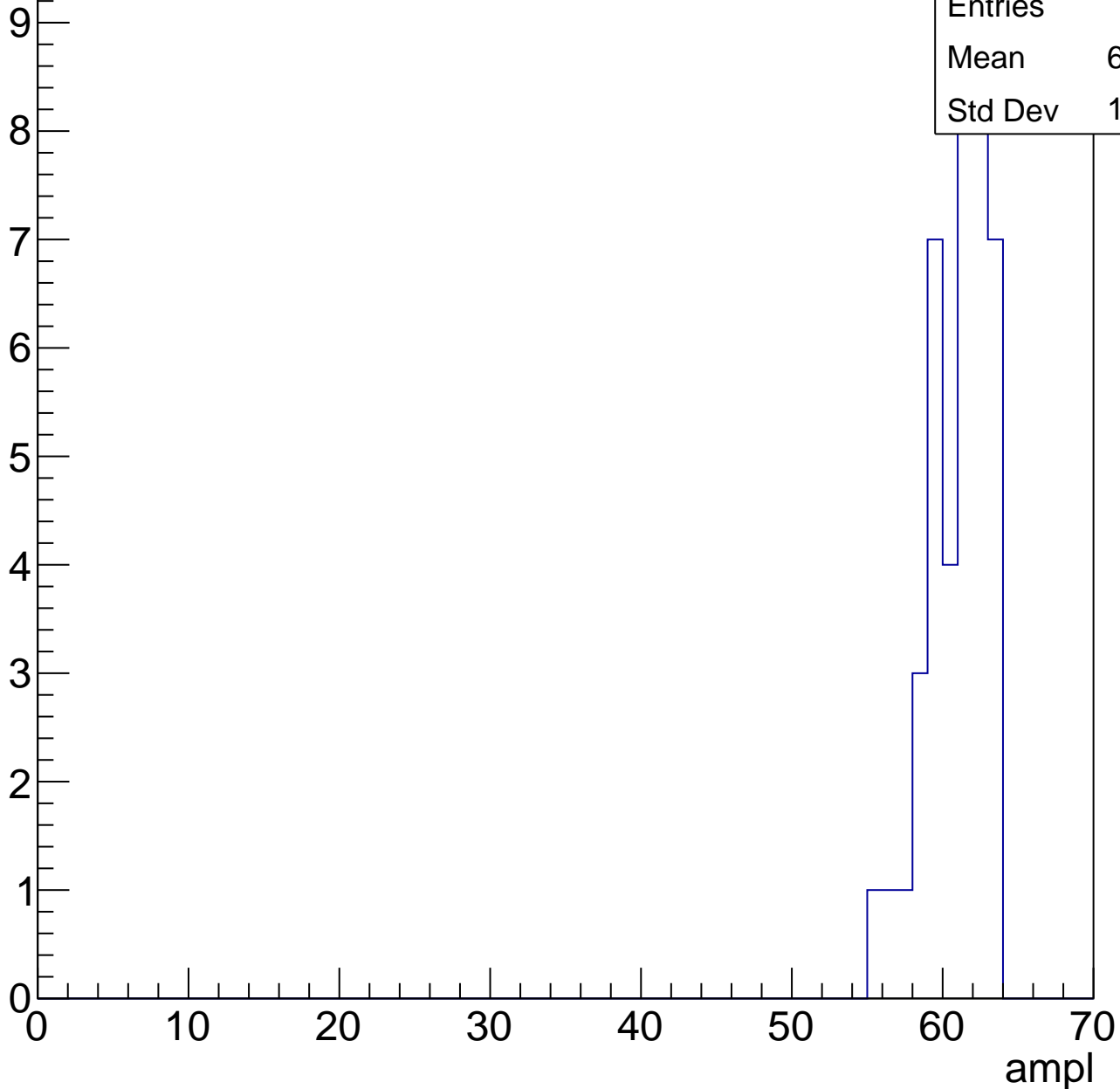


# B1L003S, U3-ch88, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

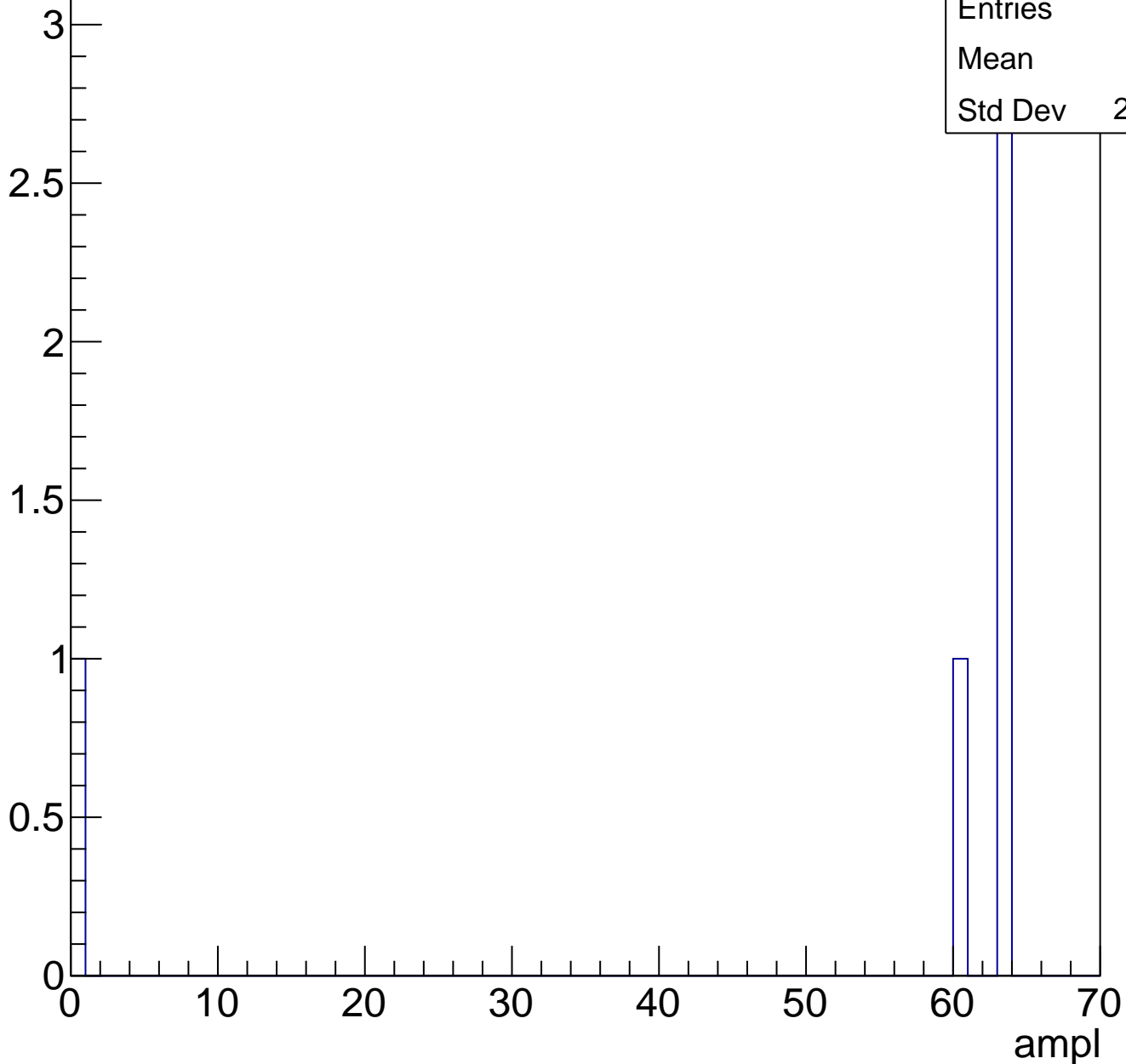
Entries	42
Mean	60.55
Std Dev	1.978



# B1L003S, U3-ch88, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch88, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U3-ch89, adc0

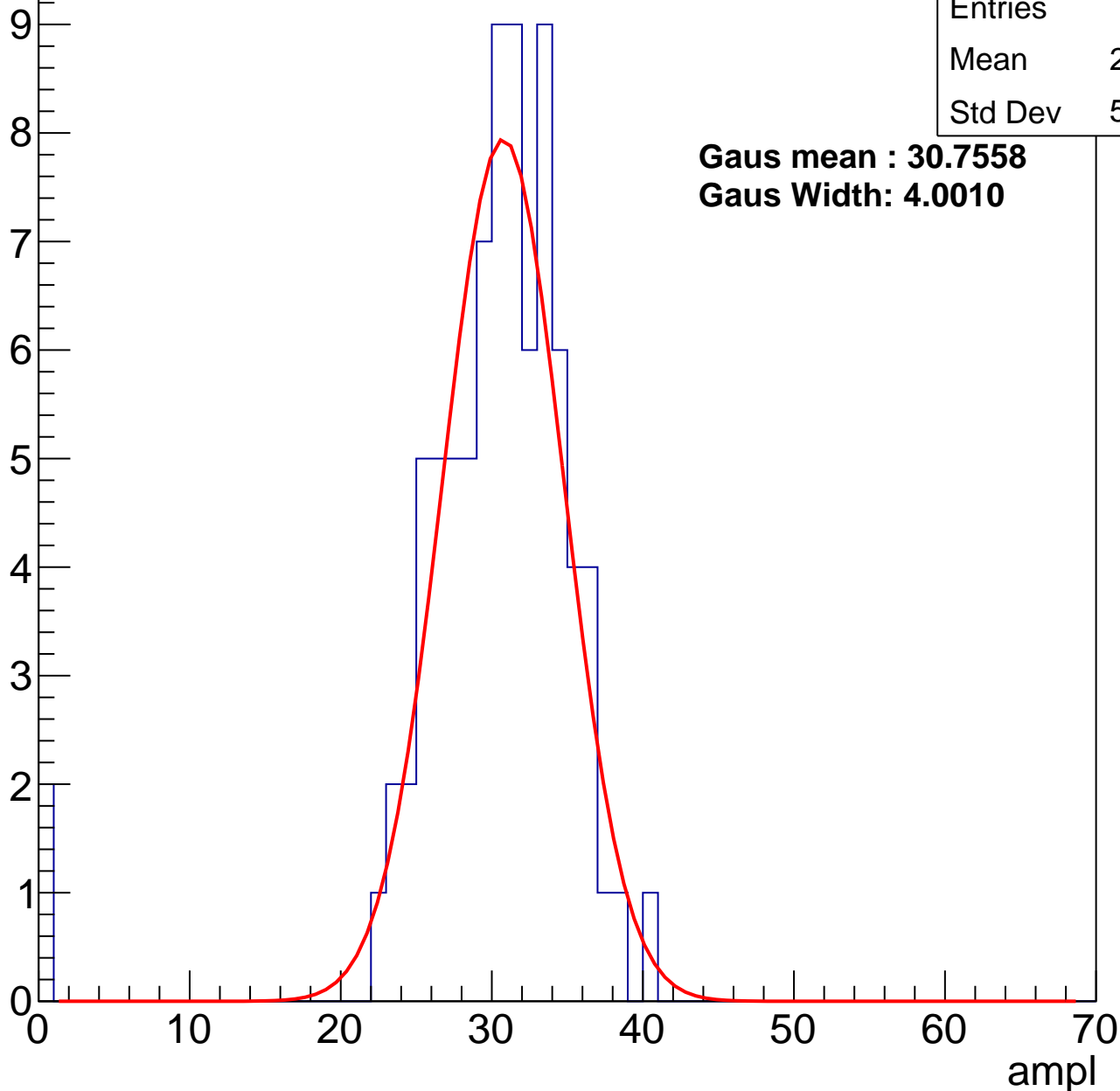
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	84
Mean	29.64
Std Dev	5.943

**Gaus mean : 30.7558**

**Gaus Width: 4.0010**



# B1L003S, U3-ch89, adc1

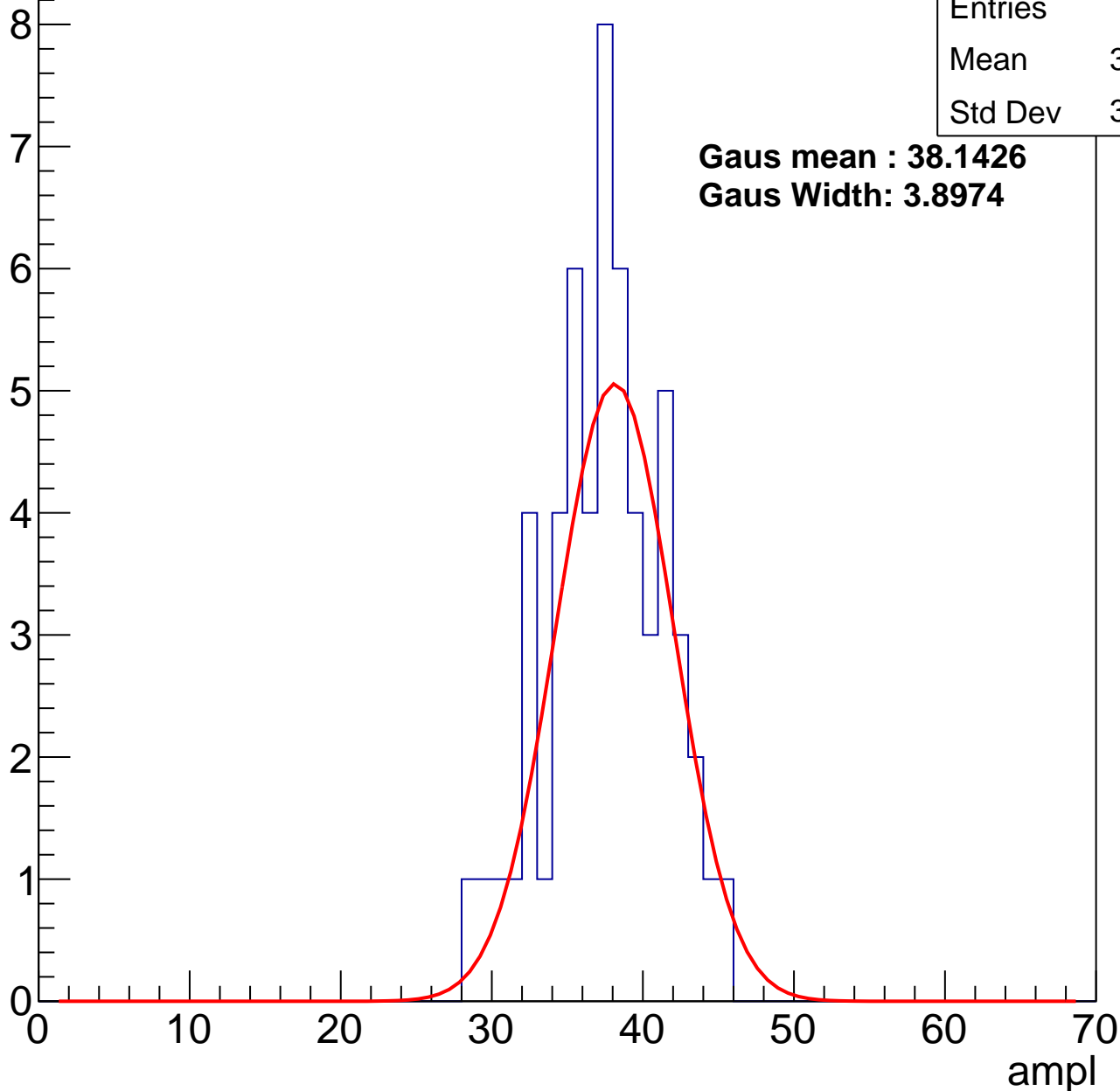
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	37.05
Std Dev	3.777

**Gaus mean : 38.1426**

**Gaus Width: 3.8974**

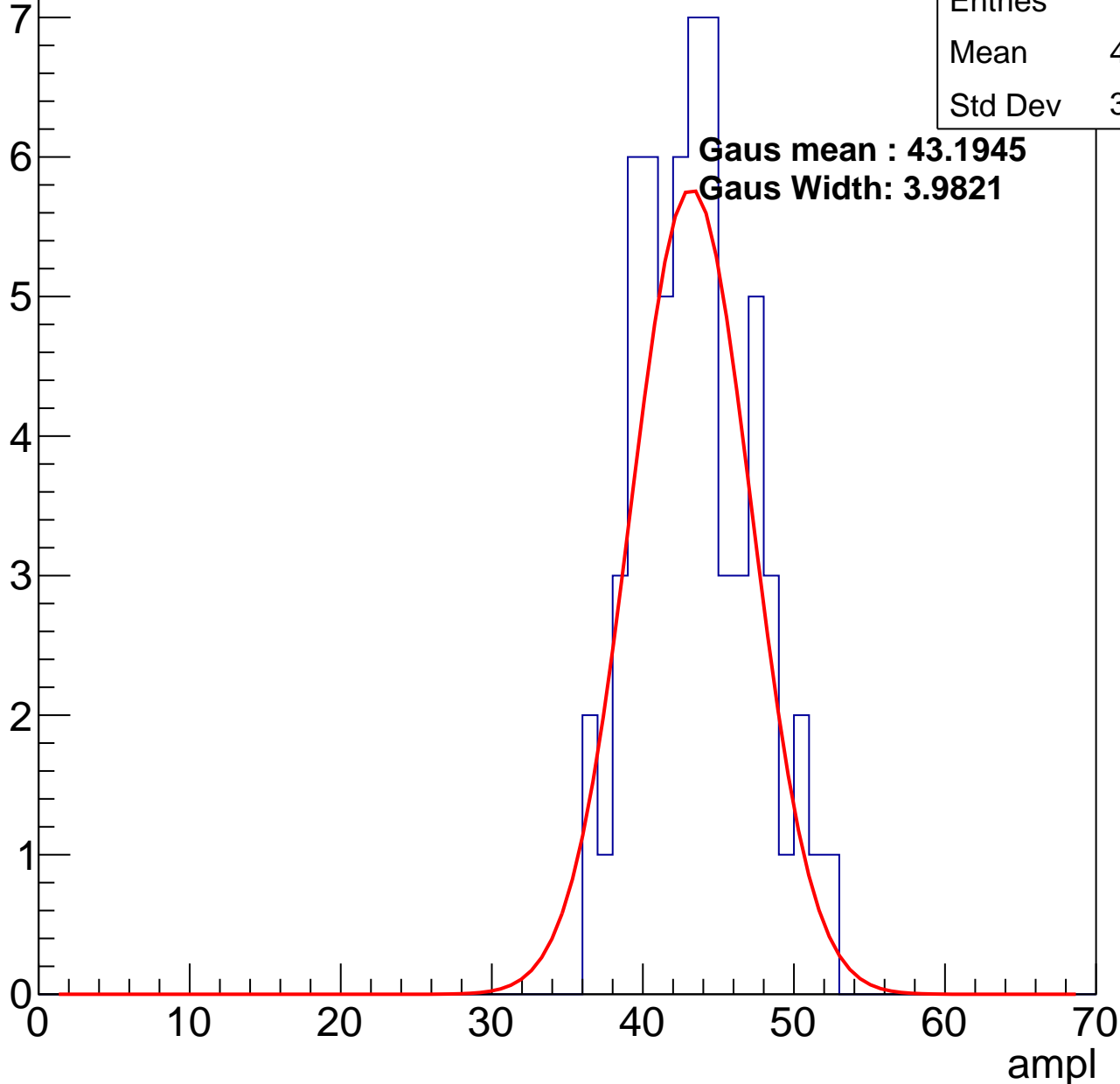


# B1L003S, U3-ch89, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	43.02
Std Dev	3.735

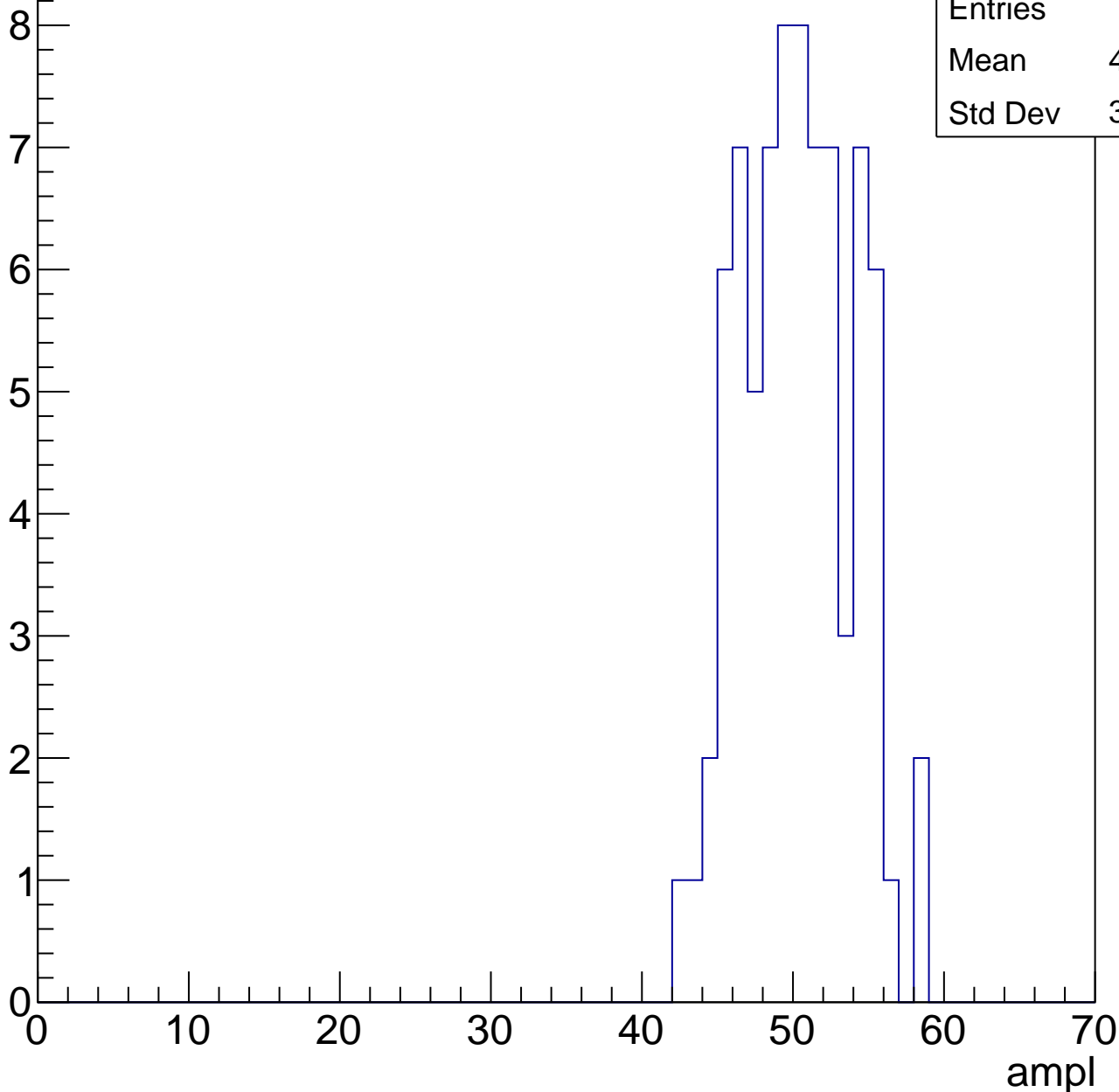


# B1L003S, U3-ch89, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	78
Mean	49.85
Std Dev	3.606

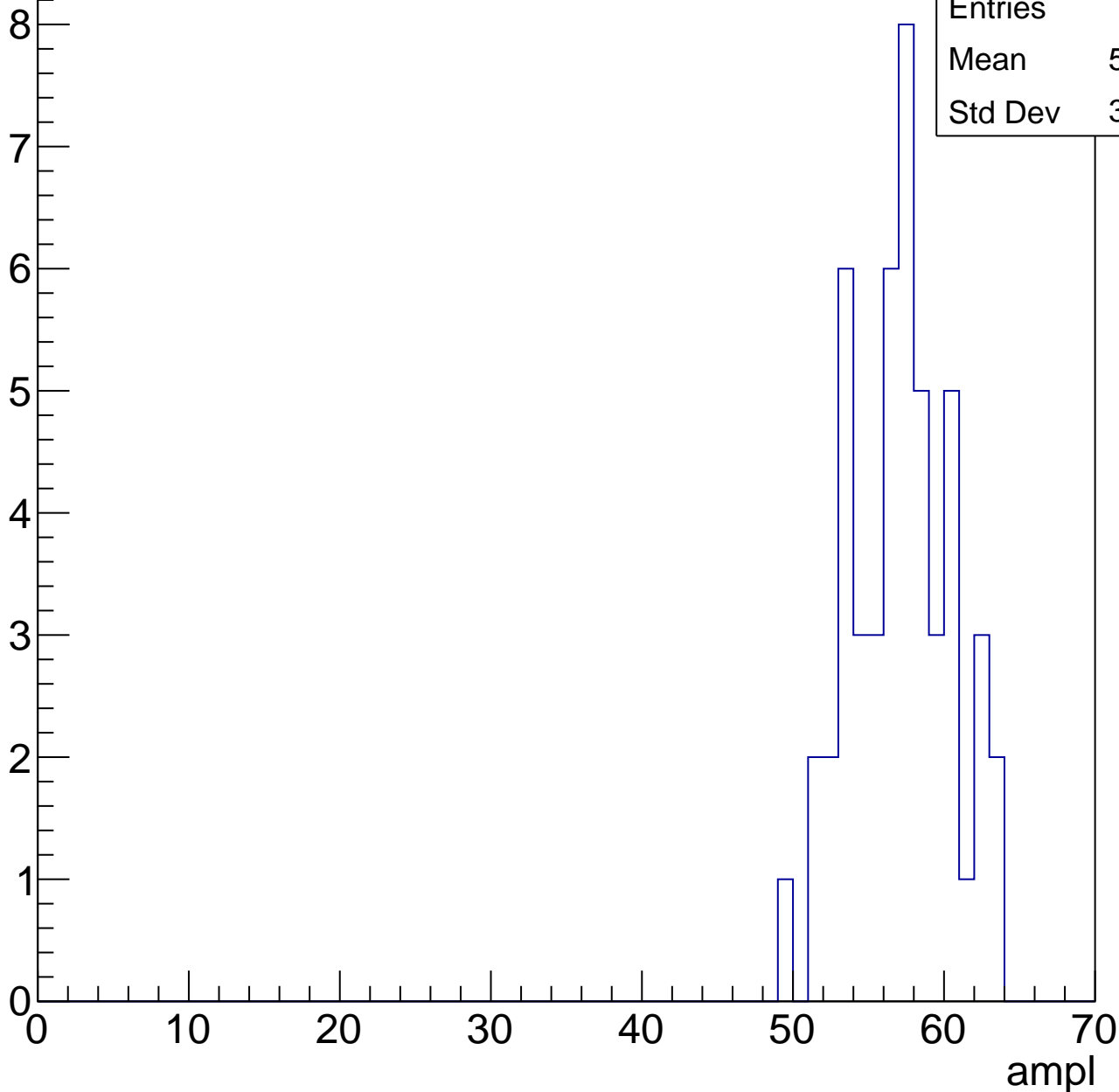


# B1L003S, U3-ch89, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

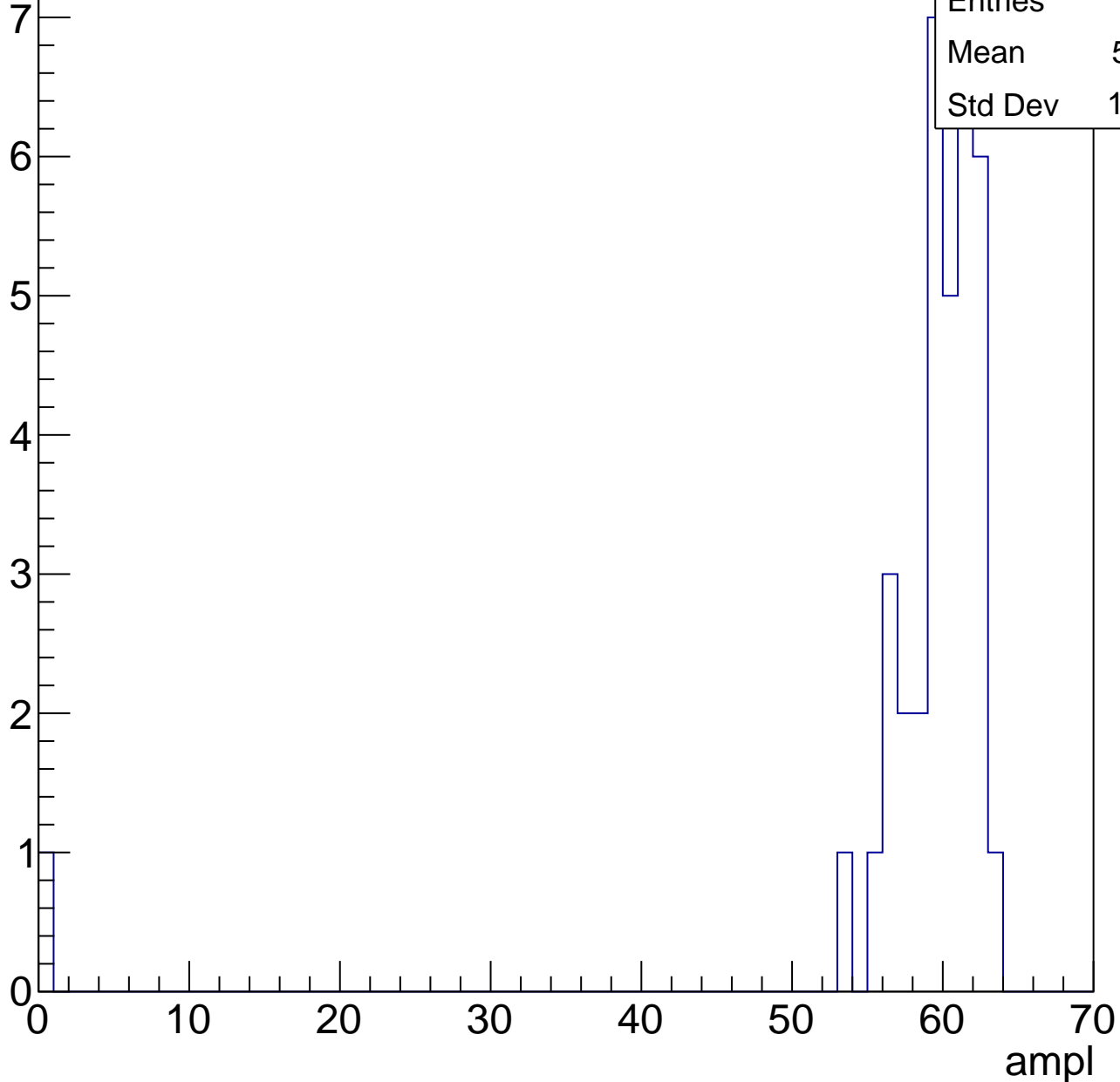
Entries	50
Mean	56.64
Std Dev	3.303



# B1L003S, U3-ch89, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

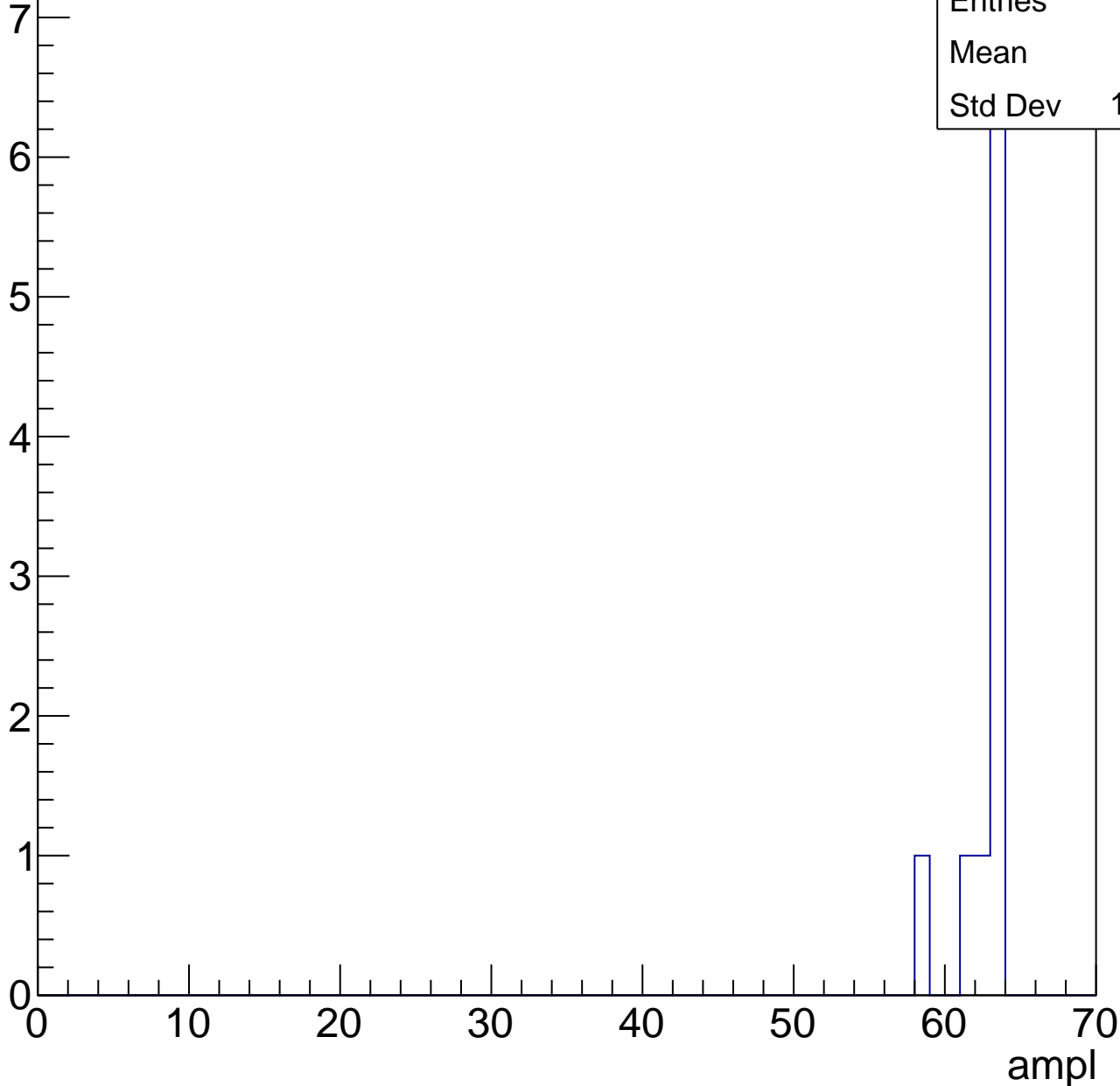


# B1L003S, U3-ch89, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	10
Mean	62.2
Std Dev	1.536

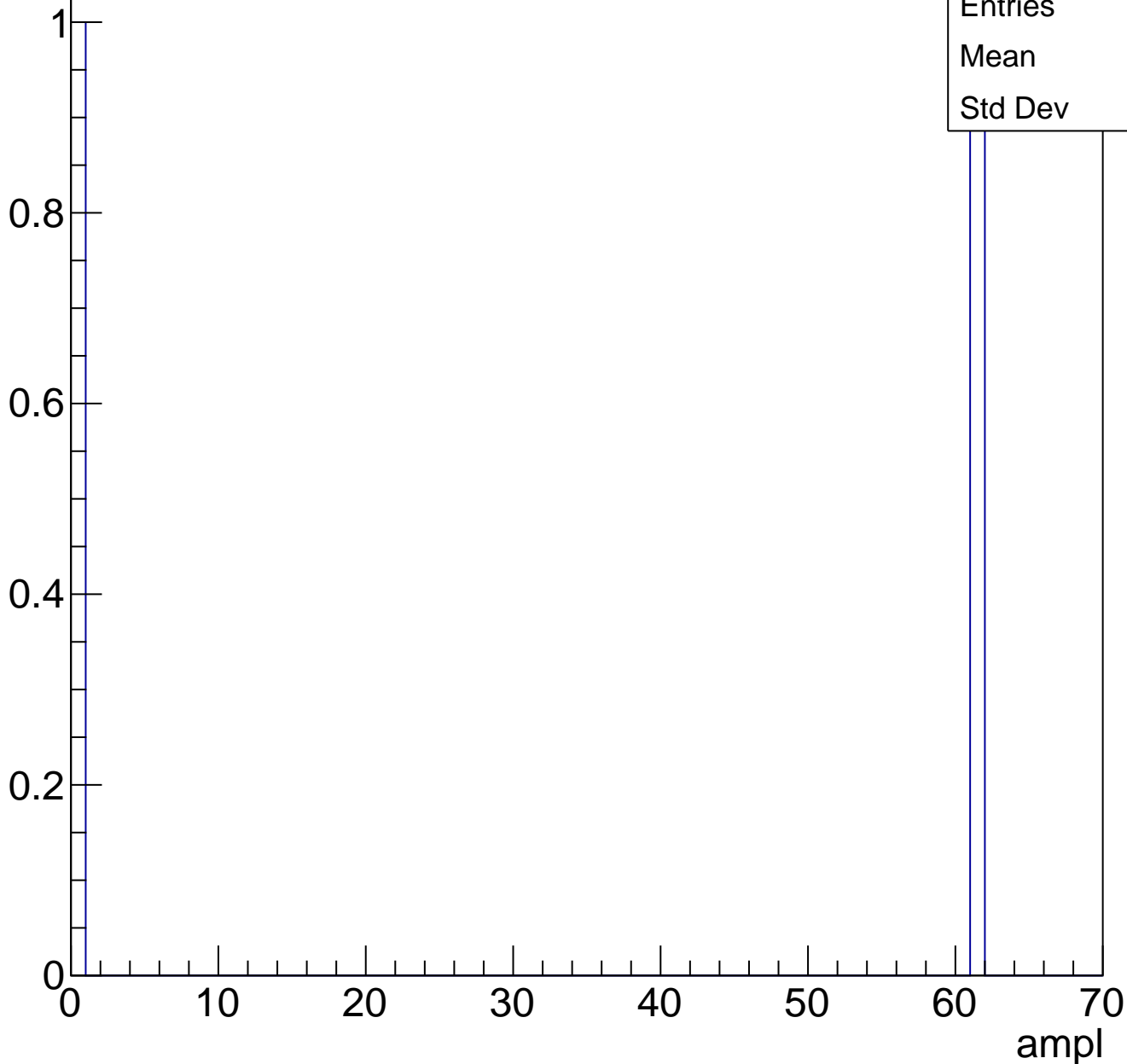




# B1L003S, U3-ch89, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U3-ch90, adc0

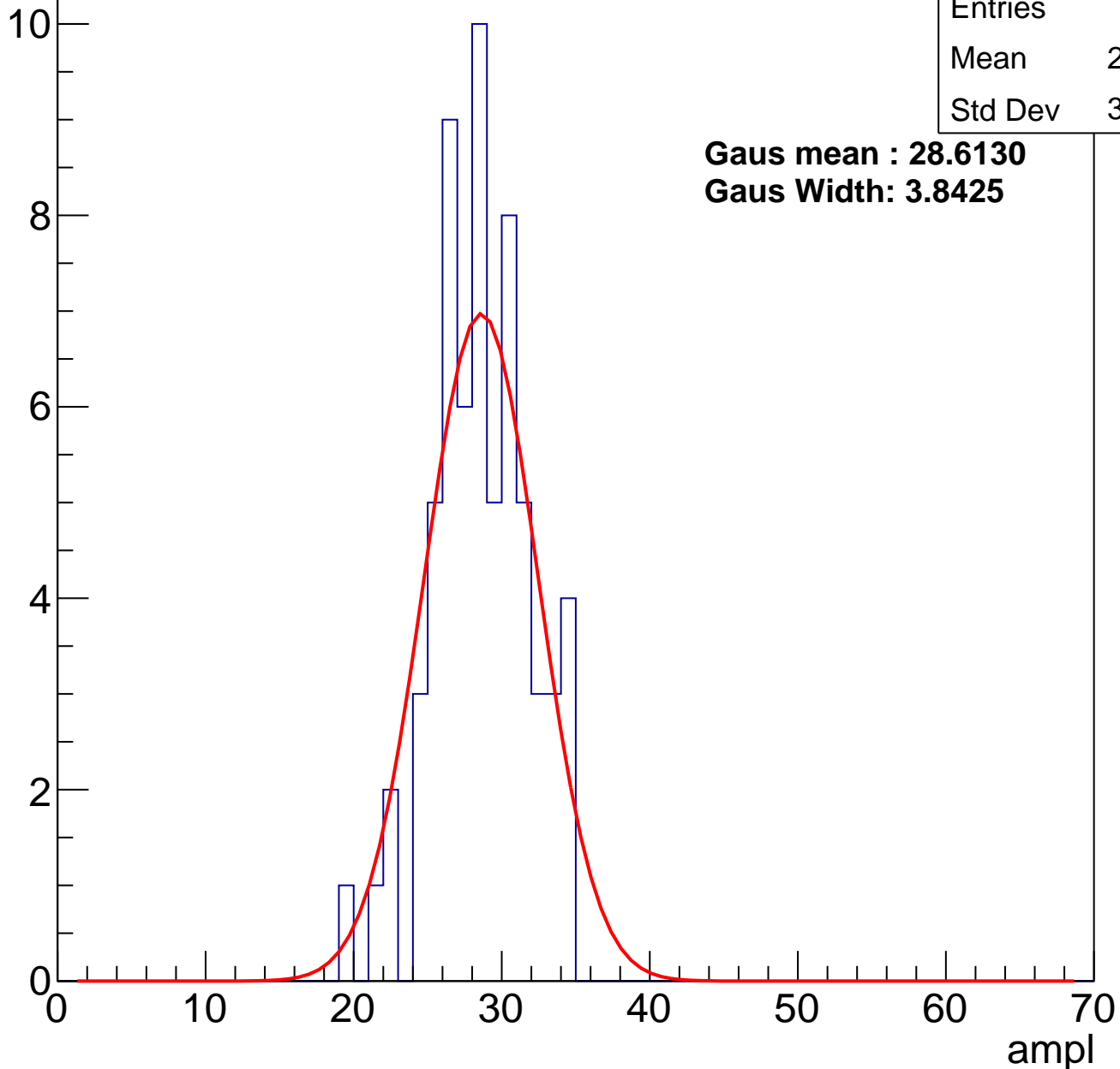
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	65
Mean	28.12
Std Dev	3.246

**Gaus mean : 28.6130**

**Gaus Width: 3.8425**

Entry



# B1L003S, U3-ch90, adc1

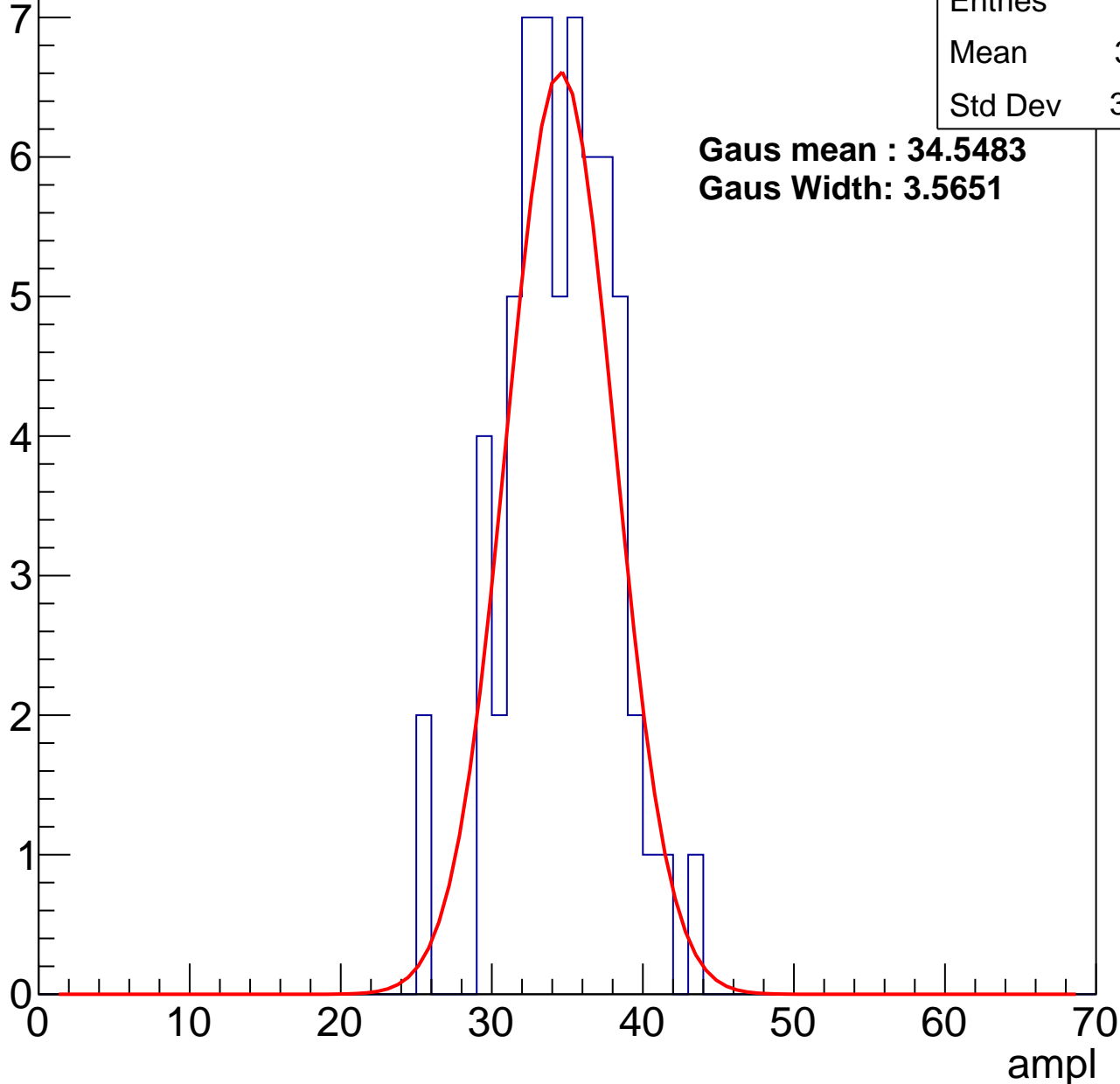
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	34.11
Std Dev	3.516

**Gaus mean : 34.5483**

**Gaus Width: 3.5651**



# B1L003S, U3-ch90, adc2

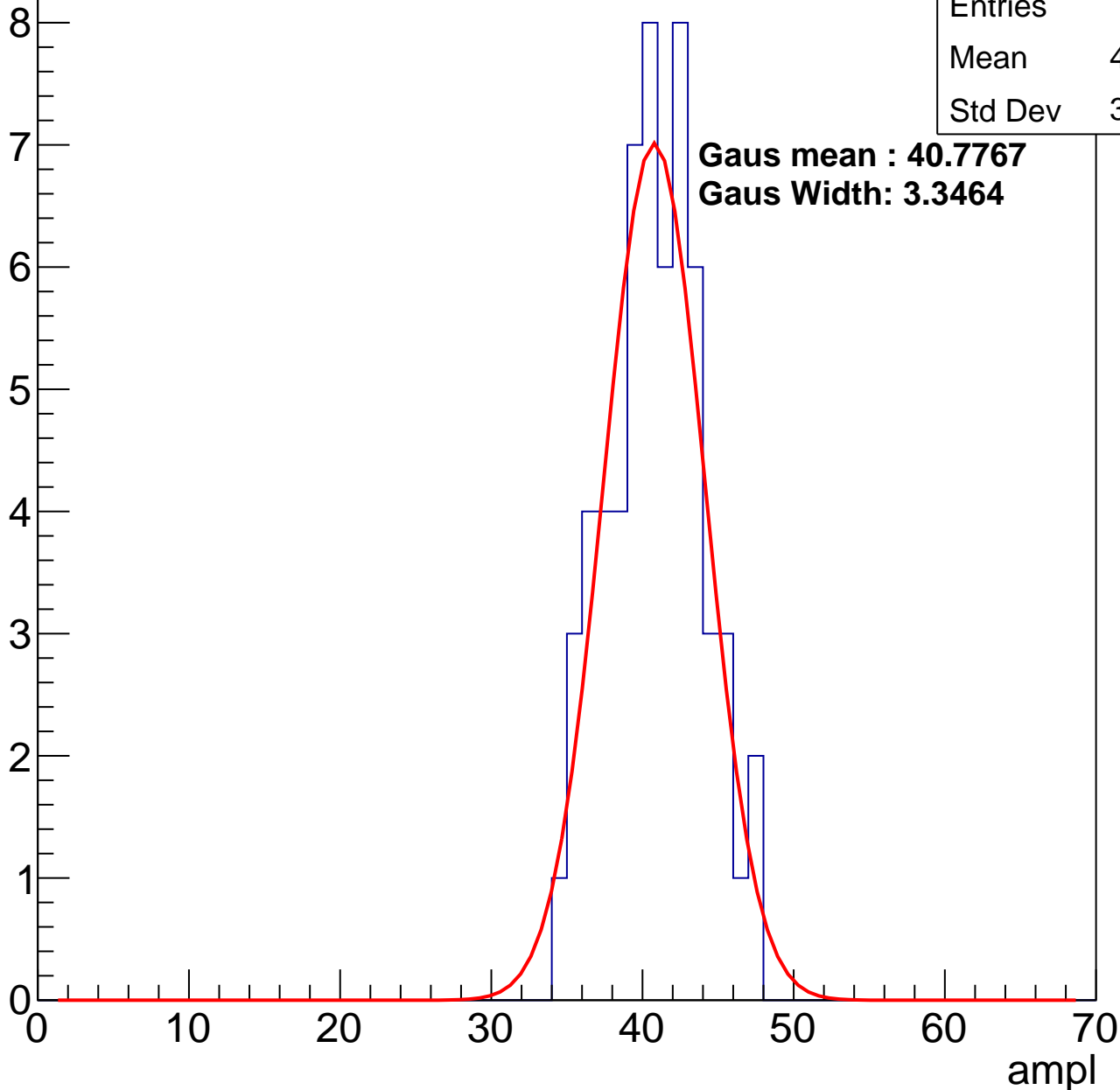
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	40.38
Std Dev	3.093

**Gaus mean : 40.7767**

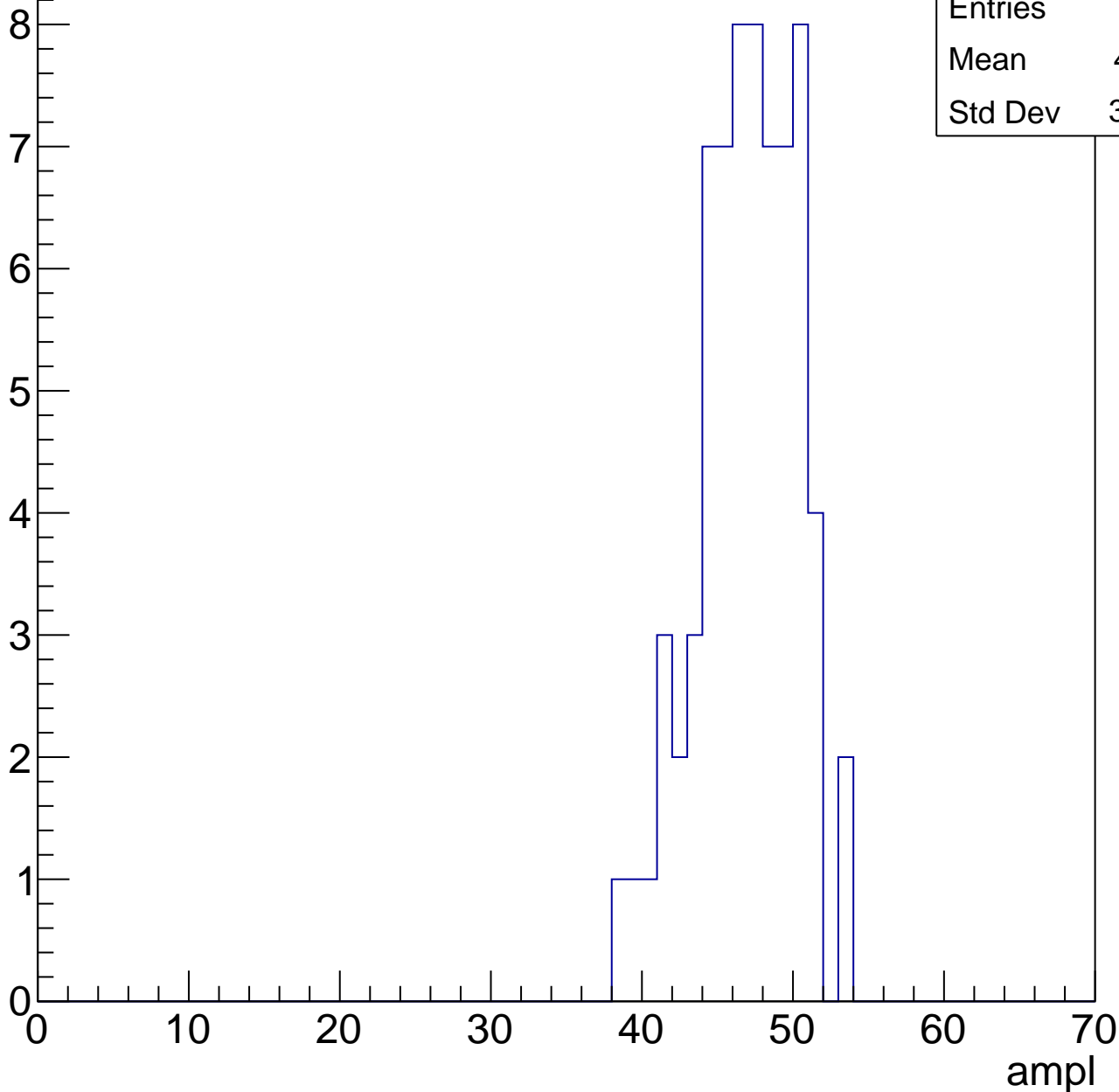
**Gaus Width: 3.3464**



# B1L003S, U3-ch90, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



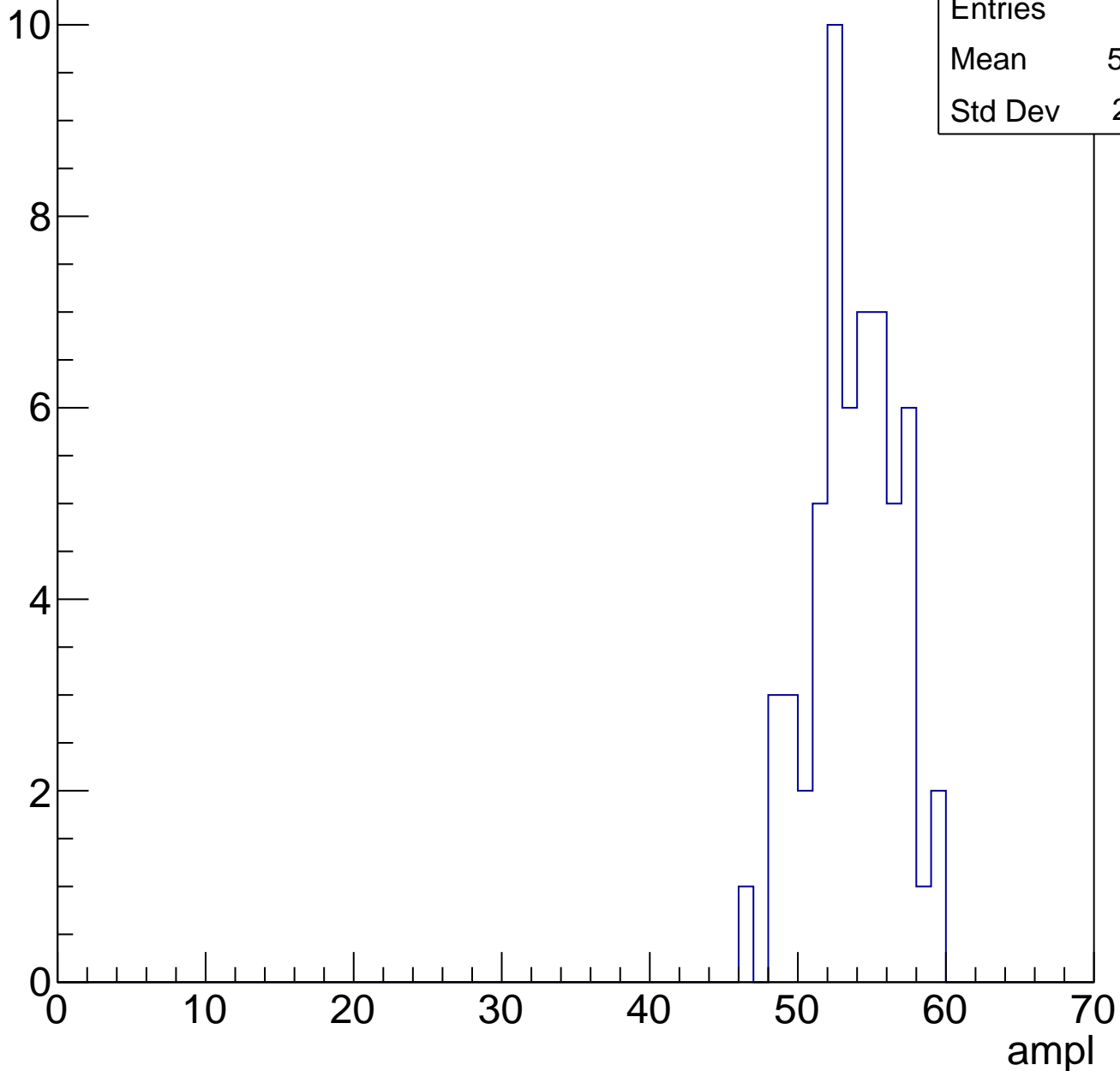
Entries	69
Mean	46.51
Std Dev	3.242

# B1L003S, U3-ch90, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	58
Mean	53.29
Std Dev	2.901

Entry

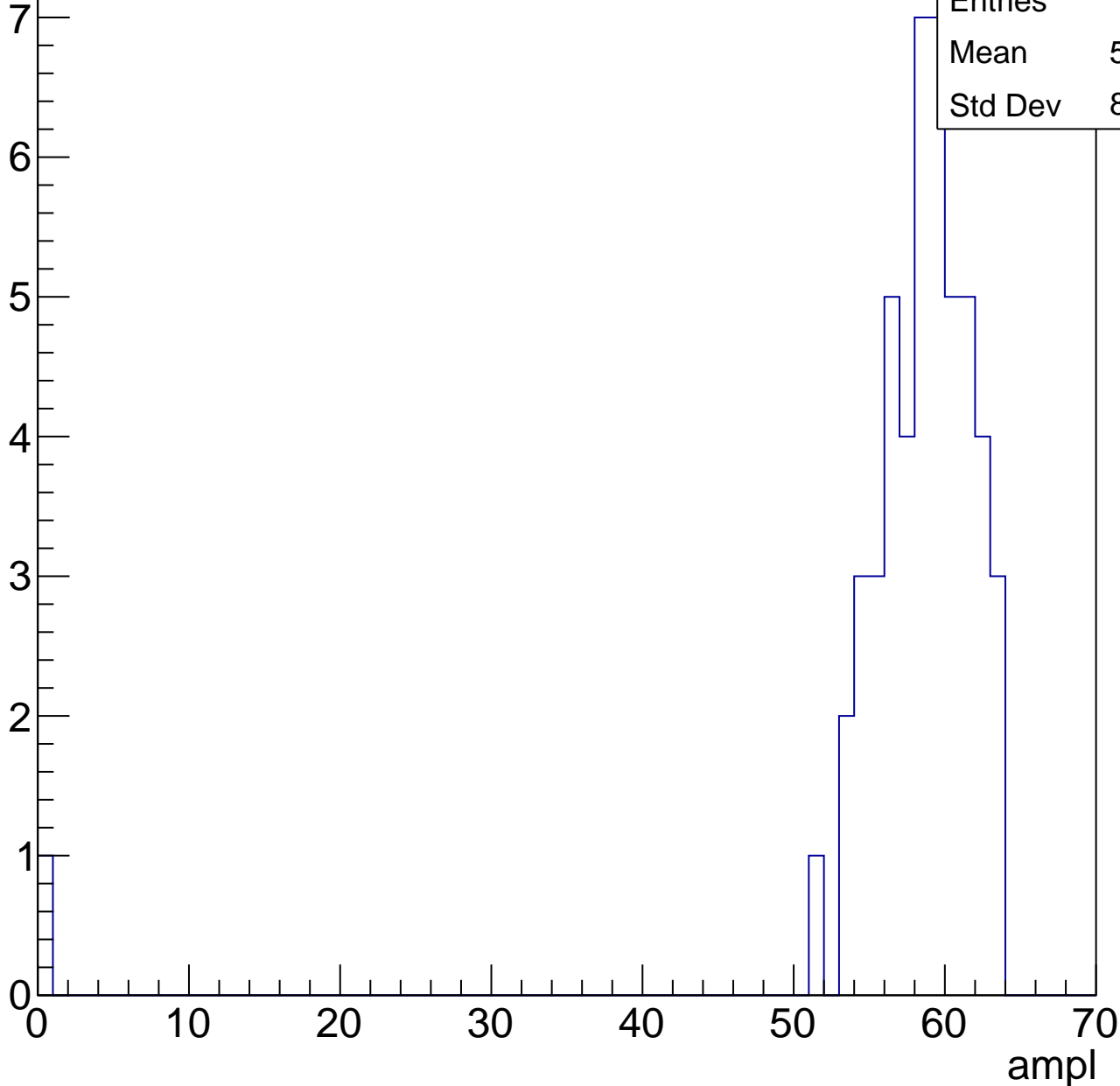


# B1L003S, U3-ch90, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

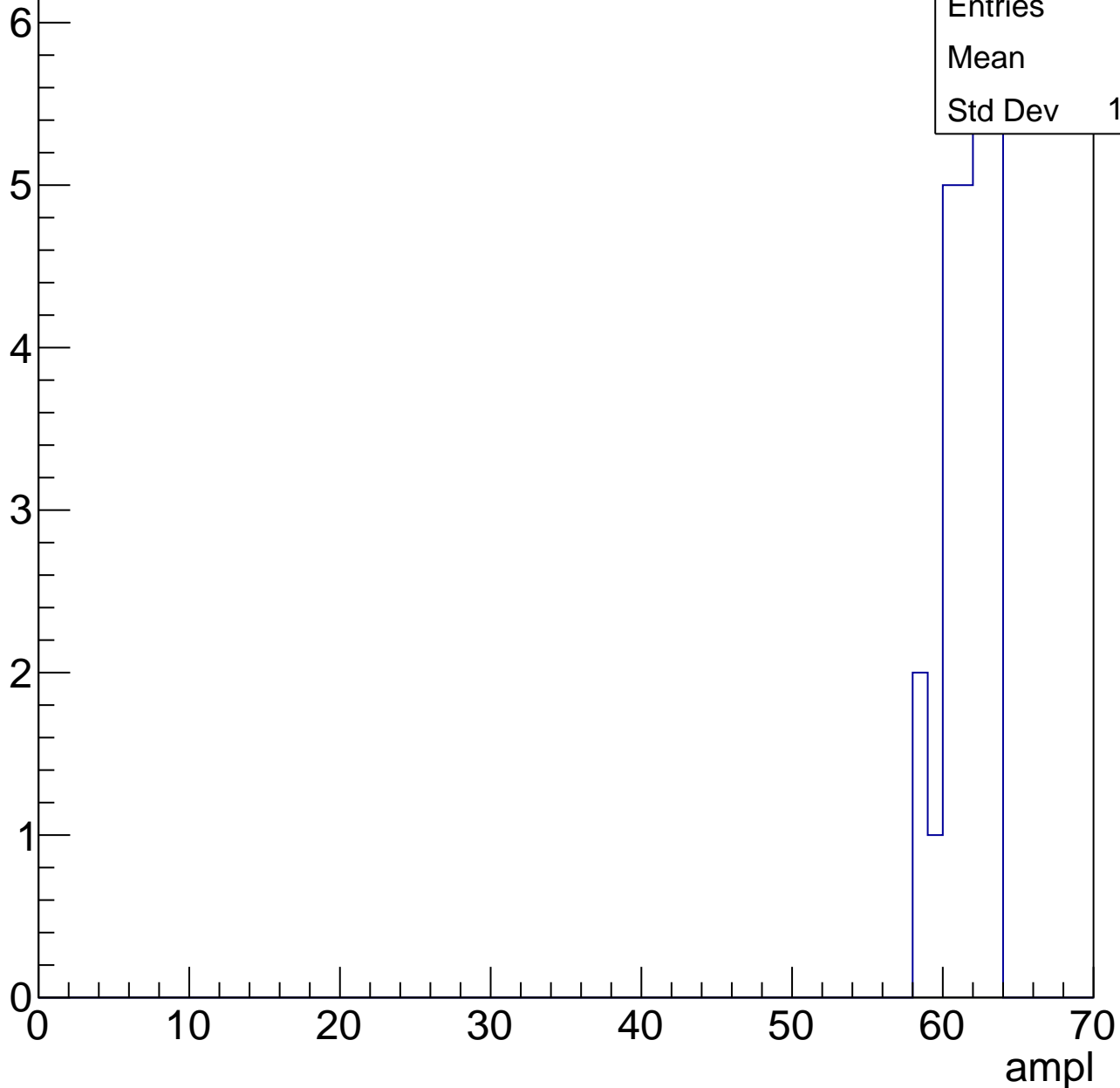
Entries	50
Mean	57.06
Std Dev	8.636



# B1L003S, U3-ch90, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch90, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U3-ch91, adc0

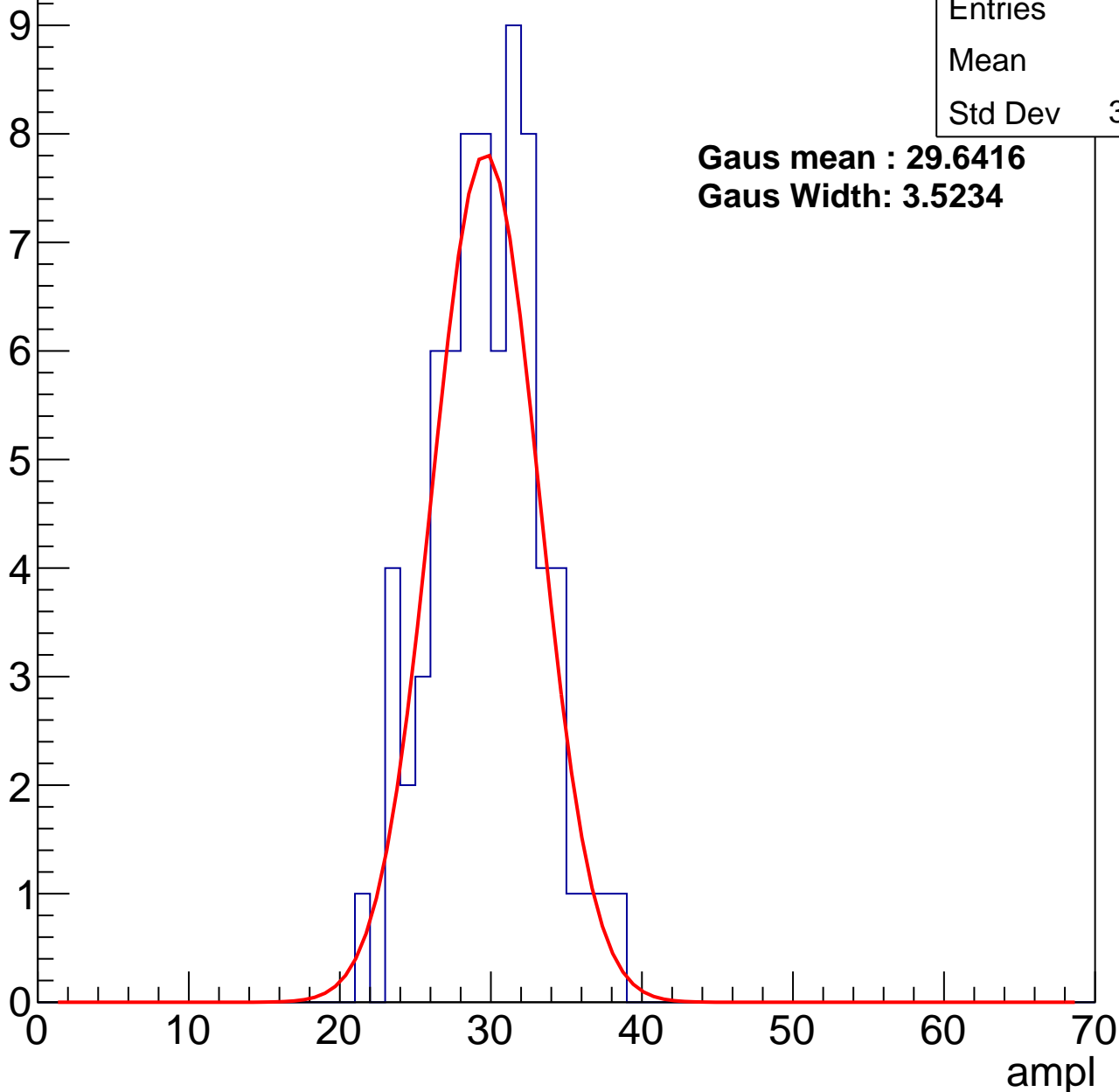
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	73
Mean	29.3
Std Dev	3.498

**Gaus mean : 29.6416**

**Gaus Width: 3.5234**



# B1L003S, U3-ch91, adc1

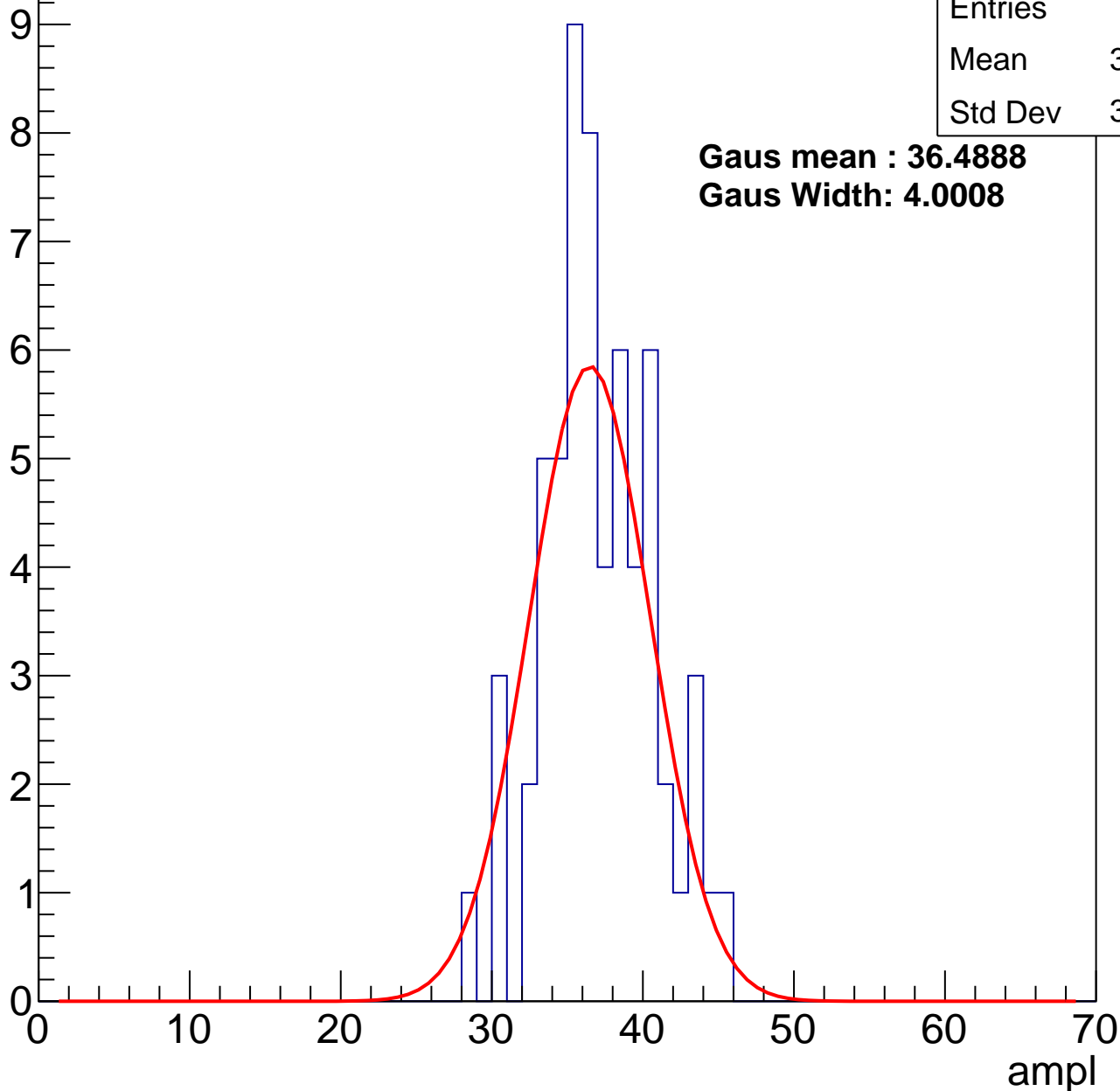
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	36.62
Std Dev	3.604

**Gaus mean : 36.4888**

**Gaus Width: 4.0008**



# B1L003S, U3-ch91, adc2

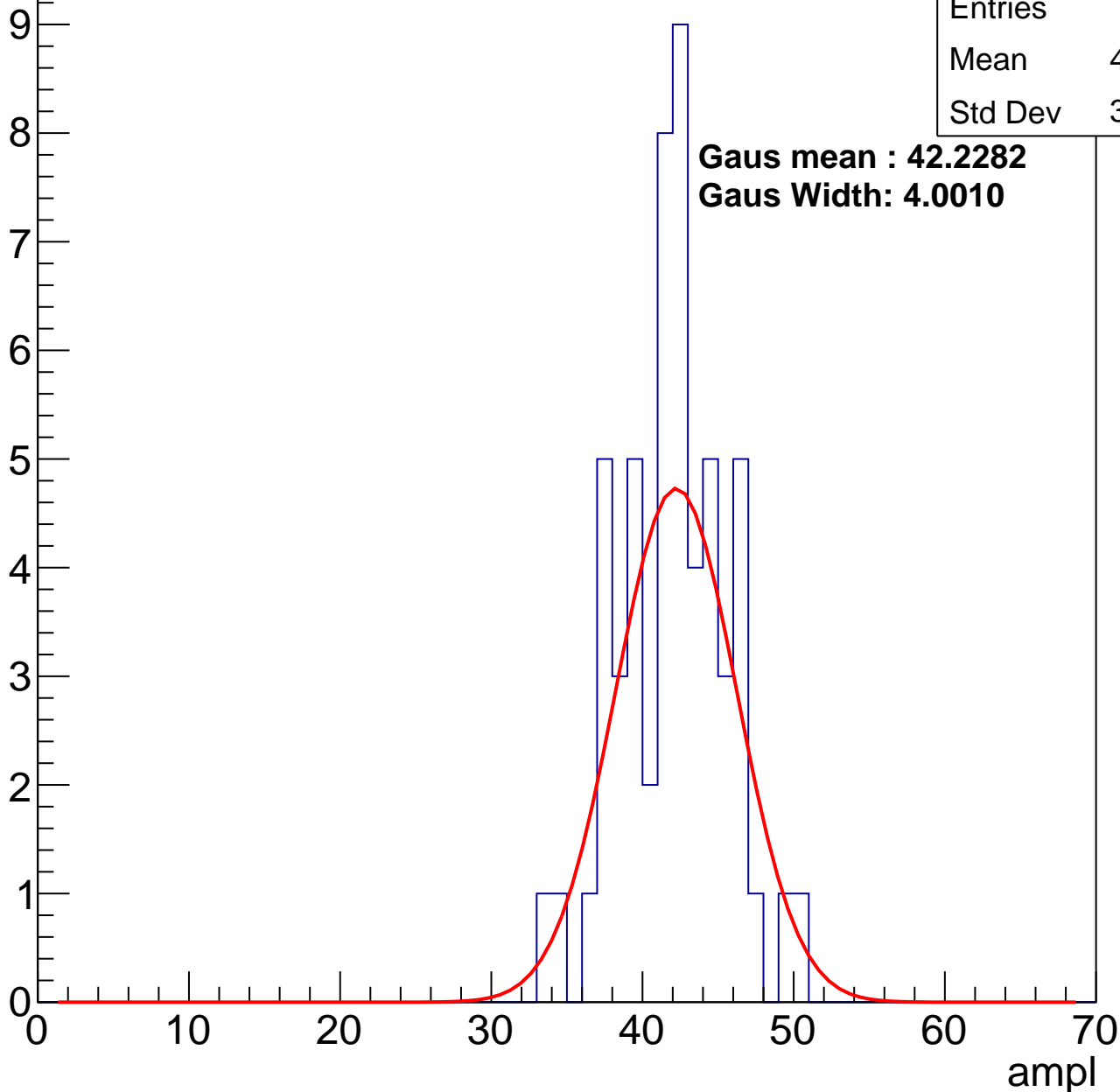
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	41.56
Std Dev	3.499

**Gaus mean : 42.2282**

**Gaus Width: 4.0010**

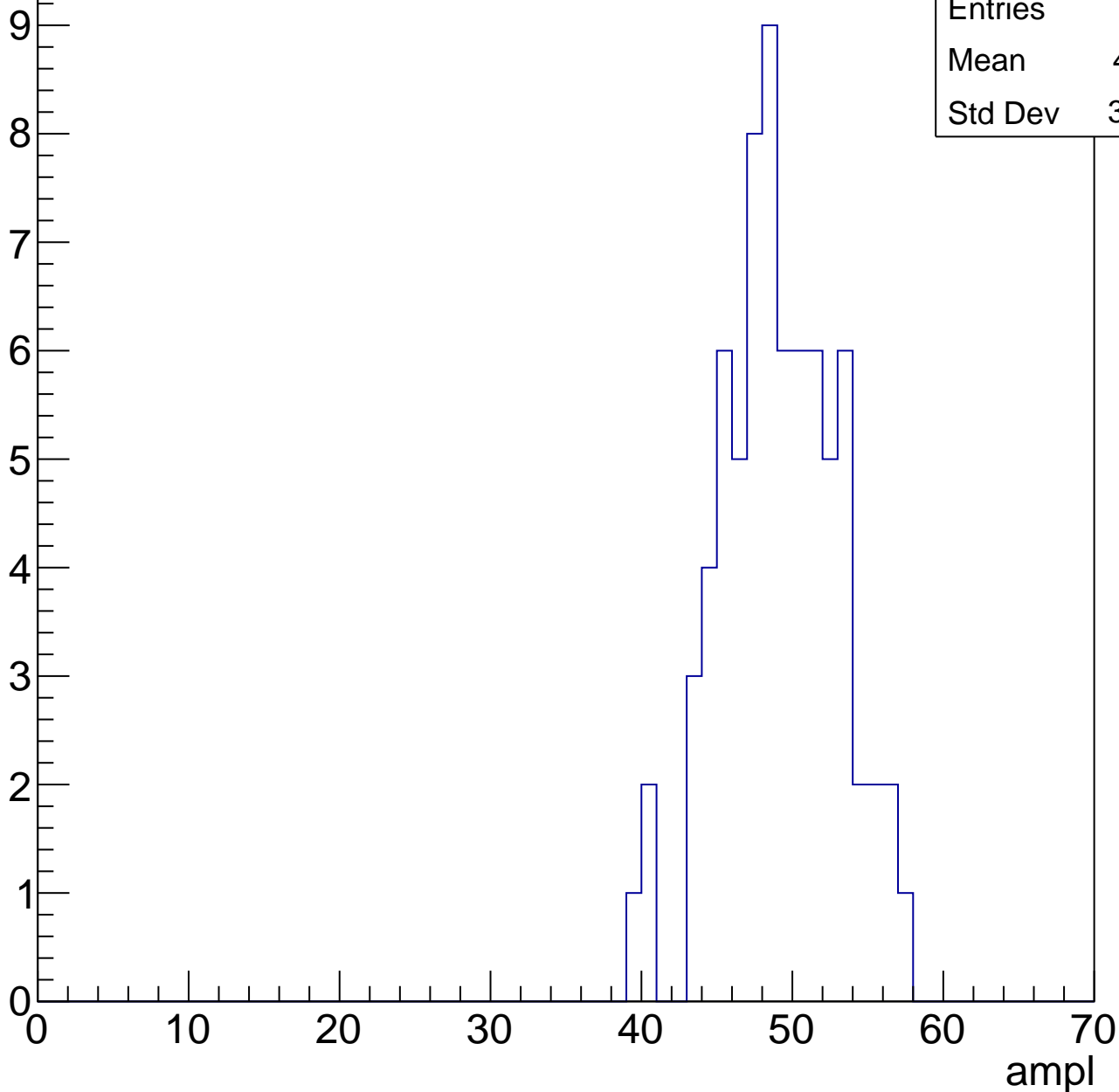


# B1L003S, U3-ch91, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	74
Mean	48.61
Std Dev	3.848

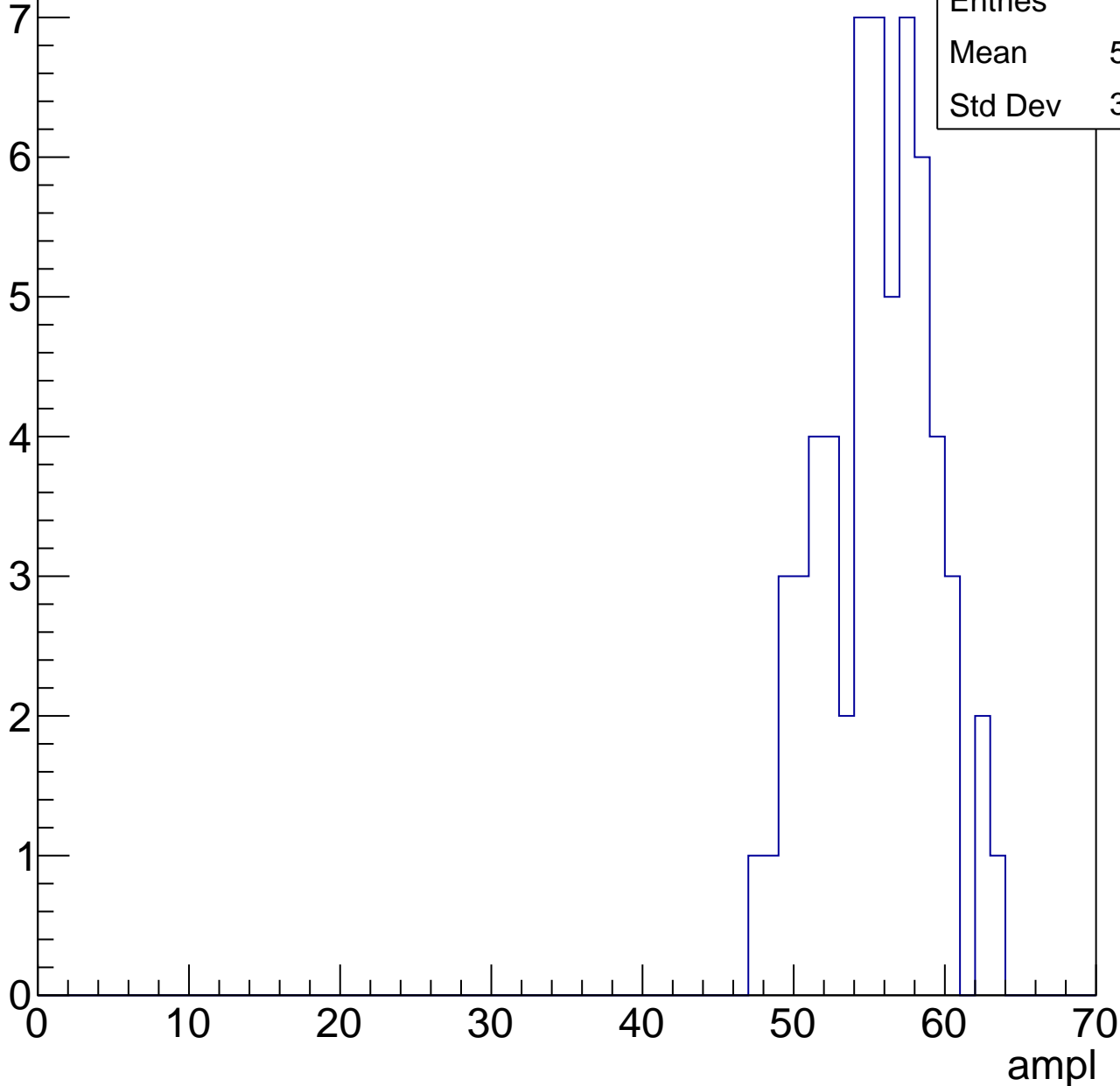


# B1L003S, U3-ch91, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	55.05
Std Dev	3.649

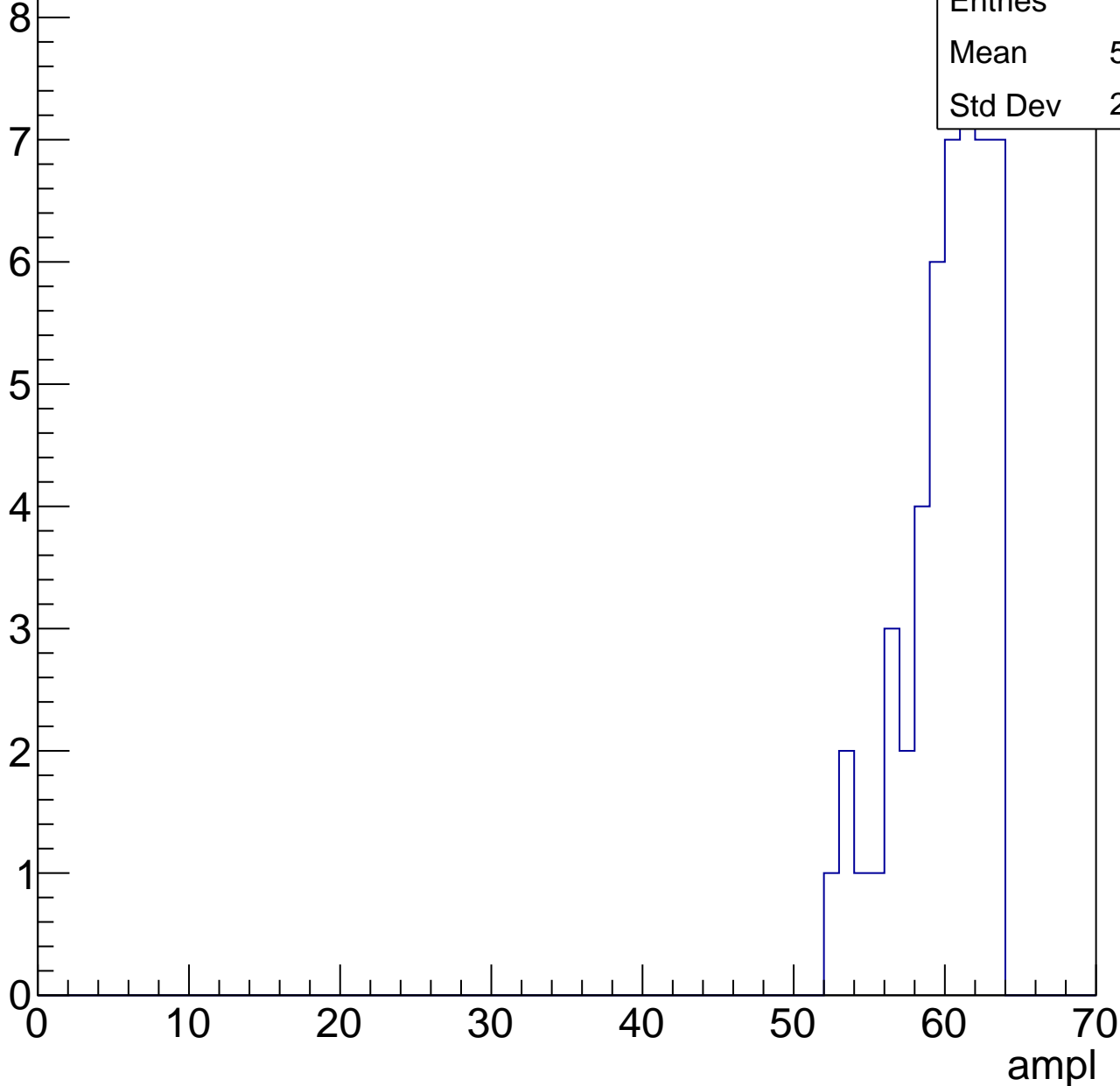


# B1L003S, U3-ch91, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

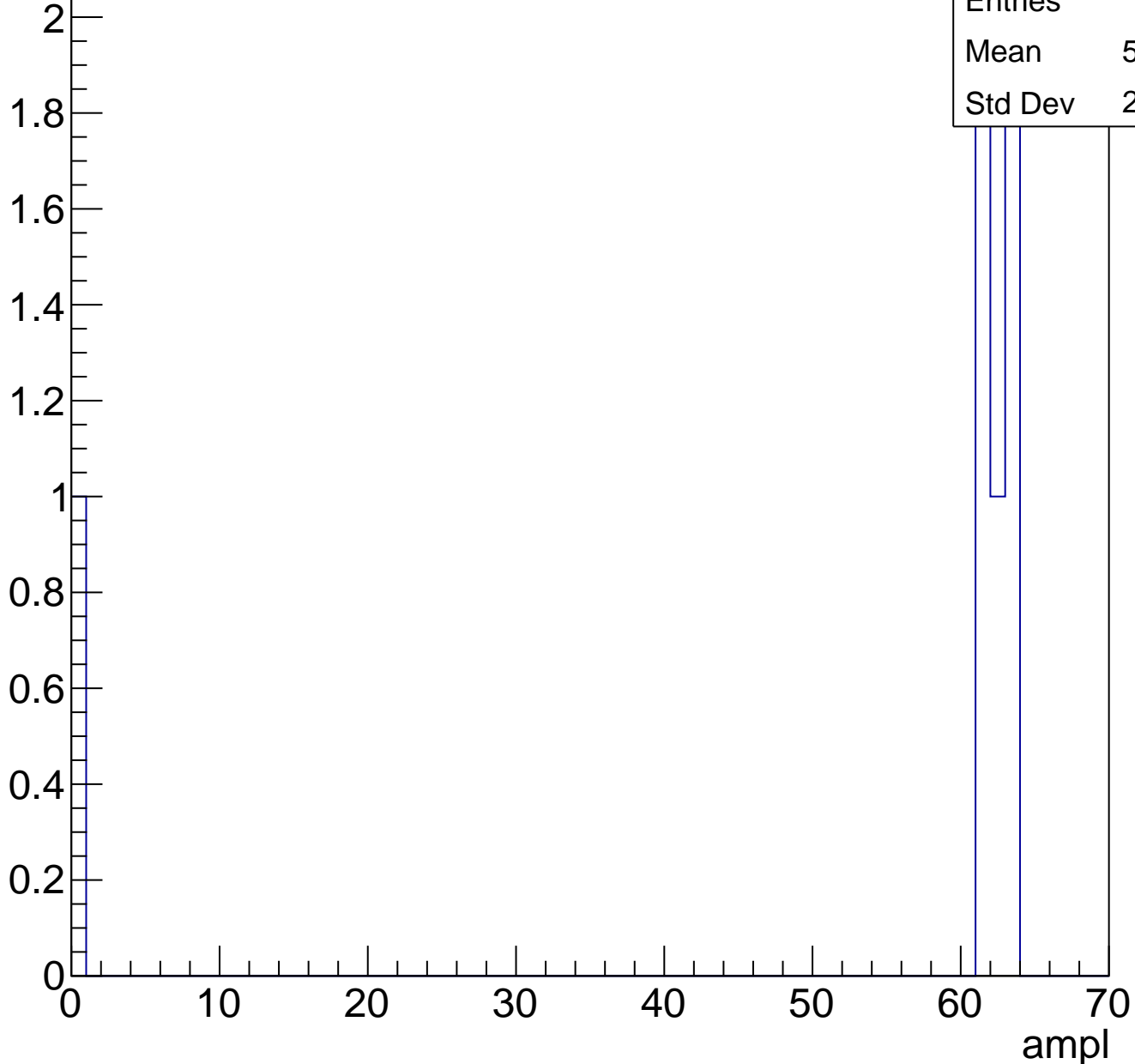
Entries	49
Mean	59.55
Std Dev	2.858



# B1L003S, U3-ch91, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	6
Mean	51.67
Std Dev	23.12



# B1L003S, U3-ch91, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U3-ch92, adc0

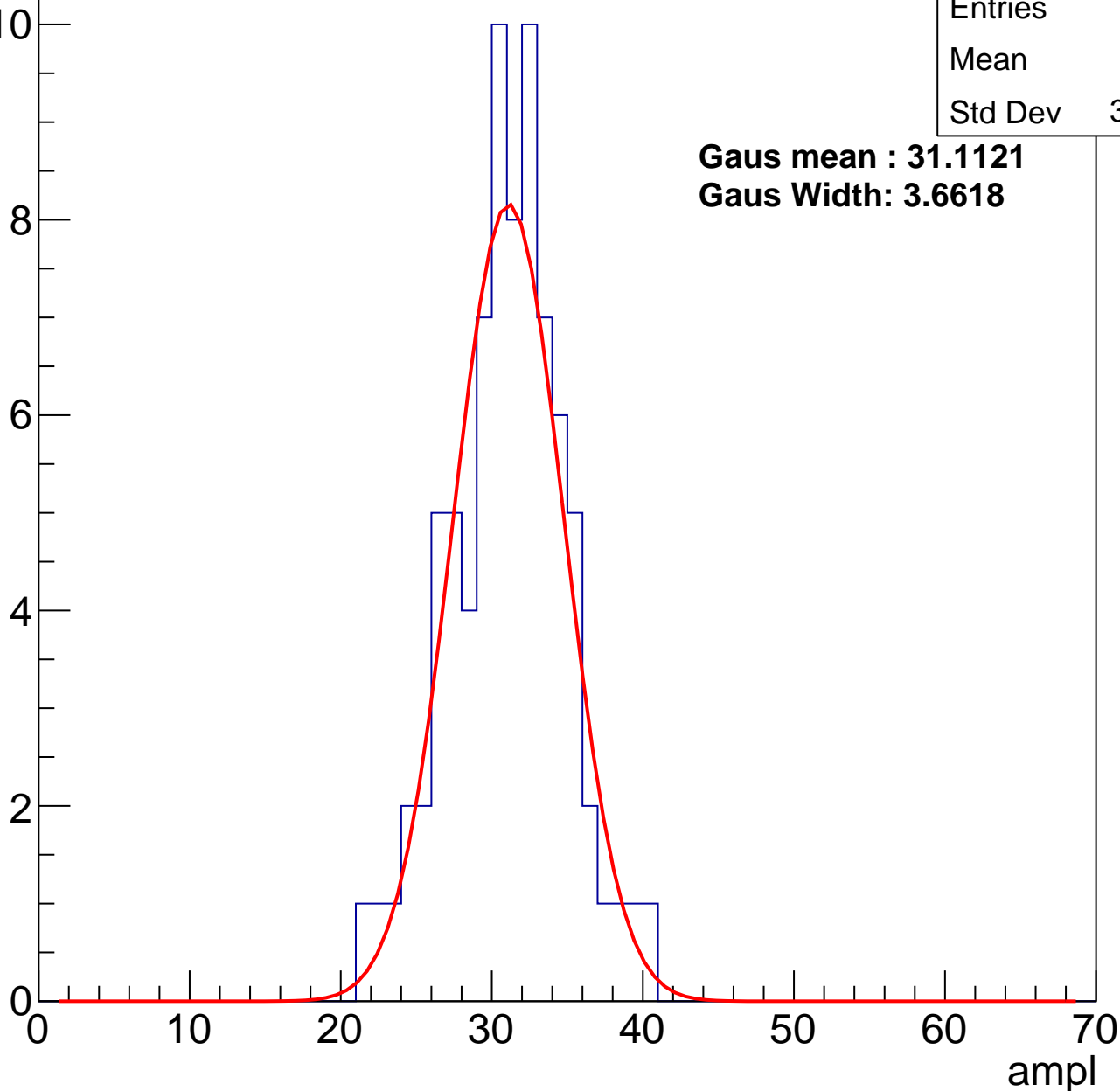
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	80
Mean	30.6
Std Dev	3.764

**Gaus mean : 31.1121**

**Gaus Width: 3.6618**



# B1L003S, U3-ch92, adc1

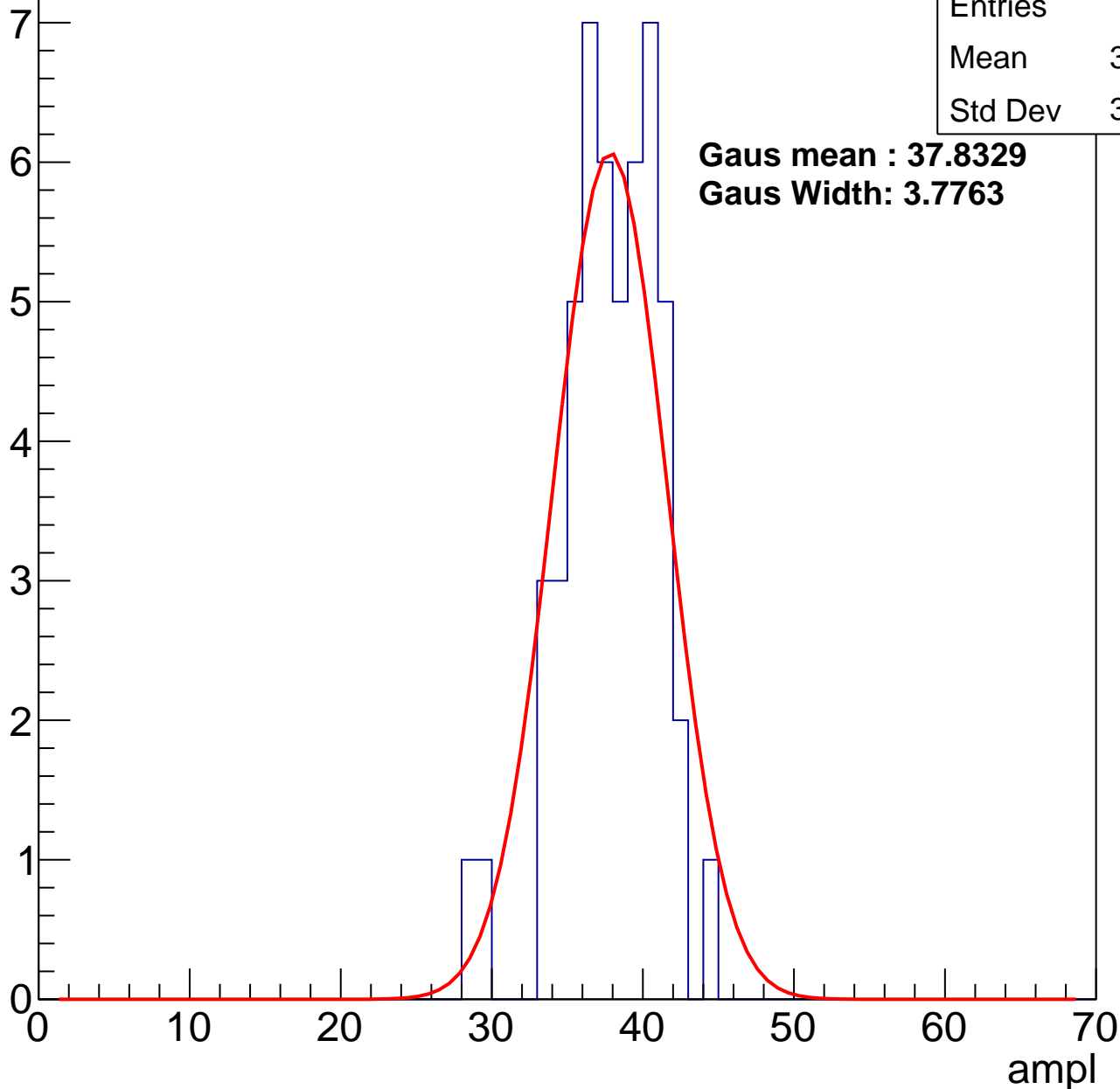
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	52
Mean	37.38
Std Dev	3.133

**Gaus mean : 37.8329**

**Gaus Width: 3.7763**



# B1L003S, U3-ch92, adc2

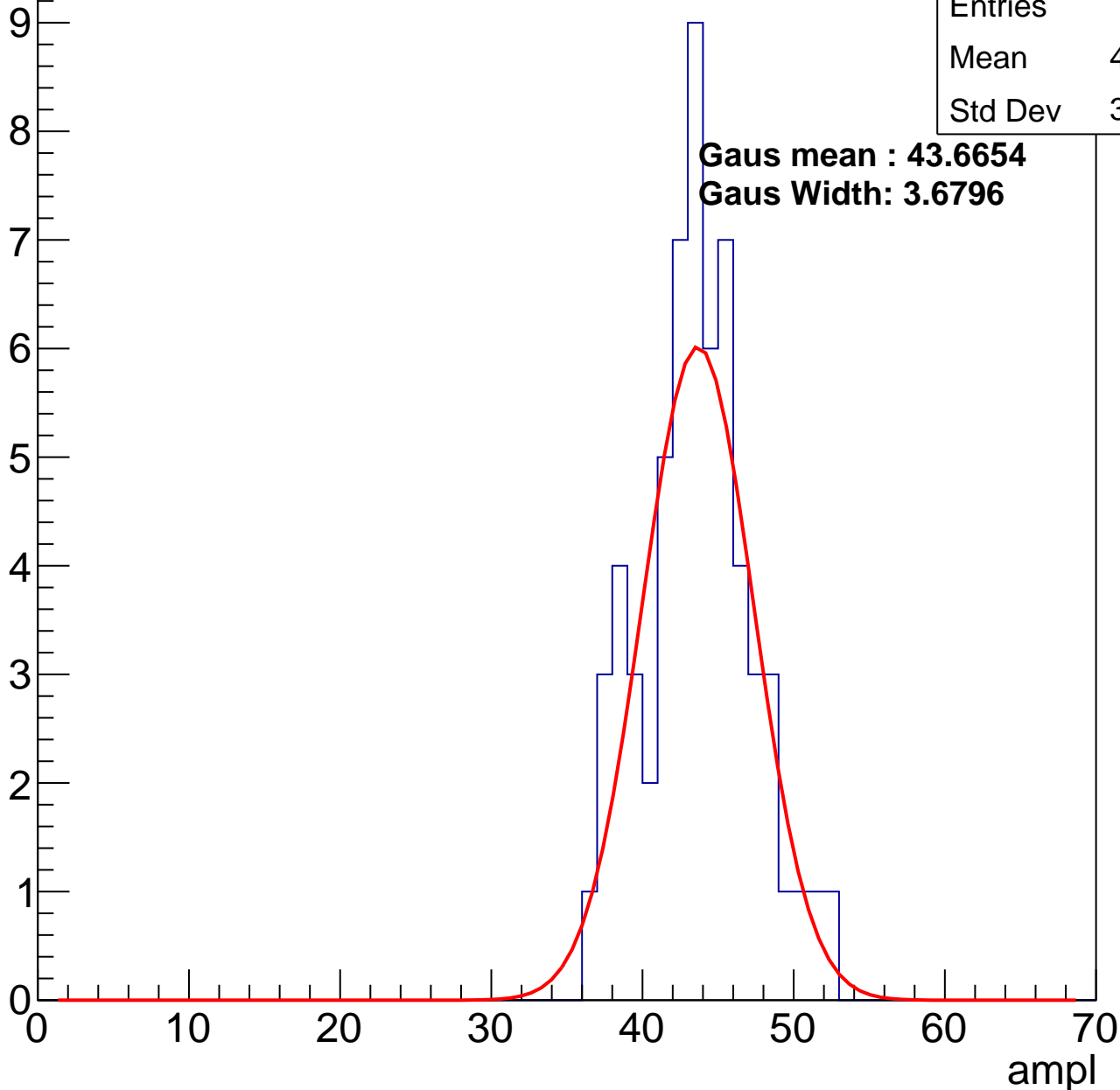
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	43.15
Std Dev	3.557

**Gaus mean : 43.6654**

**Gaus Width: 3.6796**

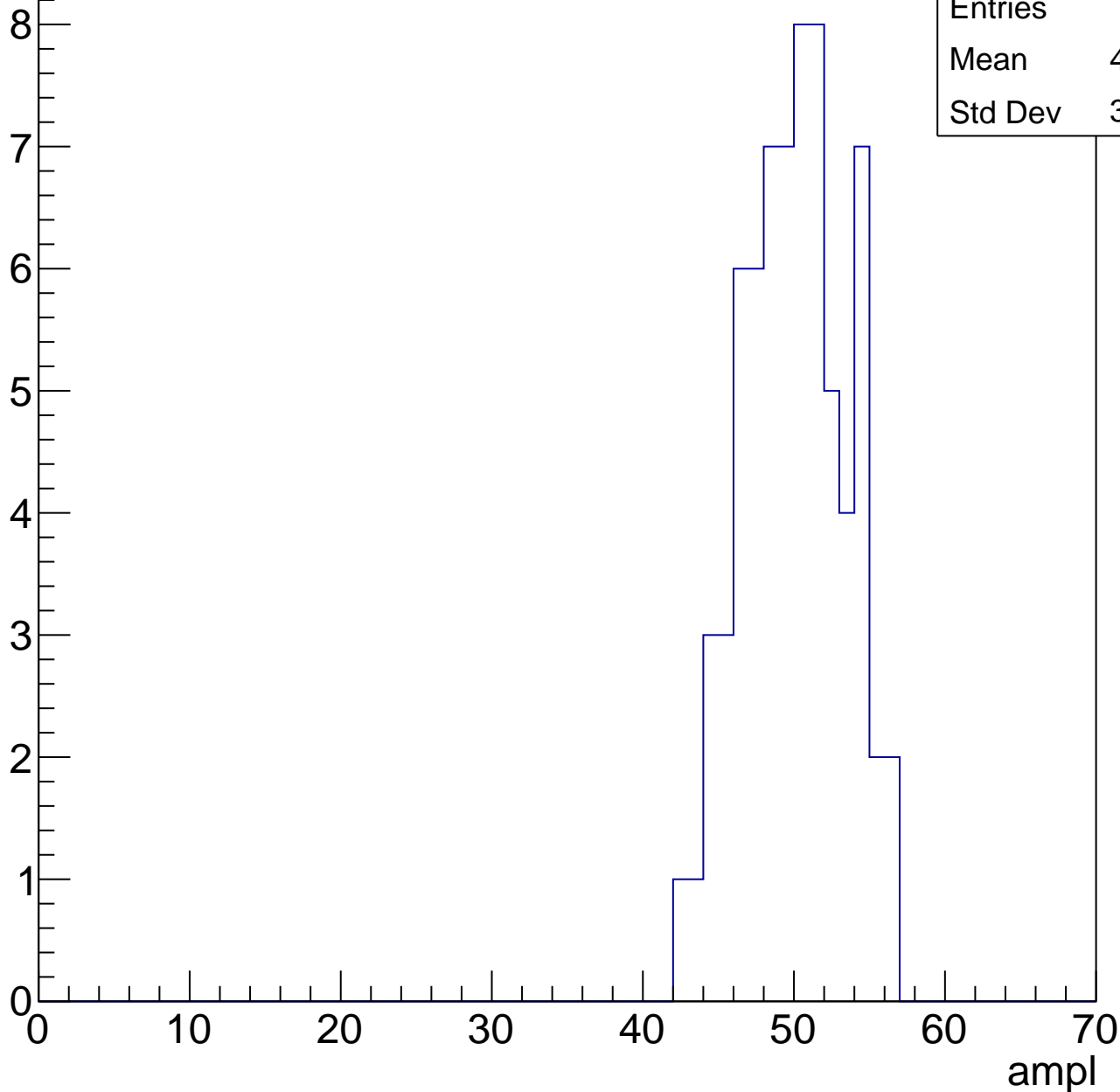


# B1L003S, U3-ch92, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	49.56
Std Dev	3.306

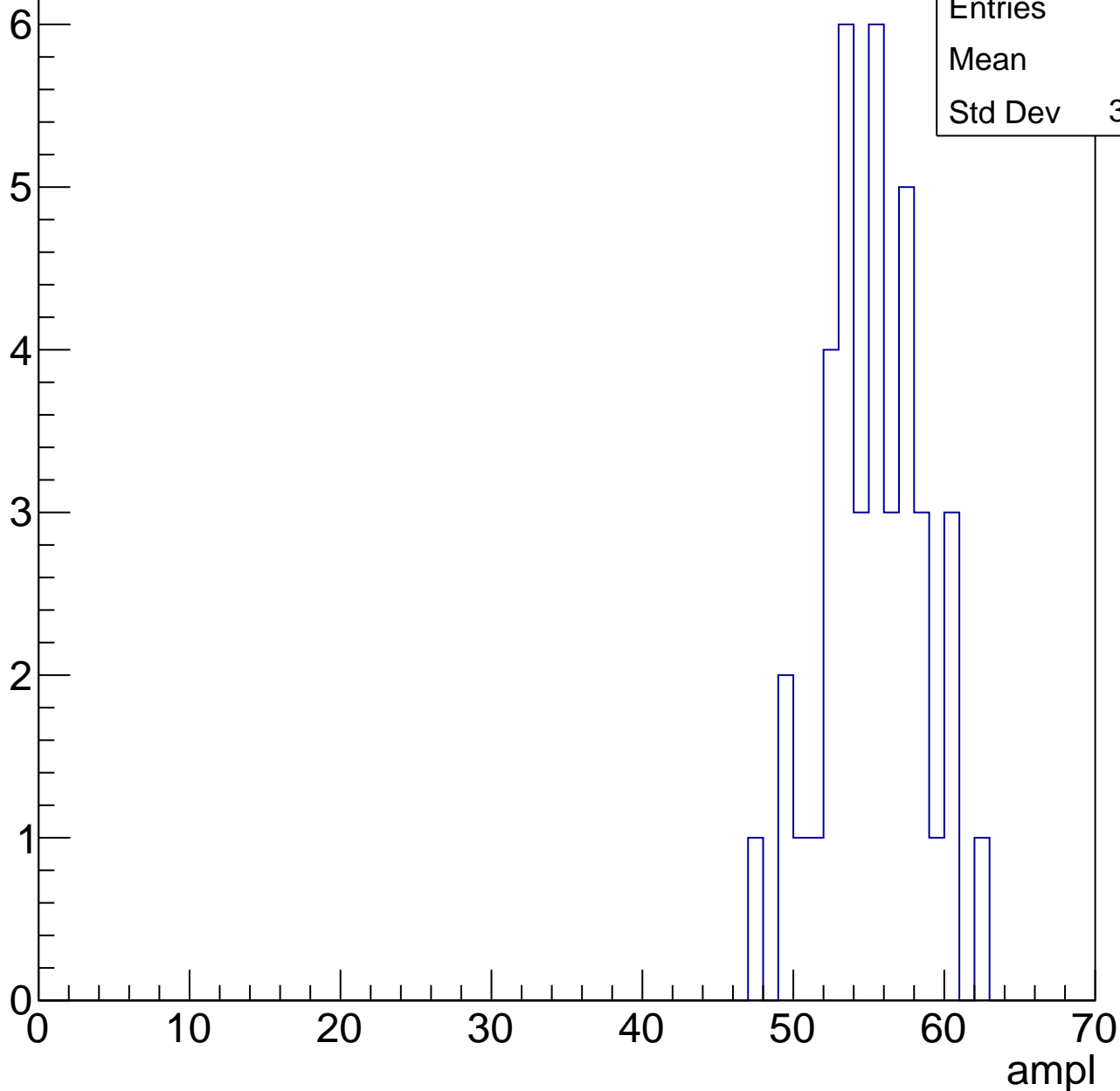


# B1L003S, U3-ch92, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	40
Mean	54.8
Std Dev	3.273

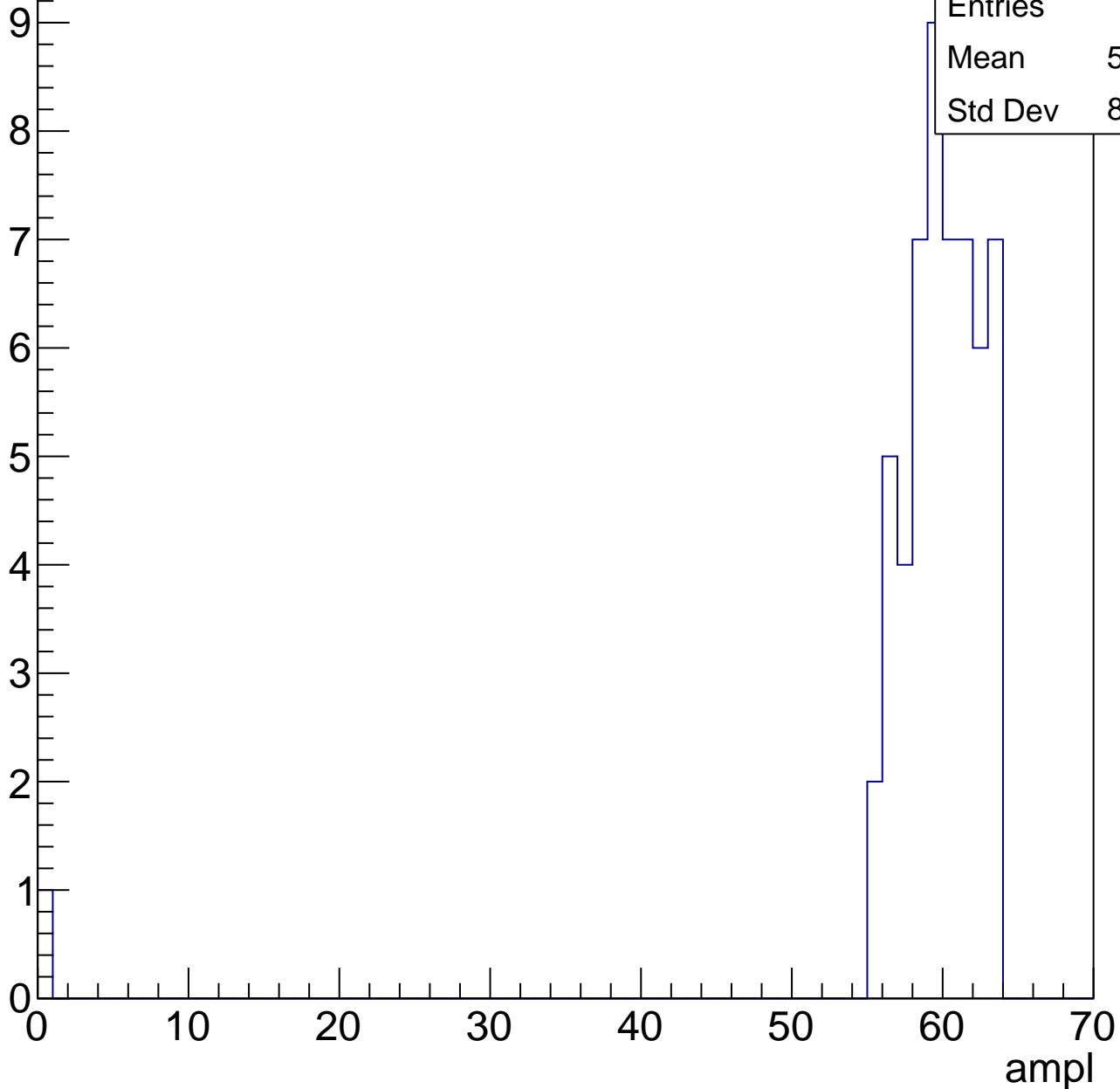


# B1L003S, U3-ch92, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

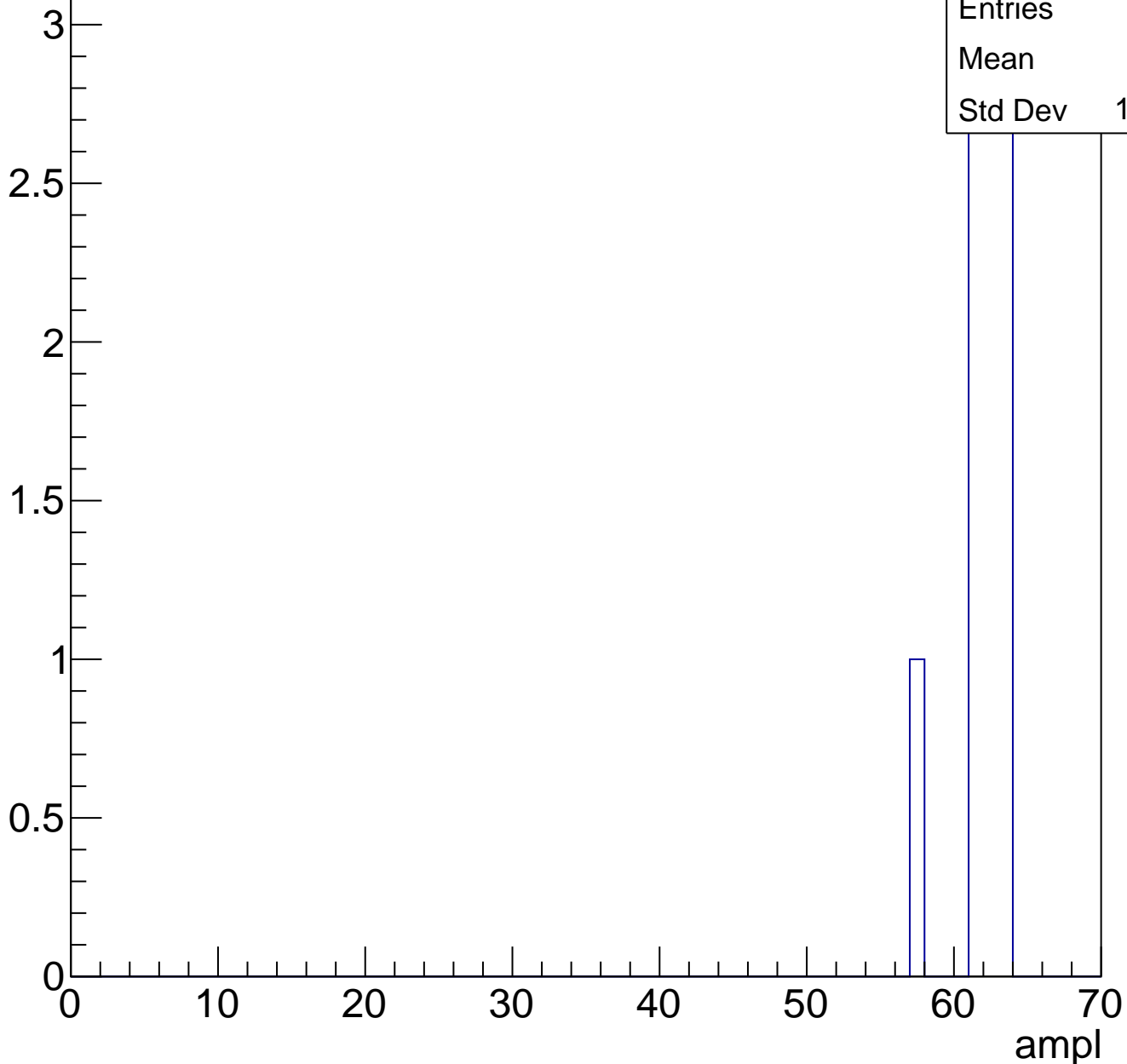
Entries	55
Mean	58.45
Std Dev	8.274



# B1L003S, U3-ch92, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch92, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U3-ch93, adc0

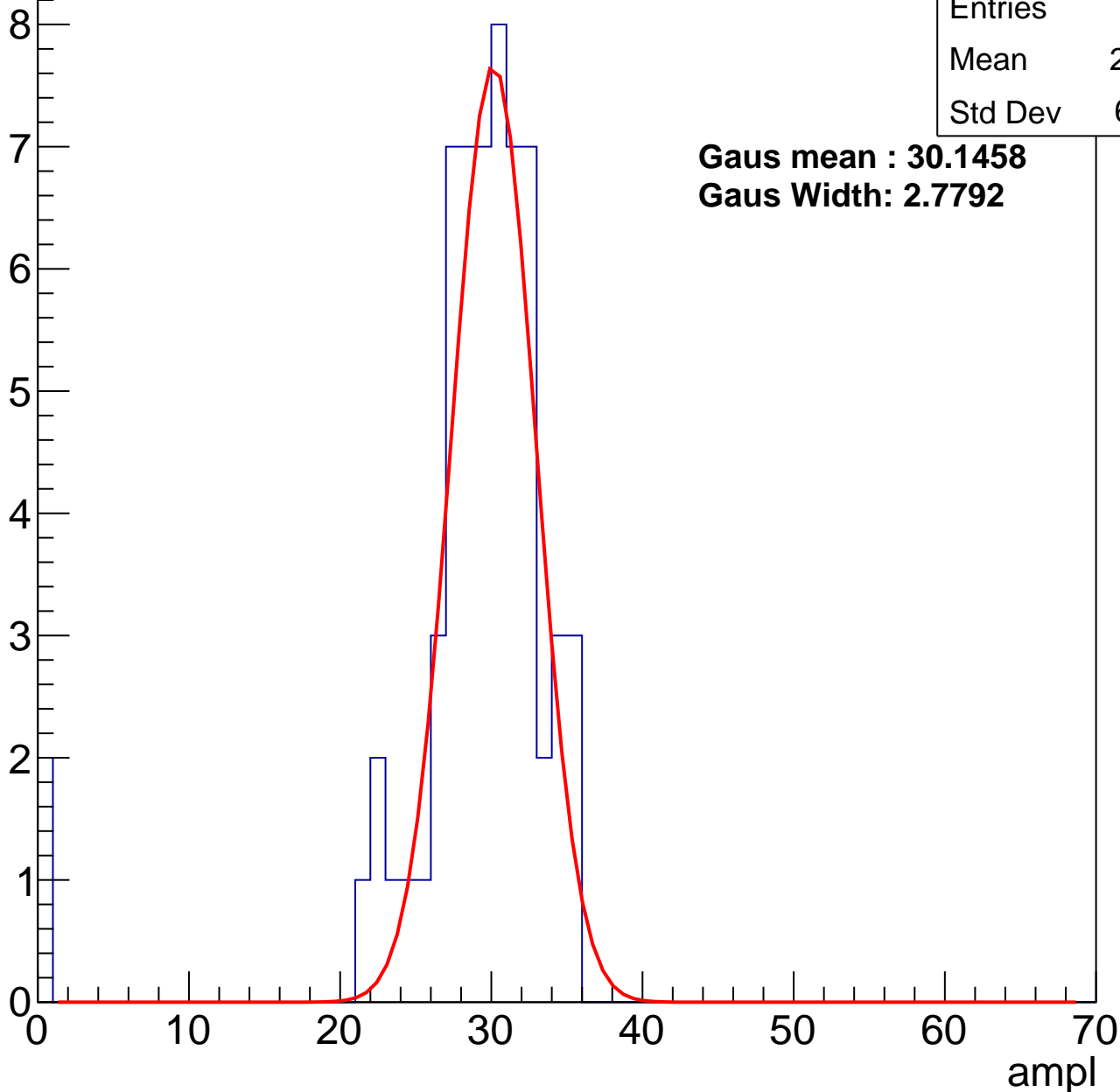
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	28.34
Std Dev	6.051

**Gaus mean : 30.1458**

**Gaus Width: 2.7792**



# B1L003S, U3-ch93, adc1

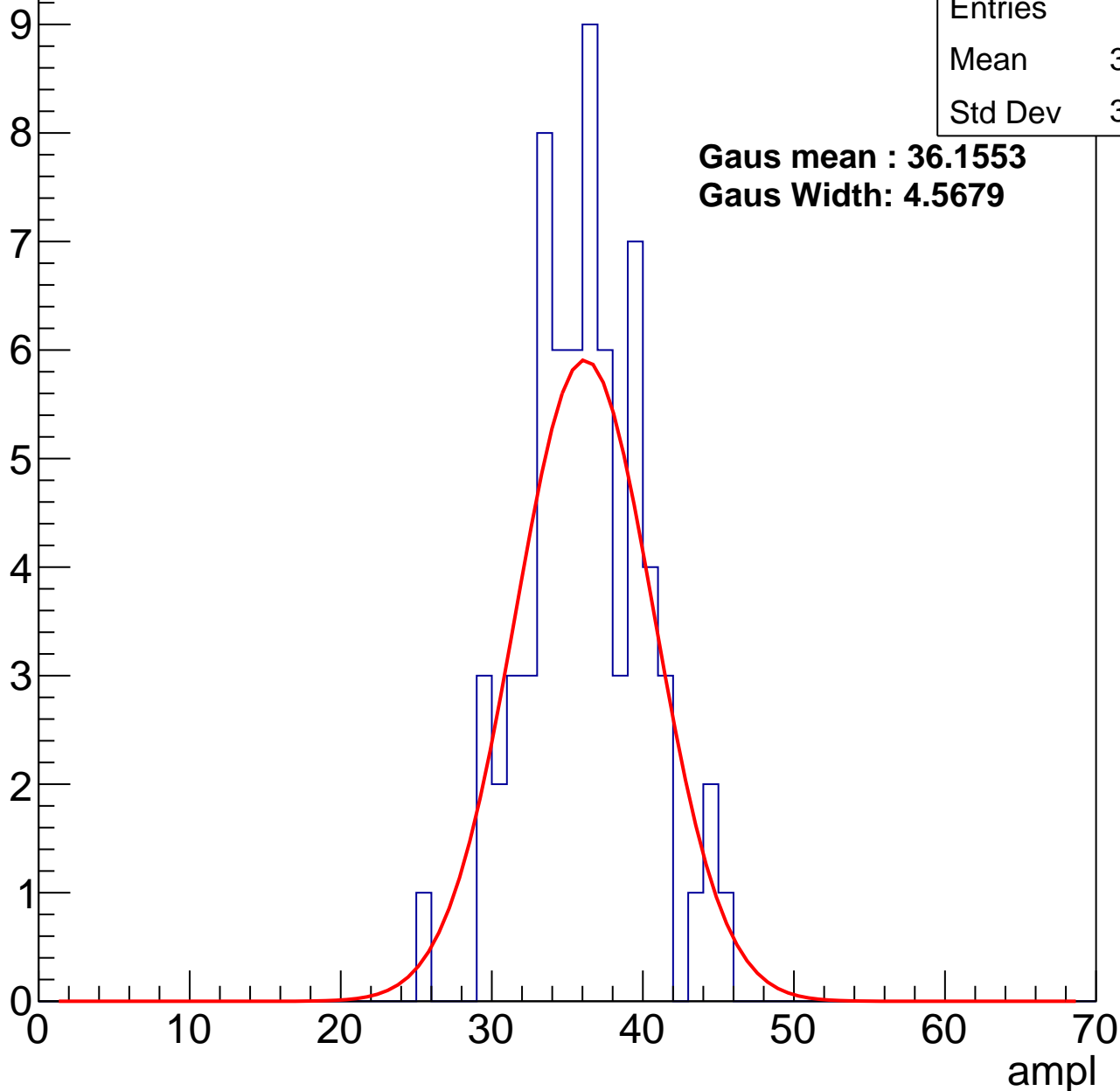
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	35.75
Std Dev	3.908

**Gaus mean : 36.1553**

**Gaus Width: 4.5679**



# B1L003S, U3-ch93, adc2

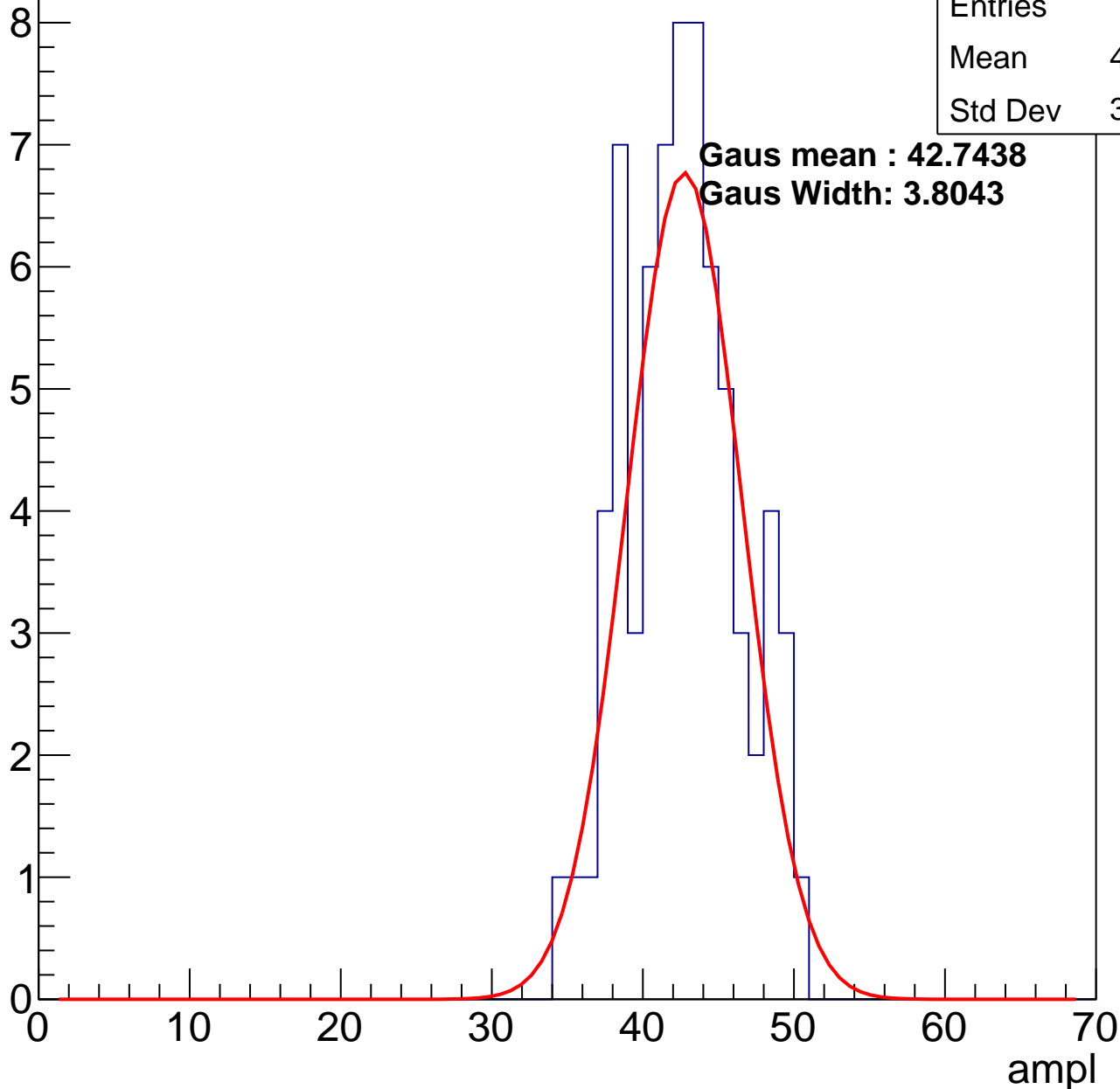
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	42.19
Std Dev	3.677

**Gaus mean : 42.7438**

**Gaus Width: 3.8043**

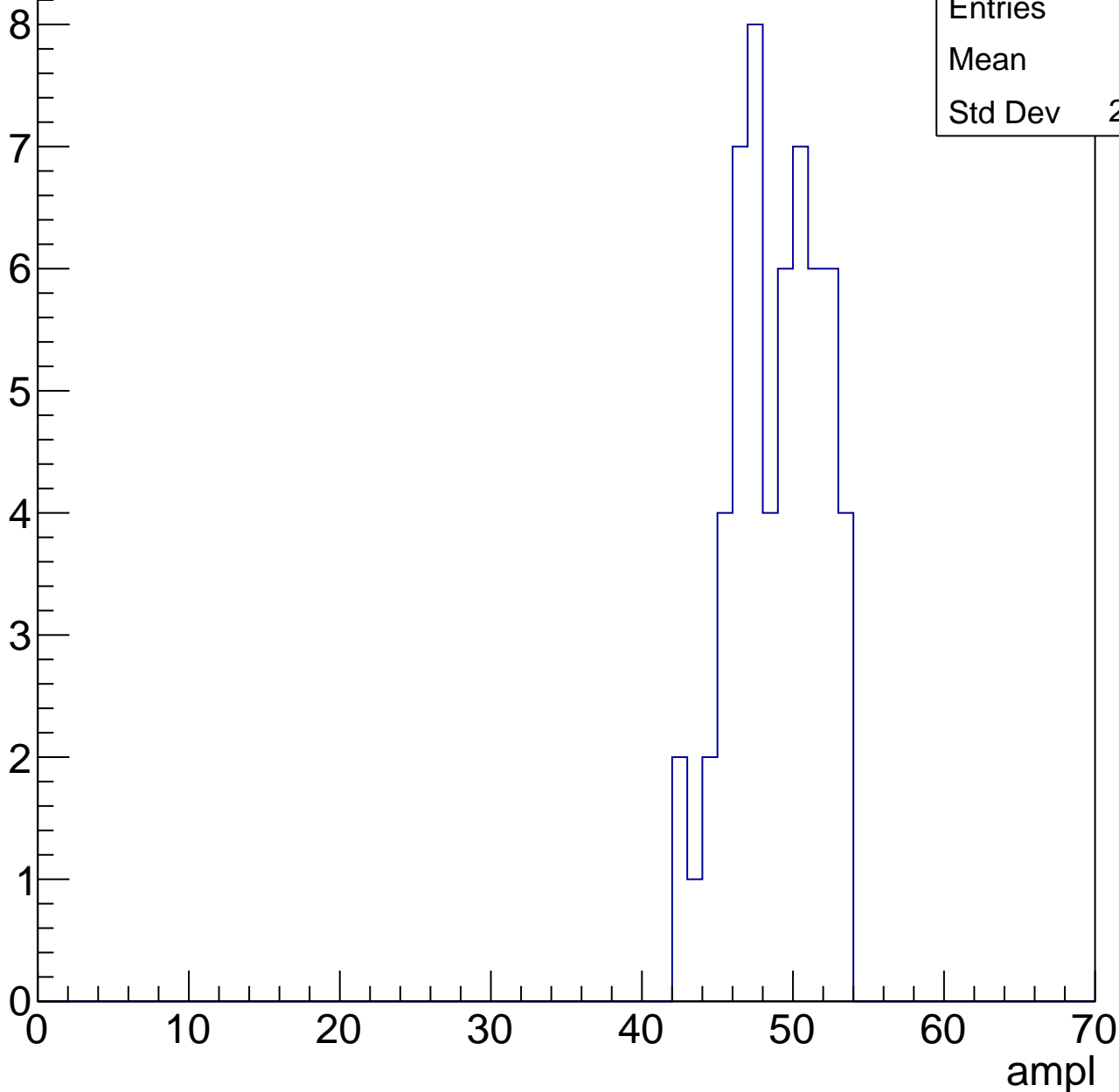


# B1L003S, U3-ch93, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	48.4
Std Dev	2.889



# B1L003S, U3-ch93, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

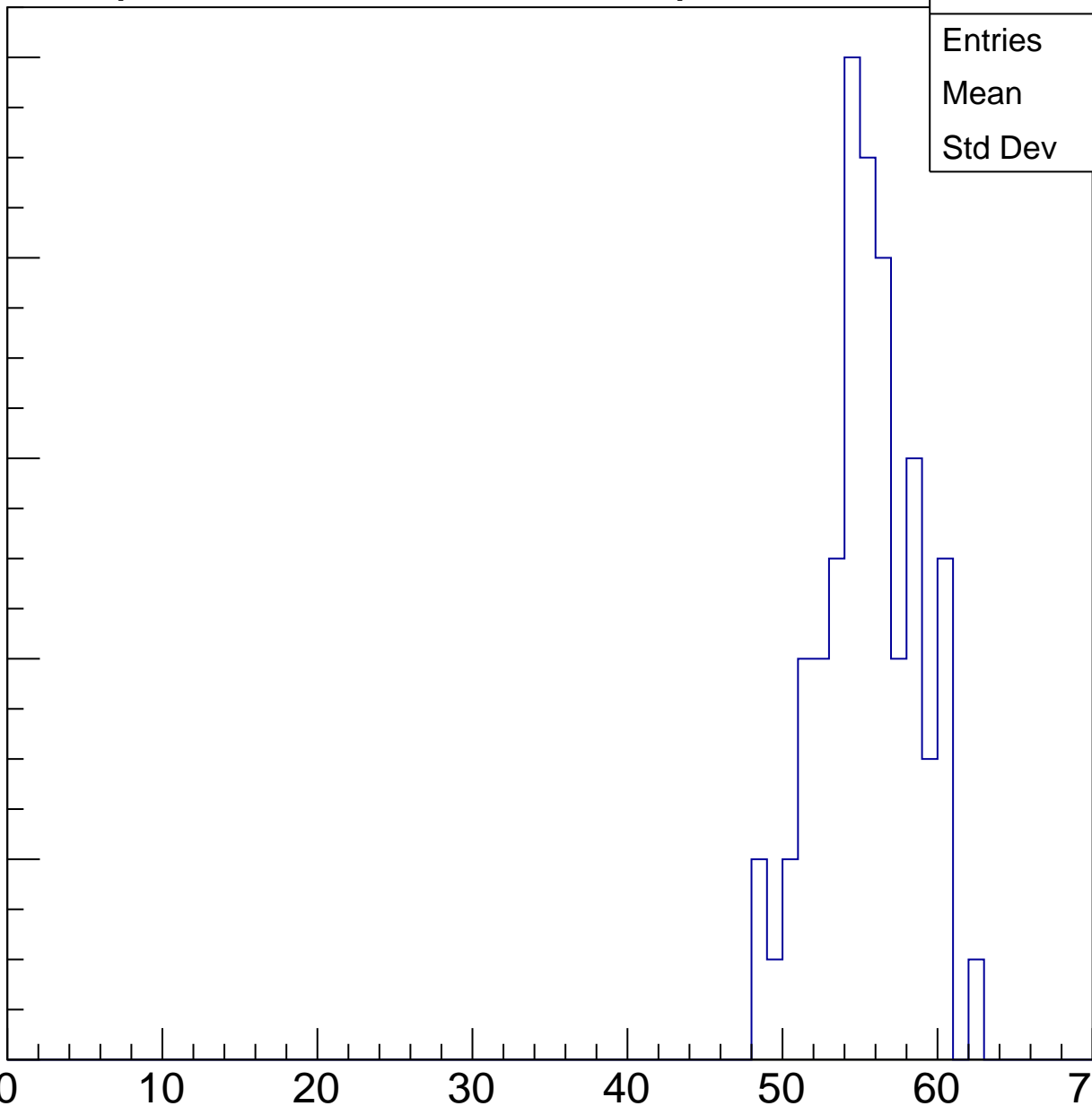
Entries	64
Mean	55
Std Dev	3.097

Entry

10  
8  
6  
4  
2  
0

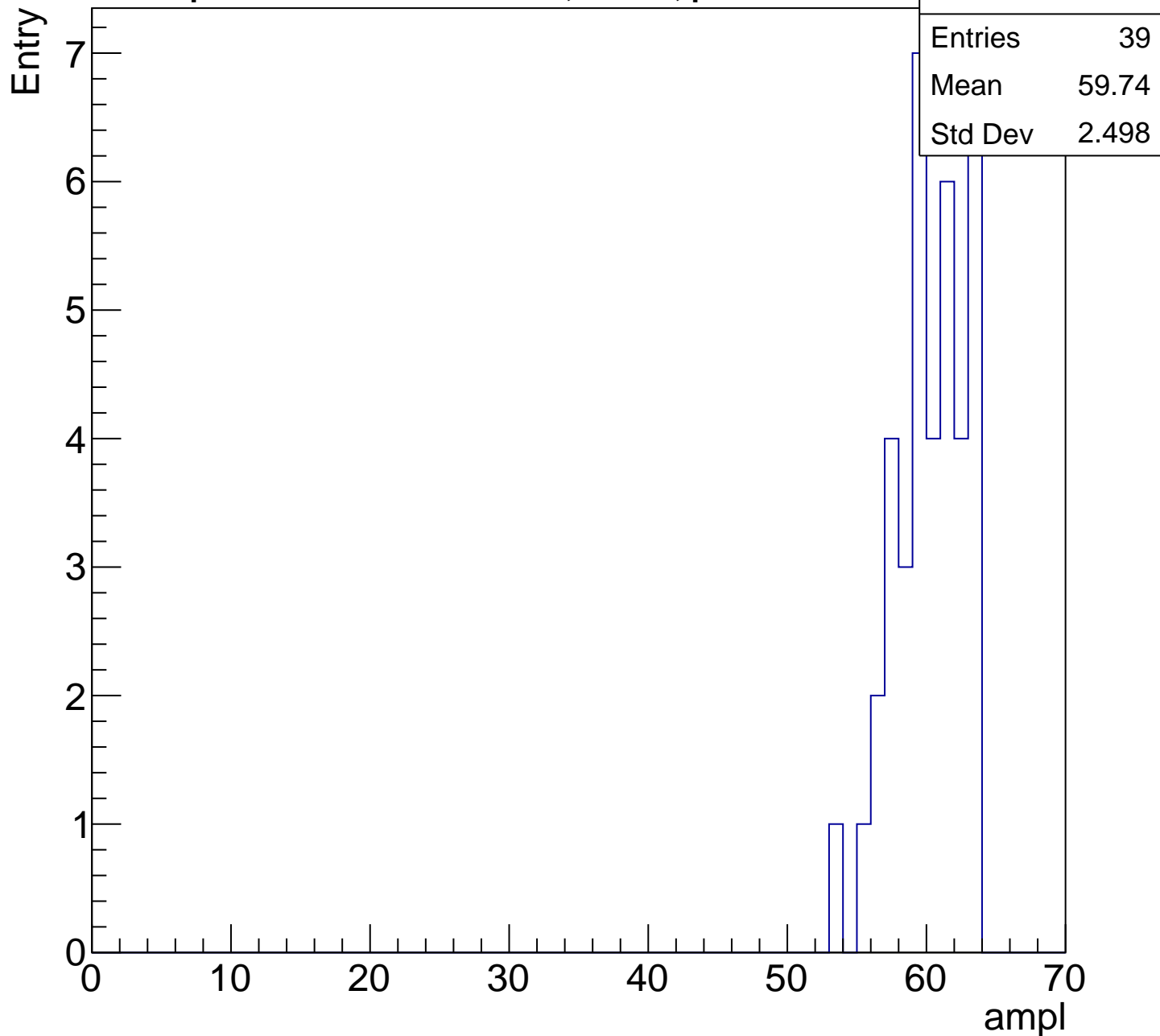
0 10 20 30 40 50 60 70

ampl



# B1L003S, U3-ch93, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

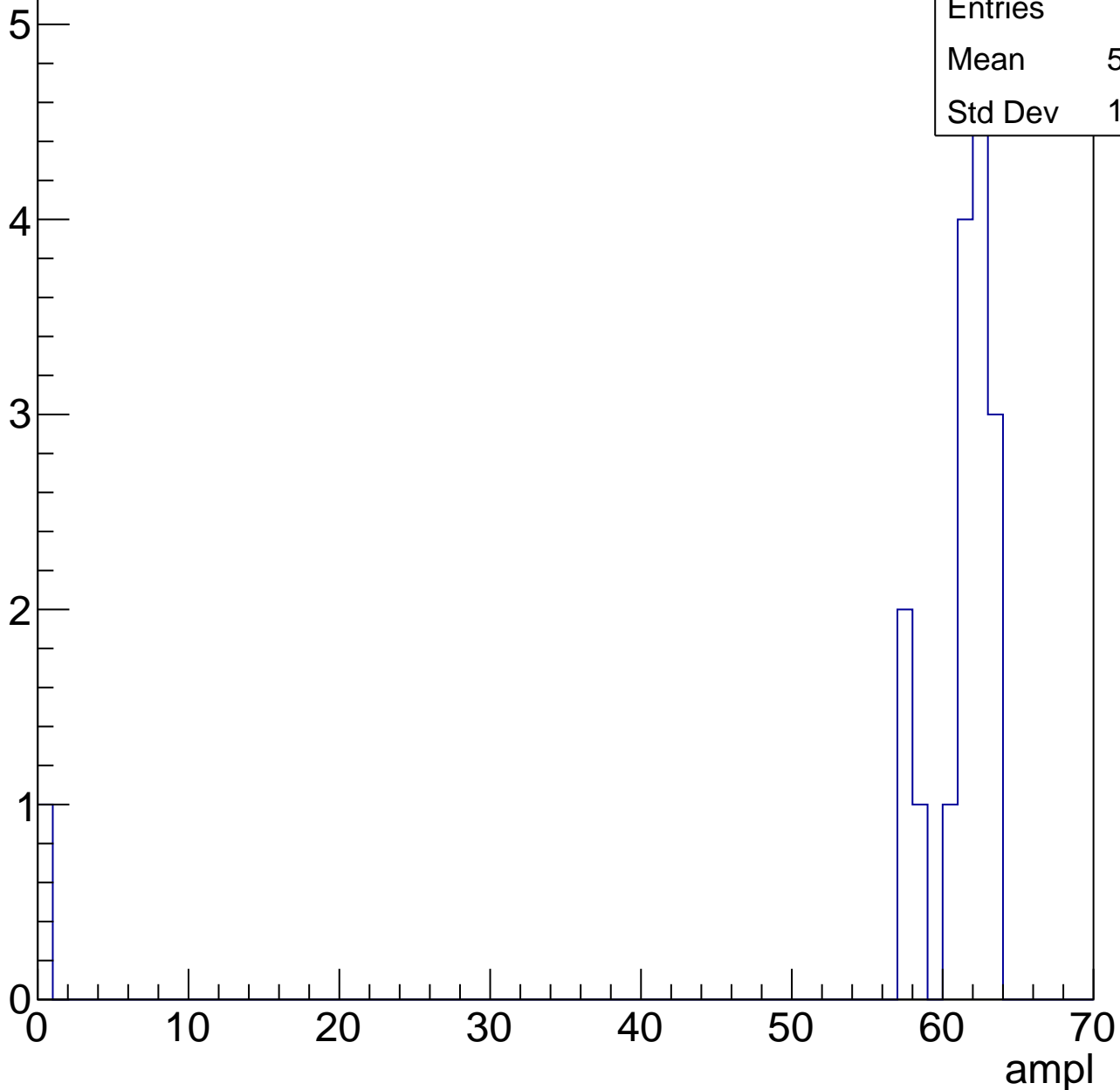


# B1L003S, U3-ch93, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	17
Mean	57.35
Std Dev	14.46





# B1L003S, U3-ch93, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U3-ch94, adc0

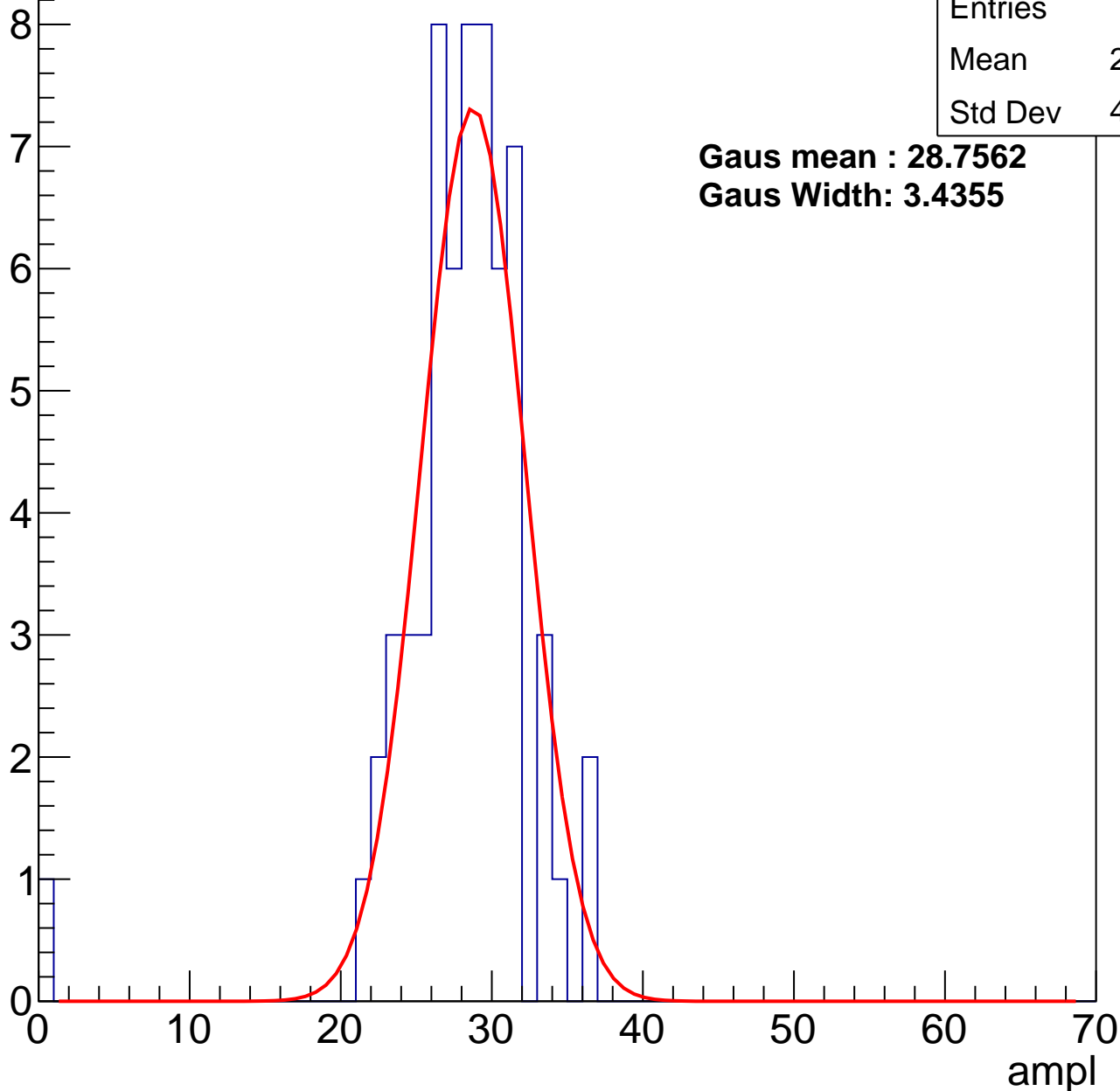
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	27.56
Std Dev	4.778

**Gaus mean : 28.7562**

**Gaus Width: 3.4355**



# B1L003S, U3-ch94, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	67
Mean	35
Std Dev	3.528

**Gaus mean : 35.2347**

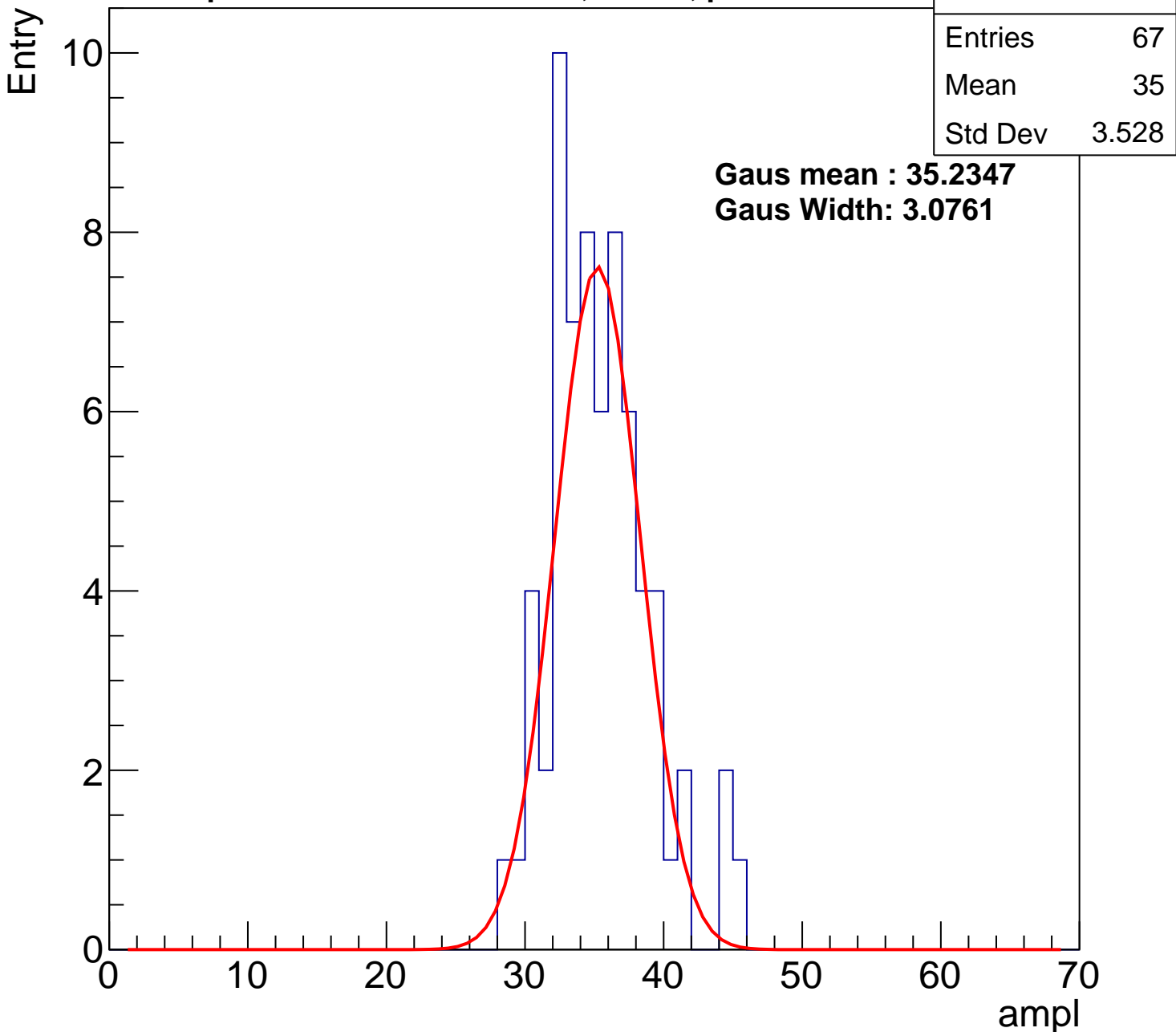
**Gaus Width: 3.0761**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U3-ch94, adc2

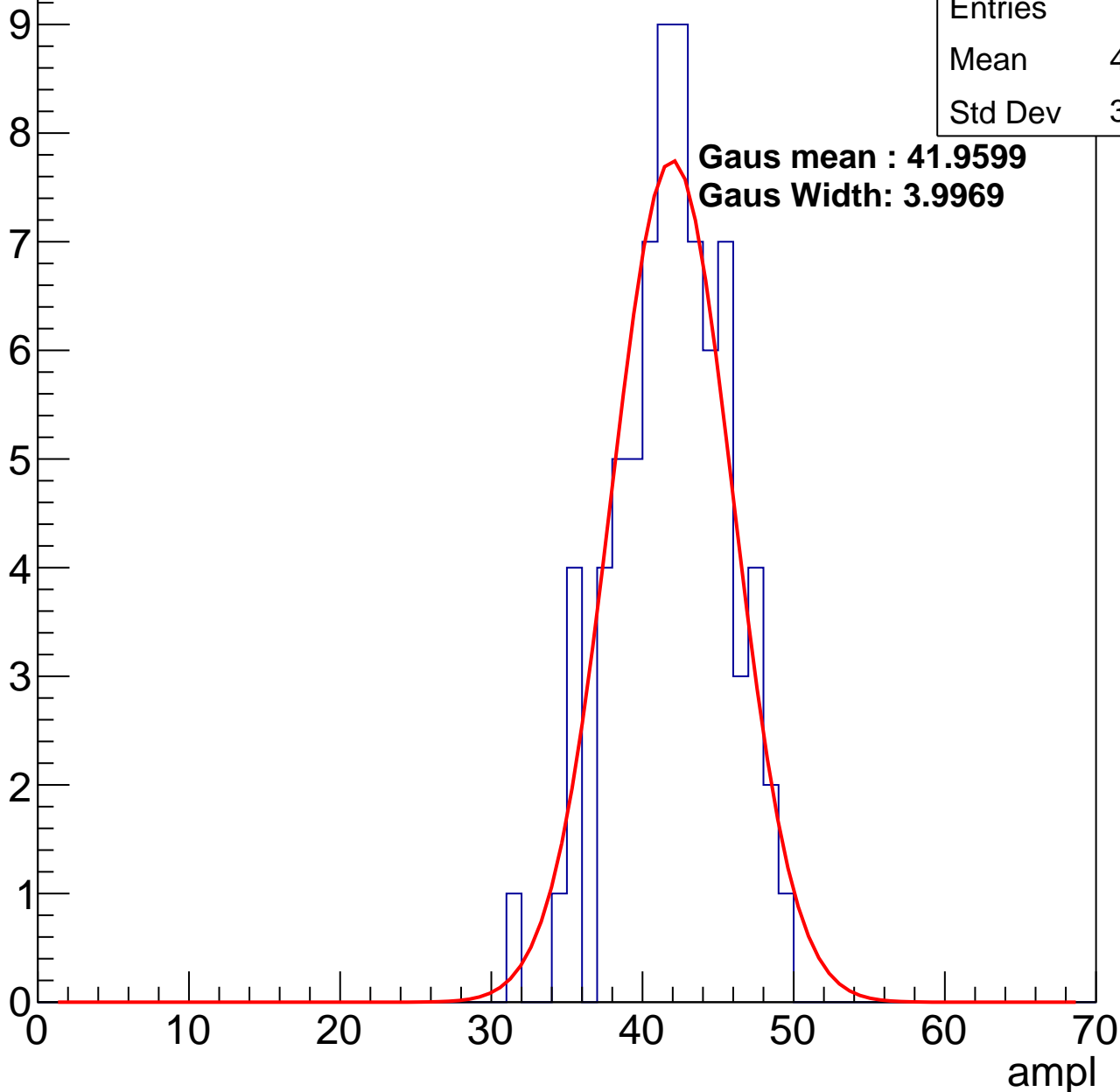
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	75
Mean	41.55
Std Dev	3.634

**Gaus mean : 41.9599**

**Gaus Width: 3.9969**

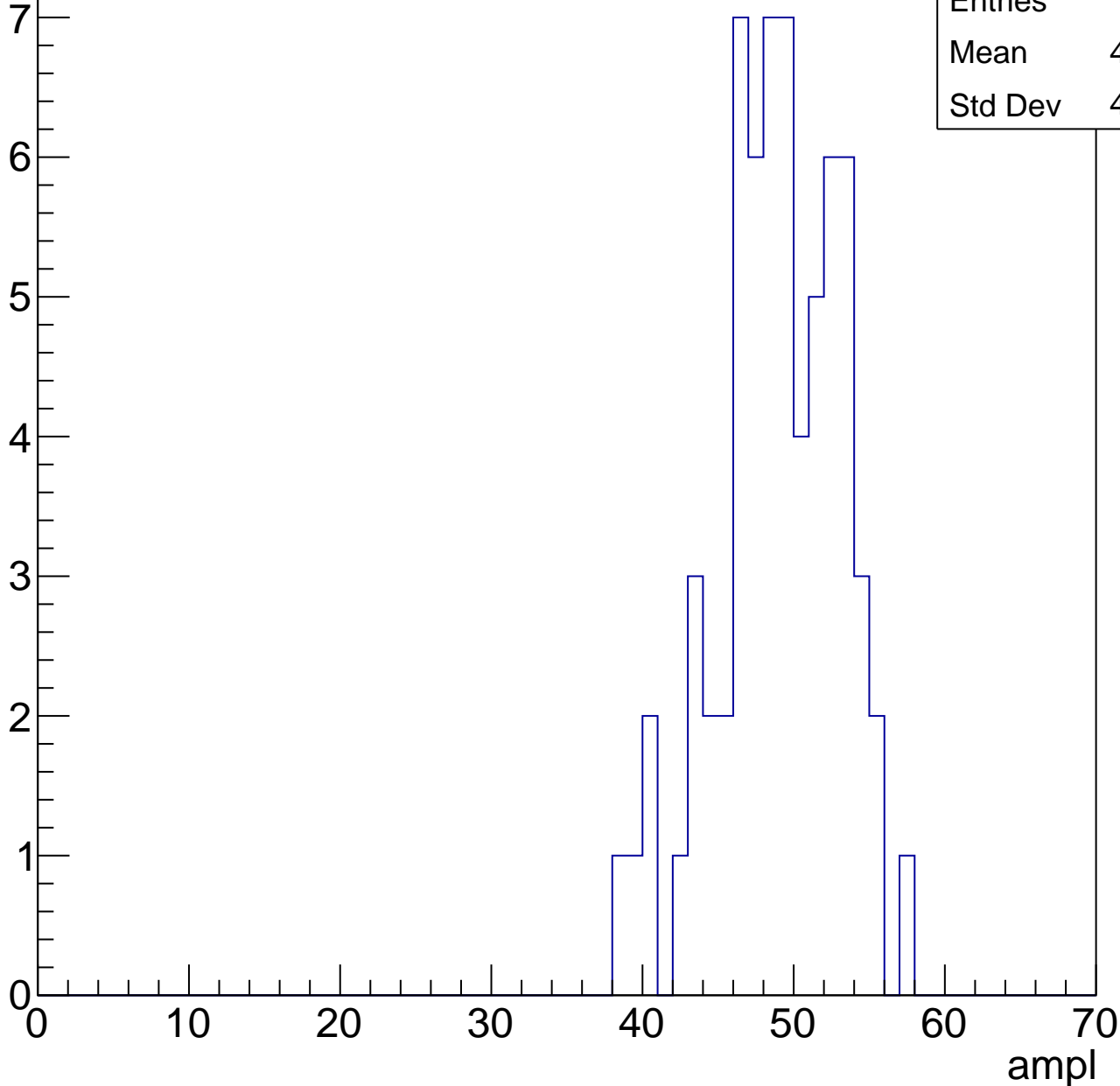


# B1L003S, U3-ch94, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	48.53
Std Dev	4.057

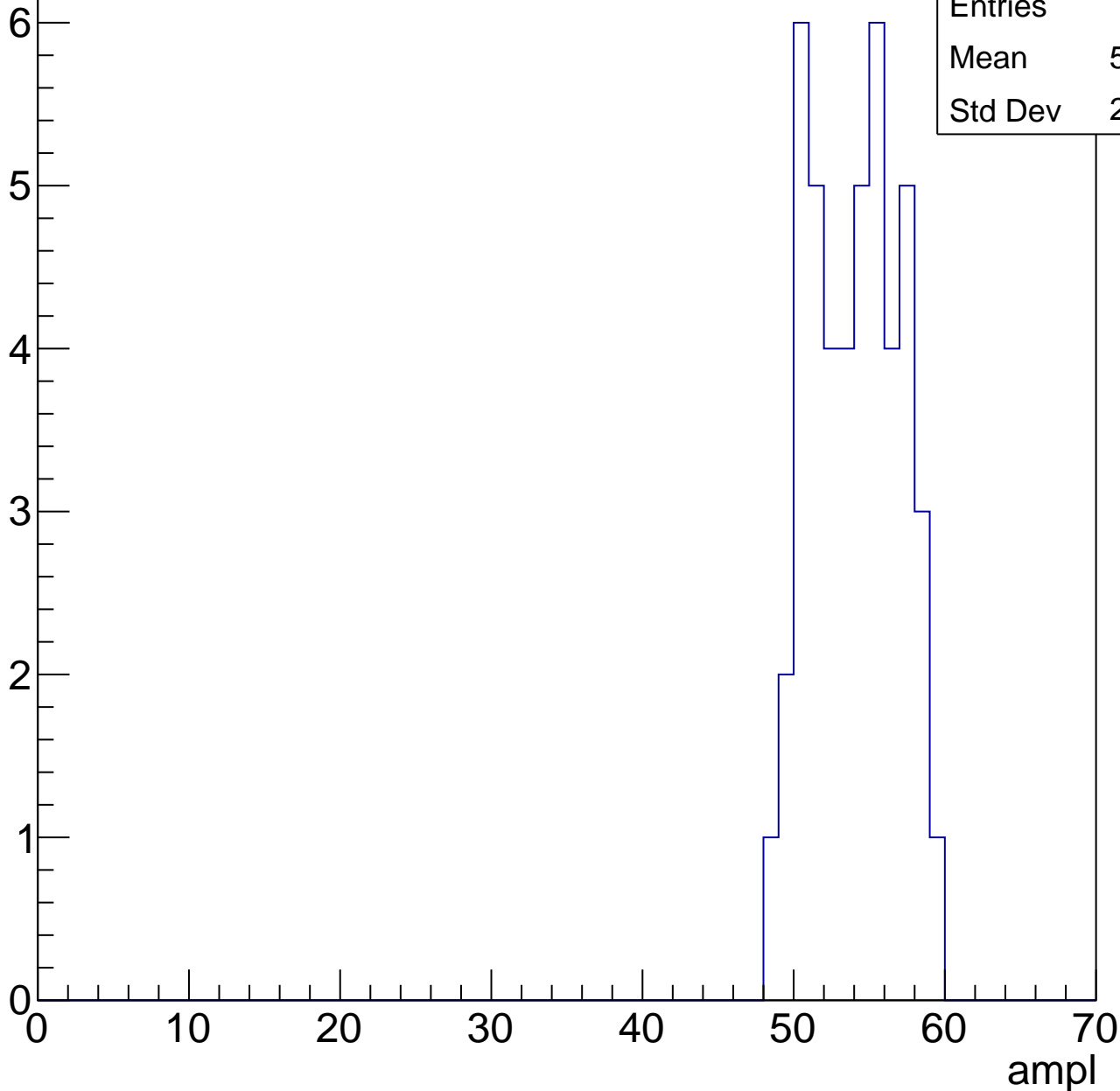


# B1L003S, U3-ch94, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

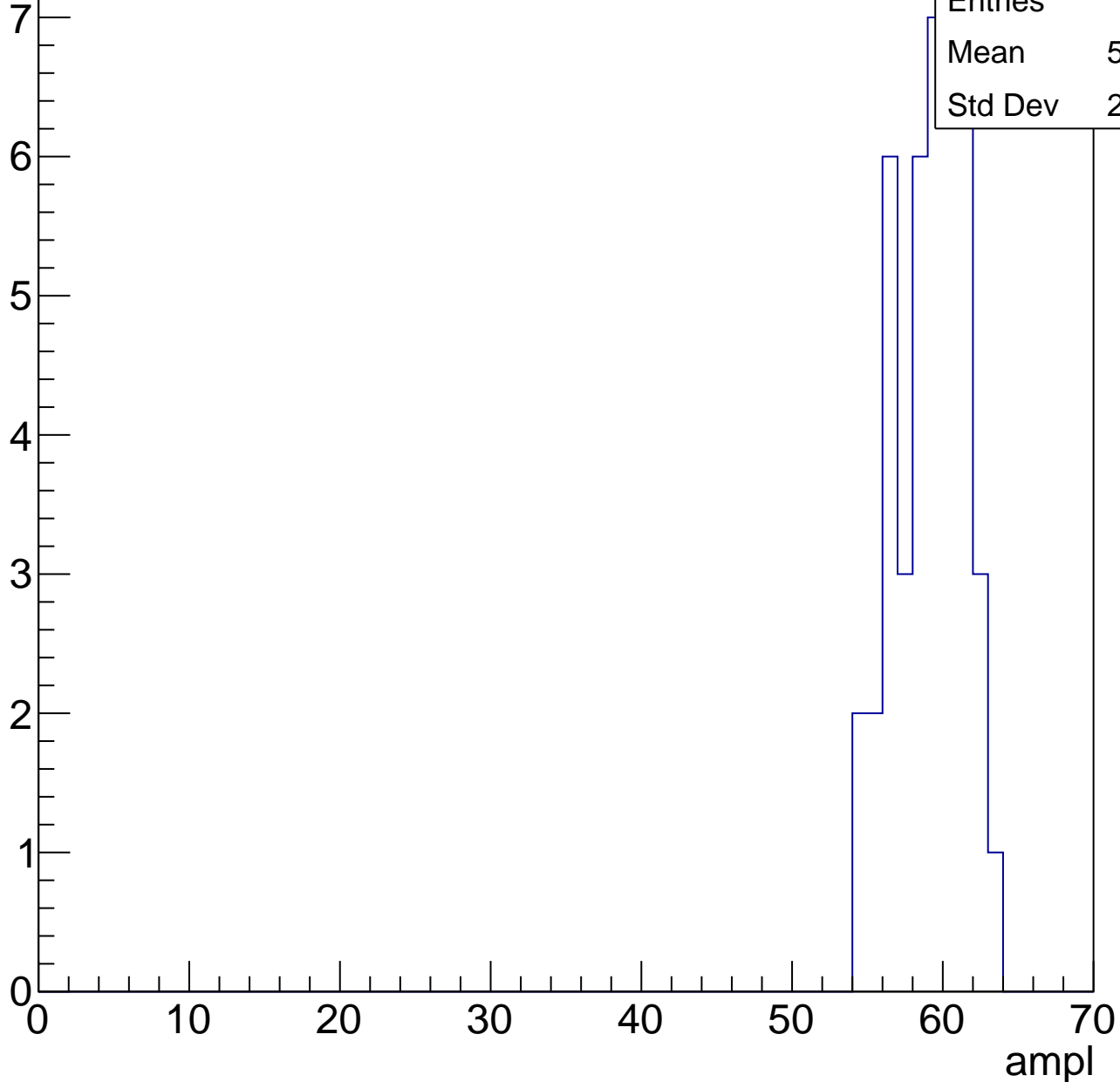
Entries	46
Mean	53.54
Std Dev	2.864



# B1L003S, U3-ch94, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

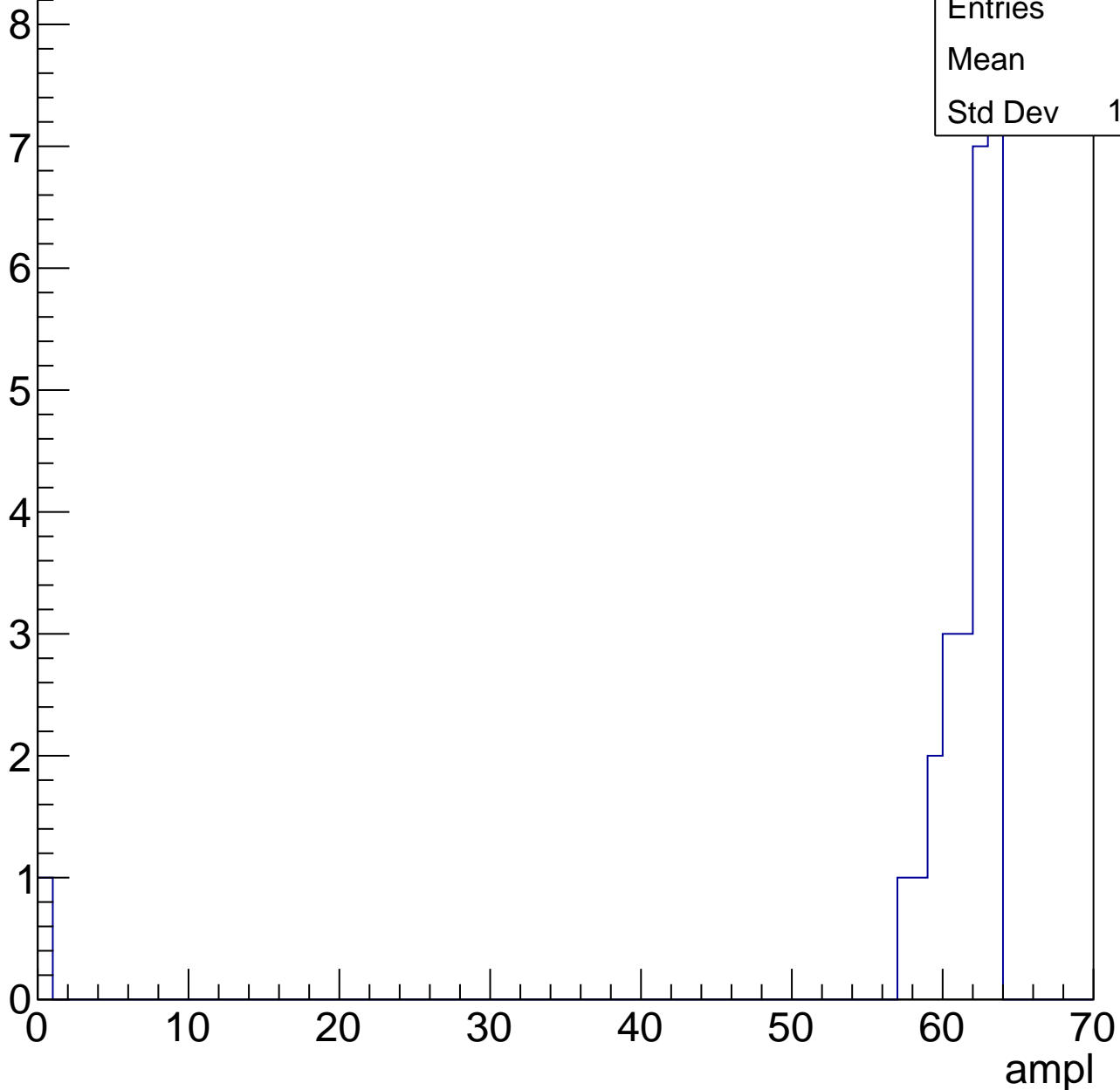


# B1L003S, U3-ch94, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	26
Mean	59
Std Dev	11.92

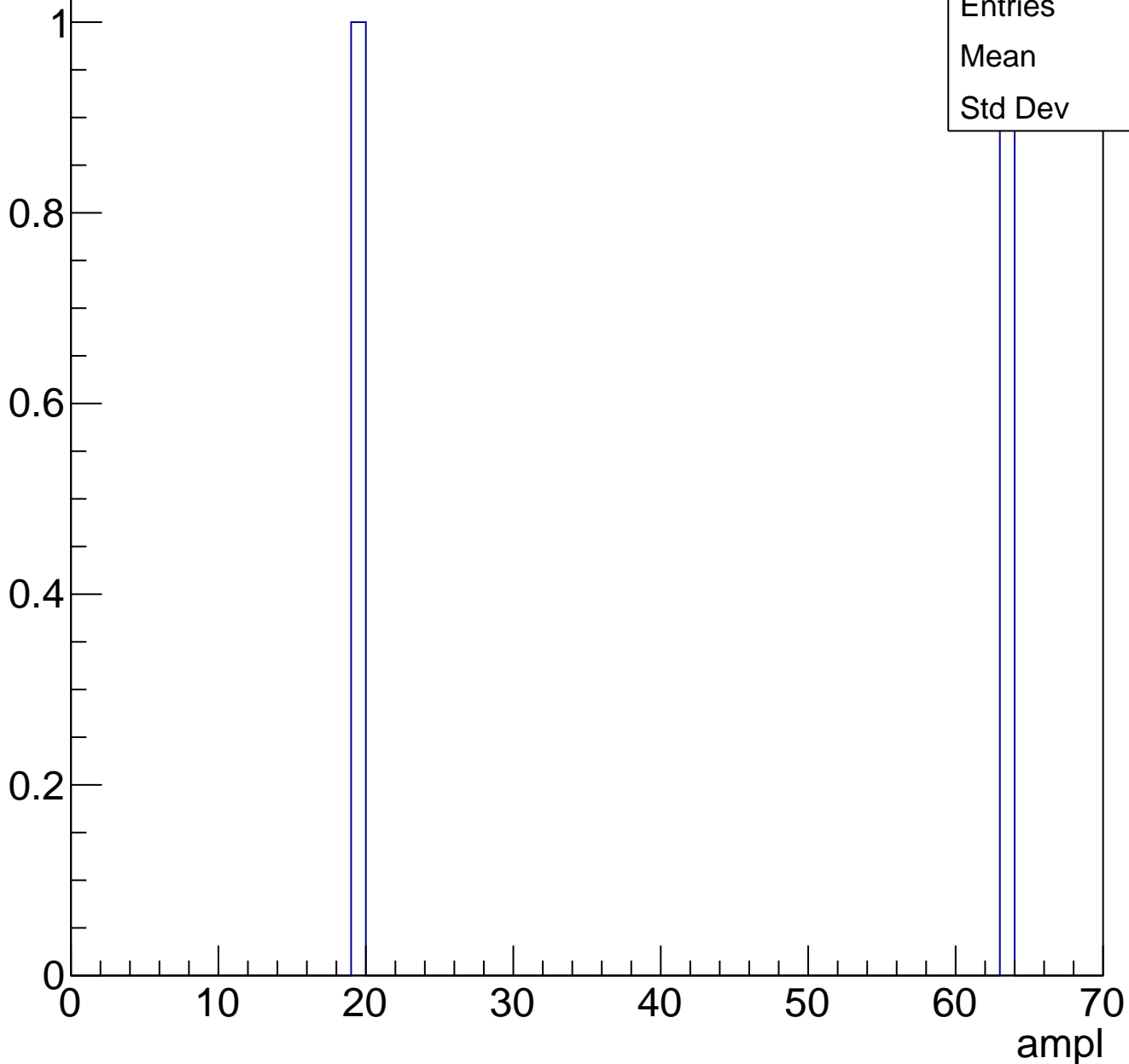




# B1L003S, U3-ch94, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U3-ch95, adc0

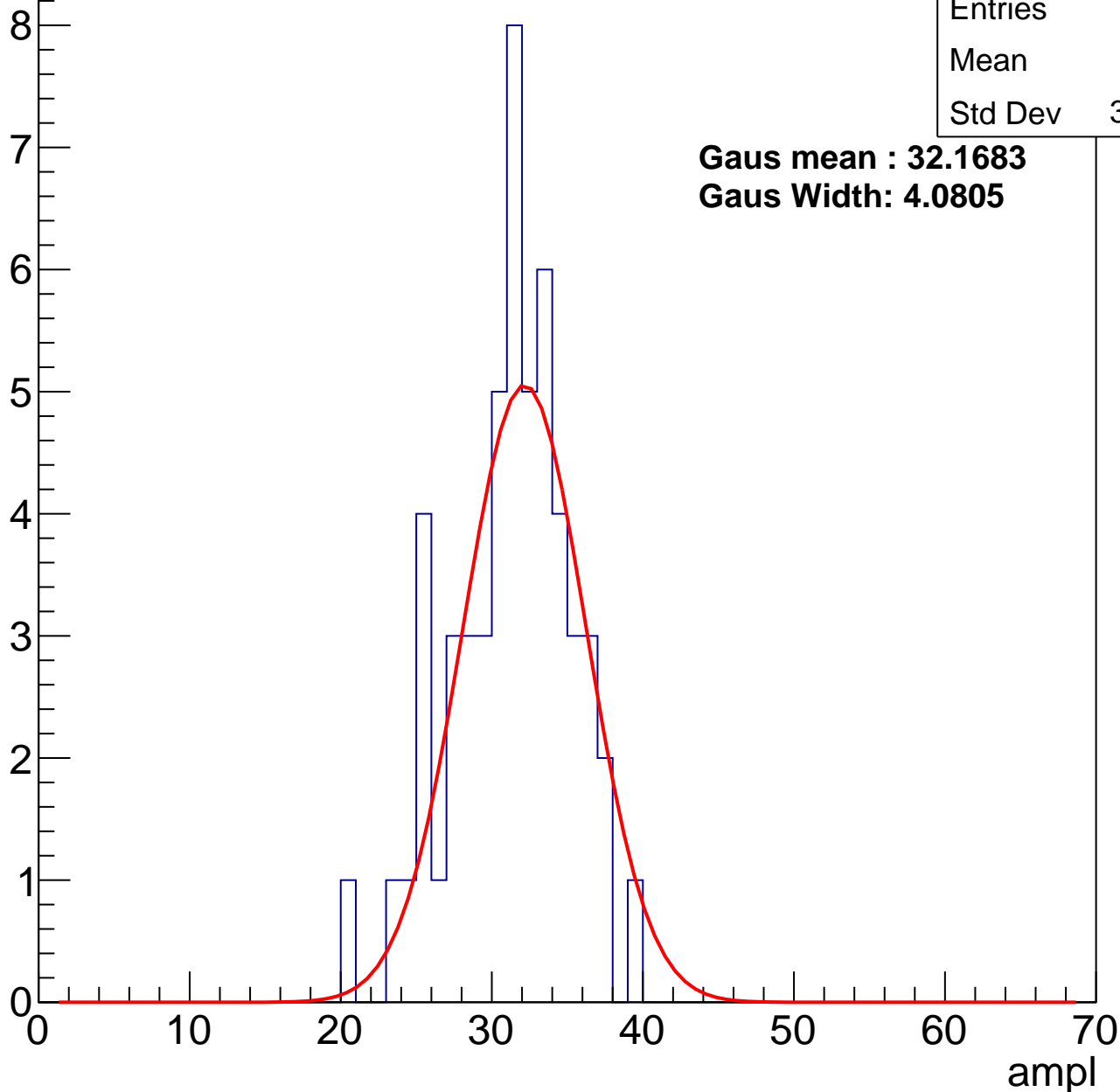
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	54
Mean	30.8
Std Dev	3.889

**Gaus mean : 32.1683**

**Gaus Width: 4.0805**



# B1L003S, U3-ch95, adc1

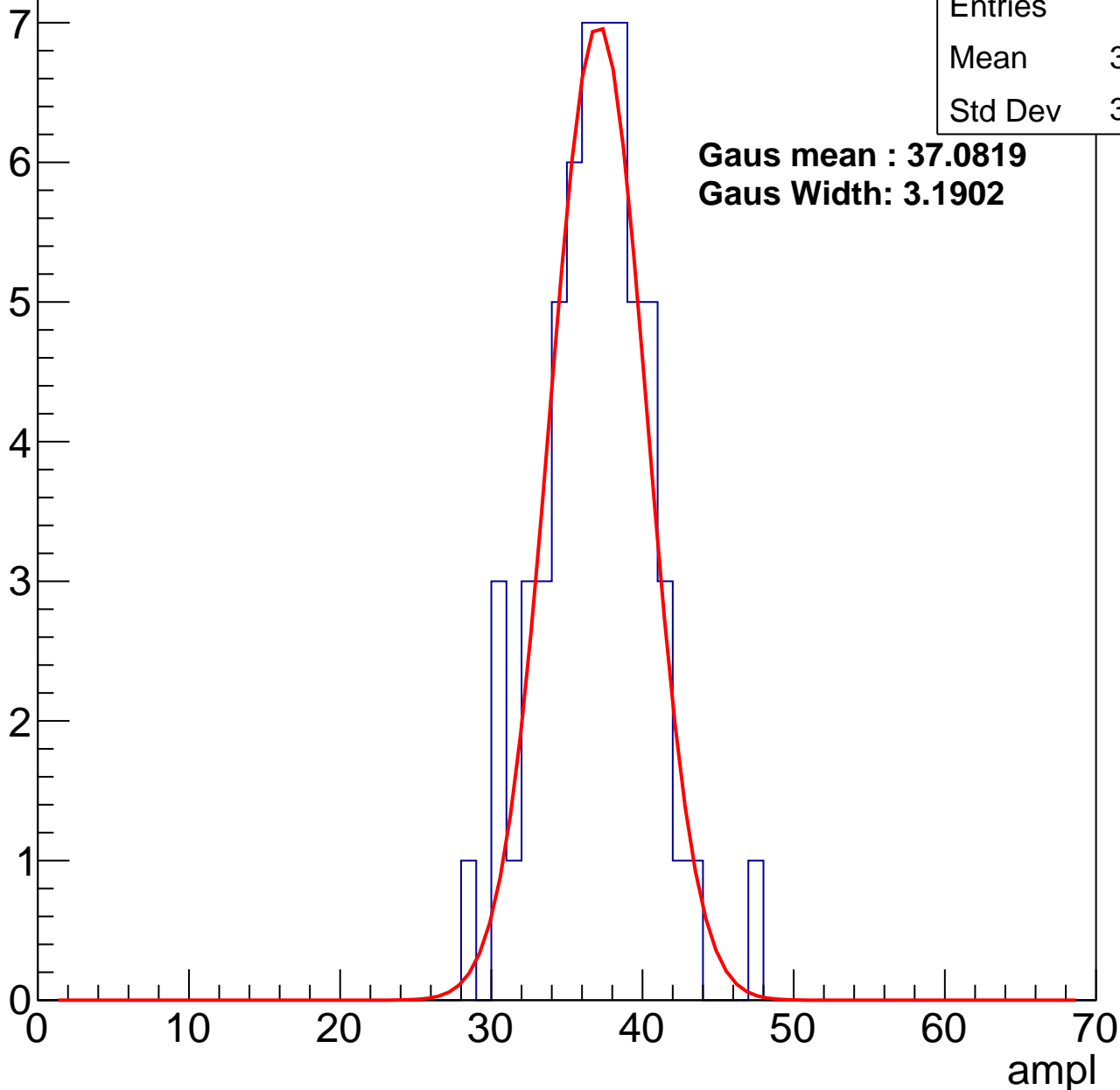
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	36.46
Std Dev	3.509

**Gaus mean : 37.0819**

**Gaus Width: 3.1902**



# B1L003S, U3-ch95, adc2

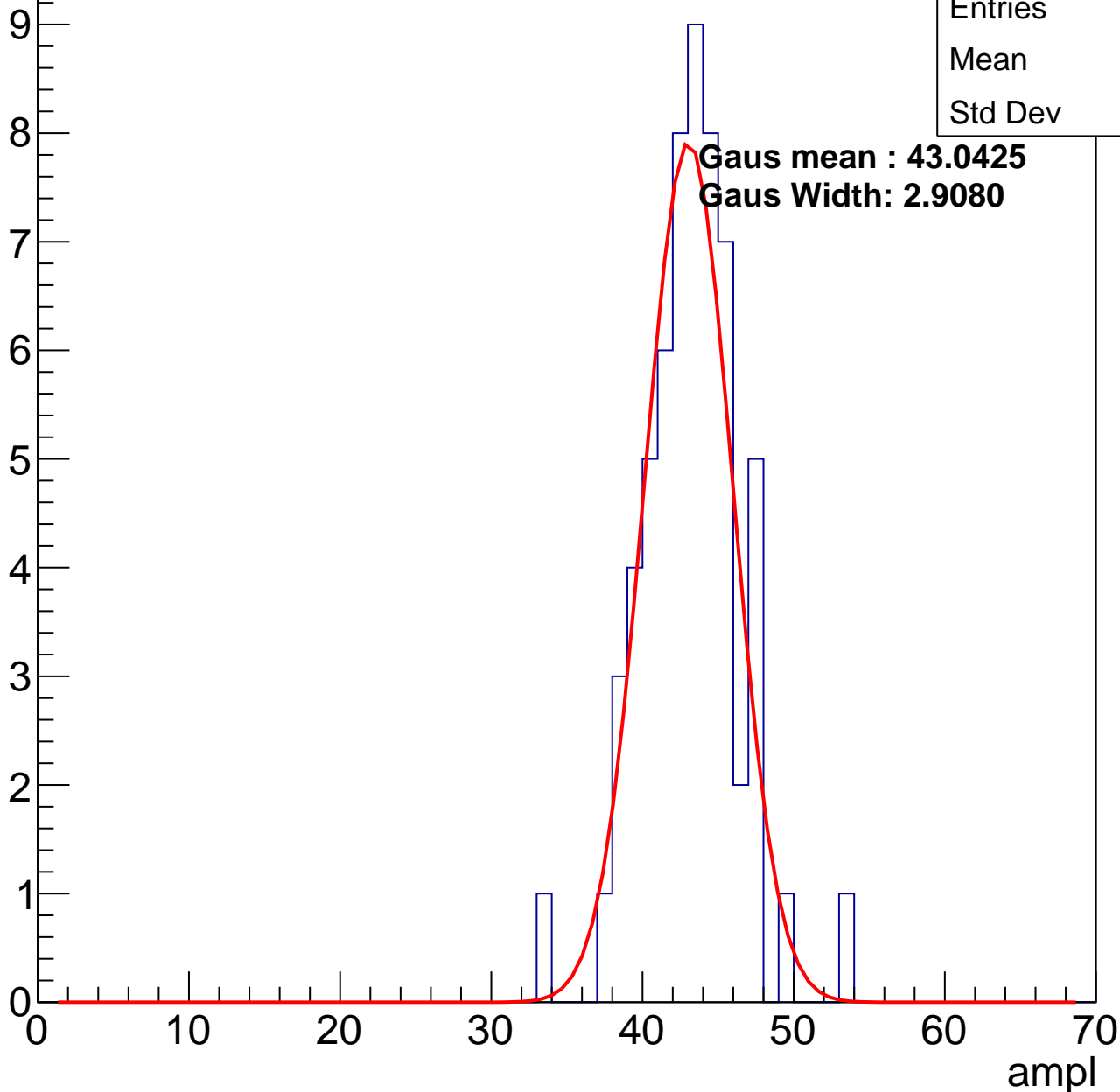
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	42.7
Std Dev	3.18

**Gaus mean : 43.0425**

**Gaus Width: 2.9080**

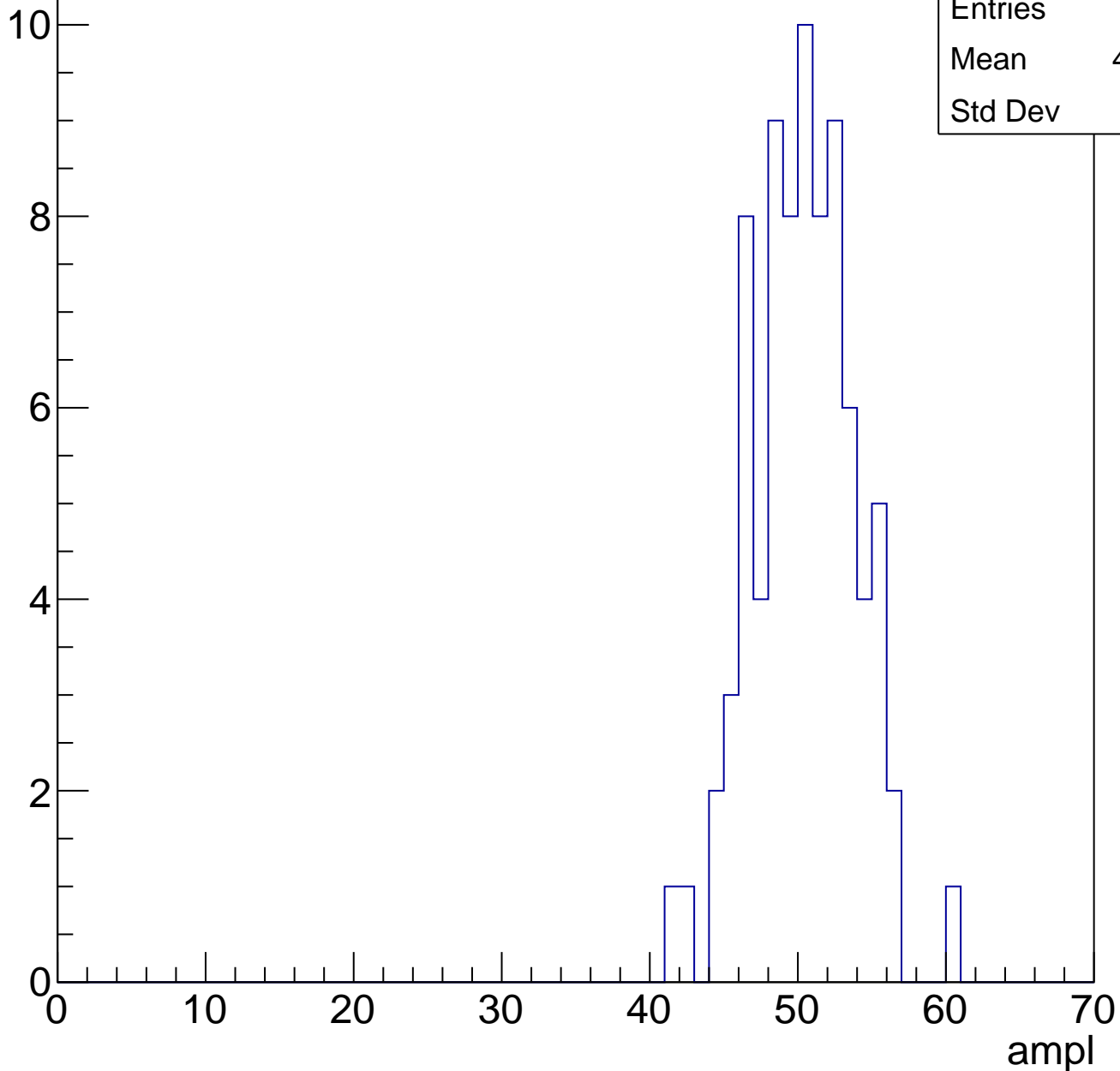


# B1L003S, U3-ch95, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	81
Mean	49.91
Std Dev	3.44

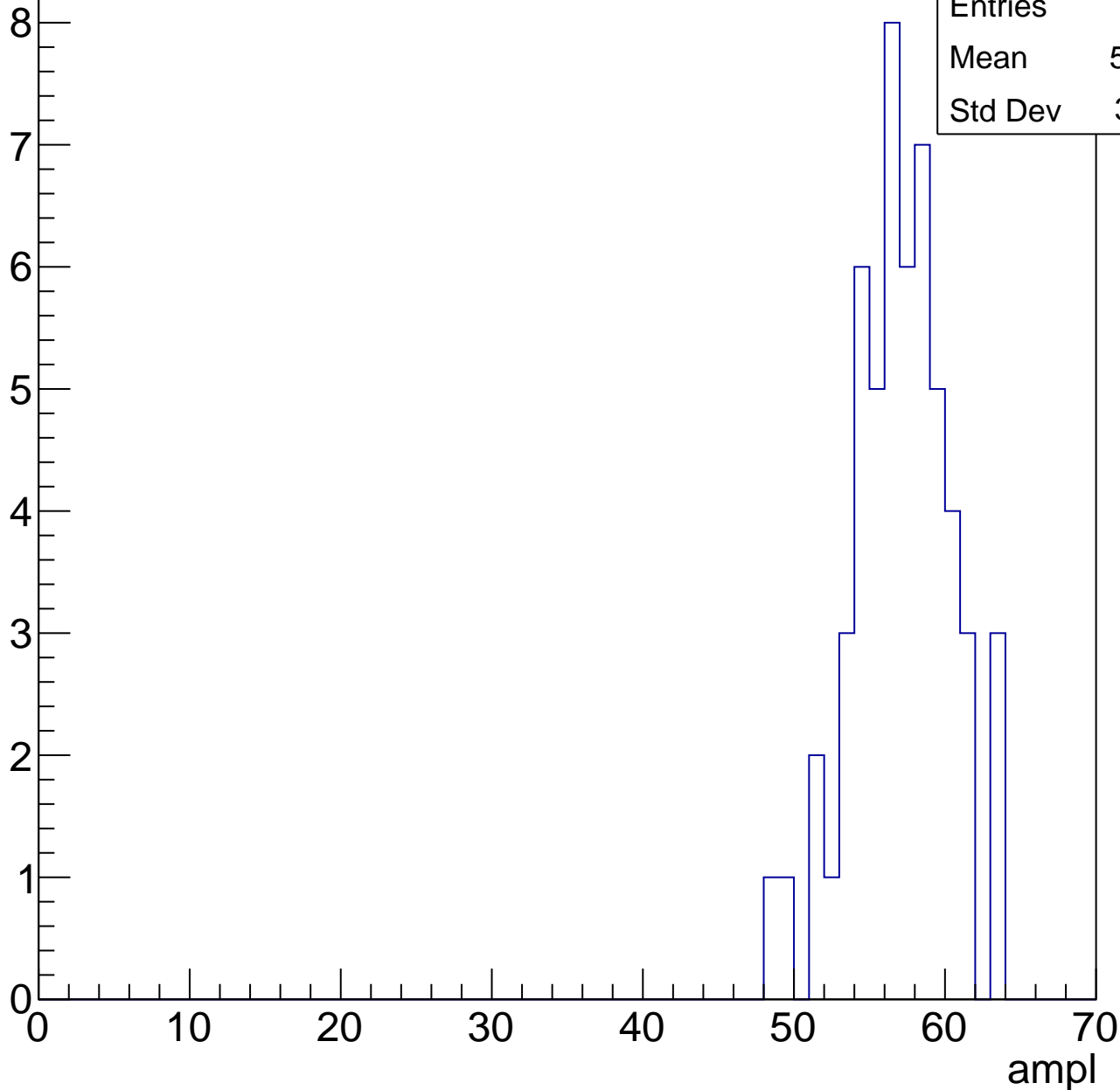
Entry



# B1L003S, U3-ch95, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



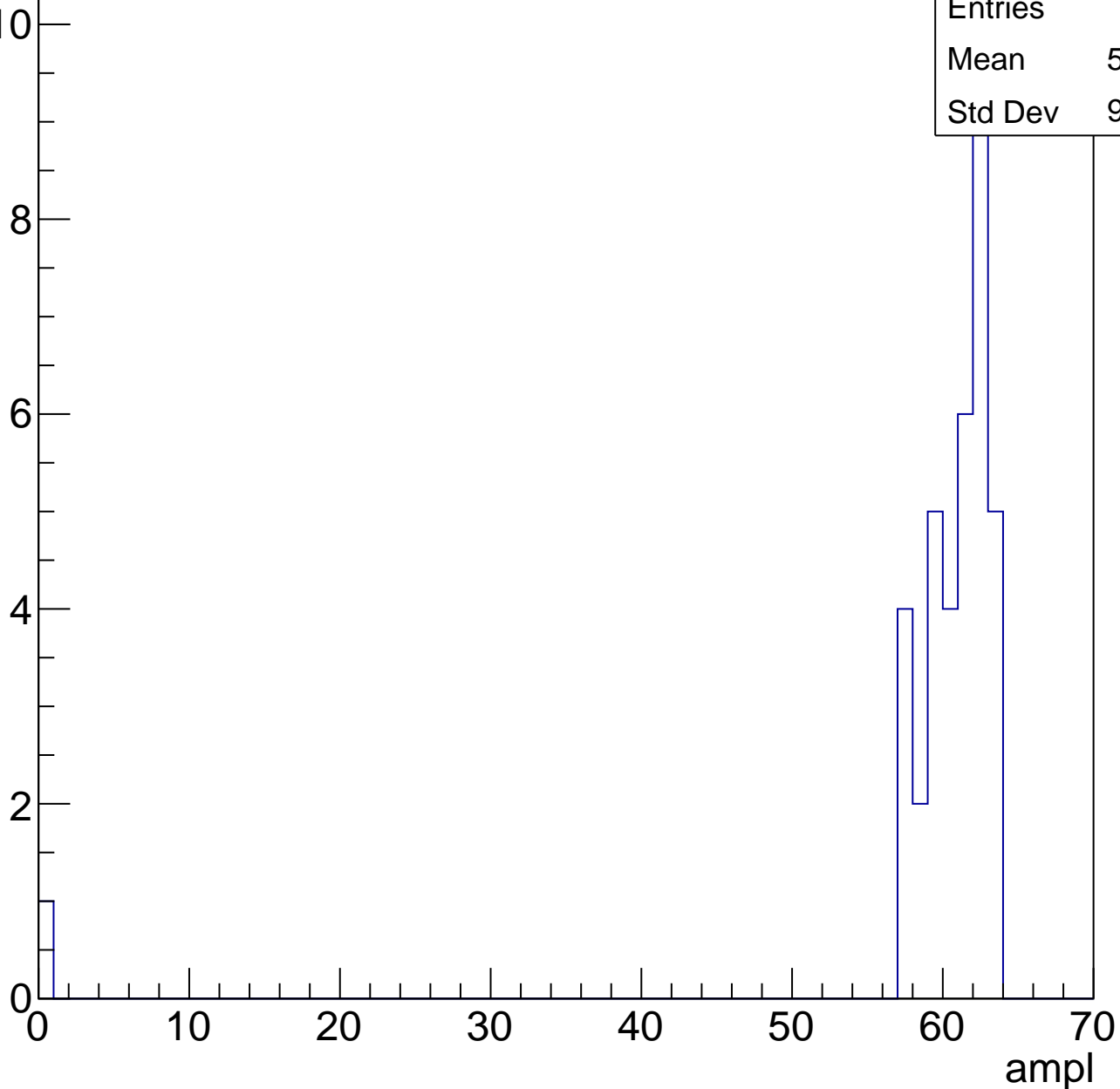
Entries	55
Mean	56.58
Std Dev	3.251

# B1L003S, U3-ch95, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

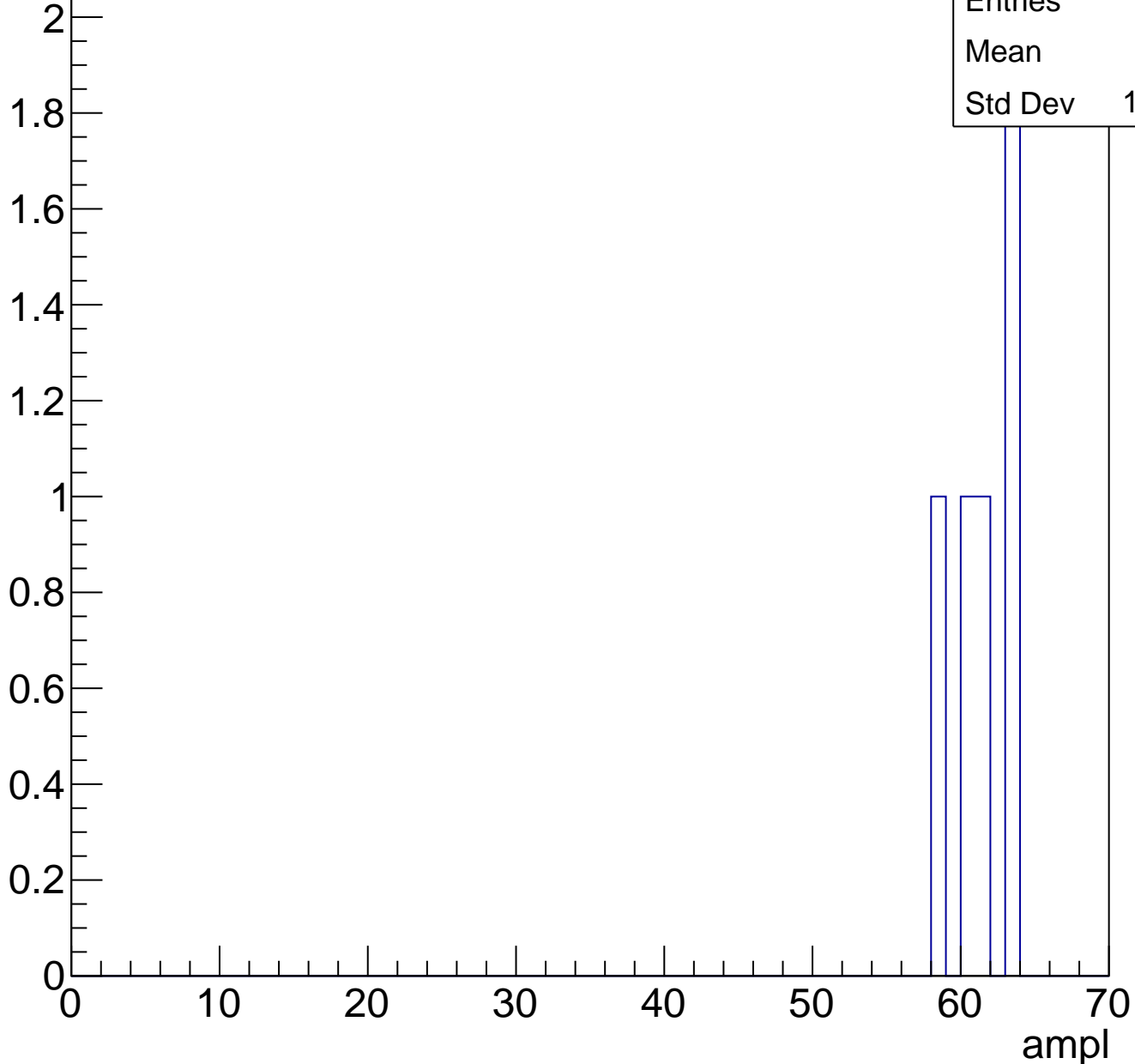
Entries	37
Mean	58.92
Std Dev	9.996



# B1L003S, U3-ch95, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch95, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L003S, U3-ch96, adc0

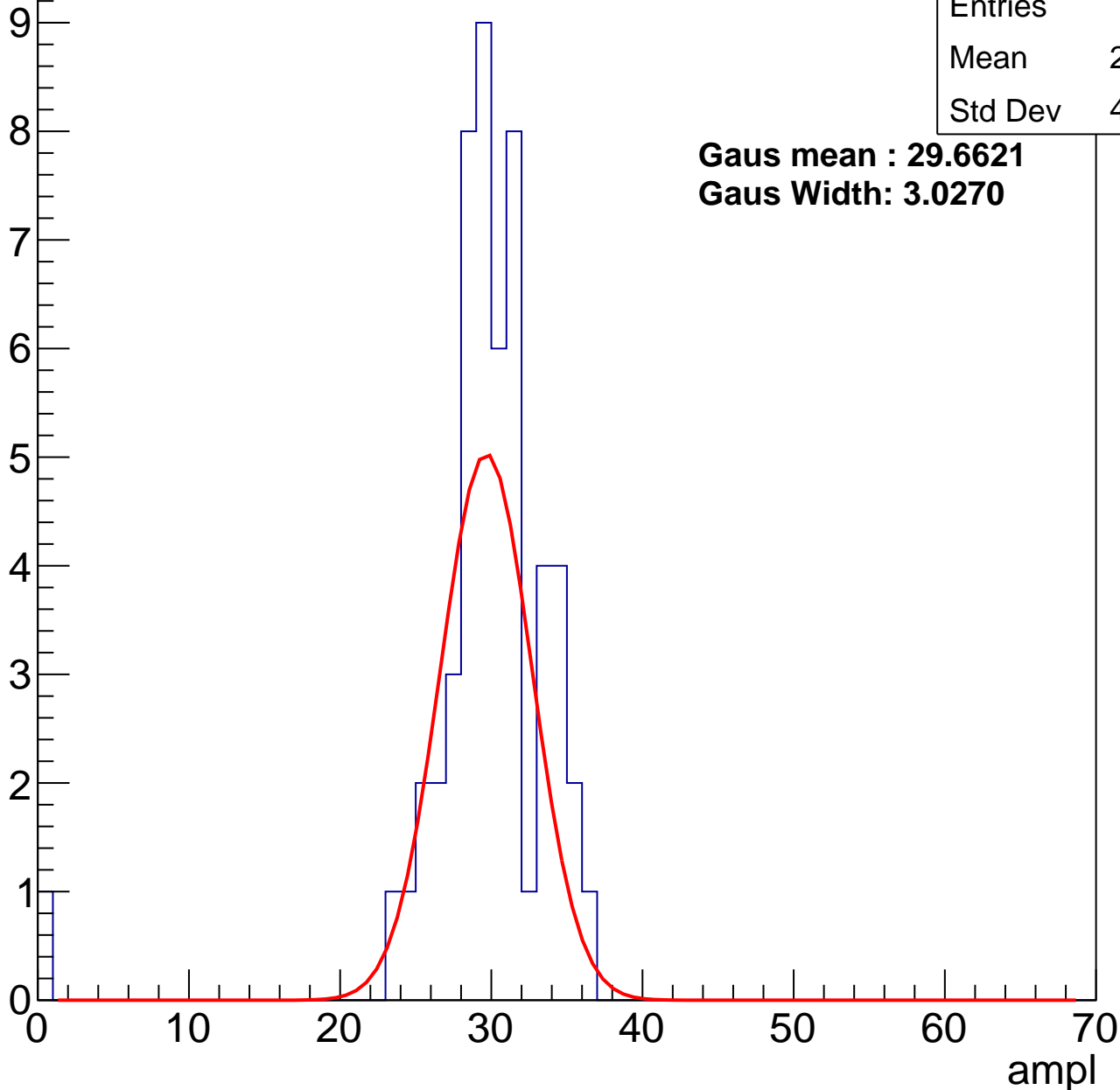
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	29.23
Std Dev	4.955

**Gaus mean : 29.6621**

**Gaus Width: 3.0270**



# B1L003S, U3-ch96, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	75
Mean	36.36
Std Dev	3.726

**Gaus mean : 36.8723**

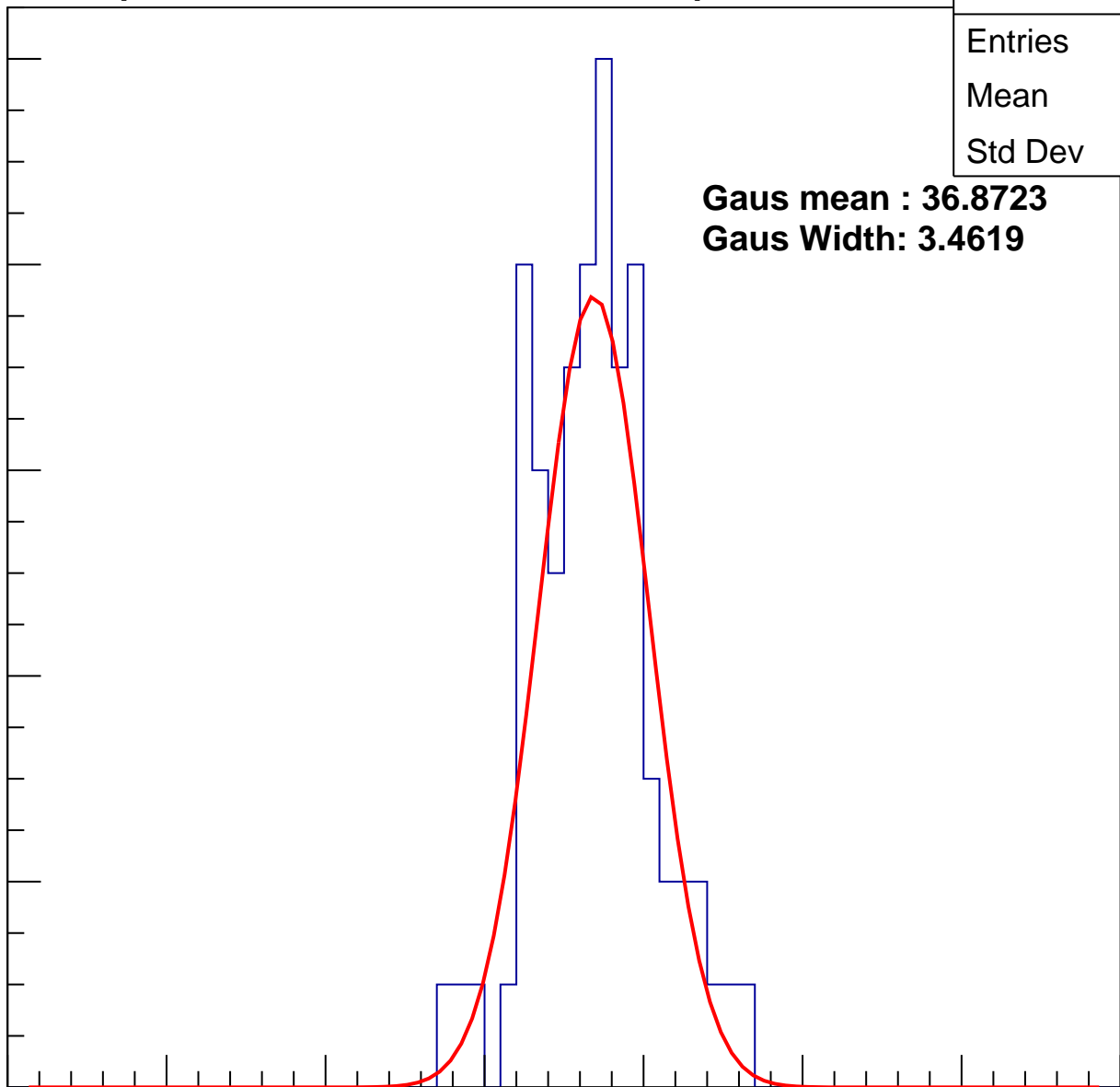
**Gaus Width: 3.4619**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L003S, U3-ch96, adc2

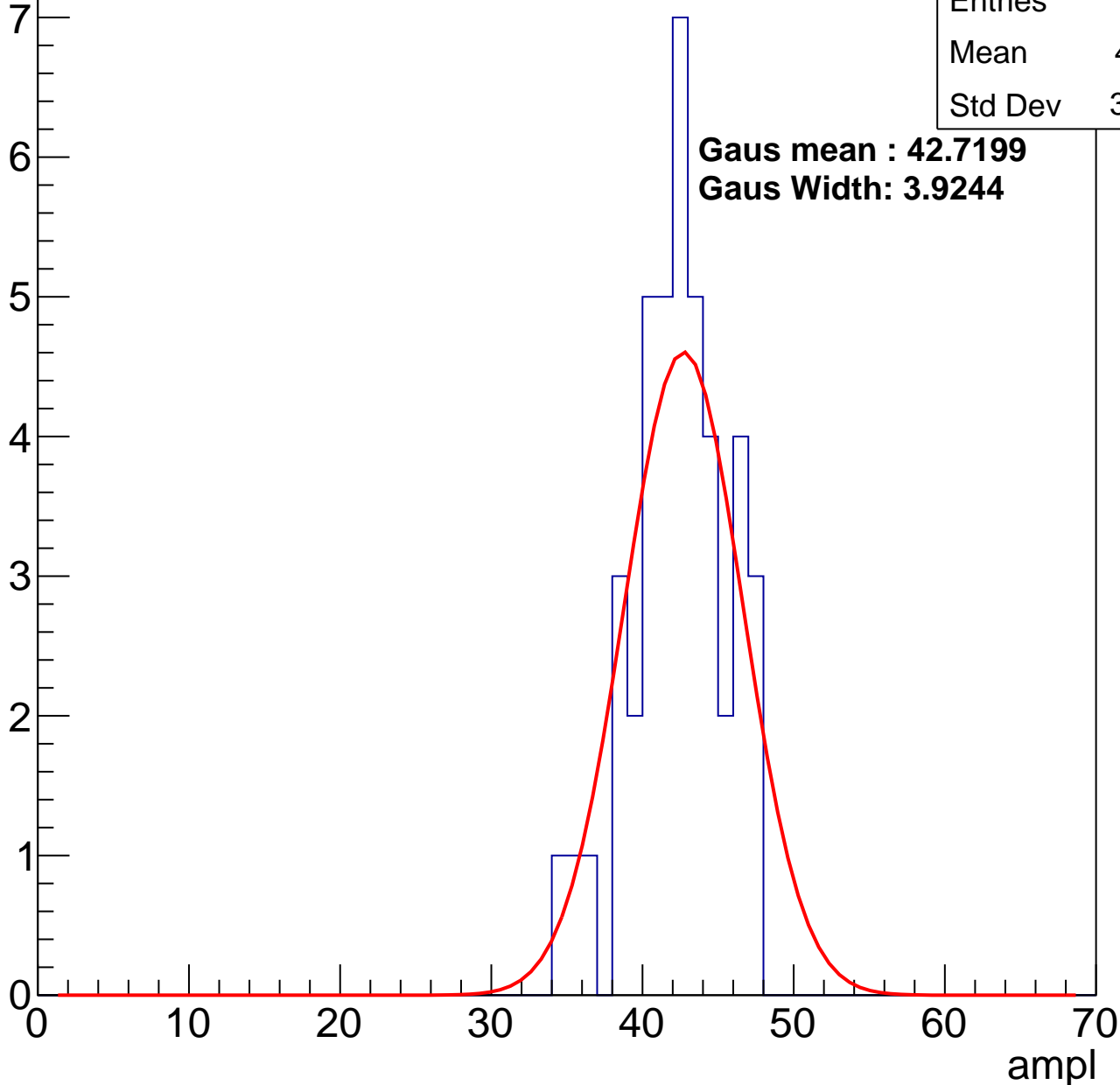
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	43
Mean	41.91
Std Dev	3.116

**Gaus mean : 42.7199**

**Gaus Width: 3.9244**



# B1L003S, U3-ch96, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

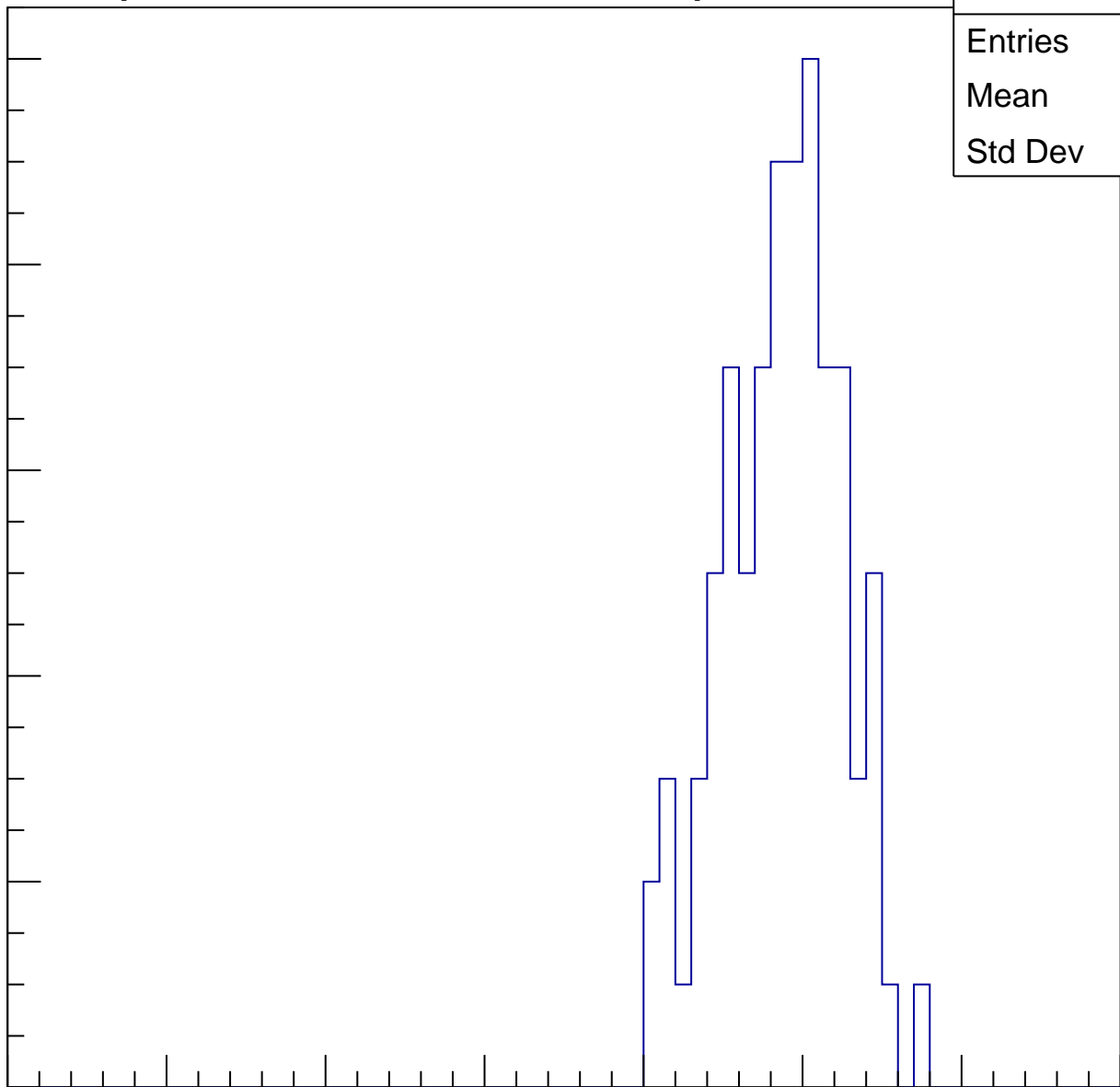
Entries	85
Mean	48.27
Std Dev	3.692

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

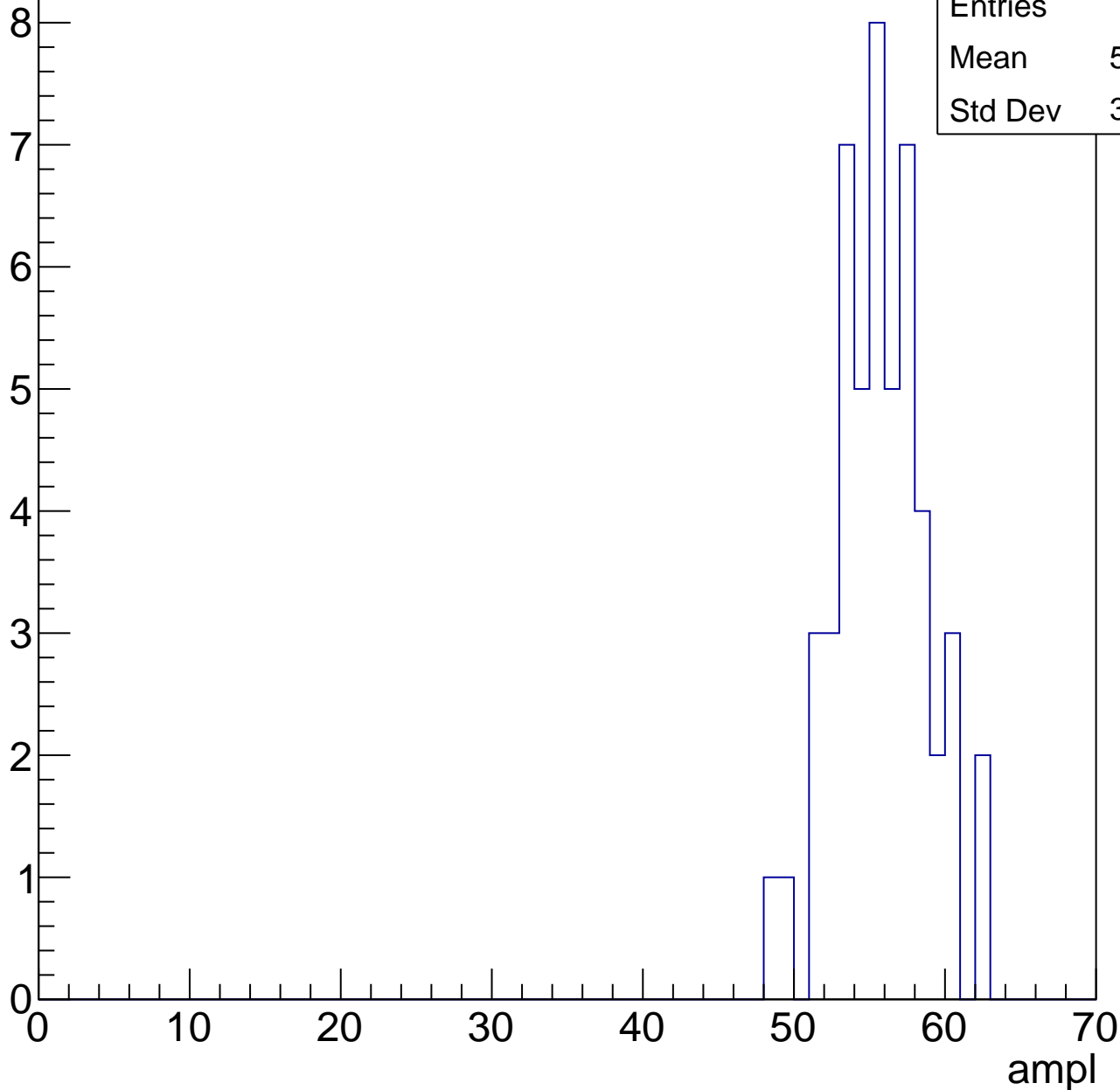


# B1L003S, U3-ch96, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	51
Mean	55.29
Std Dev	3.012

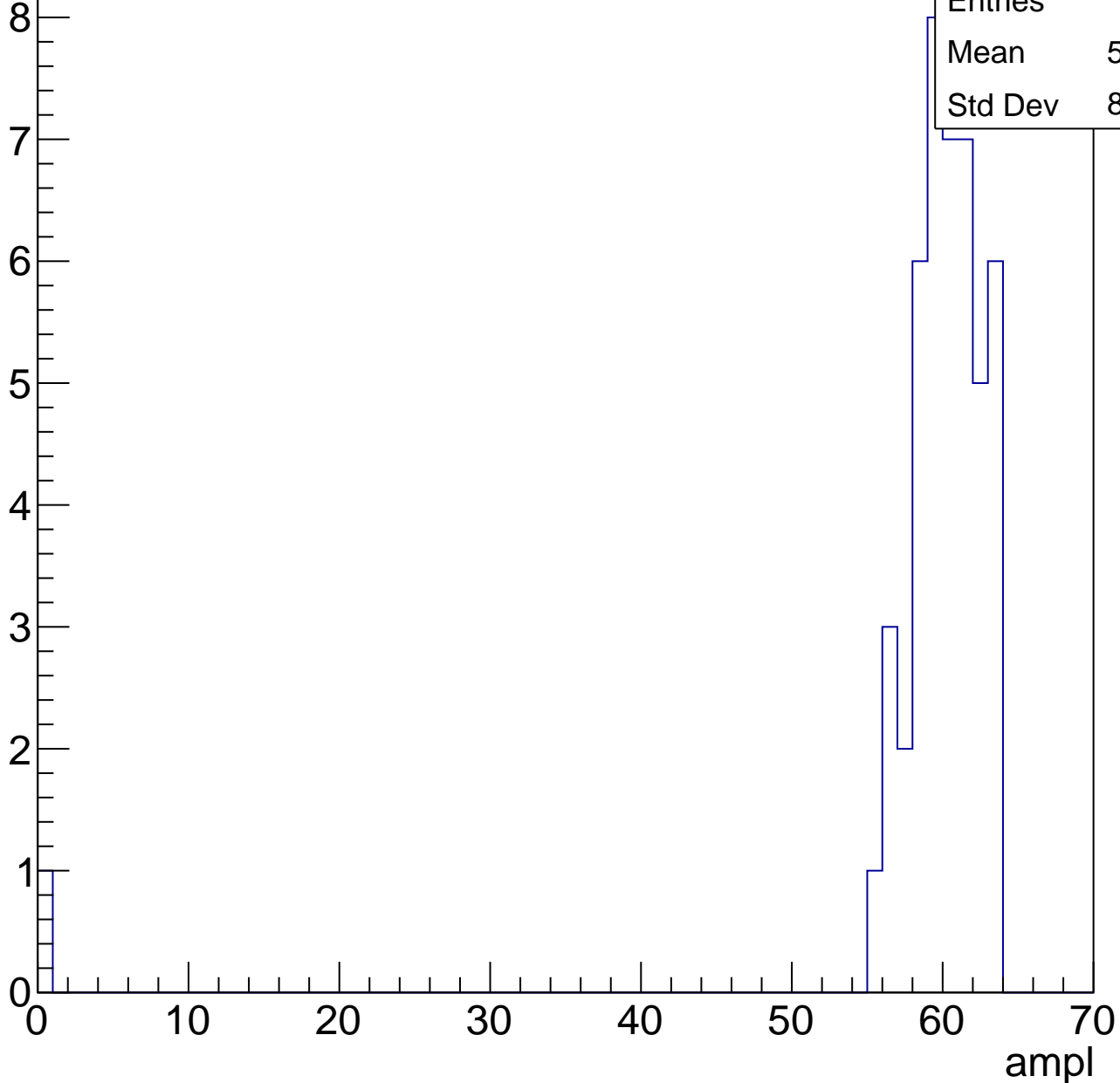


# B1L003S, U3-ch96, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

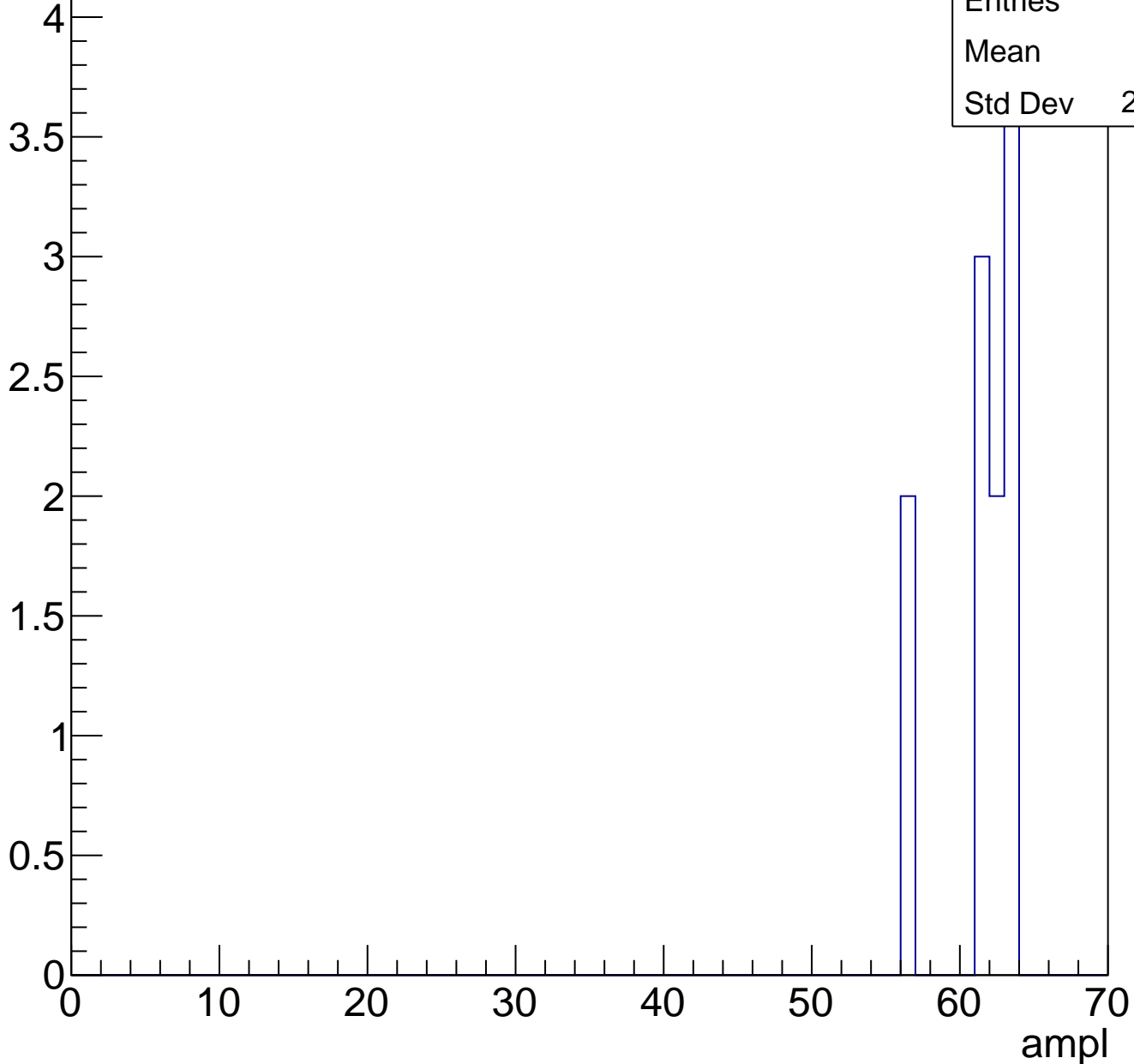
Entries	46
Mean	58.52
Std Dev	8.973



# B1L003S, U3-ch96, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

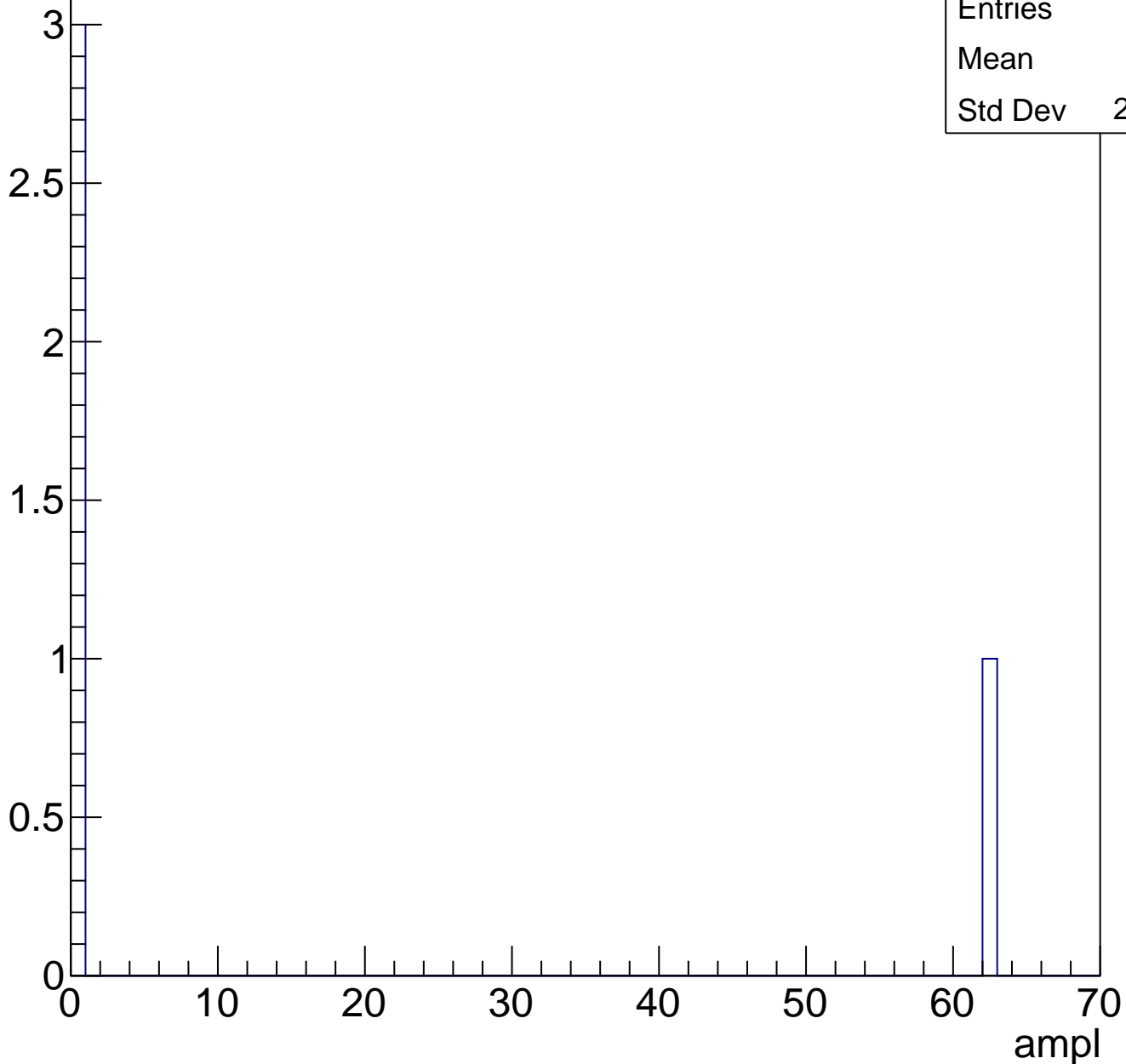




# B1L003S, U3-ch96, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U3-ch97, adc0

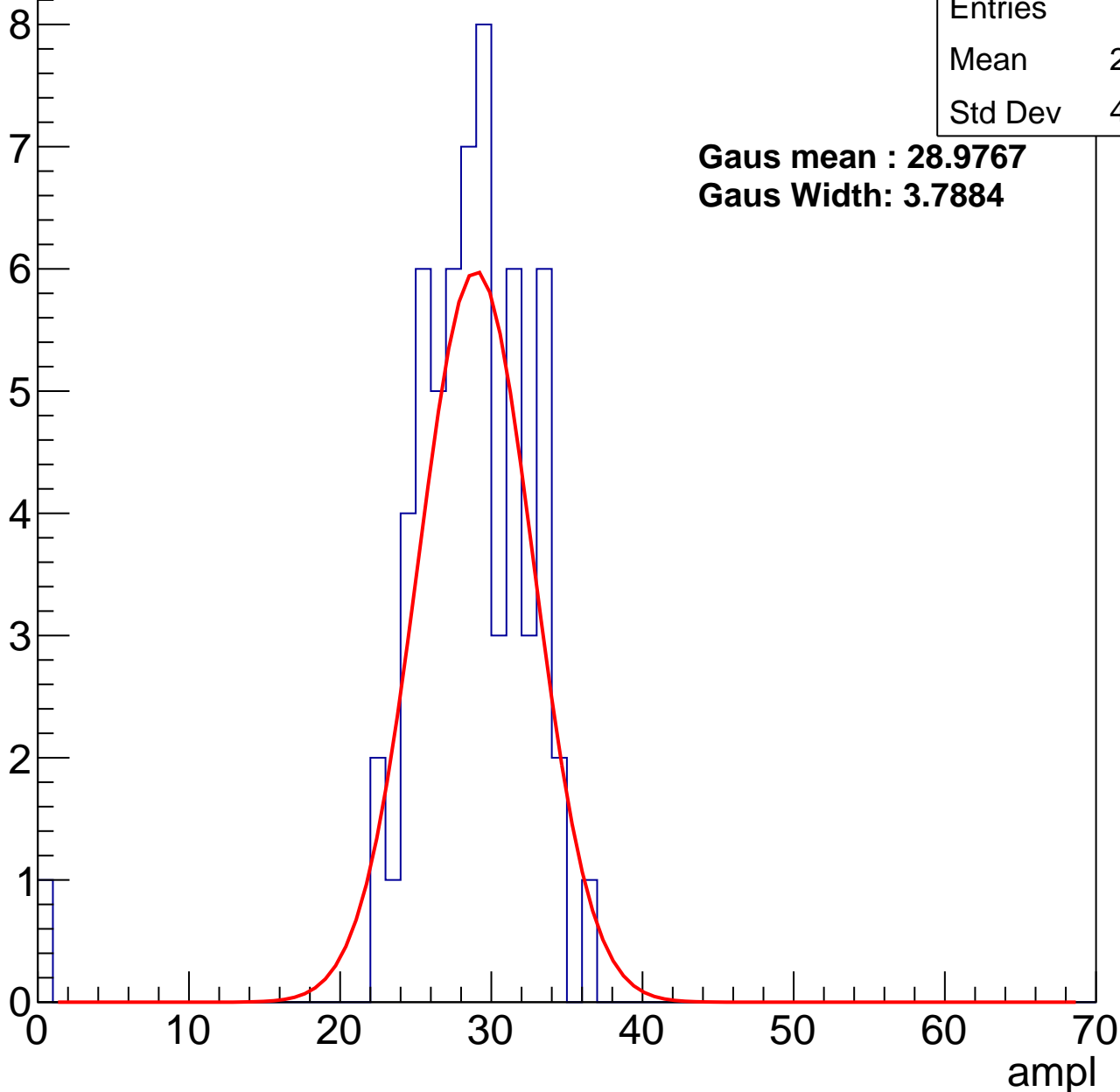
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	27.98
Std Dev	4.847

**Gaus mean : 28.9767**

**Gaus Width: 3.7884**



# B1L003S, U3-ch97, adc1

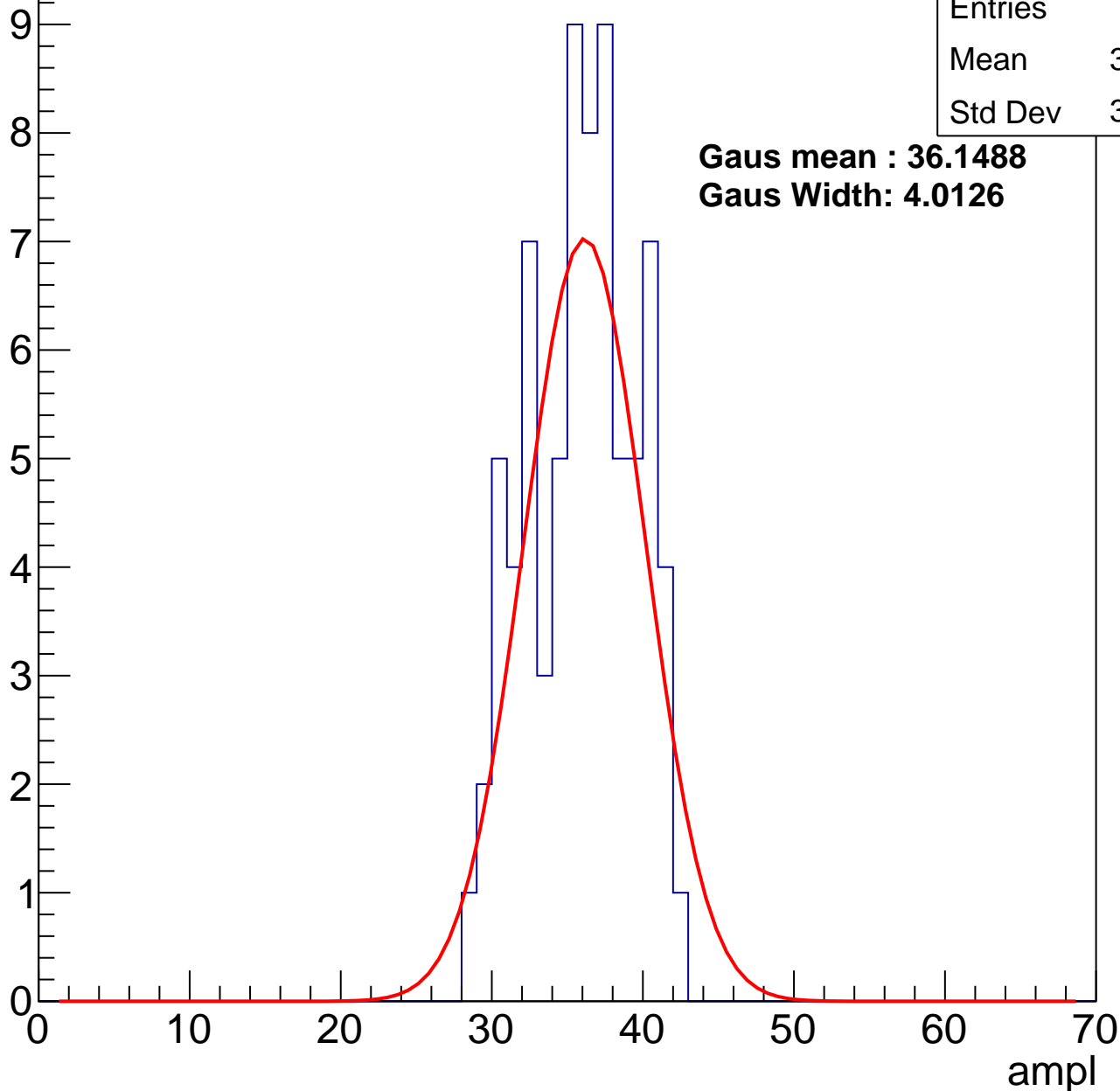
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	75
Mean	35.47
Std Dev	3.485

**Gaus mean : 36.1488**

**Gaus Width: 4.0126**



# B1L003S, U3-ch97, adc2

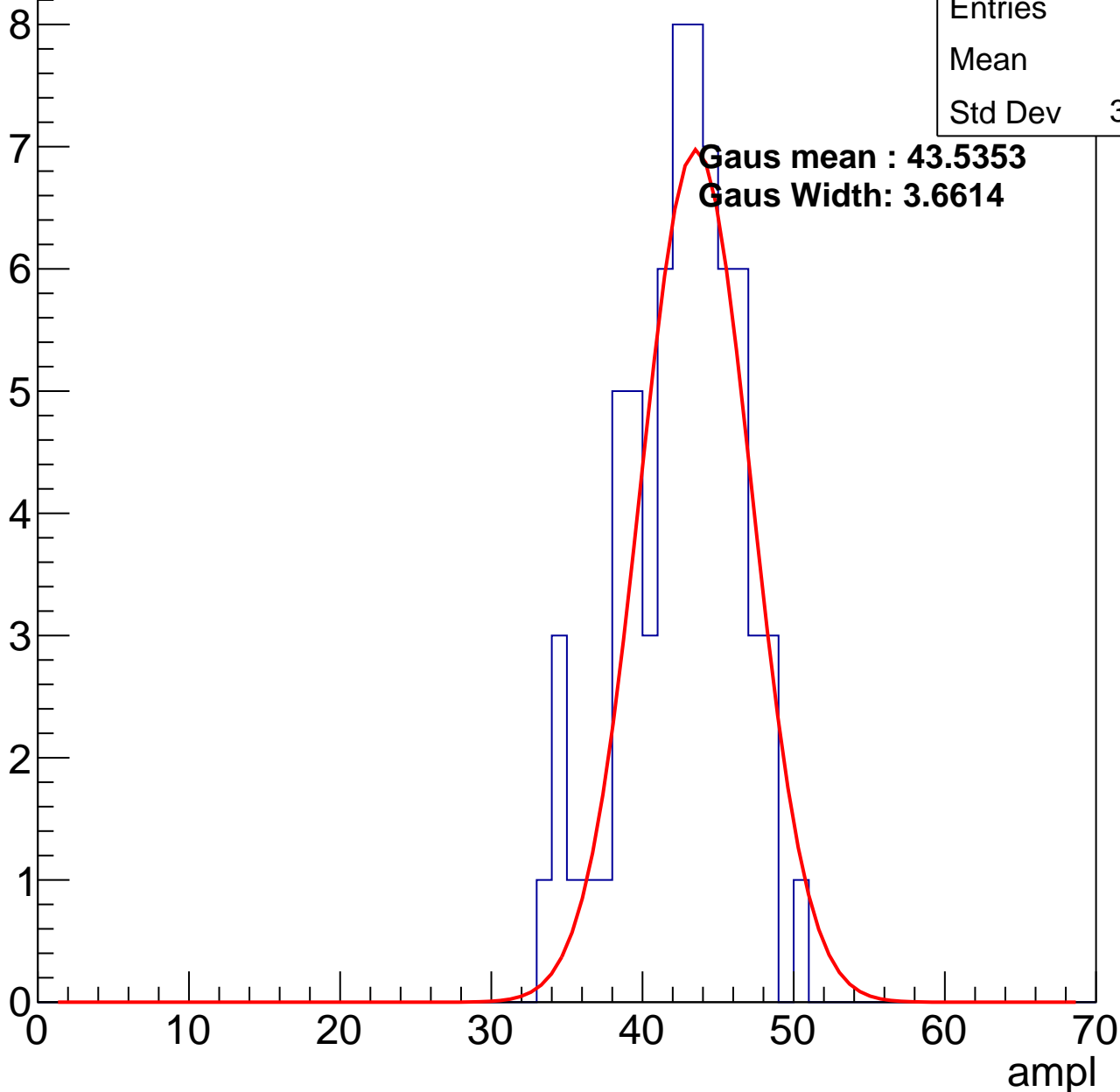
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	42.1
Std Dev	3.754

**Gaus mean : 43.5353**

**Gaus Width: 3.6614**

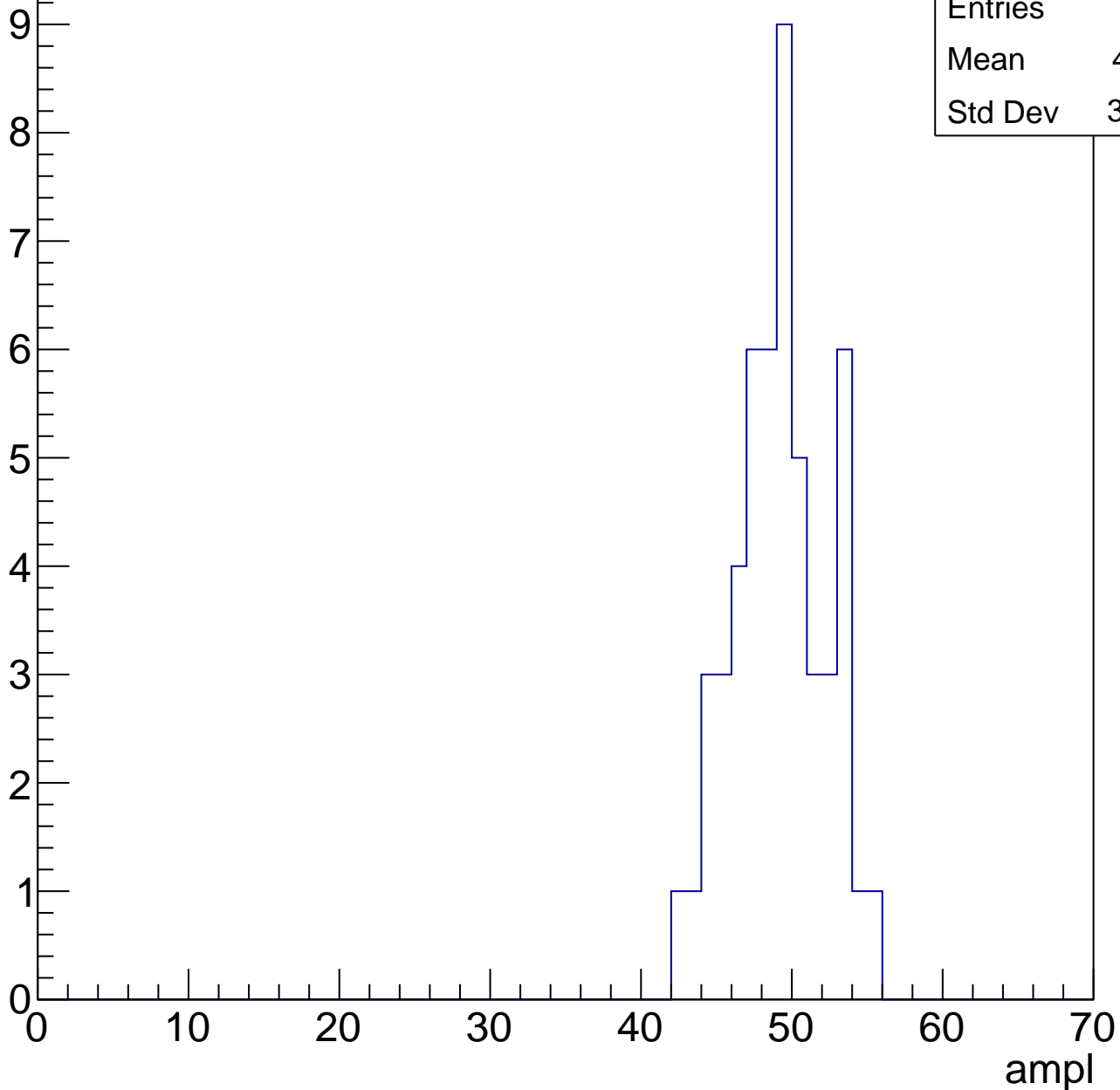


# B1L003S, U3-ch97, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	52
Mean	48.71
Std Dev	3.009

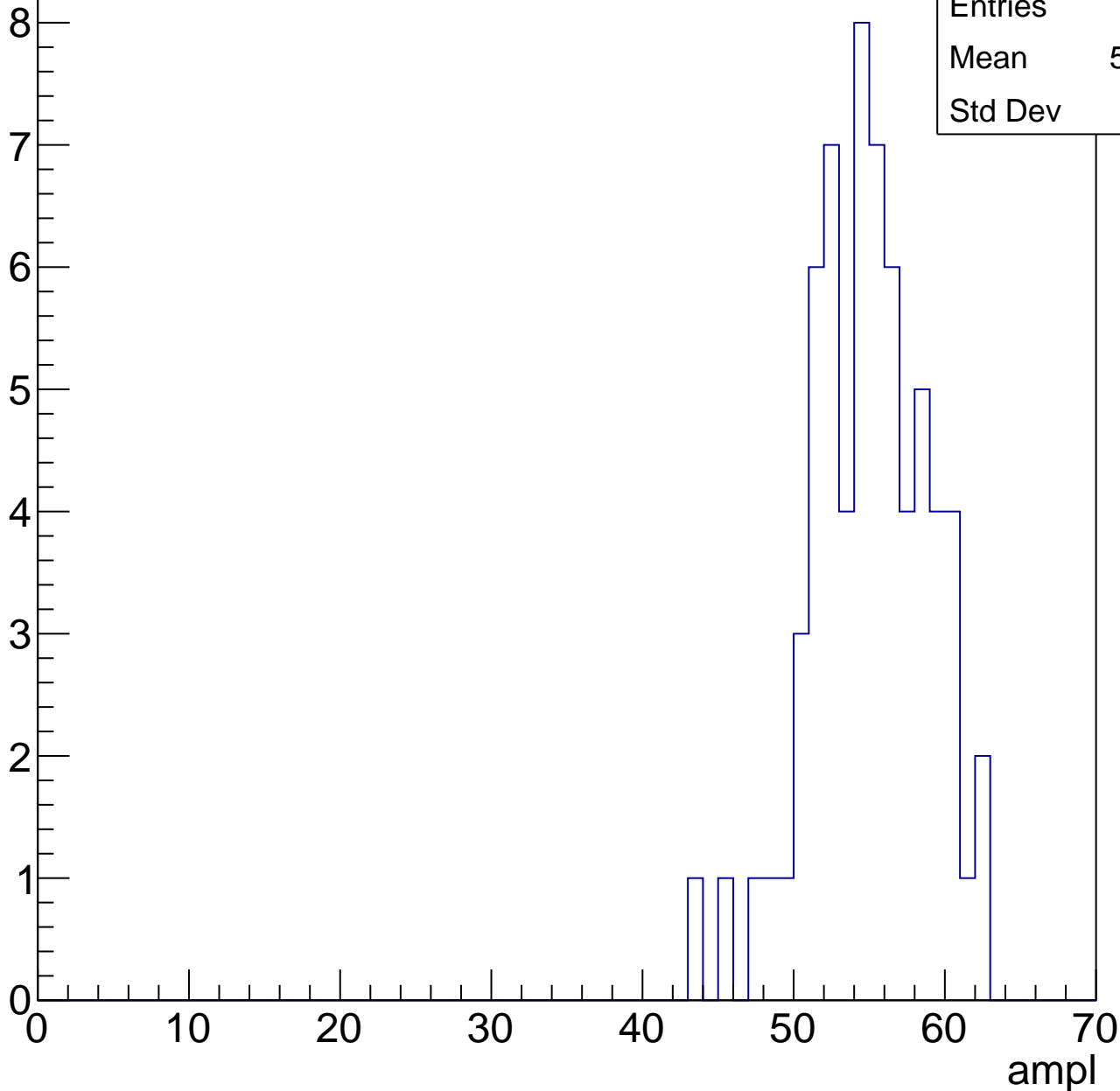


# B1L003S, U3-ch97, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	54.48
Std Dev	3.89

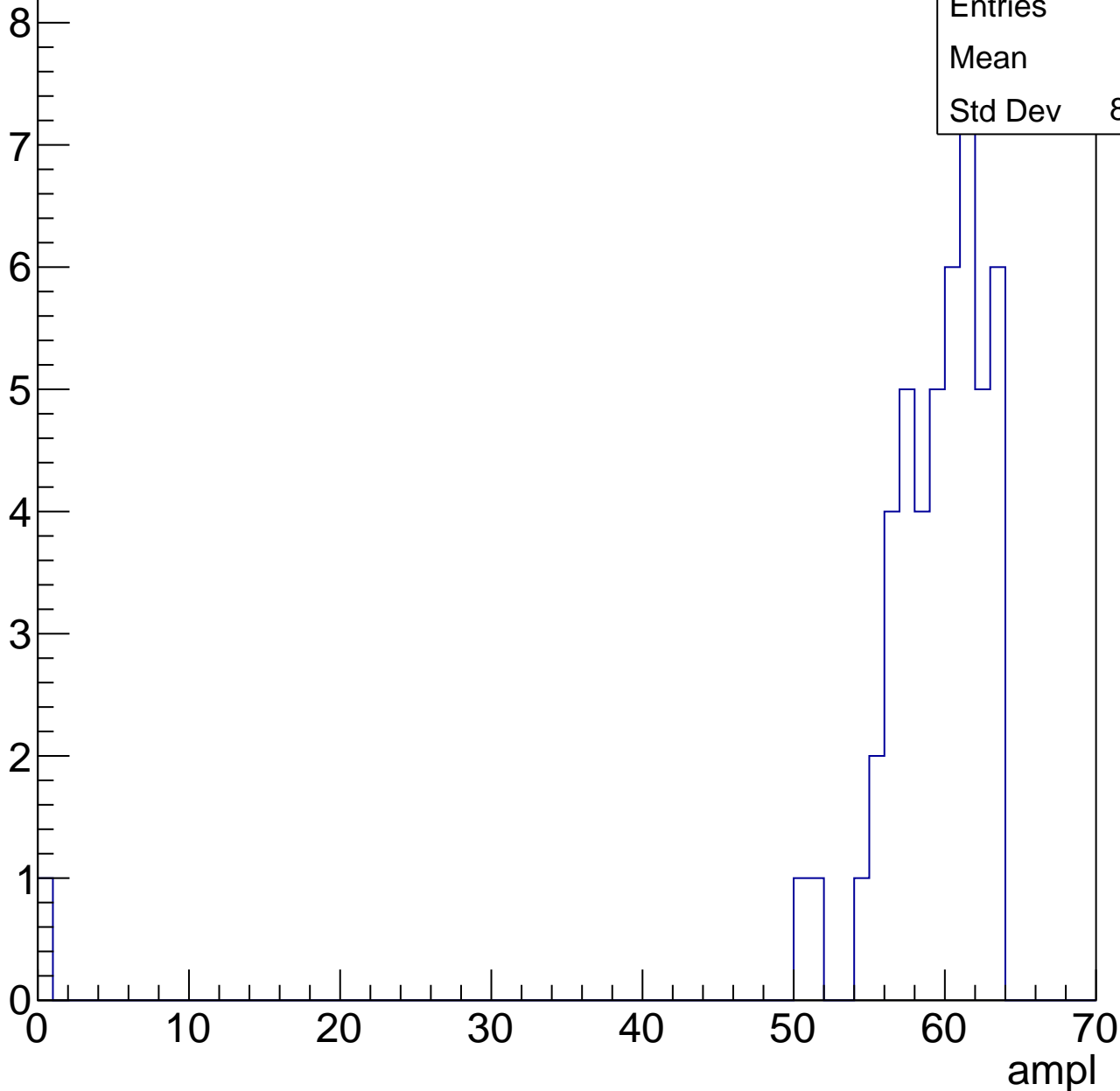


# B1L003S, U3-ch97, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

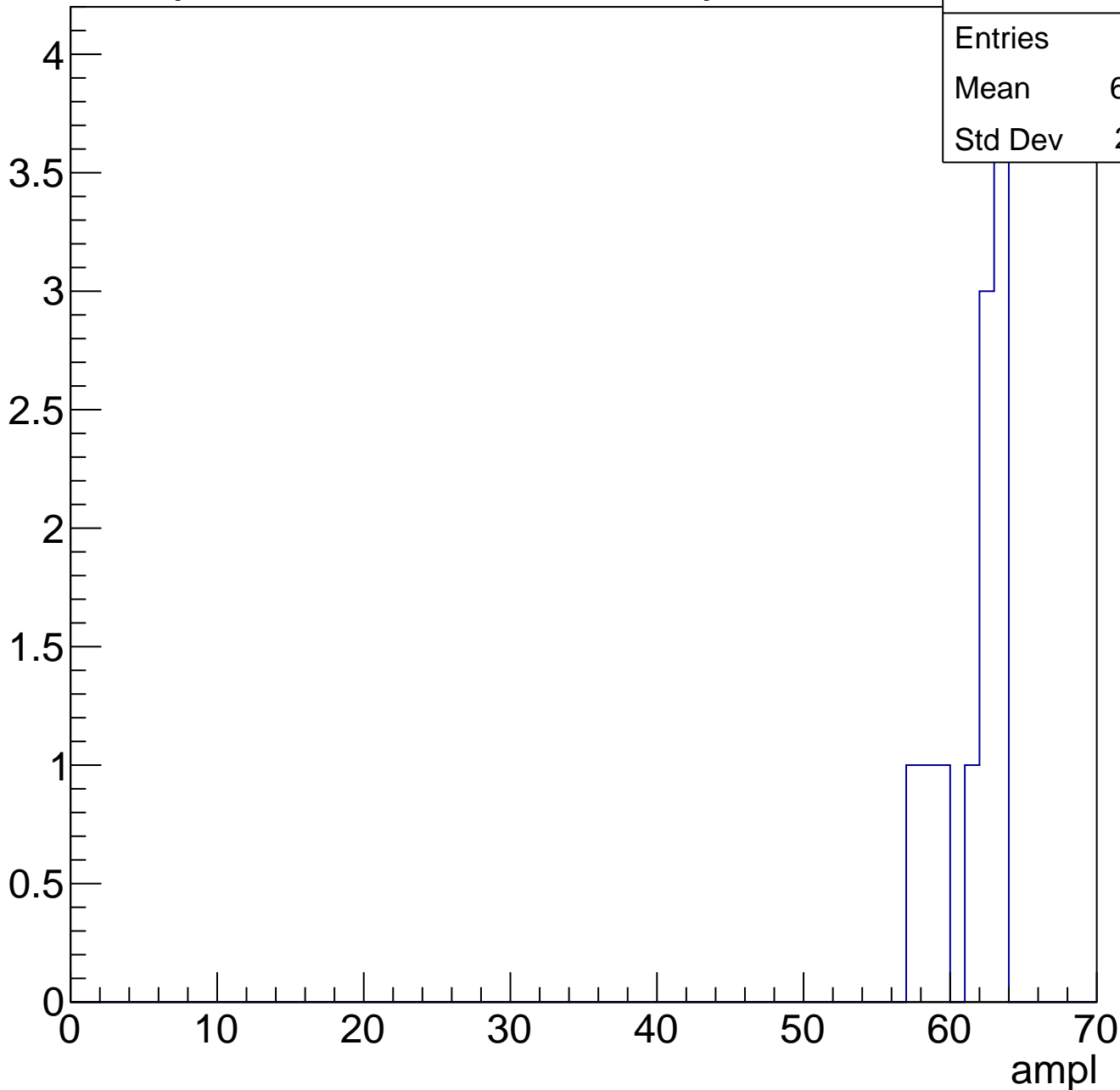
Entries	49
Mean	57.9
Std Dev	8.878



# B1L003S, U3-ch97, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch97, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U3-ch98, adc0

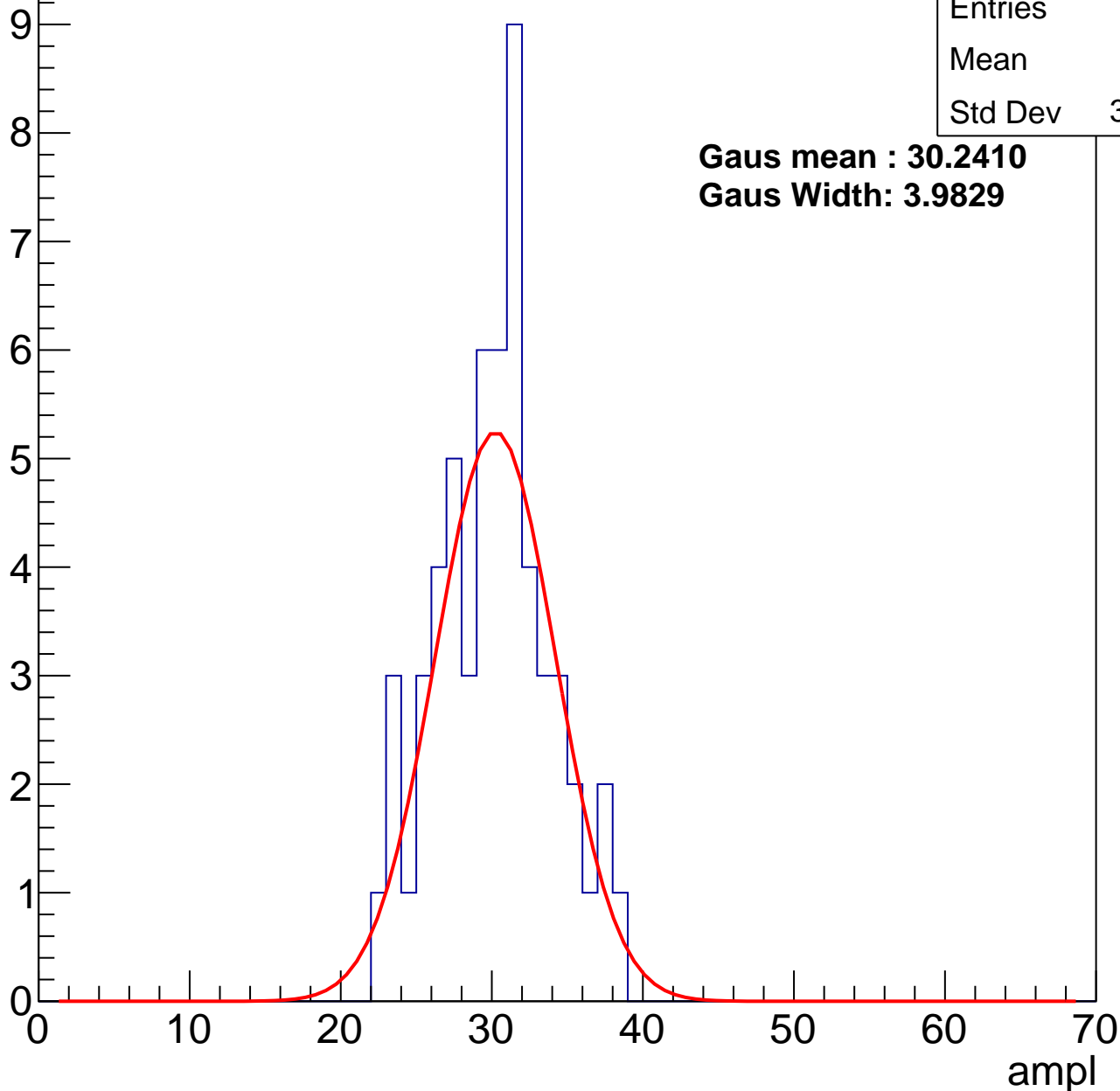
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	29.7
Std Dev	3.727

**Gaus mean : 30.2410**

**Gaus Width: 3.9829**



# B1L003S, U3-ch98, adc1

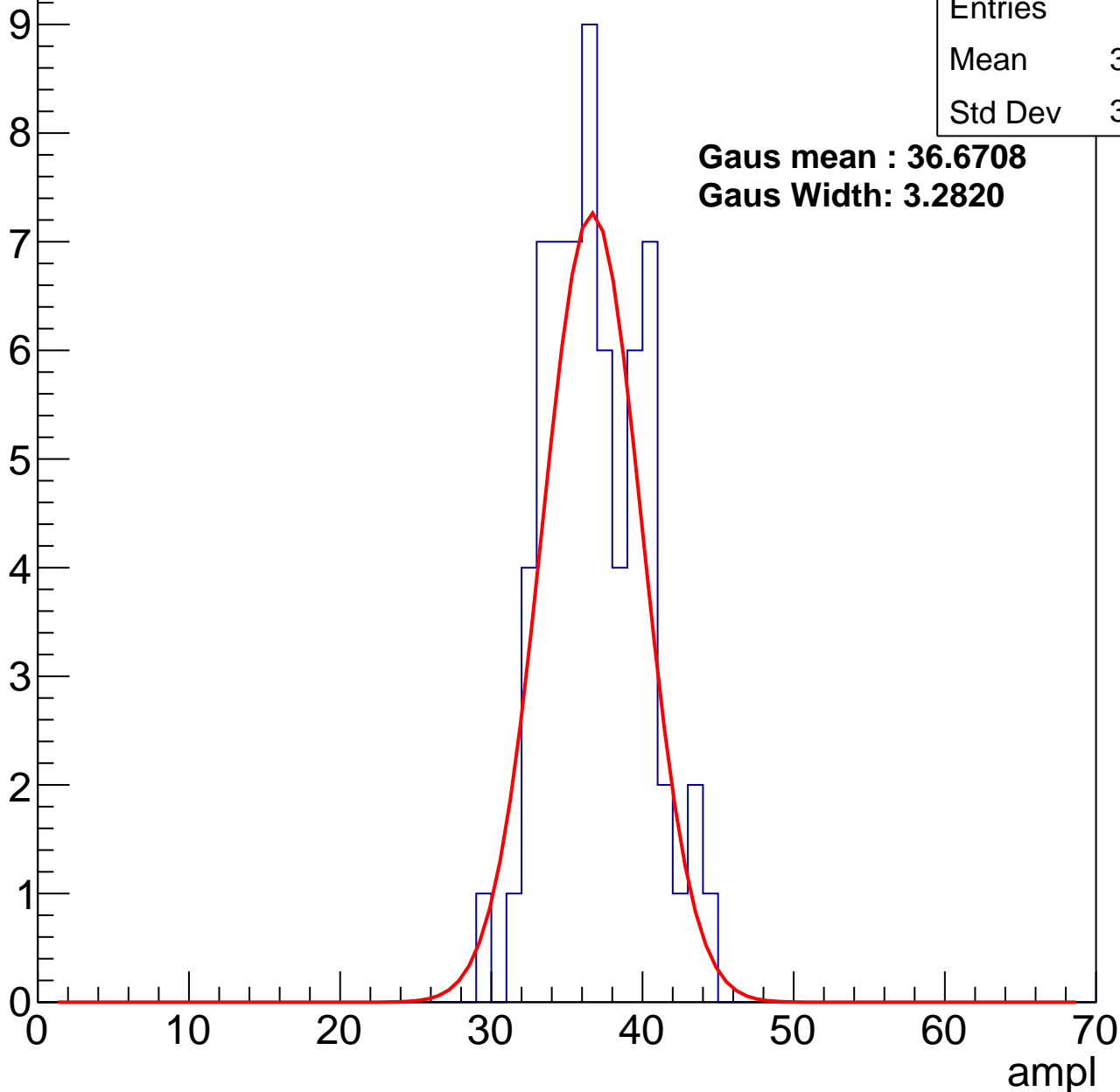
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	36.43
Std Dev	3.186

**Gaus mean : 36.6708**

**Gaus Width: 3.2820**



# B1L003S, U3-ch98, adc2

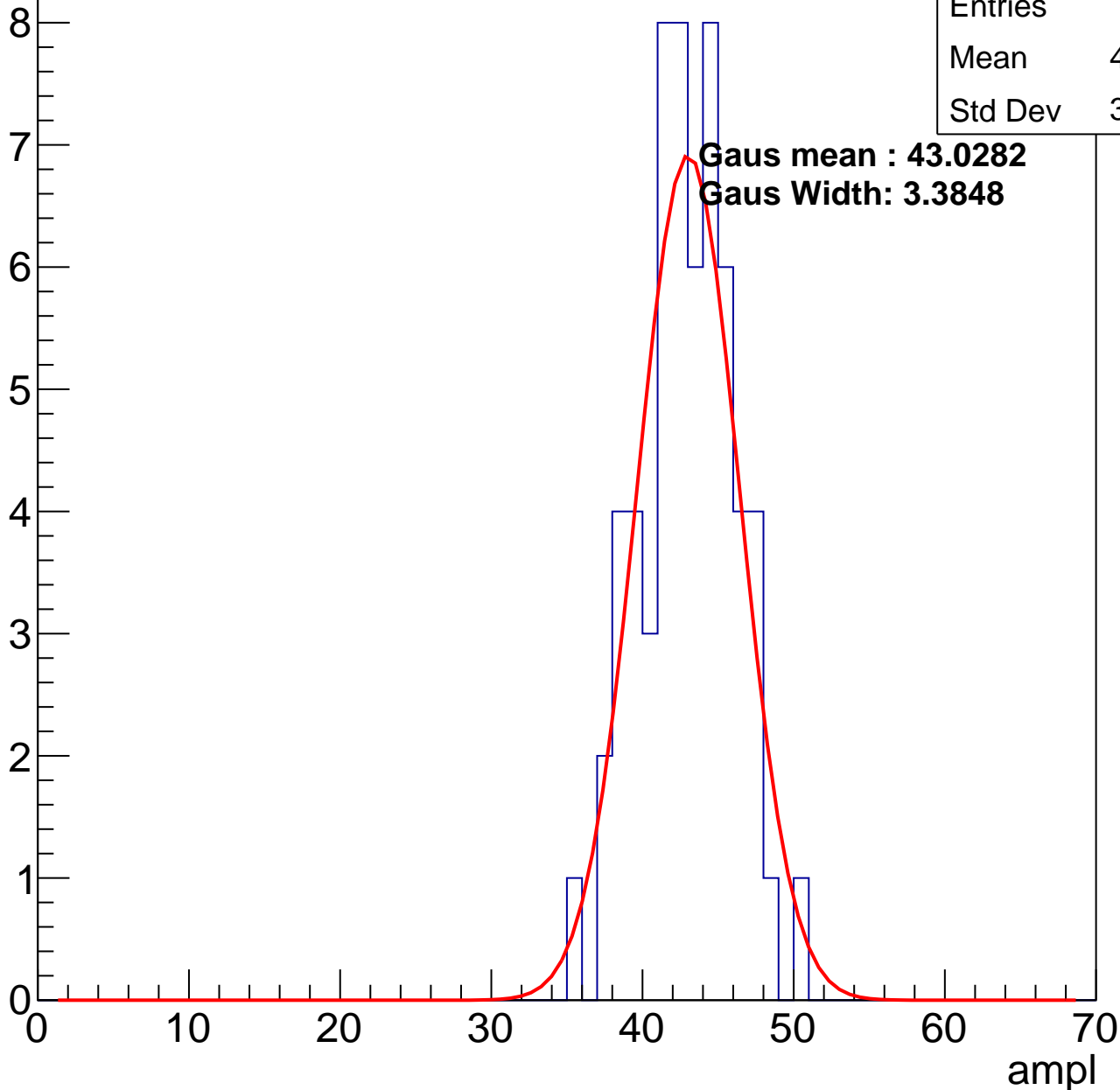
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	42.52
Std Dev	3.052

**Gaus mean : 43.0282**

**Gaus Width: 3.3848**

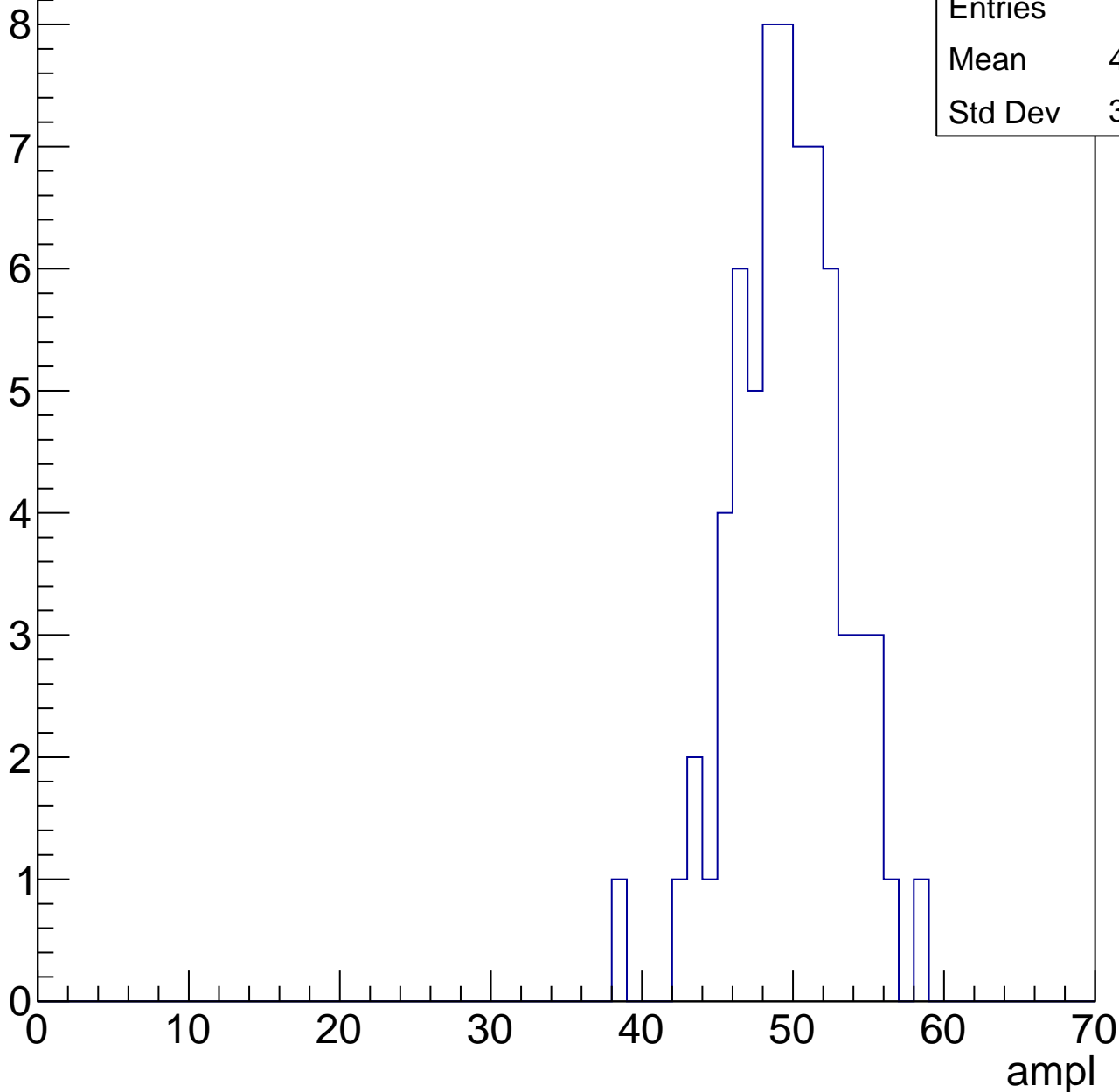


# B1L003S, U3-ch98, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	49.19
Std Dev	3.584

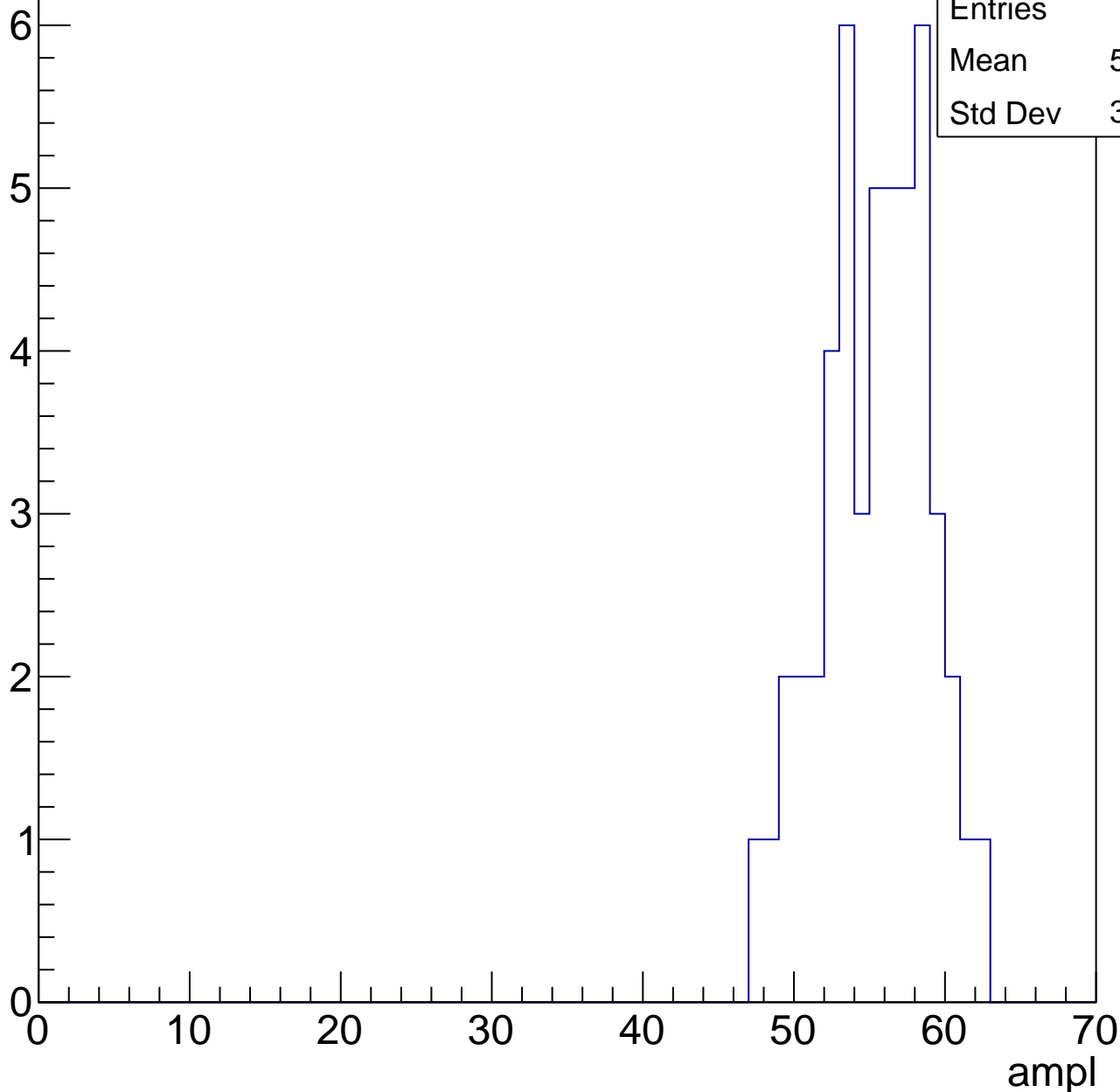


# B1L003S, U3-ch98, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	49
Mean	54.92
Std Dev	3.475

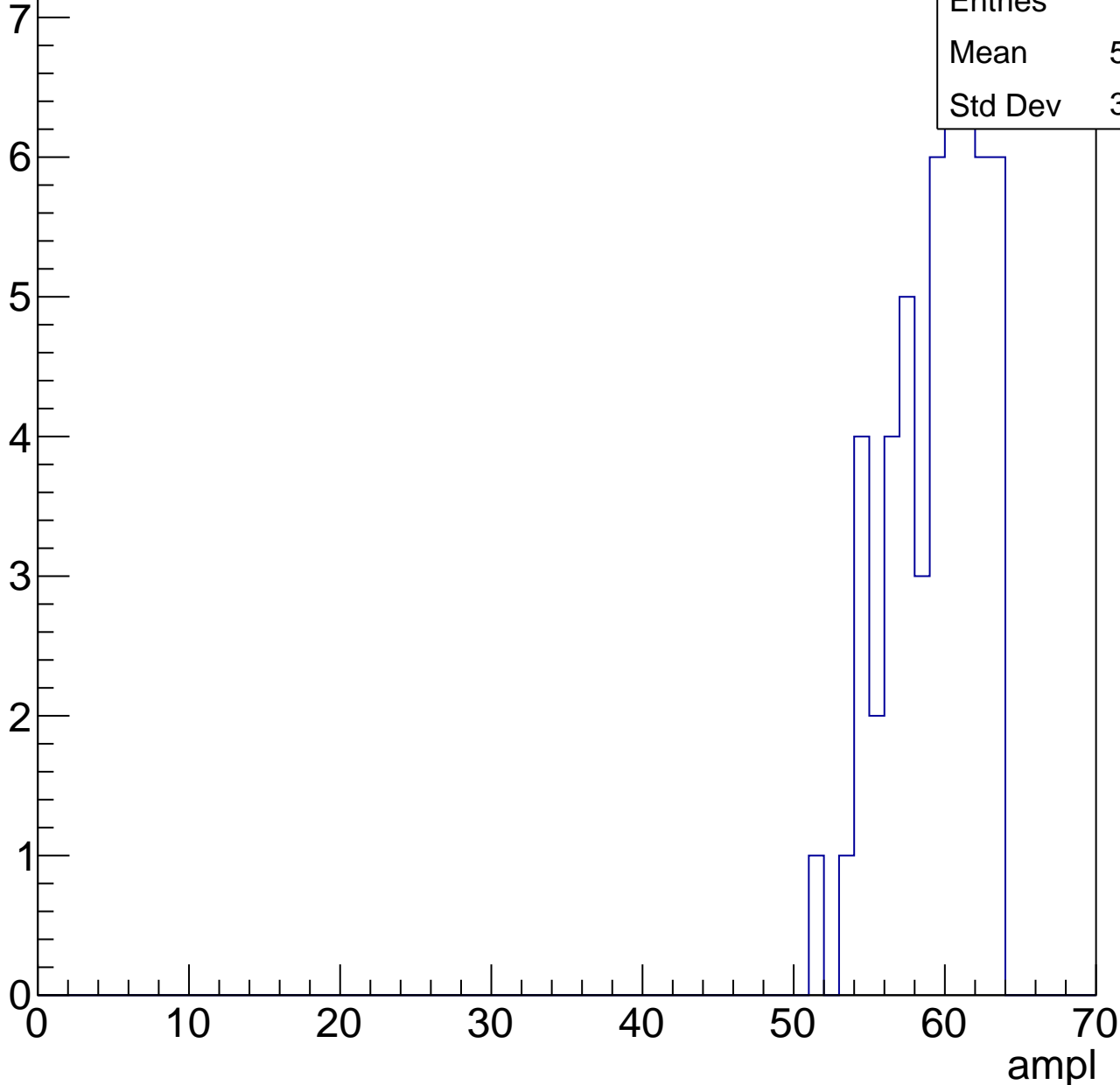


# B1L003S, U3-ch98, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

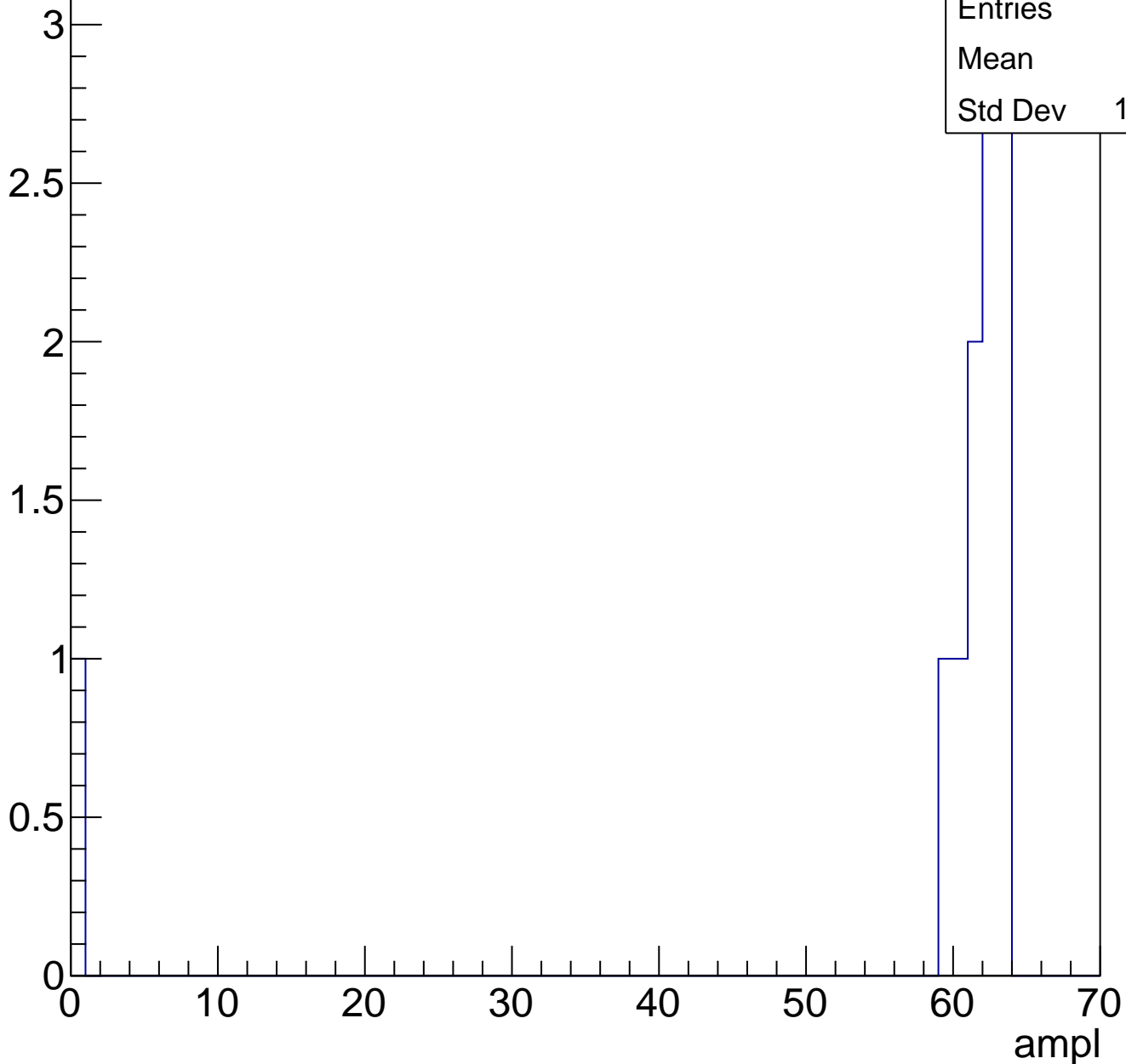
Entries	52
Mean	58.92
Std Dev	3.025



# B1L003S, U3-ch98, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

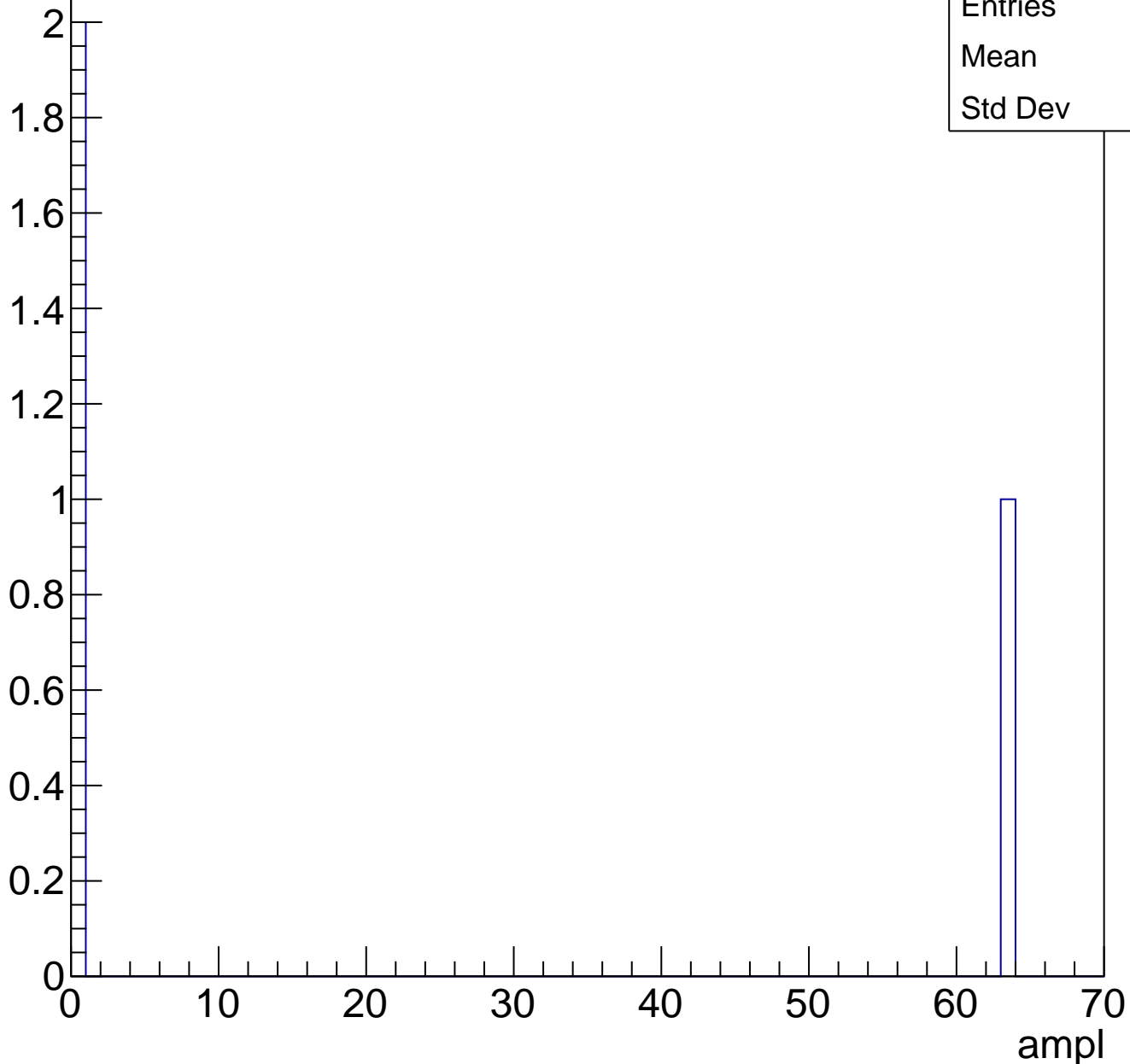




# B1L003S, U3-ch98, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	3
Mean	21
Std Dev	29.7

# B1L003S, U3-ch99, adc0

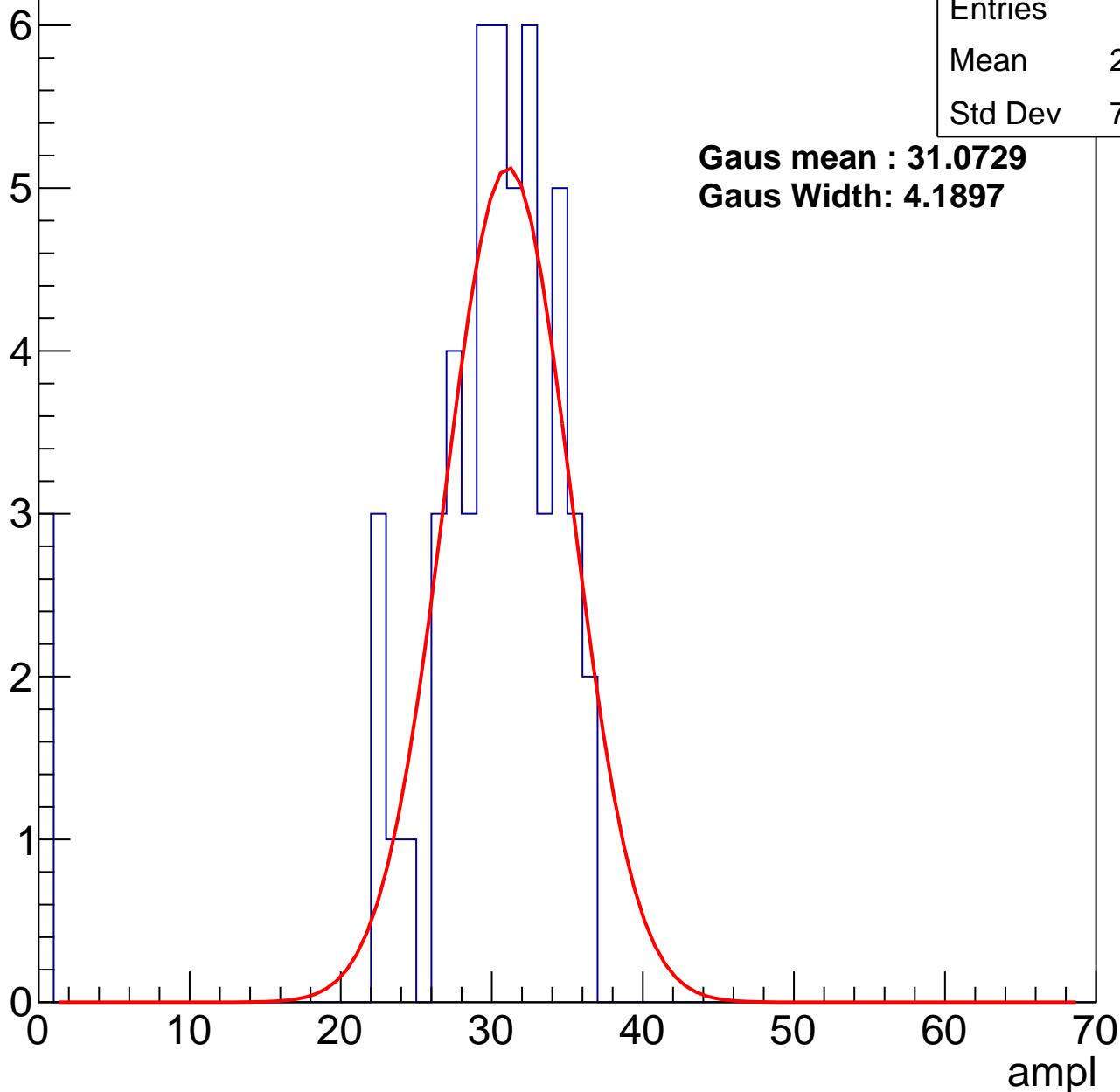
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	54
Mean	28.33
Std Dev	7.712

**Gaus mean : 31.0729**

**Gaus Width: 4.1897**



# B1L003S, U3-ch99, adc1

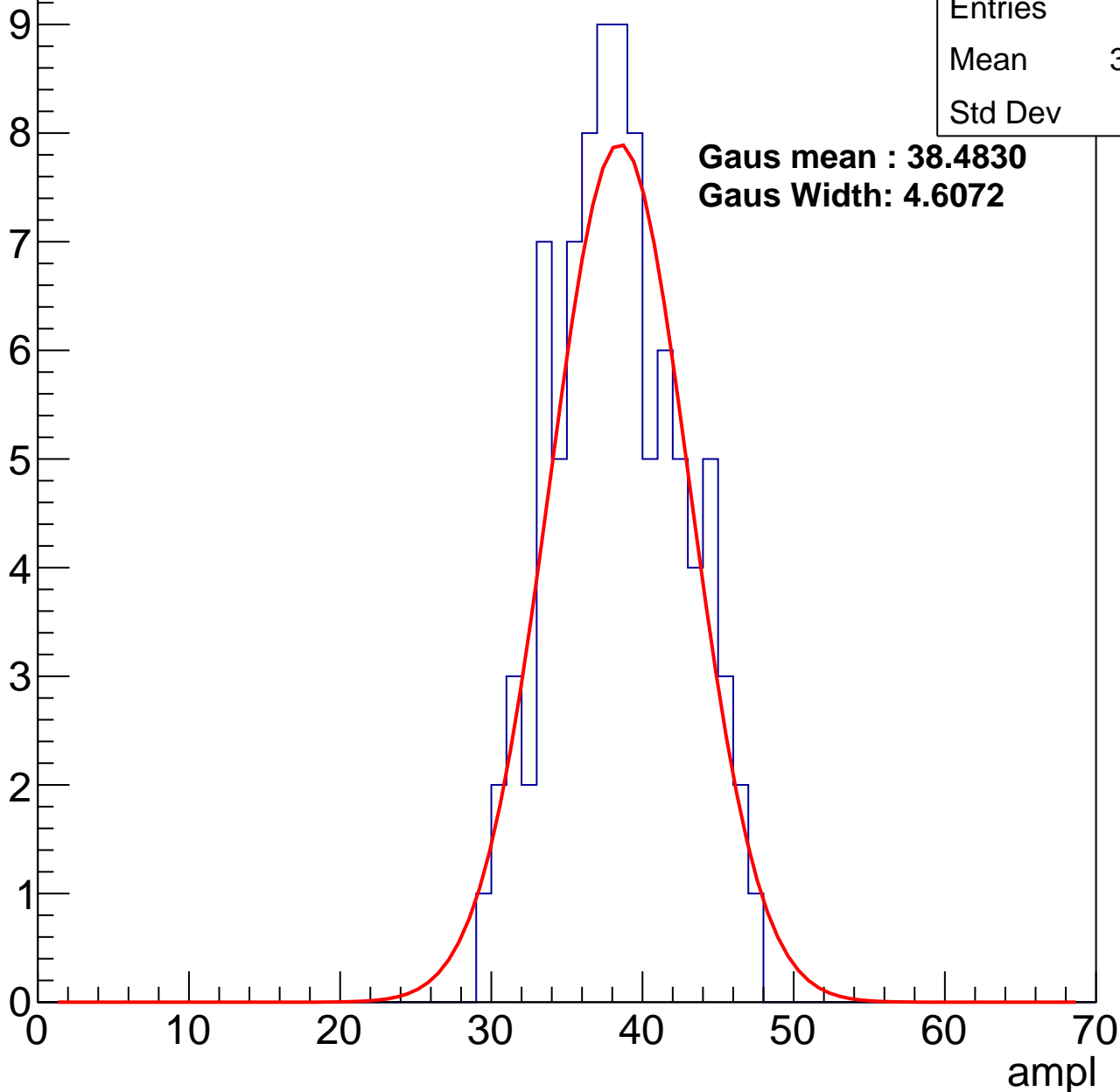
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	92
Mean	37.92
Std Dev	4.15

**Gaus mean : 38.4830**

**Gaus Width: 4.6072**



# B1L003S, U3-ch99, adc2

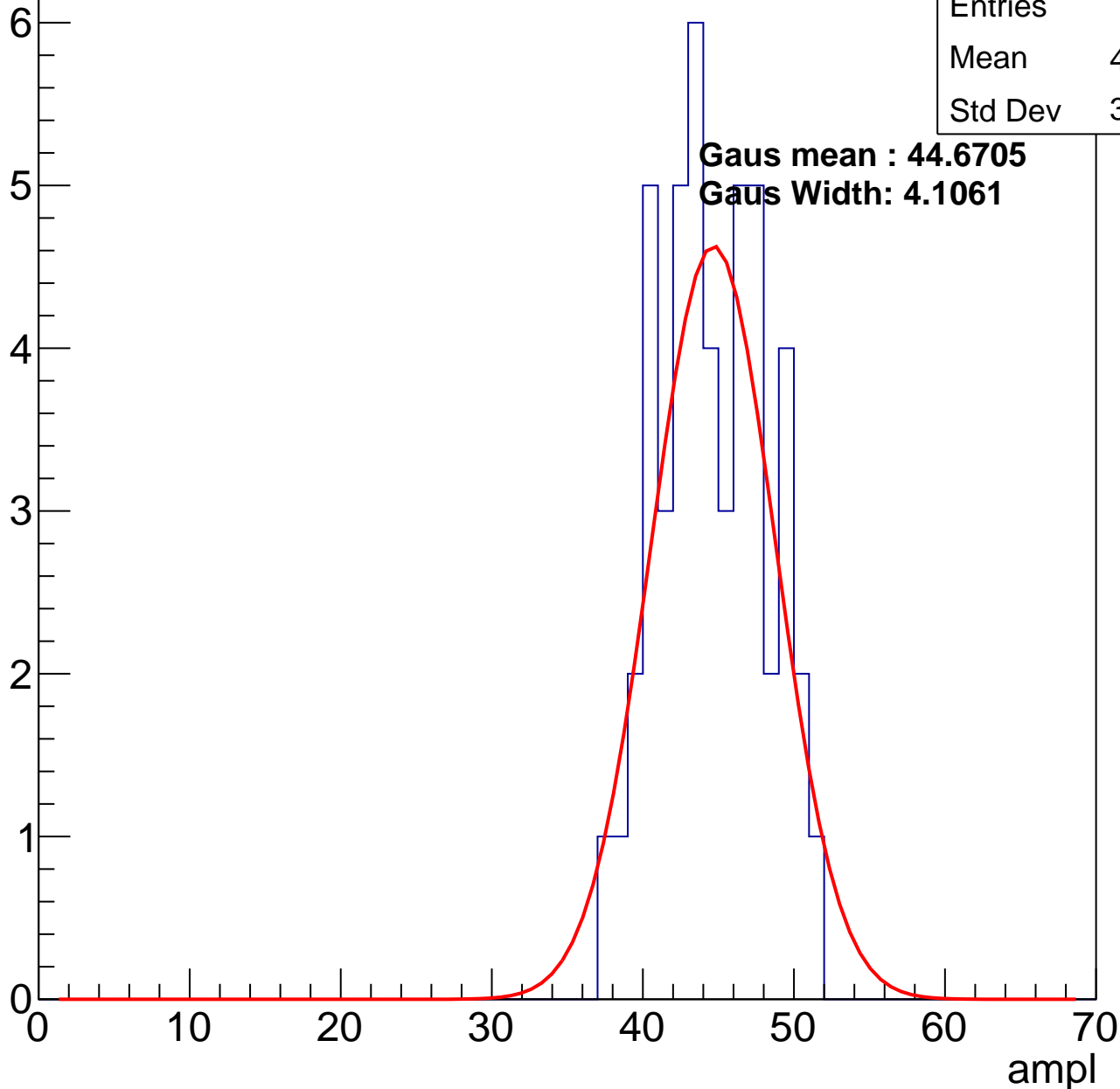
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	49
Mean	44.14
Std Dev	3.464

**Gaus mean : 44.6705**

**Gaus Width: 4.1061**

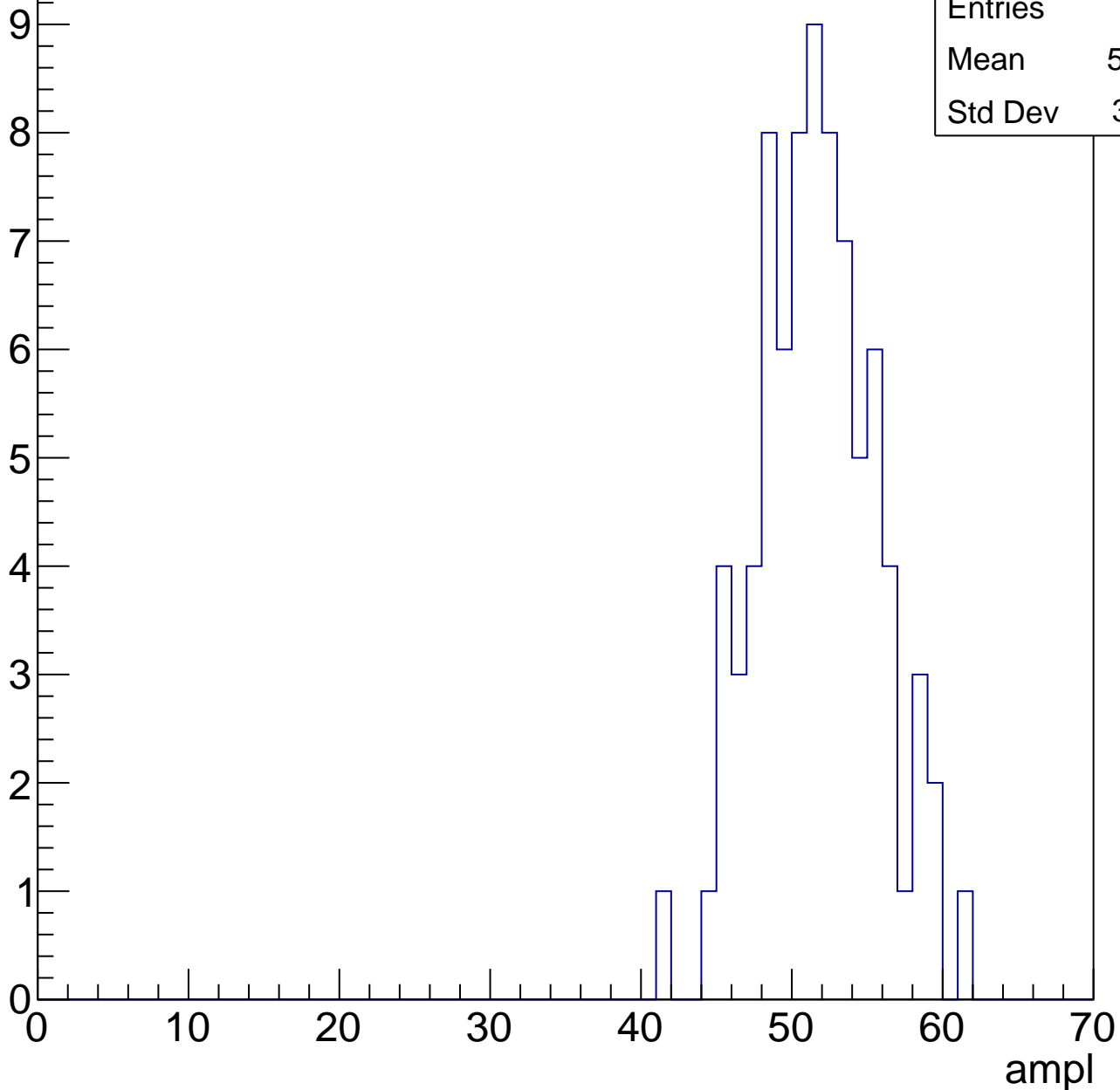


# B1L003S, U3-ch99, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	81
Mean	51.22
Std Dev	3.881

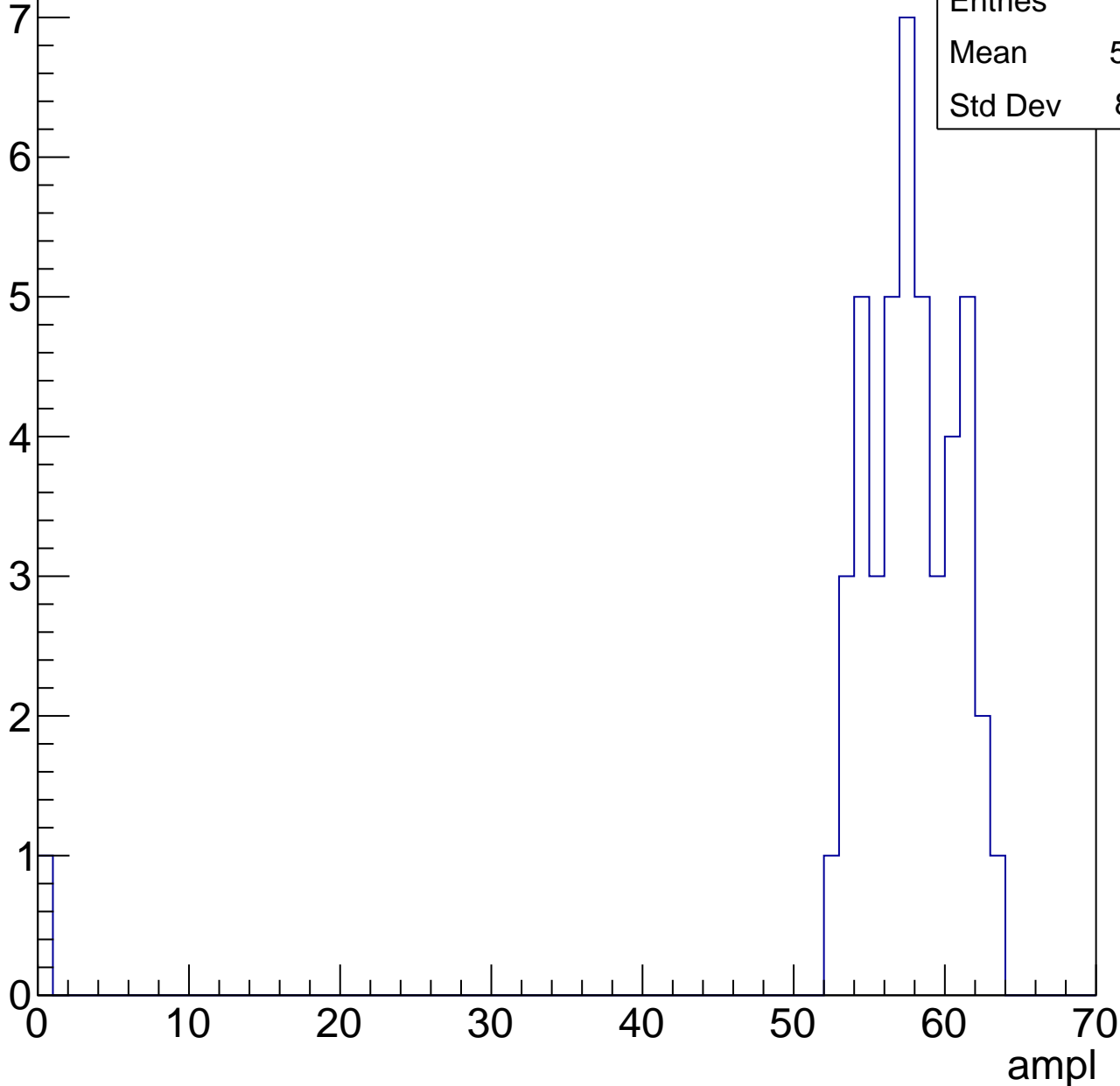


# B1L003S, U3-ch99, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	45
Mean	56.09
Std Dev	8.901

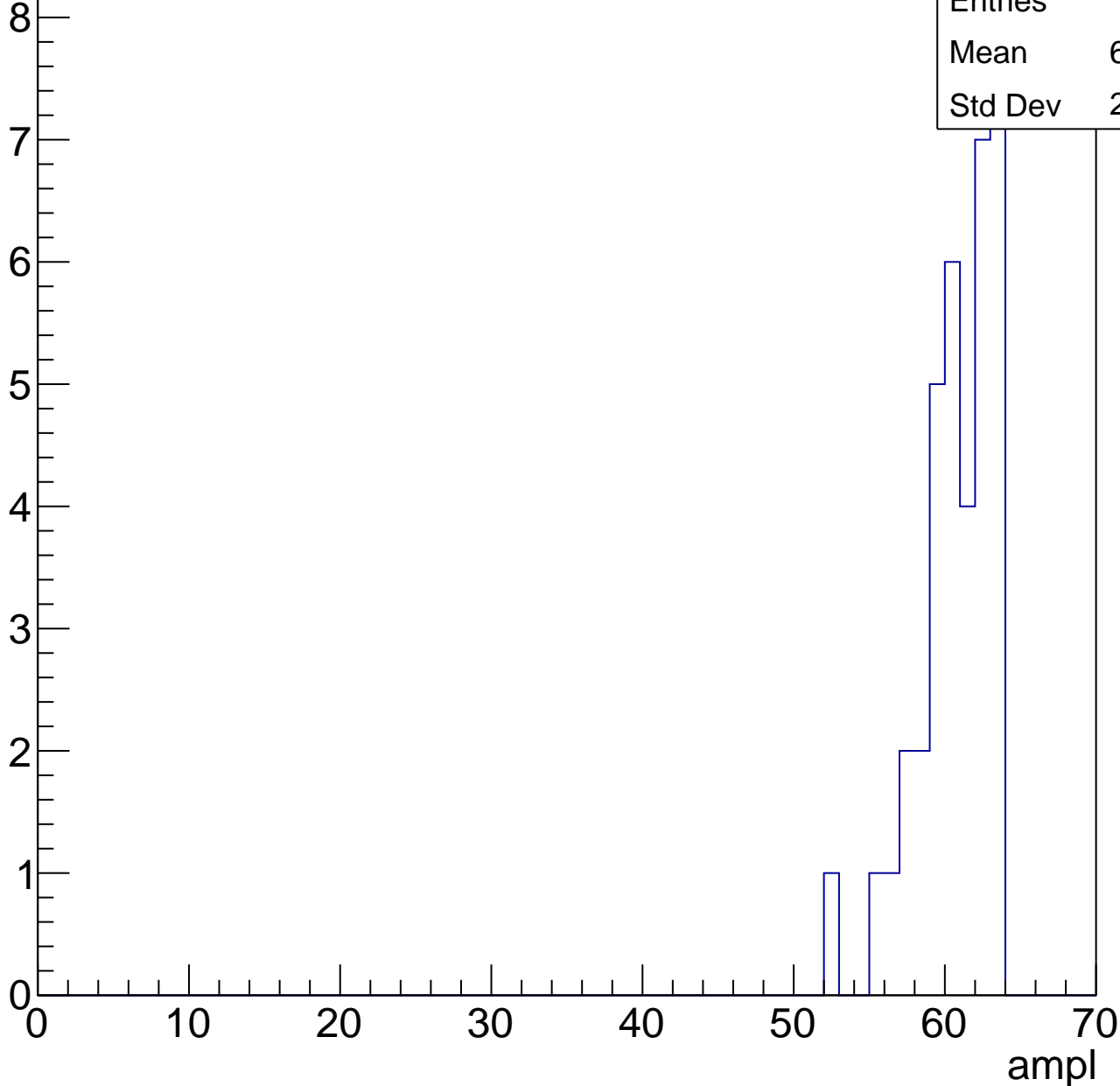


# B1L003S, U3-ch99, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	37
Mean	60.27
Std Dev	2.532



# B1L003S, U3-ch99, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch99, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U3-ch100, adc0

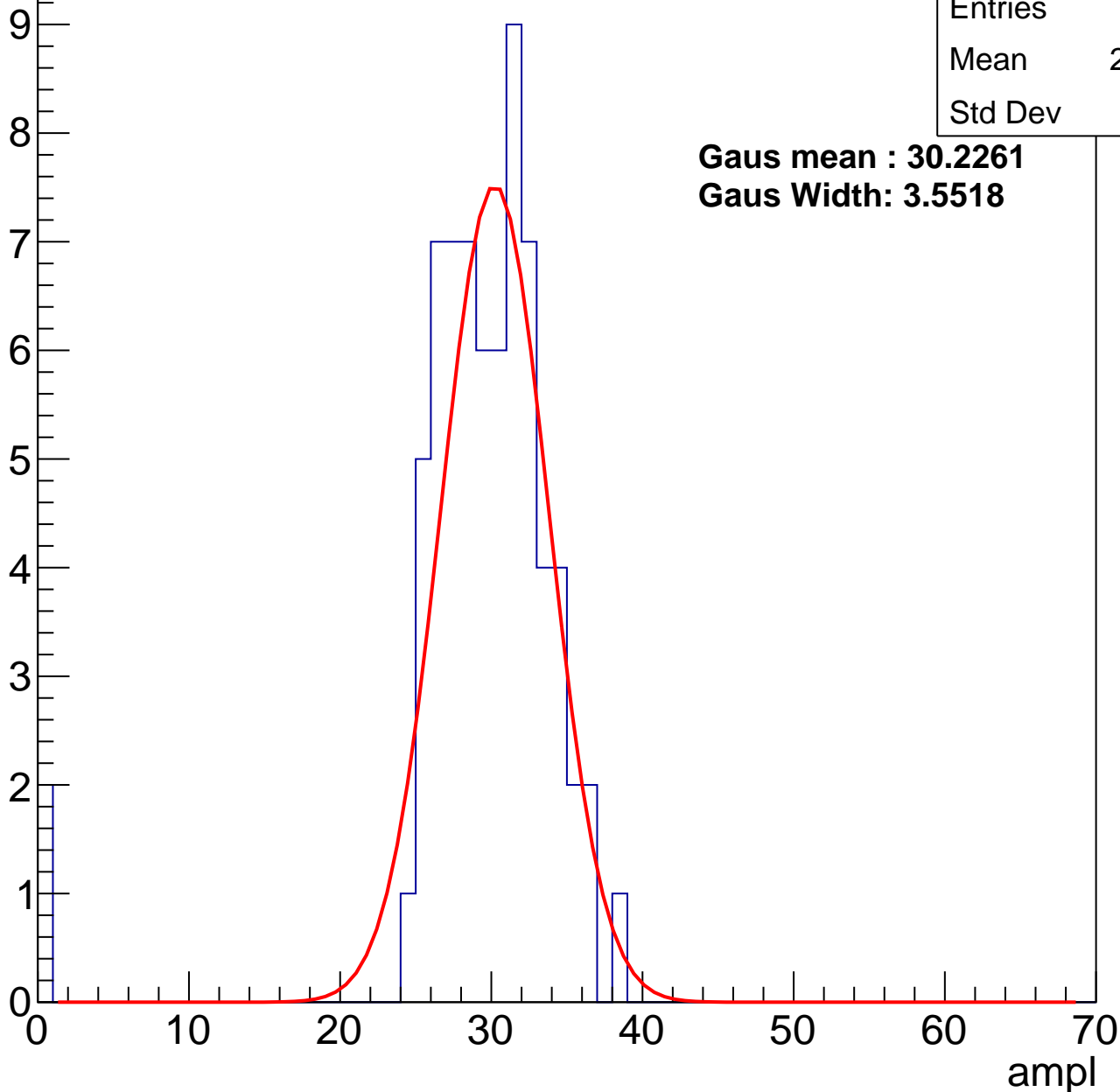
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	28.87
Std Dev	5.86

**Gaus mean : 30.2261**

**Gaus Width: 3.5518**



# B1L003S, U3-ch100, adc1

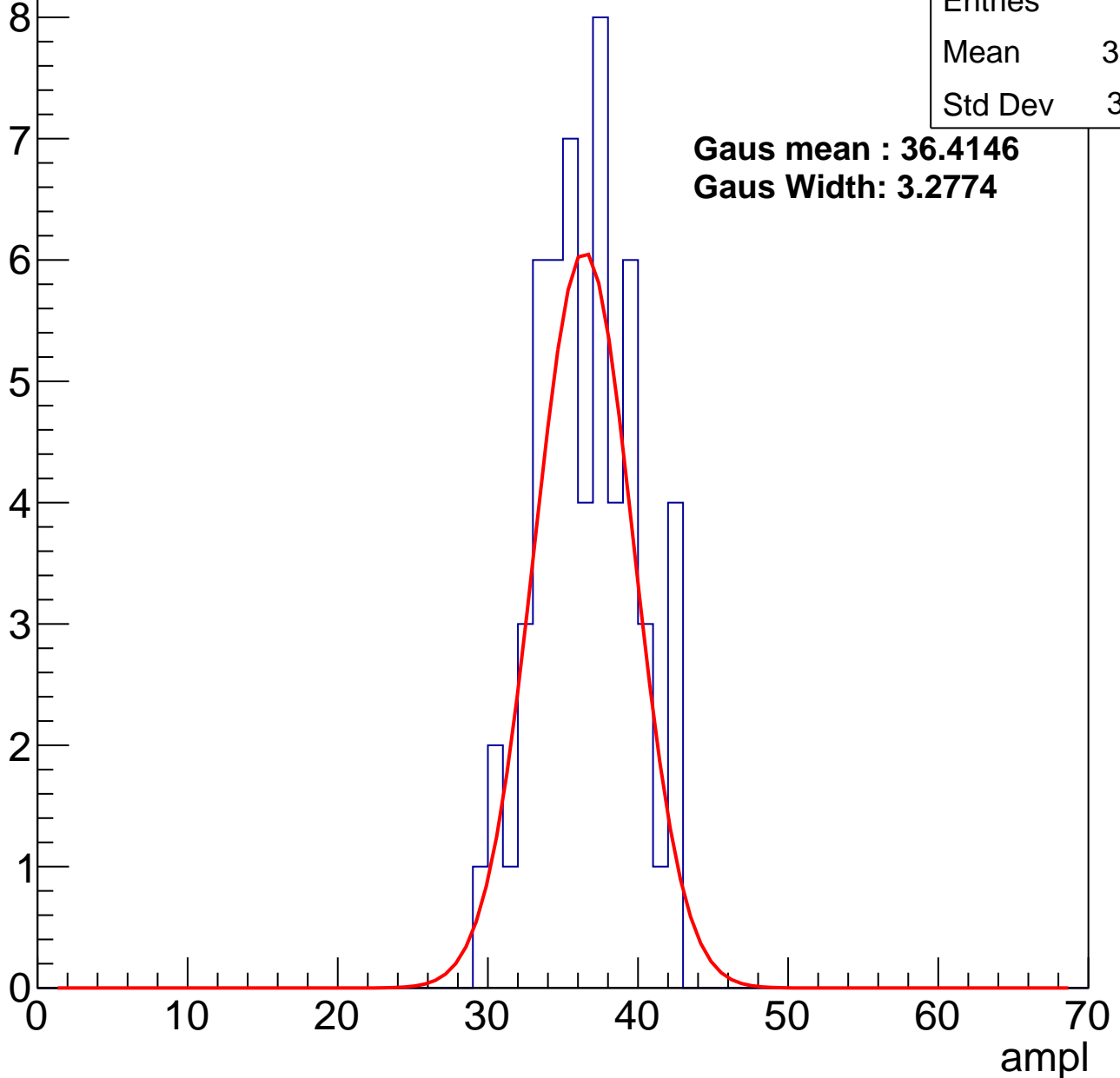
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	36.04
Std Dev	3.201

**Gaus mean : 36.4146**

**Gaus Width: 3.2774**



# B1L003S, U3-ch100, adc2

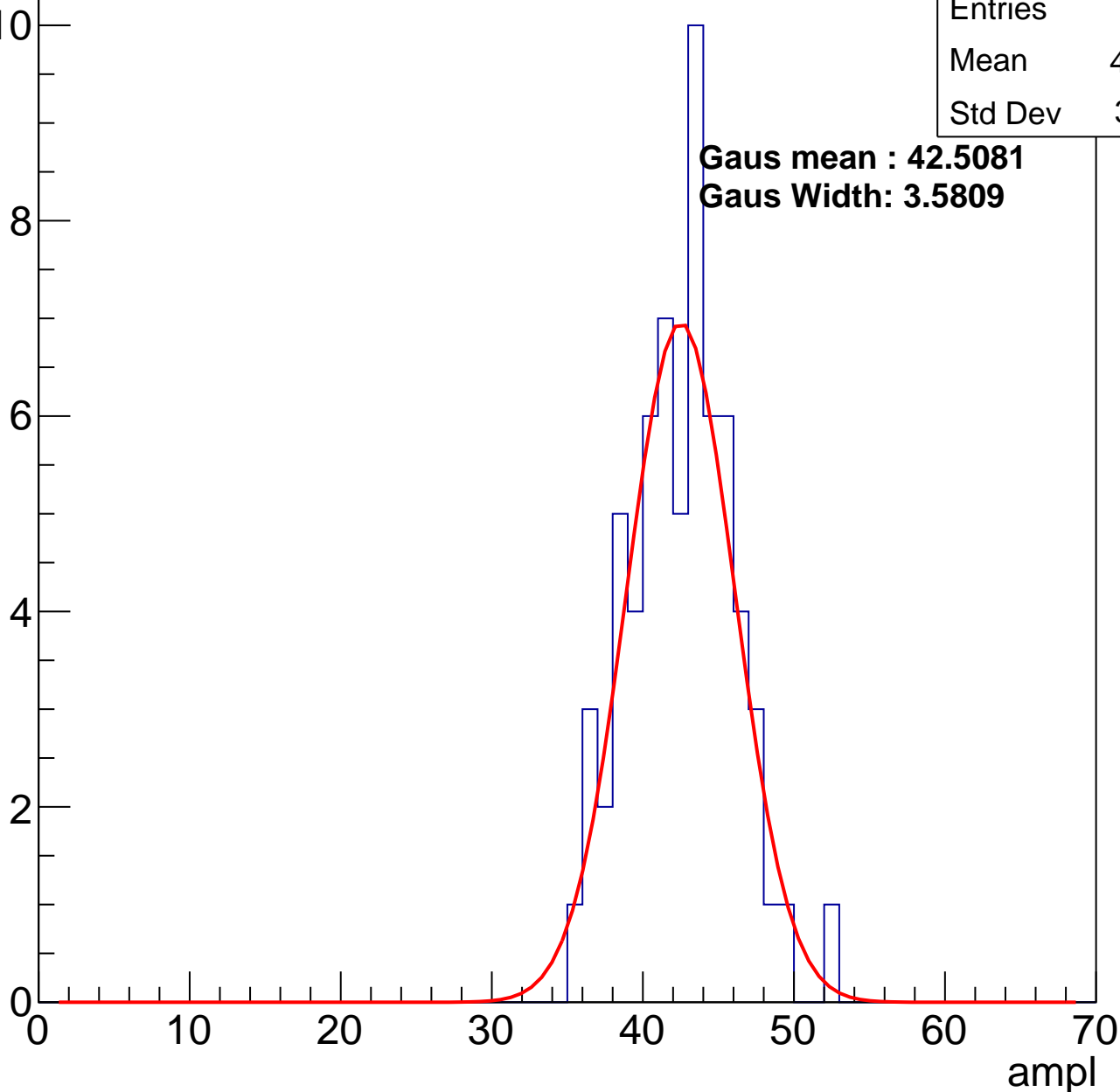
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	42.12
Std Dev	3.431

**Gaus mean : 42.5081**

**Gaus Width: 3.5809**

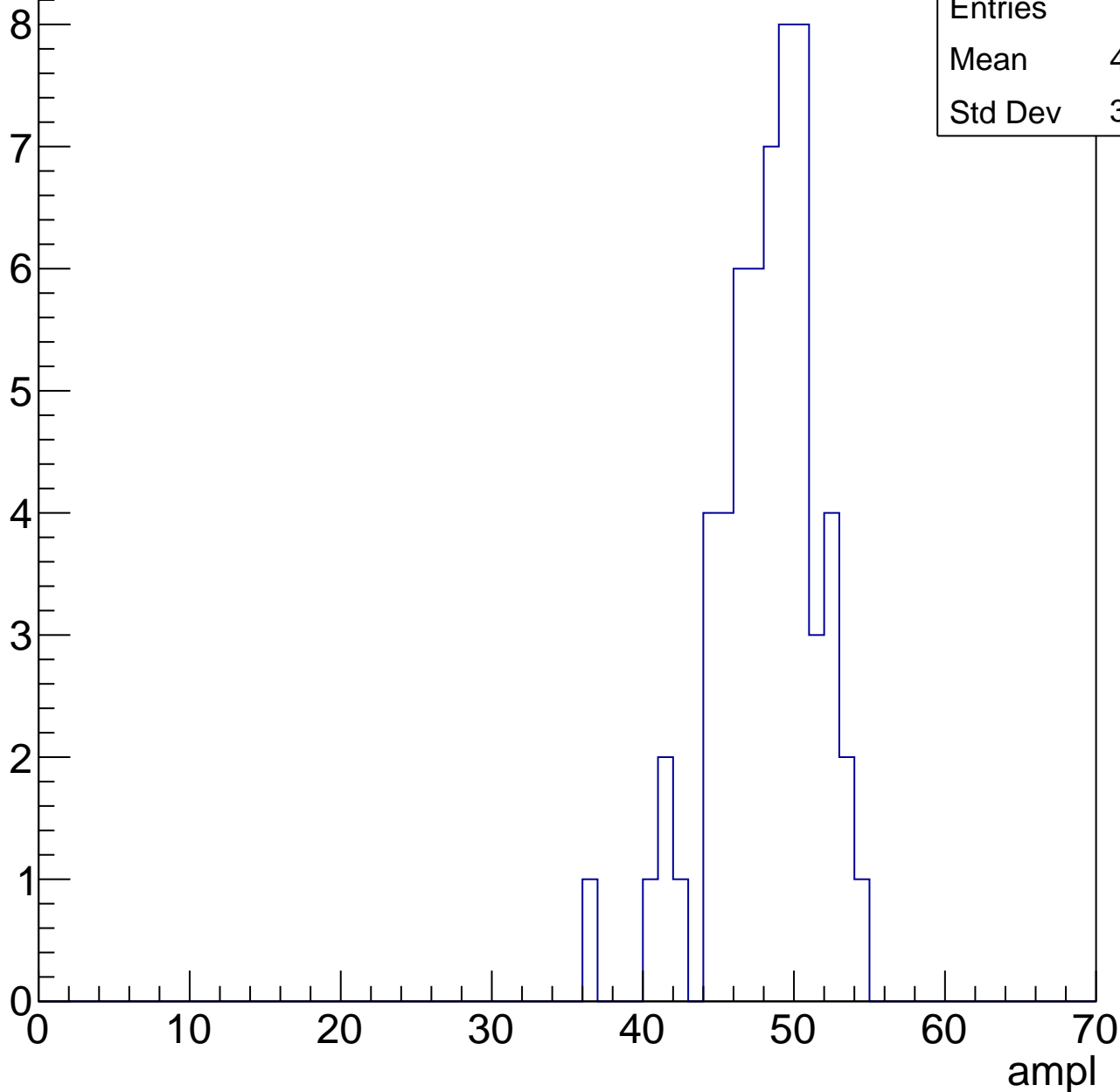


# B1L003S, U3-ch100, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	47.64
Std Dev	3.428

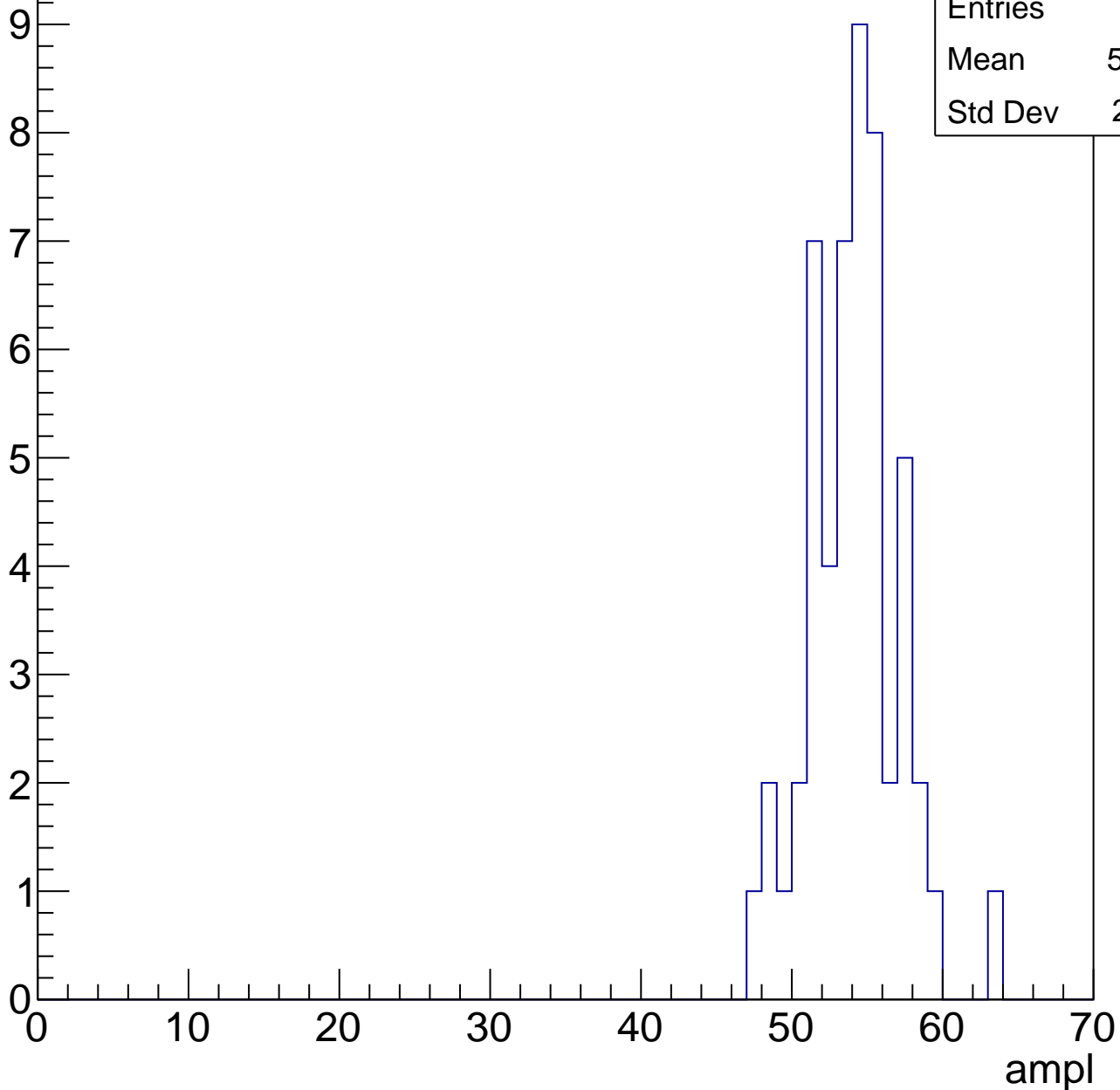


# B1L003S, U3-ch100, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	52
Mean	53.63
Std Dev	2.961

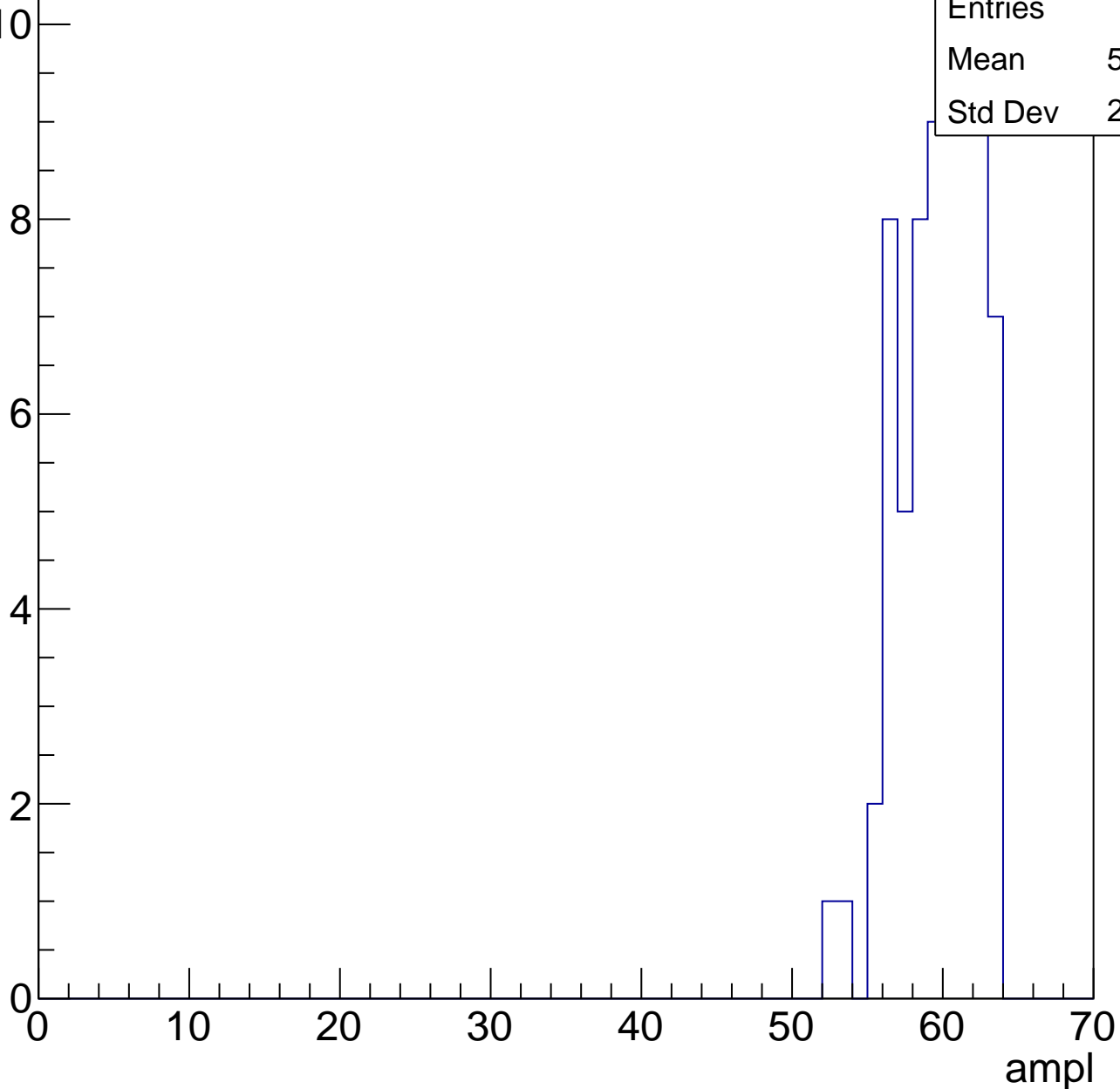


# B1L003S, U3-ch100, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	71
Mean	59.35
Std Dev	2.546



# B1L003S, U3-ch100, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch100, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U3-ch101, adc0

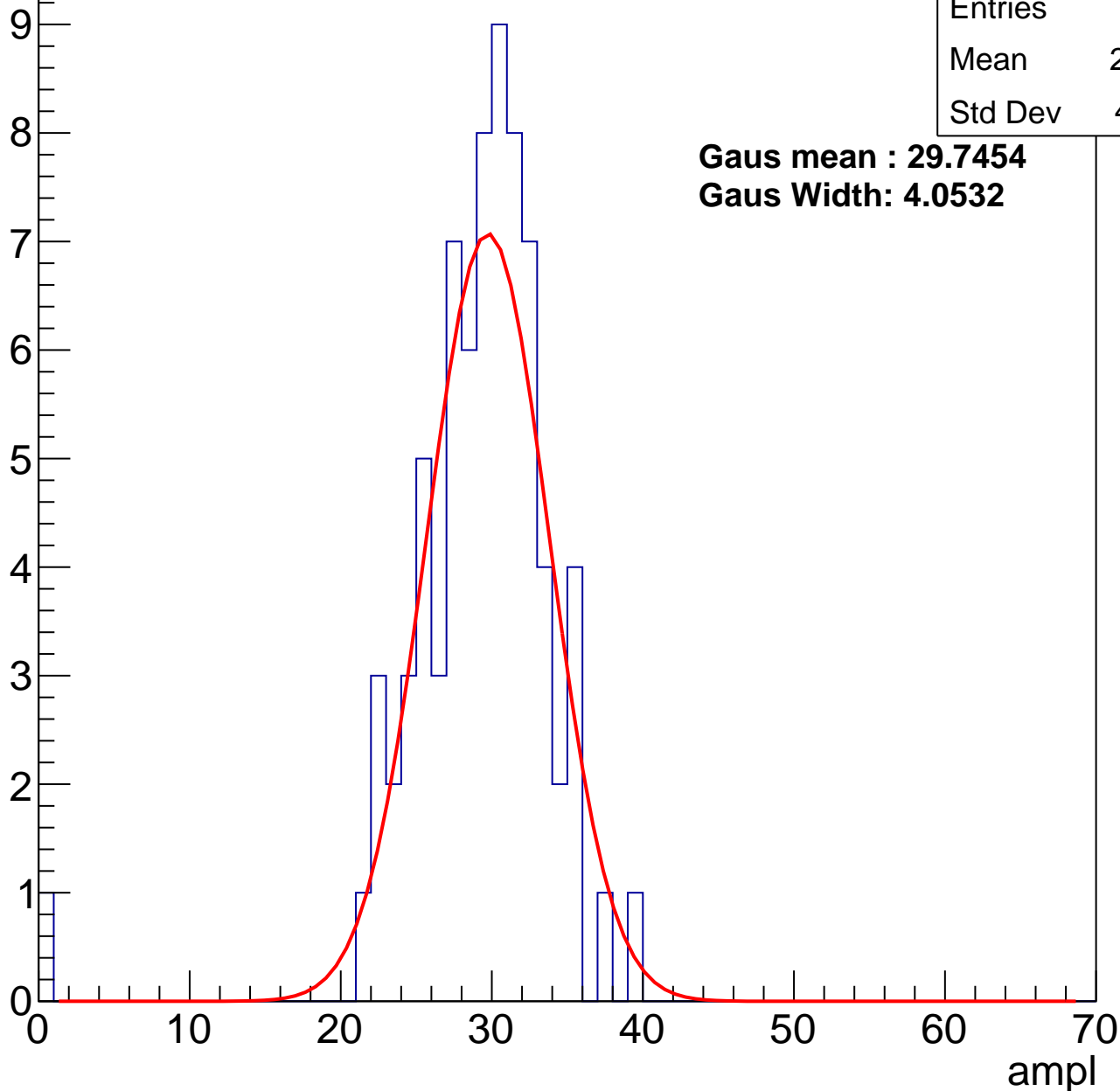
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	75
Mean	28.73
Std Dev	4.981

**Gaus mean : 29.7454**

**Gaus Width: 4.0532**



# B1L003S, U3-ch101, adc1

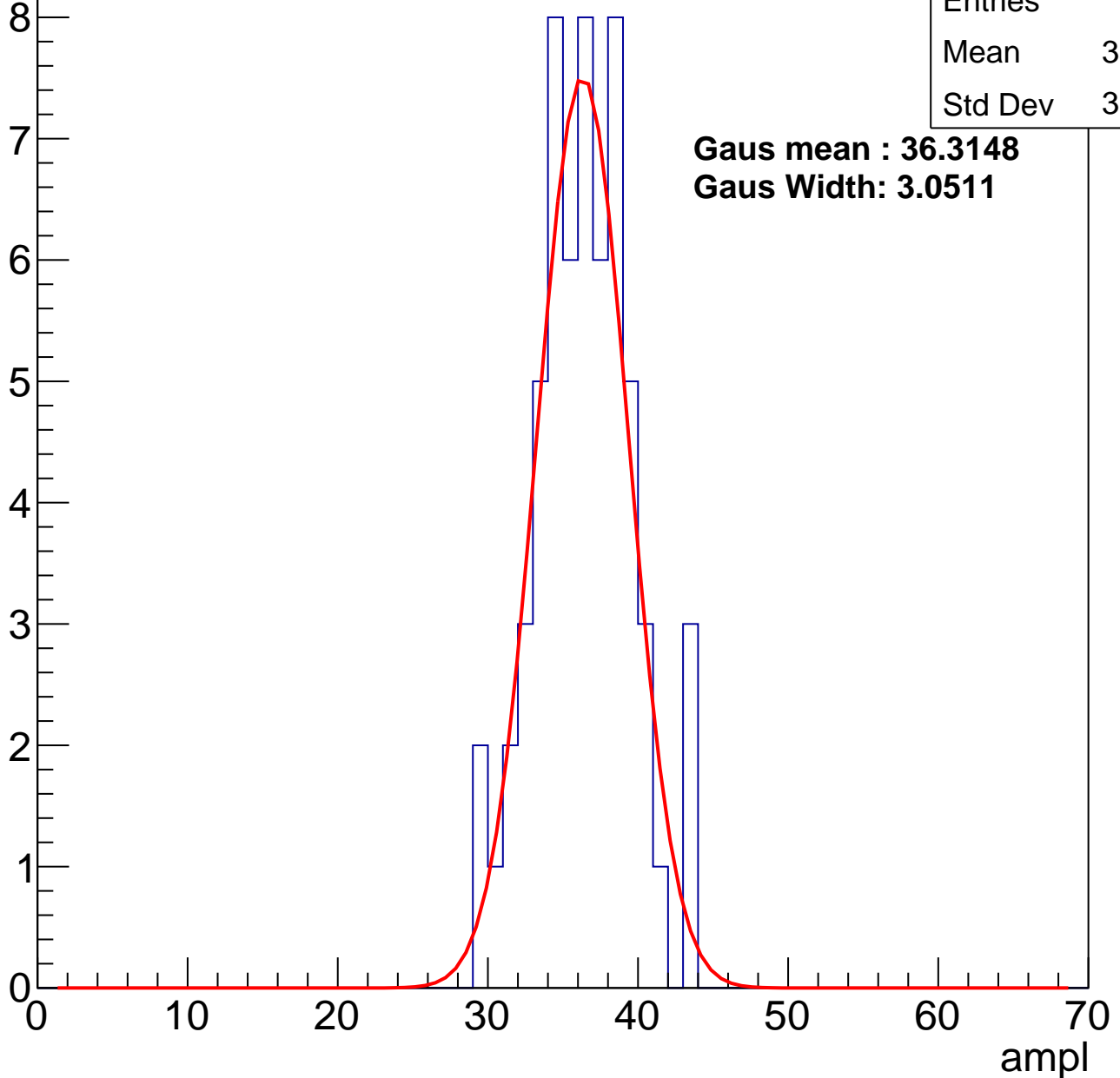
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	35.93
Std Dev	3.182

**Gaus mean : 36.3148**

**Gaus Width: 3.0511**



# B1L003S, U3-ch101, adc2

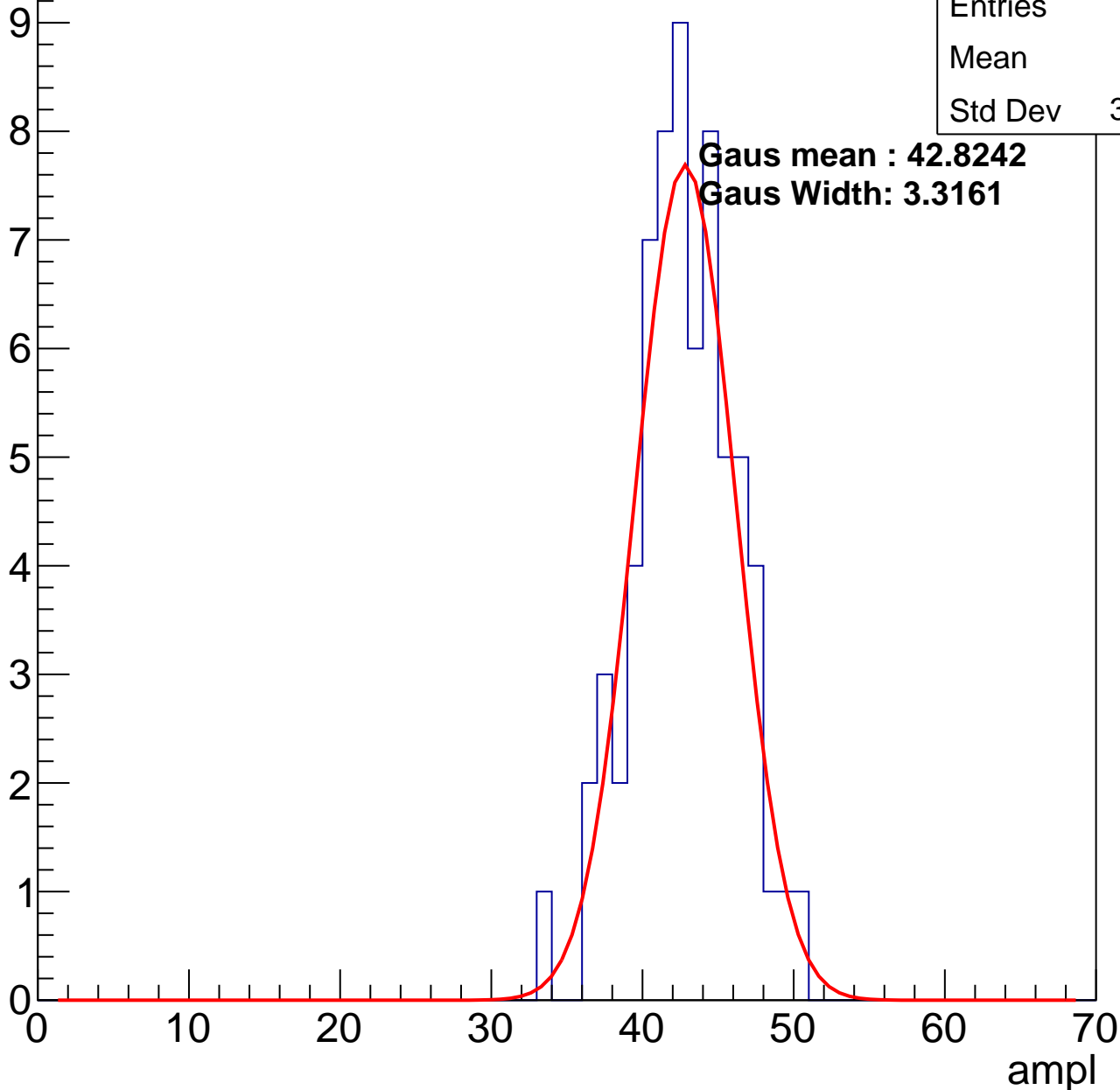
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	42.3
Std Dev	3.319

**Gaus mean : 42.8242**

**Gaus Width: 3.3161**

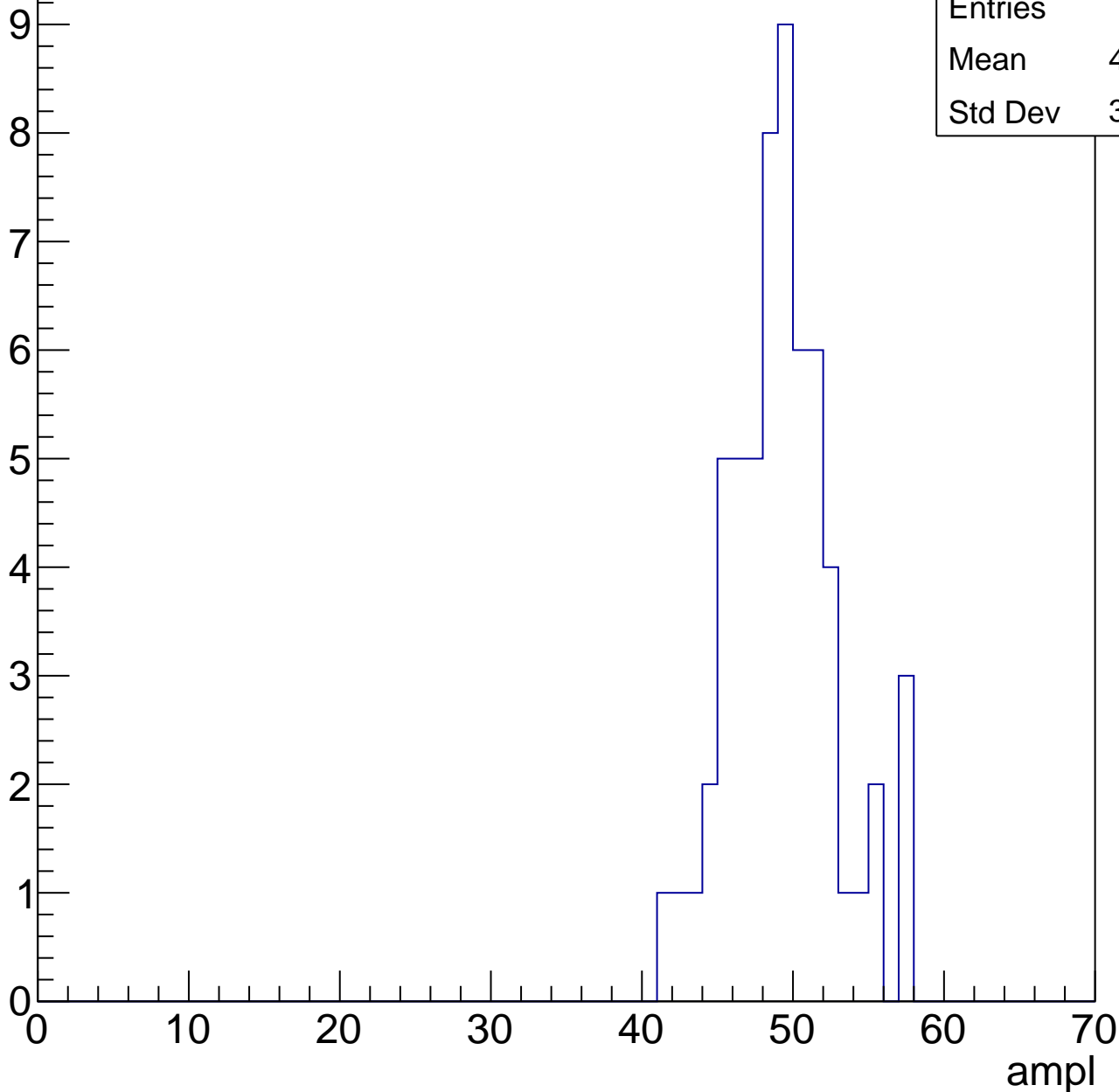


# B1L003S, U3-ch101, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	48.85
Std Dev	3.468

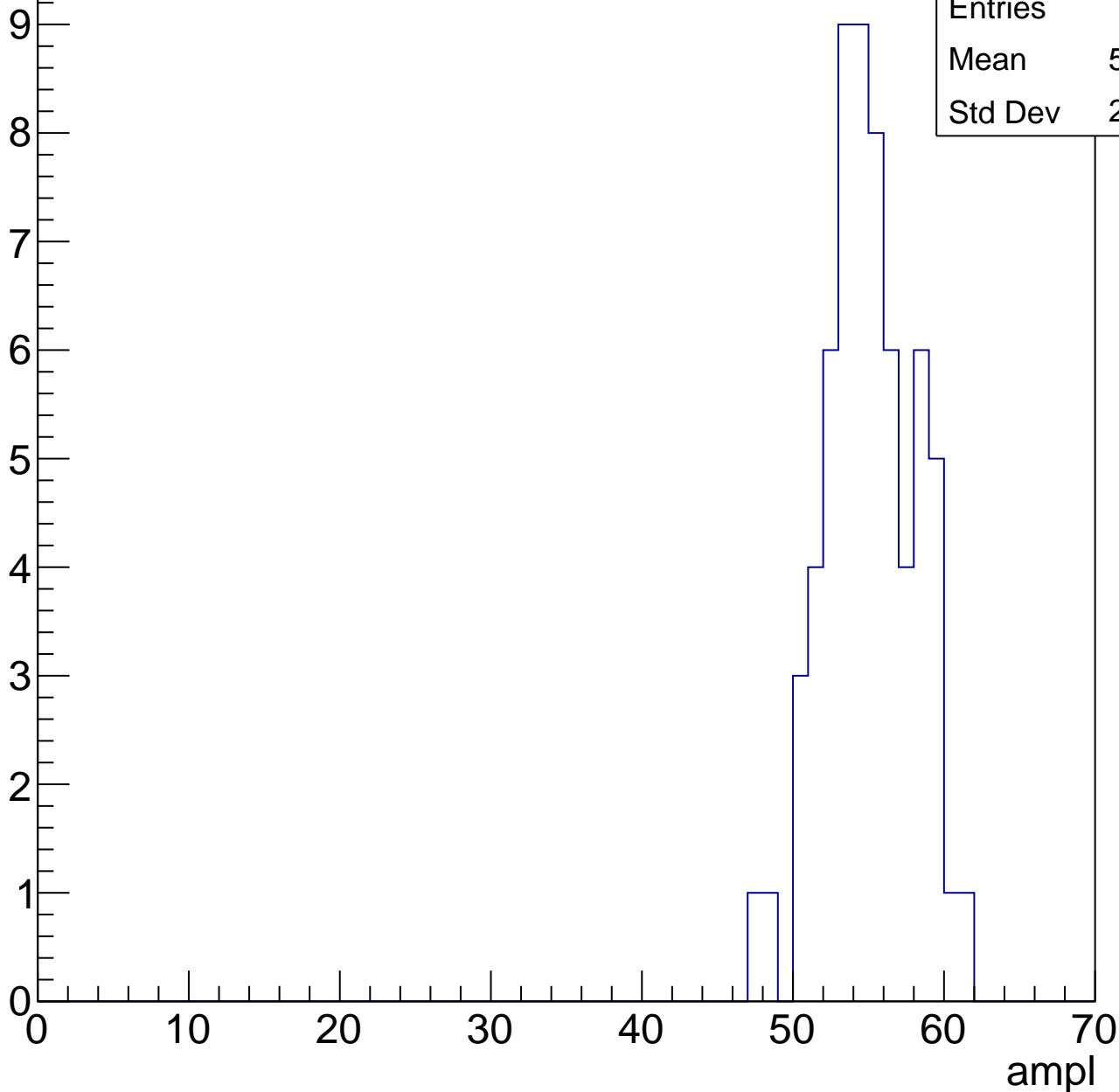


# B1L003S, U3-ch101, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	54.56
Std Dev	2.947

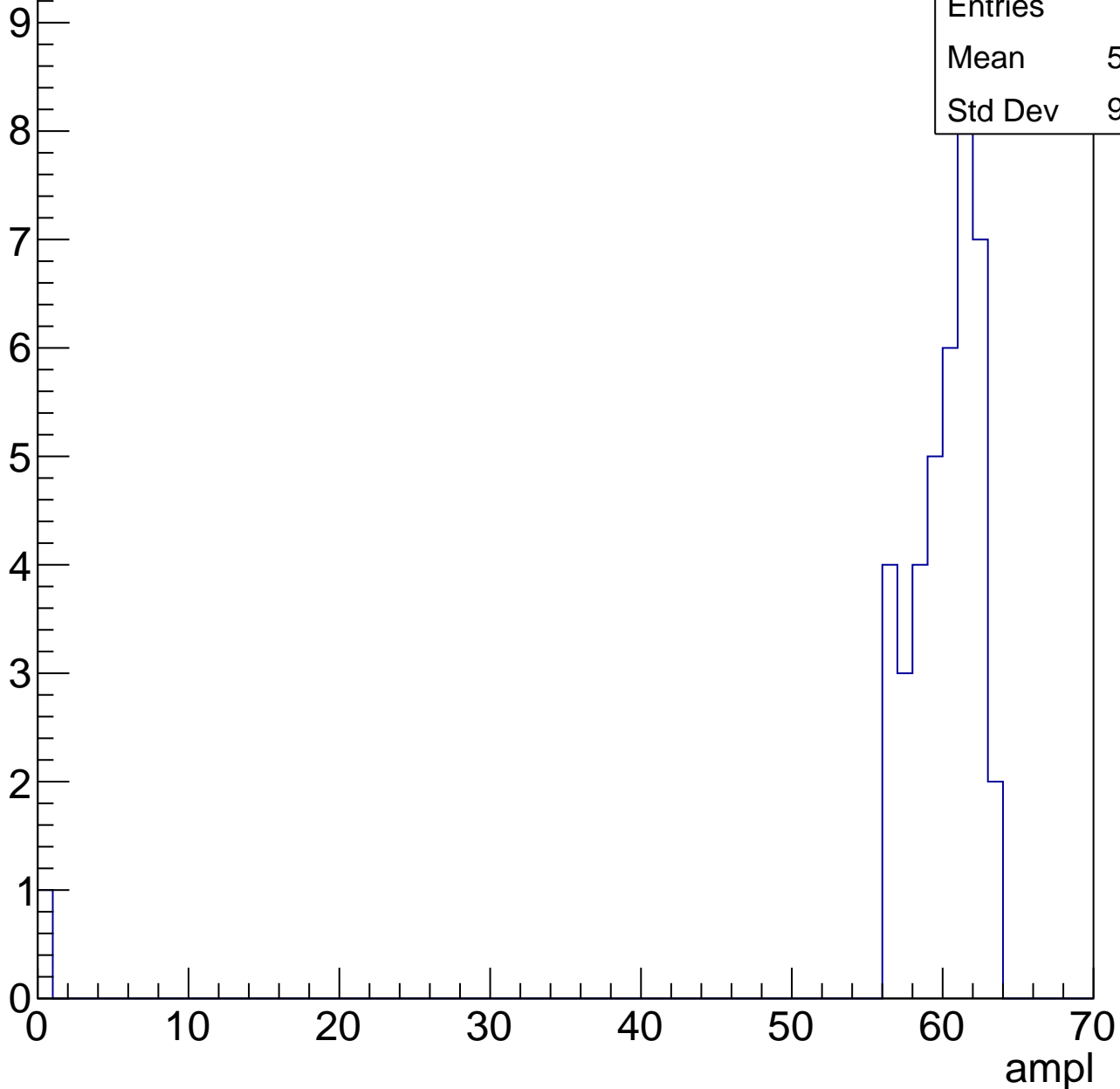


# B1L003S, U3-ch101, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	41
Mean	58.32
Std Dev	9.436

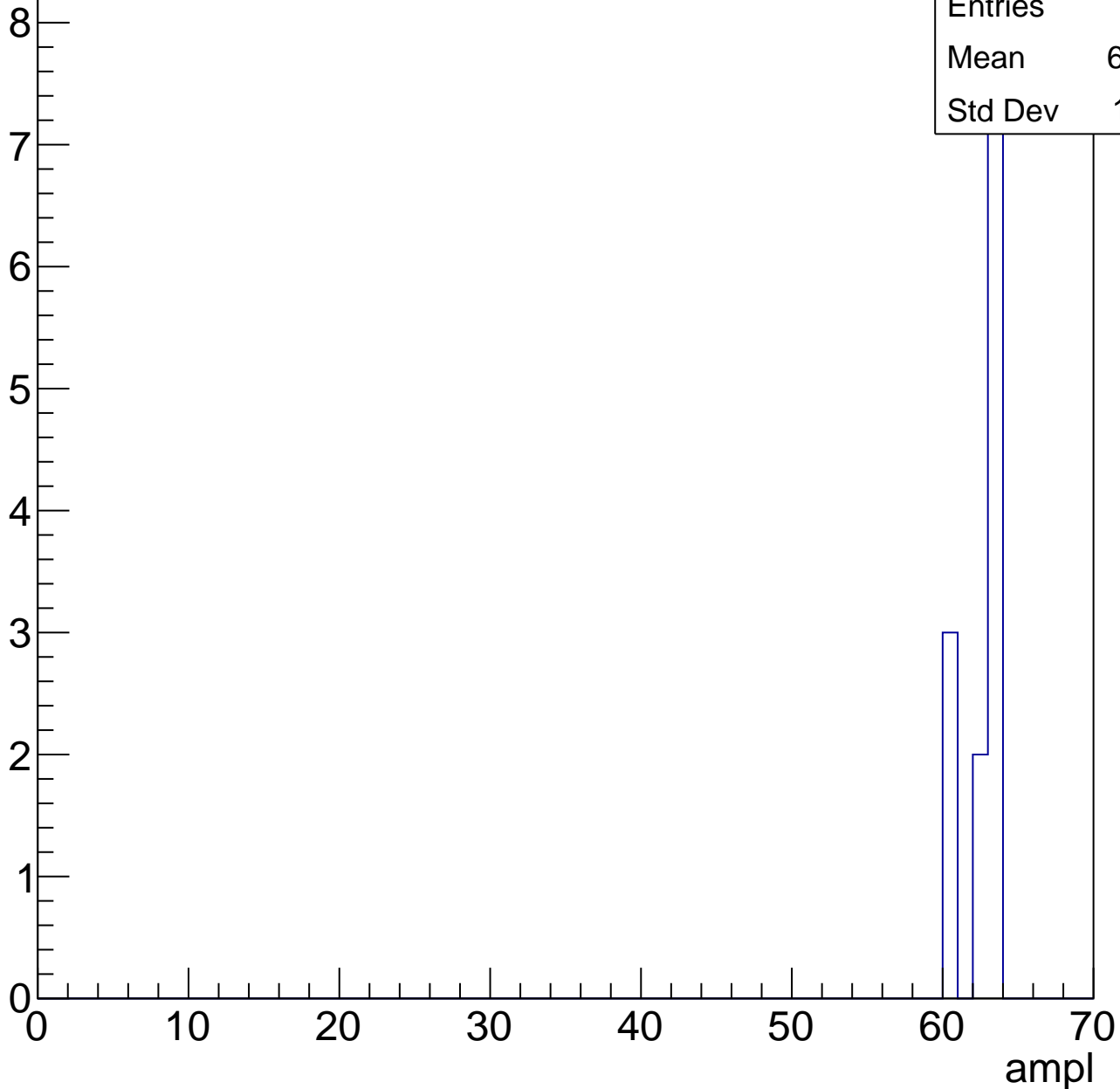


# B1L003S, U3-ch101, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	13
Mean	62.15
Std Dev	1.231





# B1L003S, U3-ch101, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U3-ch102, adc0

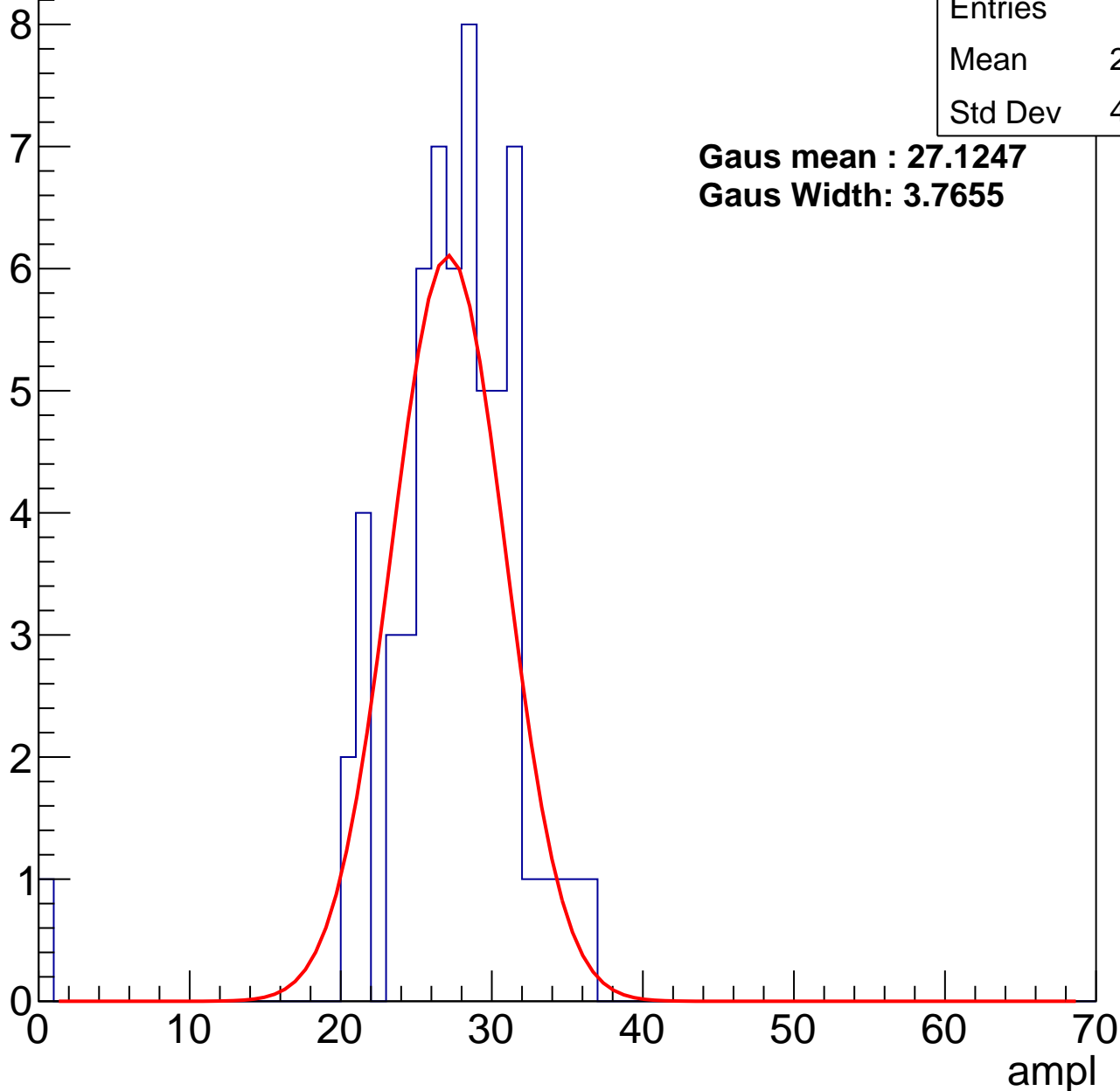
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	26.85
Std Dev	4.944

**Gaus mean : 27.1247**

**Gaus Width: 3.7655**



# B1L003S, U3-ch102, adc1

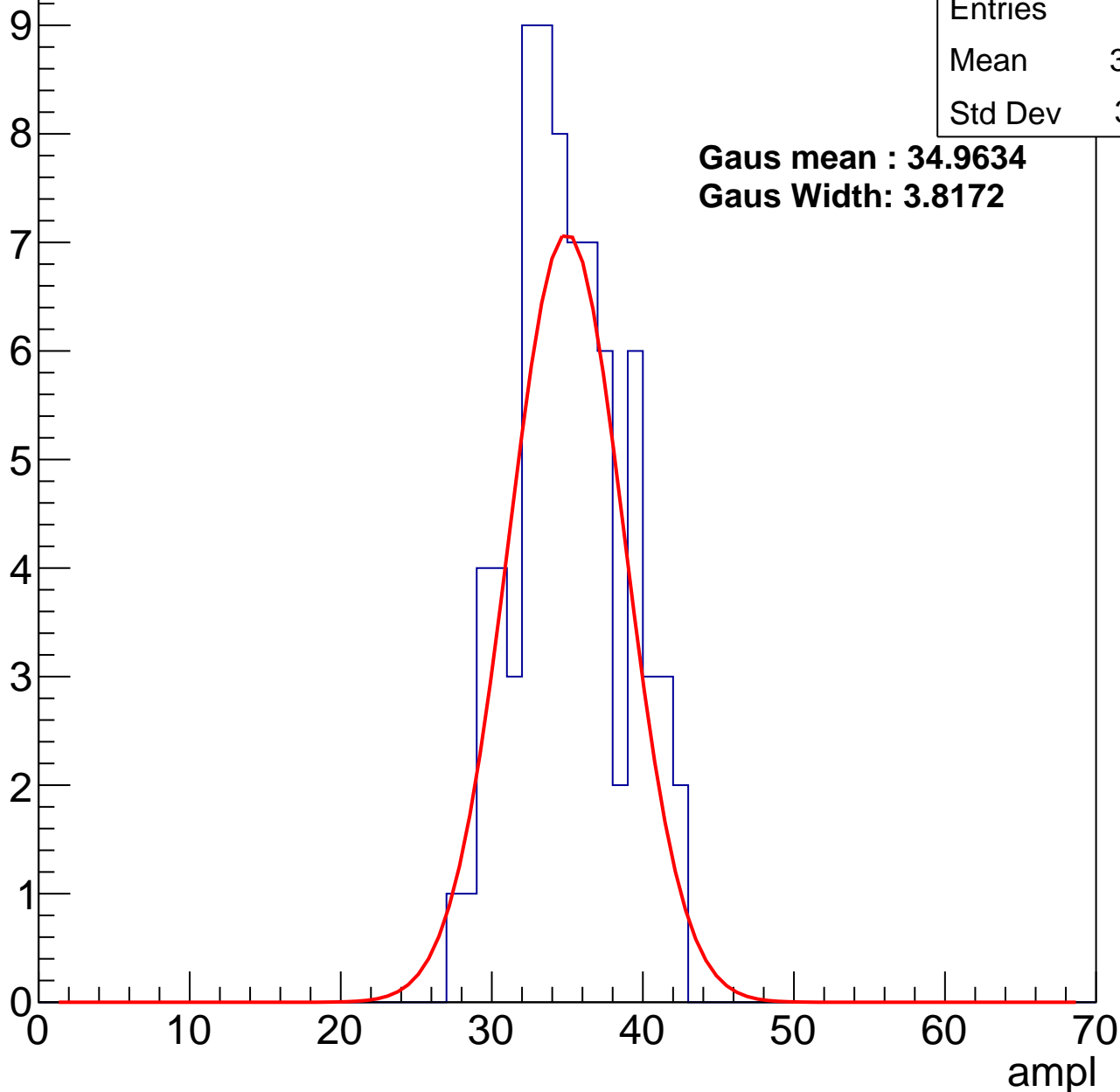
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	75
Mean	34.63
Std Dev	3.551

**Gaus mean : 34.9634**

**Gaus Width: 3.8172**



# B1L003S, U3-ch102, adc2

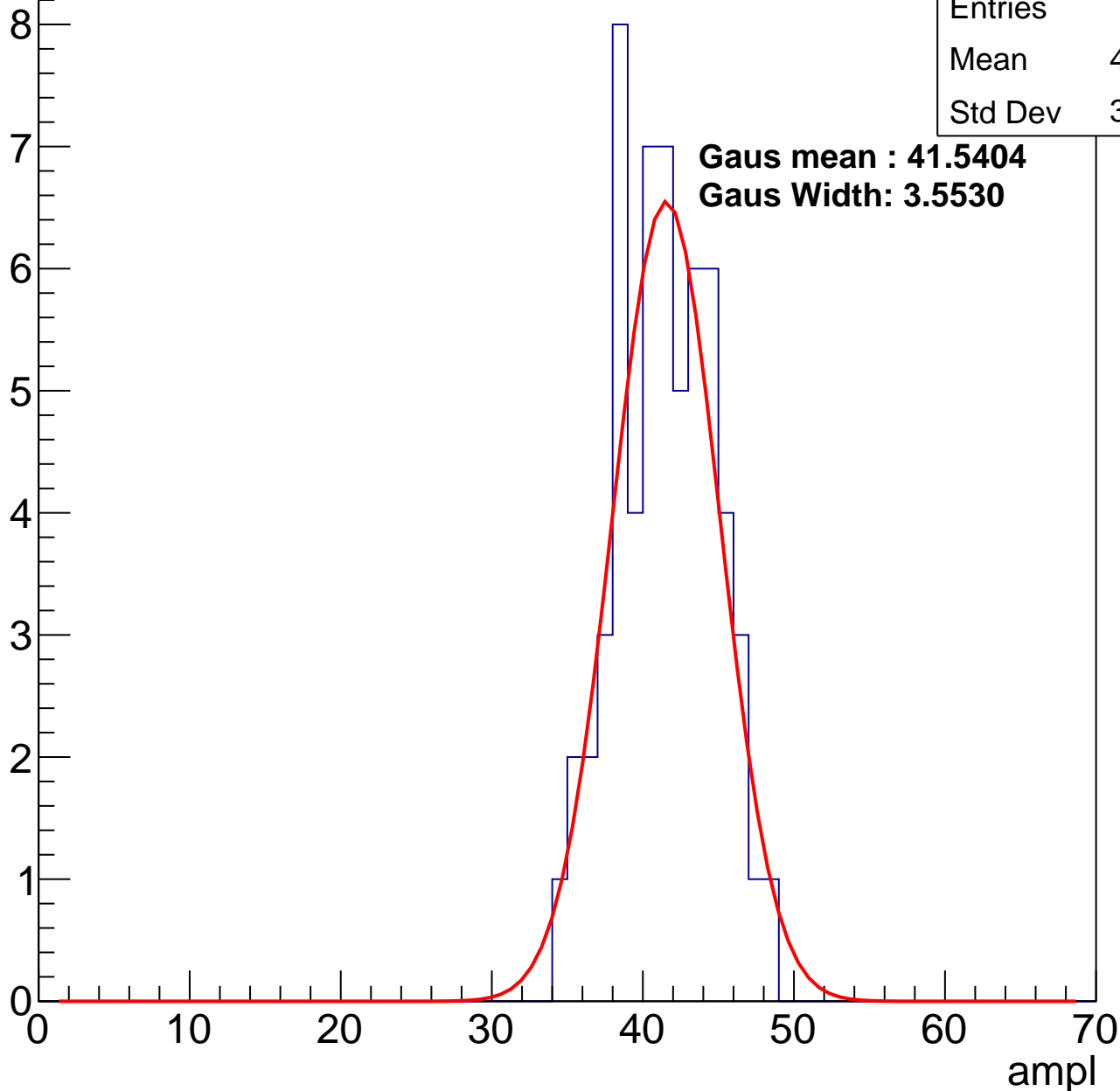
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	40.98
Std Dev	3.217

**Gaus mean : 41.5404**

**Gaus Width: 3.5530**

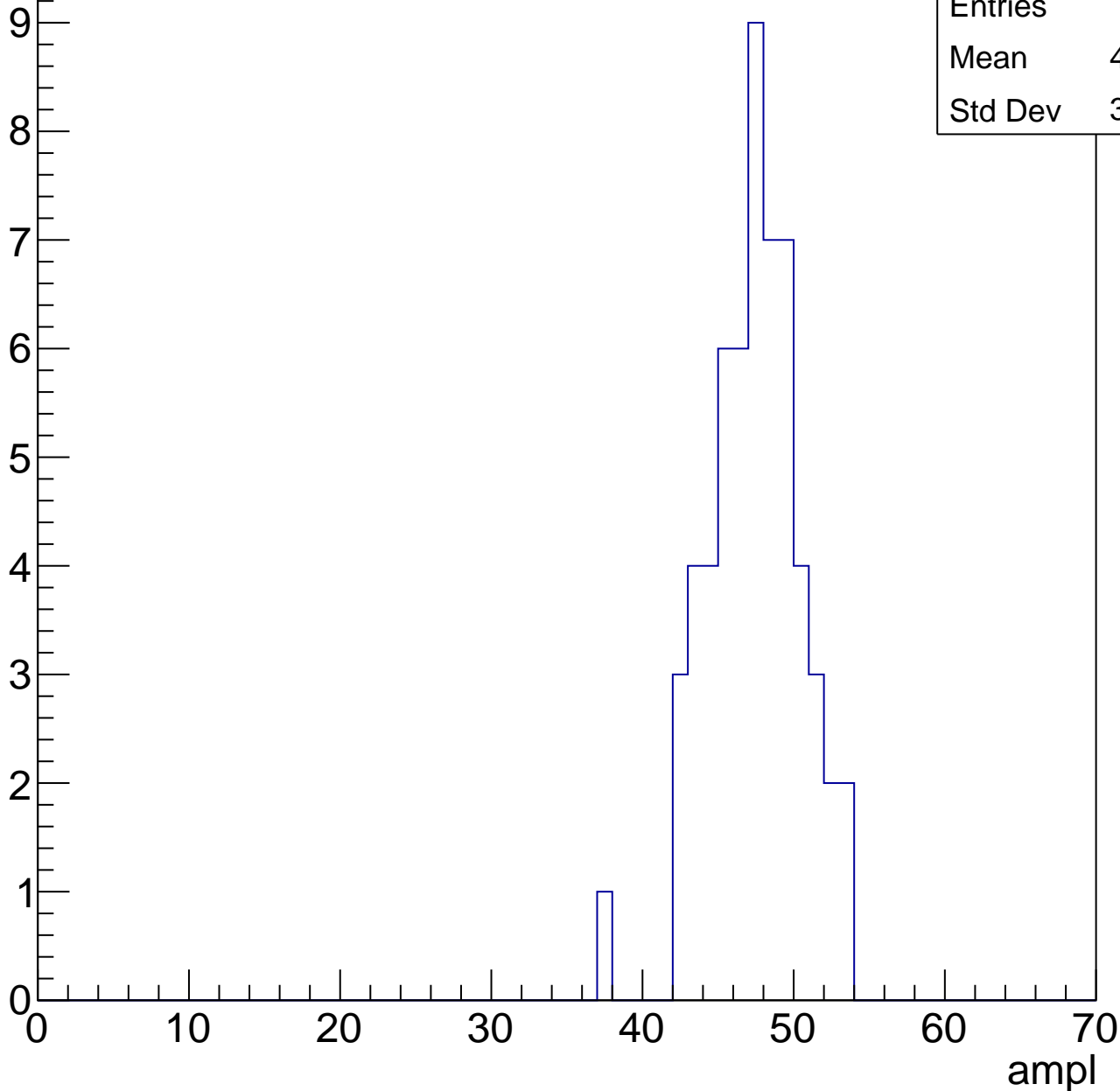


# B1L003S, U3-ch102, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

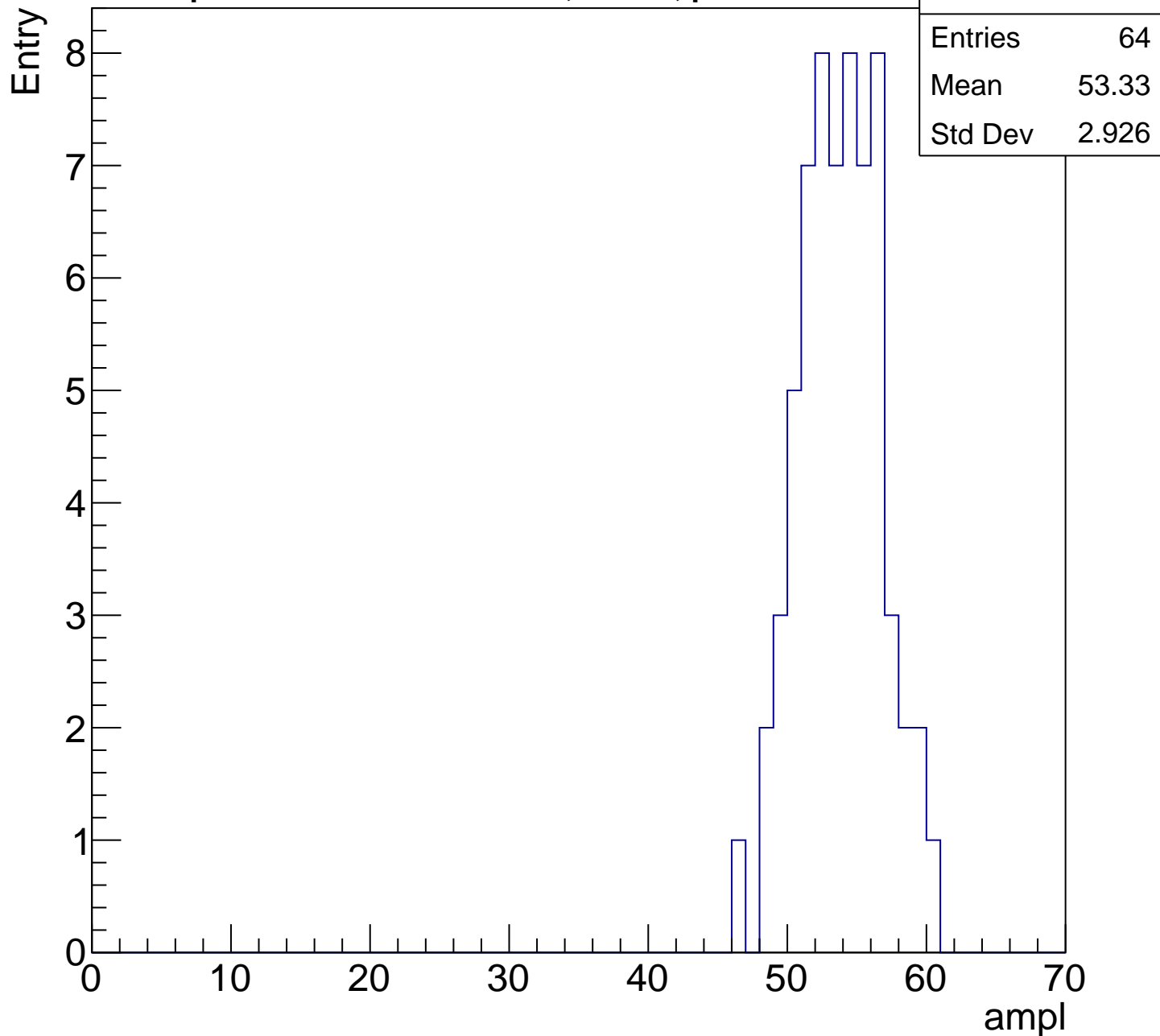
Entry

Entries	58
Mean	46.93
Std Dev	3.067



# B1L003S, U3-ch102, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

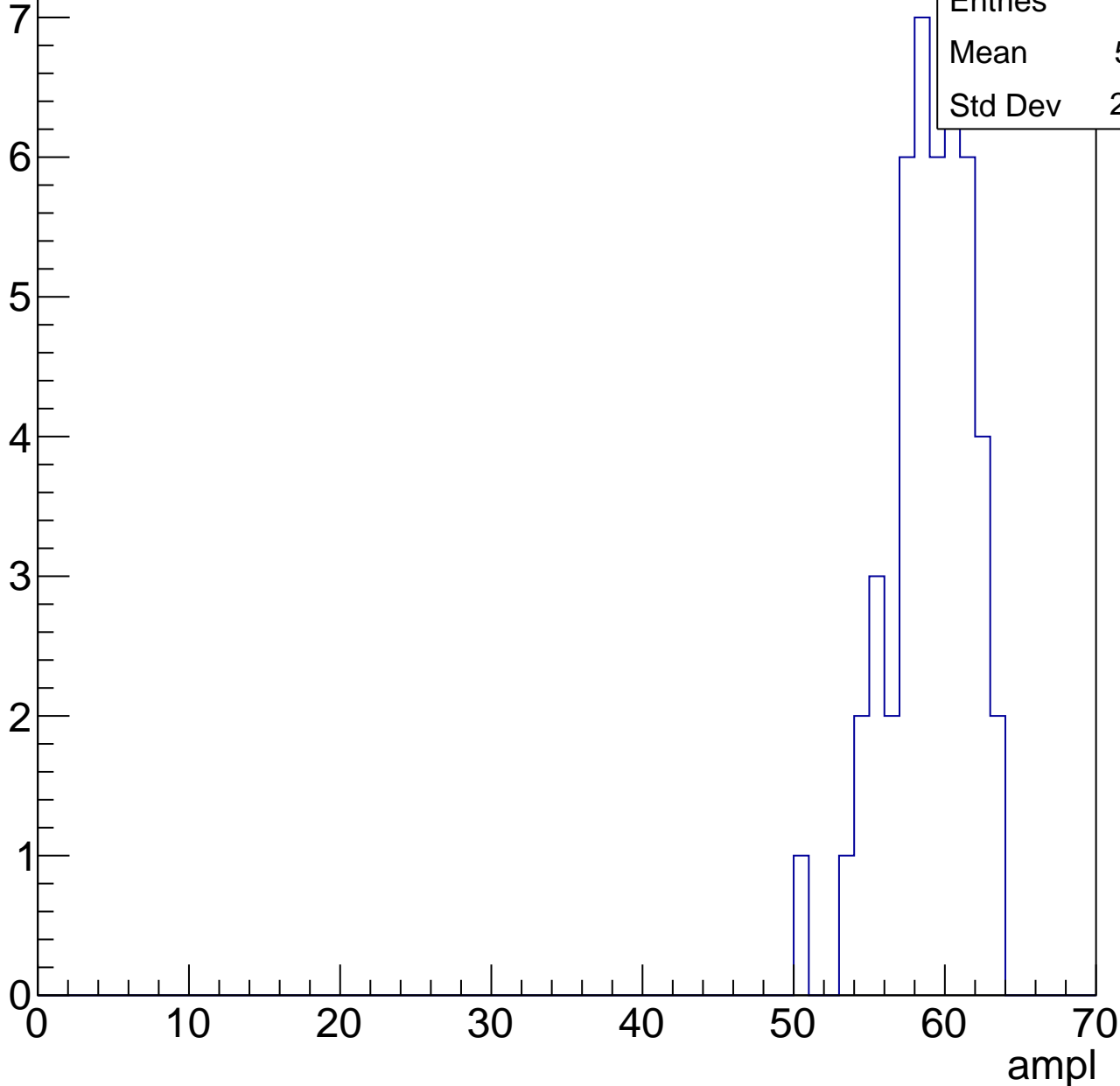


# B1L003S, U3-ch102, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	47
Mean	58.51
Std Dev	2.736

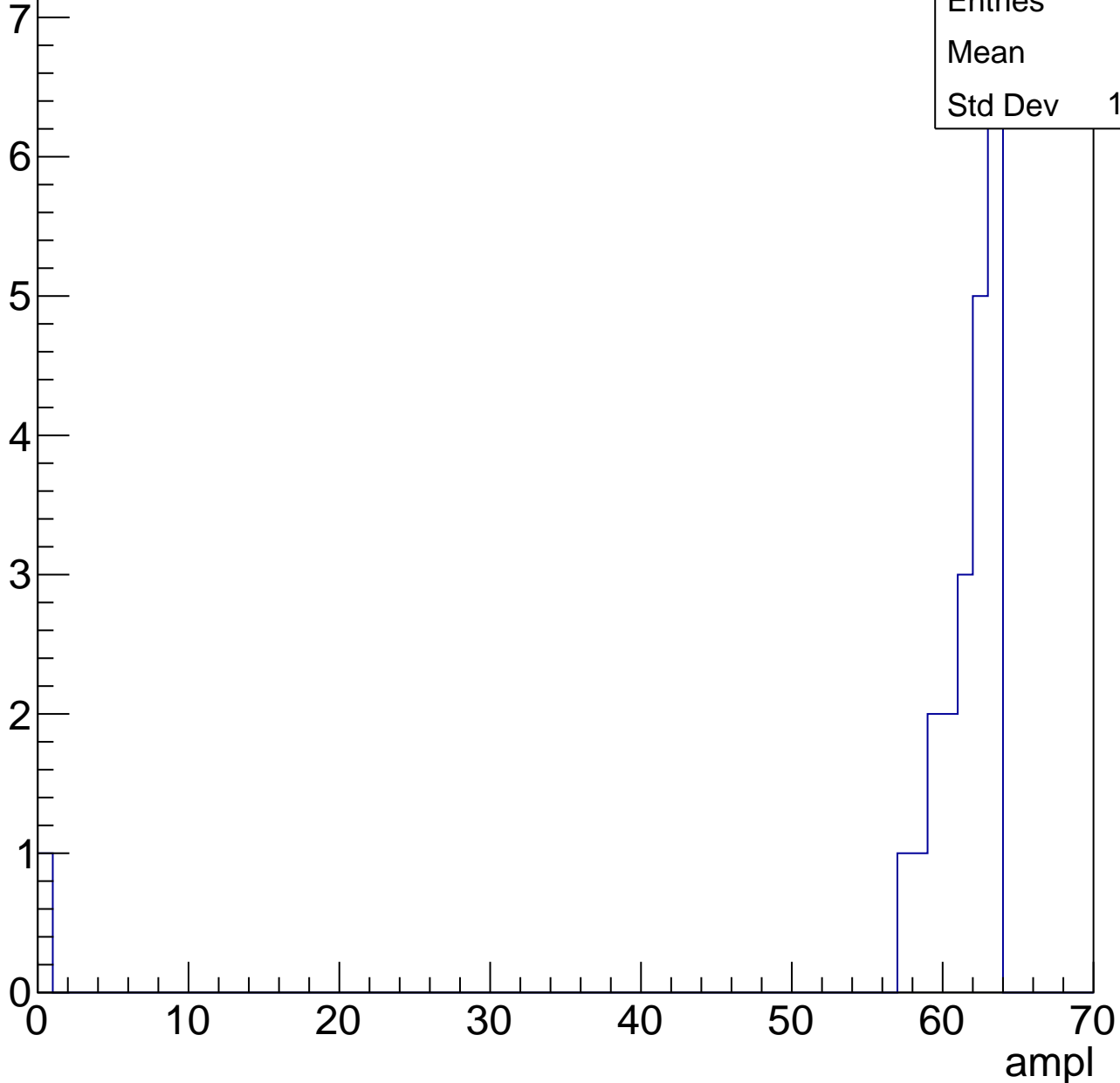


# B1L003S, U3-ch102, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	22
Mean	58.5
Std Dev	12.88

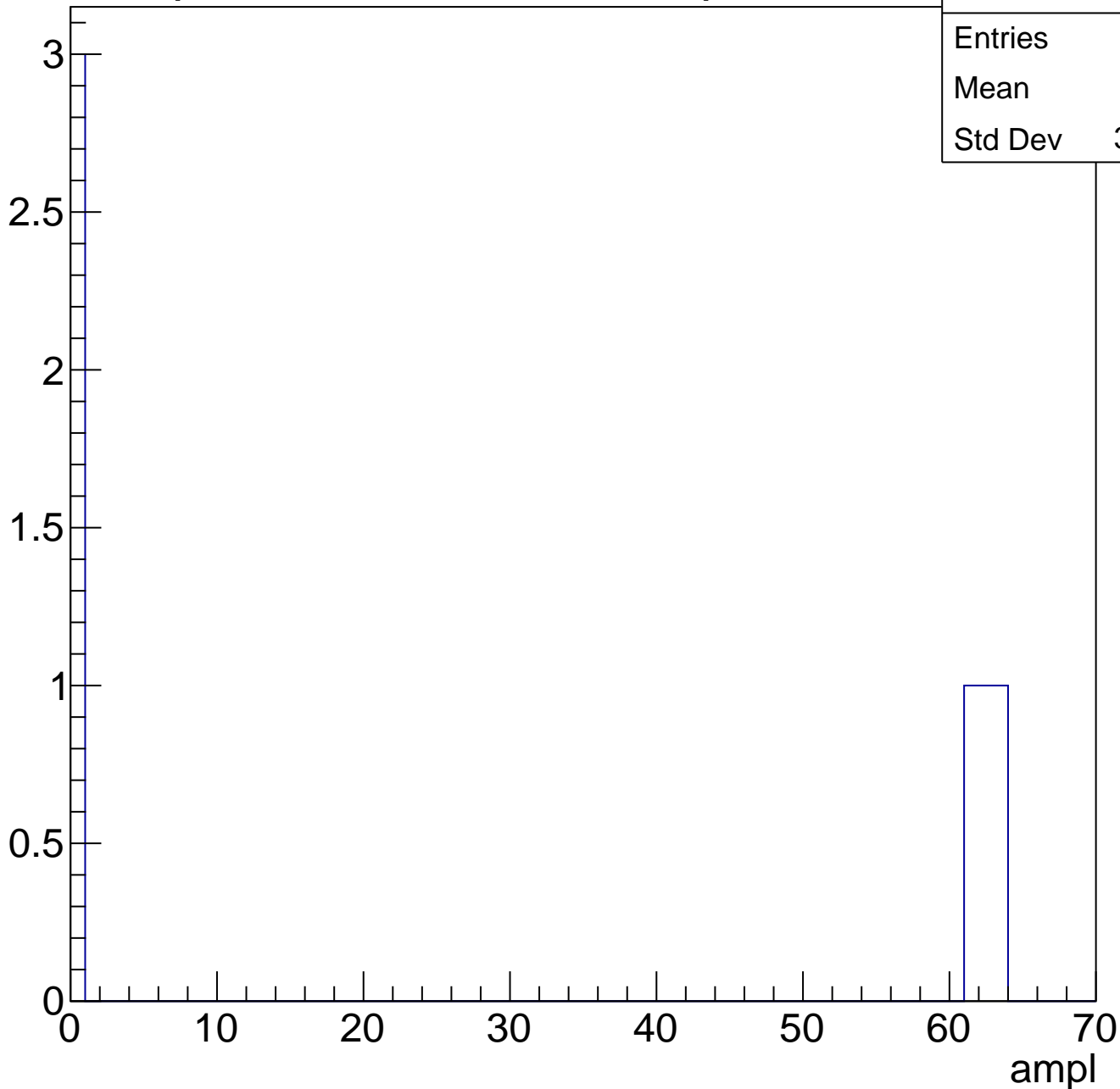




# B1L003S, U3-ch102, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U3-ch103, adc0

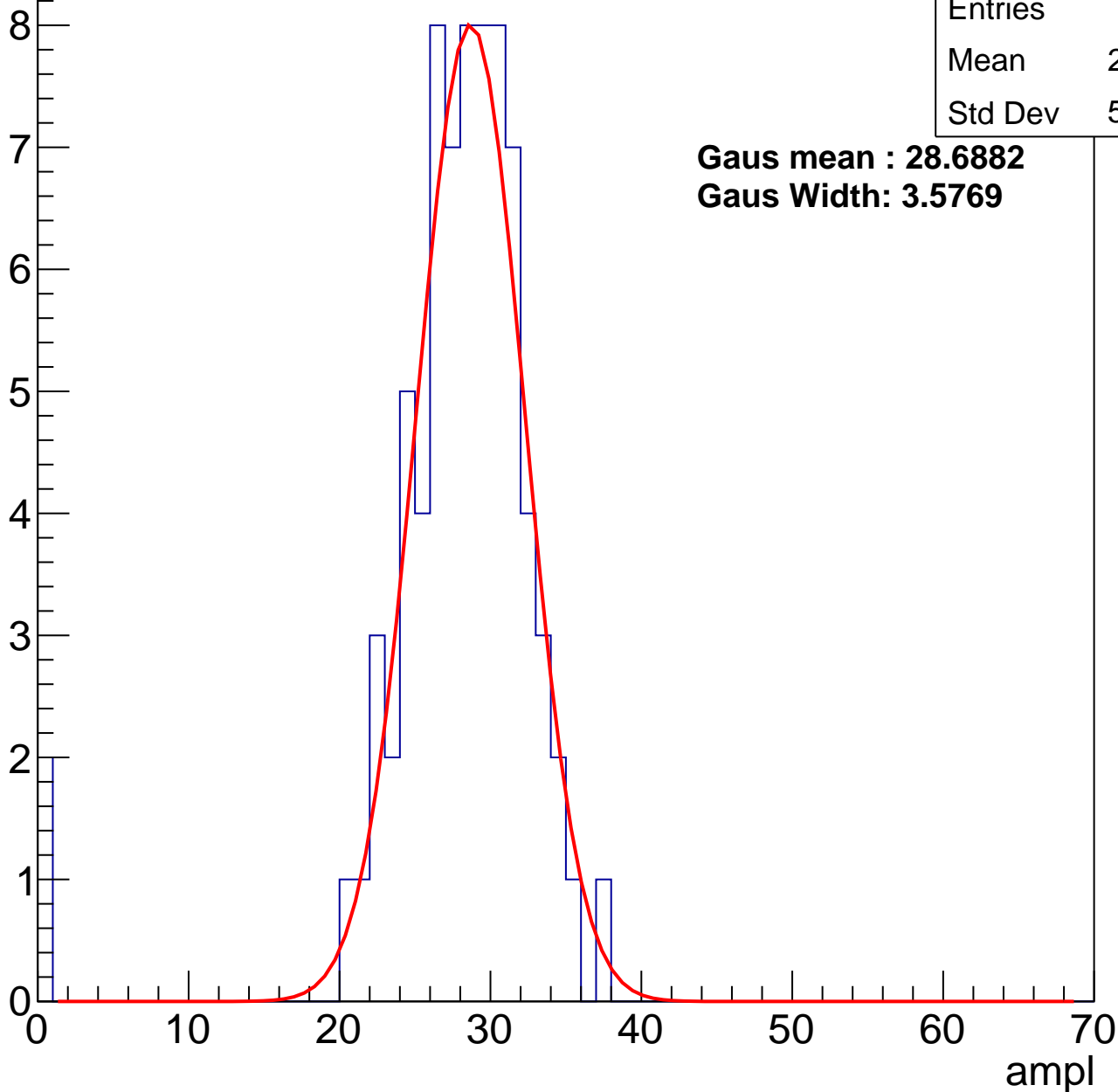
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	75
Mean	27.33
Std Dev	5.662

**Gaus mean : 28.6882**

**Gaus Width: 3.5769**



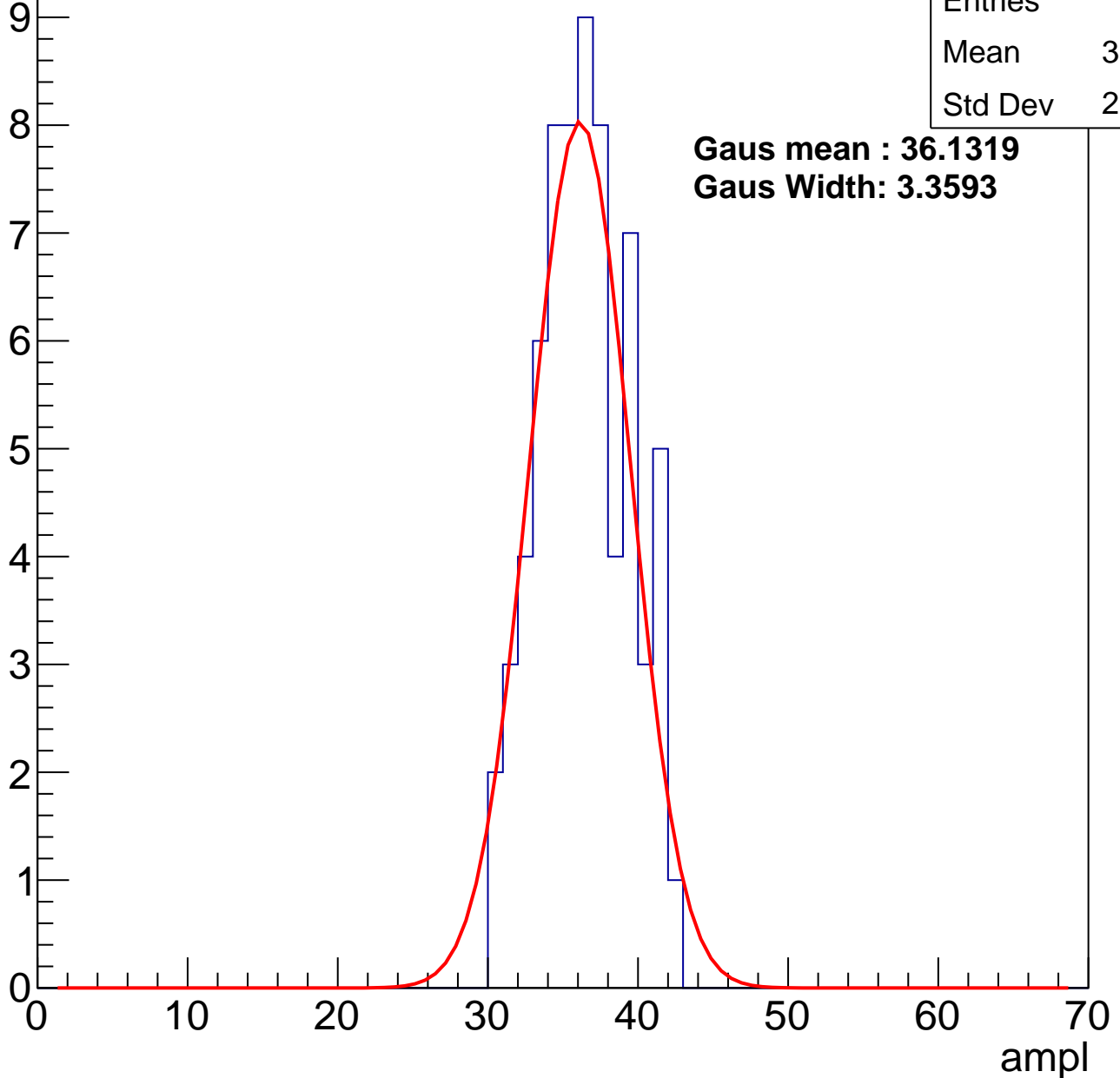
# B1L003S, U3-ch103, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	35.93
Std Dev	2.972

**Gaus mean : 36.1319**  
**Gaus Width: 3.3593**



# B1L003S, U3-ch103, adc2

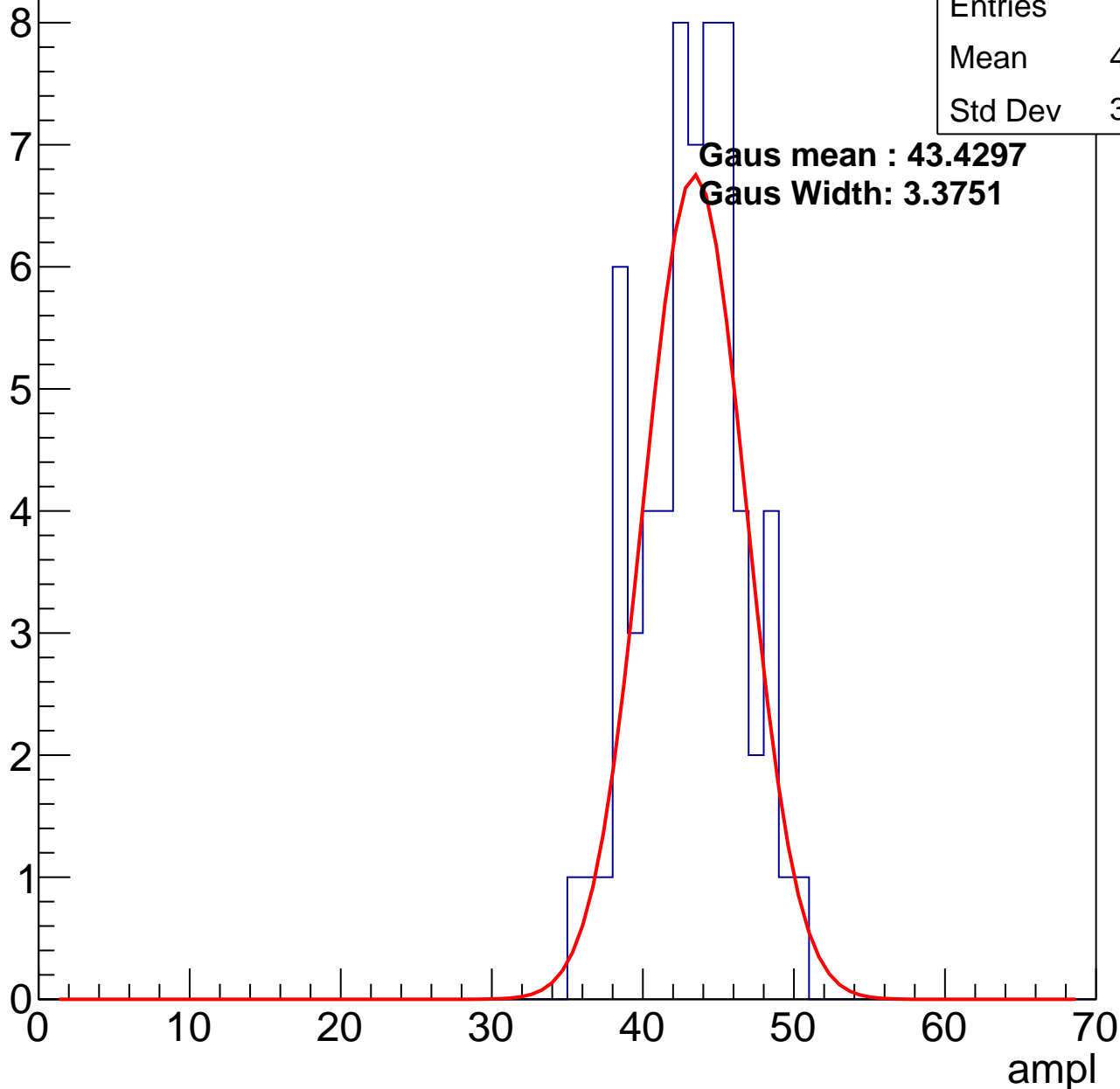
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	42.78
Std Dev	3.326

**Gaus mean : 43.4297**

**Gaus Width: 3.3751**

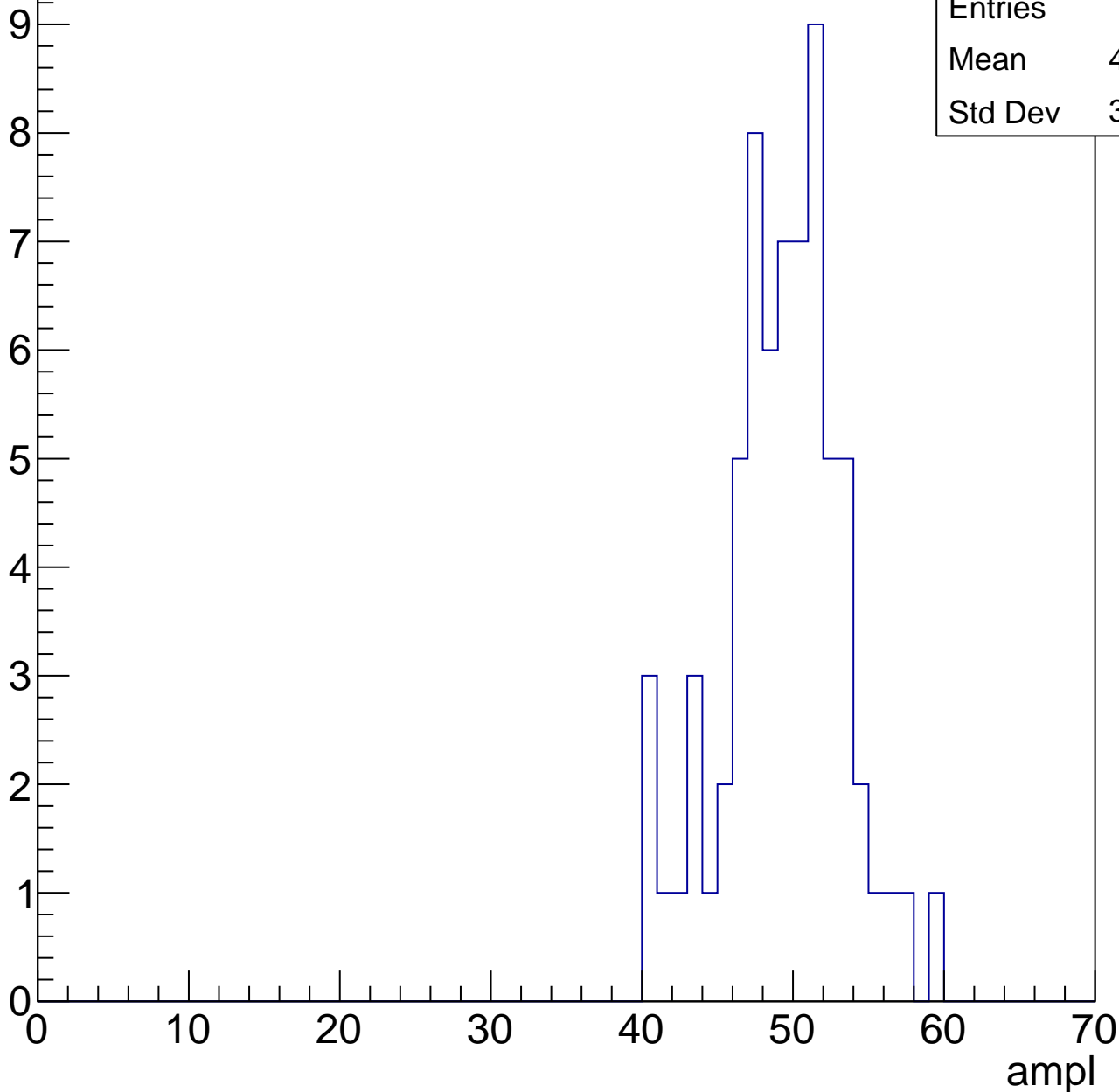


# B1L003S, U3-ch103, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	48.87
Std Dev	3.938

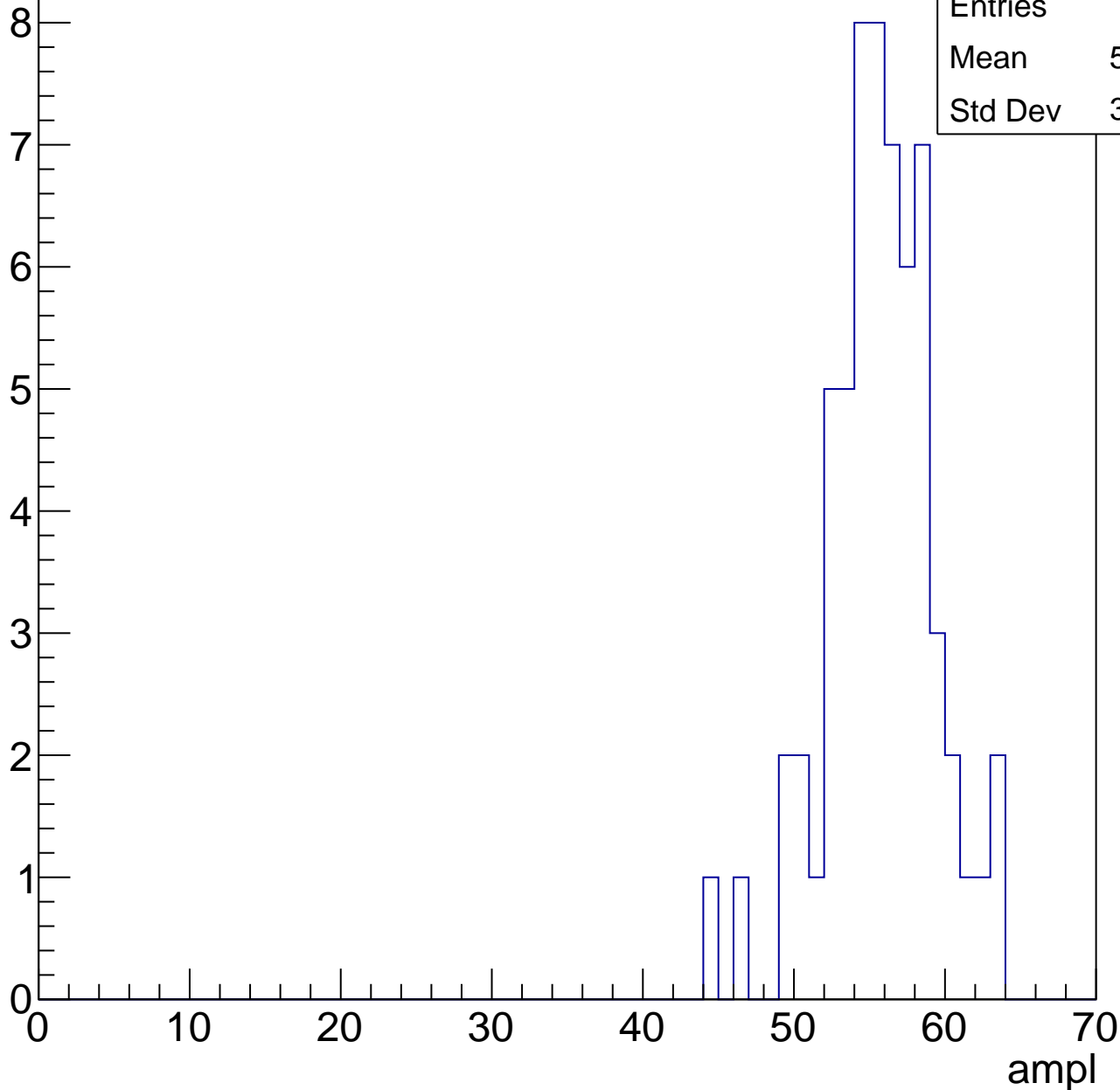


# B1L003S, U3-ch103, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	55.19
Std Dev	3.627

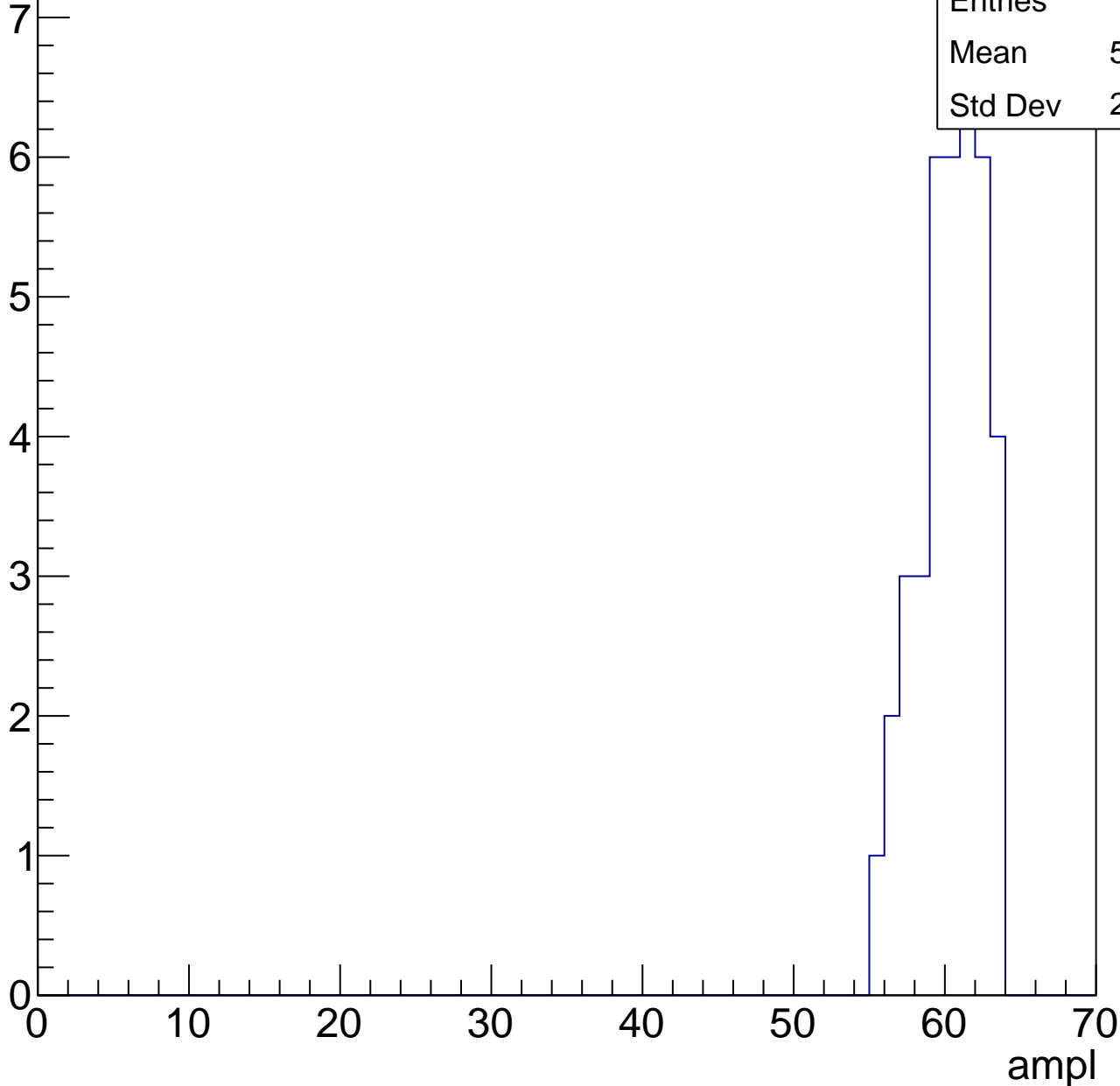


# B1L003S, U3-ch103, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

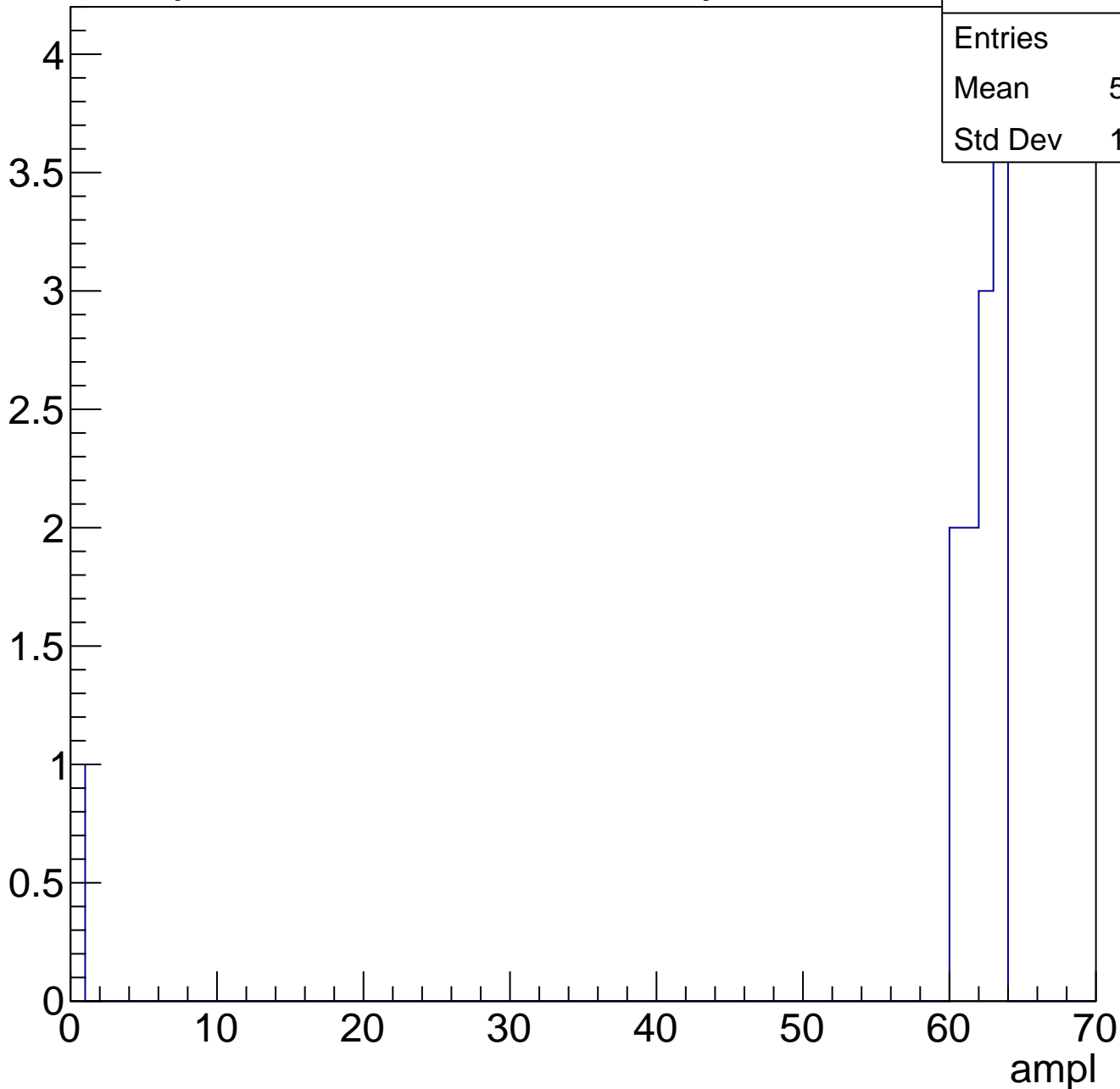
Entries	38
Mean	59.92
Std Dev	2.107



# B1L003S, U3-ch103, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch103, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L003S, U3-ch104, adc0

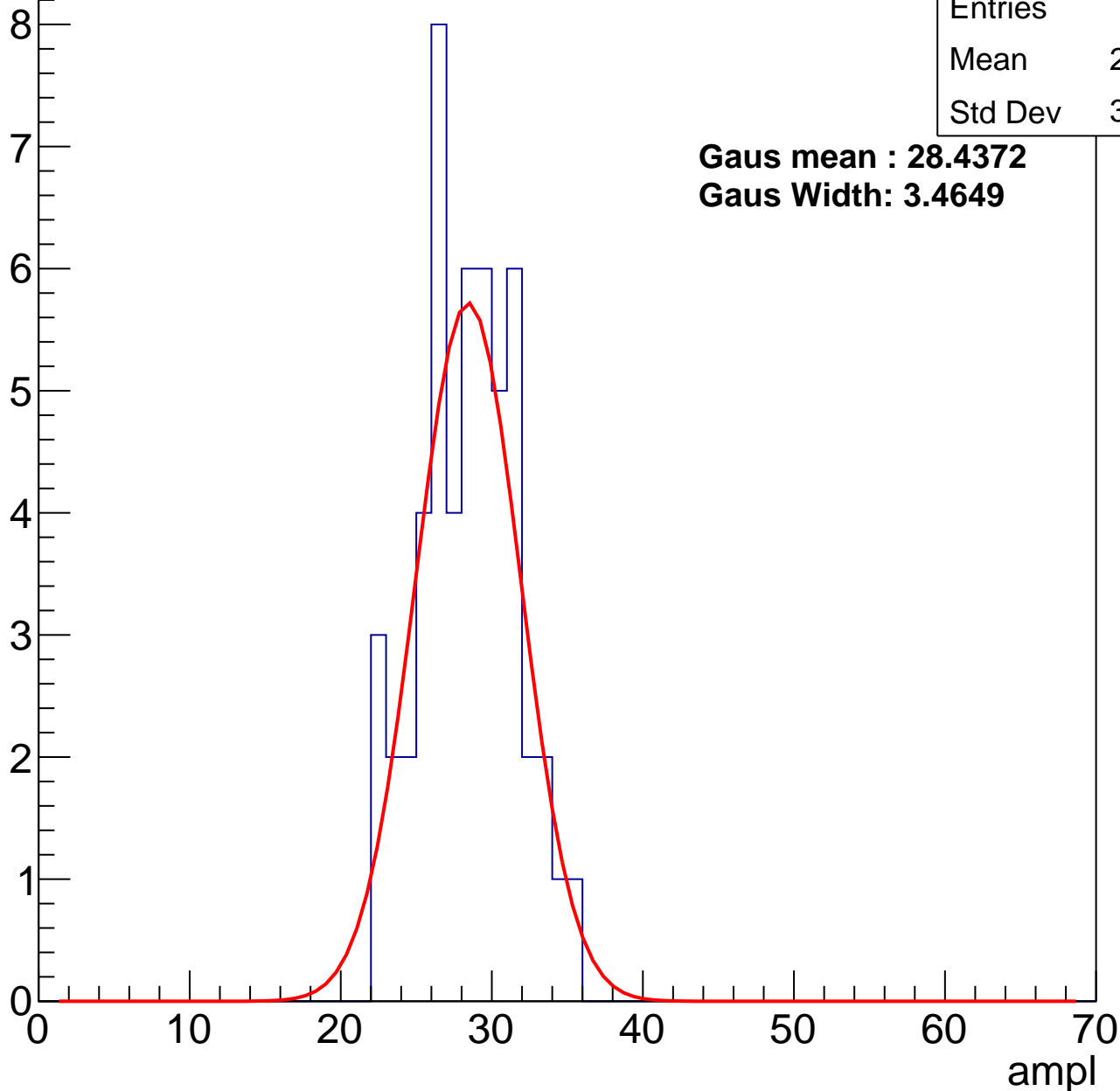
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	52
Mean	27.94
Std Dev	3.128

**Gaus mean : 28.4372**

**Gaus Width: 3.4649**



# B1L003S, U3-ch104, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	86
Mean	35.31
Std Dev	3.383

**Gaus mean : 36.2108**

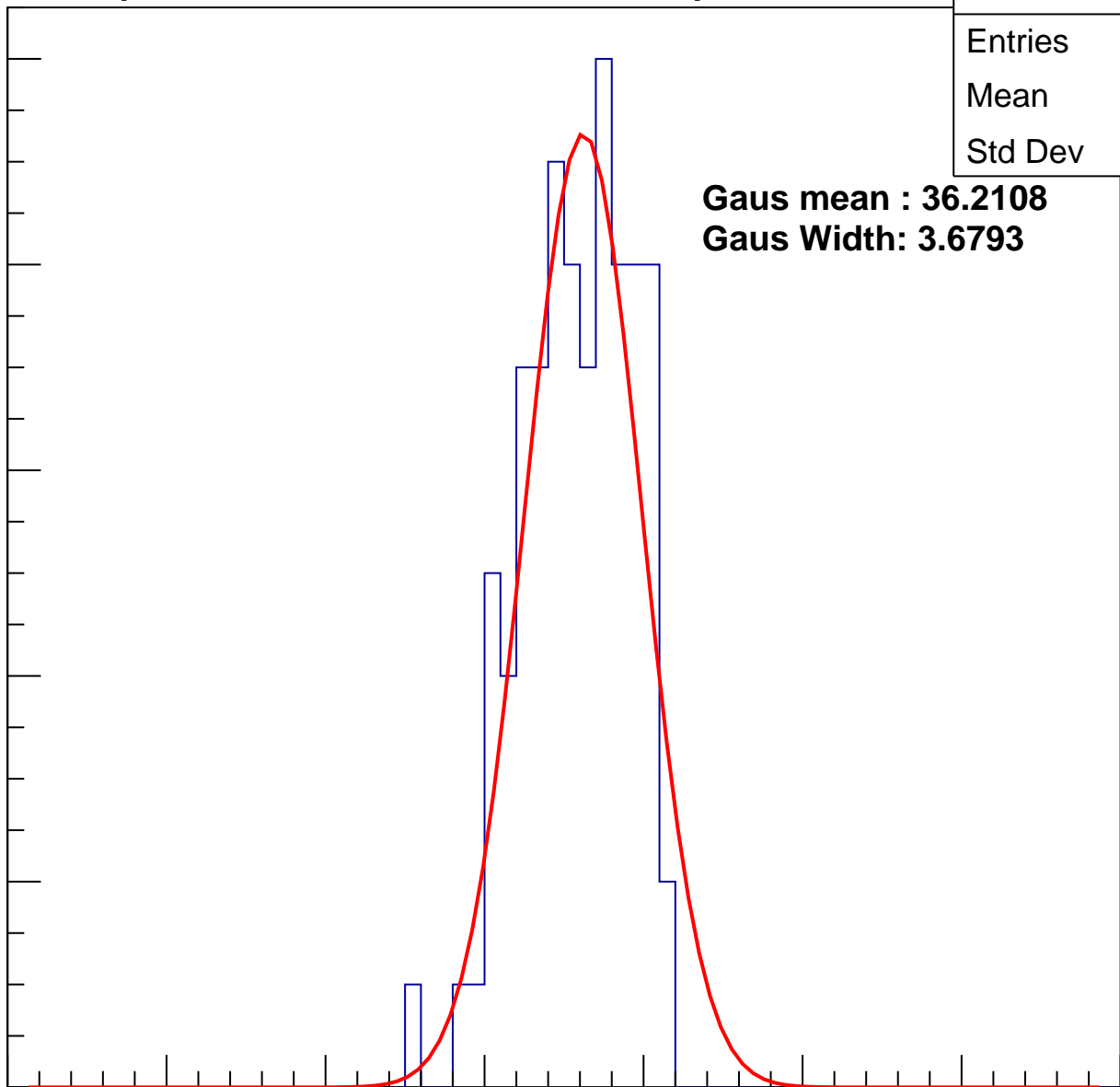
**Gaus Width: 3.6793**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U3-ch104, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	51
Mean	42.08
Std Dev	3.33

**Gaus mean : 43.1520**

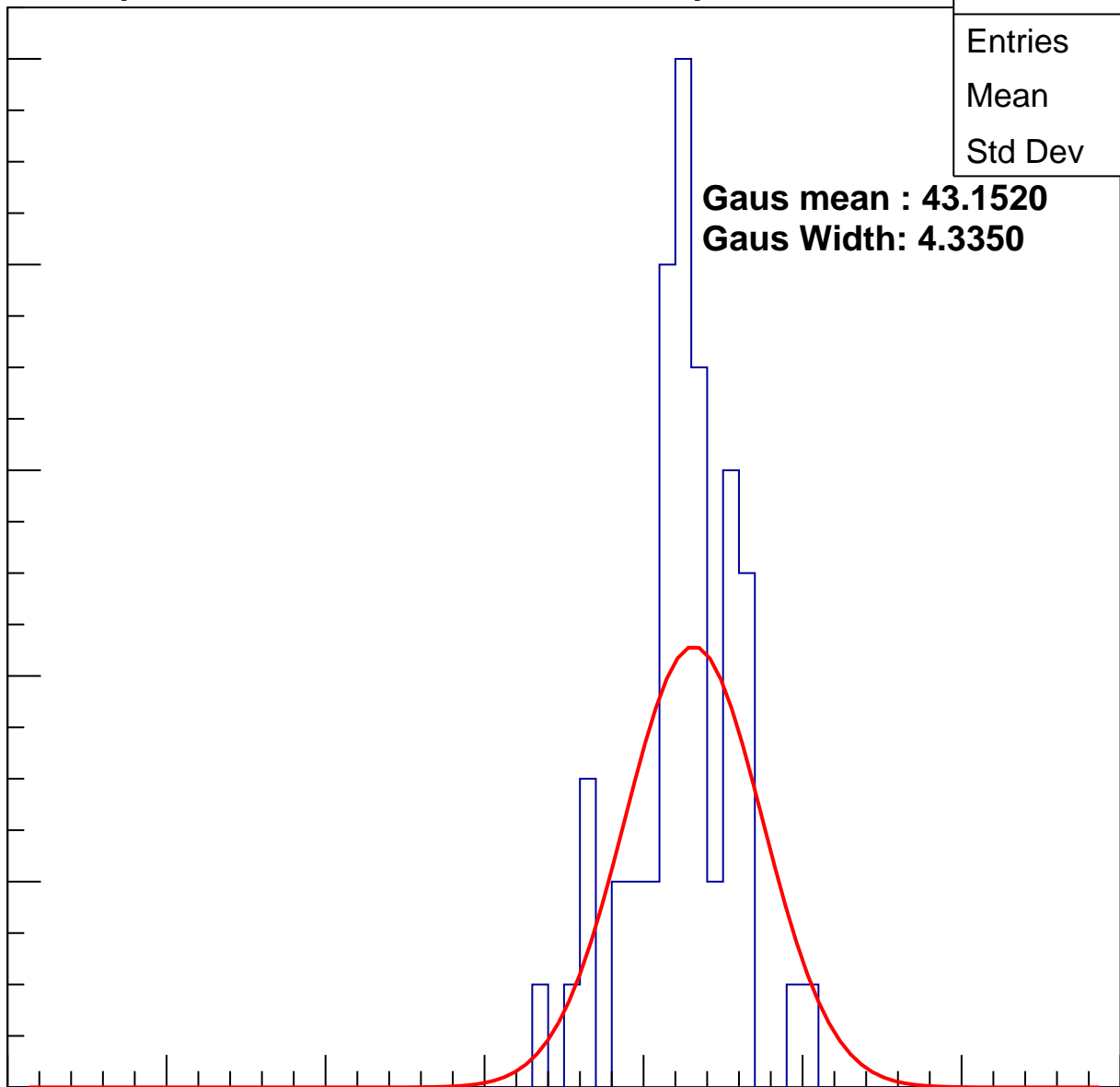
**Gaus Width: 4.3350**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

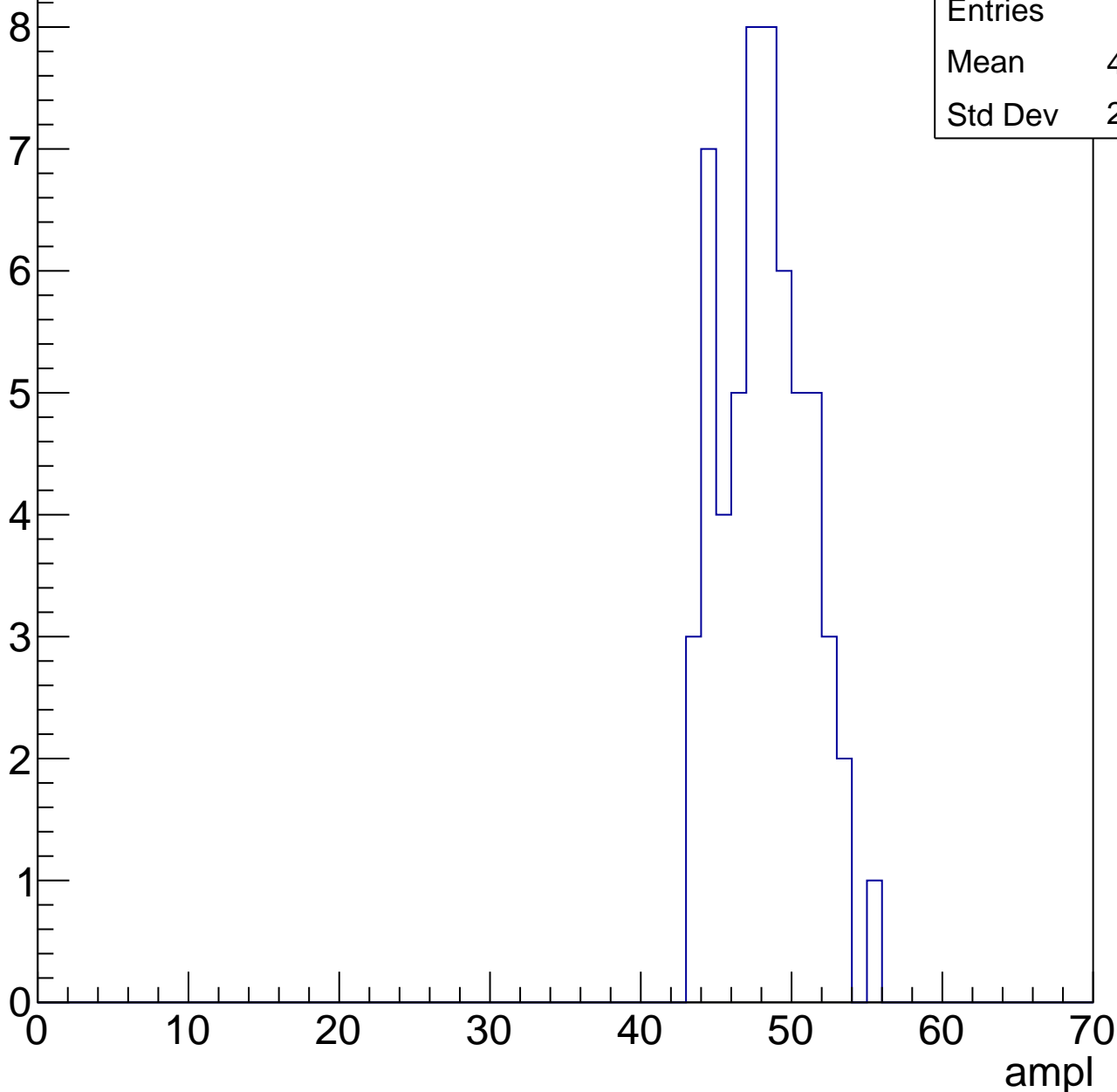


# B1L003S, U3-ch104, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

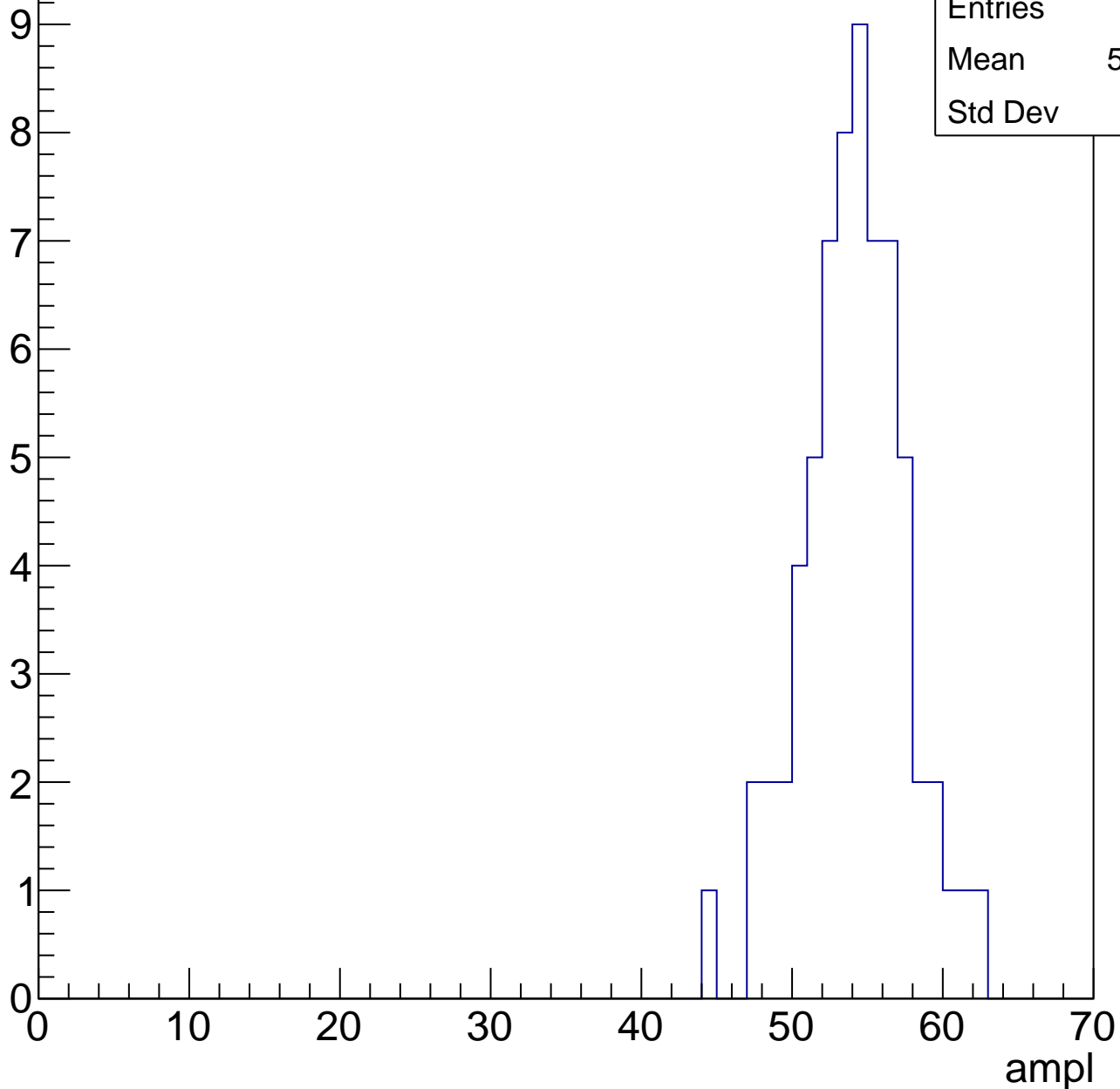
Entries	57
Mean	47.77
Std Dev	2.859



# B1L003S, U3-ch104, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U3-ch104, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

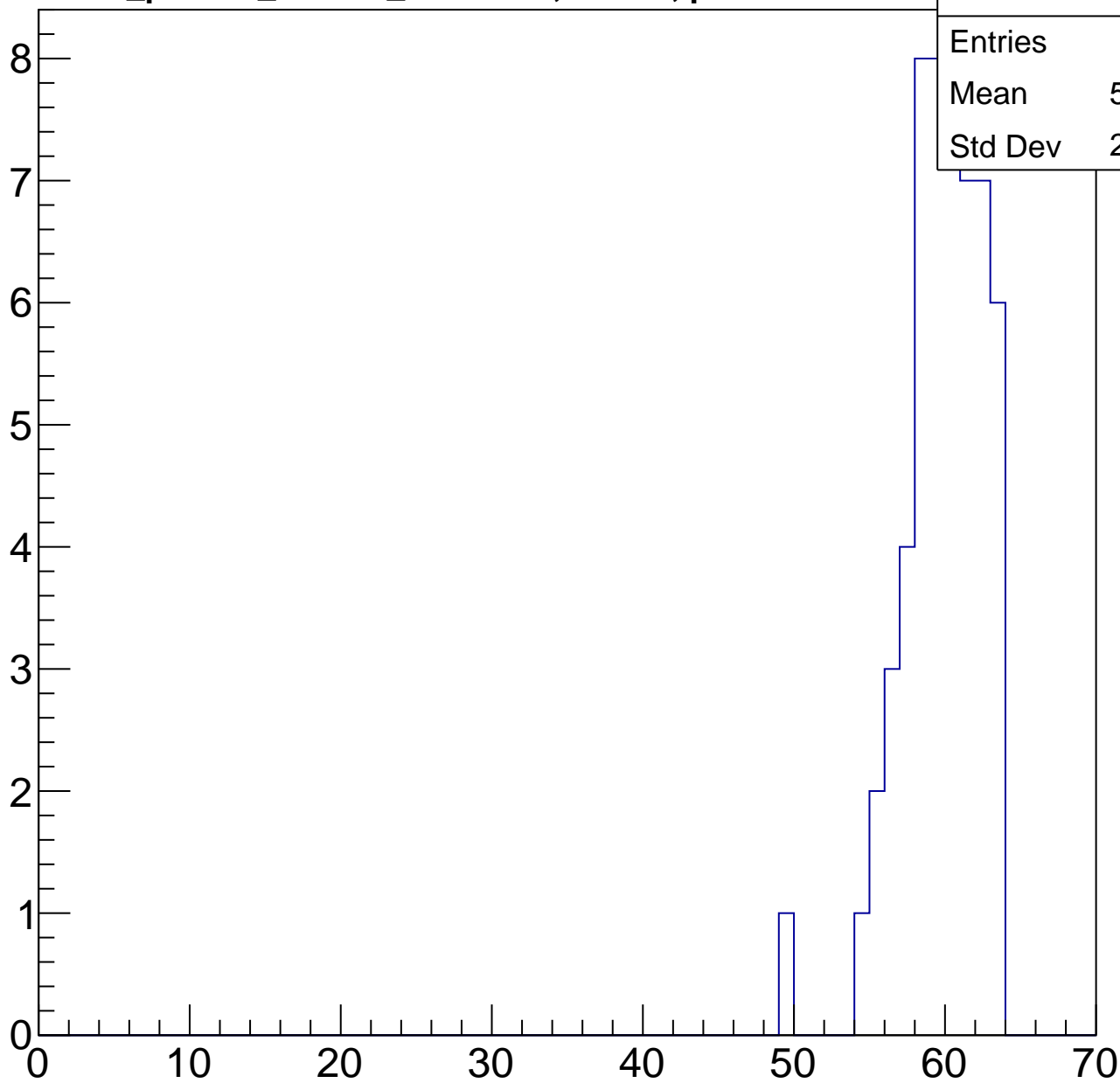
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	55
Mean	59.35
Std Dev	2.685

ampl

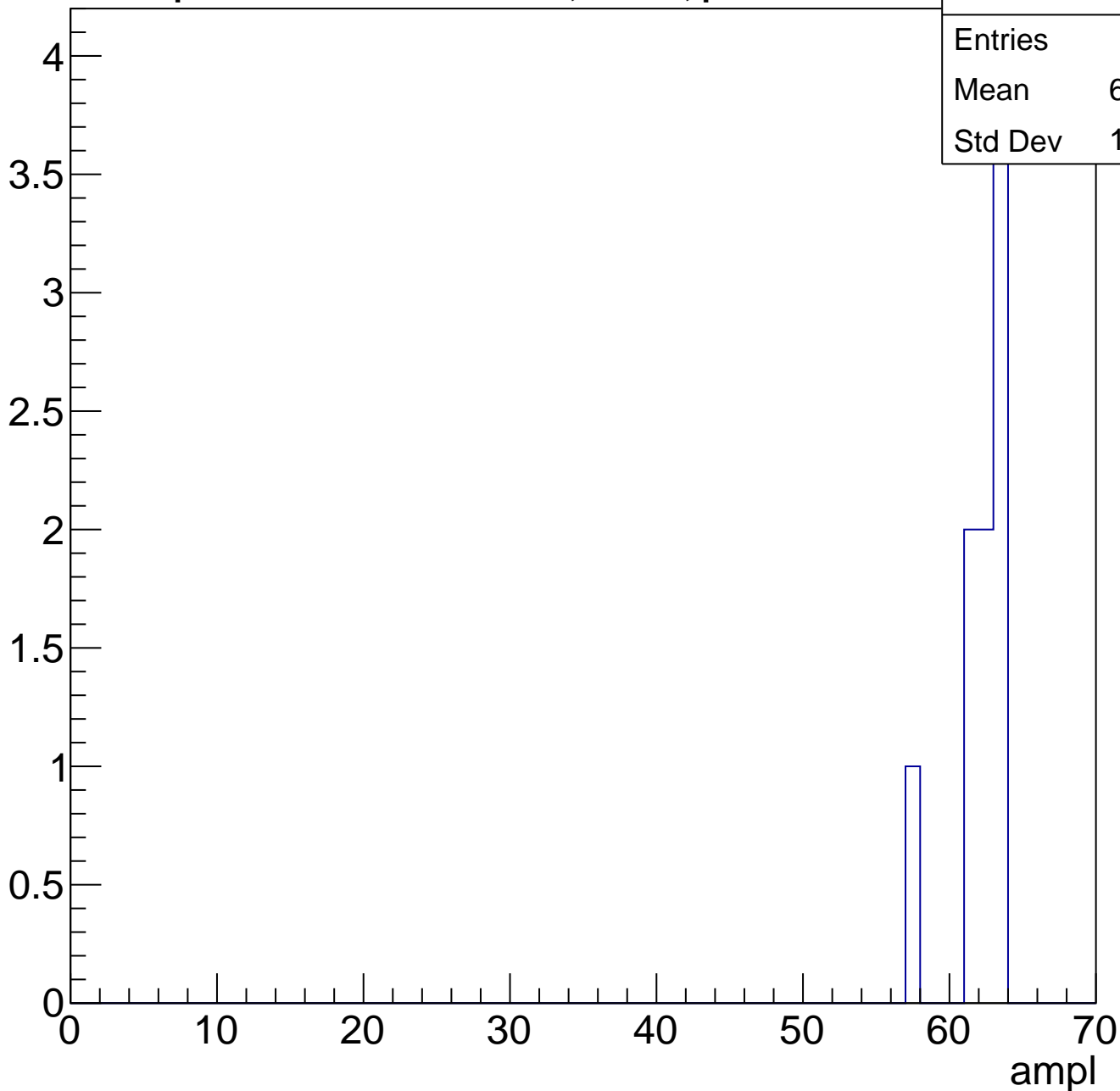
0 10 20 30 40 50 60 70



# B1L003S, U3-ch104, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

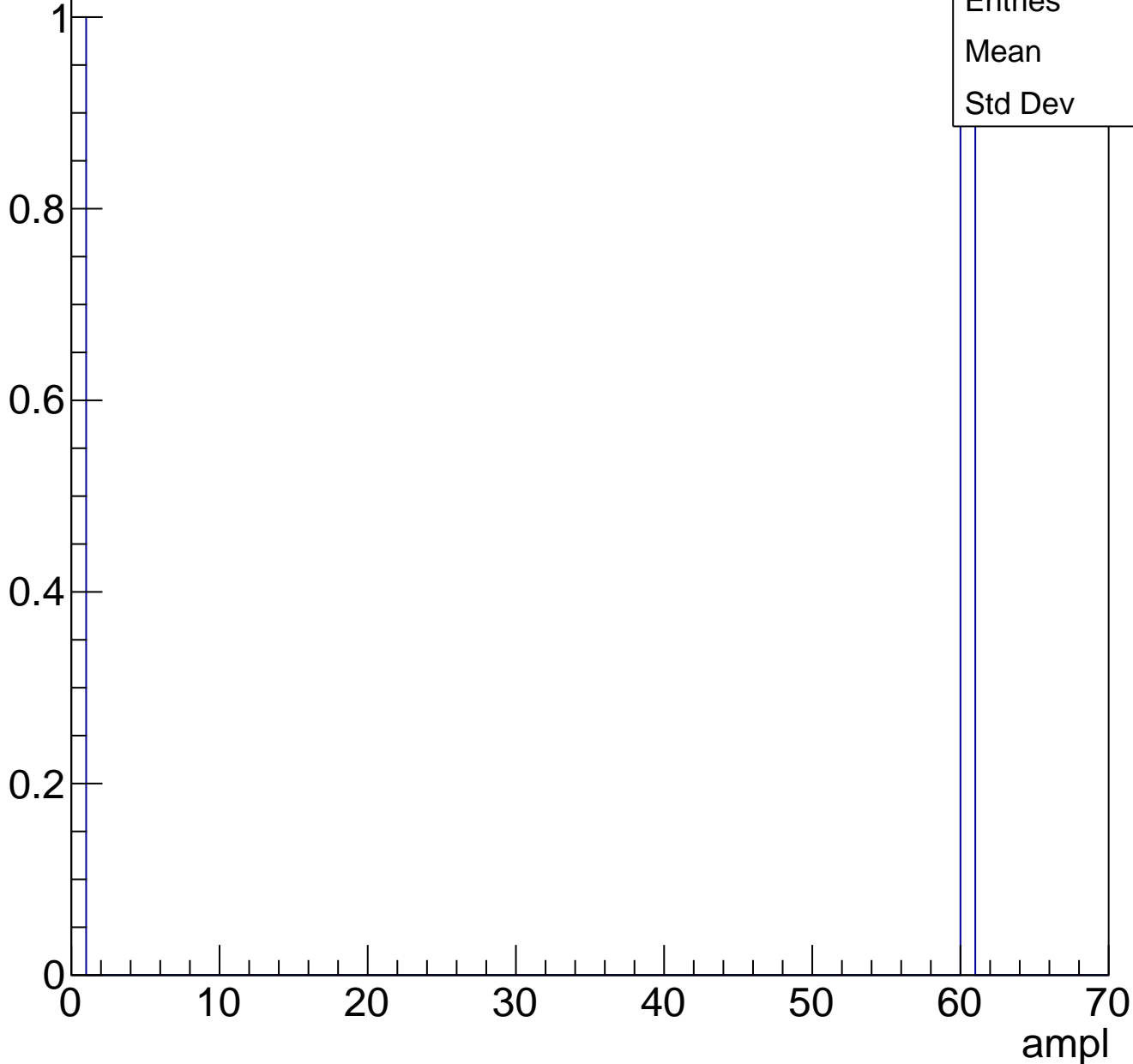




# B1L003S, U3-ch104, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U3-ch105, adc0

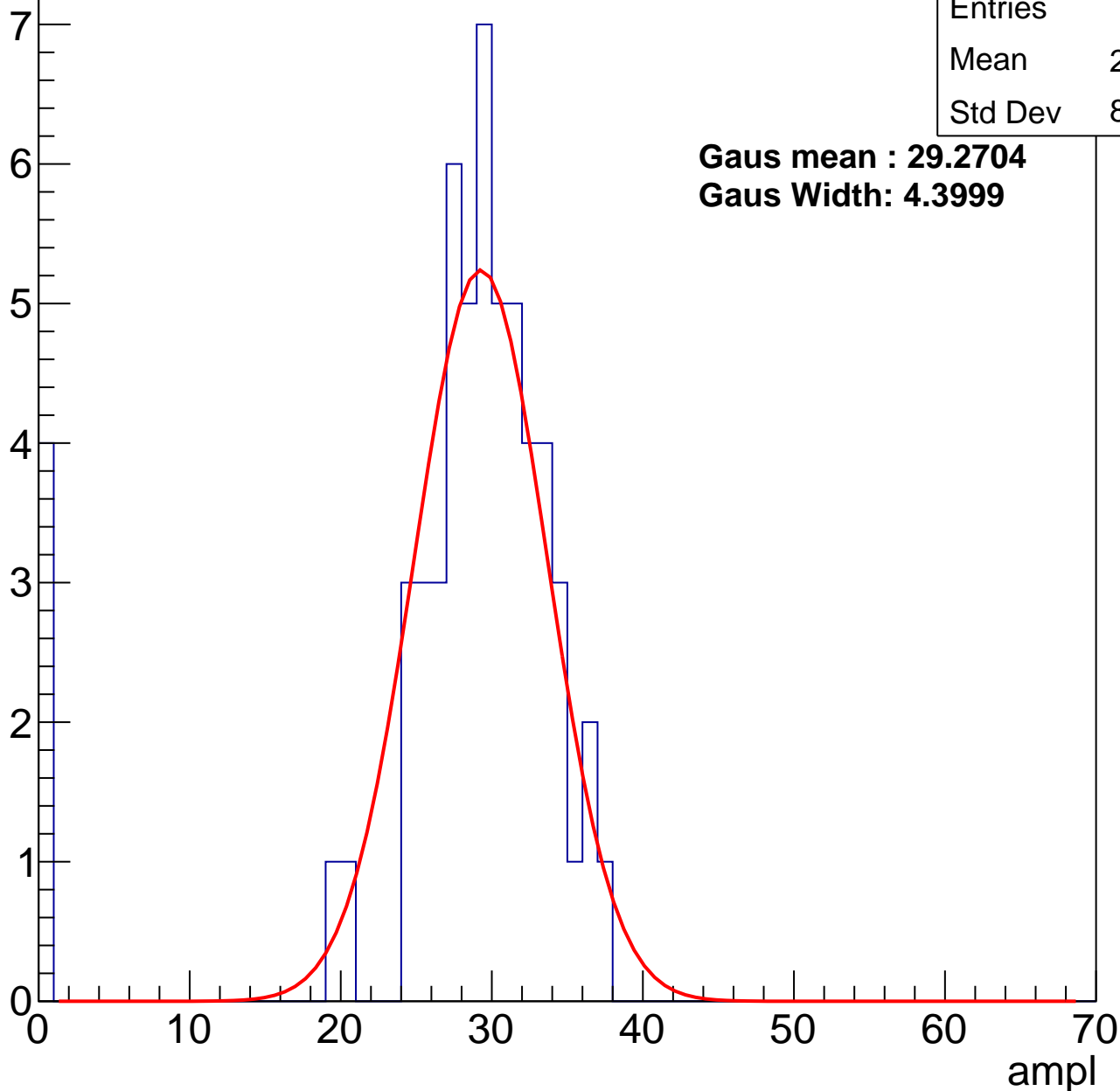
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	27.24
Std Dev	8.245

**Gaus mean : 29.2704**

**Gaus Width: 4.3999**



# B1L003S, U3-ch105, adc1

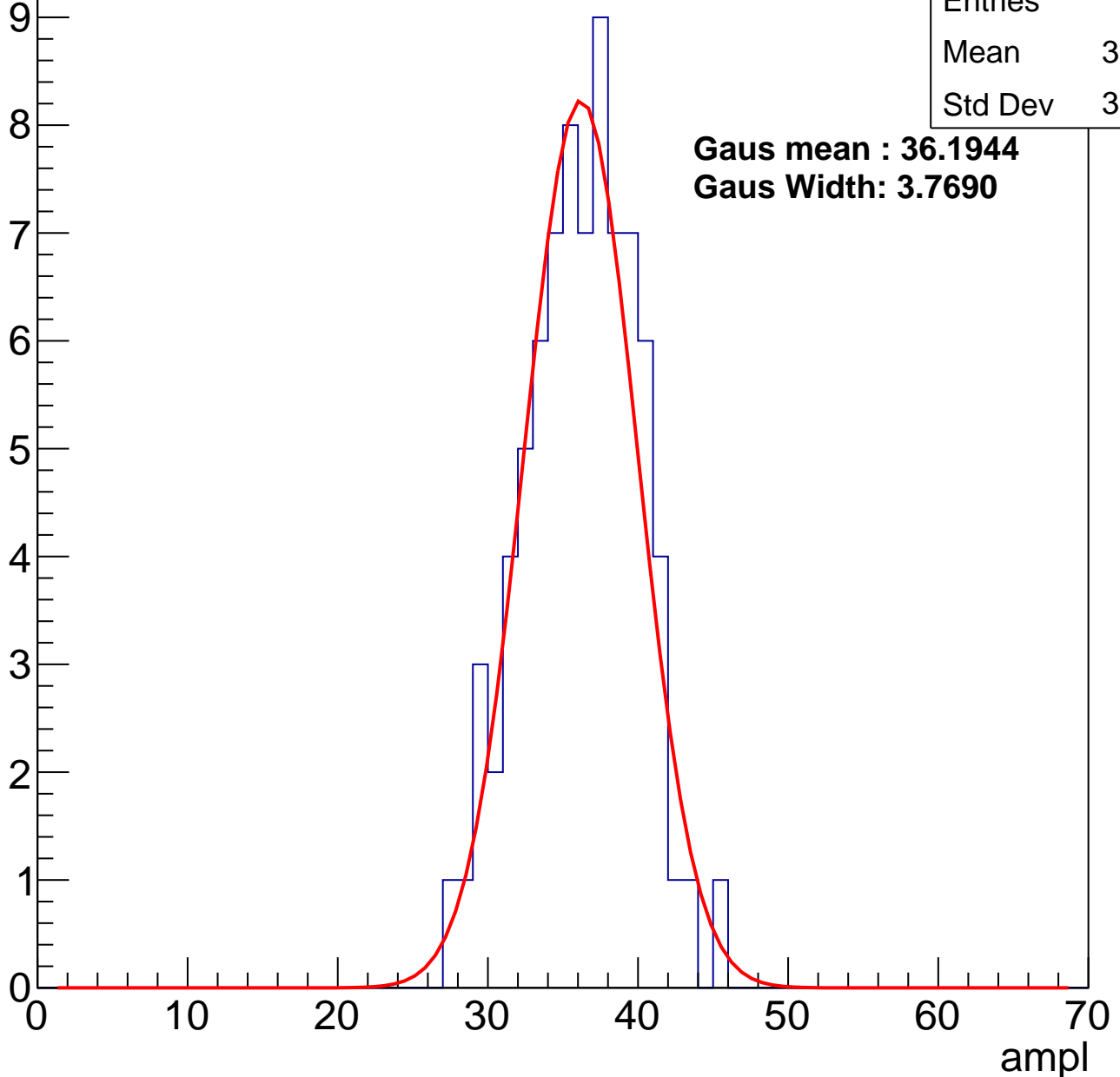
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	80
Mean	35.75
Std Dev	3.693

**Gaus mean : 36.1944**

**Gaus Width: 3.7690**



# B1L003S, U3-ch105, adc2

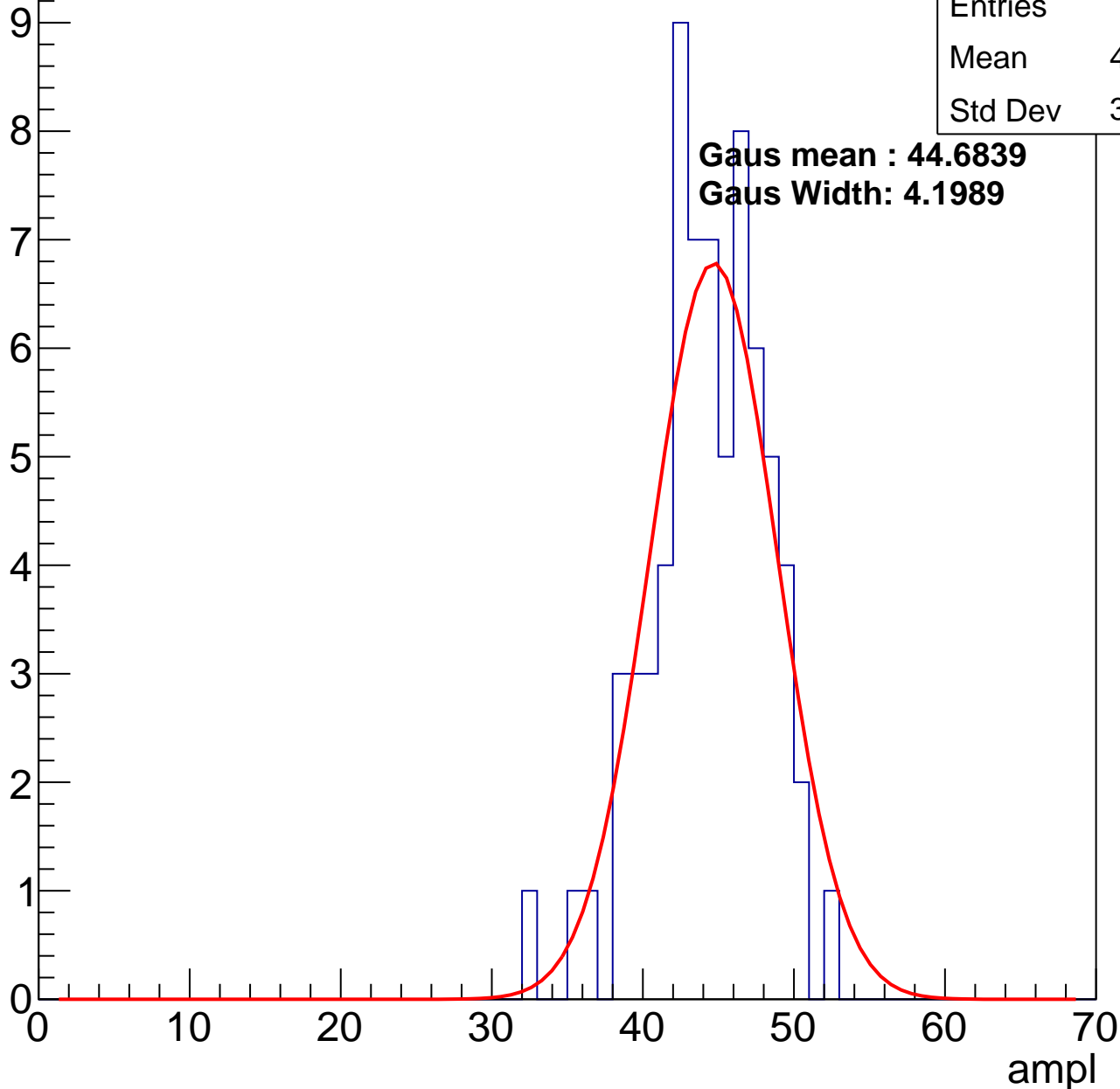
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	43.83
Std Dev	3.787

**Gaus mean : 44.6839**

**Gaus Width: 4.1989**

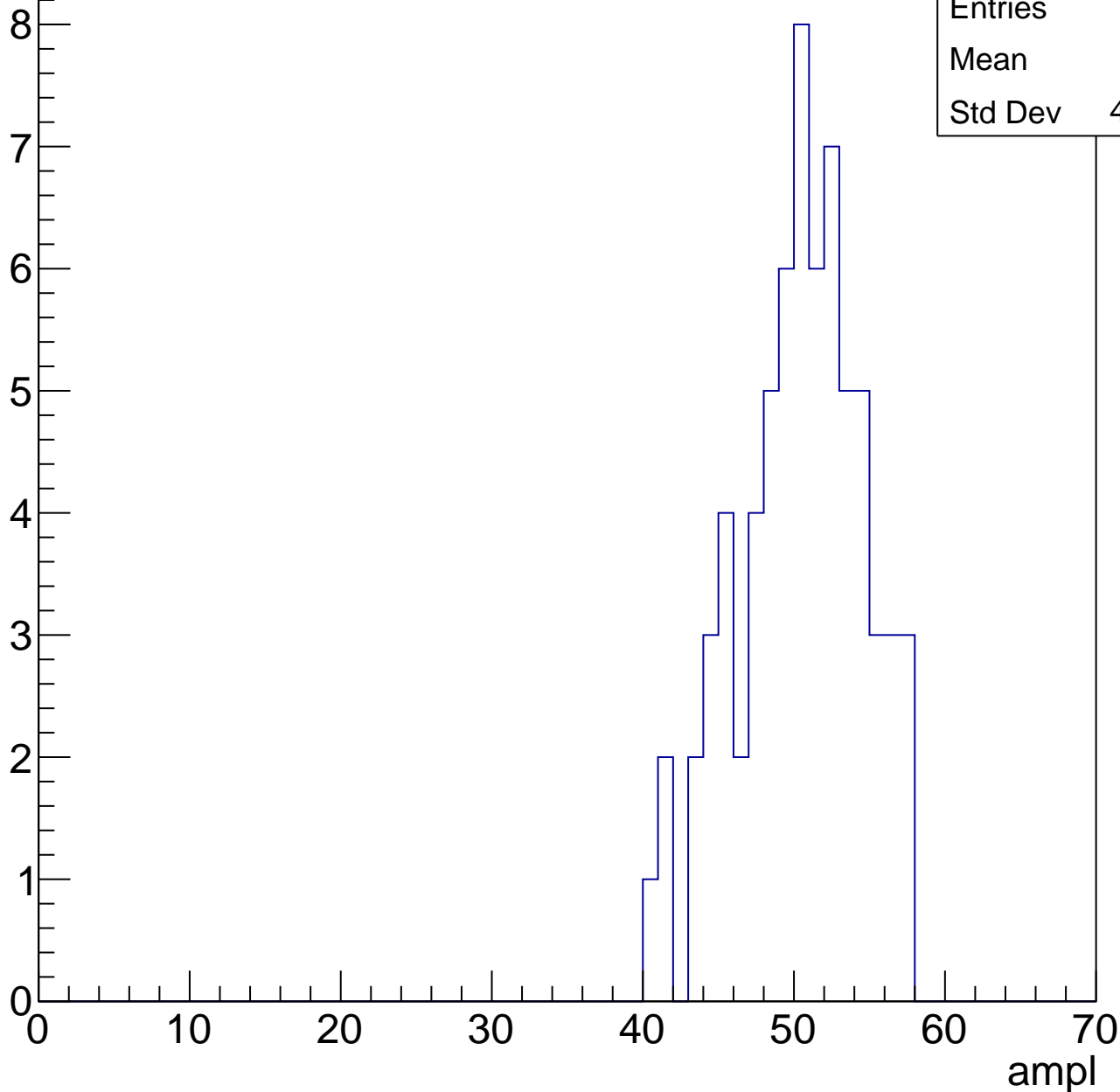


# B1L003S, U3-ch105, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	49.9
Std Dev	4.083

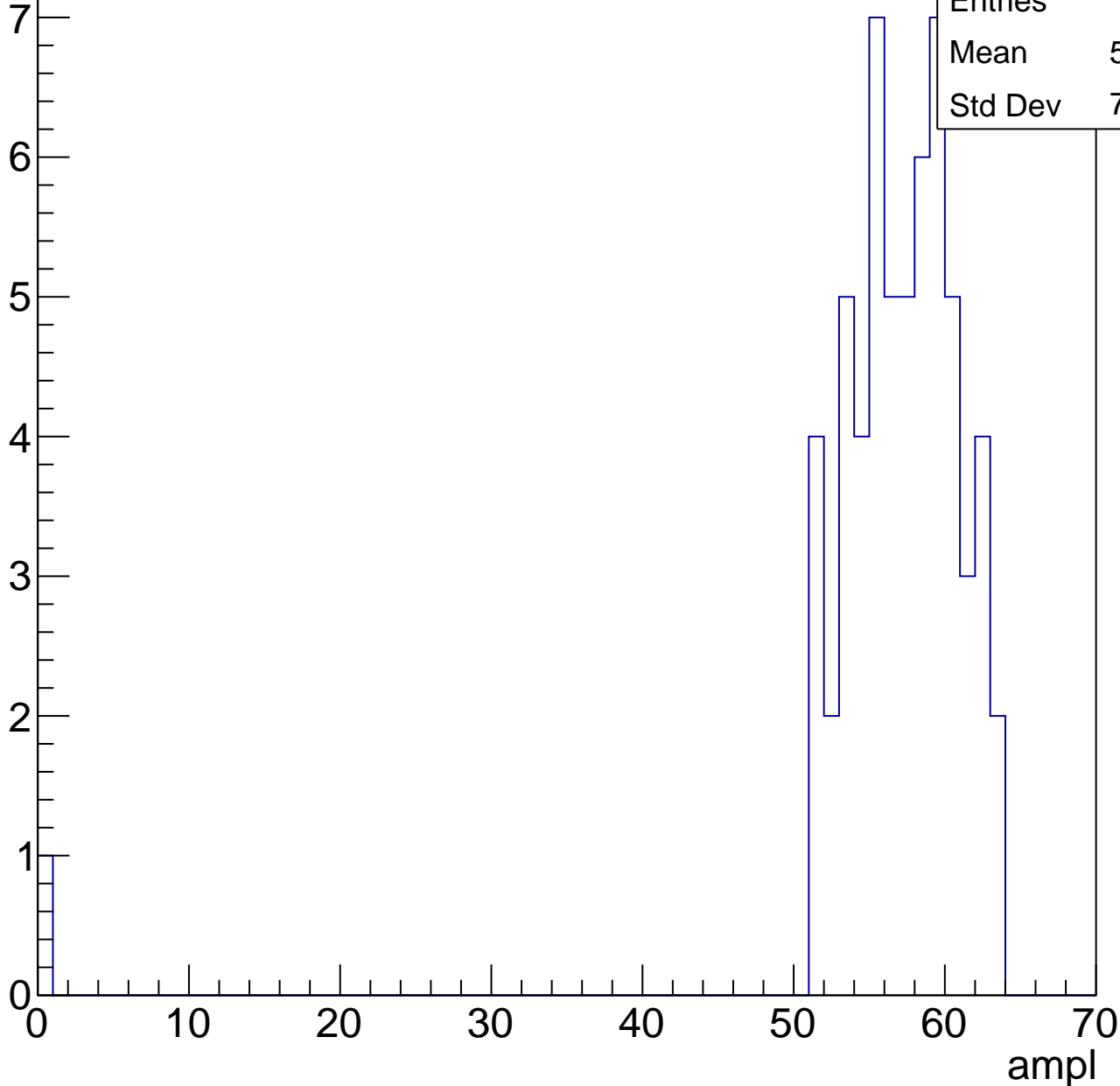


# B1L003S, U3-ch105, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	55.95
Std Dev	7.984

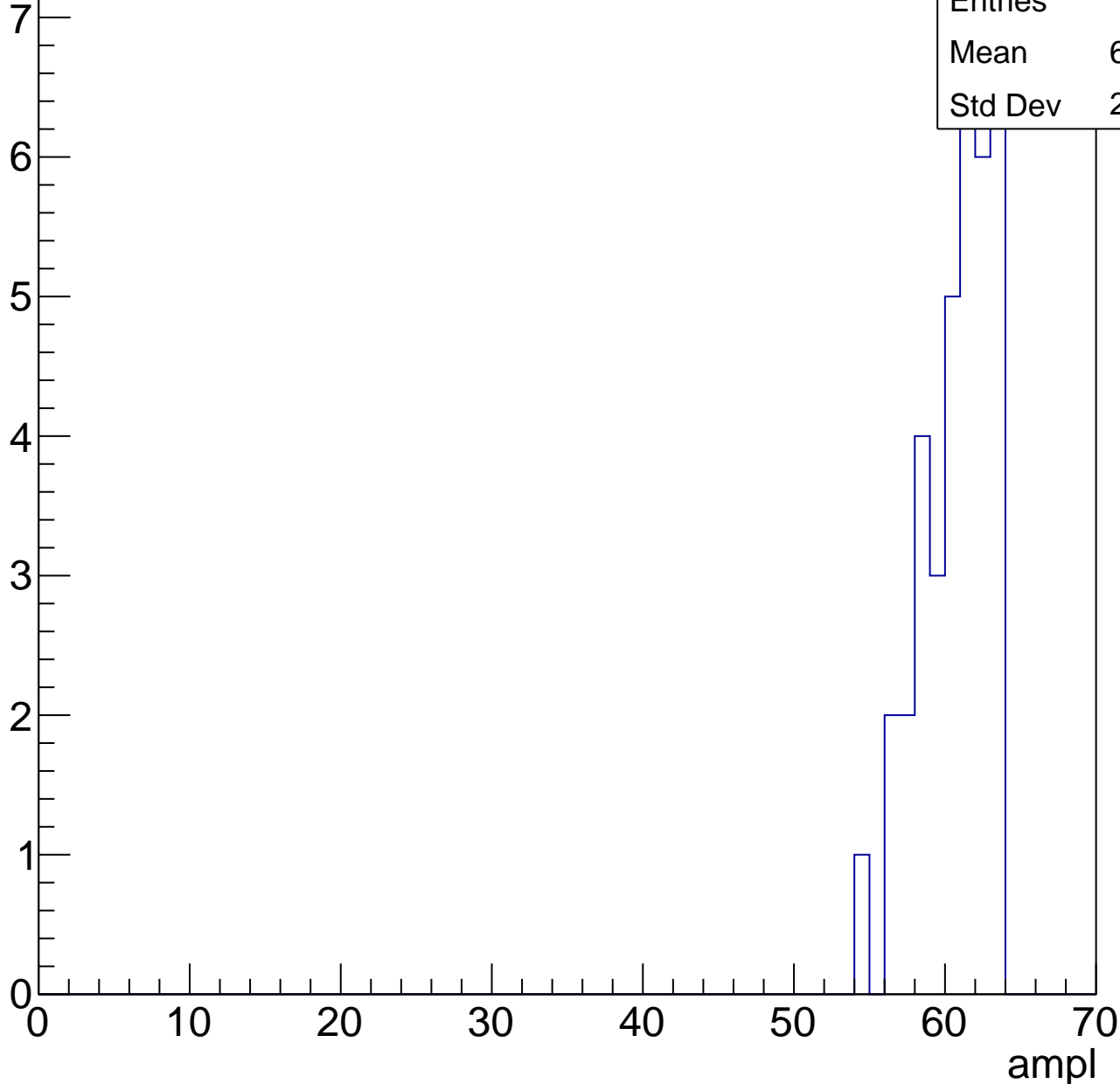


# B1L003S, U3-ch105, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	37
Mean	60.24
Std Dev	2.306



# B1L003S, U3-ch105, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

1

Mean

63

Std Dev

0



# B1L003S, U3-ch105, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L003S, U3-ch106, adc0

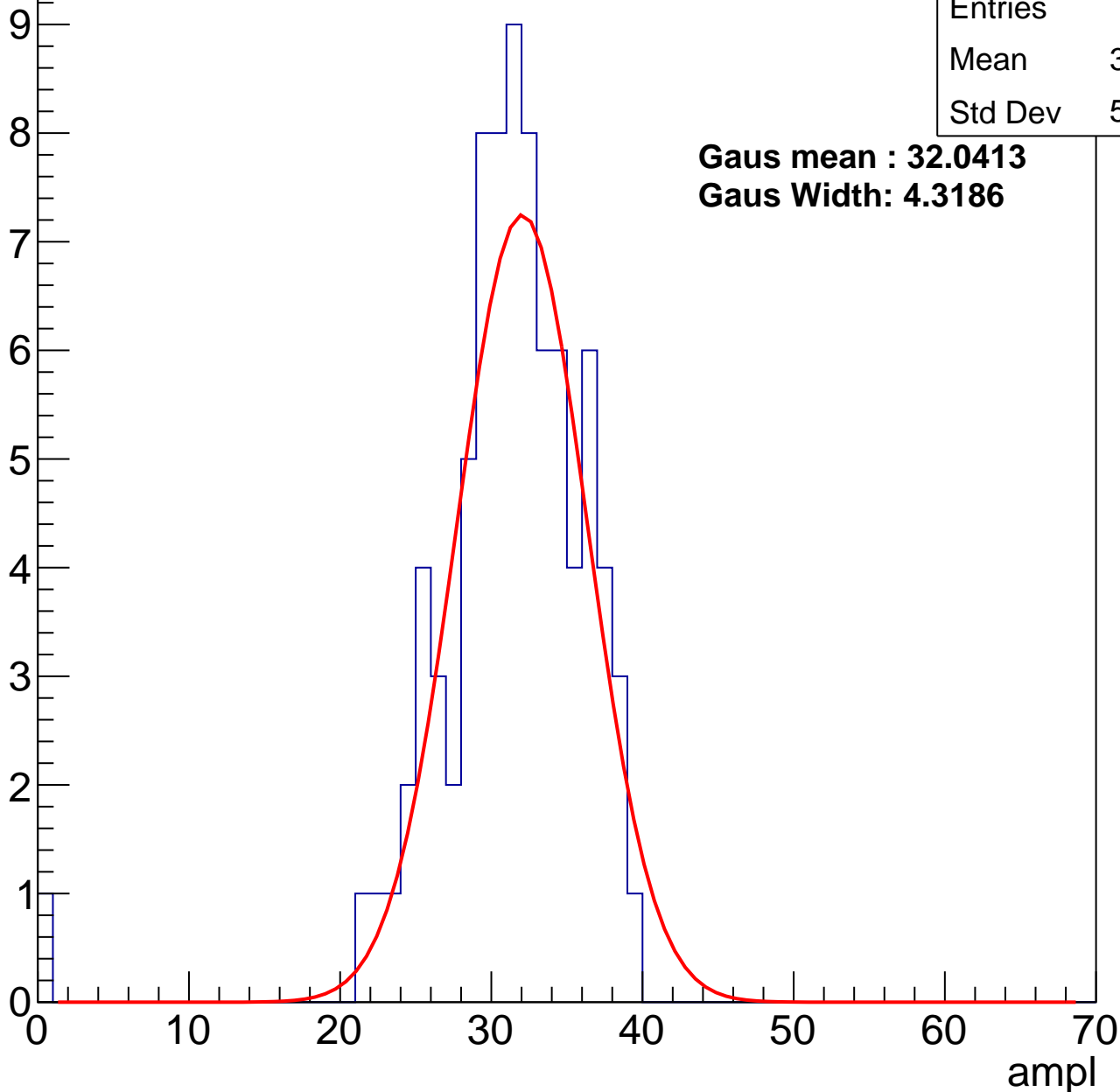
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	83
Mean	30.75
Std Dev	5.252

**Gaus mean : 32.0413**

**Gaus Width: 4.3186**



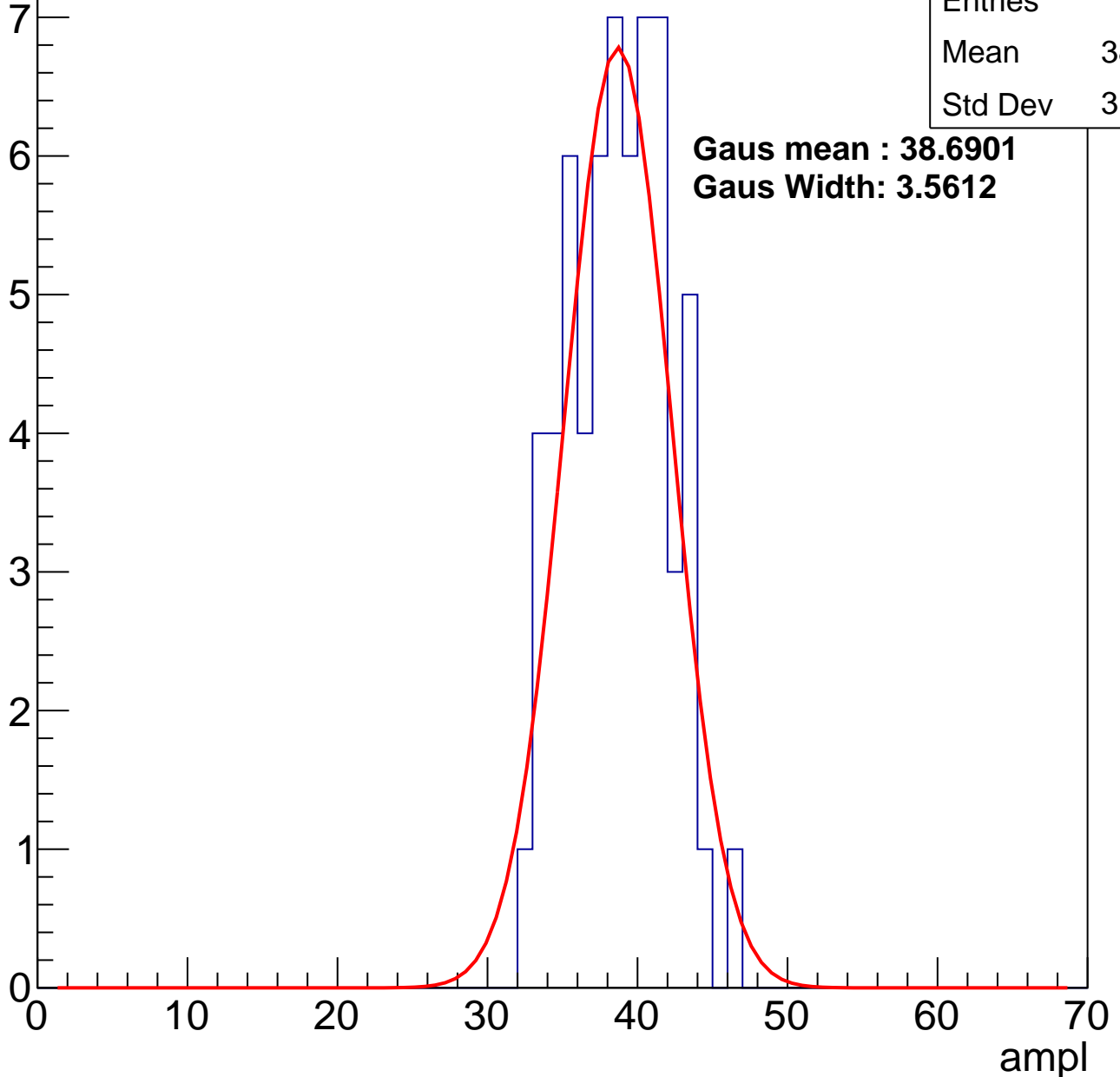
# B1L003S, U3-ch106, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	38.29
Std Dev	3.215

**Gaus mean : 38.6901**  
**Gaus Width: 3.5612**



# B1L003S, U3-ch106, adc2

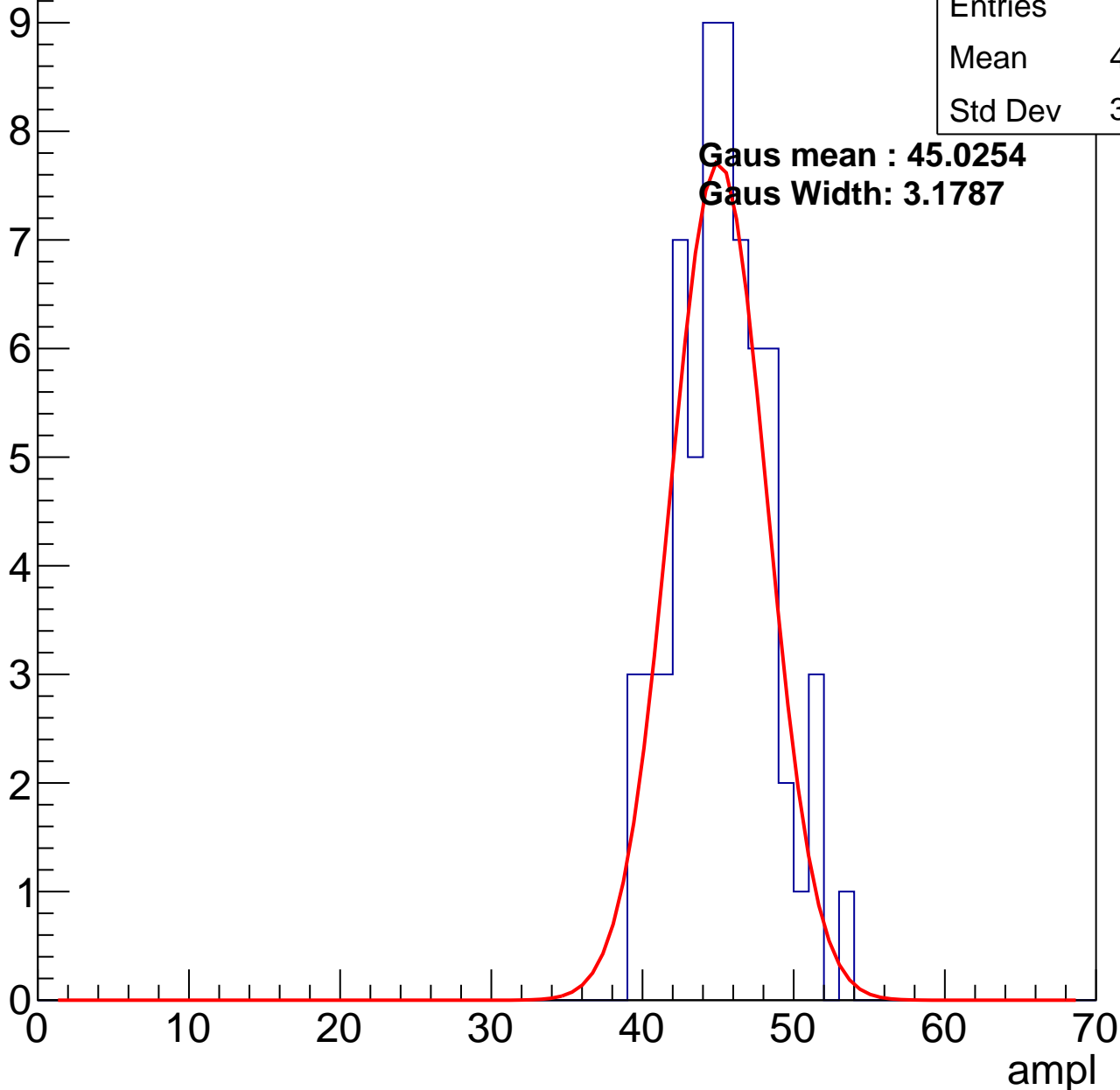
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	44.86
Std Dev	3.127

**Gaus mean : 45.0254**

**Gaus Width: 3.1787**

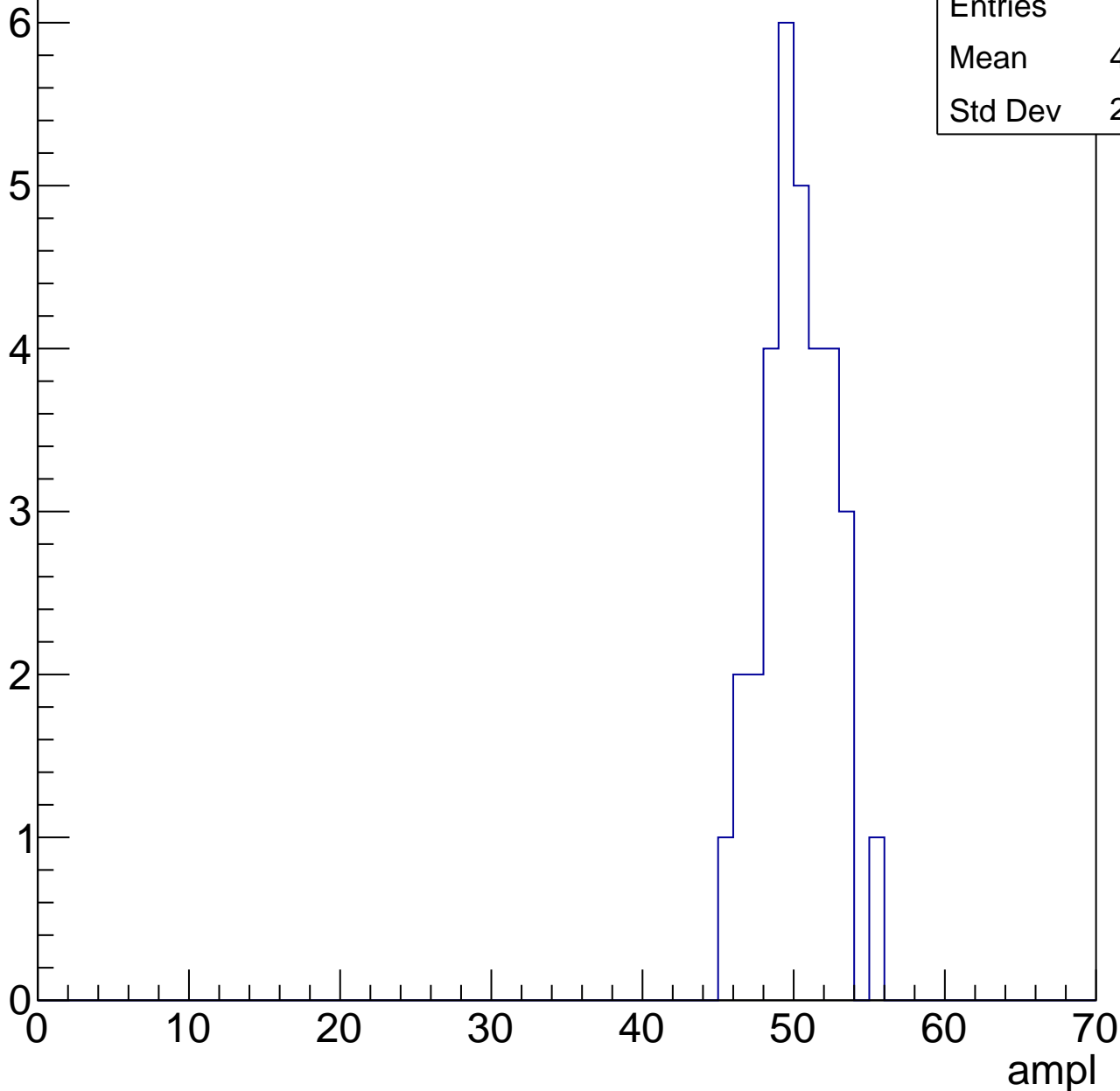


# B1L003S, U3-ch106, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	32
Mean	49.78
Std Dev	2.288

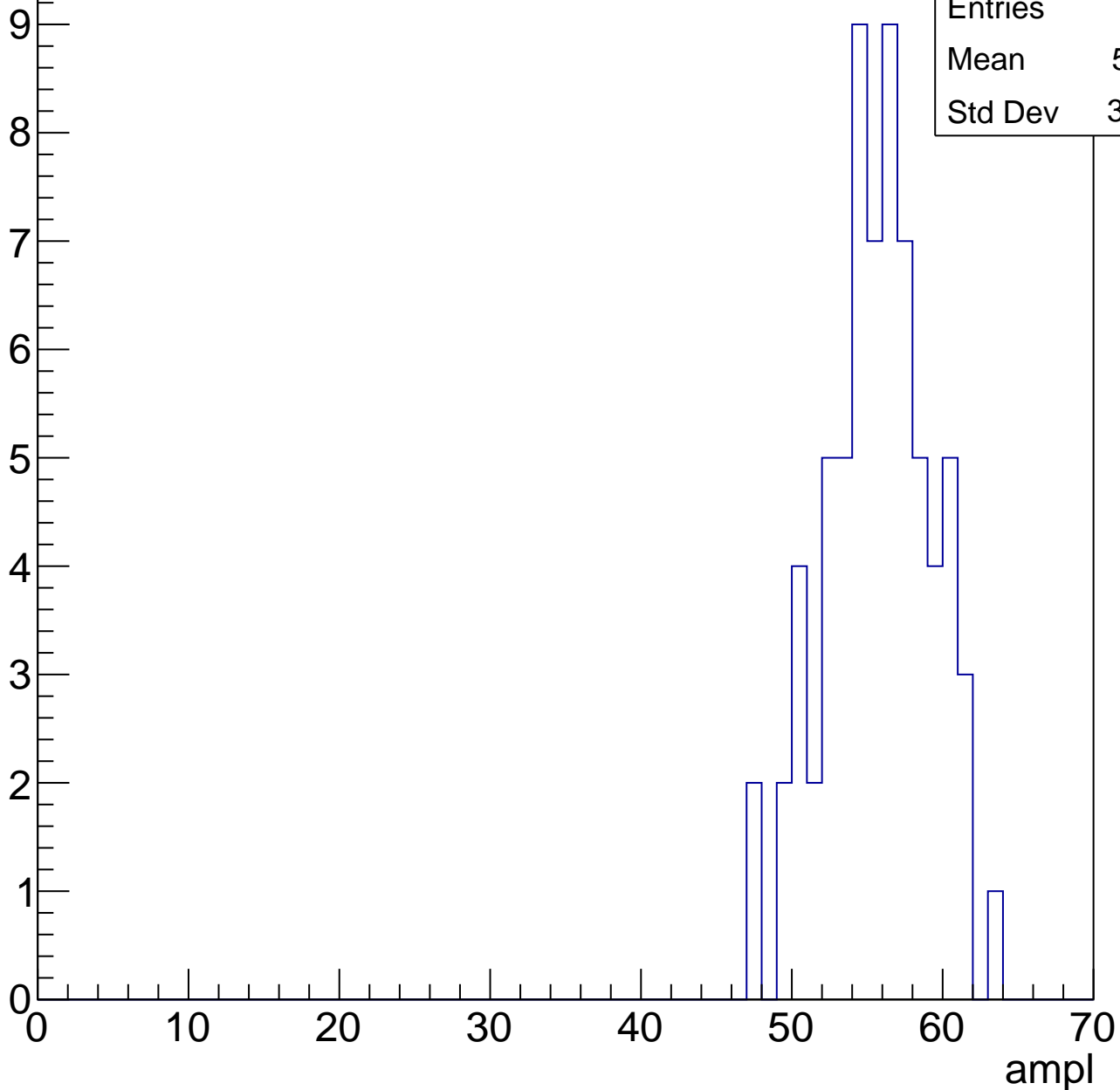


# B1L003S, U3-ch106, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	55.21
Std Dev	3.476

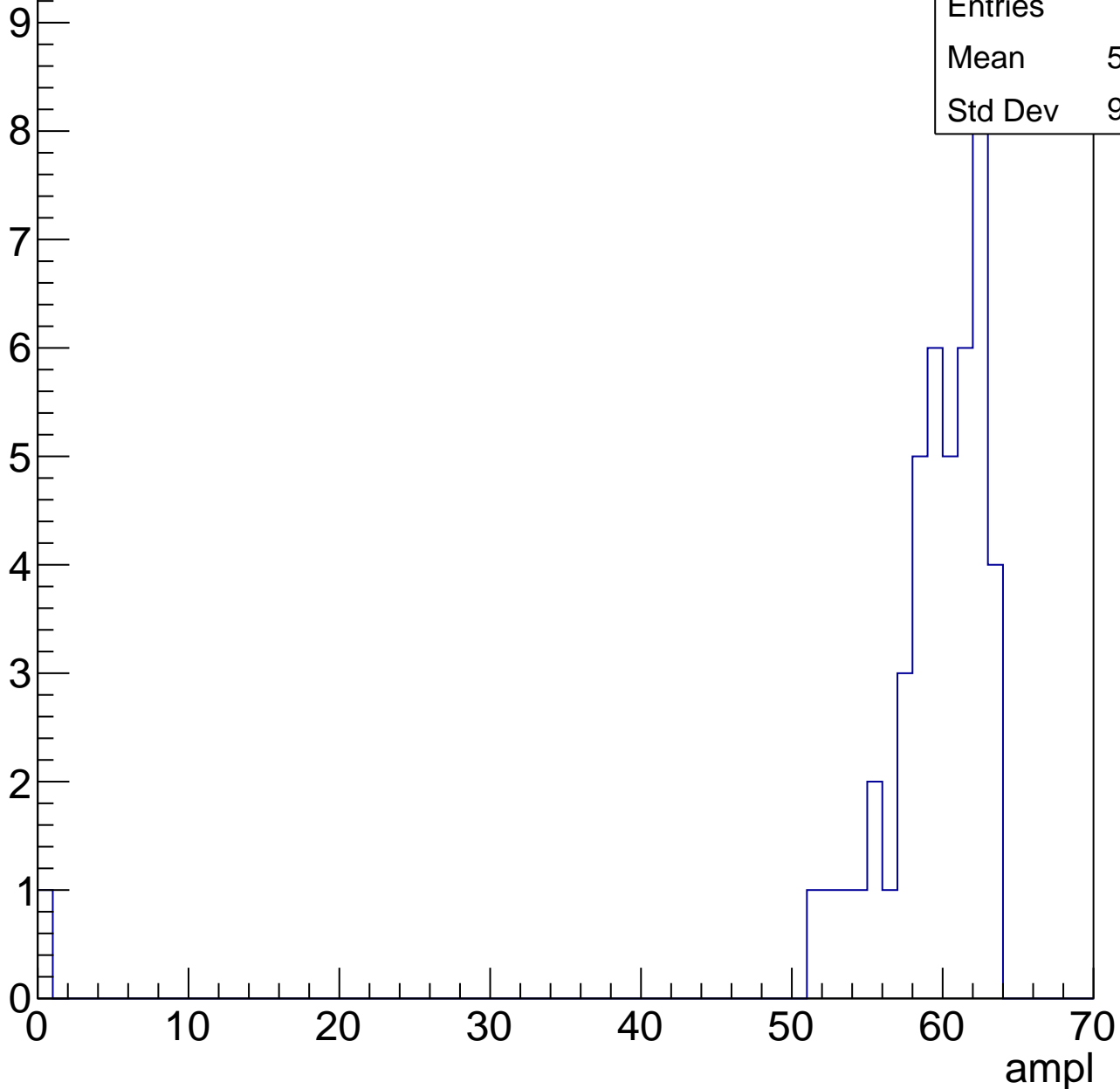


# B1L003S, U3-ch106, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	46
Mean	57.98
Std Dev	9.135

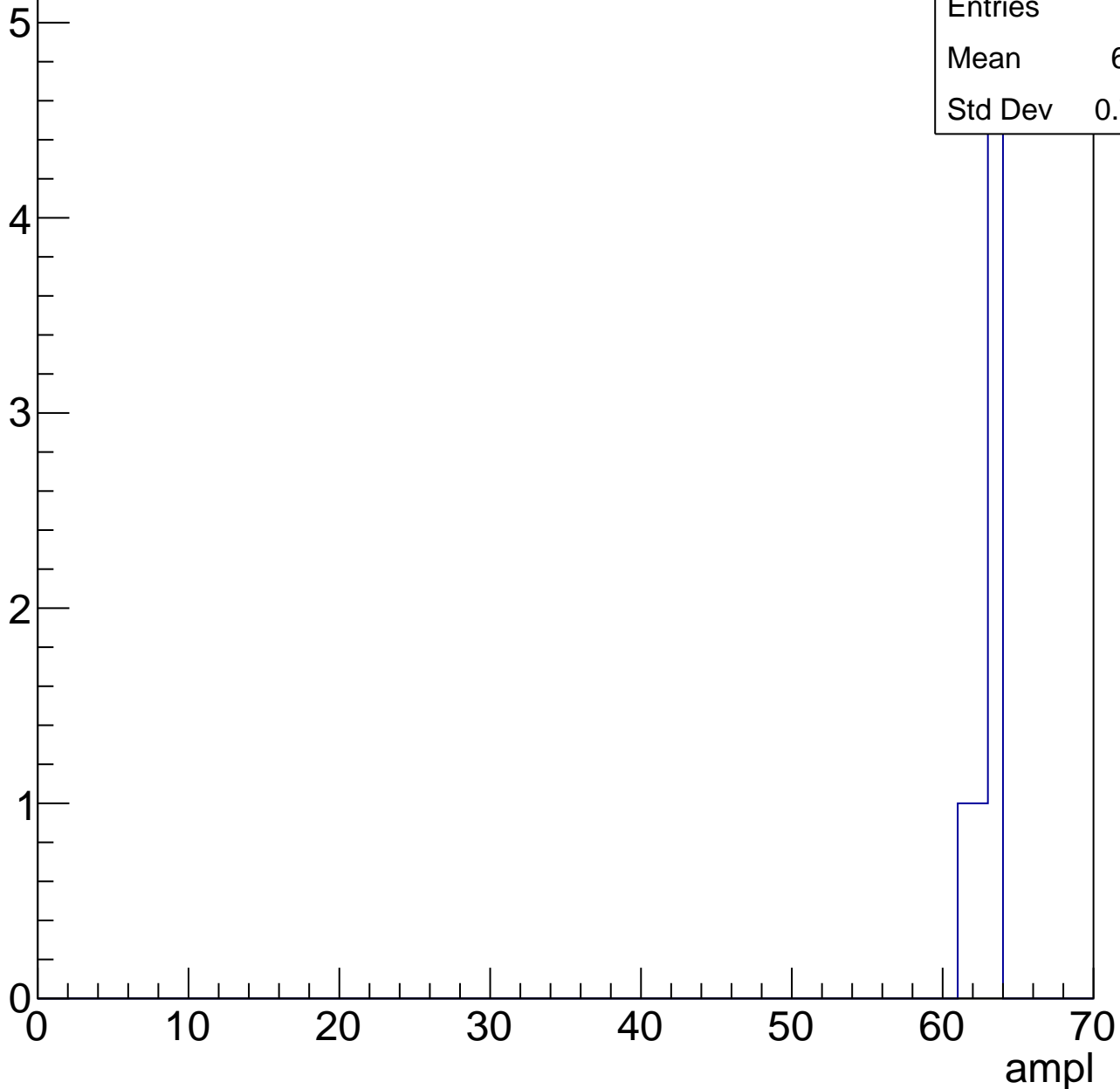


# B1L003S, U3-ch106, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	7
Mean	62.57
Std Dev	0.7284





# B1L003S, U3-ch106, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U3-ch107, adc0

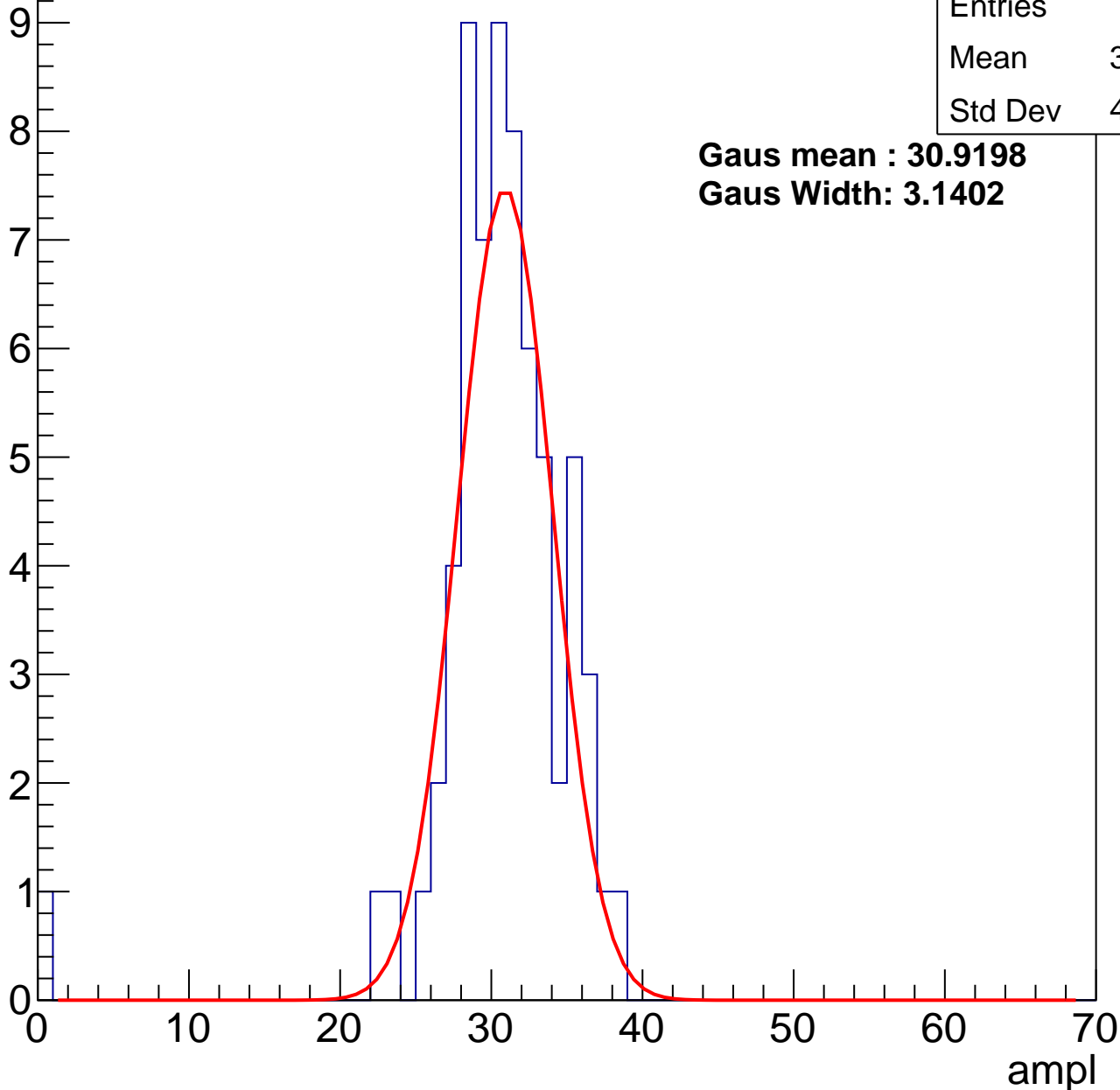
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	30.09
Std Dev	4.929

**Gaus mean : 30.9198**

**Gaus Width: 3.1402**



# B1L003S, U3-ch107, adc1

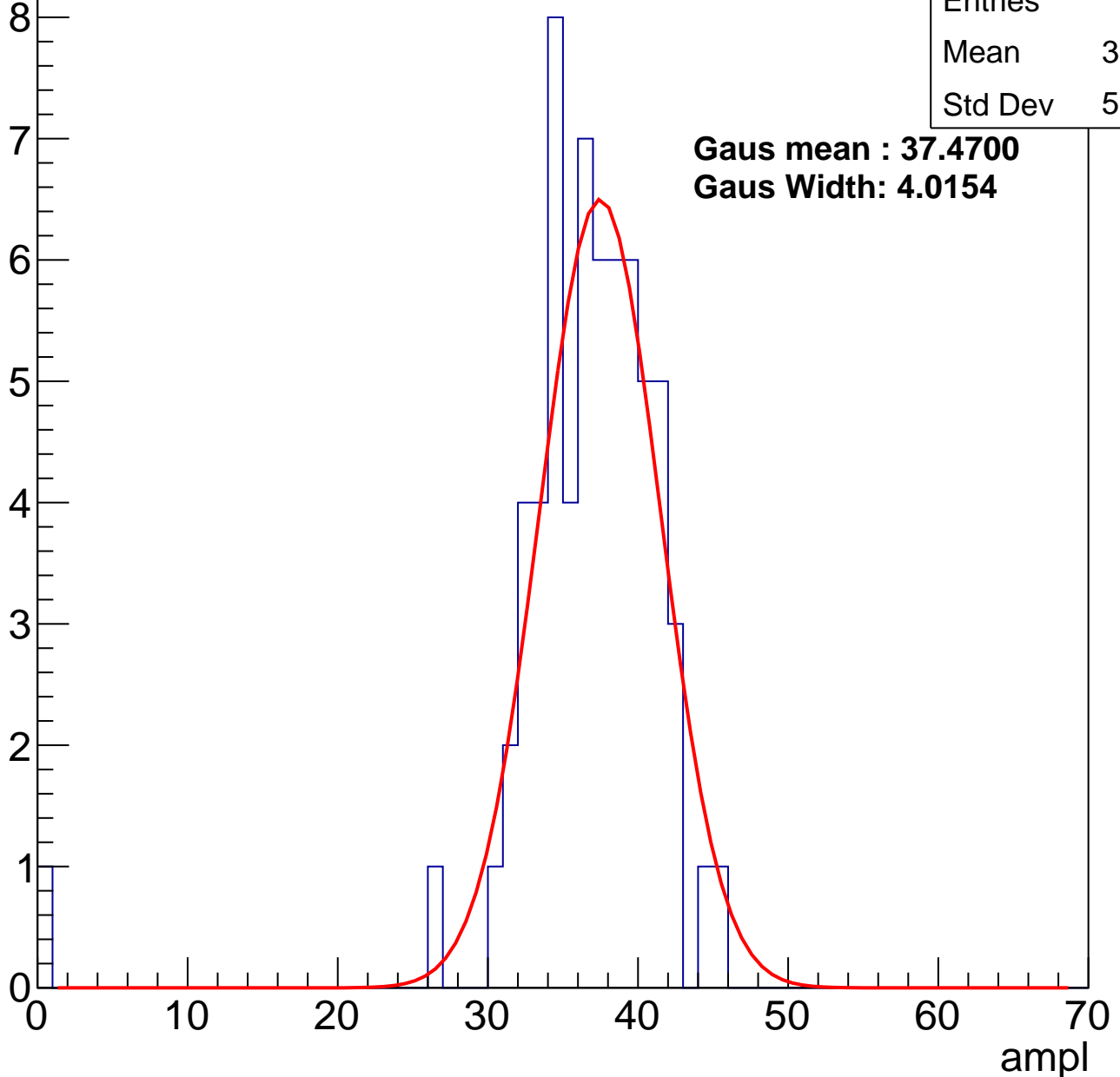
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	36.09
Std Dev	5.764

**Gaus mean : 37.4700**

**Gaus Width: 4.0154**



# B1L003S, U3-ch107, adc2

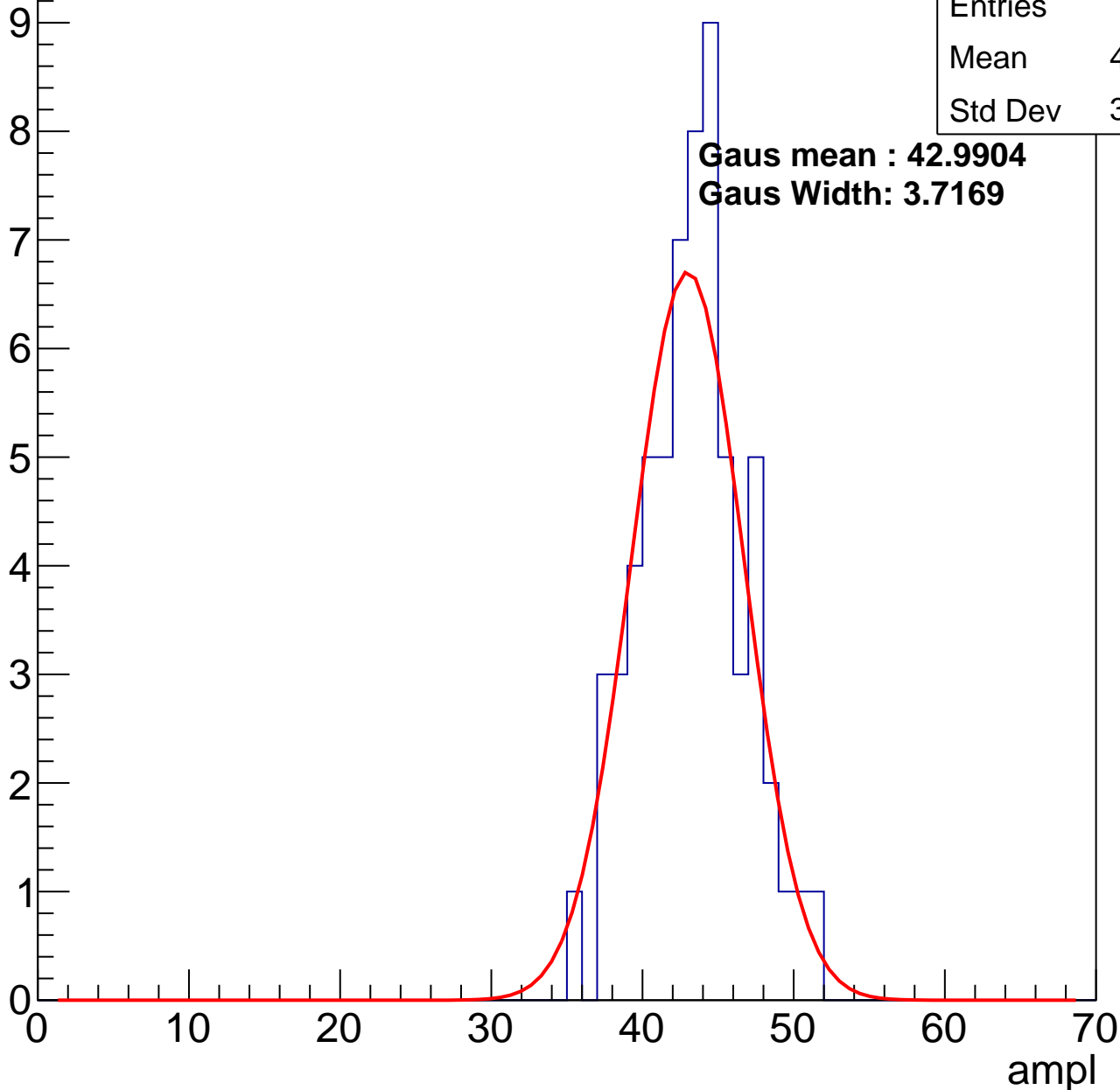
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	42.84
Std Dev	3.372

**Gaus mean : 42.9904**

**Gaus Width: 3.7169**

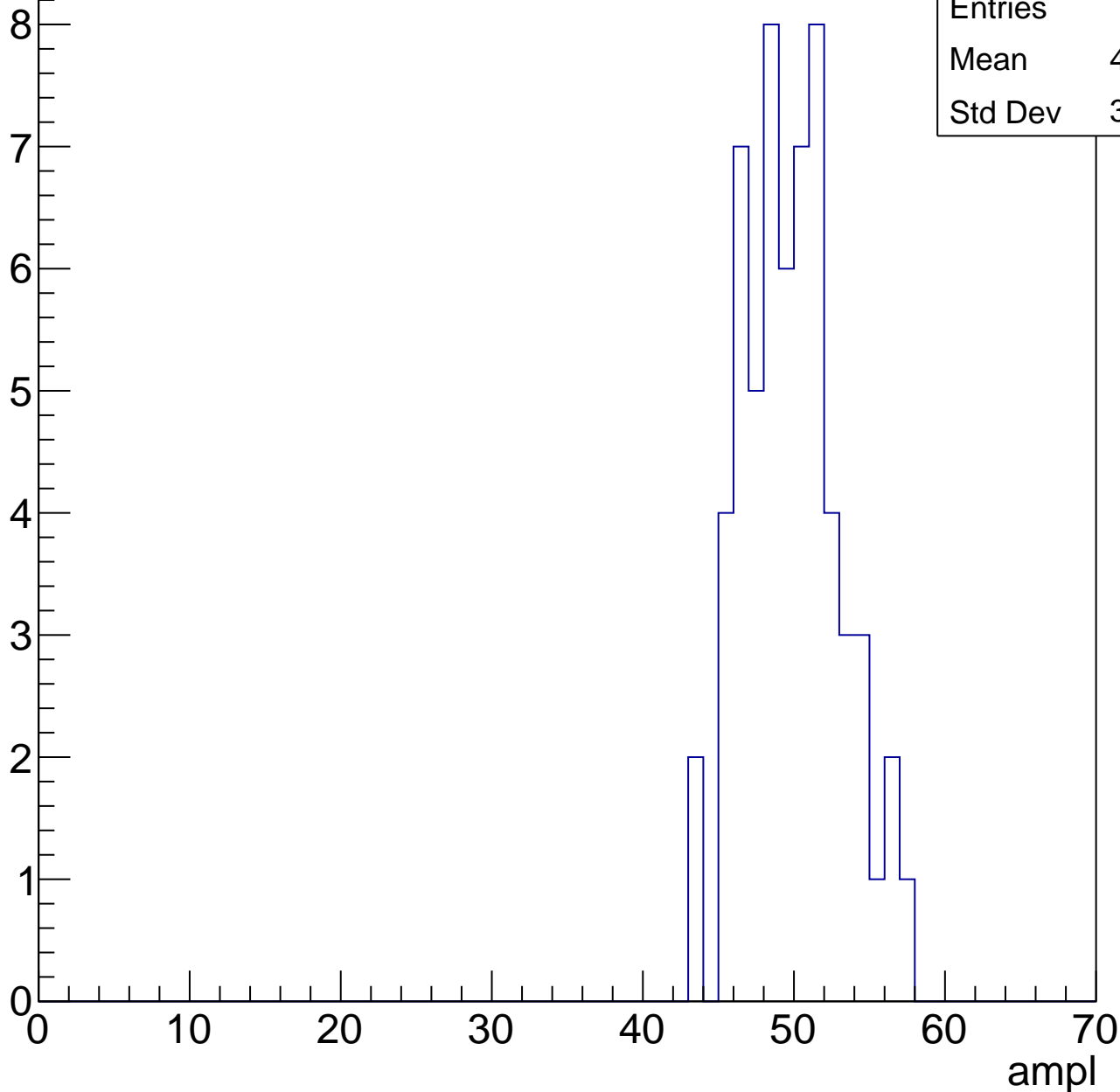


# B1L003S, U3-ch107, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	49.38
Std Dev	3.173

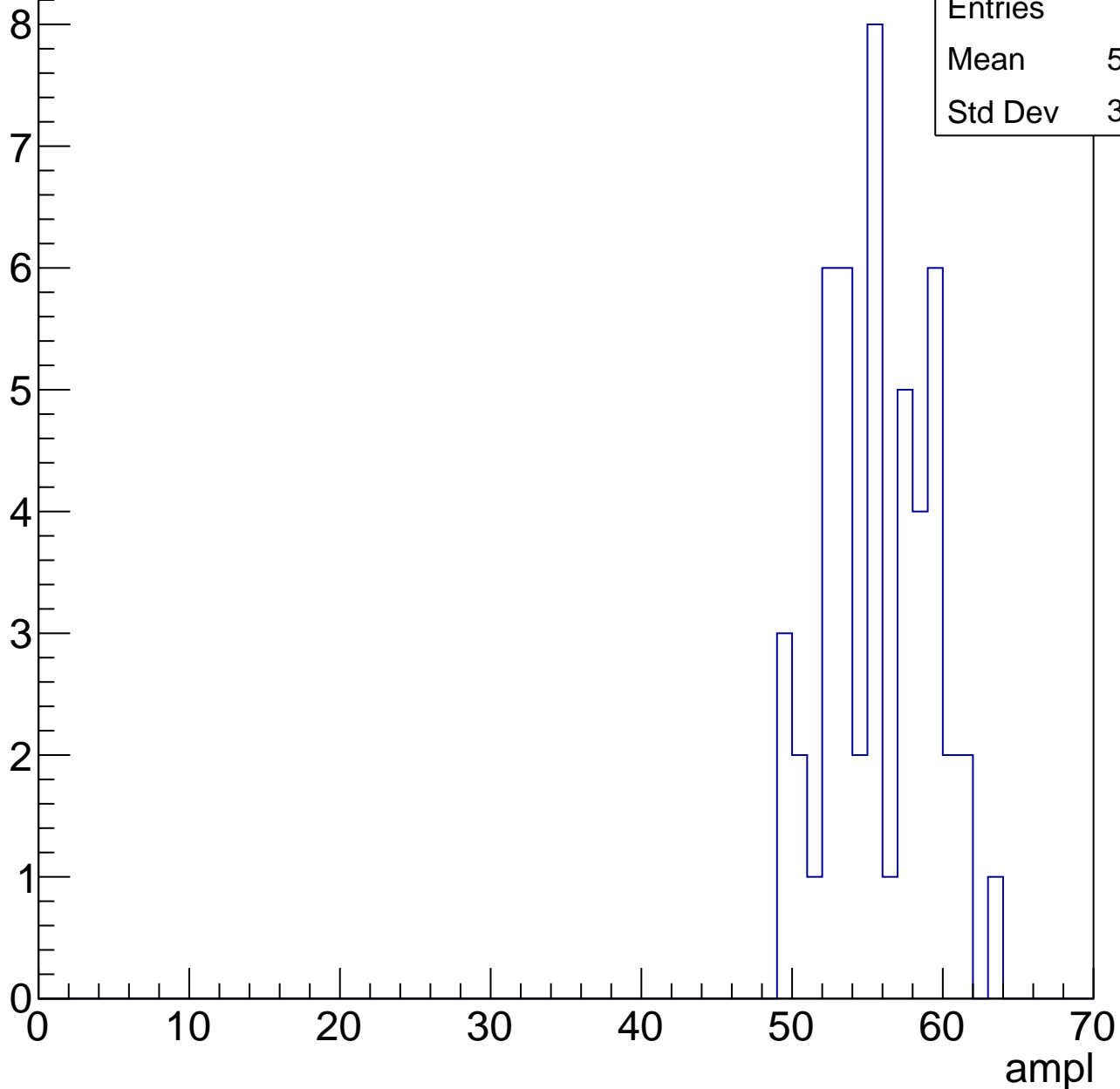


# B1L003S, U3-ch107, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	49
Mean	55.27
Std Dev	3.469

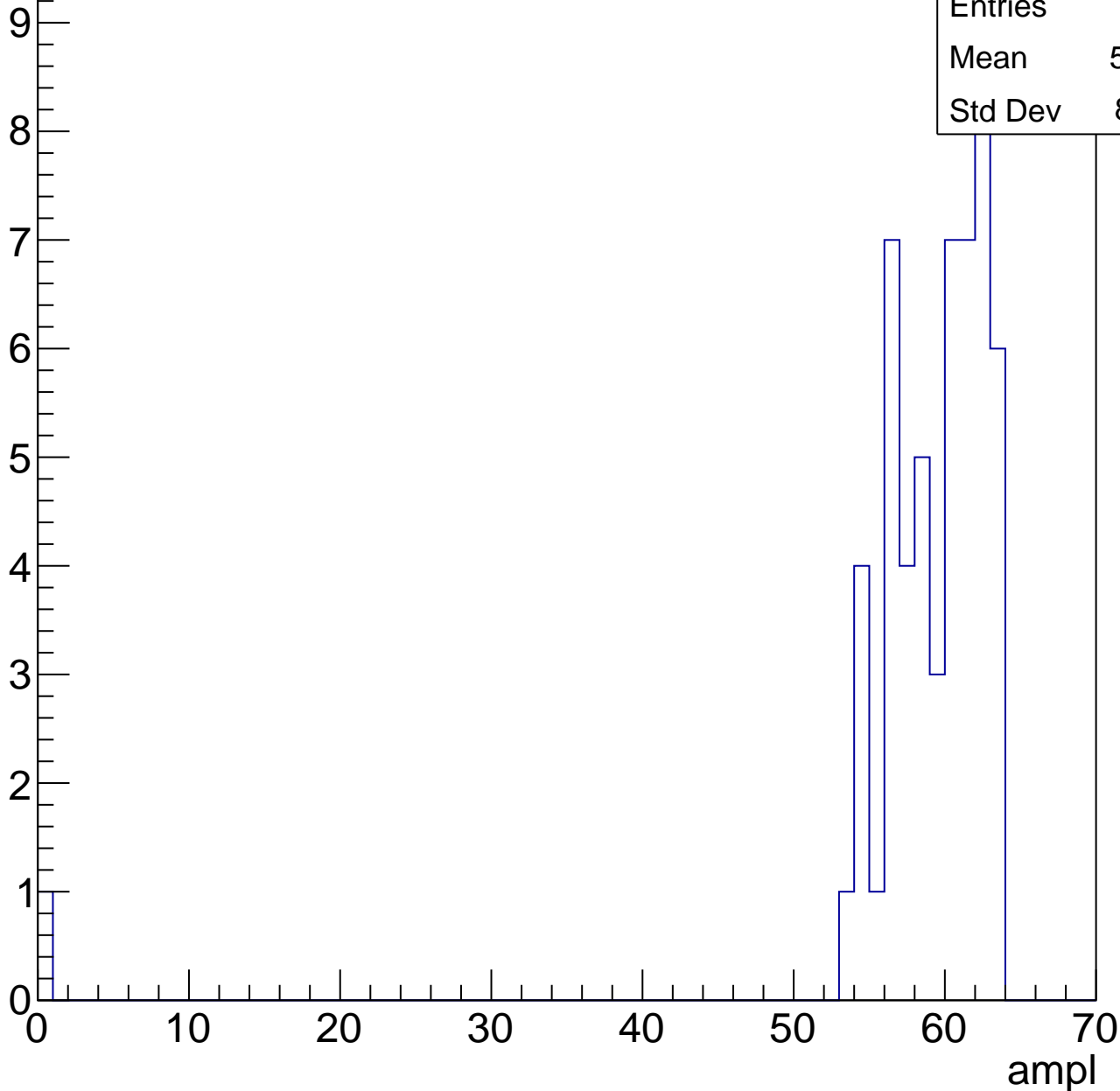


# B1L003S, U3-ch107, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	58.07
Std Dev	8.401



# B1L003S, U3-ch107, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries

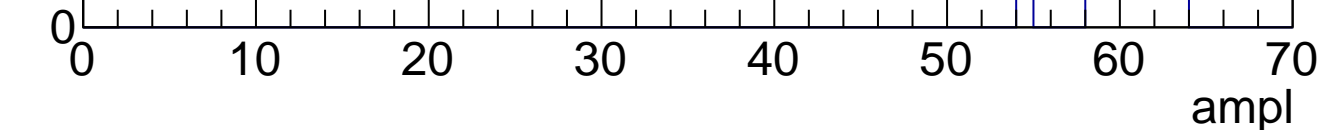
9

Mean

60.33

Std Dev

2.828





# B1L003S, U3-ch107, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U3-ch108, adc0

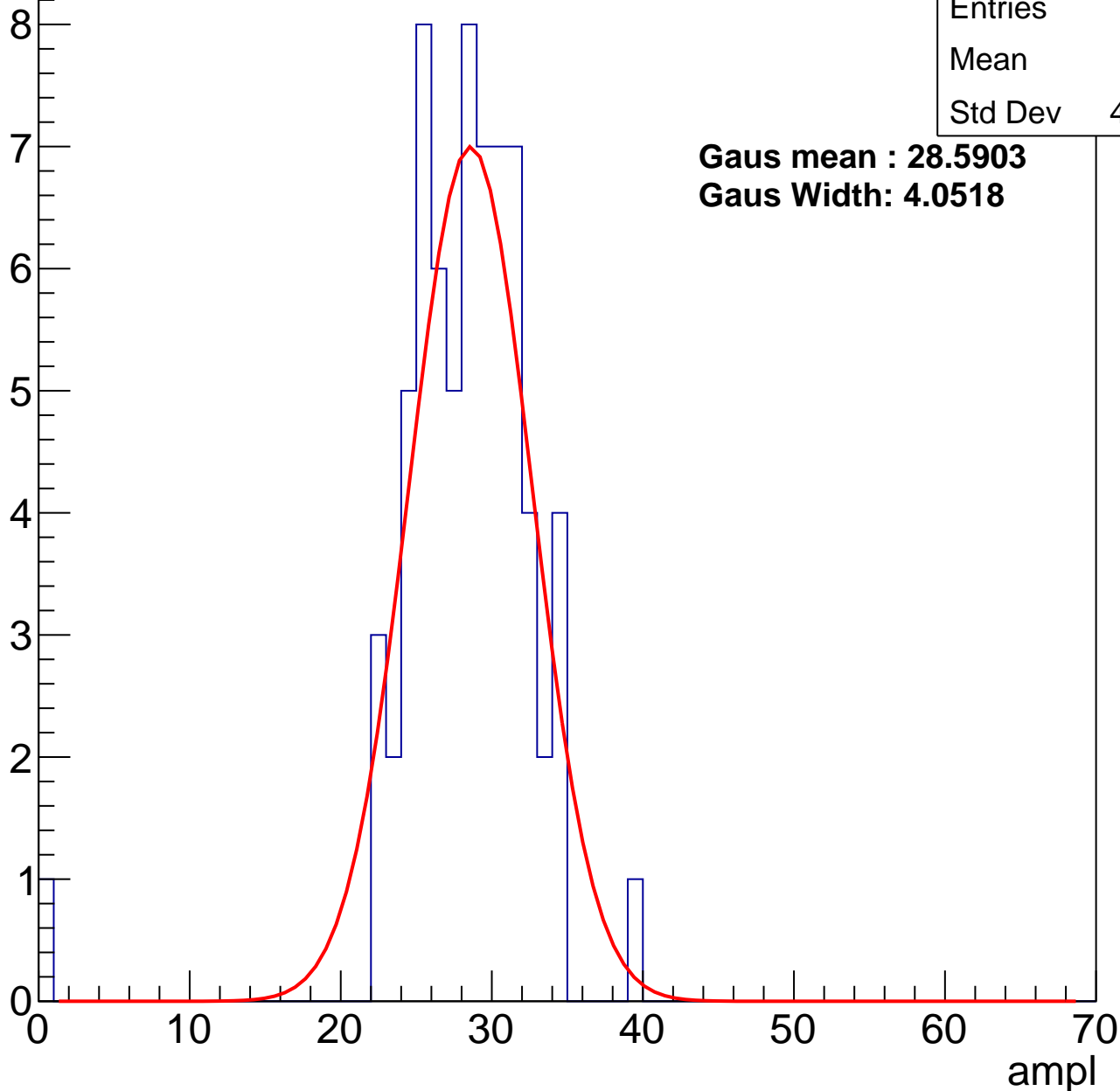
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	27.8
Std Dev	4.777

**Gaus mean : 28.5903**

**Gaus Width: 4.0518**



# B1L003S, U3-ch108, adc1

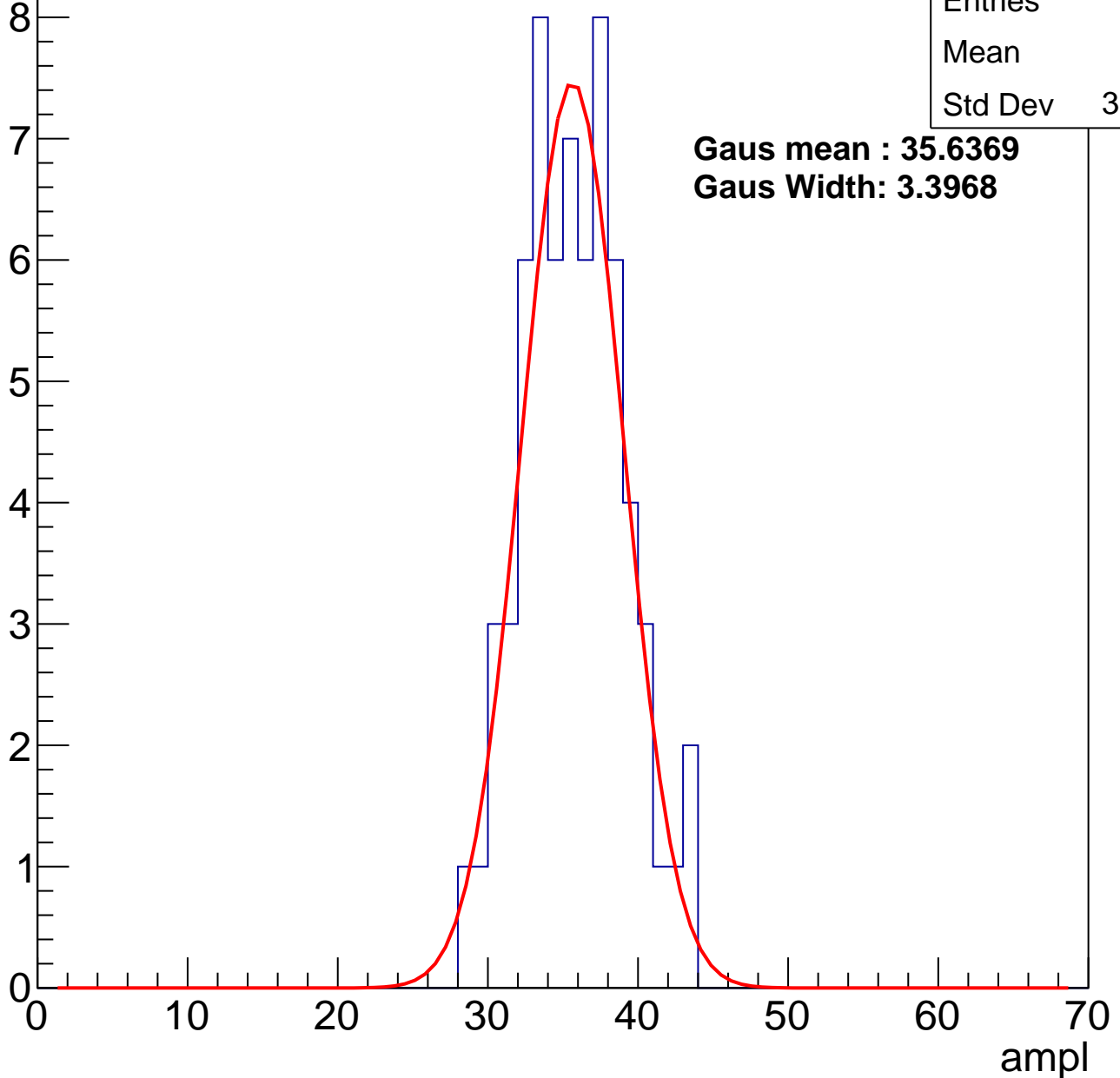
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	35.3
Std Dev	3.344

**Gaus mean : 35.6369**

**Gaus Width: 3.3968**



# B1L003S, U3-ch108, adc2

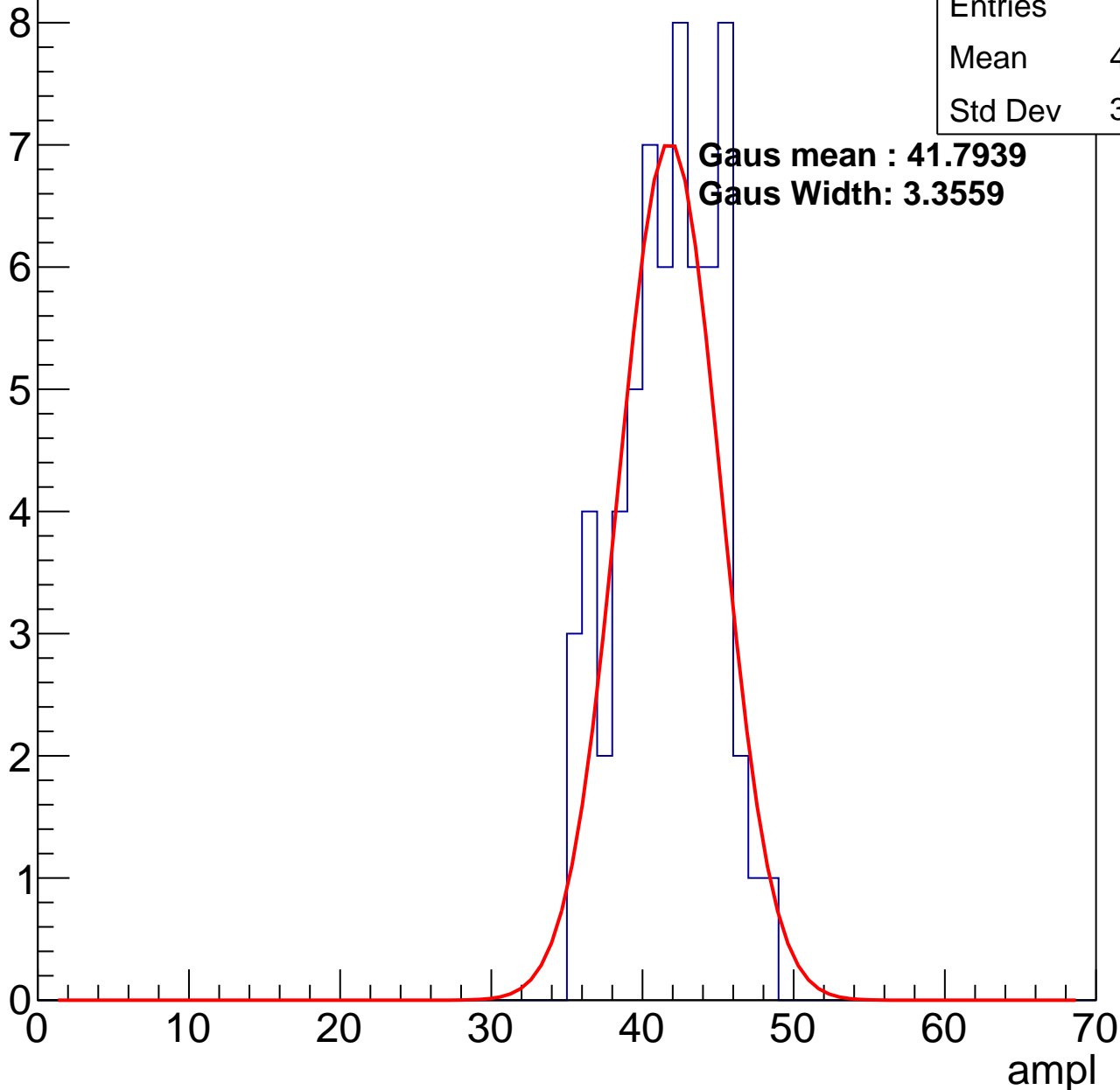
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	41.29
Std Dev	3.204

**Gaus mean : 41.7939**

**Gaus Width: 3.3559**

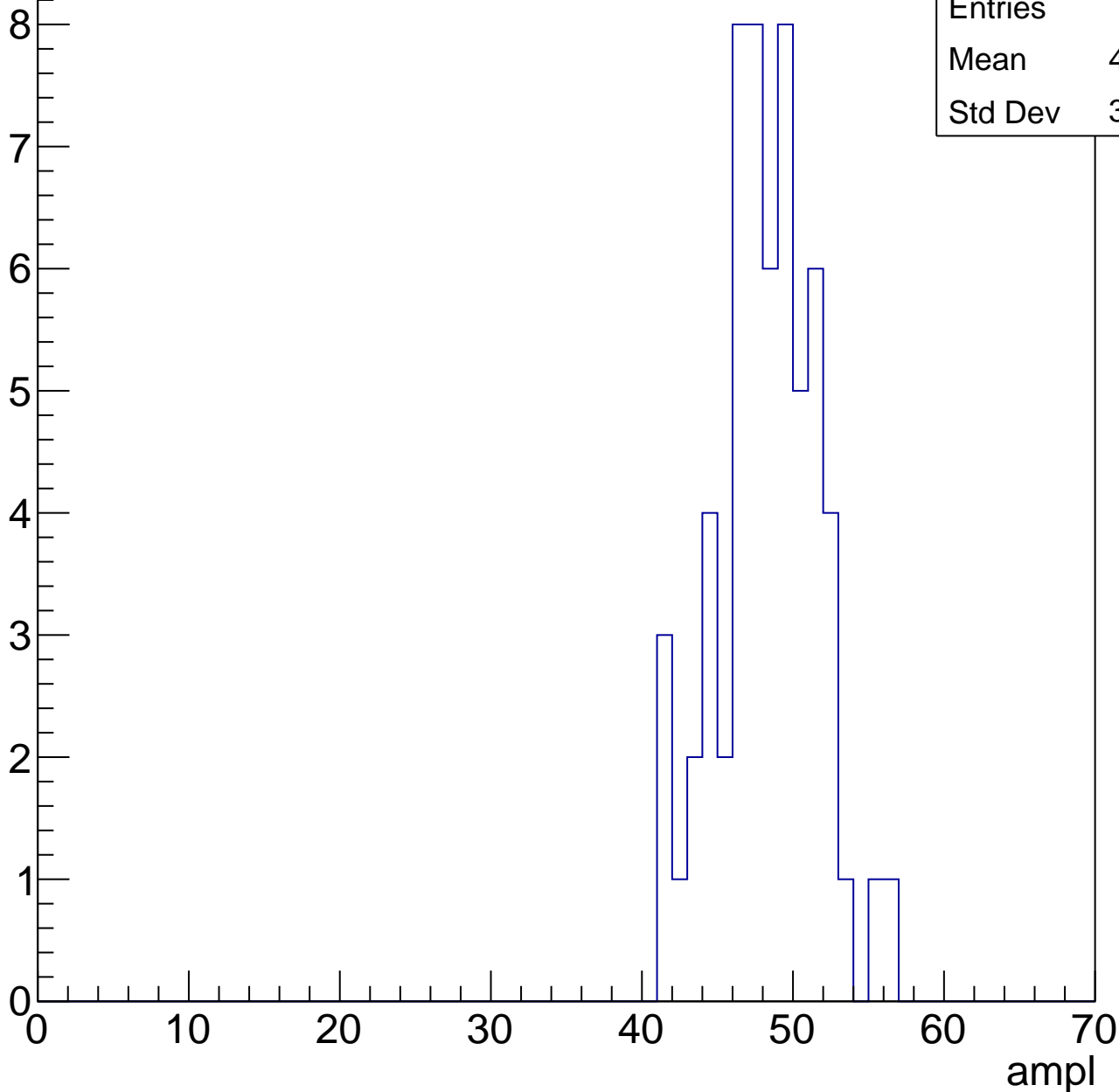


# B1L003S, U3-ch108, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	47.82
Std Dev	3.258

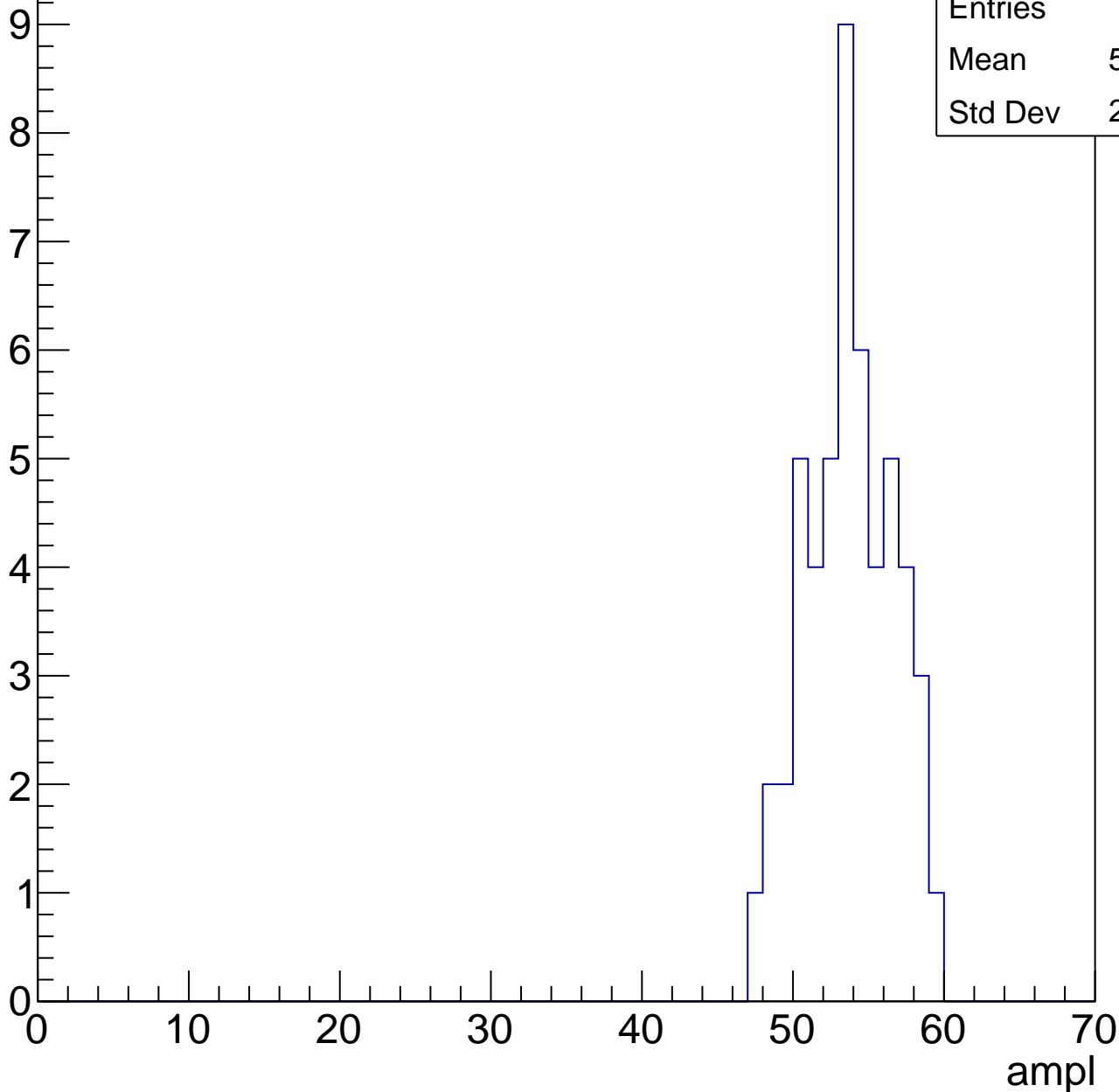


# B1L003S, U3-ch108, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	51
Mean	53.27
Std Dev	2.877

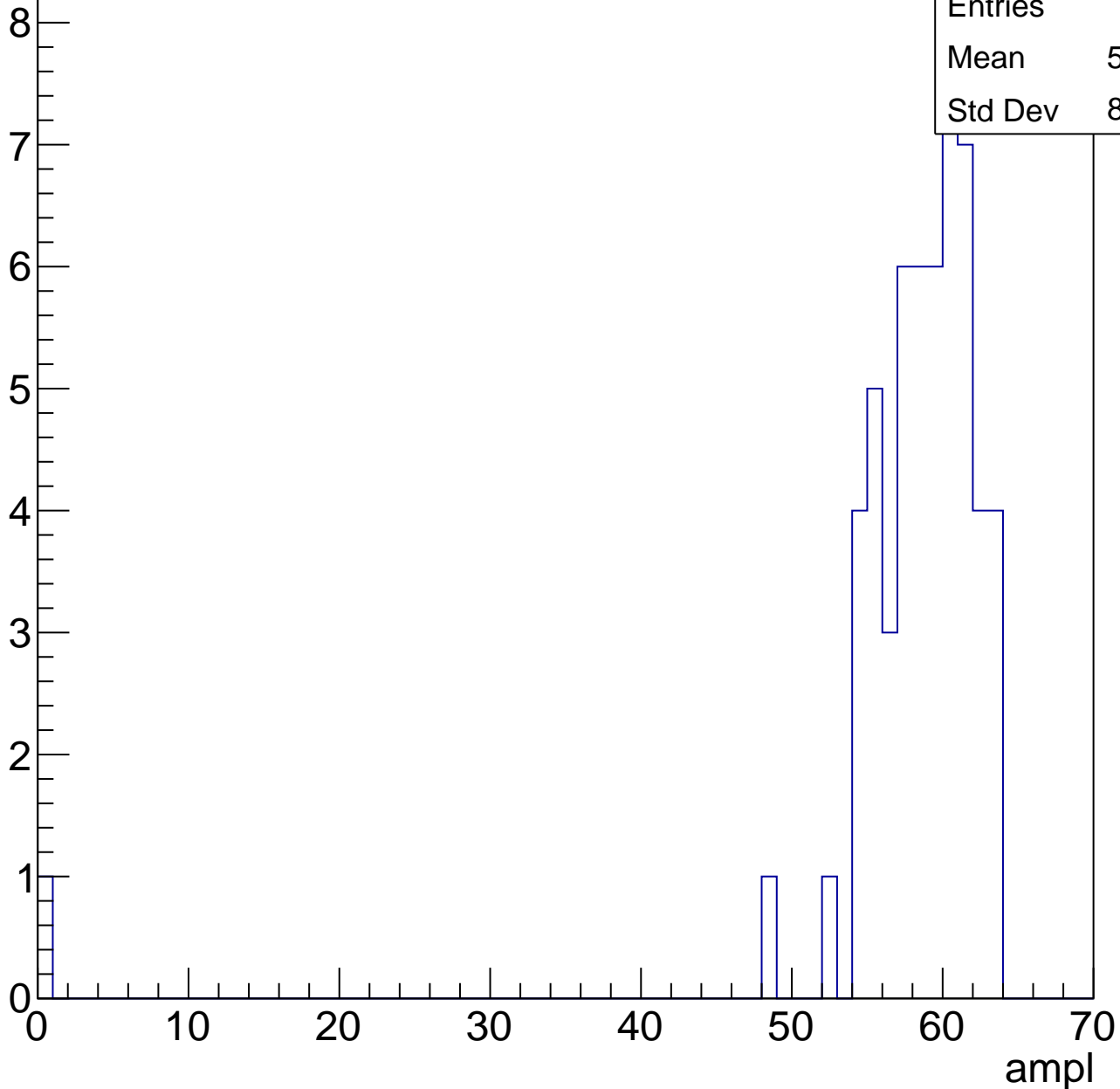


# B1L003S, U3-ch108, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

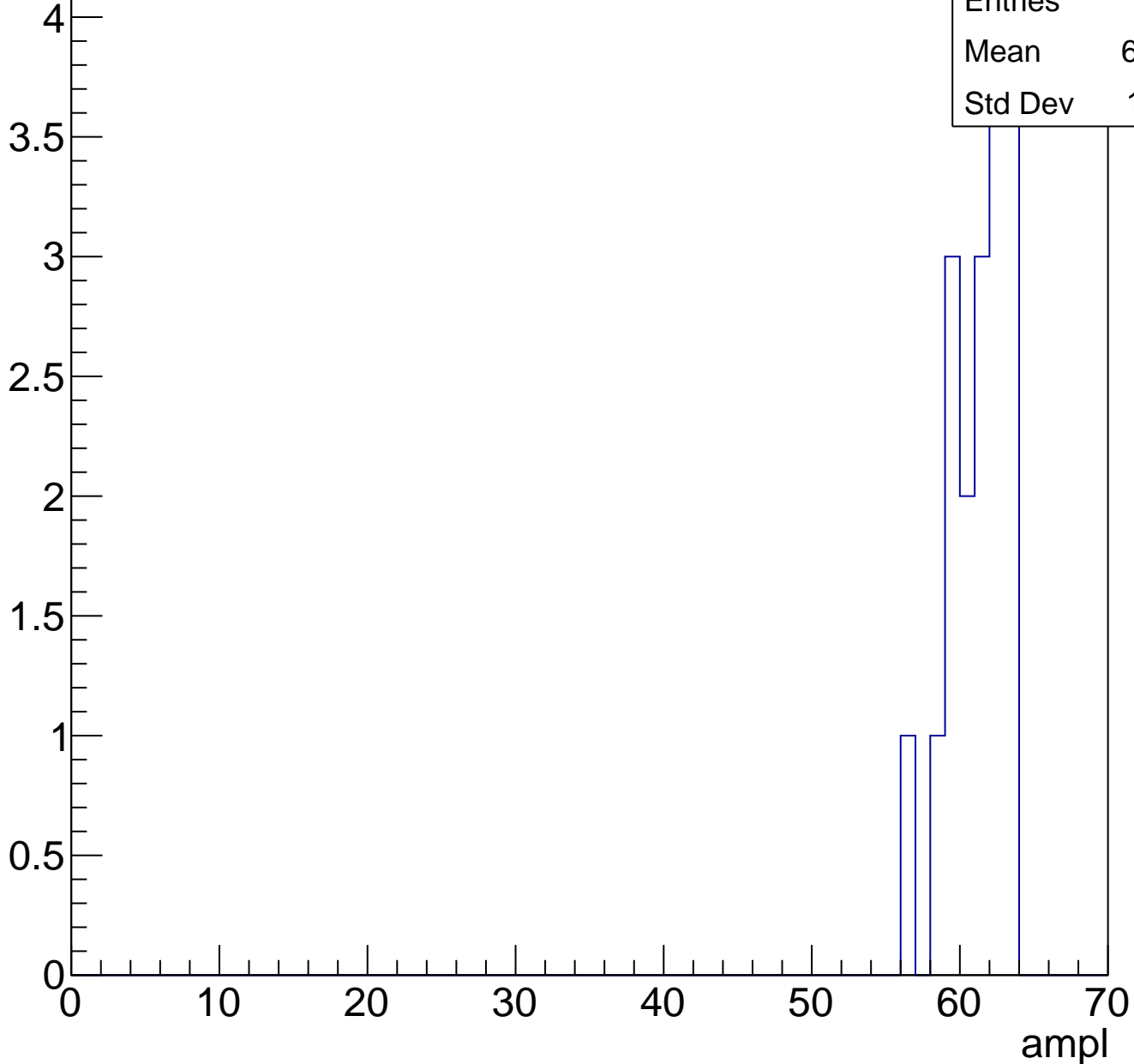
Entries	56
Mean	57.32
Std Dev	8.309



# B1L003S, U3-ch108, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

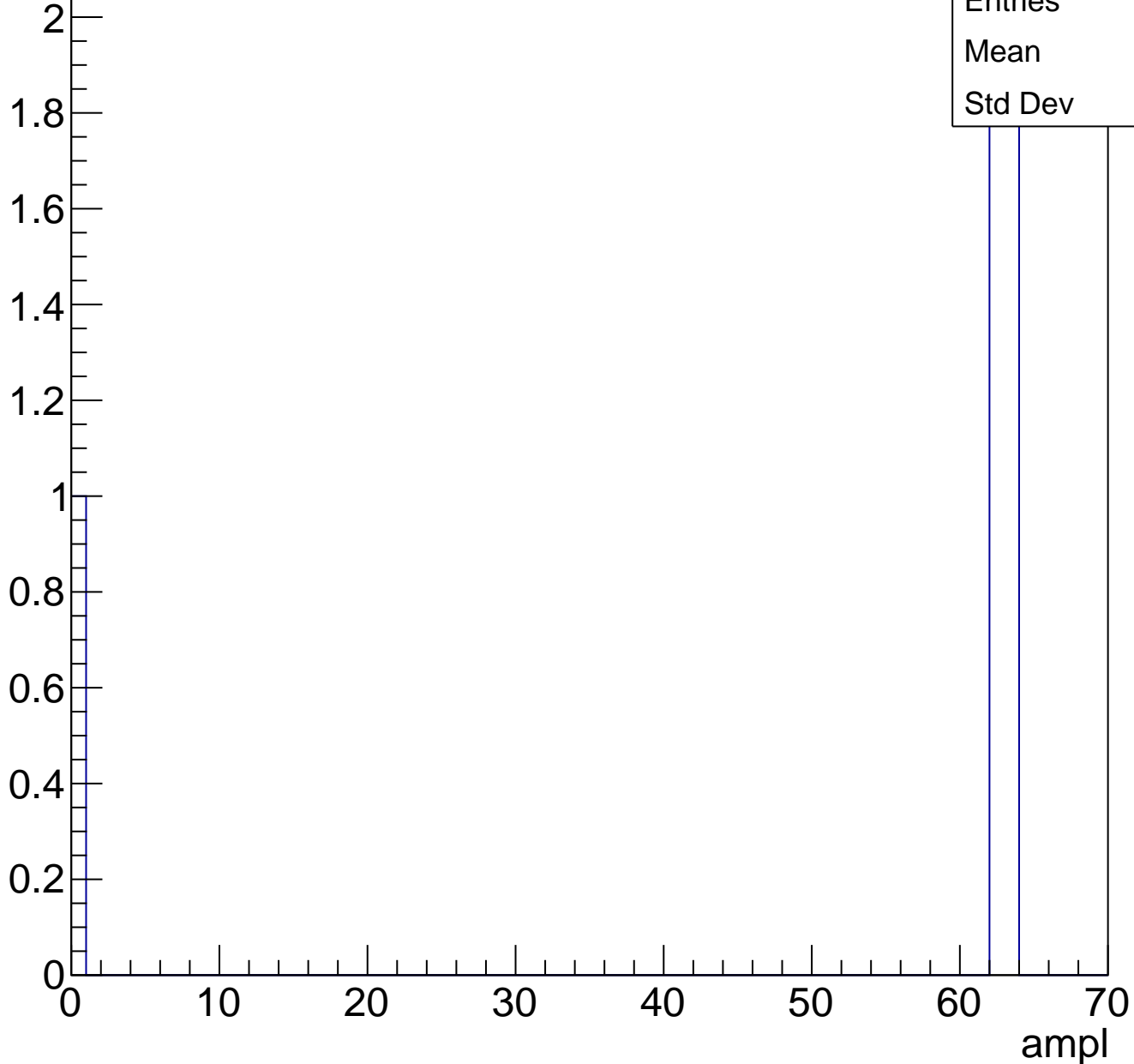




# B1L003S, U3-ch108, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	5
Mean	50
Std Dev	25

# B1L003S, U3-ch109, adc0

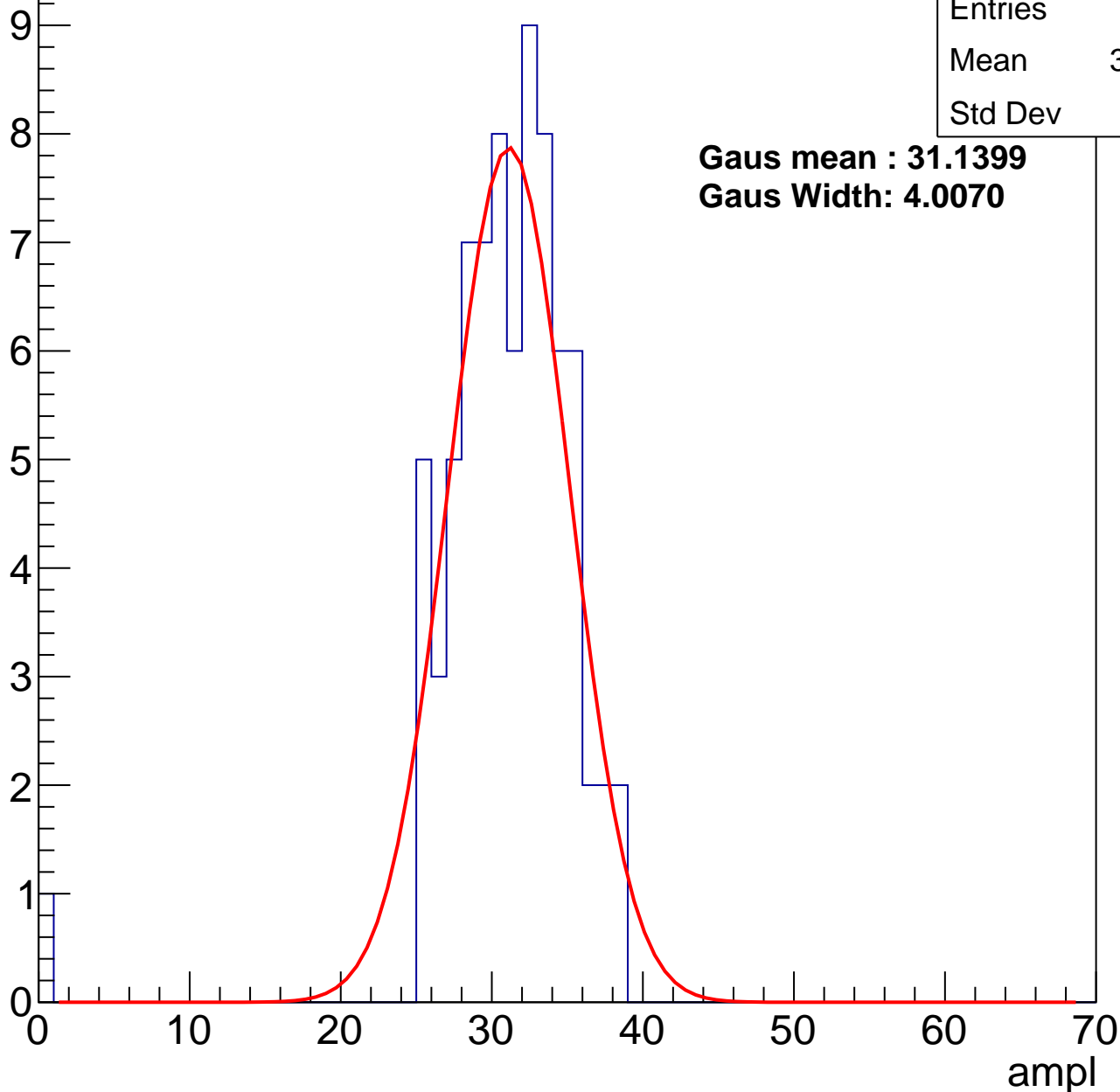
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	77
Mean	30.53
Std Dev	4.82

**Gaus mean : 31.1399**

**Gaus Width: 4.0070**



# B1L003S, U3-ch109, adc1

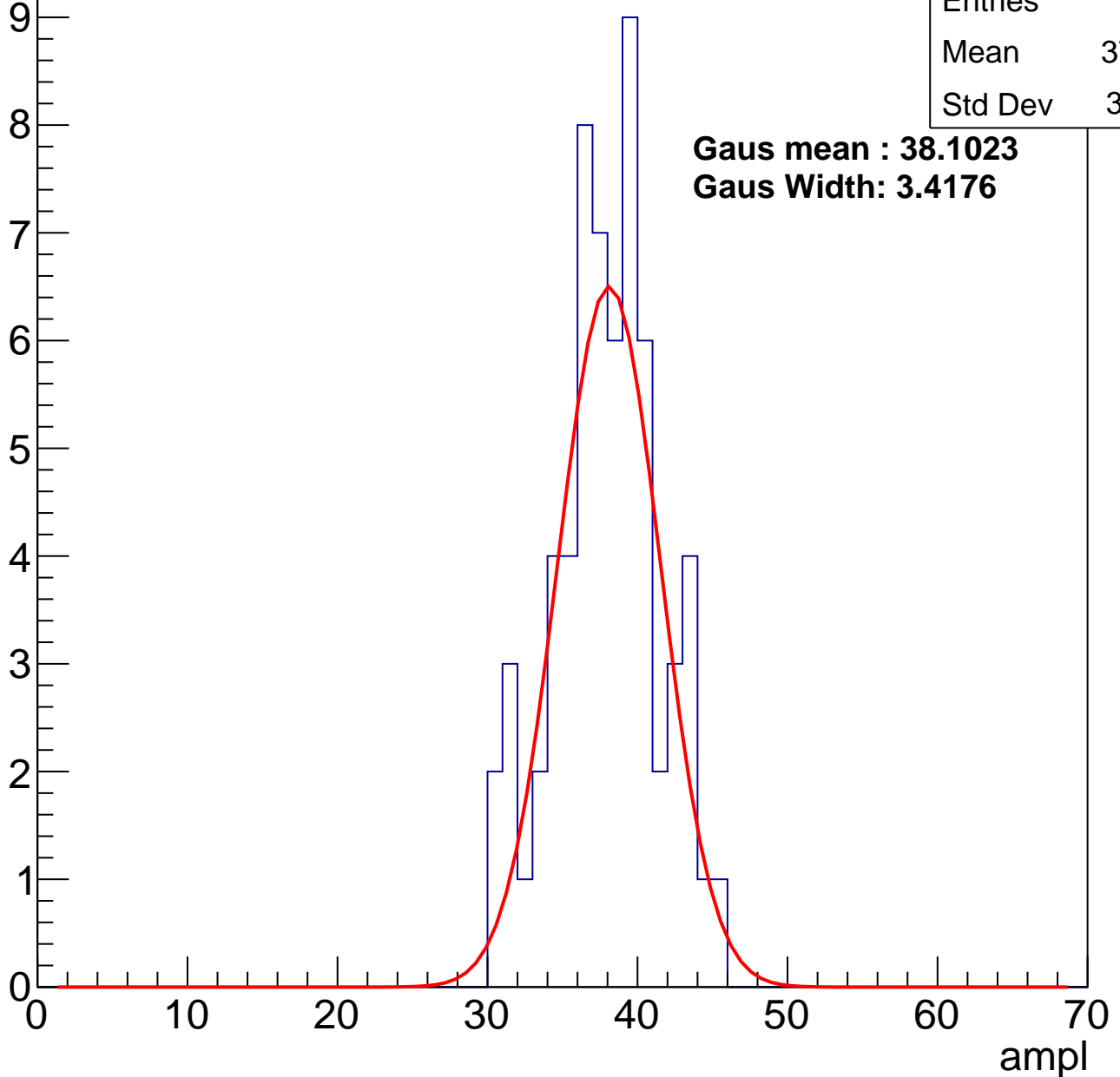
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	37.49
Std Dev	3.491

**Gaus mean : 38.1023**

**Gaus Width: 3.4176**



# B1L003S, U3-ch109, adc2

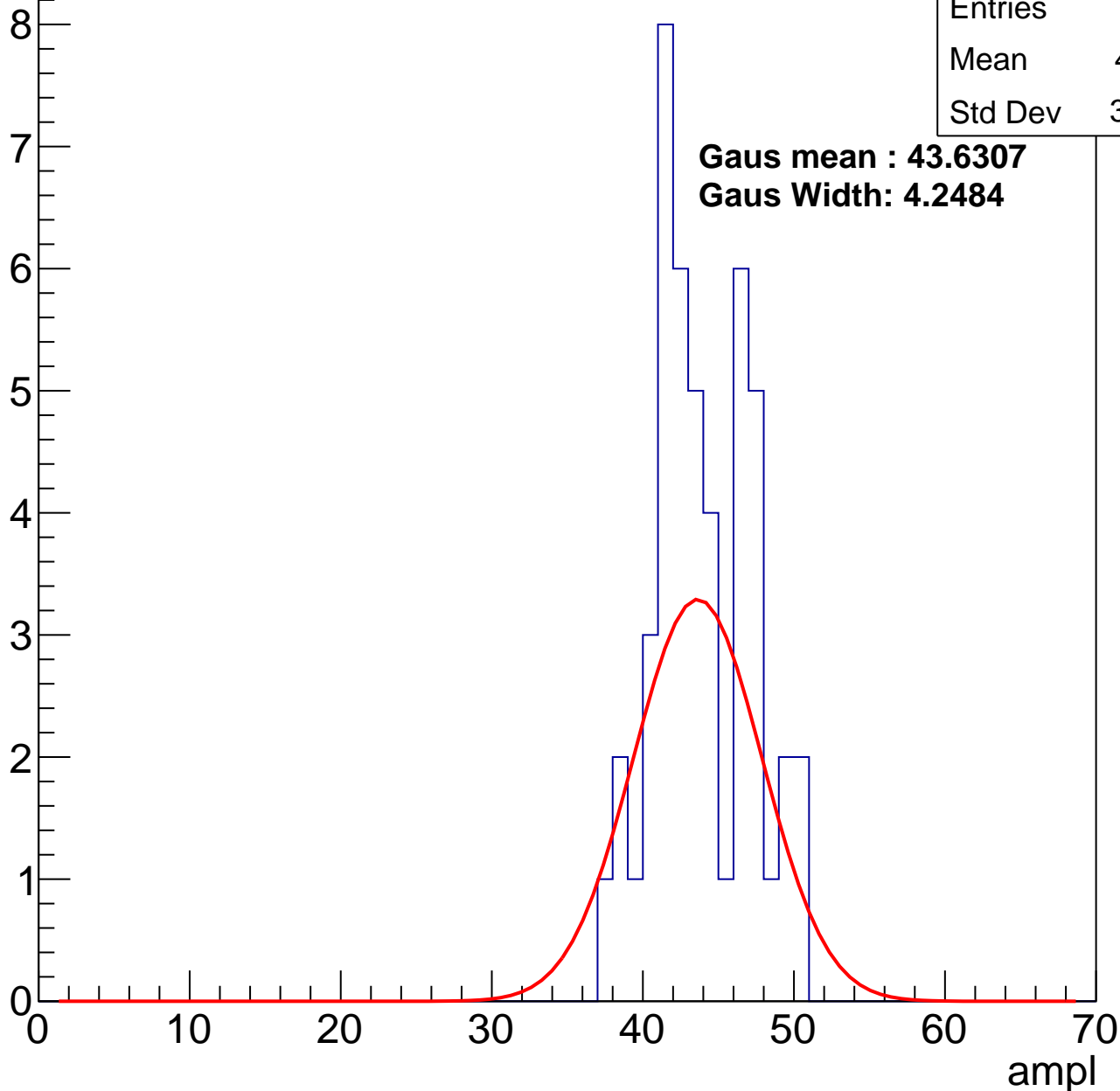
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	47
Mean	43.51
Std Dev	3.235

**Gaus mean : 43.6307**

**Gaus Width: 4.2484**

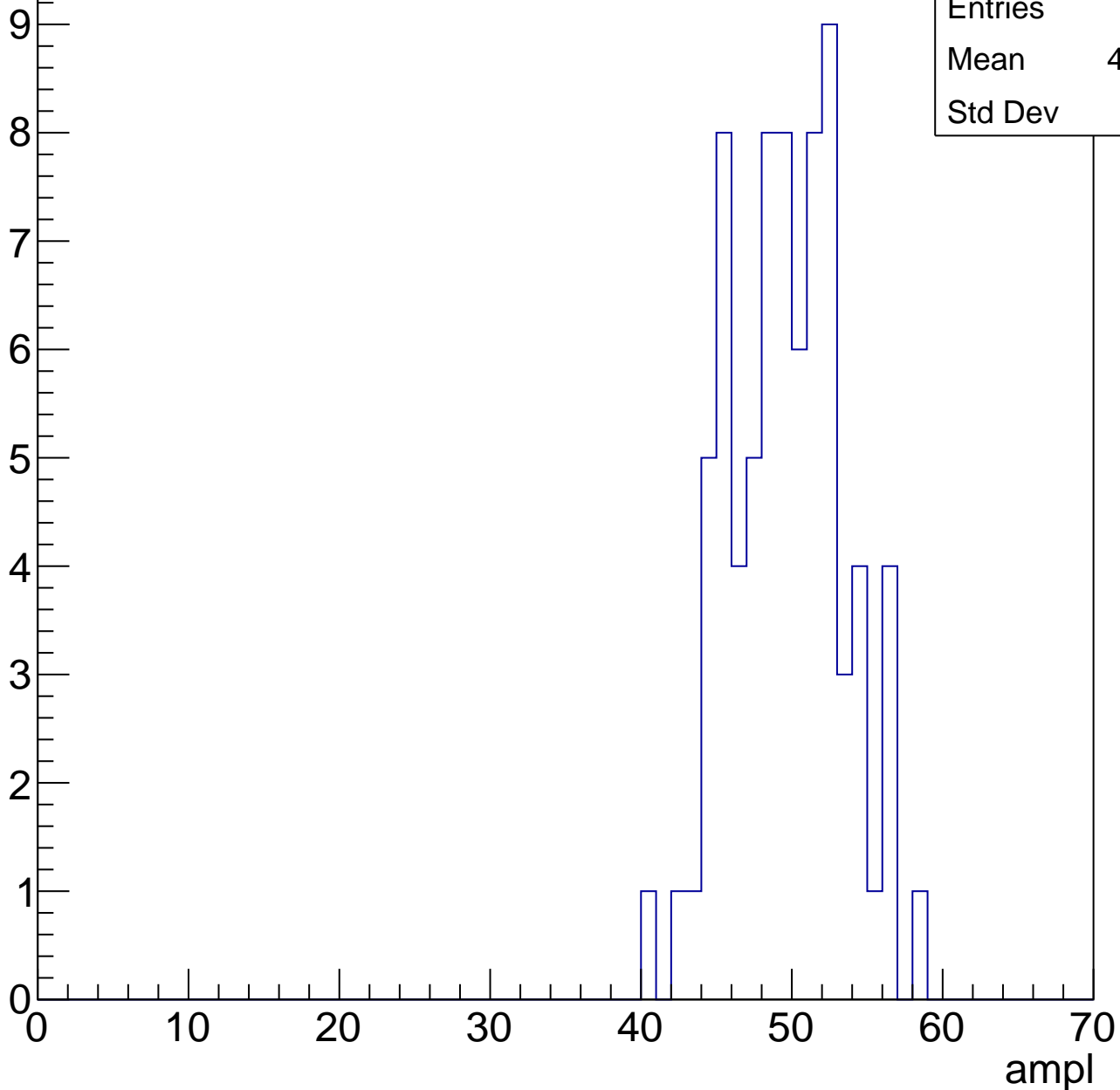


# B1L003S, U3-ch109, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	77
Mean	49.19
Std Dev	3.71

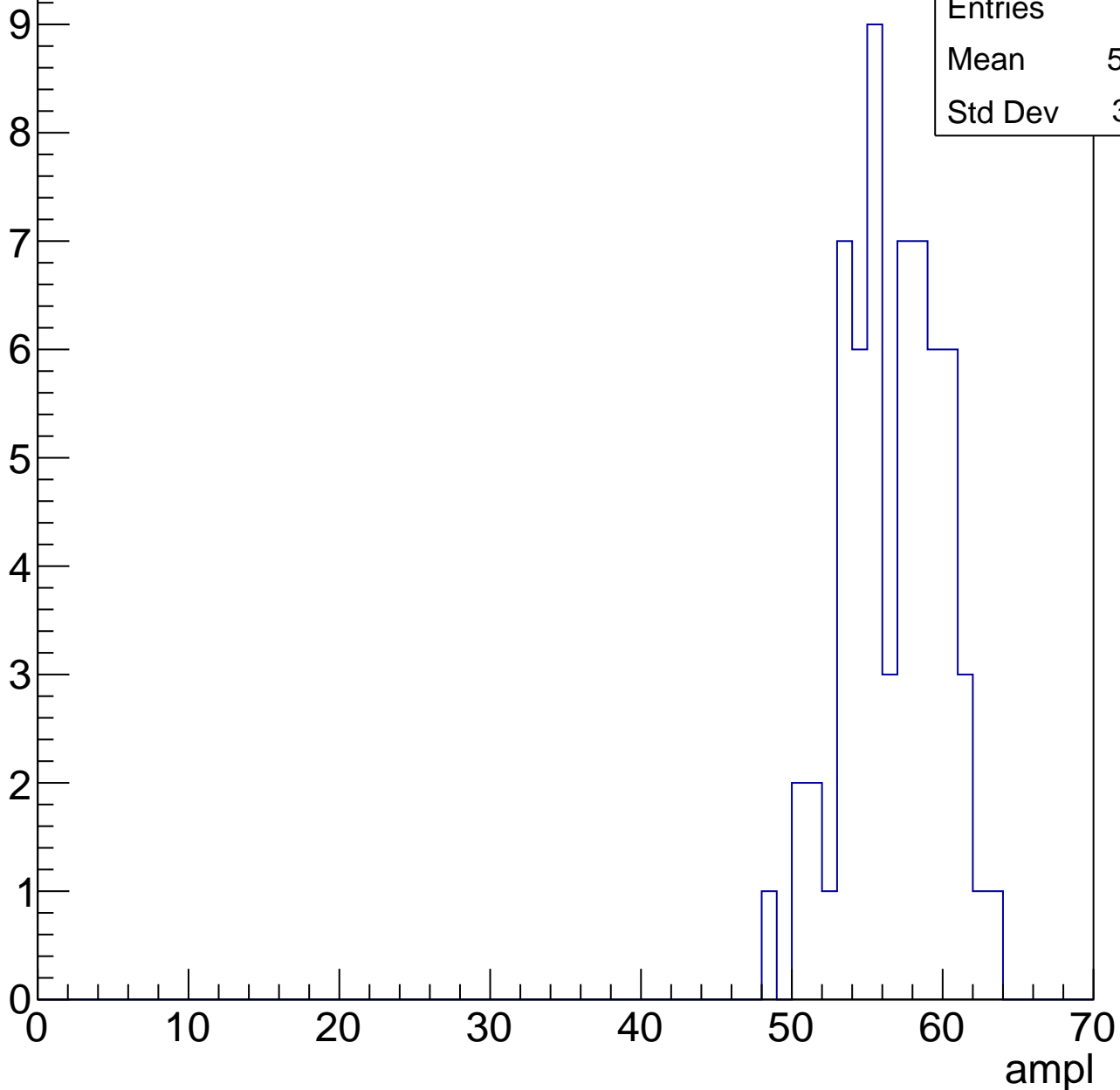


# B1L003S, U3-ch109, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	56.24
Std Dev	3.211

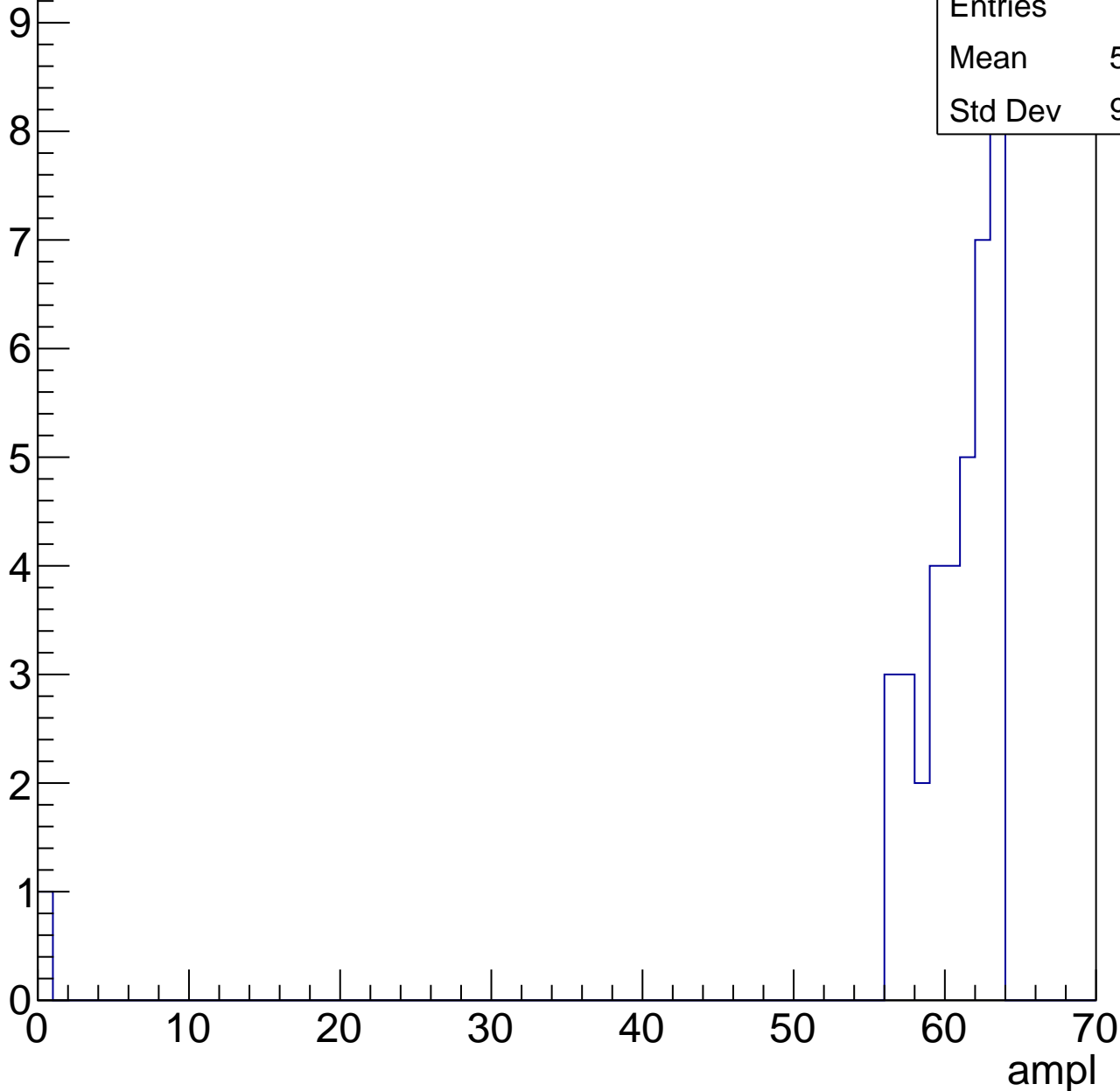


# B1L003S, U3-ch109, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

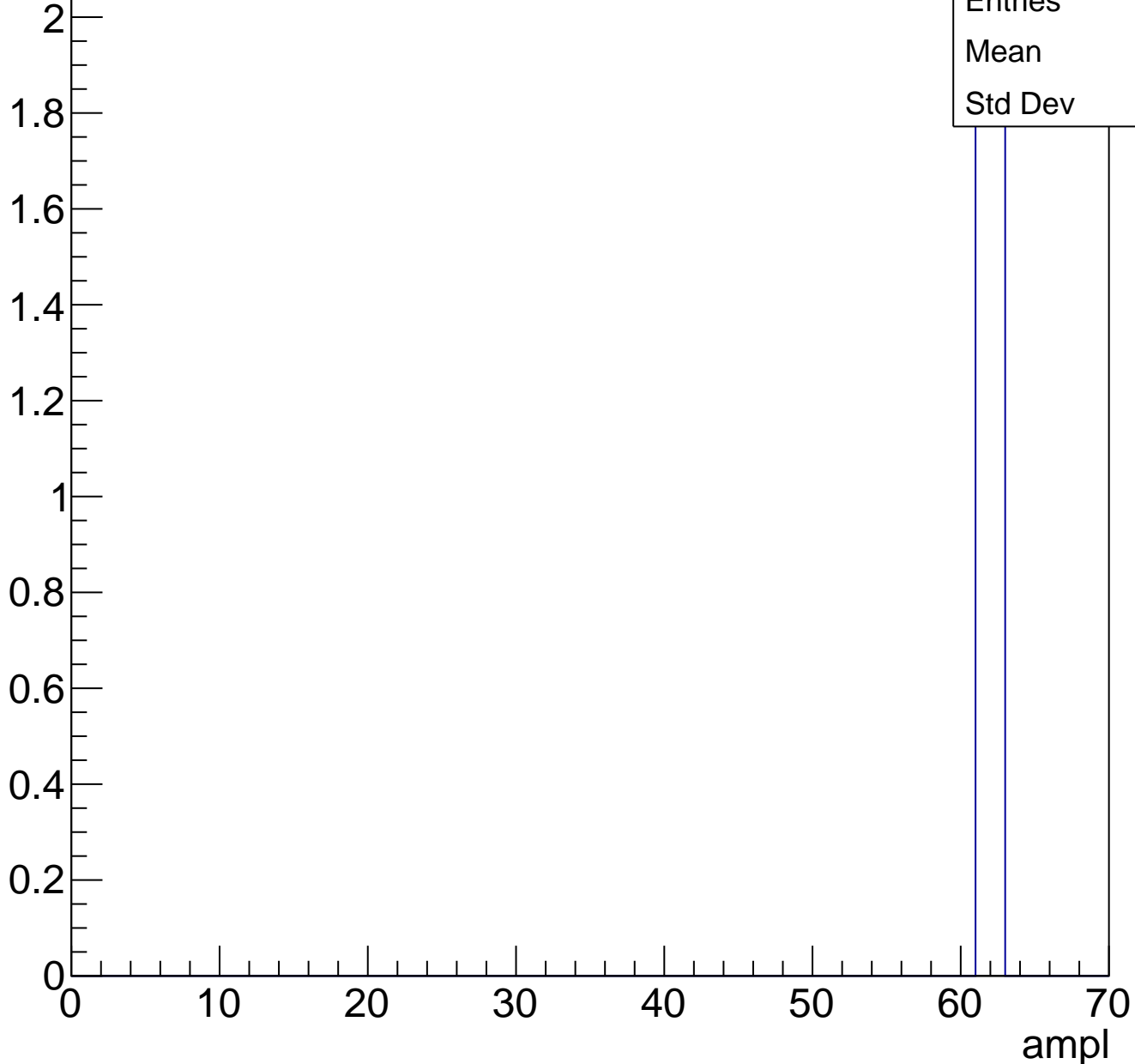
Entries	38
Mean	58.87
Std Dev	9.937



# B1L003S, U3-ch109, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch109, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U3-ch110, adc0

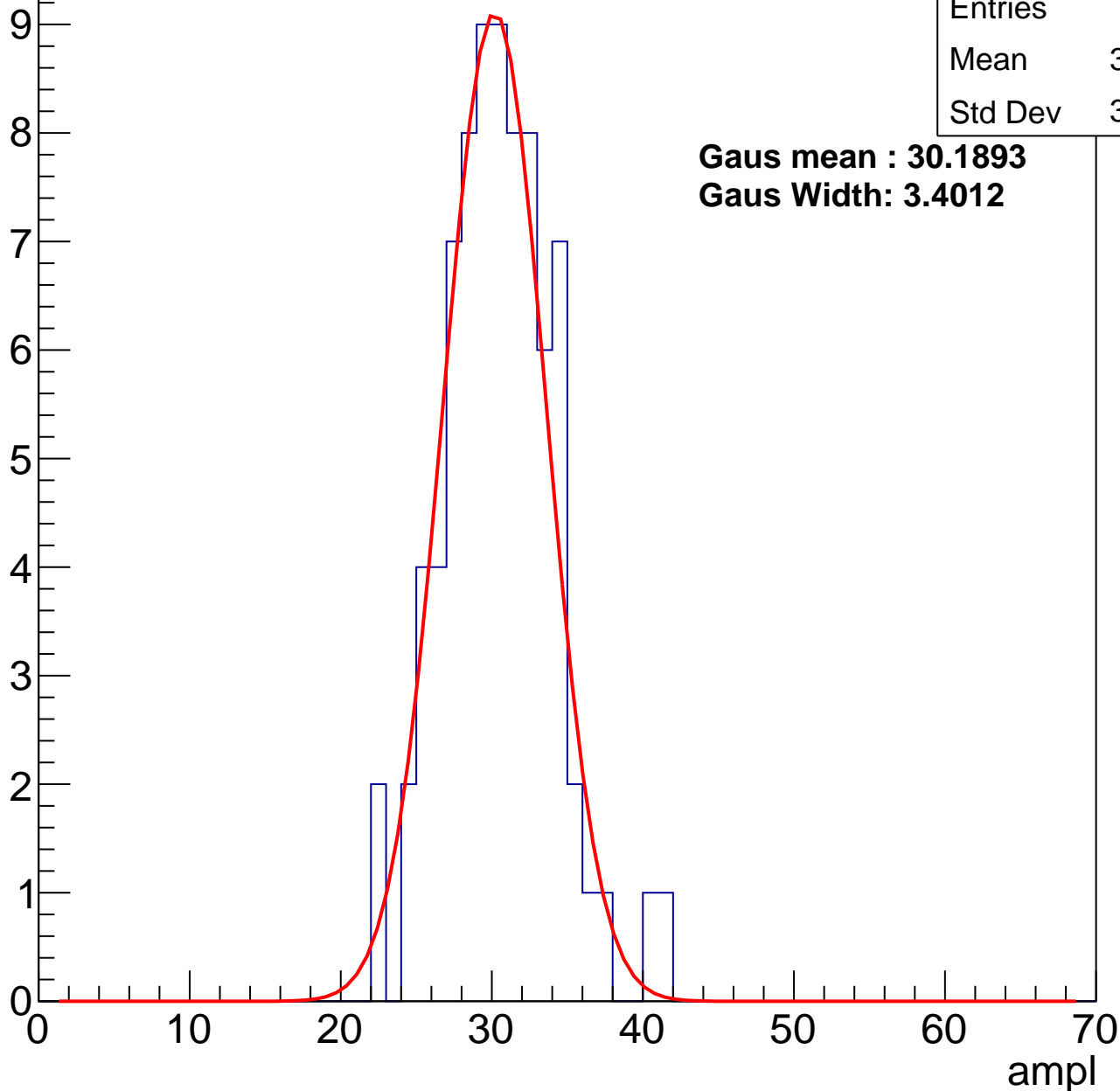
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	80
Mean	30.05
Std Dev	3.588

**Gaus mean : 30.1893**

**Gaus Width: 3.4012**



# B1L003S, U3-ch110, adc1

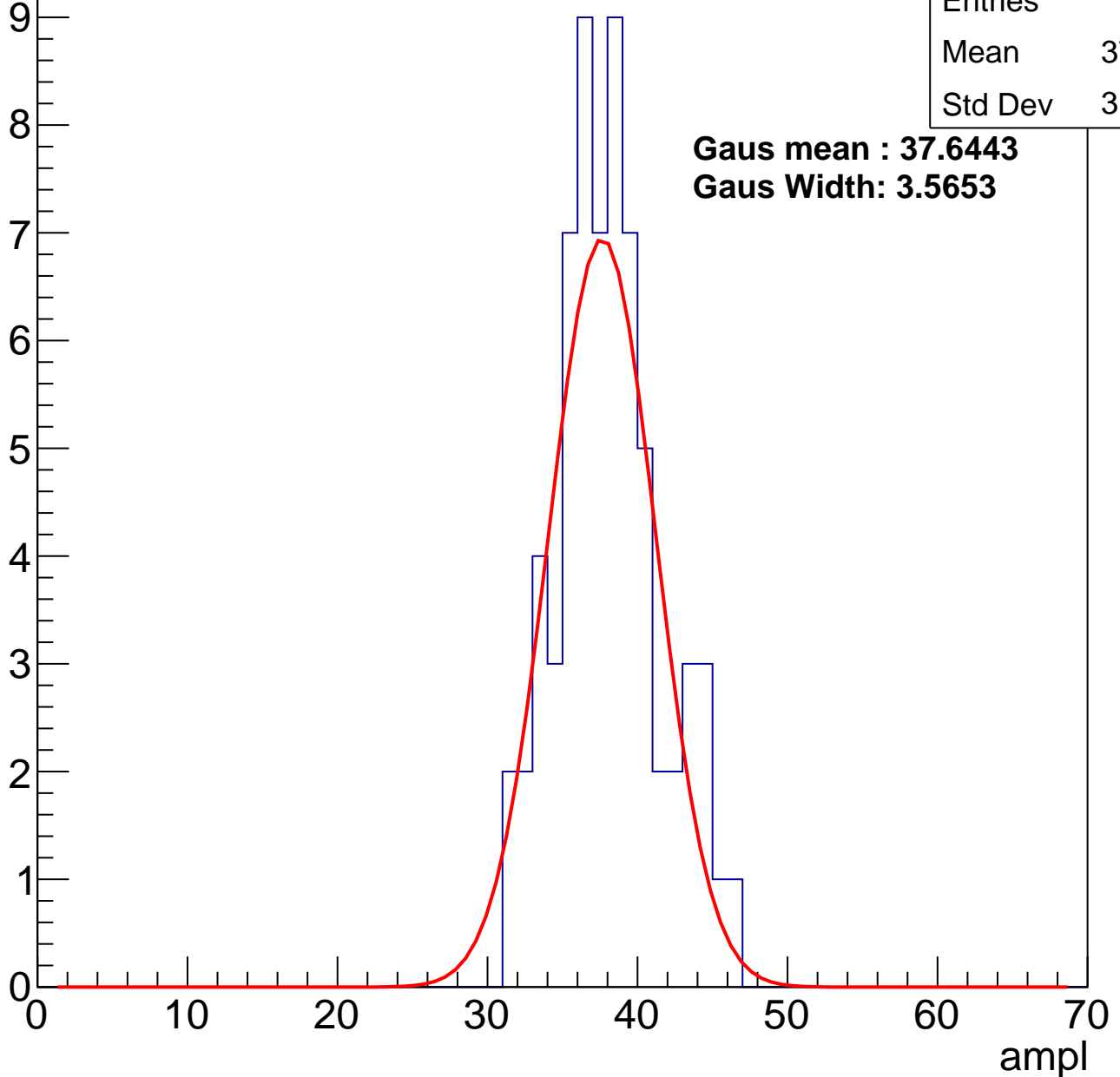
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	37.63
Std Dev	3.429

**Gaus mean : 37.6443**

**Gaus Width: 3.5653**



# B1L003S, U3-ch110, adc2

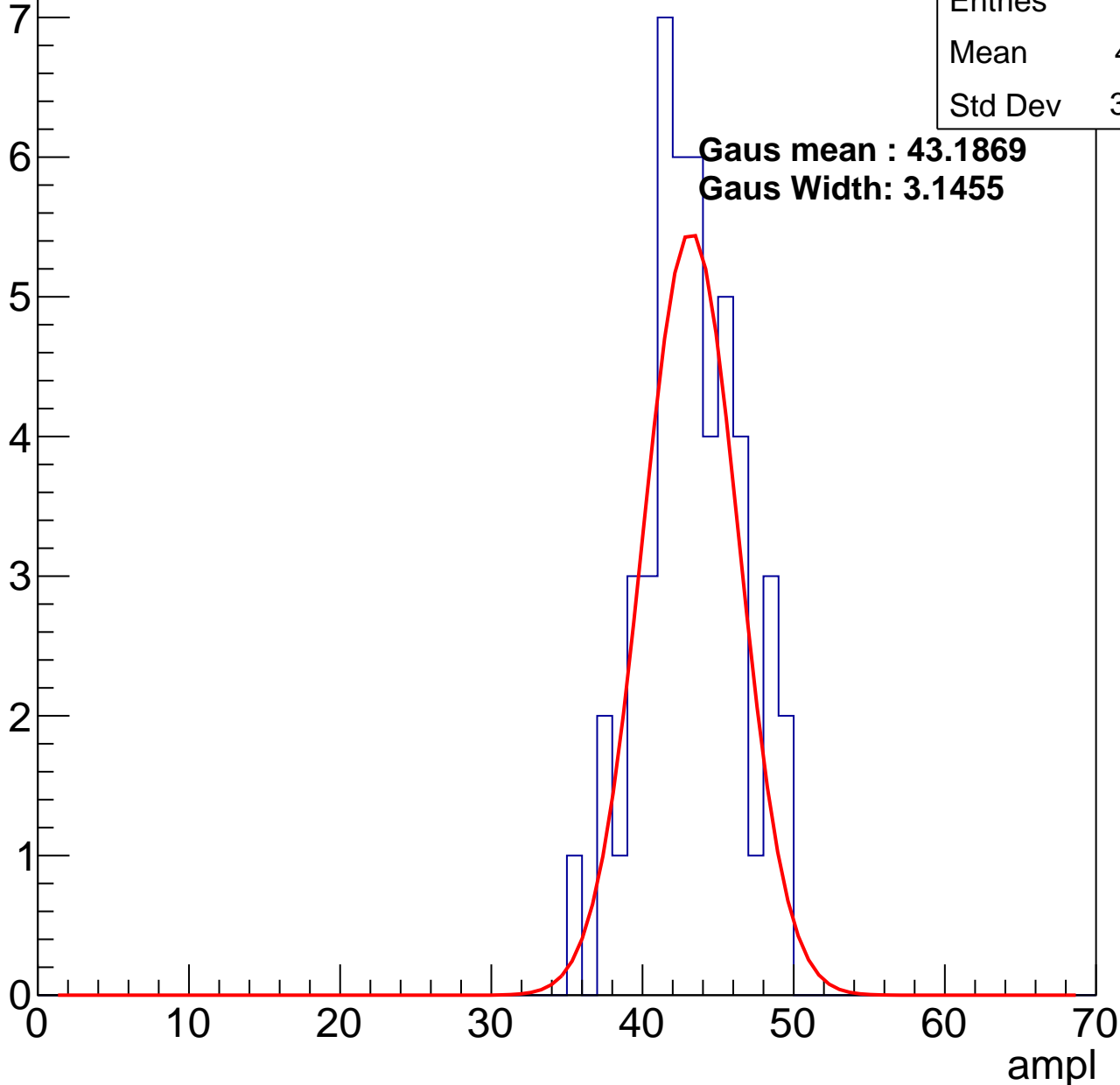
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	48
Mean	42.81
Std Dev	3.199

**Gaus mean : 43.1869**

**Gaus Width: 3.1455**

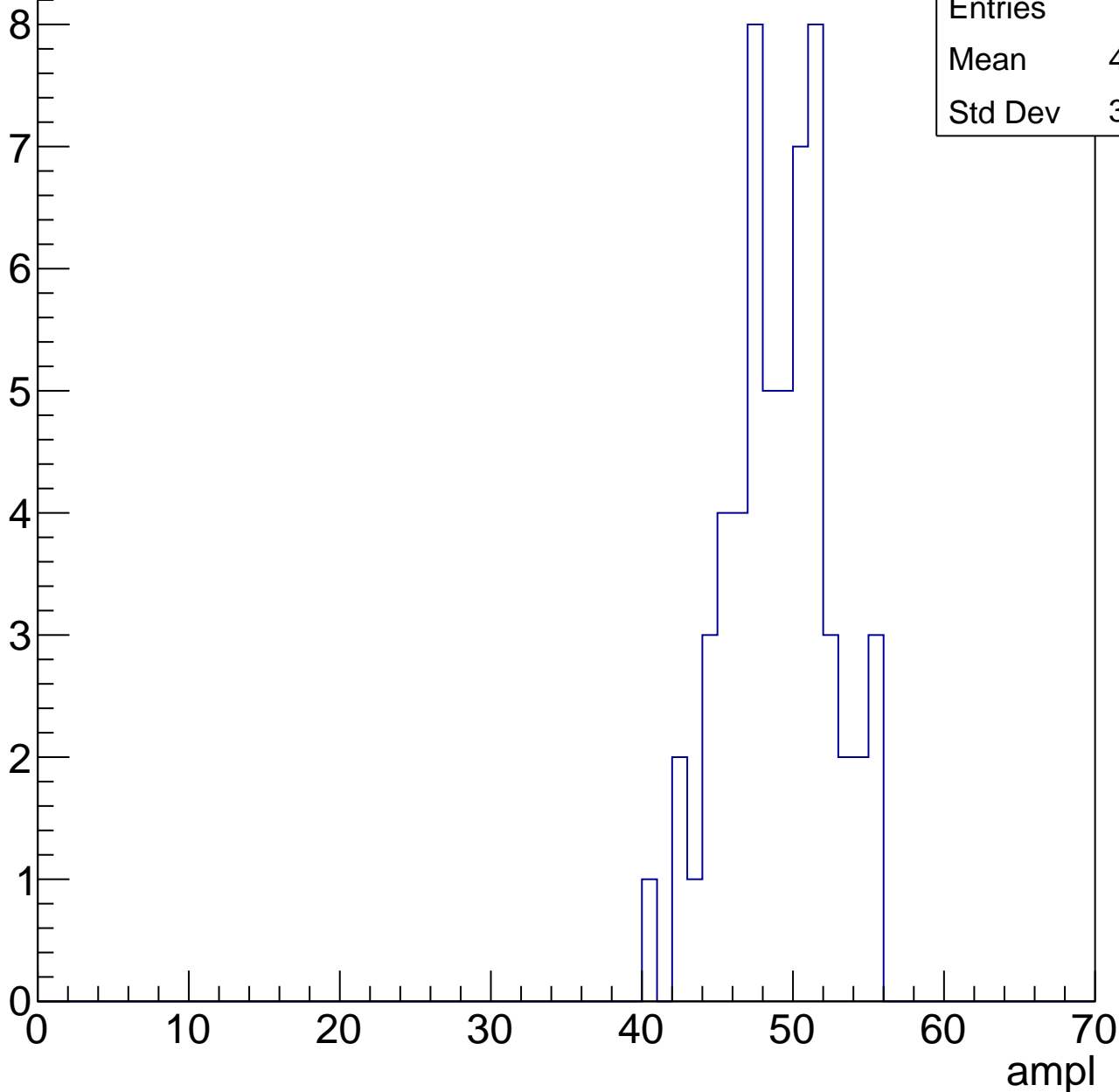


# B1L003S, U3-ch110, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	48.57
Std Dev	3.404

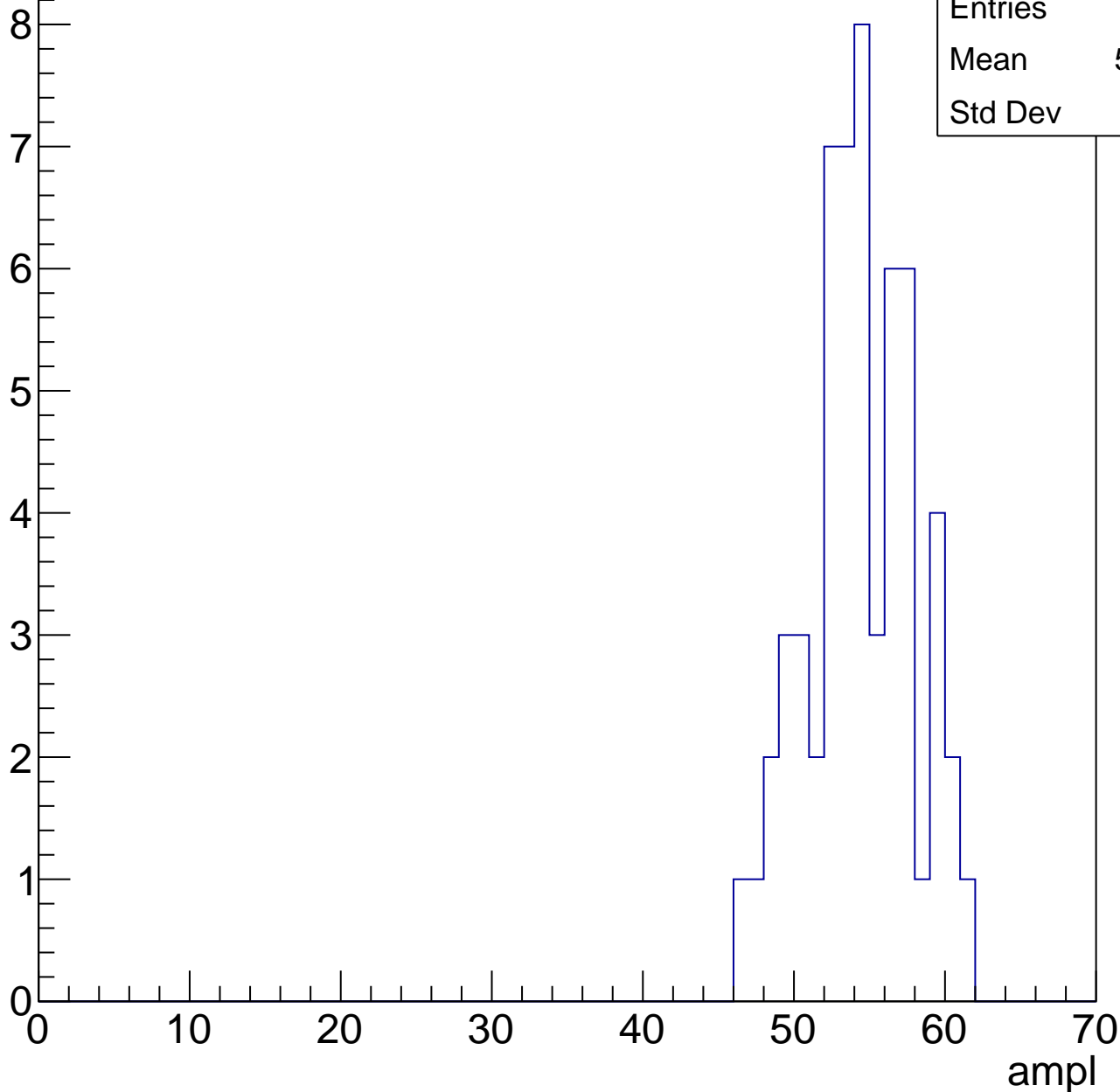


# B1L003S, U3-ch110, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	53.91
Std Dev	3.45

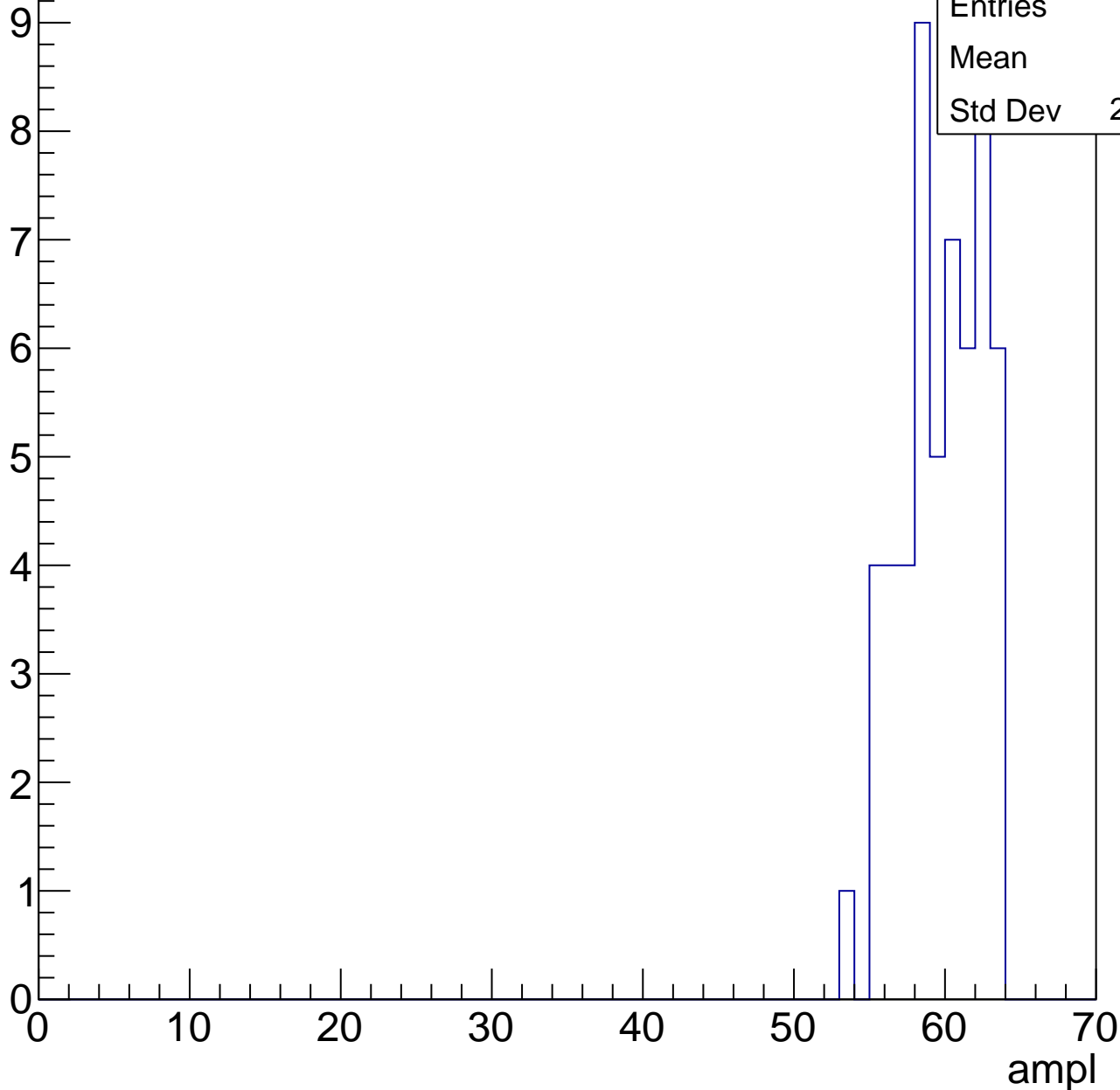


# B1L003S, U3-ch110, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

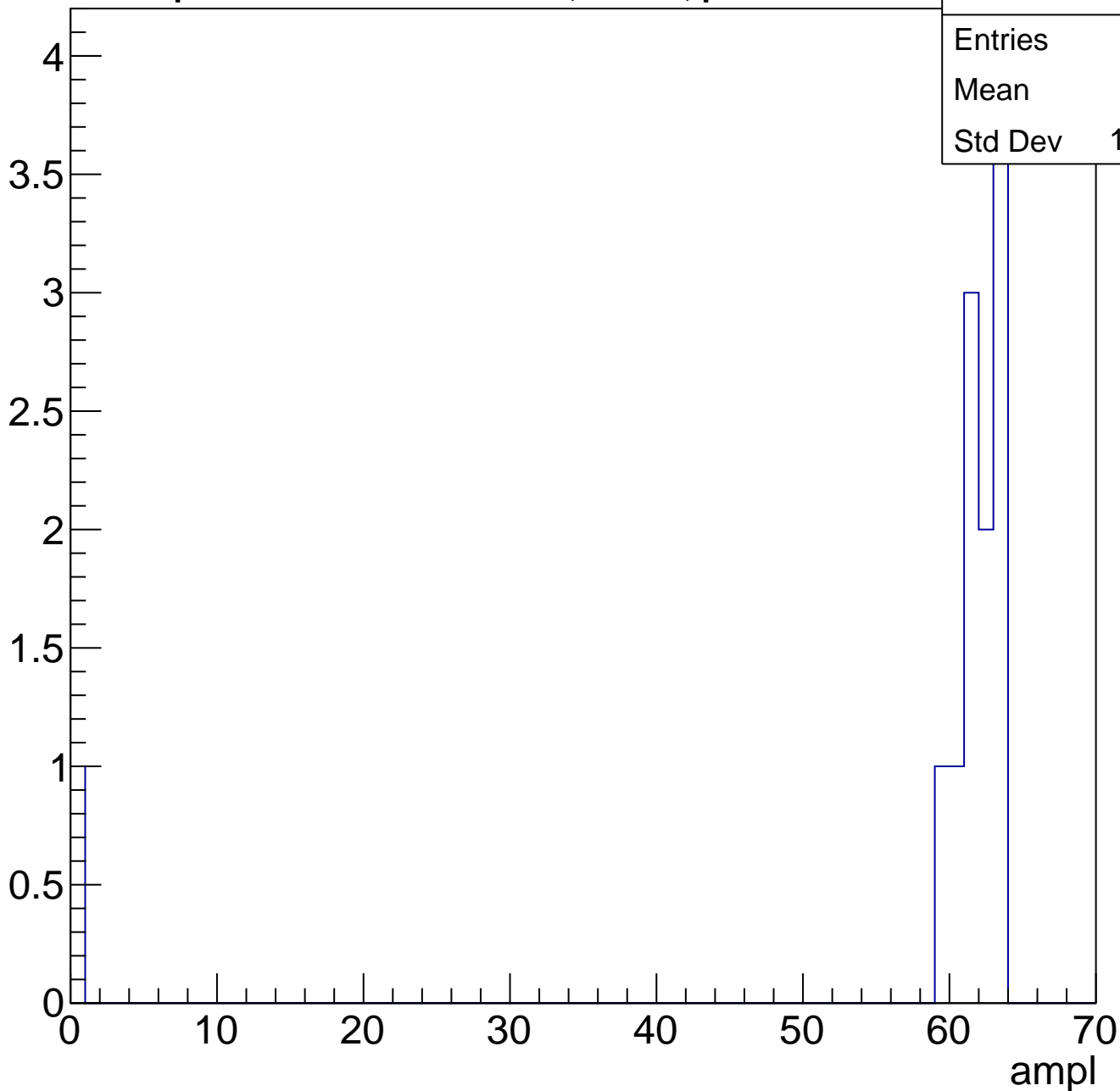
Entries	54
Mean	59.3
Std Dev	2.565



# B1L003S, U3-ch110, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	12
Mean	56.5
Std Dev	17.08



# B1L003S, U3-ch110, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U3-ch111, adc0

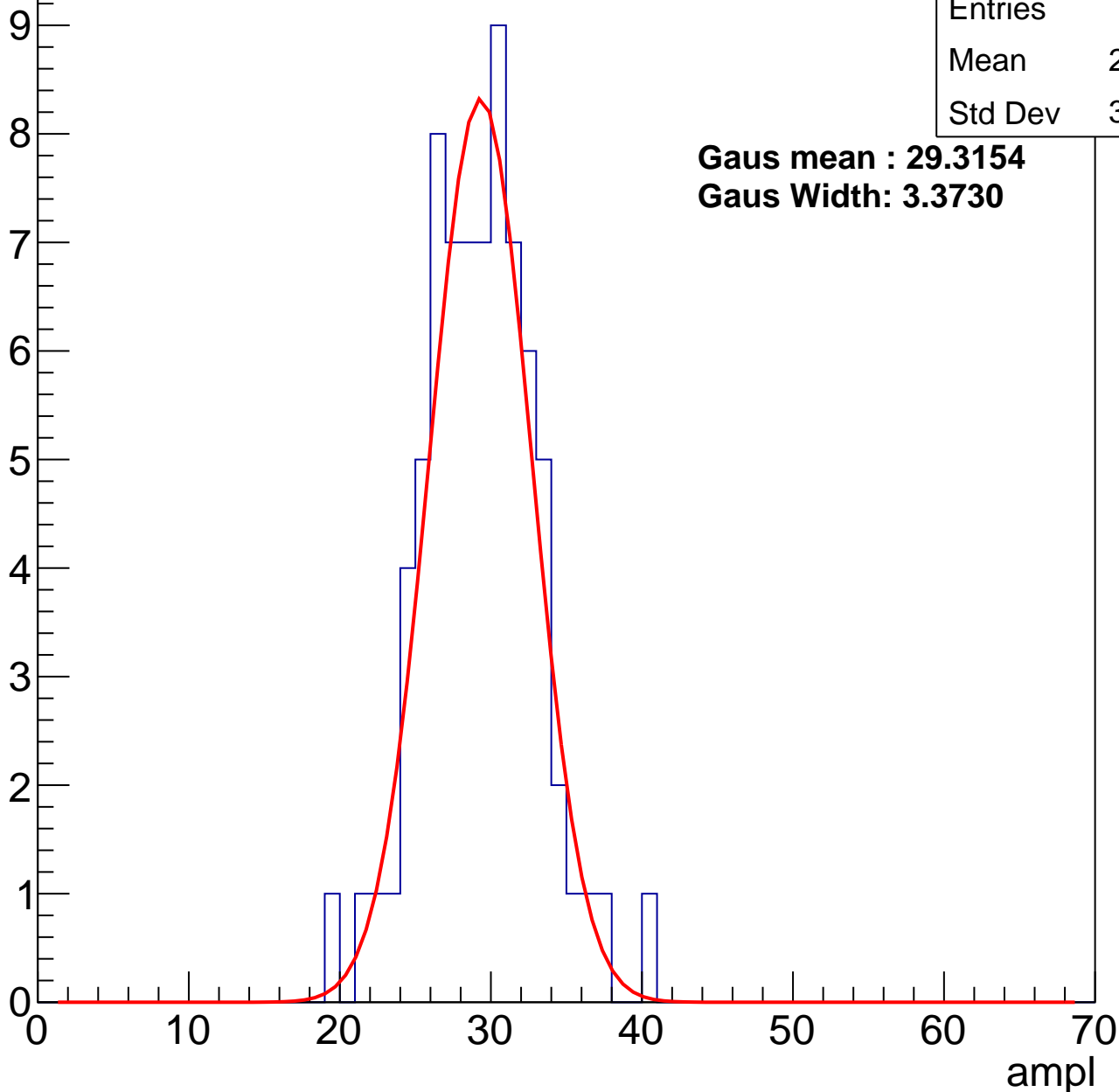
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	75
Mean	28.83
Std Dev	3.696

**Gaus mean : 29.3154**

**Gaus Width: 3.3730**



# B1L003S, U3-ch111, adc1

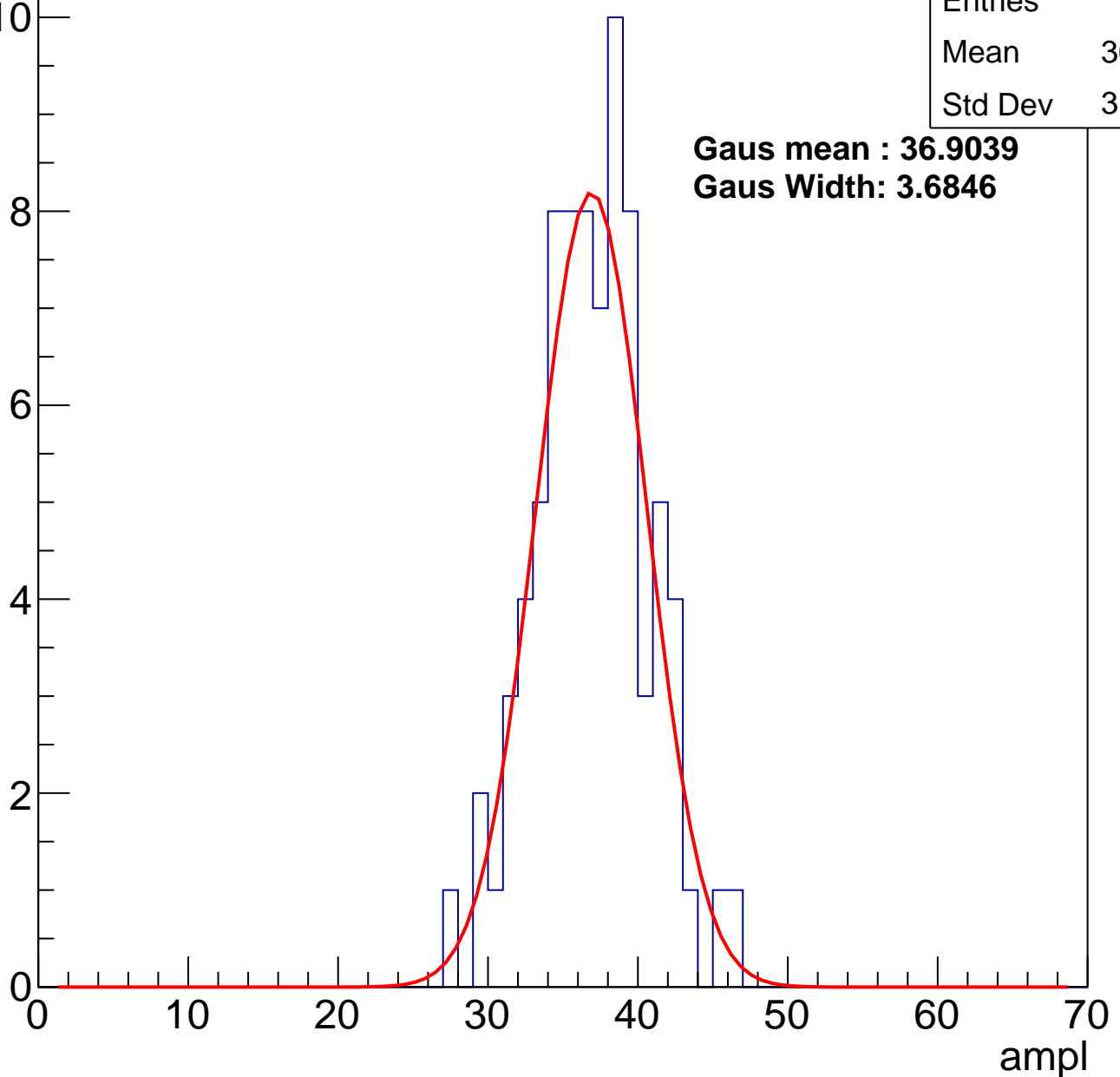
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	80
Mean	36.49
Std Dev	3.684

**Gaus mean : 36.9039**

**Gaus Width: 3.6846**



# B1L003S, U3-ch111, adc2

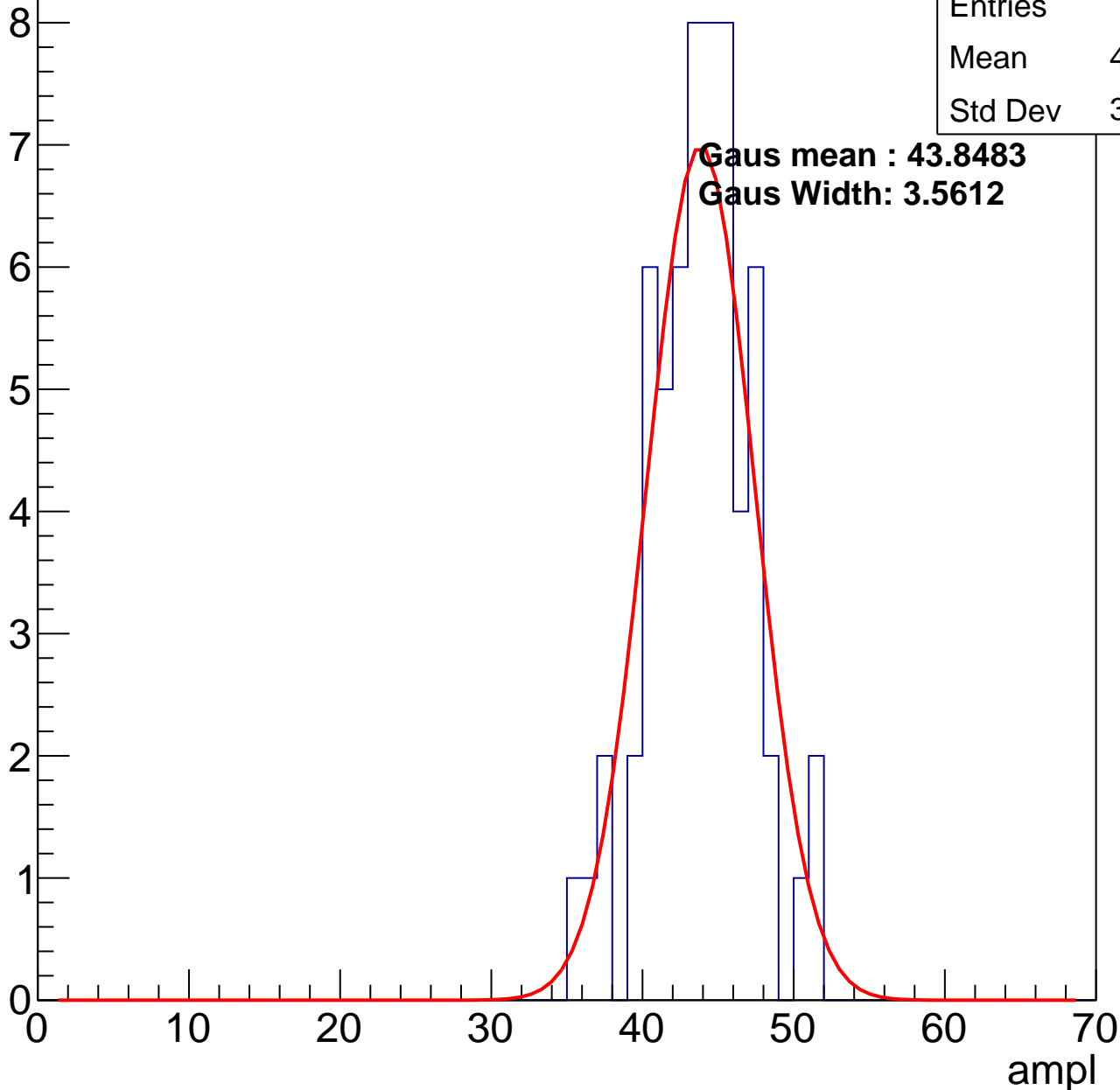
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	43.39
Std Dev	3.328

**Gaus mean : 43.8483**

**Gaus Width: 3.5612**



# B1L003S, U3-ch111, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

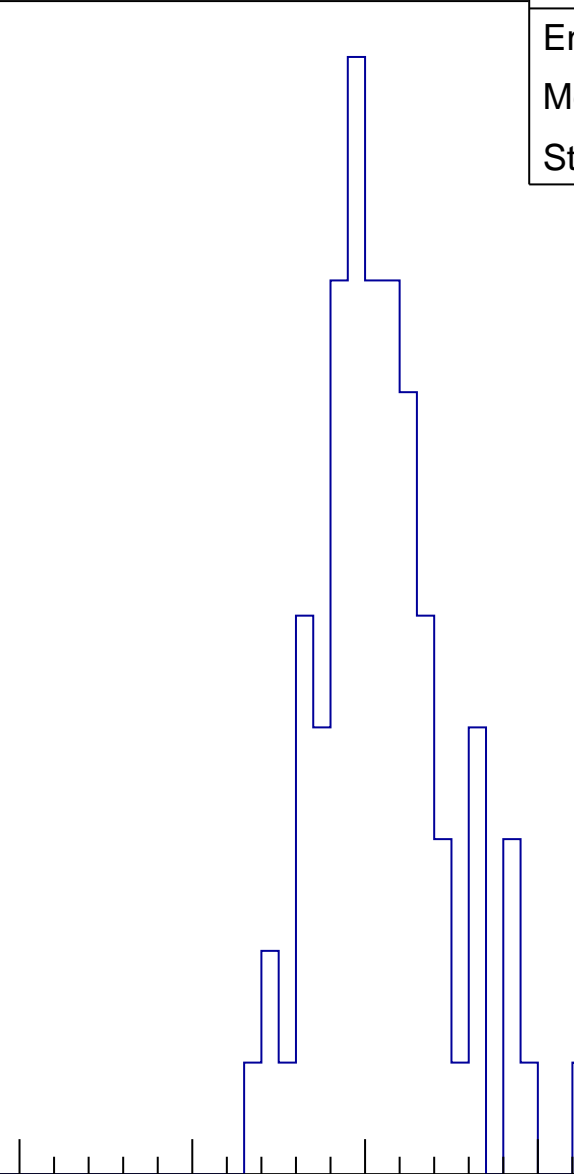
Entries	72
Mean	50.57
Std Dev	3.719

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

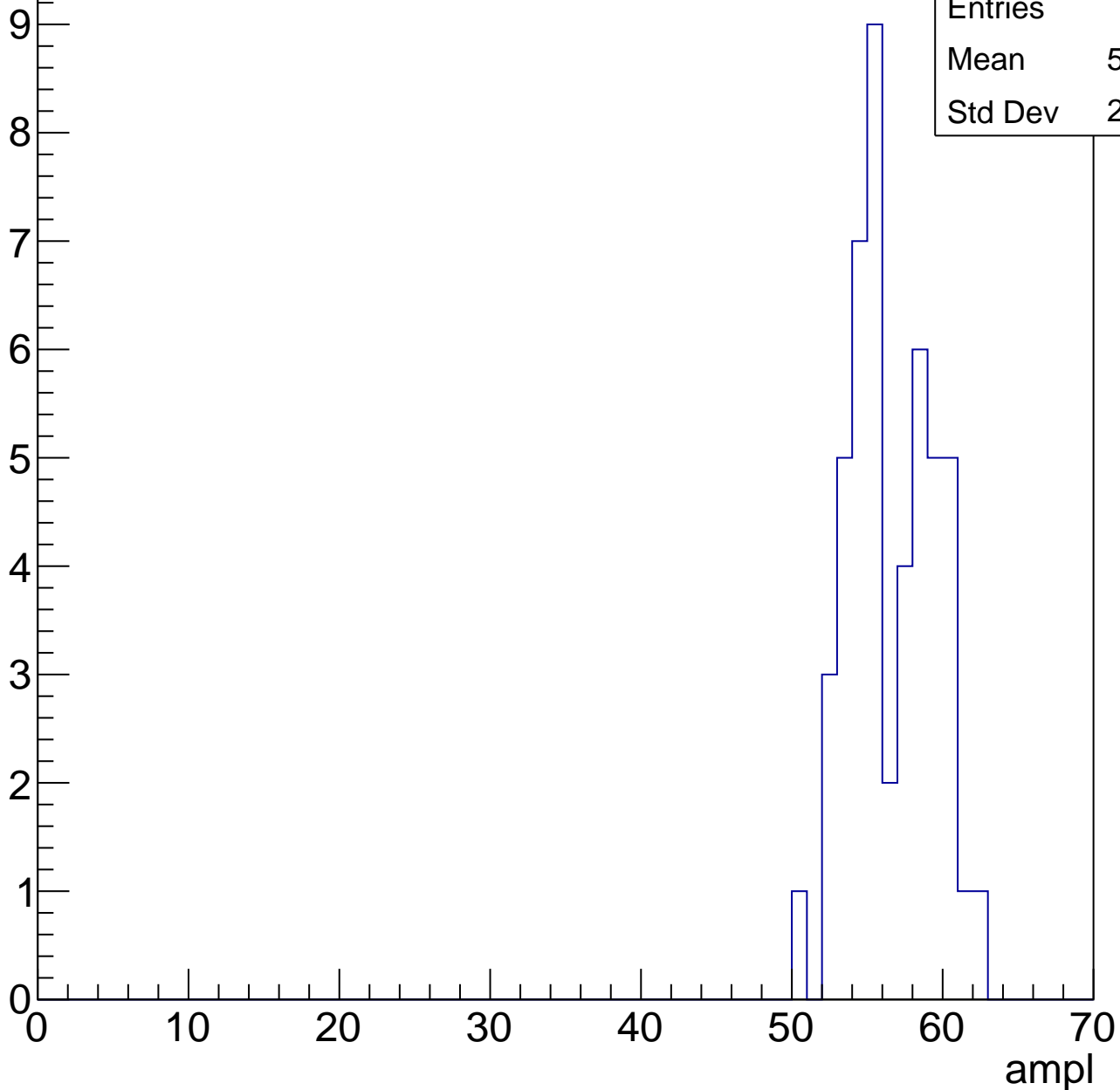


# B1L003S, U3-ch111, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	49
Mean	56.12
Std Dev	2.782

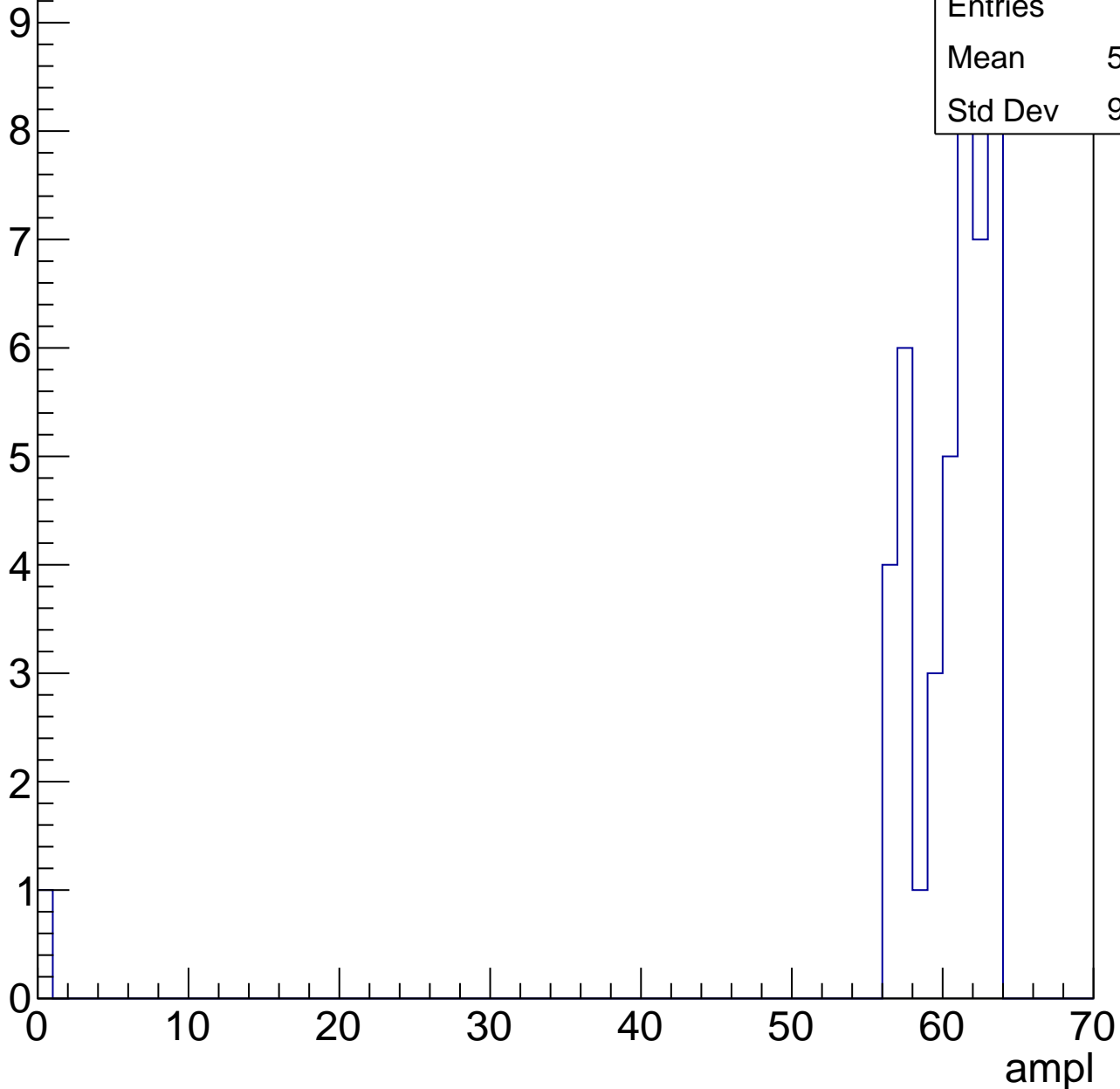


# B1L003S, U3-ch111, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

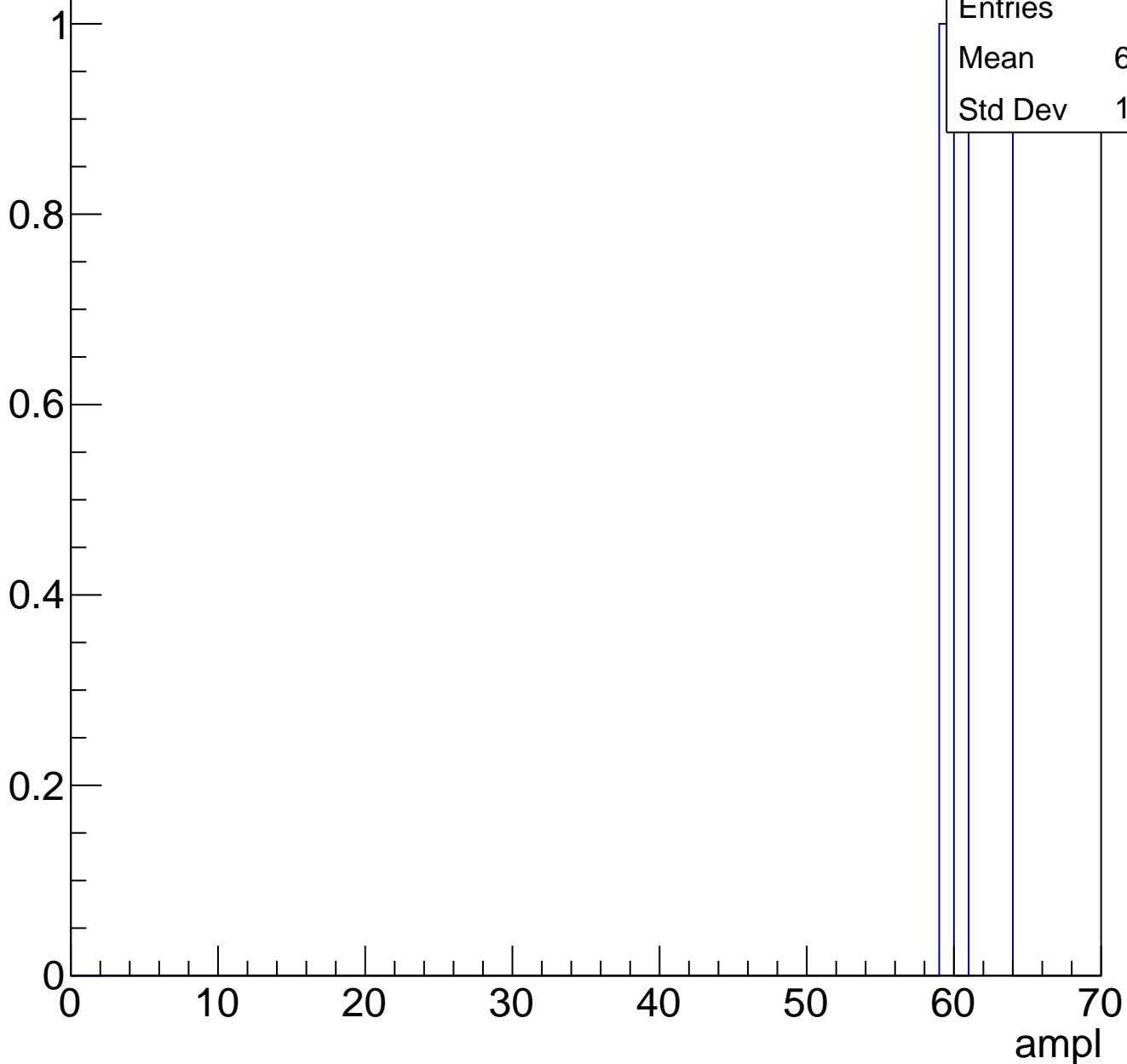
Entries	44
Mean	58.86
Std Dev	9.275



# B1L003S, U3-ch111, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch111, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U3-ch112, adc0

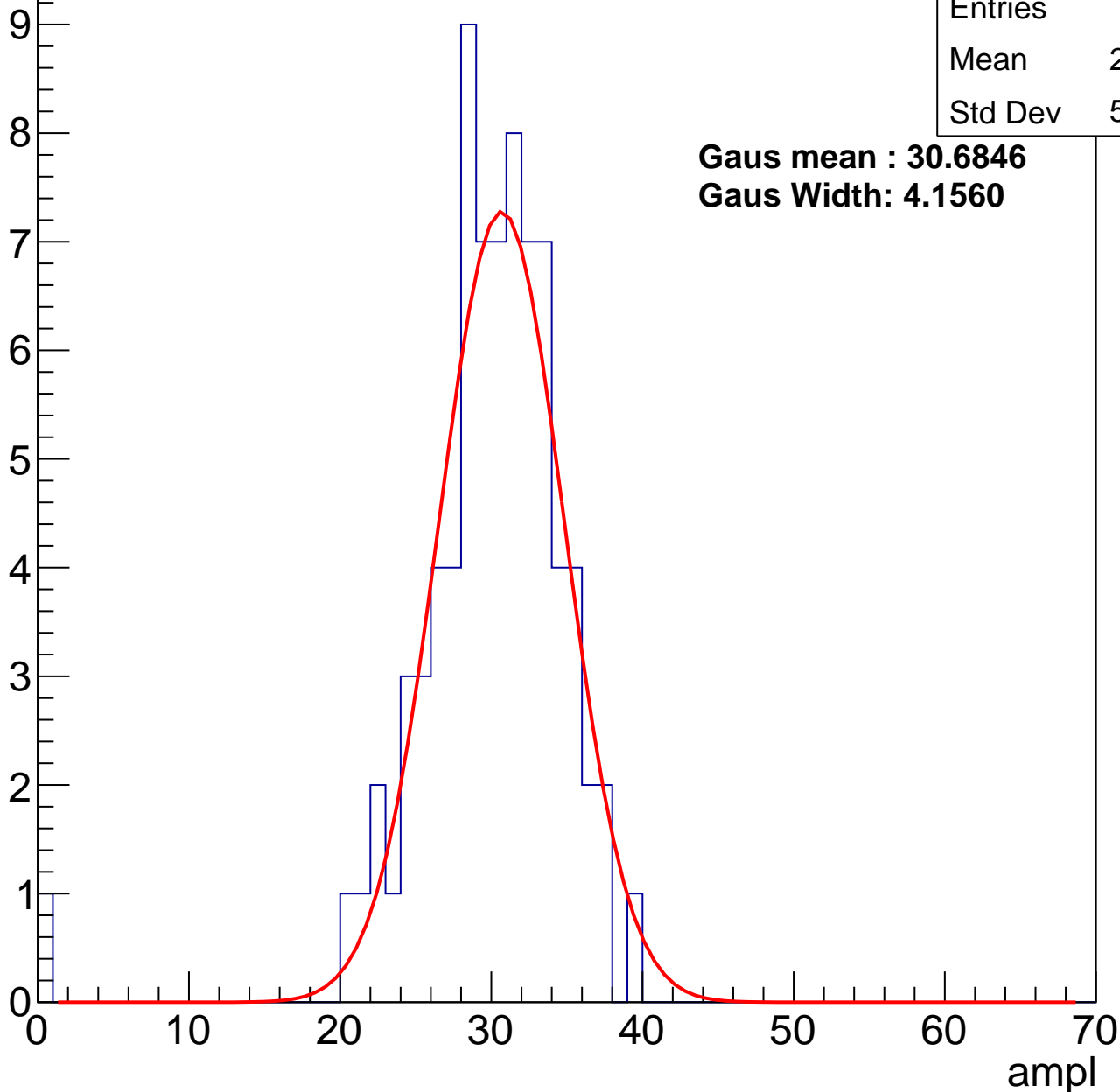
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	78
Mean	29.44
Std Dev	5.156

**Gaus mean : 30.6846**

**Gaus Width: 4.1560**



# B1L003S, U3-ch112, adc1

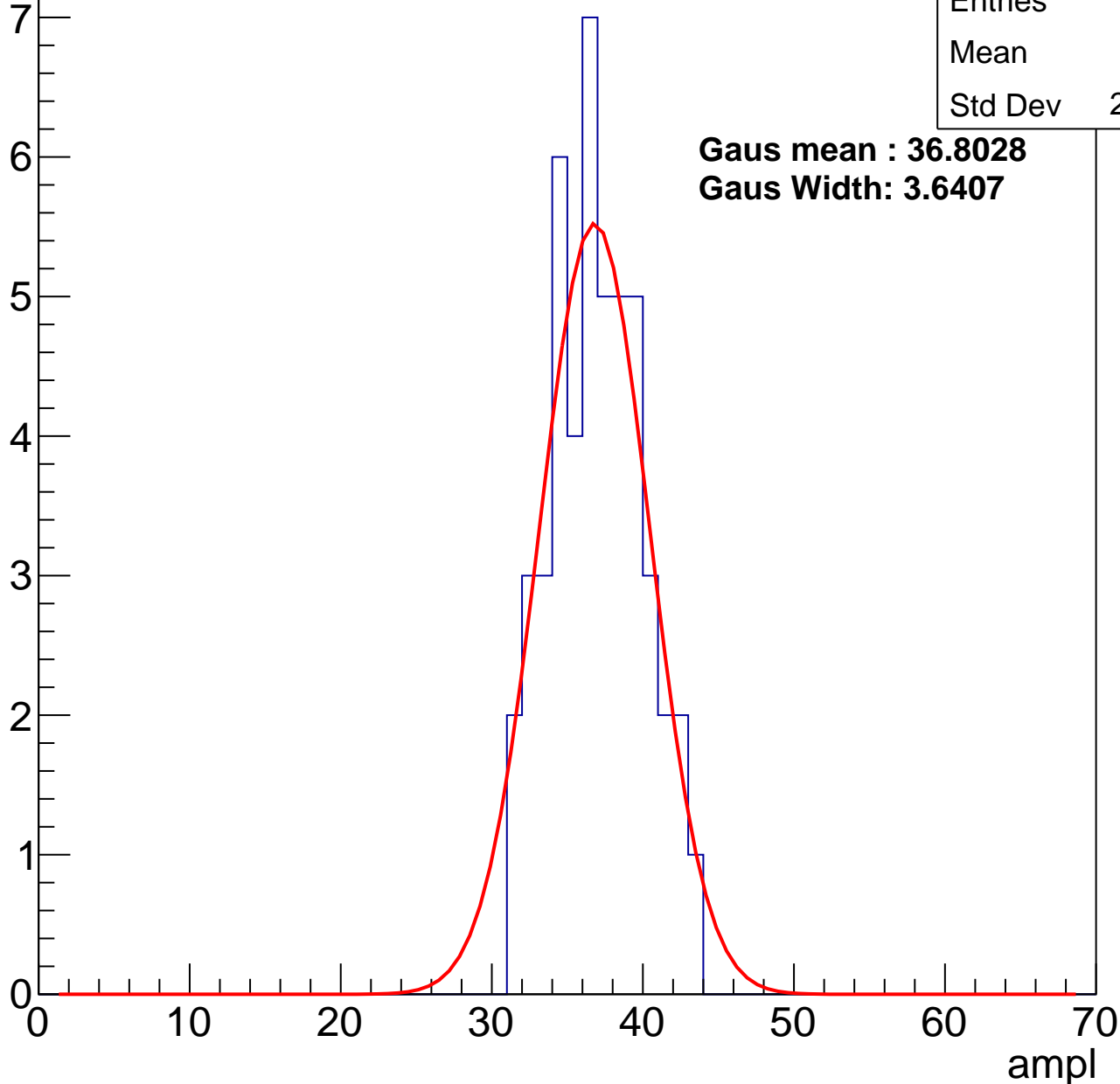
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	48
Mean	36.5
Std Dev	2.993

**Gaus mean : 36.8028**

**Gaus Width: 3.6407**



# B1L003S, U3-ch112, adc2

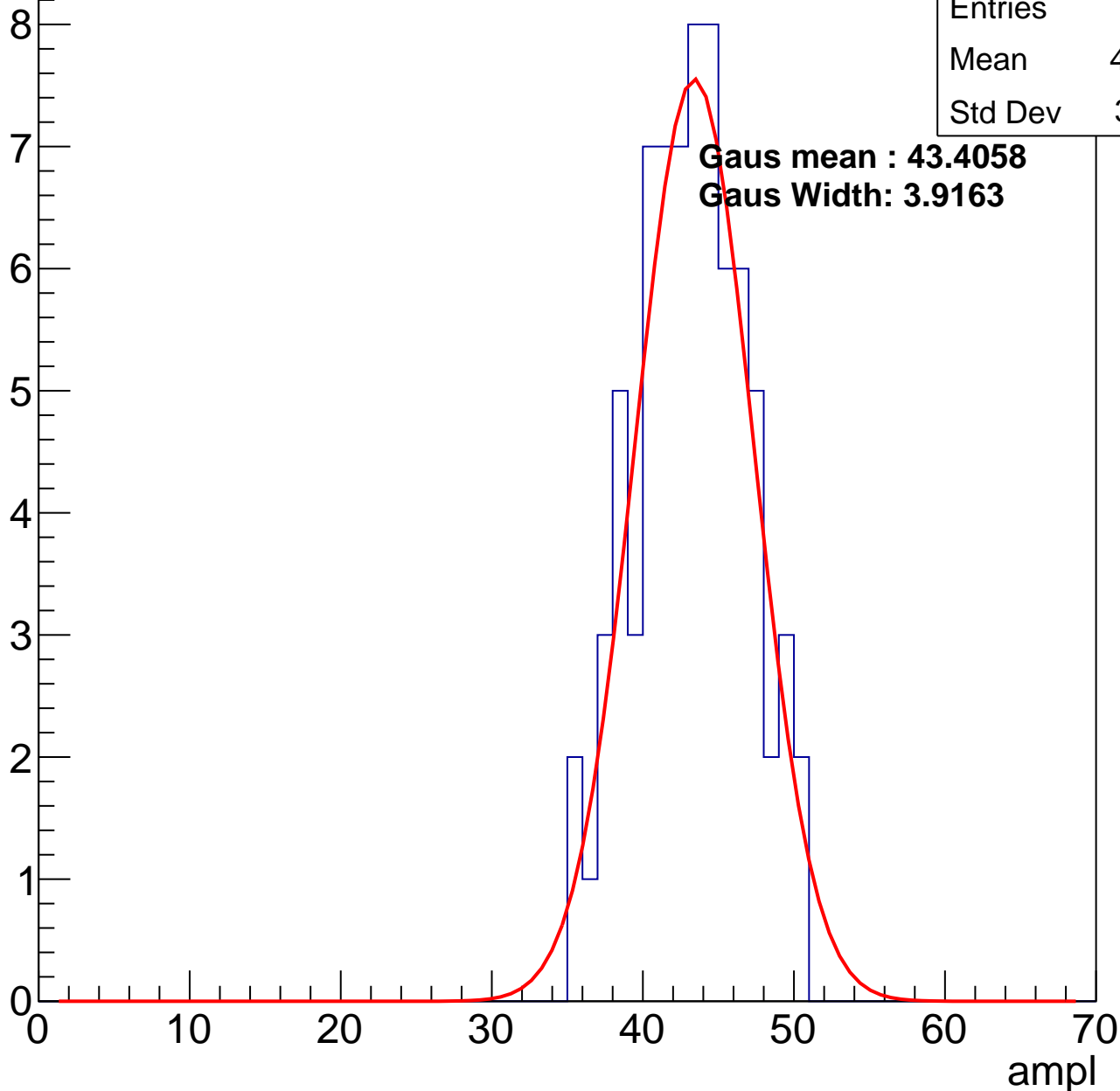
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	75
Mean	42.73
Std Dev	3.601

**Gaus mean : 43.4058**

**Gaus Width: 3.9163**

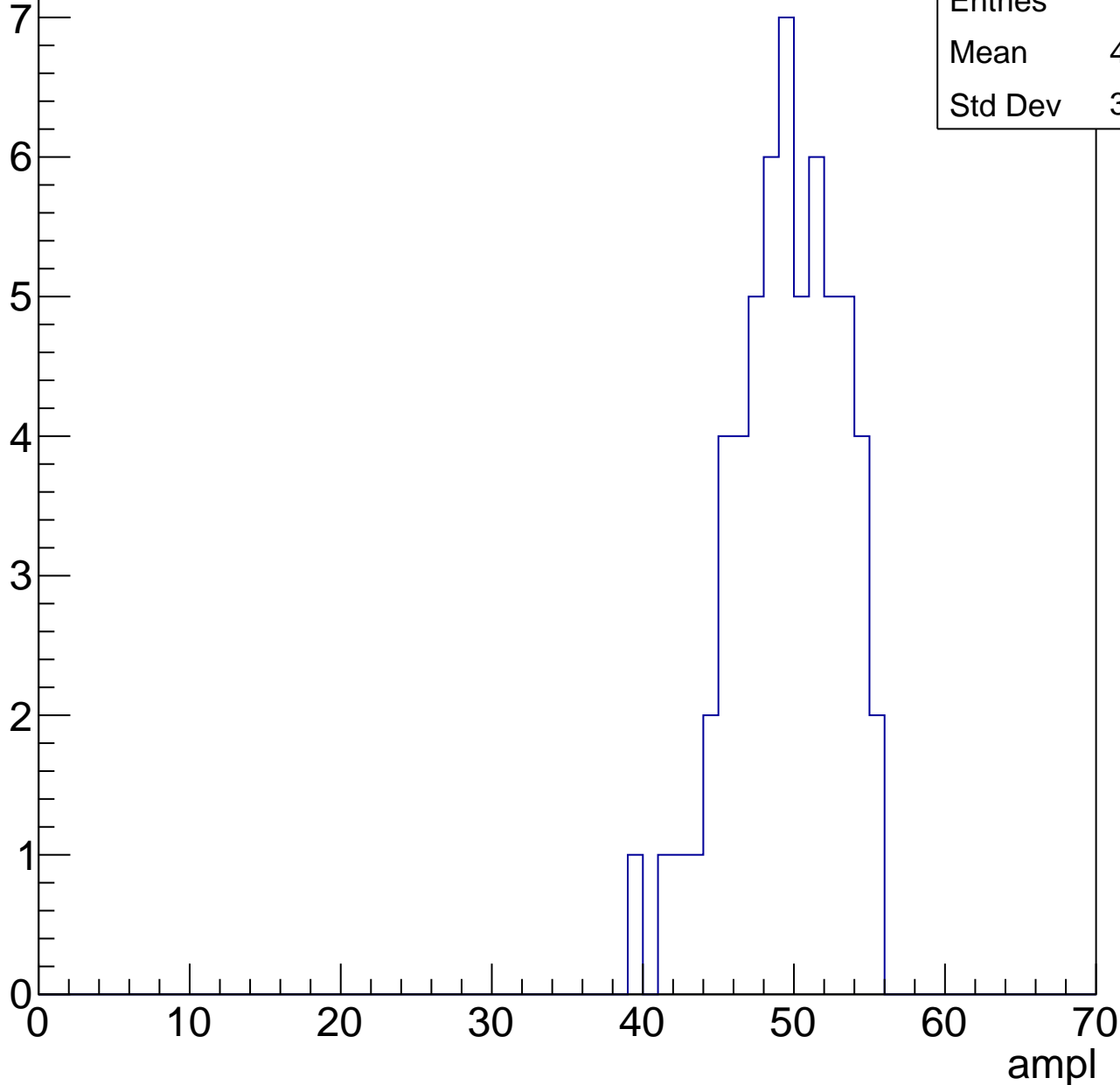


# B1L003S, U3-ch112, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	48.98
Std Dev	3.568

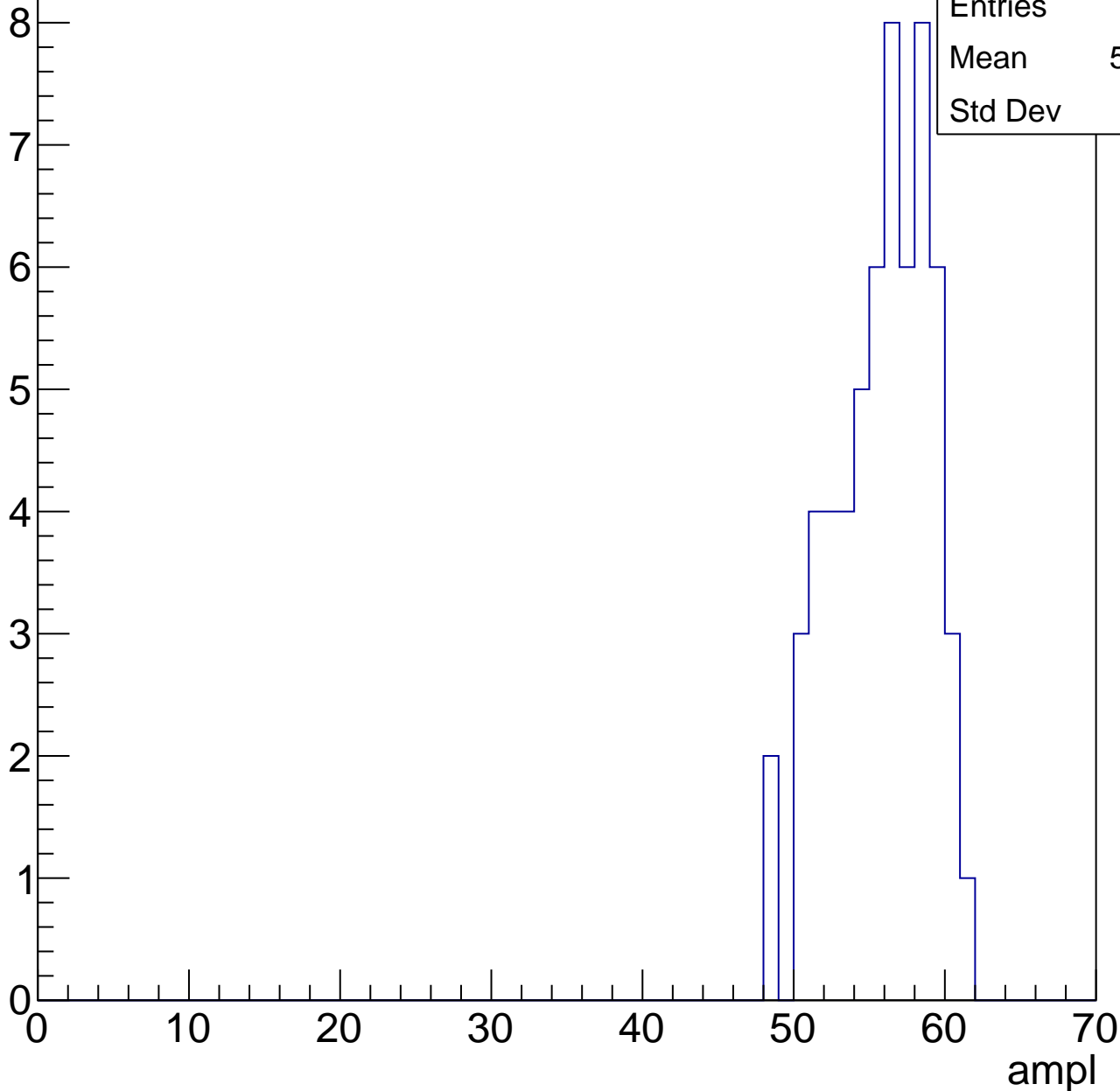


# B1L003S, U3-ch112, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	55.32
Std Dev	3.16

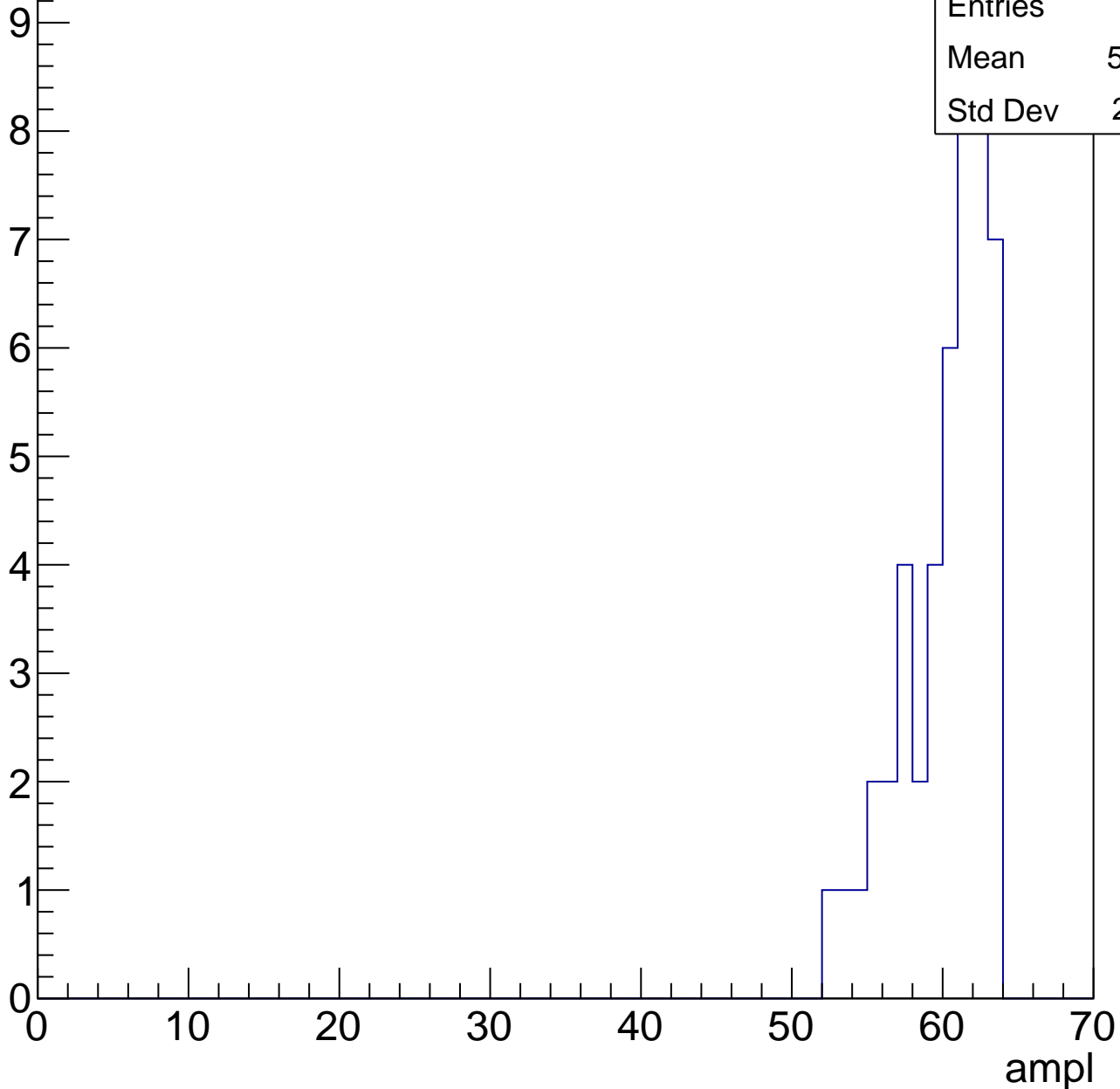


# B1L003S, U3-ch112, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

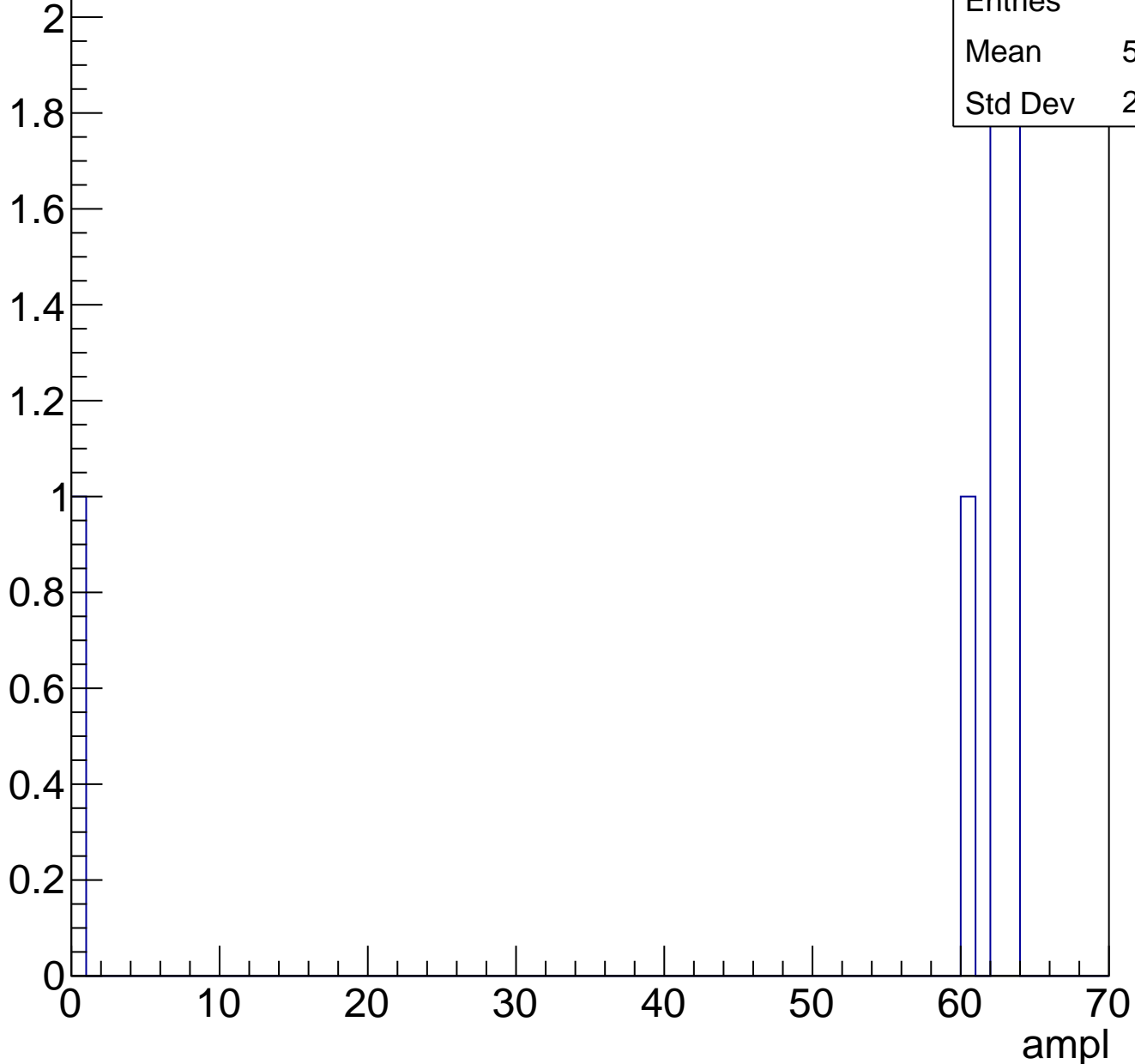
Entries	47
Mean	59.72
Std Dev	2.841



# B1L003S, U3-ch112, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch112, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	3
Mean	21
Std Dev	29.7

# B1L003S, U3-ch113, adc0

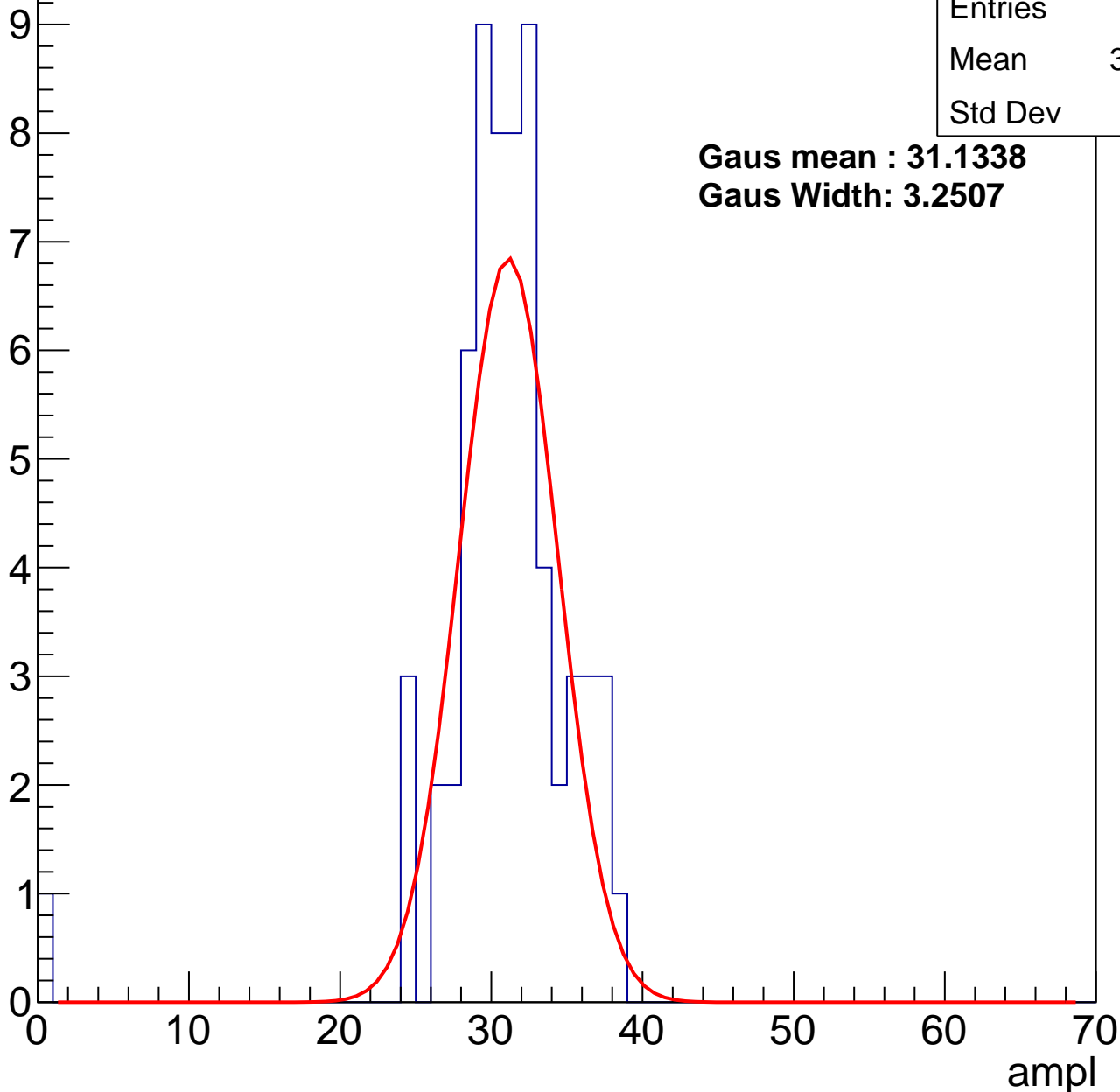
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	30.39
Std Dev	4.98

**Gaus mean : 31.1338**

**Gaus Width: 3.2507**



# B1L003S, U3-ch113, adc1

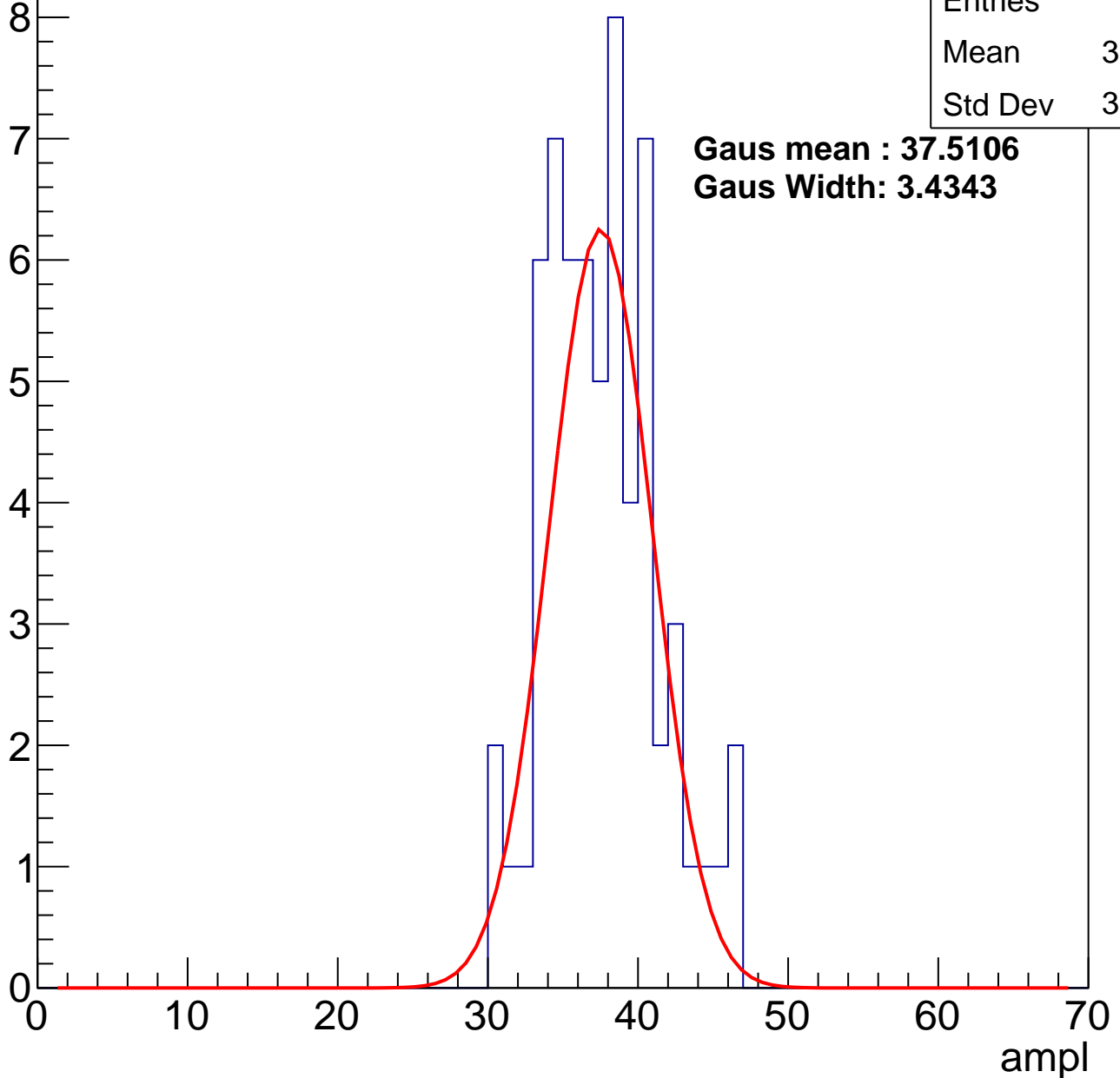
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	37.17
Std Dev	3.675

**Gaus mean : 37.5106**

**Gaus Width: 3.4343**



# B1L003S, U3-ch113, adc2

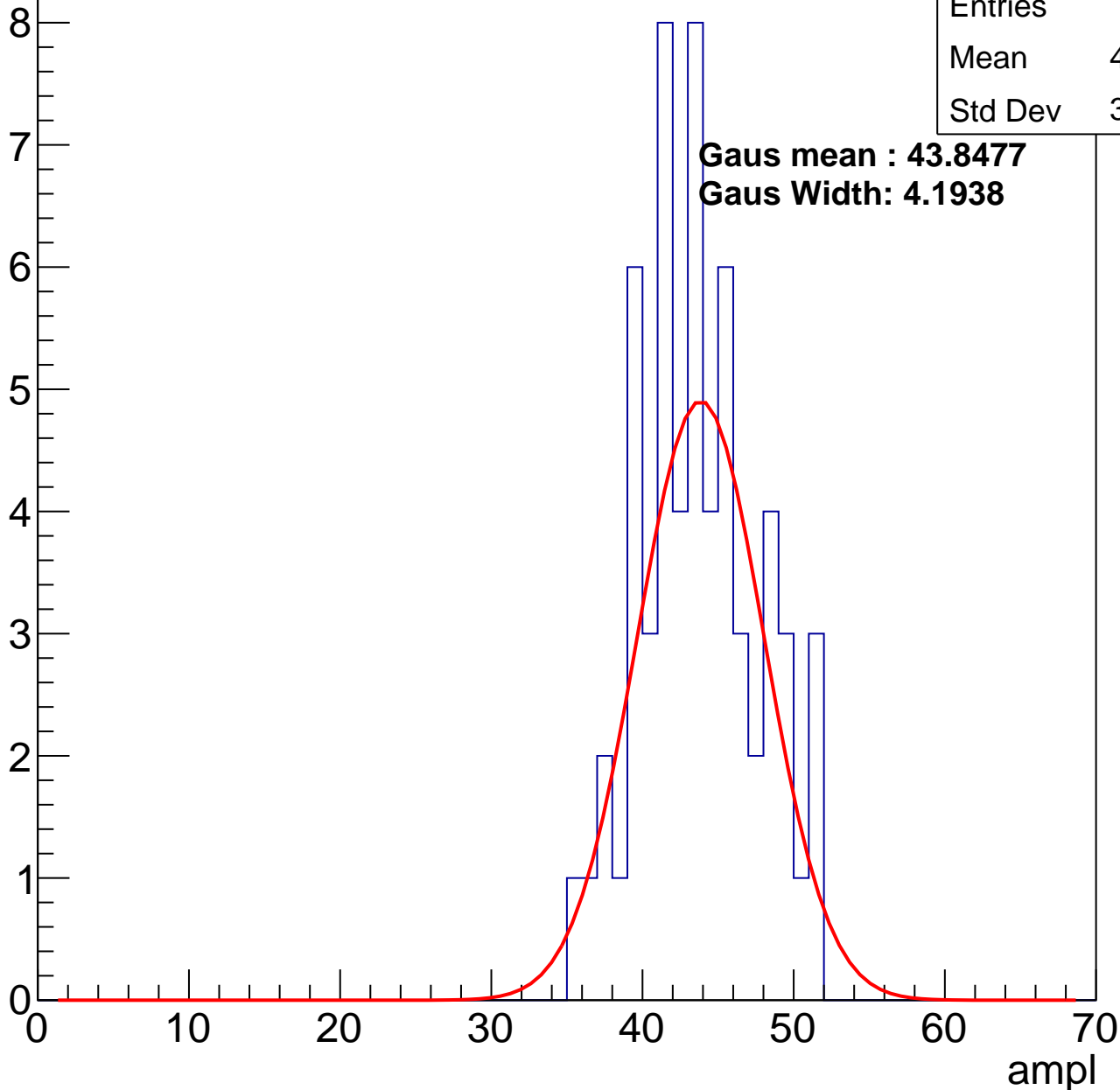
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	43.28
Std Dev	3.873

**Gaus mean : 43.8477**

**Gaus Width: 4.1938**

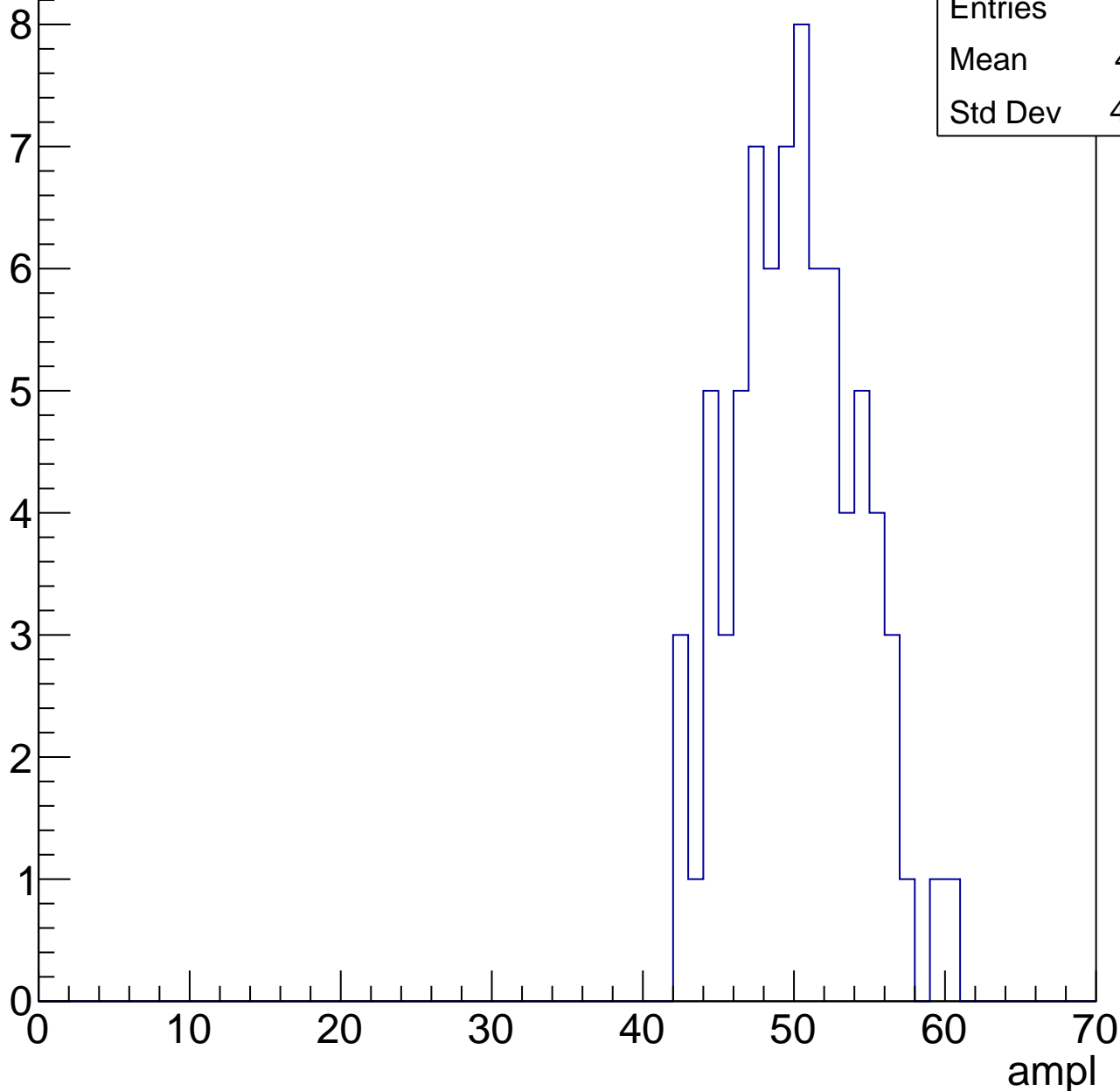


# B1L003S, U3-ch113, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	76
Mean	49.71
Std Dev	4.052

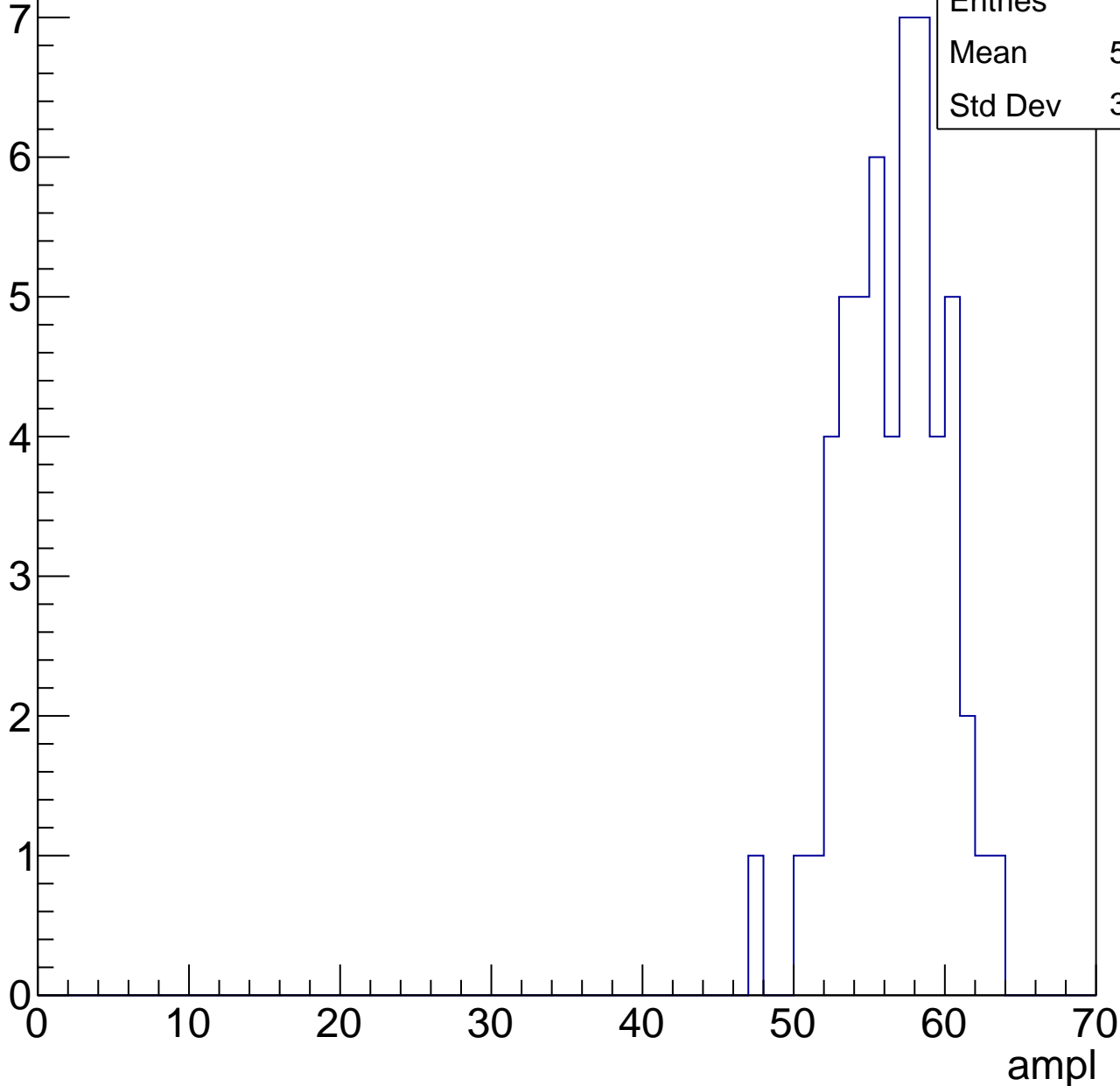


# B1L003S, U3-ch113, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	54
Mean	56.17
Std Dev	3.225

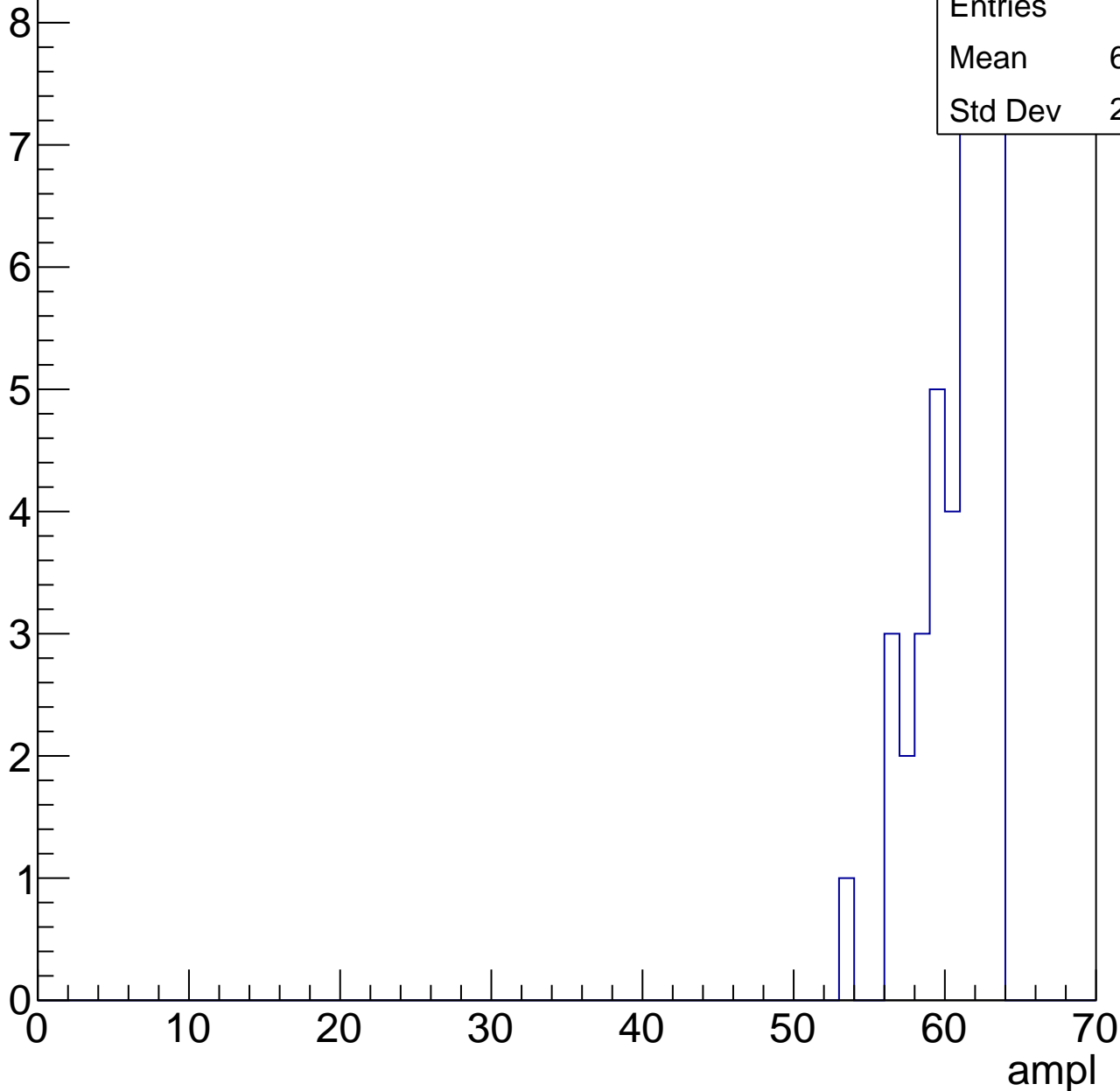


# B1L003S, U3-ch113, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	42
Mean	60.29
Std Dev	2.393



# B1L003S, U3-ch113, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	3
Mean	41.67
Std Dev	29.47



# B1L003S, U3-ch113, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L003S, U3-ch114, adc0

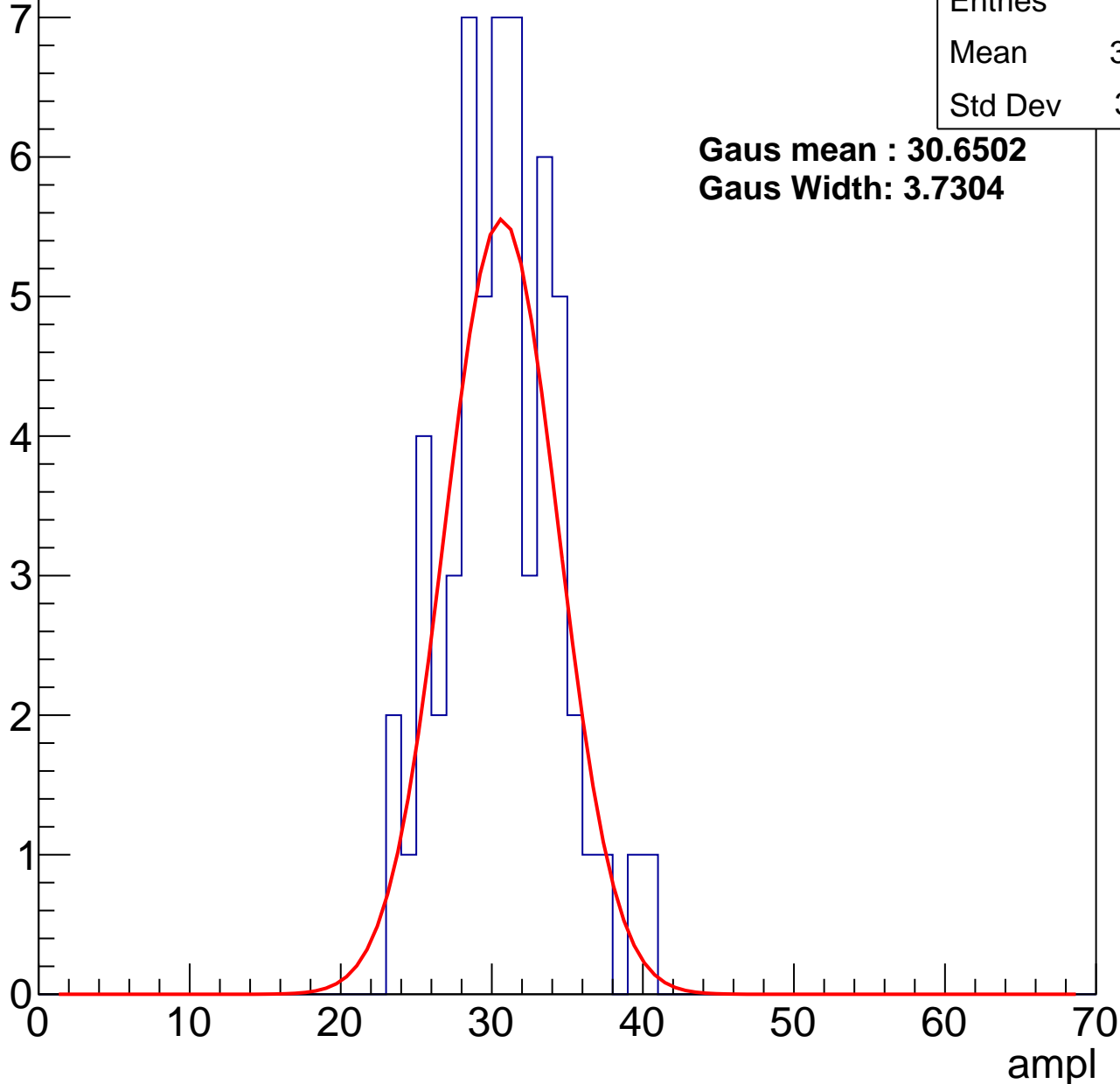
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	30.29
Std Dev	3.691

**Gaus mean : 30.6502**

**Gaus Width: 3.7304**



# B1L003S, U3-ch114, adc1

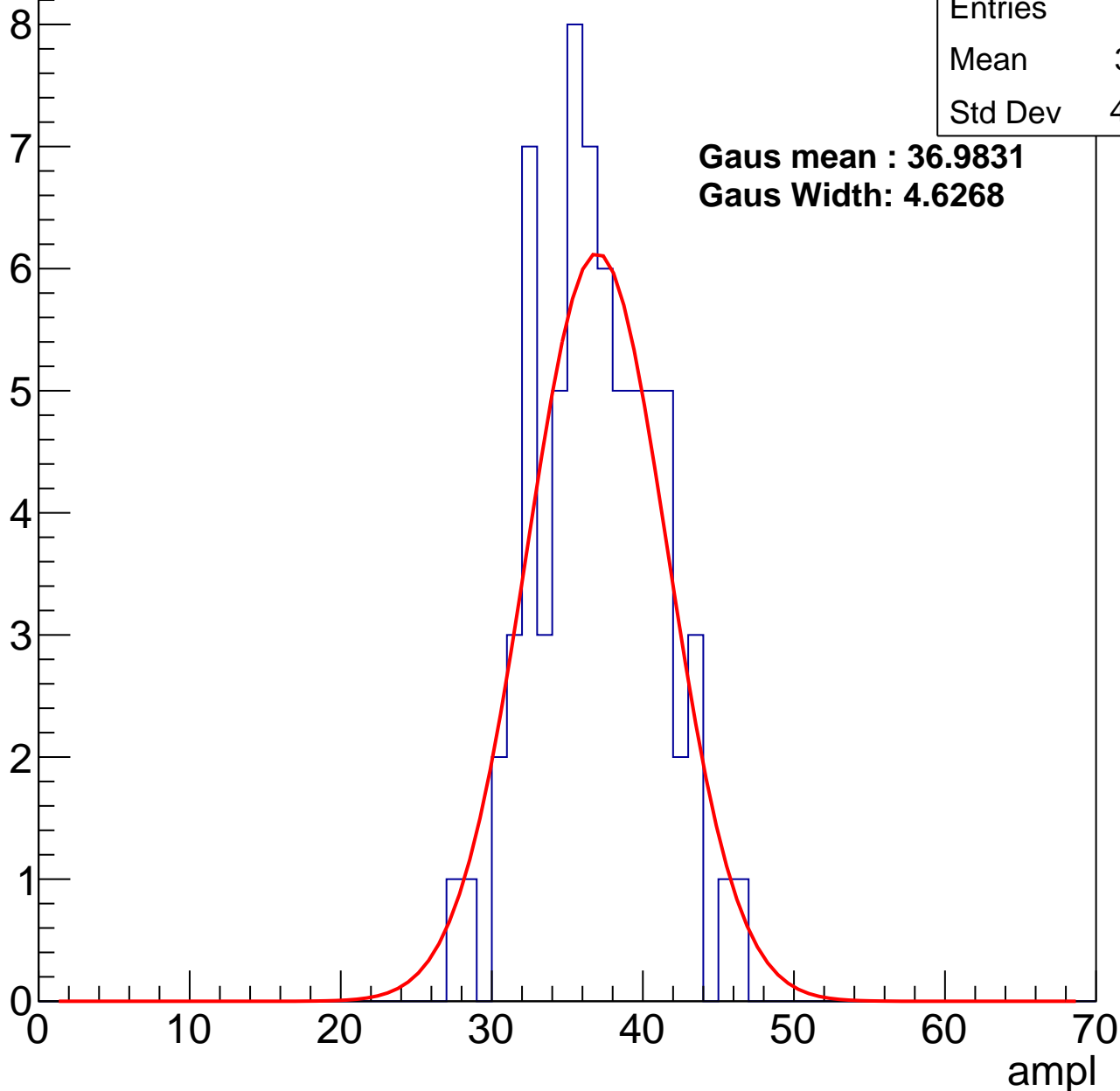
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	36.41
Std Dev	4.005

**Gaus mean : 36.9831**

**Gaus Width: 4.6268**



# B1L003S, U3-ch114, adc2

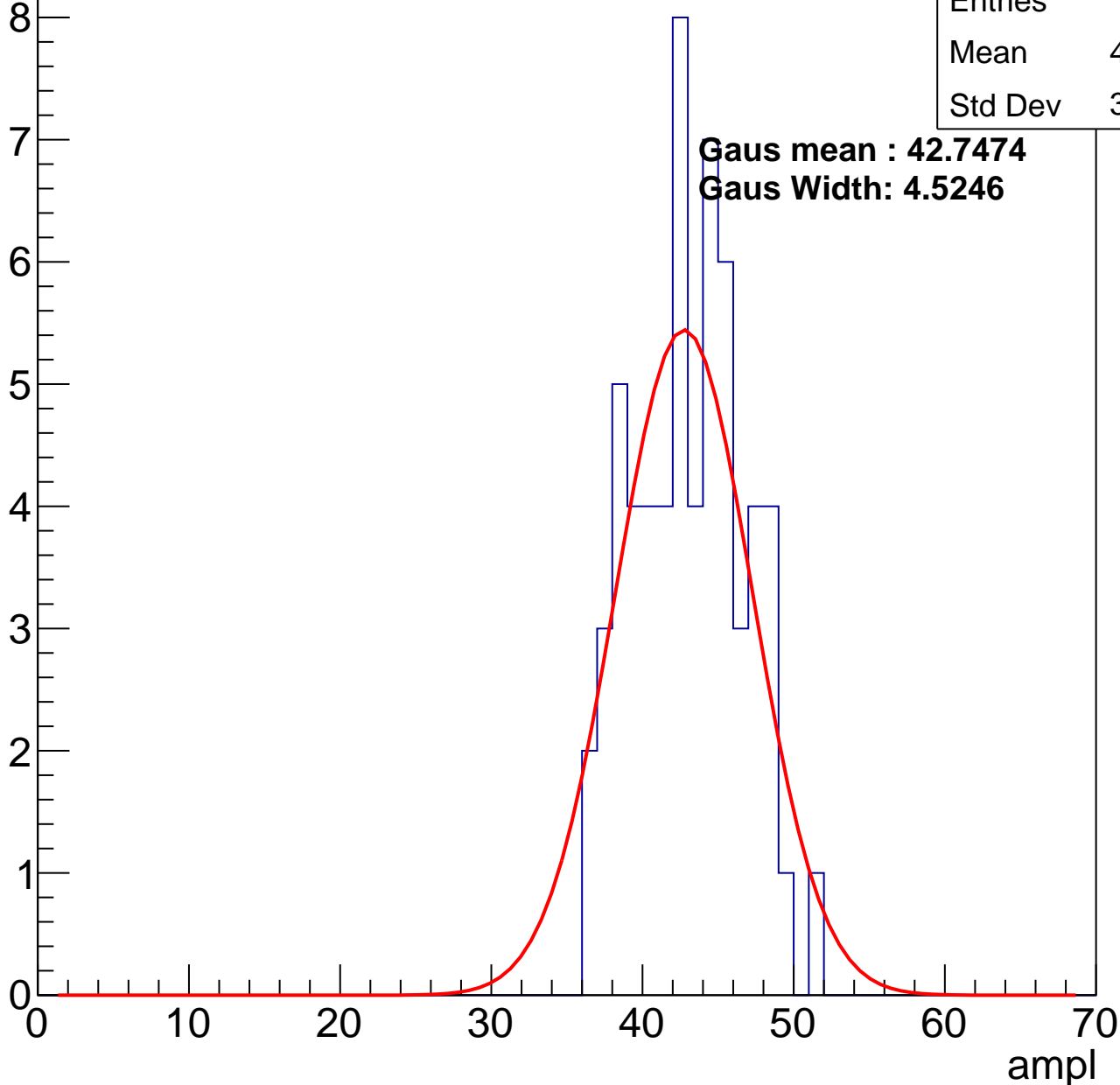
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	42.62
Std Dev	3.578

**Gaus mean : 42.7474**

**Gaus Width: 4.5246**

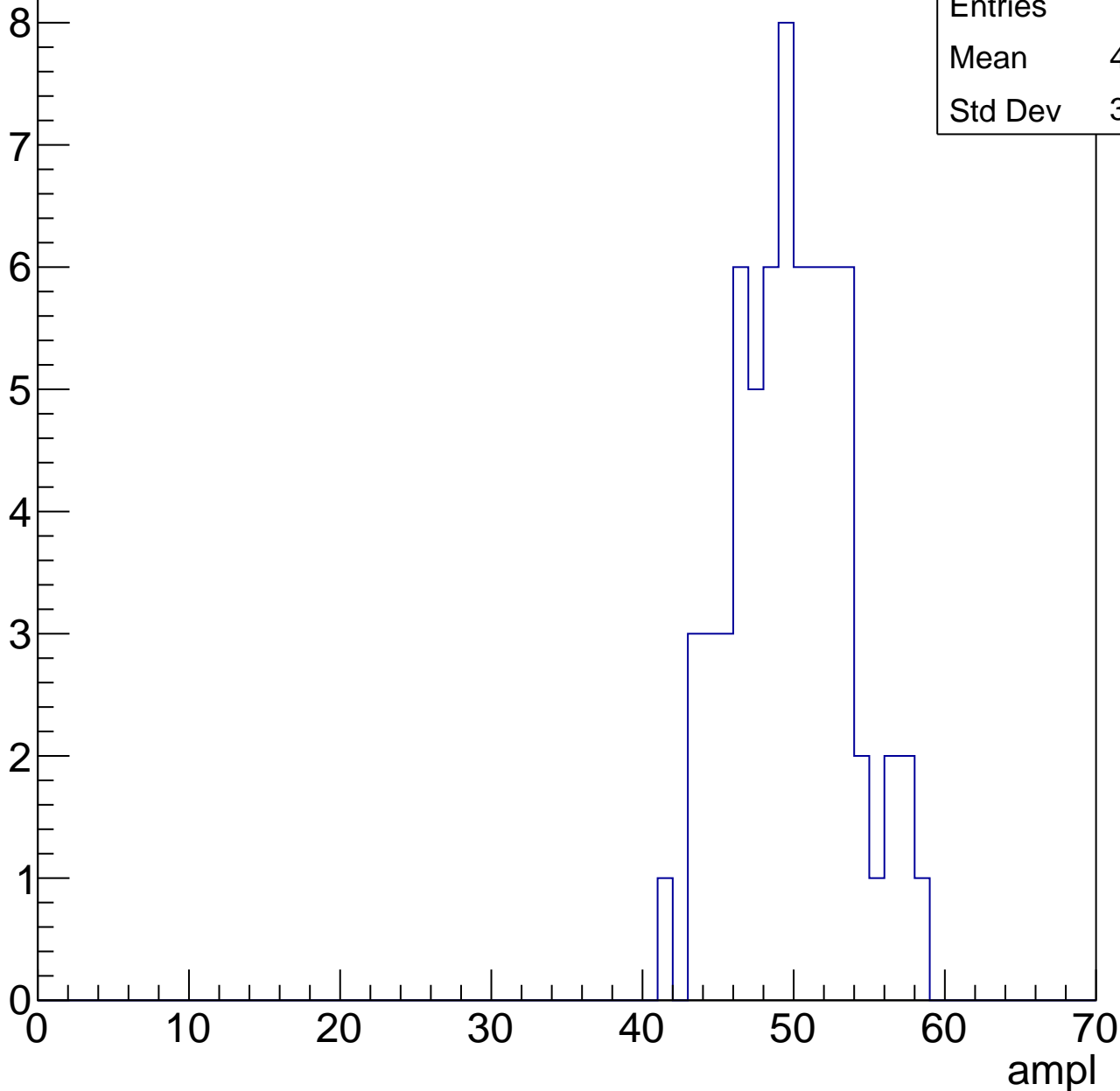


# B1L003S, U3-ch114, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	49.42
Std Dev	3.738

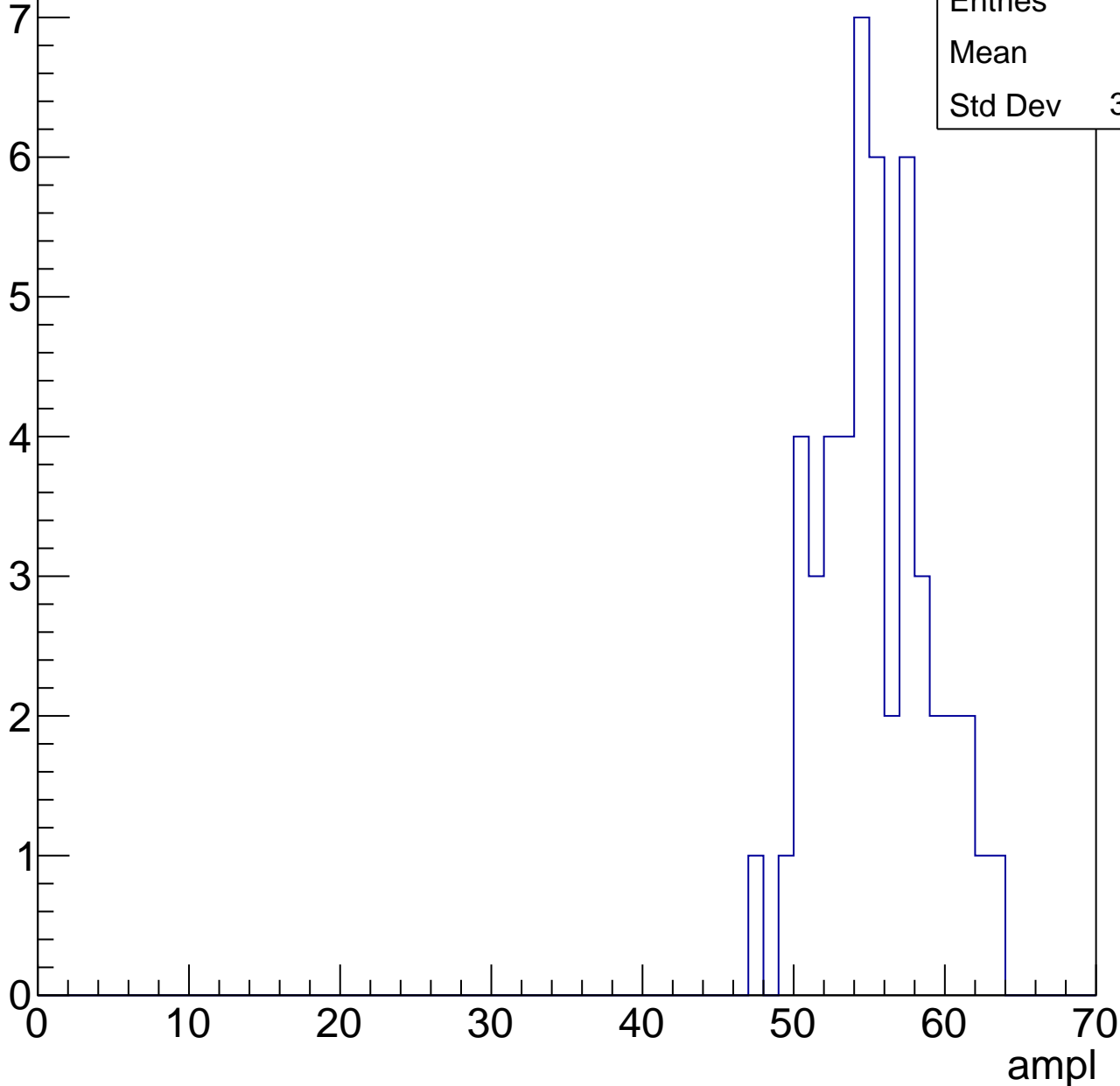


# B1L003S, U3-ch114, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	49
Mean	54.9
Std Dev	3.576

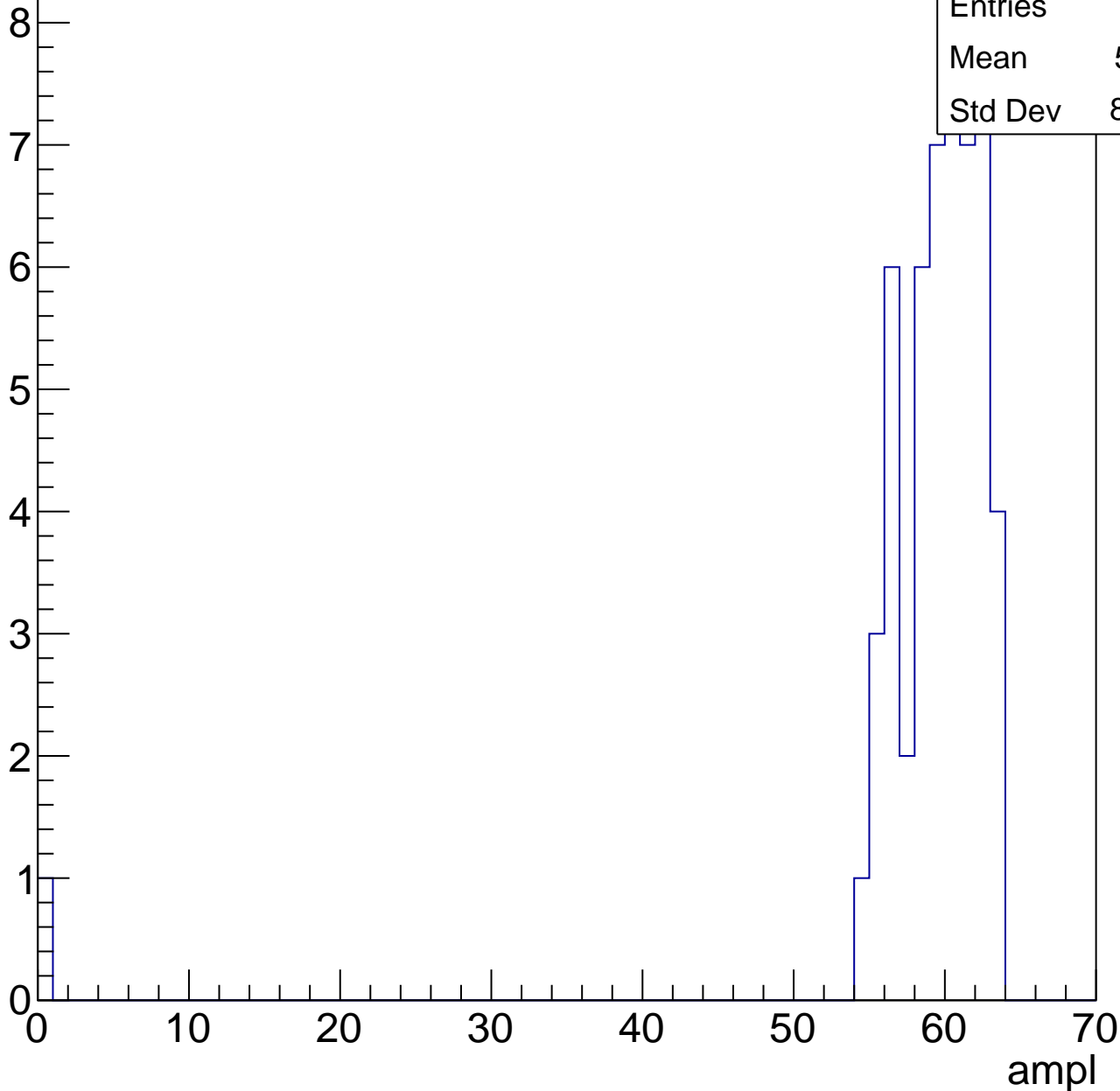


# B1L003S, U3-ch114, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

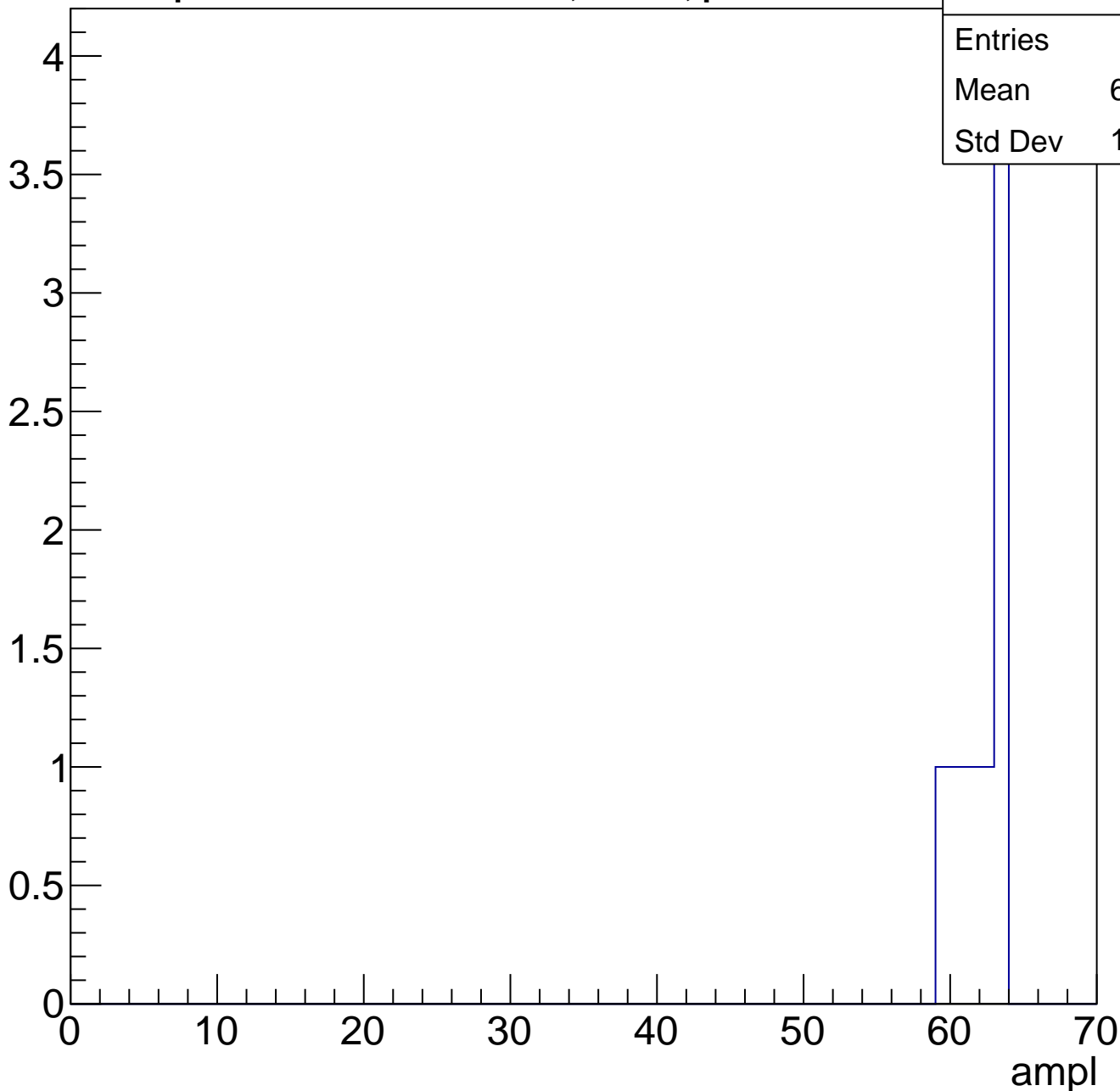
Entries	53
Mean	58.21
Std Dev	8.424



# B1L003S, U3-ch114, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch114, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U3-ch115, adc0

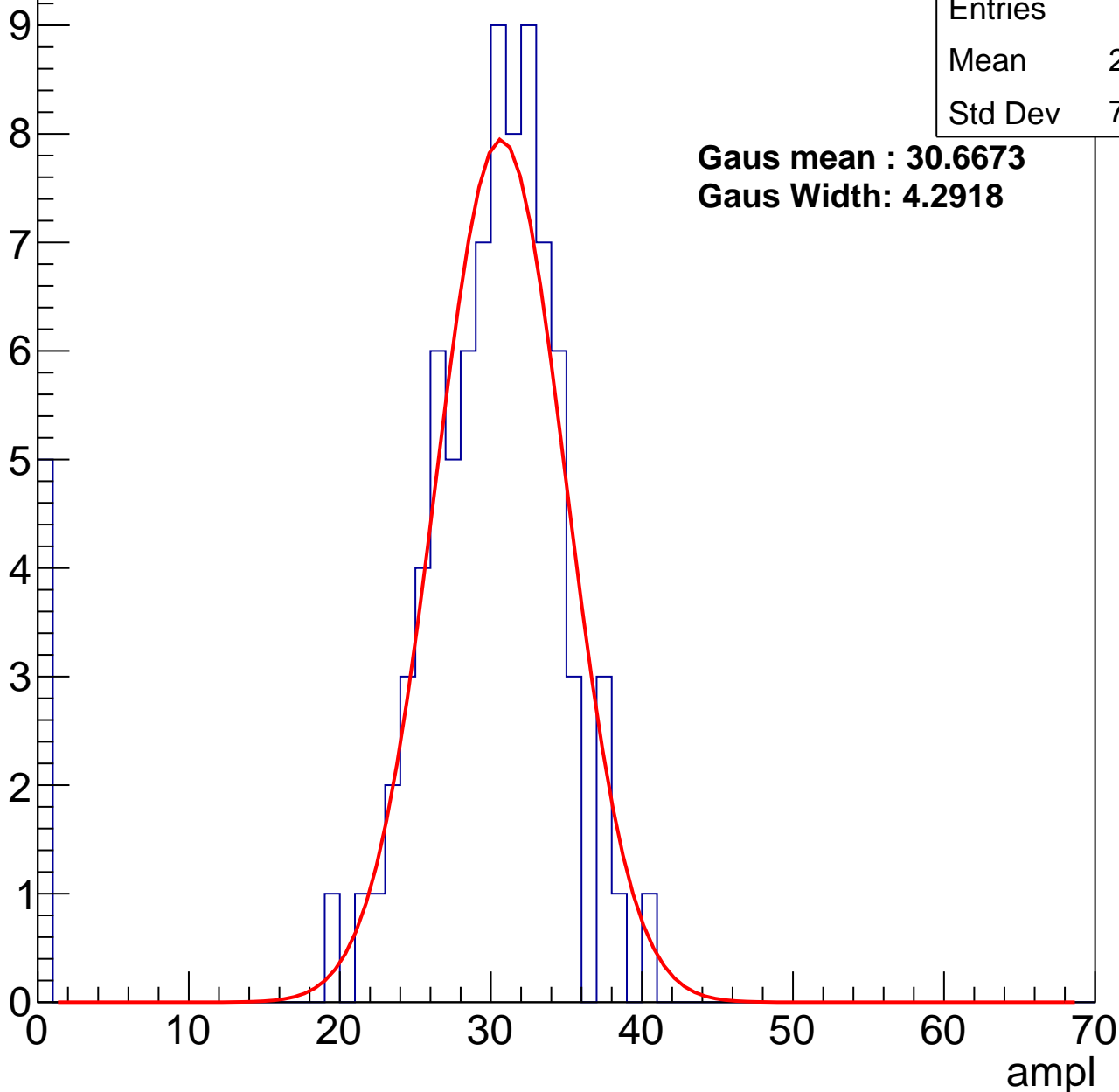
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	88
Mean	28.15
Std Dev	7.928

**Gaus mean : 30.6673**

**Gaus Width: 4.2918**



# B1L003S, U3-ch115, adc1

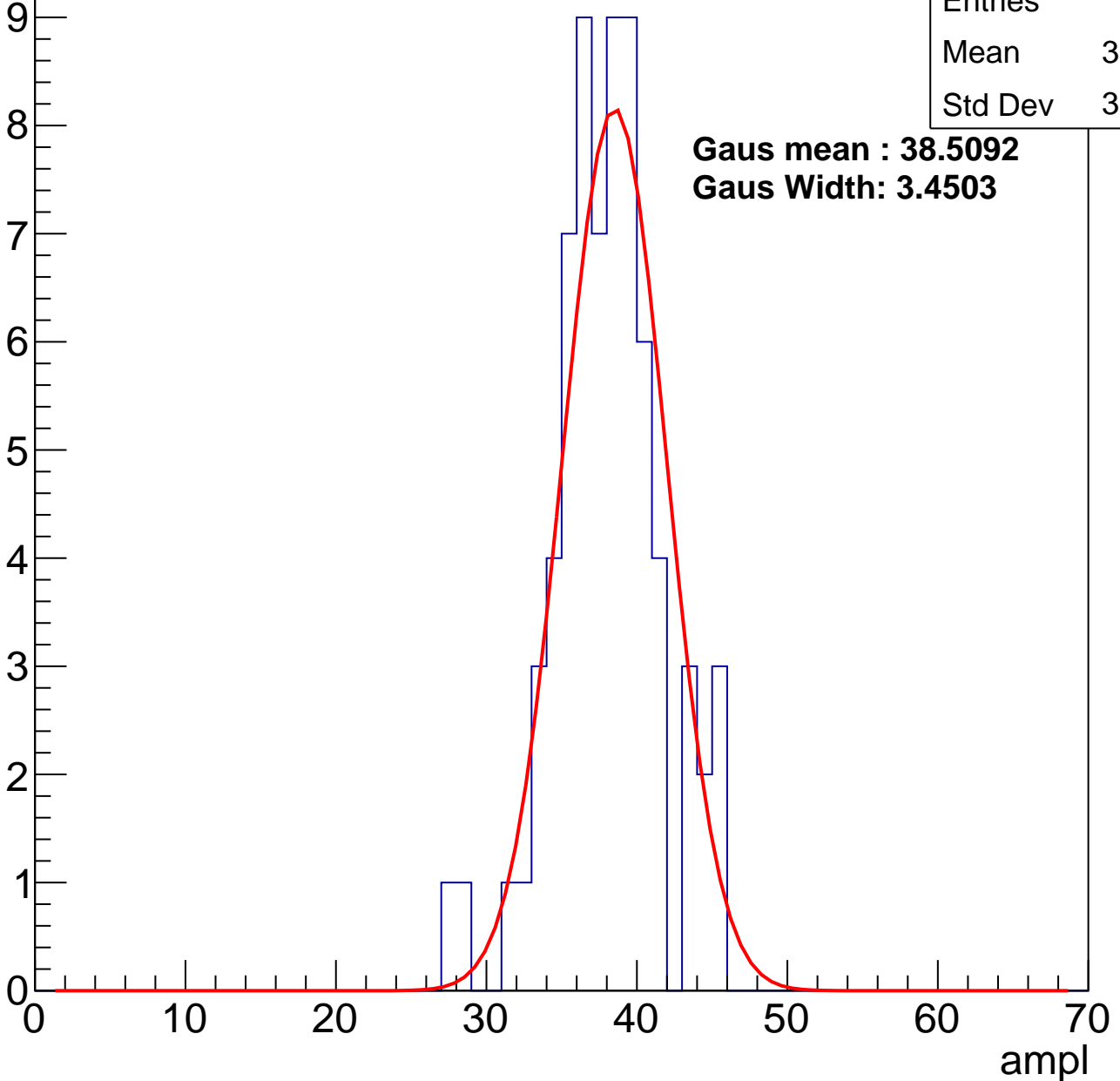
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	37.57
Std Dev	3.588

**Gaus mean : 38.5092**

**Gaus Width: 3.4503**



# B1L003S, U3-ch115, adc2

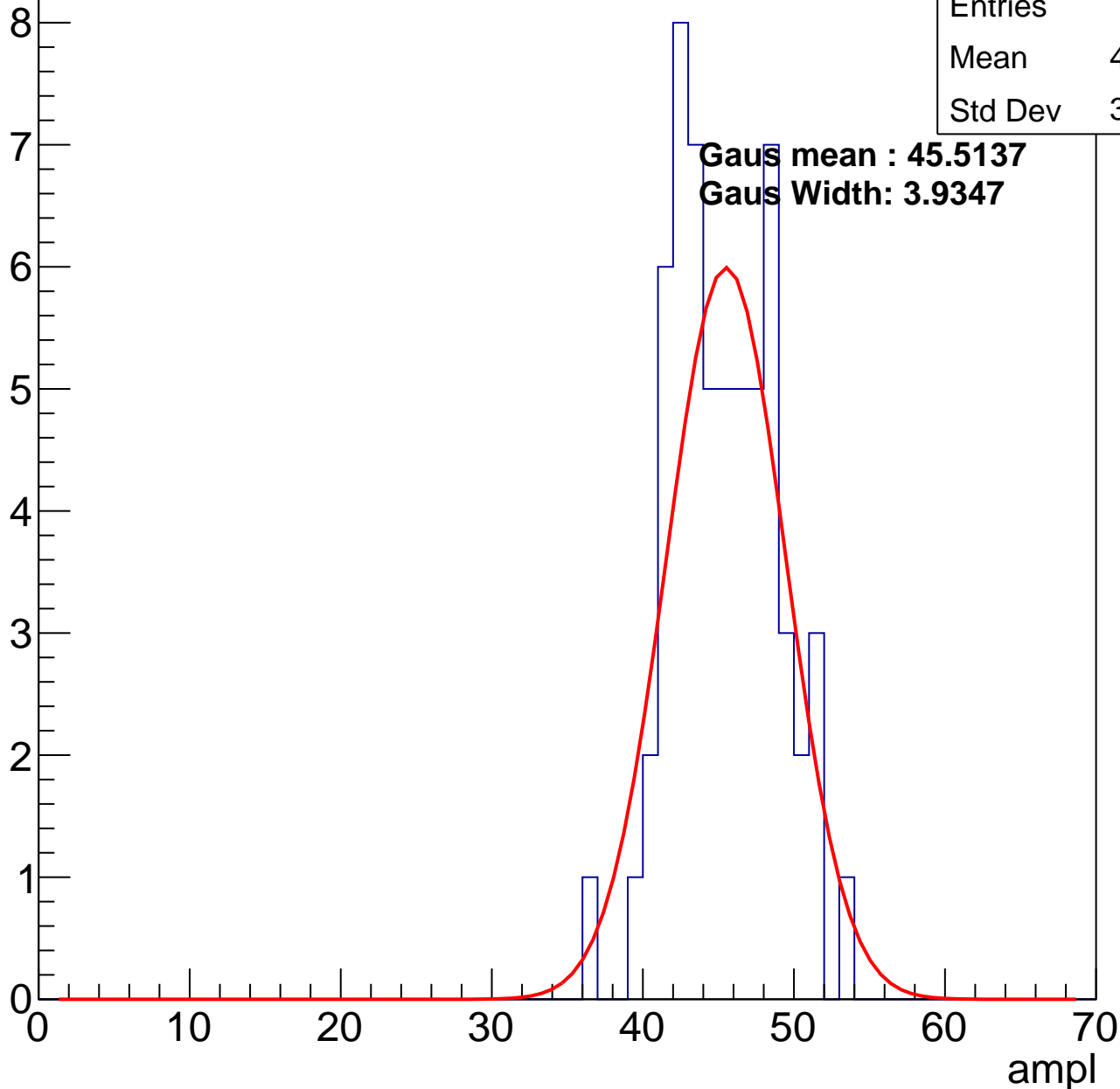
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	44.87
Std Dev	3.447

**Gaus mean : 45.5137**

**Gaus Width: 3.9347**

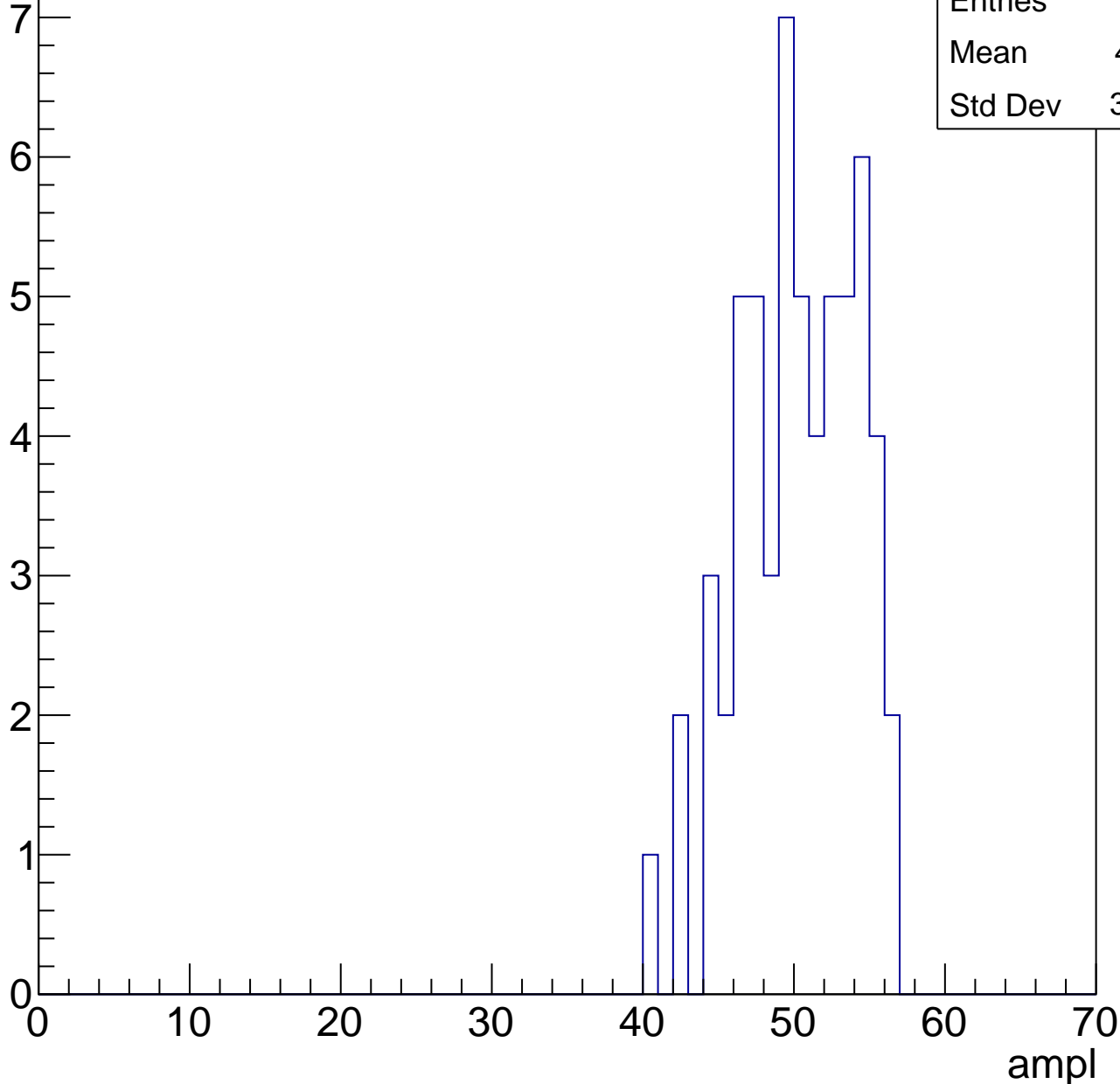


# B1L003S, U3-ch115, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	49.71
Std Dev	3.823

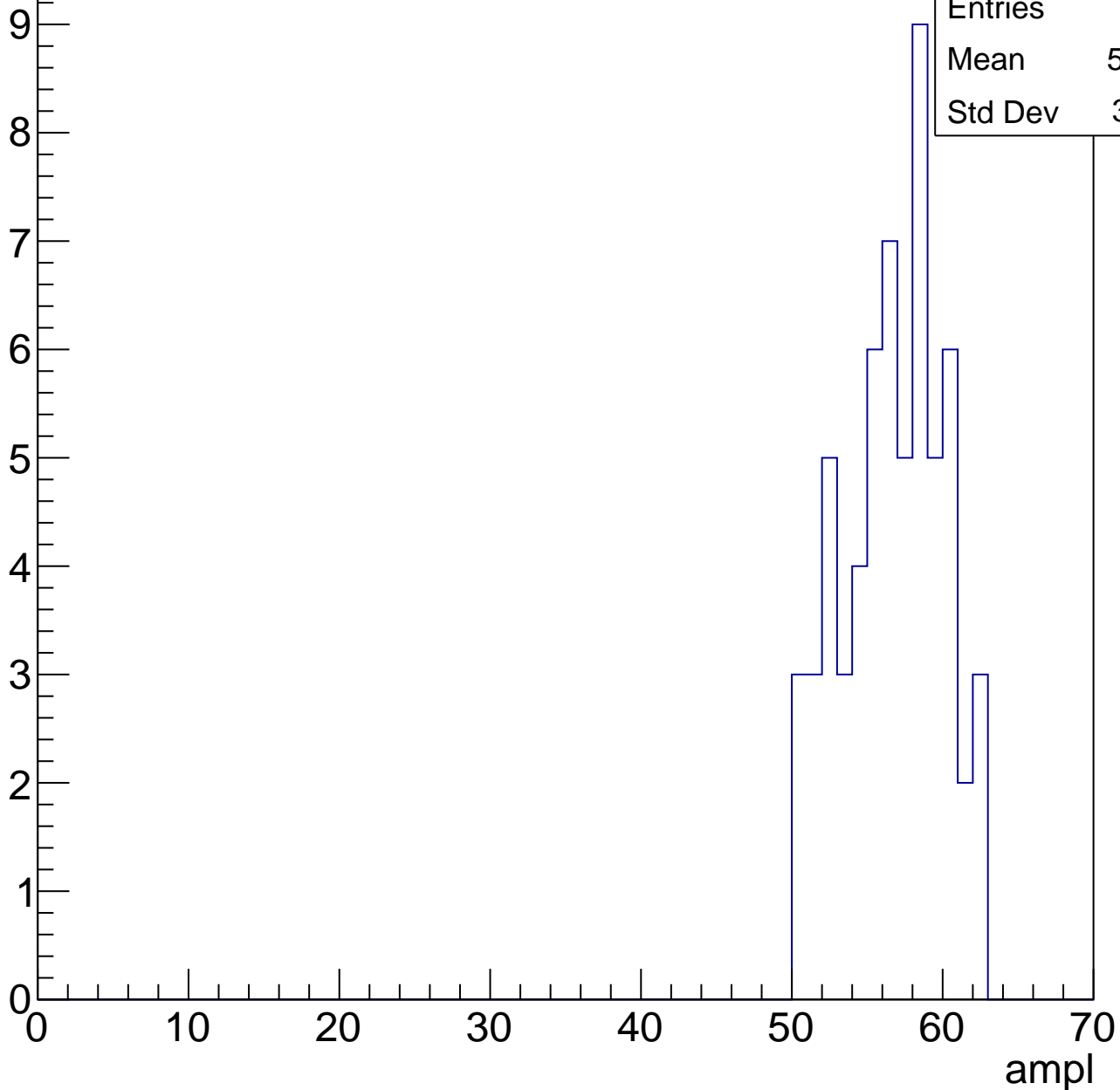


# B1L003S, U3-ch115, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	56.23
Std Dev	3.261

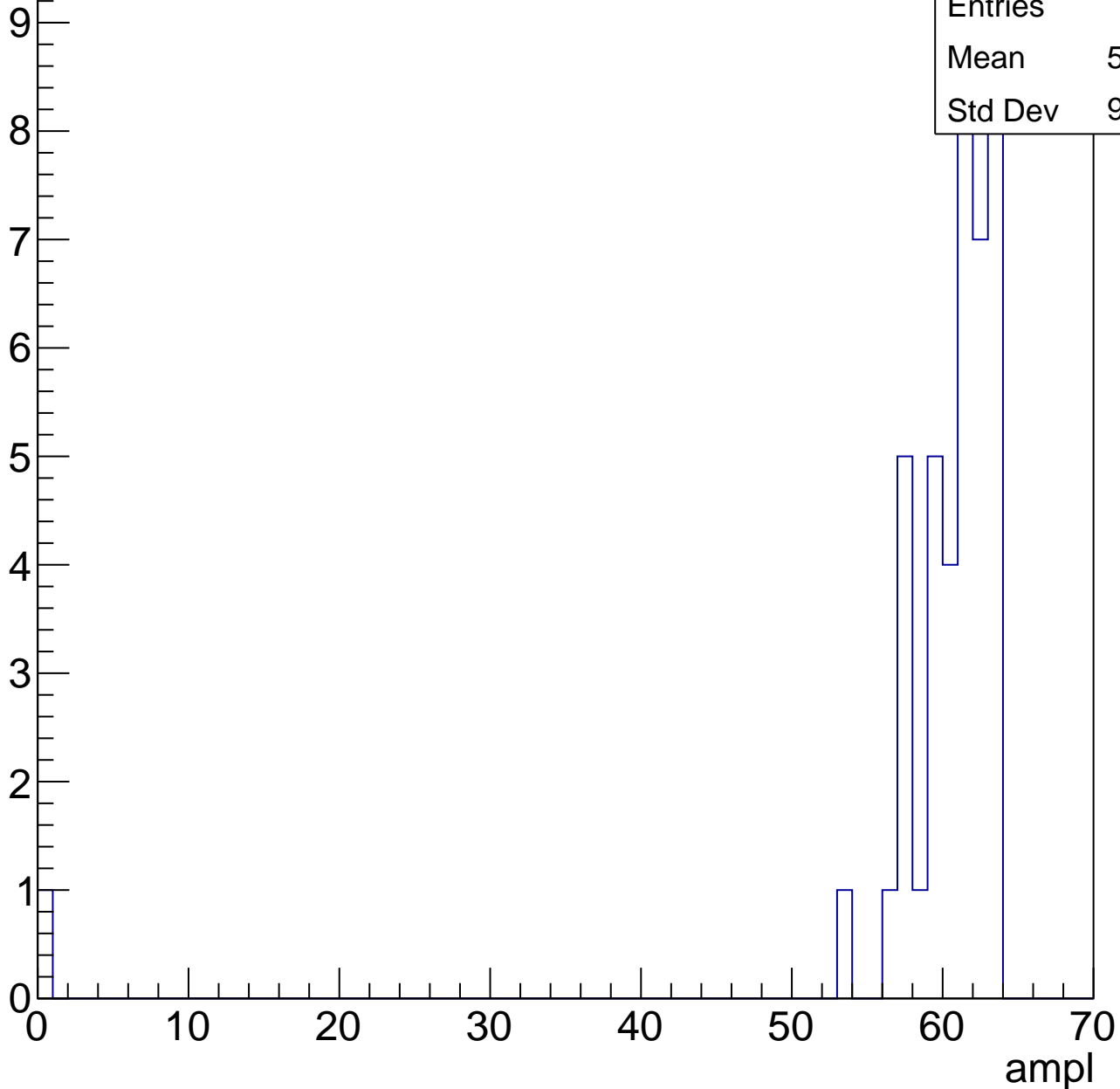


# B1L003S, U3-ch115, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	42
Mean	58.95
Std Dev	9.499



# B1L003S, U3-ch115, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	63
Std Dev	0



# B1L003S, U3-ch115, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U3-ch116, adc0

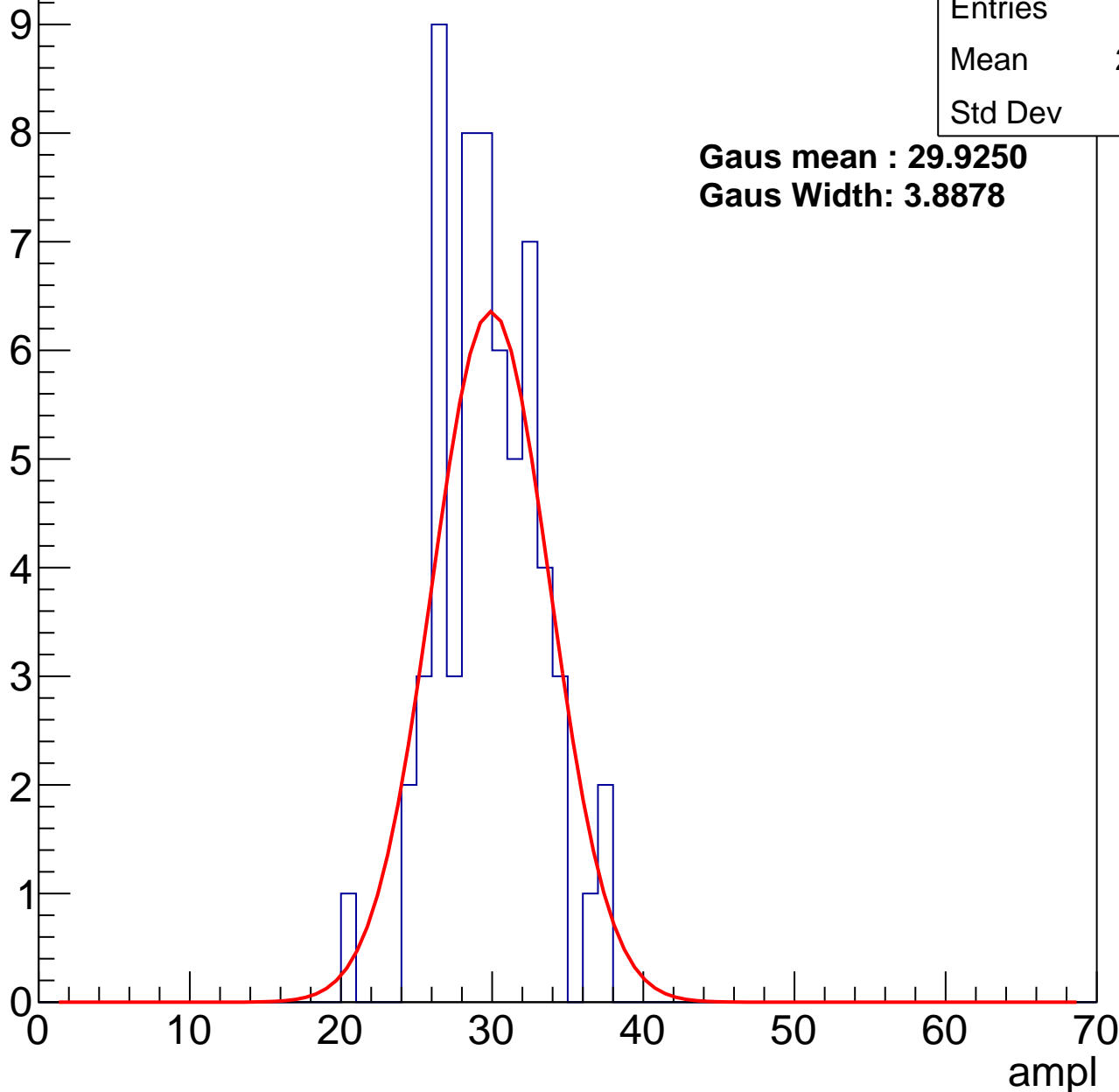
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	29.31
Std Dev	3.31

**Gaus mean : 29.9250**

**Gaus Width: 3.8878**



# B1L003S, U3-ch116, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	64
Mean	35.23
Std Dev	3.22

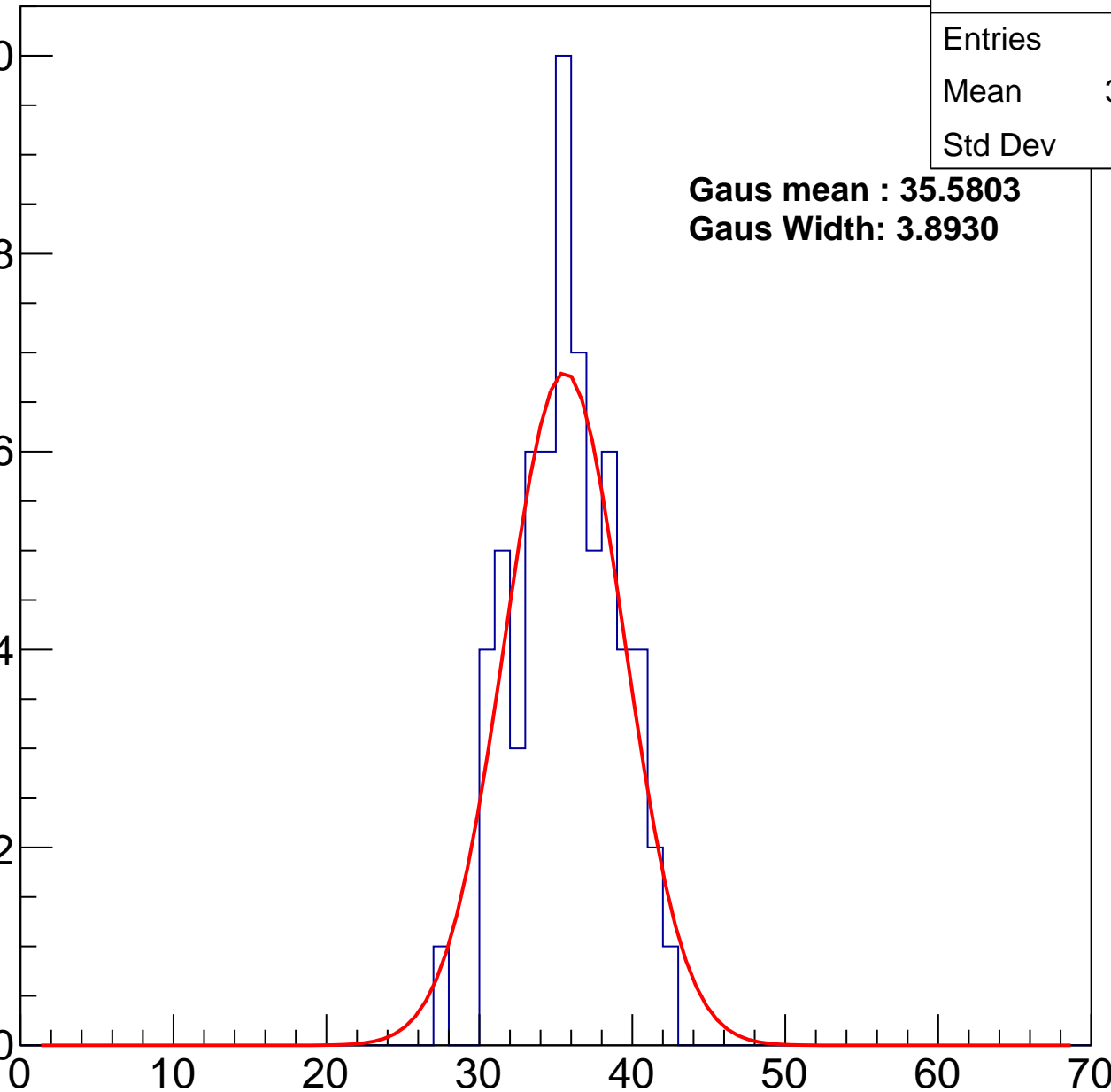
**Gaus mean : 35.5803**

**Gaus Width: 3.8930**

Entry

10  
8  
6  
4  
2  
0

ampl



# B1L003S, U3-ch116, adc2

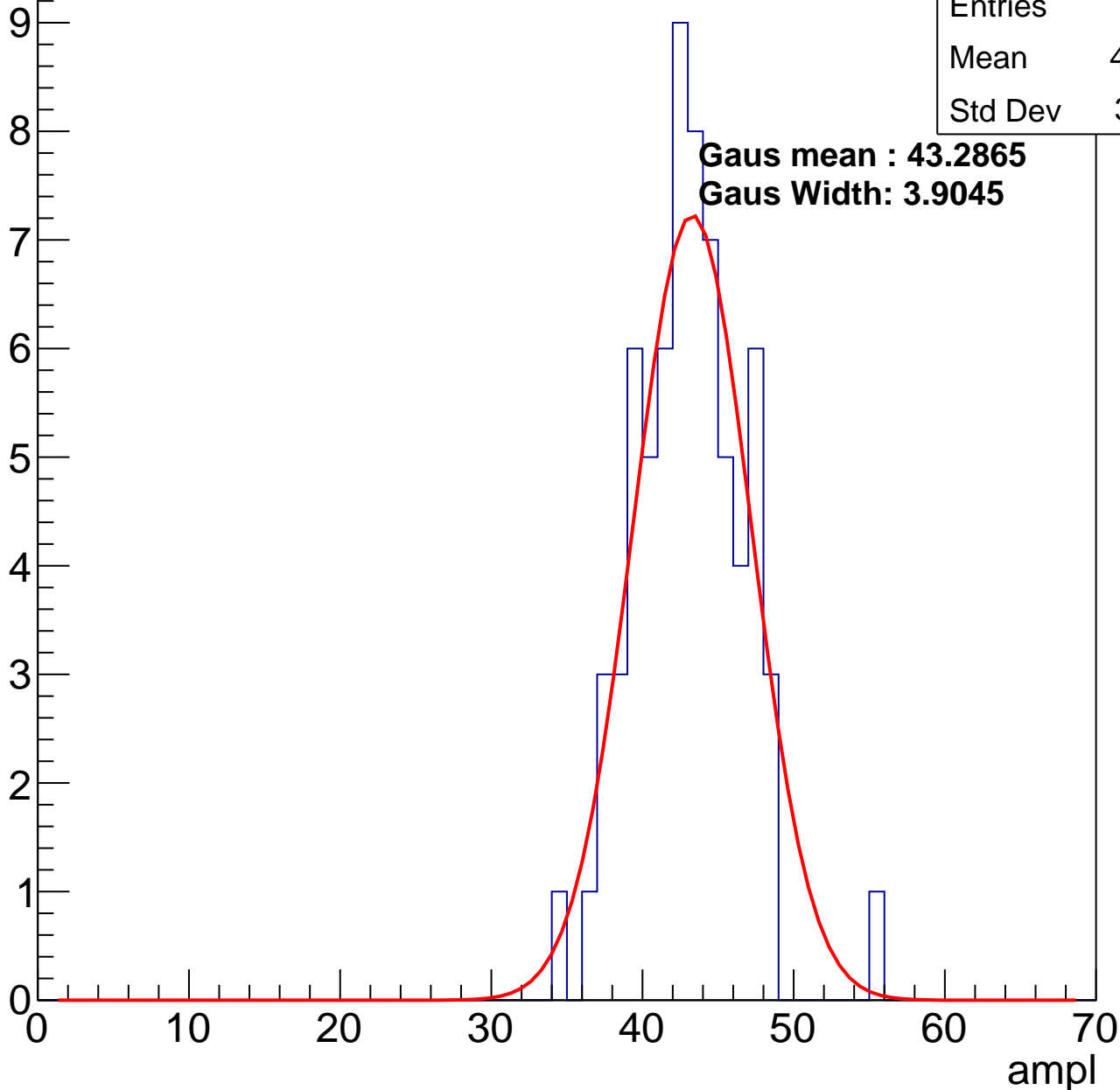
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	42.57
Std Dev	3.541

**Gaus mean : 43.2865**

**Gaus Width: 3.9045**

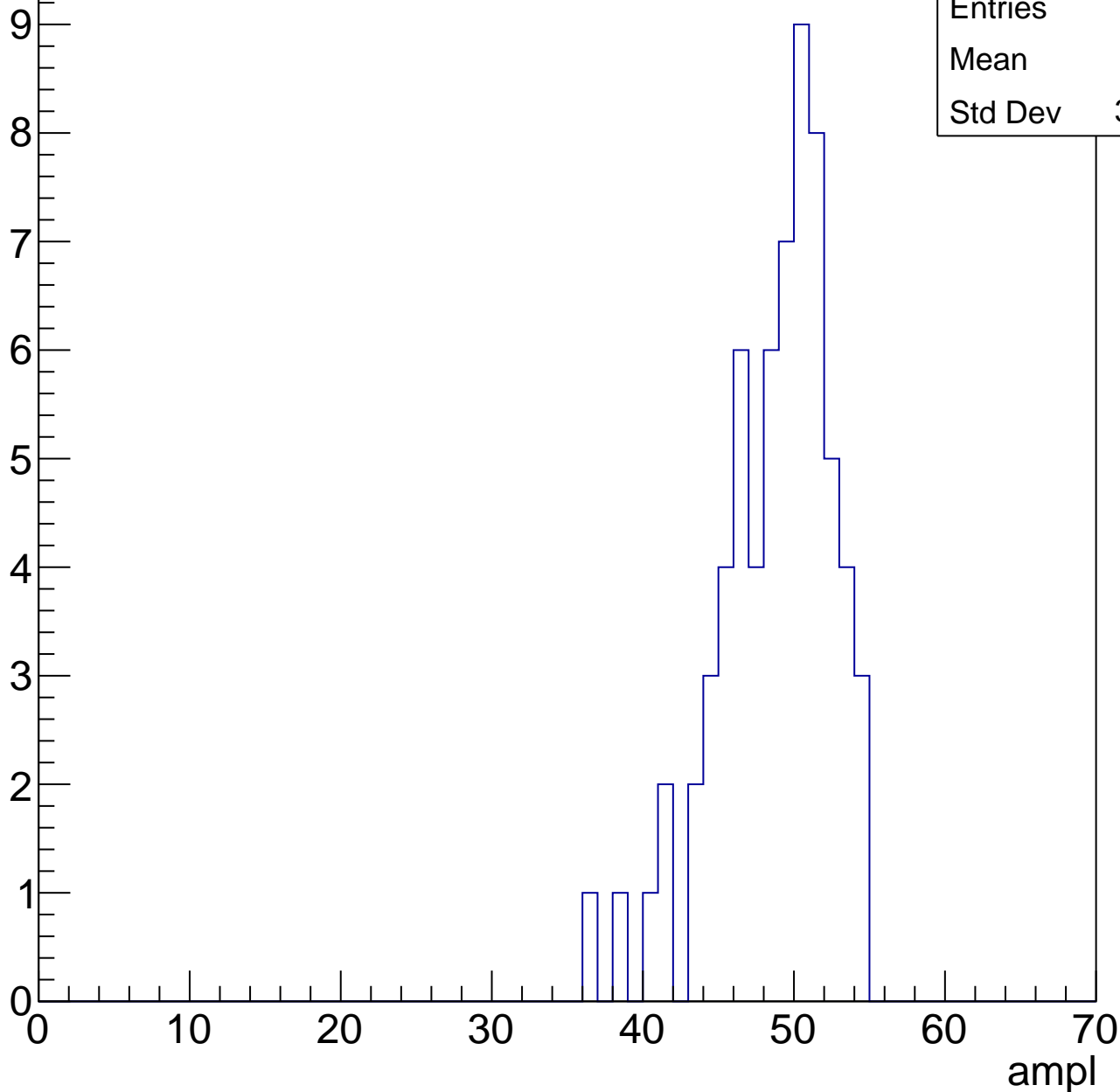


# B1L003S, U3-ch116, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	48.2
Std Dev	3.831

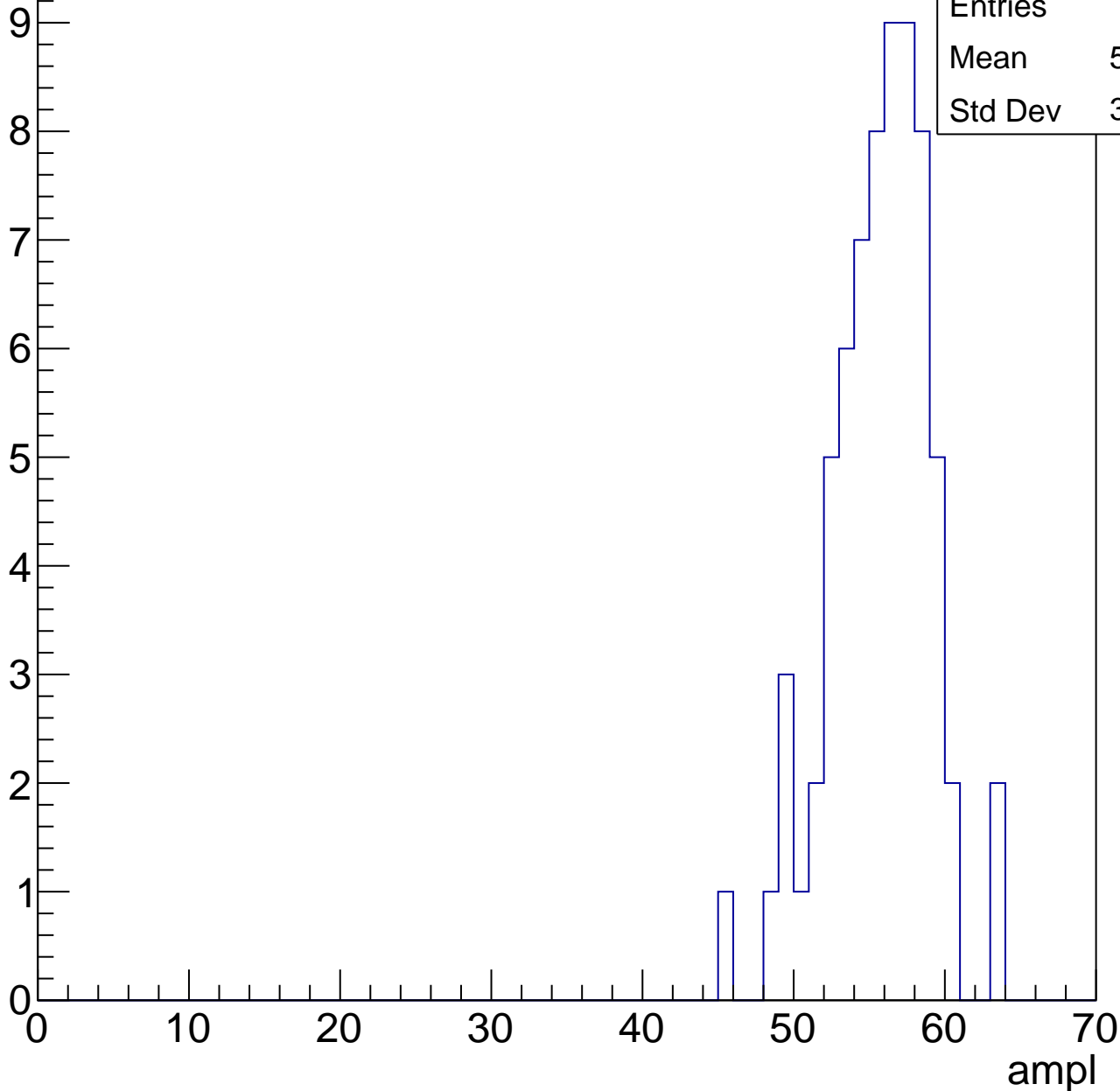


# B1L003S, U3-ch116, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	55.22
Std Dev	3.323

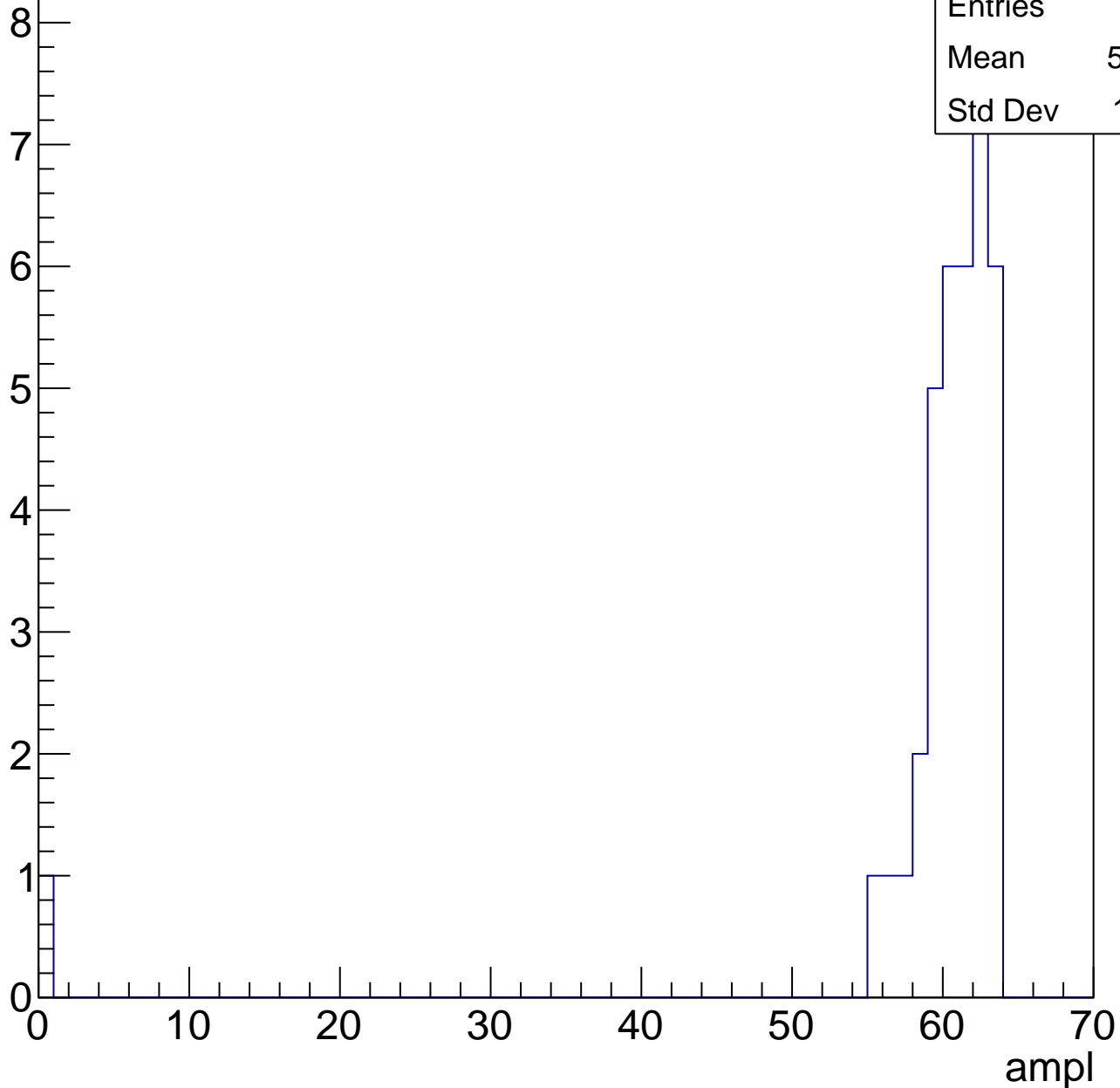


# B1L003S, U3-ch116, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

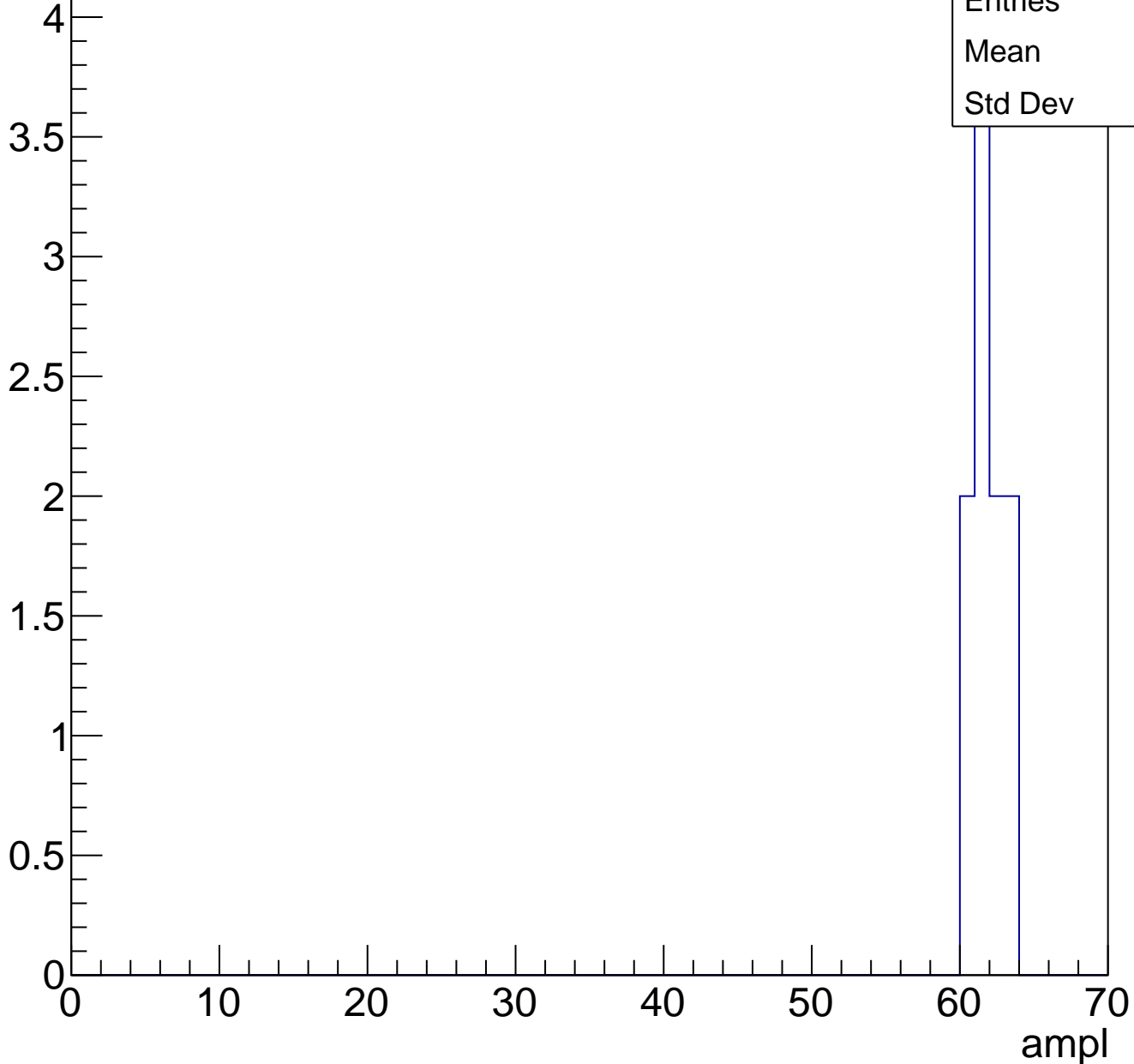
Entries	37
Mean	58.89
Std Dev	10.01



# B1L003S, U3-ch116, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



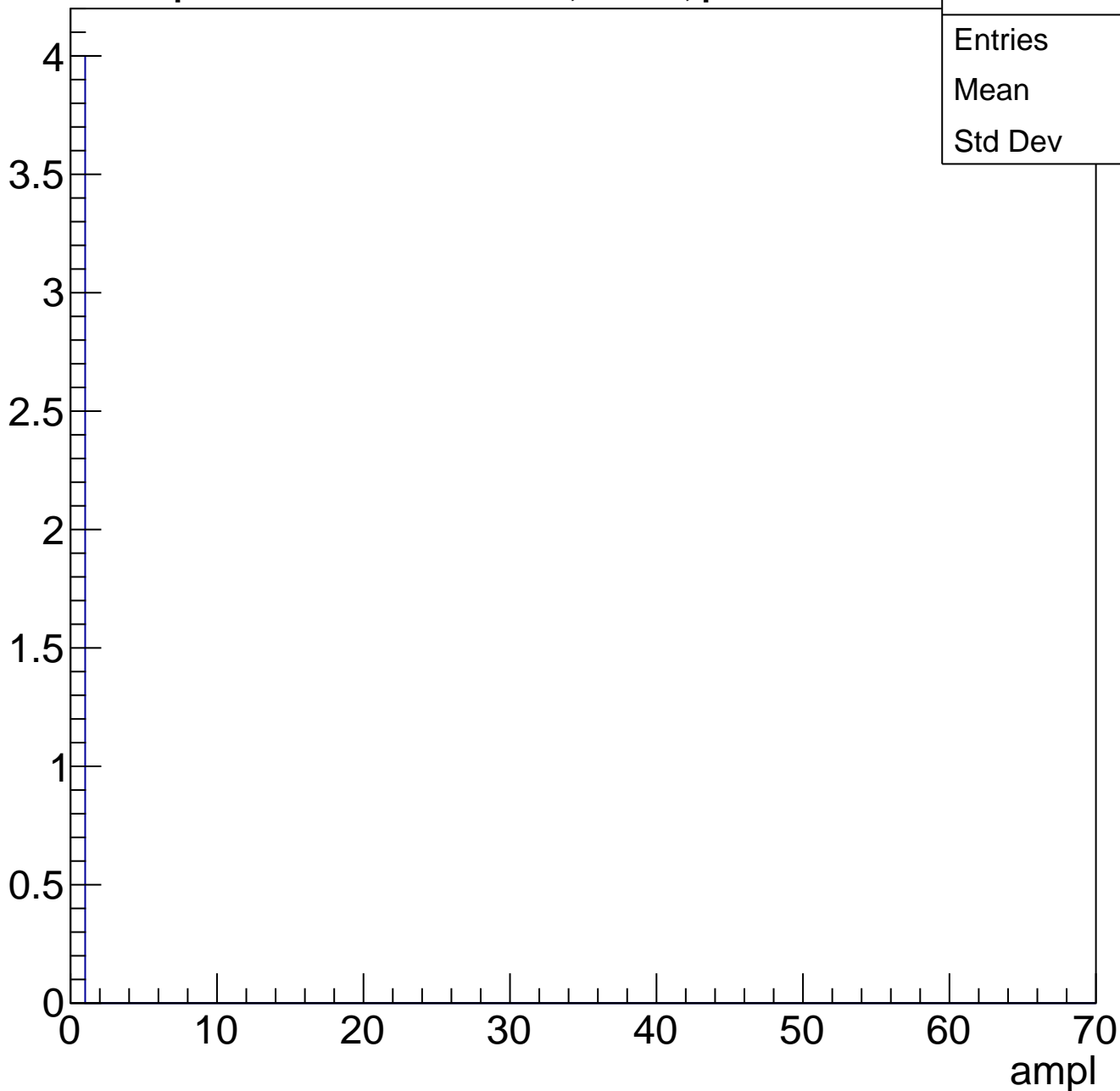
Entries	10
Mean	61.4
Std Dev	1.02



# B1L003S, U3-ch116, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	4
Mean	0
Std Dev	0

# B1L003S, U3-ch117, adc0

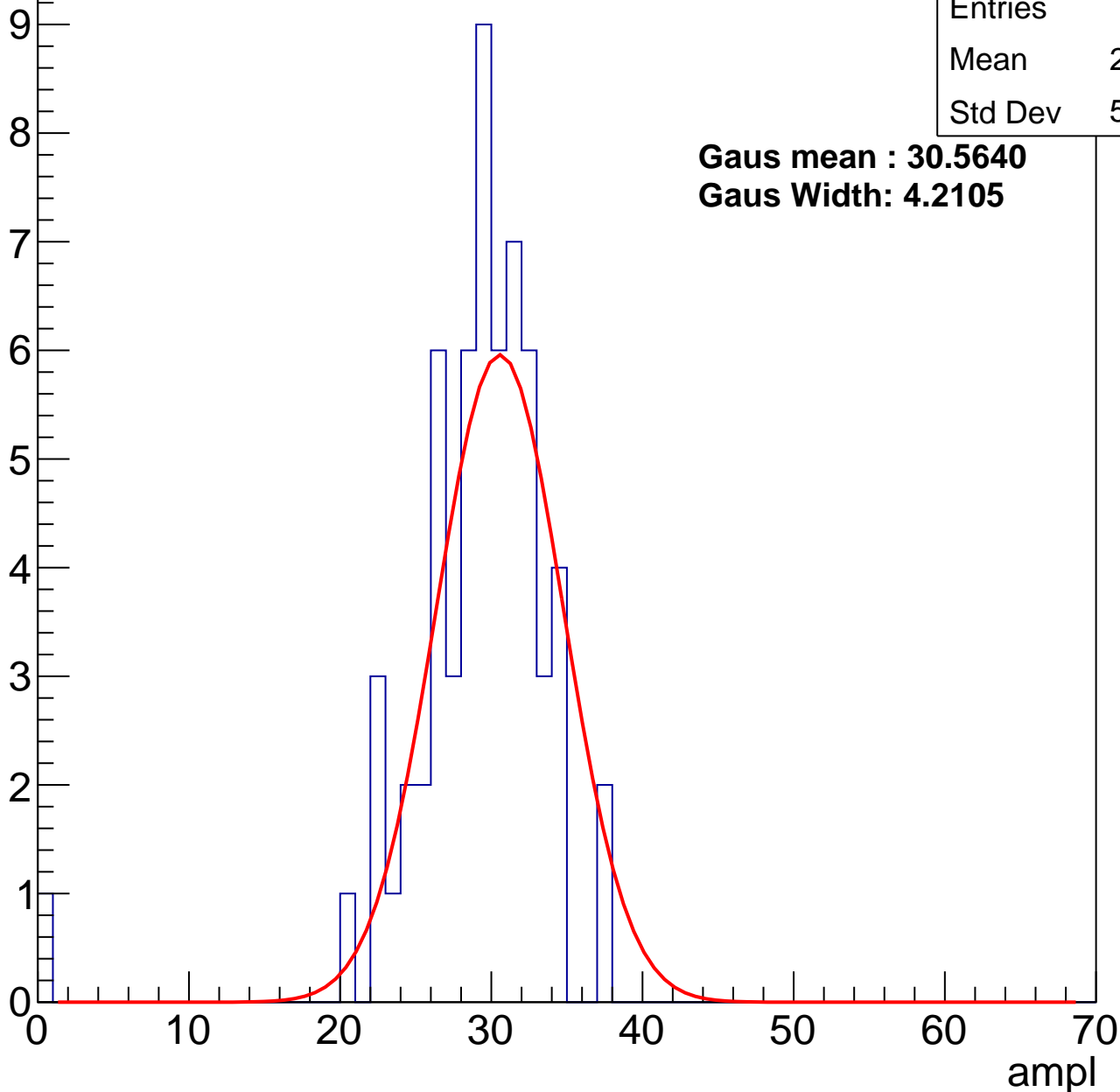
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	28.56
Std Dev	5.098

**Gaus mean : 30.5640**

**Gaus Width: 4.2105**



# B1L003S, U3-ch117, adc1

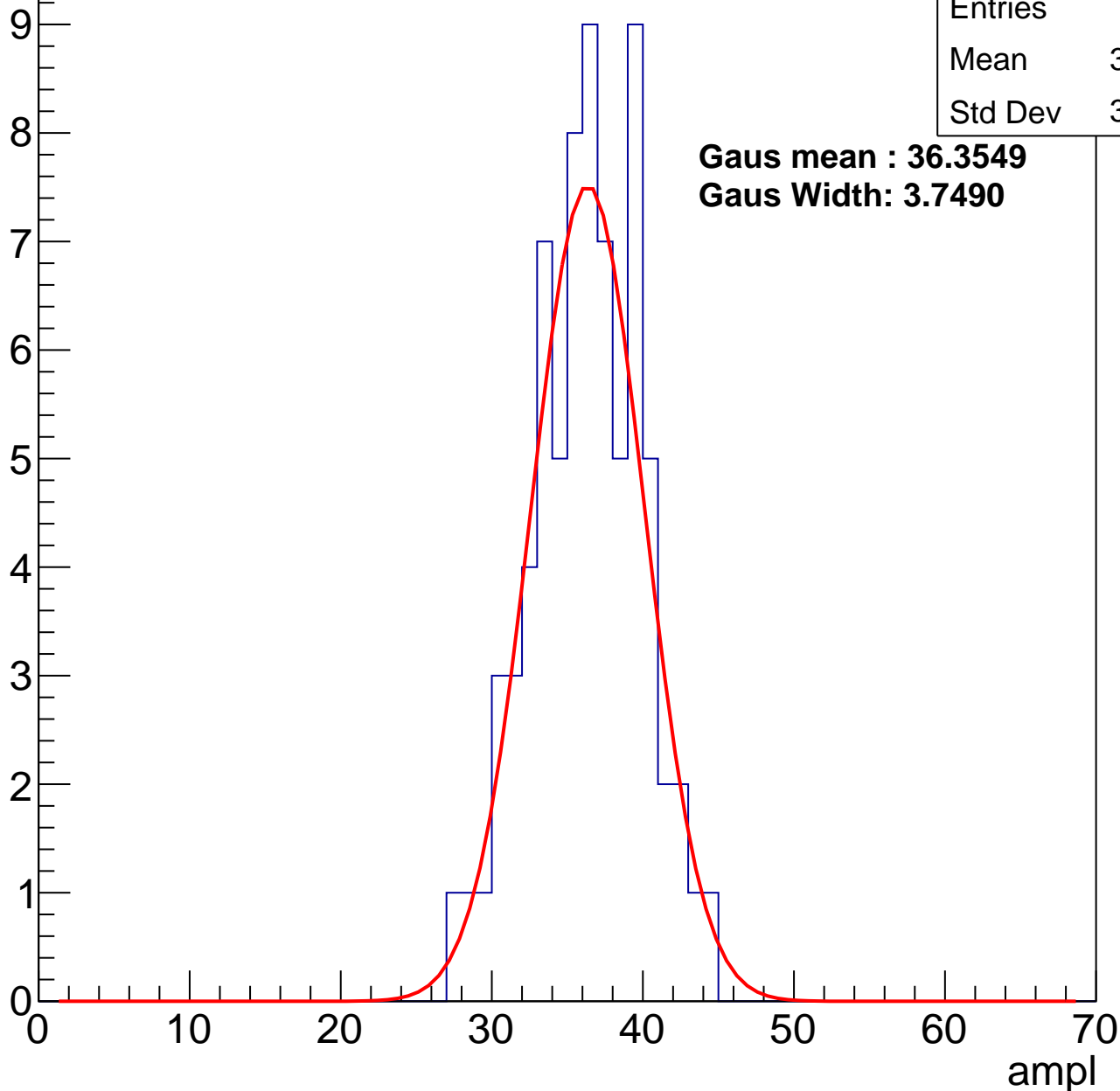
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	74
Mean	35.85
Std Dev	3.589

**Gaus mean : 36.3549**

**Gaus Width: 3.7490**



# B1L003S, U3-ch117, adc2

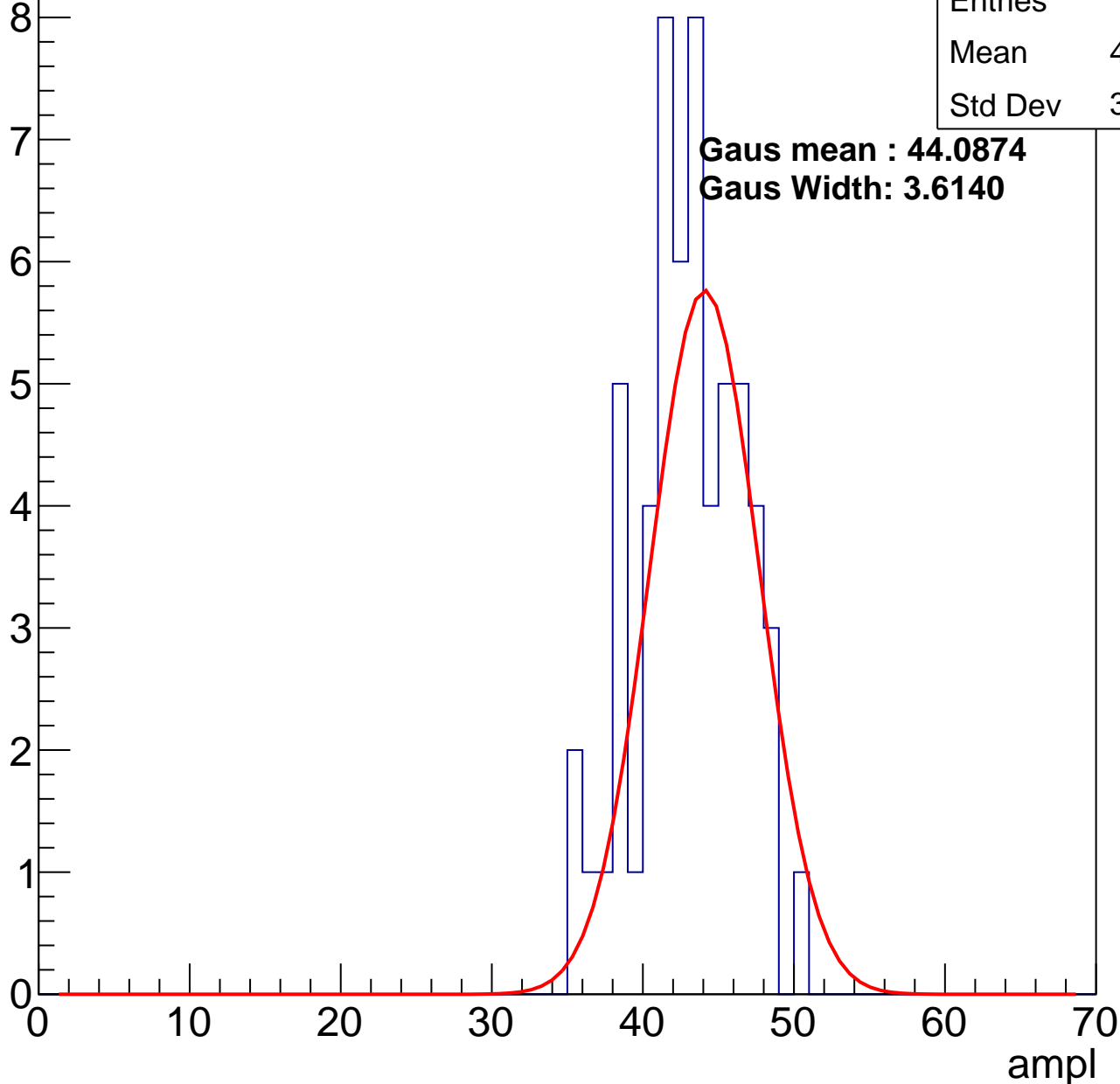
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	42.57
Std Dev	3.409

**Gaus mean : 44.0874**

**Gaus Width: 3.6140**

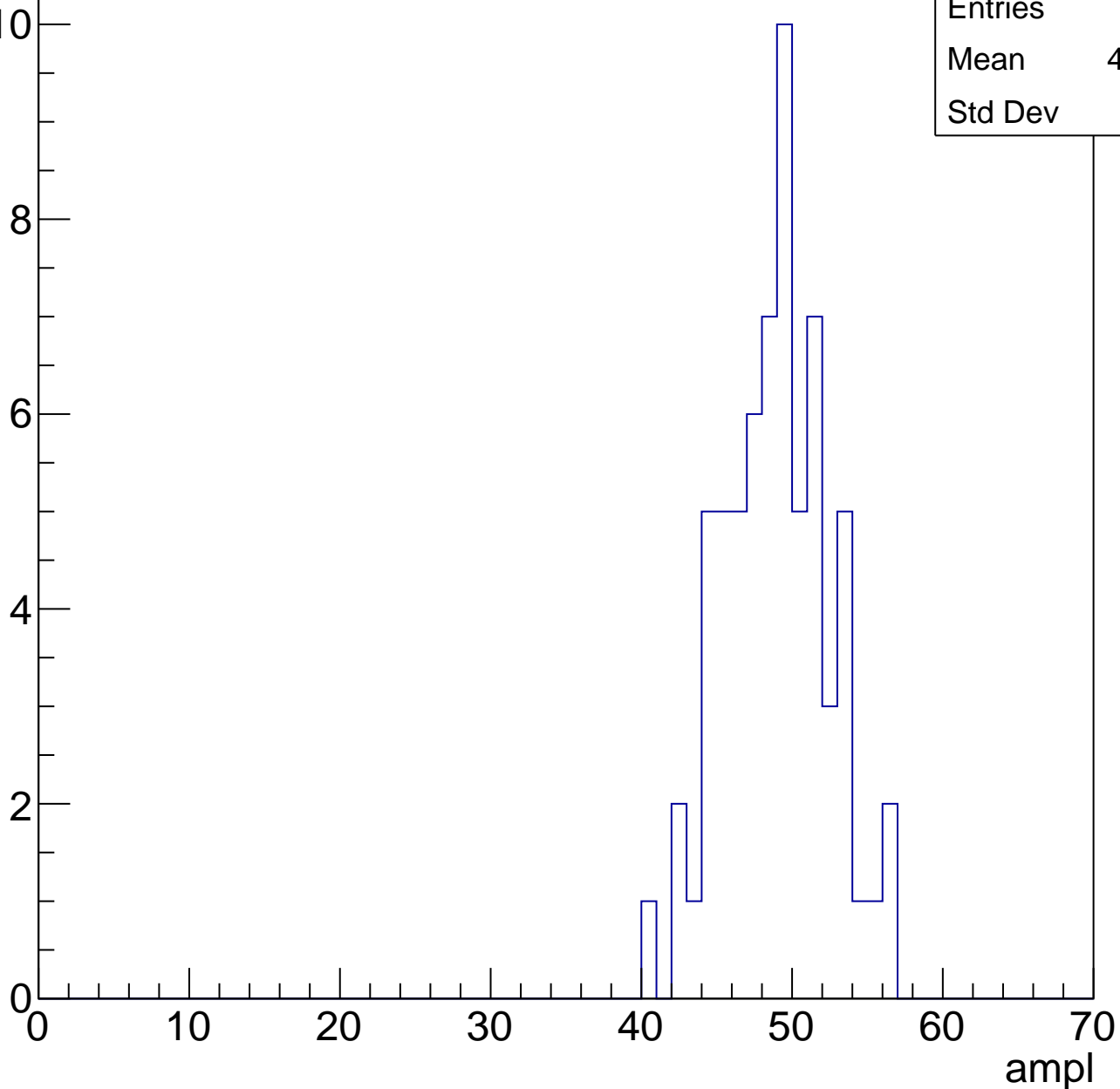


# B1L003S, U3-ch117, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	48.47
Std Dev	3.43

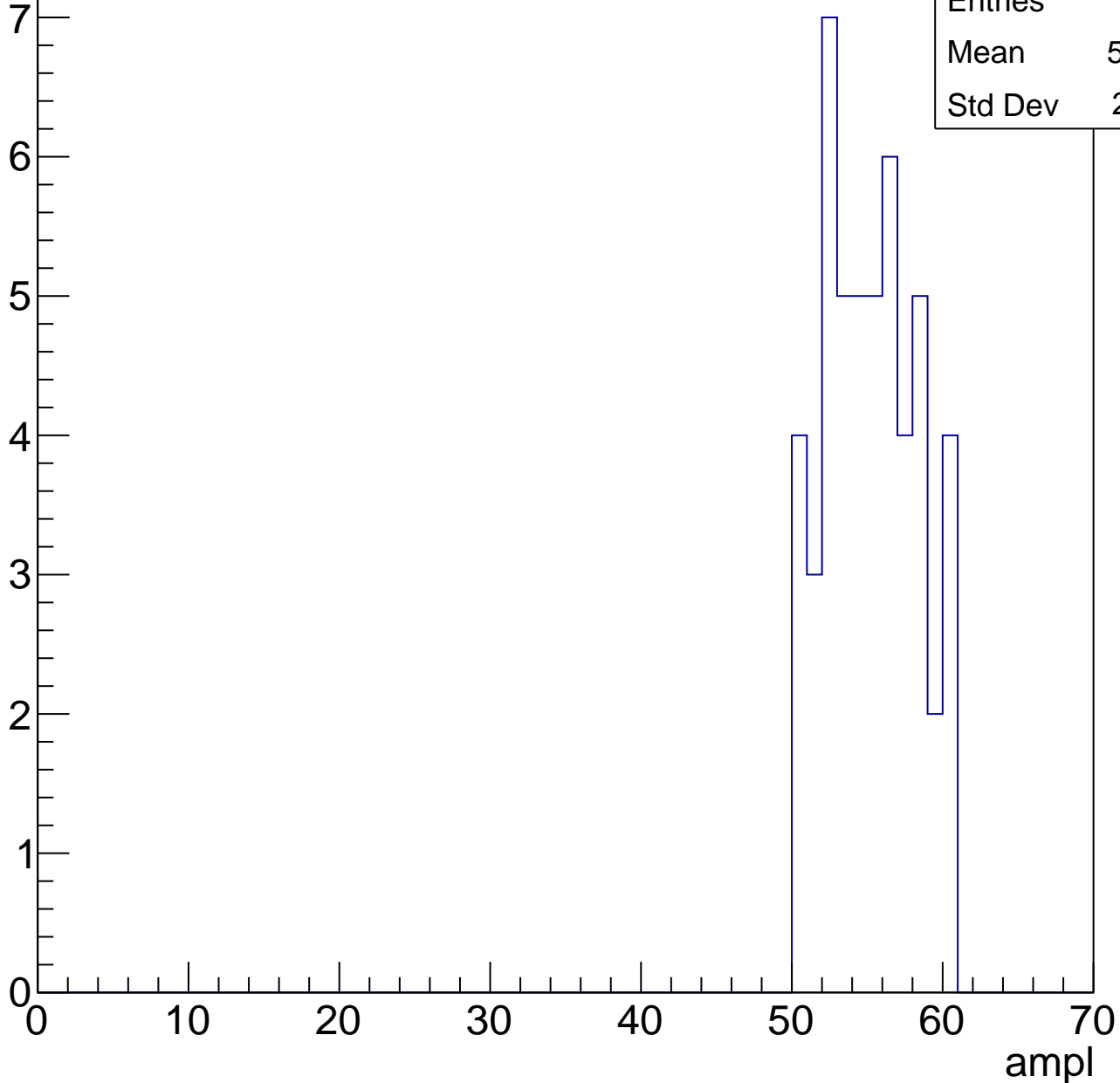


# B1L003S, U3-ch117, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	50
Mean	54.78
Std Dev	2.941



# B1L003S, U3-ch117, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	62
Mean	58.39
Std Dev	7.932

Entry

10

8

6

4

2

0

0

10

20

30

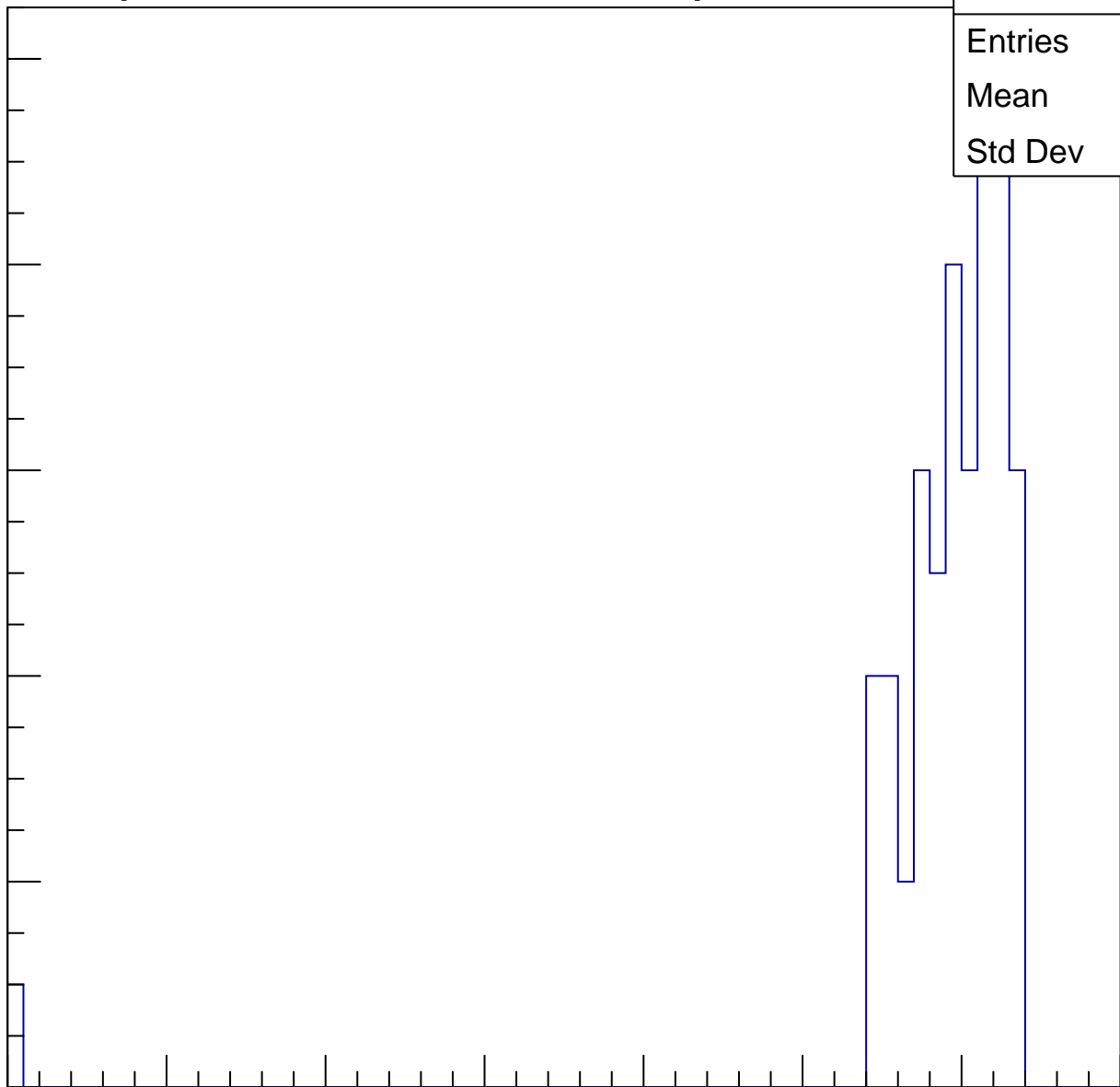
40

50

60

70

ampl



# B1L003S, U3-ch117, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

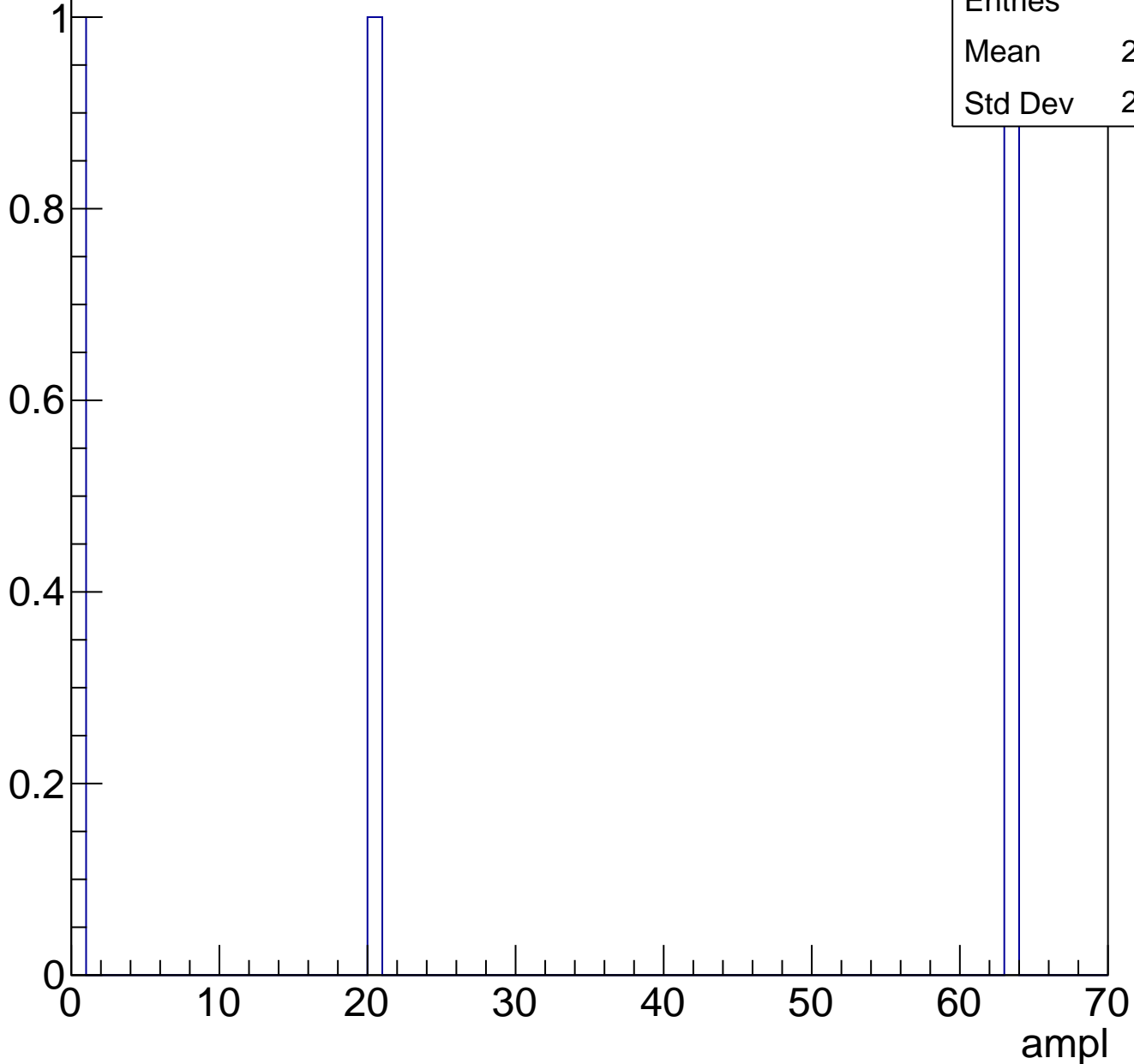




# B1L003S, U3-ch117, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	3
Mean	27.67
Std Dev	26.28

# B1L003S, U3-ch118, adc0

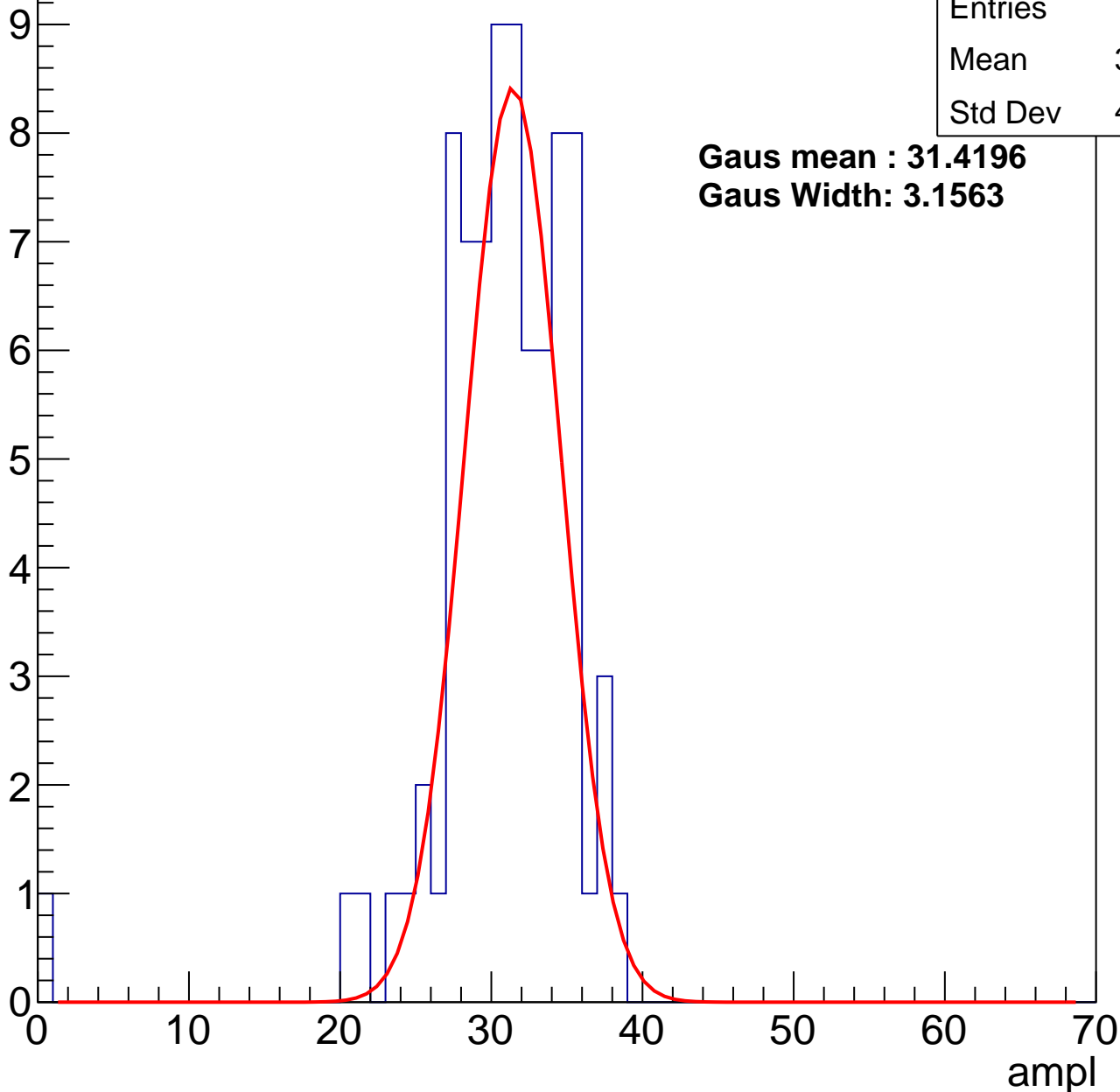
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	81
Mean	30.31
Std Dev	4.961

**Gaus mean : 31.4196**

**Gaus Width: 3.1563**



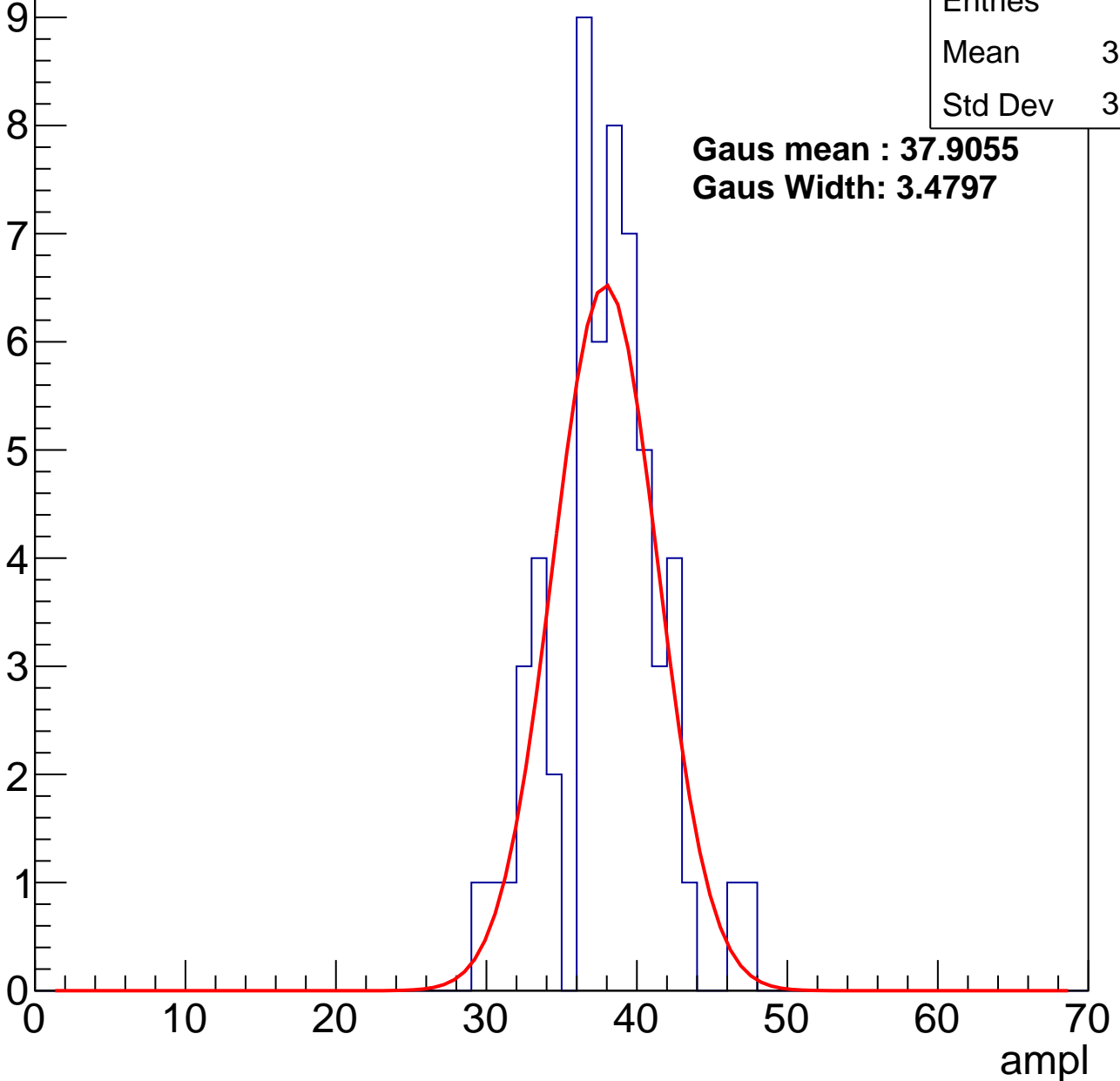
# B1L003S, U3-ch118, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	37.47
Std Dev	3.623

**Gaus mean : 37.9055**  
**Gaus Width: 3.4797**



# B1L003S, U3-ch118, adc2

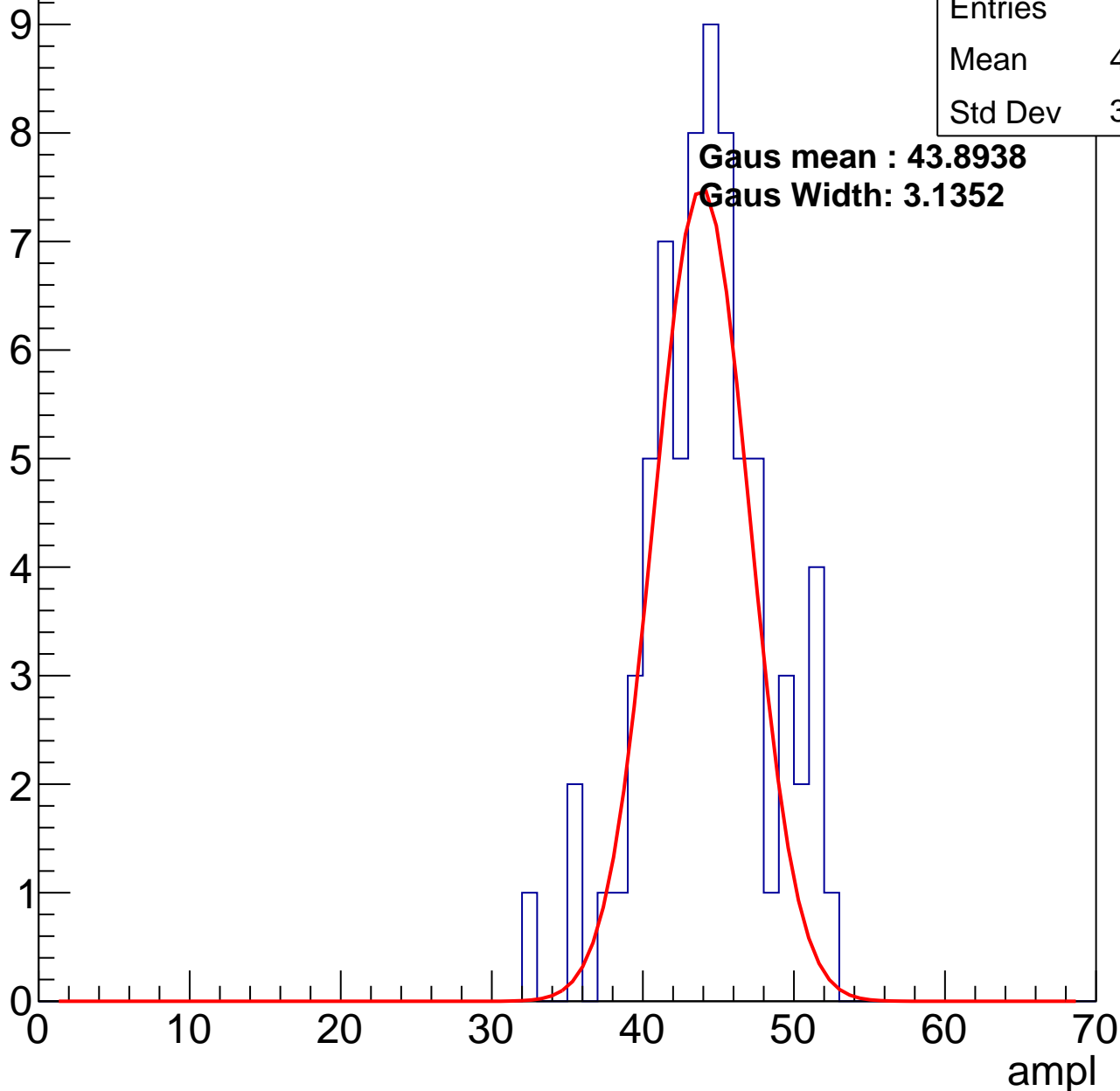
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	71
Mean	43.76
Std Dev	3.988

**Gaus mean : 43.8938**

**Gaus Width: 3.1352**

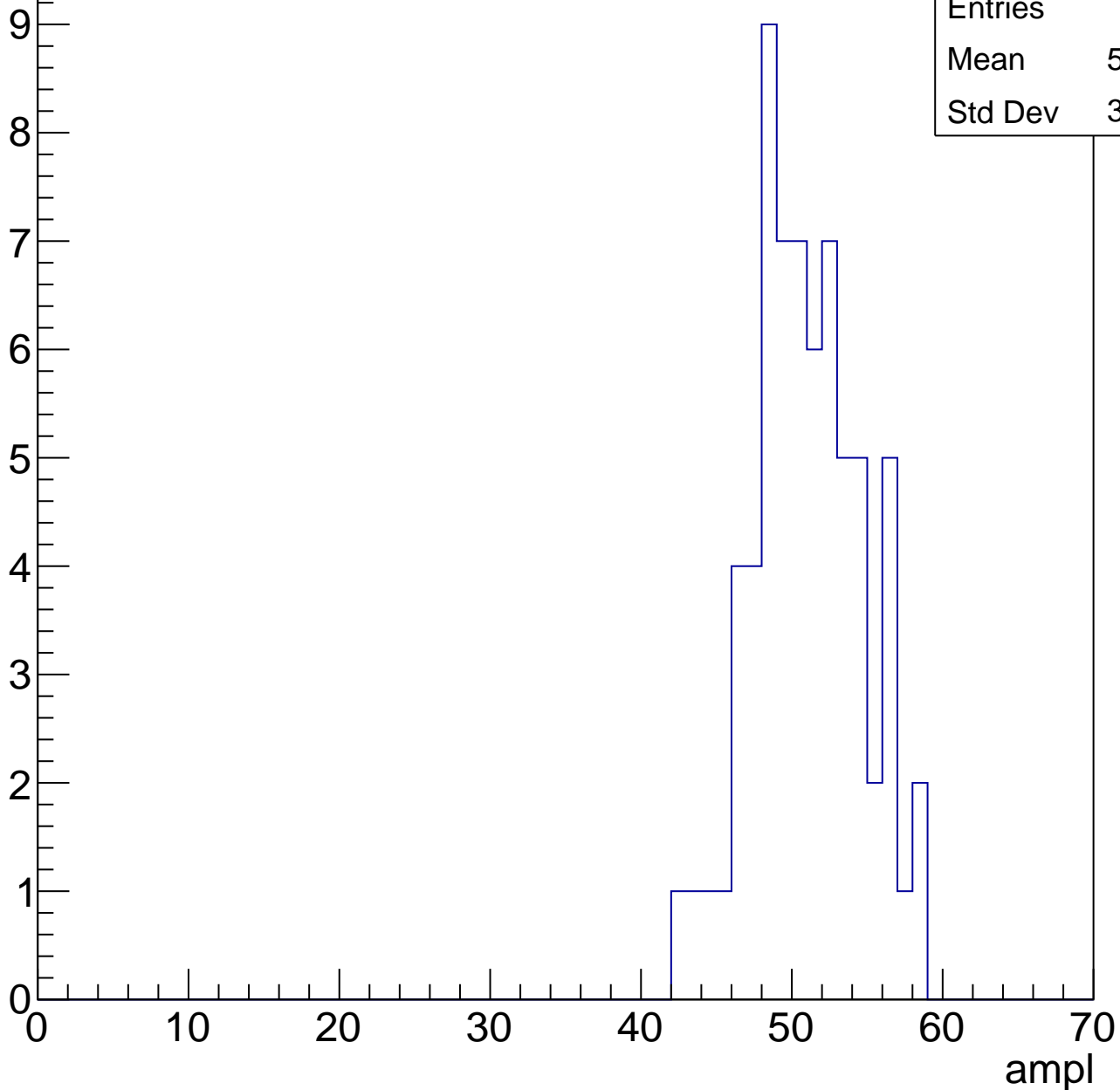


# B1L003S, U3-ch118, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	50.57
Std Dev	3.558

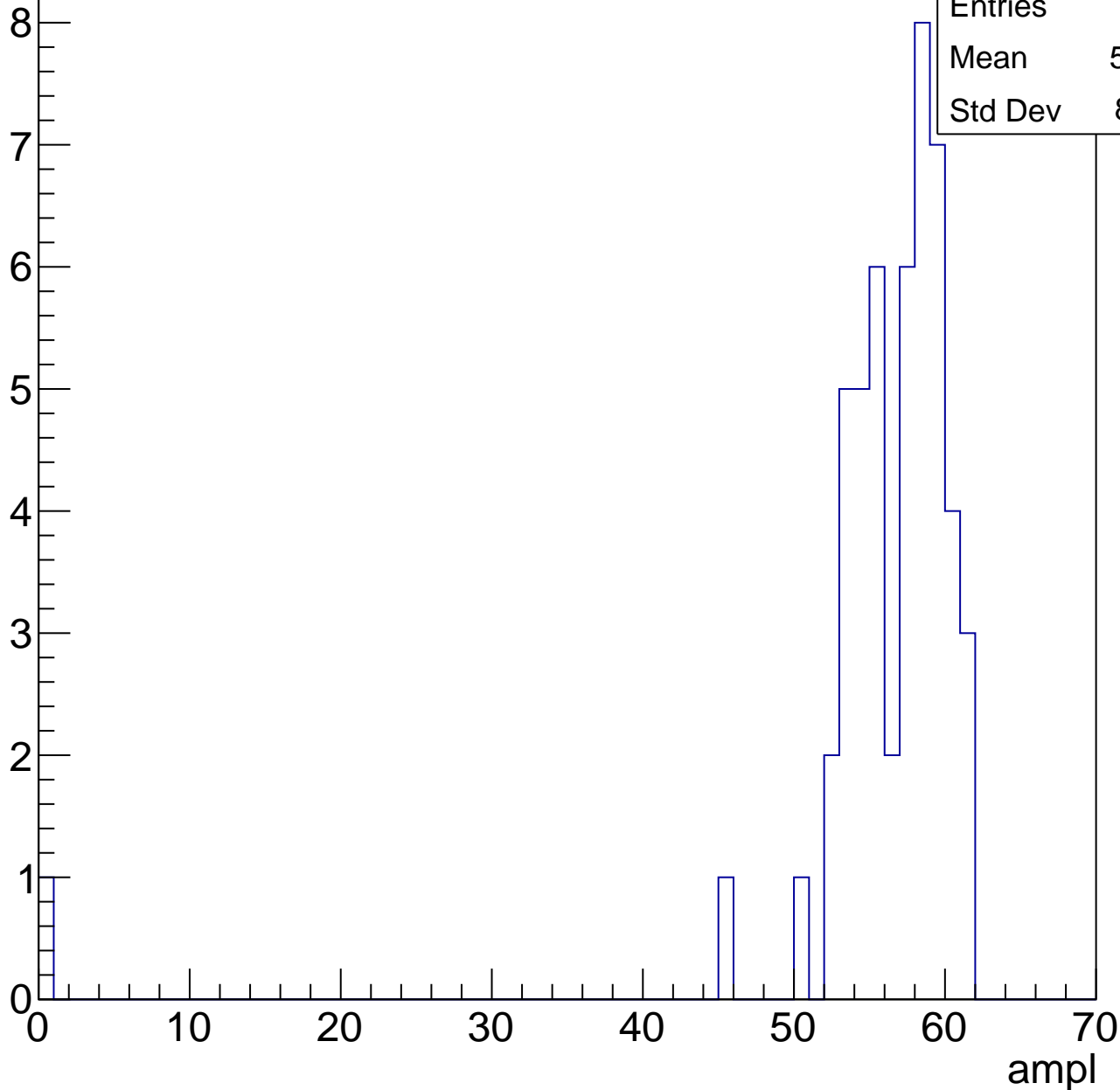


# B1L003S, U3-ch118, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	51
Mean	55.25
Std Dev	8.411

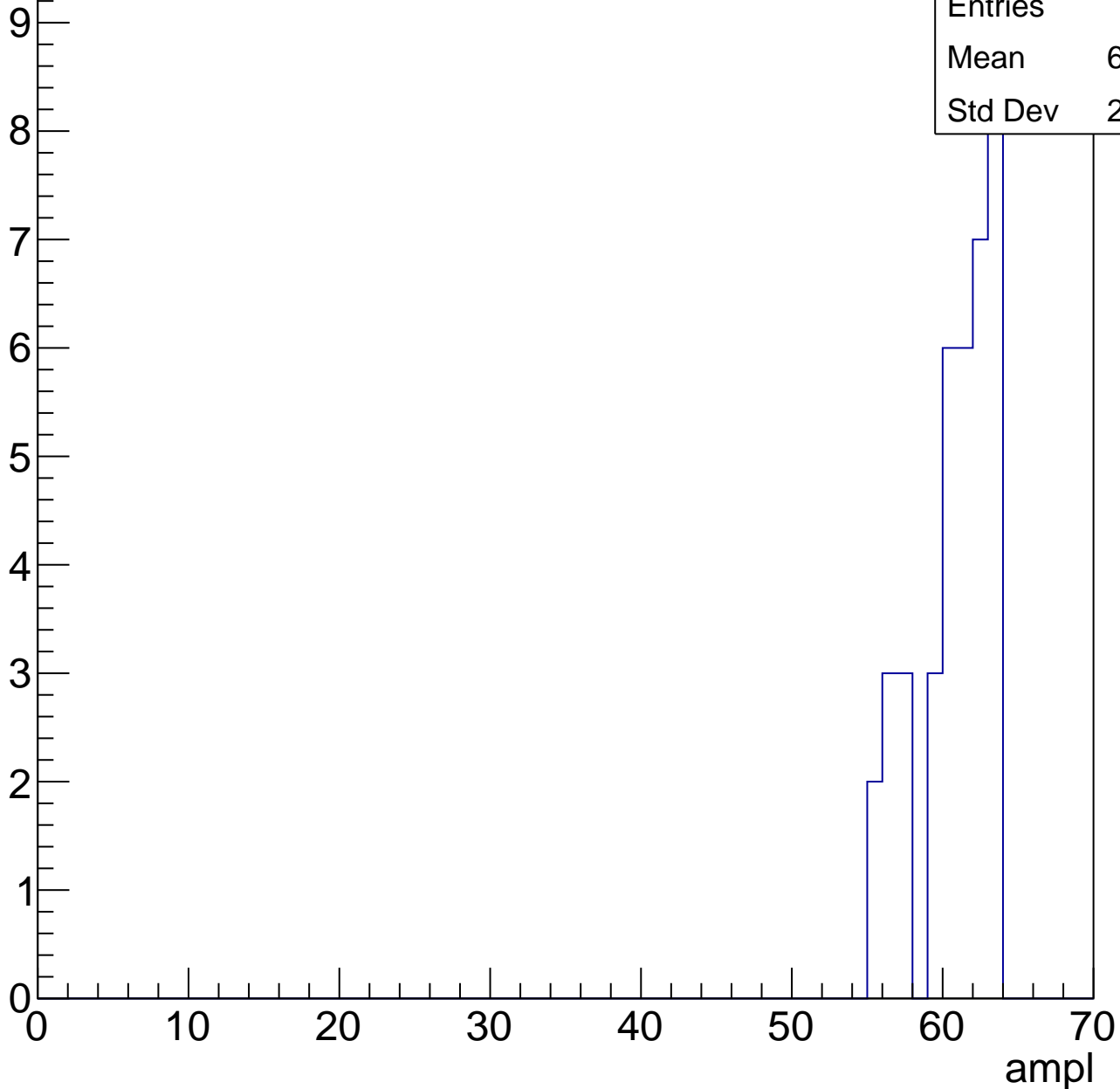


# B1L003S, U3-ch118, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	39
Mean	60.33
Std Dev	2.474



# B1L003S, U3-ch118, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch118, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U3-ch119, adc0

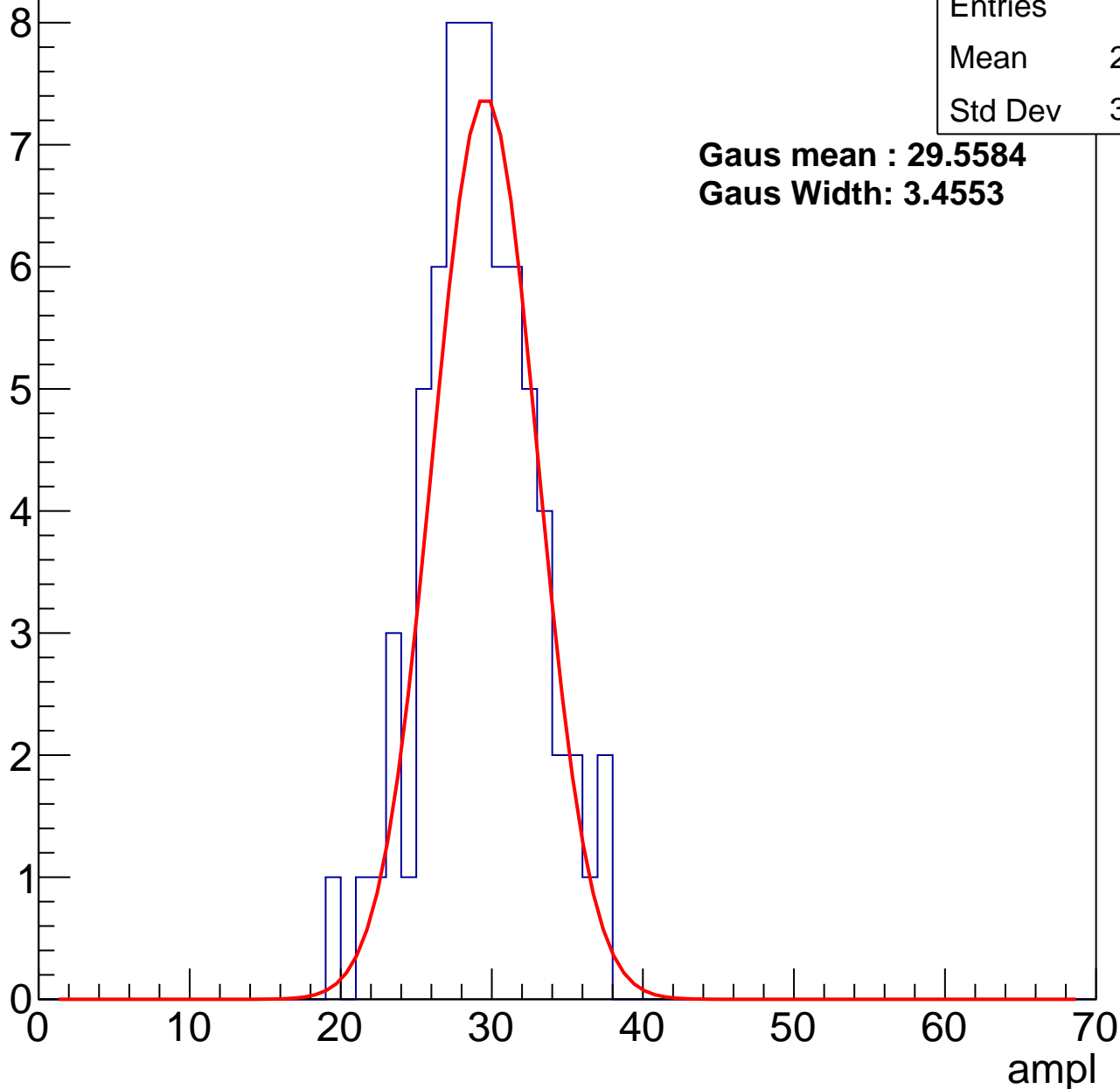
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	28.77
Std Dev	3.692

**Gaus mean : 29.5584**

**Gaus Width: 3.4553**



# B1L003S, U3-ch119, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	76
Mean	36.3
Std Dev	4.039

**Gaus mean : 36.2351**

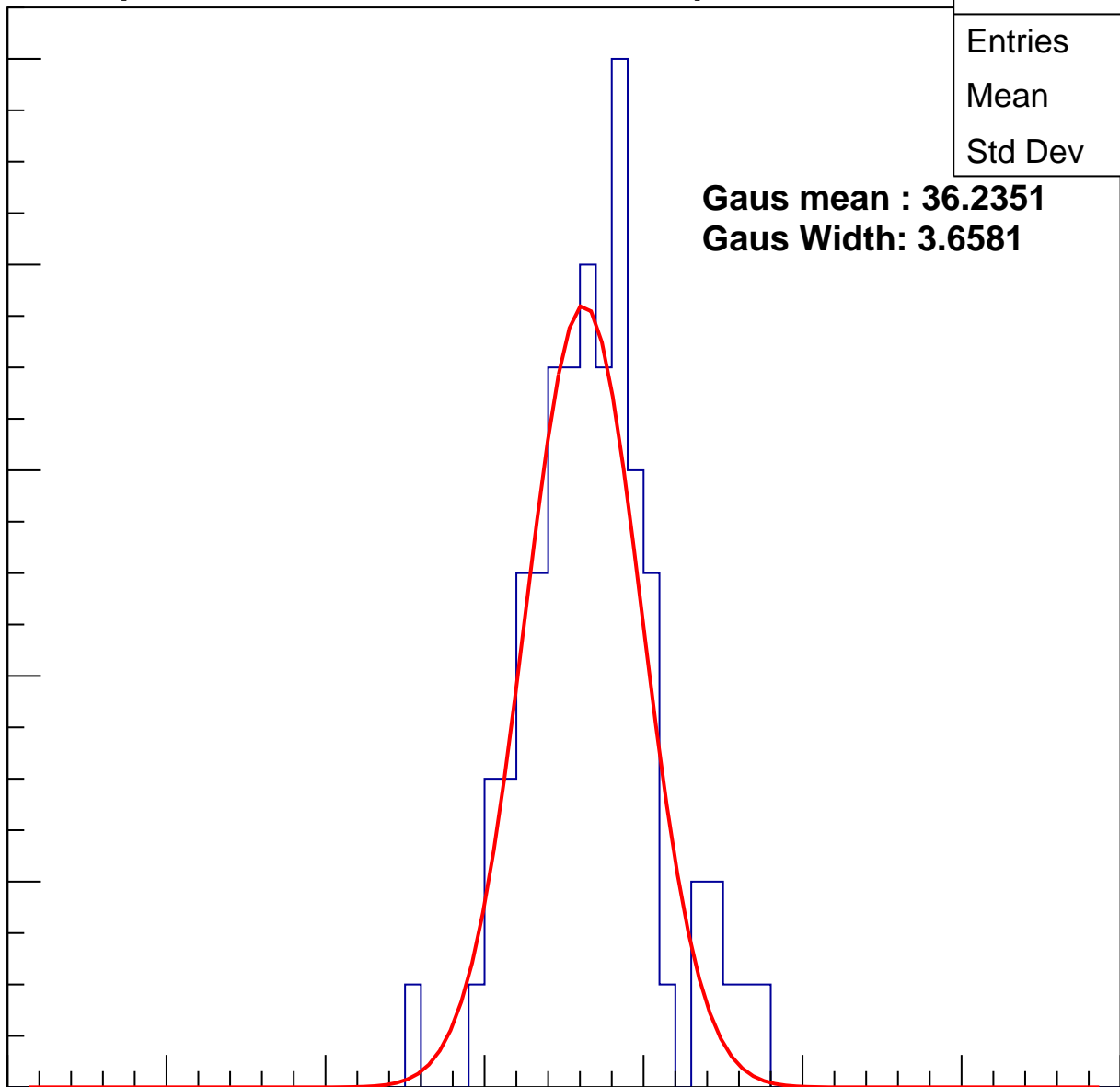
**Gaus Width: 3.6581**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L003S, U3-ch119, adc2

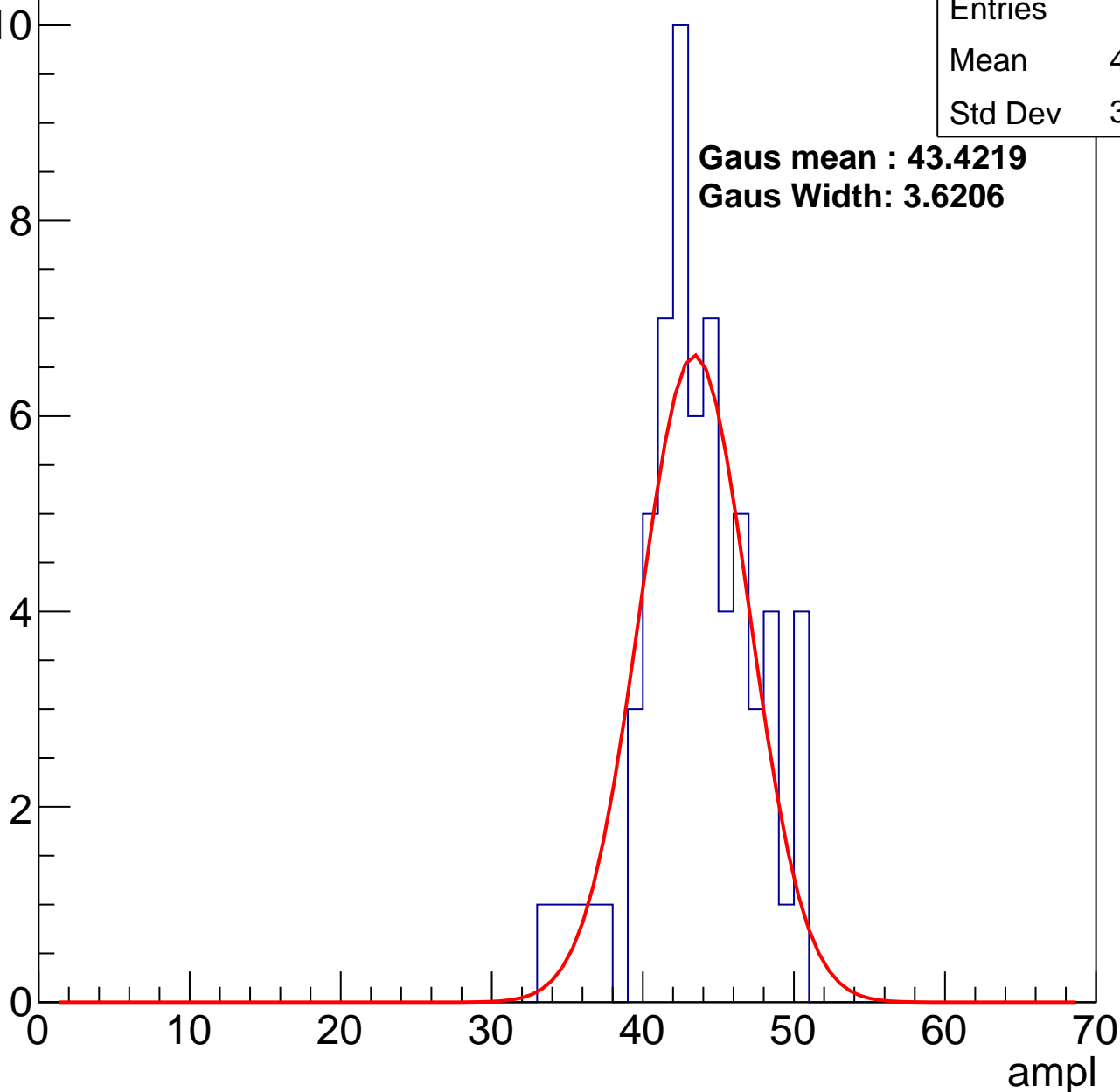
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	43.08
Std Dev	3.768

**Gaus mean : 43.4219**

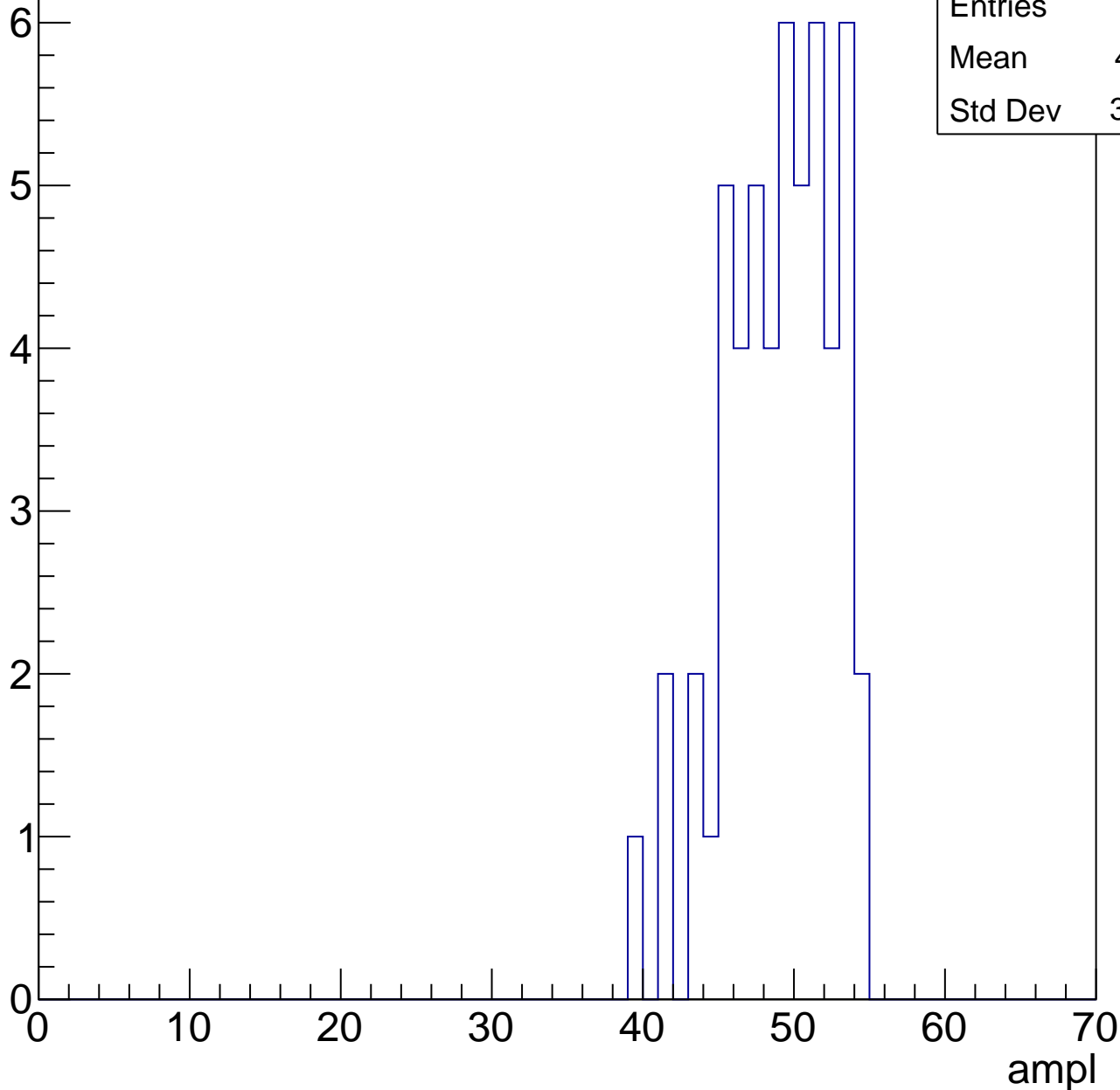
**Gaus Width: 3.6206**



# B1L003S, U3-ch119, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	53
Mean	48.51
Std Dev	3.538

# B1L003S, U3-ch119, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

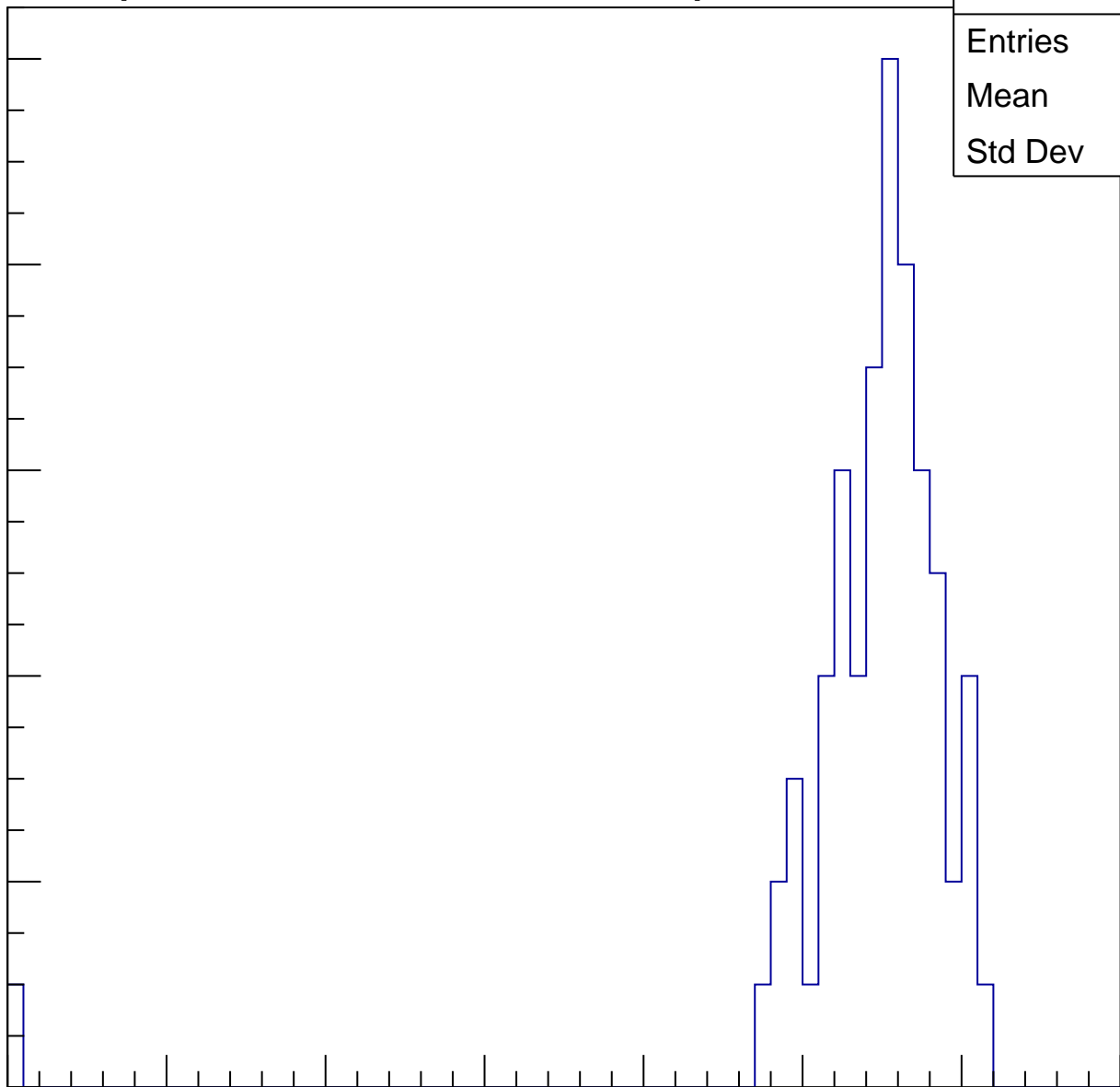
Entries	65
Mean	53.77
Std Dev	7.45

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

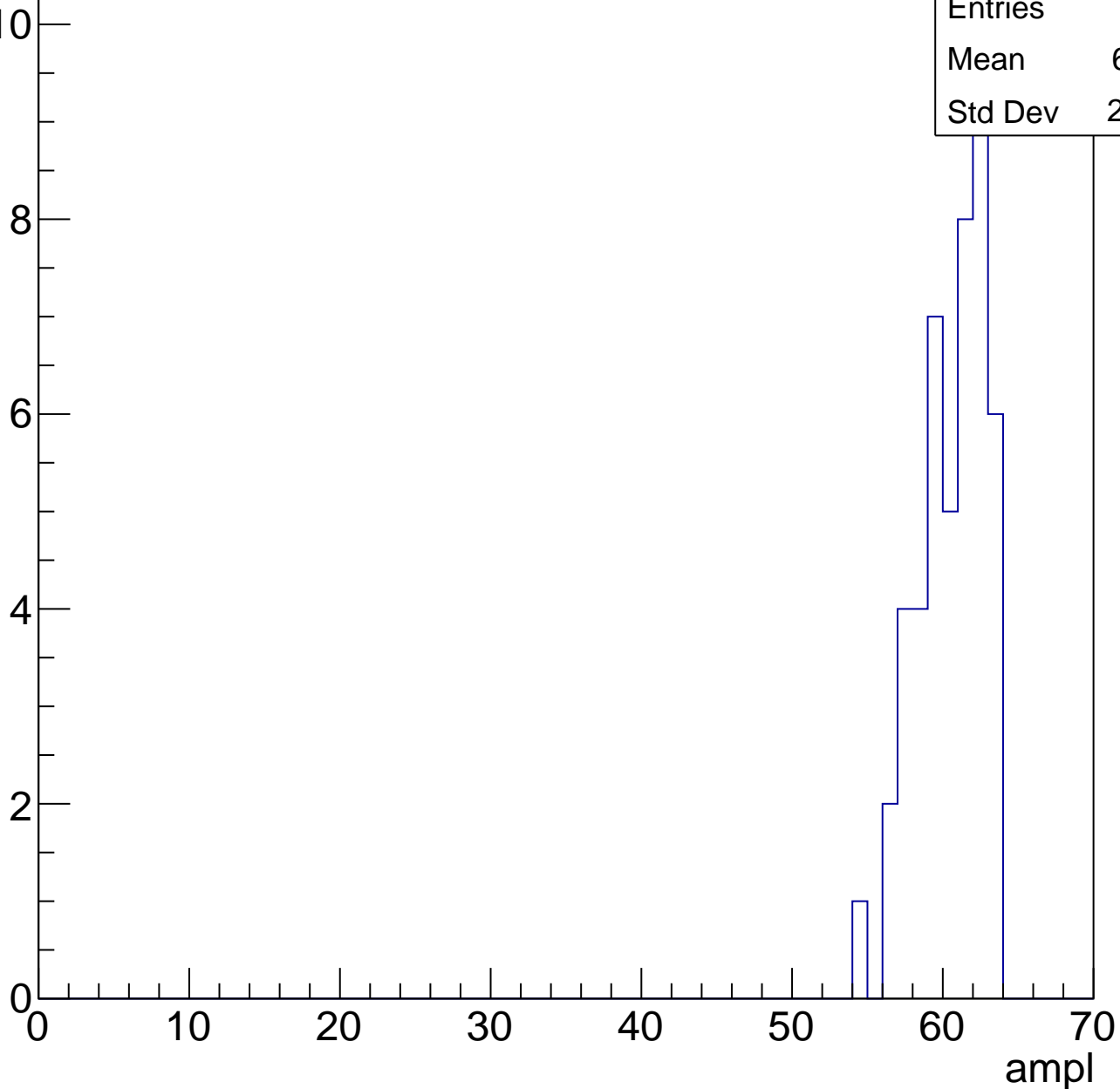


# B1L003S, U3-ch119, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

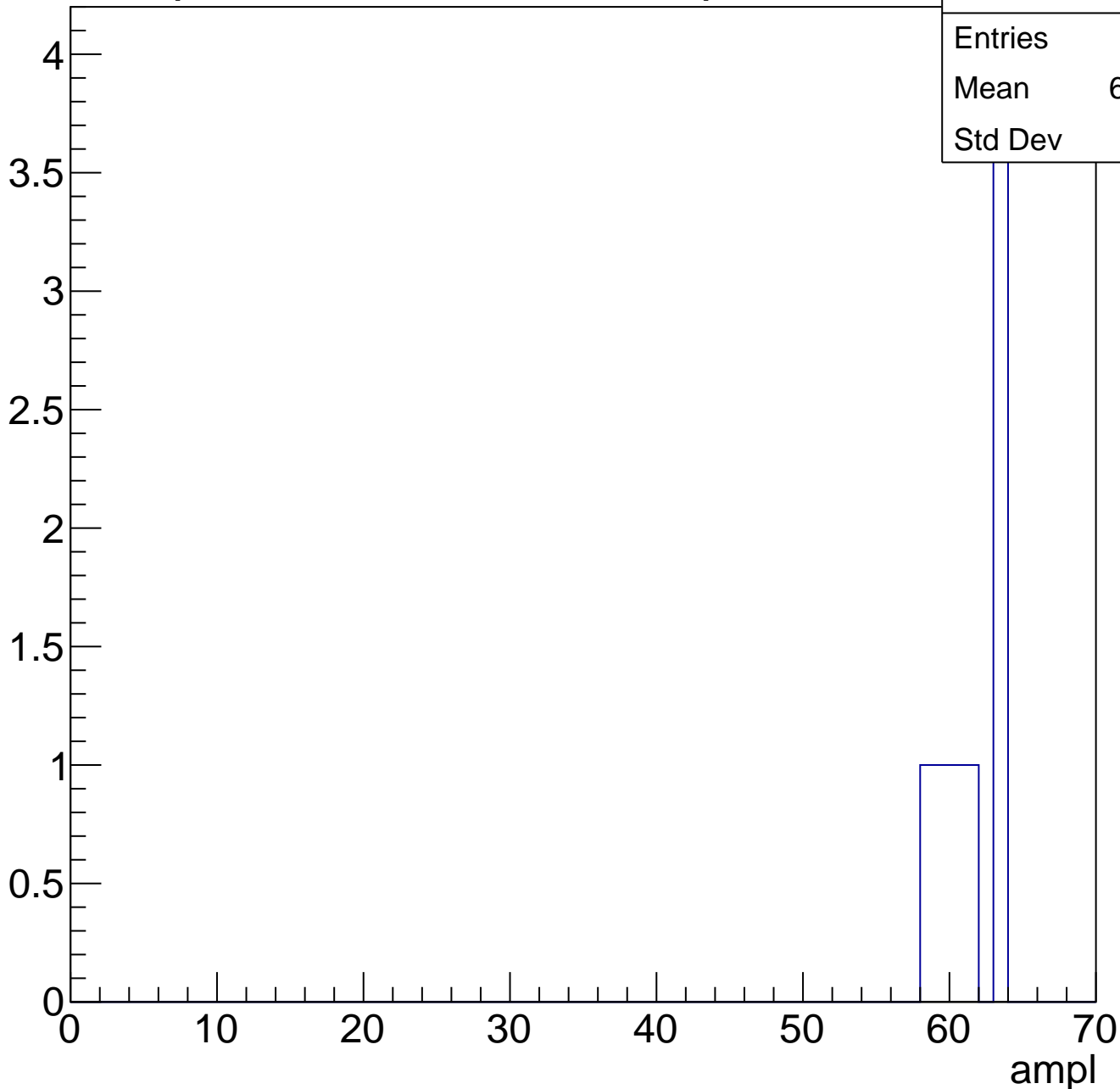
Entries	47
Mean	60.11
Std Dev	2.205



# B1L003S, U3-ch119, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch119, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U3-ch120, adc0

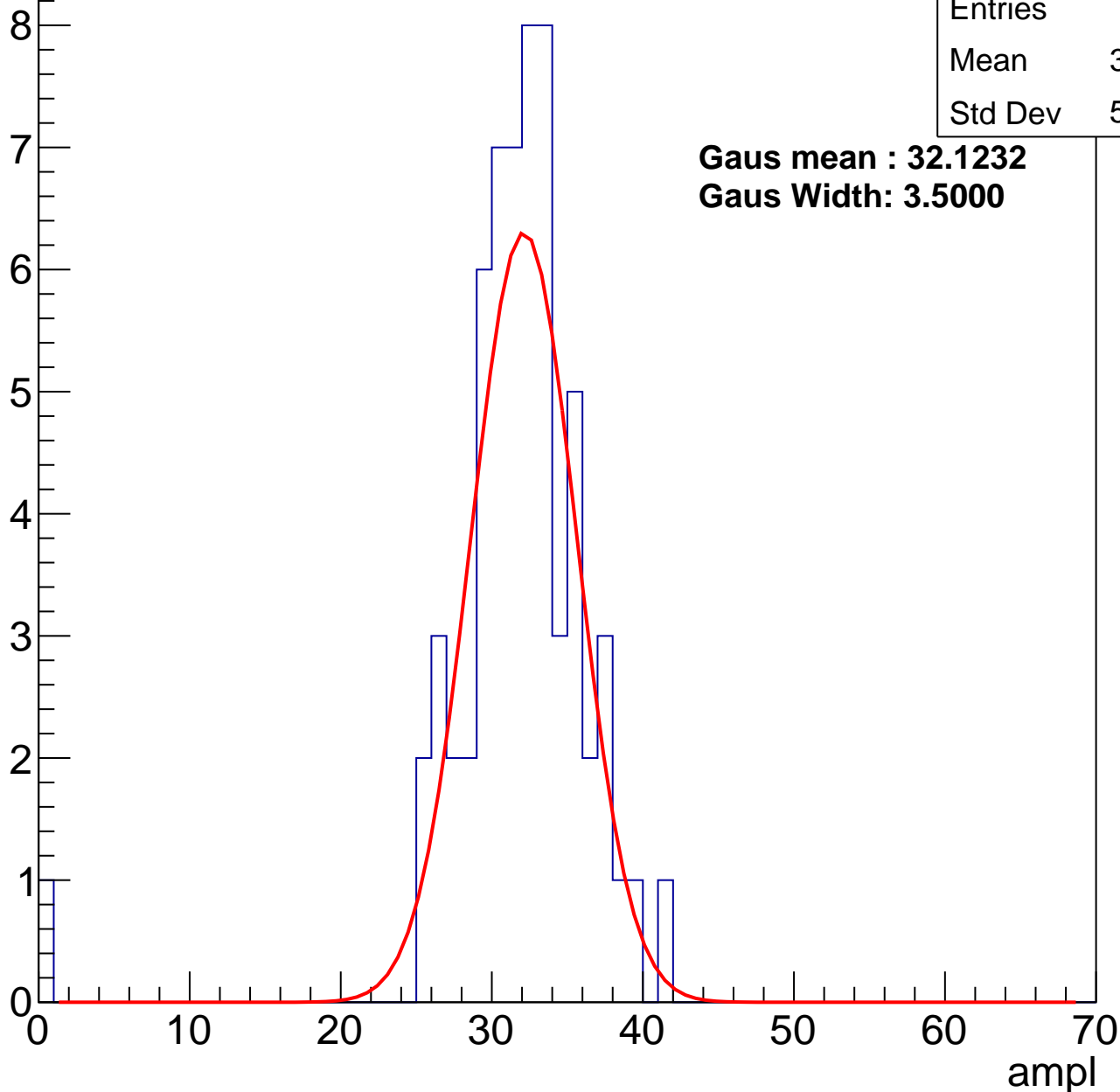
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	31.24
Std Dev	5.242

**Gaus mean : 32.1232**

**Gaus Width: 3.5000**



# B1L003S, U3-ch120, adc1

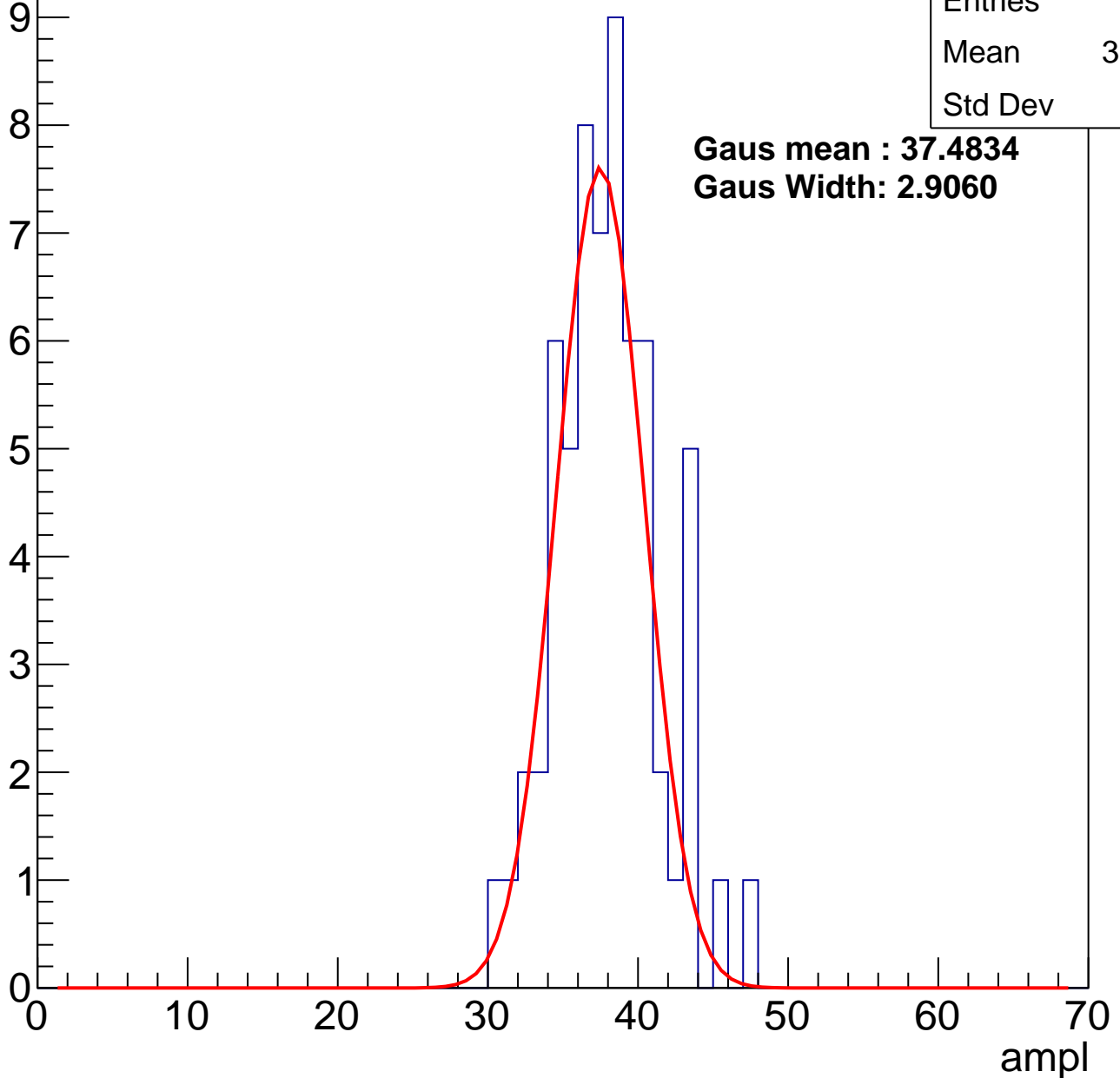
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	37.52
Std Dev	3.38

**Gaus mean : 37.4834**

**Gaus Width: 2.9060**



# B1L003S, U3-ch120, adc2

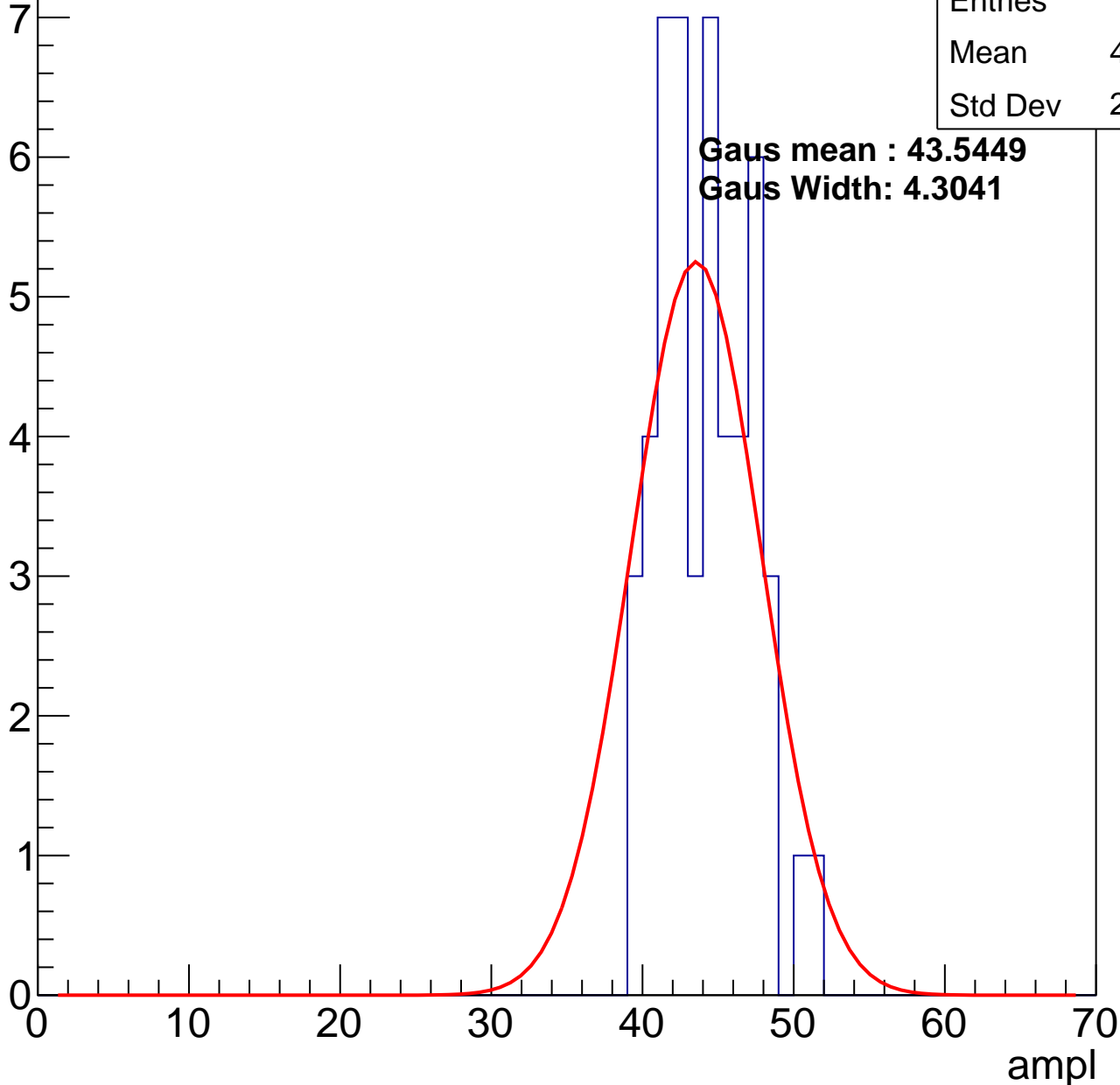
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	50
Mean	43.72
Std Dev	2.953

**Gaus mean : 43.5449**

**Gaus Width: 4.3041**

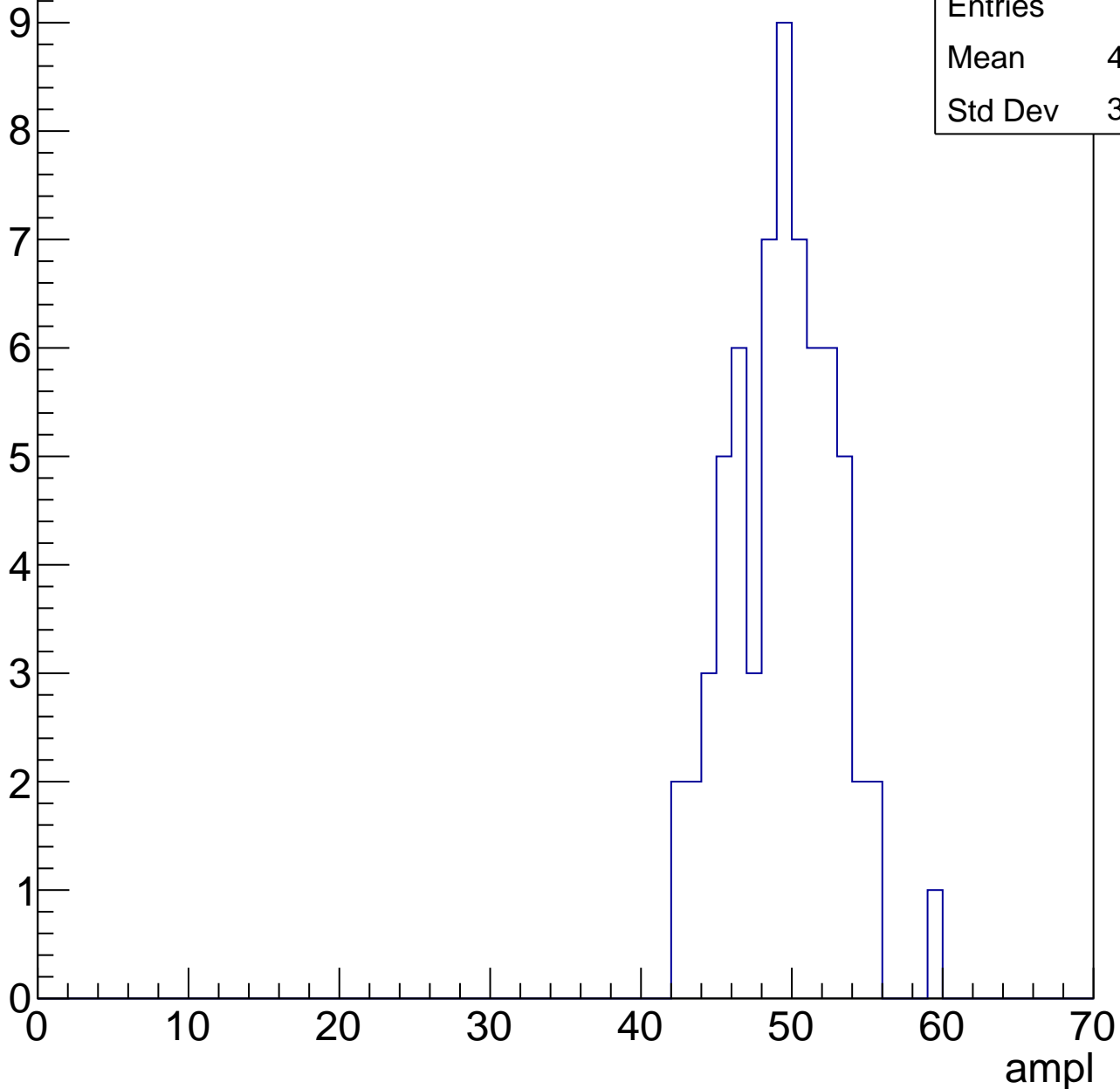


# B1L003S, U3-ch120, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

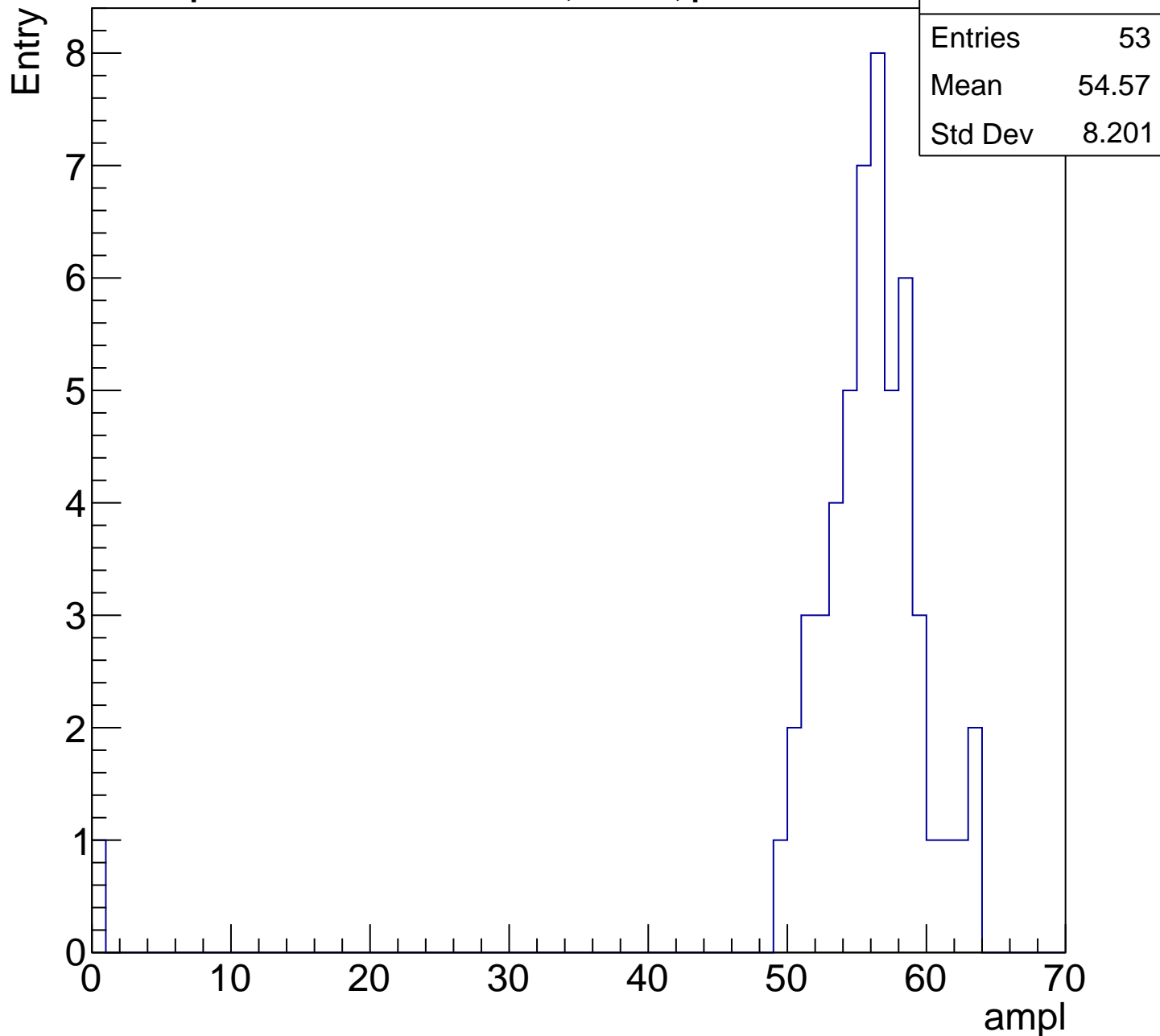
Entry

Entries	66
Mean	48.95
Std Dev	3.448



# B1L003S, U3-ch120, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

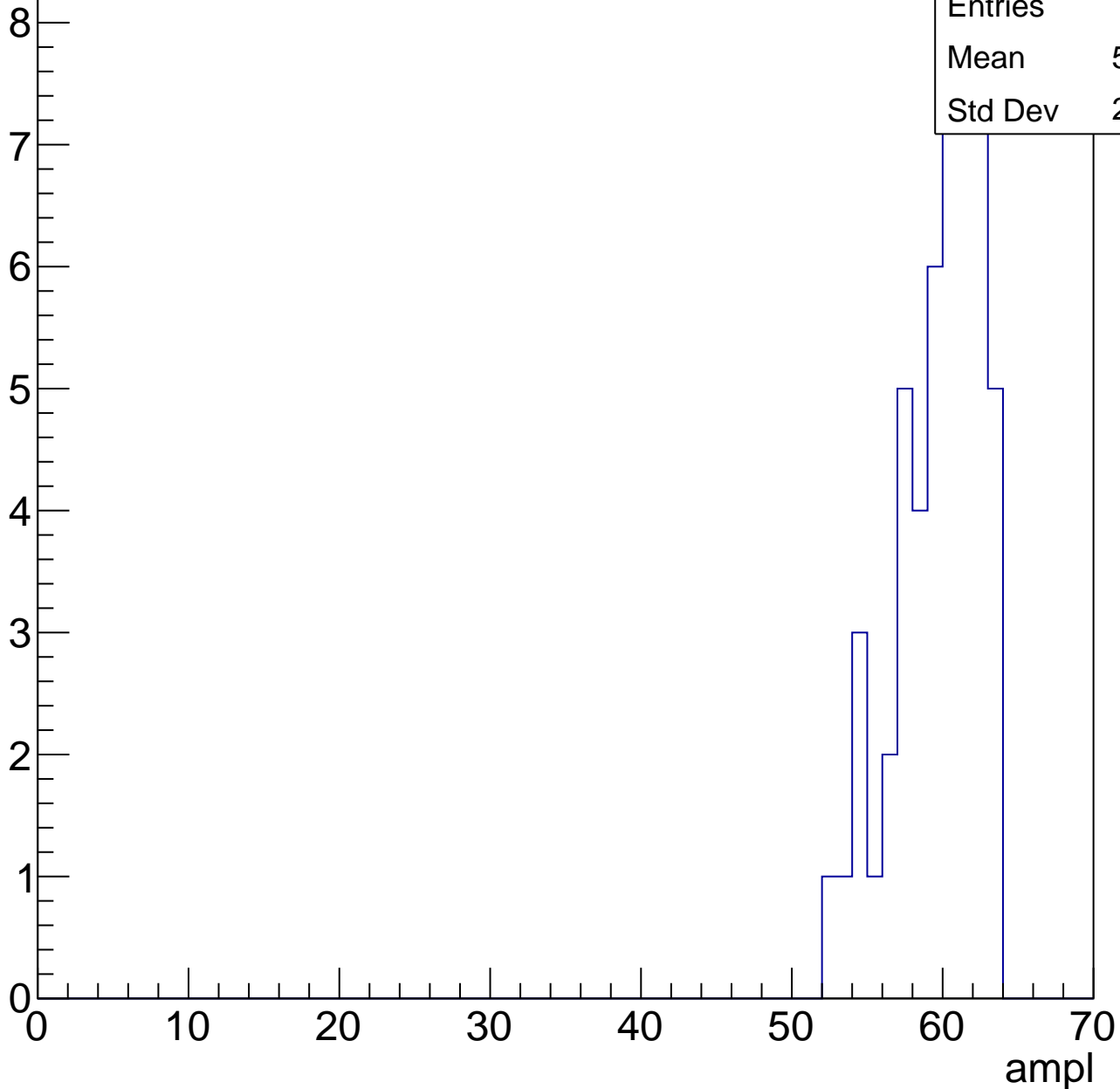


# B1L003S, U3-ch120, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	52
Mean	59.31
Std Dev	2.791



# B1L003S, U3-ch120, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch120, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L003S, U3-ch121, adc0

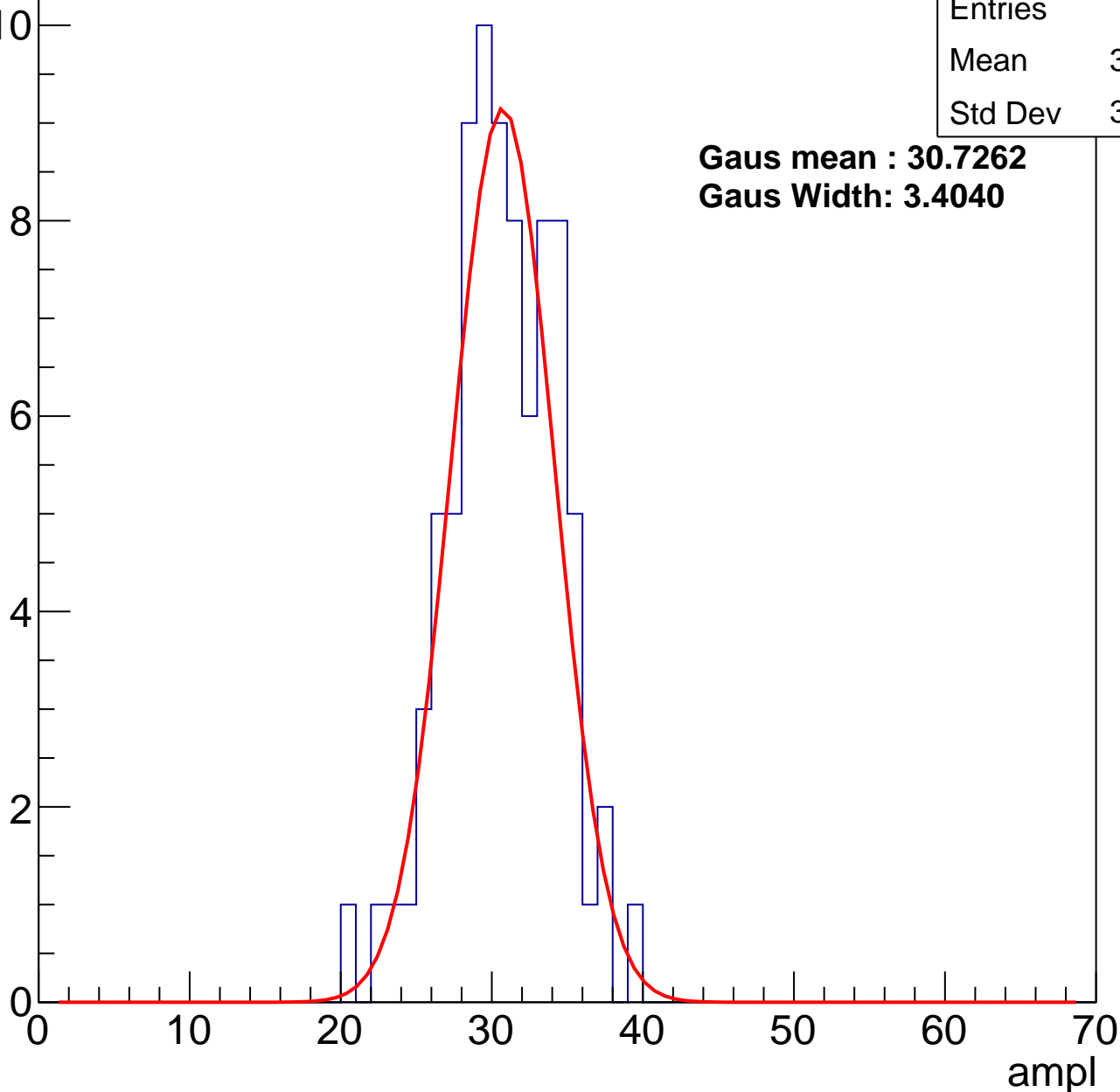
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	84
Mean	30.25
Std Dev	3.555

**Gaus mean : 30.7262**

**Gaus Width: 3.4040**



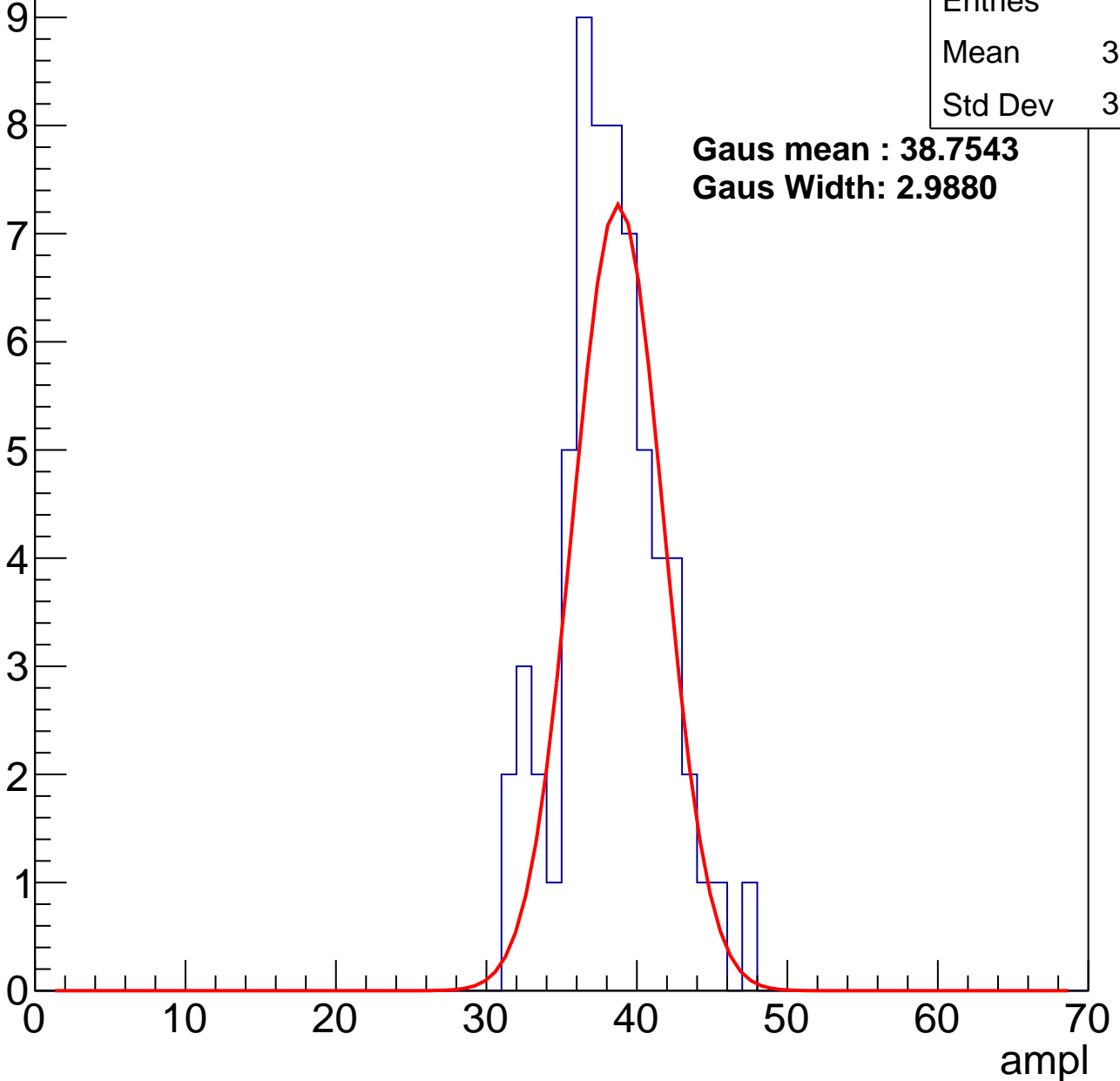
# B1L003S, U3-ch121, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	37.84
Std Dev	3.339

**Gaus mean : 38.7543**  
**Gaus Width: 2.9880**



# B1L003S, U3-ch121, adc2

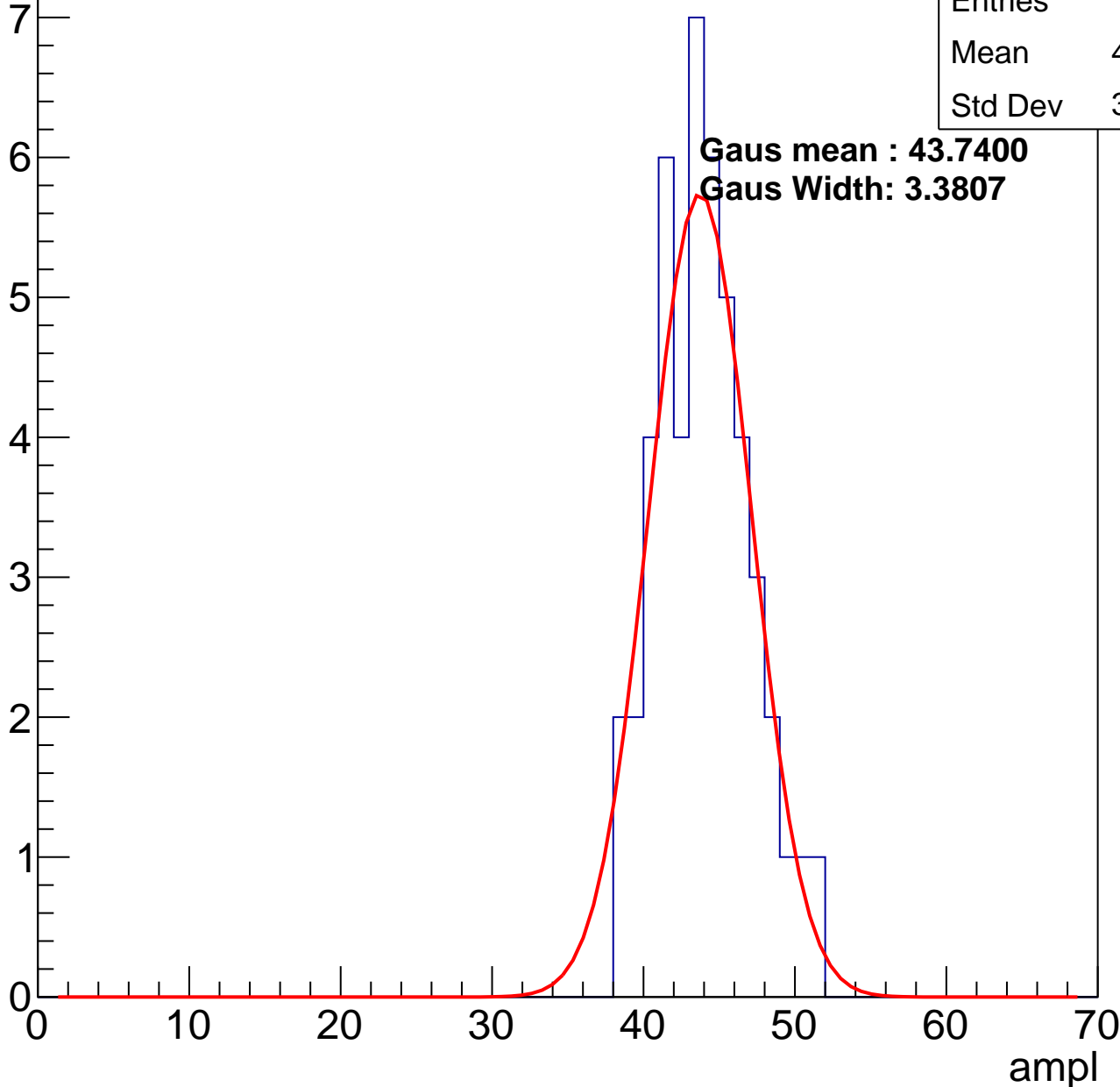
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	48
Mean	43.52
Std Dev	3.034

**Gaus mean : 43.7400**

**Gaus Width: 3.3807**

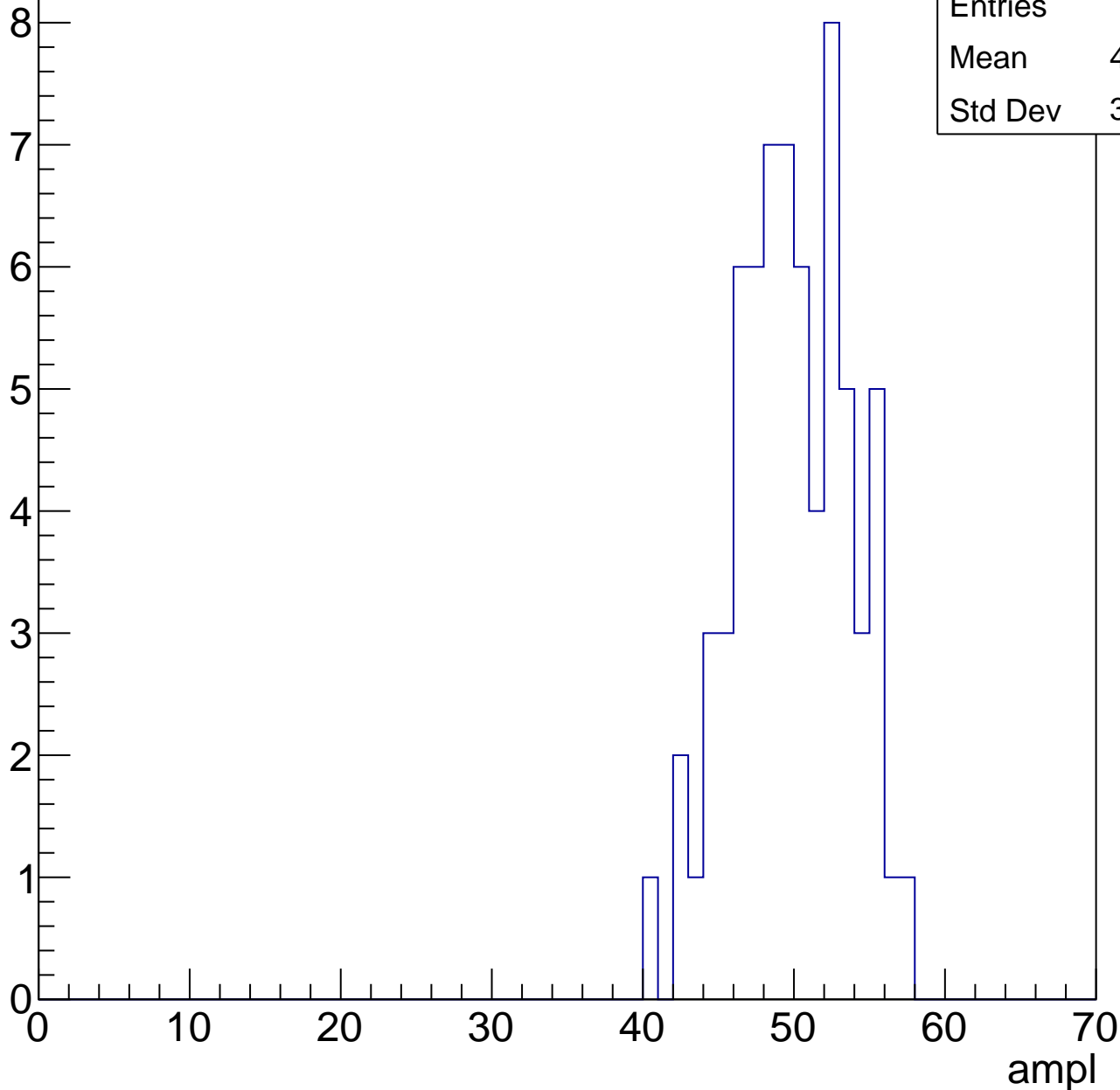


# B1L003S, U3-ch121, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

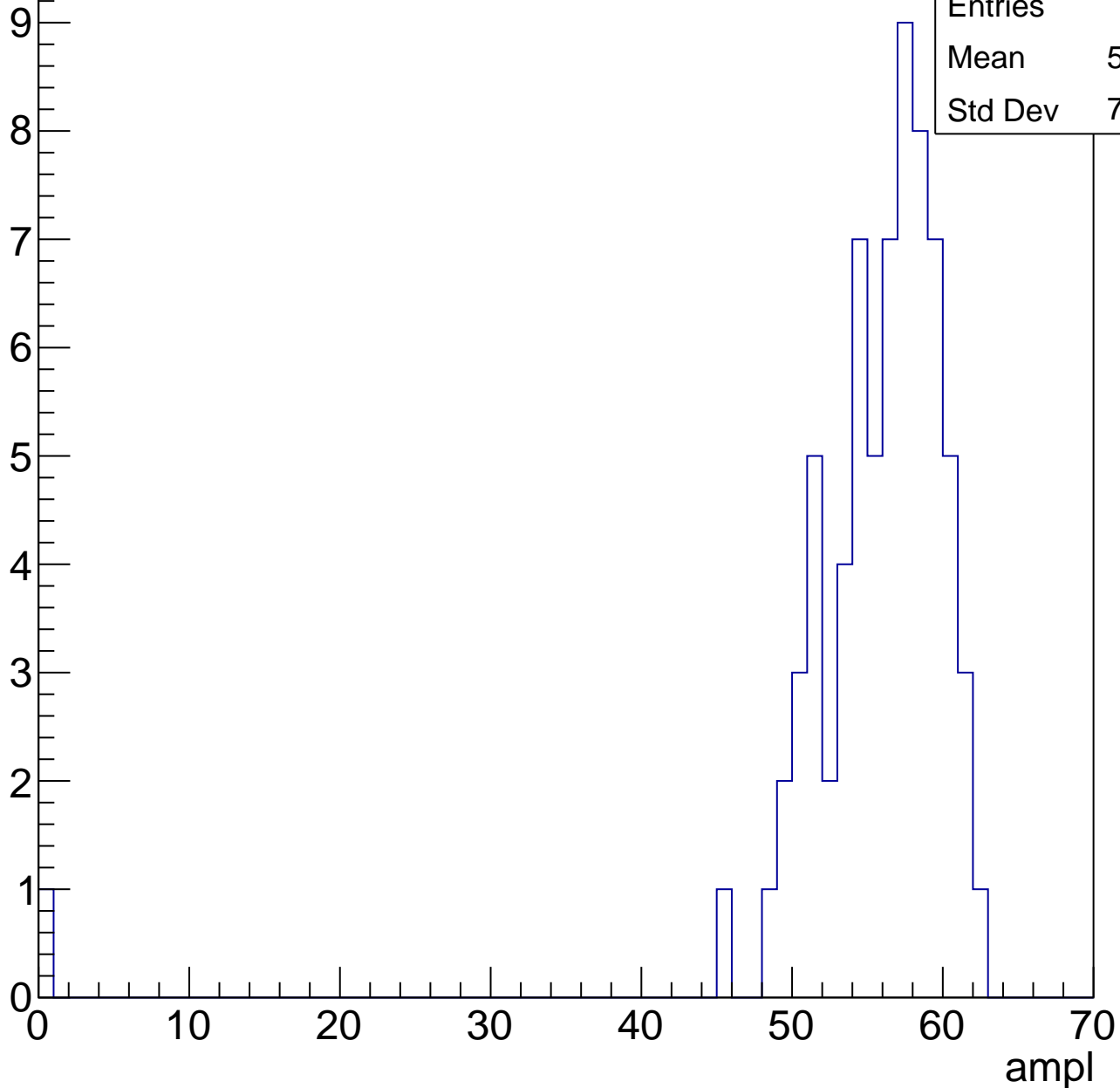
Entries	69
Mean	49.36
Std Dev	3.722



# B1L003S, U3-ch121, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

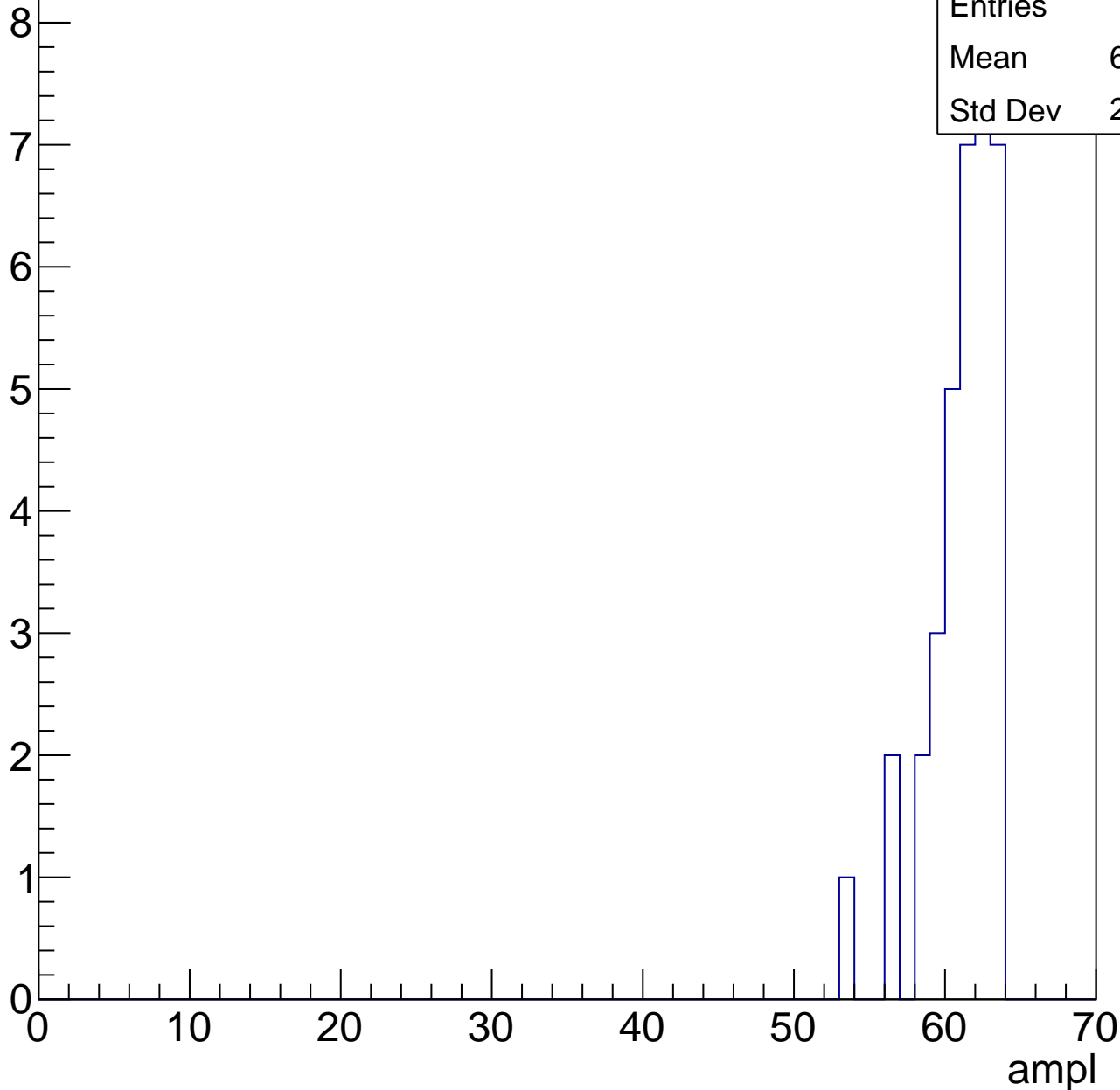


# B1L003S, U3-ch121, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

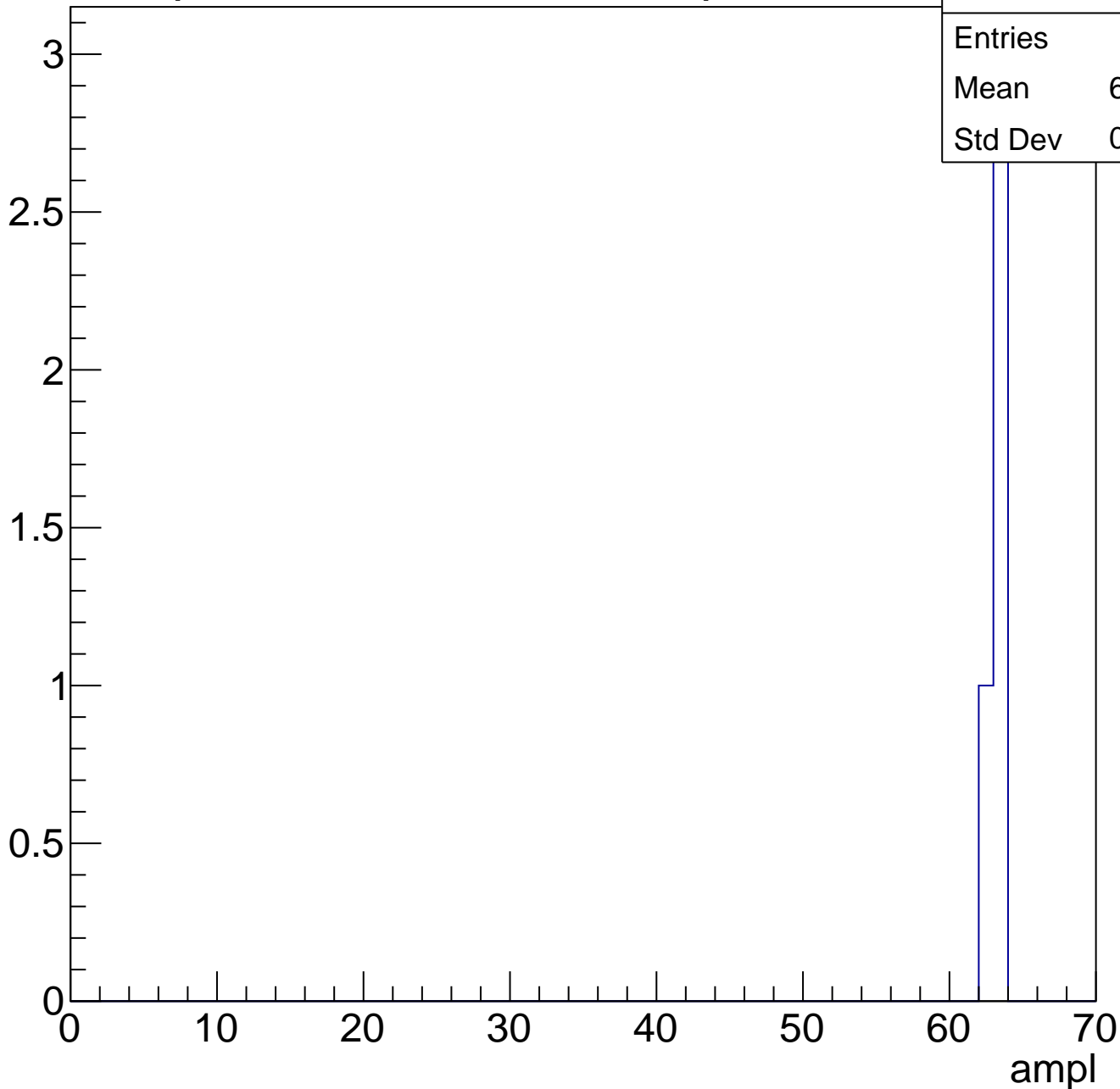
Entries	35
Mean	60.63
Std Dev	2.269



# B1L003S, U3-ch121, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch121, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U3-ch122, adc0

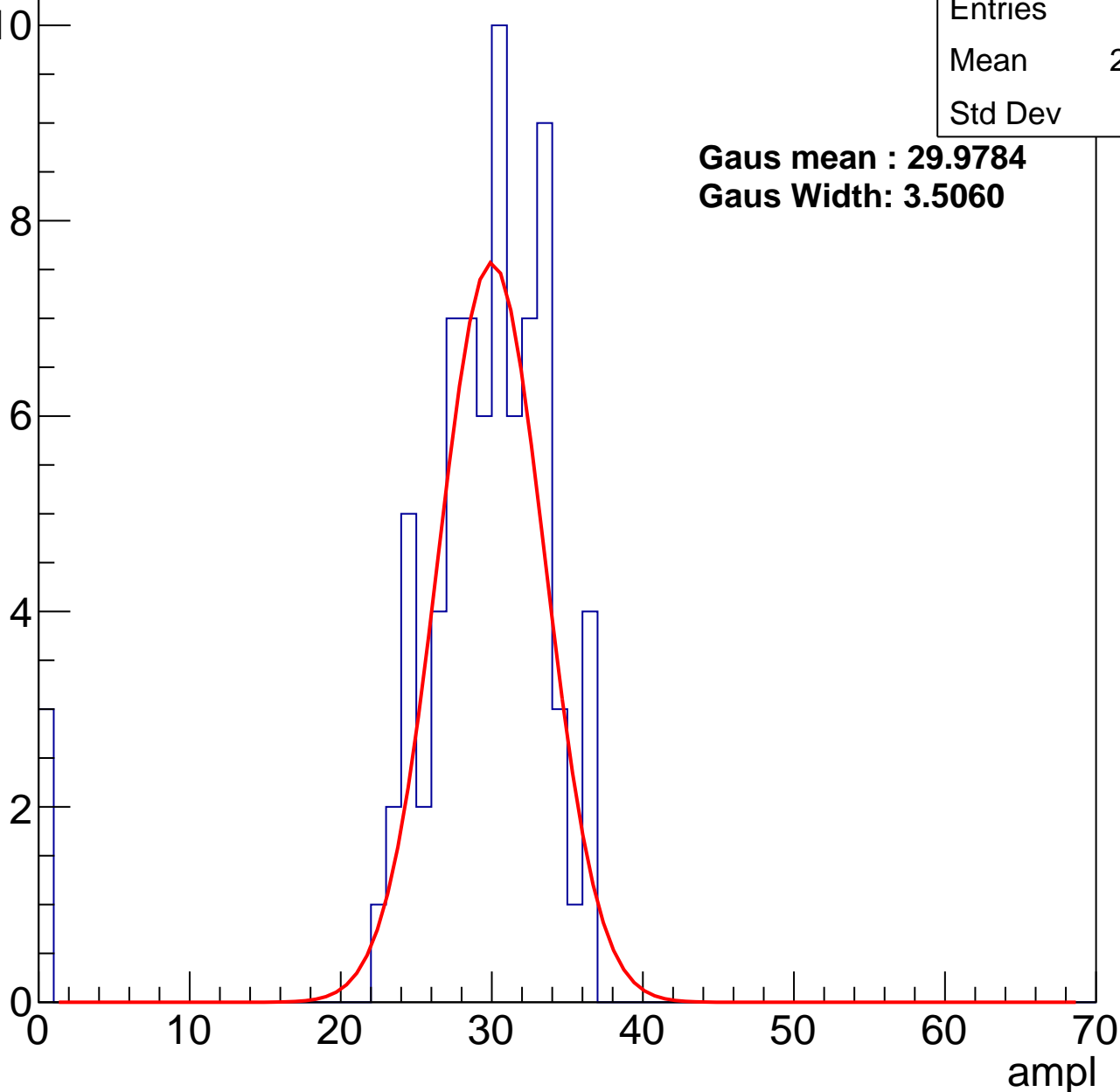
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	77
Mean	28.43
Std Dev	6.64

**Gaus mean : 29.9784**

**Gaus Width: 3.5060**



# B1L003S, U3-ch122, adc1

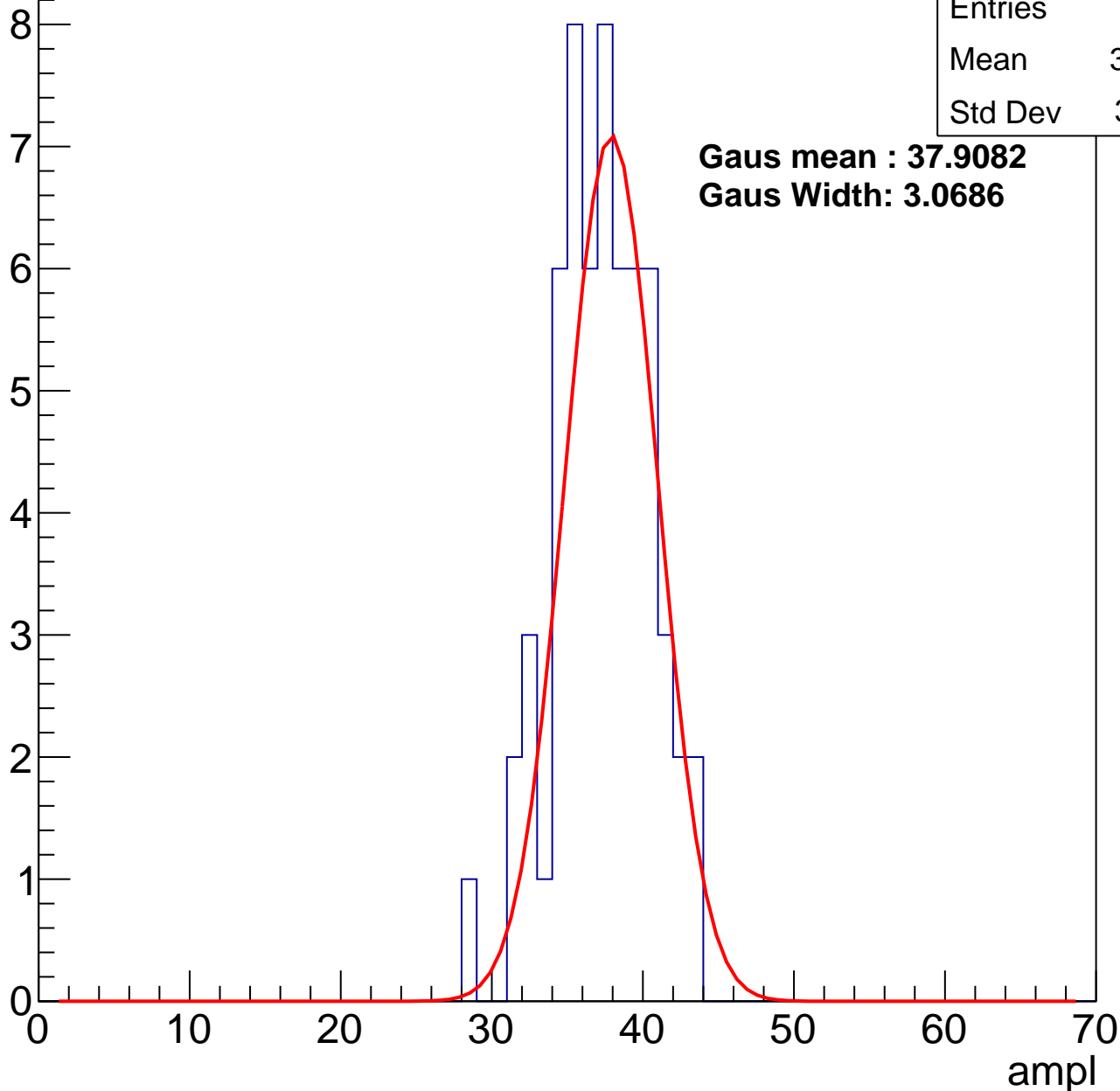
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	36.83
Std Dev	3.131

**Gaus mean : 37.9082**

**Gaus Width: 3.0686**



# B1L003S, U3-ch122, adc2

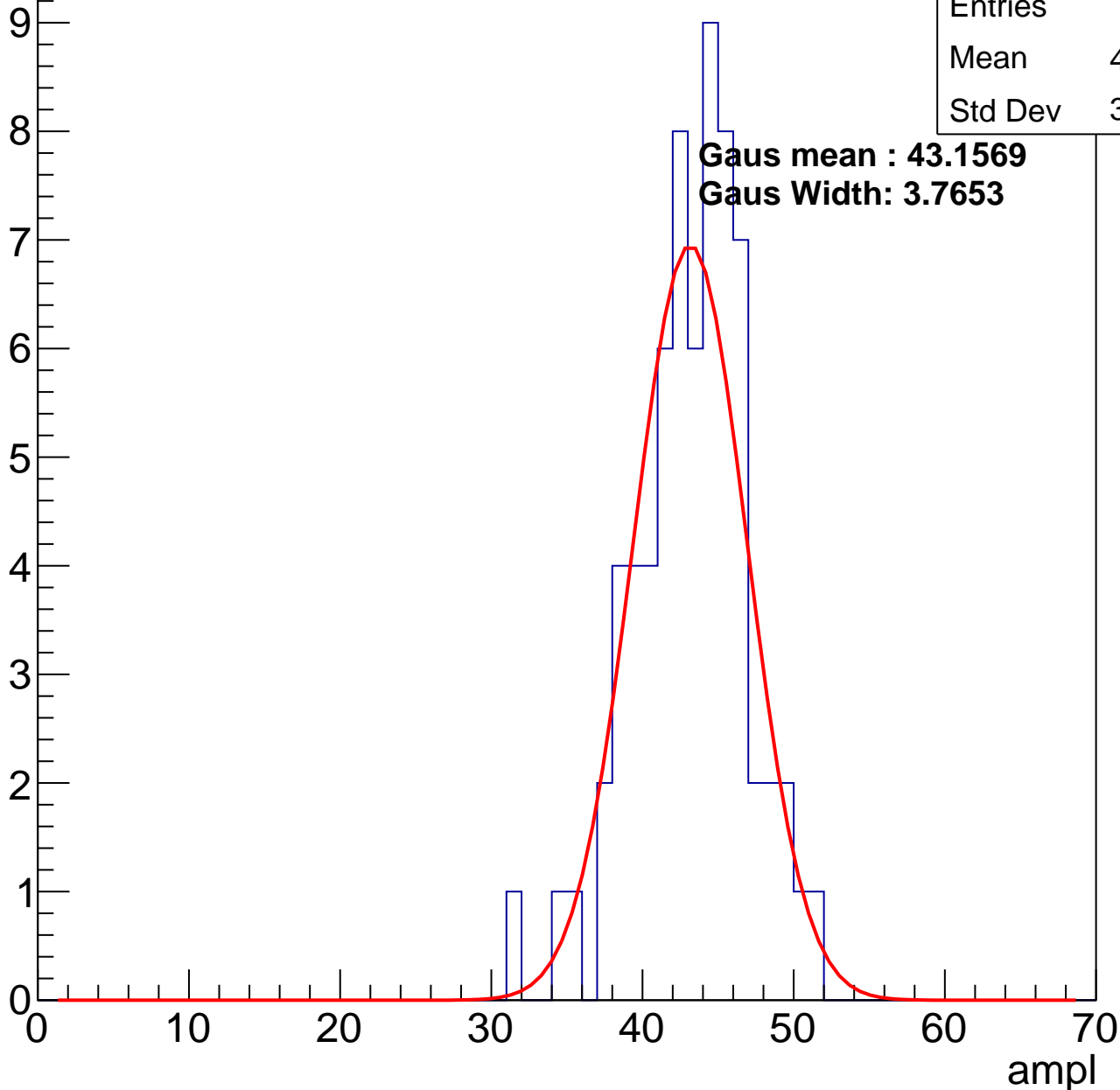
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	42.74
Std Dev	3.729

**Gaus mean : 43.1569**

**Gaus Width: 3.7653**

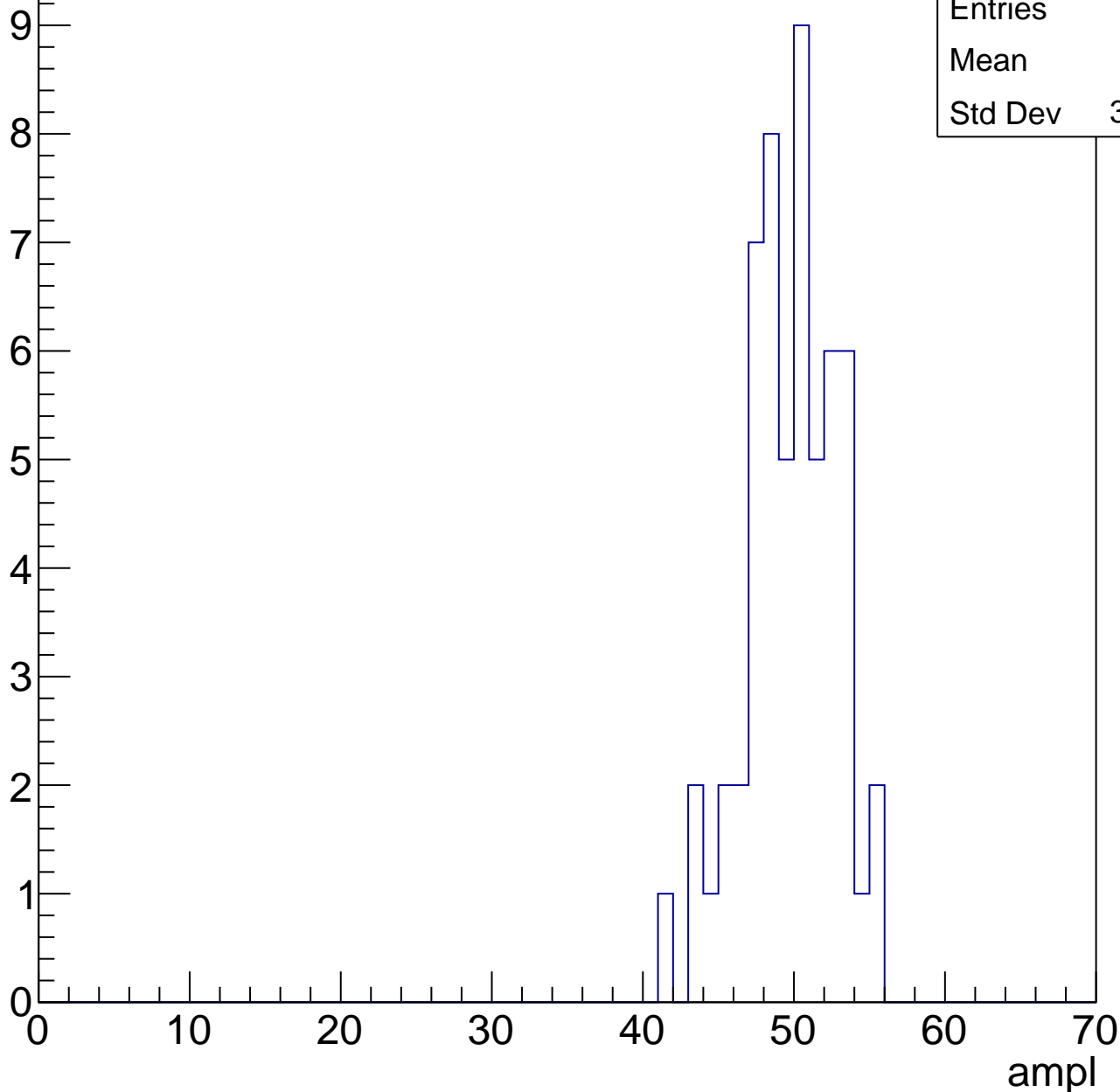


# B1L003S, U3-ch122, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	49.3
Std Dev	3.014

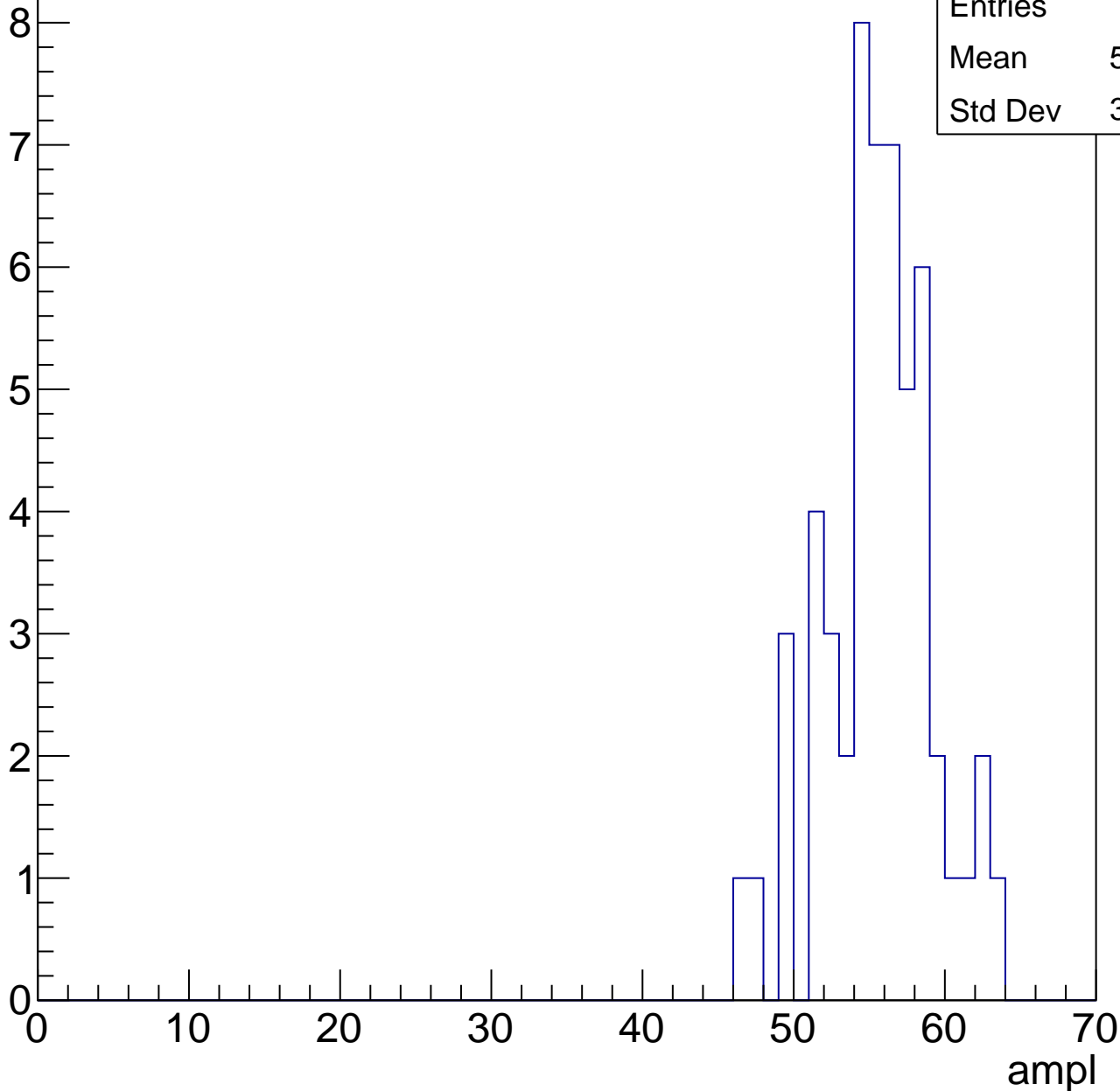


# B1L003S, U3-ch122, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	54
Mean	55.07
Std Dev	3.589

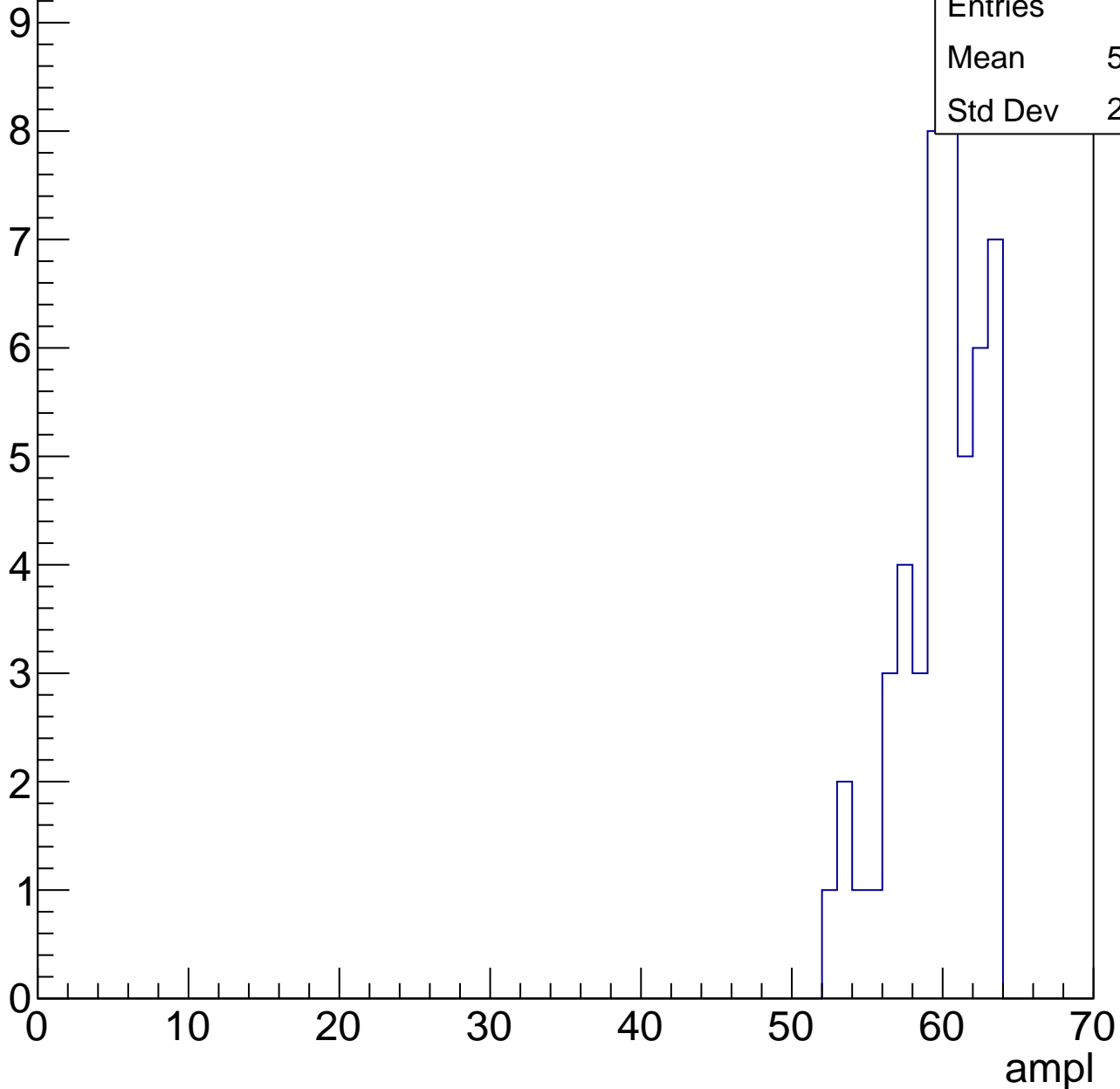


# B1L003S, U3-ch122, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

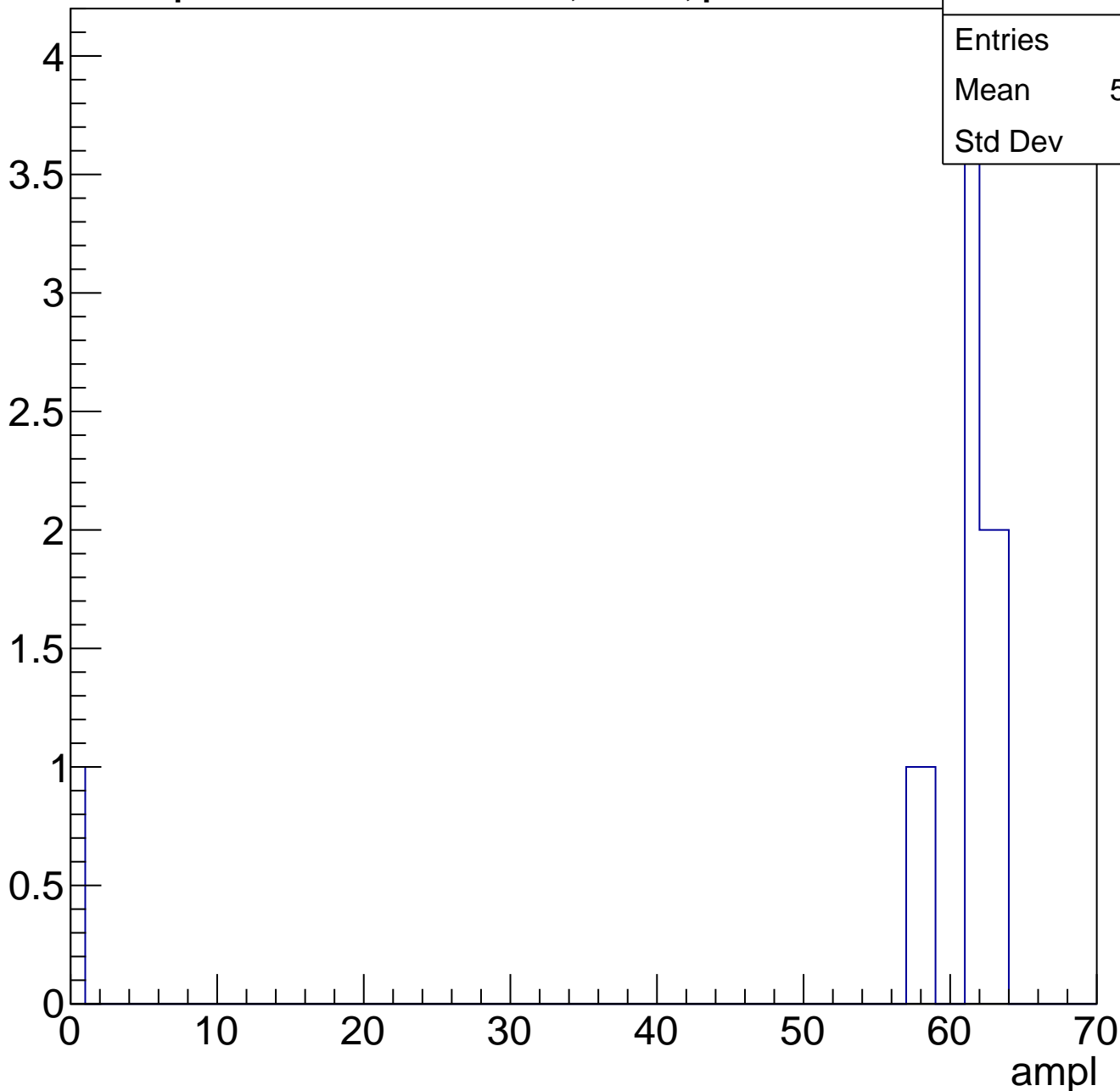
Entries	50
Mean	59.34
Std Dev	2.819



# B1L003S, U3-ch122, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	11
Mean	55.36
Std Dev	17.6



# B1L003S, U3-ch122, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U3-ch123, adc0

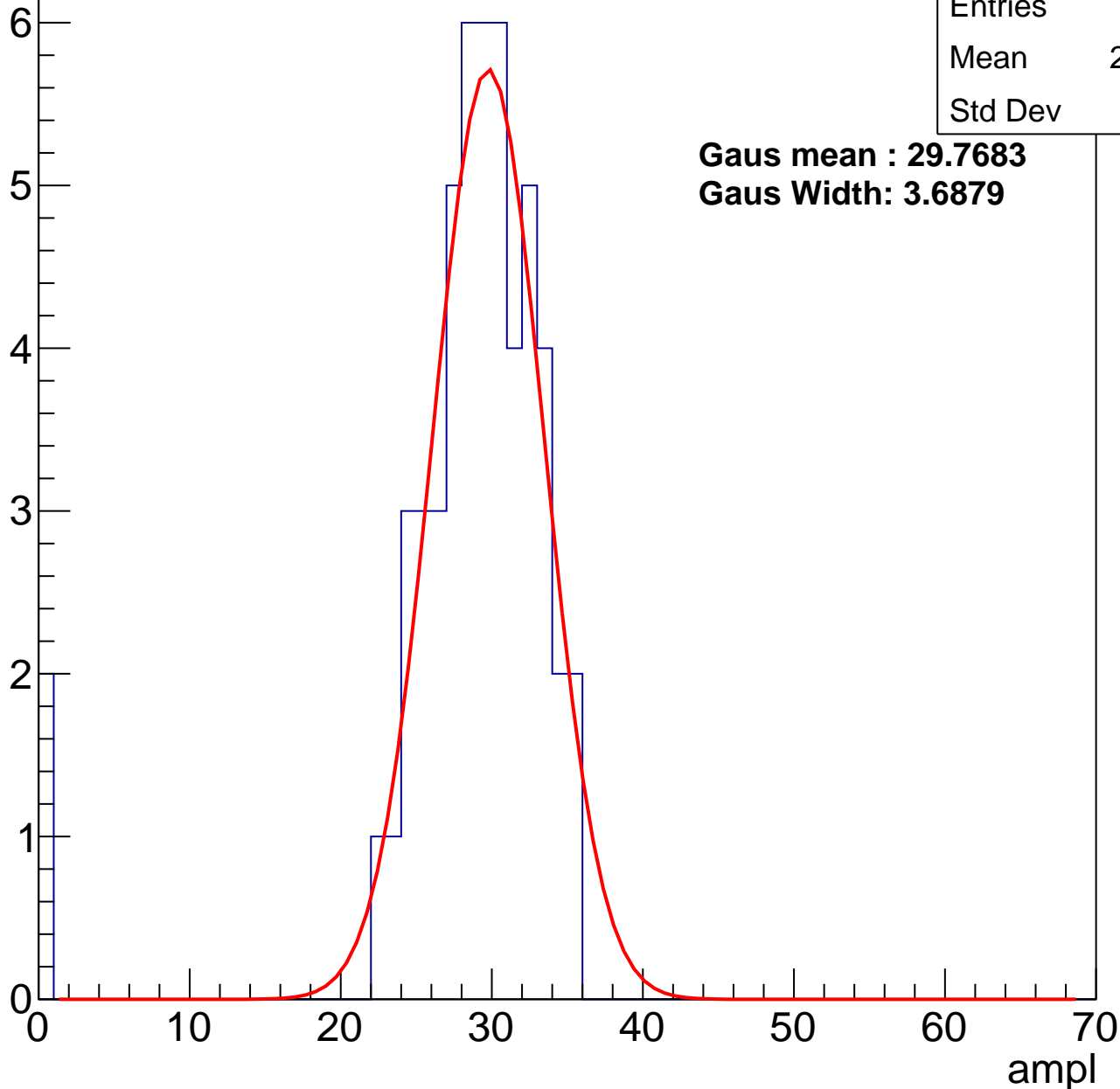
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	27.94
Std Dev	6.35

**Gaus mean : 29.7683**

**Gaus Width: 3.6879**



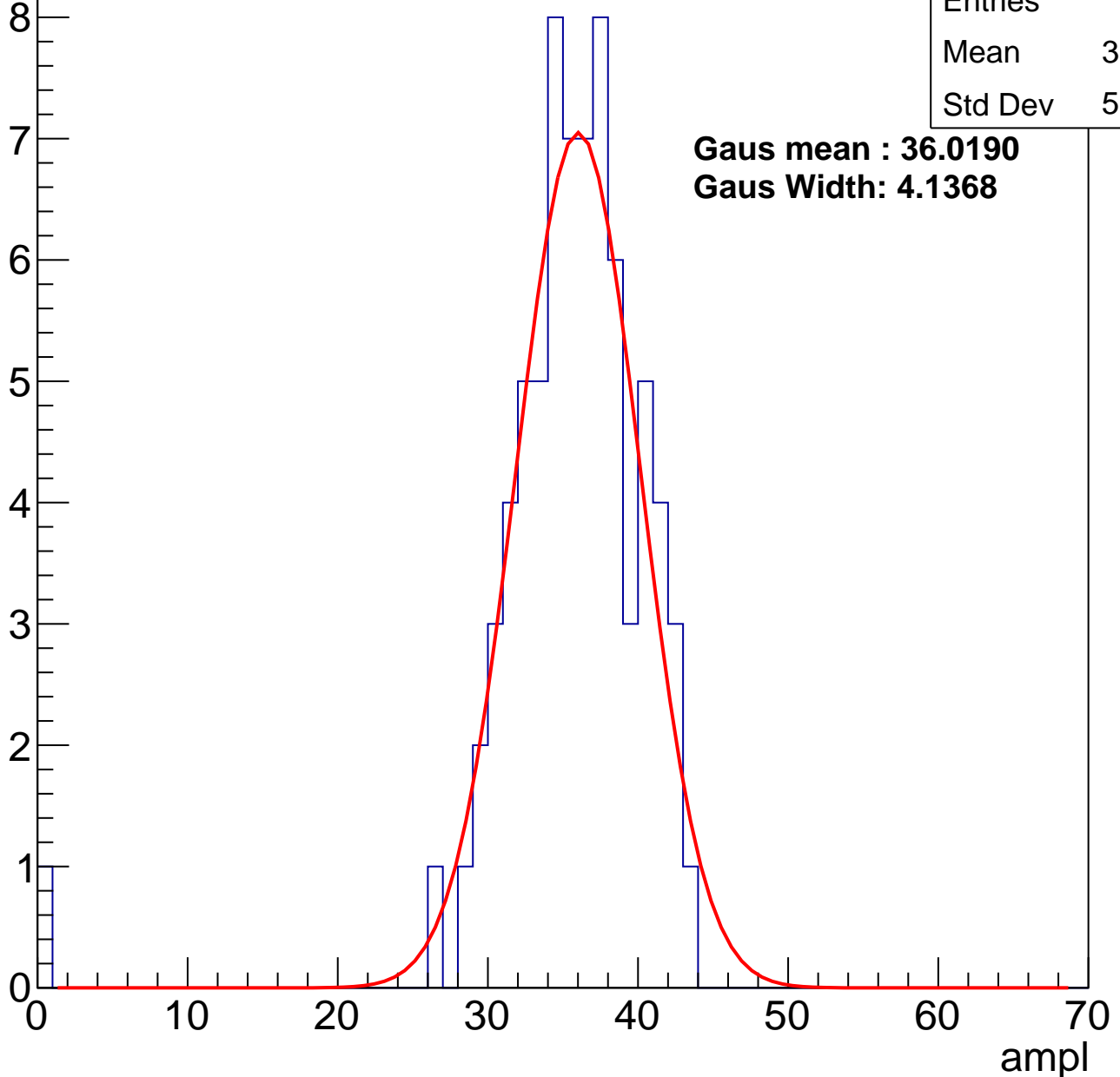
# B1L003S, U3-ch123, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	74
Mean	35.05
Std Dev	5.526

**Gaus mean : 36.0190**  
**Gaus Width: 4.1368**

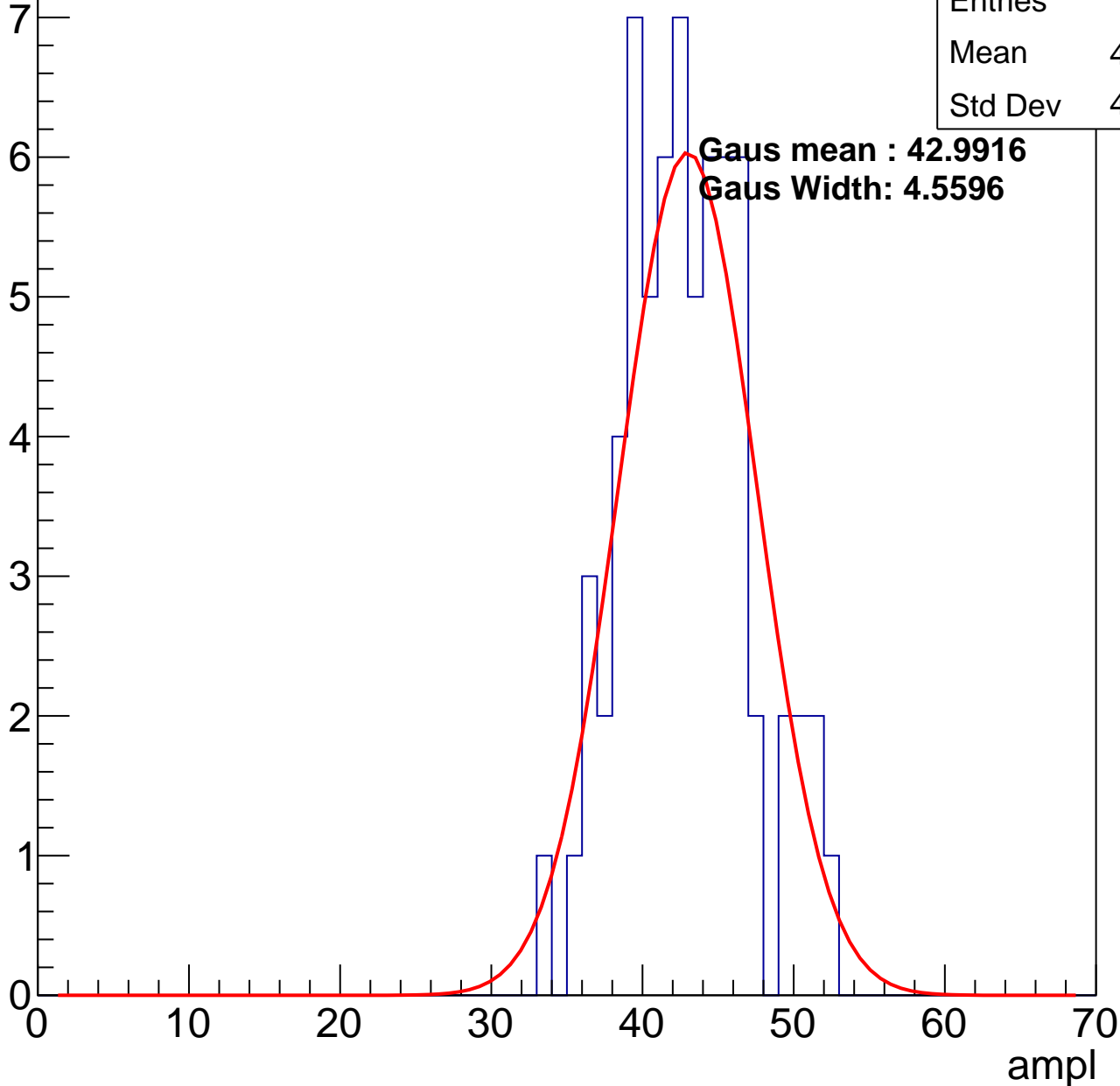


# B1L003S, U3-ch123, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	42.44
Std Dev	4.103

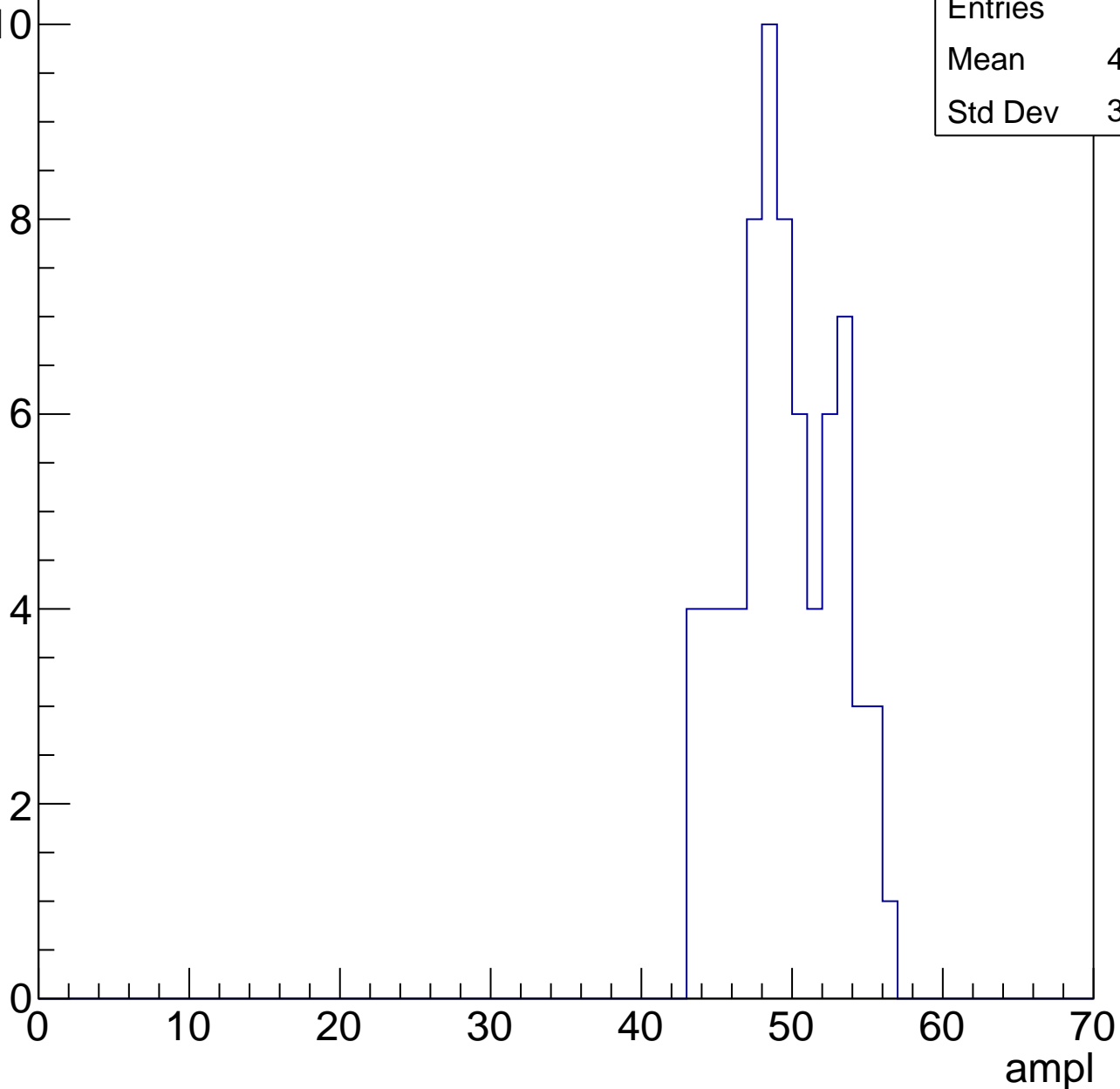


# B1L003S, U3-ch123, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	72
Mean	49.03
Std Dev	3.346

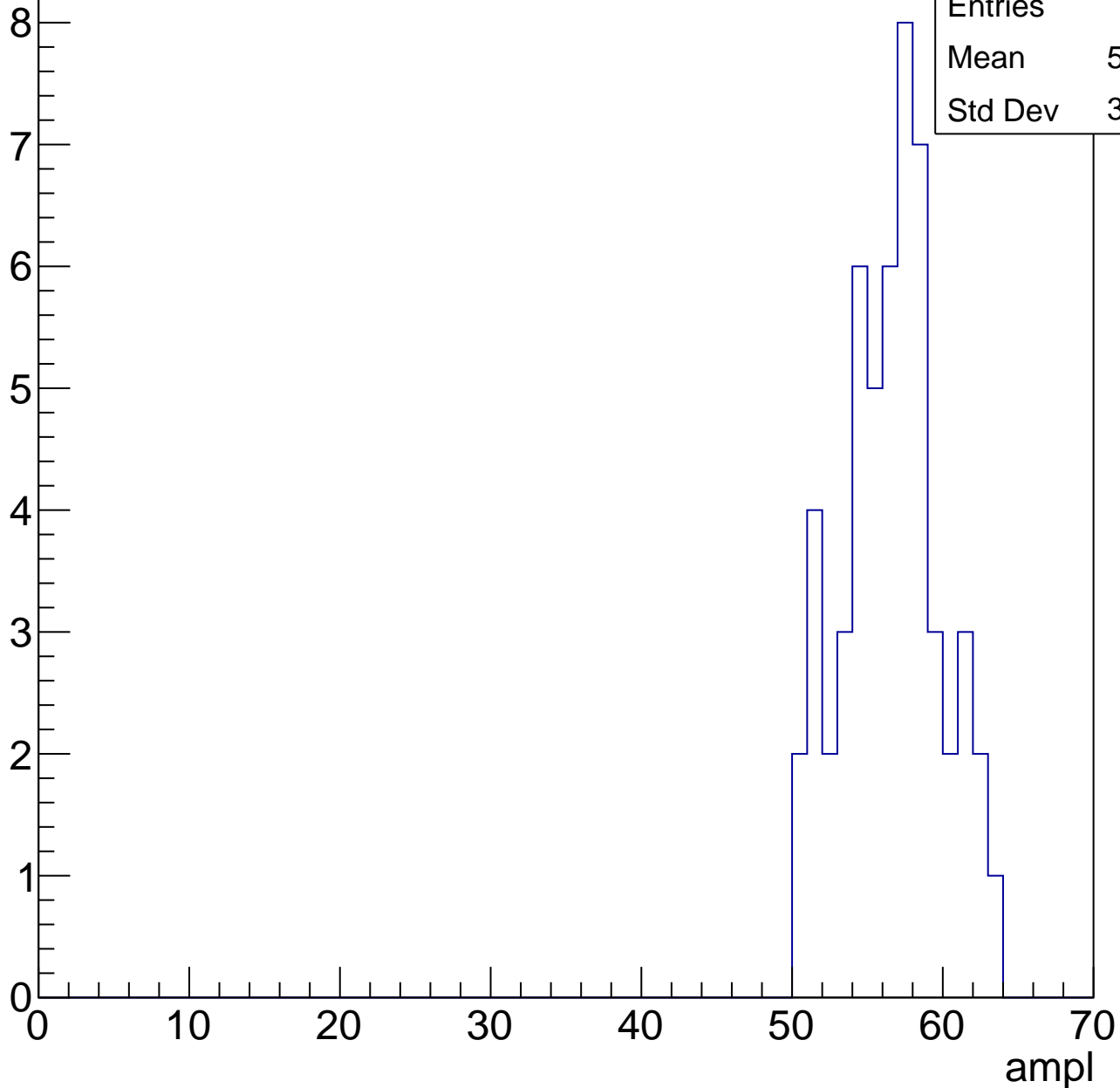


# B1L003S, U3-ch123, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	54
Mean	56.13
Std Dev	3.192

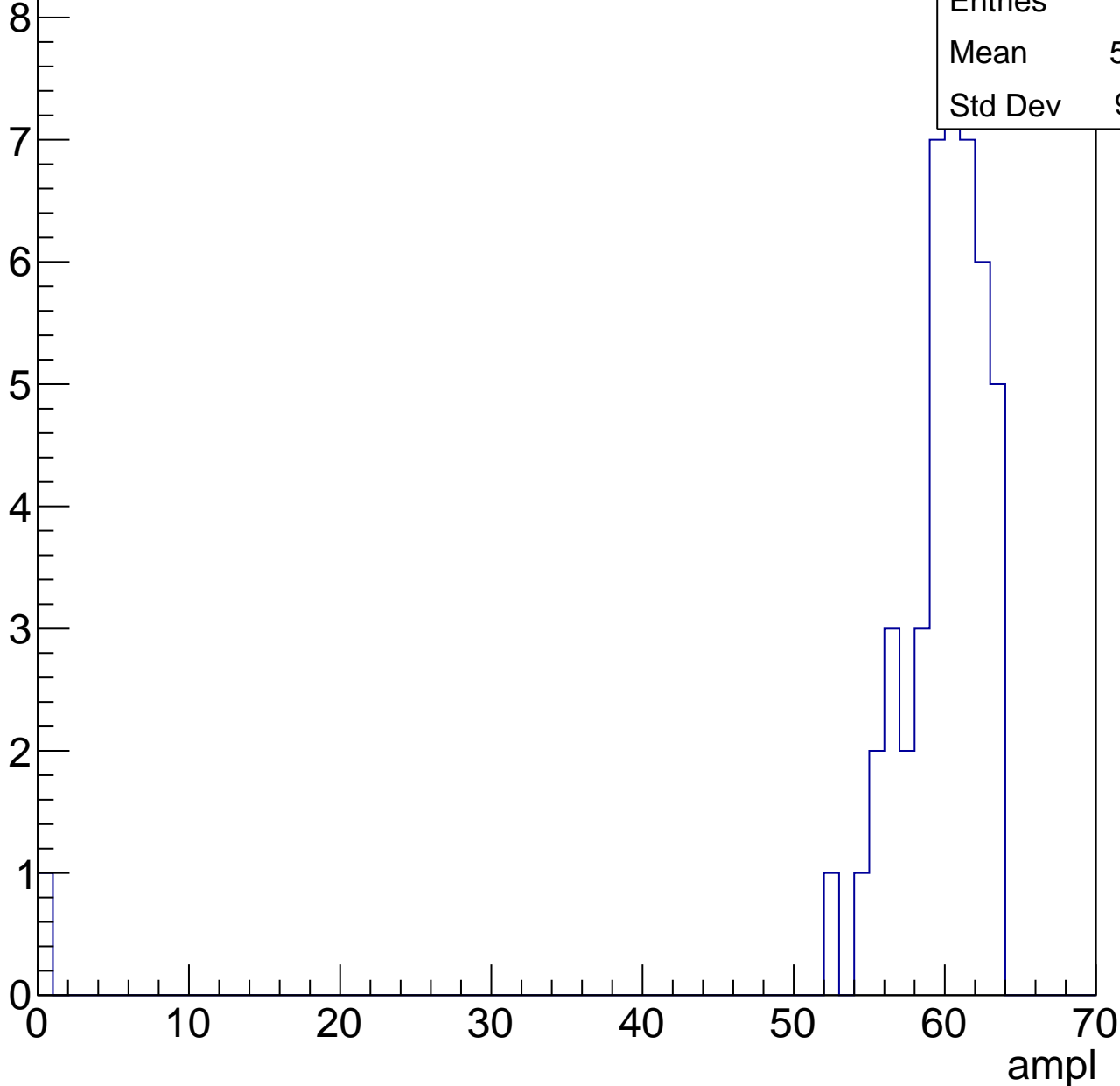


# B1L003S, U3-ch123, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

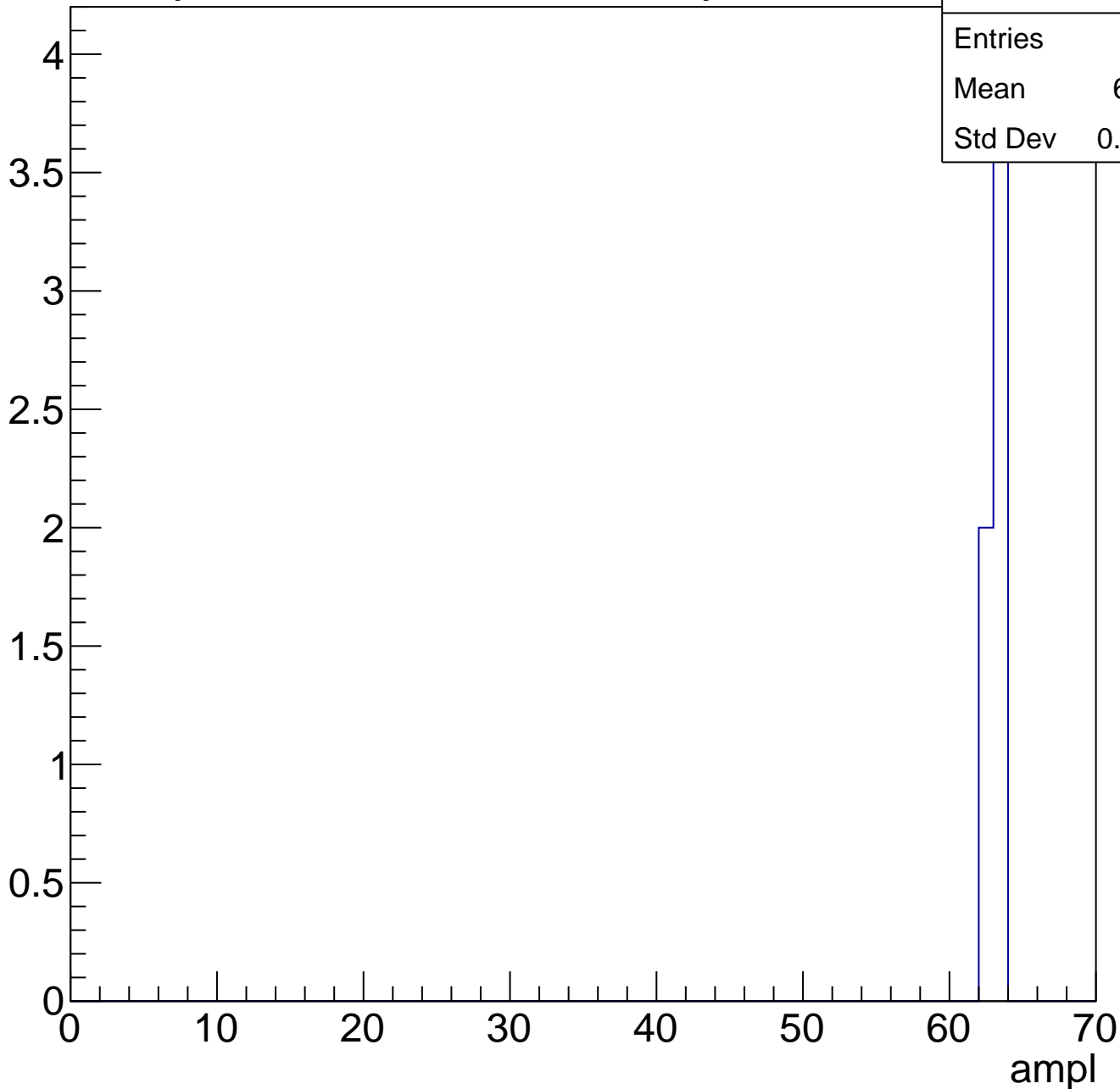
Entries	46
Mean	58.24
Std Dev	9.051



# B1L003S, U3-ch123, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch123, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L003S, U3-ch124, adc0

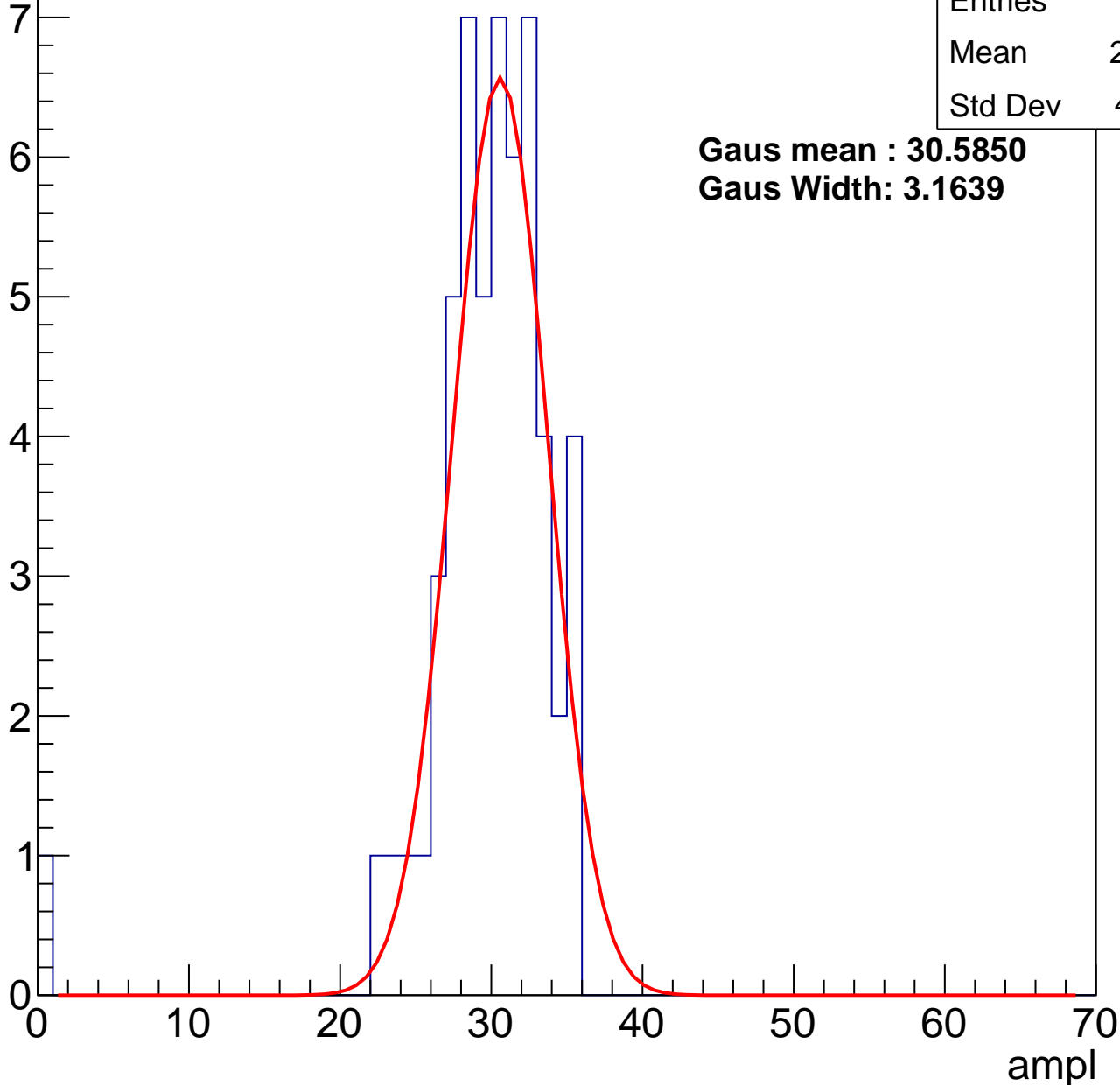
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	29.24
Std Dev	4.991

**Gaus mean : 30.5850**

**Gaus Width: 3.1639**



# B1L003S, U3-ch124, adc1

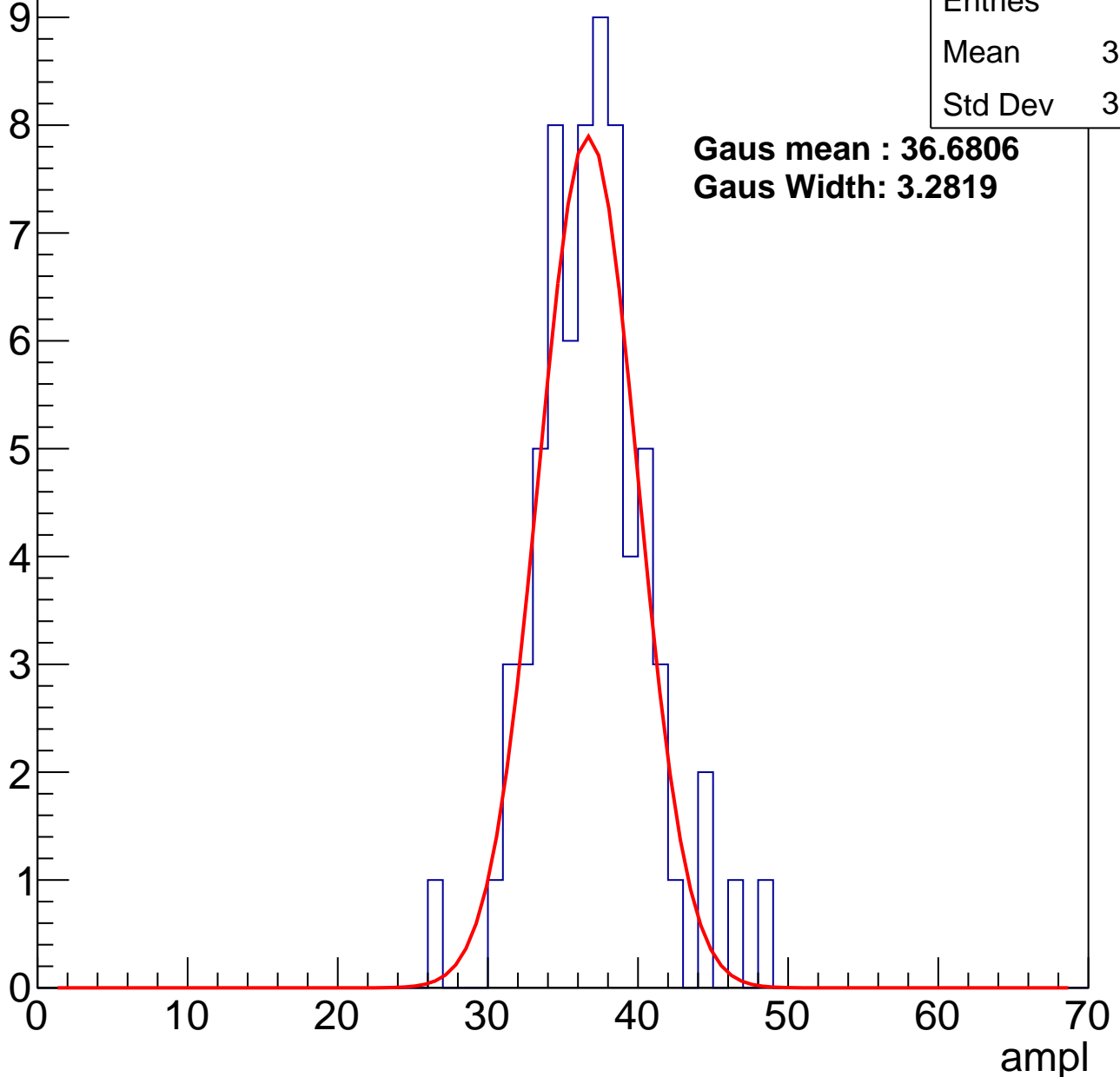
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	36.52
Std Dev	3.736

**Gaus mean : 36.6806**

**Gaus Width: 3.2819**



# B1L003S, U3-ch124, adc2

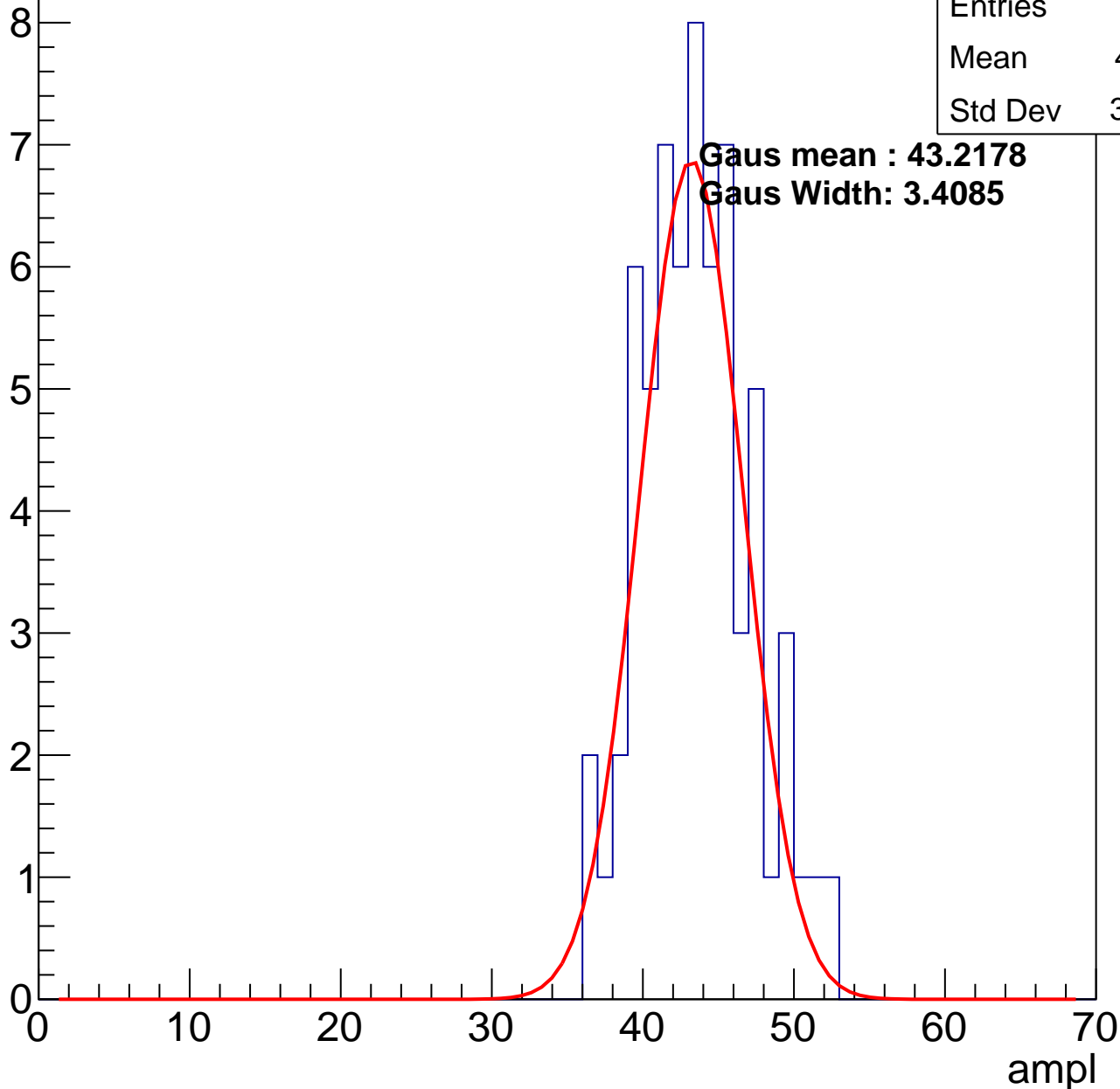
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	43.11
Std Dev	3.565

**Gaus mean : 43.2178**

**Gaus Width: 3.4085**

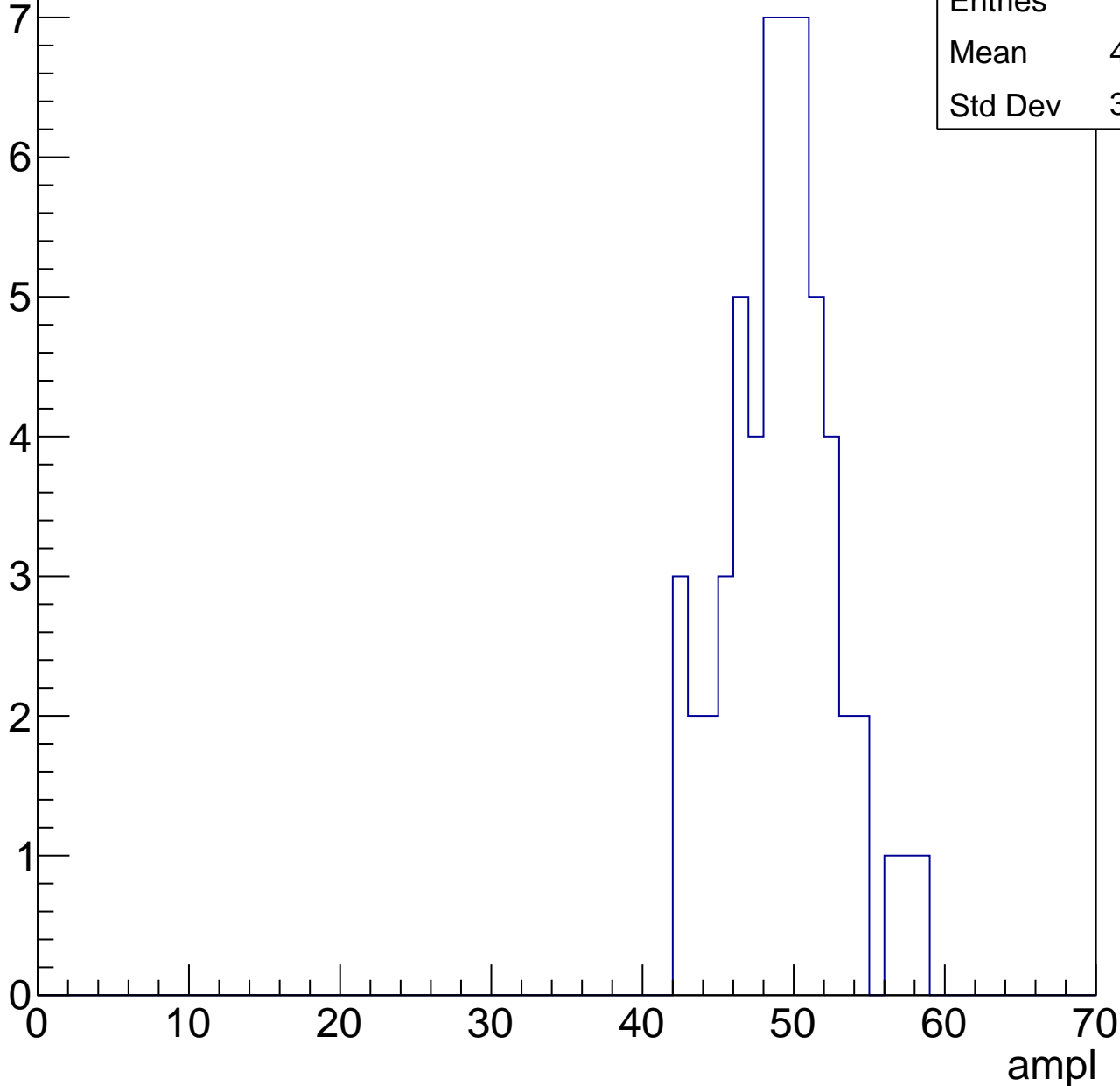


# B1L003S, U3-ch124, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	48.75
Std Dev	3.587

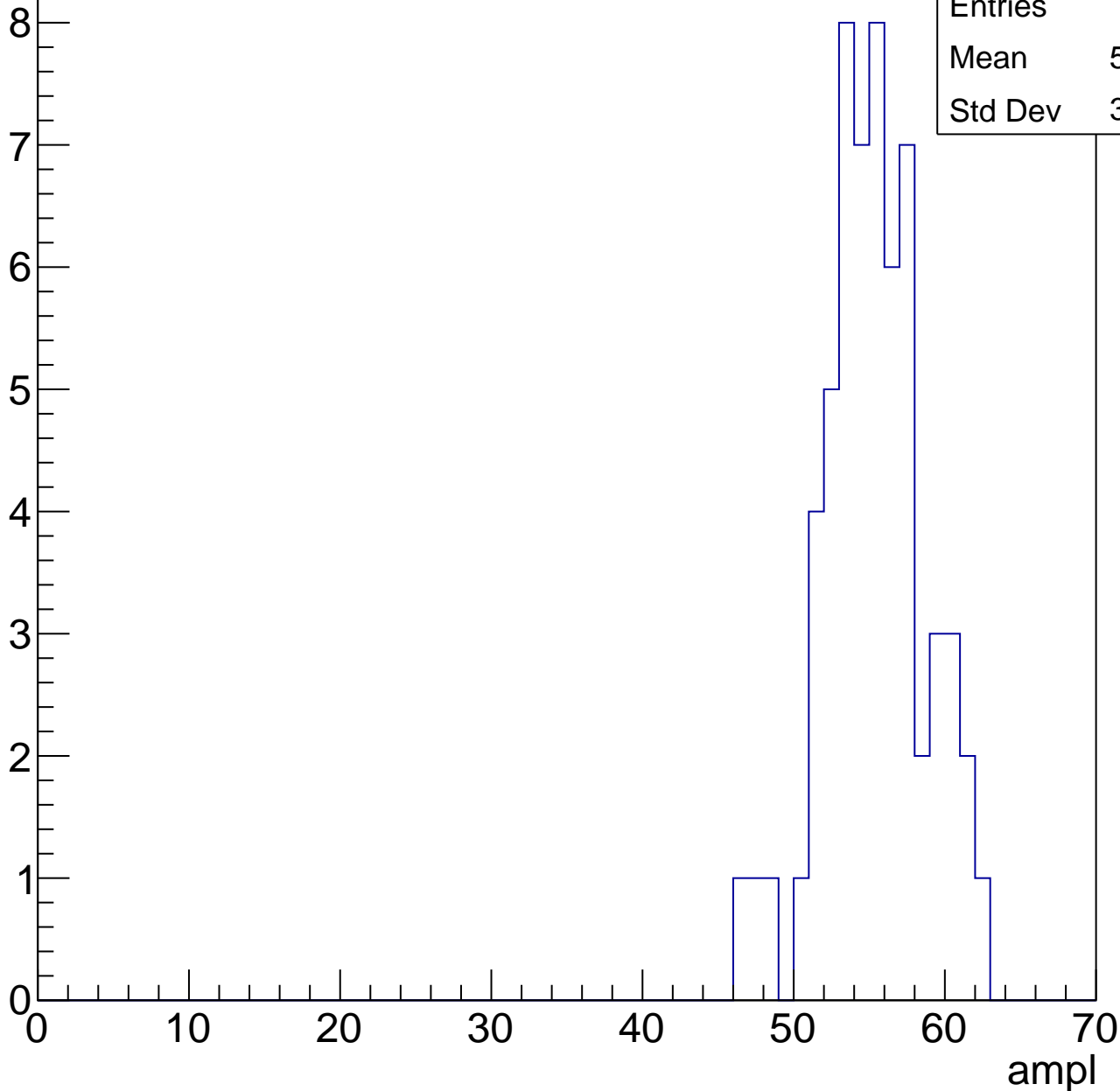


# B1L003S, U3-ch124, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	54.82
Std Dev	3.319

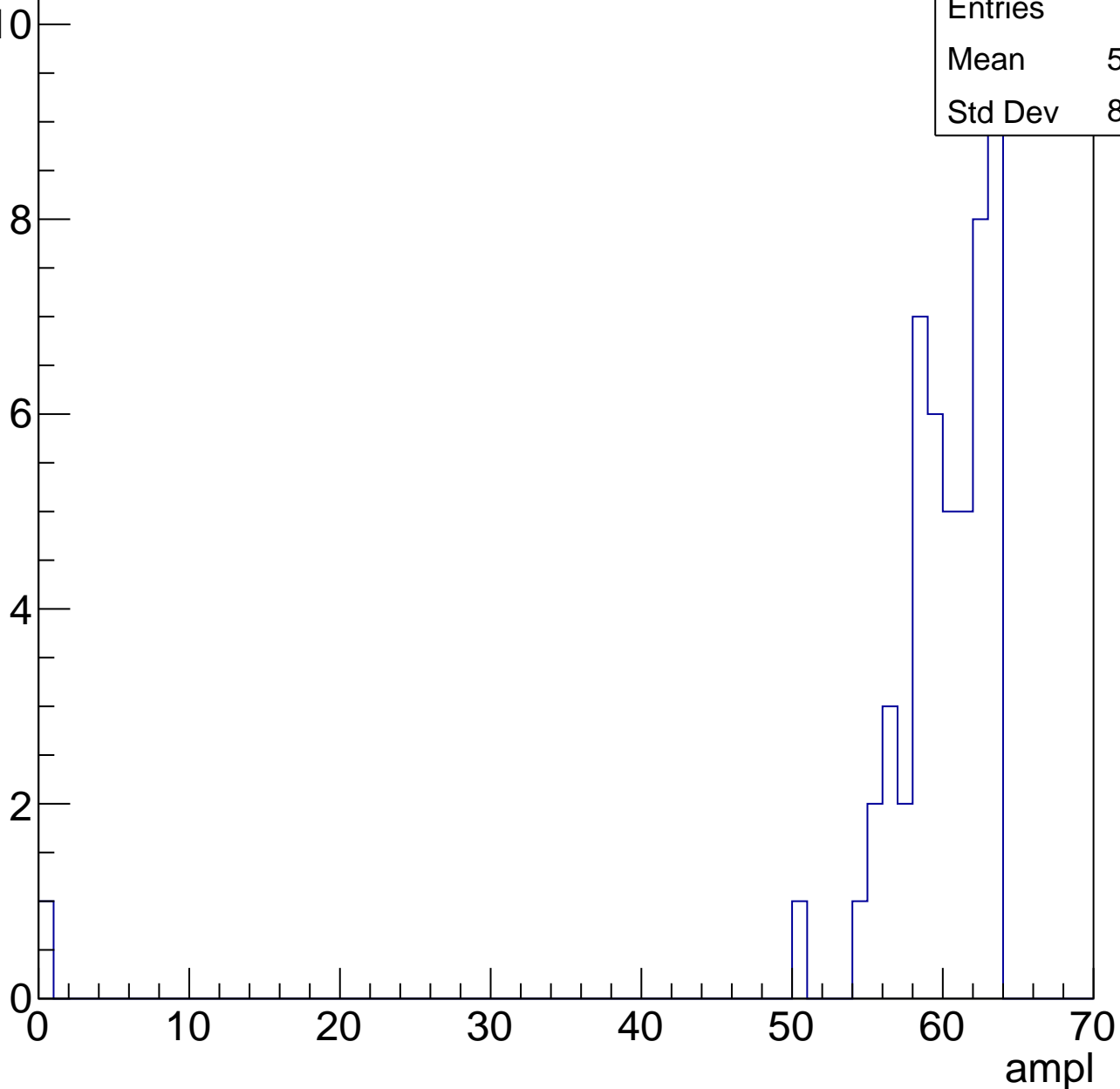


# B1L003S, U3-ch124, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

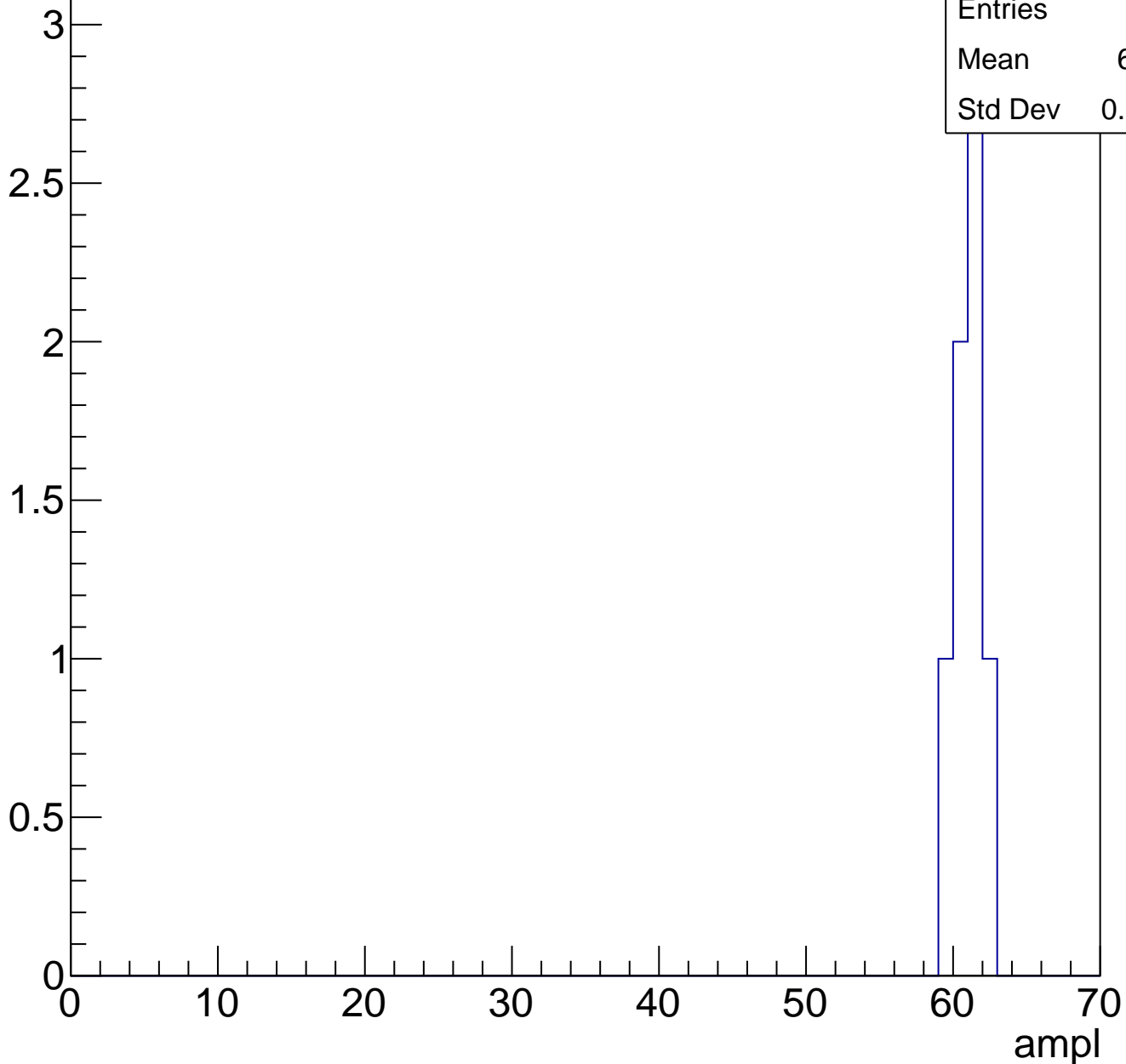
Entries	51
Mean	58.57
Std Dev	8.754



# B1L003S, U3-ch124, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch124, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U3-ch125, adc0

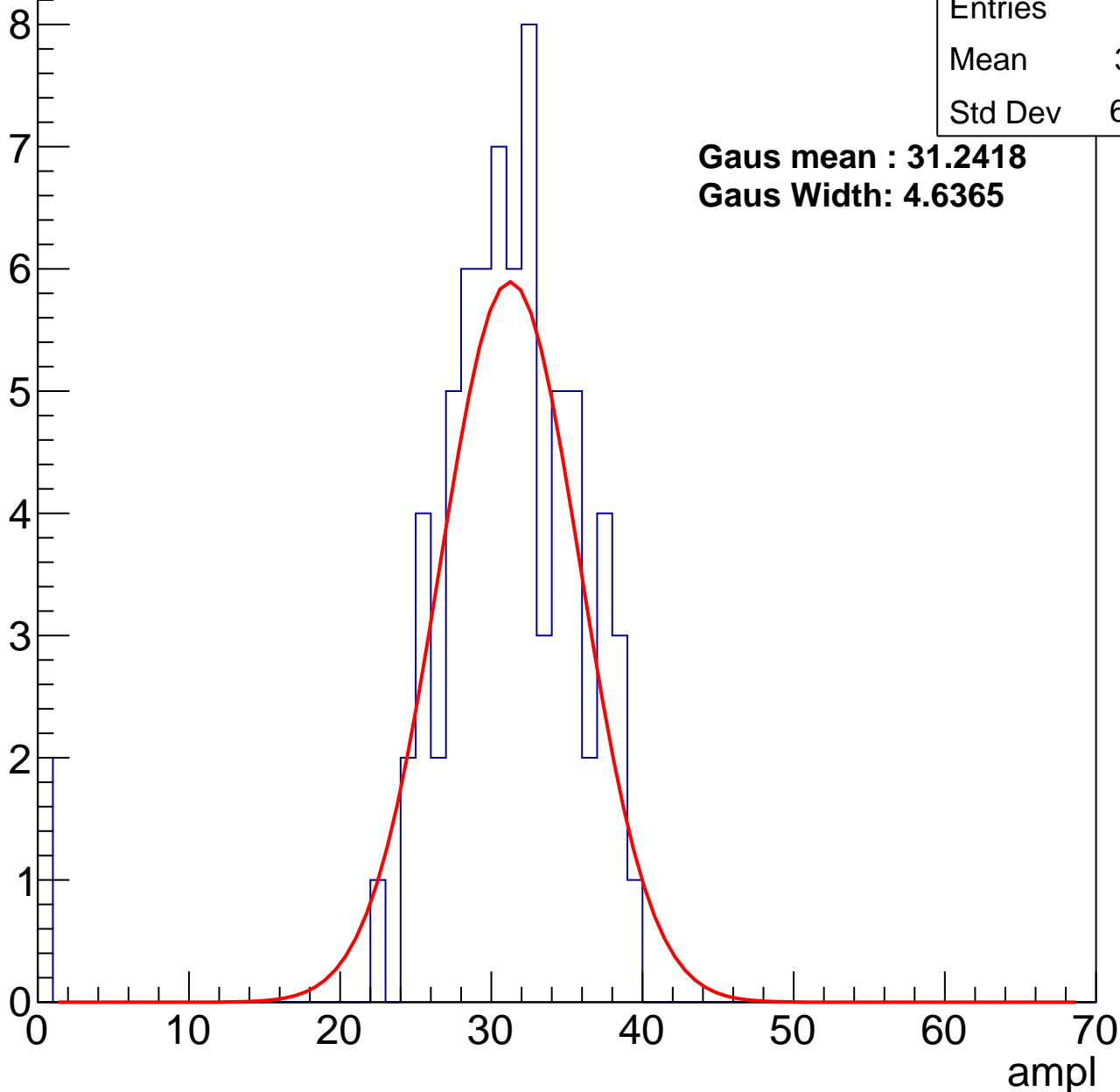
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	72
Mean	30.11
Std Dev	6.404

**Gaus mean : 31.2418**

**Gaus Width: 4.6365**



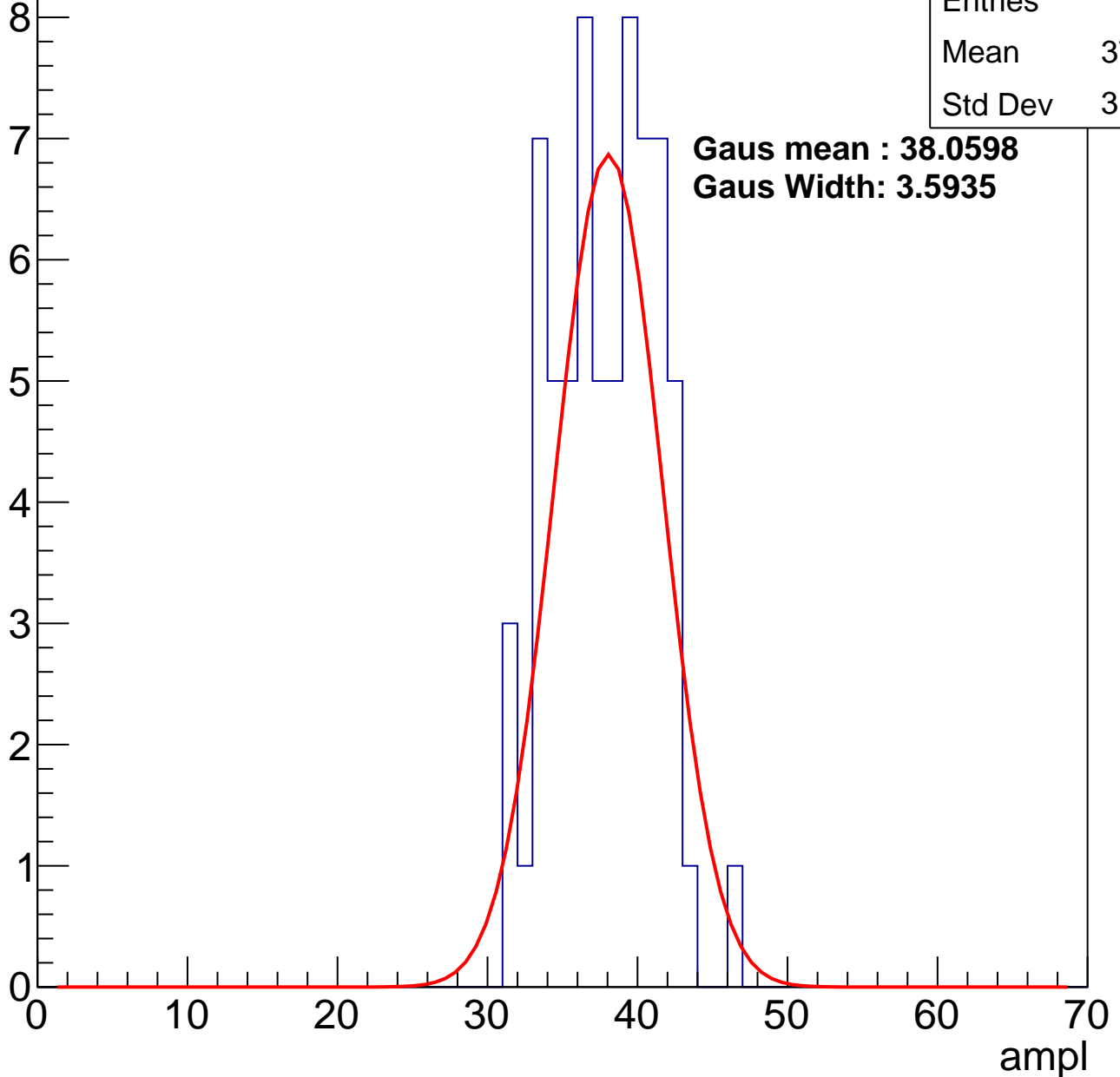
# B1L003S, U3-ch125, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	37.38
Std Dev	3.348

**Gaus mean : 38.0598**  
**Gaus Width: 3.5935**



# B1L003S, U3-ch125, adc2

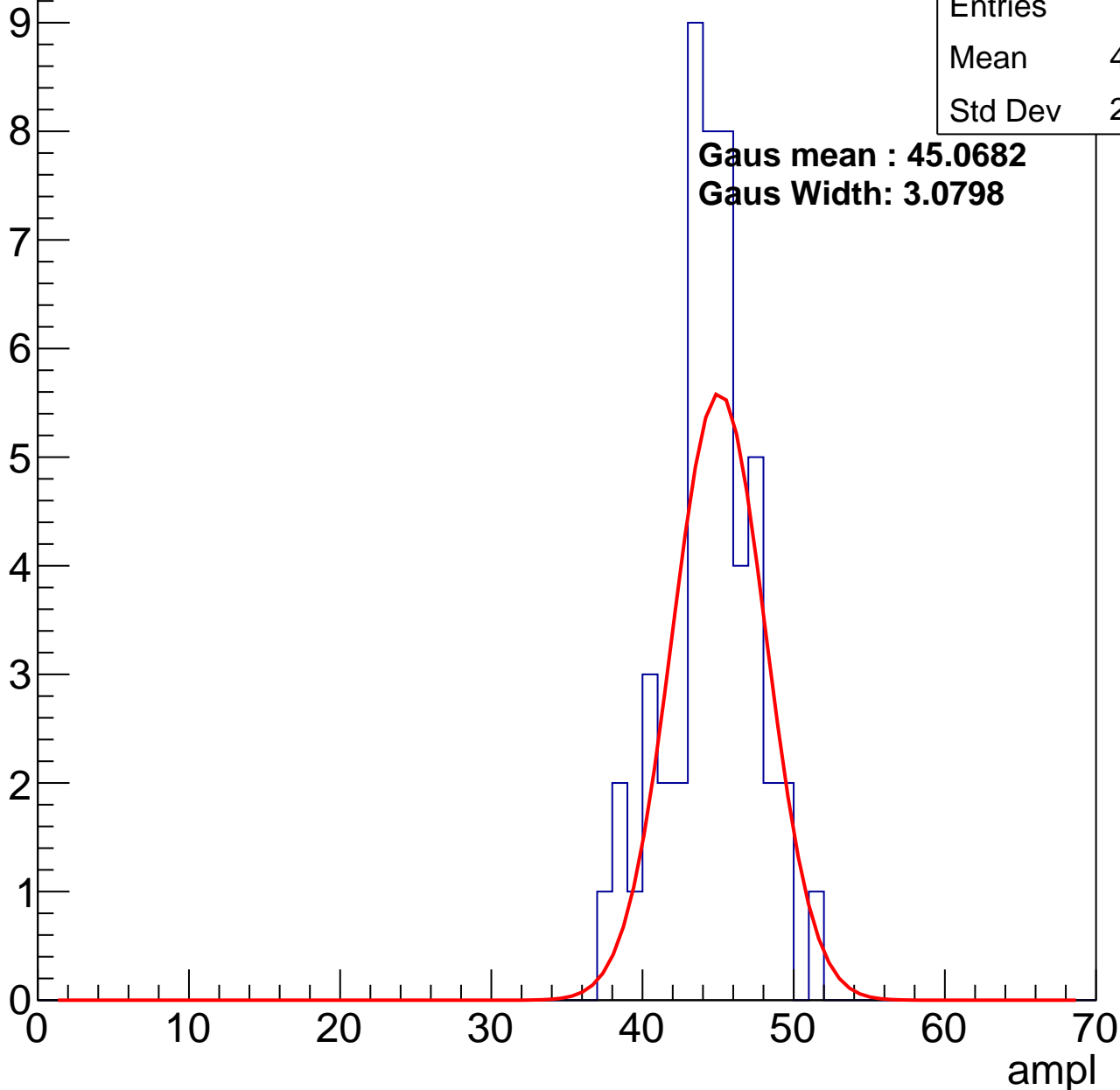
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	50
Mean	44.02
Std Dev	2.929

**Gaus mean : 45.0682**

**Gaus Width: 3.0798**

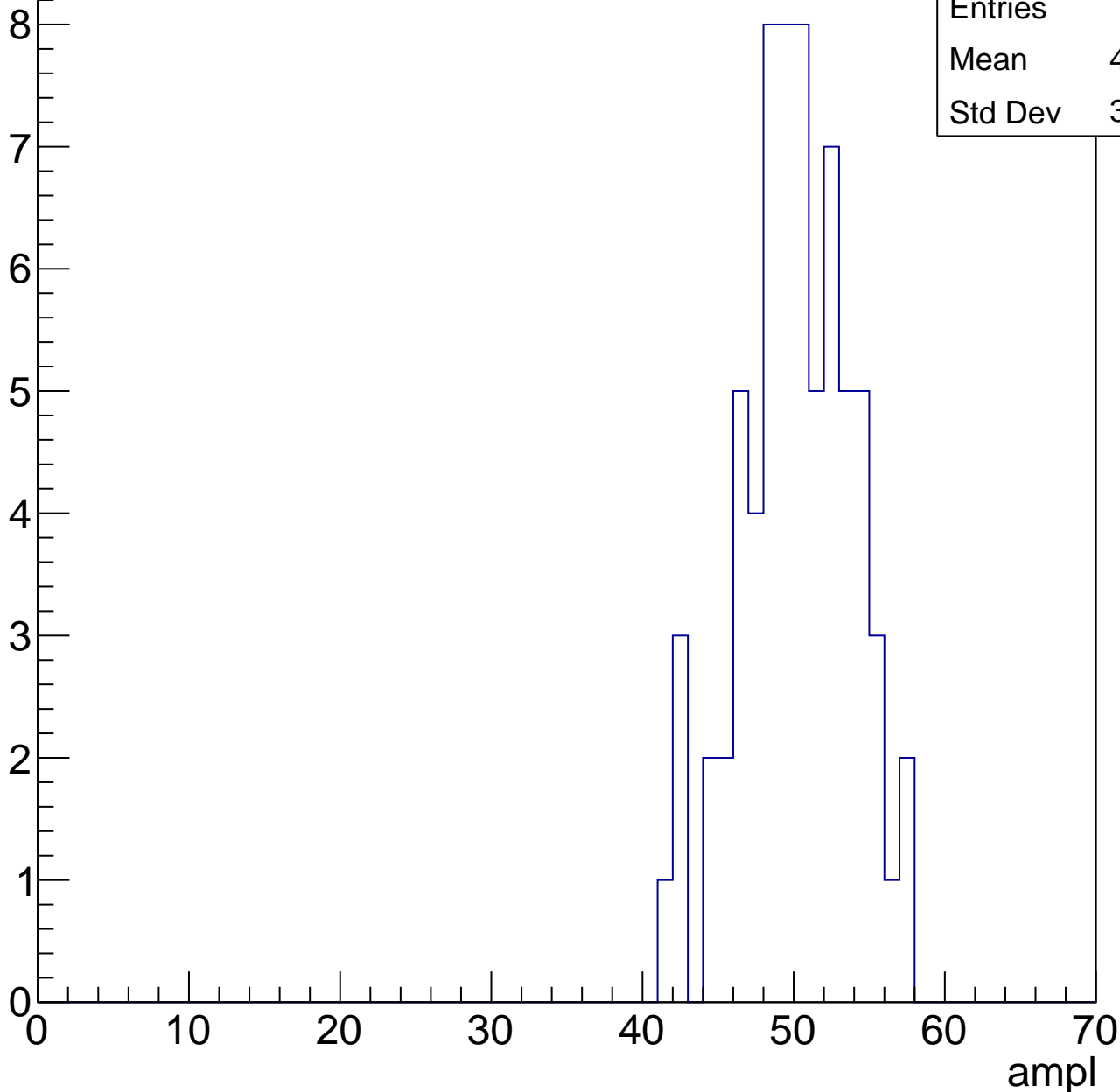


# B1L003S, U3-ch125, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	49.68
Std Dev	3.634

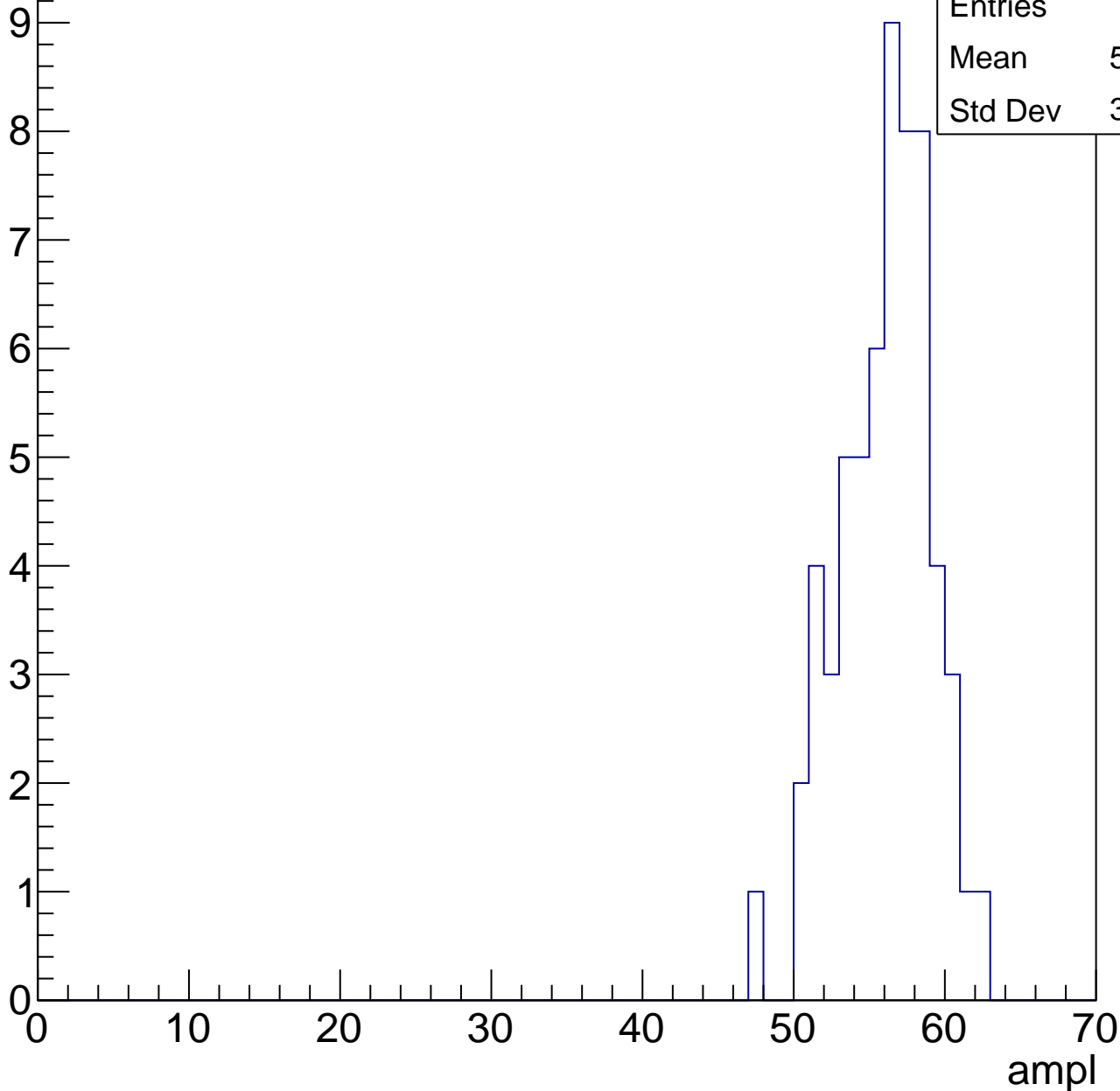


# B1L003S, U3-ch125, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	55.58
Std Dev	3.018

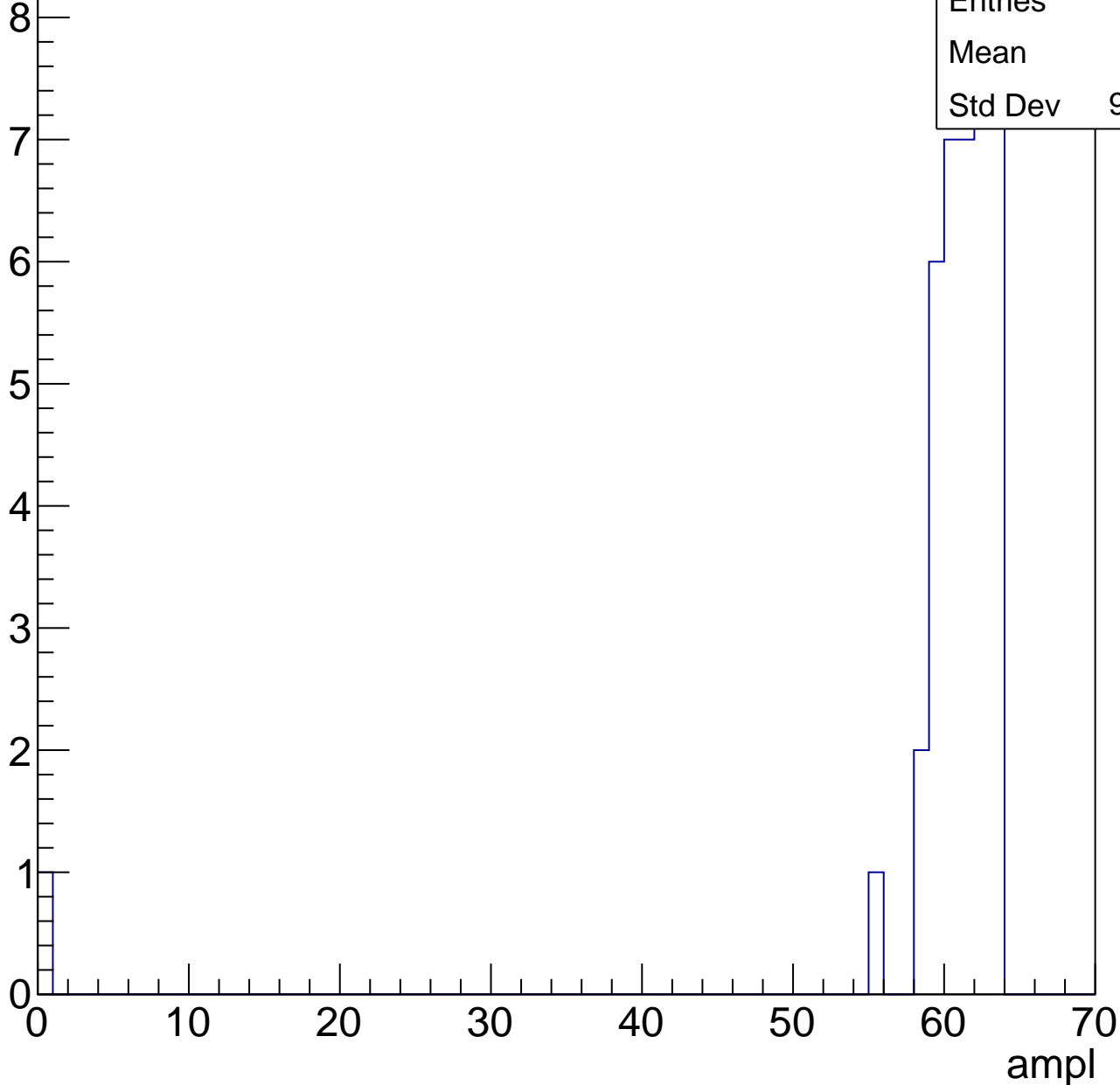


# B1L003S, U3-ch125, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

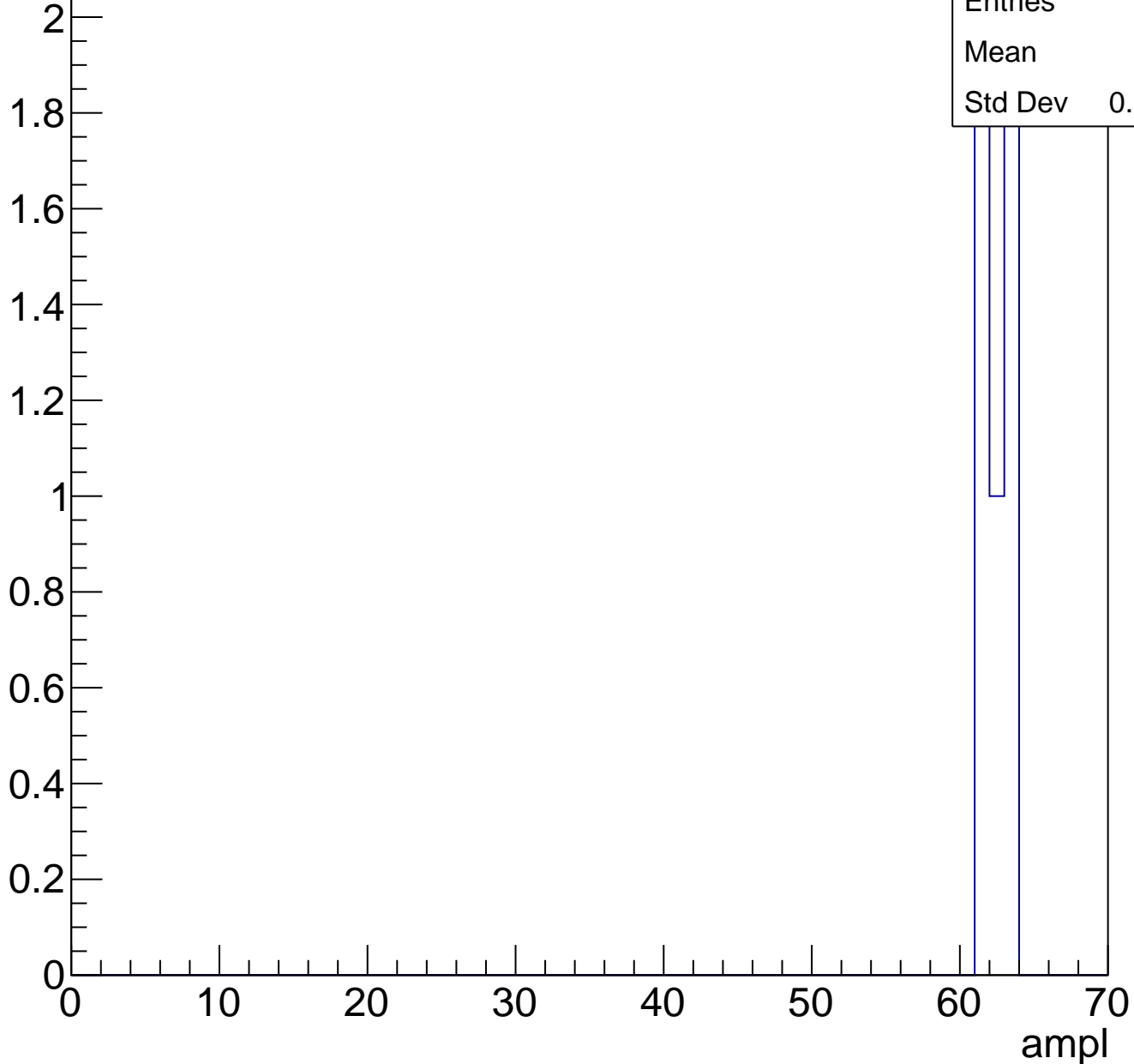
Entries	40
Mean	59.3
Std Dev	9.657



# B1L003S, U3-ch125, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U3-ch125, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L003S, U3-ch126, adc0

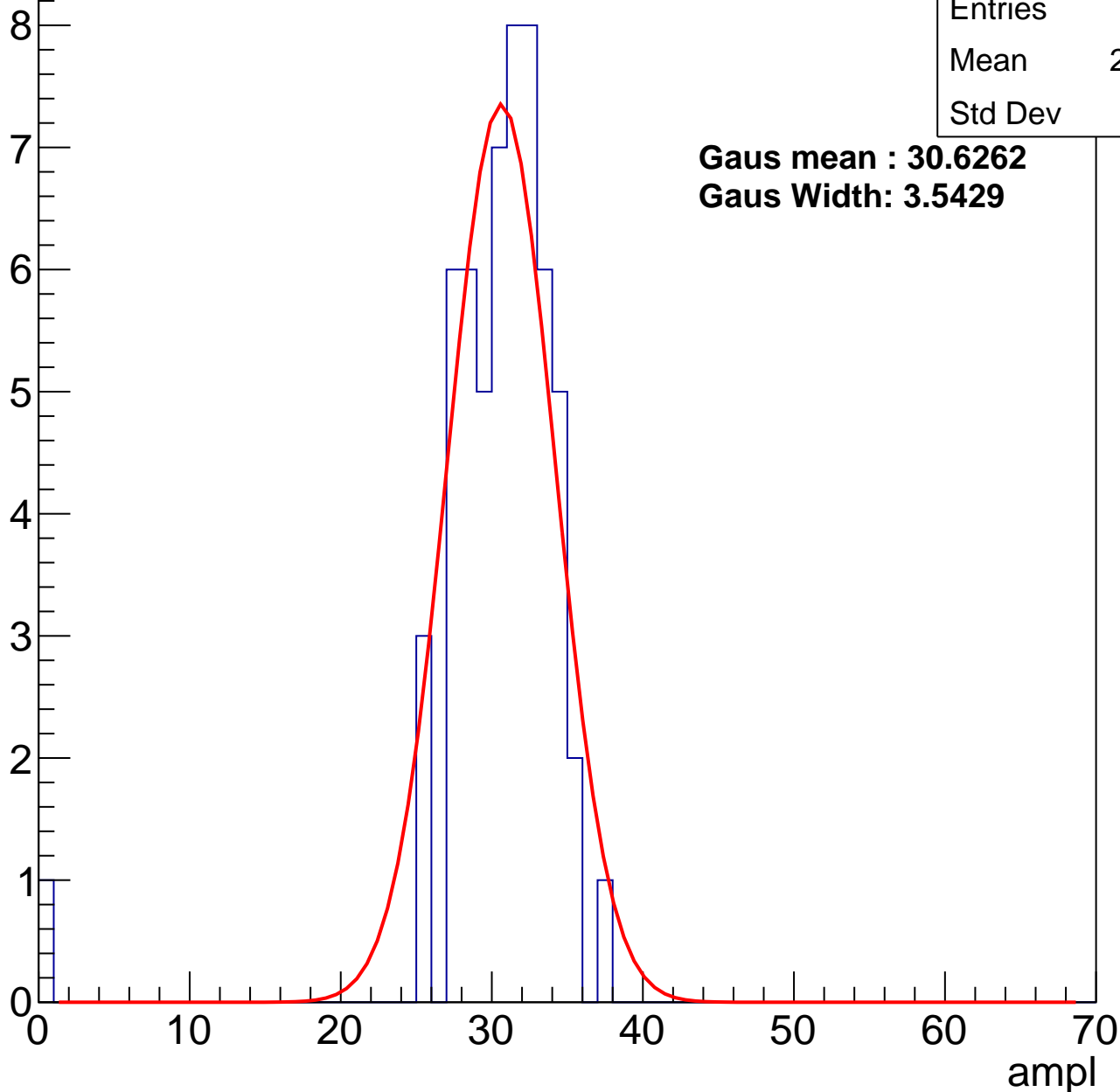
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	29.98
Std Dev	4.79

**Gaus mean : 30.6262**

**Gaus Width: 3.5429**



# B1L003S, U3-ch126, adc1

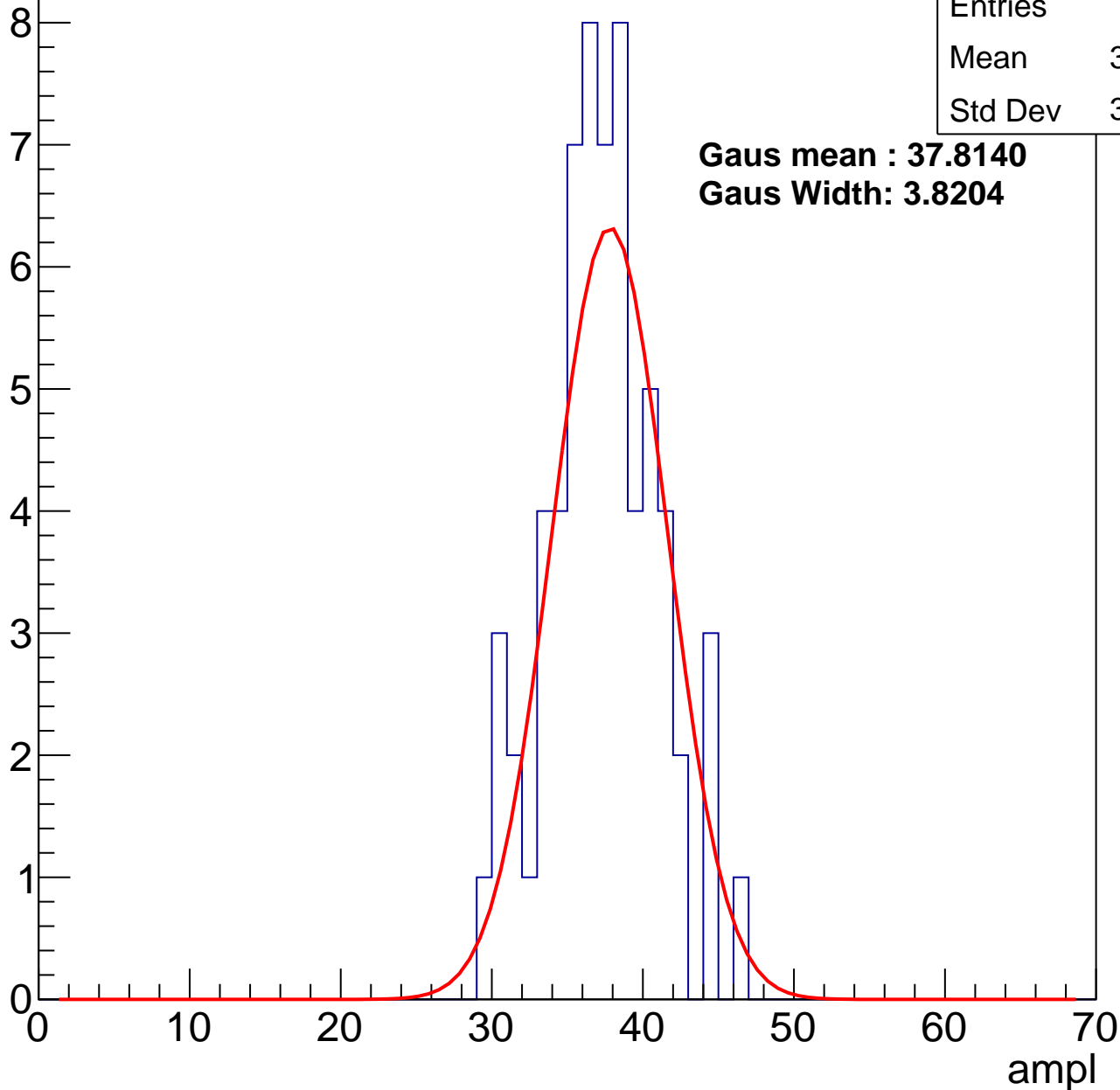
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	36.86
Std Dev	3.652

**Gaus mean : 37.8140**

**Gaus Width: 3.8204**



# B1L003S, U3-ch126, adc2

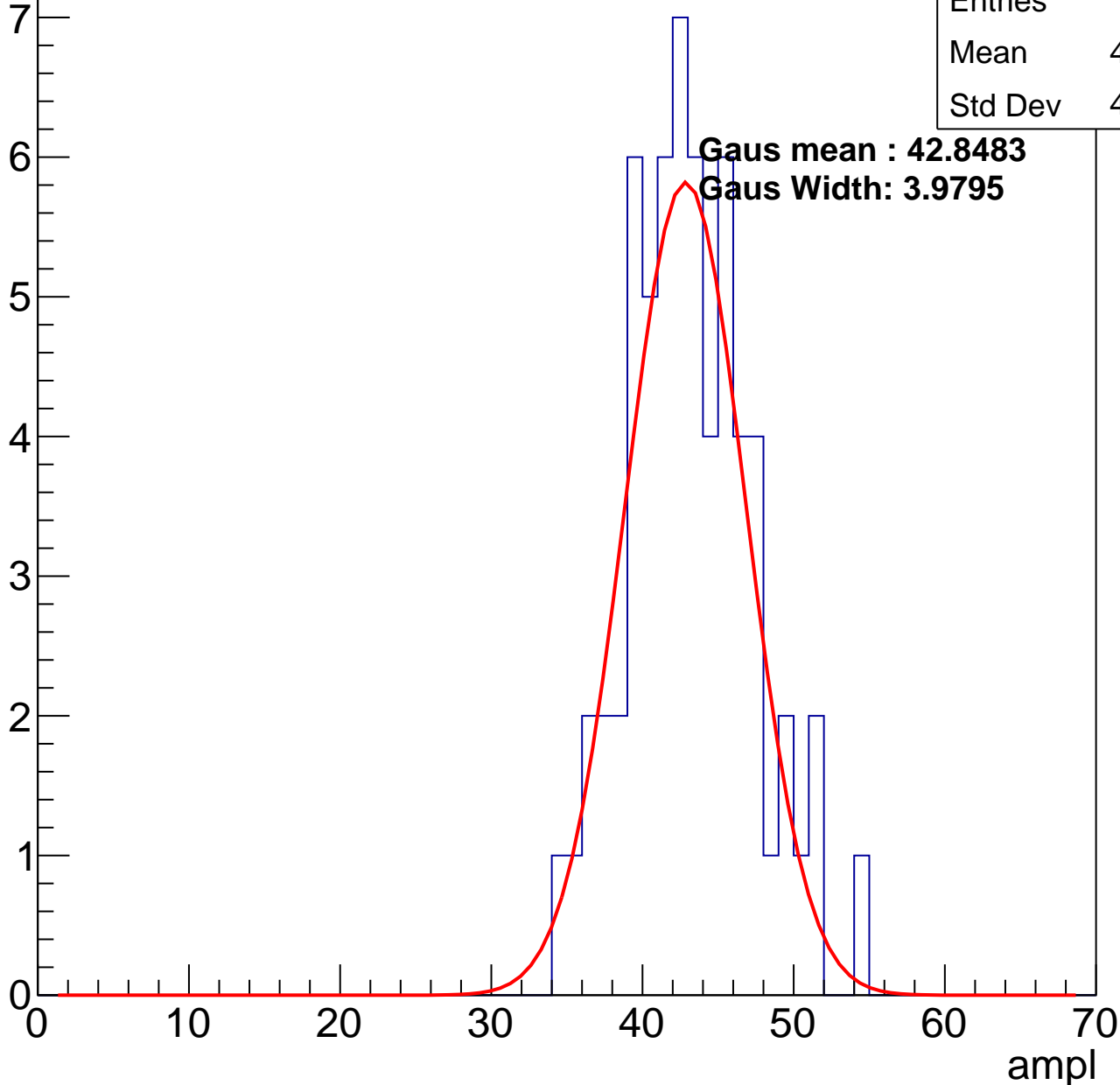
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	42.75
Std Dev	4.094

**Gaus mean : 42.8483**

**Gaus Width: 3.9795**

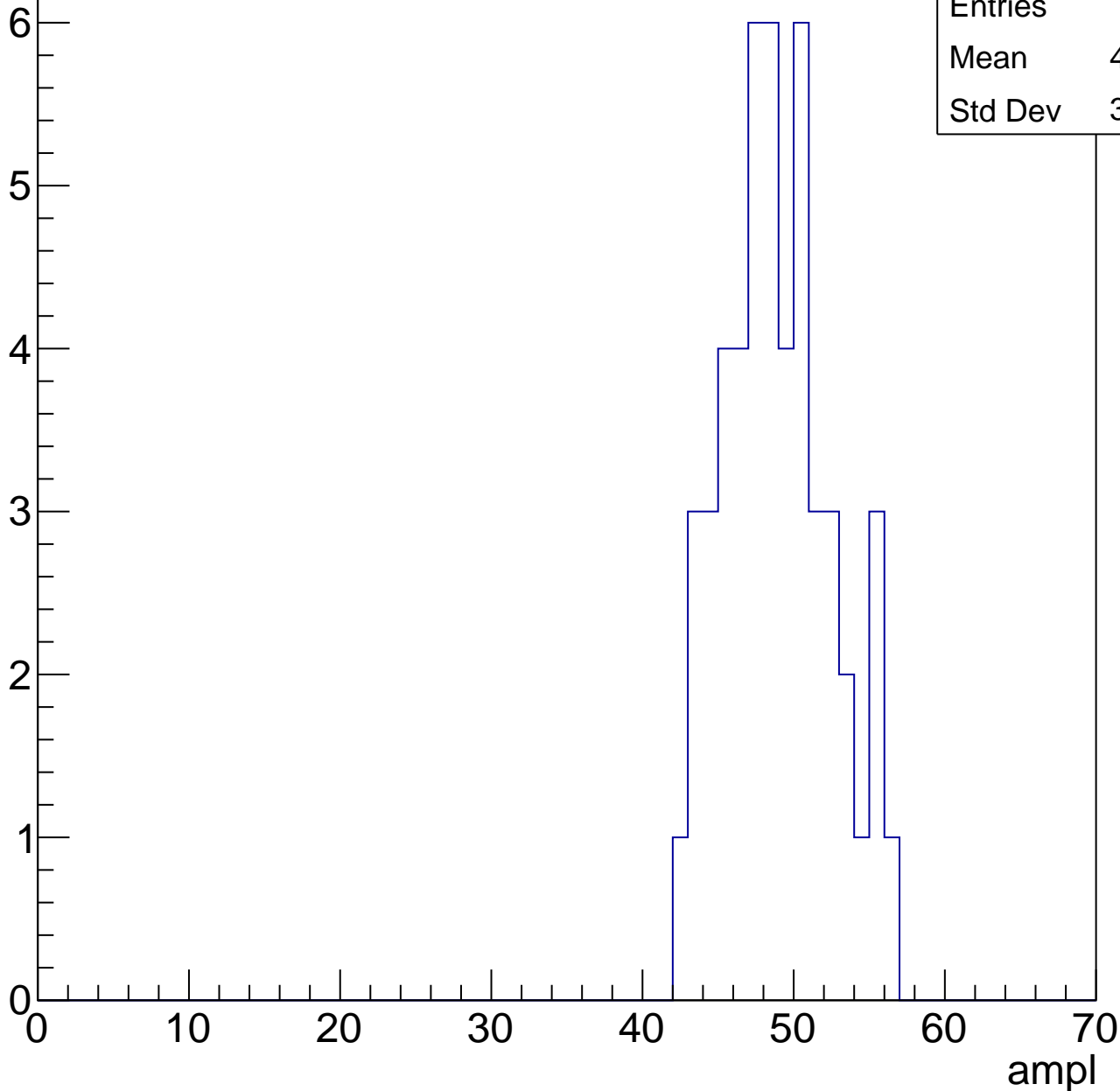


# B1L003S, U3-ch126, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	50
Mean	48.46
Std Dev	3.483

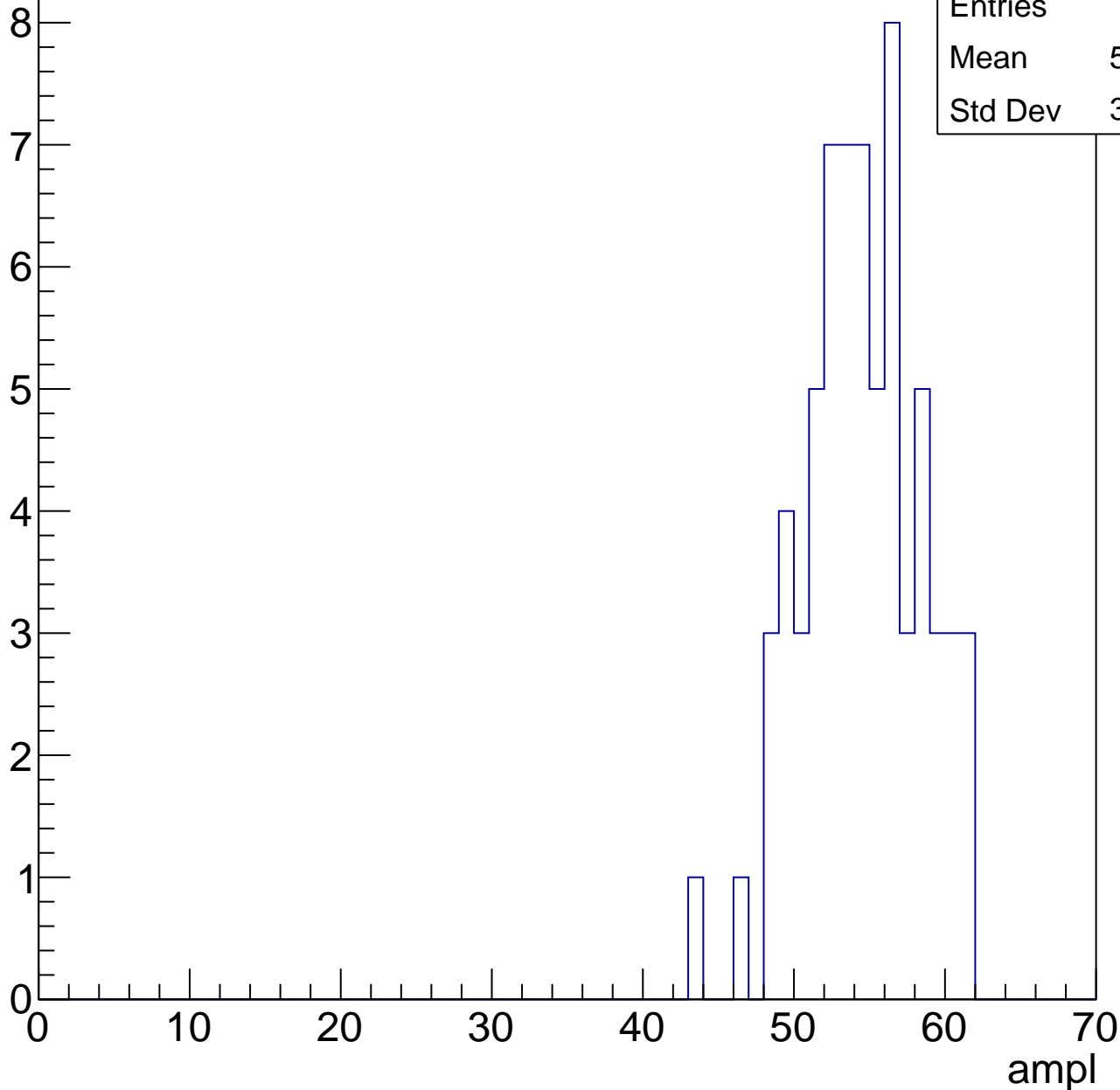


# B1L003S, U3-ch126, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	53.99
Std Dev	3.825

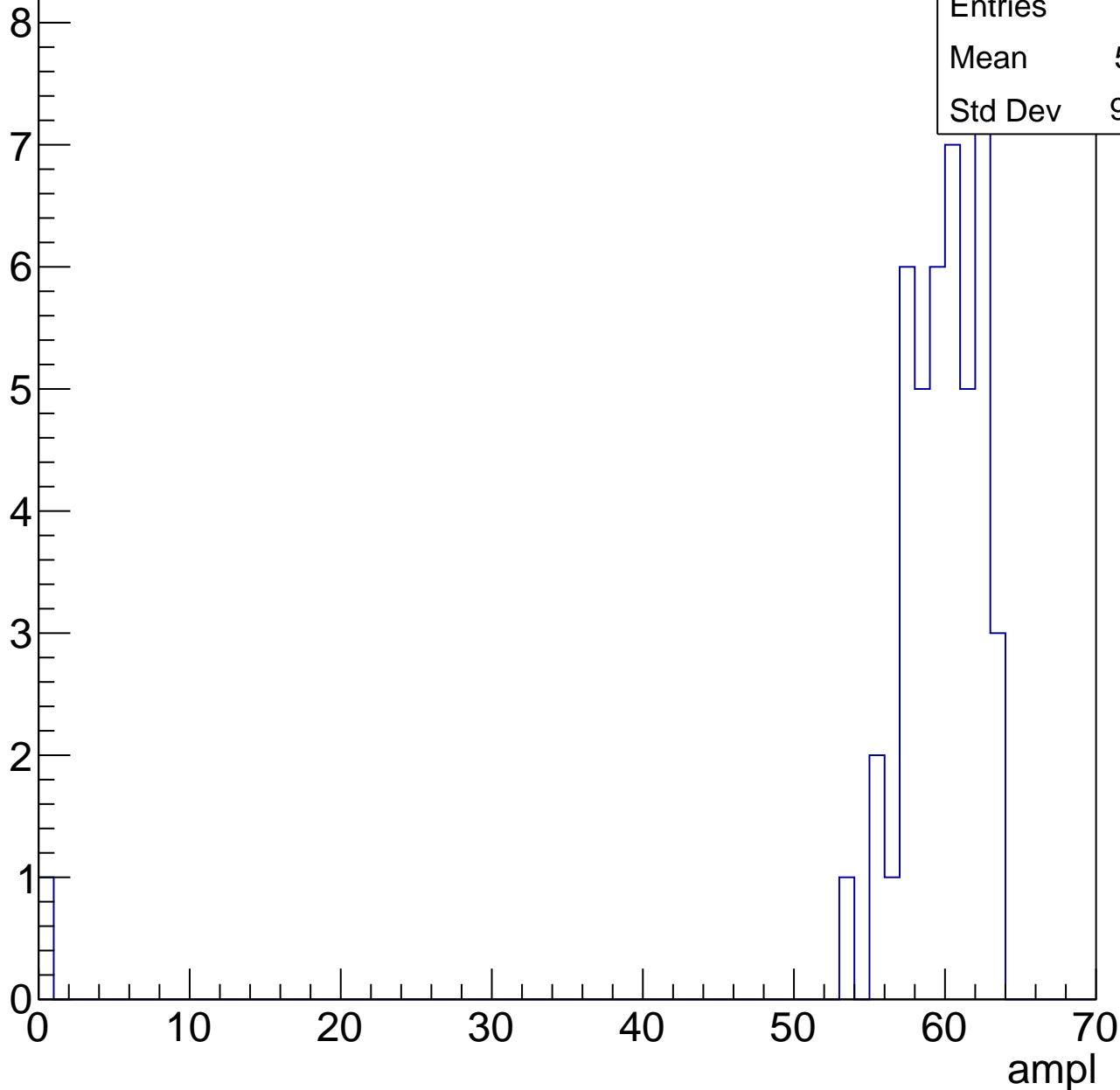


# B1L003S, U3-ch126, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	45
Mean	58.11
Std Dev	9.066

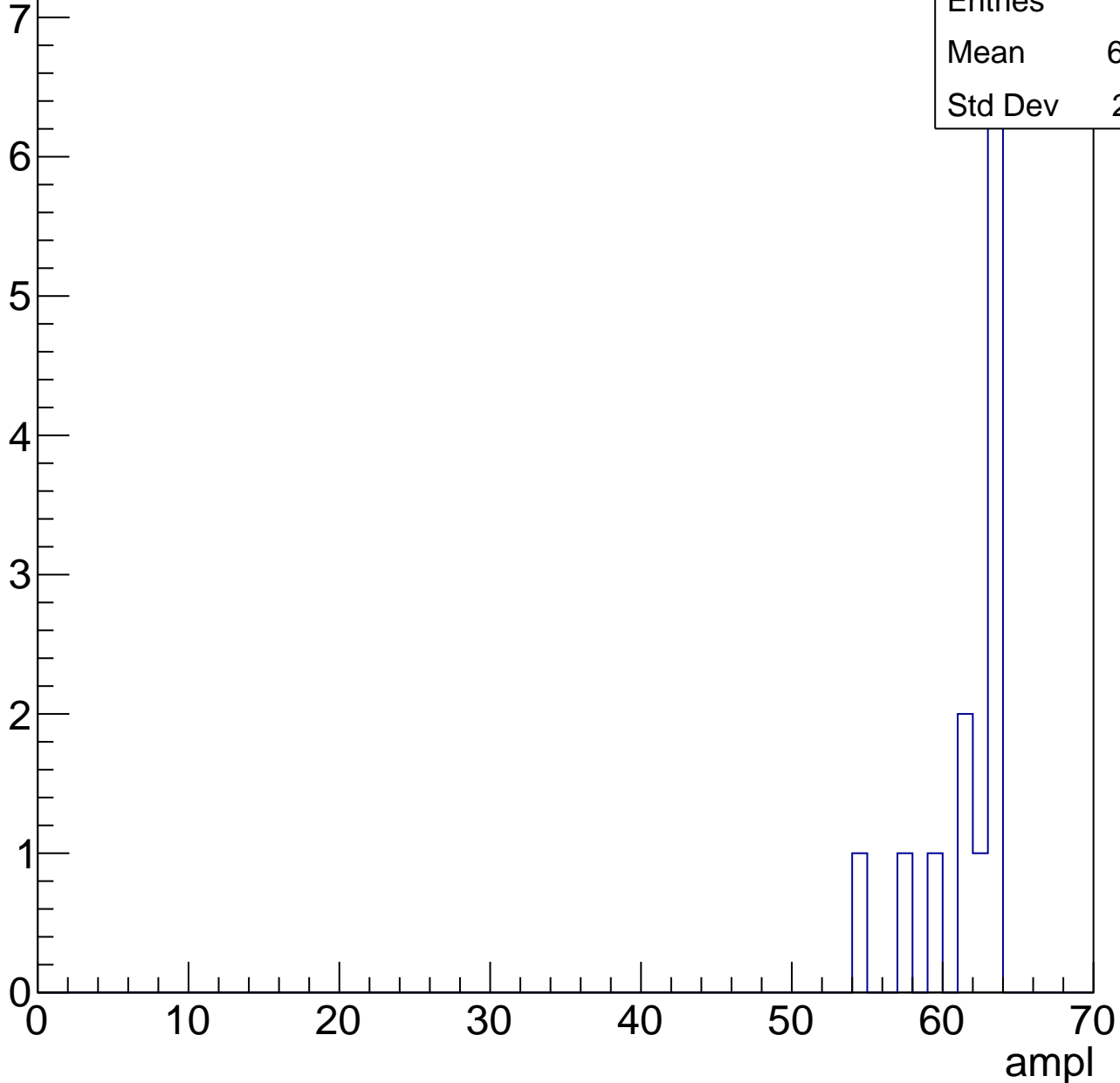


# B1L003S, U3-ch126, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	13
Mean	61.15
Std Dev	2.741

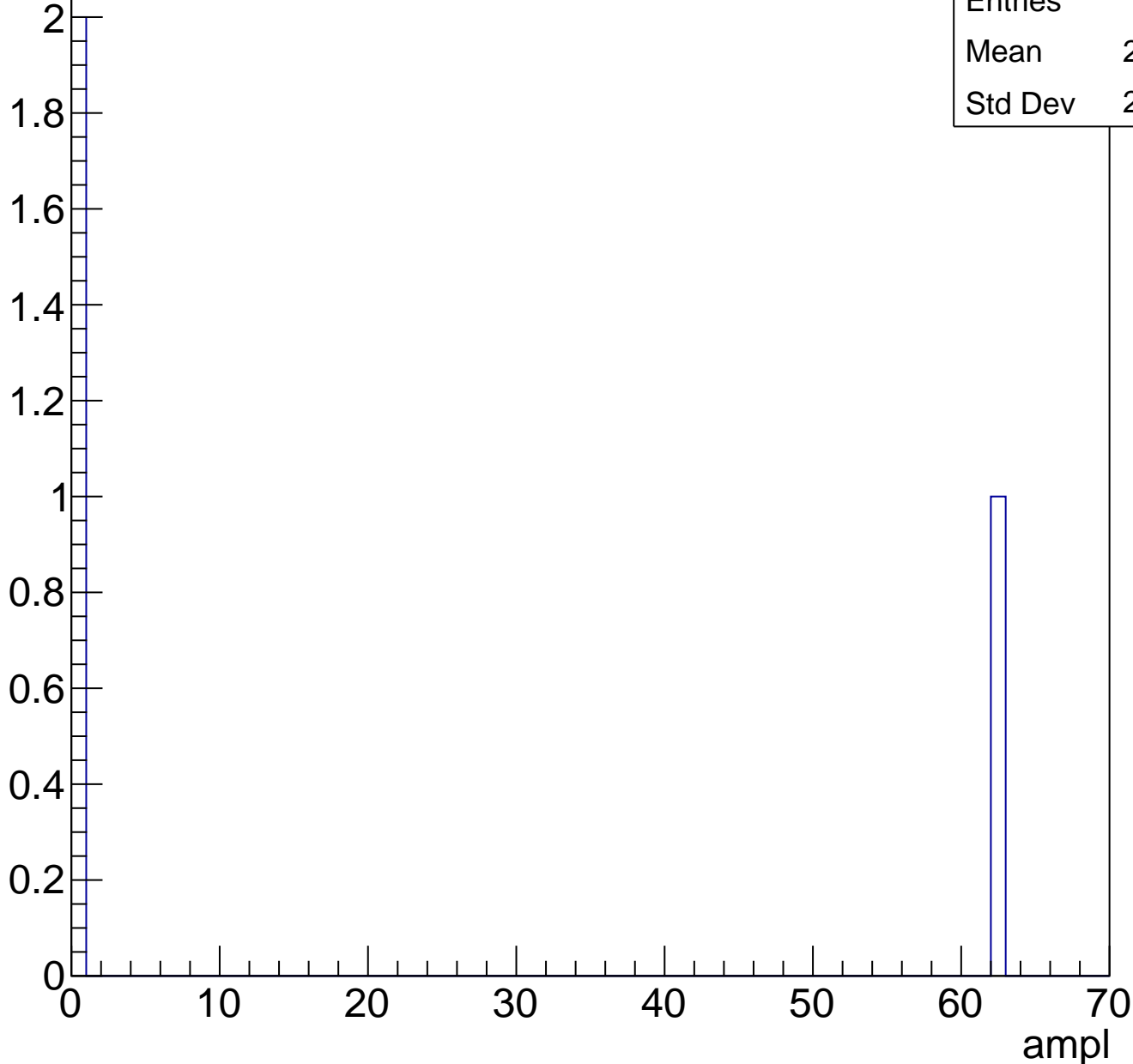




# B1L003S, U3-ch126, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	3
Mean	20.67
Std Dev	29.23

# B1L003S, U3-ch127, adc0

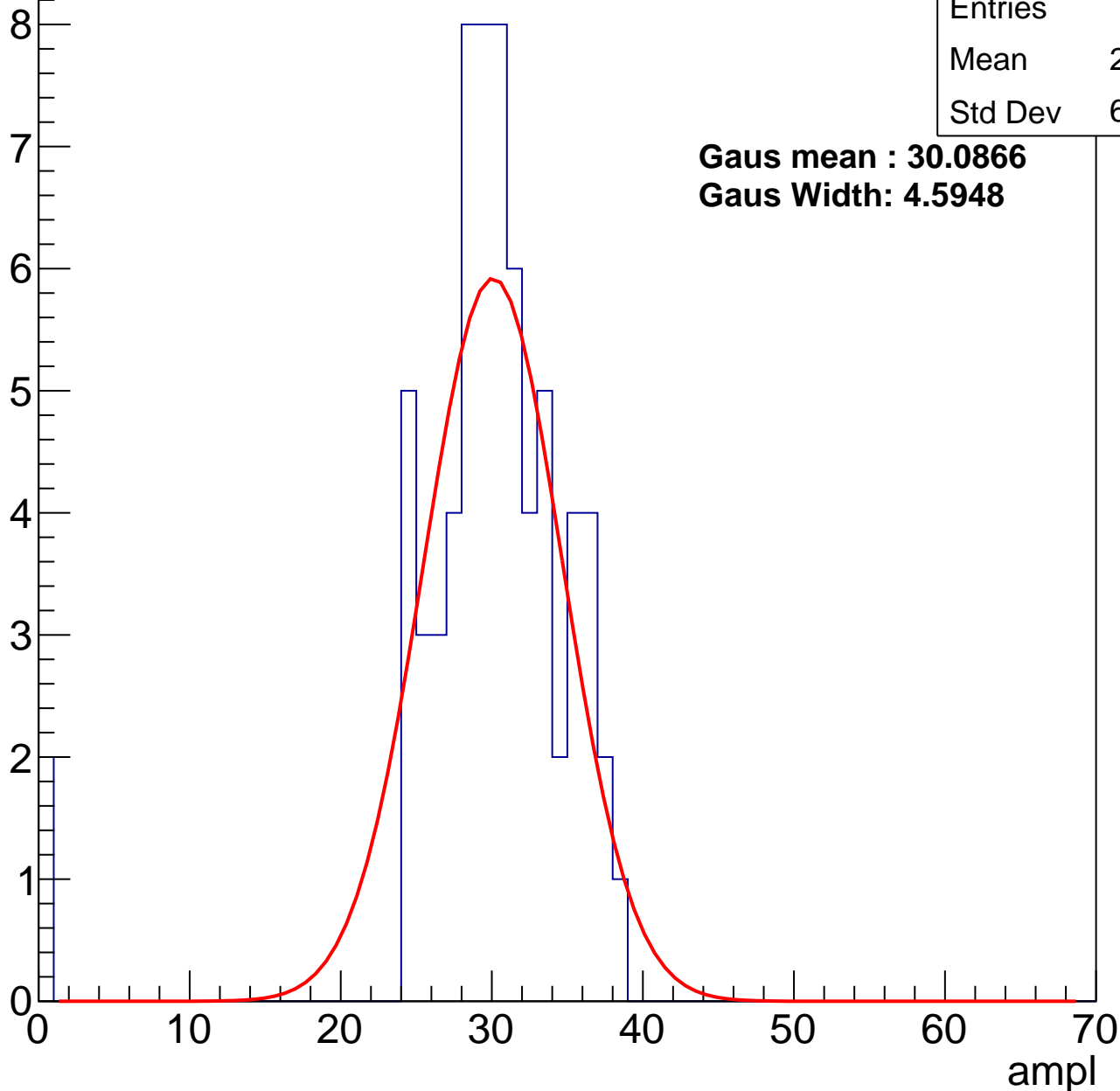
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	29.28
Std Dev	6.195

**Gaus mean : 30.0866**

**Gaus Width: 4.5948**



# B1L003S, U3-ch127, adc1

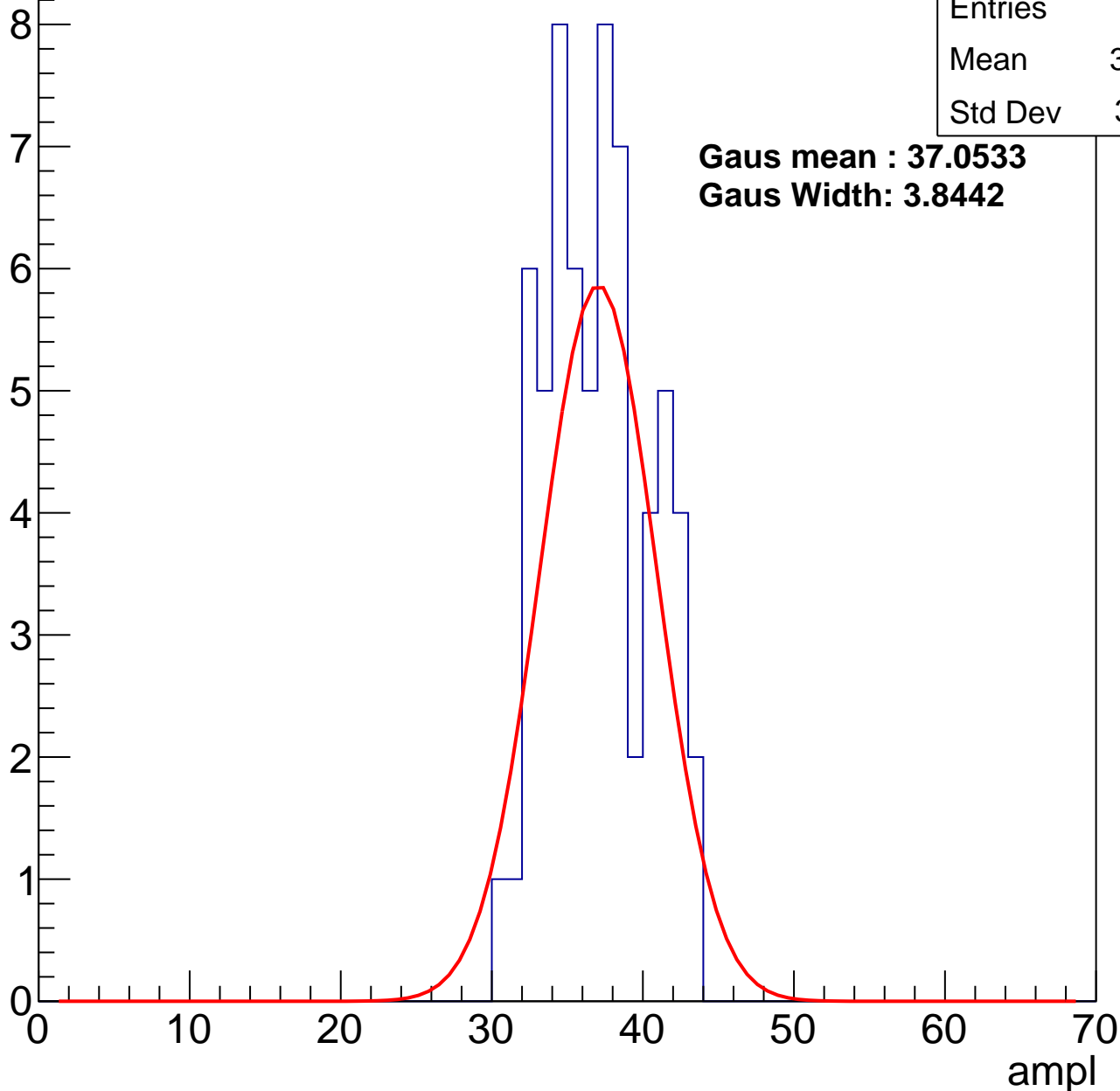
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	36.55
Std Dev	3.321

**Gaus mean : 37.0533**

**Gaus Width: 3.8442**



# B1L003S, U3-ch127, adc2

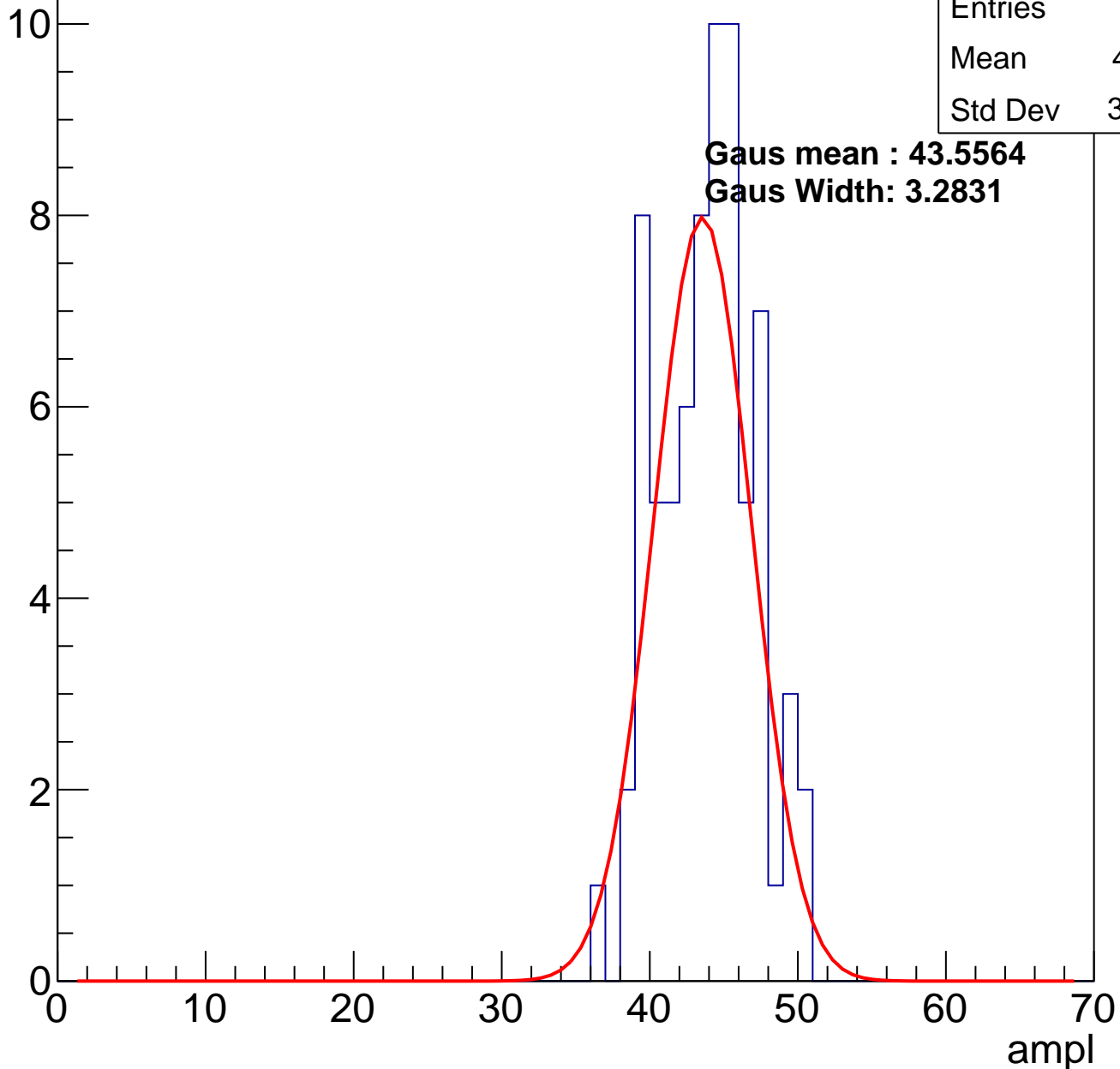
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	73
Mean	43.41
Std Dev	3.149

**Gaus mean : 43.5564**

**Gaus Width: 3.2831**

Entry

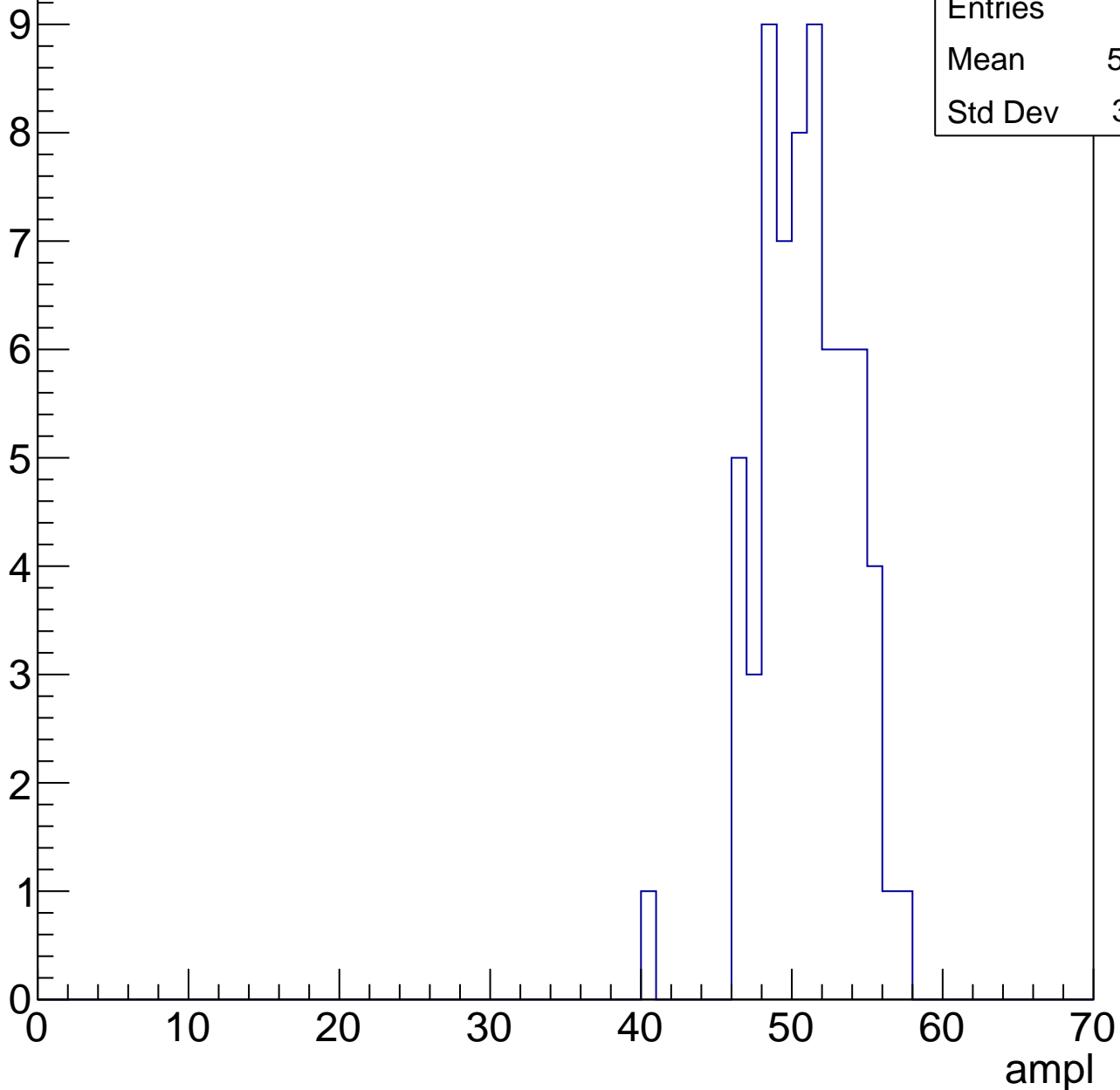


# B1L003S, U3-ch127, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	50.48
Std Dev	3.021

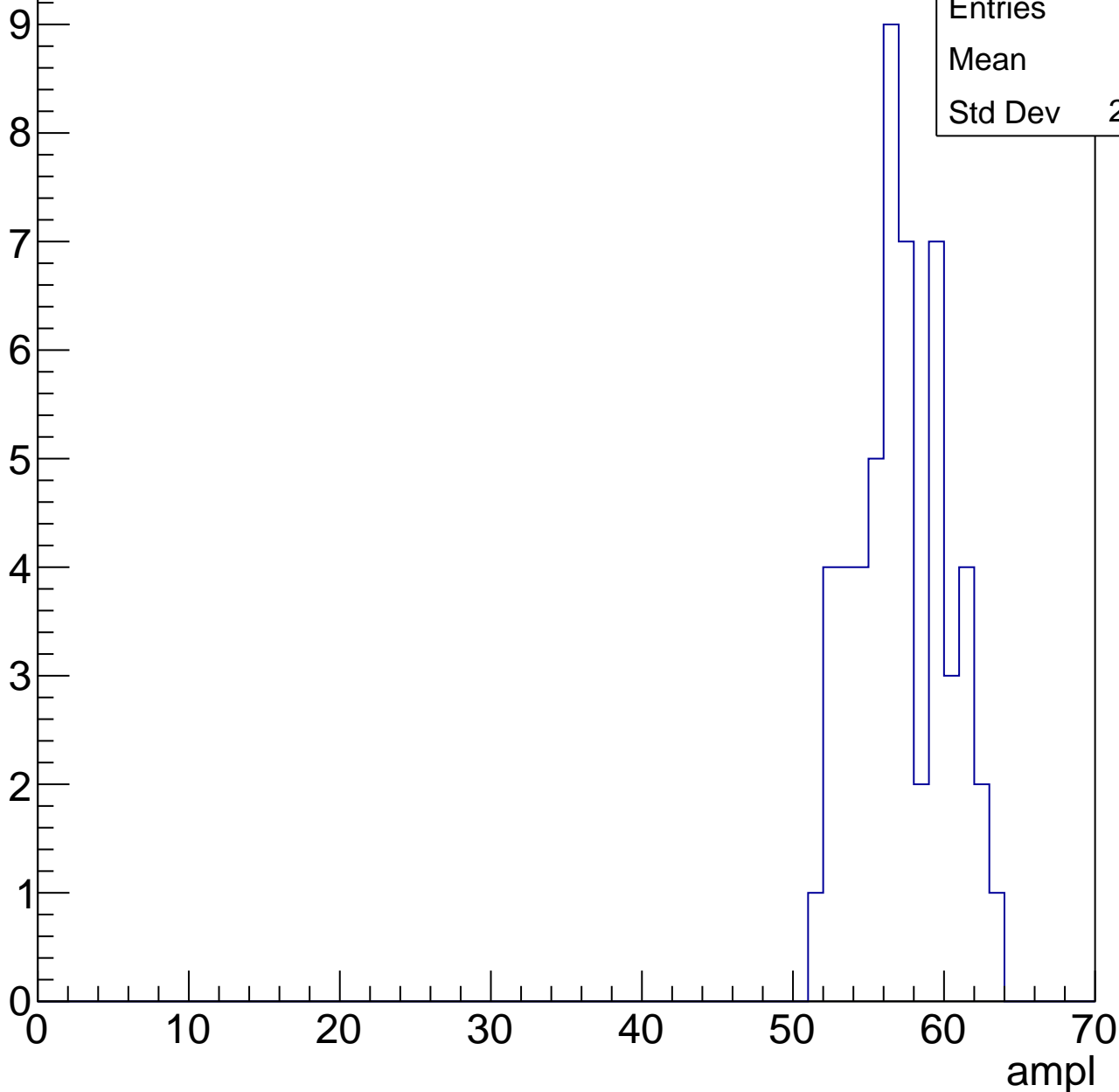


# B1L003S, U3-ch127, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	56.7
Std Dev	2.969

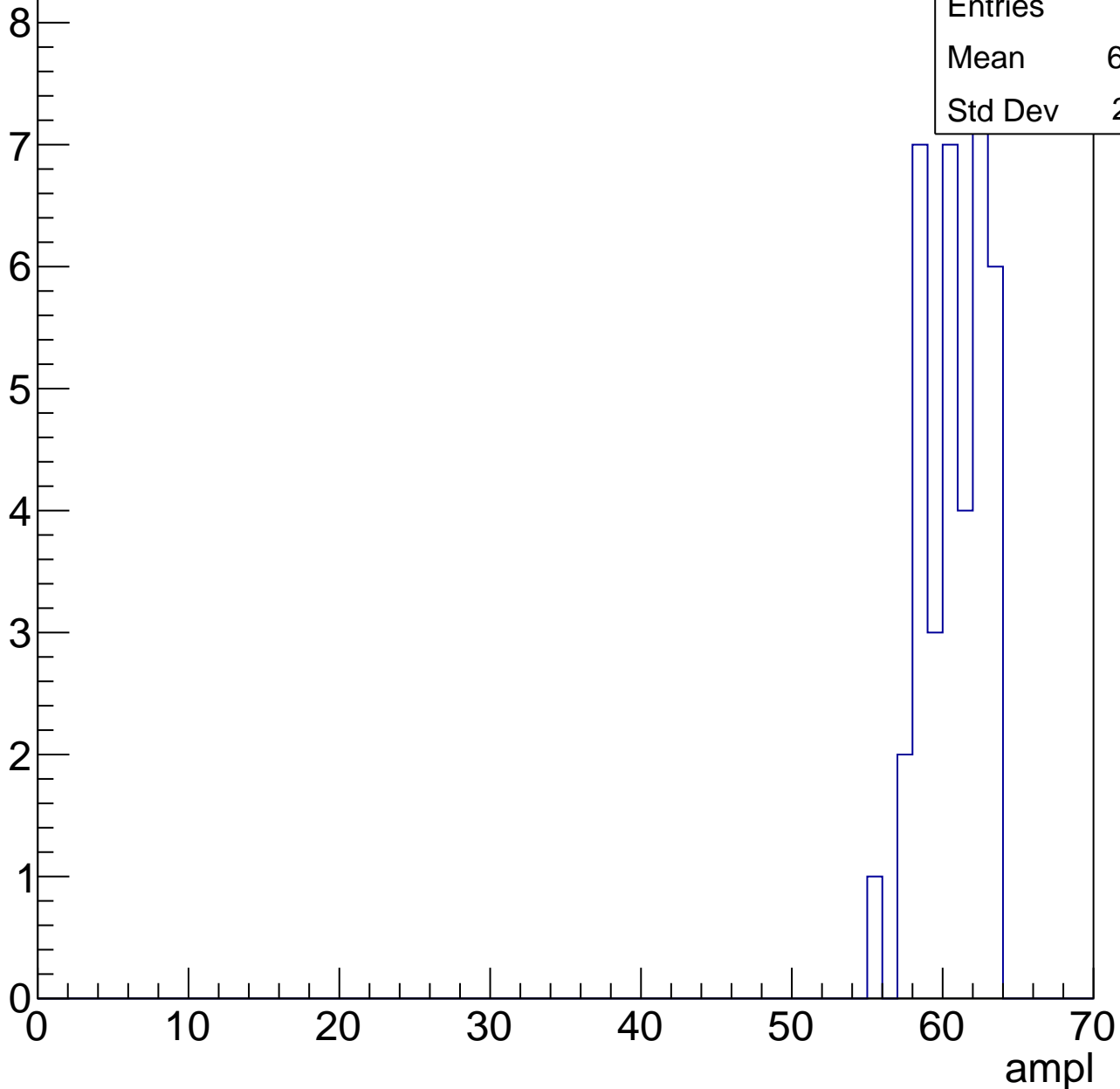


# B1L003S, U3-ch127, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

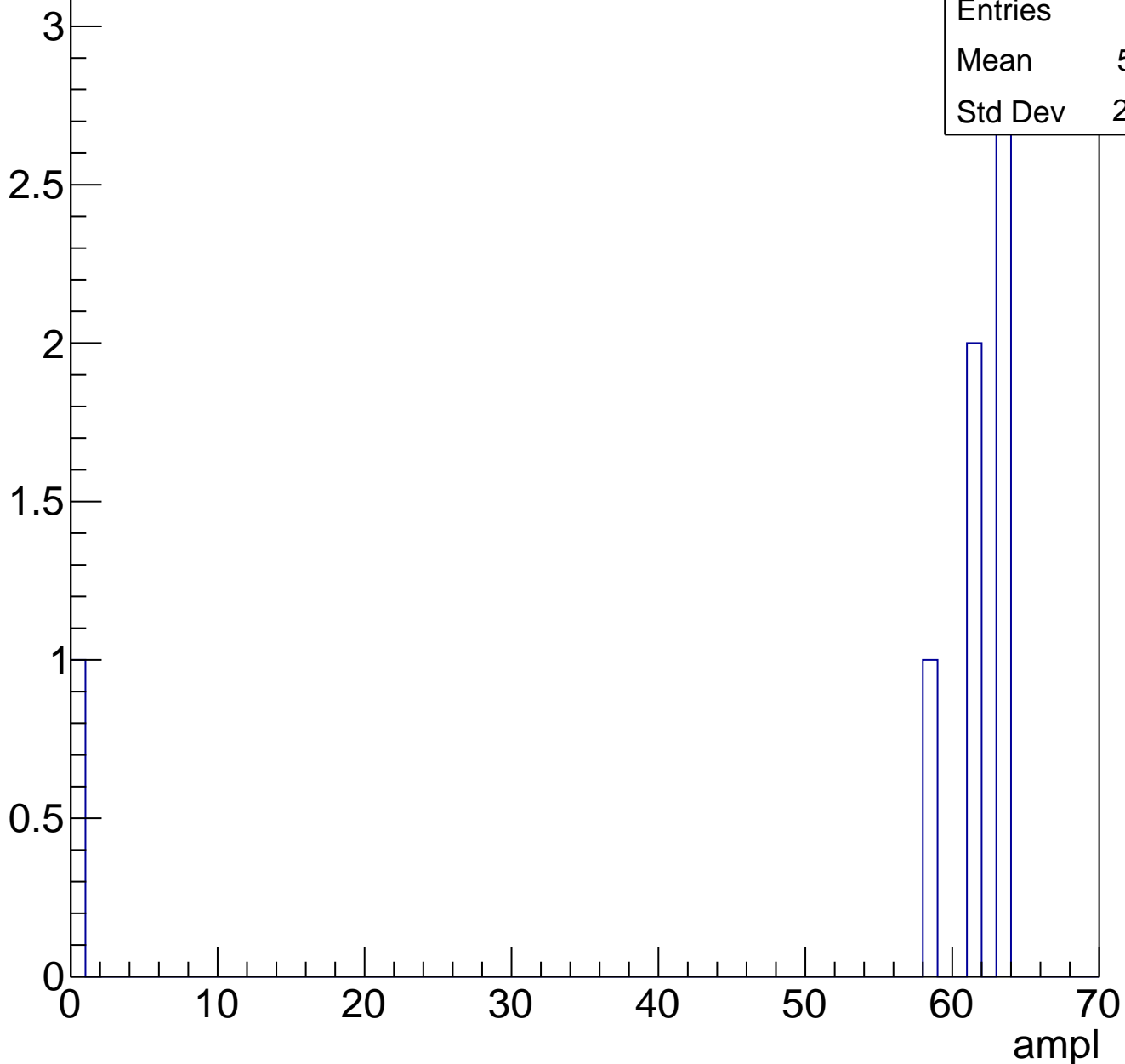
Entries	38
Mean	60.26
Std Dev	2.061



# B1L003S, U3-ch127, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	7
Mean	52.71
Std Dev	21.59



# B1L003S, U3-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U3-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

