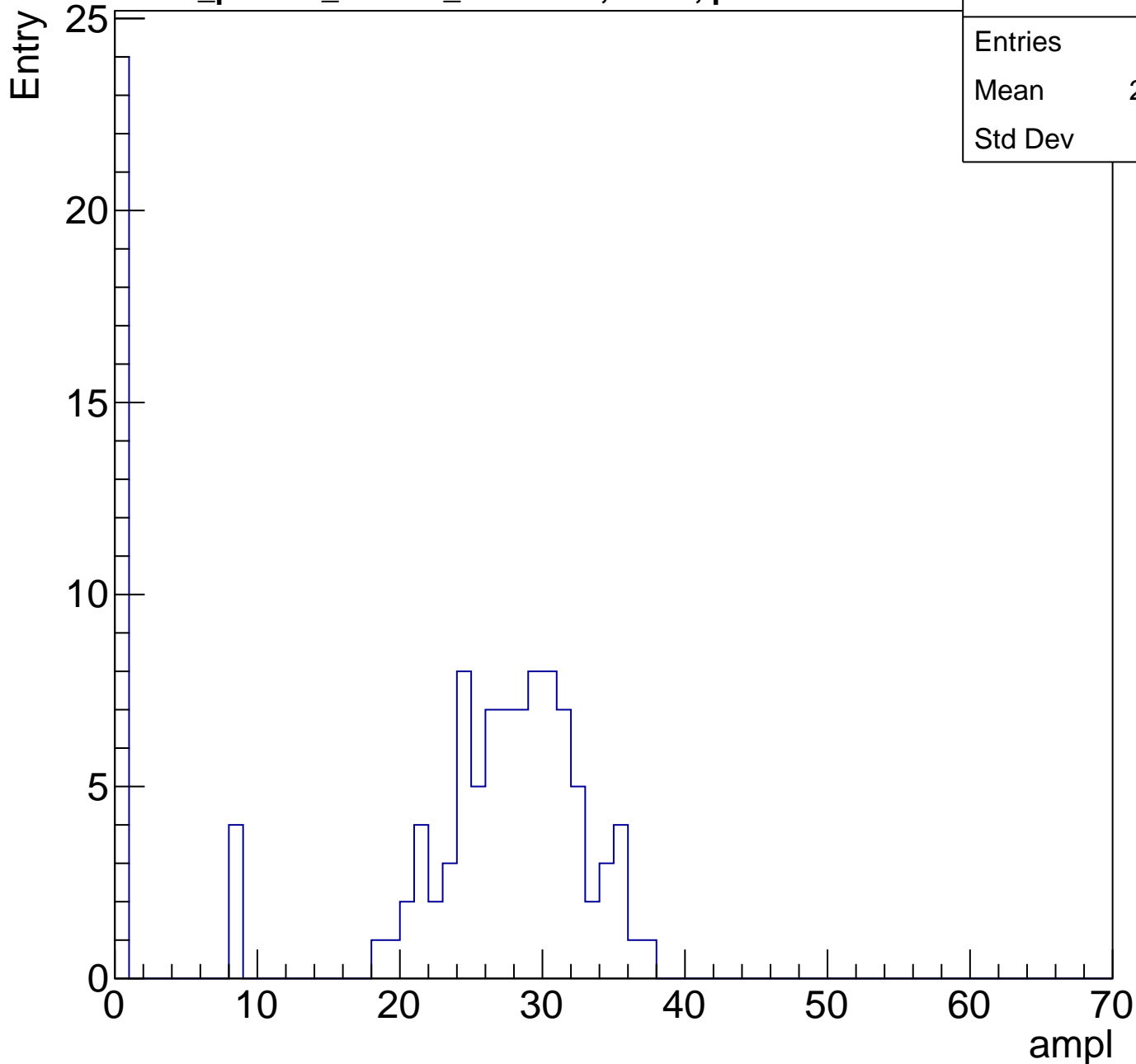


B1L103S, U12-ch0, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	114
Mean	21.23
Std Dev	12.11

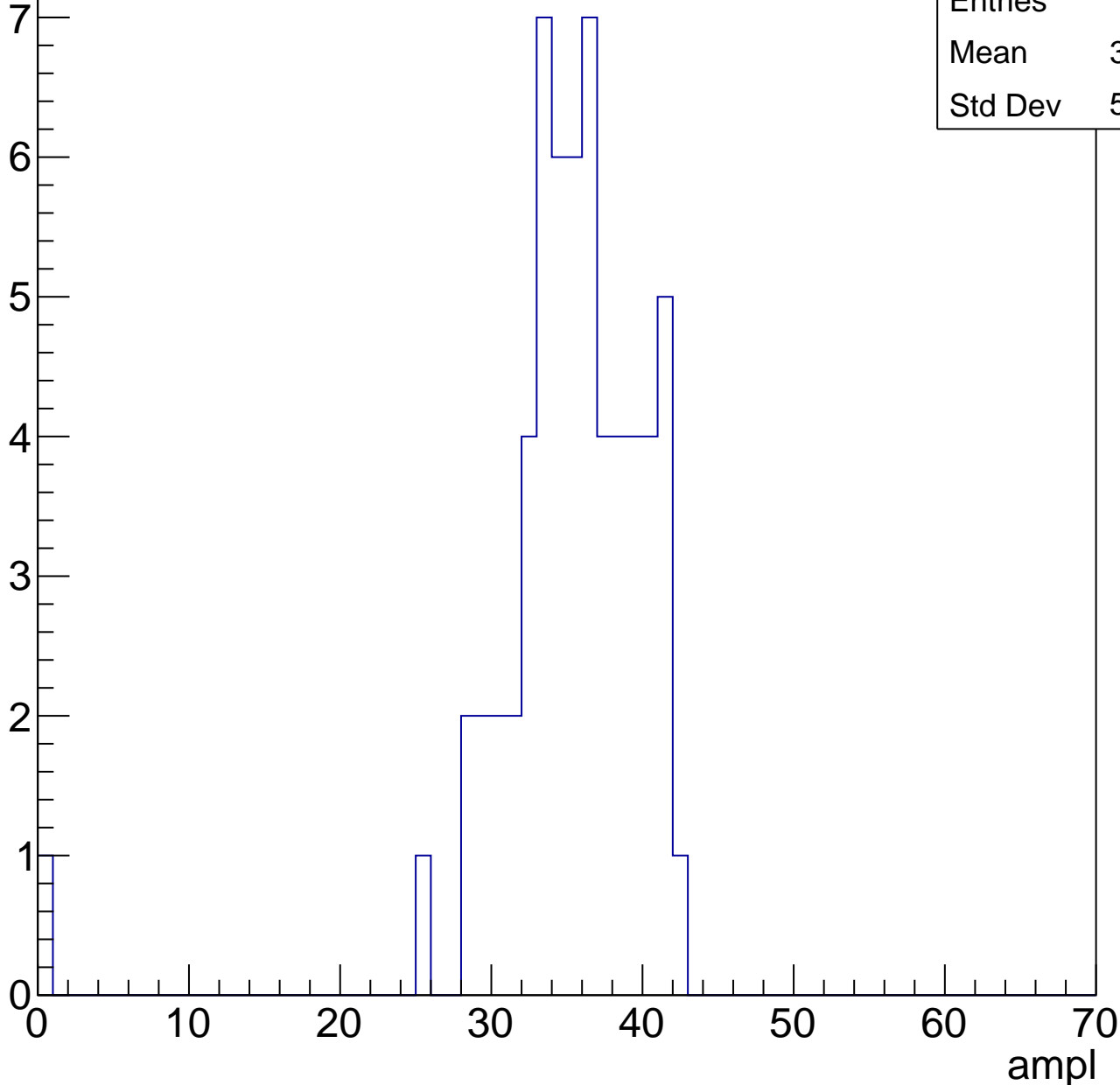


B1L103S, U12-ch0, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	34.66
Std Dev	5.809

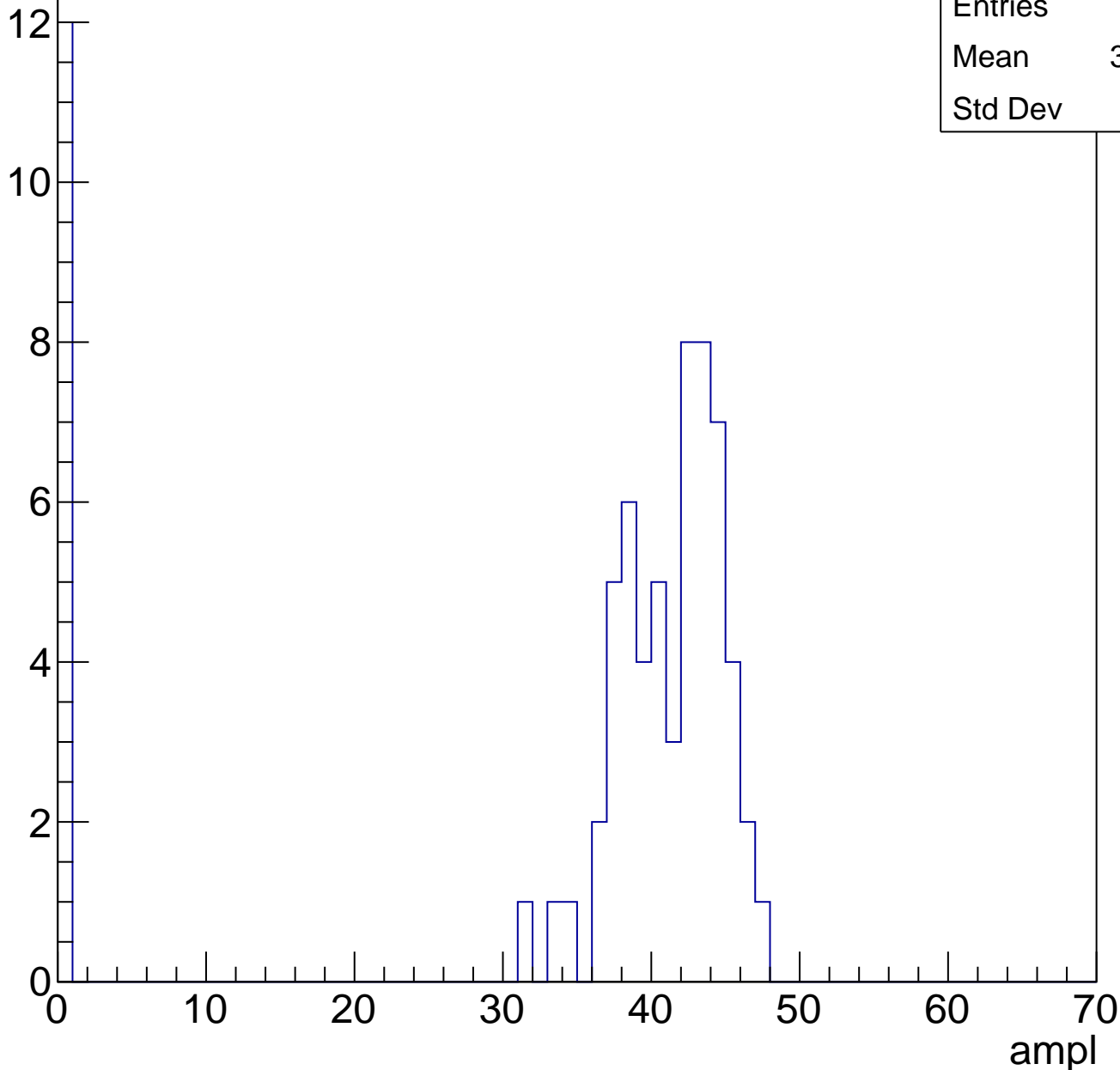


B1L103S, U12-ch0, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	70
Mean	33.84
Std Dev	15.7

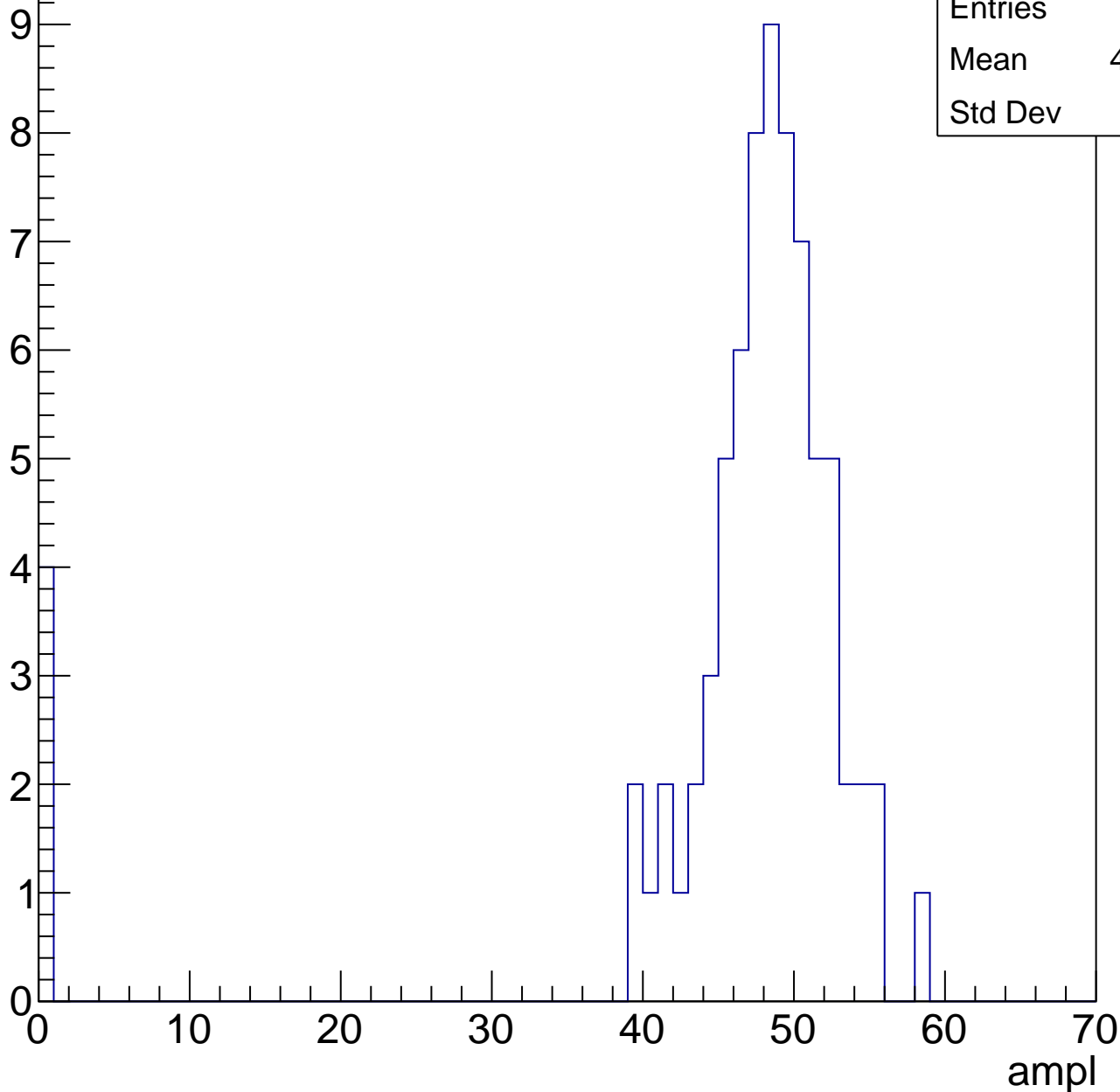
Entry



B1L103S, U12-ch0, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

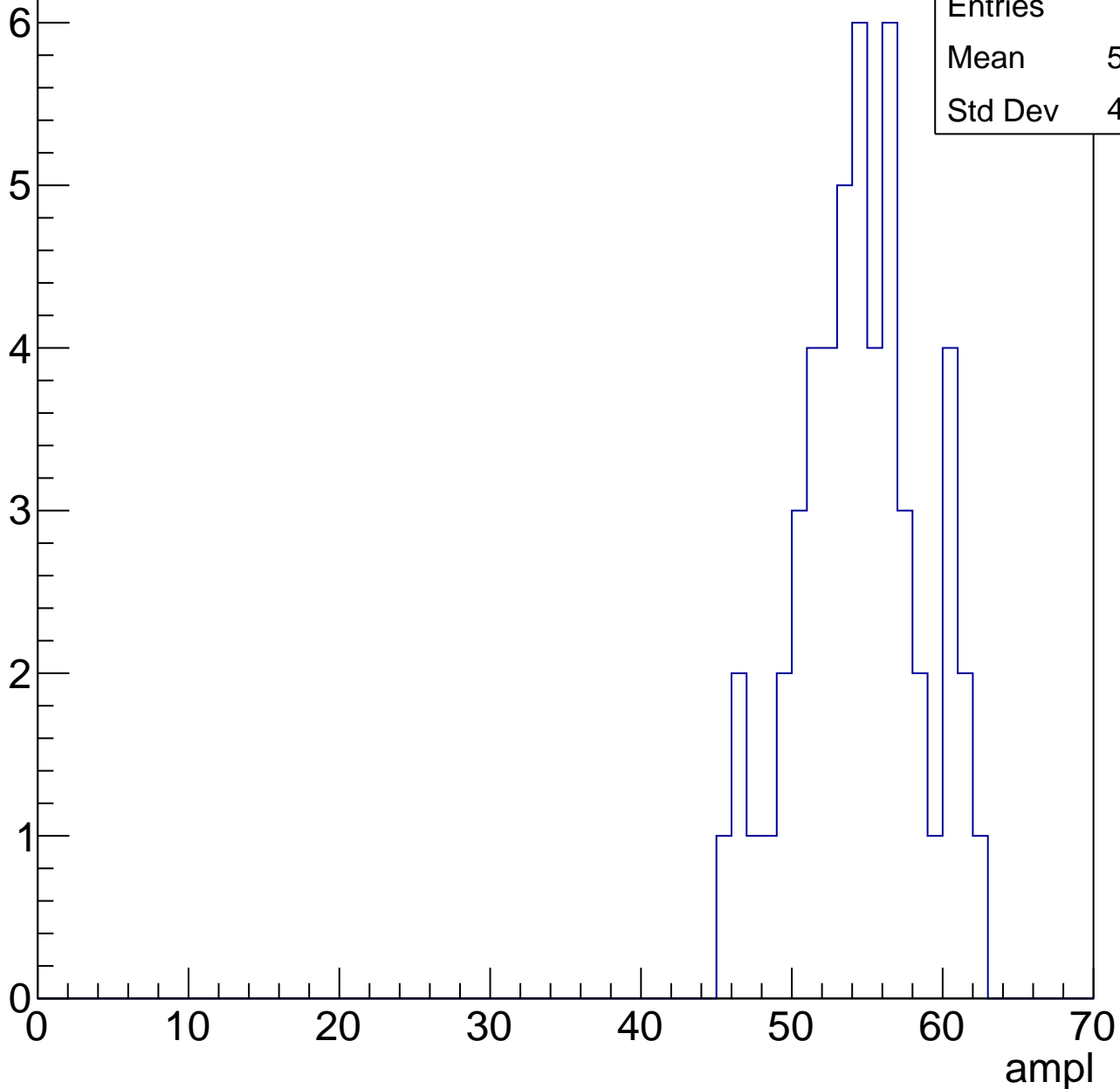


B1L103S, U12-ch0, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	52
Mean	53.98
Std Dev	4.083

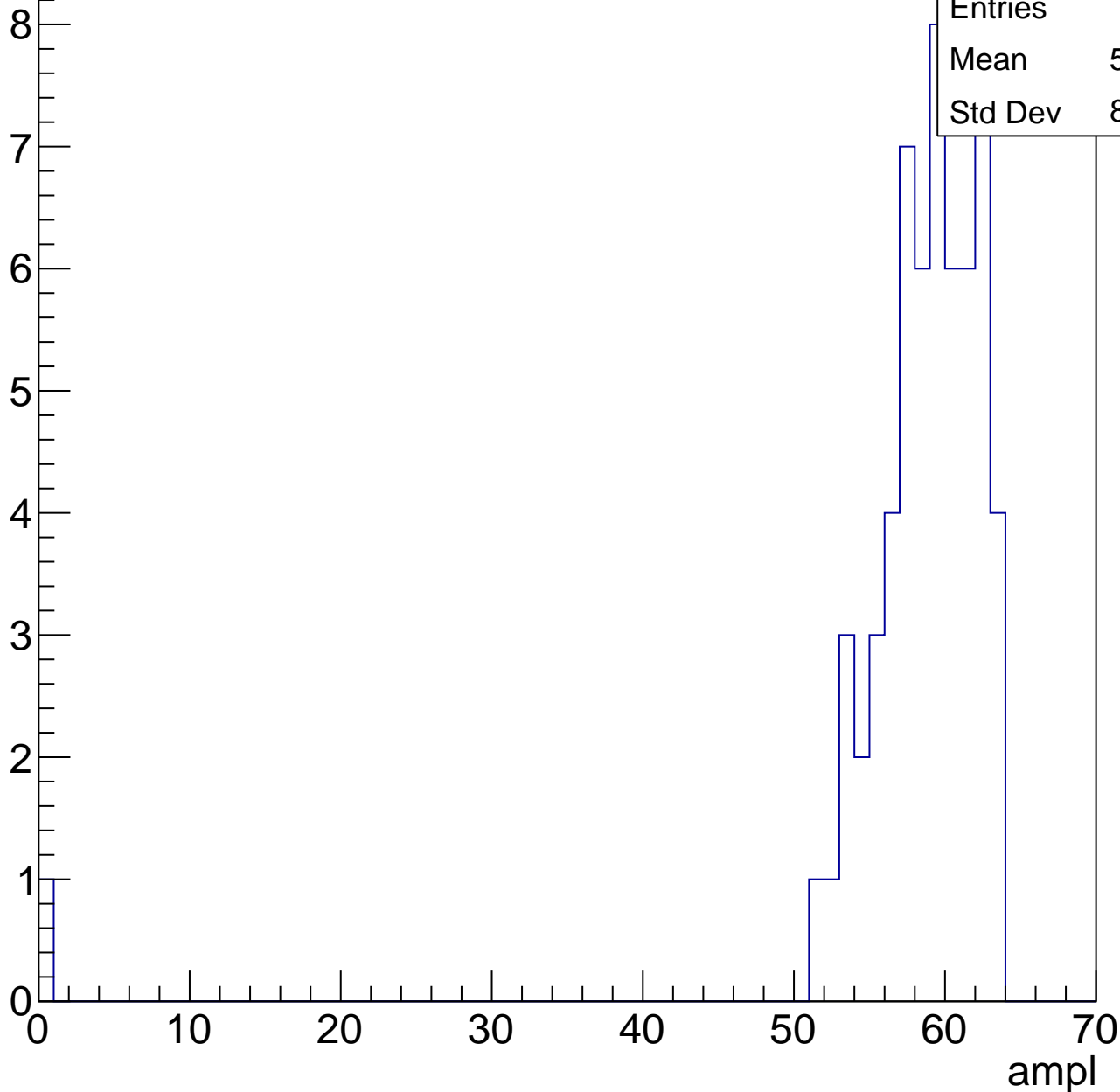


B1L103S, U12-ch0, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	57.53
Std Dev	8.069

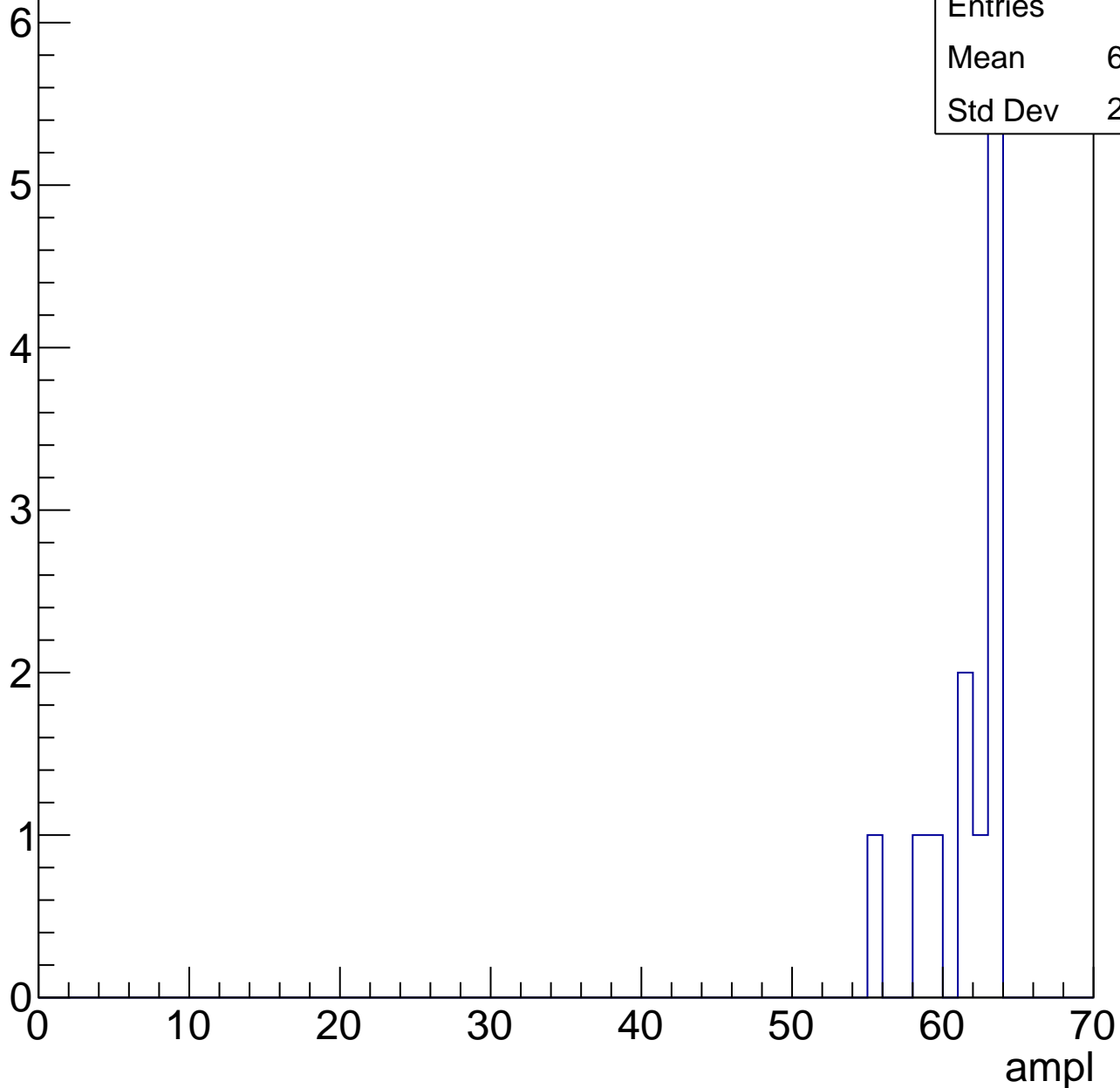


B1L103S, U12-ch0, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	12
Mean	61.17
Std Dev	2.478



B1L103S, U12-ch0, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

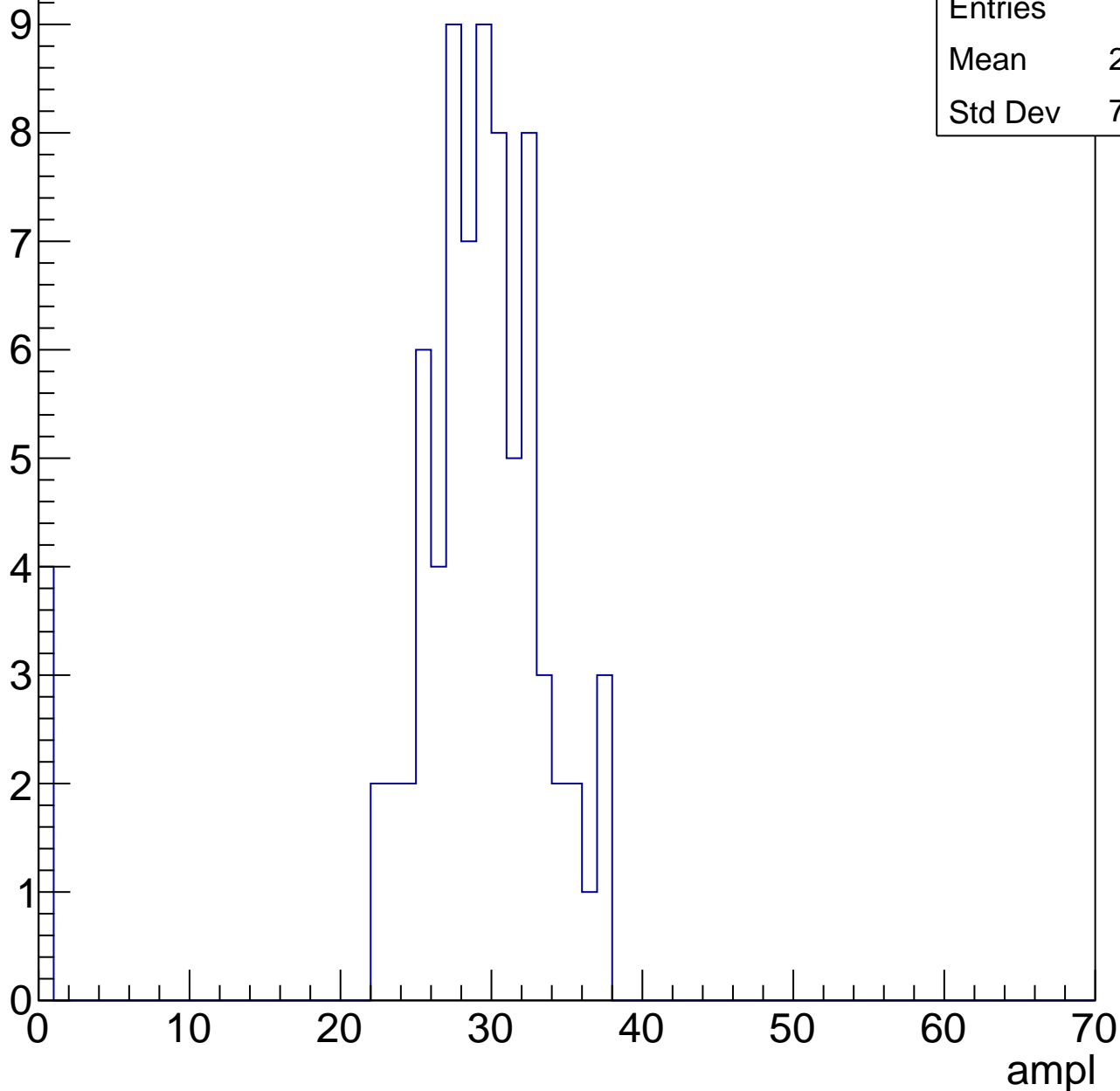


B1L103S, U12-ch1, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	77
Mean	27.62
Std Dev	7.318

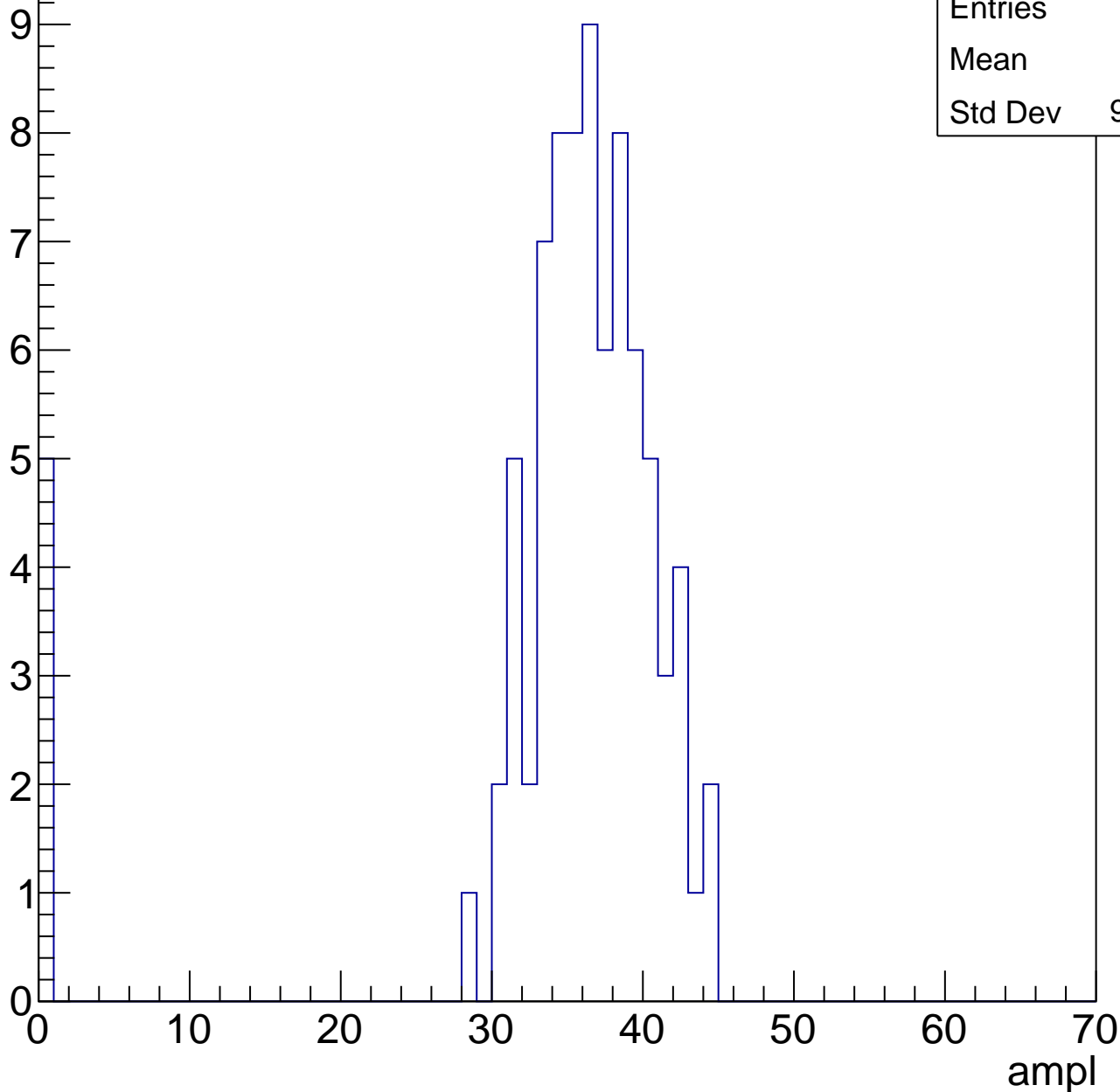


B1L103S, U12-ch1, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	82
Mean	34.1
Std Dev	9.336

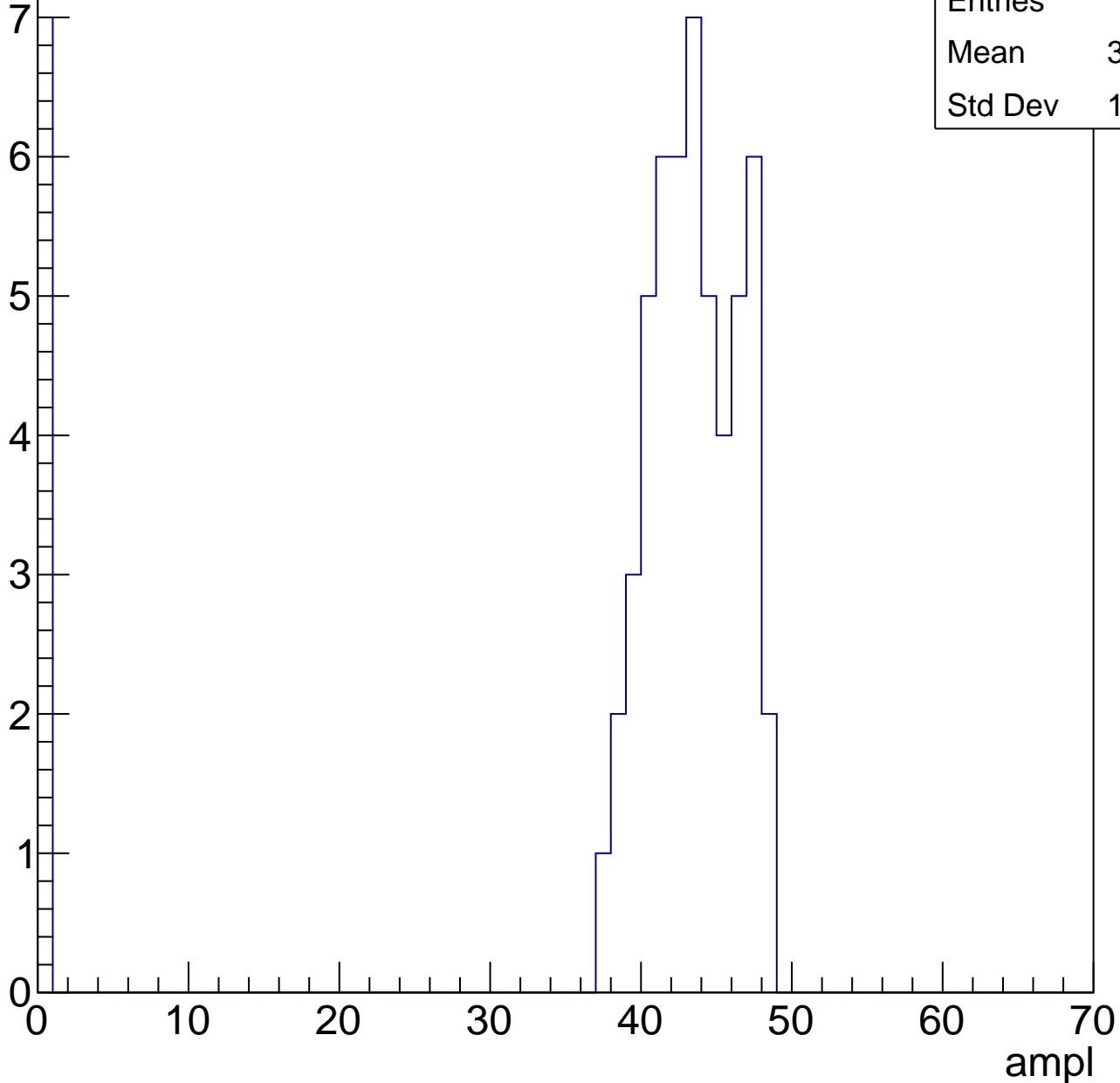


B1L103S, U12-ch1, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	37.92
Std Dev	14.17



B1L103S, U12-ch1, adc3

calib_packv5_041523_1651.root, FC#0, port C2

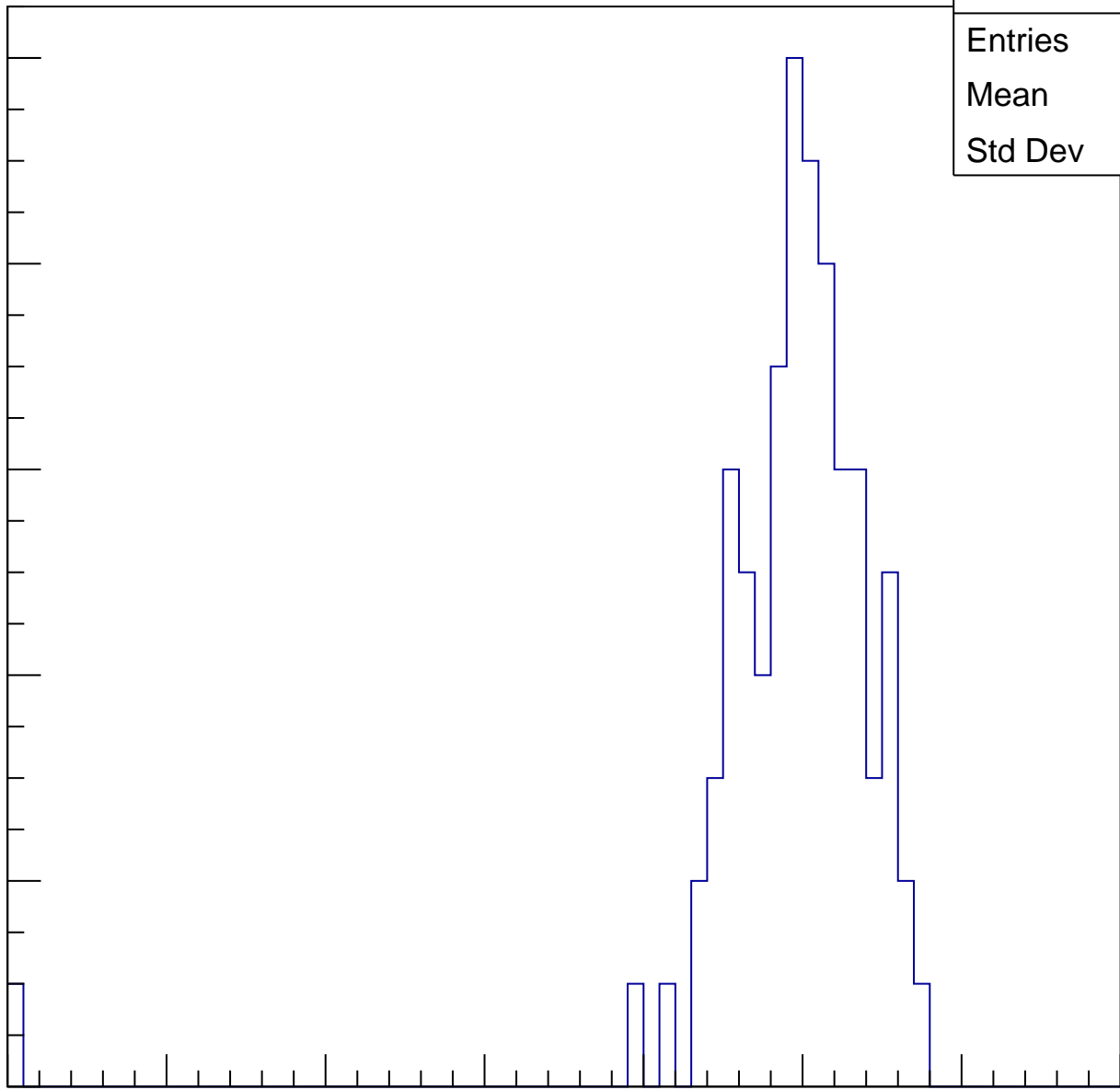
Entries	80
Mean	48.83
Std Dev	6.597

Entry

10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70

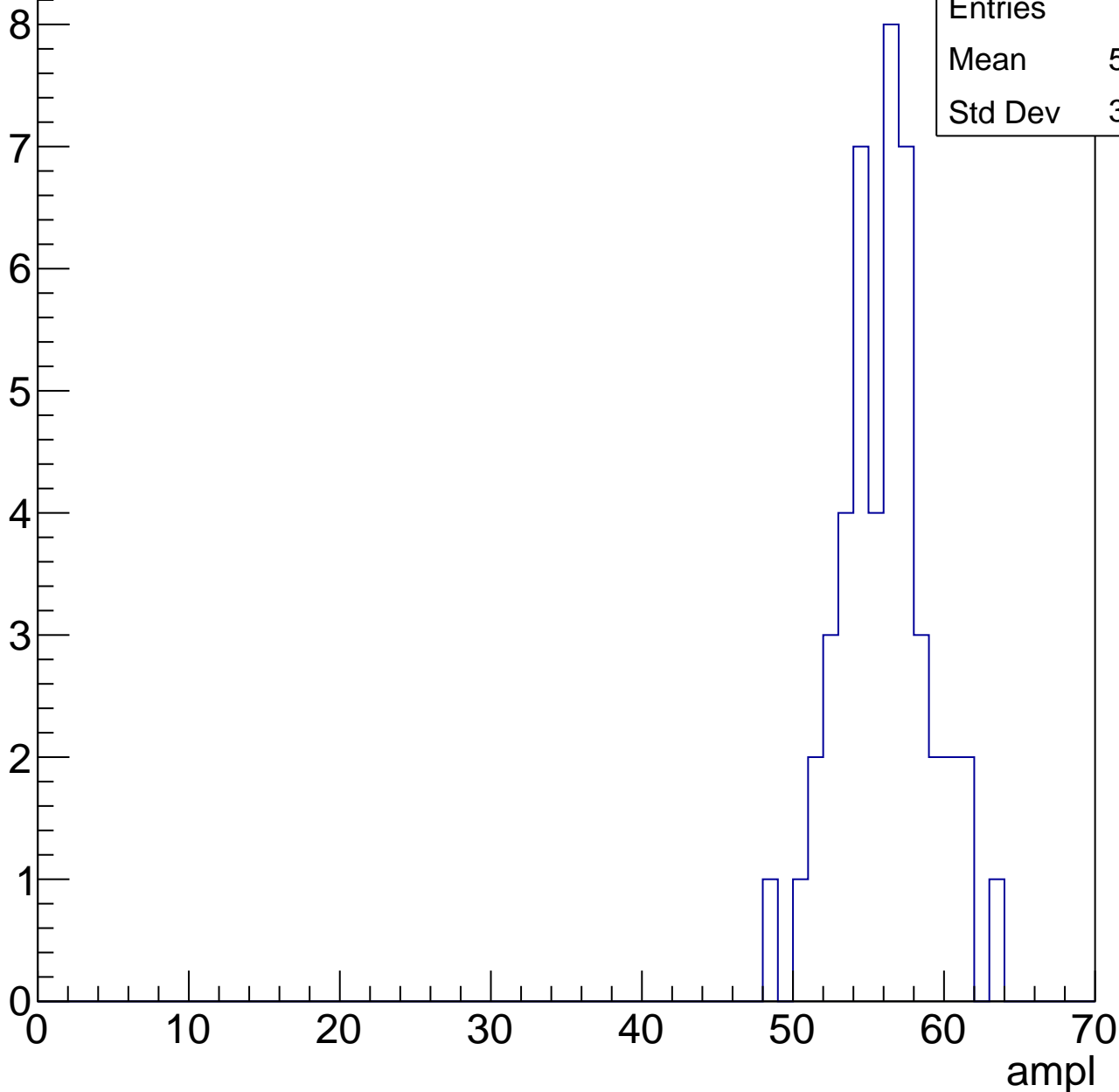


B1L103S, U12-ch1, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	47
Mean	55.53
Std Dev	3.002

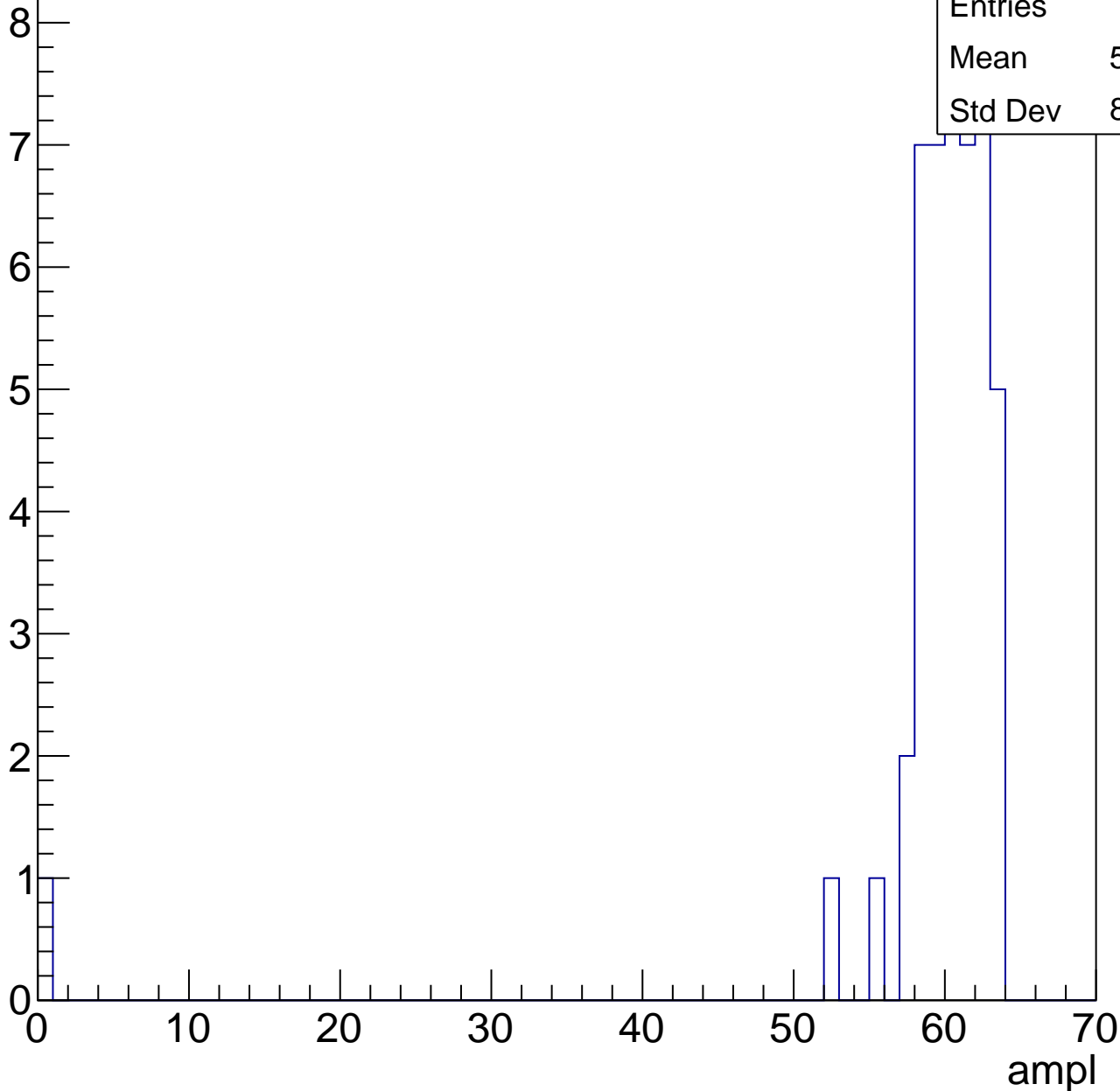


B1L103S, U12-ch1, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

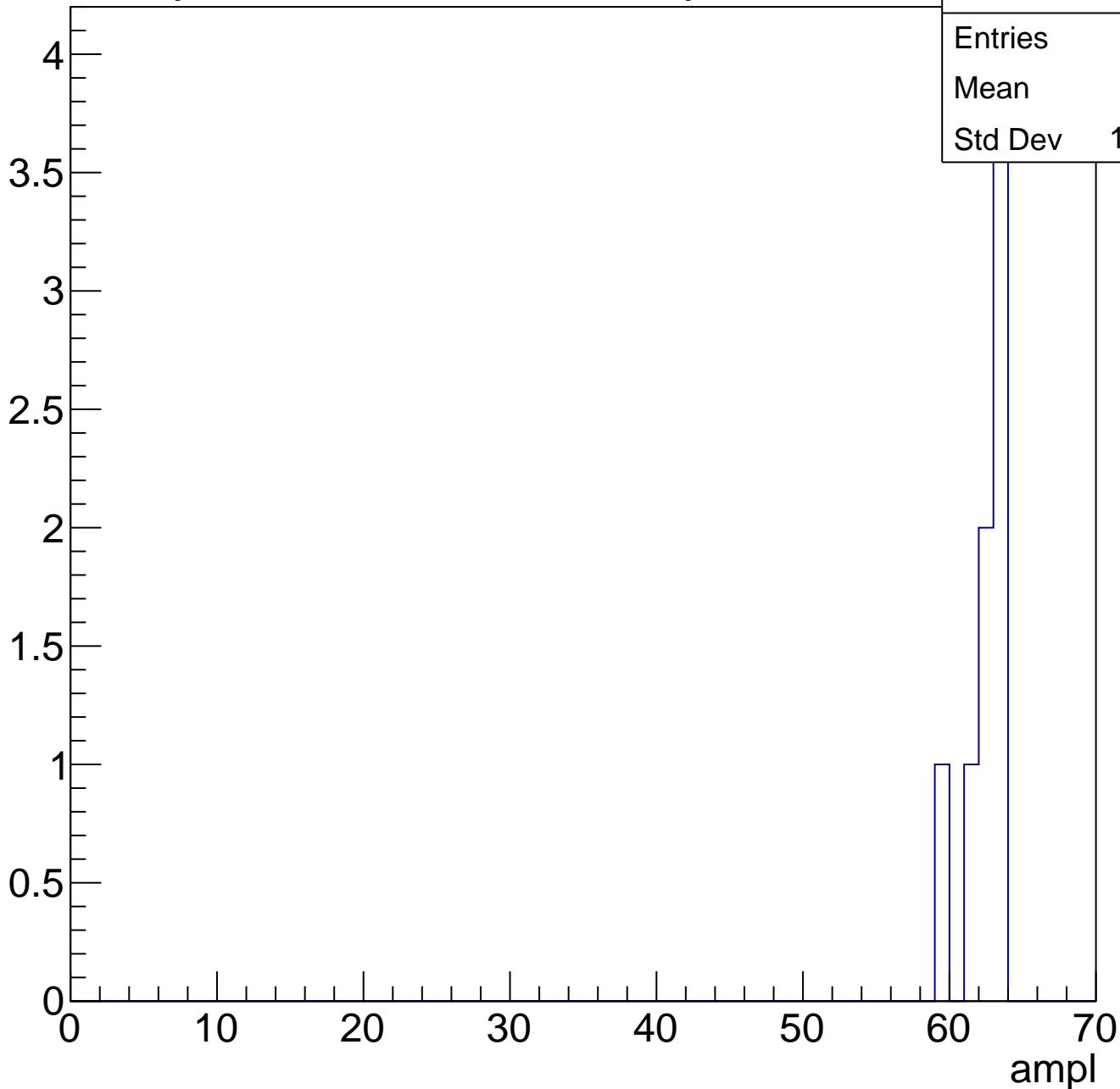
Entries	47
Mean	58.68
Std Dev	8.925



B1L103S, U12-ch1, adc6

calib_packv5_041523_1651.root, FC#0, port C2

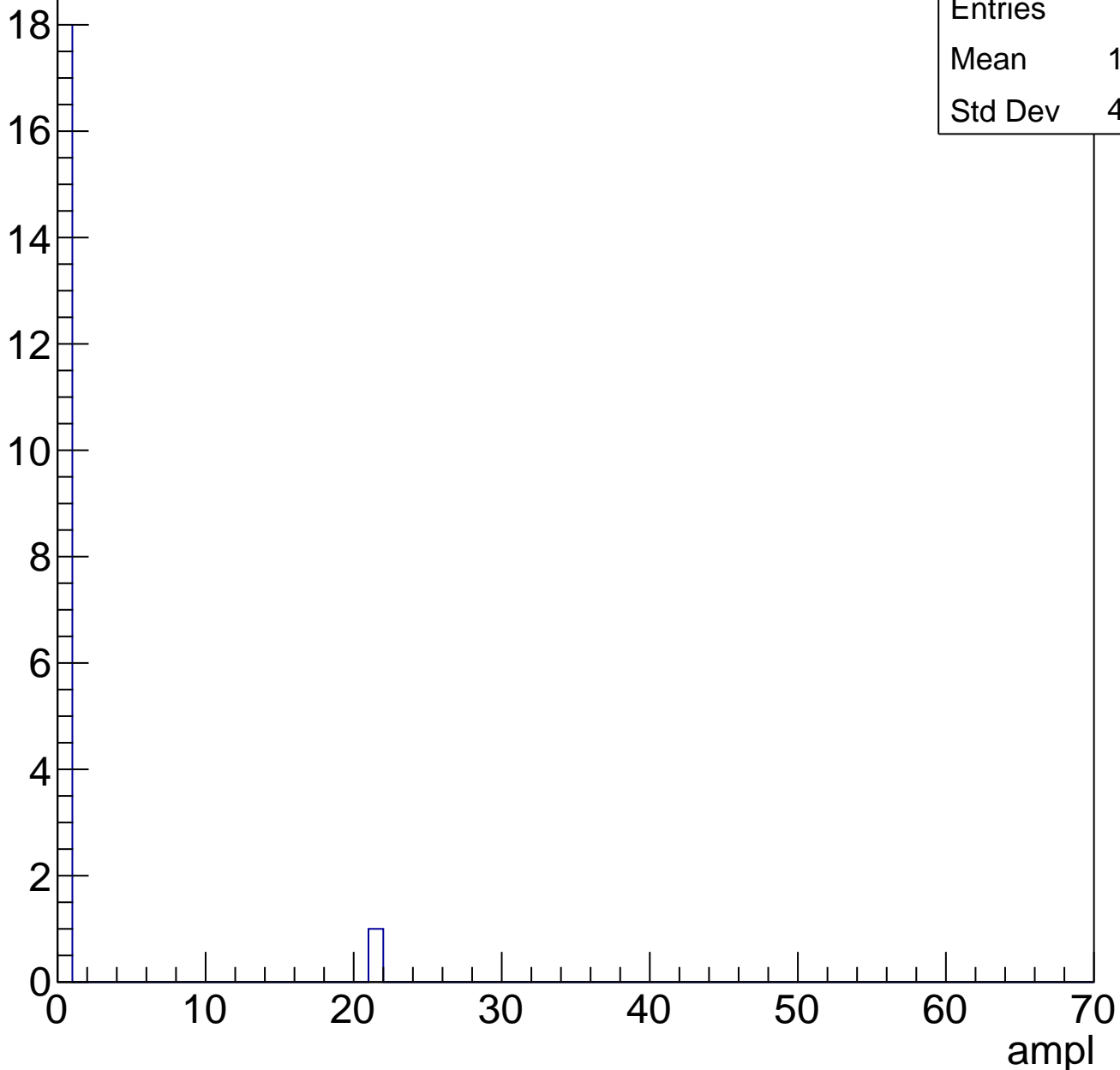
Entry



B1L103S, U12-ch1, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



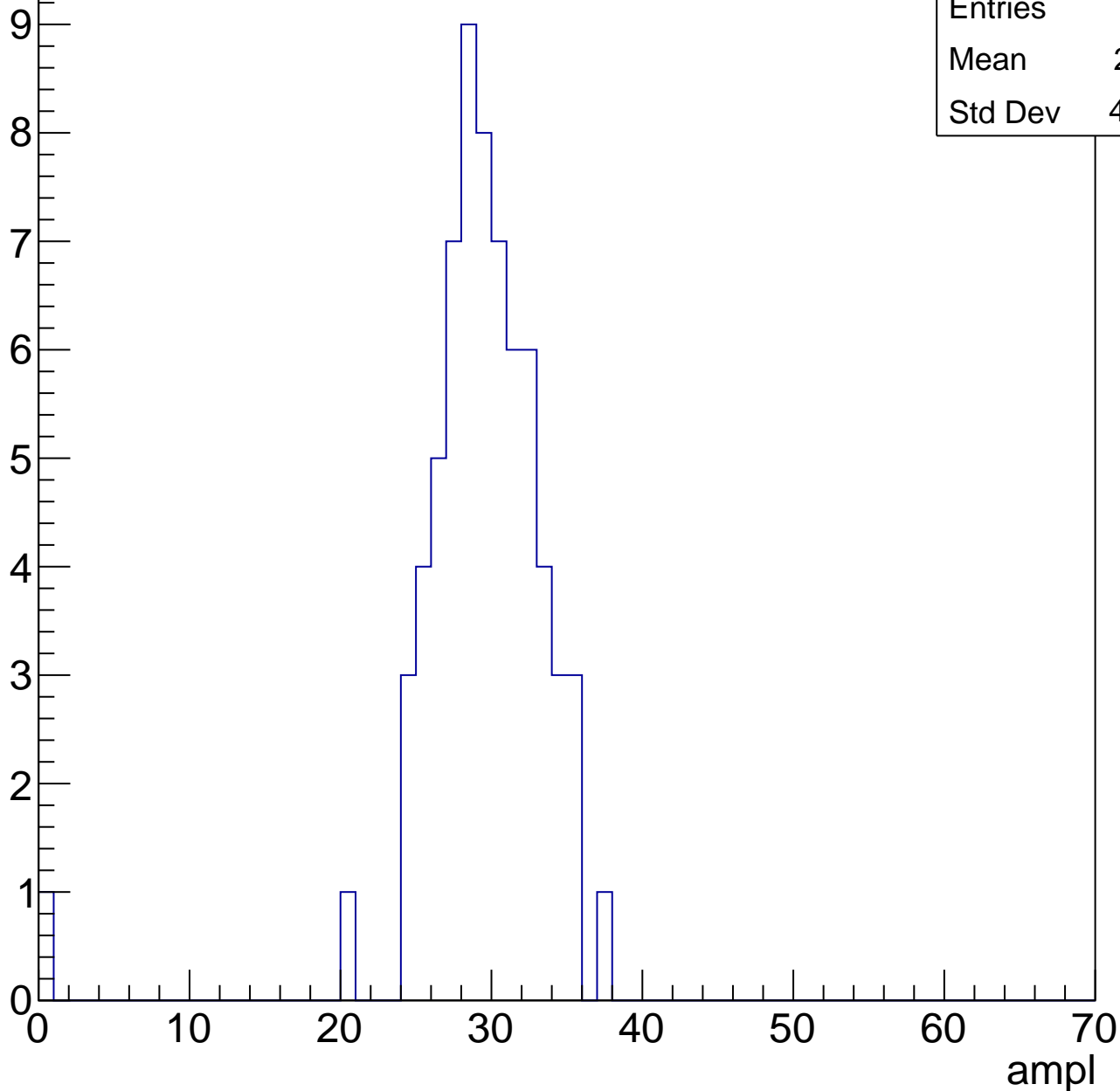
Entries	19
Mean	1.105
Std Dev	4.689

B1L103S, U12-ch2, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	28.81
Std Dev	4.754



B1L103S, U12-ch2, adc1

calib_packv5_041523_1651.root, FC#0, port C2

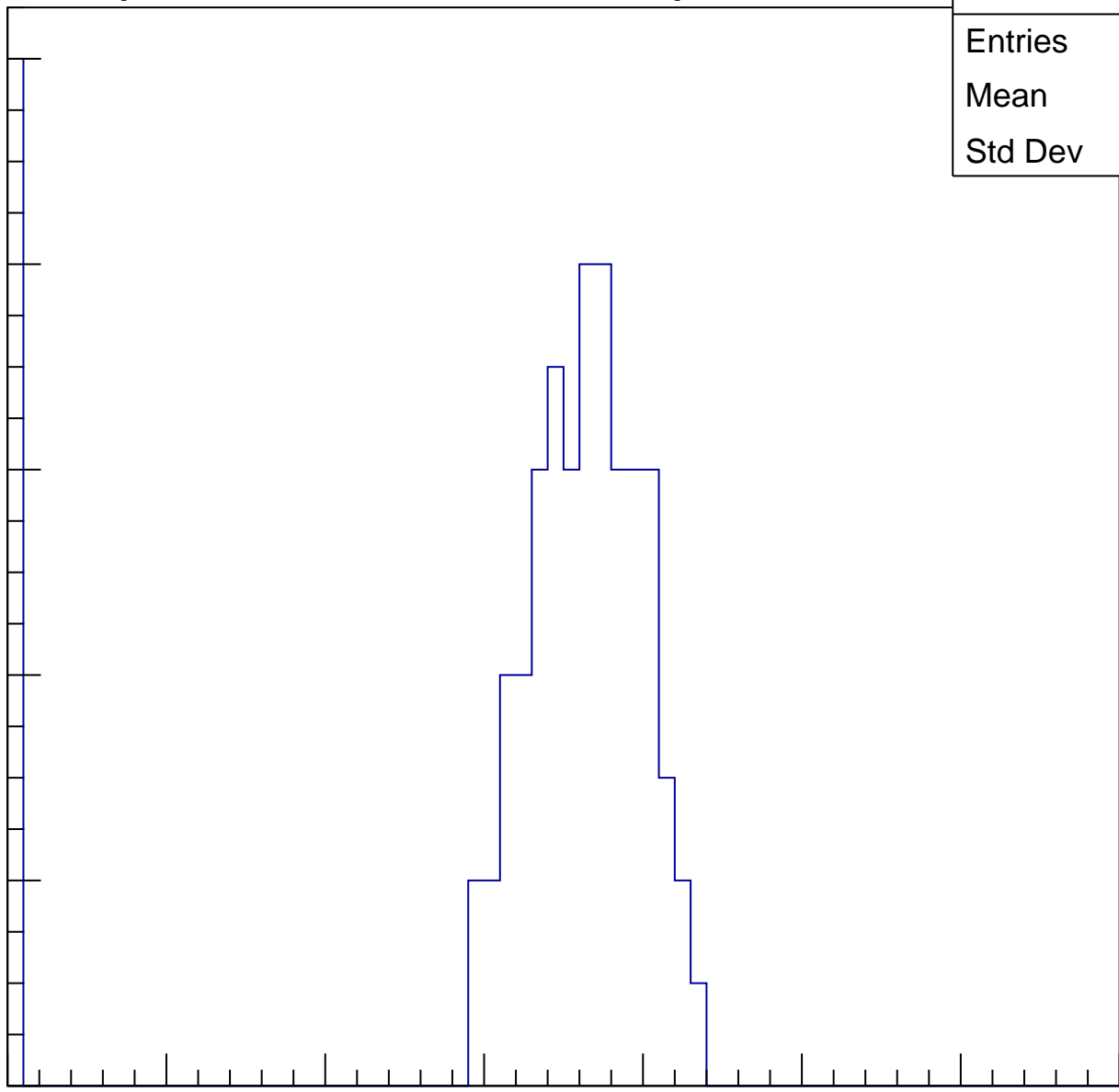
Entries	81
Mean	31.51
Std Dev	12.23

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

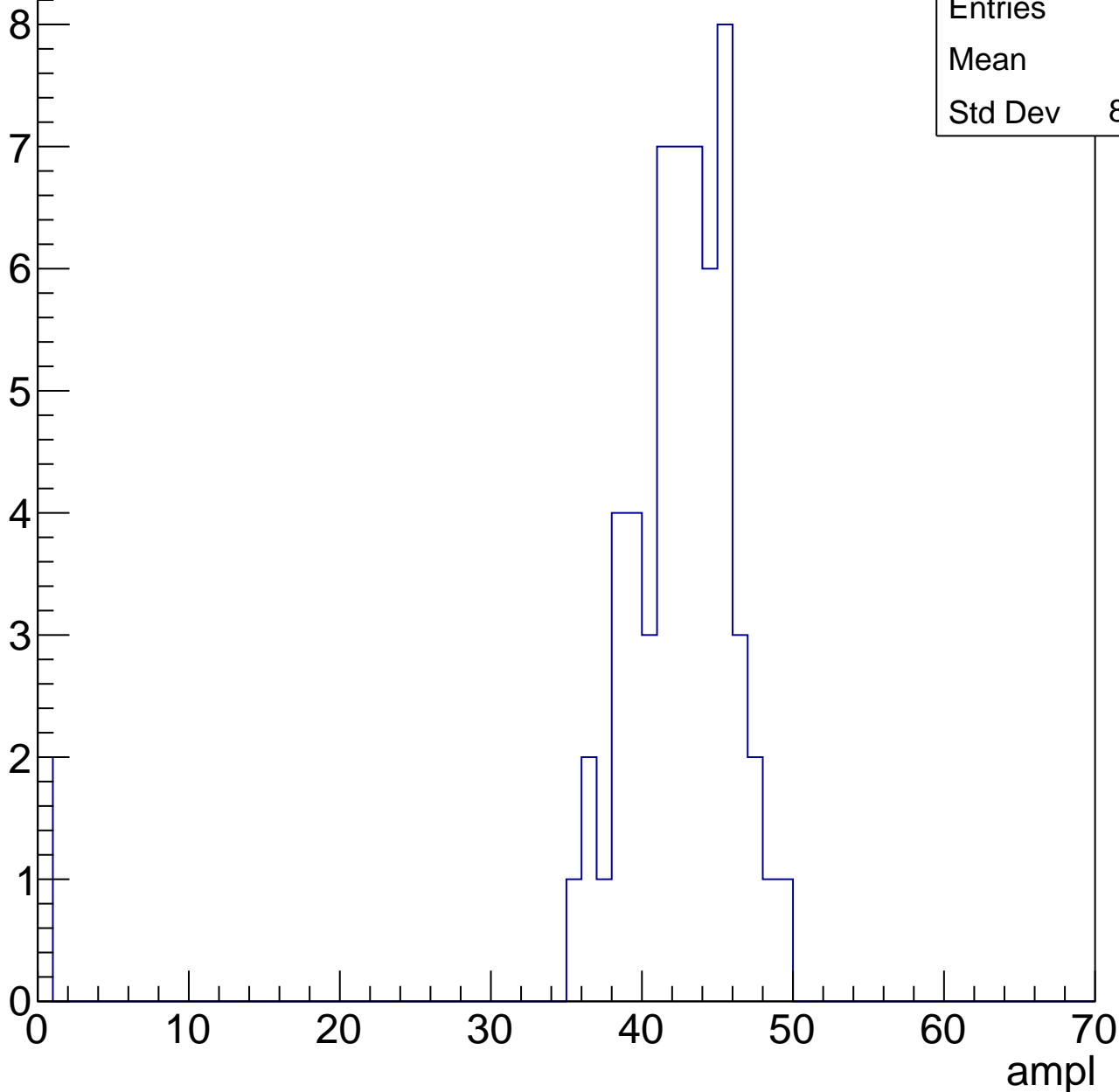


B1L103S, U12-ch2, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	40.8
Std Dev	8.227

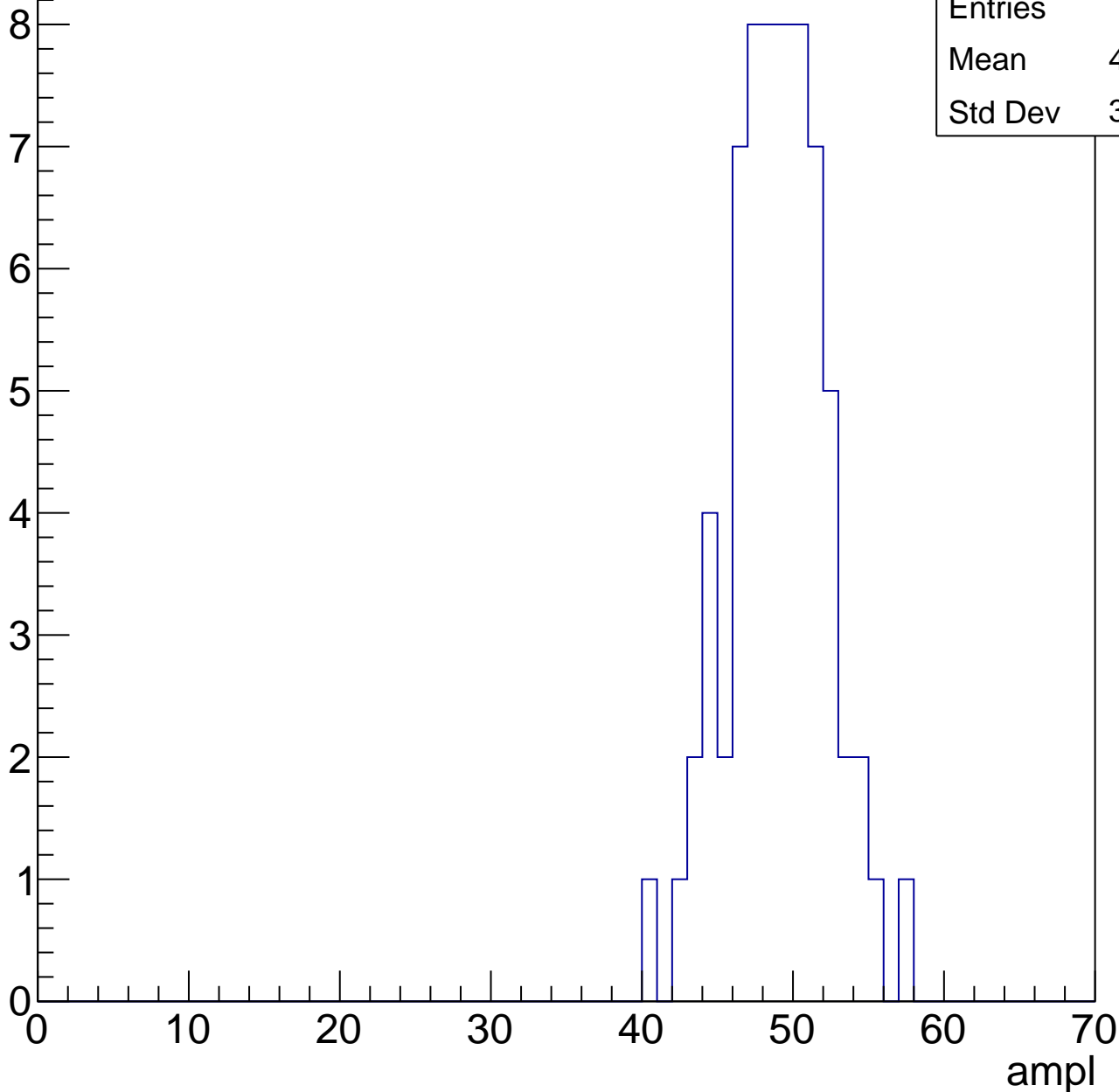


B1L103S, U12-ch2, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	48.52
Std Dev	3.197

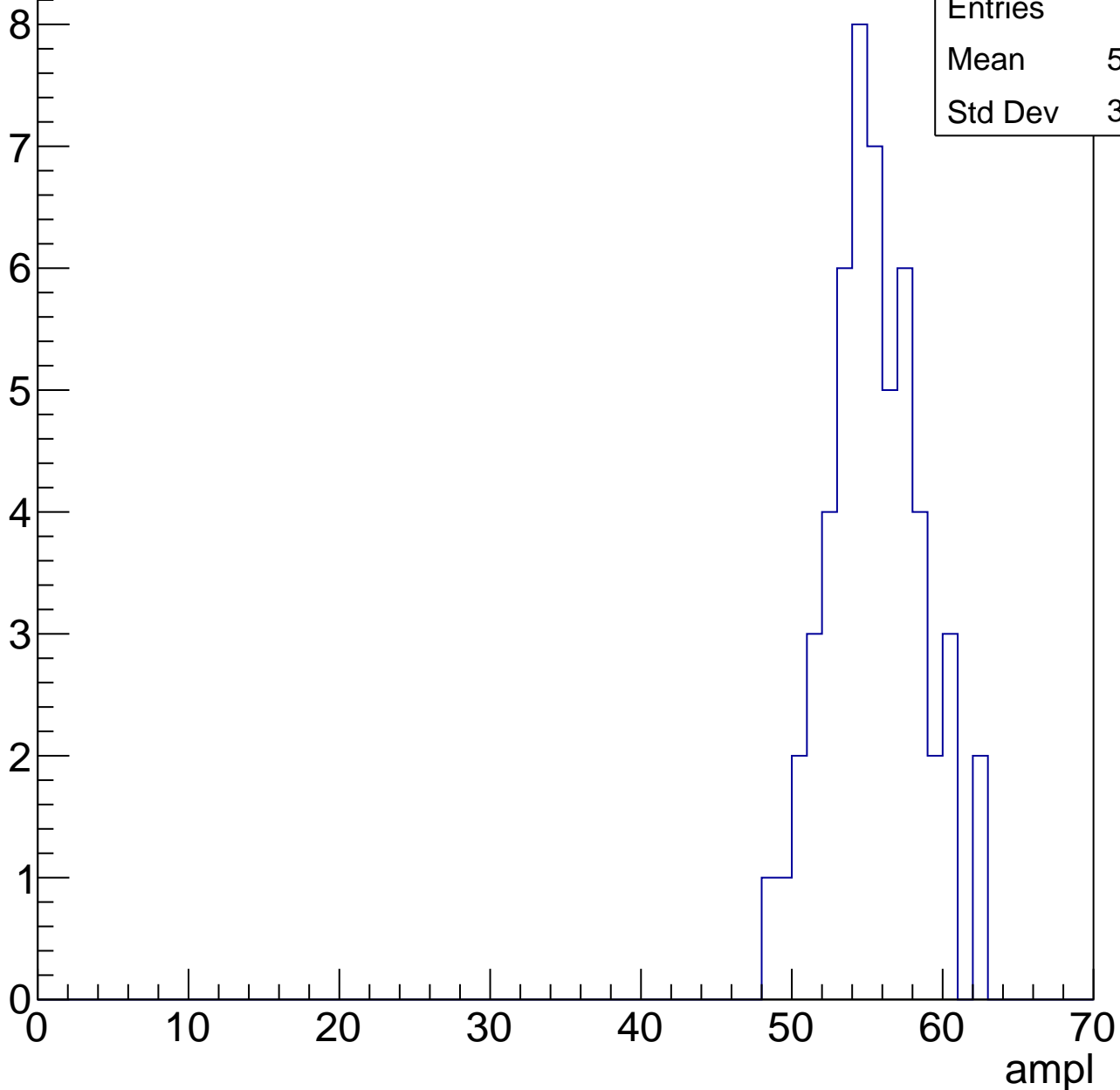


B1L103S, U12-ch2, adc4

calib_packv5_041523_1651.root, FC#0, port C2

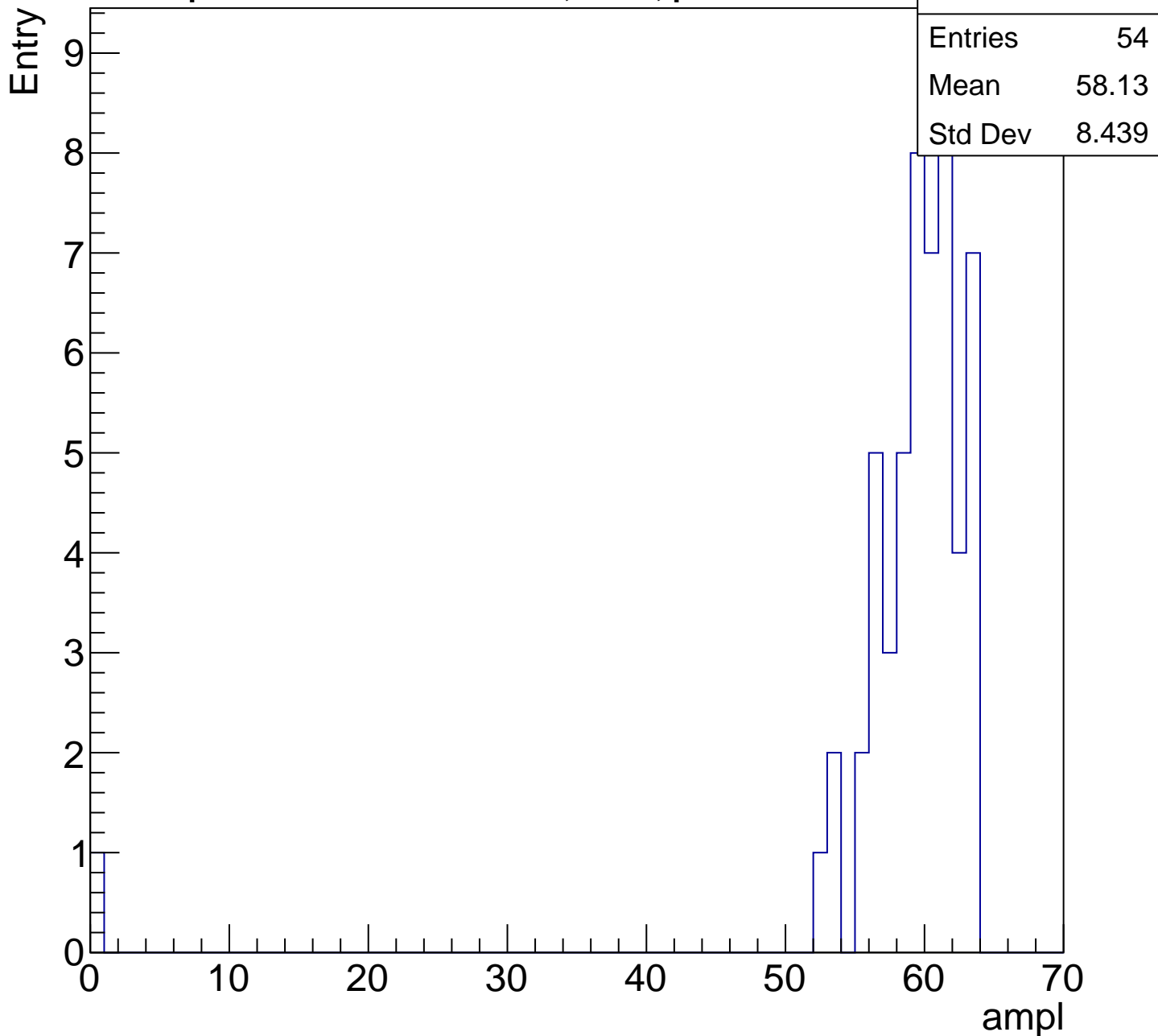
Entry

Entries	54
Mean	54.98
Std Dev	3.106



B1L103S, U12-ch2, adc5

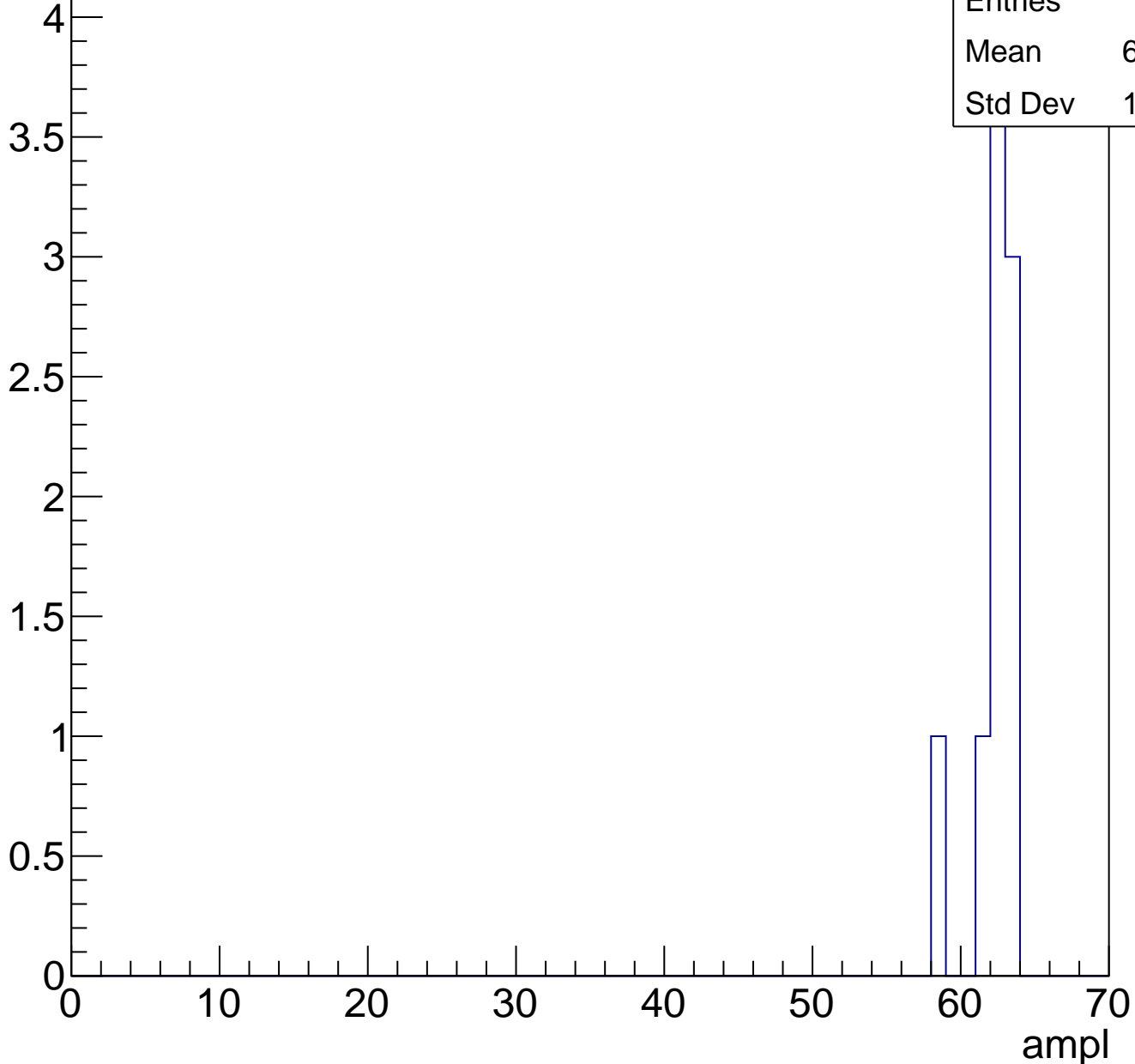
calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U12-ch2, adc6

calib_packv5_041523_1651.root, FC#0, port C2

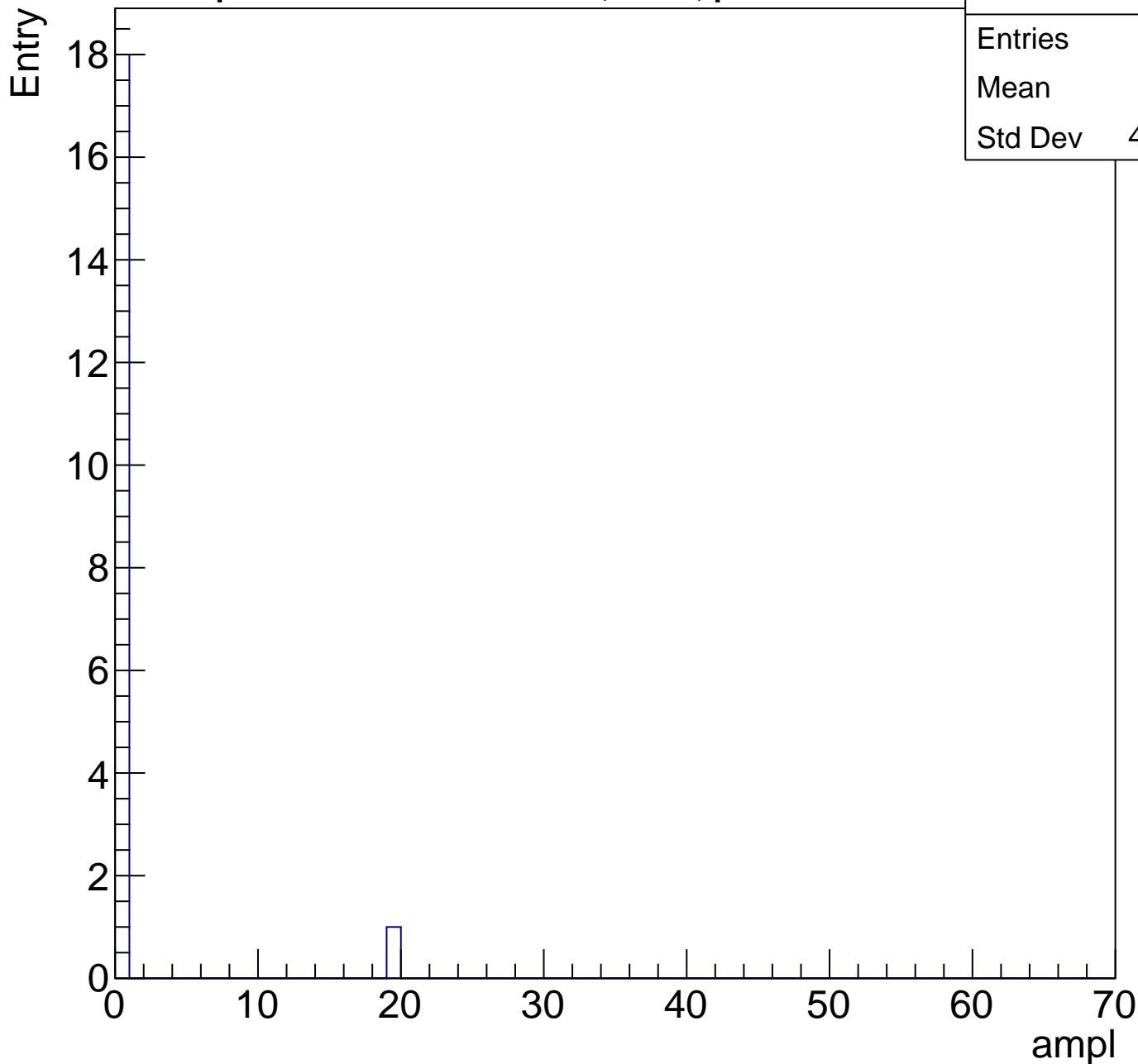
Entry



B1L103S, U12-ch2, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1
Std Dev	4.243

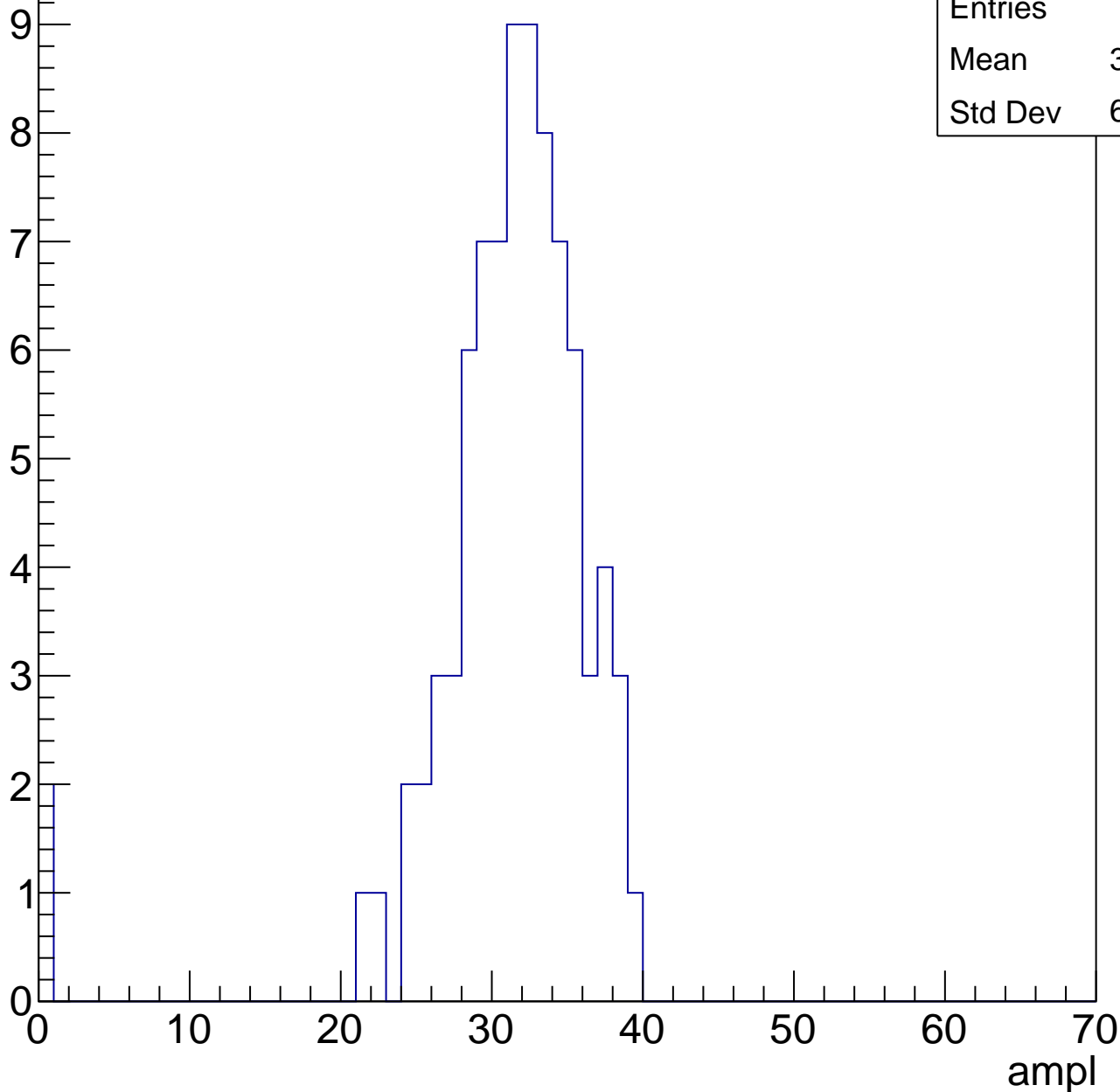


B1L103S, U12-ch3, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	84
Mean	30.58
Std Dev	6.075

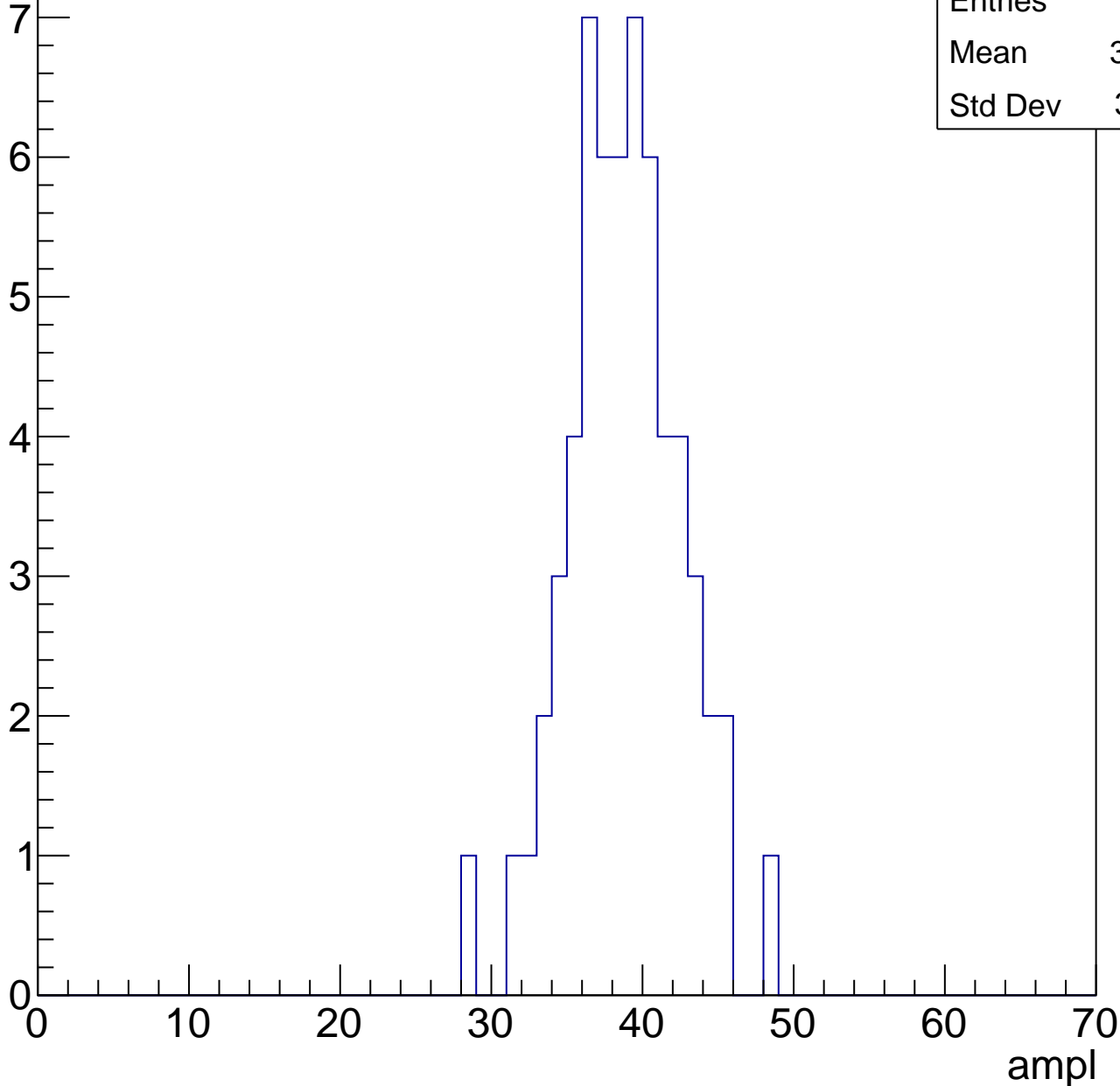


B1L103S, U12-ch3, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	38.35
Std Dev	3.701

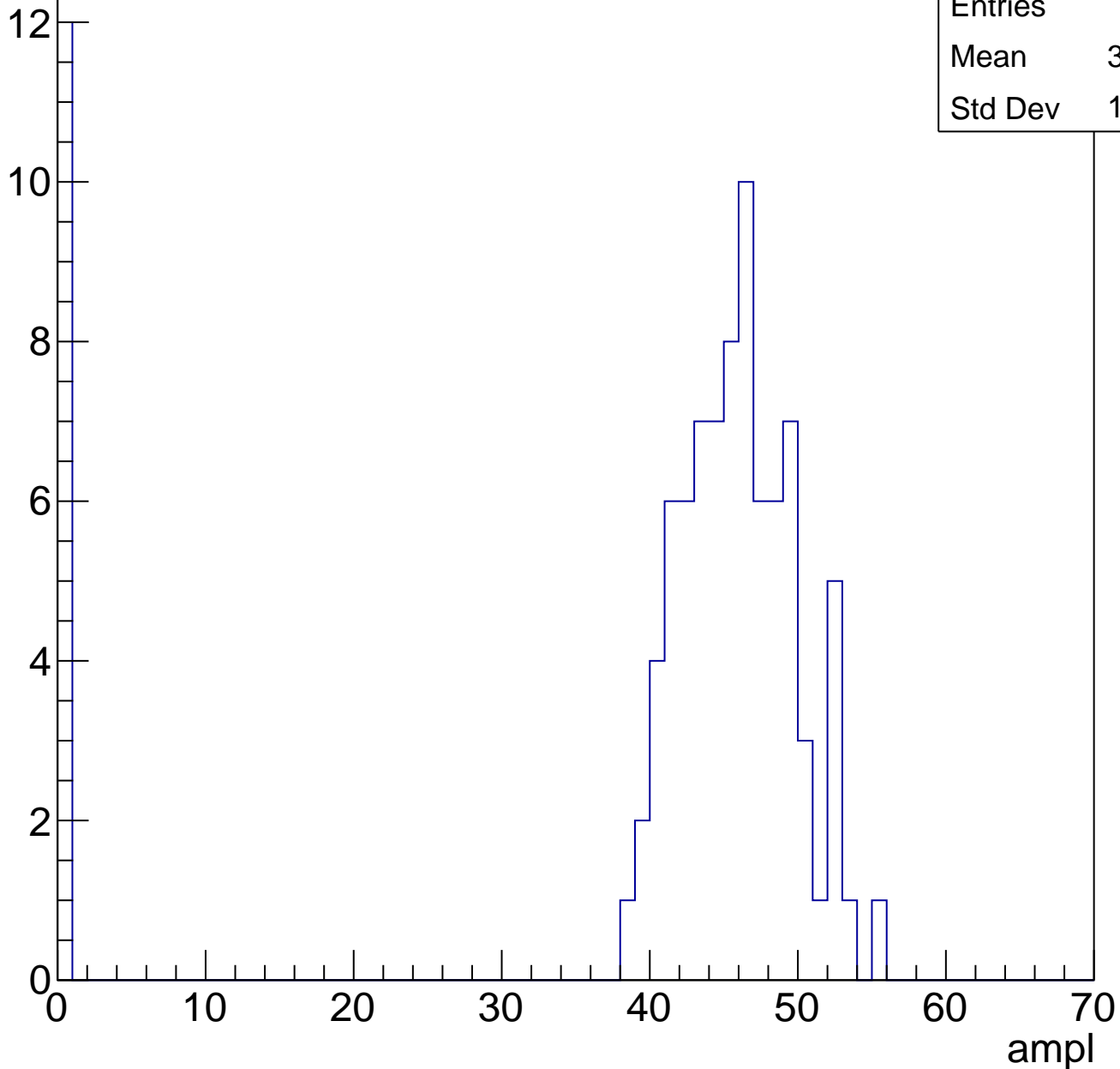


B1L103S, U12-ch3, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	93
Mean	39.62
Std Dev	15.64

Entry

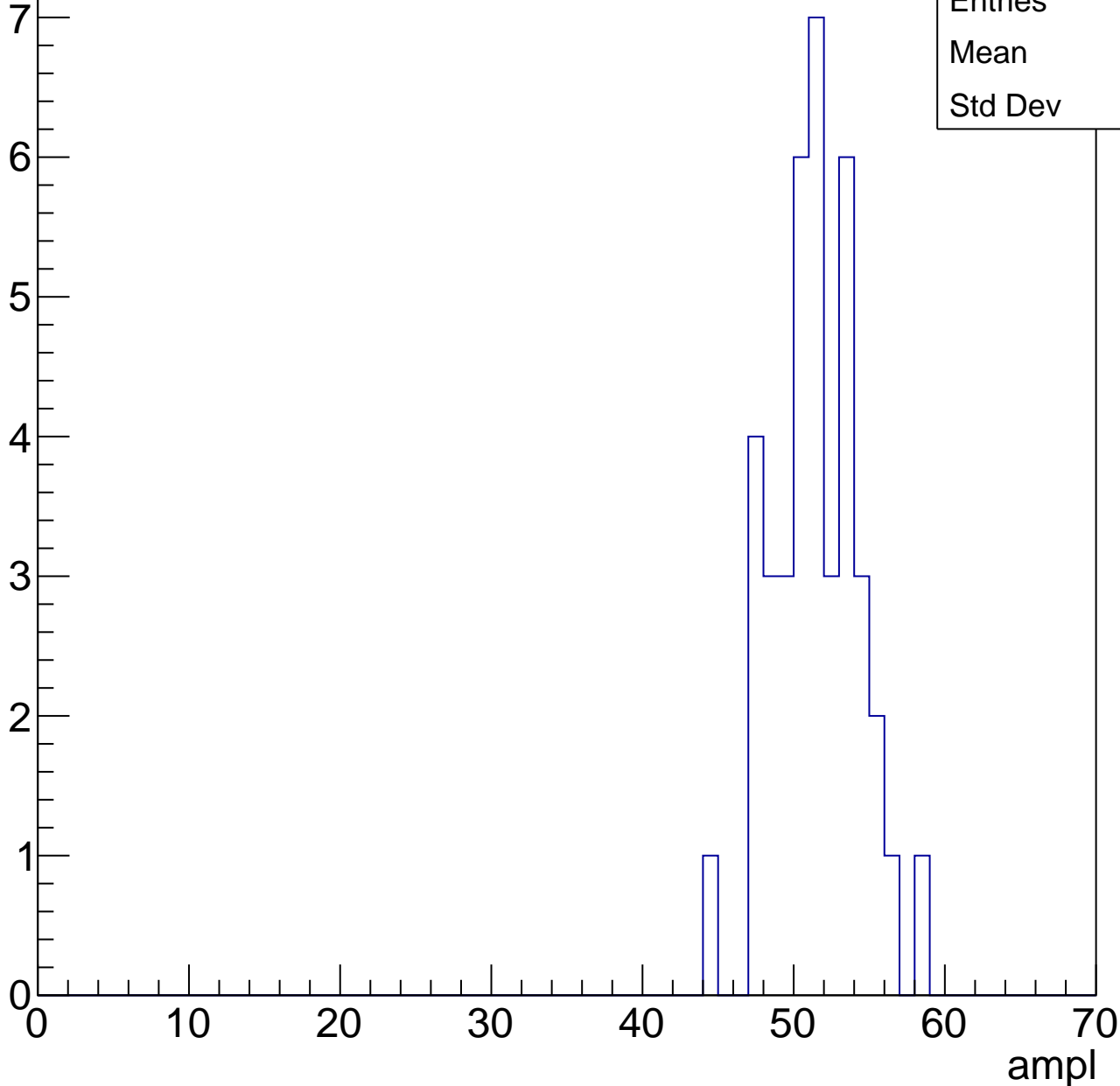


B1L103S, U12-ch3, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	40
Mean	51
Std Dev	2.82



B1L103S, U12-ch3, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entries	69
Mean	57.04
Std Dev	3.014

Entry

10

8

6

4

2

0

0

10

20

30

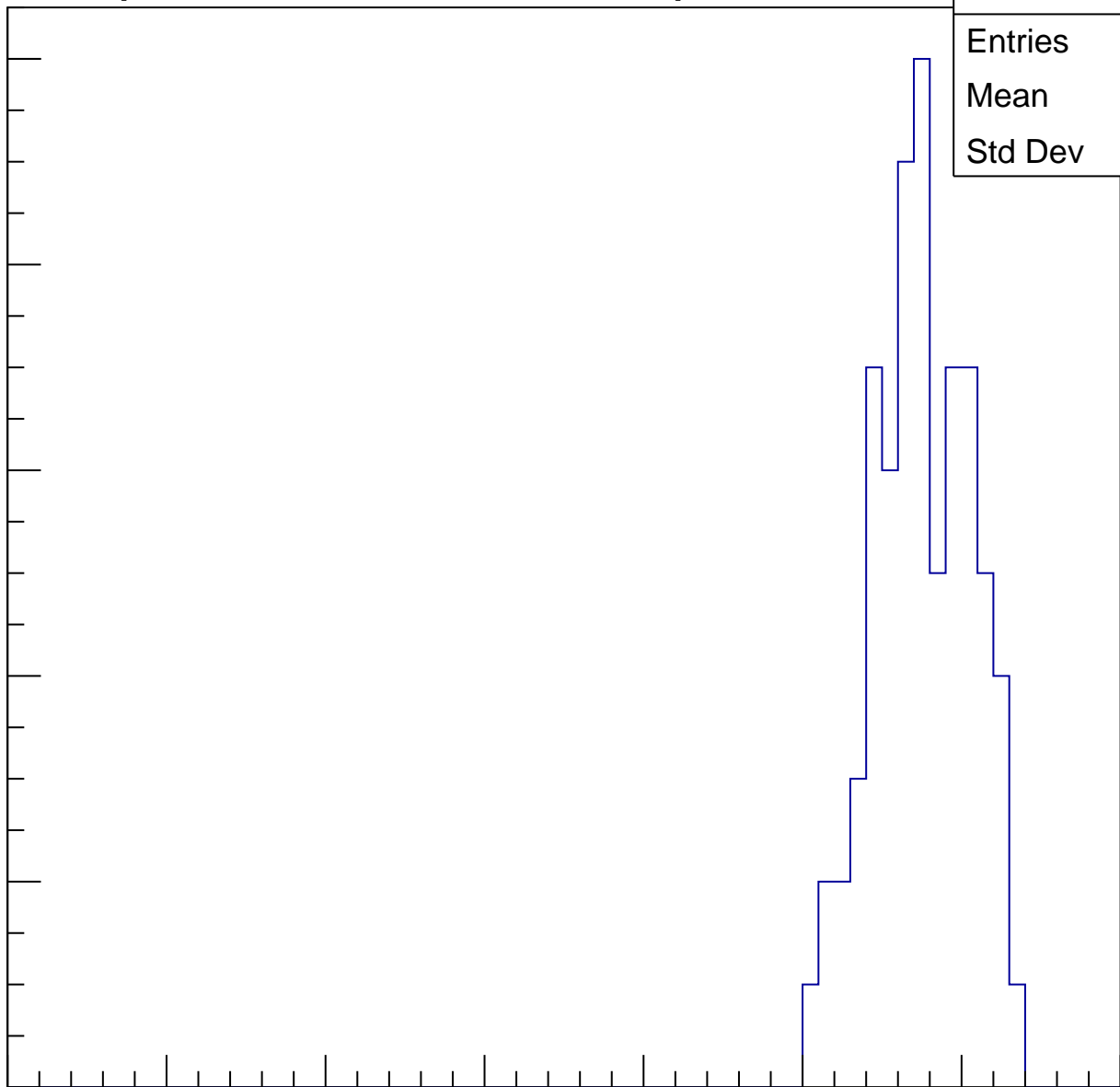
40

50

60

70

ampl

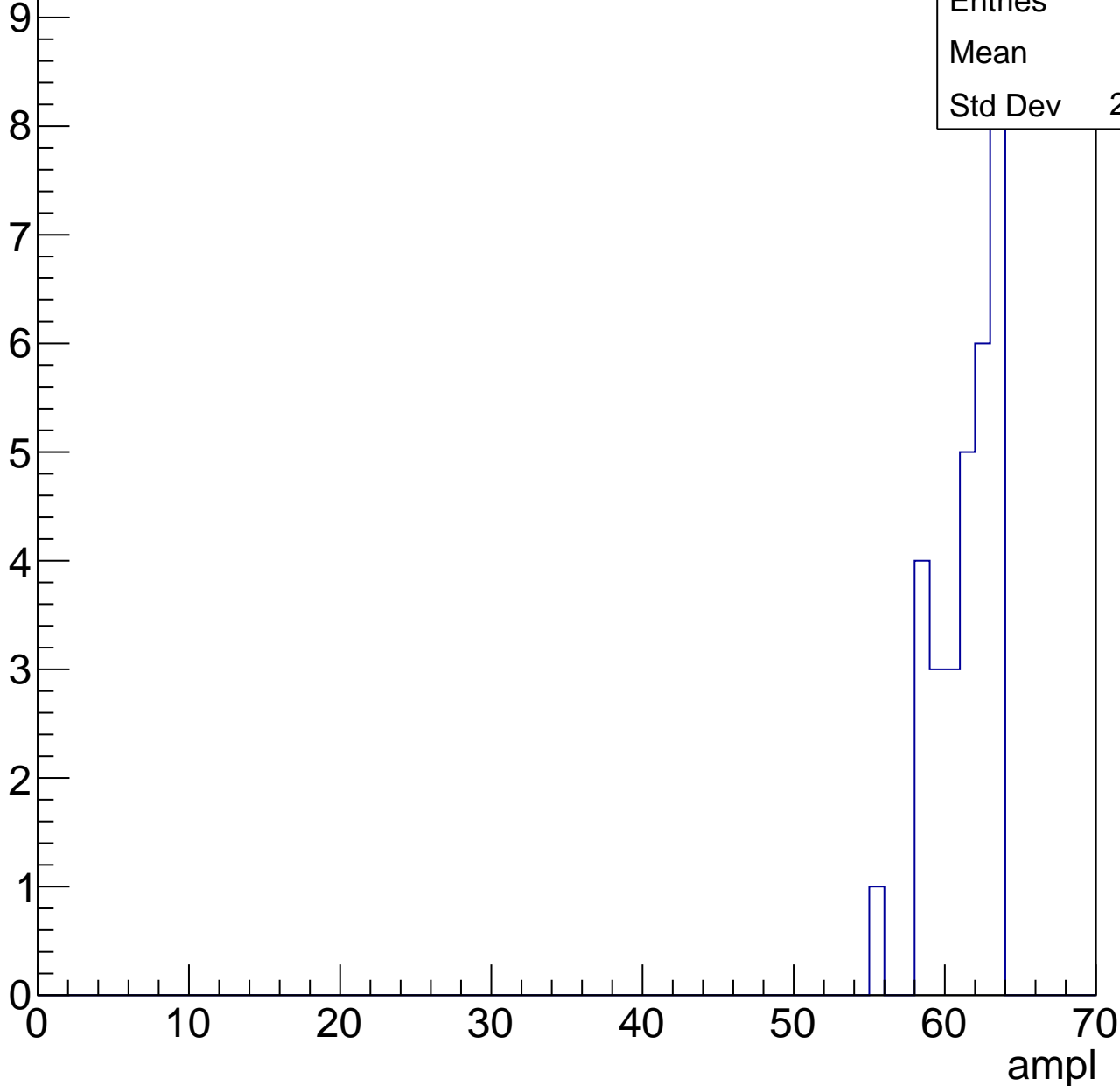


B1L103S, U12-ch3, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

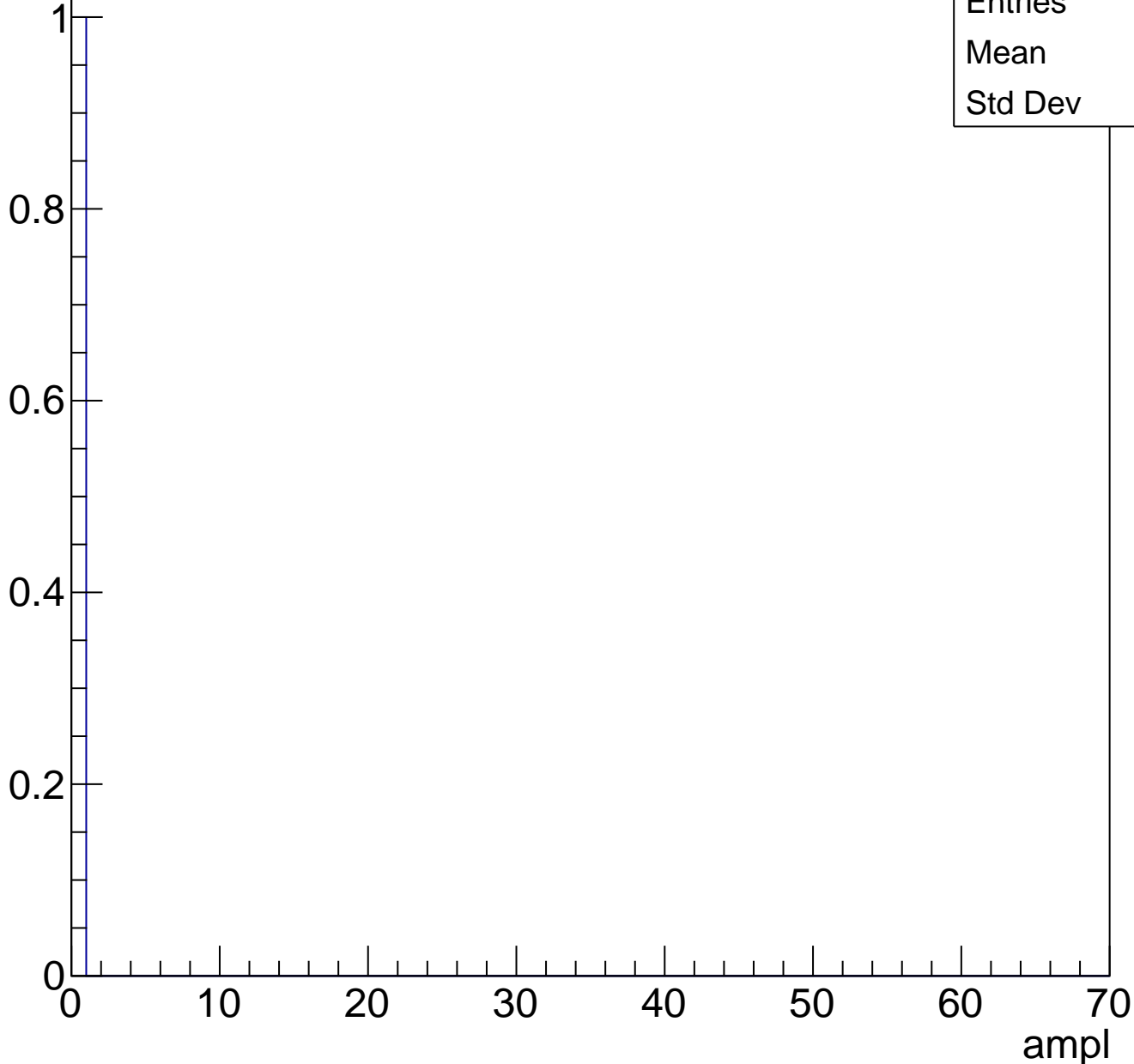
Entries	31
Mean	60.9
Std Dev	2.038



B1L103S, U12-ch3, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch3, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	18
Mean	0
Std Dev	0

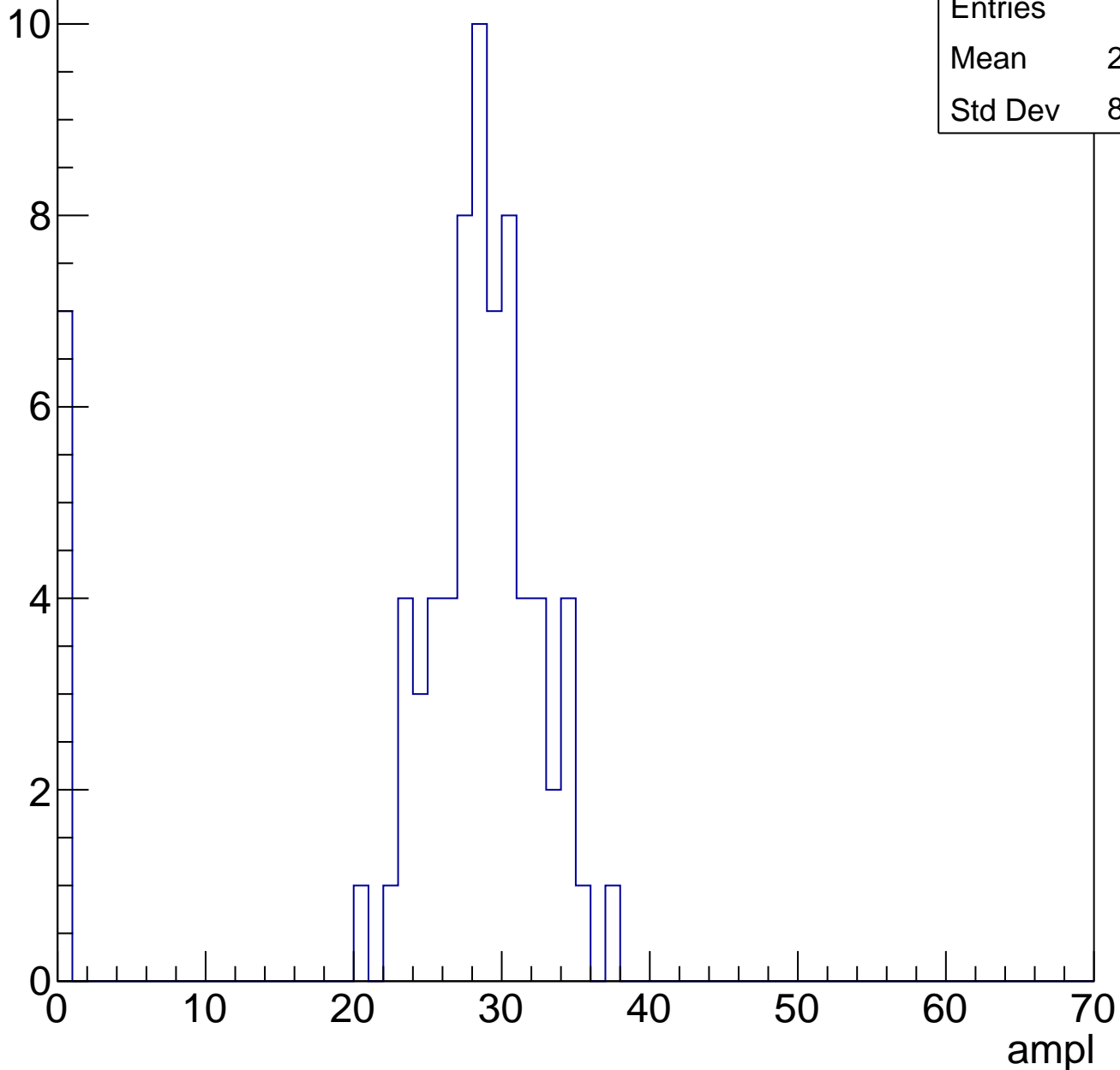
ampl

B1L103S, U12-ch4, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	73
Mean	25.68
Std Dev	8.965

Entry



B1L103S, U12-ch4, adc1

calib_packv5_041523_1651.root, FC#0, port C2

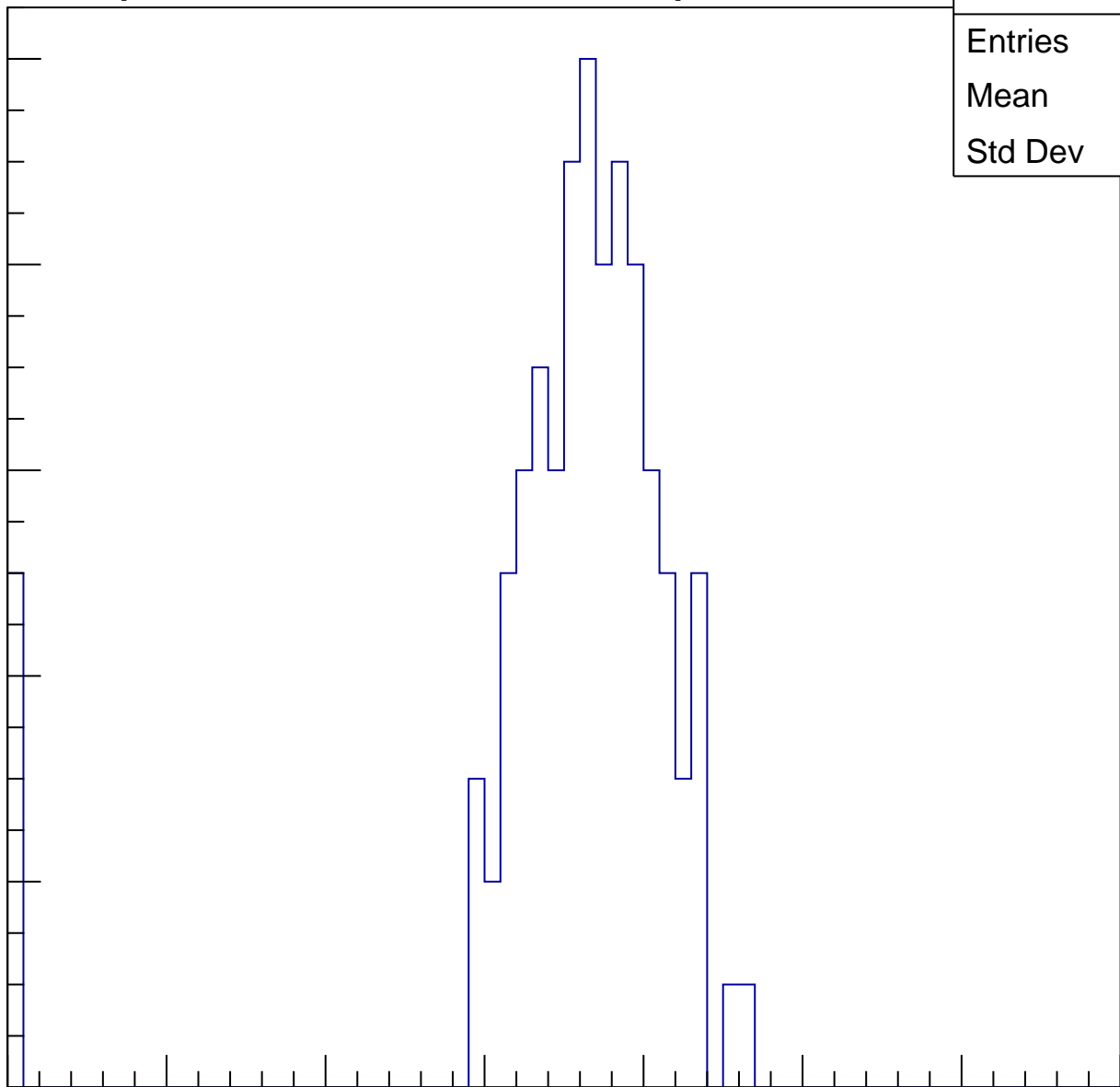
Entries	99
Mean	34.66
Std Dev	8.824

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

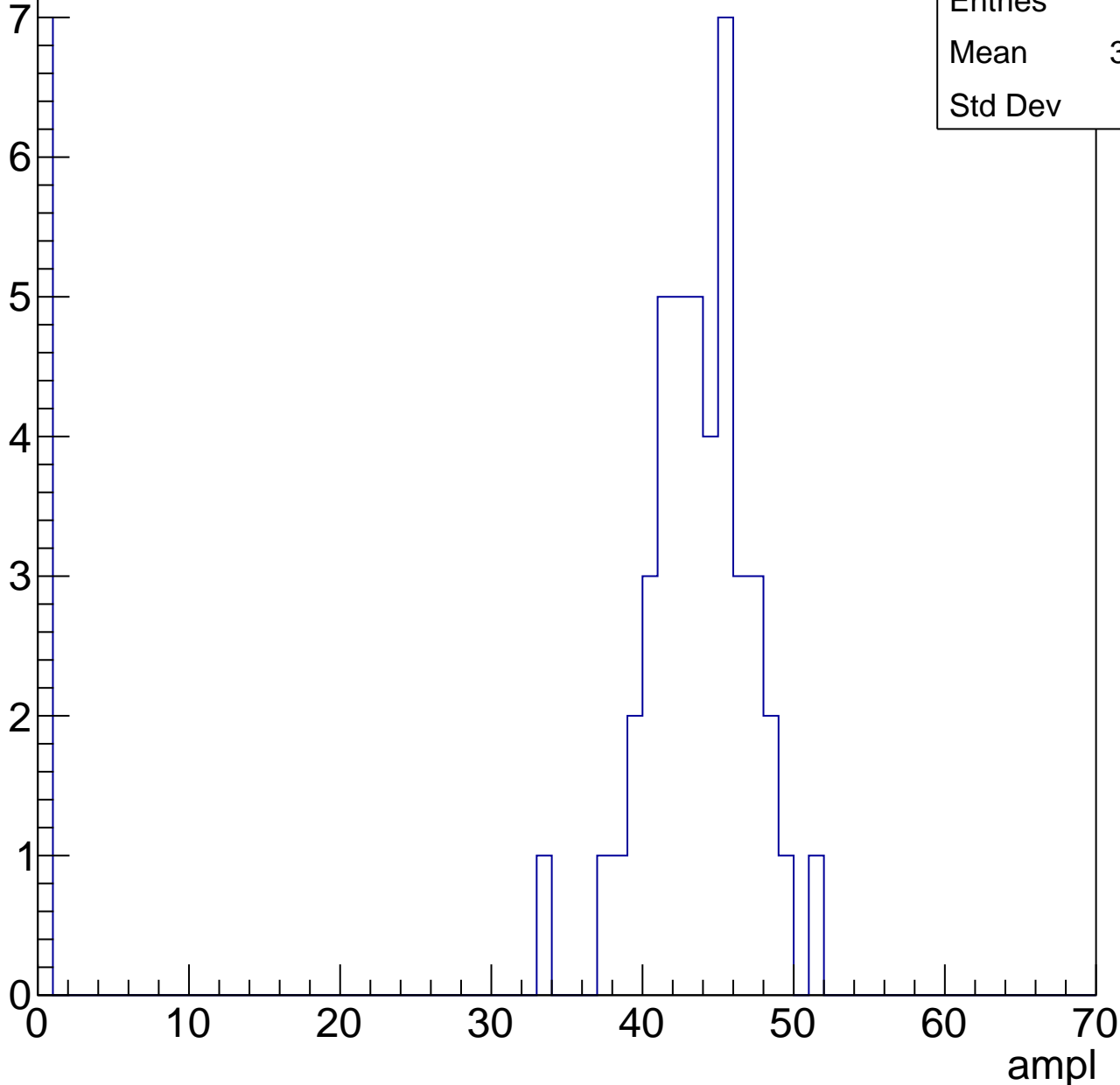


B1L103S, U12-ch4, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	51
Mean	37.29
Std Dev	15.2

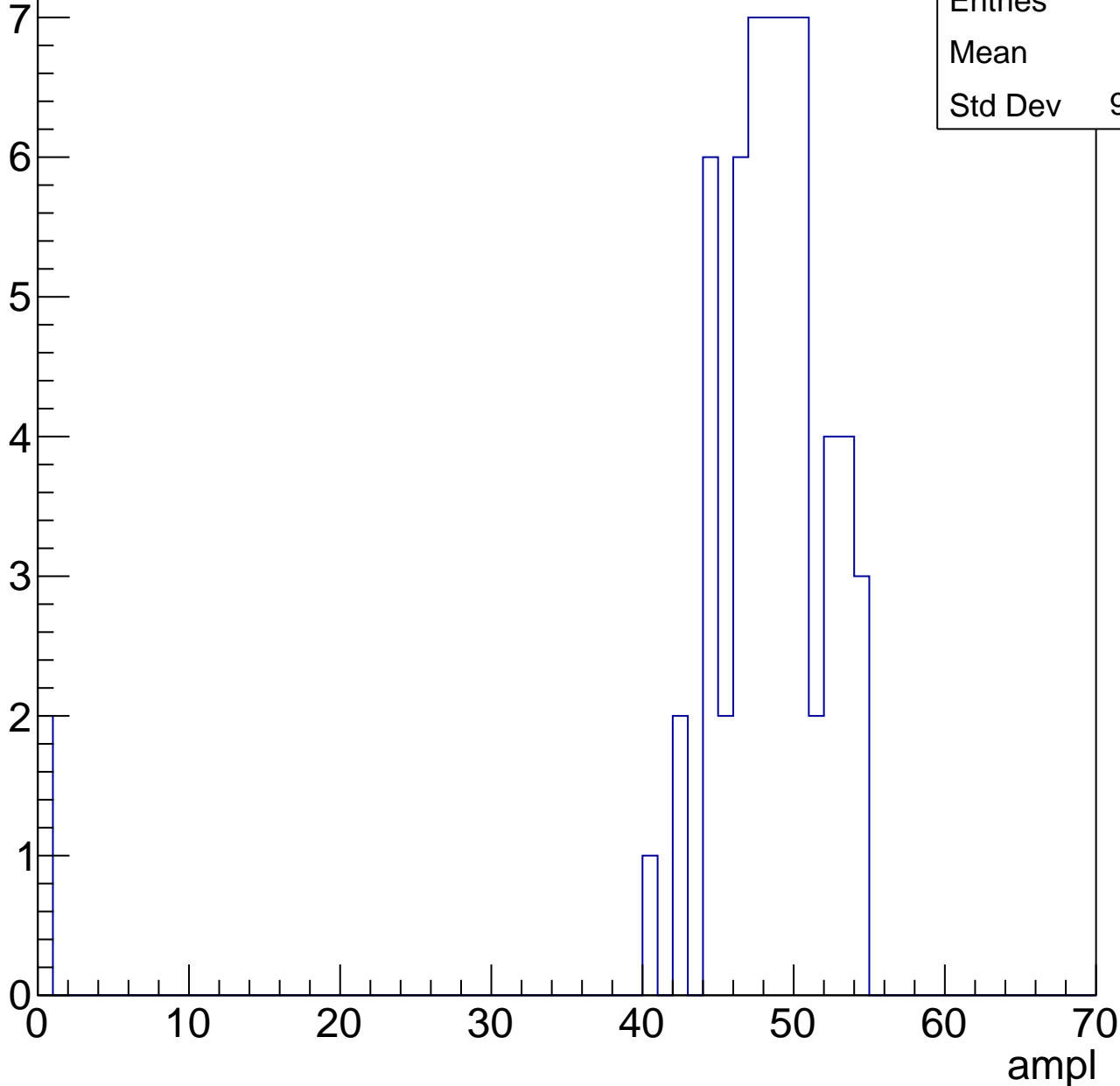


B1L103S, U12-ch4, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	46.6
Std Dev	9.216

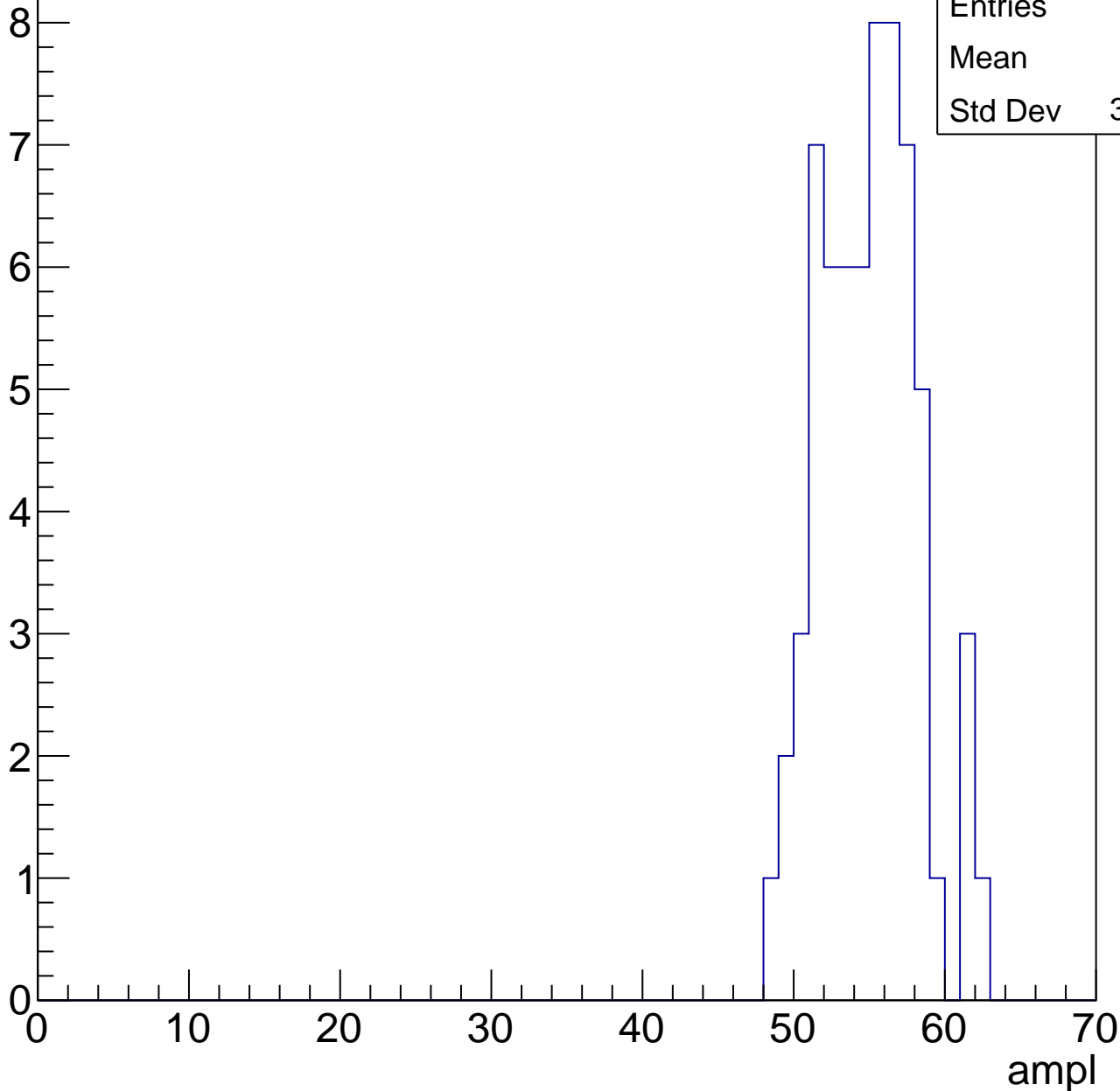


B1L103S, U12-ch4, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	54.5
Std Dev	3.137

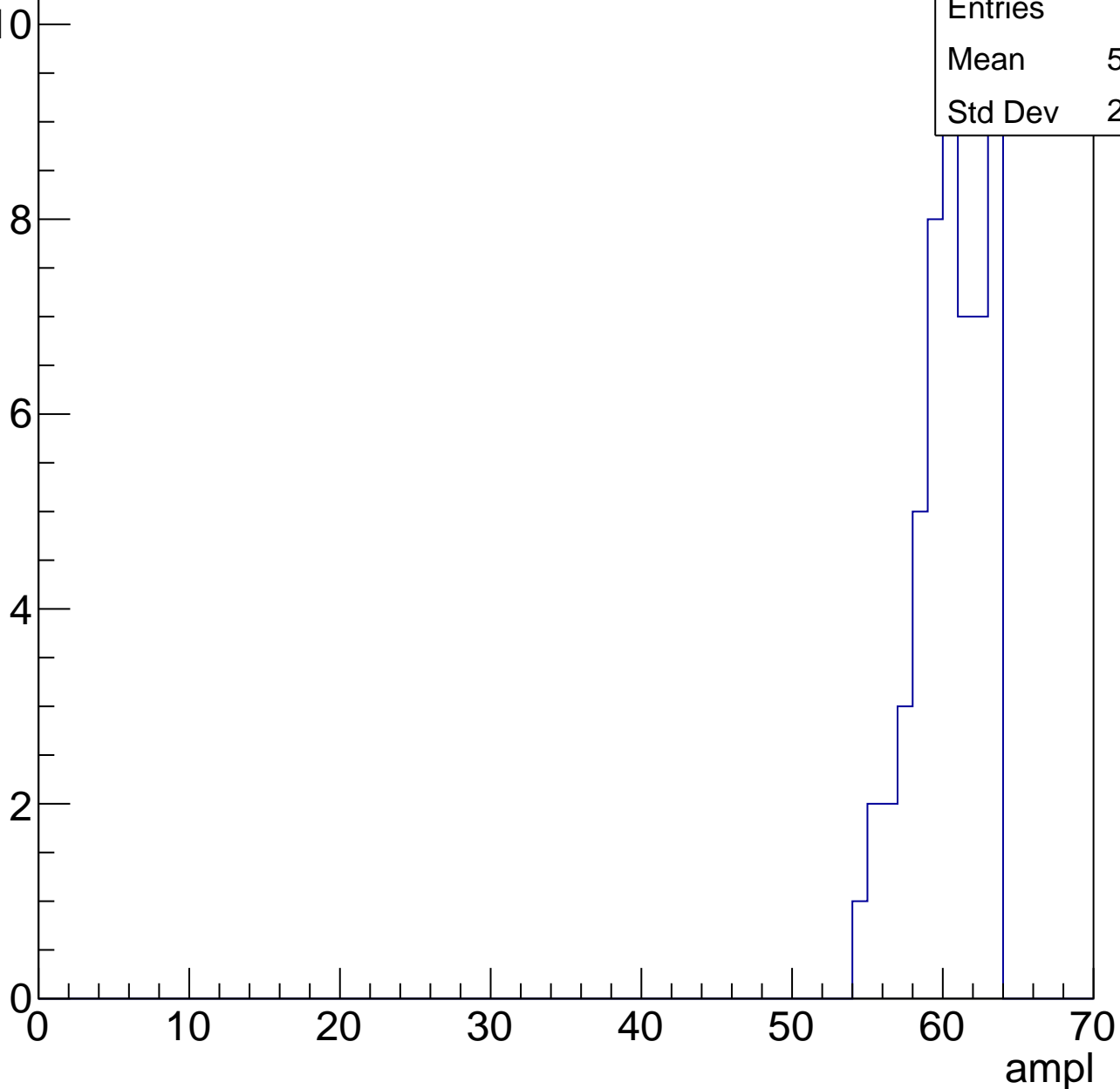


B1L103S, U12-ch4, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

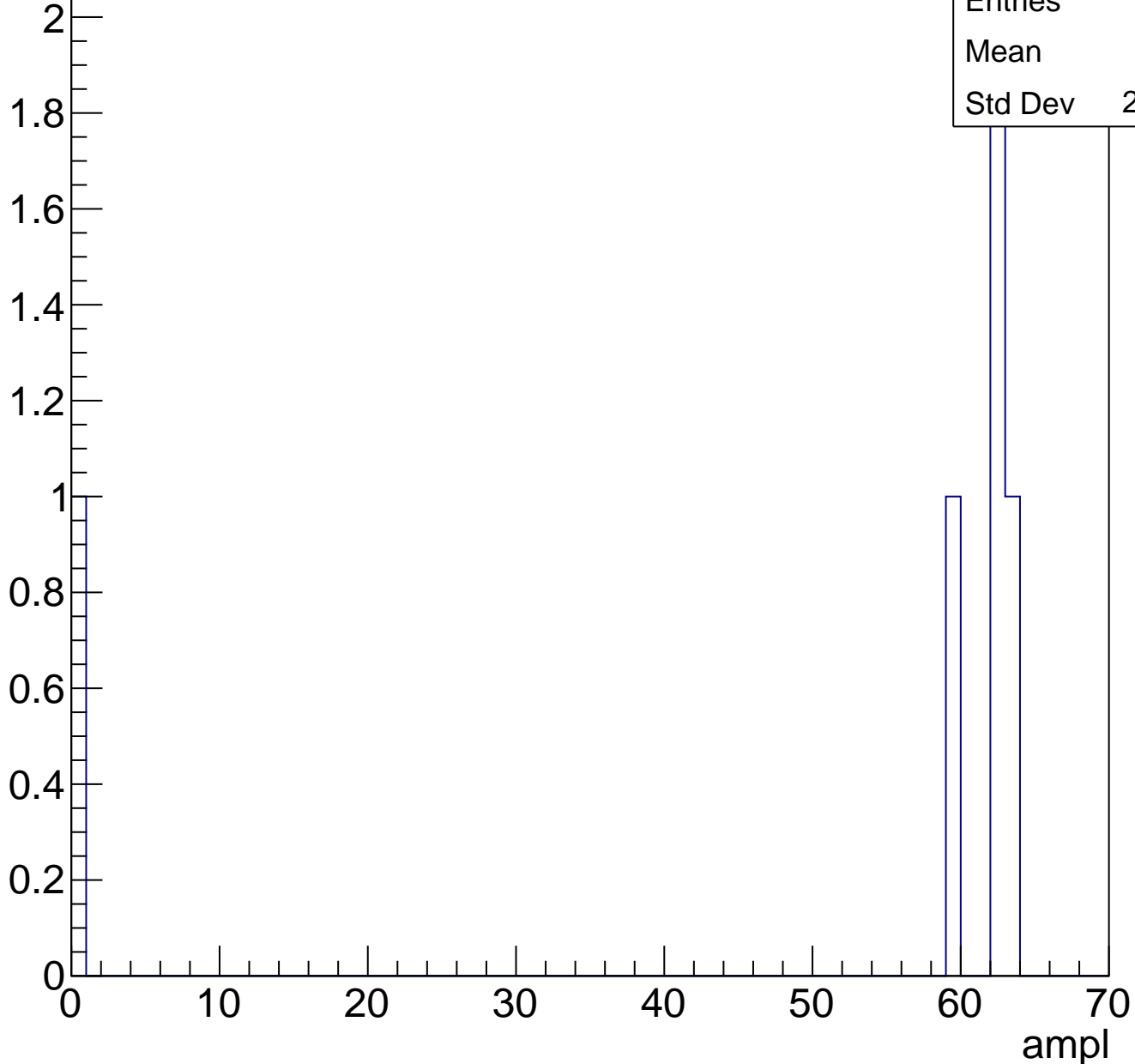
Entries	54
Mean	59.94
Std Dev	2.313



B1L103S, U12-ch4, adc6

calib_packv5_041523_1651.root, FC#0, port C2

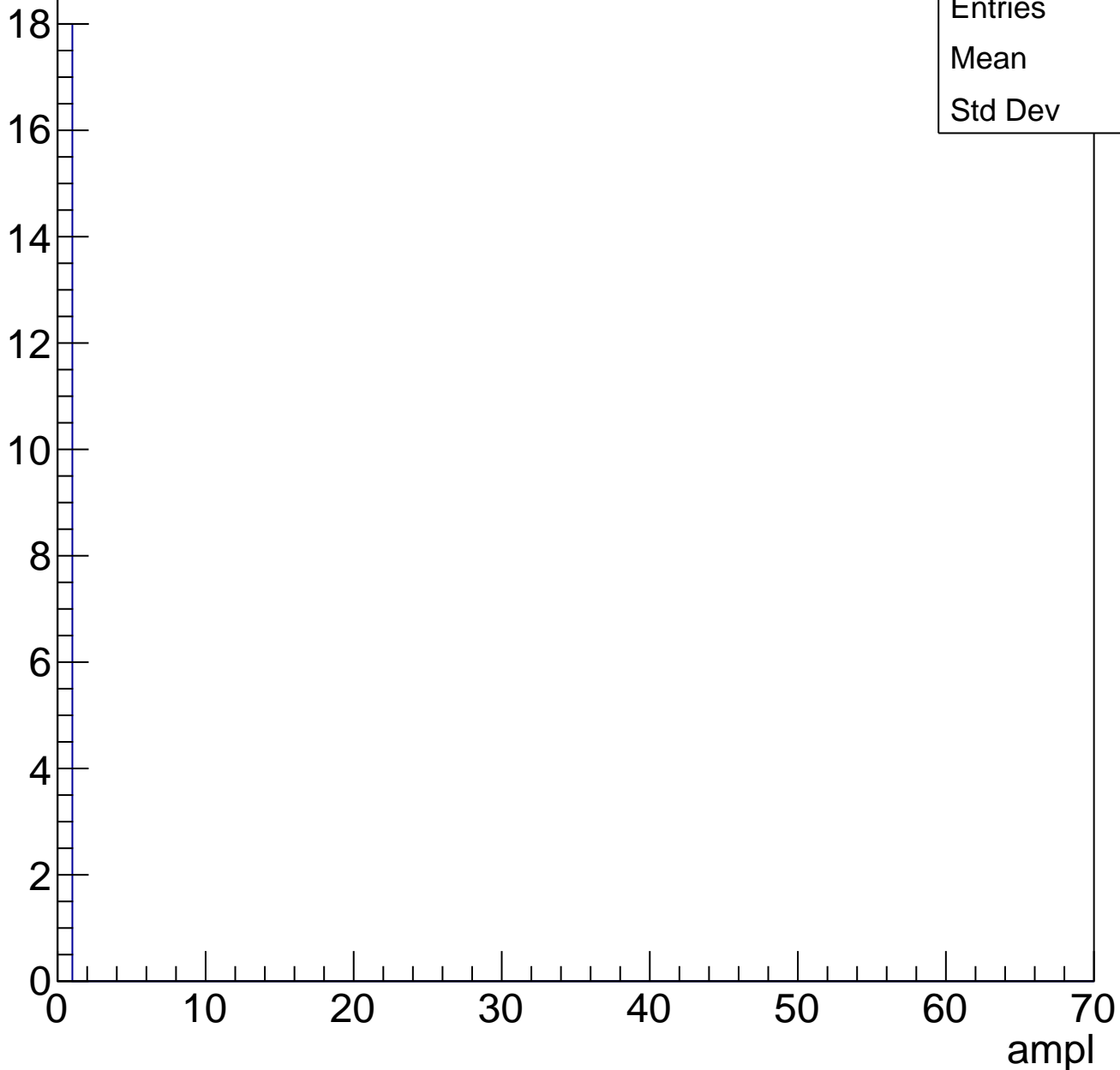
Entry



B1L103S, U12-ch4, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch5, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	61
Mean	27.64
Std Dev	7.013

Entry

10

8

6

4

2

0

0

10

20

30

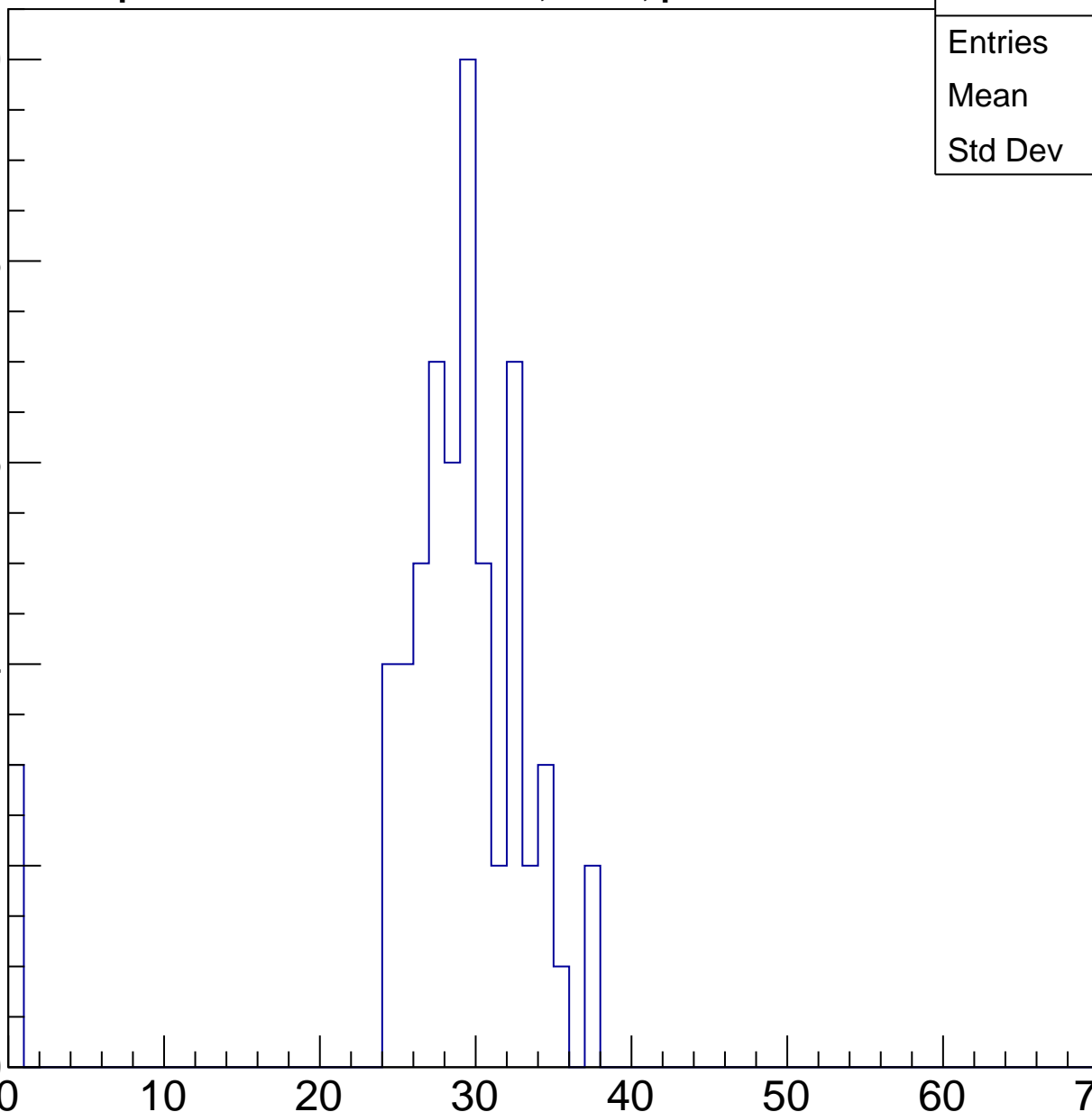
40

50

60

70

ampl

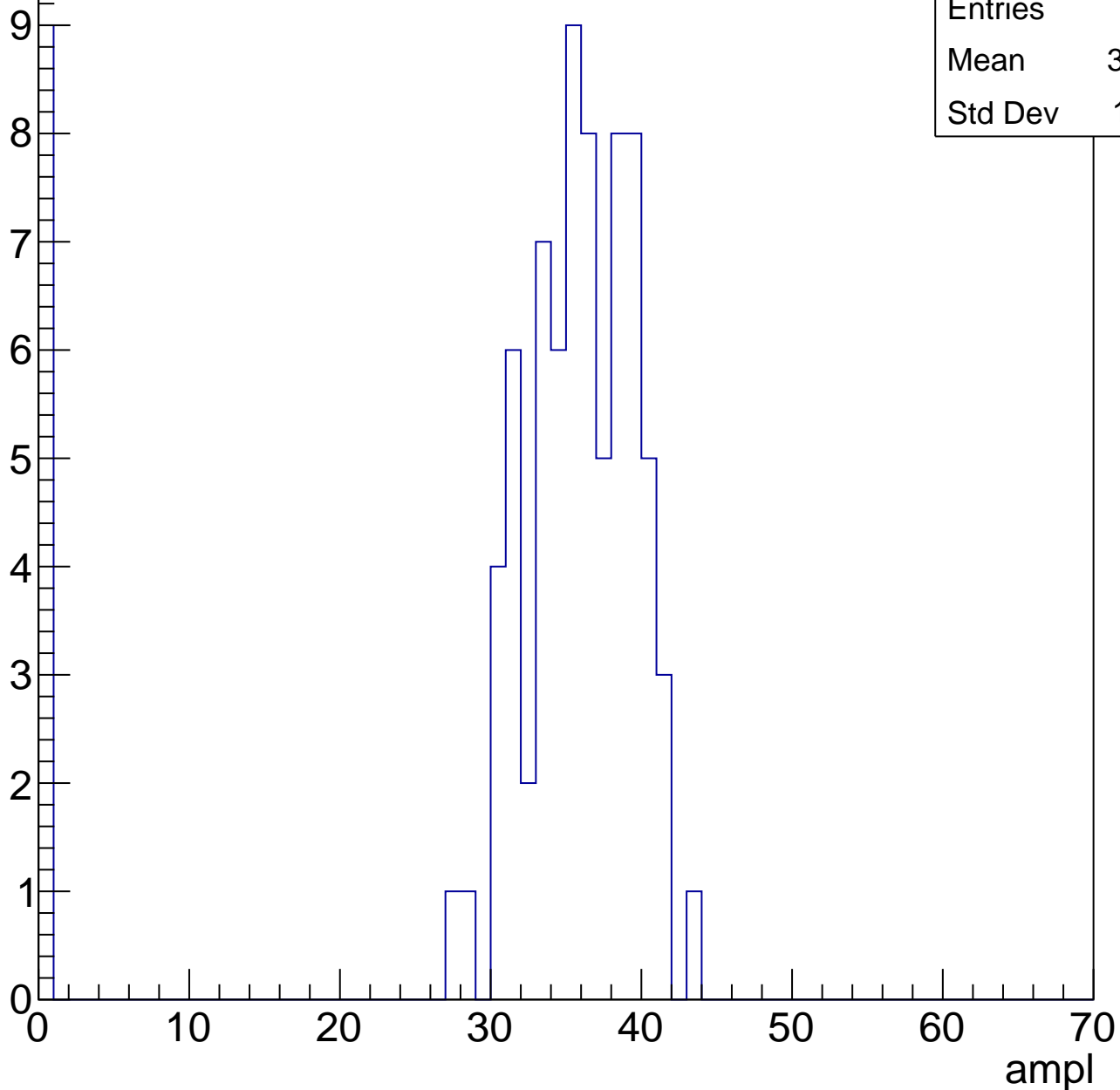


B1L103S, U12-ch5, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	83
Mean	31.69
Std Dev	11.51

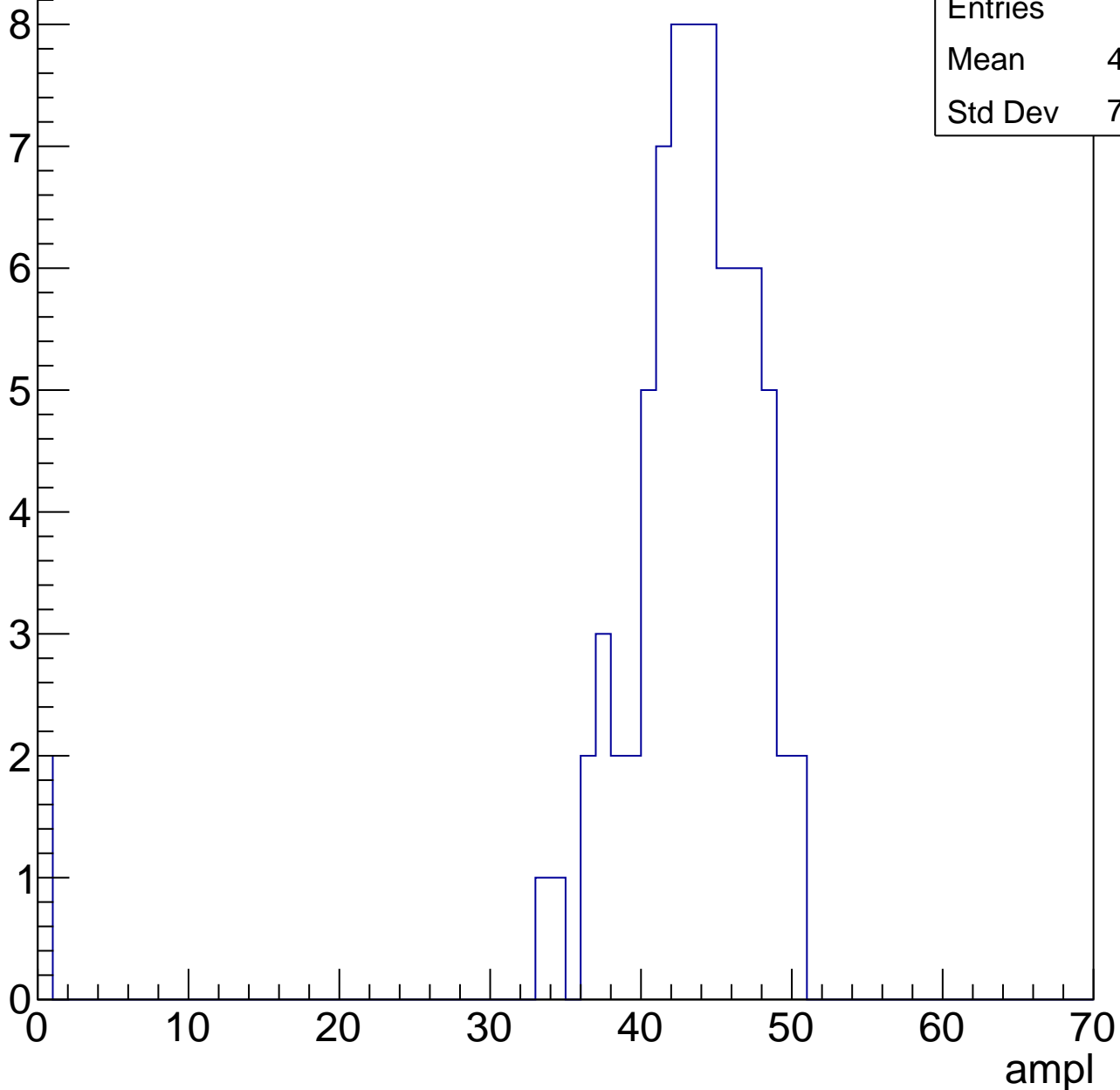


B1L103S, U12-ch5, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	76
Mean	41.96
Std Dev	7.816

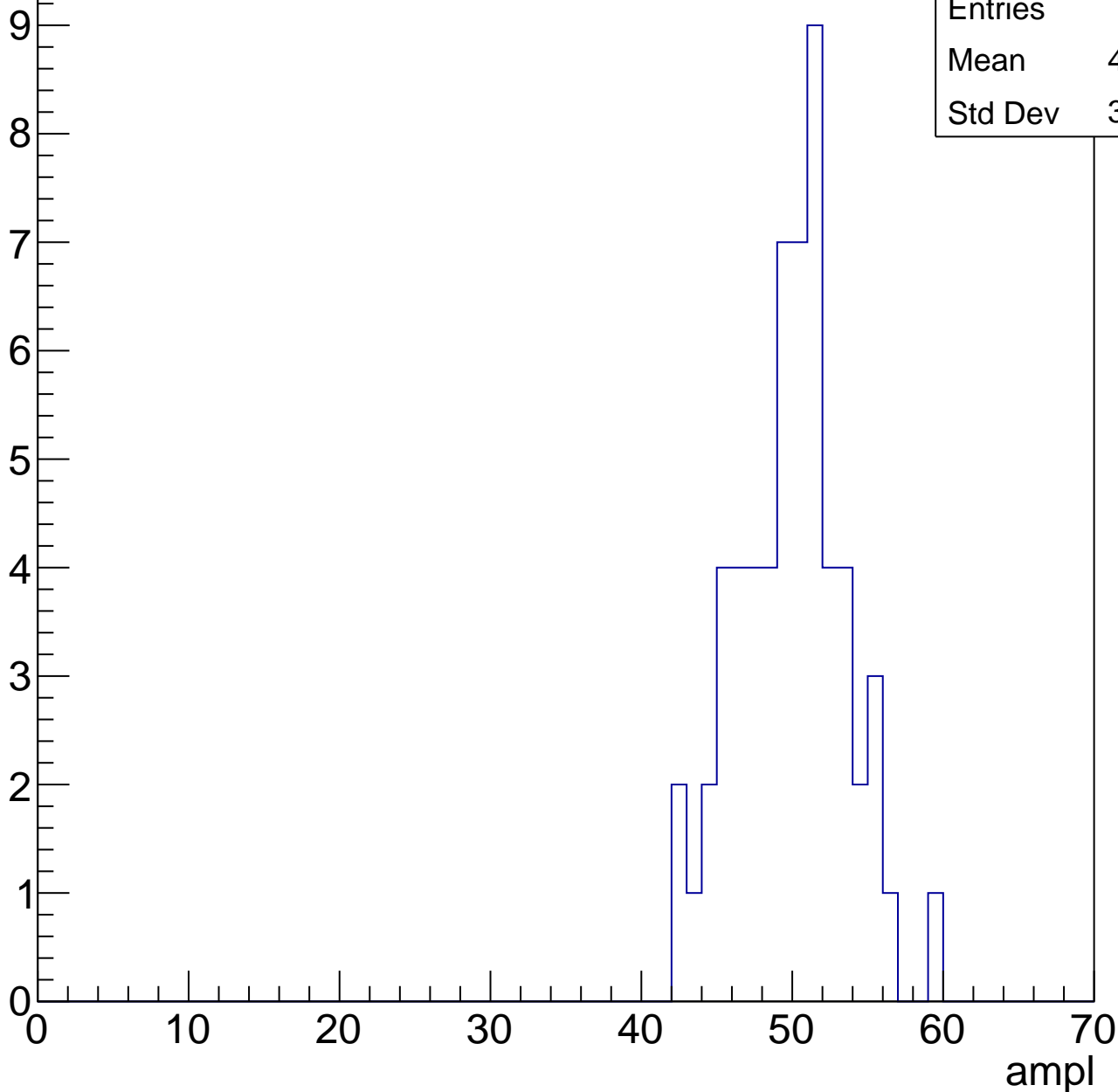


B1L103S, U12-ch5, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	49.47
Std Dev	3.543



B1L103S, U12-ch5, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

7
6
5
4
3
2
1
0

Entries	57
Mean	55.54
Std Dev	3.212

0

1

2

3

4

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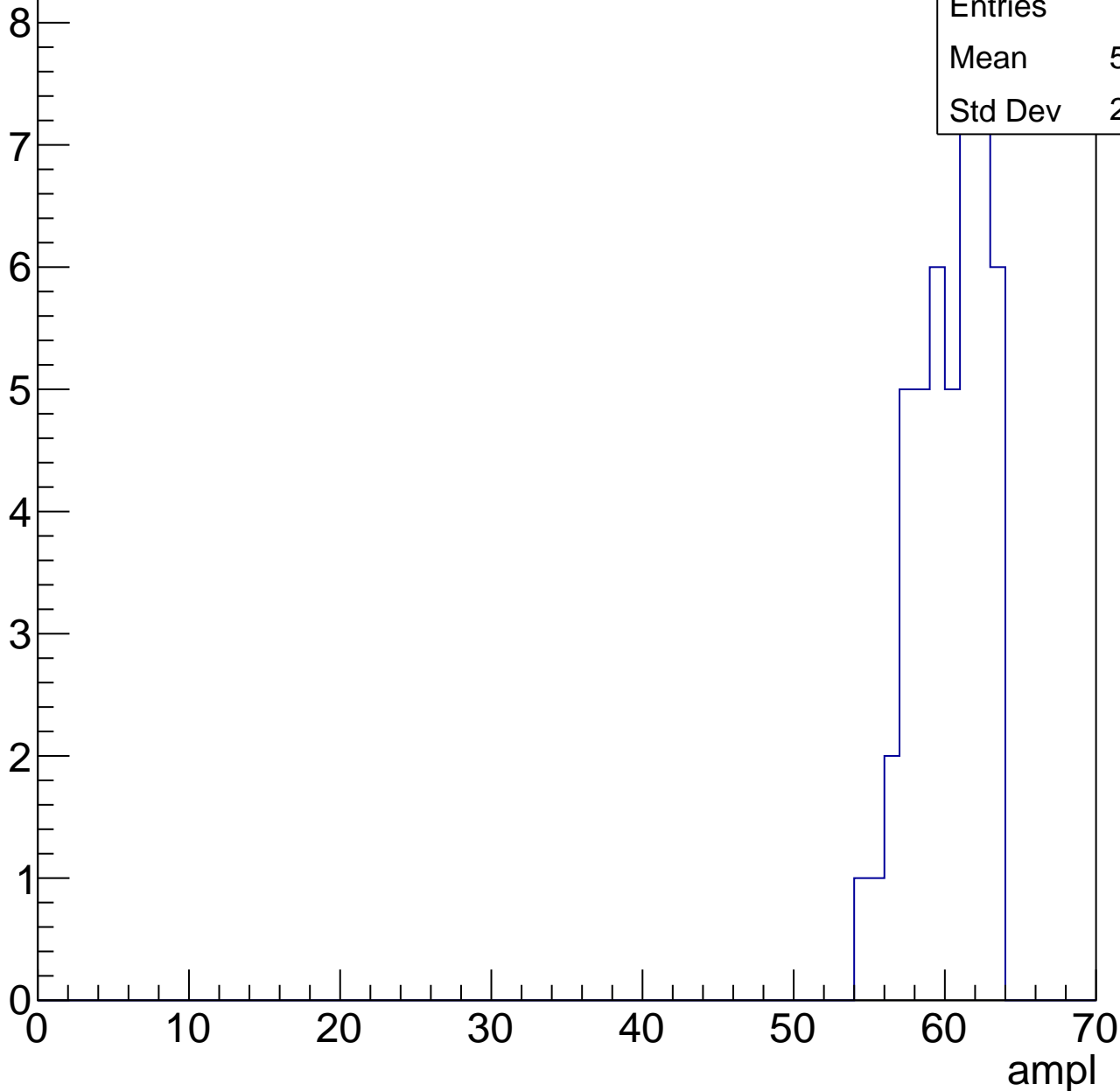
391

B1L103S, U12-ch5, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

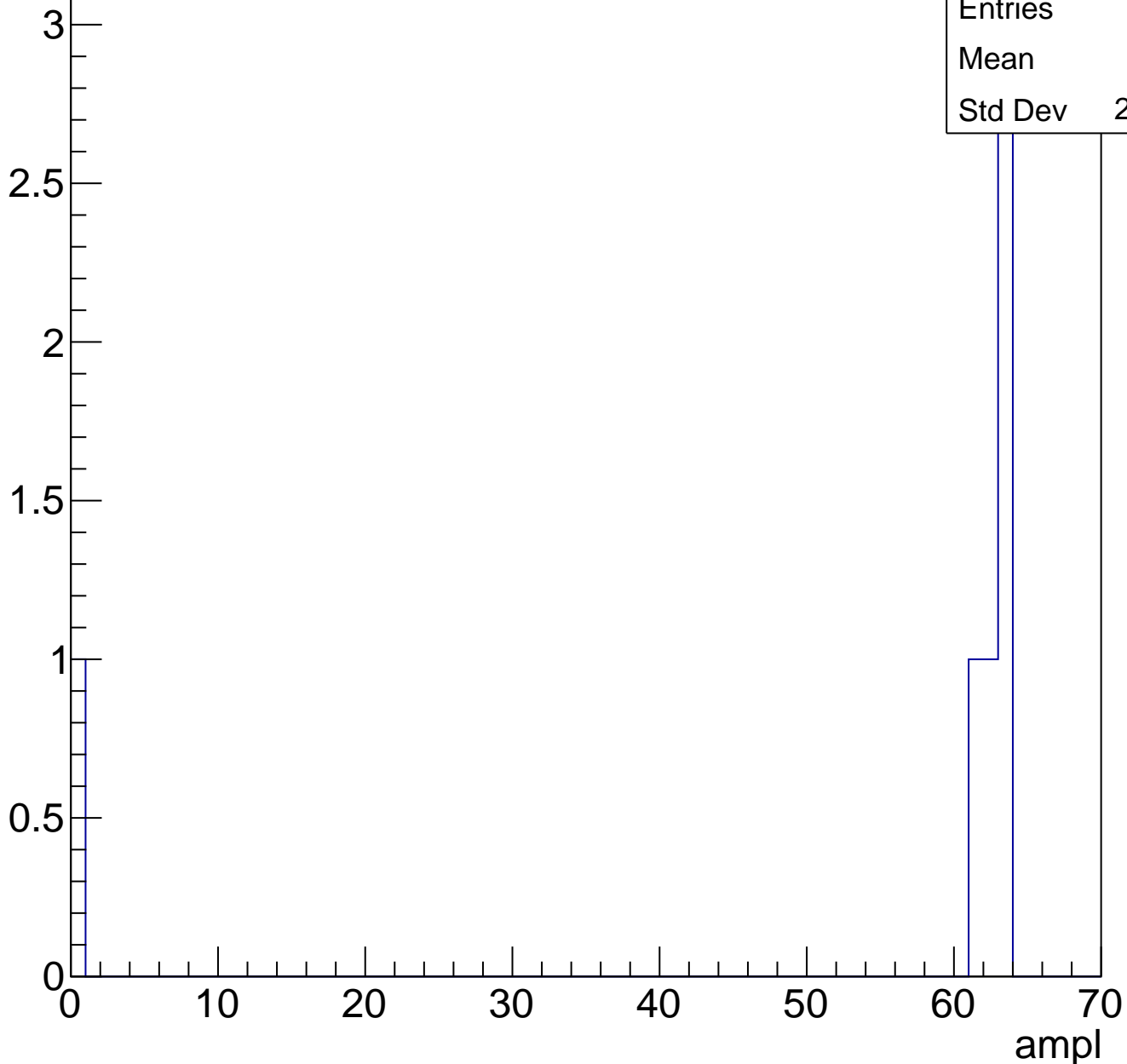
Entries	47
Mean	59.83
Std Dev	2.337



B1L103S, U12-ch5, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	6
Mean	52
Std Dev	23.27

B1L103S, U12-ch5, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

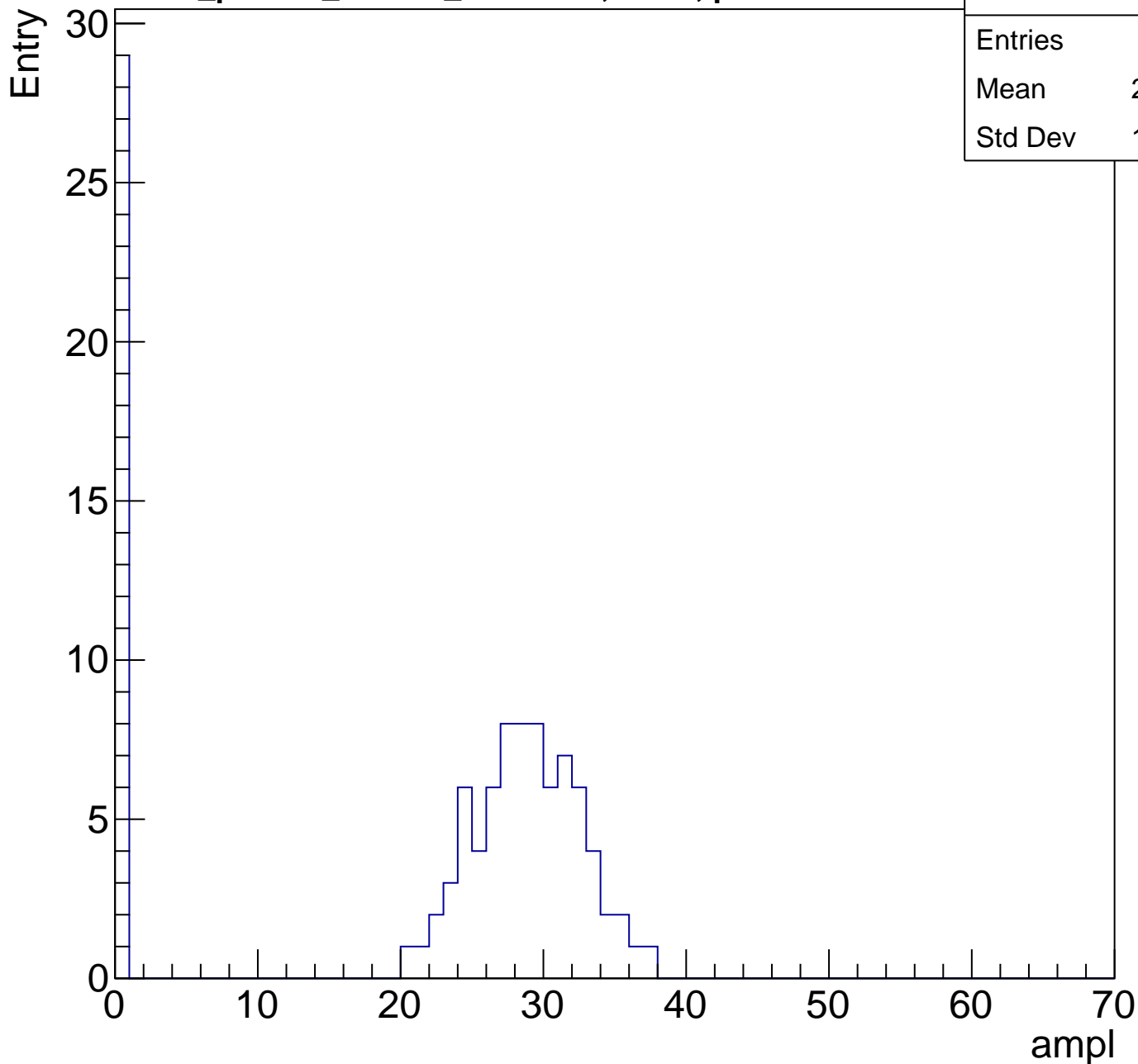
Entries	19
Mean	0
Std Dev	0

ampl

B1L103S, U12-ch6, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	105
Mean	20.55
Std Dev	13.07



B1L103S, U12-ch6, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	84
Mean	31
Std Dev	12.43

Entry

10

8

6

4

2

0

0

10

20

30

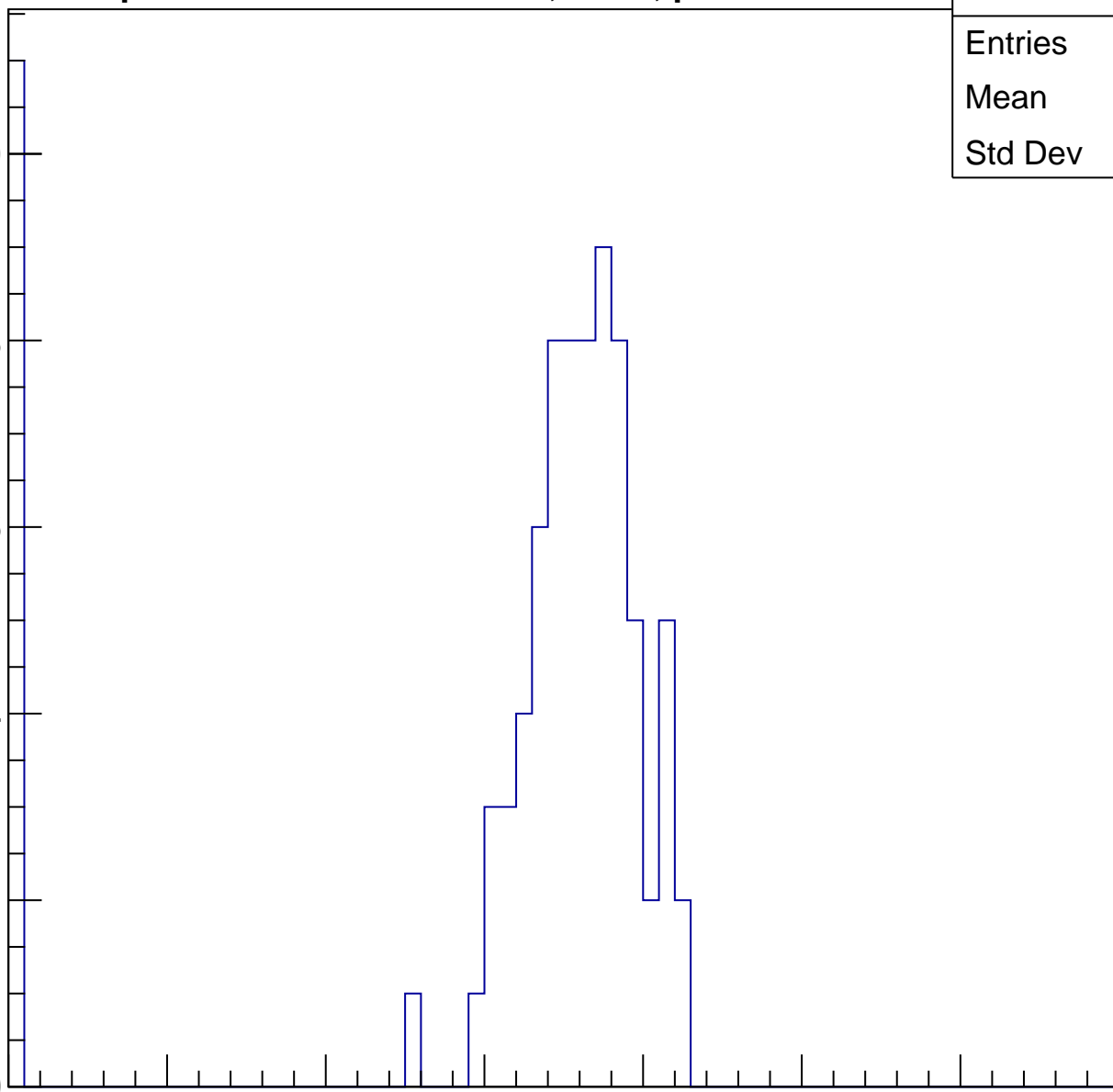
40

50

60

70

ampl



B1L103S, U12-ch6, adc2

calib_packv5_041523_1651.root, FC#0, port C2

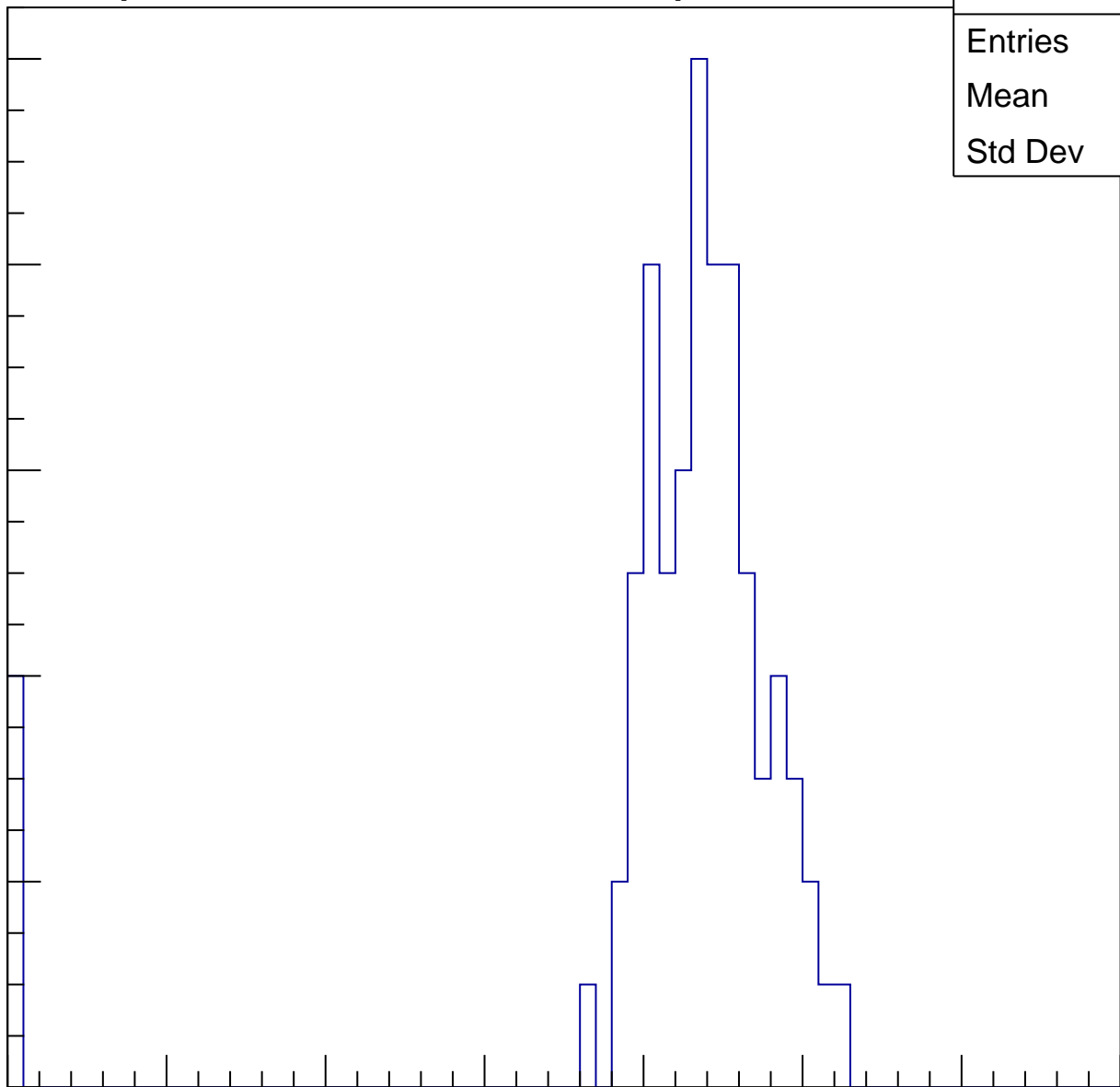
Entries	76
Mean	41.3
Std Dev	10.28

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

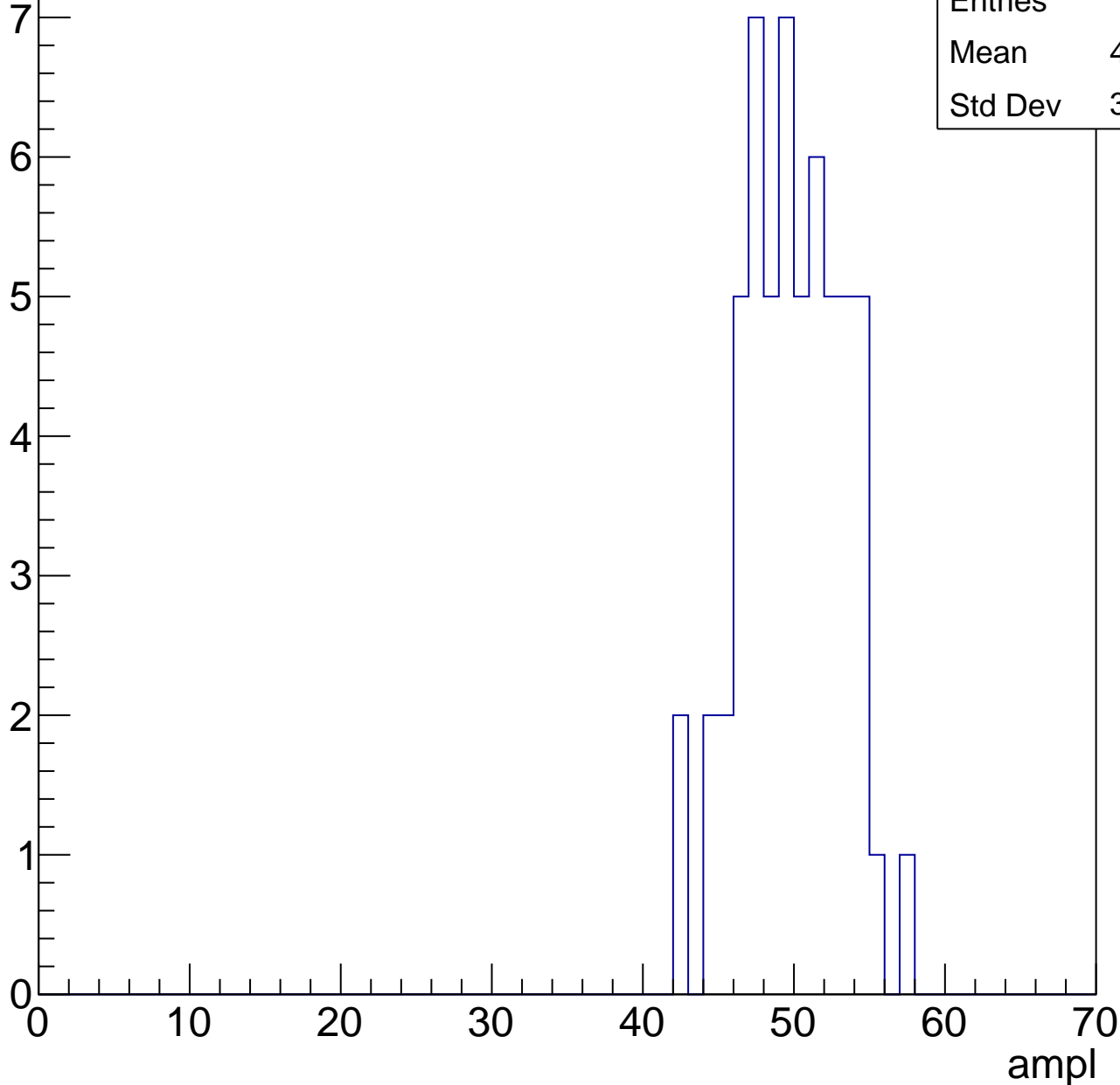
ampl



B1L103S, U12-ch6, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry



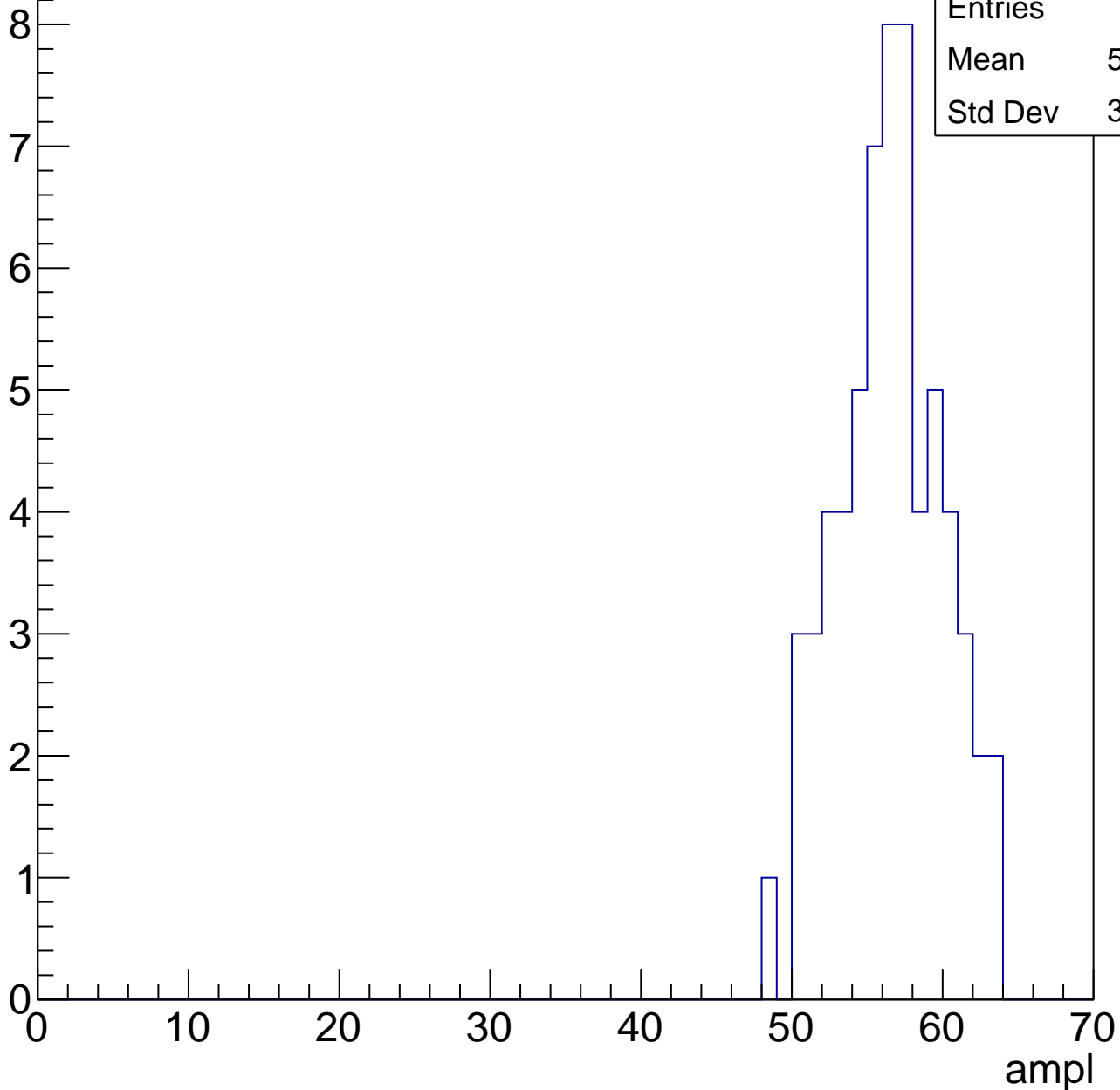
Entries	58
Mean	49.43
Std Dev	3.286

B1L103S, U12-ch6, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	63
Mean	56.03
Std Dev	3.455

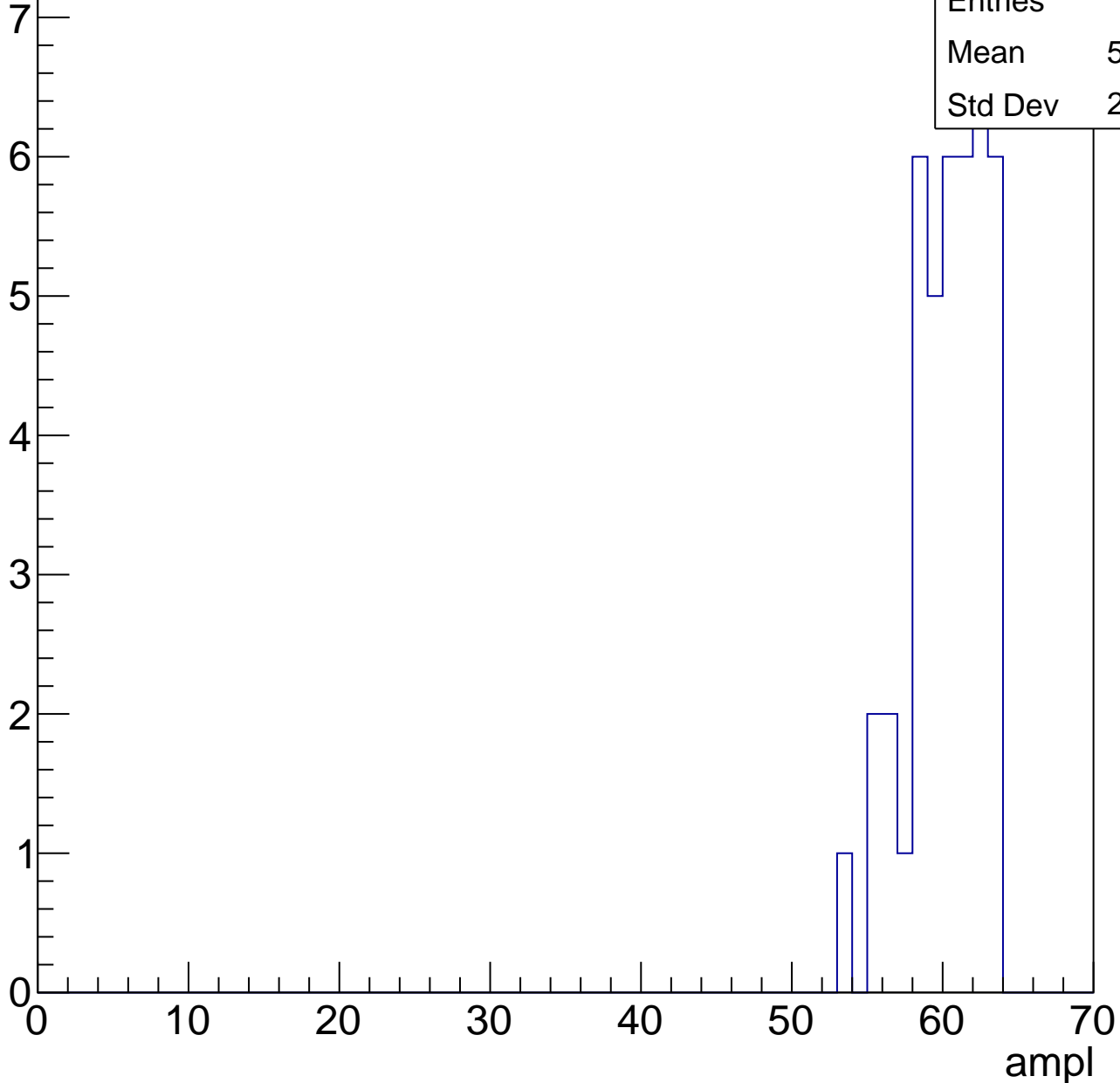


B1L103S, U12-ch6, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

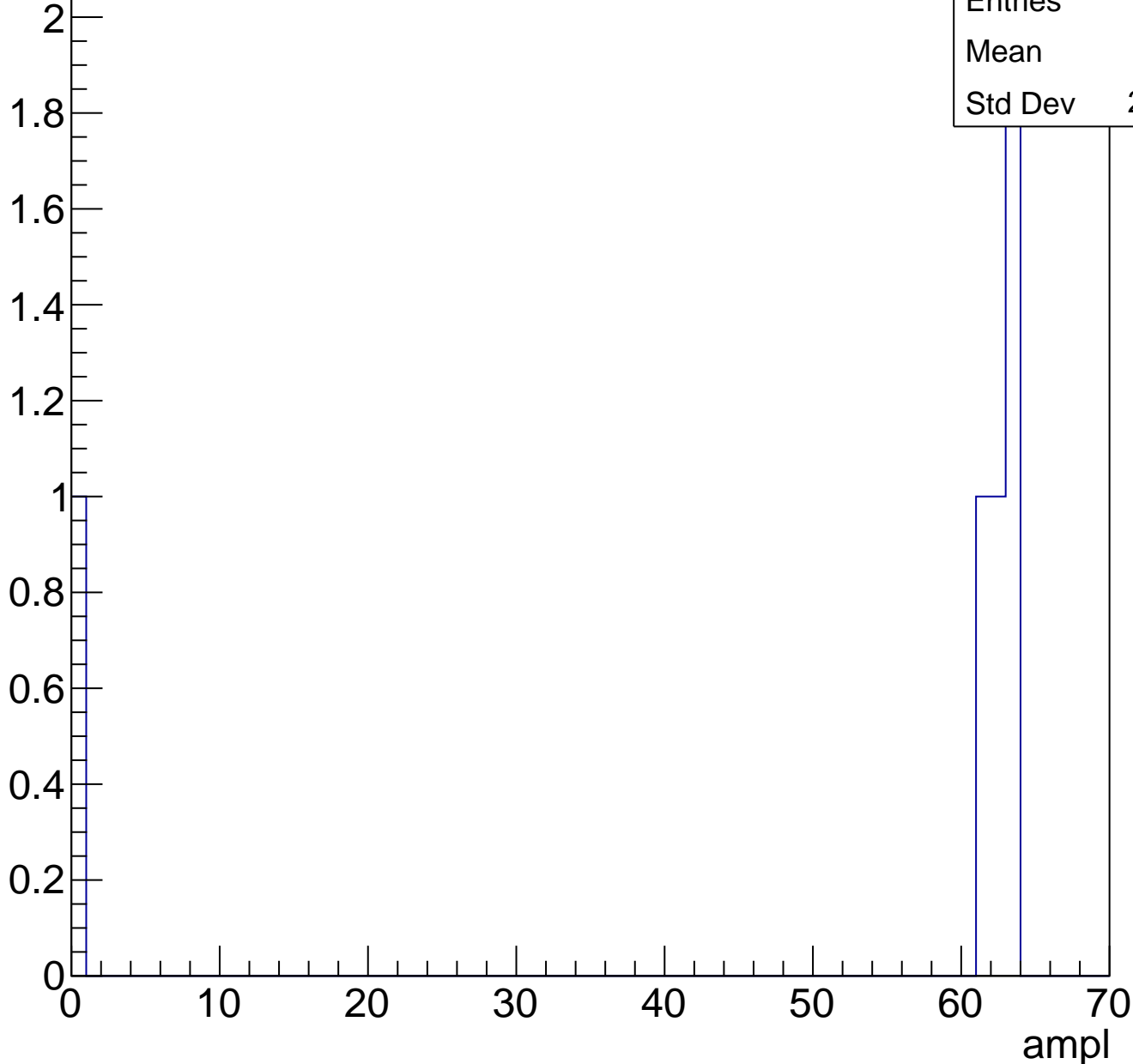
Entries	42
Mean	59.83
Std Dev	2.468



B1L103S, U12-ch6, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	5
Mean	49.8
Std Dev	24.91

B1L103S, U12-ch6, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

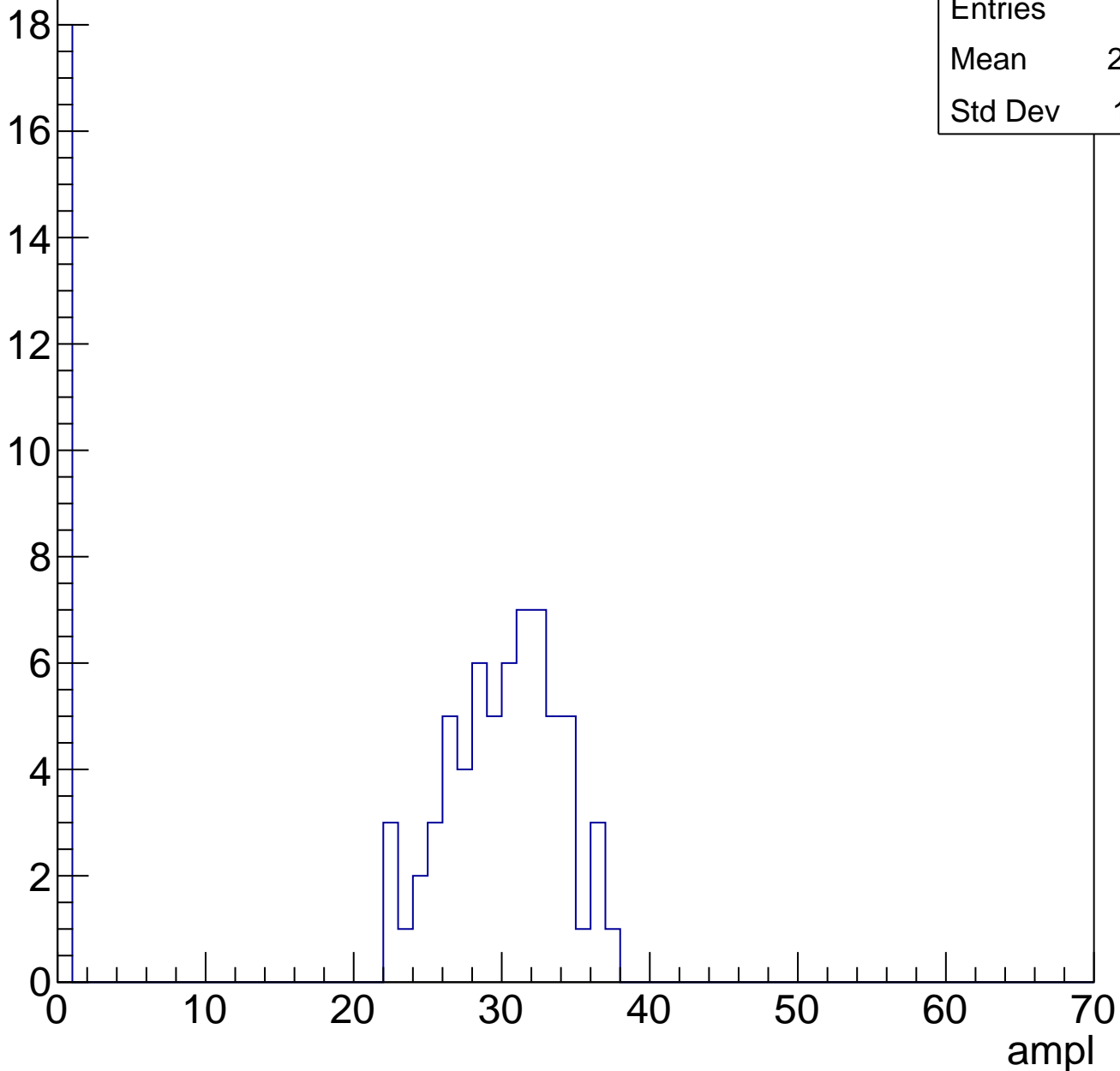
Entries	19
Mean	0
Std Dev	0

B1L103S, U12-ch7, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	82
Mean	23.16
Std Dev	12.71

Entry

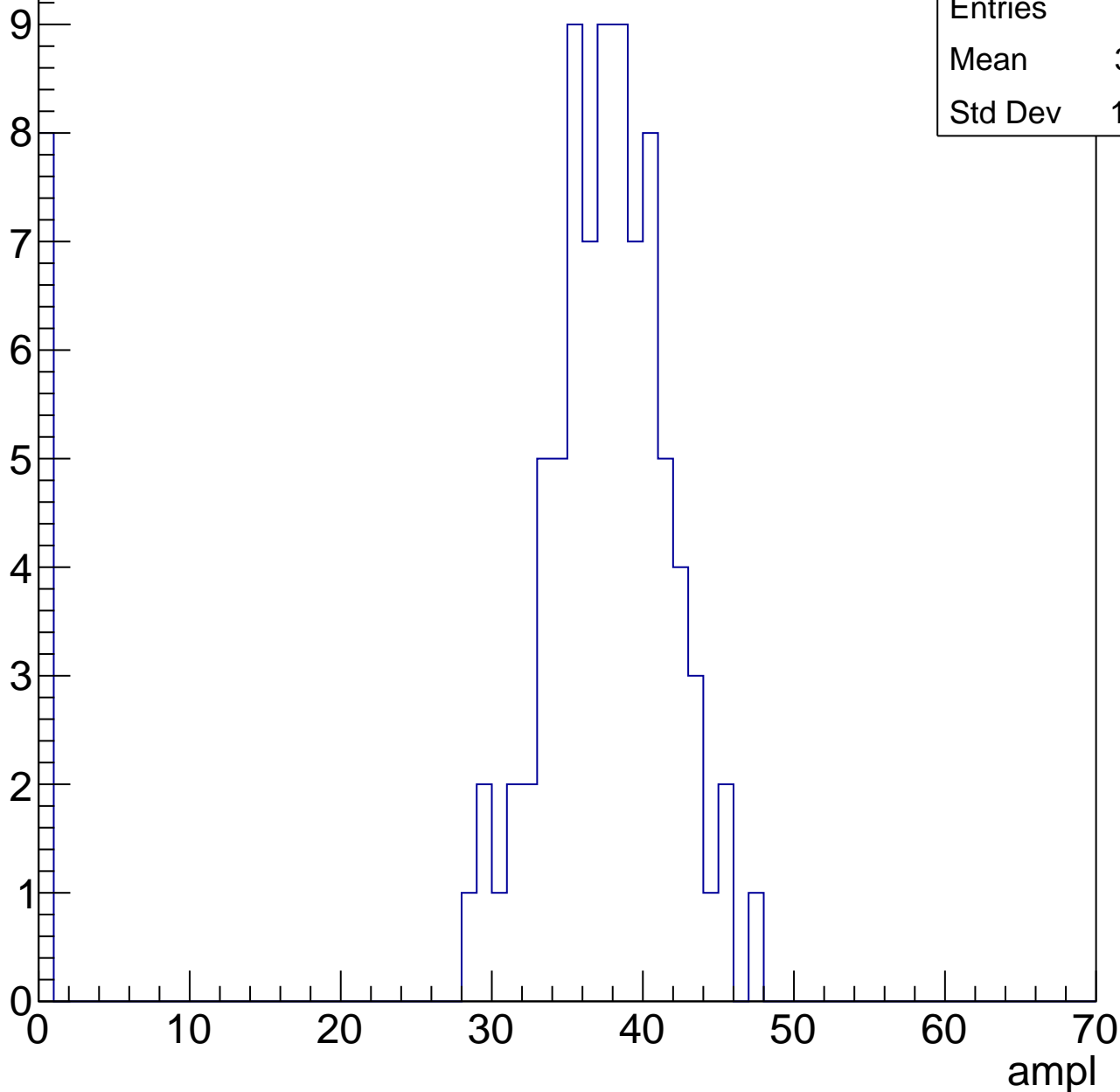


B1L103S, U12-ch7, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	91
Mean	34.01
Std Dev	11.17

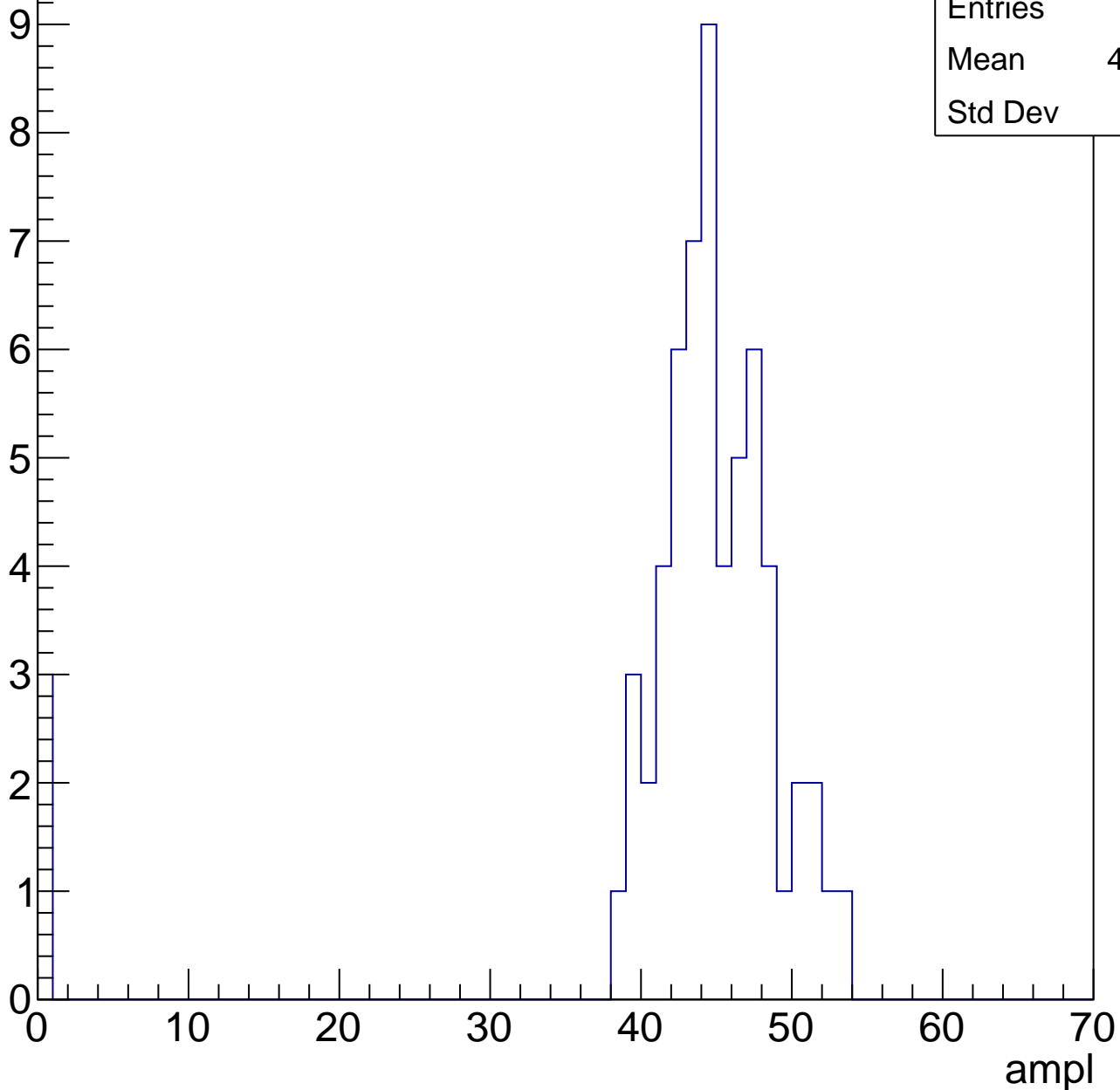


B1L103S, U12-ch7, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	42.43
Std Dev	10.2

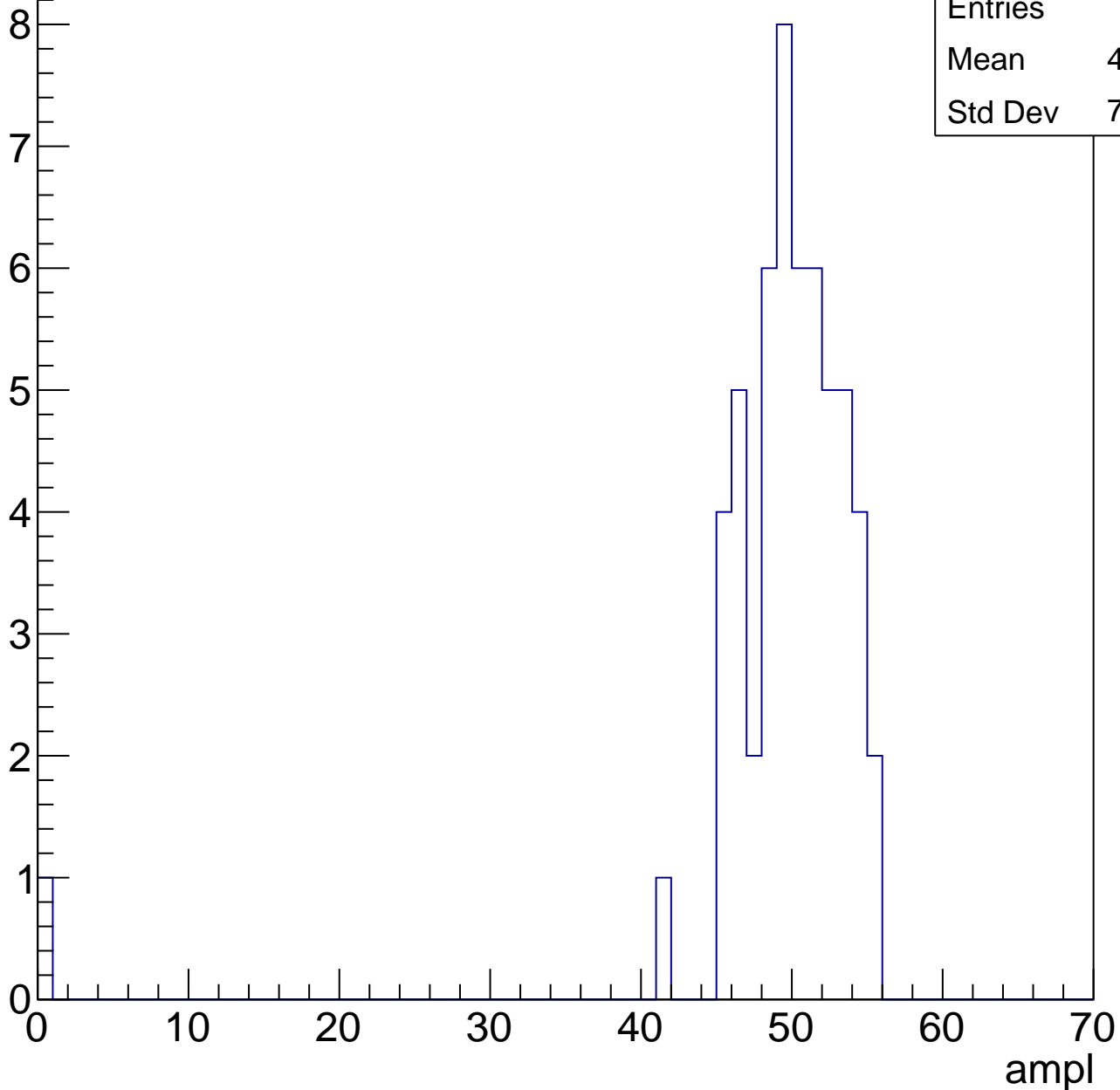


B1L103S, U12-ch7, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	48.76
Std Dev	7.276

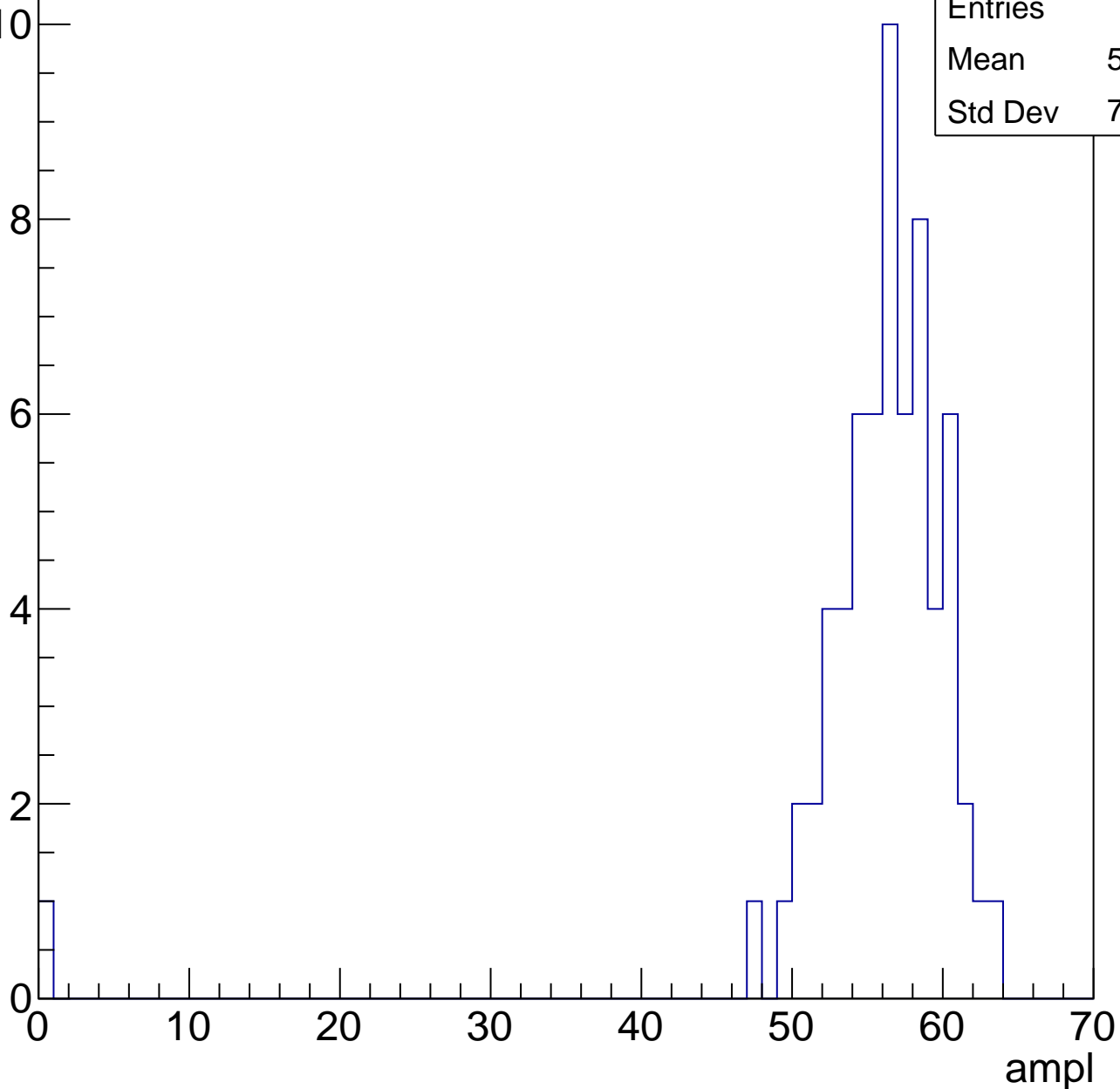


B1L103S, U12-ch7, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	55.09
Std Dev	7.615

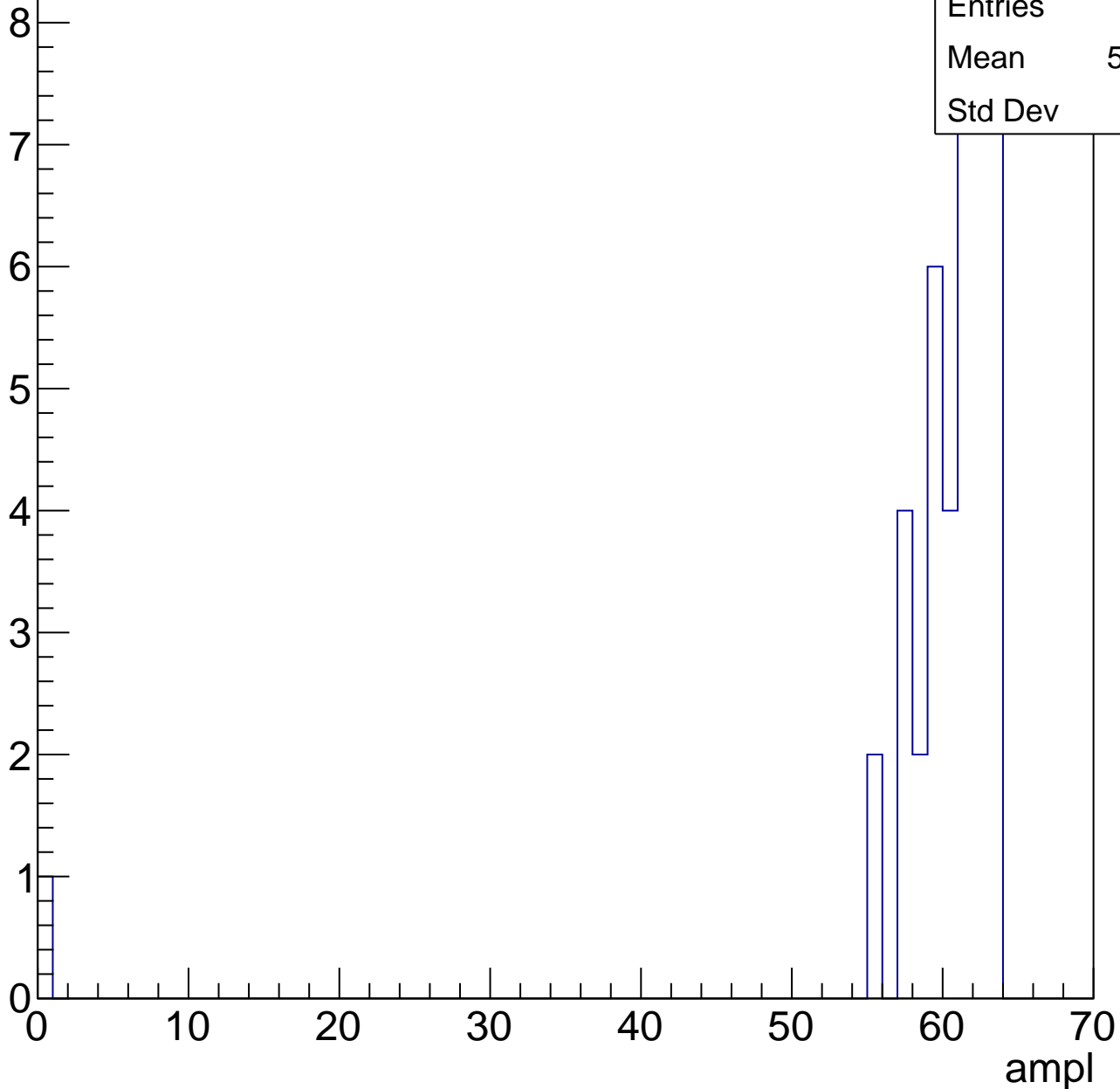


B1L103S, U12-ch7, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	43
Mean	58.98
Std Dev	9.36



B1L103S, U12-ch7, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch7, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

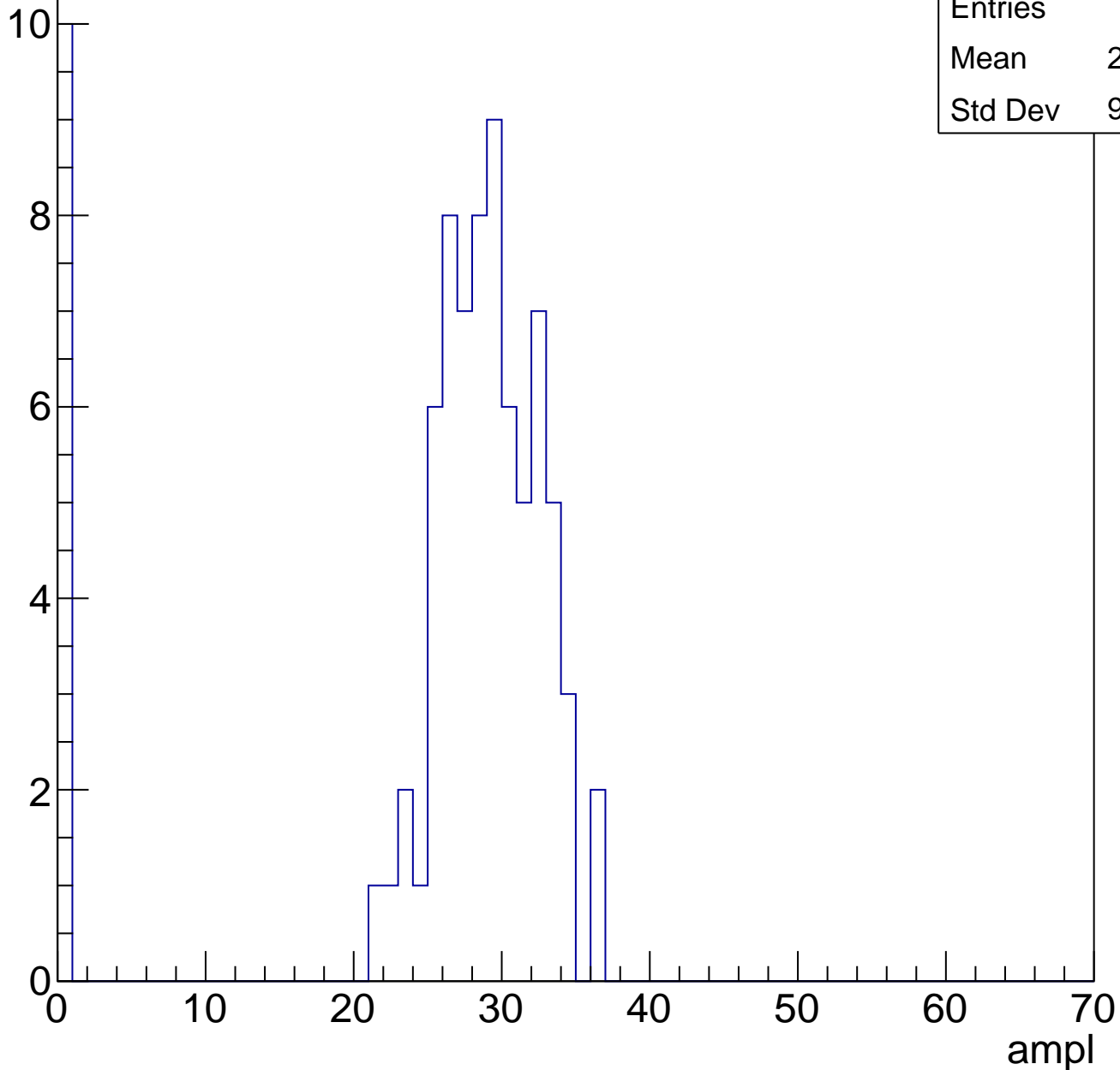
ampl

B1L103S, U12-ch8, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	81
Mean	25.22
Std Dev	9.944

Entry

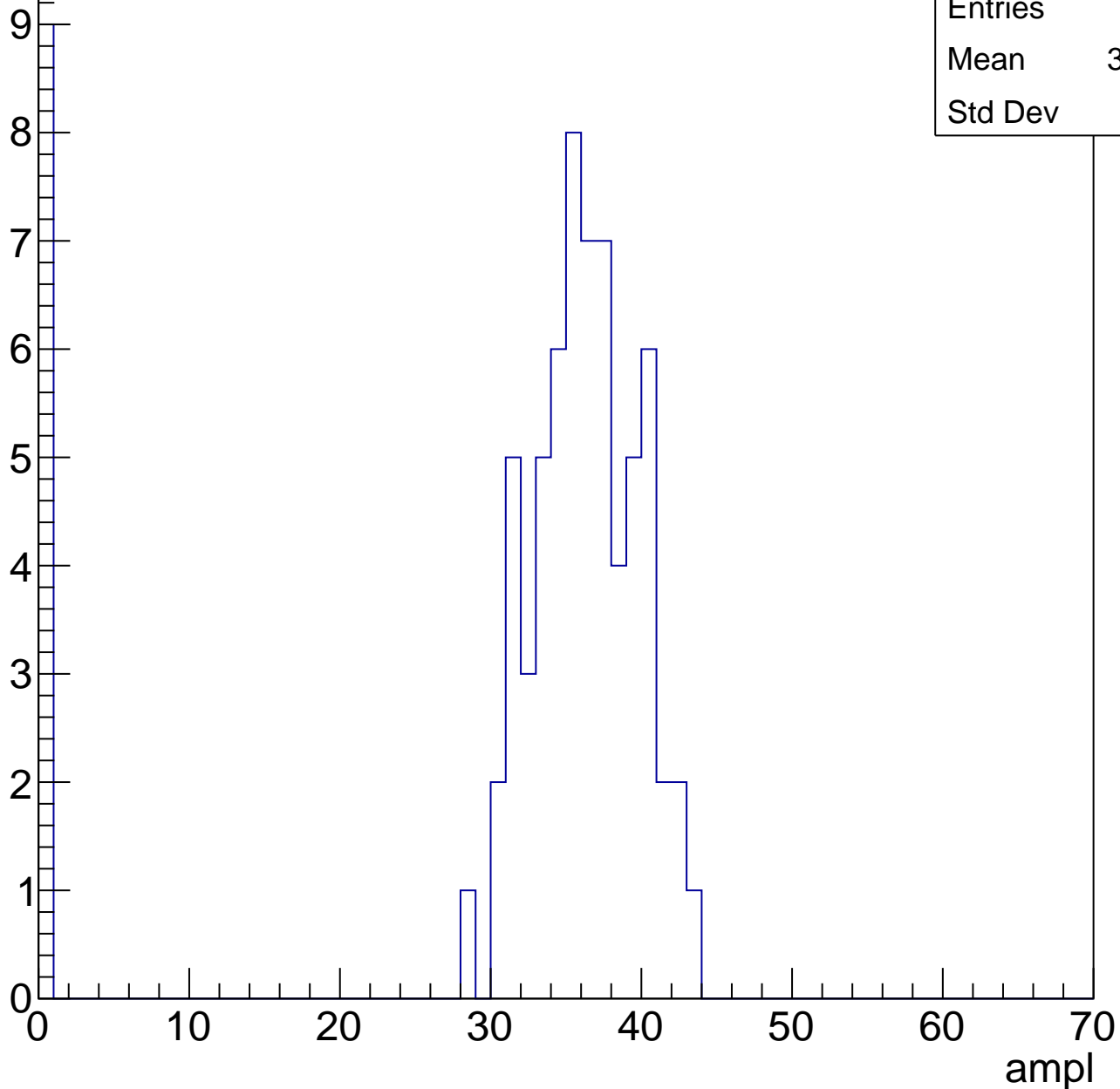


B1L103S, U12-ch8, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	73
Mean	31.44
Std Dev	12.2

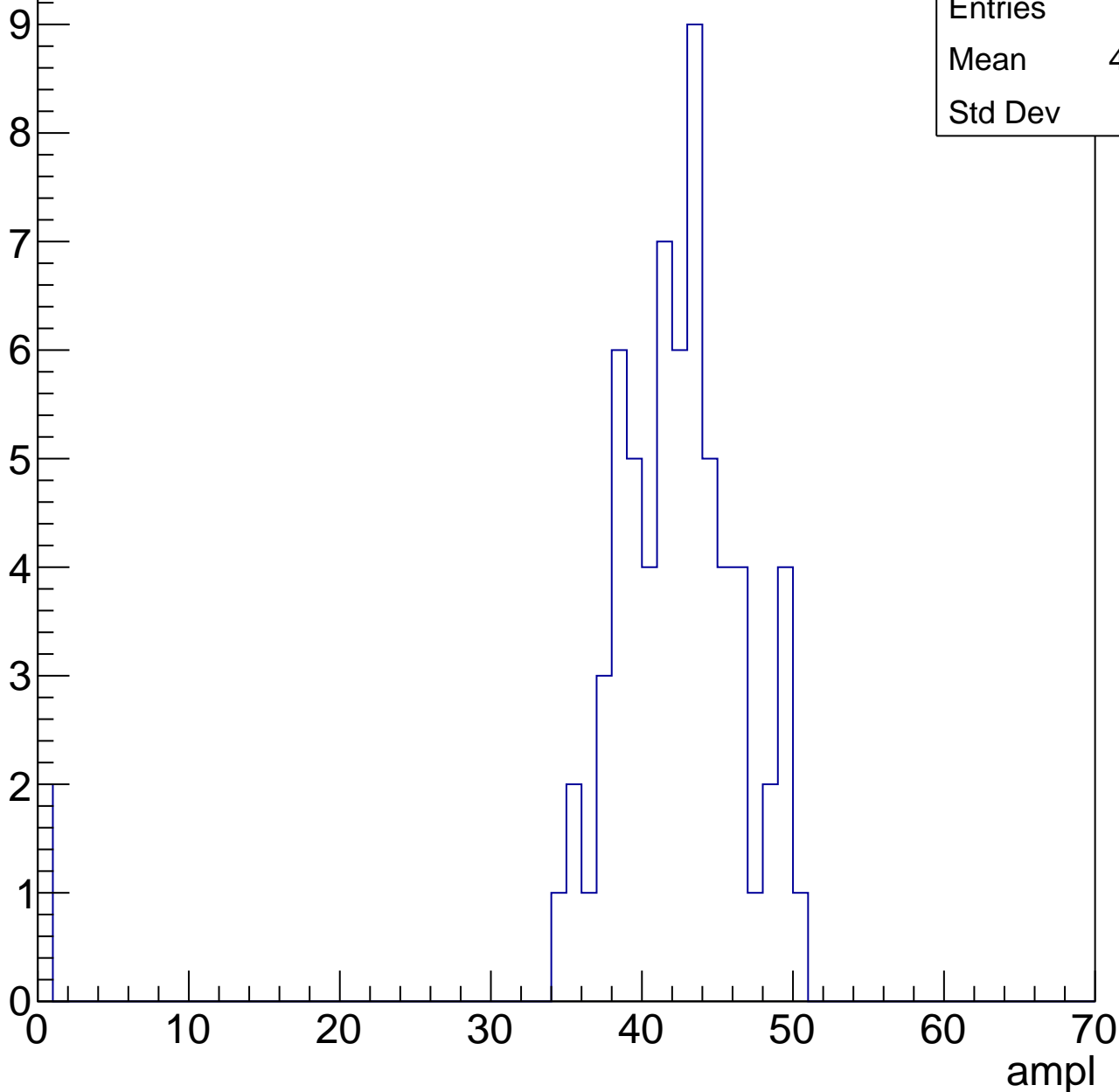


B1L103S, U12-ch8, adc2

calib_packv5_041523_1651.root, FC#0, port C2

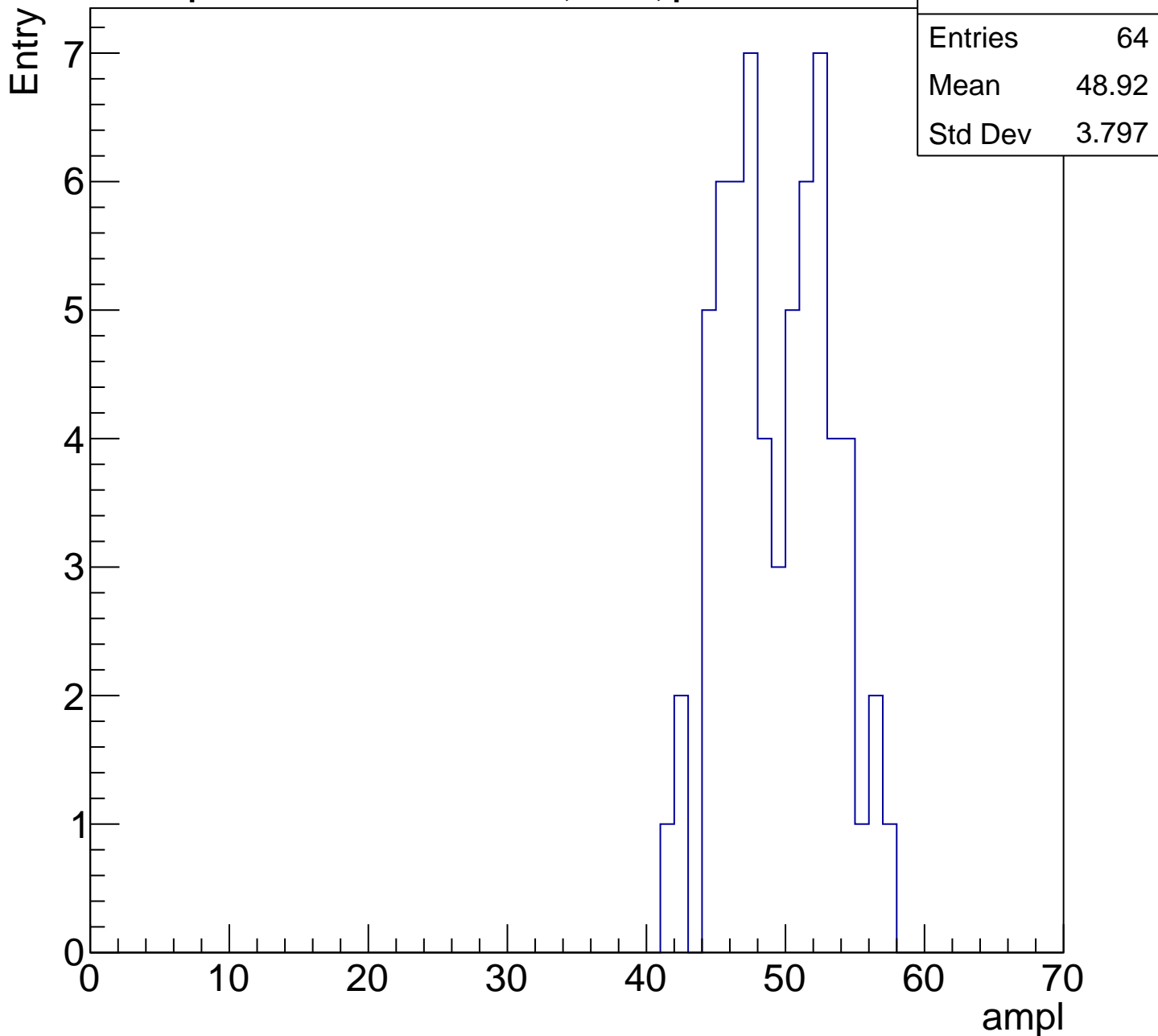
Entry

Entries	67
Mean	40.79
Std Dev	8.06



B1L103S, U12-ch8, adc3

calib_packv5_041523_1651.root, FC#0, port C2

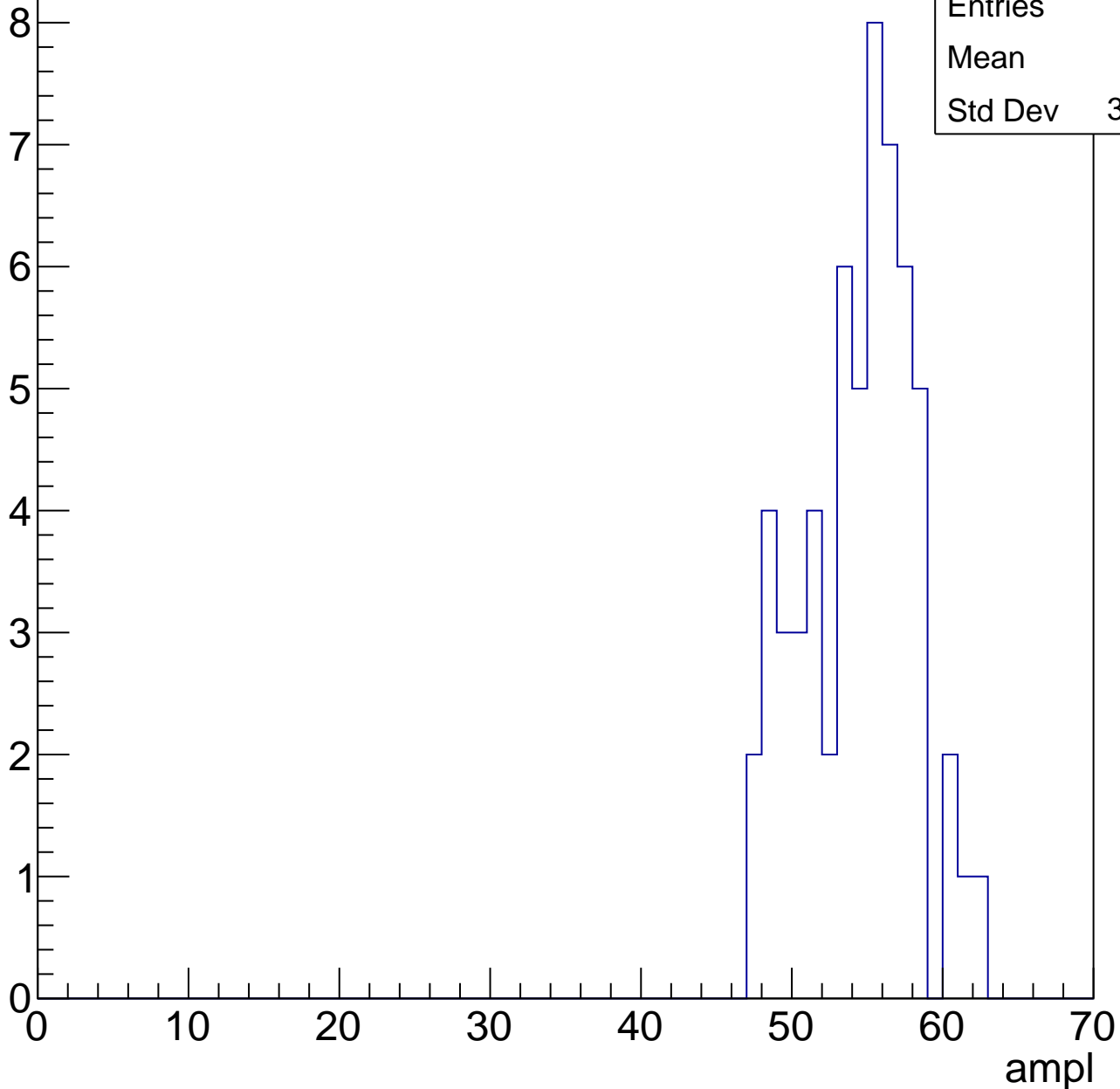


B1L103S, U12-ch8, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	54
Std Dev	3.613

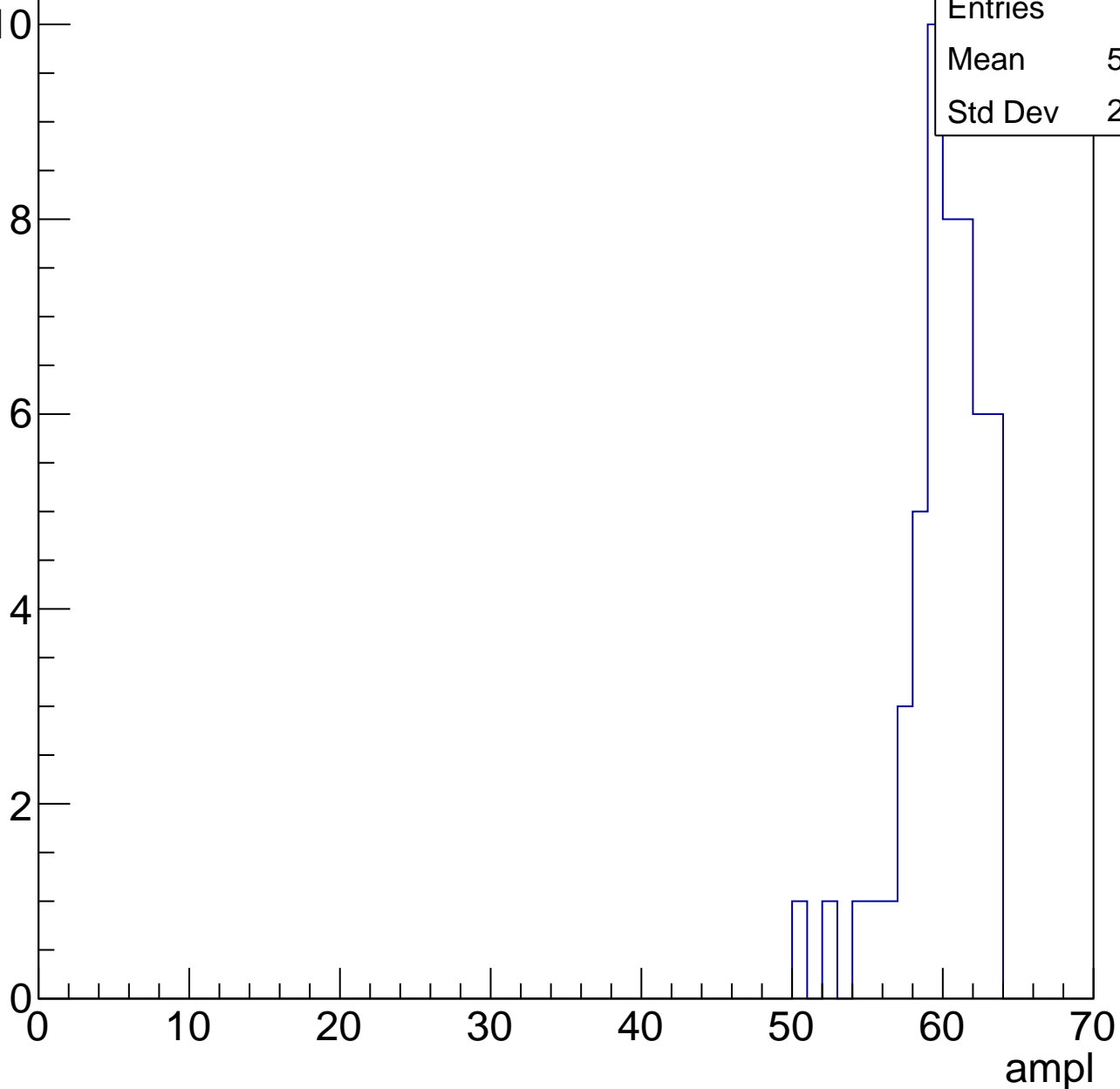


B1L103S, U12-ch8, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

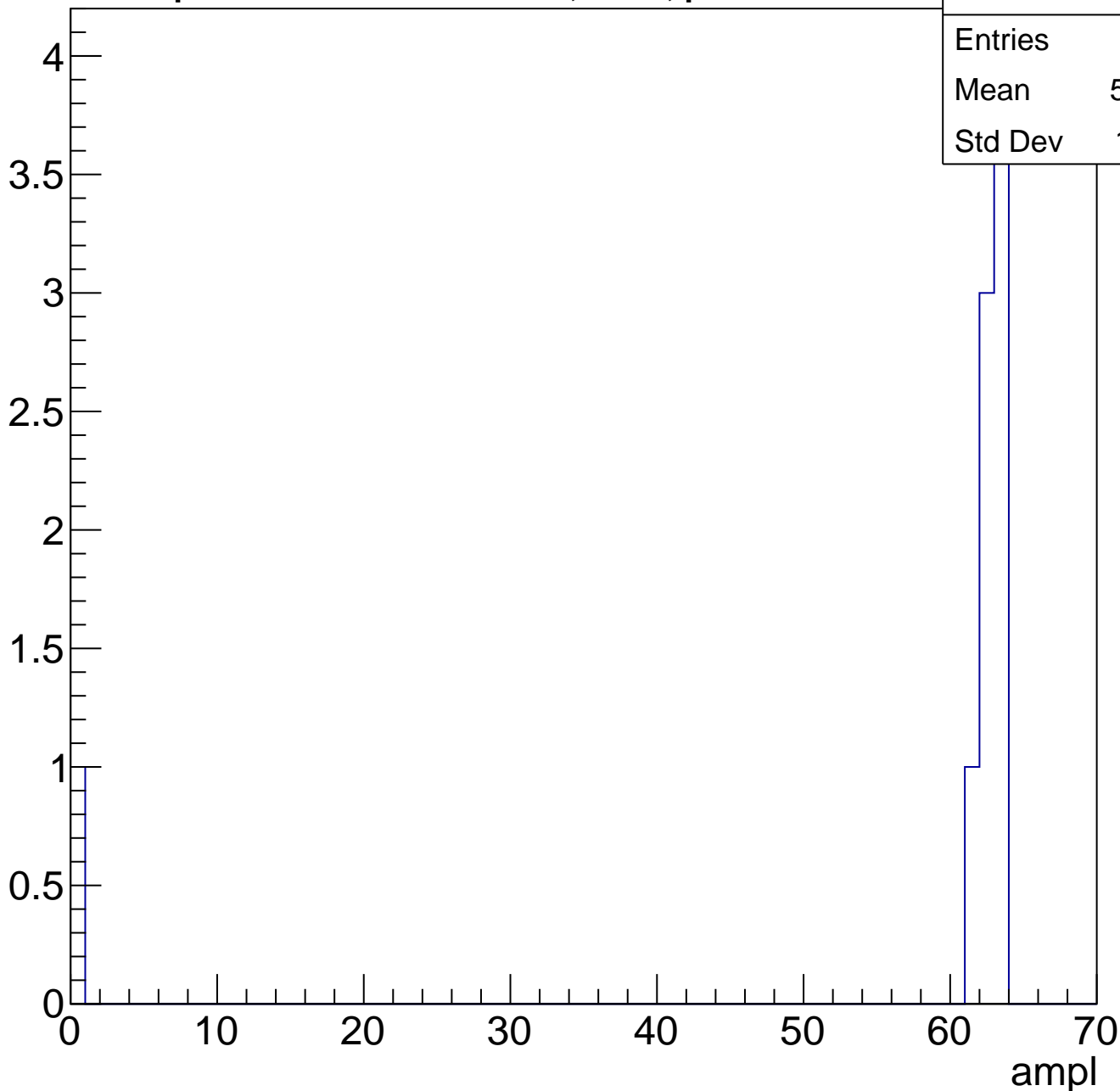
Entries	51
Mean	59.53
Std Dev	2.703



B1L103S, U12-ch8, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

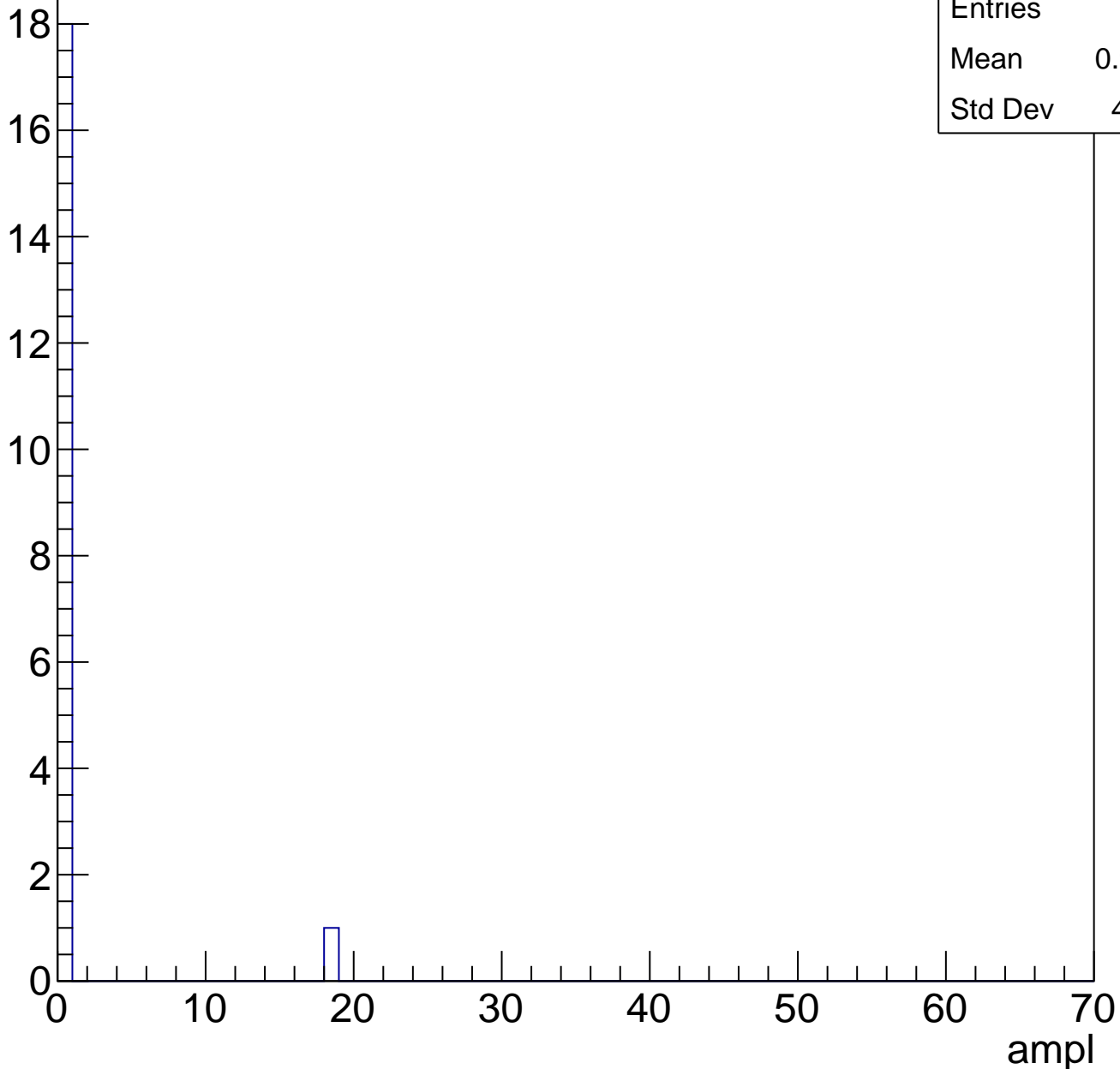


B1L103S, U12-ch8, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	0.9474
Std Dev	4.019

Entry

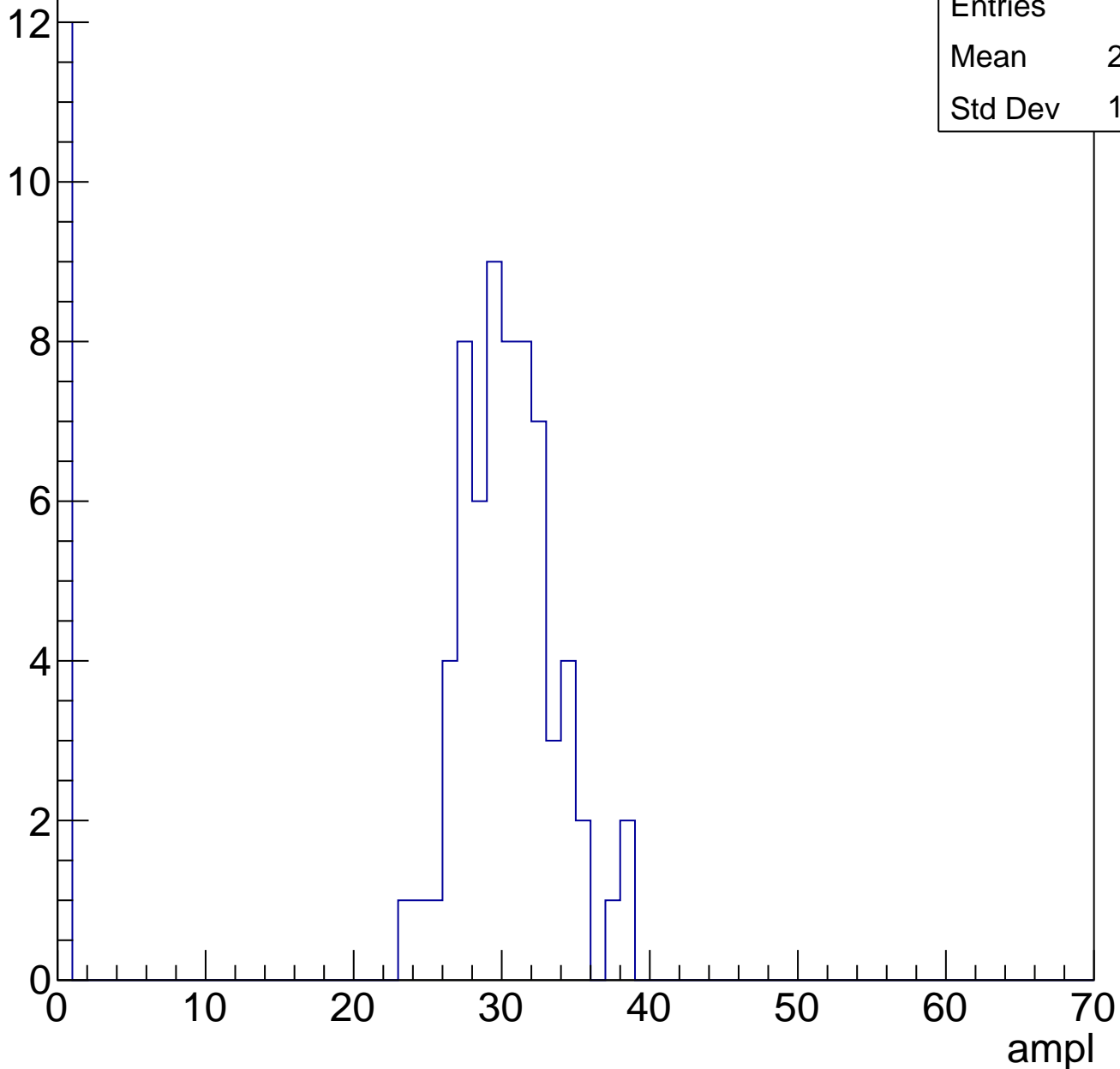


B1L103S, U12-ch9, adc0

calib_packv5_041523_1651.root, FC#0, port C2

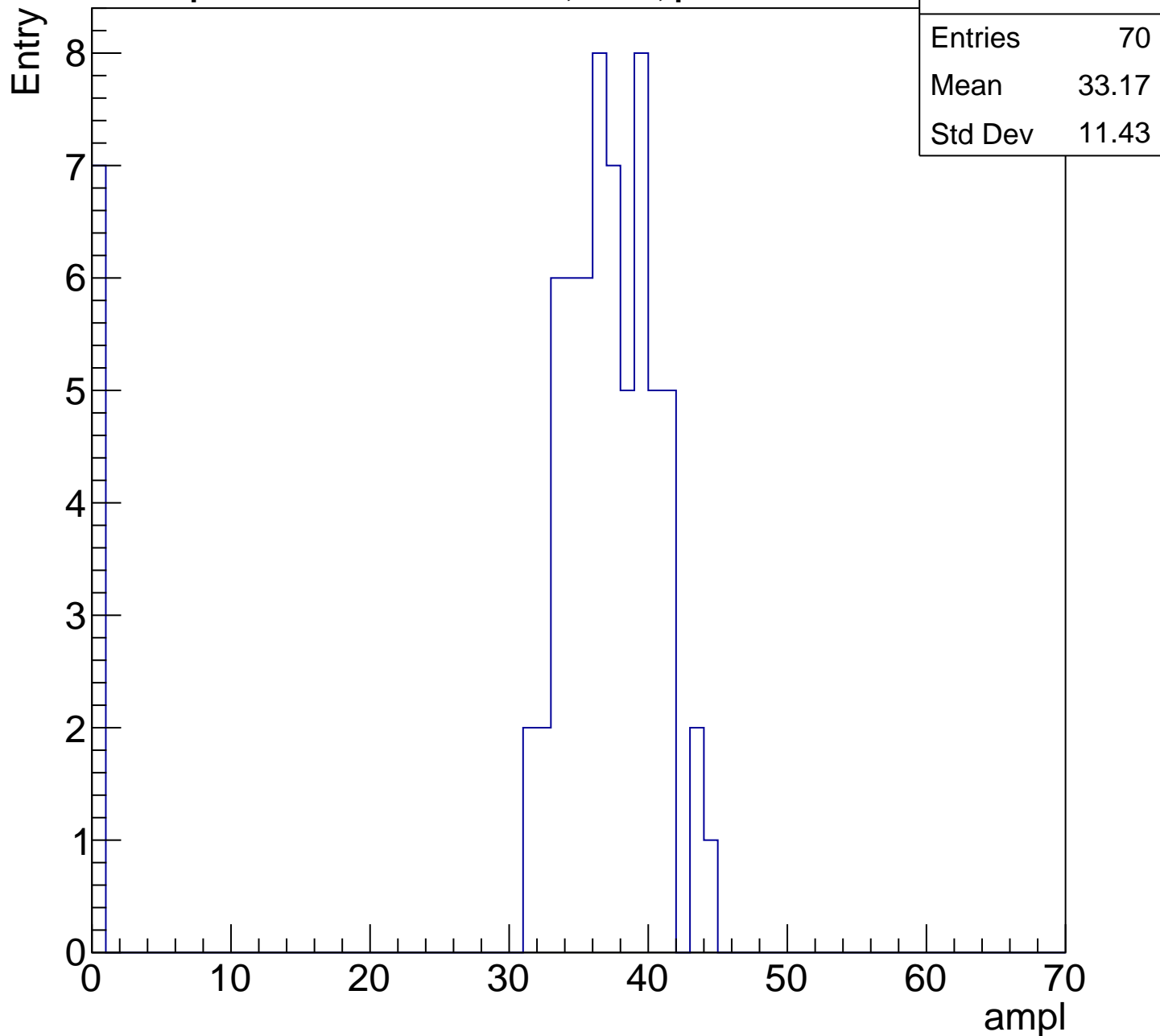
Entries	77
Mean	25.34
Std Dev	11.26

Entry



B1L103S, U12-ch9, adc1

calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U12-ch9, adc2

calib_packv5_041523_1651.root, FC#0, port C2

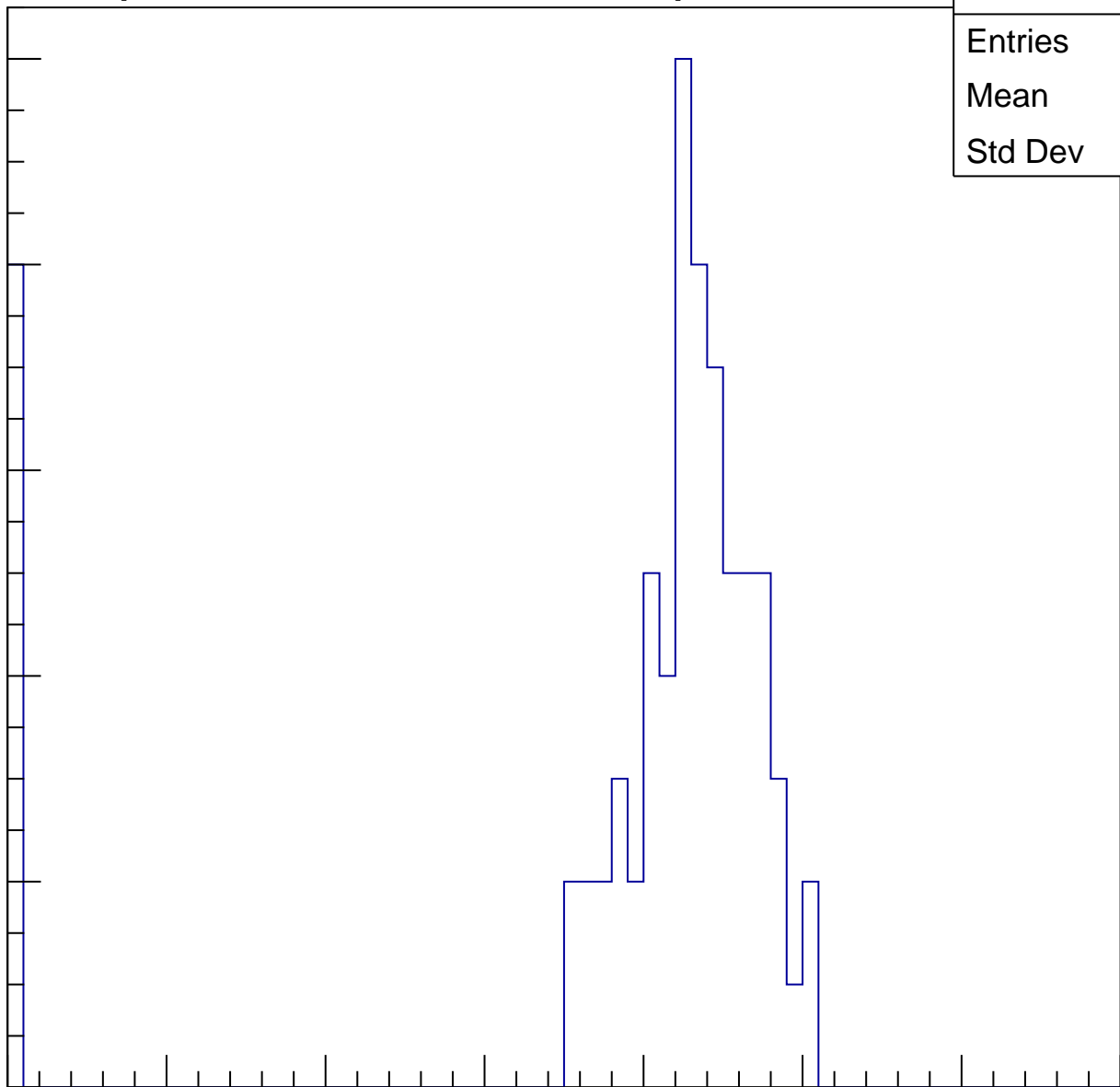
Entries	74
Mean	38.2
Std Dev	13.72

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

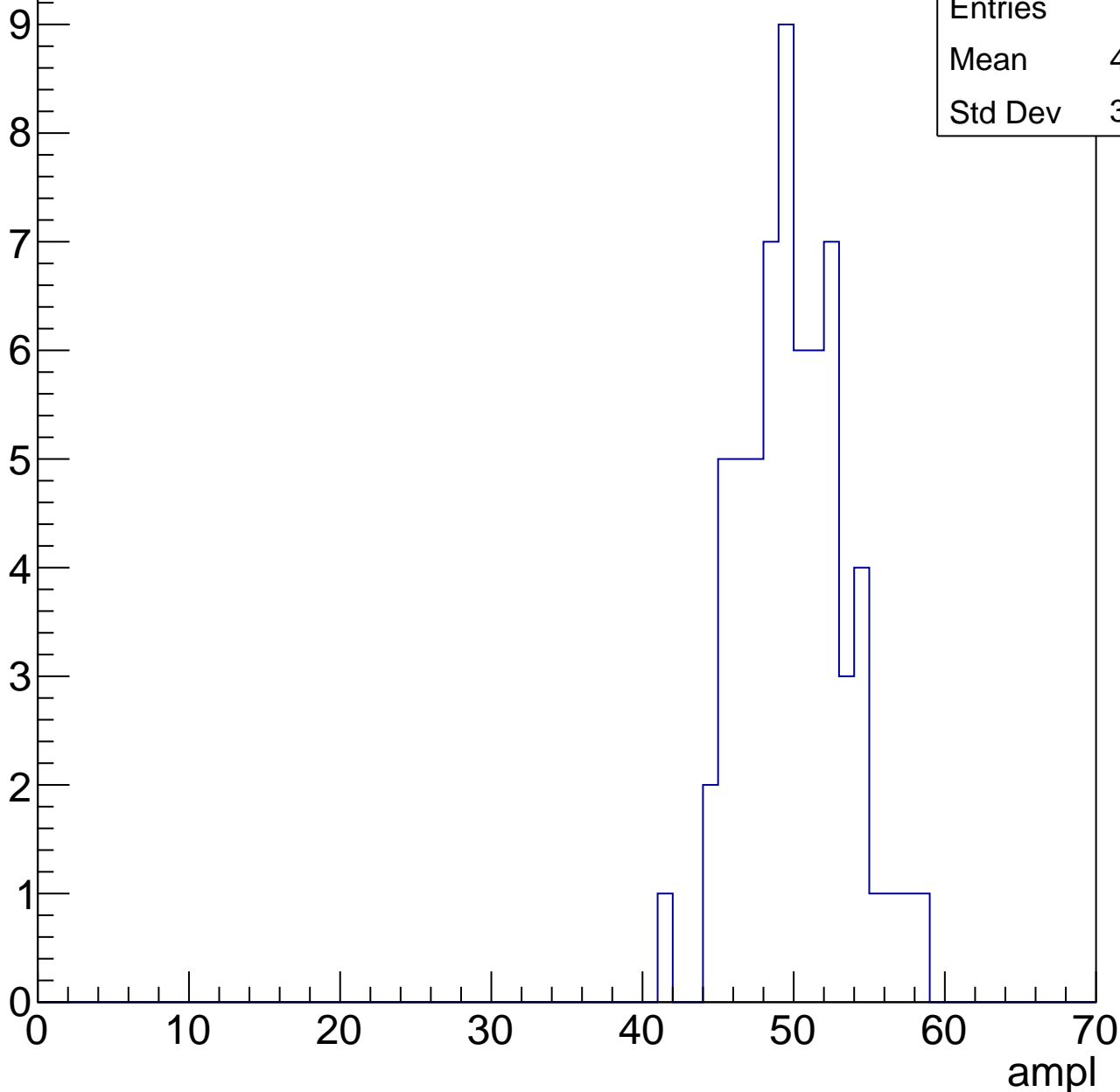


B1L103S, U12-ch9, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

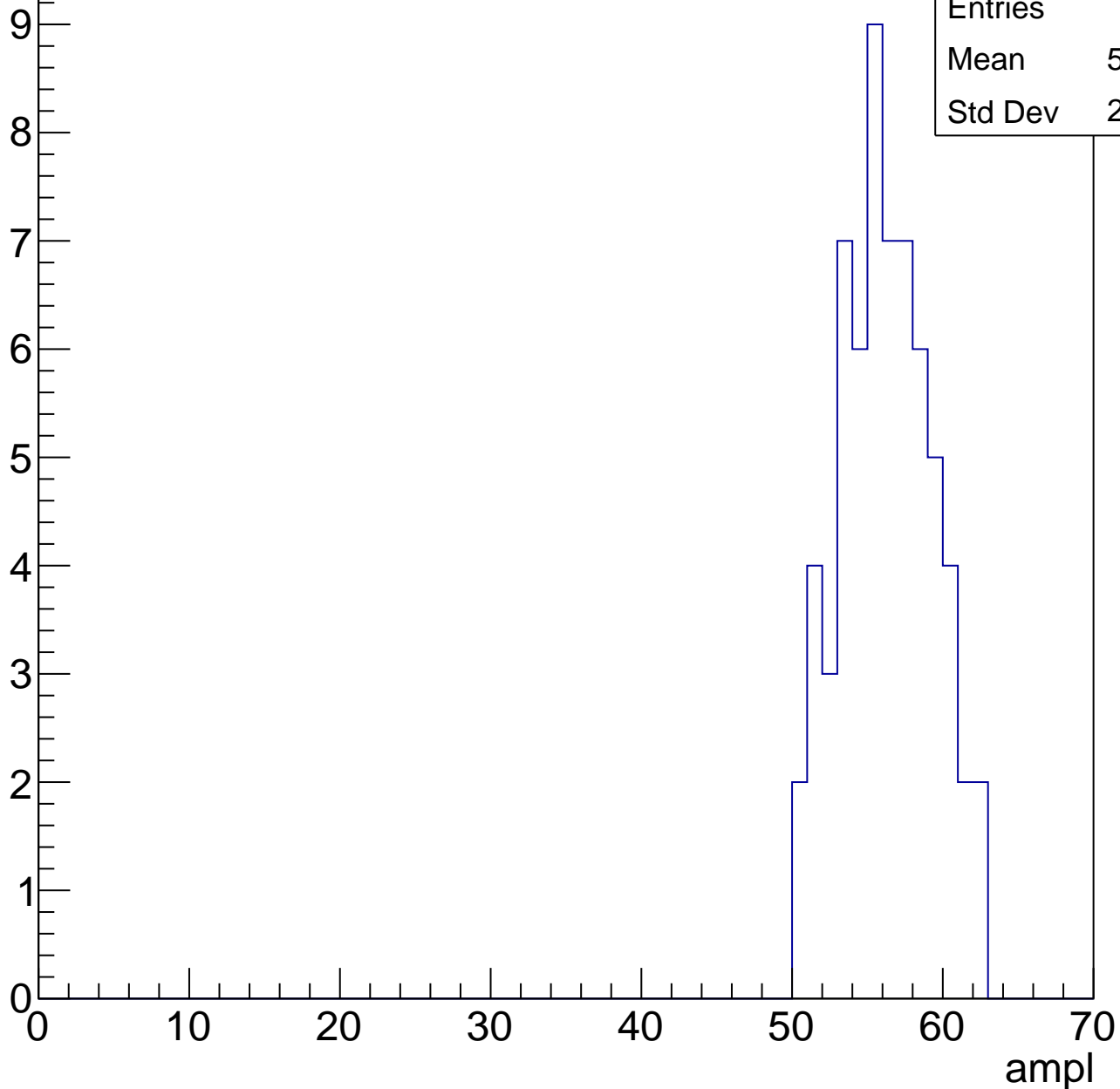
Entries	64
Mean	49.48
Std Dev	3.359



B1L103S, U12-ch9, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry



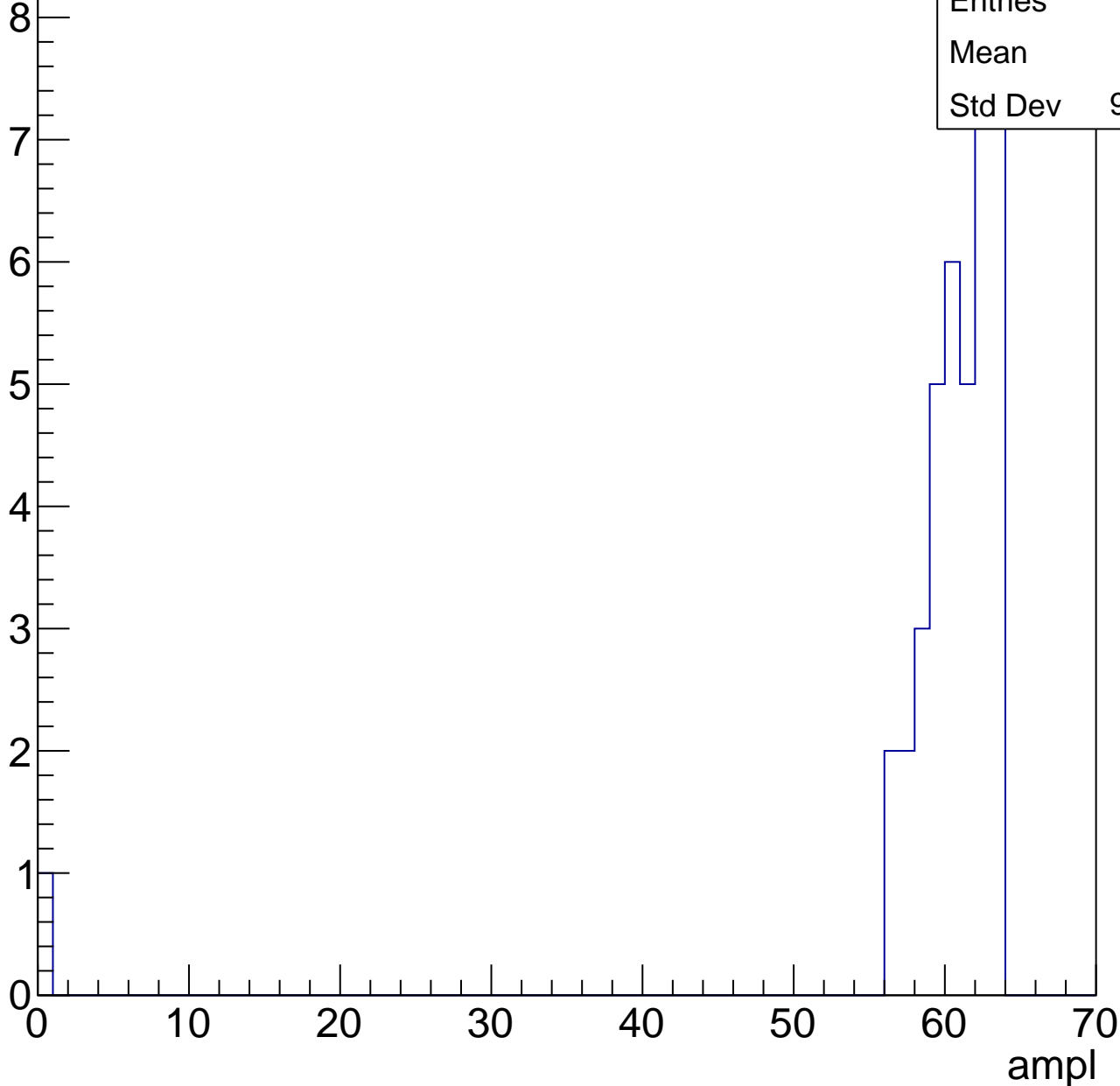
Entries	64
Mean	55.78
Std Dev	2.997

B1L103S, U12-ch9, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

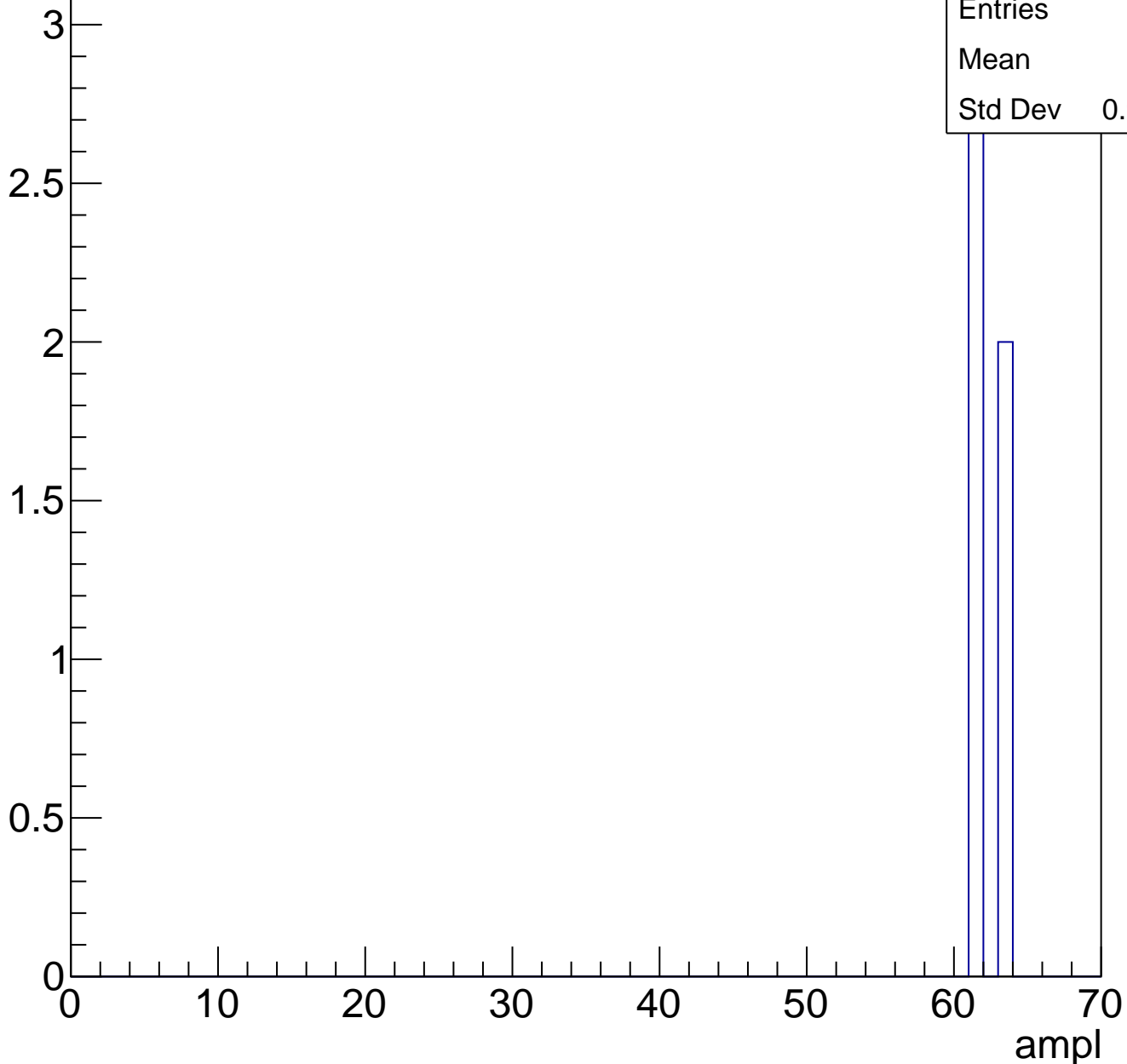
Entries	40
Mean	59
Std Dev	9.664



B1L103S, U12-ch9, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch9, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	1.211
Std Dev	5.136

ampl

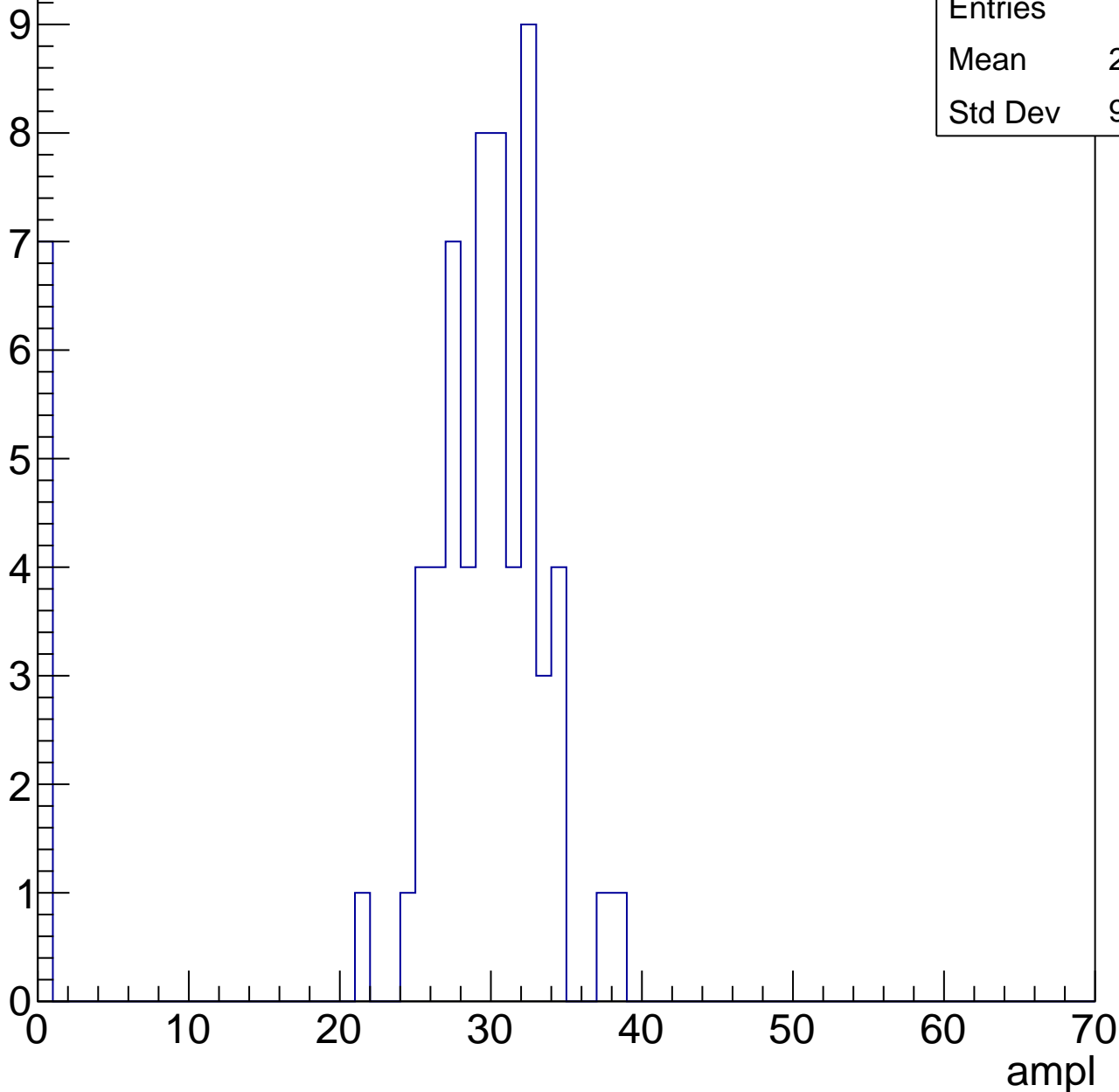
0 10 20 30 40 50 60 70

B1L103S, U12-ch10, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	26.42
Std Dev	9.589

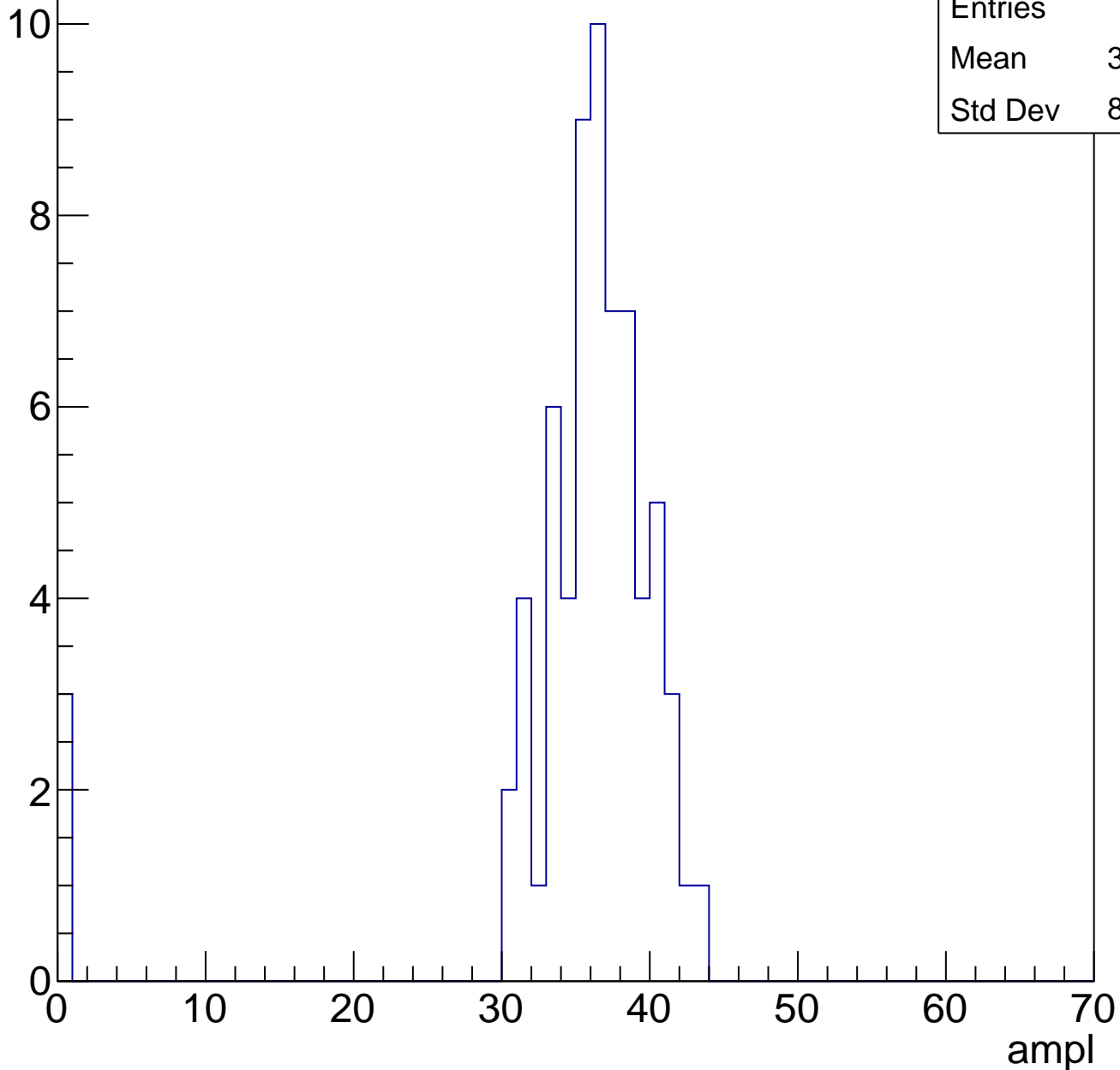


B1L103S, U12-ch10, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	67
Mean	34.54
Std Dev	8.032

Entry

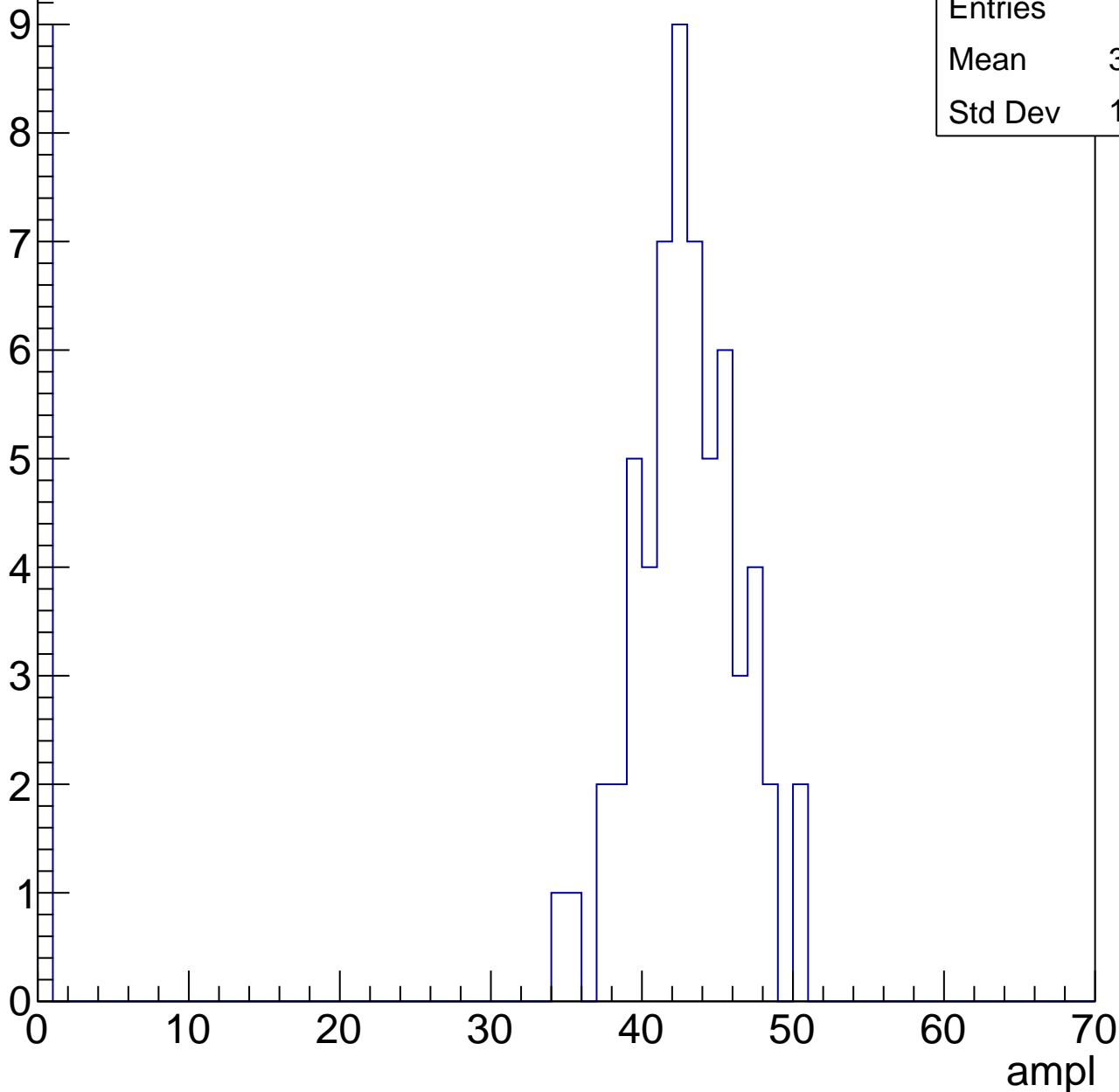


B1L103S, U12-ch10, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	36.99
Std Dev	14.66

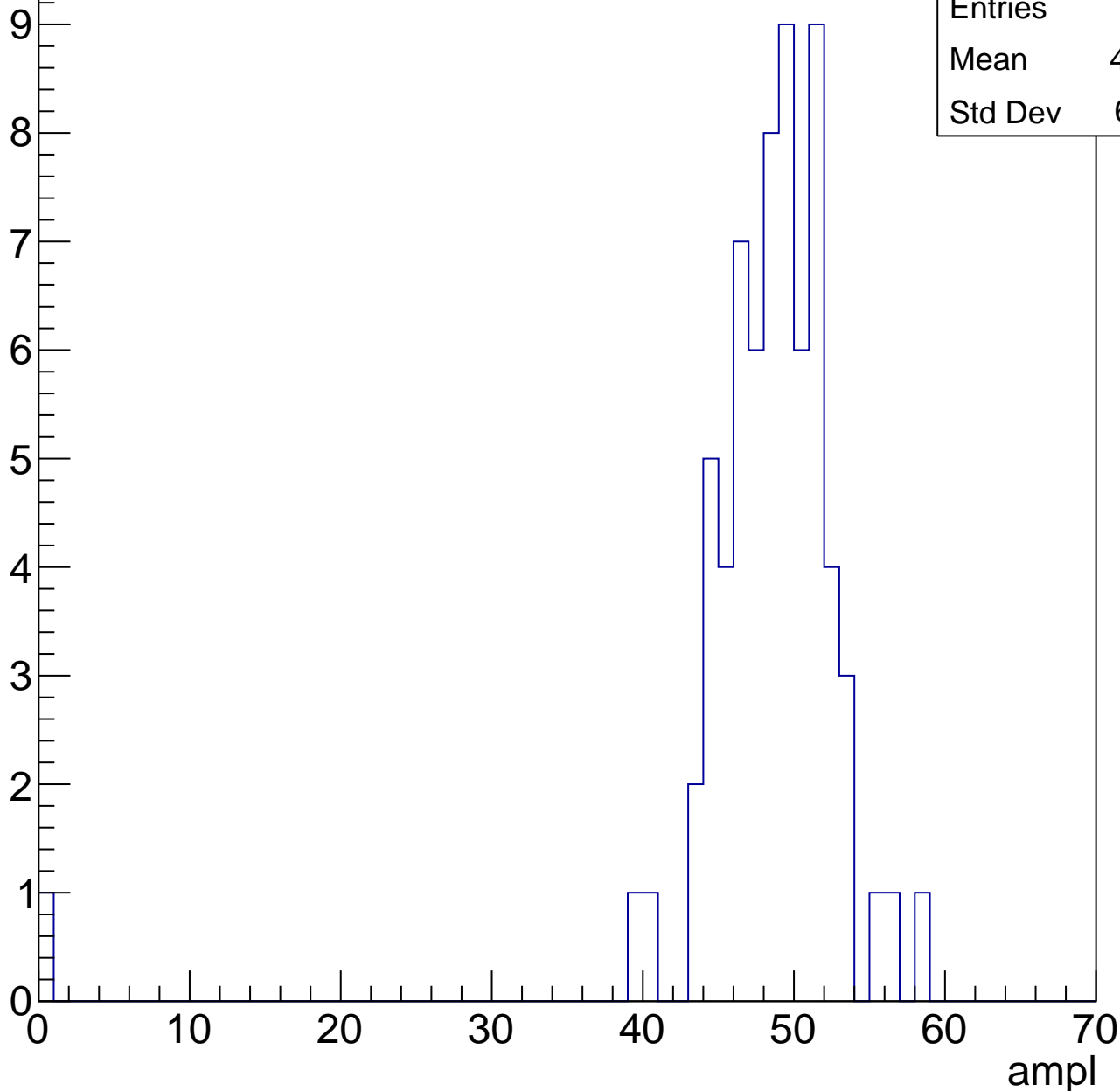


B1L103S, U12-ch10, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	47.67
Std Dev	6.711

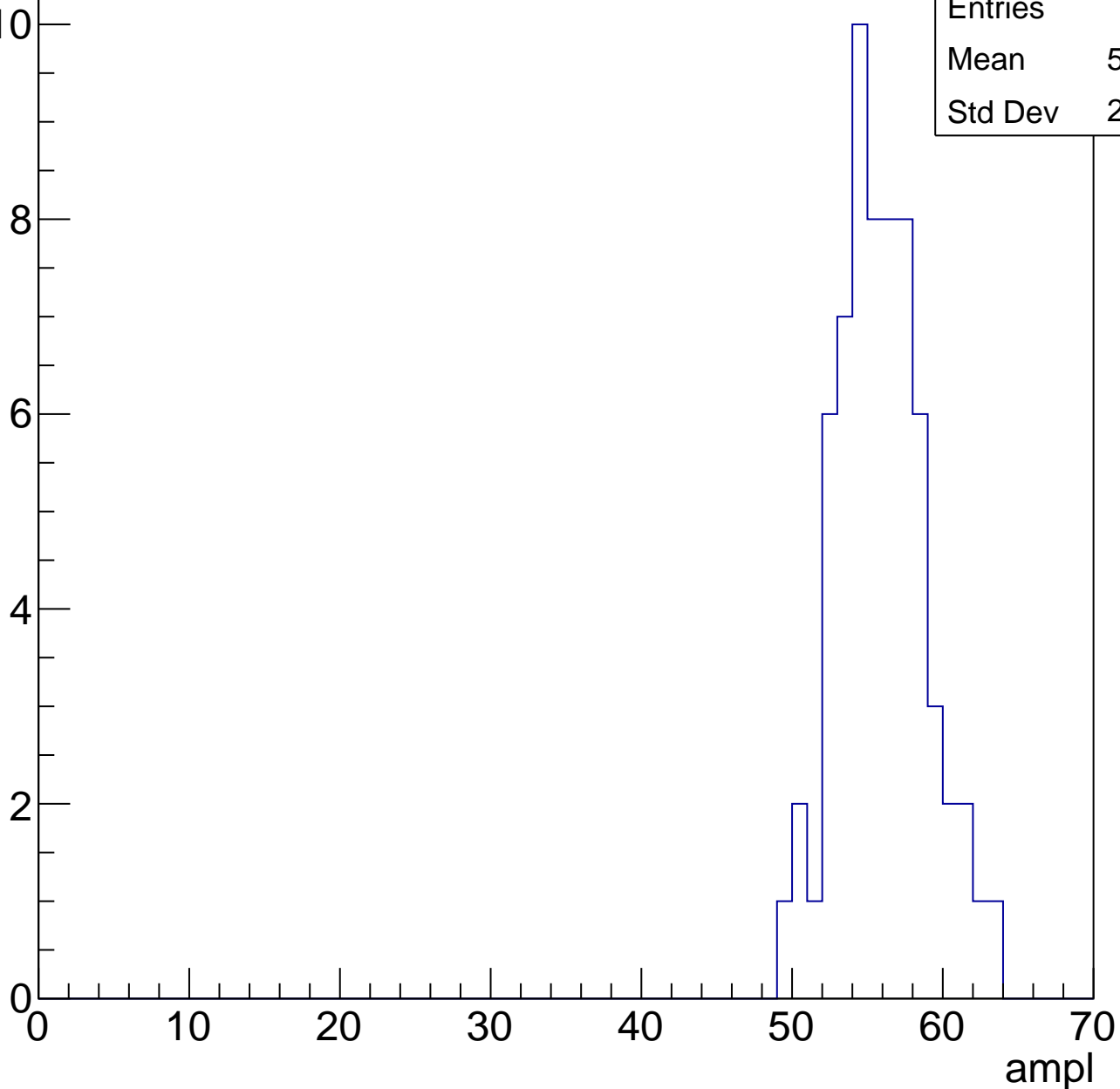


B1L103S, U12-ch10, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	55.44
Std Dev	2.908

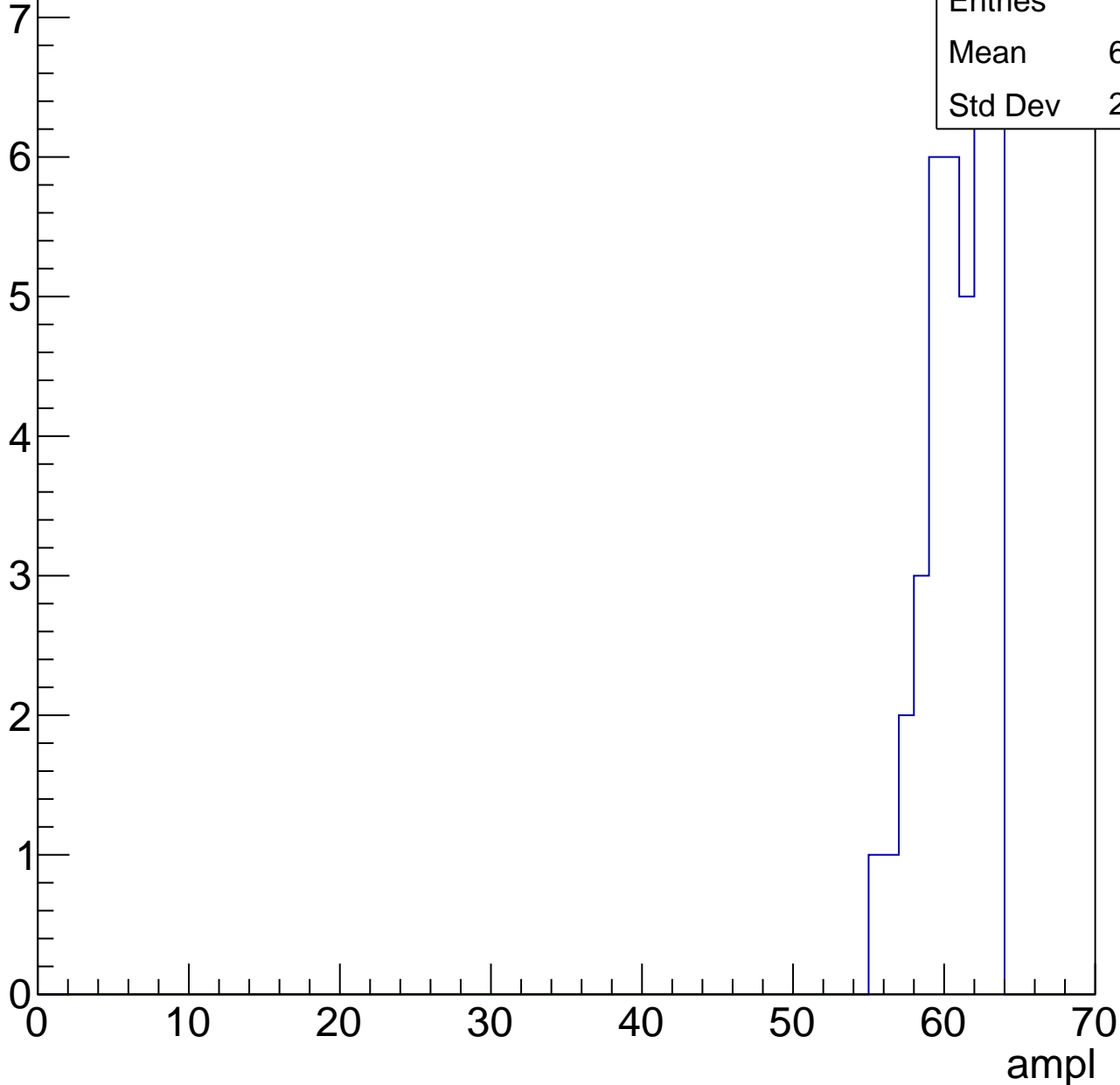


B1L103S, U12-ch10, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	38
Mean	60.34
Std Dev	2.106



B1L103S, U12-ch10, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

3

2.5

2

1.5

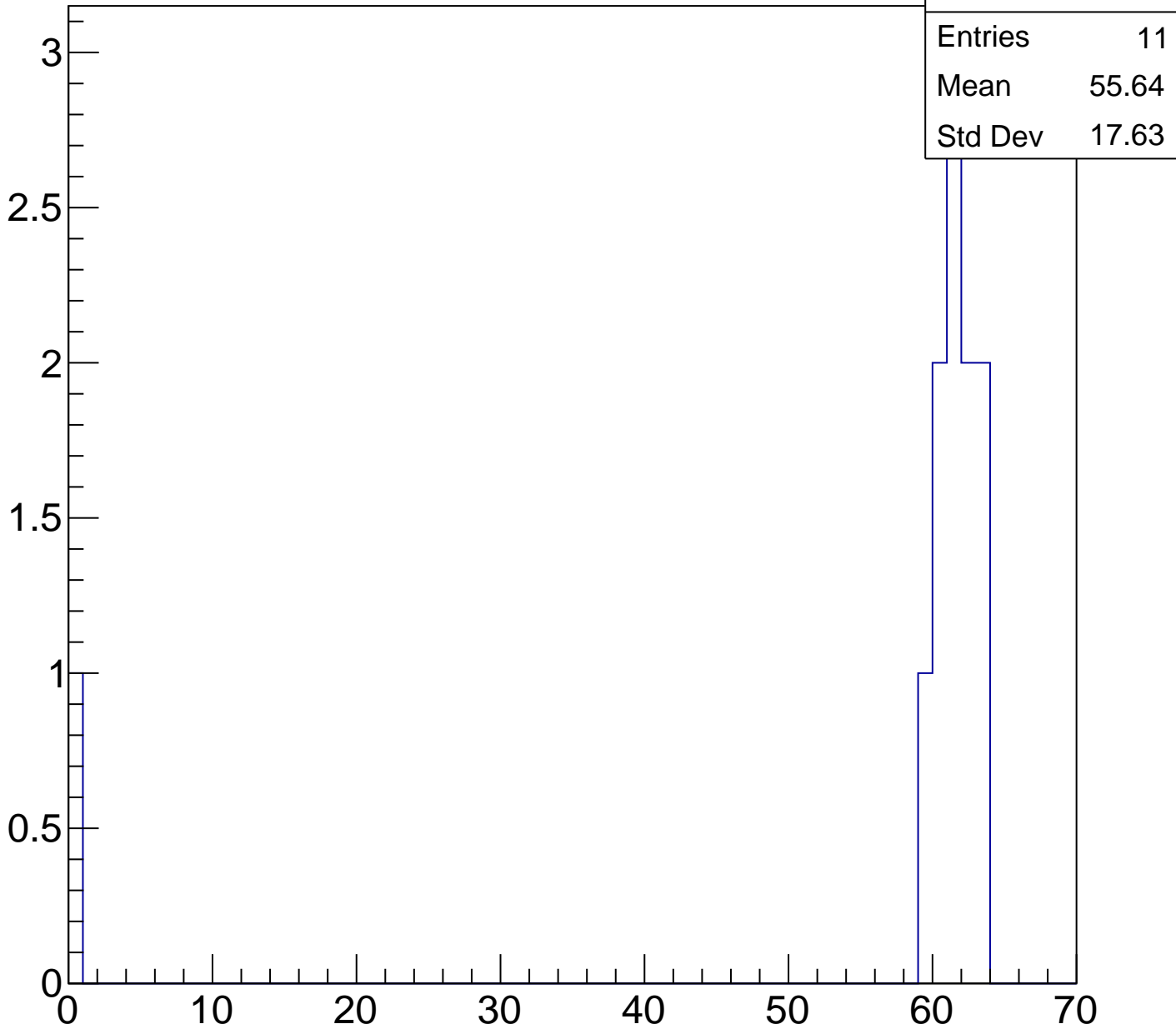
1

0.5

0

ampl

Entries	11
Mean	55.64
Std Dev	17.63



B1L103S, U12-ch10, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch11, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	79
Mean	25.94
Std Dev	10.96

Entry

10

8

6

4

2

0

0

10

20

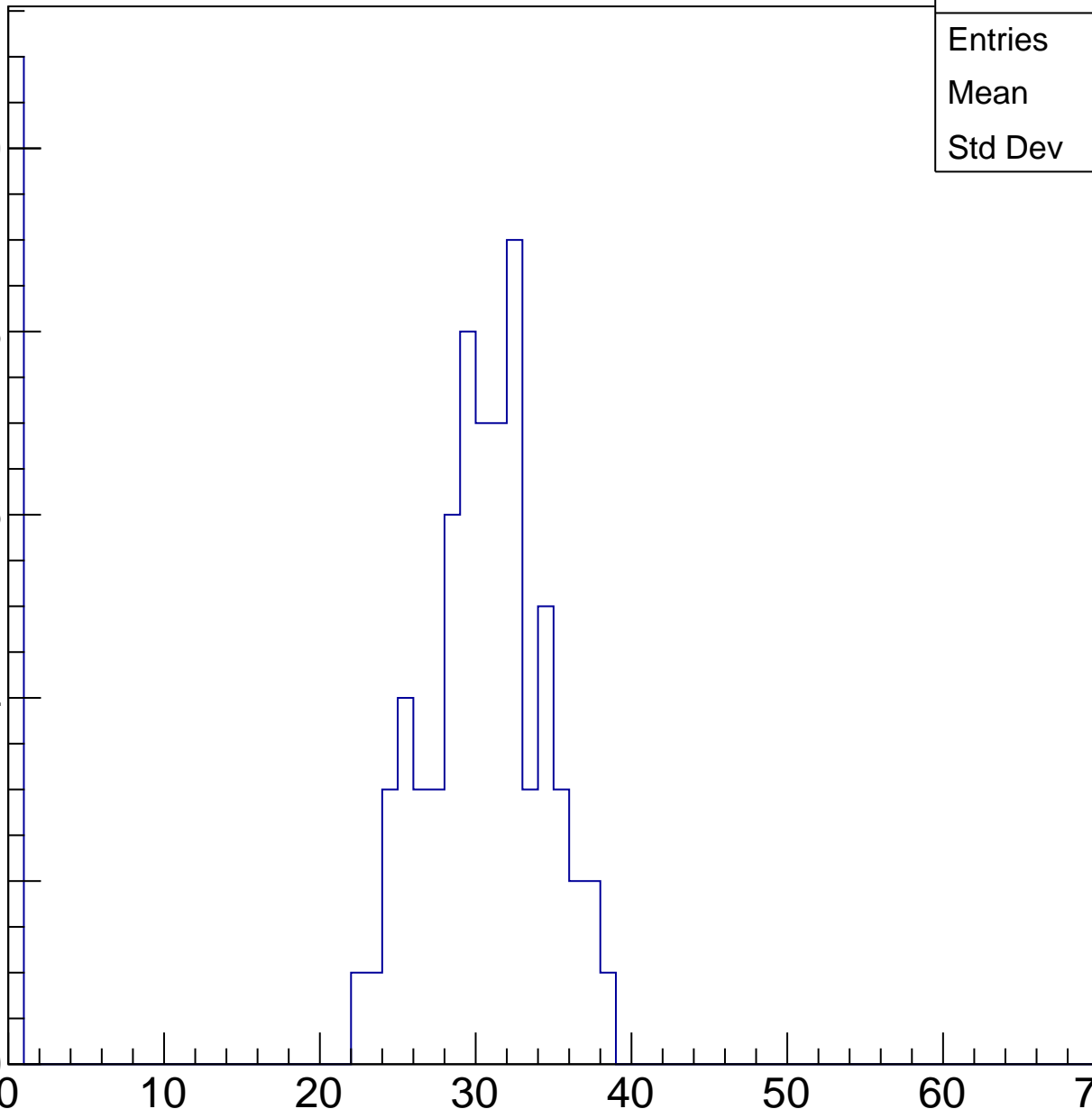
30

40

50

60

ampl

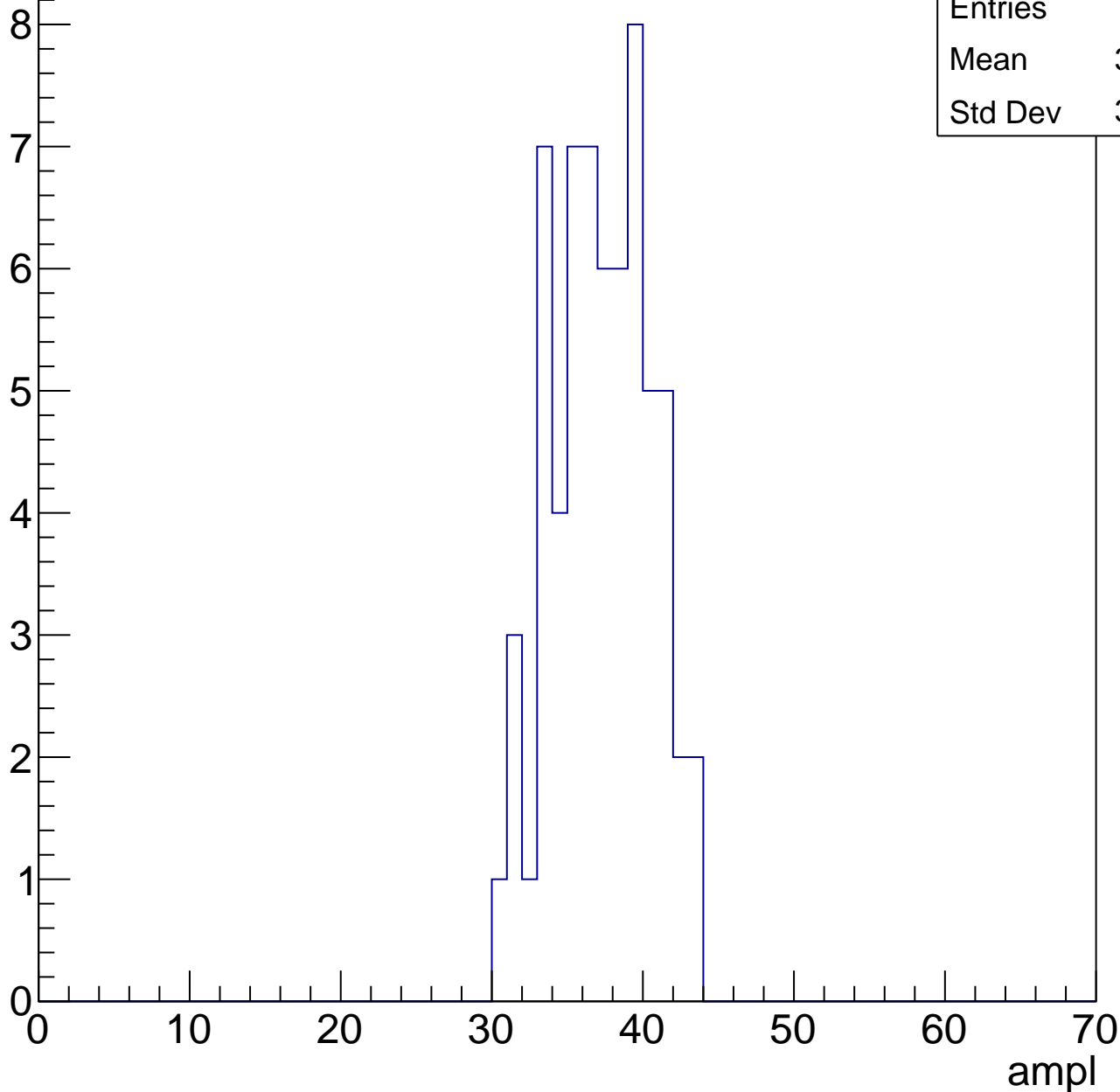


B1L103S, U12-ch11, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	36.81
Std Dev	3.181



B1L103S, U12-ch11, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

10

8

6

4

2

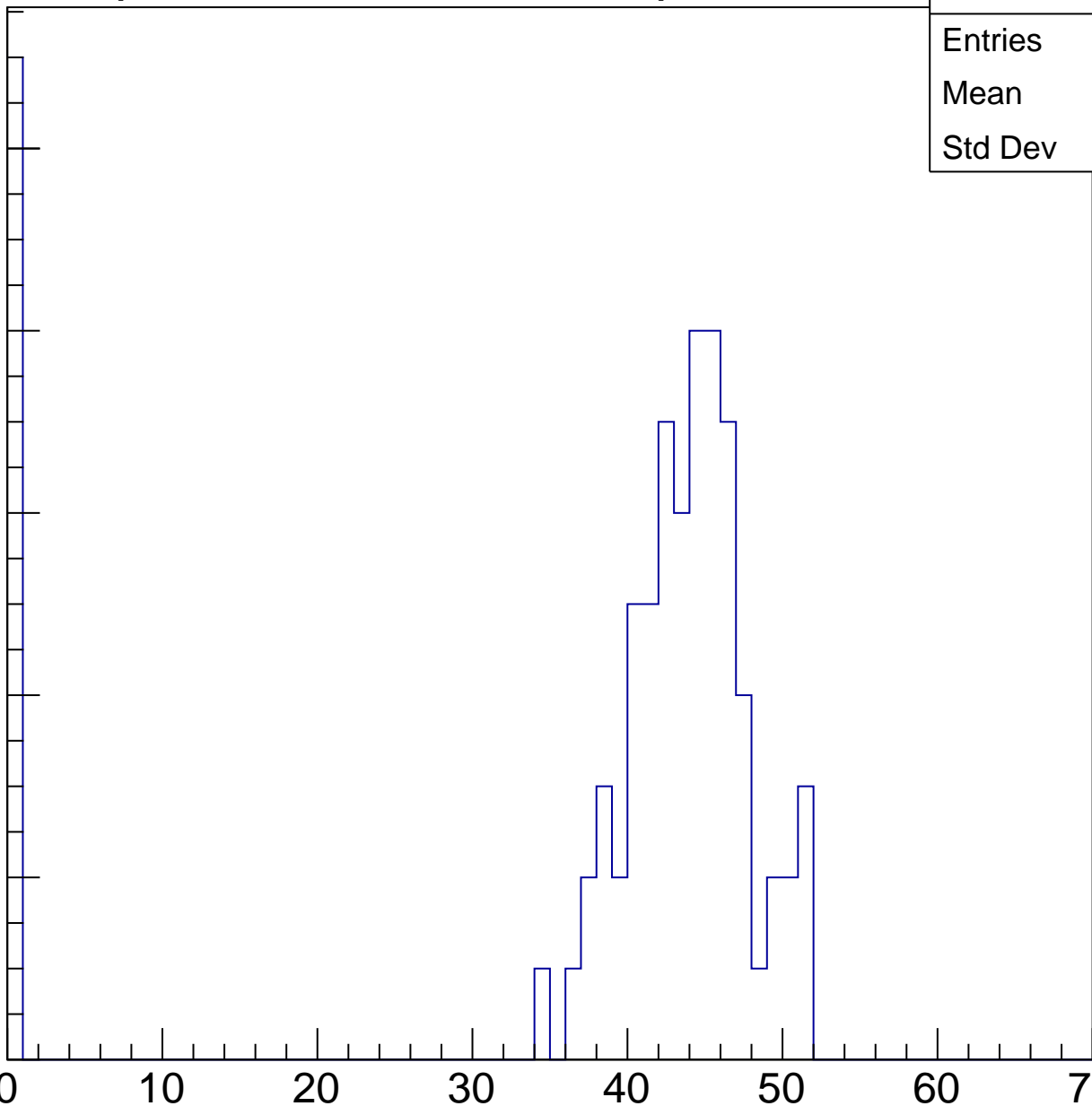
0

Entries 78

Mean 37.36

Std Dev 15.52

ampl

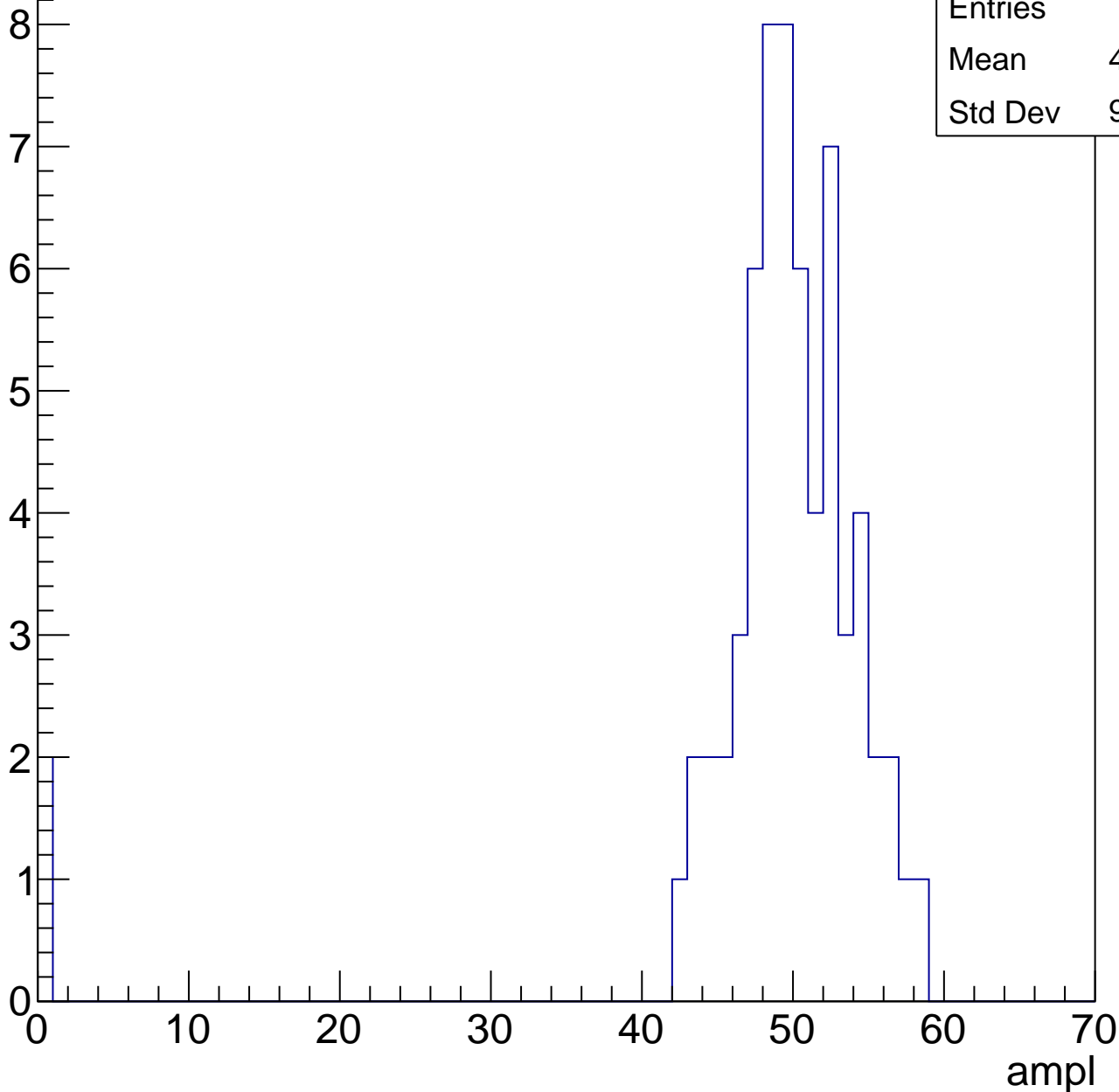


B1L103S, U12-ch11, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

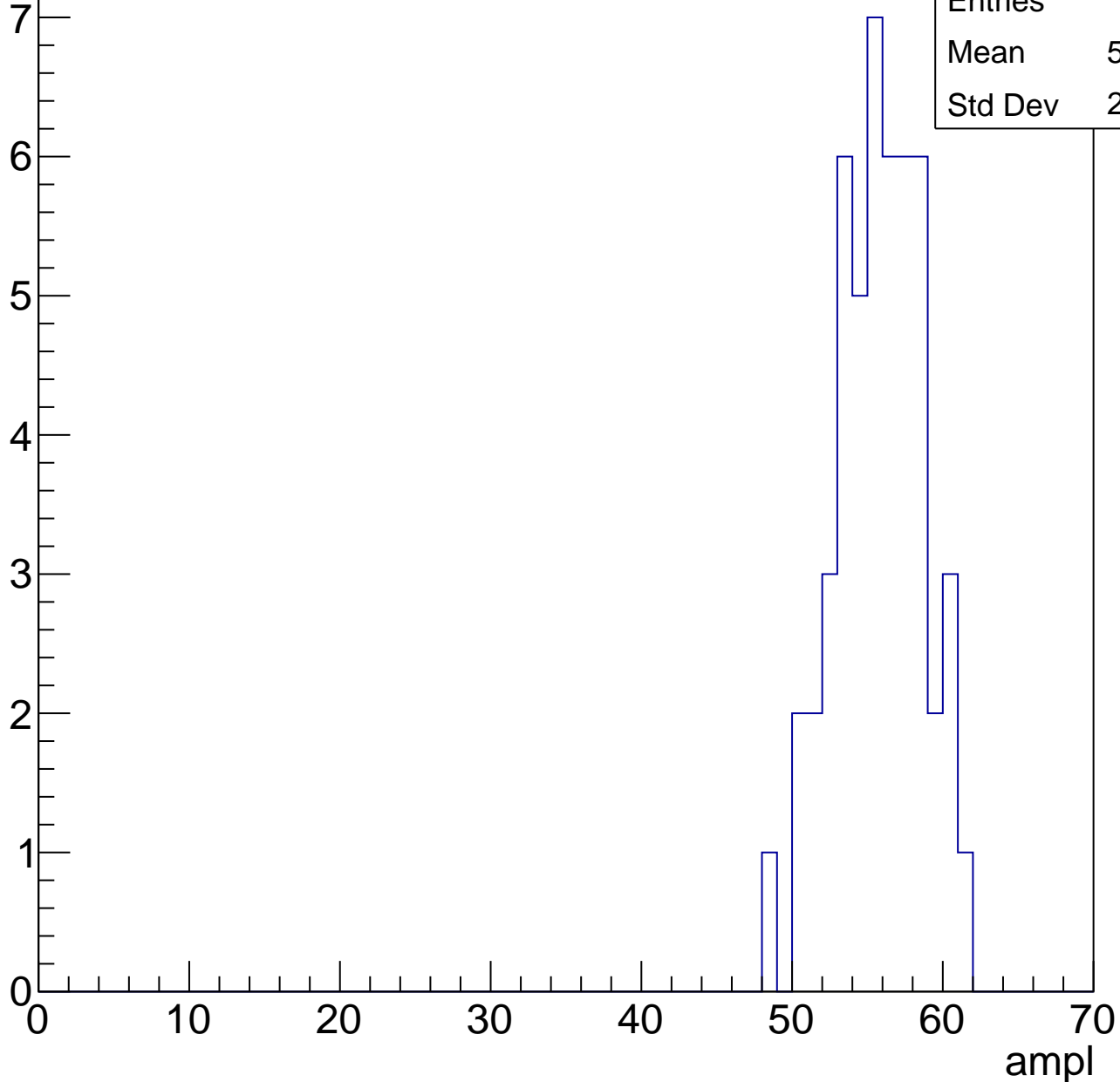
Entries	64
Mean	48.16
Std Dev	9.326



B1L103S, U12-ch11, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

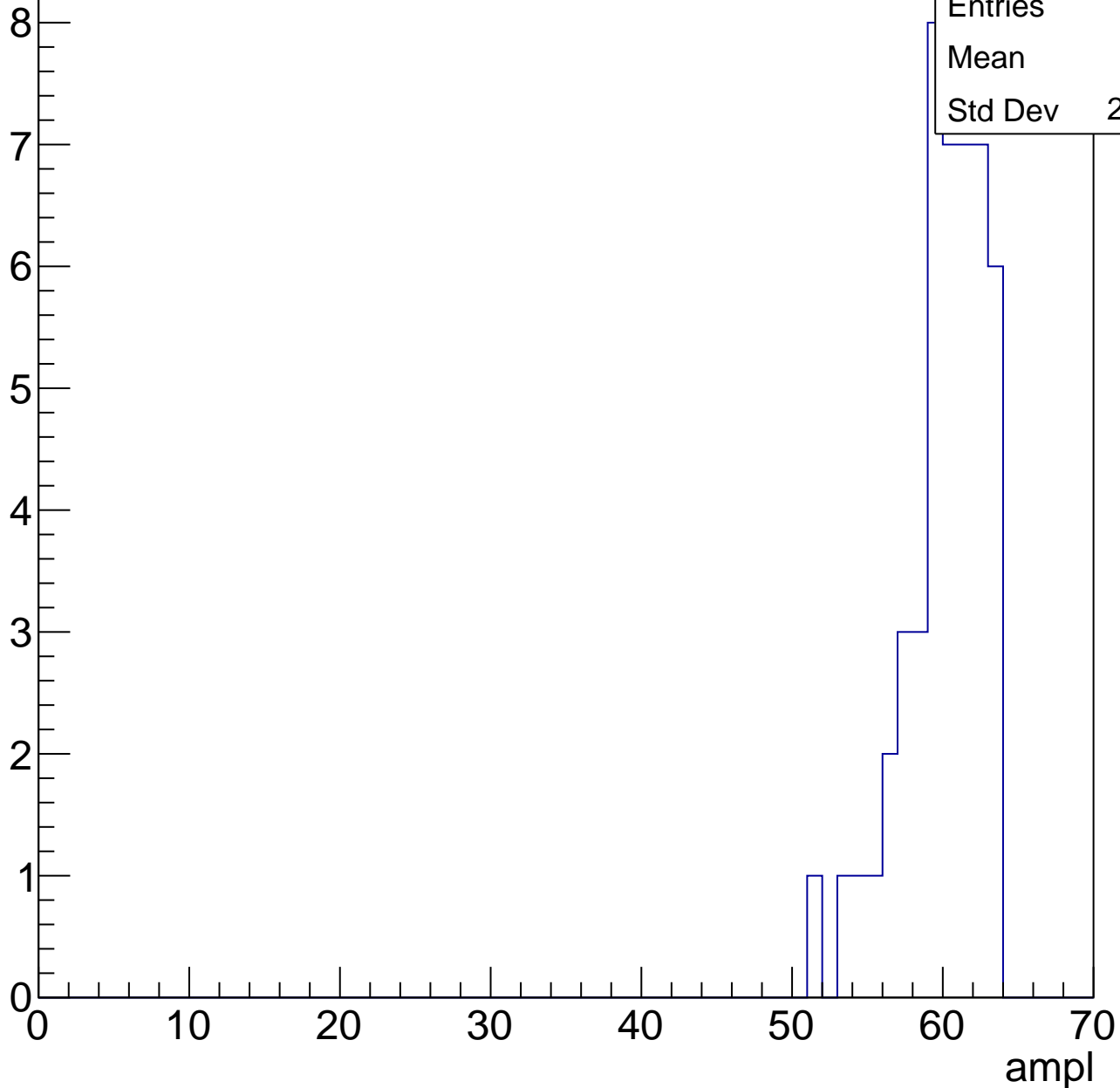


Entries	50
Mean	55.28
Std Dev	2.864

B1L103S, U12-ch11, adc5

calib_packv5_041523_1651.root, FC#0, port C2

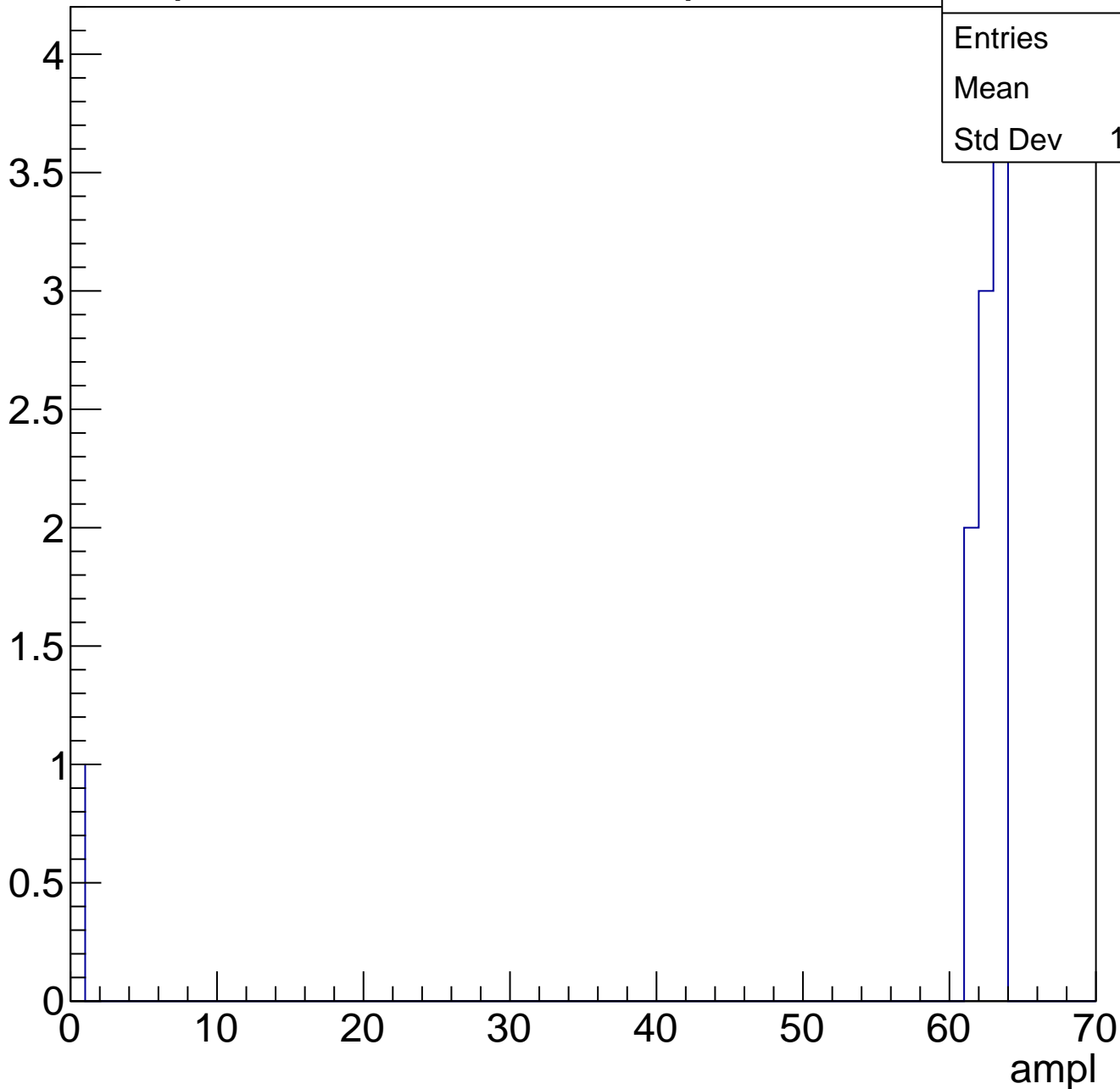
Entry



B1L103S, U12-ch11, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch11, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.158
Std Dev	4.913

Entry

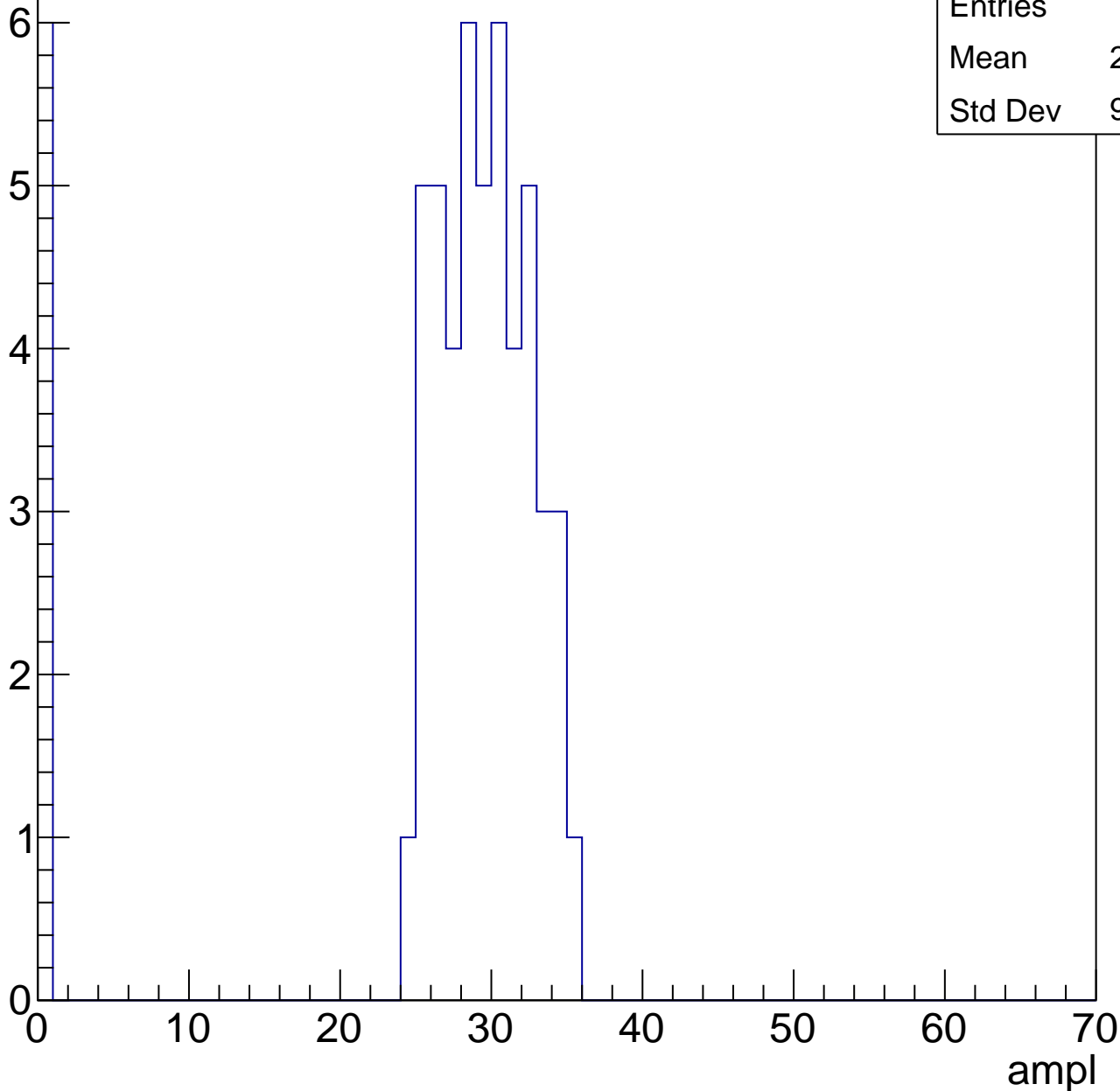


B1L103S, U12-ch12, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	54
Mean	25.93
Std Dev	9.558

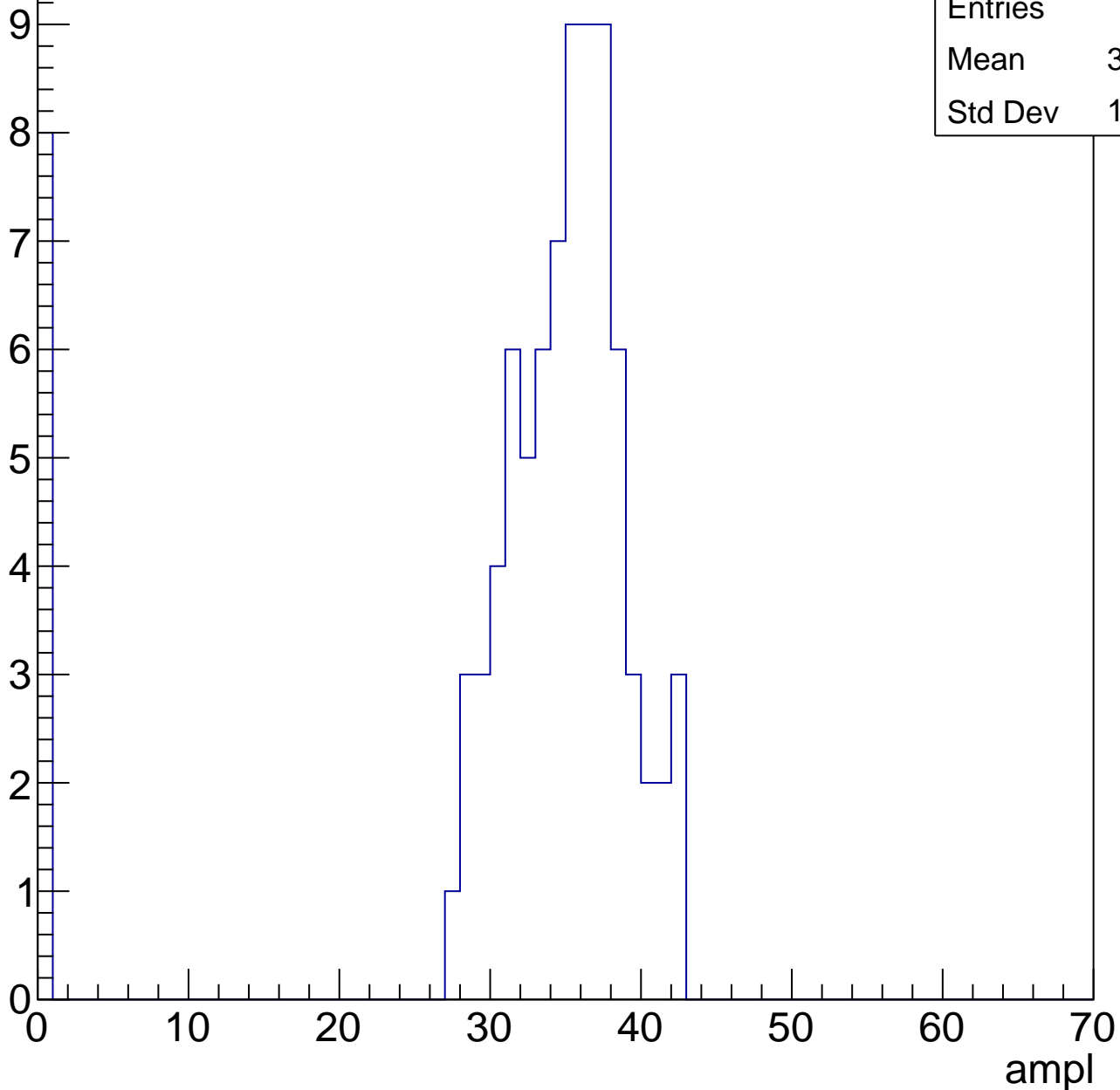


B1L103S, U12-ch12, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	86
Mean	31.45
Std Dev	10.63

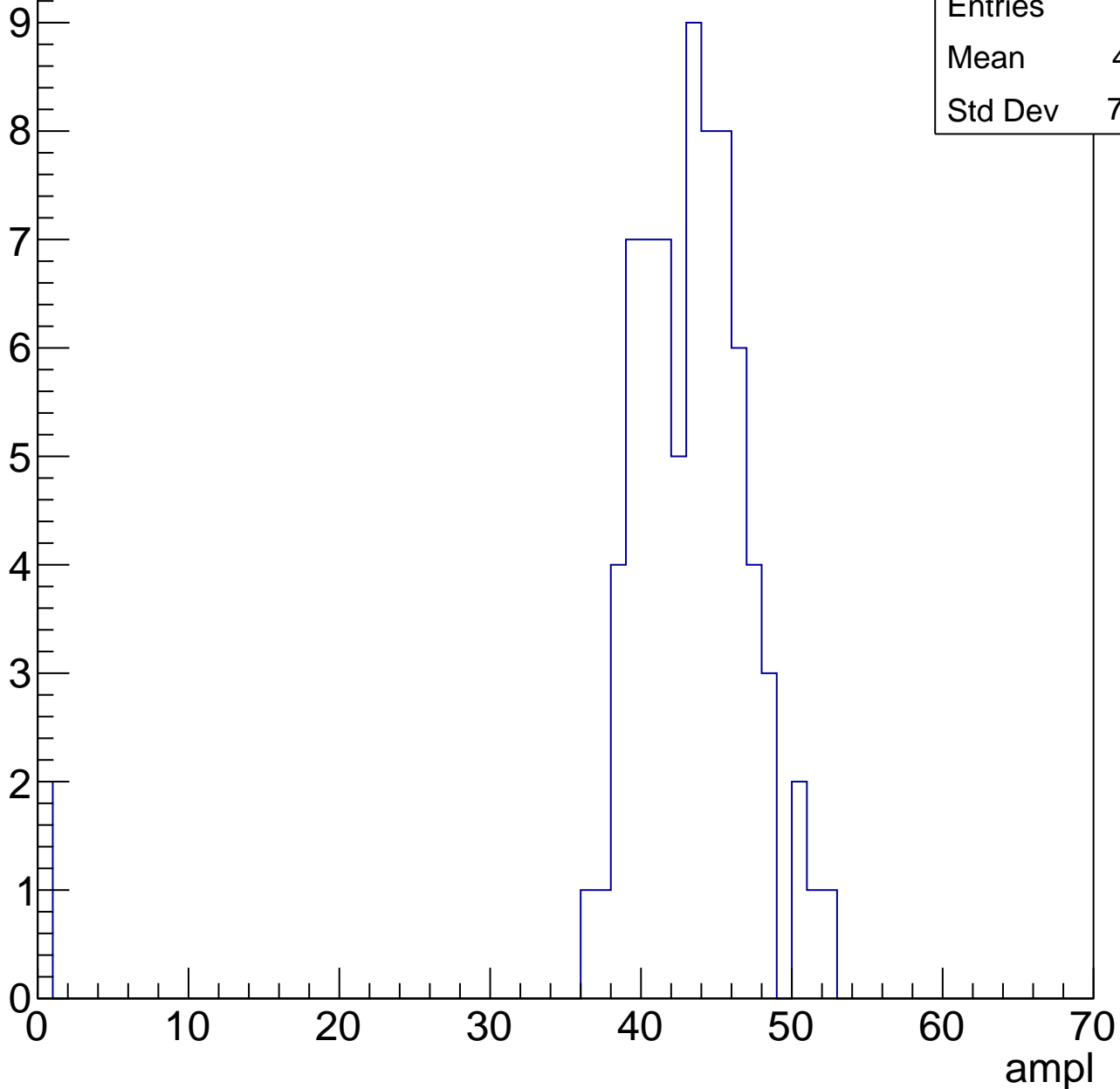


B1L103S, U12-ch12, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	76
Mean	41.91
Std Dev	7.675

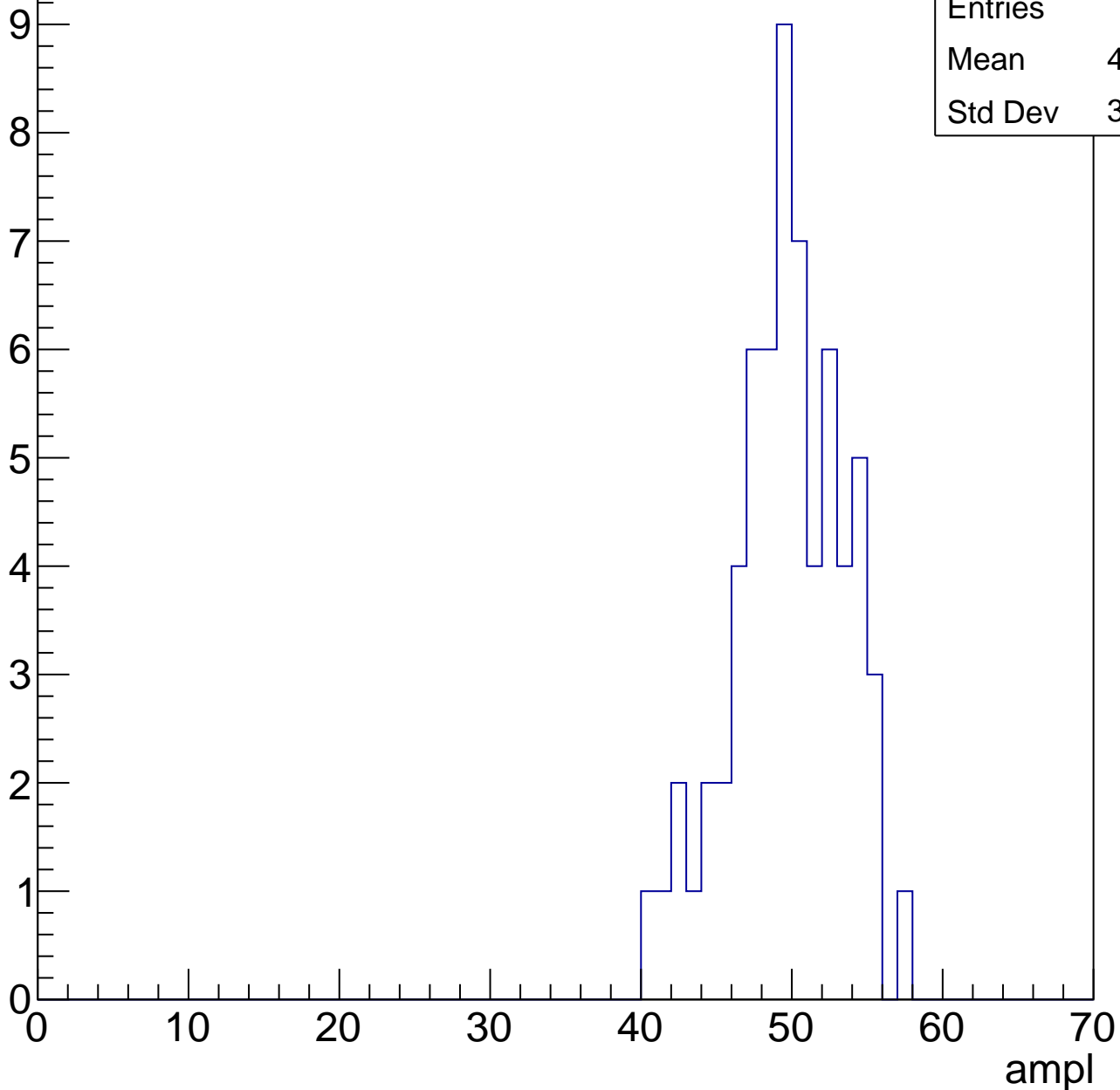


B1L103S, U12-ch12, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	49.23
Std Dev	3.669

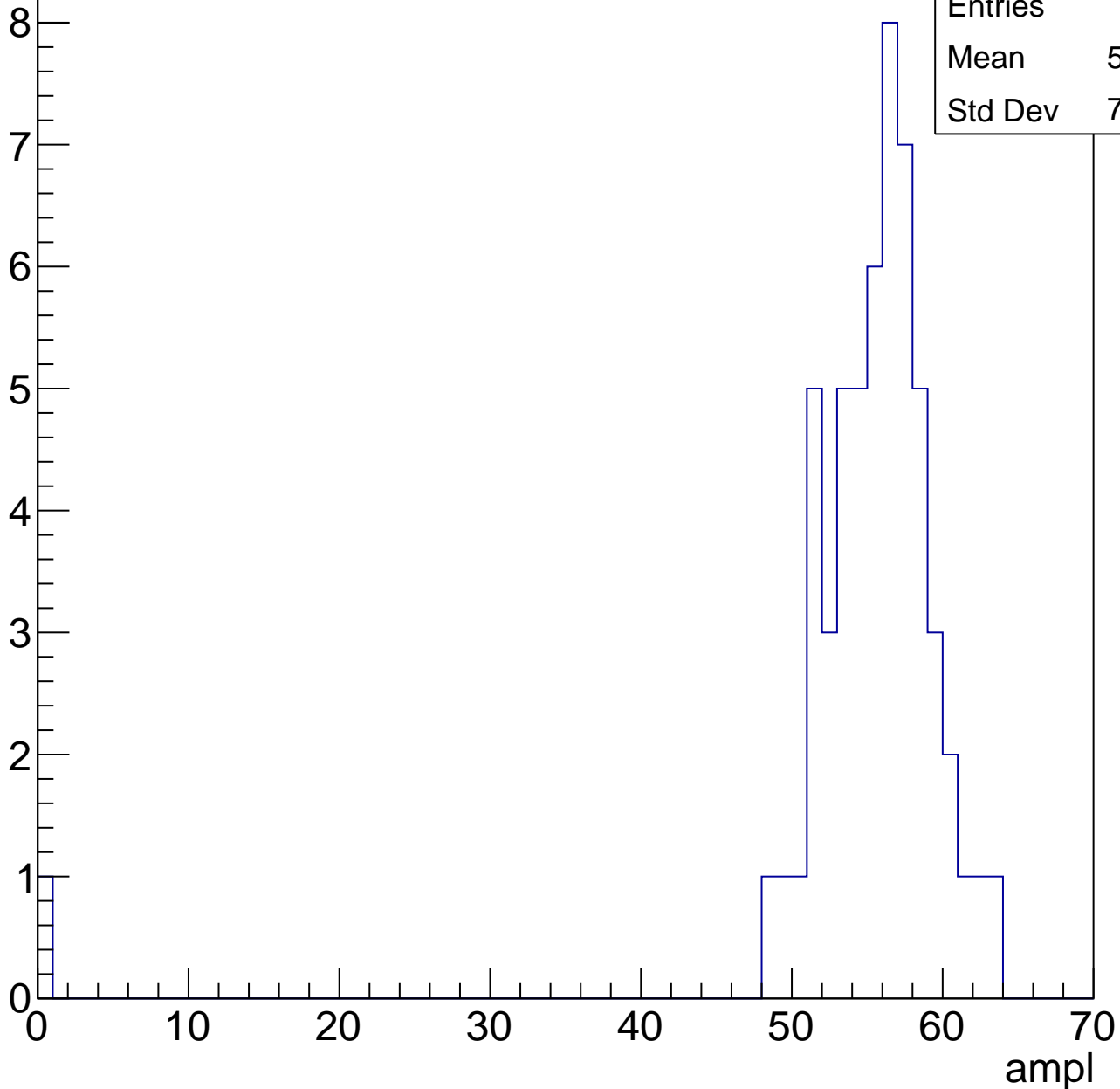


B1L103S, U12-ch12, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	56
Mean	54.34
Std Dev	7.985

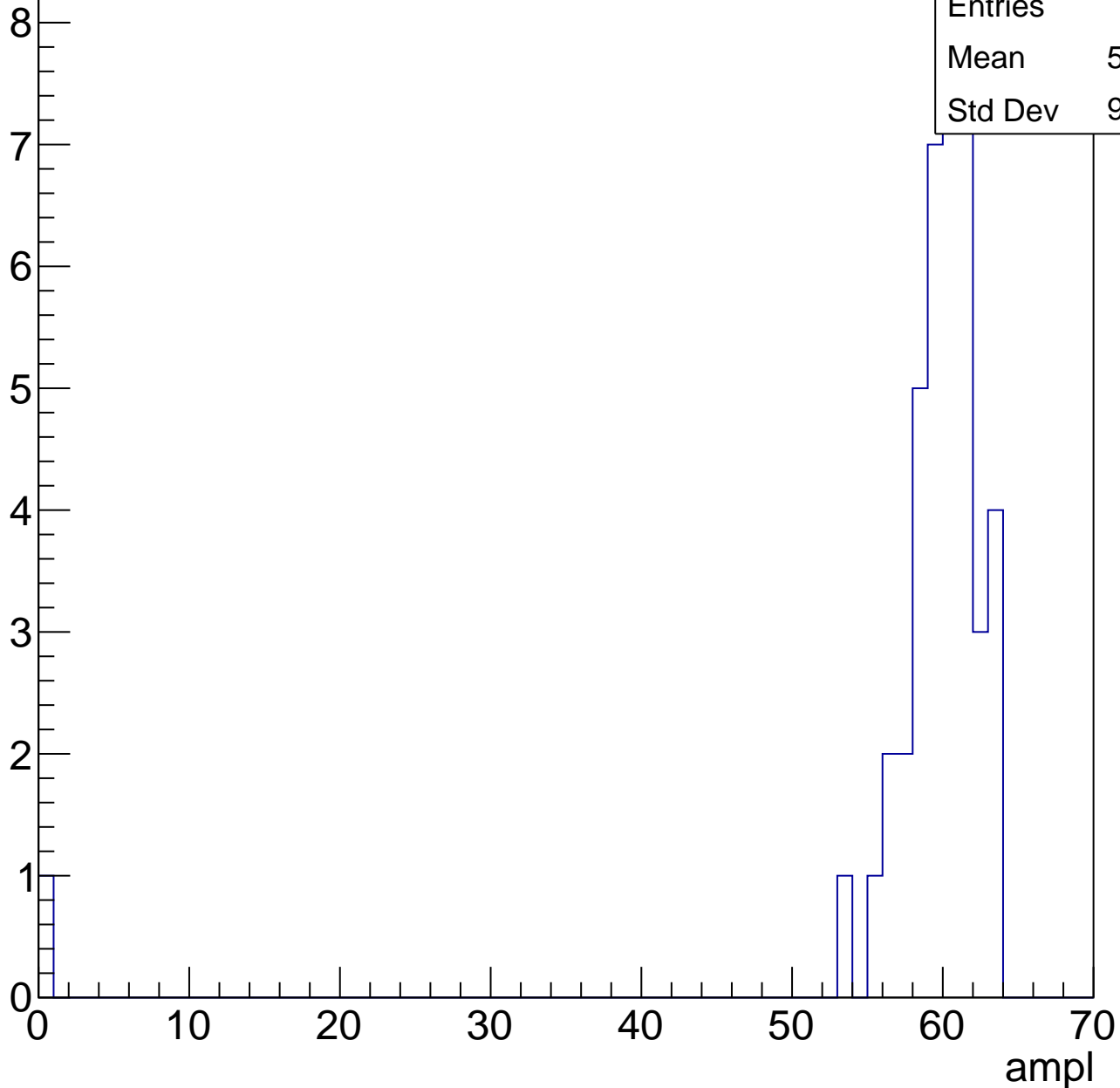


B1L103S, U12-ch12, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	42
Mean	58.17
Std Dev	9.342

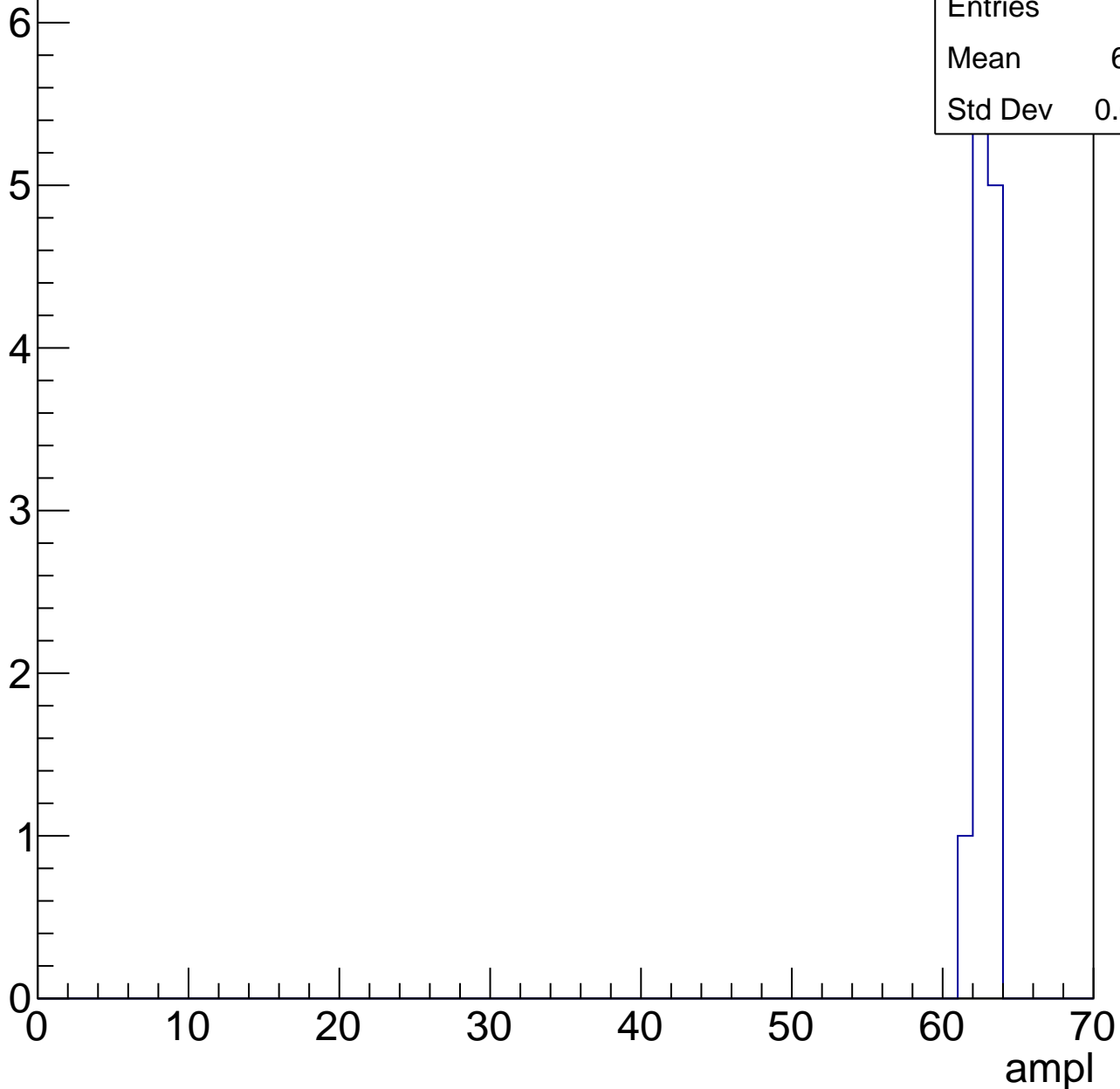


B1L103S, U12-ch12, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	12
Mean	62.33
Std Dev	0.6236



B1L103S, U12-ch12, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch13, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	95
Mean	26.76
Std Dev	10.28

Entry

10

8

6

4

2

0

0

10

20

30

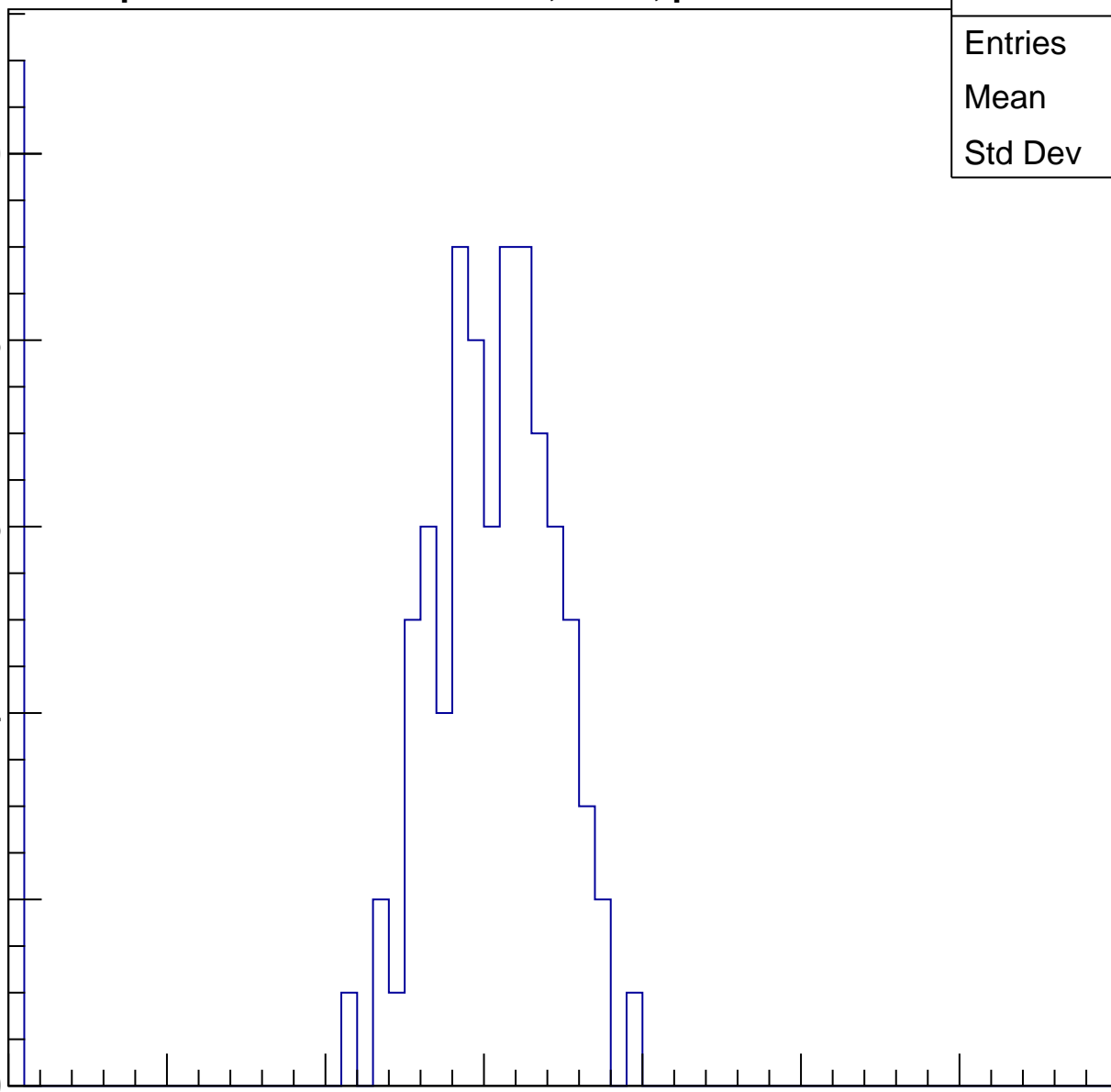
40

50

60

70

ampl

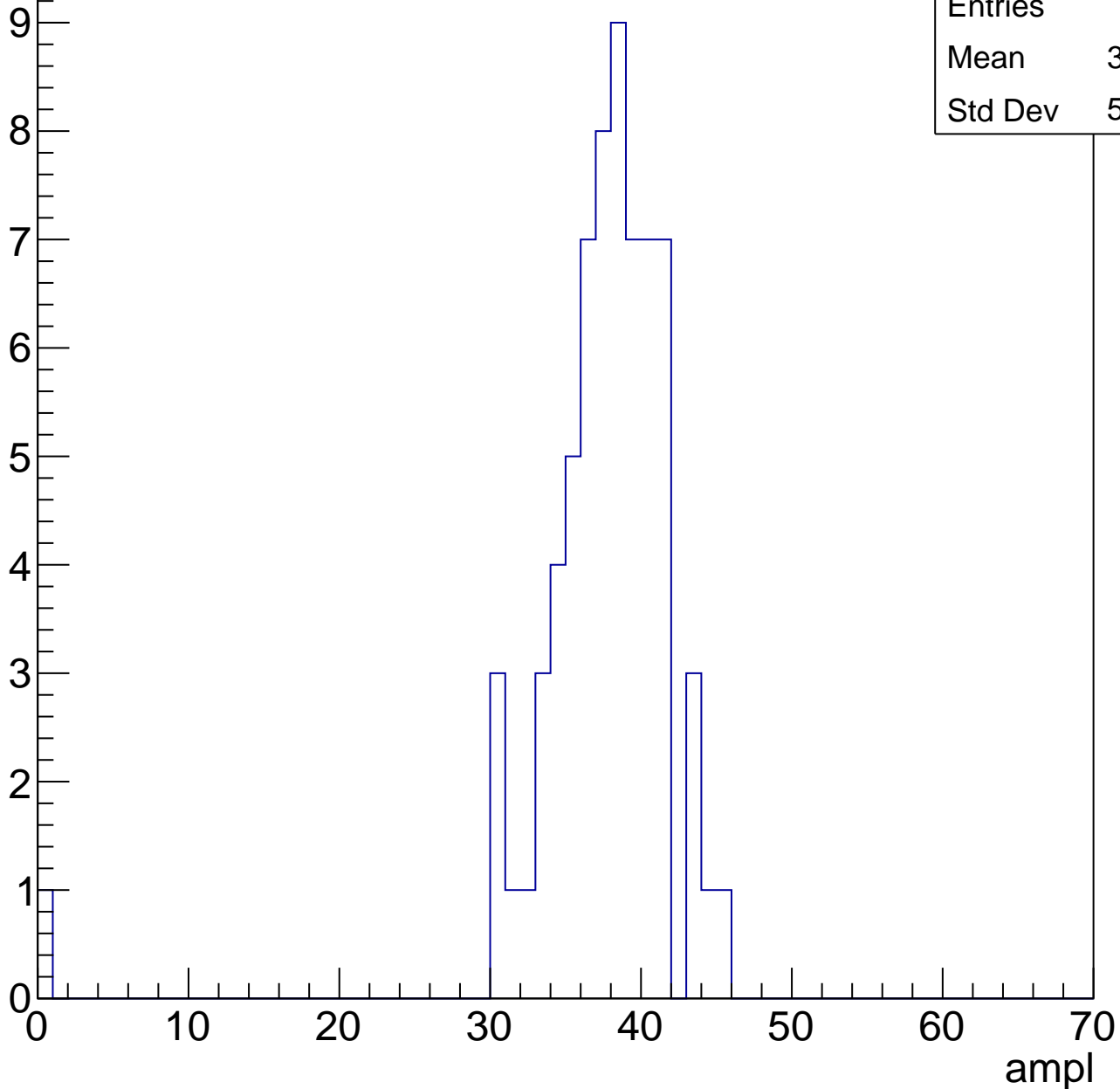


B1L103S, U12-ch13, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	36.93
Std Dev	5.584



B1L103S, U12-ch13, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	59
Mean	40.47
Std Dev	12.69

Entry

10

8

6

4

2

0

0

10

20

30

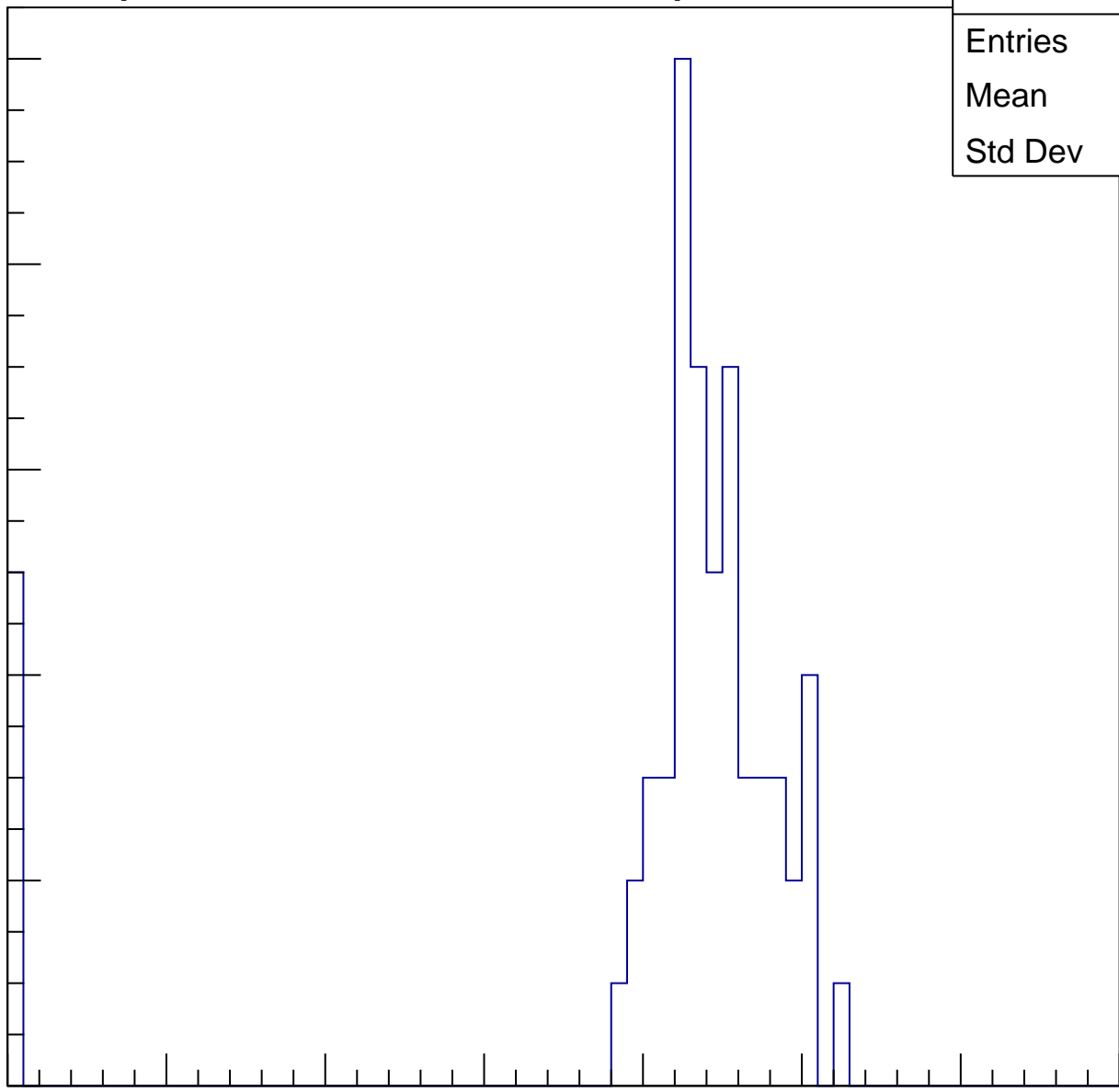
40

50

60

70

ampl

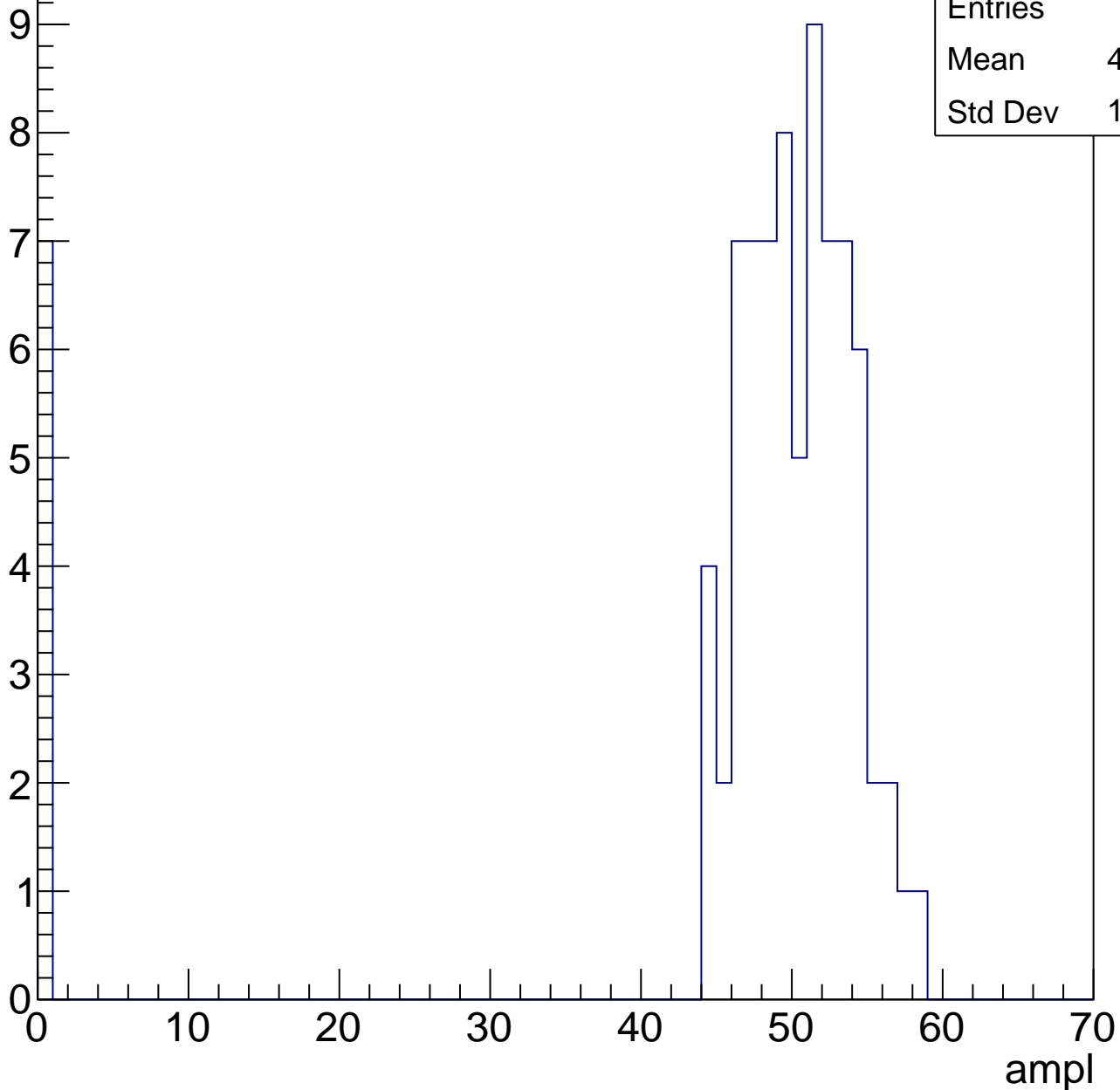


B1L103S, U12-ch13, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

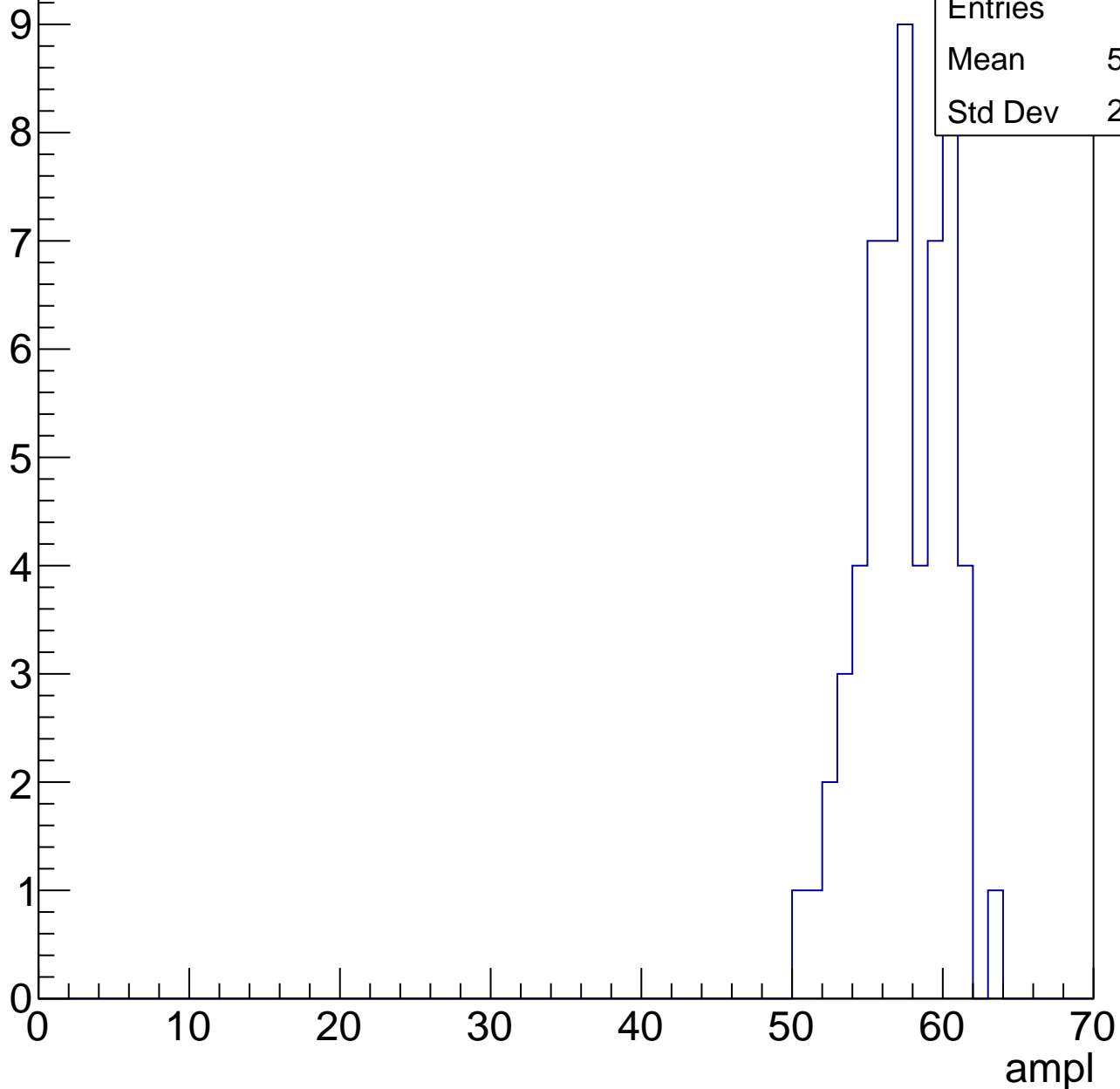
Entries	82
Mean	45.73
Std Dev	14.33



B1L103S, U12-ch13, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

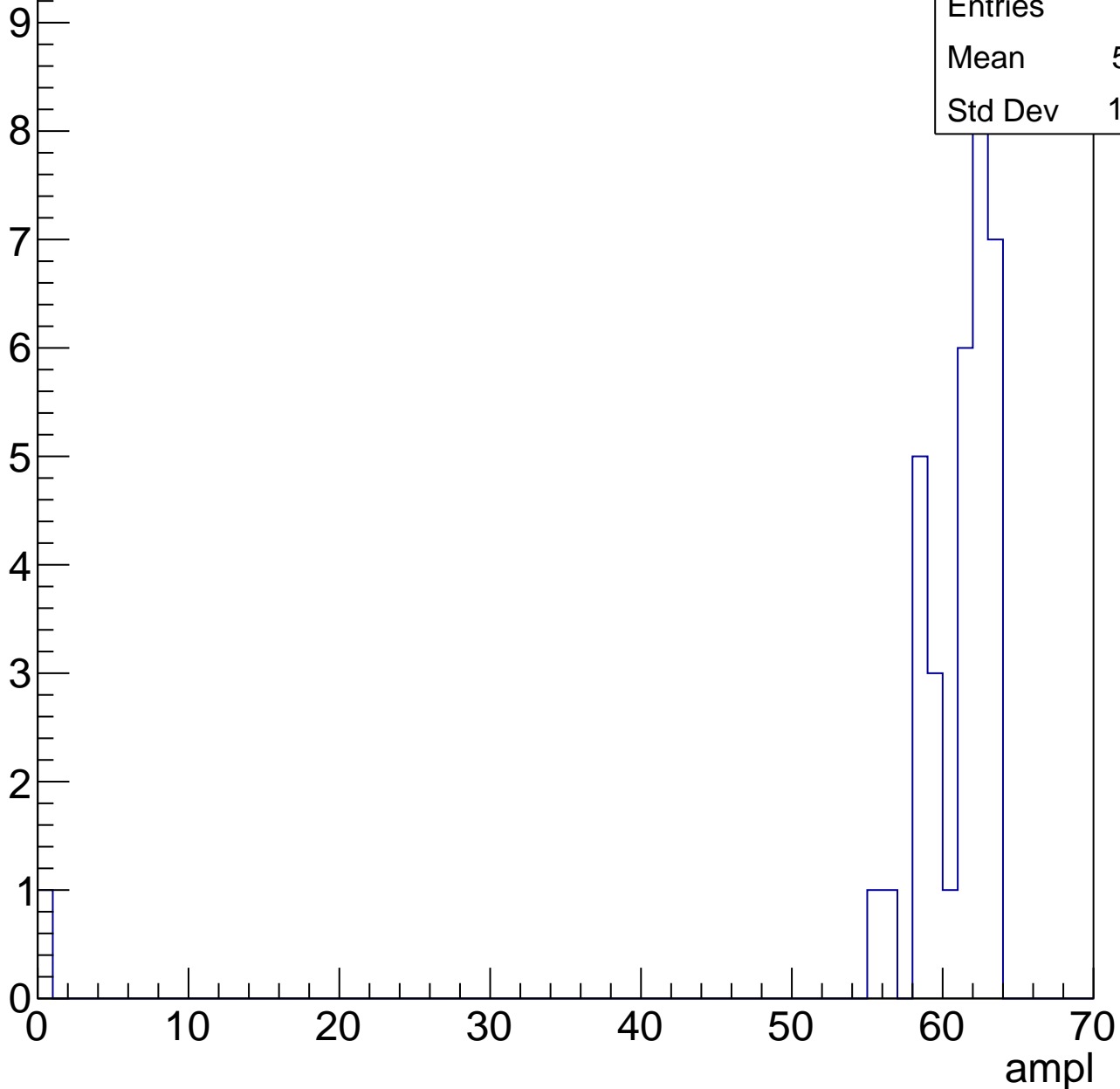


B1L103S, U12-ch13, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	34
Mean	58.91
Std Dev	10.47



B1L103S, U12-ch13, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	3
Mean	62.67
Std Dev	0.4714

ampl

0 10 20 30 40 50 60 70

B1L103S, U12-ch13, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U12-ch14, adc0

calib_packv5_041523_1651.root, FC#0, port C2

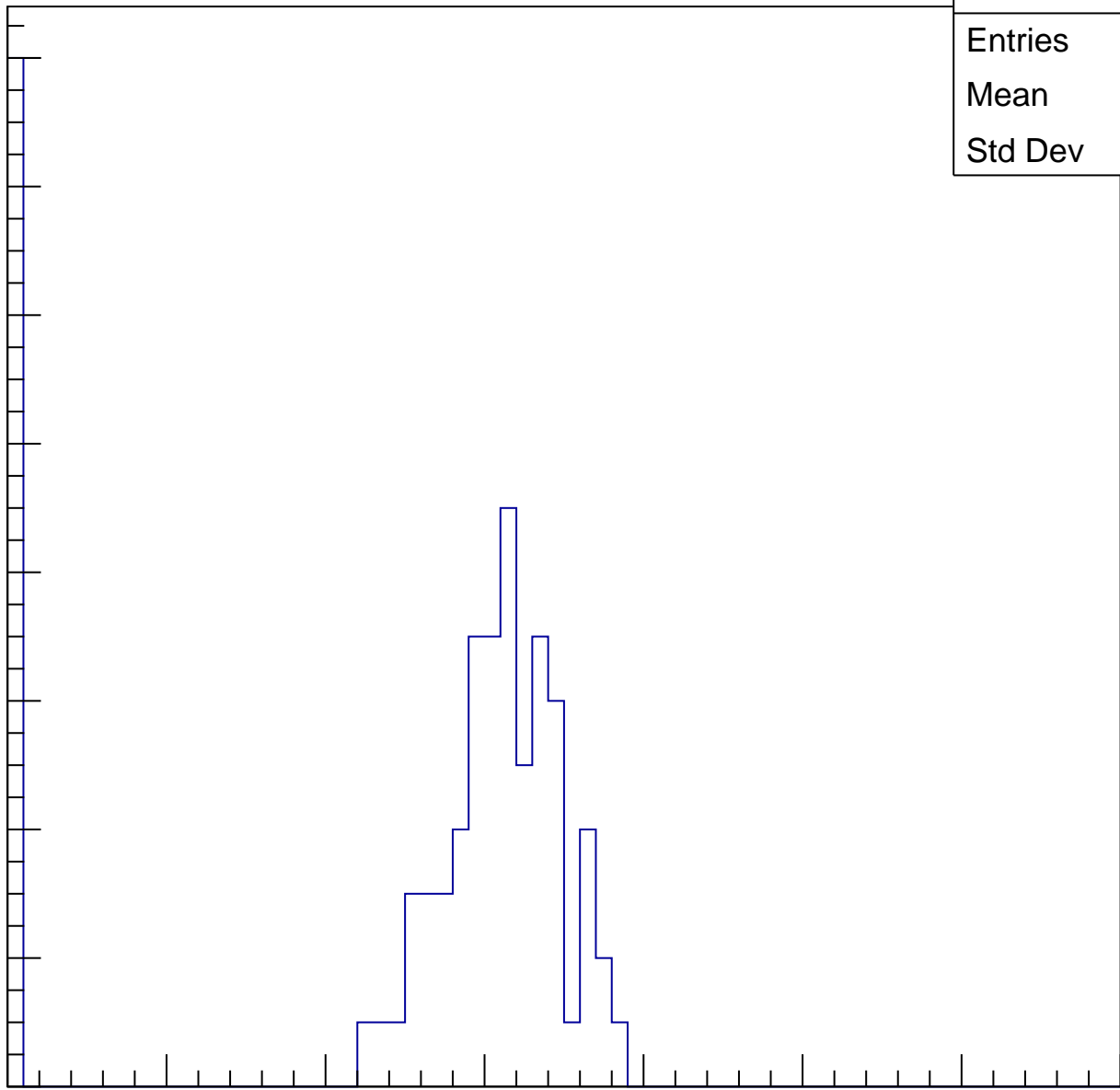
Entries	81
Mean	24.6
Std Dev	12.61

Entry

16
14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70

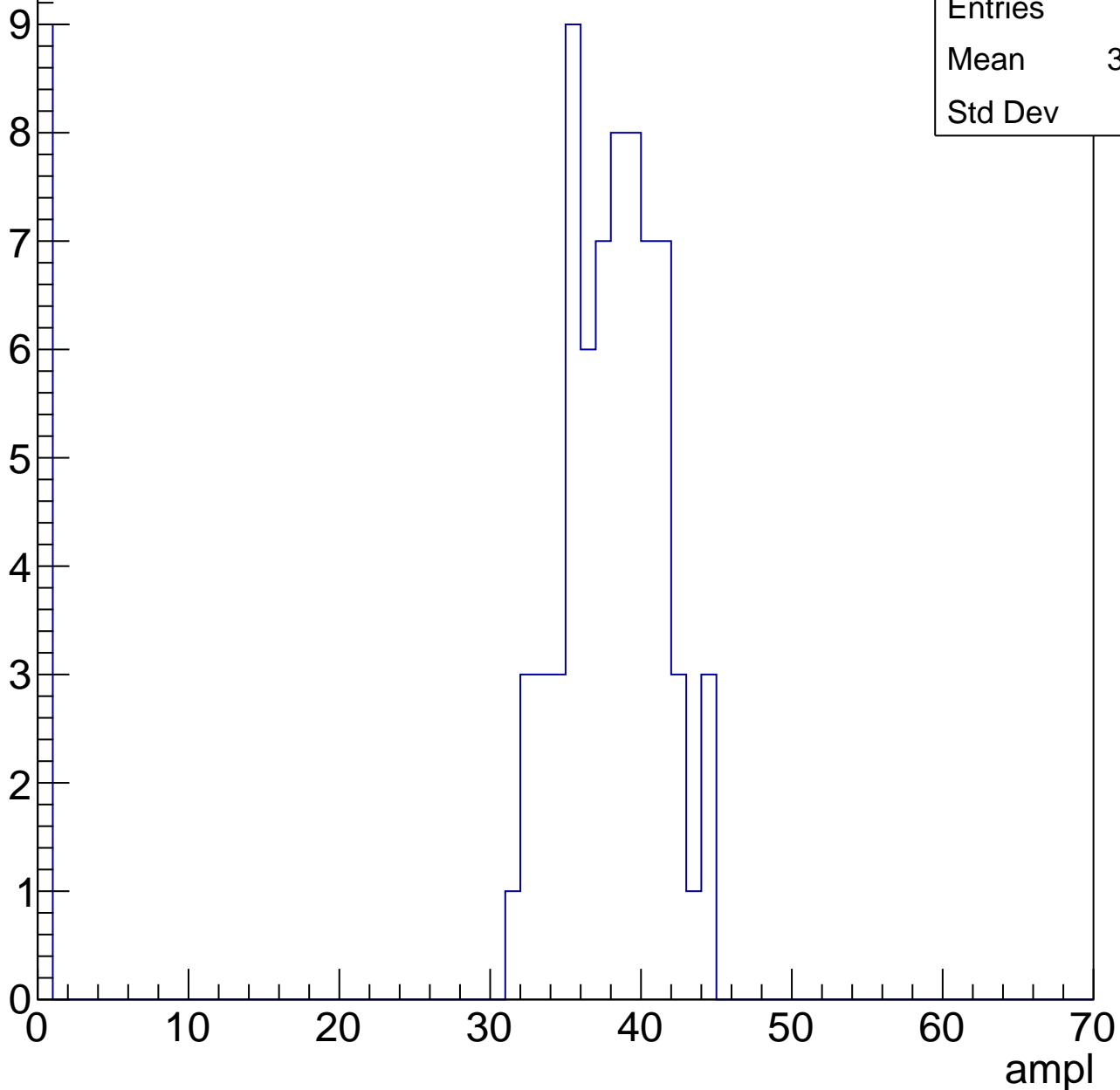


B1L103S, U12-ch14, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	78
Mean	33.36
Std Dev	12.4

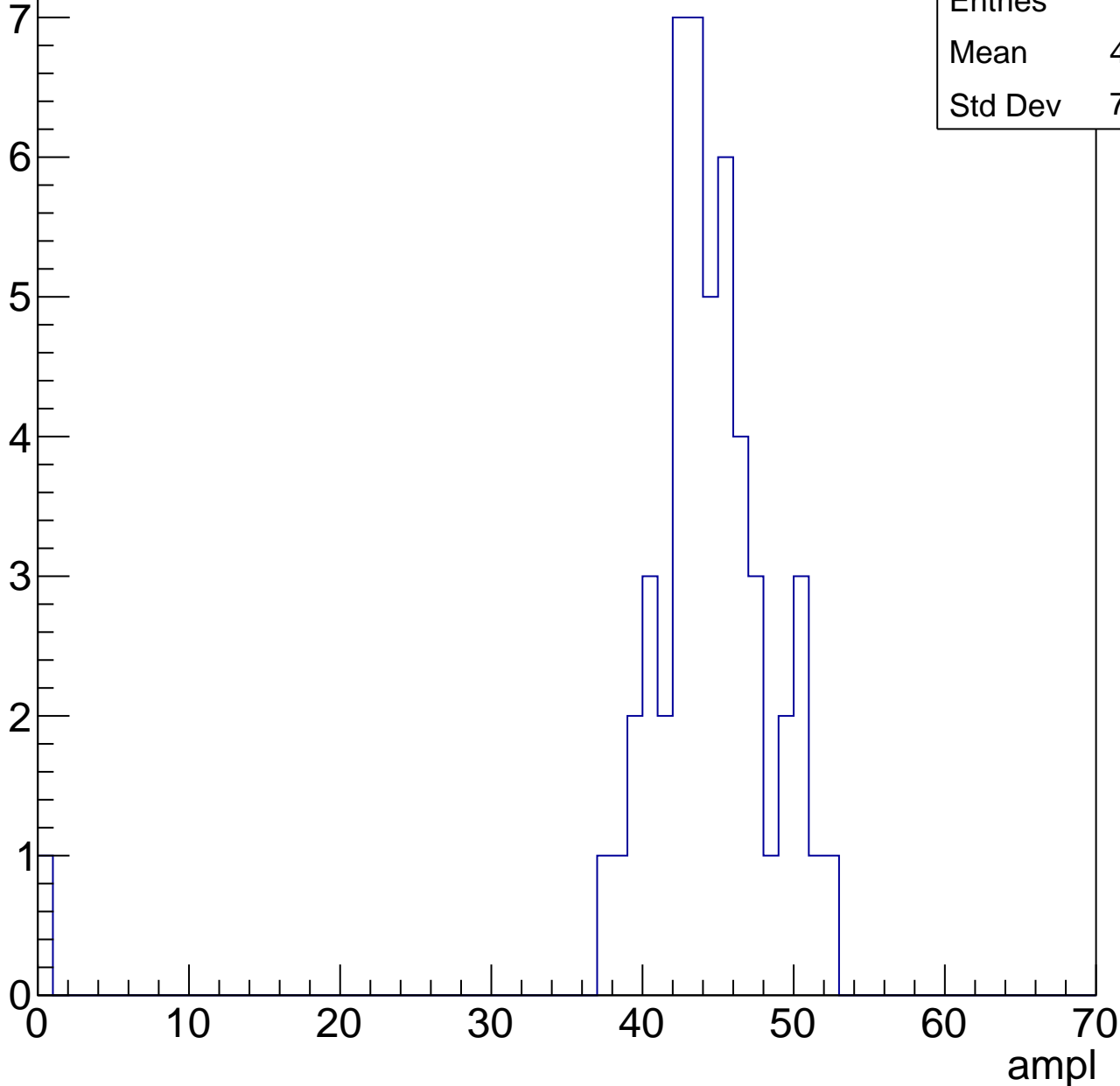


B1L103S, U12-ch14, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	50
Mean	43.28
Std Dev	7.046

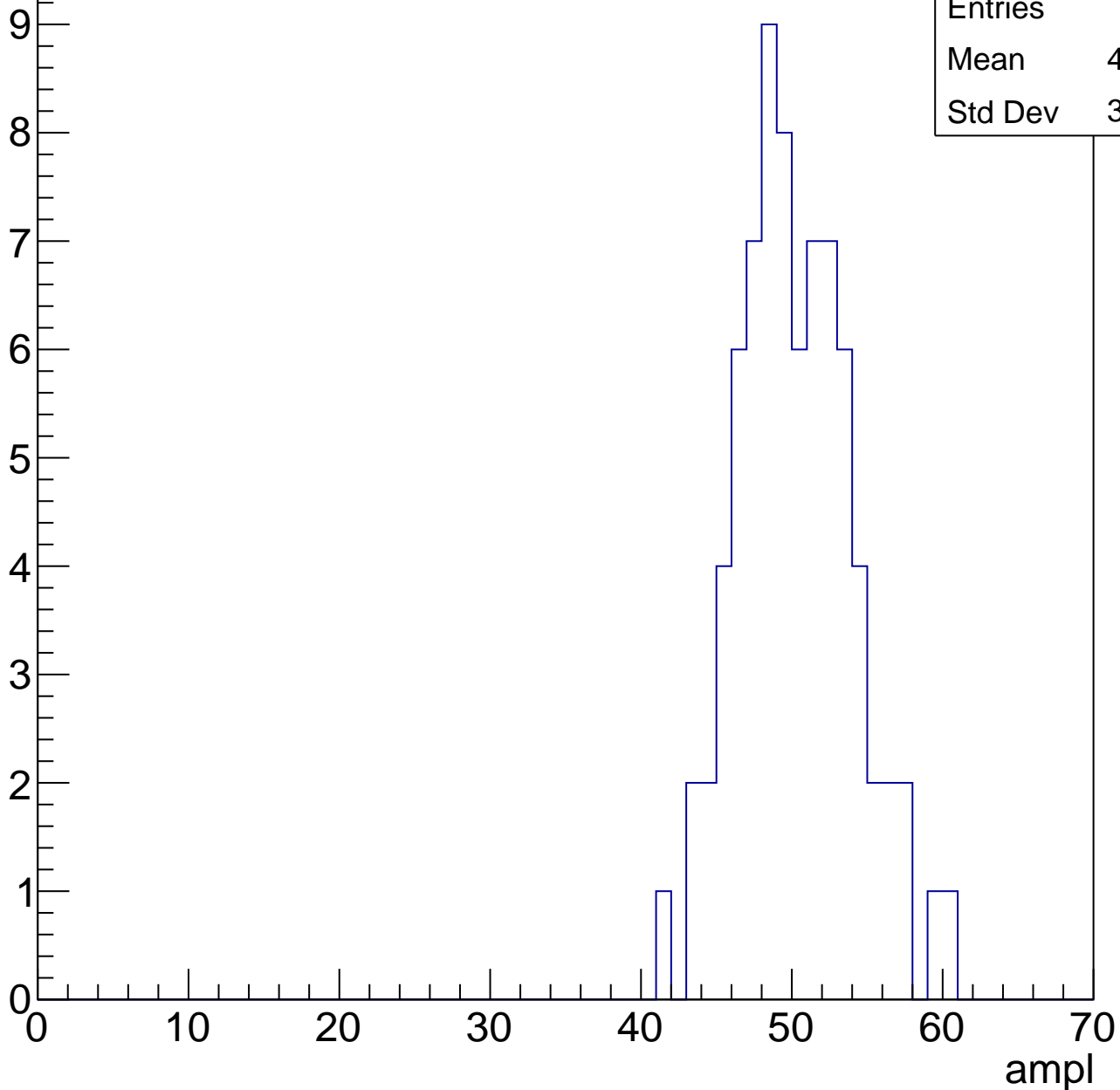


B1L103S, U12-ch14, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	77
Mean	49.79
Std Dev	3.788

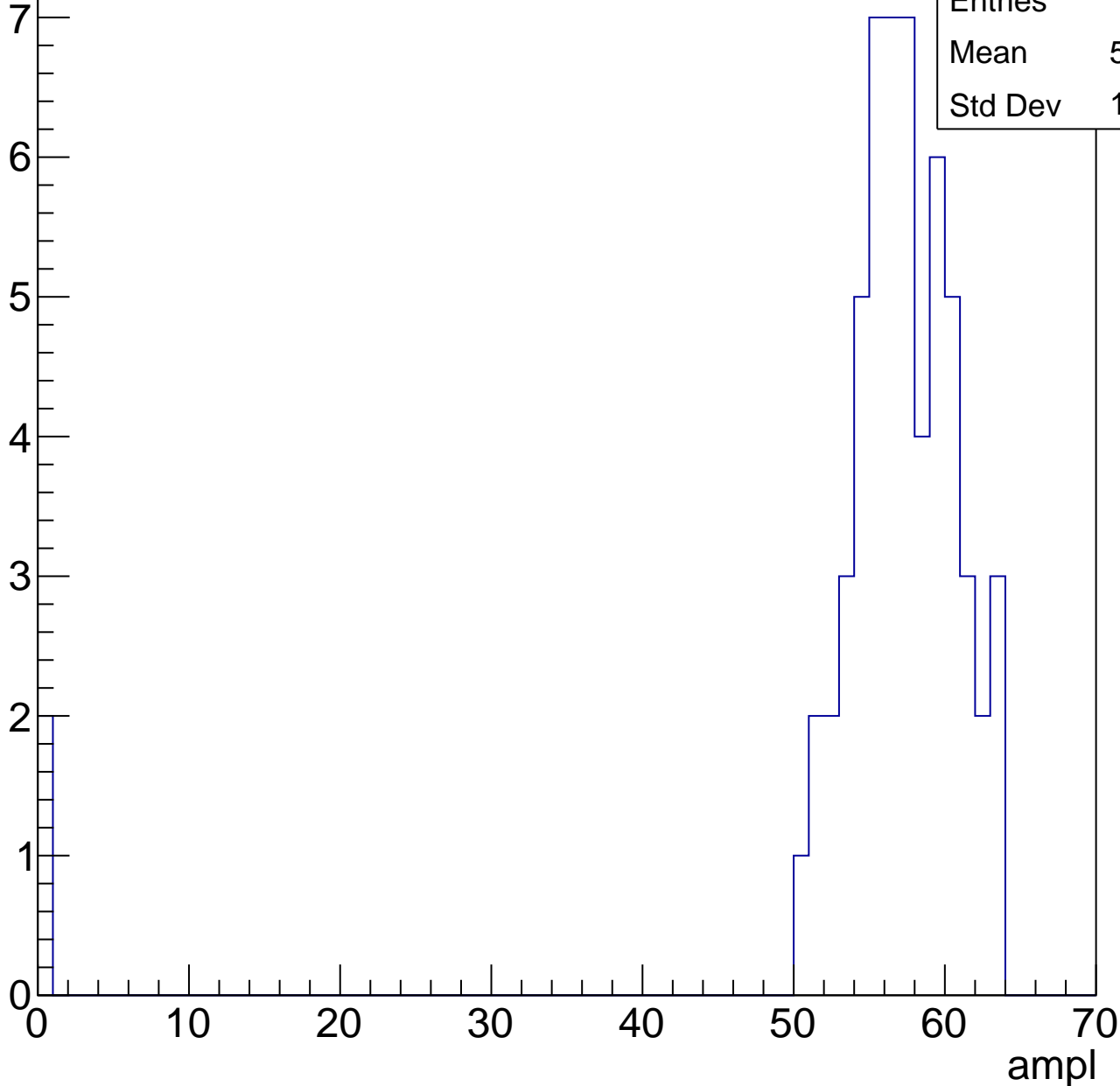


B1L103S, U12-ch14, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	54.97
Std Dev	10.76

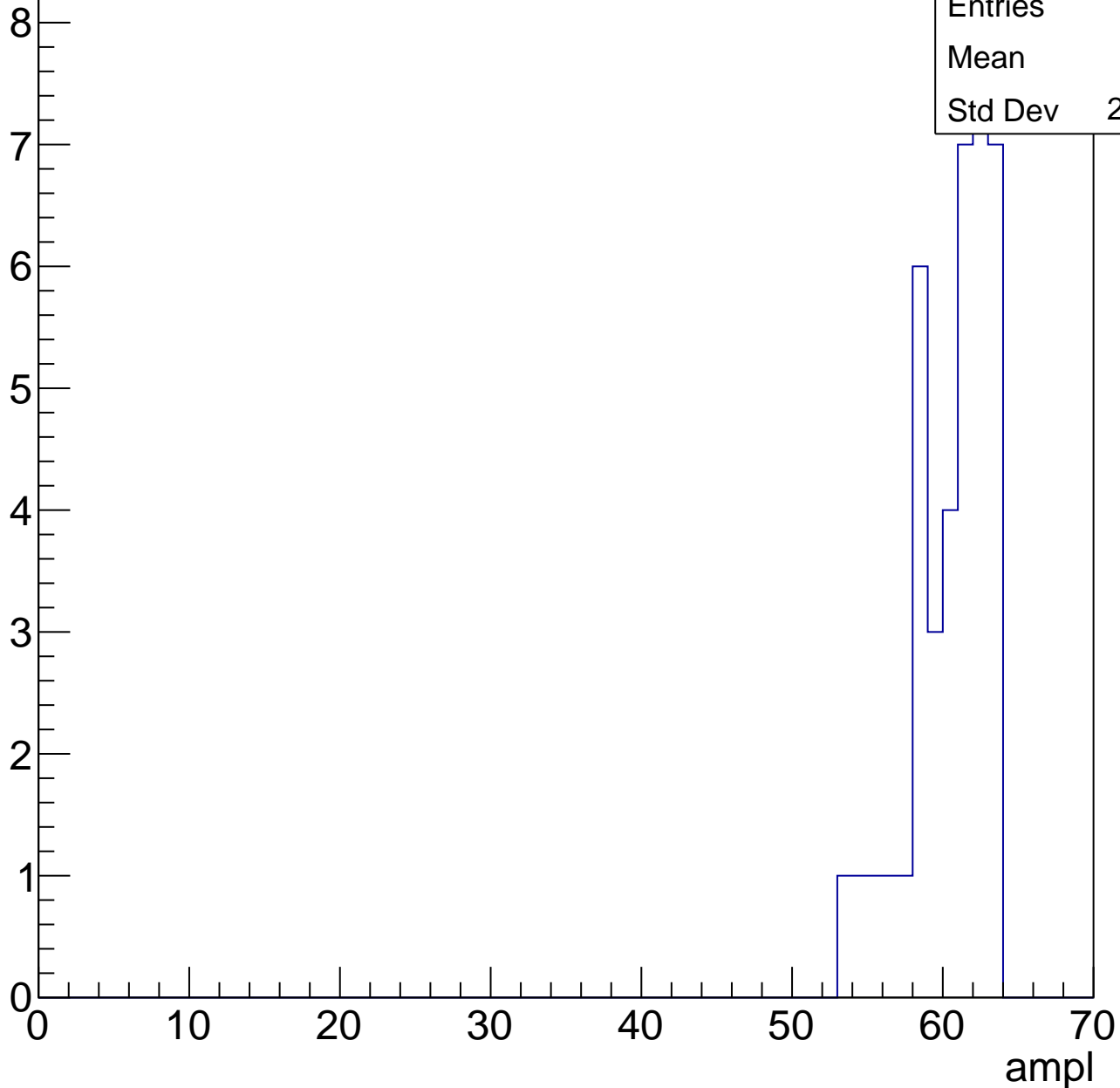


B1L103S, U12-ch14, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	40
Mean	60.1
Std Dev	2.567



B1L103S, U12-ch14, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	1
Mean	0
Std Dev	0

B1L103S, U12-ch14, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

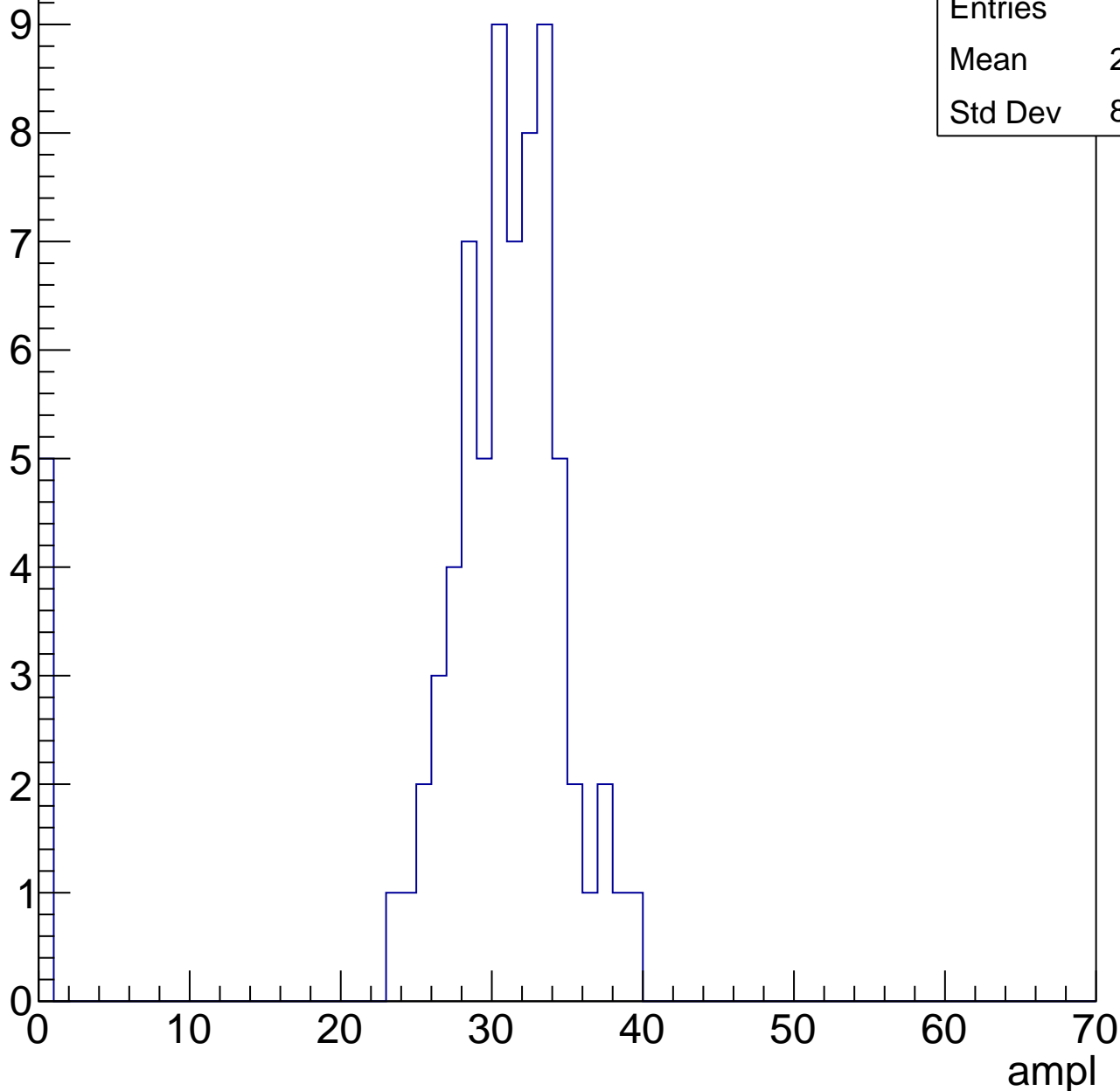


B1L103S, U12-ch15, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	73
Mean	28.64
Std Dev	8.397

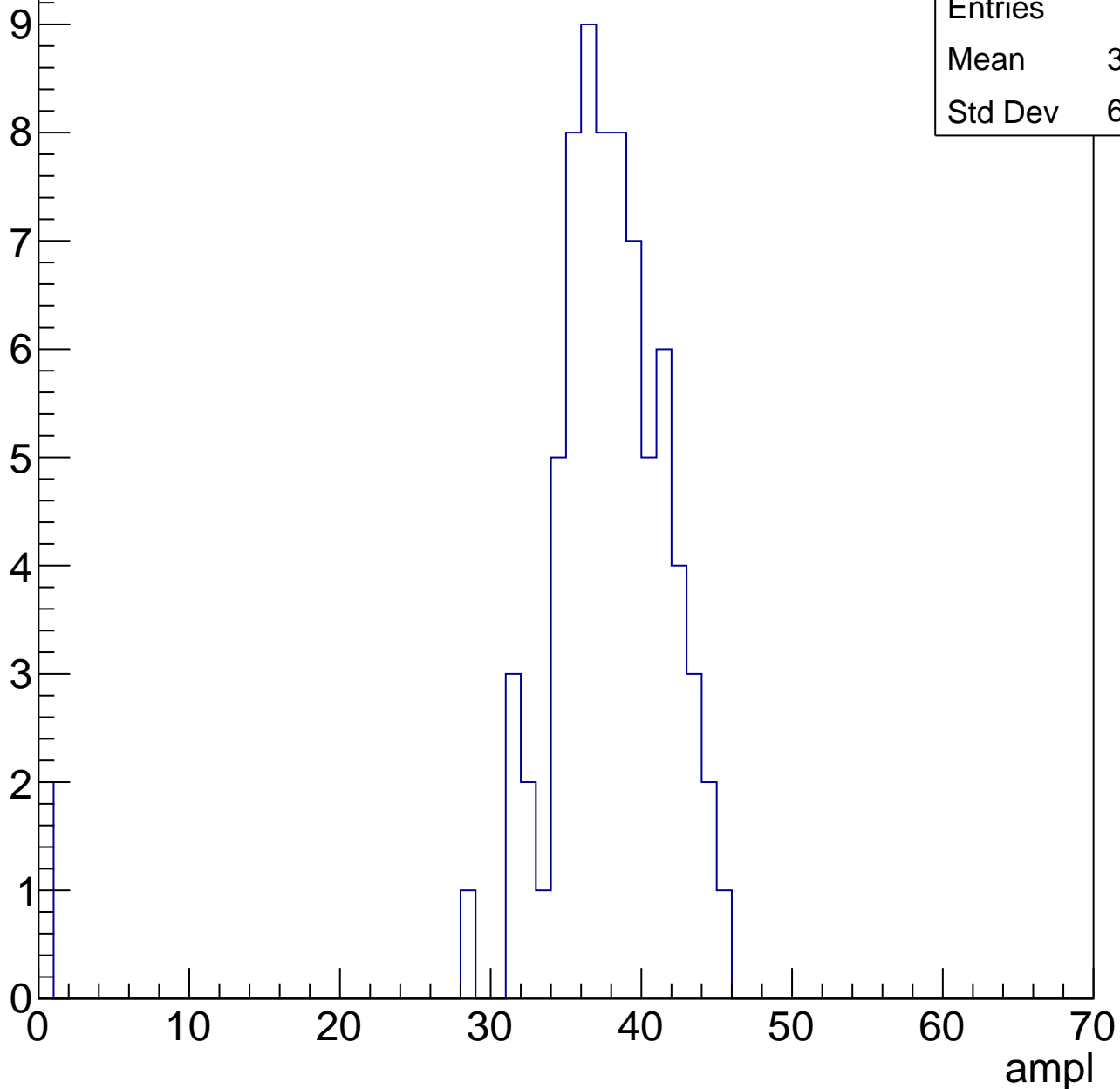


B1L103S, U12-ch15, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

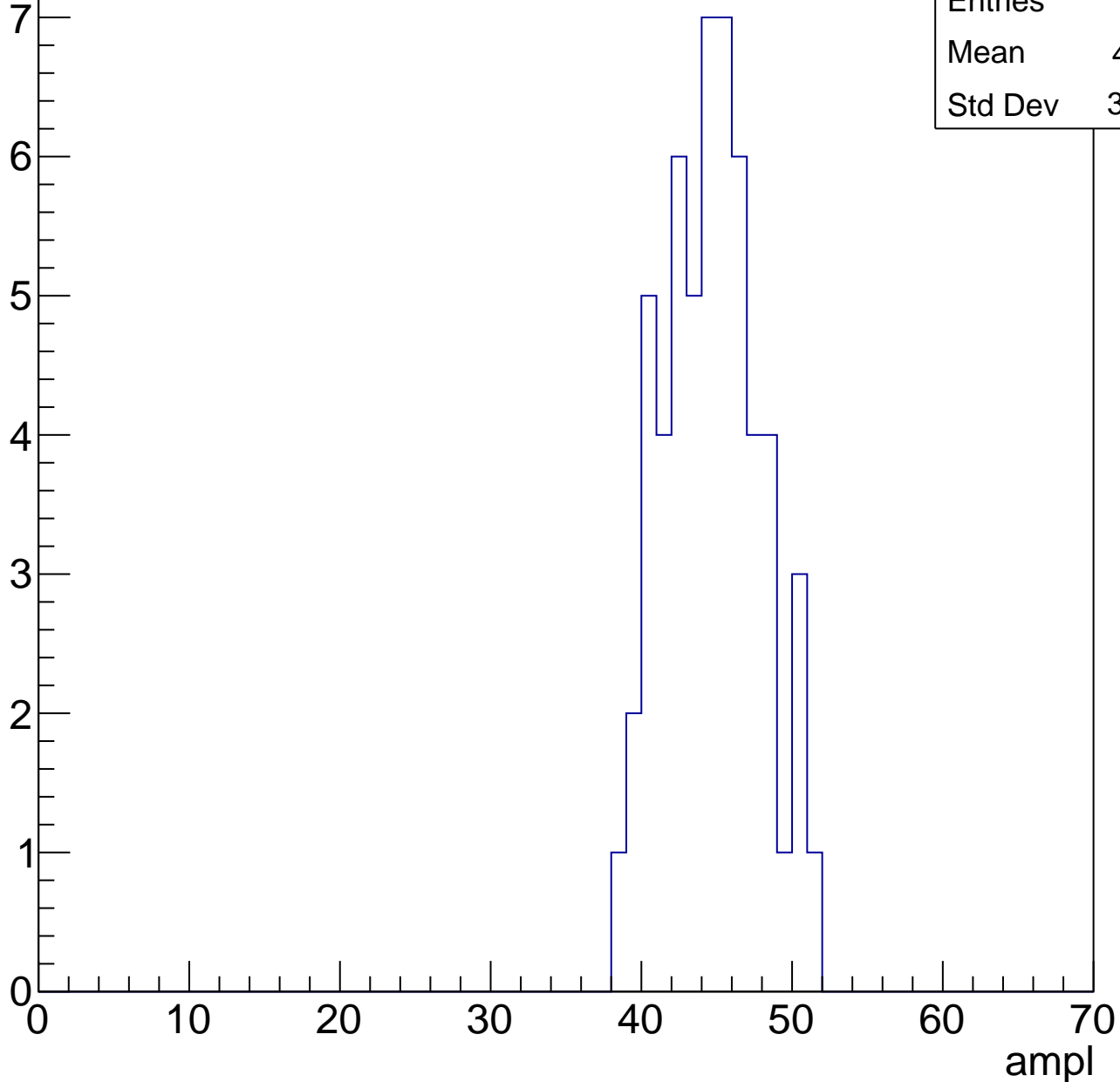
Entries	75
Mean	36.55
Std Dev	6.938



B1L103S, U12-ch15, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry



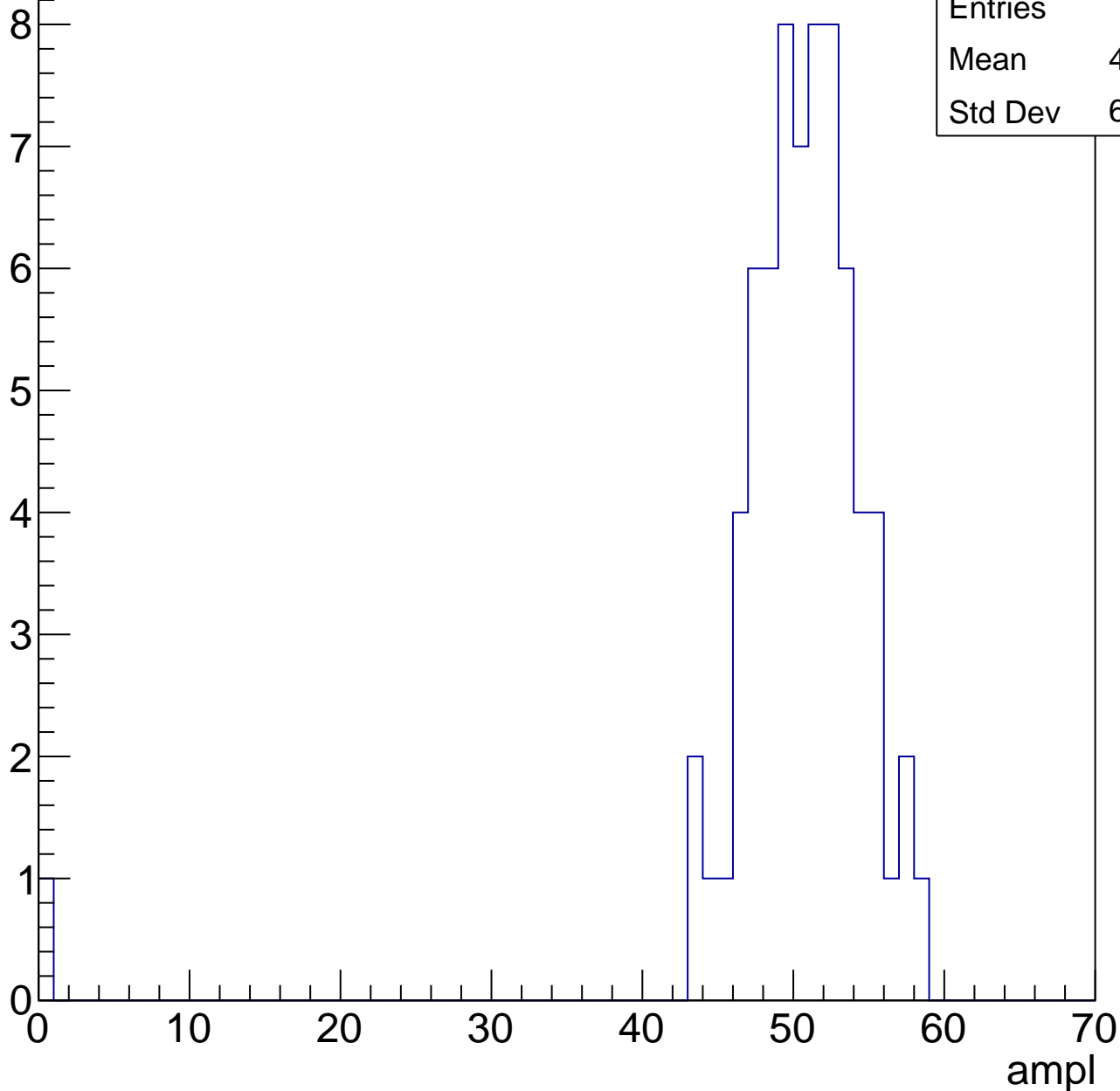
Entries	56
Mean	44.21
Std Dev	3.109

B1L103S, U12-ch15, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	49.67
Std Dev	6.822

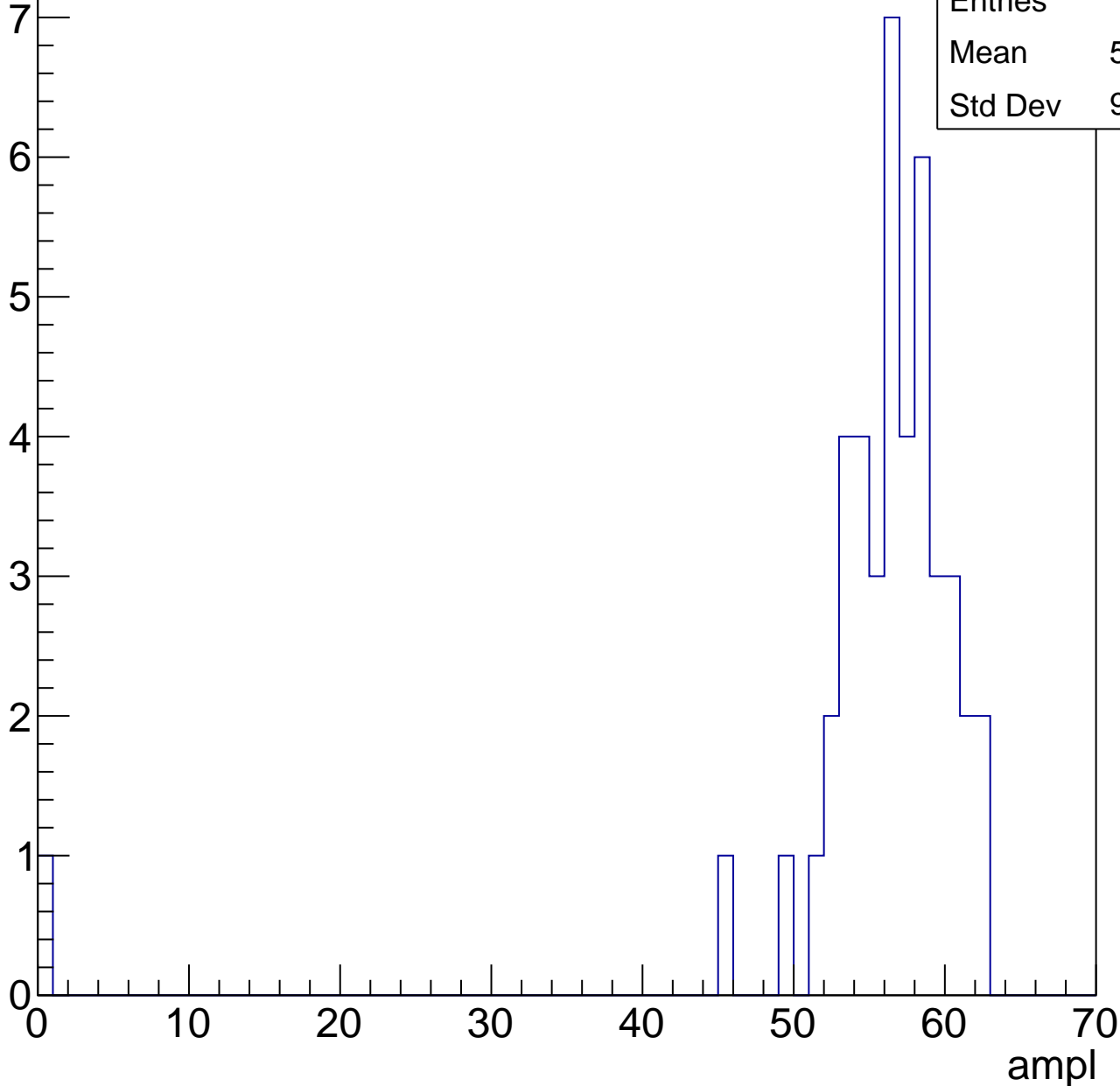


B1L103S, U12-ch15, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	44
Mean	54.84
Std Dev	9.025

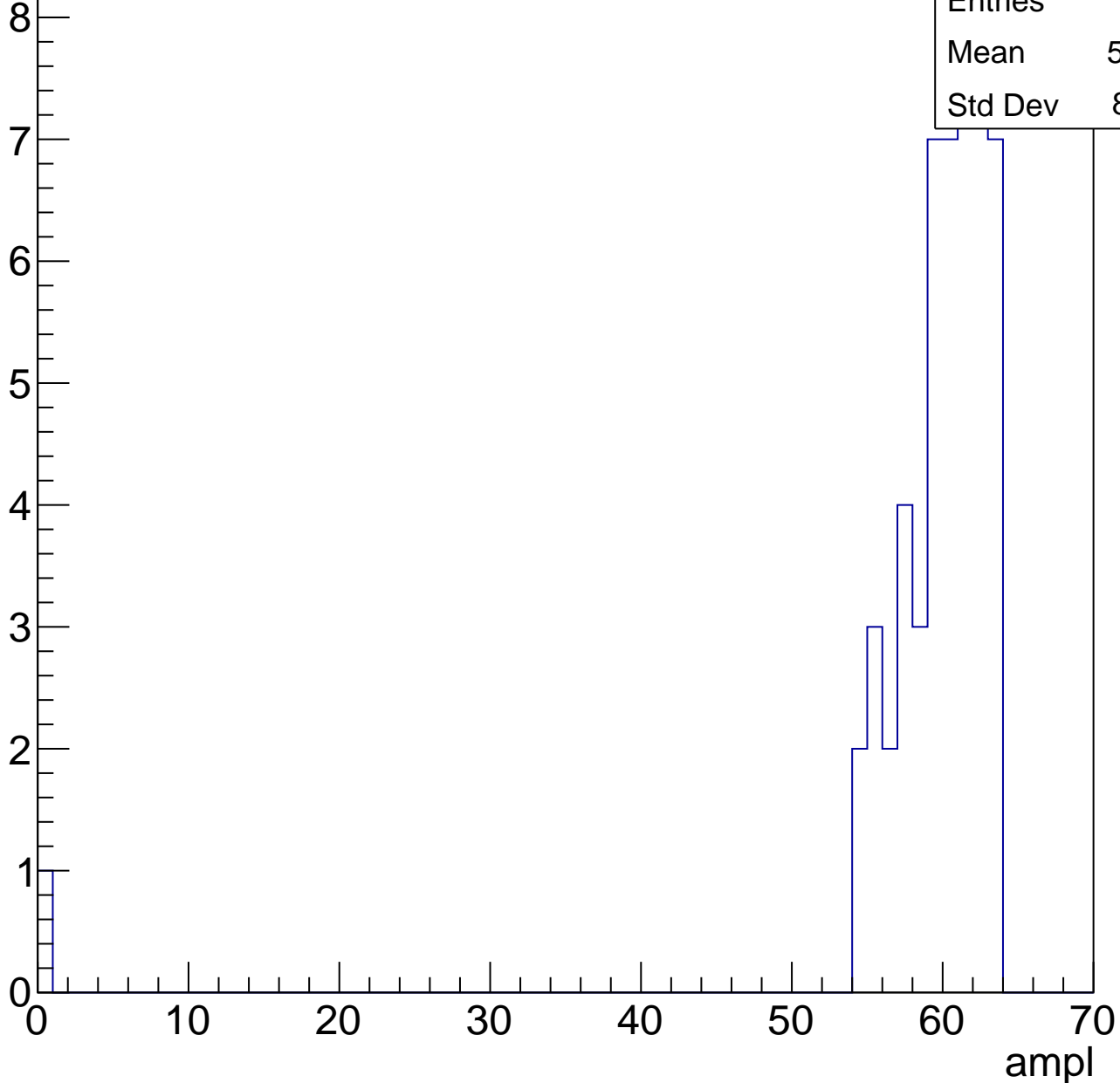


B1L103S, U12-ch15, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	52
Mean	58.56
Std Dev	8.581



B1L103S, U12-ch15, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

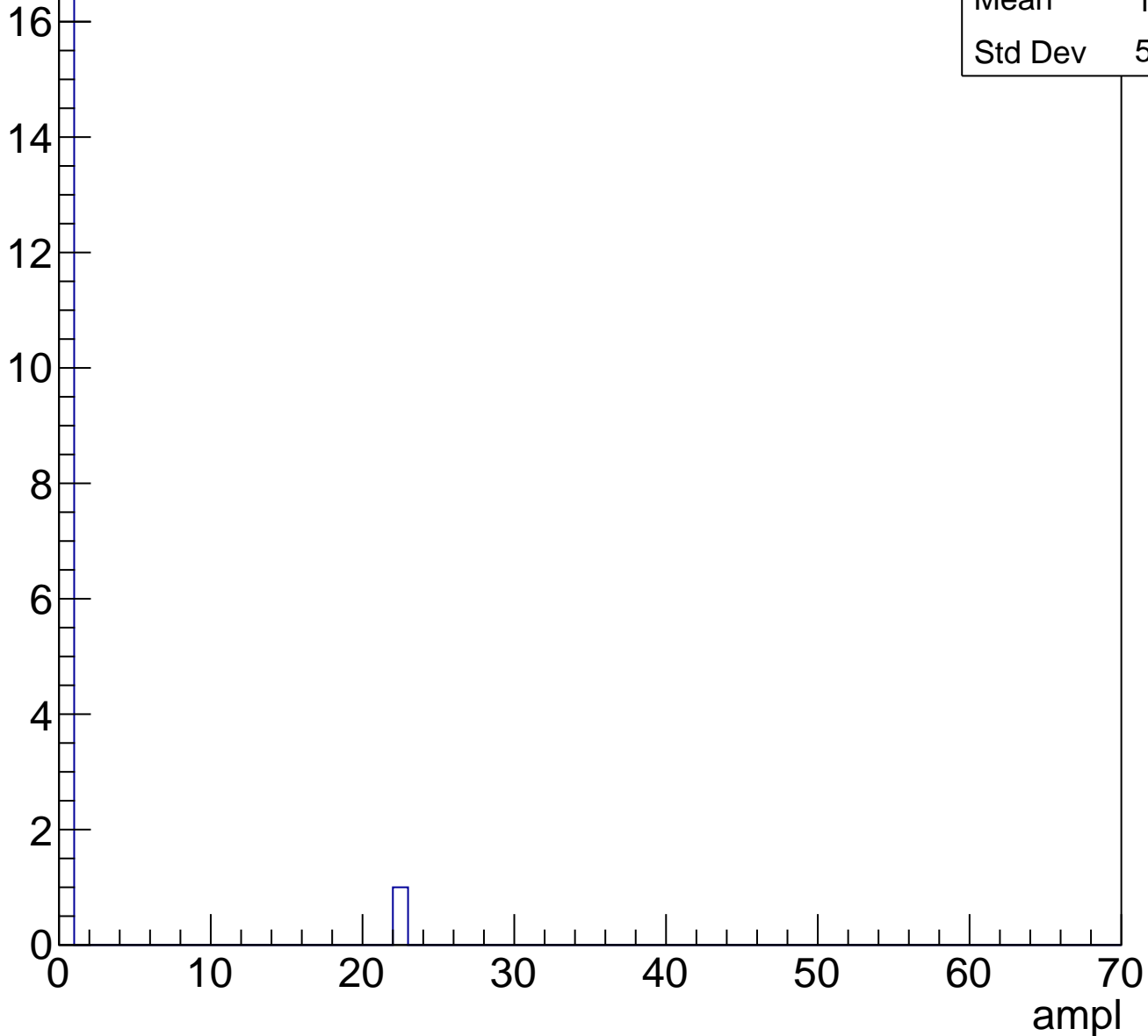


B1L103S, U12-ch15, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	18
Mean	1.222
Std Dev	5.039

Entry

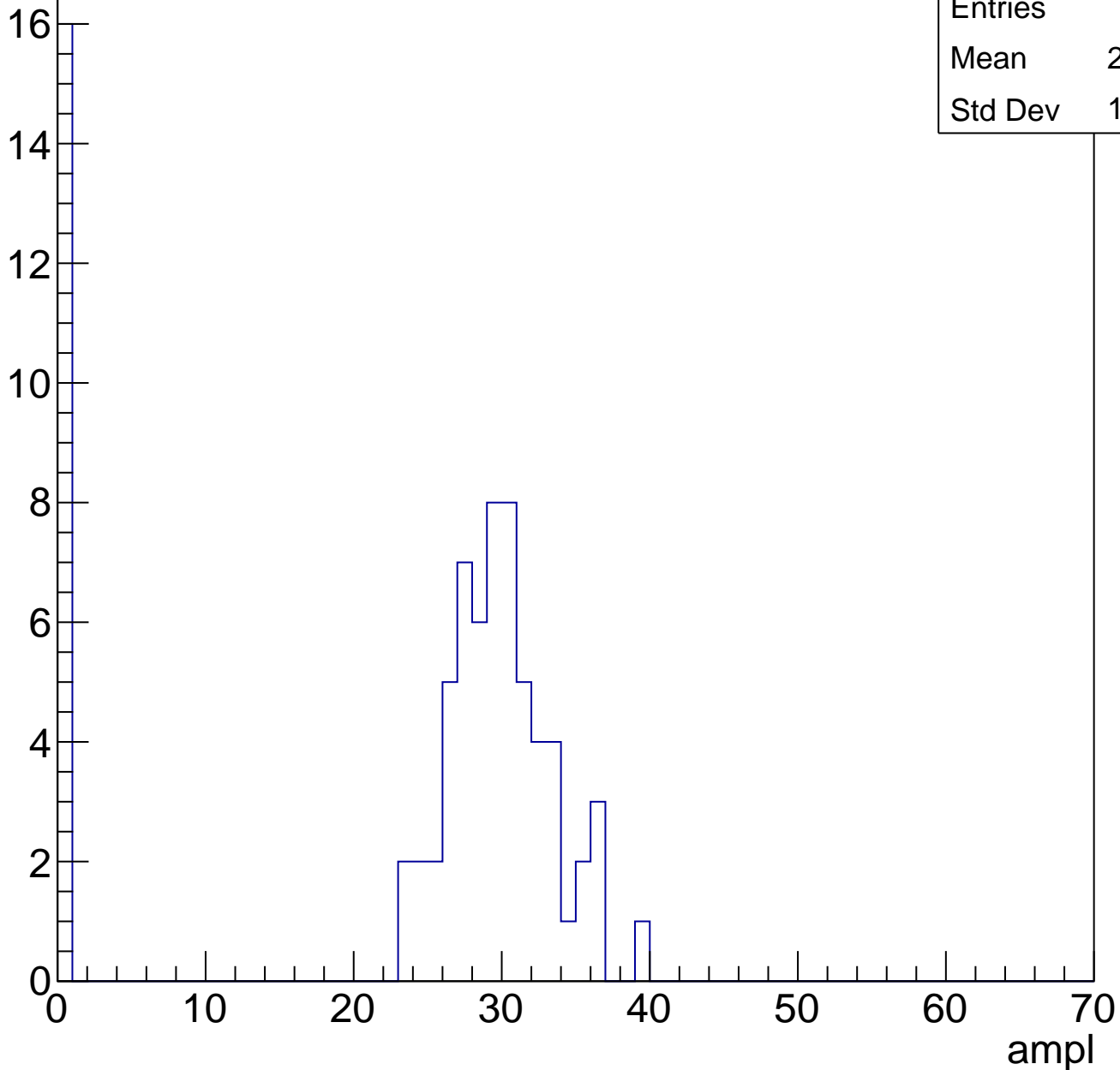


B1L103S, U12-ch16, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	76
Mean	23.28
Std Dev	12.39

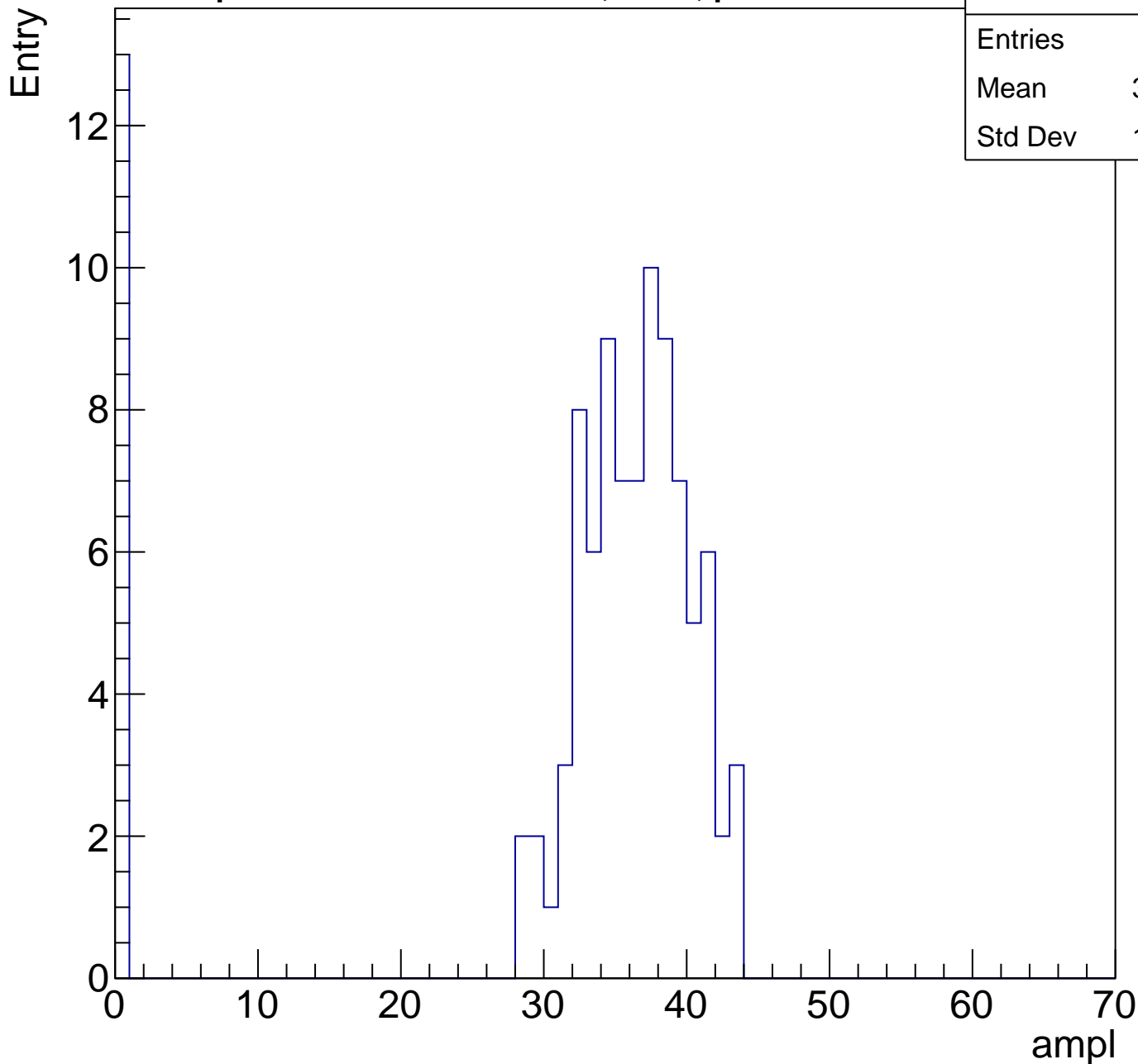
Entry



B1L103S, U12-ch16, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	100
Mean	31.38
Std Dev	12.58

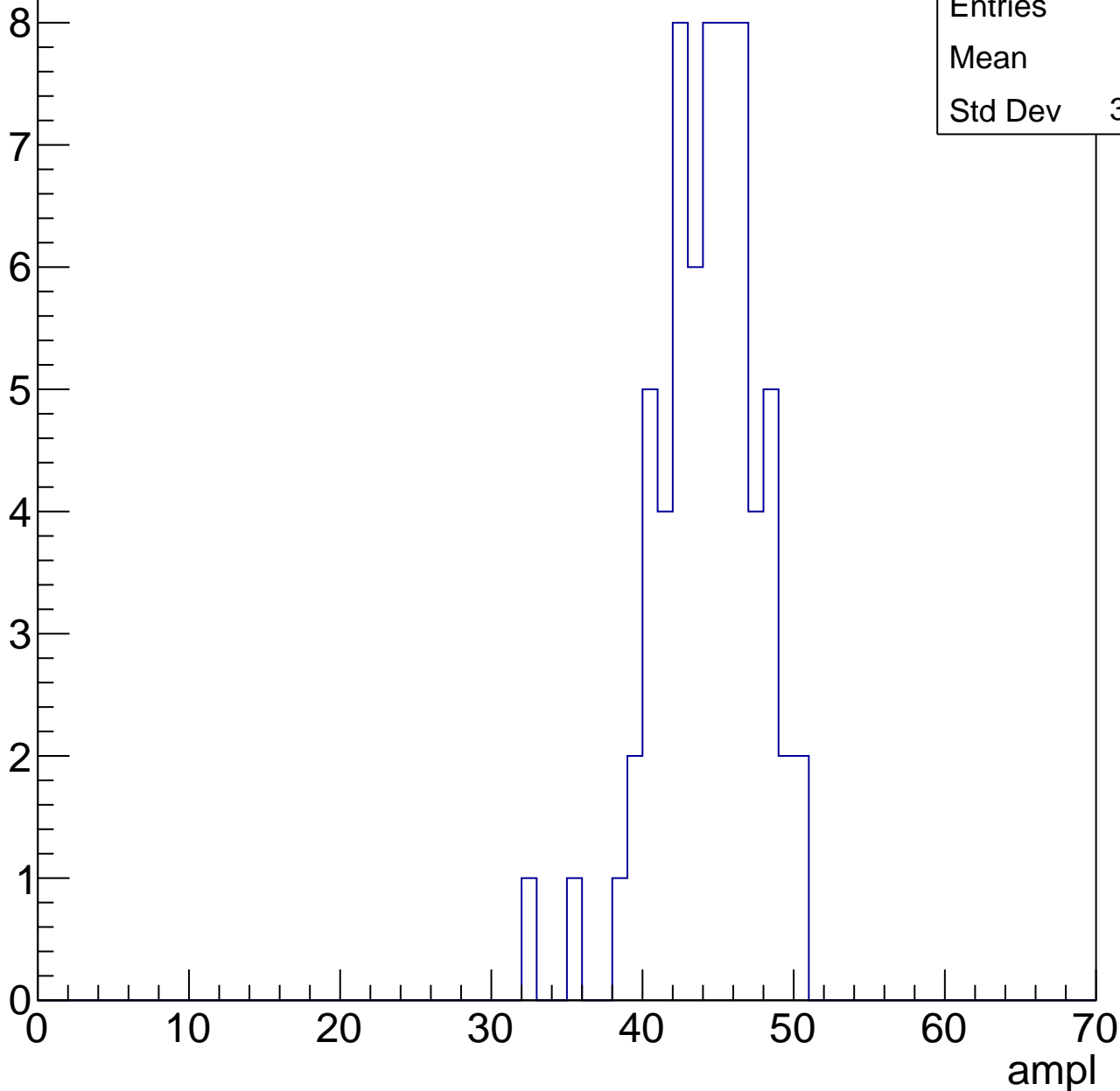


B1L103S, U12-ch16, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	43.8
Std Dev	3.375

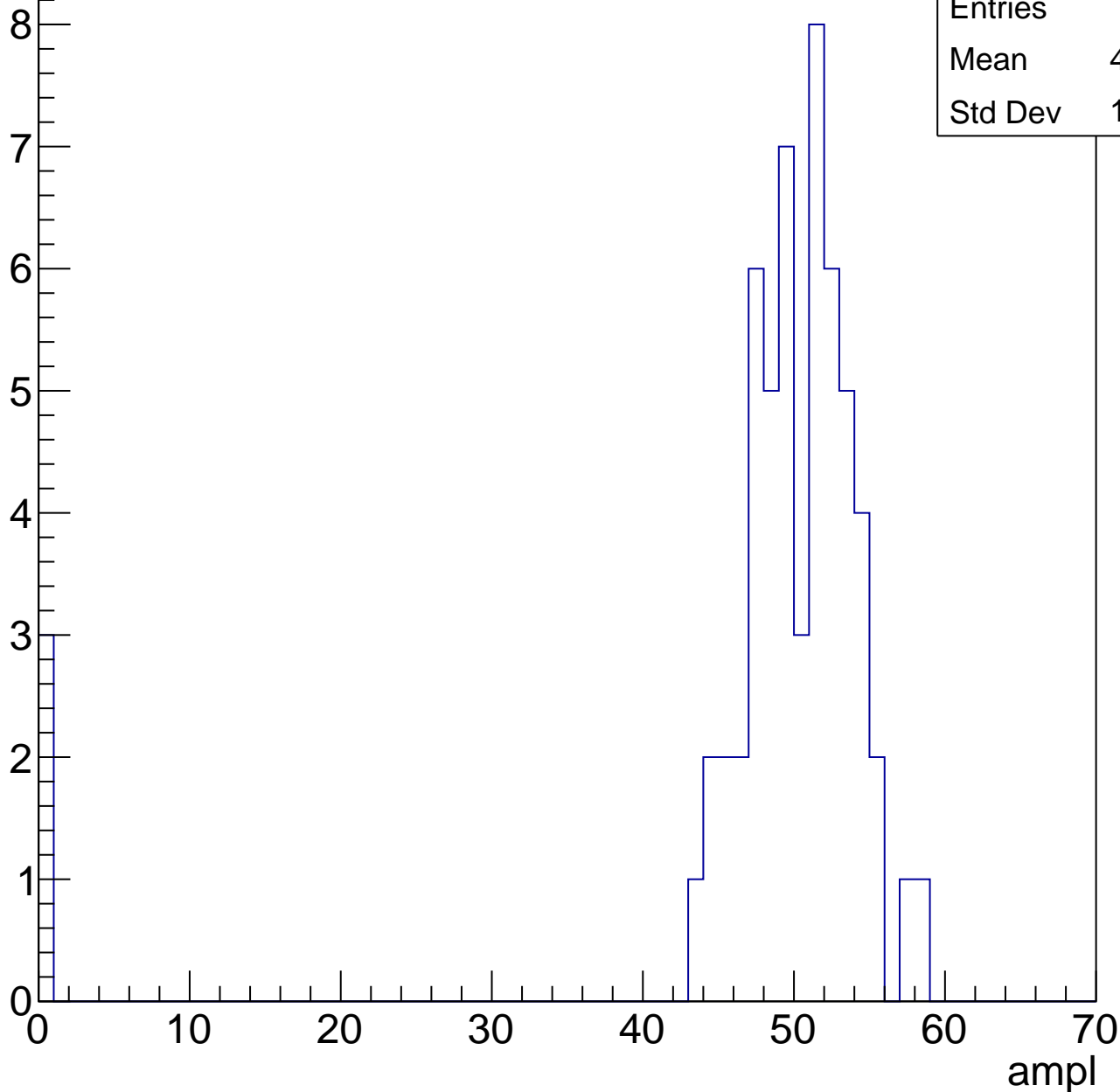


B1L103S, U12-ch16, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	47.48
Std Dev	11.54

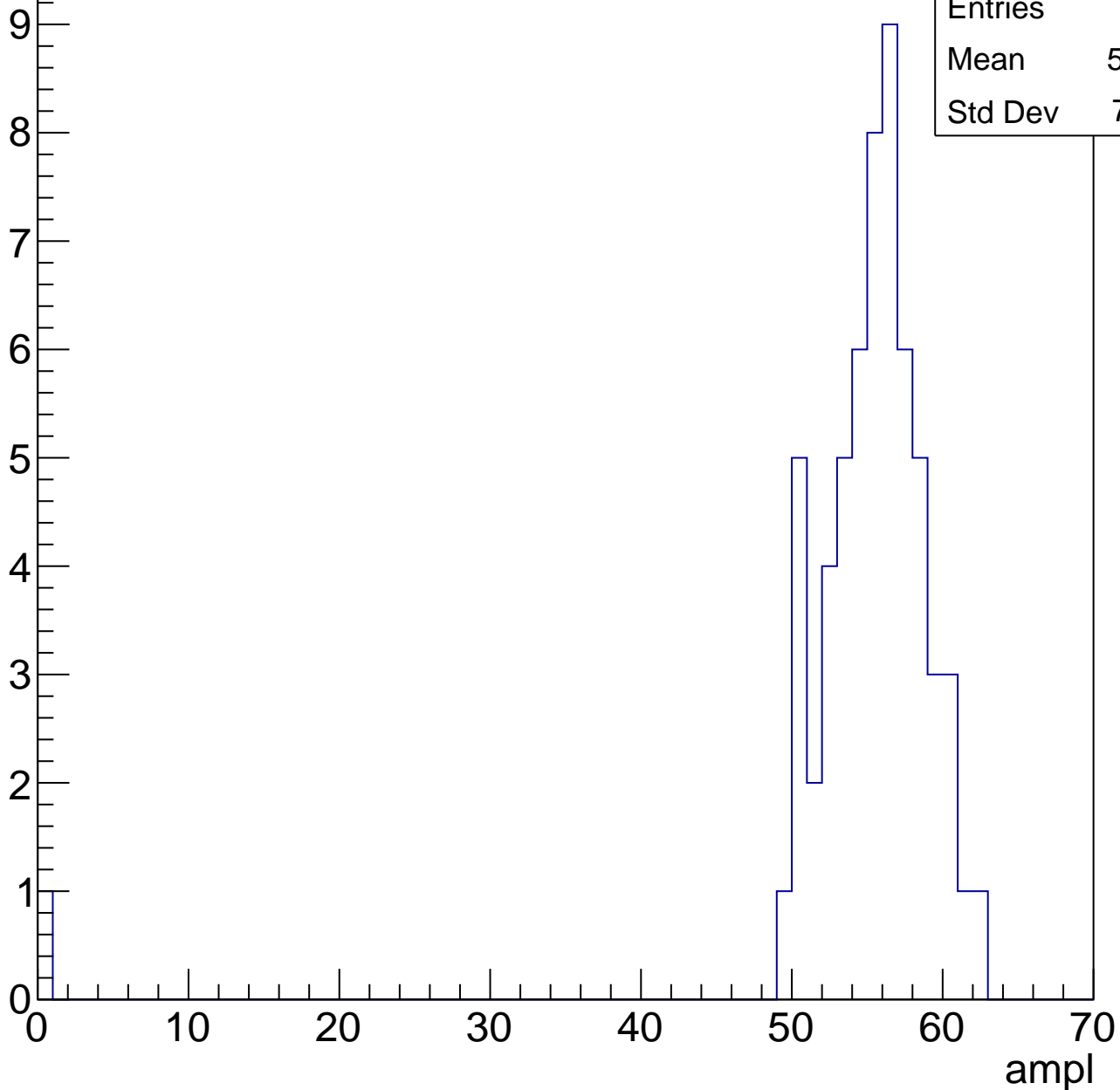


B1L103S, U12-ch16, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	54.23
Std Dev	7.671

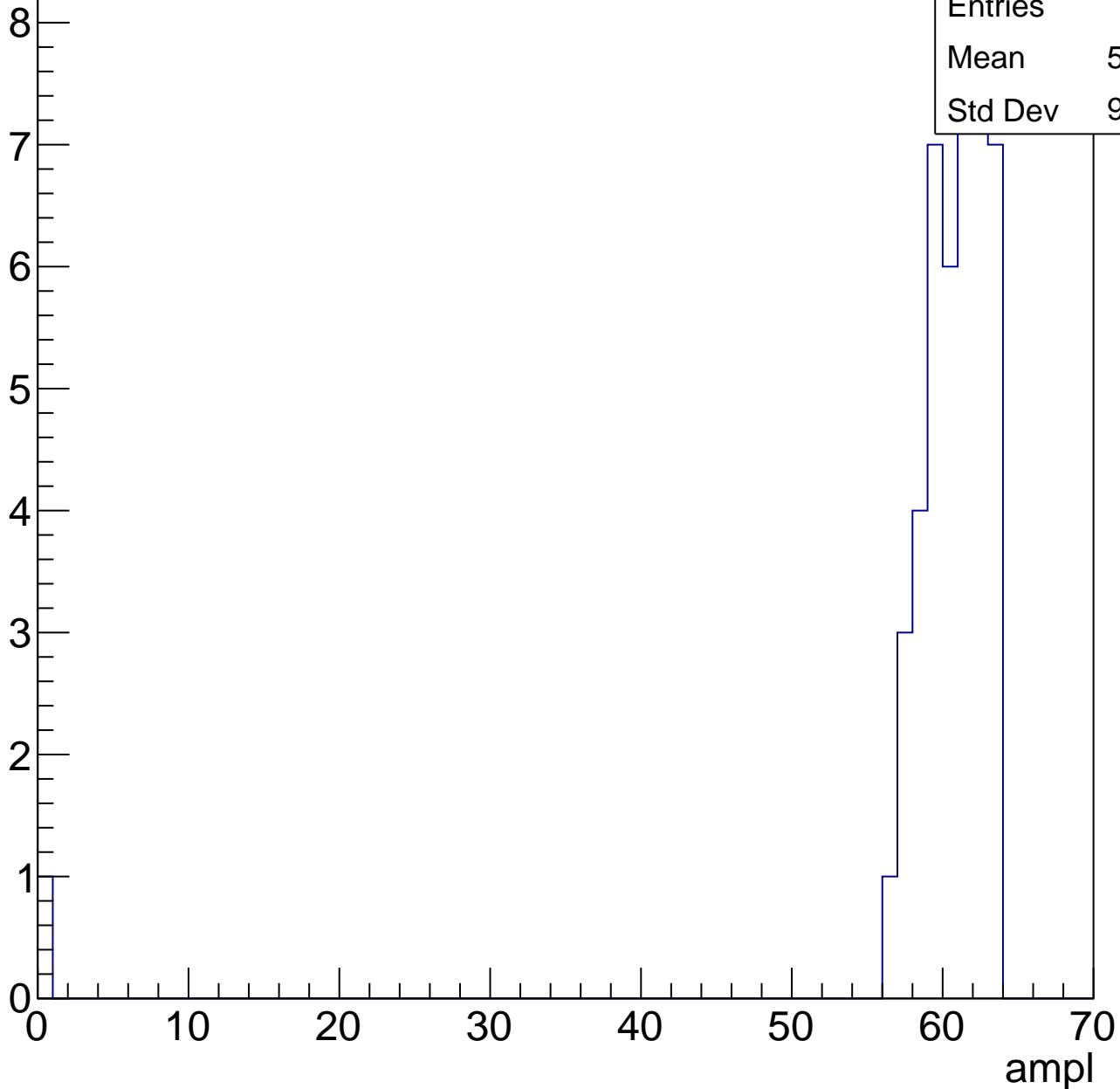


B1L103S, U12-ch16, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	45
Mean	59.04
Std Dev	9.102



B1L103S, U12-ch16, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

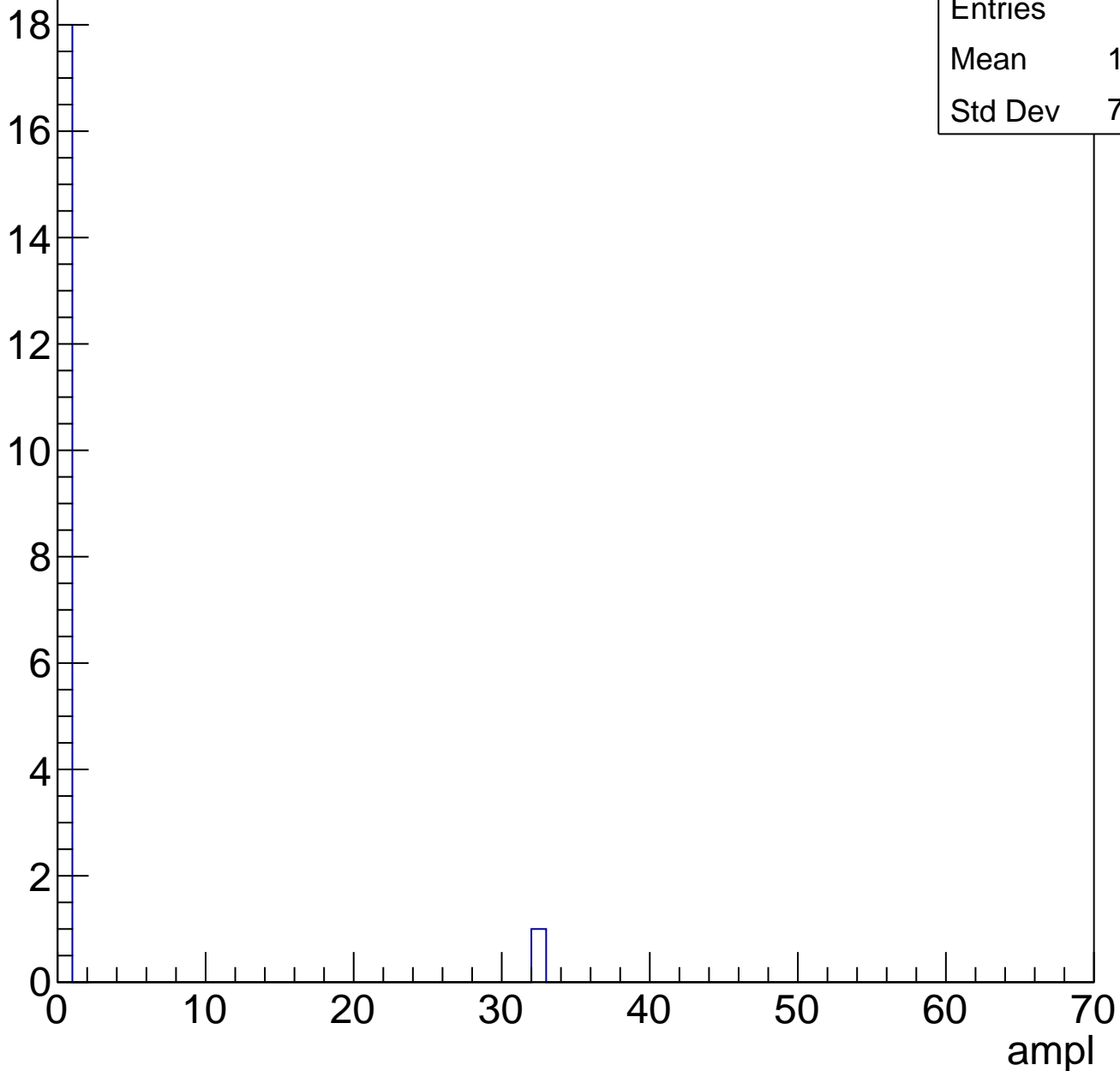


B1L103S, U12-ch16, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.684
Std Dev	7.146

Entry

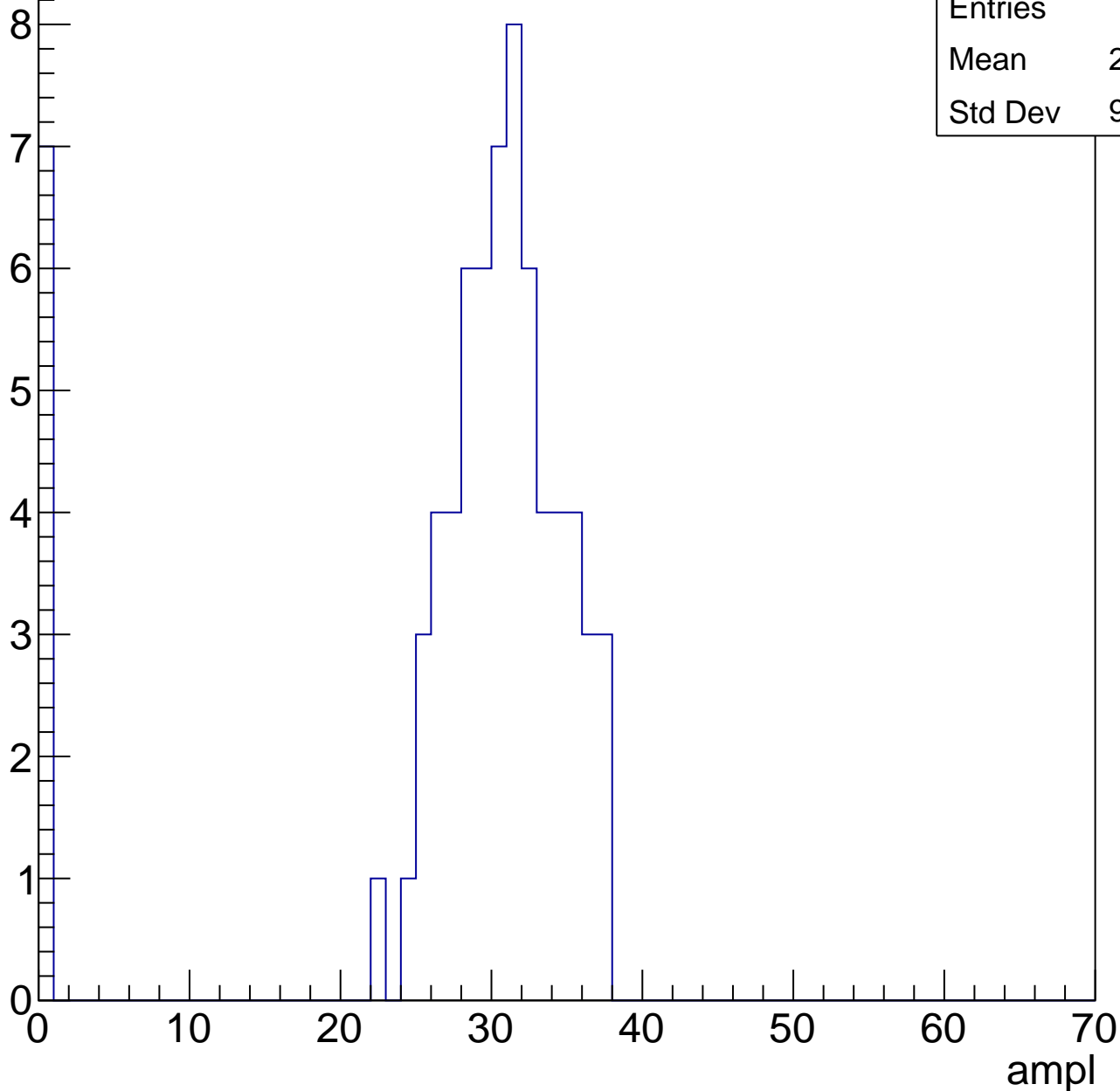


B1L103S, U12-ch17, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	27.49
Std Dev	9.675

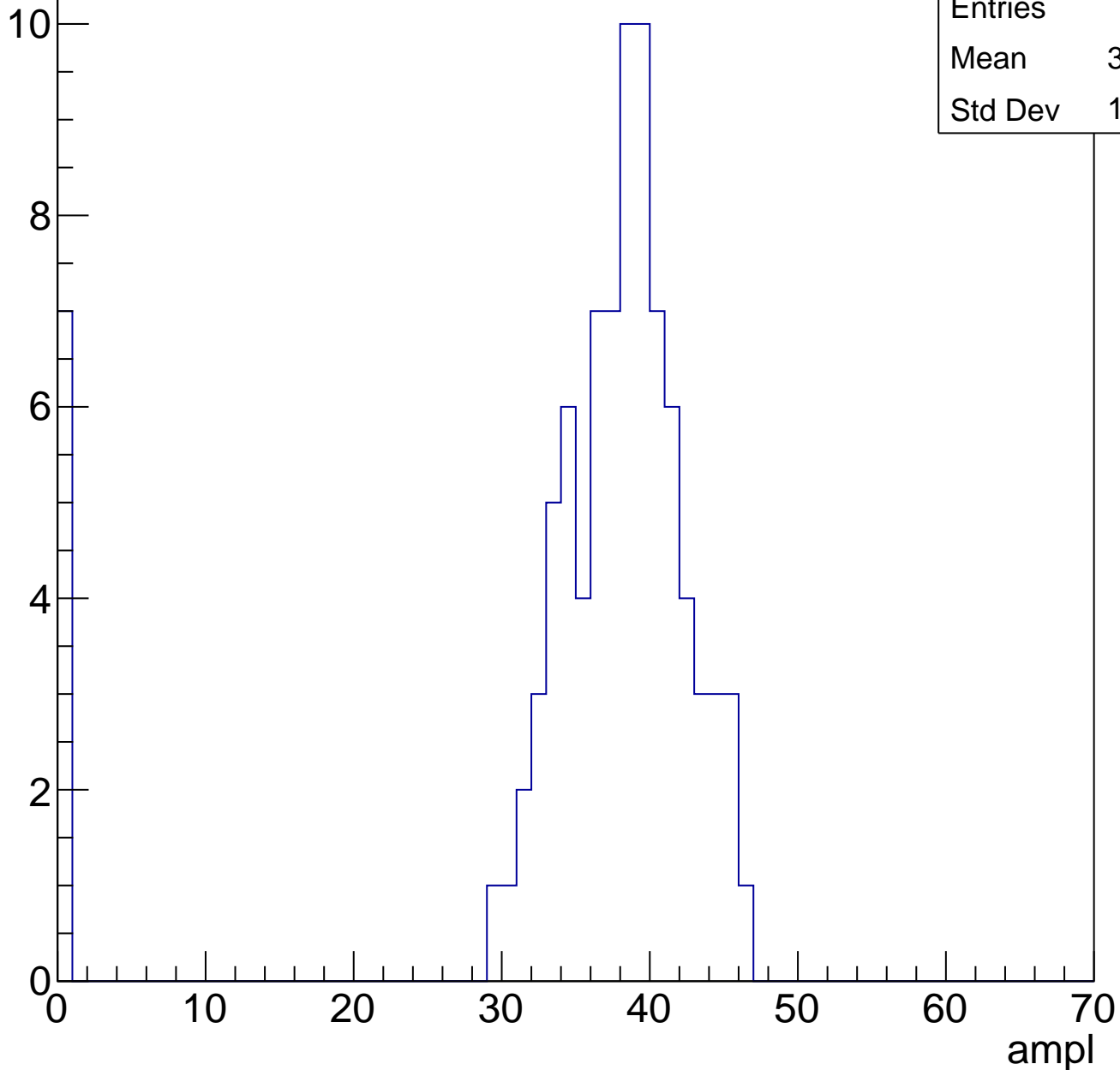


B1L103S, U12-ch17, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	90
Mean	34.92
Std Dev	10.77

Entry

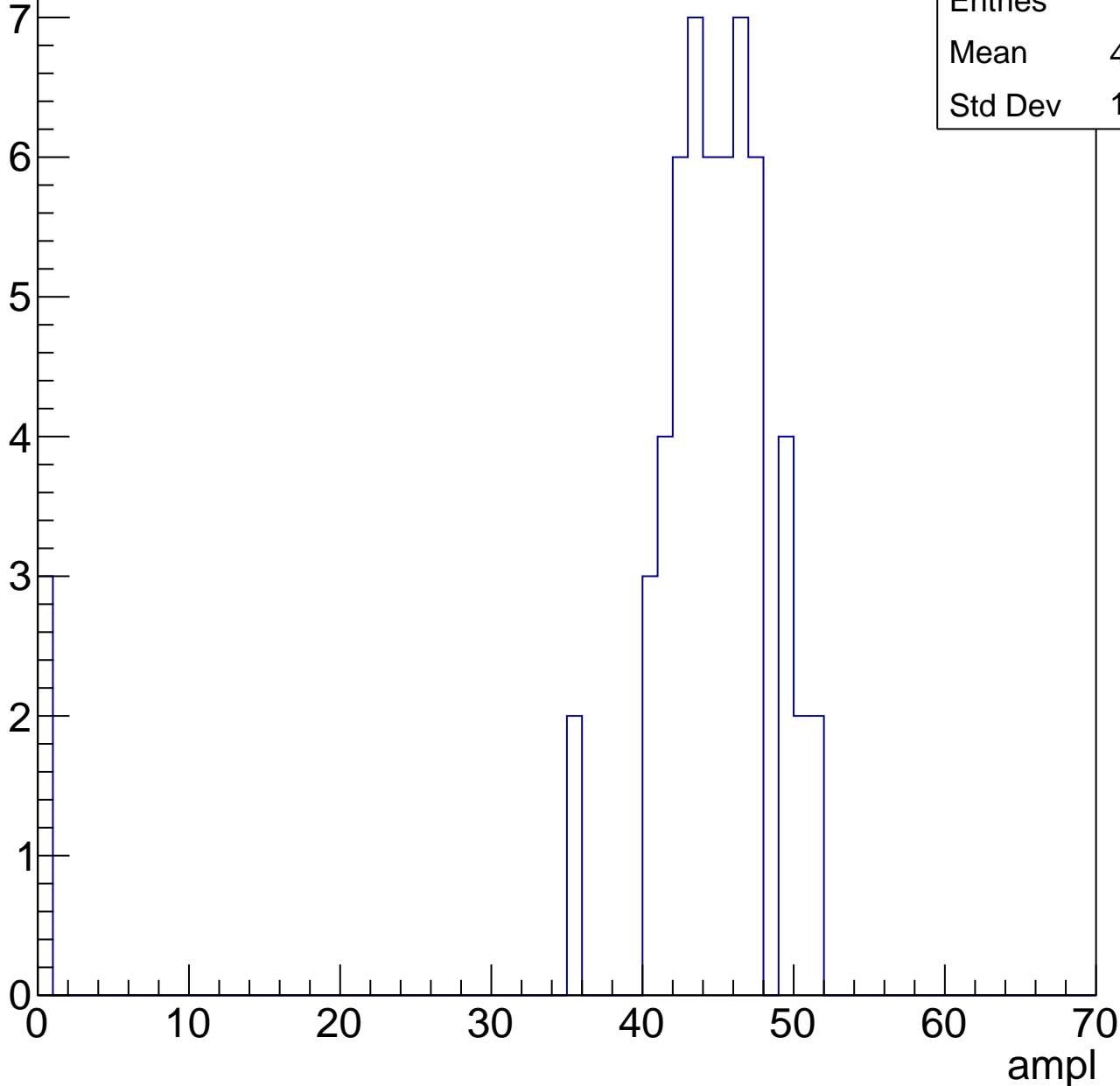


B1L103S, U12-ch17, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	42.12
Std Dev	10.37



B1L103S, U12-ch17, adc3

calib_packv5_041523_1651.root, FC#0, port C2

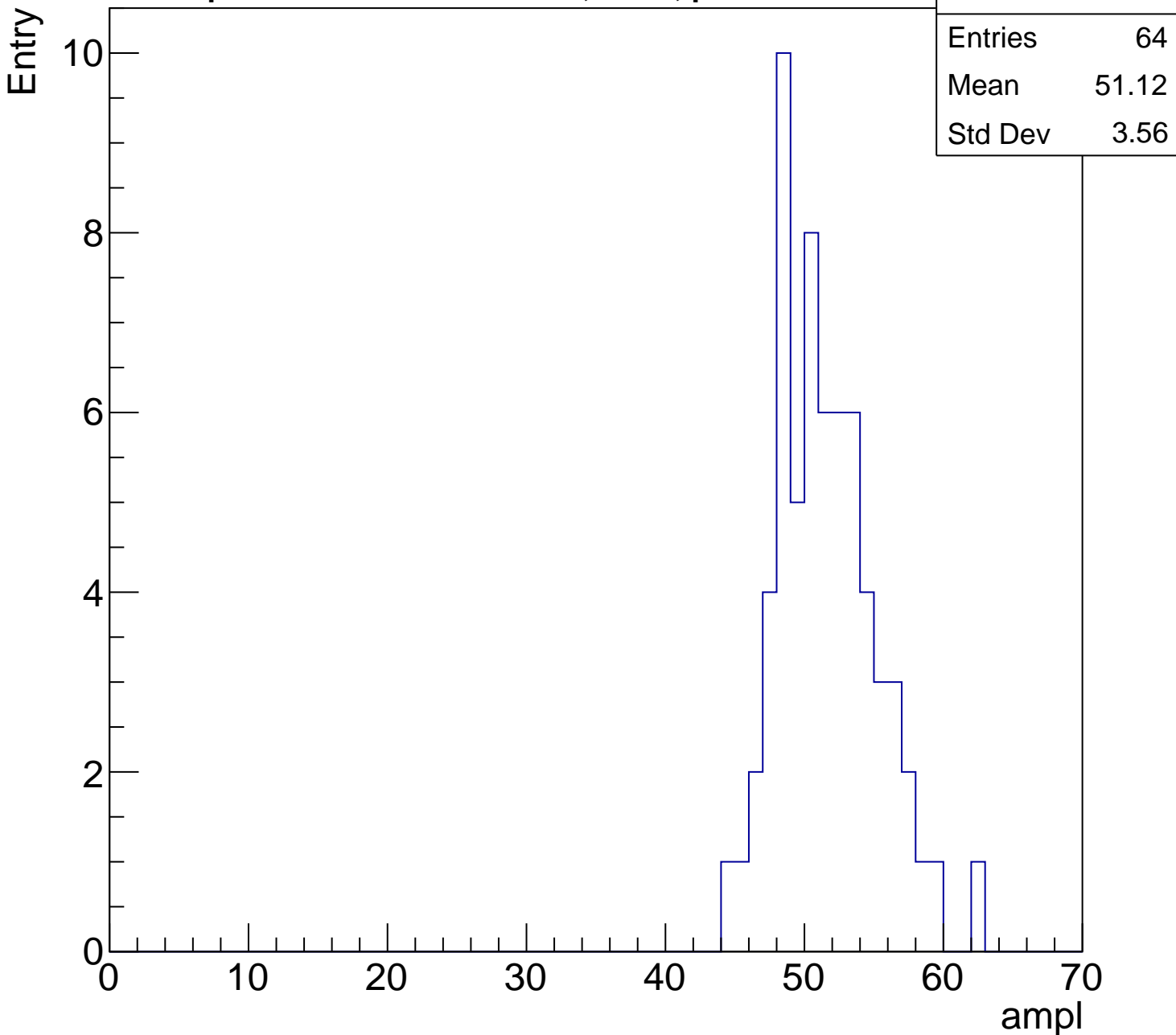
Entries	64
Mean	51.12
Std Dev	3.56

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

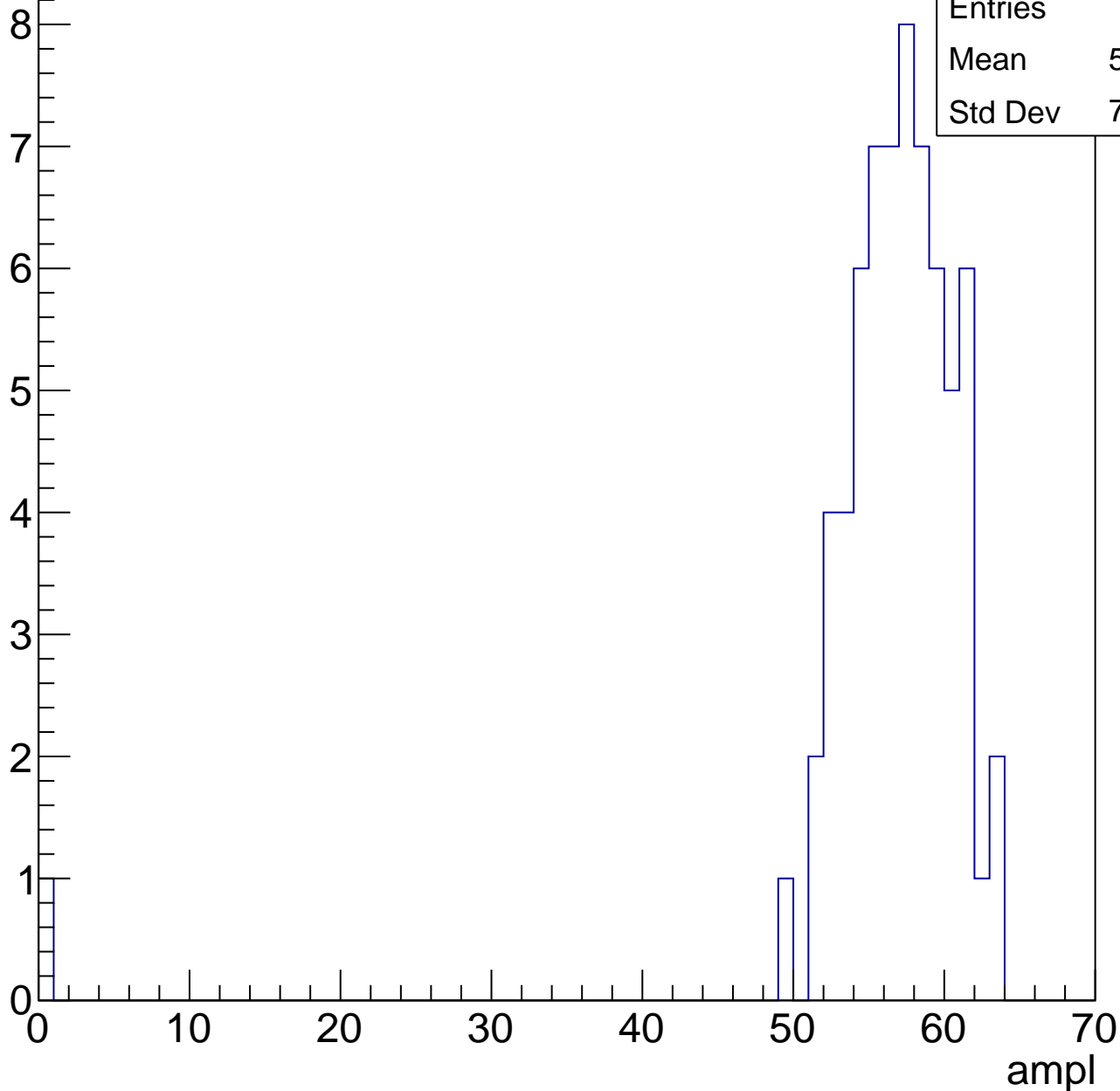


B1L103S, U12-ch17, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	55.85
Std Dev	7.549

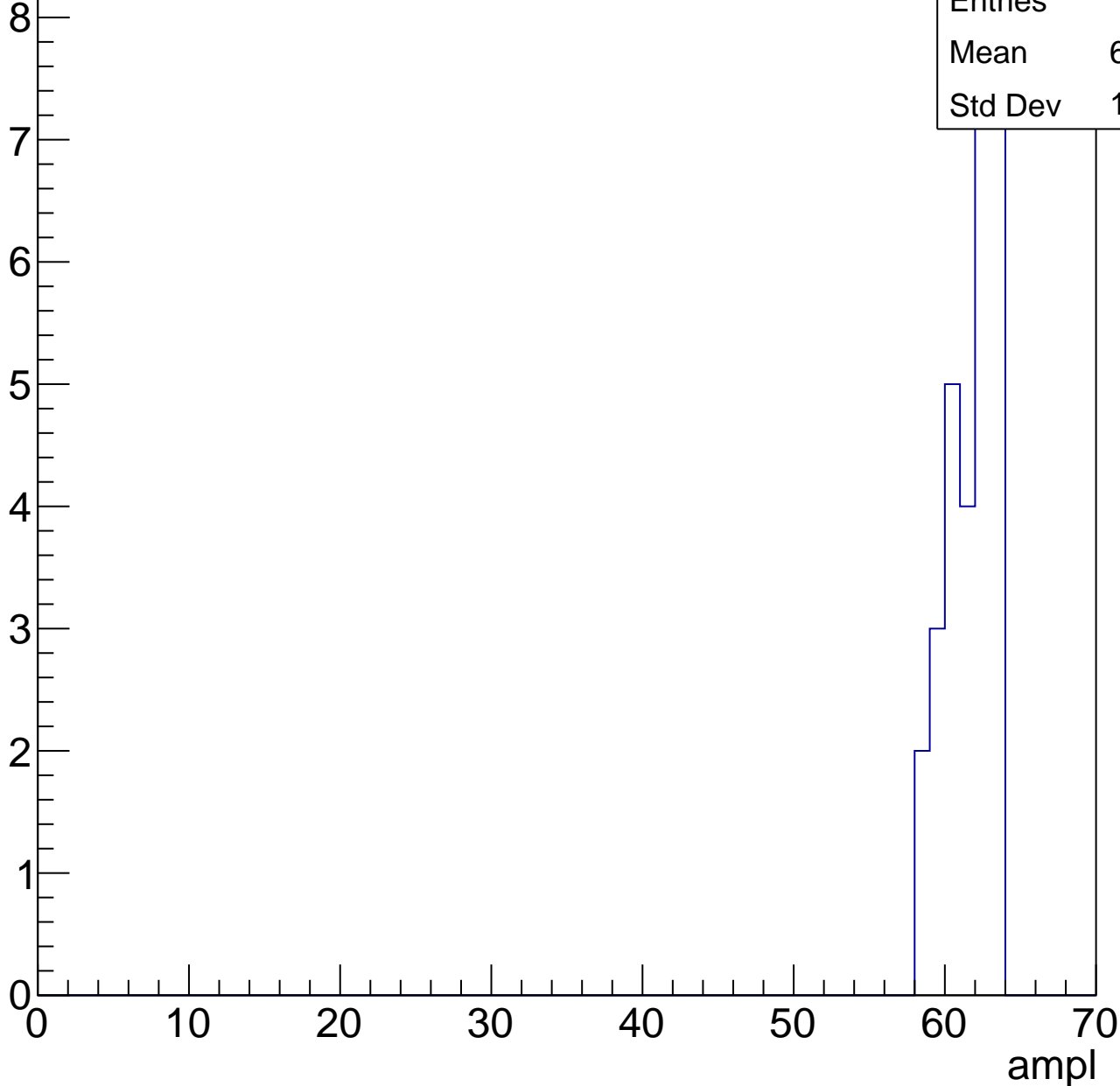


B1L103S, U12-ch17, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	30
Mean	61.23
Std Dev	1.564



B1L103S, U12-ch17, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	0
Mean	0
Std Dev	0

B1L103S, U12-ch17, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

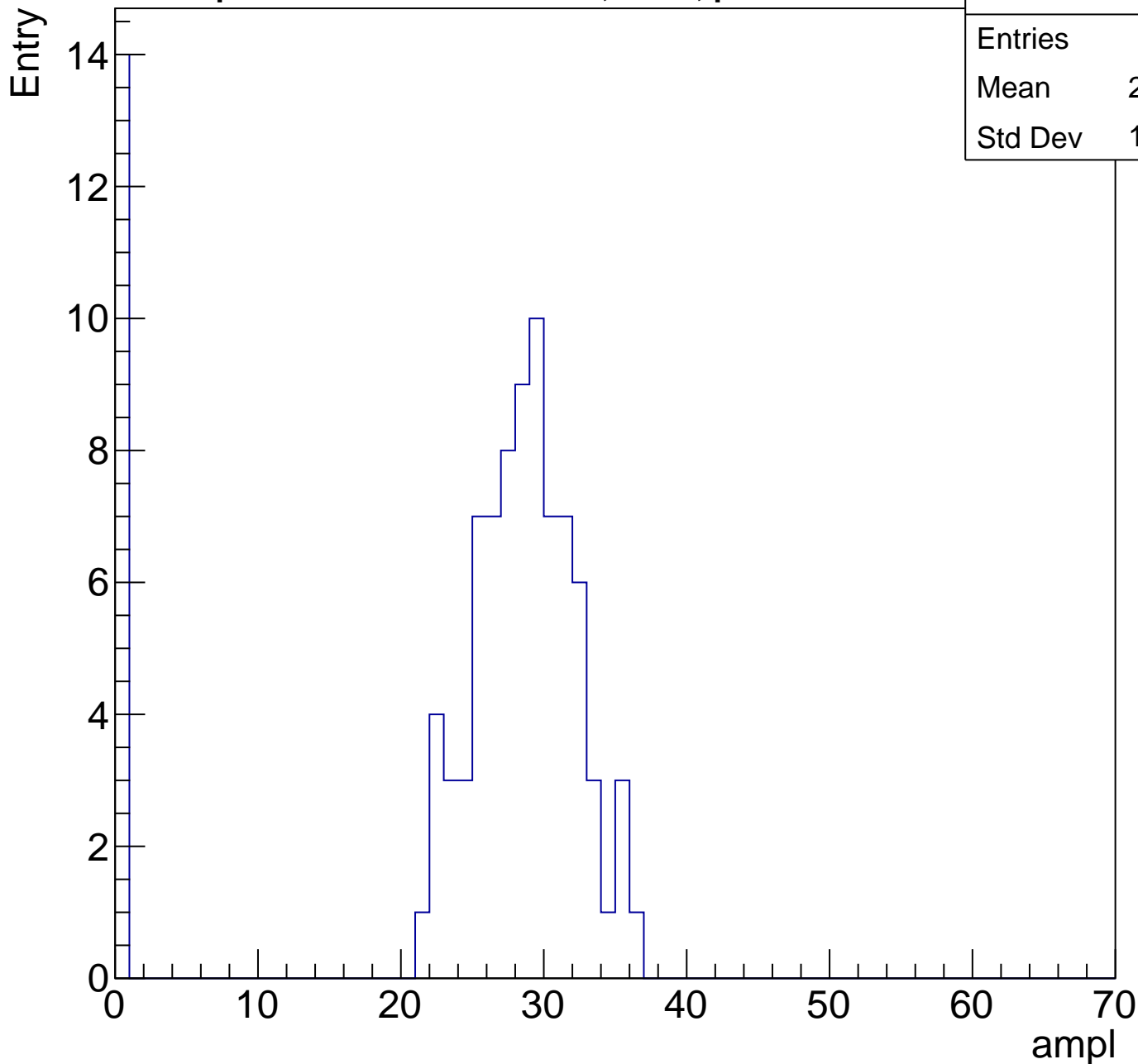
ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U12-ch18, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	94
Mean	24.02
Std Dev	10.53



B1L103S, U12-ch18, adc1

calib_packv5_041523_1651.root, FC#0, port C2

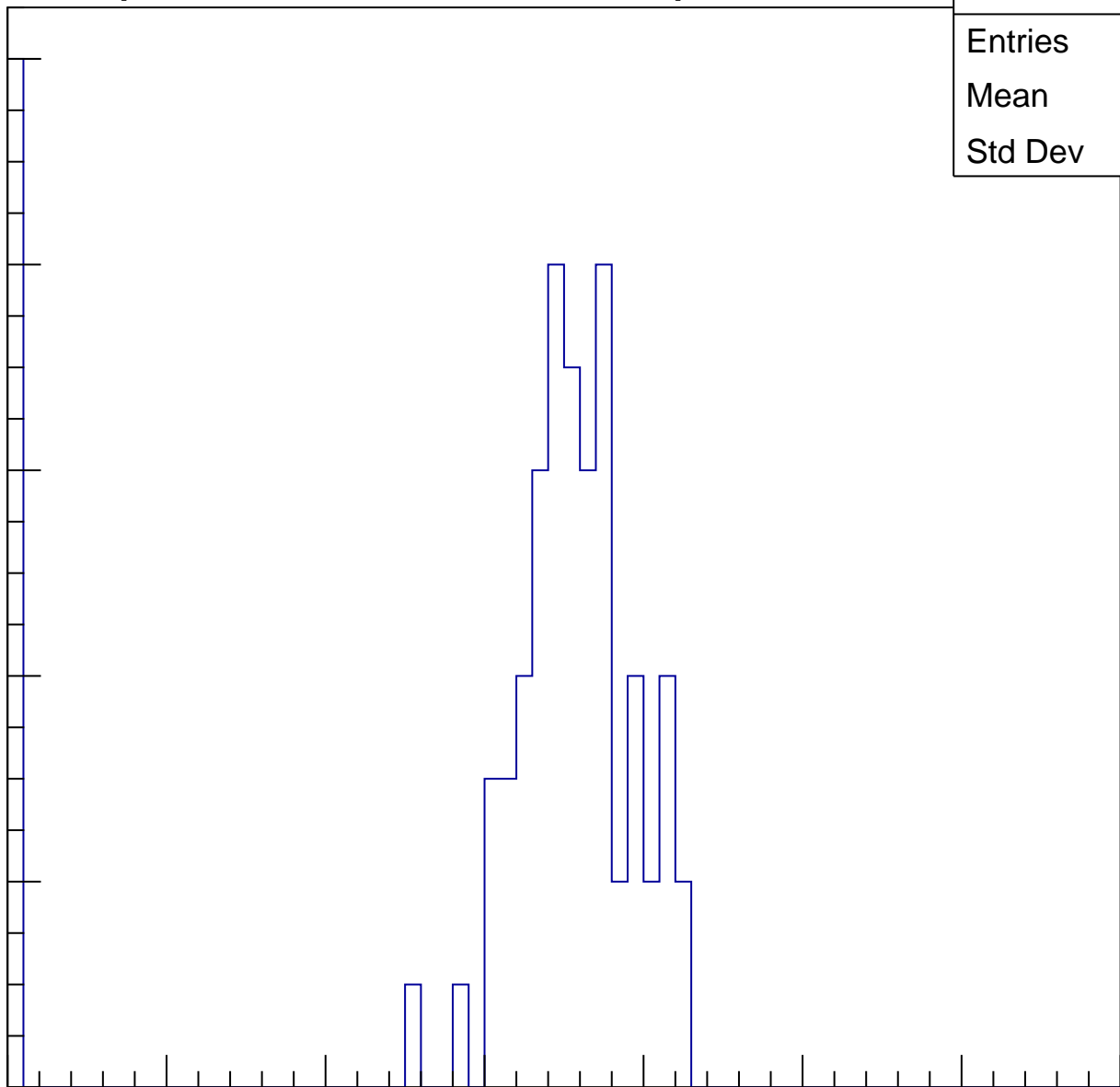
Entries	71
Mean	30.3
Std Dev	12.69

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

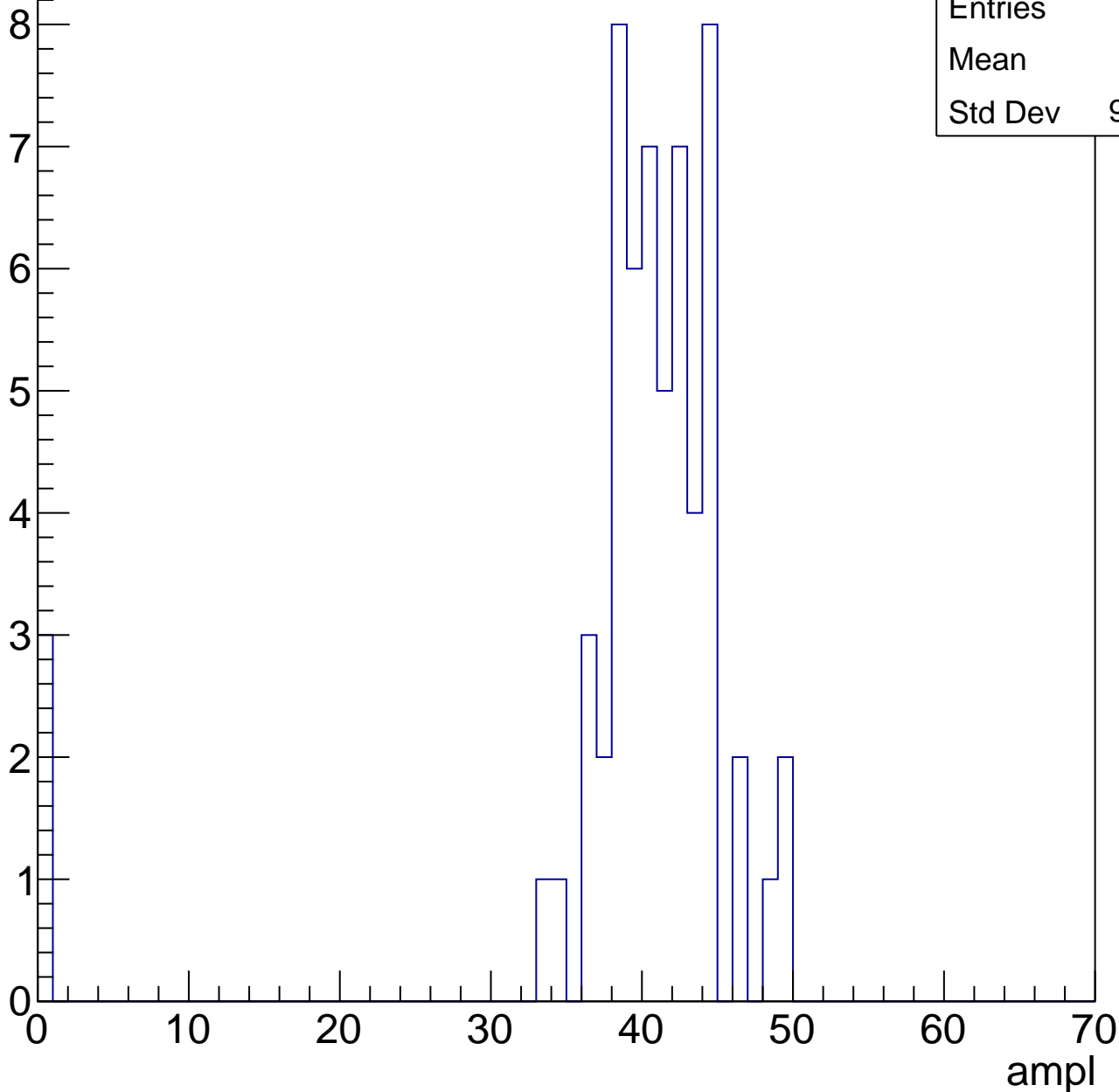


B1L103S, U12-ch18, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	38.8
Std Dev	9.485

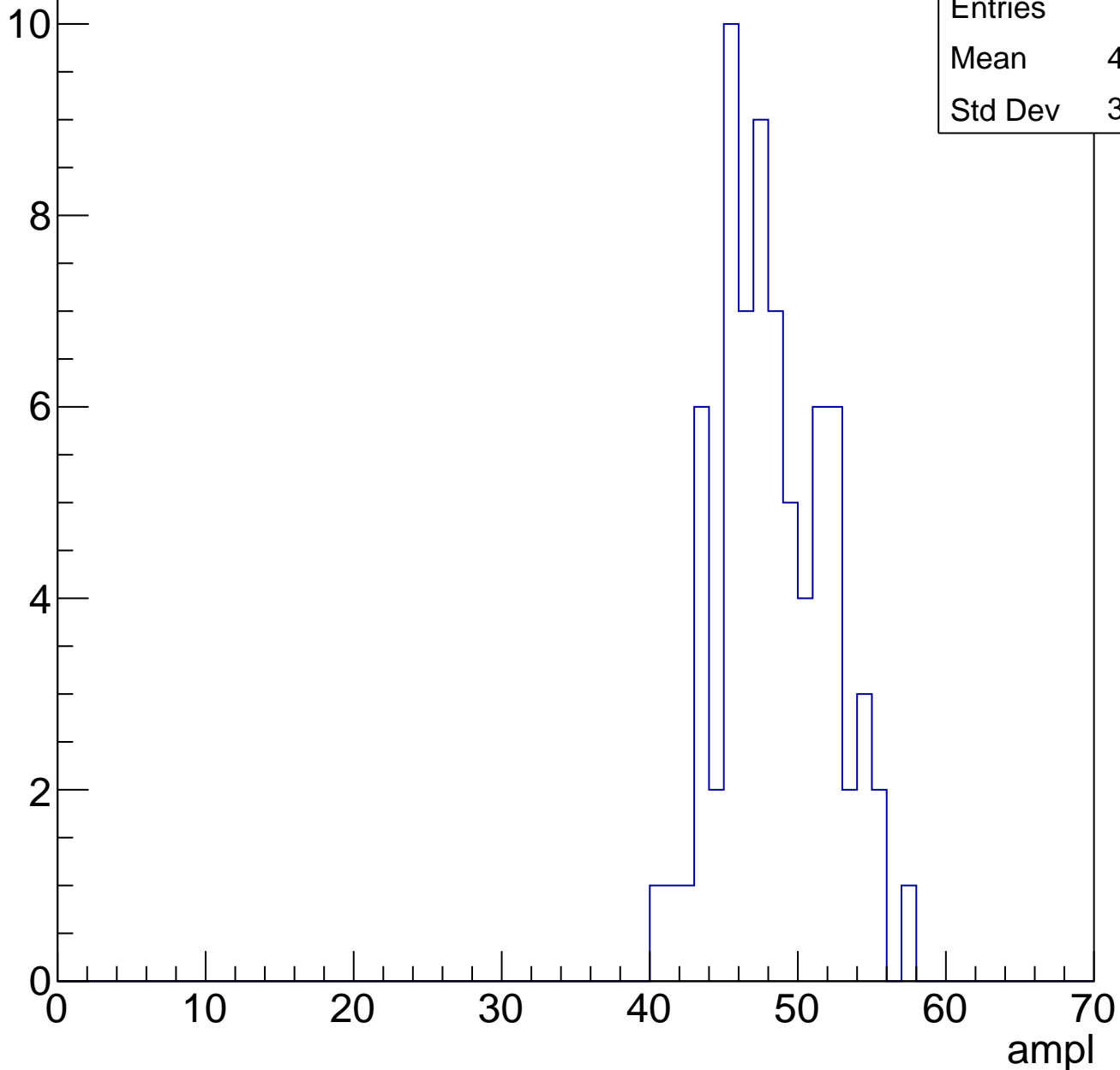


B1L103S, U12-ch18, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	73
Mean	47.92
Std Dev	3.637

Entry

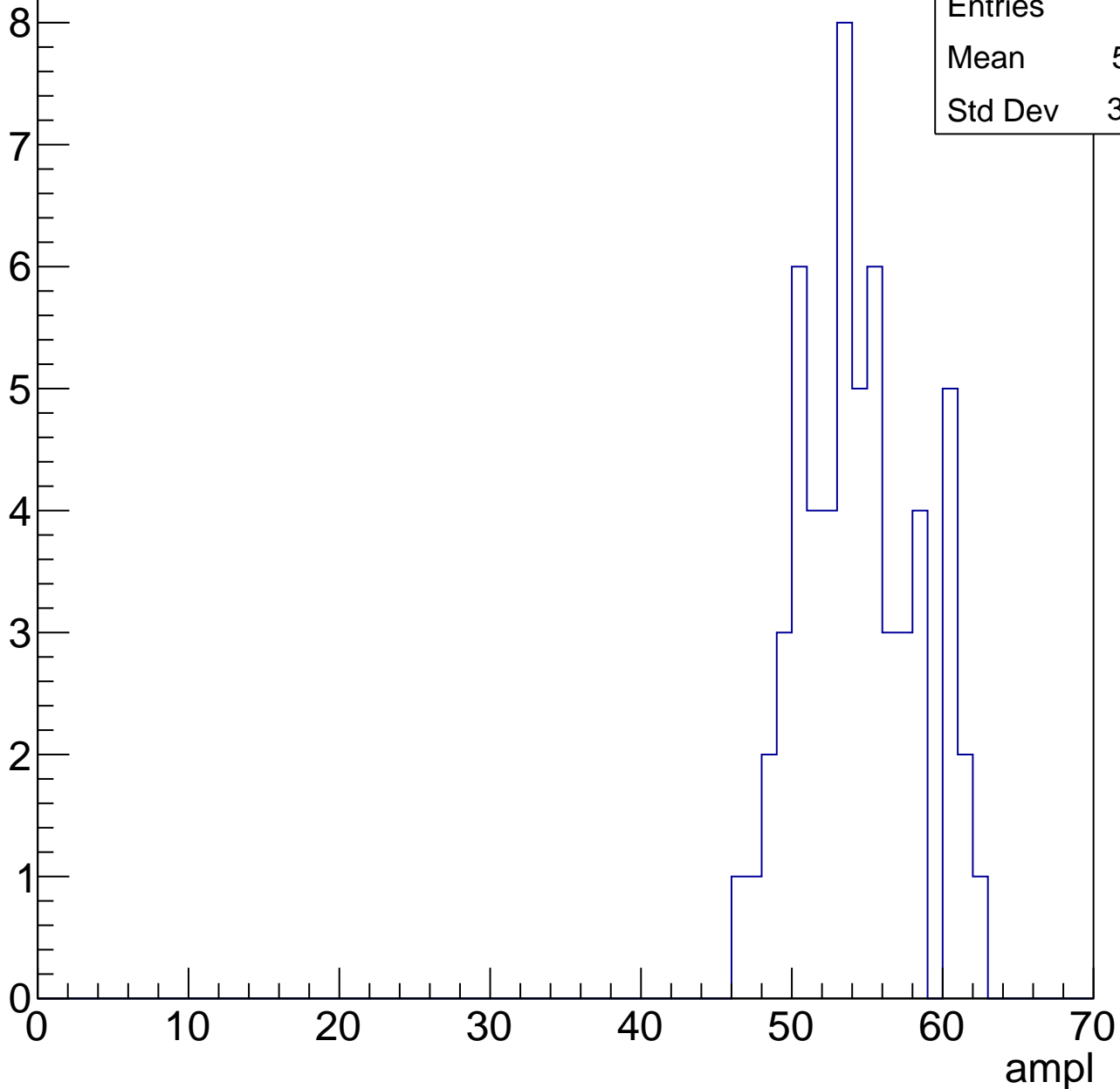


B1L103S, U12-ch18, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

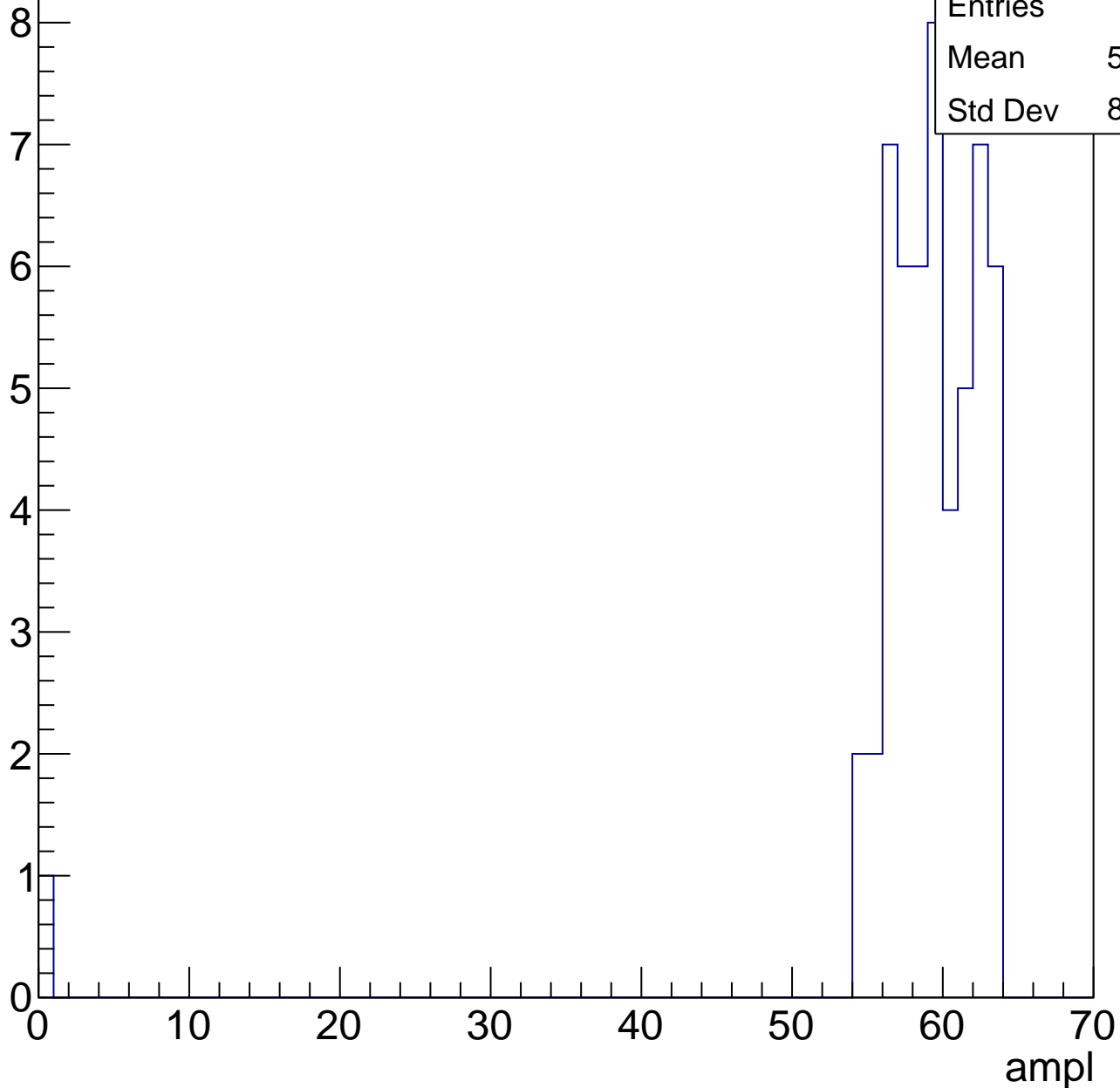
Entries	58
Mean	53.91
Std Dev	3.865



B1L103S, U12-ch18, adc5

calib_packv5_041523_1651.root, FC#0, port C2

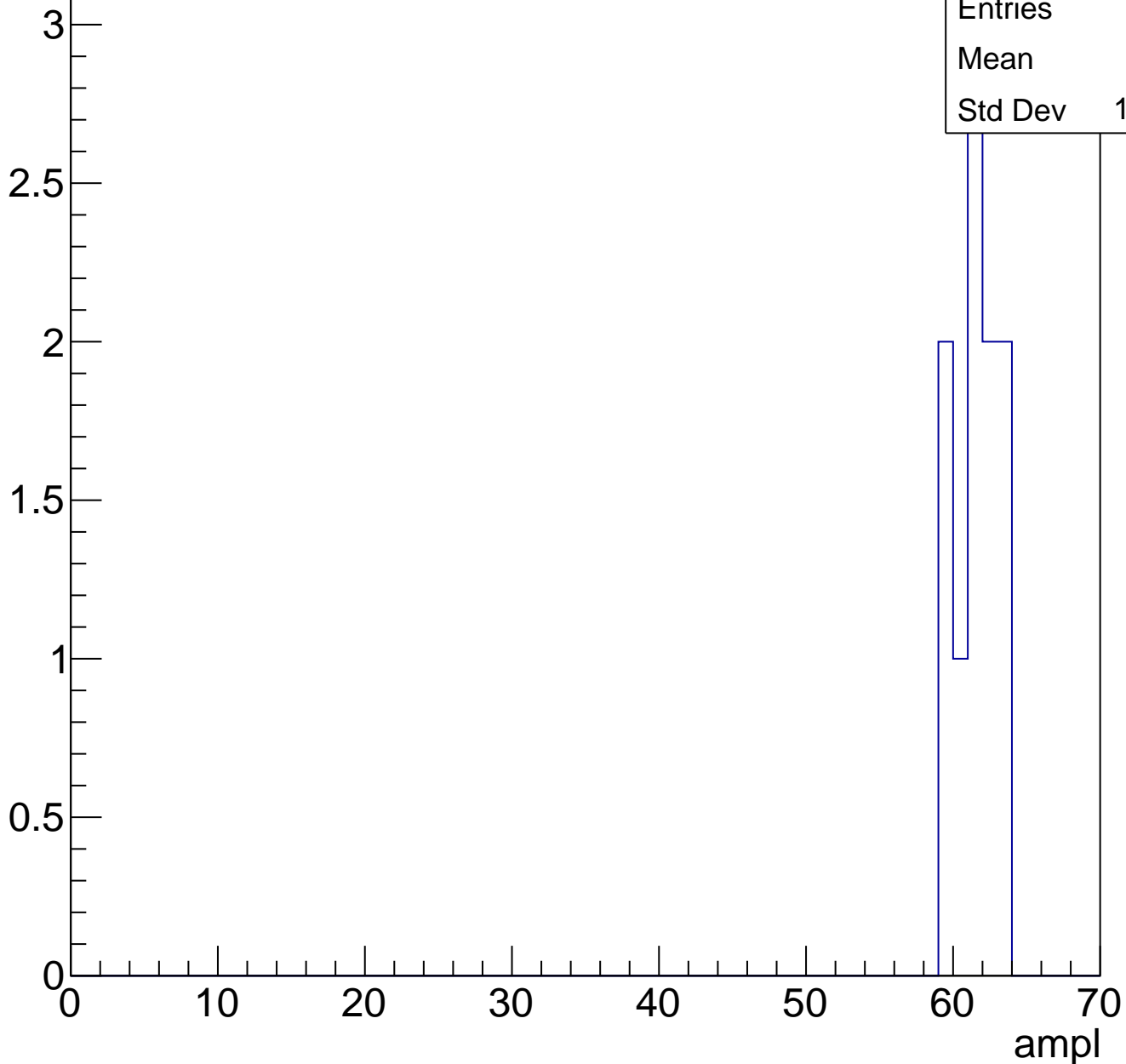
Entry



B1L103S, U12-ch18, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch18, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	7.25
Std Dev	19.04

Entry

16

14

12

10

8

6

4

2

0

0

10

20

30

40

50

60

ampl

70

B1L103S, U12-ch19, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	89
Mean	26.72
Std Dev	10.61

Entry

10

8

6

4

2

0

ampl

0

10

20

30

40

50

60

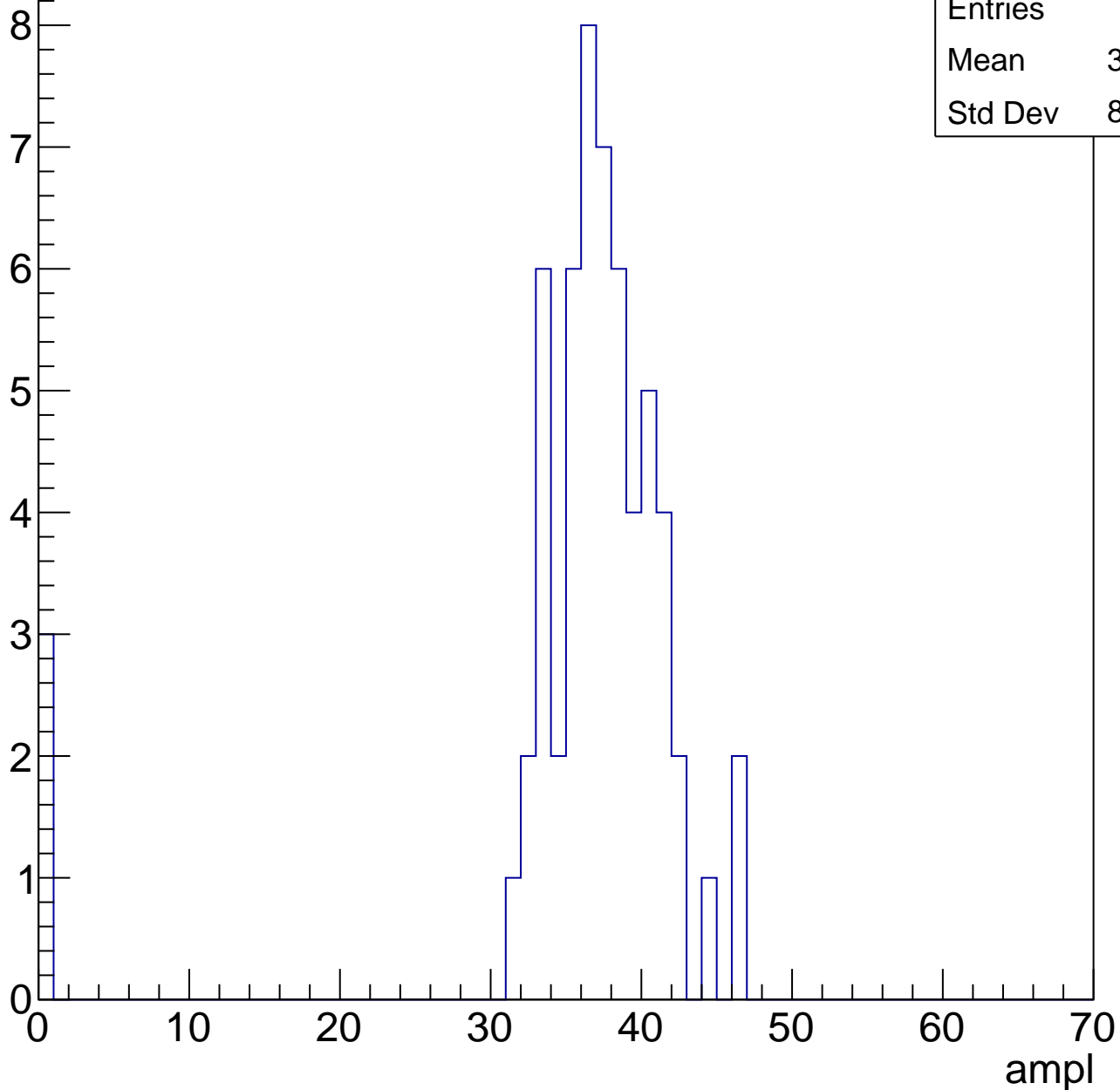
70

B1L103S, U12-ch19, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	35.36
Std Dev	8.802

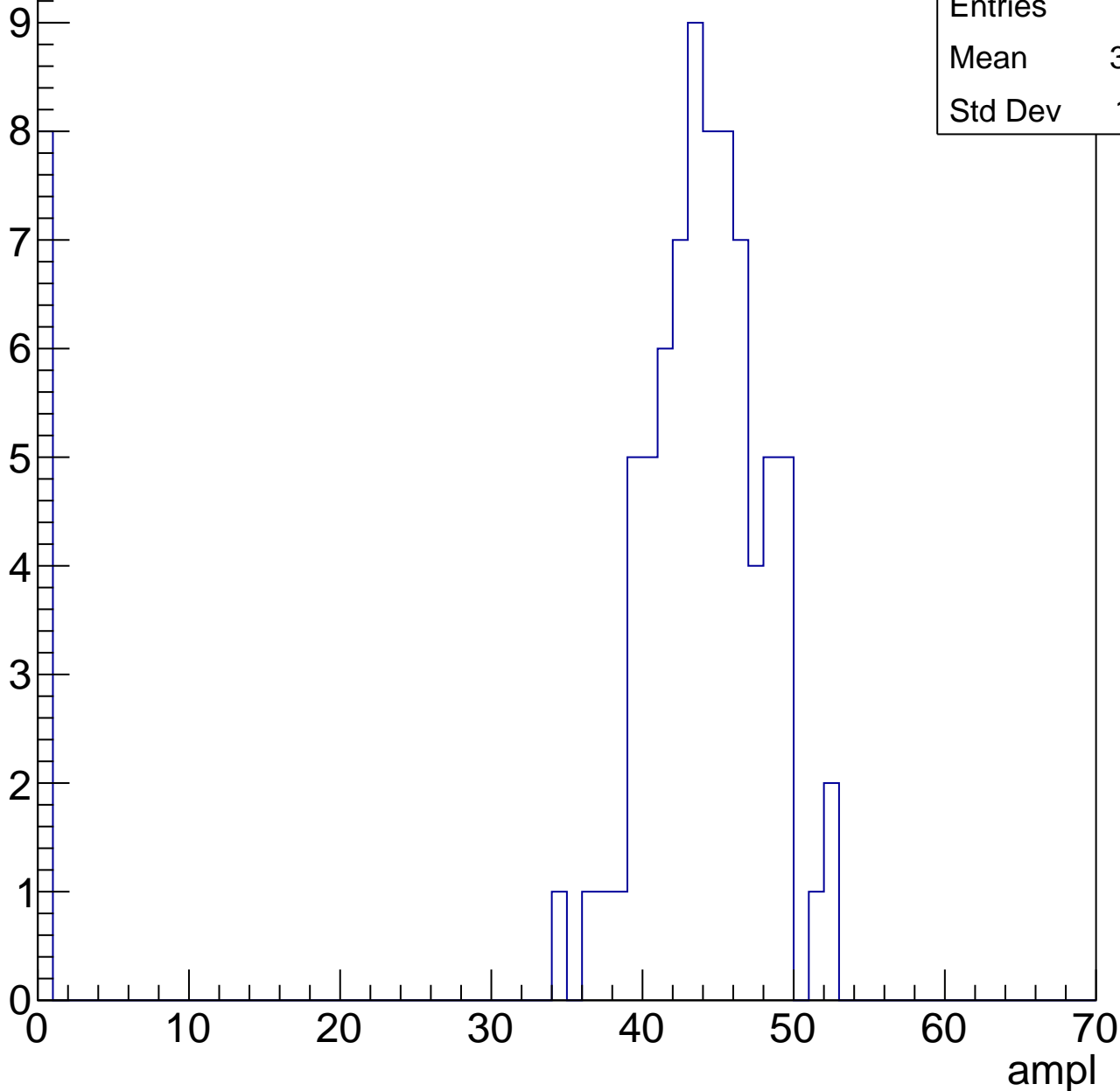


B1L103S, U12-ch19, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	84
Mean	39.63
Std Dev	13.31

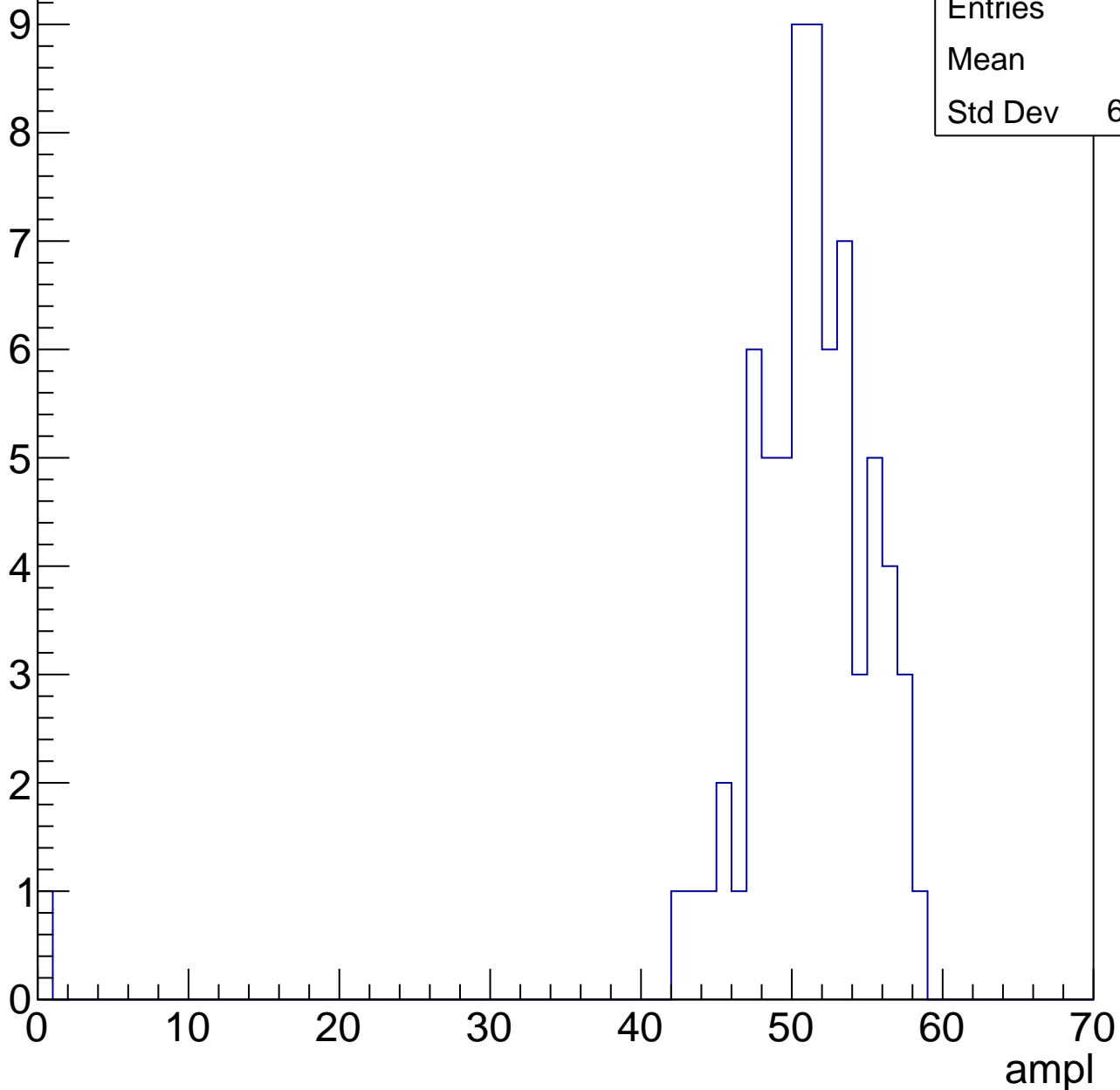


B1L103S, U12-ch19, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	50.2
Std Dev	6.985

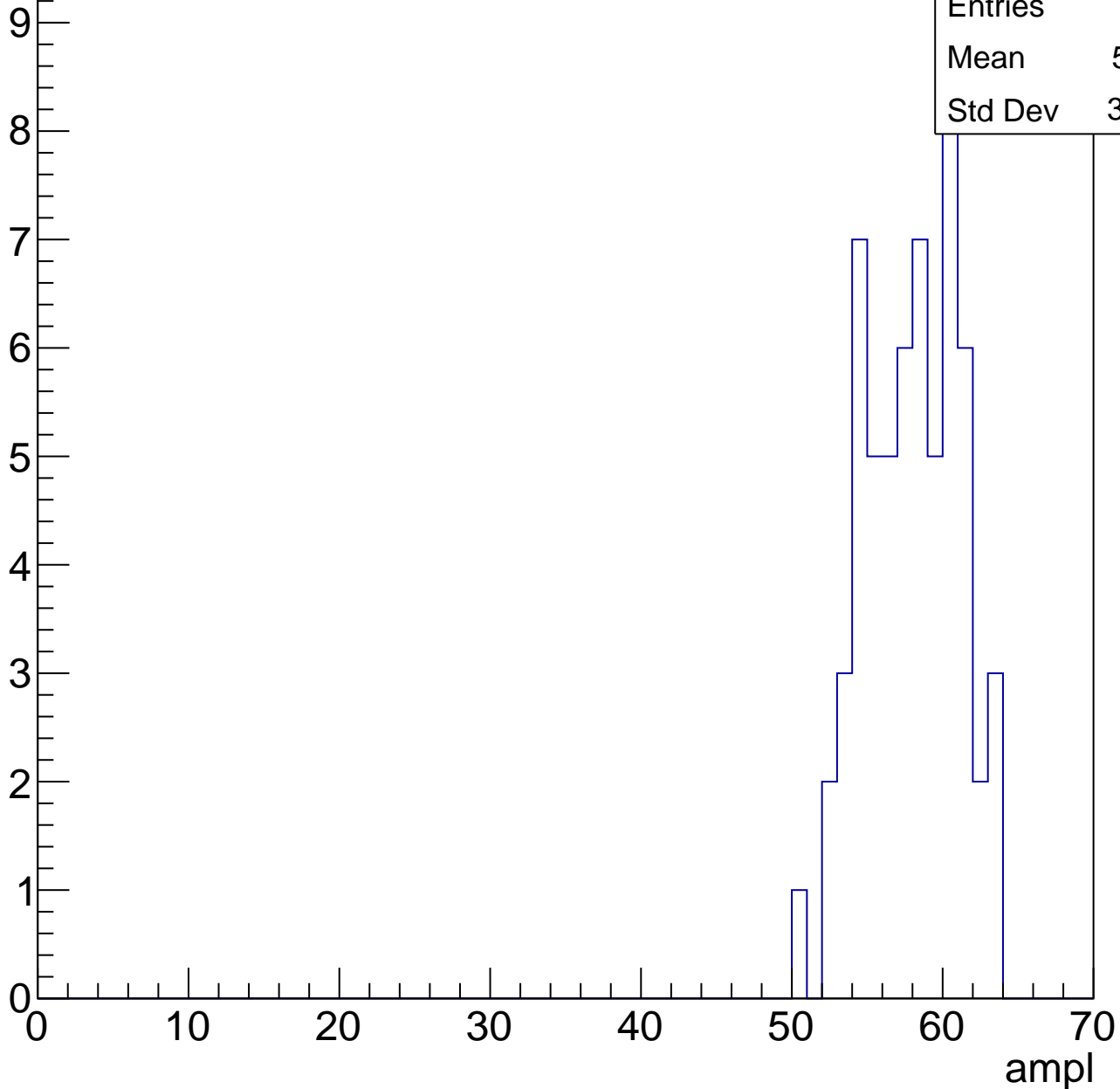


B1L103S, U12-ch19, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	57.51
Std Dev	3.087

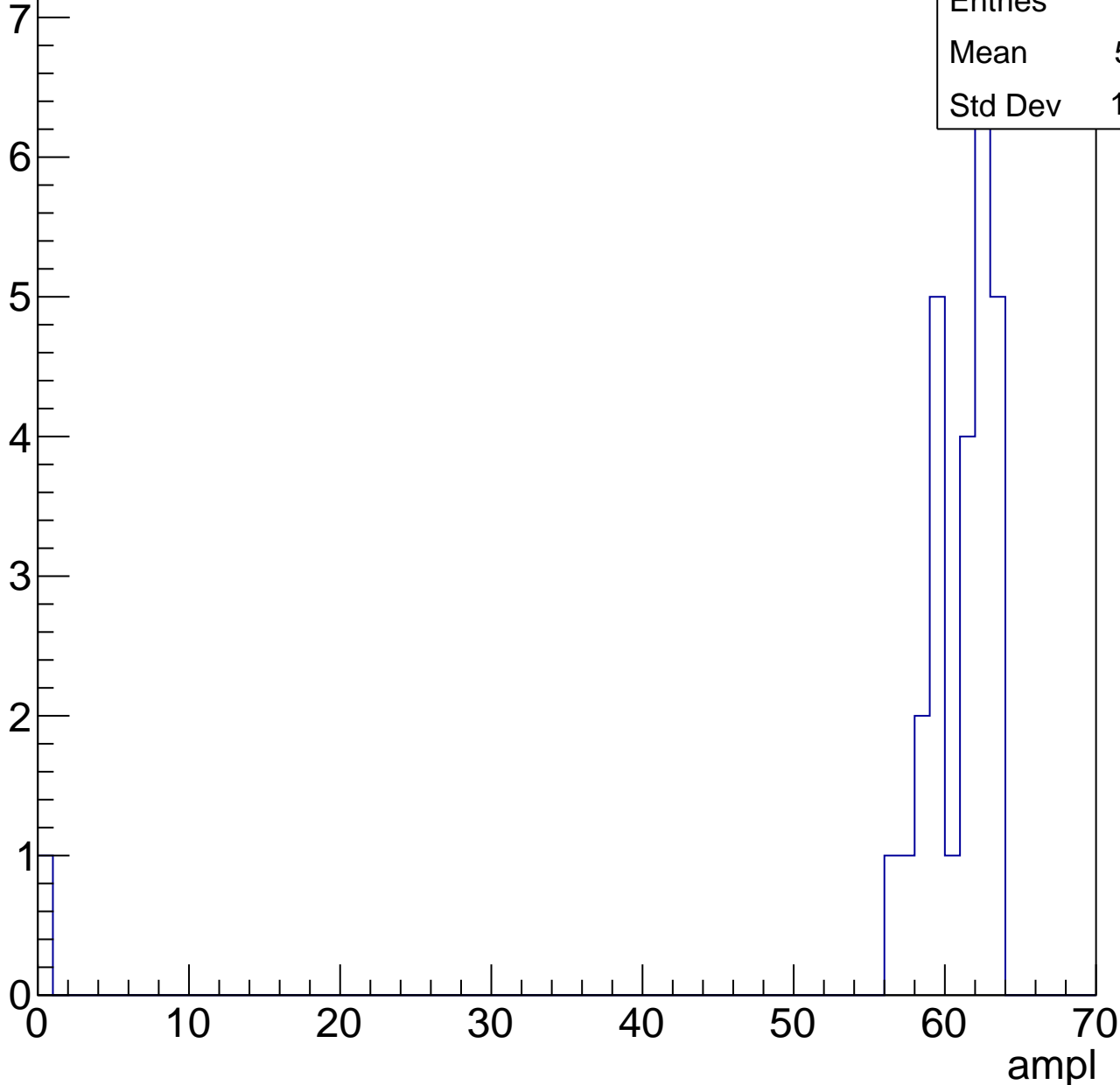


B1L103S, U12-ch19, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	27
Mean	58.41
Std Dev	11.62



B1L103S, U12-ch19, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch19, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

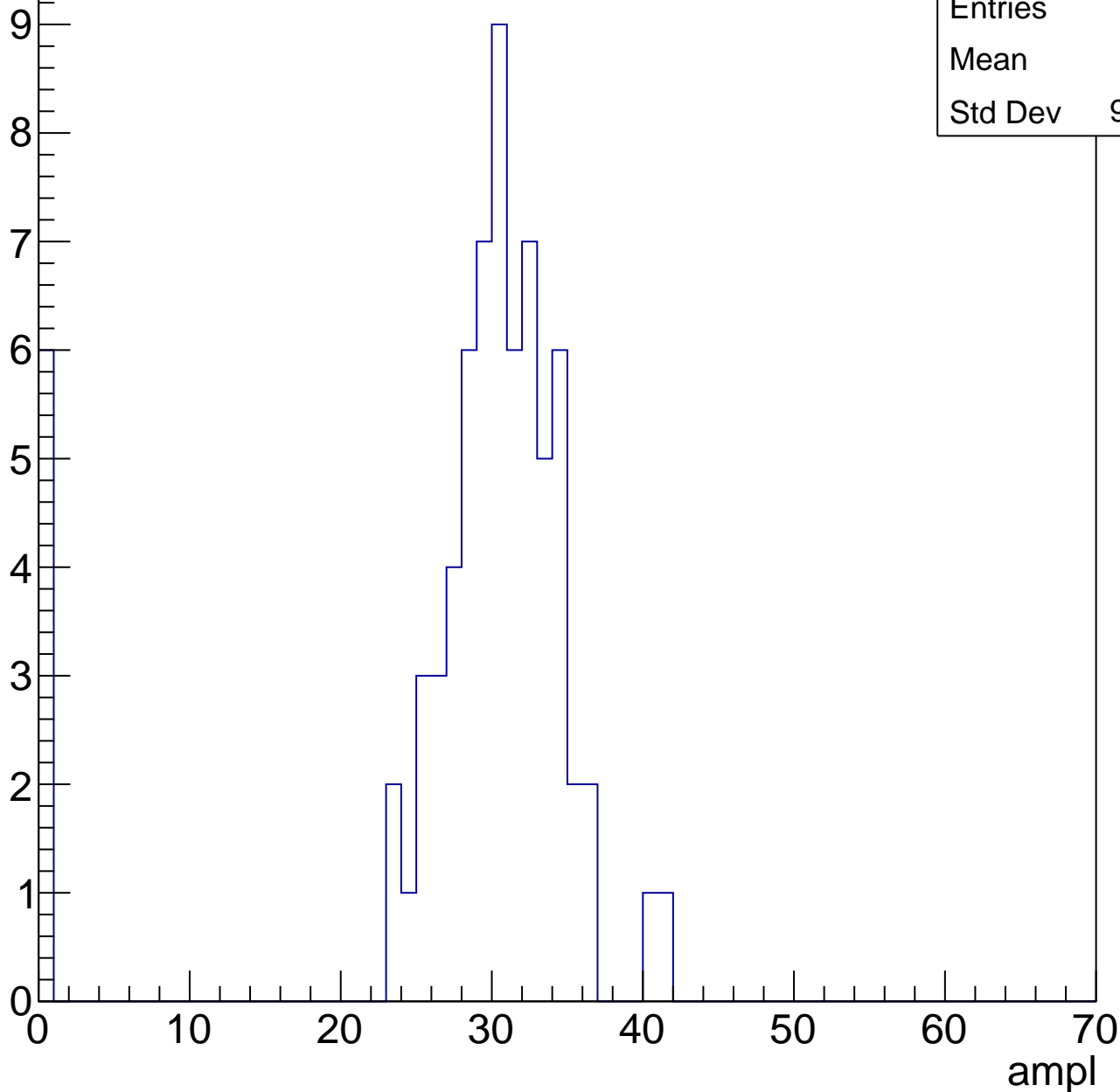
Entries	19
Mean	0
Std Dev	0

B1L103S, U12-ch20, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	27.8
Std Dev	9.115

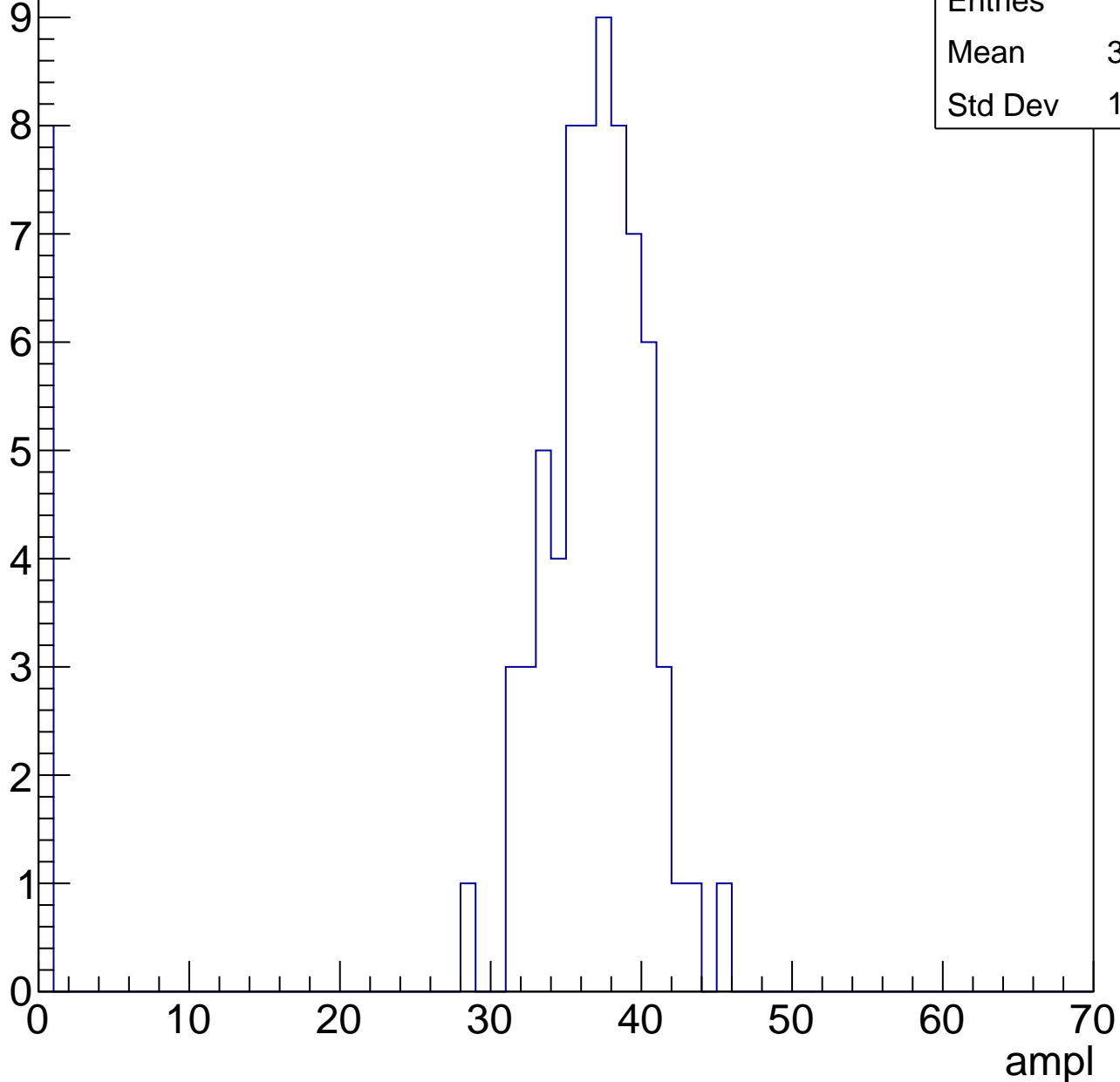


B1L103S, U12-ch20, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	76
Mean	32.75
Std Dev	11.62

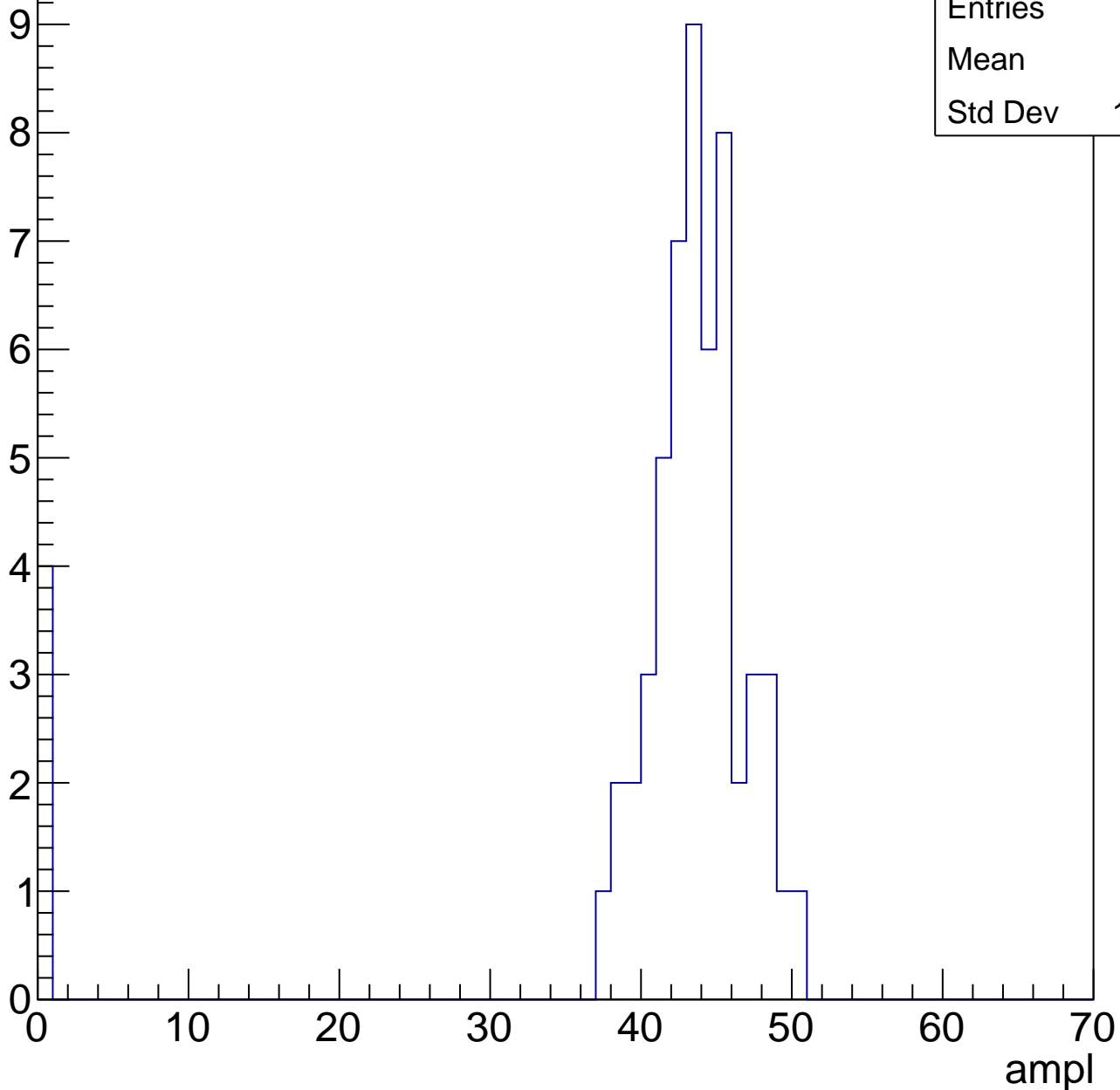


B1L103S, U12-ch20, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	57
Mean	40.3
Std Dev	11.41

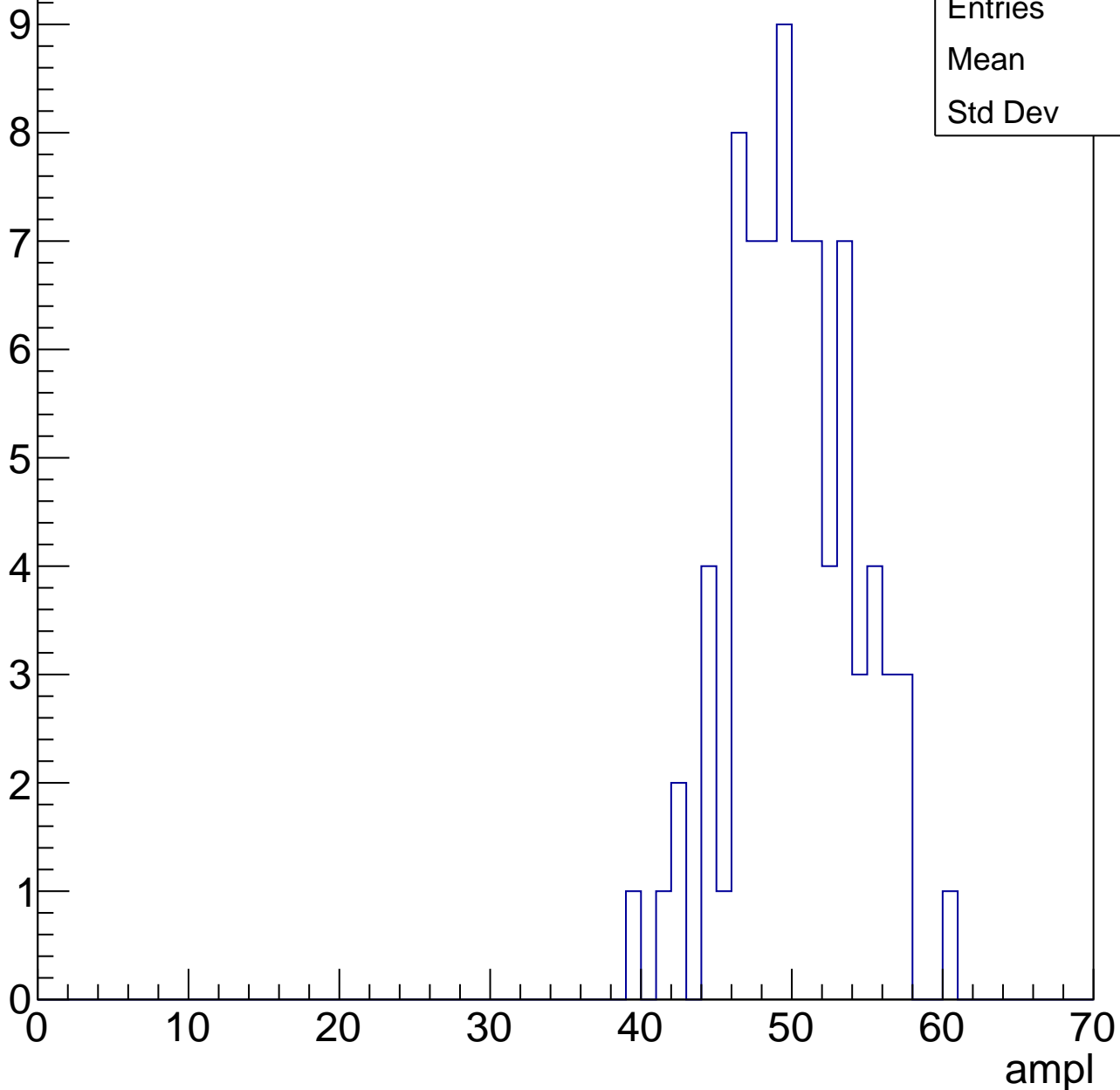


B1L103S, U12-ch20, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	79
Mean	49.7
Std Dev	4.07

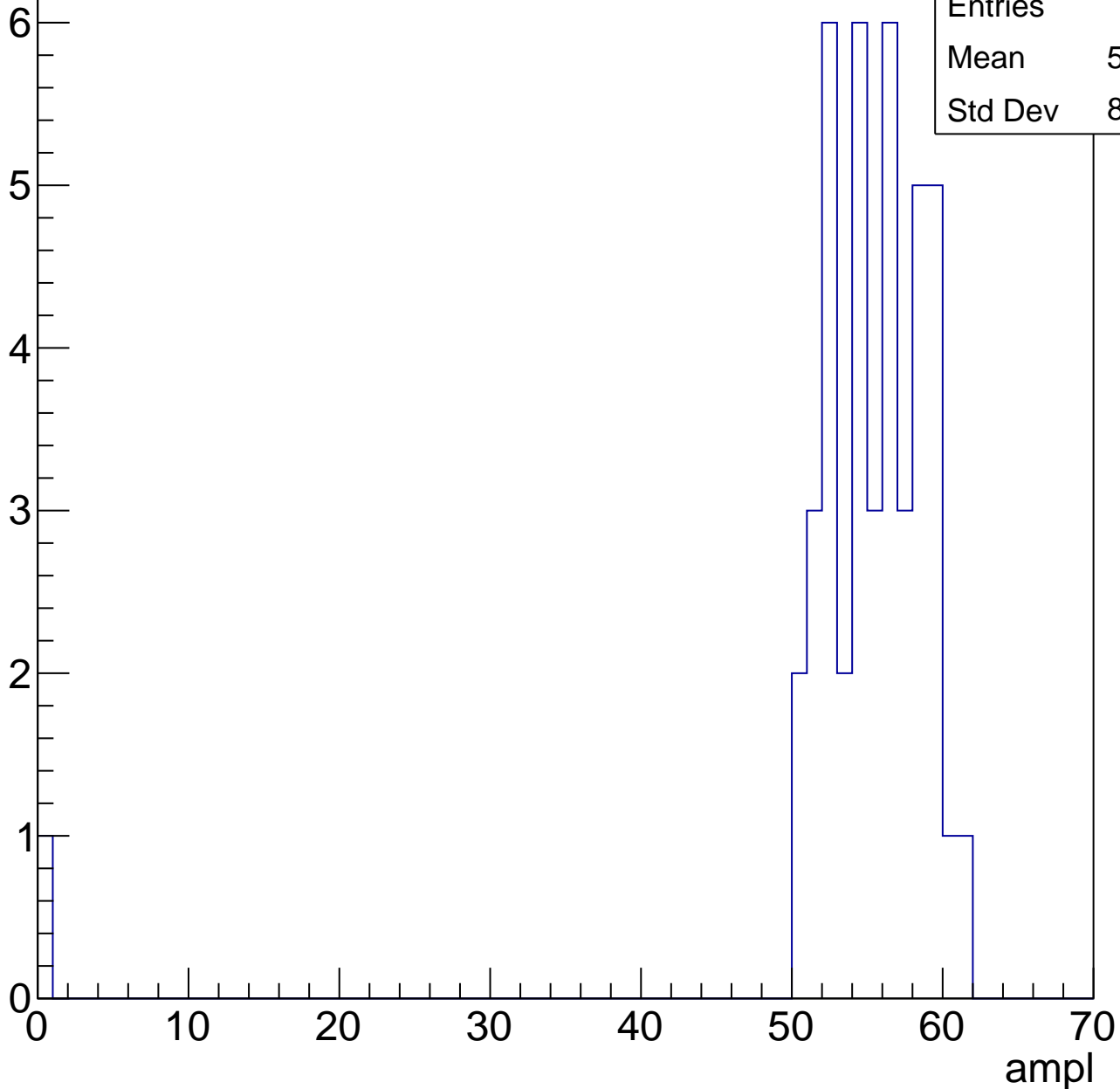


B1L103S, U12-ch20, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

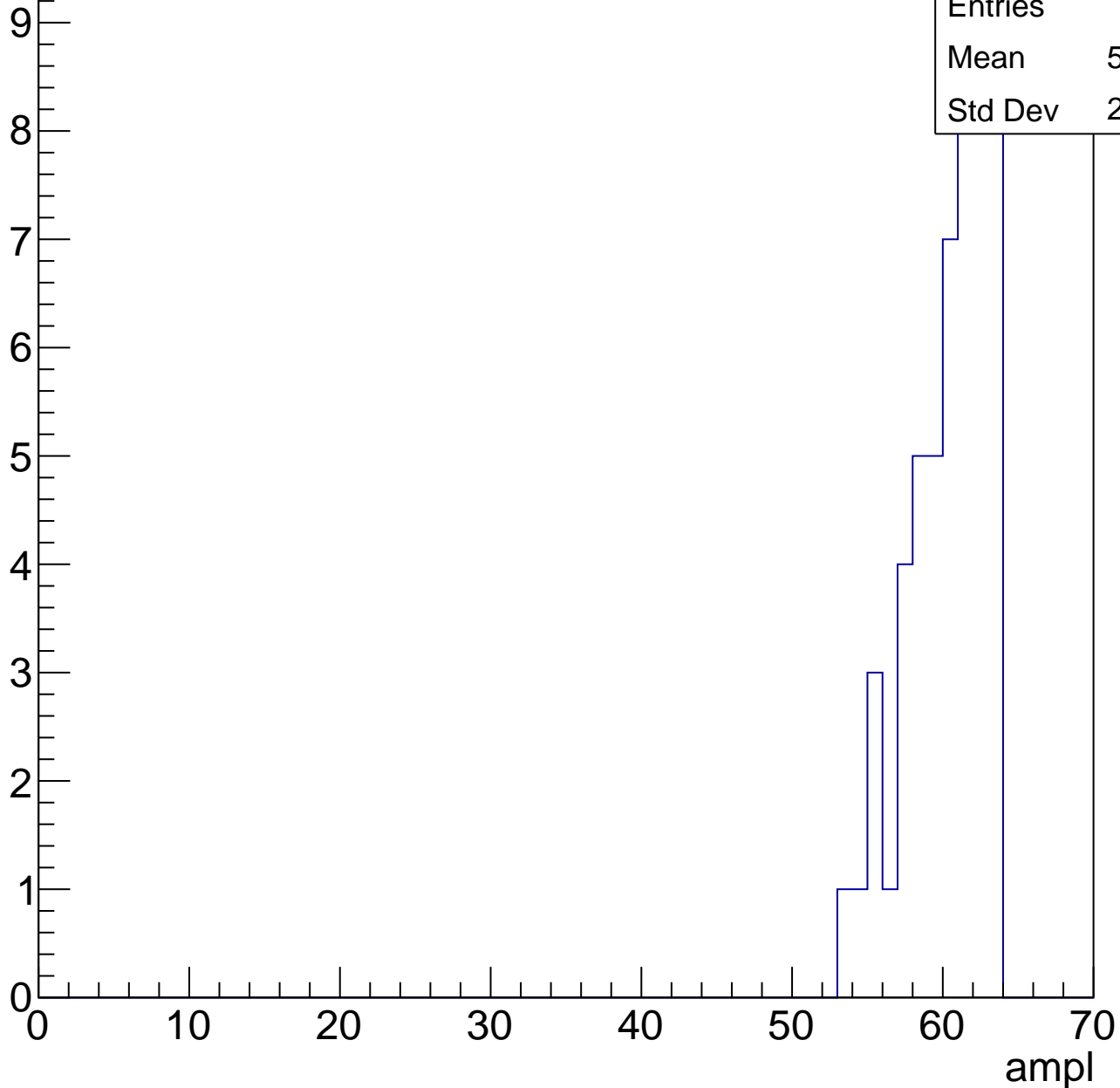
Entries	44
Mean	53.93
Std Dev	8.719



B1L103S, U12-ch20, adc5

calib_packv5_041523_1651.root, FC#0, port C2

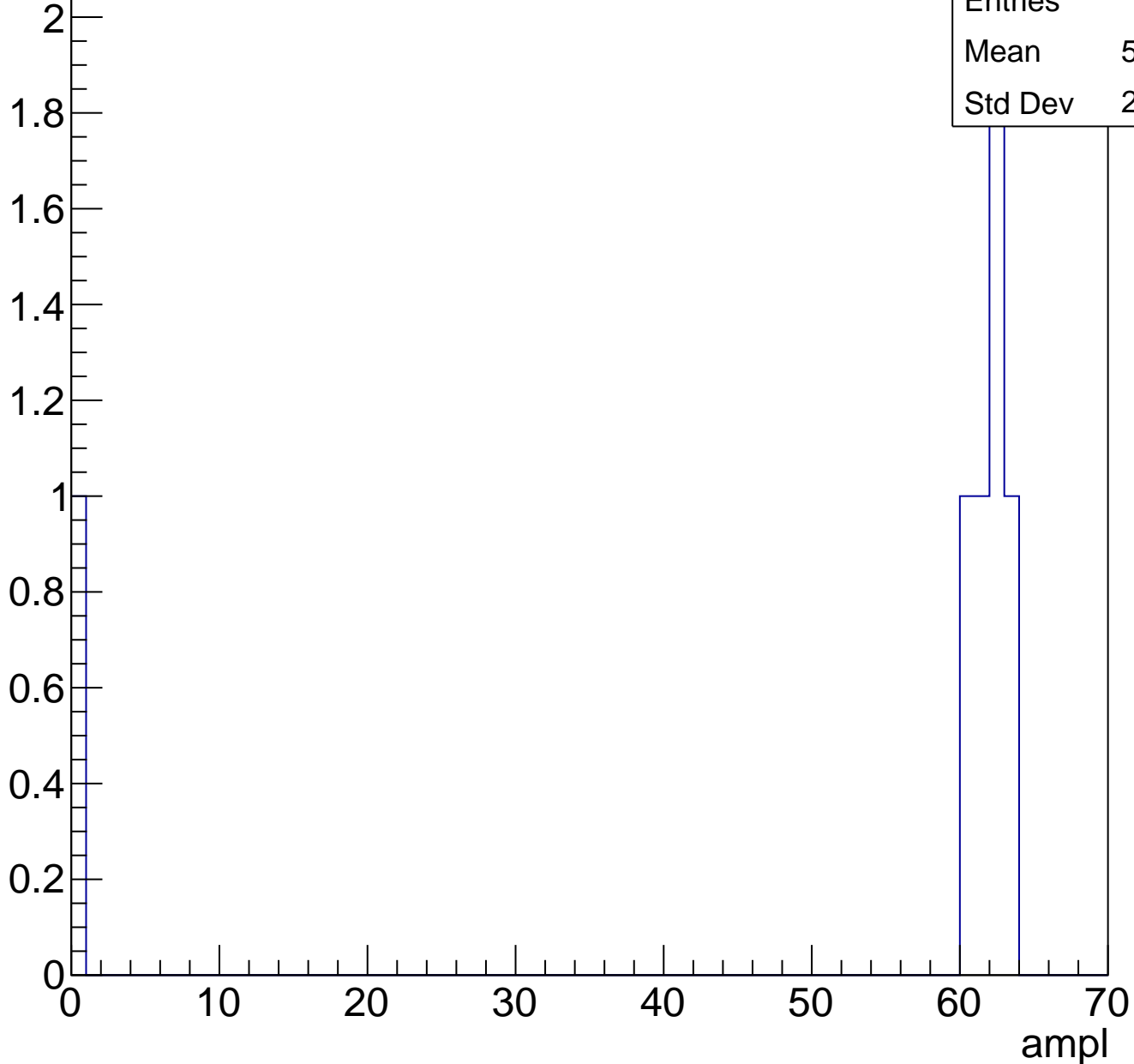
Entry



B1L103S, U12-ch20, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

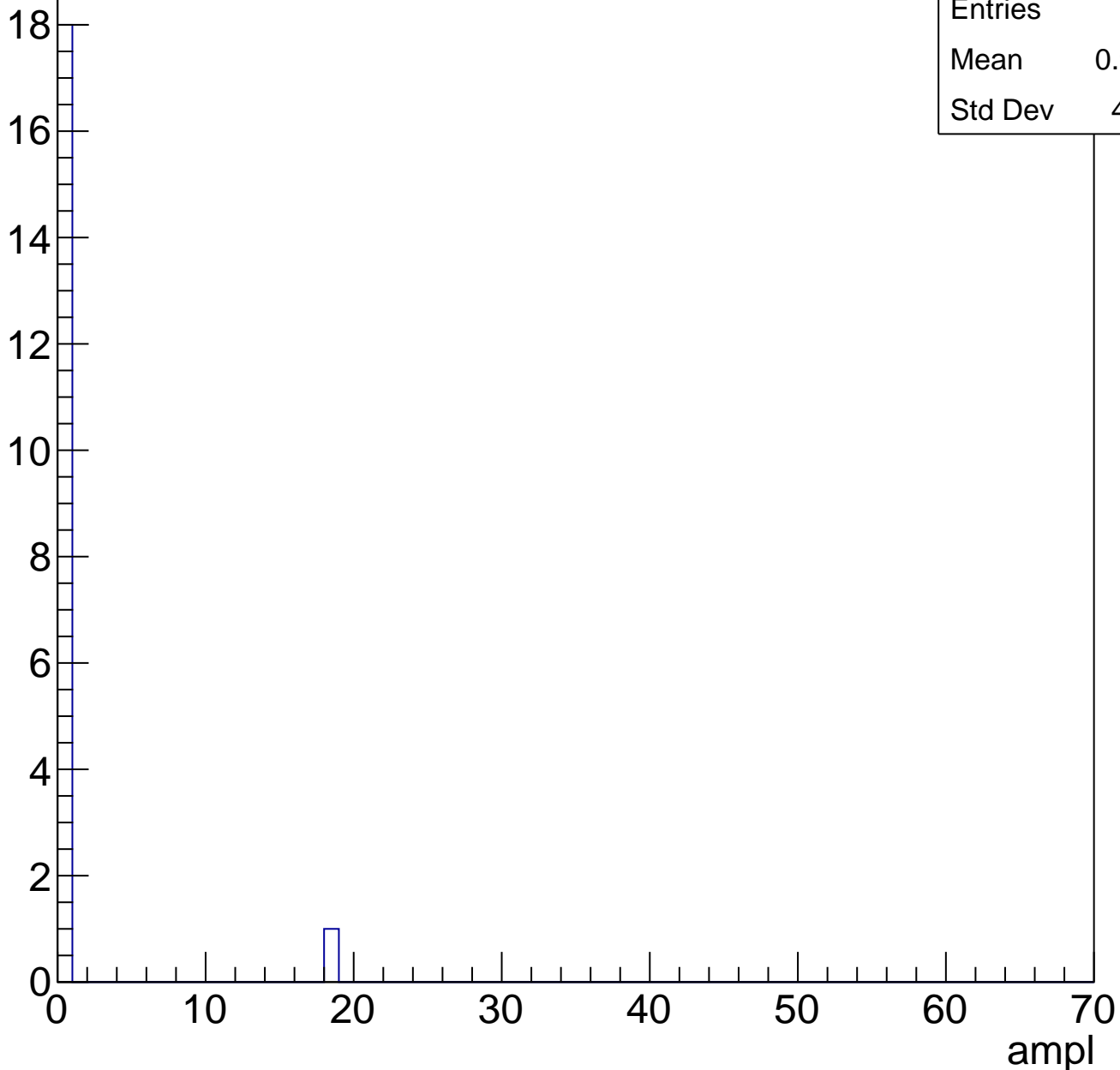


B1L103S, U12-ch20, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	0.9474
Std Dev	4.019

Entry

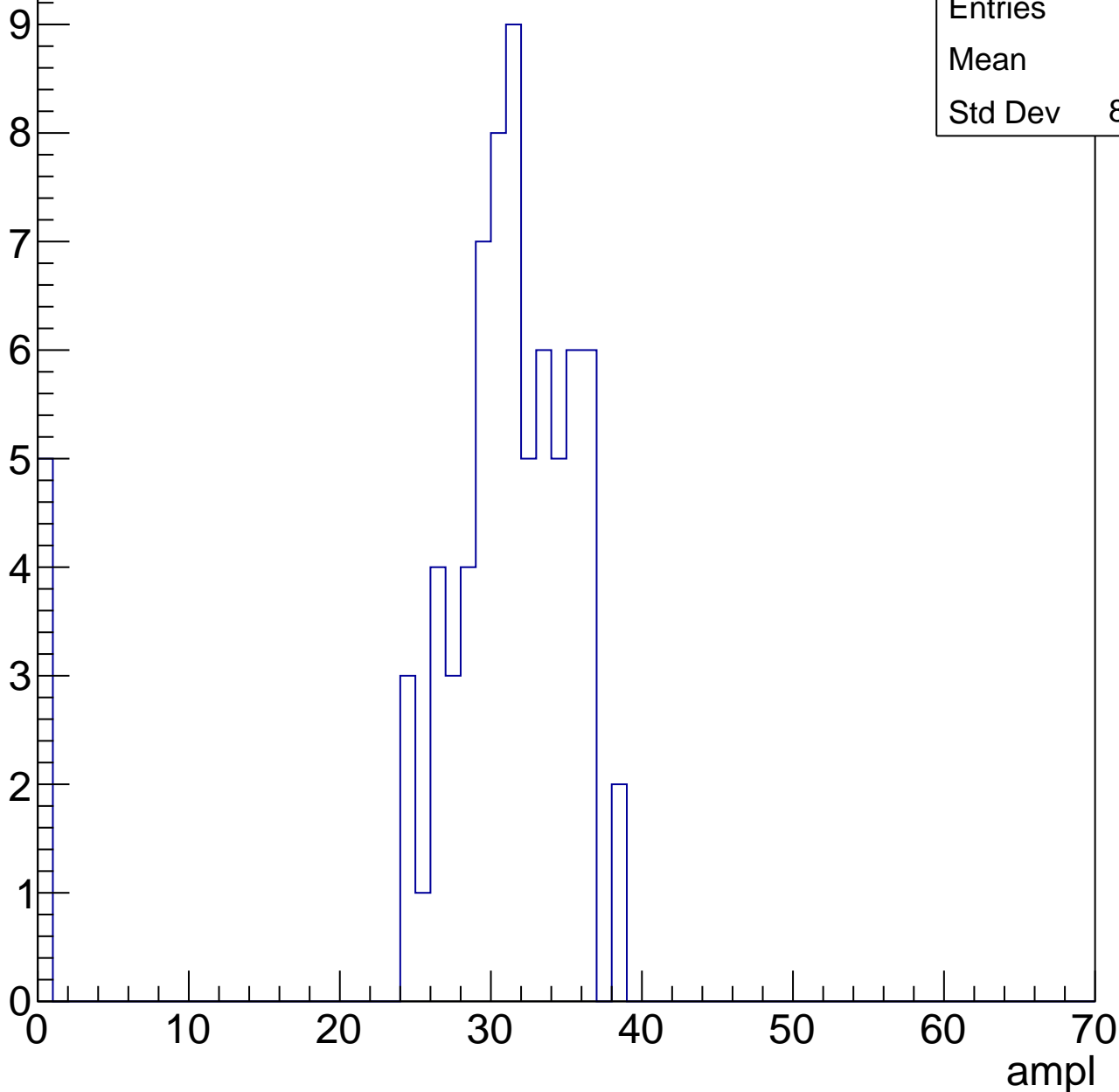


B1L103S, U12-ch21, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	74
Mean	29
Std Dev	8.487

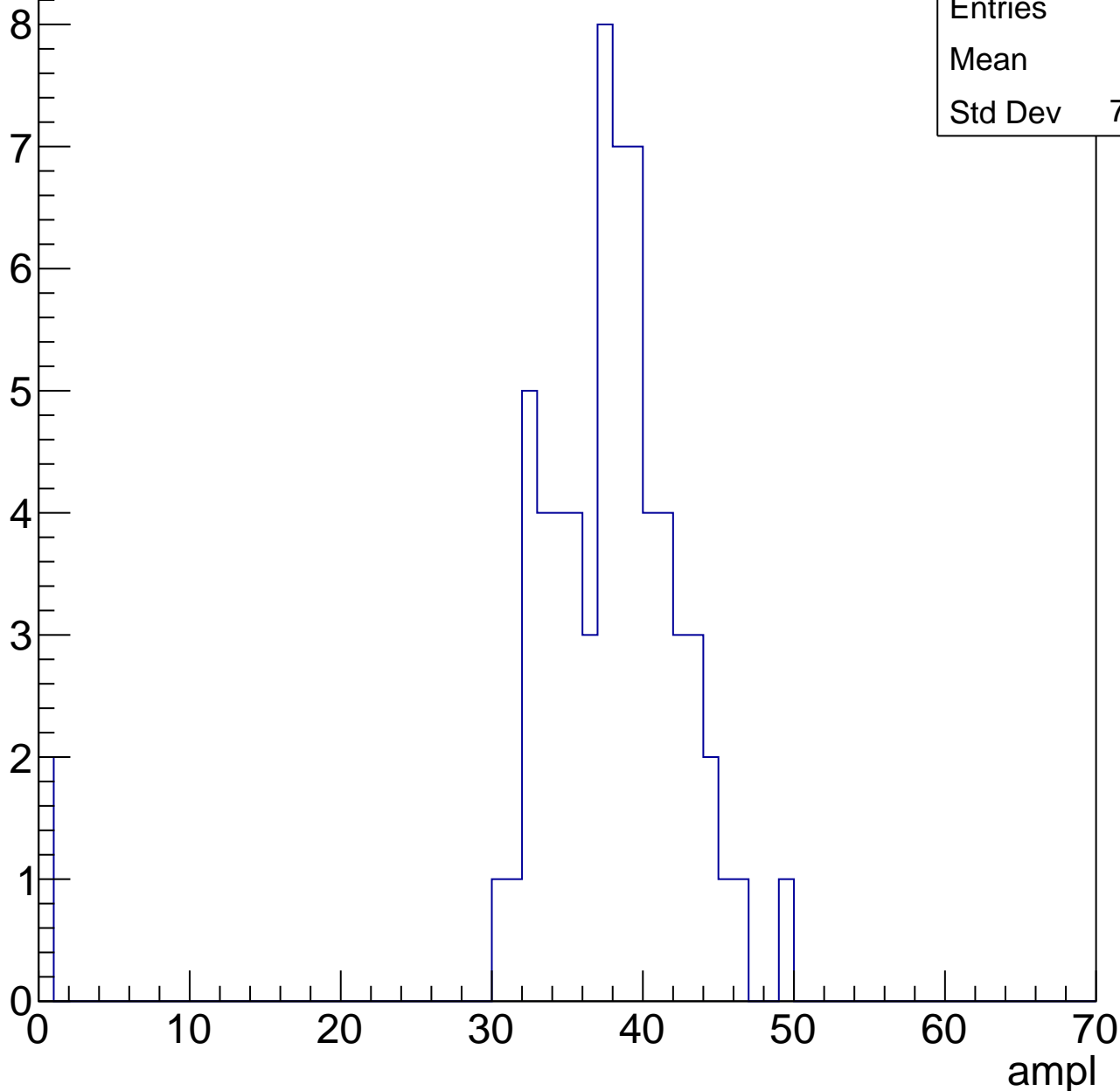


B1L103S, U12-ch21, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	36.6
Std Dev	7.607

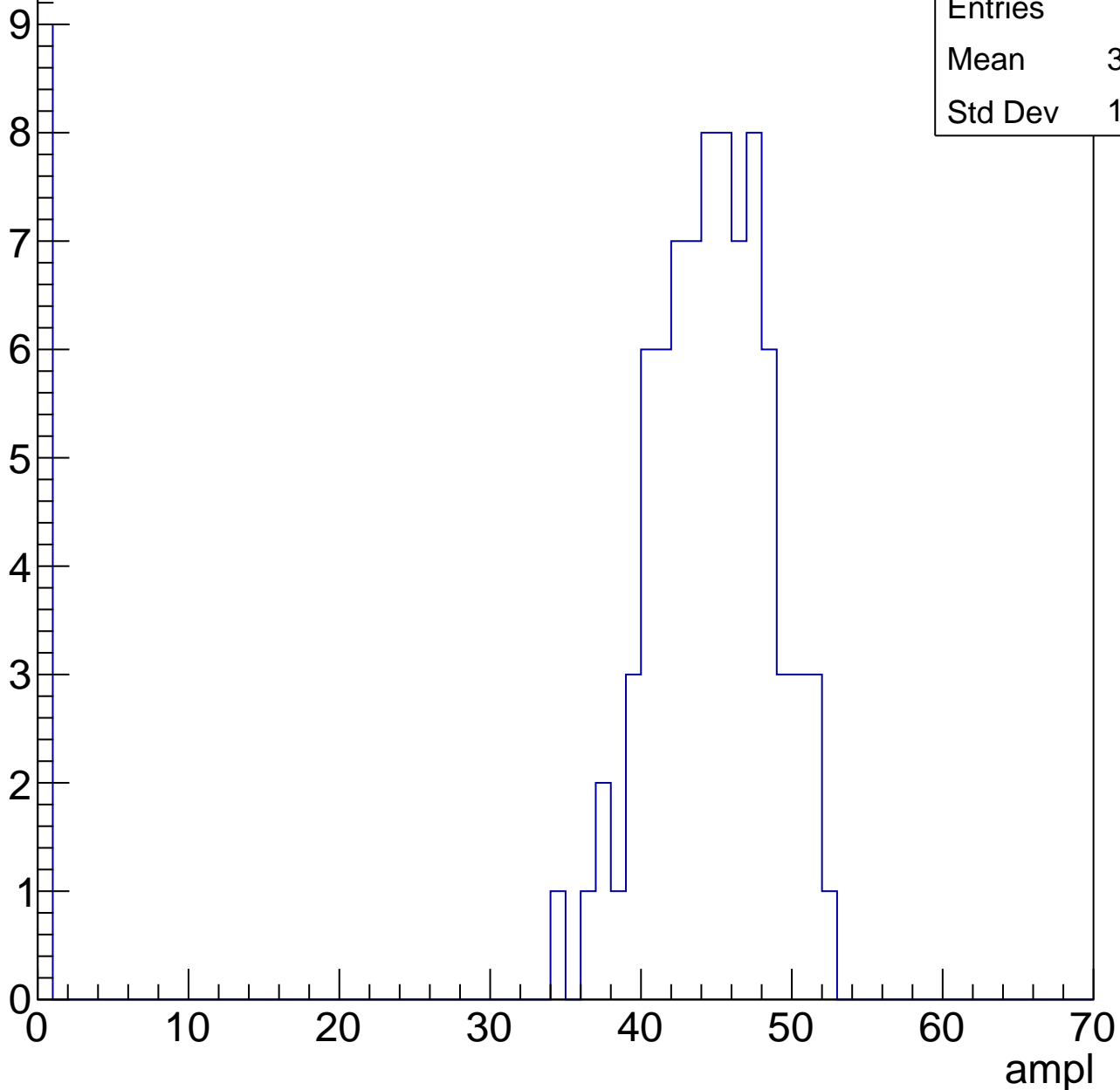


B1L103S, U12-ch21, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	90
Mean	39.78
Std Dev	13.73

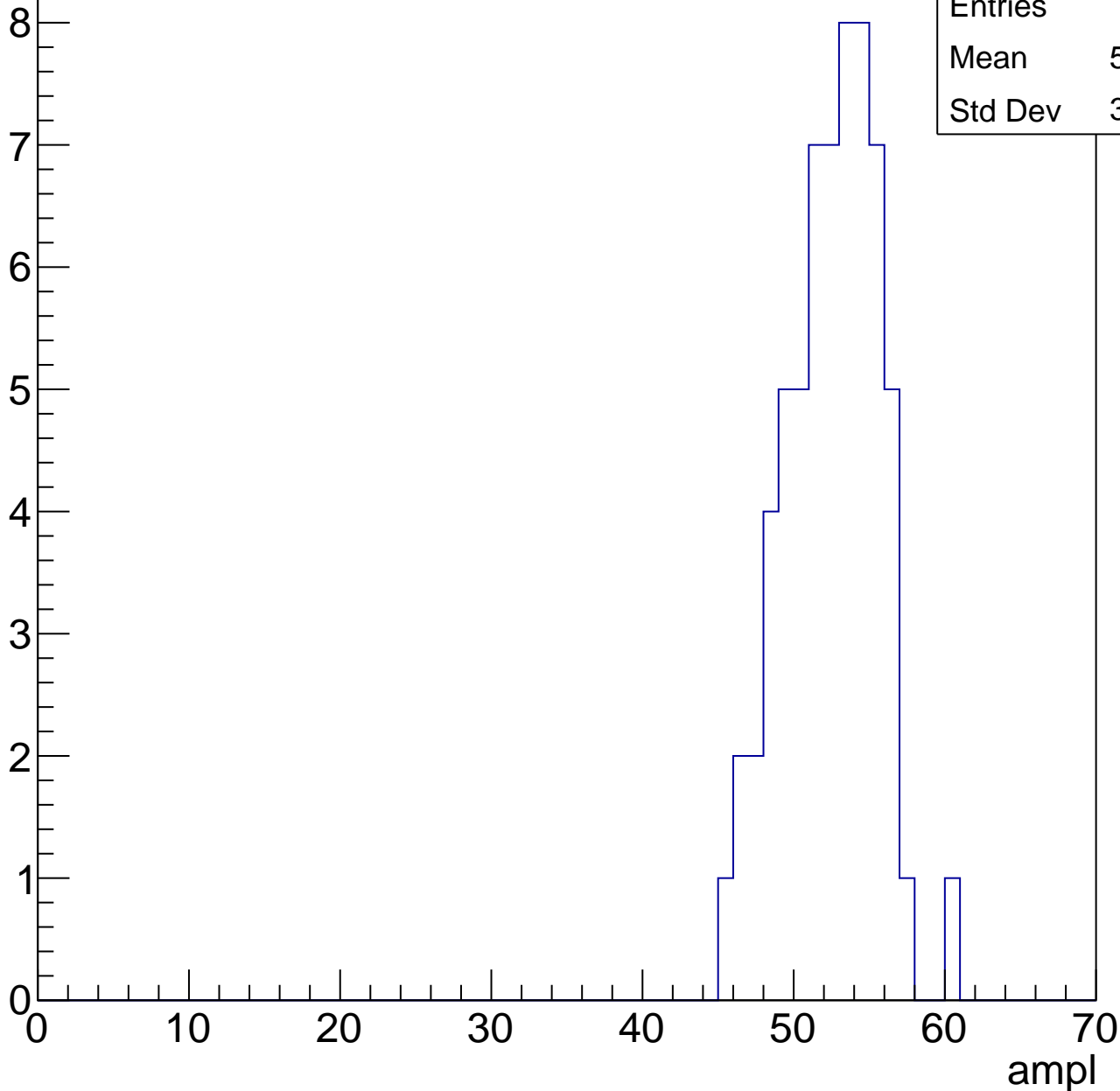


B1L103S, U12-ch21, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

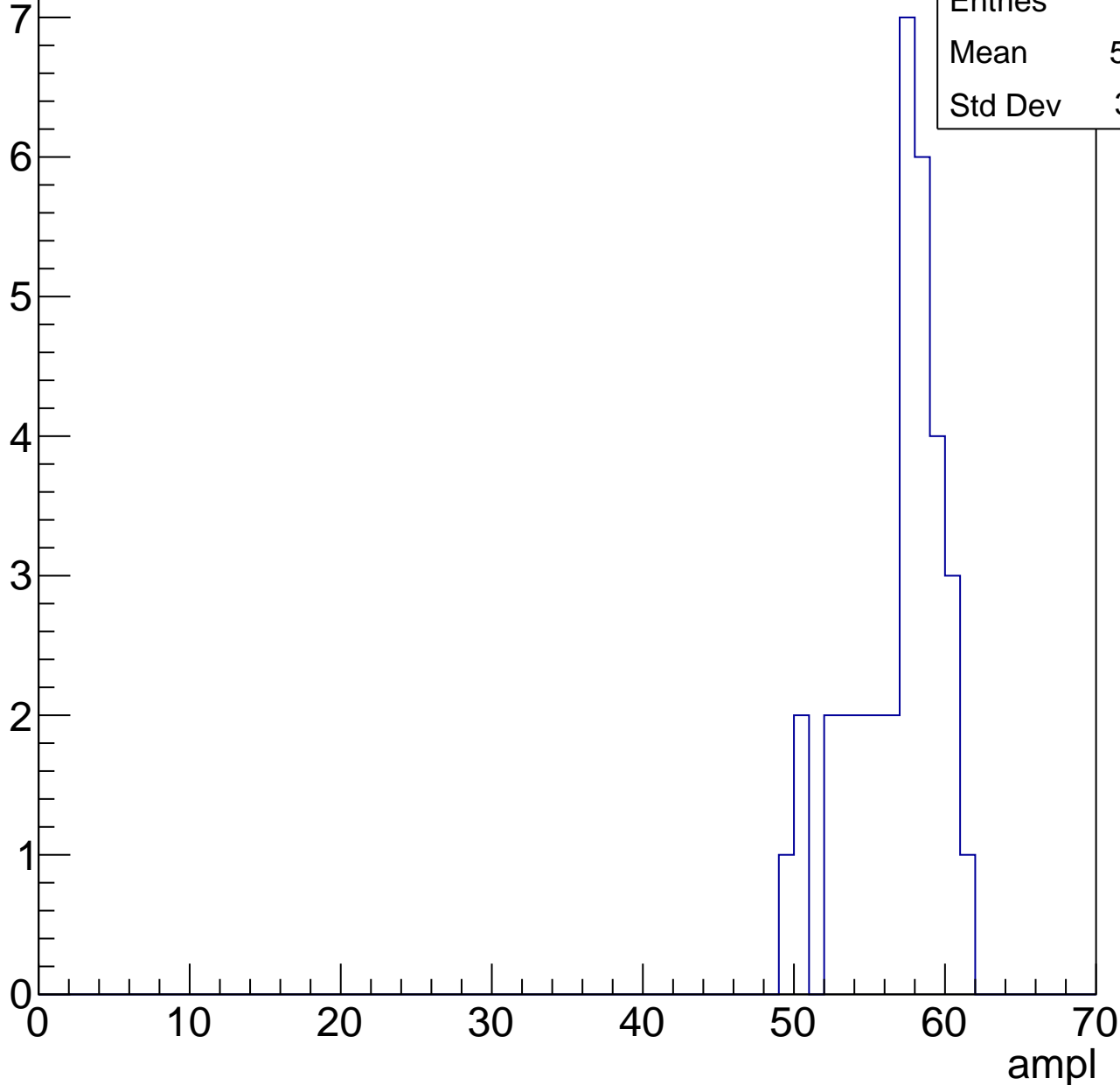
Entries	63
Mean	52.02
Std Dev	3.032



B1L103S, U12-ch21, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

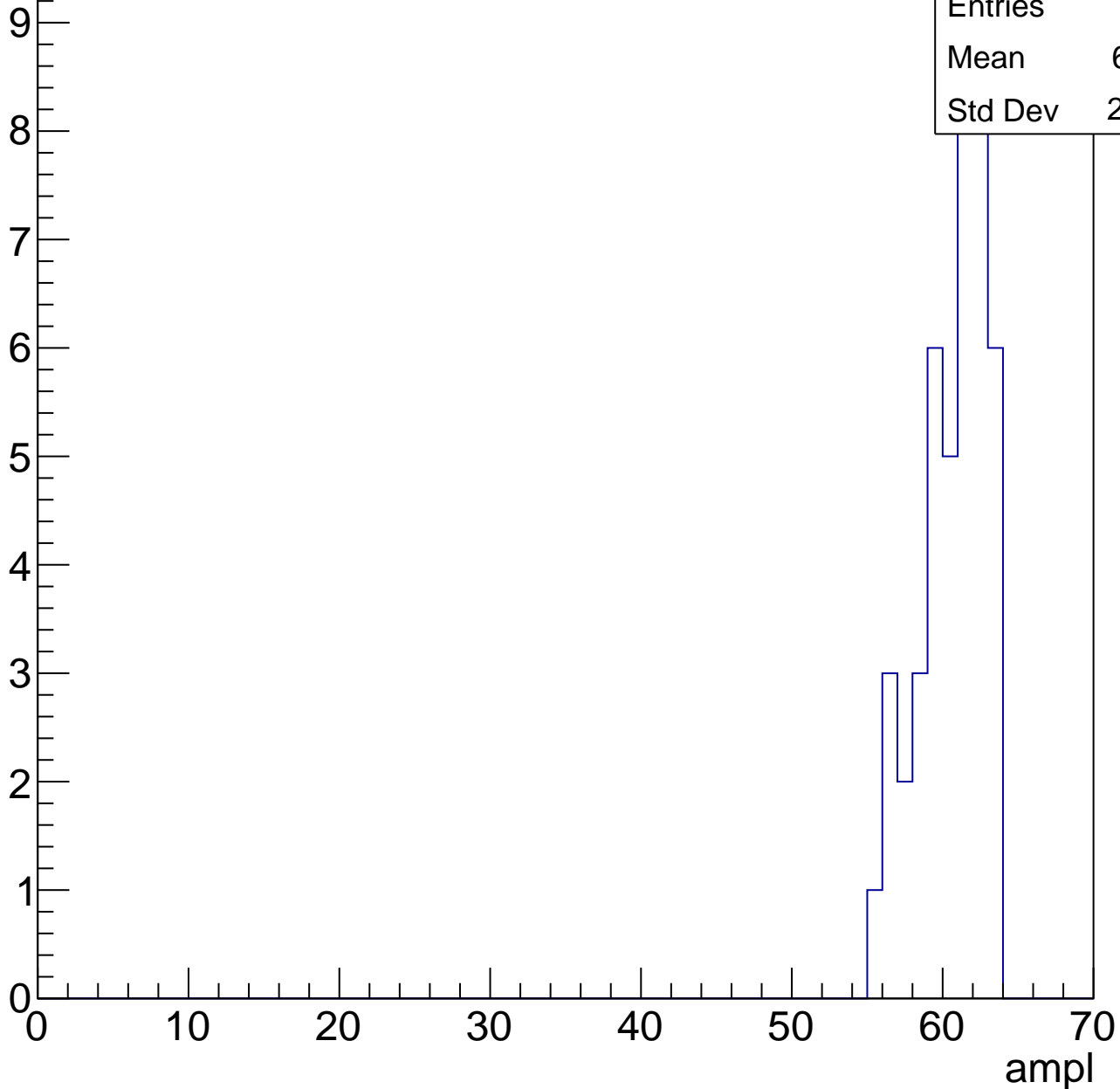


B1L103S, U12-ch21, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

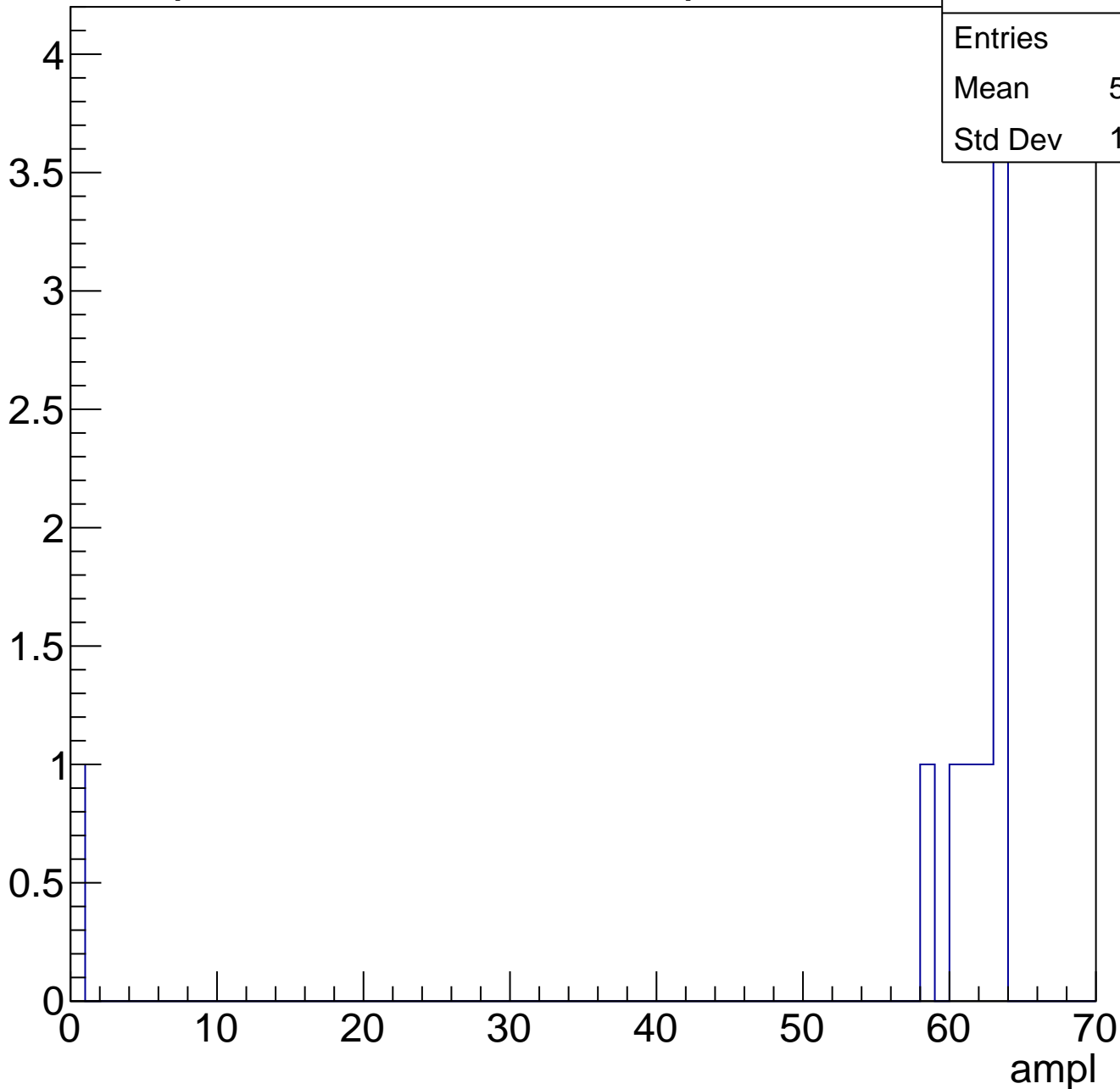
Entries	43
Mean	60.21
Std Dev	2.184



B1L103S, U12-ch21, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

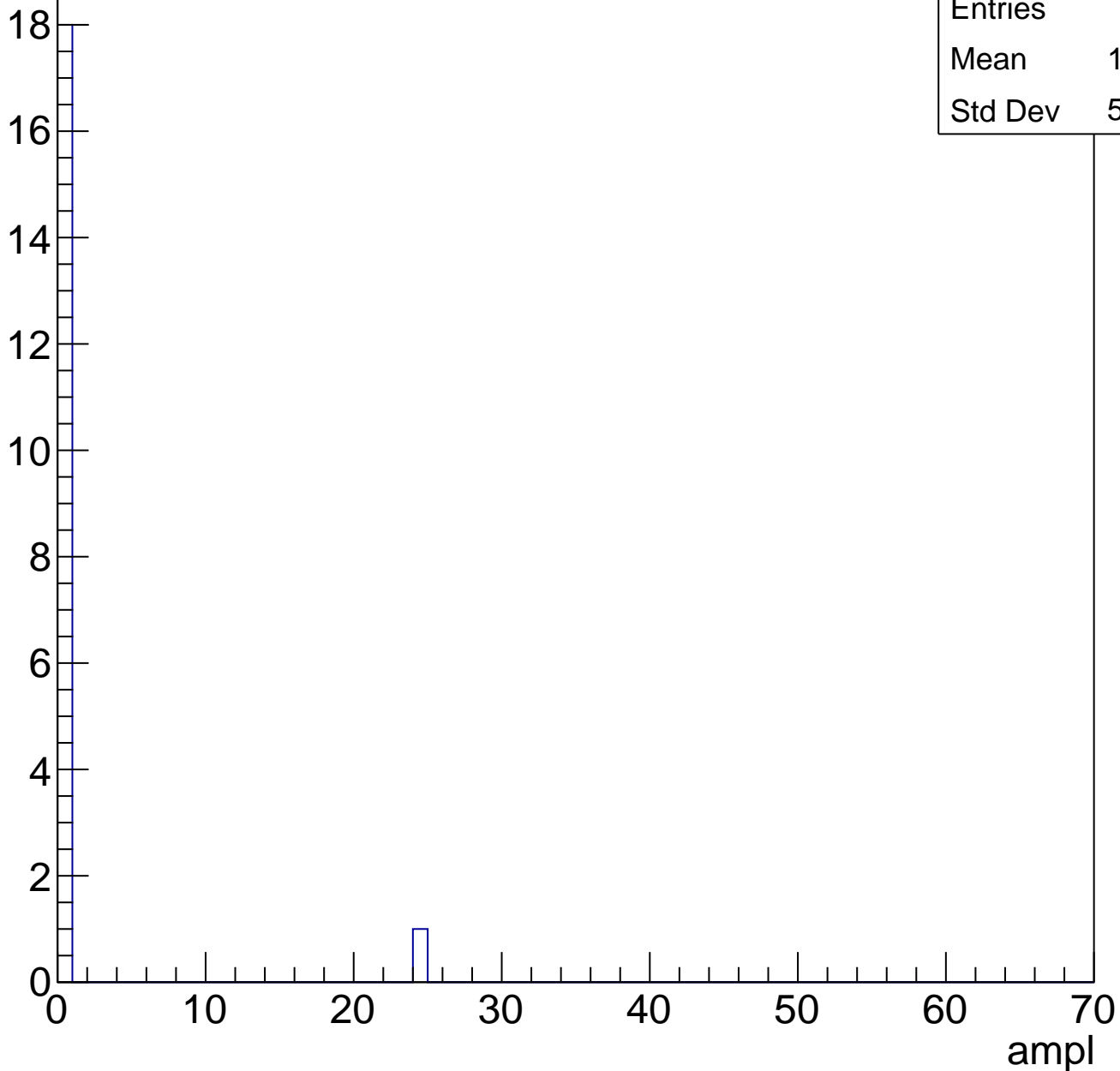


B1L103S, U12-ch21, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.263
Std Dev	5.359

Entry



B1L103S, U12-ch22, adc0

calib_packv5_041523_1651.root, FC#0, port C2

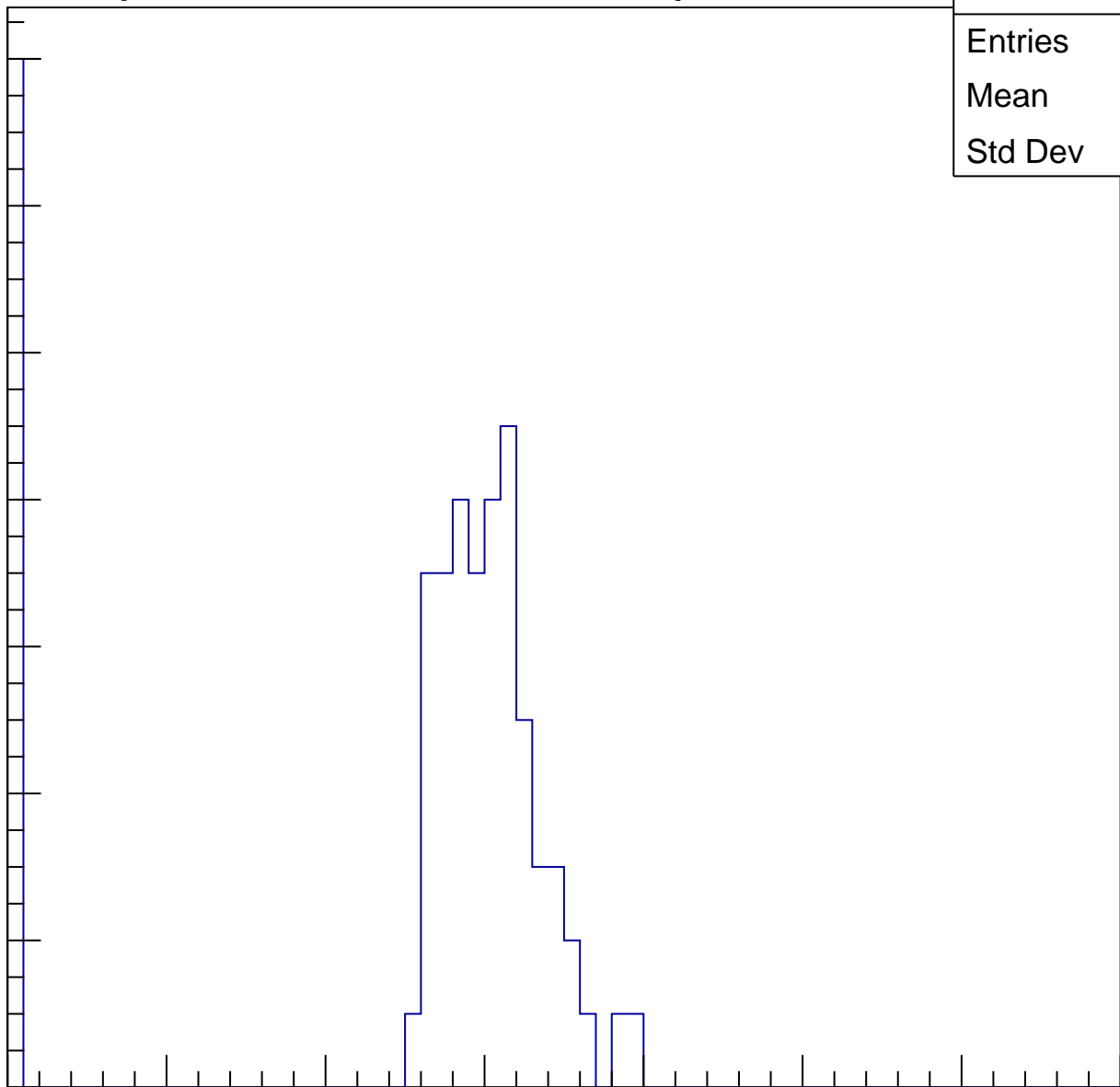
Entries	77
Mean	24.49
Std Dev	11.86

Entry

14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

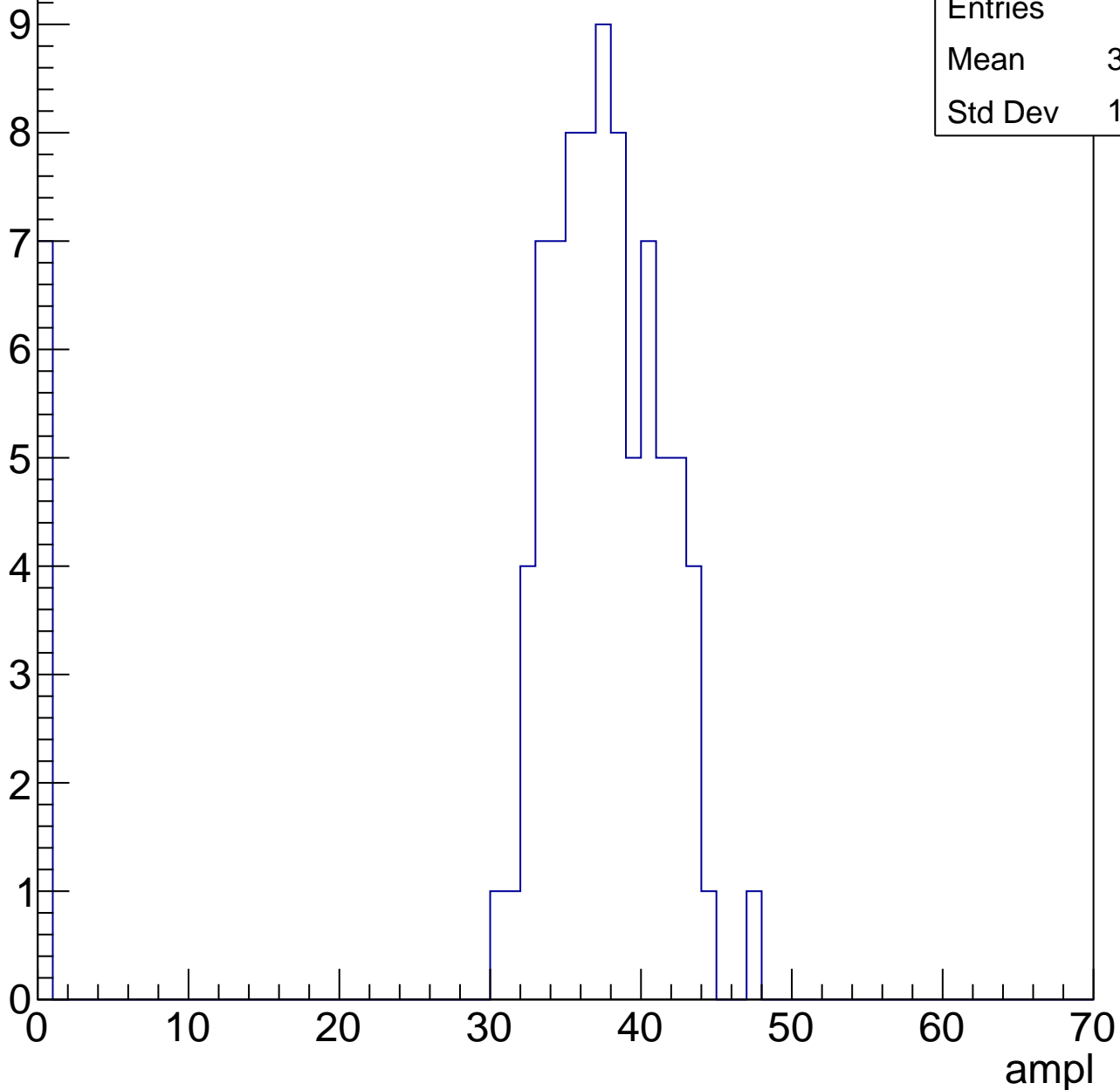


B1L103S, U12-ch22, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	88
Mean	34.27
Std Dev	10.62

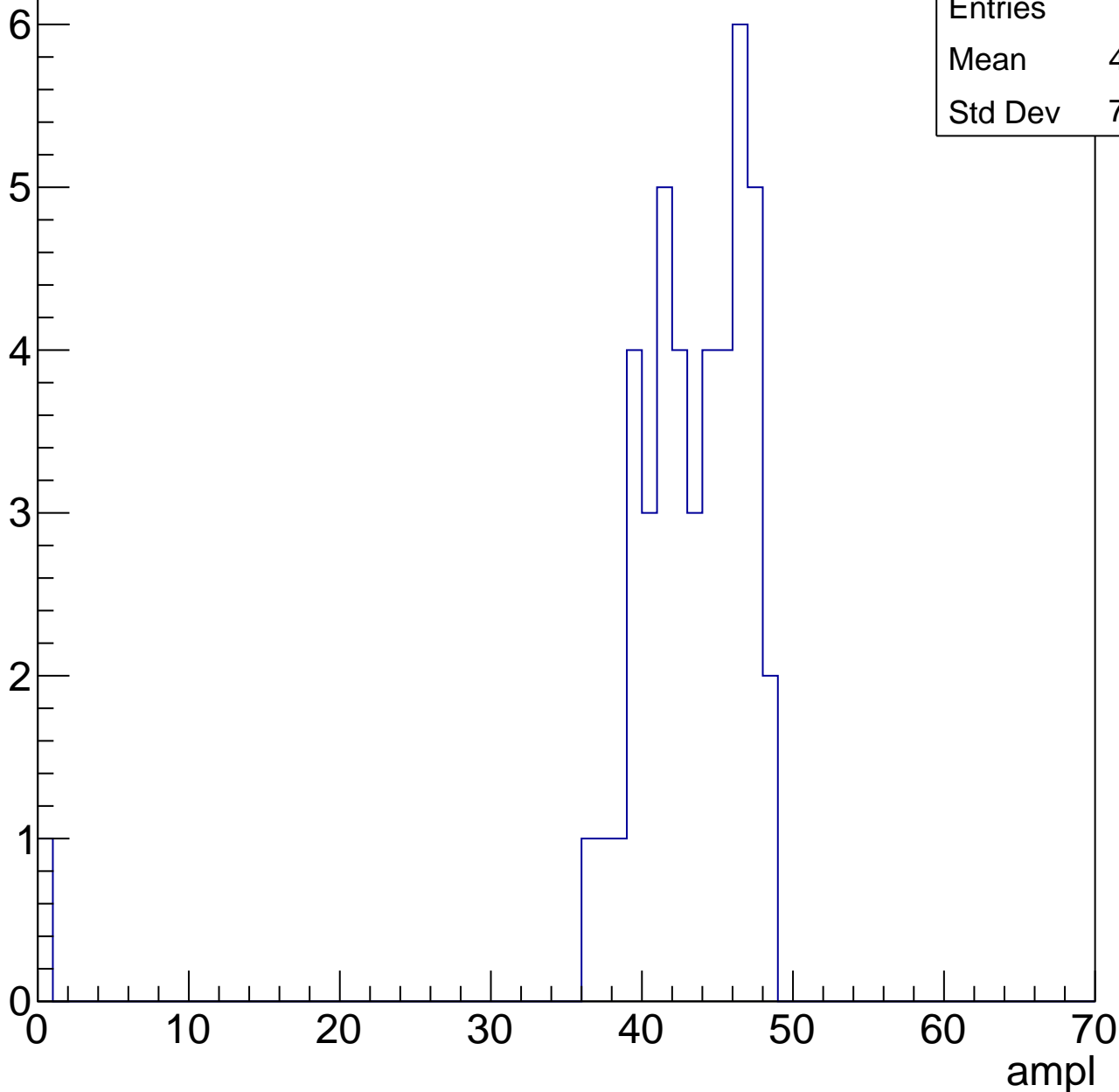


B1L103S, U12-ch22, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	44
Mean	42.09
Std Dev	7.138



B1L103S, U12-ch22, adc3

calib_packv5_041523_1651.root, FC#0, port C2

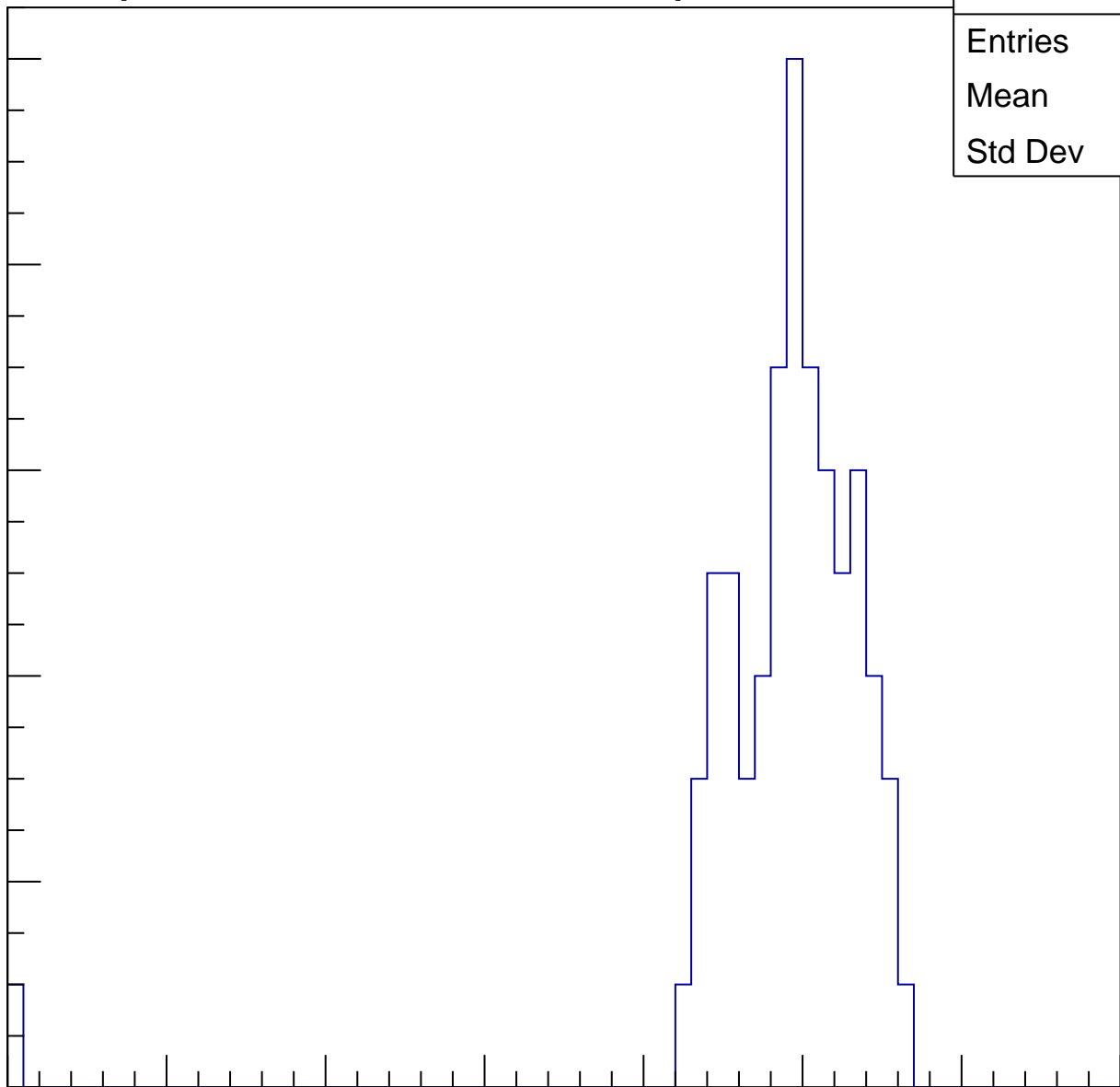
Entries	71
Mean	48.44
Std Dev	6.734

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

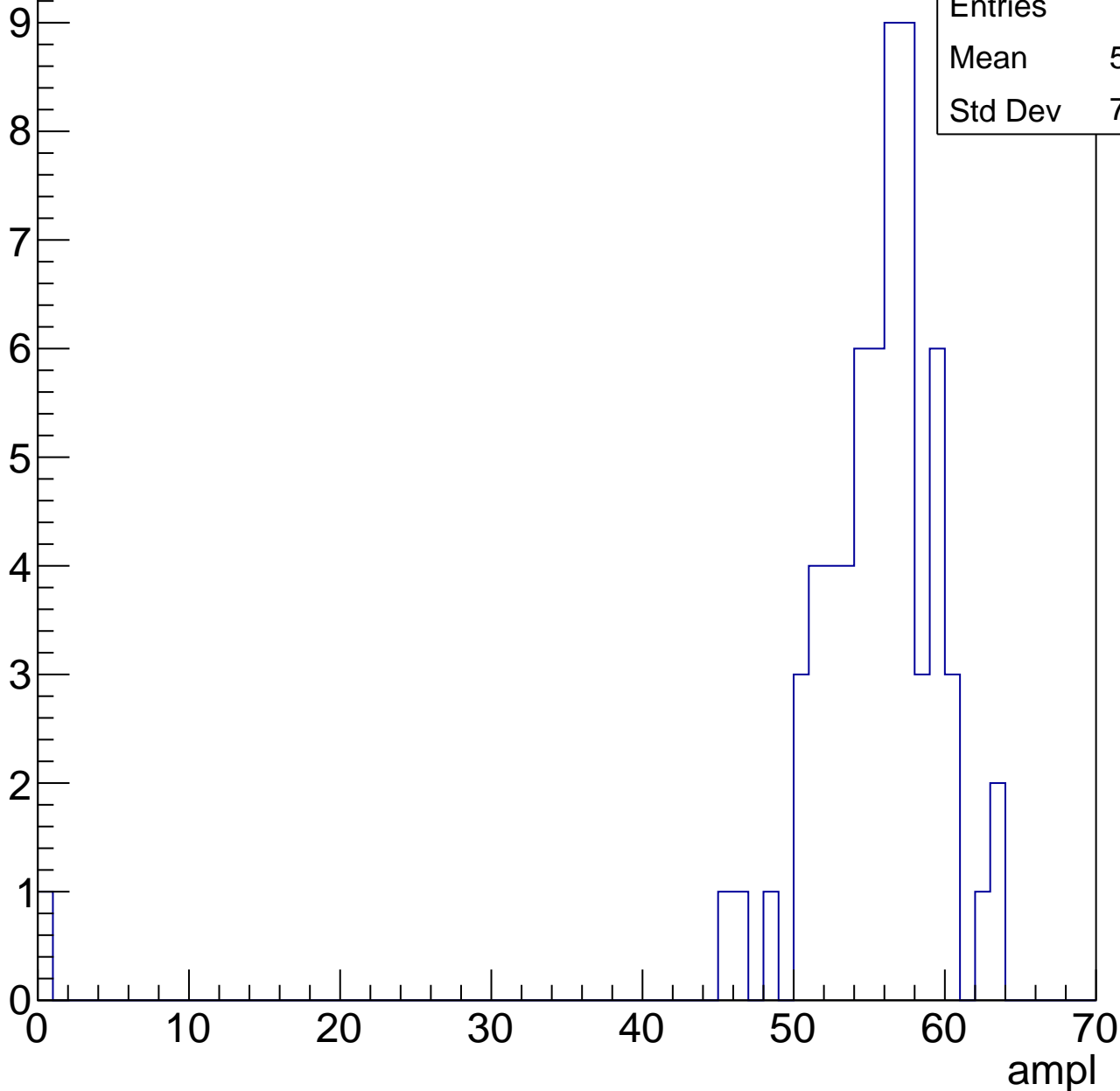


B1L103S, U12-ch22, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	54.38
Std Dev	7.753

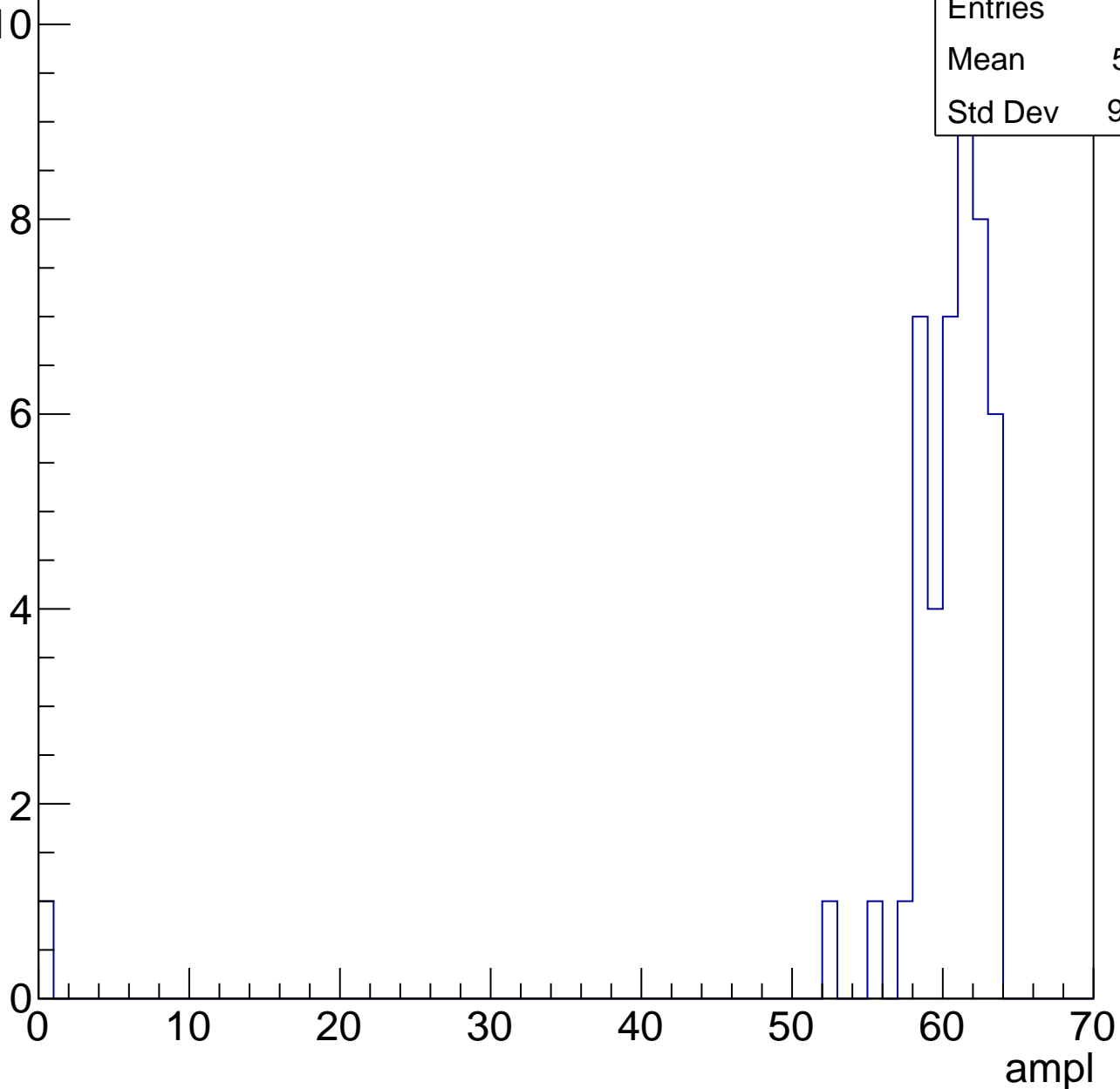


B1L103S, U12-ch22, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	46
Mean	58.91
Std Dev	9.055



B1L103S, U12-ch22, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

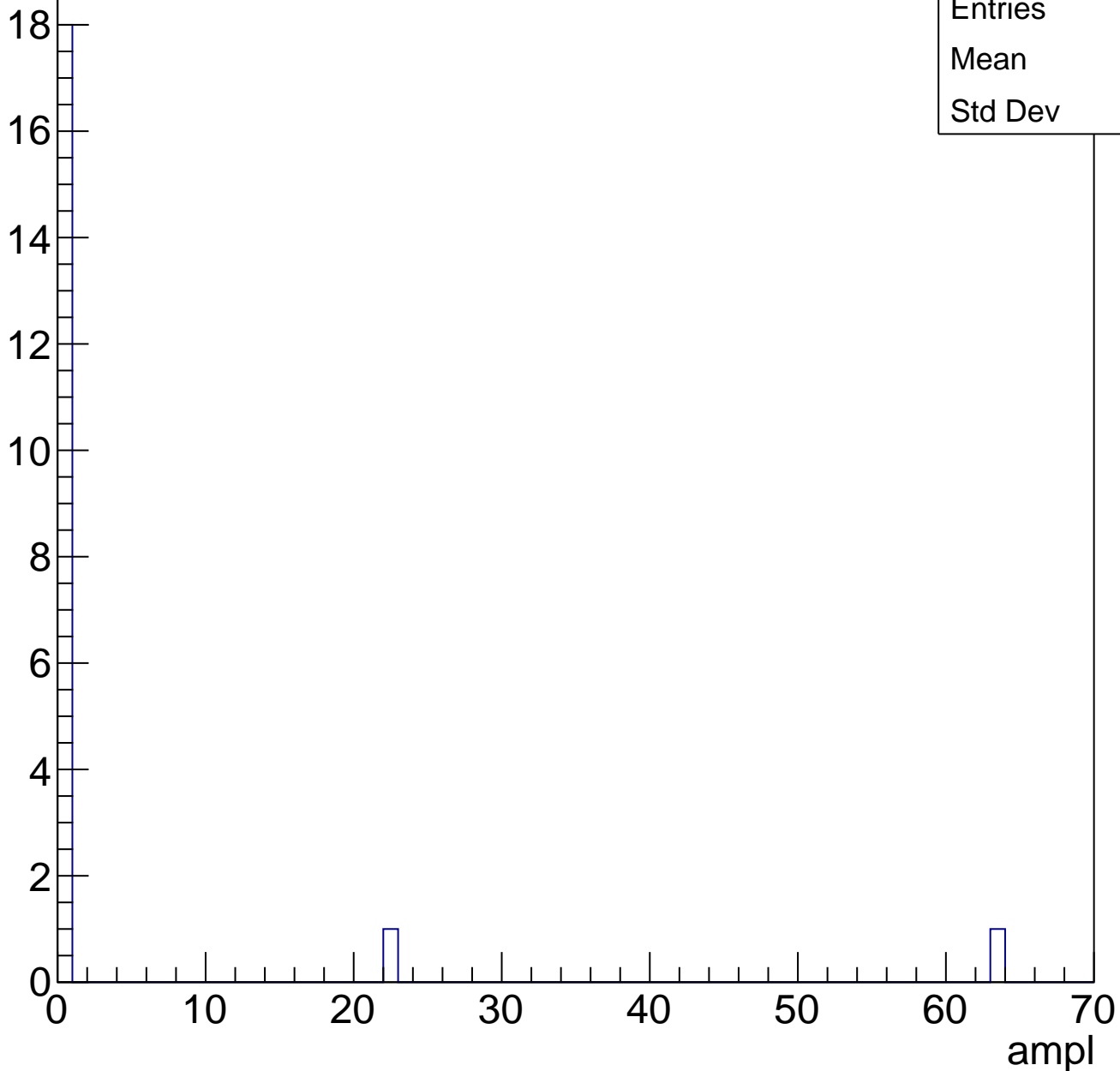


B1L103S, U12-ch22, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	4.25
Std Dev	14.3

Entry

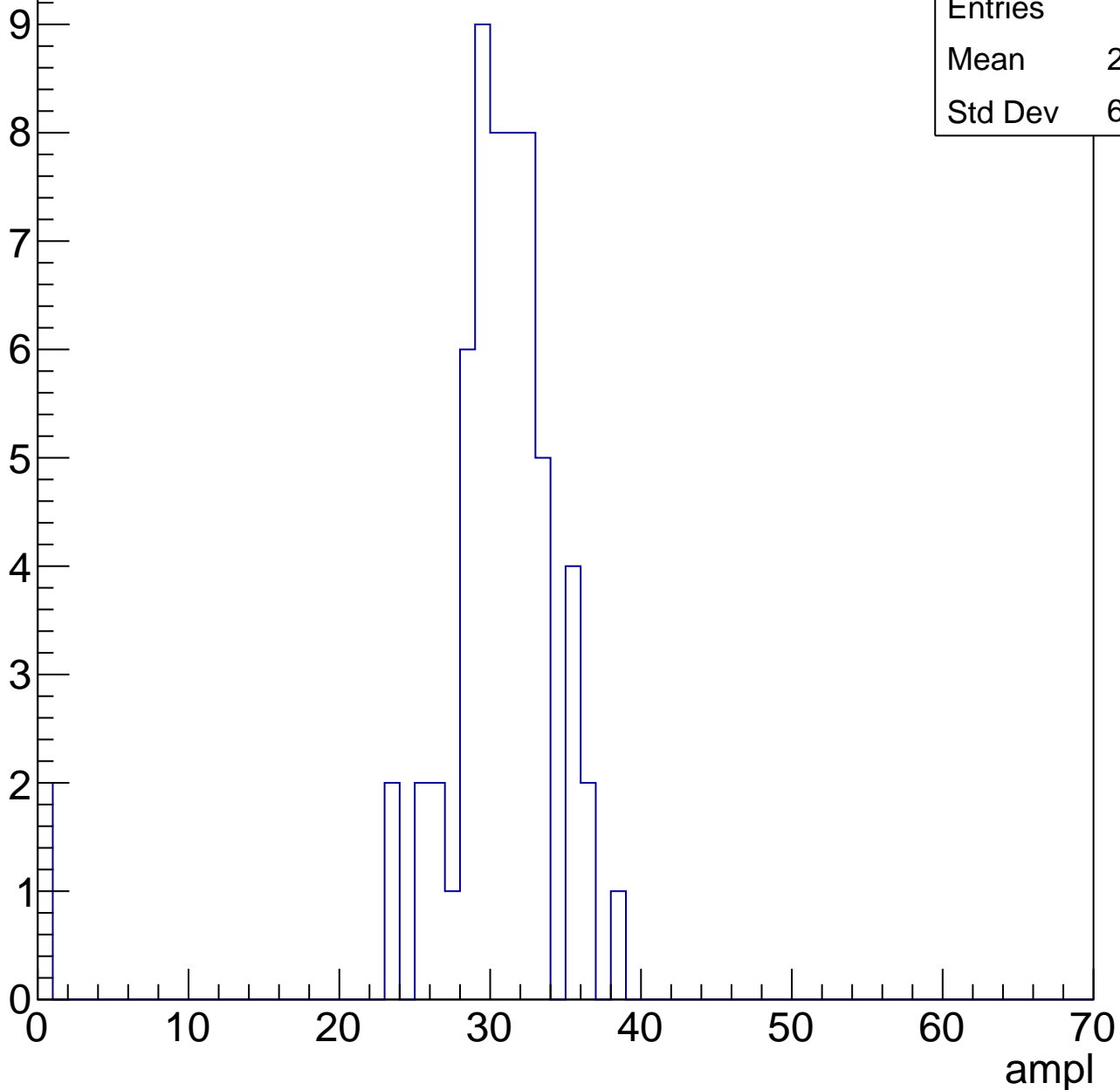


B1L103S, U12-ch23, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	29.38
Std Dev	6.218



B1L103S, U12-ch23, adc1

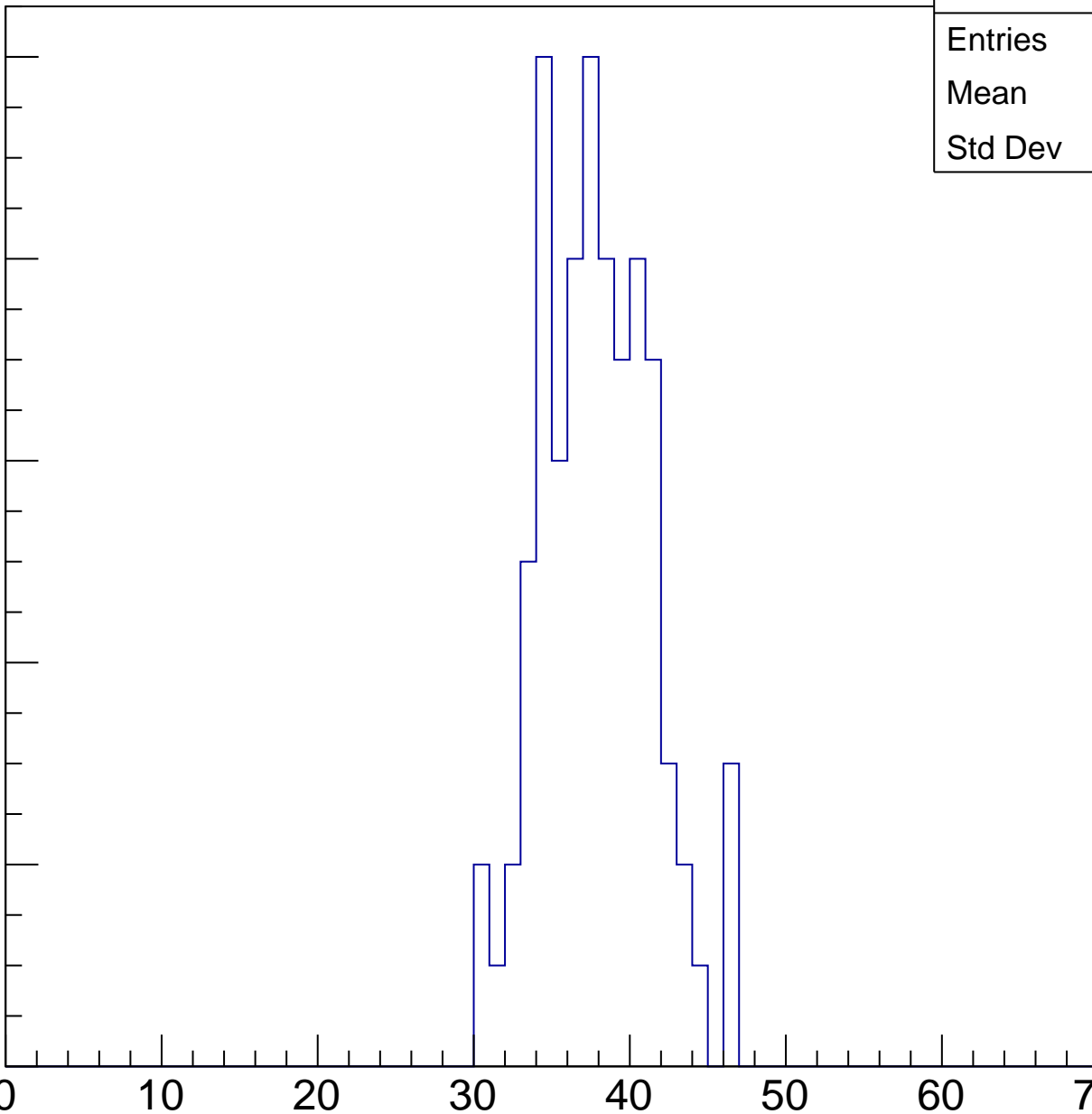
calib_packv5_041523_1651.root, FC#0, port C2

Entries	83
Mean	37.42
Std Dev	3.523

Entry

10
8
6
4
2
0

ampl

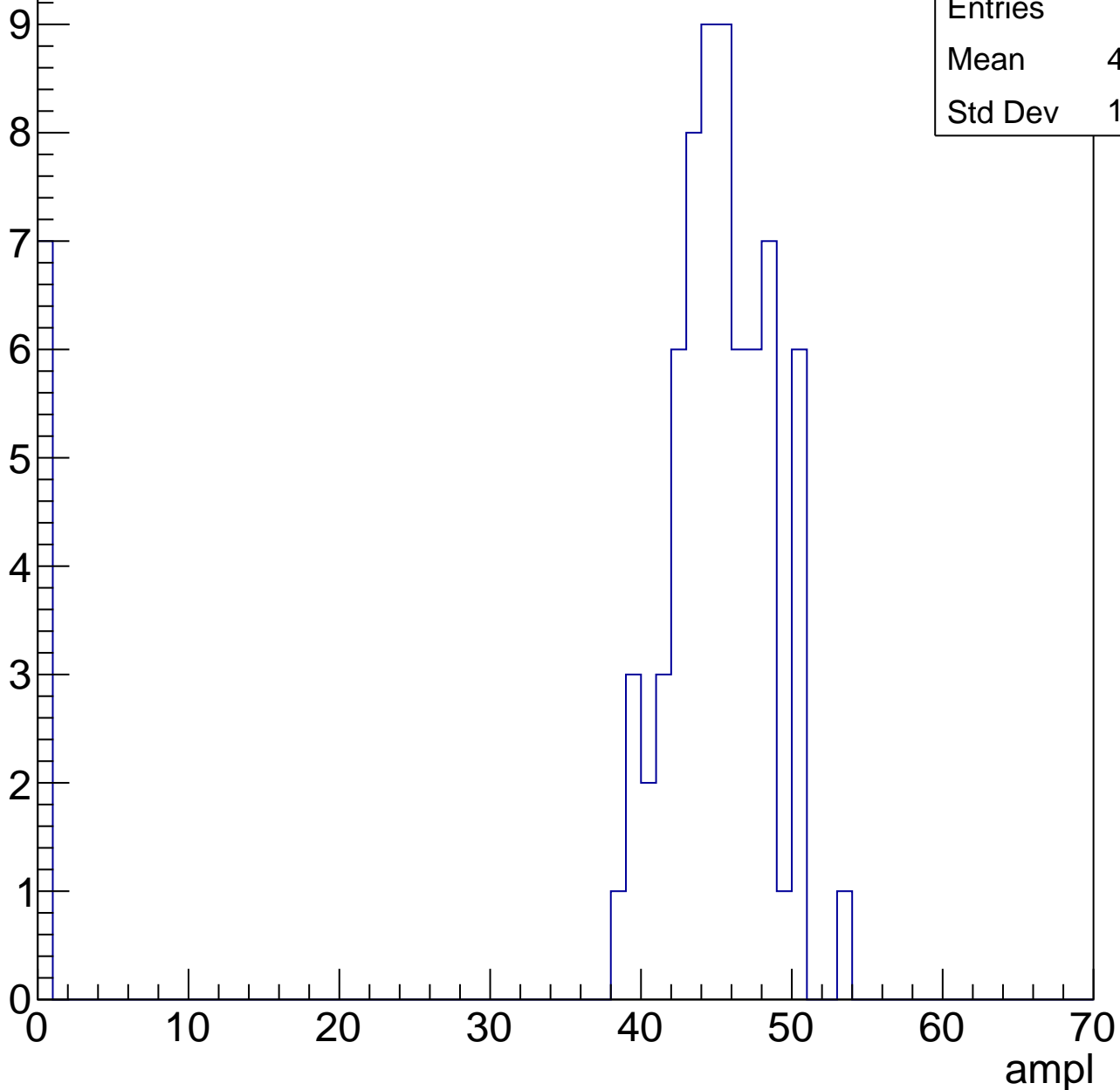


B1L103S, U12-ch23, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	75
Mean	40.68
Std Dev	13.39



B1L103S, U12-ch23, adc3

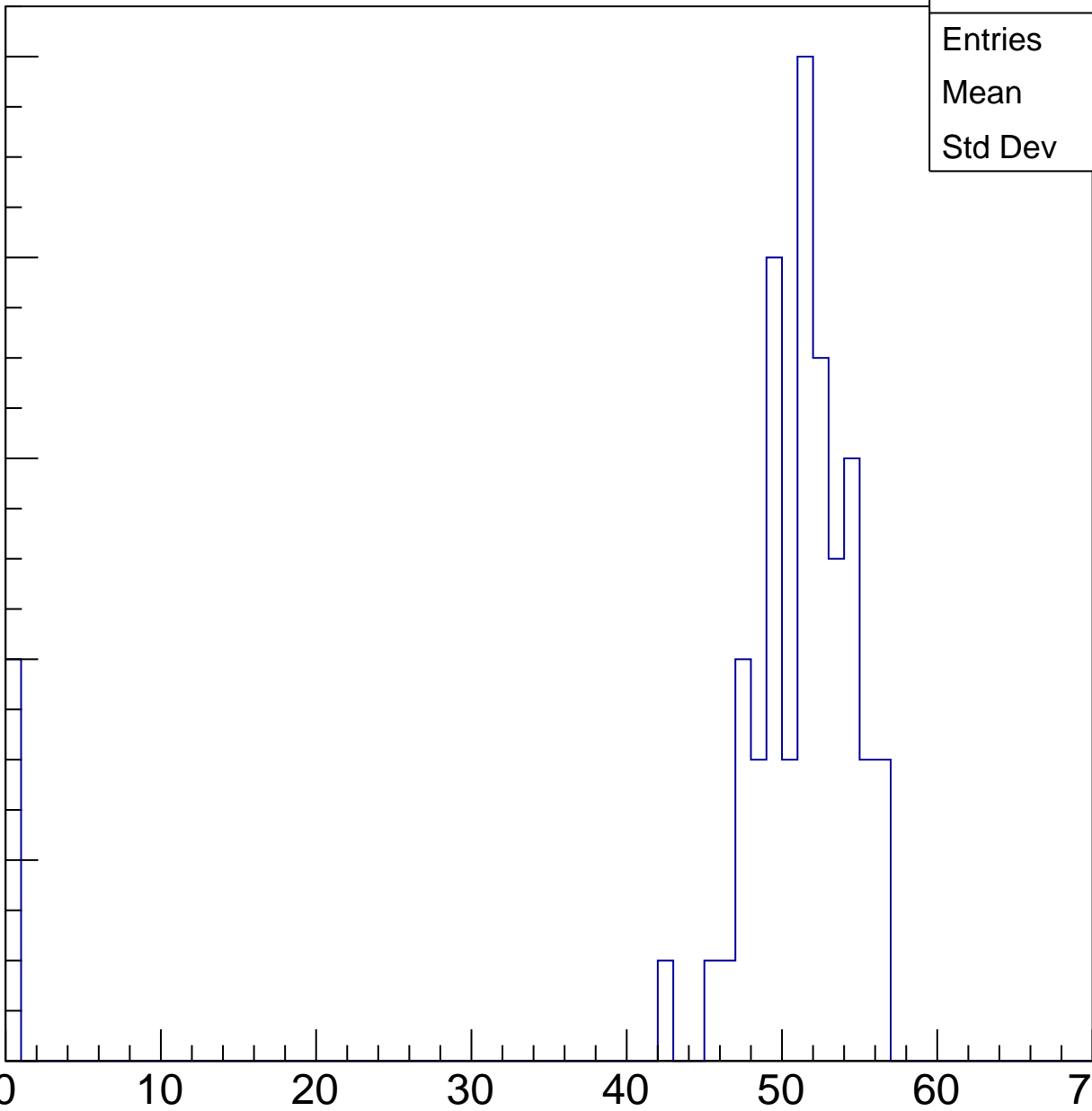
calib_packv5_041523_1651.root, FC#0, port C2

Entries	59
Mean	47.51
Std Dev	13.12

Entry

10
8
6
4
2
0

ampl

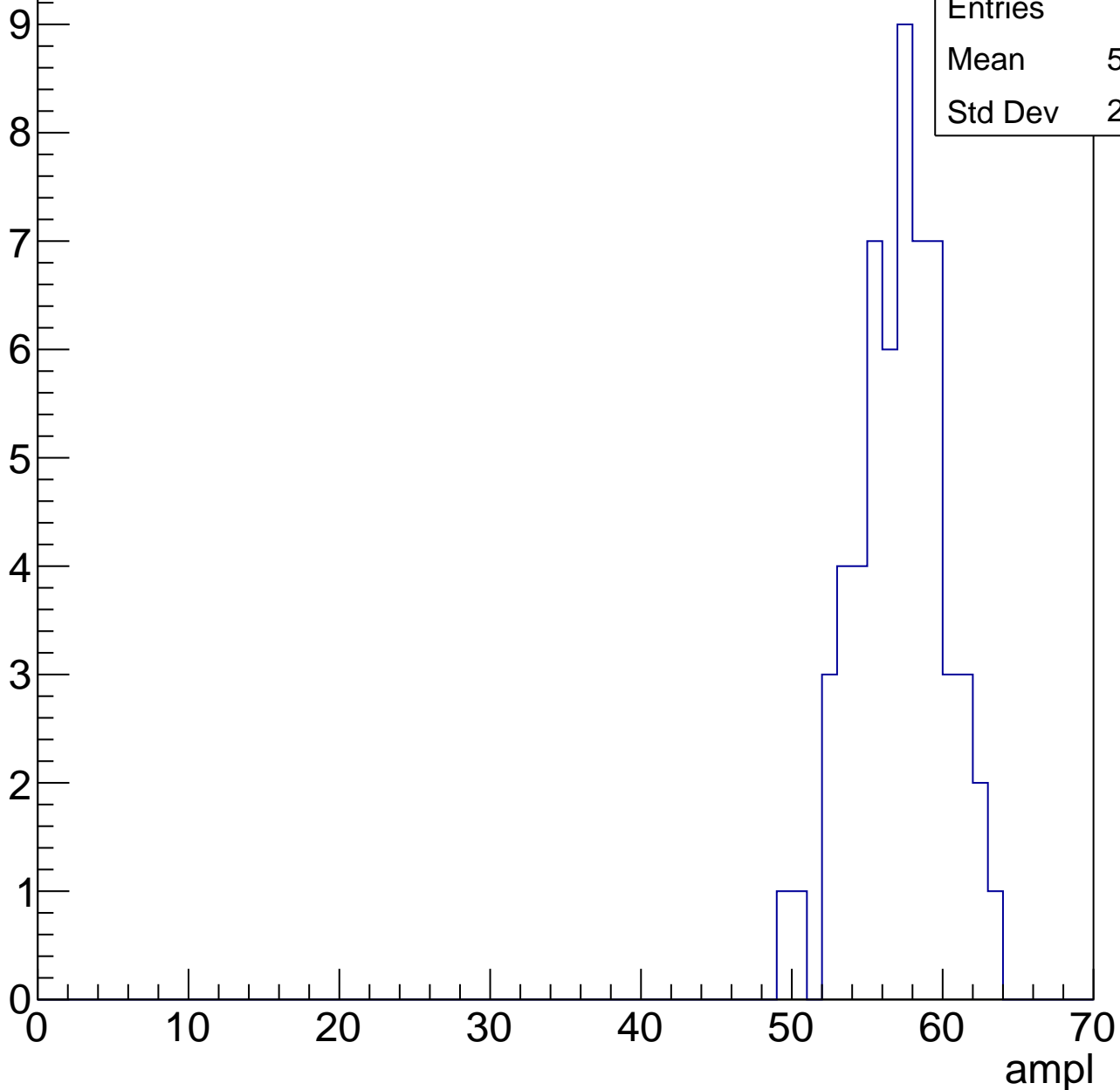


B1L103S, U12-ch23, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	56.66
Std Dev	2.969

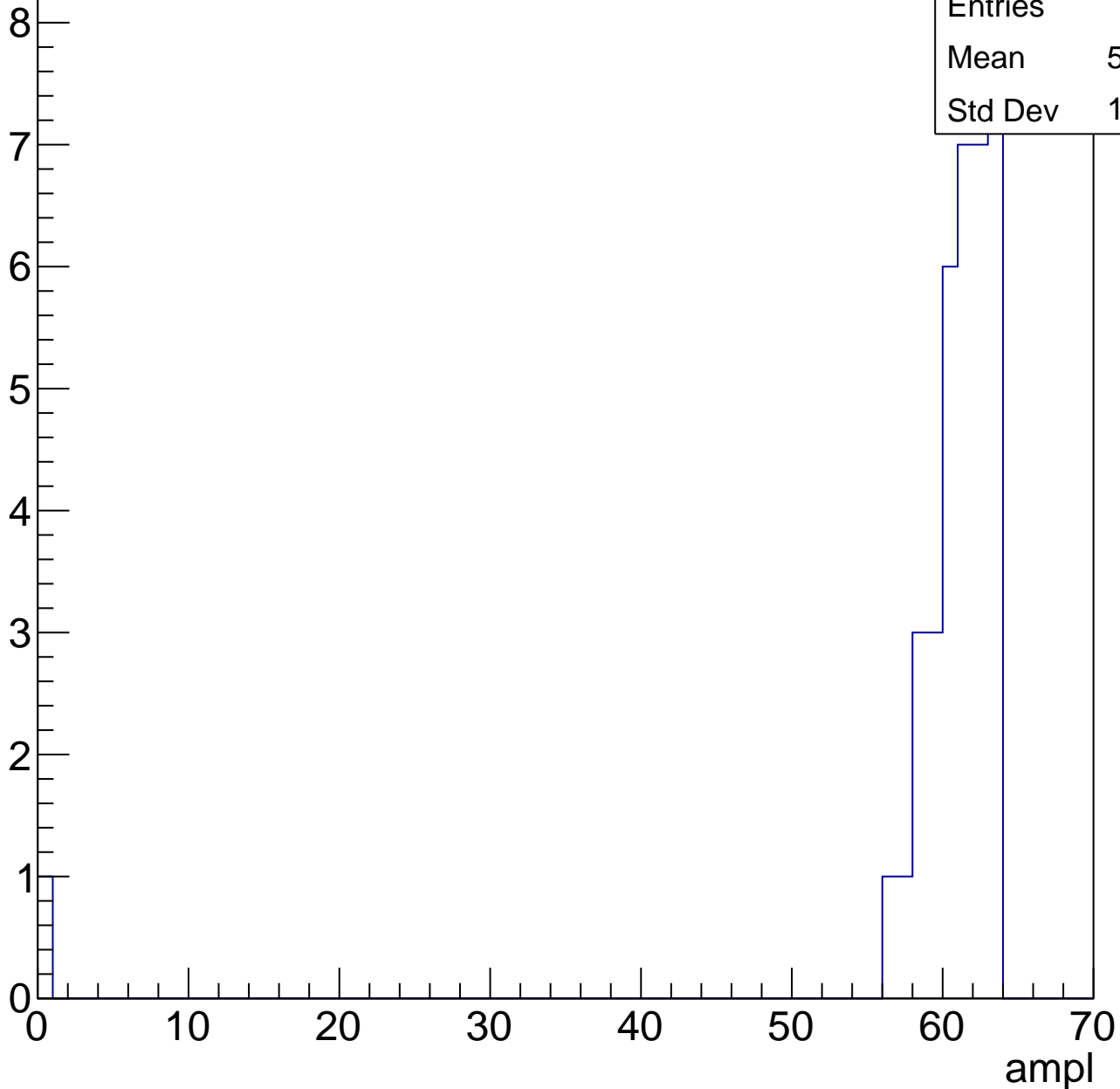


B1L103S, U12-ch23, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	37
Mean	59.16
Std Dev	10.03



B1L103S, U12-ch23, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch23, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

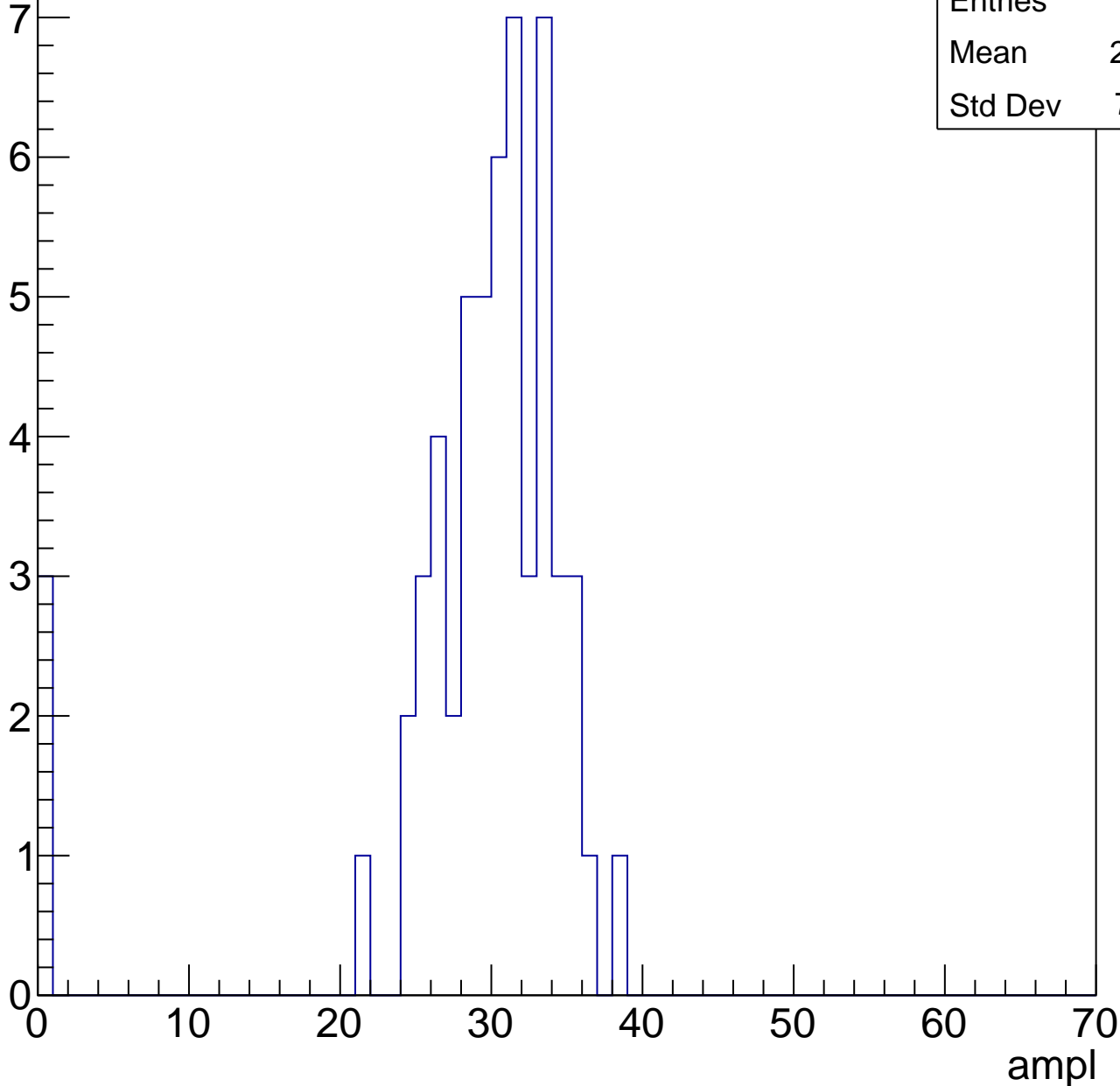


B1L103S, U12-ch24, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	56
Mean	28.43
Std Dev	7.561



B1L103S, U12-ch24, adc1

calib_packv5_041523_1651.root, FC#0, port C2

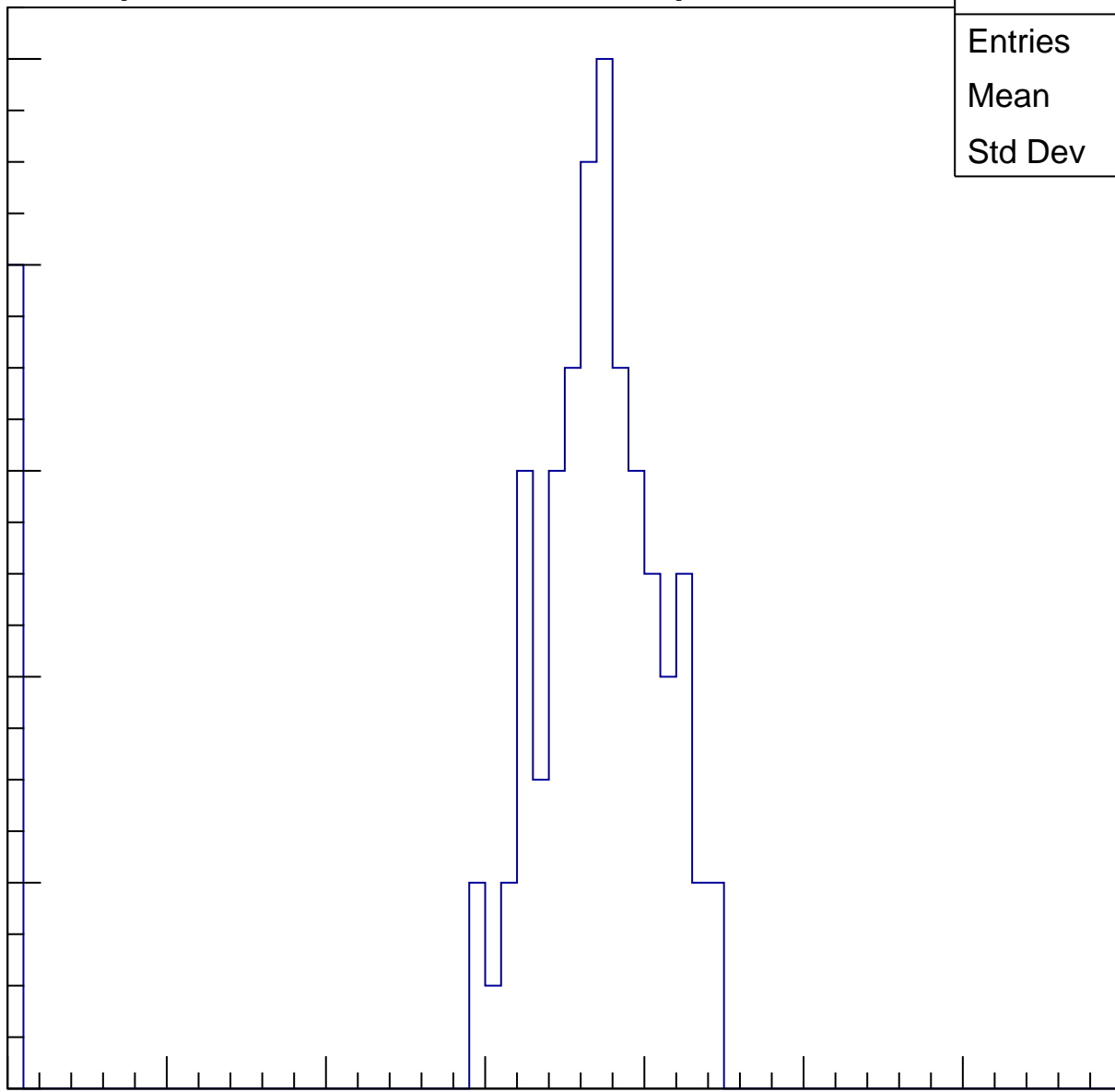
Entries	85
Mean	33.32
Std Dev	11.26

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

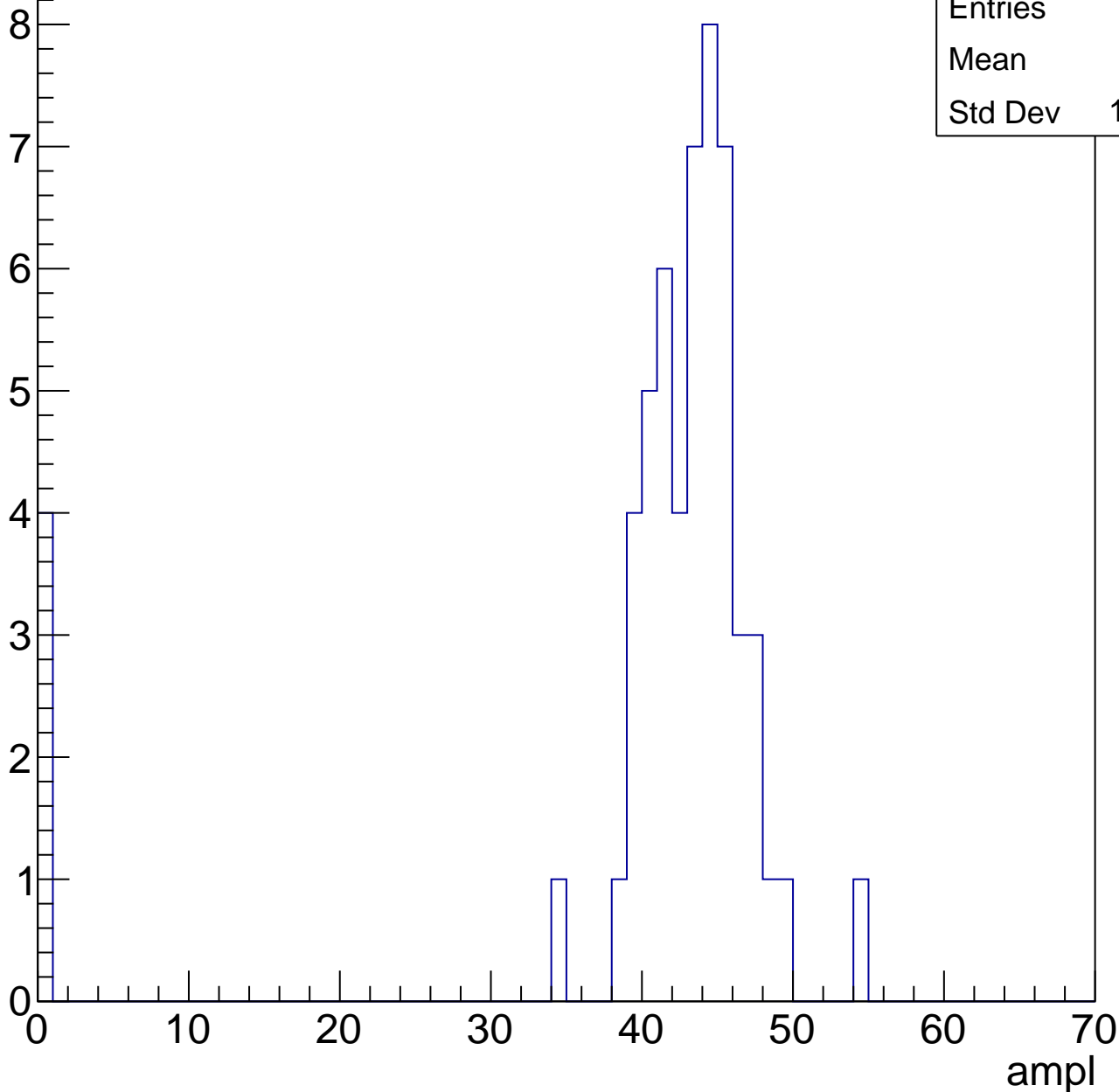


B1L103S, U12-ch24, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	56
Mean	40
Std Dev	11.52

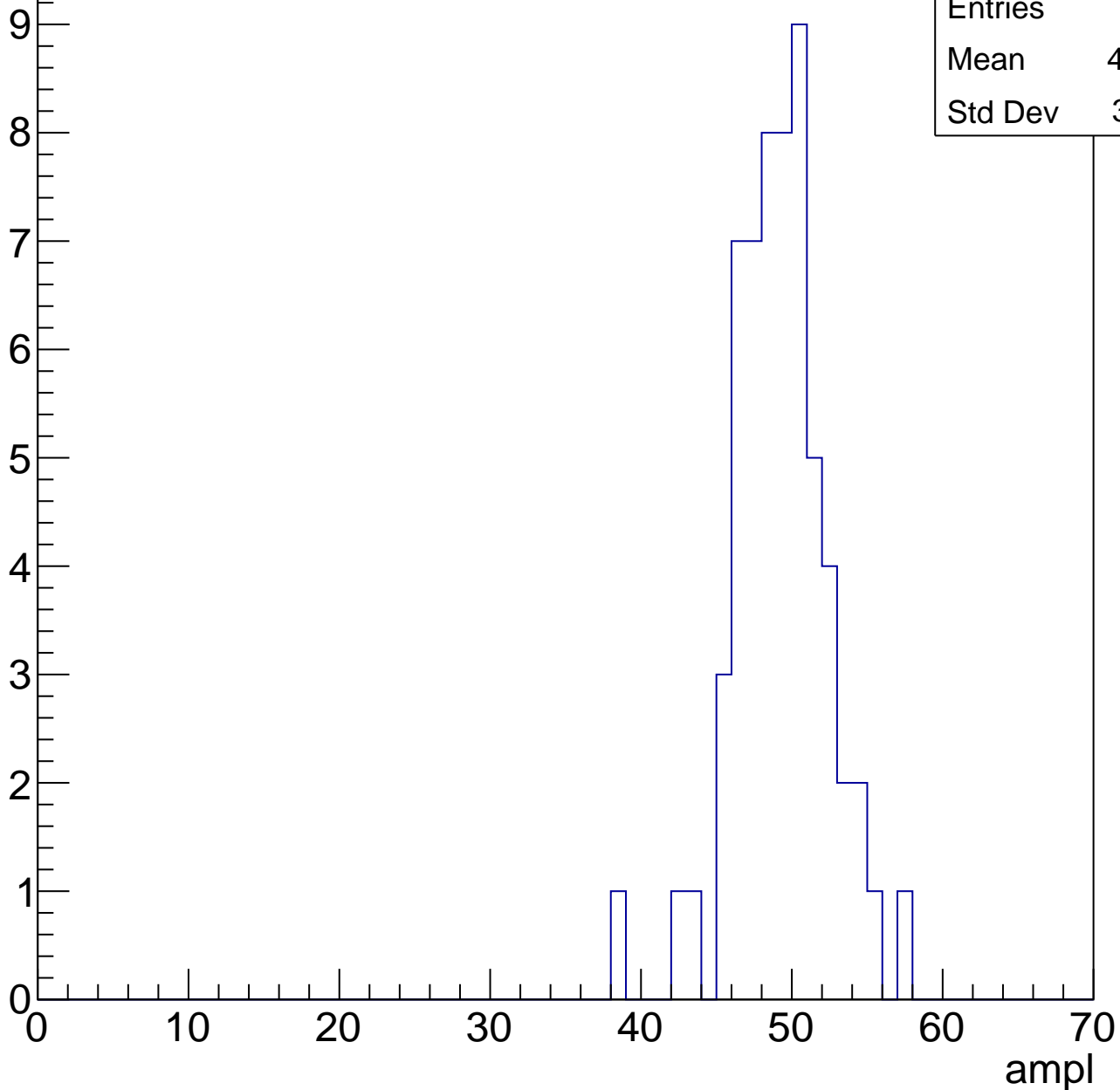


B1L103S, U12-ch24, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	48.73
Std Dev	3.151

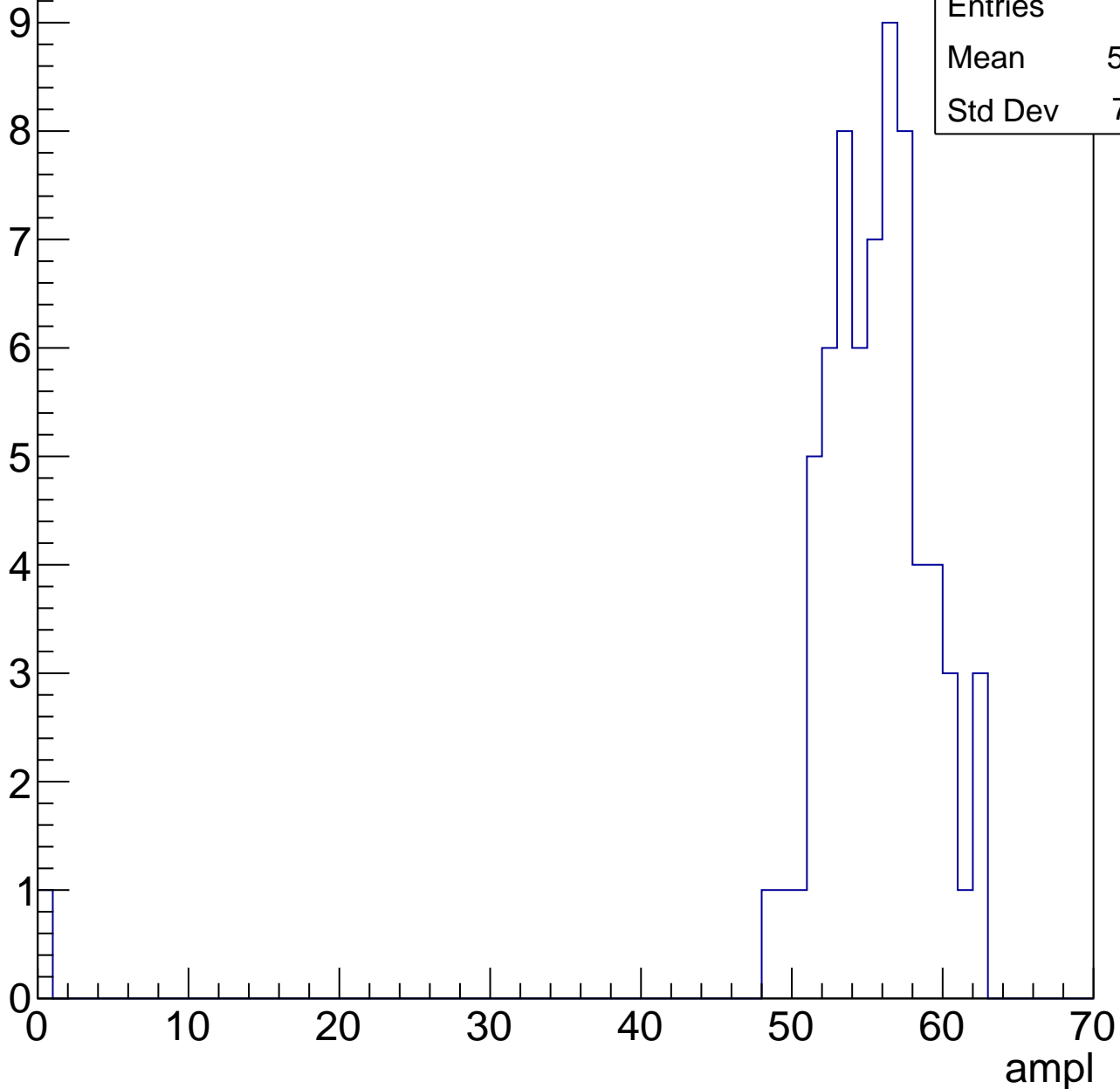


B1L103S, U12-ch24, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

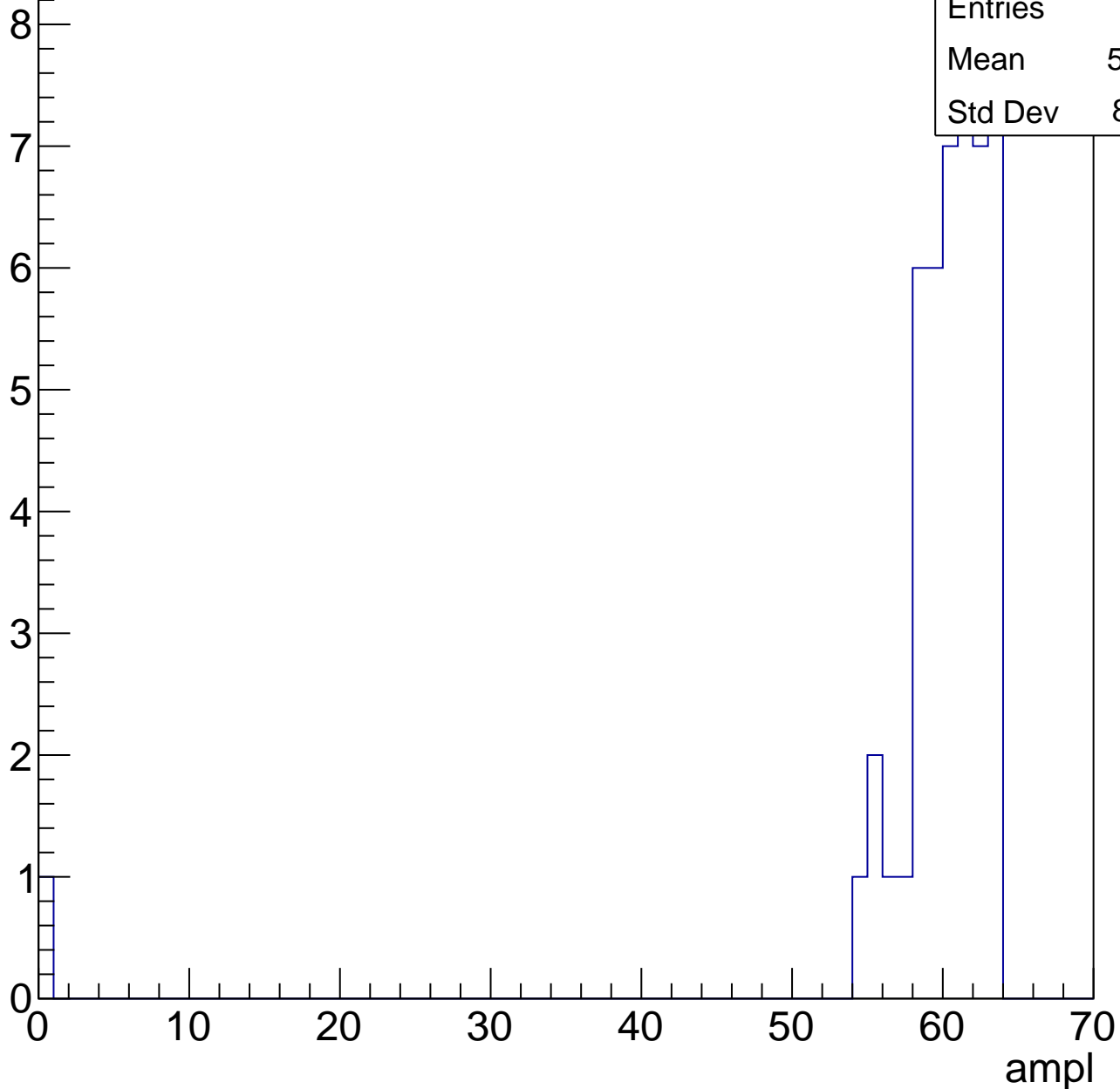
Entries	68
Mean	54.44
Std Dev	7.361



B1L103S, U12-ch24, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch24, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch24, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

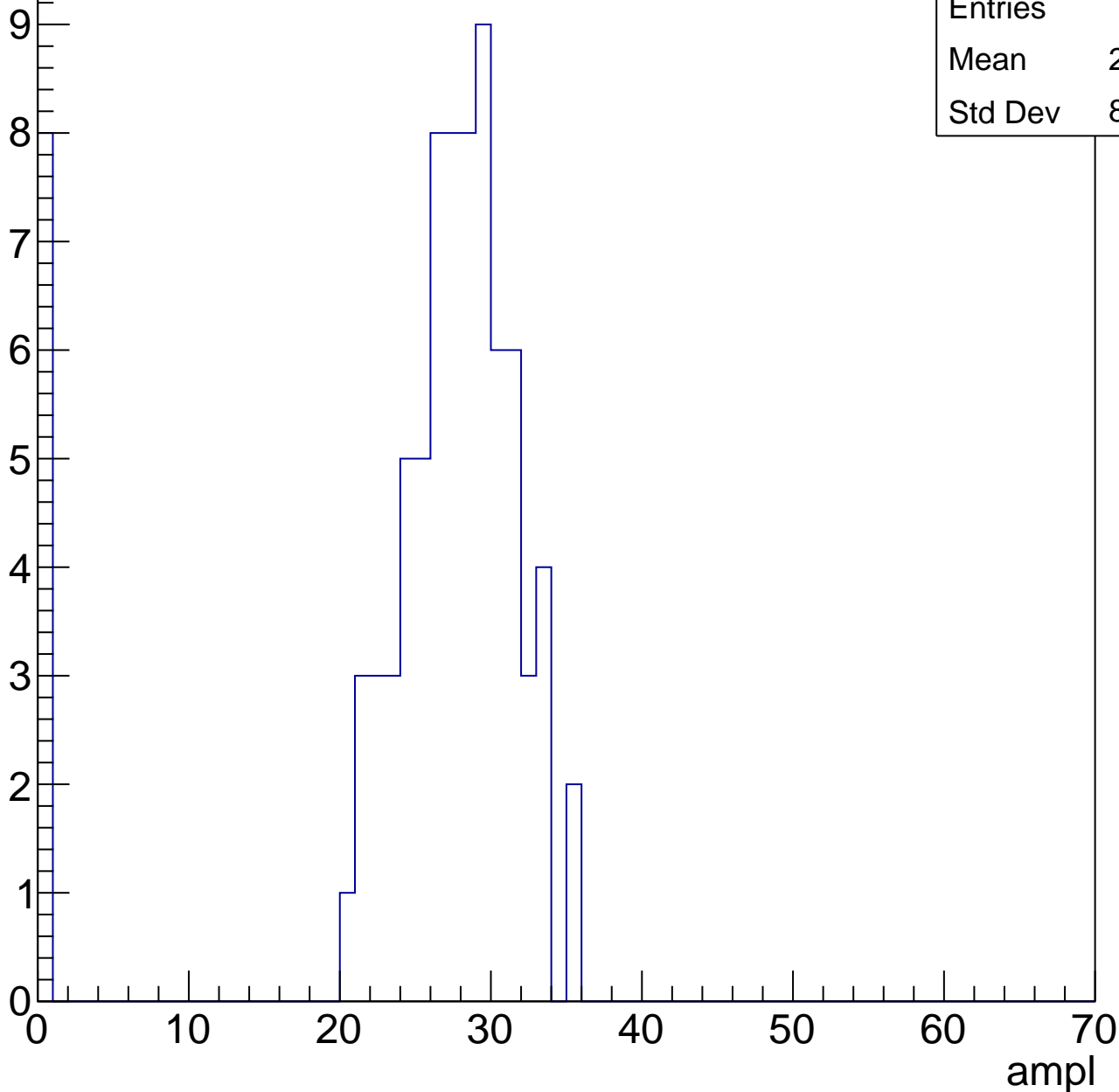
Entries	19
Mean	0
Std Dev	0

B1L103S, U12-ch25, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	82
Mean	24.83
Std Dev	8.793

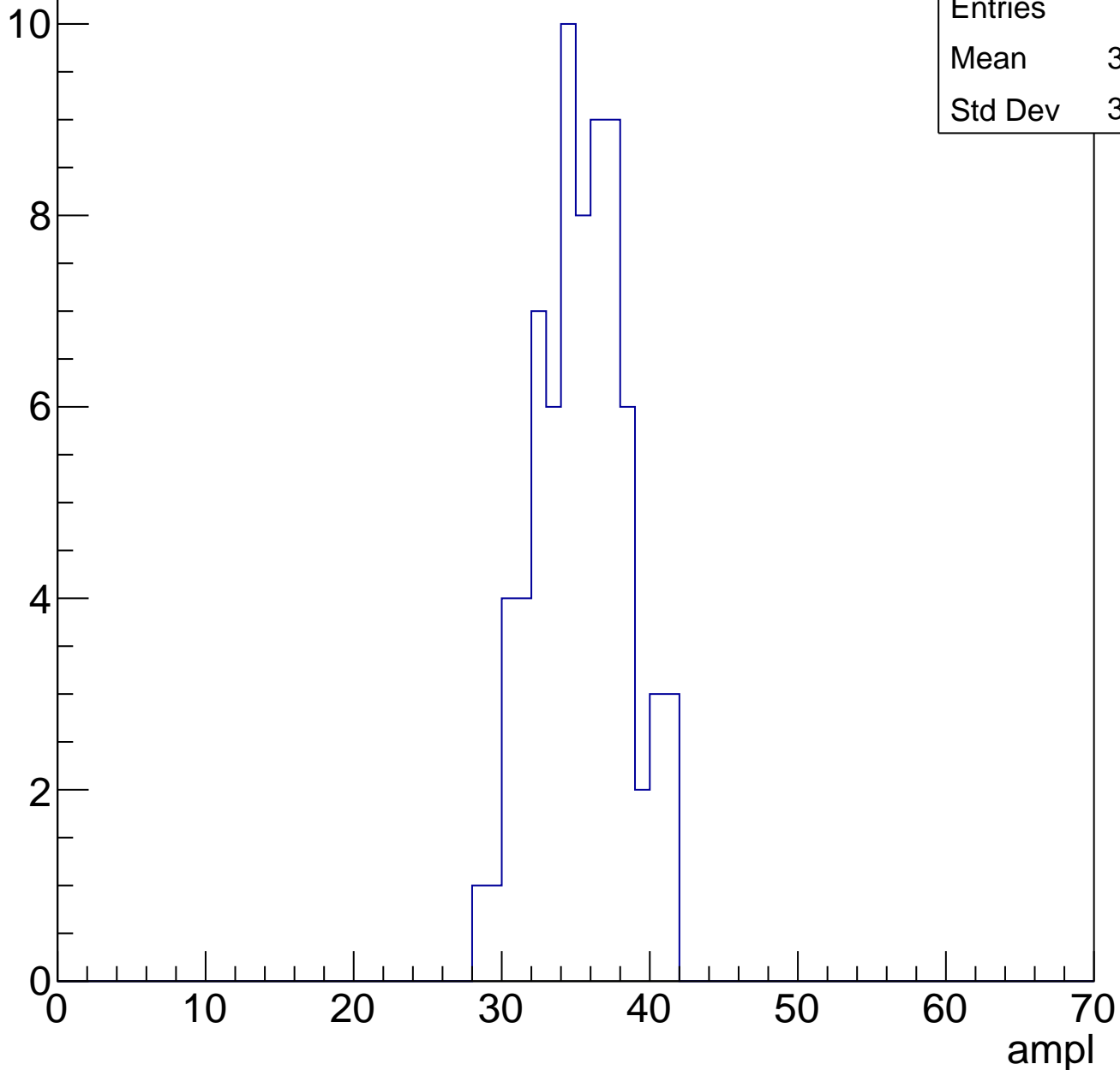


B1L103S, U12-ch25, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	73
Mean	34.92
Std Dev	3.006

Entry

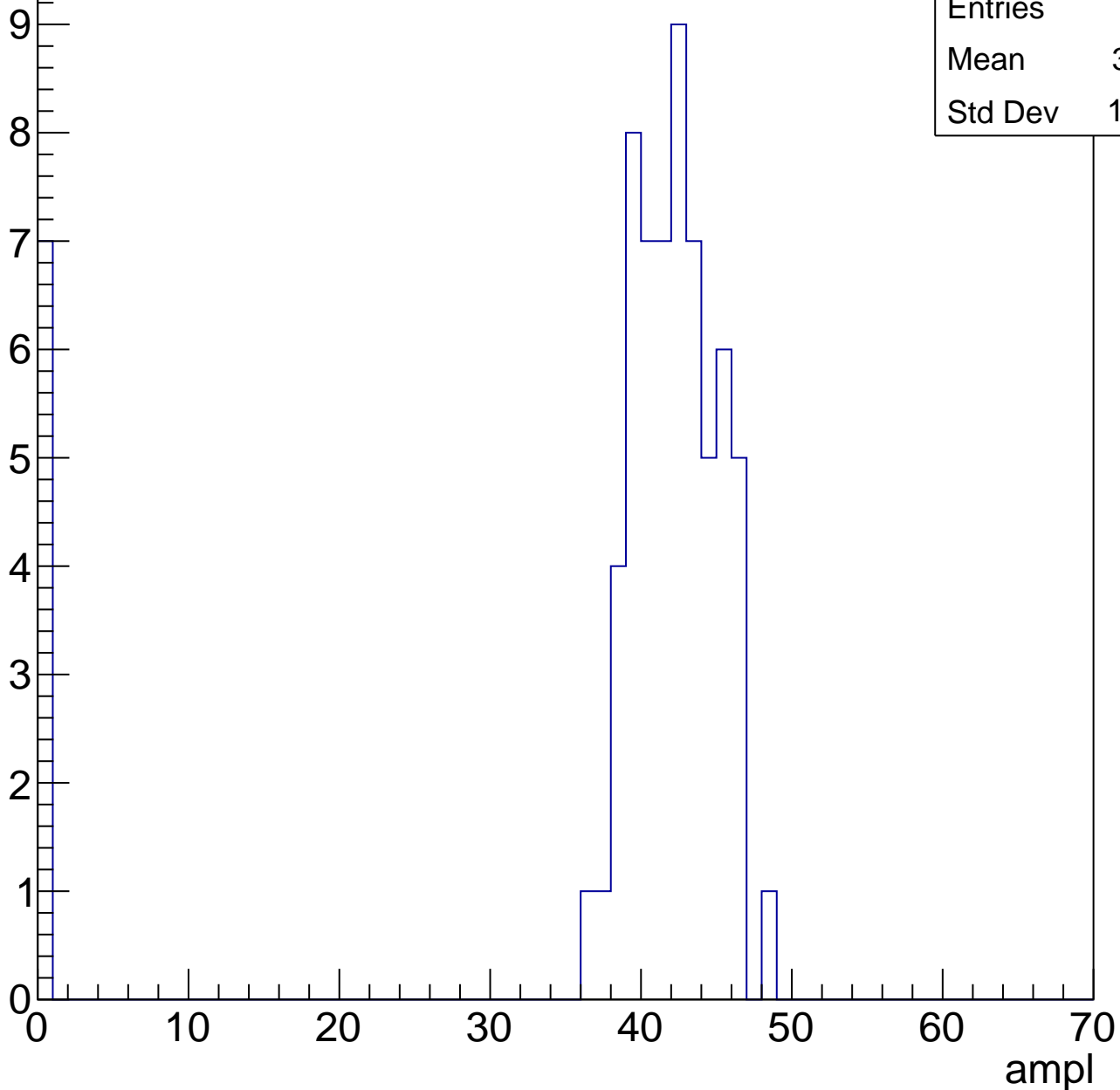


B1L103S, U12-ch25, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	37.51
Std Dev	12.95

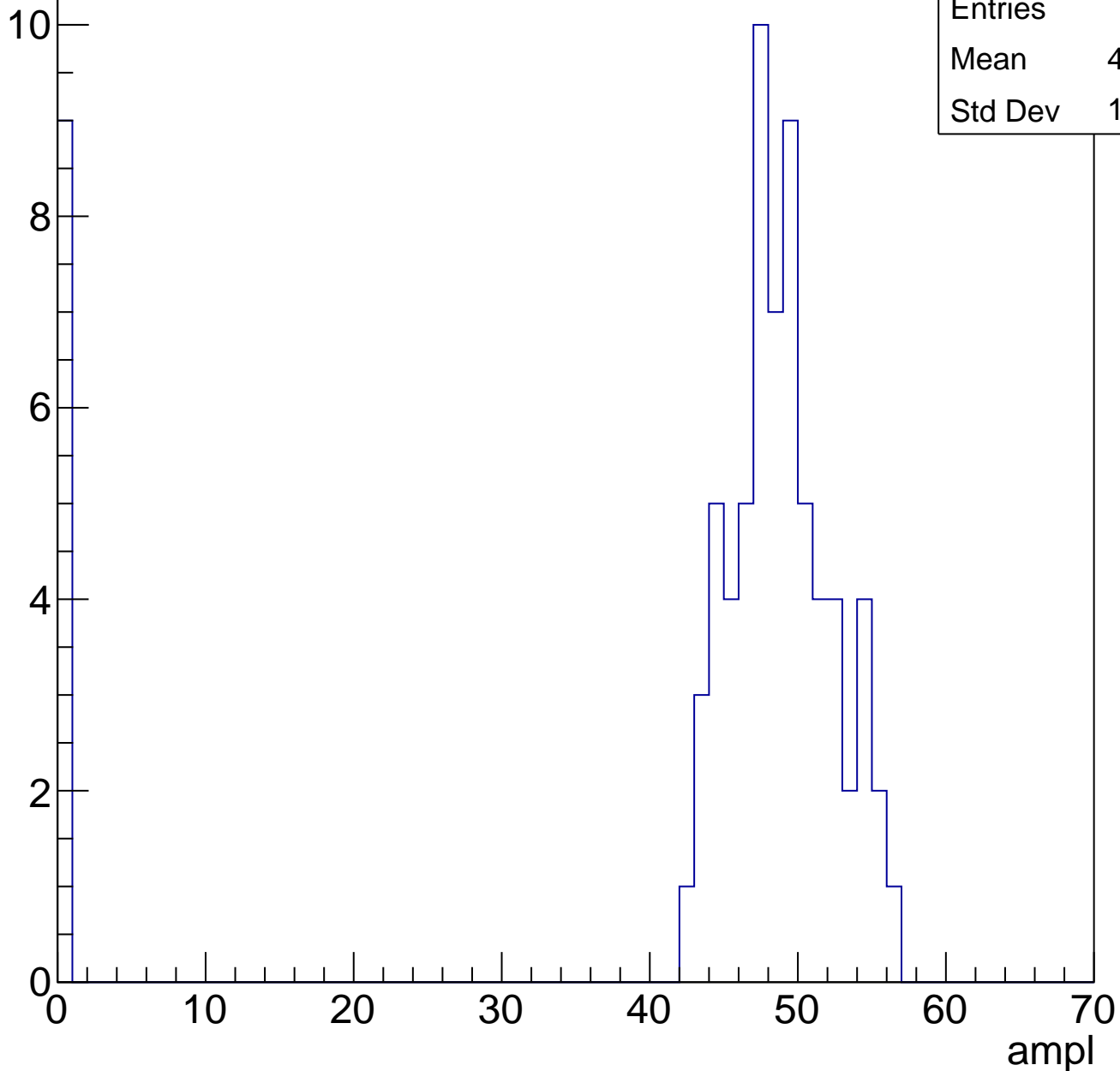


B1L103S, U12-ch25, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	75
Mean	42.64
Std Dev	16.05

Entry

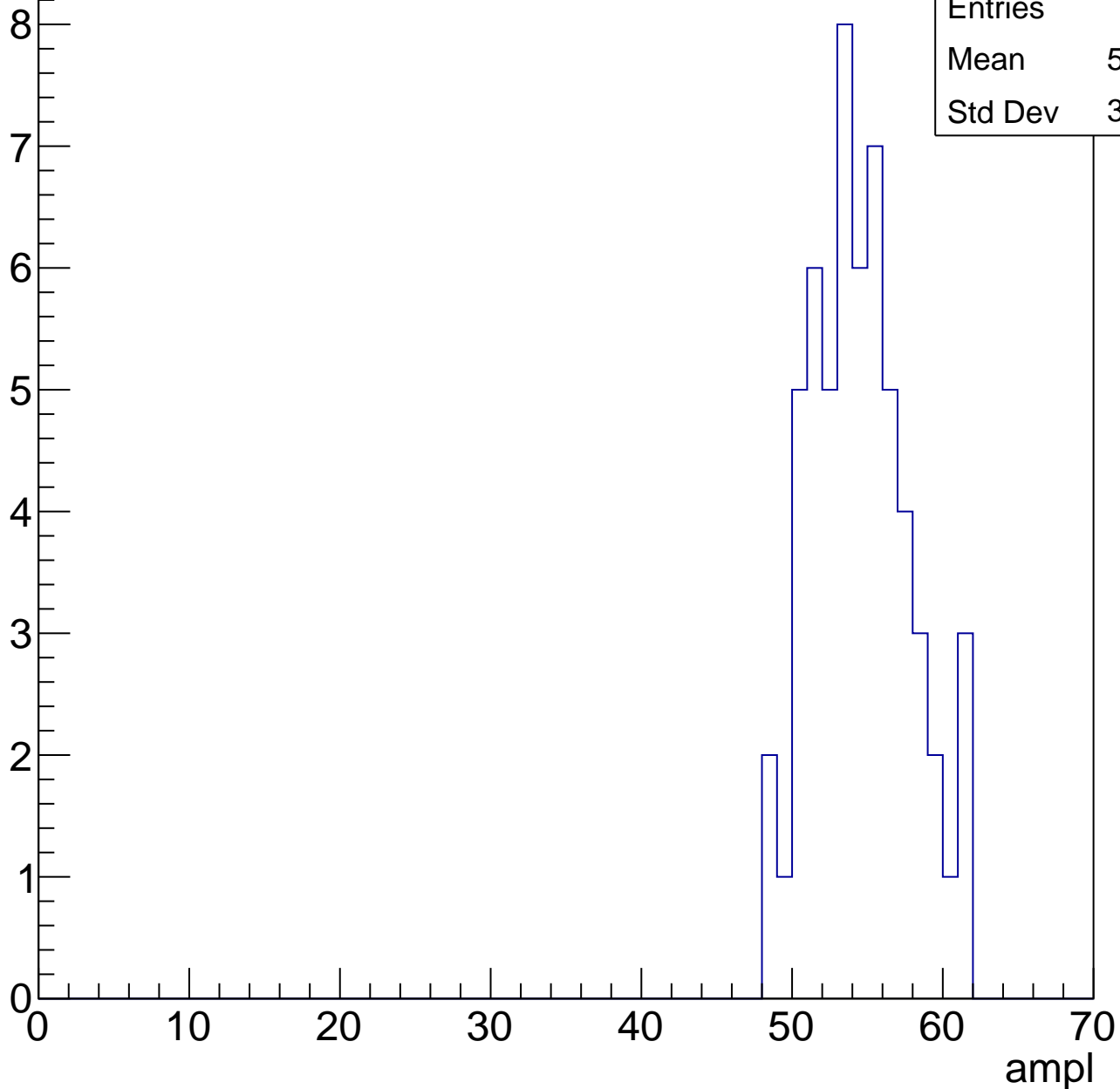


B1L103S, U12-ch25, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

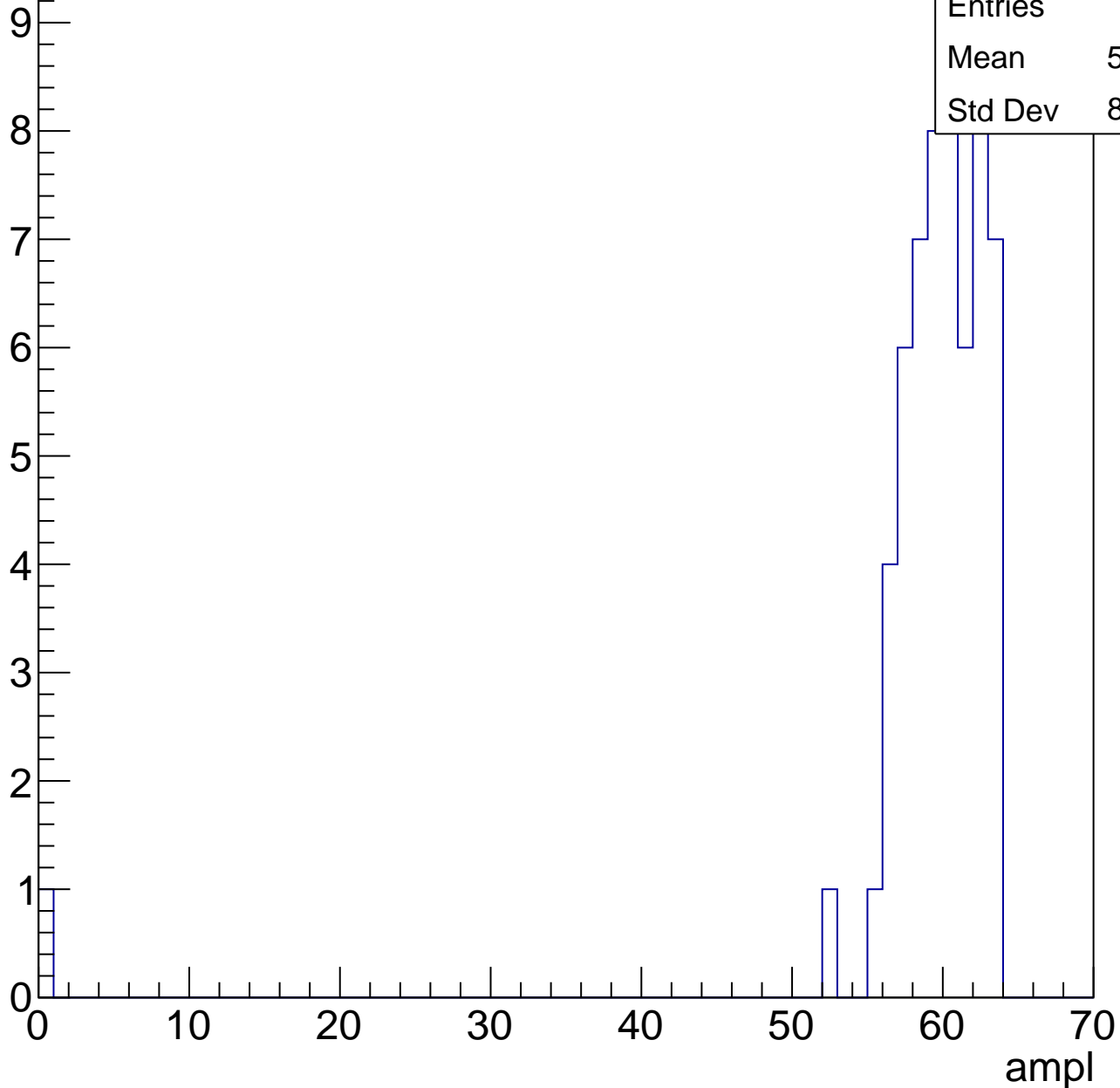
Entries	58
Mean	54.09
Std Dev	3.223



B1L103S, U12-ch25, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch25, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	5
Mean	62.4
Std Dev	0.8

B1L103S, U12-ch25, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

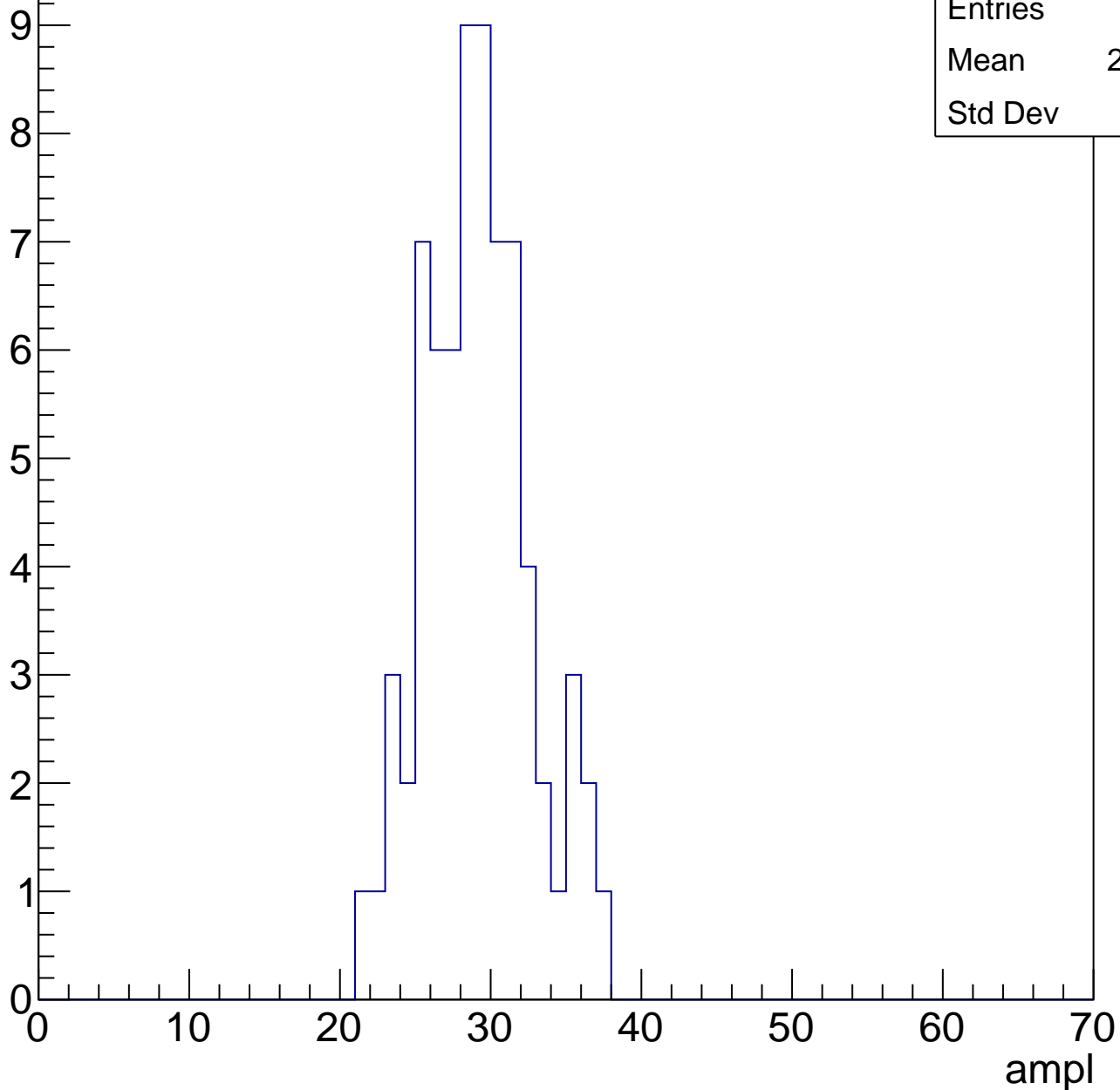


B1L103S, U12-ch26, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	28.66
Std Dev	3.48

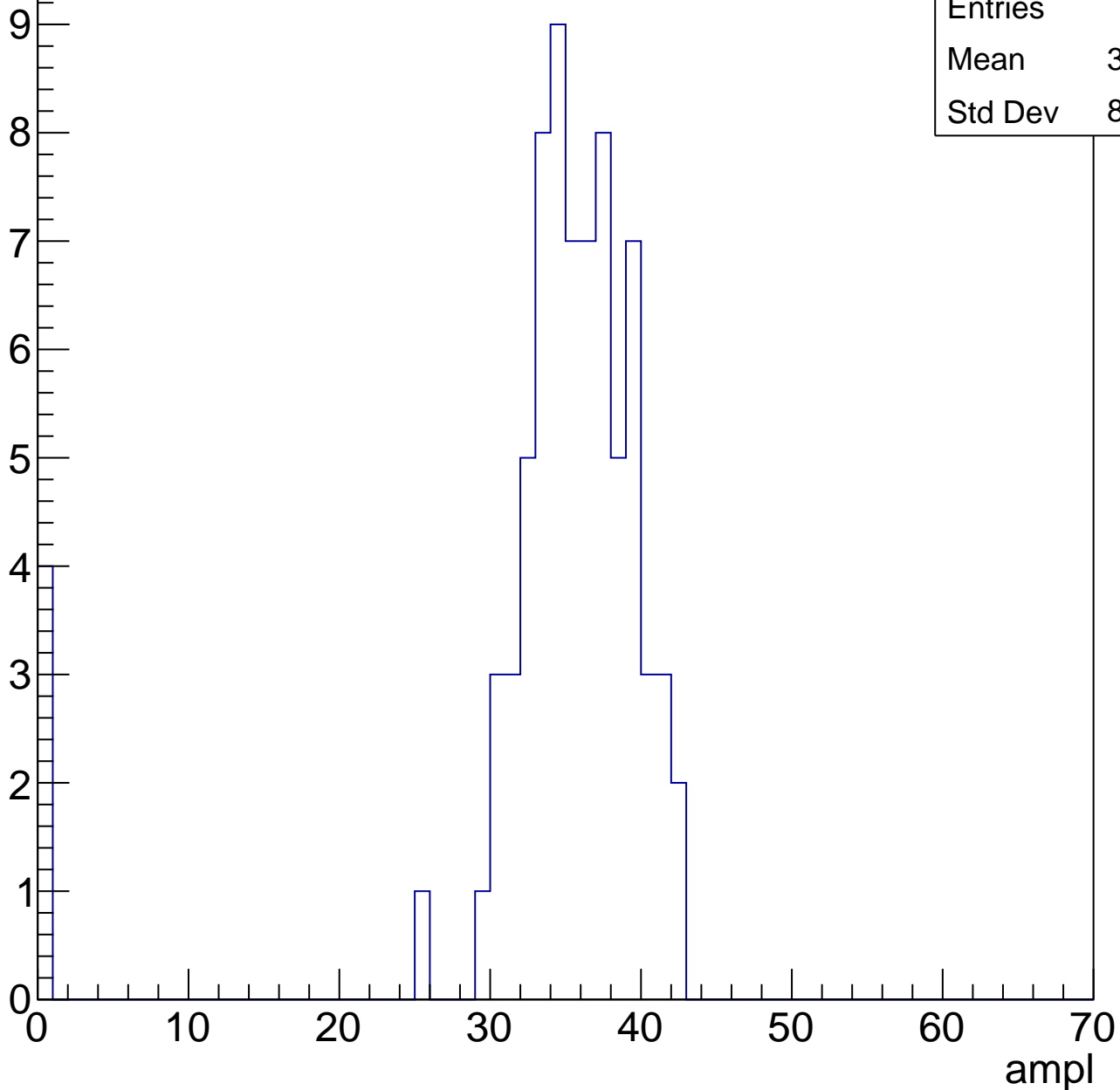


B1L103S, U12-ch26, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	76
Mean	33.55
Std Dev	8.555

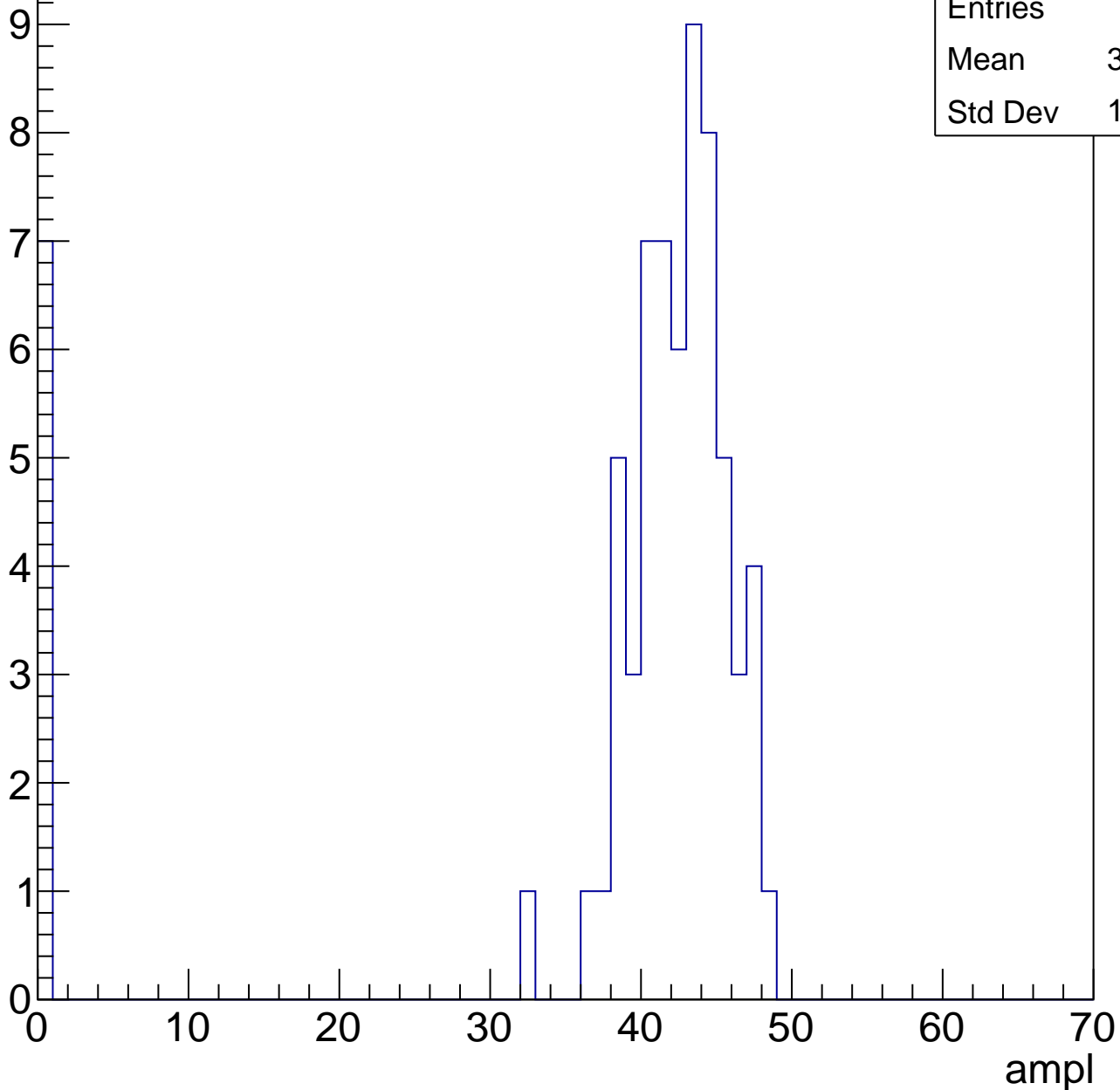


B1L103S, U12-ch26, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

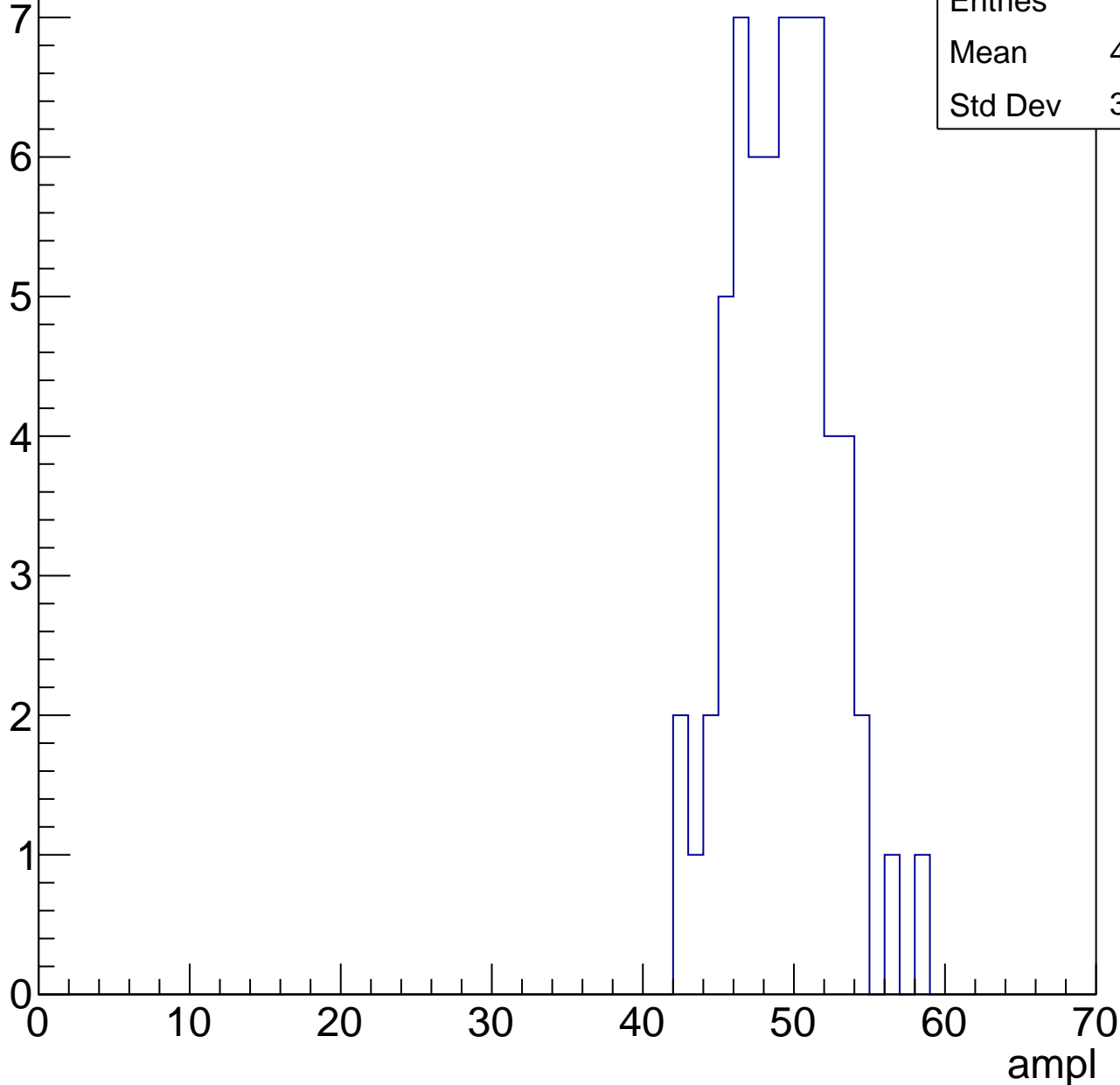
Entries	68
Mean	37.78
Std Dev	13.12



B1L103S, U12-ch26, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

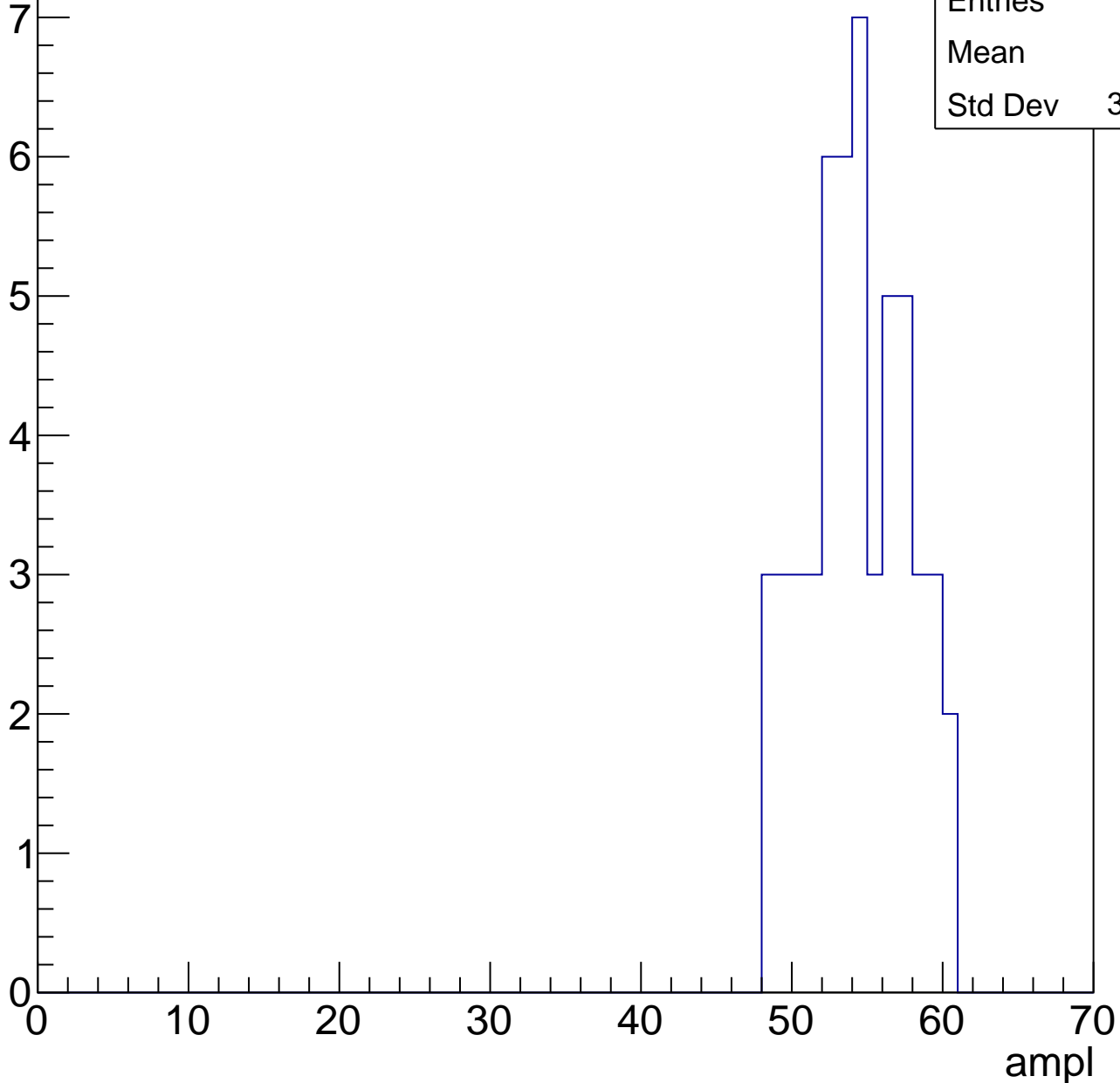


B1L103S, U12-ch26, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	52
Mean	53.9
Std Dev	3.254

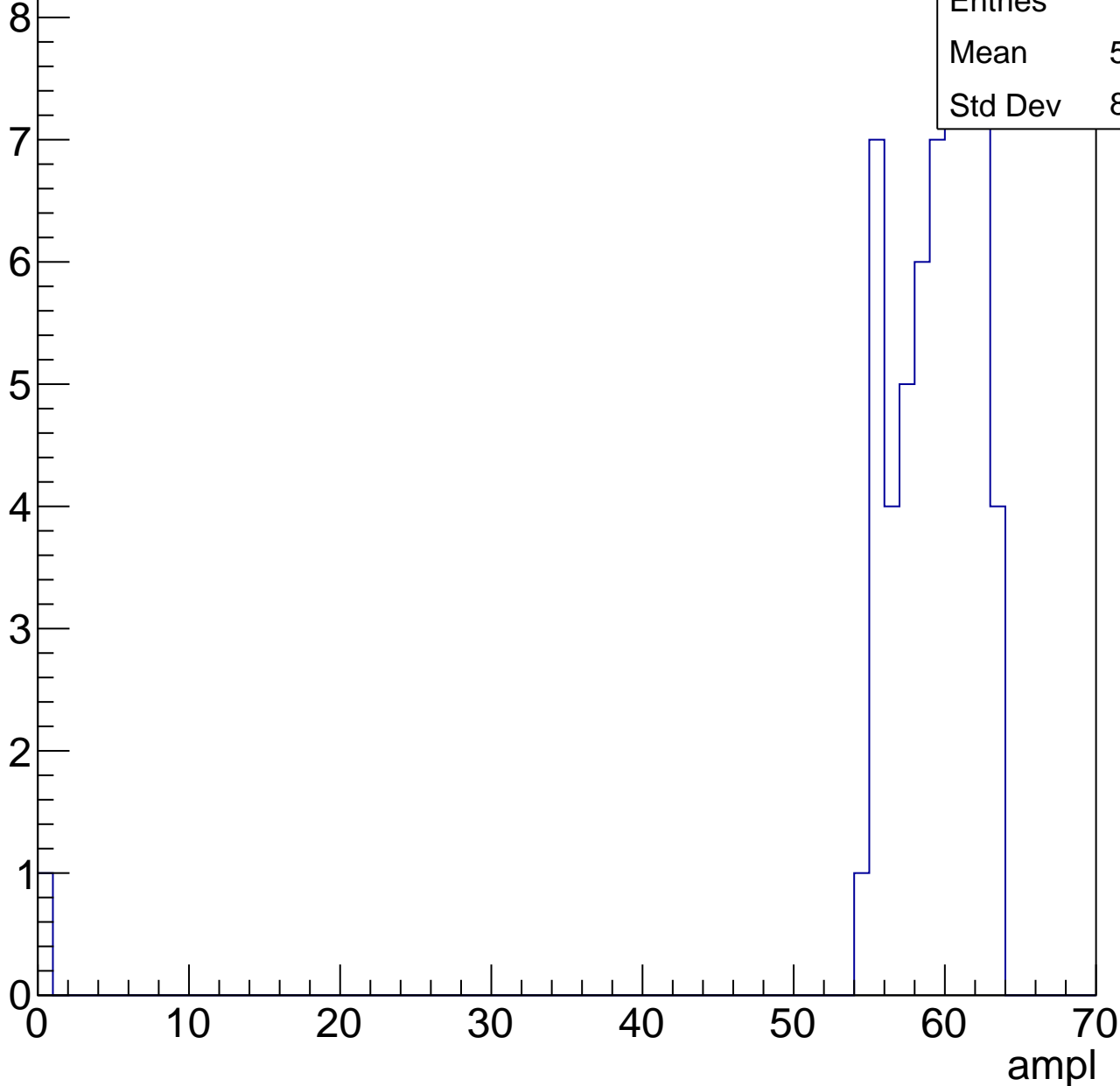


B1L103S, U12-ch26, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	58.05
Std Dev	8.028

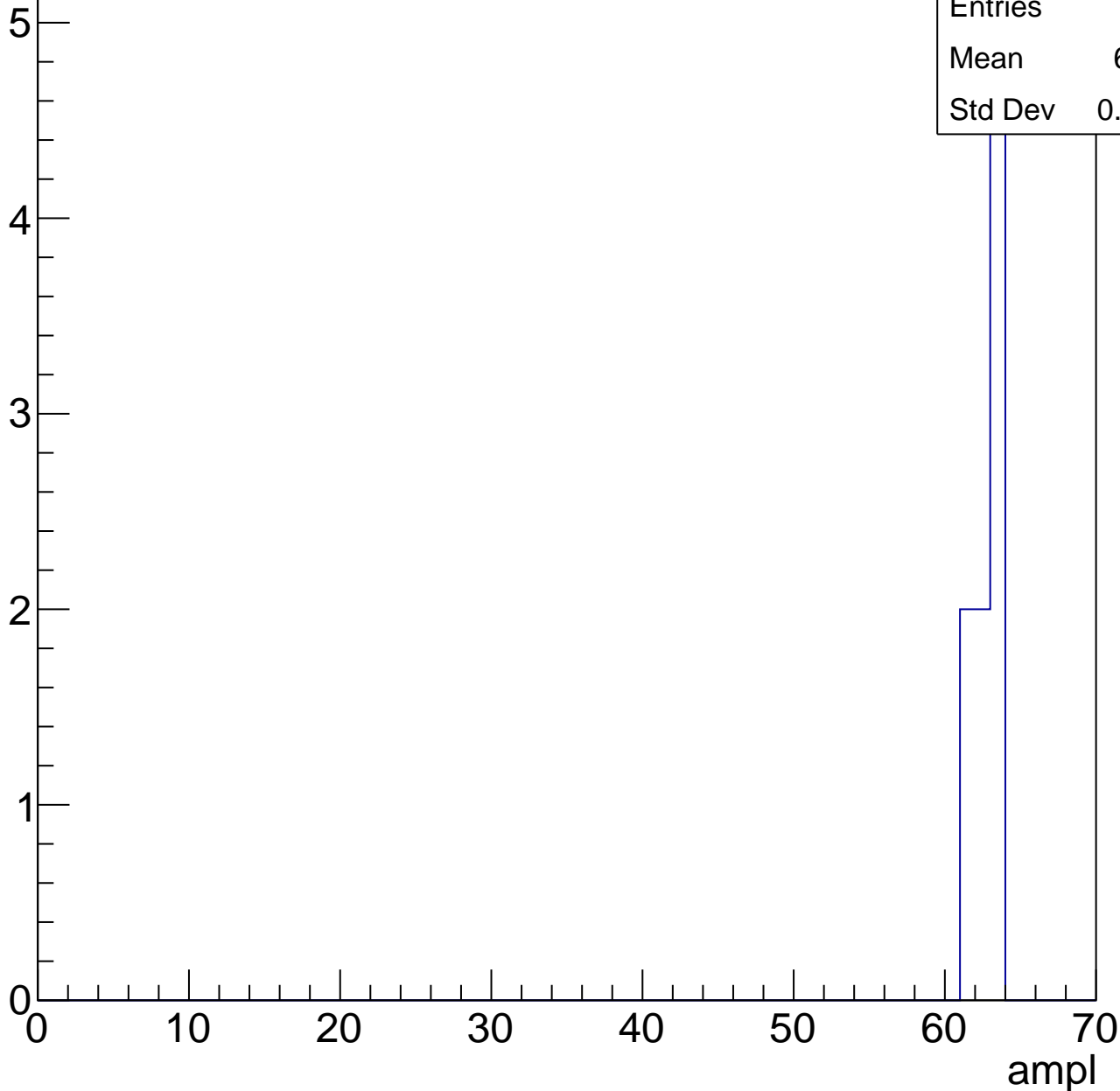


B1L103S, U12-ch26, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	9
Mean	62.33
Std Dev	0.8165

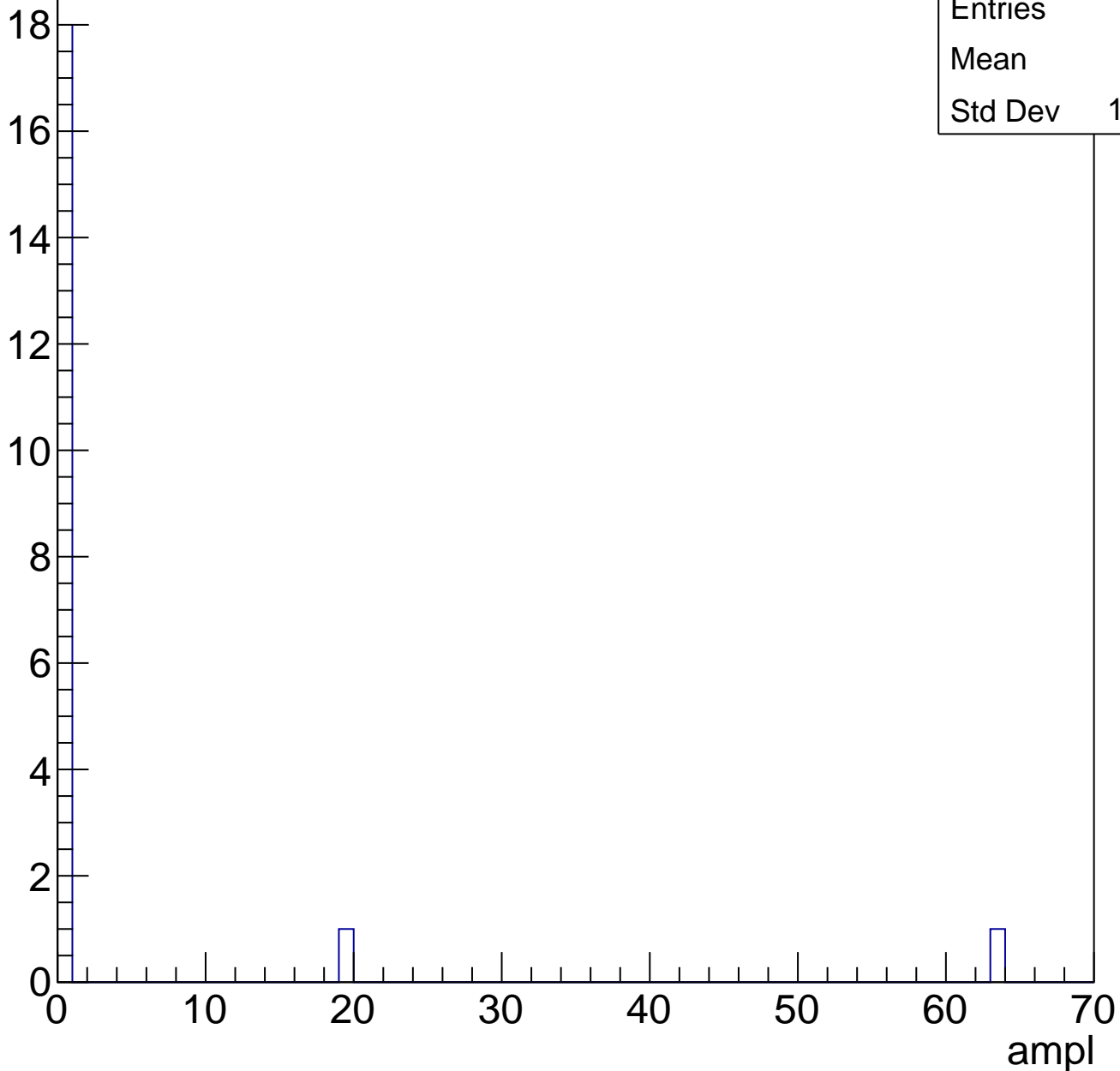


B1L103S, U12-ch26, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	4.1
Std Dev	14.13

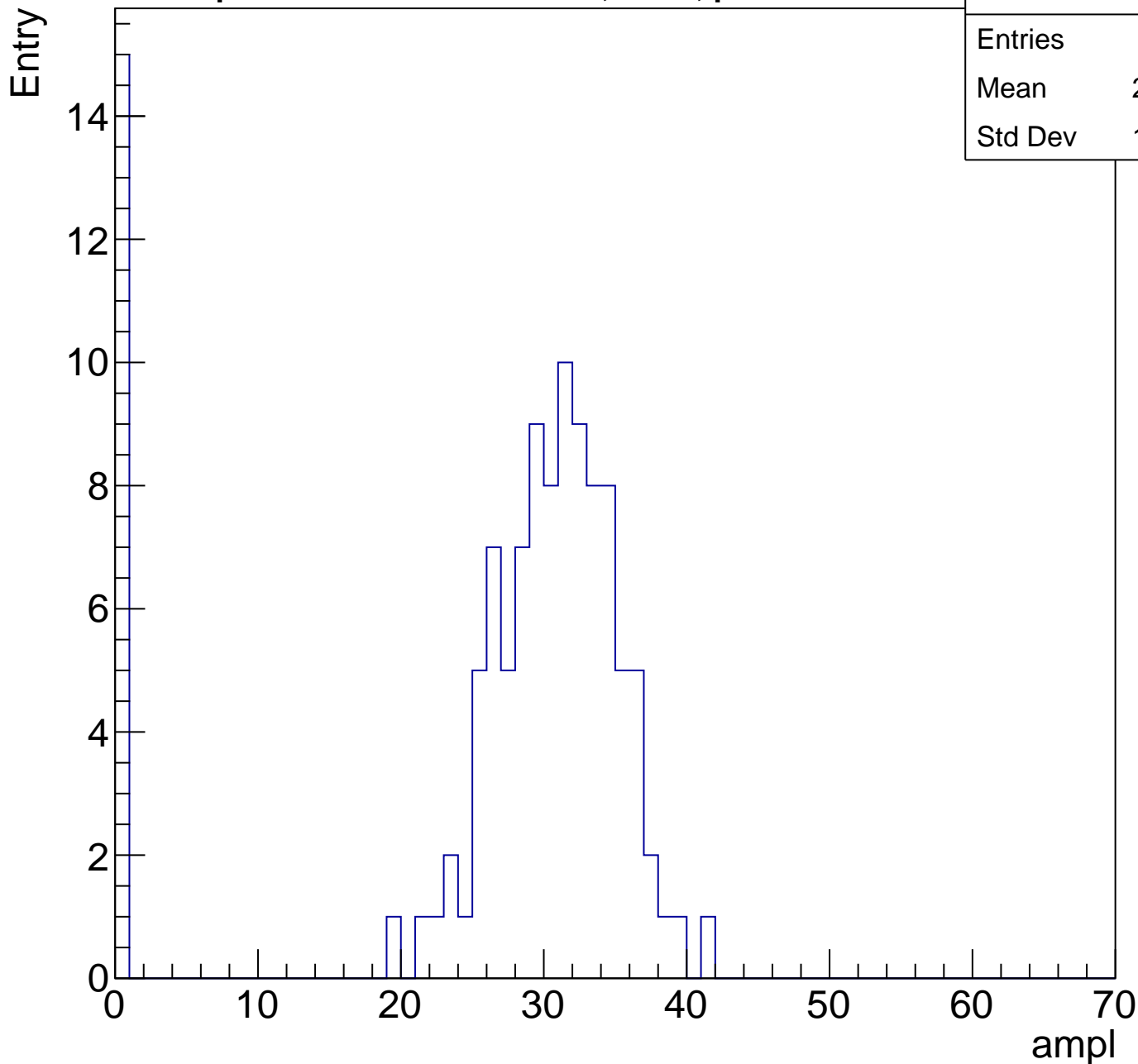
Entry



B1L103S, U12-ch27, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	112
Mean	26.36
Std Dev	11.04

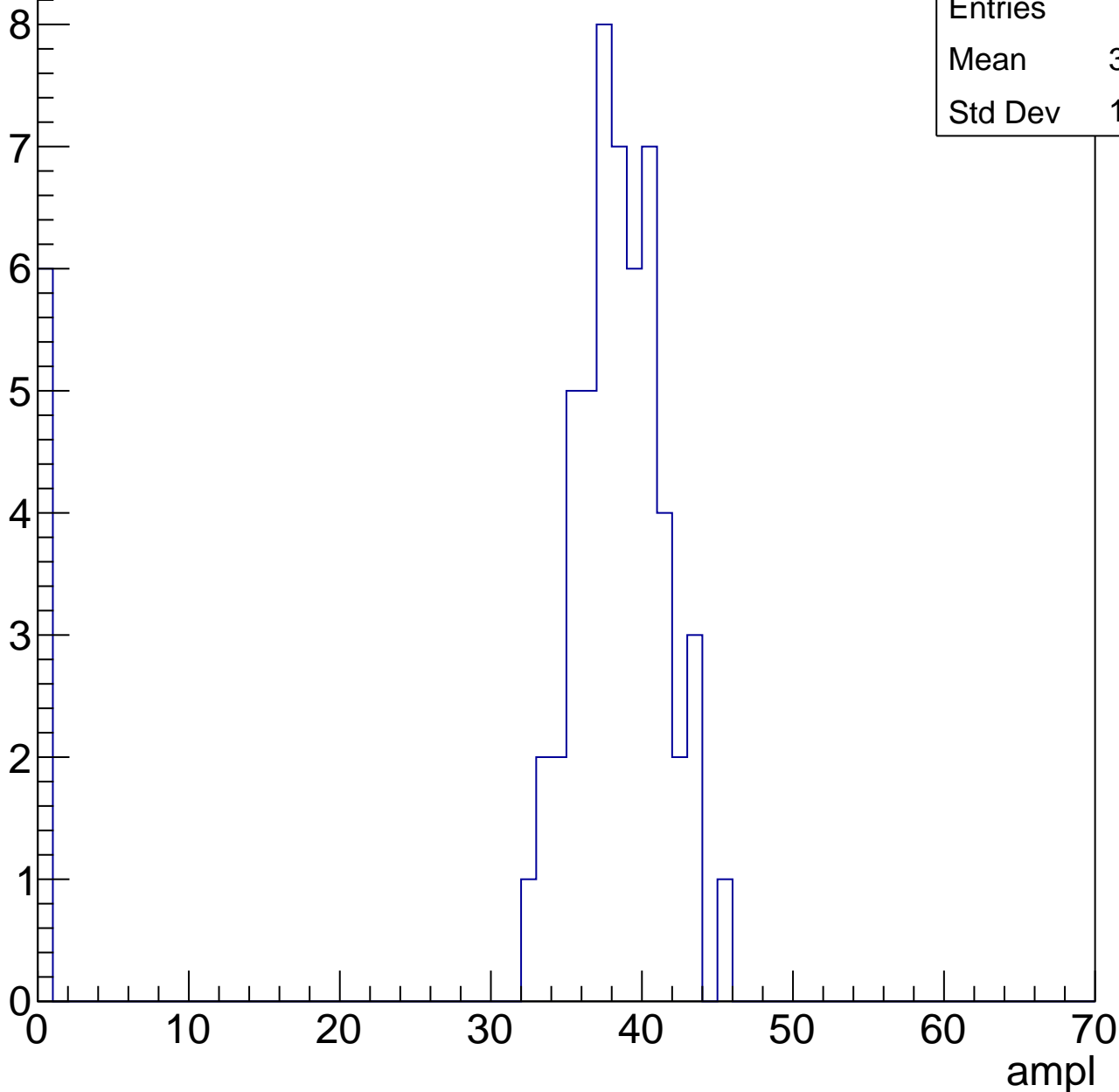


B1L103S, U12-ch27, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	34.22
Std Dev	11.82

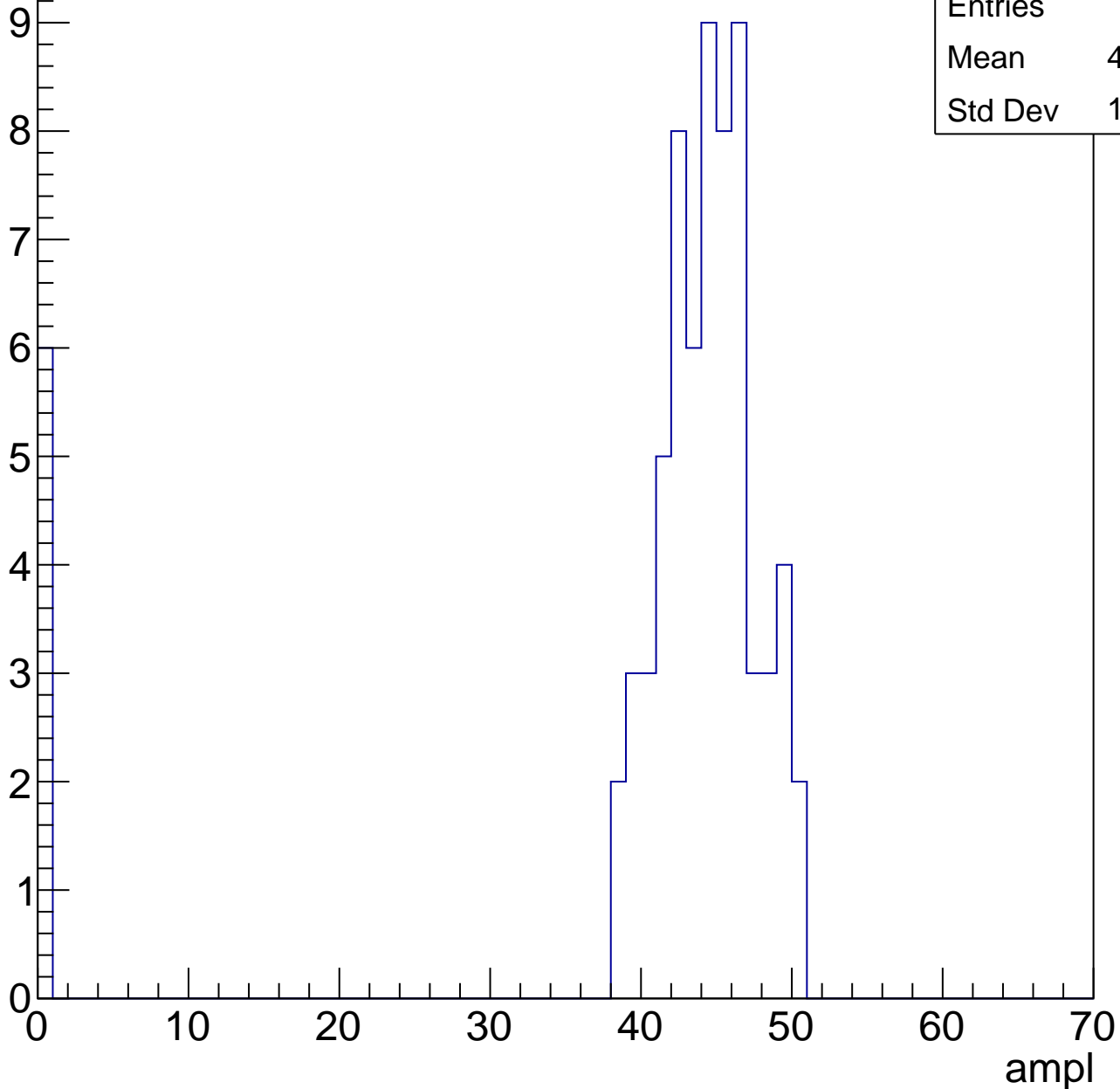


B1L103S, U12-ch27, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	40.32
Std Dev	12.57

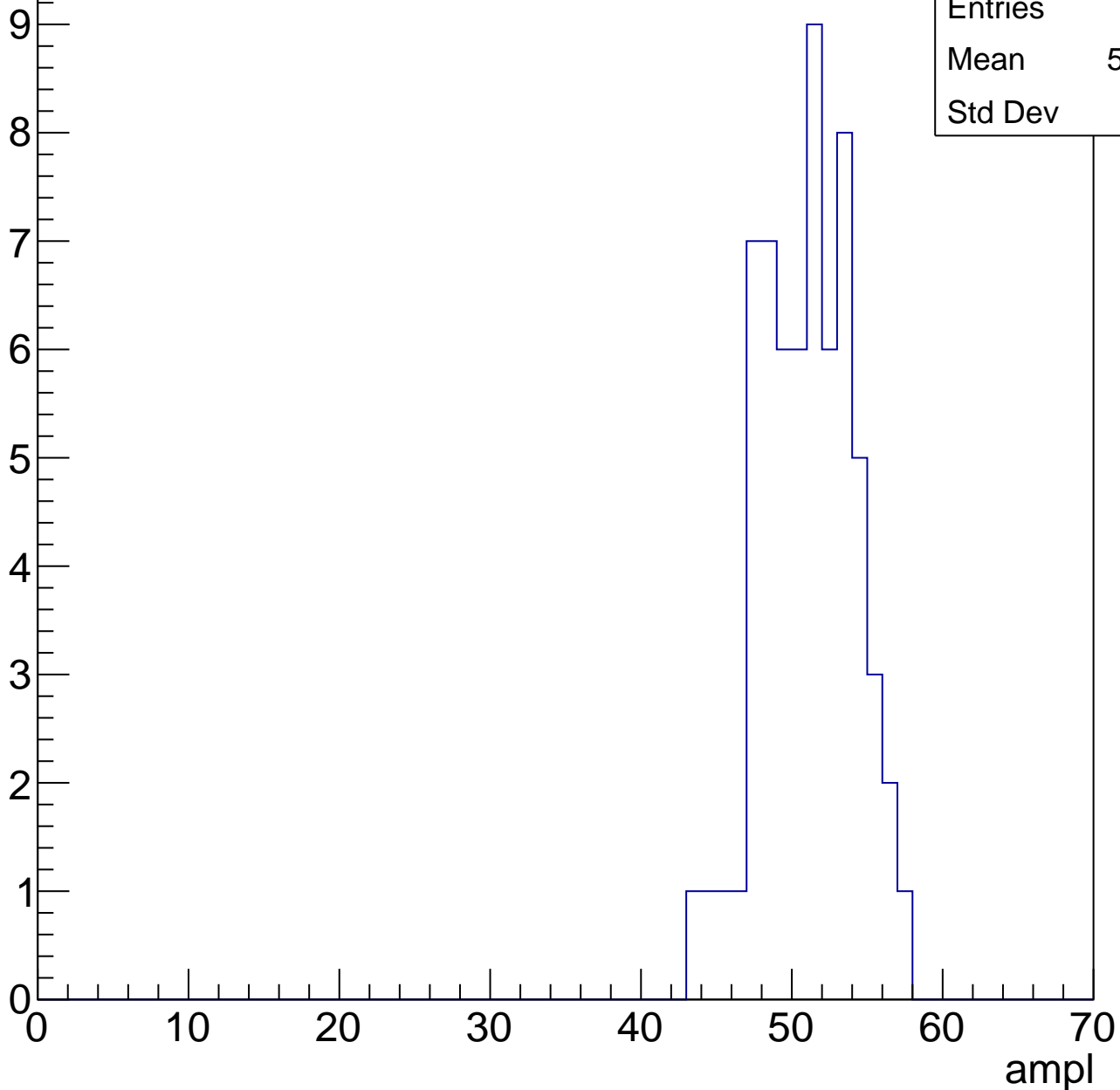


B1L103S, U12-ch27, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

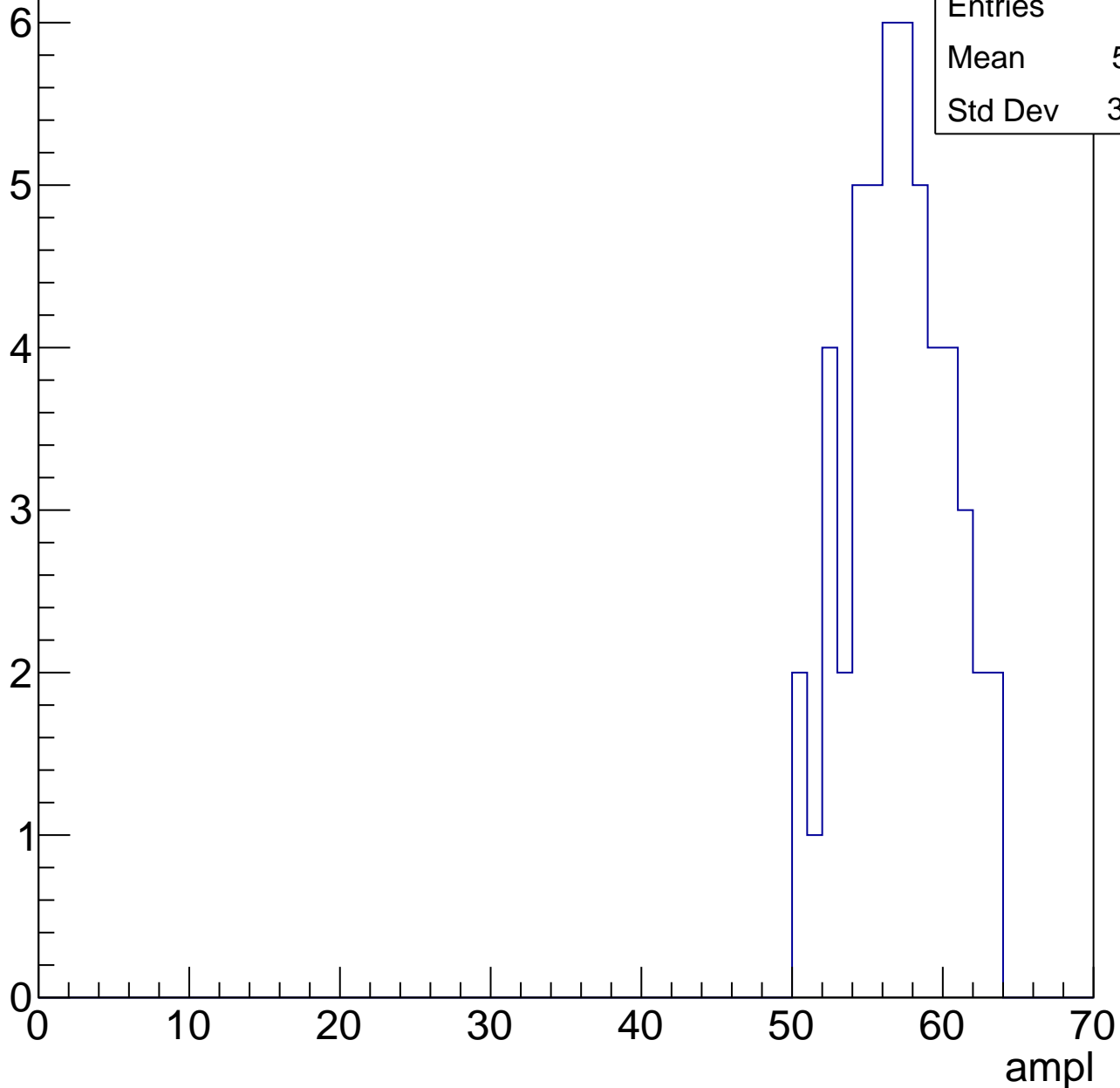
Entries	64
Mean	50.56
Std Dev	3.02



B1L103S, U12-ch27, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

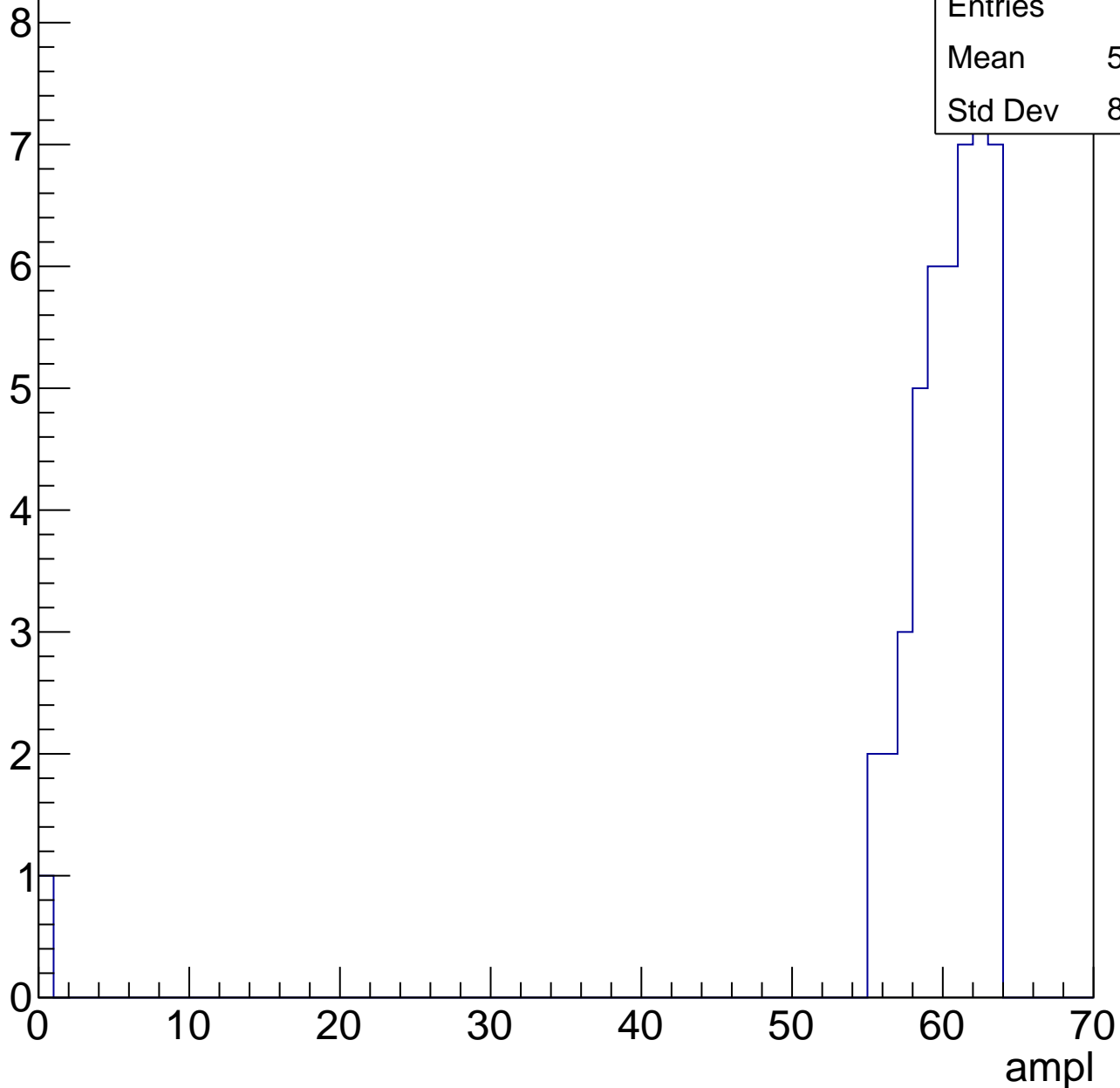


B1L103S, U12-ch27, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	47
Mean	58.74
Std Dev	8.948



B1L103S, U12-ch27, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch27, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

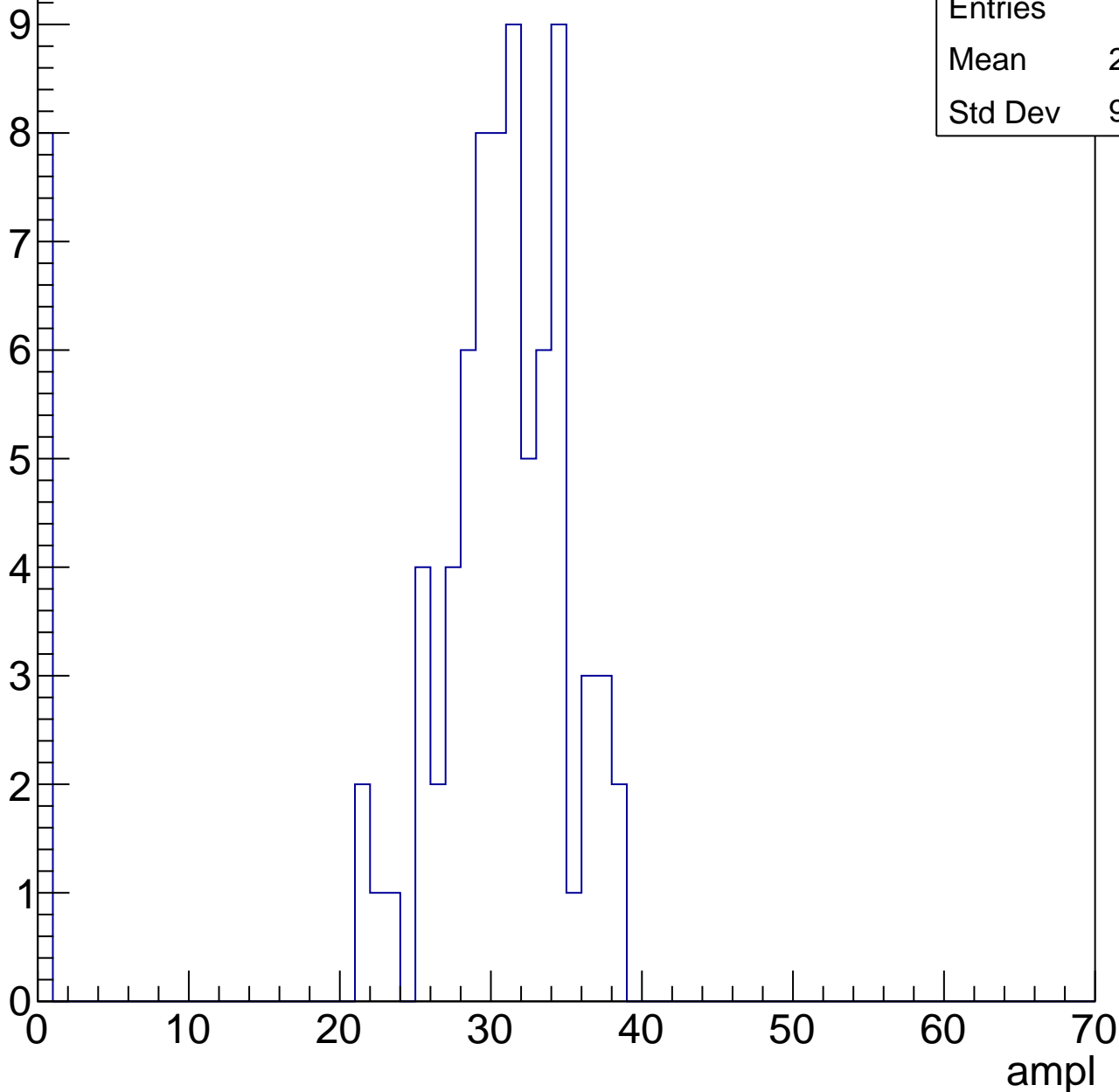
Entries	19
Mean	0
Std Dev	0

B1L103S, U12-ch28, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	82
Mean	27.56
Std Dev	9.767

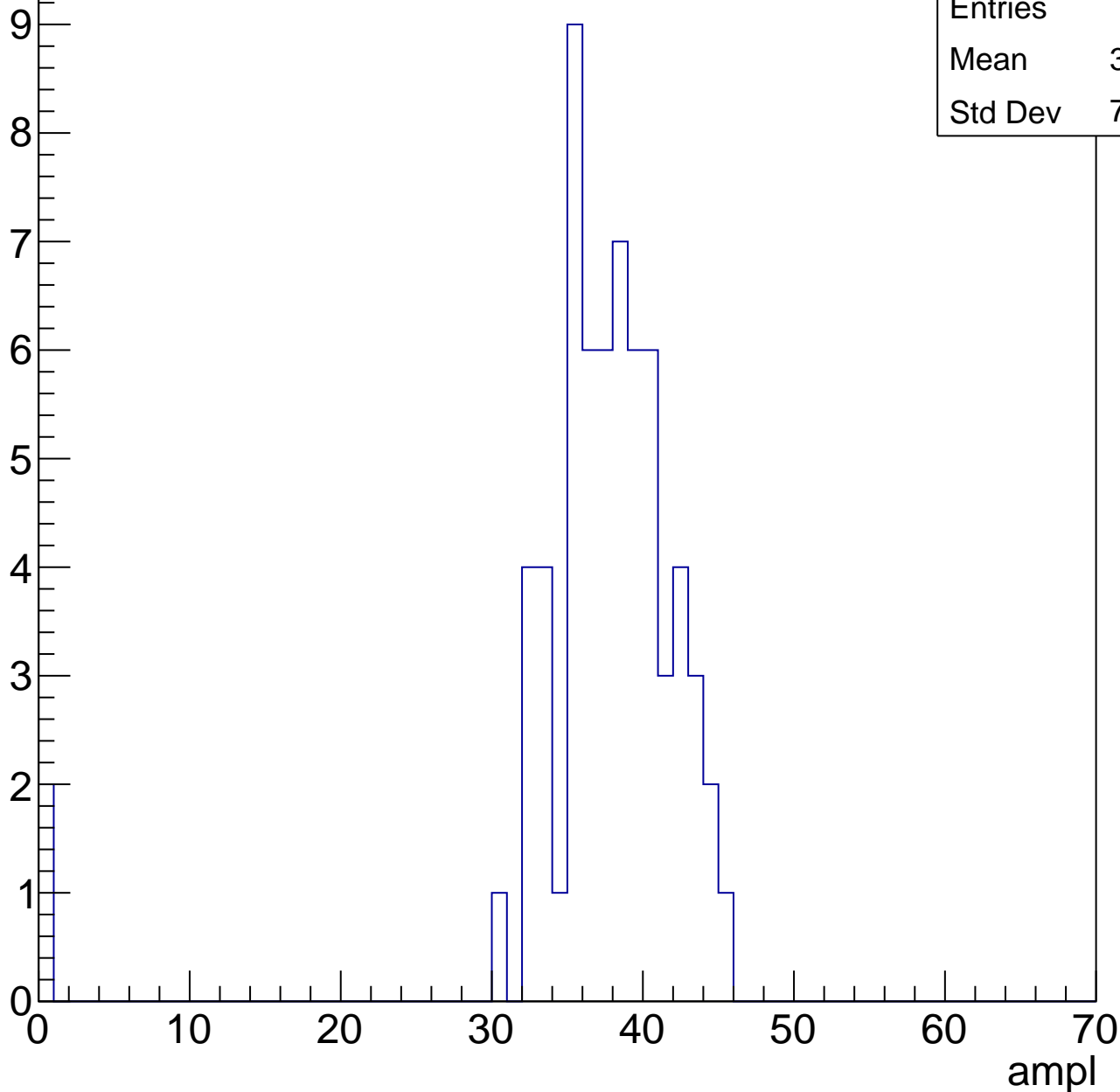


B1L103S, U12-ch28, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

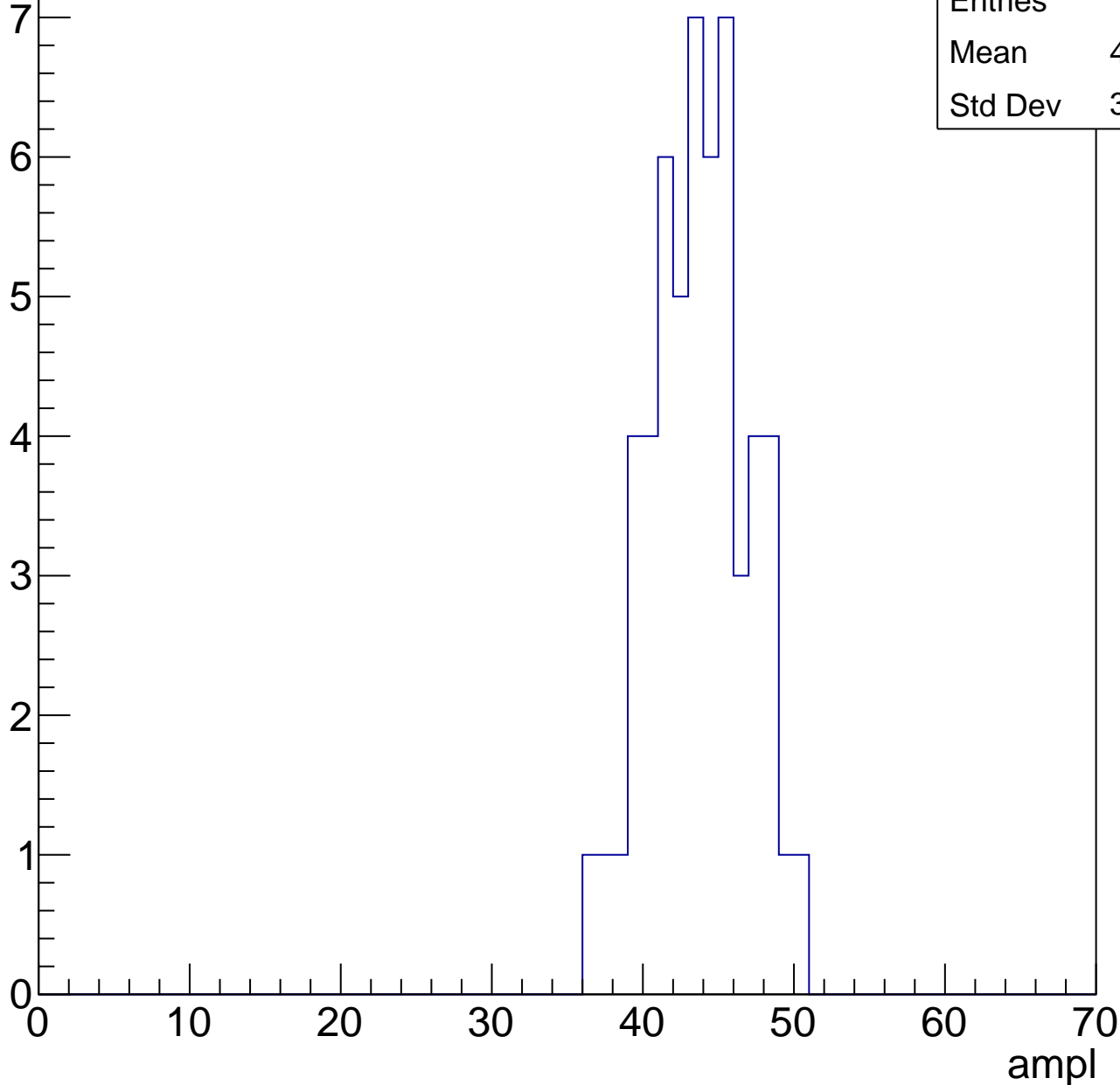
Entries	65
Mean	36.46
Std Dev	7.323



B1L103S, U12-ch28, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

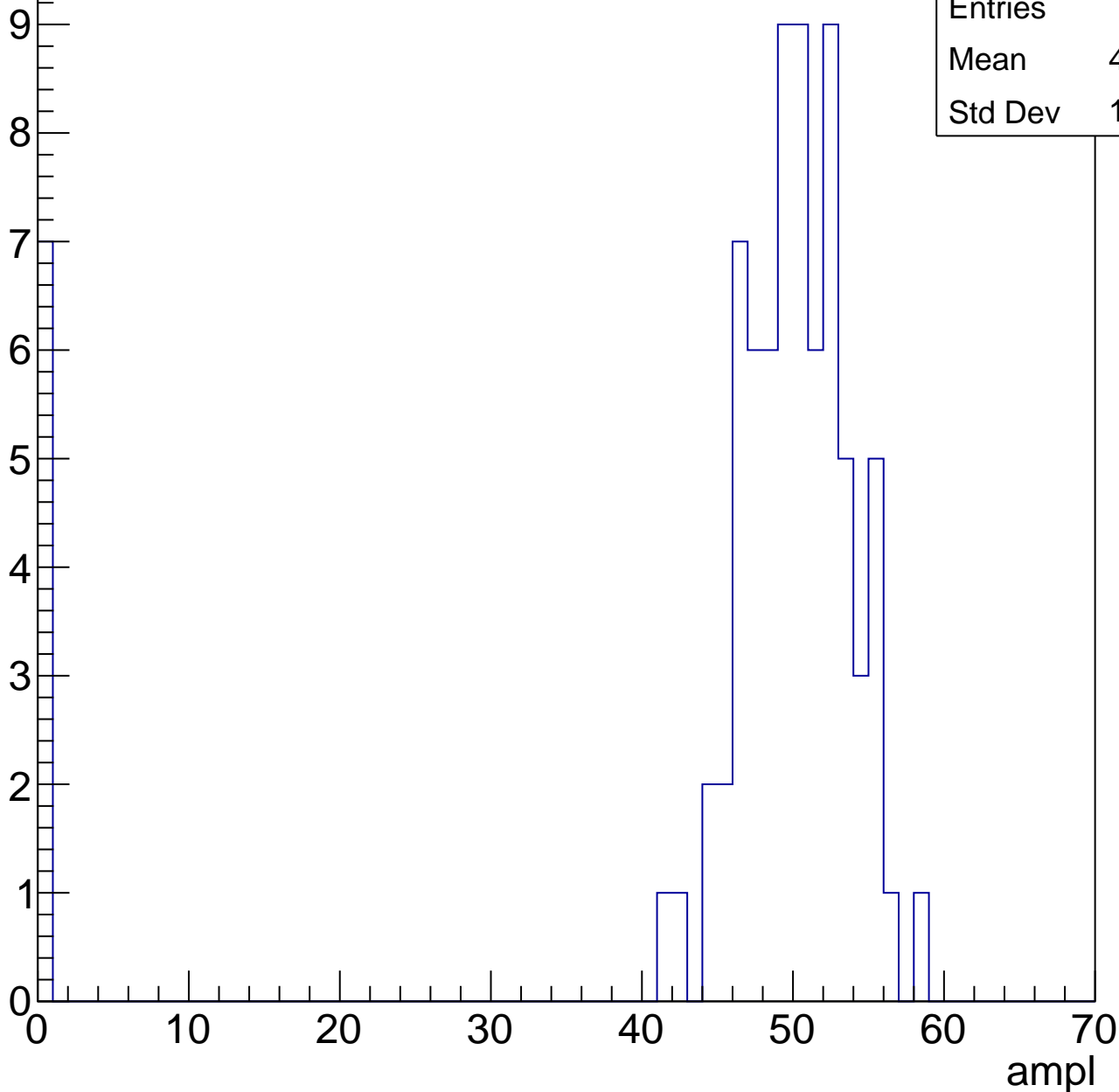


B1L103S, U12-ch28, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	80
Mean	45.42
Std Dev	14.43

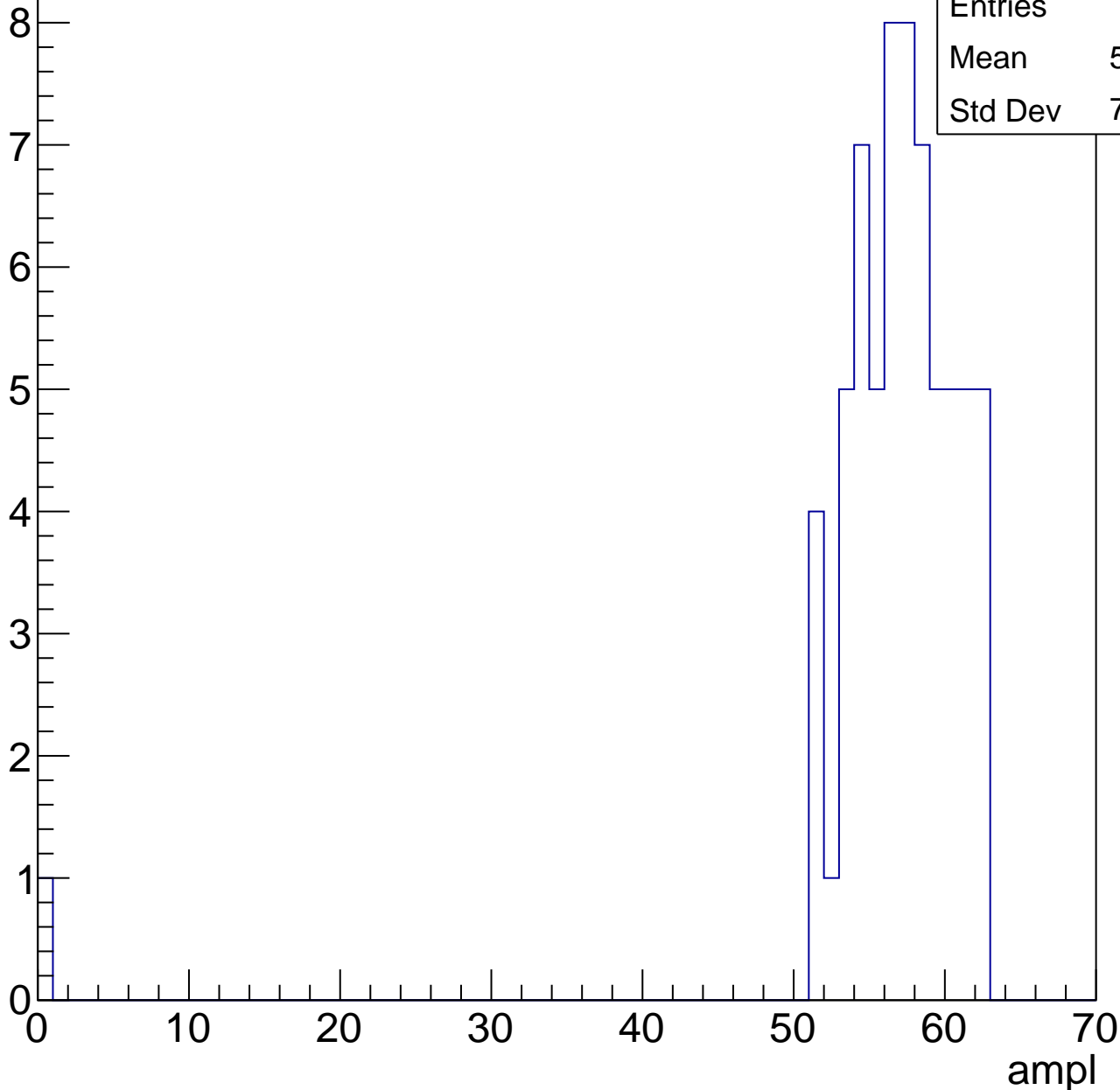


B1L103S, U12-ch28, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	55.97
Std Dev	7.584

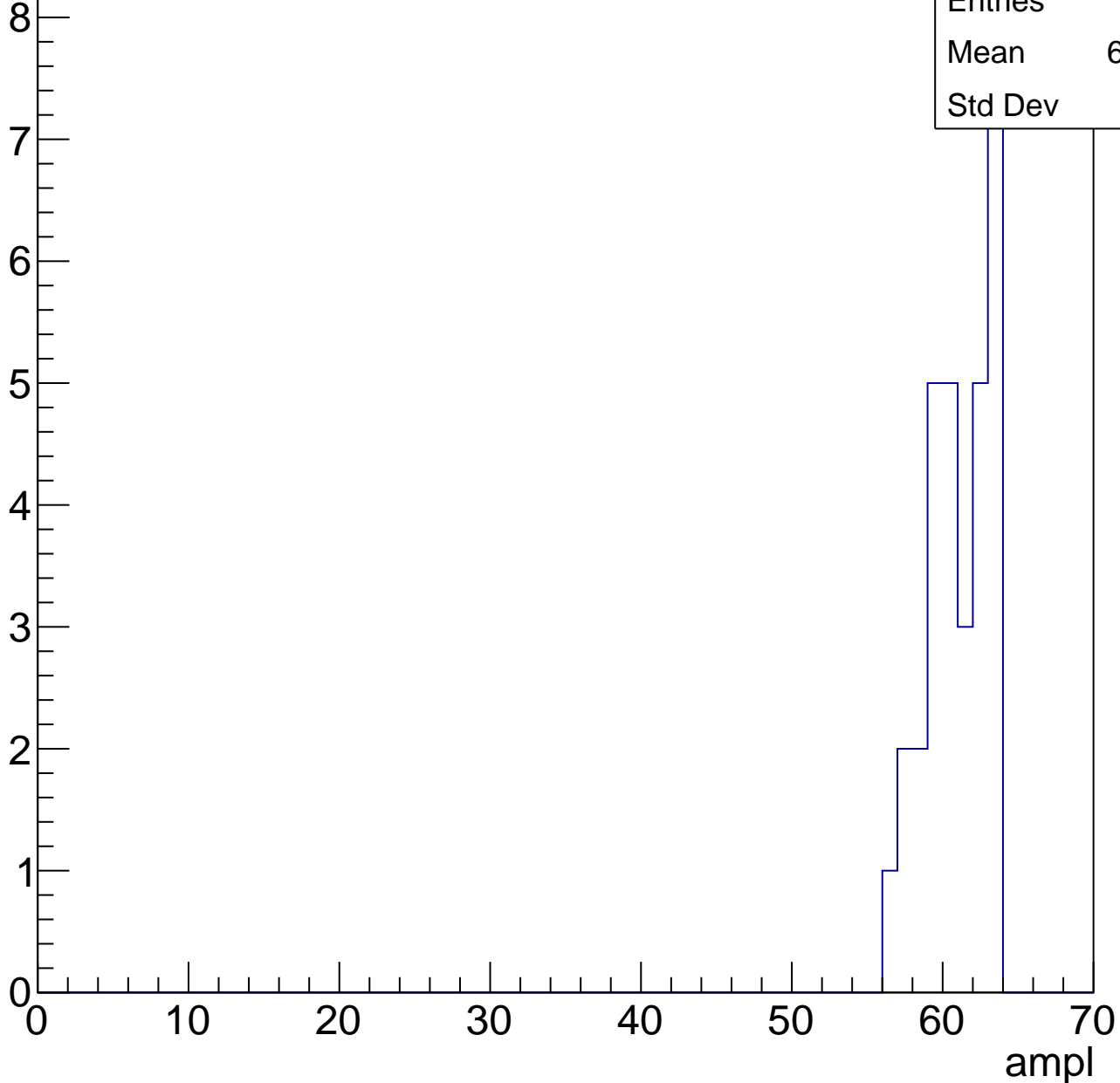


B1L103S, U12-ch28, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

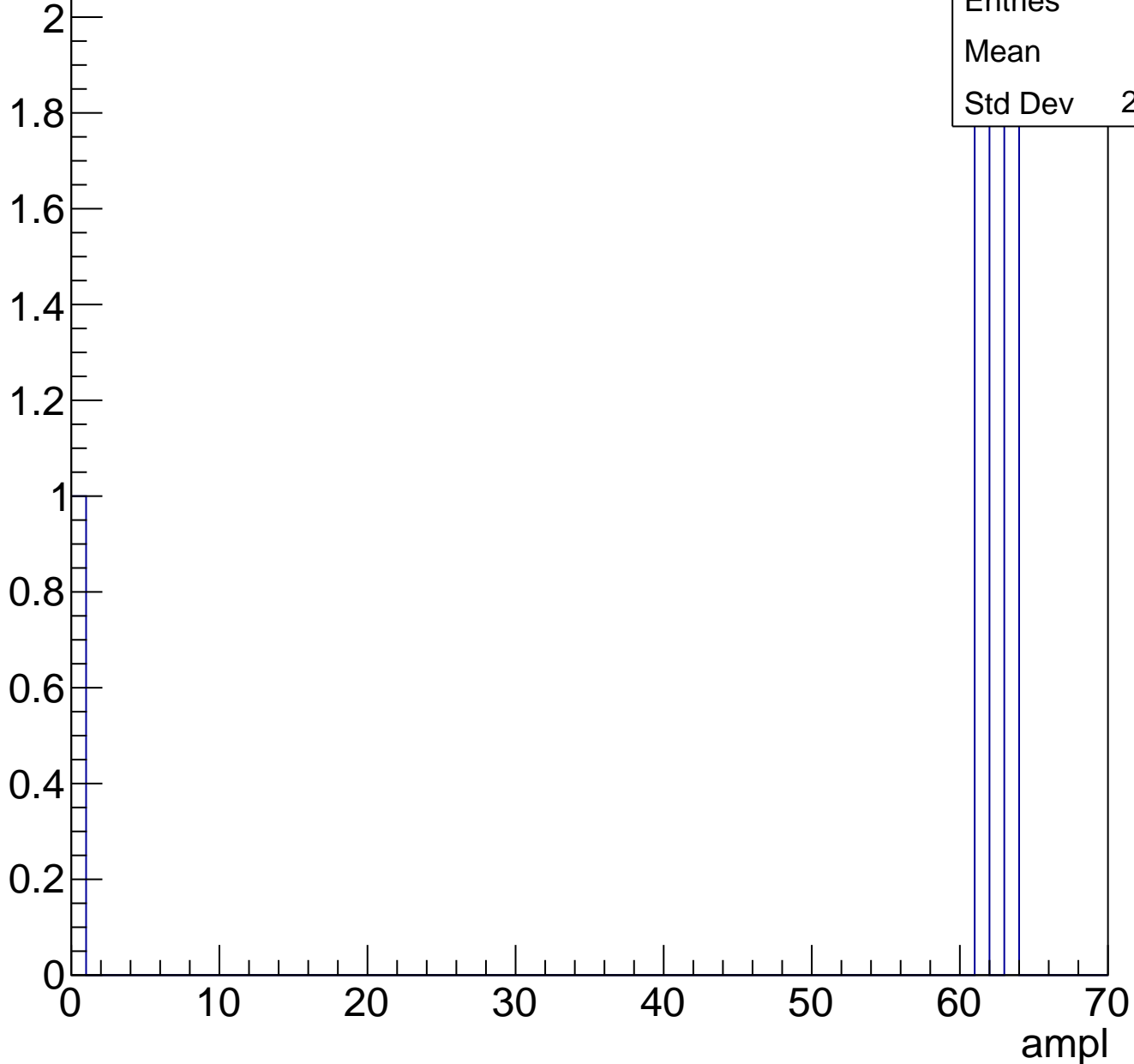
Entries	31
Mean	60.58
Std Dev	2.06



B1L103S, U12-ch28, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch28, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

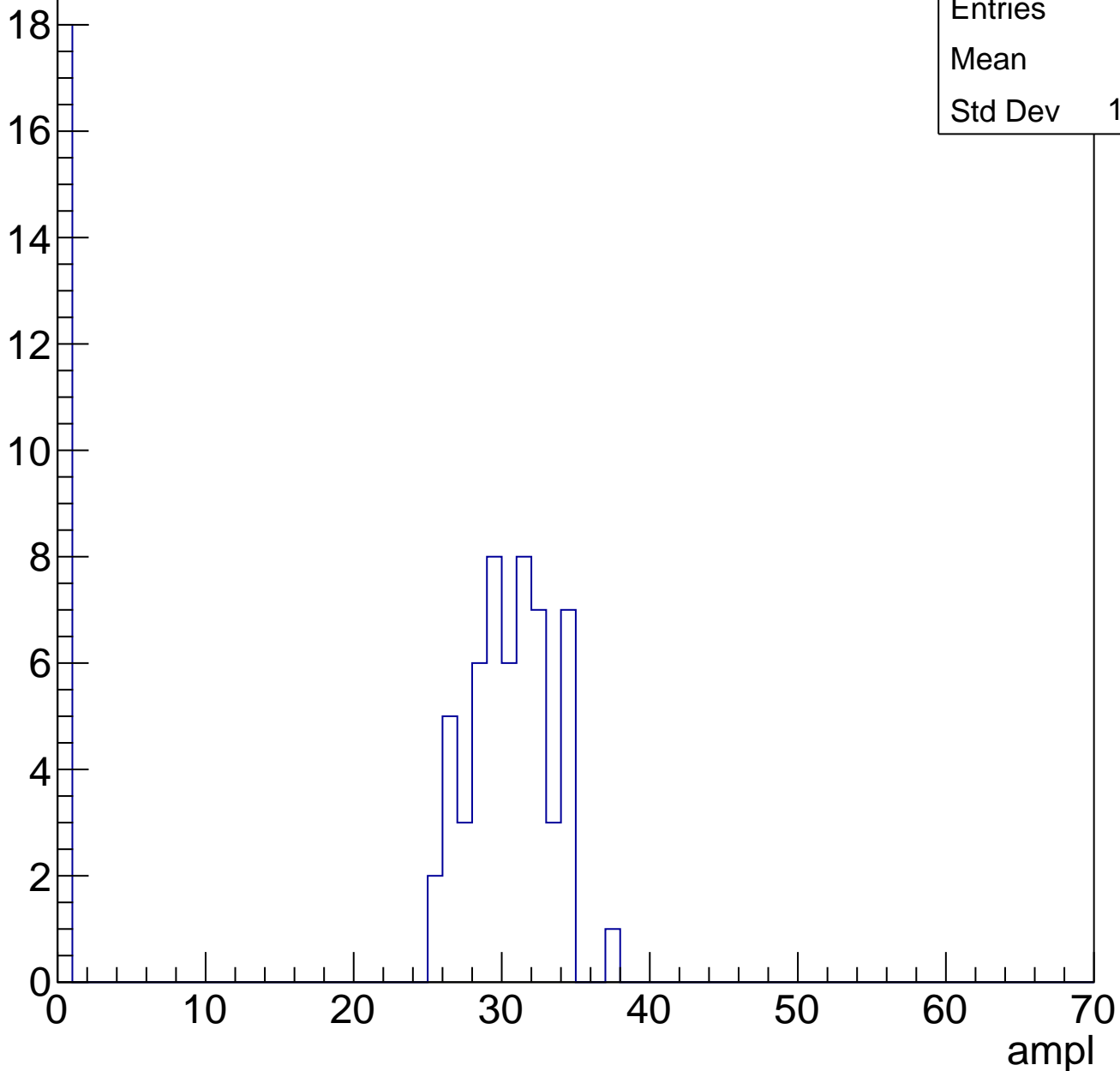


B1L103S, U12-ch29, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	74
Mean	22.8
Std Dev	13.14

Entry



B1L103S, U12-ch29, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	83
Mean	31.73
Std Dev	12.87

Entry

10

8

6

4

2

0

0

10

20

30

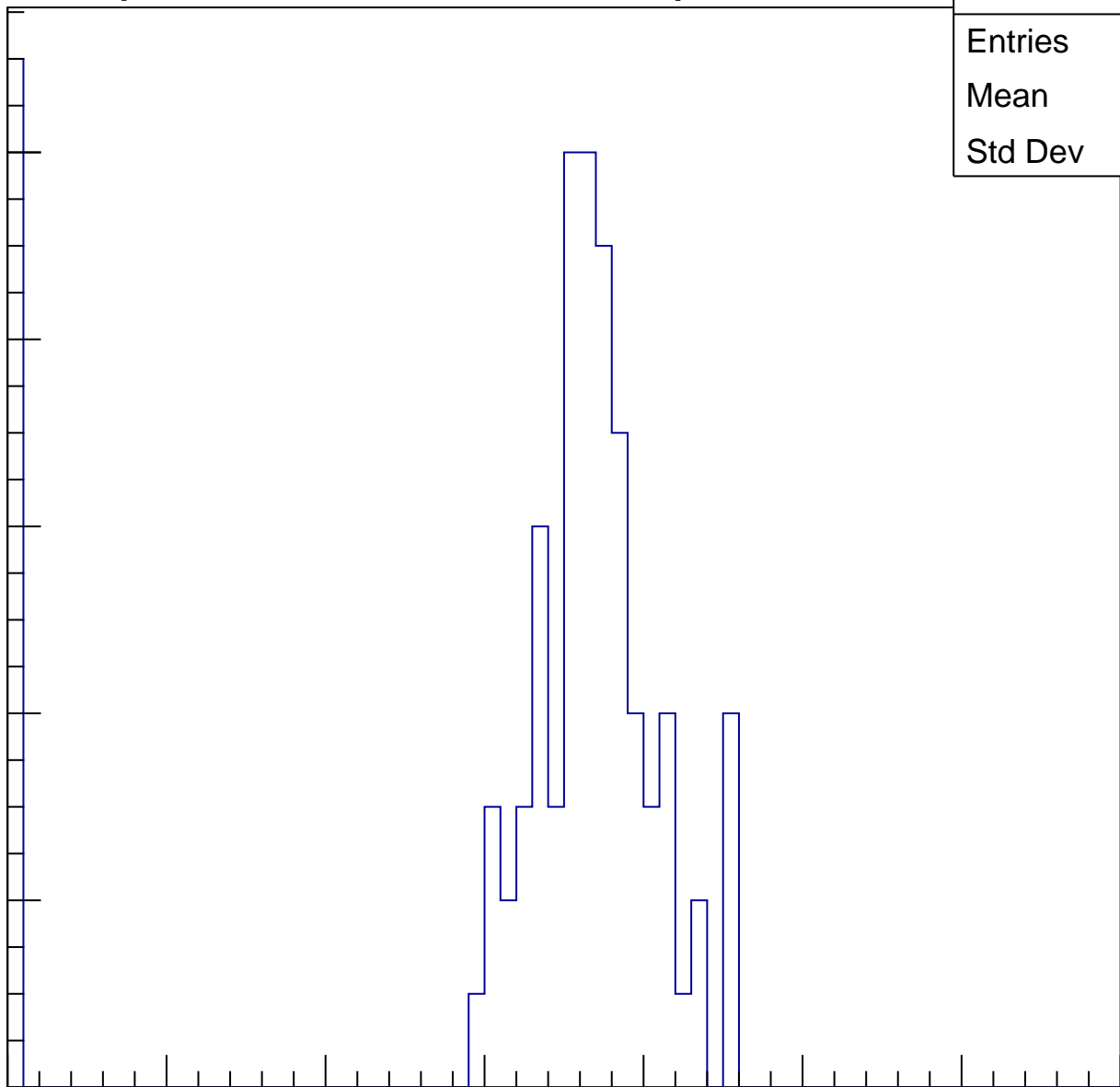
40

50

60

70

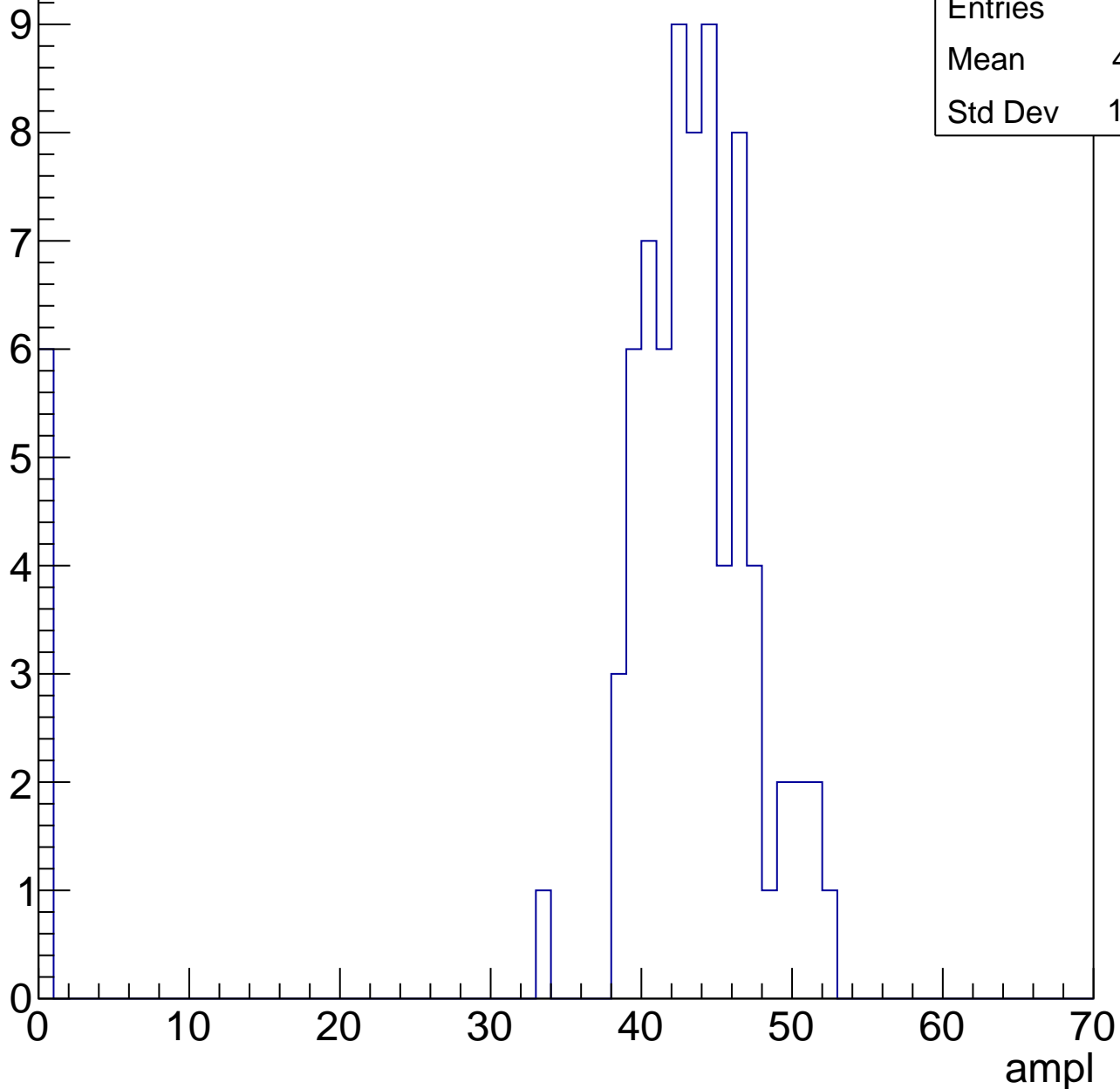
ampl



B1L103S, U12-ch29, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

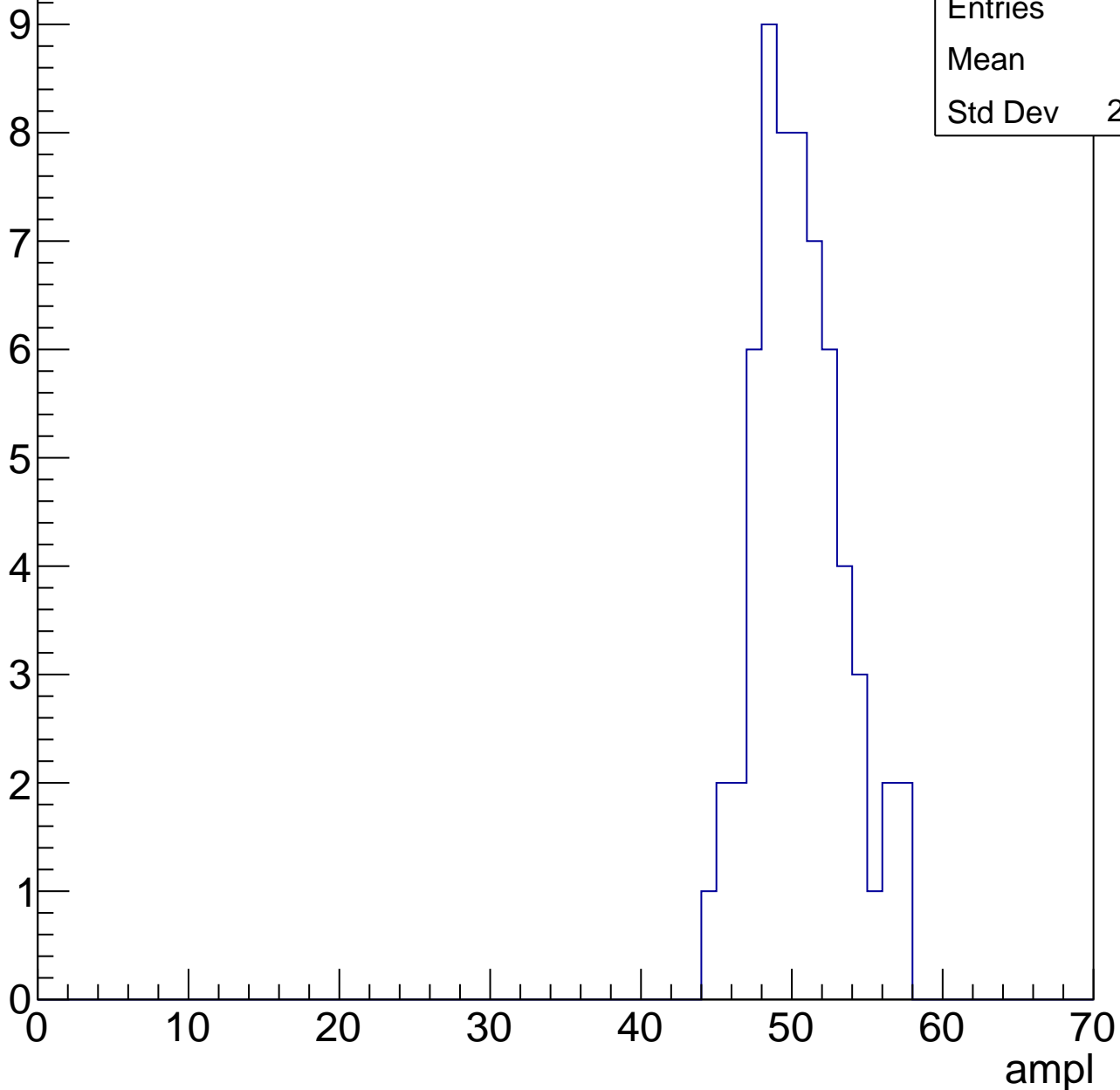


B1L103S, U12-ch29, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	50.1
Std Dev	2.935

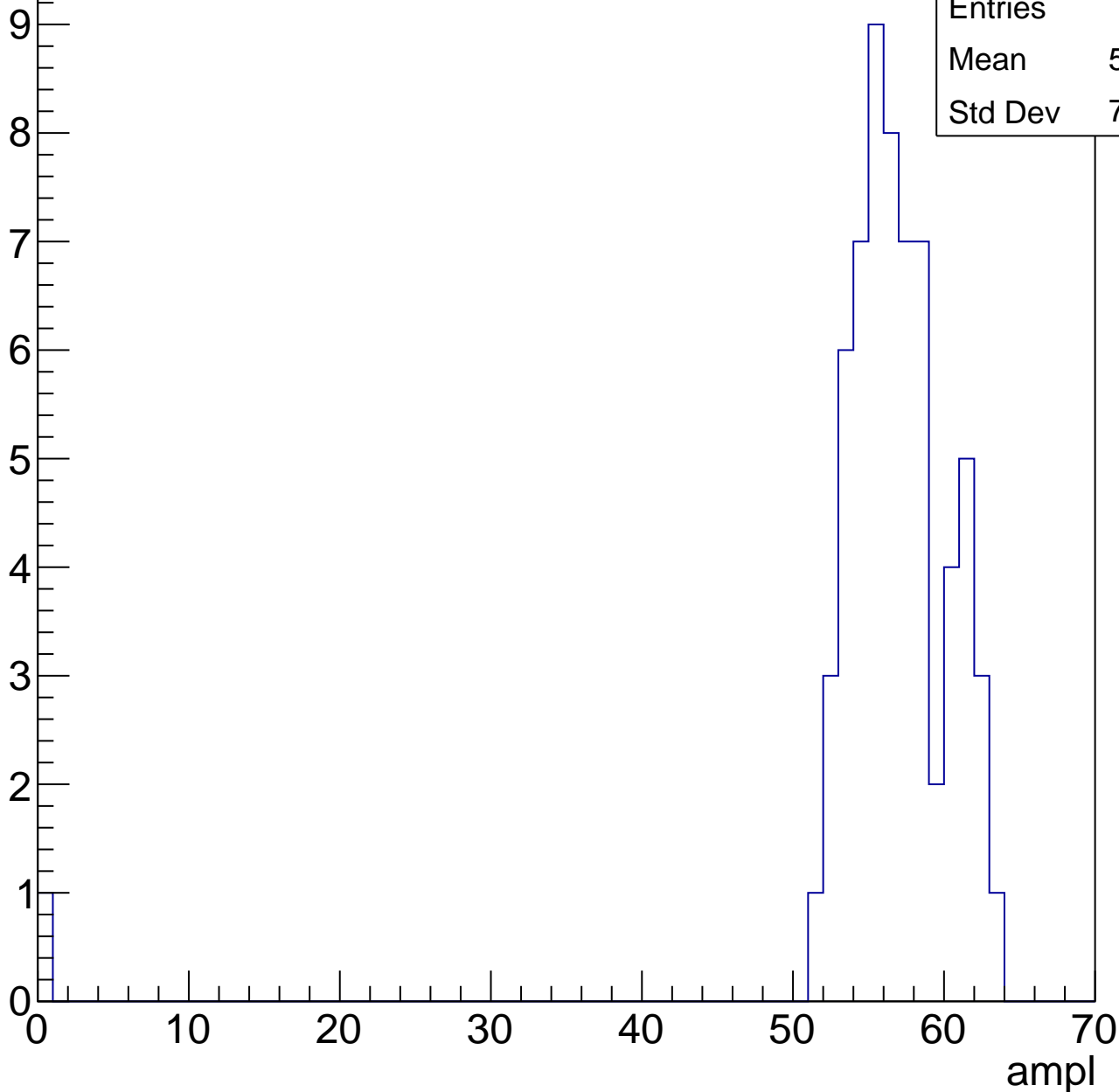


B1L103S, U12-ch29, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

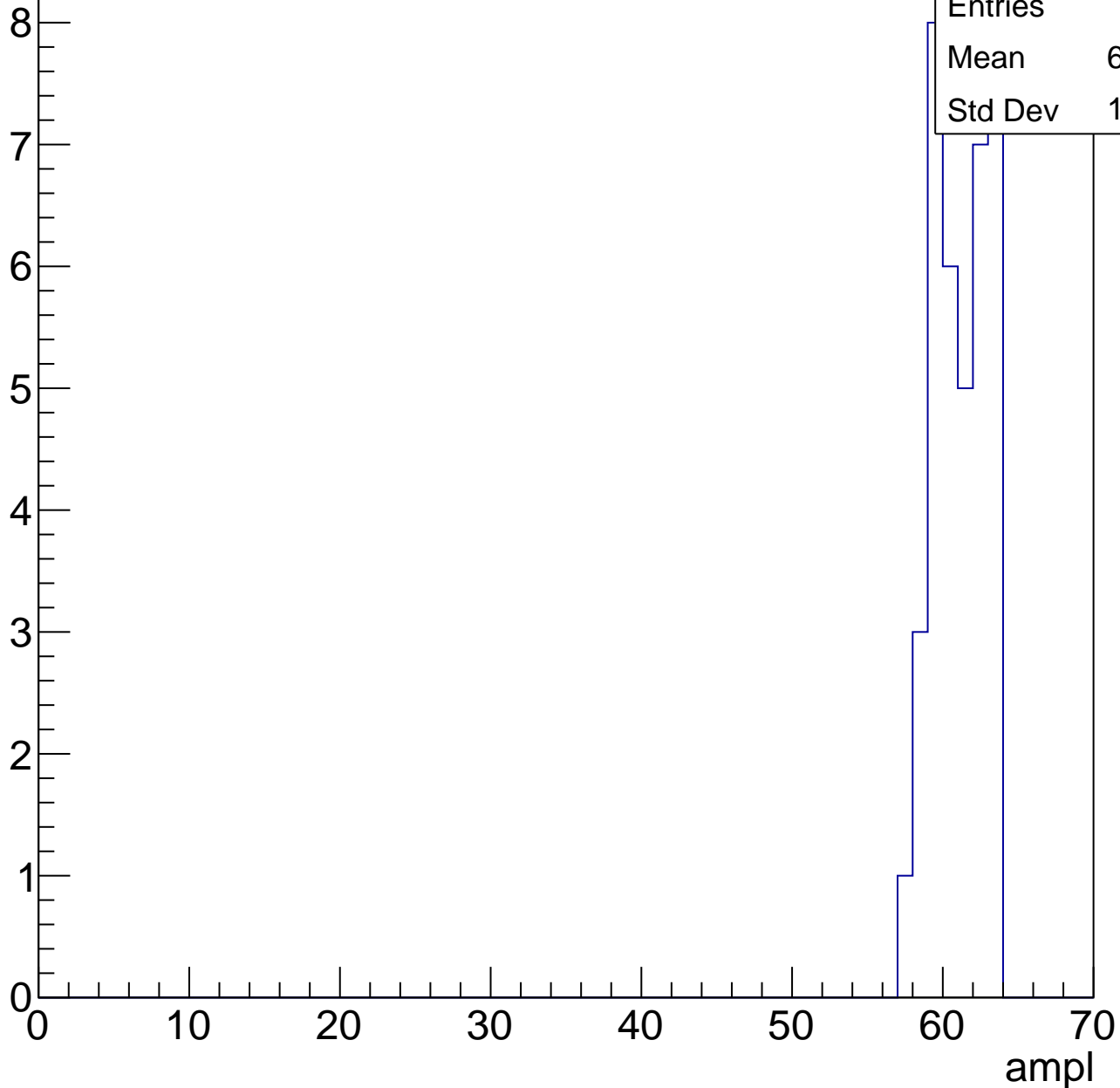
Entries	64
Mean	55.67
Std Dev	7.595



B1L103S, U12-ch29, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch29, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch29, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.158
Std Dev	4.913

Entry

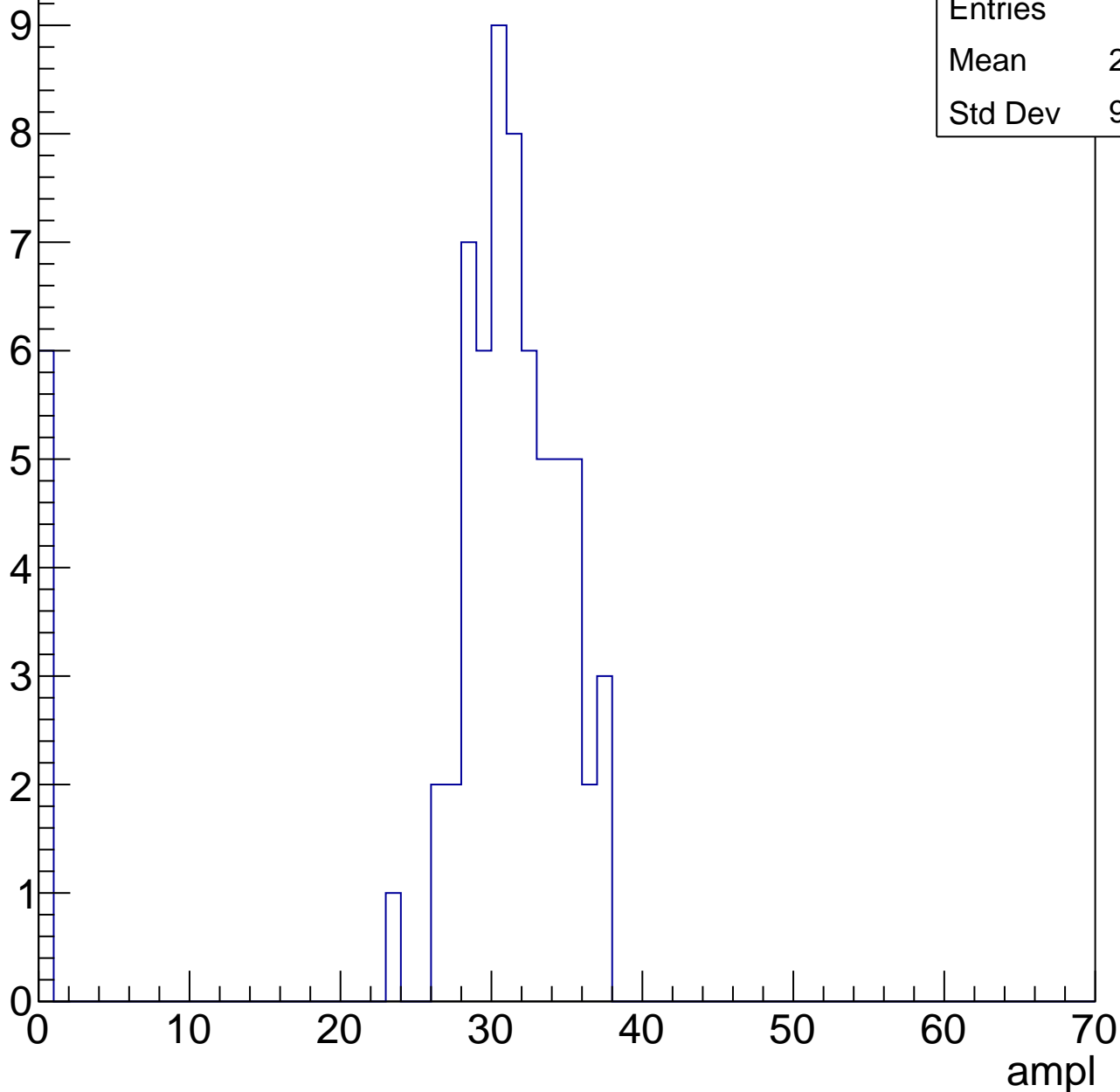


B1L103S, U12-ch30, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	28.39
Std Dev	9.352

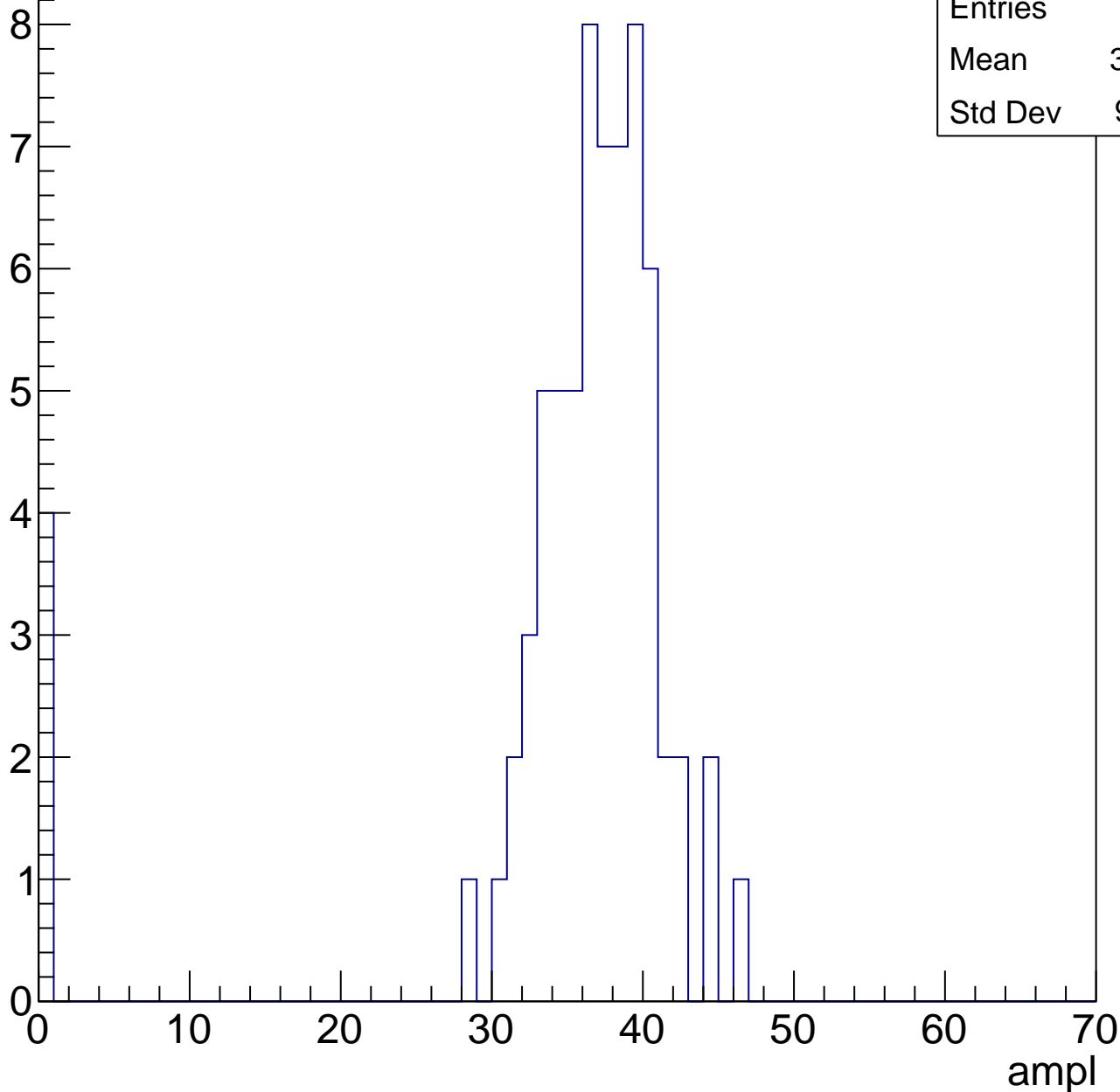


B1L103S, U12-ch30, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	34.65
Std Dev	9.231

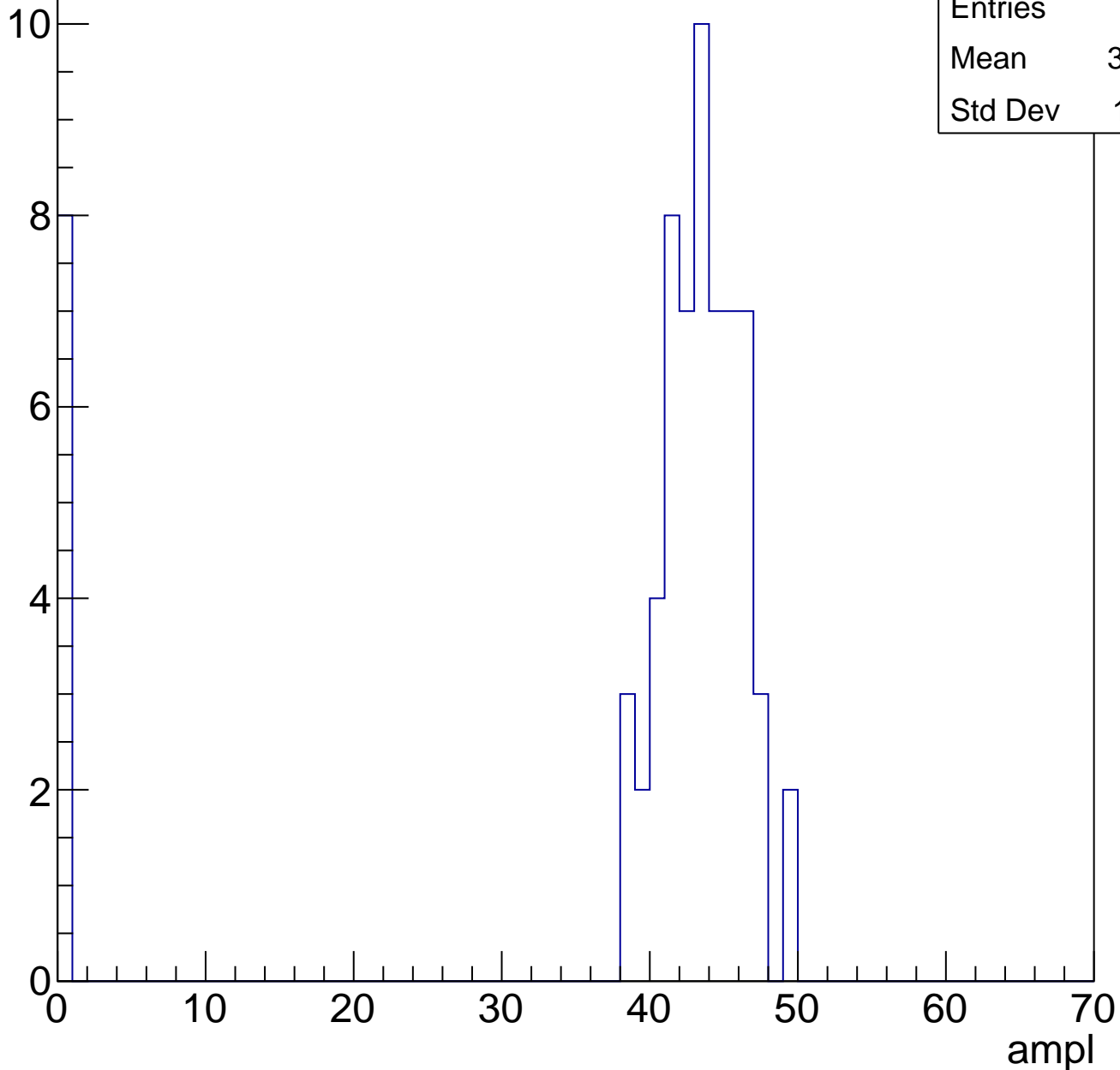


B1L103S, U12-ch30, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	68
Mean	38.06
Std Dev	14.11

Entry

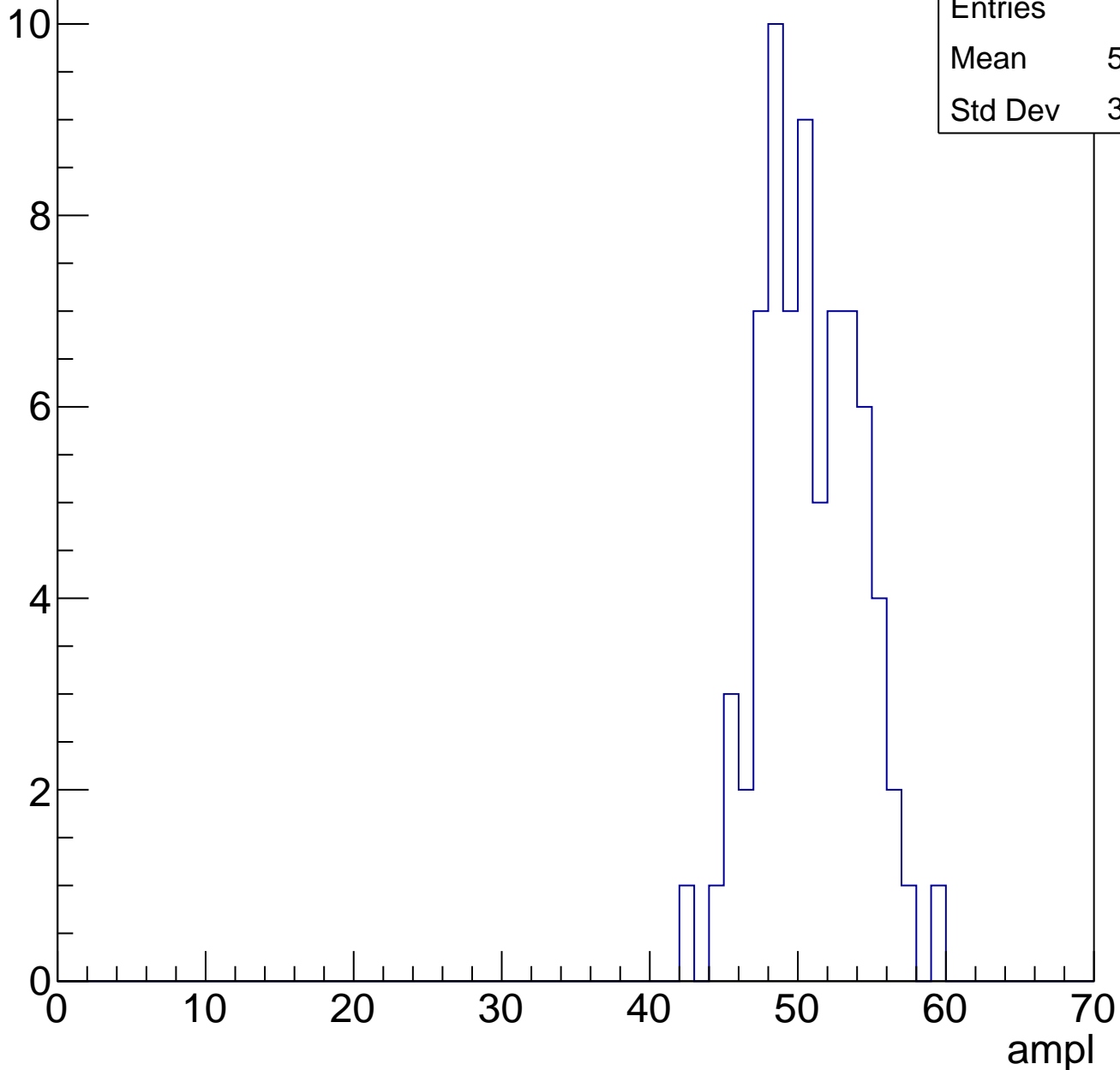


B1L103S, U12-ch30, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	73
Mean	50.37
Std Dev	3.313

Entry

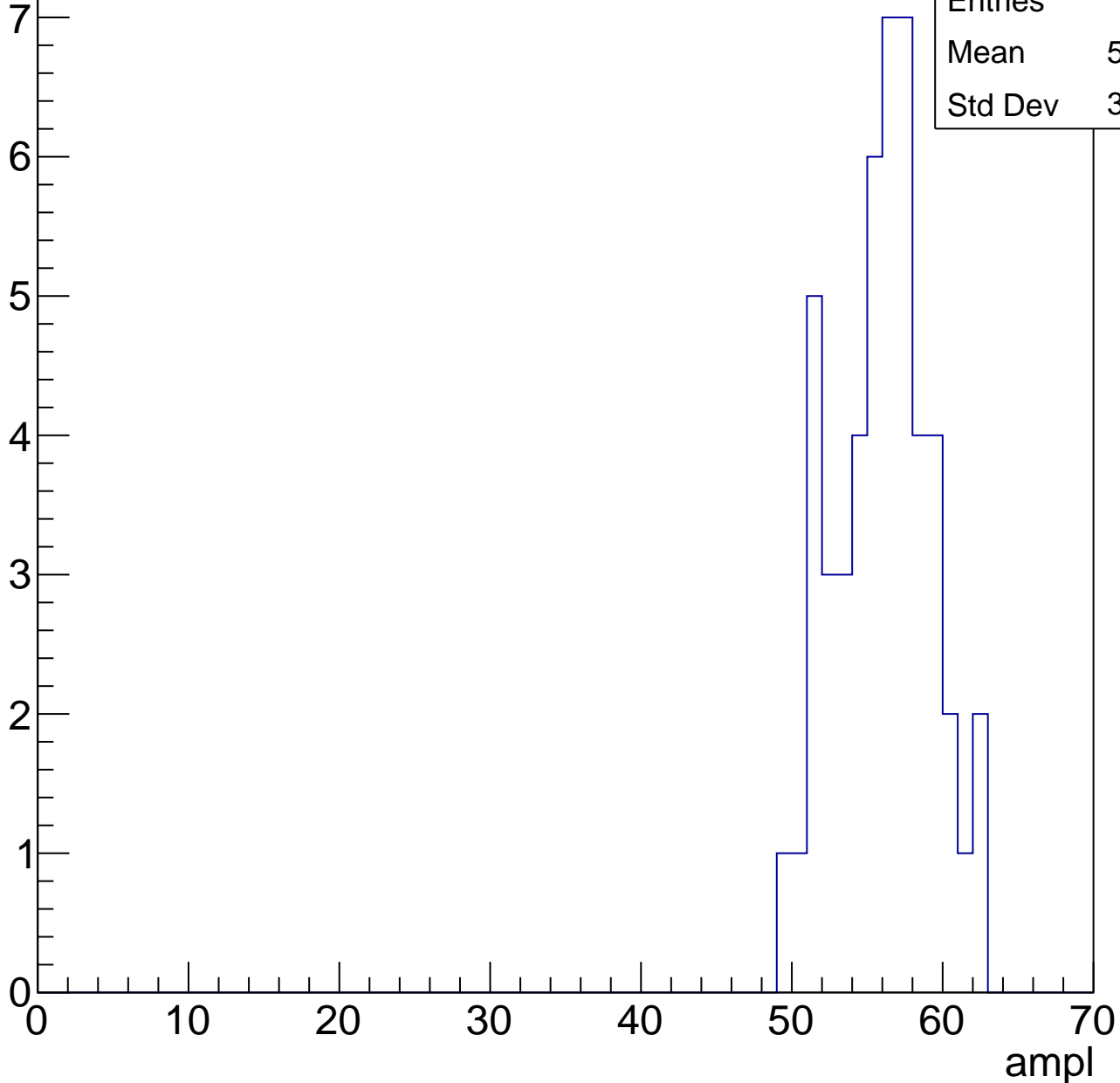


B1L103S, U12-ch30, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

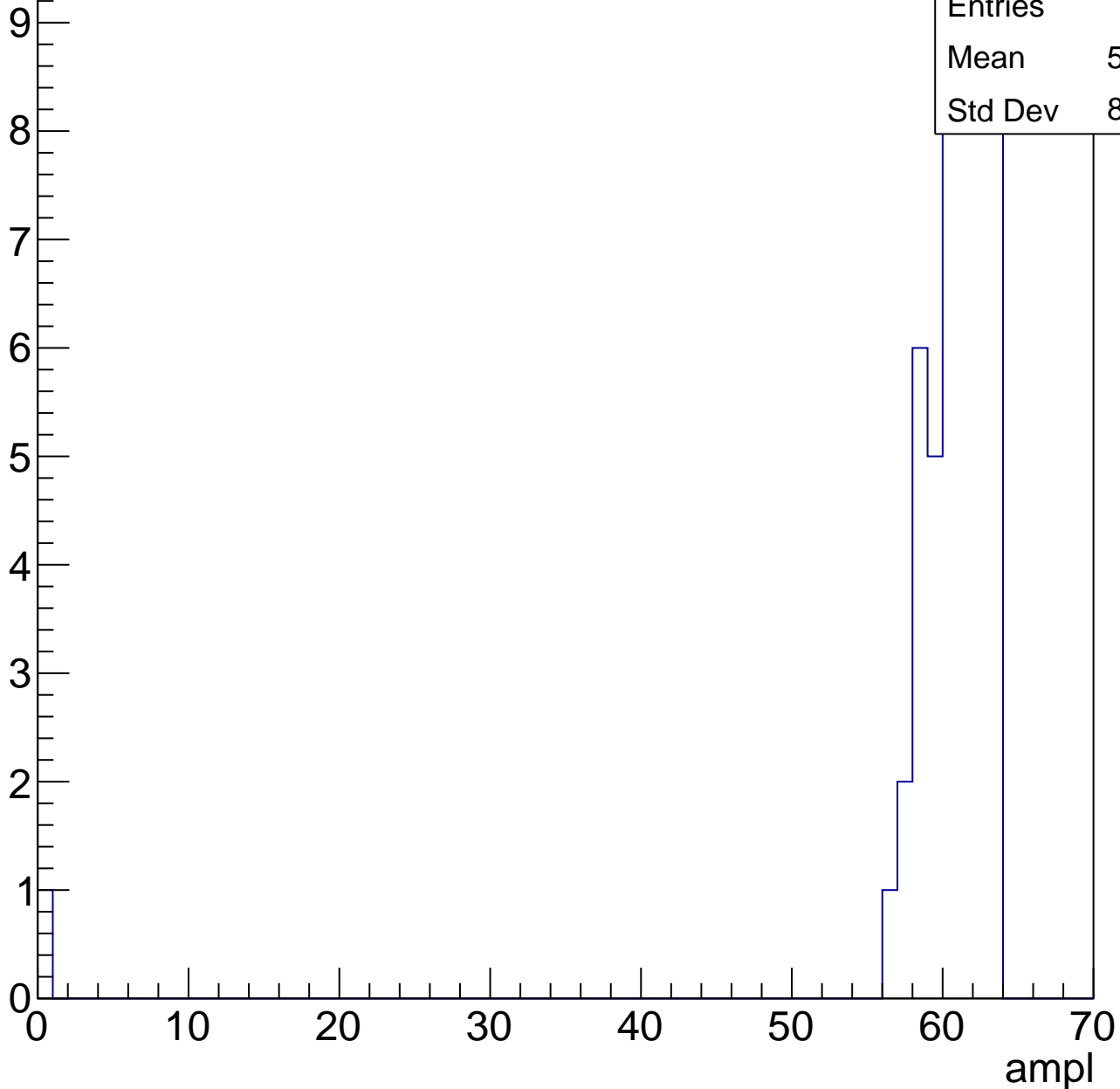
Entries	50
Mean	55.58
Std Dev	3.118



B1L103S, U12-ch30, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch30, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch30, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.158
Std Dev	4.913

Entry

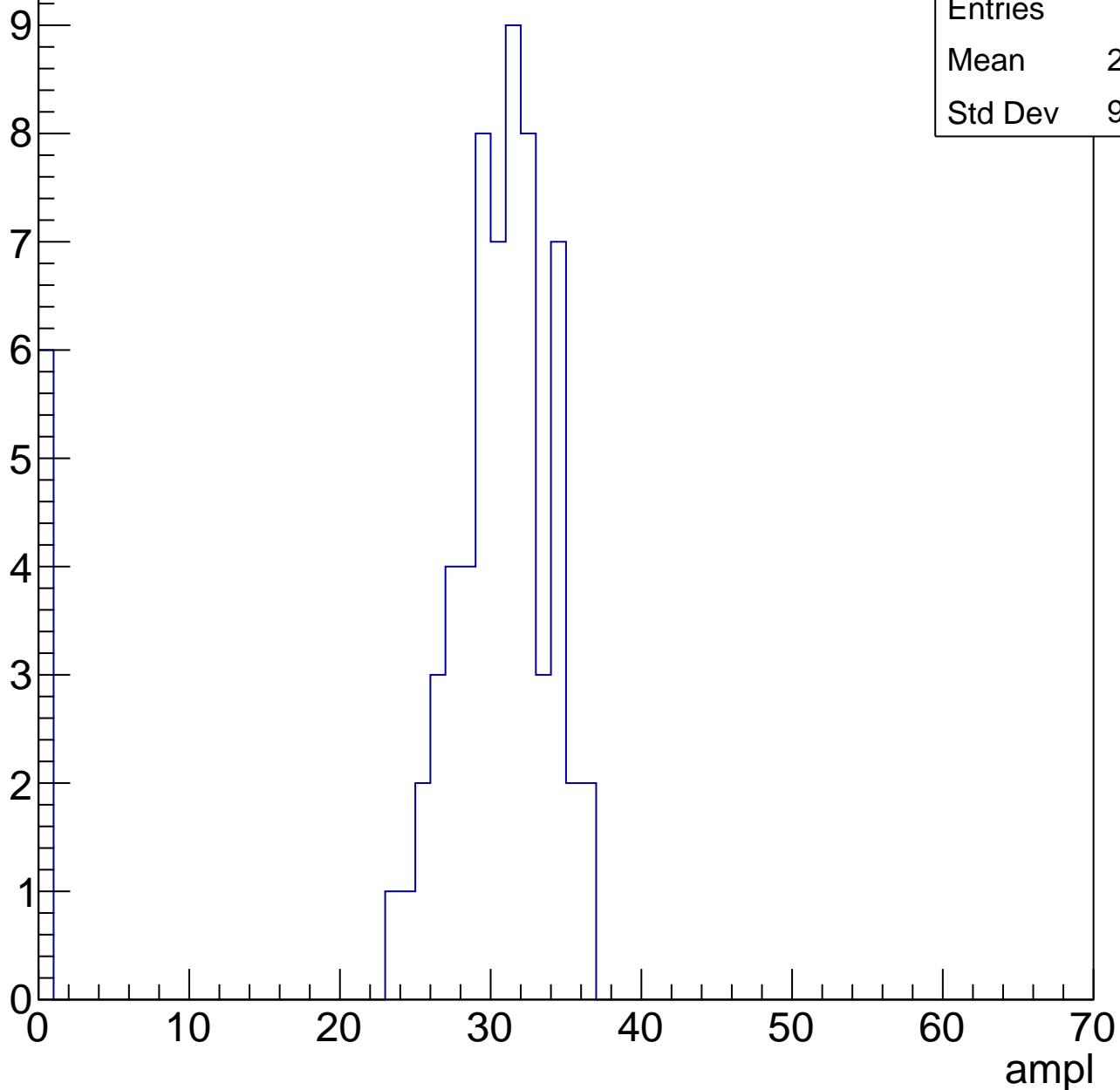


B1L103S, U12-ch31, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	27.63
Std Dev	9.116

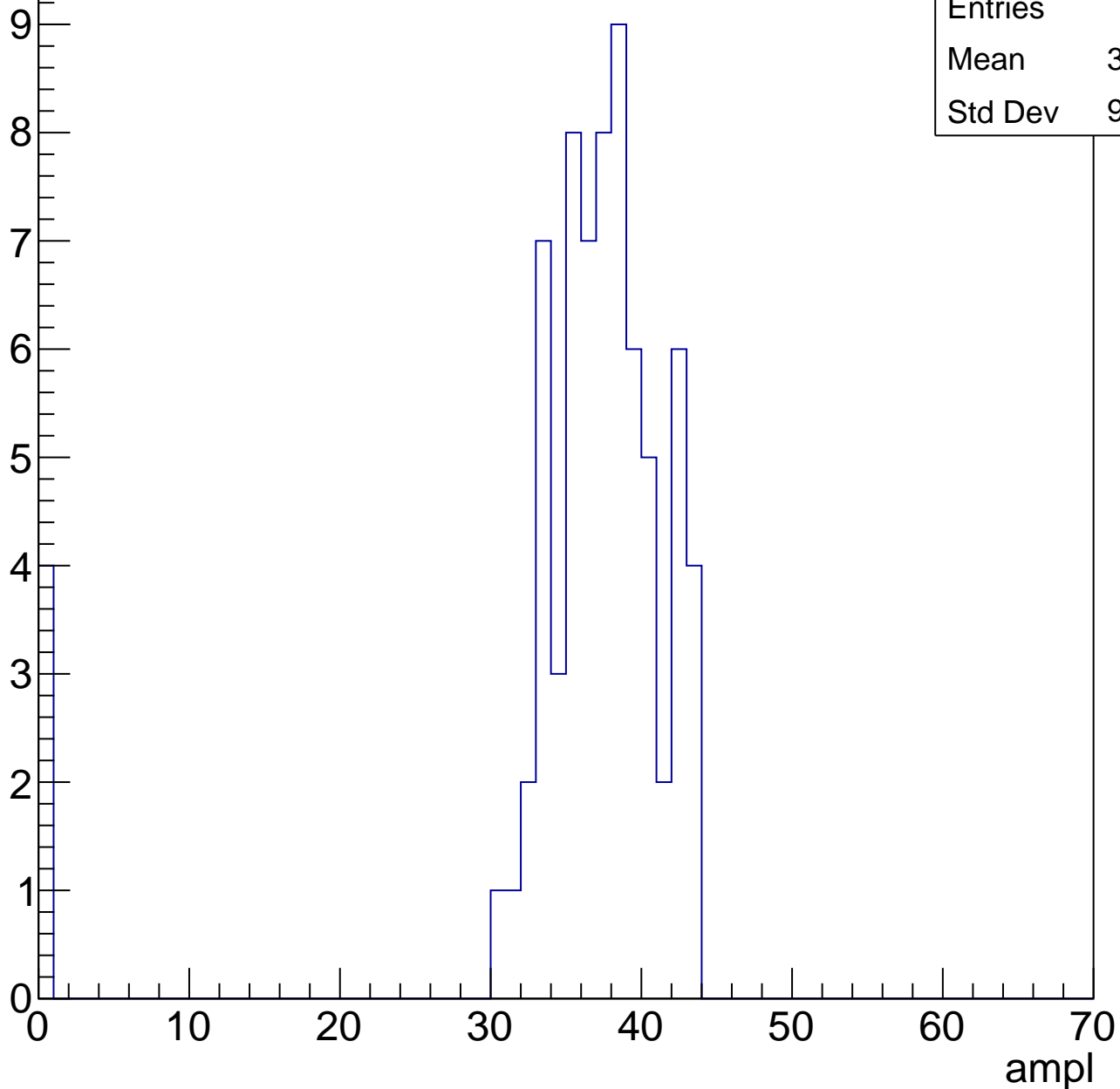


B1L103S, U12-ch31, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	73
Mean	35.18
Std Dev	9.029

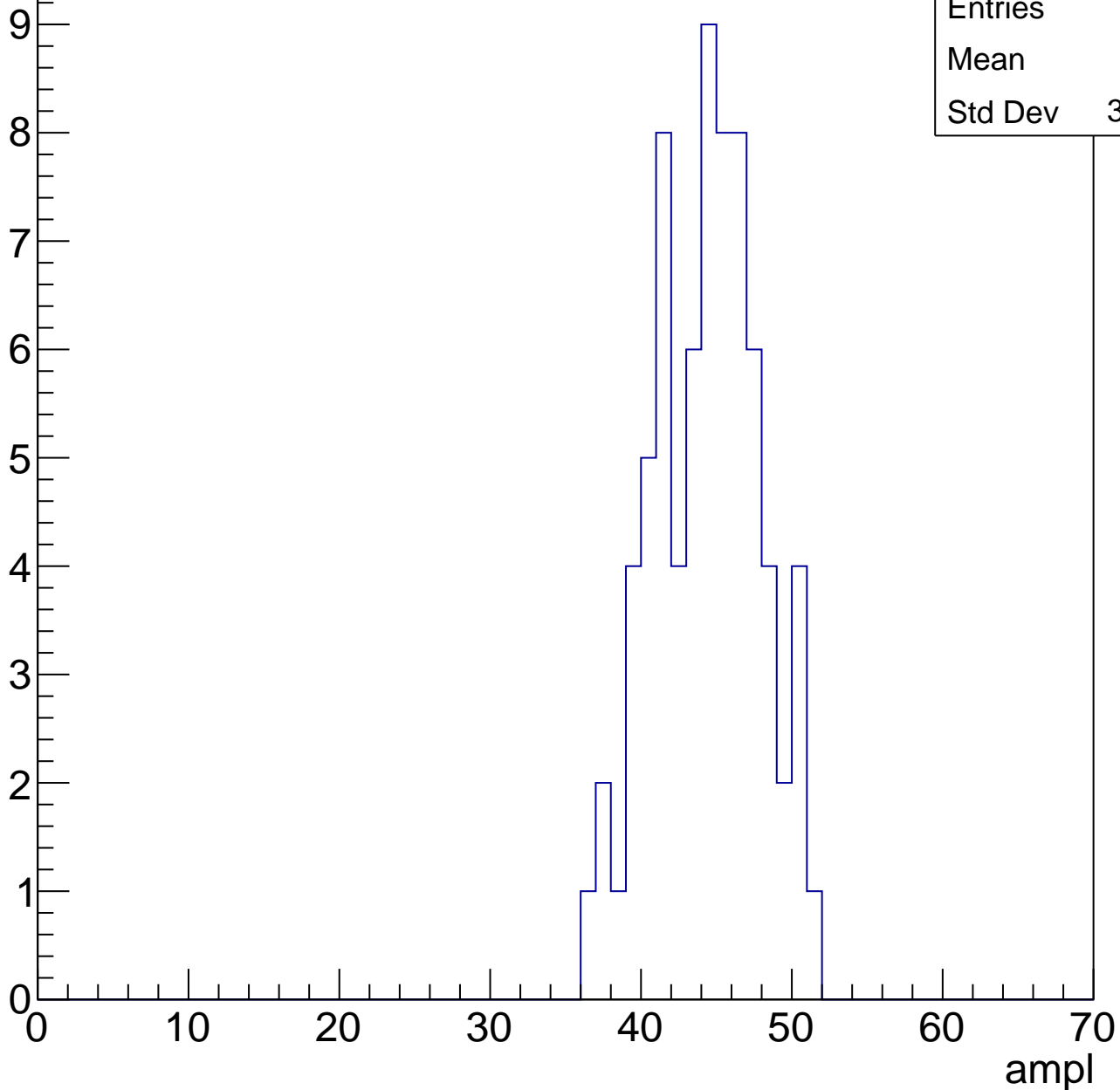


B1L103S, U12-ch31, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	73
Mean	43.9
Std Dev	3.457



B1L103S, U12-ch31, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	71
Mean	50.28
Std Dev	6.722

Entry

10

8

6

4

2

0

0

10

20

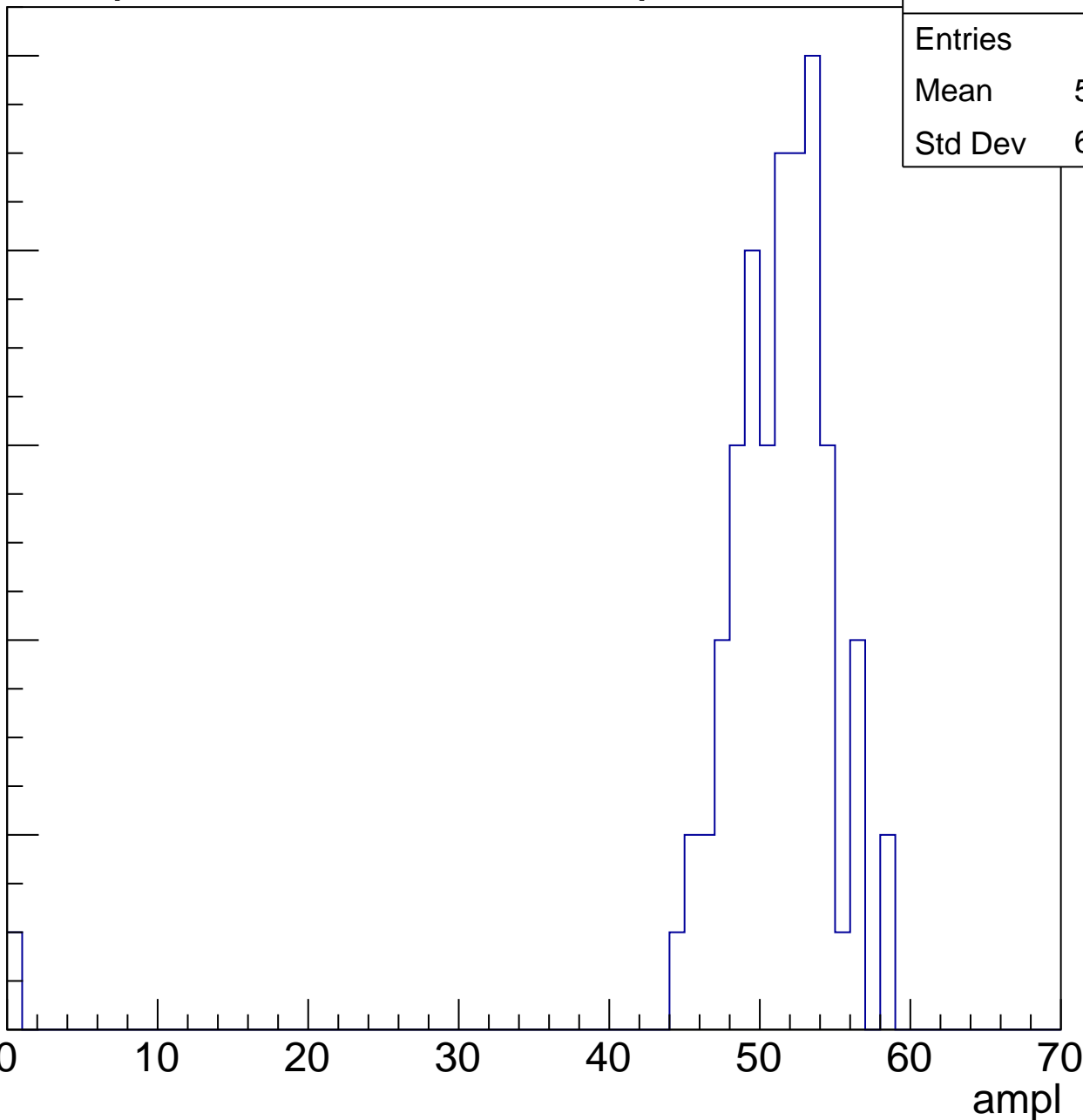
30

40

50

60

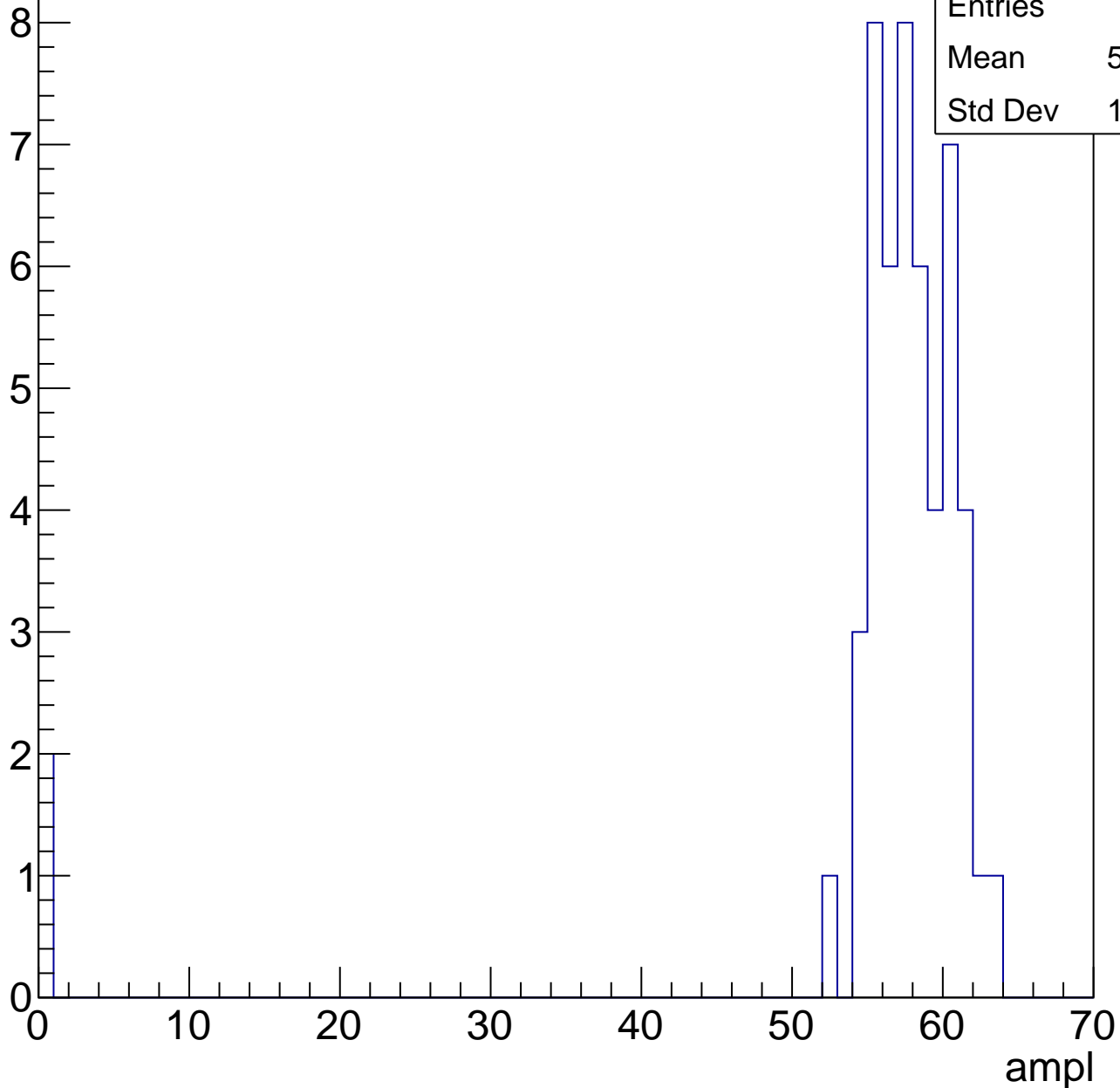
ampl



B1L103S, U12-ch31, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

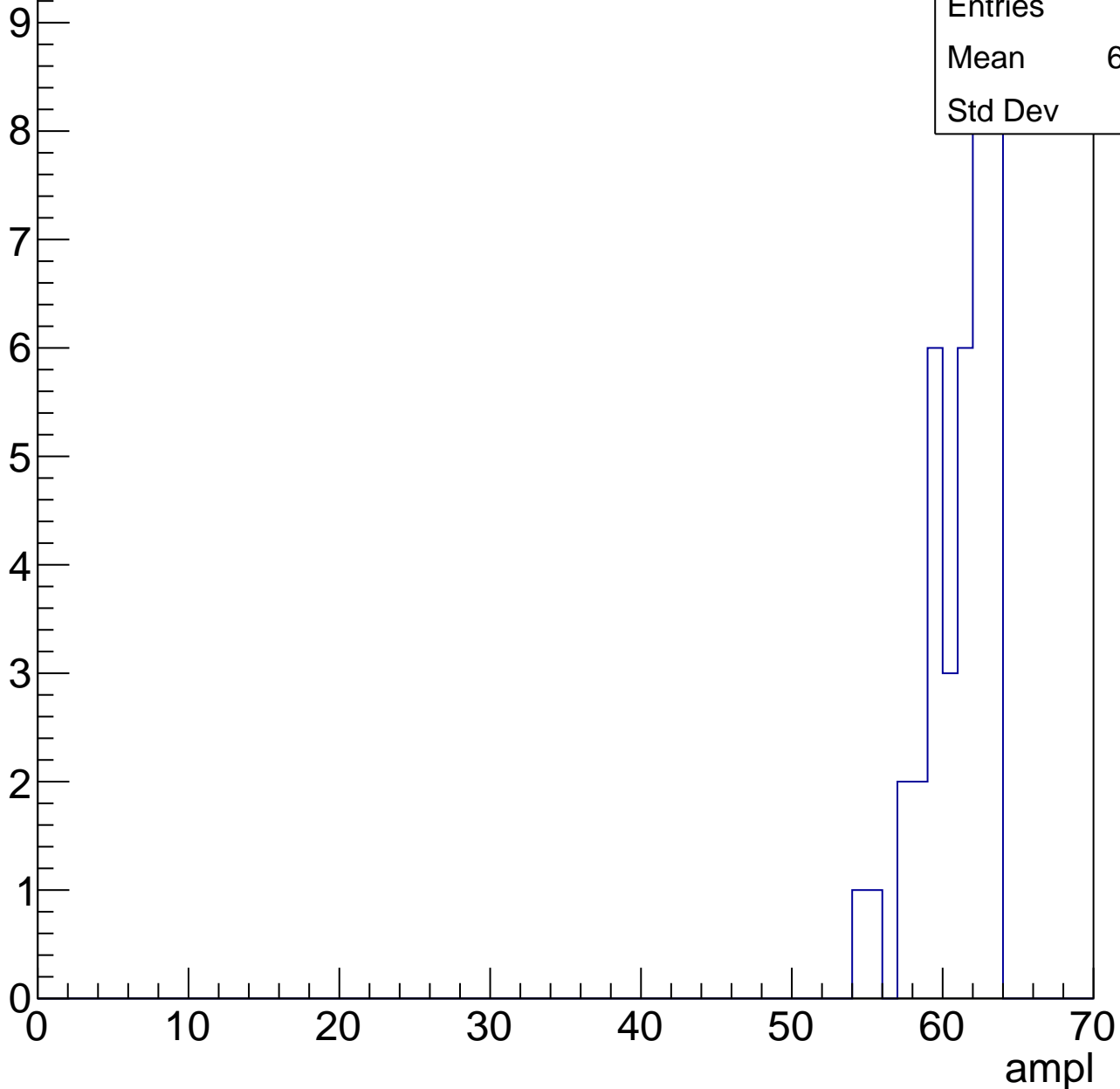


B1L103S, U12-ch31, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	38
Mean	60.58
Std Dev	2.29



B1L103S, U12-ch31, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch31, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.211
Std Dev	5.136

Entry

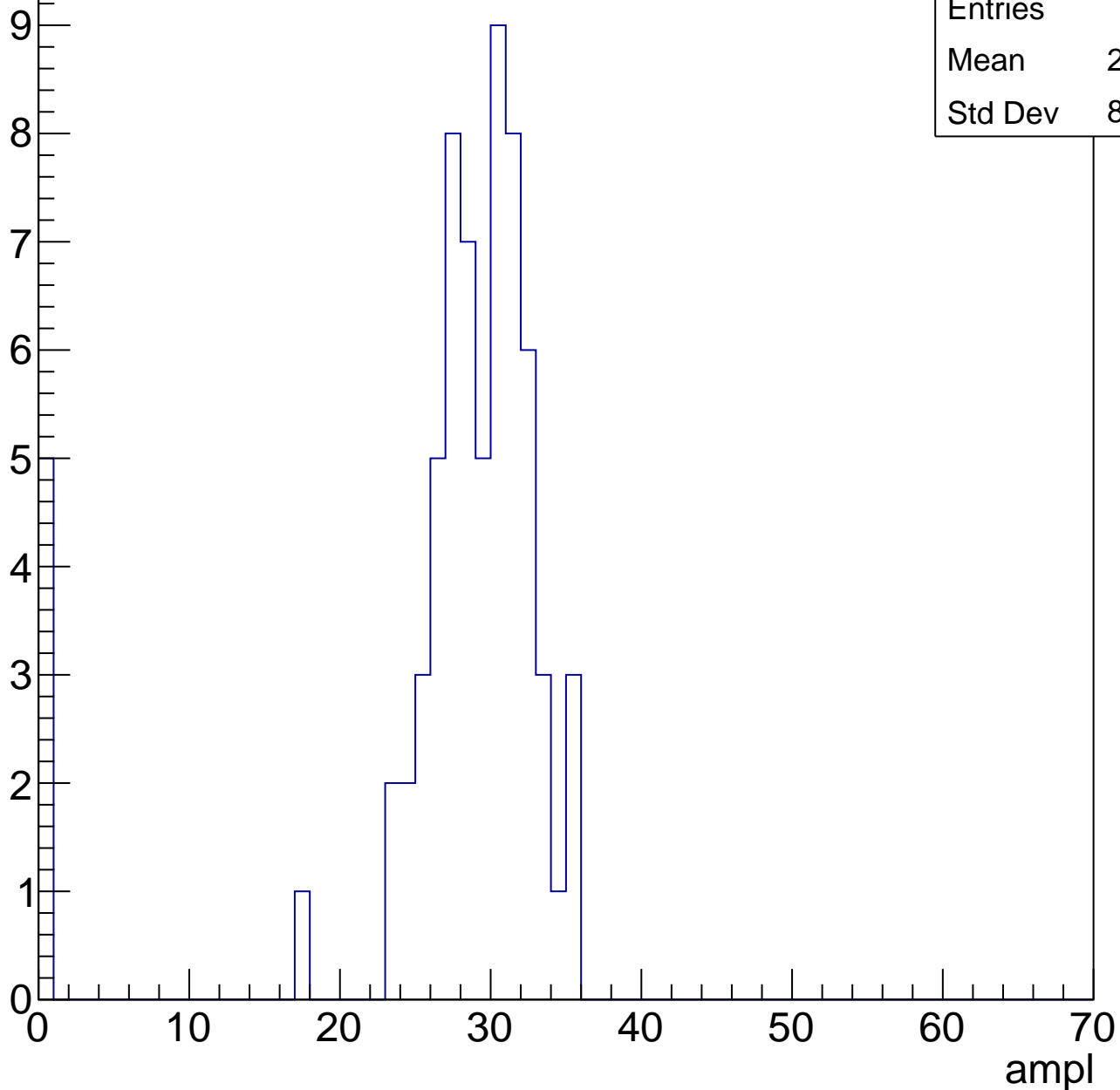


B1L103S, U12-ch32, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	26.78
Std Dev	8.174

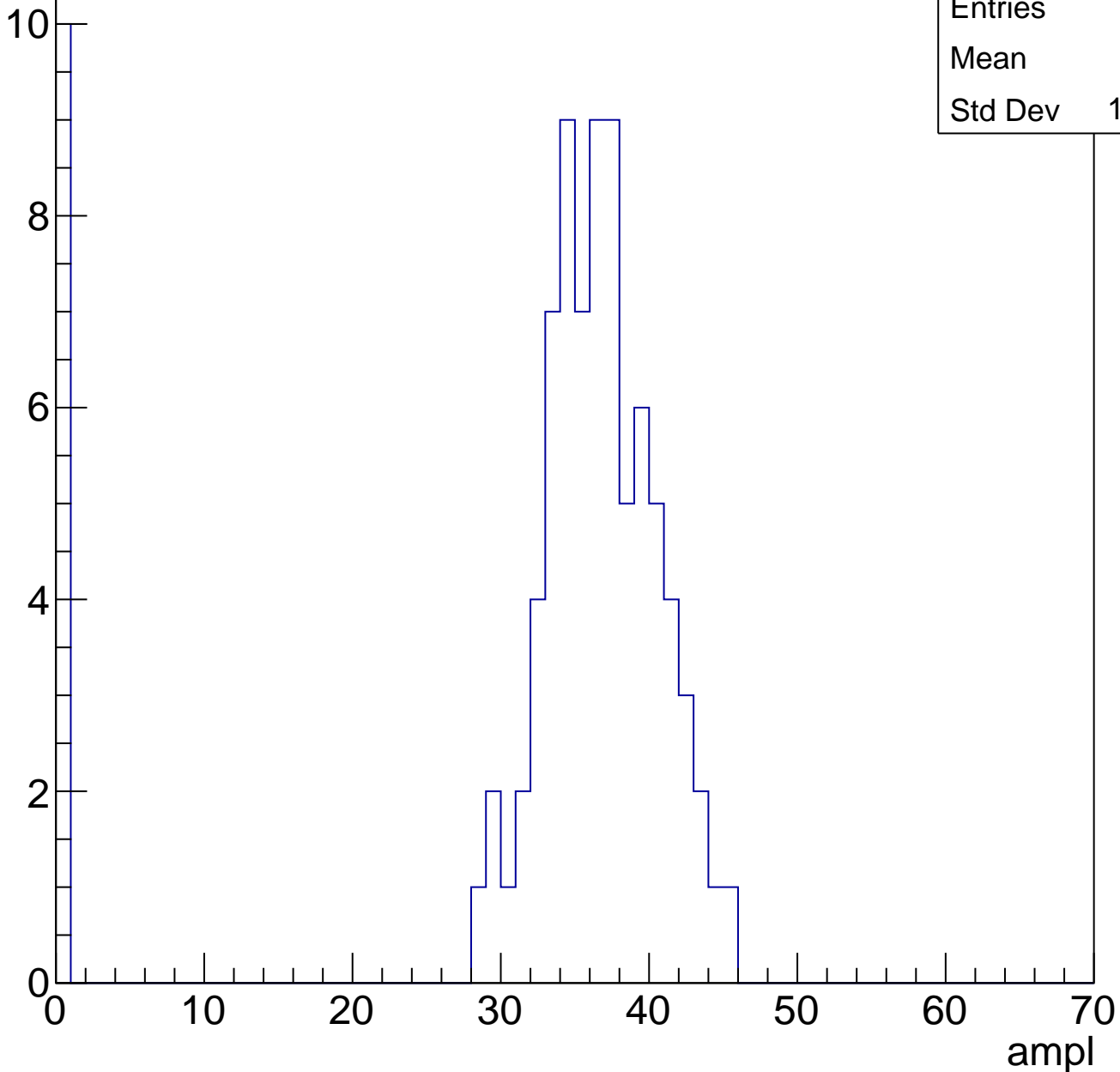


B1L103S, U12-ch32, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	88
Mean	32.2
Std Dev	12.02

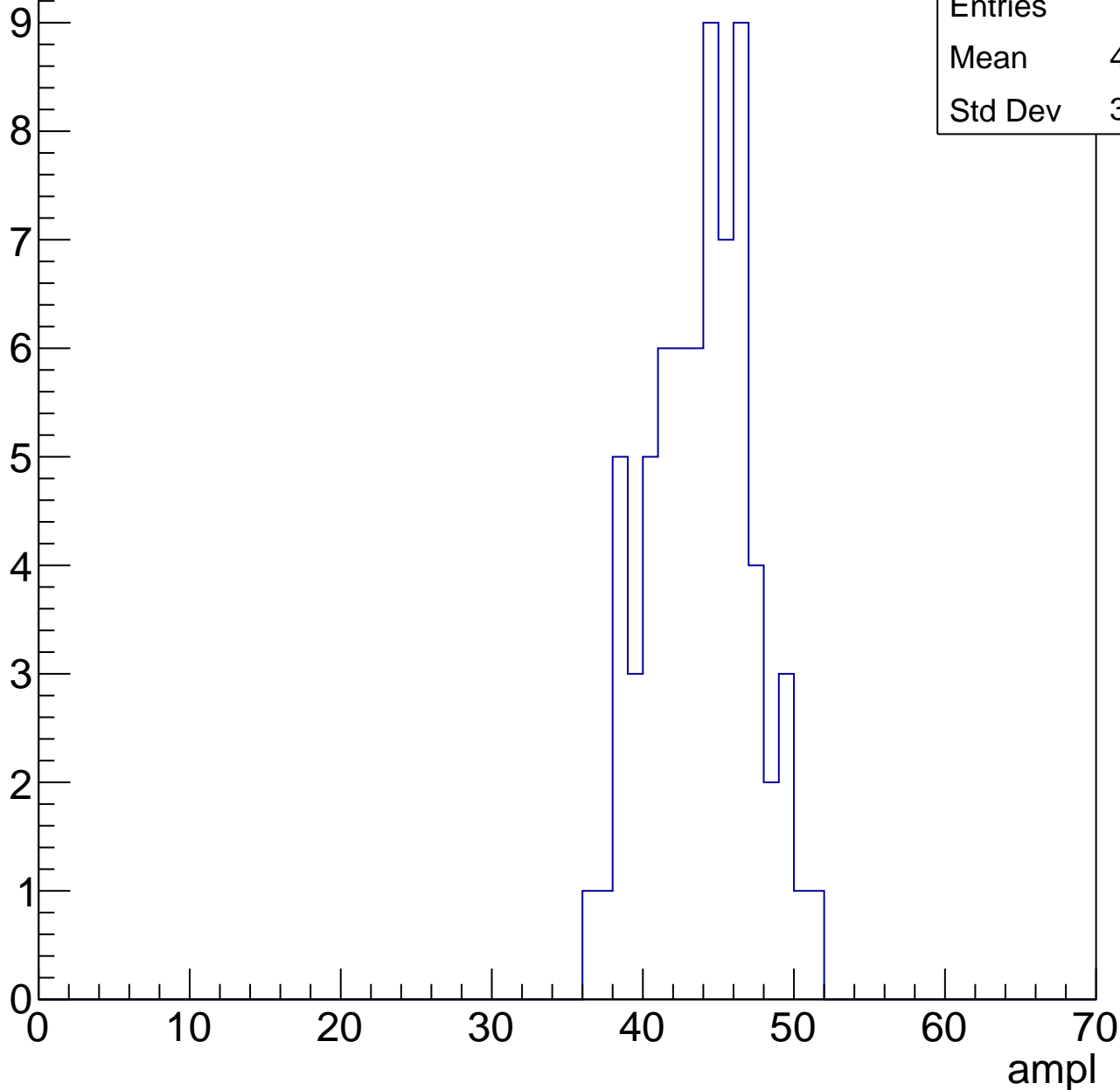
Entry



B1L103S, U12-ch32, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry



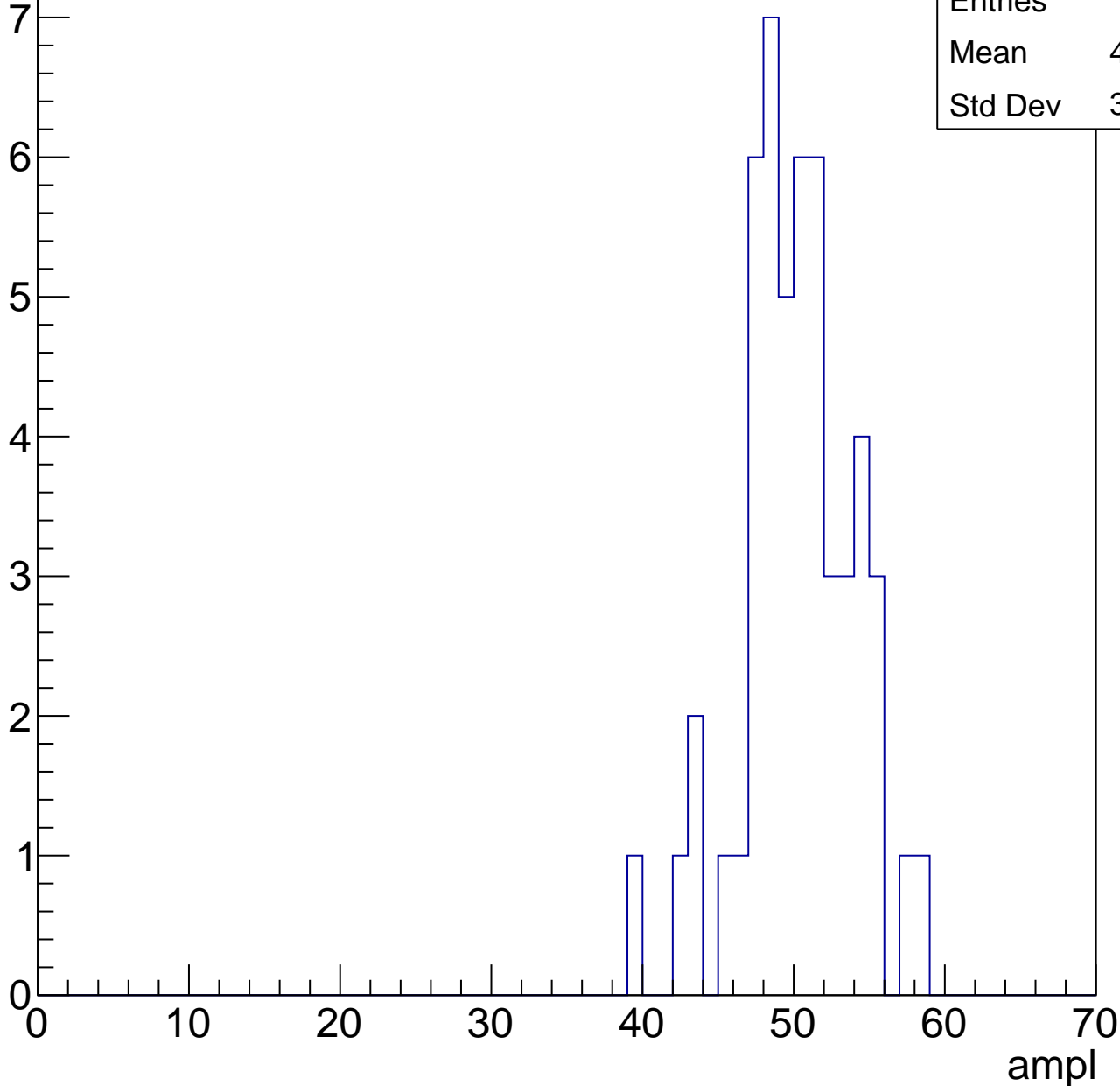
Entries	69
Mean	43.38
Std Dev	3.354

B1L103S, U12-ch32, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	51
Mean	49.76
Std Dev	3.718

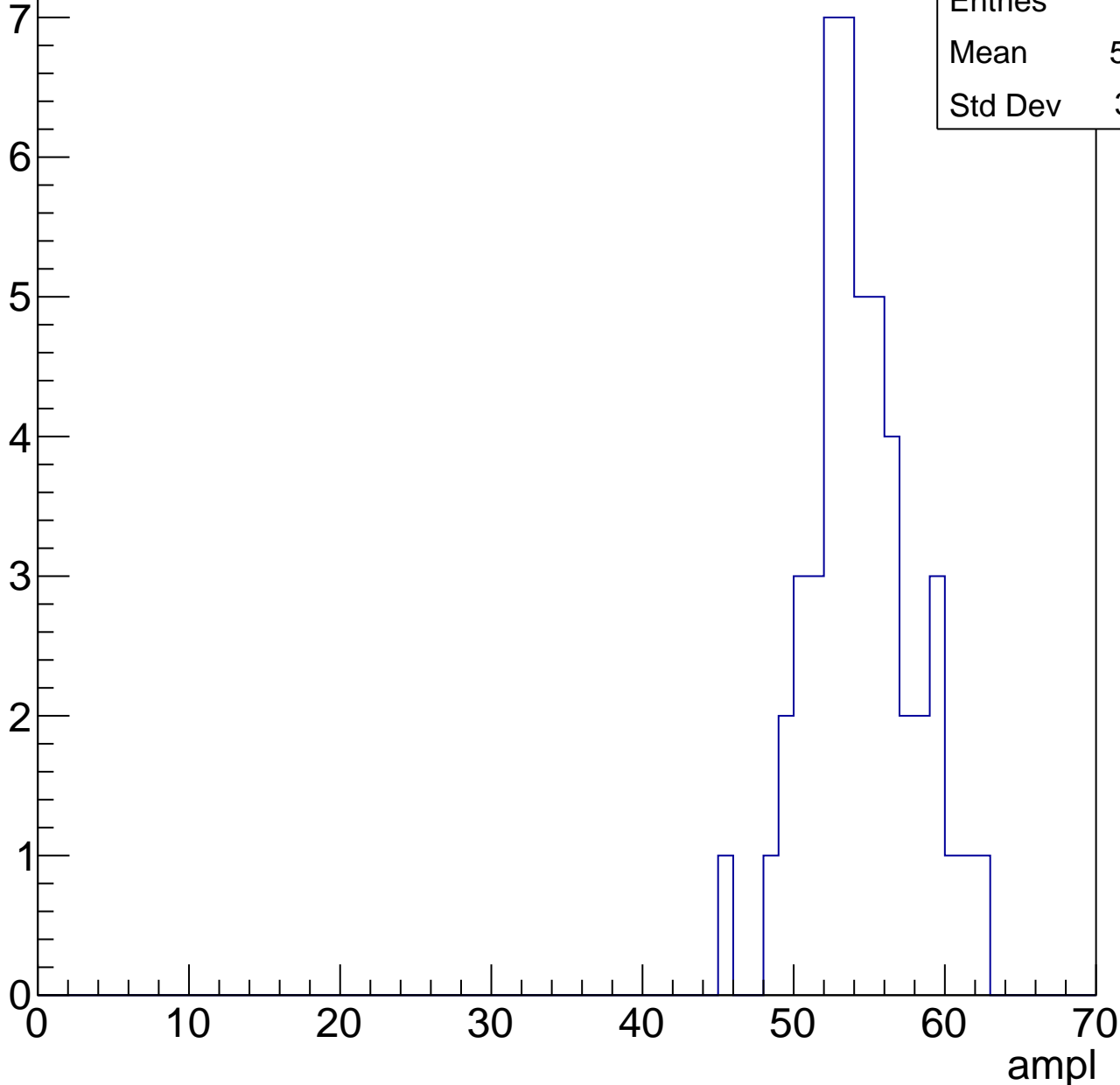


B1L103S, U12-ch32, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

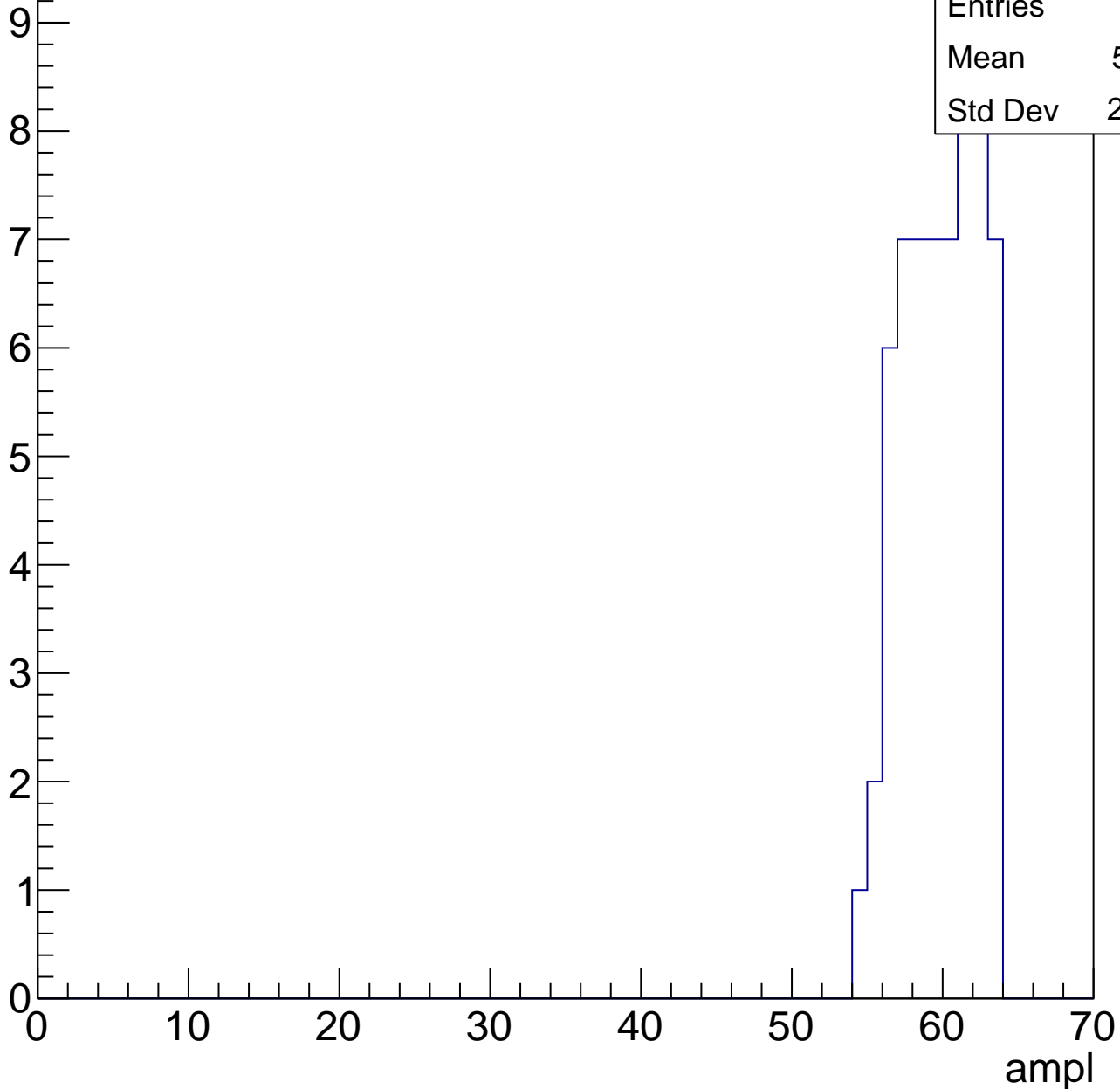
Entries	48
Mean	53.92
Std Dev	3.451



B1L103S, U12-ch32, adc5

calib_packv5_041523_1651.root, FC#0, port C2

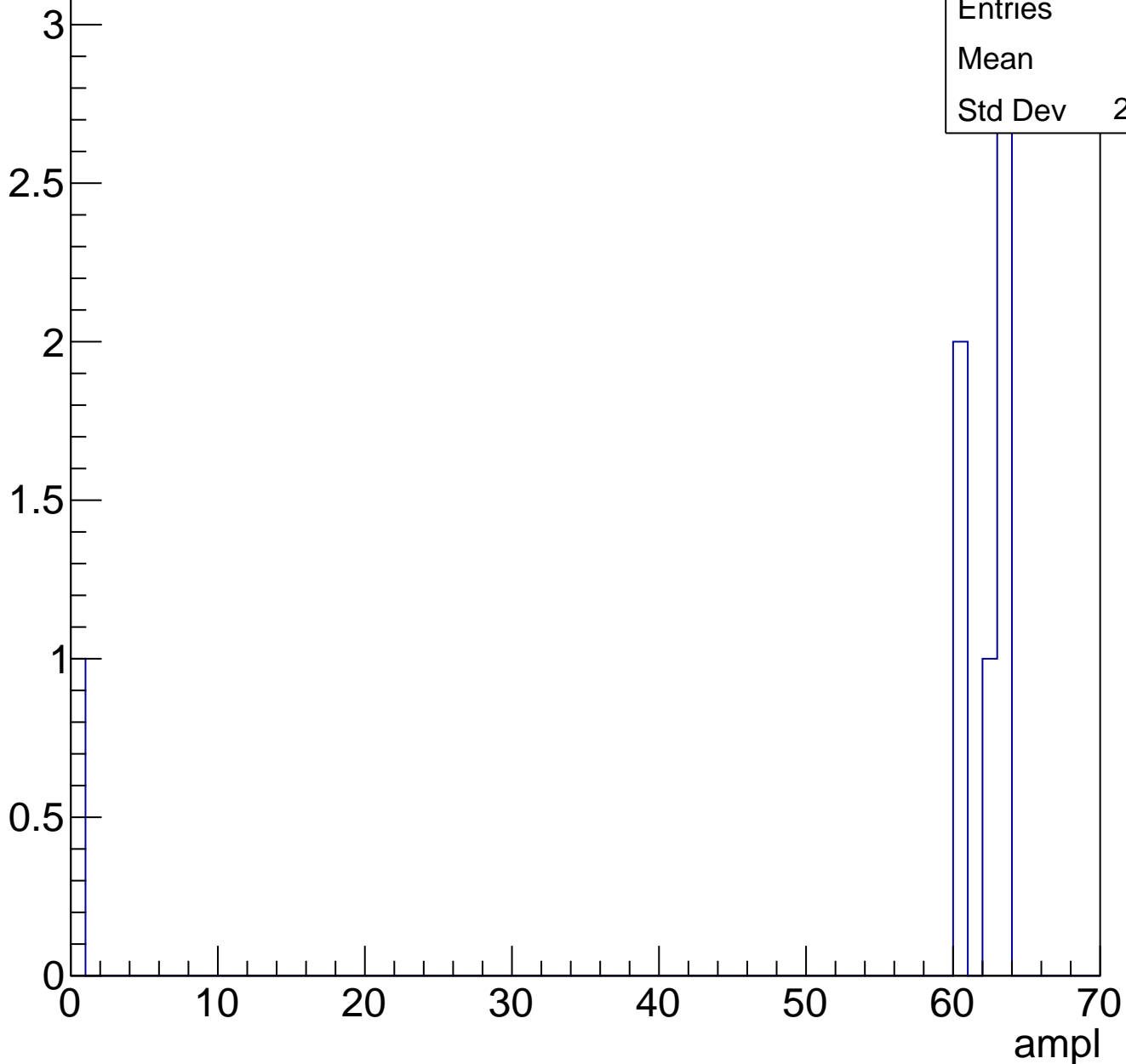
Entry



B1L103S, U12-ch32, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch32, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

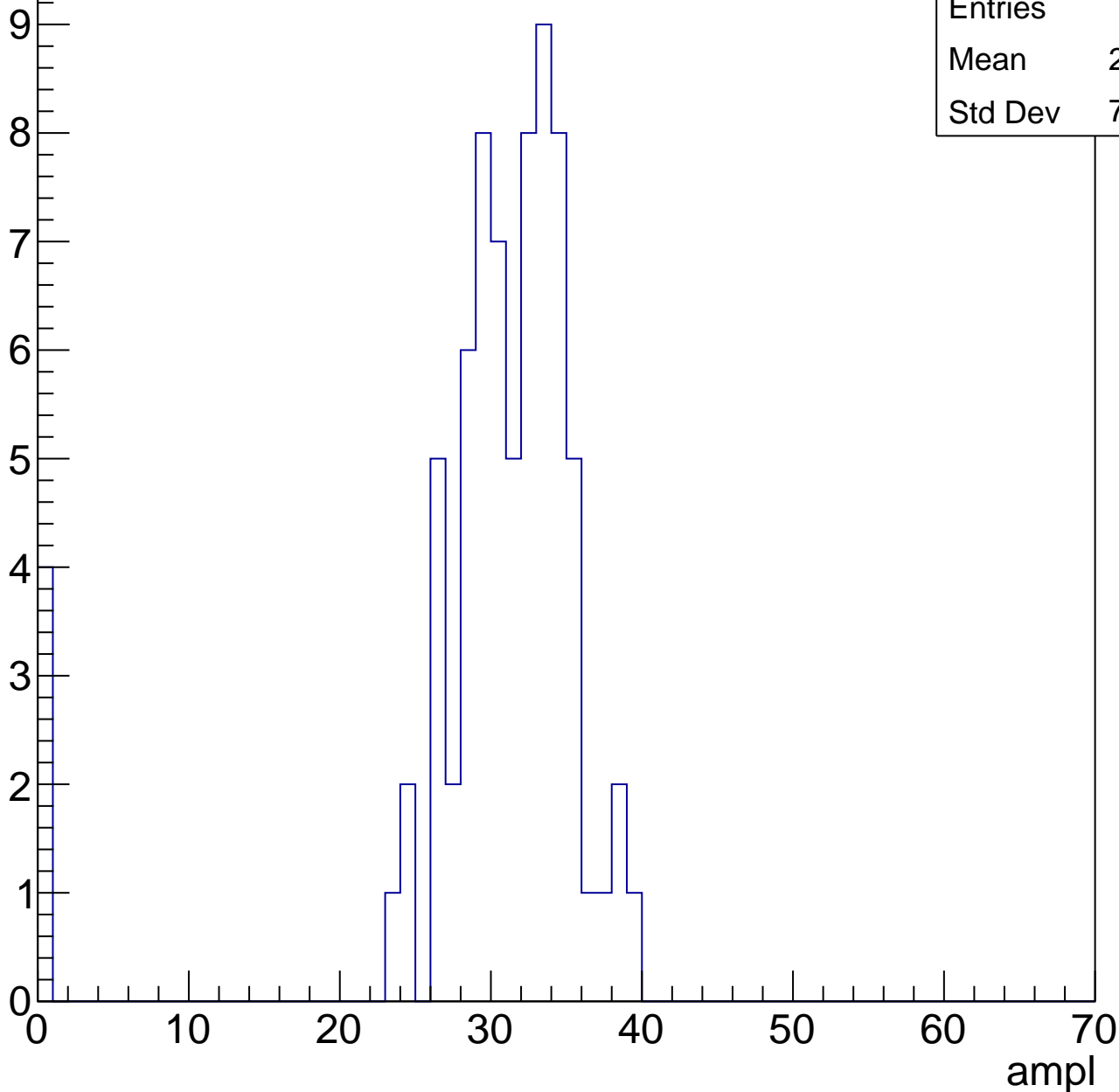
Entries	19
Mean	0
Std Dev	0

B1L103S, U12-ch33, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	75
Mean	29.44
Std Dev	7.739

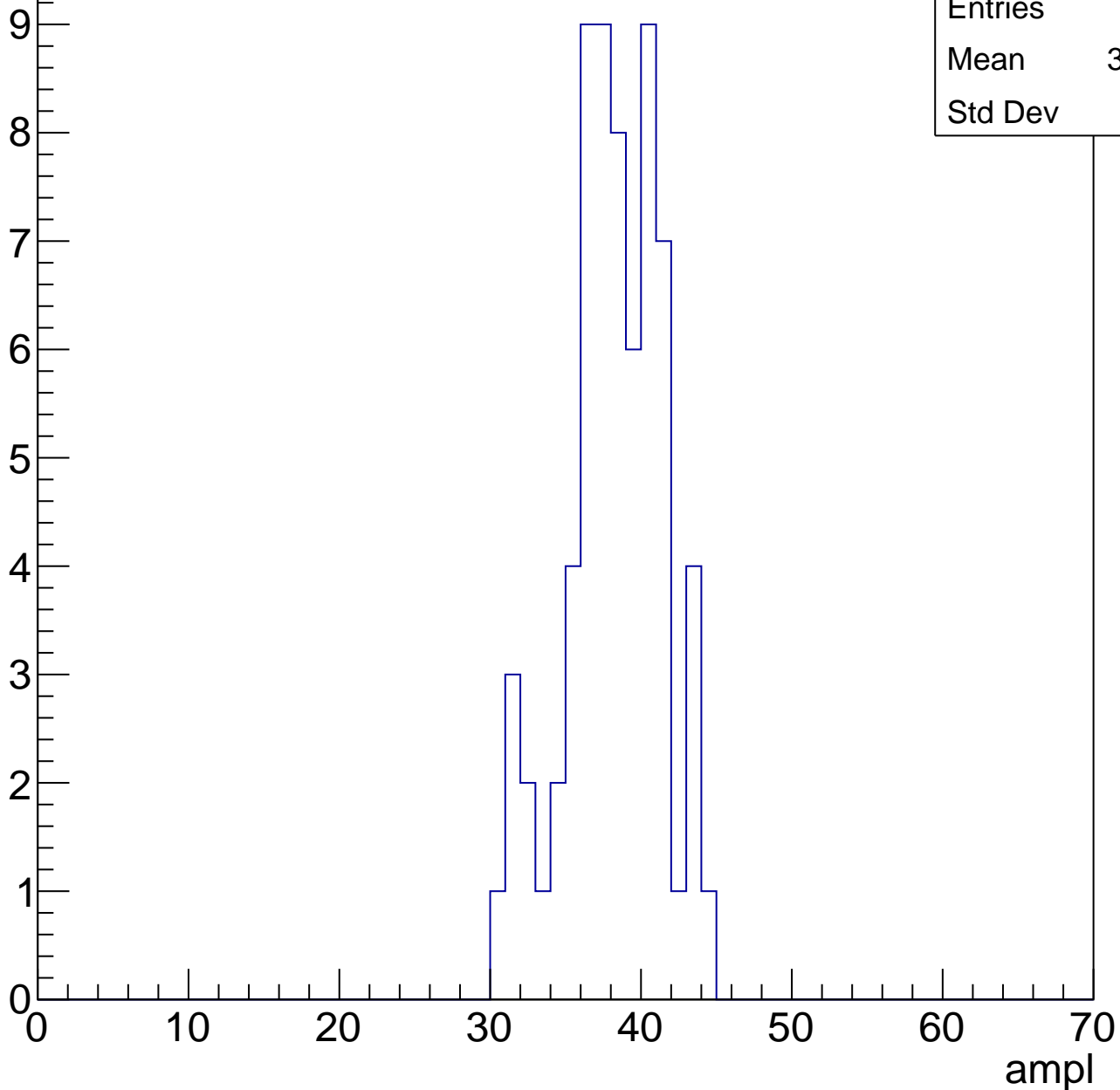


B1L103S, U12-ch33, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	37.73
Std Dev	3.17

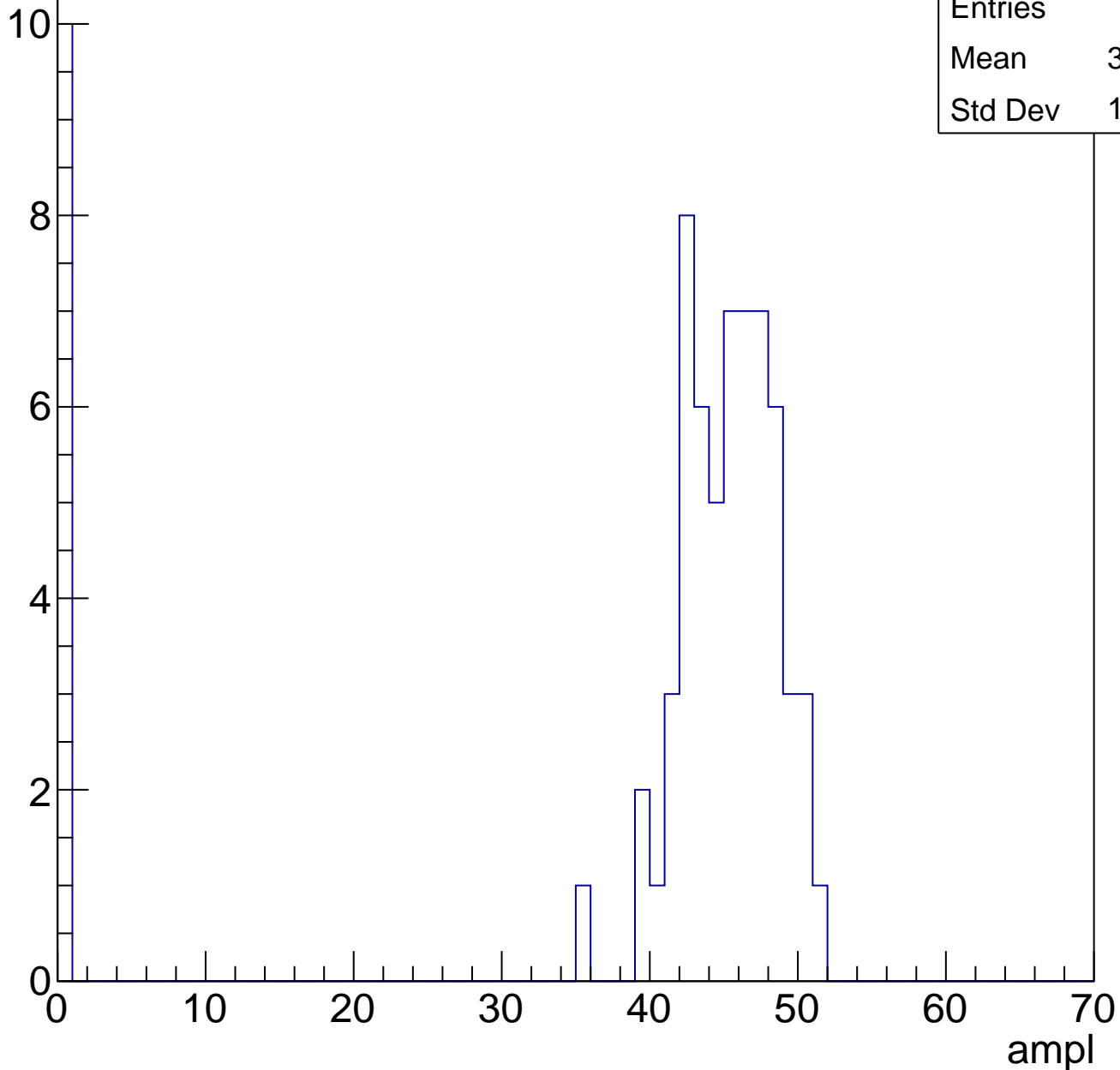


B1L103S, U12-ch33, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	70
Mean	38.46
Std Dev	15.97

Entry

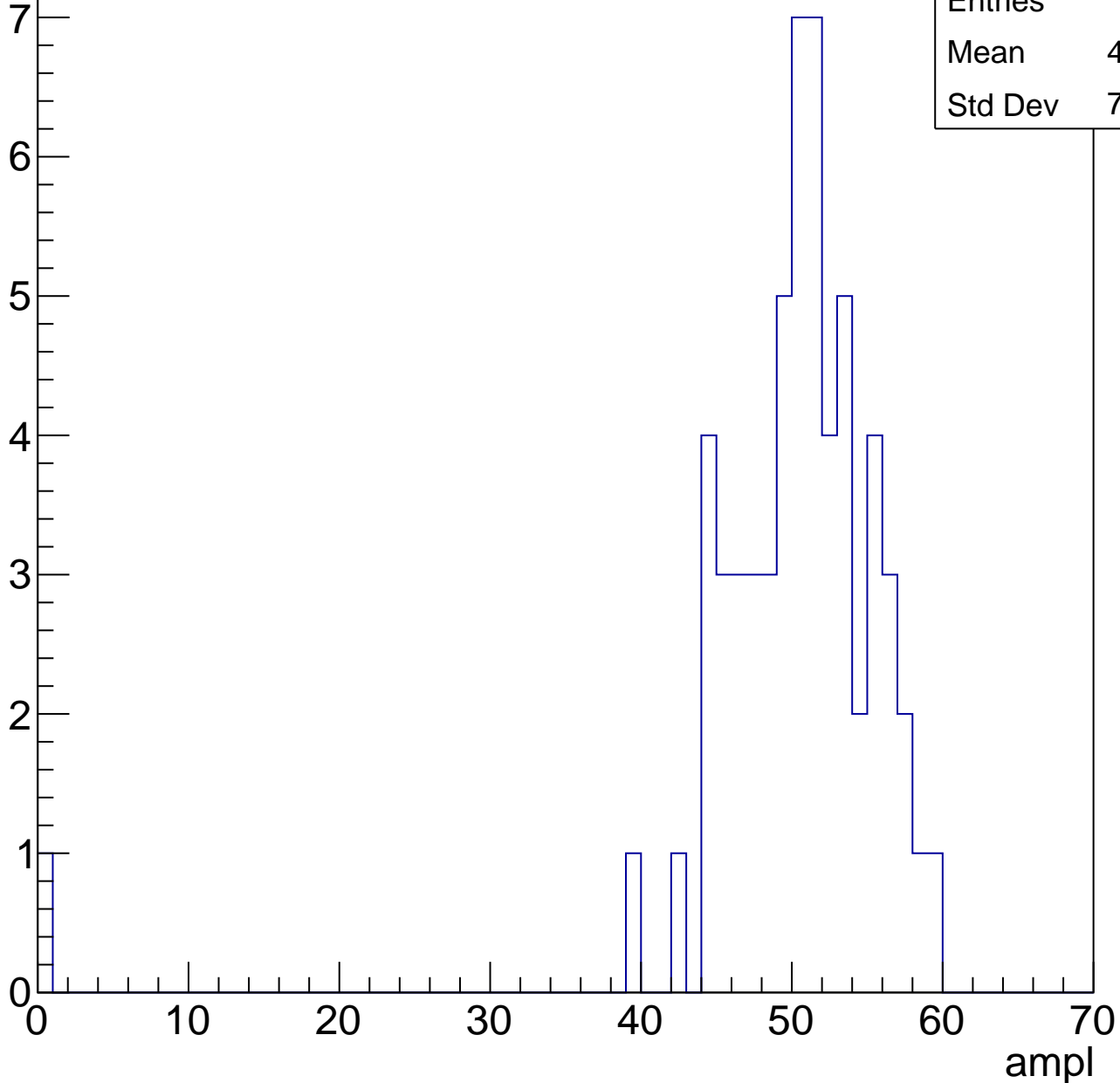


B1L103S, U12-ch33, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	49.45
Std Dev	7.669

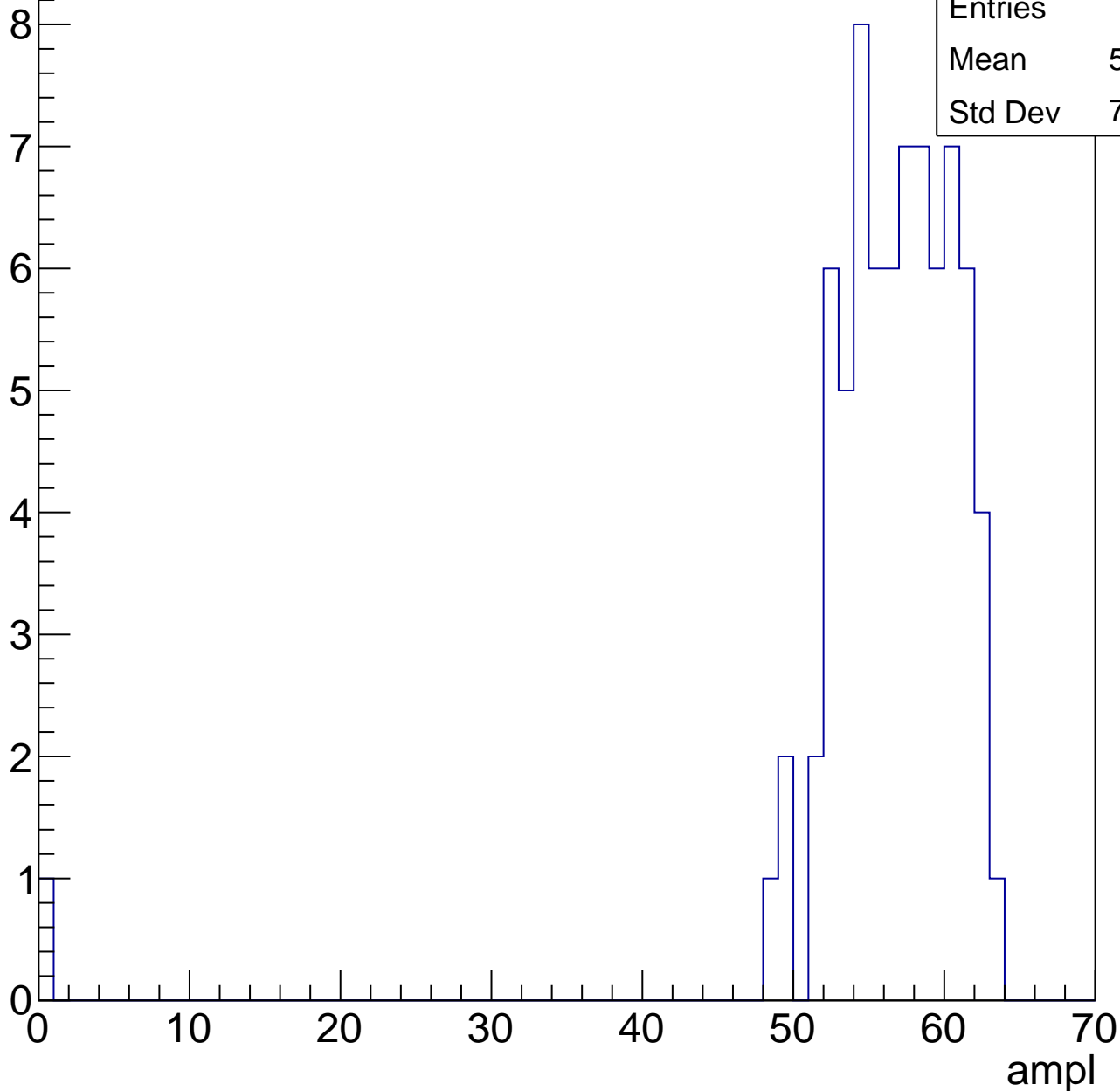


B1L103S, U12-ch33, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	75
Mean	55.72
Std Dev	7.362

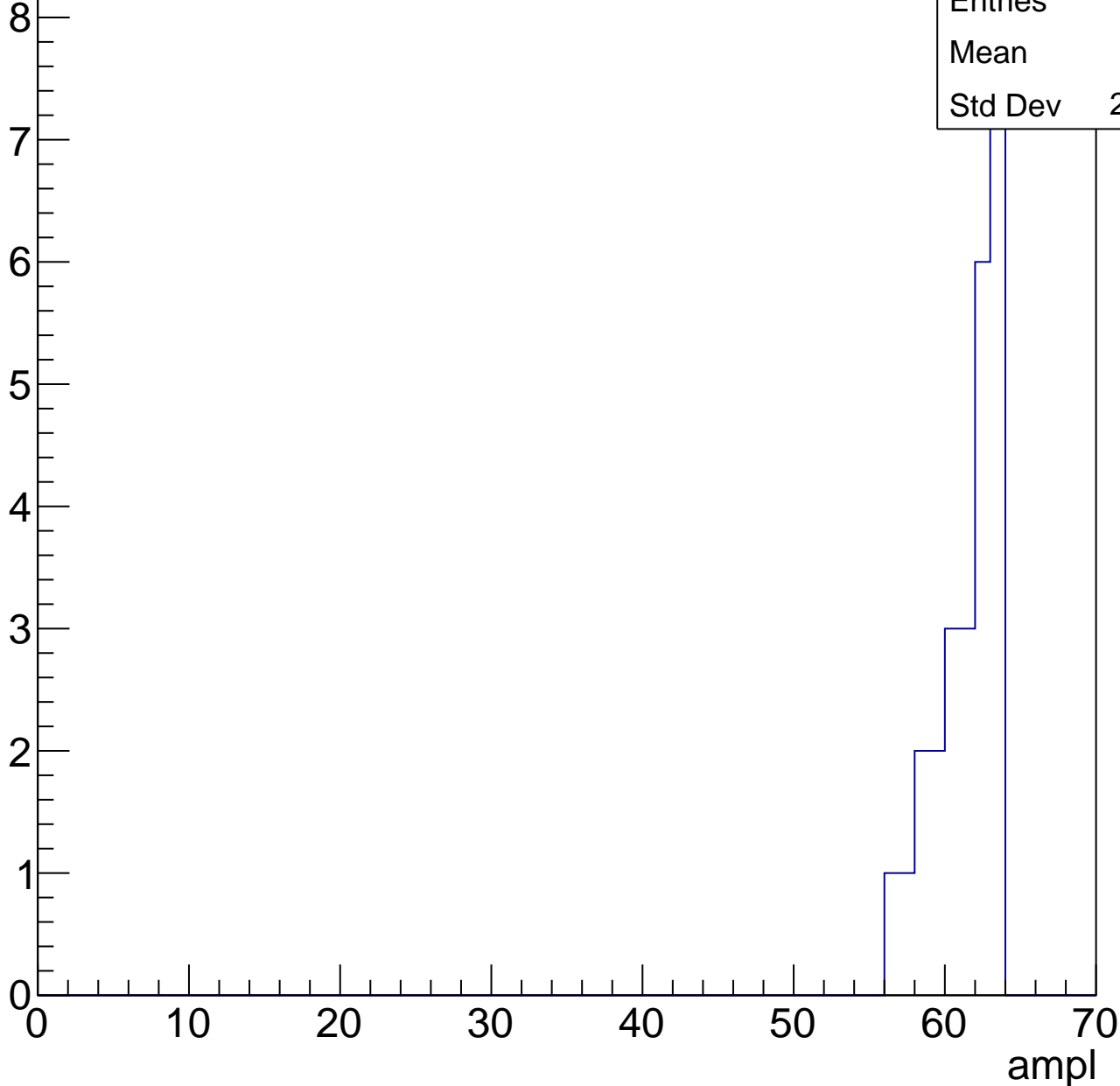


B1L103S, U12-ch33, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

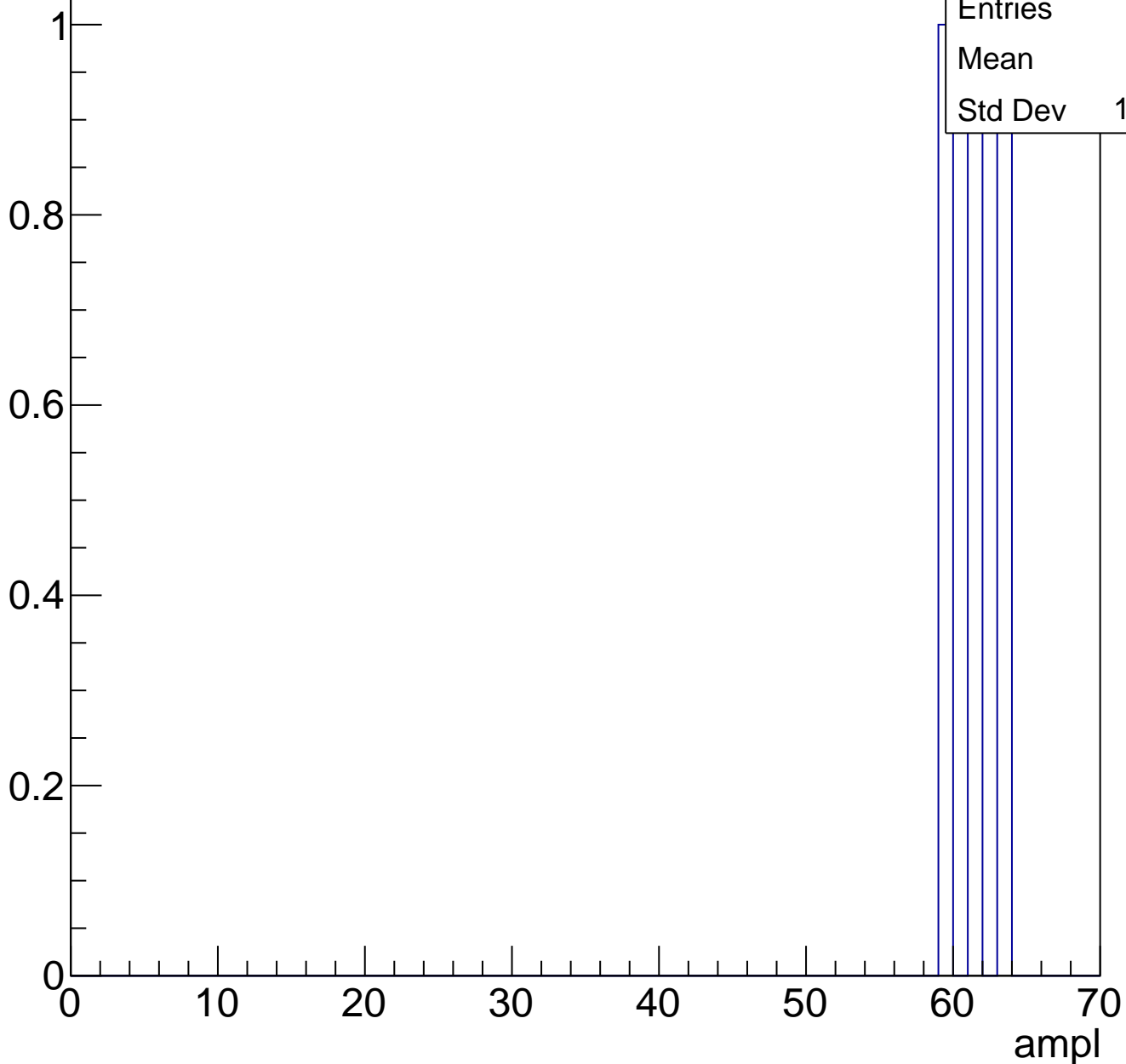
Entries	26
Mean	61
Std Dev	2.038



B1L103S, U12-ch33, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch33, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	18
Mean	1.222
Std Dev	5.039

Entry

16
14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70

B1L103S, U12-ch34, adc0

calib_packv5_041523_1651.root, FC#0, port C2

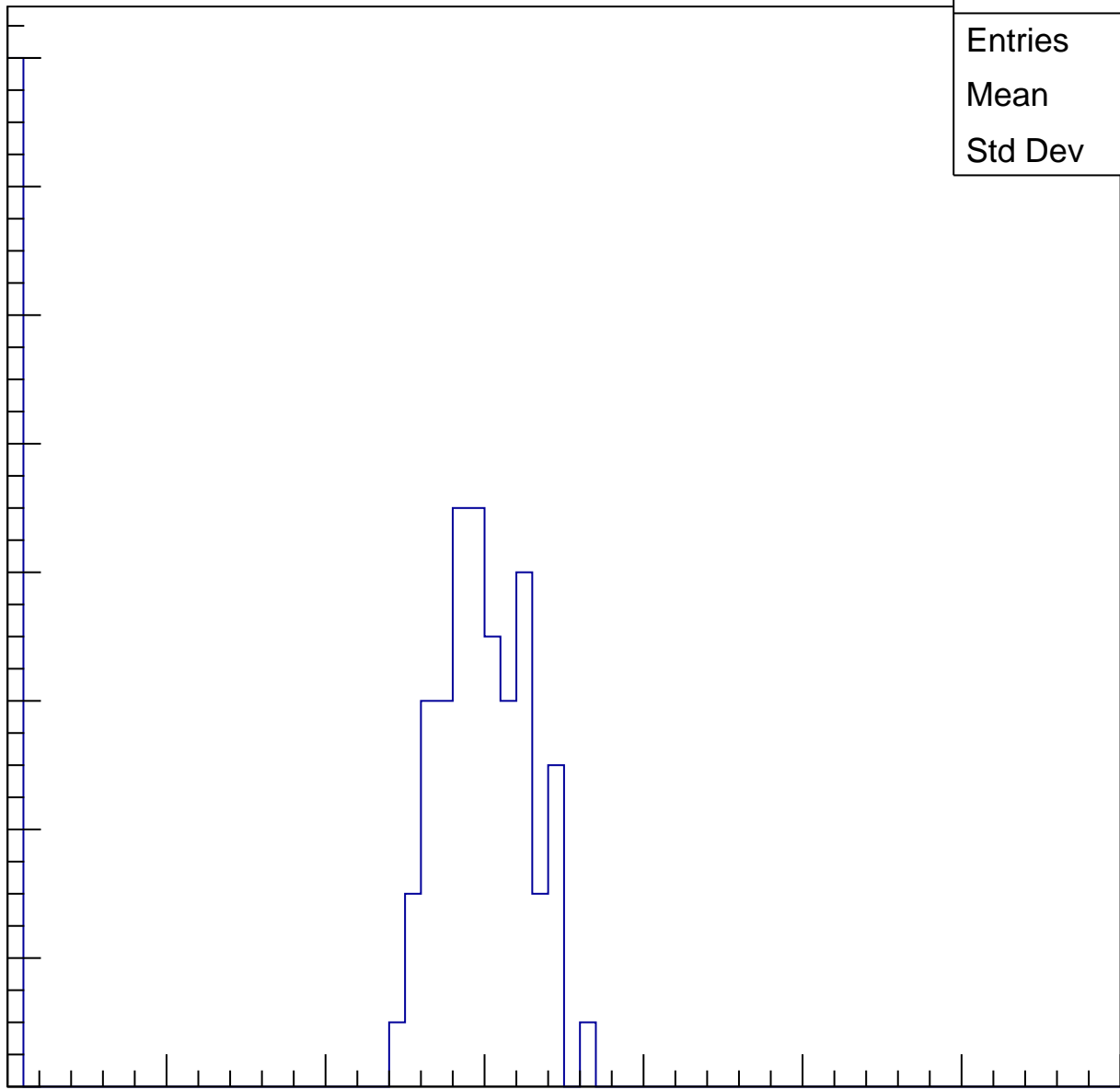
Entries	80
Mean	23.59
Std Dev	12.04

Entry

16
14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70

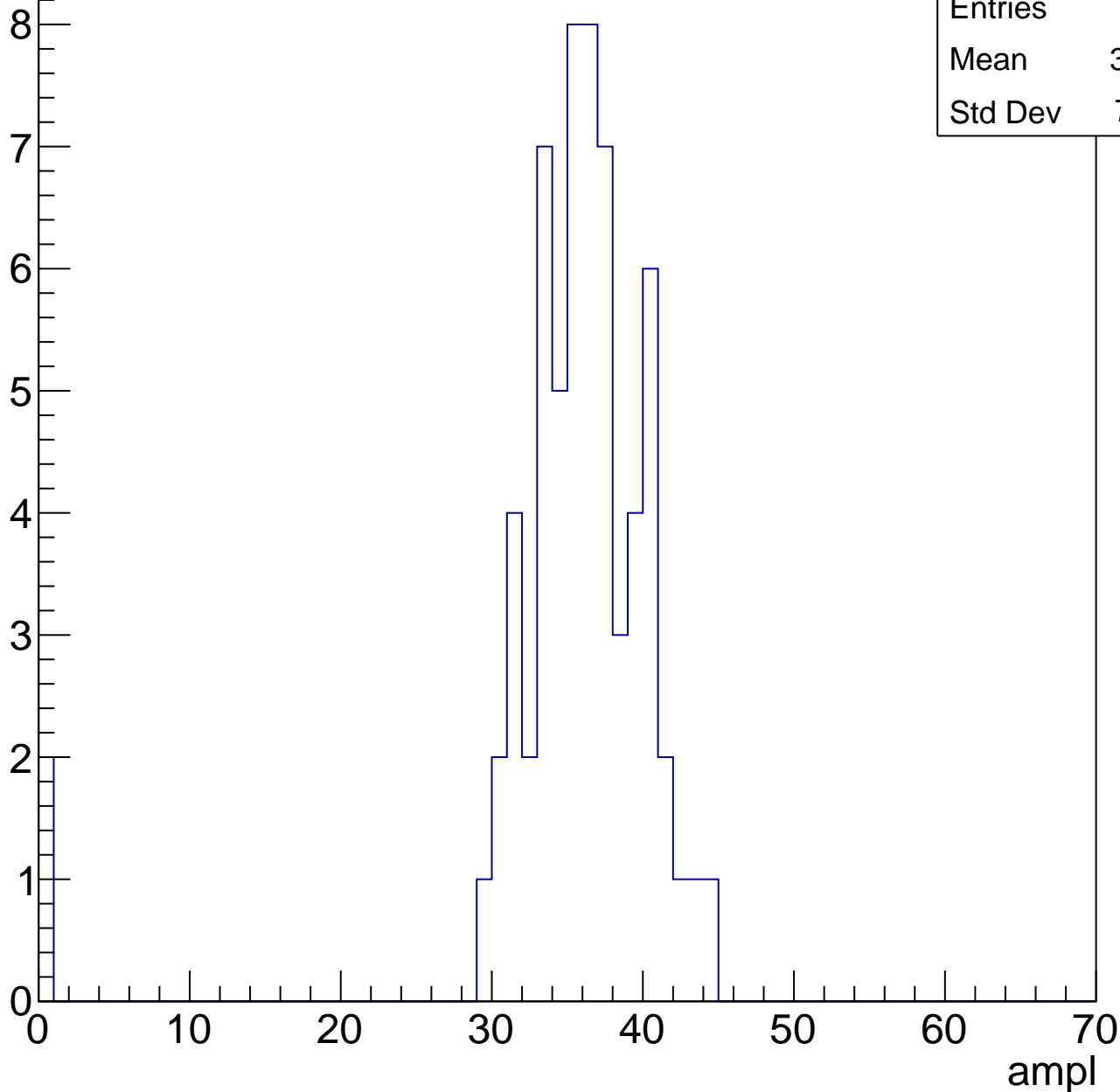


B1L103S, U12-ch34, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	34.78
Std Dev	7.061



B1L103S, U12-ch34, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

10

8

6

4

2

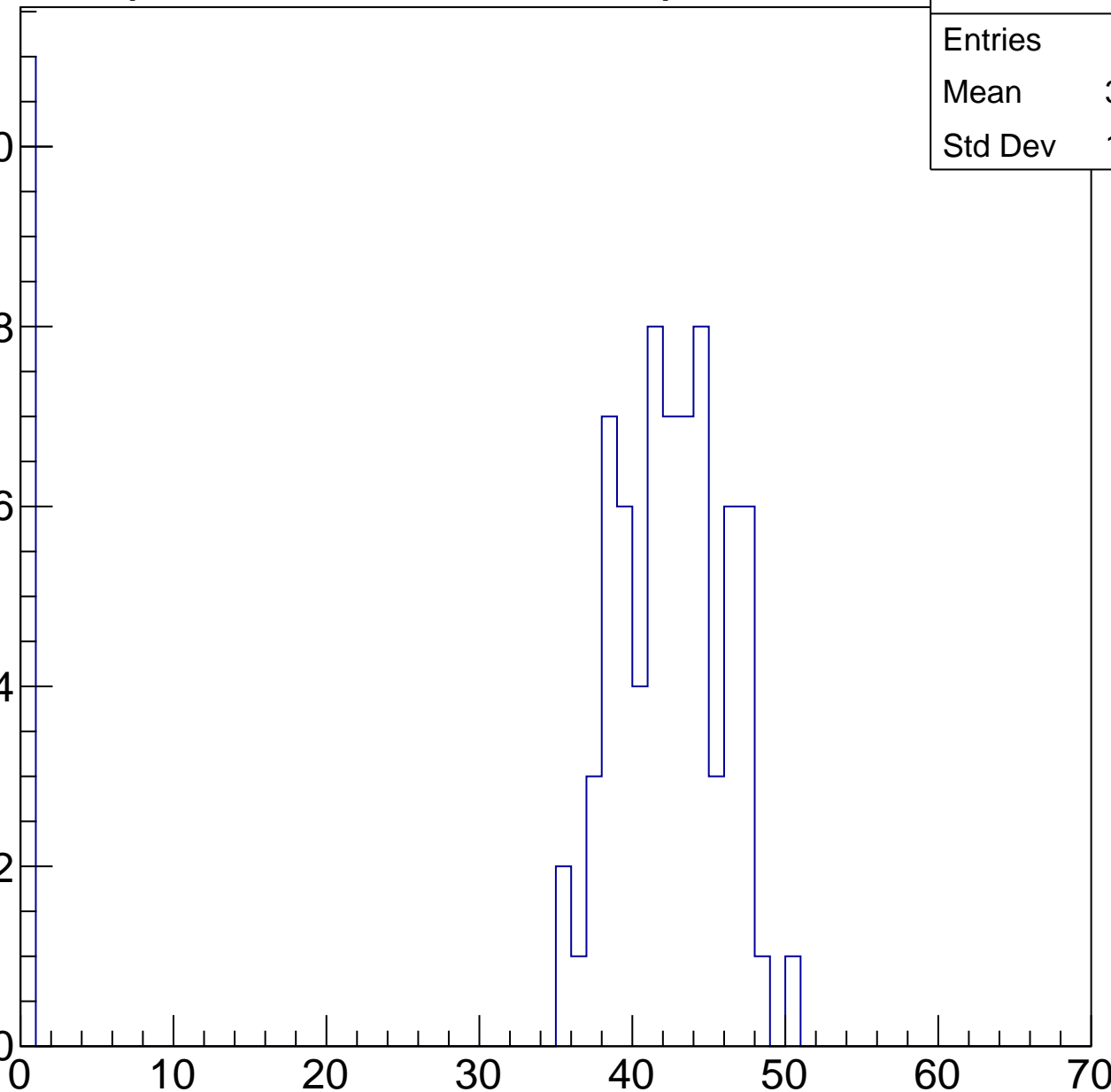
0

Entries 81

Mean 36.33

Std Dev 14.75

ampl

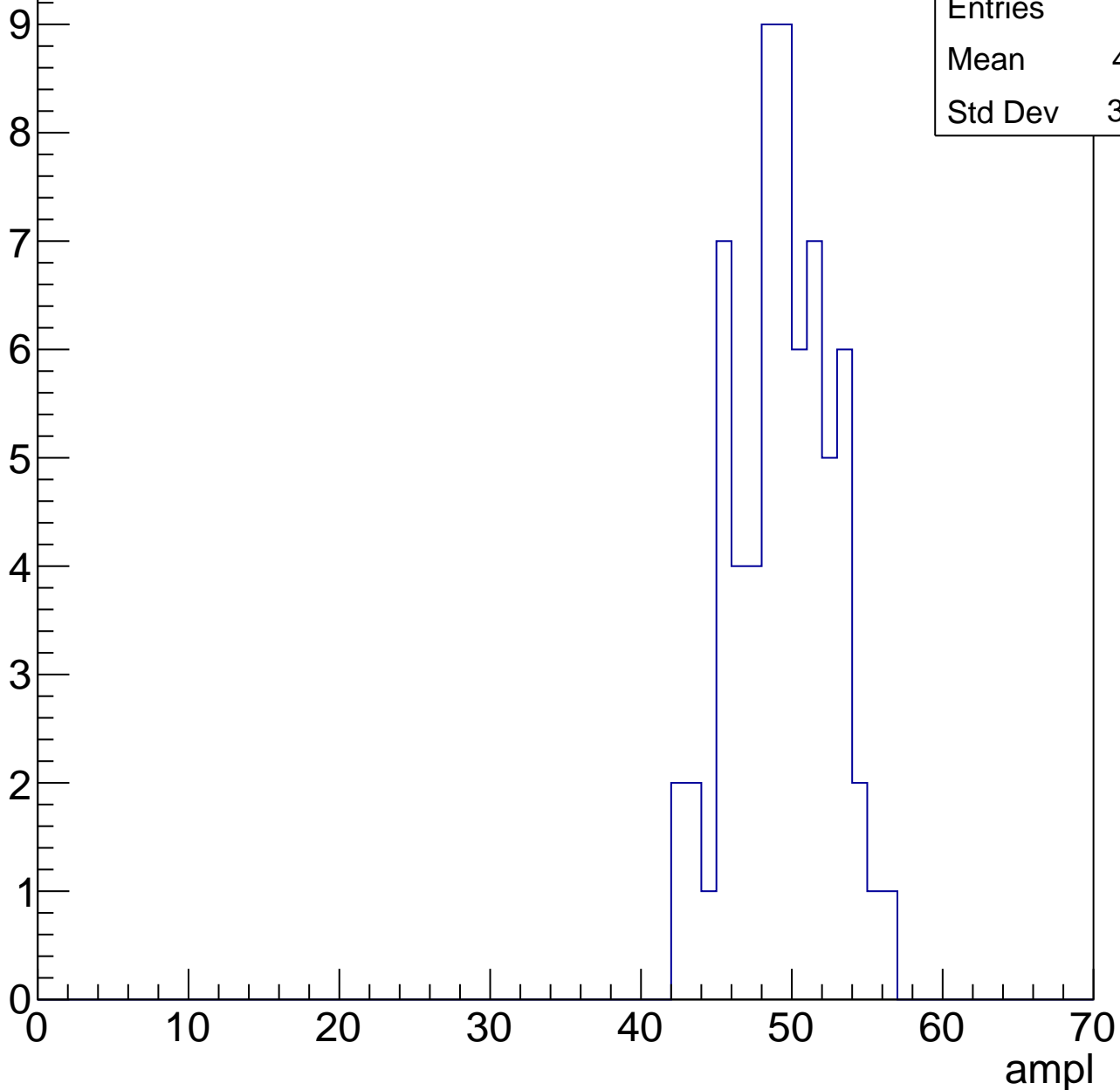


B1L103S, U12-ch34, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

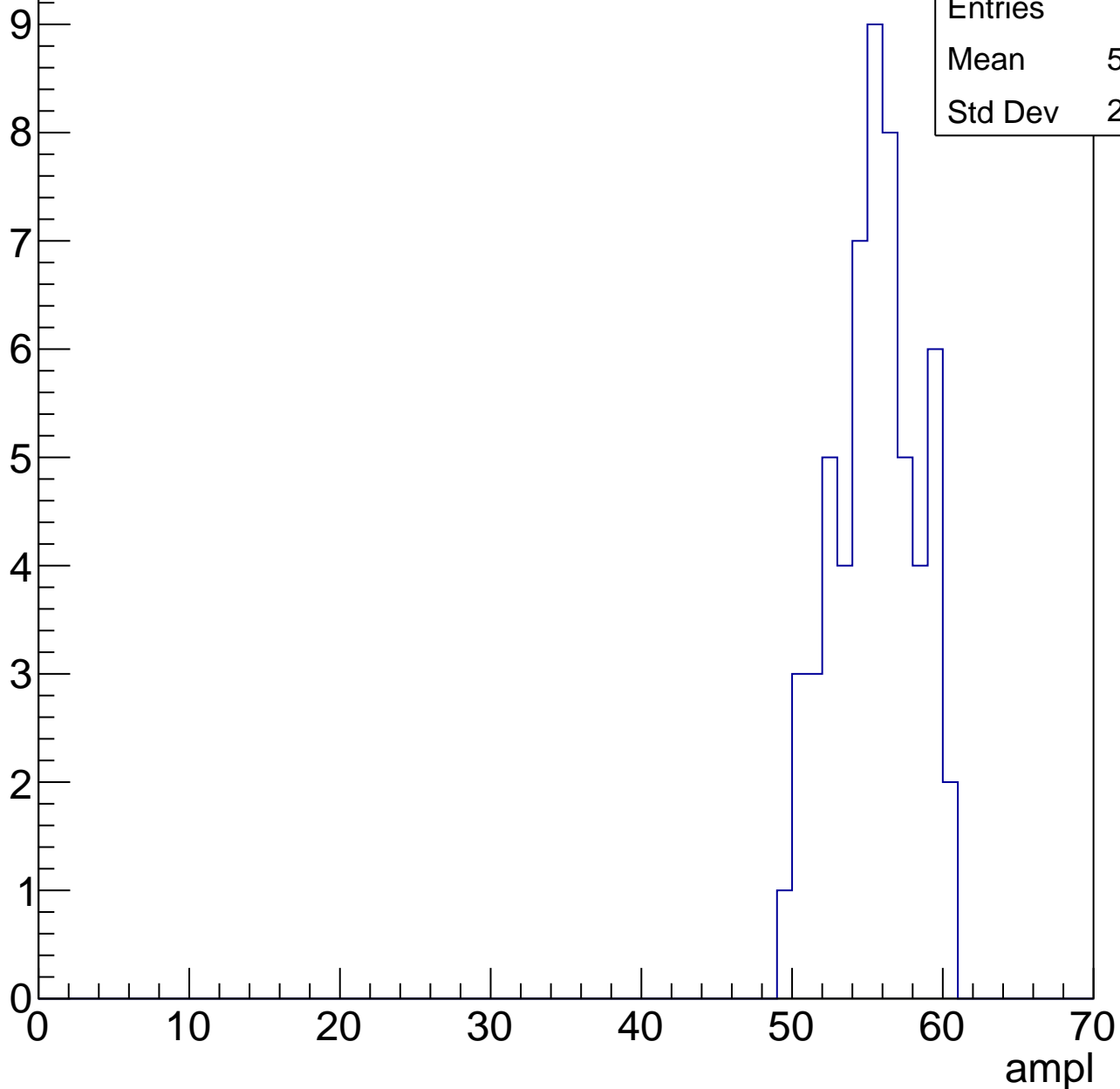
Entries	66
Mean	48.91
Std Dev	3.204



B1L103S, U12-ch34, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch34, adc5

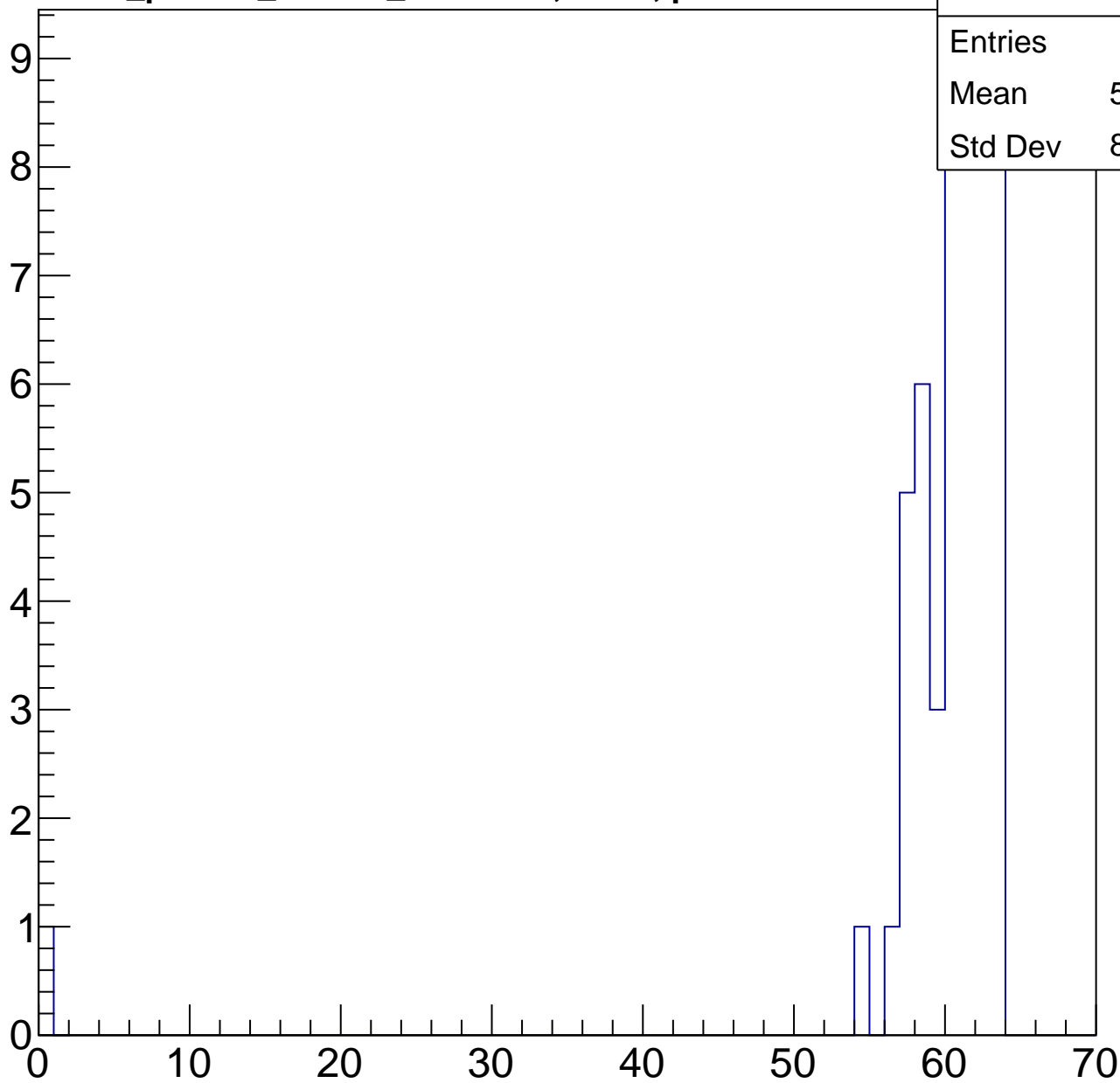
calib_packv5_041523_1651.root, FC#0, port C2

Entry

9
8
7
6
5
4
3
2
1
0

Entries	51
Mean	59.06
Std Dev	8.633

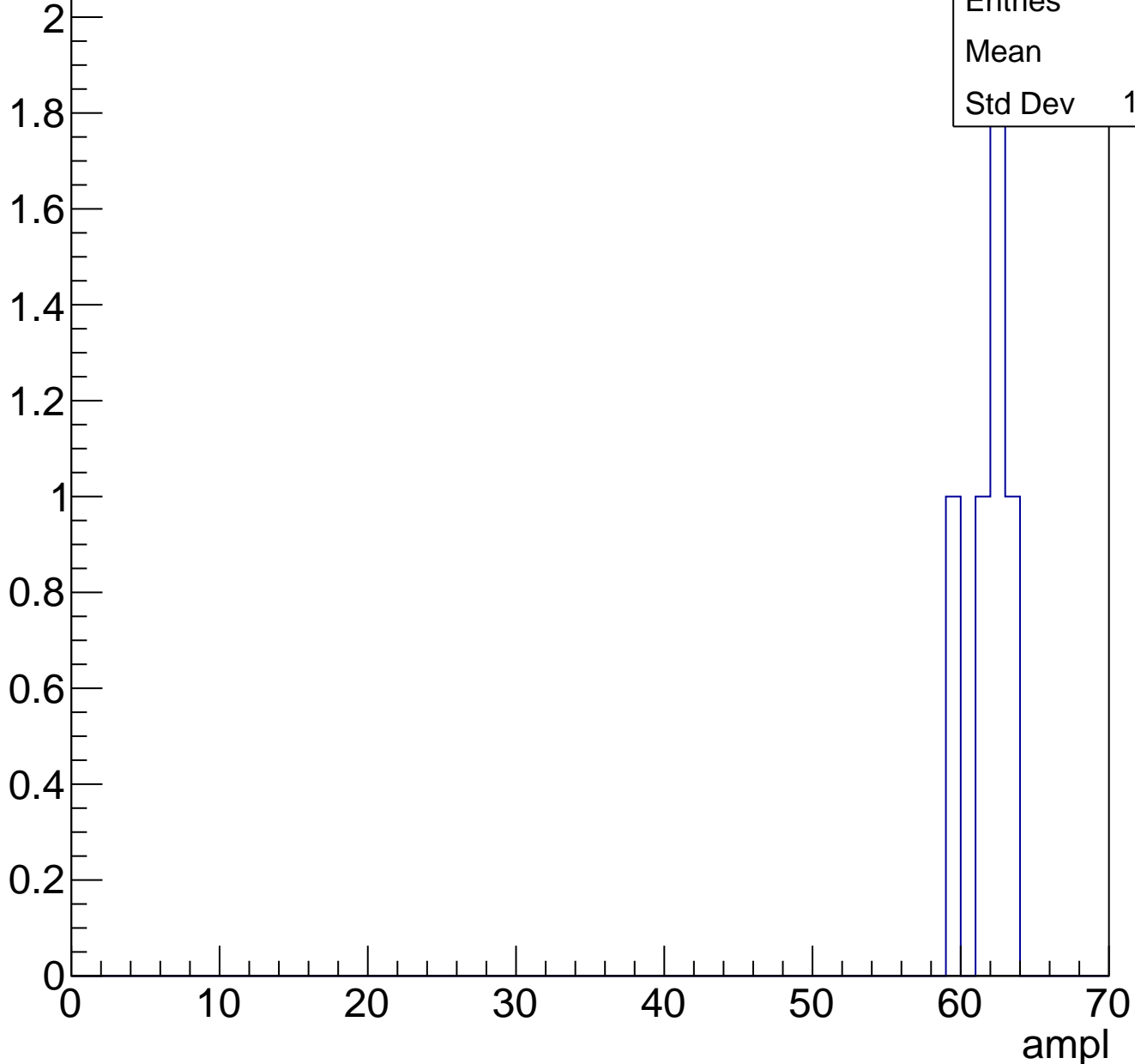
ampl



B1L103S, U12-ch34, adc6

calib_packv5_041523_1651.root, FC#0, port C2

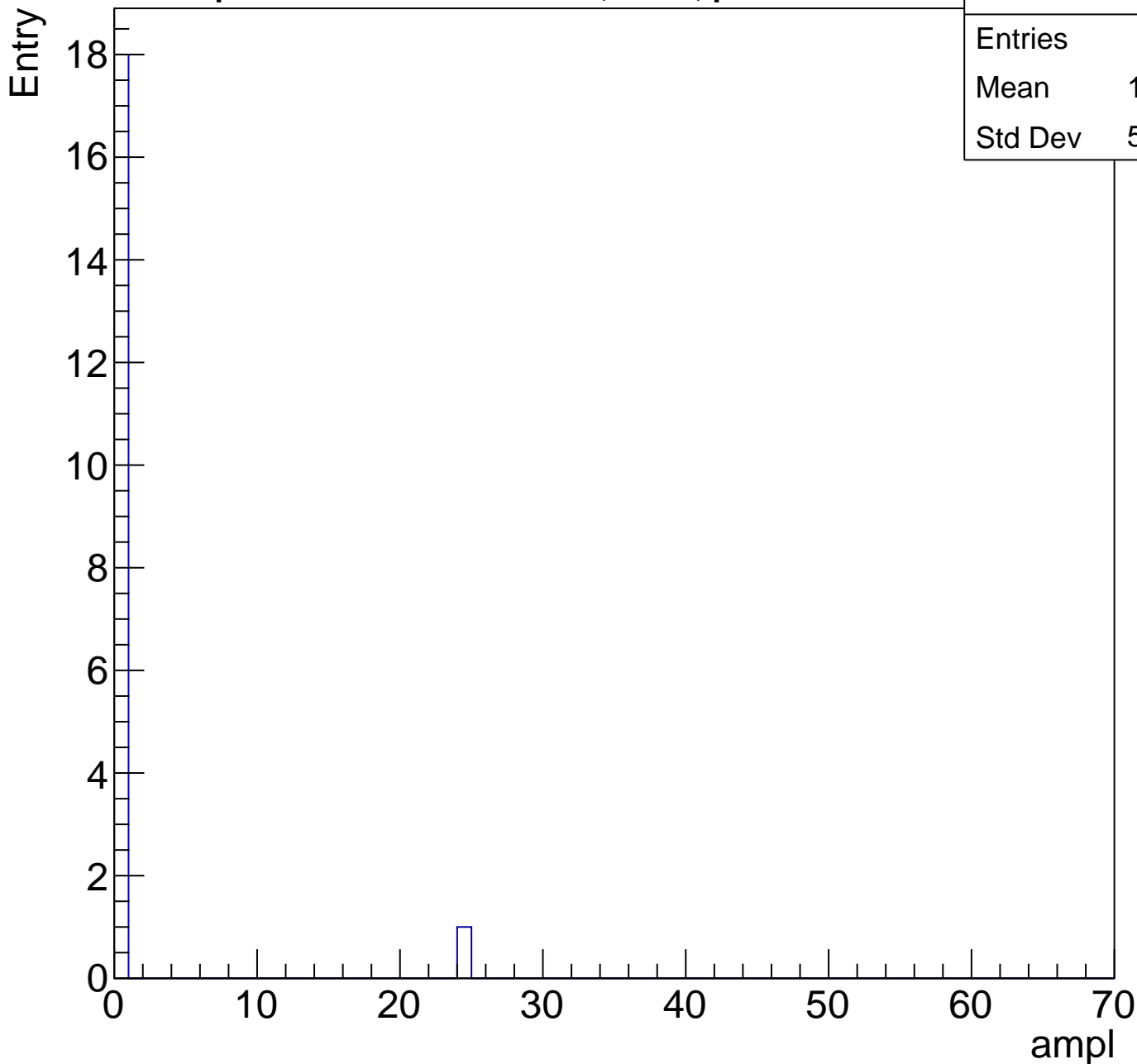
Entry



B1L103S, U12-ch34, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.263
Std Dev	5.359

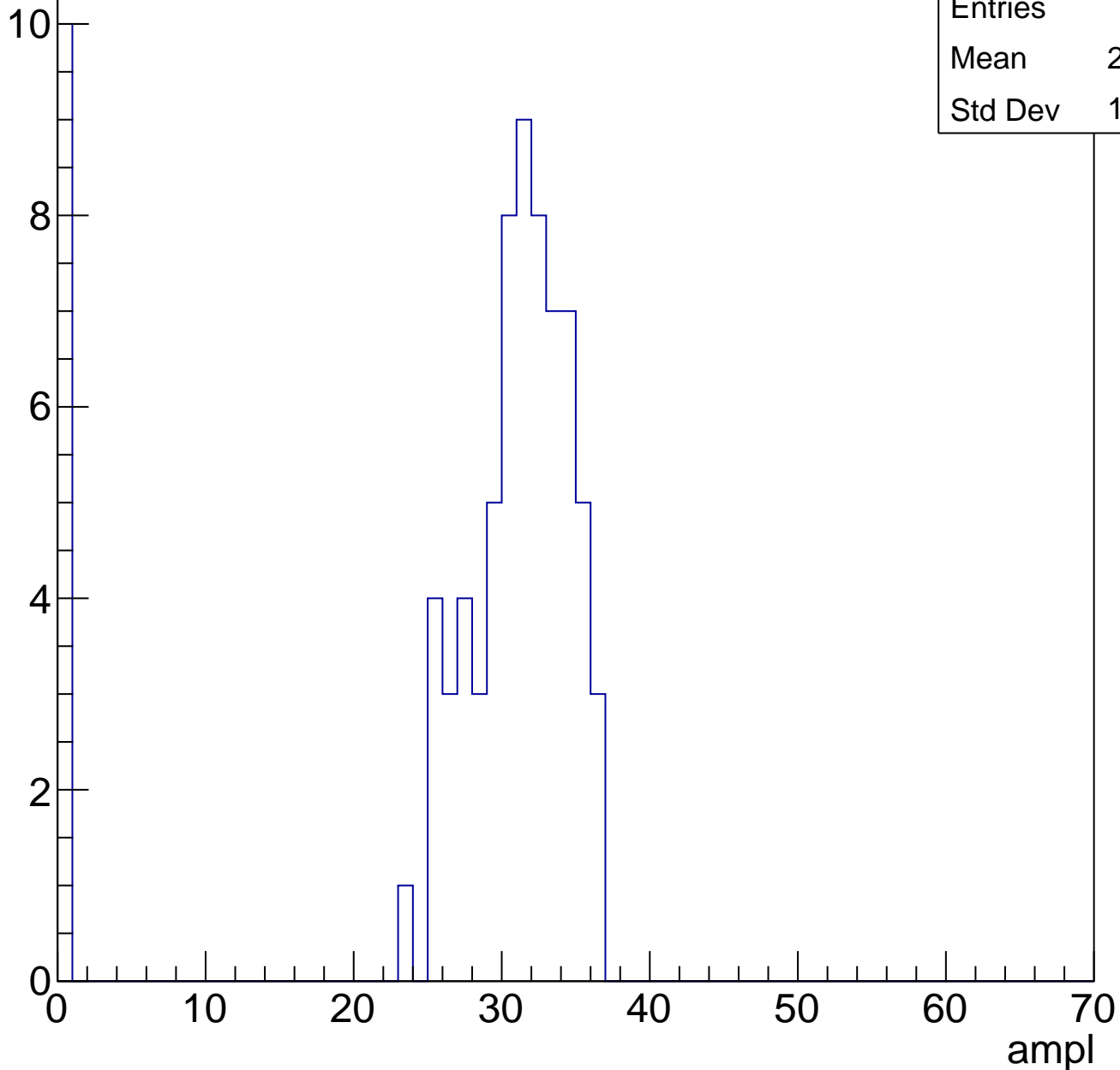


B1L103S, U12-ch35, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	77
Mean	26.82
Std Dev	10.76

Entry

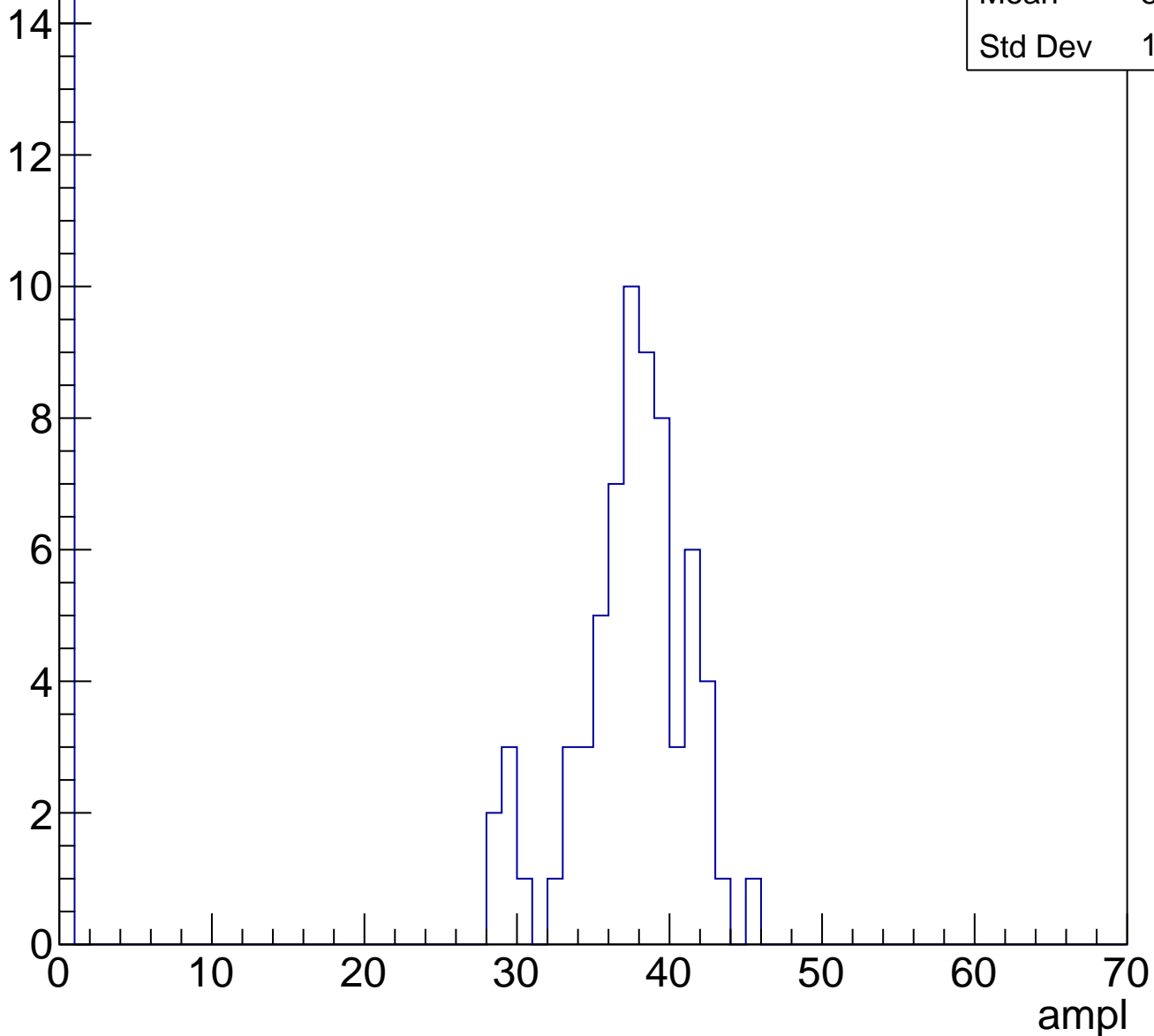


B1L103S, U12-ch35, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	82
Mean	30.23
Std Dev	14.68

Entry

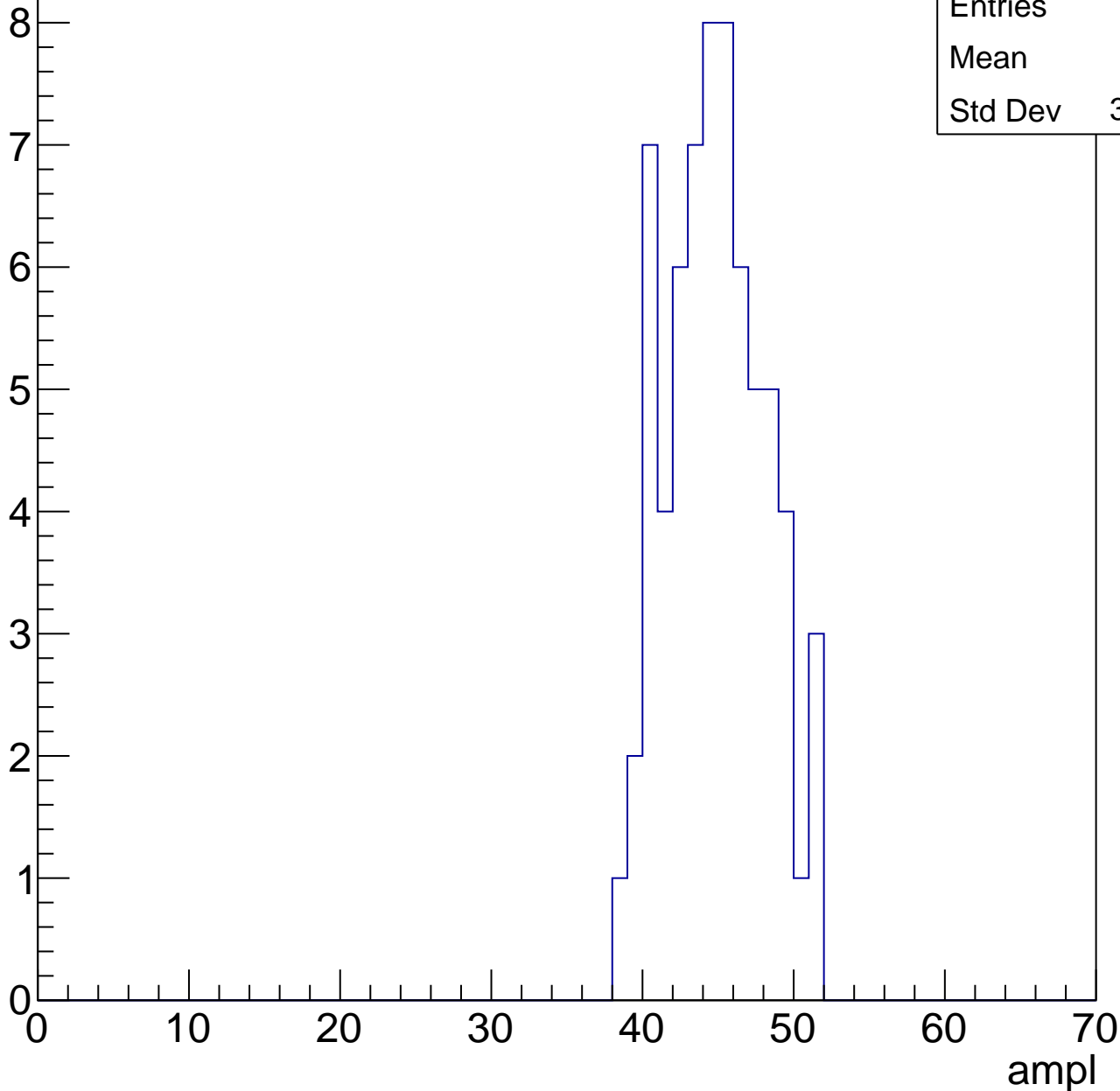


B1L103S, U12-ch35, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	44.4
Std Dev	3.219

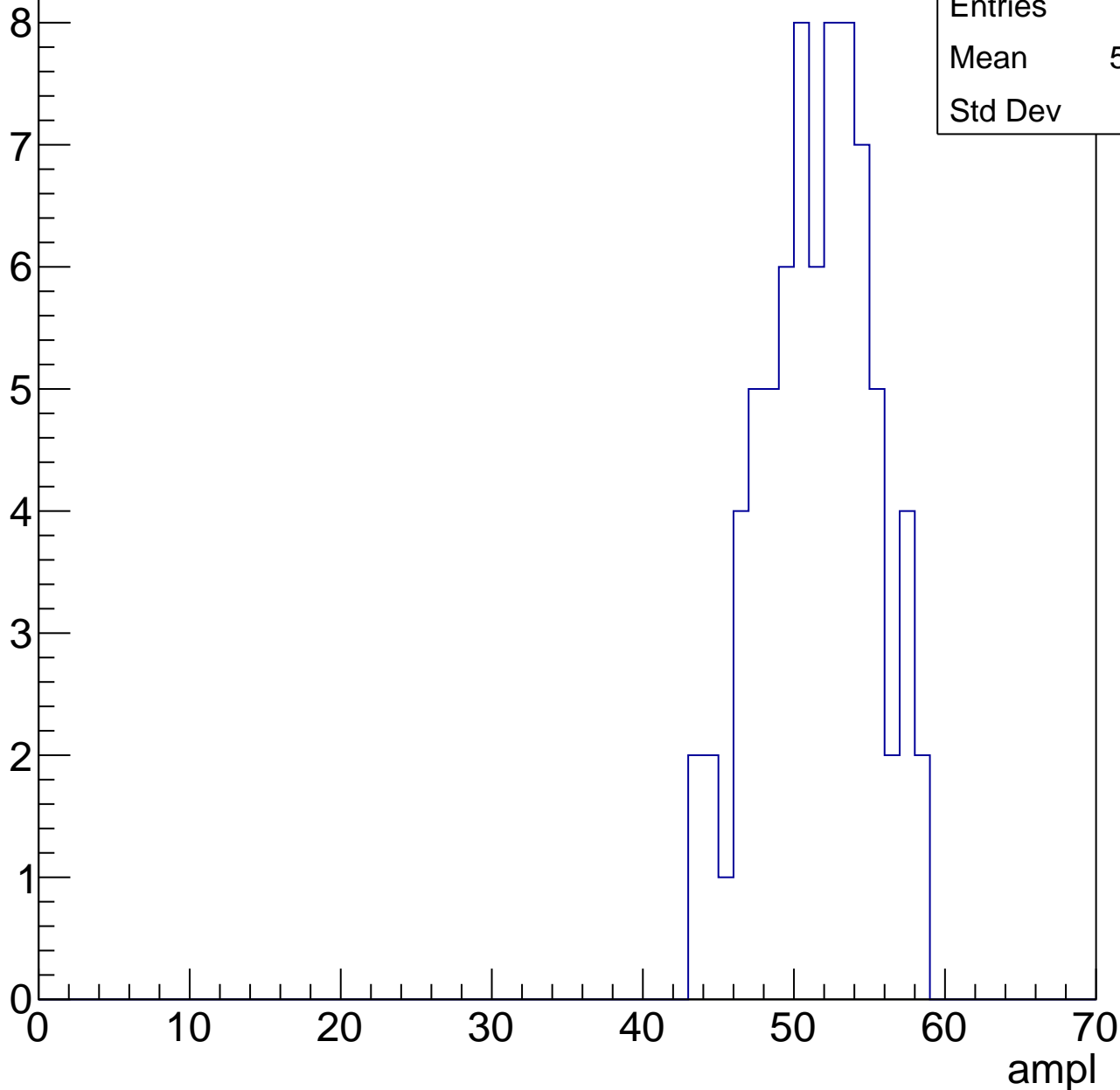


B1L103S, U12-ch35, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	75
Mean	51.03
Std Dev	3.64

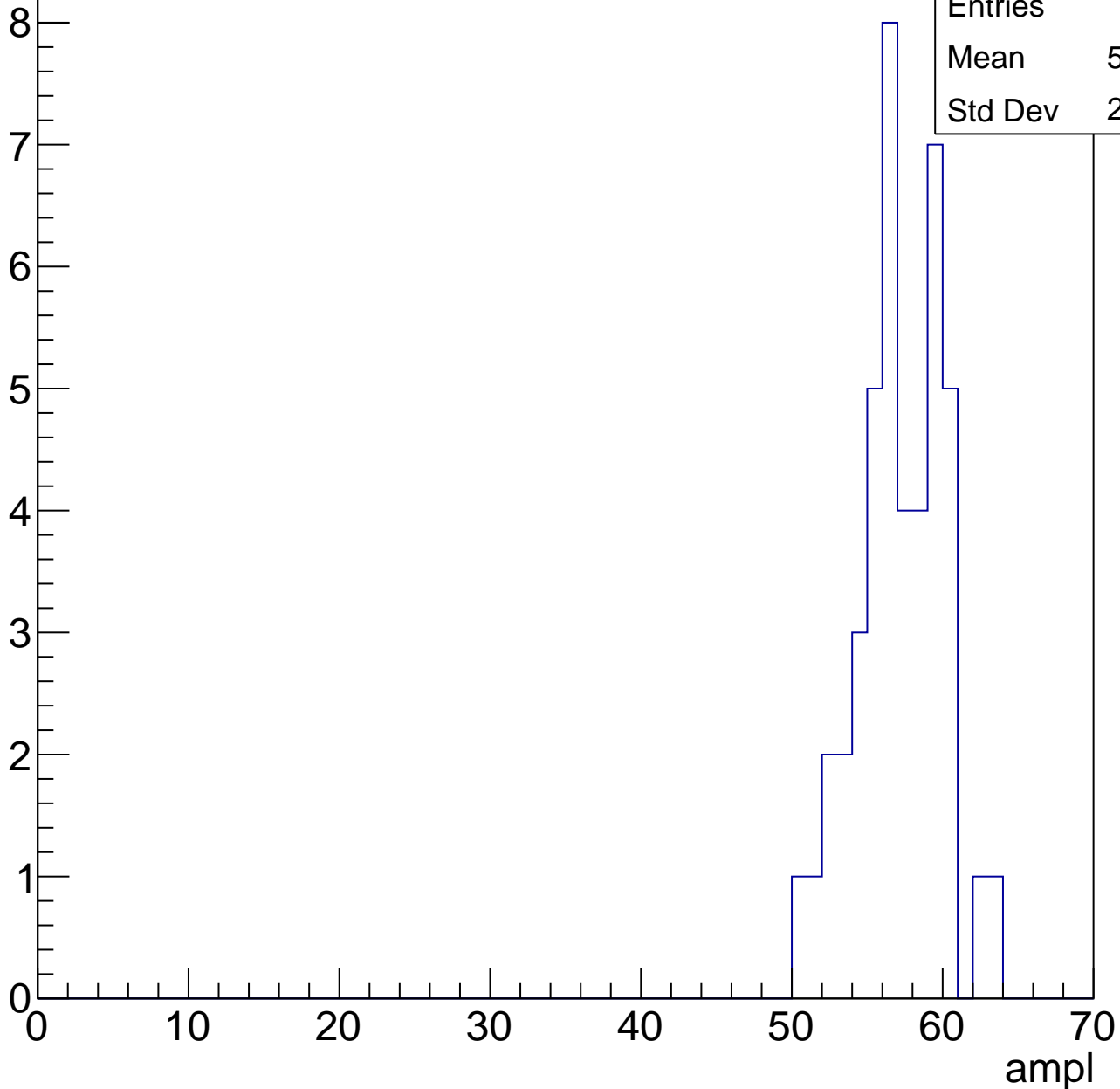


B1L103S, U12-ch35, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	44
Mean	56.68
Std Dev	2.843

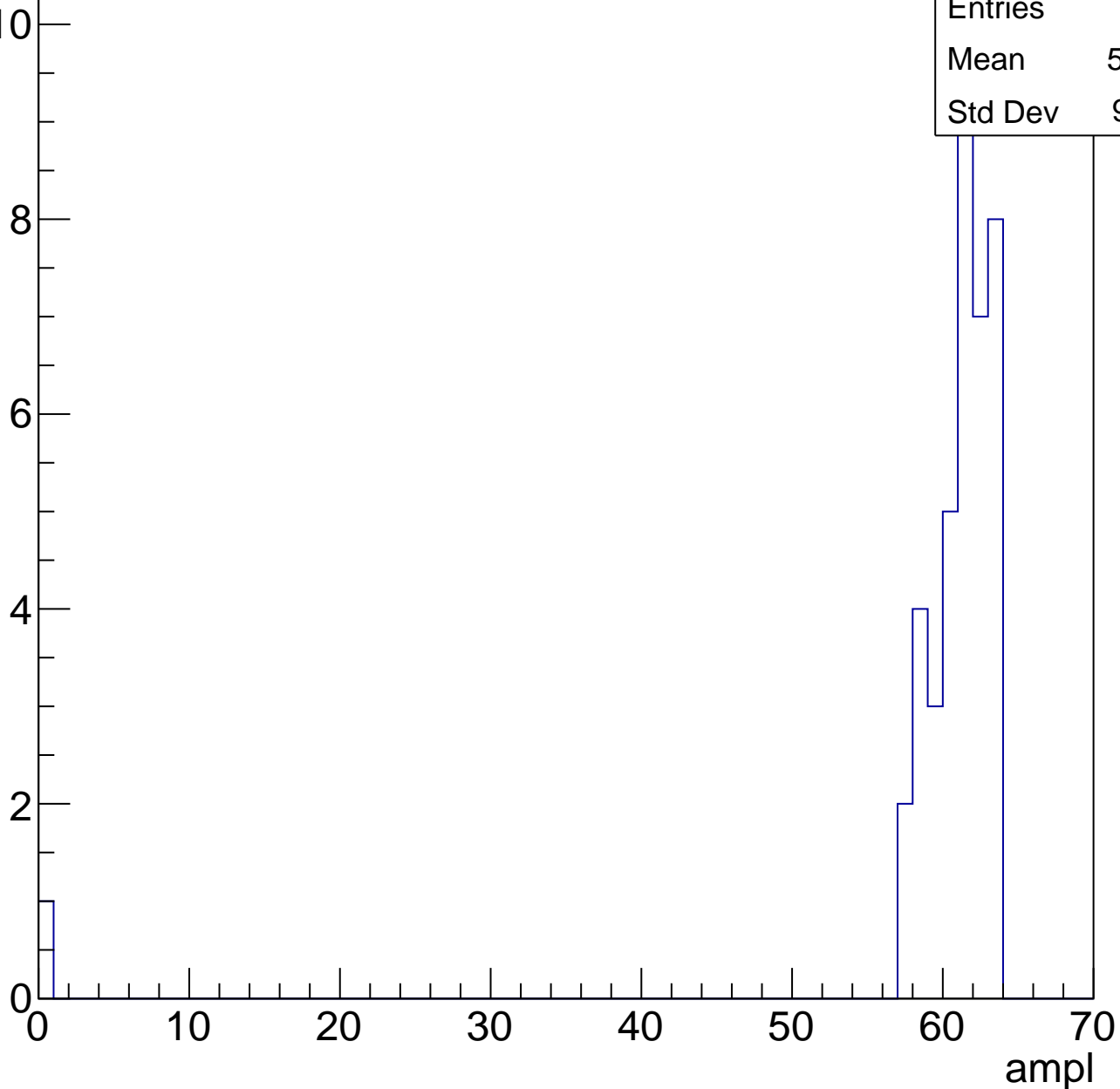


B1L103S, U12-ch35, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	40
Mean	59.27
Std Dev	9.651



B1L103S, U12-ch35, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	3
Mean	62.33
Std Dev	0.4714

ampl

0 10 20 30 40 50 60 70

B1L103S, U12-ch35, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch36, adc0

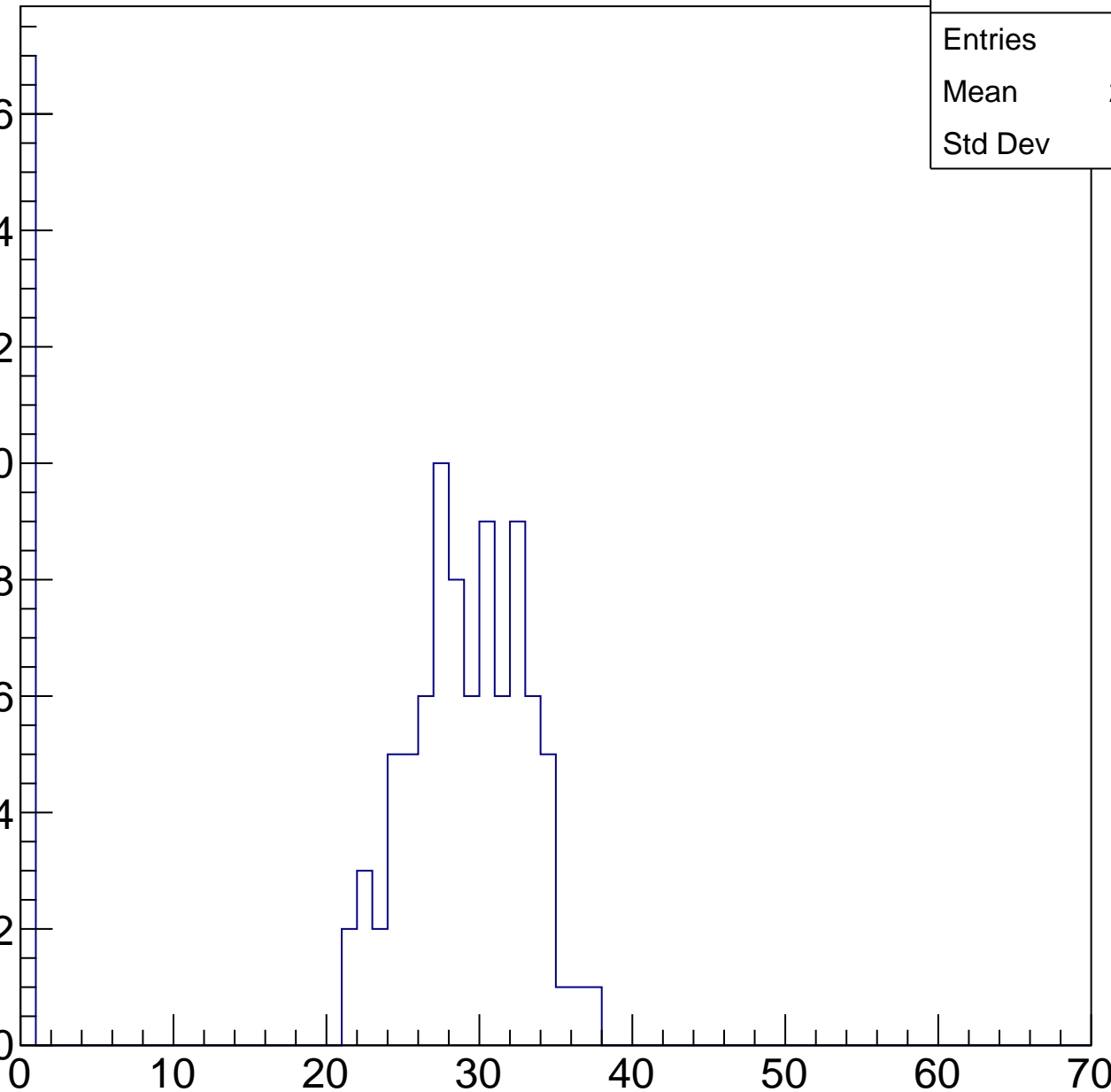
calib_packv5_041523_1651.root, FC#0, port C2

Entries	102
Mean	23.95
Std Dev	11.22

Entry

16
14
12
10
8
6
4
2
0

ampl

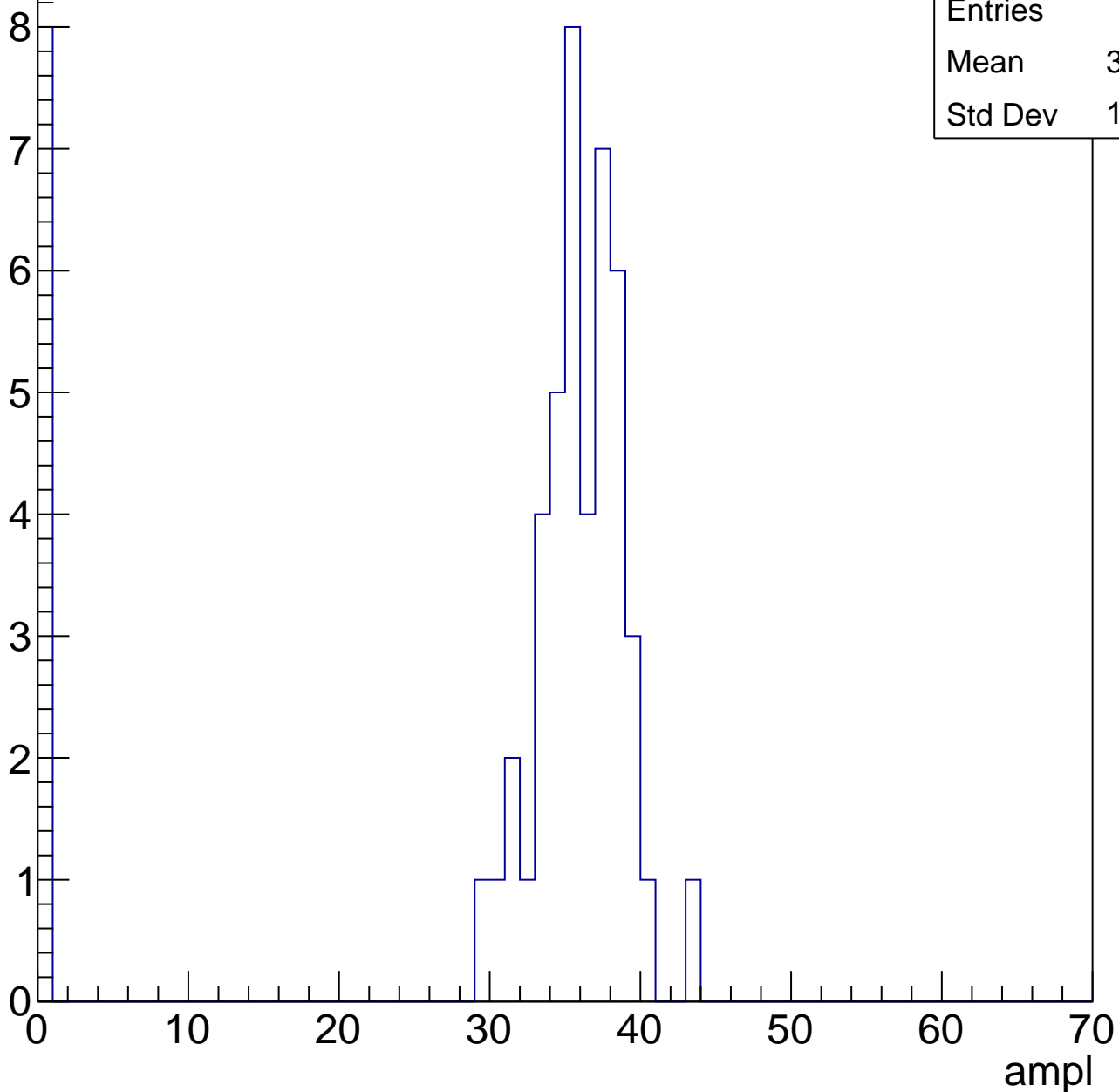


B1L103S, U12-ch36, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	52
Mean	30.12
Std Dev	13.09



B1L103S, U12-ch36, adc2

calib_packv5_041523_1651.root, FC#0, port C2

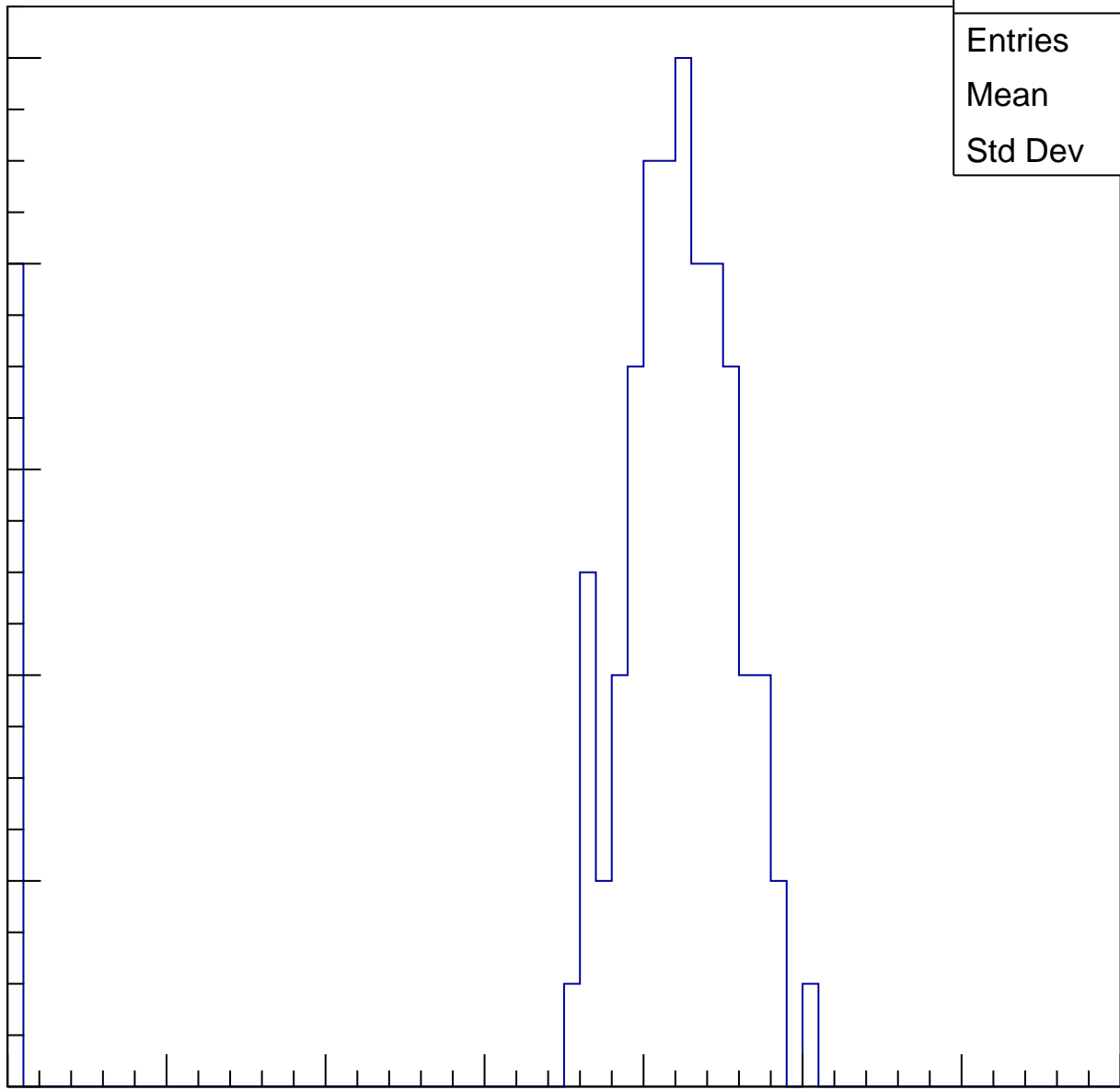
Entries	89
Mean	38.11
Std Dev	12.37

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

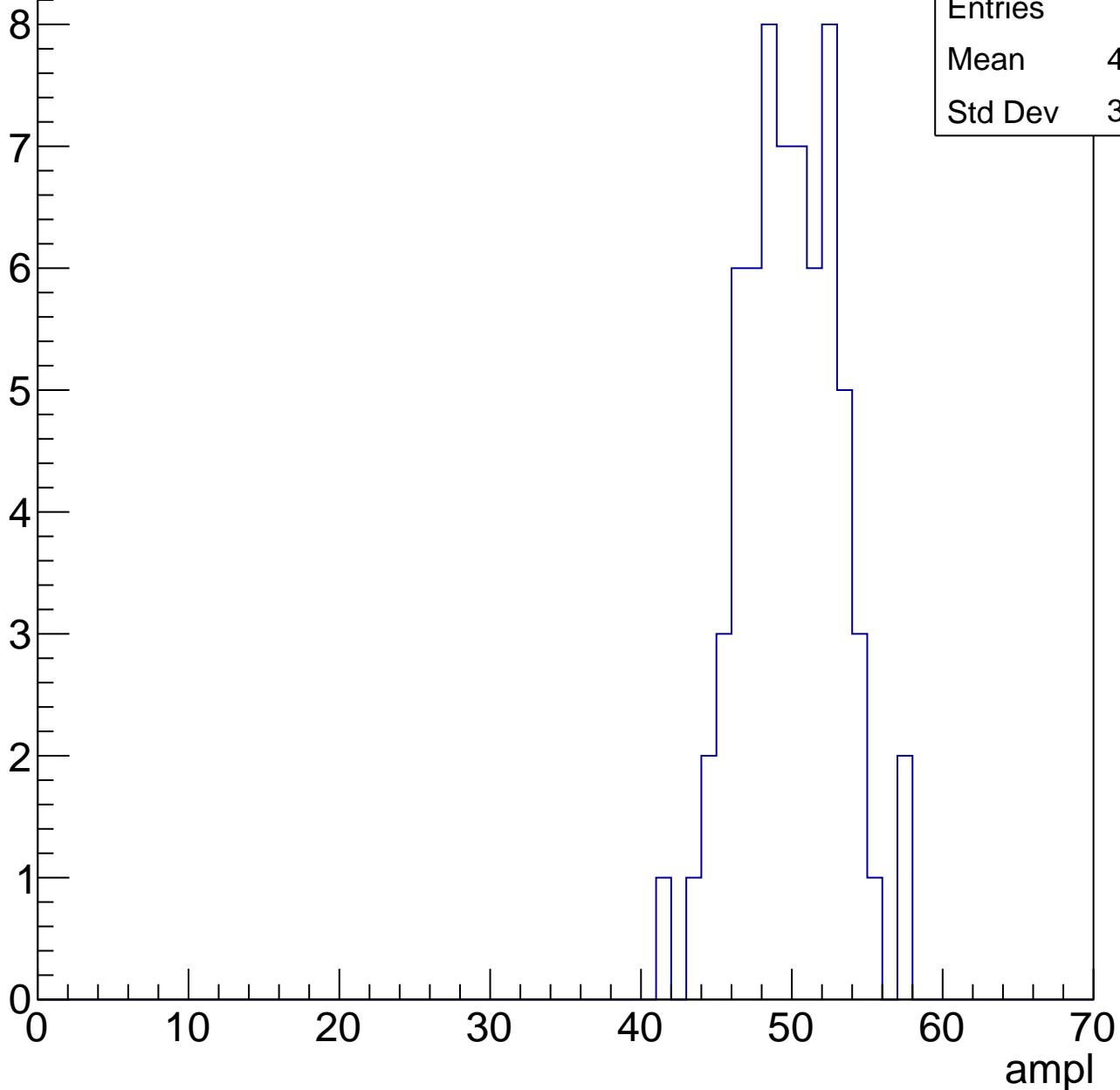


B1L103S, U12-ch36, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	49.39
Std Dev	3.247

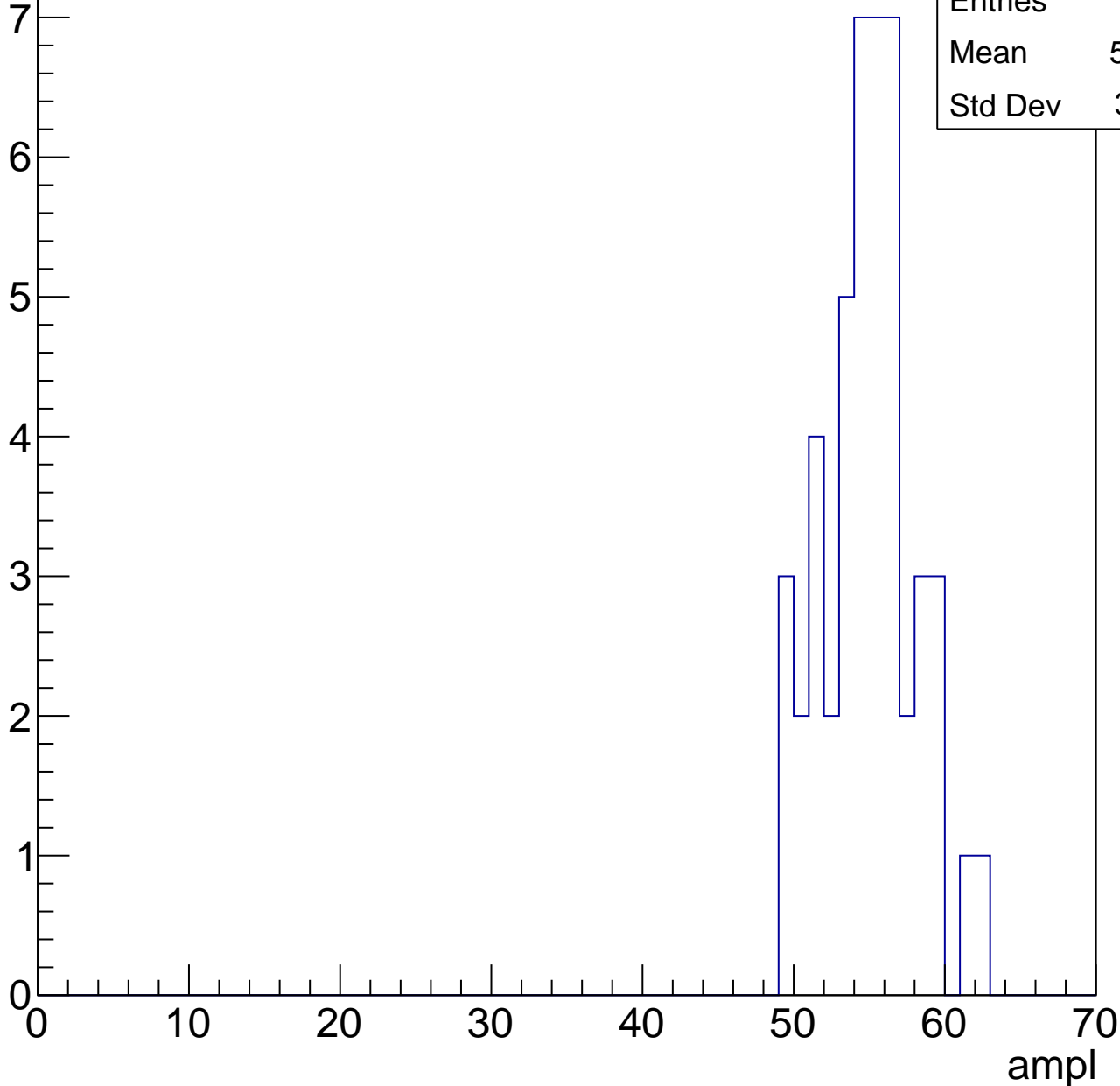


B1L103S, U12-ch36, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

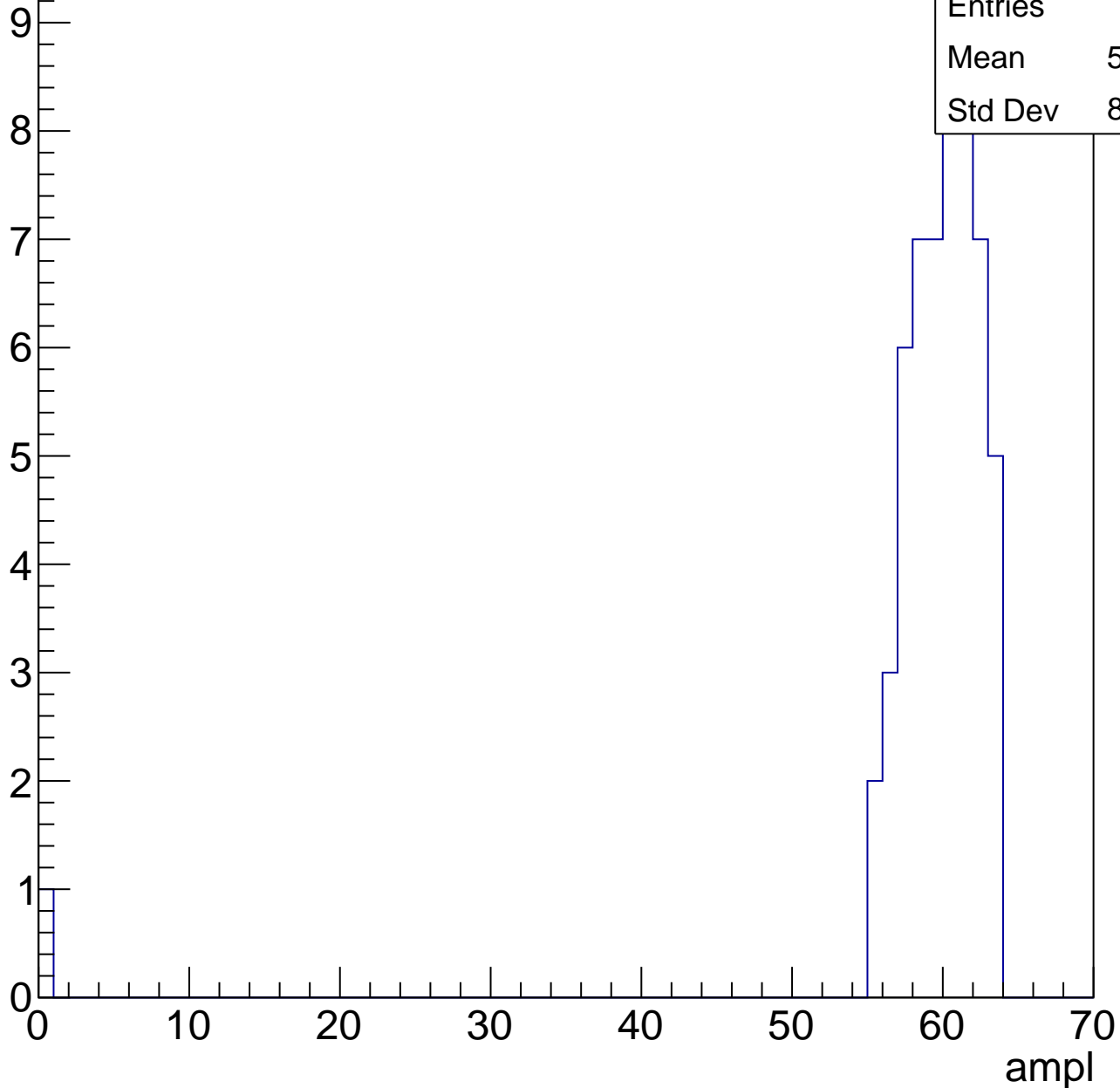
Entries	47
Mean	54.53
Std Dev	3.031



B1L103S, U12-ch36, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

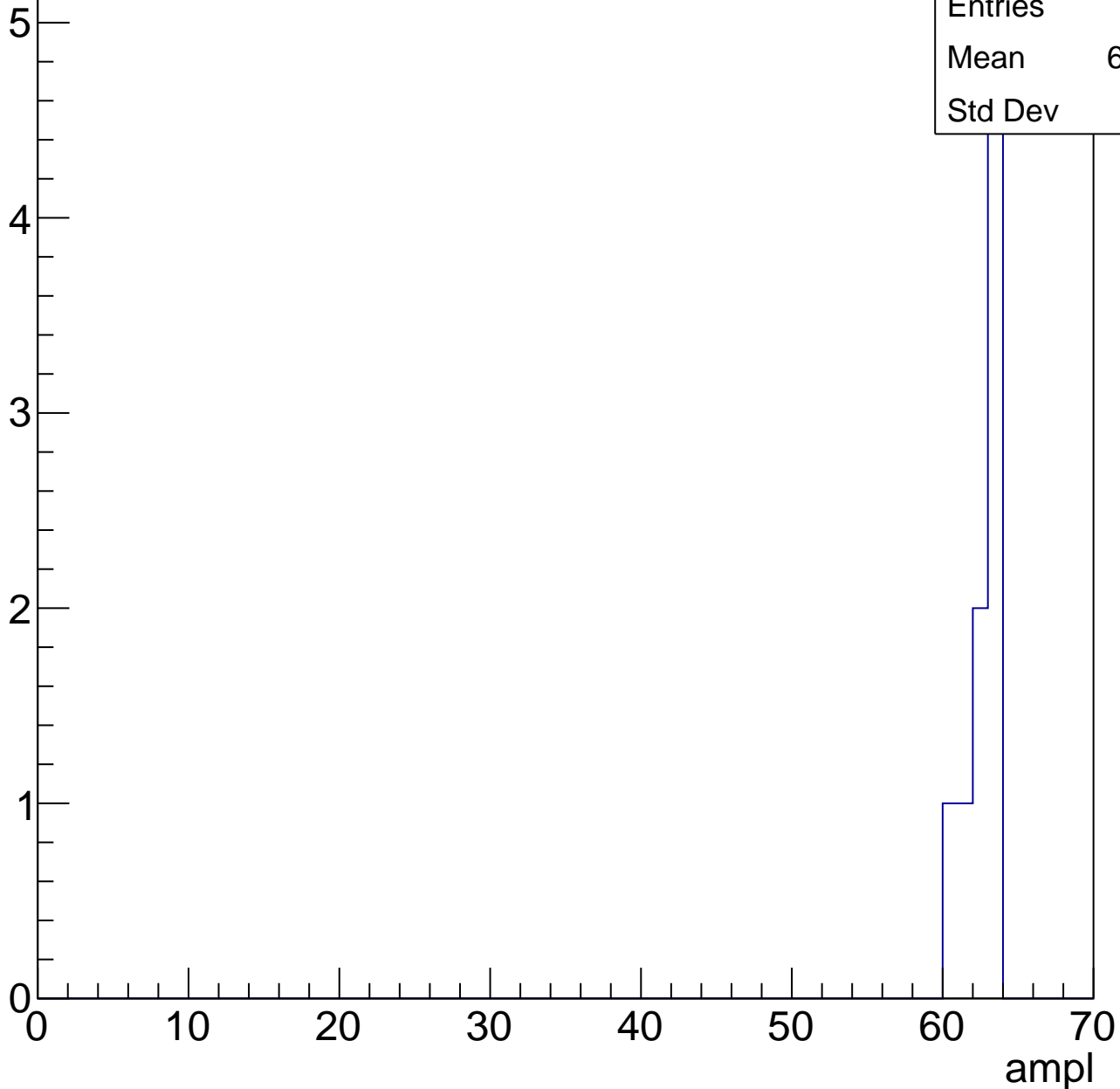


B1L103S, U12-ch36, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	9
Mean	62.22
Std Dev	1.03



B1L103S, U12-ch36, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

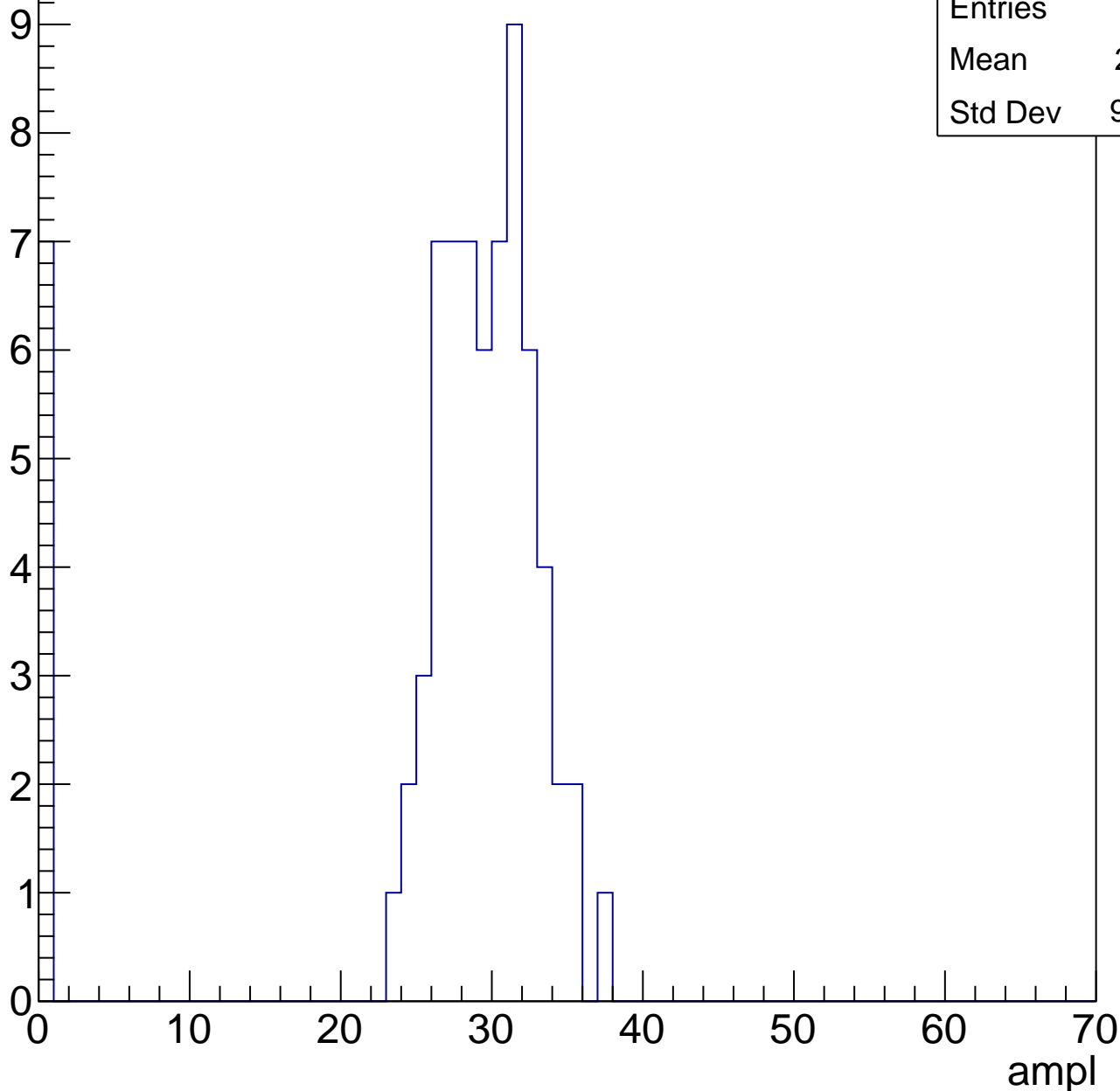
Entries	19
Mean	0
Std Dev	0

B1L103S, U12-ch37, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	26.41
Std Dev	9.184



B1L103S, U12-ch37, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	83
Mean	31.46
Std Dev	12.63

Entry

10

8

6

4

2

0

0

10

20

30

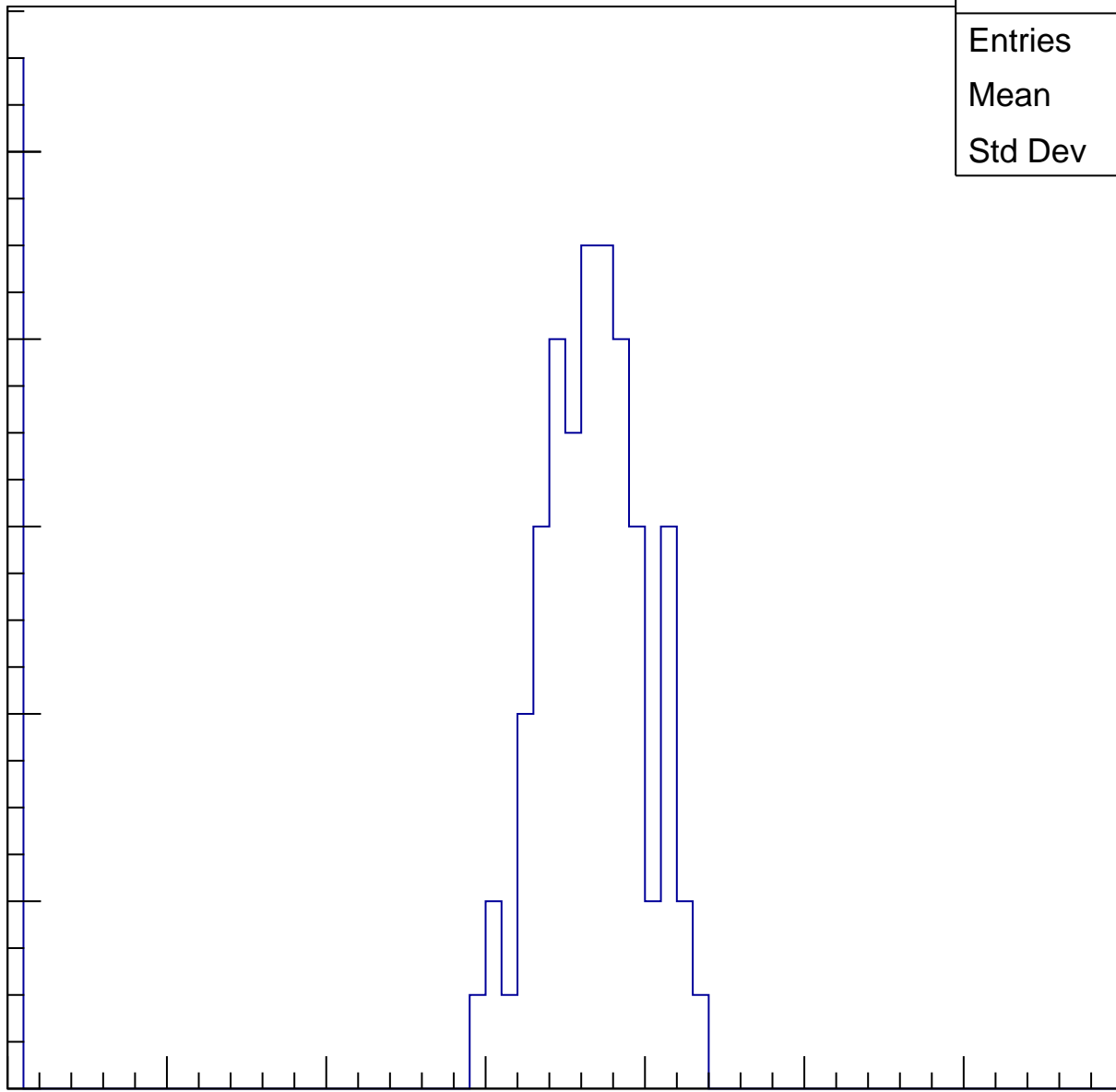
40

50

60

70

ampl

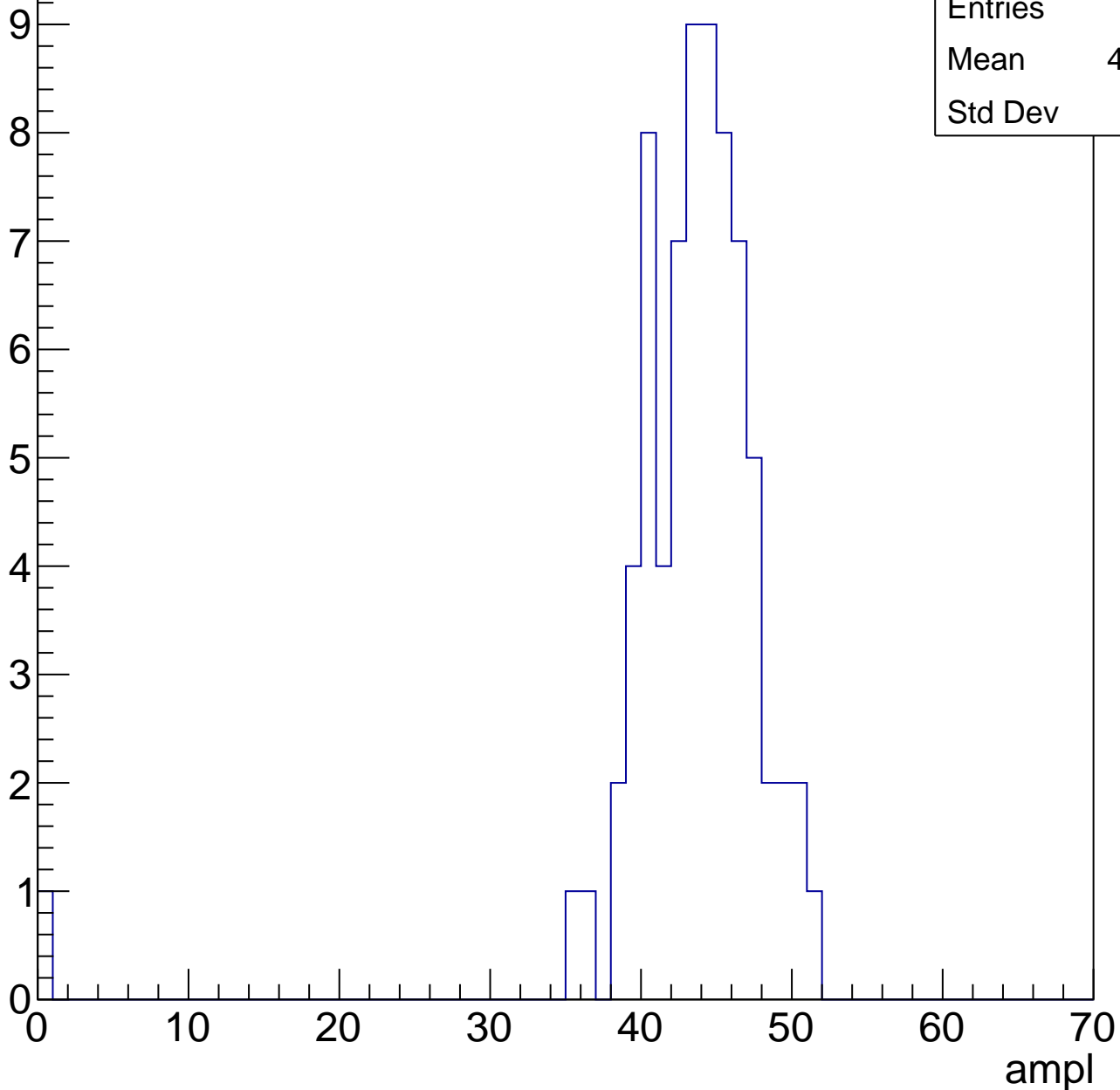


B1L103S, U12-ch37, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	73
Mean	42.82
Std Dev	6.01

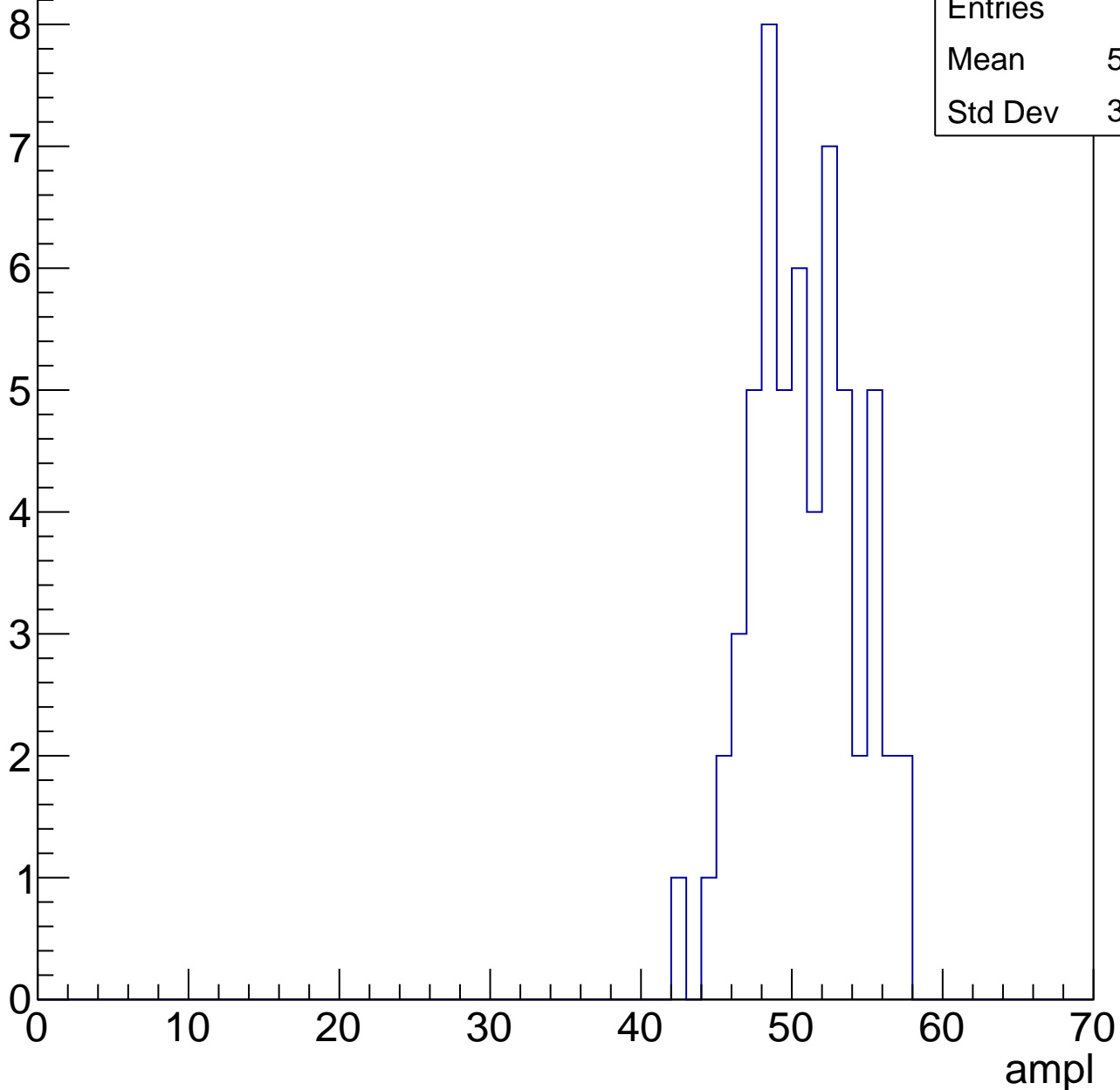


B1L103S, U12-ch37, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	50.34
Std Dev	3.417

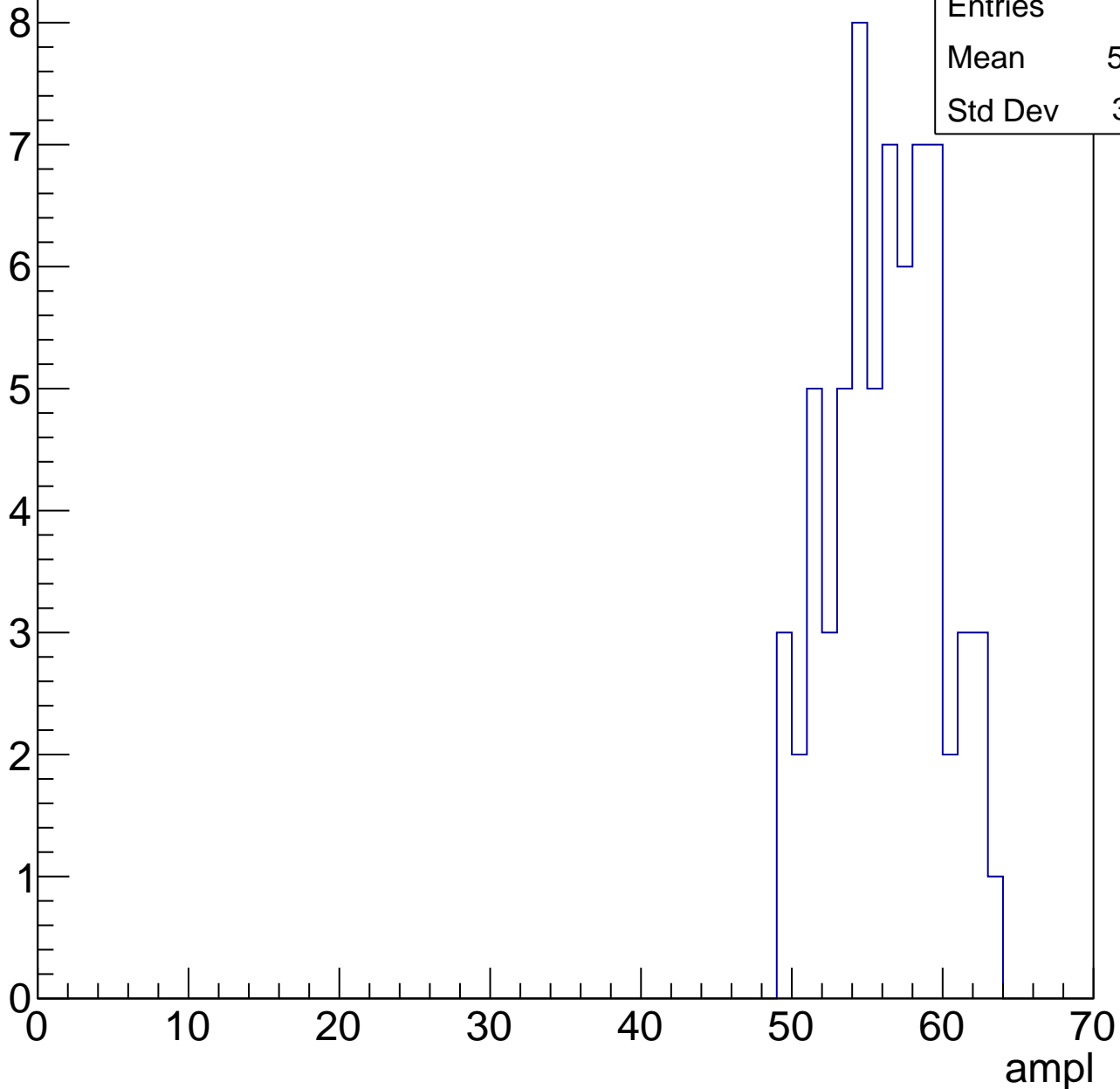


B1L103S, U12-ch37, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	55.75
Std Dev	3.521

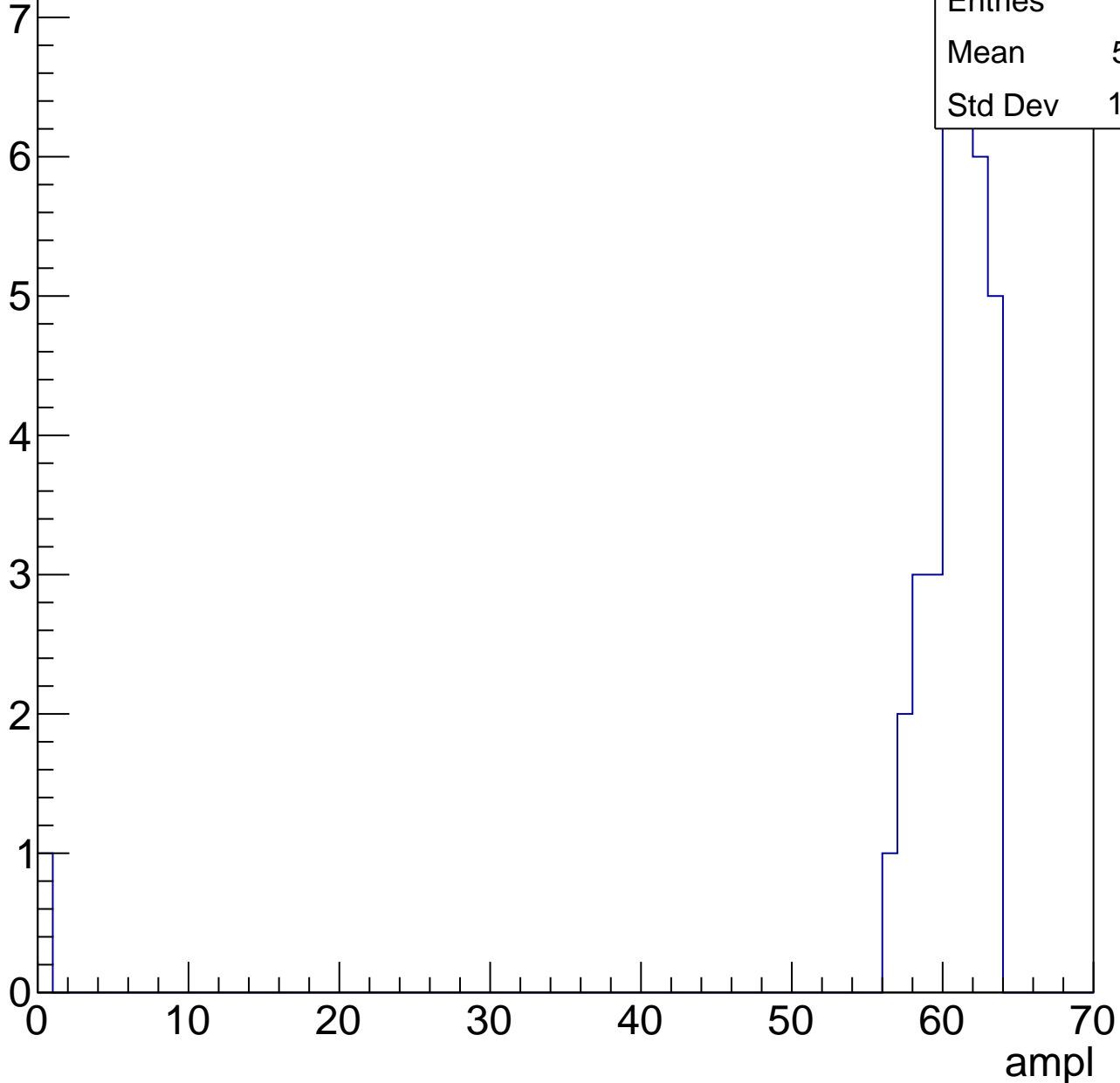


B1L103S, U12-ch37, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

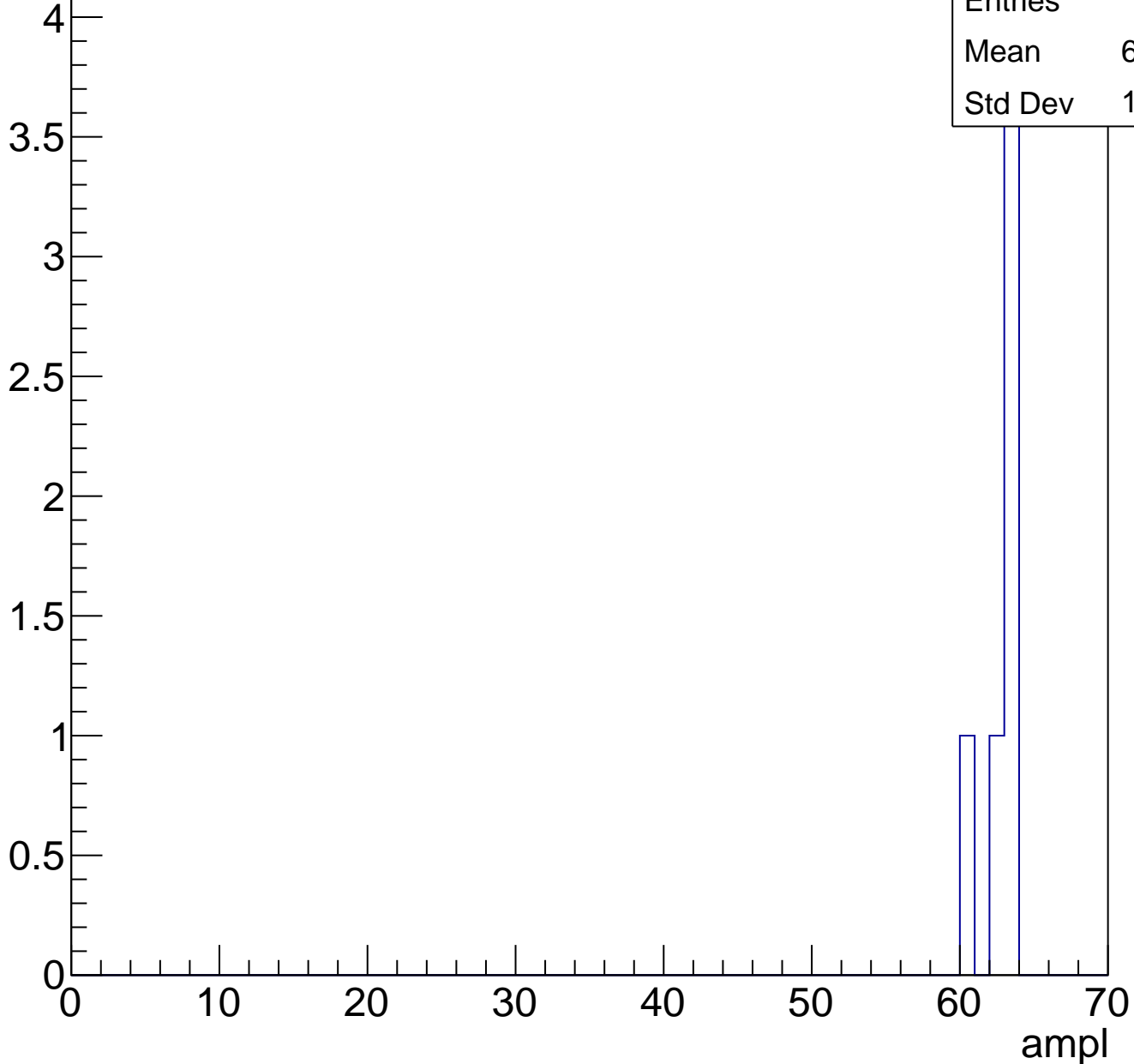
Entries	35
Mean	58.71
Std Dev	10.24



B1L103S, U12-ch37, adc6

calib_packv5_041523_1651.root, FC#0, port C2

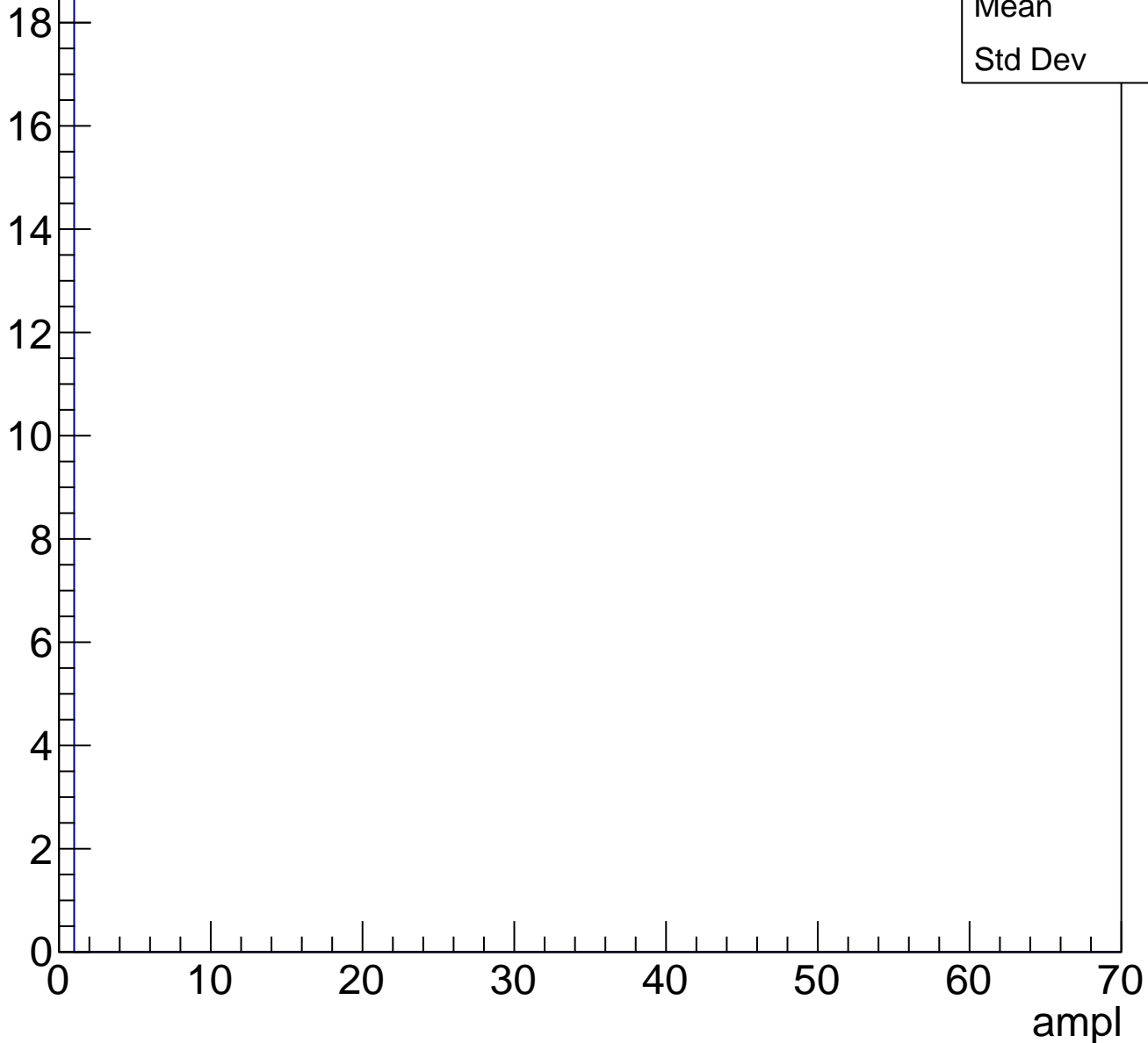
Entry



B1L103S, U12-ch37, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch38, adc0

calib_packv5_041523_1651.root, FC#0, port C2

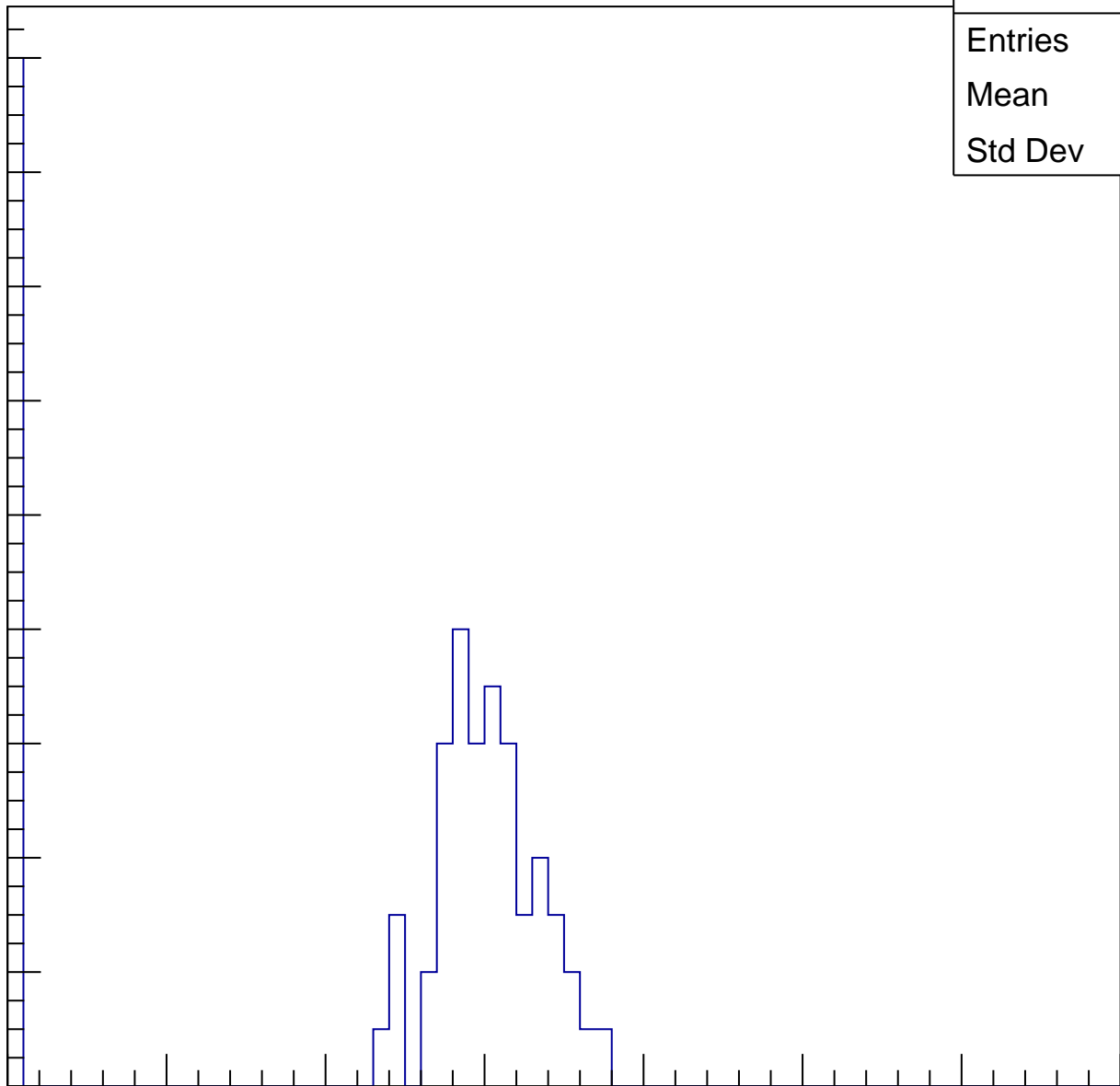
Entry

18
16
14
12
10
8
6
4
2
0

Entries	71
Mean	22.2
Std Dev	13.21

ampl

0 10 20 30 40 50 60 70



B1L103S, U12-ch38, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	82
Mean	31.13
Std Dev	12.68

Entry

10

8

6

4

2

0

0

10

20

30

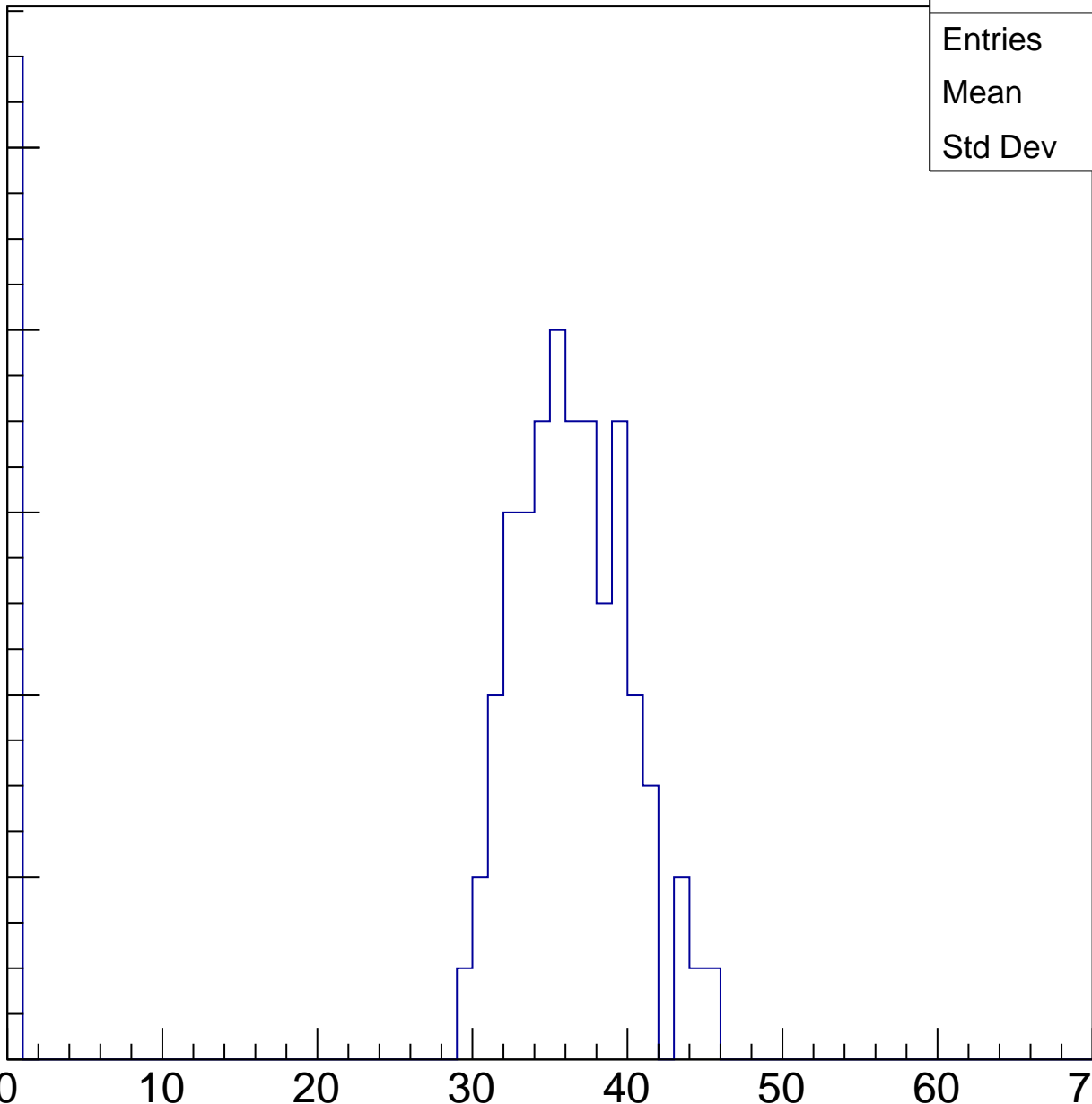
40

50

60

70

ampl

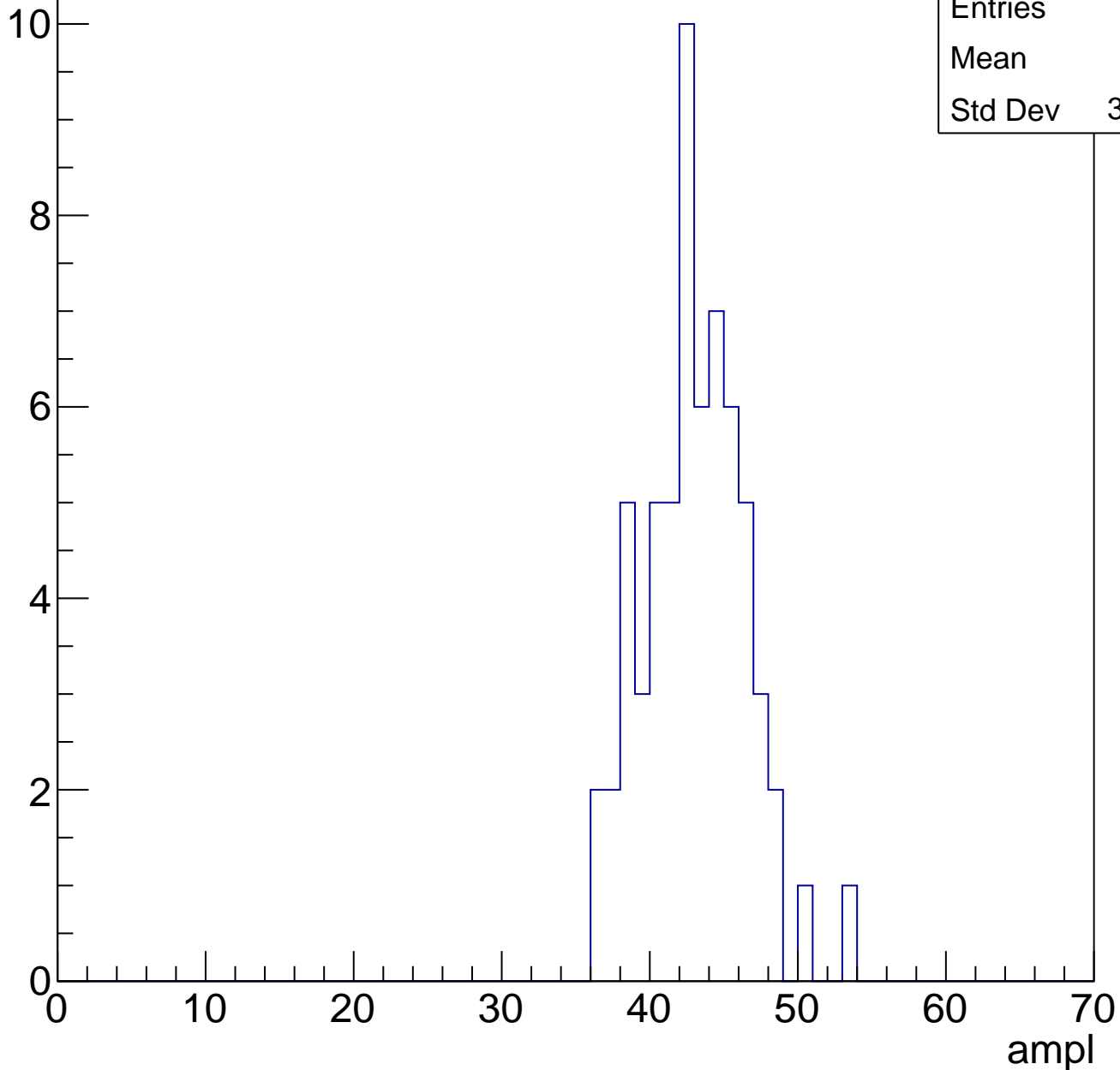


B1L103S, U12-ch38, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	63
Mean	42.6
Std Dev	3.407

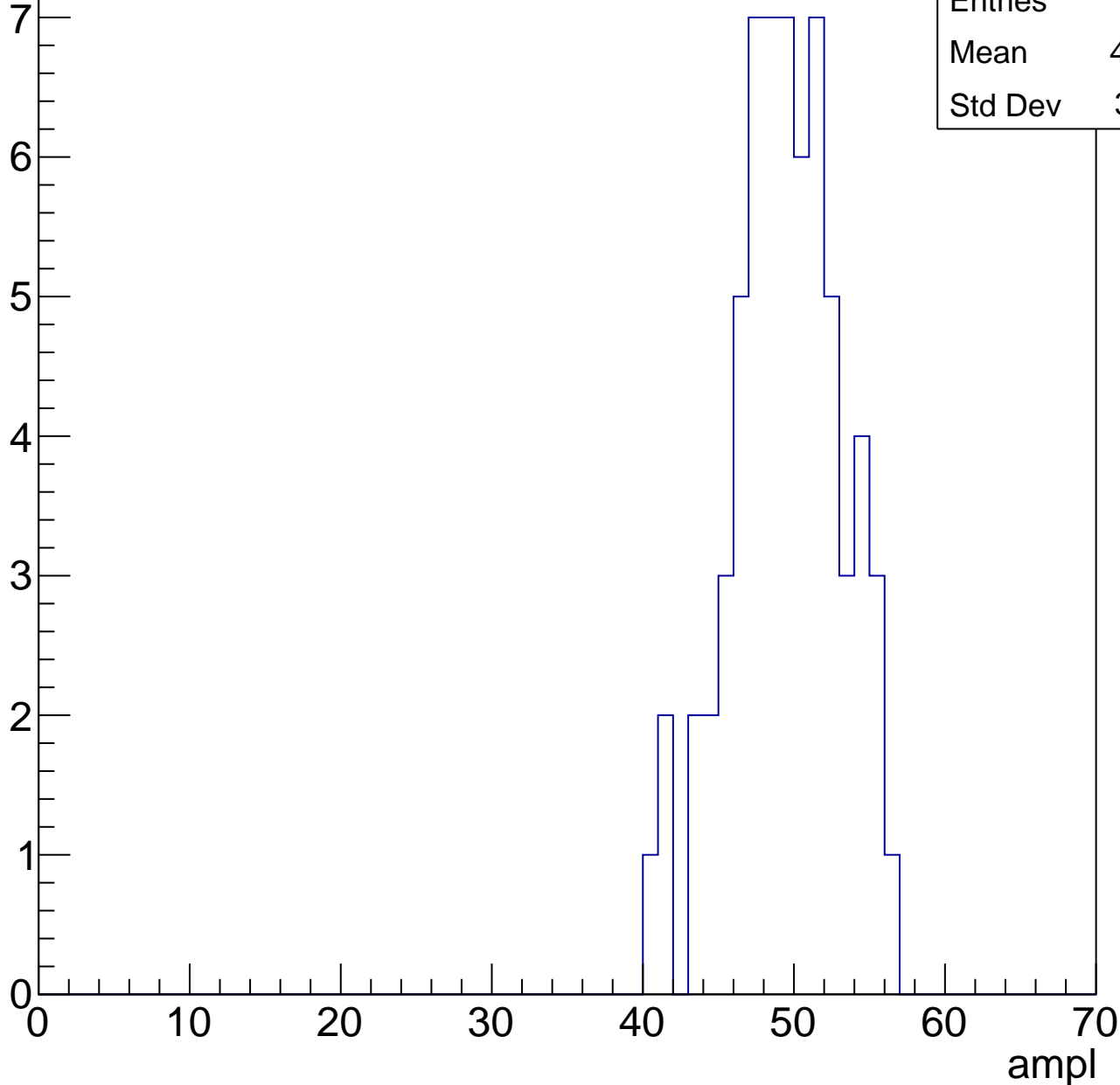
Entry



B1L103S, U12-ch38, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry



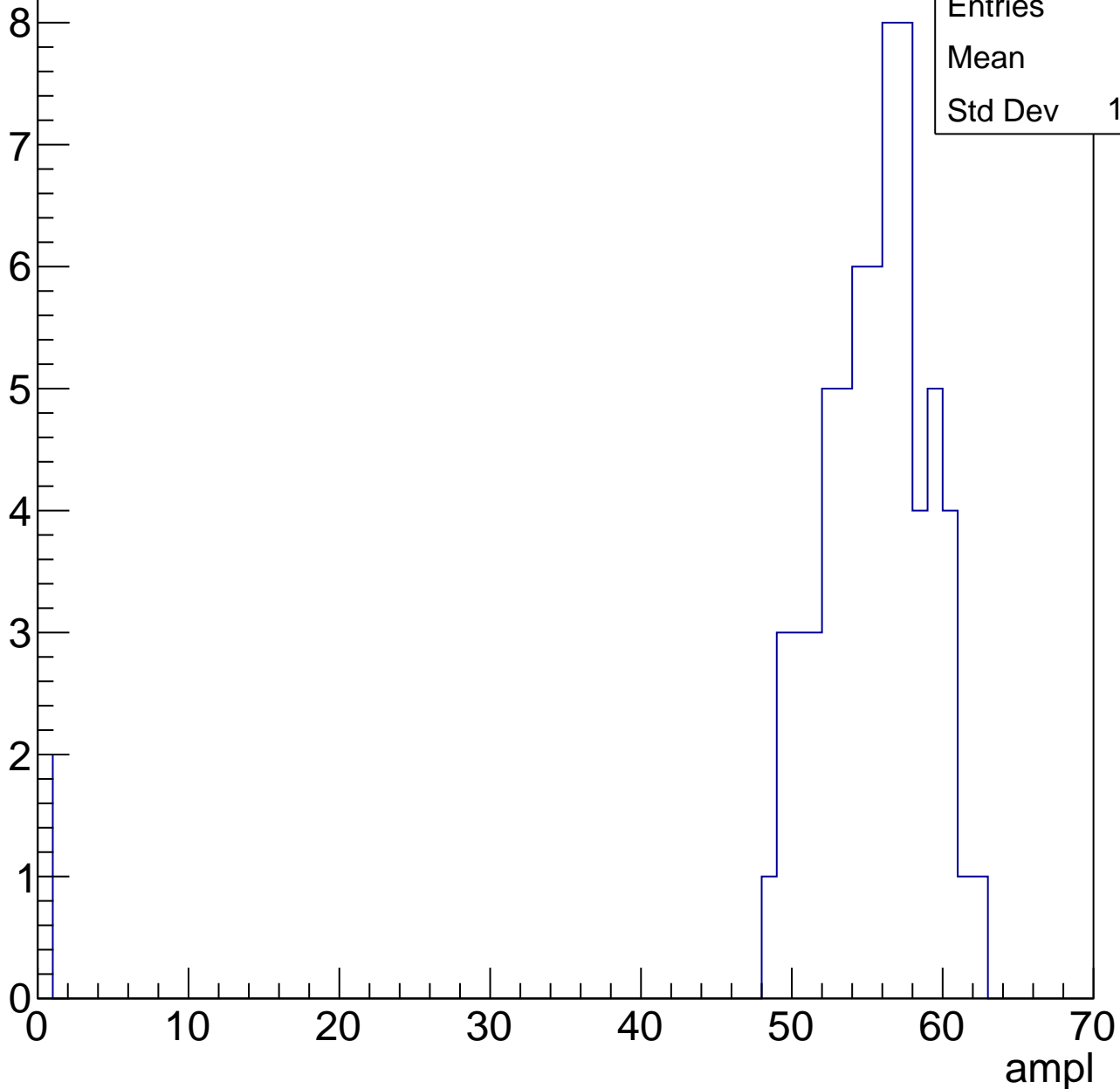
Entries	65
Mean	48.95
Std Dev	3.601

B1L103S, U12-ch38, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	53.4
Std Dev	10.06

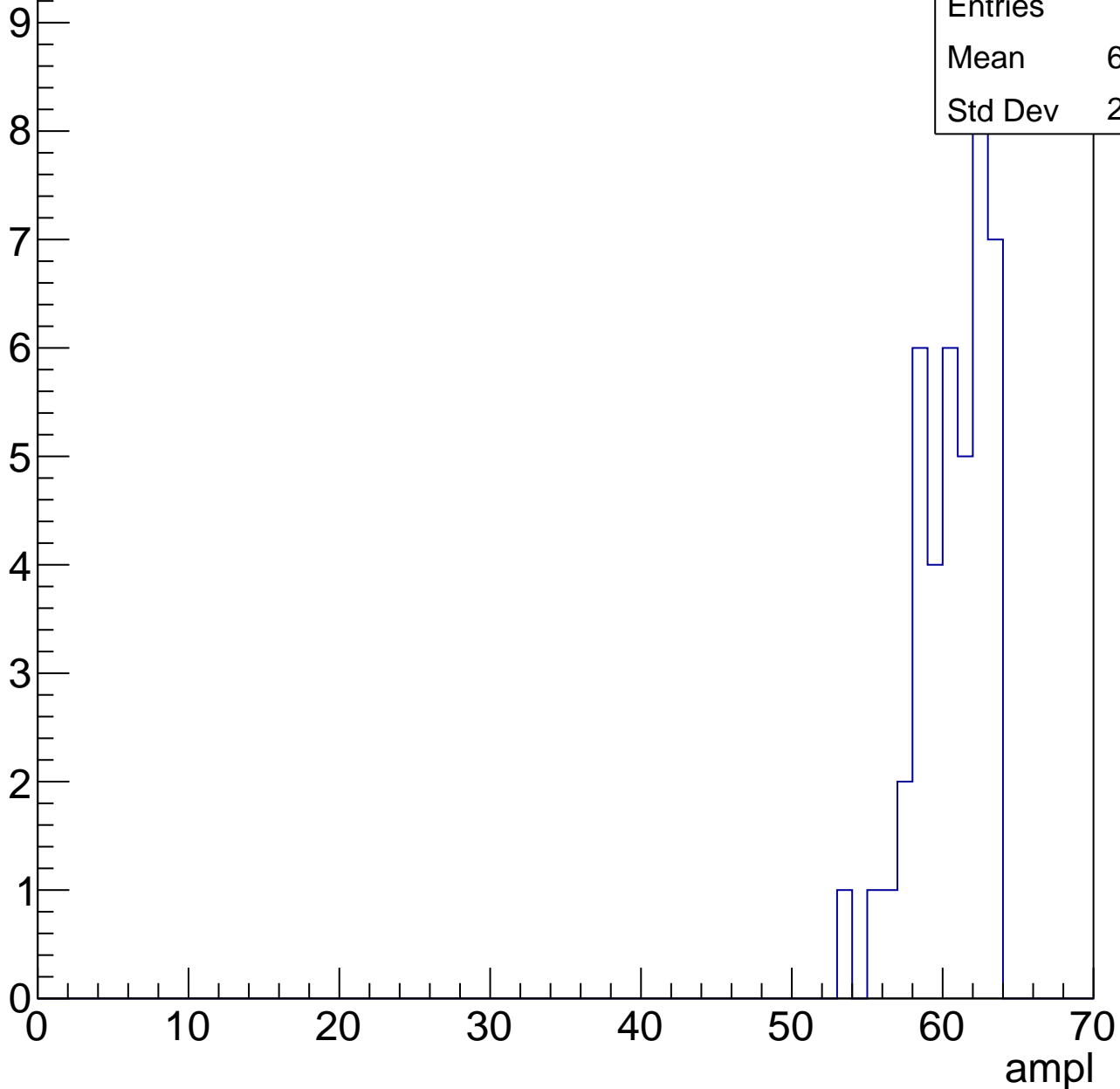


B1L103S, U12-ch38, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

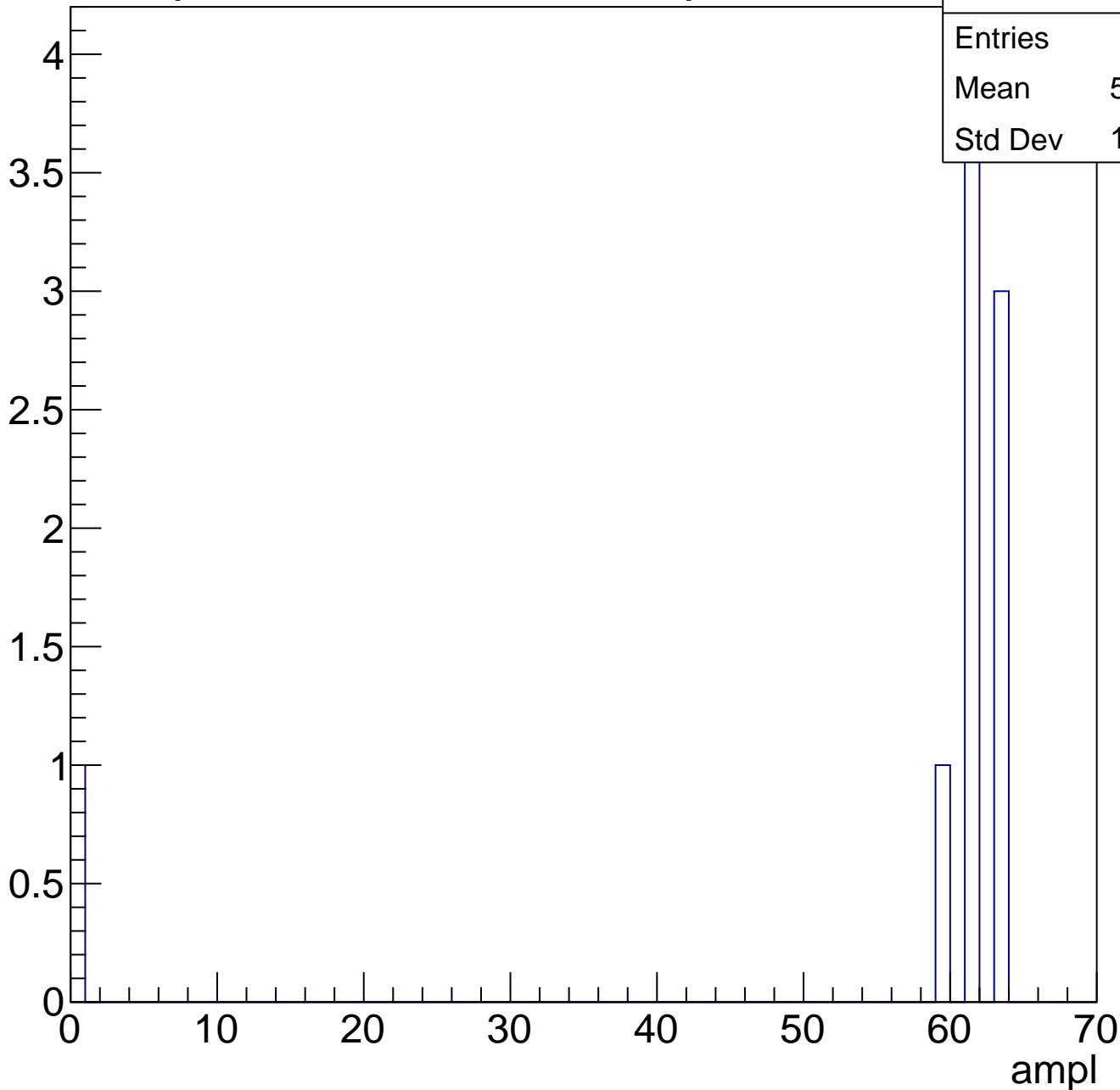
Entries	42
Mean	60.14
Std Dev	2.386



B1L103S, U12-ch38, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch38, adc7

calib_packv5_041523_1651.root, FC#0, port C2

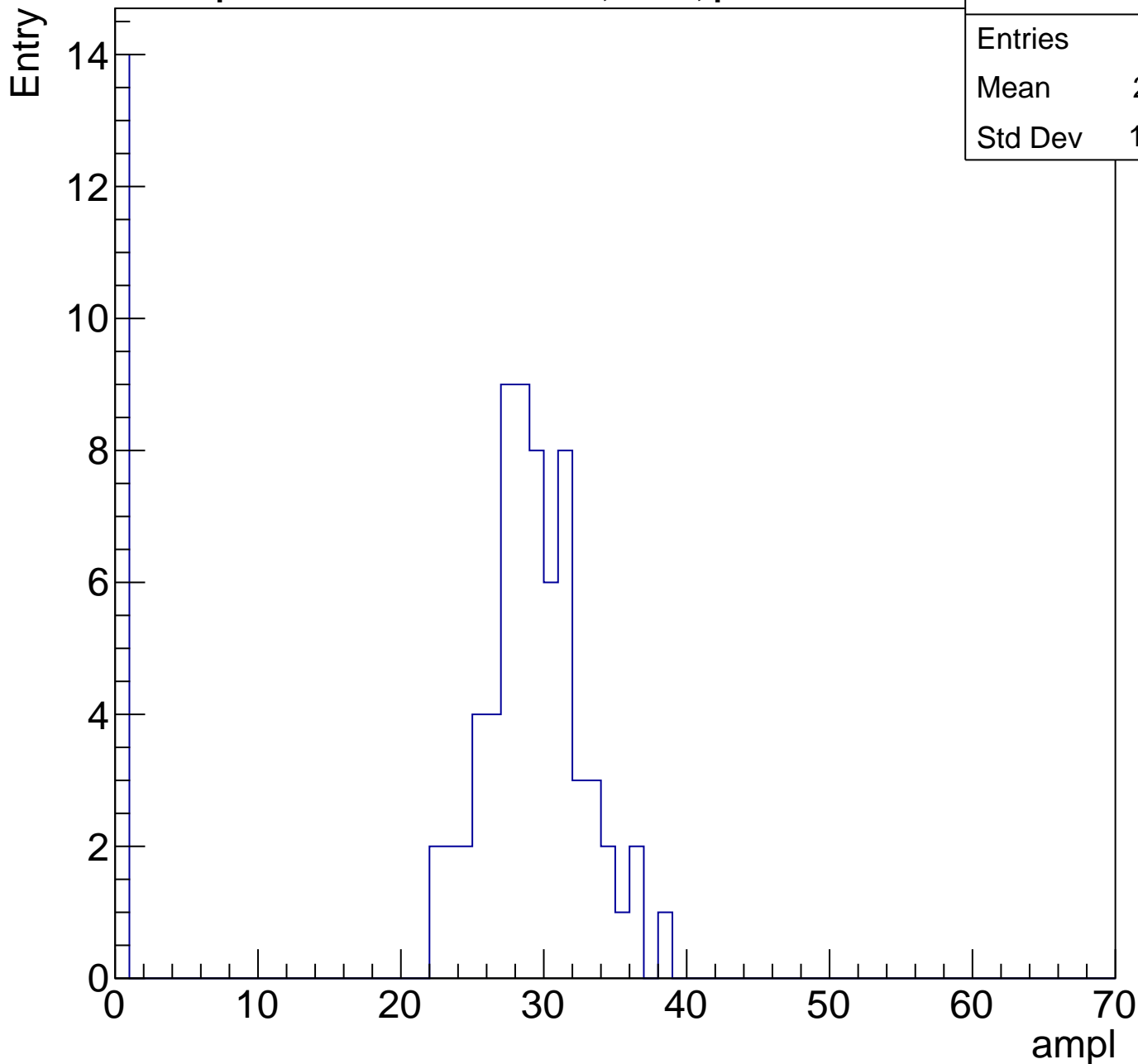
Entry



B1L103S, U12-ch39, adc0

calib_packv5_041523_1651.root, FC#0, port C2

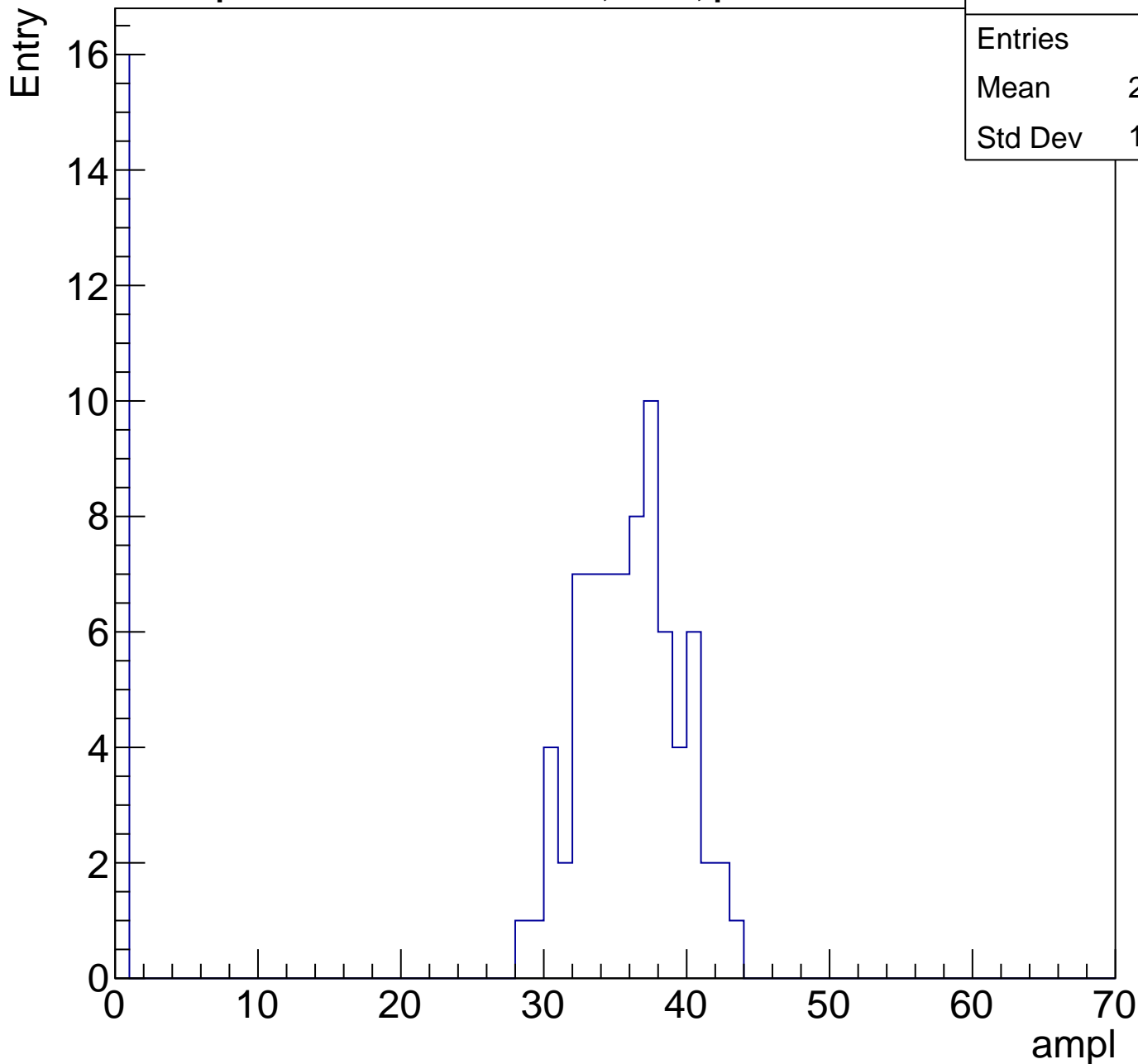
Entries	80
Mean	23.81
Std Dev	11.38



B1L103S, U12-ch39, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	91
Mean	29.32
Std Dev	13.88

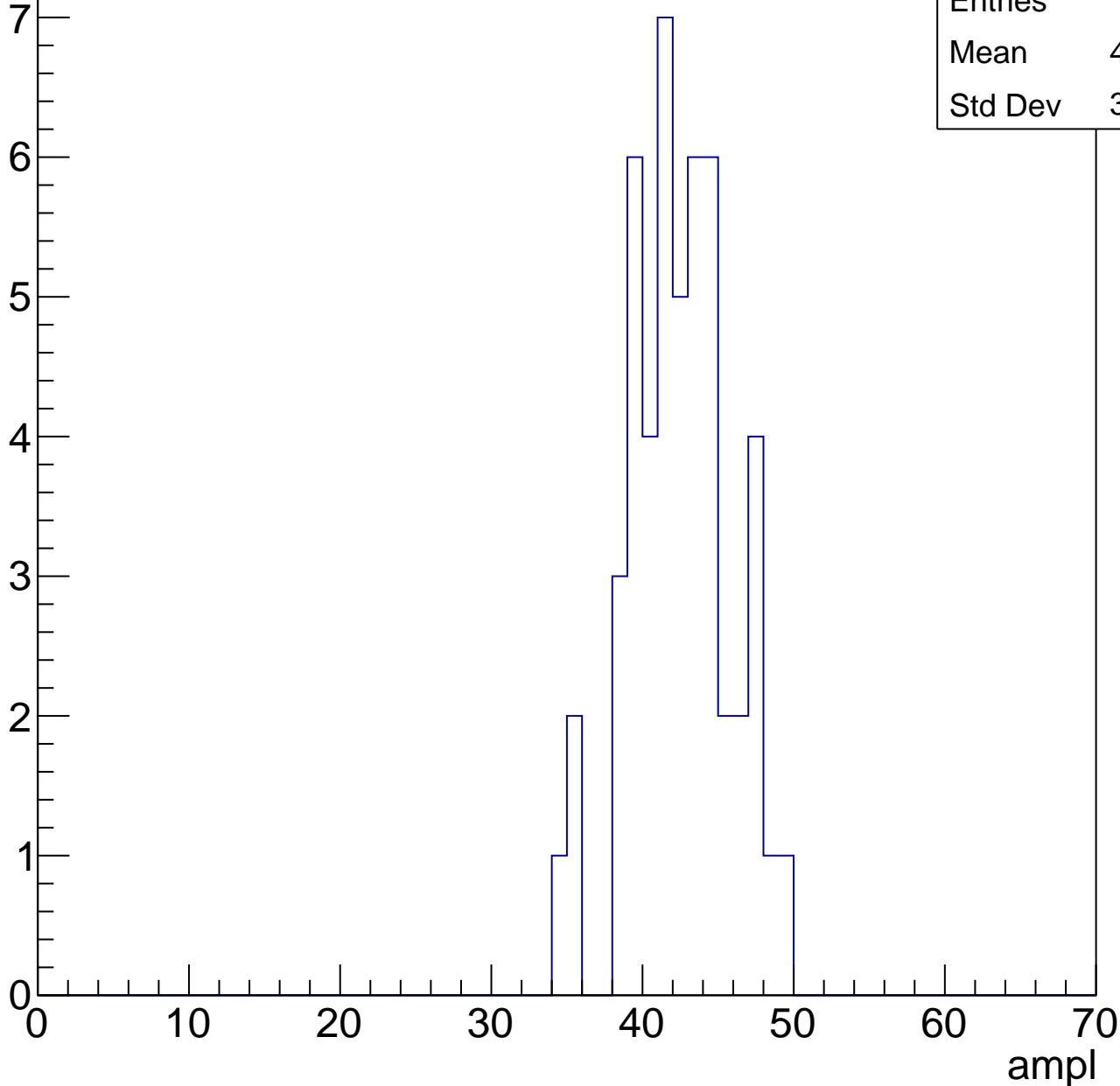


B1L103S, U12-ch39, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	50
Mean	41.96
Std Dev	3.322

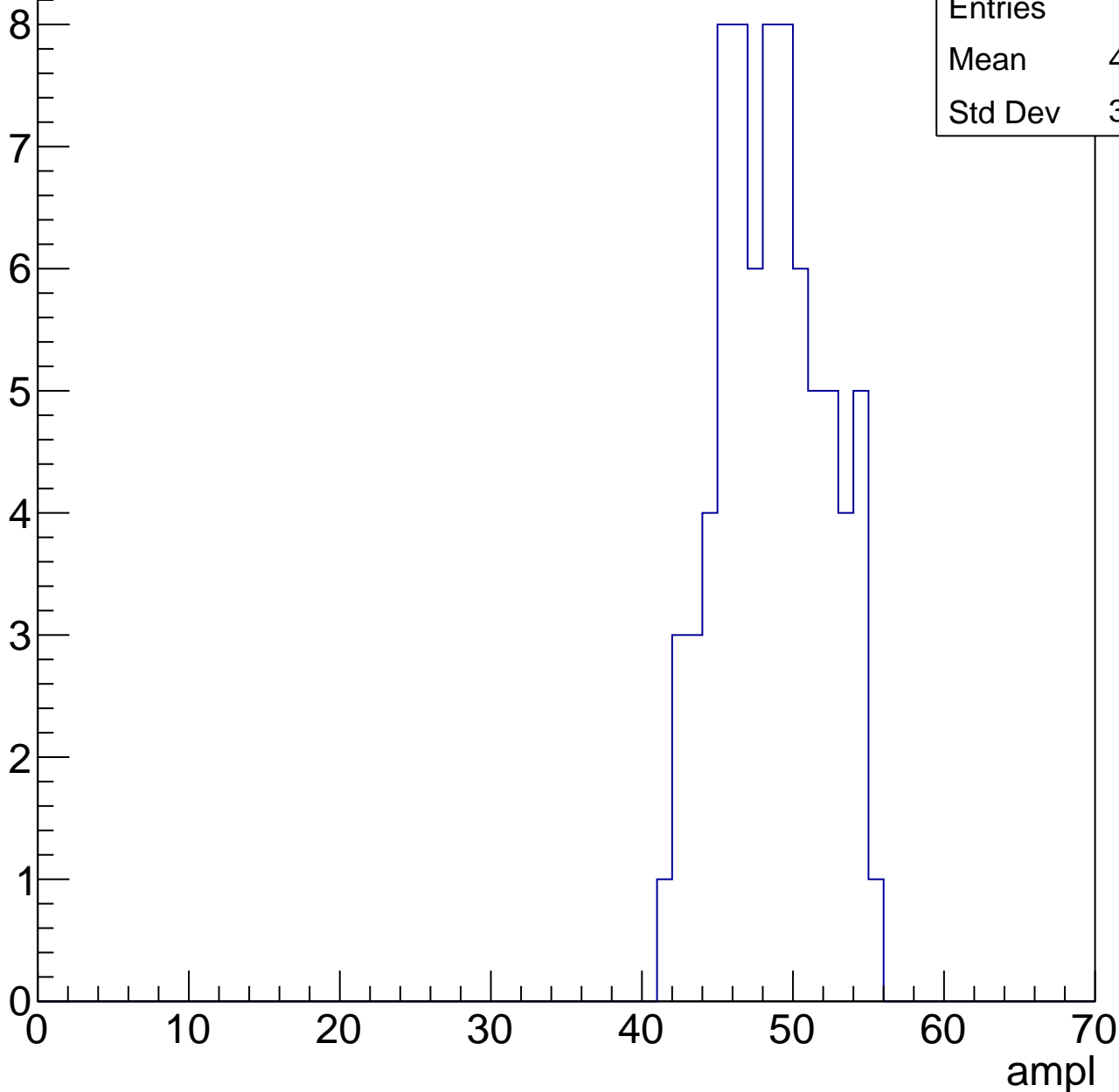


B1L103S, U12-ch39, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	75
Mean	48.13
Std Dev	3.446

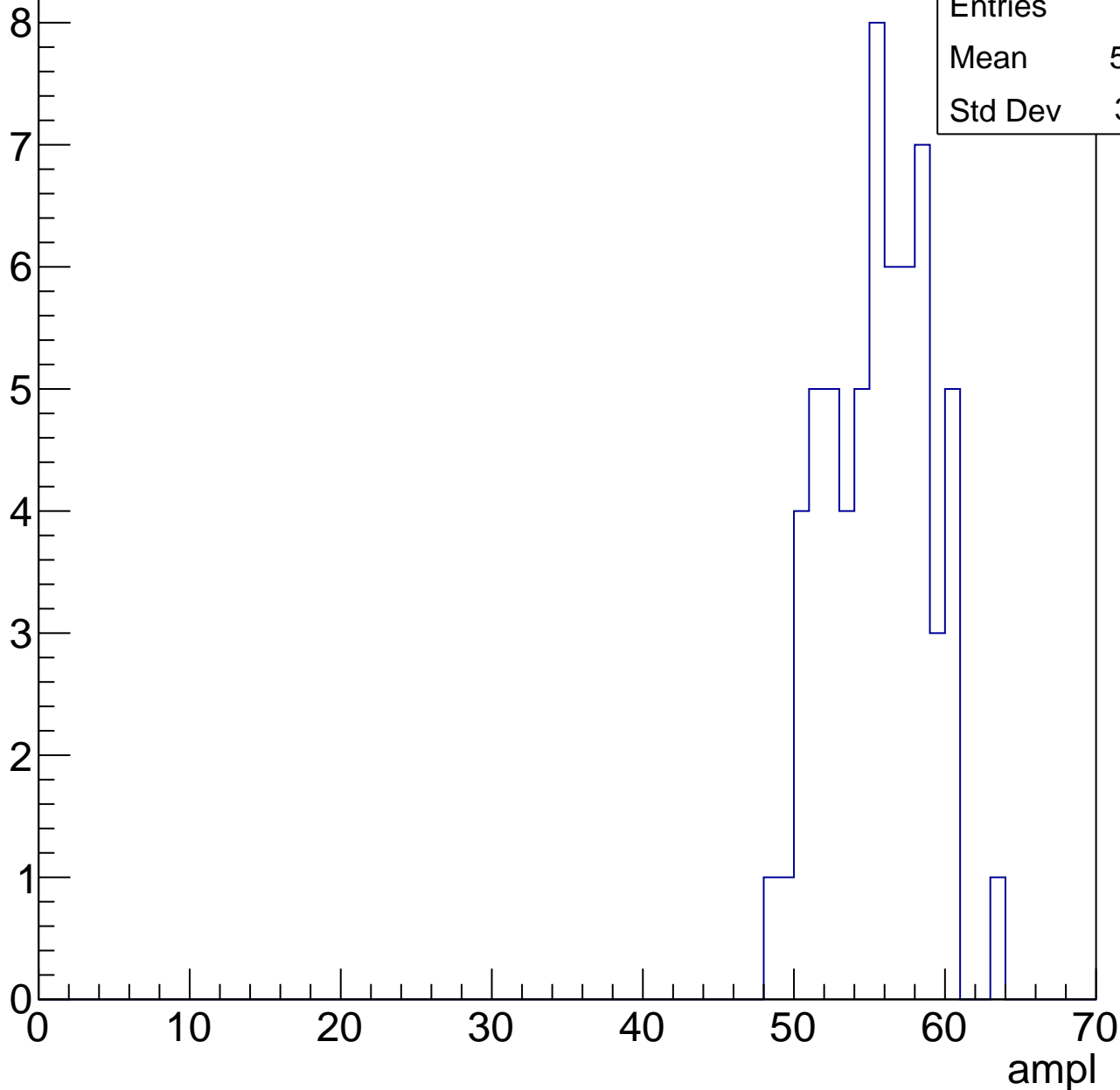


B1L103S, U12-ch39, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	55.05
Std Dev	3.291

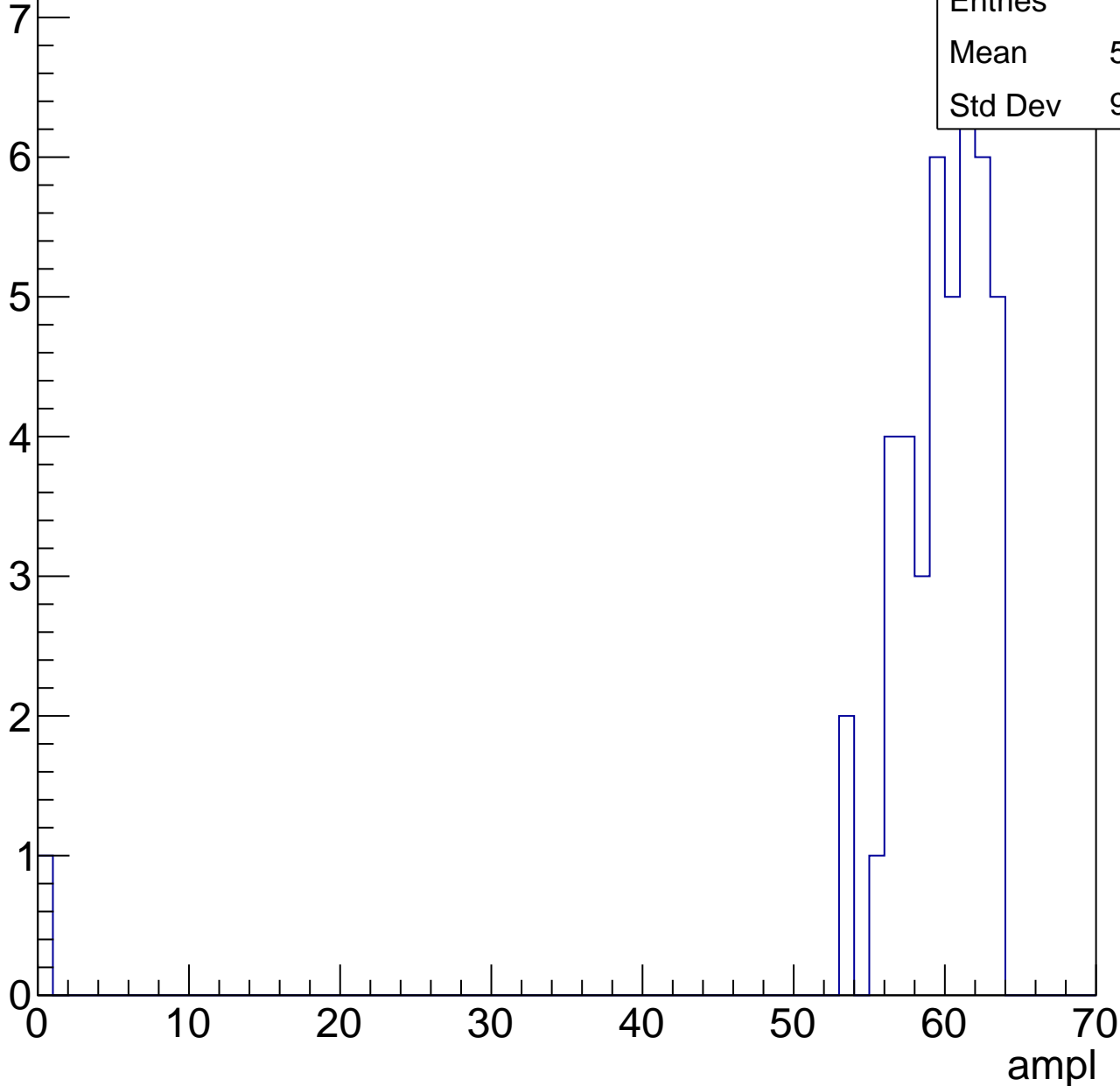


B1L103S, U12-ch39, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

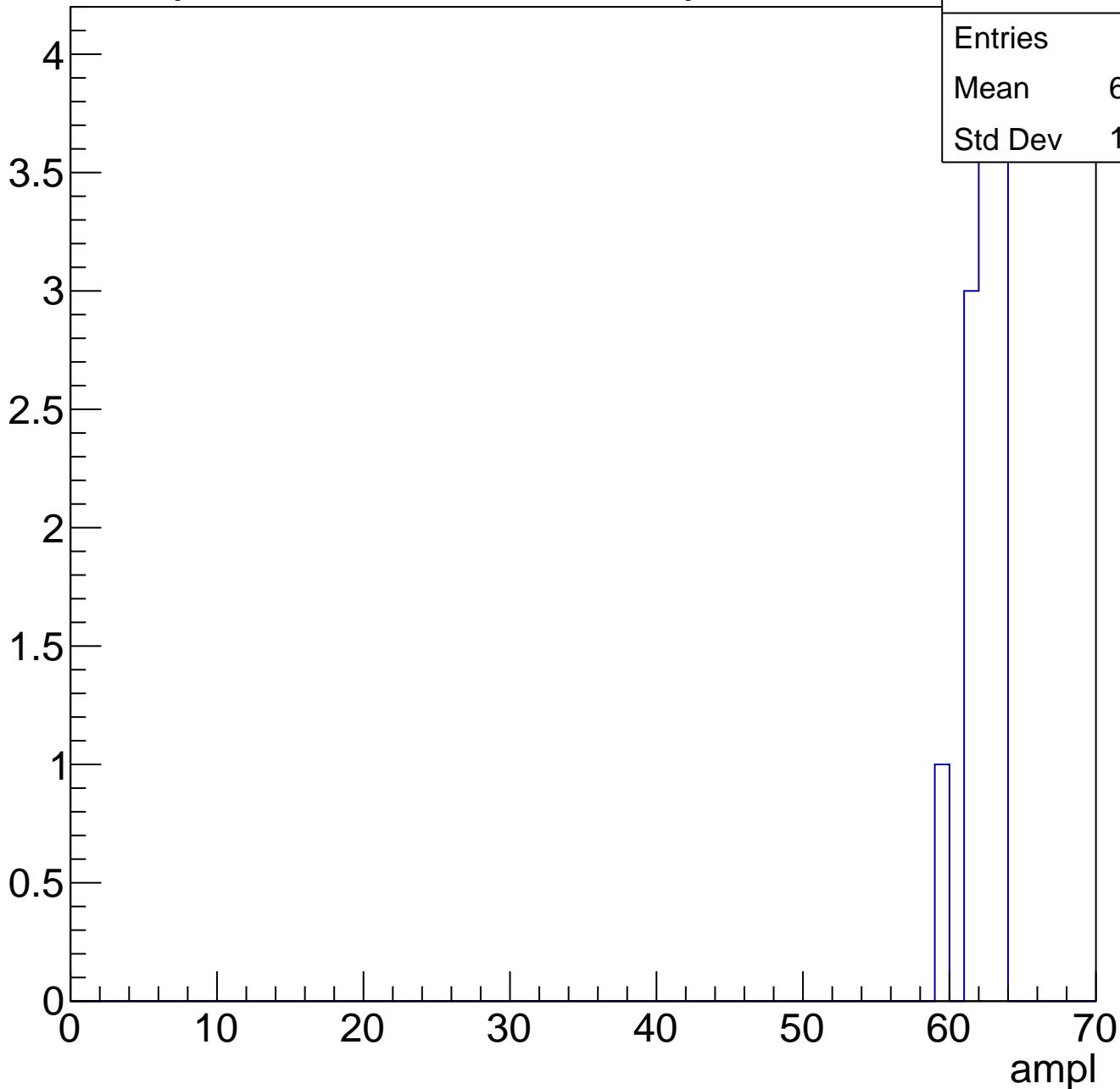
Entries	44
Mean	58.07
Std Dev	9.235



B1L103S, U12-ch39, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

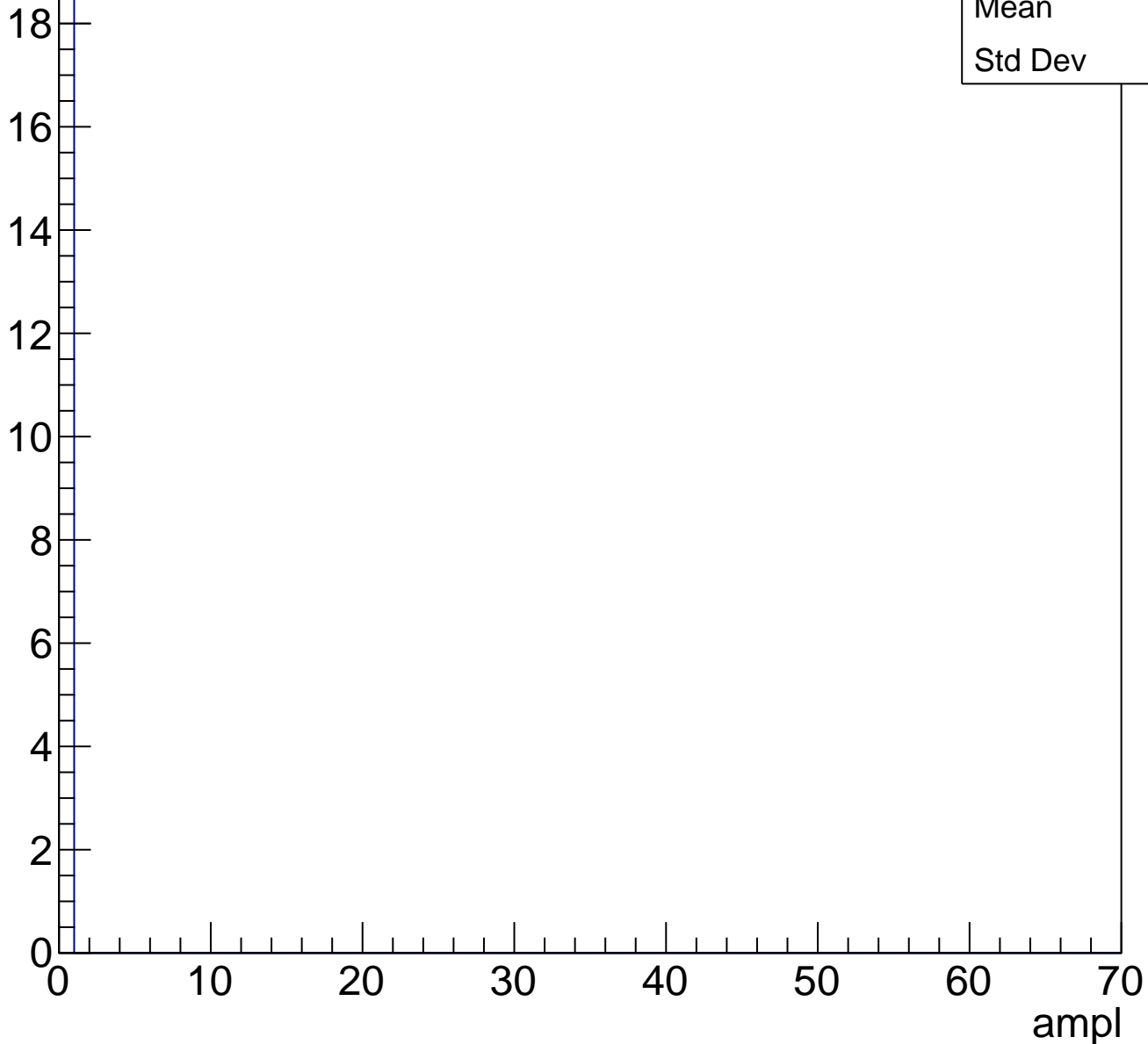


B1L103S, U12-ch39, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	0
Std Dev	0

Entry



B1L103S, U12-ch40, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	94
Mean	25.17
Std Dev	10.09

Entry

10

8

6

4

2

0

0

10

20

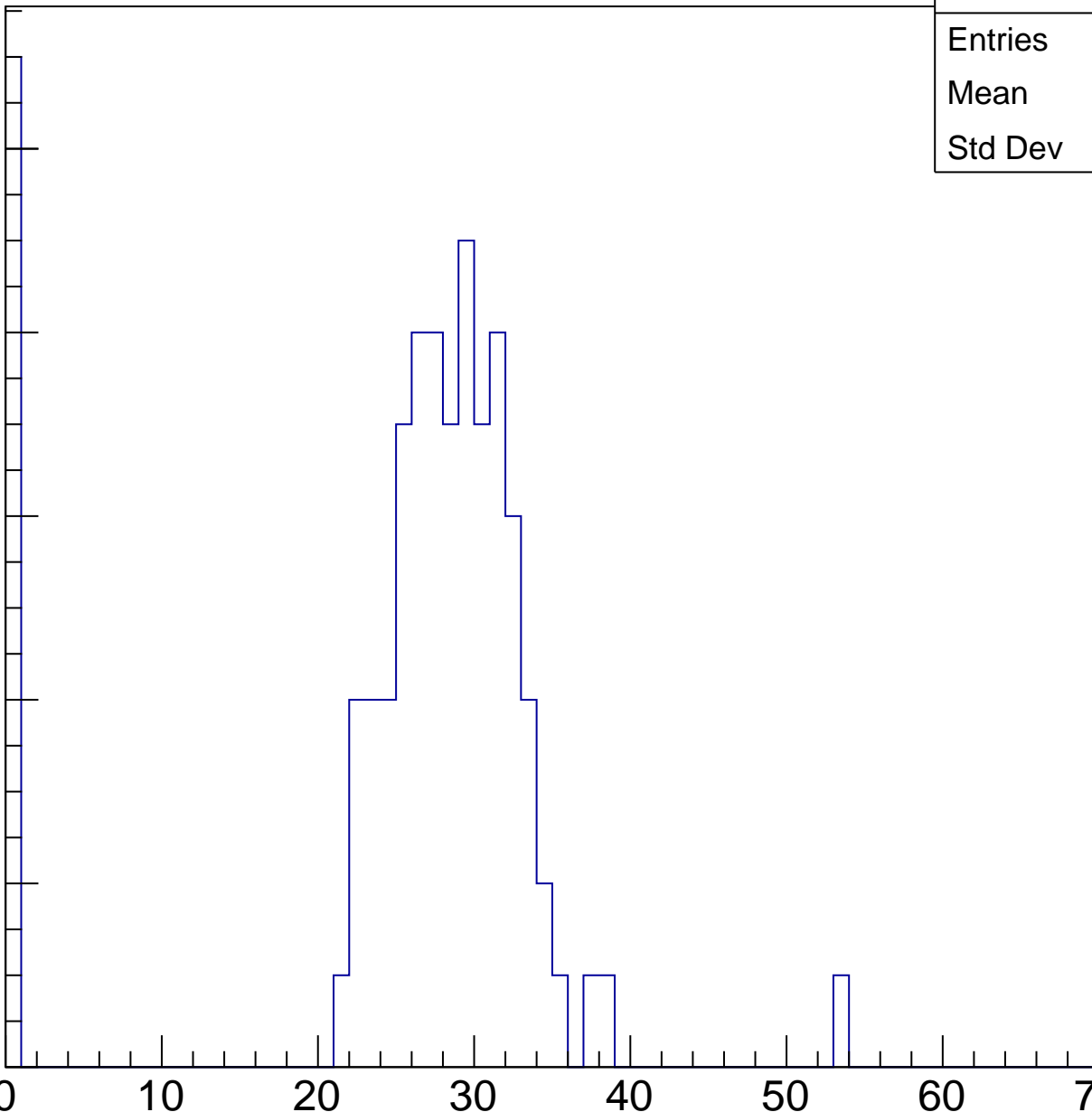
30

40

50

60

ampl

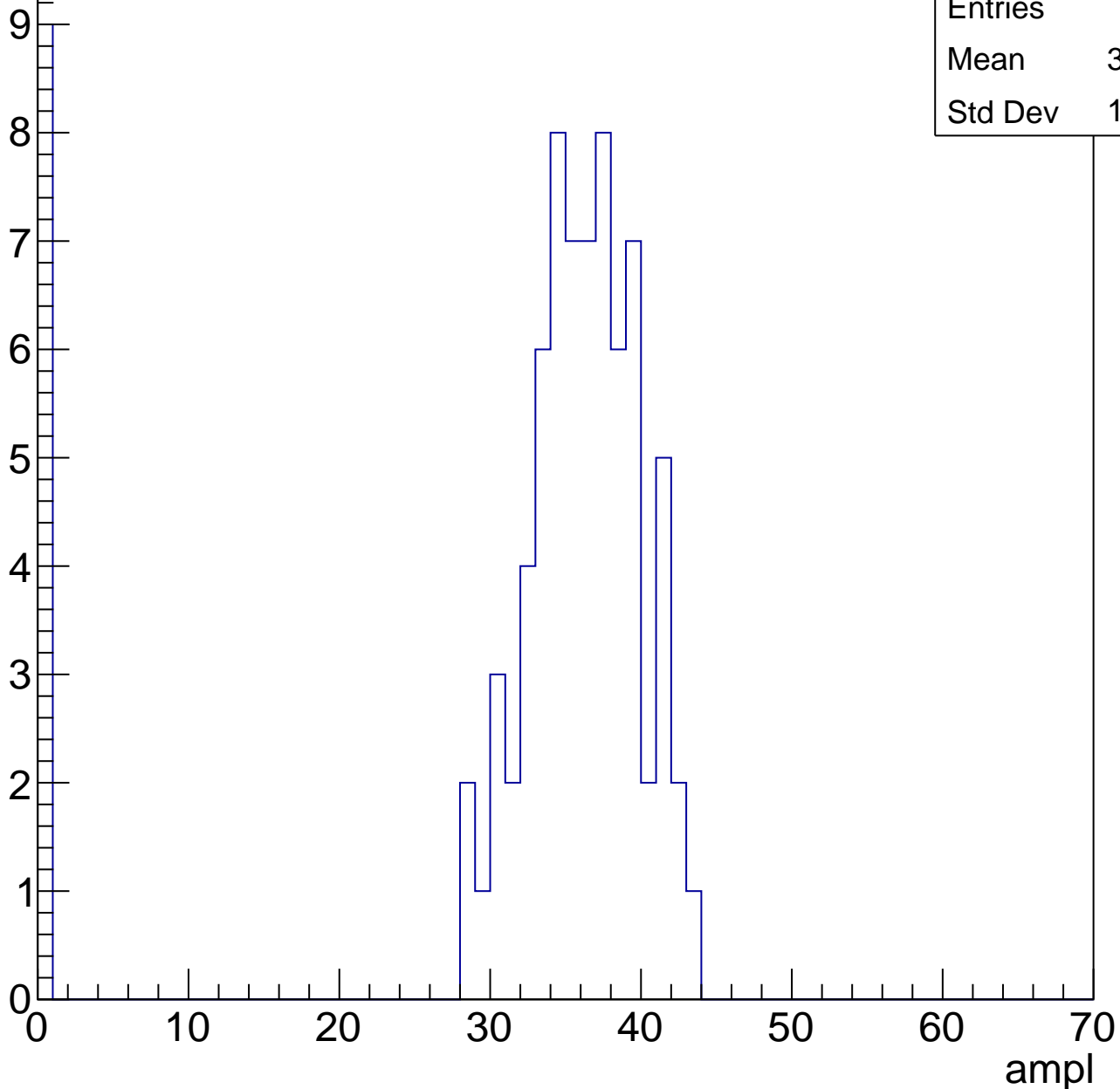


B1L103S, U12-ch40, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	80
Mean	31.76
Std Dev	11.78

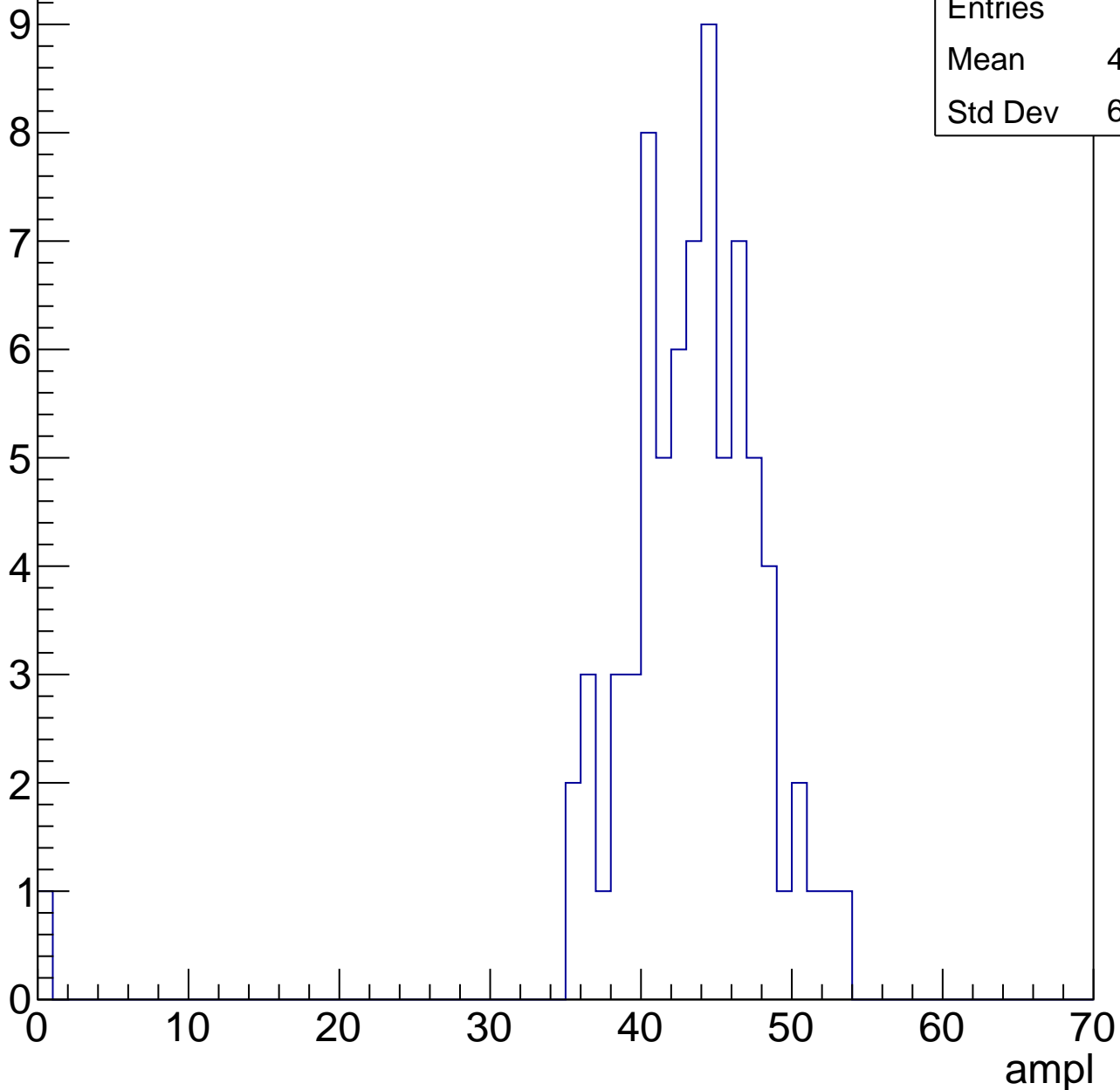


B1L103S, U12-ch40, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	75
Mean	42.65
Std Dev	6.349

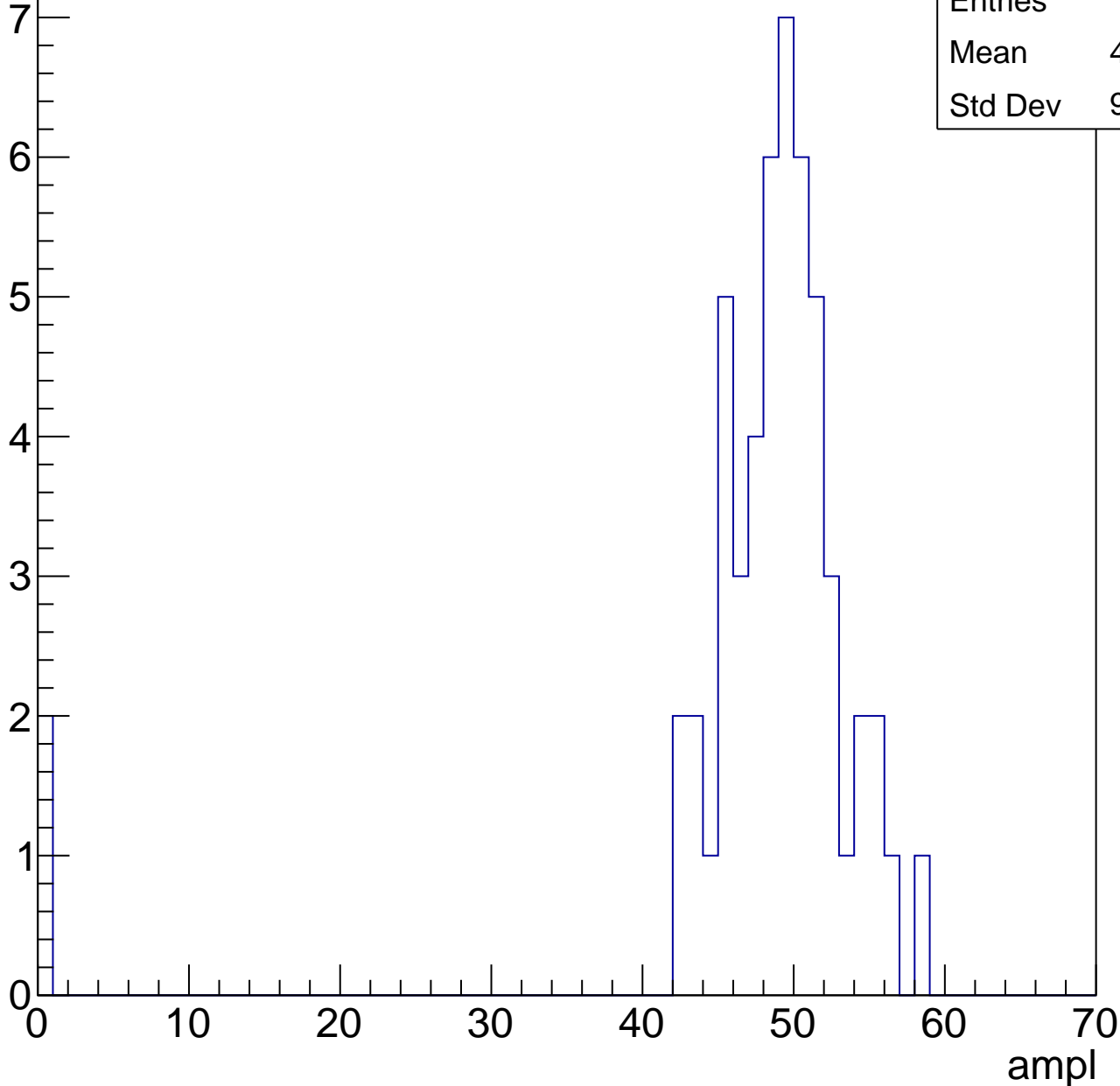


B1L103S, U12-ch40, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	53
Mean	47.02
Std Dev	9.942

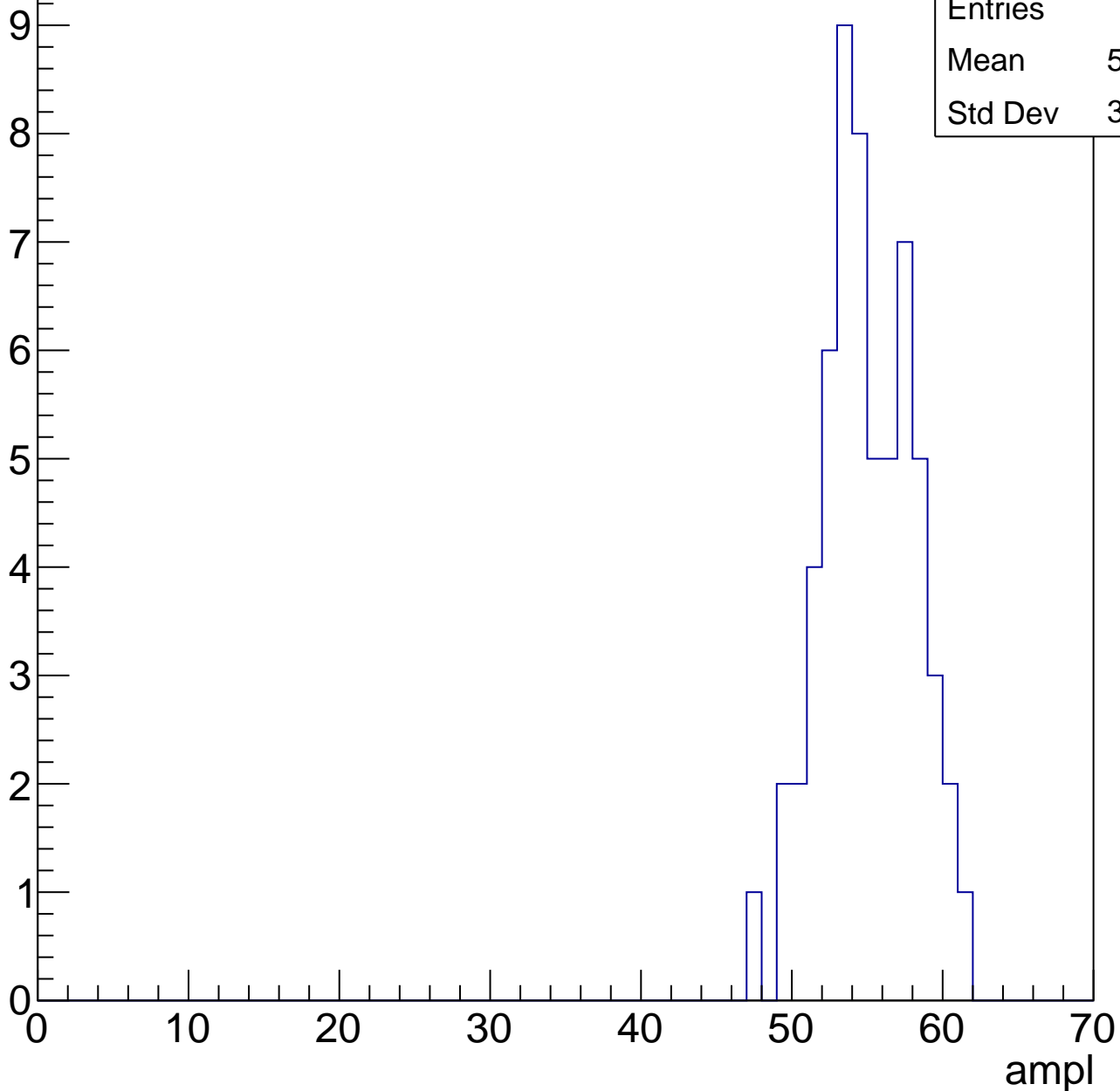


B1L103S, U12-ch40, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	54.53
Std Dev	3.019



B1L103S, U12-ch40, adc5

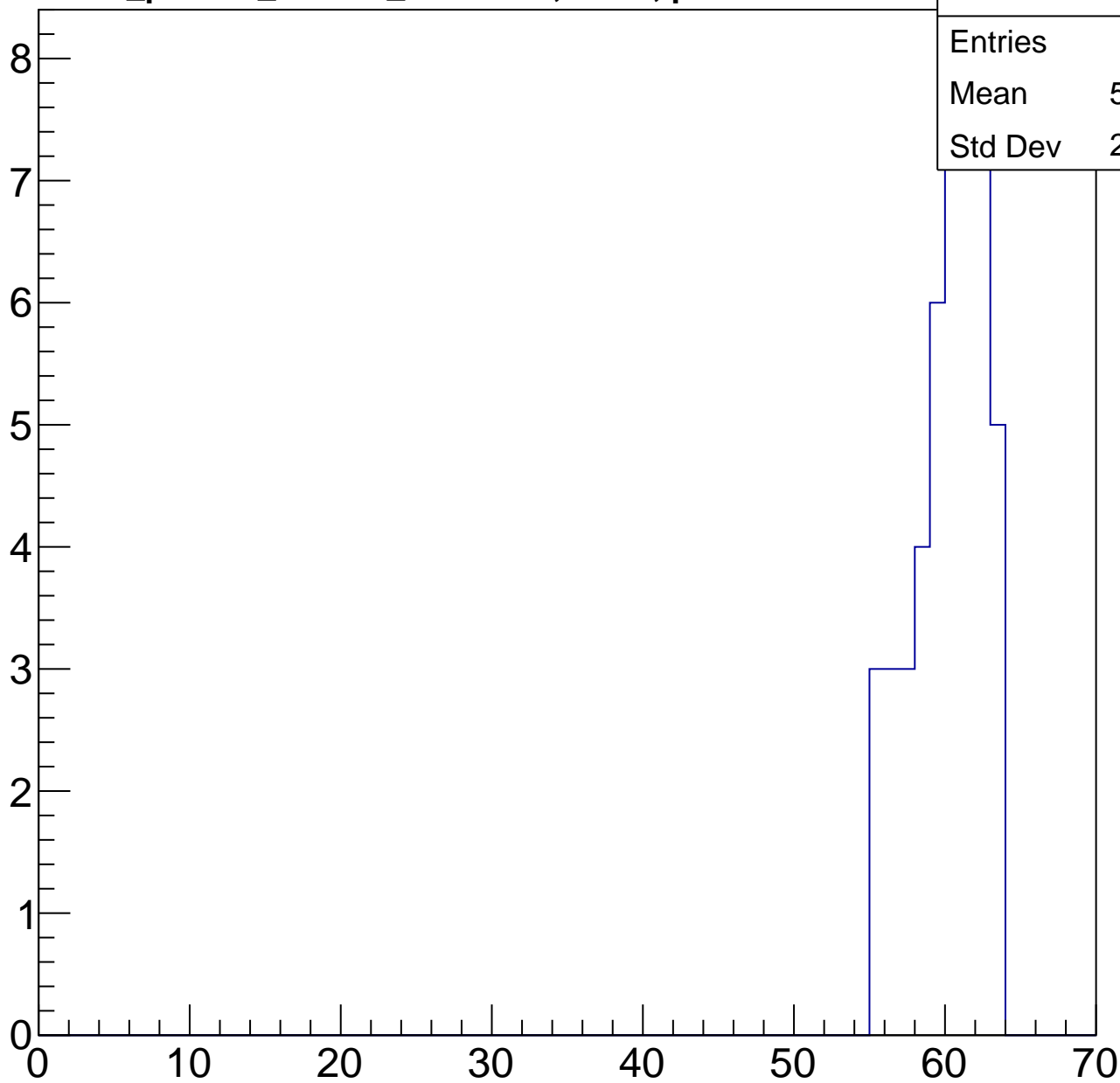
calib_packv5_041523_1651.root, FC#0, port C2

Entry

8
7
6
5
4
3
2
1
0

Entries	48
Mean	59.77
Std Dev	2.303

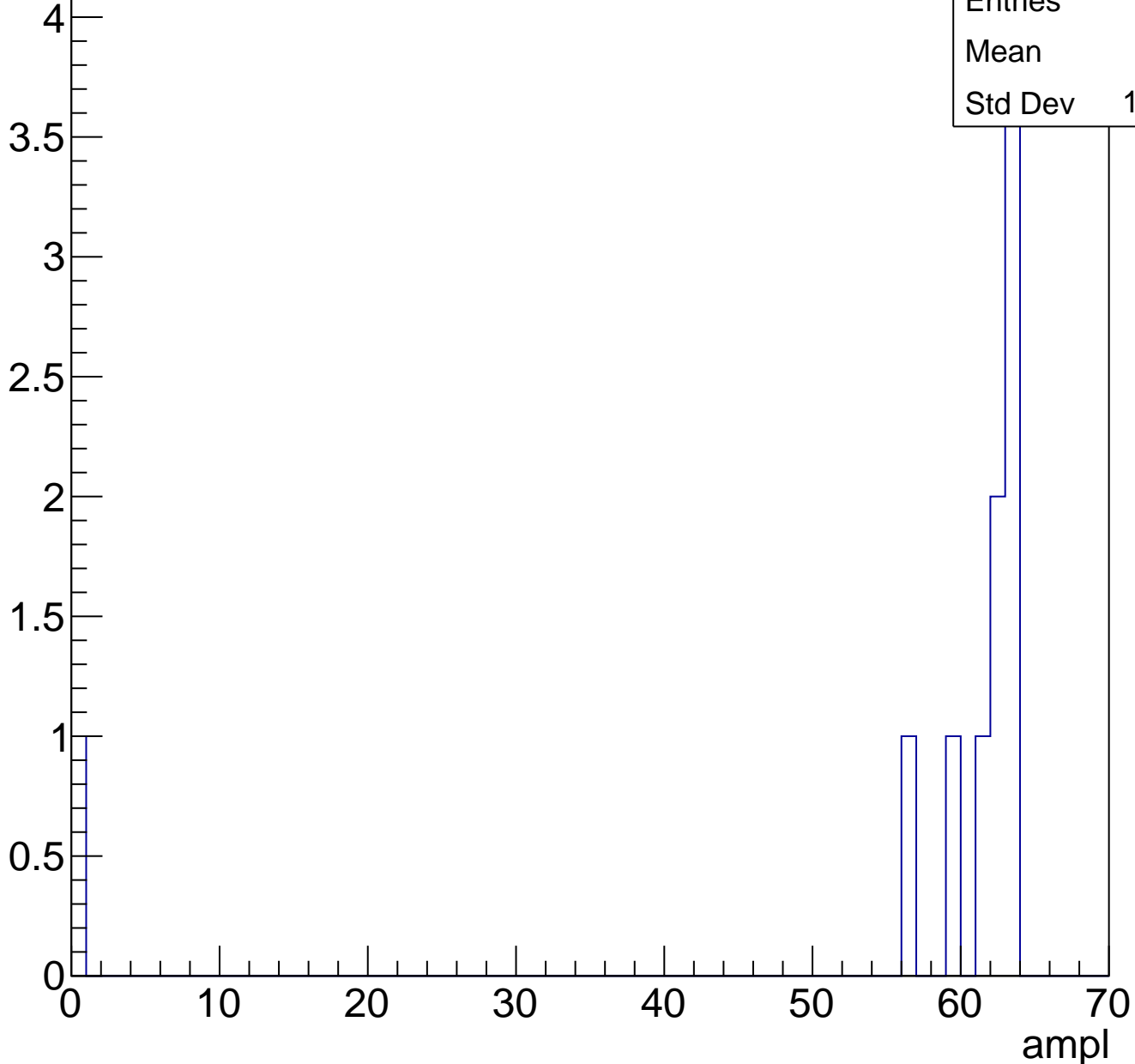
ampl



B1L103S, U12-ch40, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	10
Mean	55.2
Std Dev	18.52

B1L103S, U12-ch40, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	3.316
Std Dev	14.07

Entry

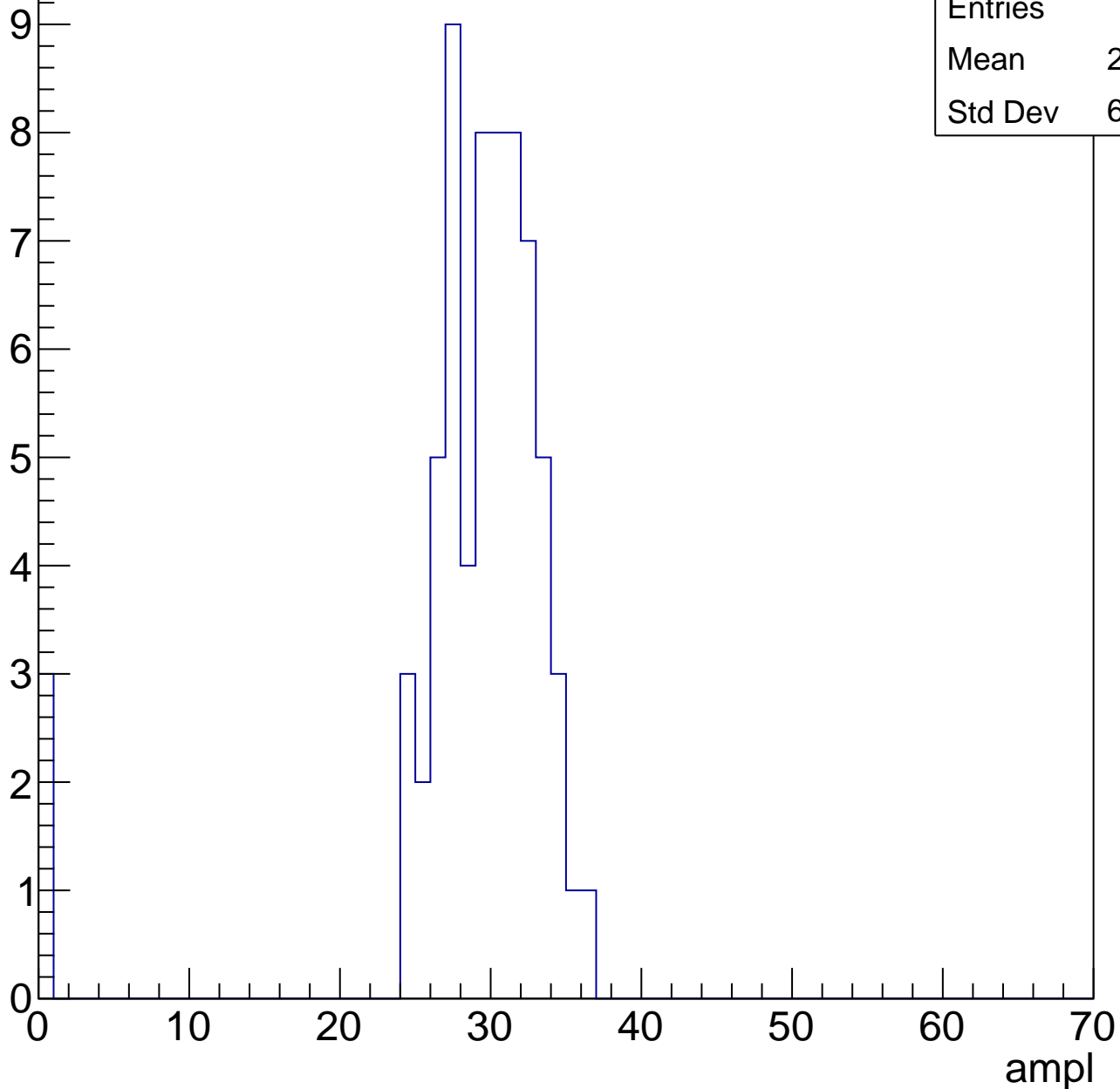


B1L103S, U12-ch41, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

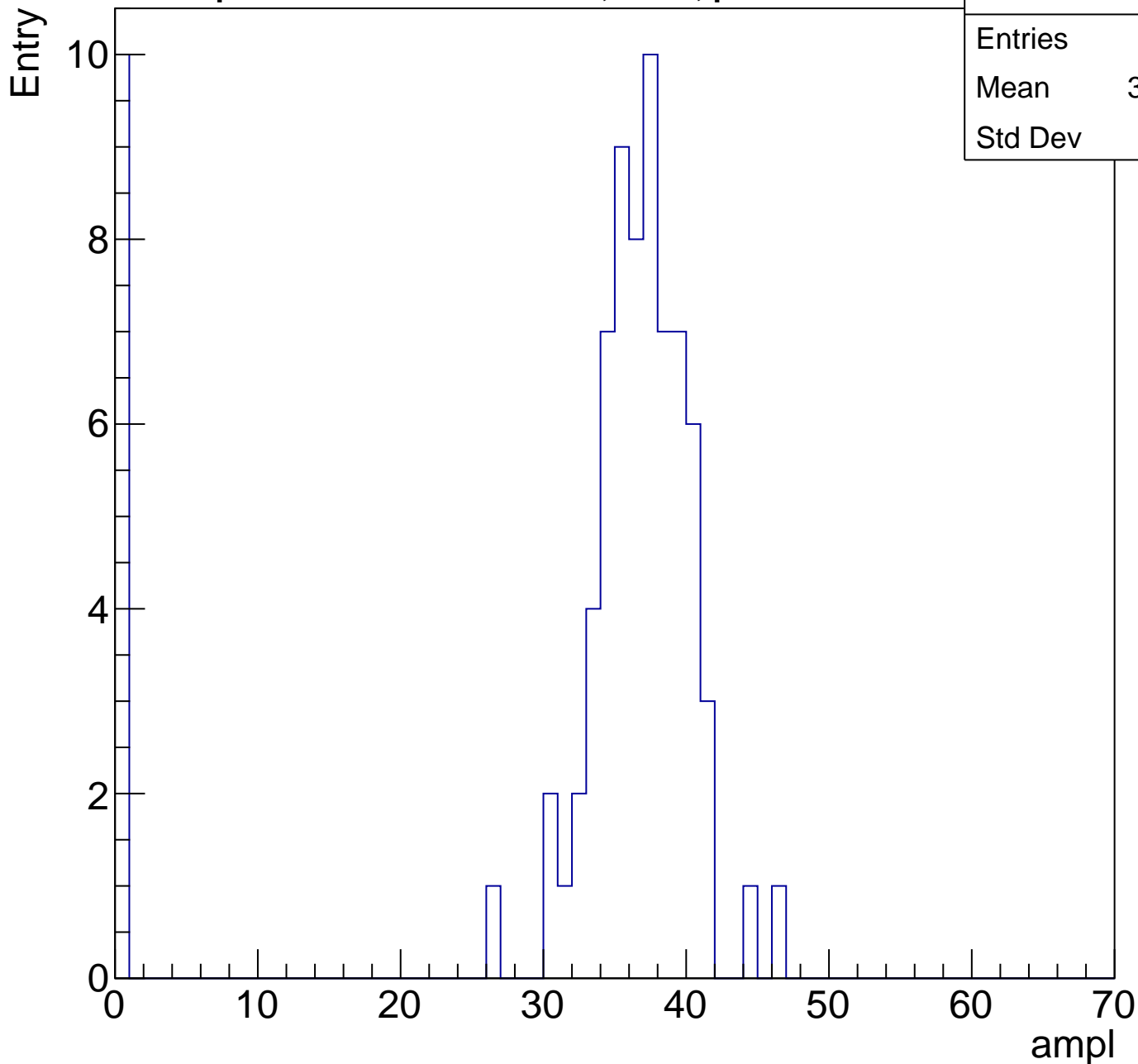
Entries	67
Mean	28.19
Std Dev	6.708



B1L103S, U12-ch41, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	79
Mean	31.85
Std Dev	12.5



B1L103S, U12-ch41, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	59
Mean	41.88
Std Dev	6.266

Entry

10

8

6

4

2

0

0

10

20

30

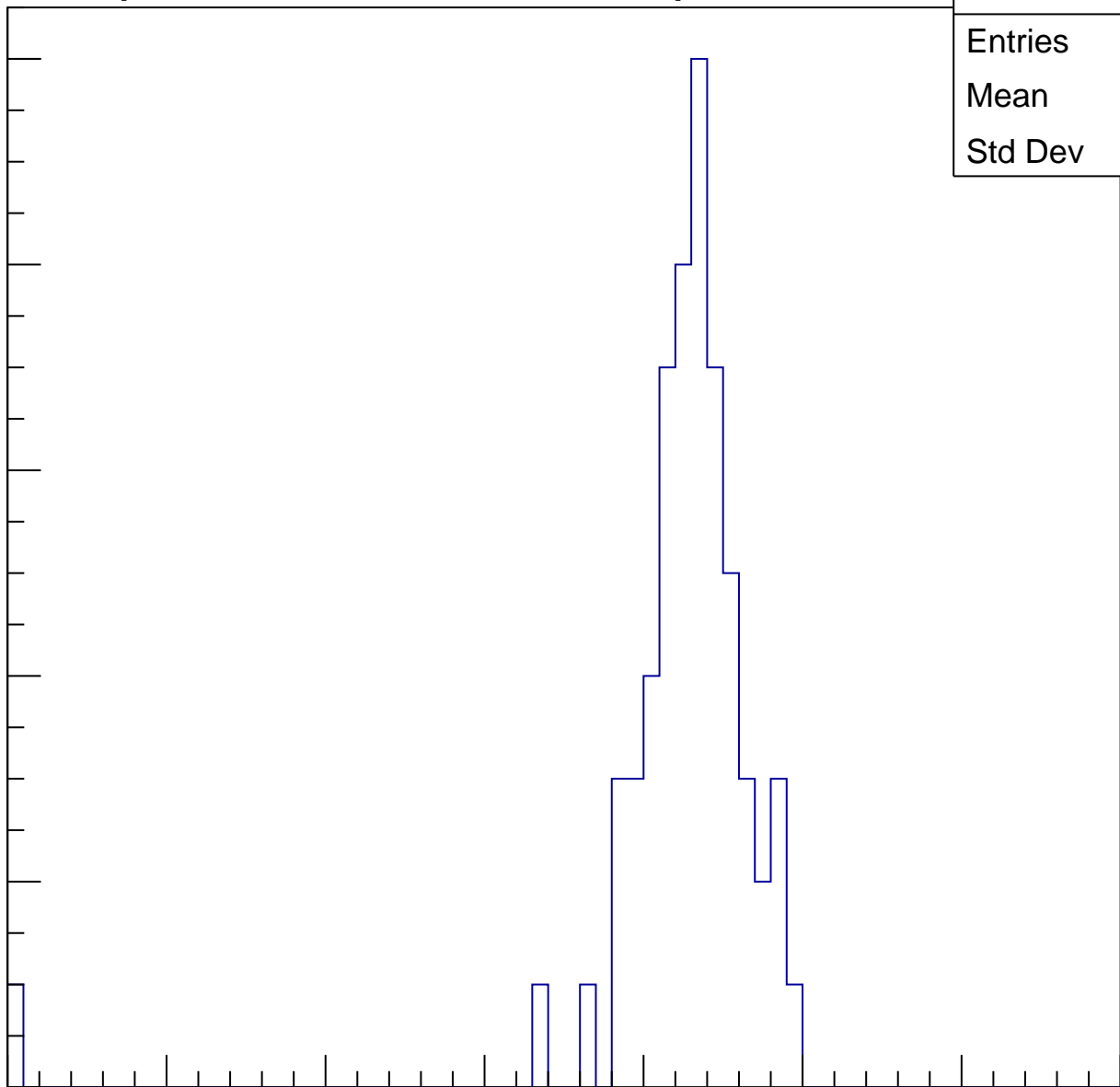
40

50

60

70

ampl

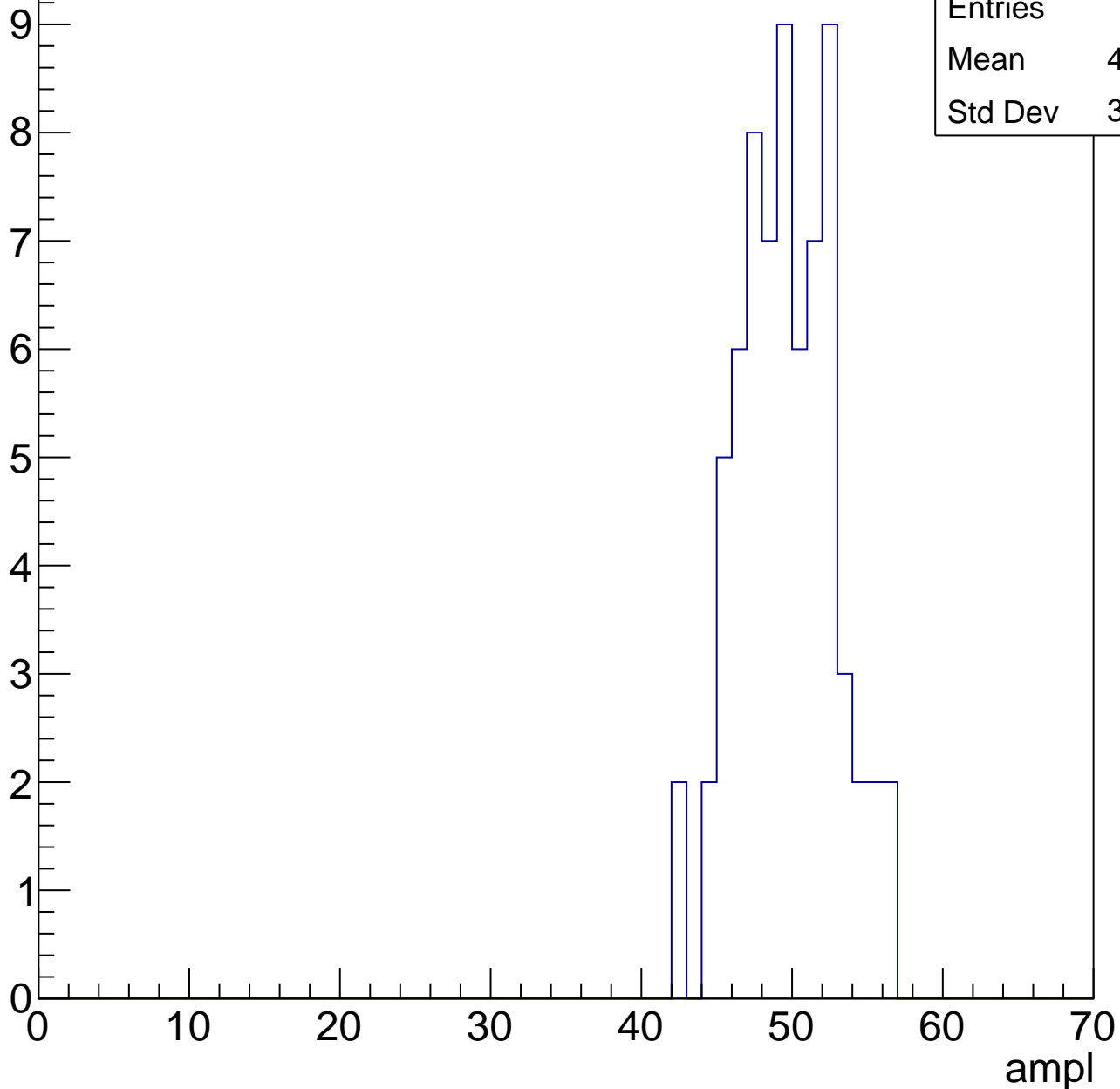


B1L103S, U12-ch41, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	49.14
Std Dev	3.168

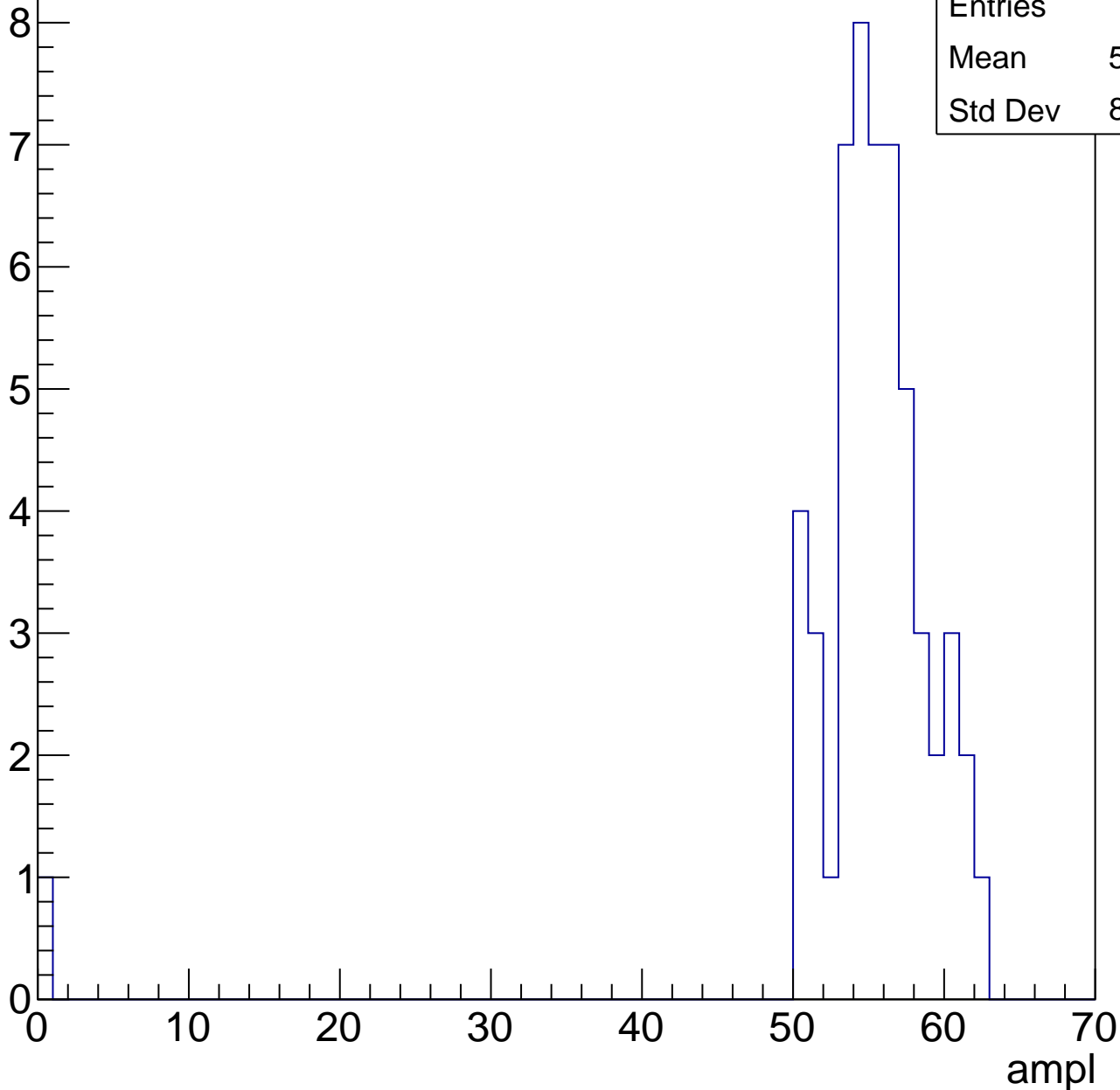


B1L103S, U12-ch41, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

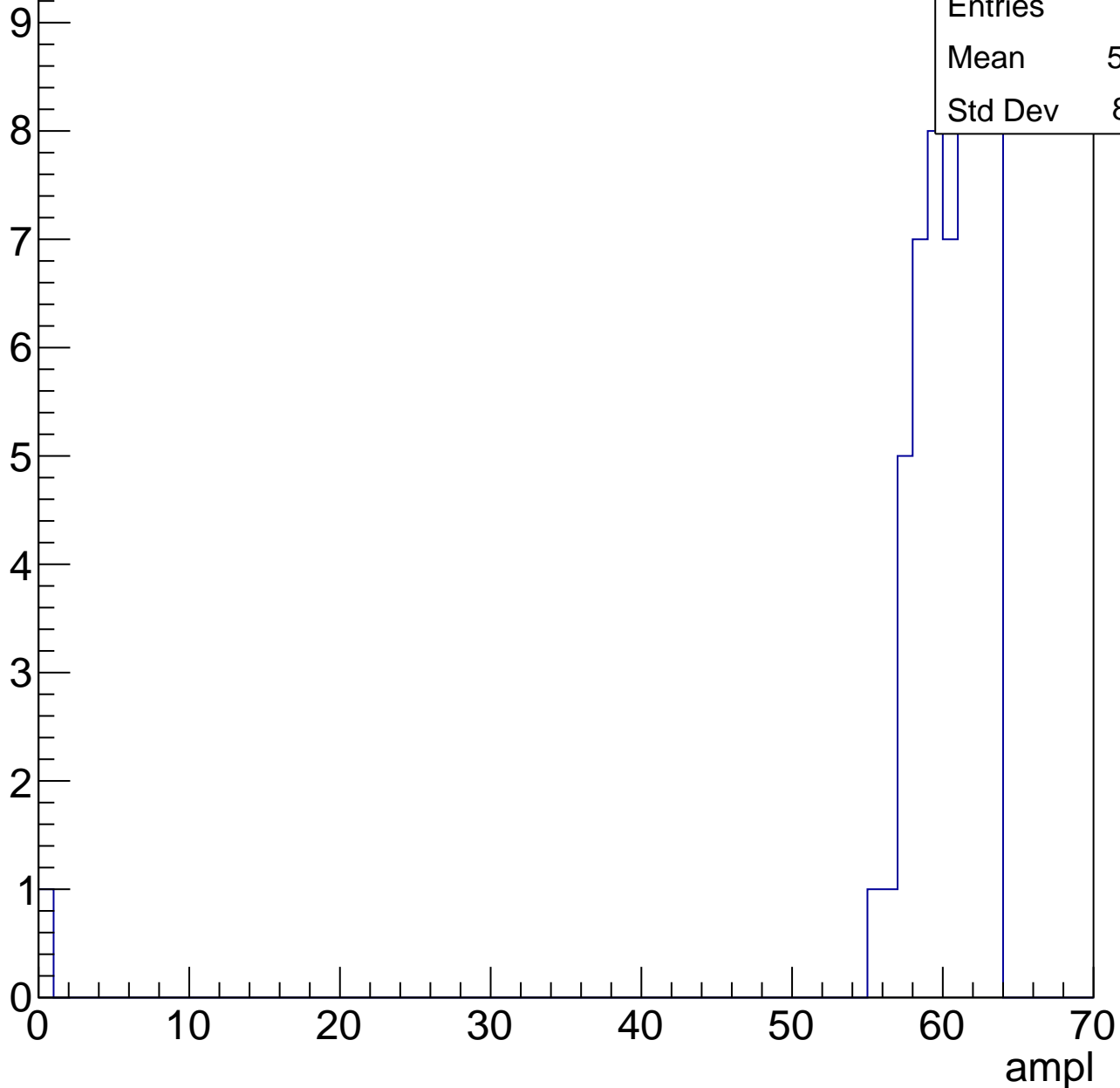
Entries	54
Mean	54.19
Std Dev	8.009



B1L103S, U12-ch41, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch41, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

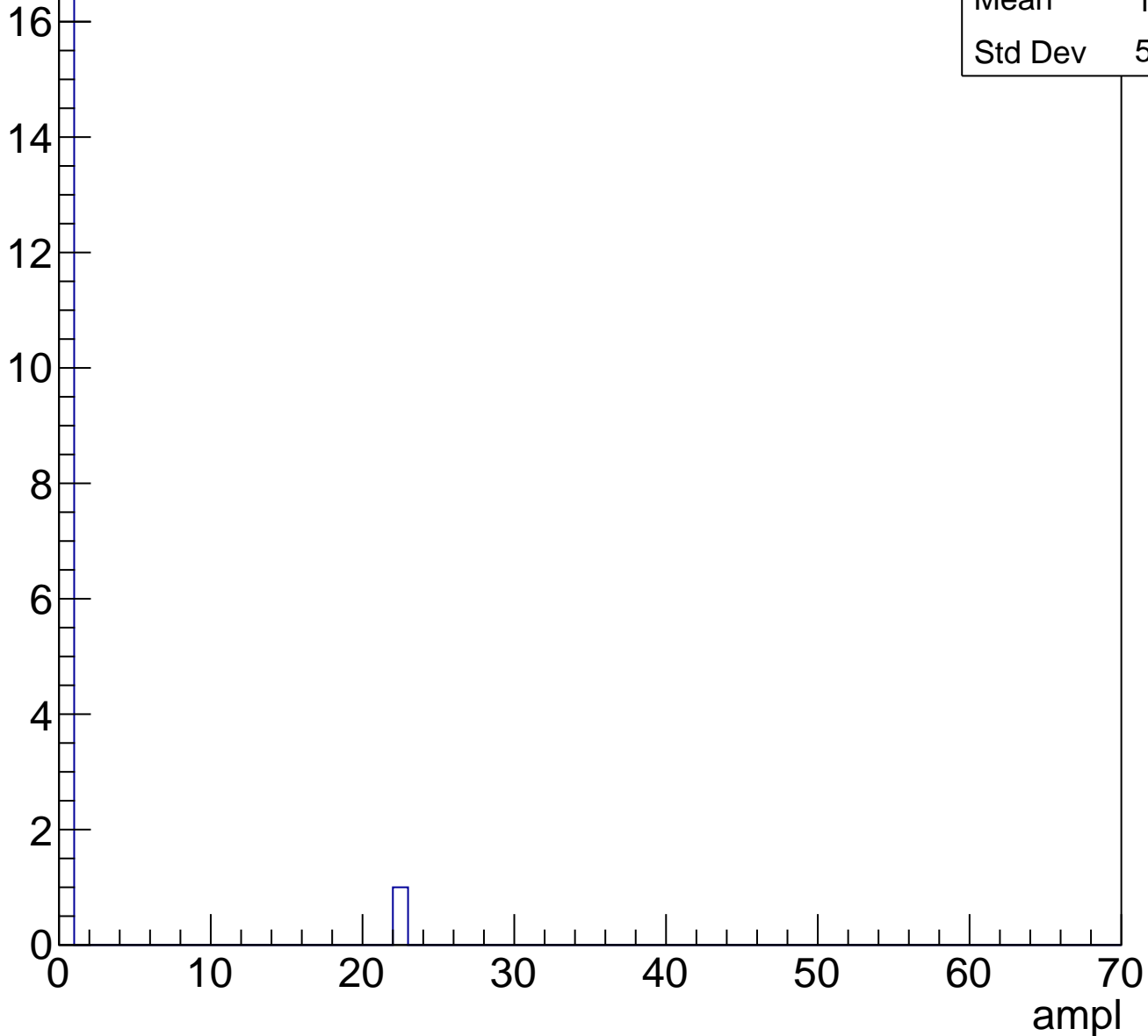


B1L103S, U12-ch41, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	18
Mean	1.222
Std Dev	5.039

Entry

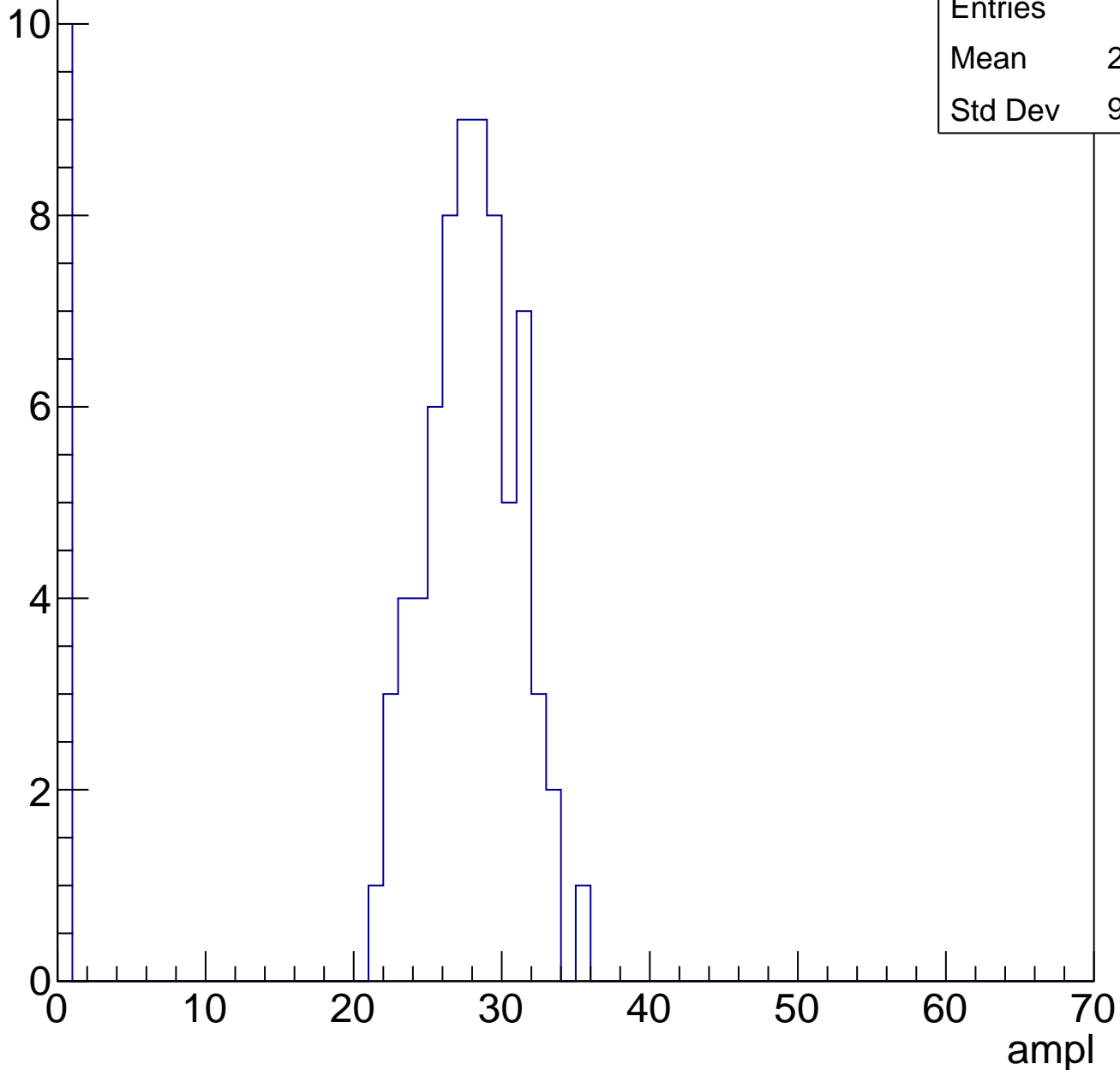


B1L103S, U12-ch42, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	80
Mean	24.05
Std Dev	9.517

Entry



B1L103S, U12-ch42, adc1

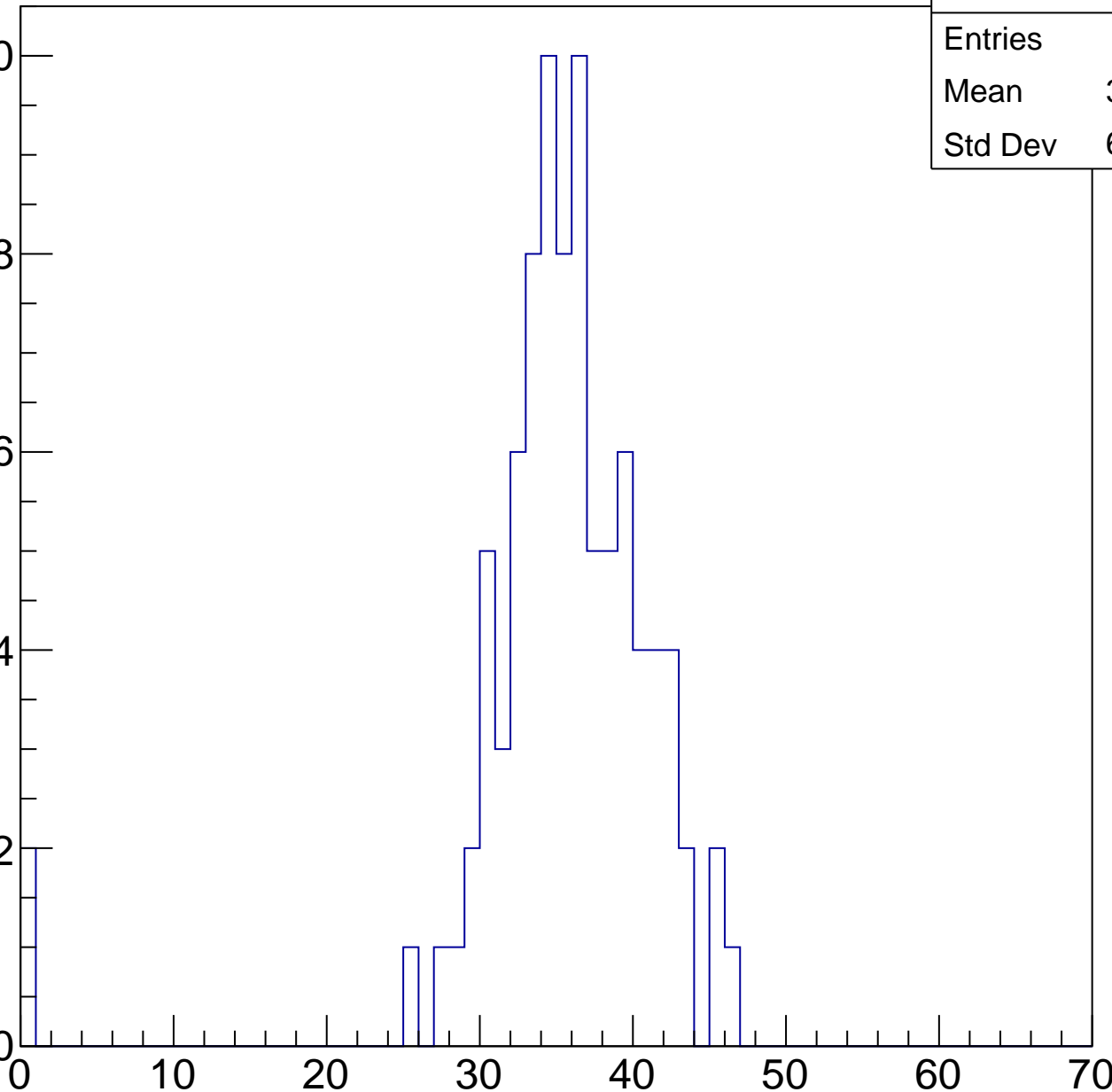
calib_packv5_041523_1651.root, FC#0, port C2

Entries	90
Mean	34.89
Std Dev	6.719

Entry

10
8
6
4
2
0

ampl

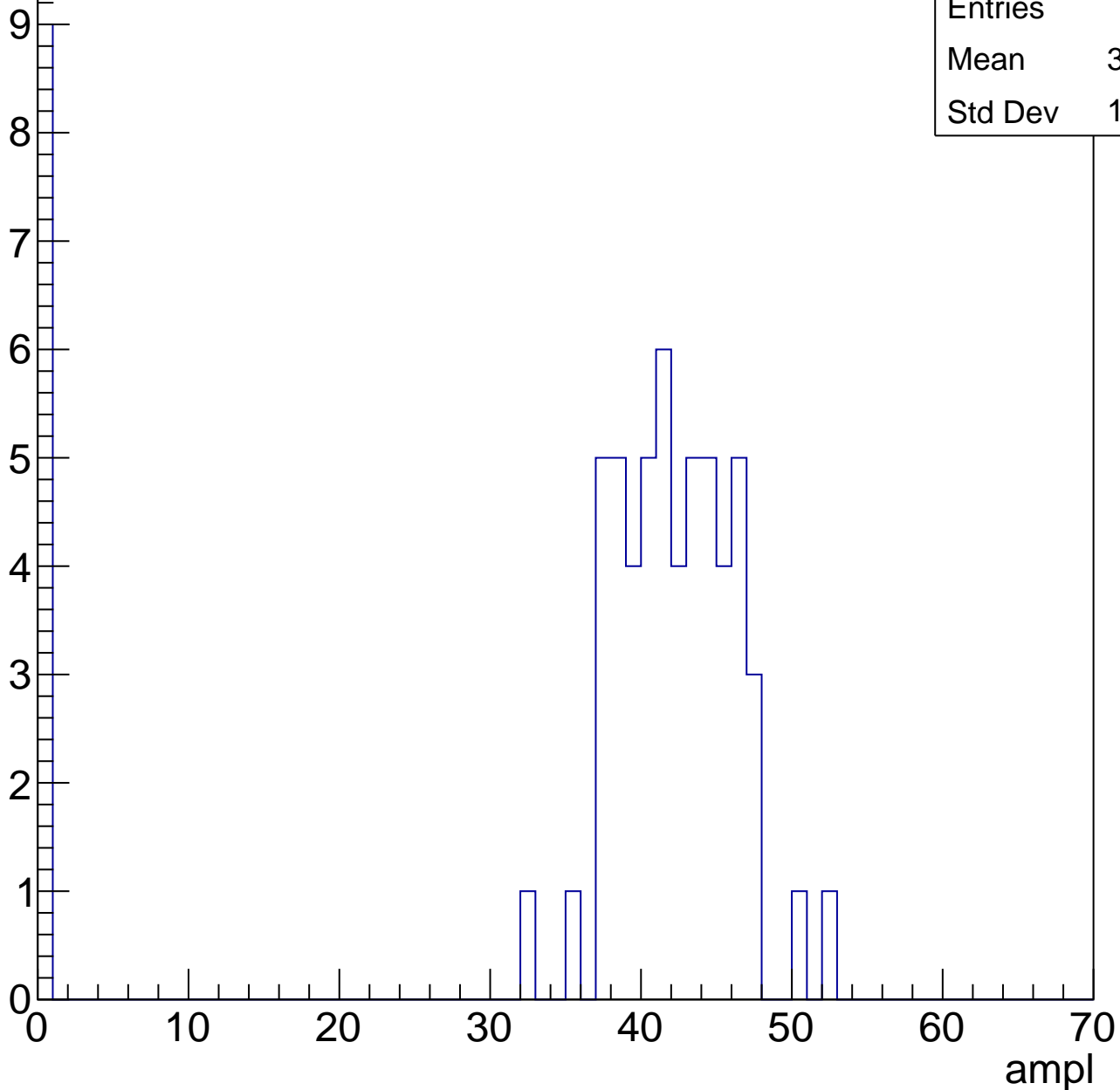


B1L103S, U12-ch42, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	35.94
Std Dev	14.96

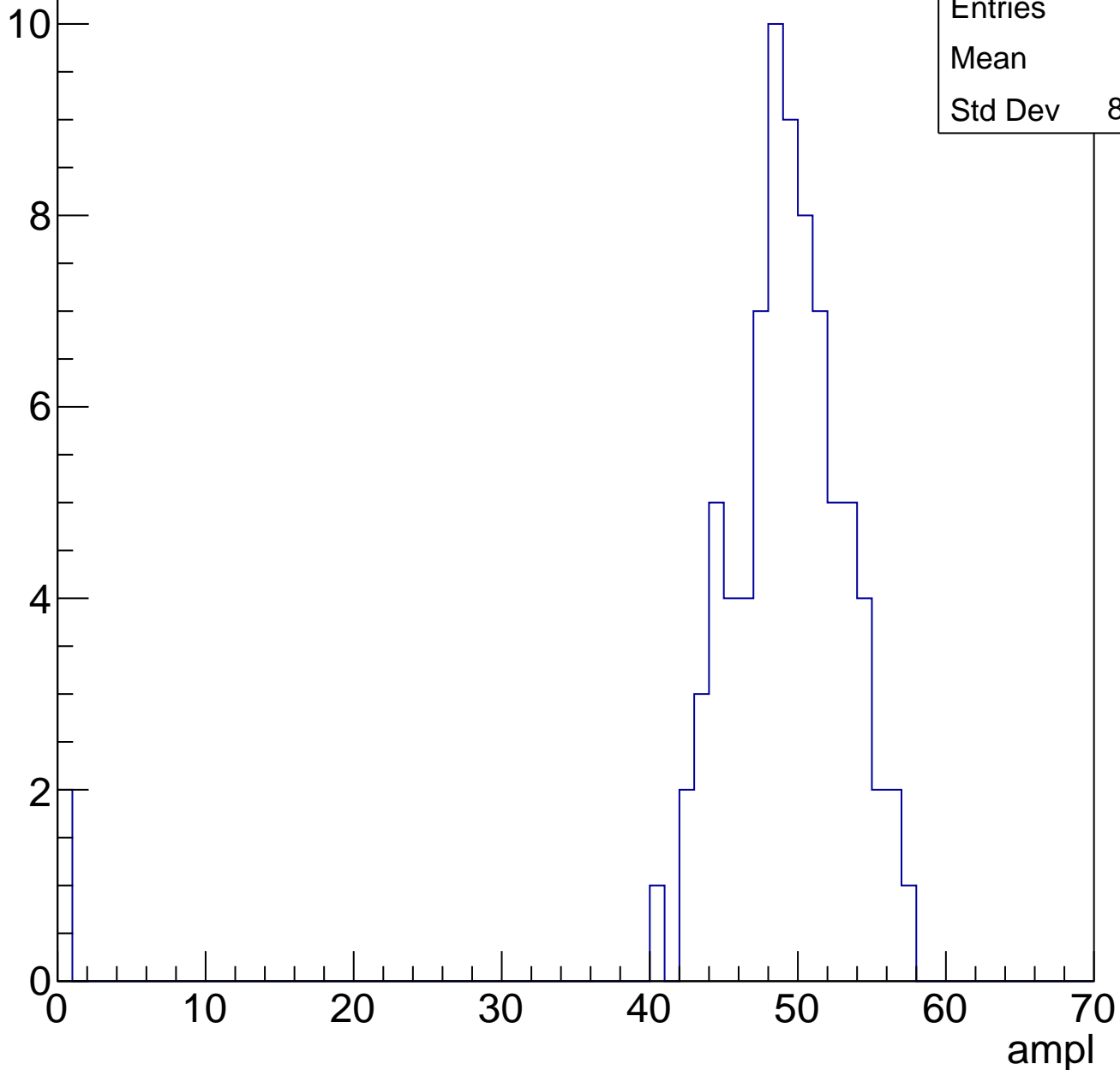


B1L103S, U12-ch42, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	81
Mean	47.7
Std Dev	8.397

Entry

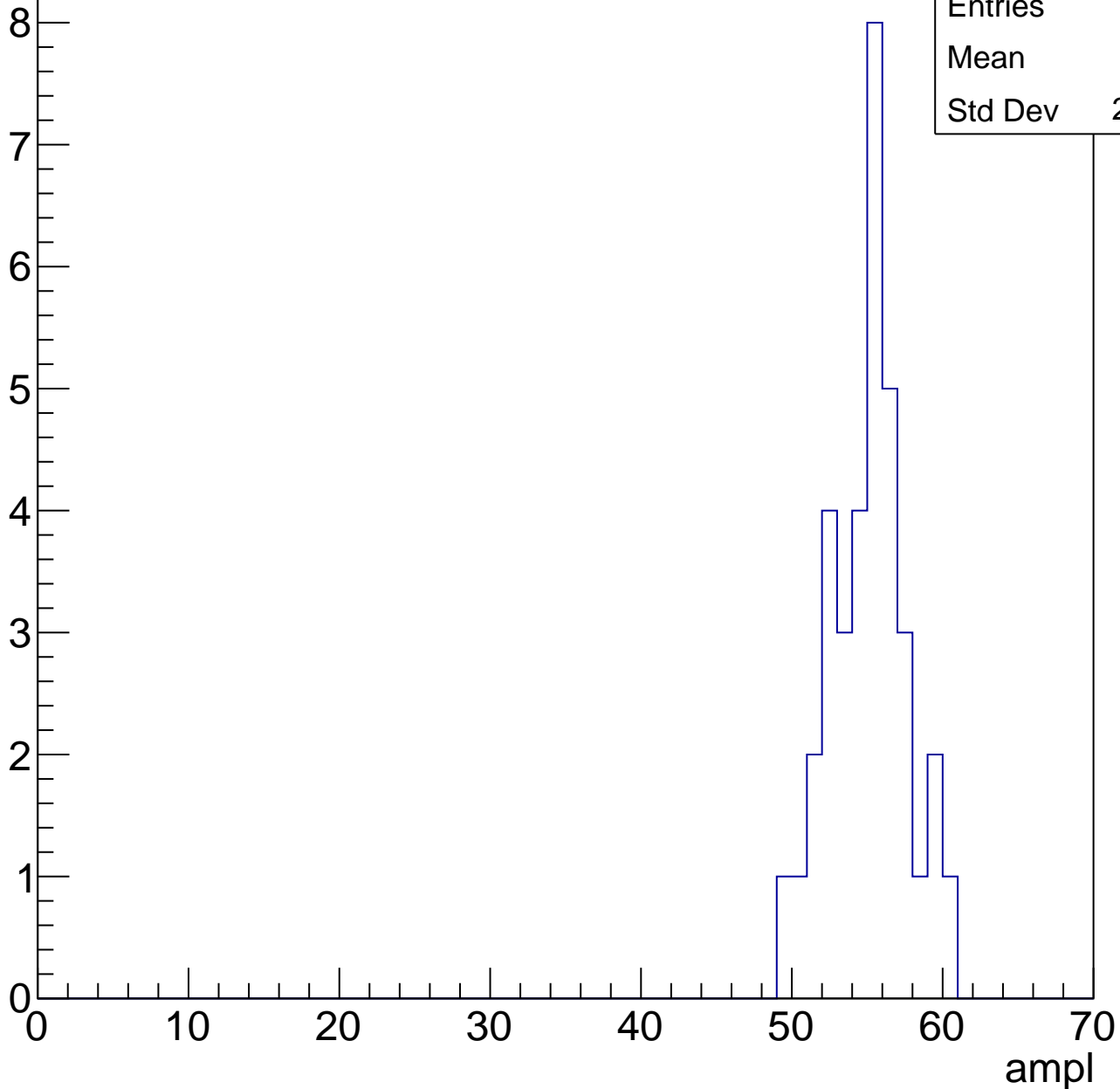


B1L103S, U12-ch42, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	35
Mean	54.6
Std Dev	2.521

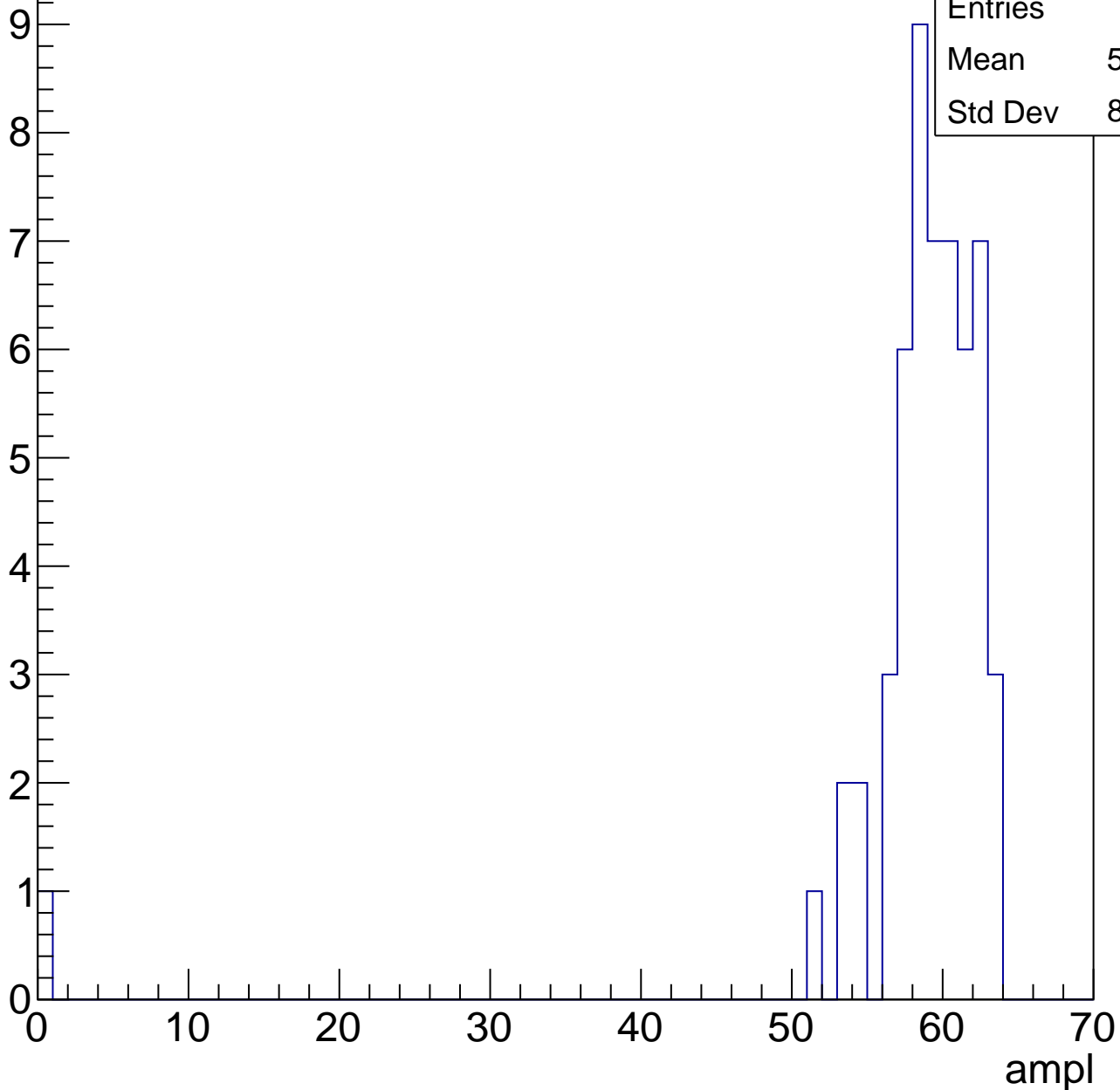


B1L103S, U12-ch42, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	54
Mean	57.76
Std Dev	8.373

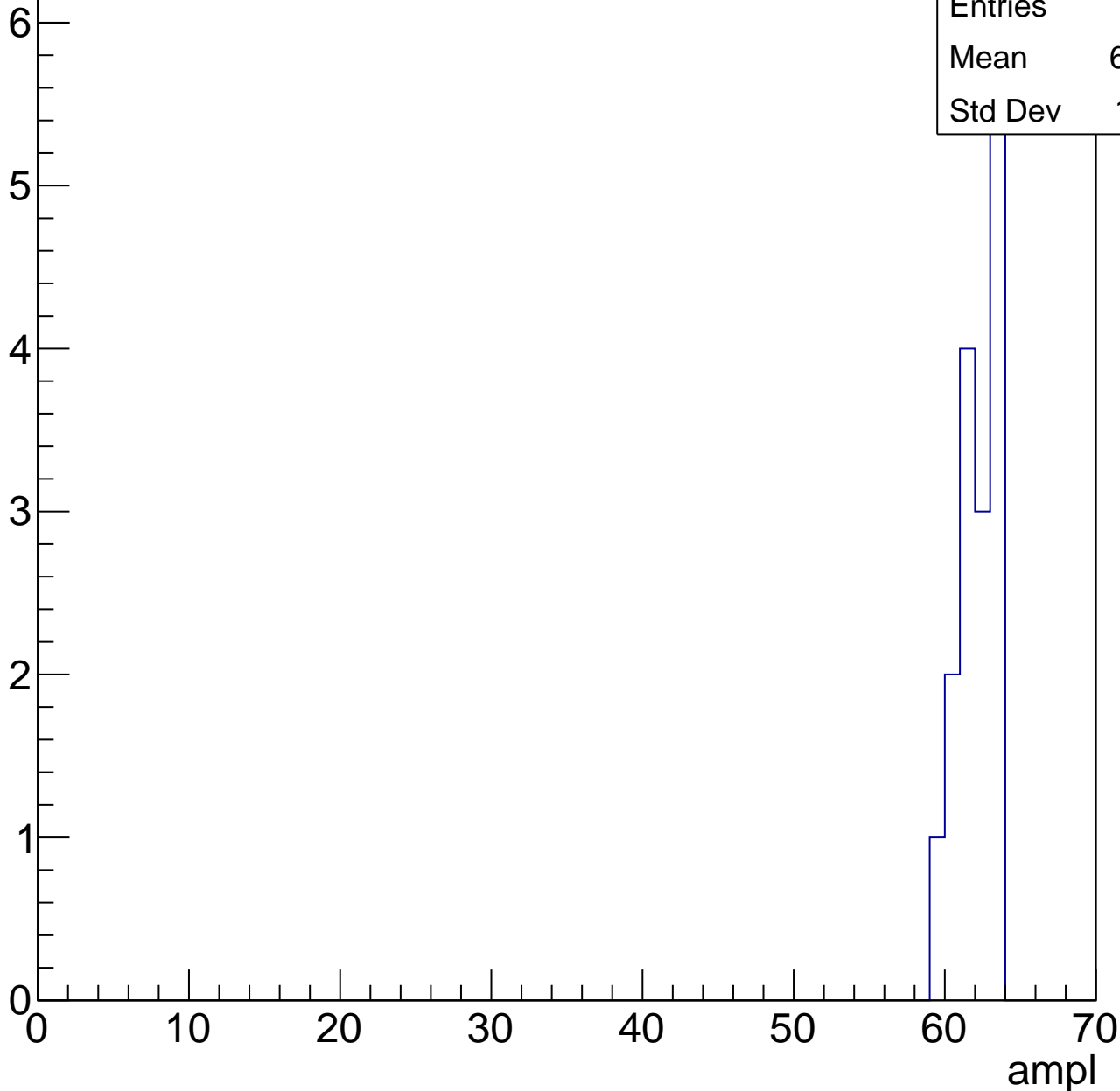


B1L103S, U12-ch42, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	16
Mean	61.69
Std Dev	1.261

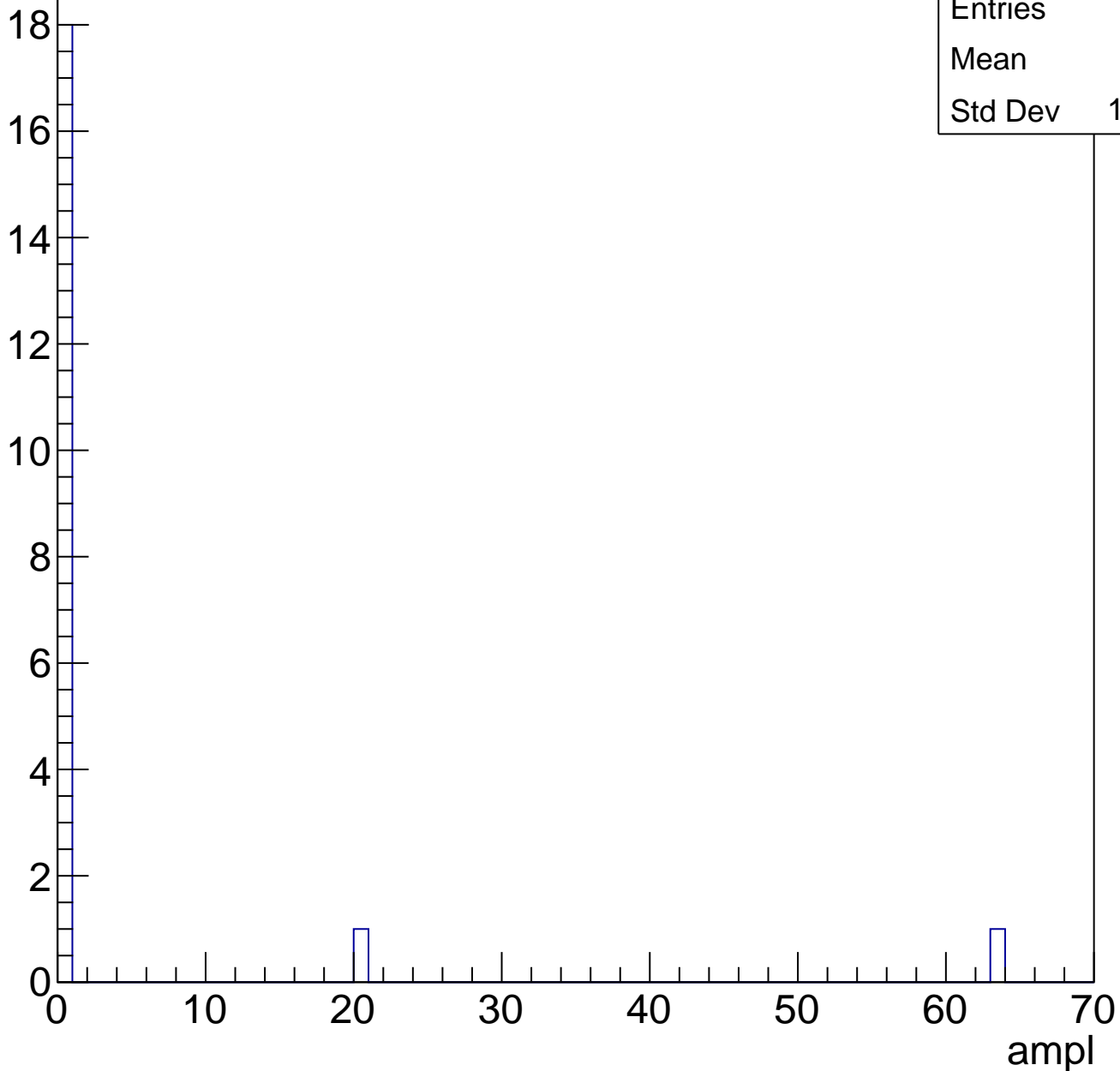


B1L103S, U12-ch42, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	4.15
Std Dev	14.19

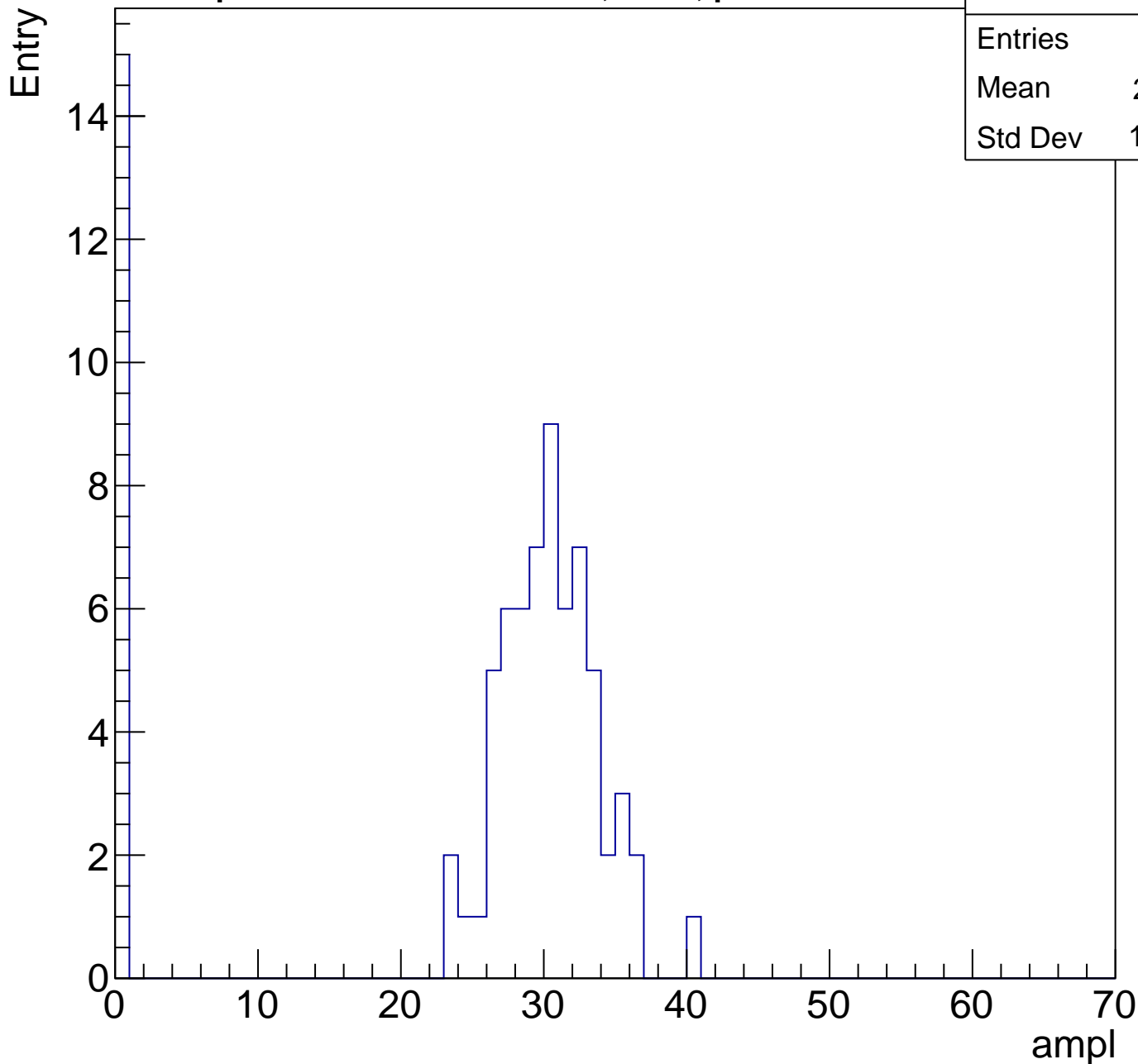
Entry



B1L103S, U12-ch43, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	78
Mean	24.21
Std Dev	12.18



B1L103S, U12-ch43, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	86
Mean	31.88
Std Dev	12.63

Entry

10

8

6

4

2

0

0

10

20

30

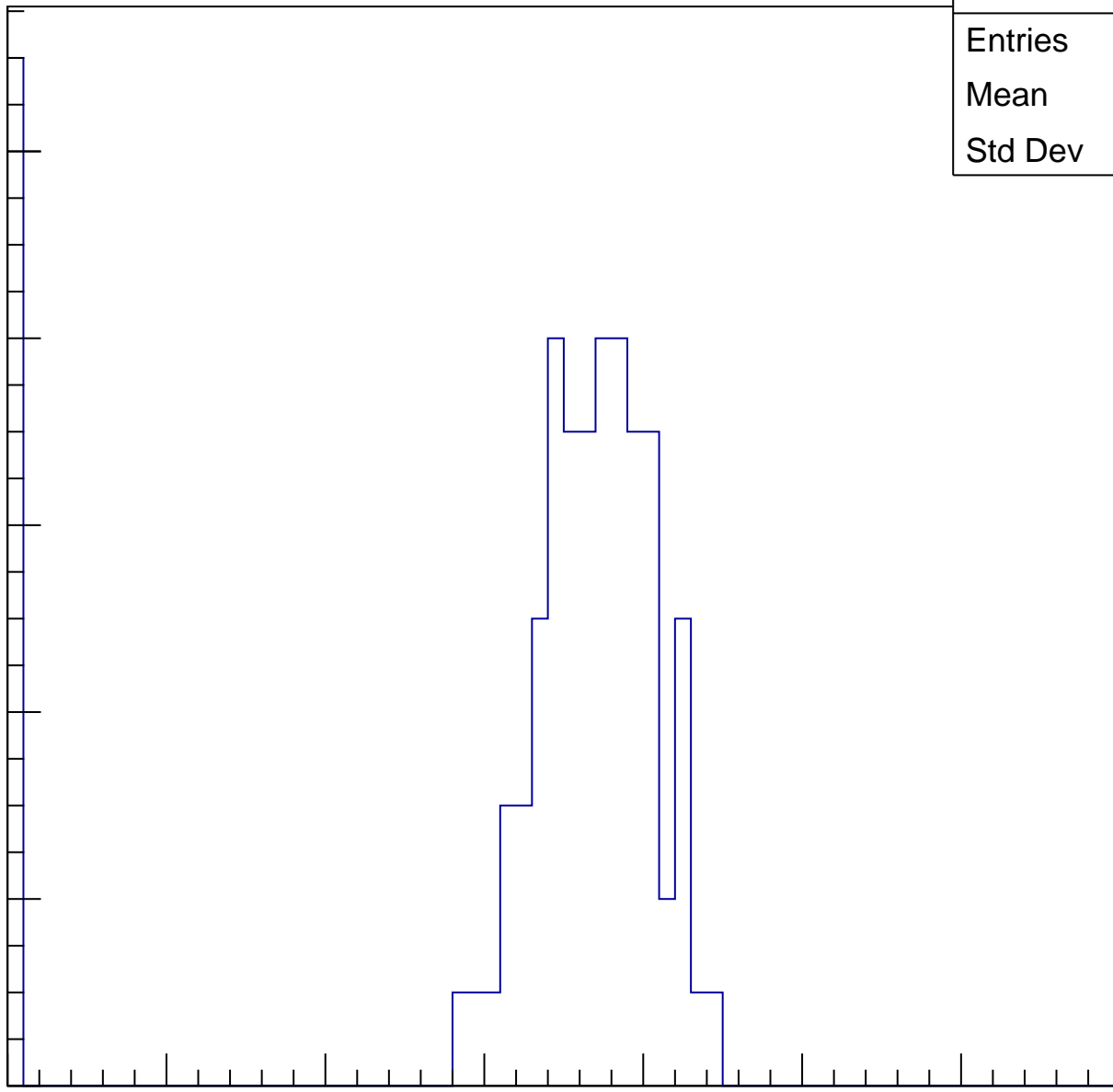
40

50

60

70

ampl

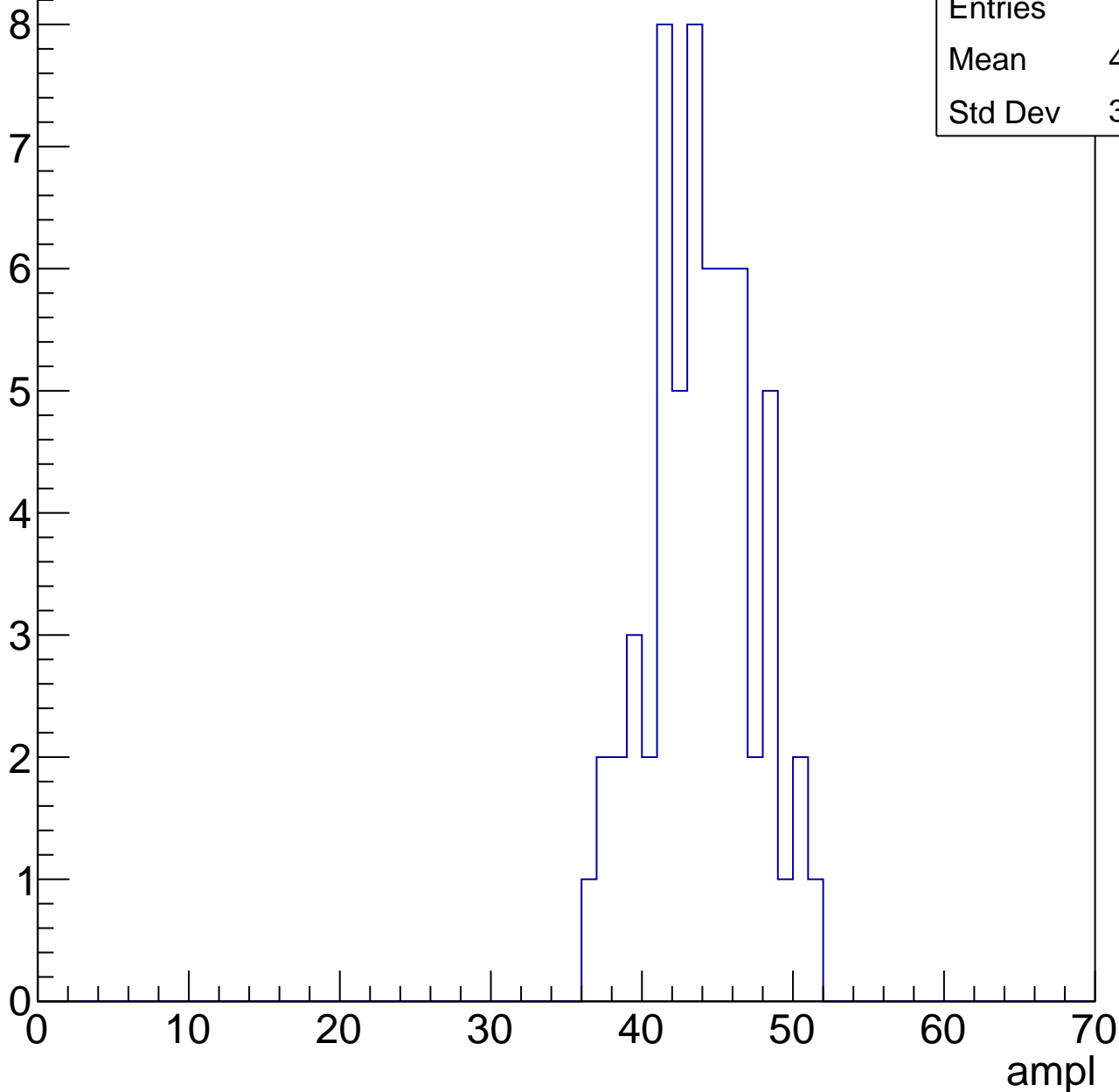


B1L103S, U12-ch43, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	43.48
Std Dev	3.413

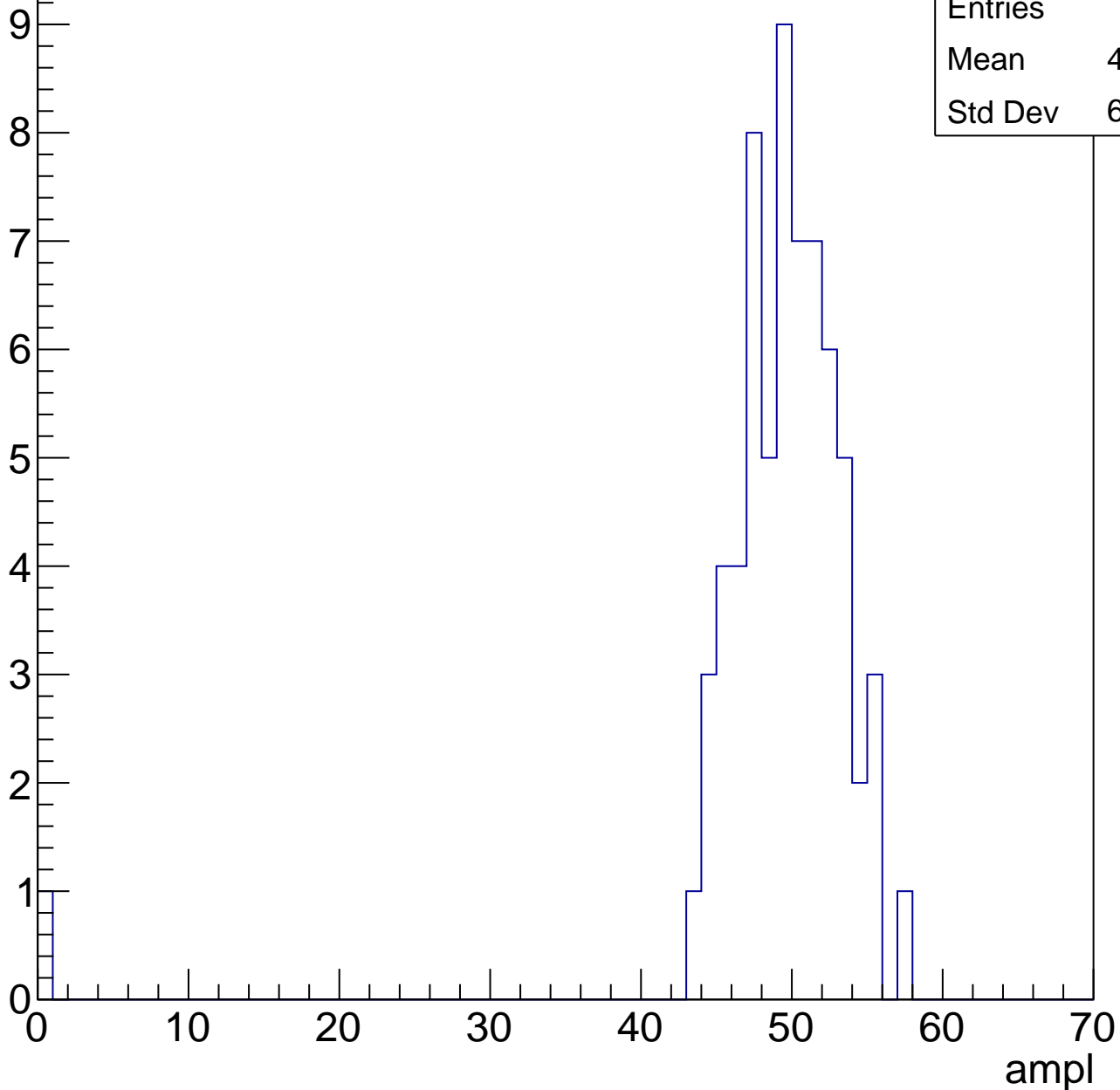


B1L103S, U12-ch43, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	48.64
Std Dev	6.777



B1L103S, U12-ch43, adc4

calib_packv5_041523_1651.root, FC#0, port C2

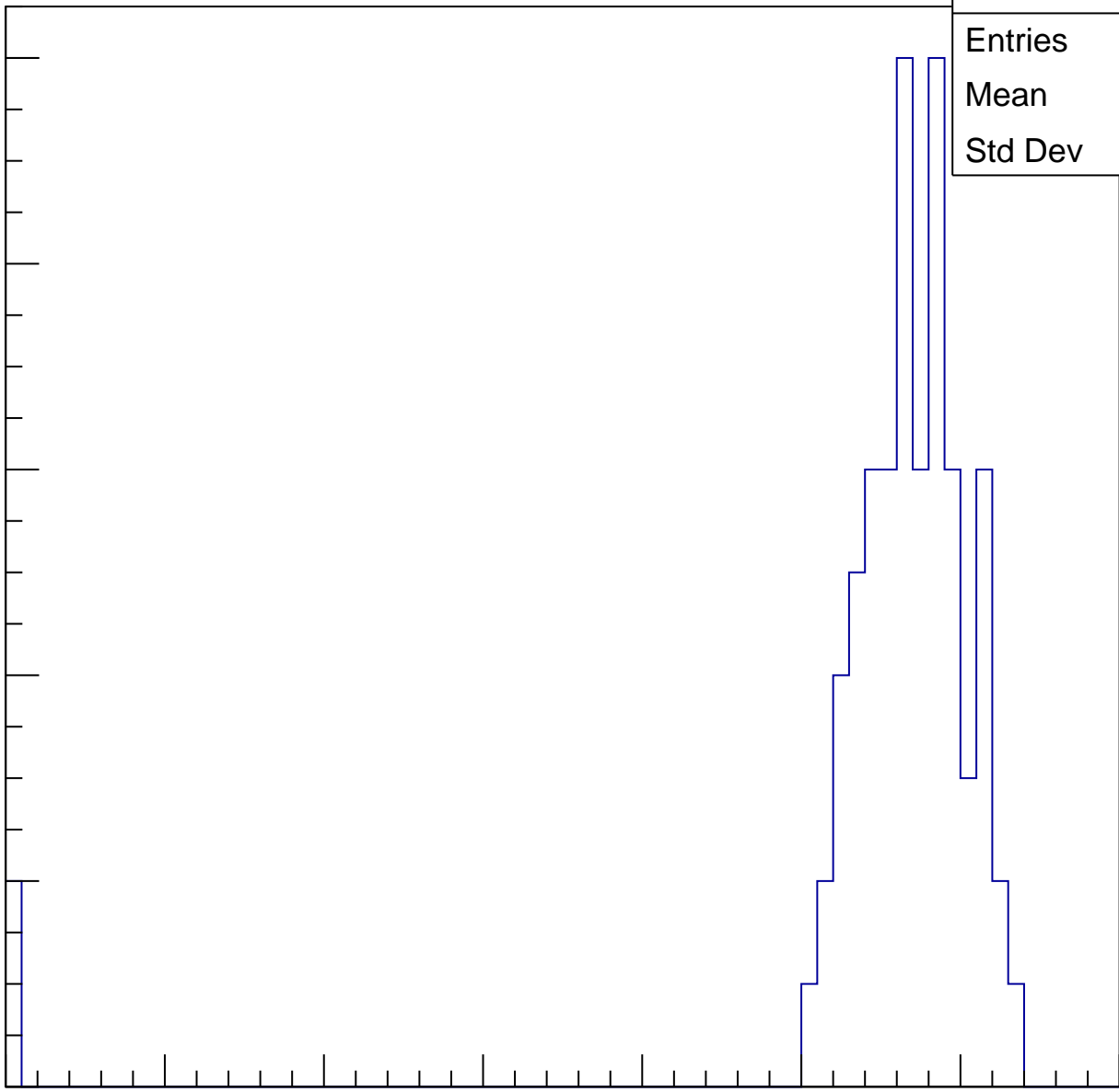
Entries	70
Mean	54.97
Std Dev	9.886

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

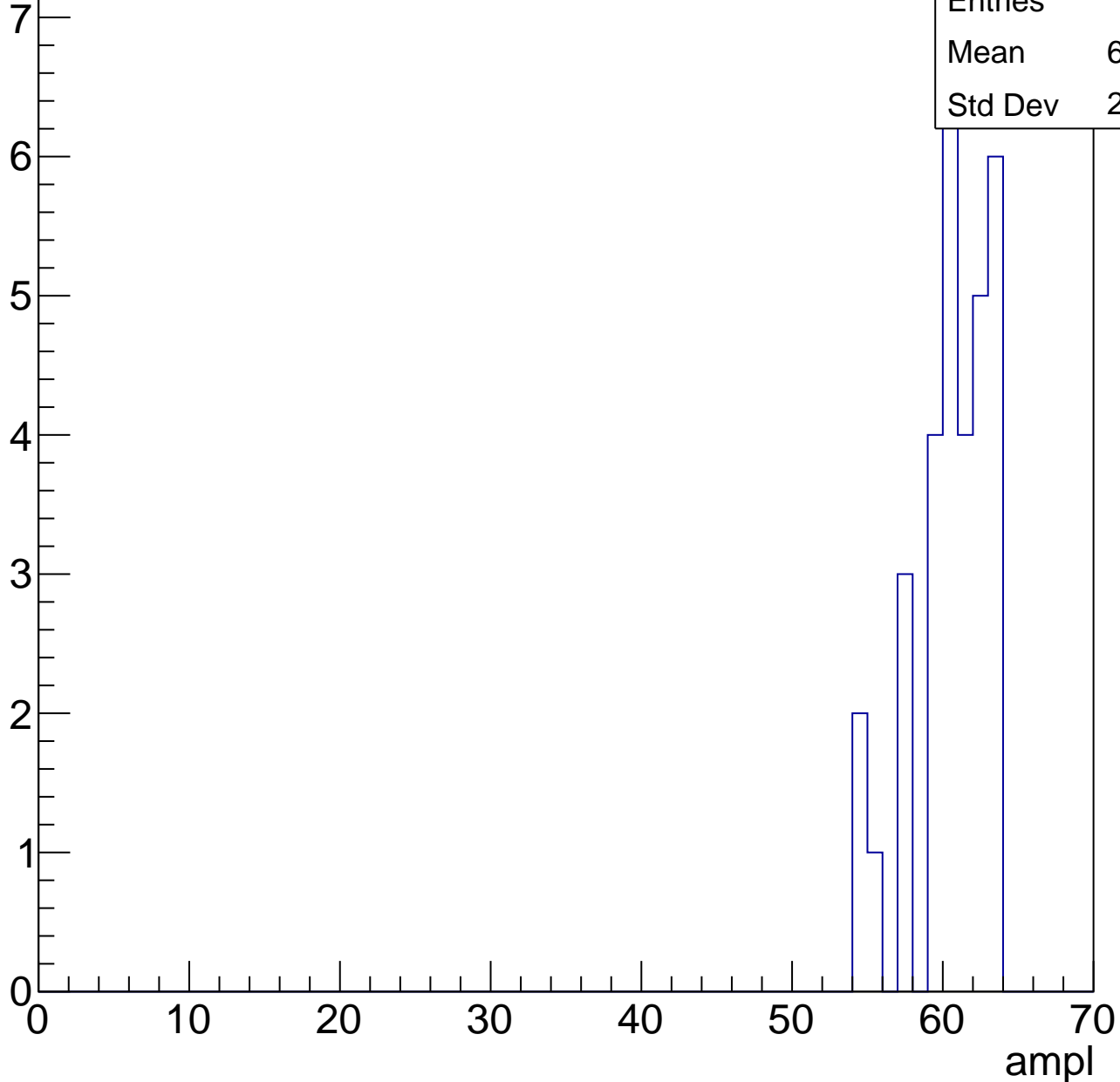
ampl



B1L103S, U12-ch43, adc5

calib_packv5_041523_1651.root, FC#0, port C2

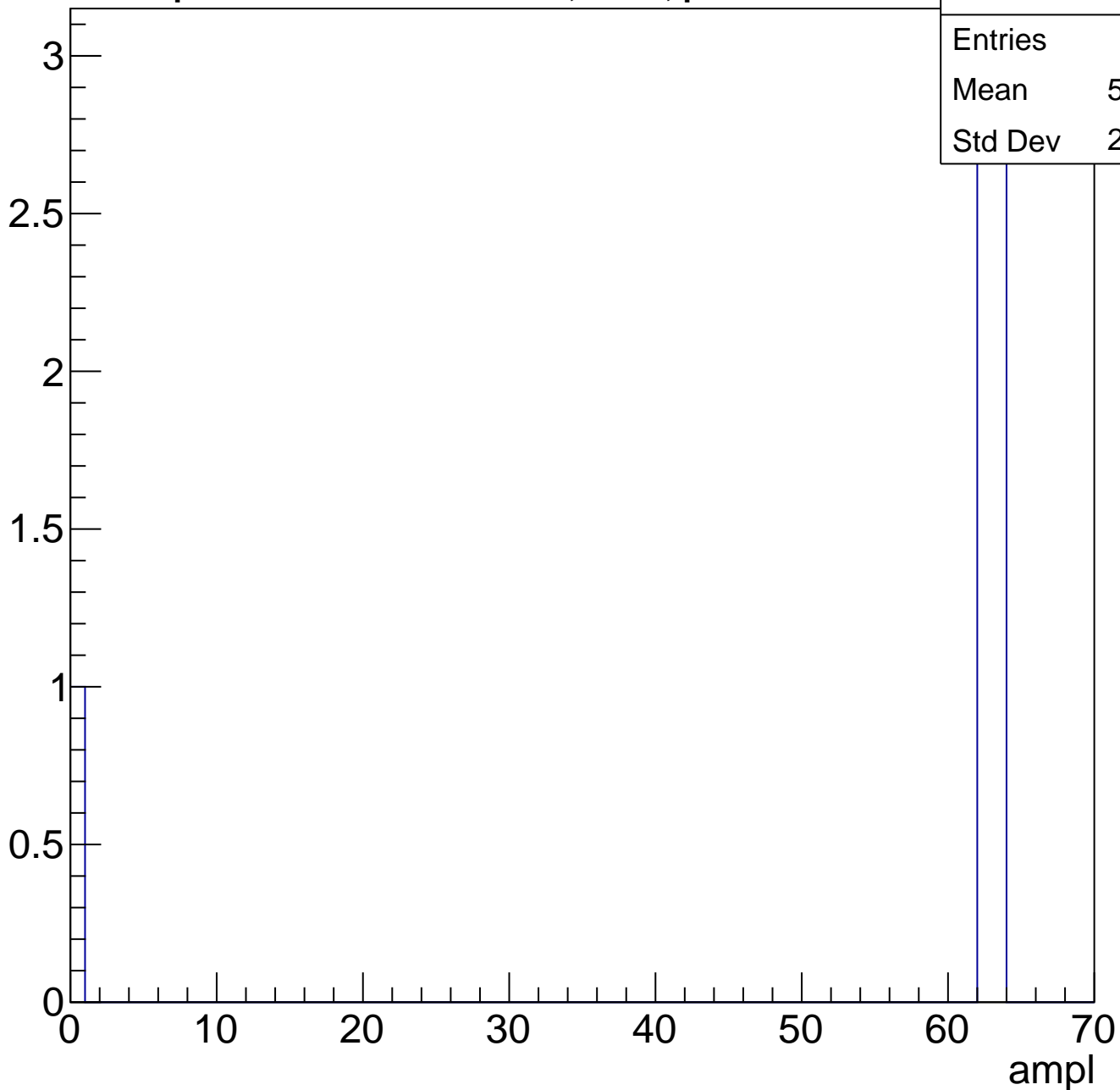
Entry



B1L103S, U12-ch43, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch43, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch44, adc0

calib_packv5_041523_1651.root, FC#0, port C2

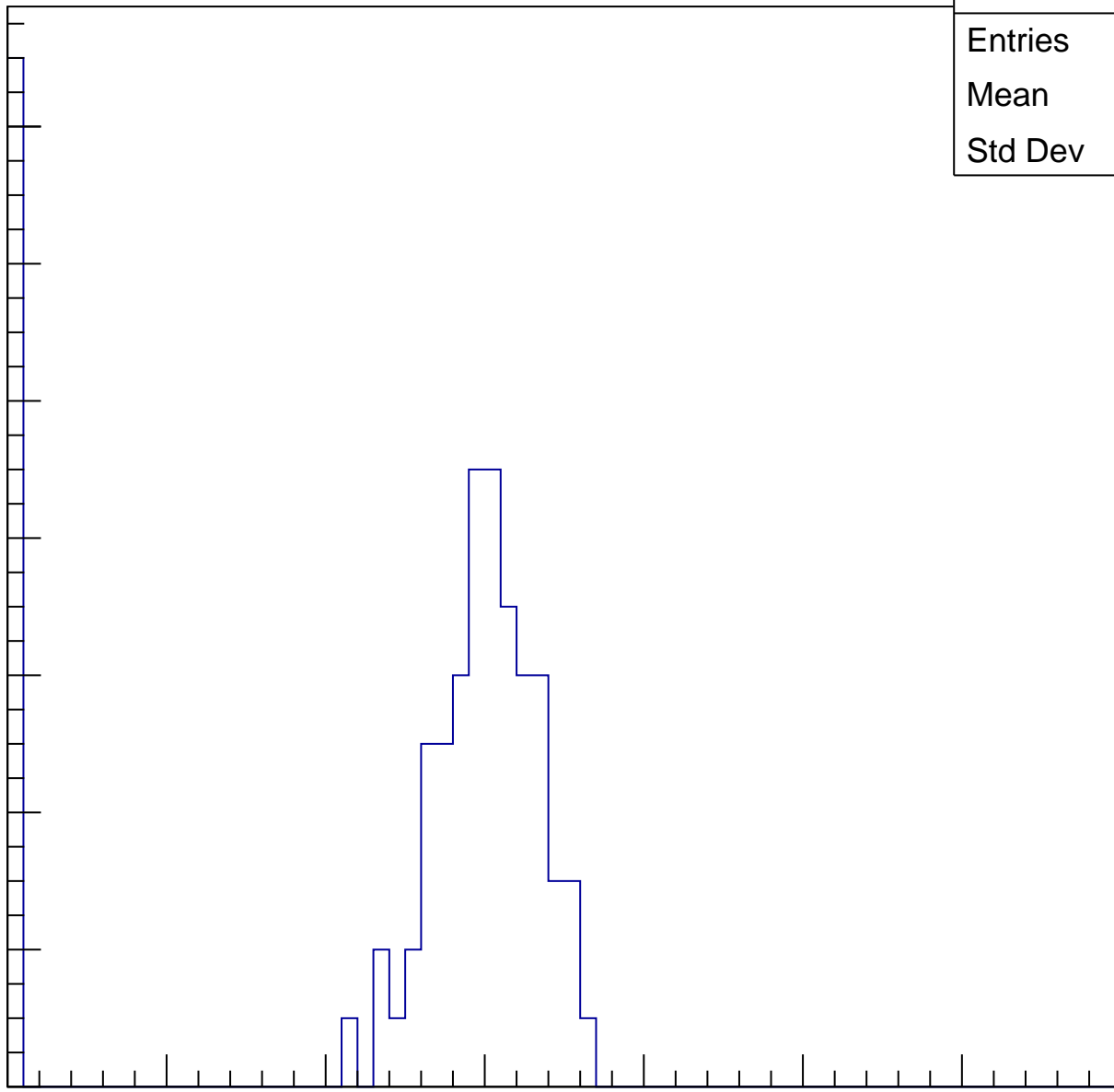
Entries	81
Mean	24.14
Std Dev	11.85

Entry

14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

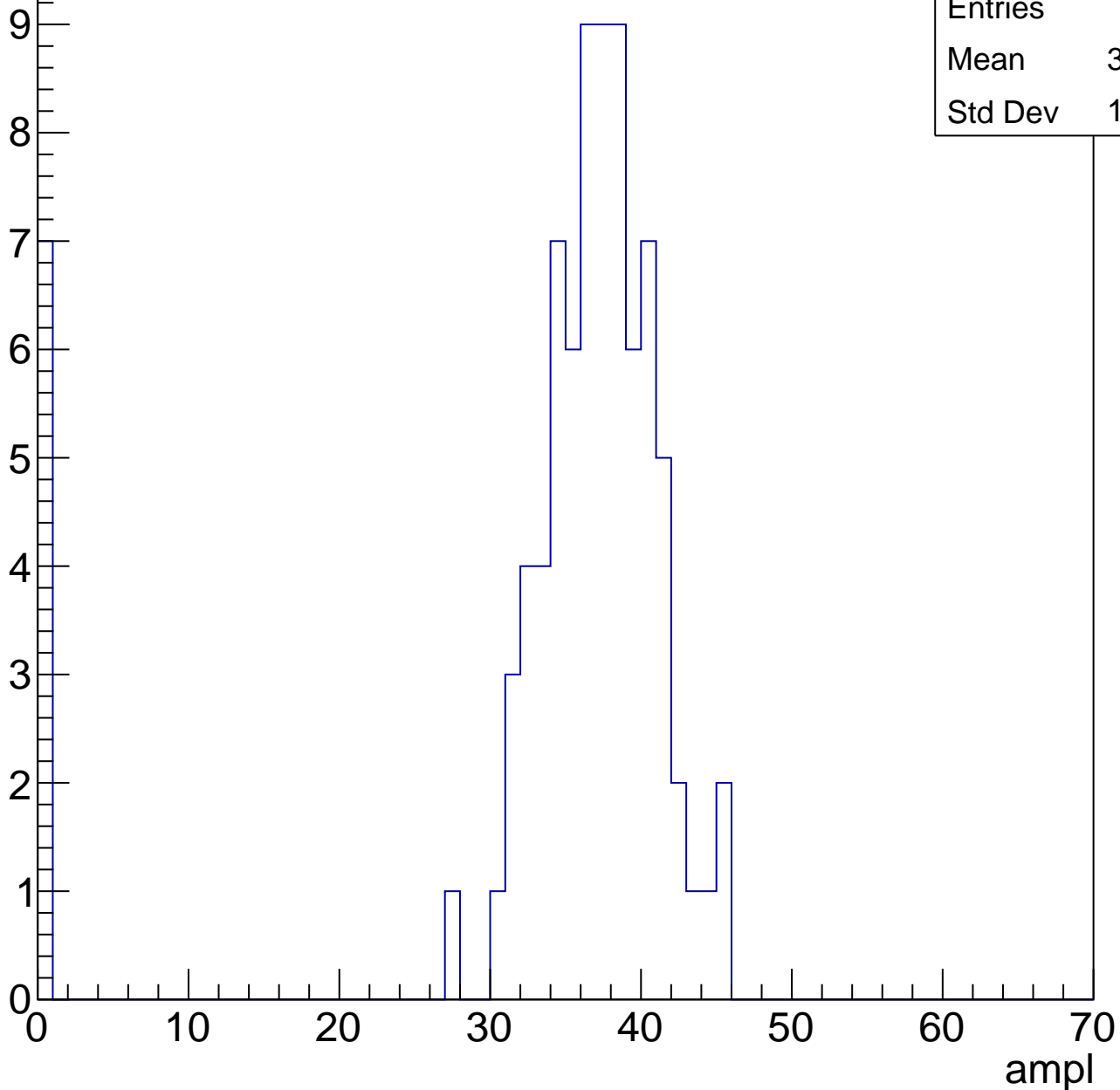


B1L103S, U12-ch44, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	84
Mean	33.77
Std Dev	10.73

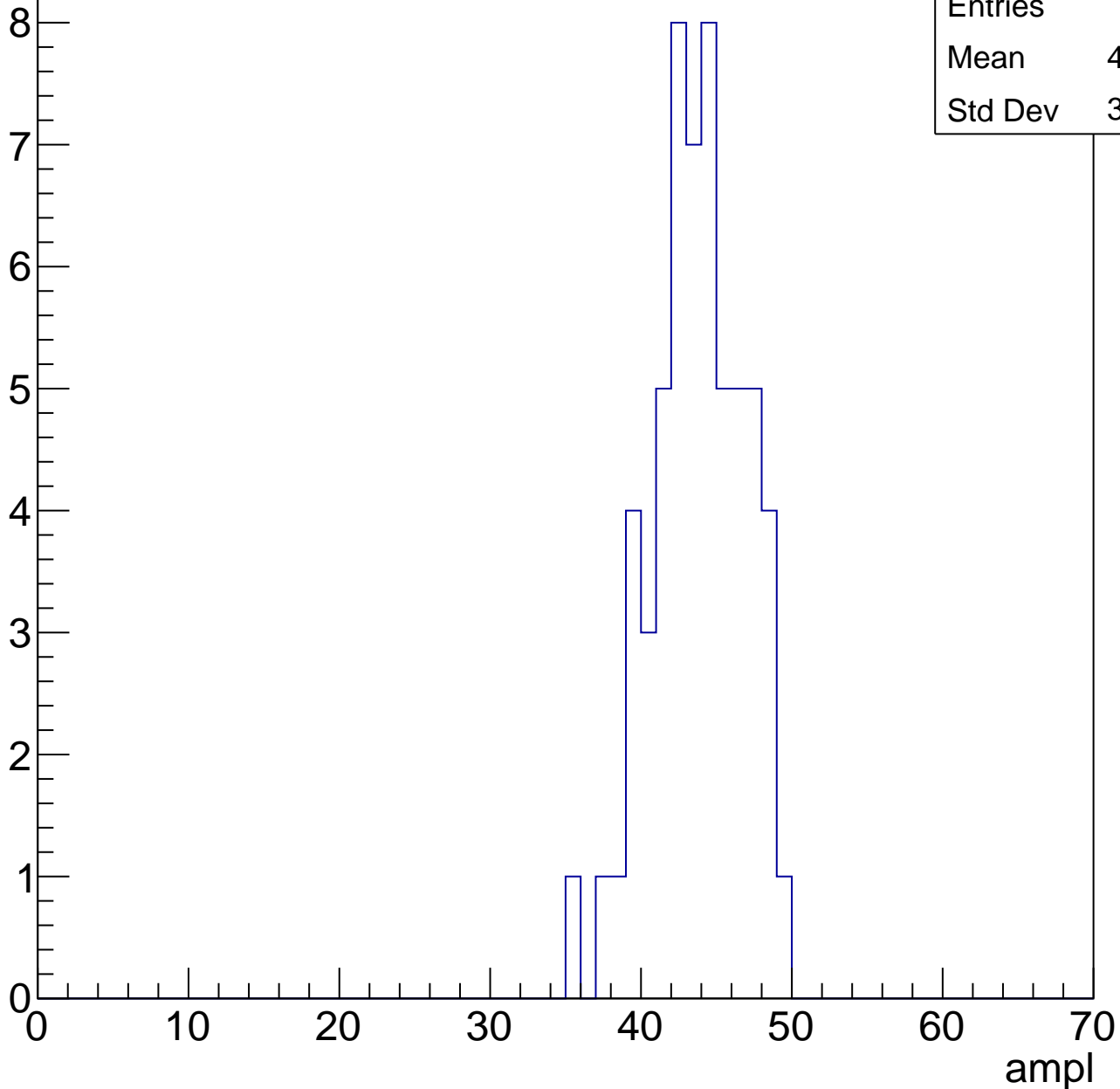


B1L103S, U12-ch44, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	43.29
Std Dev	3.017

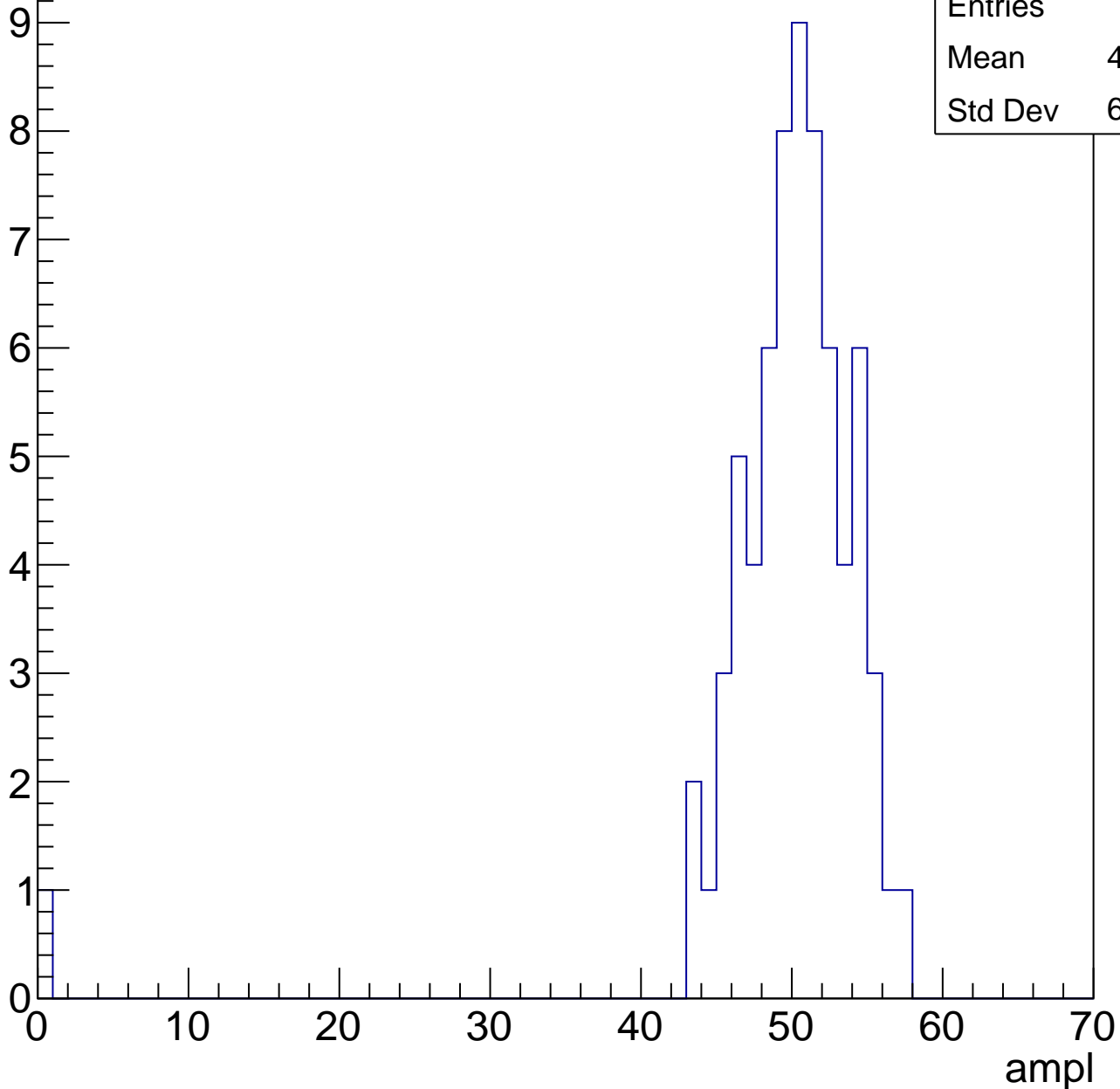


B1L103S, U12-ch44, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	49.22
Std Dev	6.795

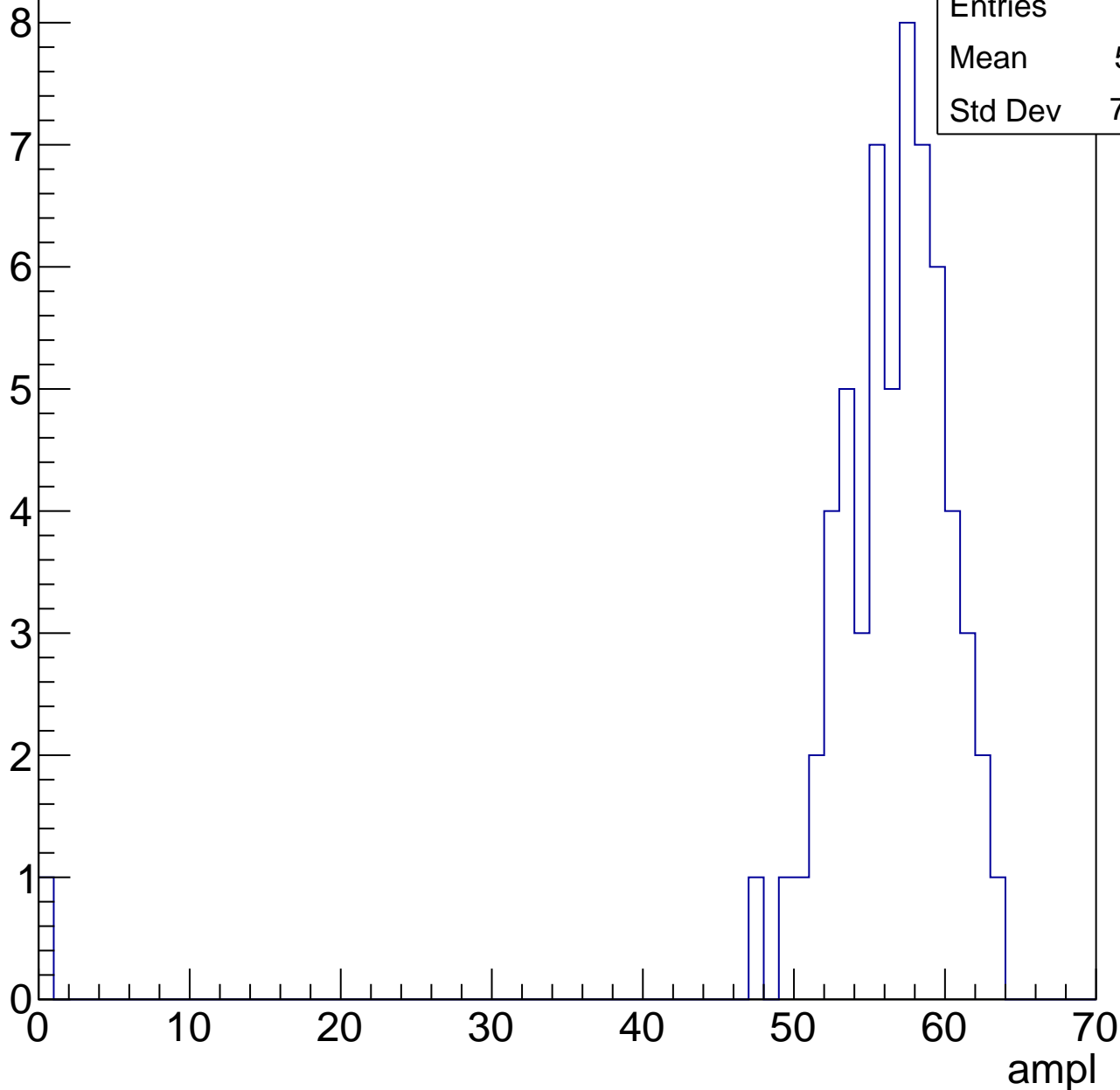


B1L103S, U12-ch44, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	55.31
Std Dev	7.894

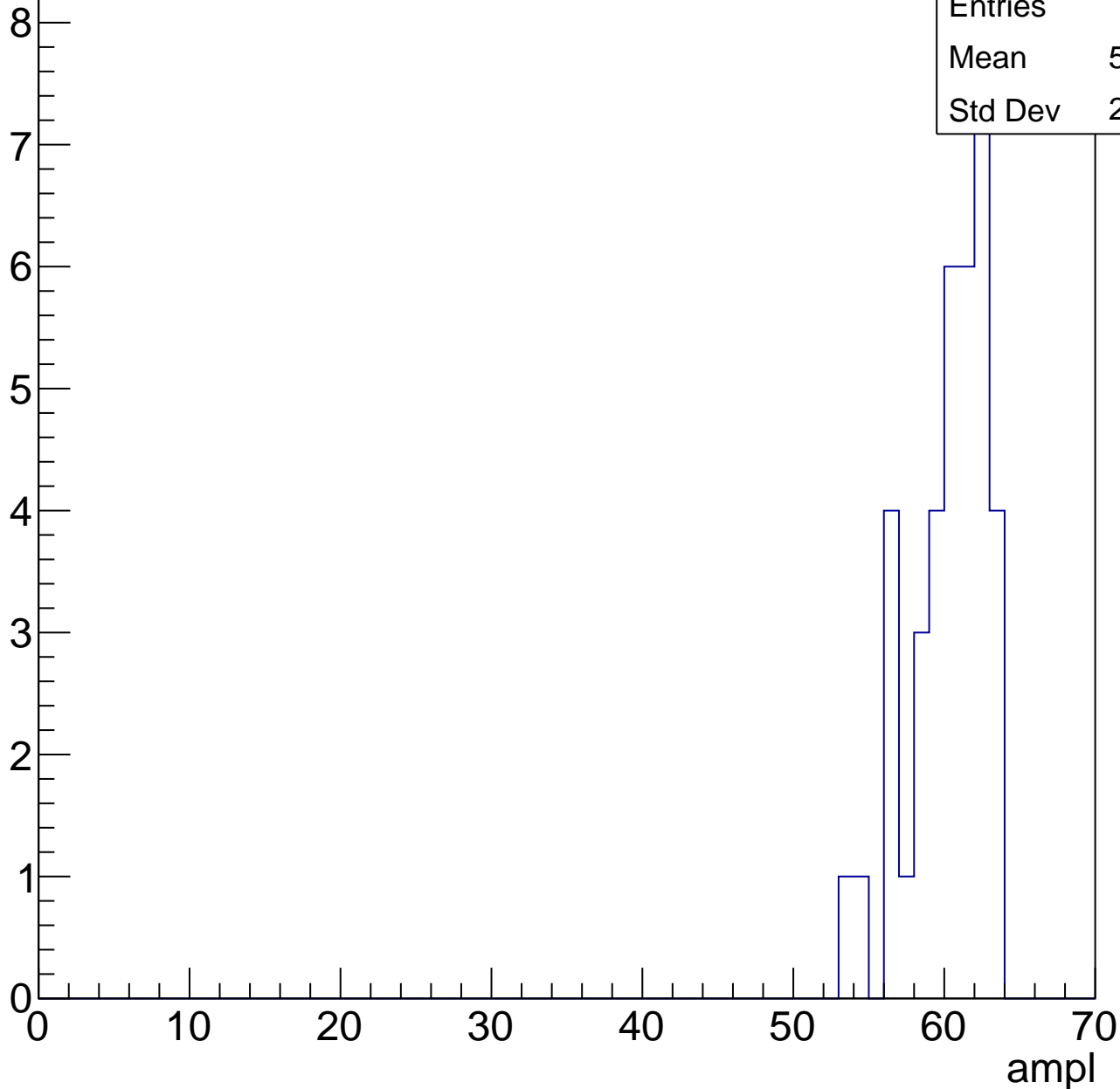


B1L103S, U12-ch44, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	38
Mean	59.79
Std Dev	2.546

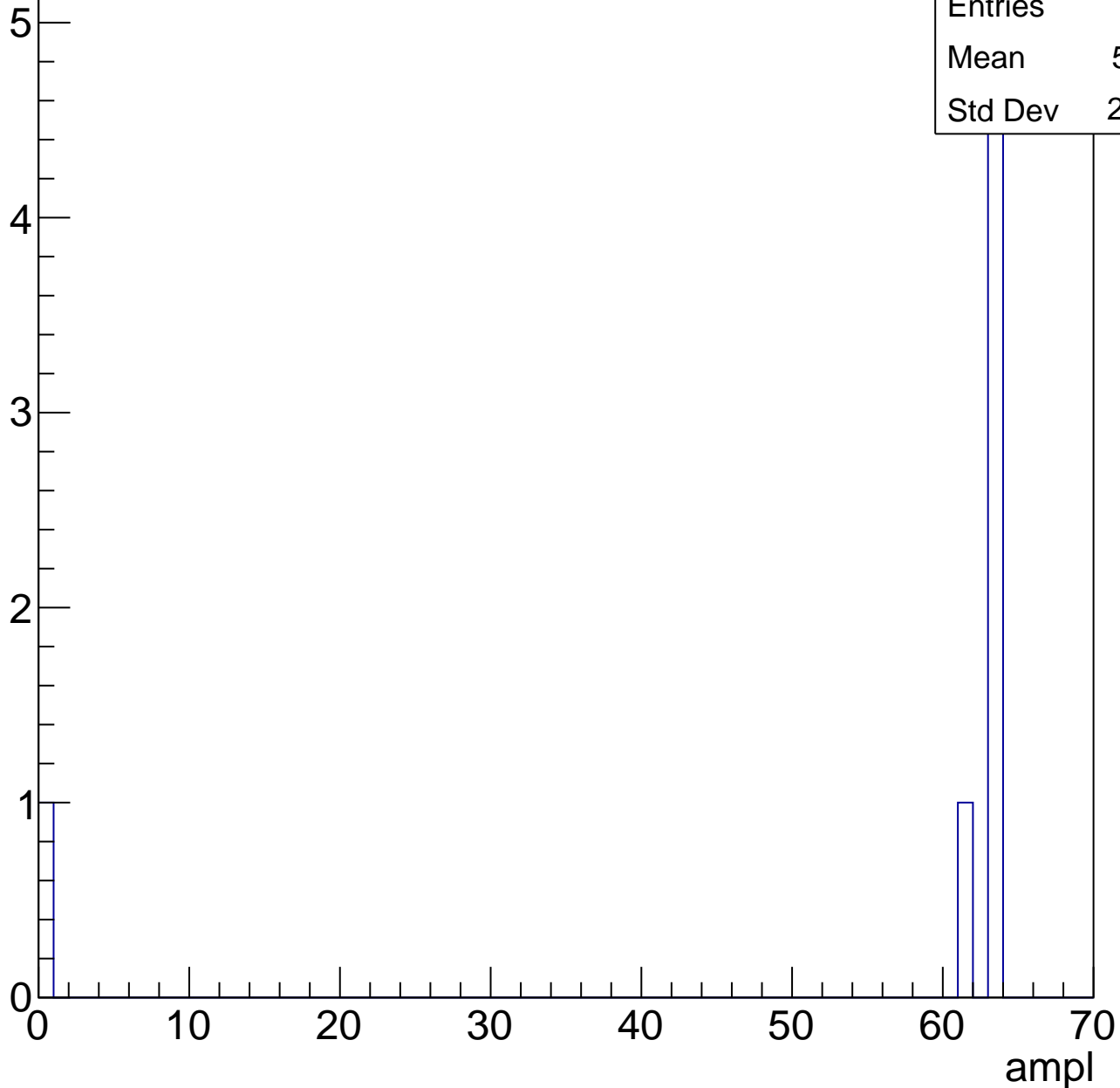


B1L103S, U12-ch44, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	7
Mean	53.71
Std Dev	21.94



B1L103S, U12-ch44, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch45, adc0

calib_packv5_041523_1651.root, FC#0, port C2

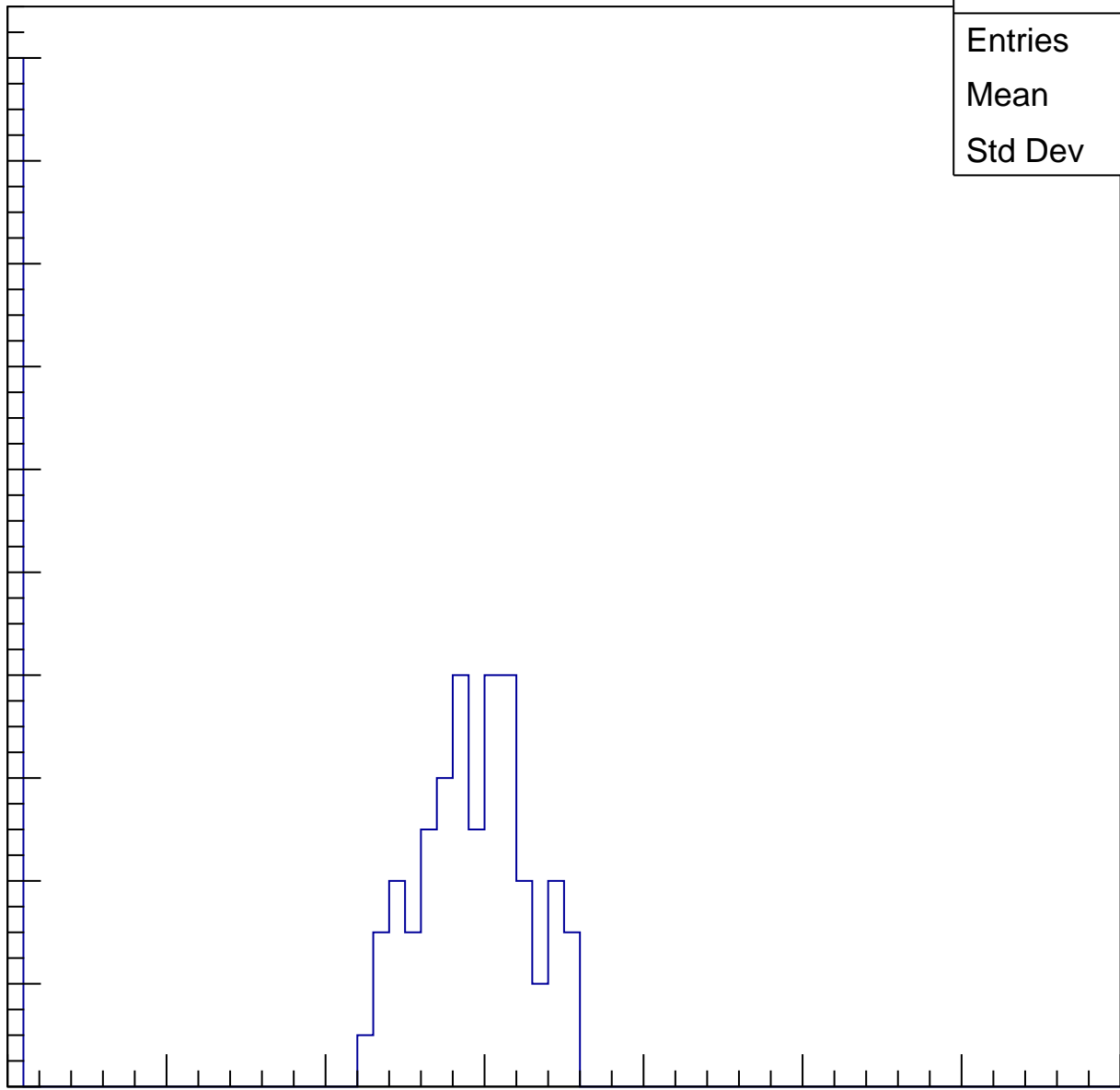
Entries	84
Mean	21.98
Std Dev	12.62

Entry

20
18
16
14
12
10
8
6
4
2
0

ampl

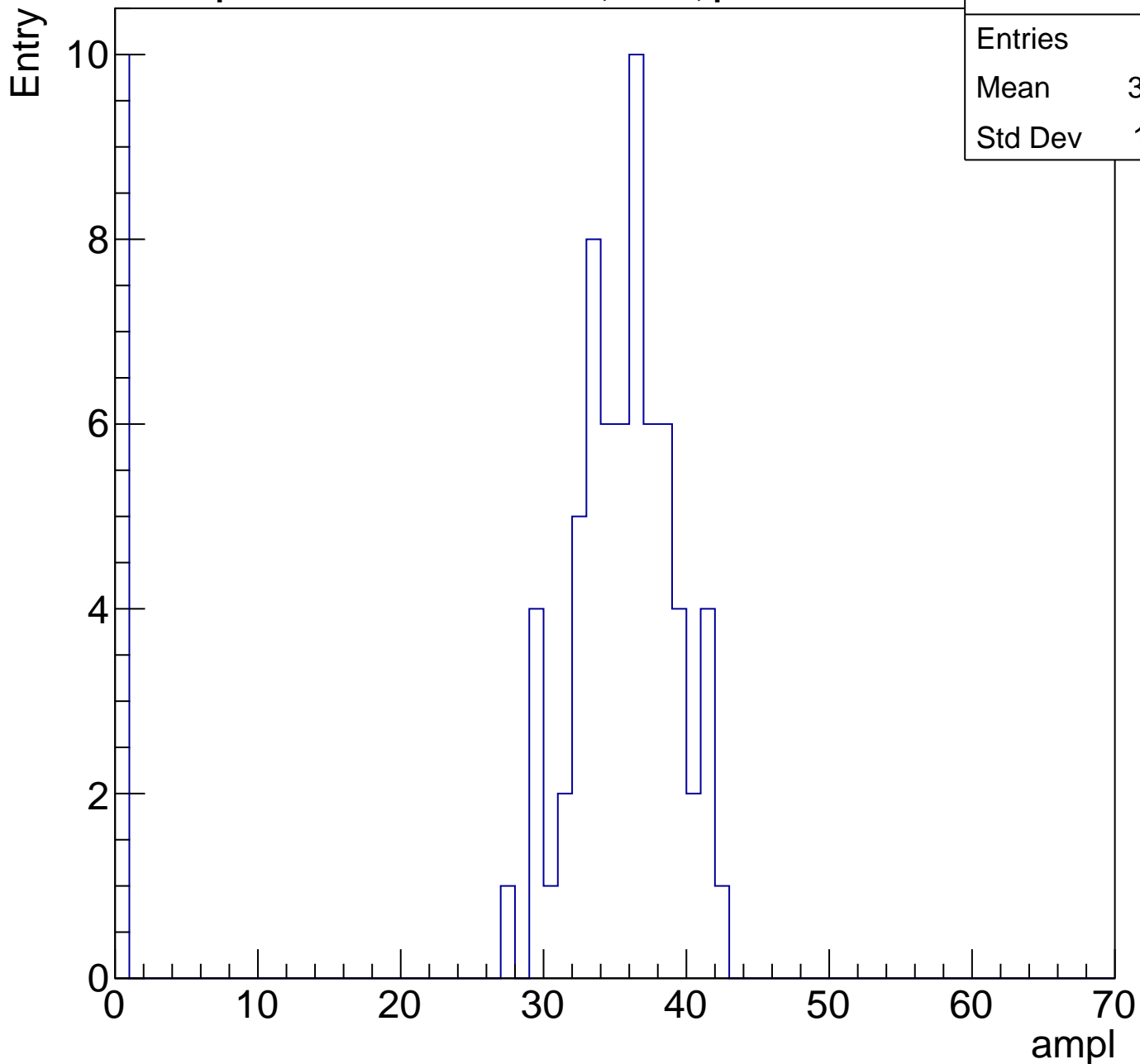
0 10 20 30 40 50 60 70



B1L103S, U12-ch45, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	76
Mean	30.59
Std Dev	12.31

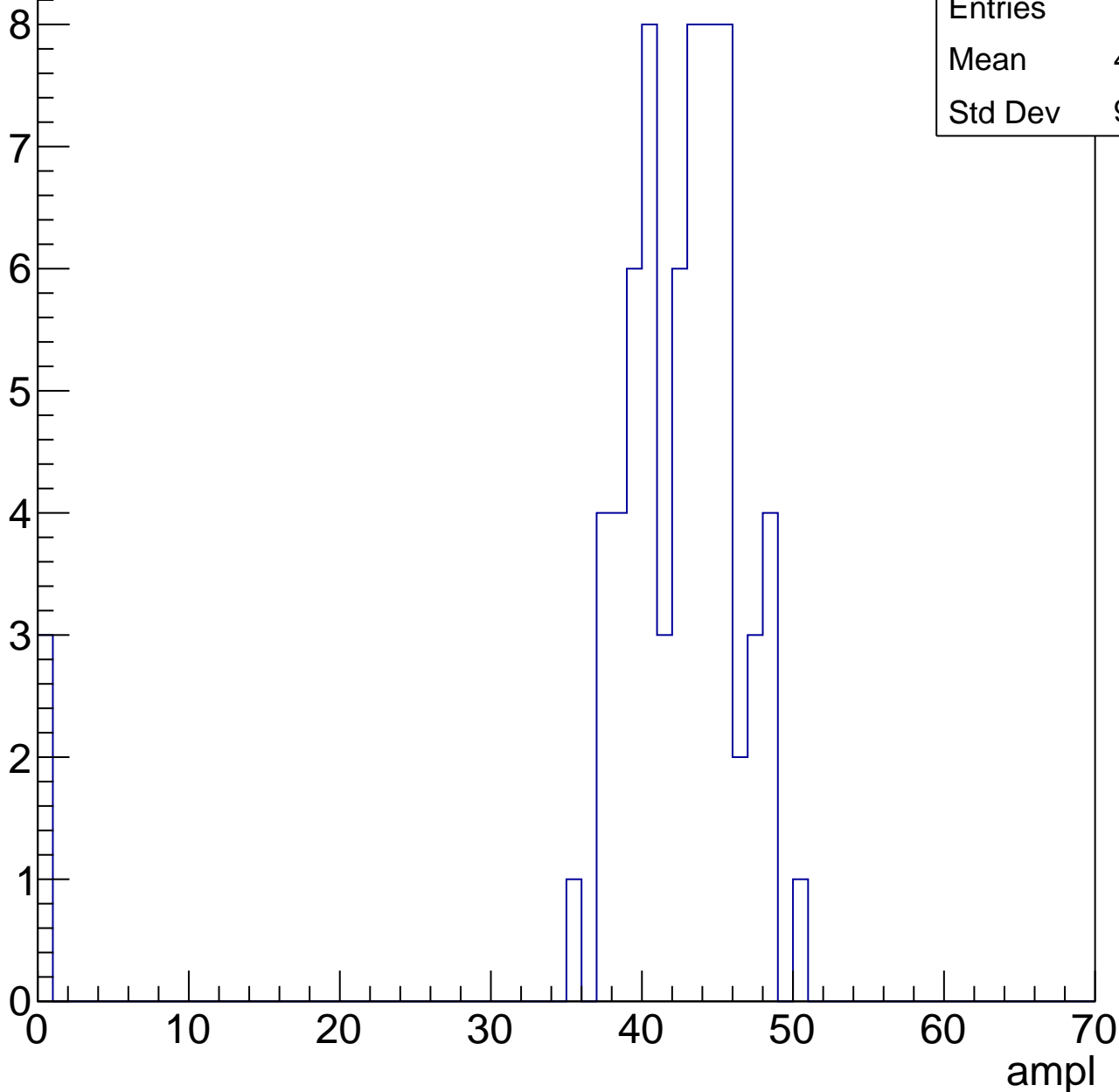


B1L103S, U12-ch45, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	40.51
Std Dev	9.221

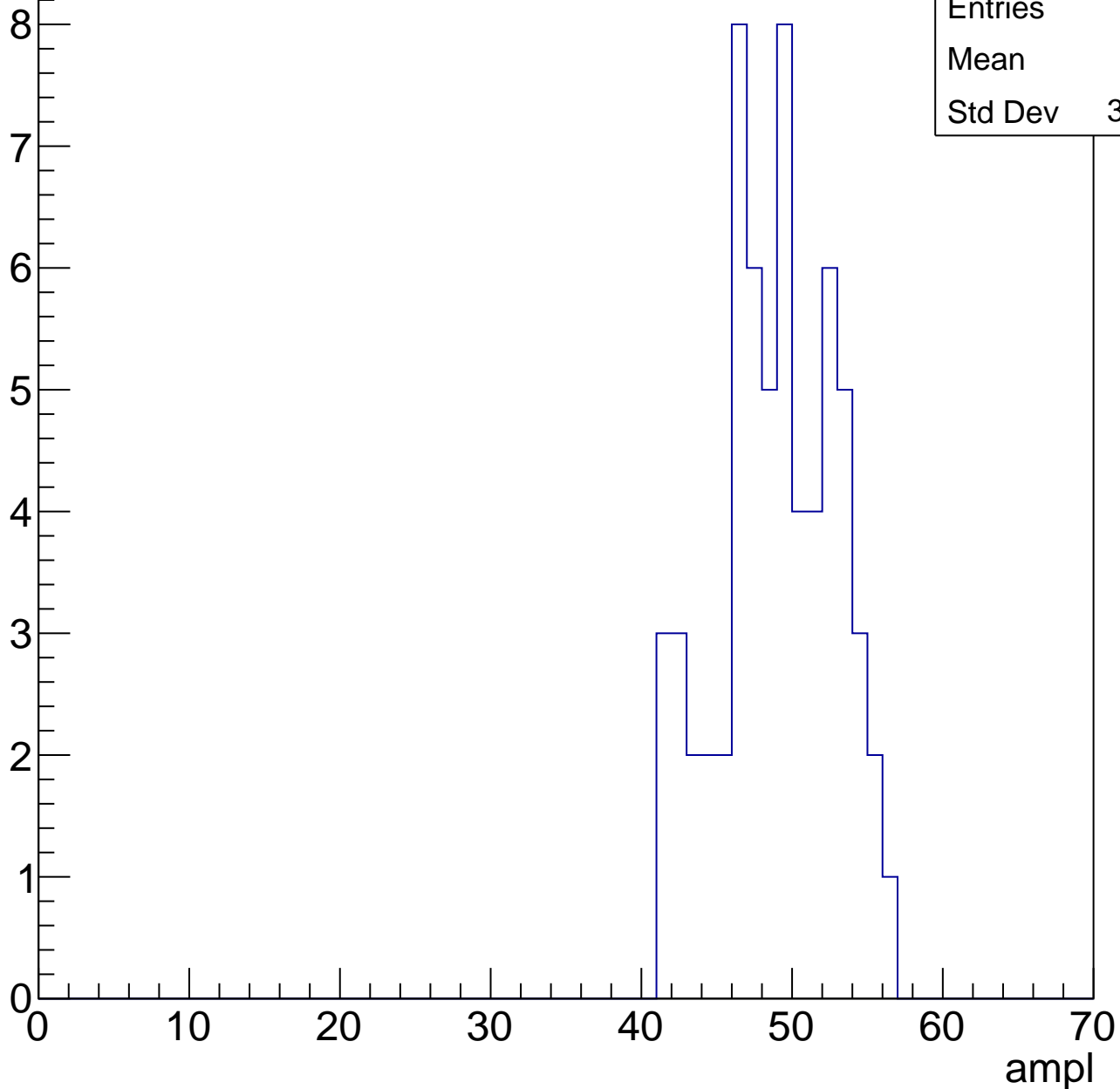


B1L103S, U12-ch45, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	48.5
Std Dev	3.808

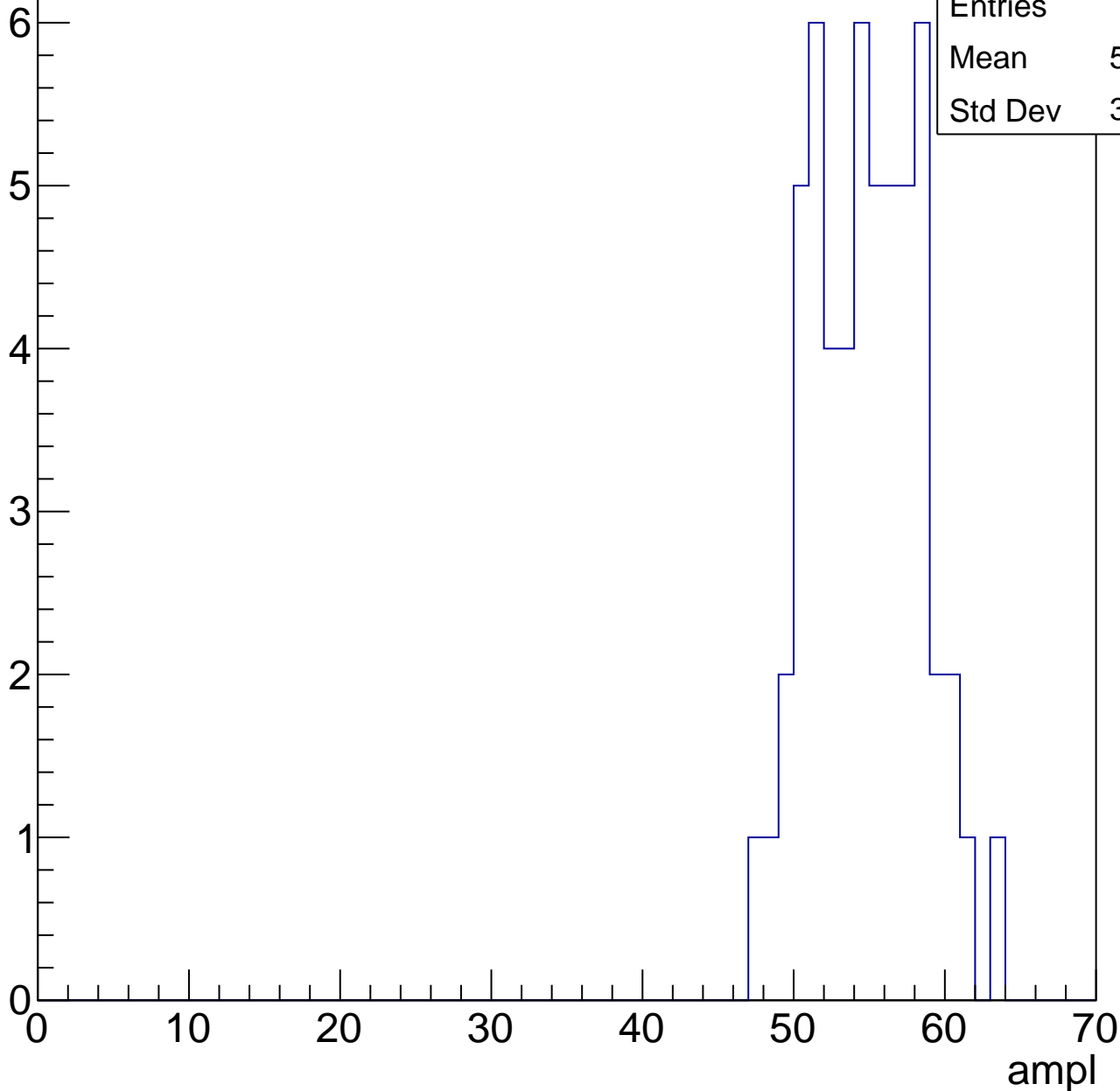


B1L103S, U12-ch45, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

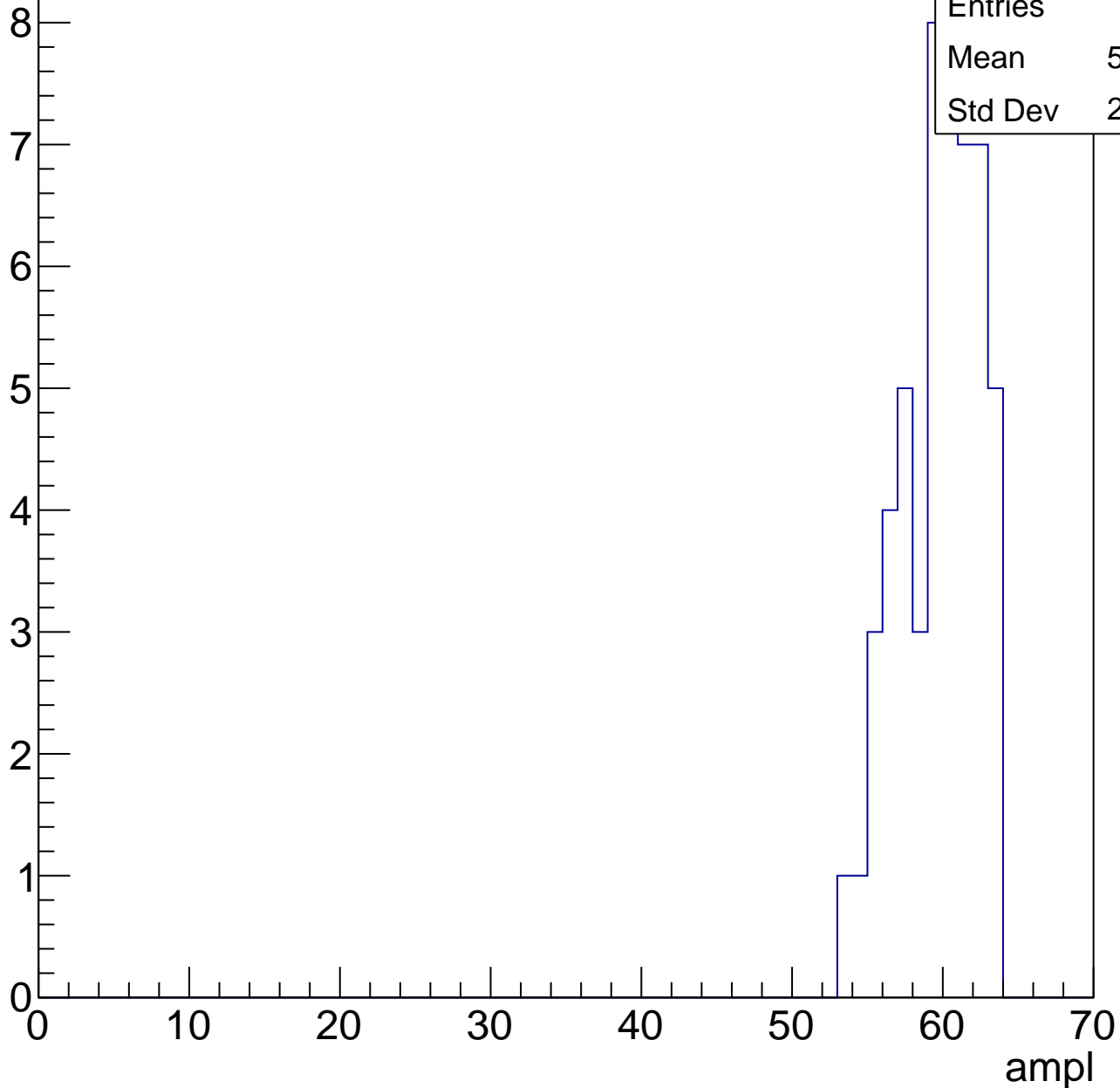
Entries	56
Mean	54.34
Std Dev	3.537



B1L103S, U12-ch45, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

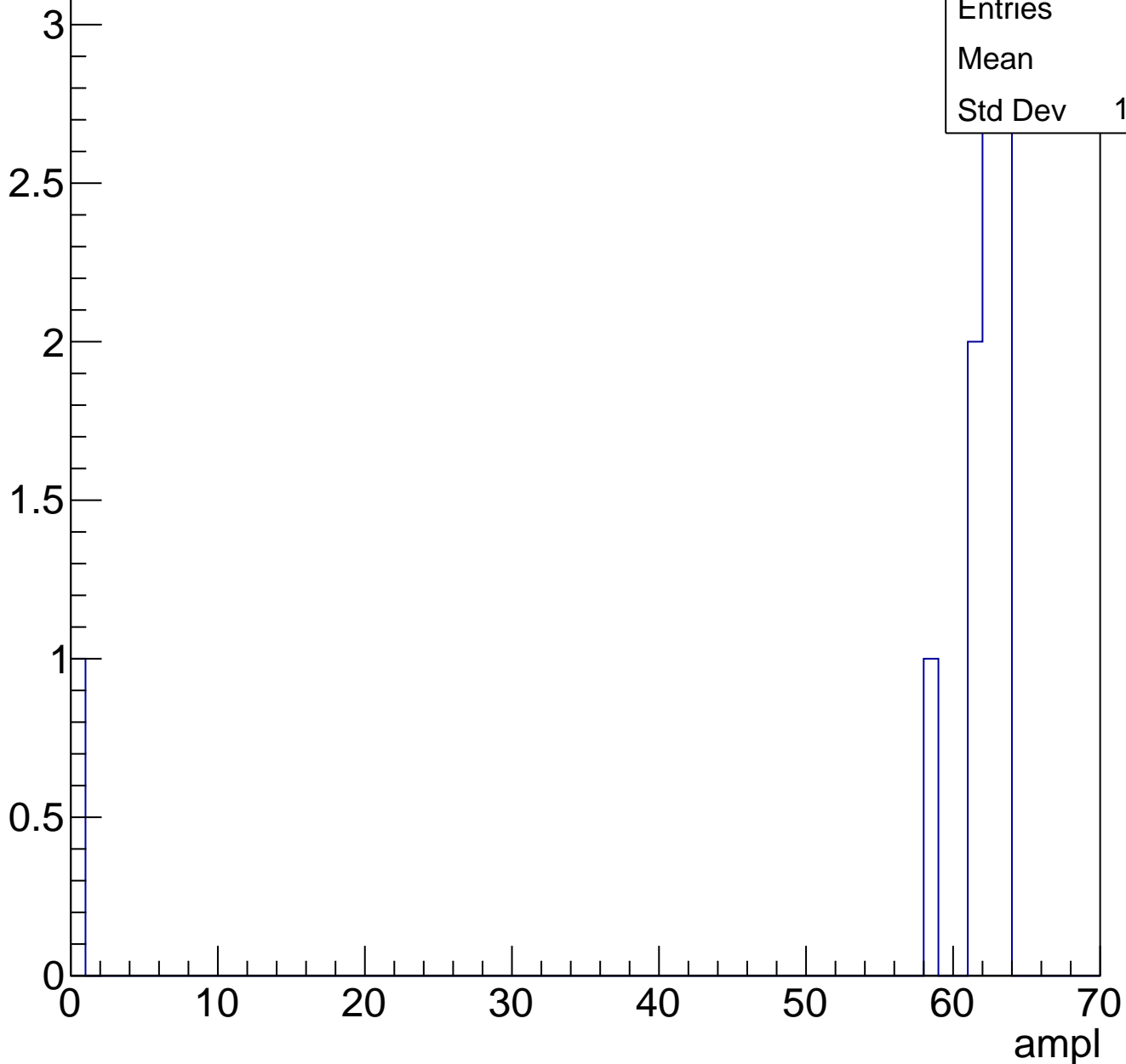


Entries	52
Mean	59.29
Std Dev	2.567

B1L103S, U12-ch45, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch45, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.15
Std Dev	13.73

Entry

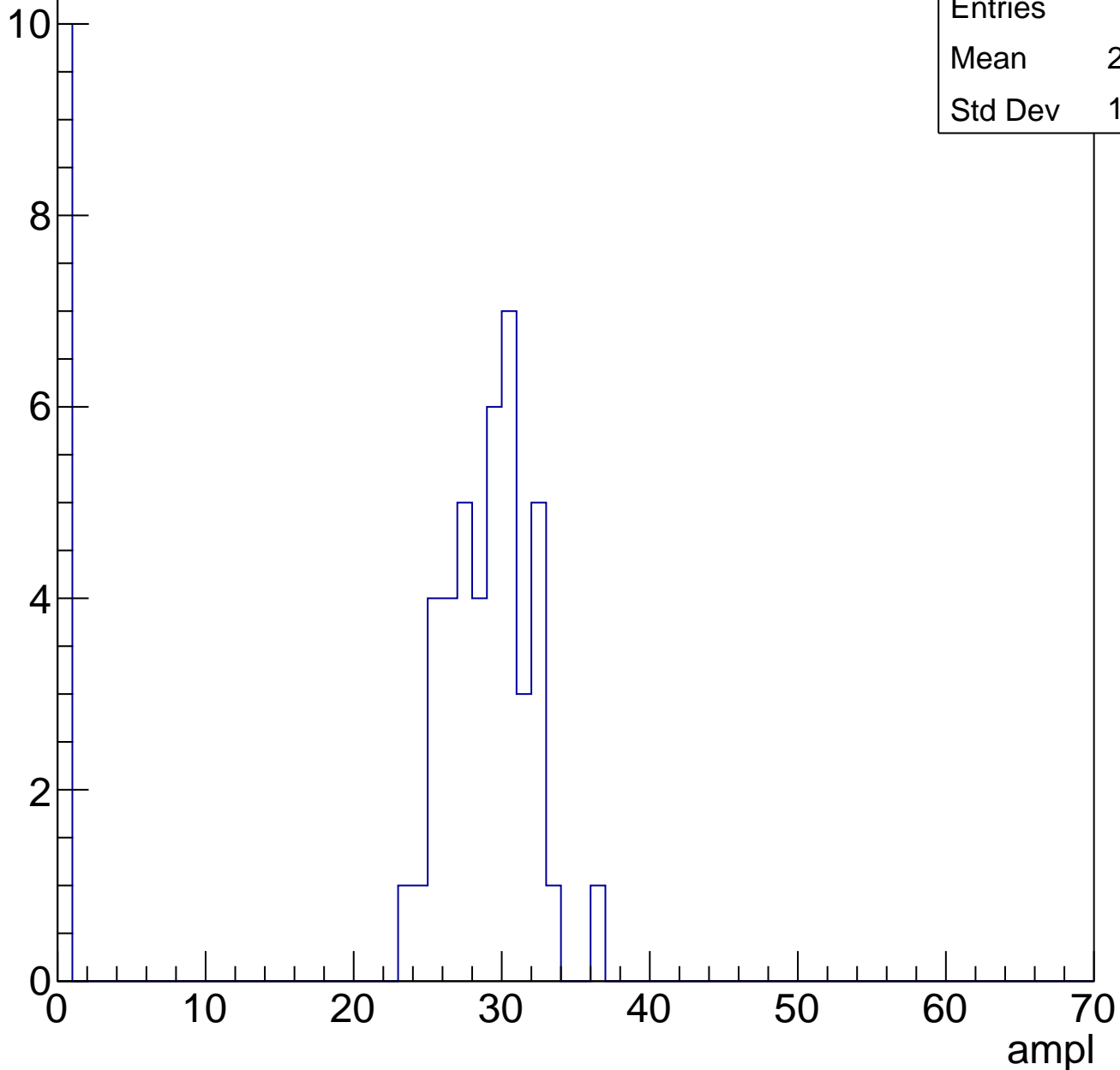


B1L103S, U12-ch46, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	52
Mean	23.15
Std Dev	11.56

Entry

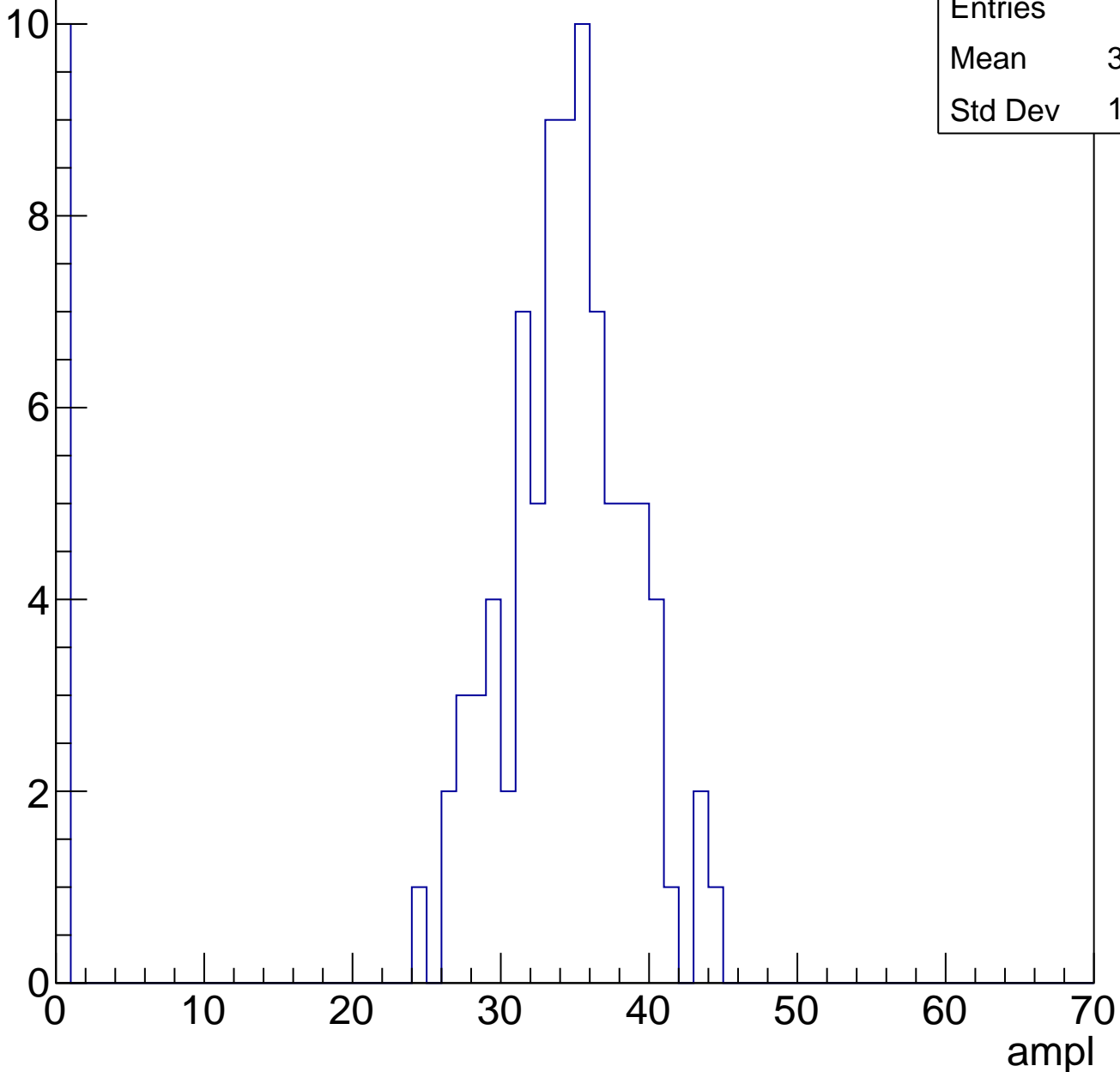


B1L103S, U12-ch46, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	95
Mean	30.53
Std Dev	11.18

Entry

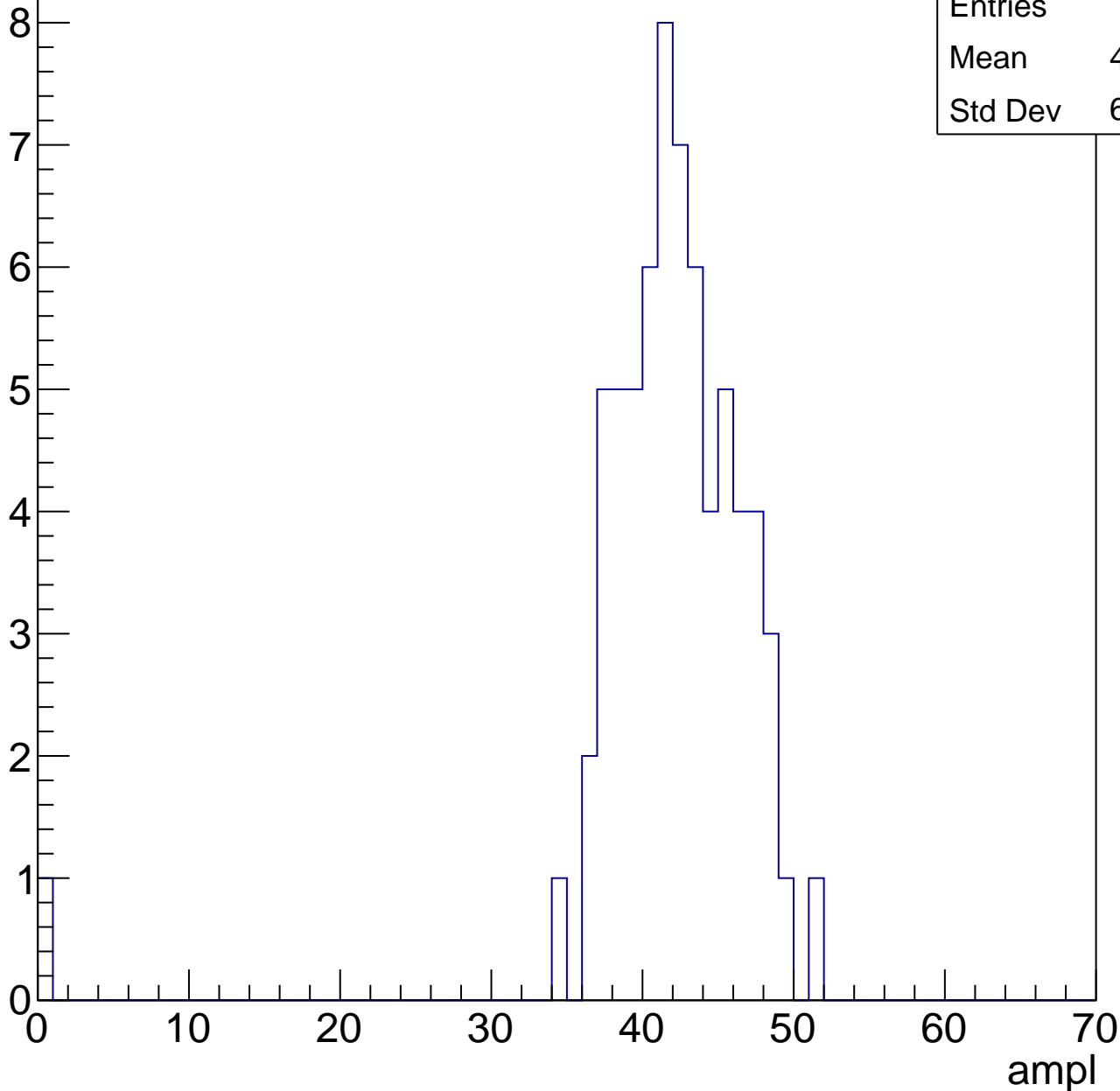


B1L103S, U12-ch46, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	41.37
Std Dev	6.212

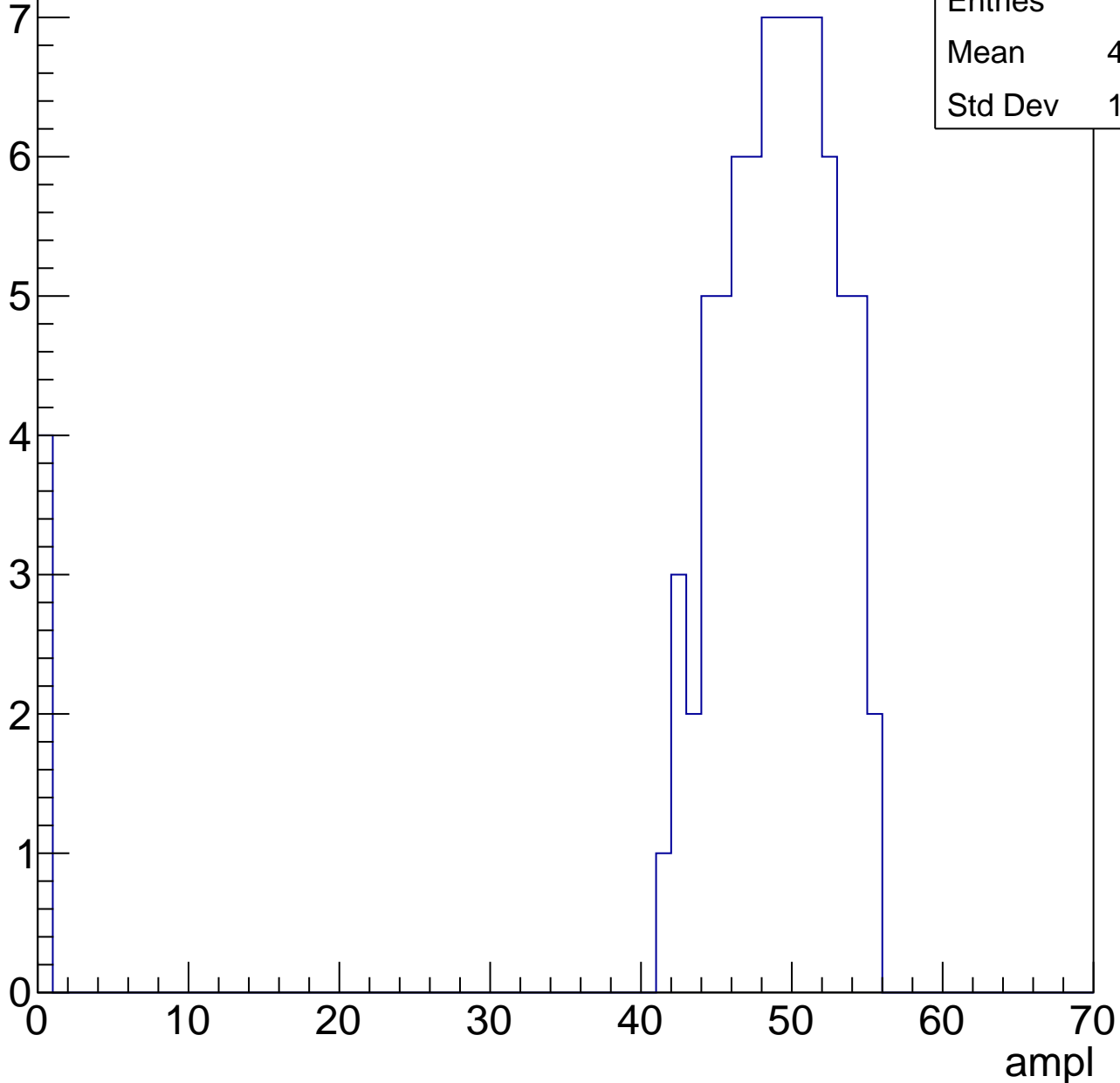


B1L103S, U12-ch46, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	78
Mean	46.14
Std Dev	11.27

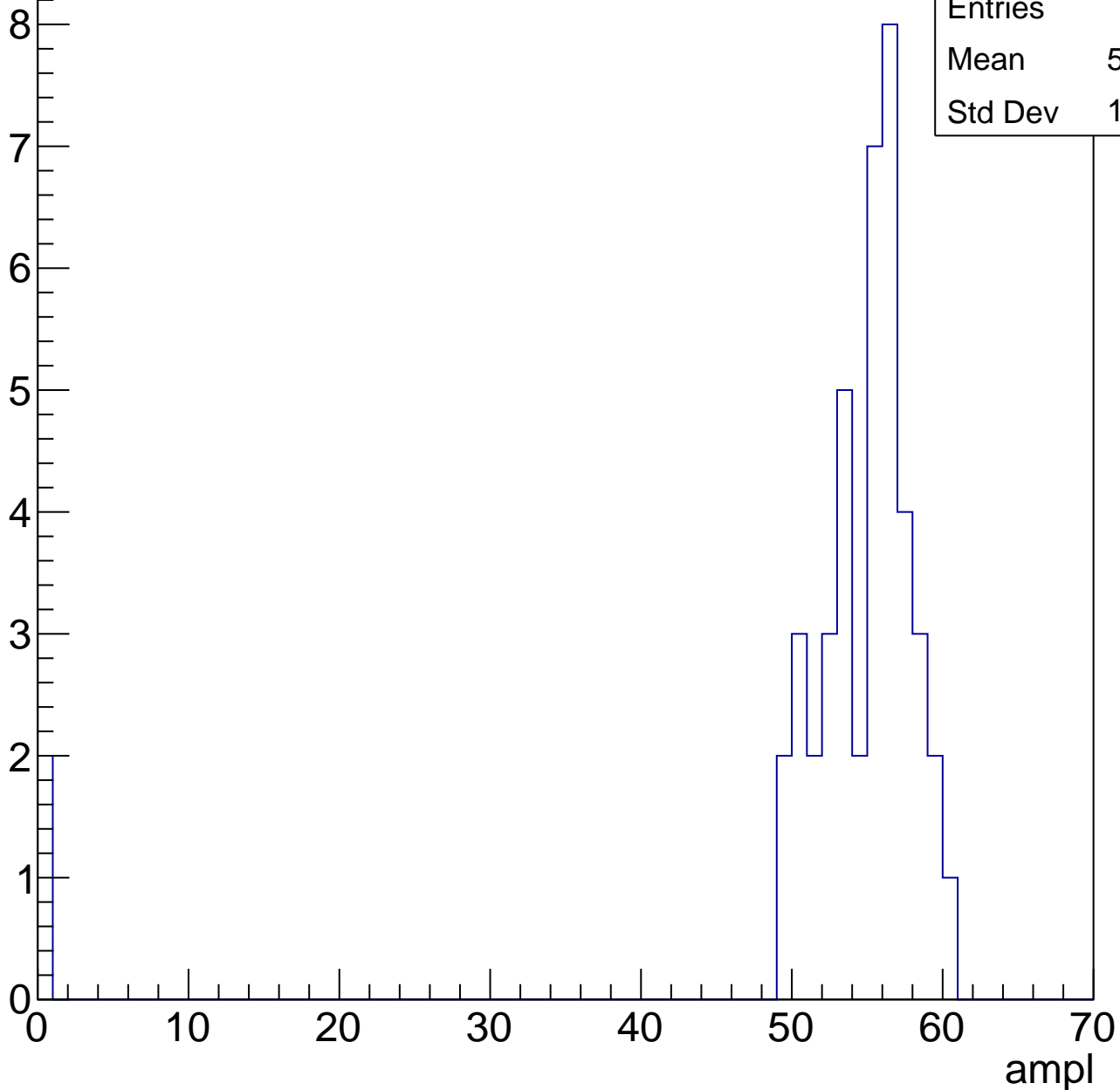


B1L103S, U12-ch46, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	44
Mean	52.09
Std Dev	11.69

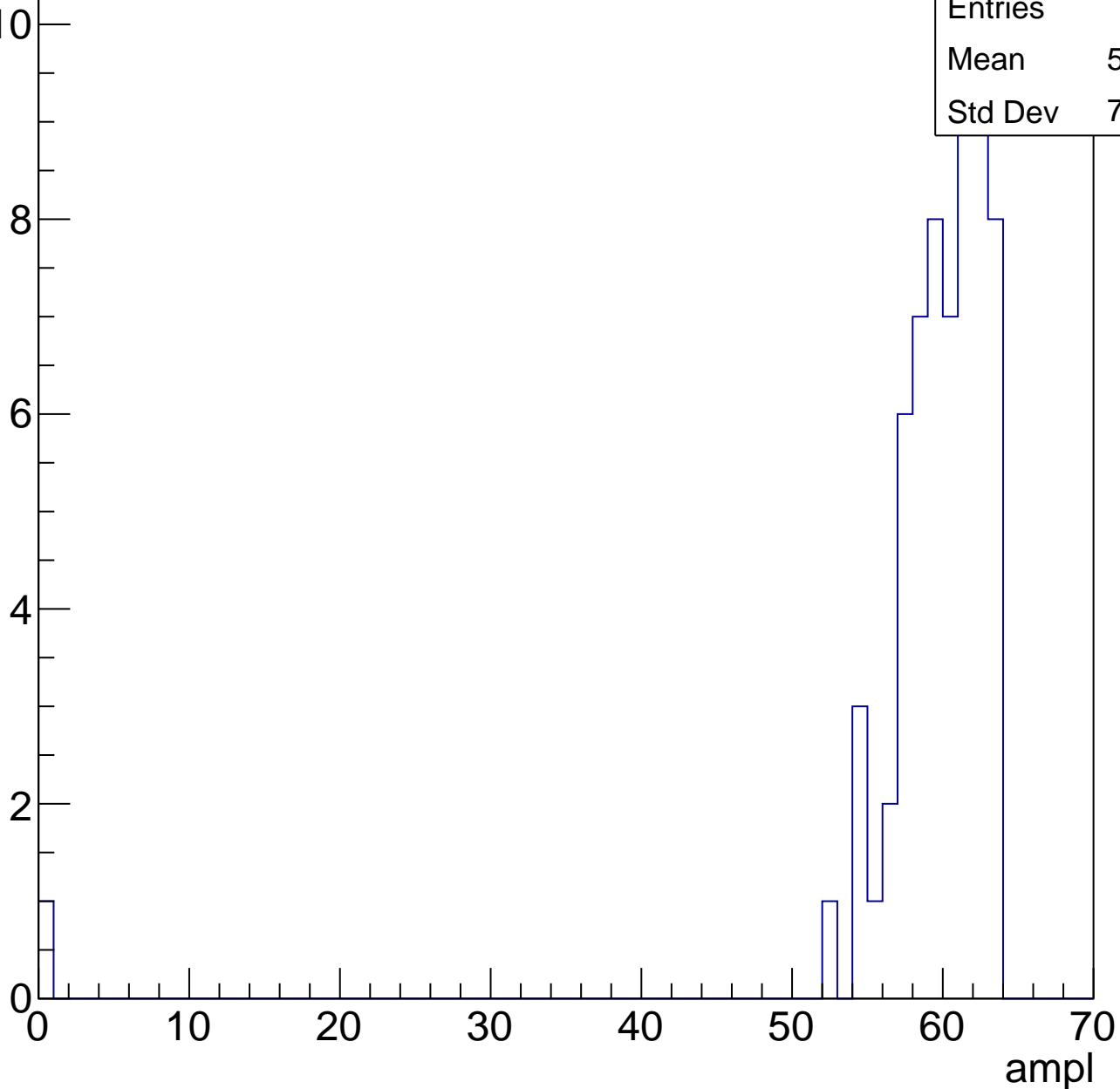


B1L103S, U12-ch46, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	63
Mean	58.62
Std Dev	7.885



B1L103S, U12-ch46, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	5
Mean	61.6
Std Dev	1.356

ampl

0 10 20 30 40 50 60 70

B1L103S, U12-ch46, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.211
Std Dev	5.136

Entry

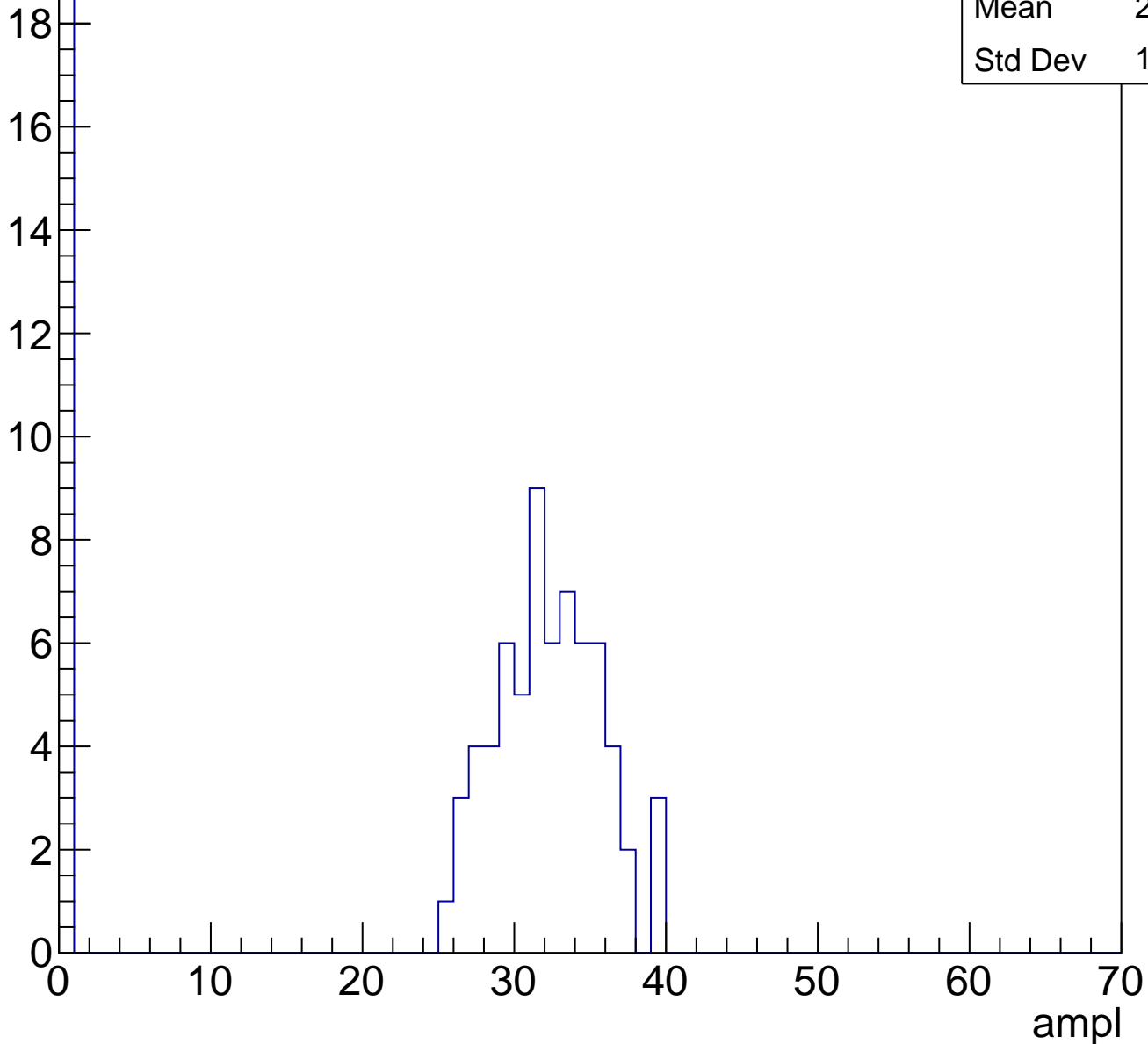


B1L103S, U12-ch47, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	85
Mean	24.68
Std Dev	13.57

Entry



B1L103S, U12-ch47, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	63
Mean	30.6
Std Dev	14.51

Entry

10

8

6

4

2

0

0

10

20

30

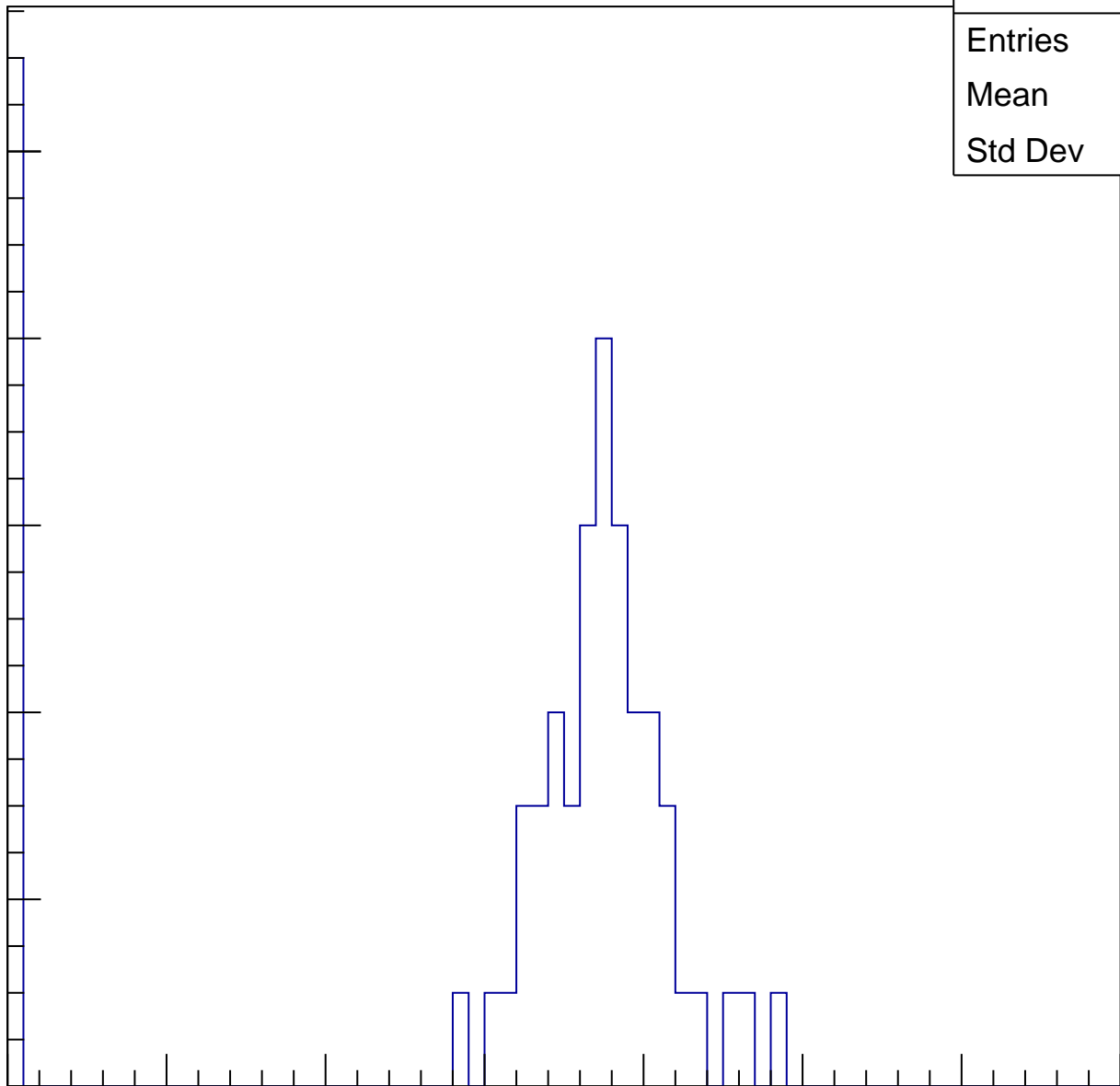
40

50

60

70

ampl

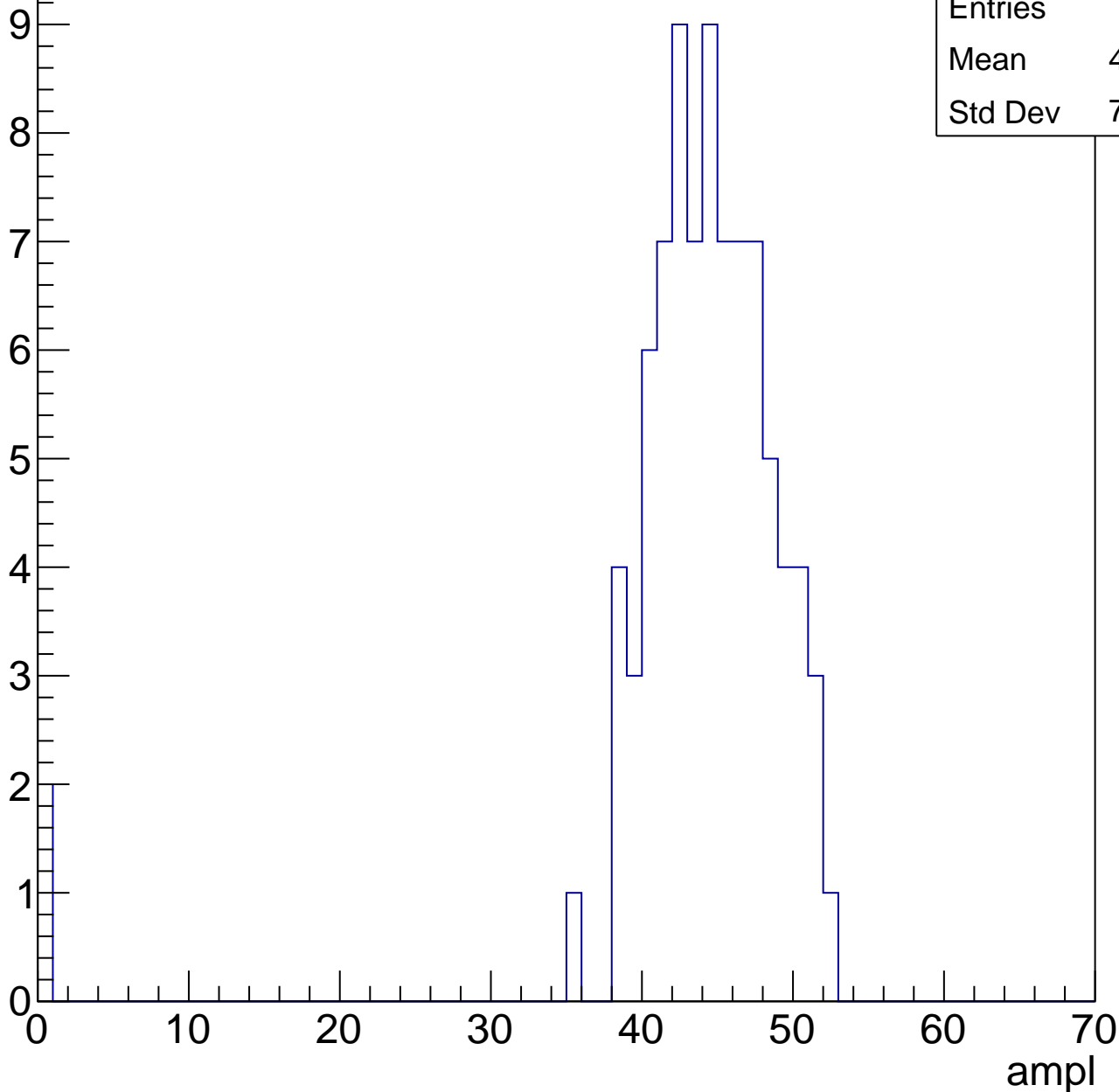


B1L103S, U12-ch47, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	86
Mean	43.17
Std Dev	7.585

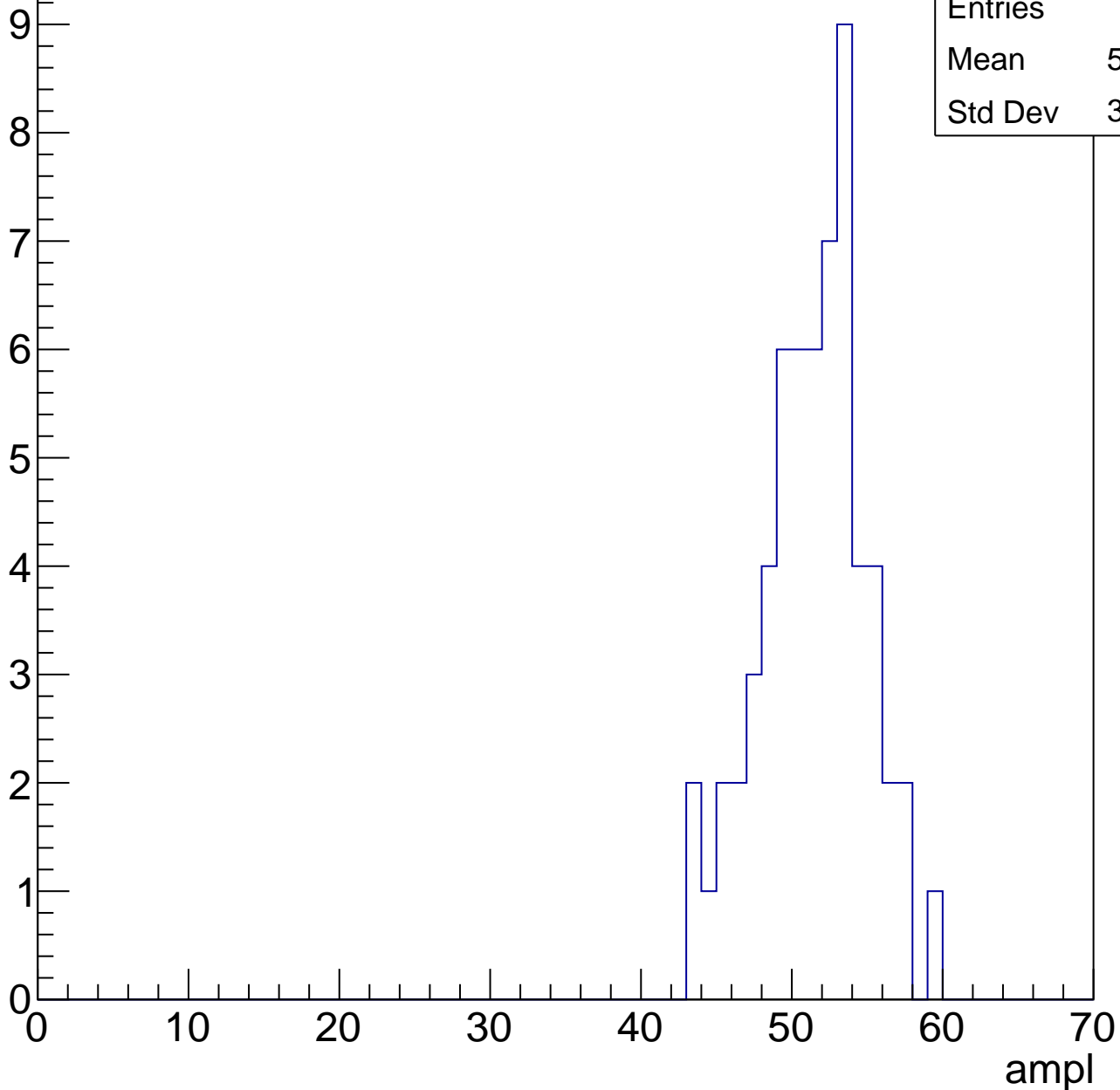


B1L103S, U12-ch47, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	50.93
Std Dev	3.487

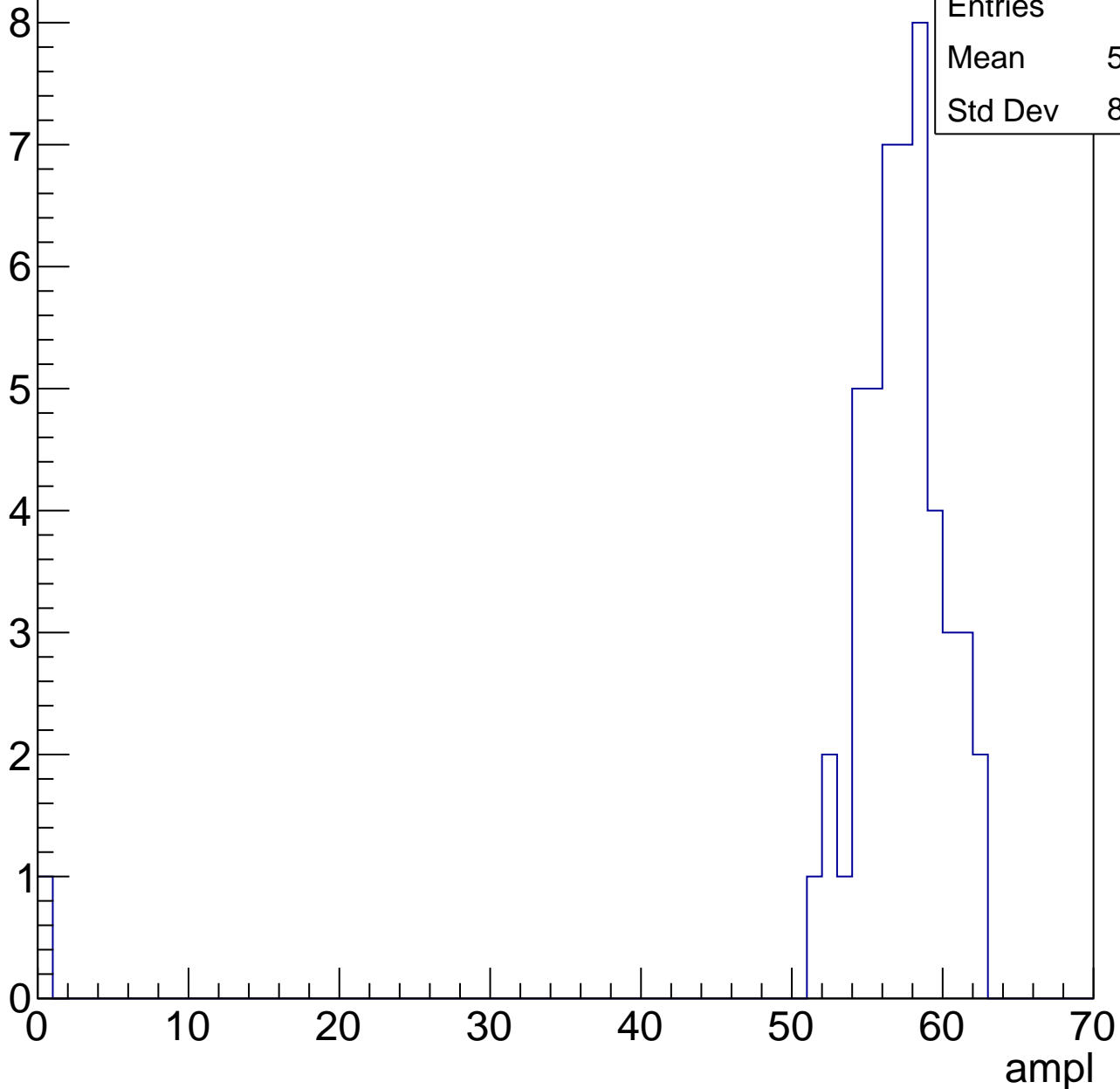


B1L103S, U12-ch47, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	49
Mean	55.73
Std Dev	8.444



B1L103S, U12-ch47, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

9
8
7
6
5
4
3
2
1
0

Entries	42
Mean	59.12
Std Dev	9.495

ampl

0

10

20

30

40

50

60

70

B1L103S, U12-ch47, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch47, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U12-ch48, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	93
Mean	26.8
Std Dev	8.979

Entry

10
8
6
4
2
0

0

10

20

30

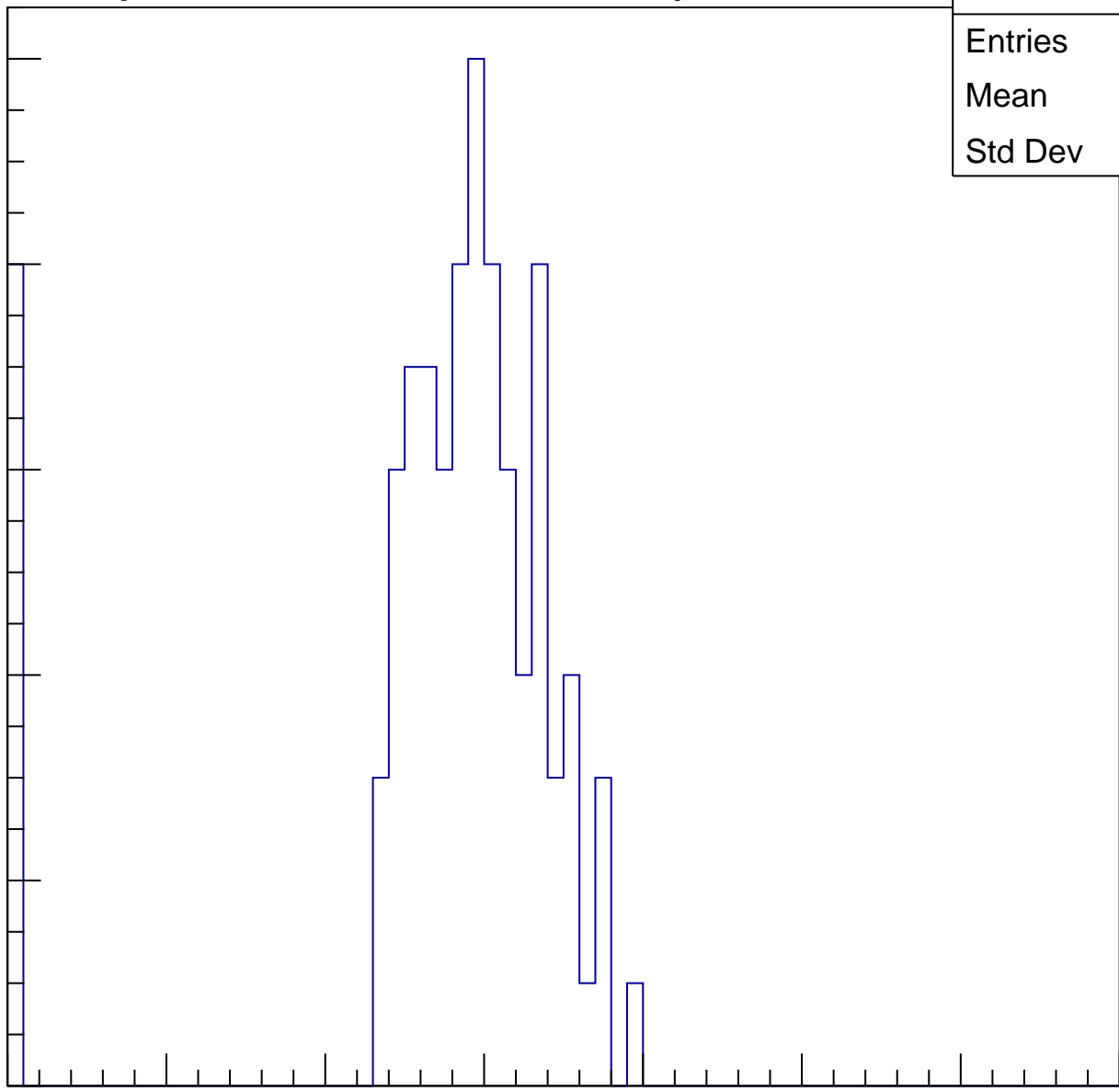
40

50

60

70

ampl

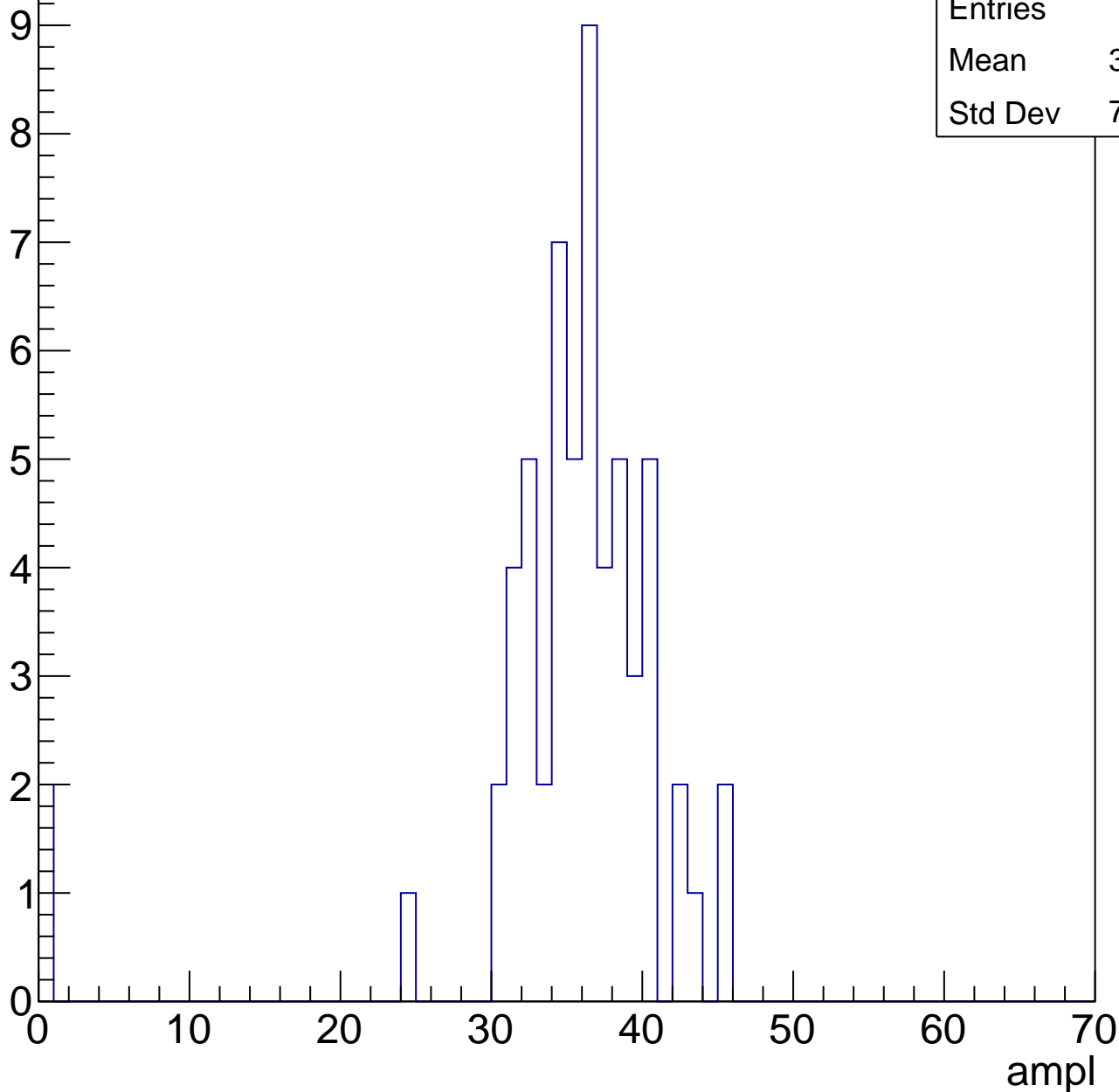


B1L103S, U12-ch48, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

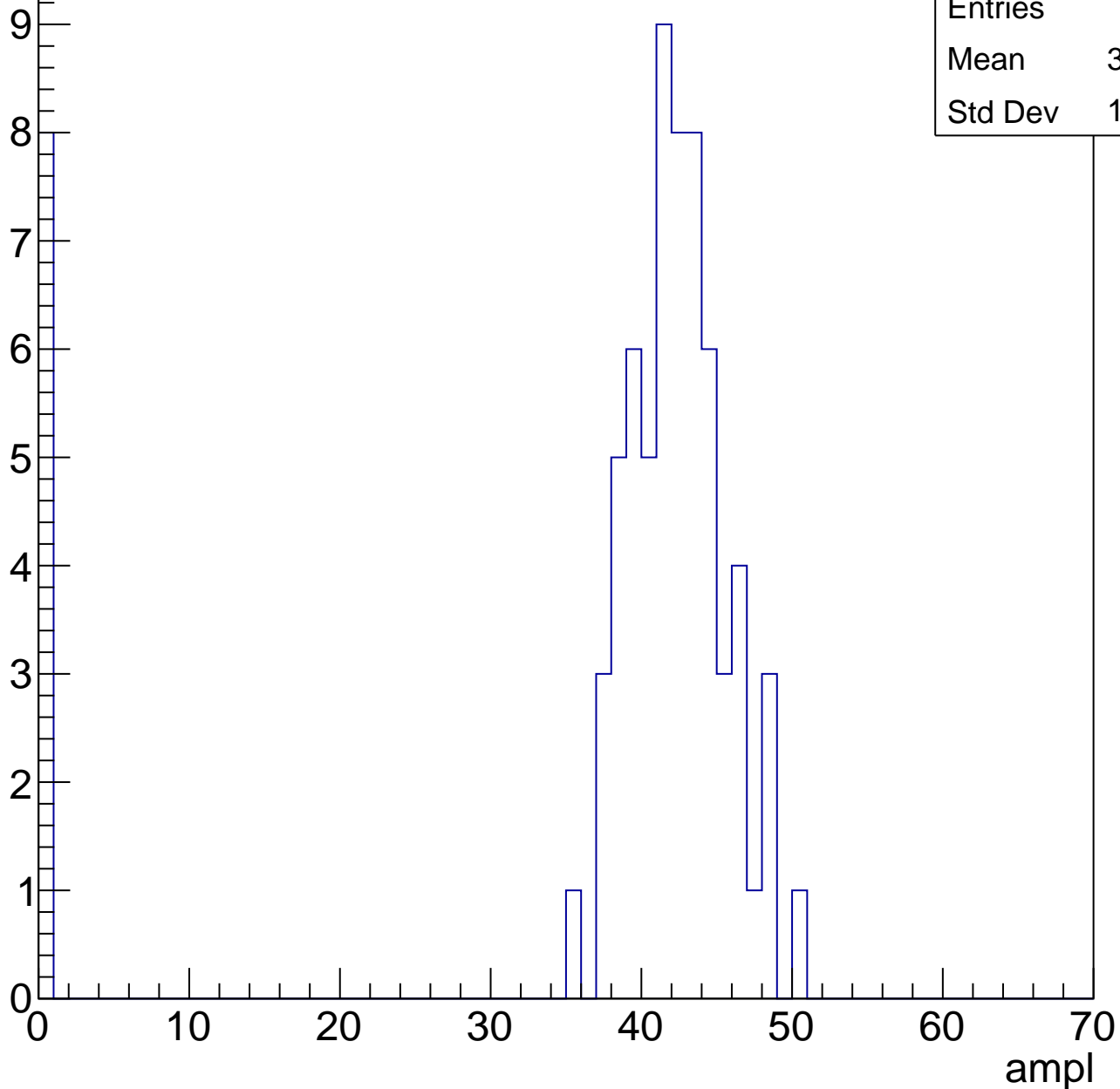
Entries	59
Mean	34.63
Std Dev	7.526



B1L103S, U12-ch48, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

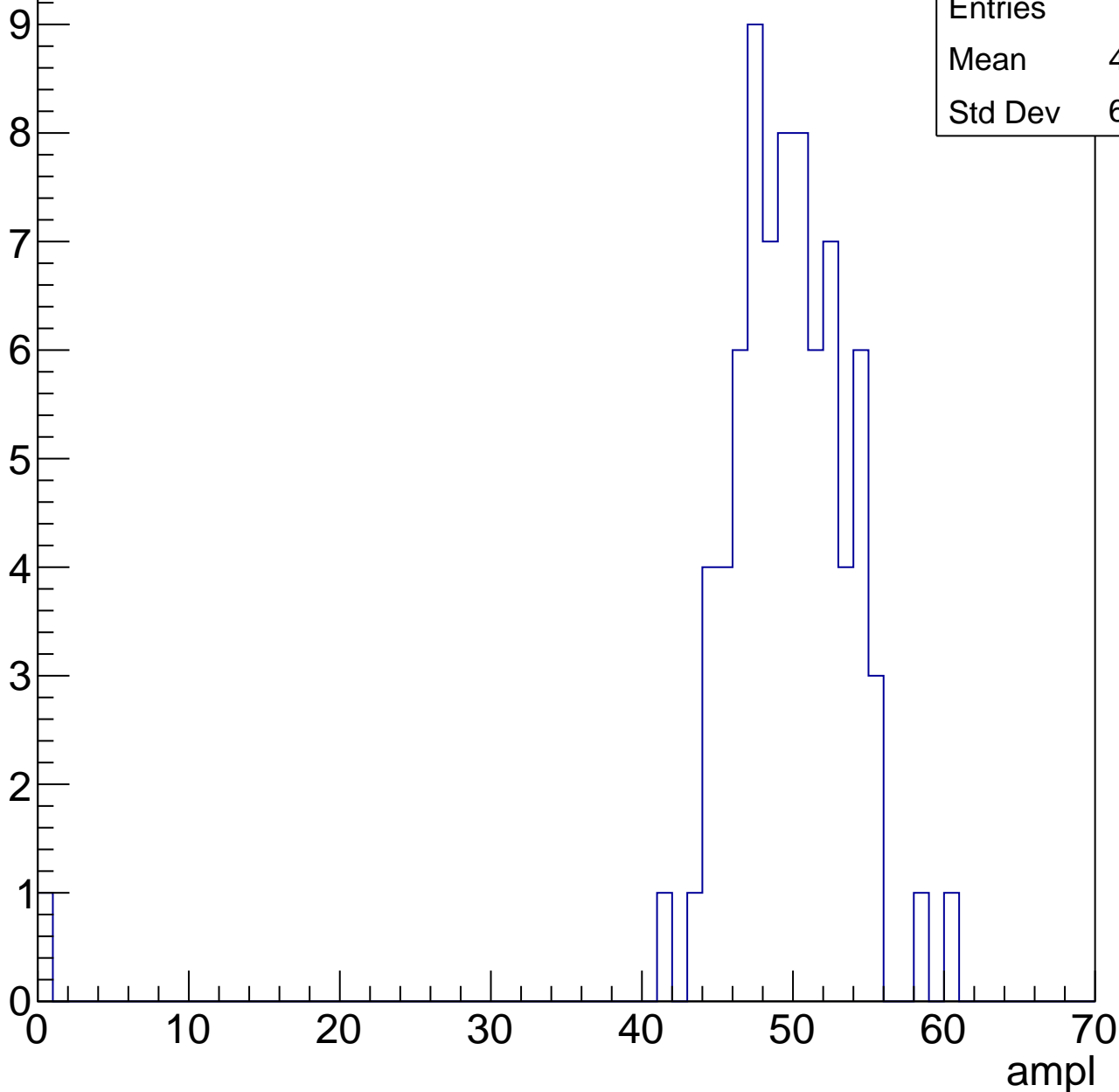


B1L103S, U12-ch48, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	77
Mean	48.78
Std Dev	6.623

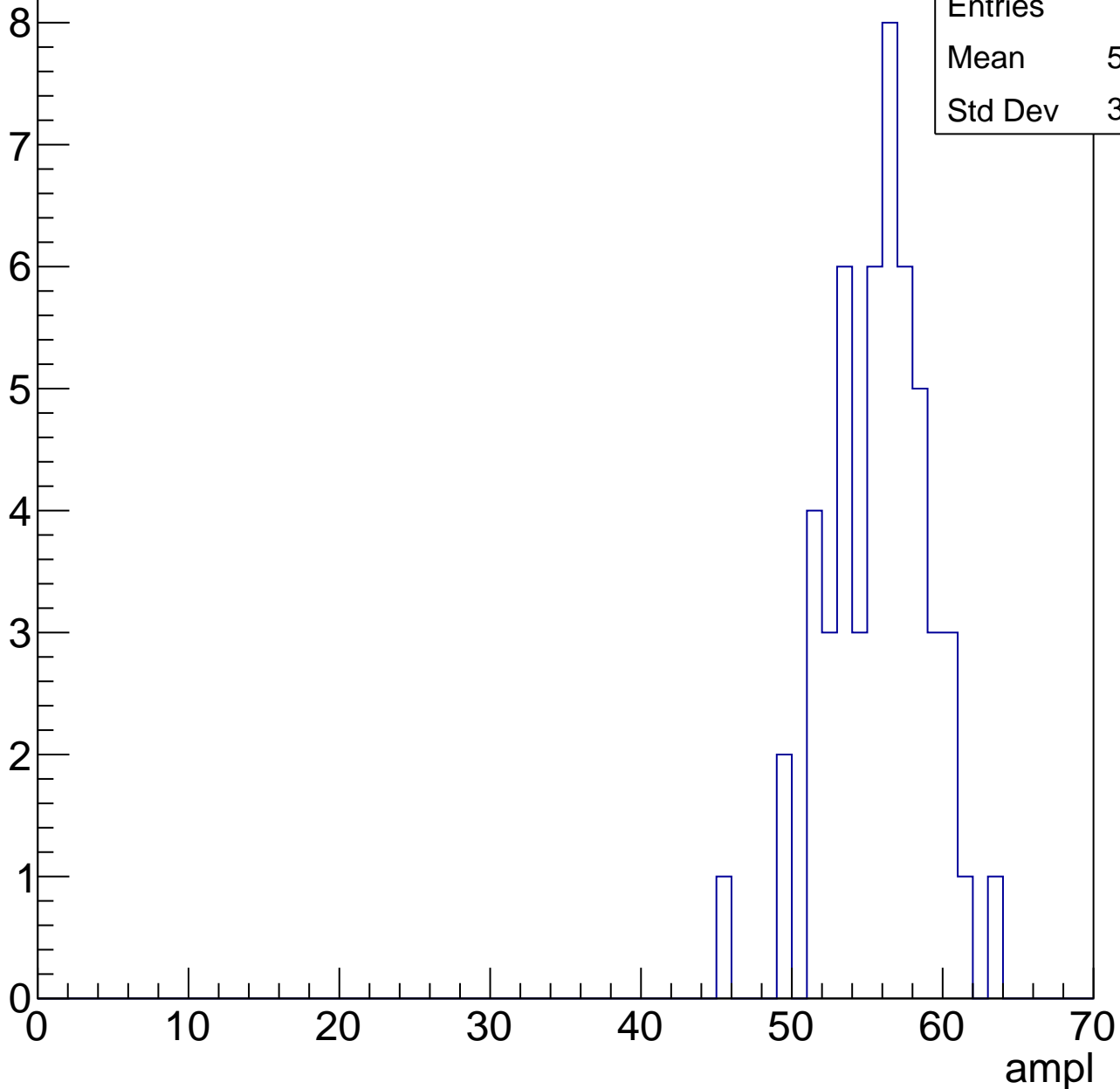


B1L103S, U12-ch48, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	52
Mean	55.27
Std Dev	3.358

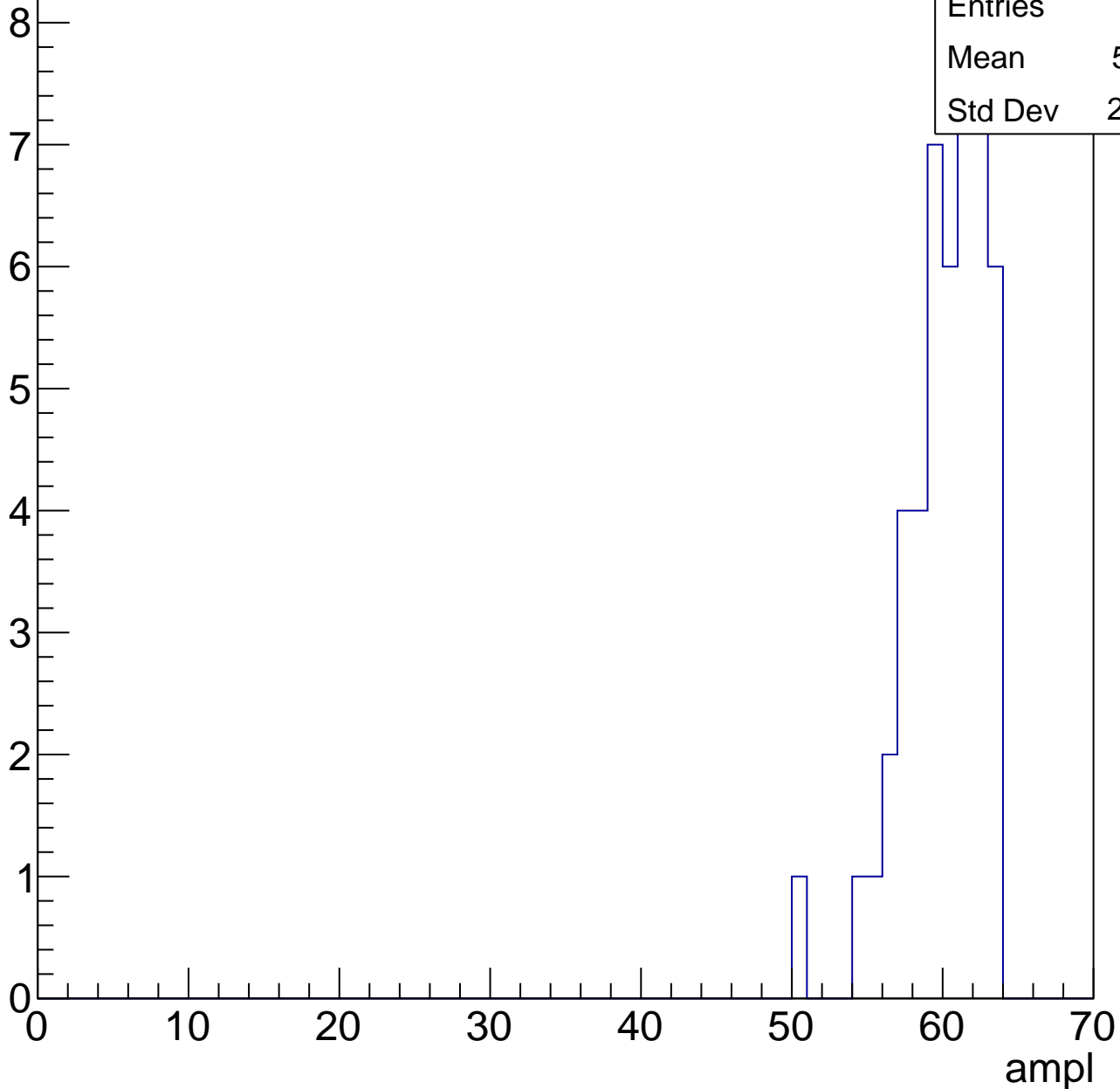


B1L103S, U12-ch48, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	48
Mean	59.71
Std Dev	2.669



B1L103S, U12-ch48, adc6

calib_packv5_041523_1651.root, FC#0, port C2

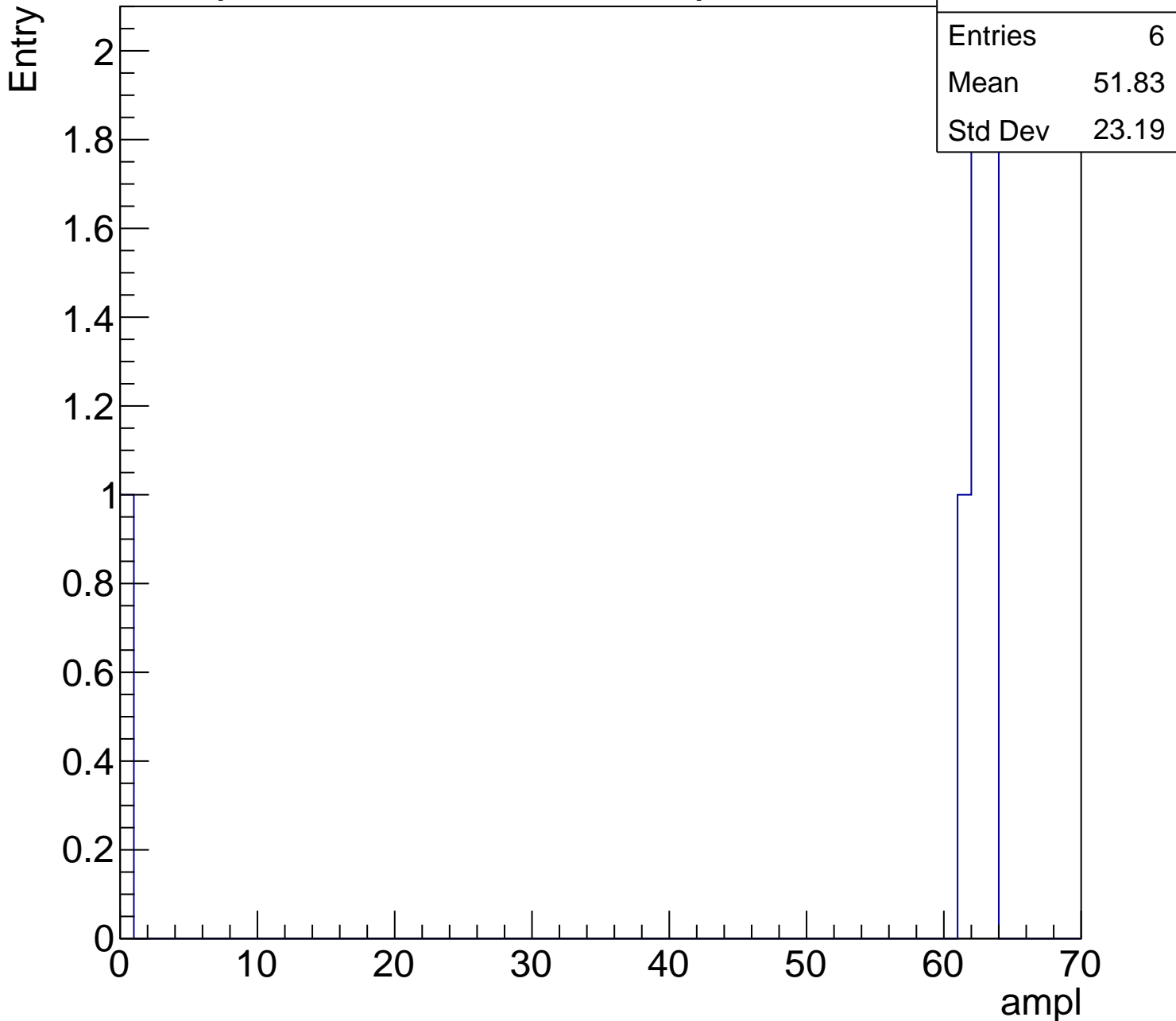
Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	6
Mean	51.83
Std Dev	23.19

0 10 20 30 40 50 60 70

ampl



B1L103S, U12-ch48, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.15
Std Dev	13.73

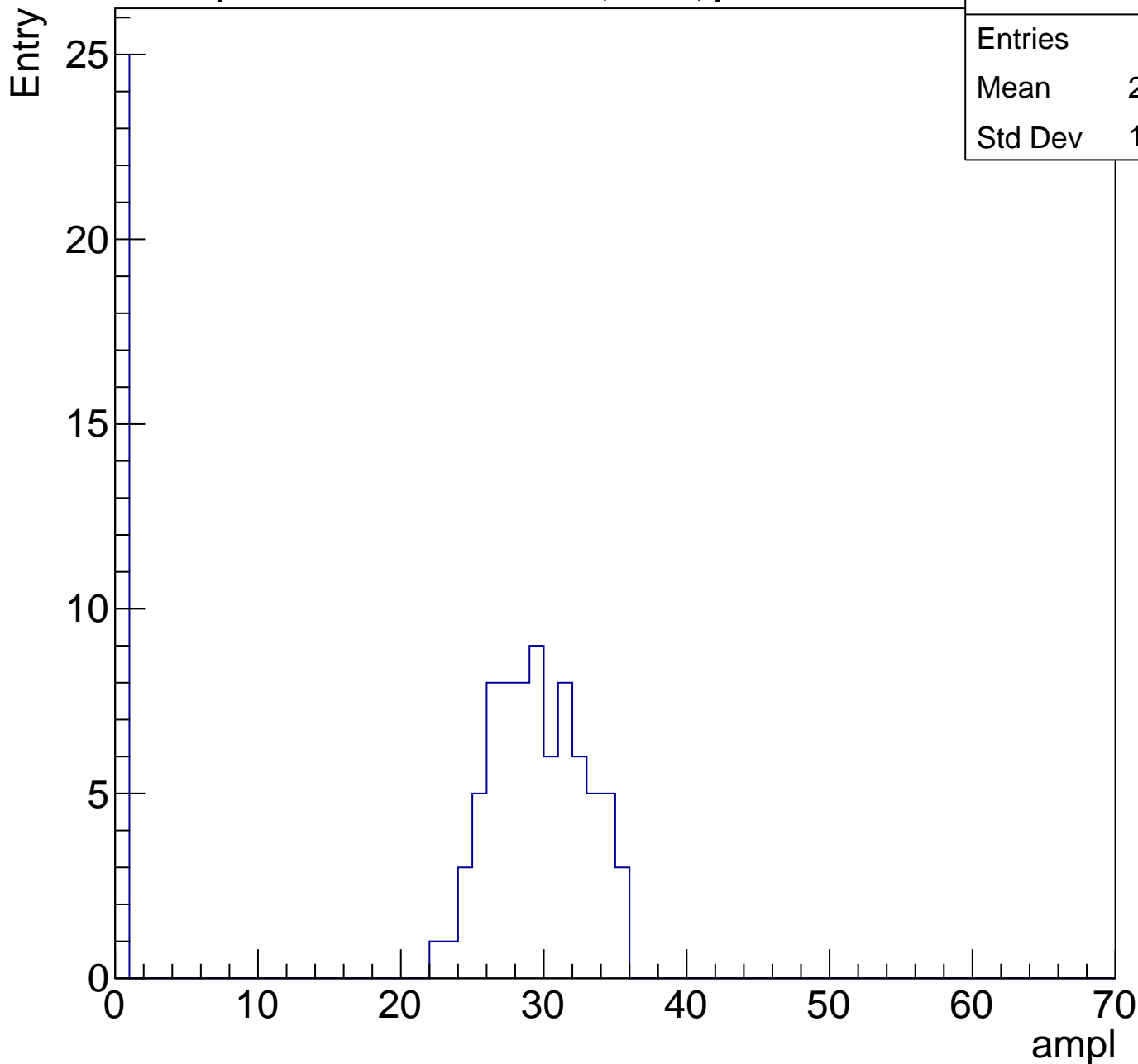
Entry



B1L103S, U12-ch49, adc0

calib_packv5_041523_1651.root, FC#0, port C2

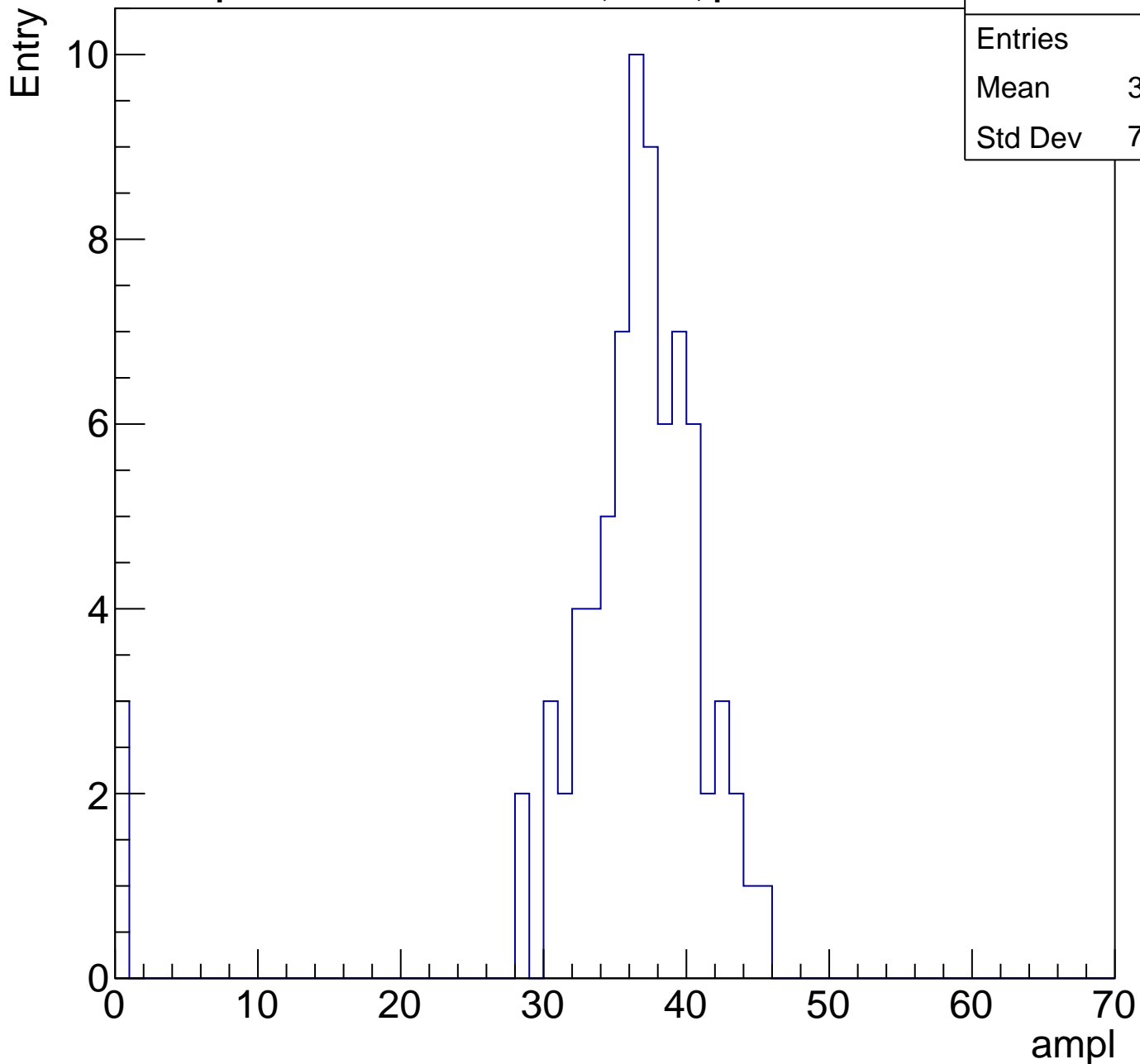
Entries	101
Mean	21.89
Std Dev	12.85



B1L103S, U12-ch49, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	77
Mean	35.06
Std Dev	7.917

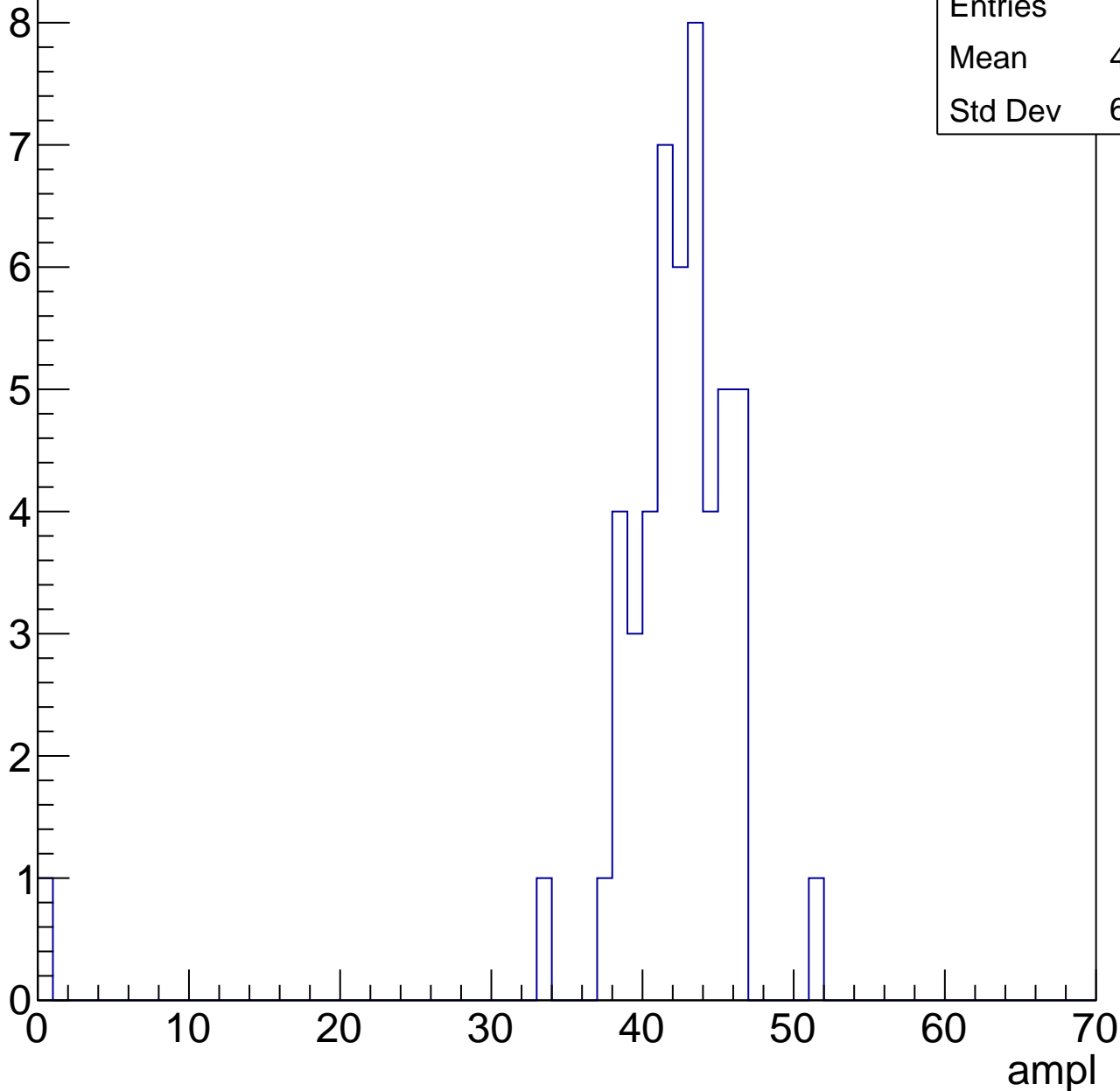


B1L103S, U12-ch49, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	50
Mean	41.28
Std Dev	6.615



B1L103S, U12-ch49, adc3

calib_packv5_041523_1651.root, FC#0, port C2

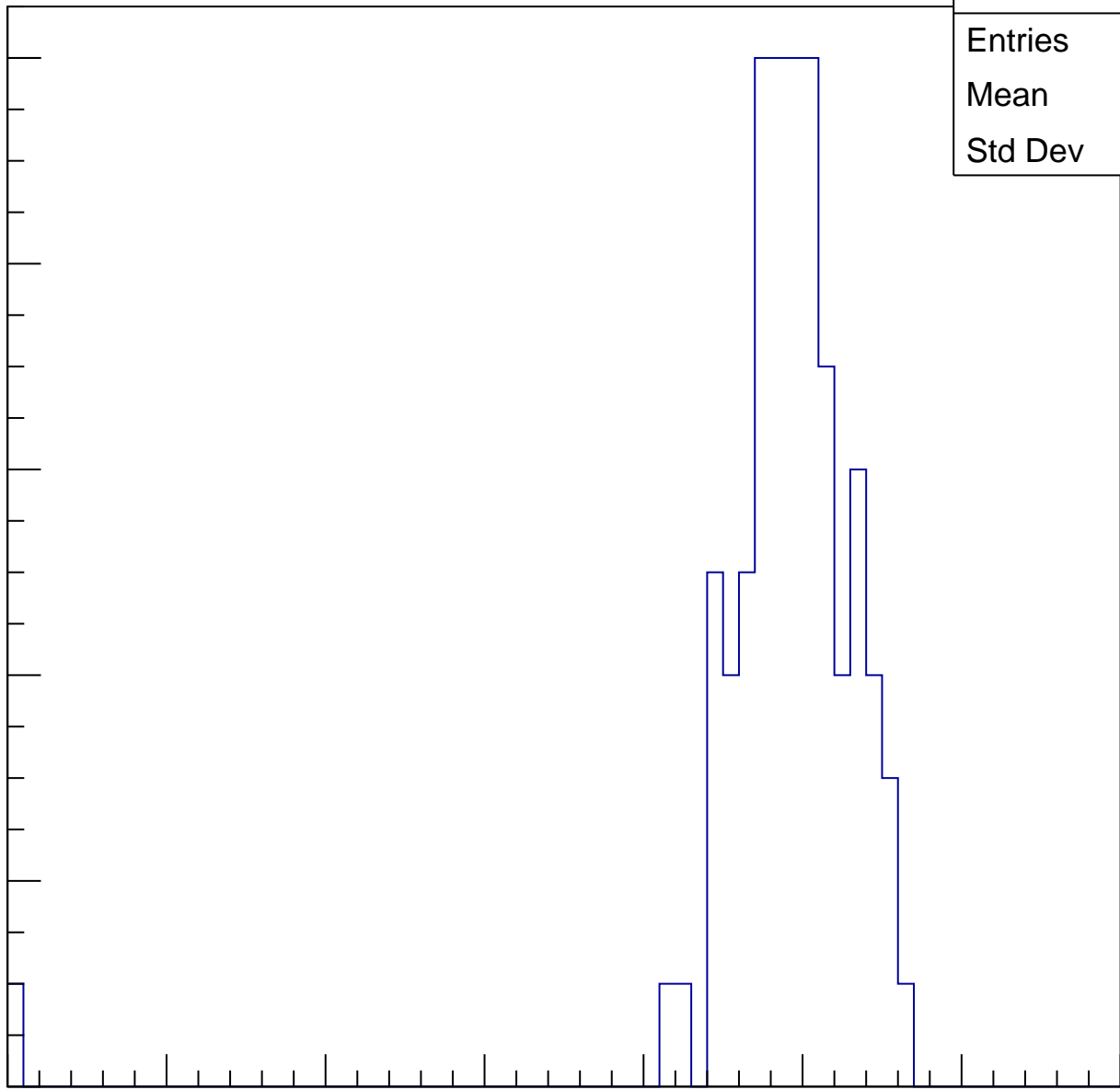
Entries	82
Mean	48.45
Std Dev	6.247

Entry

10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70

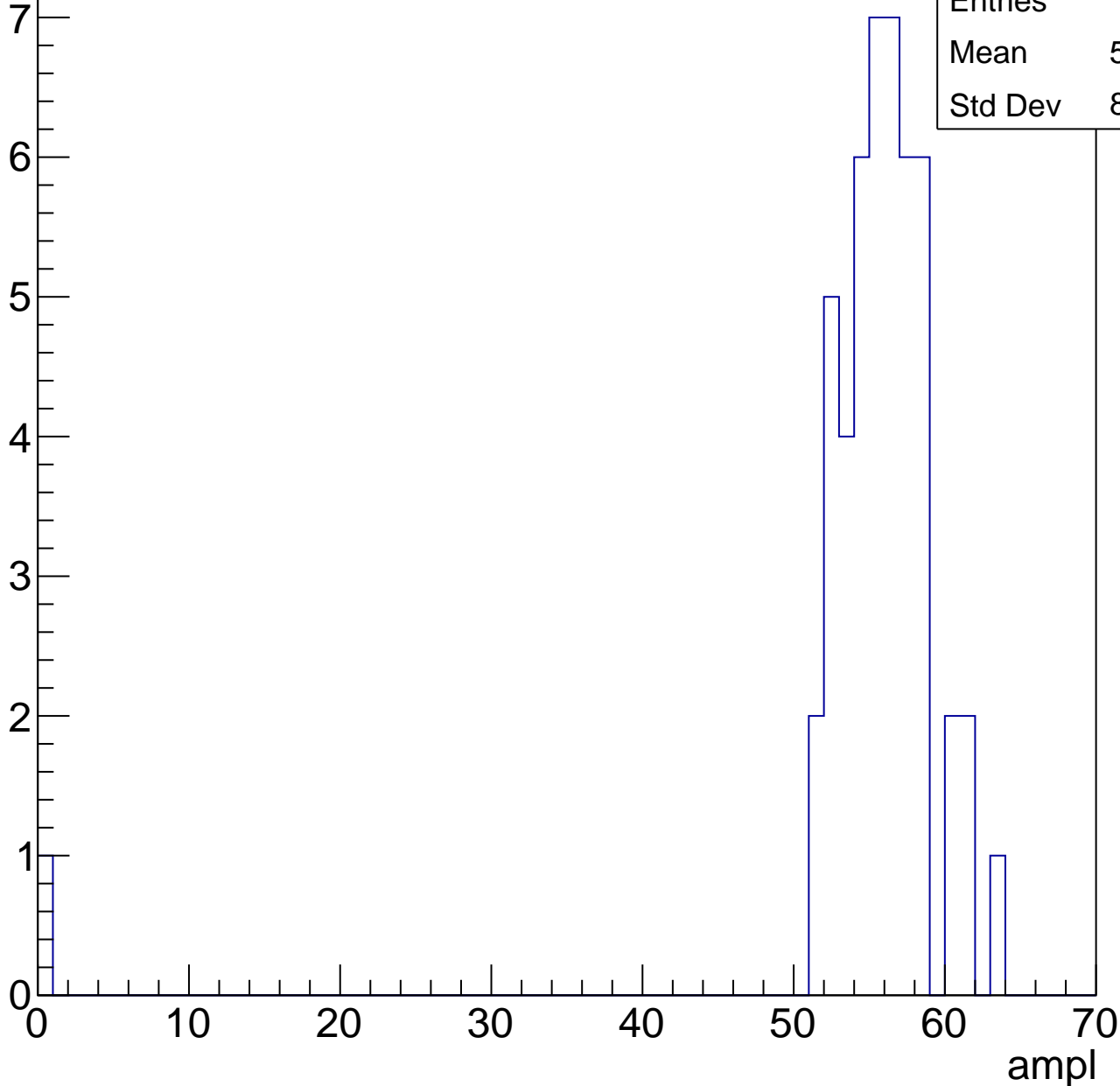


B1L103S, U12-ch49, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

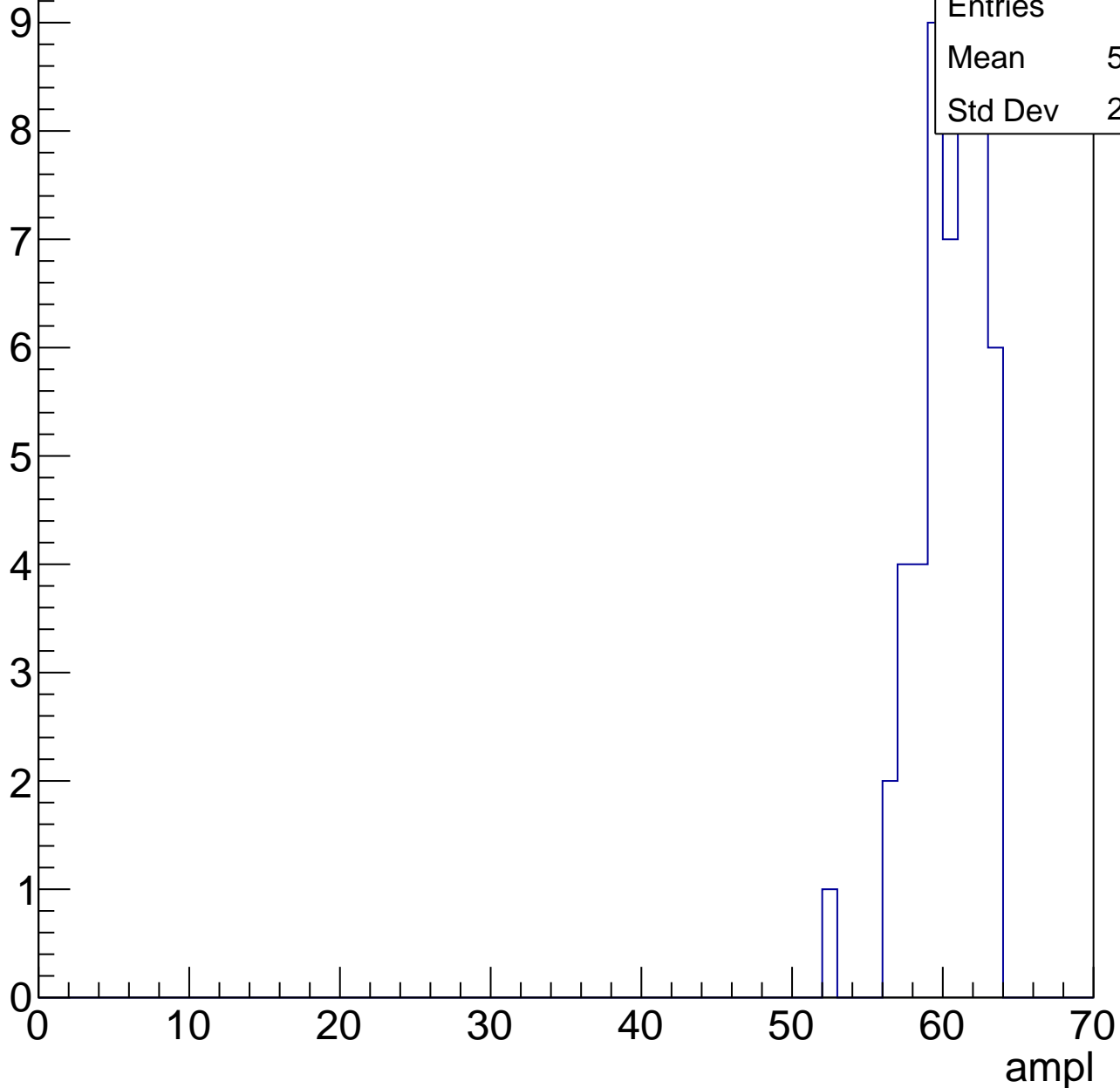
Entries	49
Mean	54.49
Std Dev	8.308



B1L103S, U12-ch49, adc5

calib_packv5_041523_1651.root, FC#0, port C2

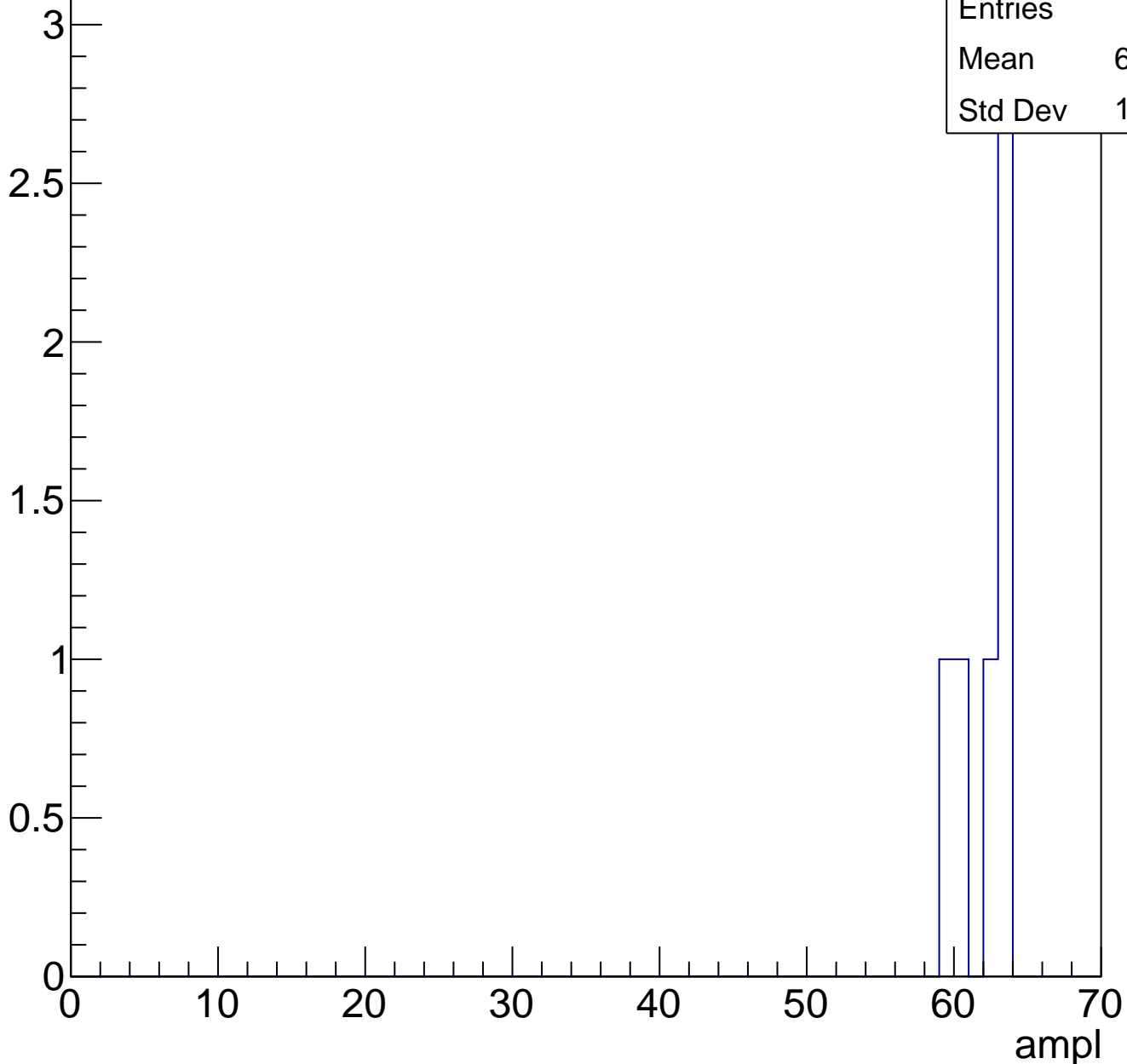
Entry



B1L103S, U12-ch49, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

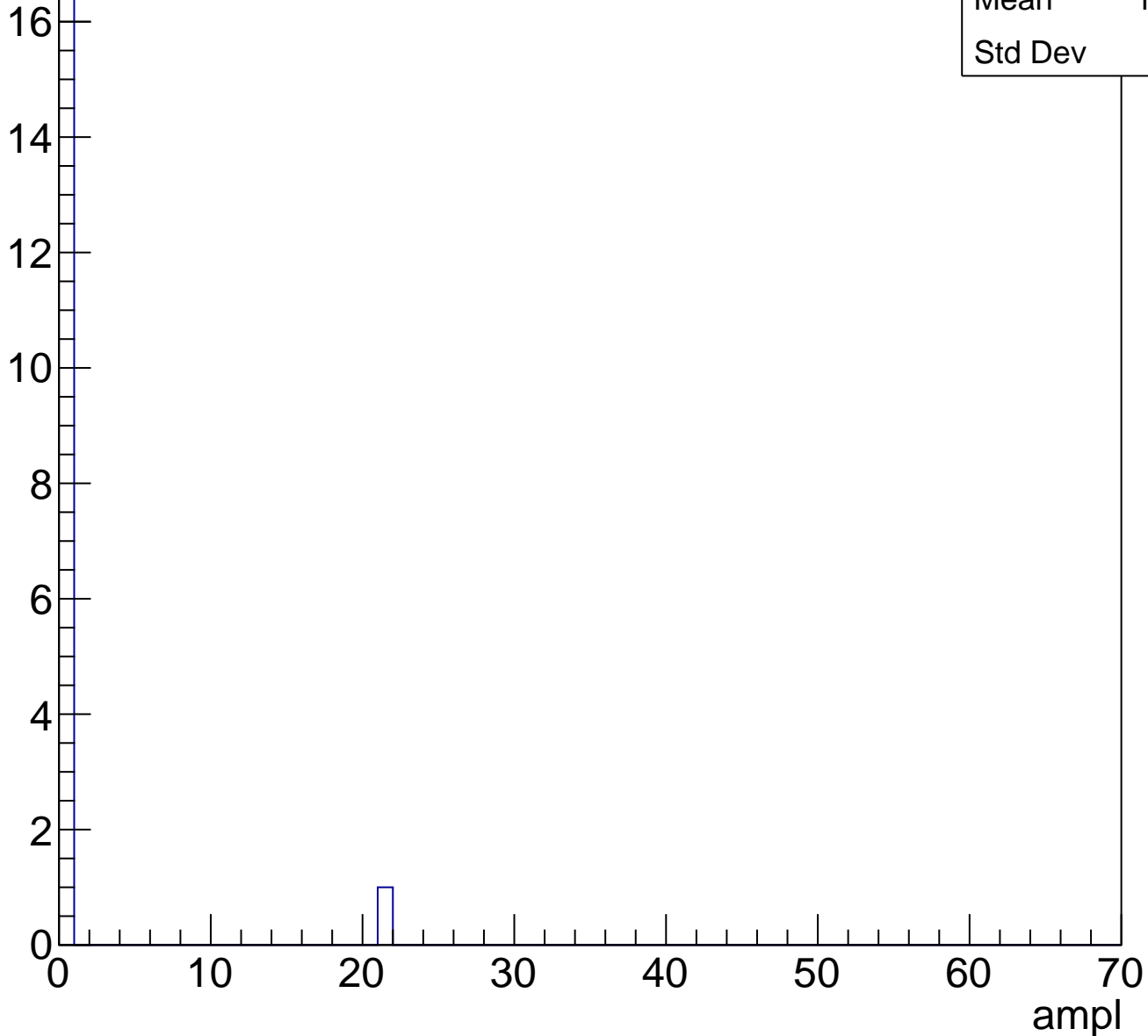


B1L103S, U12-ch49, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	18
Mean	1.167
Std Dev	4.81

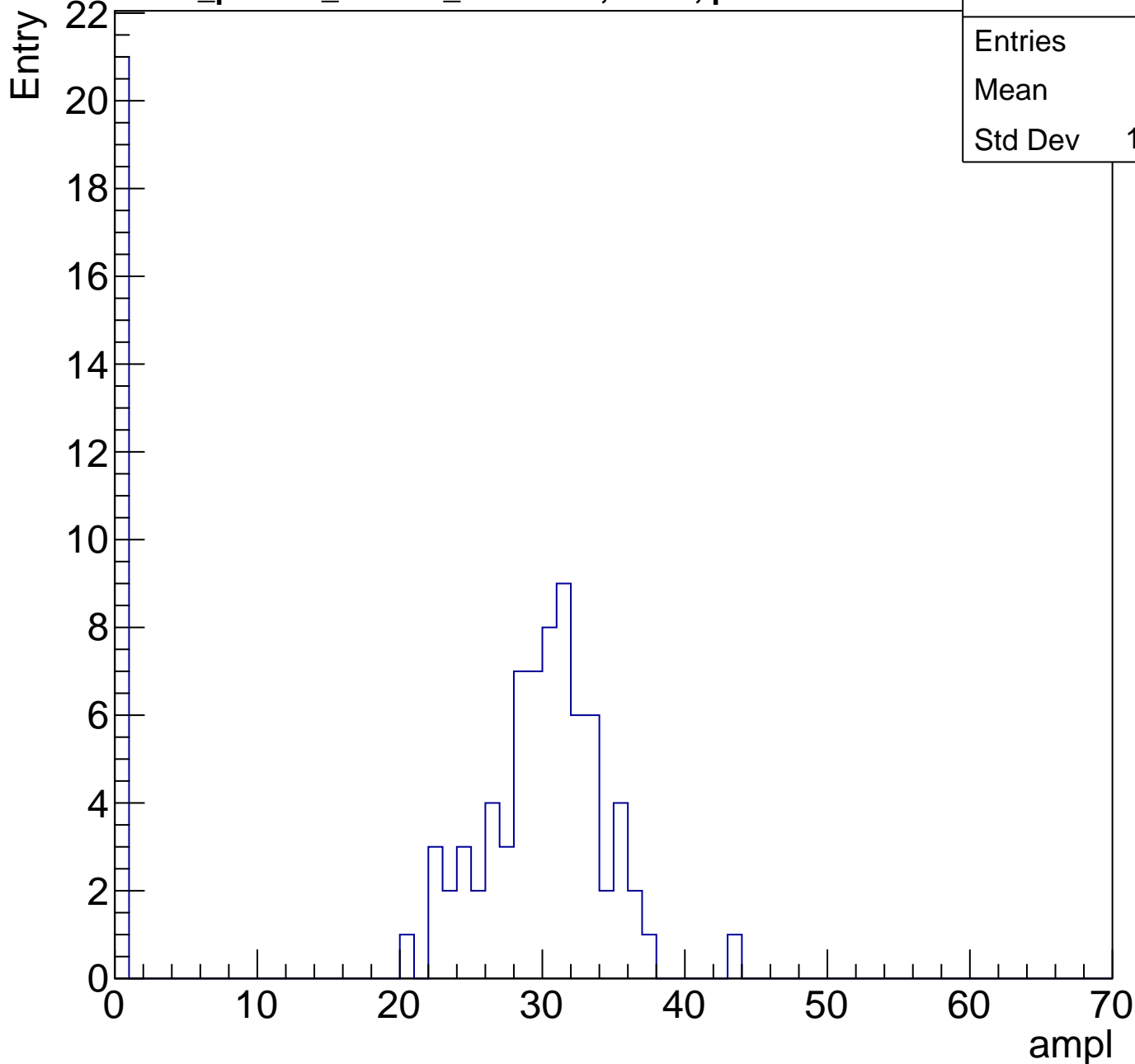
Entry



B1L103S, U12-ch50, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	92
Mean	22.9
Std Dev	12.96

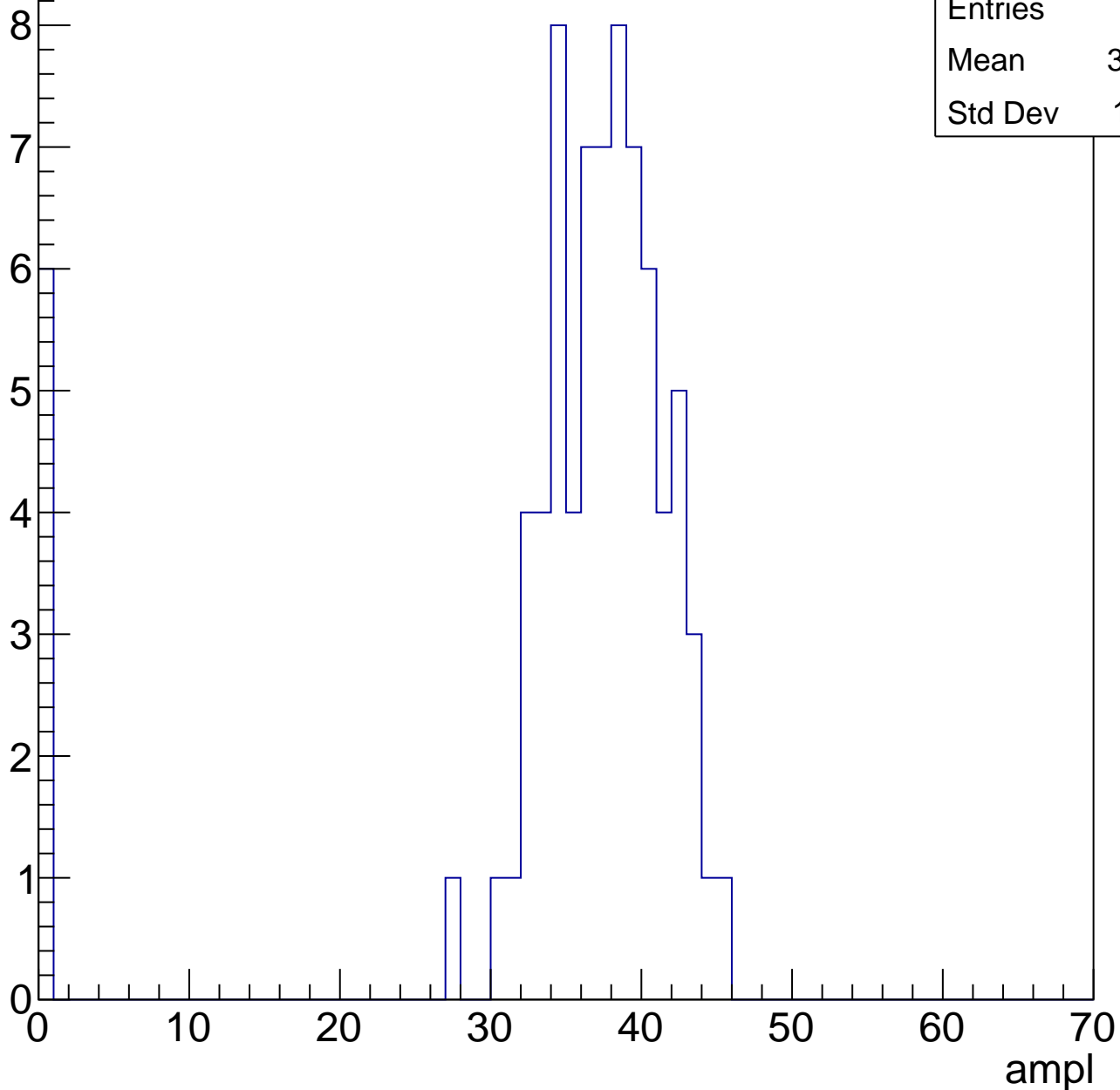


B1L103S, U12-ch50, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	78
Mean	34.36
Std Dev	10.51

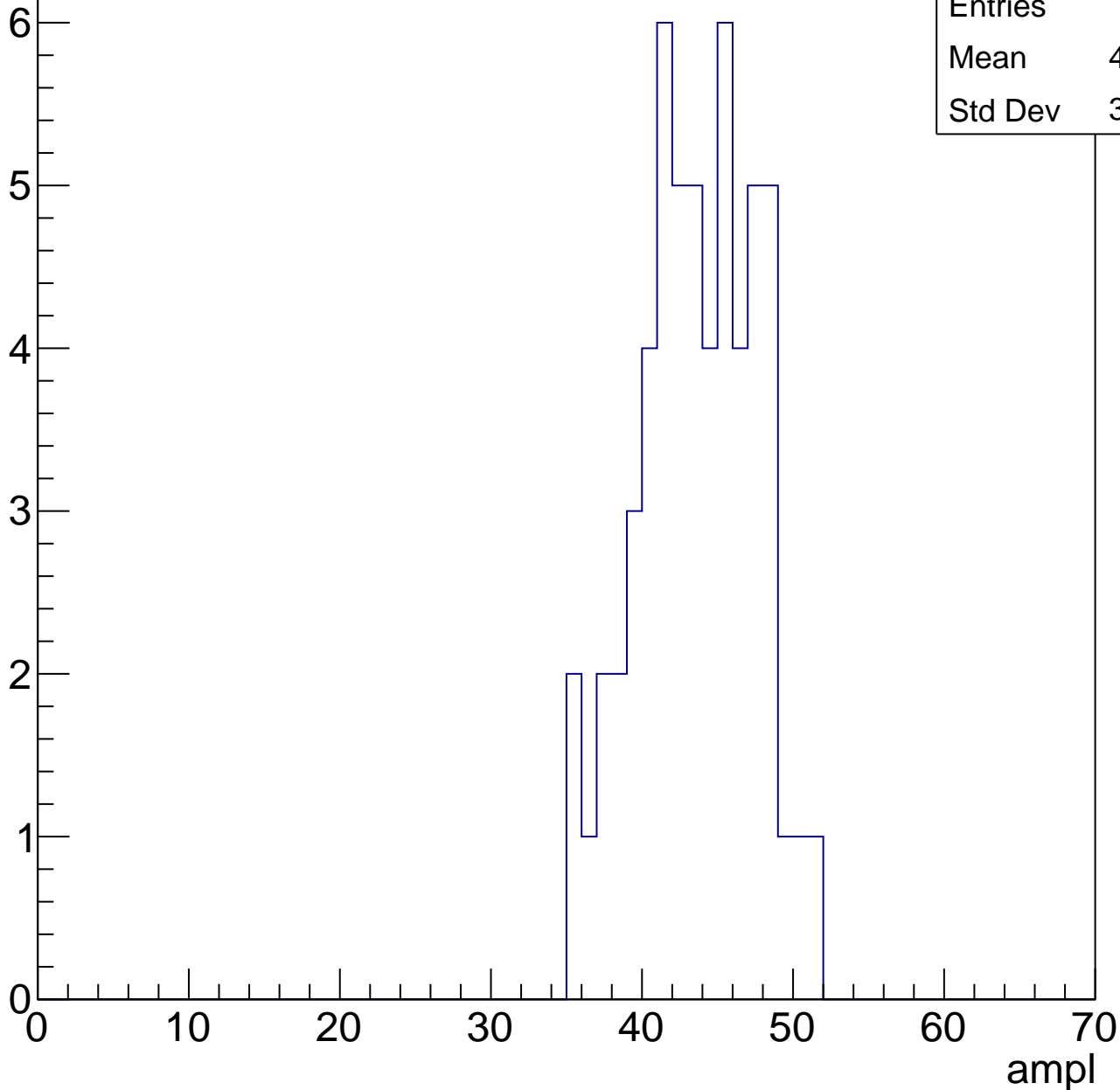


B1L103S, U12-ch50, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	57
Mean	43.14
Std Dev	3.813

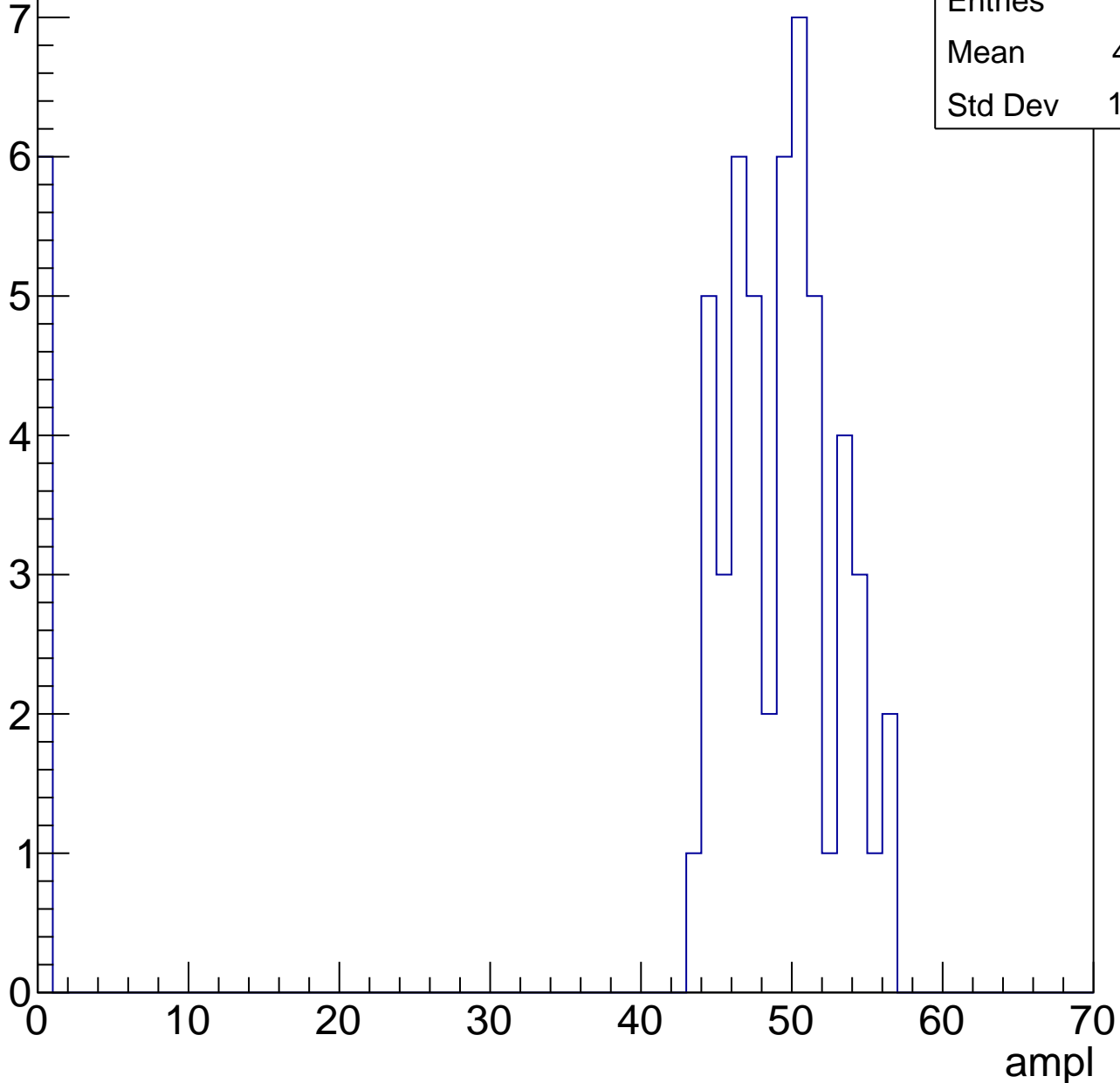


B1L103S, U12-ch50, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	57
Mean	43.81
Std Dev	15.37

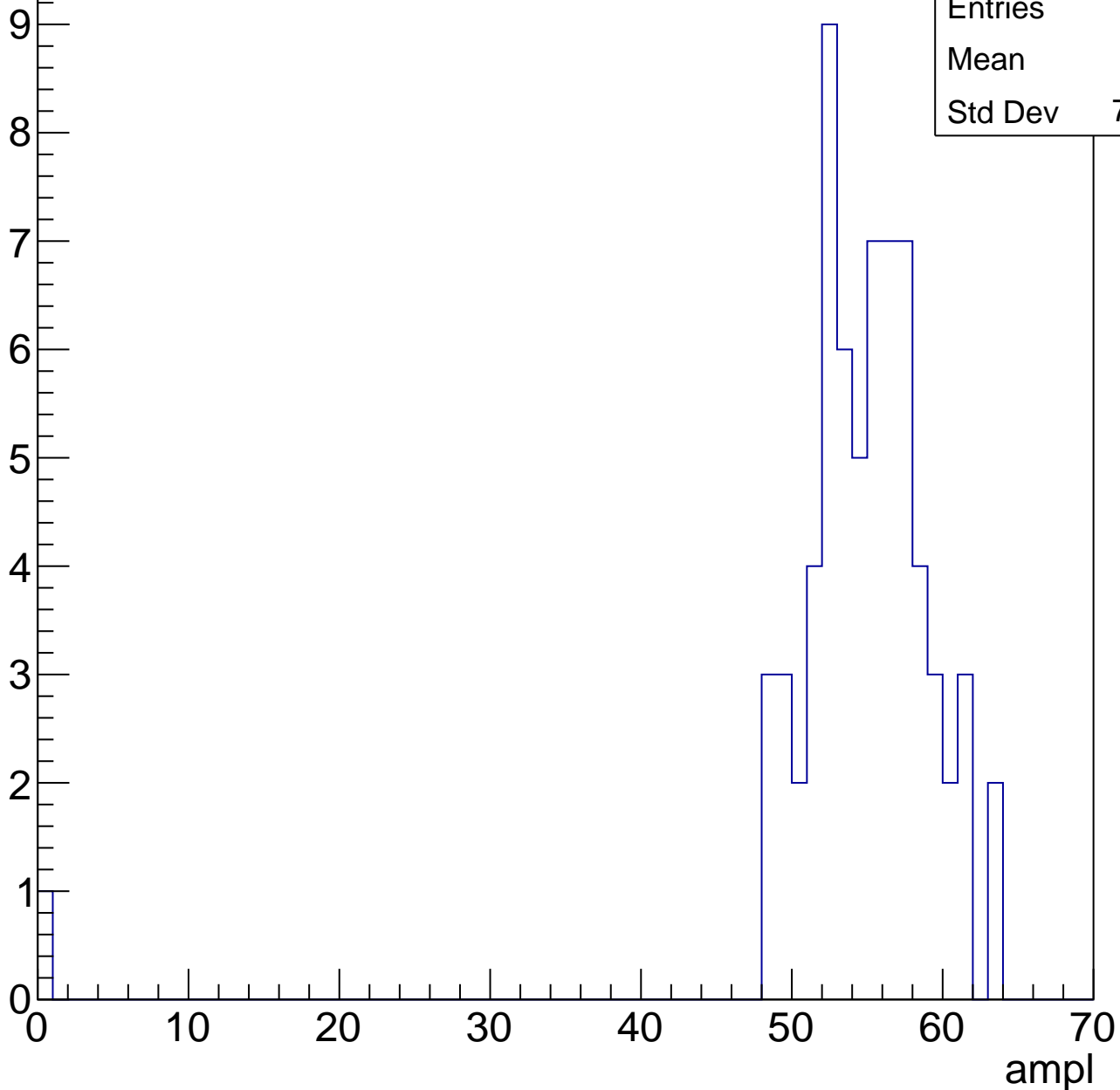


B1L103S, U12-ch50, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	53.9
Std Dev	7.501

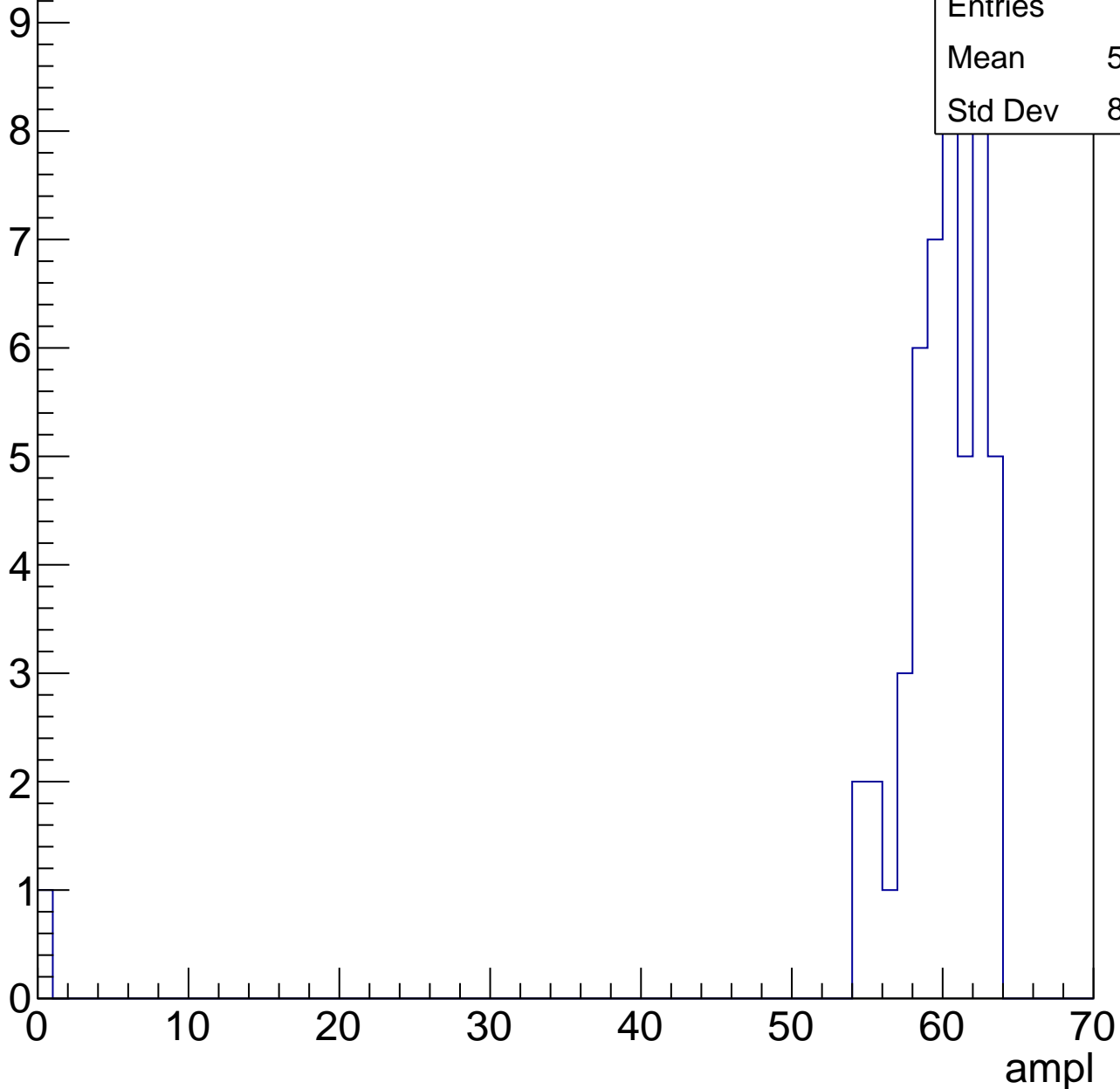


B1L103S, U12-ch50, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	49
Mean	58.45
Std Dev	8.765



B1L103S, U12-ch50, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch50, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

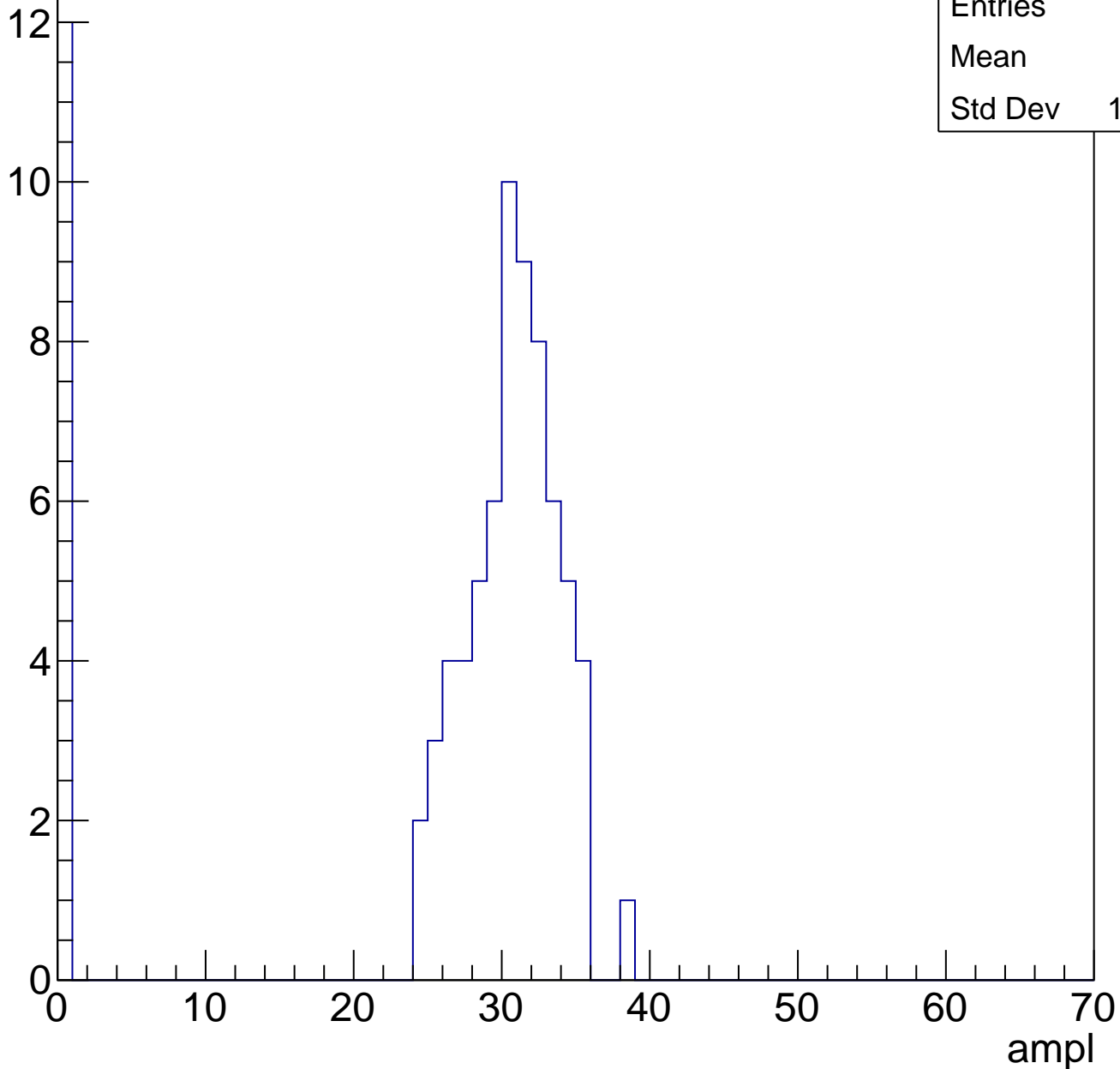
Entries	19
Mean	0
Std Dev	0

B1L103S, U12-ch51, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	79
Mean	25.7
Std Dev	11.22

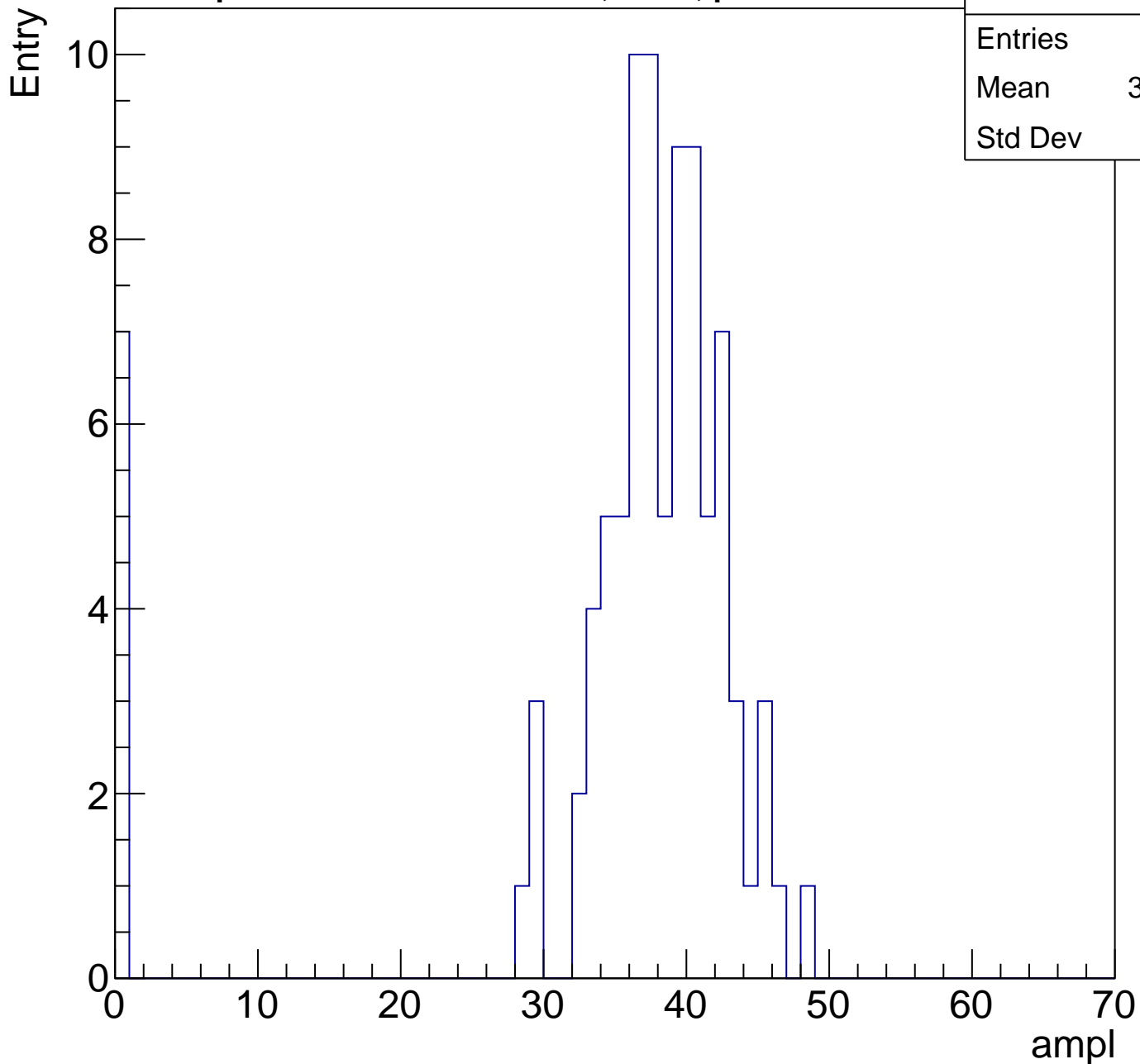
Entry



B1L103S, U12-ch51, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	91
Mean	35.03
Std Dev	10.8

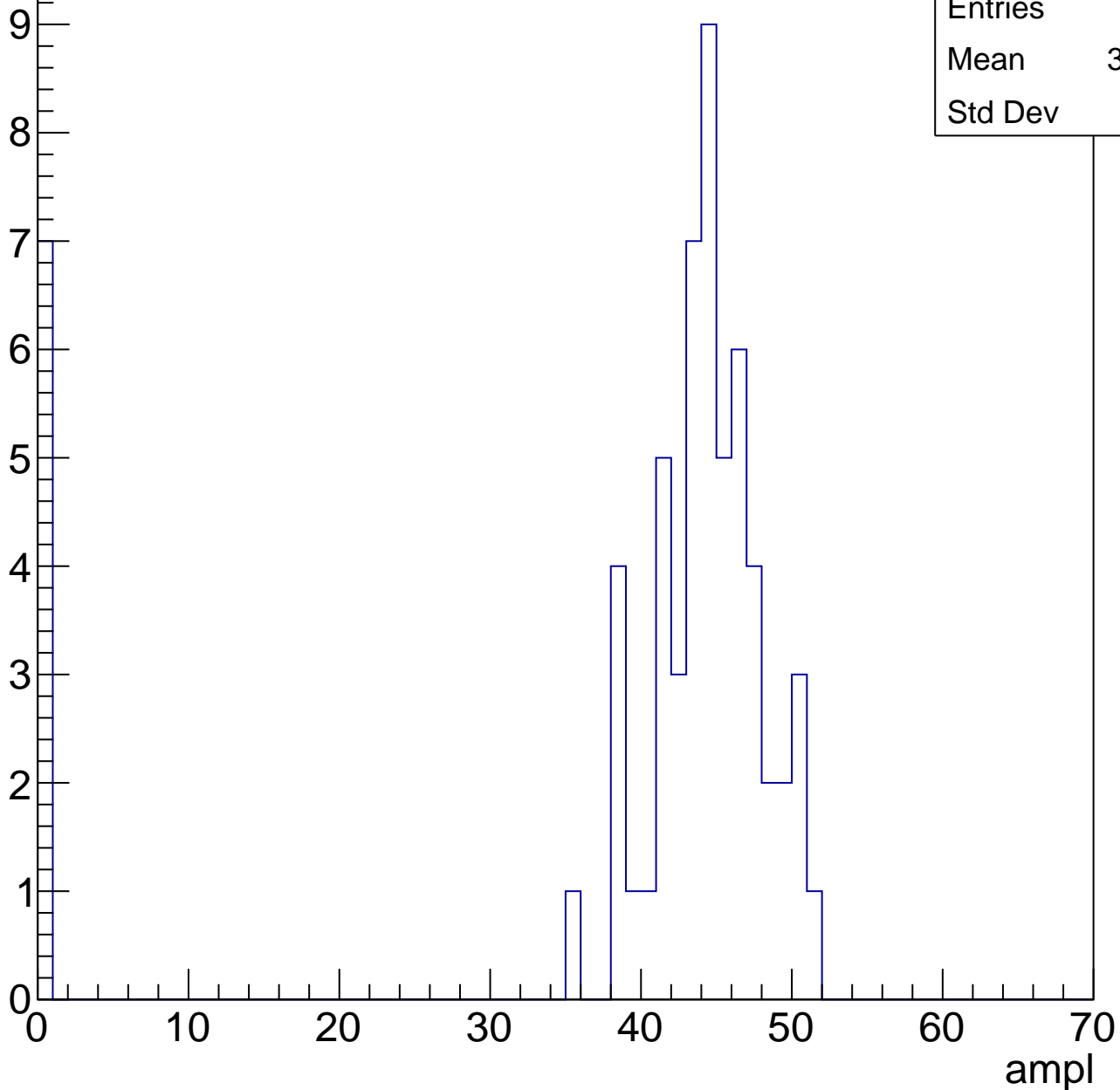


B1L103S, U12-ch51, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

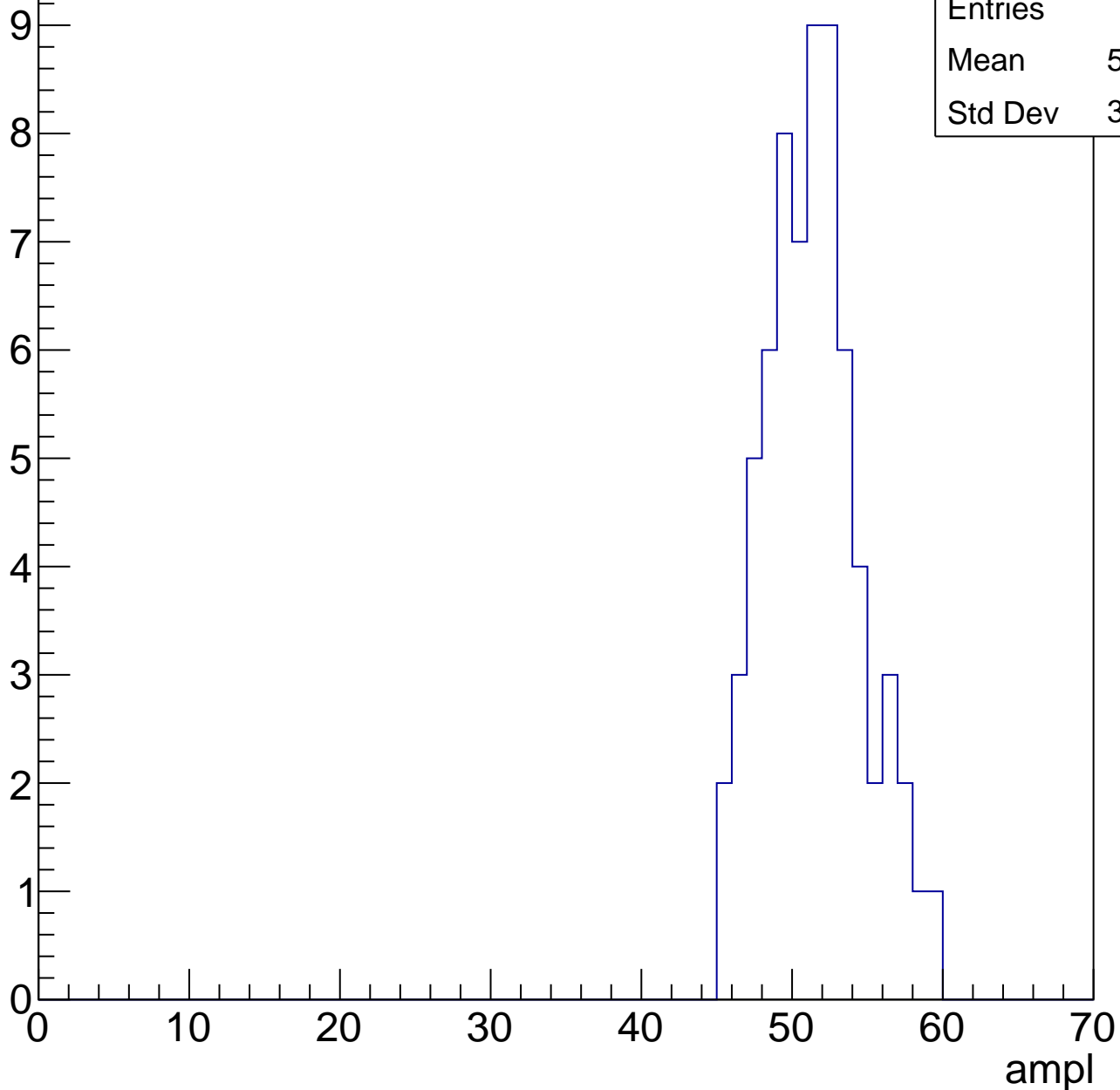
Entries	61
Mean	38.98
Std Dev	14.4



B1L103S, U12-ch51, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

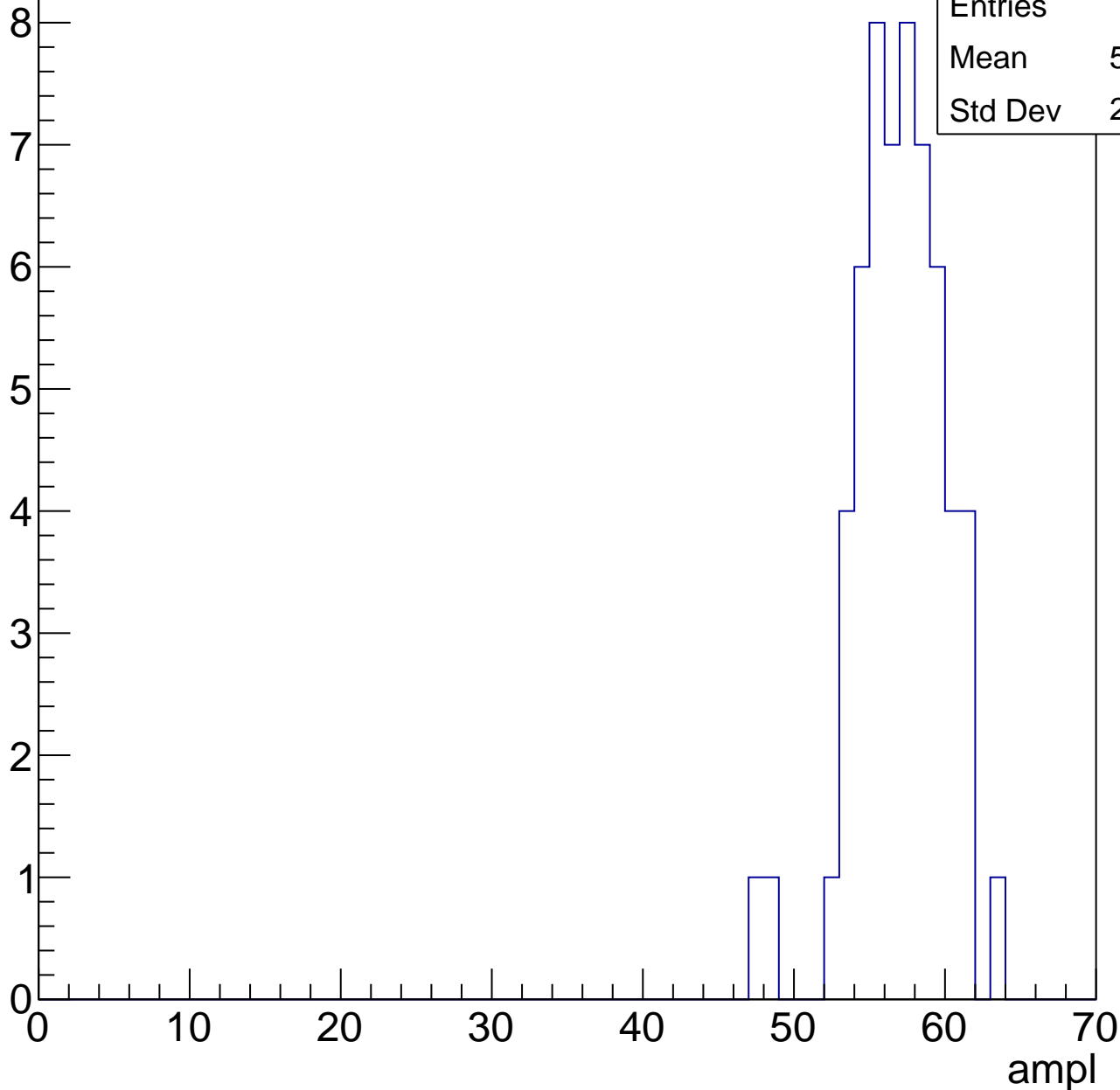


B1L103S, U12-ch51, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	56.52
Std Dev	2.984

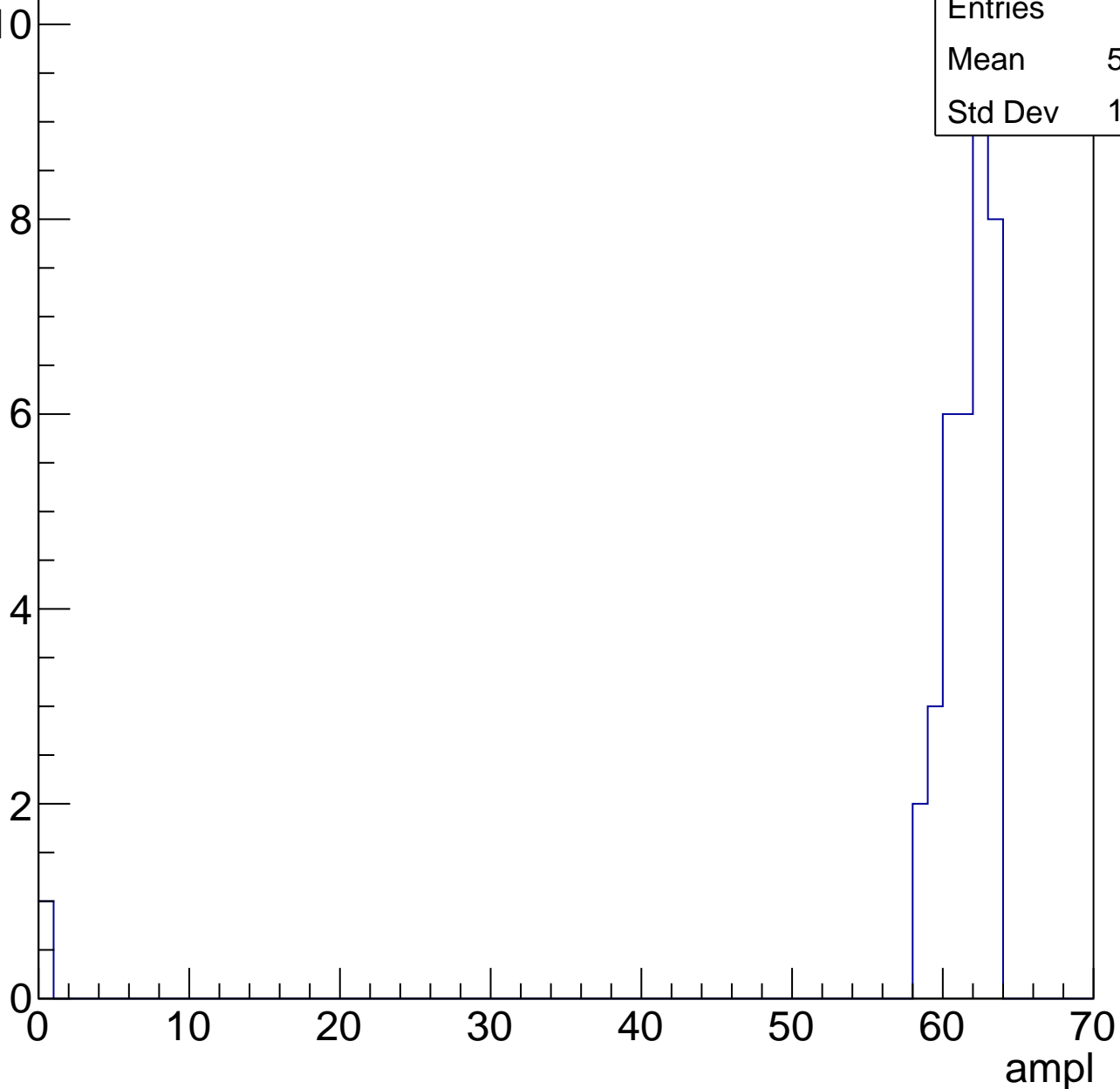


B1L103S, U12-ch51, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	36
Mean	59.53
Std Dev	10.17



B1L103S, U12-ch51, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch51, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

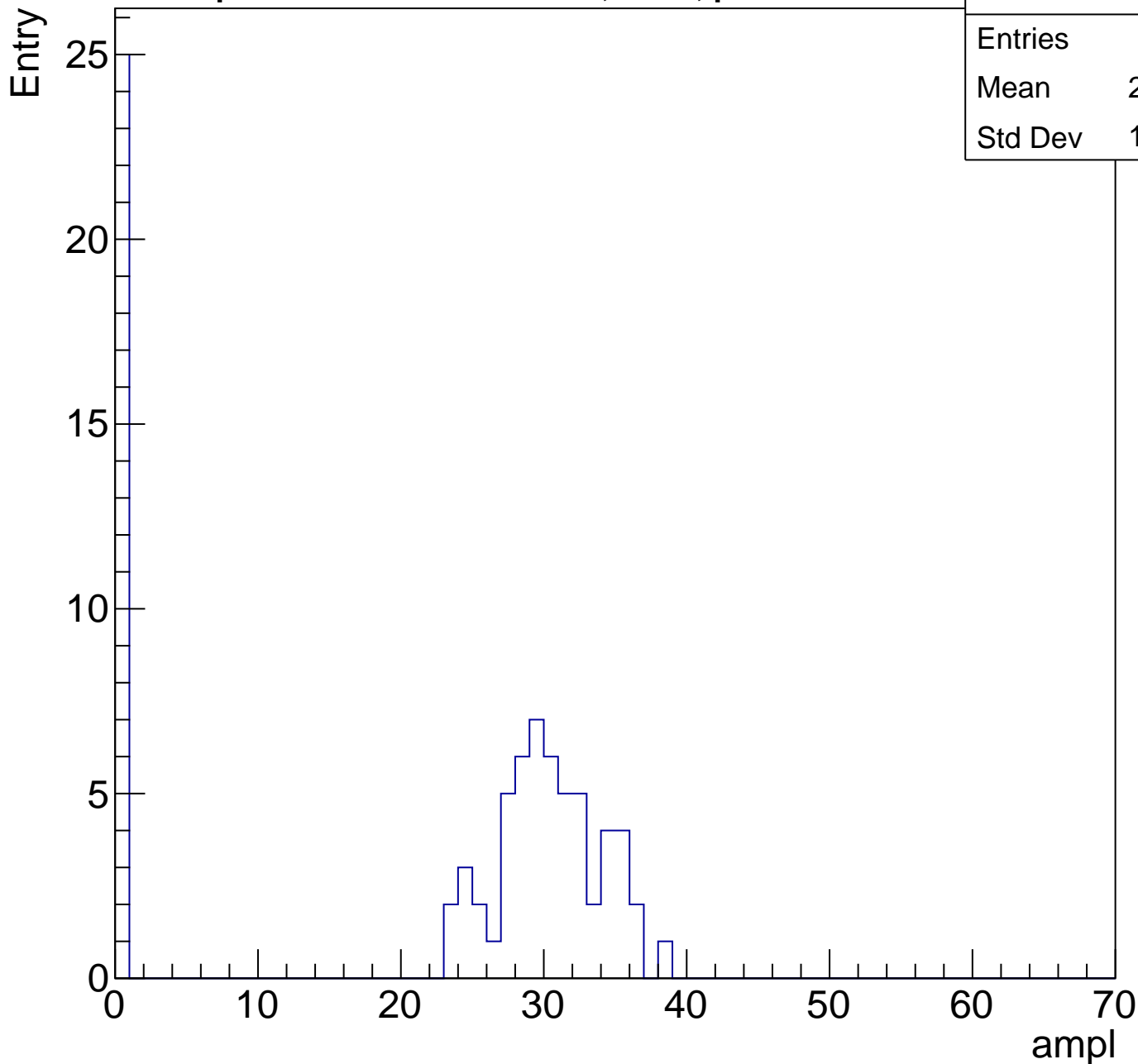


Entries	19
Mean	0
Std Dev	0

B1L103S, U12-ch52, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	80
Mean	20.59
Std Dev	14.19

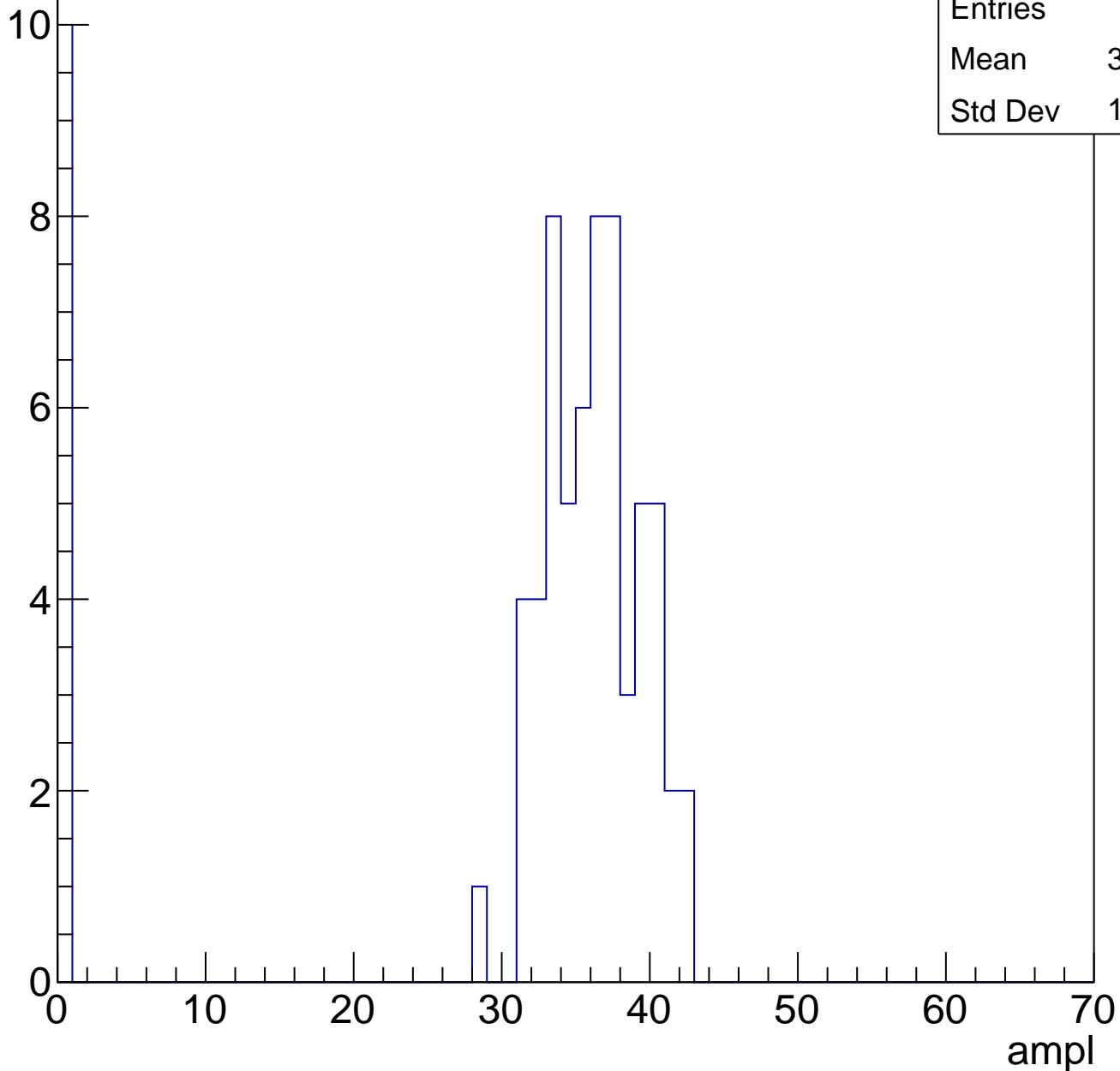


B1L103S, U12-ch52, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	71
Mean	30.75
Std Dev	12.78

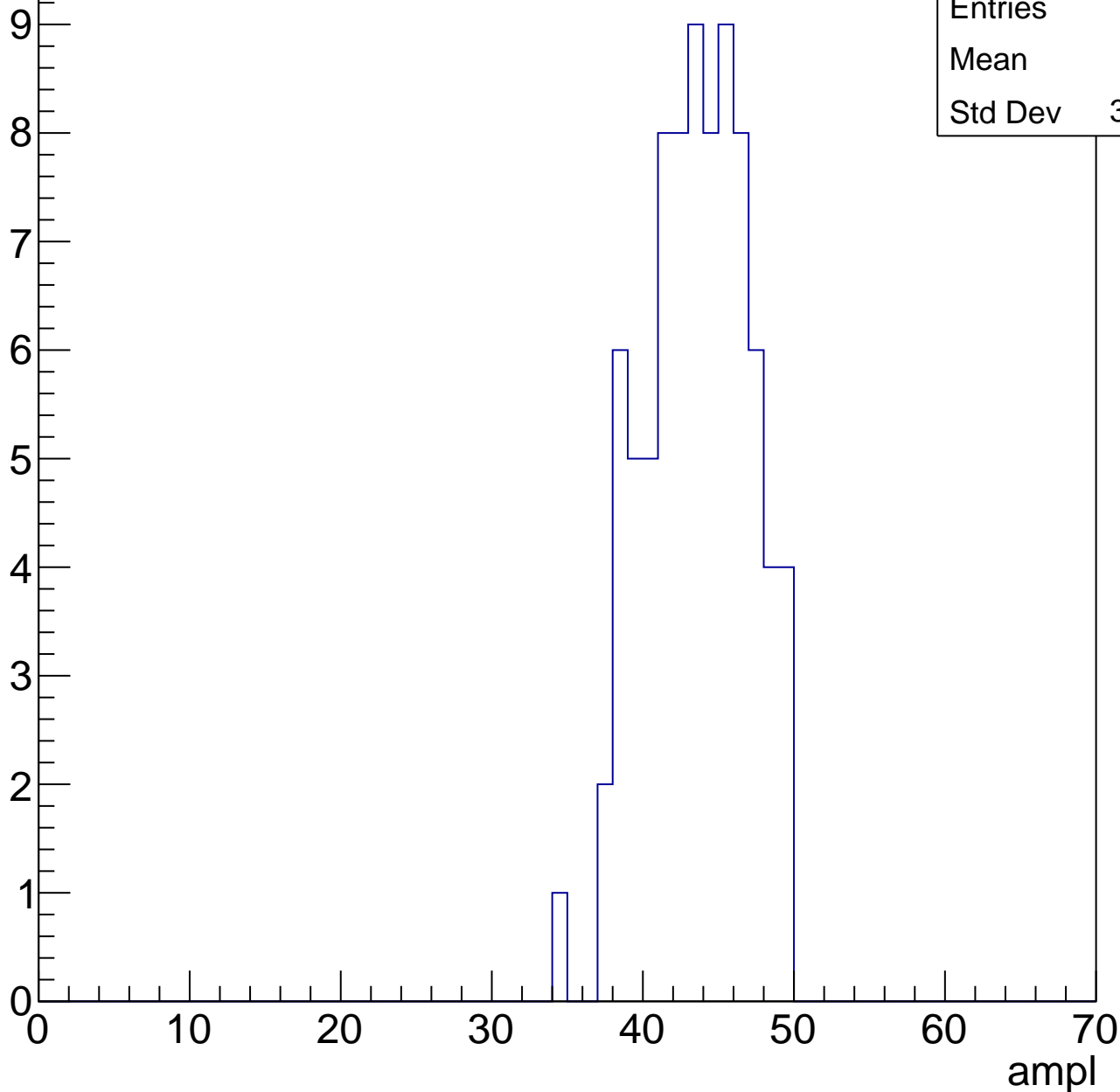
Entry



B1L103S, U12-ch52, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

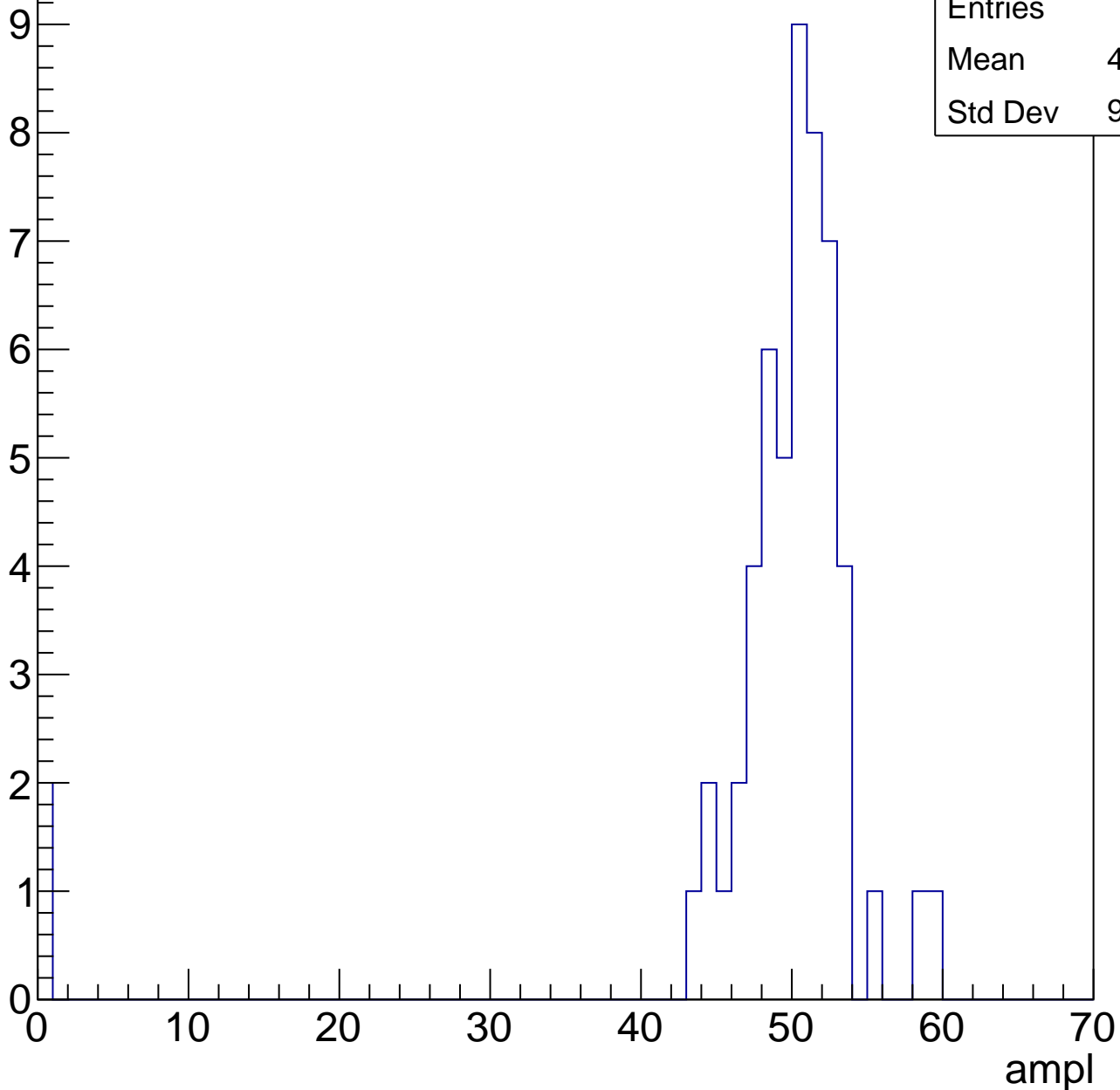


B1L103S, U12-ch52, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	54
Mean	48.06
Std Dev	9.889



B1L103S, U12-ch52, adc4

calib_packv5_041523_1651.root, FC#0, port C2

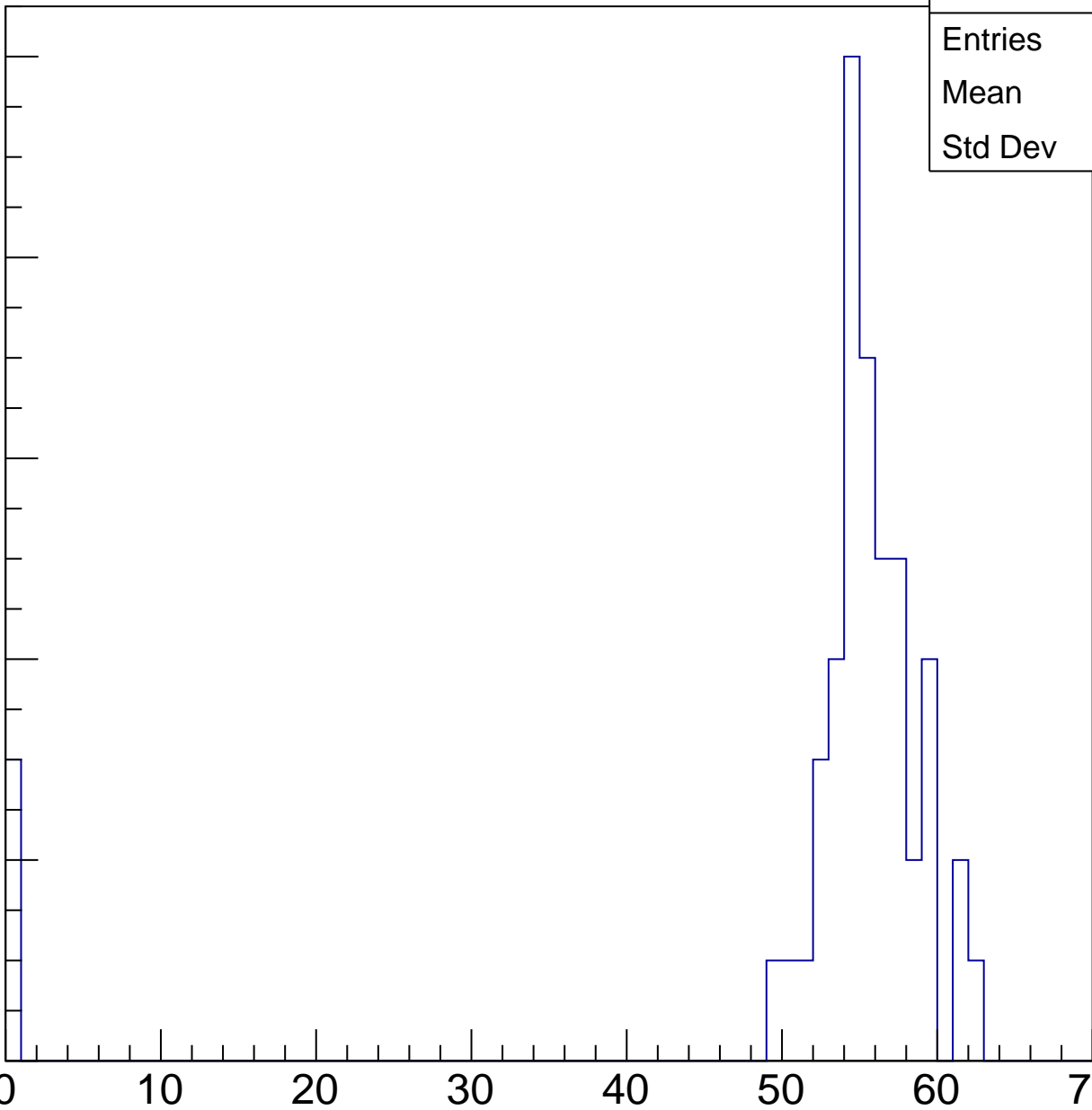
Entries	49
Mean	51.92
Std Dev	13.53

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

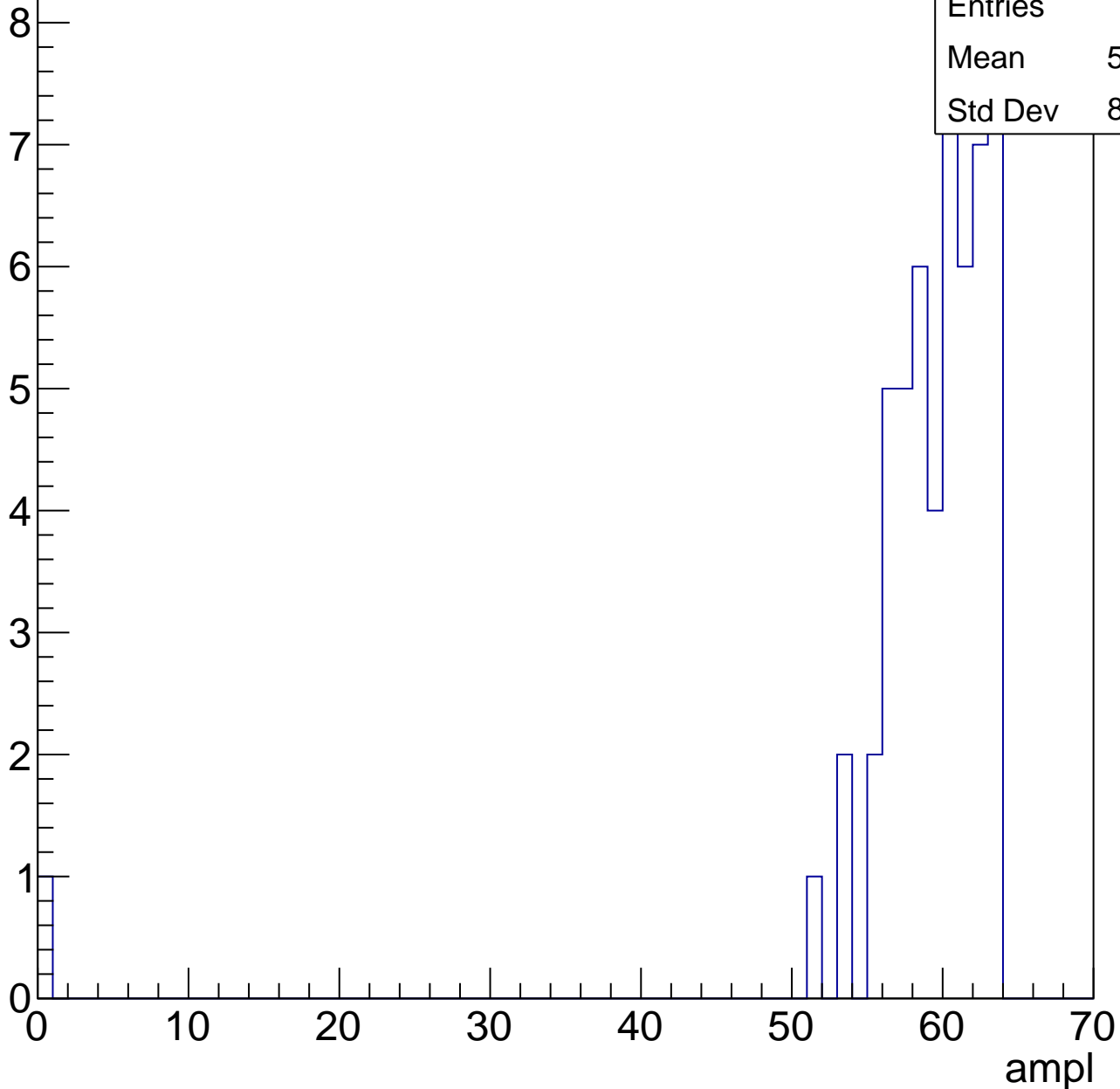


B1L103S, U12-ch52, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	58.18
Std Dev	8.427



B1L103S, U12-ch52, adc6

calib_packv5_041523_1651.root, FC#0, port C2

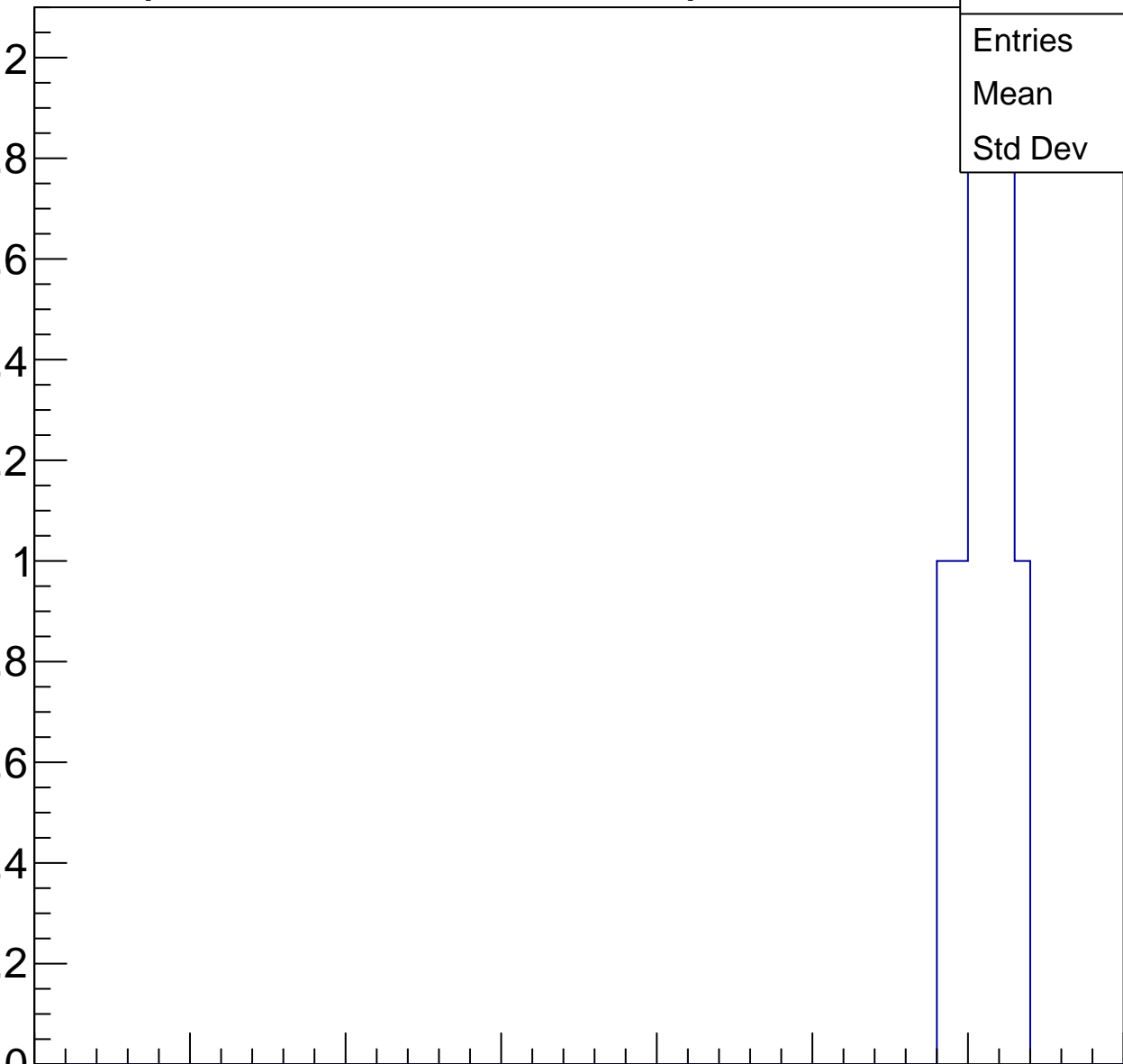
Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	9
Mean	60.67
Std Dev	1.491

0 10 20 30 40 50 60 70

ampl



B1L103S, U12-ch52, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.15
Std Dev	13.73

Entry

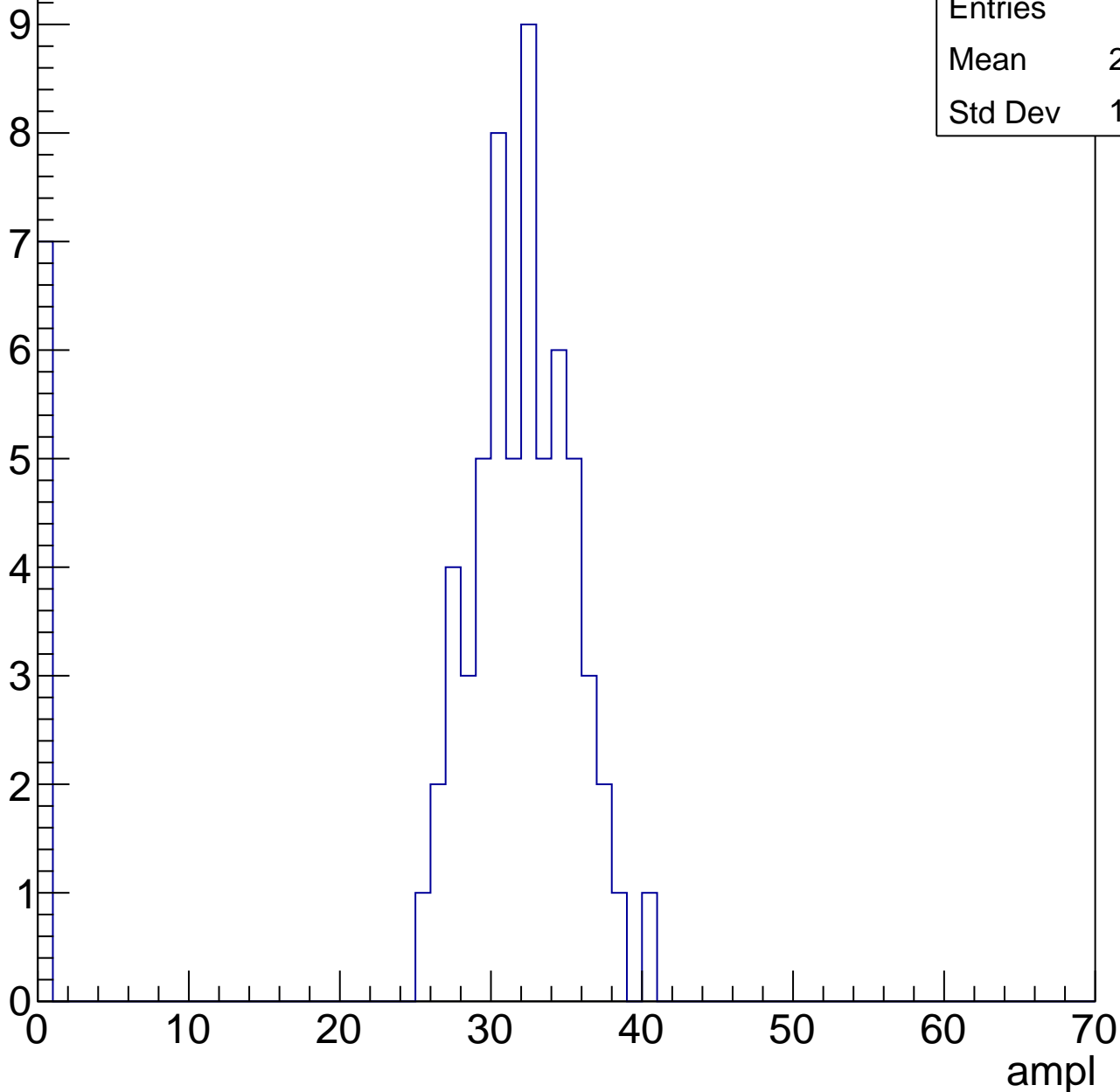


B1L103S, U12-ch53, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	28.37
Std Dev	10.16

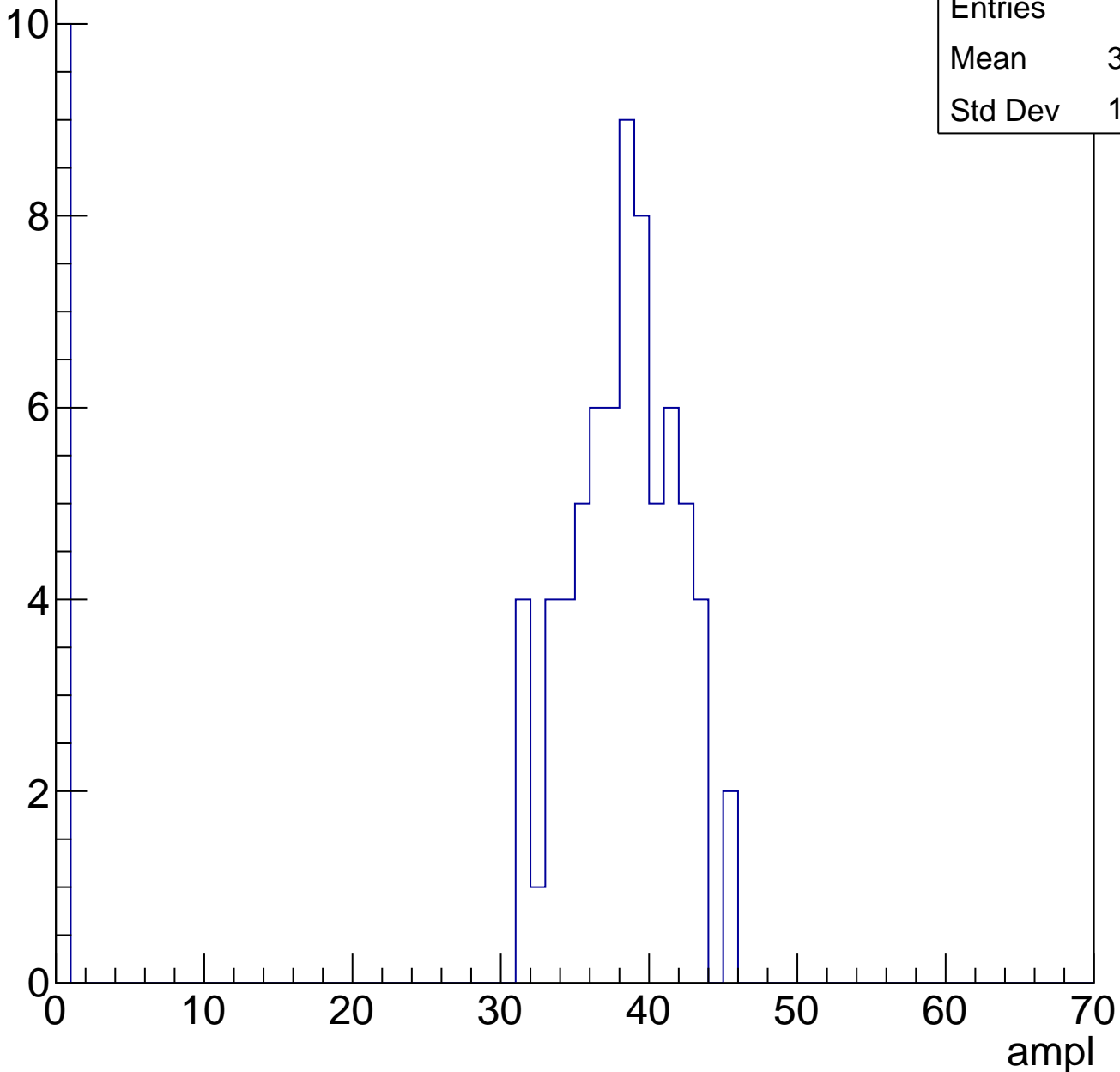


B1L103S, U12-ch53, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	79
Mean	33.03
Std Dev	12.98

Entry

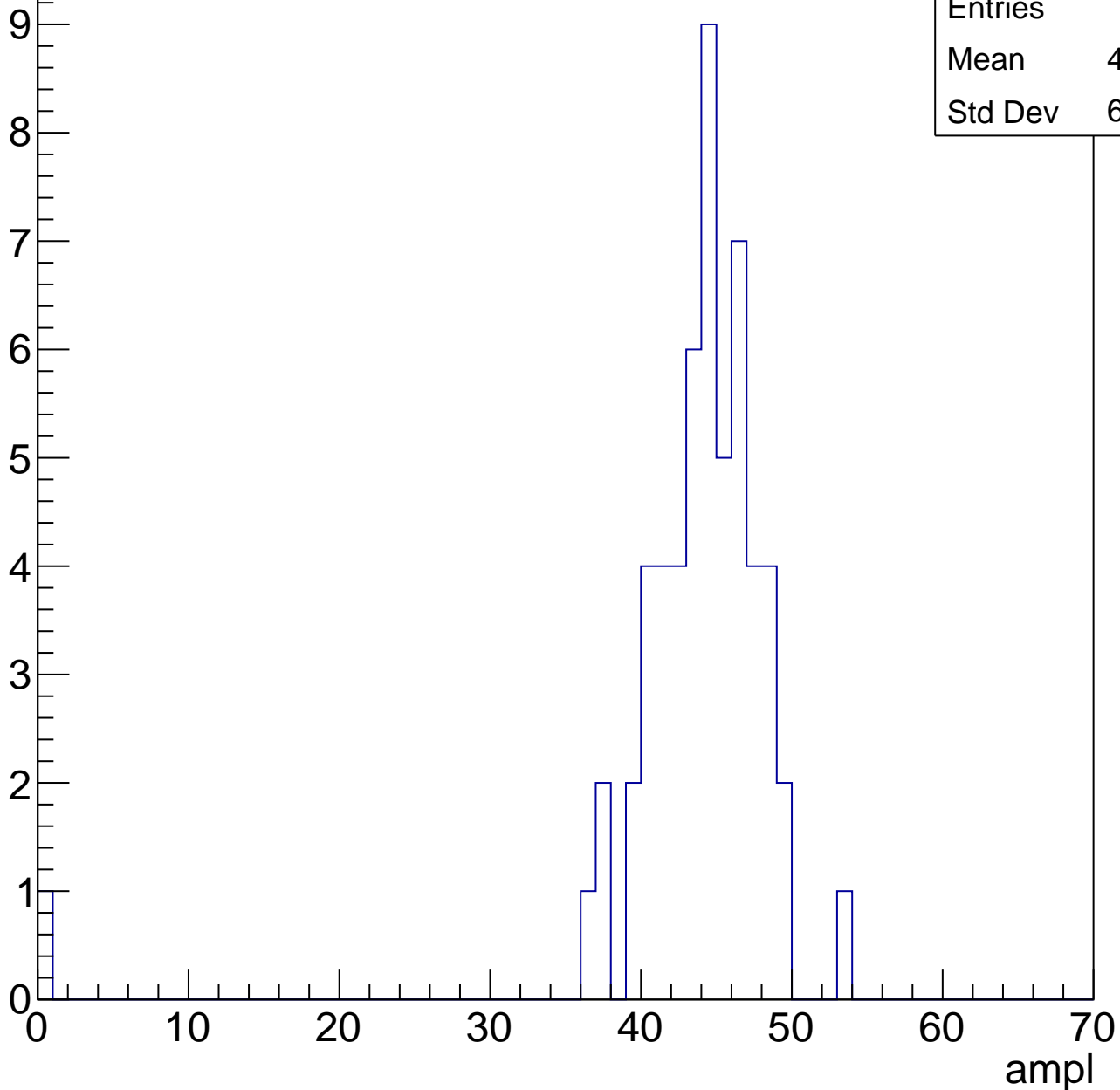


B1L103S, U12-ch53, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	56
Mean	43.07
Std Dev	6.662

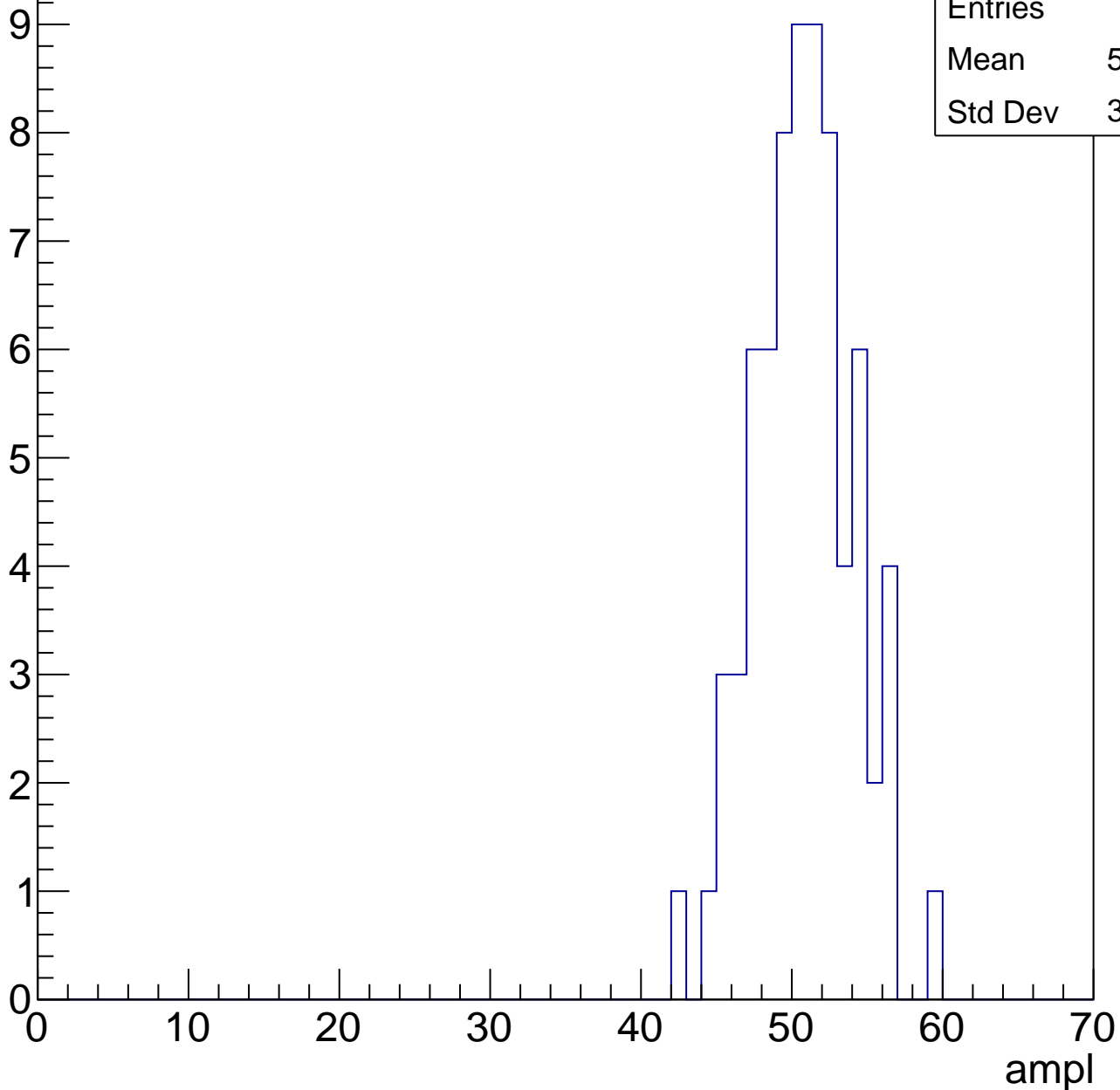


B1L103S, U12-ch53, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	50.35
Std Dev	3.246

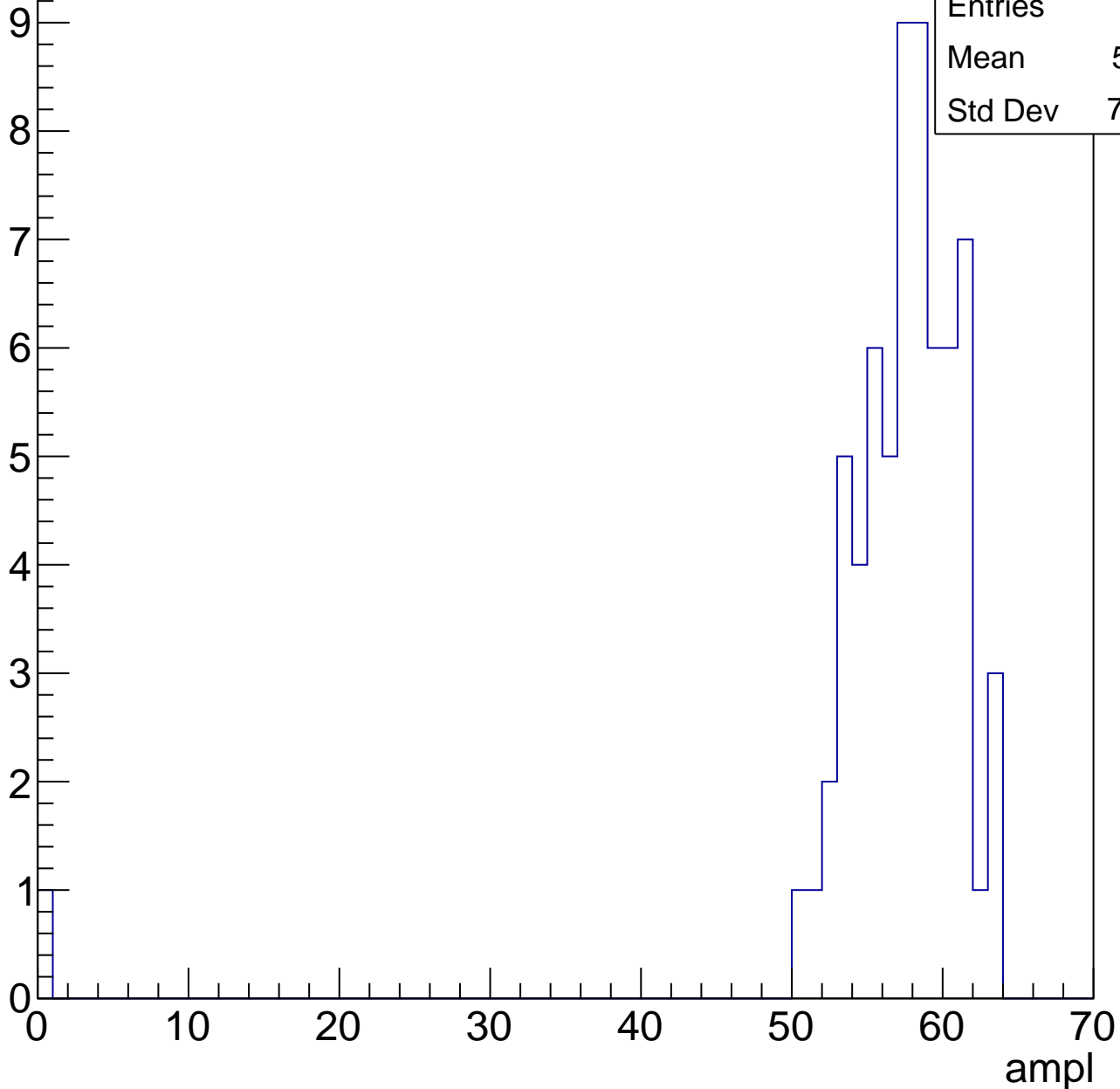


B1L103S, U12-ch53, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	56.41
Std Dev	7.626

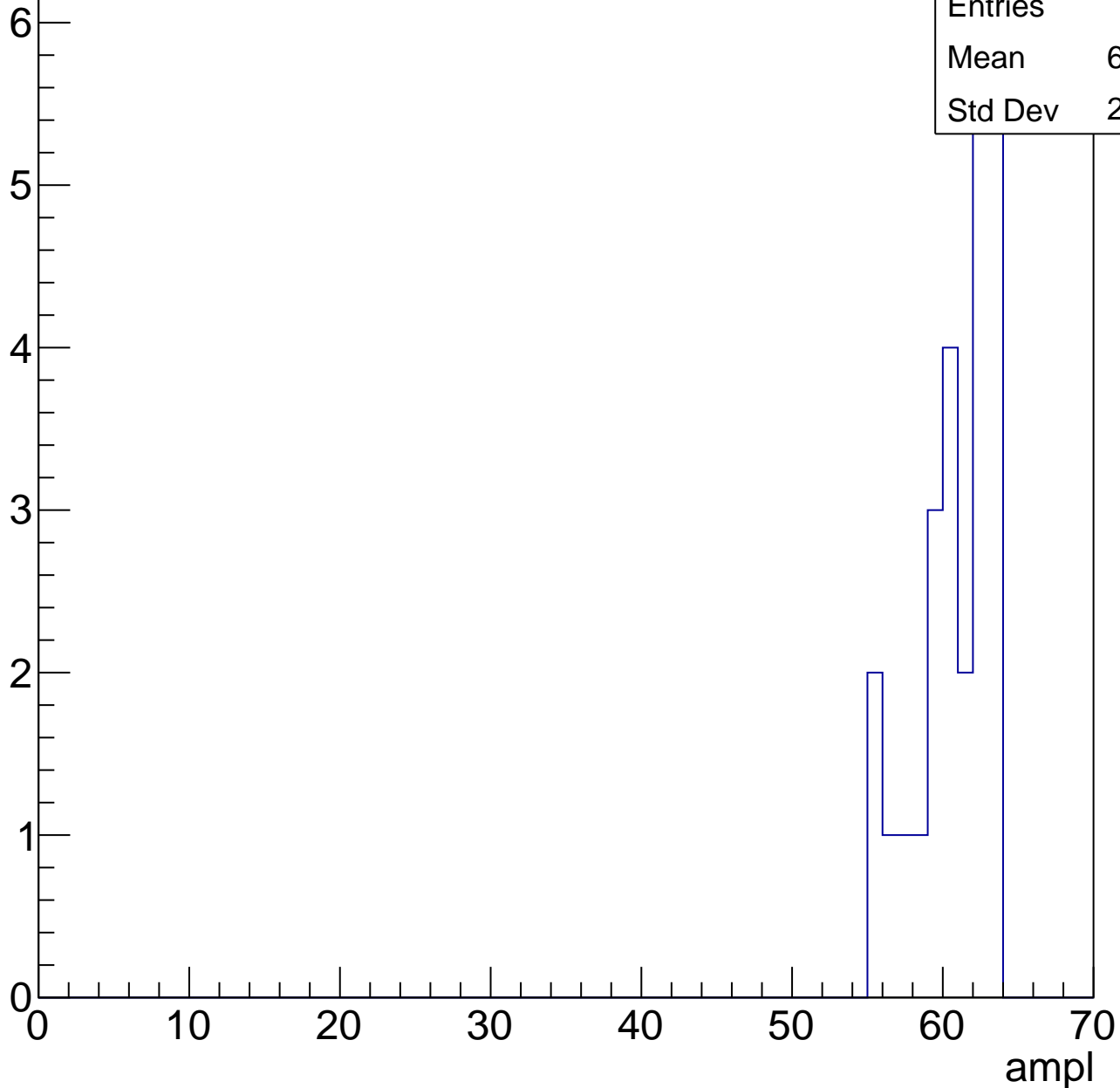


B1L103S, U12-ch53, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

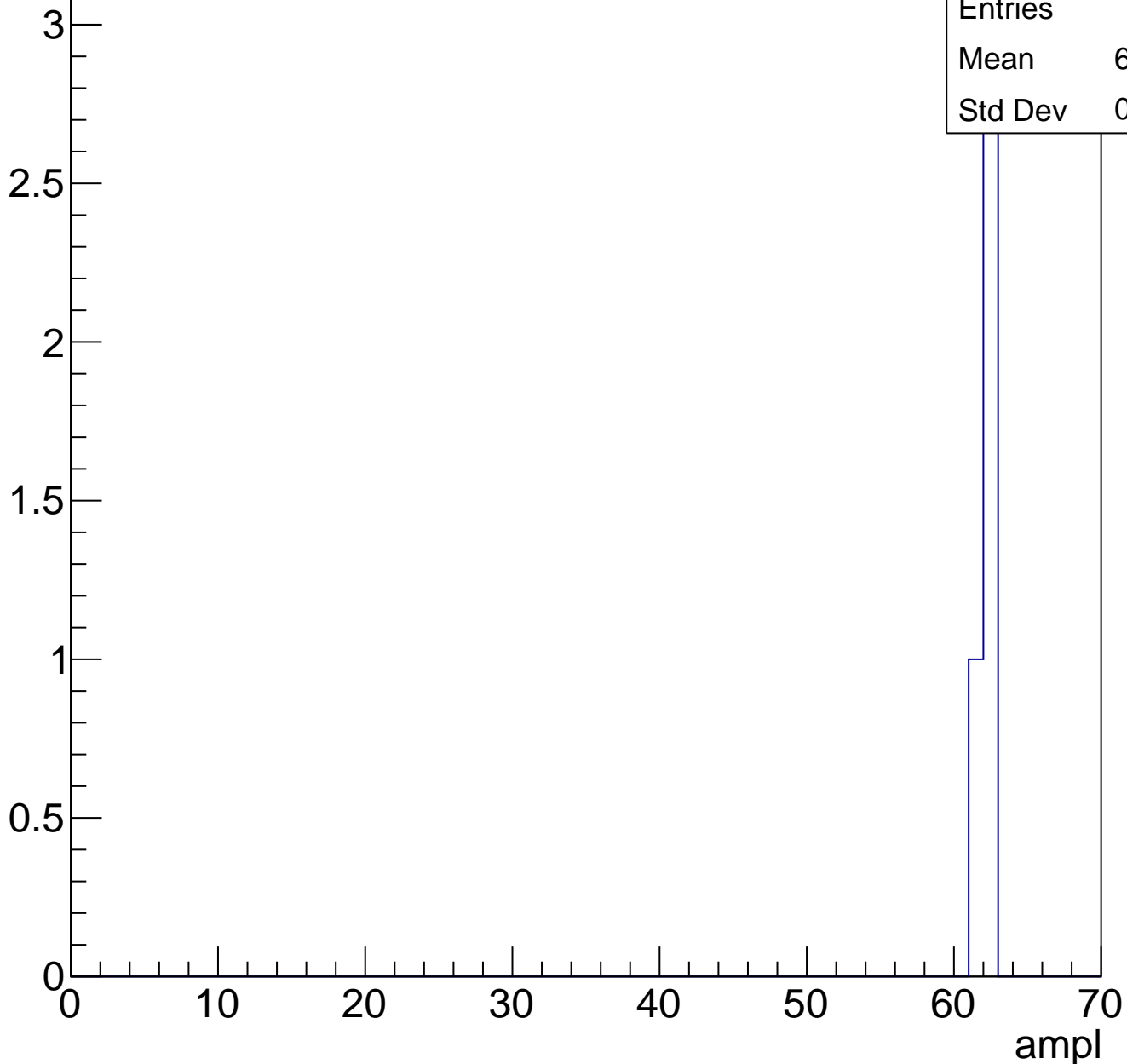
Entries	26
Mean	60.38
Std Dev	2.466



B1L103S, U12-ch53, adc6

calib_packv5_041523_1651.root, FC#0, port C2

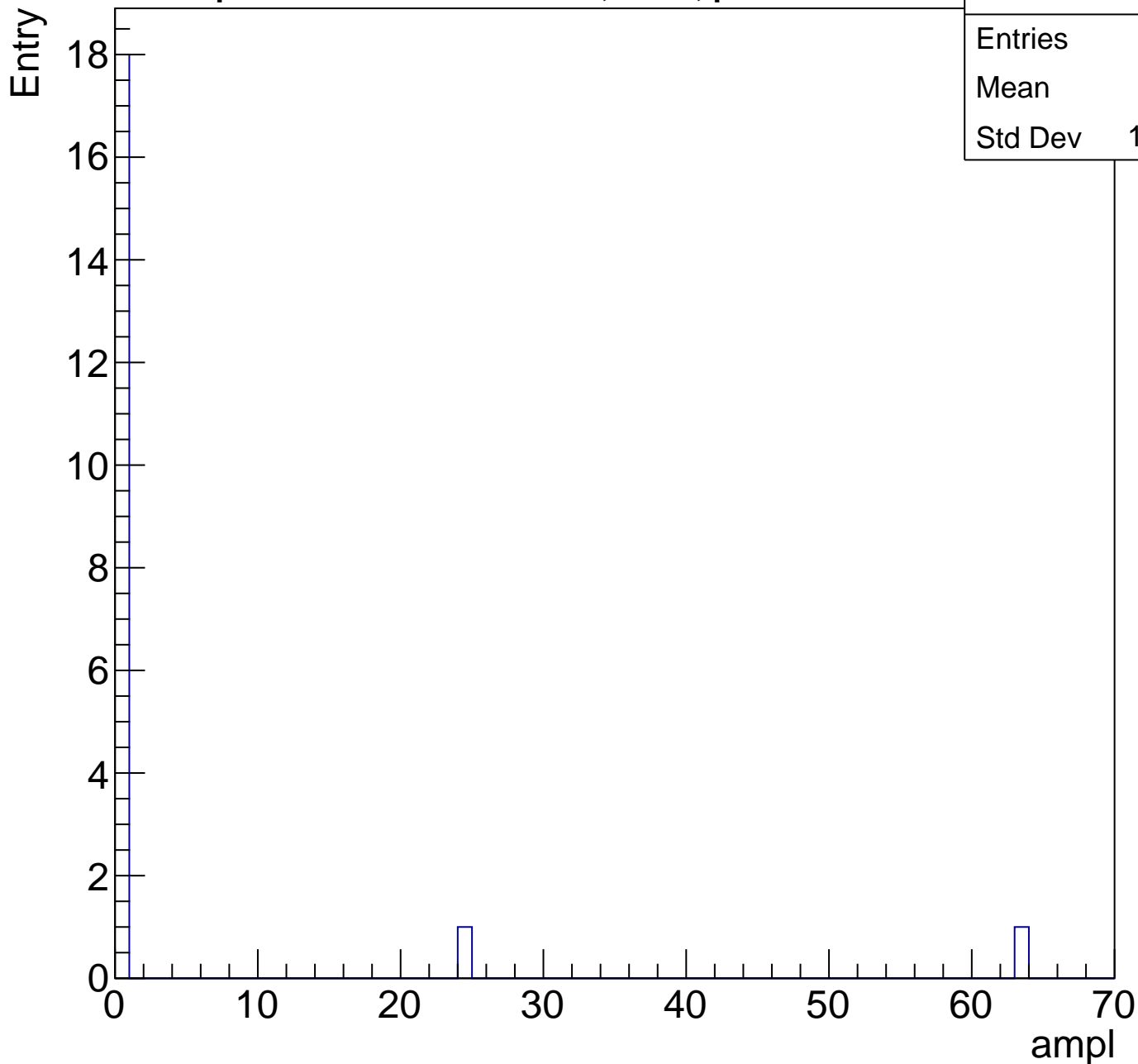
Entry



B1L103S, U12-ch53, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	4.35
Std Dev	14.43

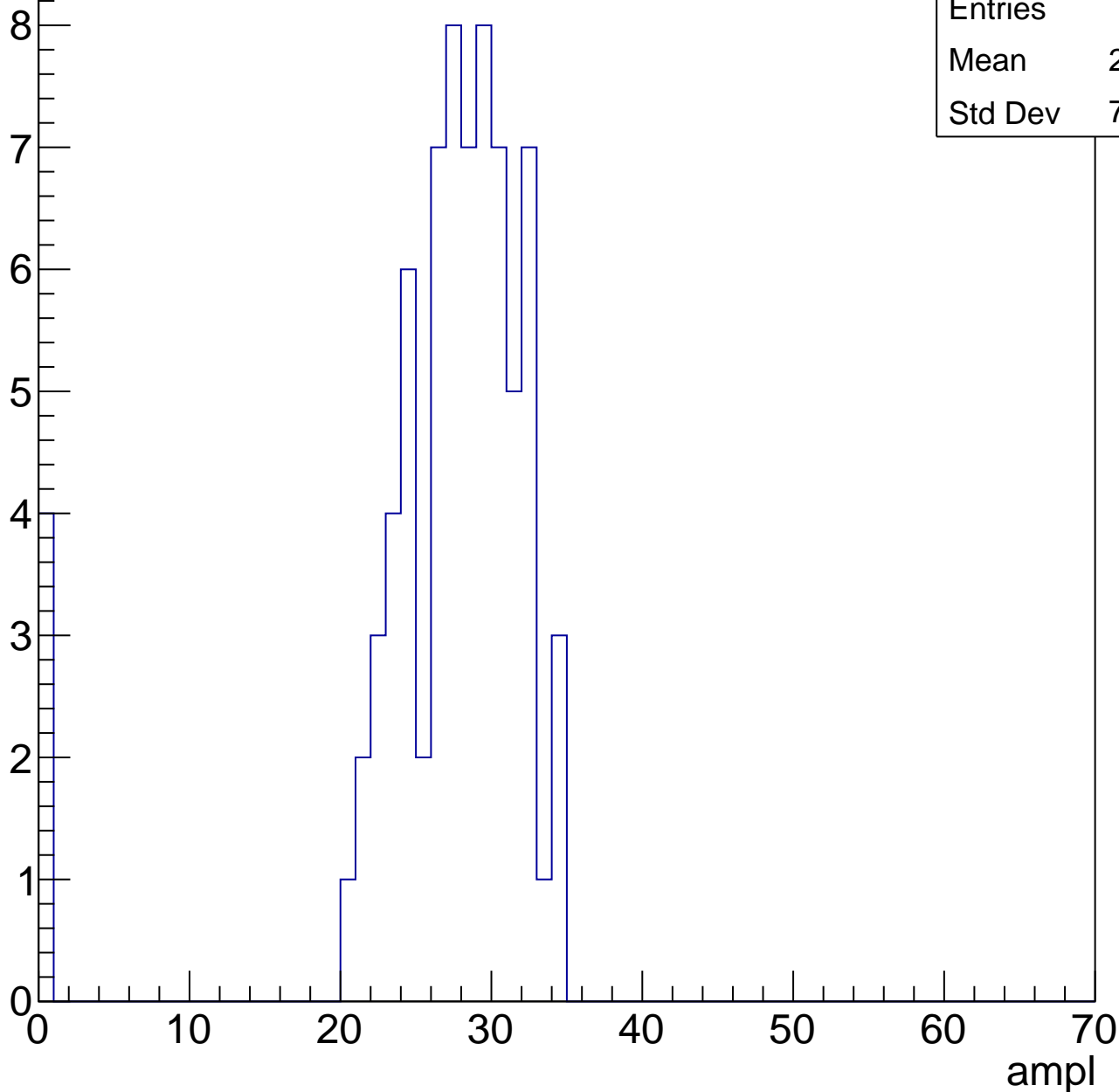


B1L103S, U12-ch54, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	75
Mean	26.19
Std Dev	7.057

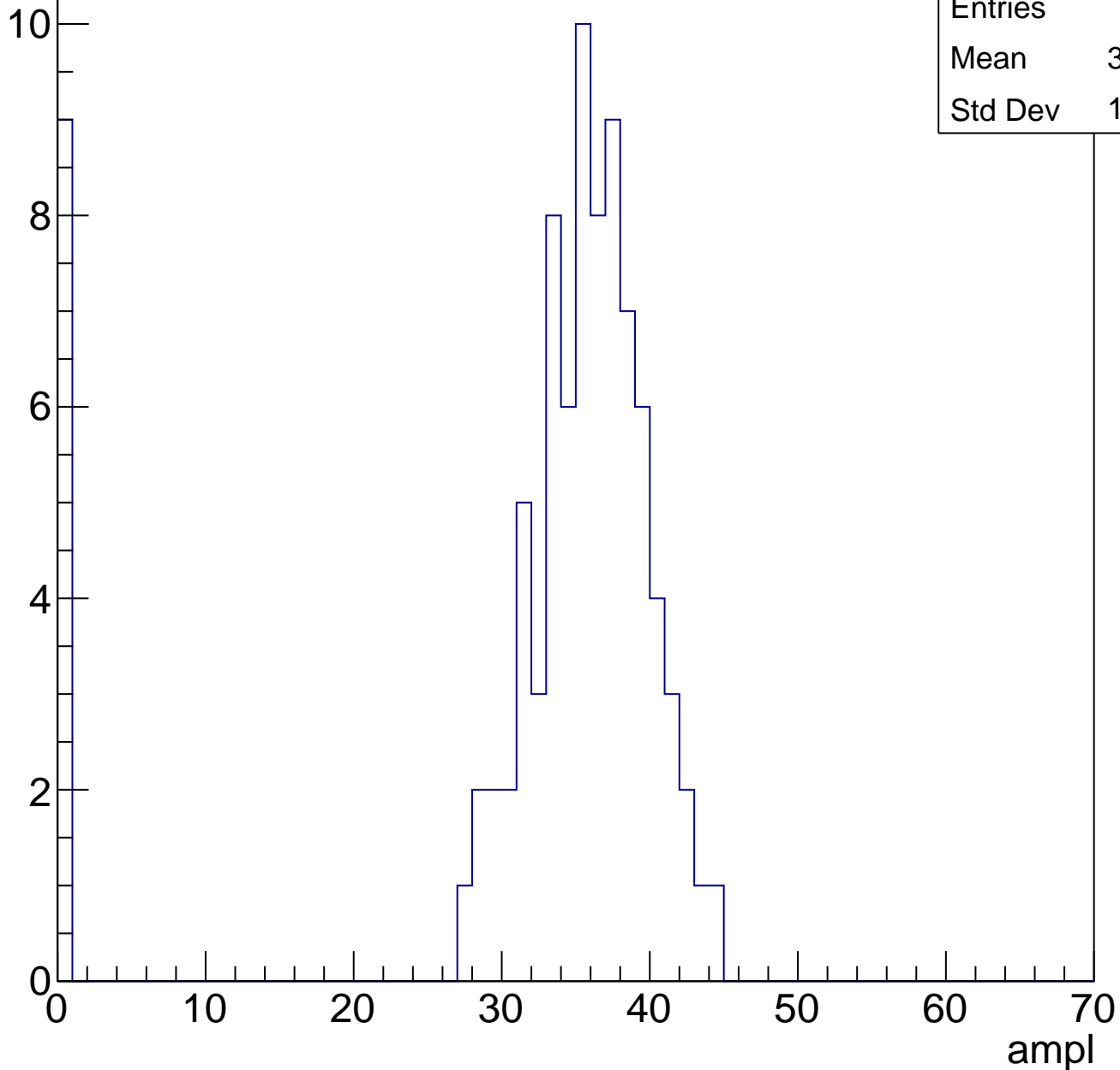


B1L103S, U12-ch54, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	89
Mean	31.97
Std Dev	11.26

Entry

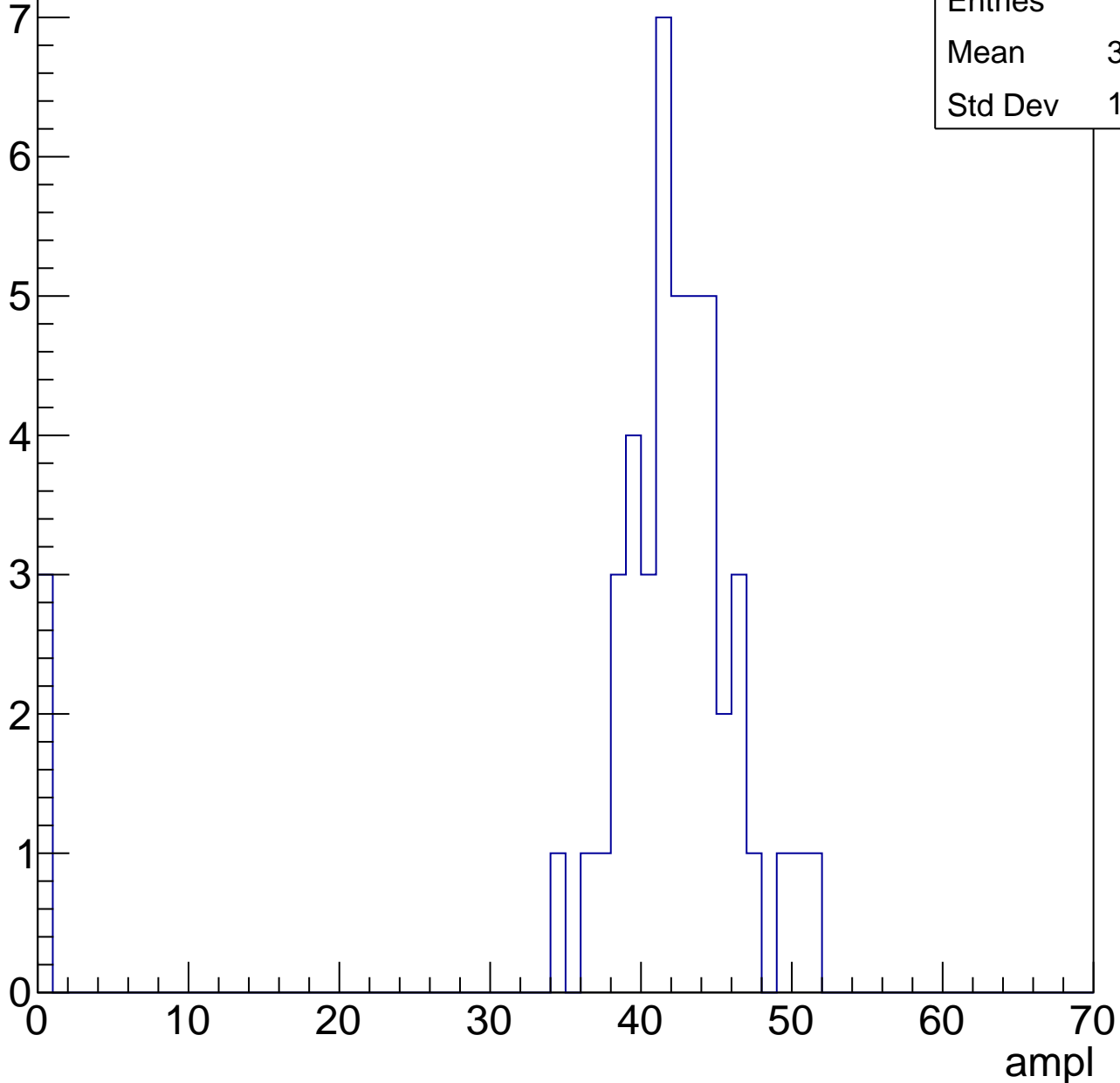


B1L103S, U12-ch54, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

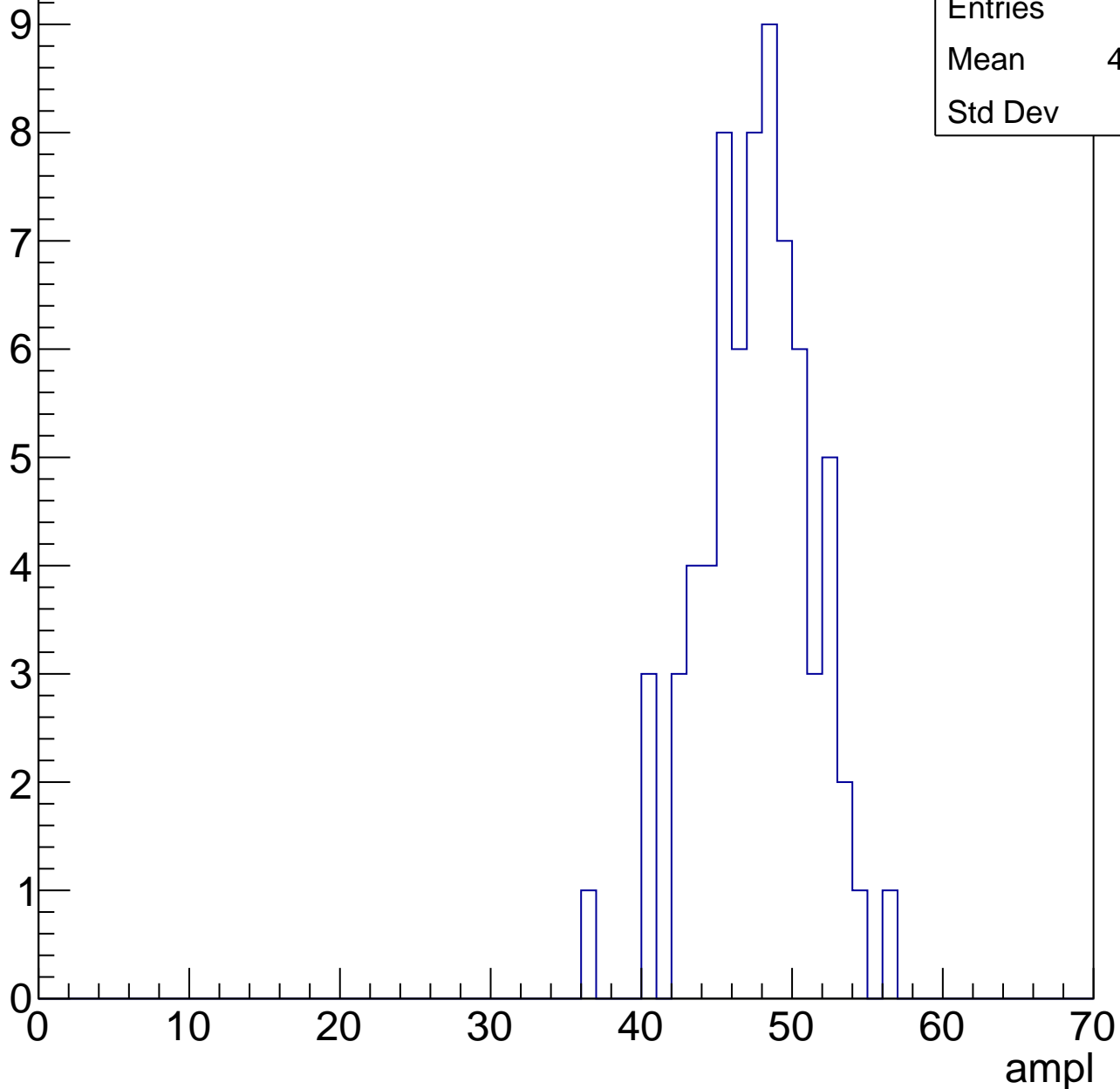
Entries	47
Mean	39.45
Std Dev	10.84



B1L103S, U12-ch54, adc3

calib_packv5_041523_1651.root, FC#0, port C2

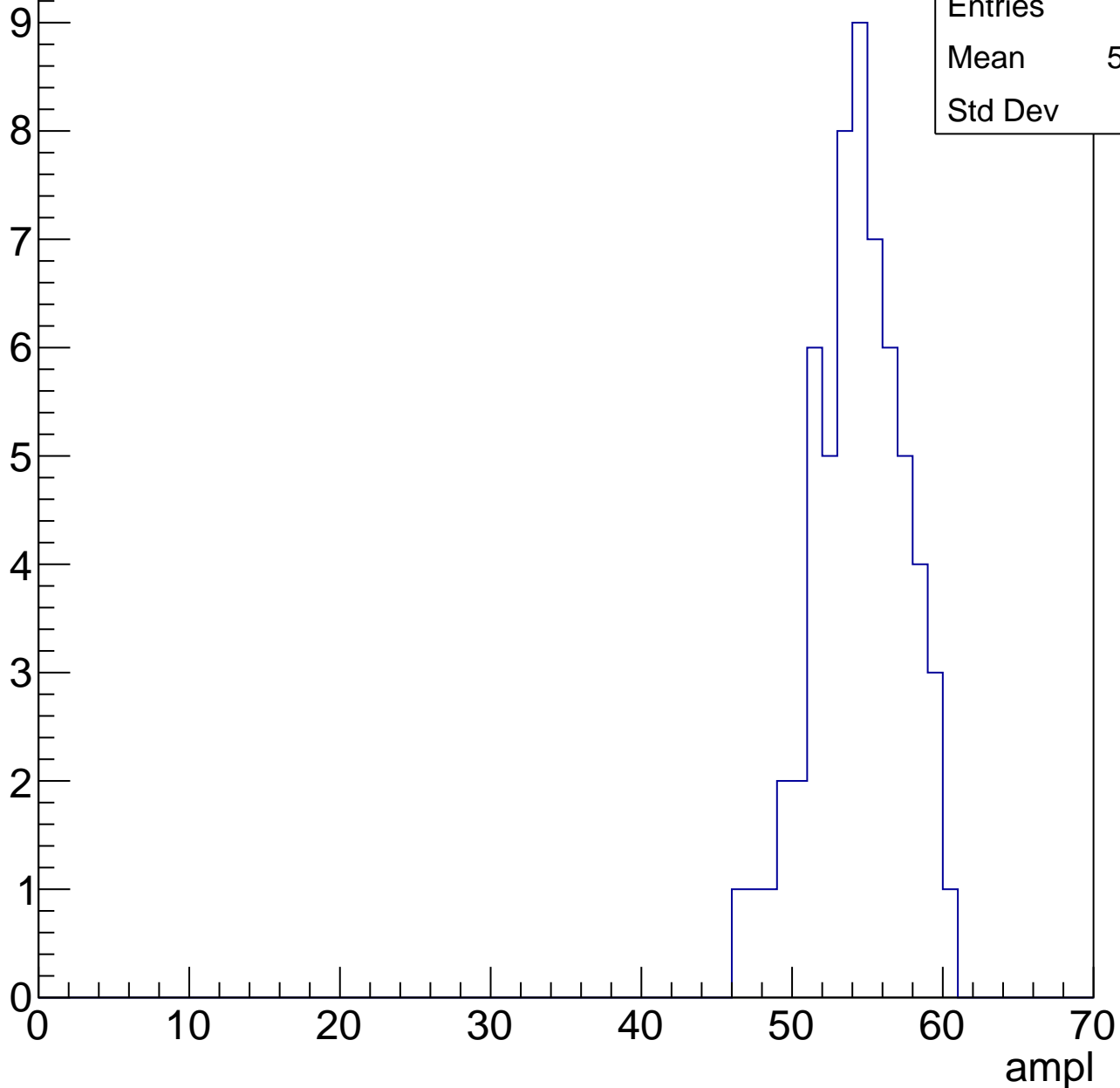
Entry



B1L103S, U12-ch54, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry



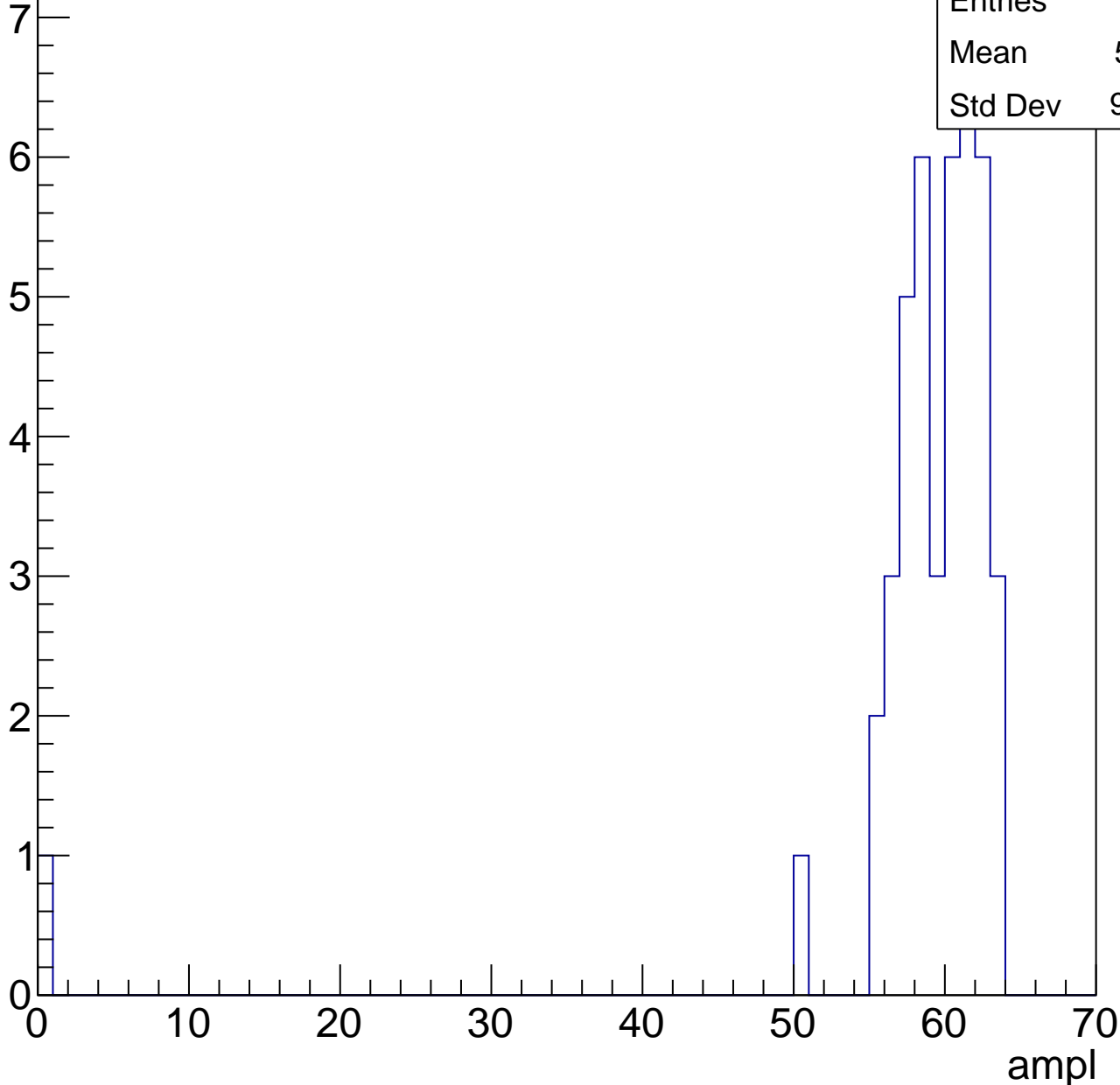
Entries	61
Mean	53.93
Std Dev	3.04

B1L103S, U12-ch54, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	43
Mean	57.81
Std Dev	9.304

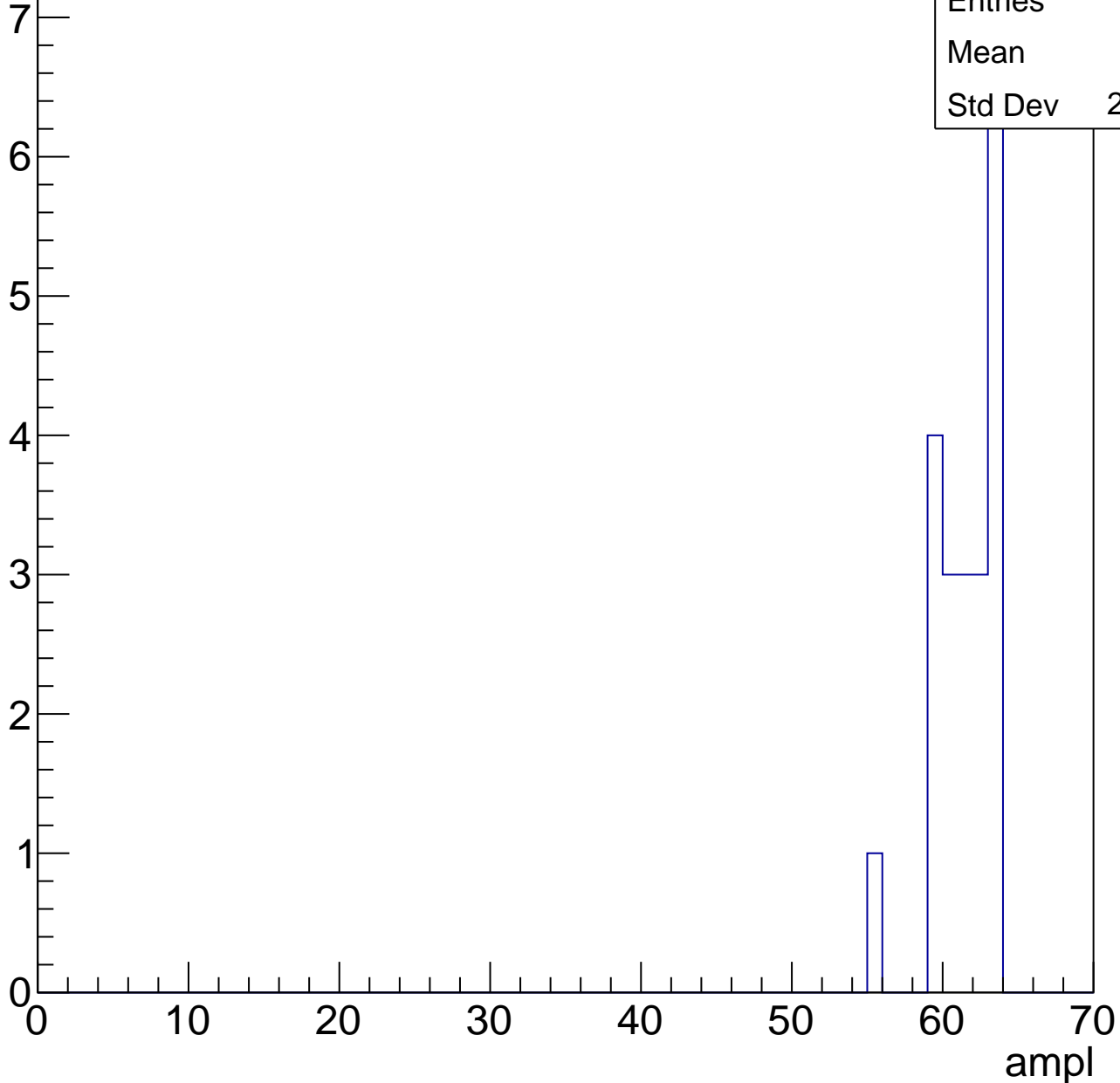


B1L103S, U12-ch54, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	21
Mean	61
Std Dev	2.024



B1L103S, U12-ch54, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	3.263
Std Dev	13.84

Entry



B1L103S, U12-ch55, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	89
Mean	22.21
Std Dev	13.02

Entry

22
20
18
16
14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70

B1L103S, U12-ch55, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	69
Mean	29.83
Std Dev	13.38

Entry

10

8

6

4

2

0

0

10

20

30

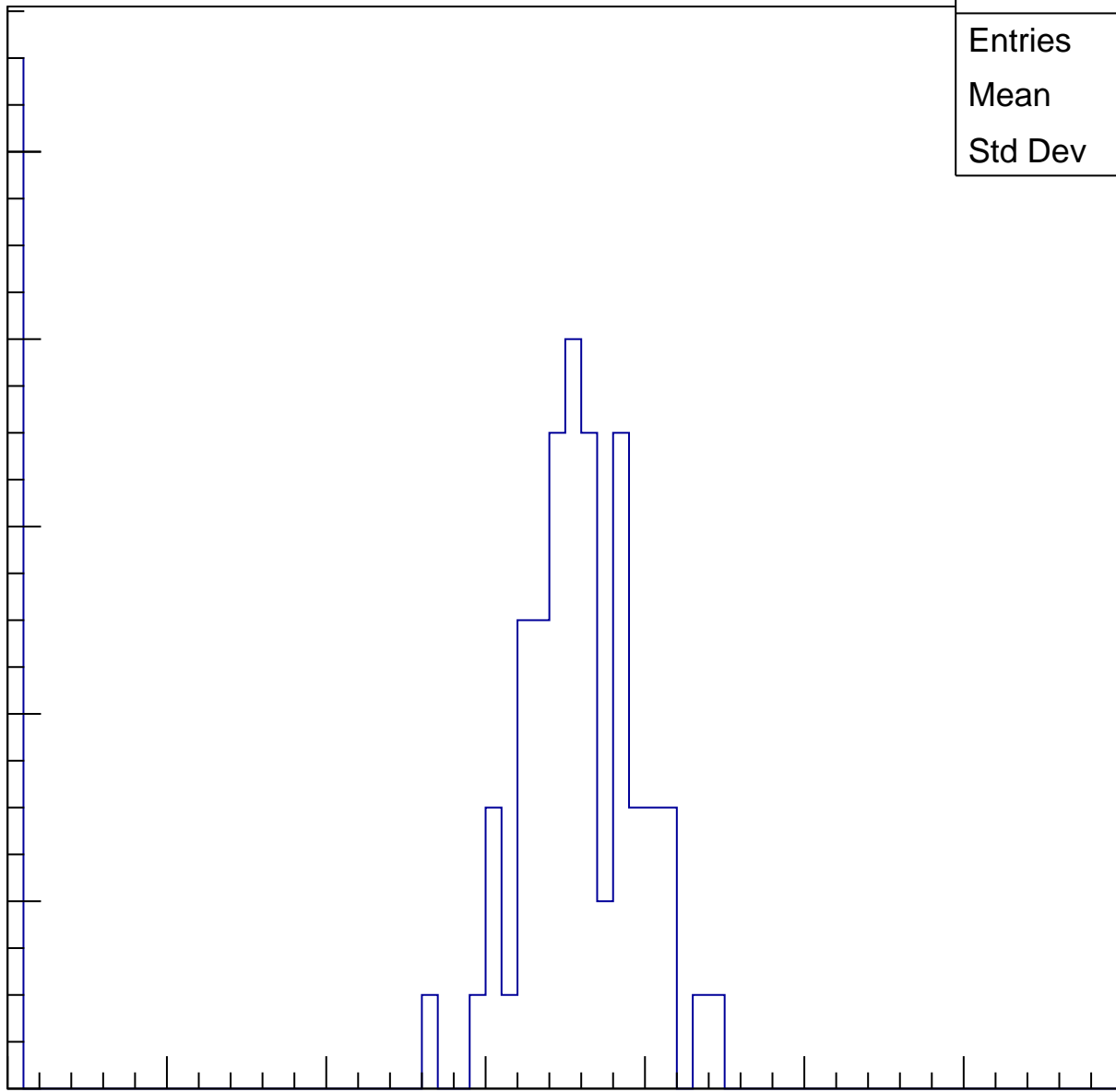
40

50

60

70

ampl

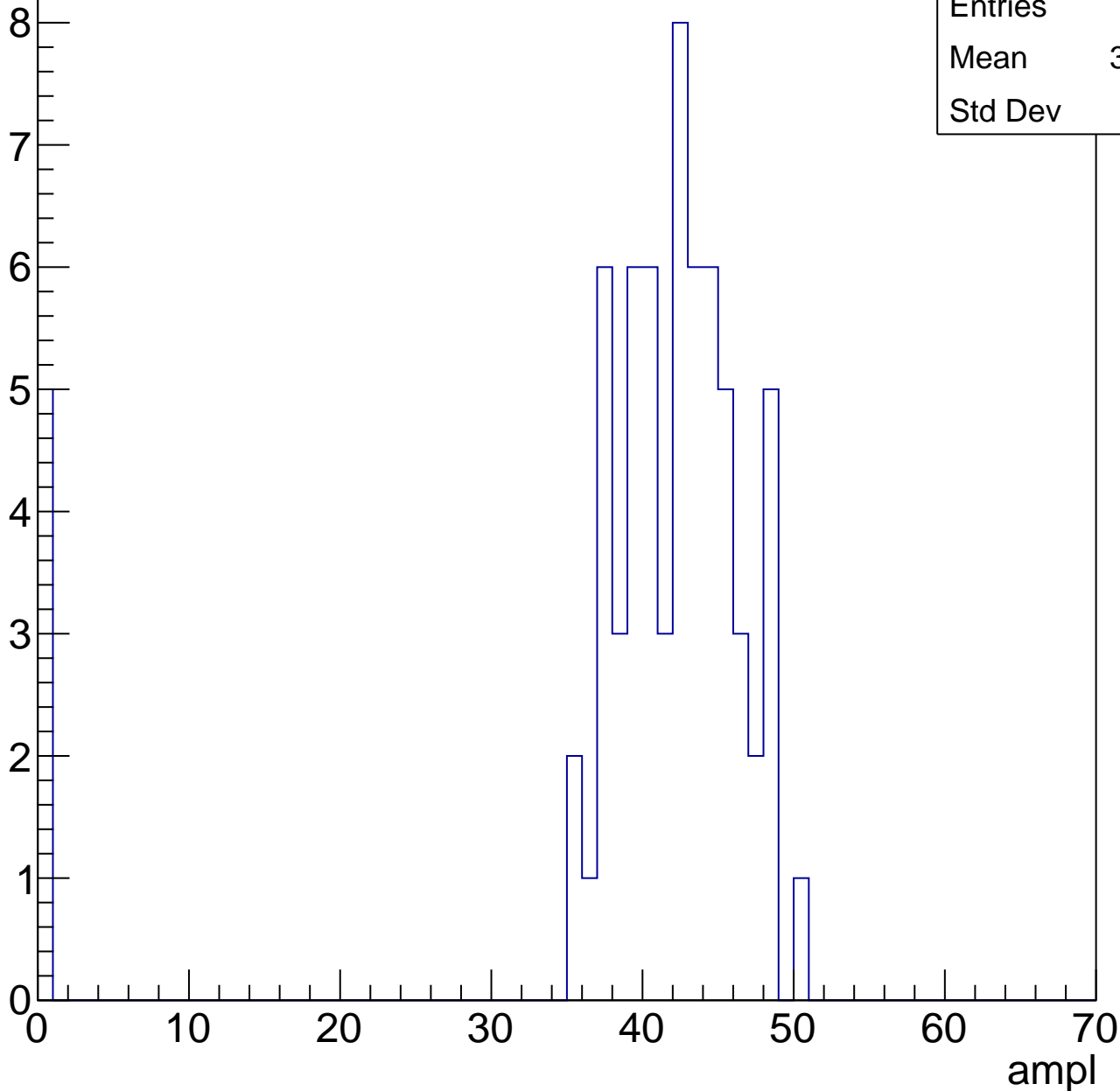


B1L103S, U12-ch55, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	38.88
Std Dev	11.5



B1L103S, U12-ch55, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	92
Mean	48.92
Std Dev	4.092

Entry

10

8

6

4

2

0

0

10

20

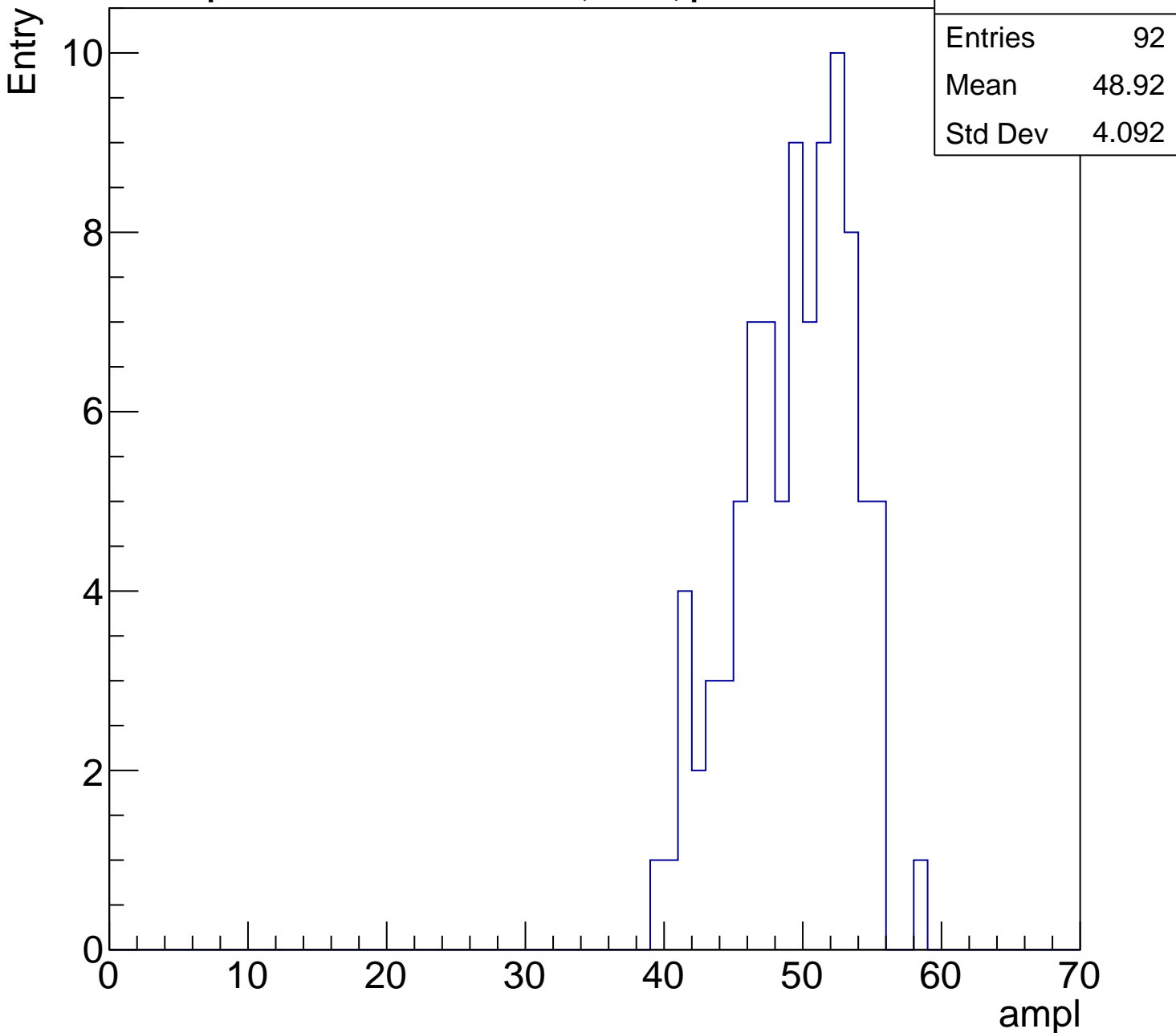
30

40

50

60

ampl

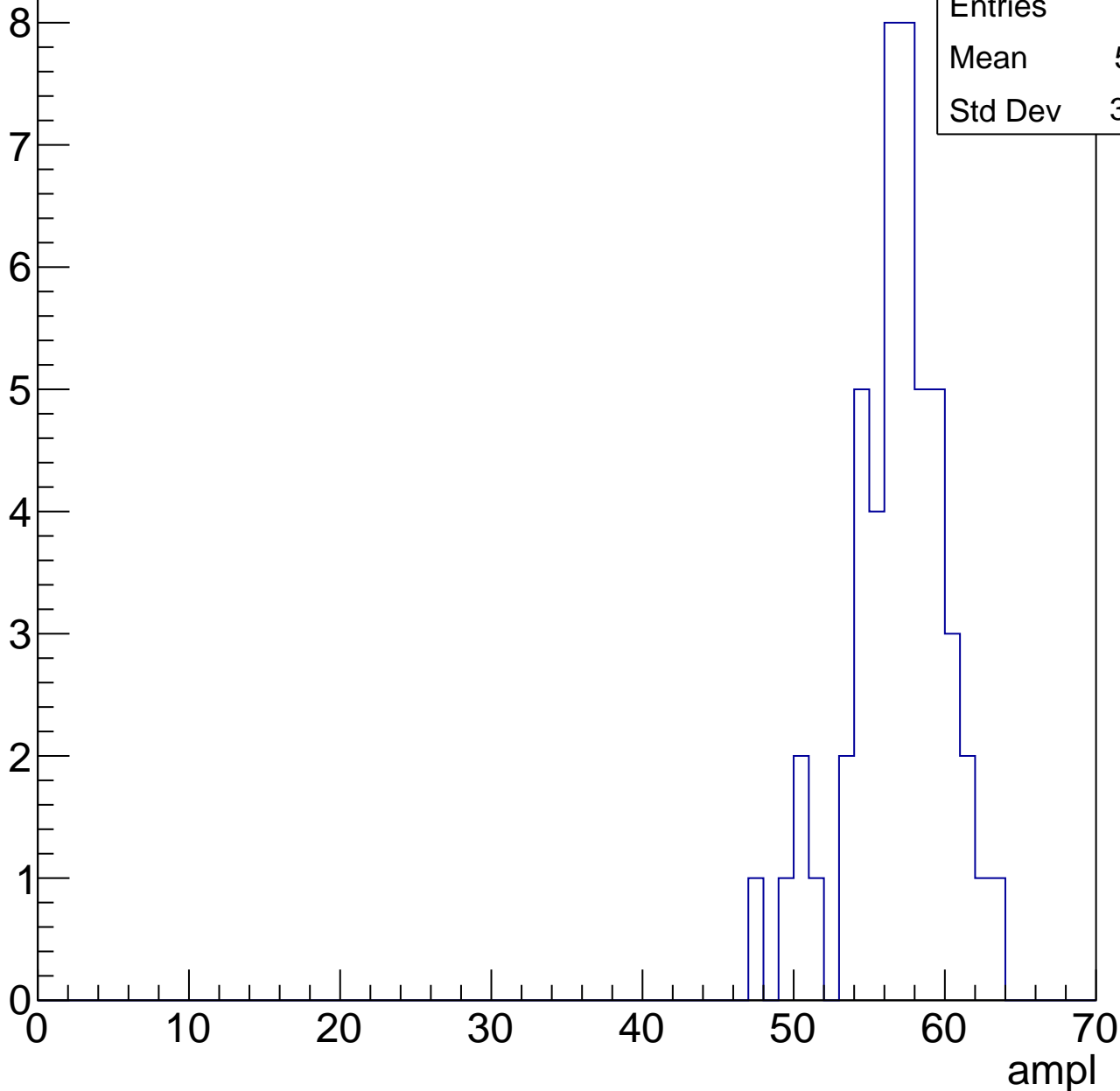


B1L103S, U12-ch55, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	49
Mean	56.31
Std Dev	3.259

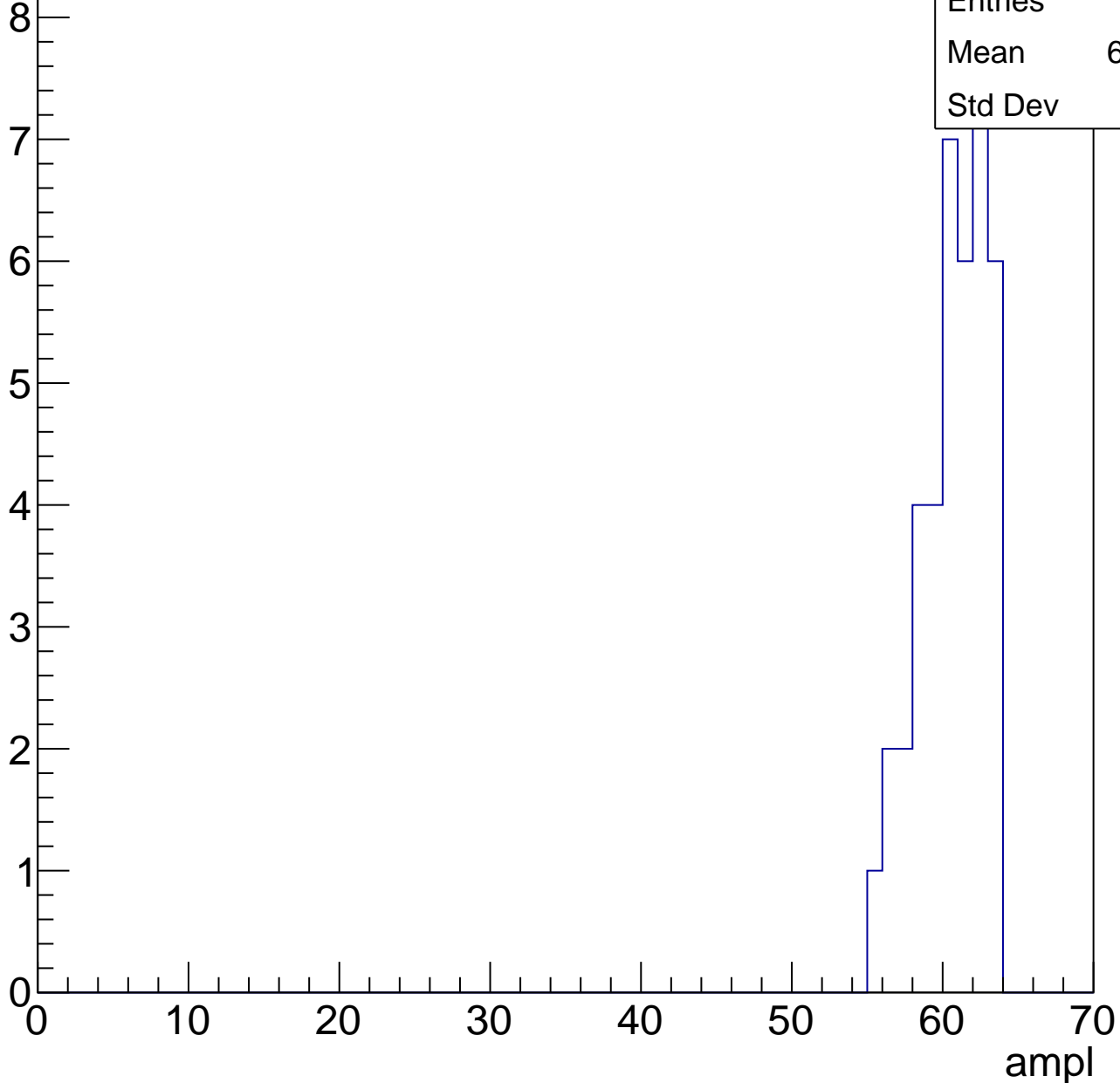


B1L103S, U12-ch55, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	40
Mean	60.23
Std Dev	2.15



B1L103S, U12-ch55, adc6

calib_packv5_041523_1651.root, FC#0, port C2

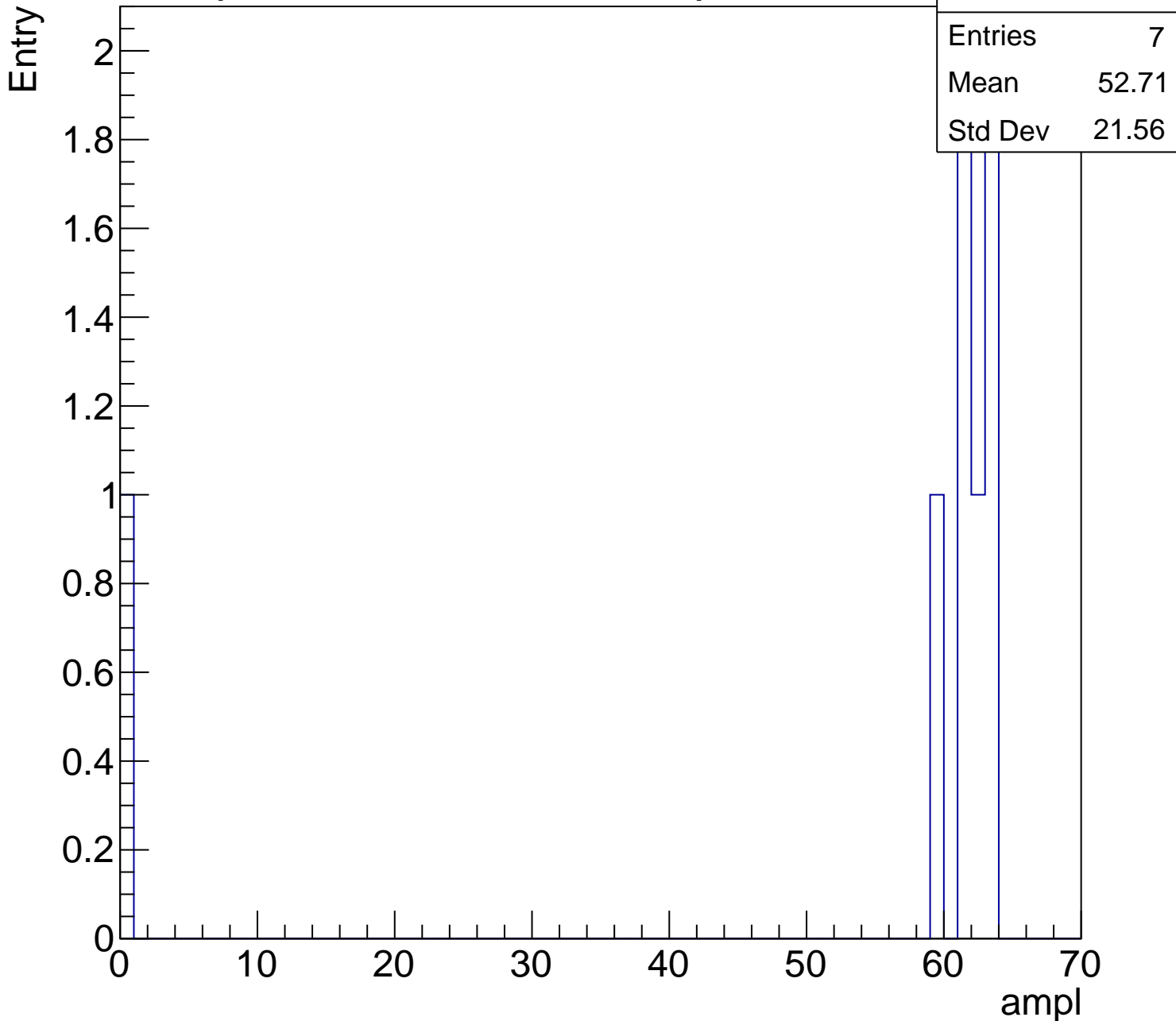
Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	7
Mean	52.71
Std Dev	21.56

0 10 20 30 40 50 60 70

ampl



B1L103S, U12-ch55, adc7

calib_packv5_041523_1651.root, FC#0, port C2

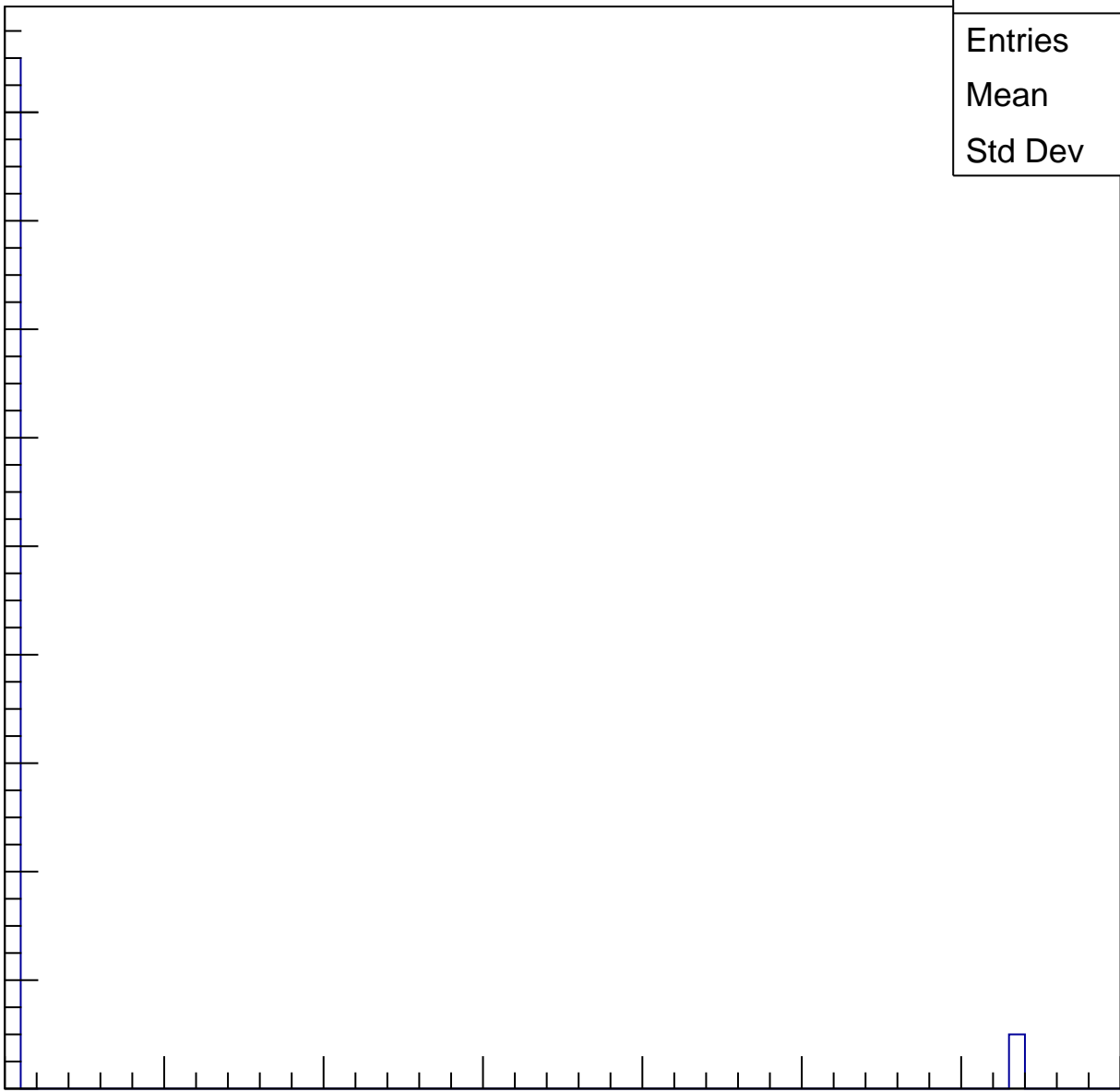
Entries	20
Mean	3.15
Std Dev	13.73

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

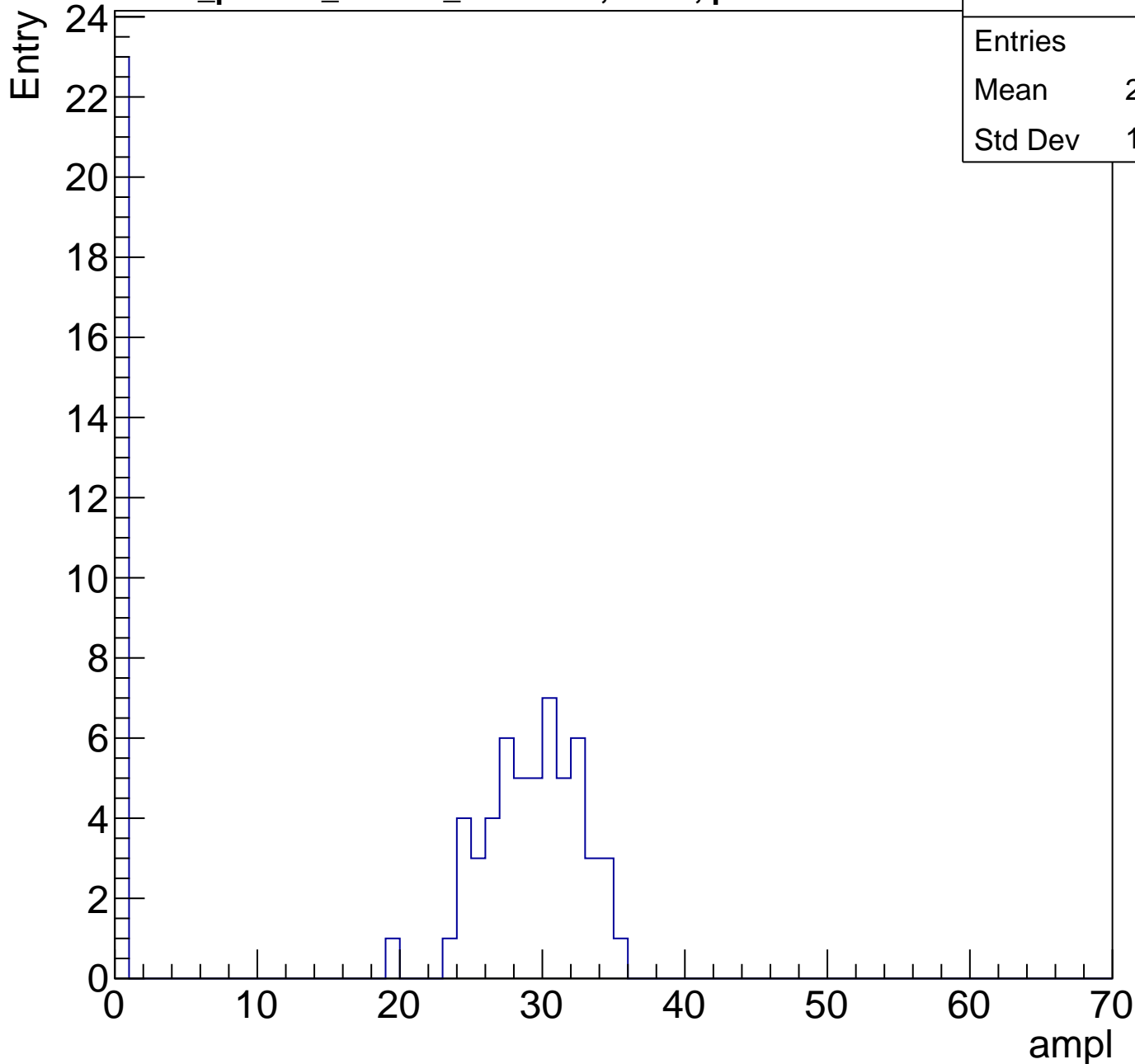
ampl



B1L103S, U12-ch56, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	77
Mean	20.22
Std Dev	13.48



B1L103S, U12-ch56, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	85
Mean	30.65
Std Dev	12.34

Entry

10

8

6

4

2

0

0

10

20

30

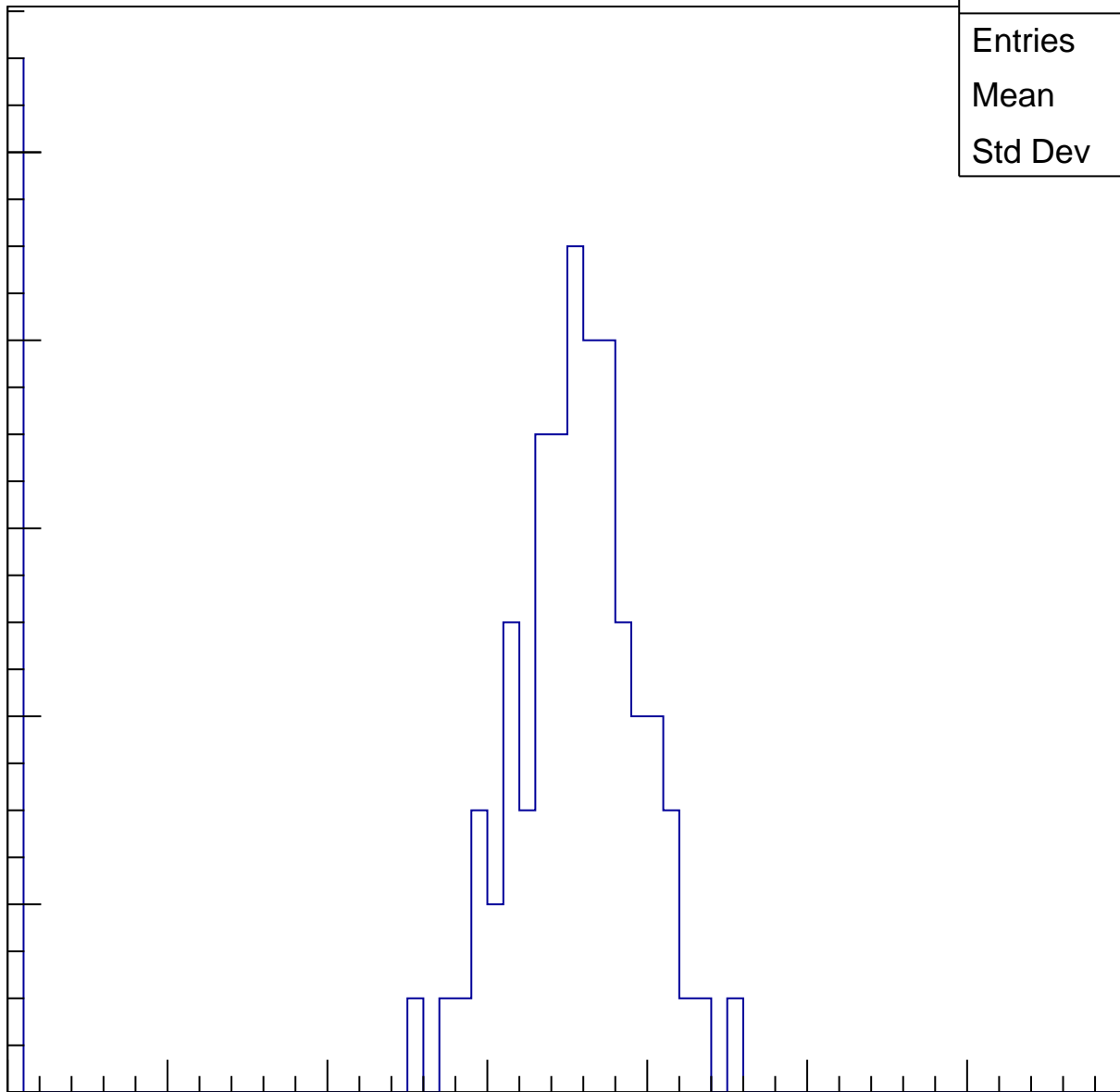
40

50

60

70

ampl

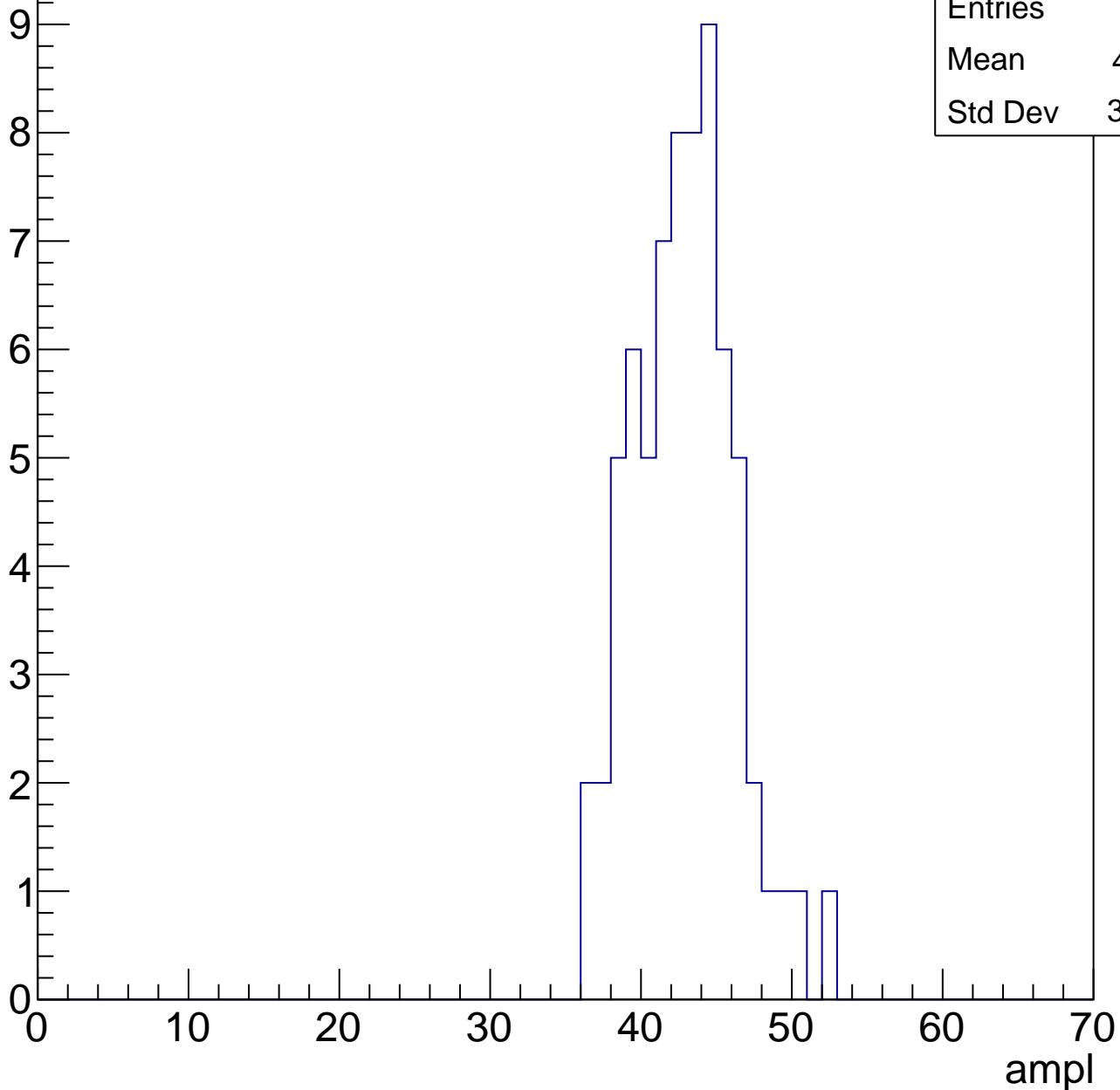


B1L103S, U12-ch56, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	42.41
Std Dev	3.294

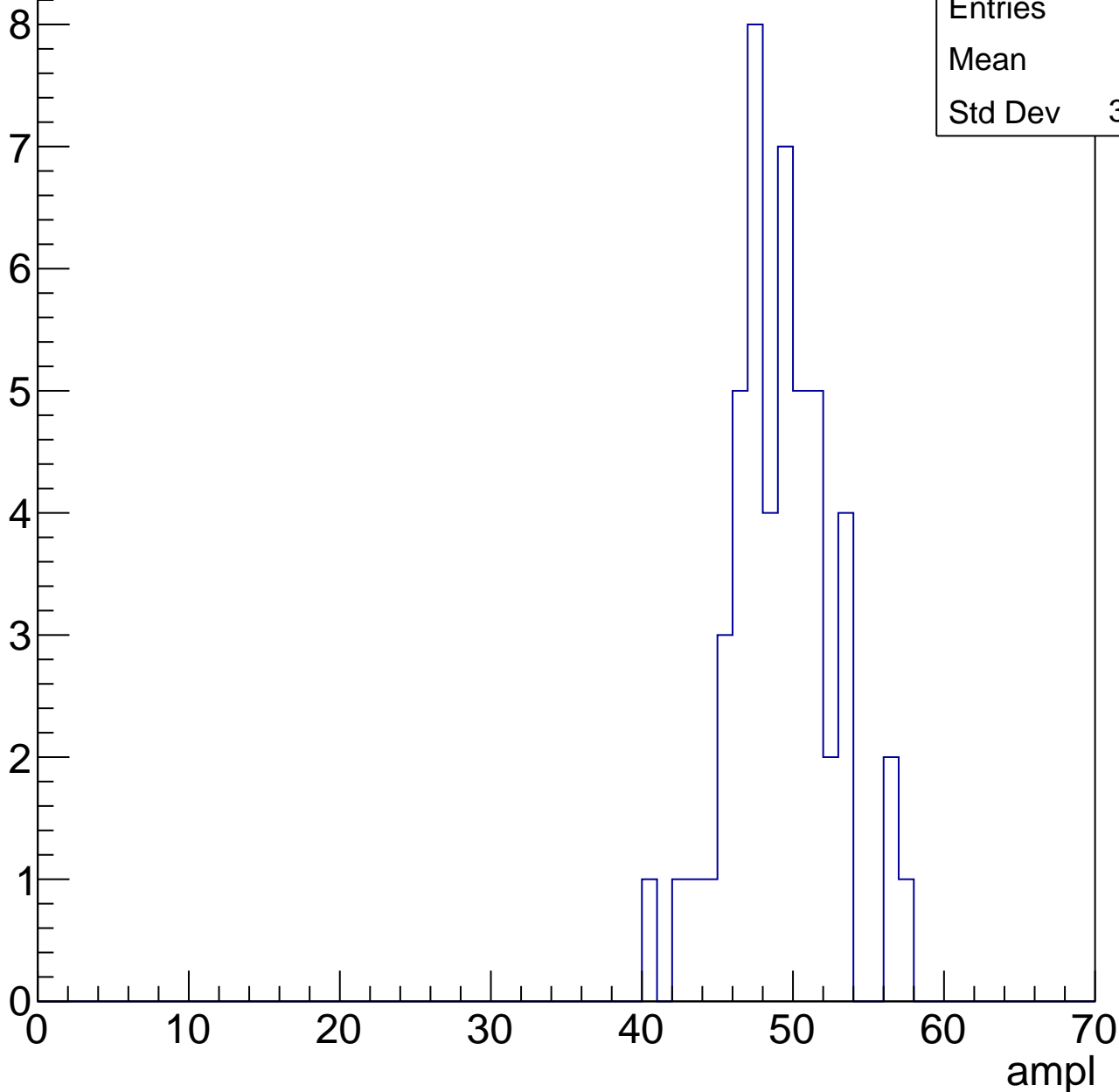


B1L103S, U12-ch56, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	50
Mean	48.7
Std Dev	3.419



B1L103S, U12-ch56, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entries	73
Mean	53.68
Std Dev	7.271

Entry

10

8

6

4

2

0

0

10

20

30

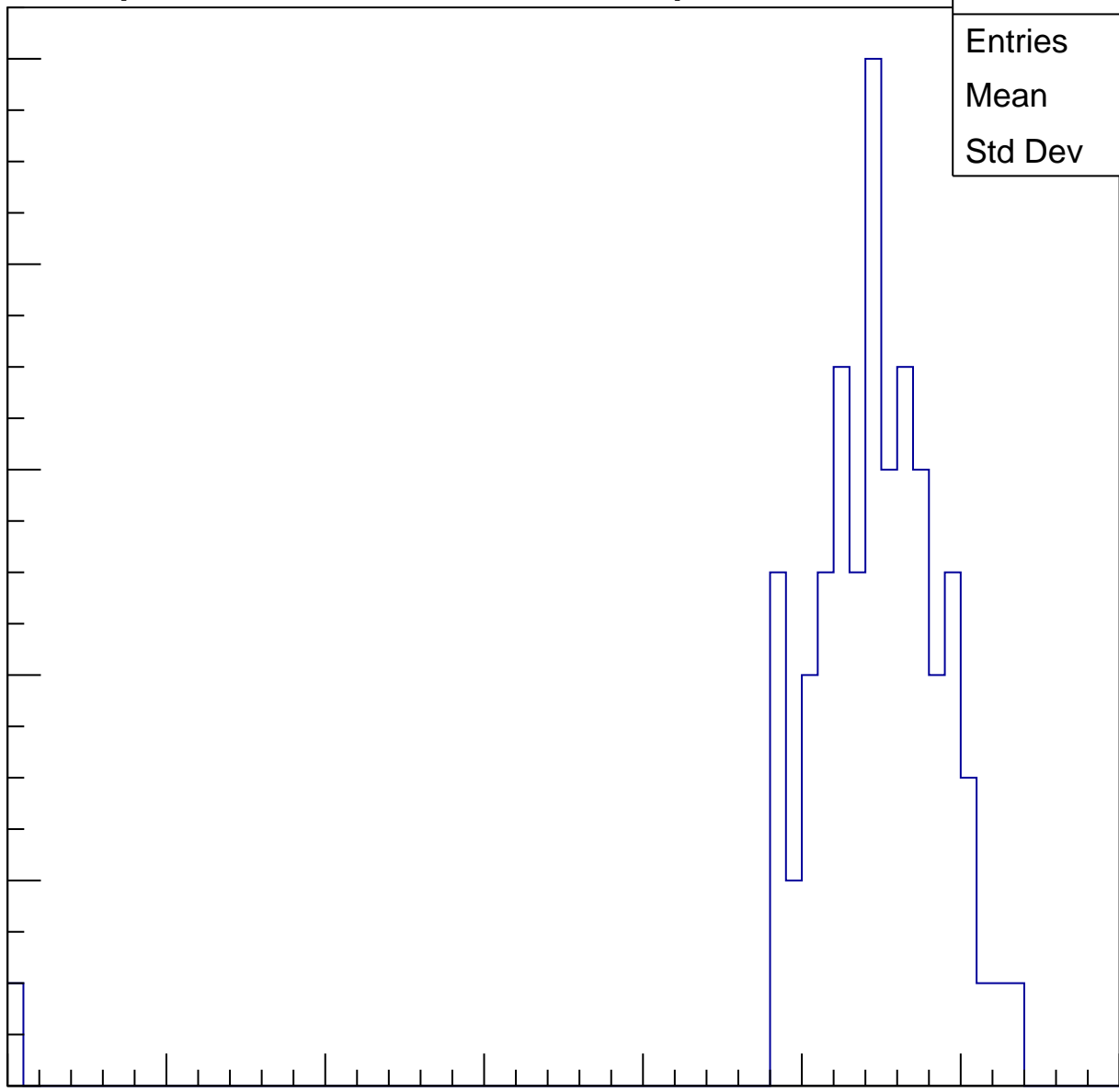
40

50

60

70

ampl

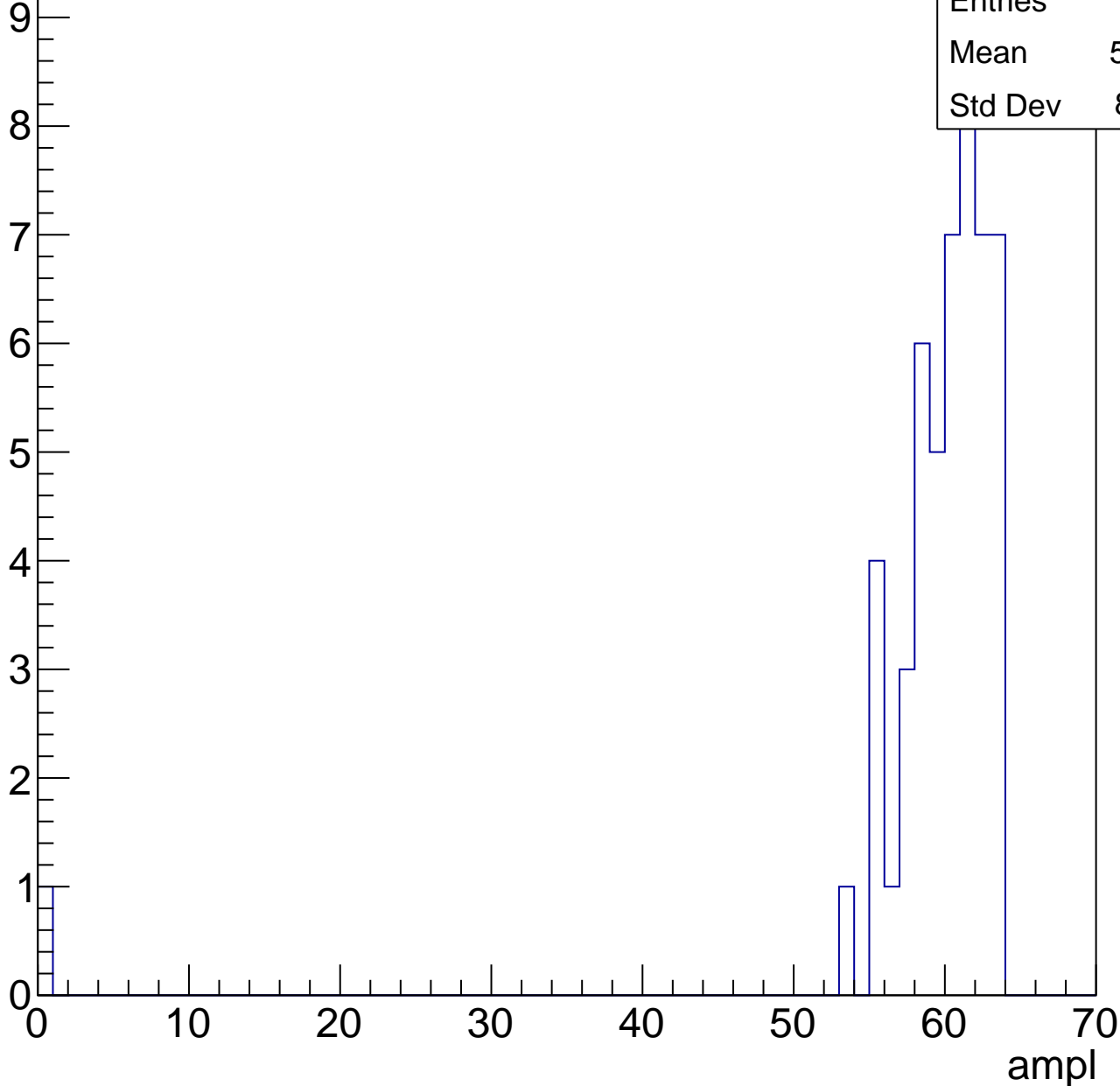


B1L103S, U12-ch56, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	51
Mean	58.57
Std Dev	8.651



B1L103S, U12-ch56, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch56, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

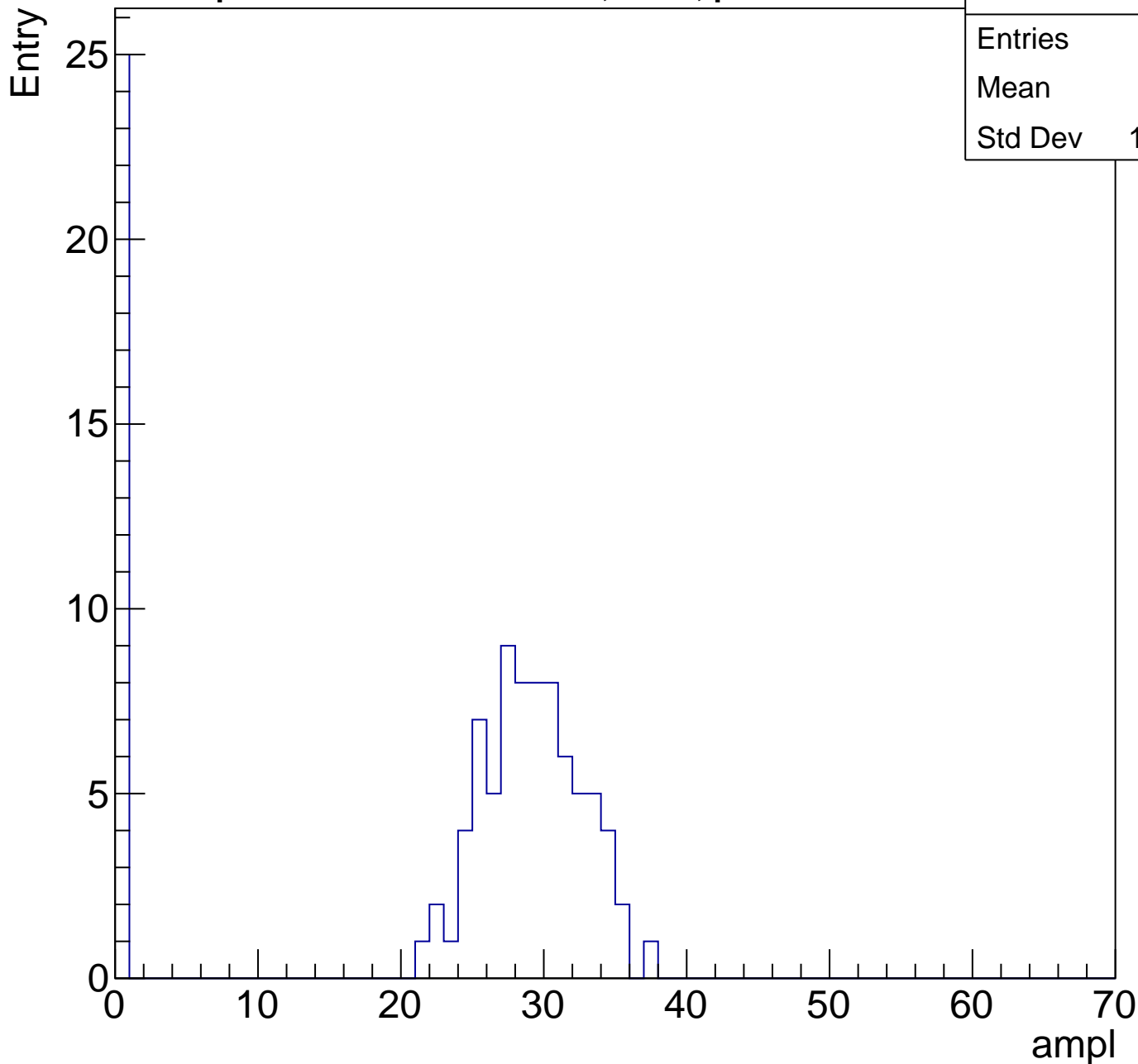
ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U12-ch57, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	101
Mean	21.6
Std Dev	12.74

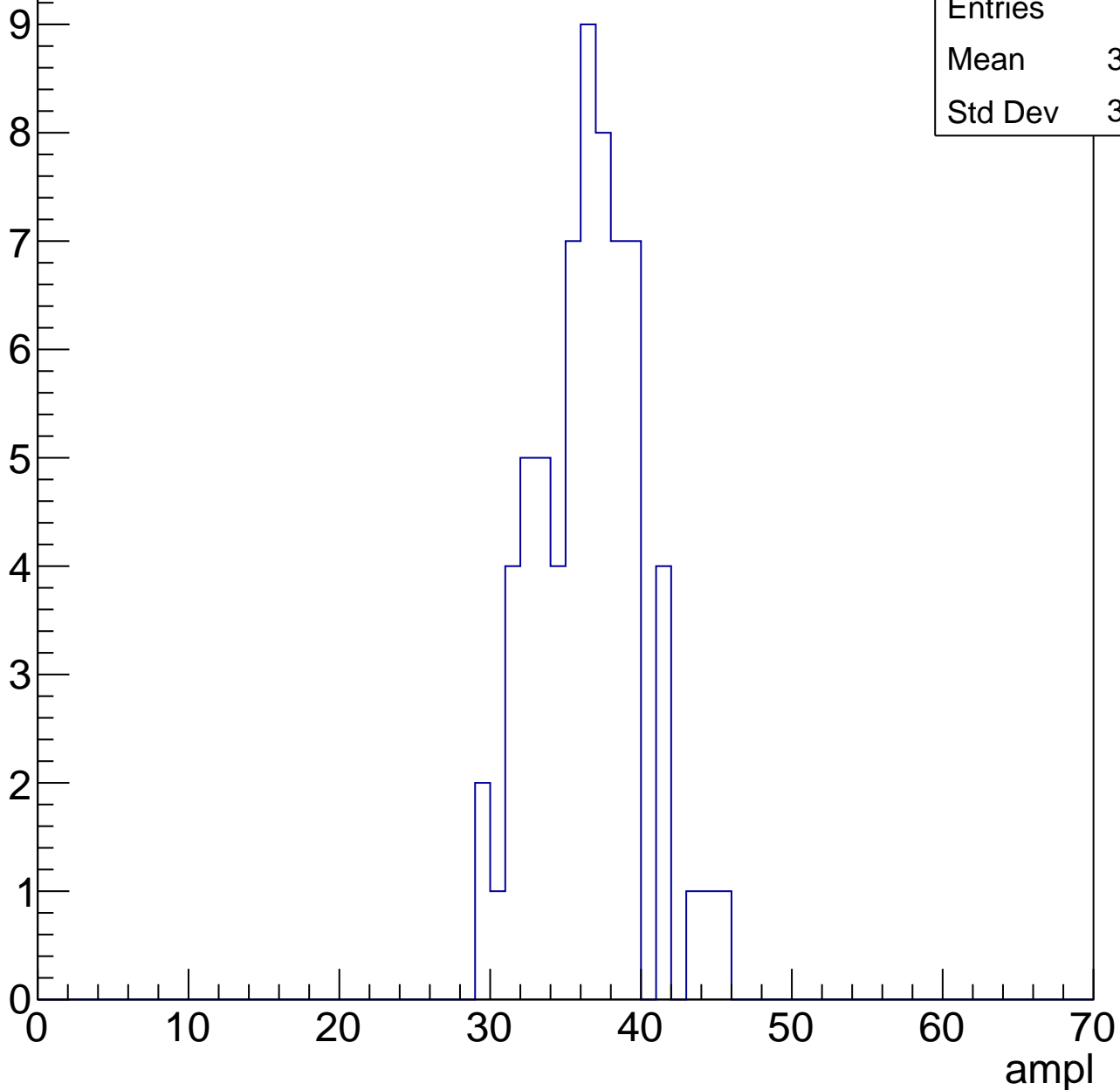


B1L103S, U12-ch57, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	35.95
Std Dev	3.426



B1L103S, U12-ch57, adc2

calib_packv5_041523_1651.root, FC#0, port C2

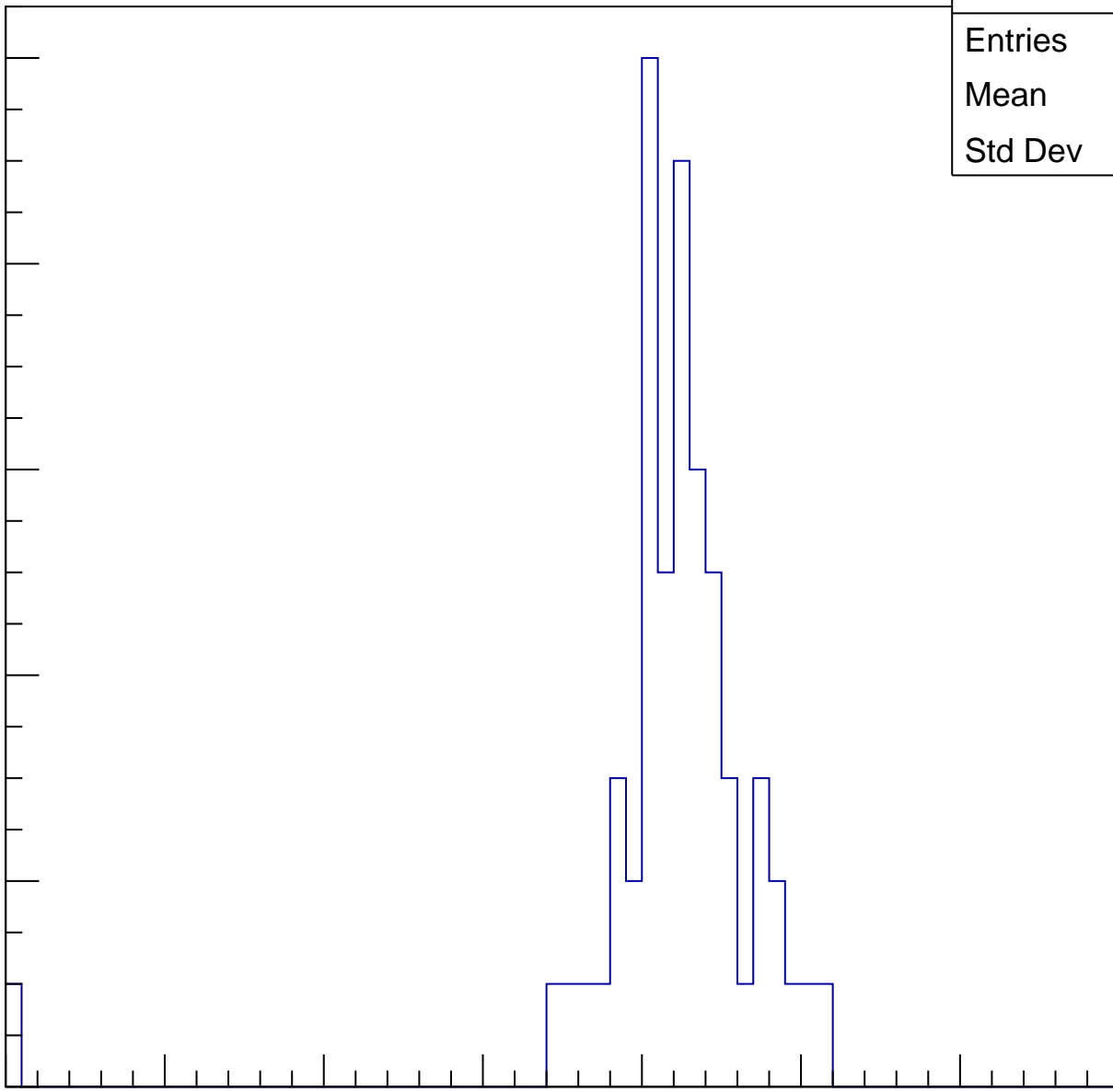
Entries	57
Mean	41.46
Std Dev	6.546

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

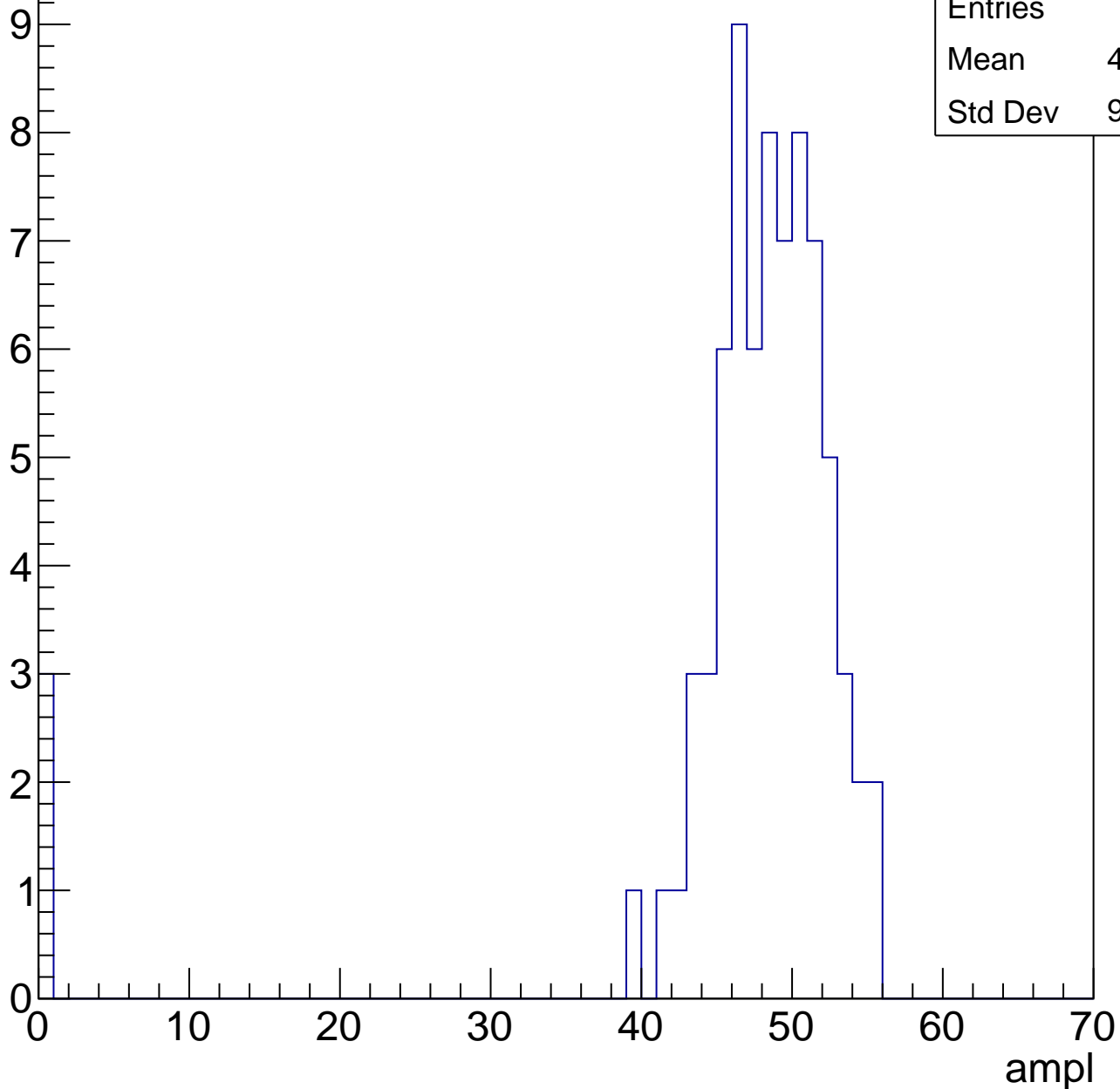
ampl



B1L103S, U12-ch57, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

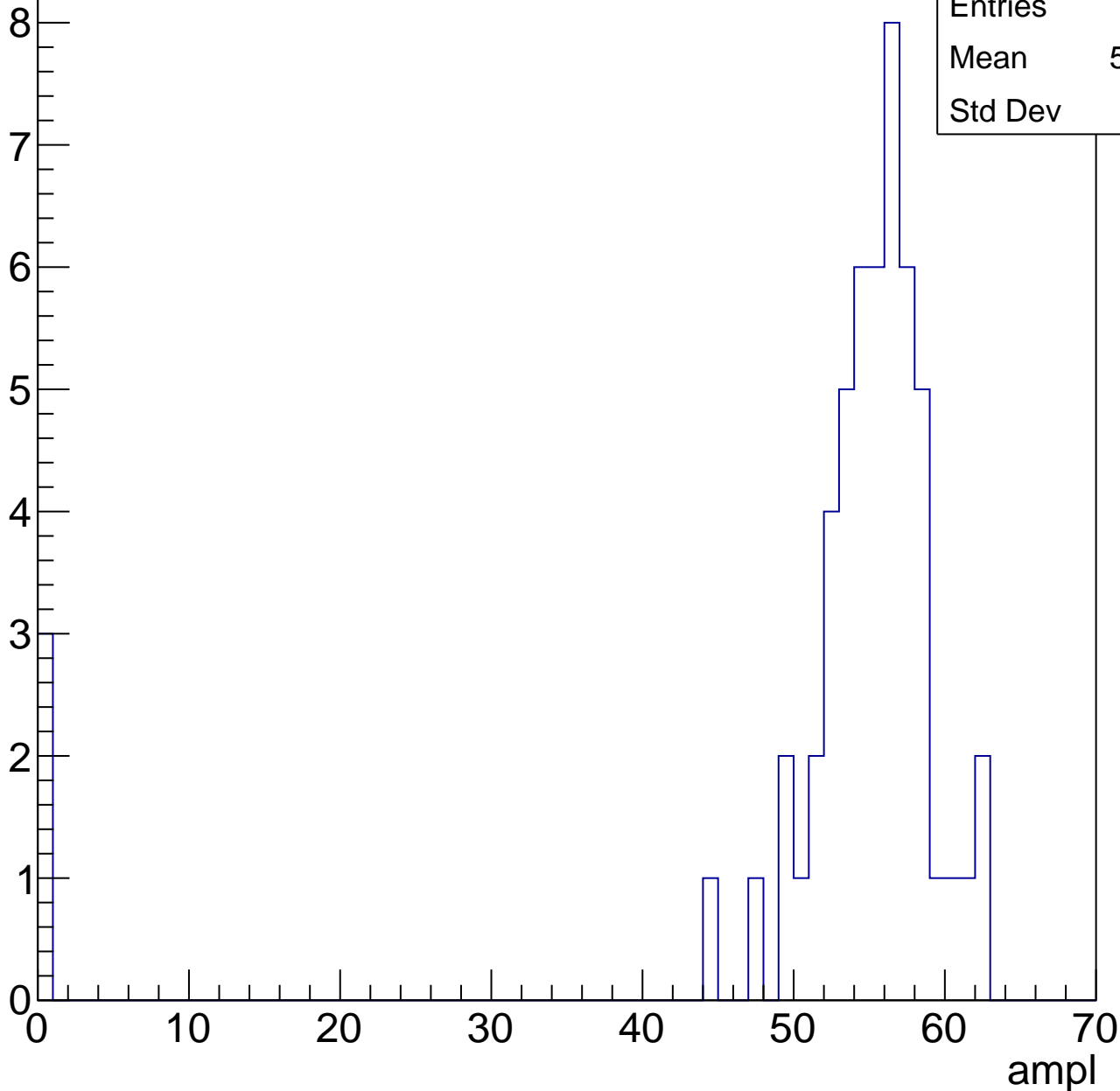


B1L103S, U12-ch57, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

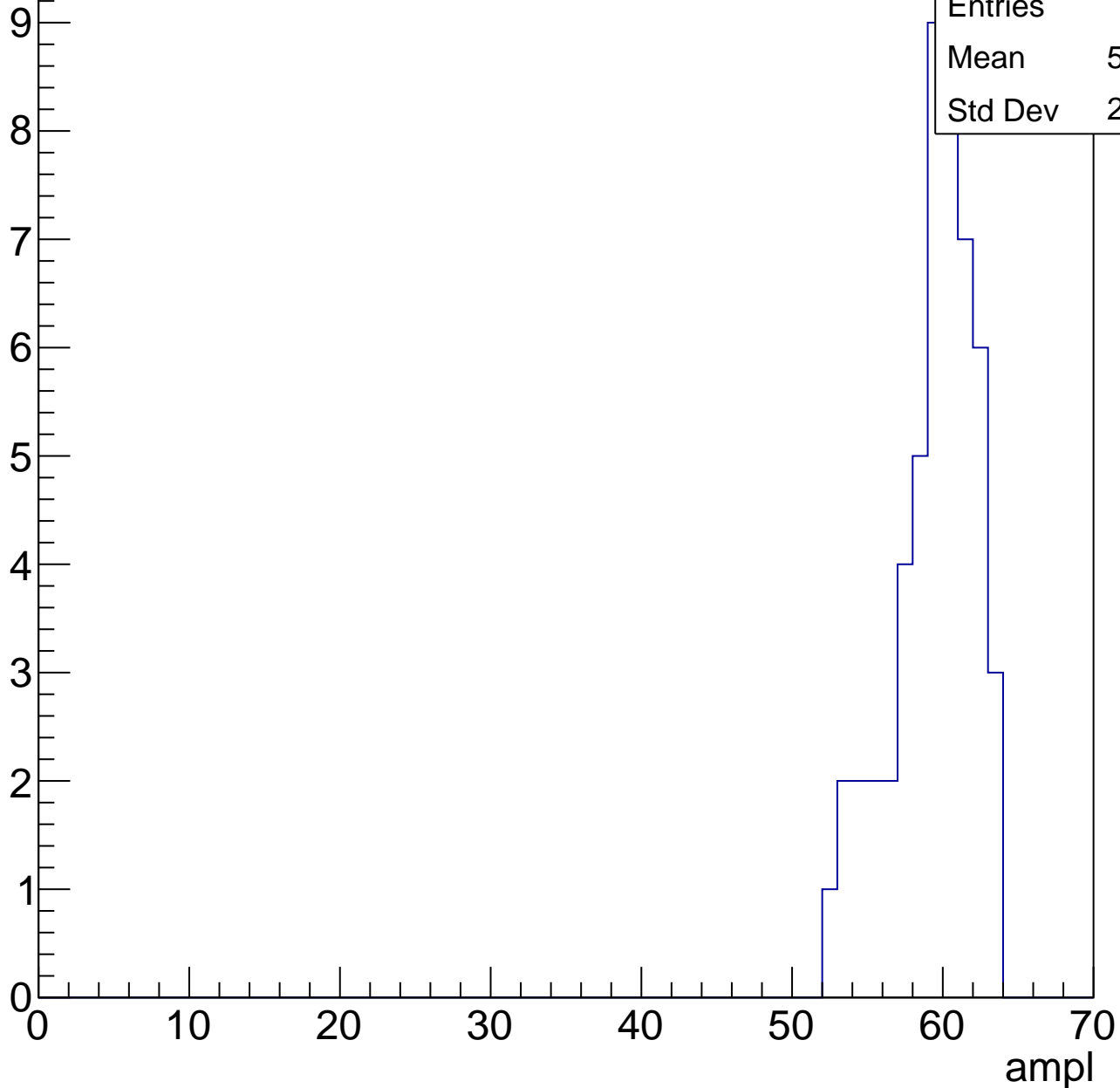
Entries	55
Mean	51.85
Std Dev	12.9



B1L103S, U12-ch57, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



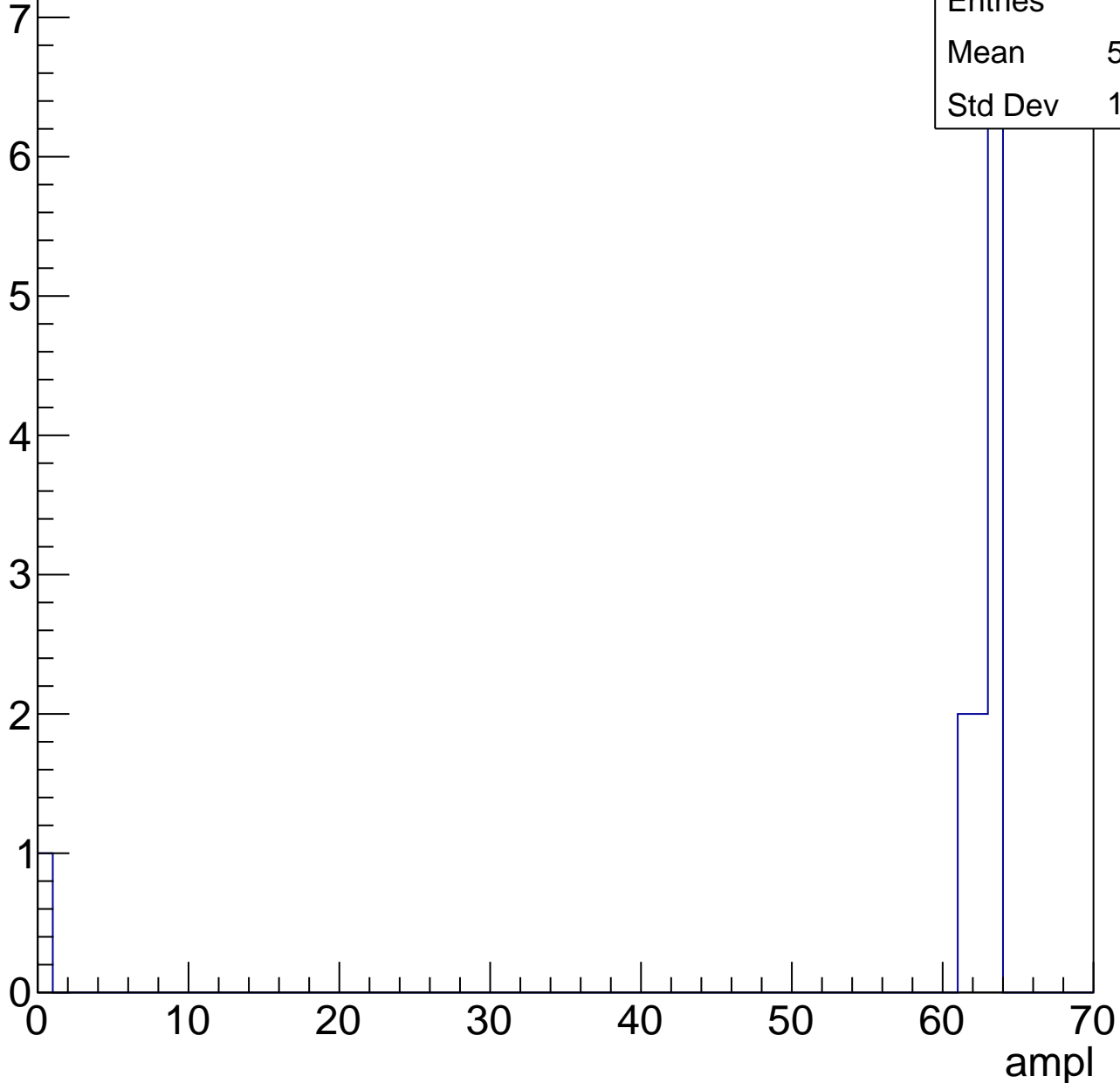
Entries	52
Mean	58.94
Std Dev	2.706

B1L103S, U12-ch57, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	12
Mean	57.25
Std Dev	17.28



B1L103S, U12-ch57, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch58, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	96
Mean	25.01
Std Dev	10.48

Entry

12

10

8

6

4

2

0

0

10

20

30

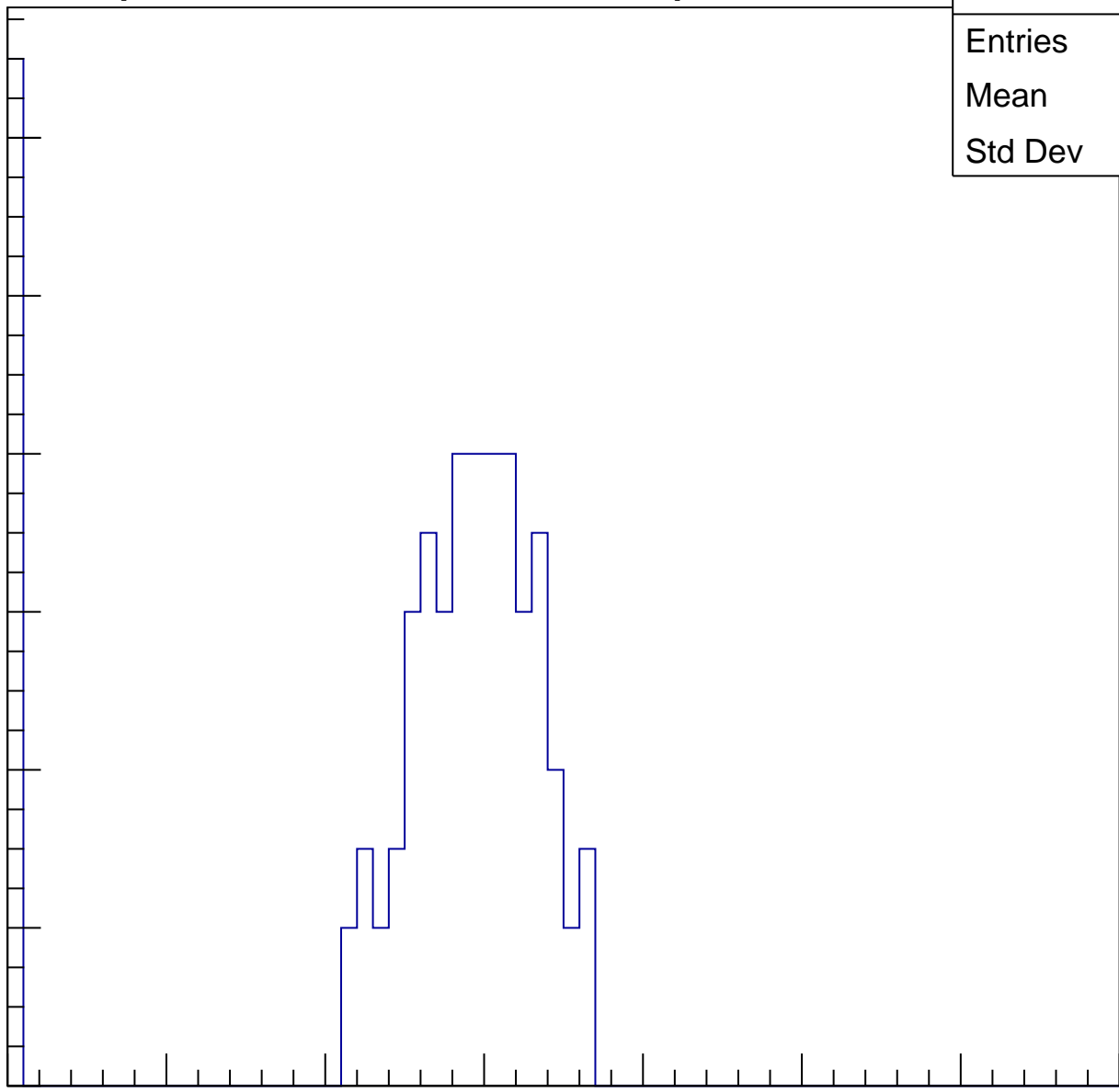
40

50

60

70

ampl

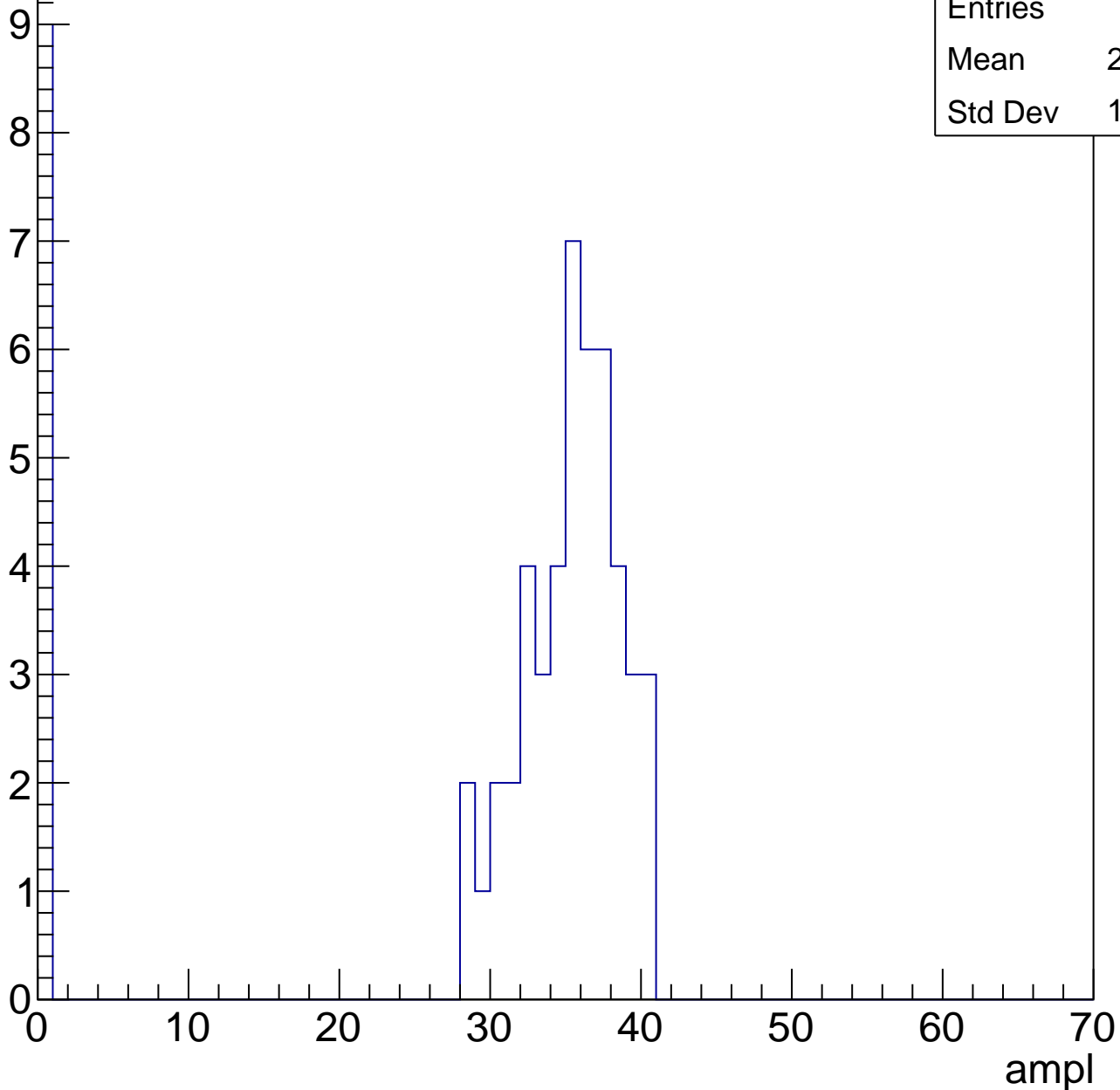


B1L103S, U12-ch58, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	56
Mean	29.32
Std Dev	13.14



B1L103S, U12-ch58, adc2

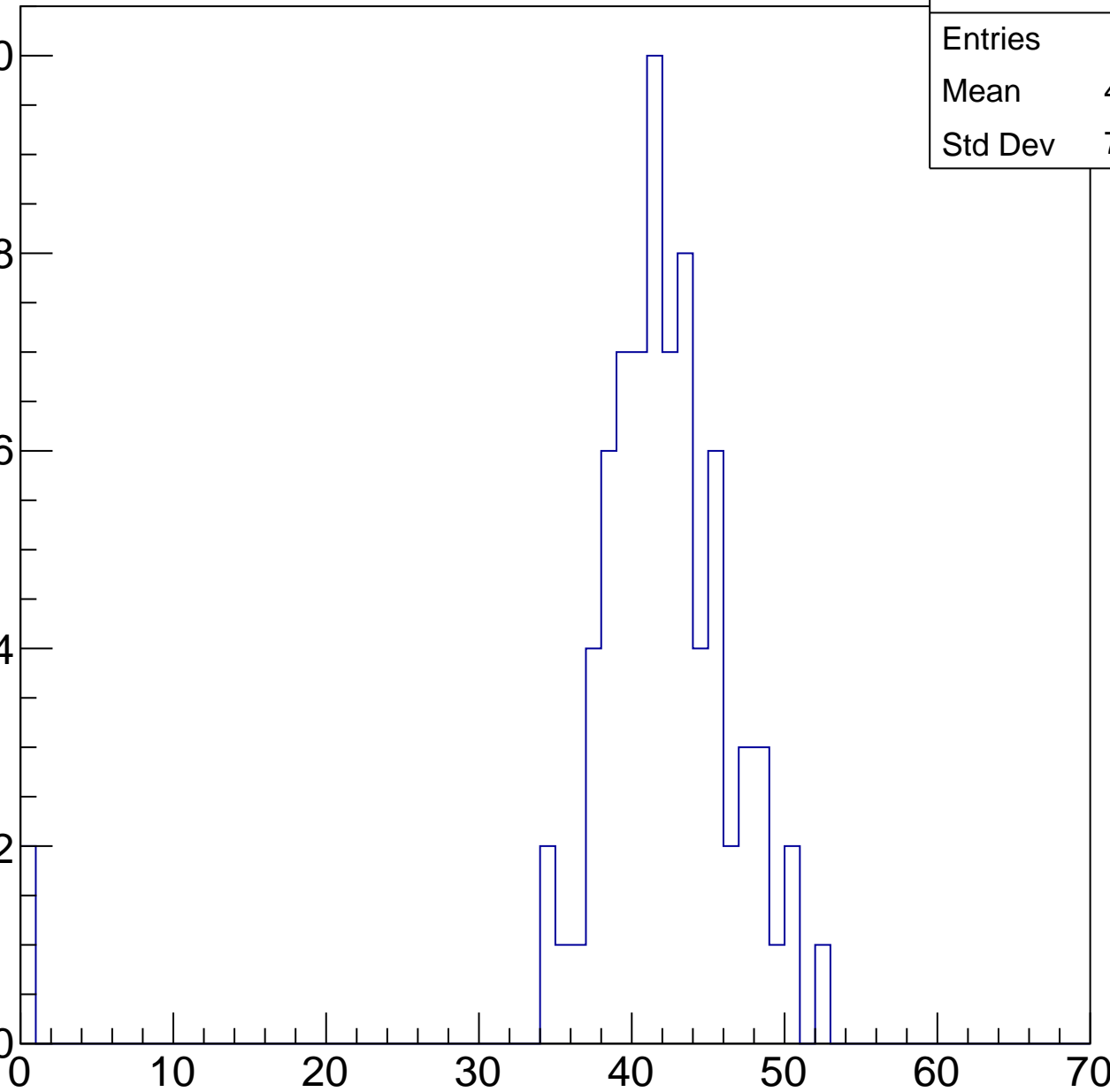
calib_packv5_041523_1651.root, FC#0, port C2

Entries	77
Mean	40.78
Std Dev	7.639

Entry

10
8
6
4
2
0

ampl

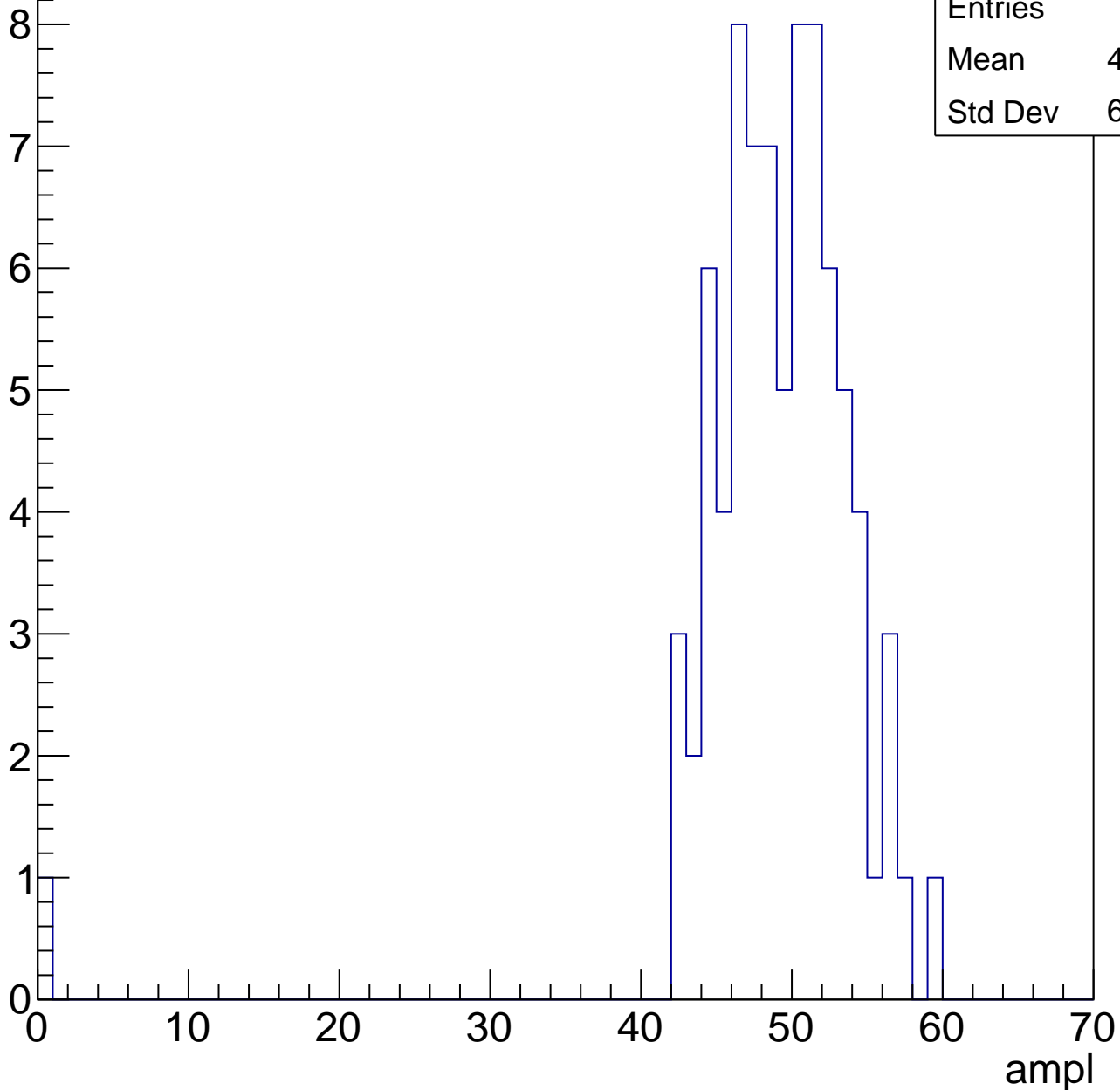


B1L103S, U12-ch58, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	80
Mean	48.42
Std Dev	6.648

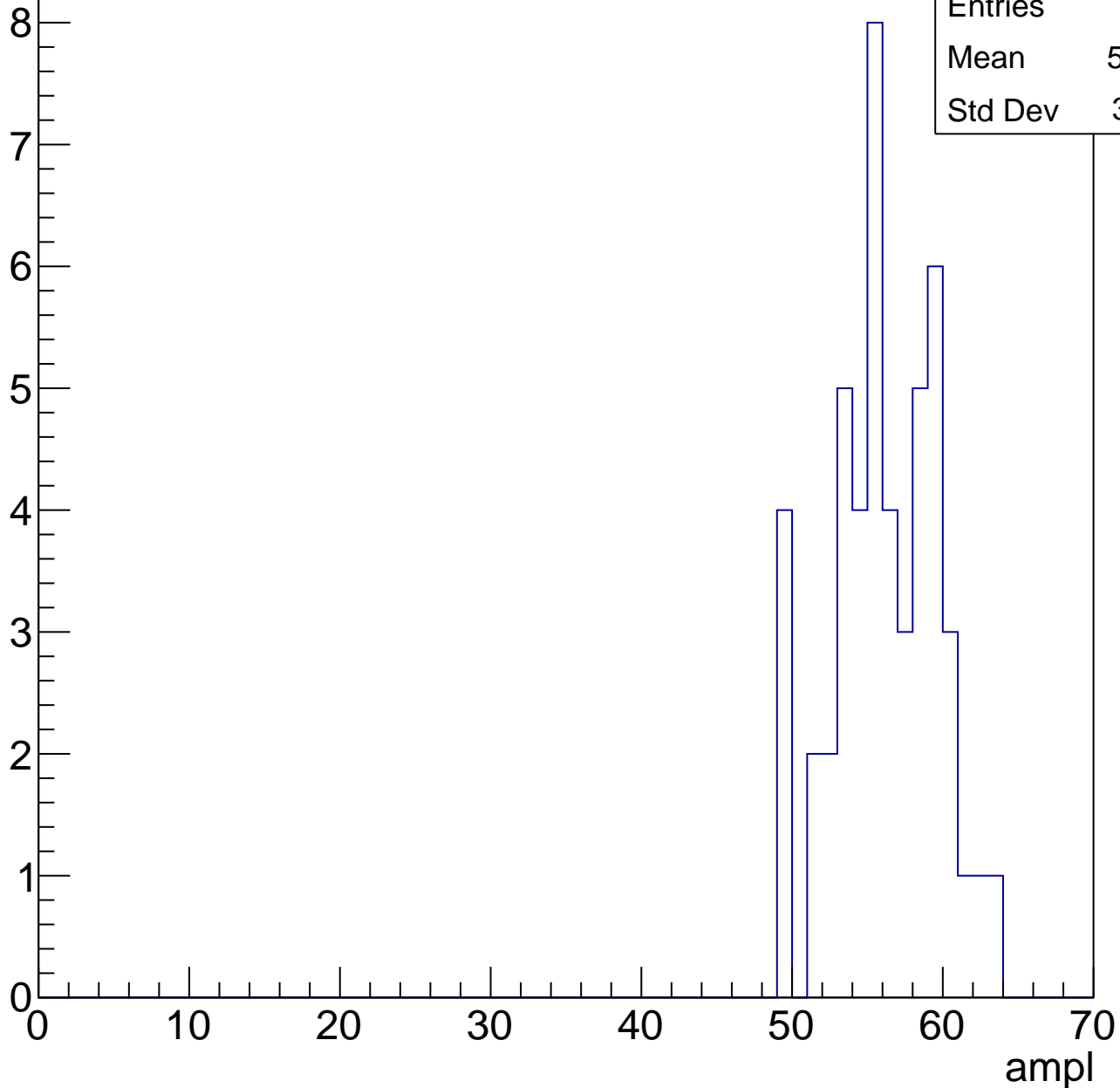


B1L103S, U12-ch58, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

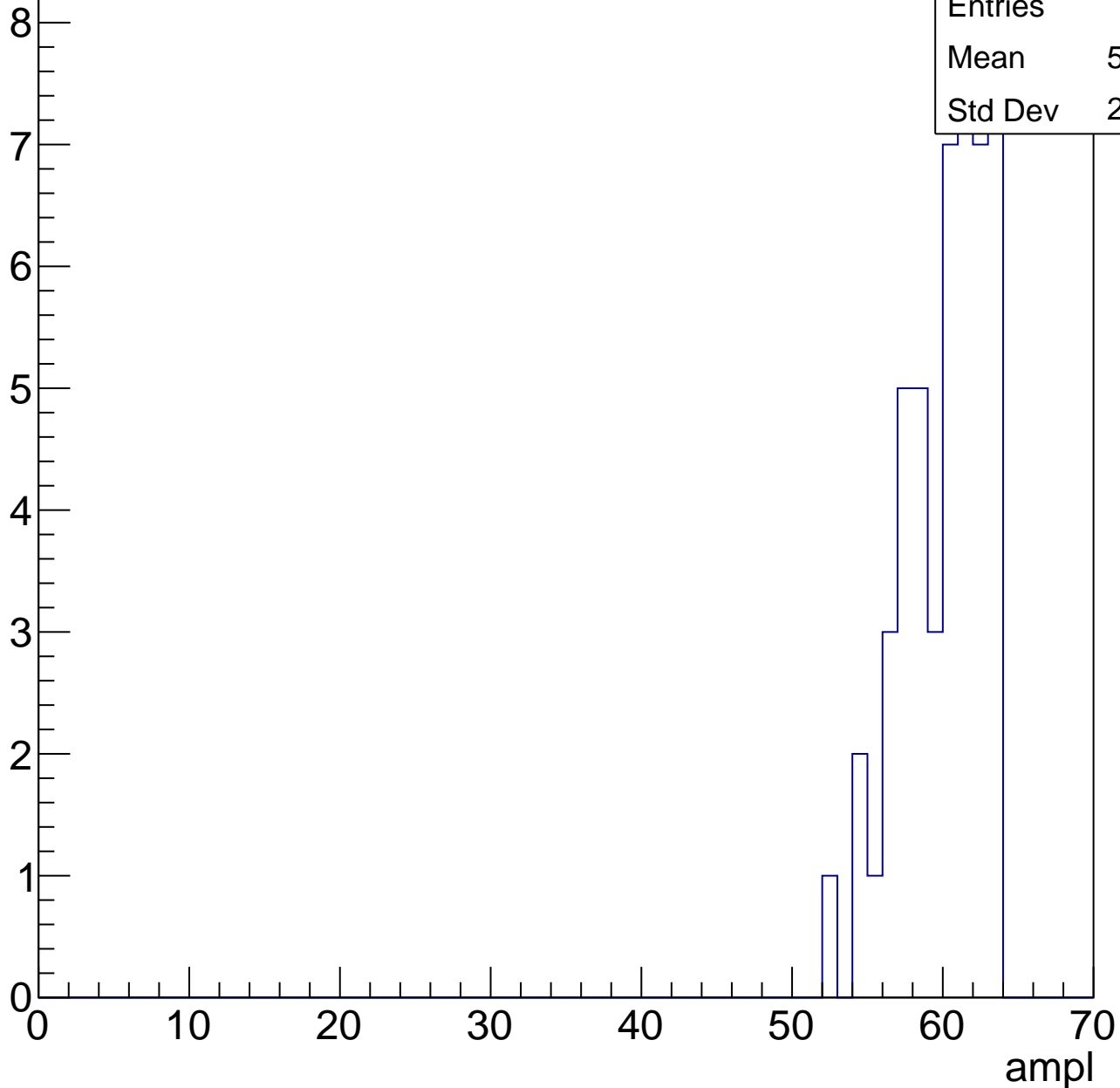
Entries	49
Mean	55.67
Std Dev	3.431



B1L103S, U12-ch58, adc5

calib_packv5_041523_1651.root, FC#0, port C2

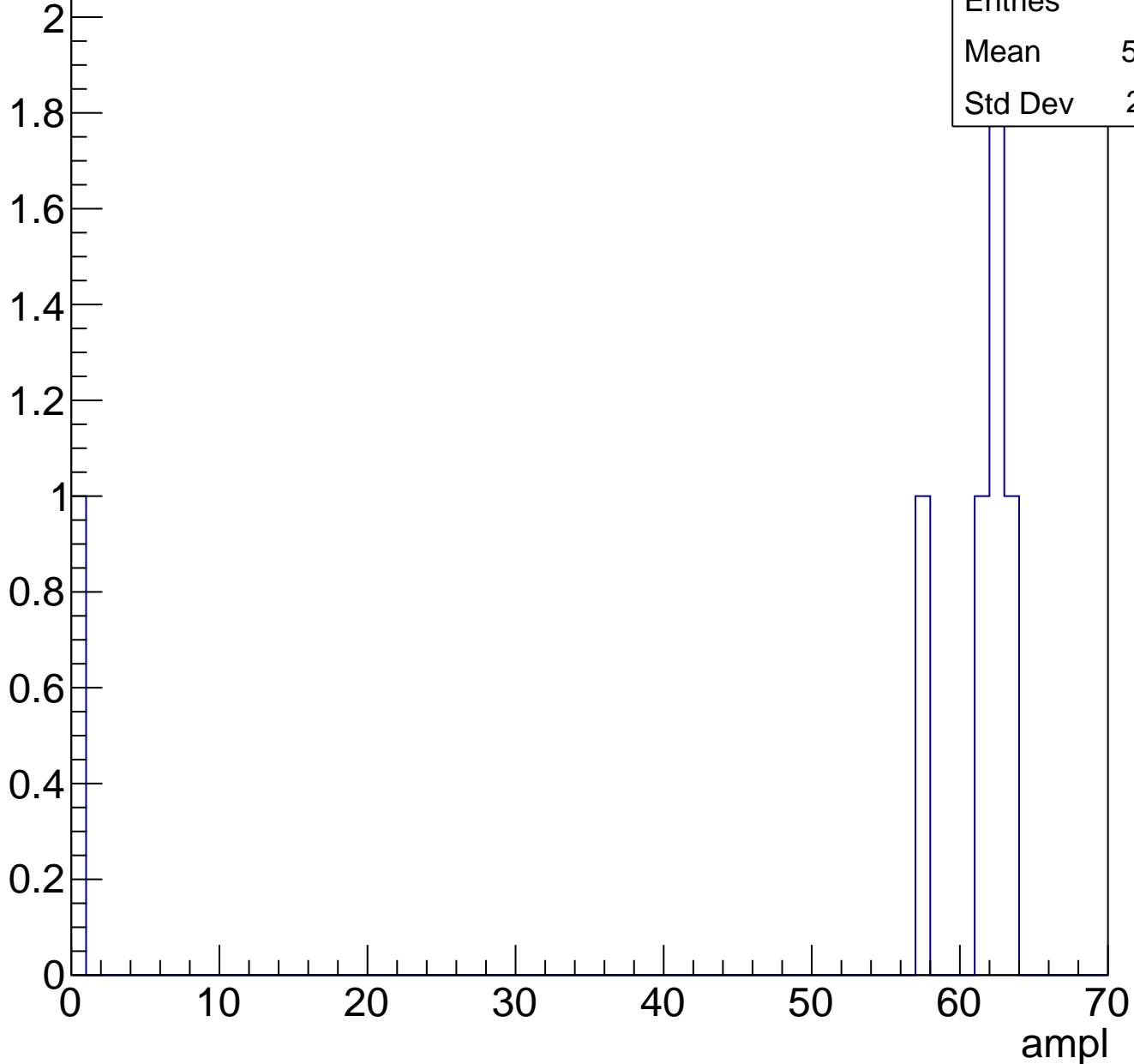
Entry



B1L103S, U12-ch58, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch58, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

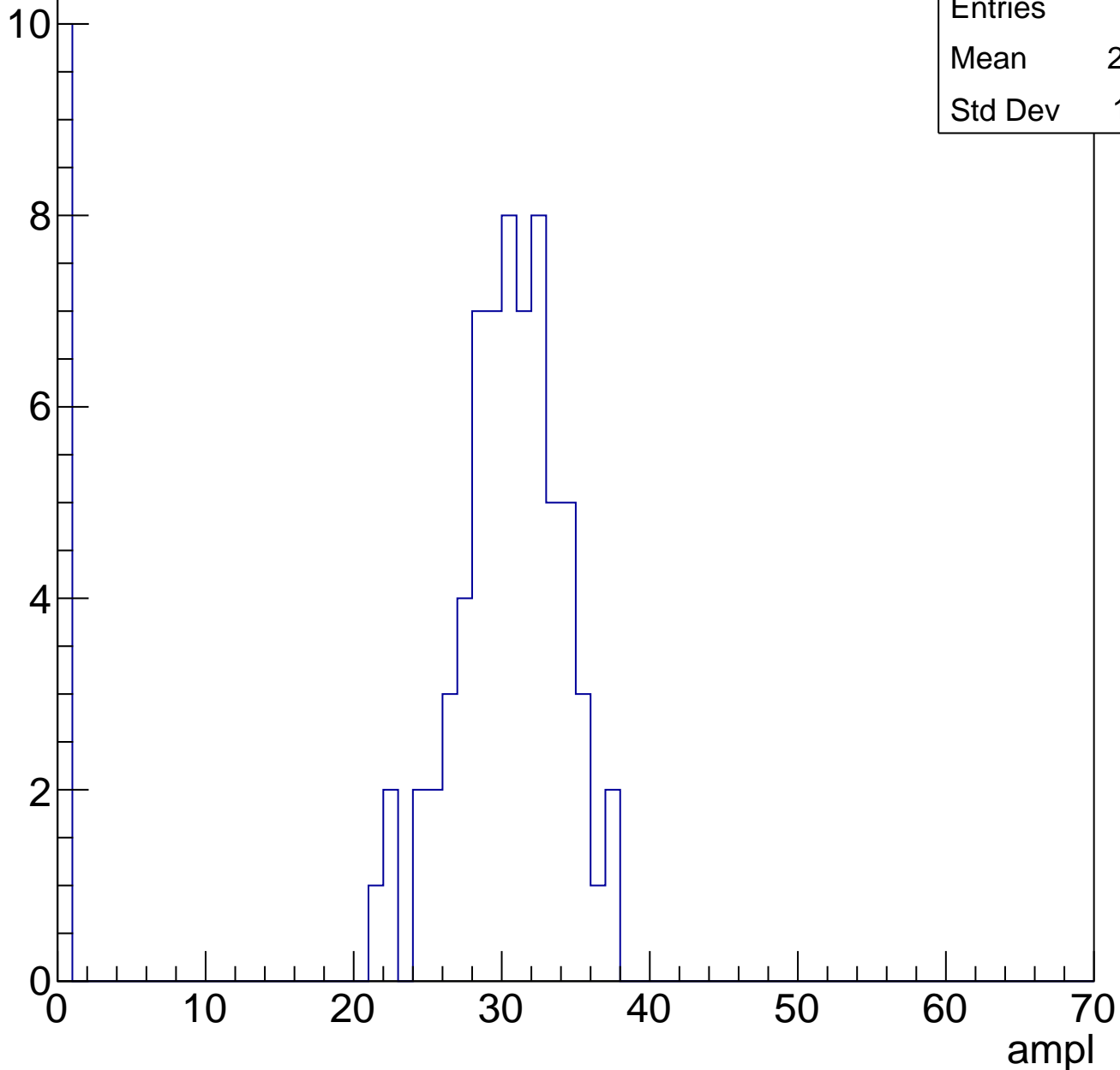
Entries	19
Mean	0
Std Dev	0

B1L103S, U12-ch59, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	77
Mean	26.12
Std Dev	10.61

Entry

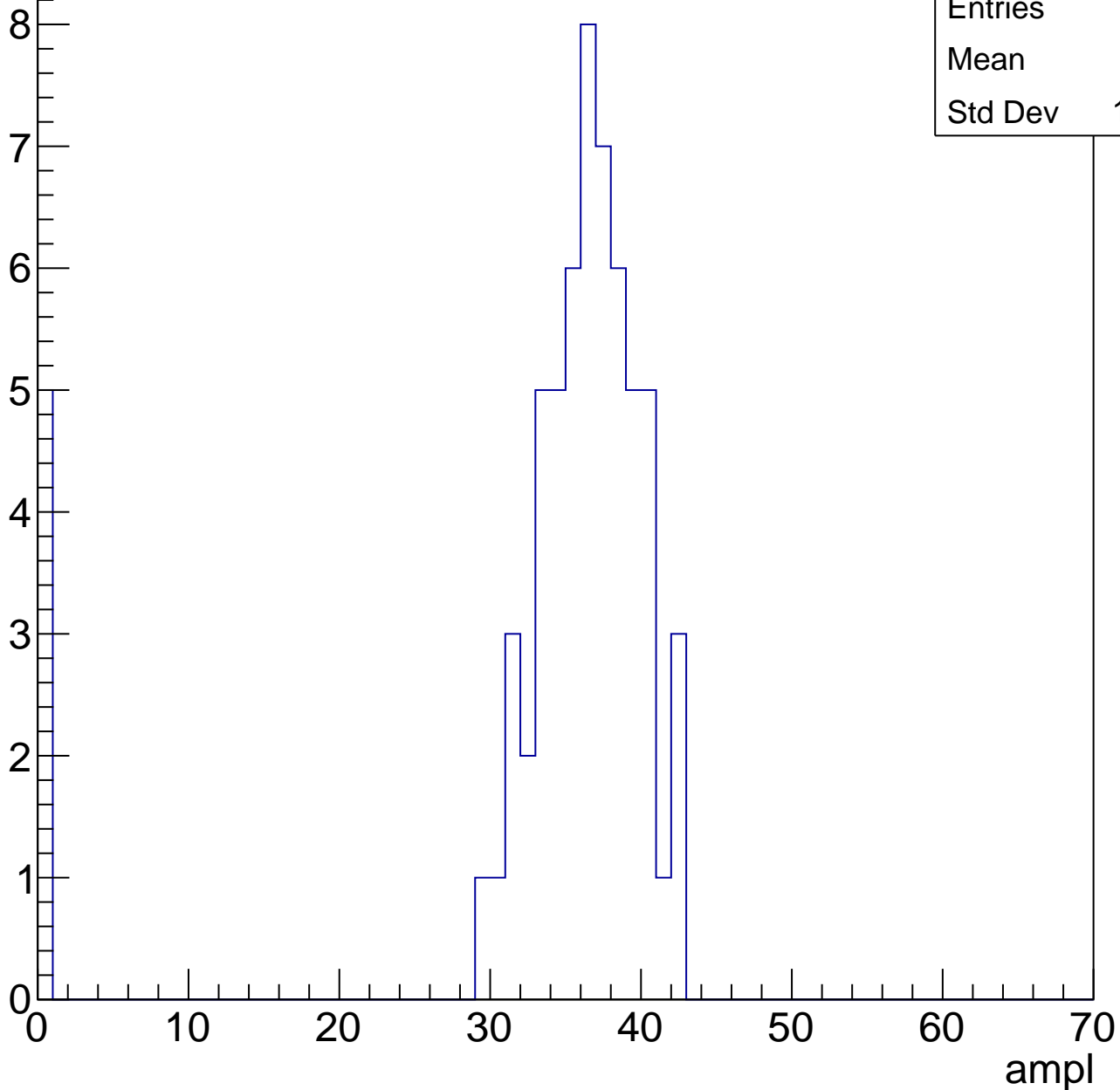


B1L103S, U12-ch59, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	63
Mean	33.3
Std Dev	10.21

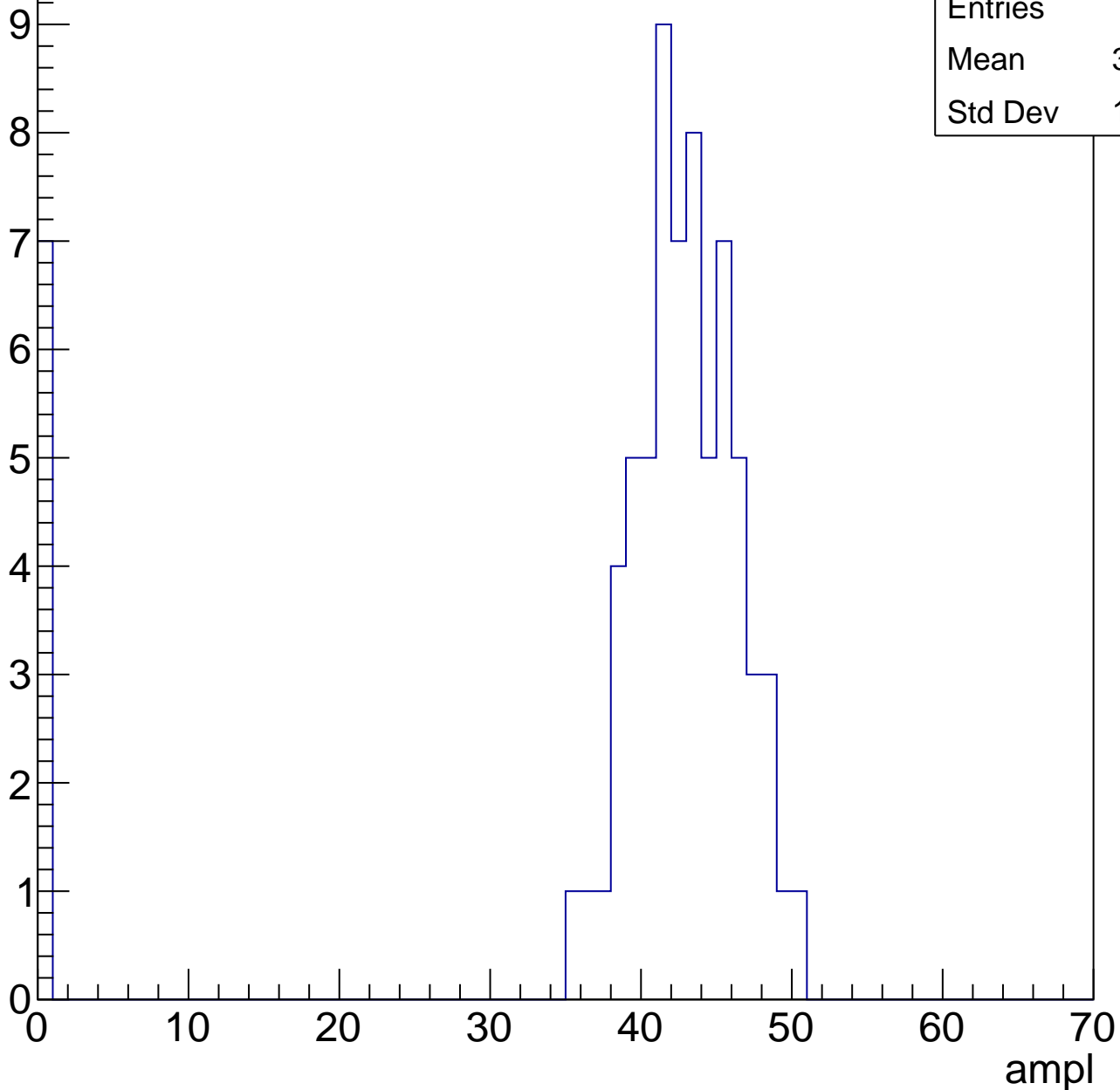


B1L103S, U12-ch59, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	73
Mean	38.51
Std Dev	12.91

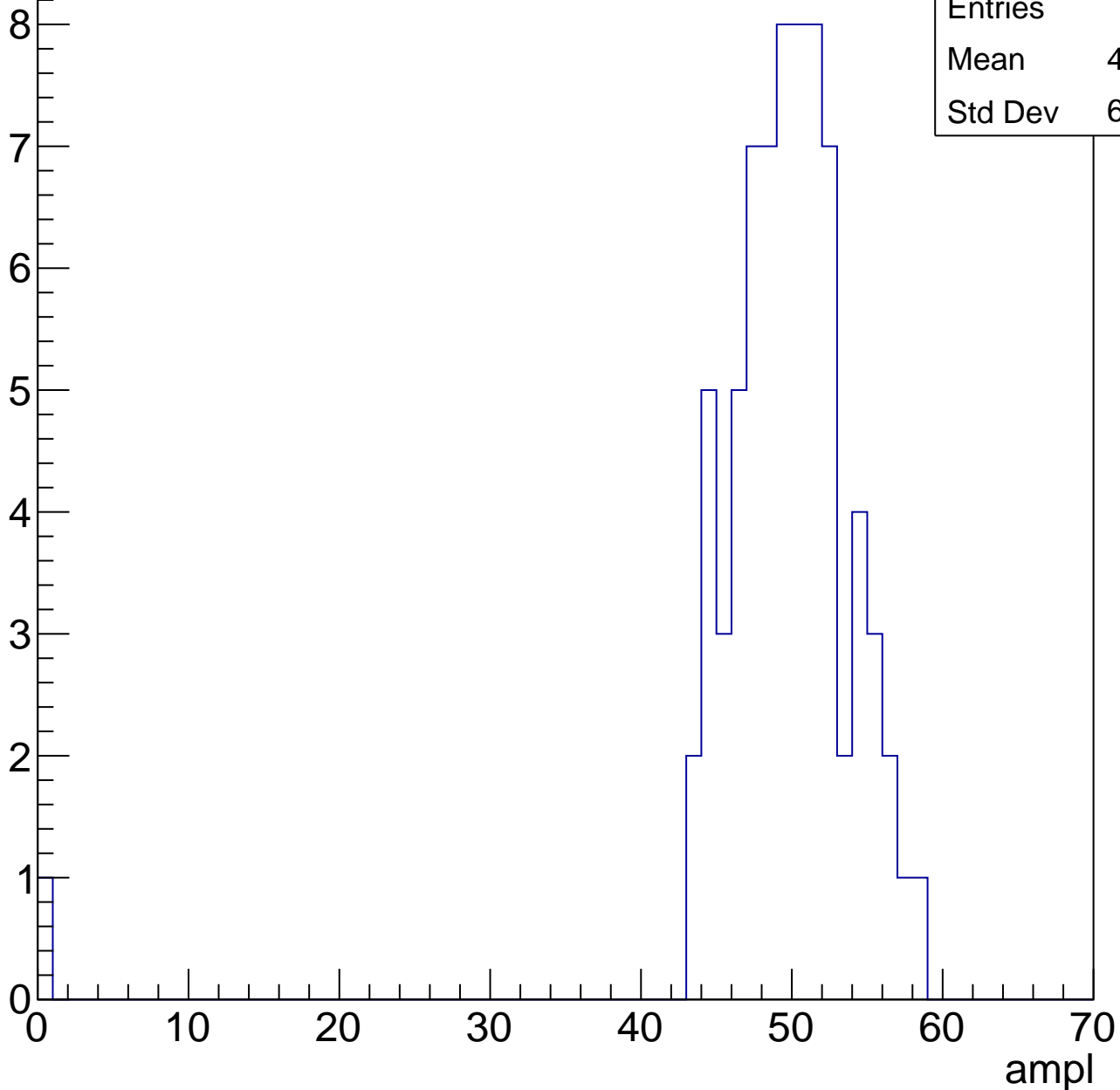


B1L103S, U12-ch59, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

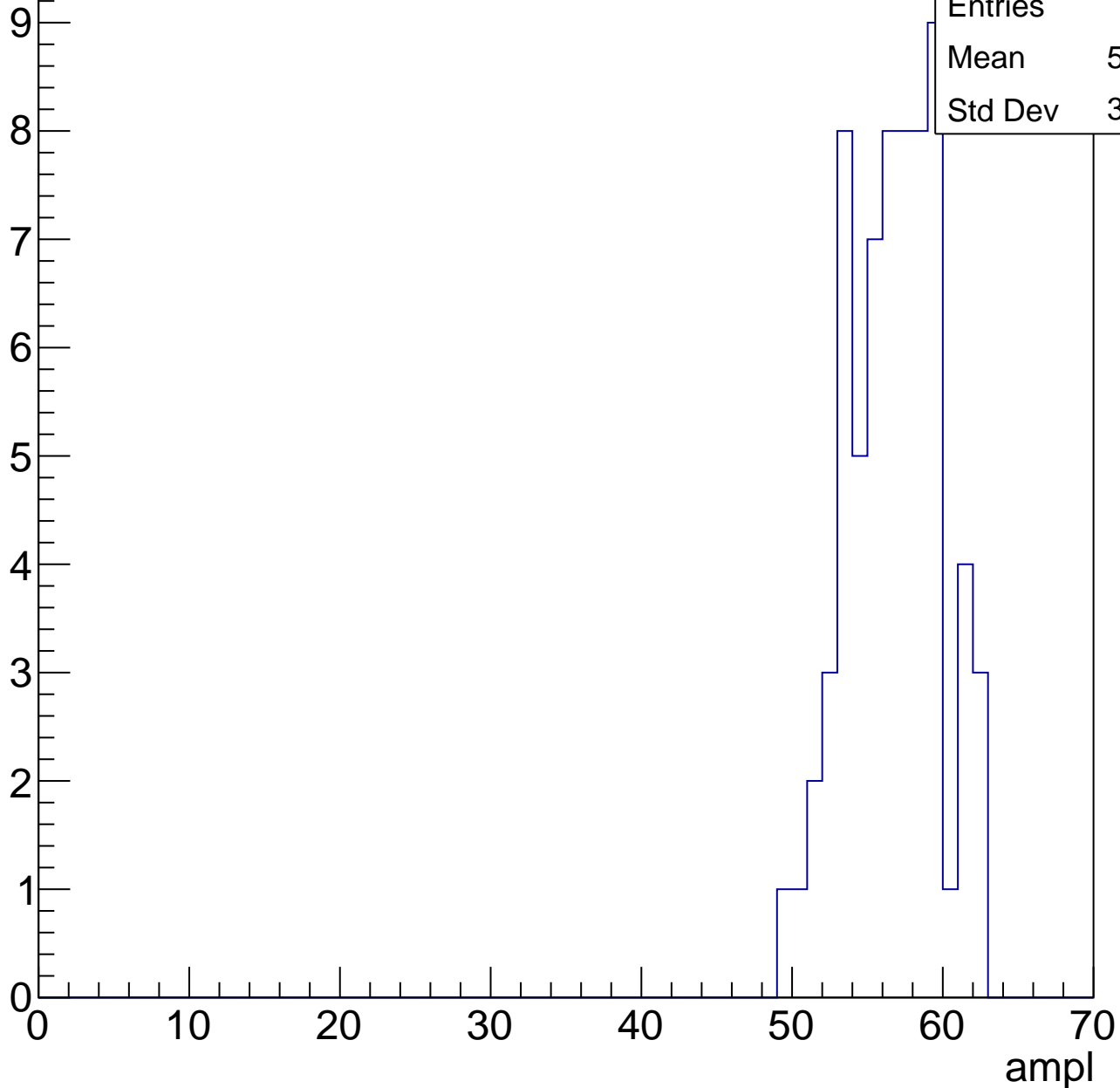
Entries	74
Mean	48.84
Std Dev	6.688



B1L103S, U12-ch59, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

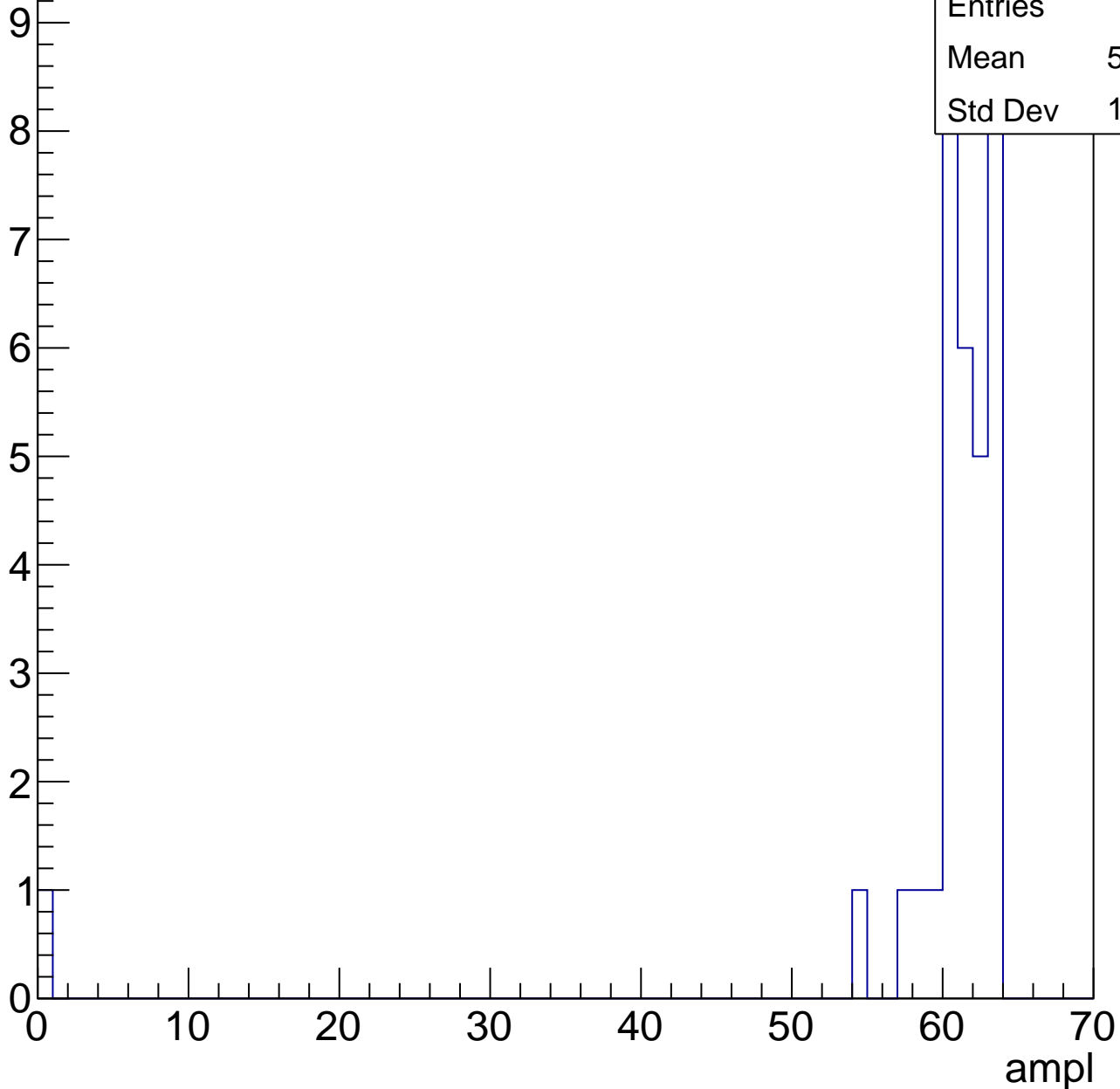


B1L103S, U12-ch59, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

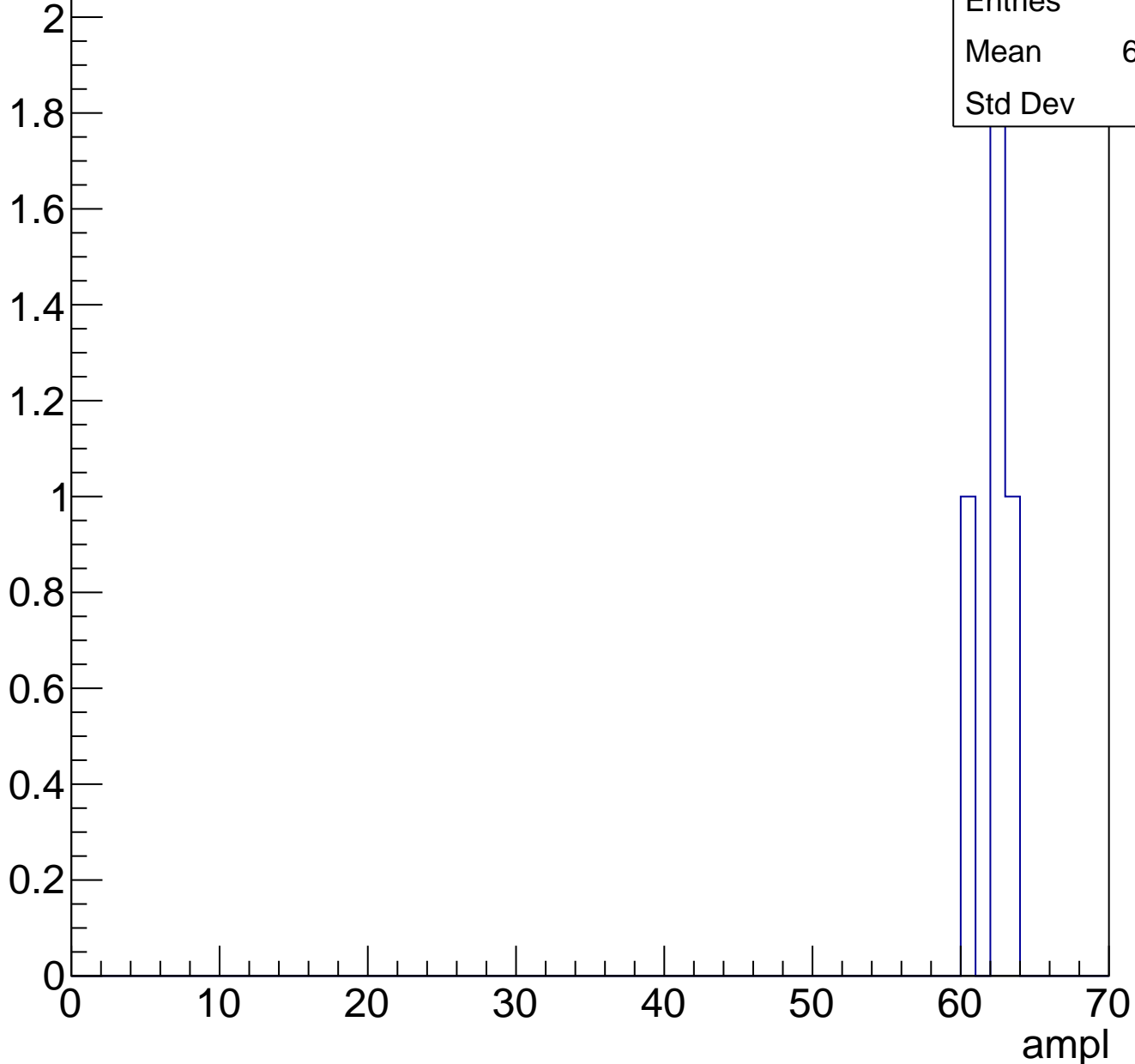
Entries	33
Mean	59.12
Std Dev	10.63



B1L103S, U12-ch59, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch59, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

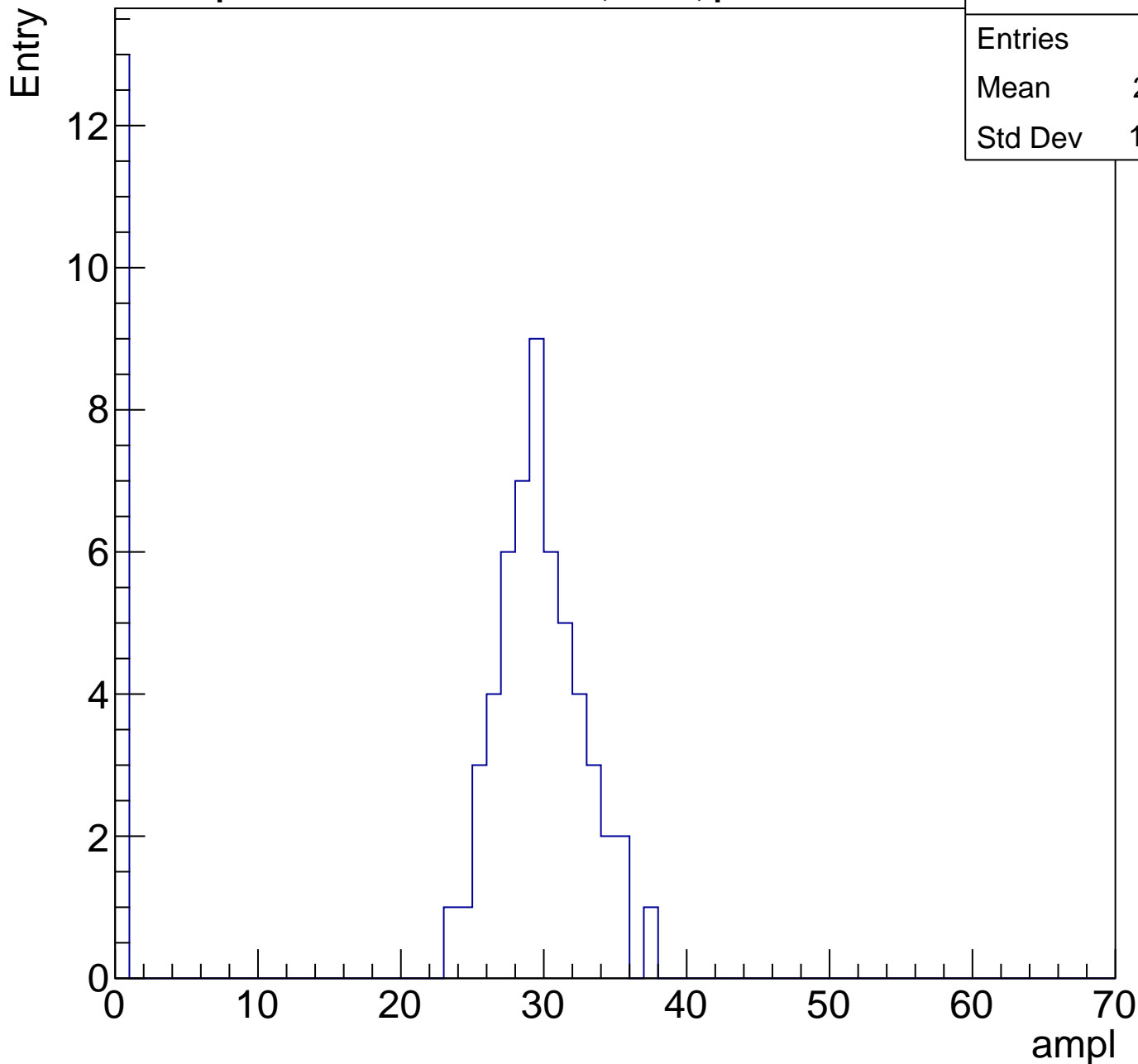
ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U12-ch60, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	67
Mean	23.61
Std Dev	11.88

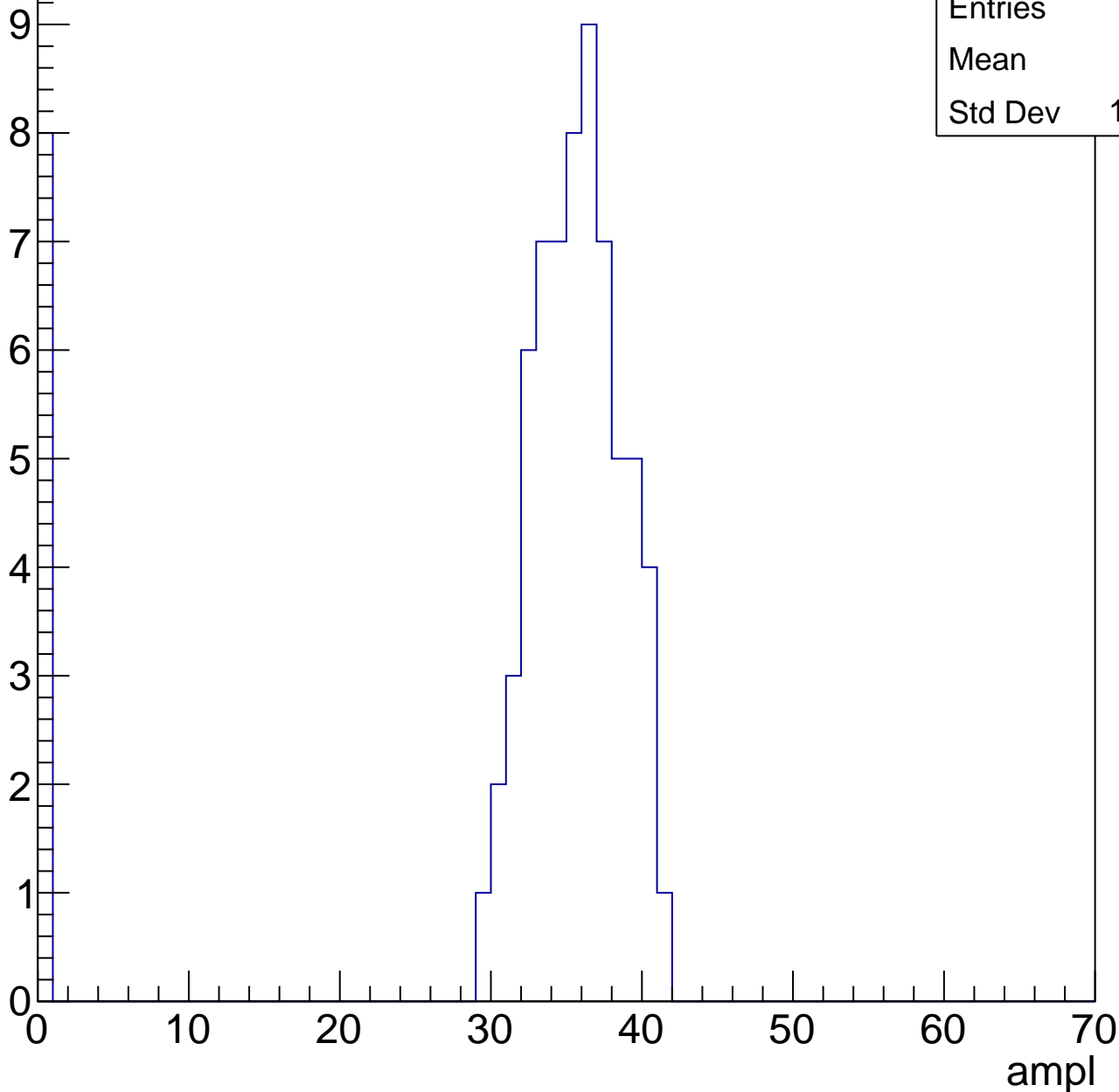


B1L103S, U12-ch60, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	73
Mean	31.4
Std Dev	11.33

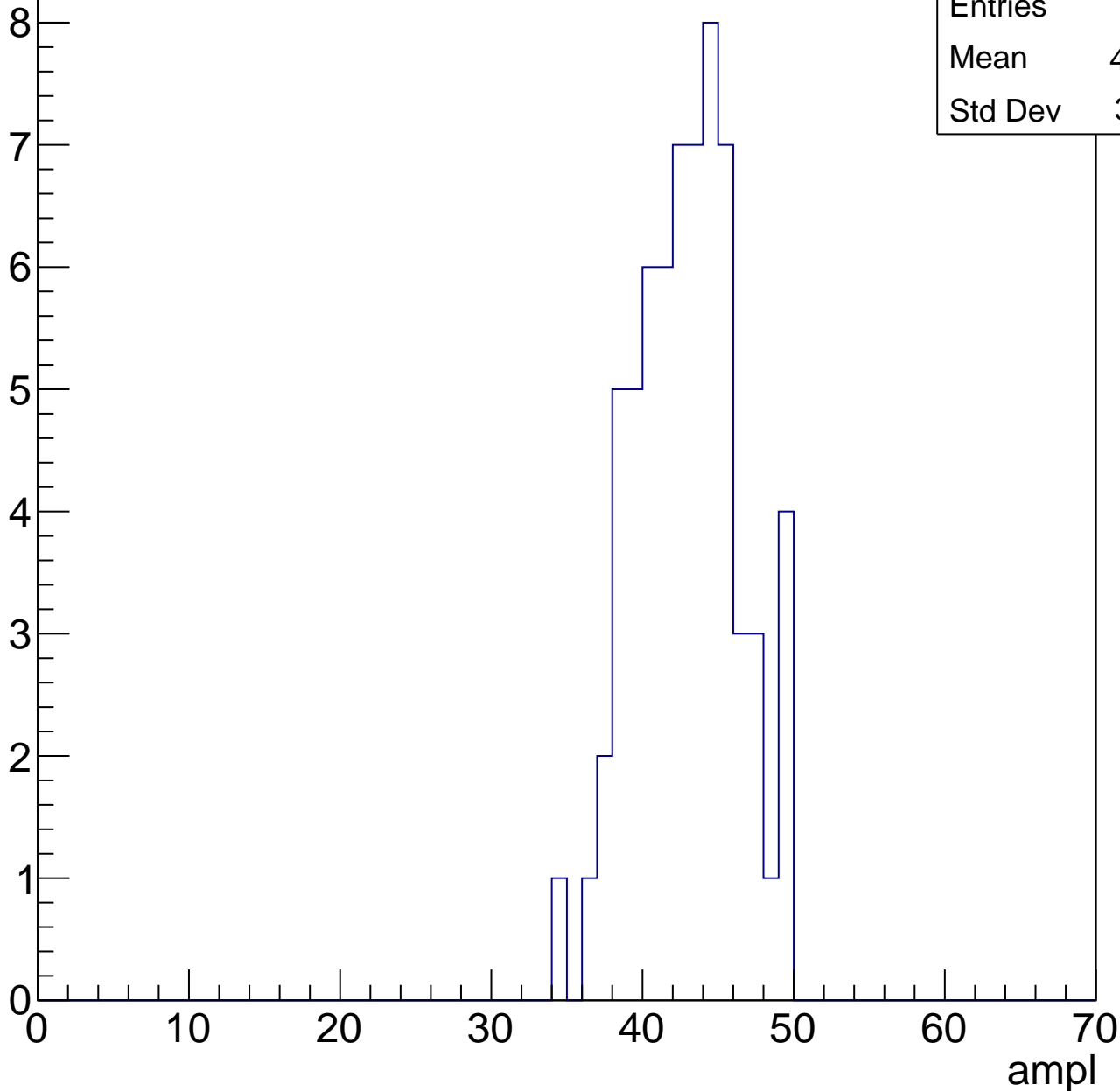


B1L103S, U12-ch60, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	42.42
Std Dev	3.371

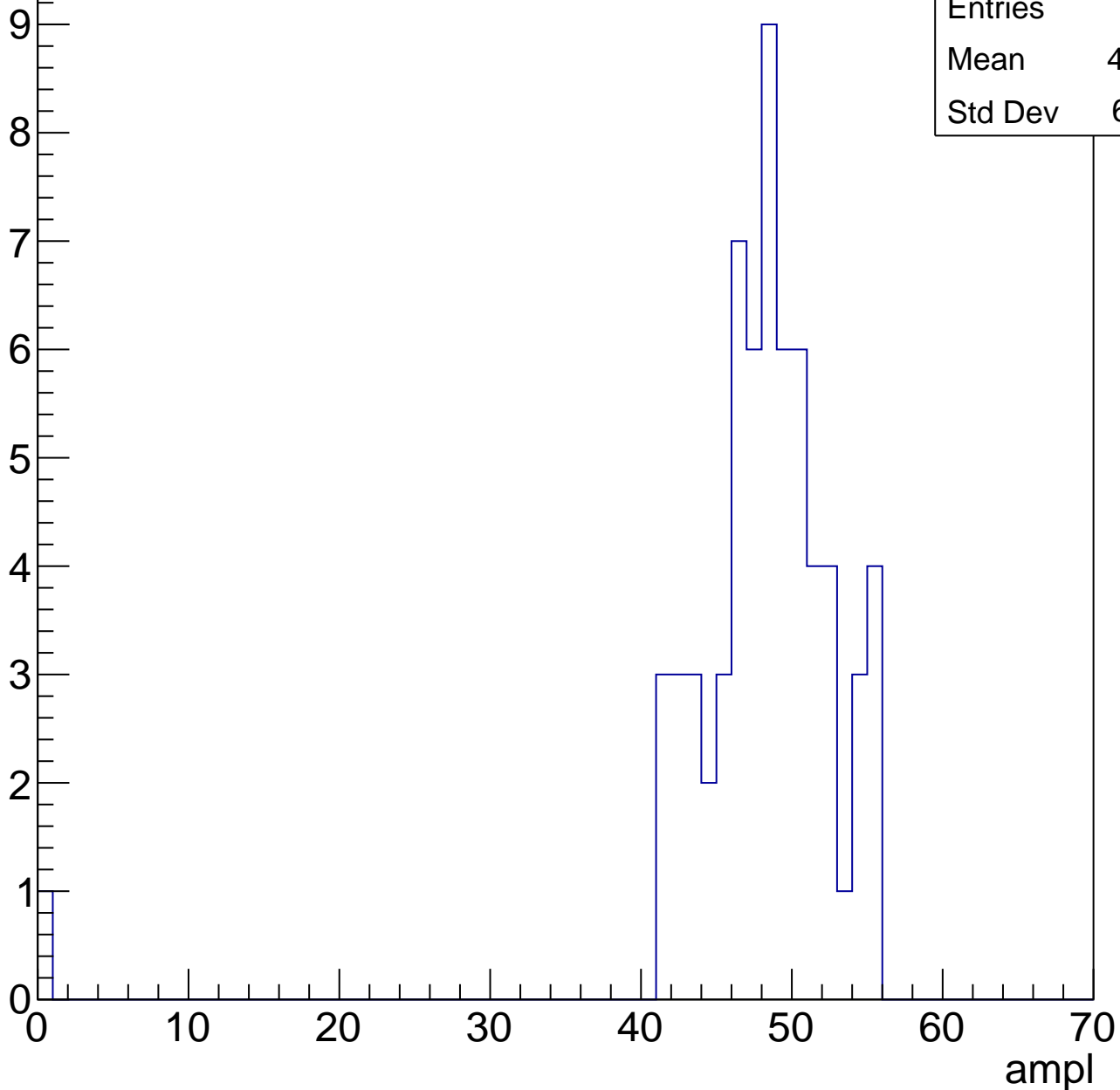


B1L103S, U12-ch60, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	47.35
Std Dev	6.971

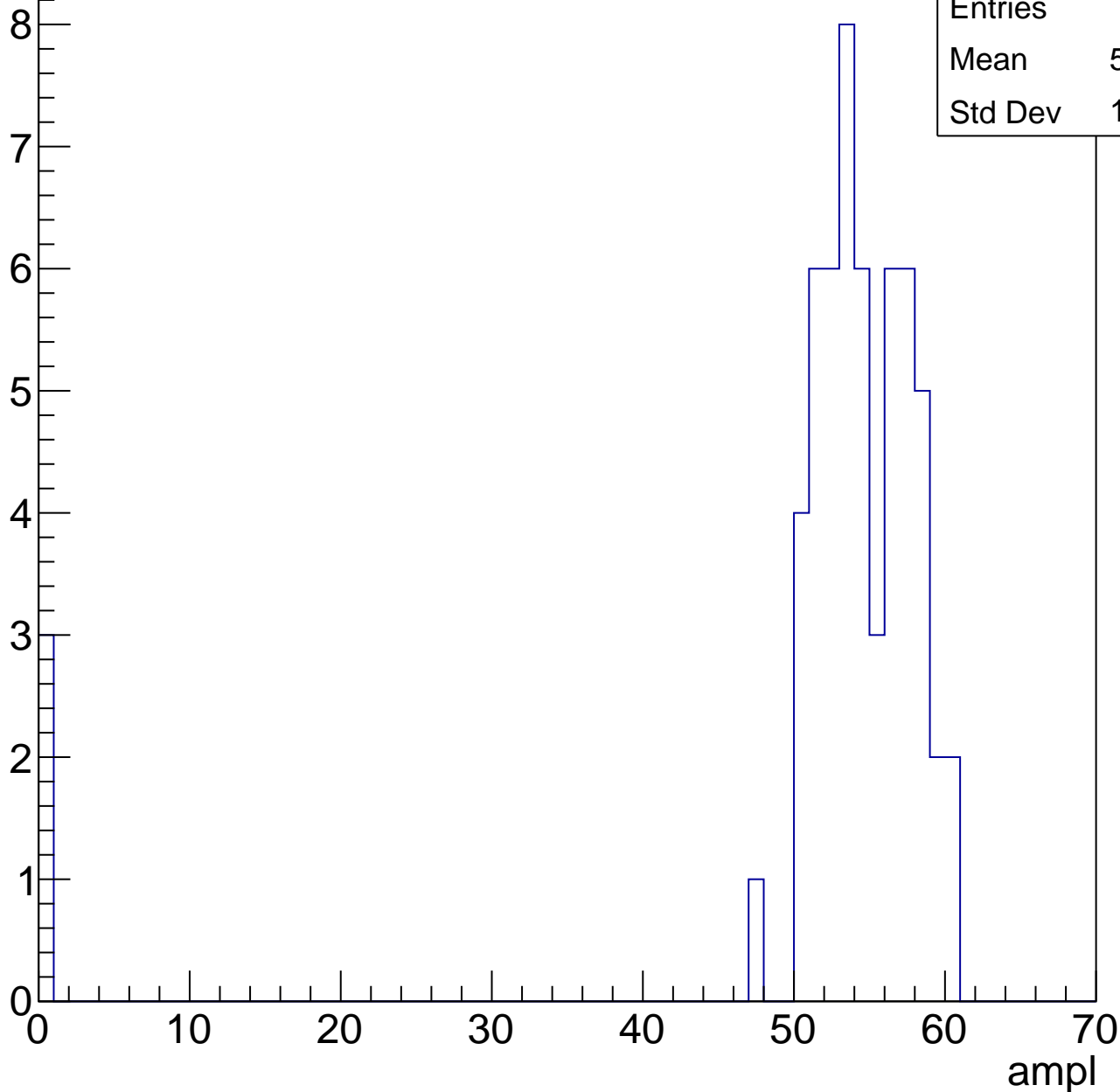


B1L103S, U12-ch60, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

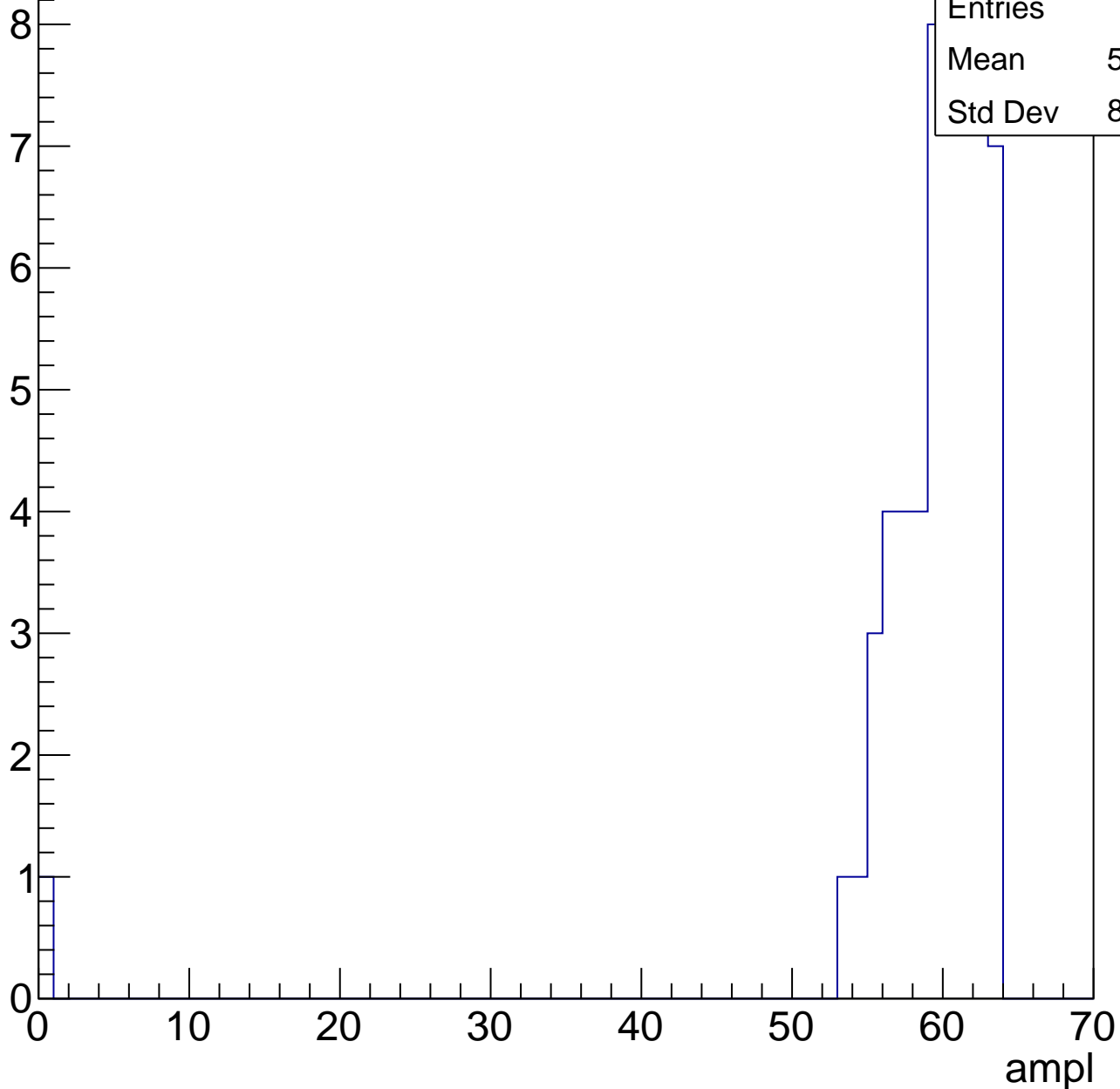
Entries	58
Mean	51.45
Std Dev	12.35



B1L103S, U12-ch60, adc5

calib_packv5_041523_1651.root, FC#0, port C2

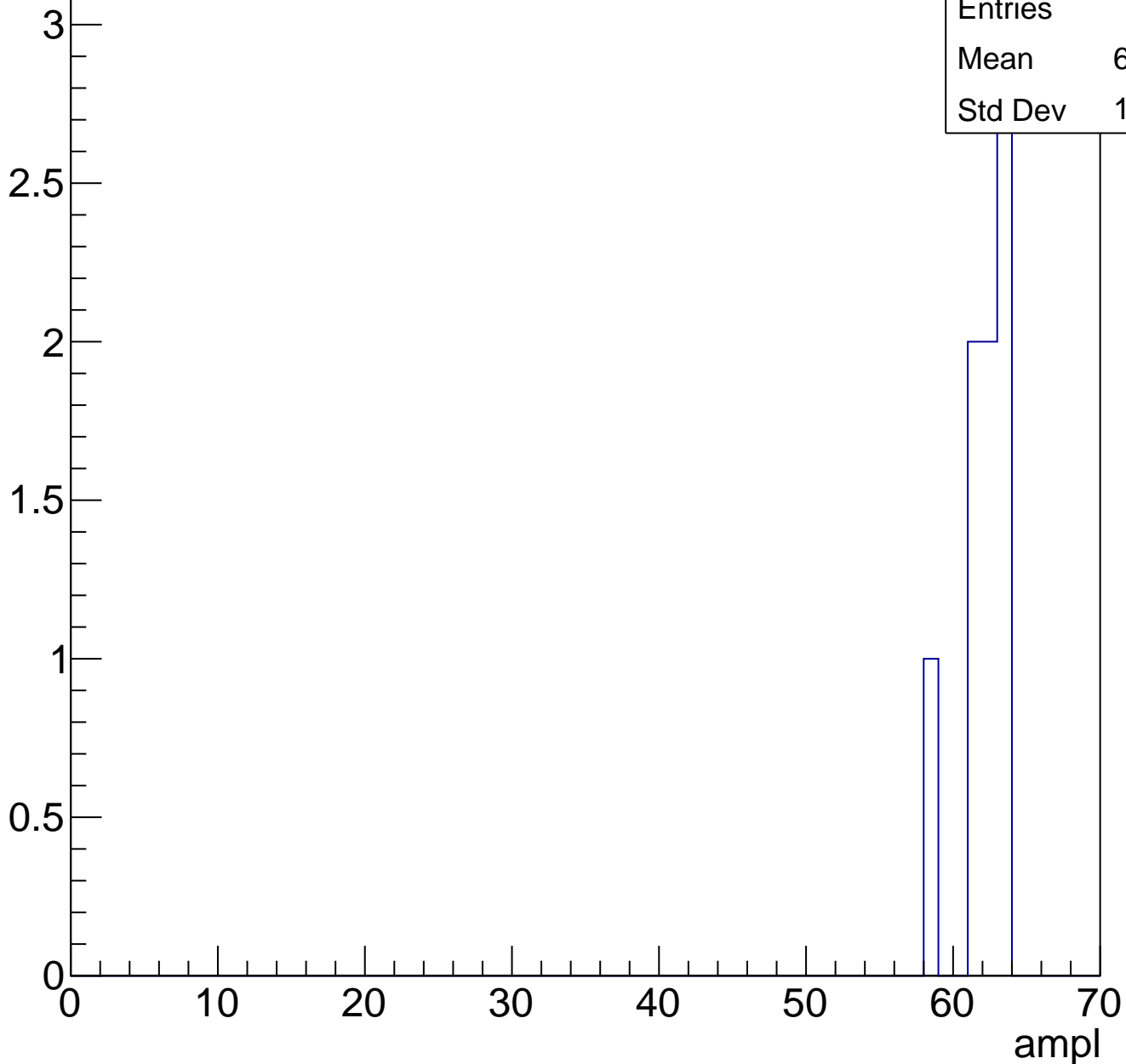
Entry



B1L103S, U12-ch60, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch60, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.105
Std Dev	4.689

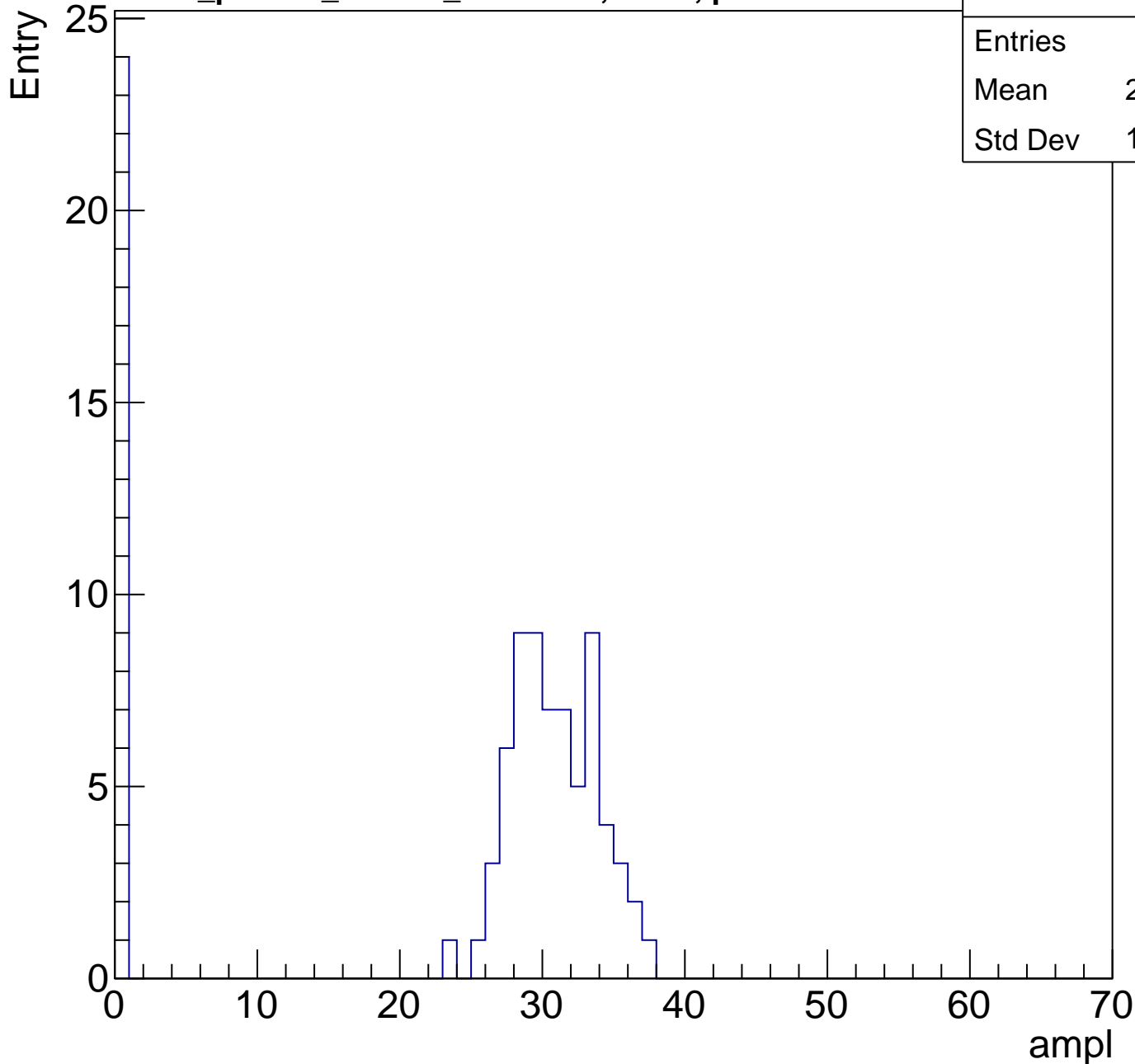
Entry



B1L103S, U12-ch61, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	91
Mean	22.36
Std Dev	13.62



B1L103S, U12-ch61, adc1

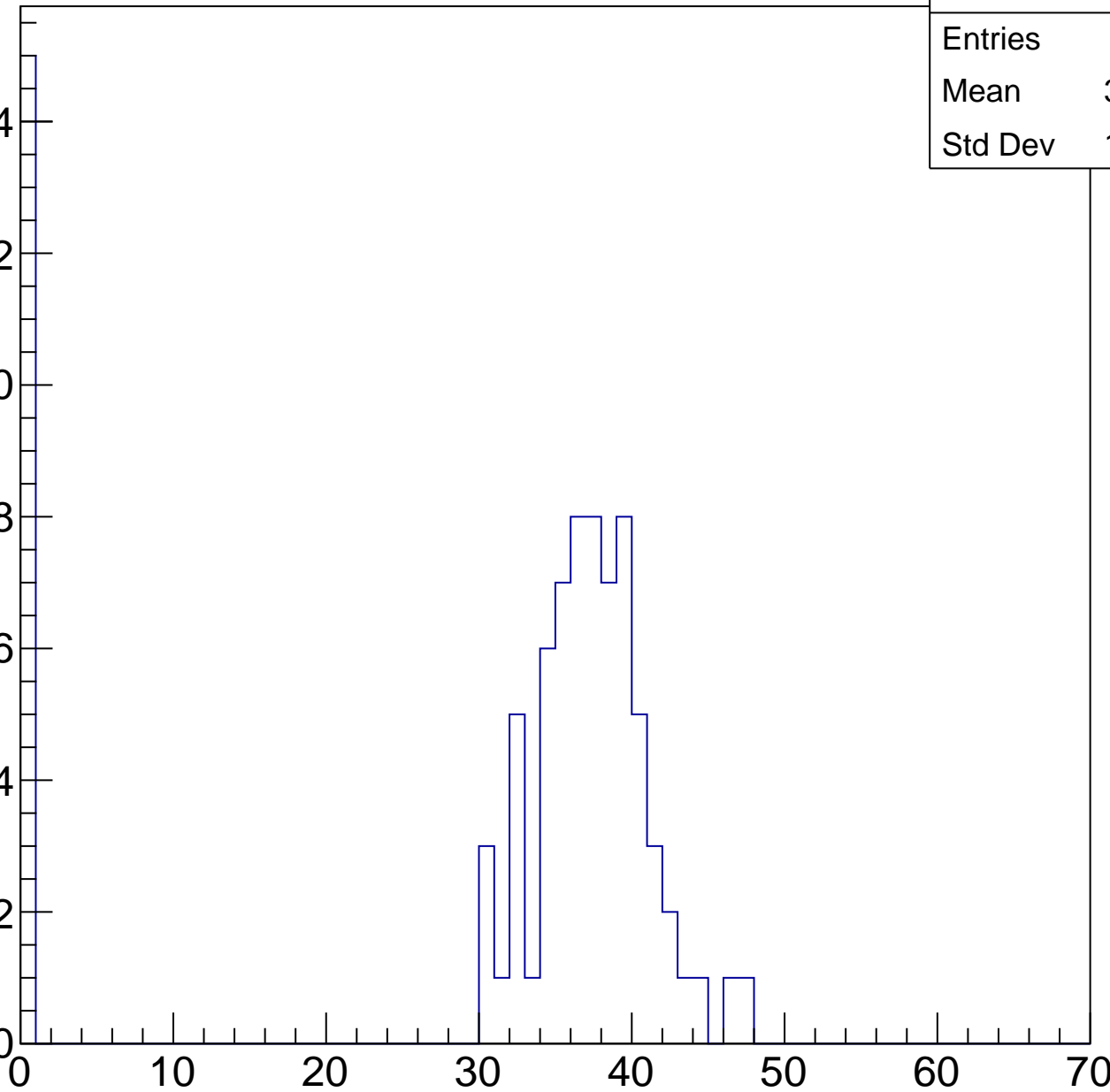
calib_packv5_041523_1651.root, FC#0, port C2

Entries	83
Mean	30.27
Std Dev	14.58

Entry

14
12
10
8
6
4
2
0

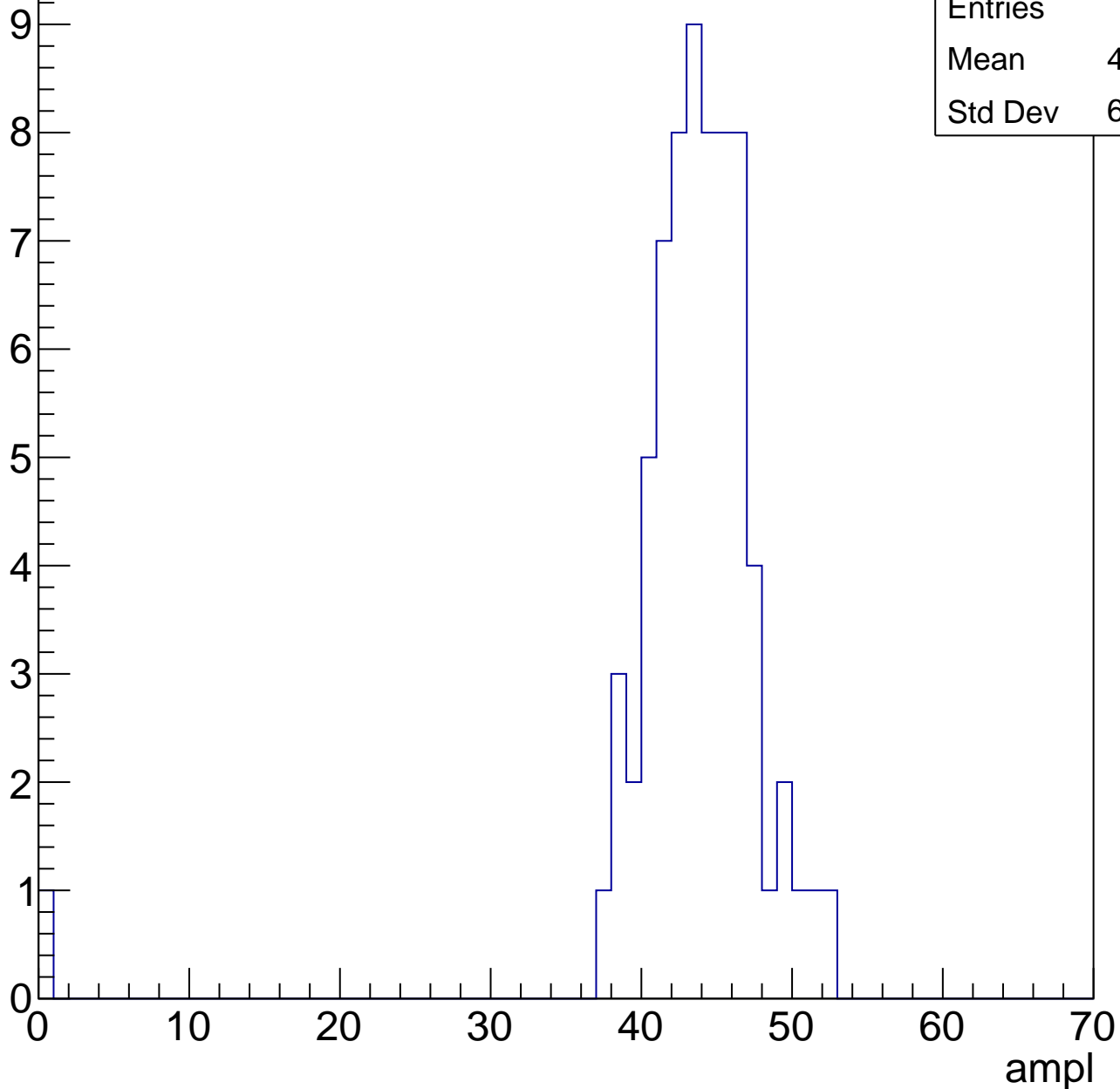
ampl



B1L103S, U12-ch61, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

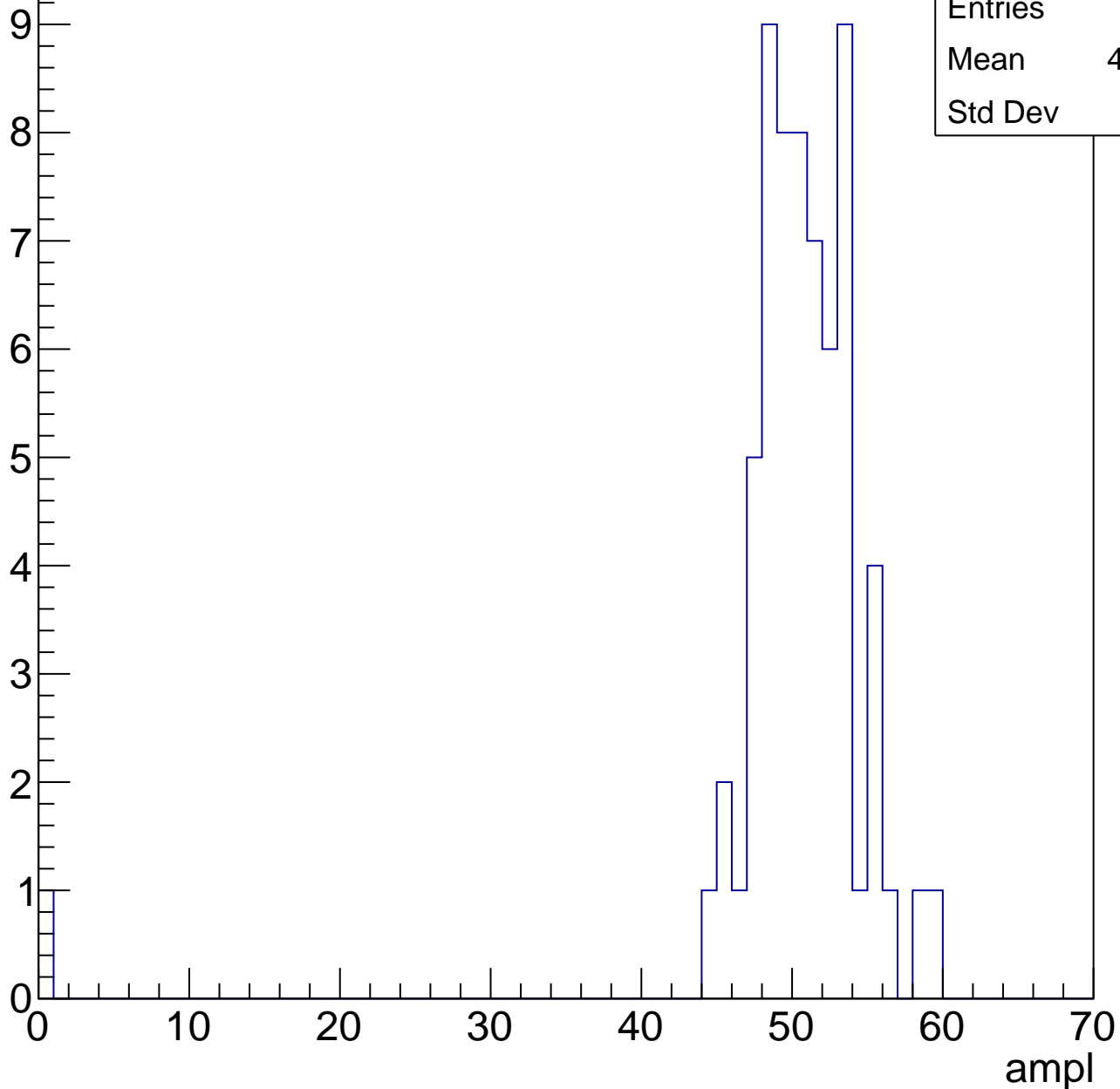


Entries	70
Mean	42.94
Std Dev	6.023

B1L103S, U12-ch61, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

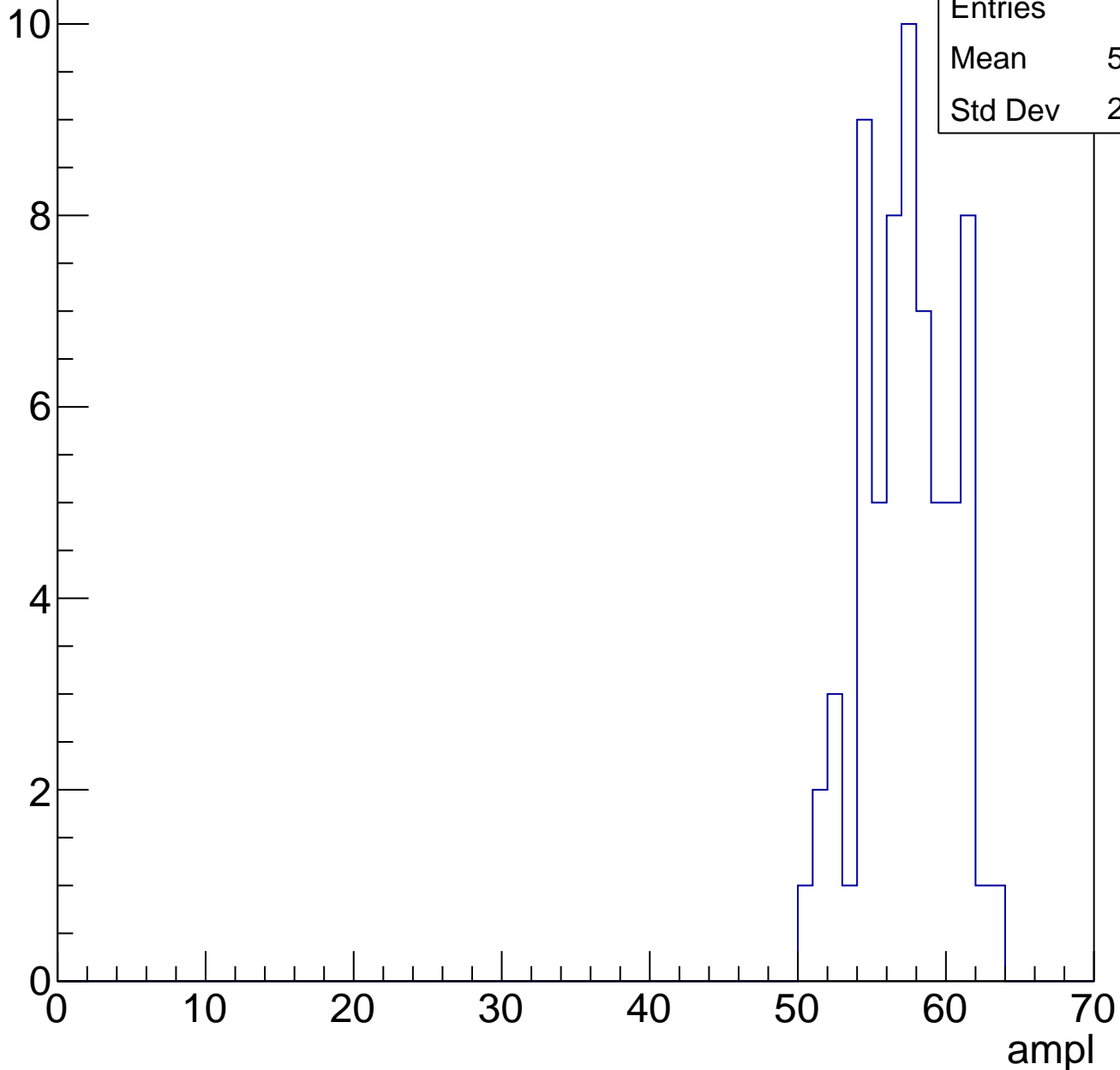


B1L103S, U12-ch61, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entries	66
Mean	56.88
Std Dev	2.967

Entry

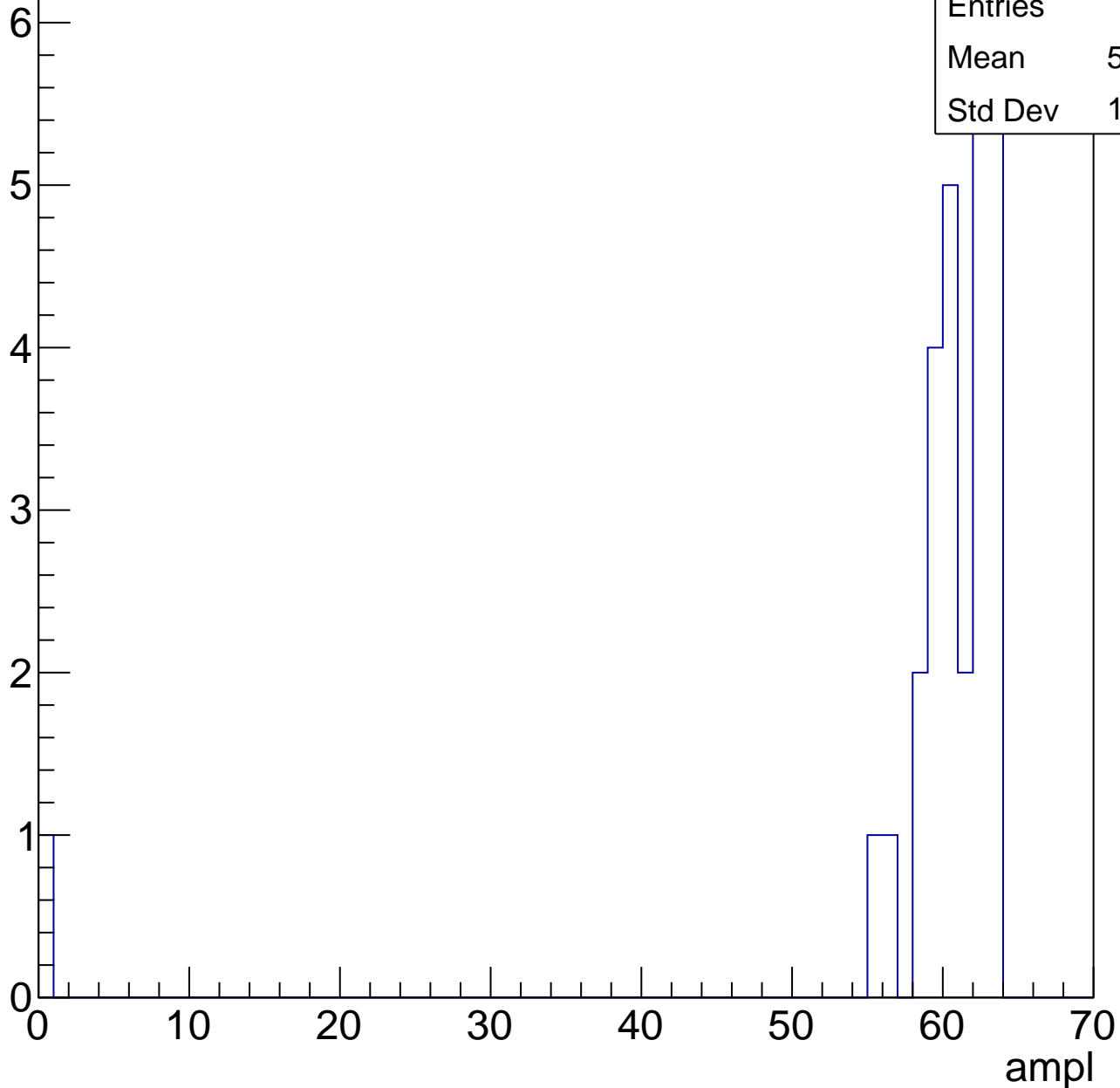


B1L103S, U12-ch61, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	28
Mean	58.39
Std Dev	11.43



B1L103S, U12-ch61, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch61, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.1
Std Dev	13.51

Entry

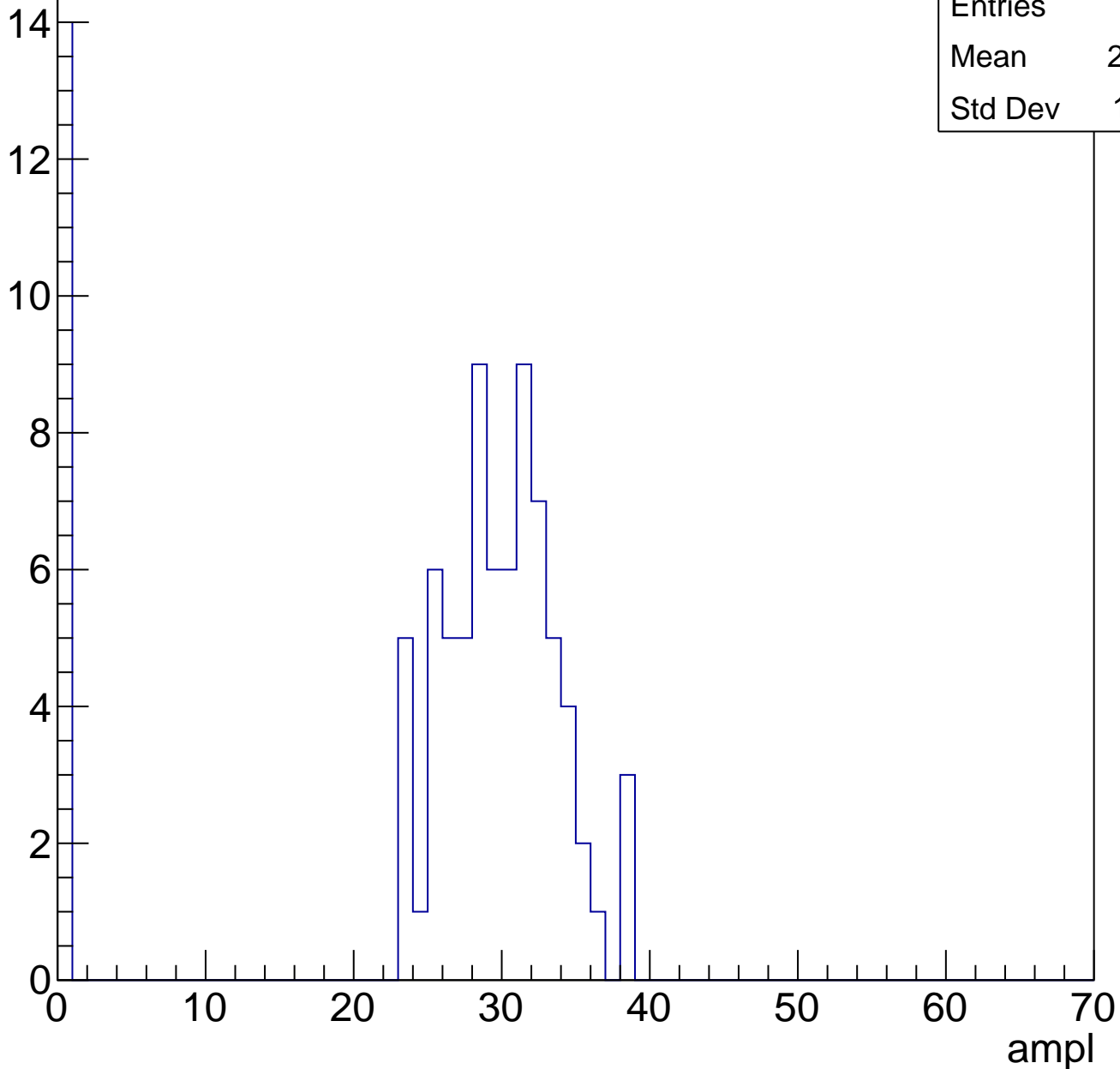


B1L103S, U12-ch62, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	88
Mean	24.82
Std Dev	11.31

Entry

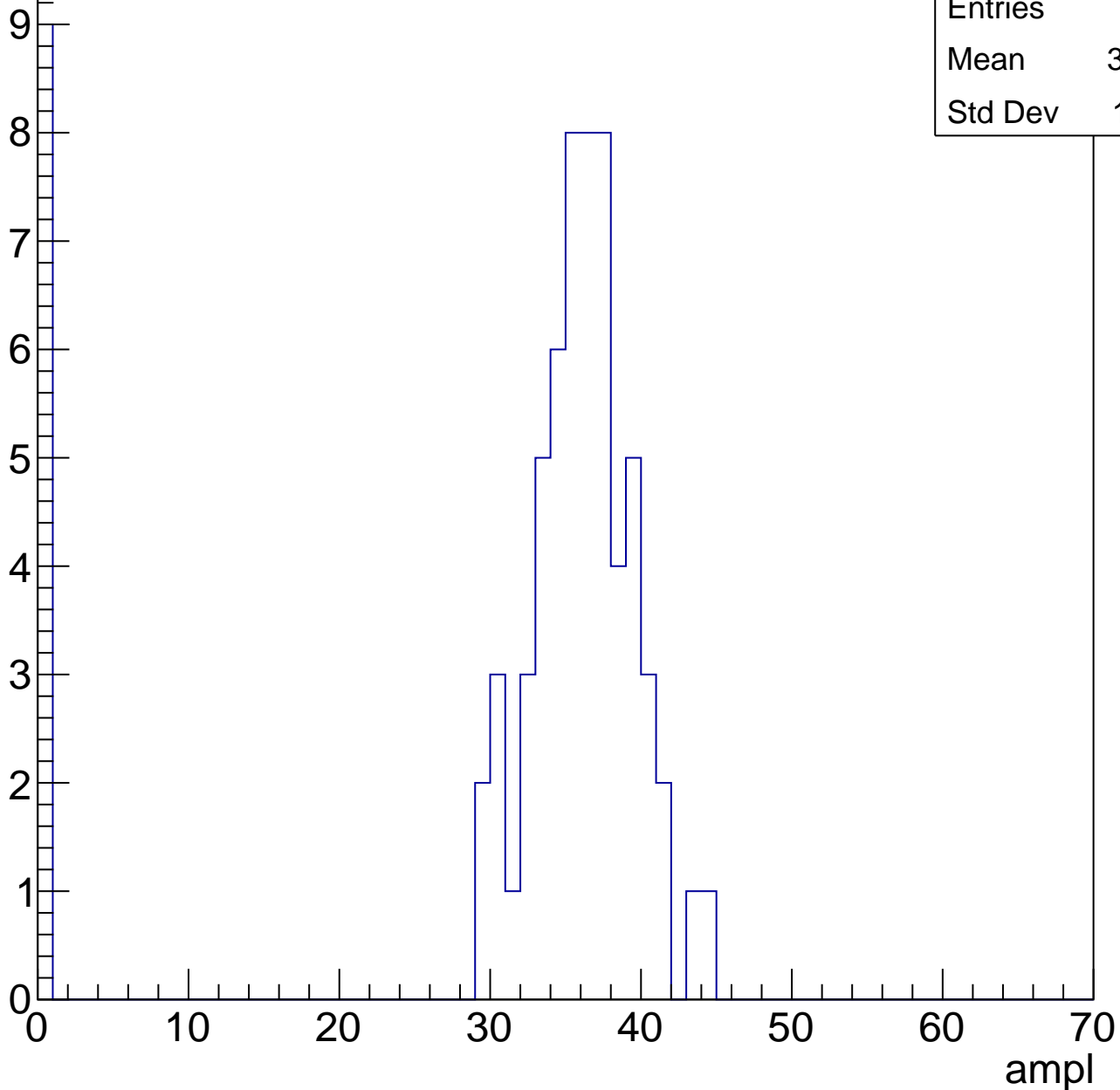


B1L103S, U12-ch62, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	31.07
Std Dev	12.41



B1L103S, U12-ch62, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

10

Entries 77

Mean 41.56

Std Dev 7.358

8

6

4

2

0

0

10

20

30

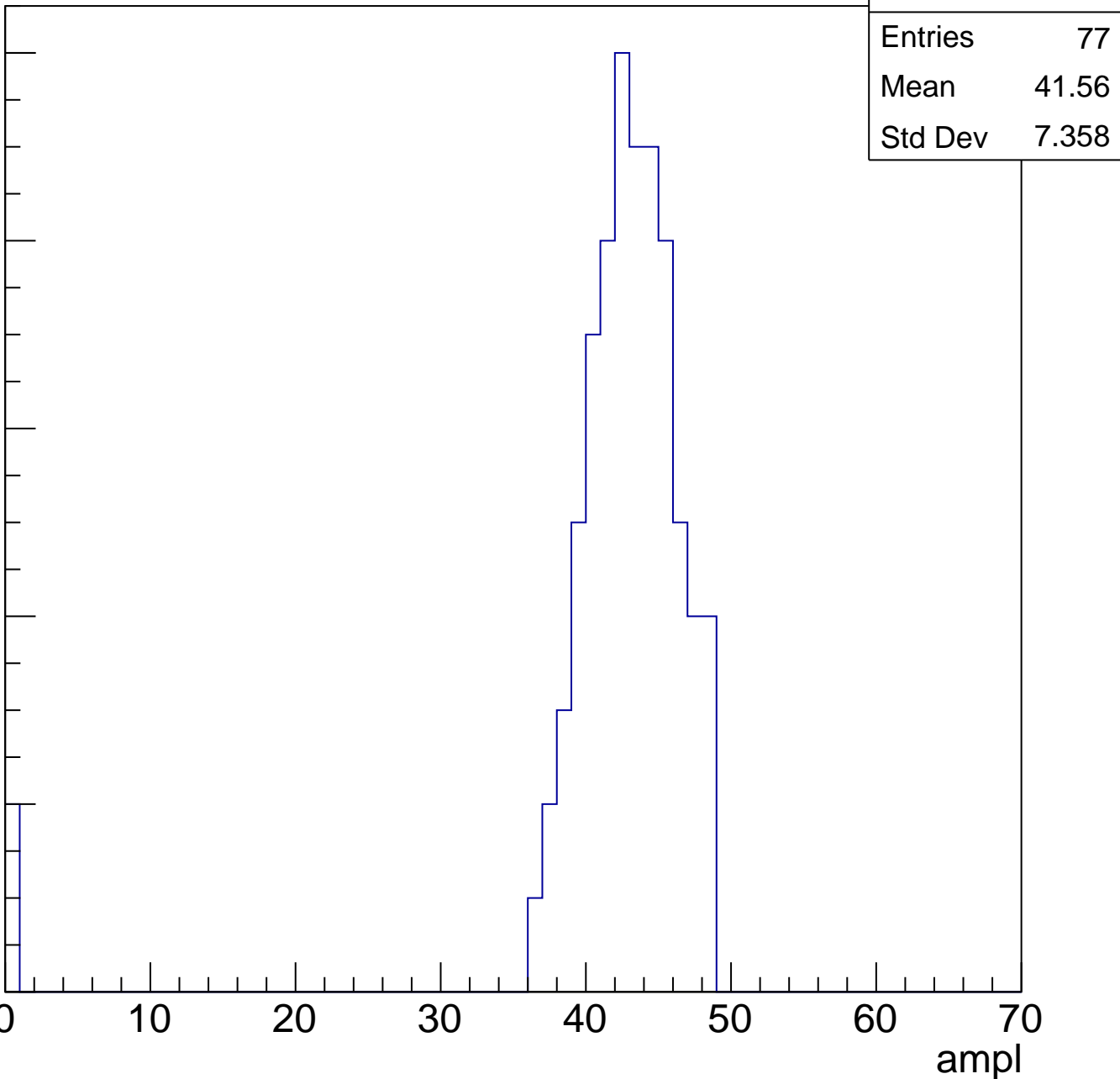
40

50

60

70

ampl

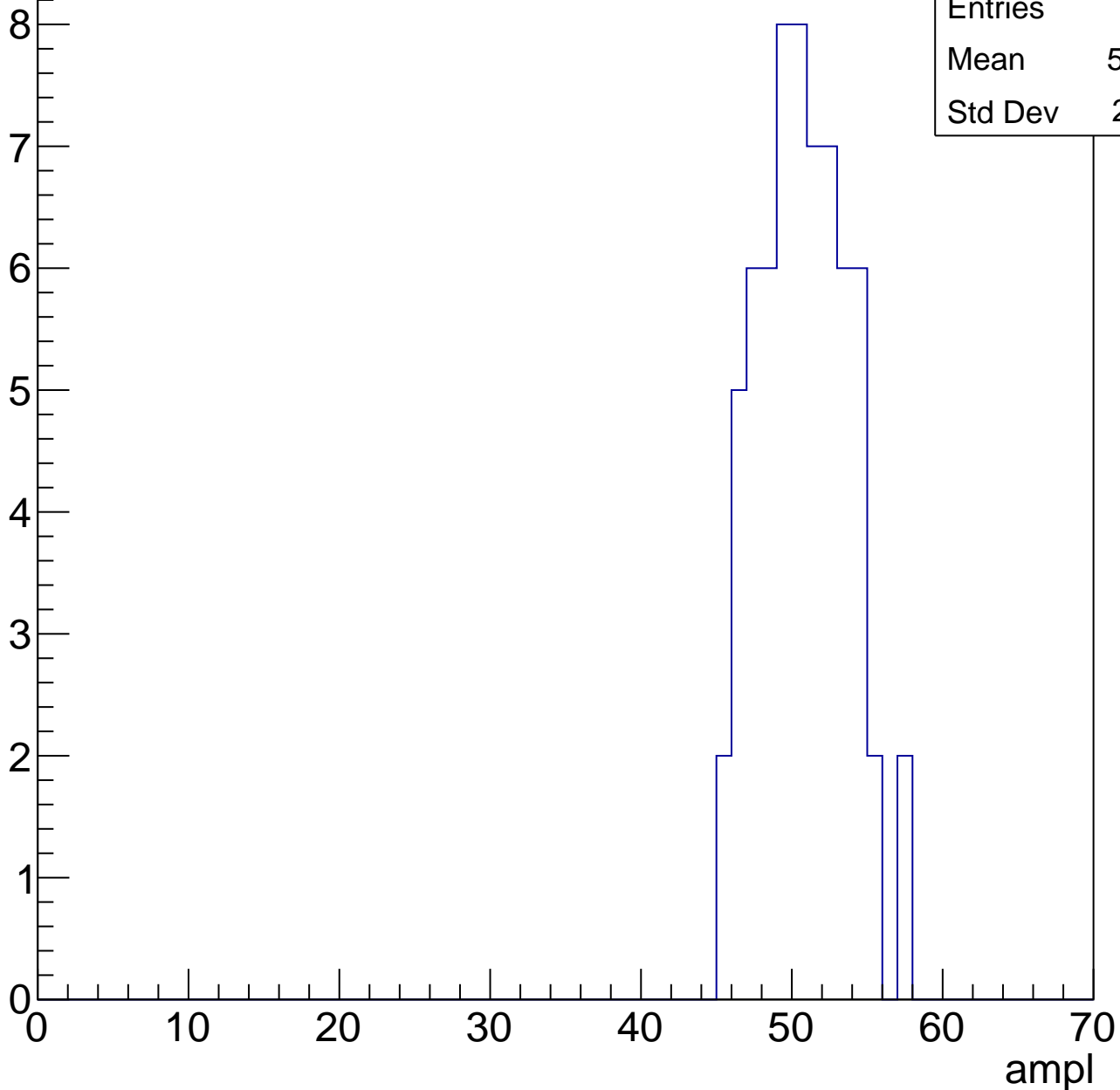


B1L103S, U12-ch62, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	50.29
Std Dev	2.891

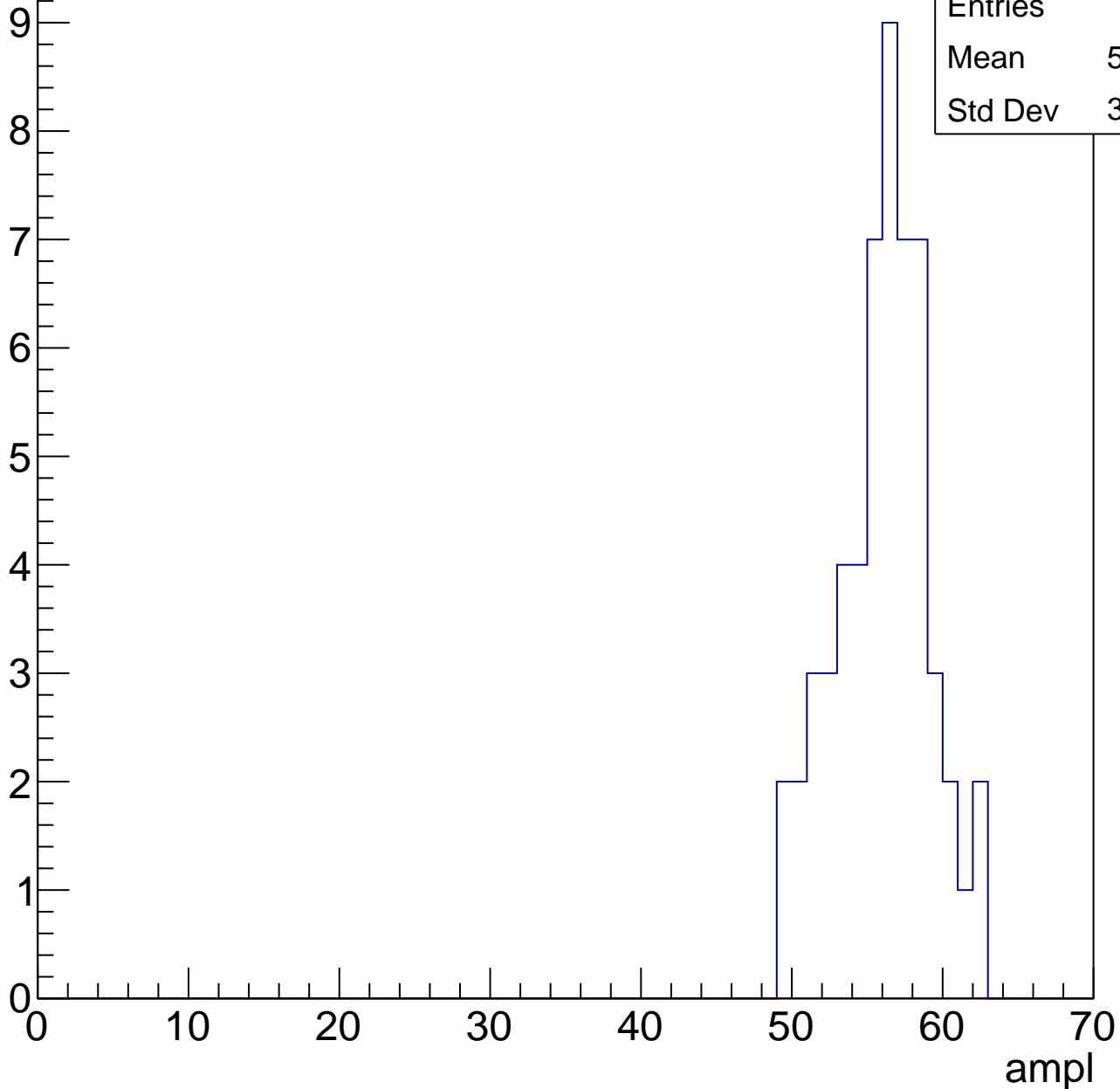


B1L103S, U12-ch62, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	56
Mean	55.55
Std Dev	3.082

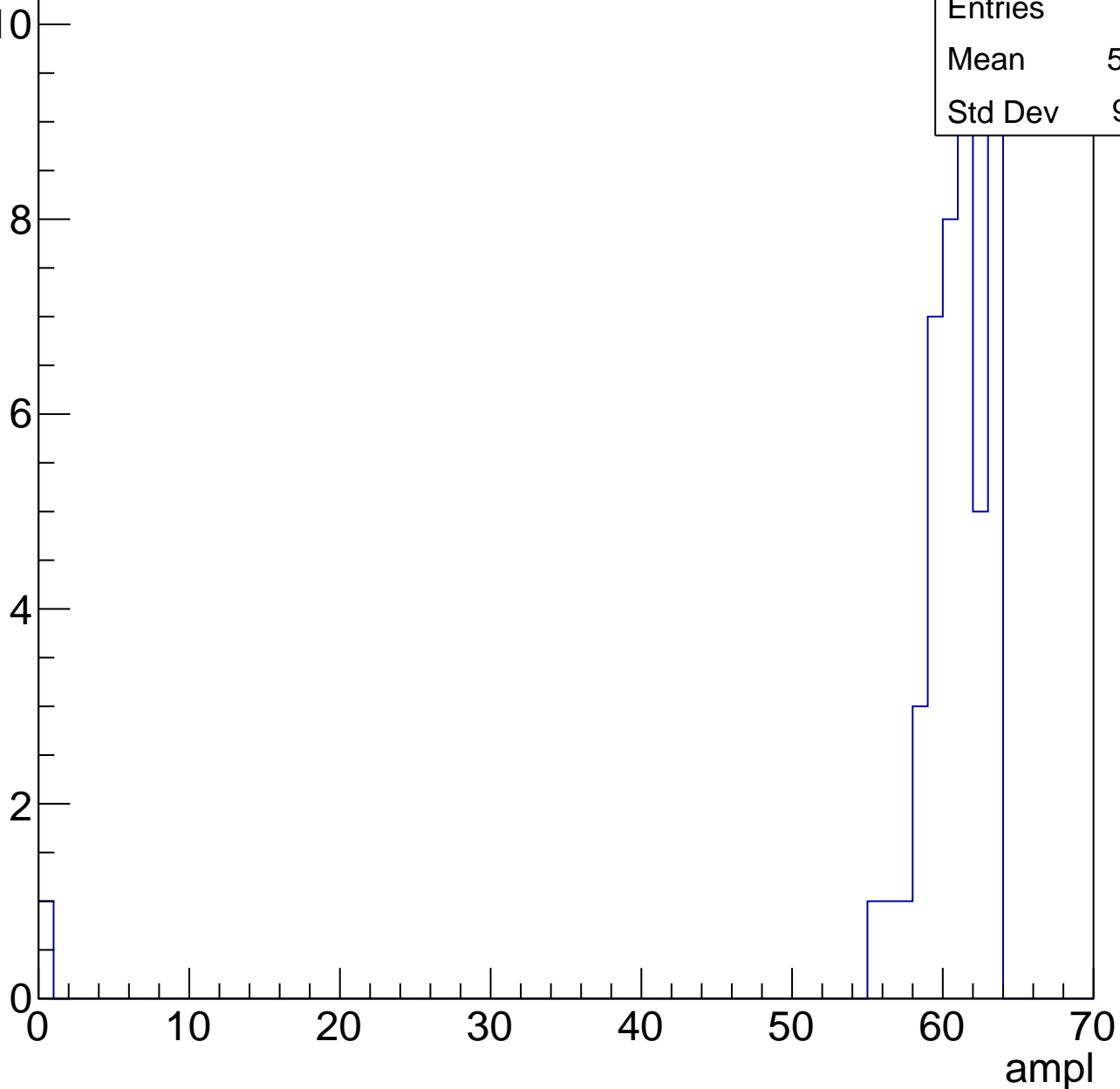


B1L103S, U12-ch62, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	46
Mean	59.22
Std Dev	9.041



B1L103S, U12-ch62, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries

3

Mean

62

Std Dev

0

B1L103S, U12-ch62, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

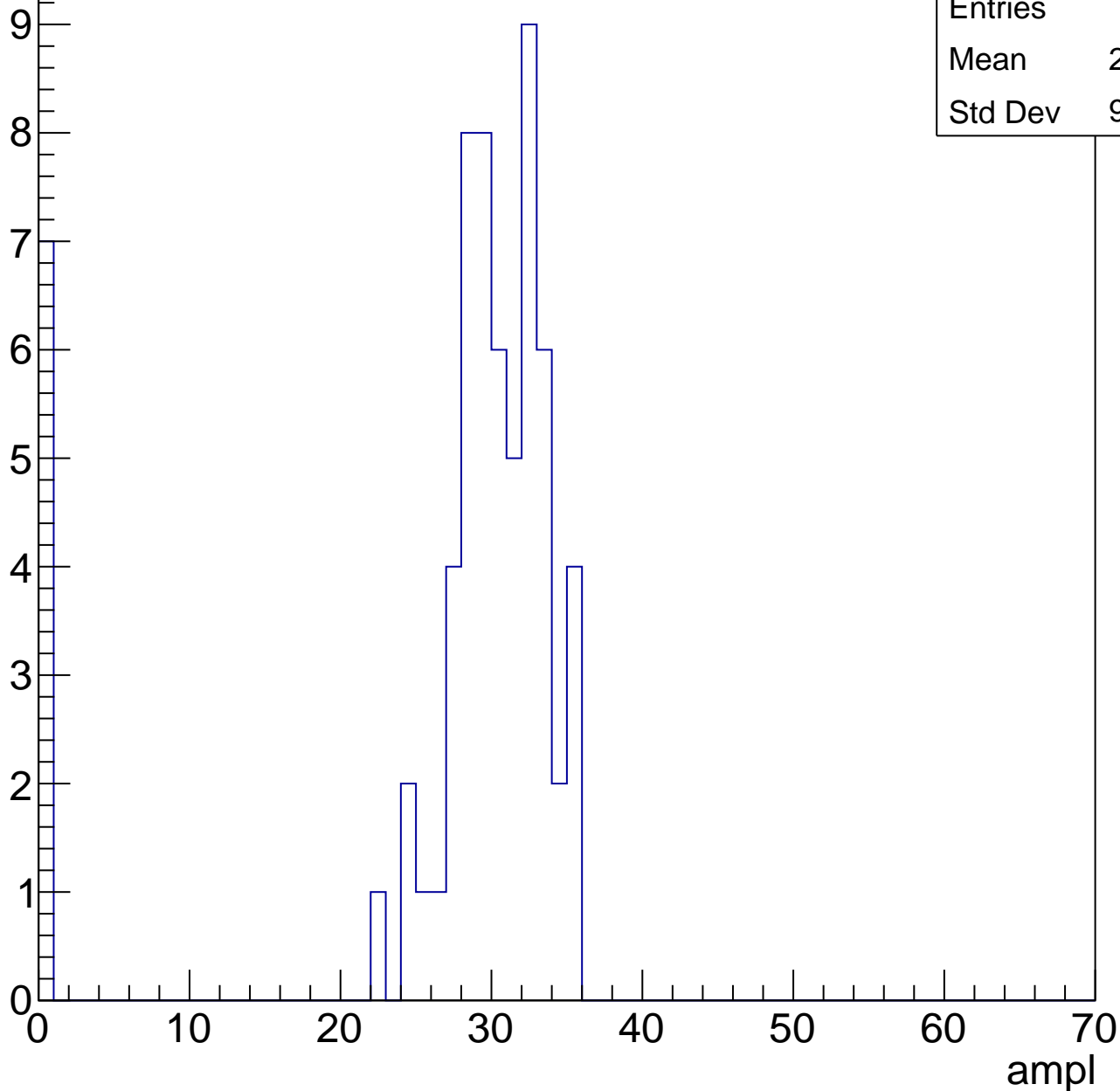


B1L103S, U12-ch63, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	26.78
Std Dev	9.776

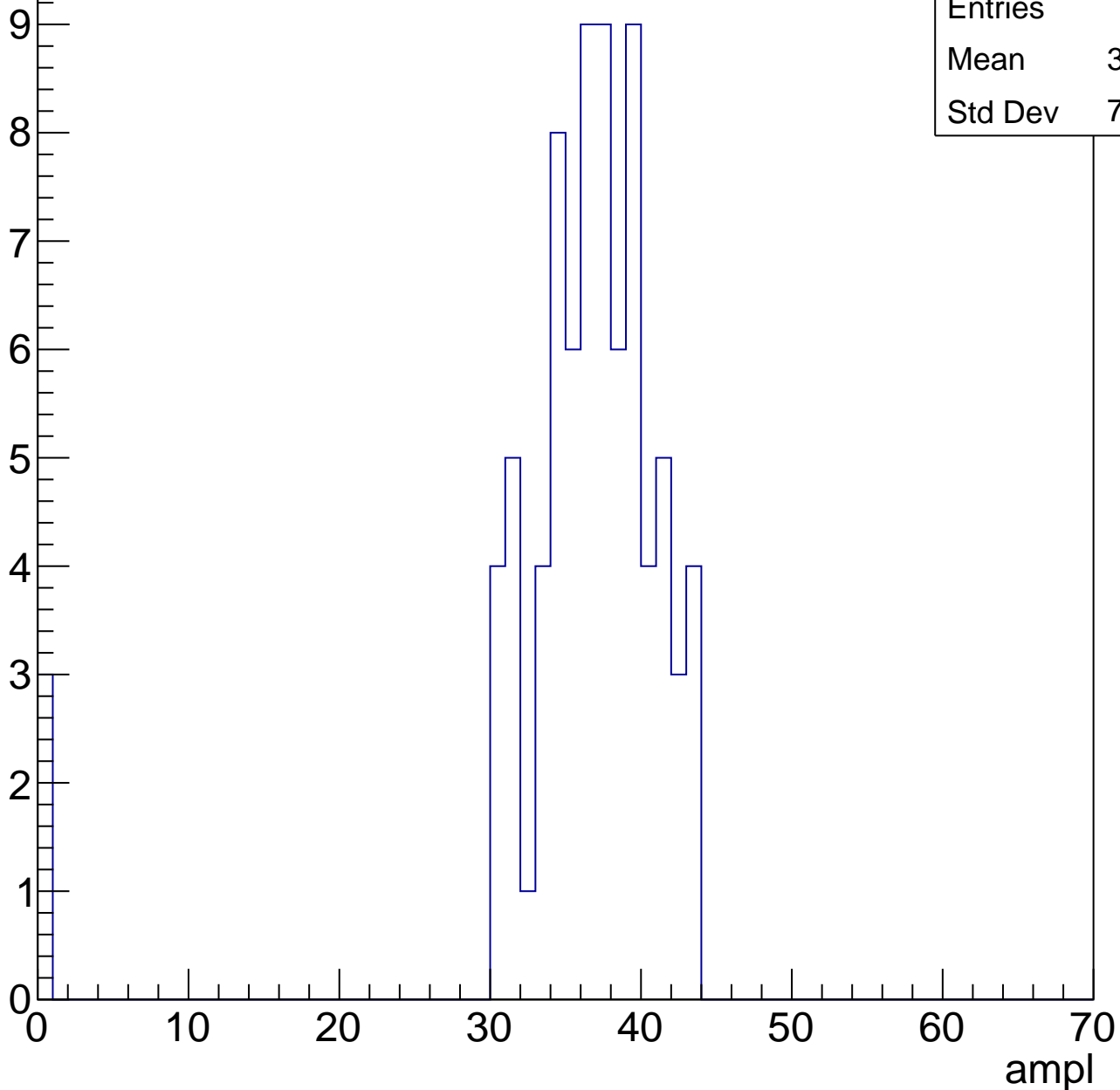


B1L103S, U12-ch63, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	80
Mean	35.25
Std Dev	7.753

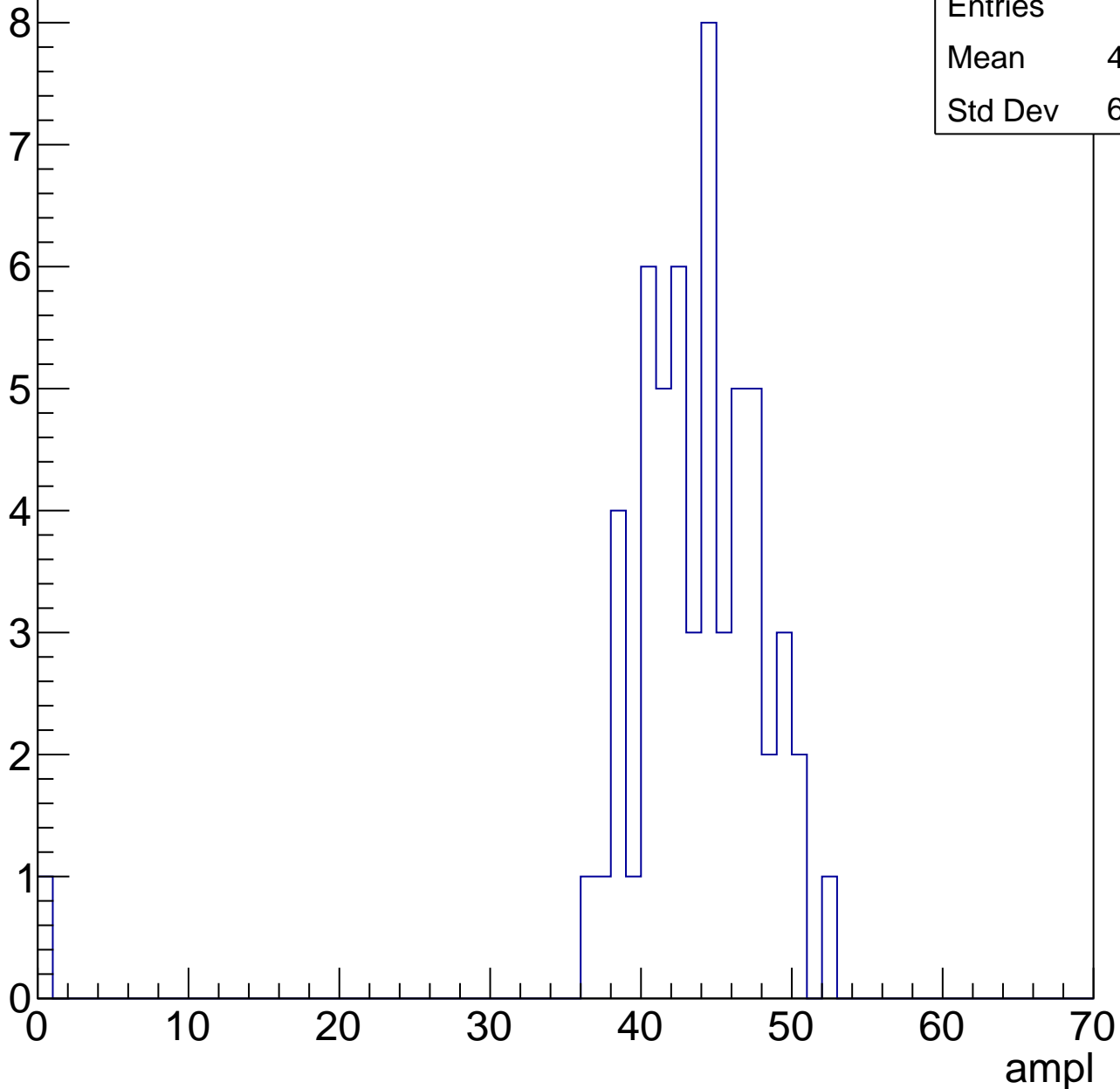


B1L103S, U12-ch63, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	57
Mean	42.75
Std Dev	6.765

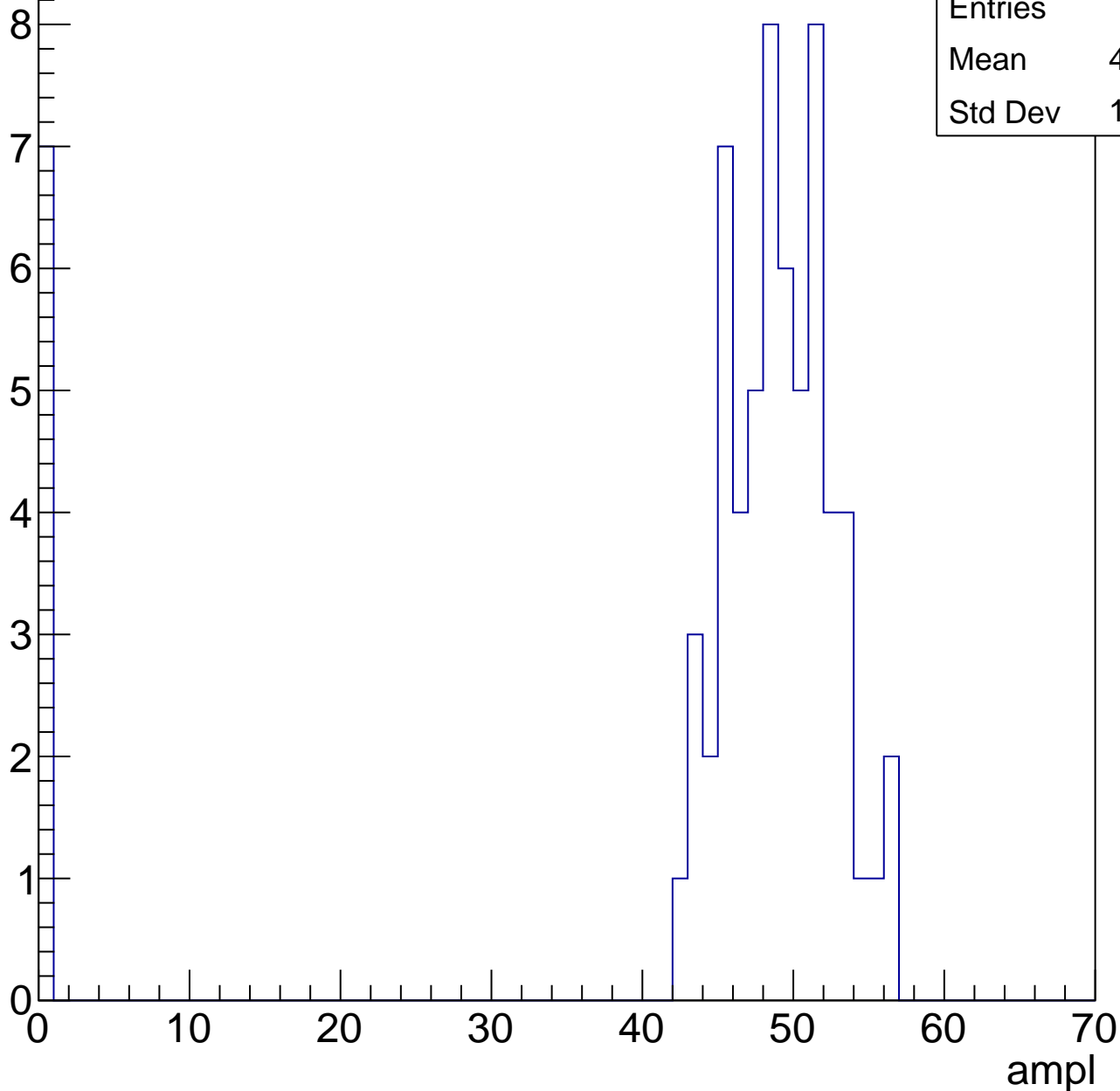


B1L103S, U12-ch63, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	43.68
Std Dev	15.13

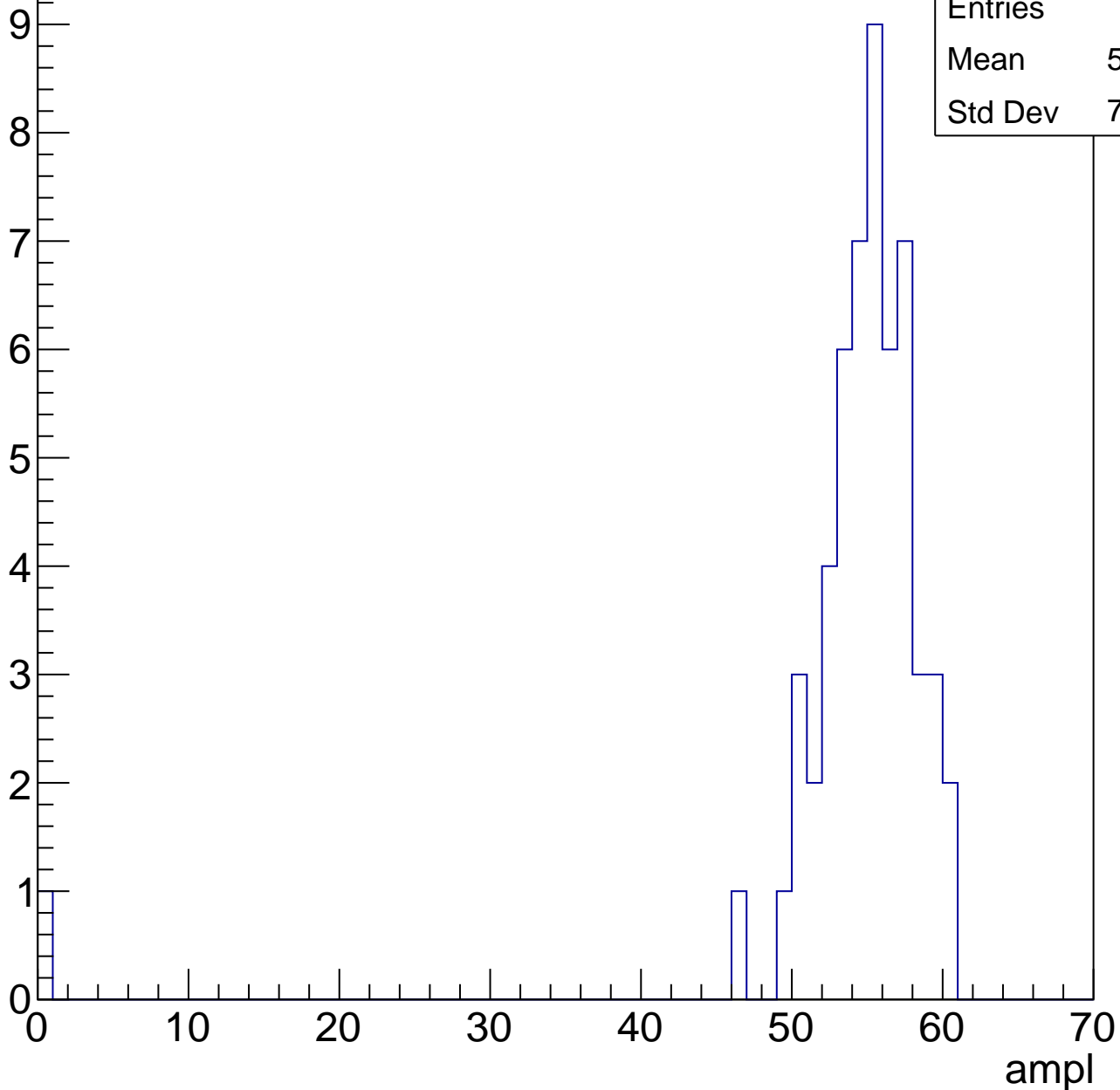


B1L103S, U12-ch63, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	53.67
Std Dev	7.837

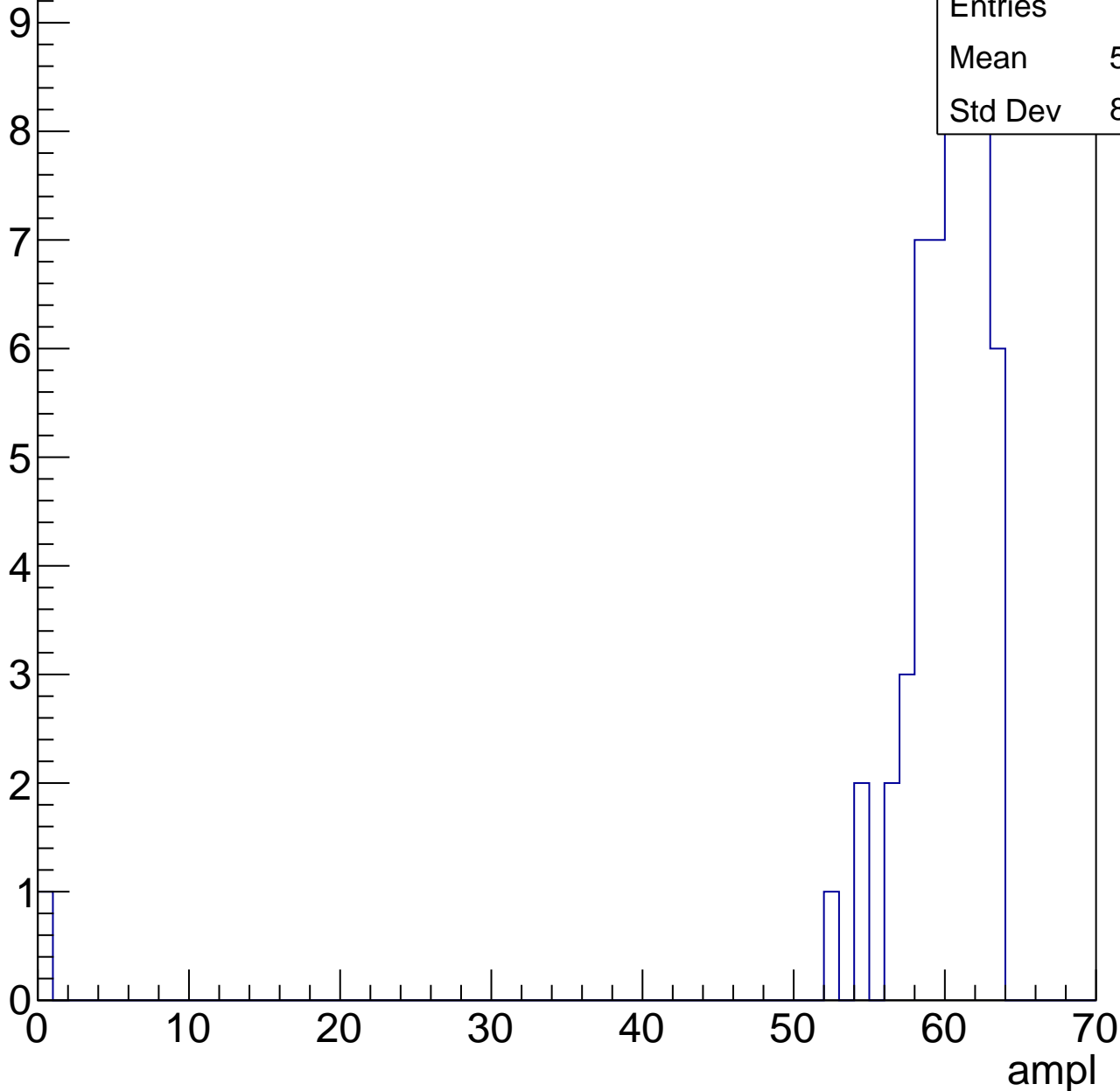


B1L103S, U12-ch63, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	58.67
Std Dev	8.347



B1L103S, U12-ch63, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

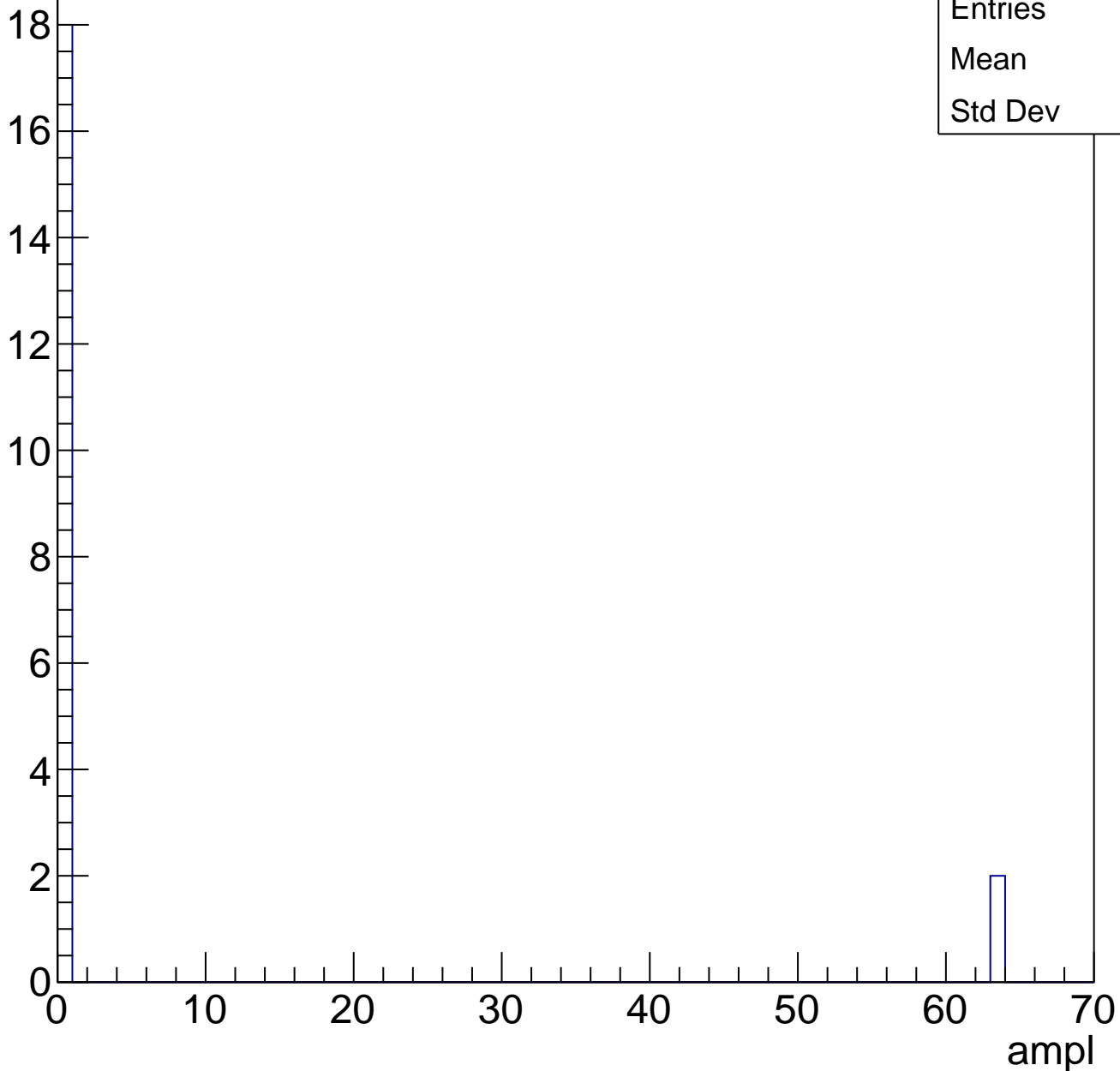


B1L103S, U12-ch63, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	6.3
Std Dev	18.9

Entry

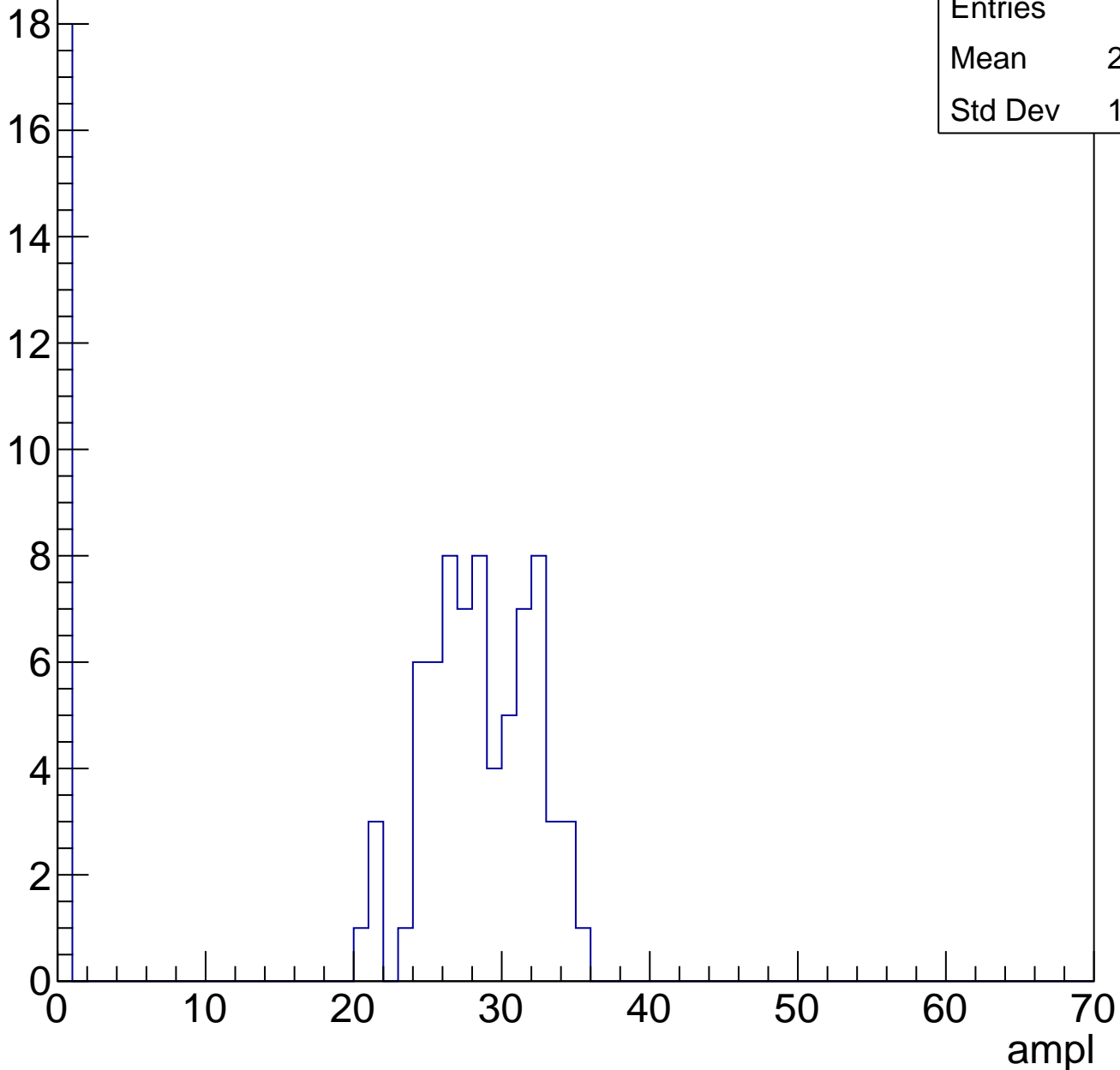


B1L103S, U12-ch64, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	89
Mean	22.43
Std Dev	11.72

Entry

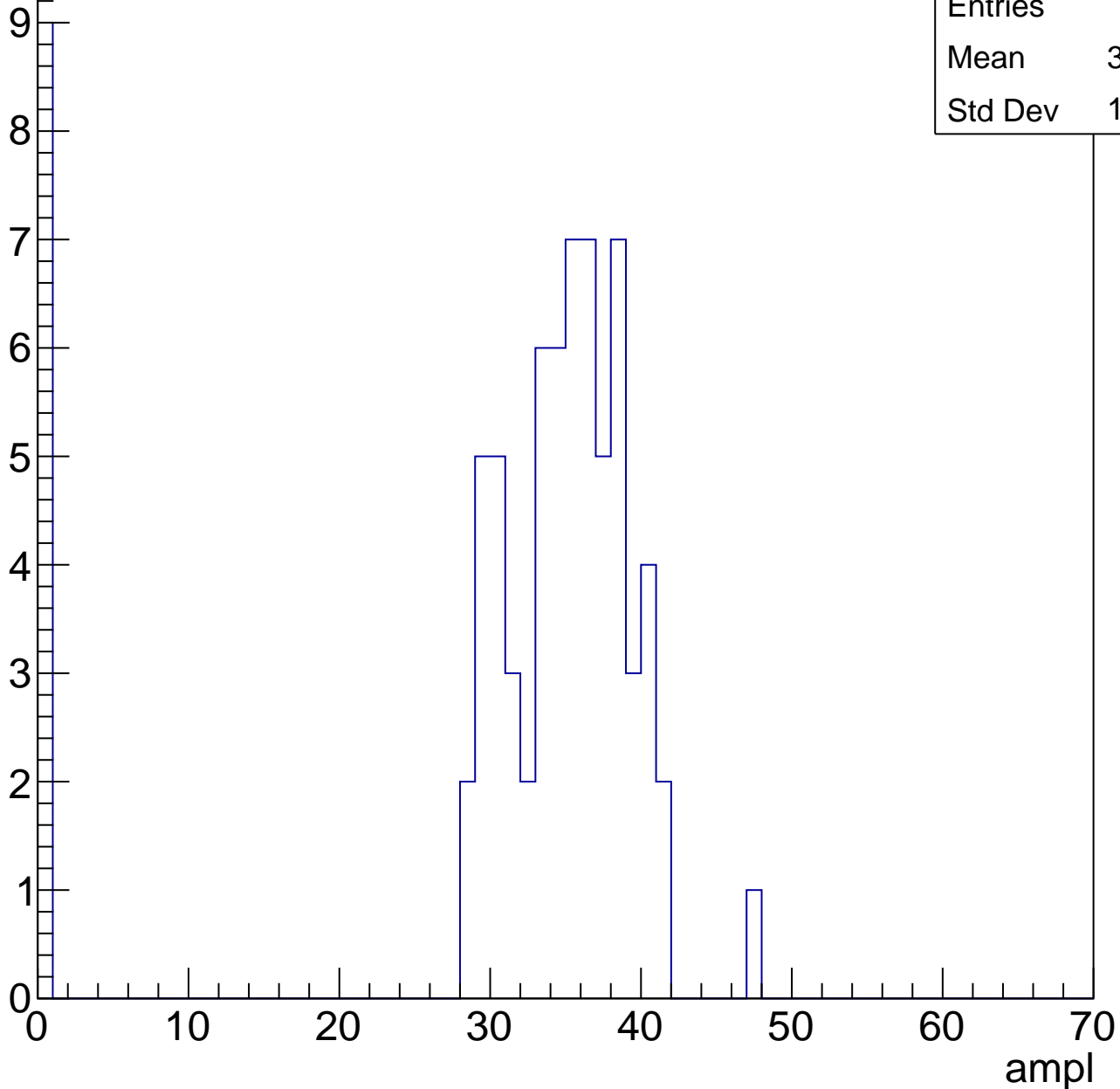


B1L103S, U12-ch64, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	74
Mean	30.59
Std Dev	11.94

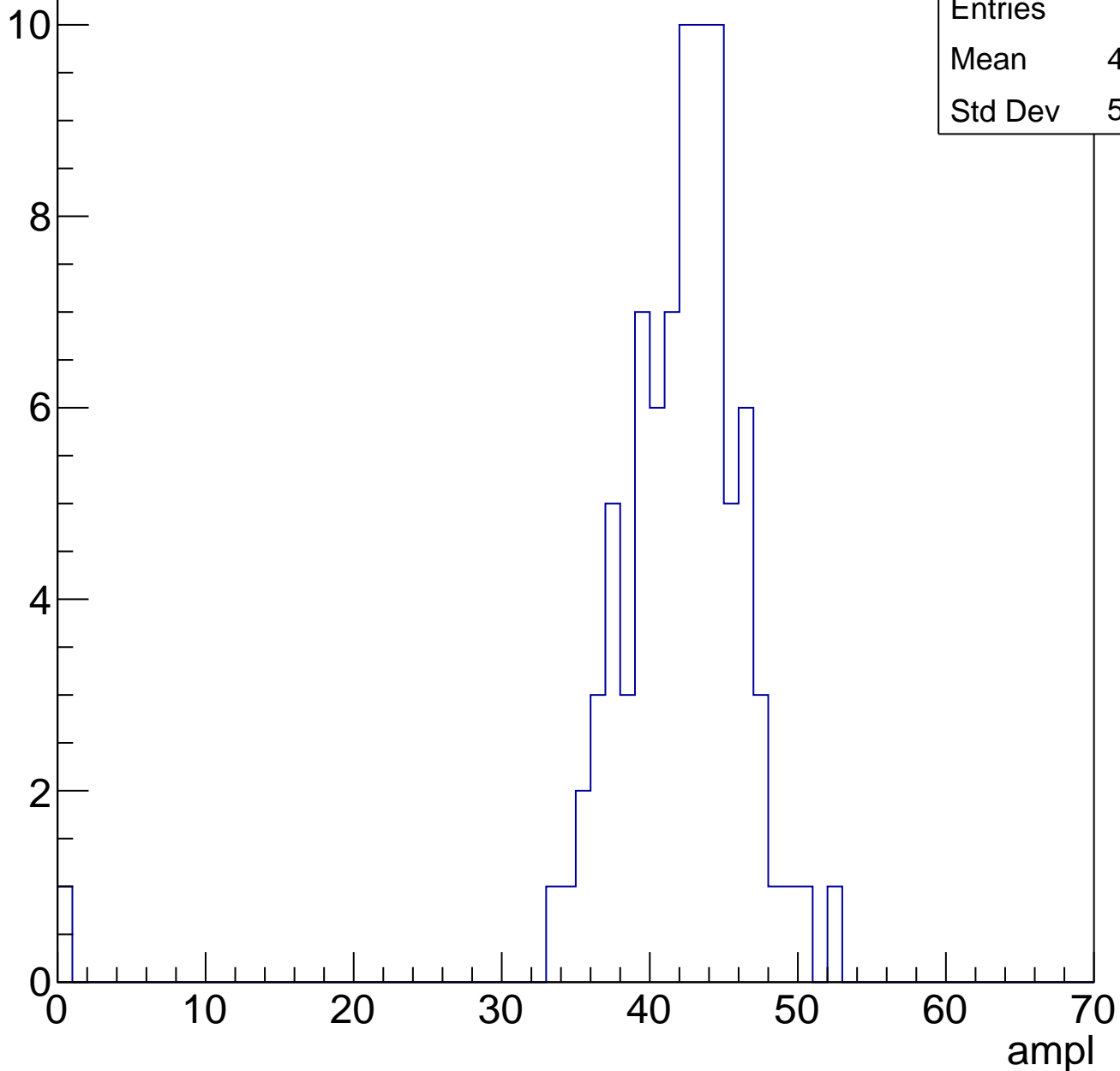


B1L103S, U12-ch64, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	84
Mean	41.37
Std Dev	5.839

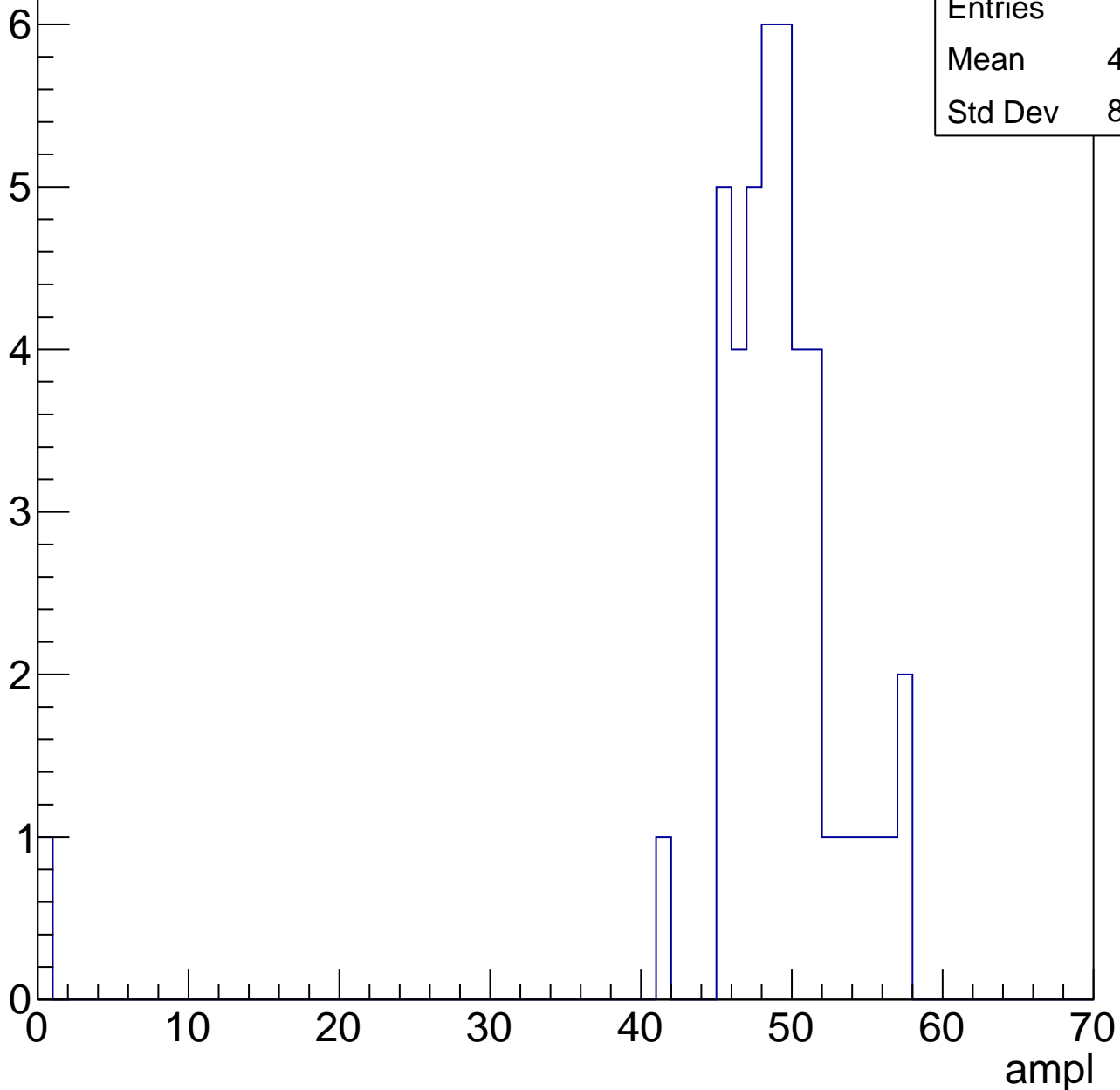


B1L103S, U12-ch64, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	43
Mean	47.79
Std Dev	8.108

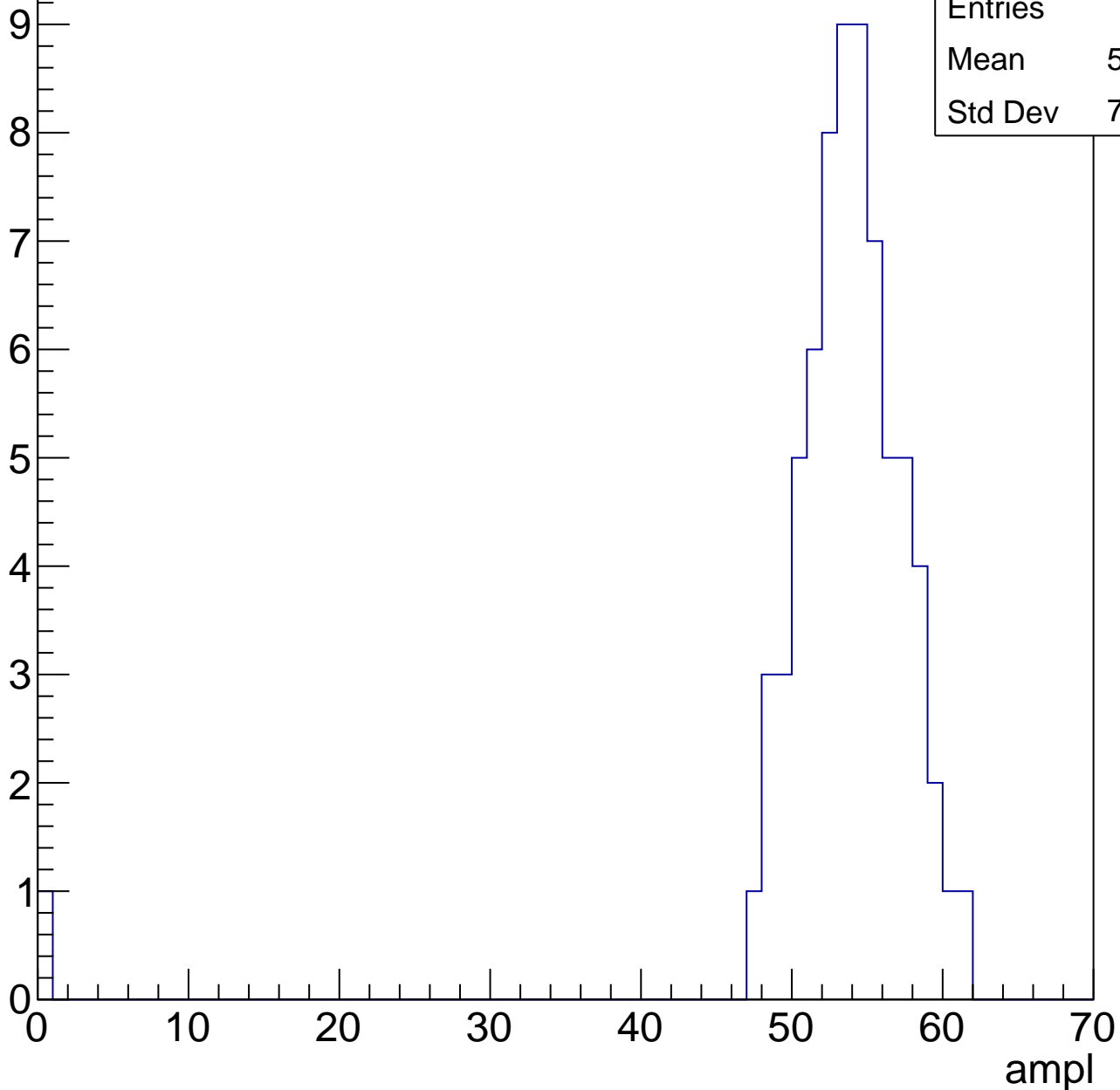


B1L103S, U12-ch64, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	52.77
Std Dev	7.059

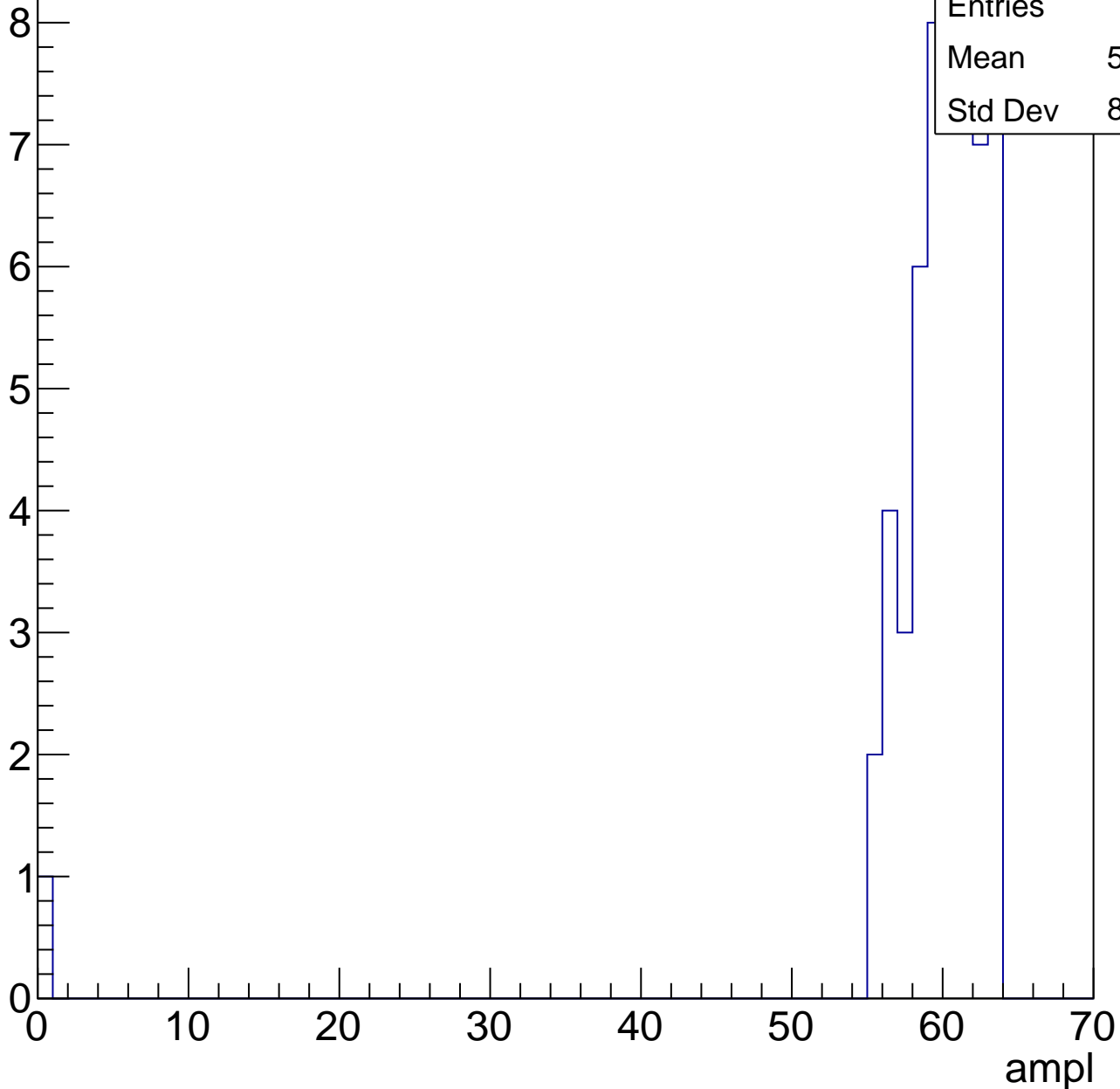


B1L103S, U12-ch64, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	58.75
Std Dev	8.306



B1L103S, U12-ch64, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch64, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

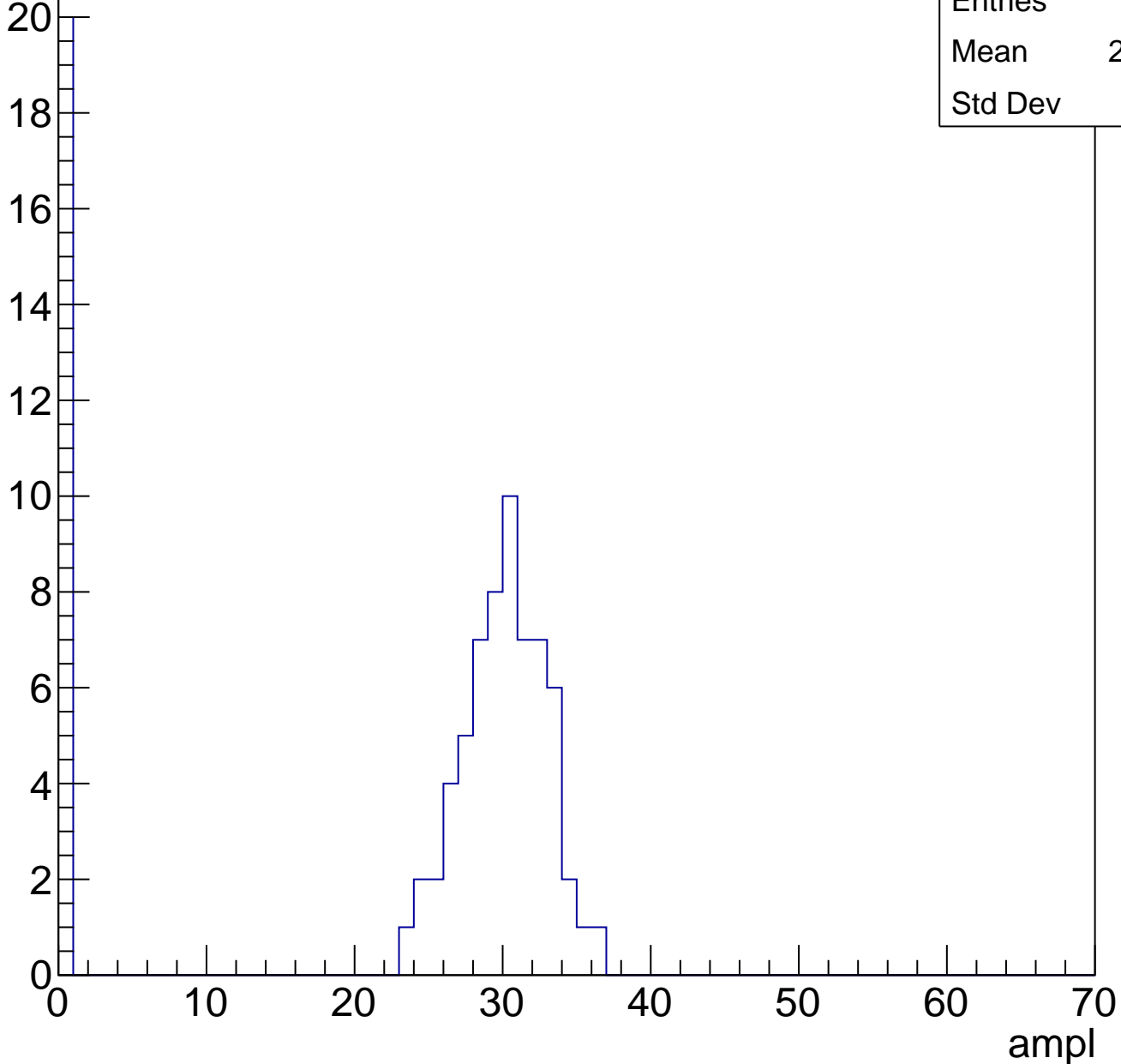
Entries	19
Mean	0
Std Dev	0

B1L103S, U12-ch65, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	83
Mean	22.48
Std Dev	12.9

Entry

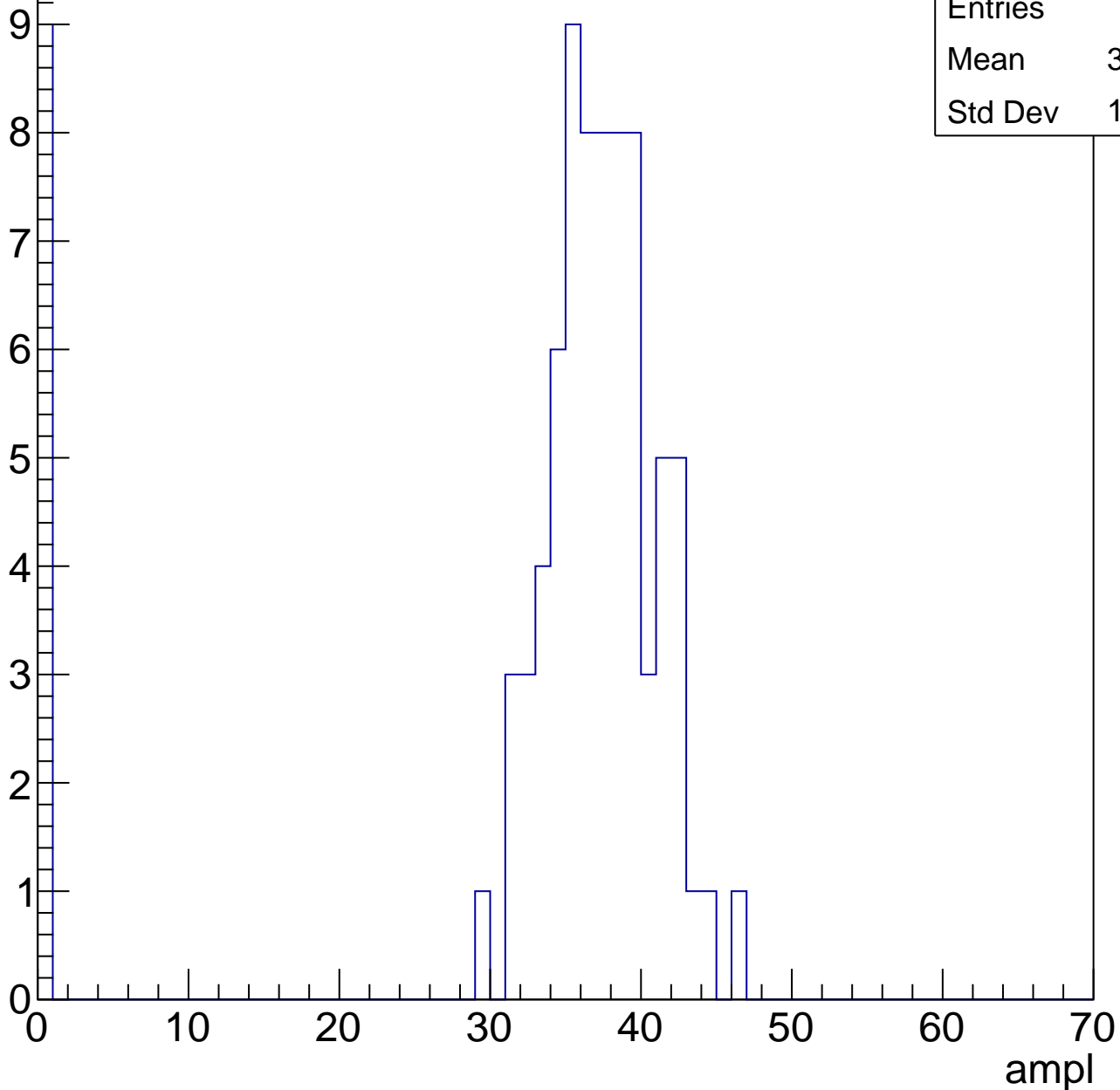


B1L103S, U12-ch65, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	83
Mean	32.98
Std Dev	11.94

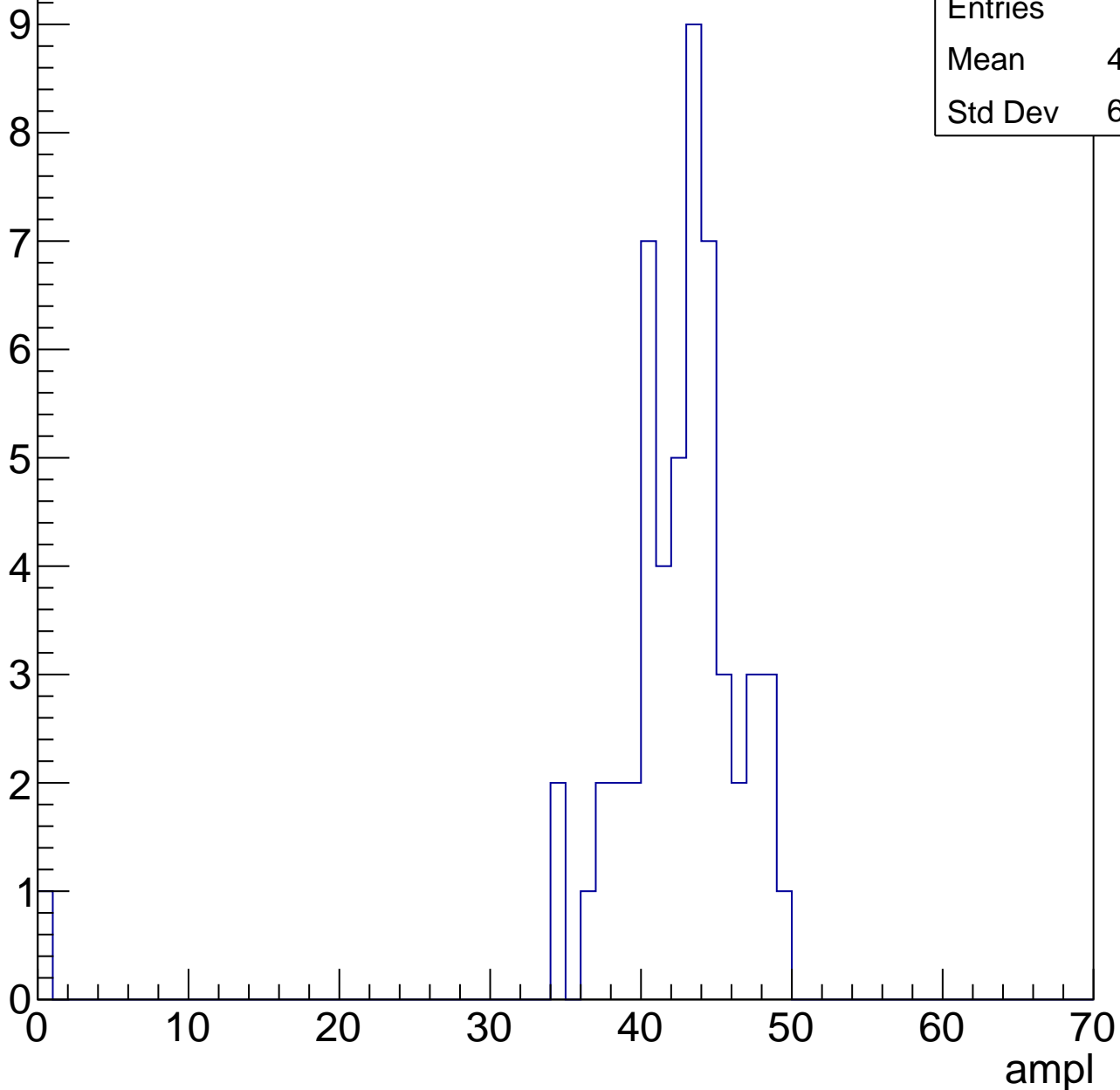


B1L103S, U12-ch65, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	54
Mean	41.52
Std Dev	6.633



B1L103S, U12-ch65, adc3

calib_packv5_041523_1651.root, FC#0, port C2

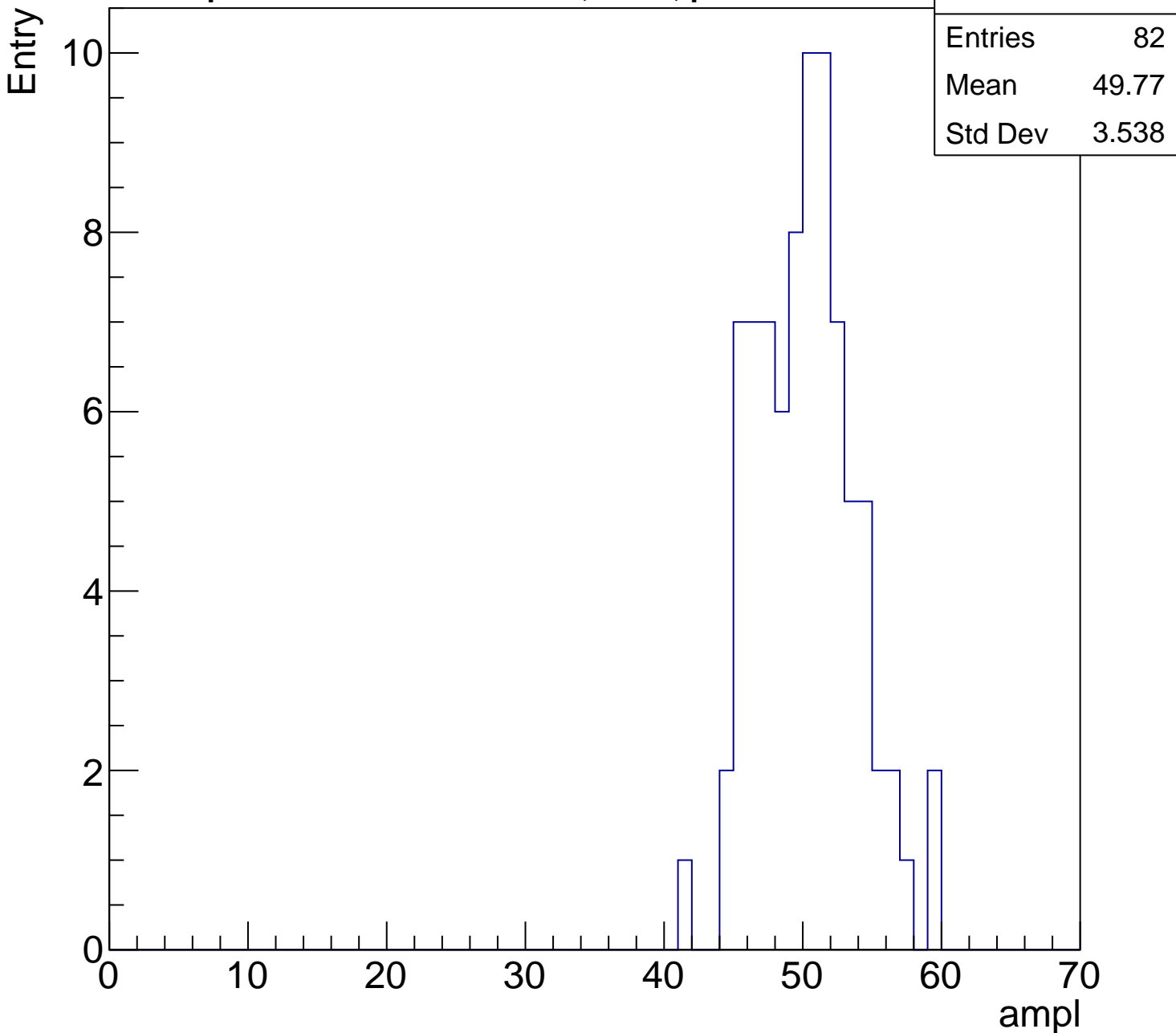
Entries	82
Mean	49.77
Std Dev	3.538

Entry

10
8
6
4
2
0

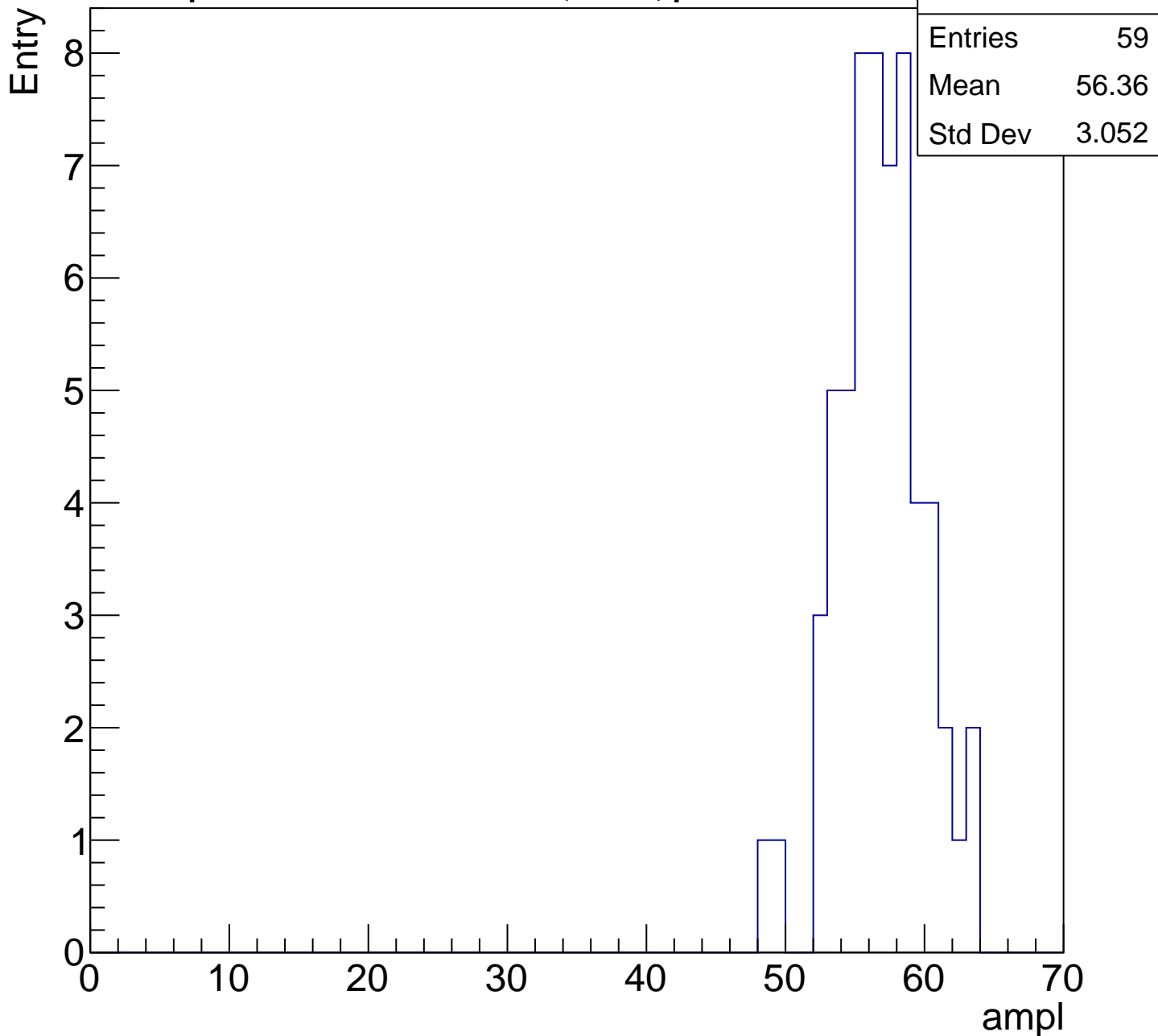
0 10 20 30 40 50 60 70

ampl



B1L103S, U12-ch65, adc4

calib_packv5_041523_1651.root, FC#0, port C2

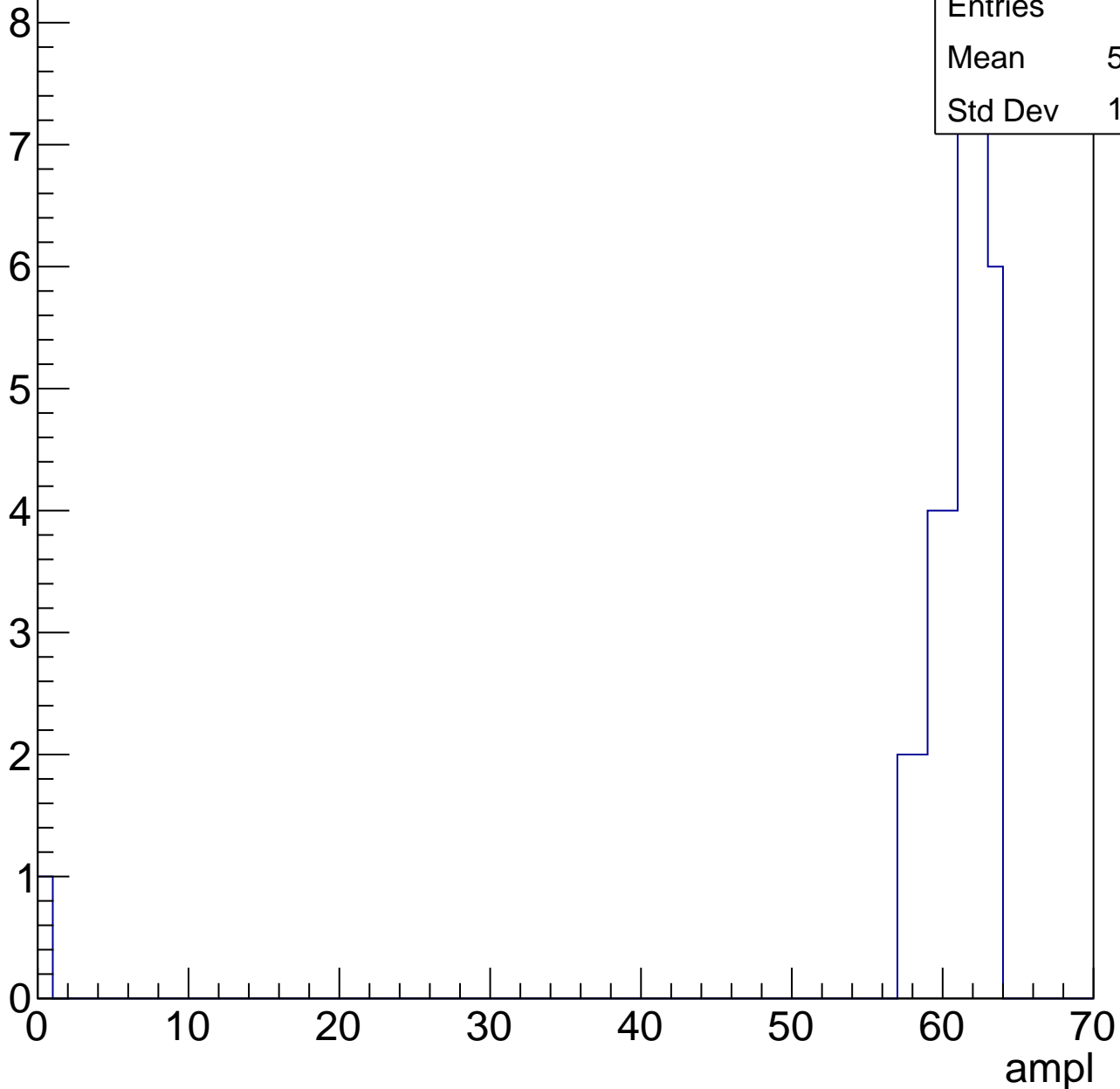


B1L103S, U12-ch65, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	35
Mean	59.09
Std Dev	10.27



B1L103S, U12-ch65, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	5
Mean	61.6
Std Dev	1.356

ampl

B1L103S, U12-ch65, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

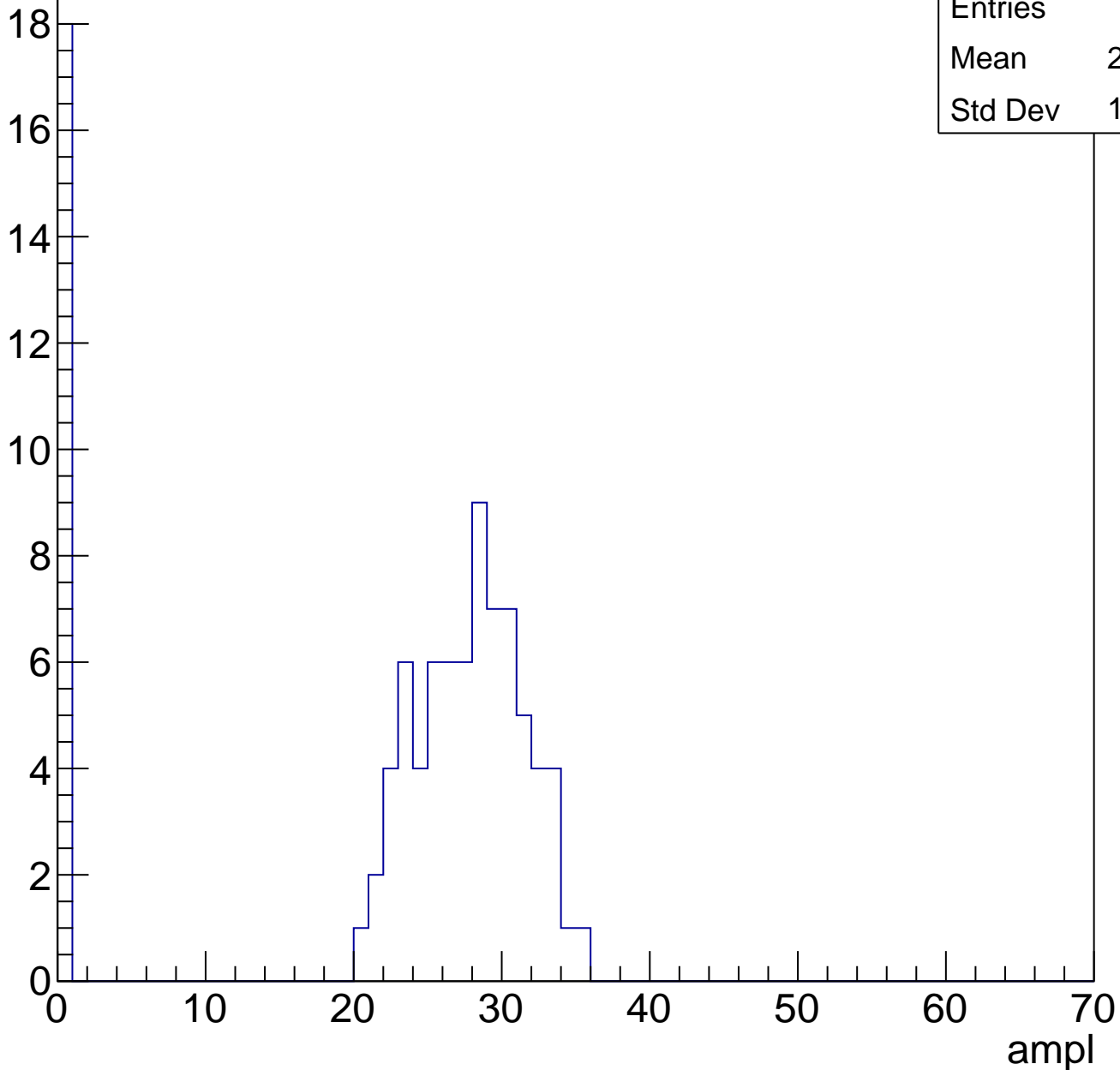
Entries	19
Mean	0
Std Dev	0

B1L103S, U12-ch66, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	91
Mean	21.99
Std Dev	11.37

Entry

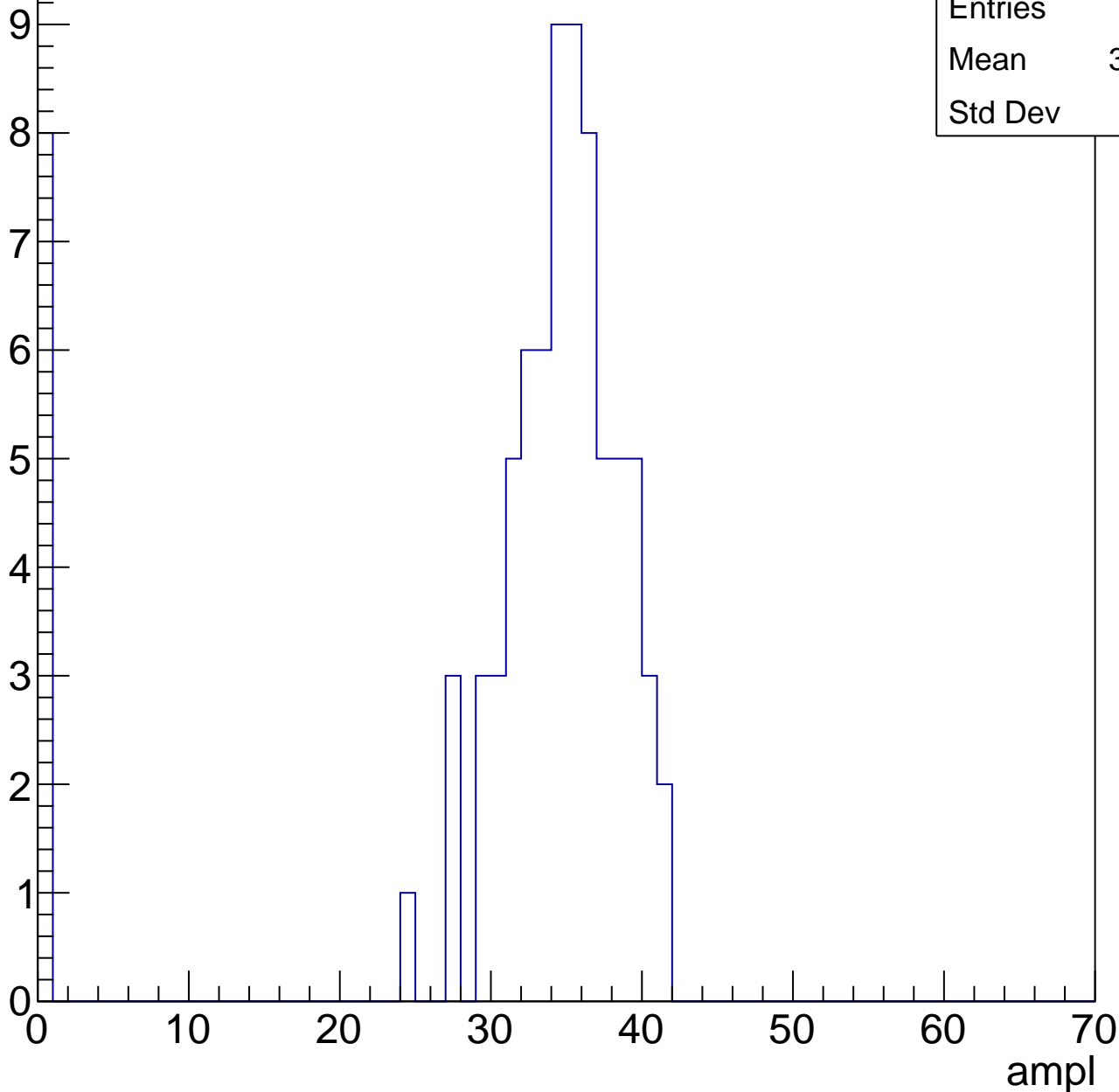


B1L103S, U12-ch66, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	81
Mean	30.96
Std Dev	10.8

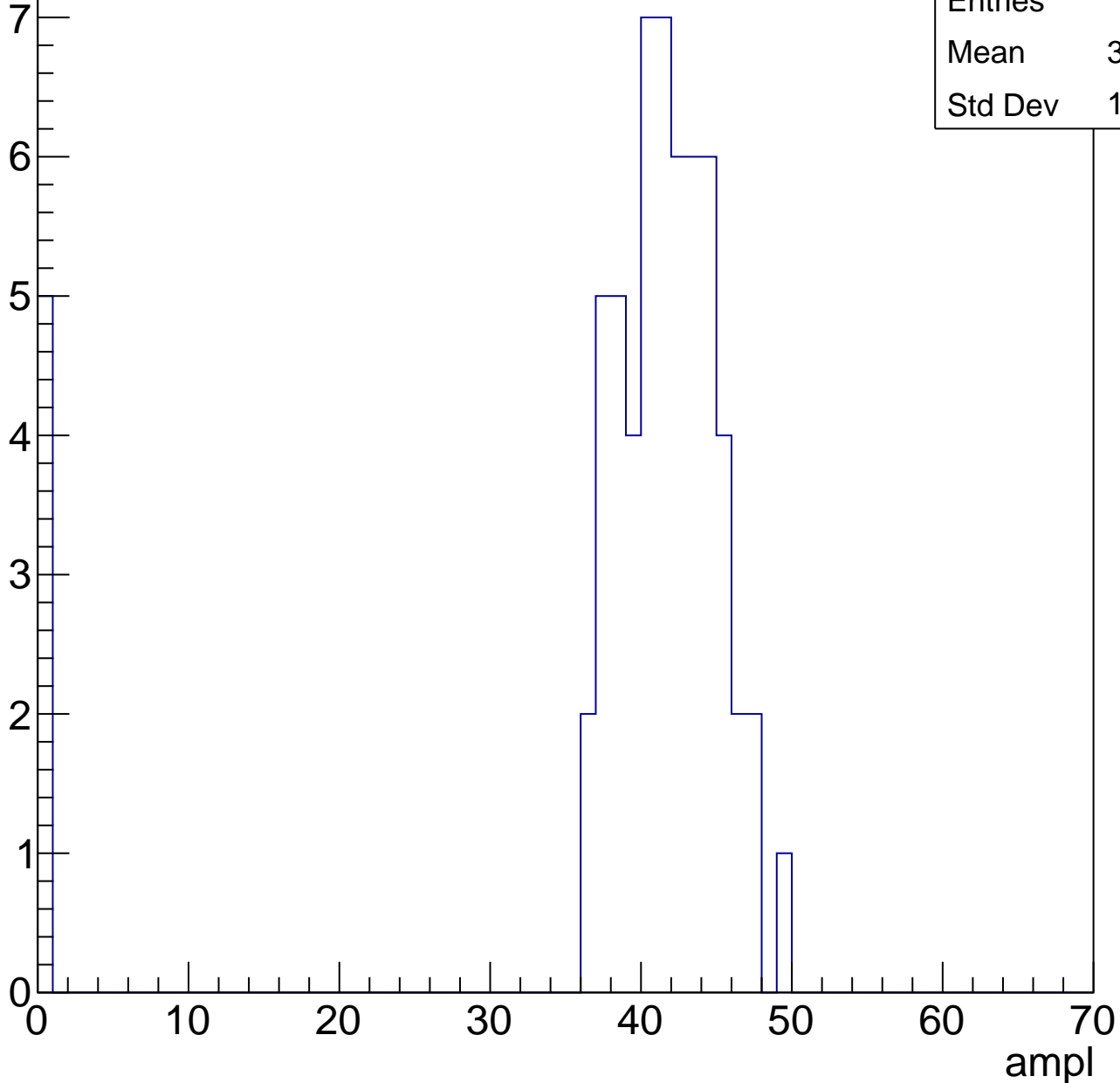


B1L103S, U12-ch66, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	38.05
Std Dev	11.64

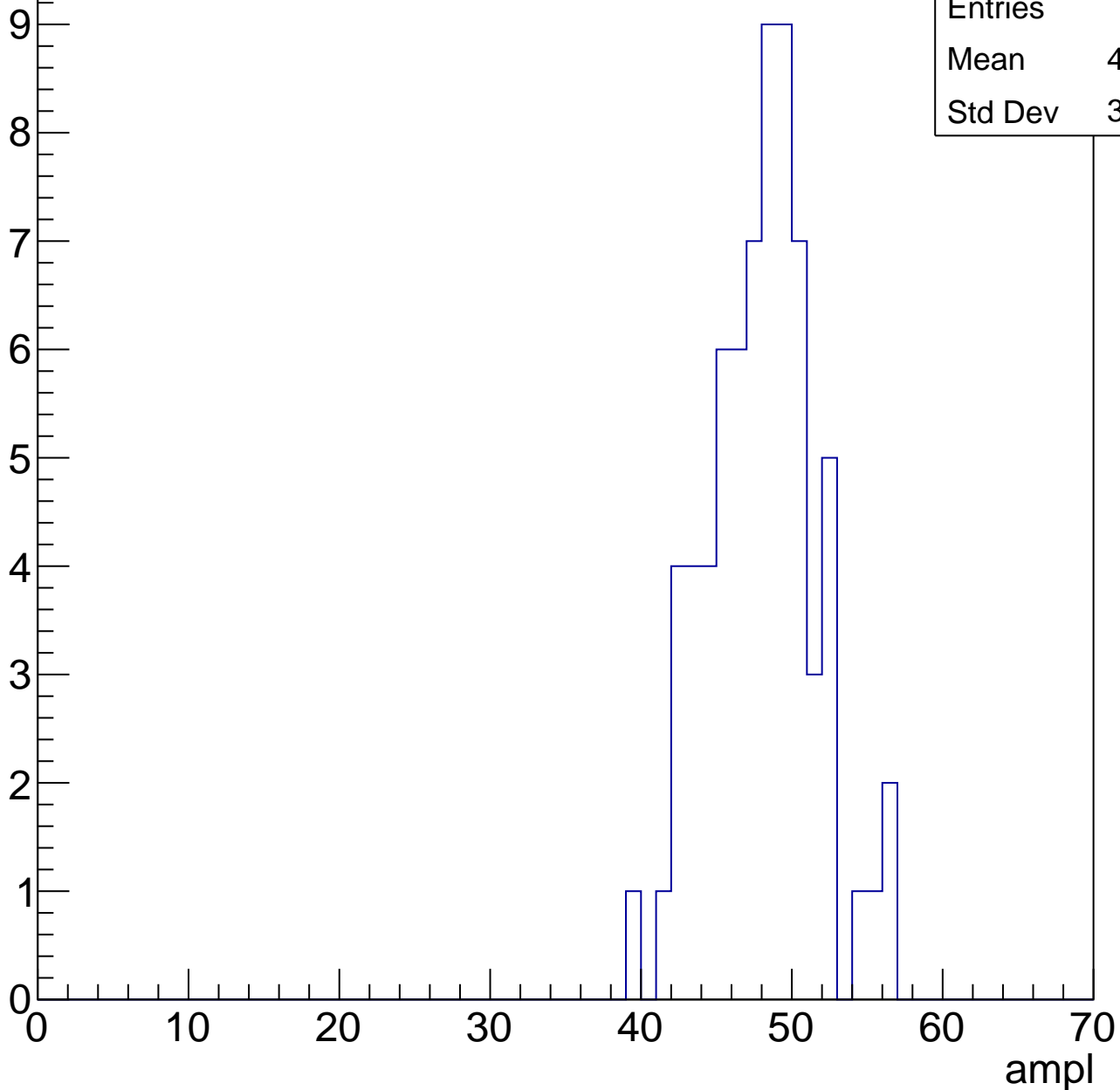


B1L103S, U12-ch66, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	47.54
Std Dev	3.516

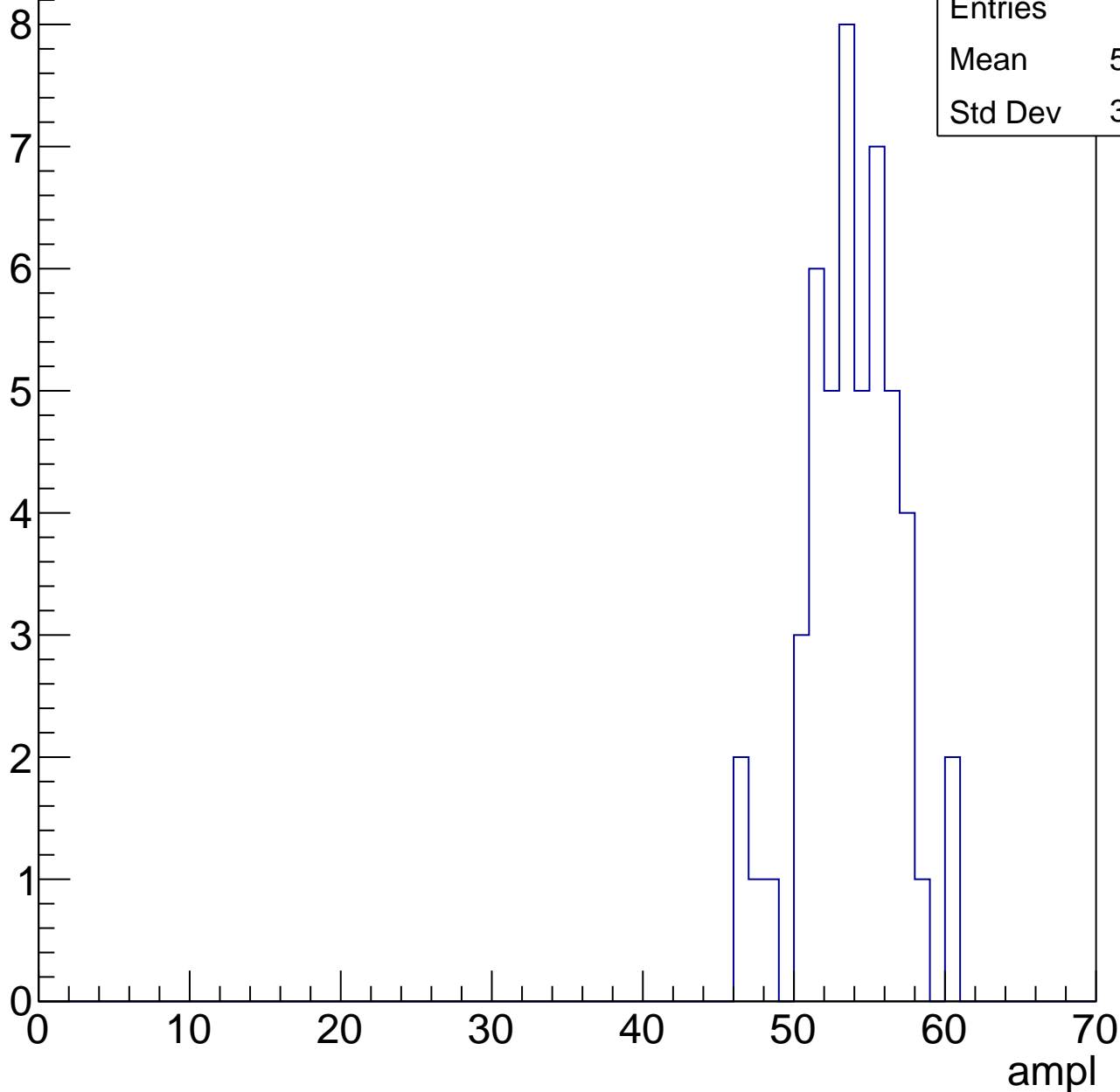


B1L103S, U12-ch66, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

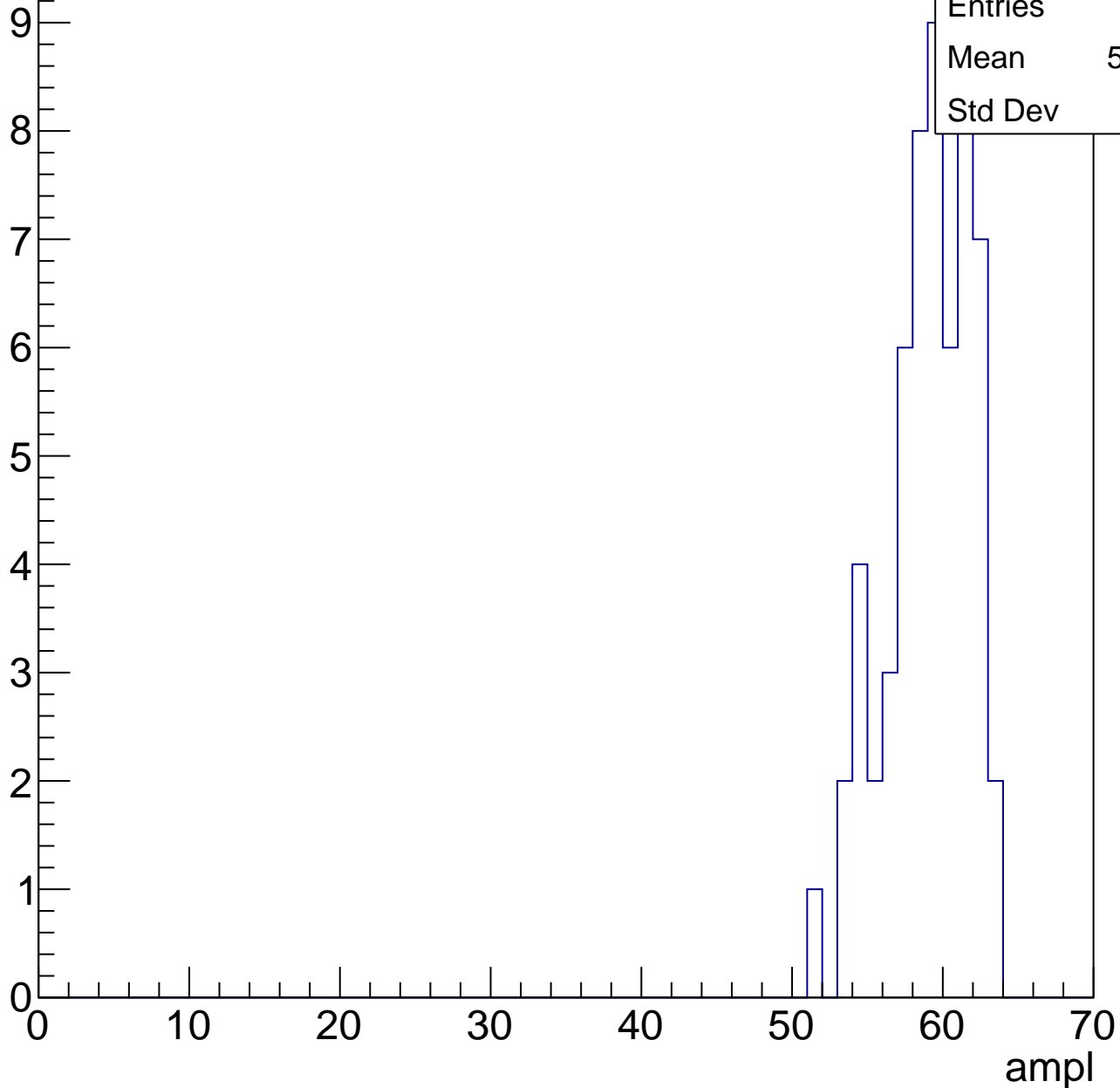
Entries	50
Mean	53.36
Std Dev	3.077



B1L103S, U12-ch66, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

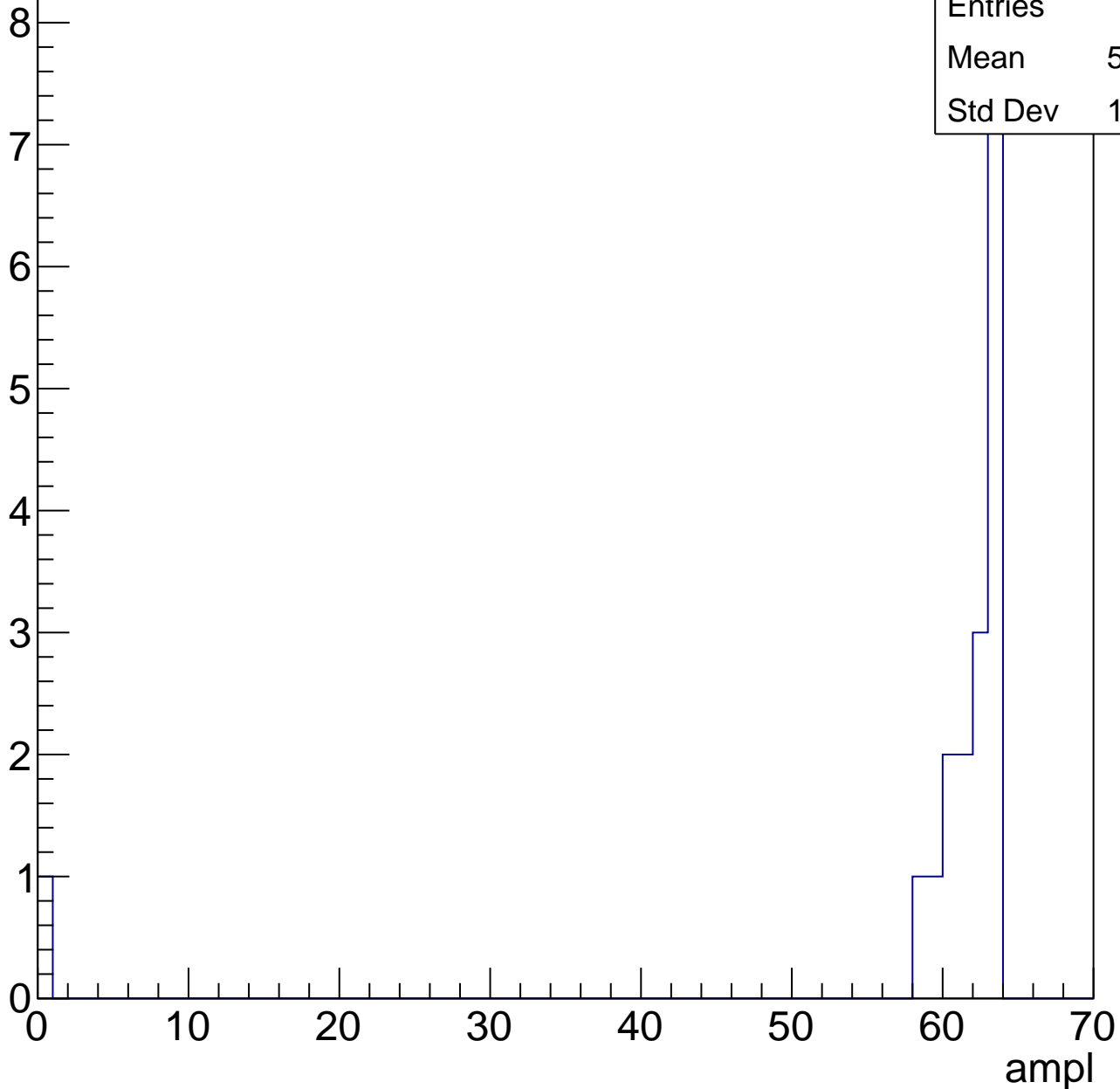


B1L103S, U12-ch66, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	18
Mean	58.28
Std Dev	14.22



B1L103S, U12-ch66, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U12-ch67, adc0

calib_packv5_041523_1651.root, FC#0, port C2

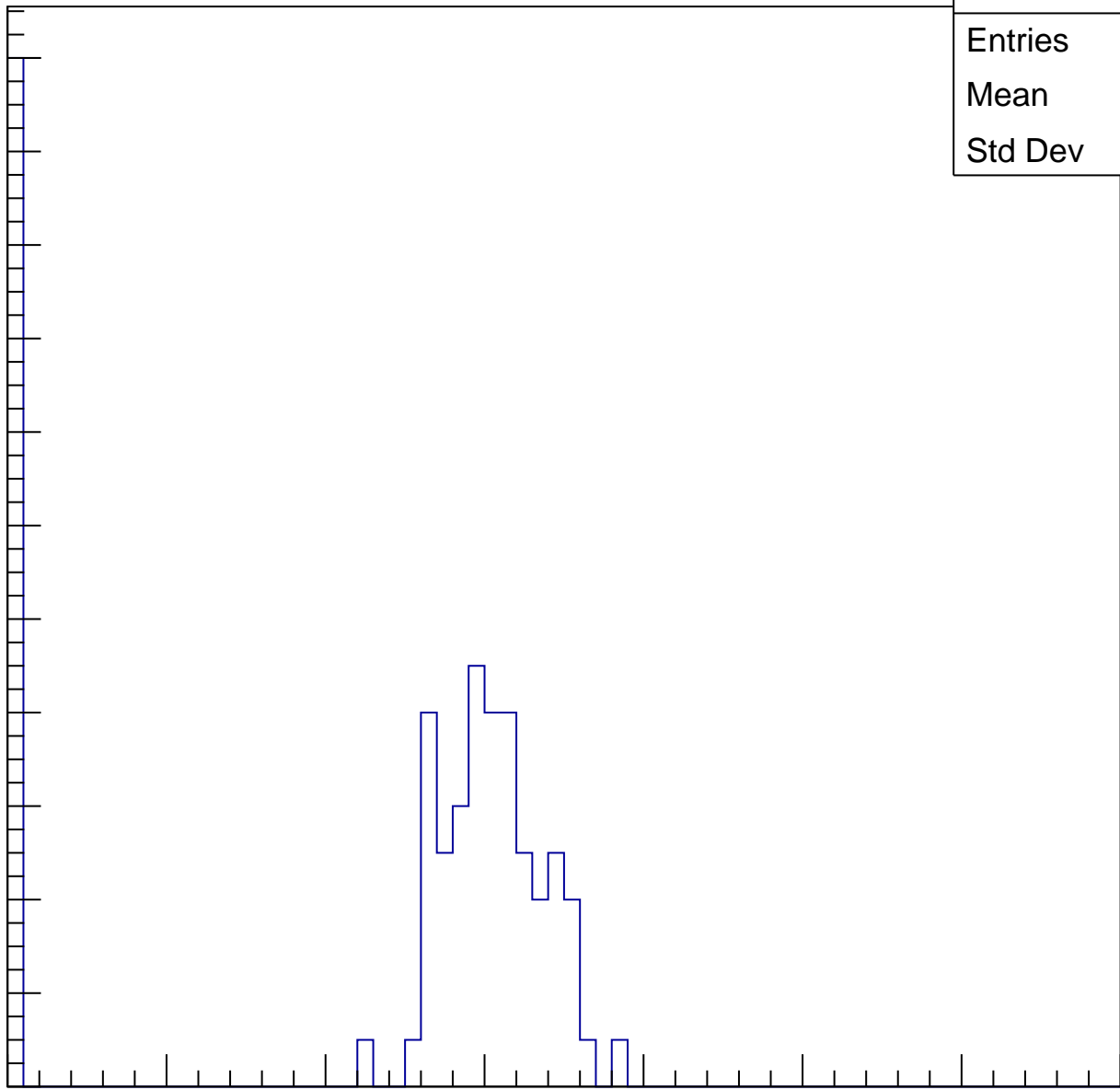
Entries	88
Mean	22.53
Std Dev	13.29

Entry

22
20
18
16
14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70

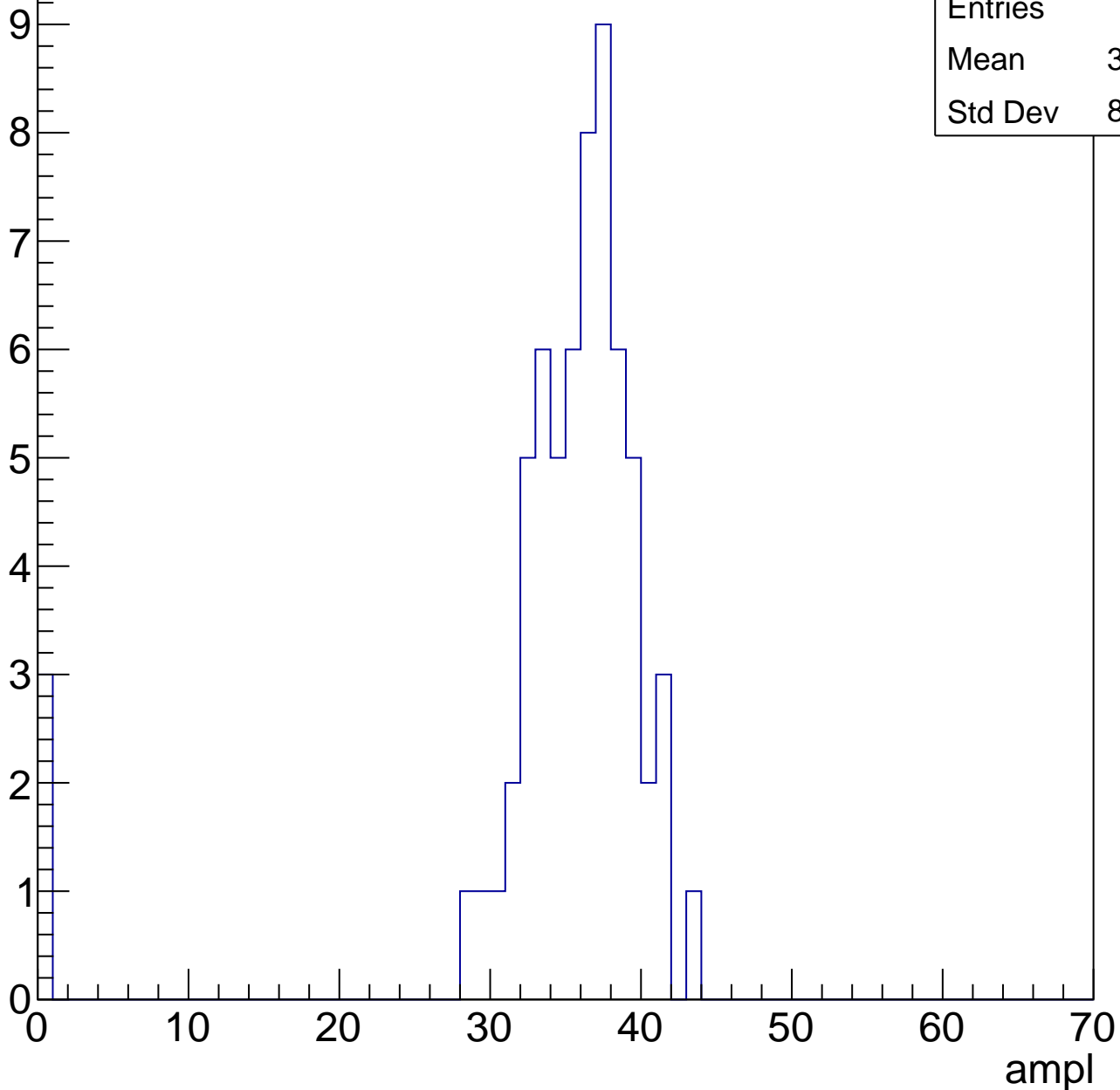


B1L103S, U12-ch67, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	34.02
Std Dev	8.129

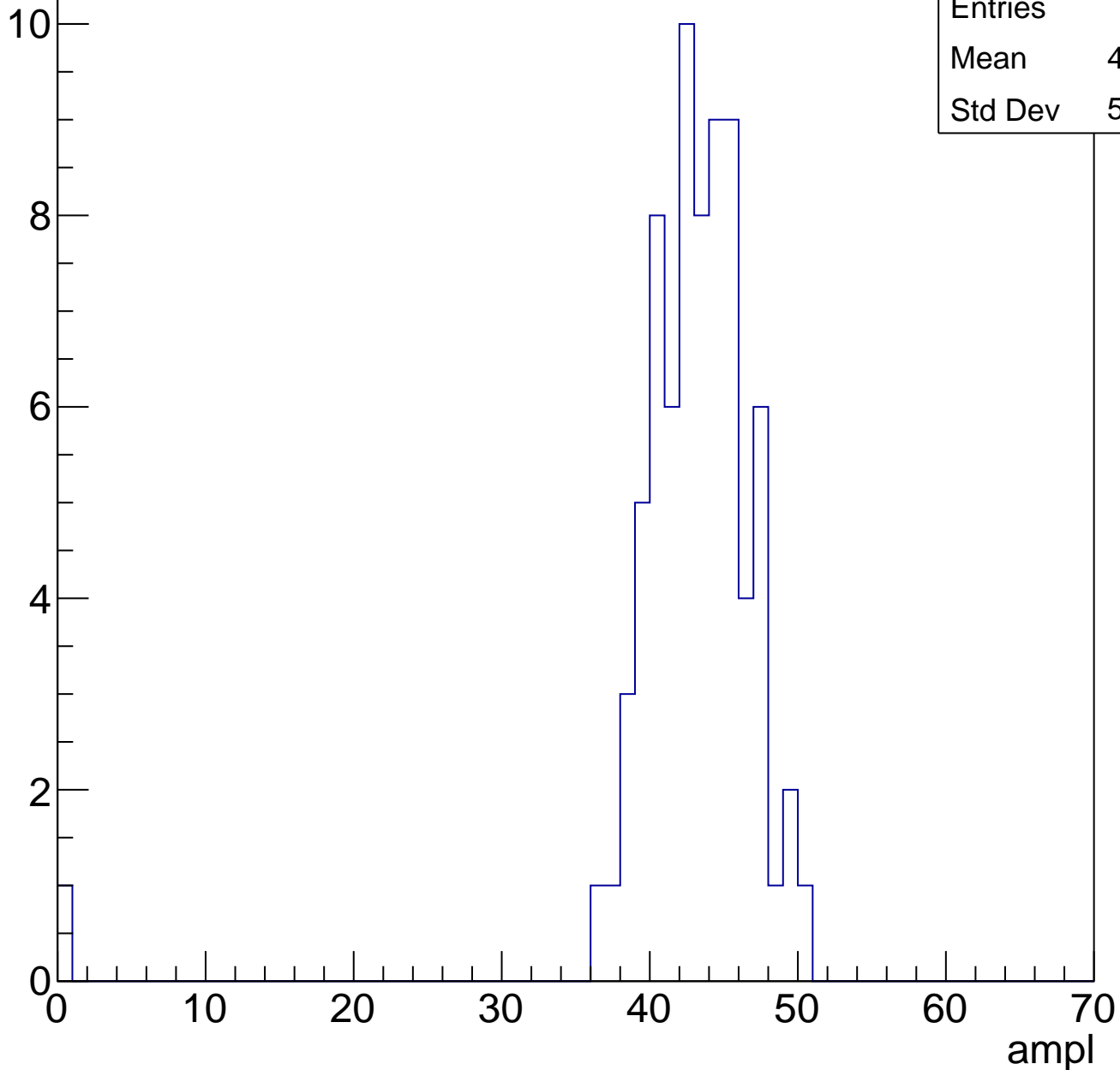


B1L103S, U12-ch67, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	75
Mean	42.33
Std Dev	5.756

Entry

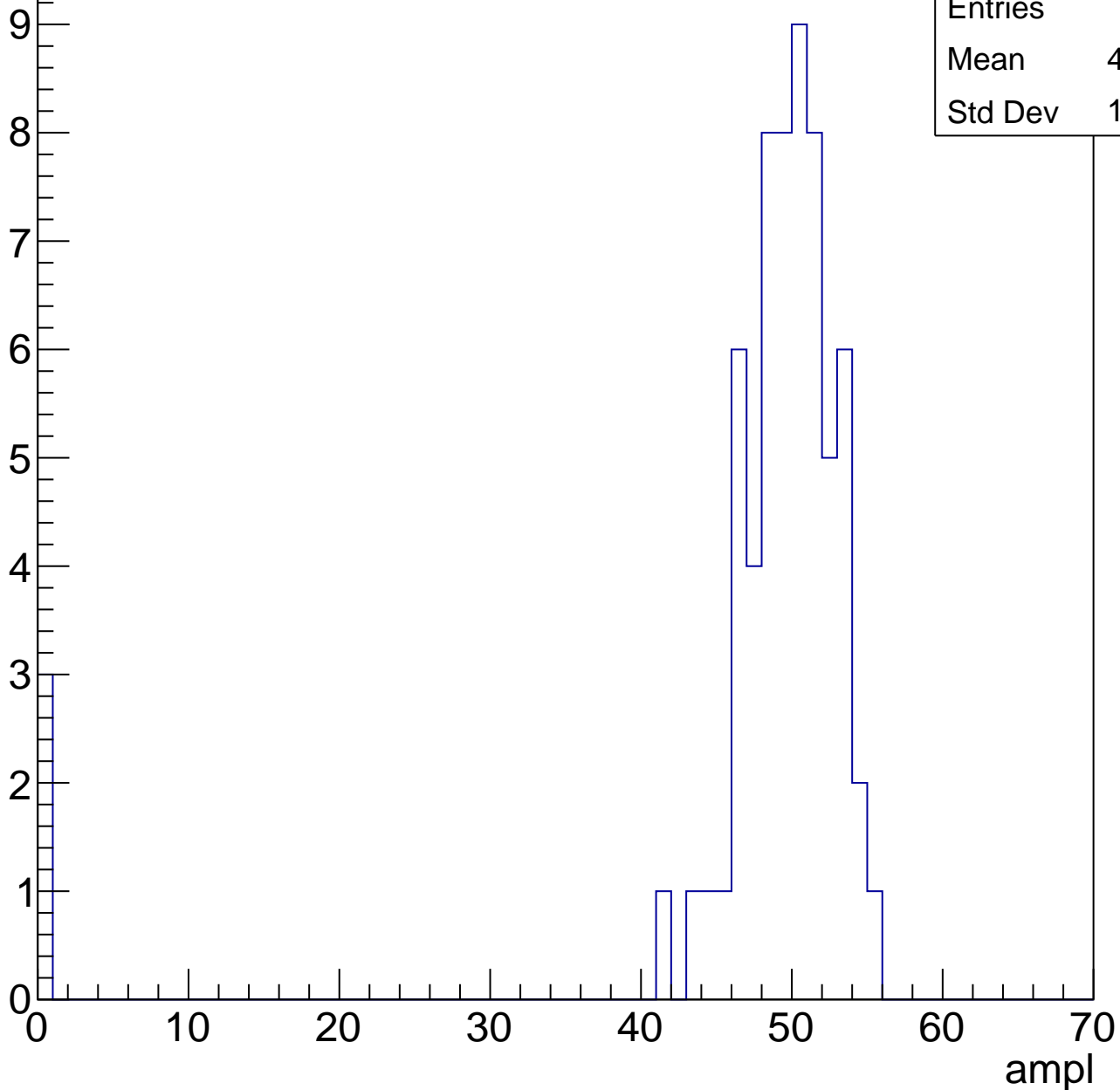


B1L103S, U12-ch67, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	47.06
Std Dev	10.79

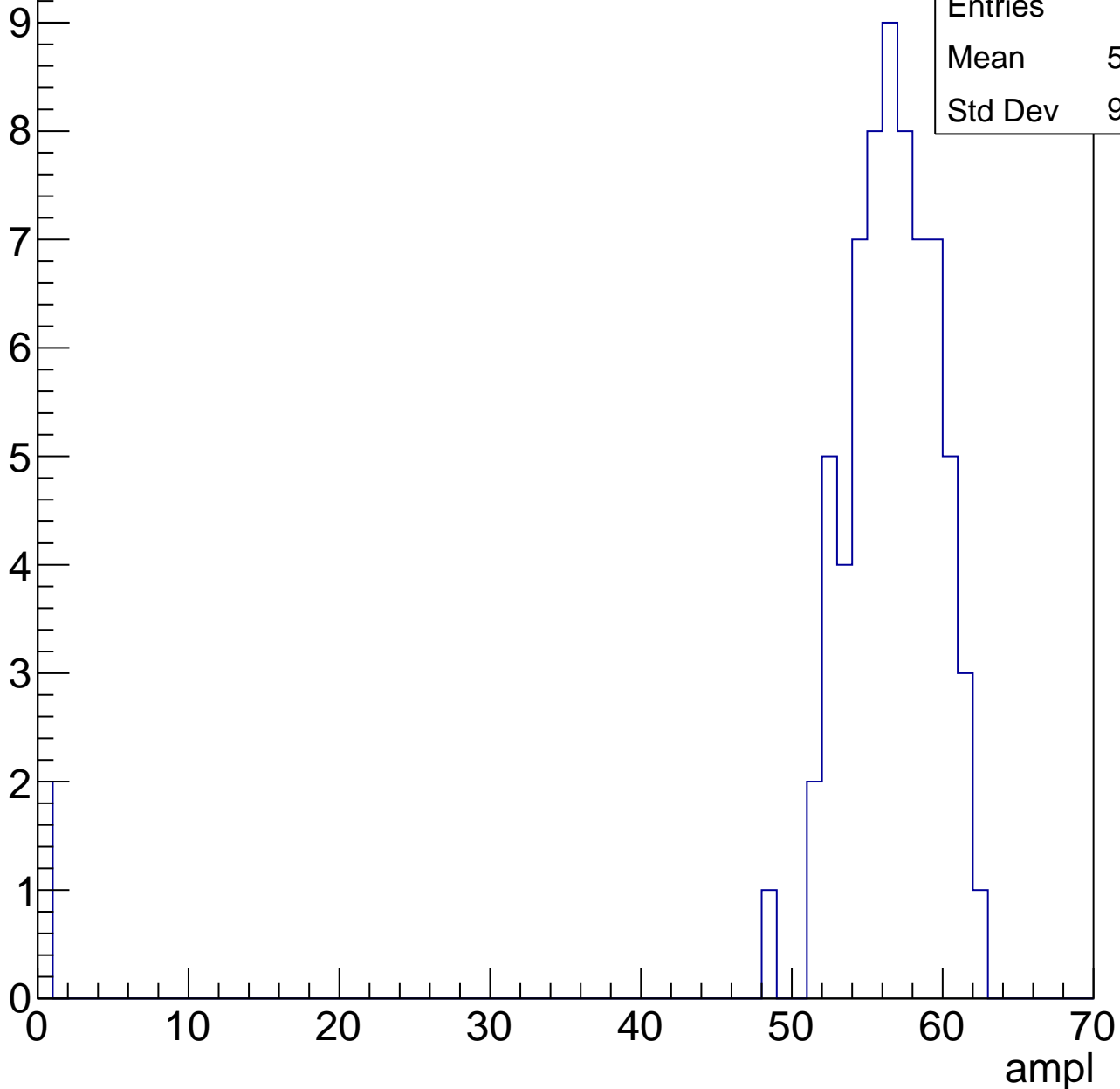


B1L103S, U12-ch67, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	54.55
Std Dev	9.842

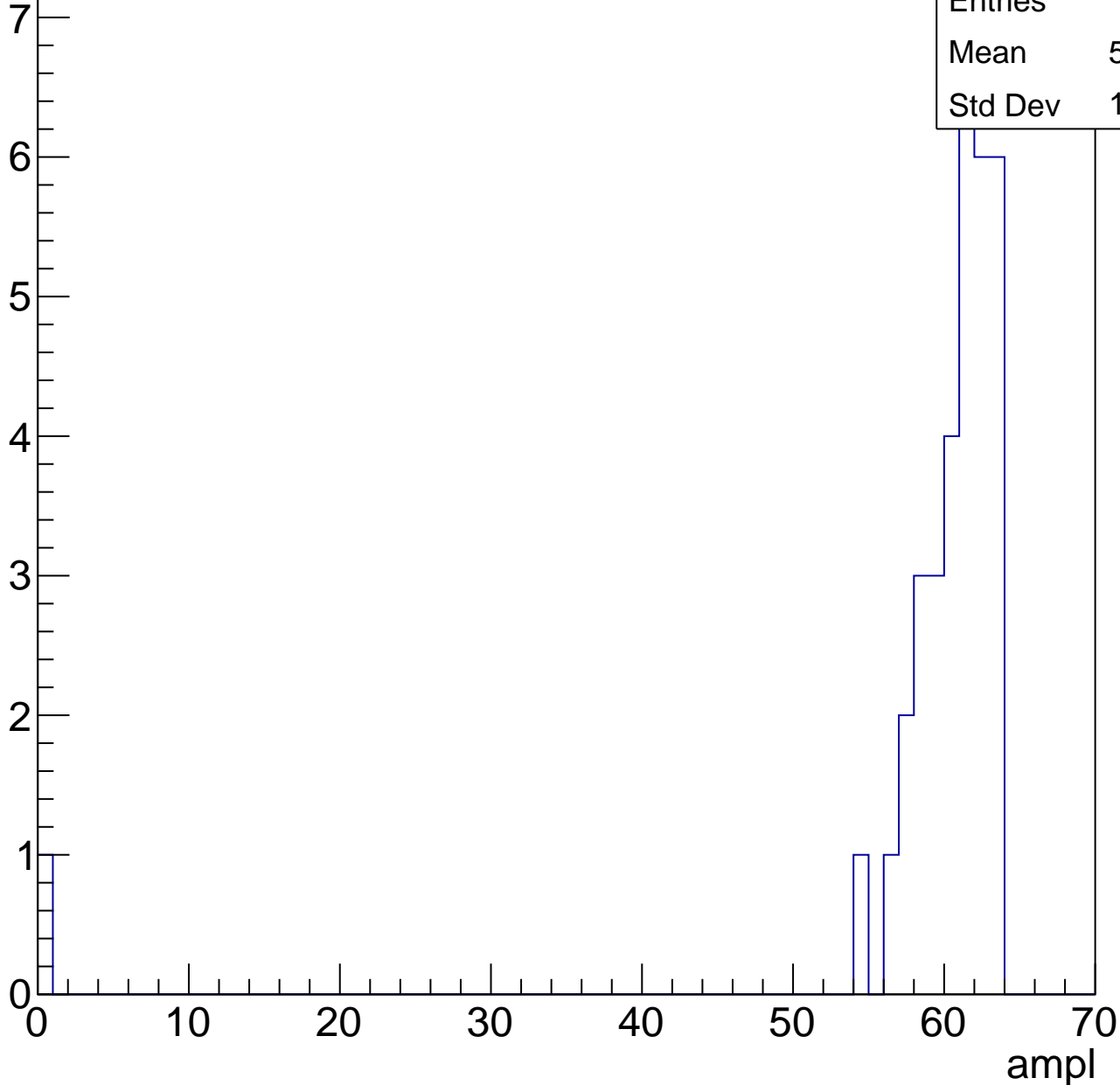


B1L103S, U12-ch67, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

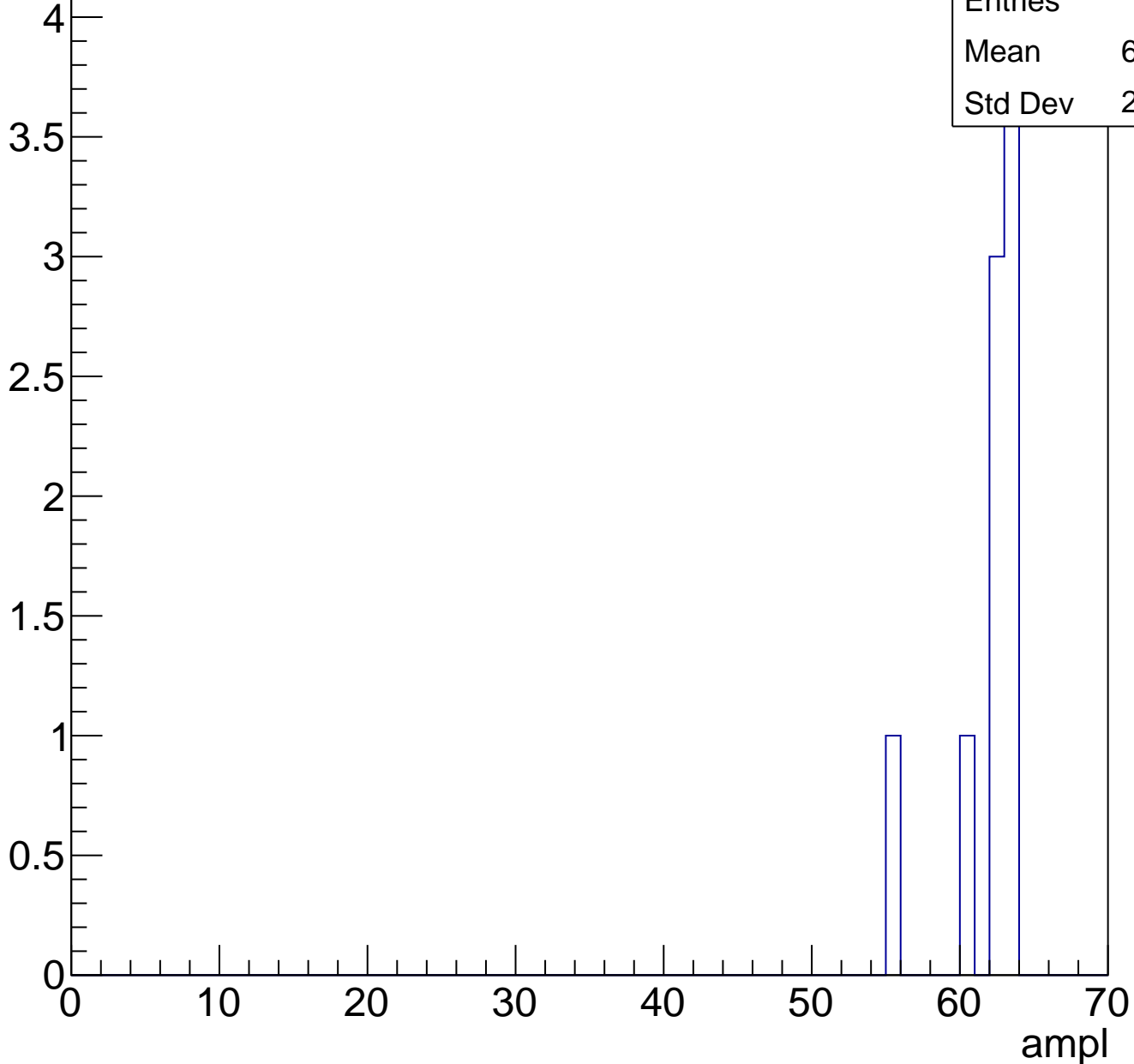
Entries	34
Mean	58.59
Std Dev	10.44



B1L103S, U12-ch67, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch67, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



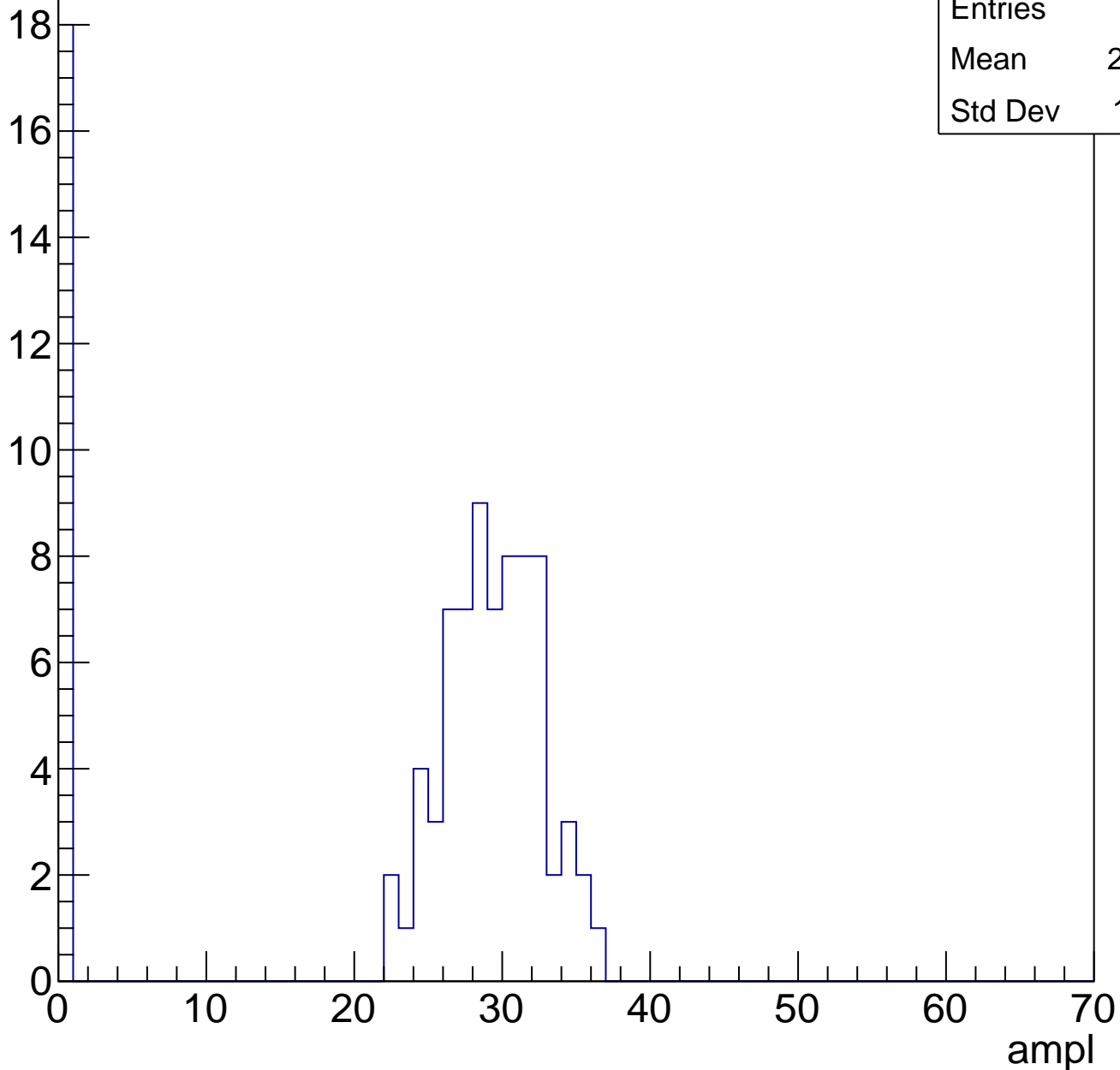
Entries	18
Mean	0
Std Dev	0

B1L103S, U12-ch68, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	90
Mean	23.13
Std Dev	11.91

Entry

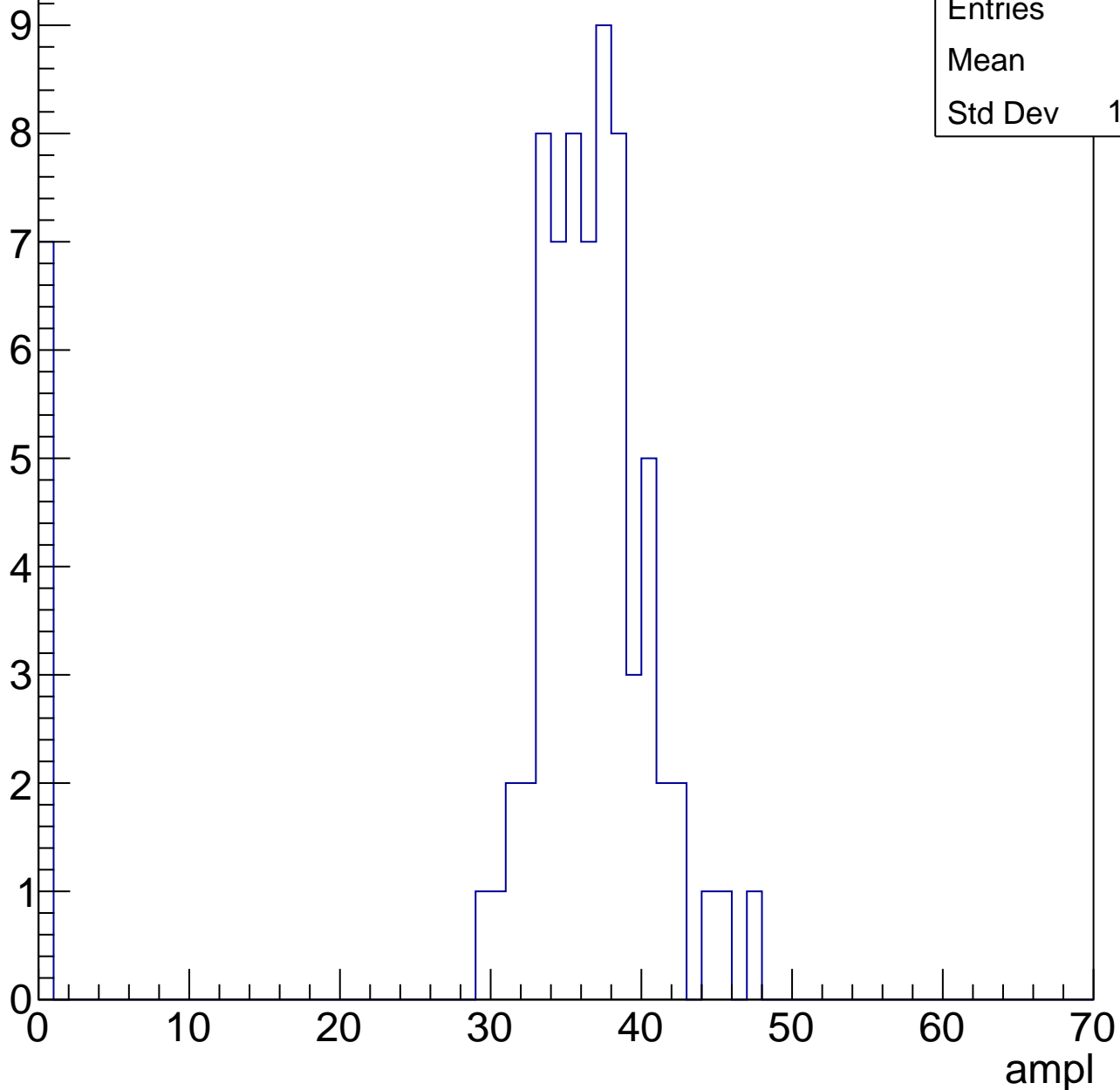


B1L103S, U12-ch68, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	75
Mean	33
Std Dev	11.08

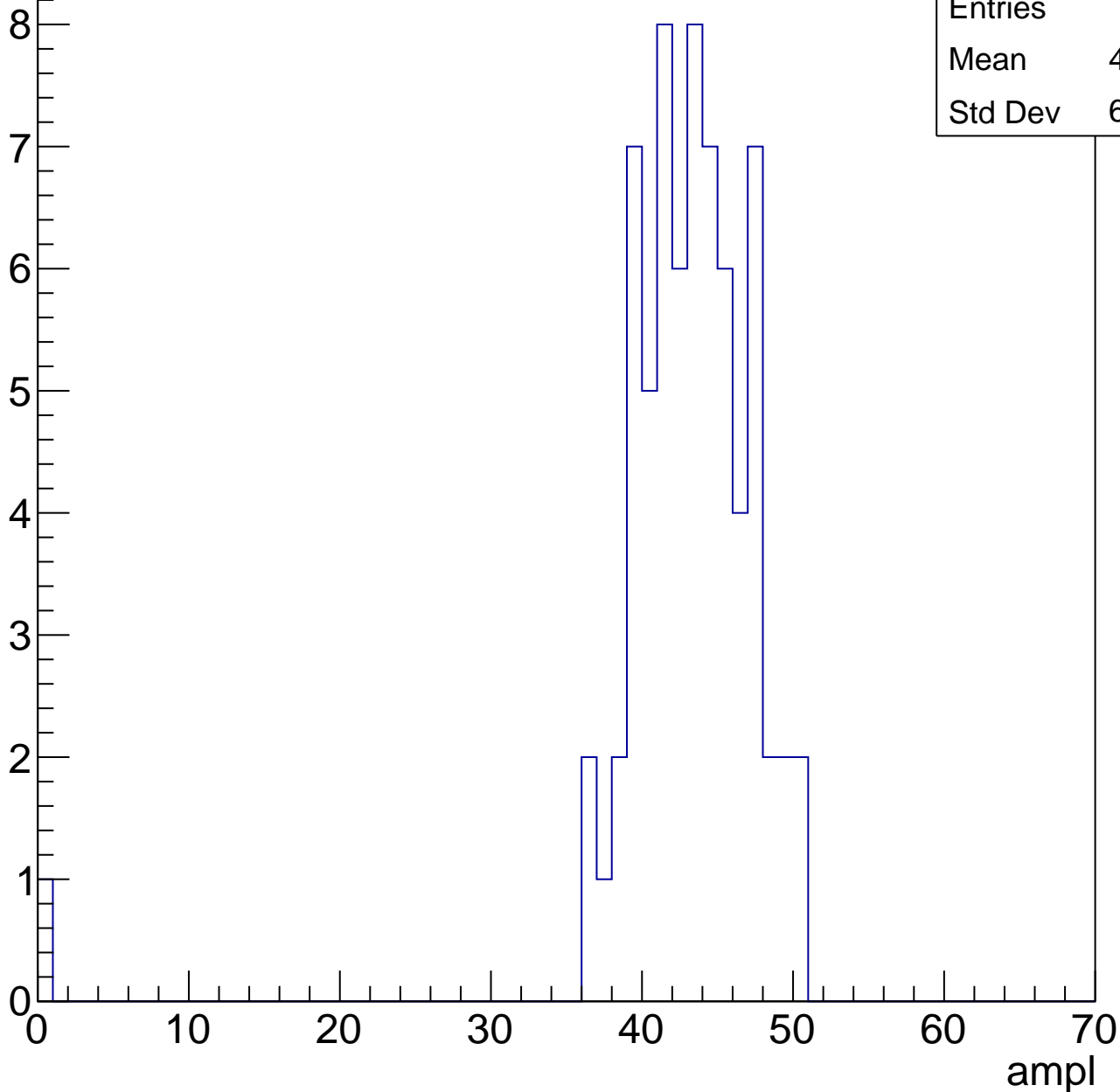


B1L103S, U12-ch68, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	42.39
Std Dev	6.095

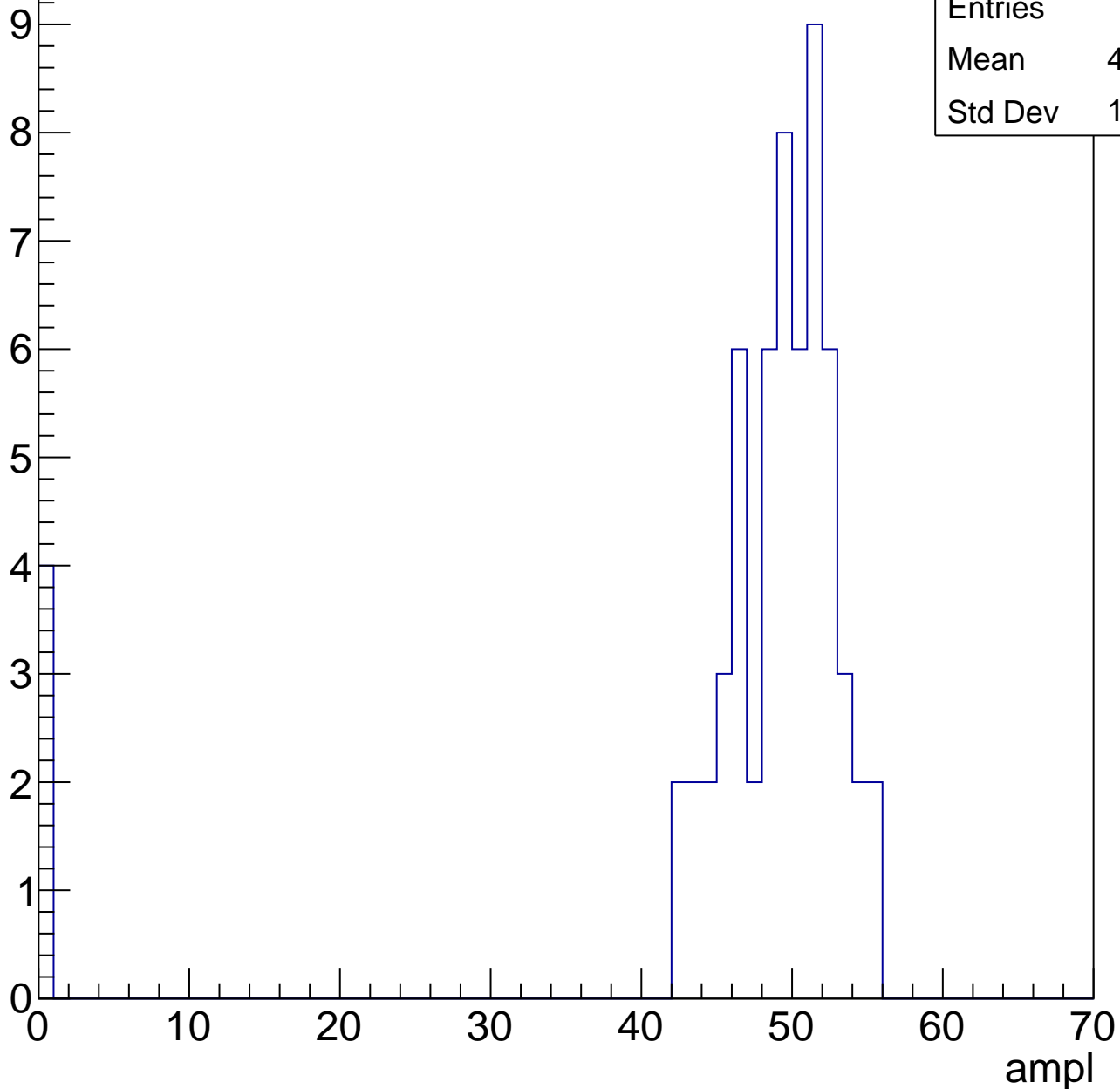


B1L103S, U12-ch68, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	63
Mean	45.89
Std Dev	12.34

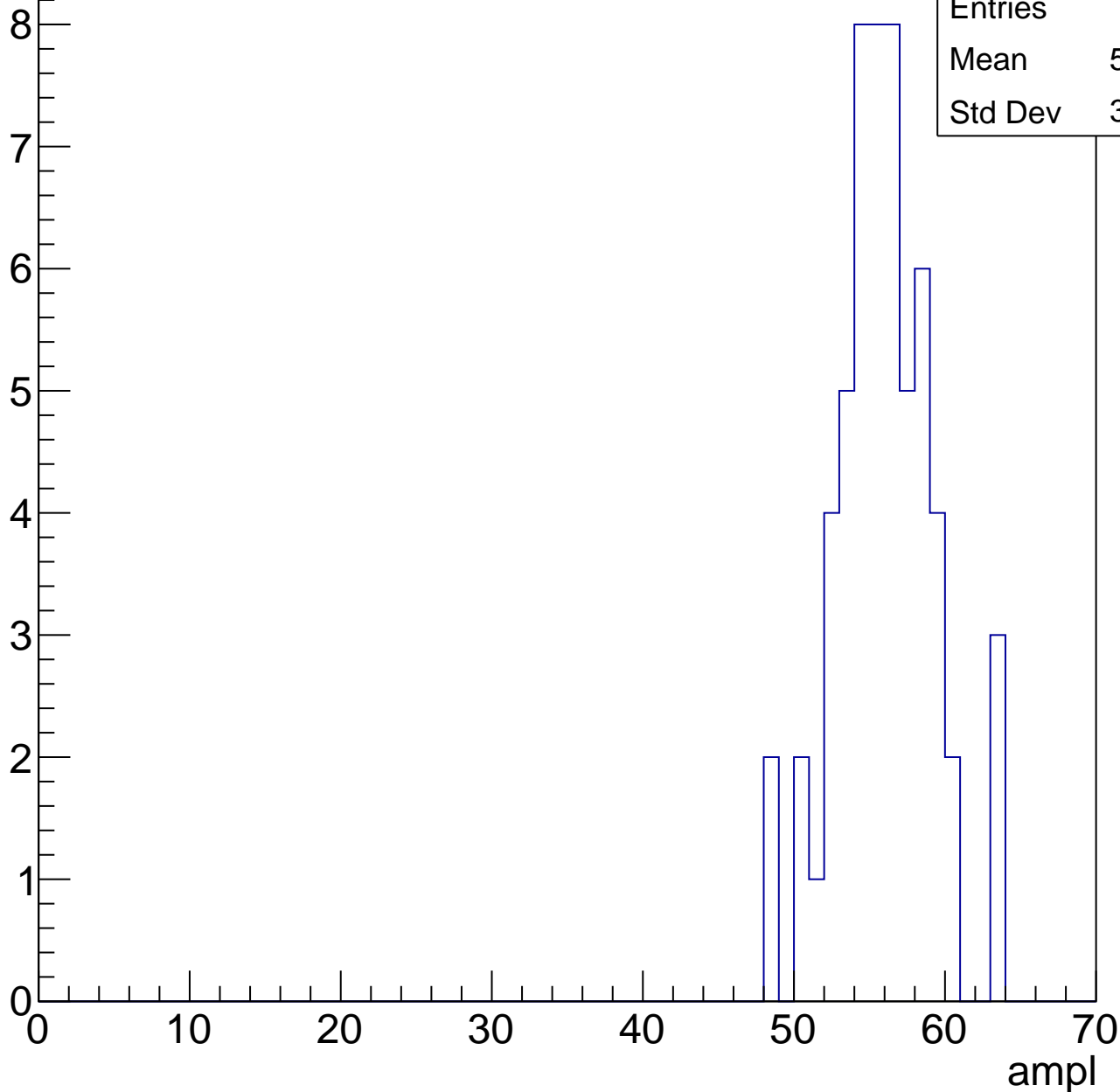


B1L103S, U12-ch68, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	55.48
Std Dev	3.223

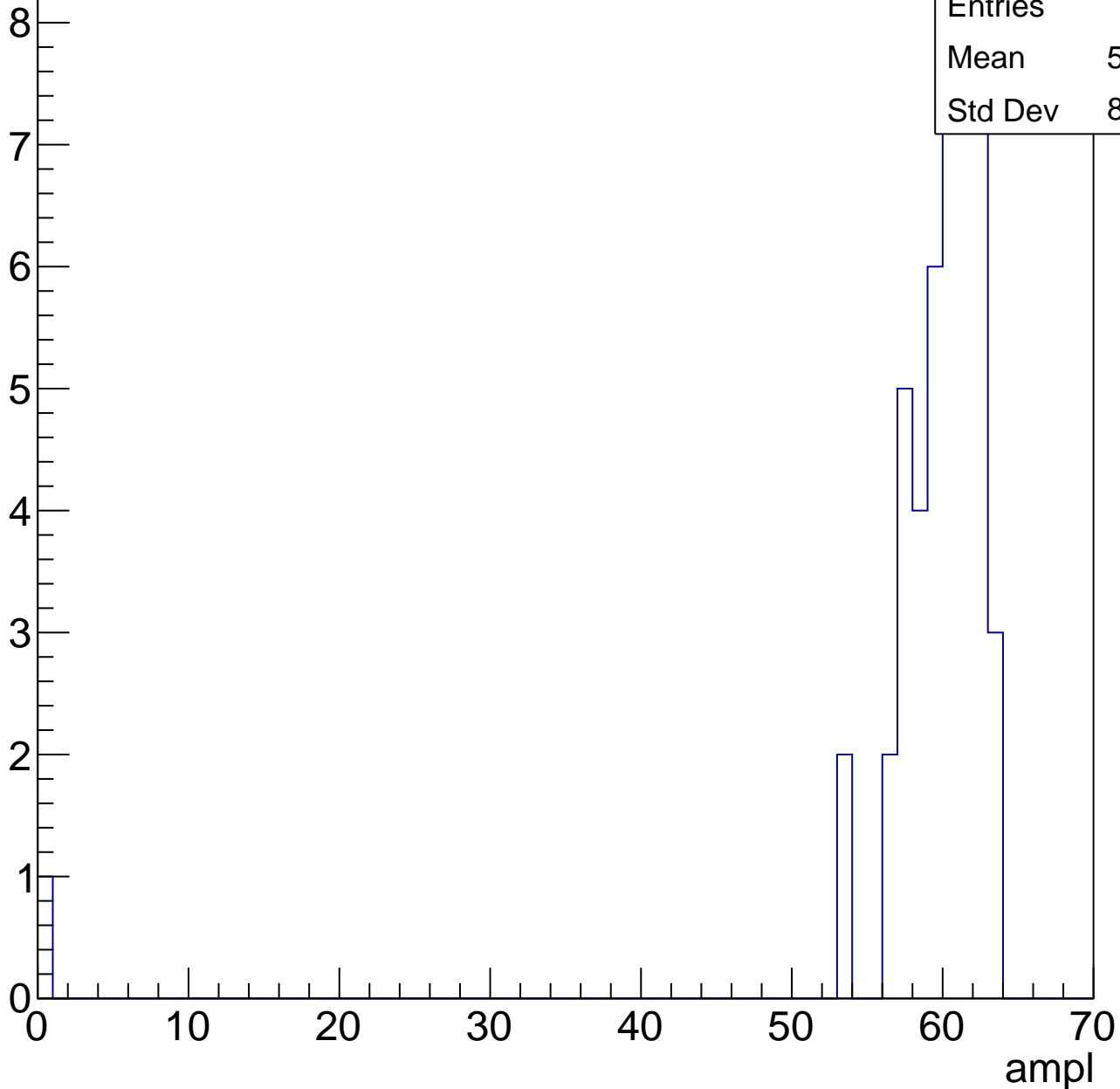


B1L103S, U12-ch68, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	47
Mean	58.34
Std Dev	8.914



B1L103S, U12-ch68, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

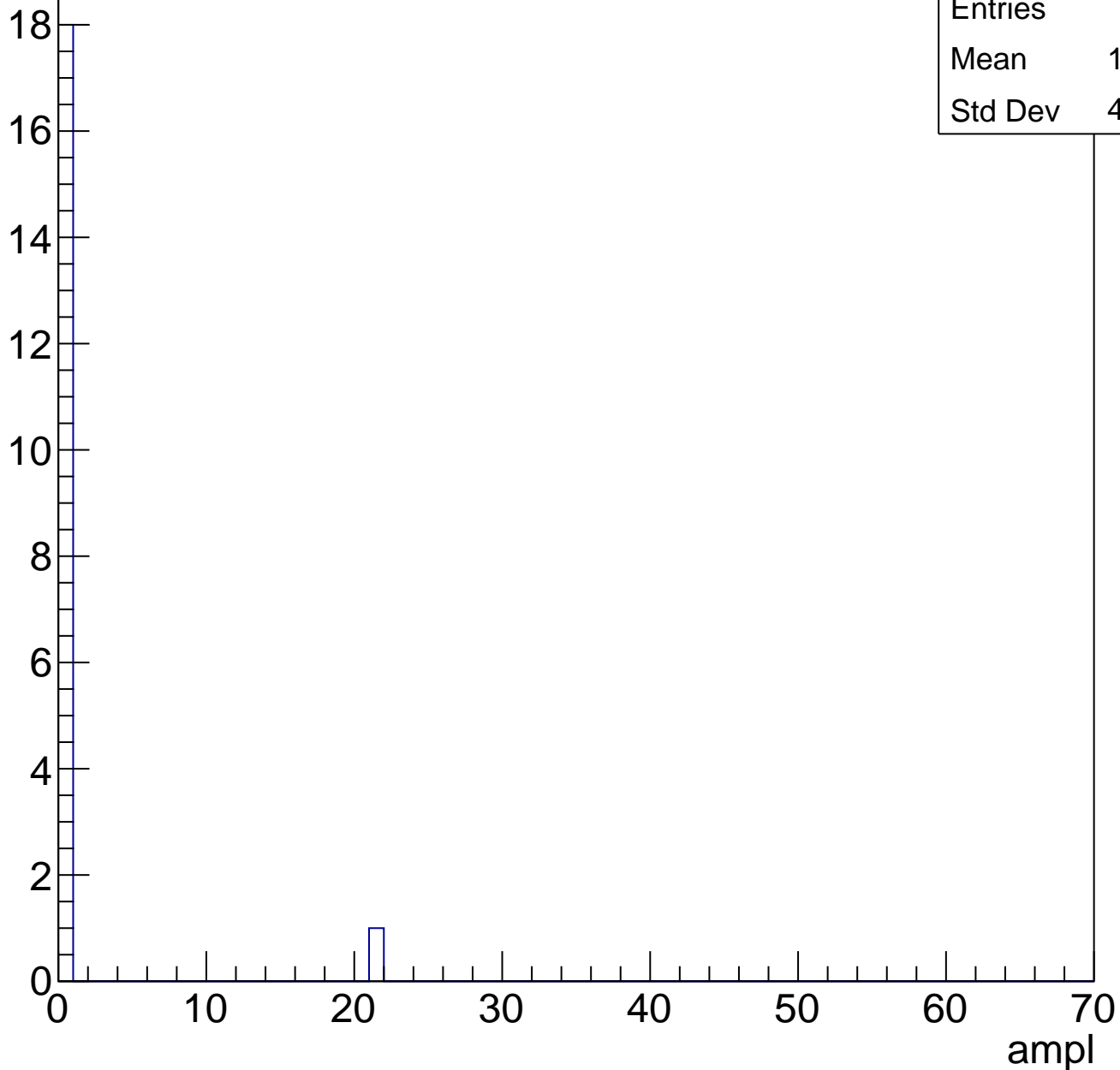


B1L103S, U12-ch68, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.105
Std Dev	4.689

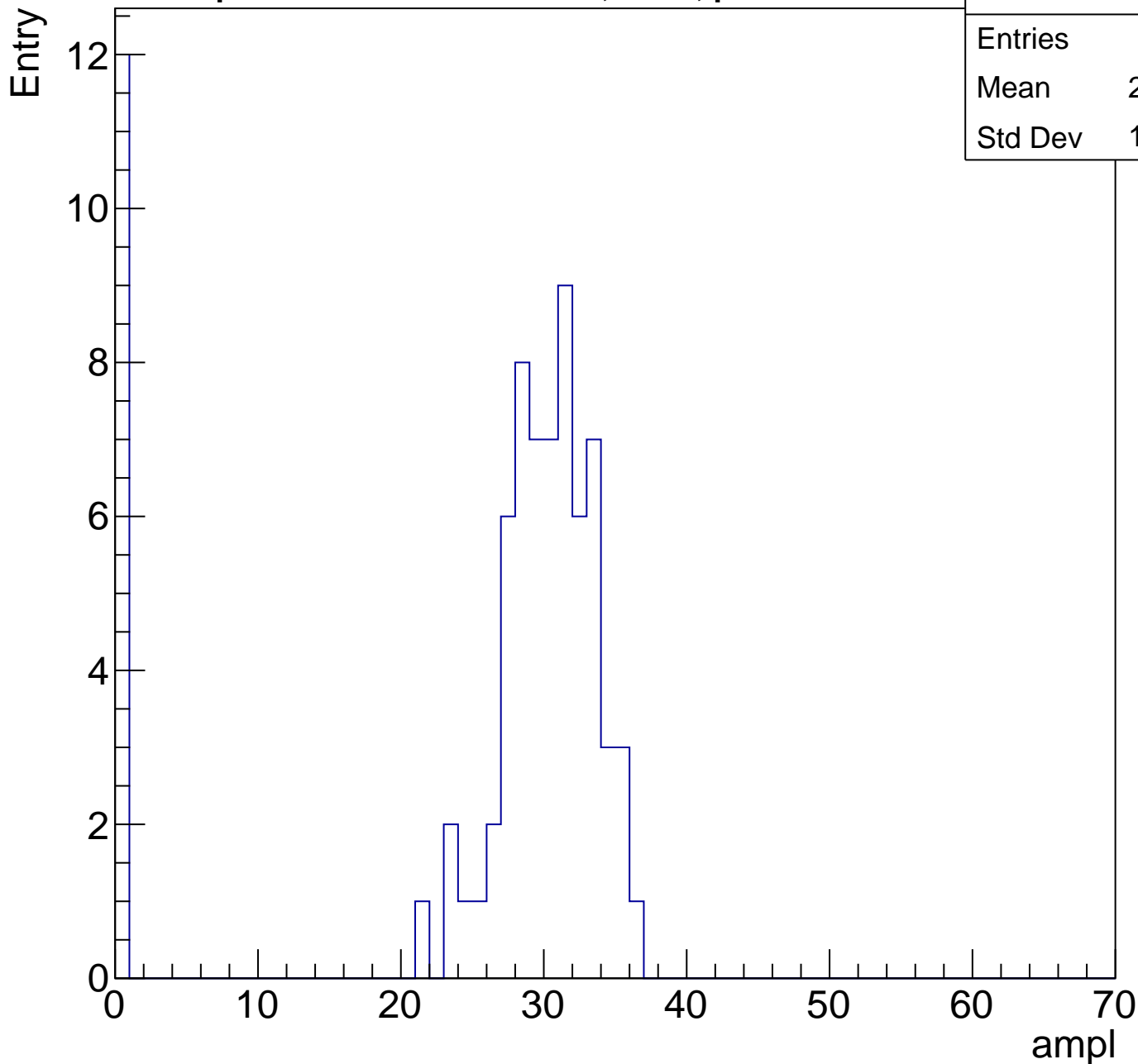
Entry



B1L103S, U12-ch69, adc0

calib_packv5_041523_1651.root, FC#0, port C2

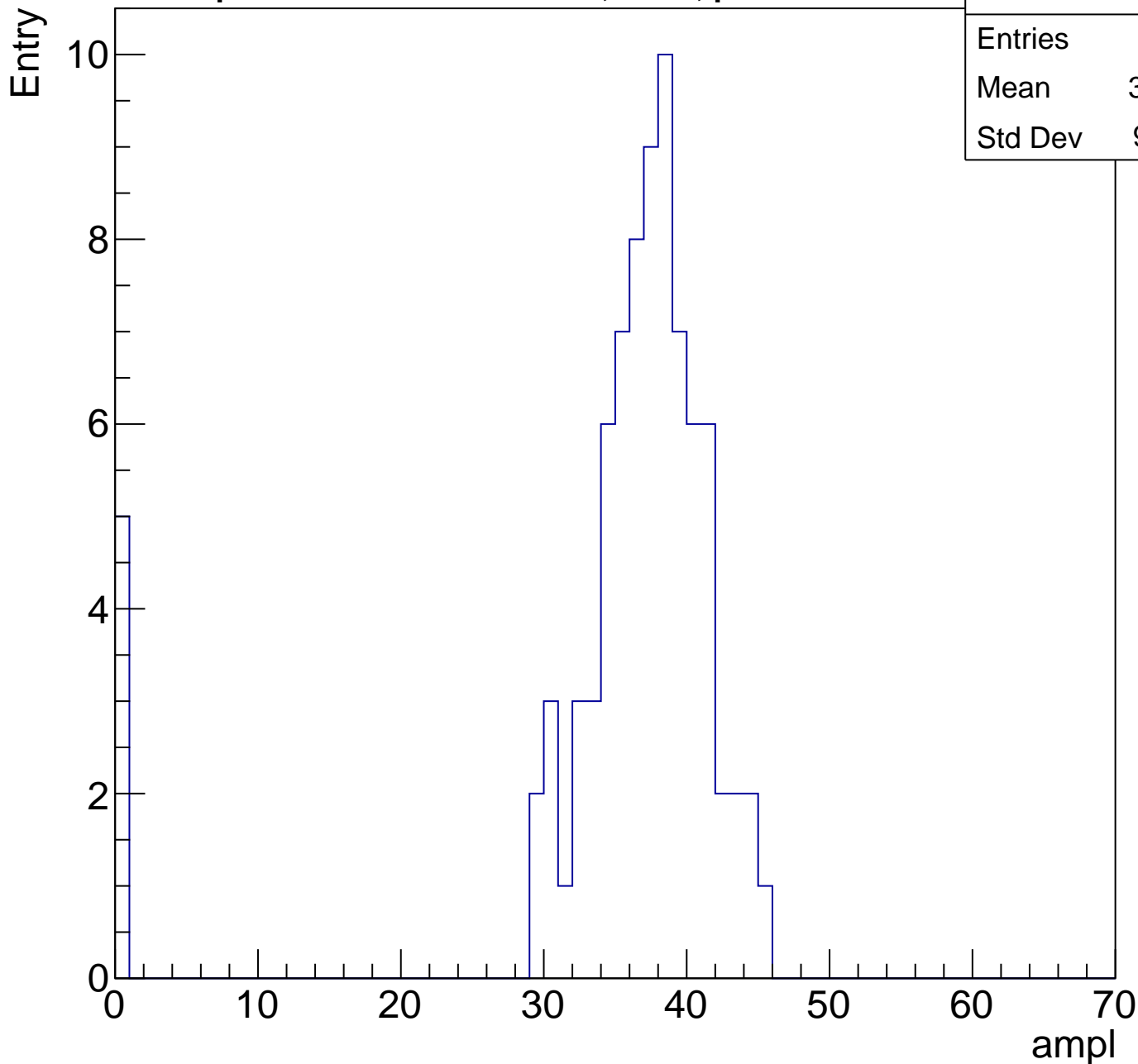
Entries	76
Mean	25.16
Std Dev	11.26



B1L103S, U12-ch69, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	83
Mean	34.77
Std Dev	9.461

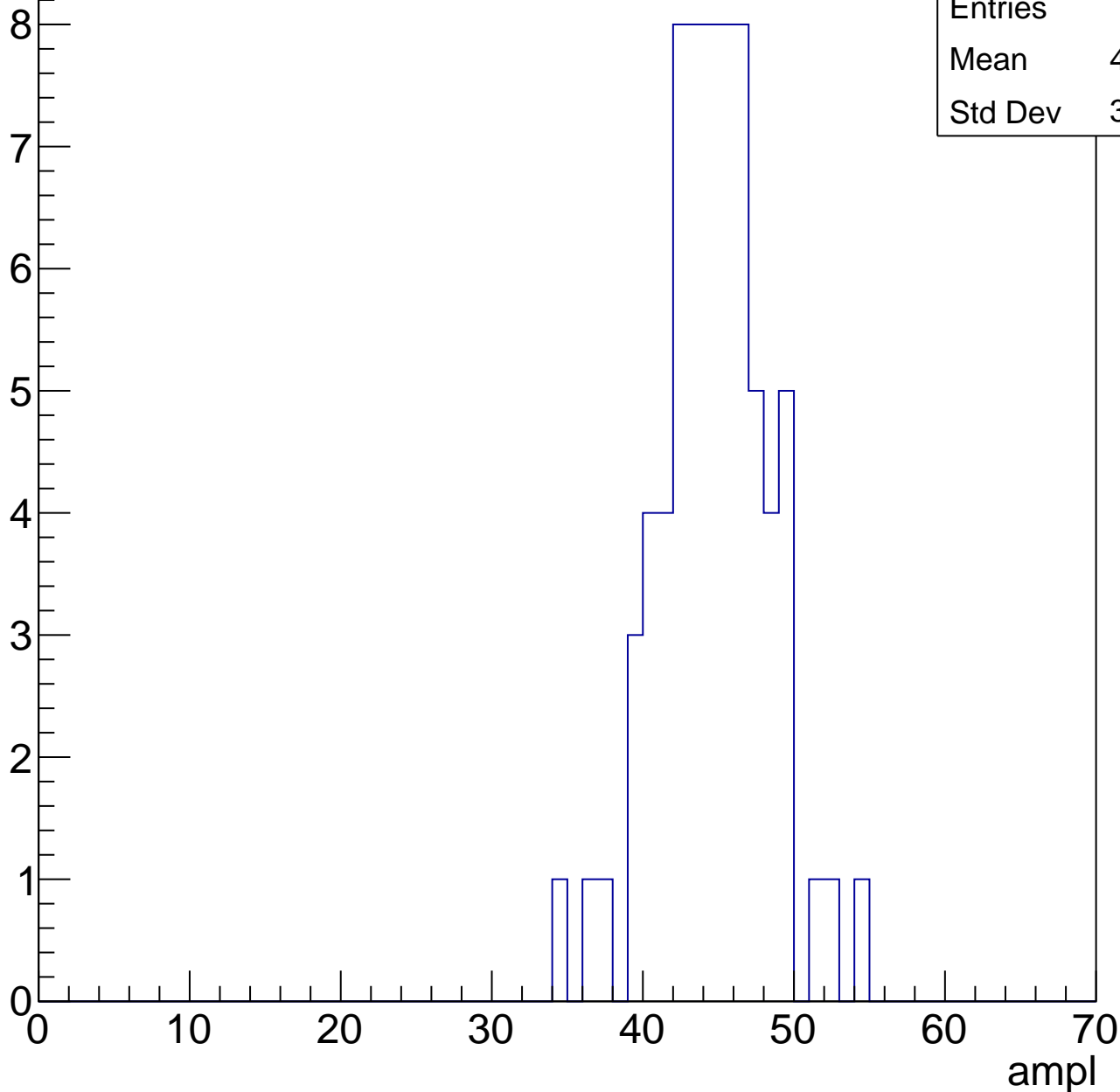


B1L103S, U12-ch69, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	44.18
Std Dev	3.585

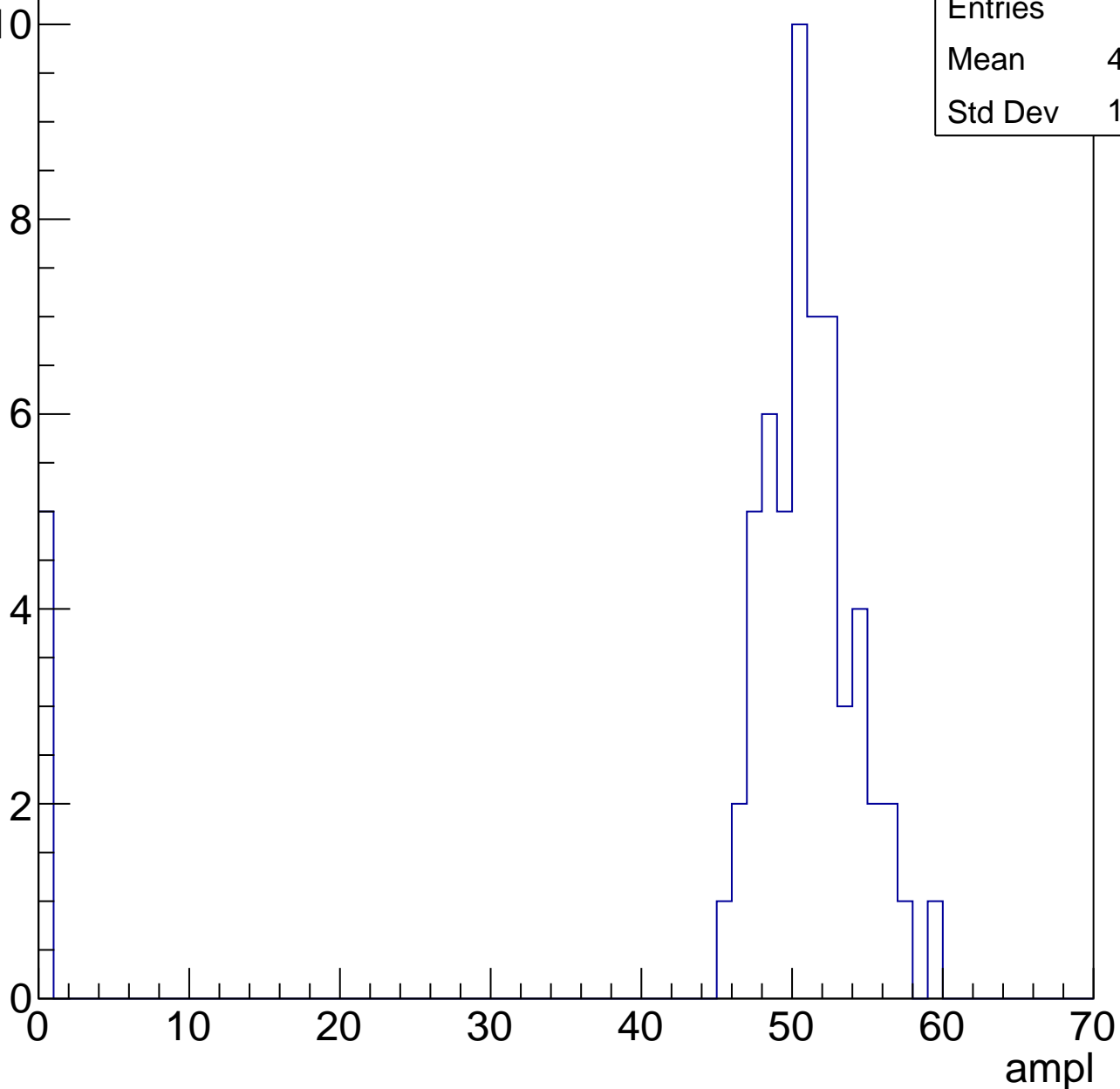


B1L103S, U12-ch69, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	46.54
Std Dev	14.19

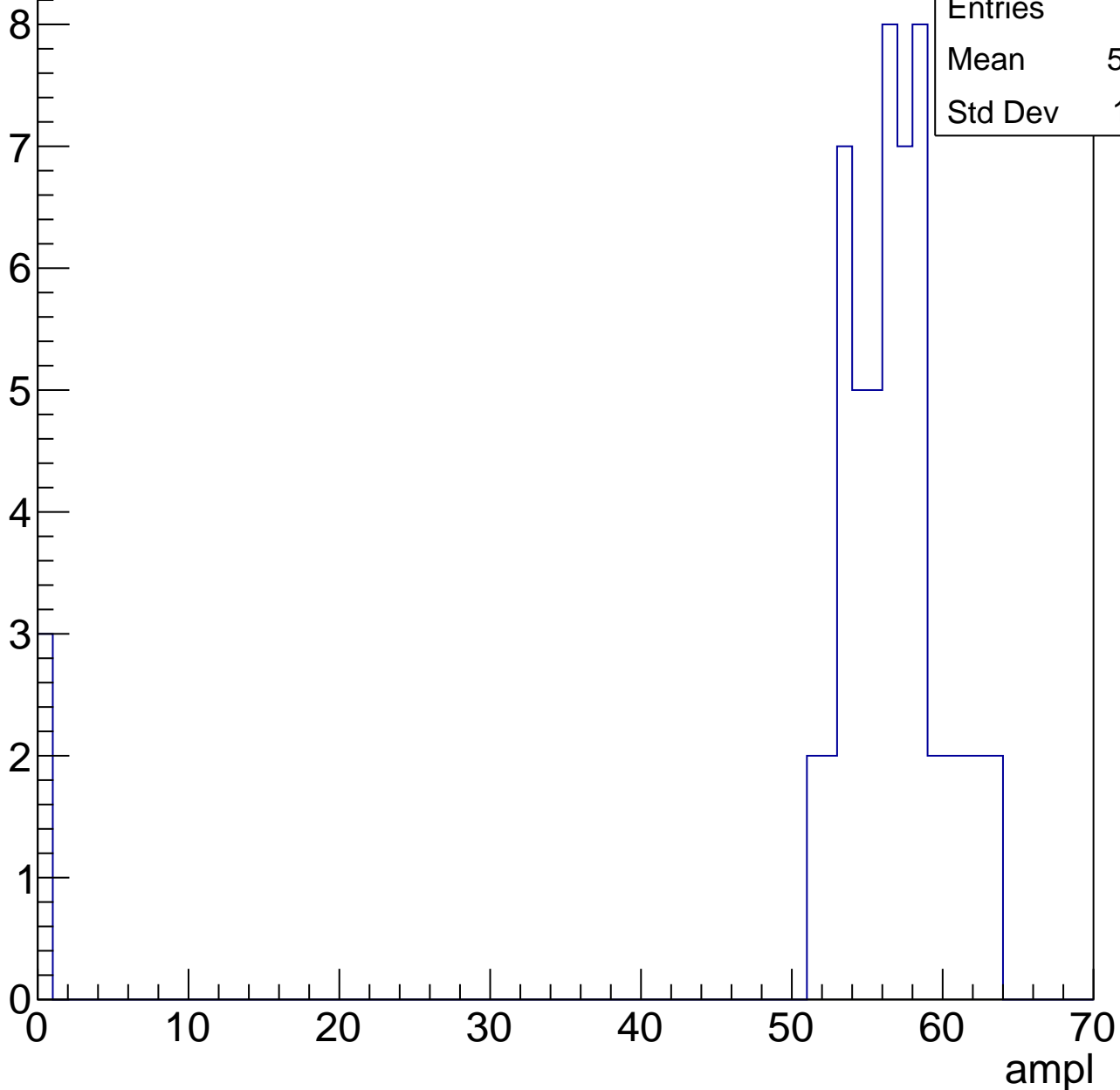


B1L103S, U12-ch69, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	57
Mean	53.39
Std Dev	12.91

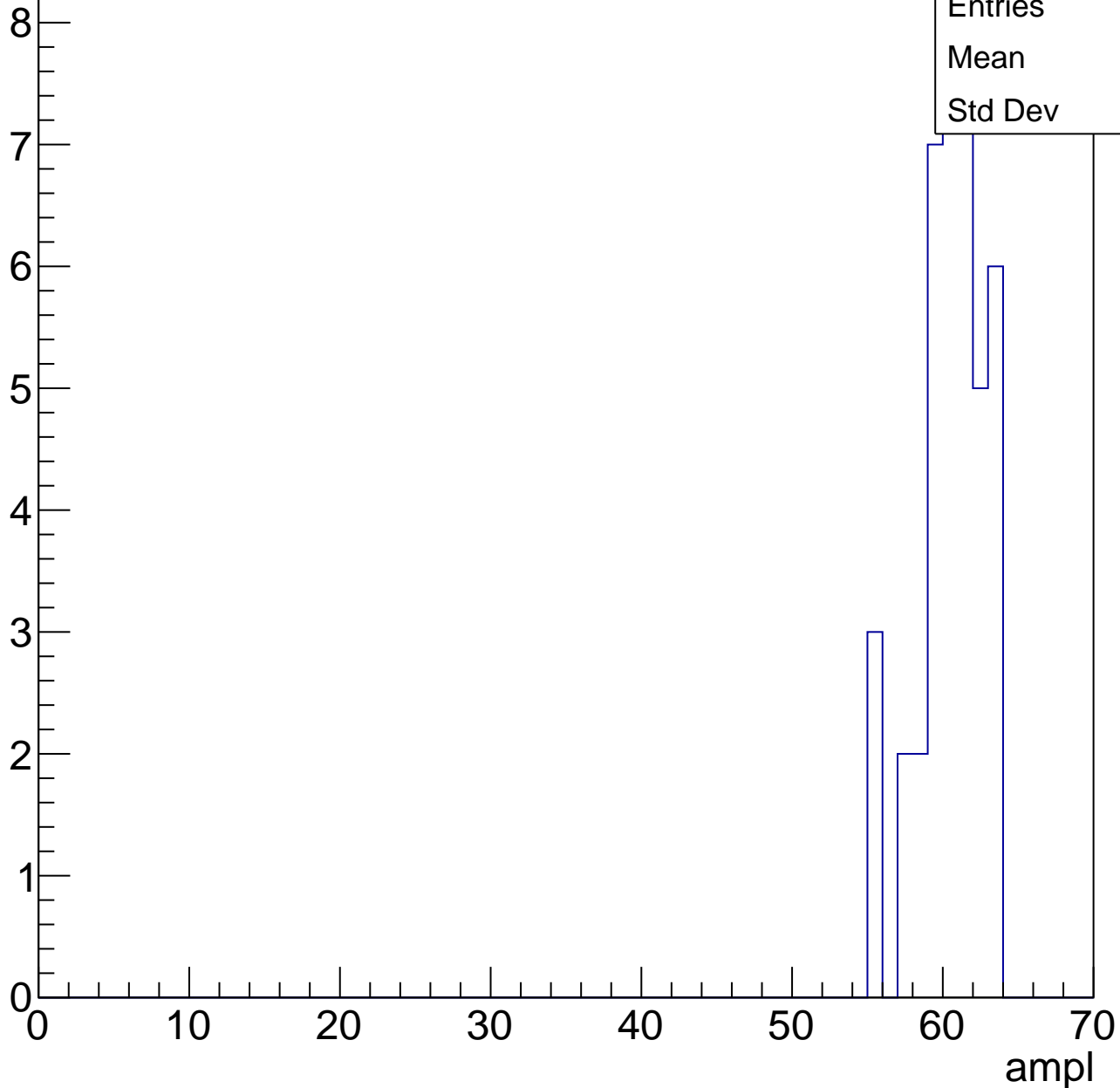


B1L103S, U12-ch69, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	41
Mean	60.1
Std Dev	2.15



B1L103S, U12-ch69, adc6

calib_packv5_041523_1651.root, FC#0, port C2

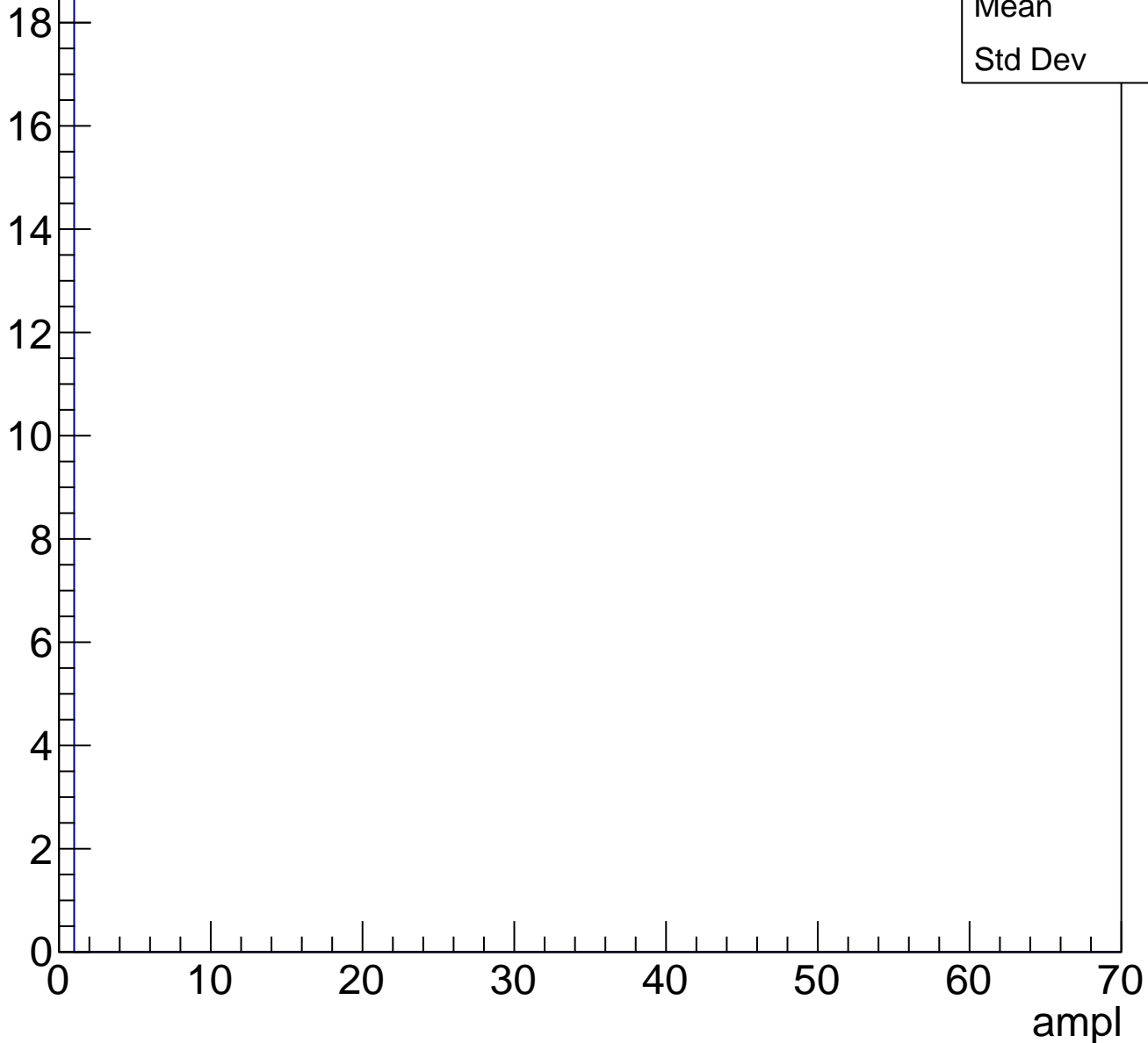
Entry



B1L103S, U12-ch69, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

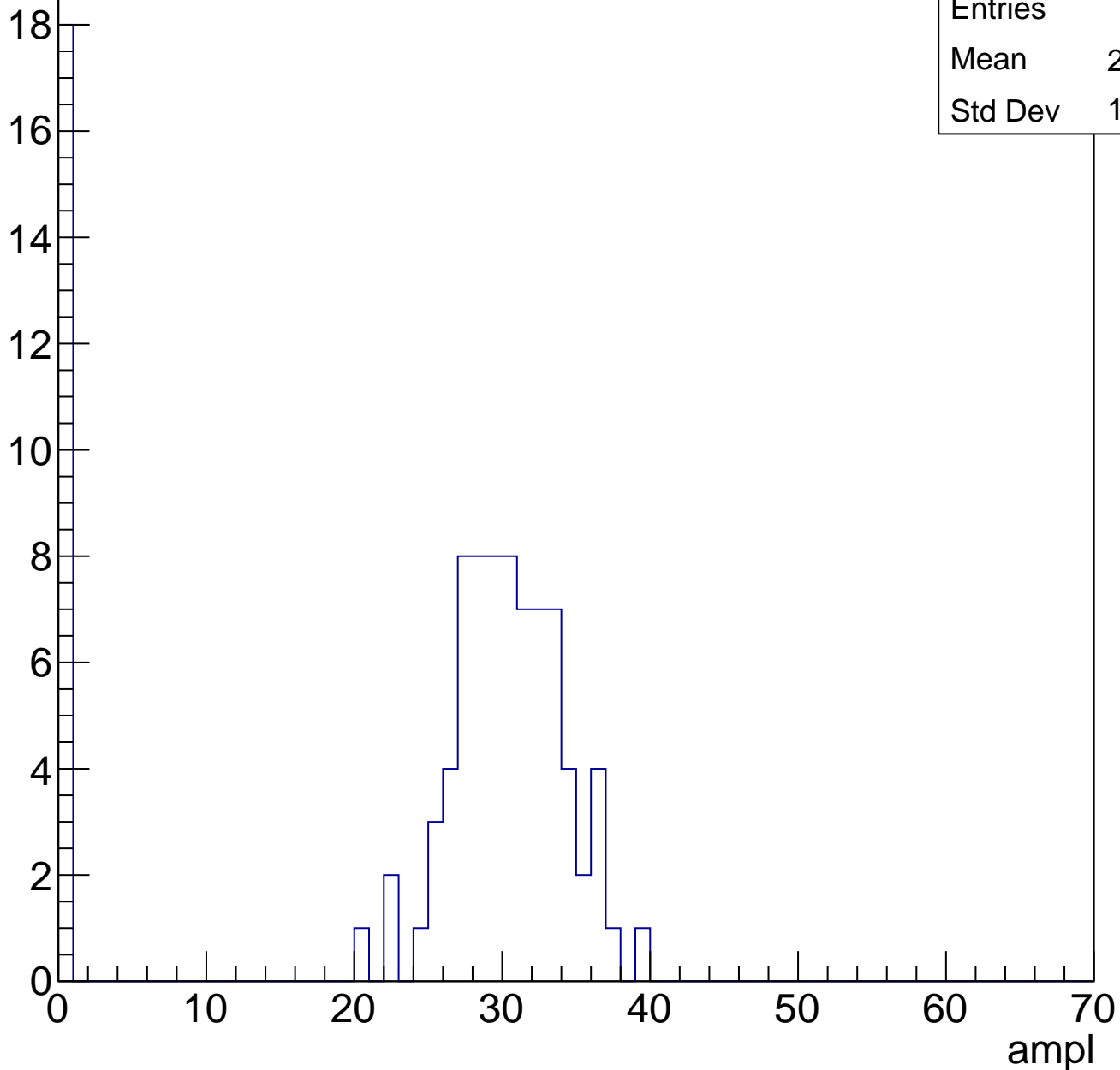


B1L103S, U12-ch70, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	94
Mean	24.22
Std Dev	12.23

Entry

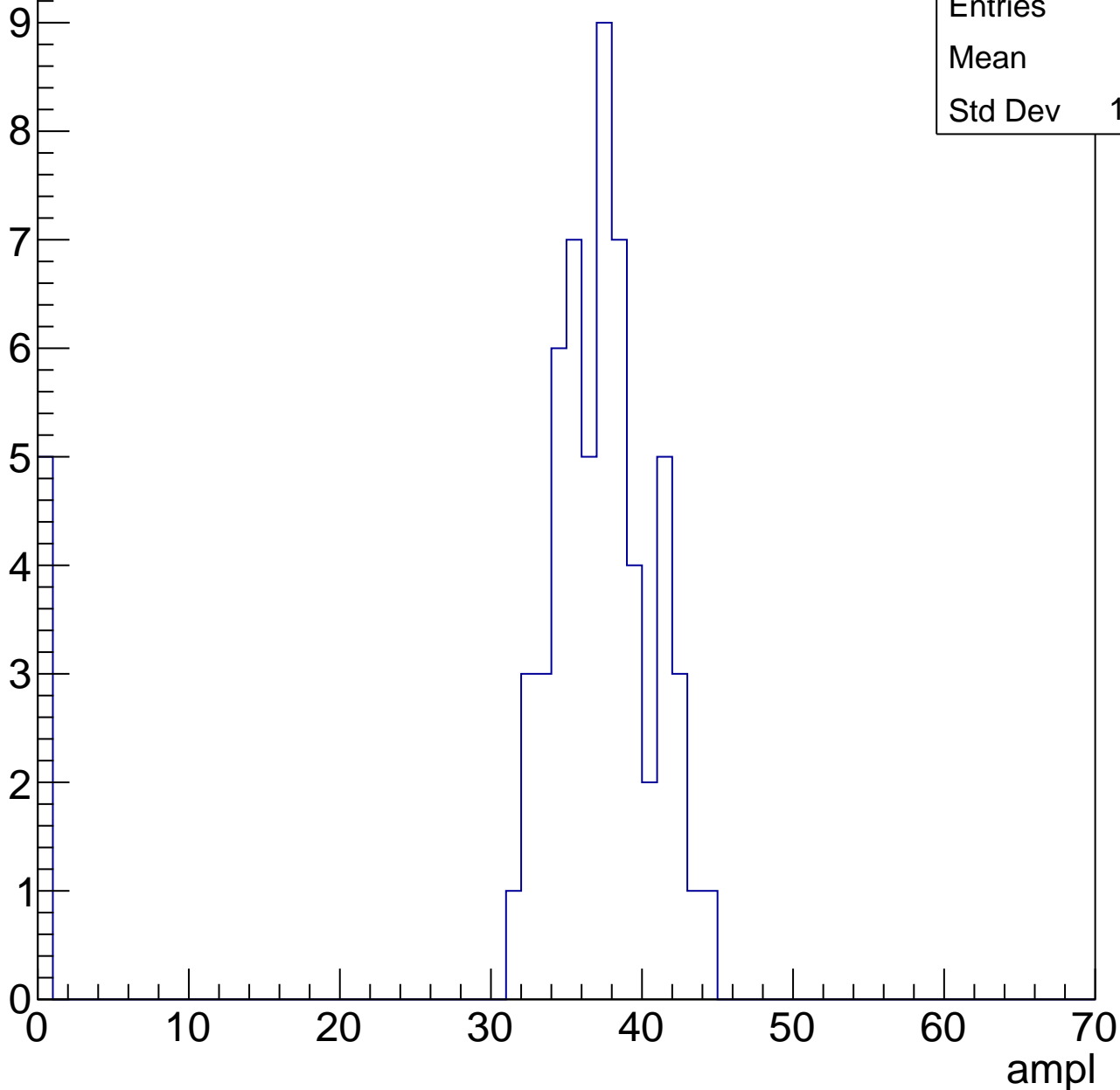


B1L103S, U12-ch70, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	34
Std Dev	10.48

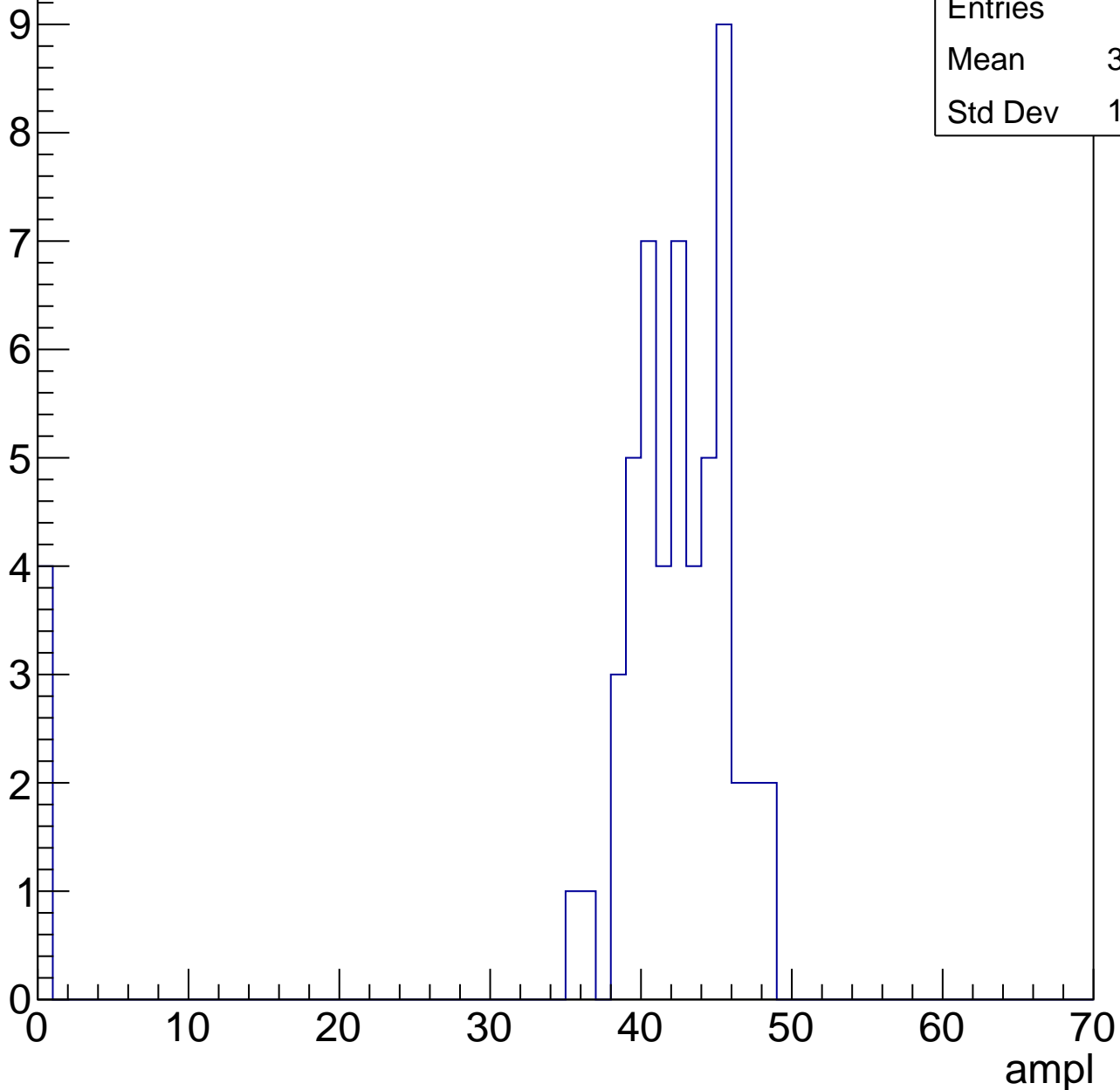


B1L103S, U12-ch70, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	56
Mean	39.23
Std Dev	11.26



B1L103S, U12-ch70, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	74
Mean	48.5
Std Dev	3.488

Entry

10

8

6

4

2

0

0

10

20

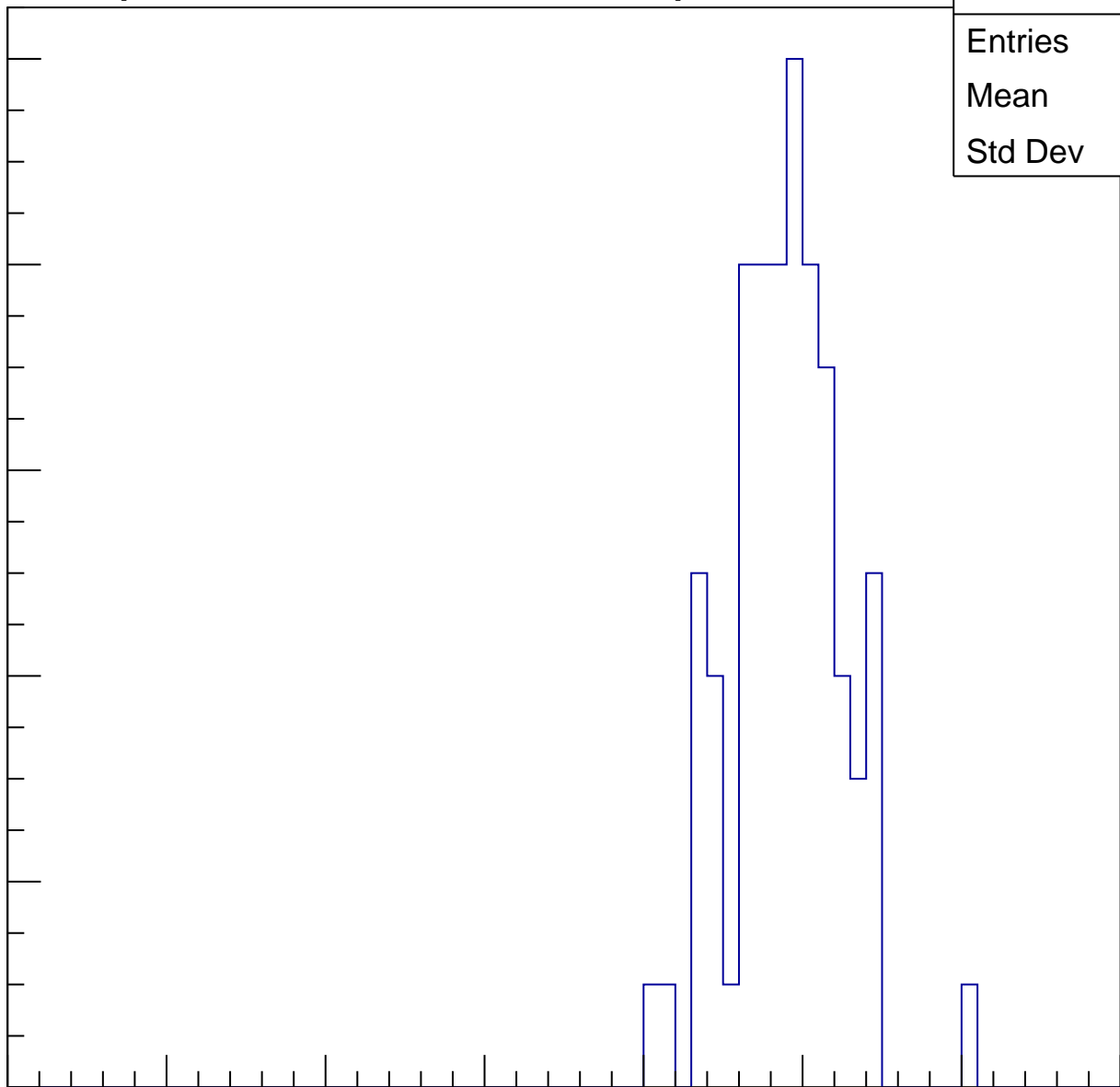
30

40

50

60

ampl

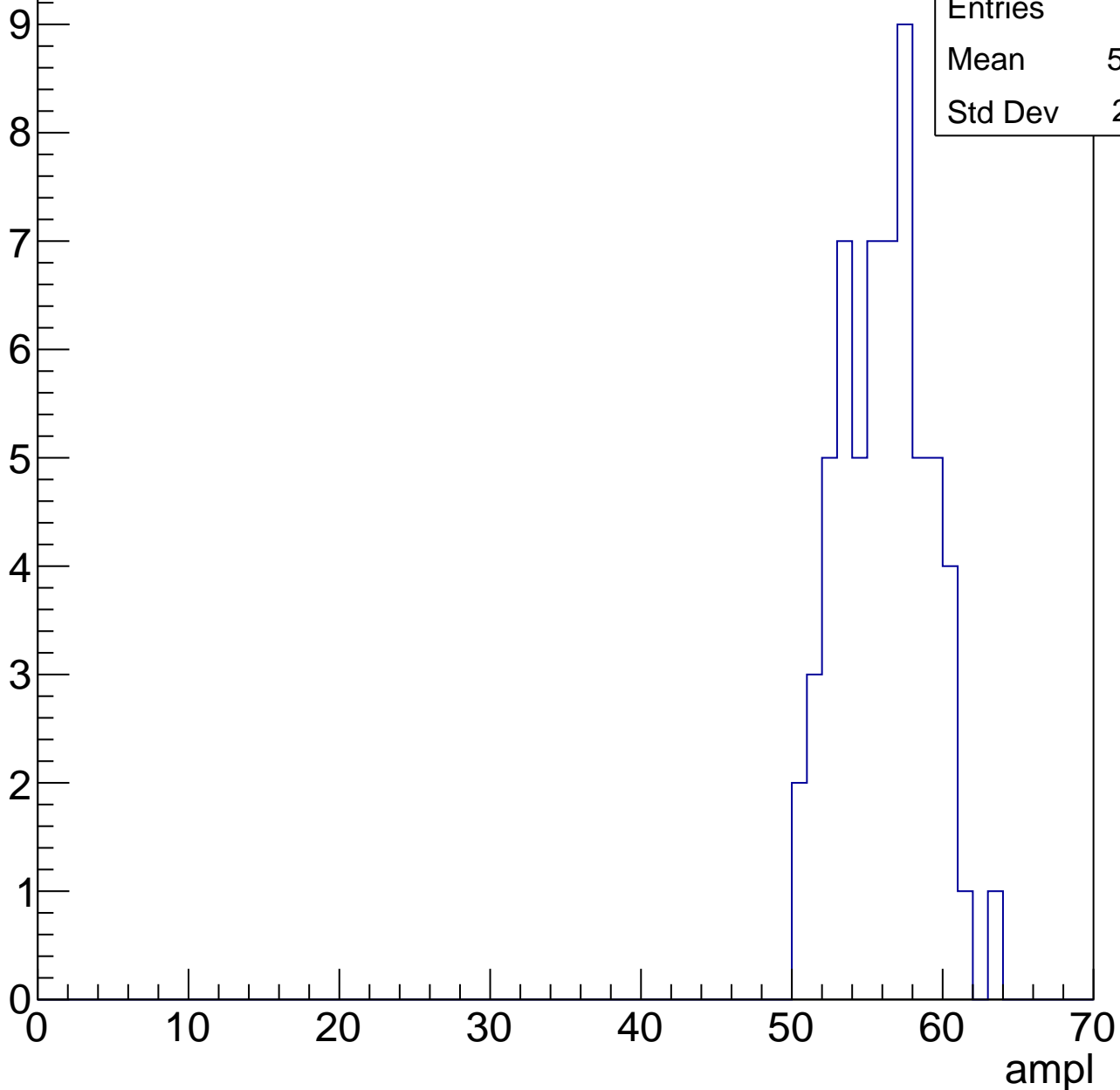


B1L103S, U12-ch70, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	55.62
Std Dev	2.921

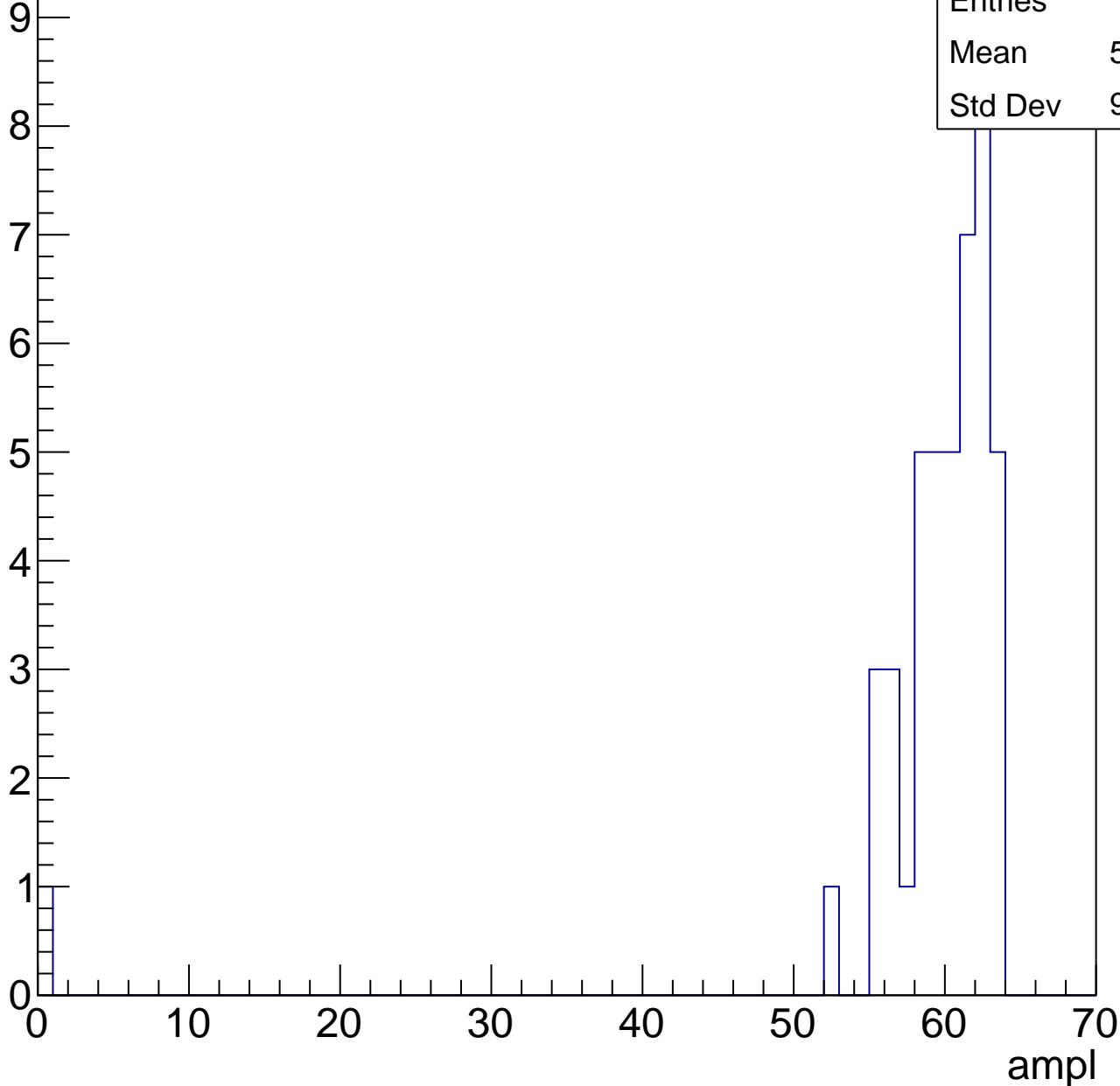


B1L103S, U12-ch70, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	45
Mean	58.38
Std Dev	9.178



B1L103S, U12-ch70, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch70, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.15
Std Dev	13.73

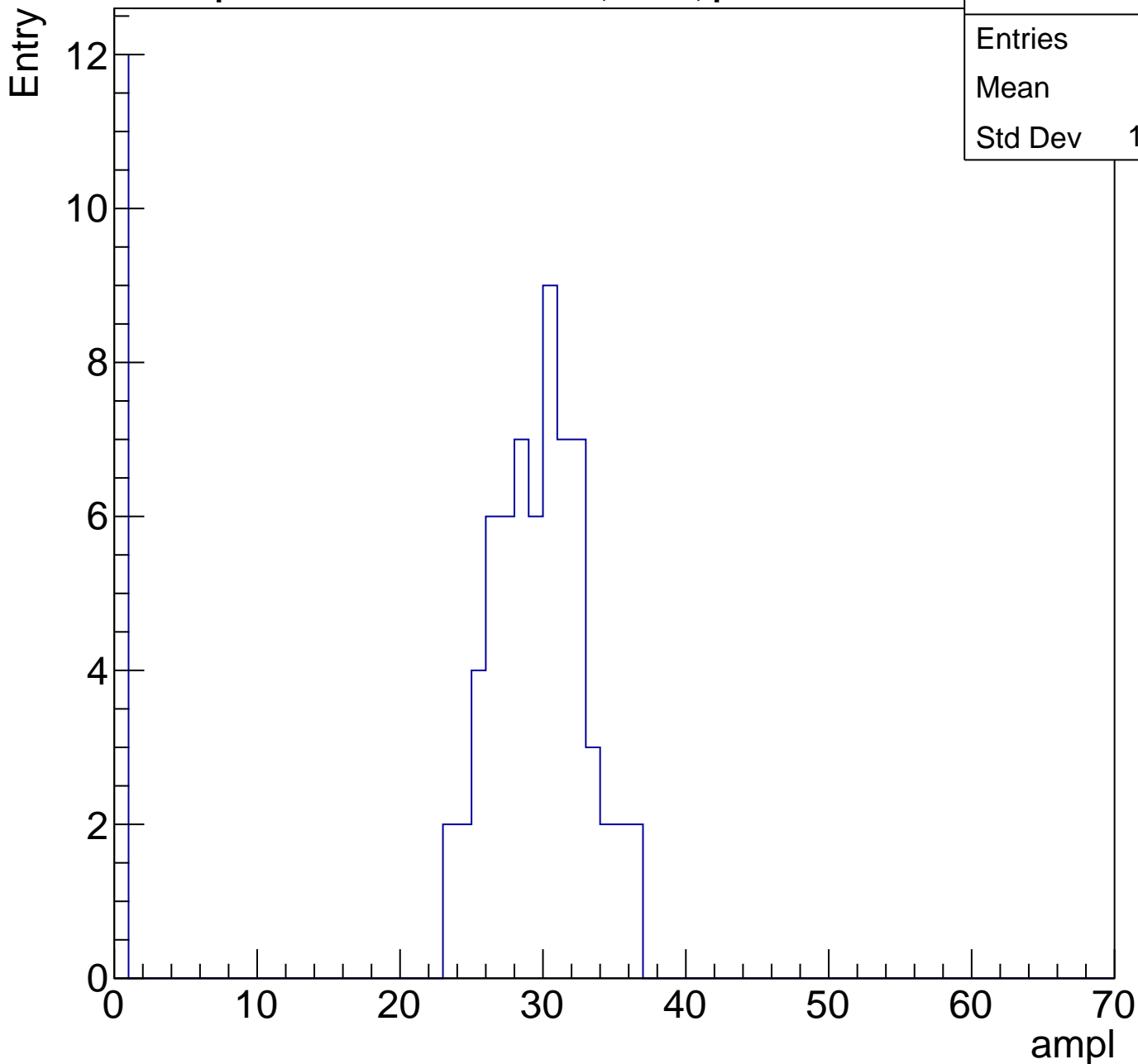
Entry



B1L103S, U12-ch71, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	77
Mean	24.7
Std Dev	10.99

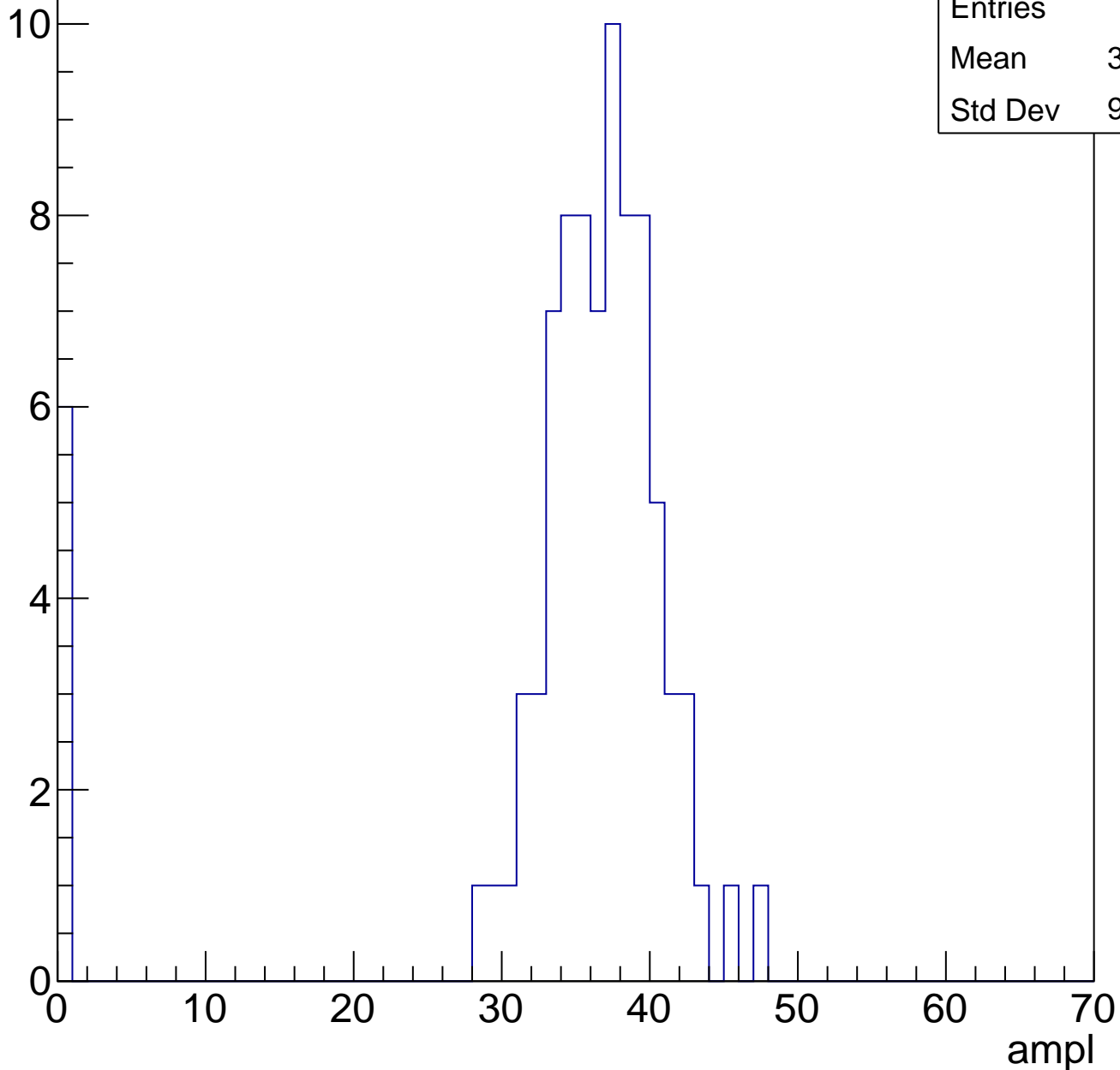


B1L103S, U12-ch71, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	85
Mean	33.89
Std Dev	9.942

Entry

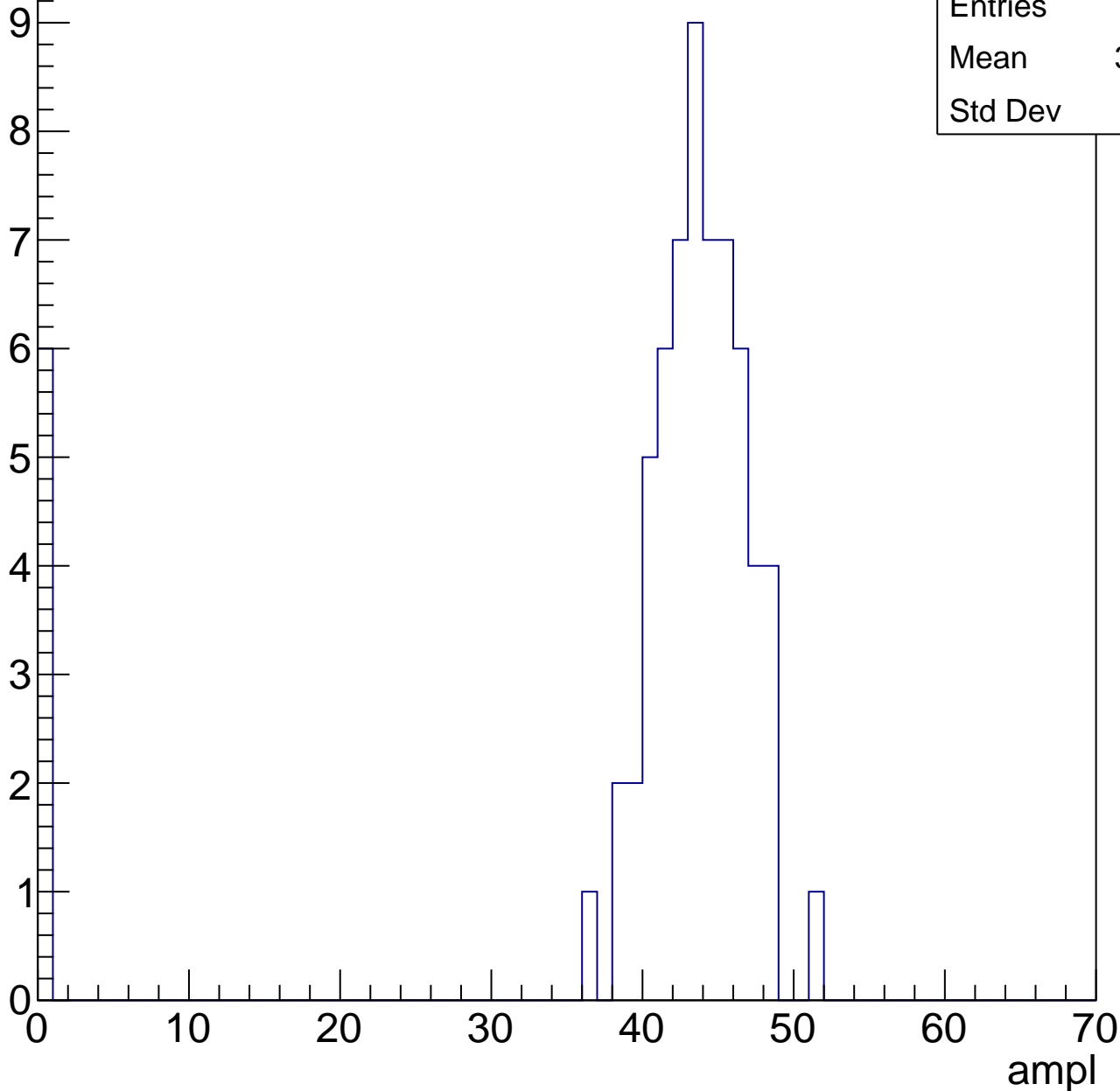


B1L103S, U12-ch71, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	39.51
Std Dev	12.7

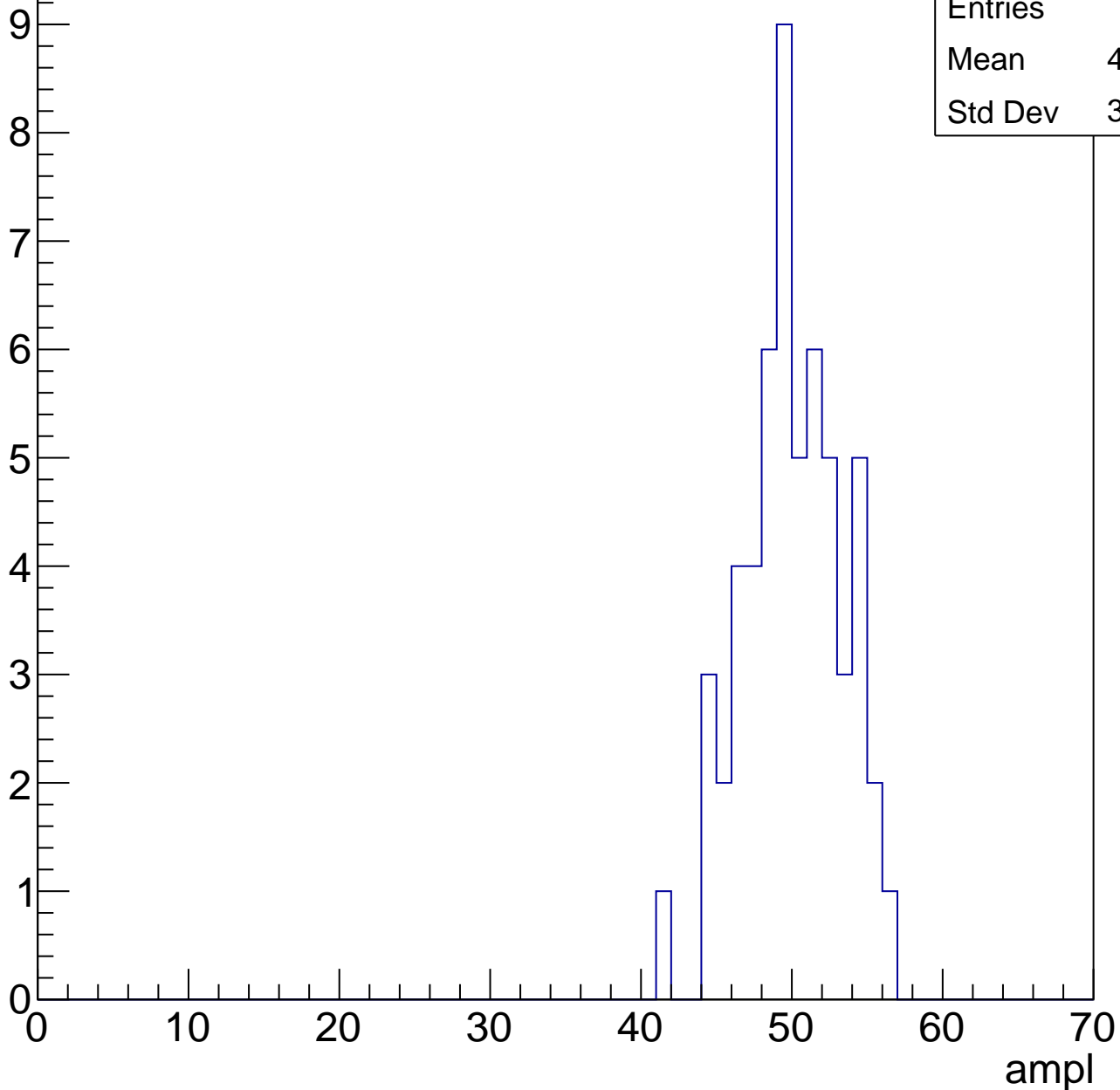


B1L103S, U12-ch71, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	56
Mean	49.55
Std Dev	3.218

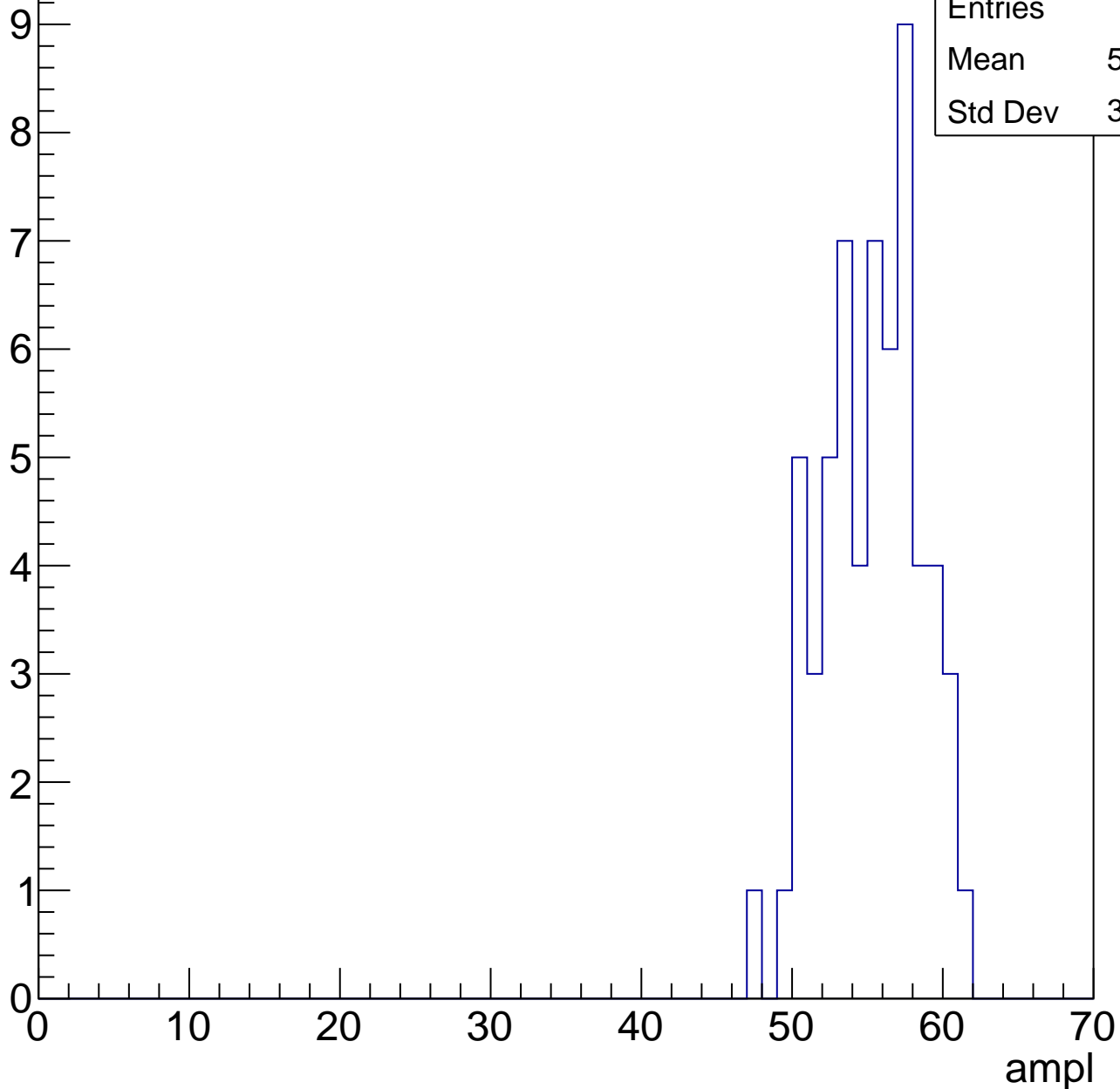


B1L103S, U12-ch71, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	54.82
Std Dev	3.165

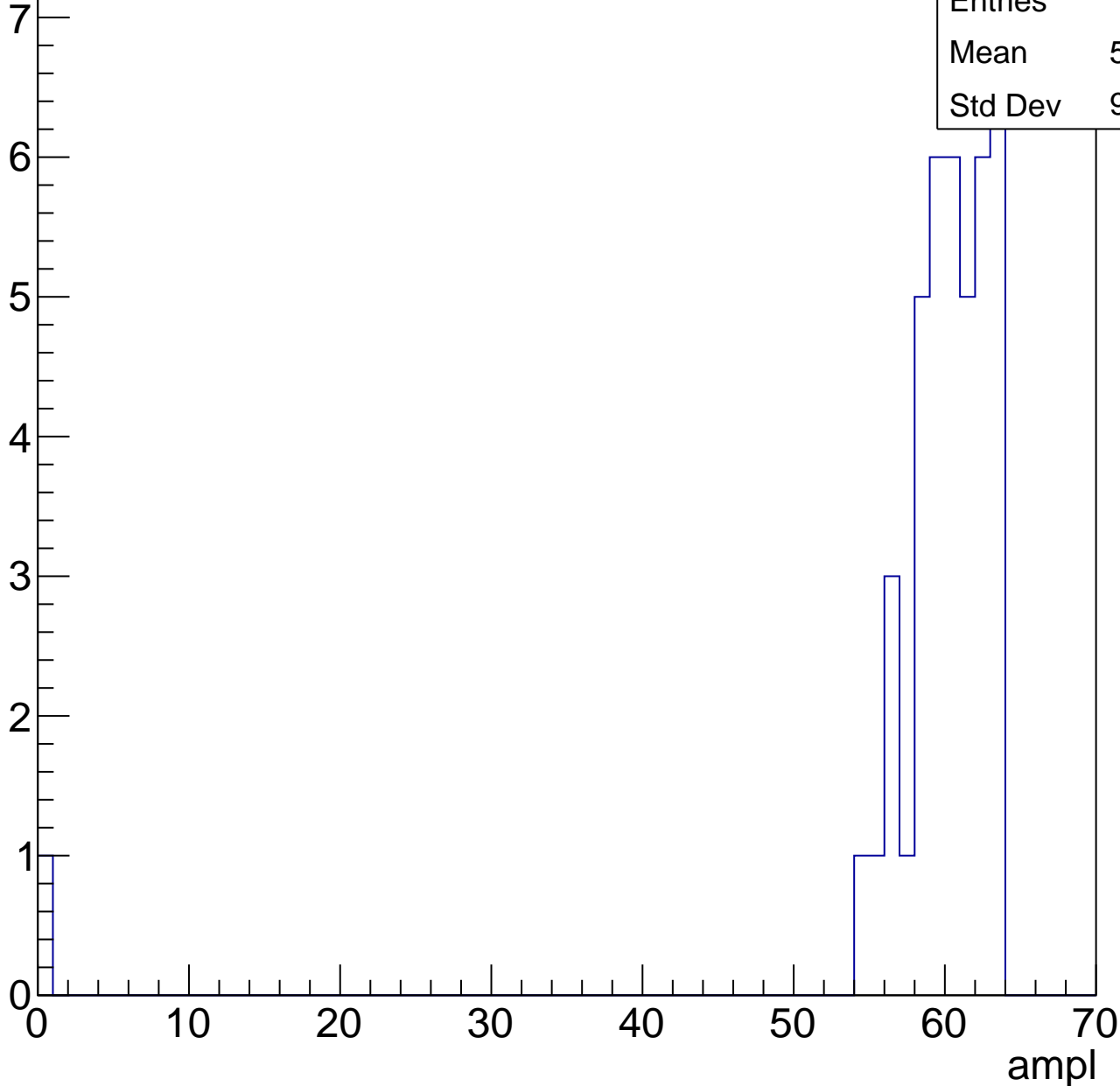


B1L103S, U12-ch71, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

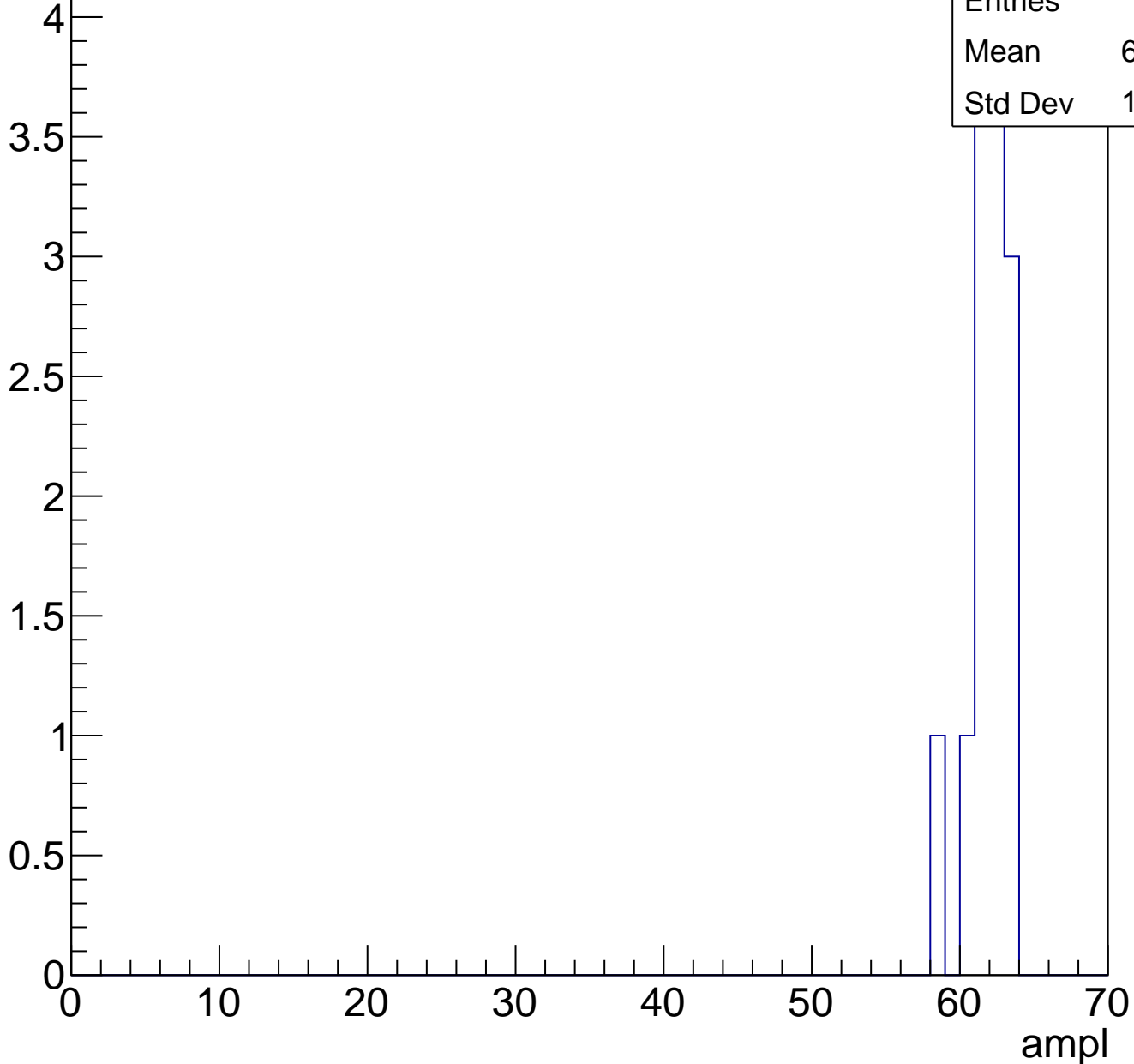
Entries	42
Mean	58.48
Std Dev	9.435



B1L103S, U12-ch71, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch71, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

ampl

B1L103S, U12-ch72, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	90
Mean	23.31
Std Dev	11.6

Entry

16
14
12
10
8
6
4
2
0

0

10

20

30

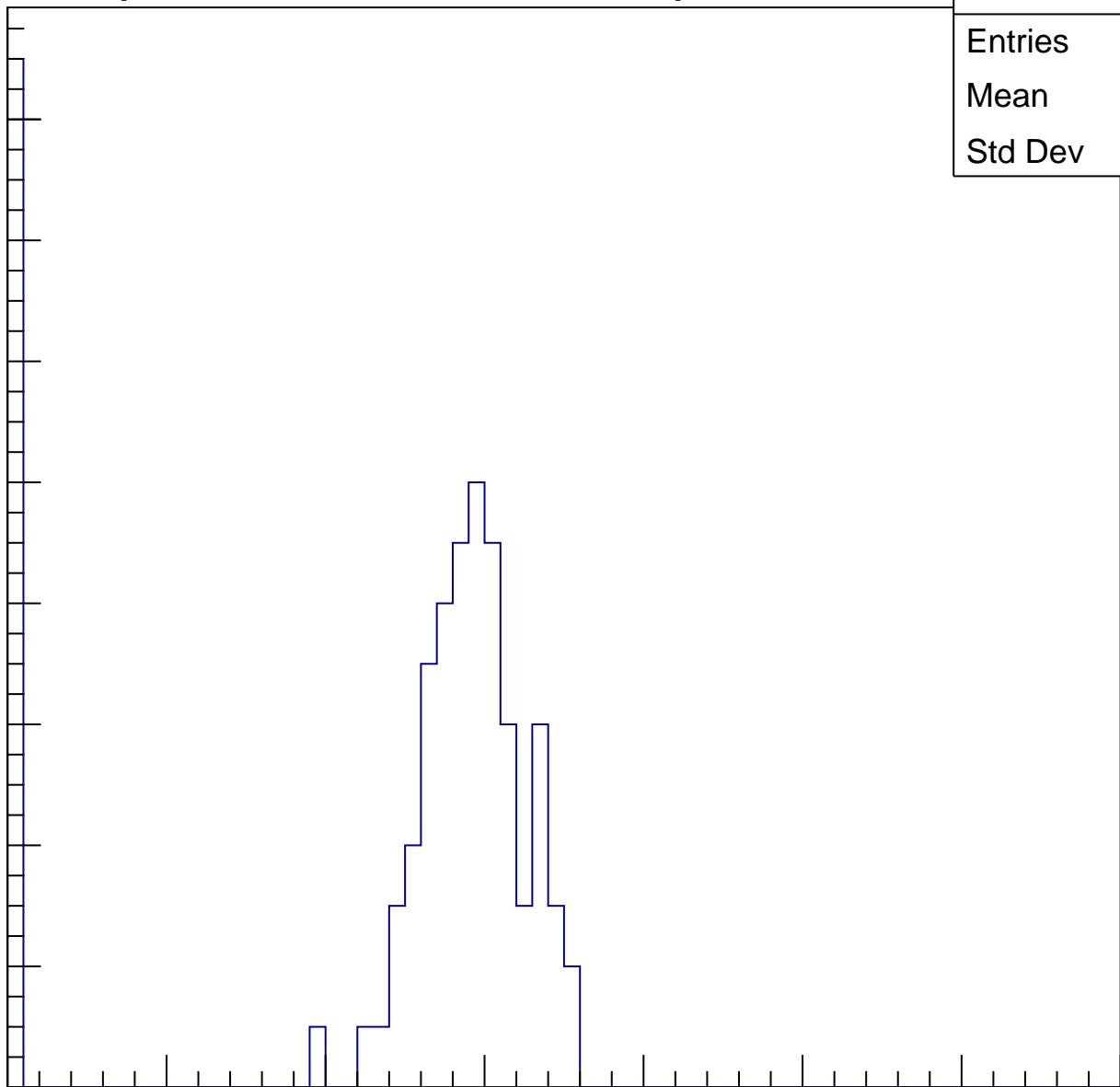
40

50

60

70

ampl

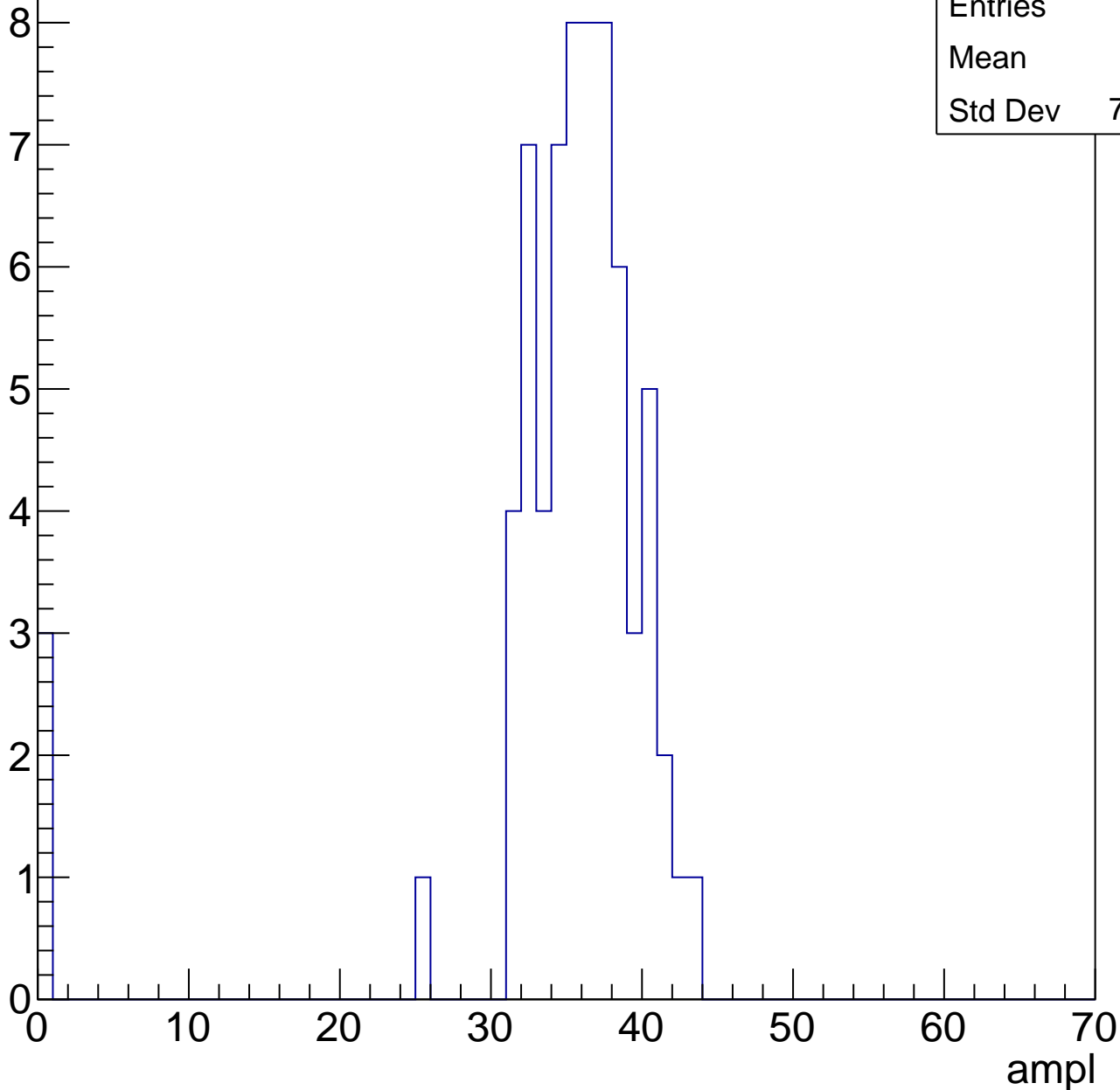


B1L103S, U12-ch72, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	34.1
Std Dev	7.973

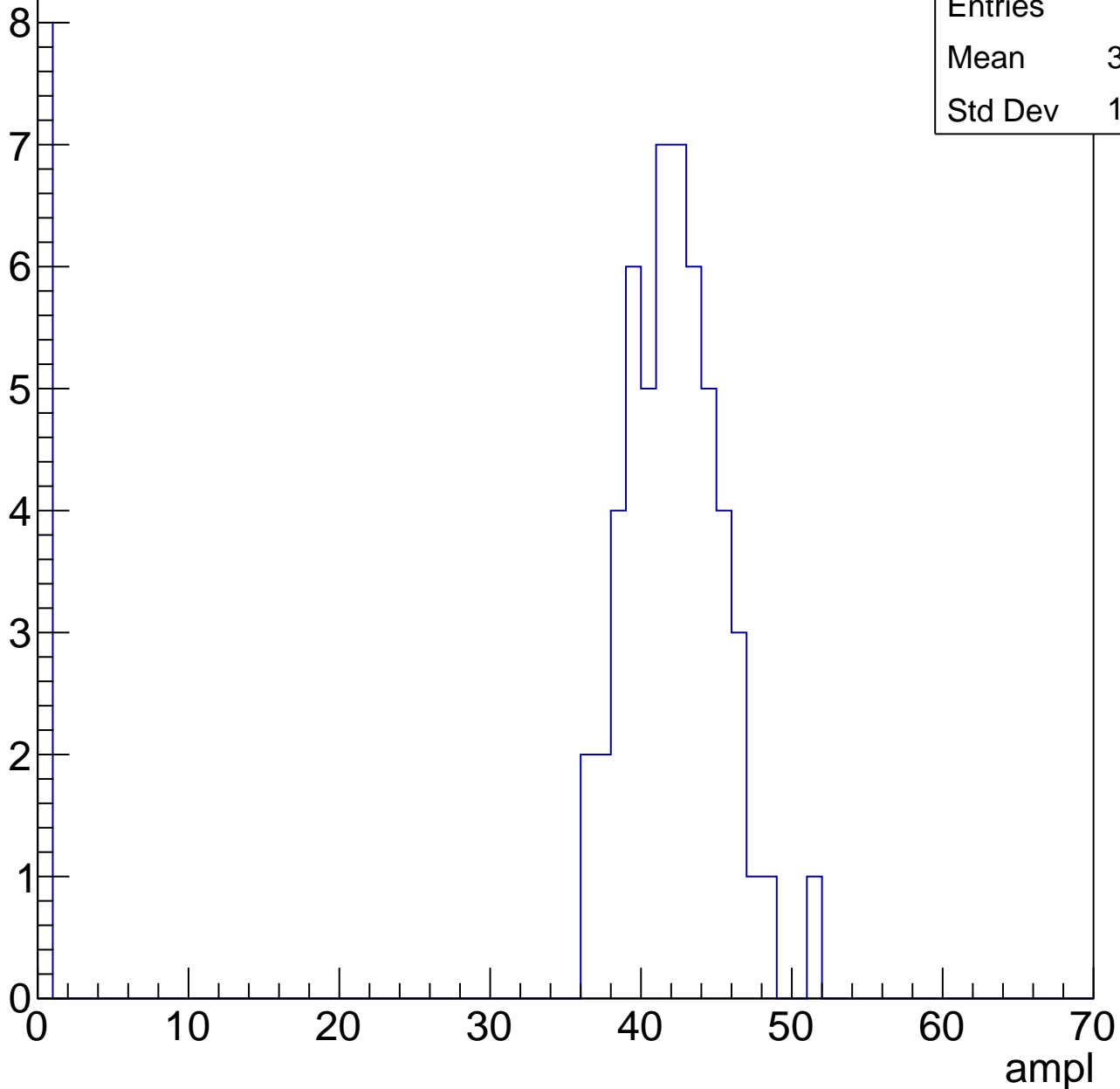


B1L103S, U12-ch72, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	36.37
Std Dev	14.29

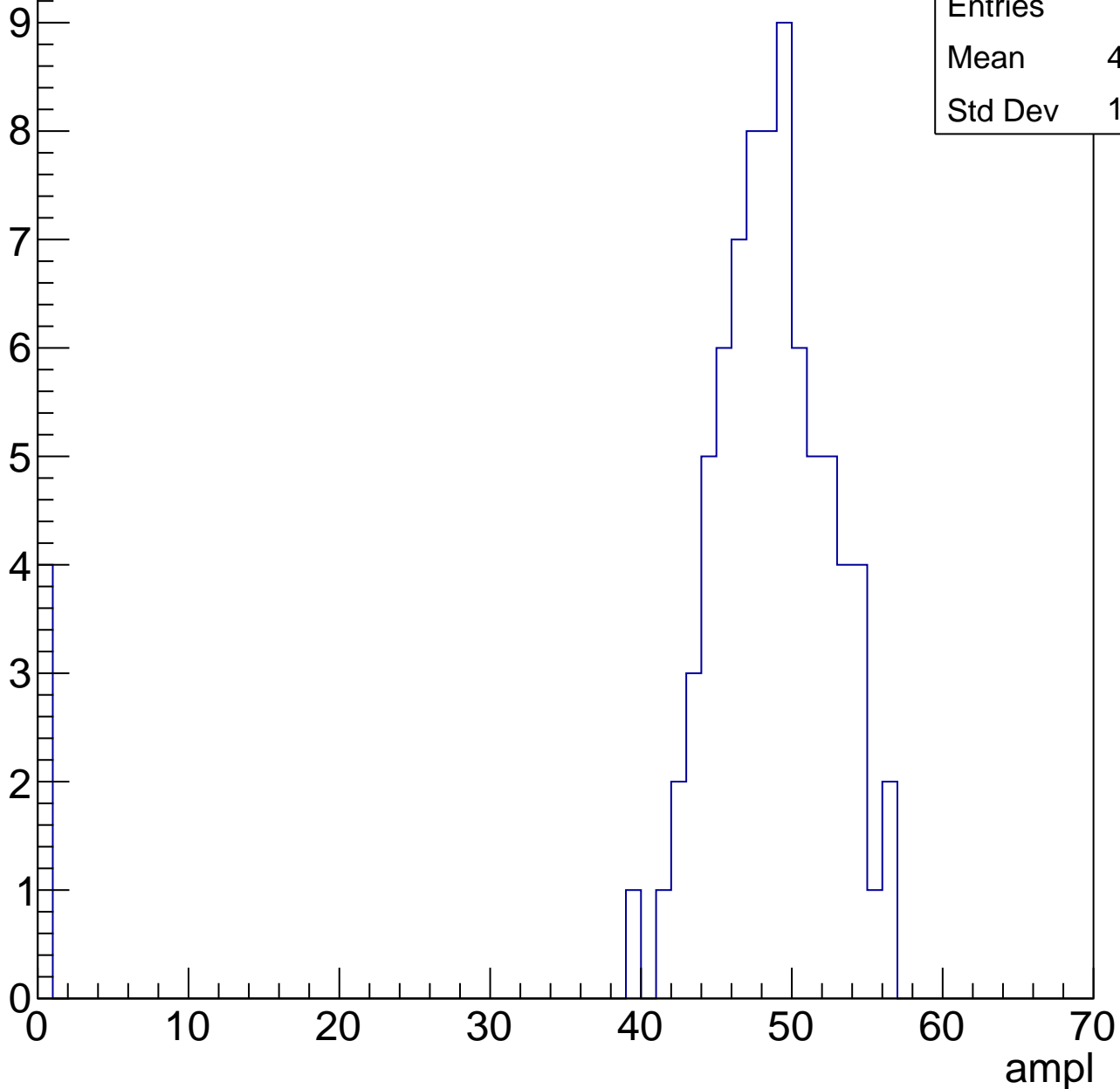


B1L103S, U12-ch72, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	81
Mean	45.88
Std Dev	11.04

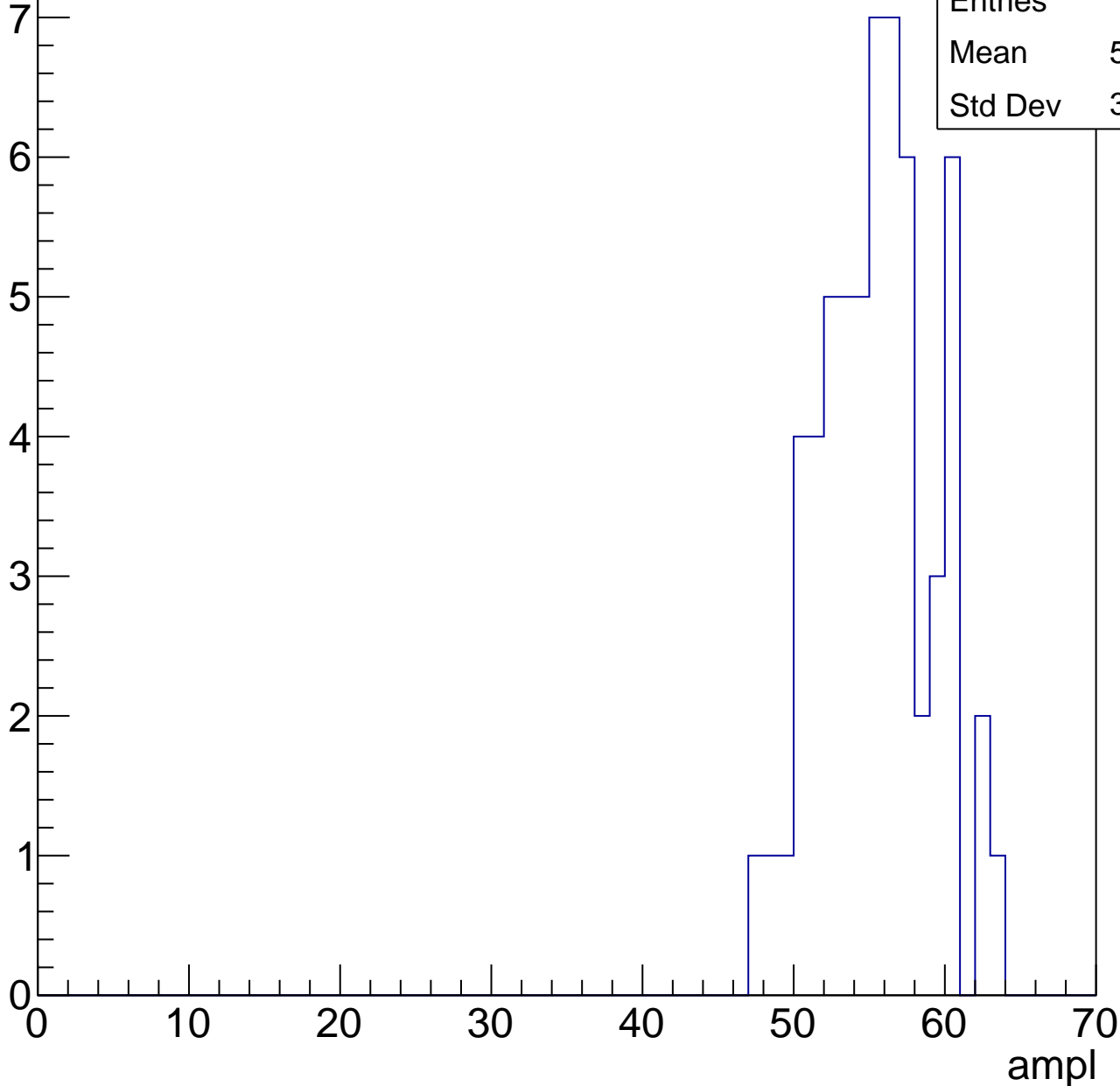


B1L103S, U12-ch72, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

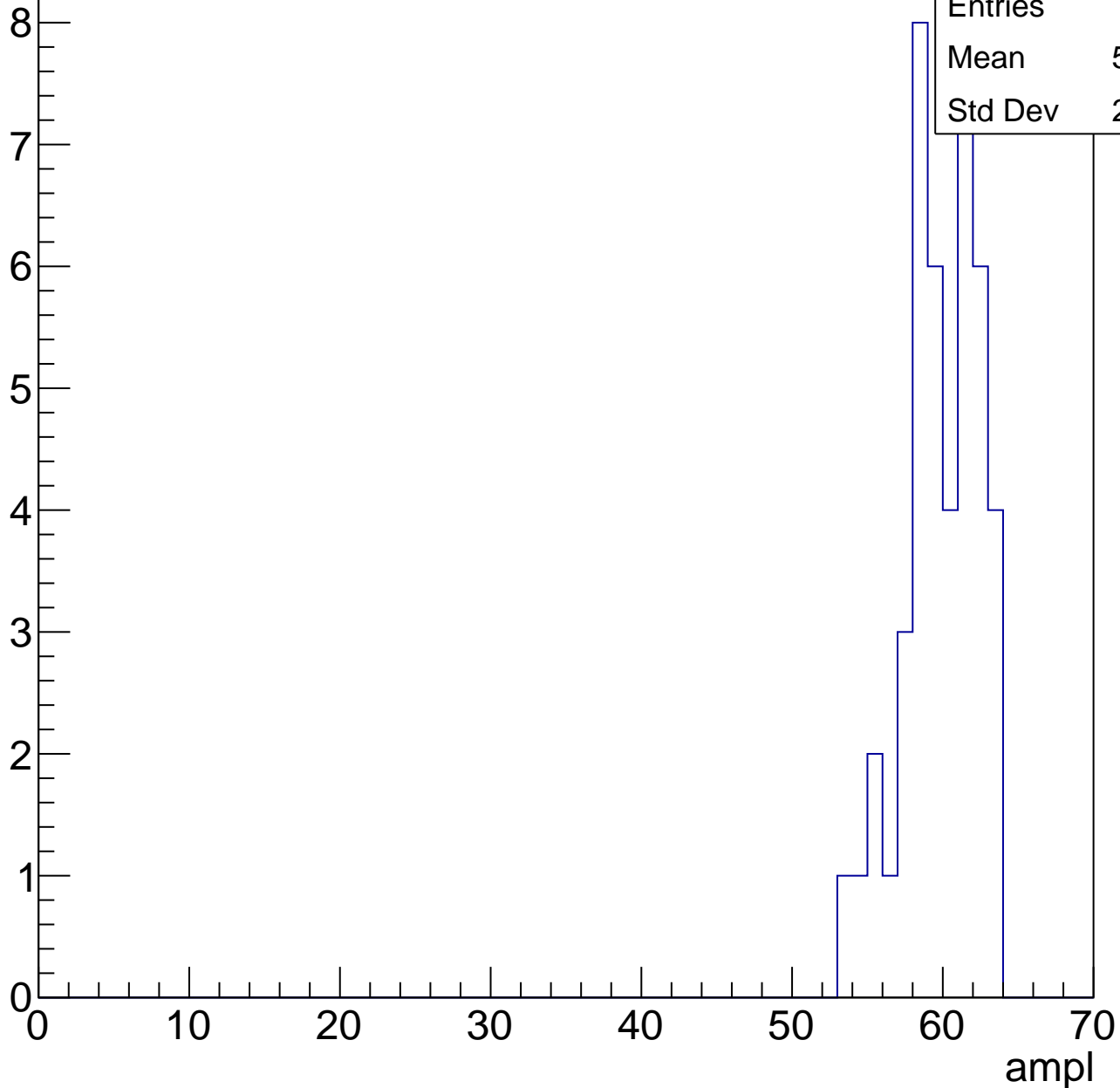
Entries	60
Mean	55.03
Std Dev	3.633



B1L103S, U12-ch72, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

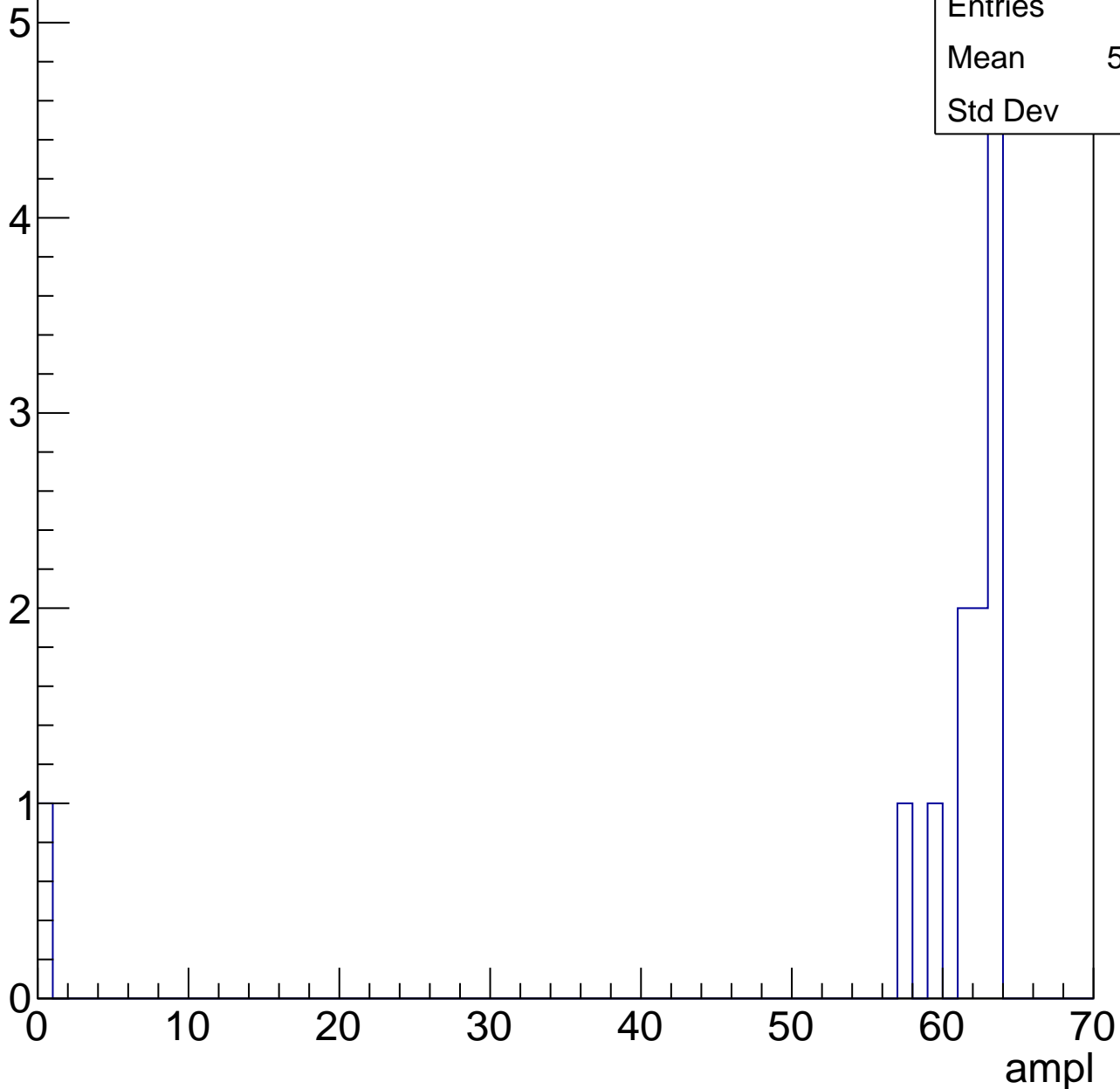


B1L103S, U12-ch72, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	12
Mean	56.42
Std Dev	17.1



B1L103S, U12-ch72, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

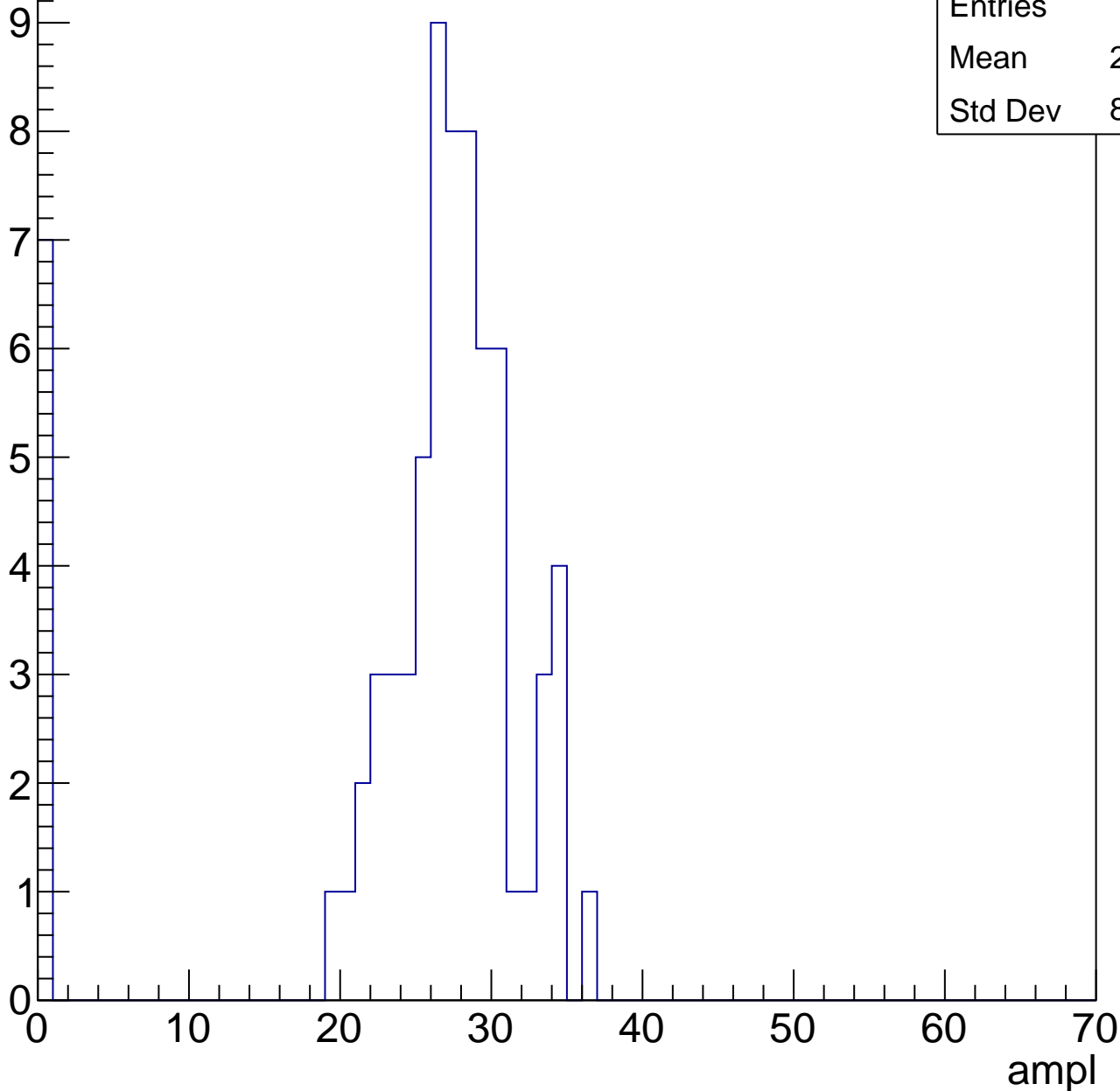


B1L103S, U12-ch73, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	72
Mean	24.65
Std Dev	8.805

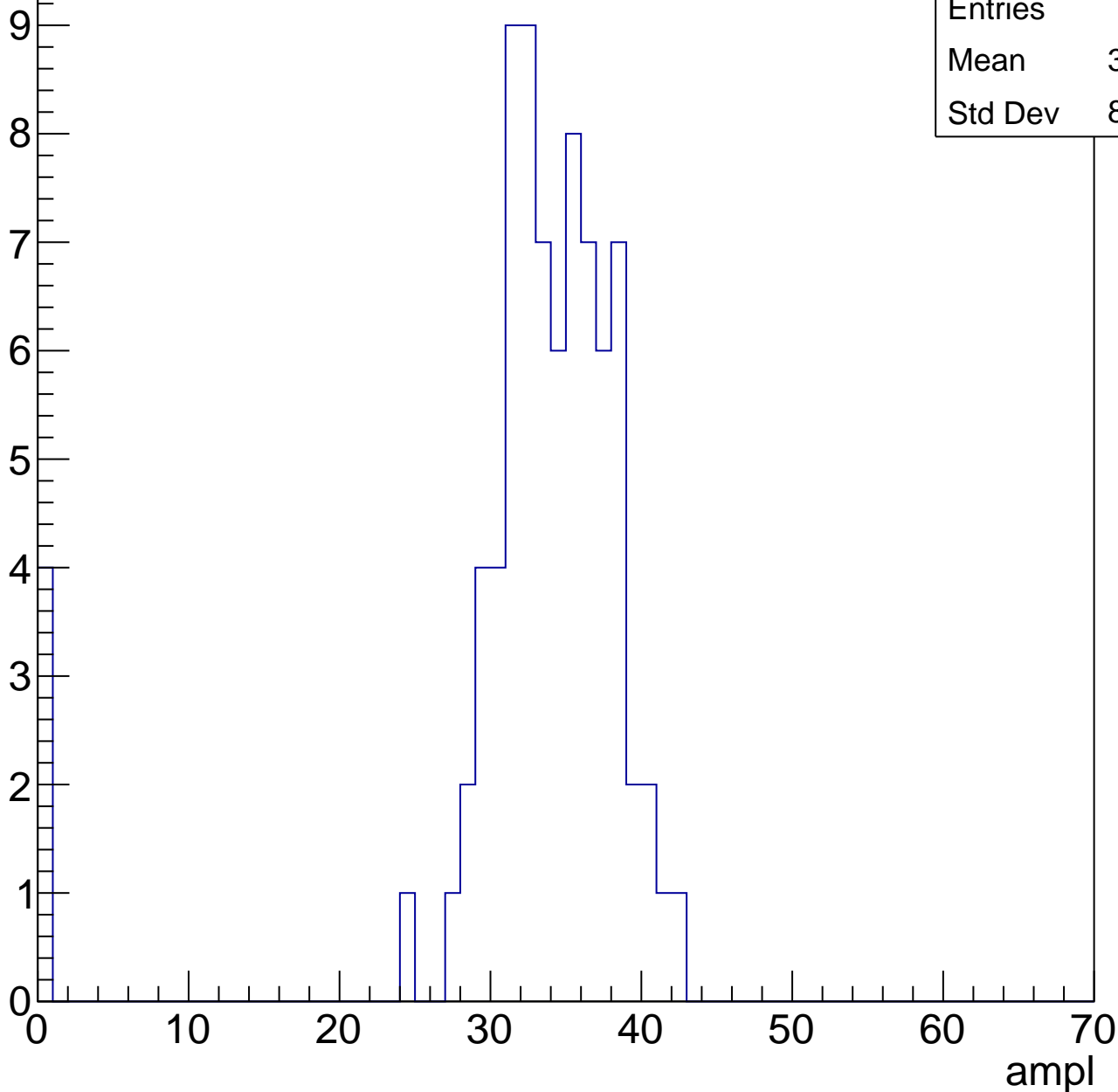


B1L103S, U12-ch73, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	81
Mean	32.17
Std Dev	8.089

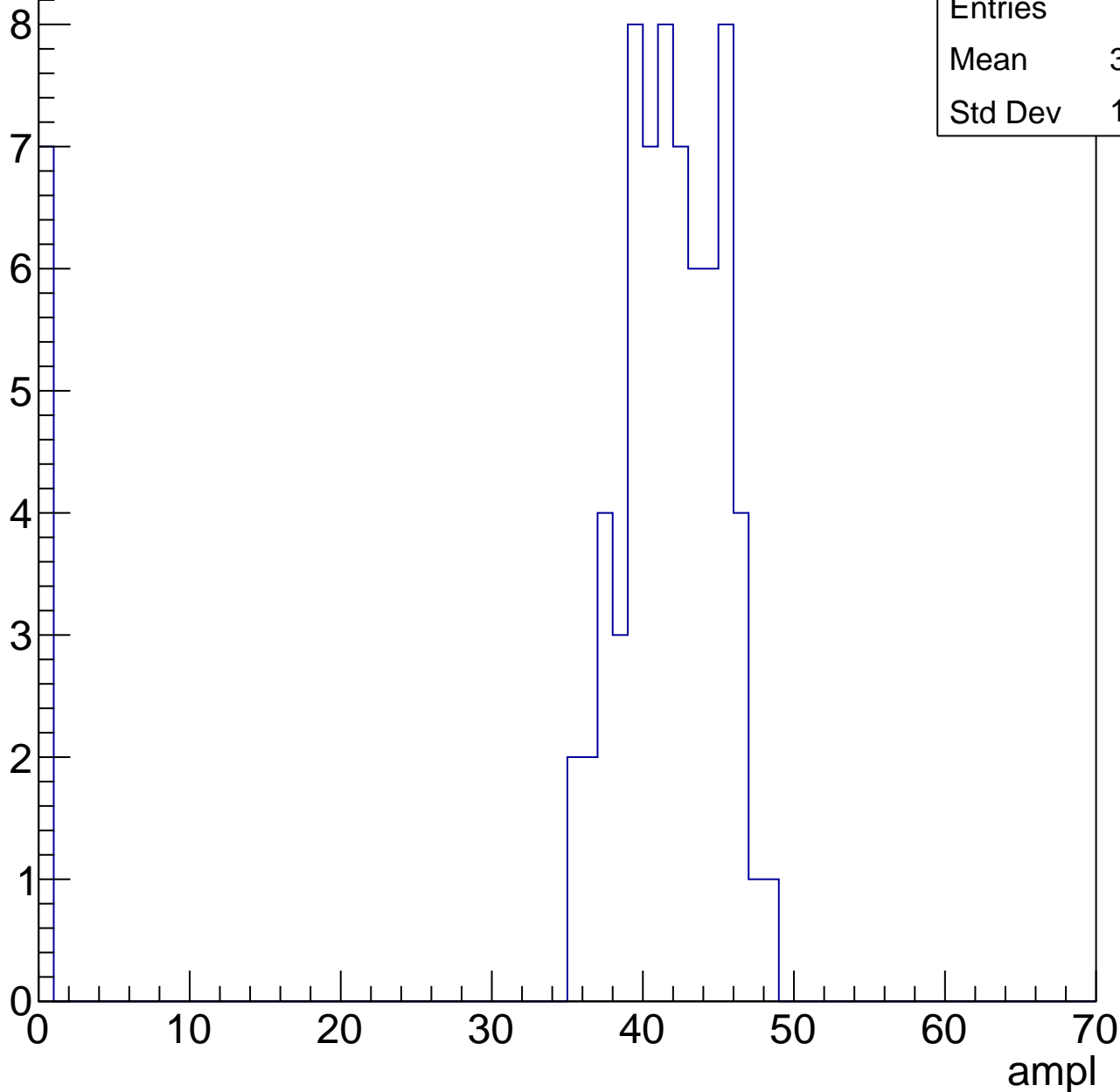


B1L103S, U12-ch73, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	74
Mean	37.55
Std Dev	12.49

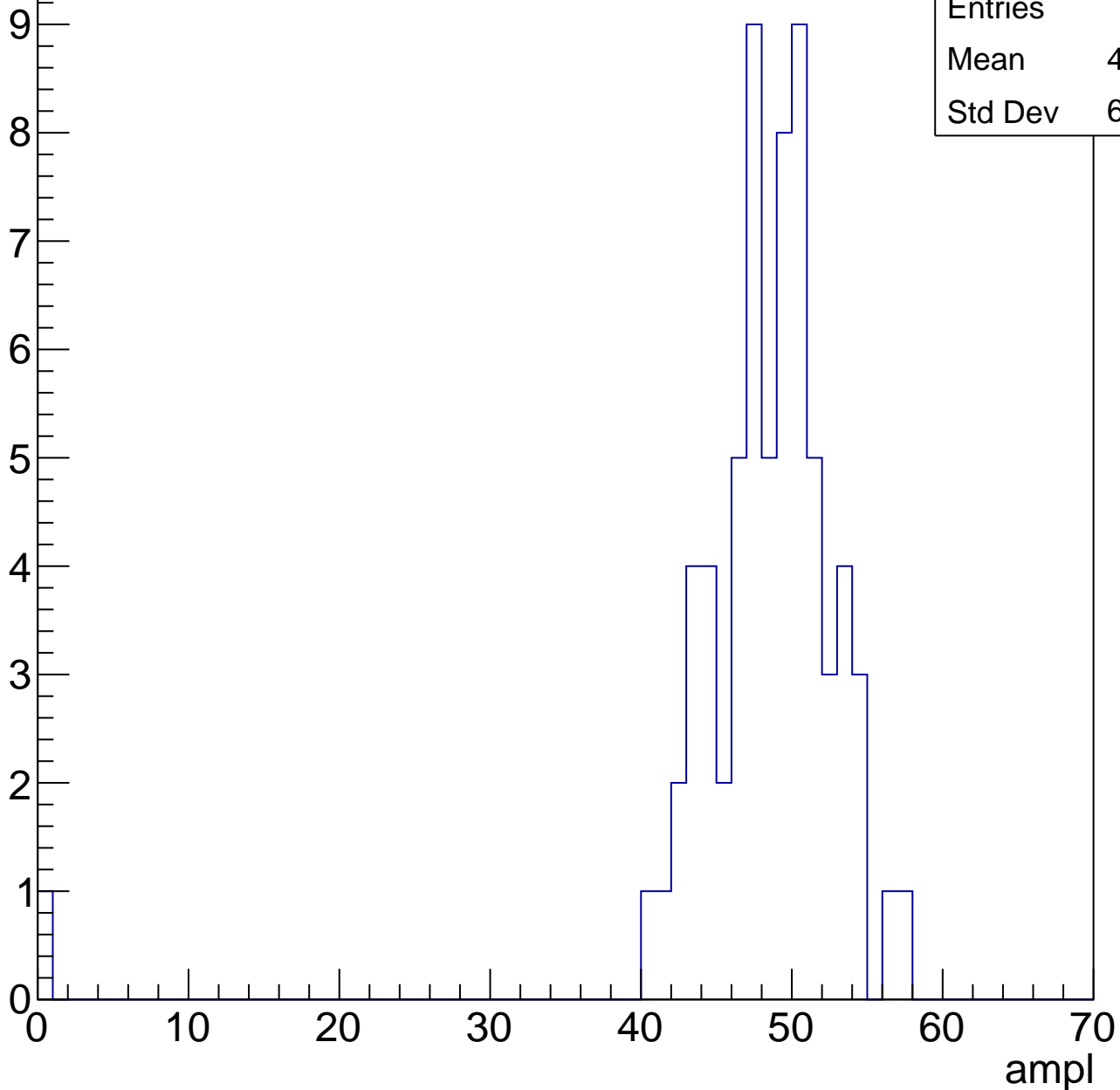


B1L103S, U12-ch73, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	47.59
Std Dev	6.837

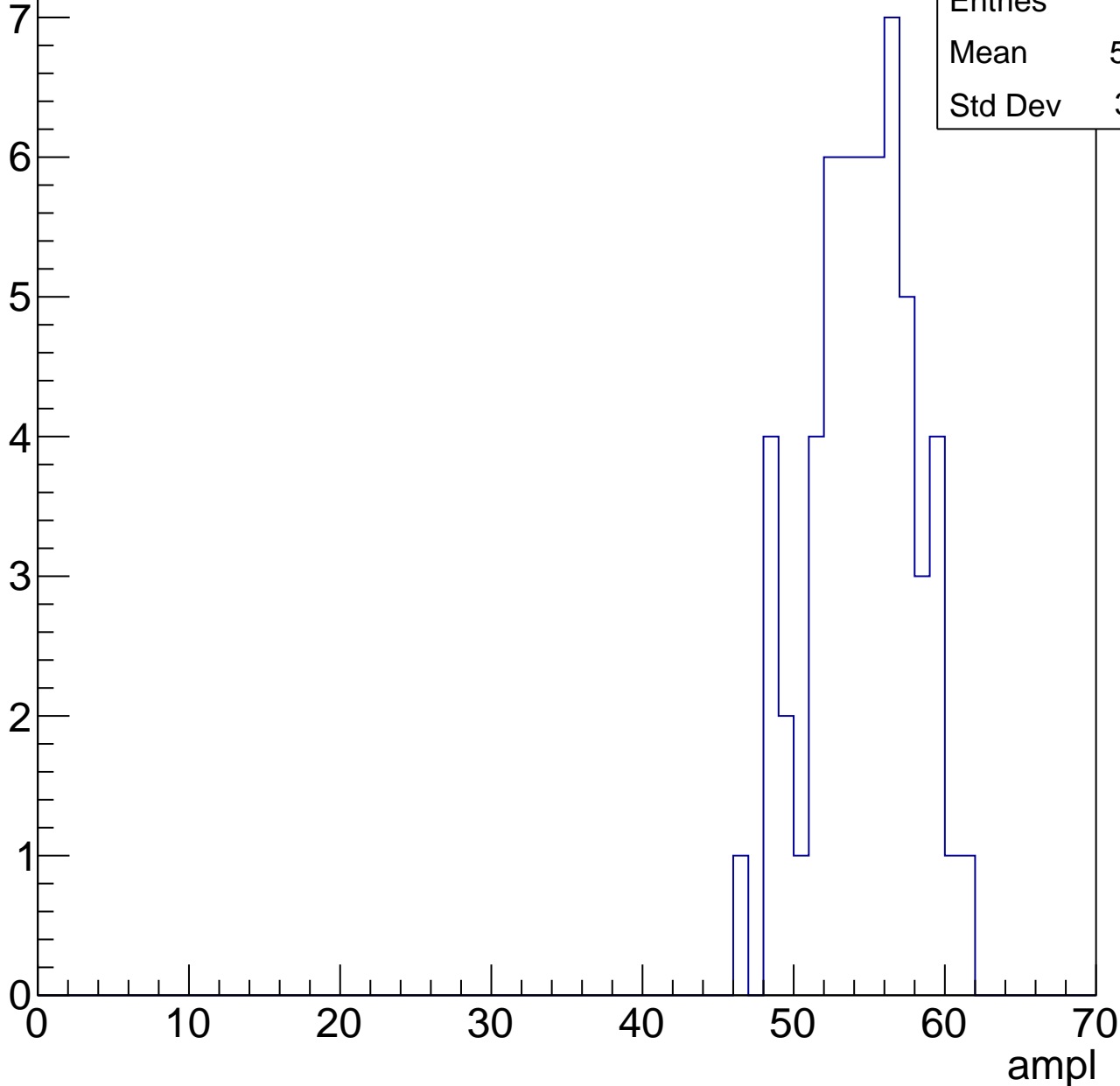


B1L103S, U12-ch73, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	57
Mean	54.07
Std Dev	3.381

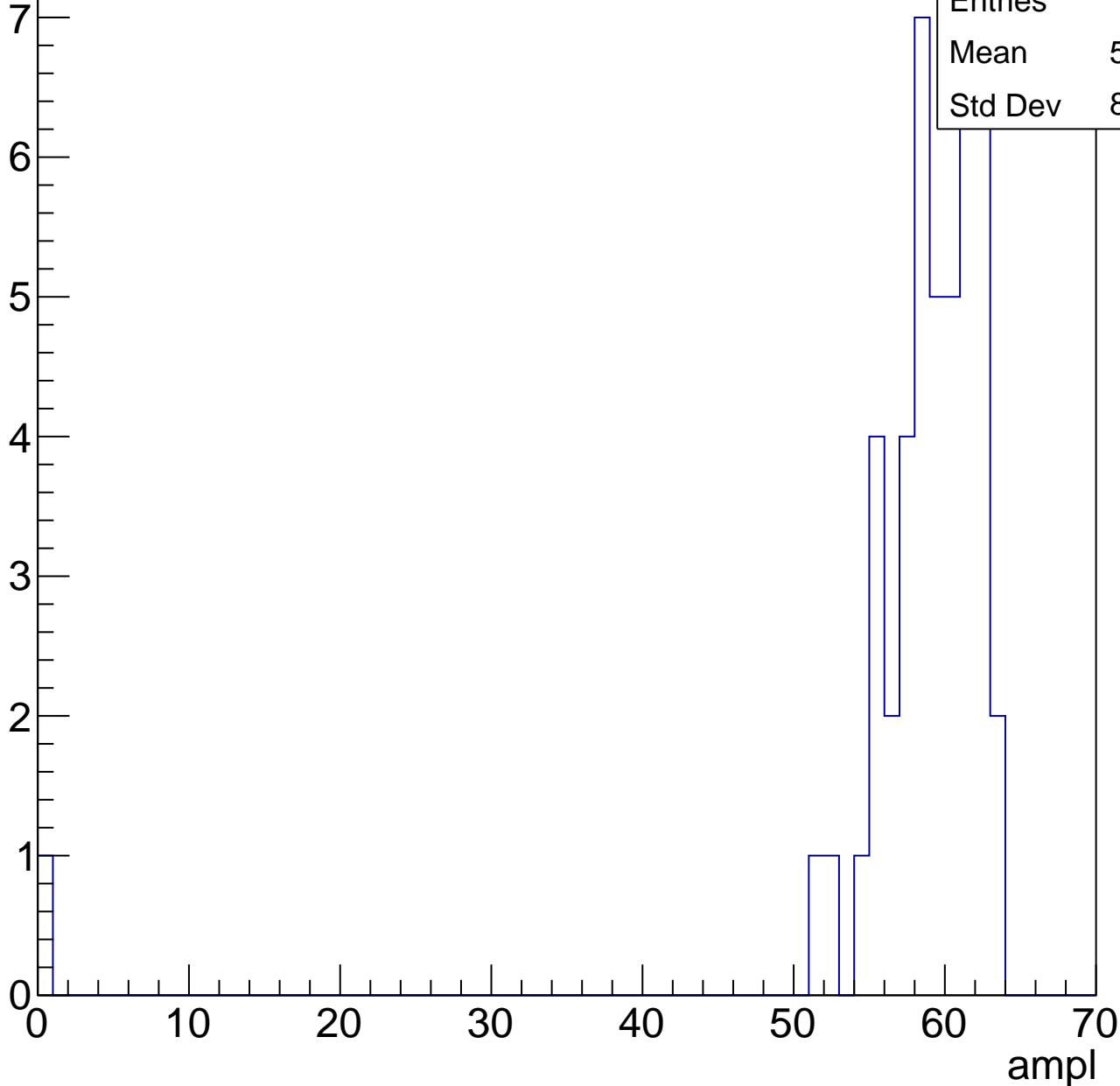


B1L103S, U12-ch73, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

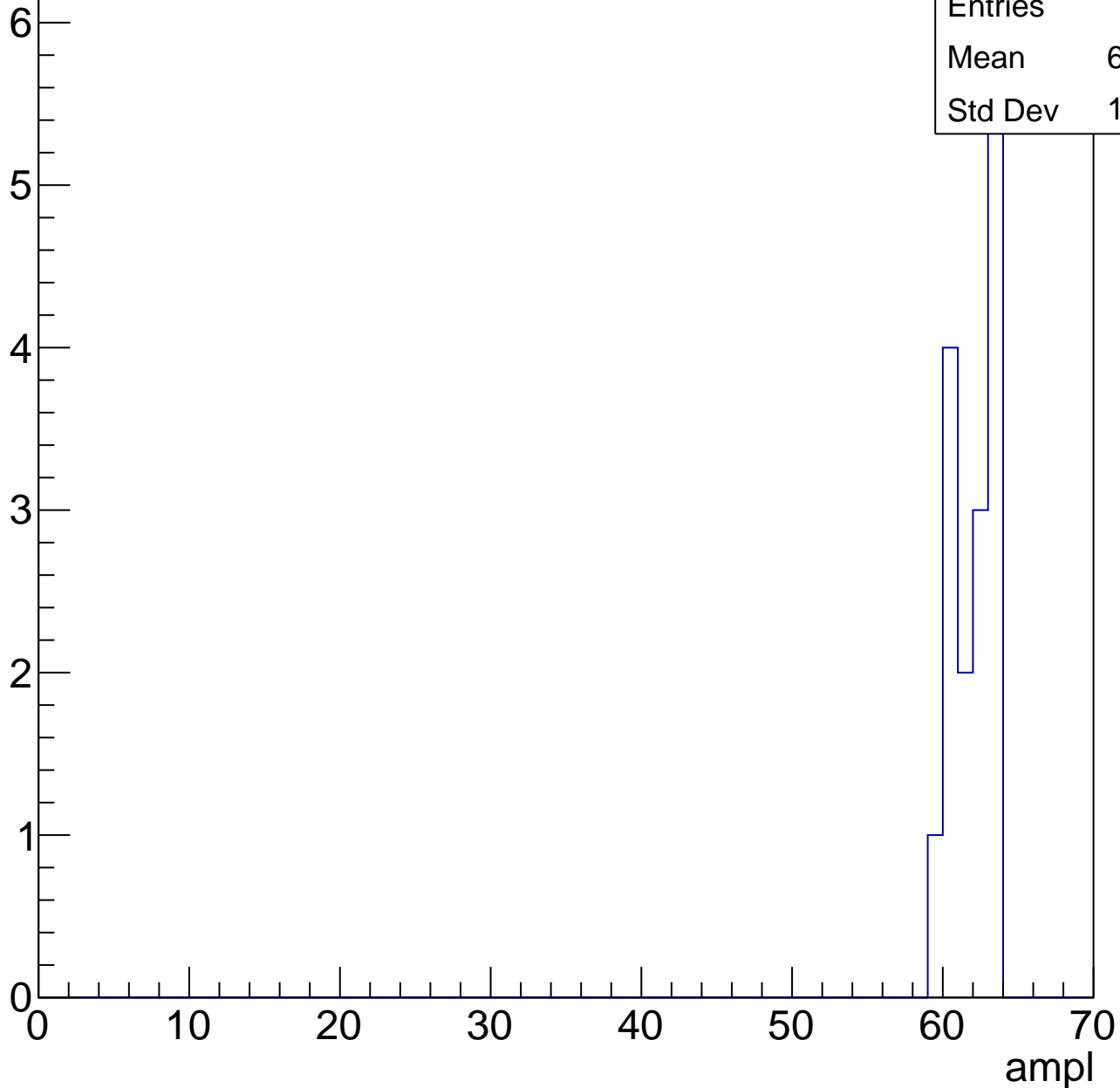
Entries	47
Mean	57.55
Std Dev	8.937



B1L103S, U12-ch73, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

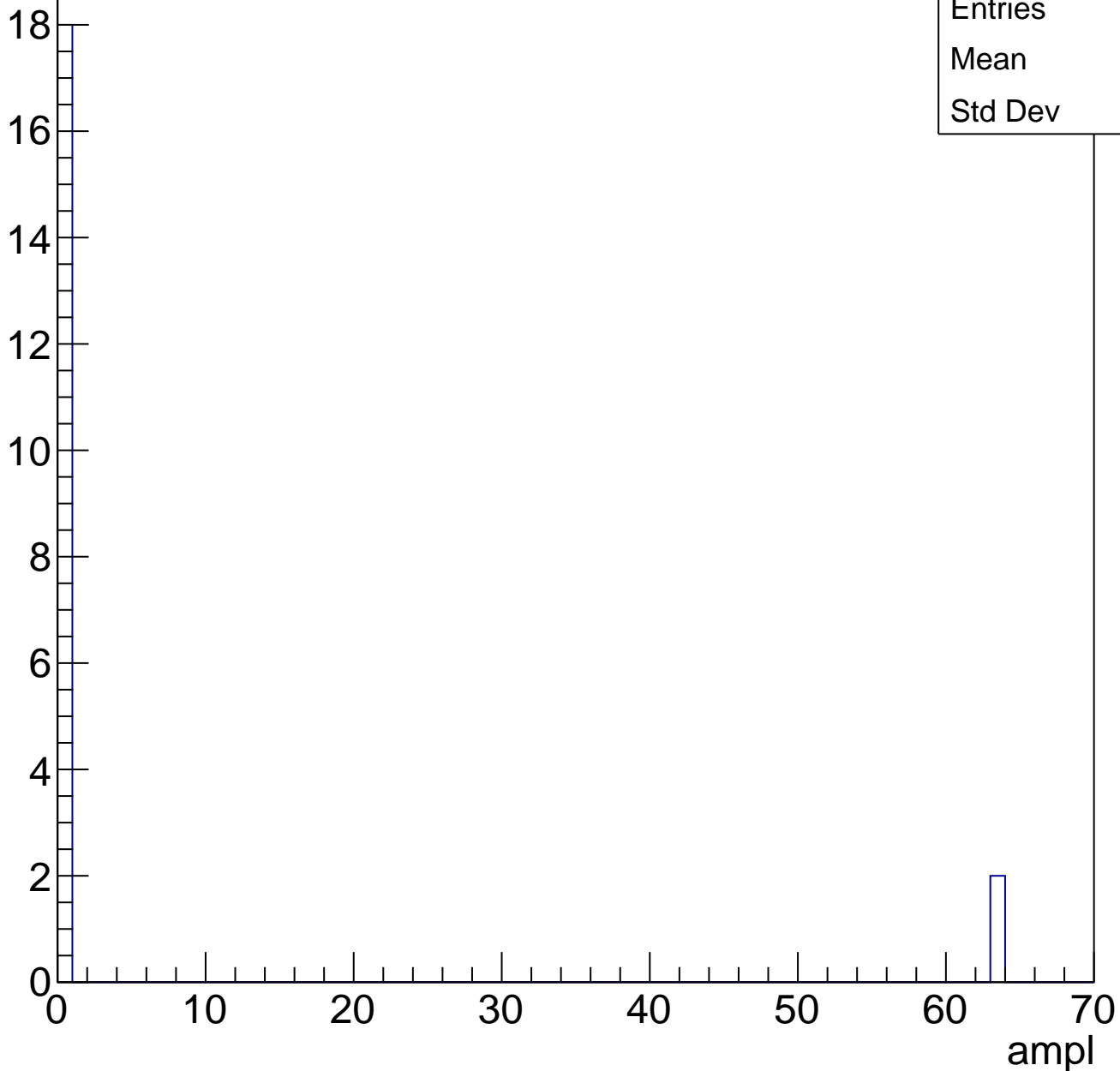


B1L103S, U12-ch73, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	6.3
Std Dev	18.9

Entry

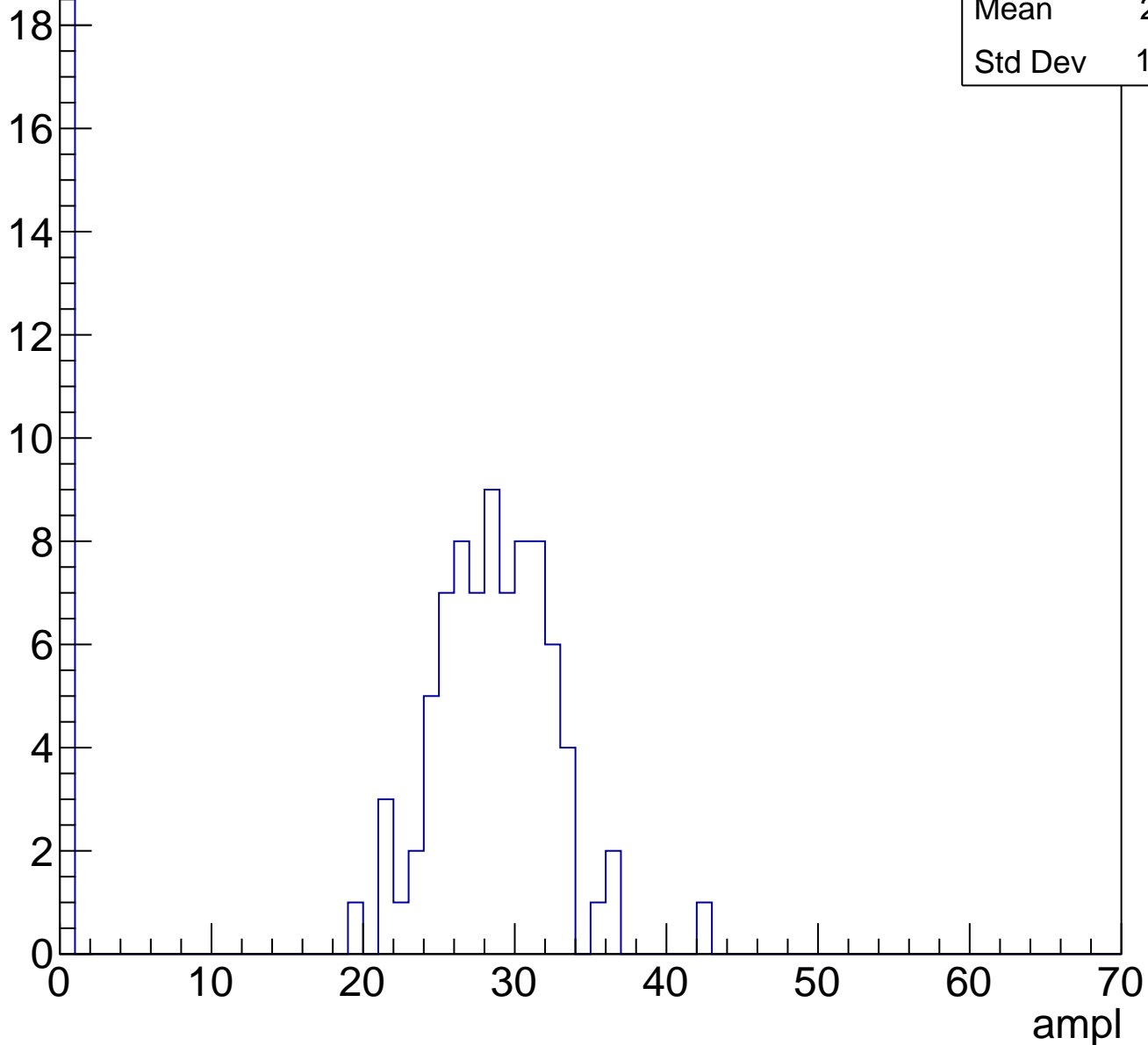


B1L103S, U12-ch74, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	99
Mean	22.81
Std Dev	11.64

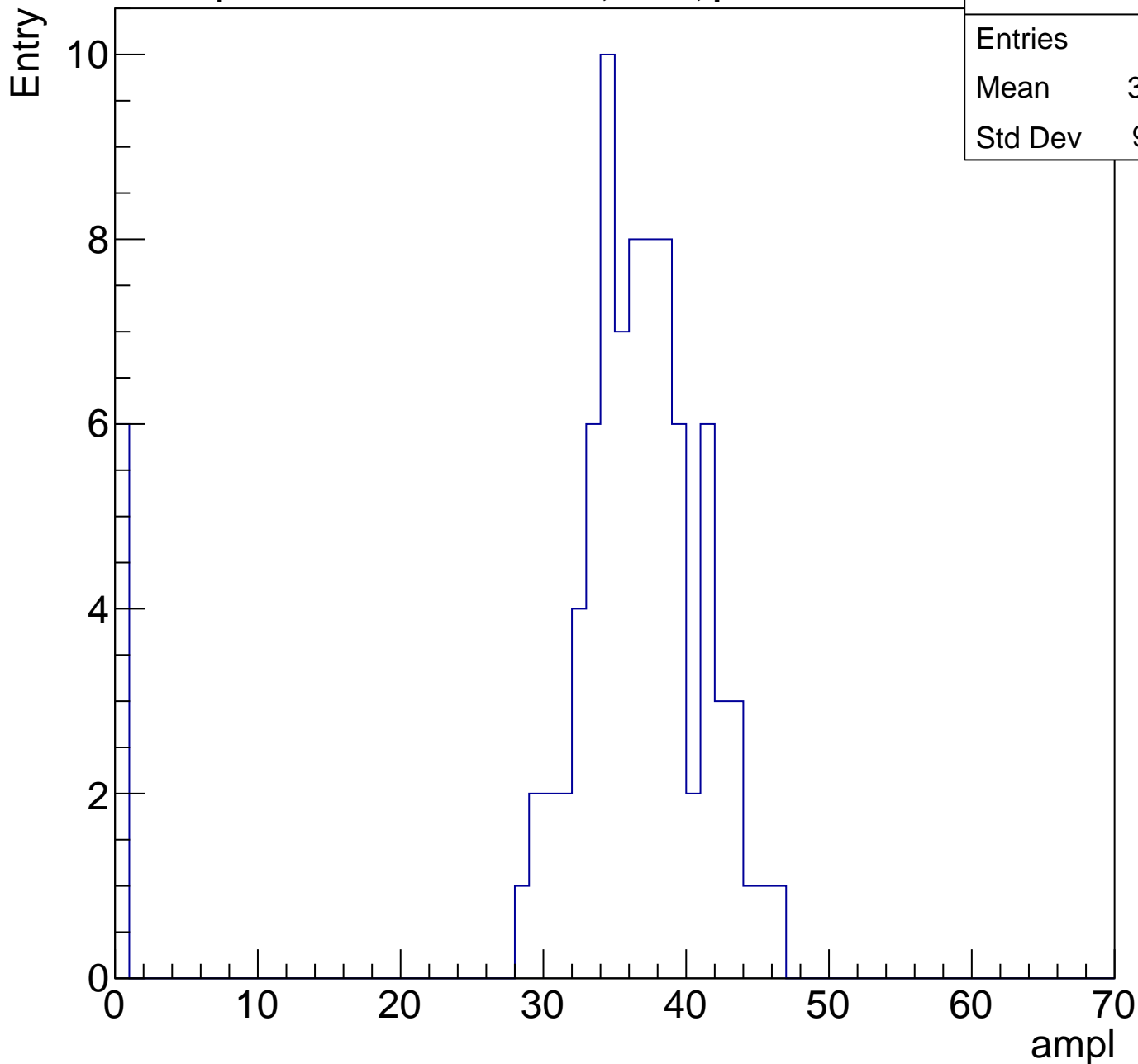
Entry



B1L103S, U12-ch74, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	87
Mean	33.99
Std Dev	9.971



B1L103S, U12-ch74, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	54
Mean	33.57
Std Dev	17.25

Entry

10

8

6

4

2

0

0

10

20

30

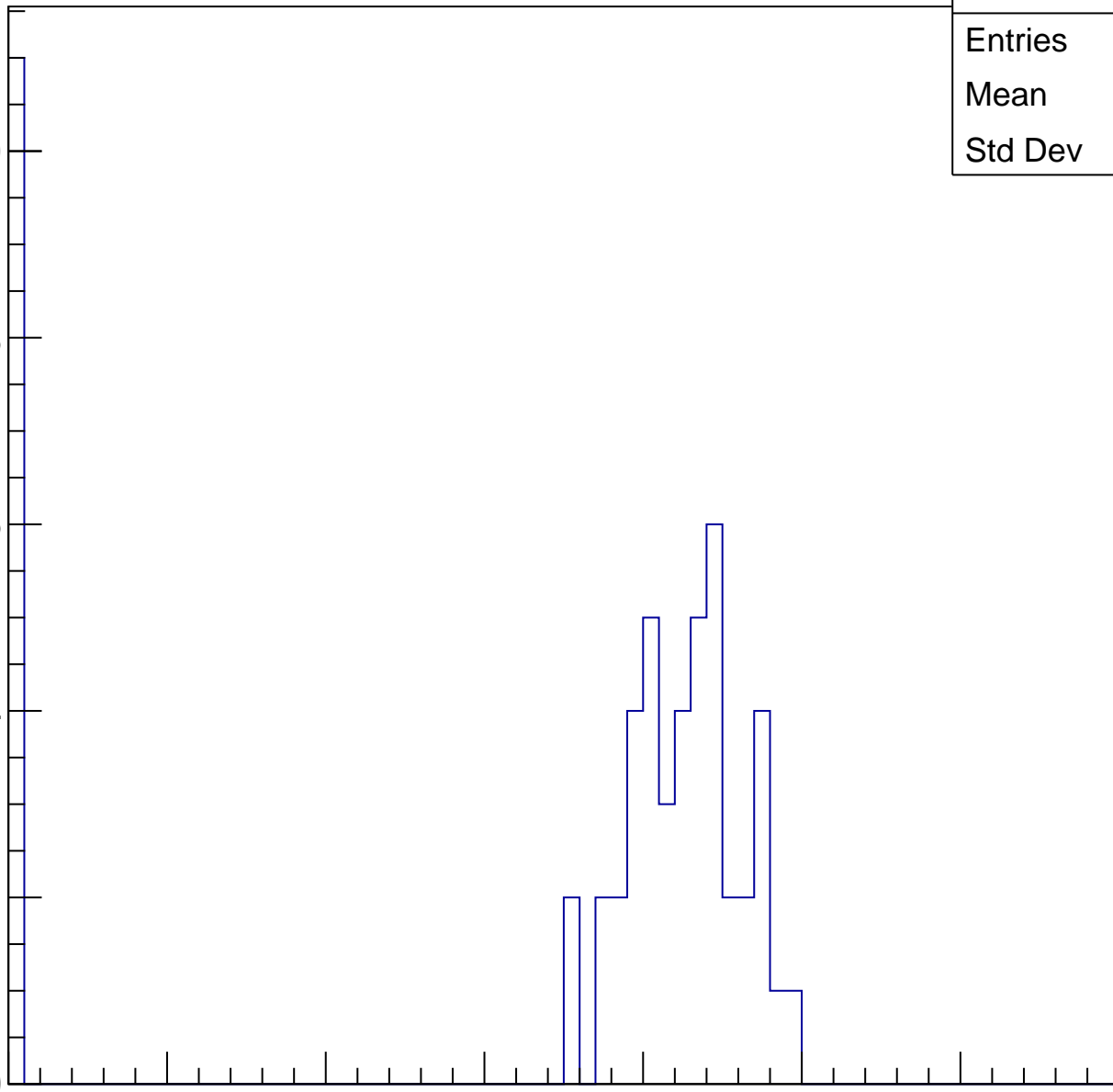
40

50

60

70

ampl

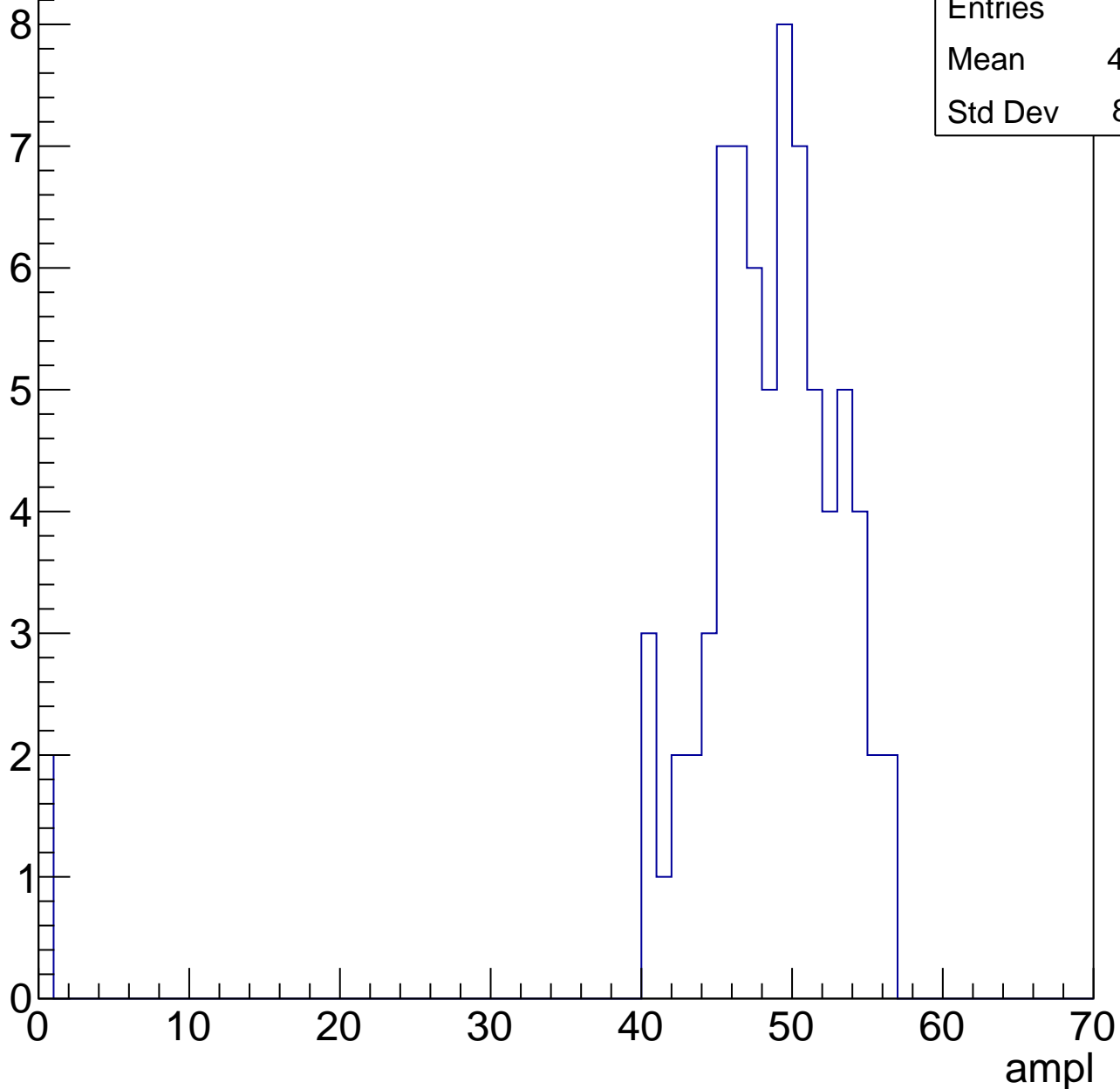


B1L103S, U12-ch74, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	75
Mean	47.07
Std Dev	8.711

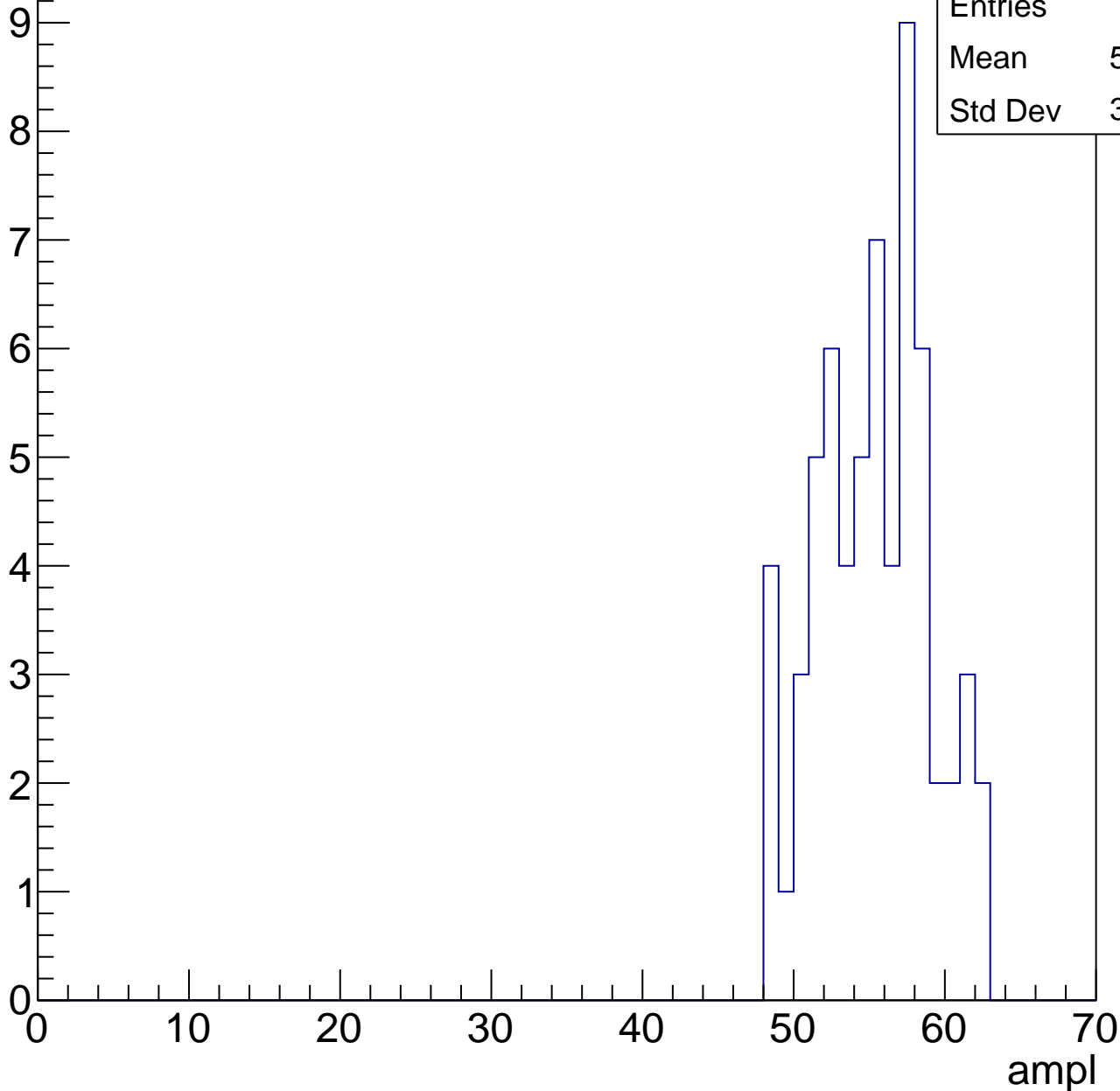


B1L103S, U12-ch74, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	63
Mean	54.84
Std Dev	3.657

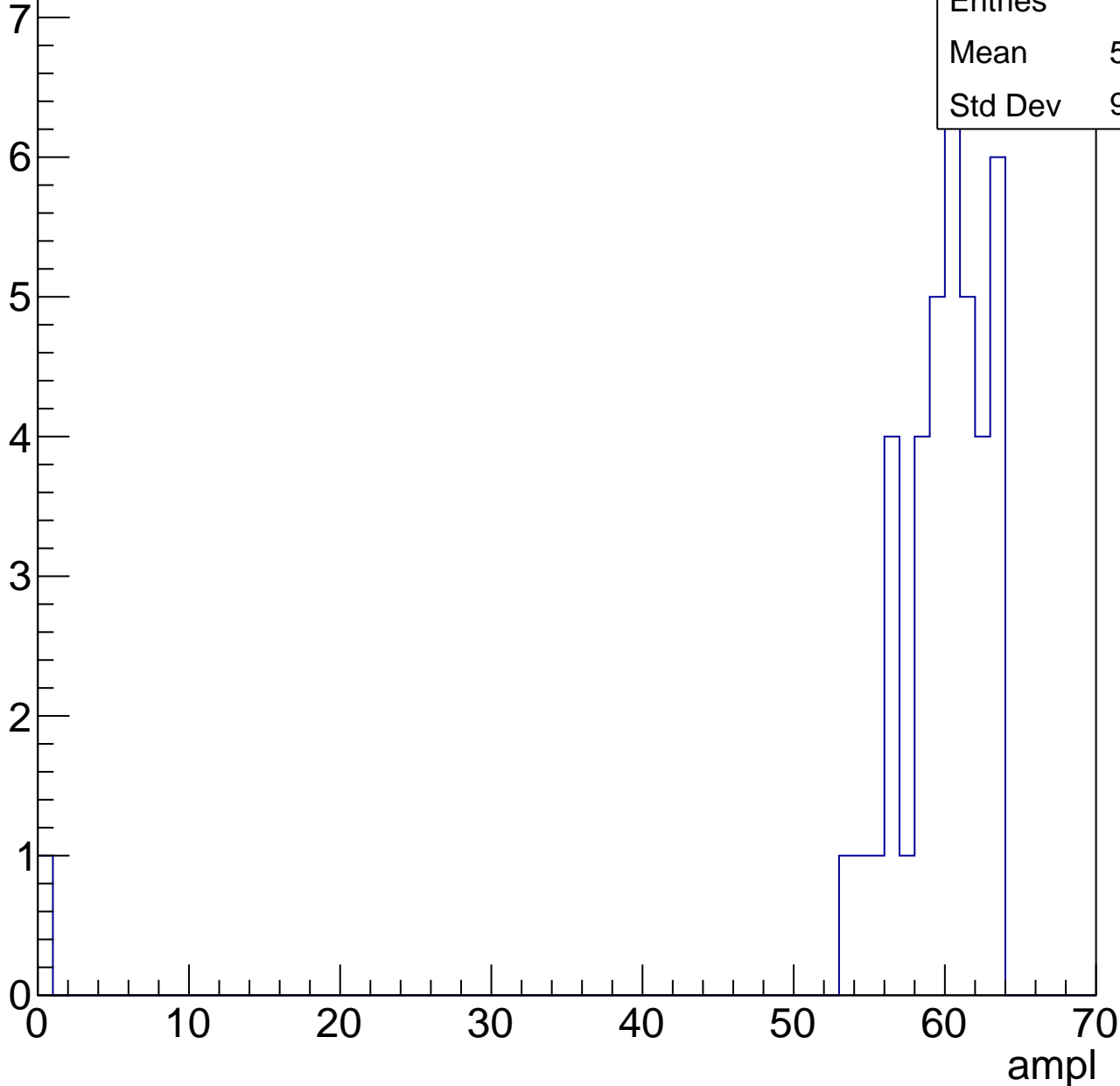


B1L103S, U12-ch74, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

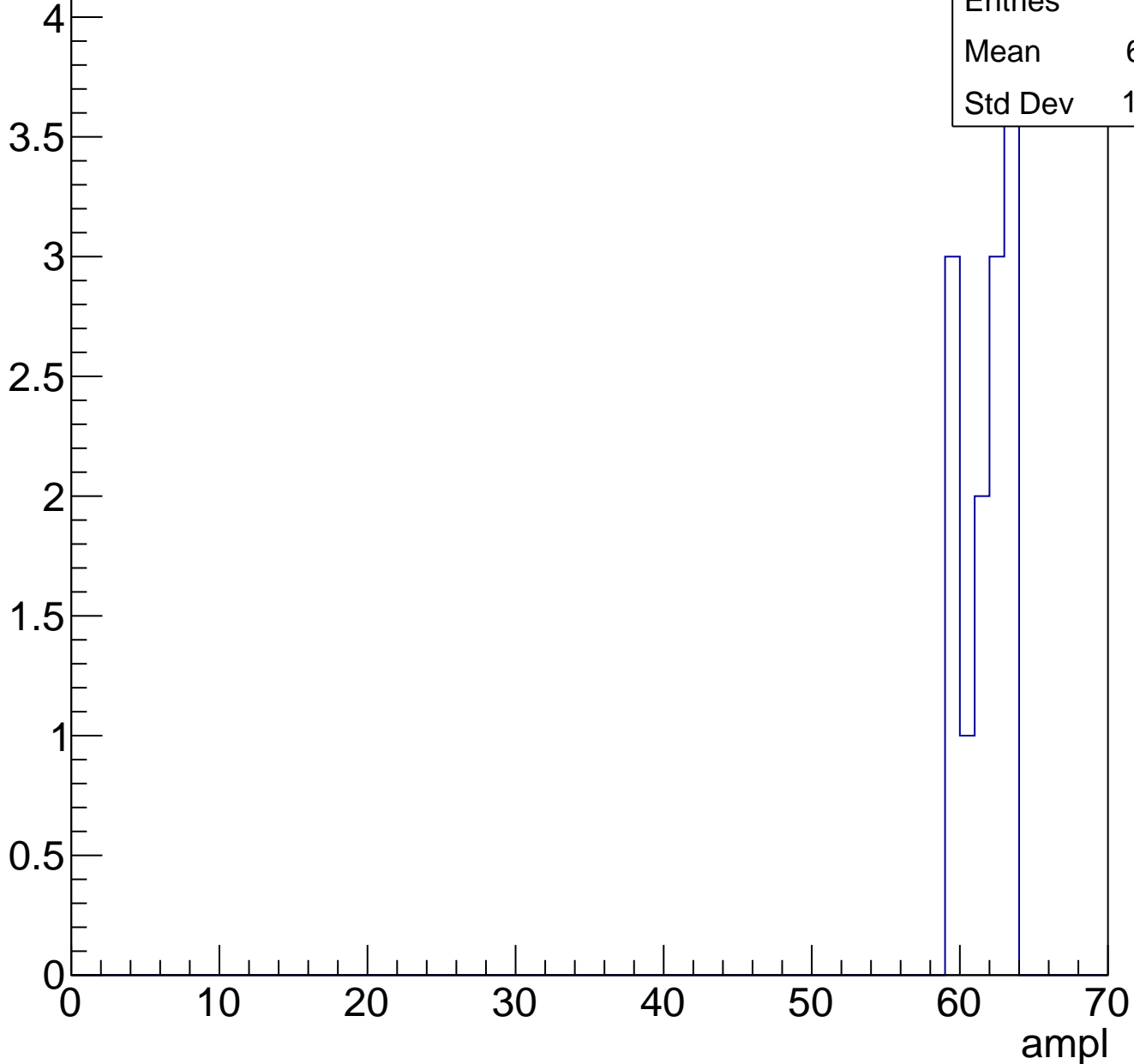
Entries	40
Mean	58.02
Std Dev	9.648



B1L103S, U12-ch74, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

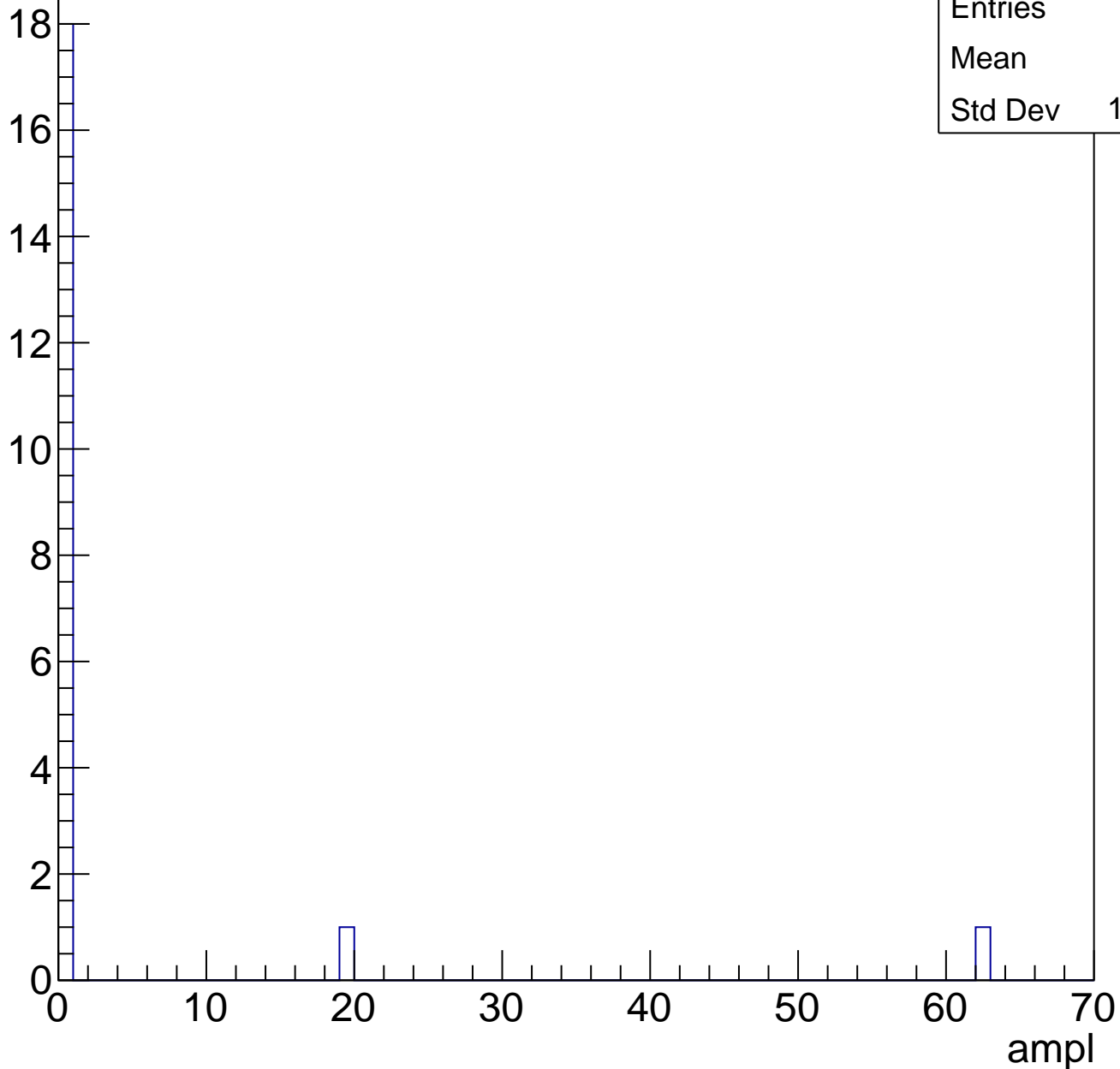


B1L103S, U12-ch74, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	4.05
Std Dev	13.92

Entry



B1L103S, U12-ch75, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	84
Mean	26.54
Std Dev	10.24

Entry

10
8
6
4
2
0

ampl

0

10

20

30

40

50

60

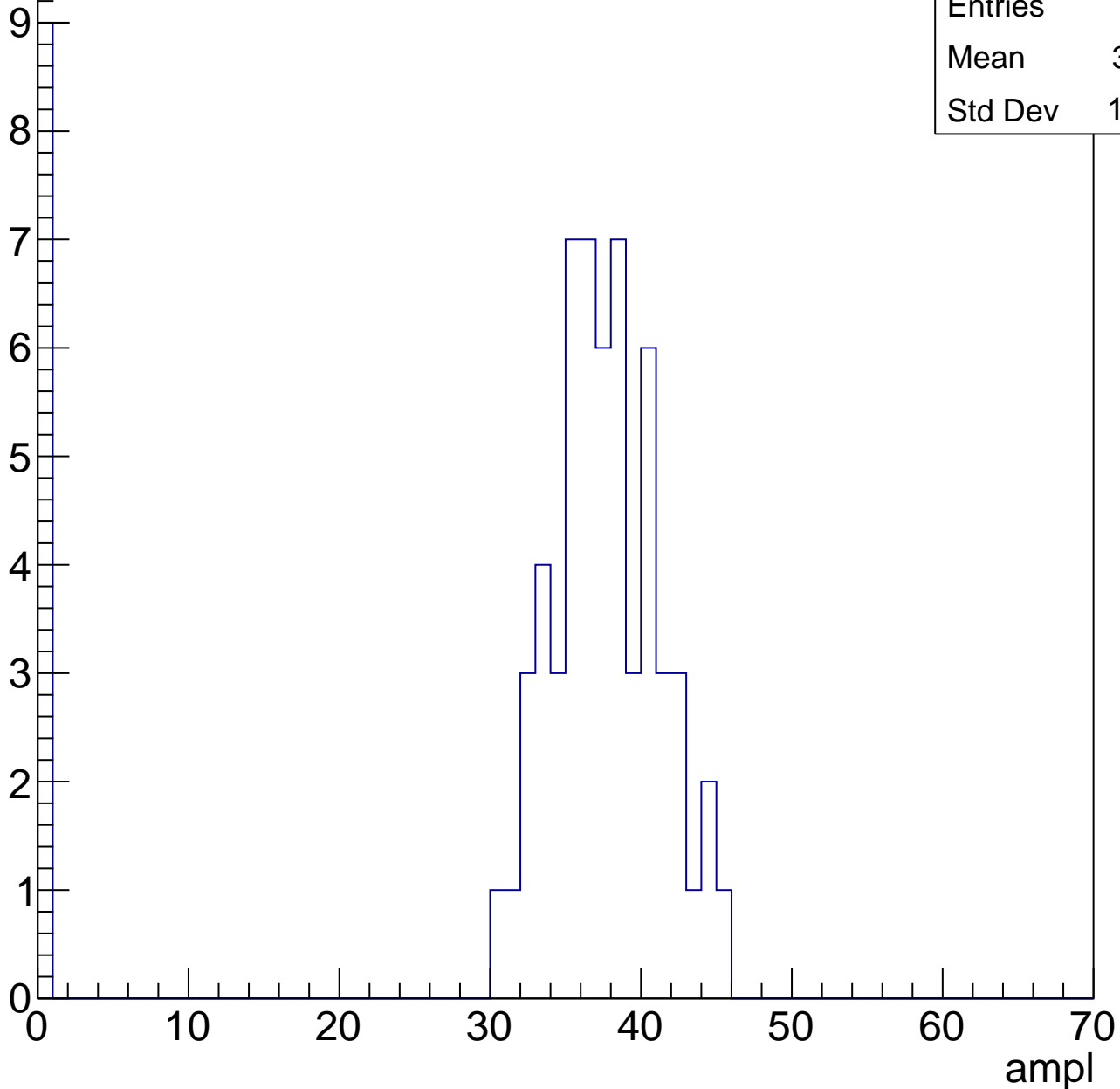
70

B1L103S, U12-ch75, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	32.21
Std Dev	13.08

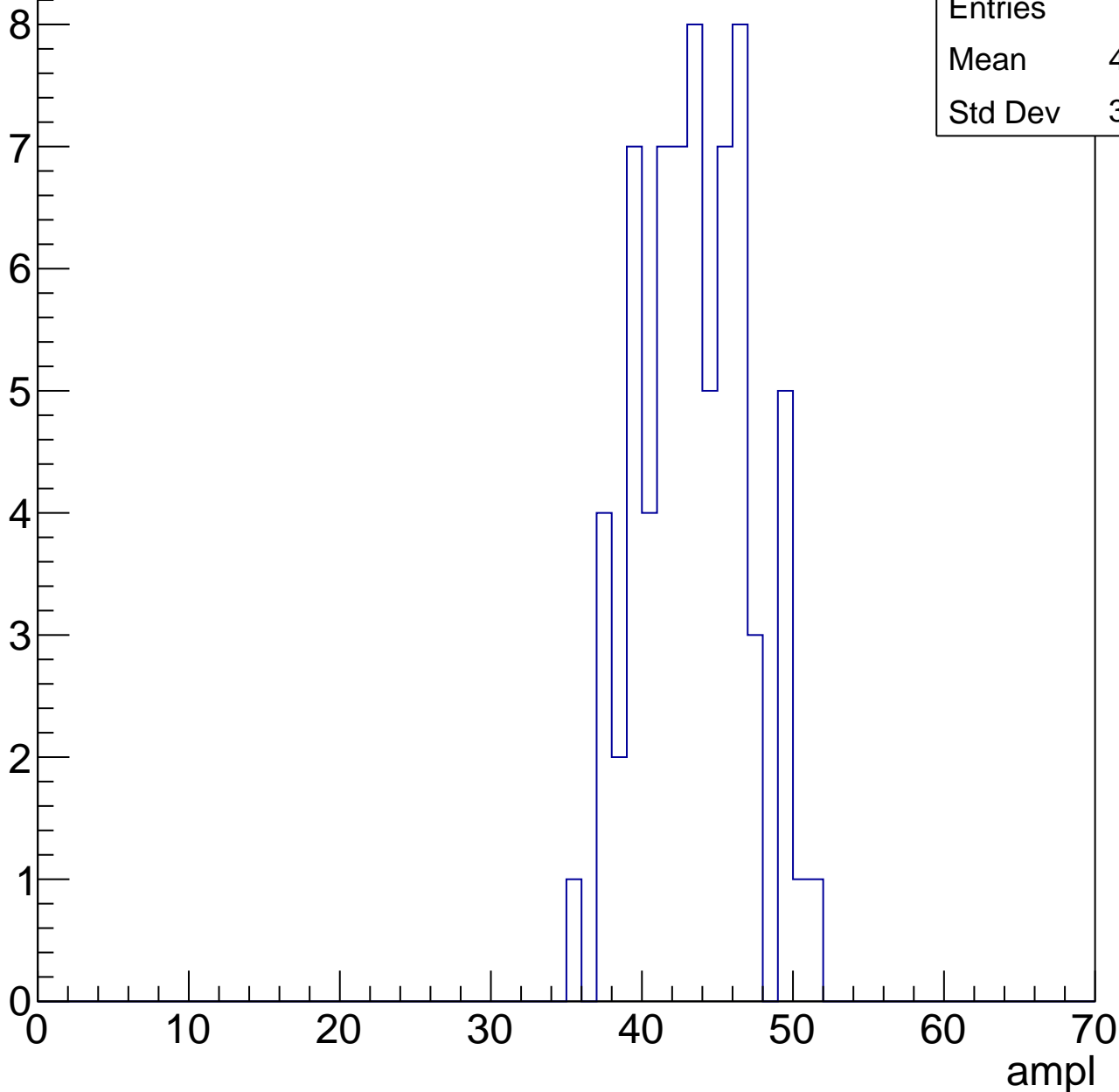


B1L103S, U12-ch75, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	42.96
Std Dev	3.559

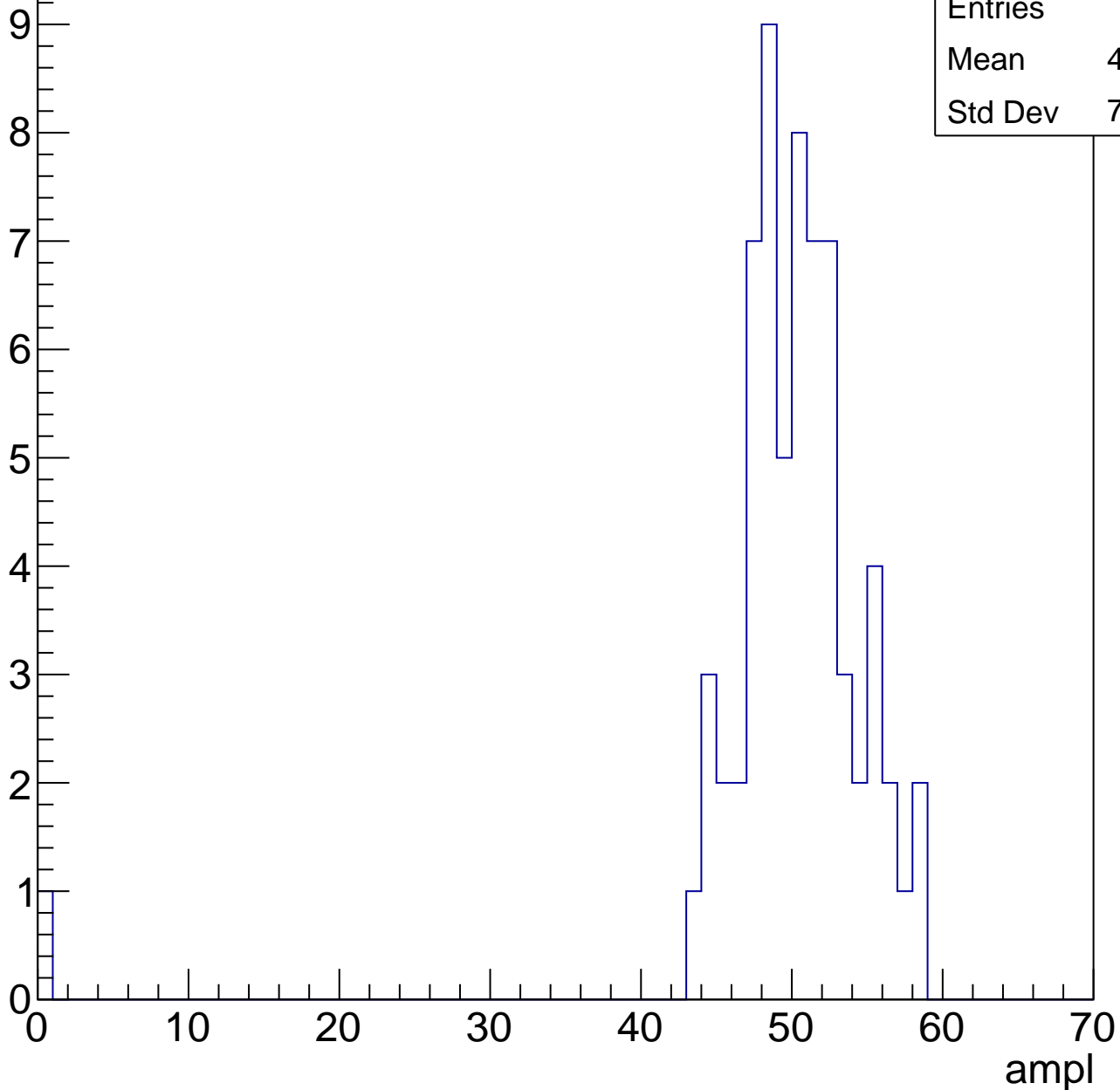


B1L103S, U12-ch75, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	49.33
Std Dev	7.024

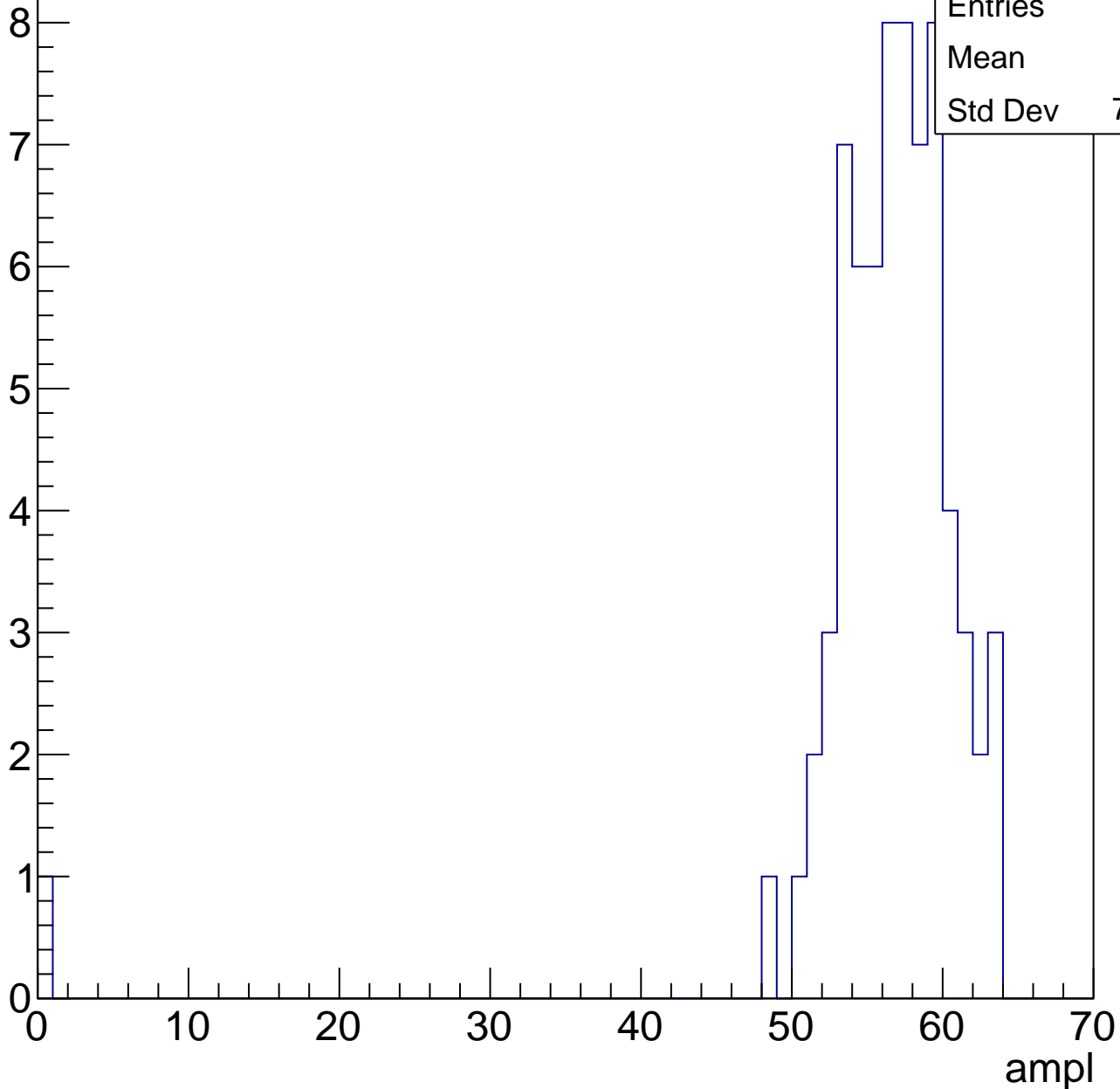


B1L103S, U12-ch75, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	55.7
Std Dev	7.451

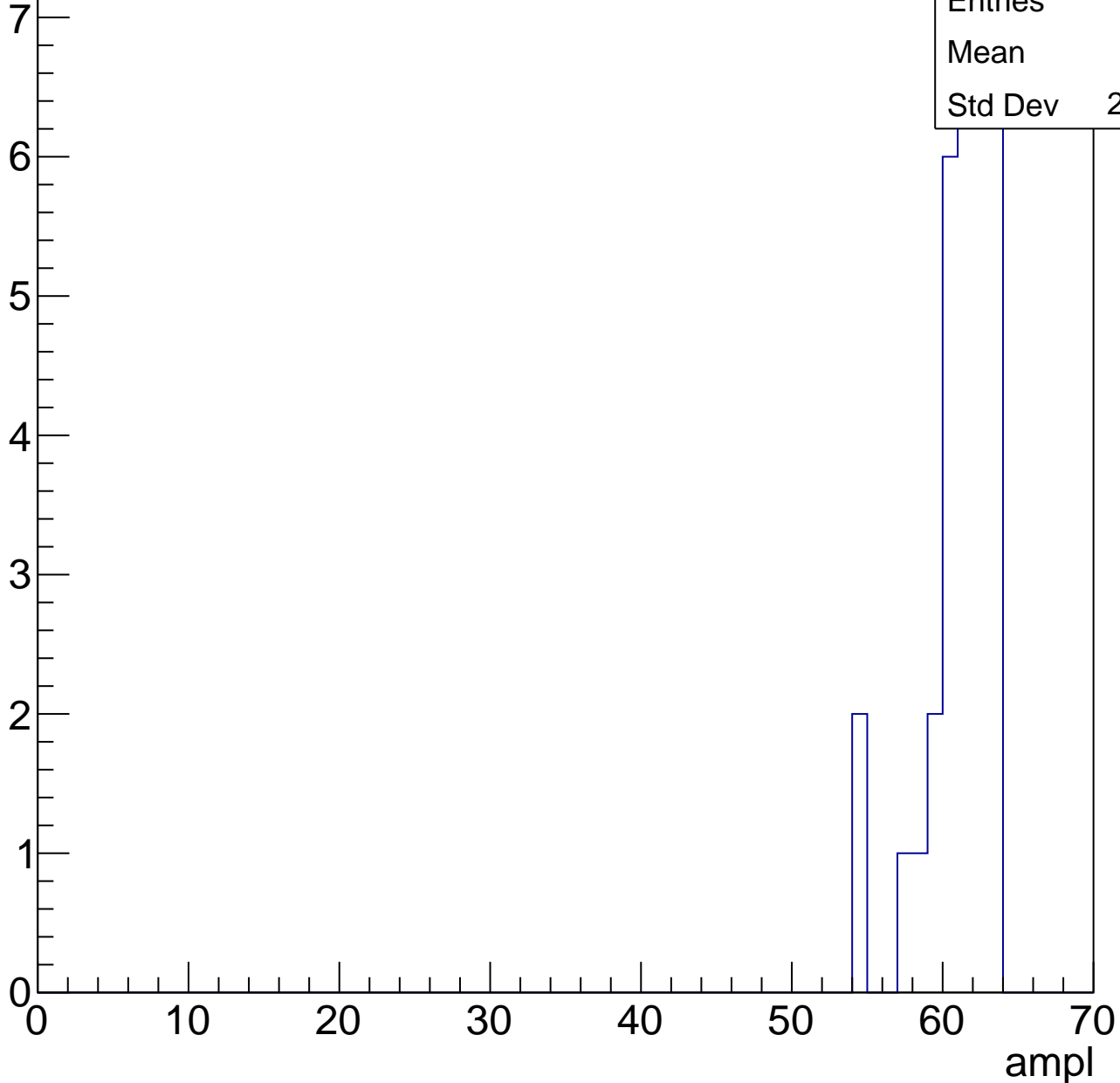


B1L103S, U12-ch75, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	33
Mean	60.7
Std Dev	2.263



B1L103S, U12-ch75, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch75, adc7

calib_packv5_041523_1651.root, FC#0, port C2

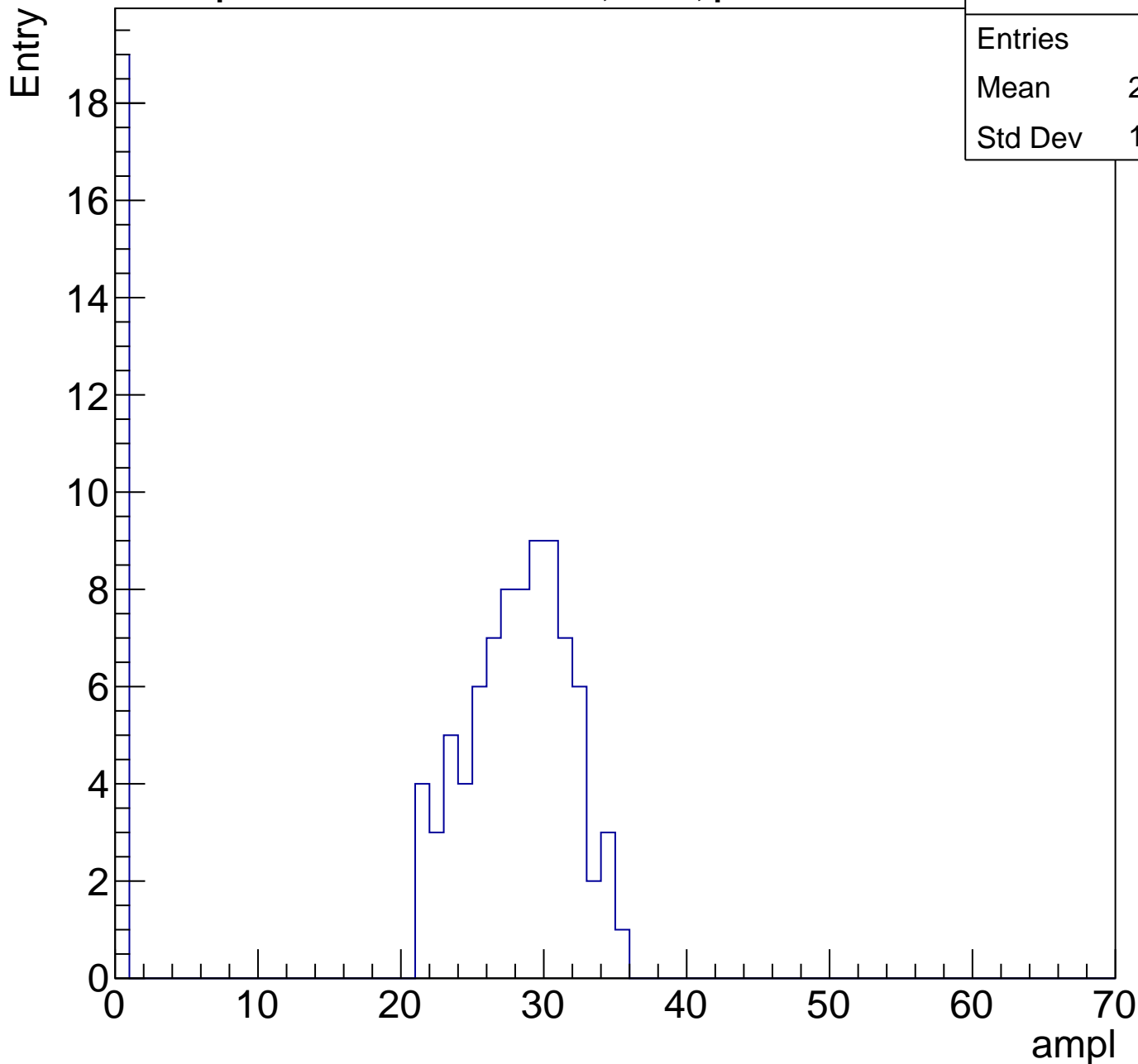
Entry



B1L103S, U12-ch76, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	101
Mean	22.53
Std Dev	11.29

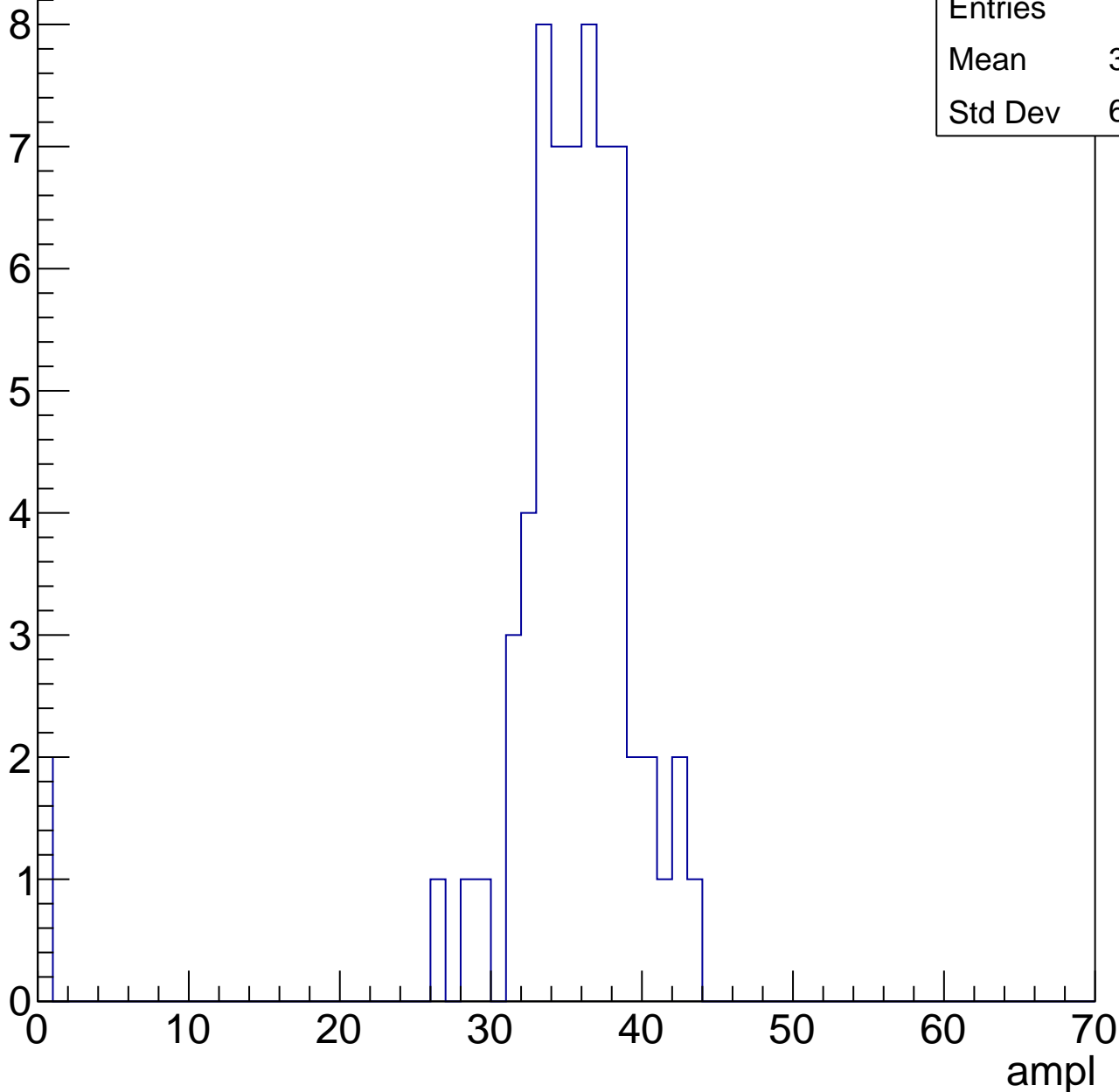


B1L103S, U12-ch76, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	34.22
Std Dev	6.936



B1L103S, U12-ch76, adc2

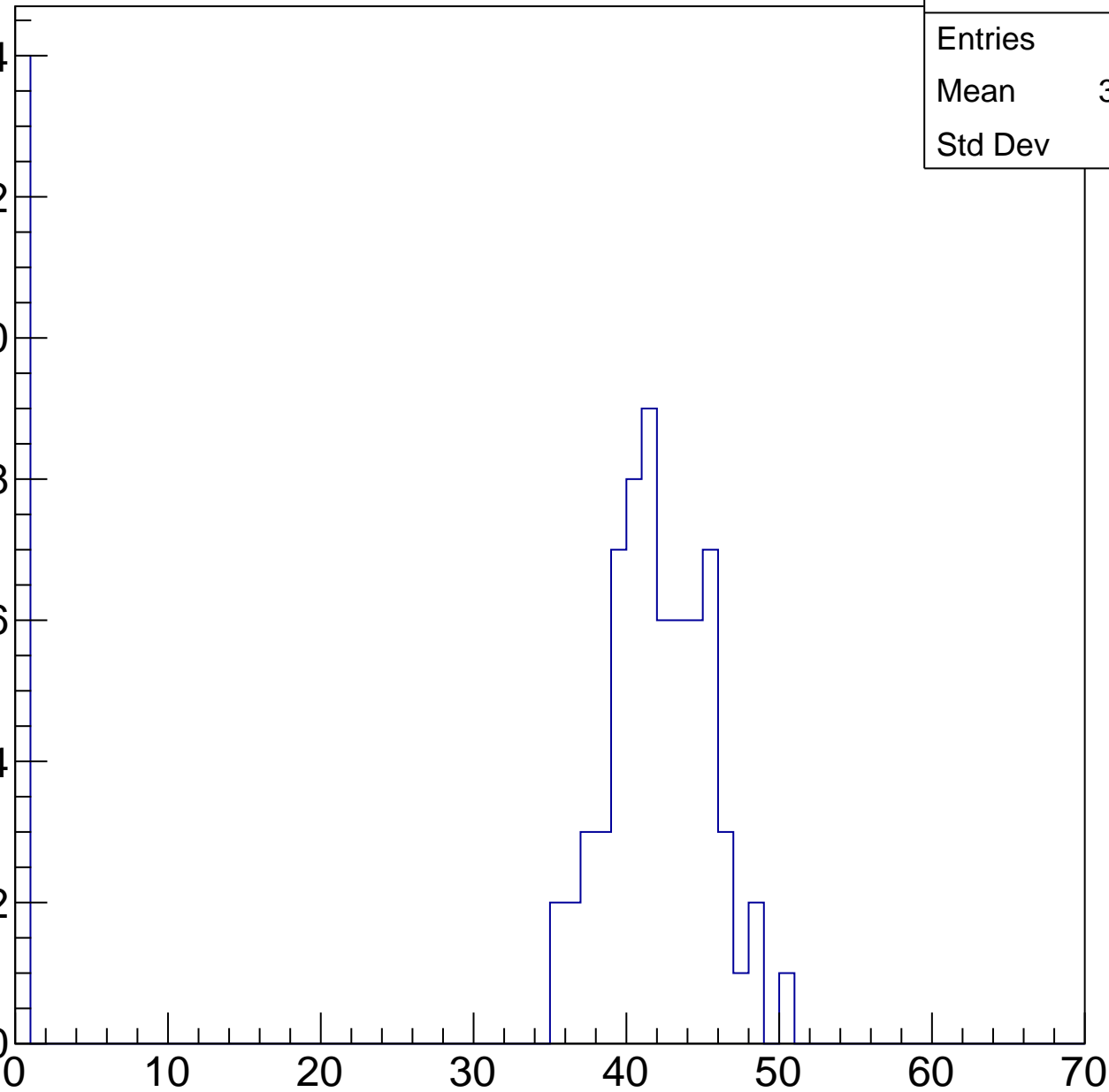
calib_packv5_041523_1651.root, FC#0, port C2

Entries	80
Mean	34.36
Std Dev	16.1

Entry

14
12
10
8
6
4
2
0

ampl

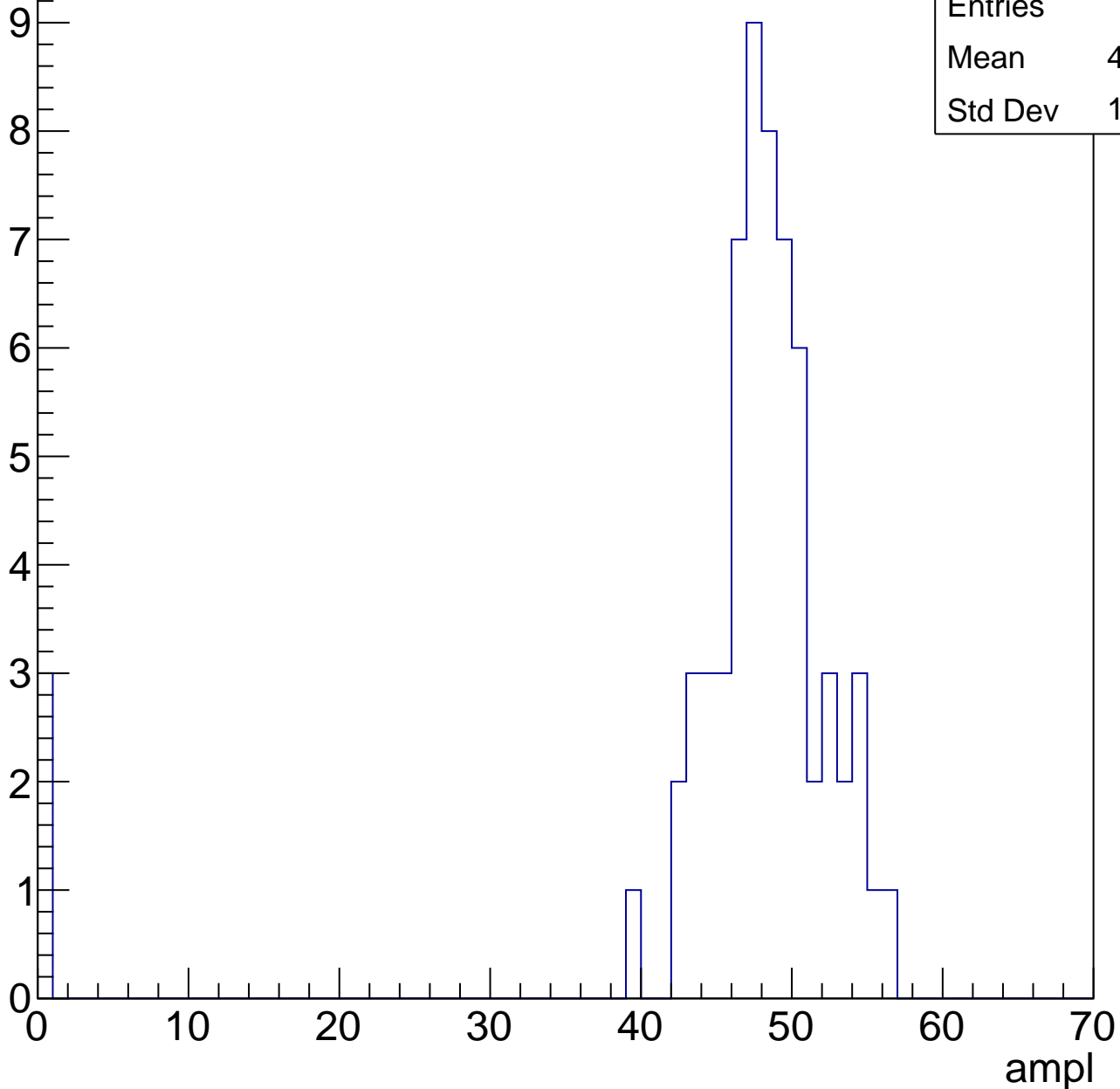


B1L103S, U12-ch76, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	45.75
Std Dev	10.68

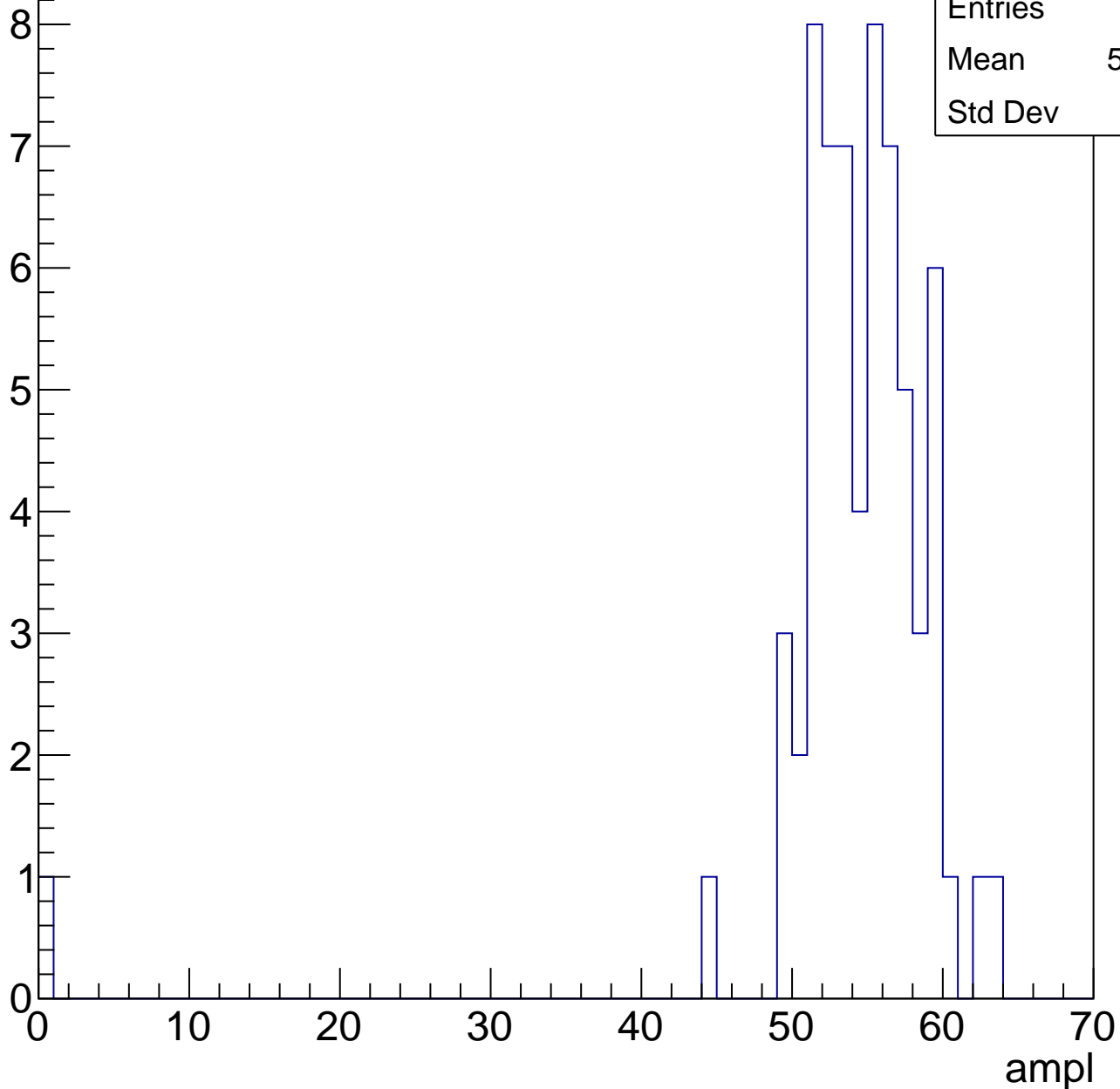


B1L103S, U12-ch76, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

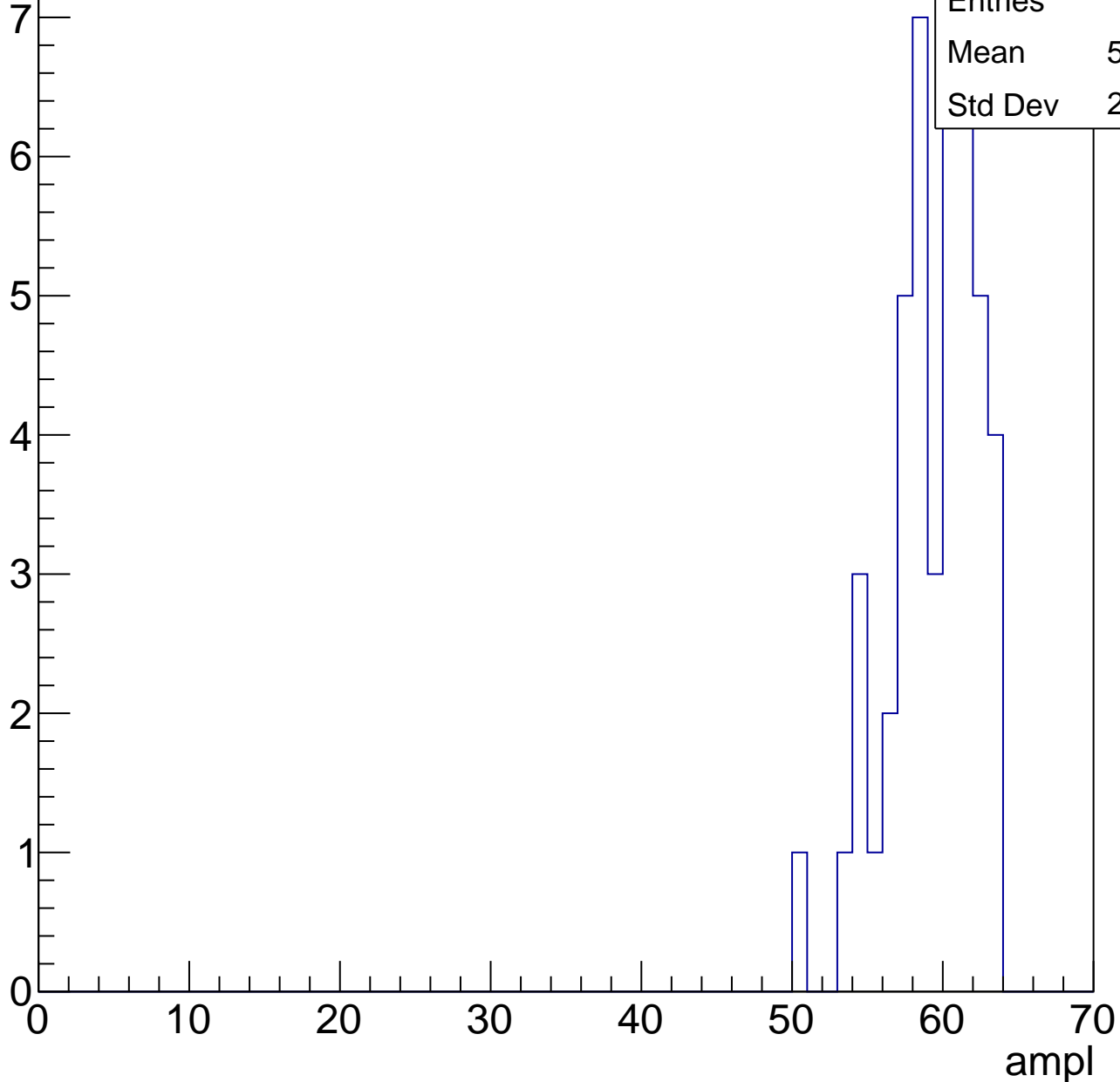
Entries	65
Mean	53.54
Std Dev	7.52



B1L103S, U12-ch76, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch76, adc6

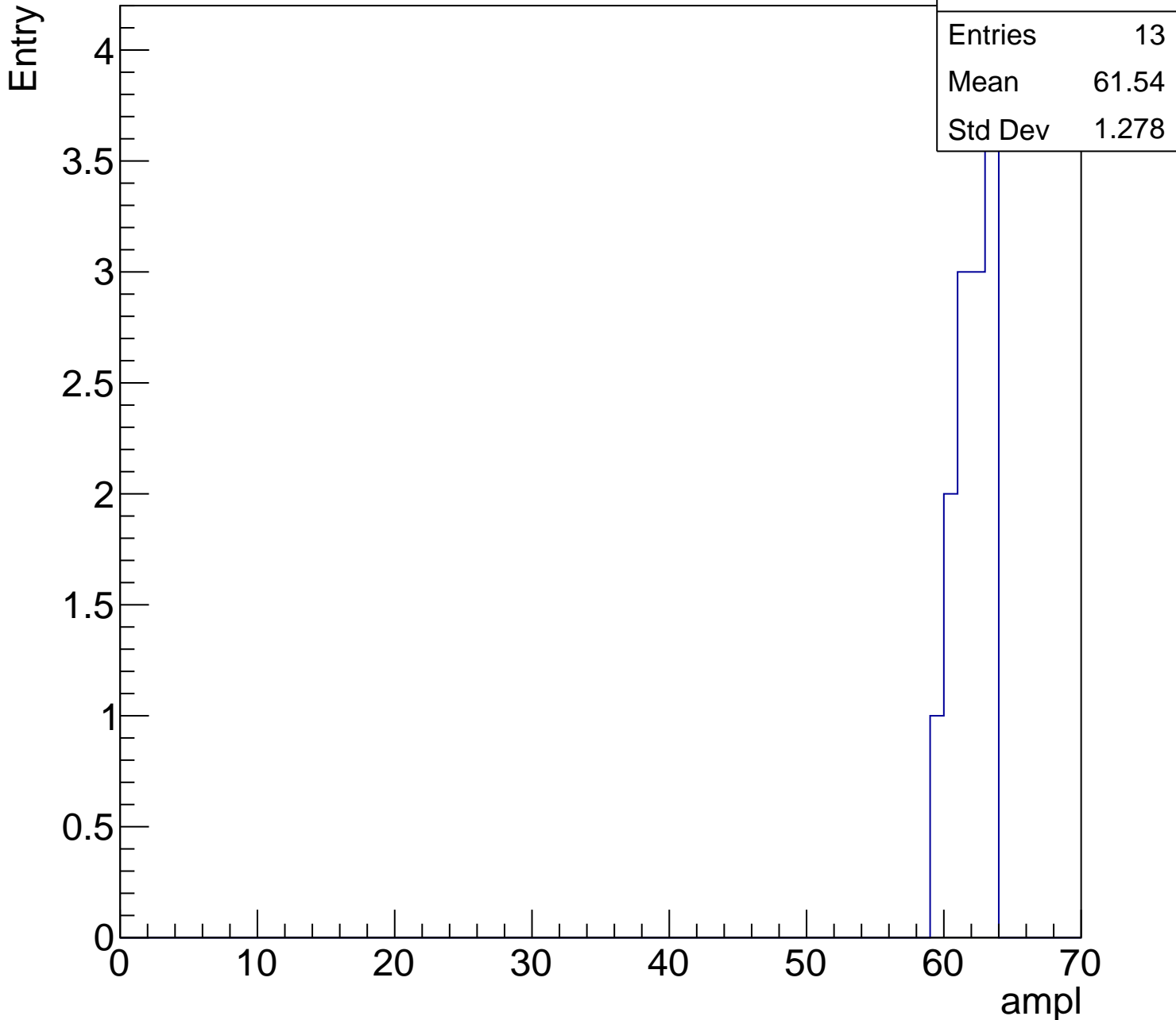
calib_packv5_041523_1651.root, FC#0, port C2

Entry

4
3.5
3
2.5
2
1.5
1
0.5
0

Entries	13
Mean	61.54
Std Dev	1.278

ampl



B1L103S, U12-ch76, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	21
Mean	5.952
Std Dev	18.35

Entry



B1L103S, U12-ch77, adc0

calib_packv5_041523_1651.root, FC#0, port C2

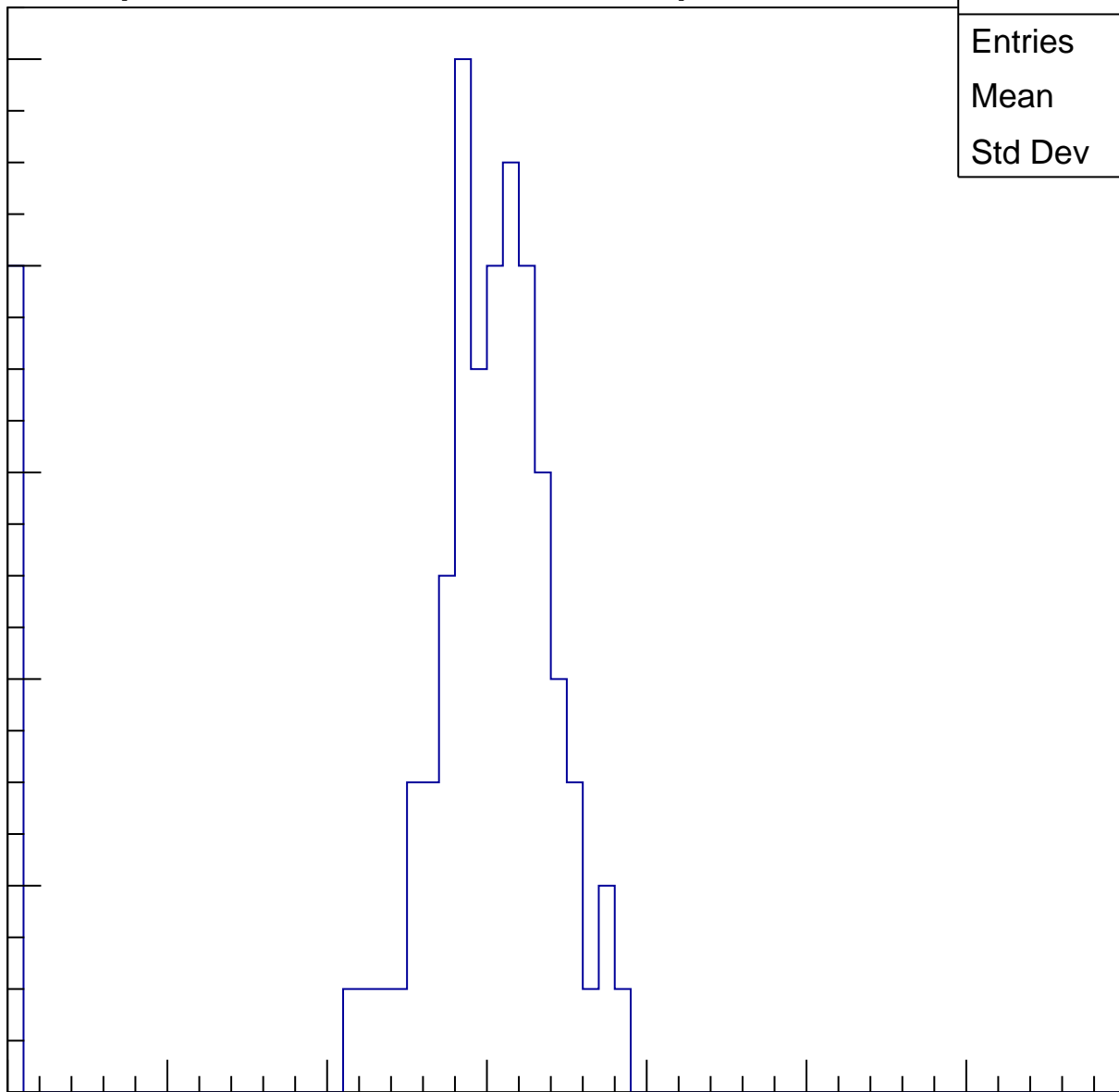
Entries	82
Mean	27.11
Std Dev	9.495

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

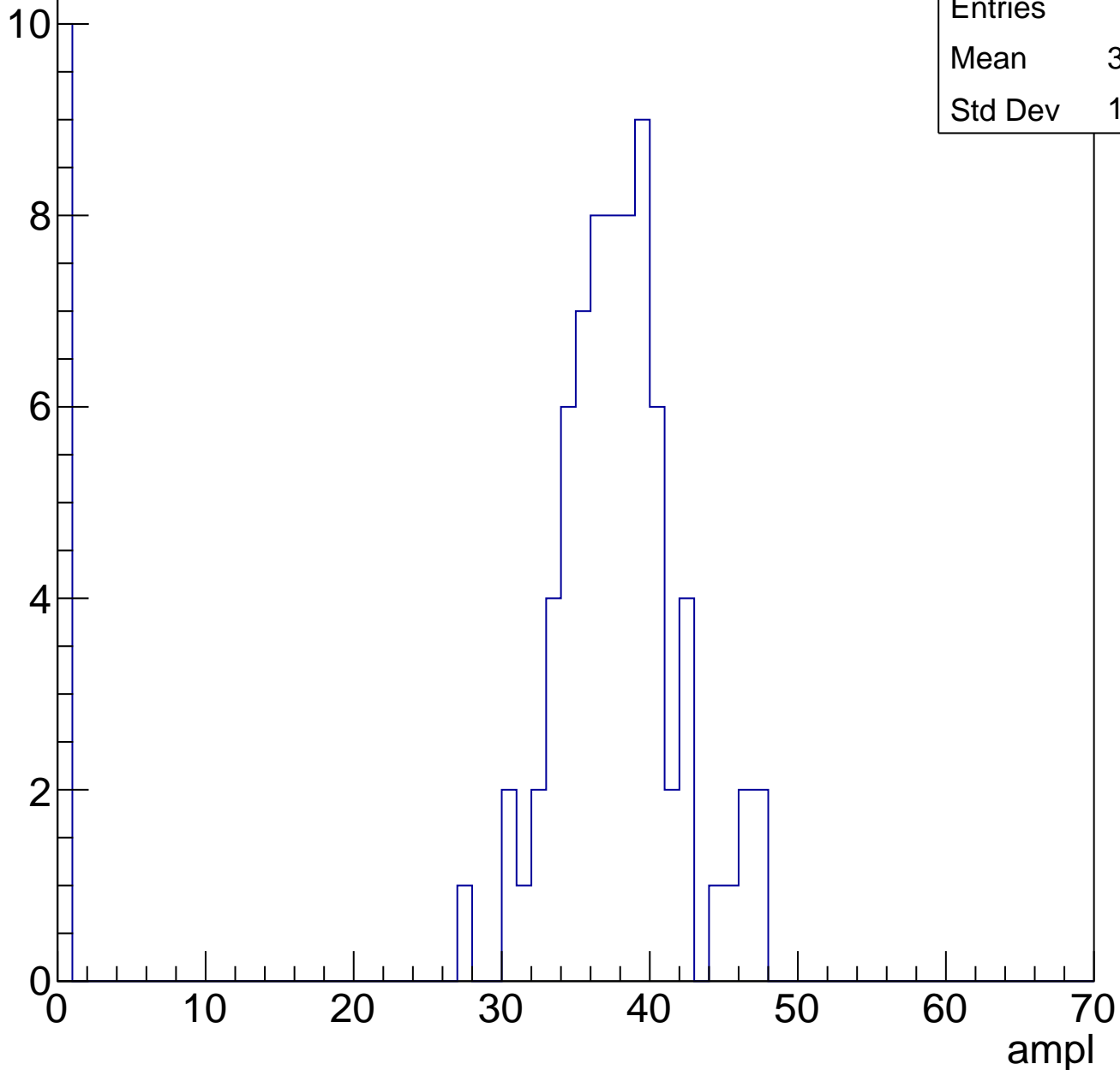


B1L103S, U12-ch77, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	84
Mean	32.94
Std Dev	12.65

Entry

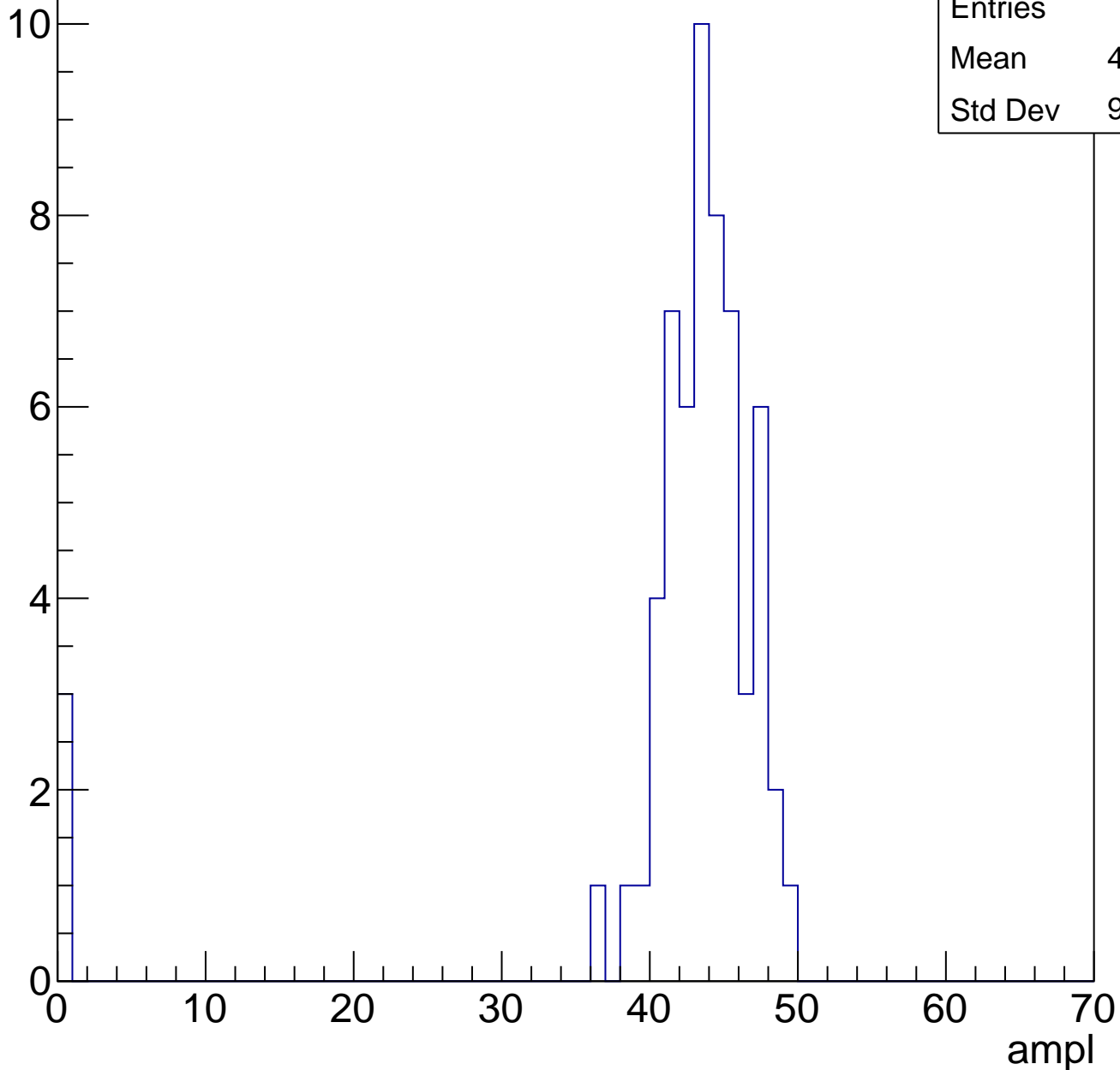


B1L103S, U12-ch77, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	60
Mean	41.23
Std Dev	9.802

Entry

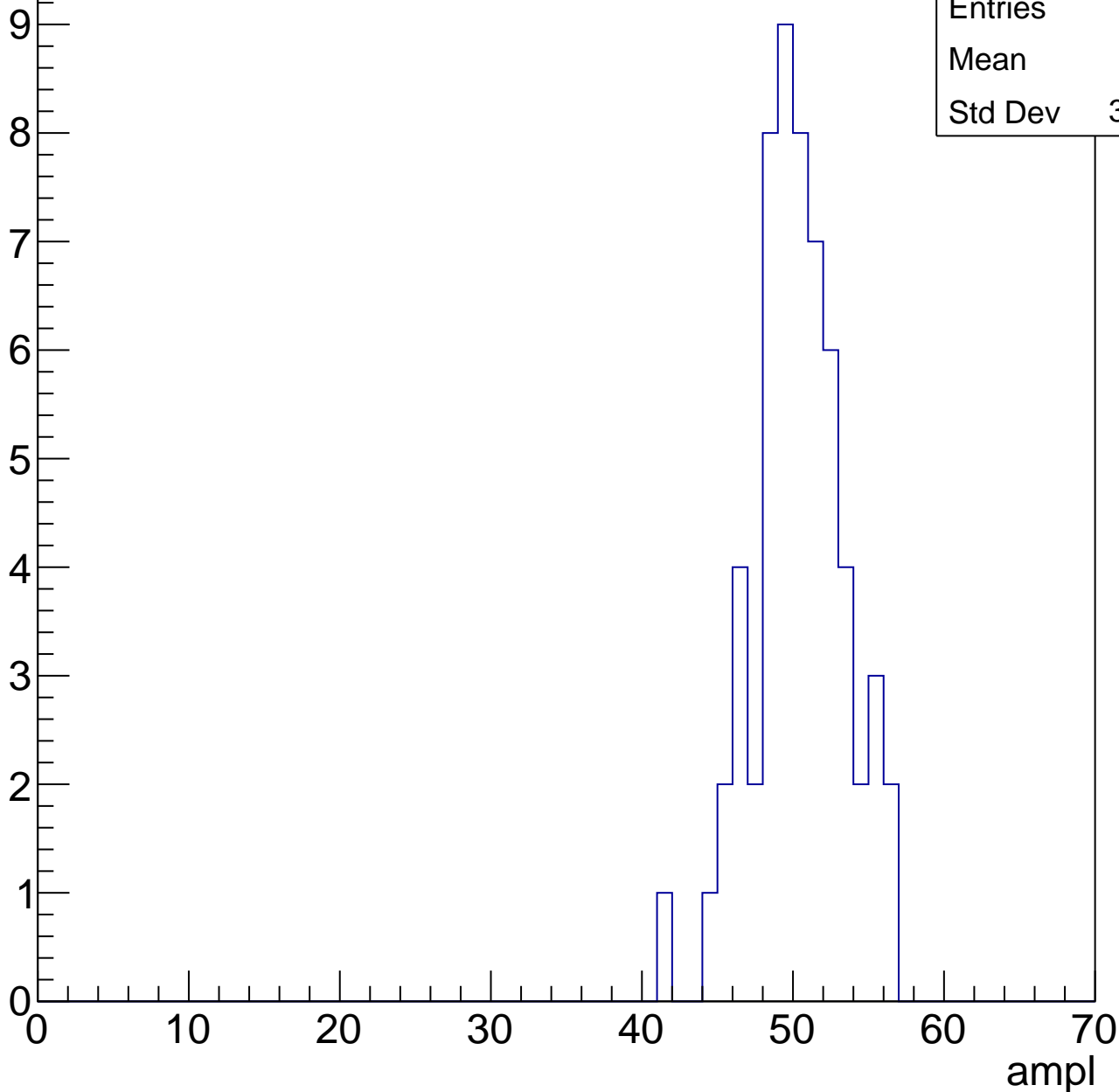


B1L103S, U12-ch77, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	49.9
Std Dev	3.012

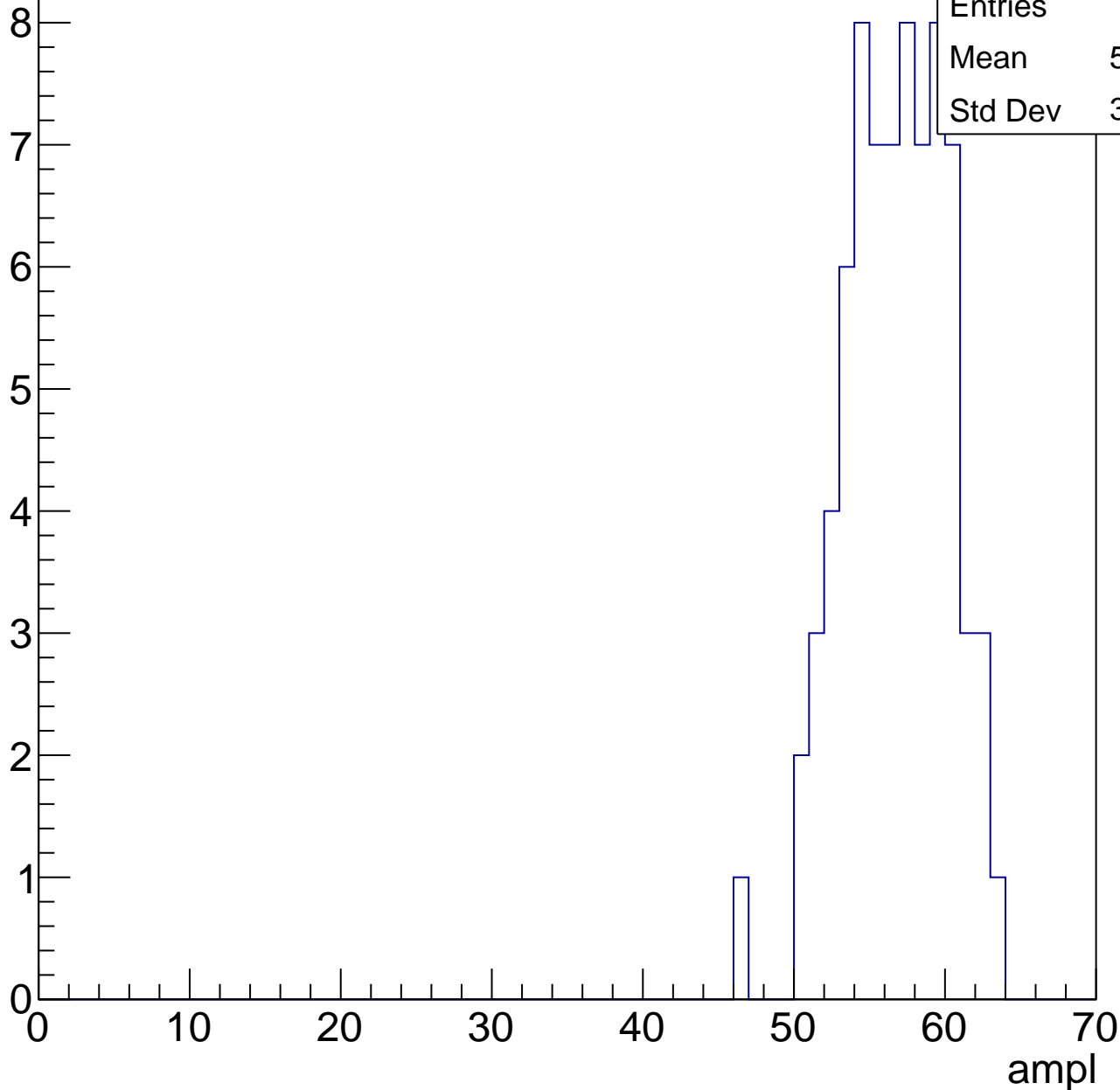


B1L103S, U12-ch77, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	75
Mean	56.27
Std Dev	3.368

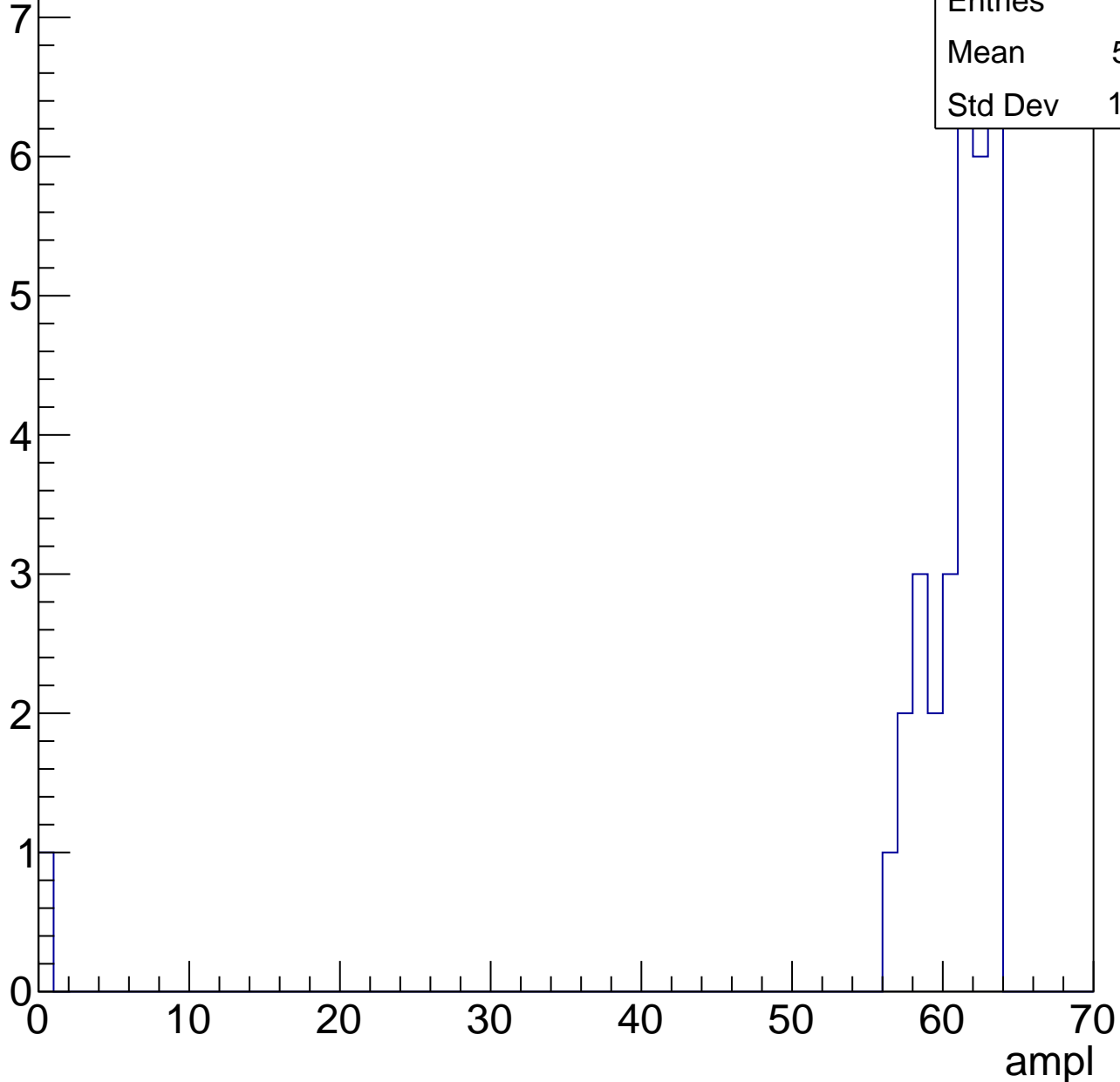


B1L103S, U12-ch77, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	32
Mean	58.81
Std Dev	10.75



B1L103S, U12-ch77, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	3
Mean	62.67
Std Dev	0.4714

ampl

0 10 20 30 40 50 60 70

B1L103S, U12-ch77, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U12-ch78, adc0

calib_packv5_041523_1651.root, FC#0, port C2

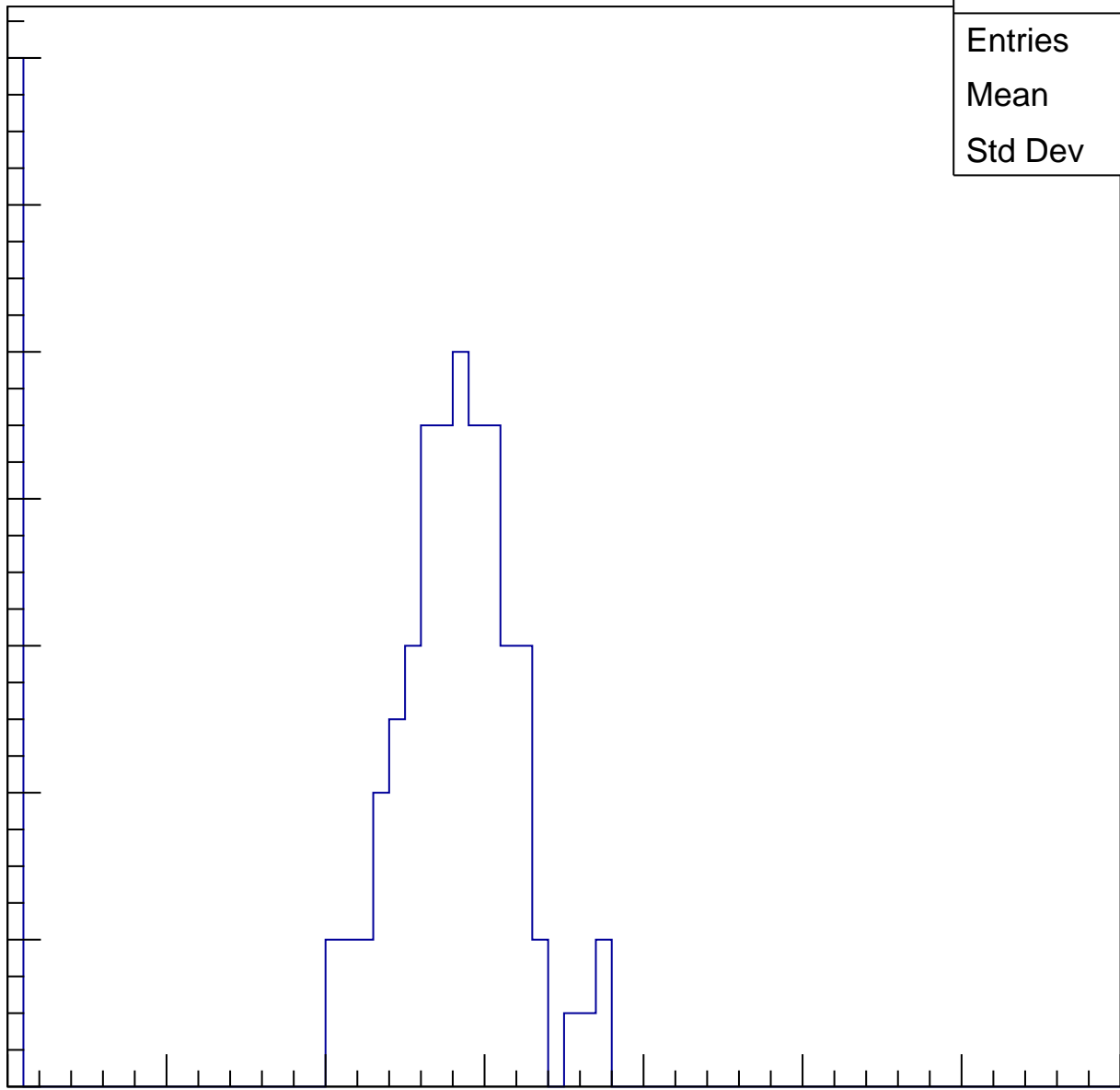
Entries	99
Mean	23.89
Std Dev	10.25

Entry

14
12
10
8
6
4
2
0

ampl

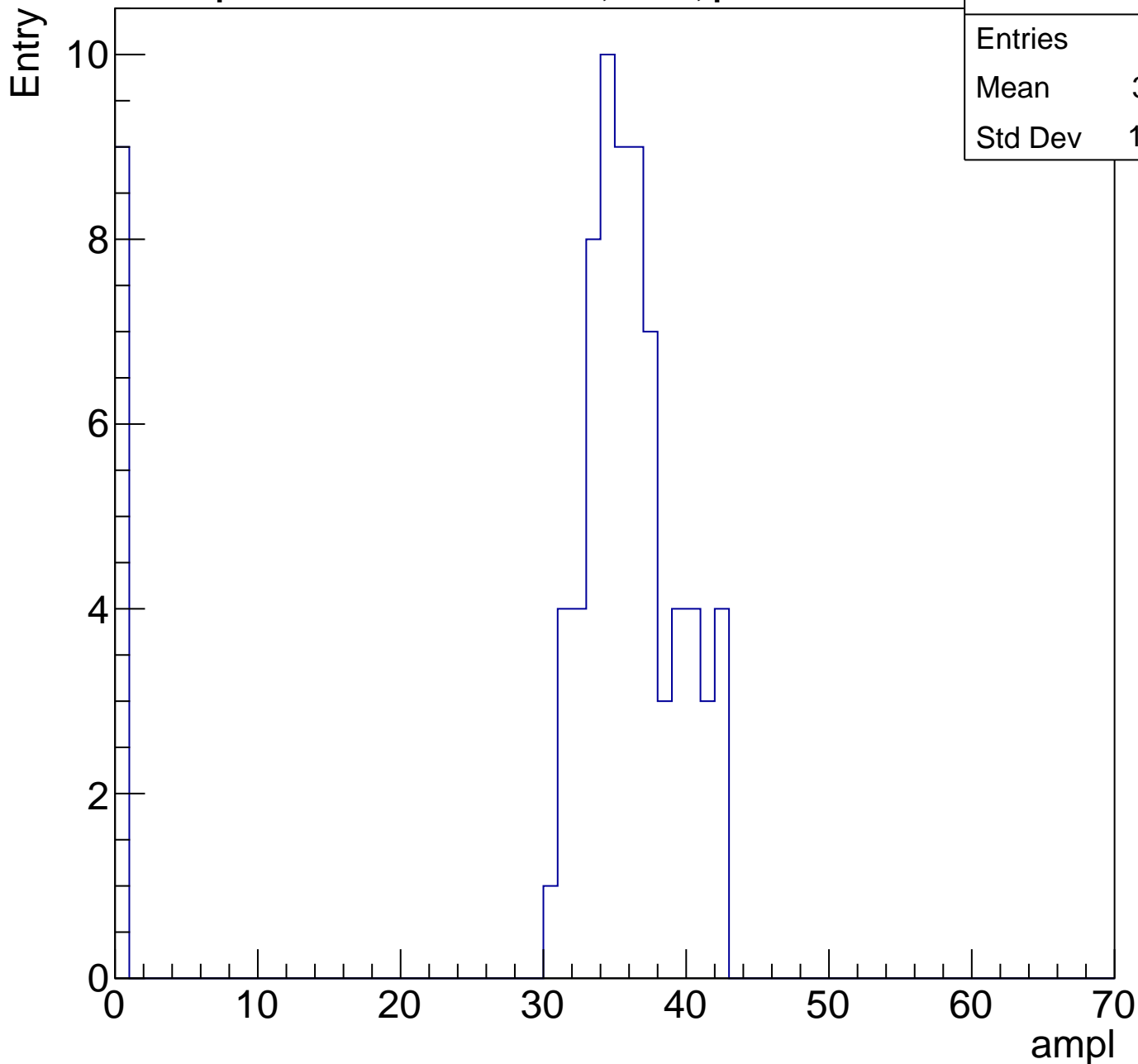
0 10 20 30 40 50 60 70



B1L103S, U12-ch78, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	79
Mean	31.71
Std Dev	11.73

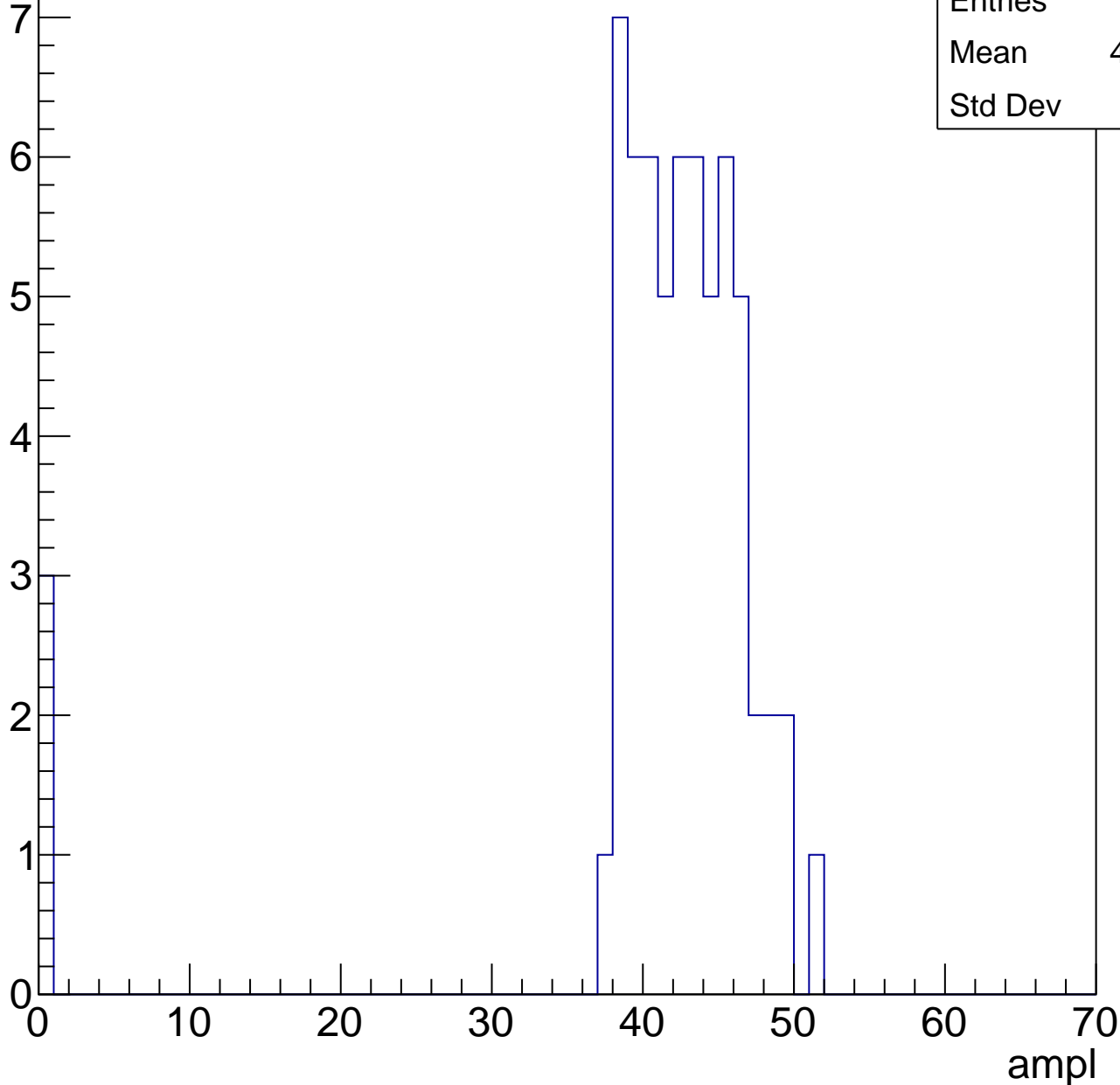


B1L103S, U12-ch78, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	63
Mean	40.49
Std Dev	9.62

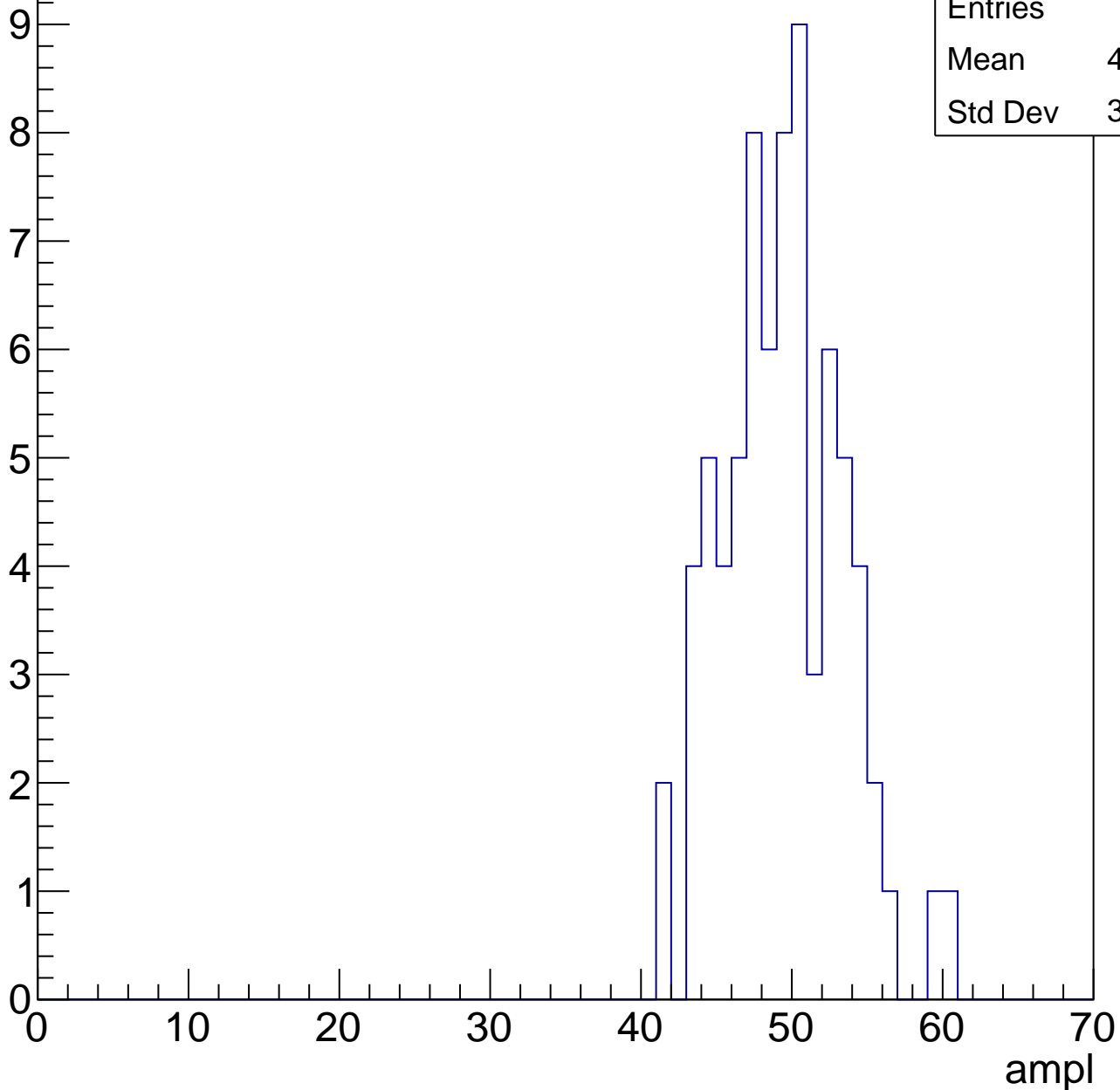


B1L103S, U12-ch78, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	74
Mean	48.93
Std Dev	3.926

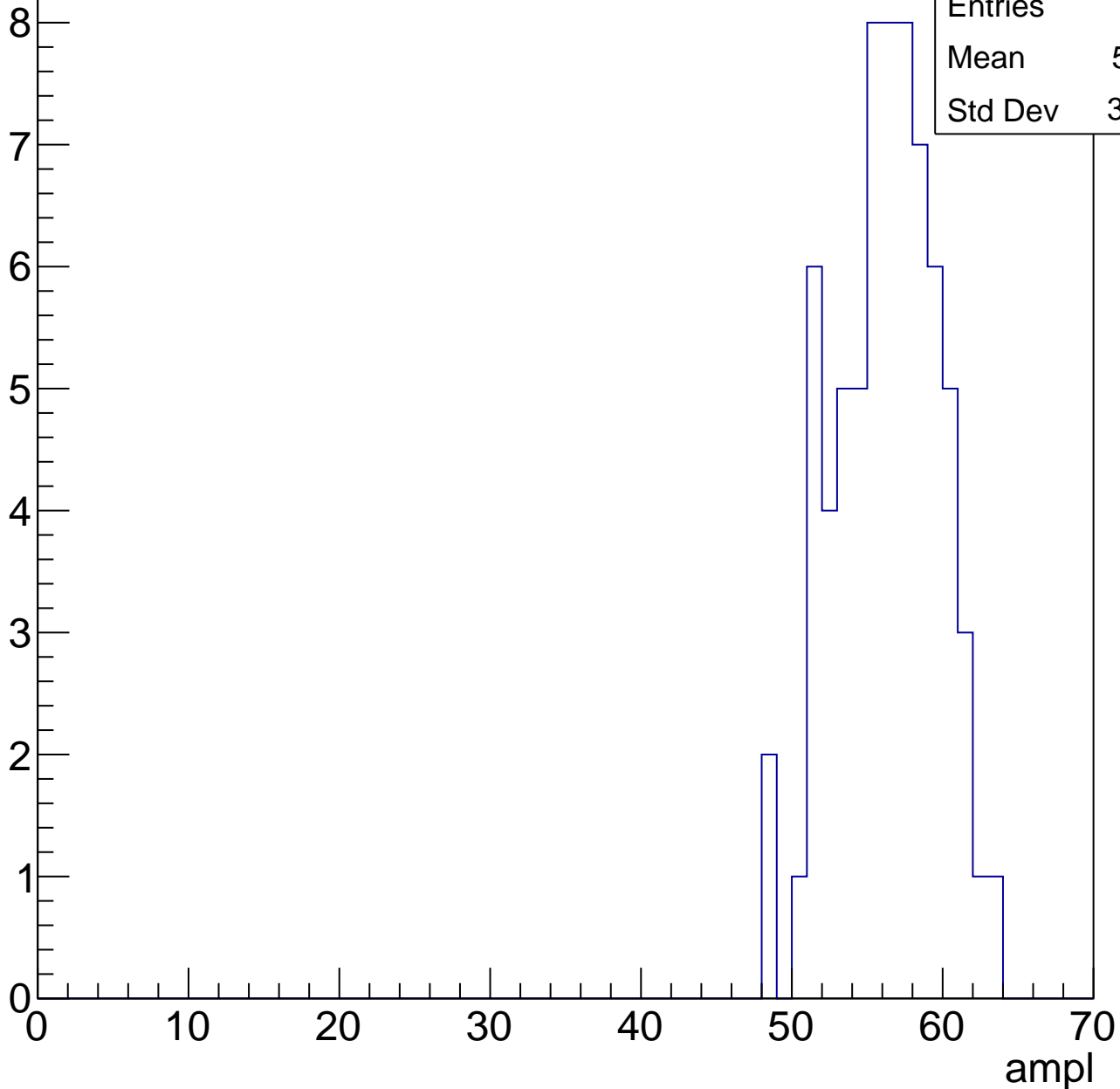


B1L103S, U12-ch78, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	55.81
Std Dev	3.335

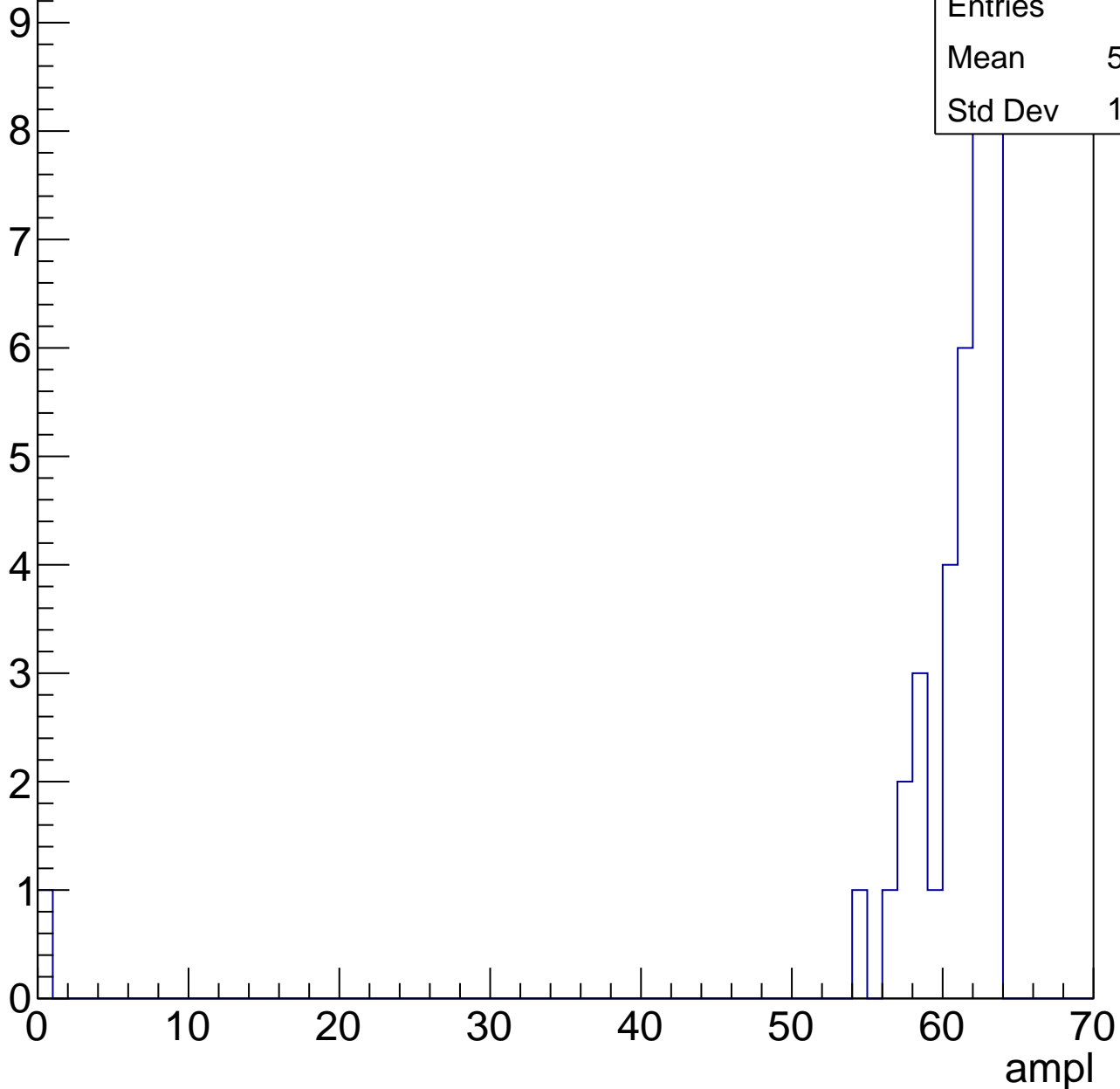


B1L103S, U12-ch78, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

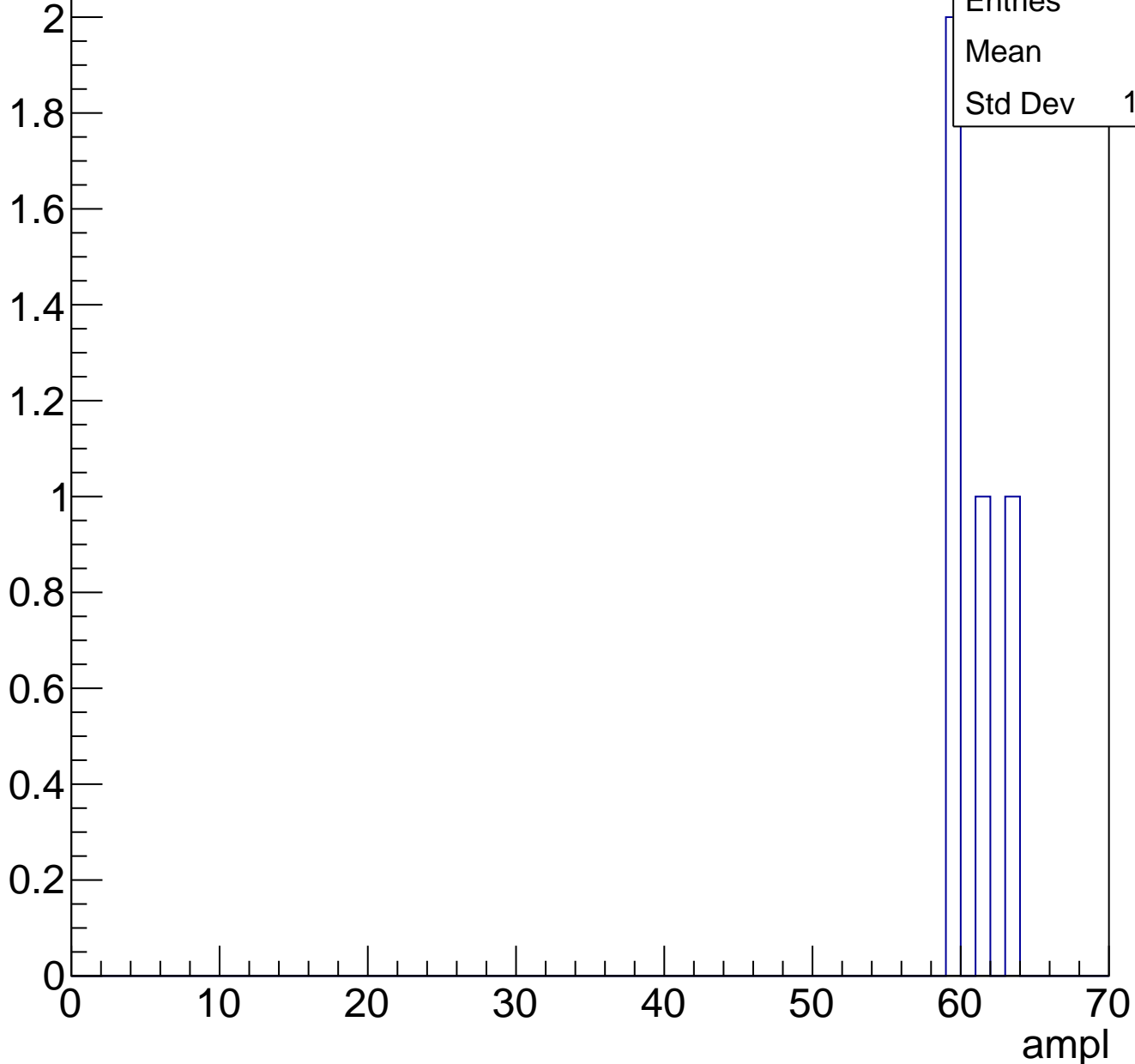
Entries	36
Mean	59.03
Std Dev	10.22



B1L103S, U12-ch78, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch78, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

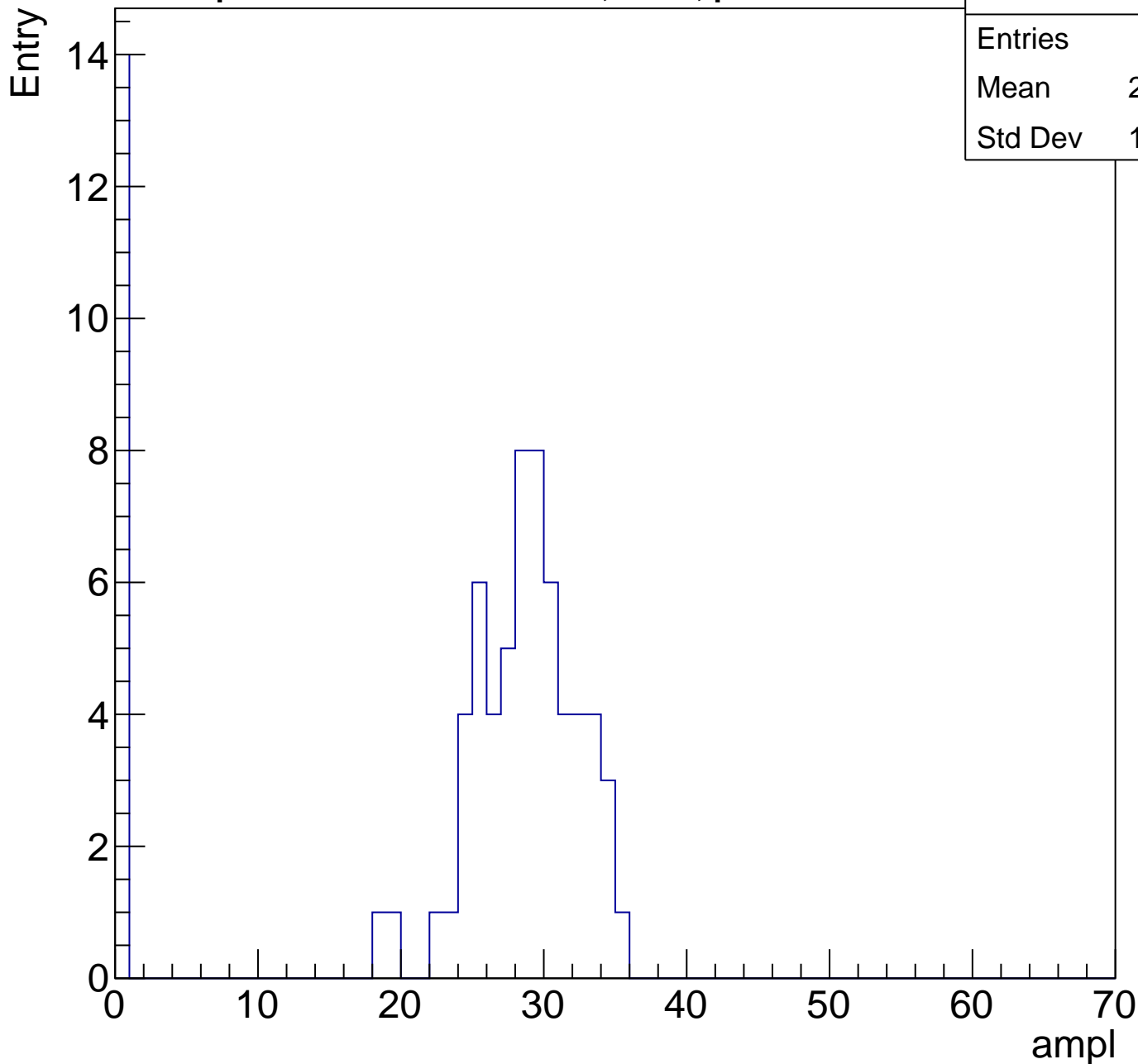
ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U12-ch79, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	75
Mean	22.99
Std Dev	11.47



B1L103S, U12-ch79, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	106
Mean	31.89
Std Dev	12.43

Entry

12

10

8

6

4

2

0

0

10

20

30

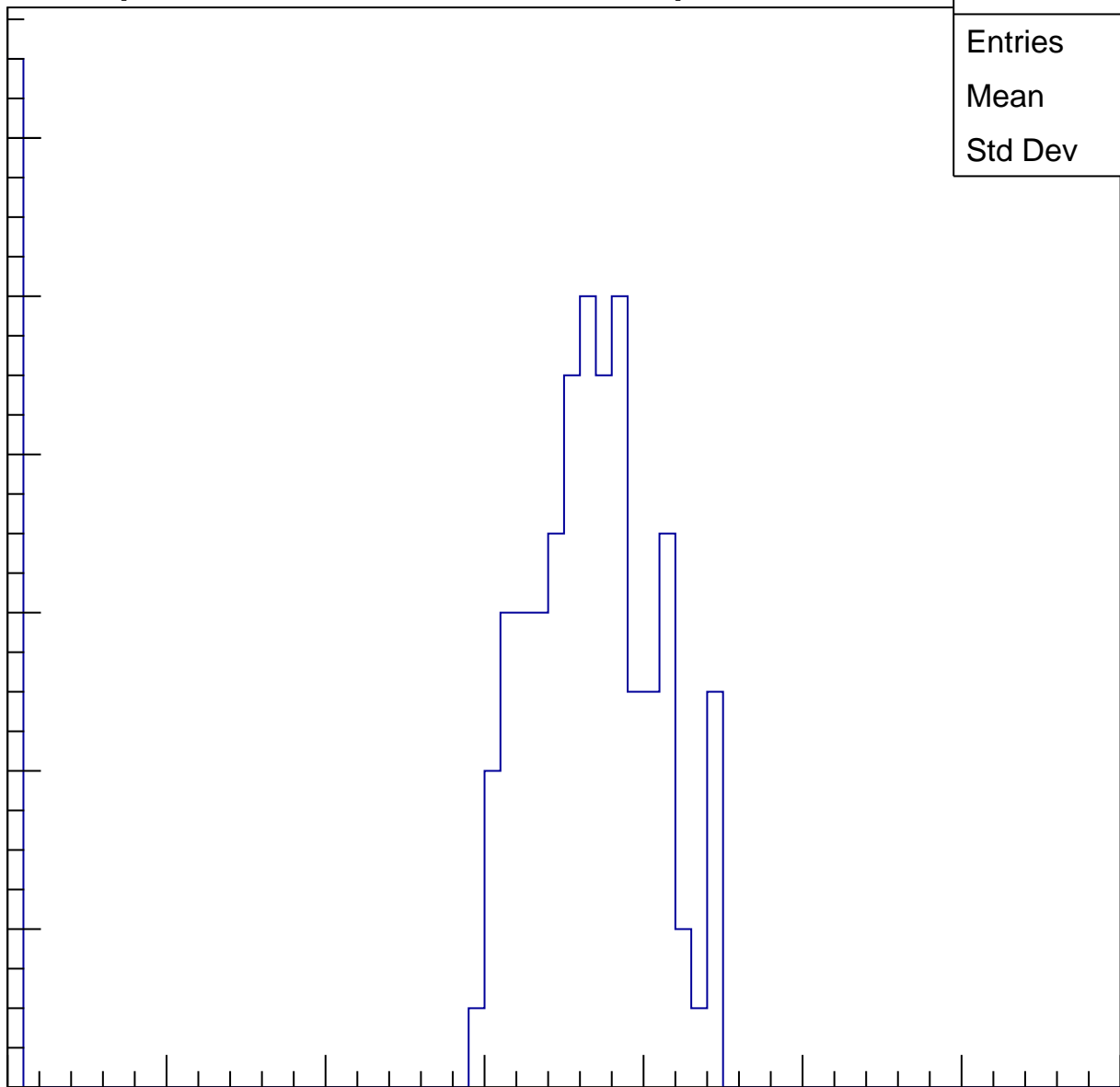
40

50

60

70

ampl

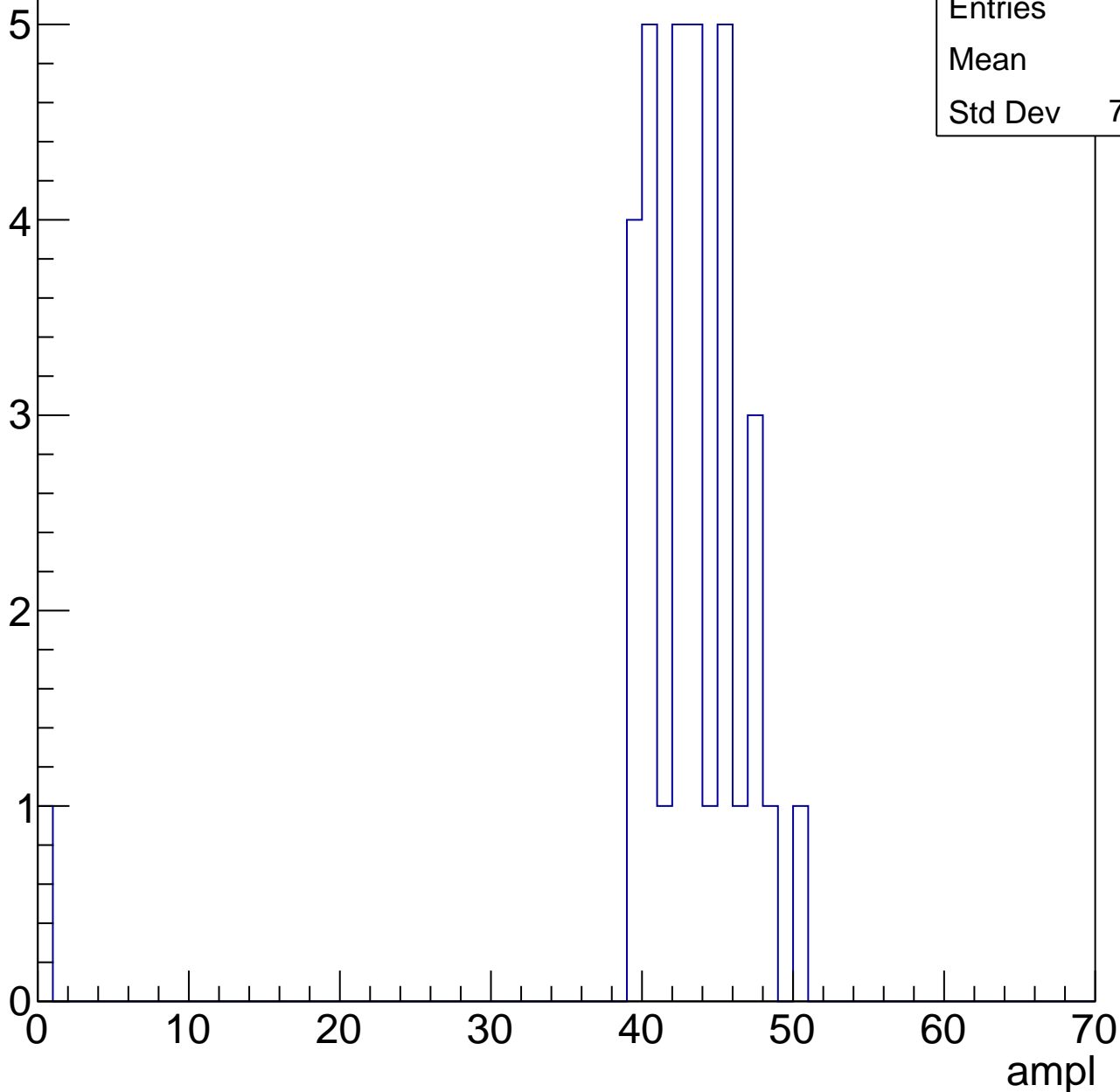


B1L103S, U12-ch79, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	33
Mean	41.7
Std Dev	7.907

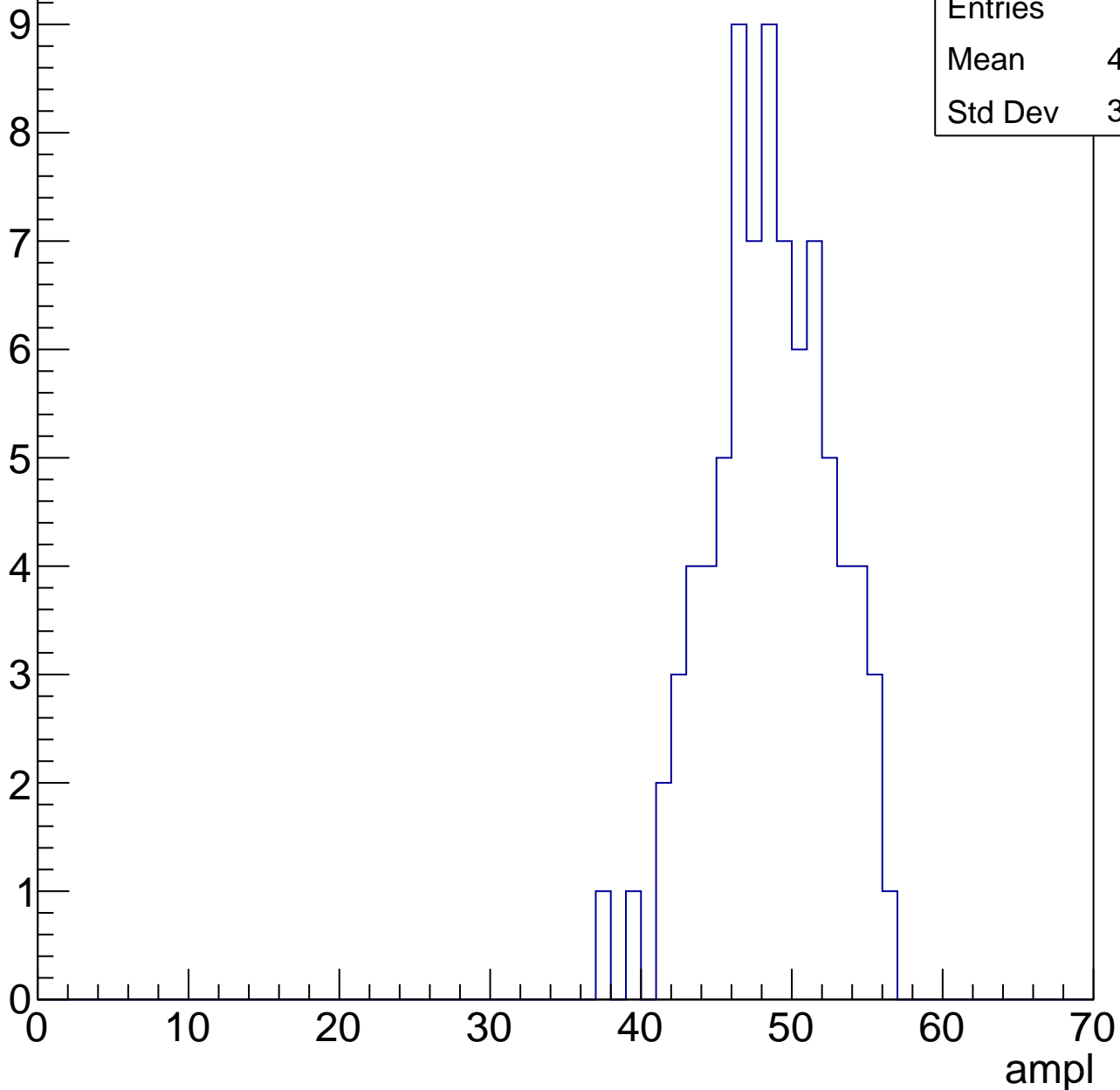


B1L103S, U12-ch79, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

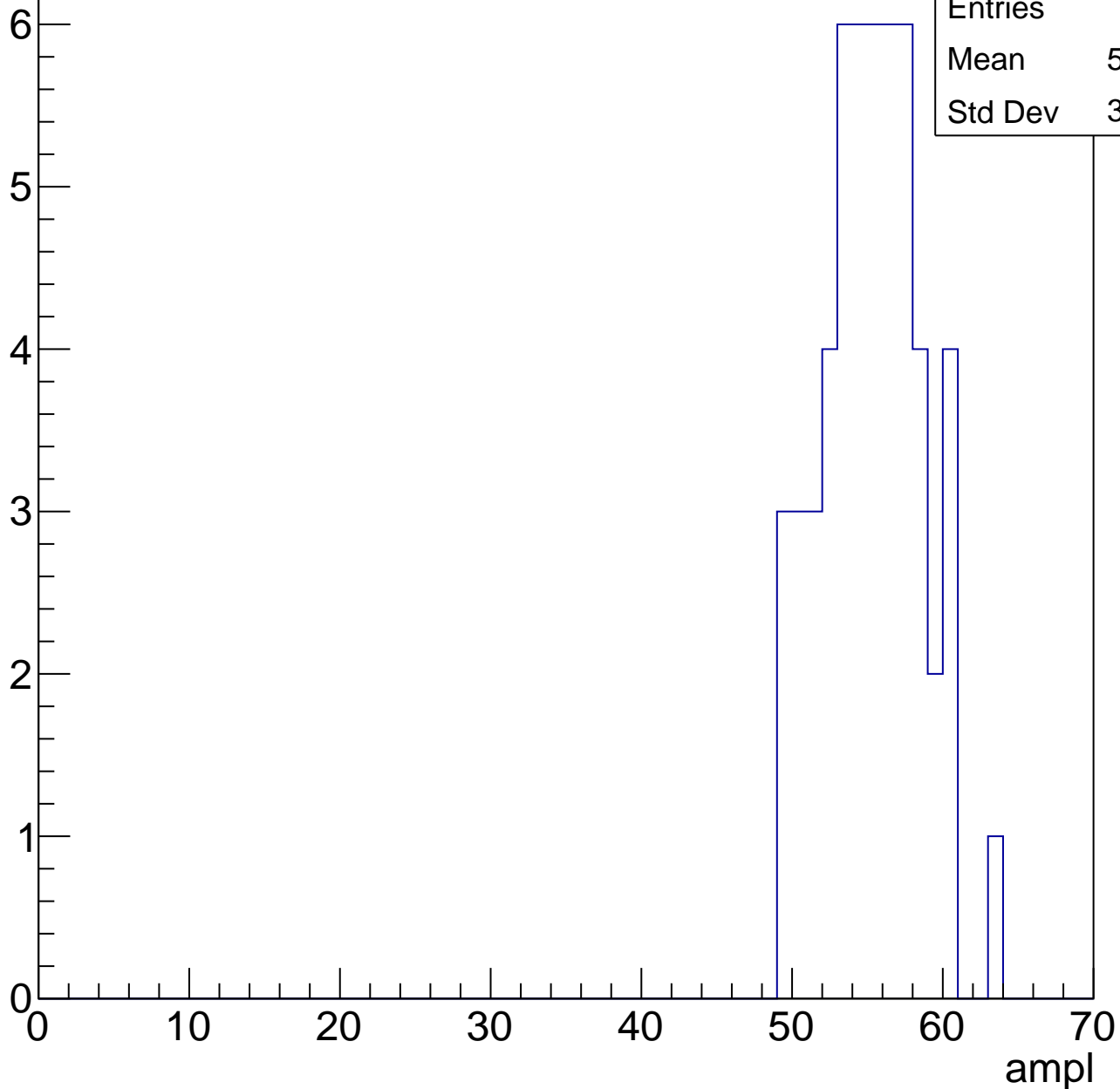
Entries	82
Mean	48.06
Std Dev	3.964



B1L103S, U12-ch79, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

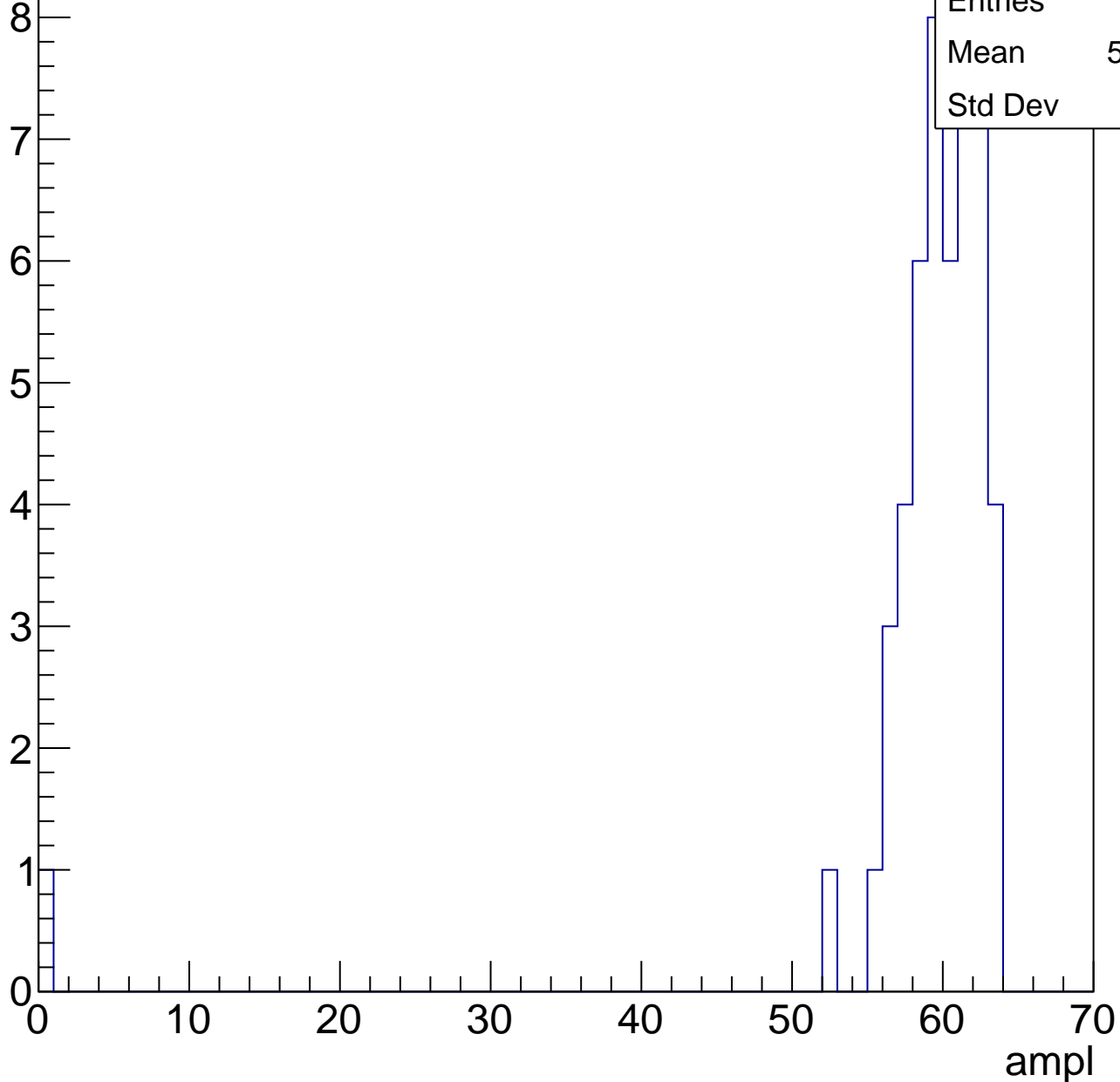


Entries	54
Mean	54.83
Std Dev	3.213

B1L103S, U12-ch79, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch79, adc6

calib_packv5_041523_1651.root, FC#0, port C2

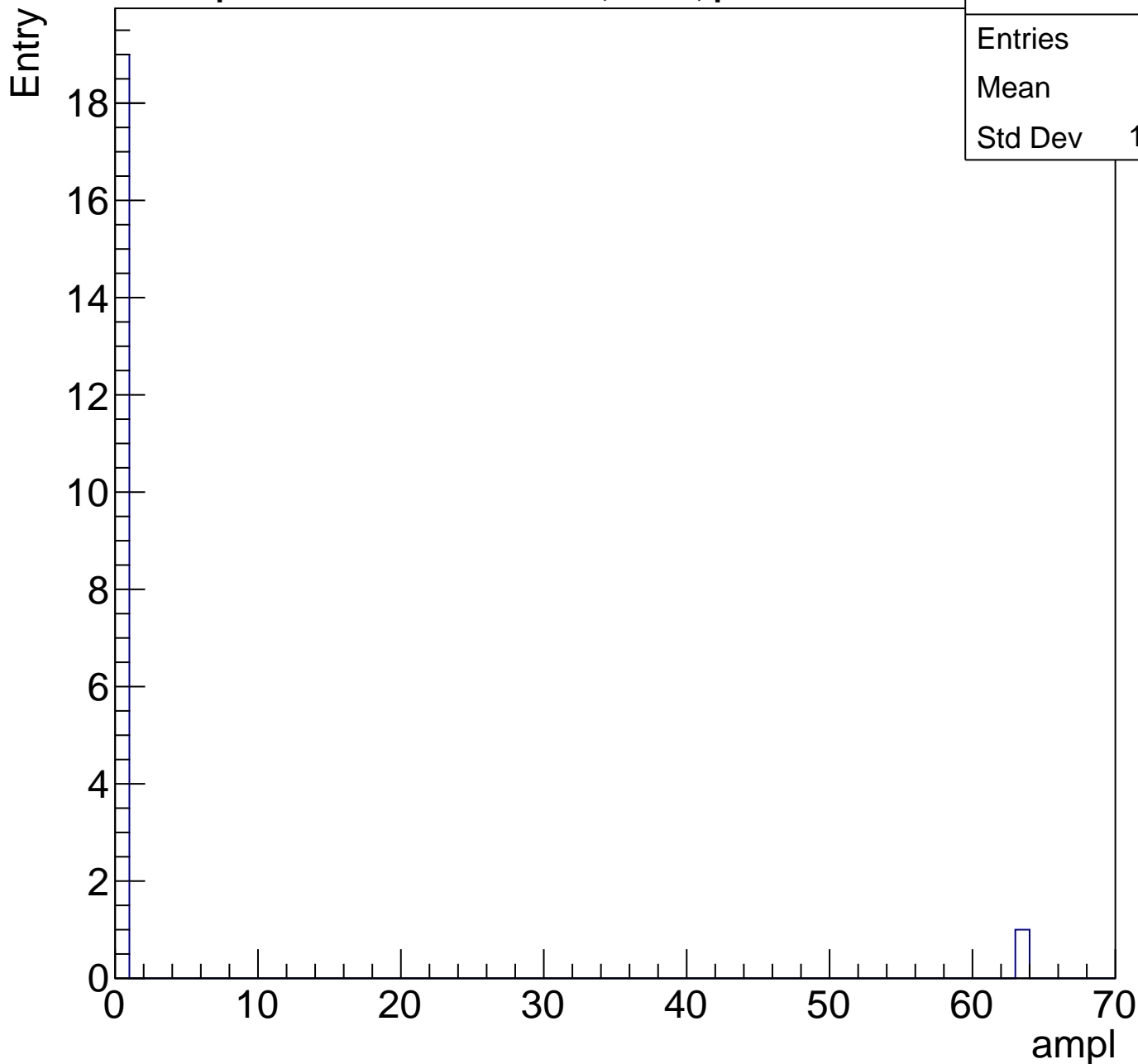
Entry



B1L103S, U12-ch79, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.15
Std Dev	13.73



B1L103S, U12-ch80, adc0

calib_packv5_041523_1651.root, FC#0, port C2

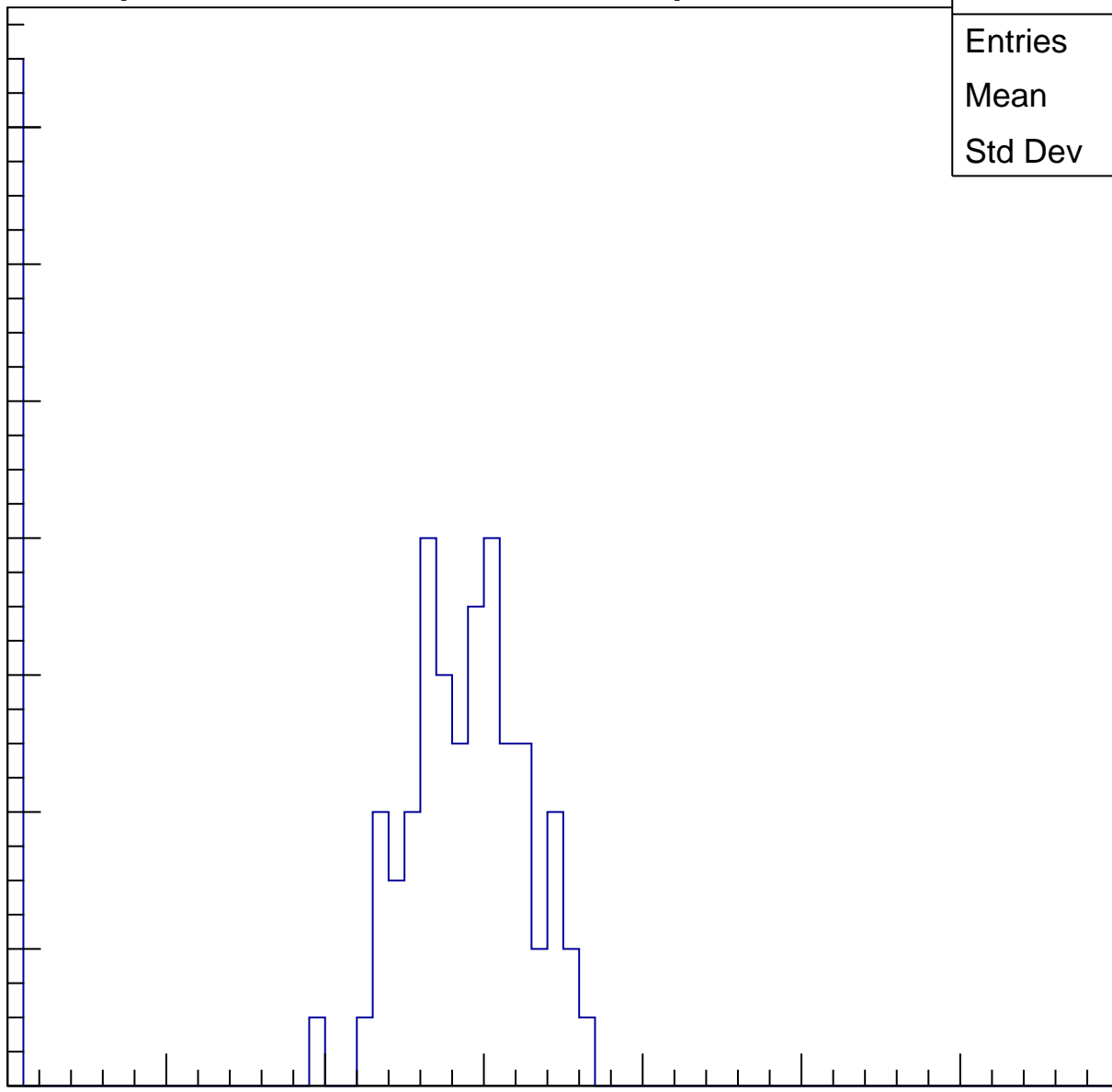
Entries	81
Mean	23.22
Std Dev	11.53

Entry

14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl



B1L103S, U12-ch80, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	70
Mean	28.81
Std Dev	12.82

Entry

10

8

6

4

2

0

0

10

20

30

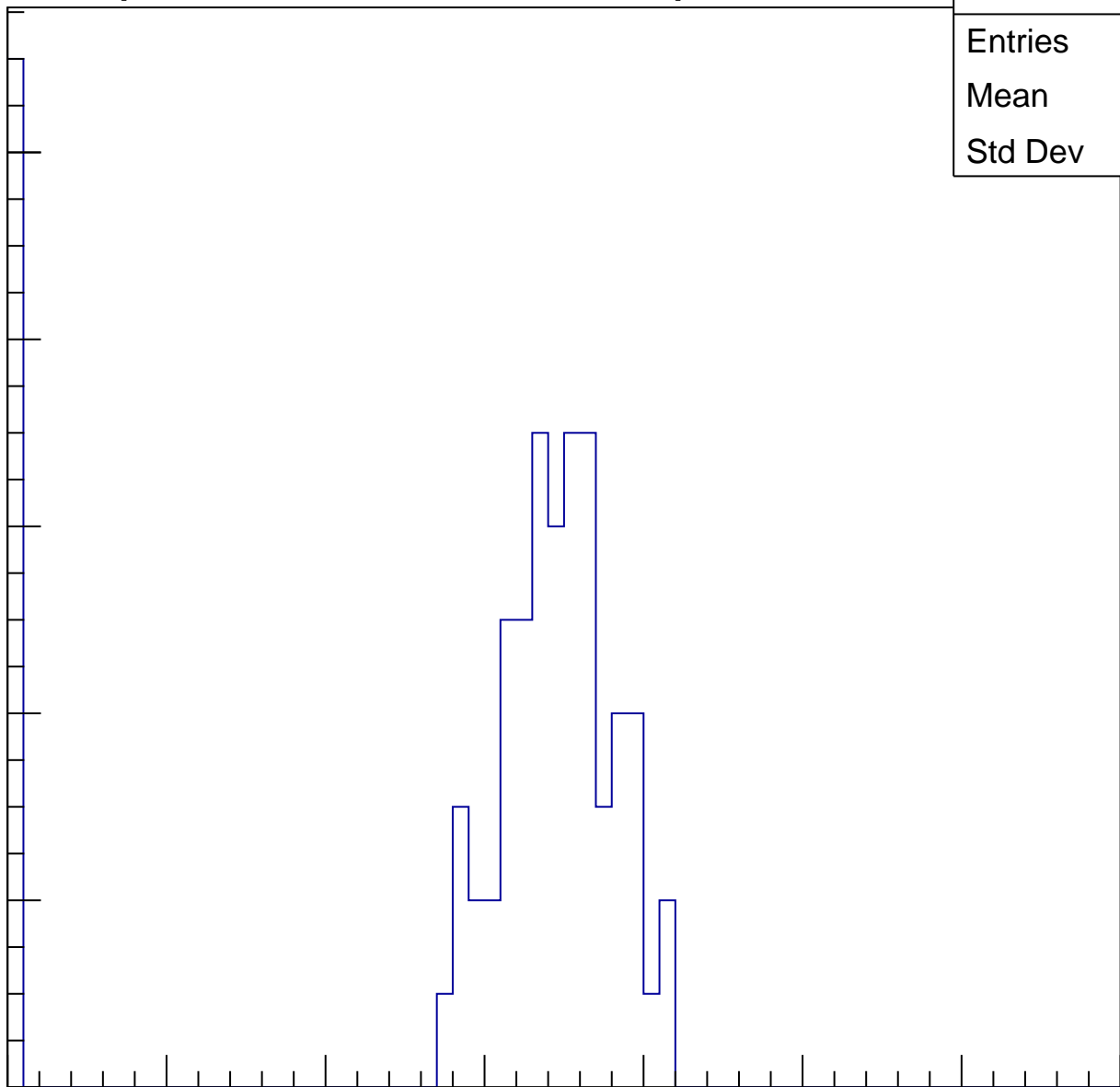
40

50

60

70

ampl

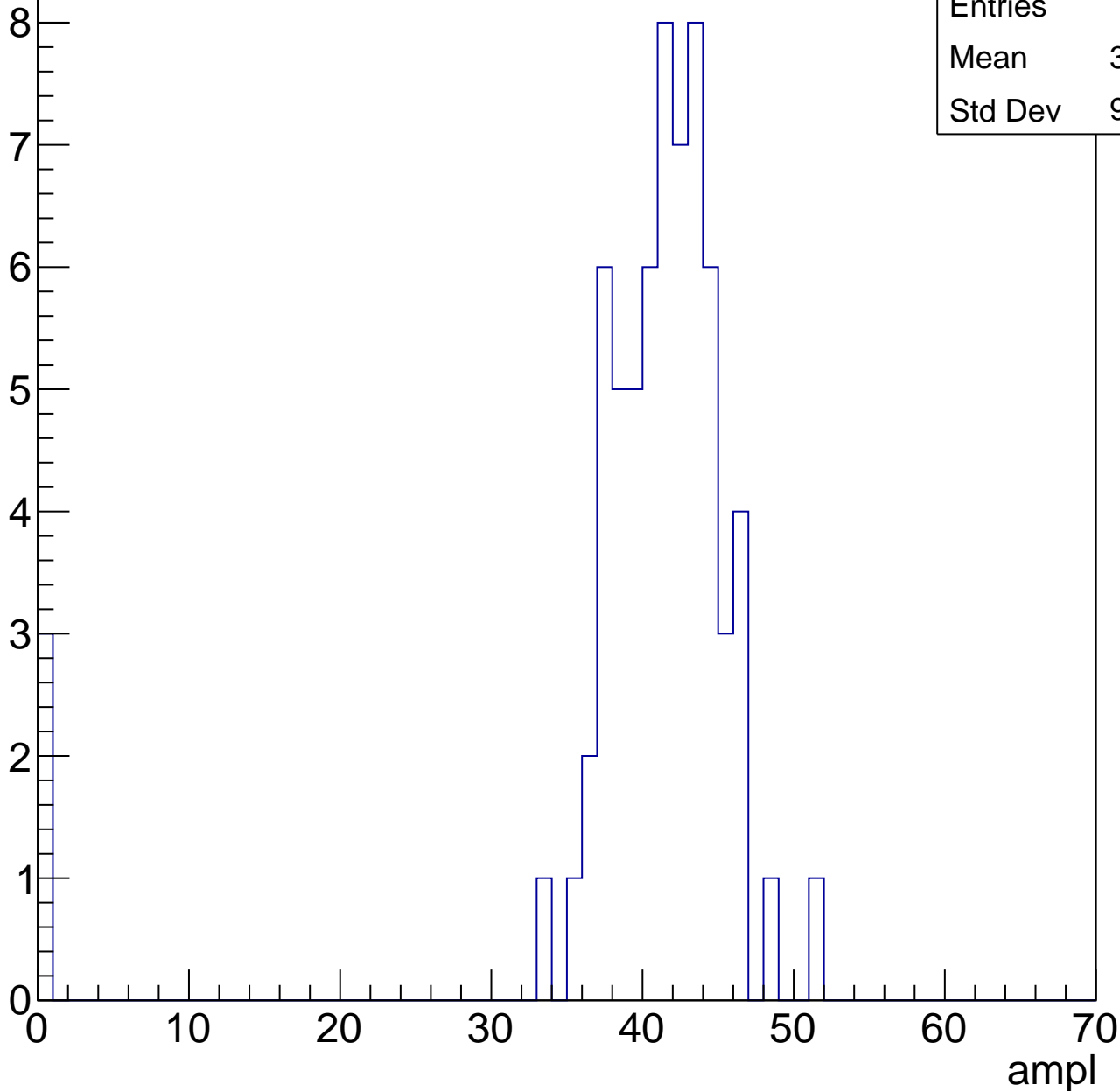


B1L103S, U12-ch80, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	39.33
Std Dev	9.112

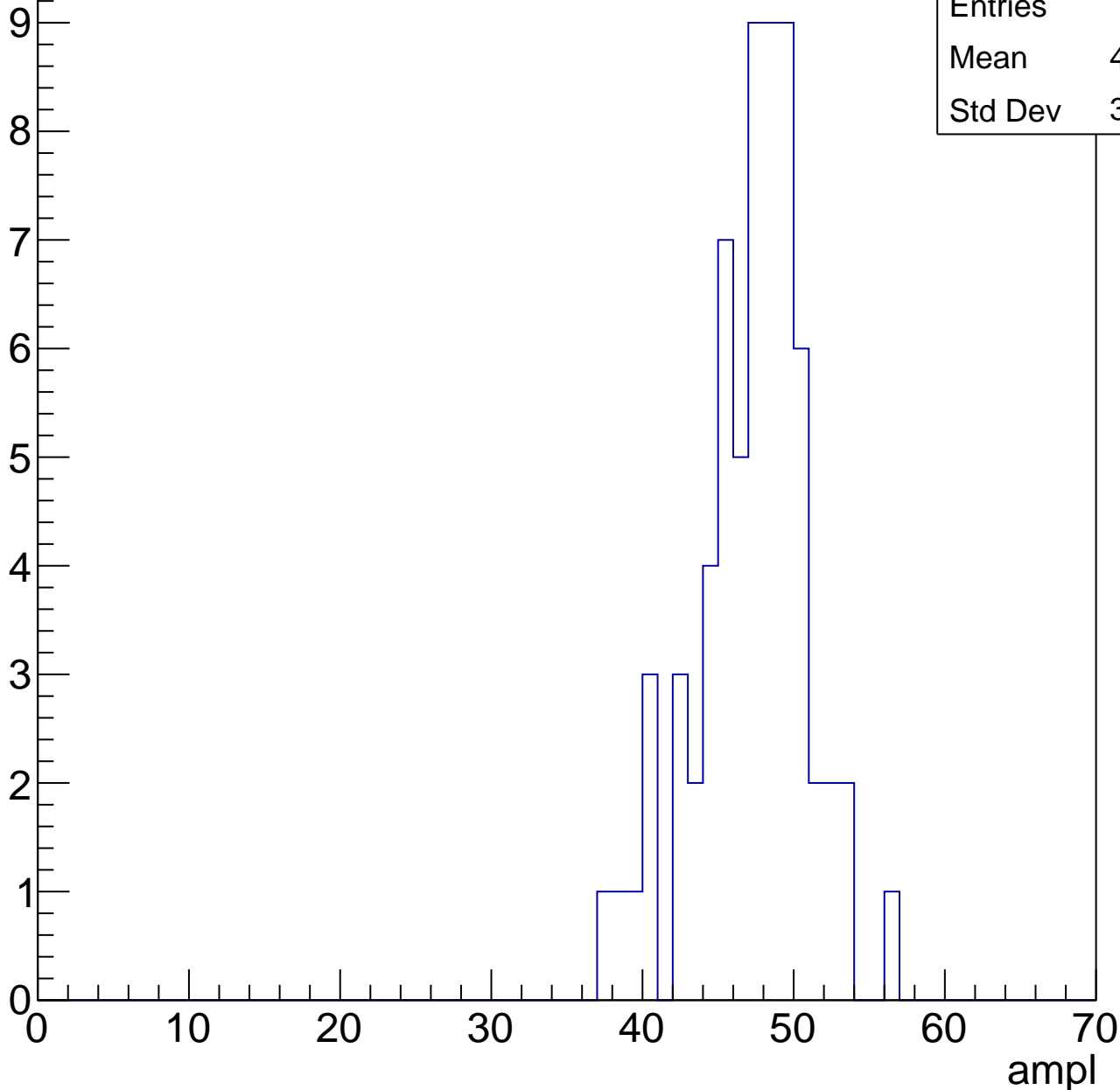


B1L103S, U12-ch80, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	46.73
Std Dev	3.659

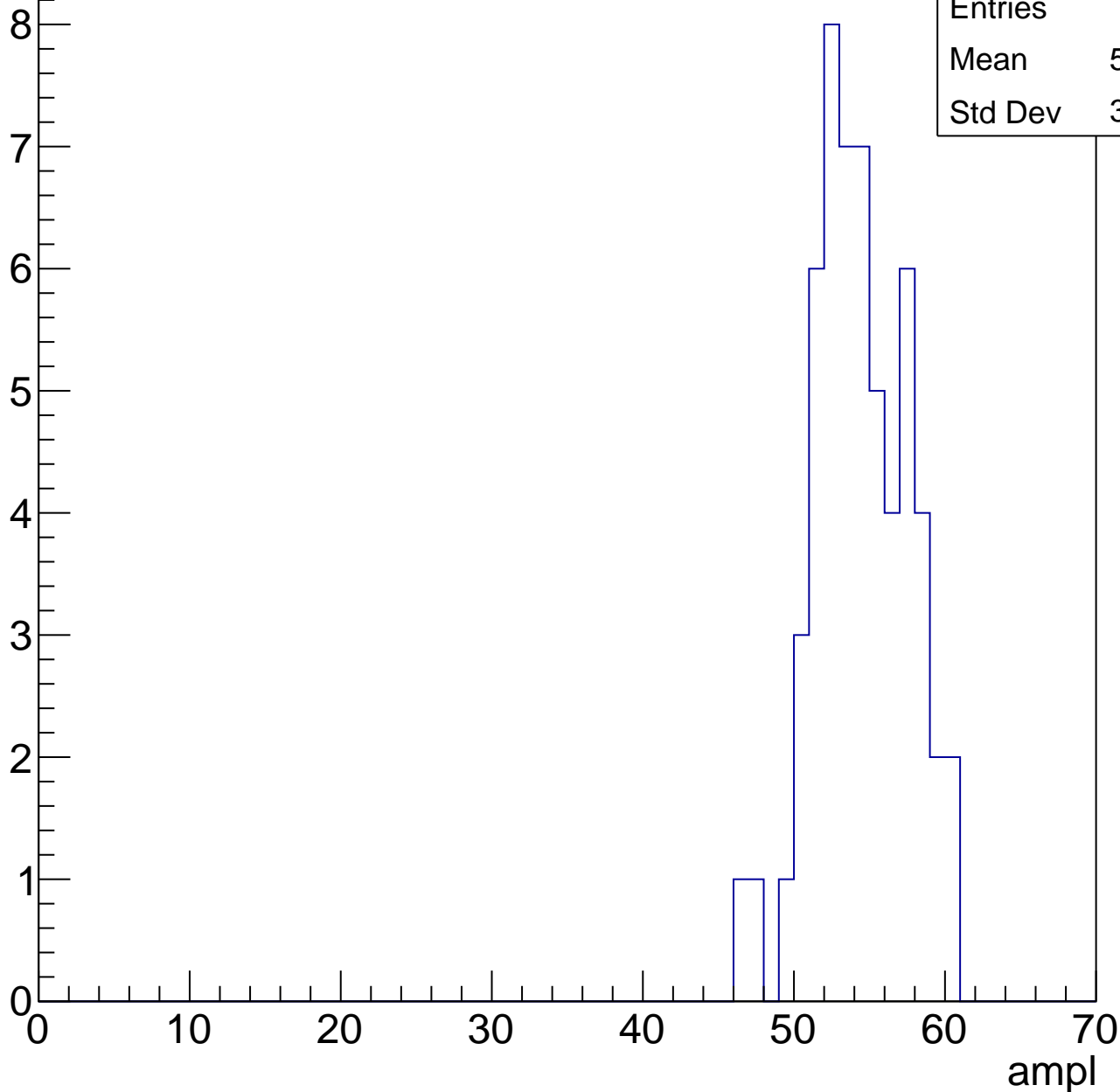


B1L103S, U12-ch80, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	57
Mean	53.93
Std Dev	3.077

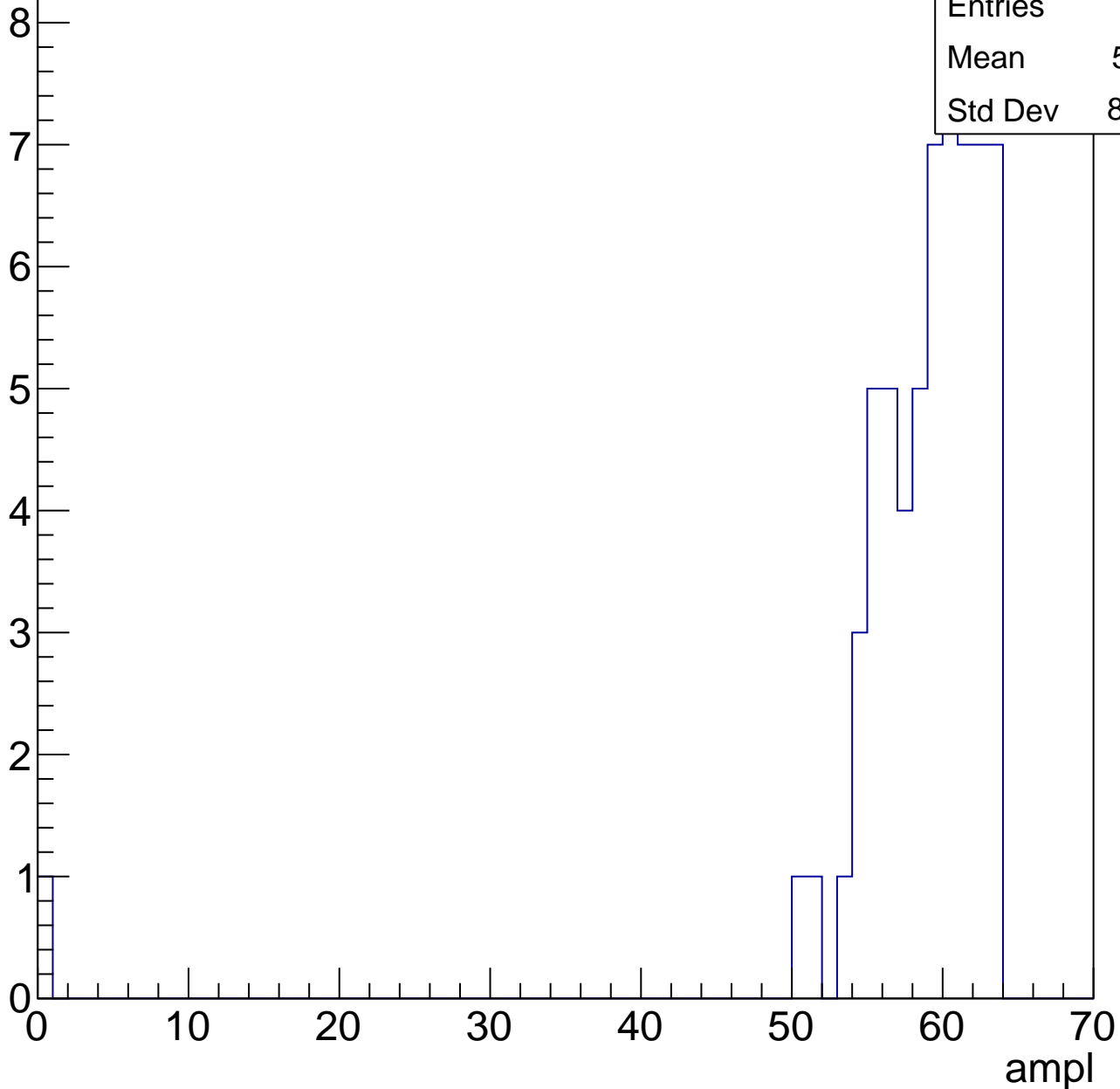


B1L103S, U12-ch80, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	57.81
Std Dev	8.038



B1L103S, U12-ch80, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

3

2.5

2

1.5

1

0.5

0

ampl

Entries	9
Mean	61.22
Std Dev	1.685

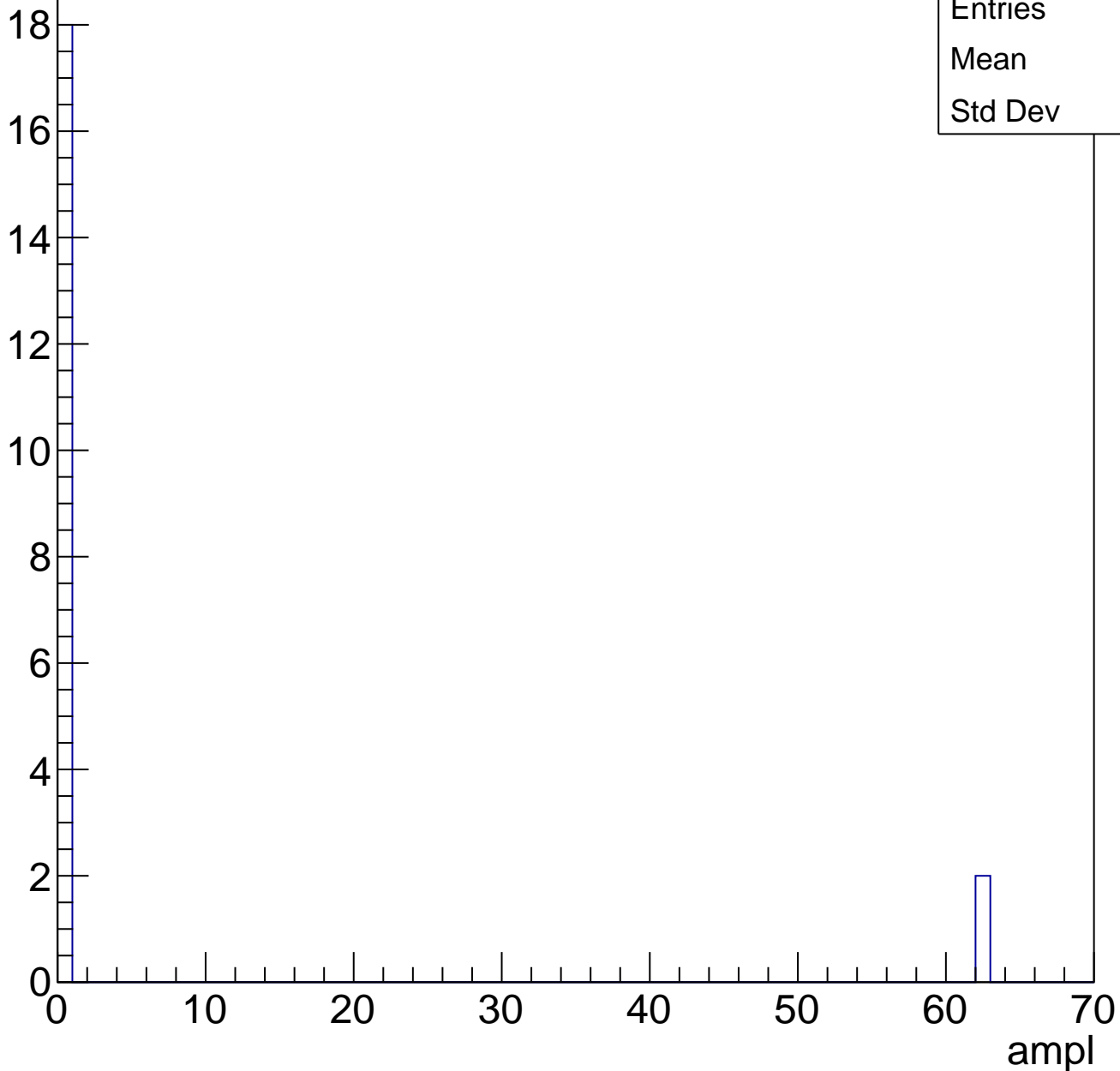
0 10 20 30 40 50 60 70

B1L103S, U12-ch80, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	6.2
Std Dev	18.6

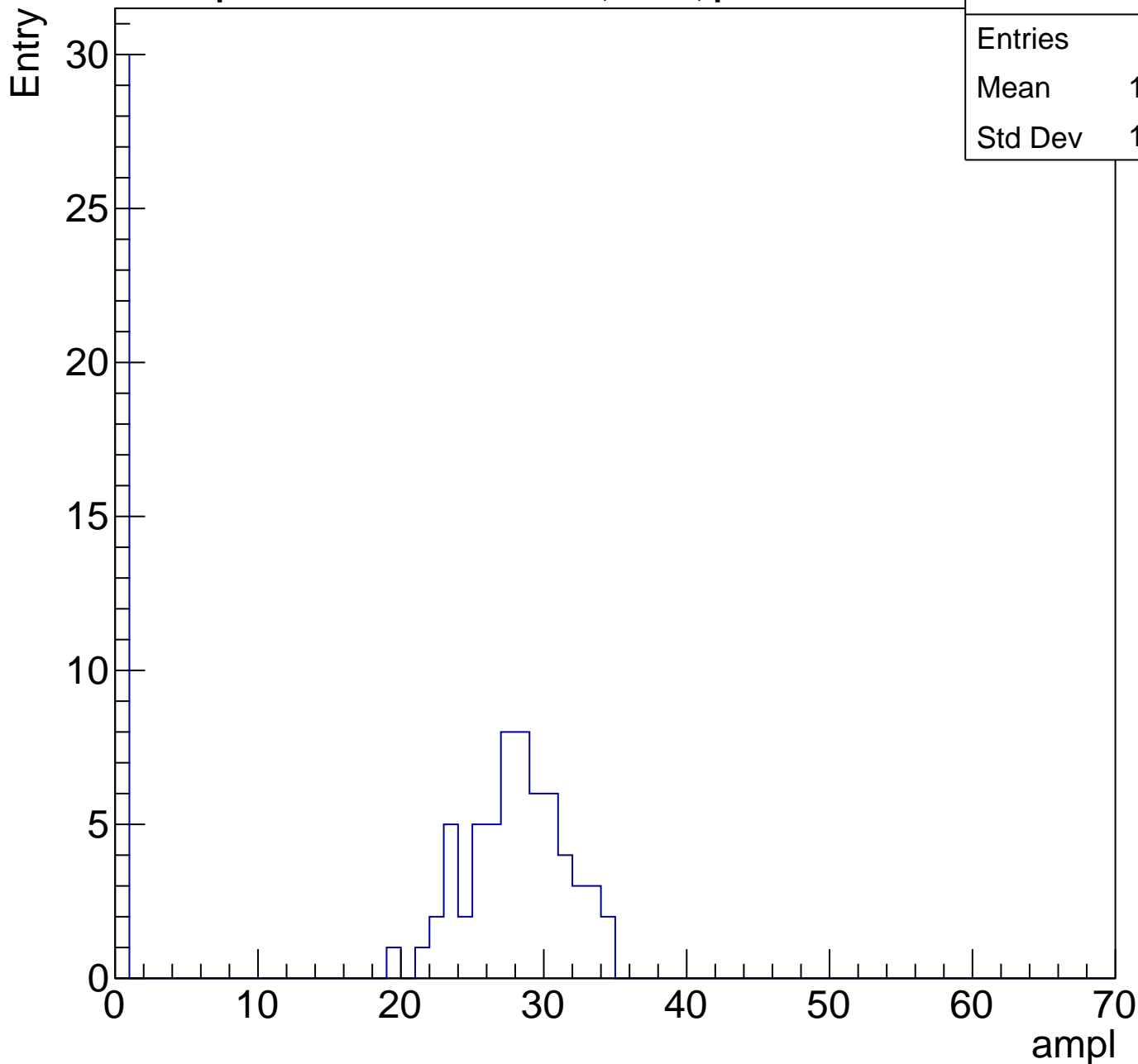
Entry



B1L103S, U12-ch81, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	91
Mean	18.49
Std Dev	13.26



B1L103S, U12-ch81, adc1

calib_packv5_041523_1651.root, FC#0, port C2

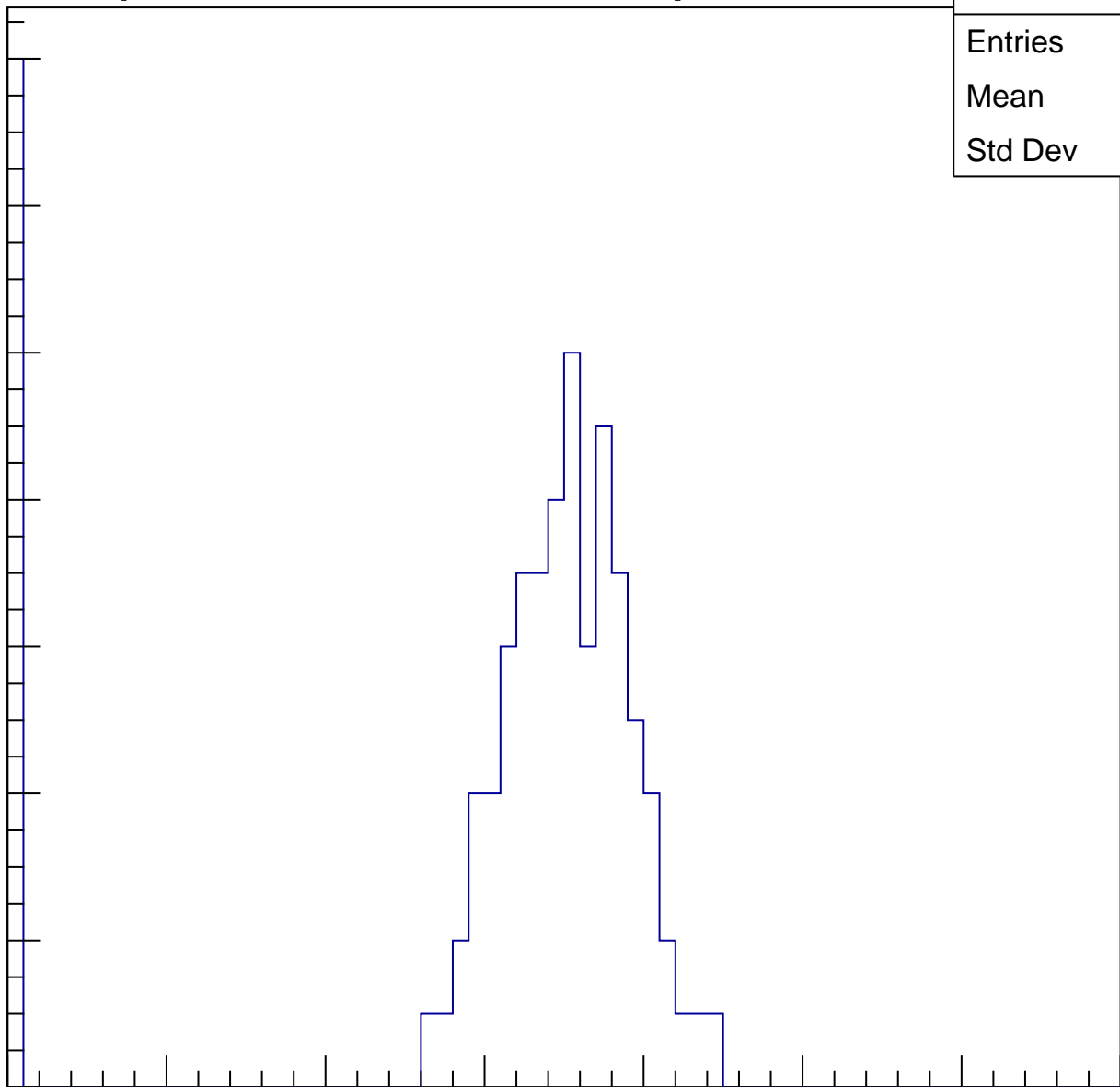
Entries	100
Mean	29.89
Std Dev	12.56

Entry

14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

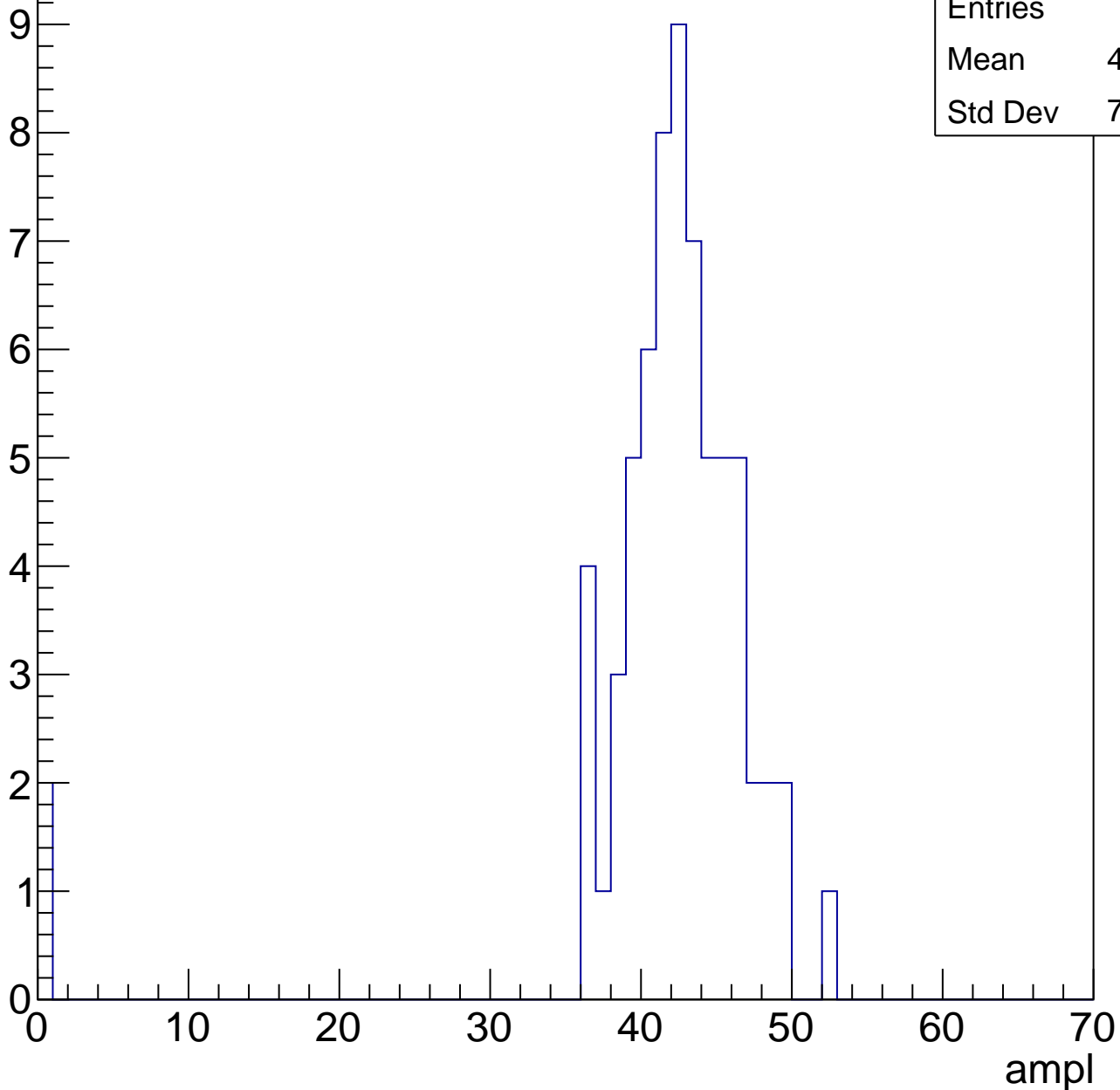


B1L103S, U12-ch81, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	41.07
Std Dev	7.952

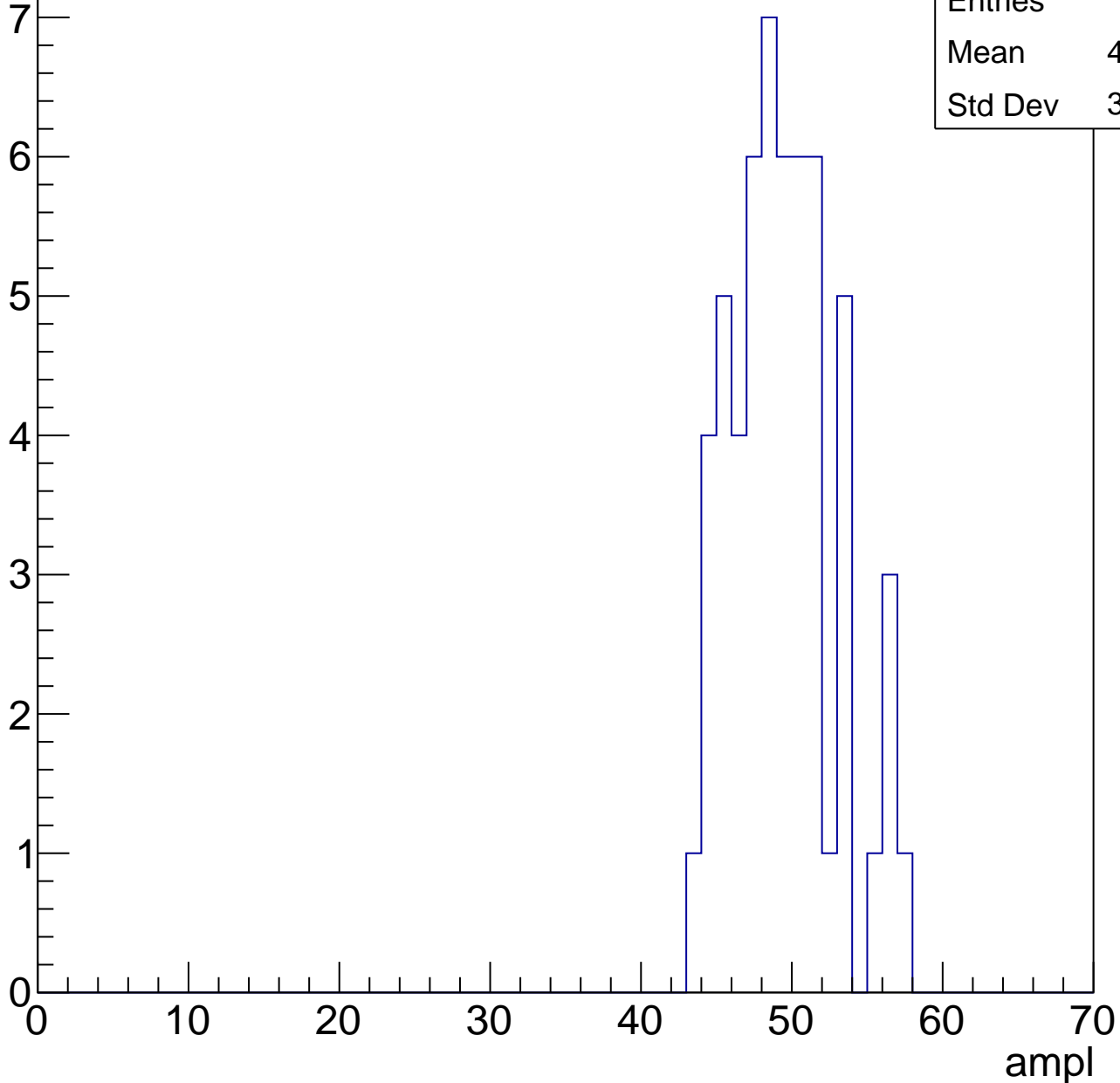


B1L103S, U12-ch81, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	56
Mean	48.98
Std Dev	3.404



B1L103S, U12-ch81, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entries	67
Mean	54.01
Std Dev	3.767

Entry

10

8

6

4

2

0

0

10

20

30

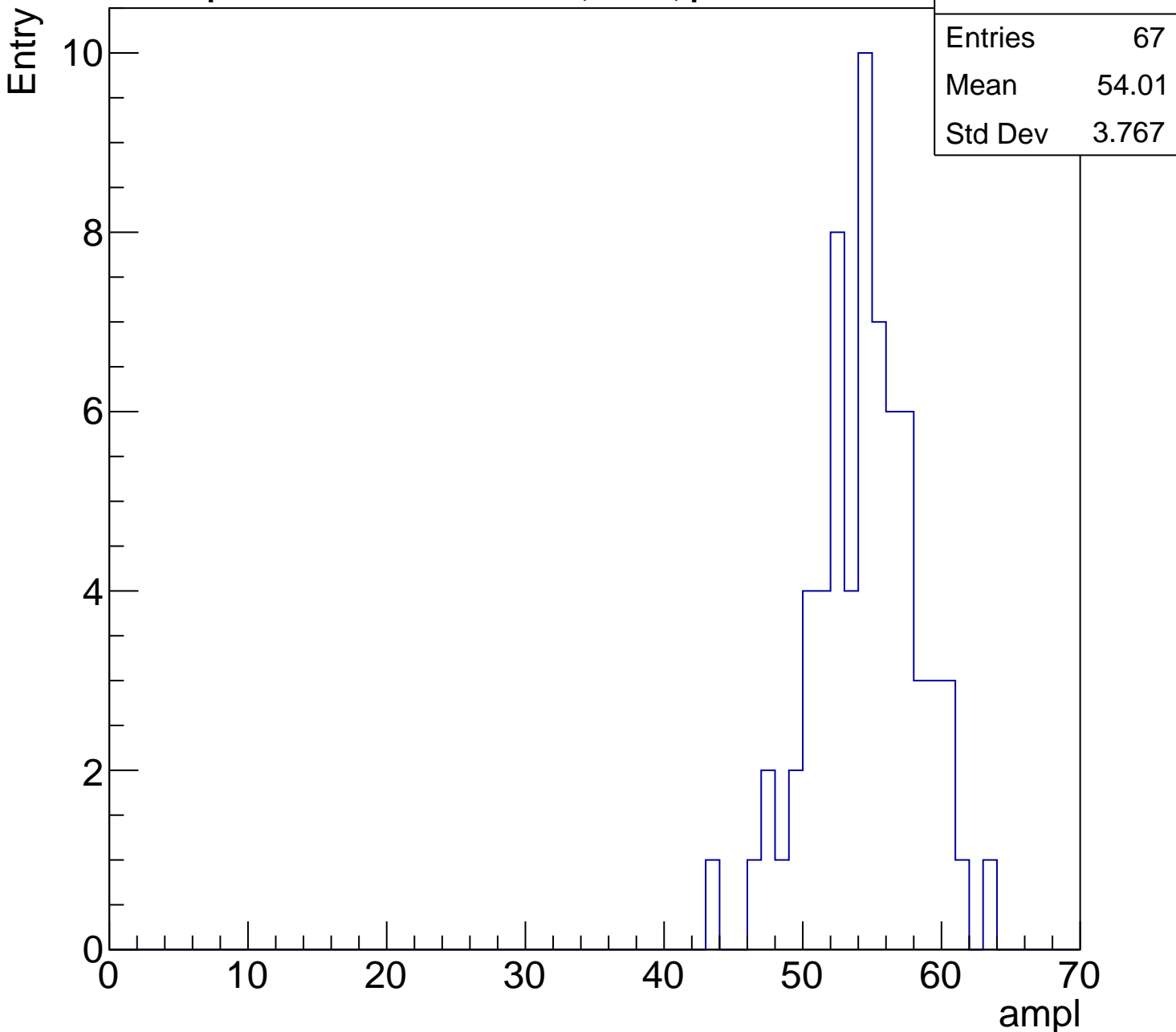
40

50

60

ampl

70

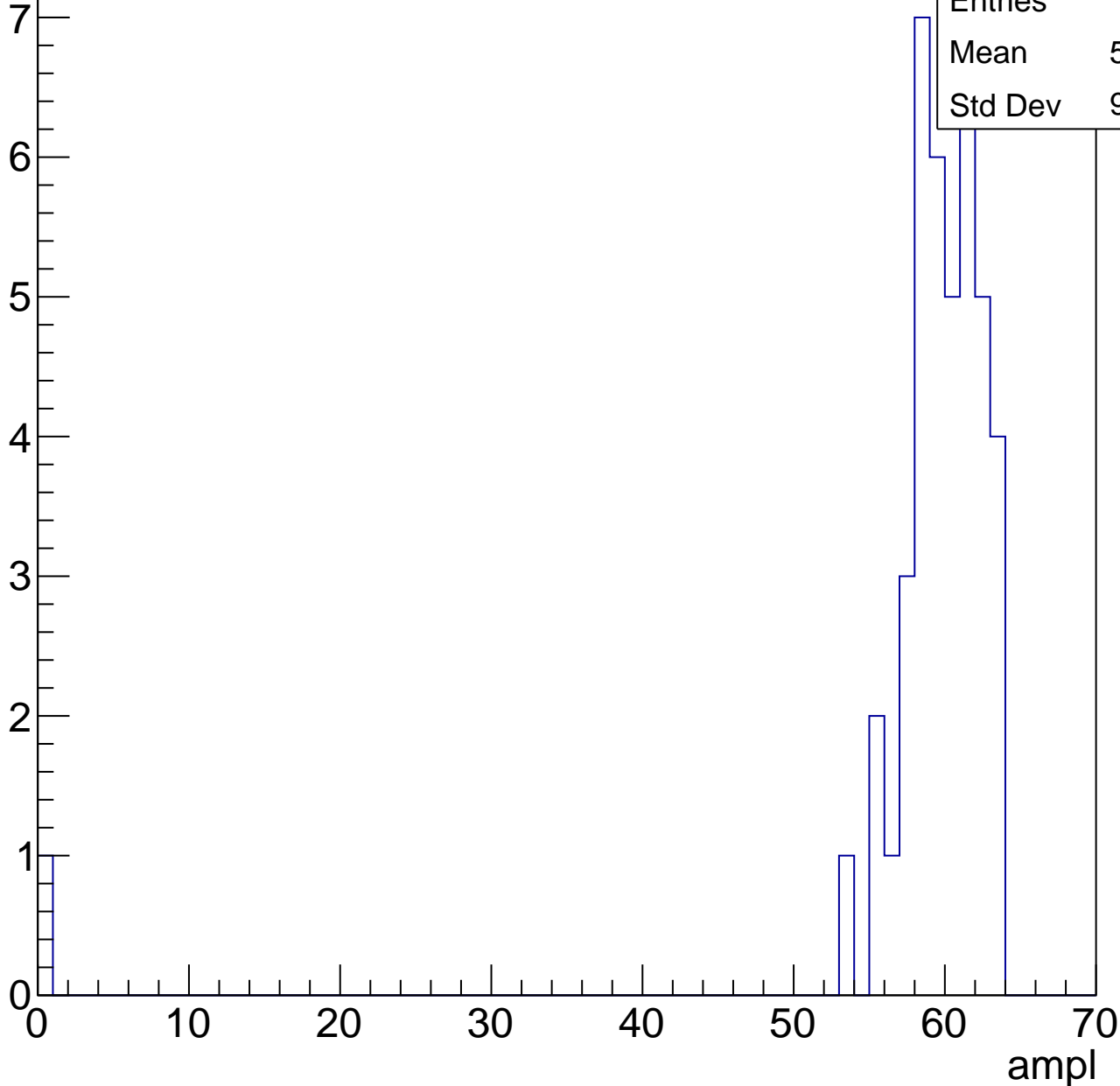


B1L103S, U12-ch81, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	42
Mean	58.07
Std Dev	9.364

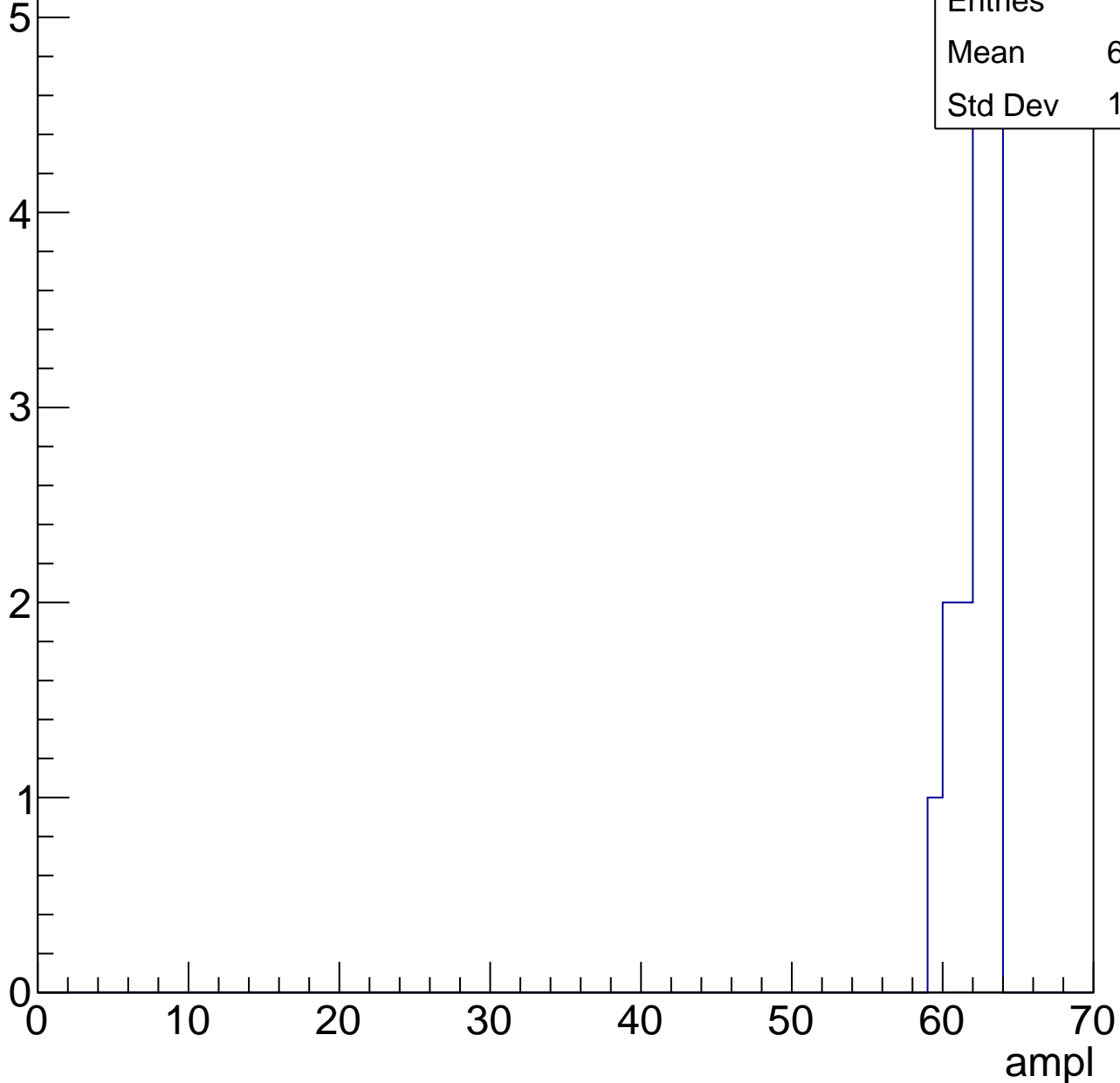


B1L103S, U12-ch81, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	15
Mean	61.73
Std Dev	1.236



B1L103S, U12-ch81, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

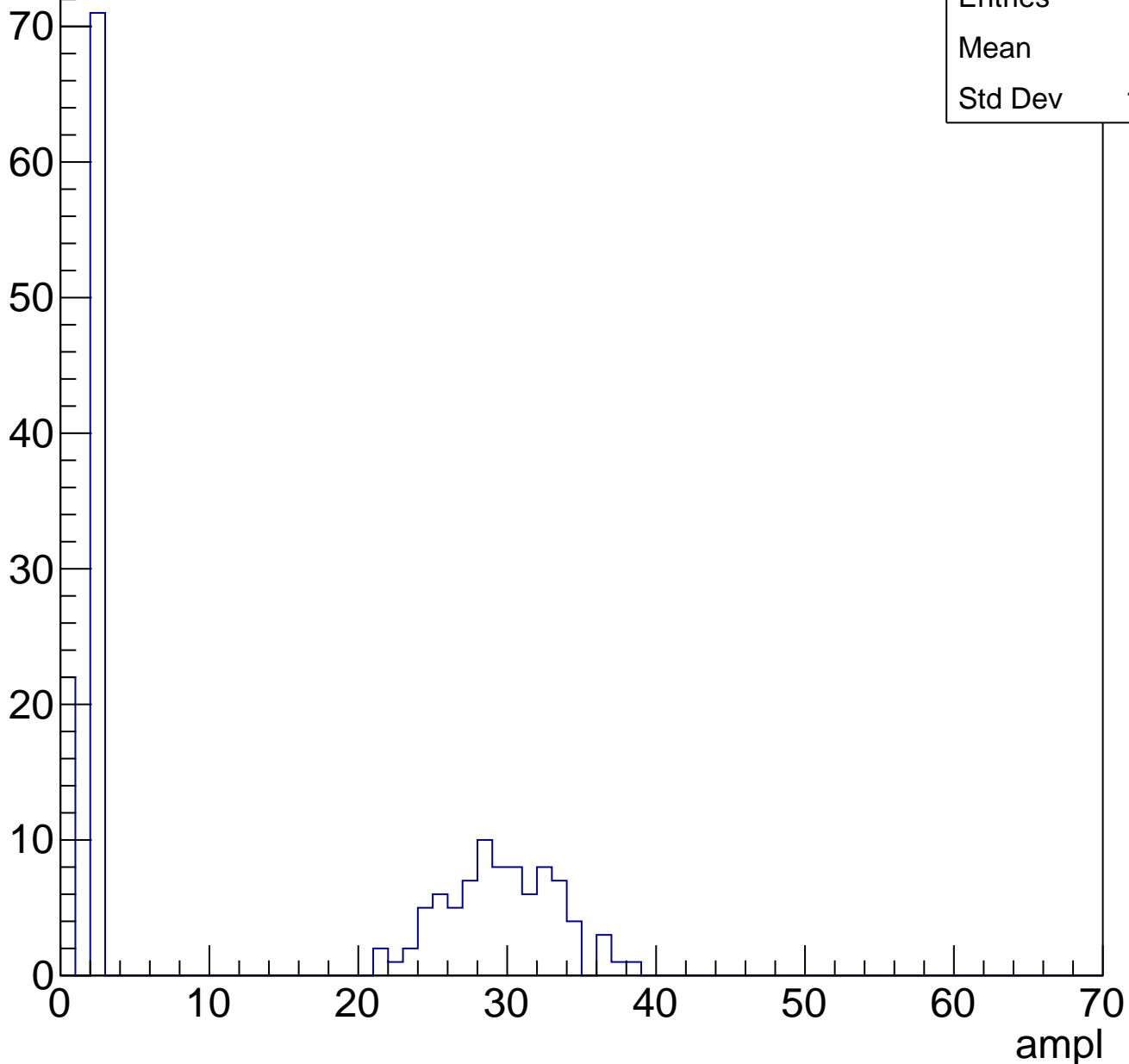
Entries	19
Mean	0
Std Dev	0

B1L103S, U12-ch82, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	177
Mean	14.6
Std Dev	14.01

Entry

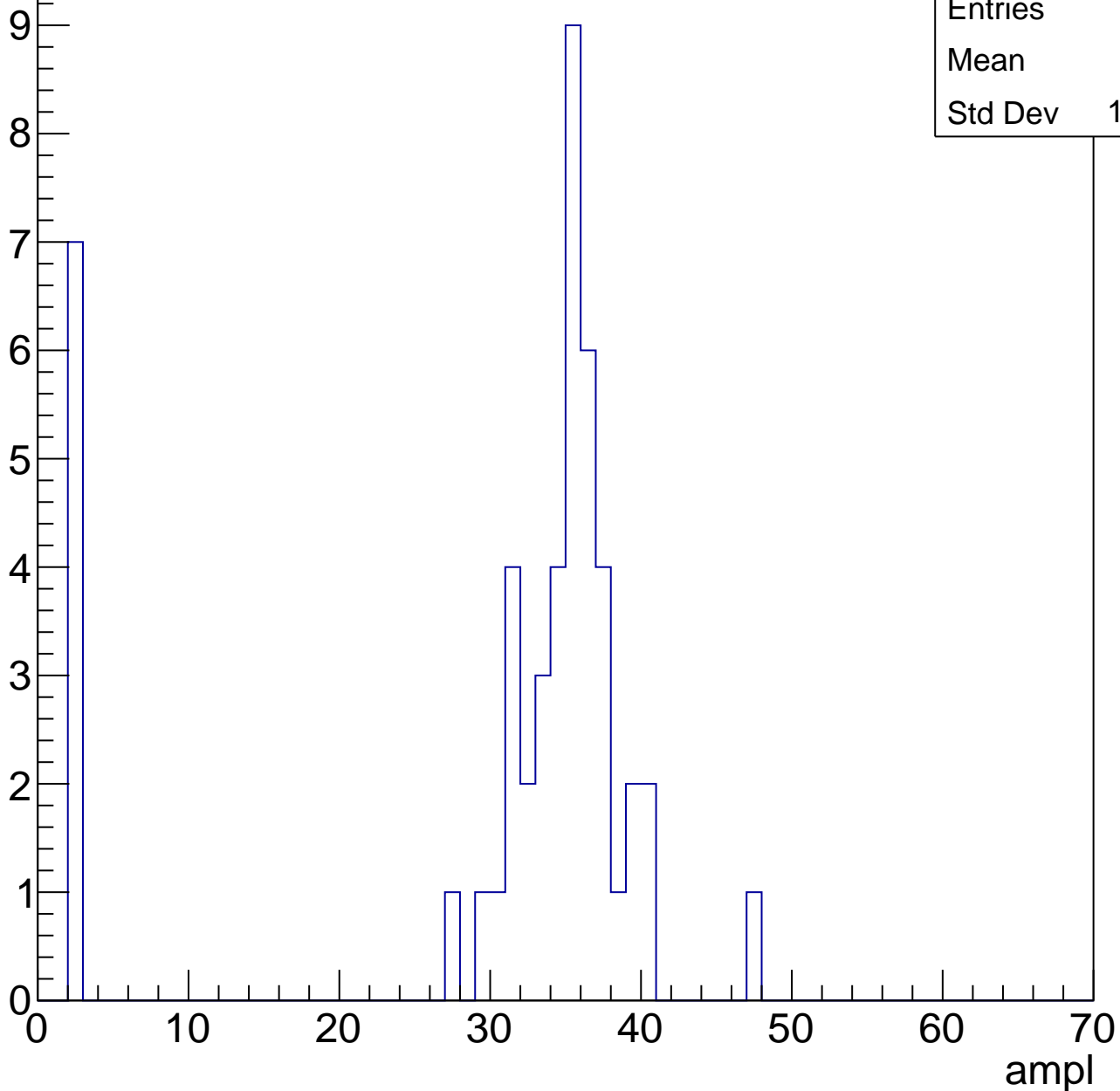


B1L103S, U12-ch82, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	48
Mean	30.1
Std Dev	12.04



B1L103S, U12-ch82, adc2

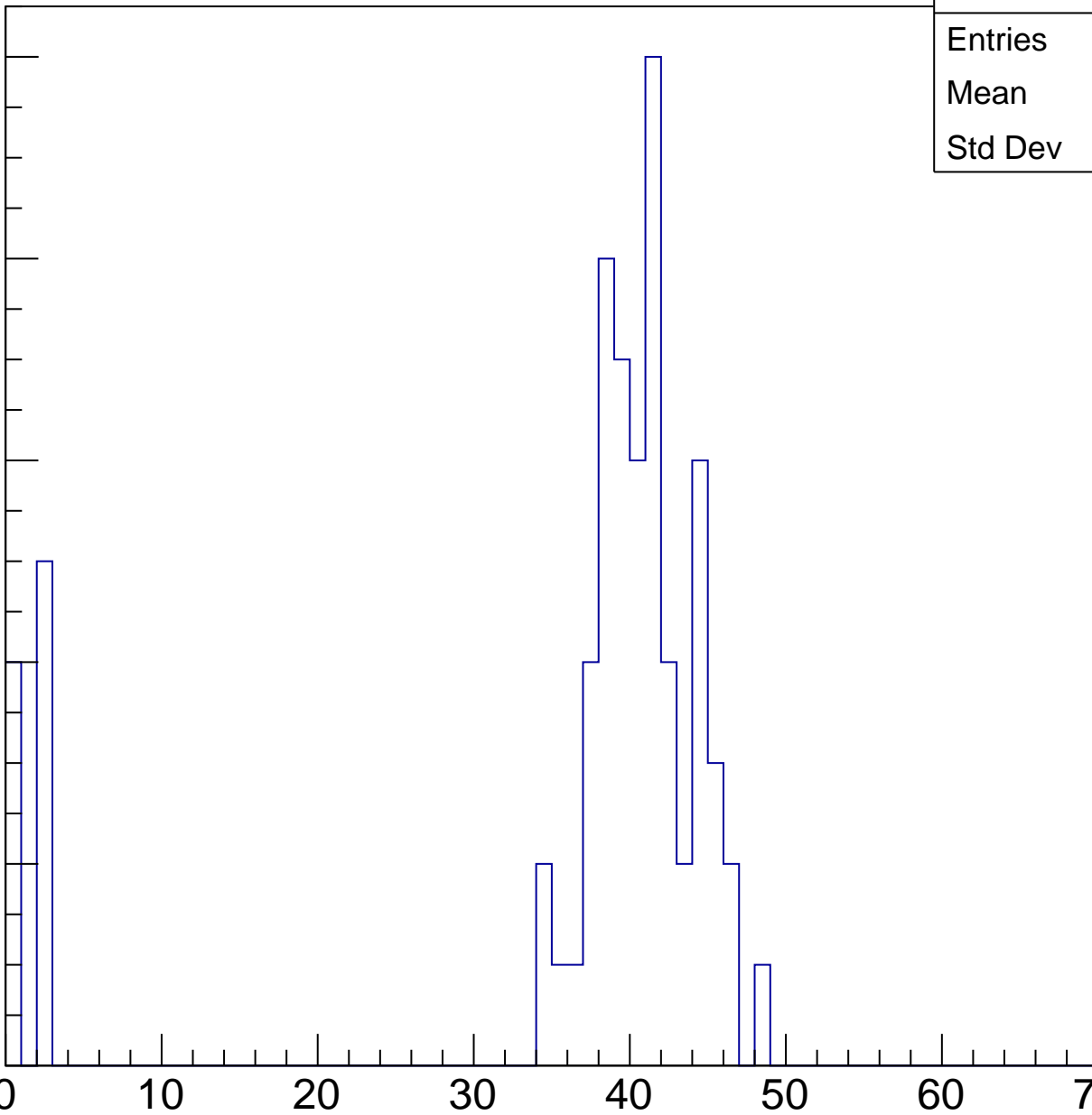
calib_packv5_041523_1651.root, FC#0, port C2

Entries	66
Mean	35.11
Std Dev	13.81

Entry

10
8
6
4
2
0

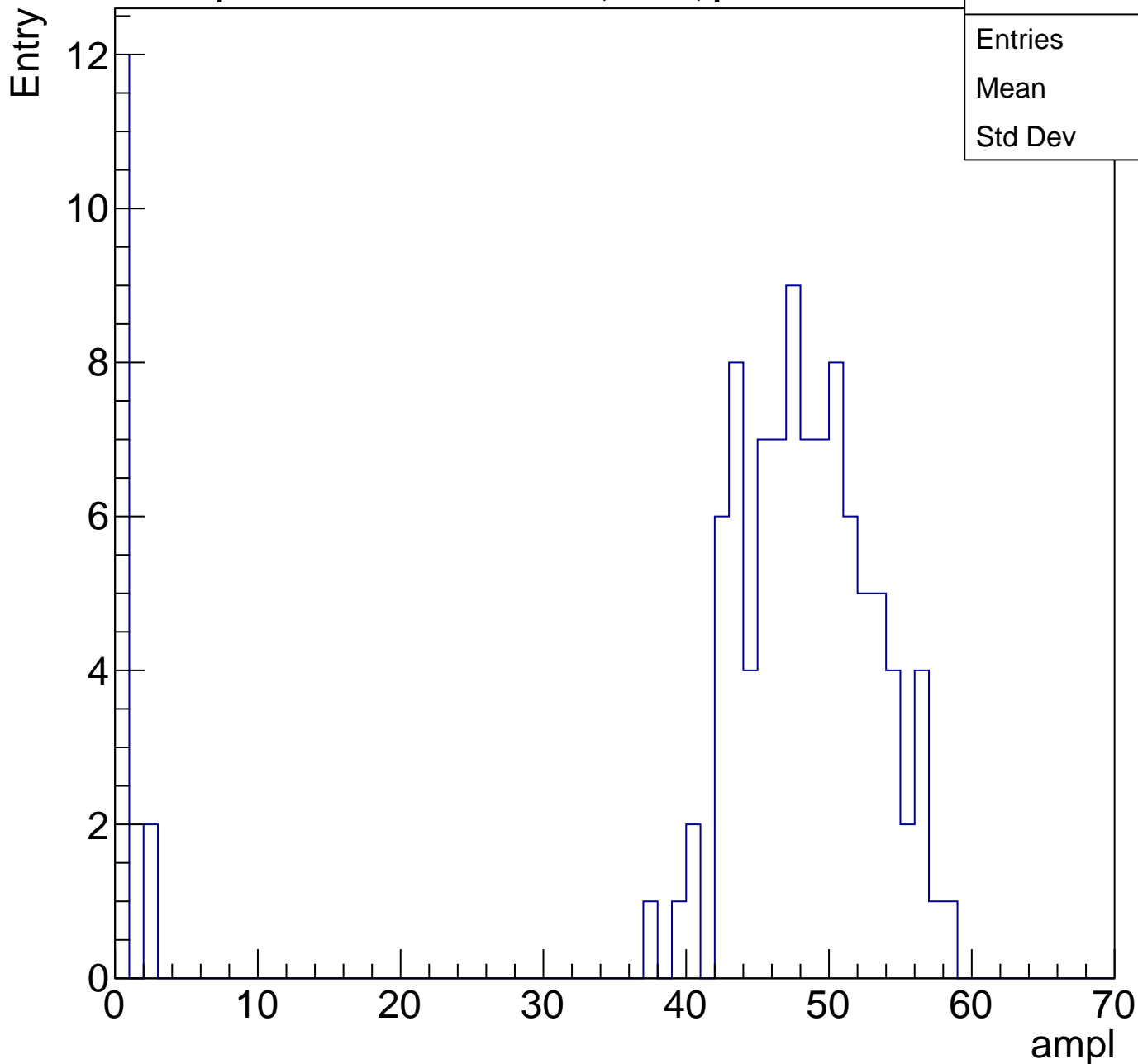
ampl



B1L103S, U12-ch82, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	109
Mean	41.9
Std Dev	16.51

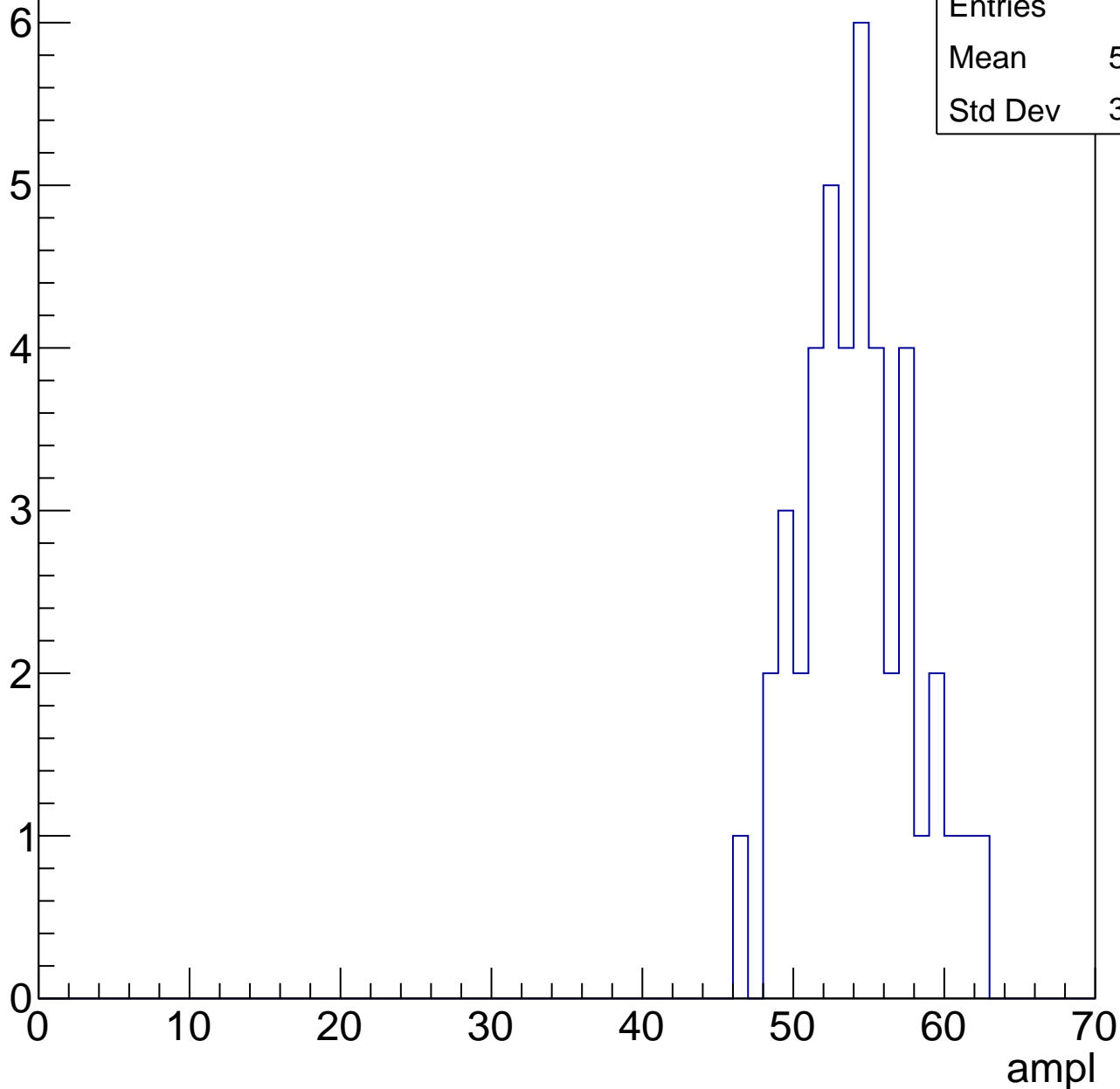


B1L103S, U12-ch82, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	43
Mean	53.67
Std Dev	3.613

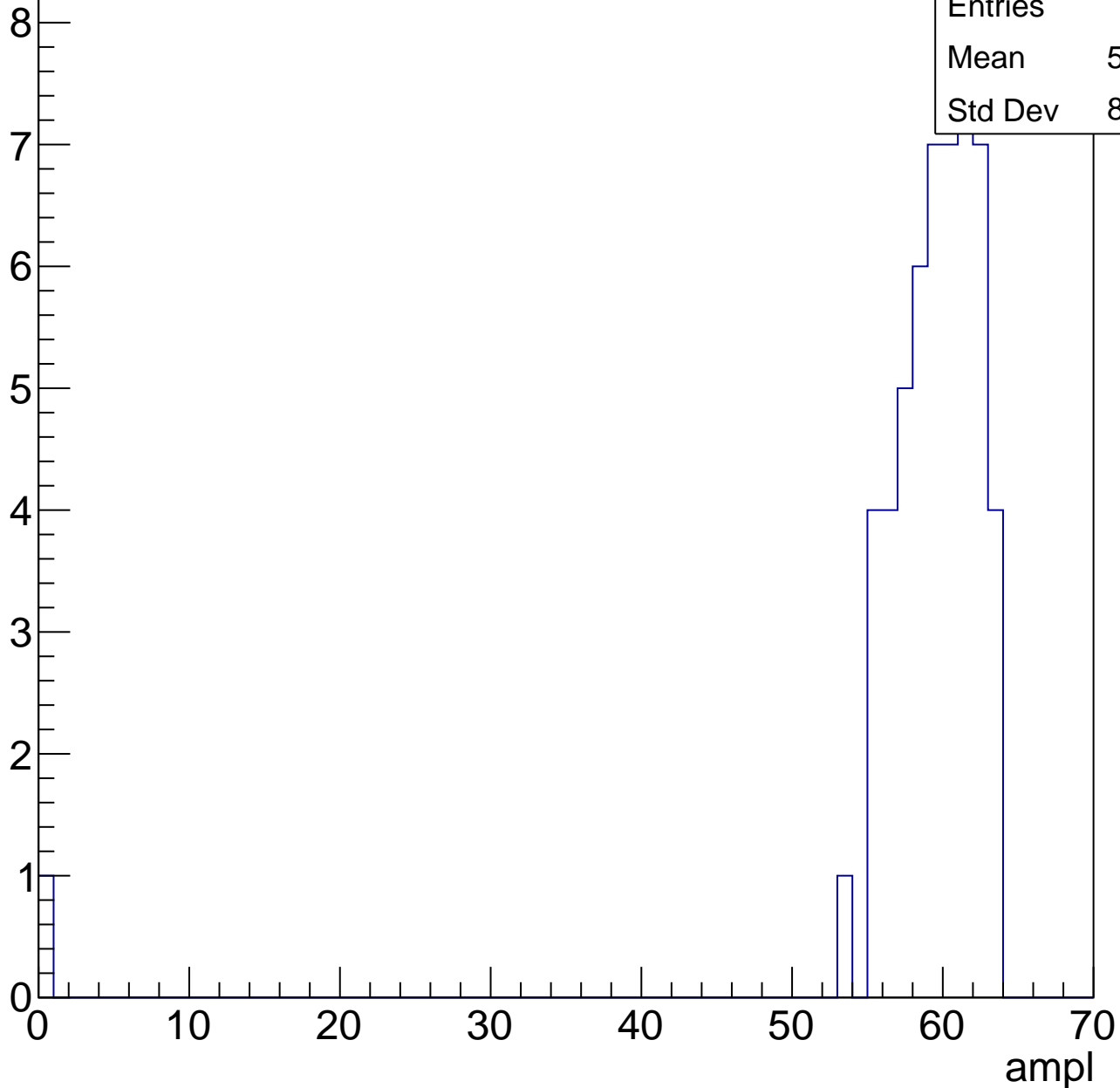


B1L103S, U12-ch82, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

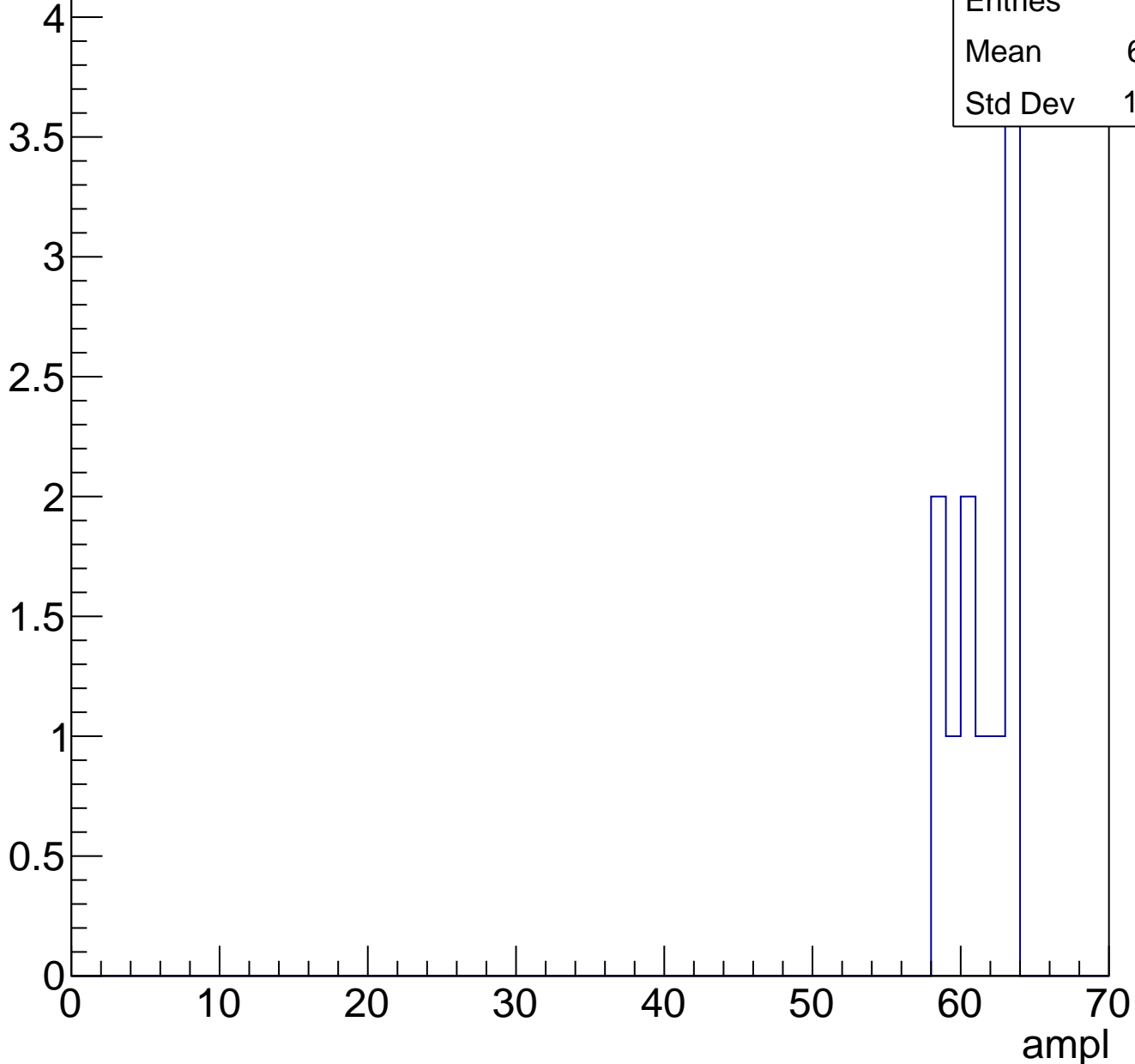
Entries	54
Mean	58.09
Std Dev	8.349



B1L103S, U12-ch82, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



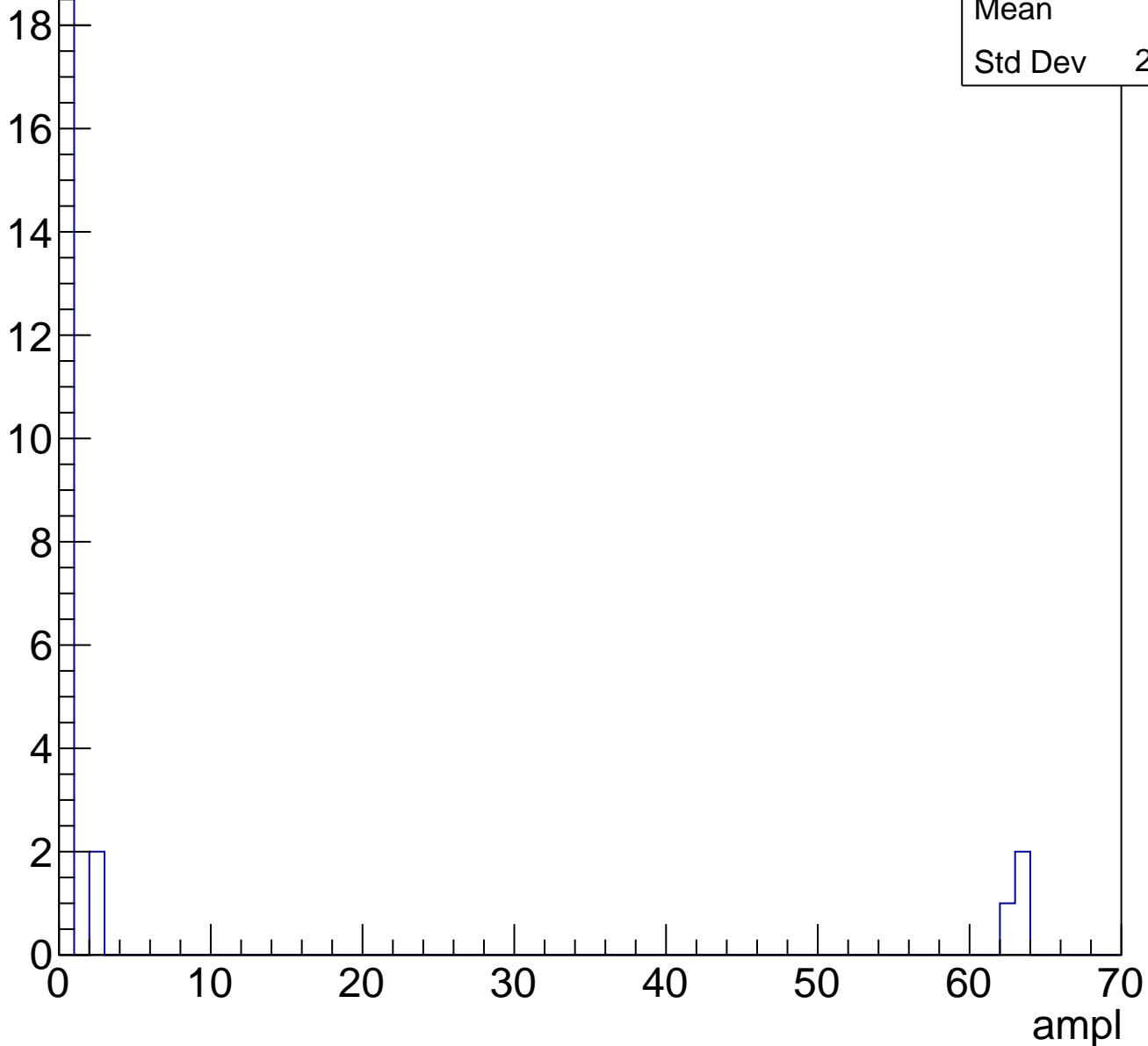
Entries	11
Mean	60.91
Std Dev	1.928

B1L103S, U12-ch82, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	24
Mean	8
Std Dev	20.67

Entry

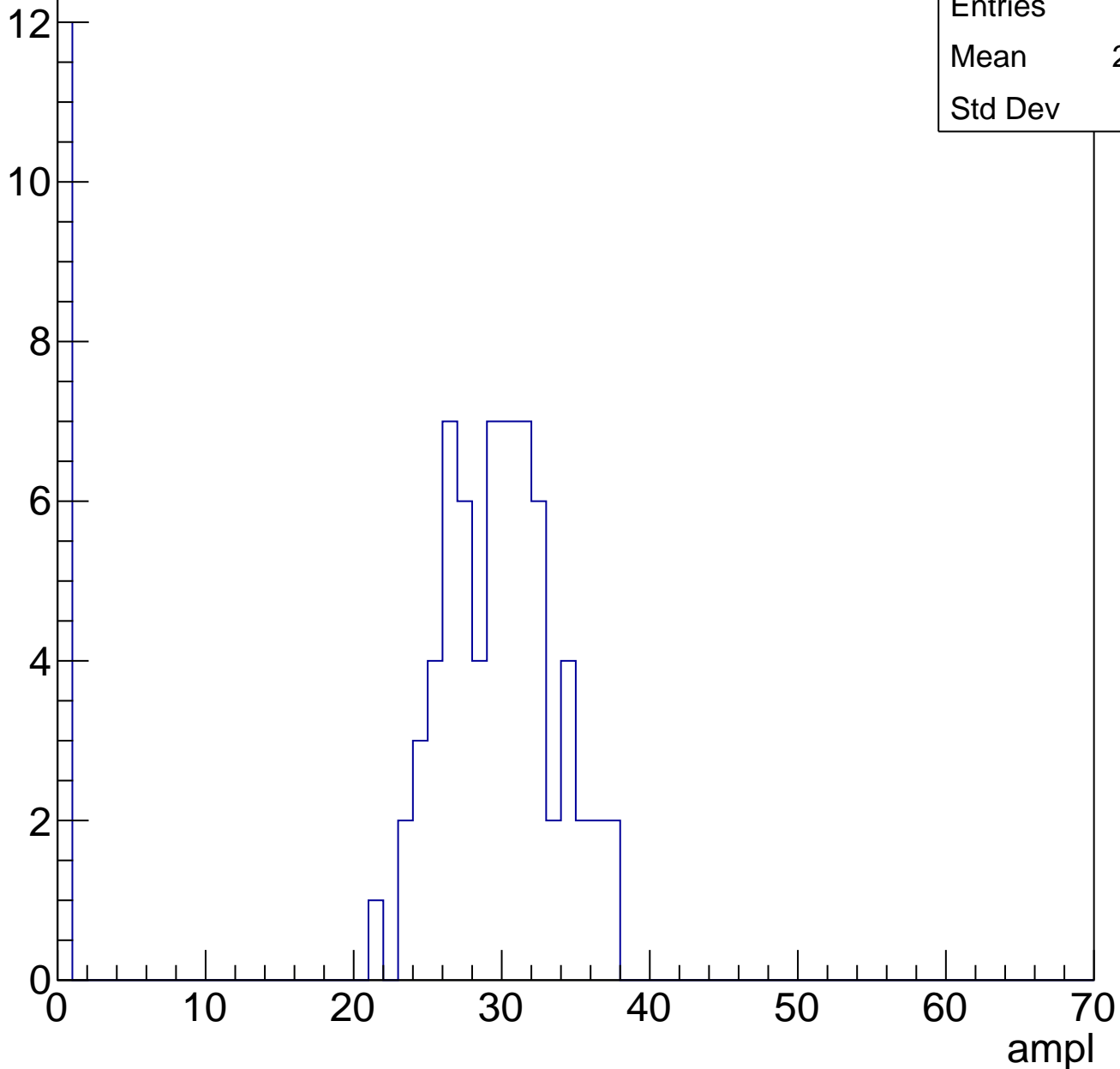


B1L103S, U12-ch83, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	78
Mean	24.81
Std Dev	11.1

Entry



B1L103S, U12-ch83, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	97
Mean	32.87
Std Dev	12.3

Entry

10

8

6

4

2

0

0

10

20

30

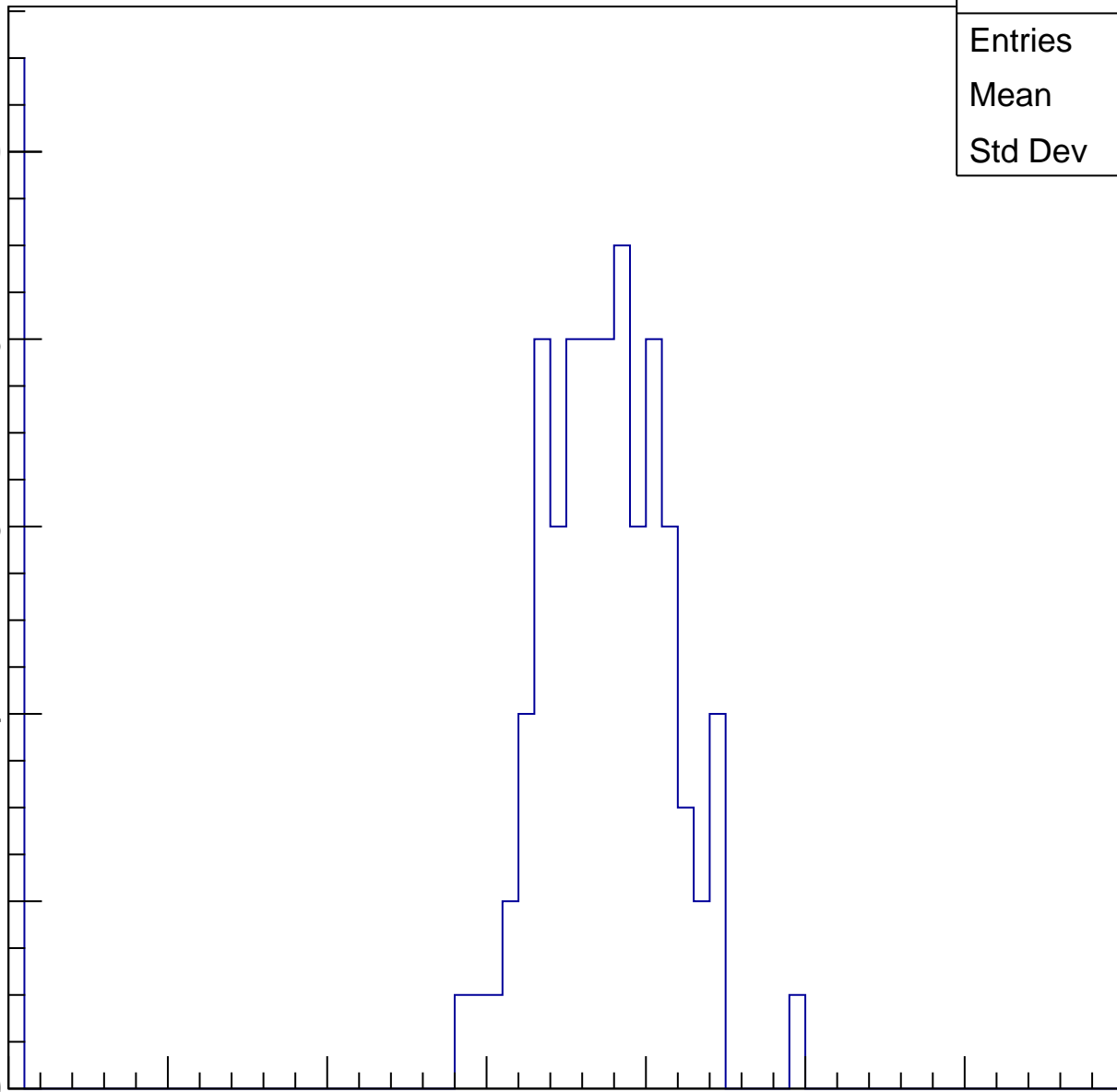
40

50

60

70

ampl

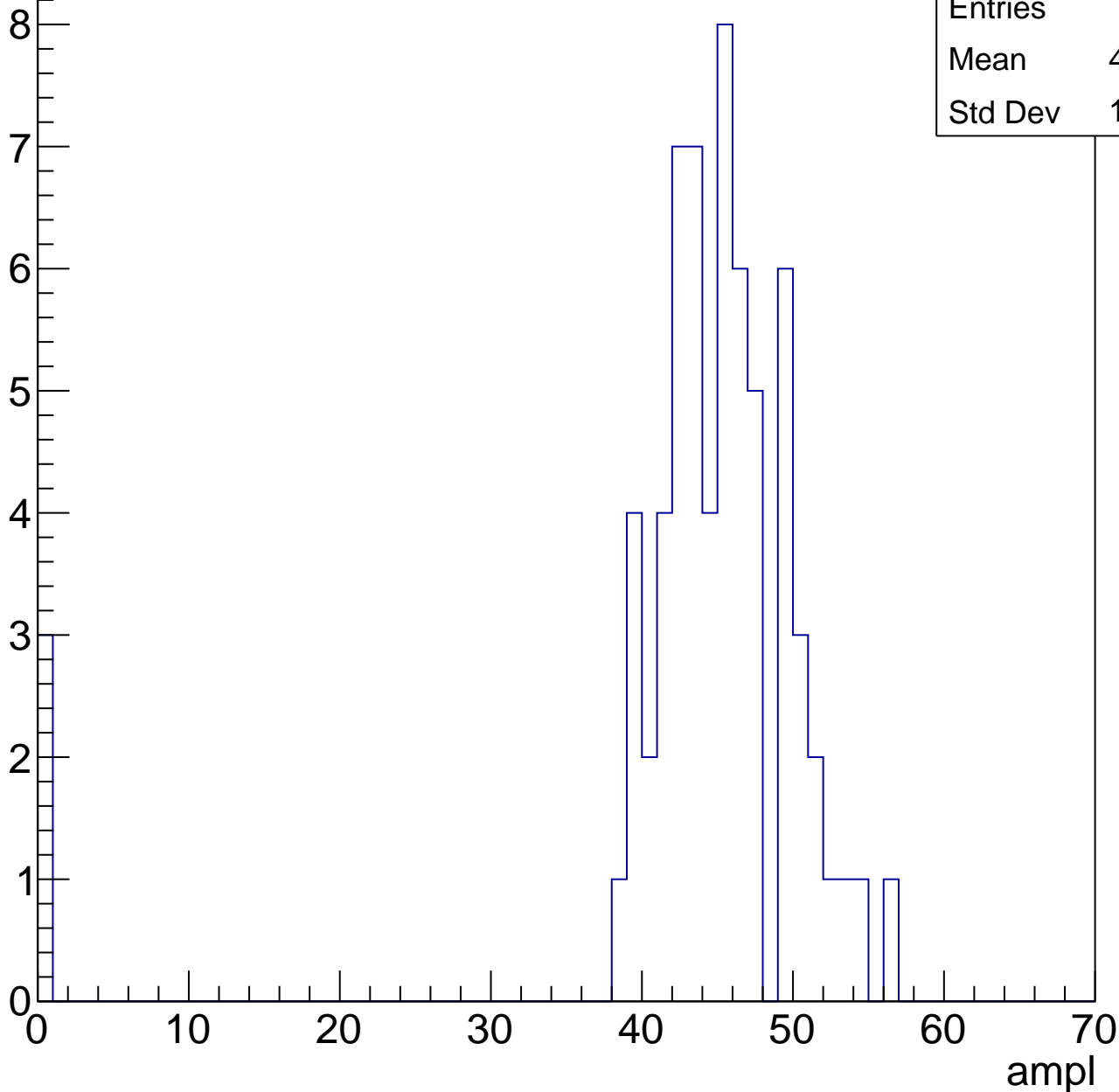


B1L103S, U12-ch83, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

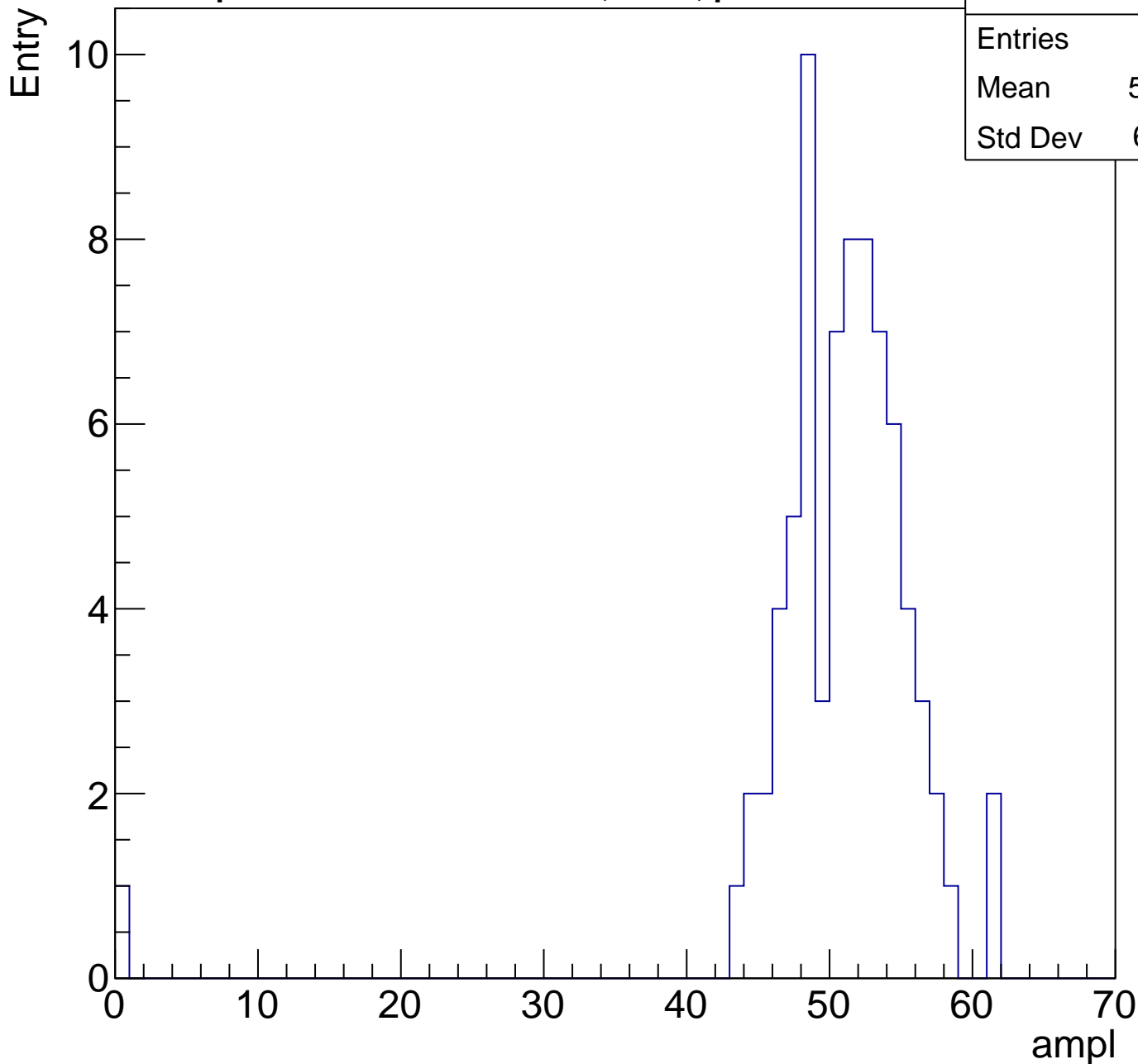
Entries	66
Mean	43.05
Std Dev	10.16



B1L103S, U12-ch83, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	76
Mean	50.24
Std Dev	6.911



B1L103S, U12-ch83, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

6

5

4

3

2

1

0

0

10

20

30

40

50

60

ampl

Entries	42
Mean	57.12
Std Dev	2.402

0

1

2

3

4

5

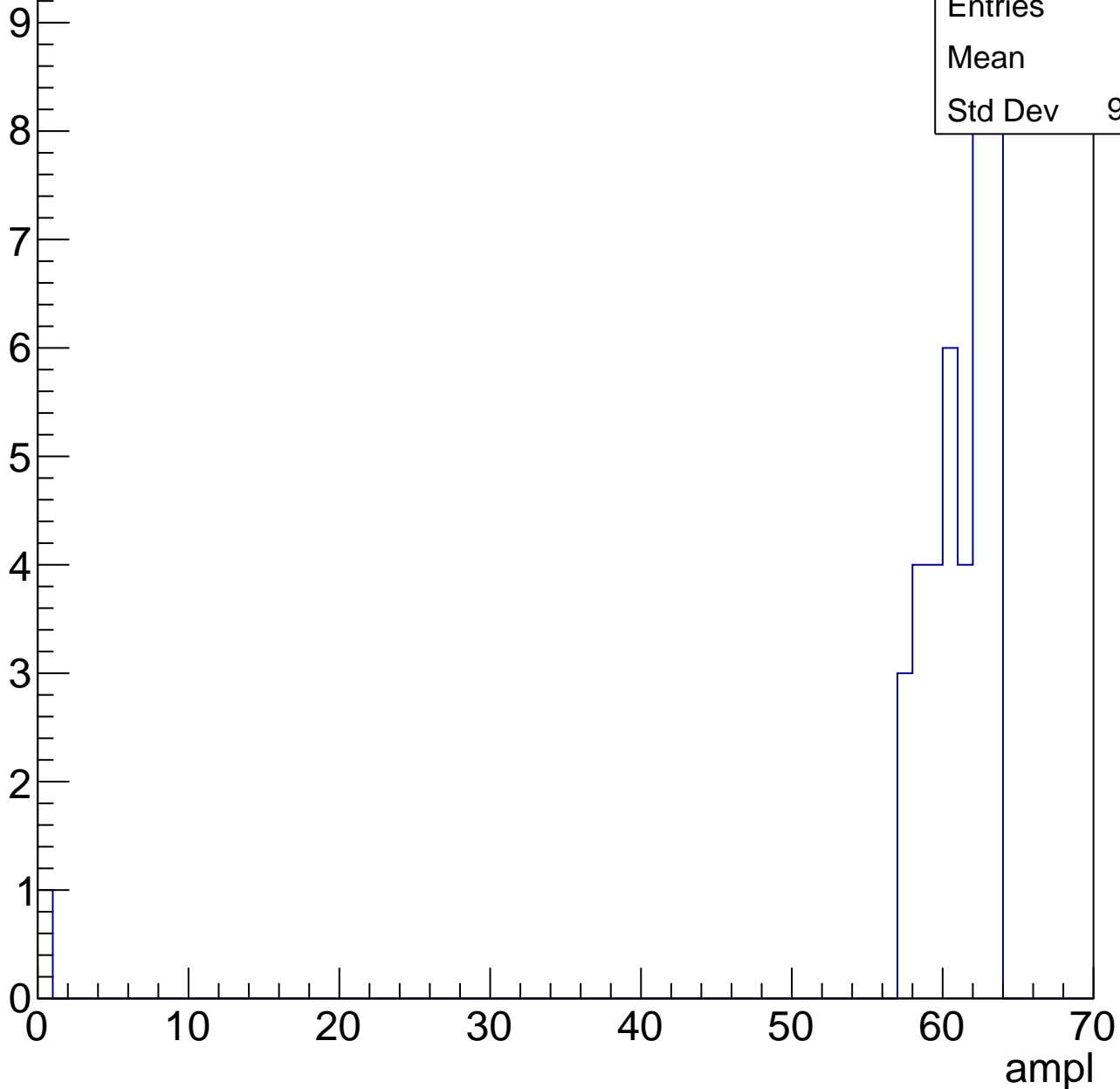
6

B1L103S, U12-ch83, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	40
Mean	59.2
Std Dev	9.673



B1L103S, U12-ch83, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch83, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U12-ch84, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	90
Mean	22.08
Std Dev	10.35

Entry

14
12
10
8
6
4
2
0

0

10

20

30

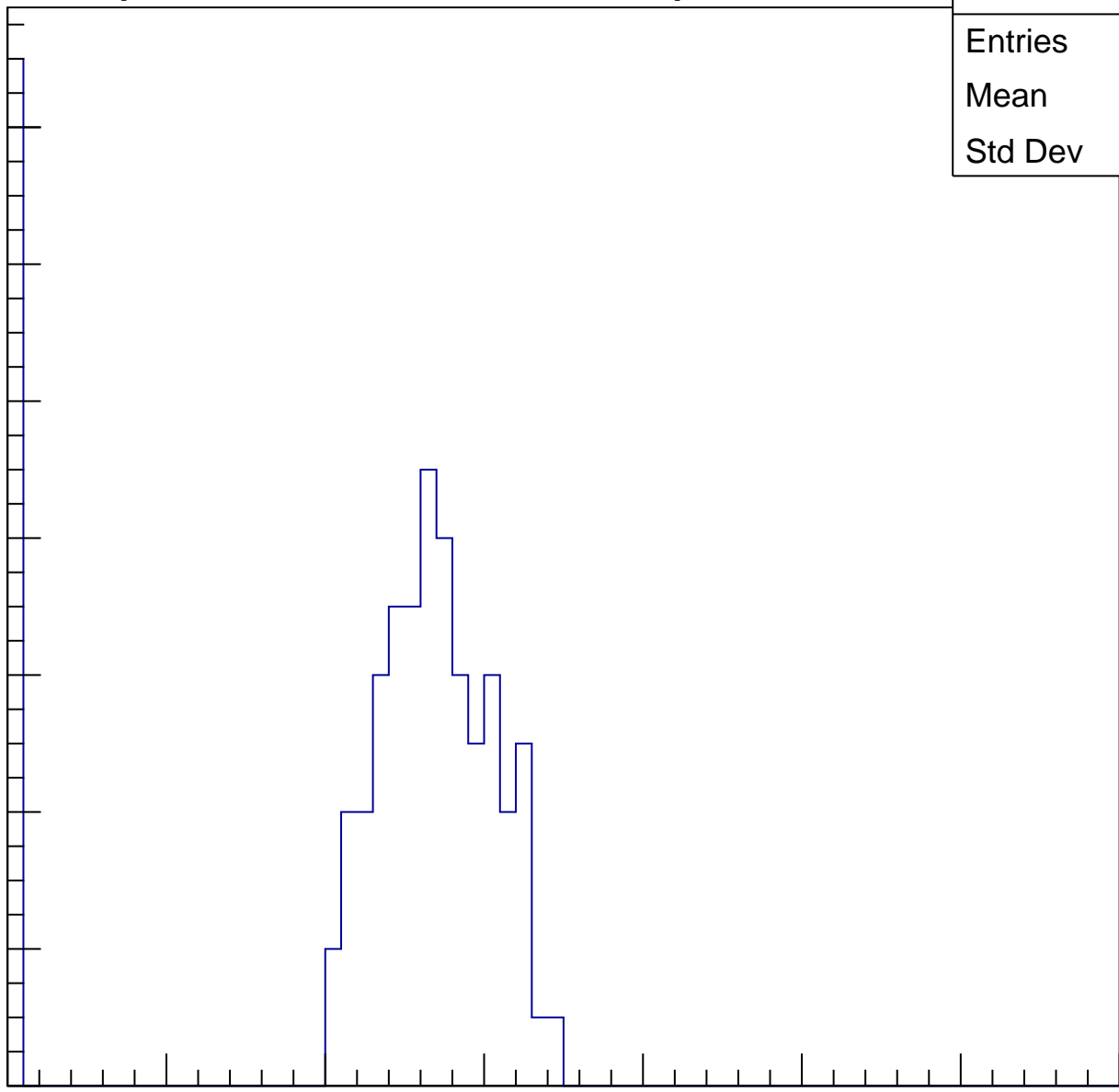
40

50

60

70

ampl

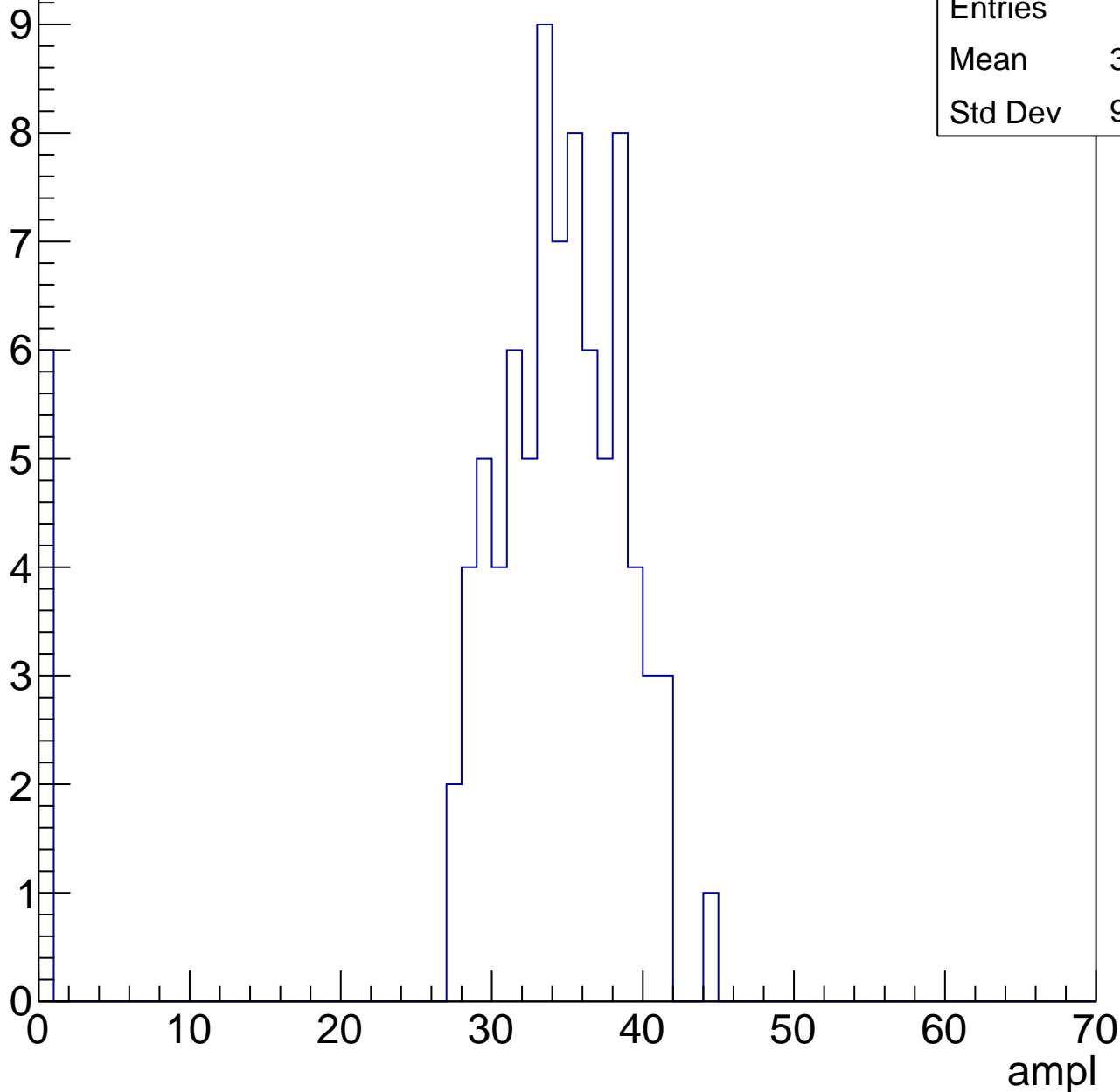


B1L103S, U12-ch84, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	86
Mean	31.86
Std Dev	9.472

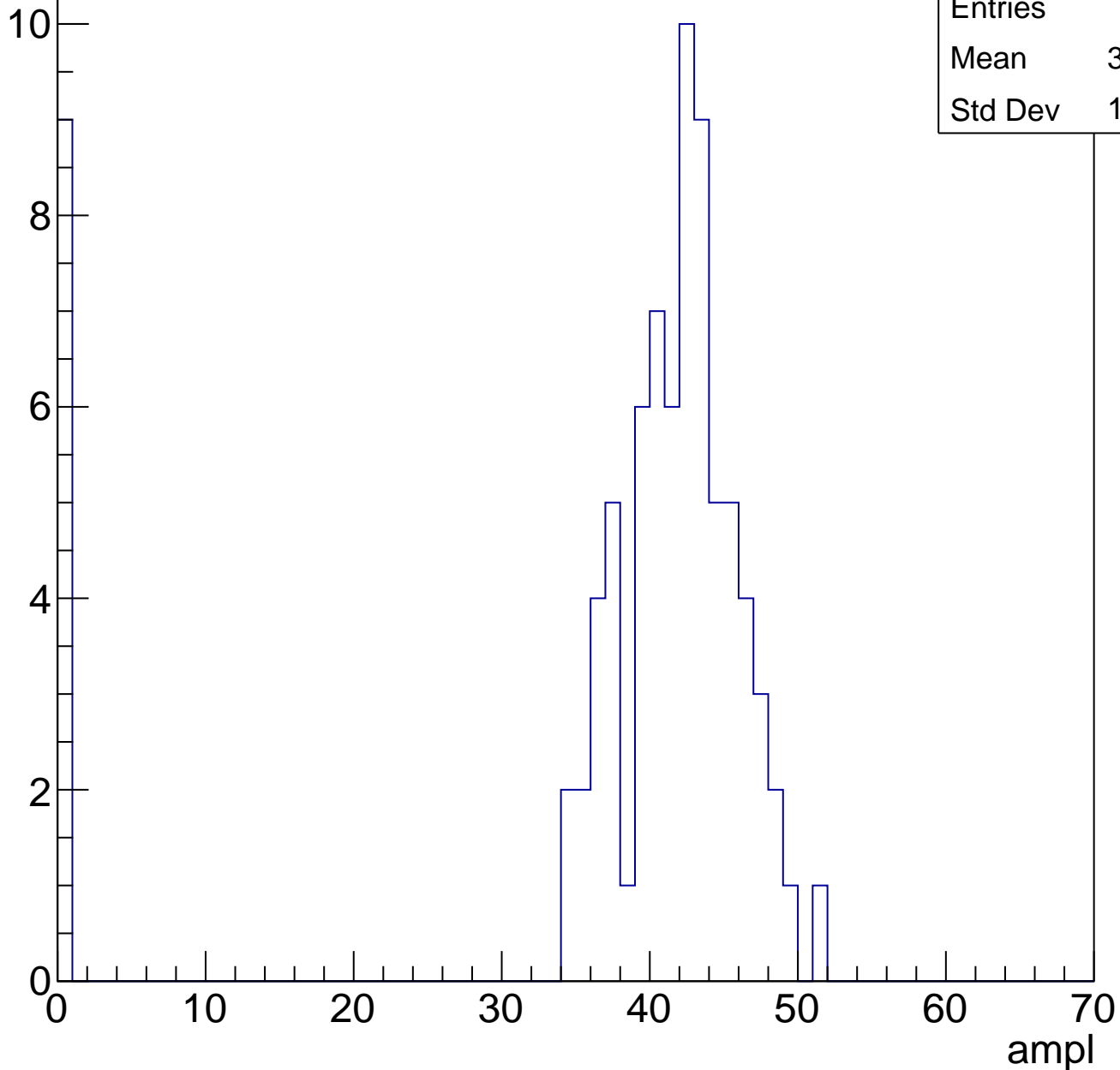


B1L103S, U12-ch84, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	82
Mean	37.05
Std Dev	13.47

Entry

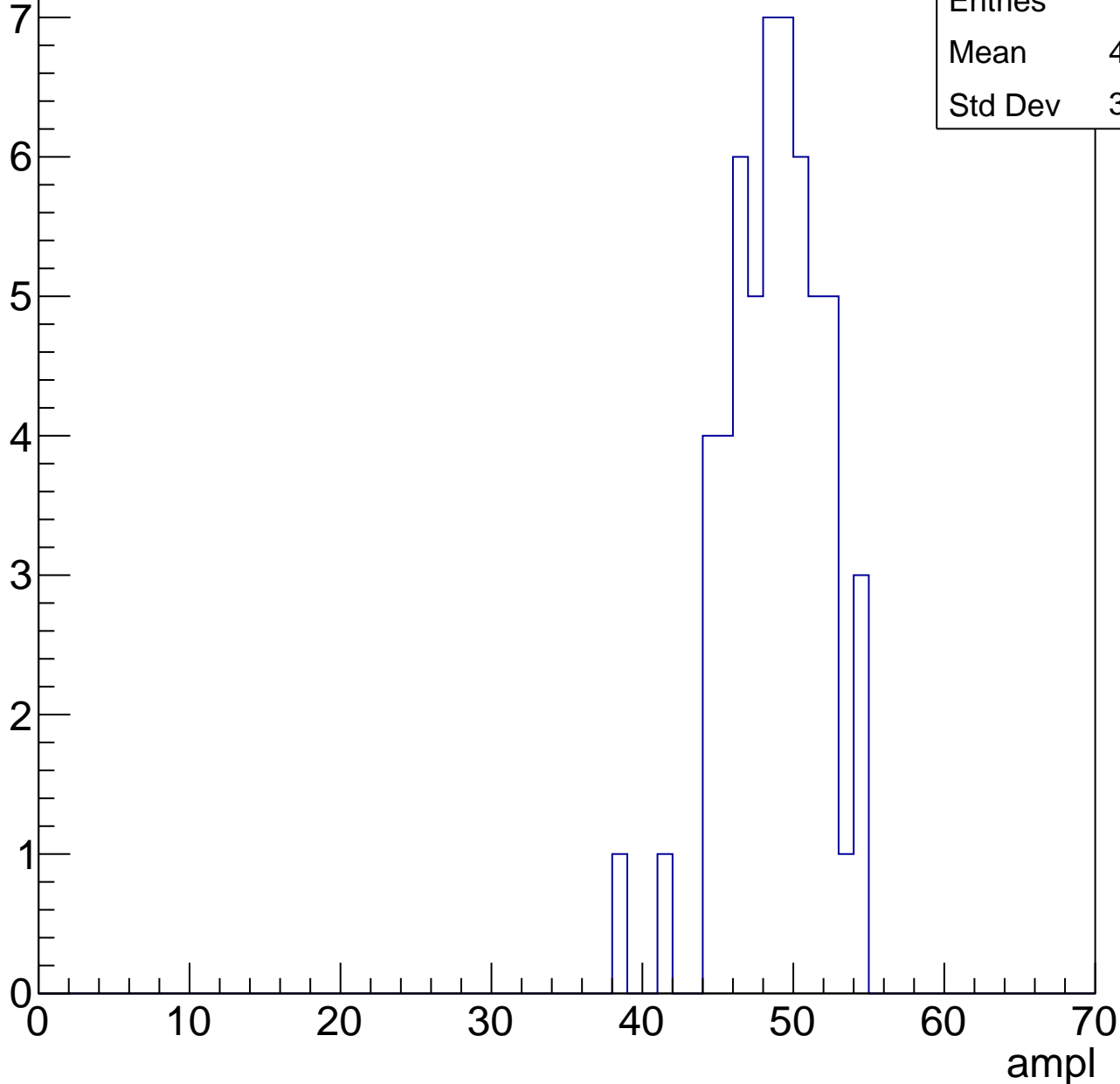


B1L103S, U12-ch84, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	48.27
Std Dev	3.199

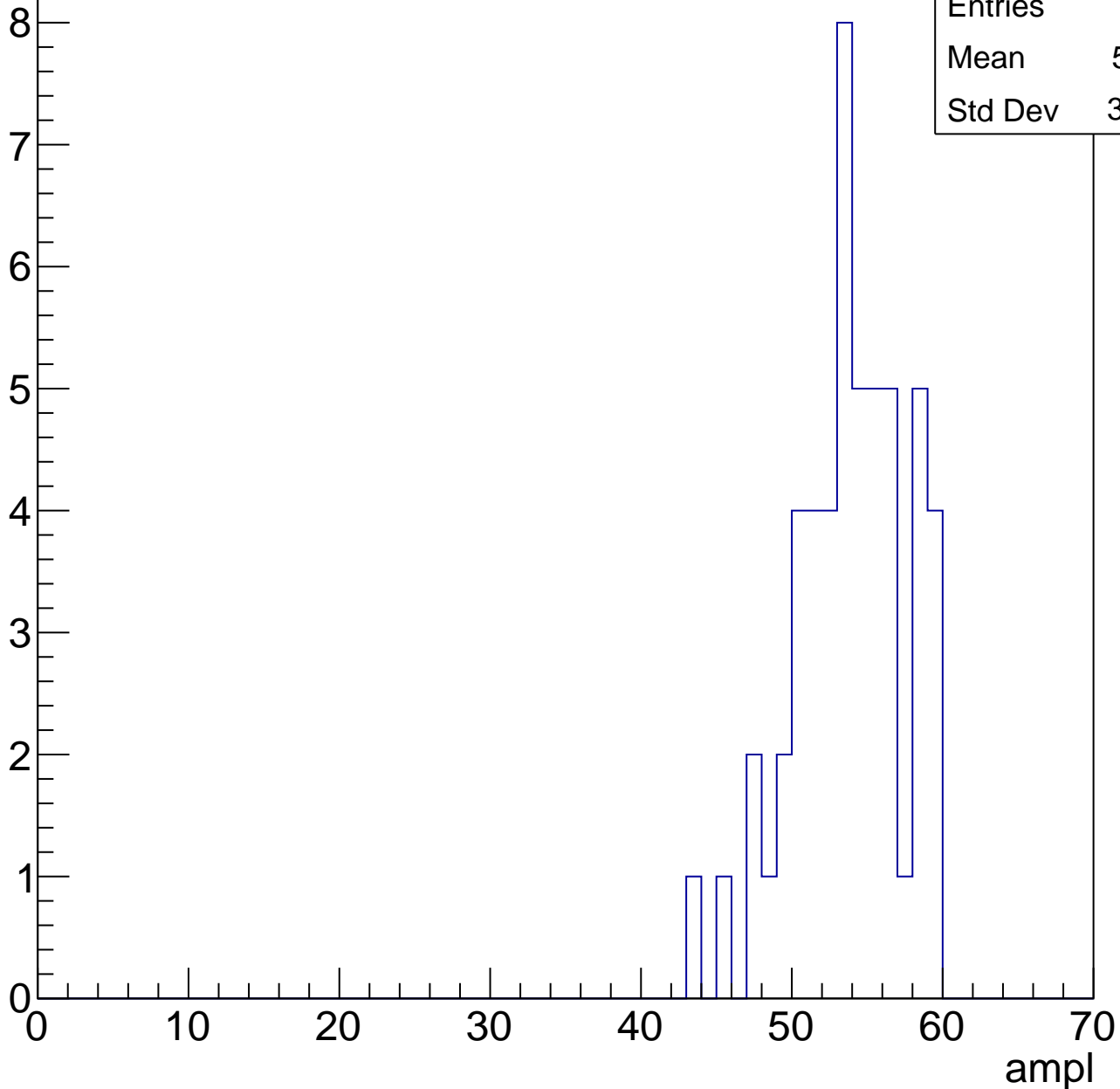


B1L103S, U12-ch84, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

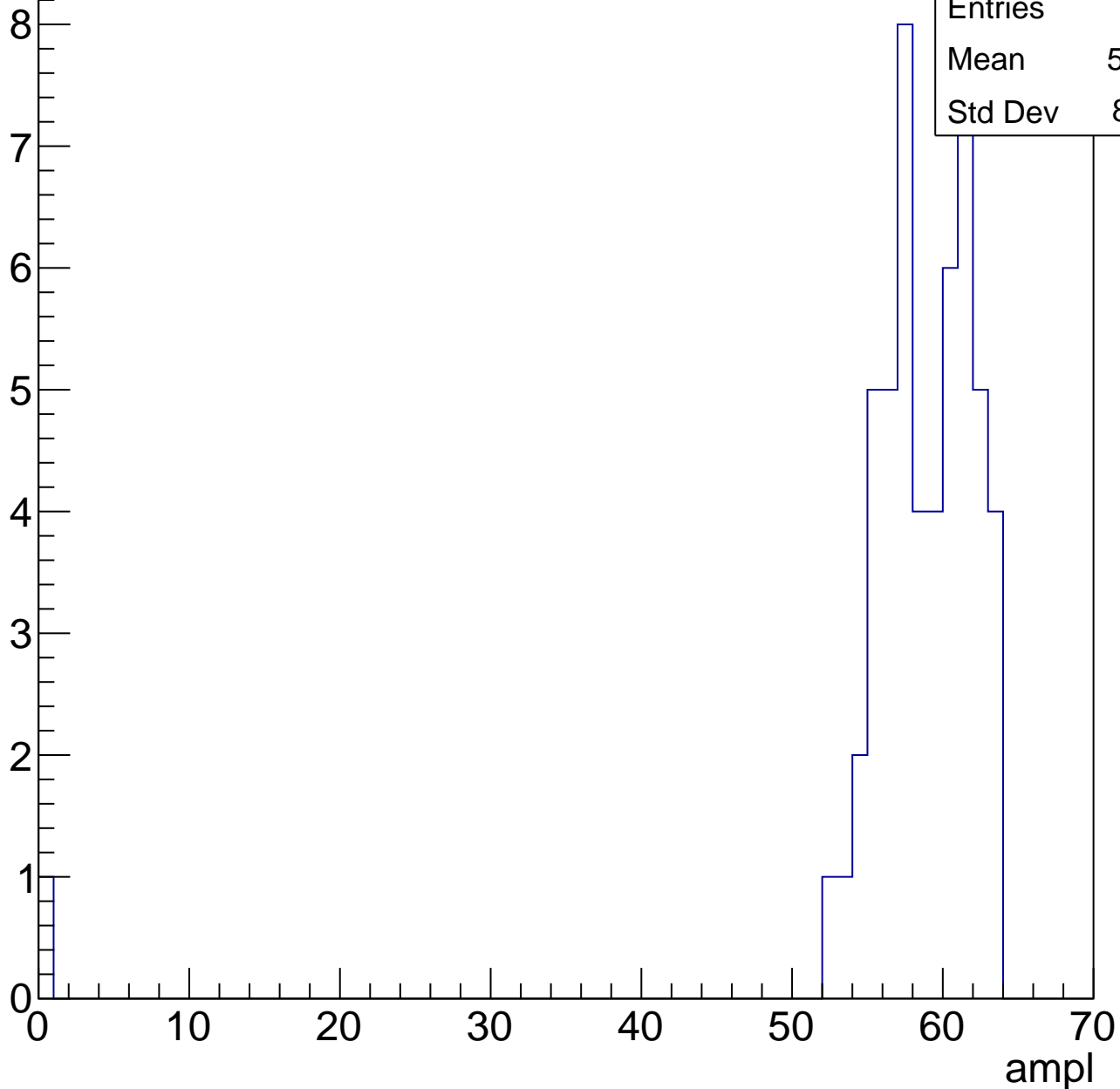
Entries	52
Mean	53.31
Std Dev	3.667



B1L103S, U12-ch84, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

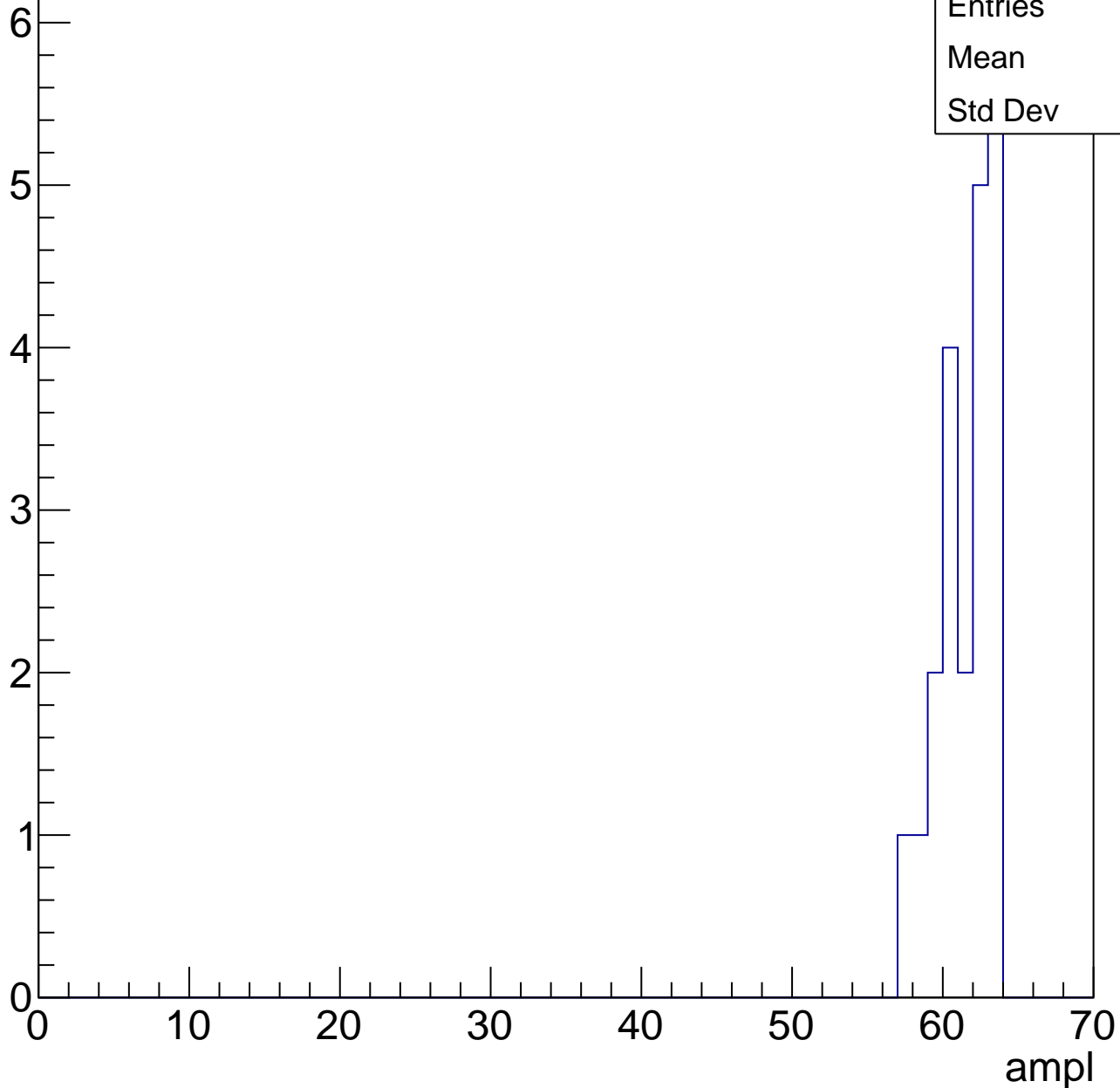


B1L103S, U12-ch84, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	21
Mean	61.1
Std Dev	1.77



B1L103S, U12-ch84, adc7

calib_packv5_041523_1651.root, FC#0, port C2

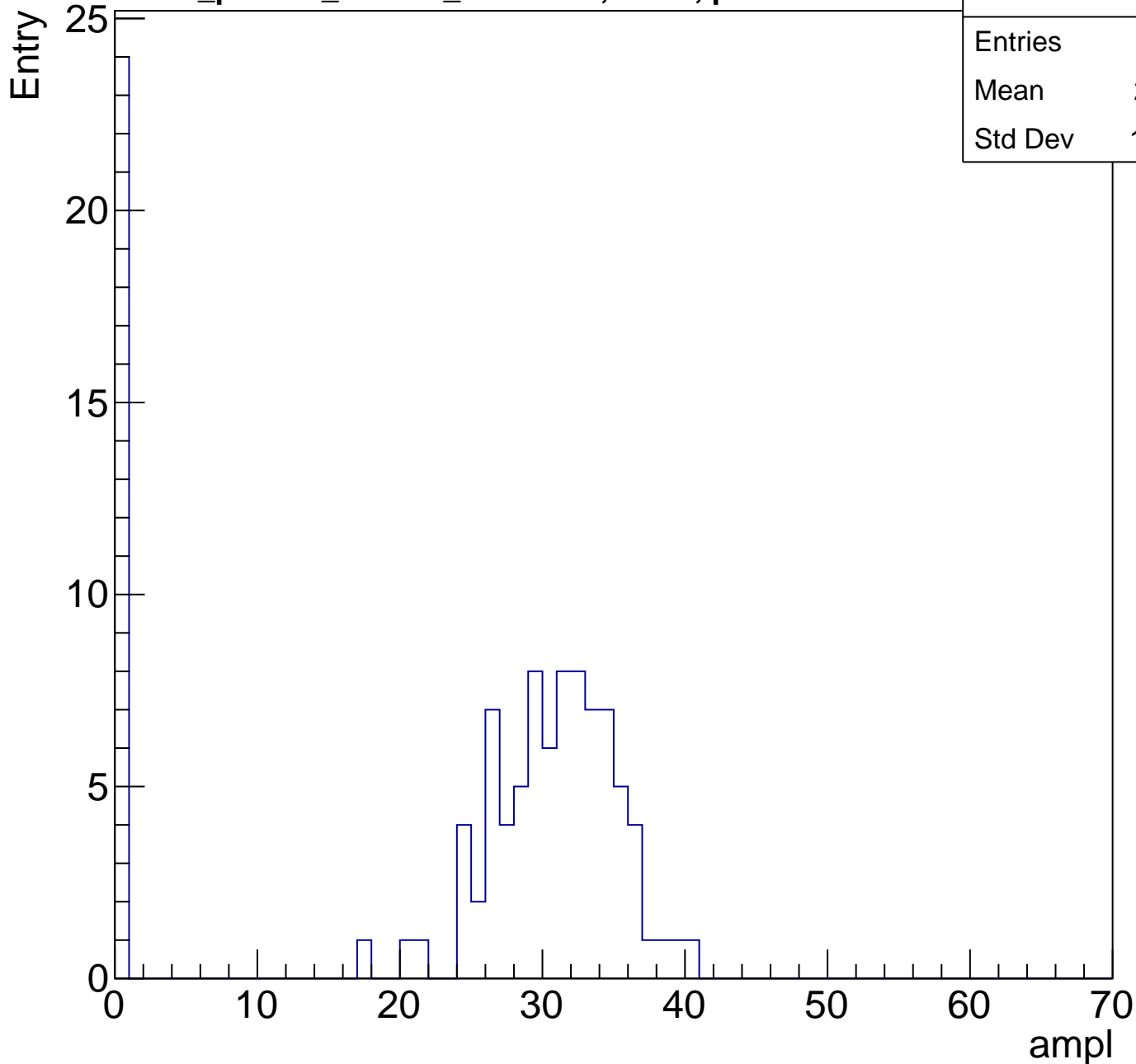
Entry



B1L103S, U12-ch85, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	106
Mean	23.51
Std Dev	13.26

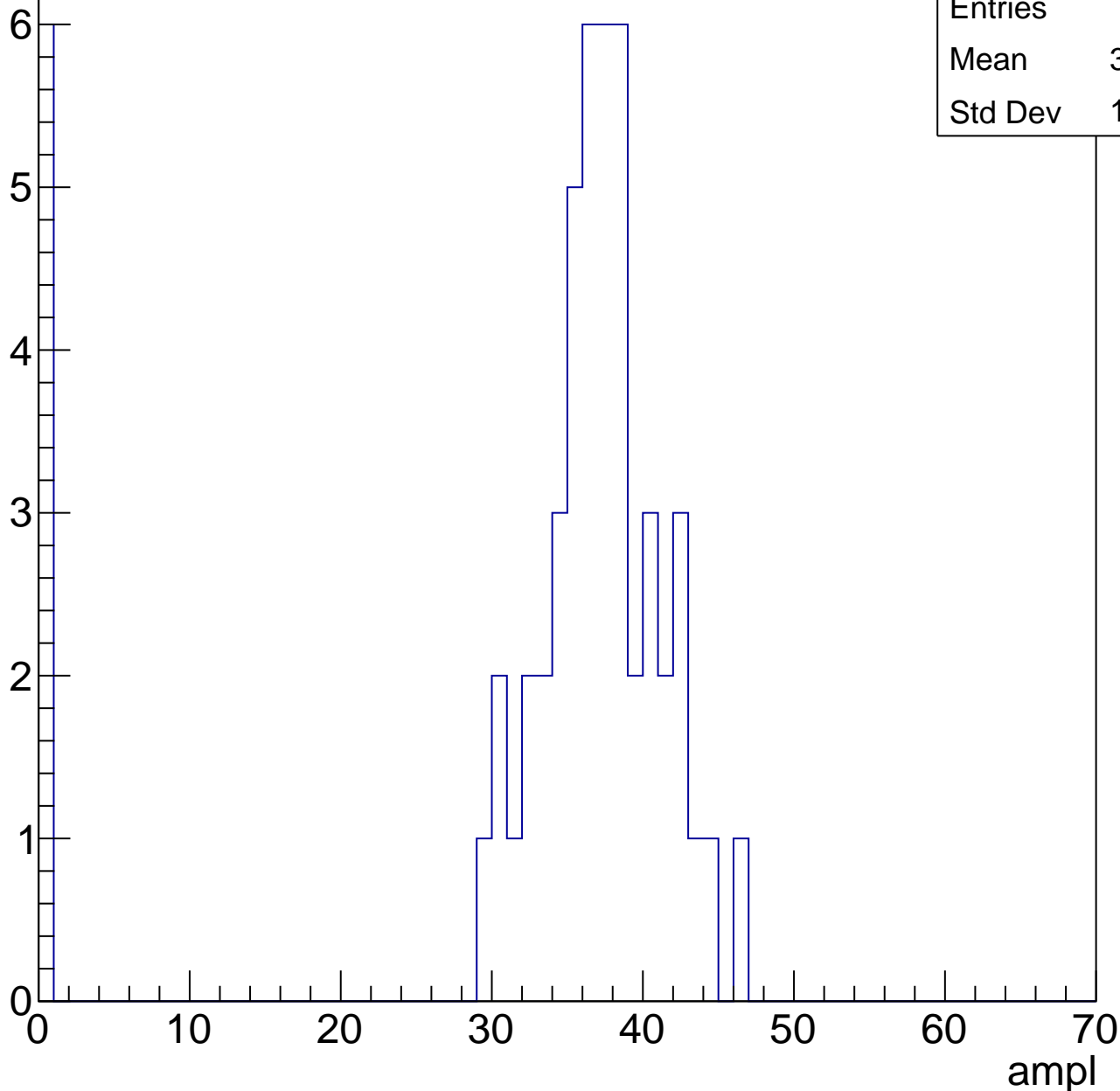


B1L103S, U12-ch85, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

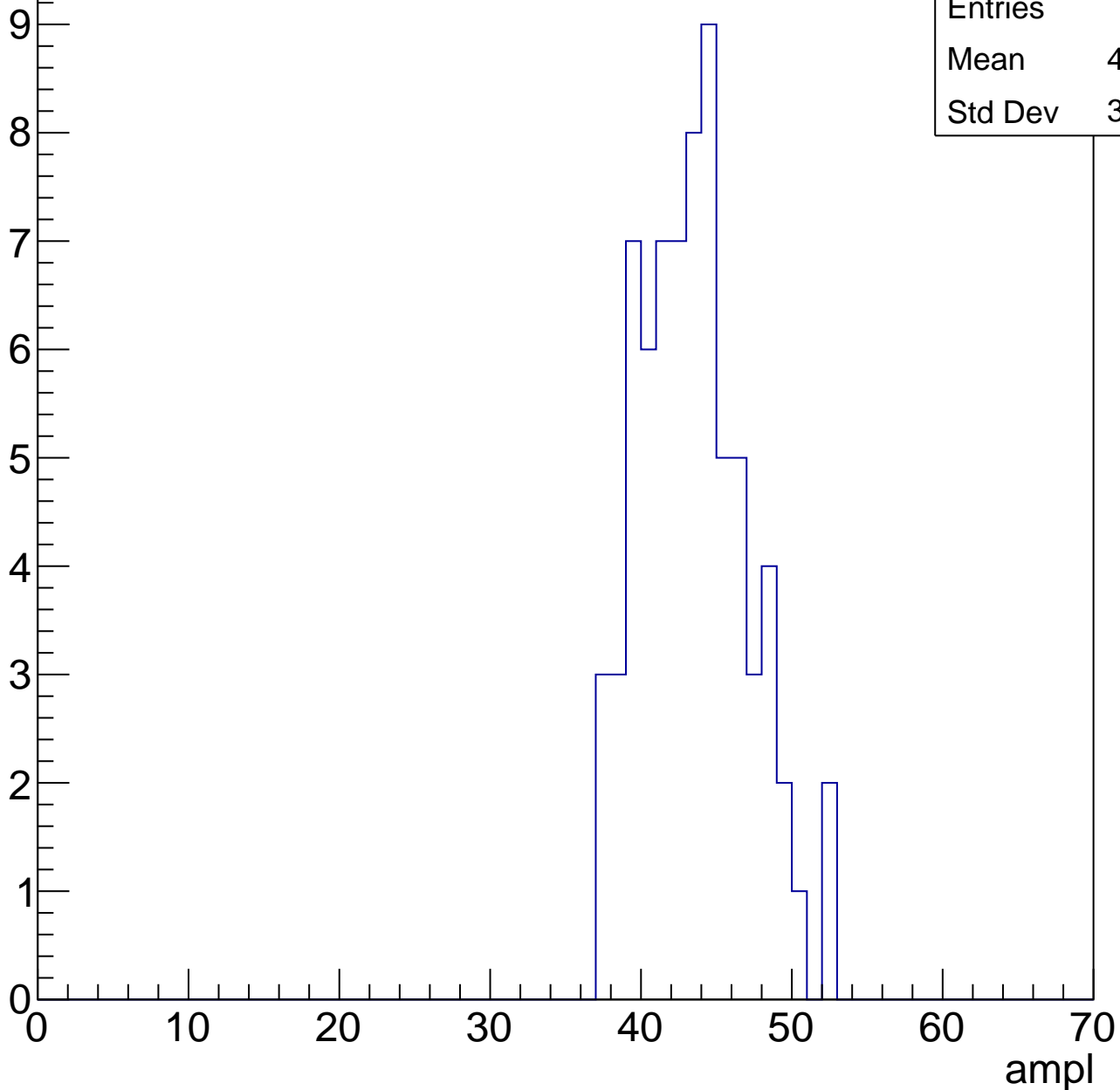
Entries	53
Mean	32.68
Std Dev	12.19



B1L103S, U12-ch85, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

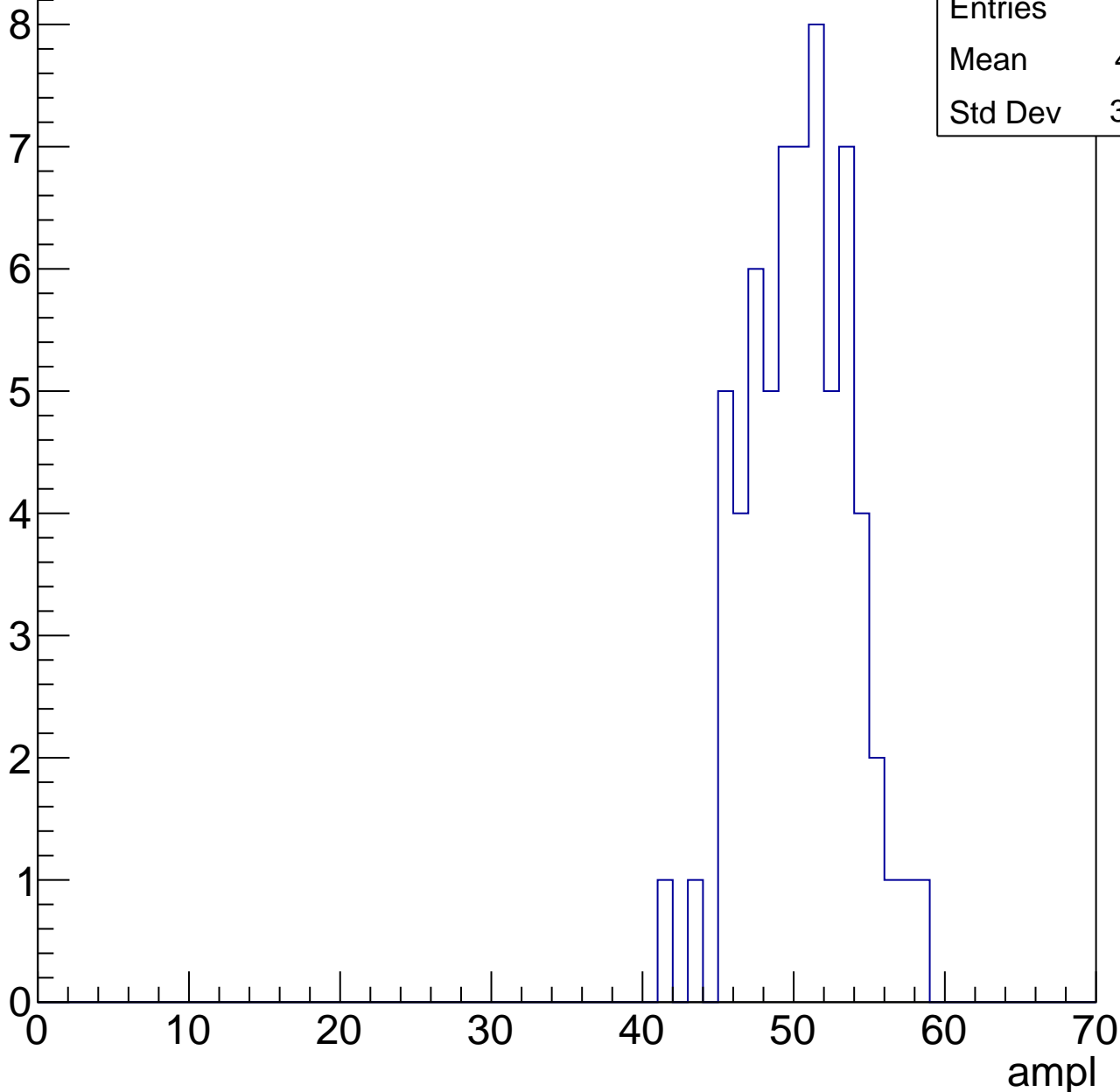


B1L103S, U12-ch85, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	49.91
Std Dev	3.405

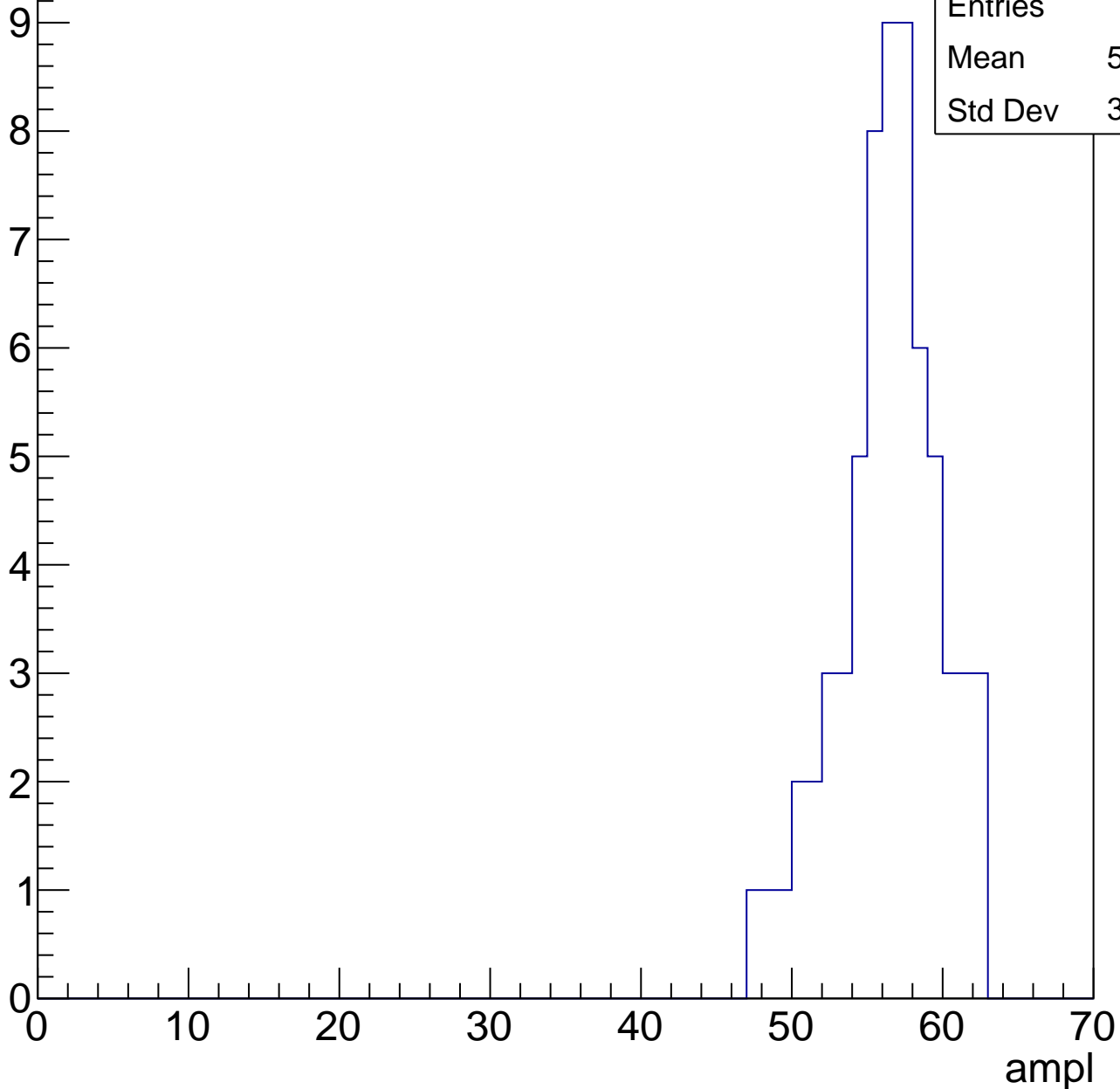


B1L103S, U12-ch85, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	55.94
Std Dev	3.372

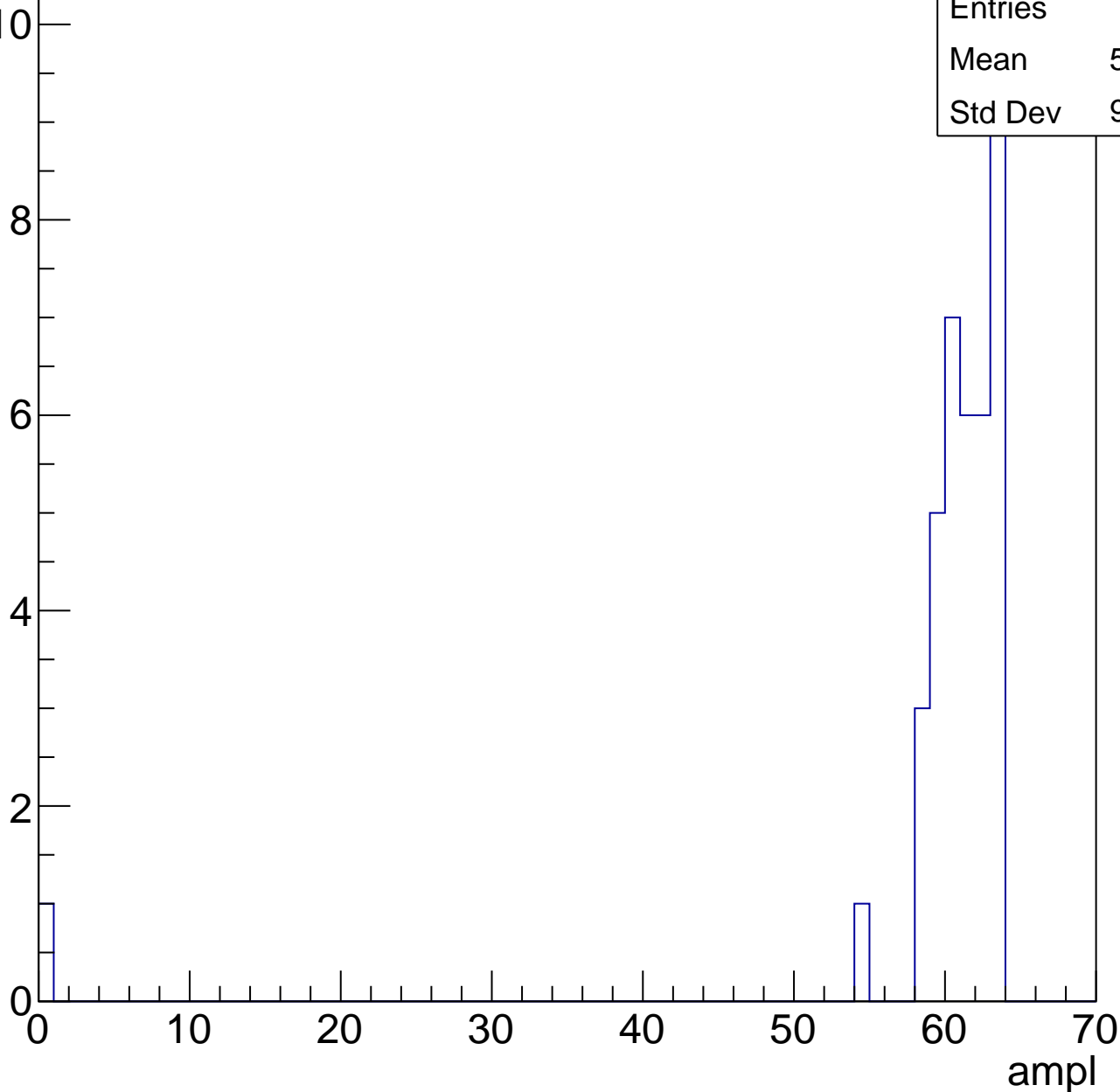


B1L103S, U12-ch85, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	39
Mean	59.26
Std Dev	9.808



B1L103S, U12-ch85, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch85, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

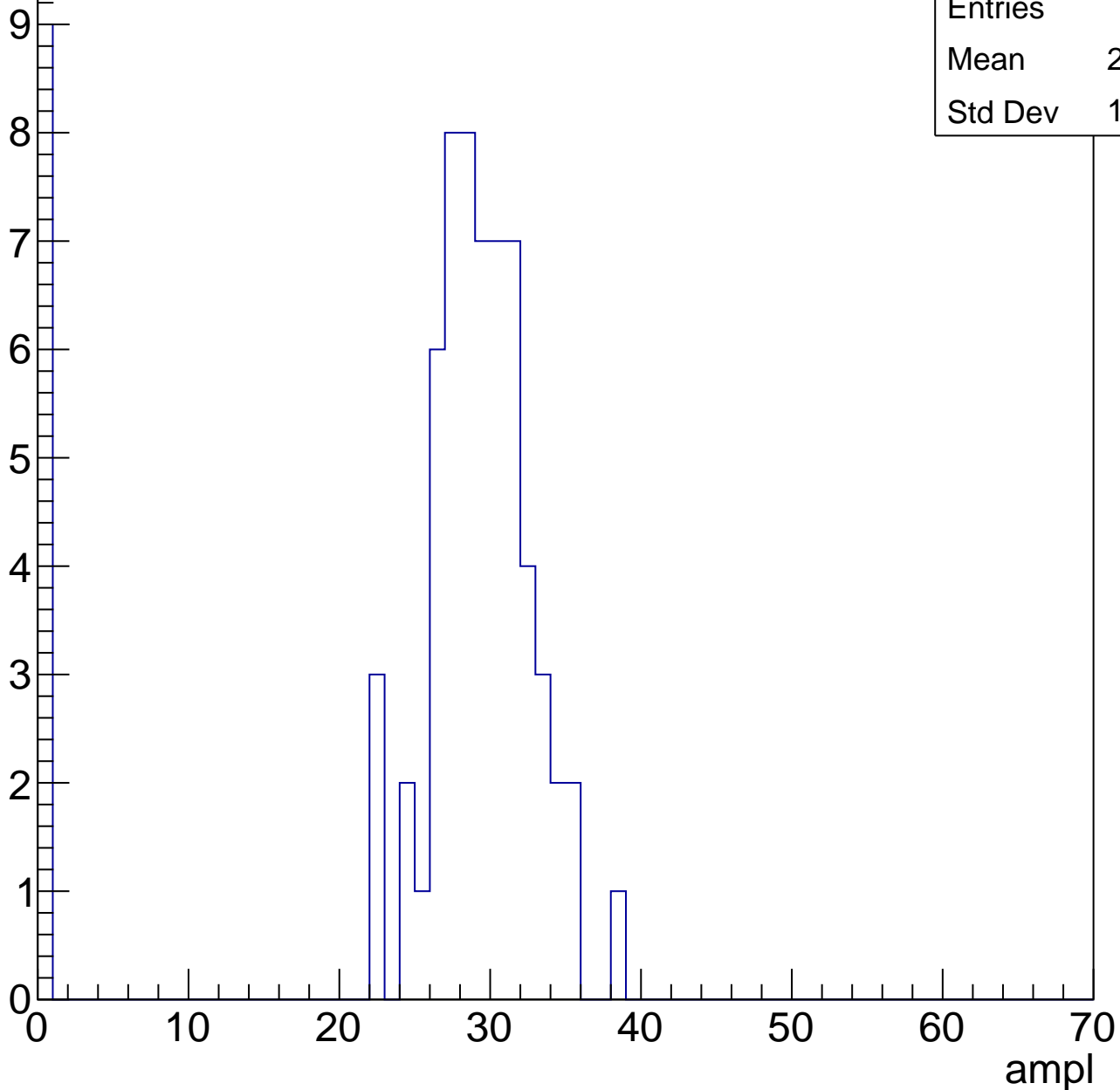


B1L103S, U12-ch86, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	25.26
Std Dev	10.15

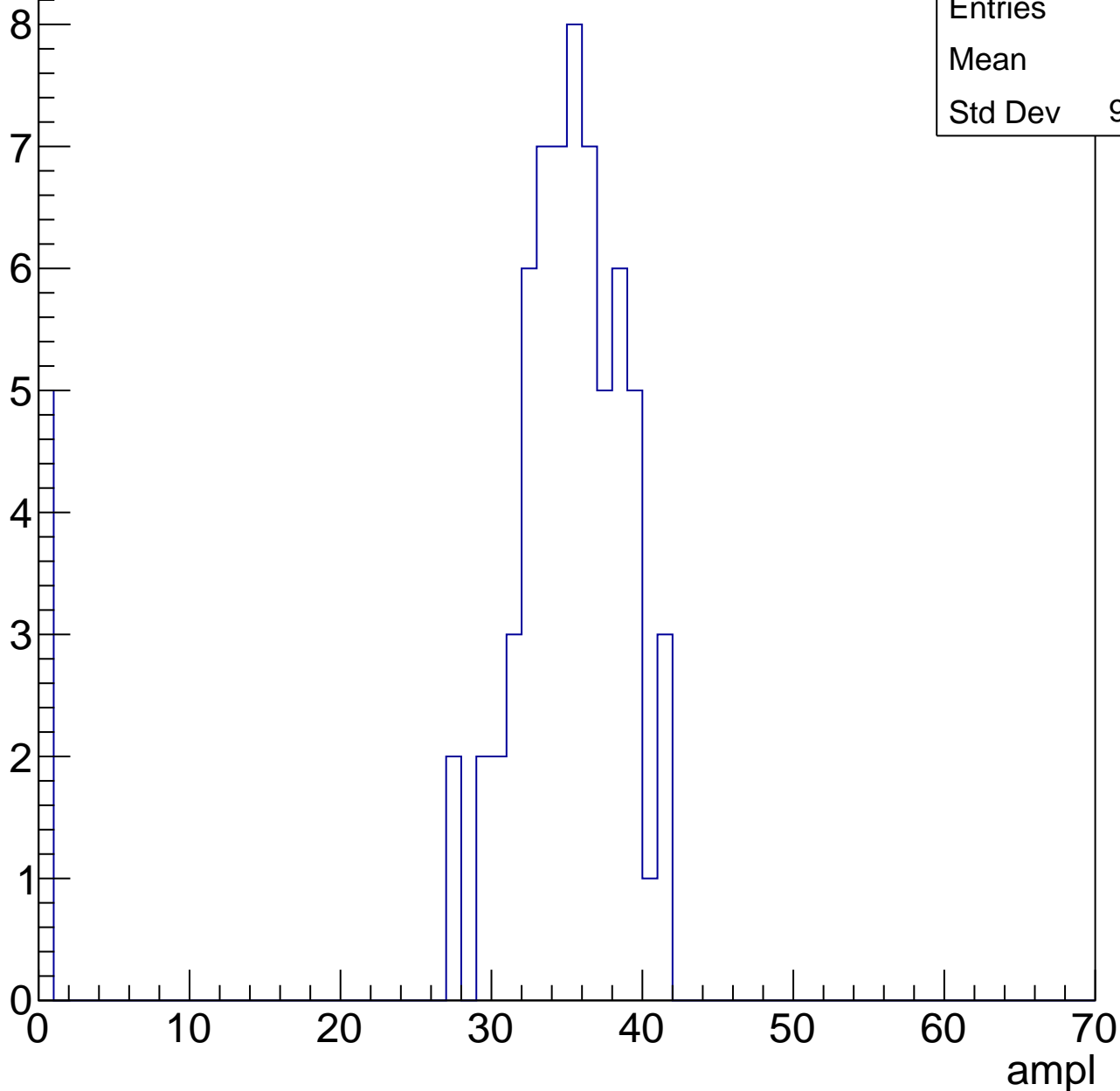


B1L103S, U12-ch86, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	32.3
Std Dev	9.559

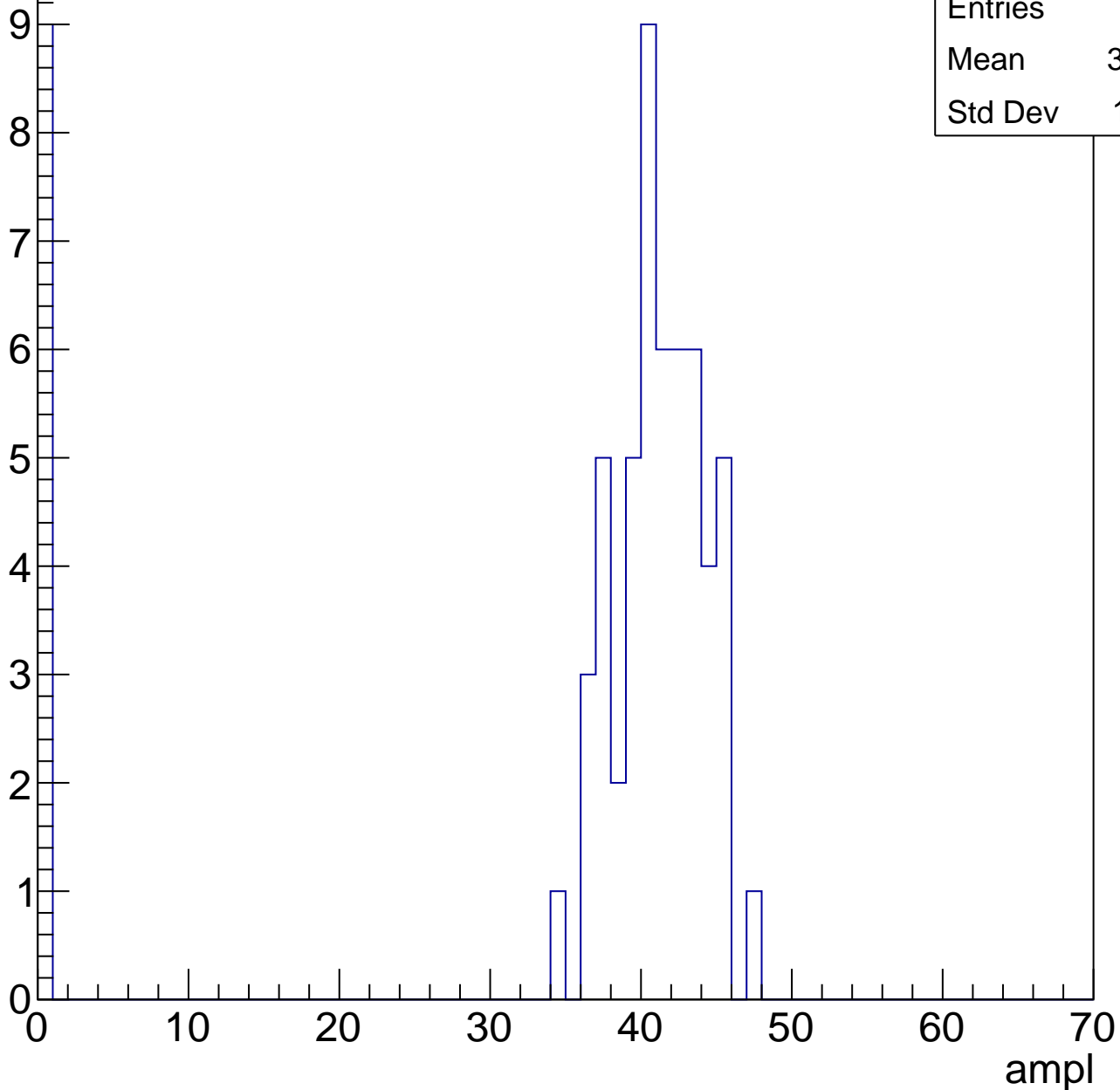


B1L103S, U12-ch86, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	34.87
Std Dev	14.61



B1L103S, U12-ch86, adc3

calib_packv5_041523_1651.root, FC#0, port C2

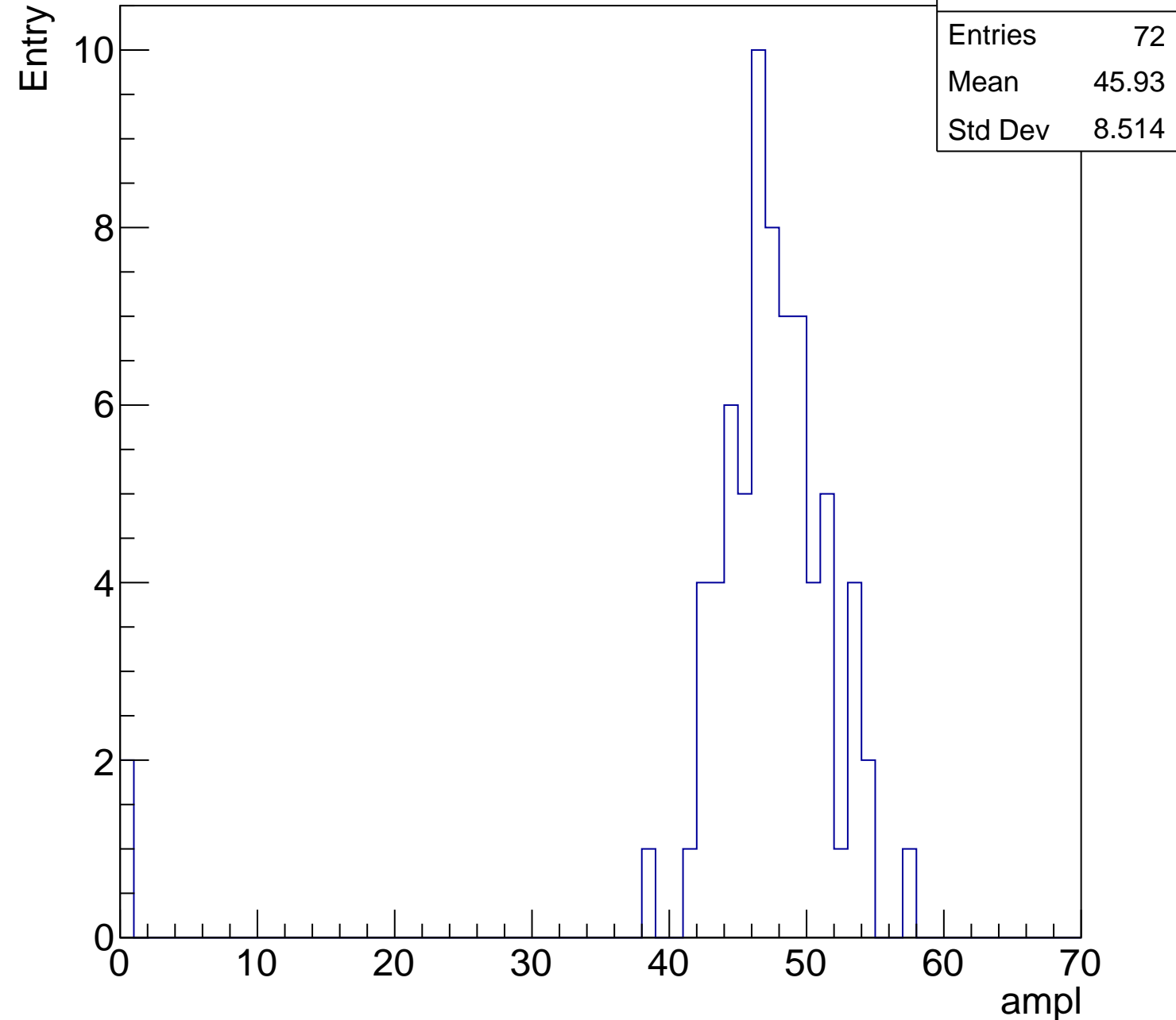
Entries	72
Mean	45.93
Std Dev	8.514

Entry

10
8
6
4
2
0

ampl

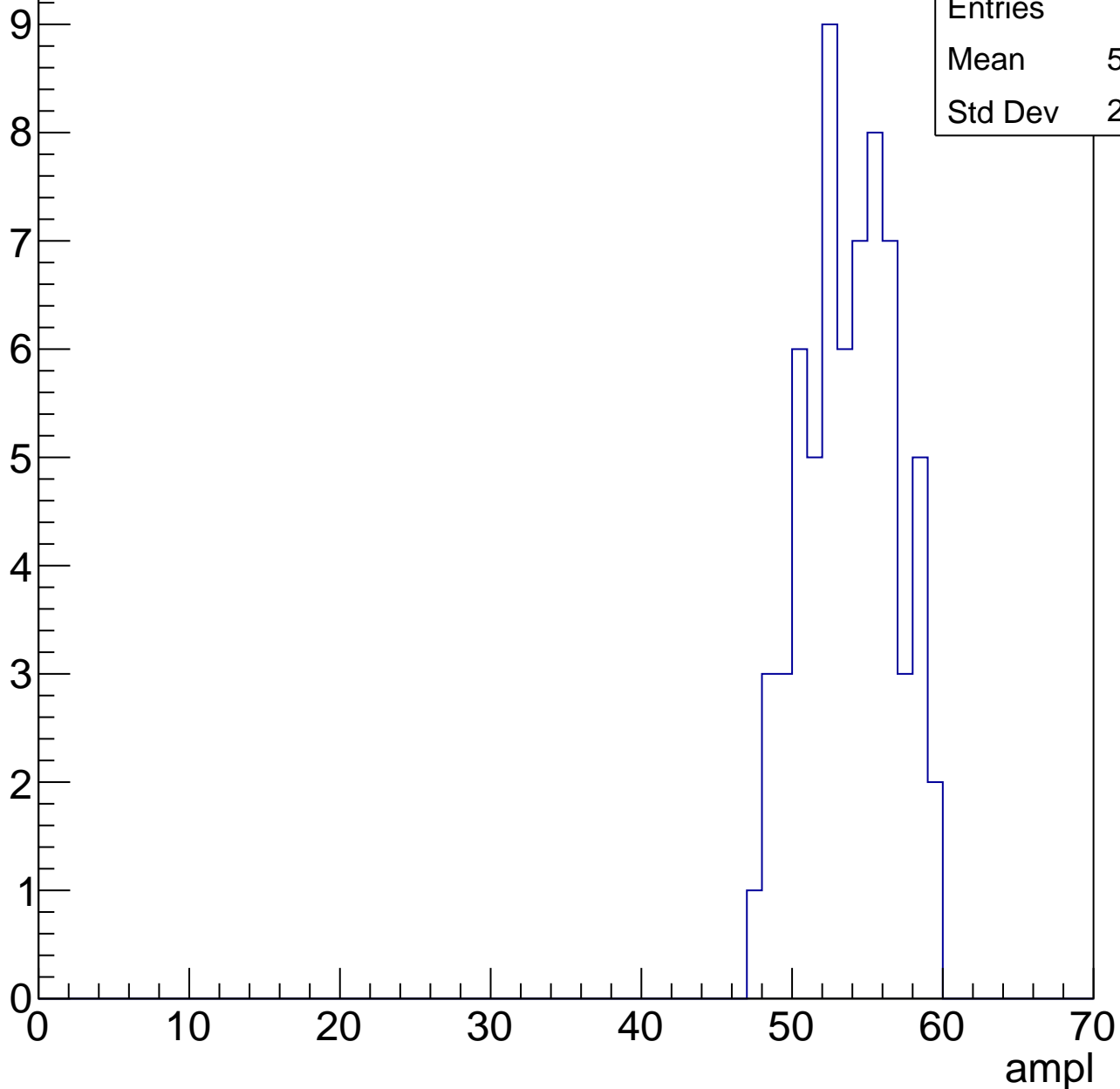
0 10 20 30 40 50 60 70



B1L103S, U12-ch86, adc4

calib_packv5_041523_1651.root, FC#0, port C2

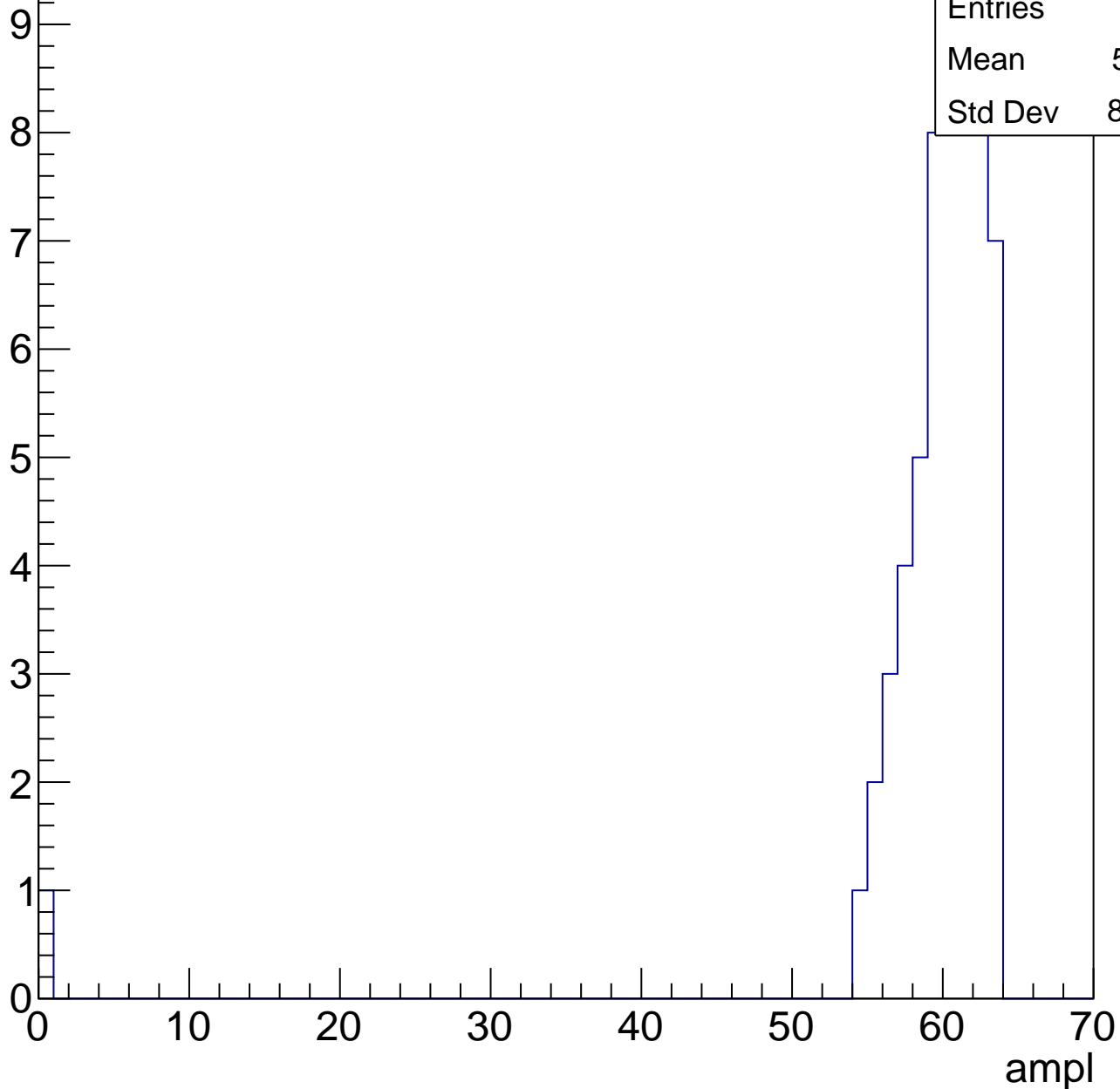
Entry



B1L103S, U12-ch86, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	56
Mean	58.71
Std Dev	8.248

B1L103S, U12-ch86, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

3

2.5

2

1.5

1

0.5

0

Entries	10
Mean	60.8
Std Dev	2.182

ampl

0

10

20

30

40

50

60

70

B1L103S, U12-ch86, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.053
Std Dev	4.466

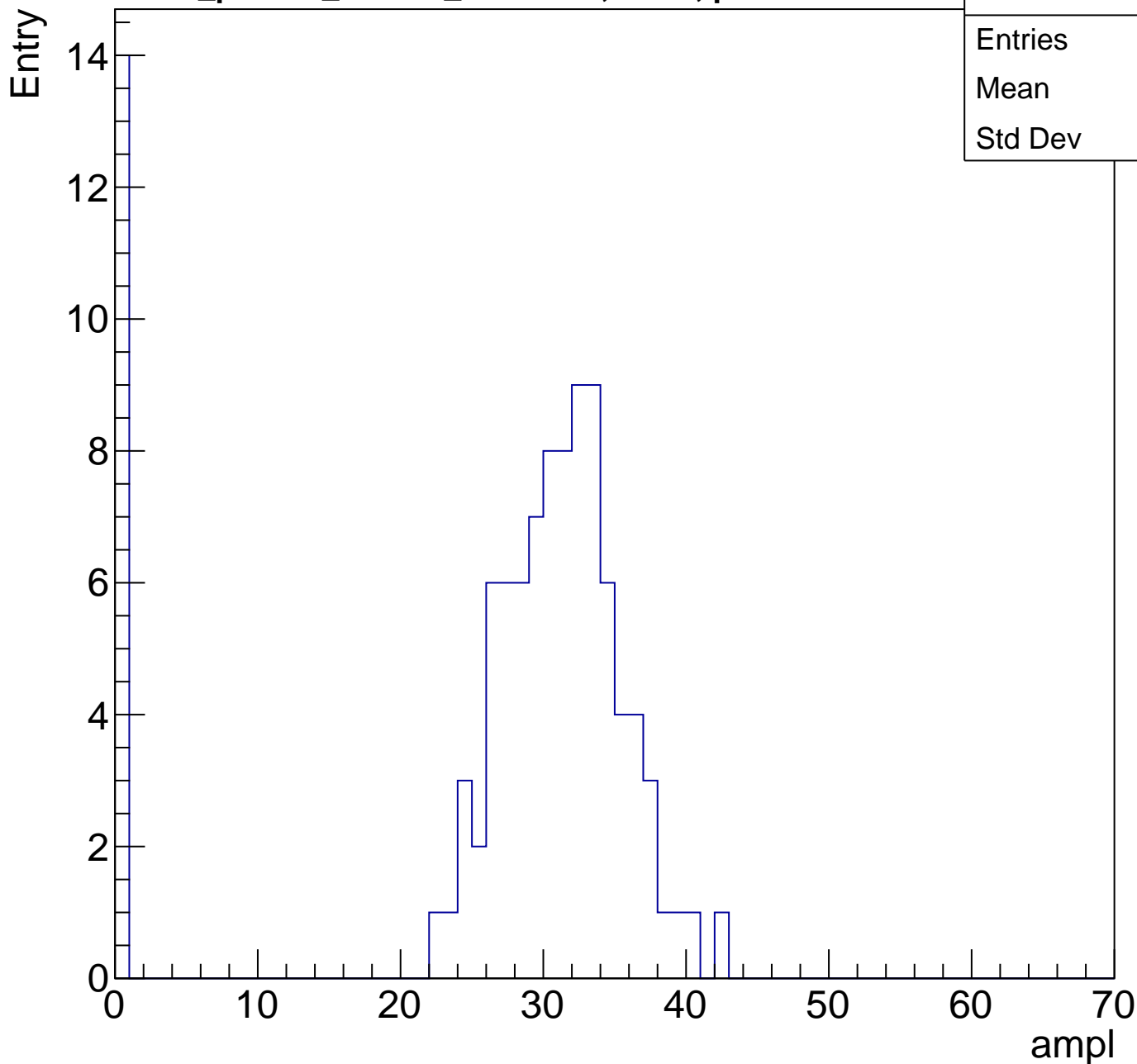
Entry



B1L103S, U12-ch87, adc0

calib_packv5_041523_1651.root, FC#0, port C2

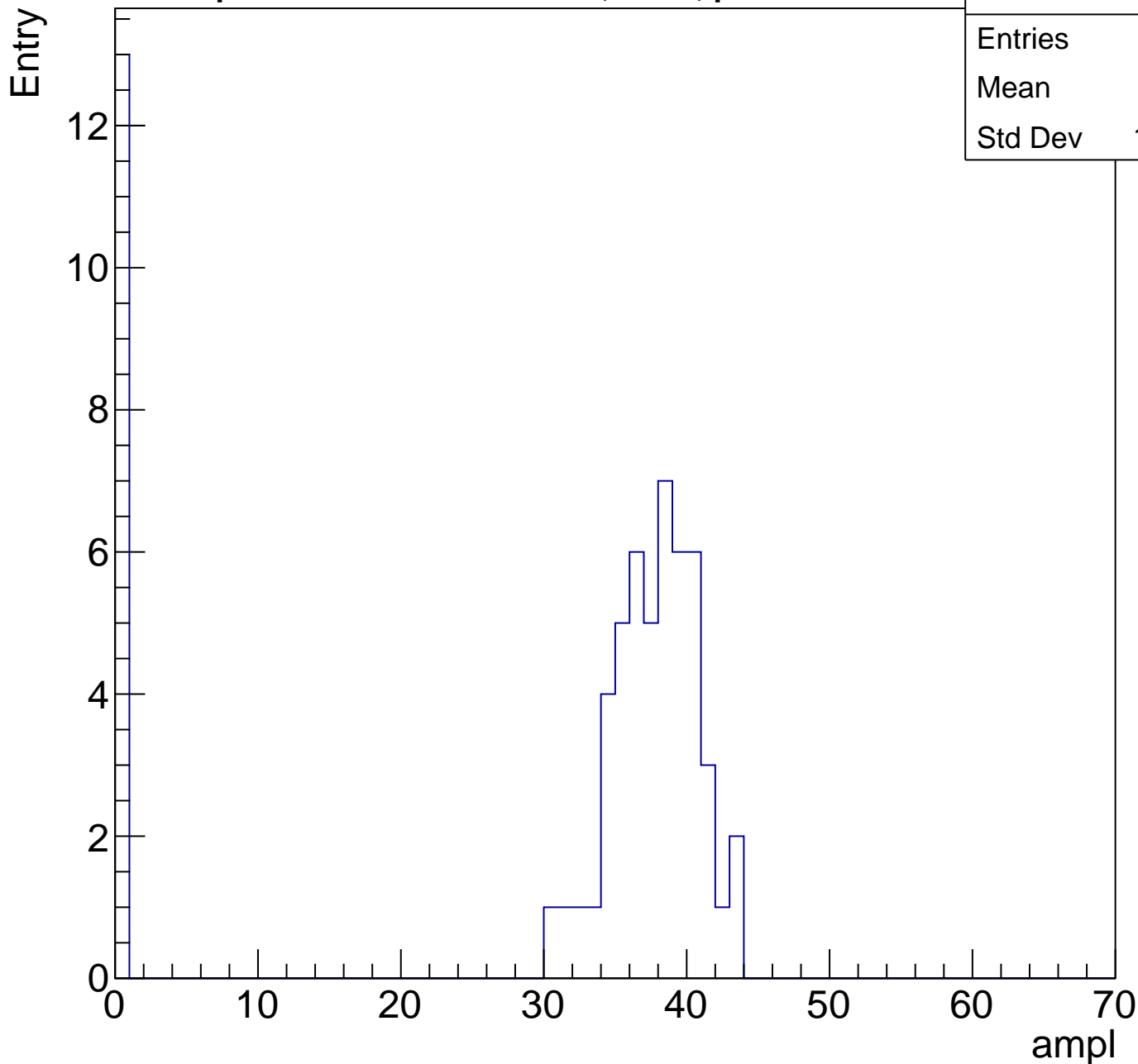
Entries	101
Mean	26.6
Std Dev	11.3



B1L103S, U12-ch87, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	62
Mean	29.5
Std Dev	15.41

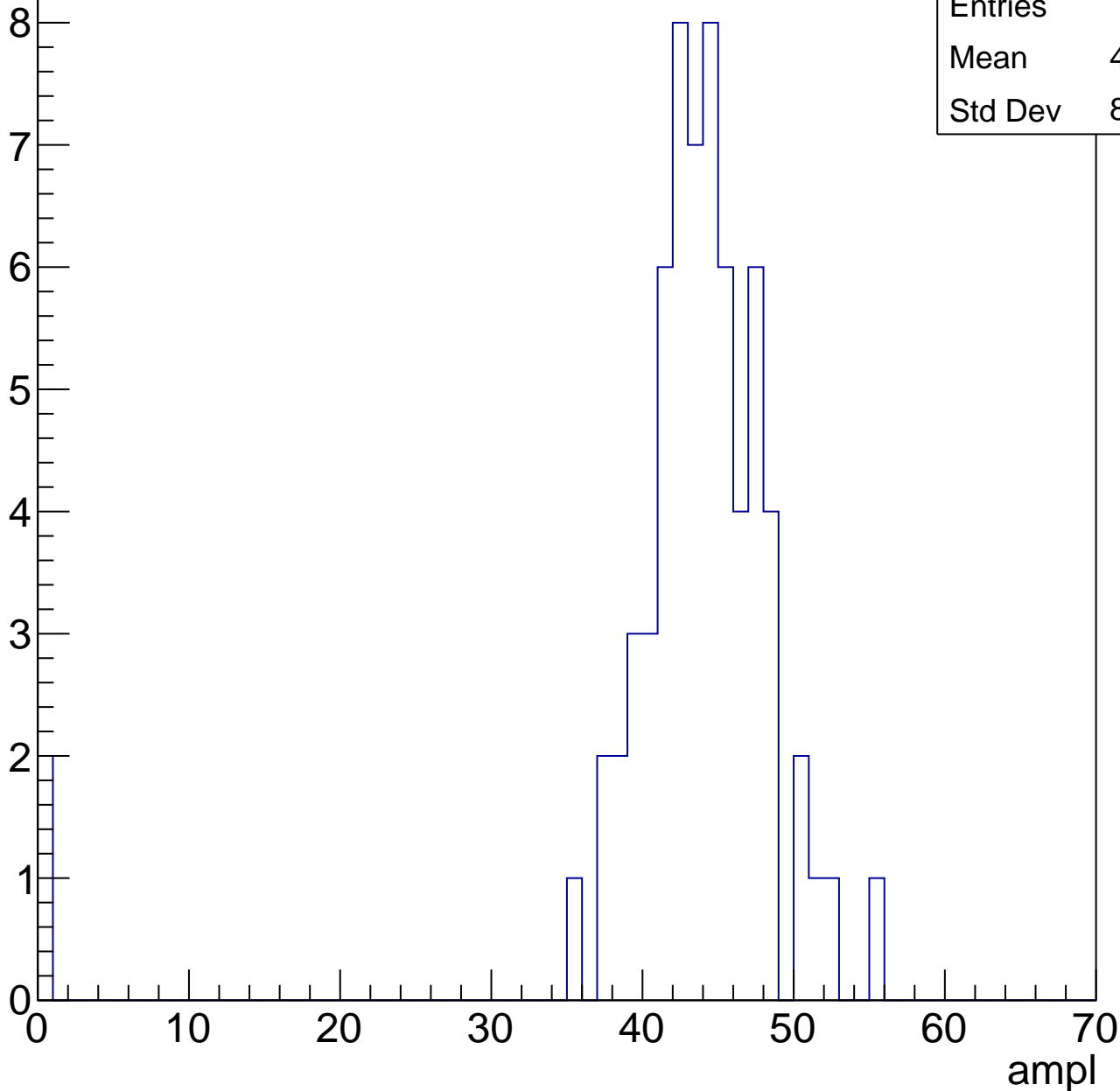


B1L103S, U12-ch87, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	42.43
Std Dev	8.304



B1L103S, U12-ch87, adc3

calib_packv5_041523_1651.root, FC#0, port C2

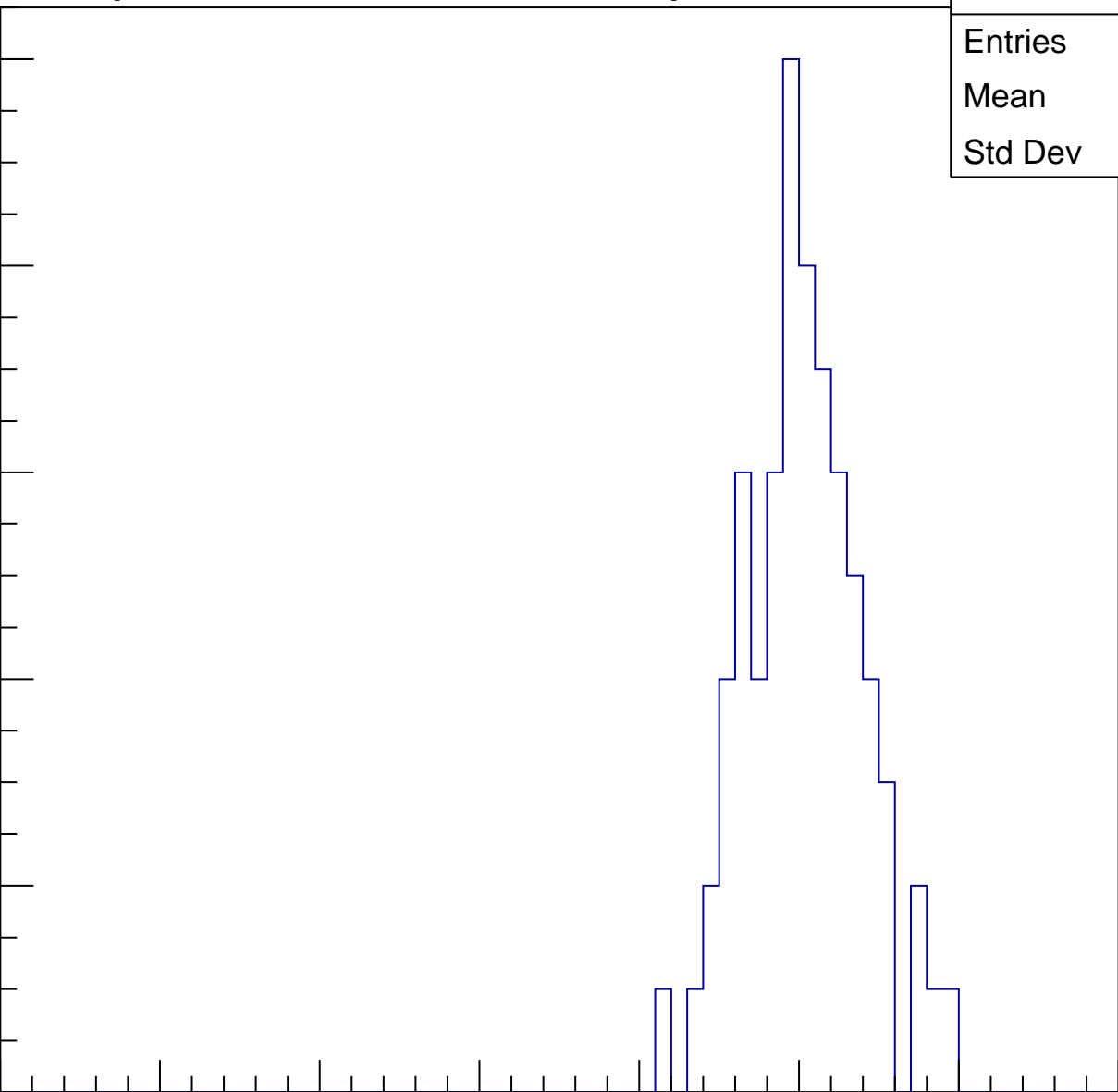
Entries	71
Mean	49.86
Std Dev	3.609

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

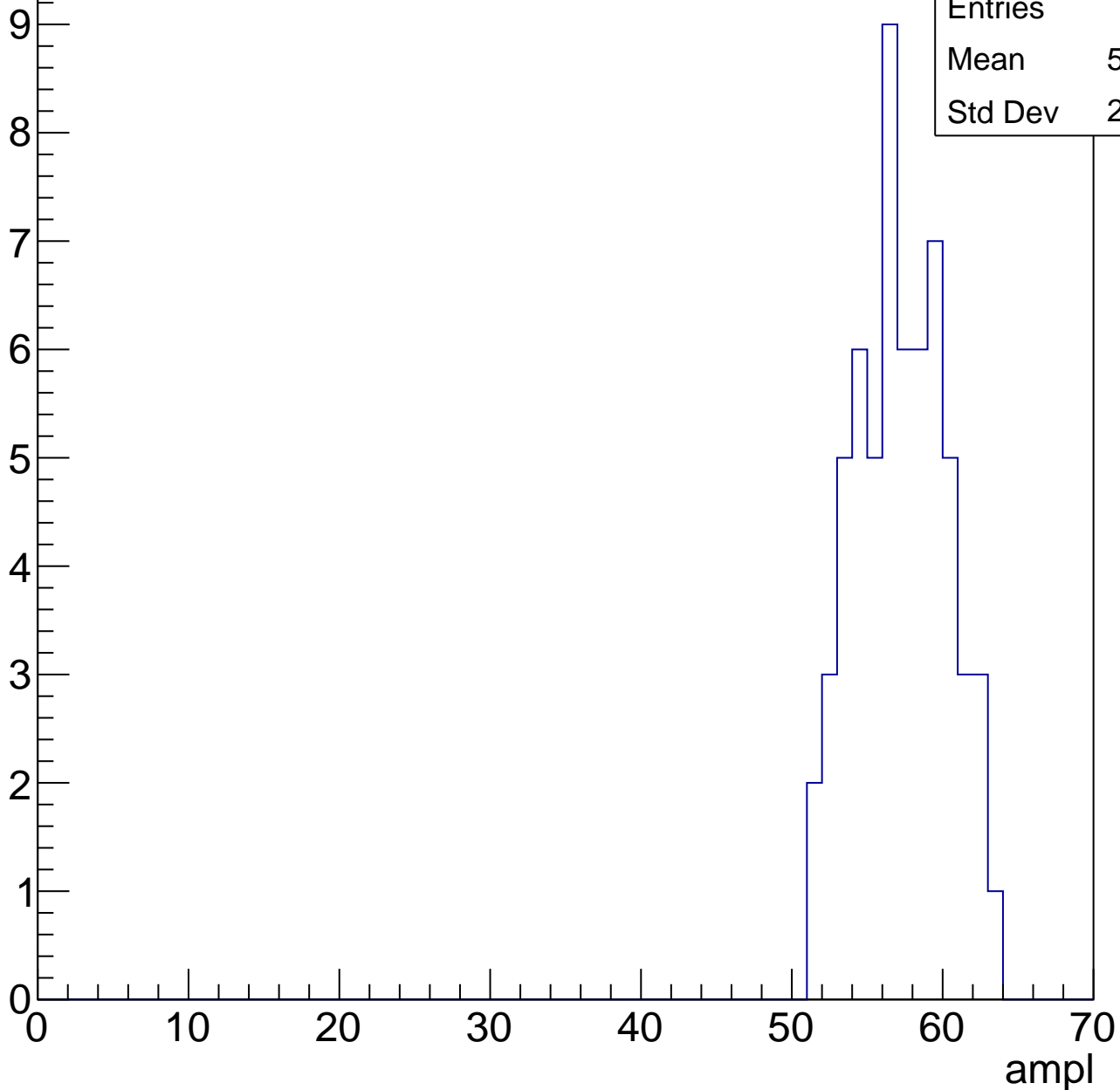


B1L103S, U12-ch87, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	56.74
Std Dev	2.986

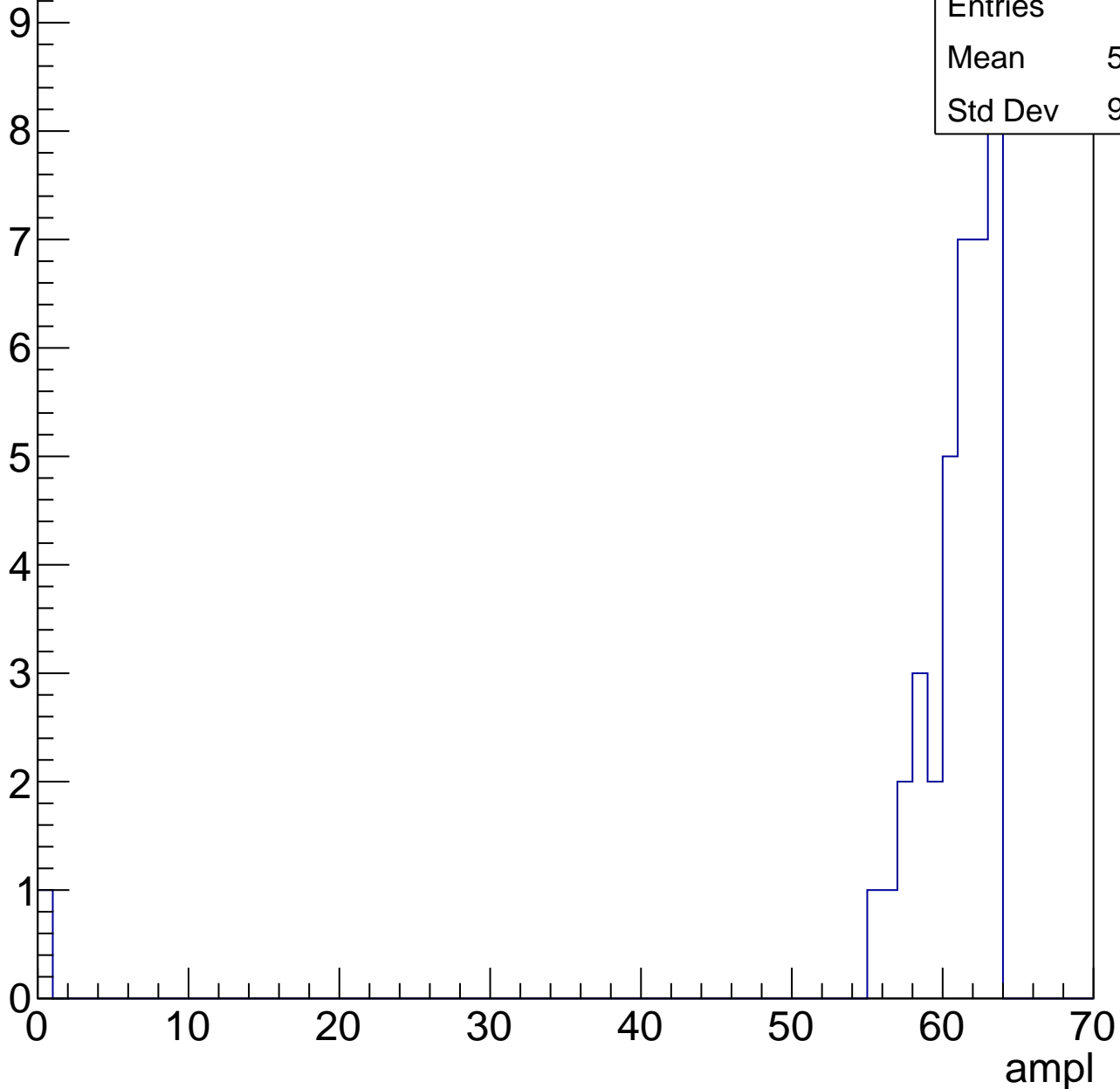


B1L103S, U12-ch87, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	38
Mean	59.08
Std Dev	9.943



B1L103S, U12-ch87, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	0
Mean	0
Std Dev	0

B1L103S, U12-ch87, adc7

calib_packv5_041523_1651.root, FC#0, port C2

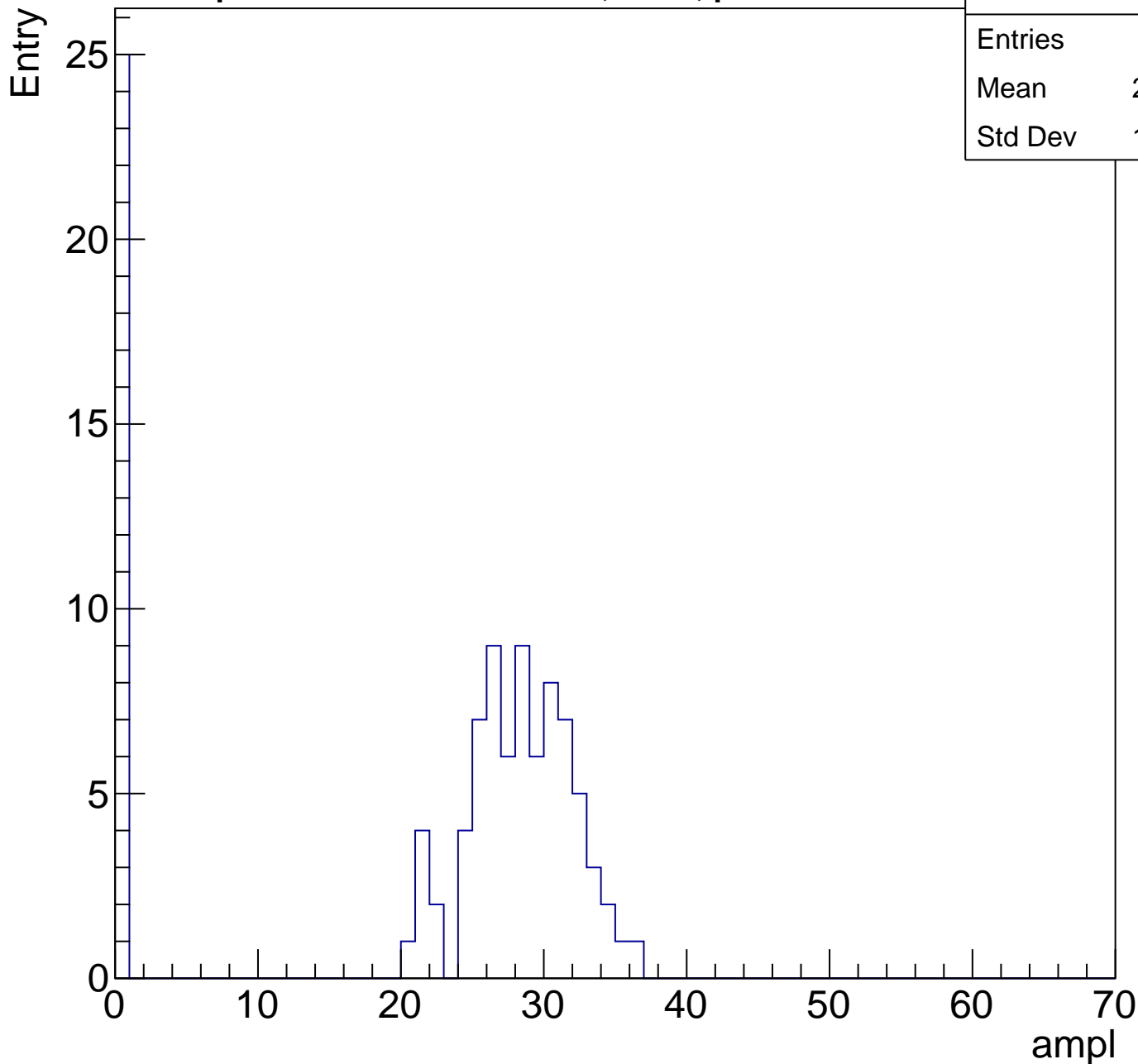
Entry



B1L103S, U12-ch88, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	100
Mean	20.96
Std Dev	12.48

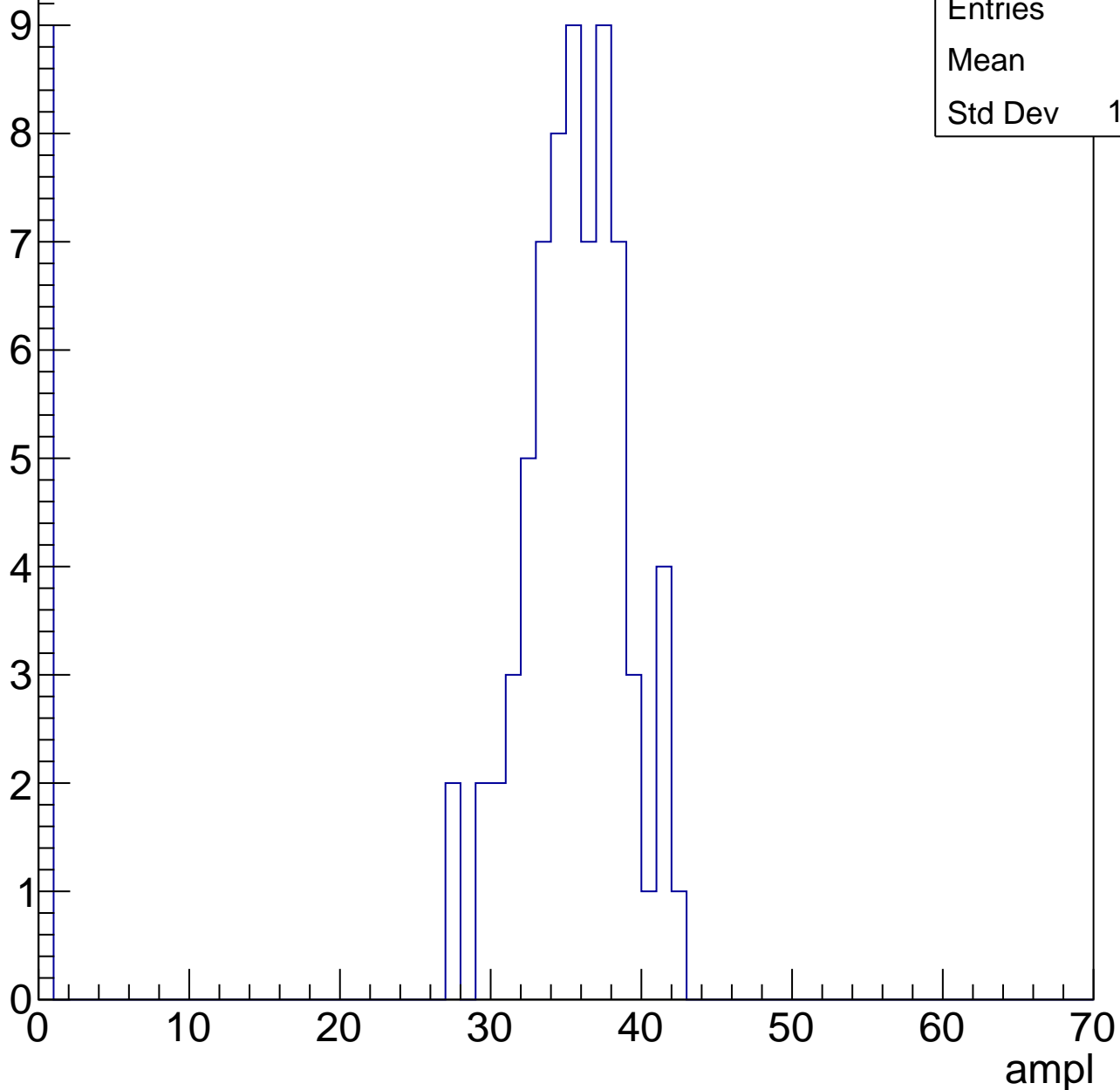


B1L103S, U12-ch88, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	79
Mean	31.1
Std Dev	11.57

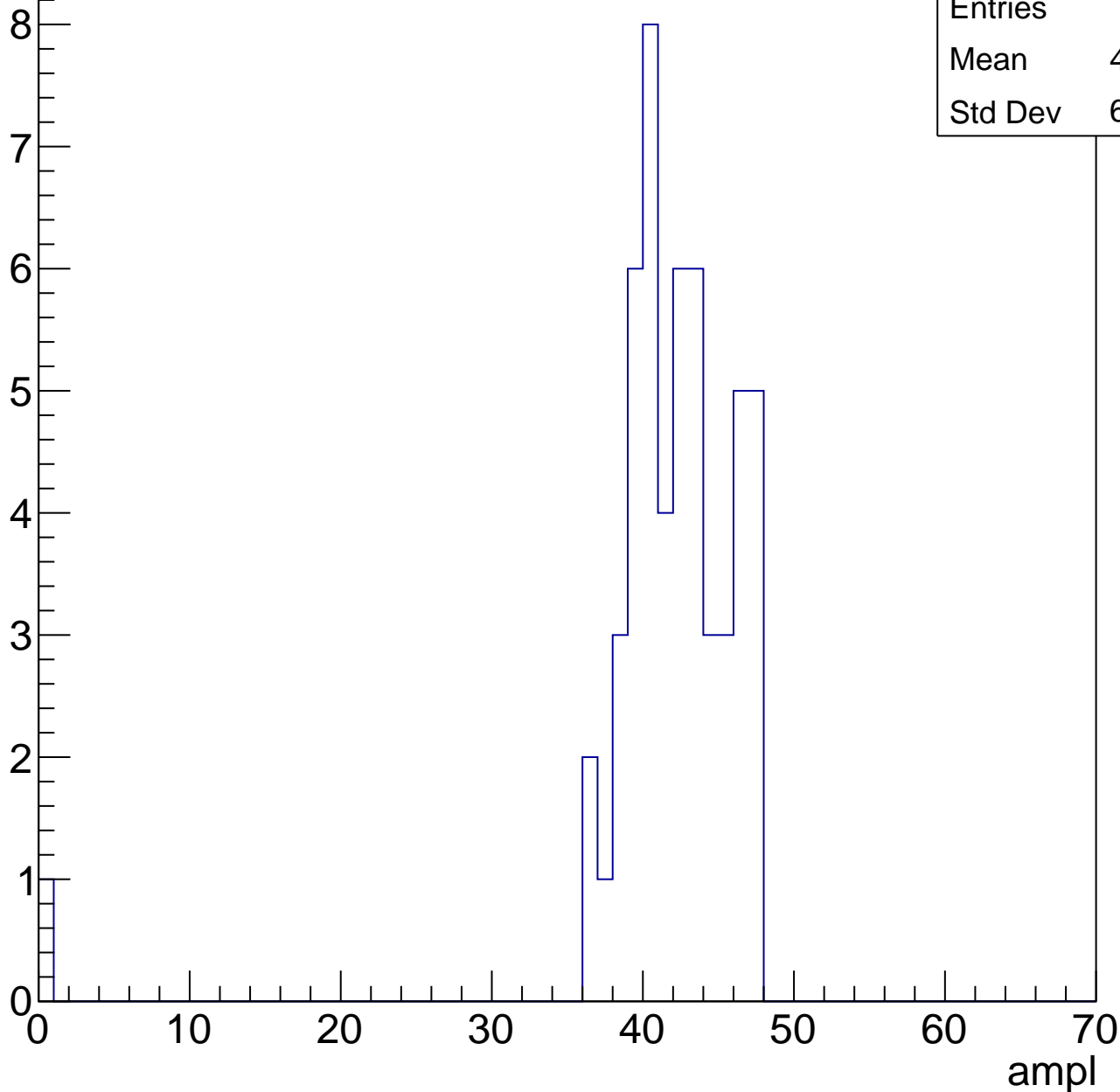


B1L103S, U12-ch88, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	53
Mean	41.19
Std Dev	6.463

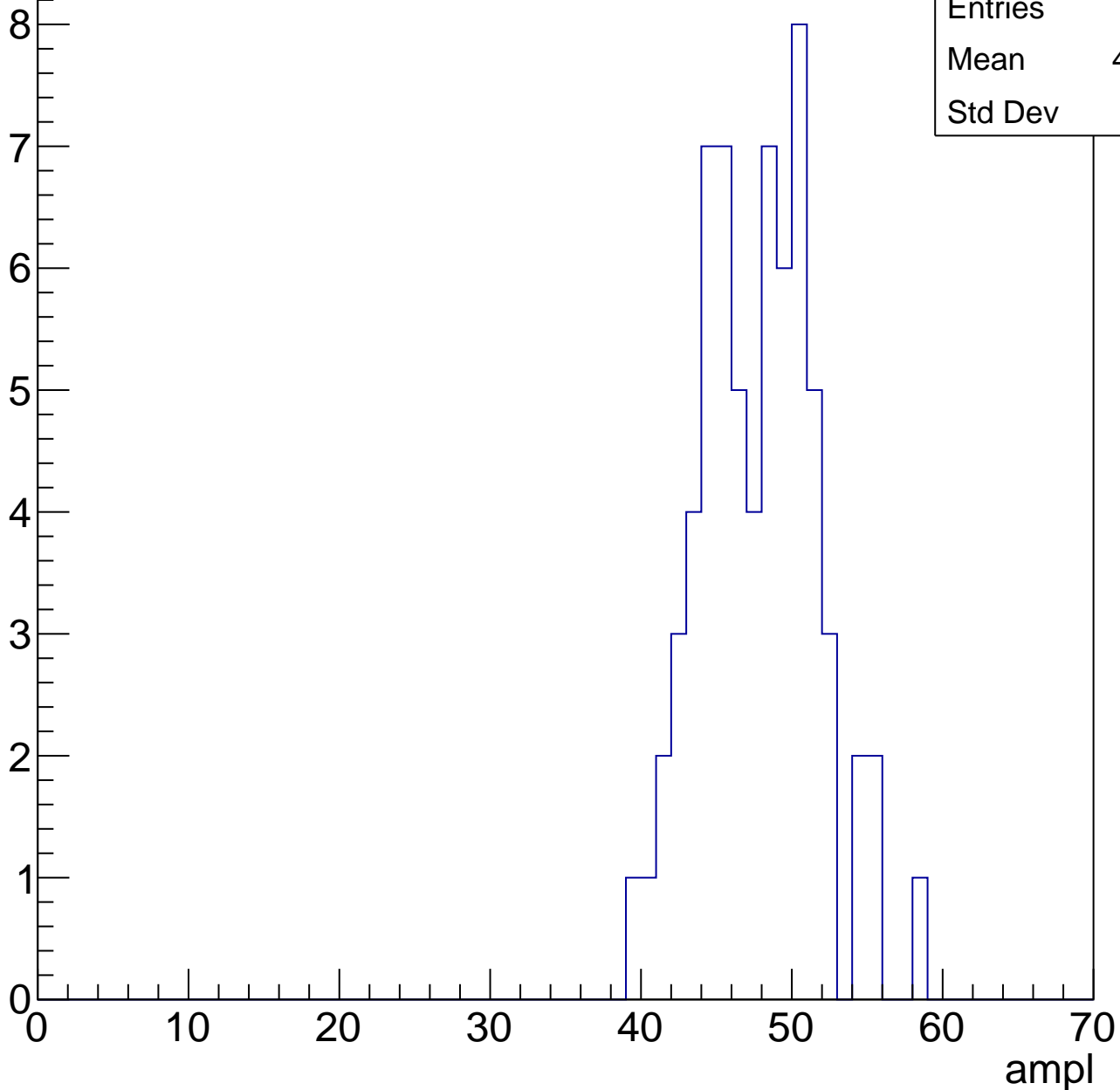


B1L103S, U12-ch88, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	47.31
Std Dev	3.87

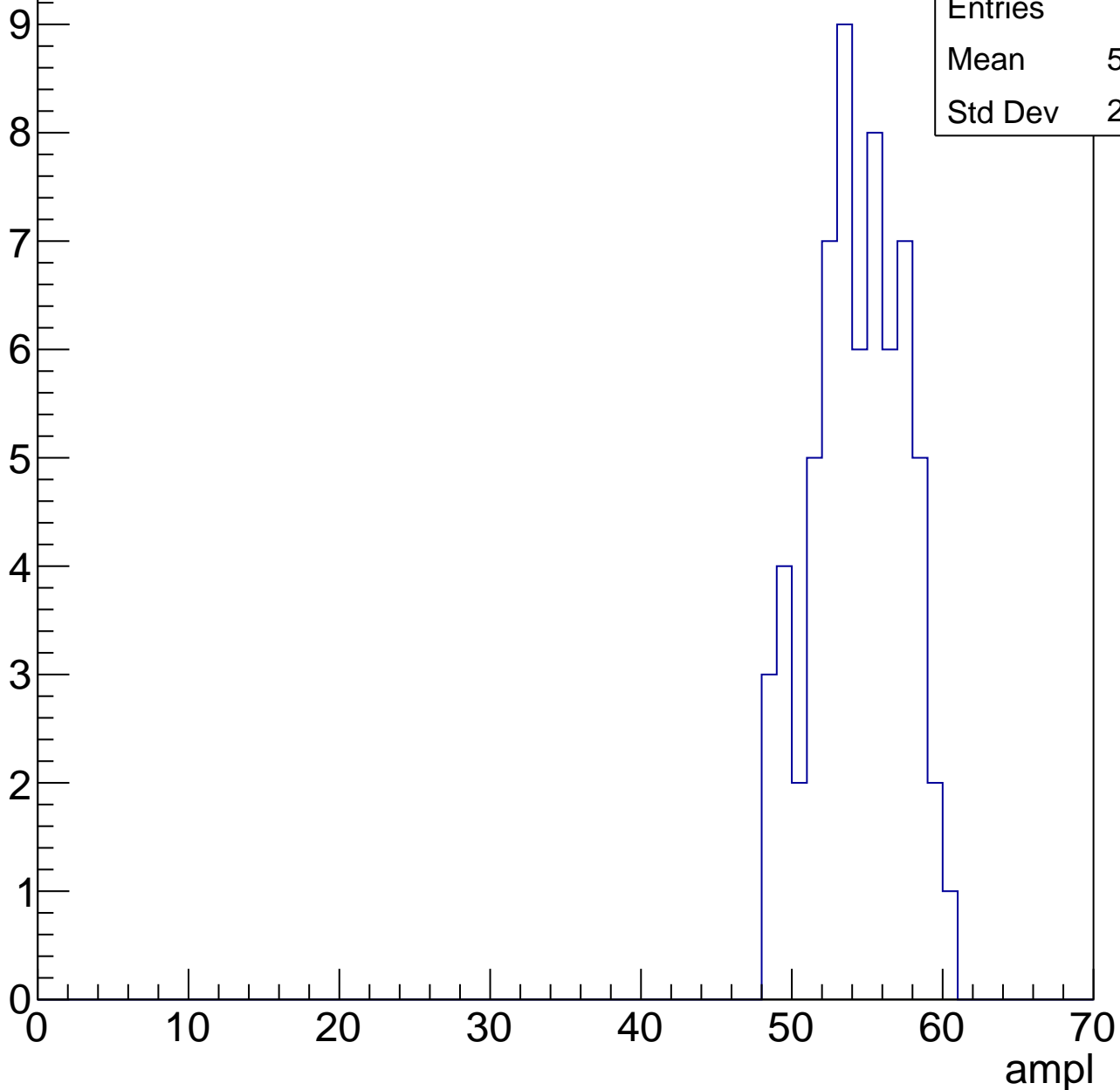


B1L103S, U12-ch88, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	53.89
Std Dev	2.993

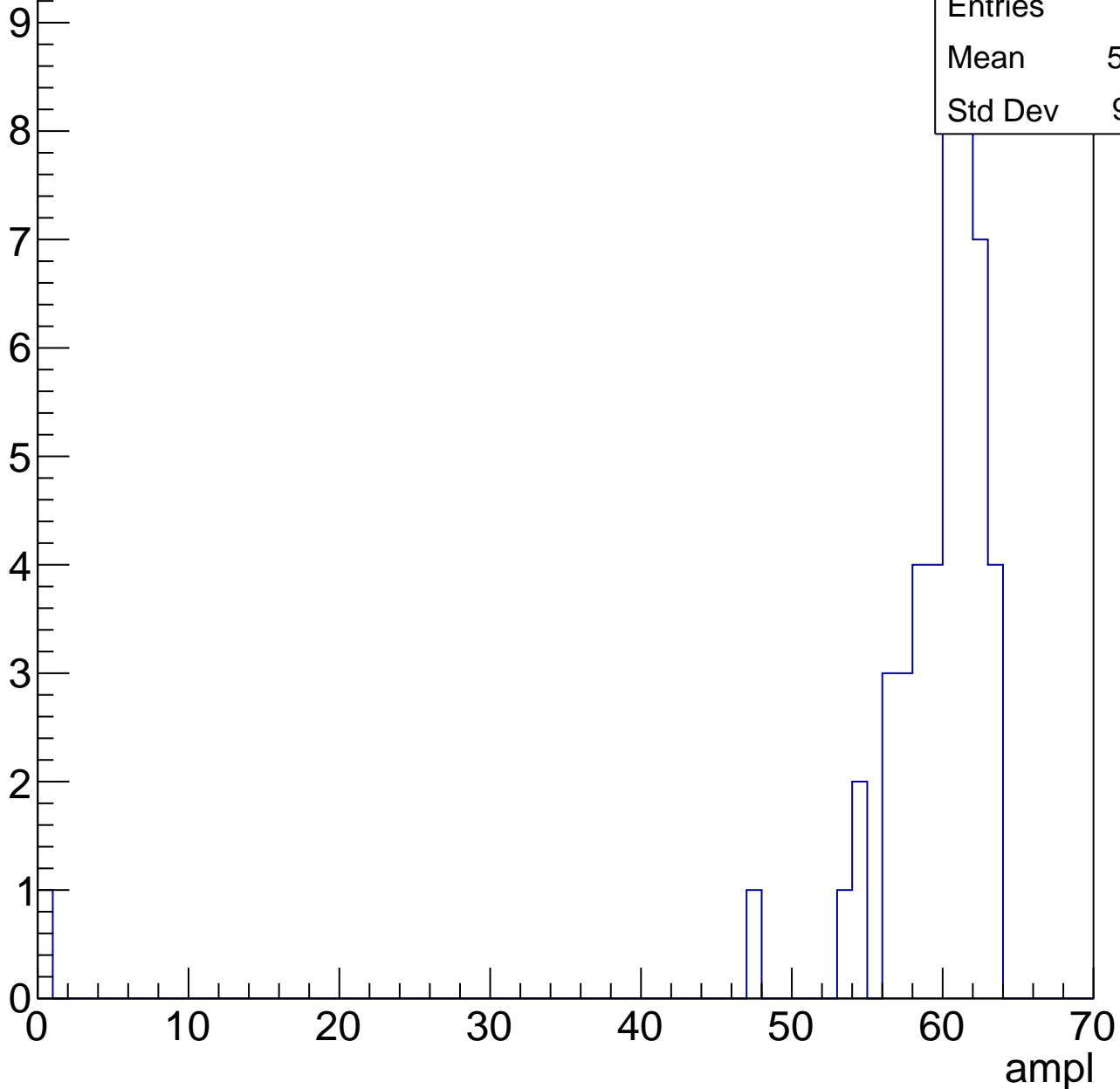


B1L103S, U12-ch88, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	48
Mean	58.12
Std Dev	9.001

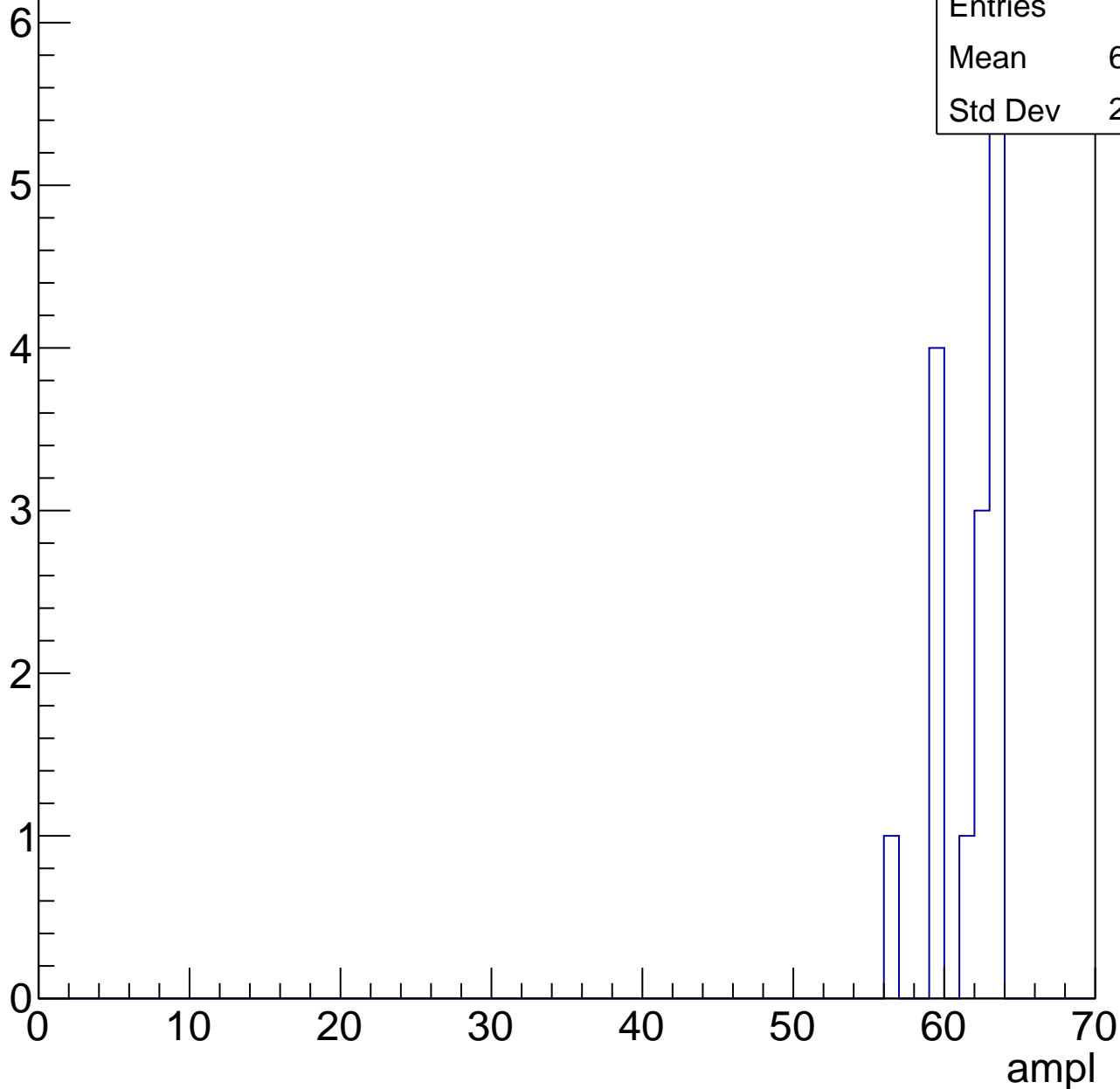


B1L103S, U12-ch88, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	15
Mean	61.13
Std Dev	2.125



B1L103S, U12-ch88, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

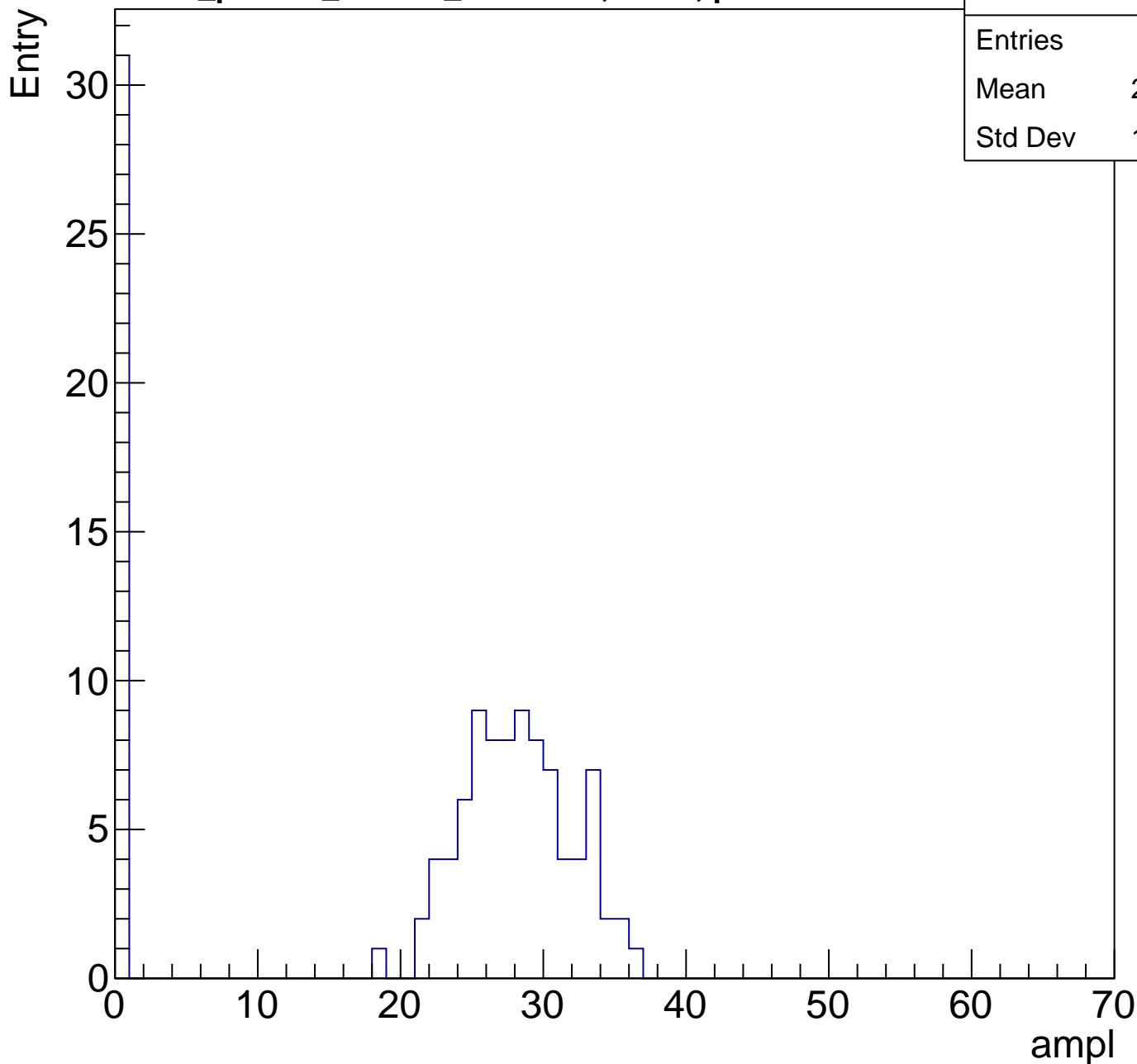
ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U12-ch89, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	117
Mean	20.38
Std Dev	12.64

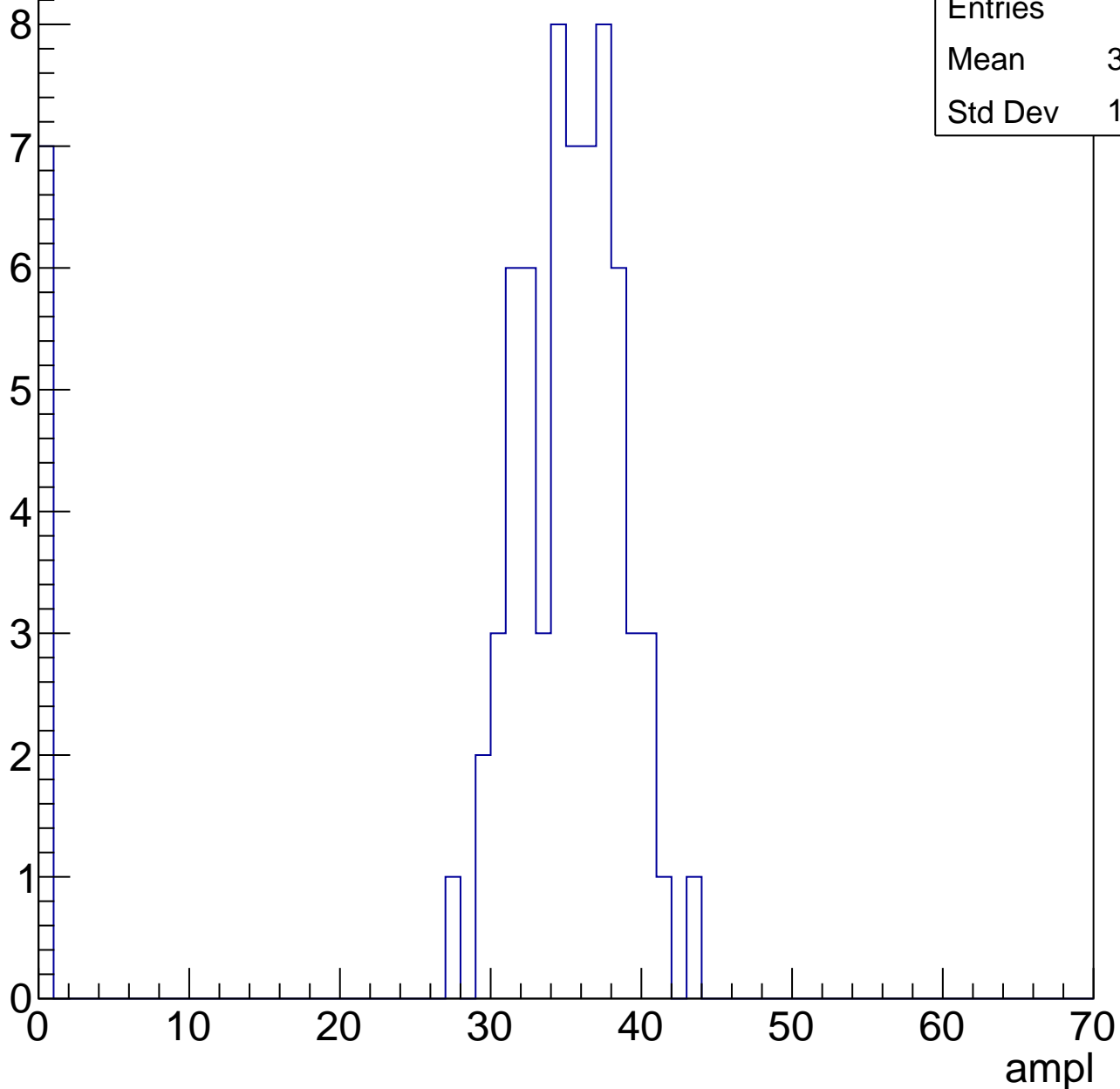


B1L103S, U12-ch89, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	72
Mean	31.47
Std Dev	10.79

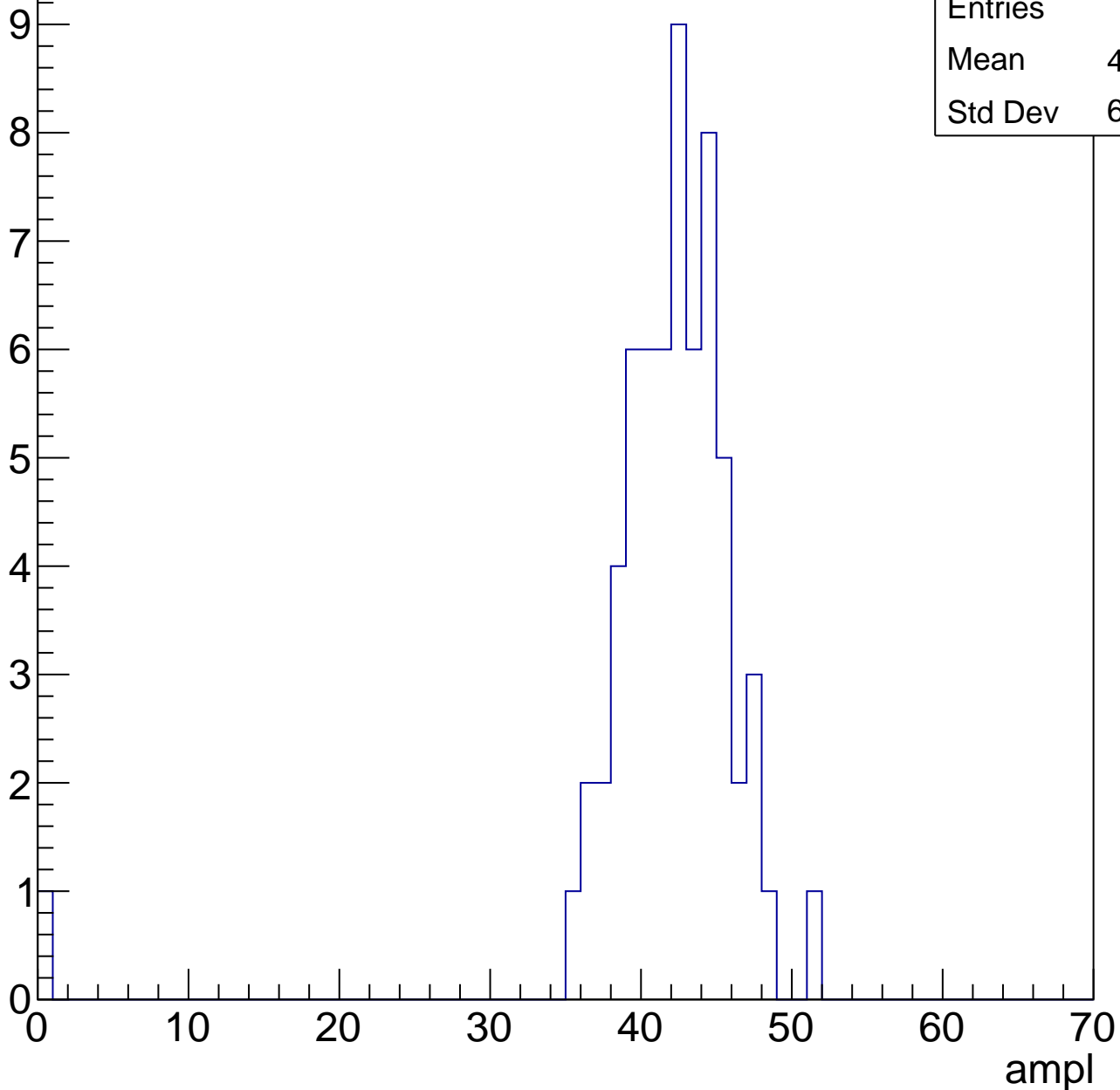


B1L103S, U12-ch89, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	63
Mean	41.24
Std Dev	6.112

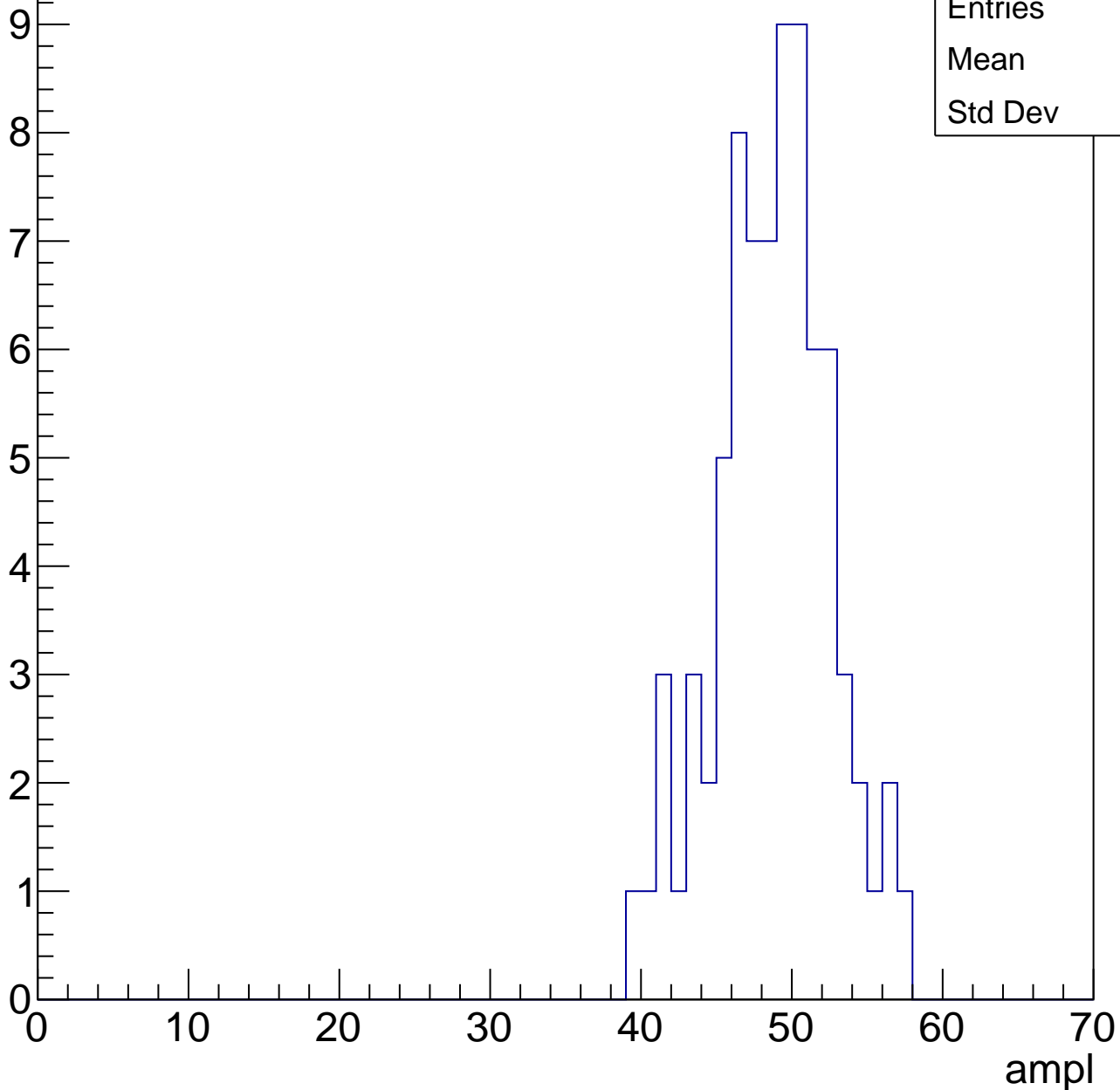


B1L103S, U12-ch89, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

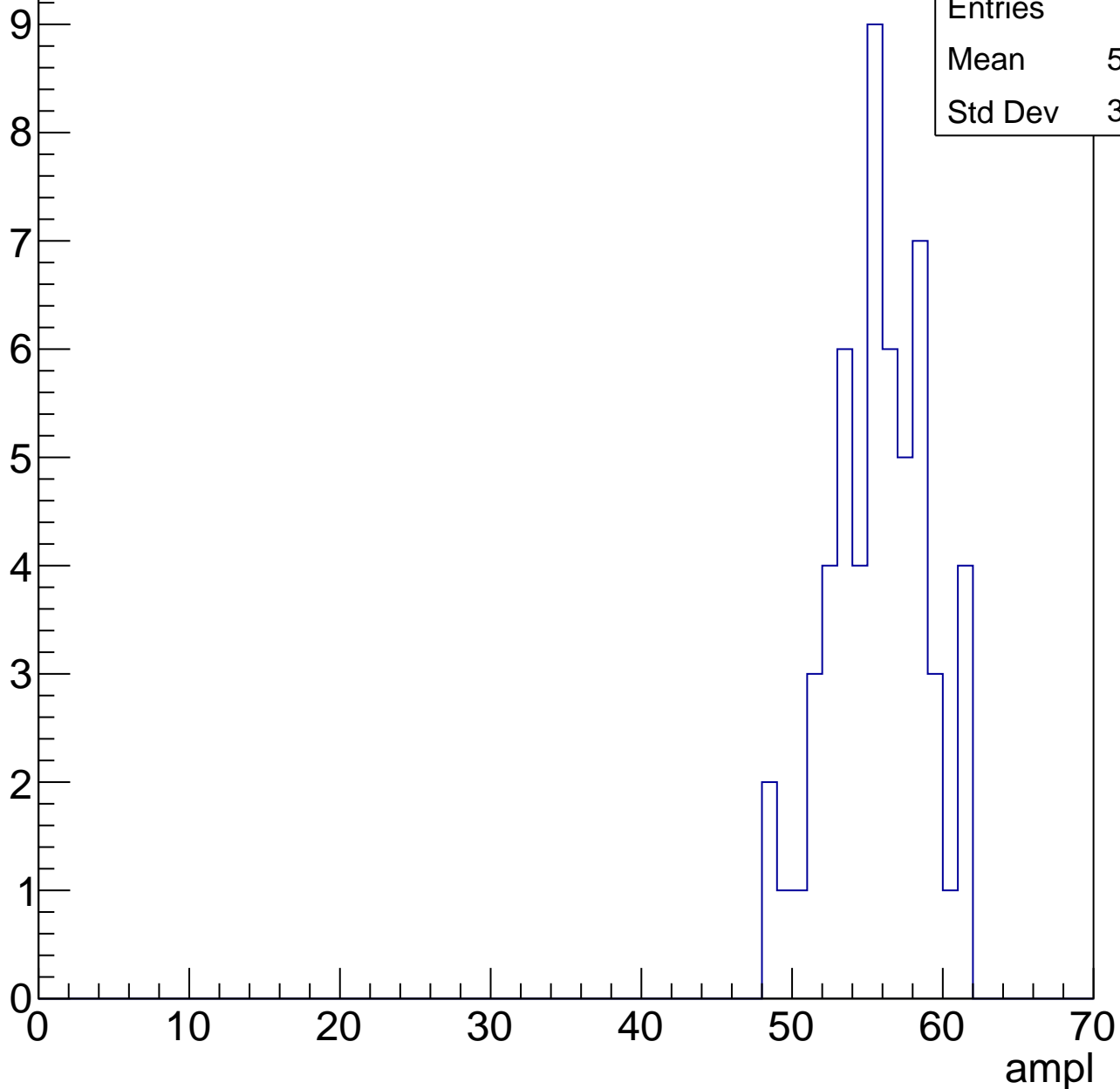
Entries	77
Mean	48.3
Std Dev	3.8



B1L103S, U12-ch89, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry



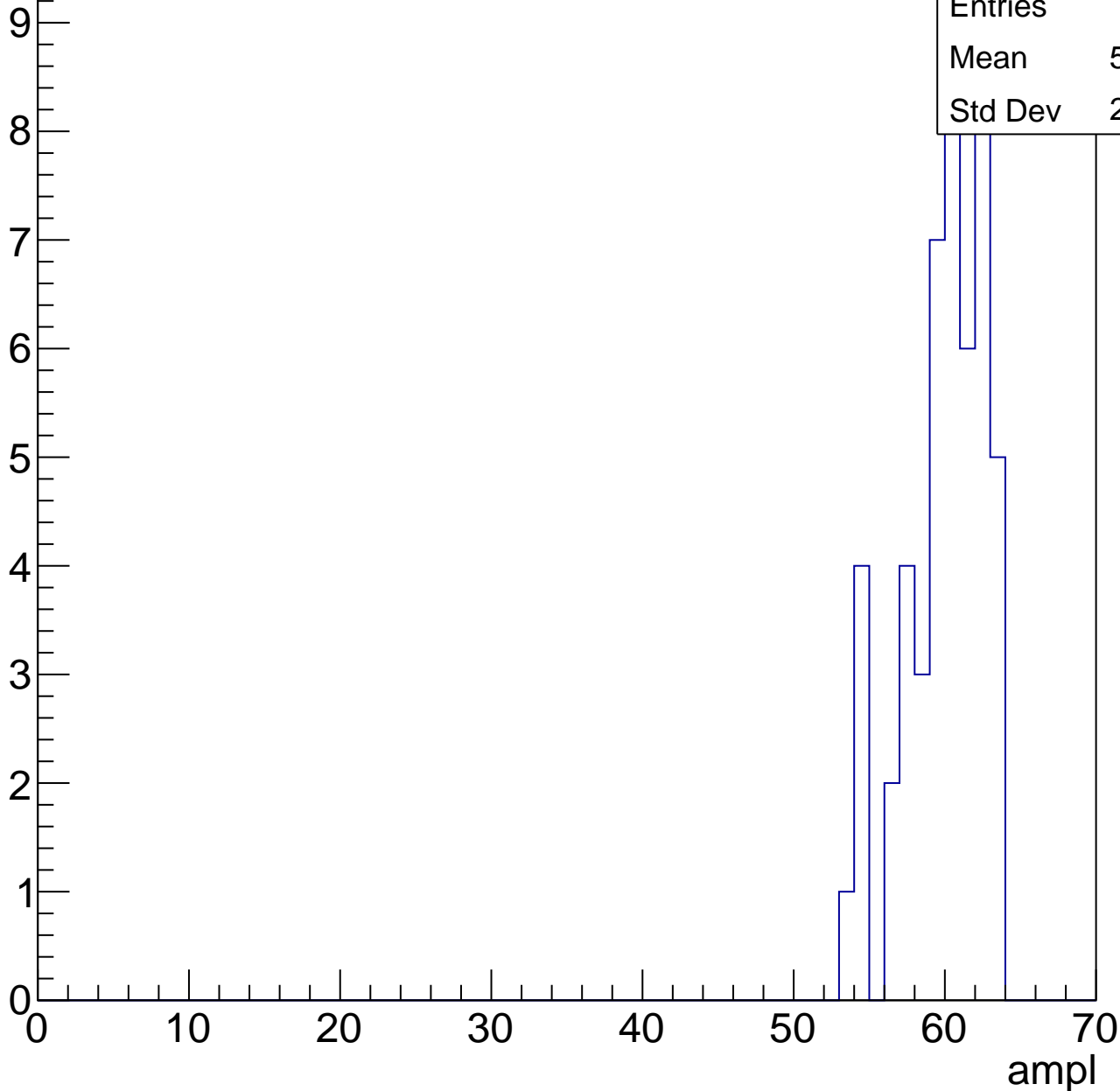
Entries	56
Mean	55.23
Std Dev	3.202

B1L103S, U12-ch89, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	49
Mean	59.45
Std Dev	2.665

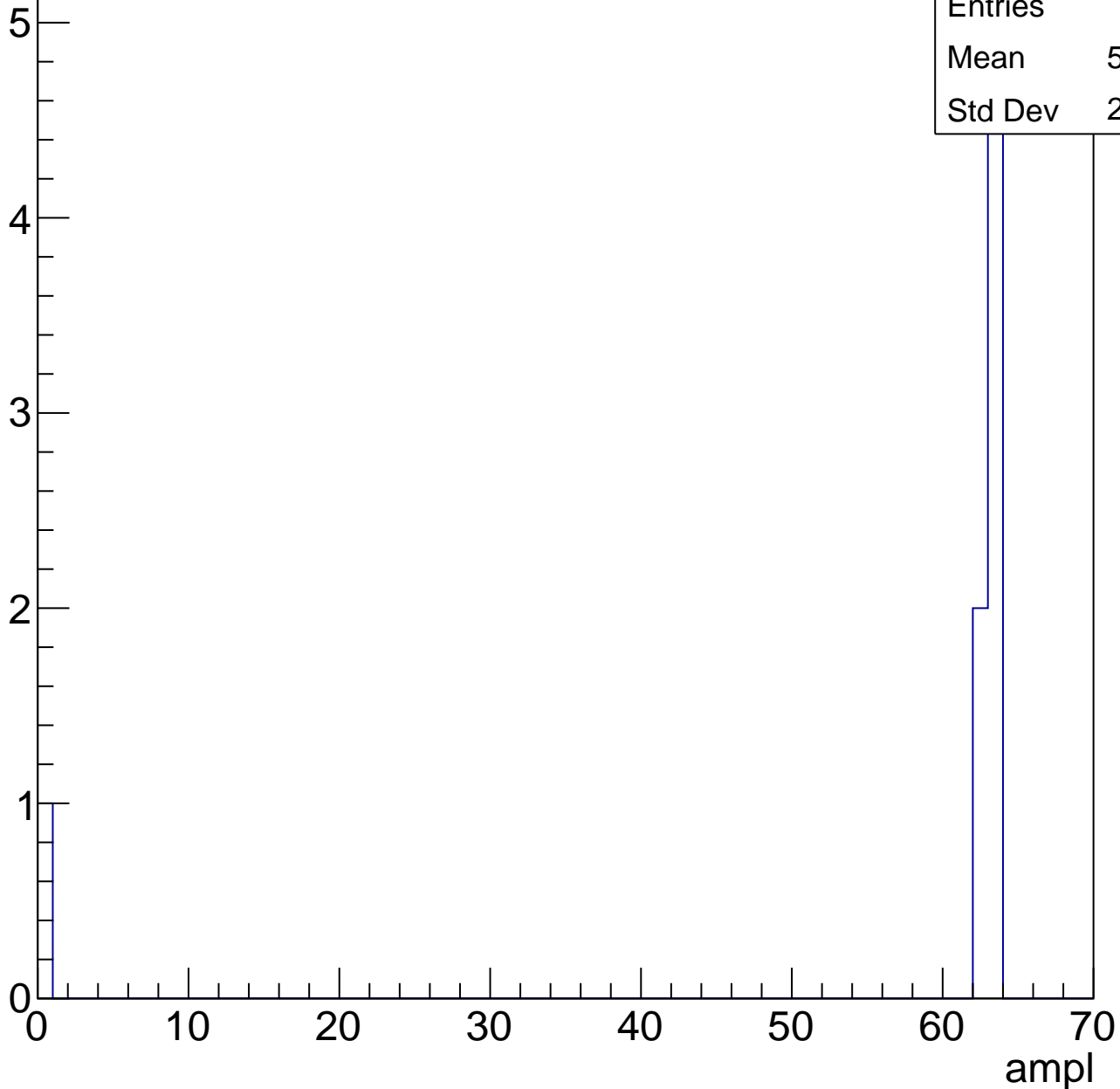


B1L103S, U12-ch89, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	8
Mean	54.88
Std Dev	20.75



B1L103S, U12-ch89, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U12-ch90, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	82
Mean	23.52
Std Dev	9.935

Entry

10

8

6

4

2

0

0

10

20

30

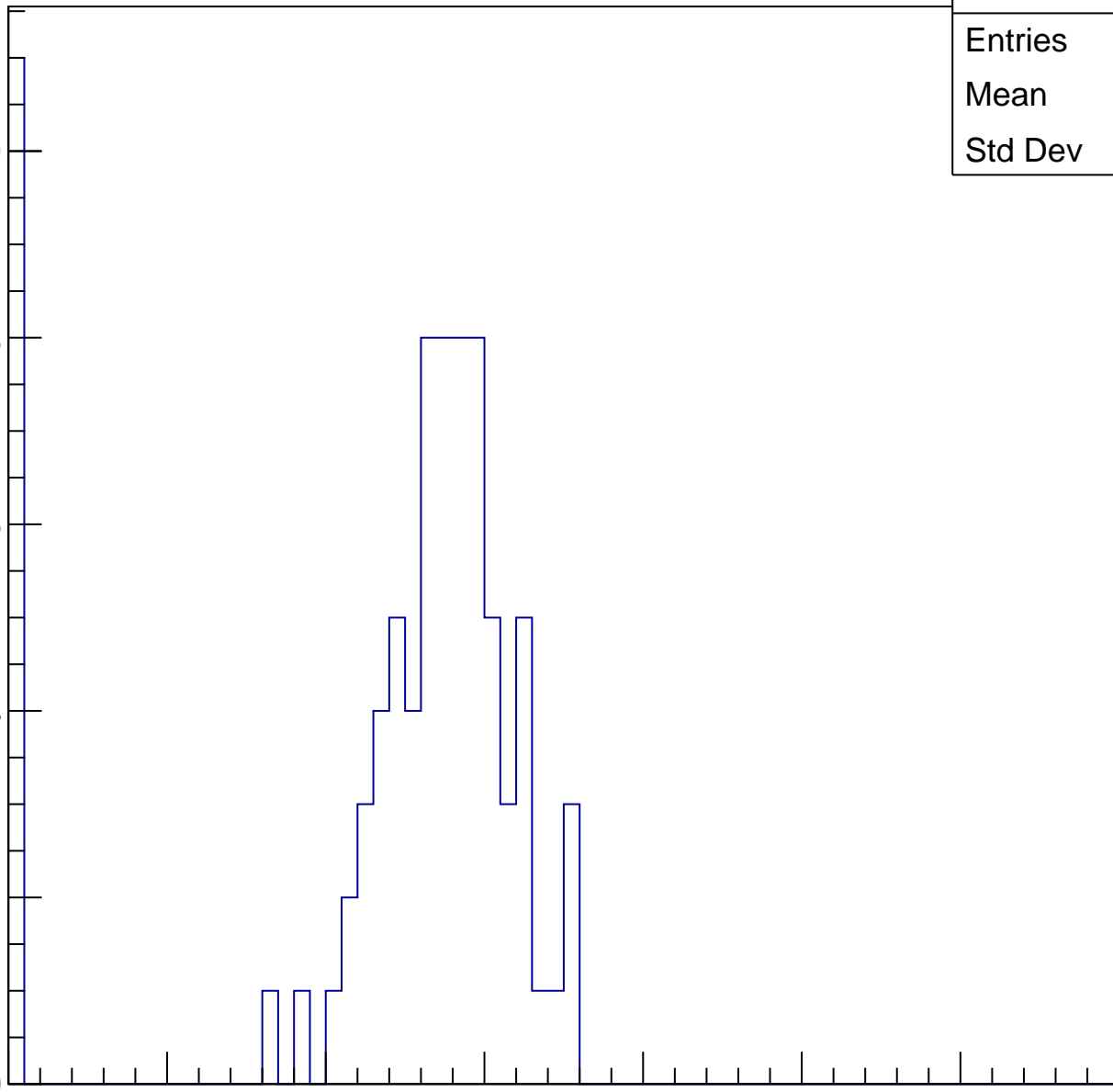
40

50

60

70

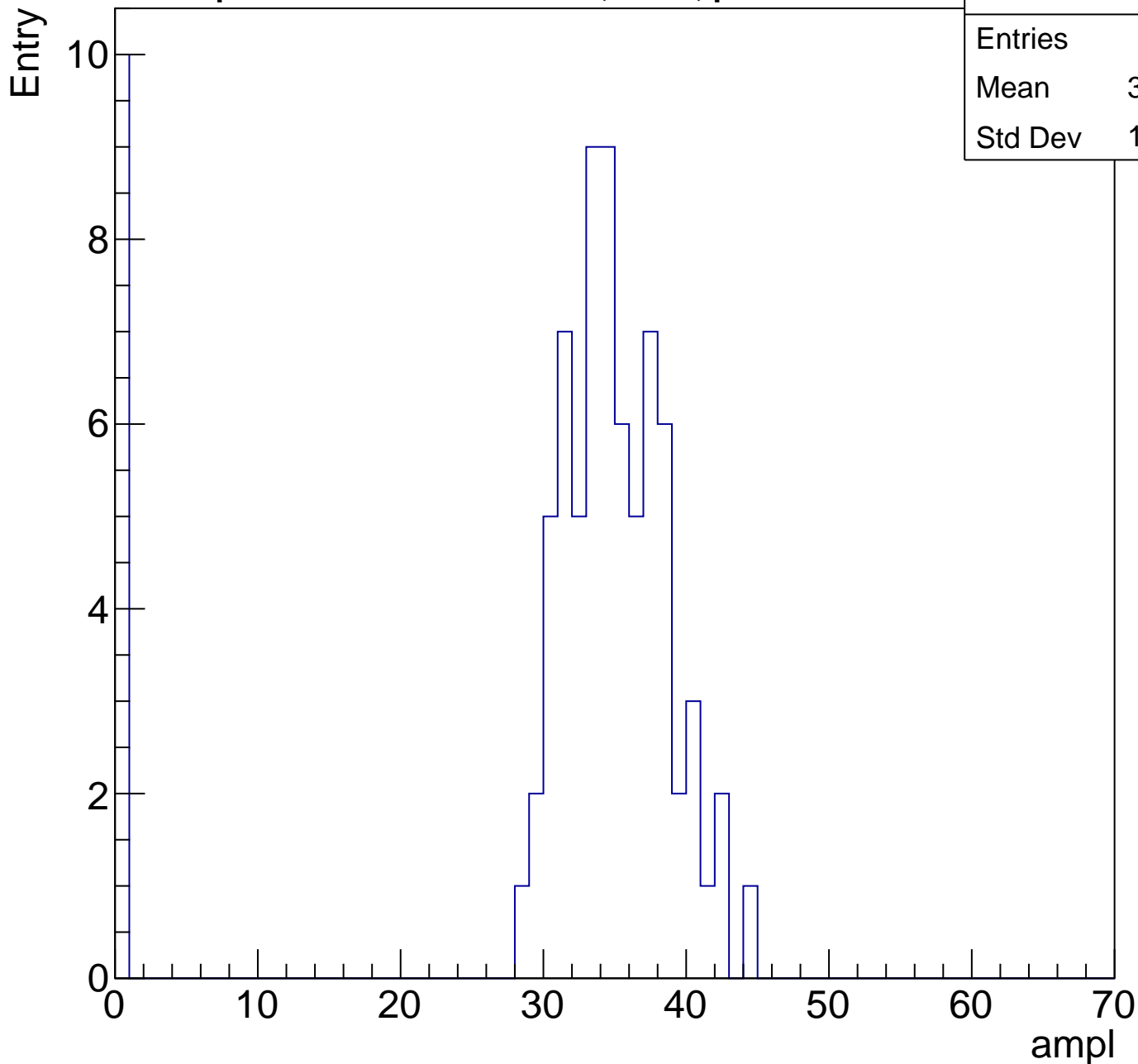
ampl



B1L103S, U12-ch90, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	81
Mean	30.37
Std Dev	11.85

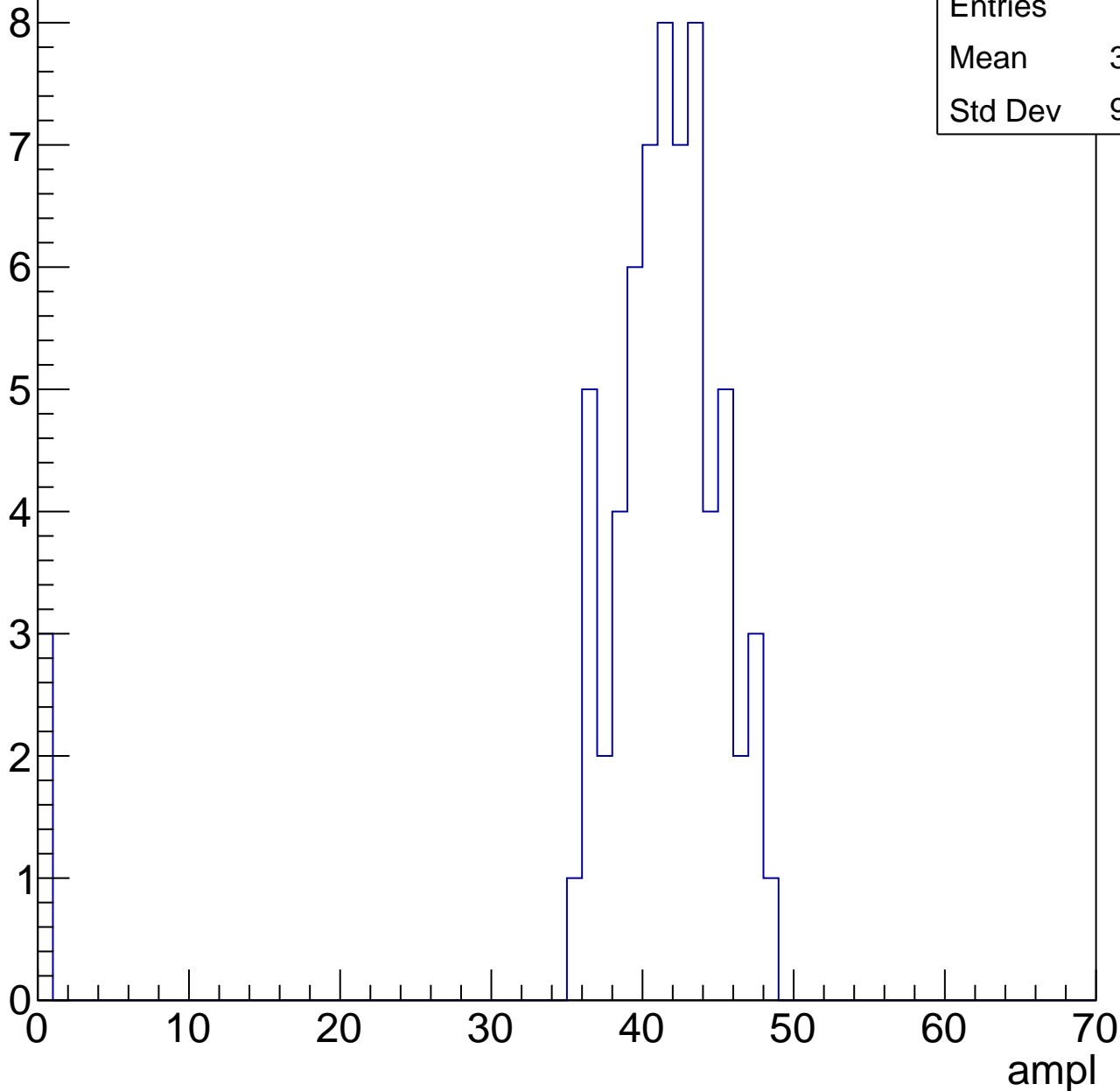


B1L103S, U12-ch90, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	39.44
Std Dev	9.132

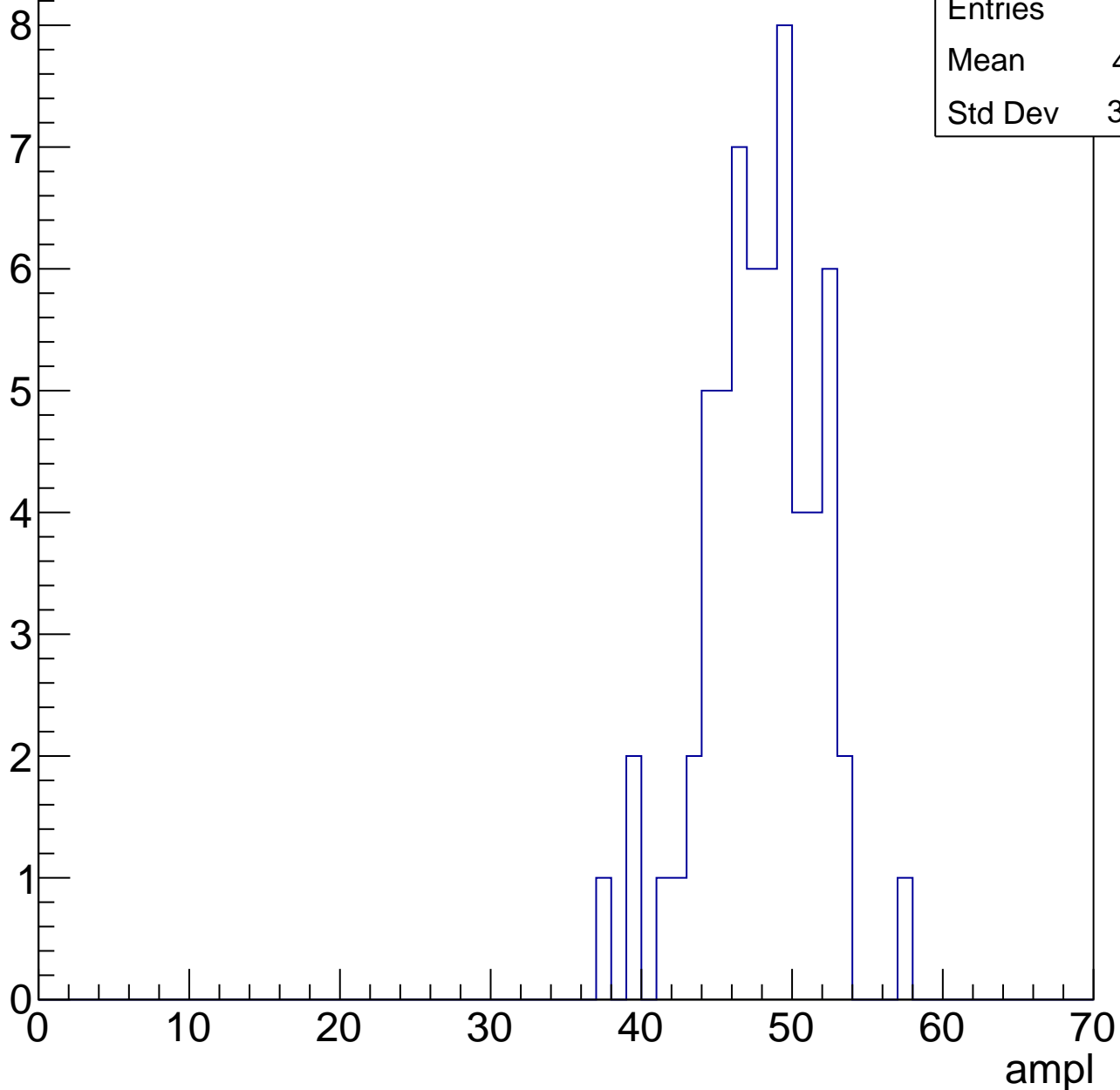


B1L103S, U12-ch90, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	47.41
Std Dev	3.717

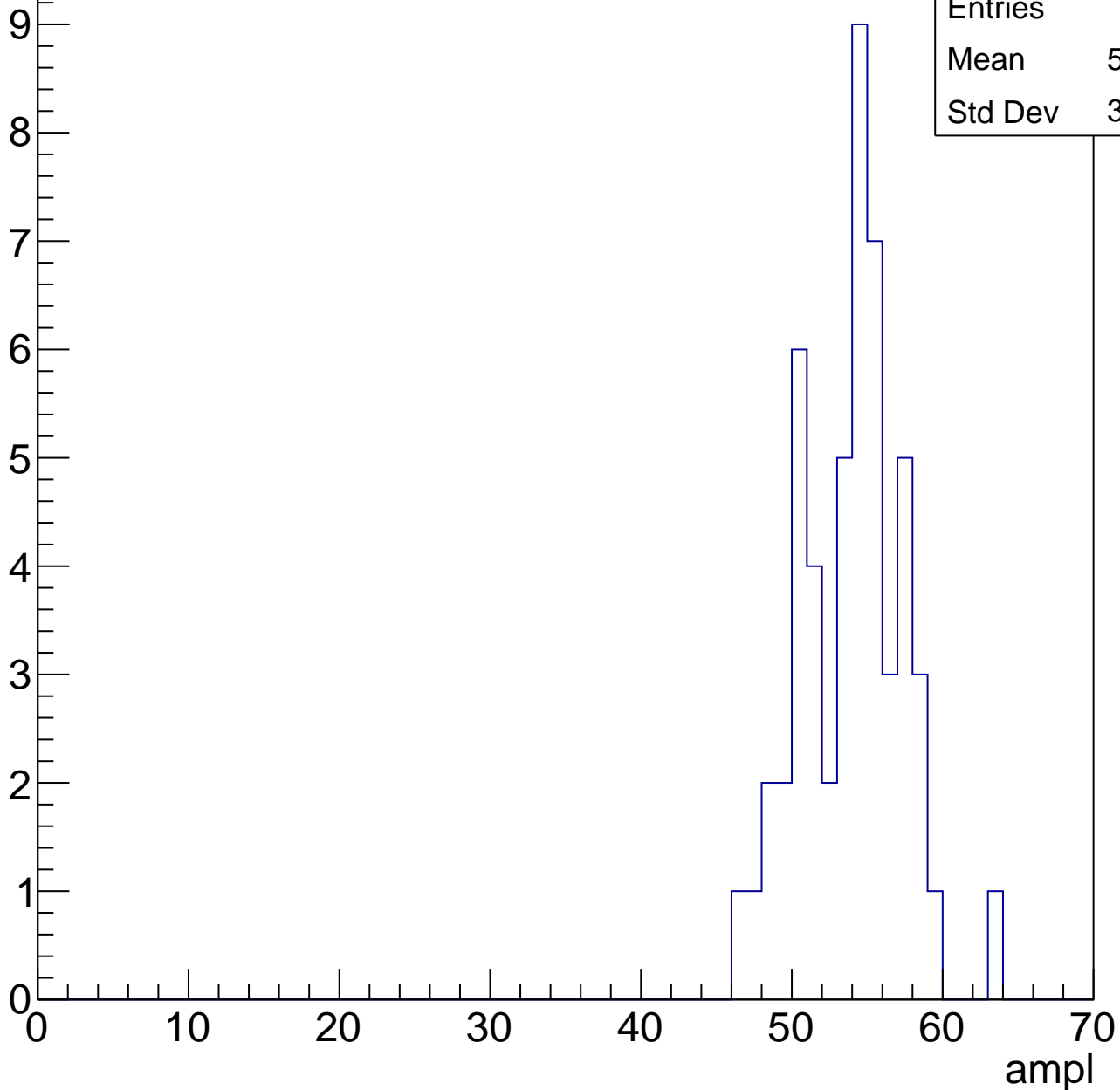


B1L103S, U12-ch90, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	52
Mean	53.46
Std Dev	3.348

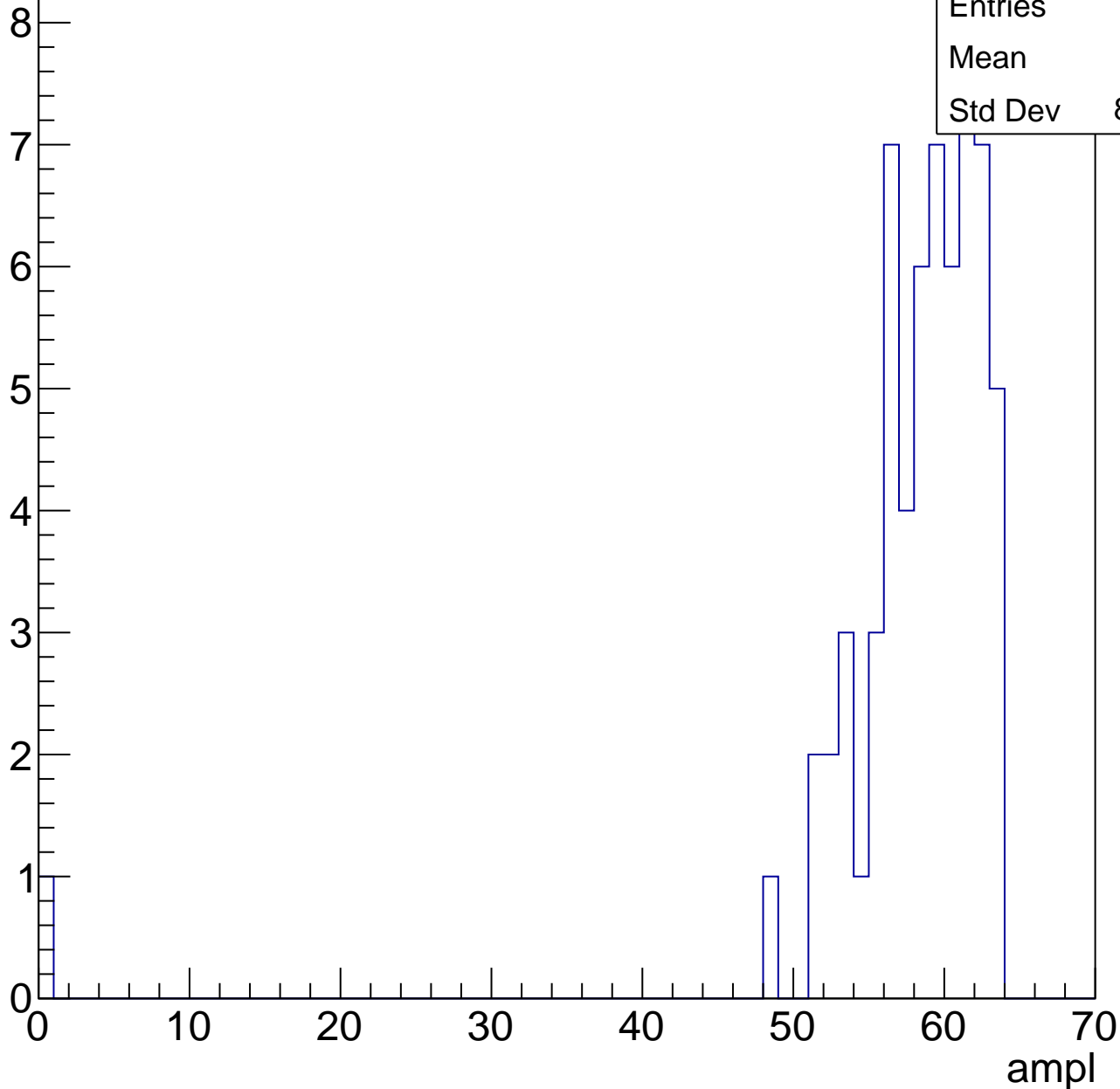


B1L103S, U12-ch90, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

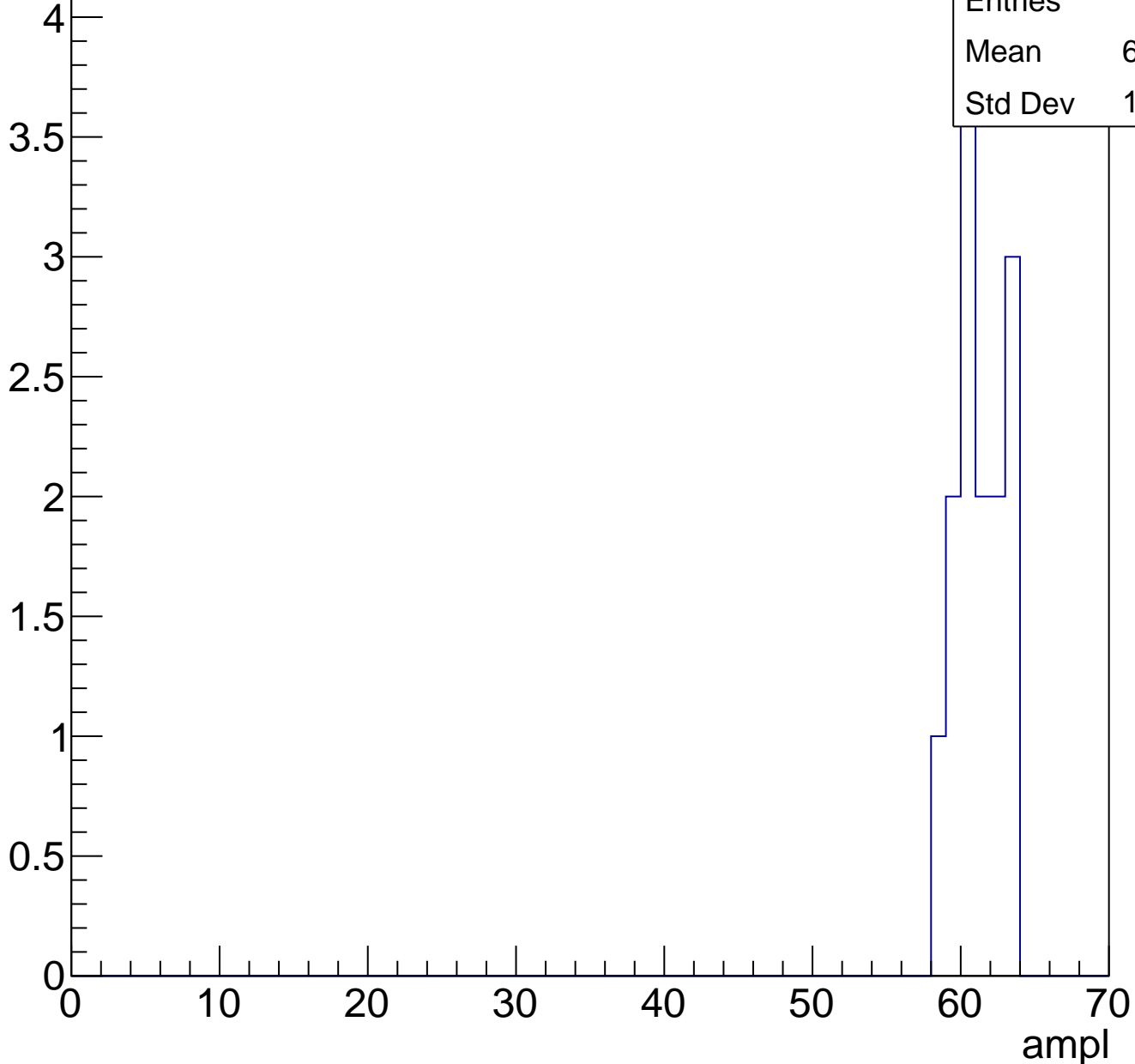
Entries	63
Mean	57.3
Std Dev	8.061



B1L103S, U12-ch90, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



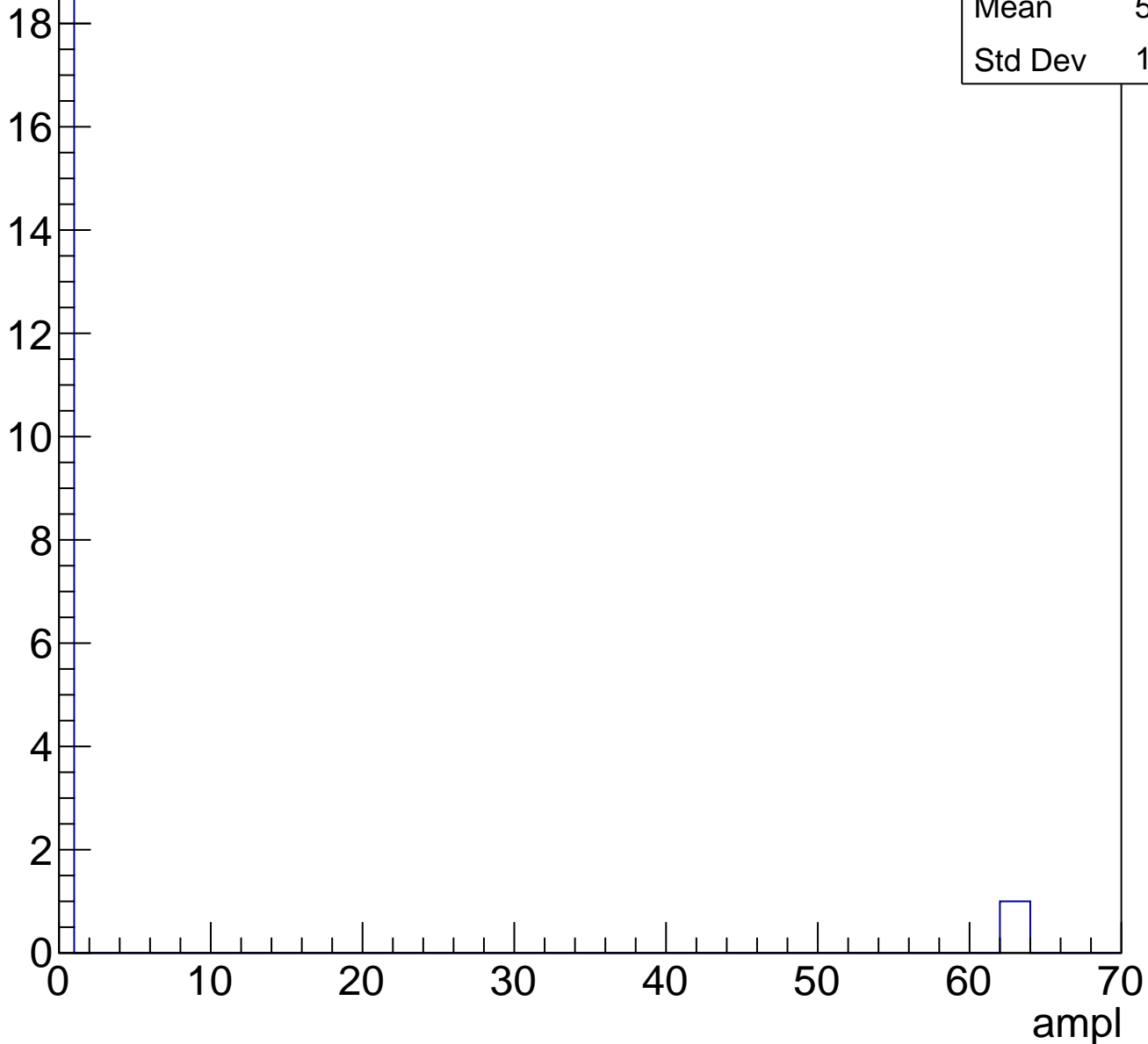
Entries	14
Mean	60.79
Std Dev	1.567

B1L103S, U12-ch90, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	21
Mean	5.952
Std Dev	18.35

Entry

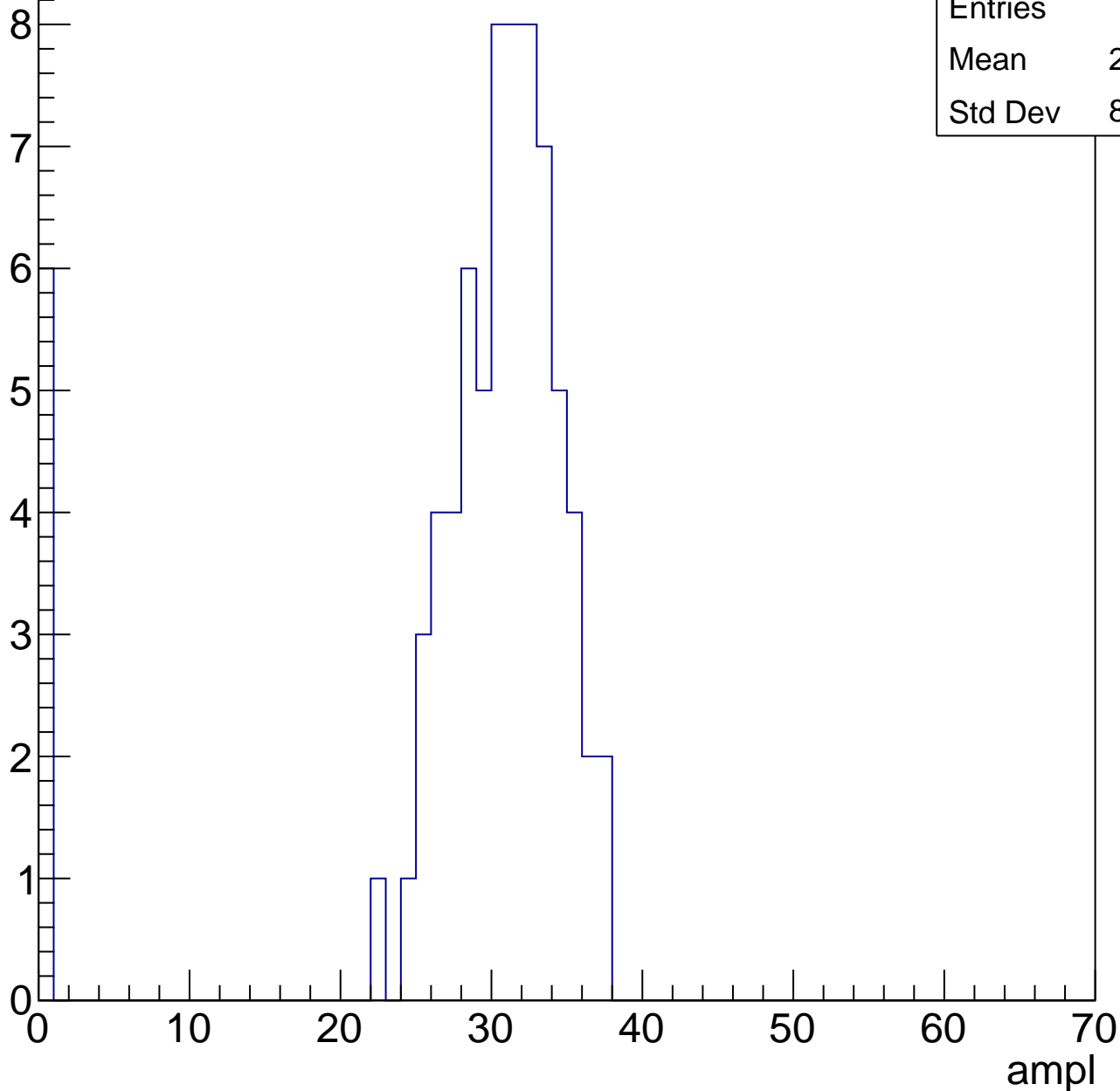


B1L103S, U12-ch91, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

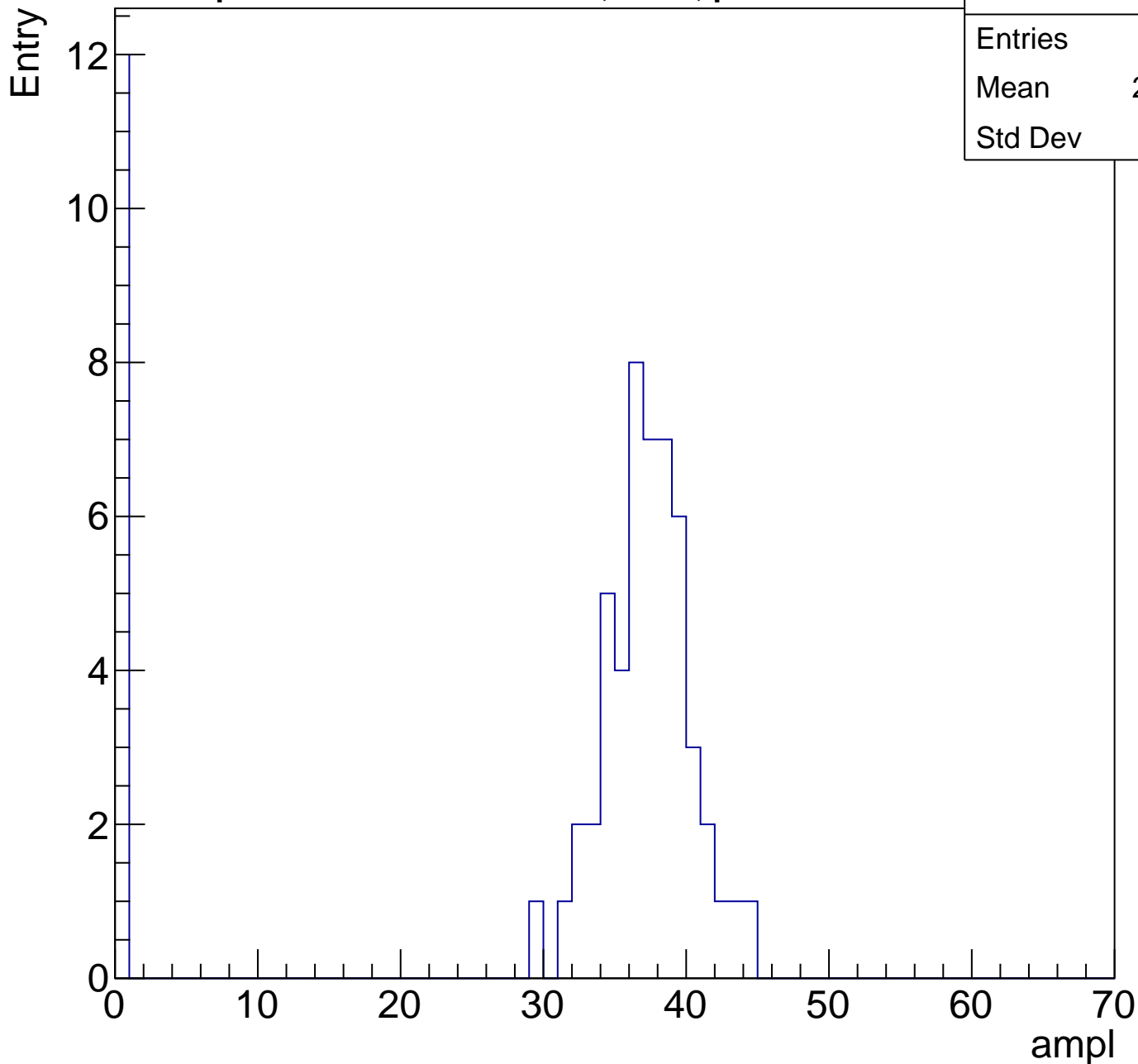
Entries	74
Mean	28.07
Std Dev	8.915



B1L103S, U12-ch91, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	63
Mean	29.81
Std Dev	14.7

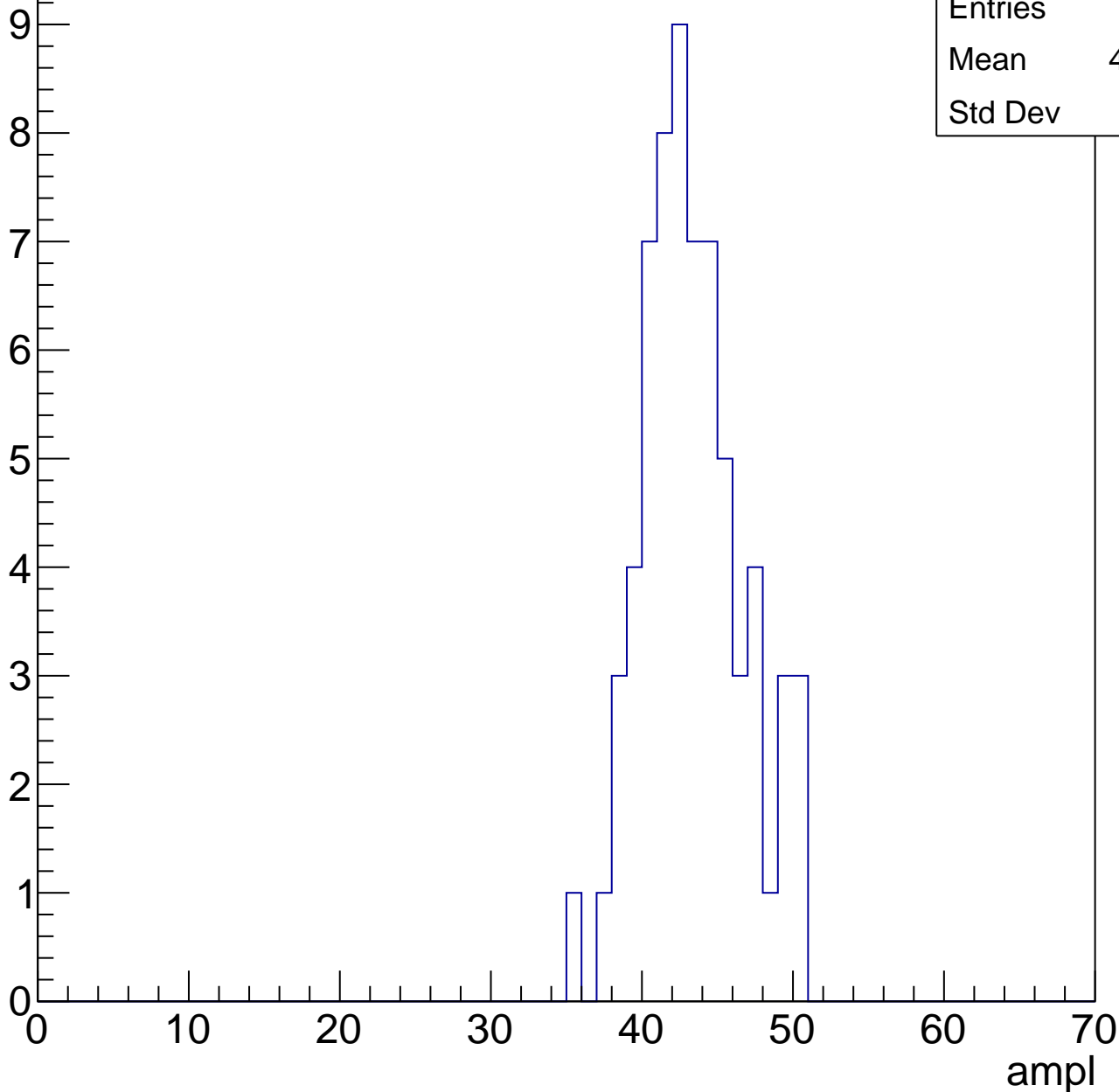


B1L103S, U12-ch91, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	42.92
Std Dev	3.35

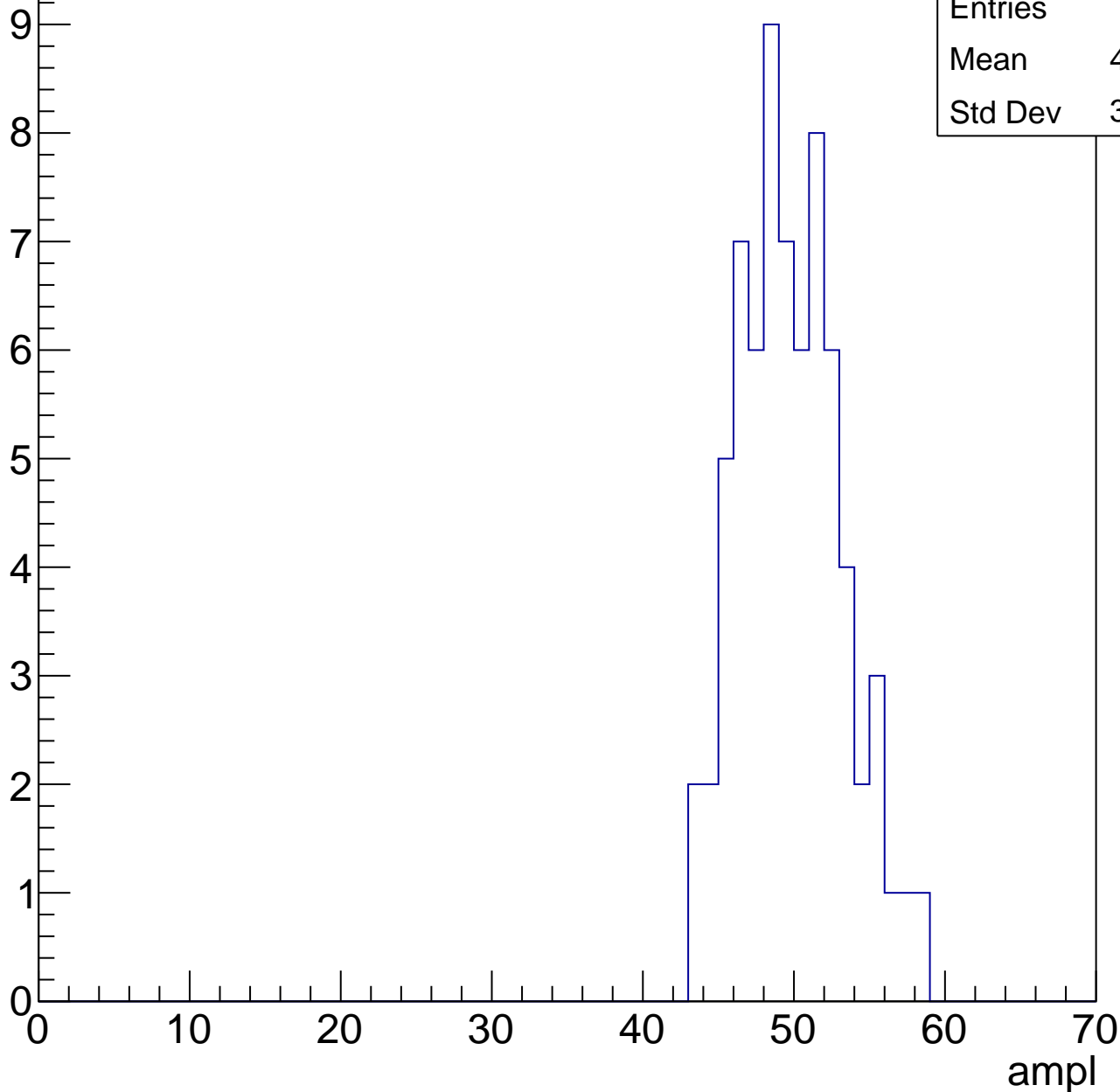


B1L103S, U12-ch91, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	49.34
Std Dev	3.376

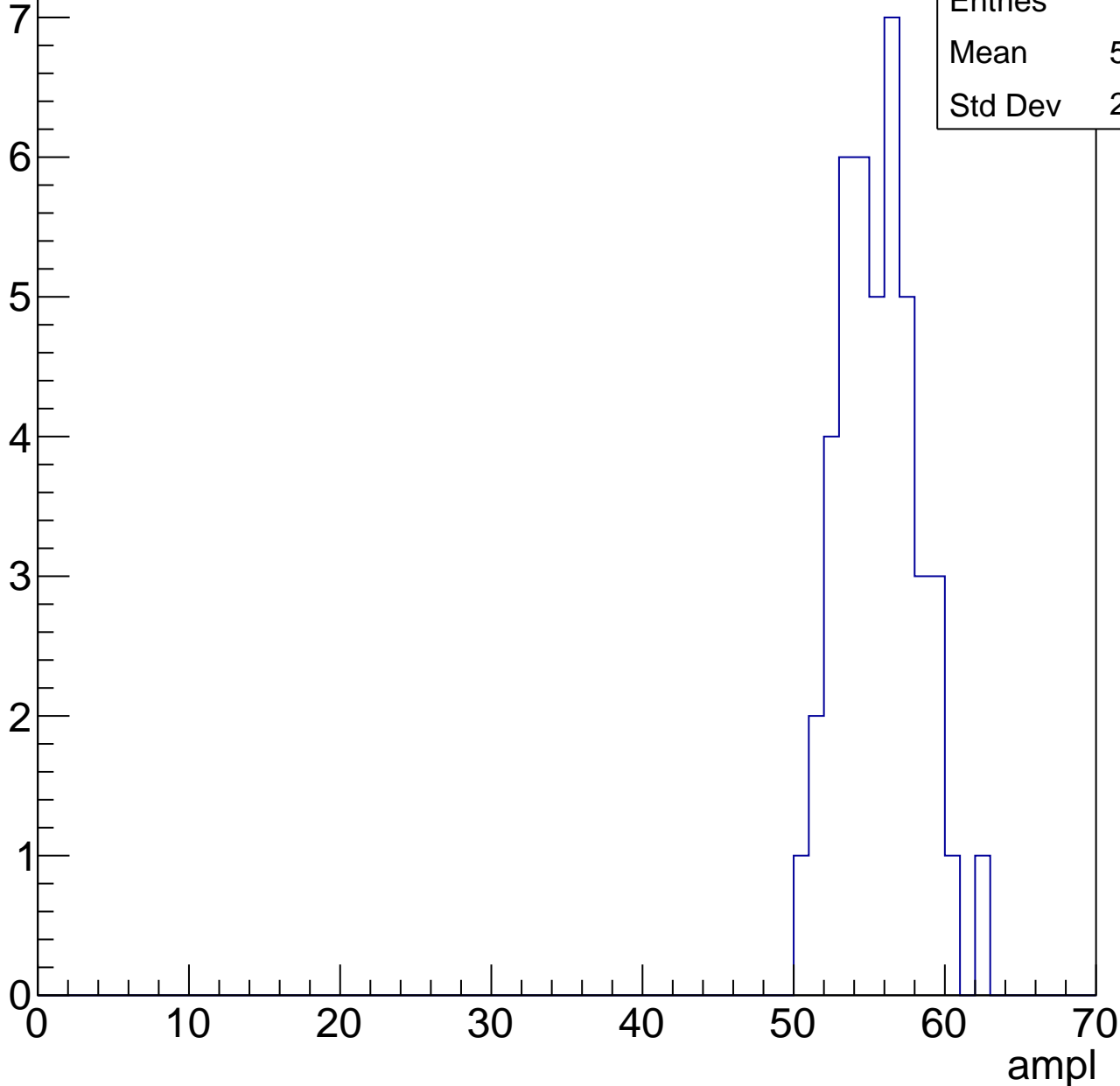


B1L103S, U12-ch91, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

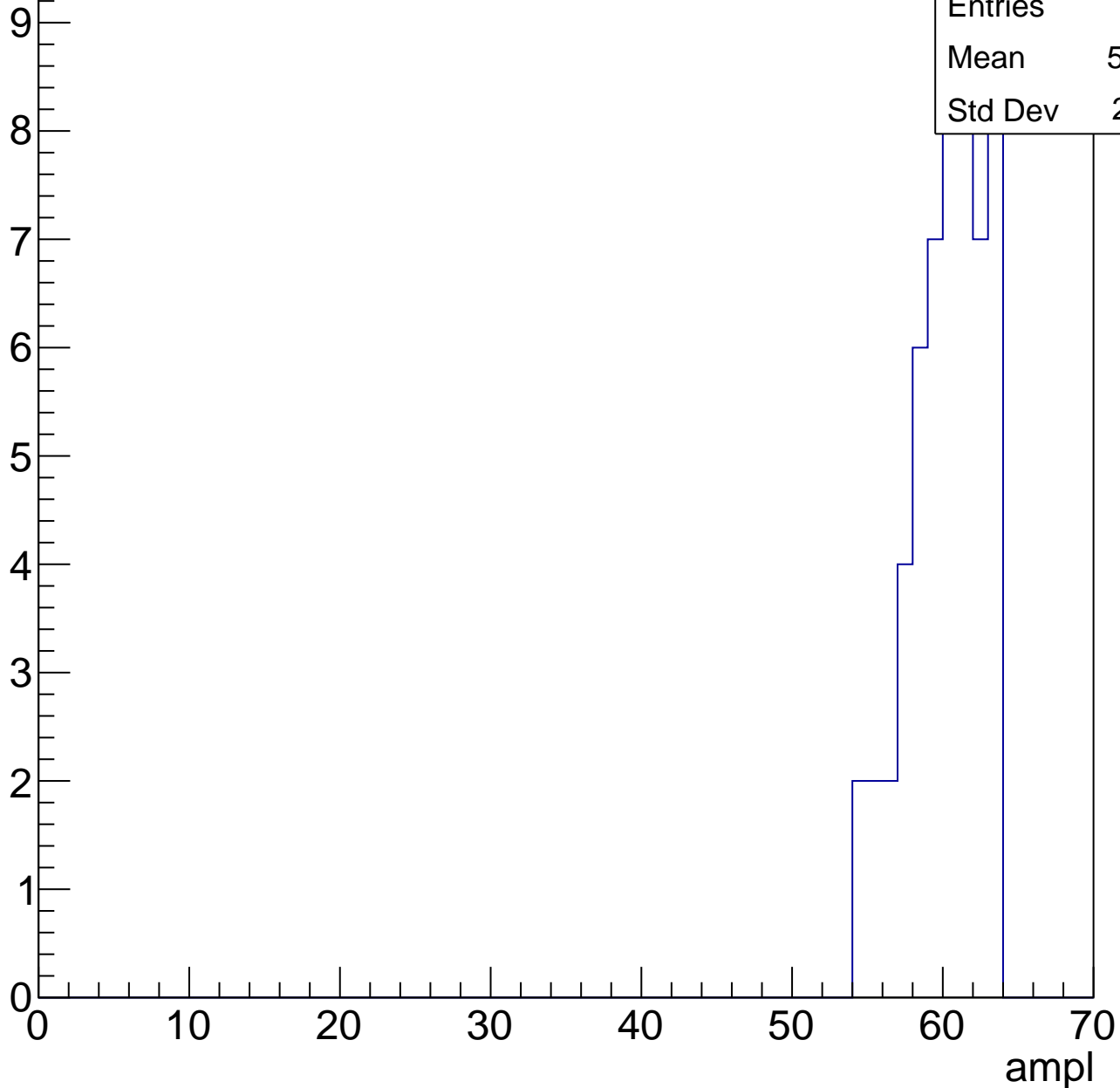
Entries	44
Mean	55.16
Std Dev	2.602



B1L103S, U12-ch91, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	55
Mean	59.73
Std Dev	2.431

B1L103S, U12-ch91, adc6

calib_packv5_041523_1651.root, FC#0, port C2

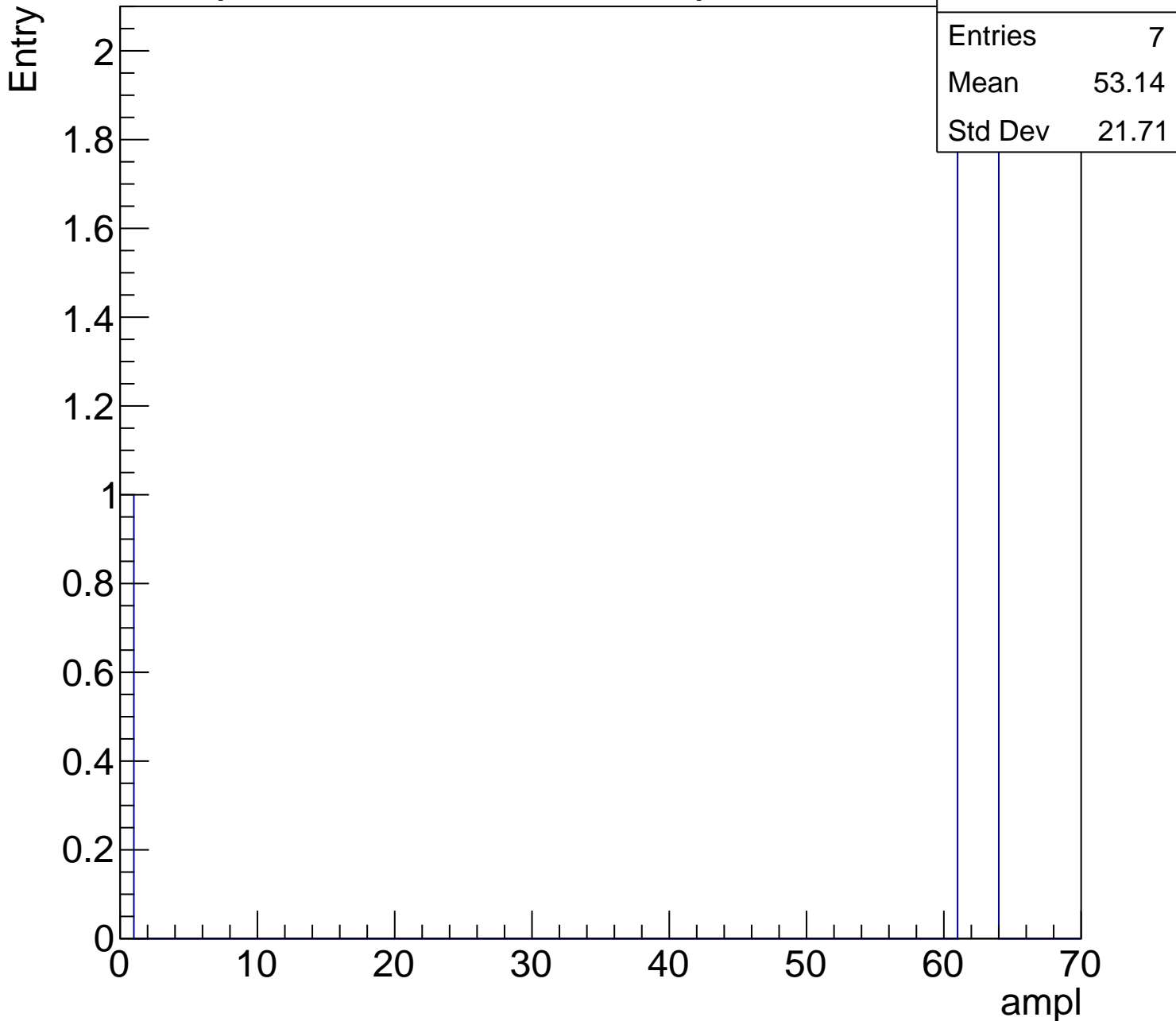
Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	7
Mean	53.14
Std Dev	21.71

0 10 20 30 40 50 60 70

ampl

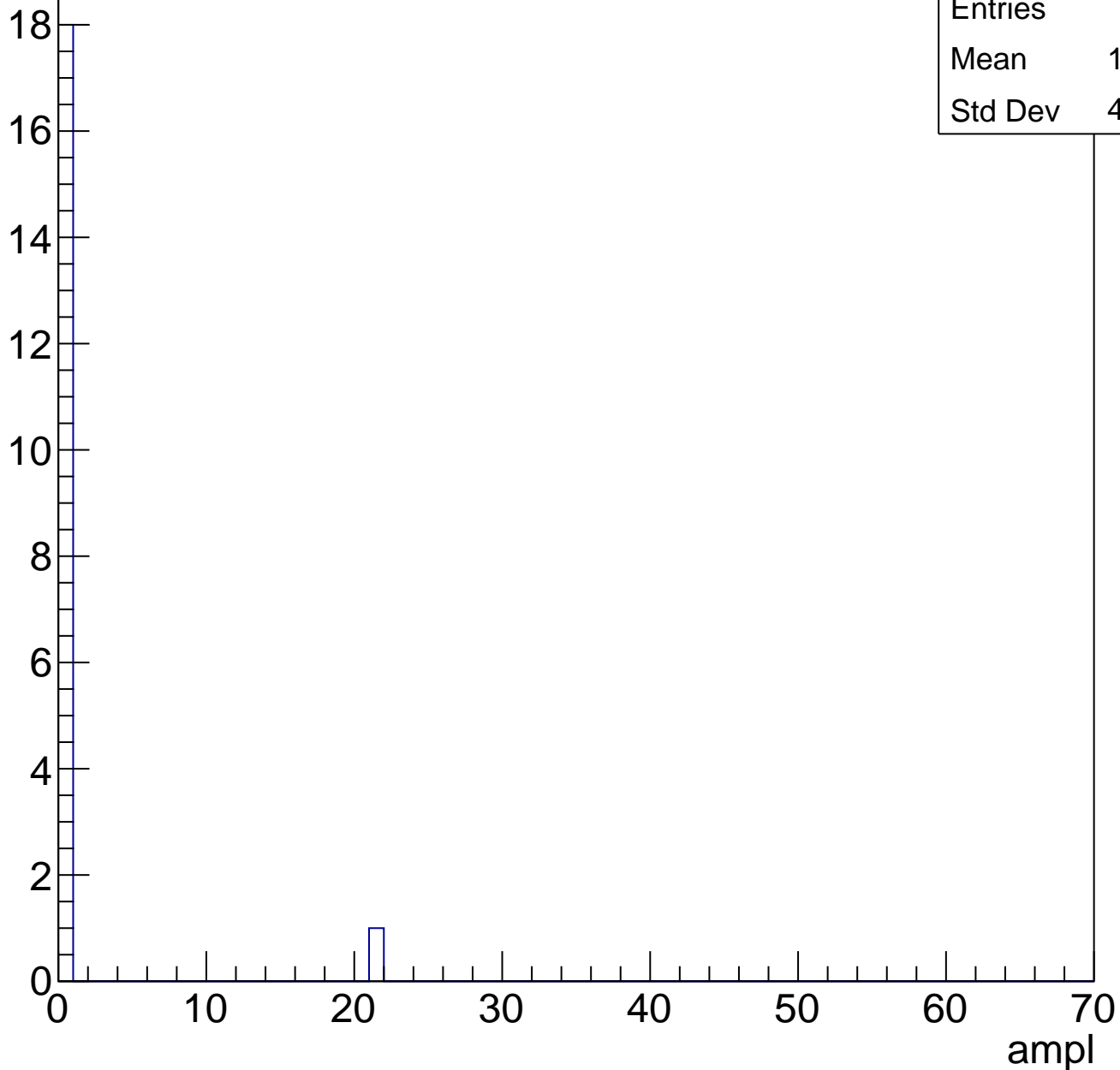


B1L103S, U12-ch91, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.105
Std Dev	4.689

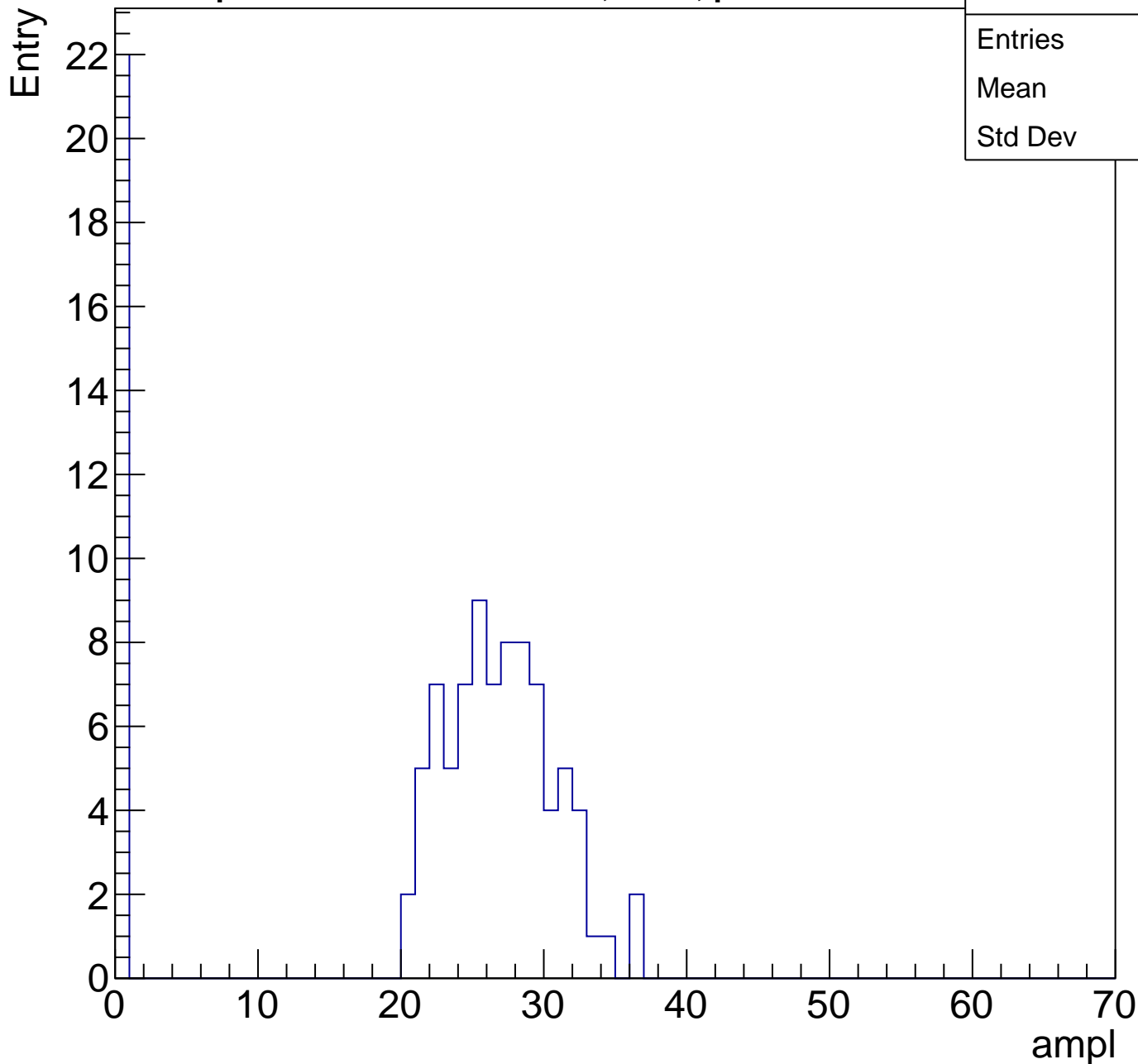
Entry



B1L103S, U12-ch92, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	104
Mean	20.9
Std Dev	11.31

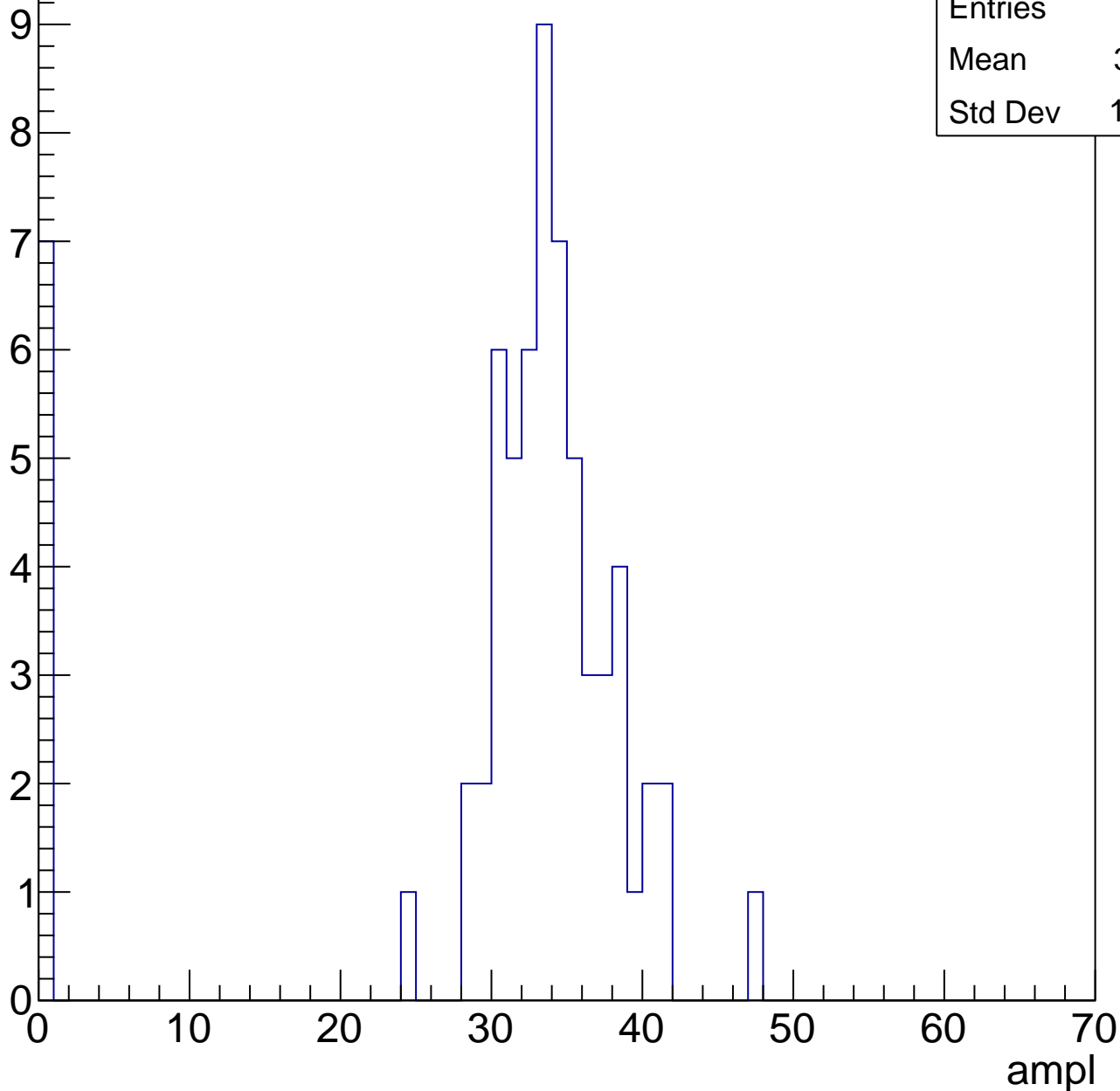


B1L103S, U12-ch92, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	30.21
Std Dev	11.02

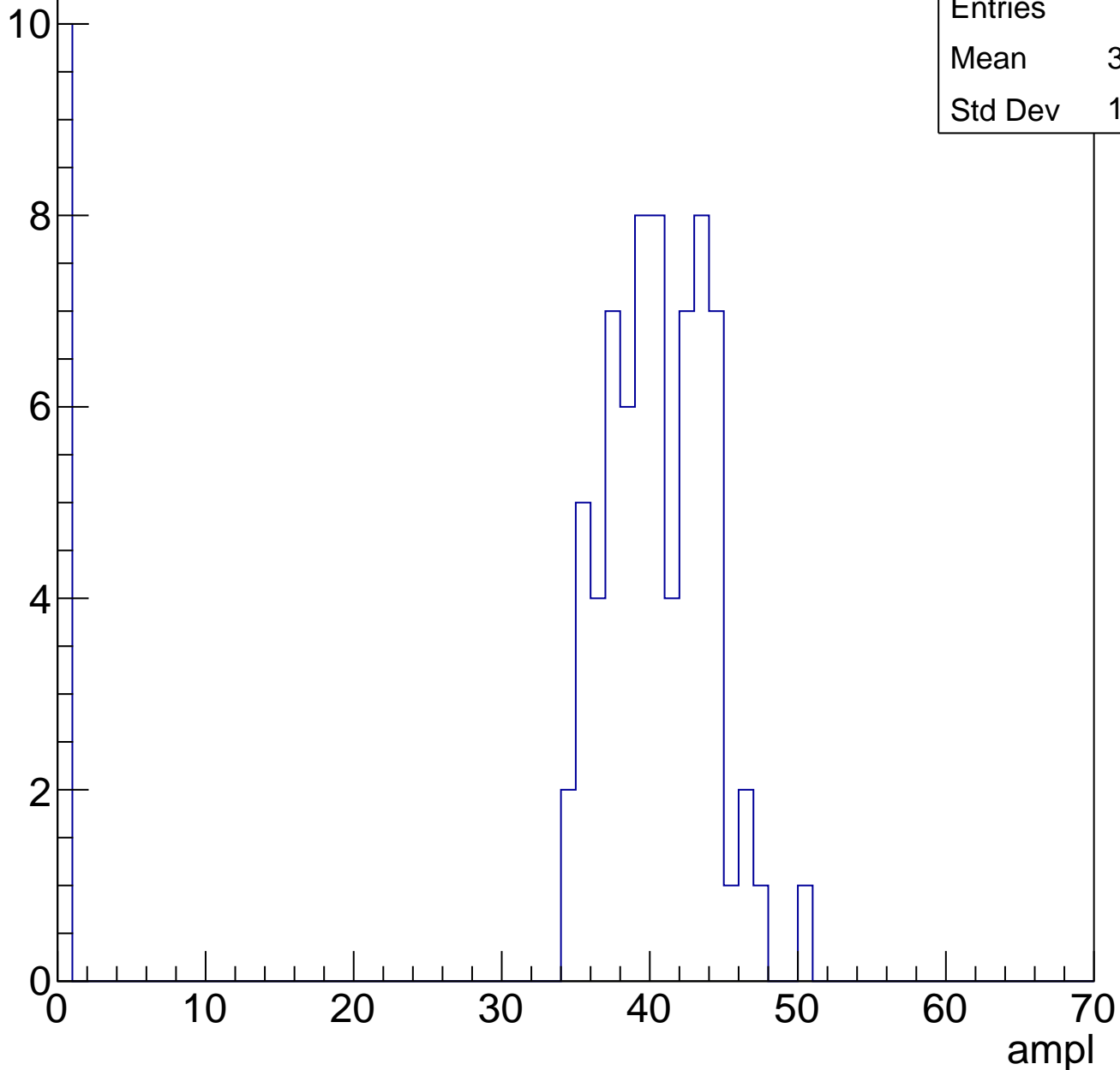


B1L103S, U12-ch92, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	81
Mean	35.19
Std Dev	13.58

Entry

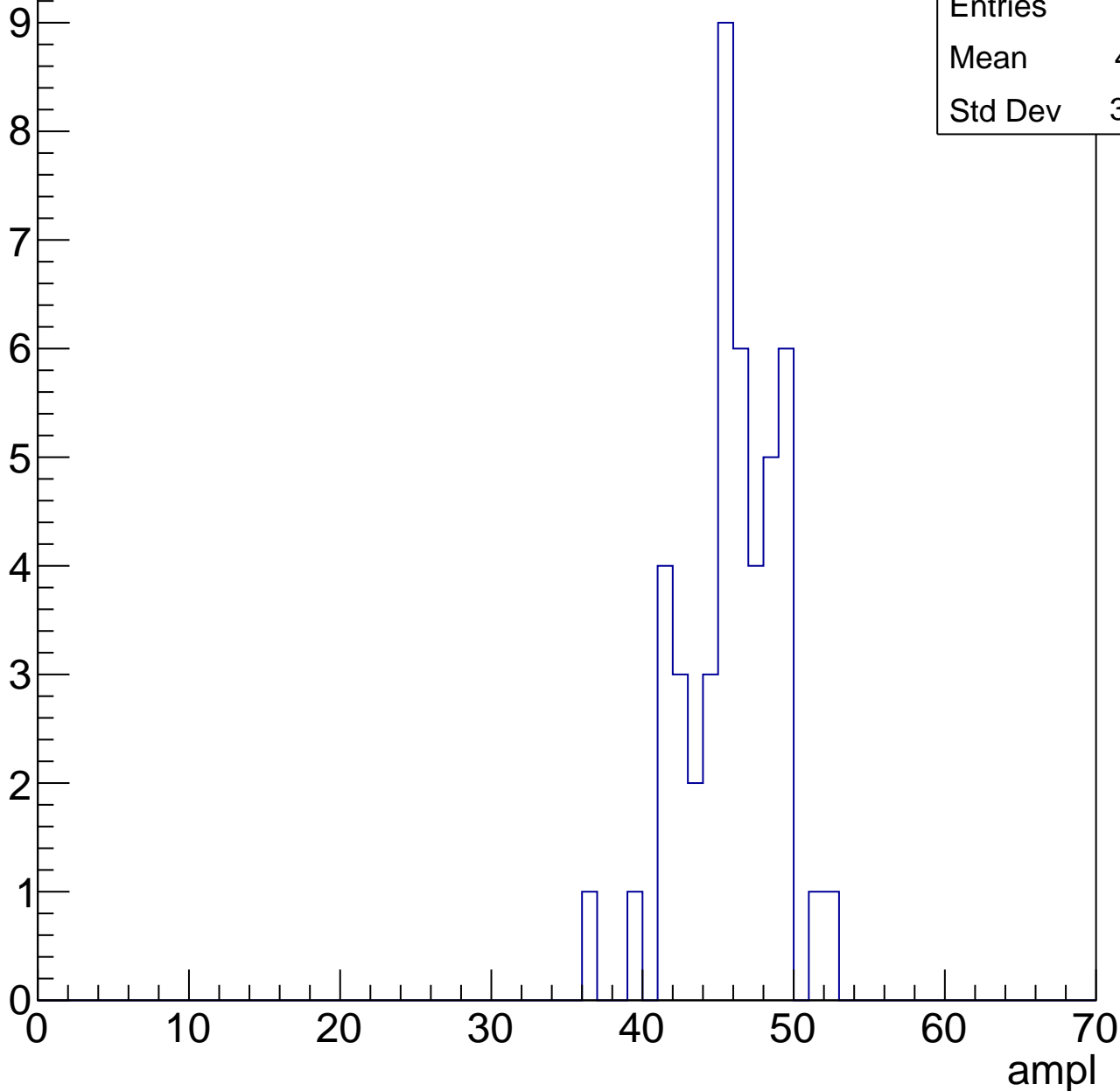


B1L103S, U12-ch92, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

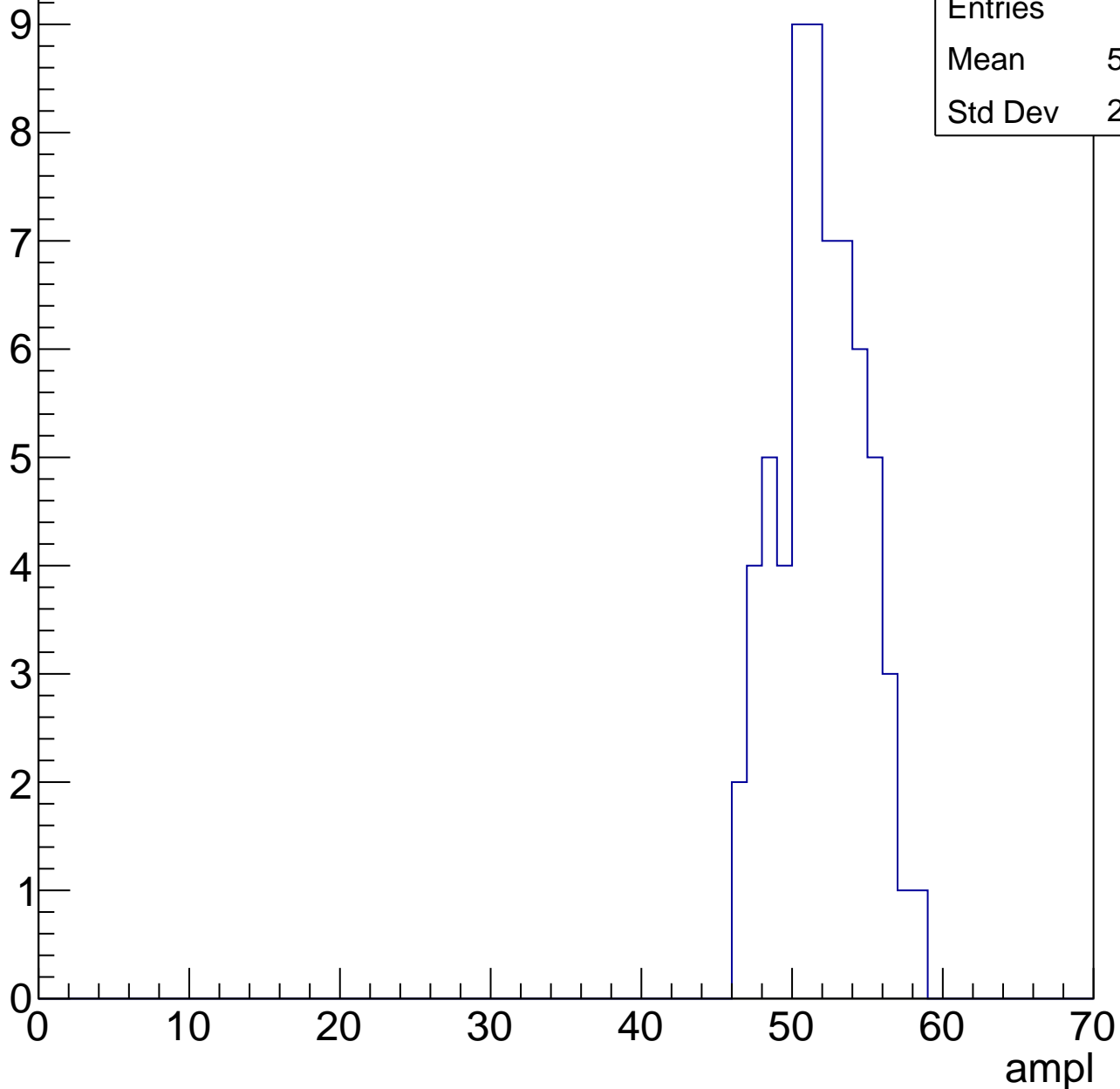
Entries	46
Mean	45.41
Std Dev	3.159



B1L103S, U12-ch92, adc4

calib_packv5_041523_1651.root, FC#0, port C2

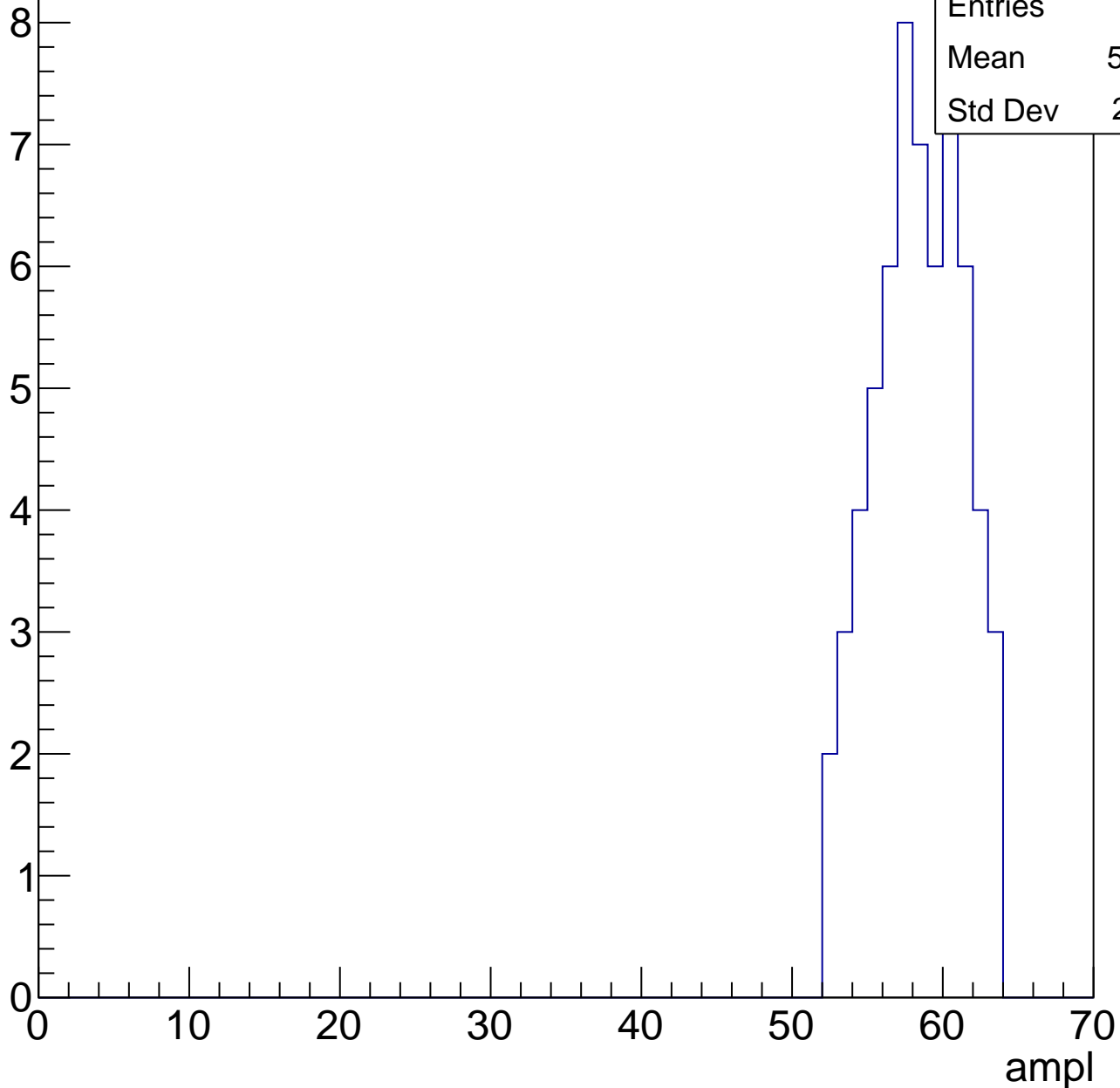
Entry



B1L103S, U12-ch92, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

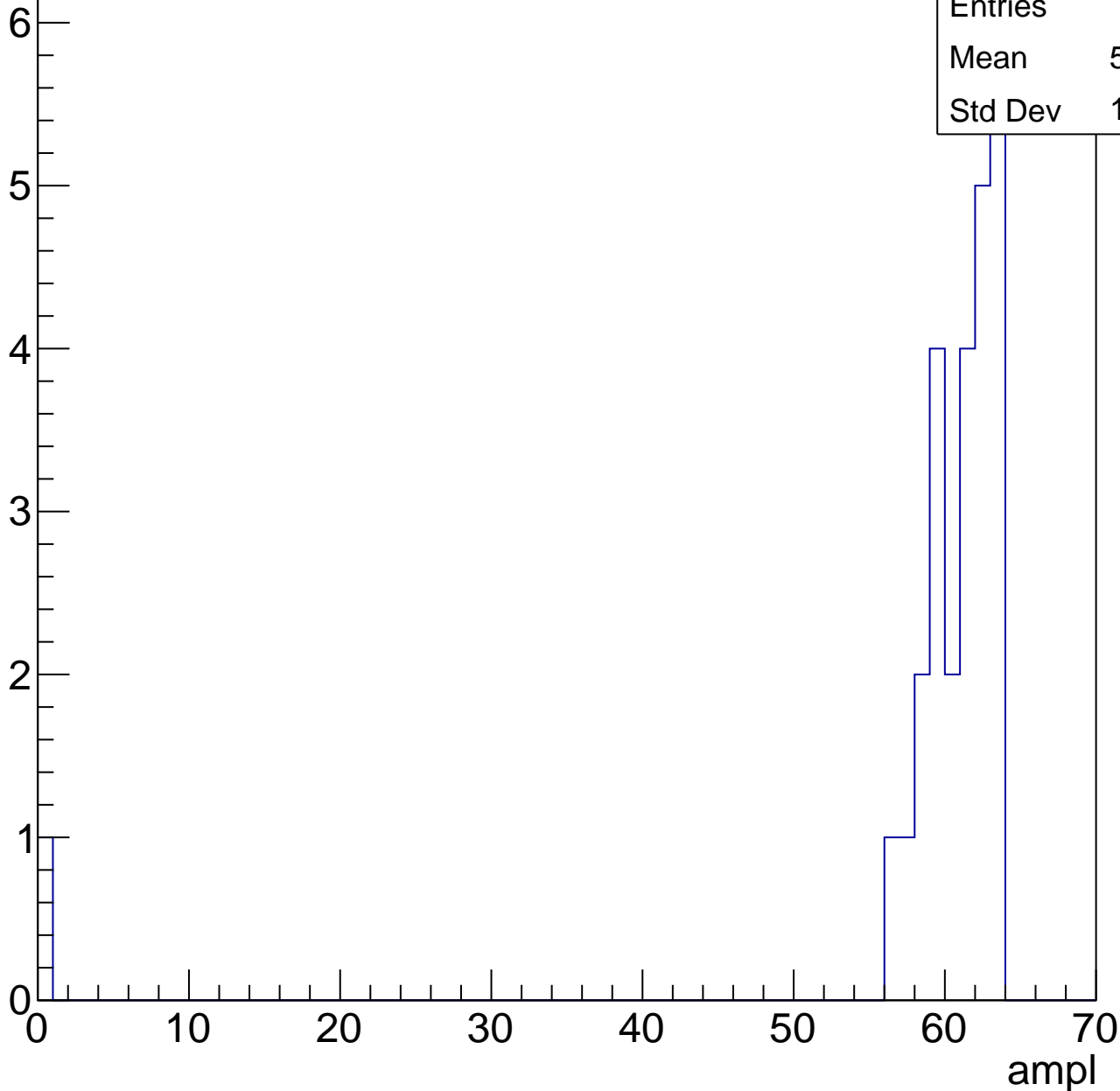


B1L103S, U12-ch92, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	26
Mean	58.35
Std Dev	11.84

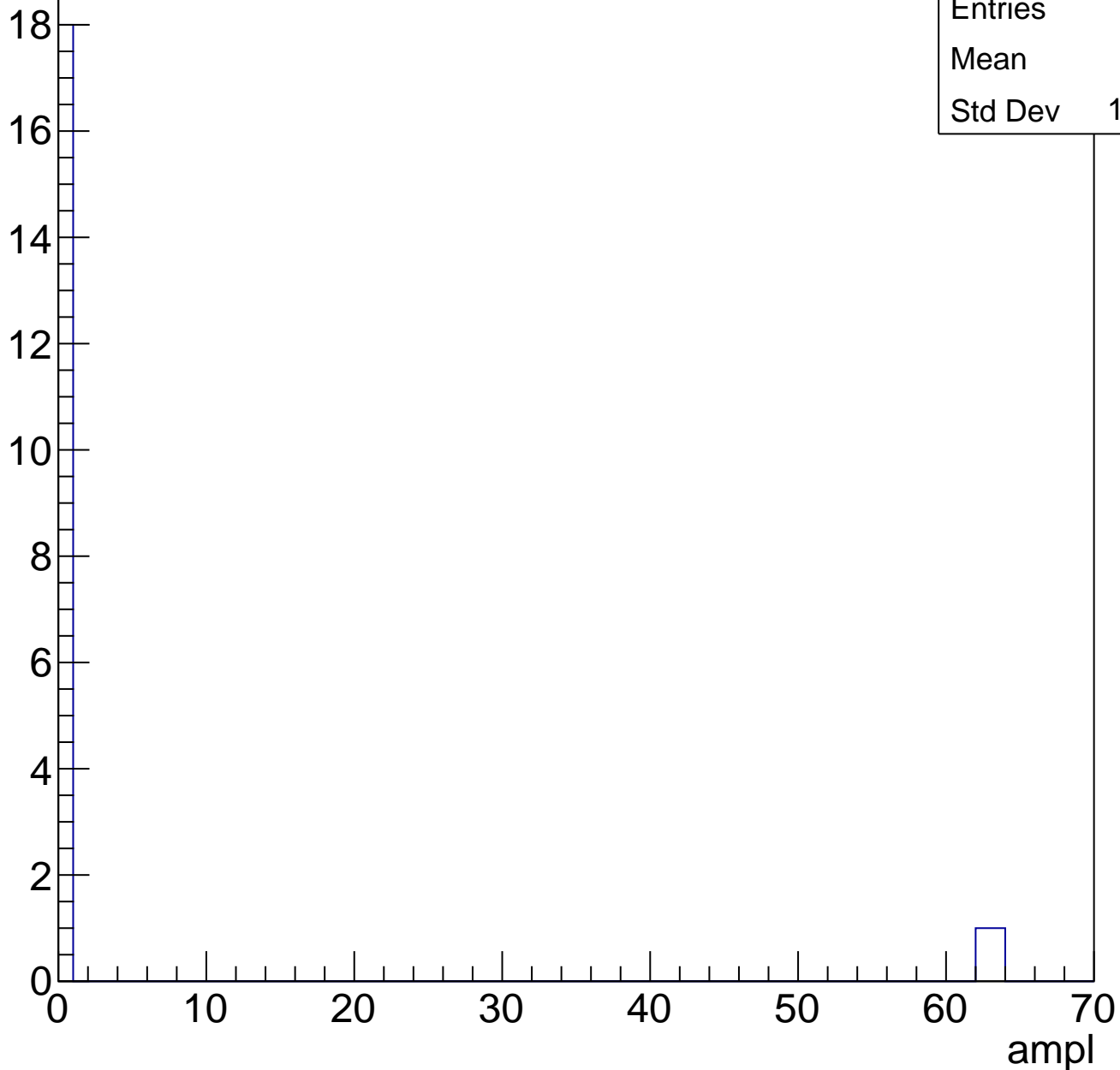


B1L103S, U12-ch92, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	6.25
Std Dev	18.75

Entry

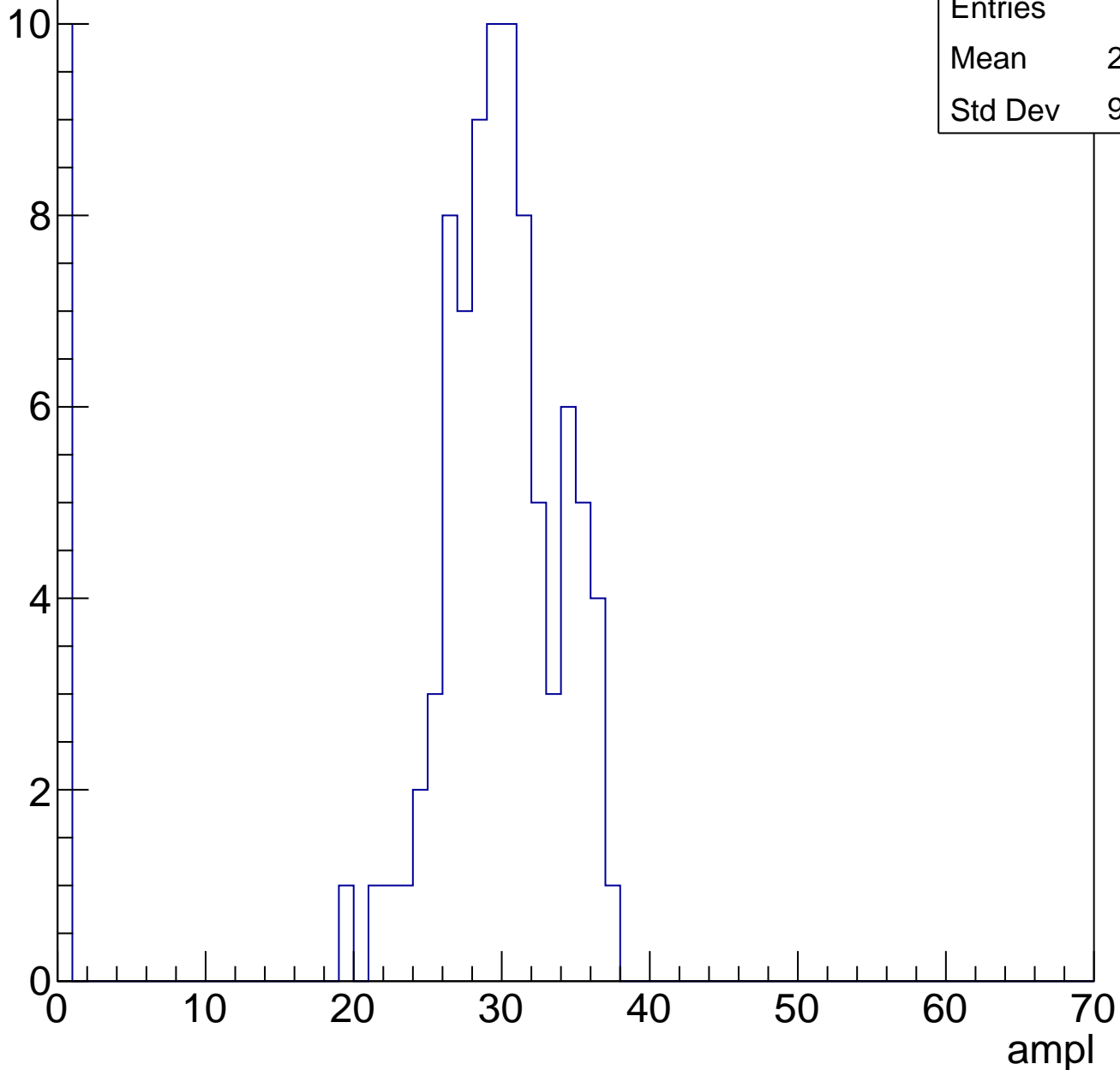


B1L103S, U12-ch93, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	95
Mean	26.46
Std Dev	9.722

Entry

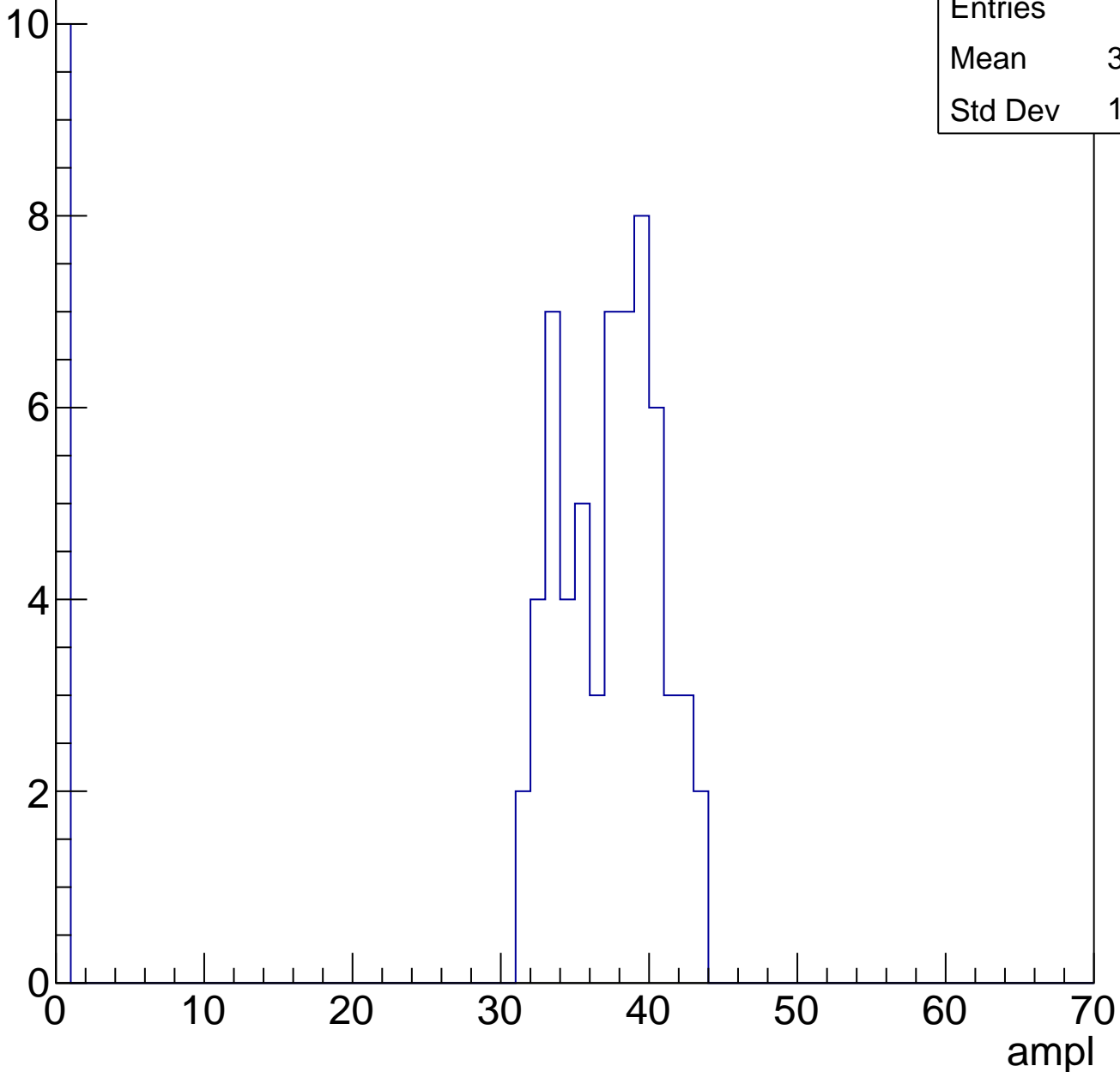


B1L103S, U12-ch93, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	71
Mean	31.72
Std Dev	13.18

Entry

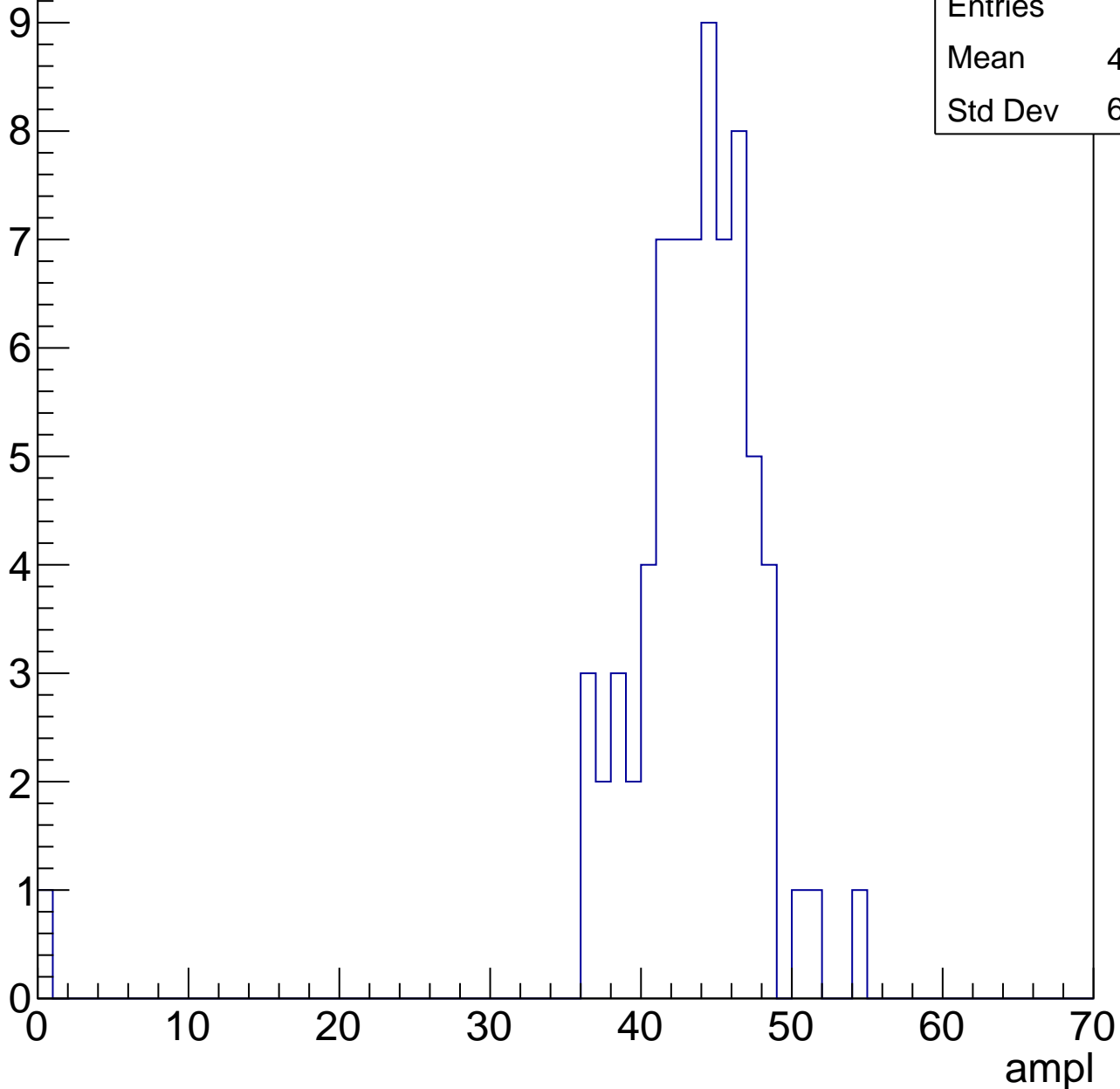


B1L103S, U12-ch93, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	72
Mean	42.74
Std Dev	6.196



B1L103S, U12-ch93, adc3

calib_packv5_041523_1651.root, FC#0, port C2

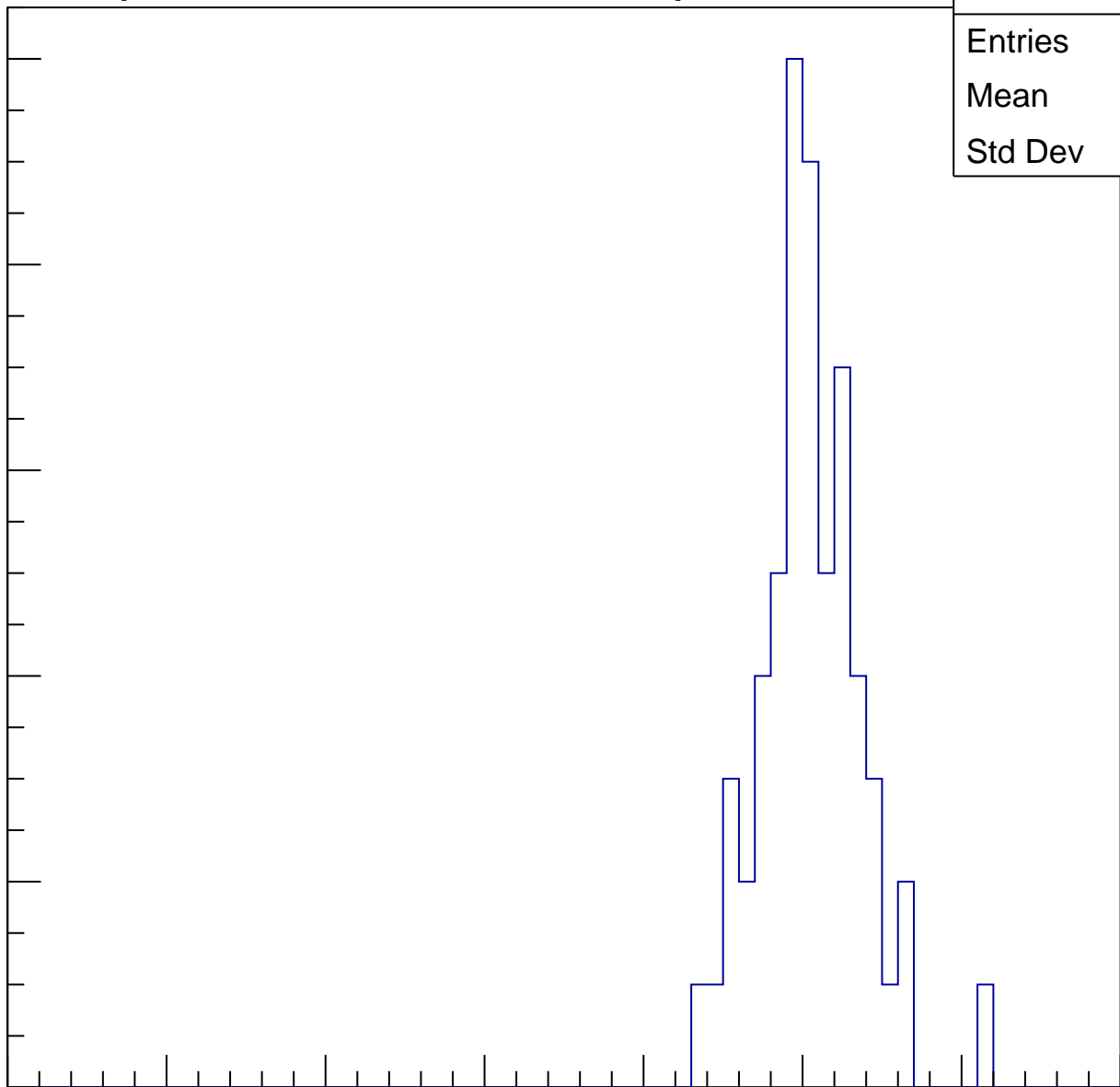
Entries	58
Mean	50.05
Std Dev	3.197

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

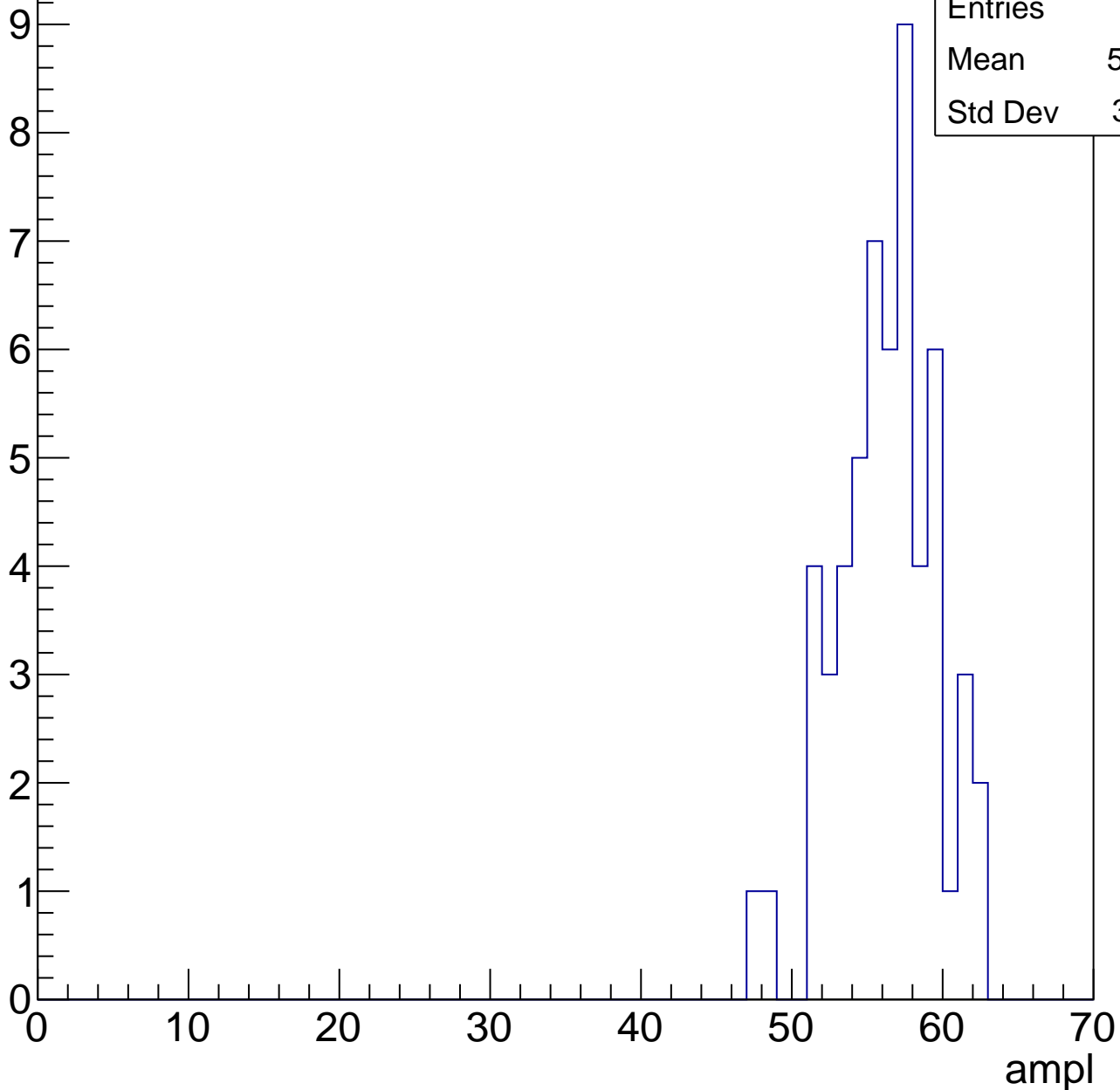


B1L103S, U12-ch93, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

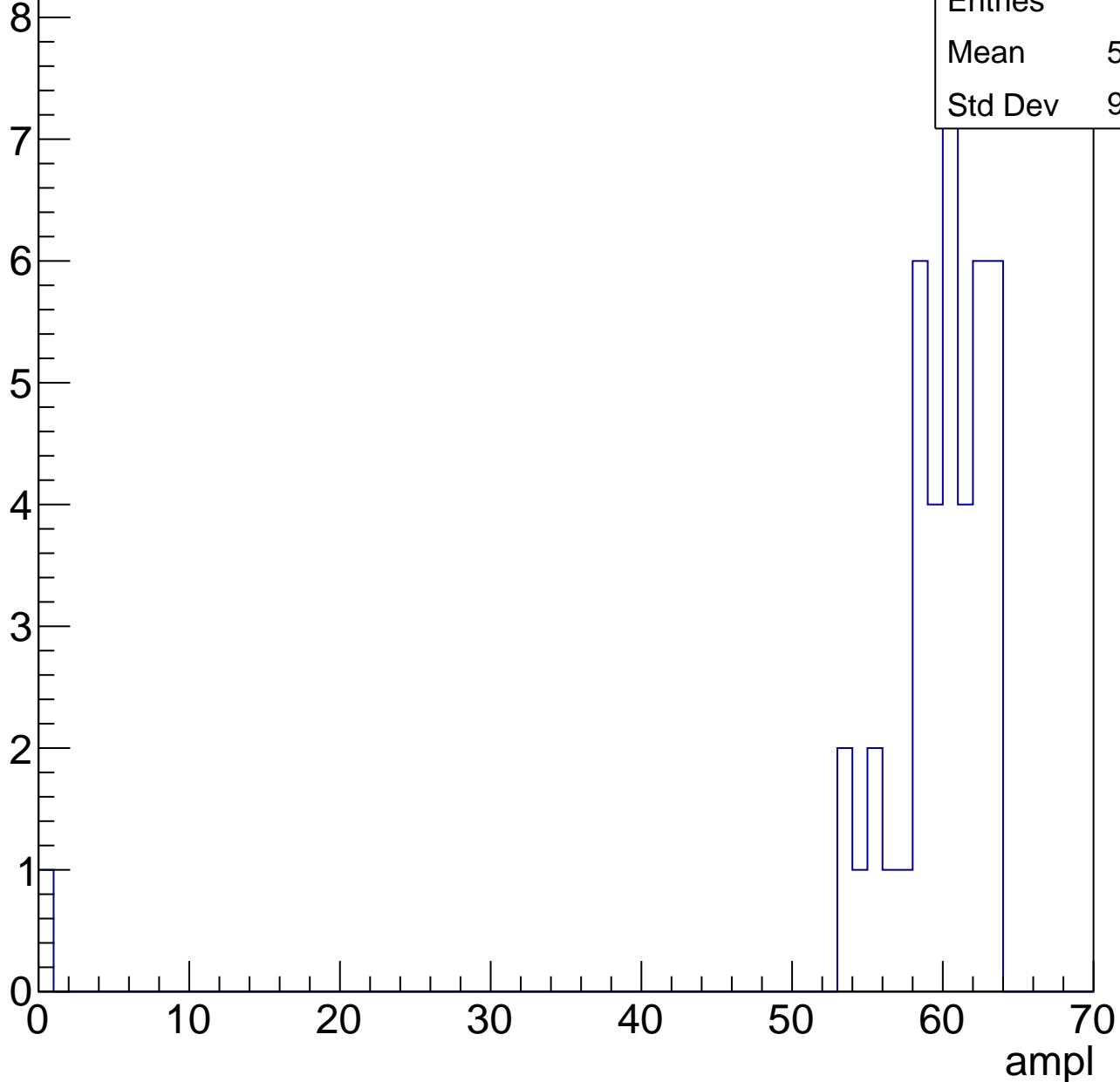
Entries	56
Mean	55.79
Std Dev	3.261



B1L103S, U12-ch93, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch93, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries

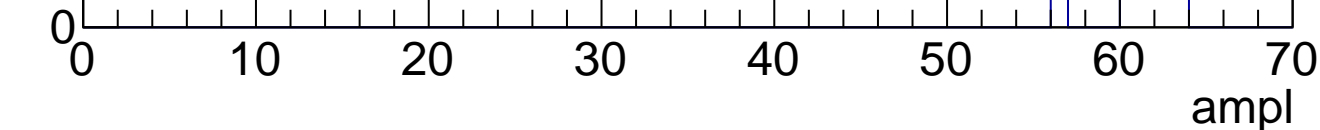
9

Mean

61.22

Std Dev

2.096

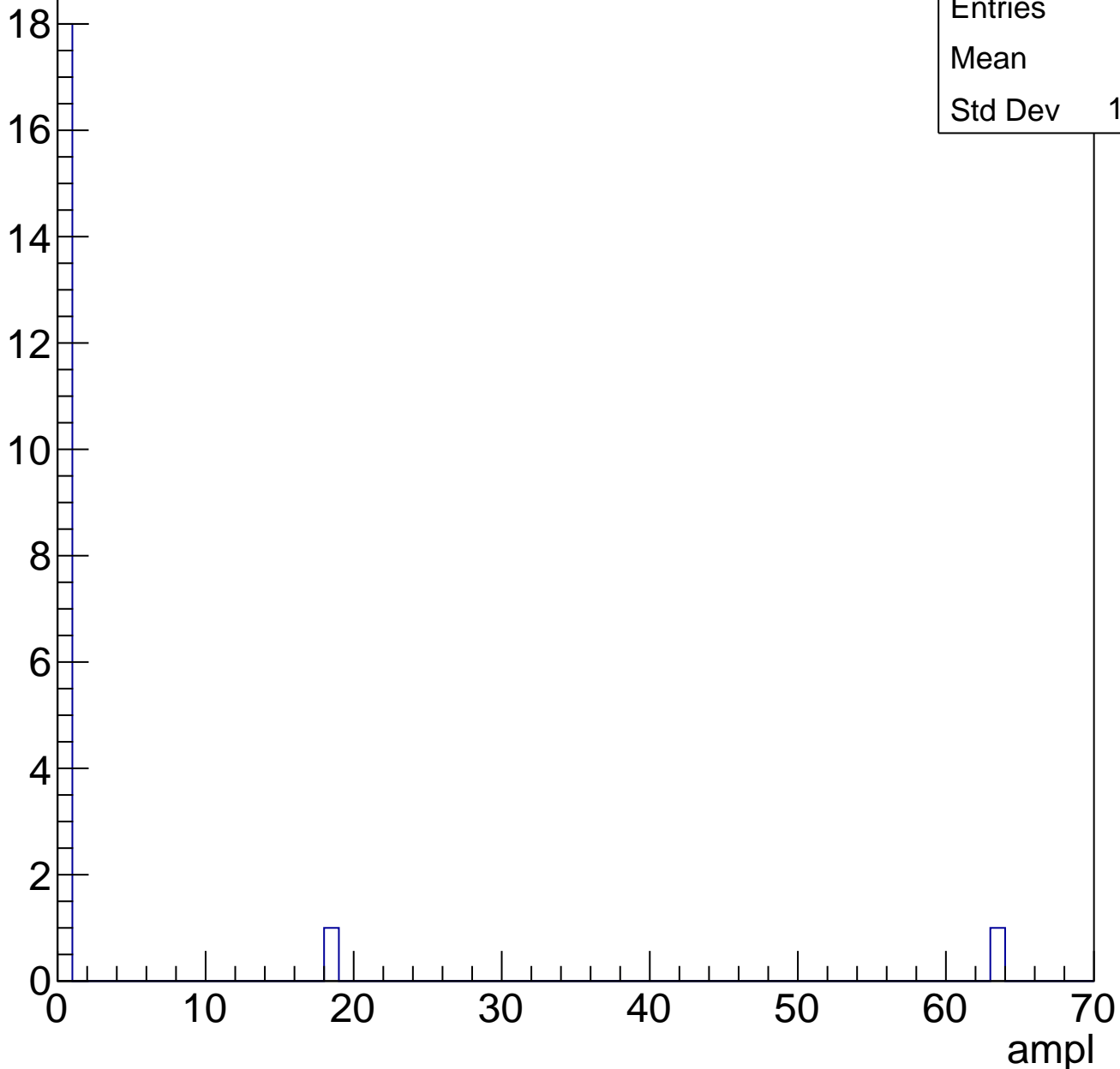


B1L103S, U12-ch93, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	4.05
Std Dev	14.08

Entry

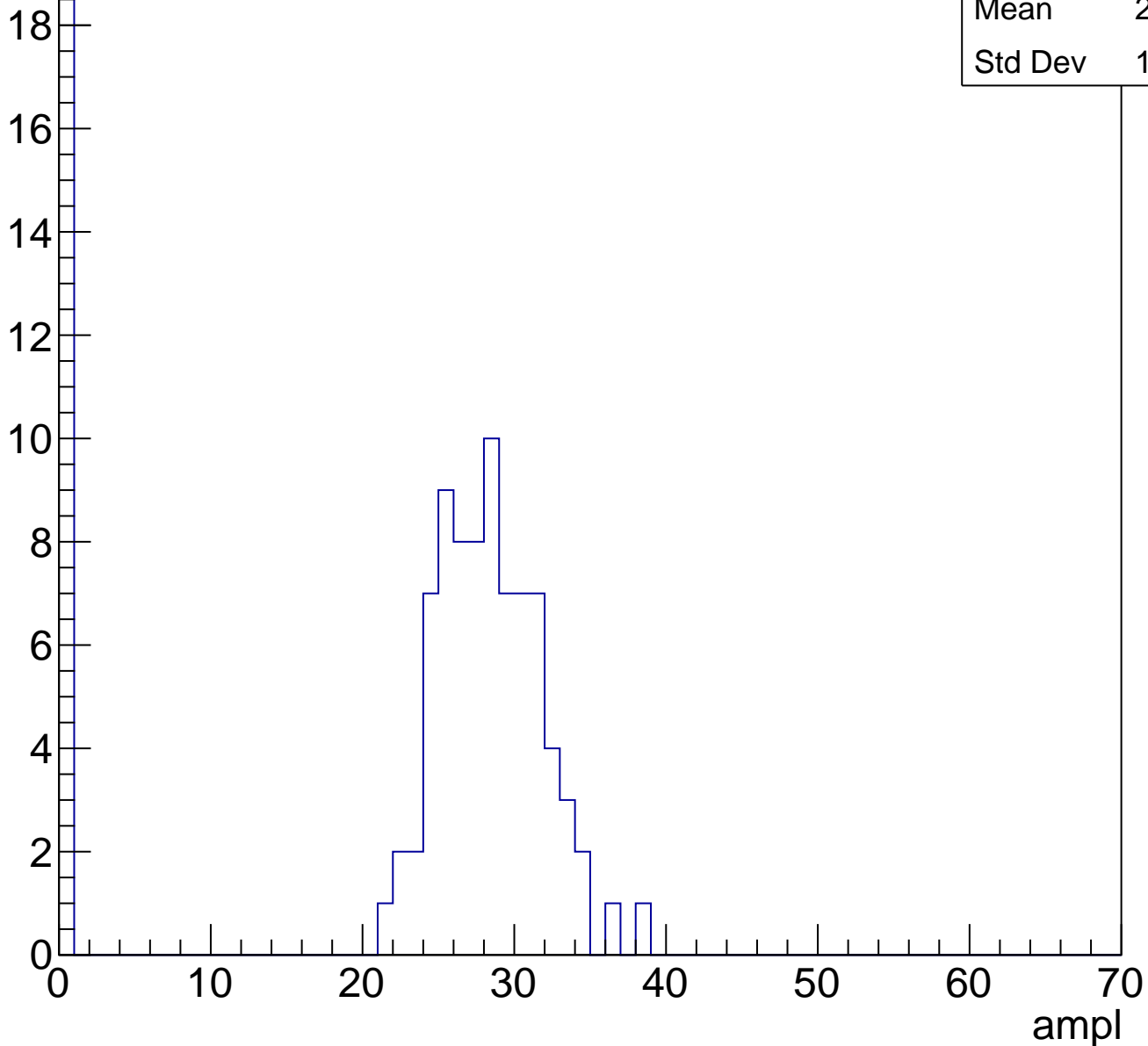


B1L103S, U12-ch94, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	98
Mean	22.52
Std Dev	11.44

Entry

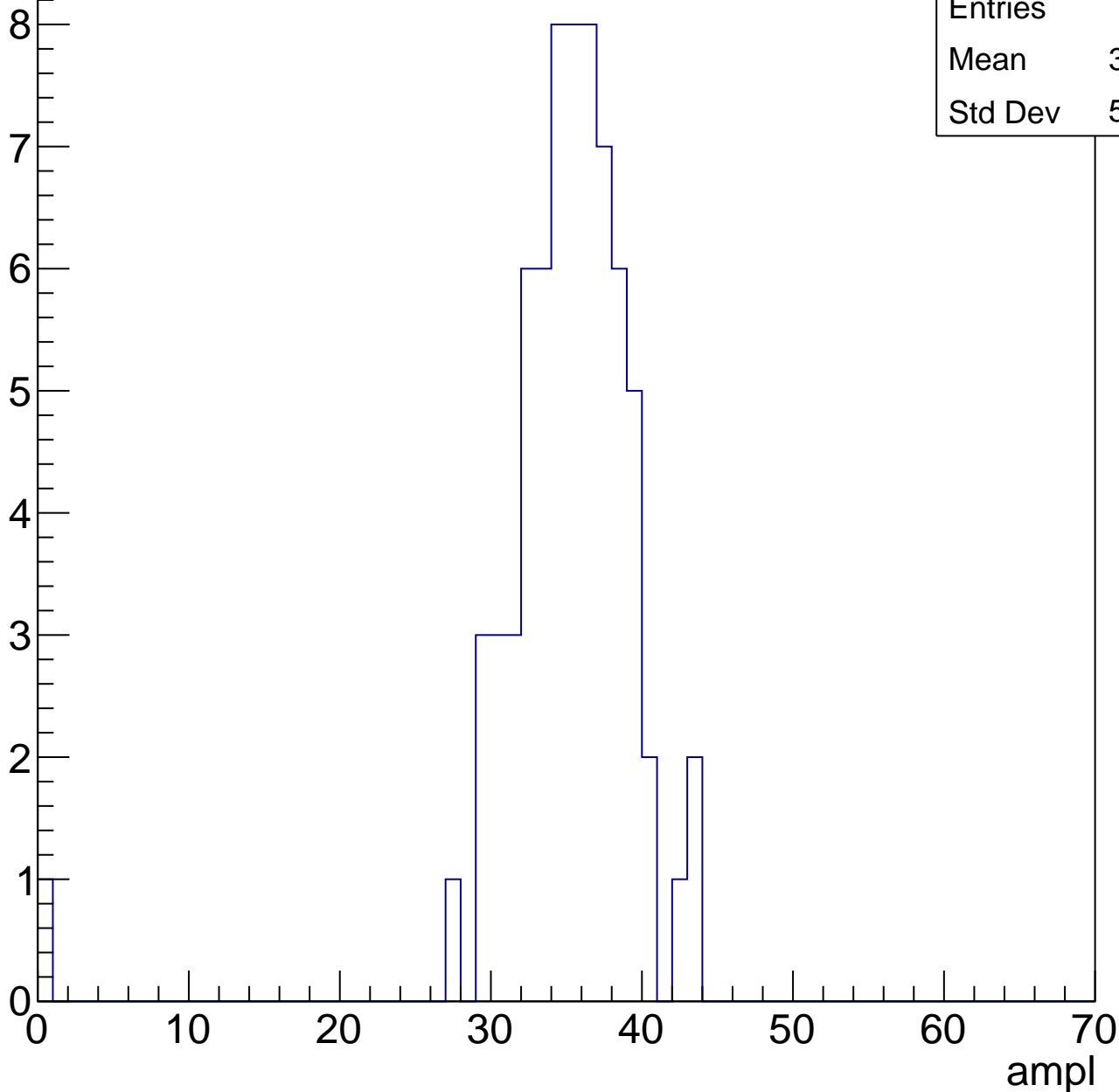


B1L103S, U12-ch94, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	34.53
Std Dev	5.328



B1L103S, U12-ch94, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

10

8

6

4

2

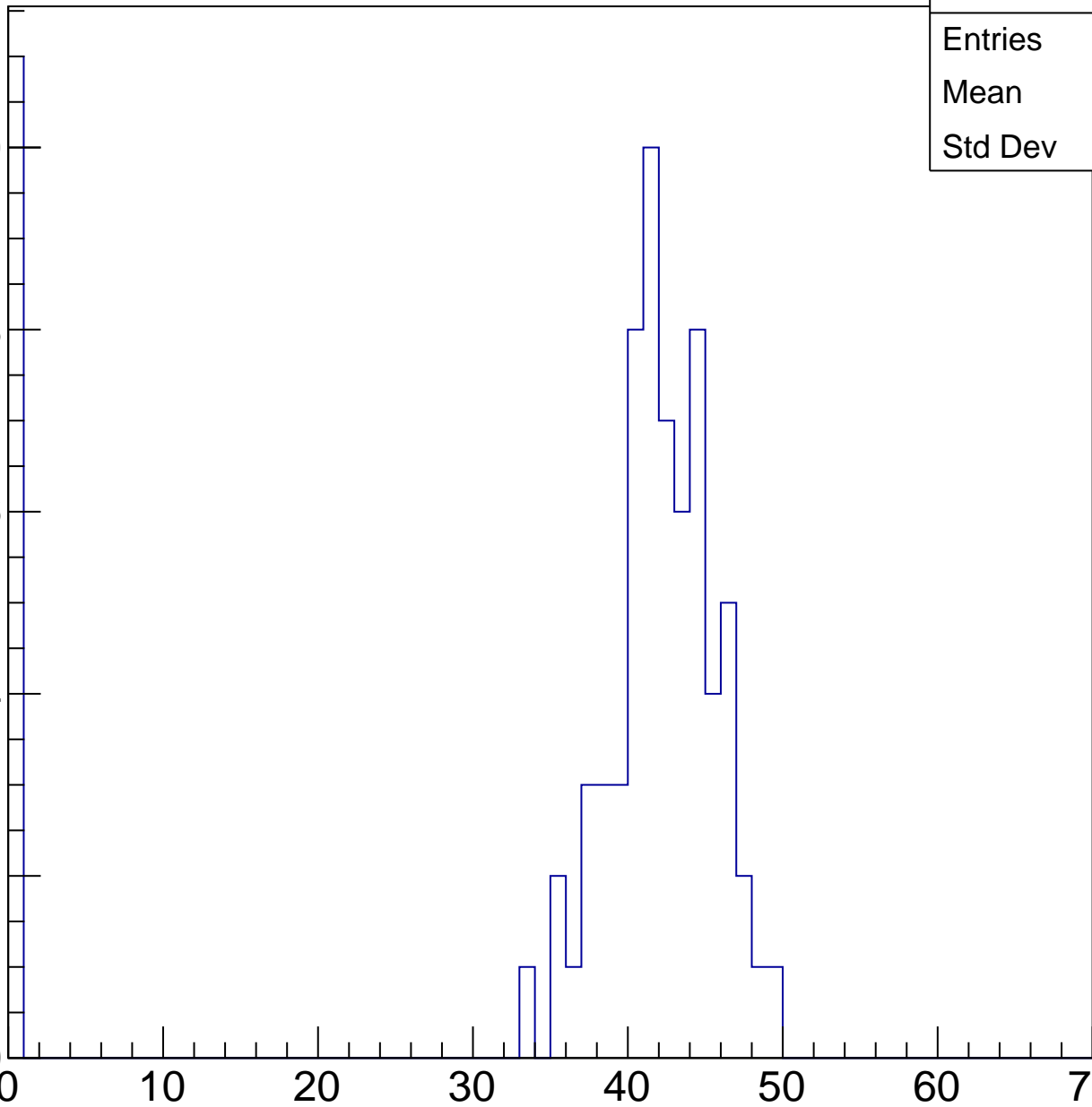
0

Entries 76

Mean 35.74

Std Dev 15.01

ampl

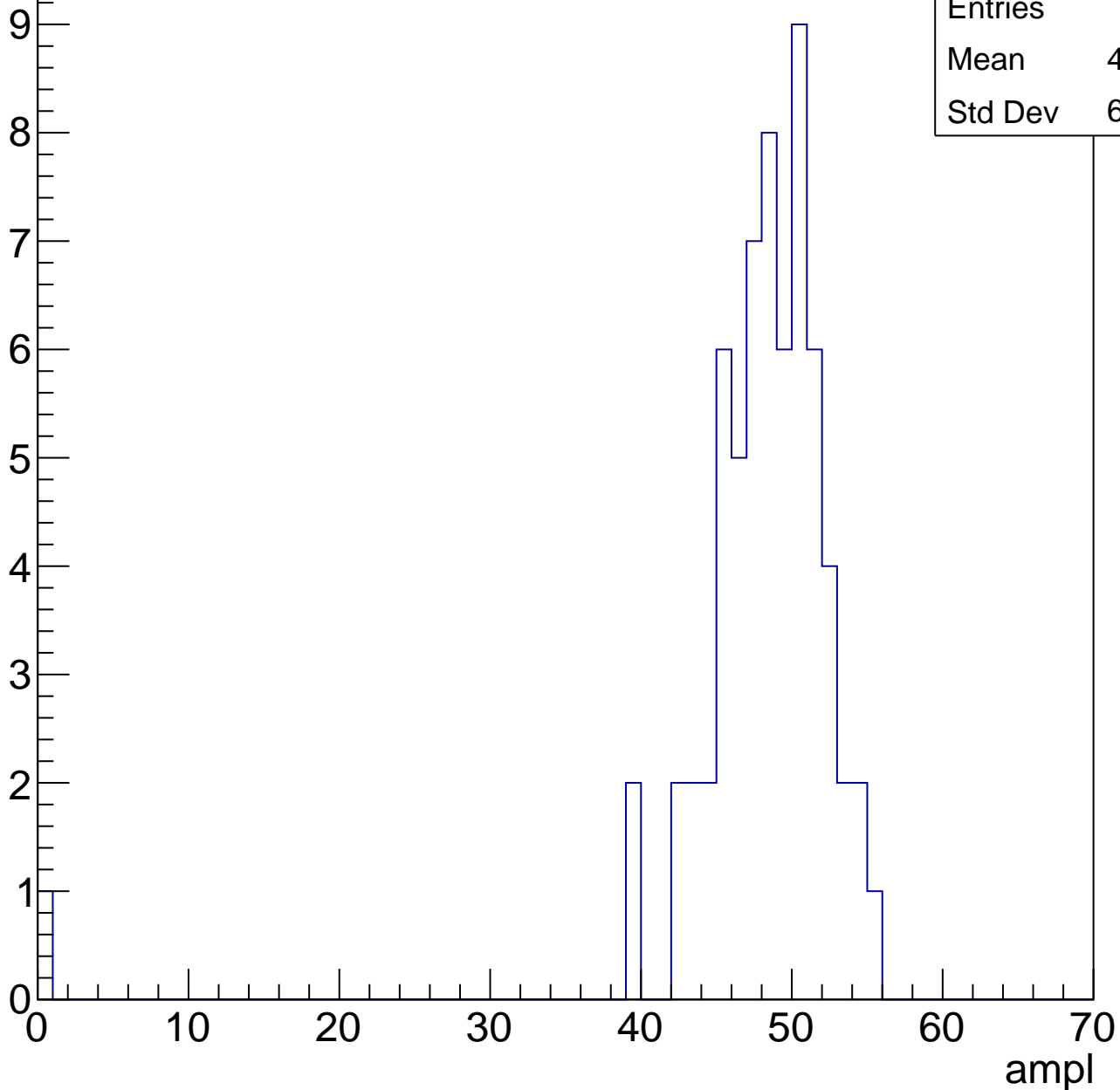


B1L103S, U12-ch94, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	47.32
Std Dev	6.796

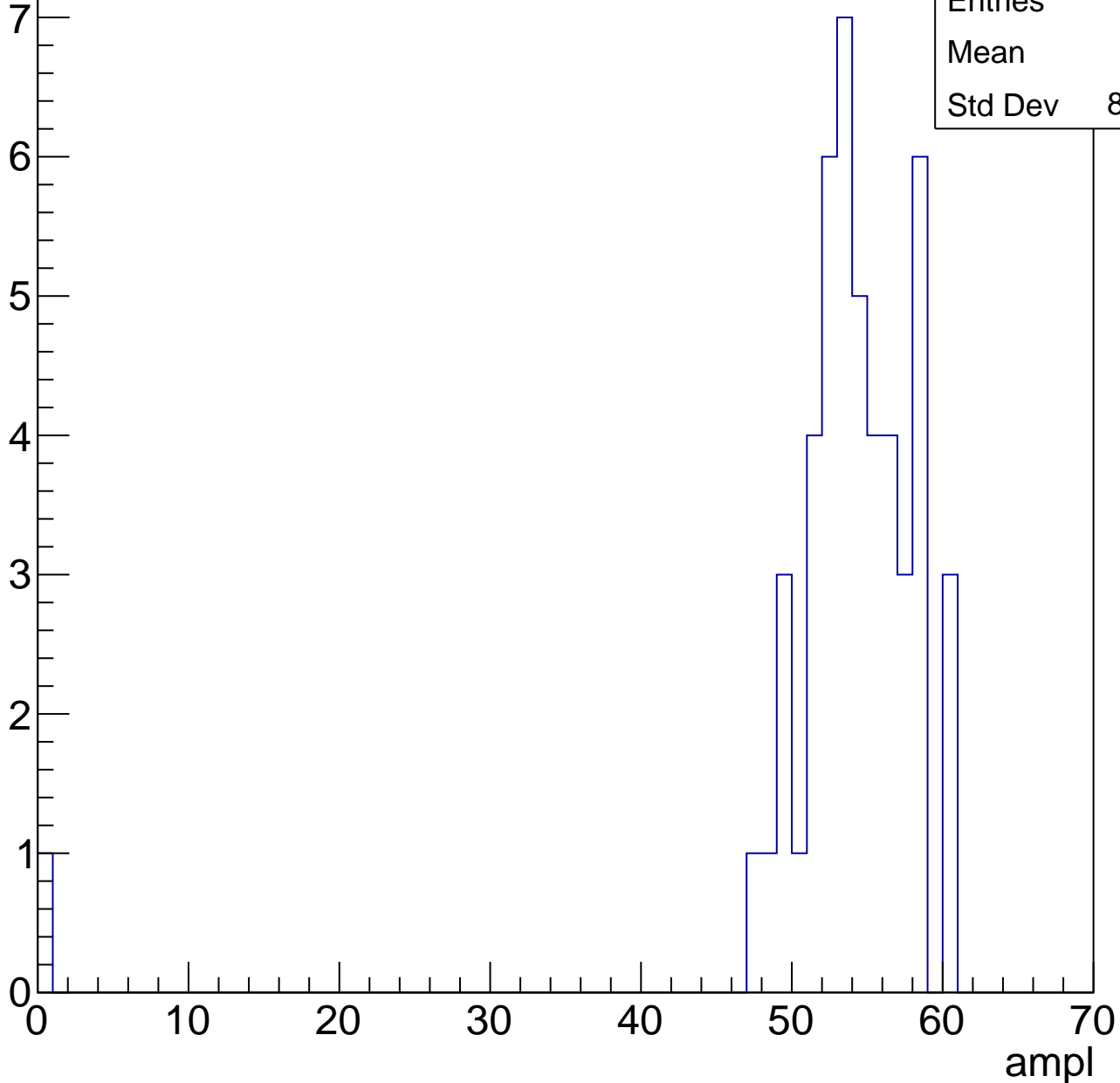


B1L103S, U12-ch94, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	49
Mean	52.9
Std Dev	8.269

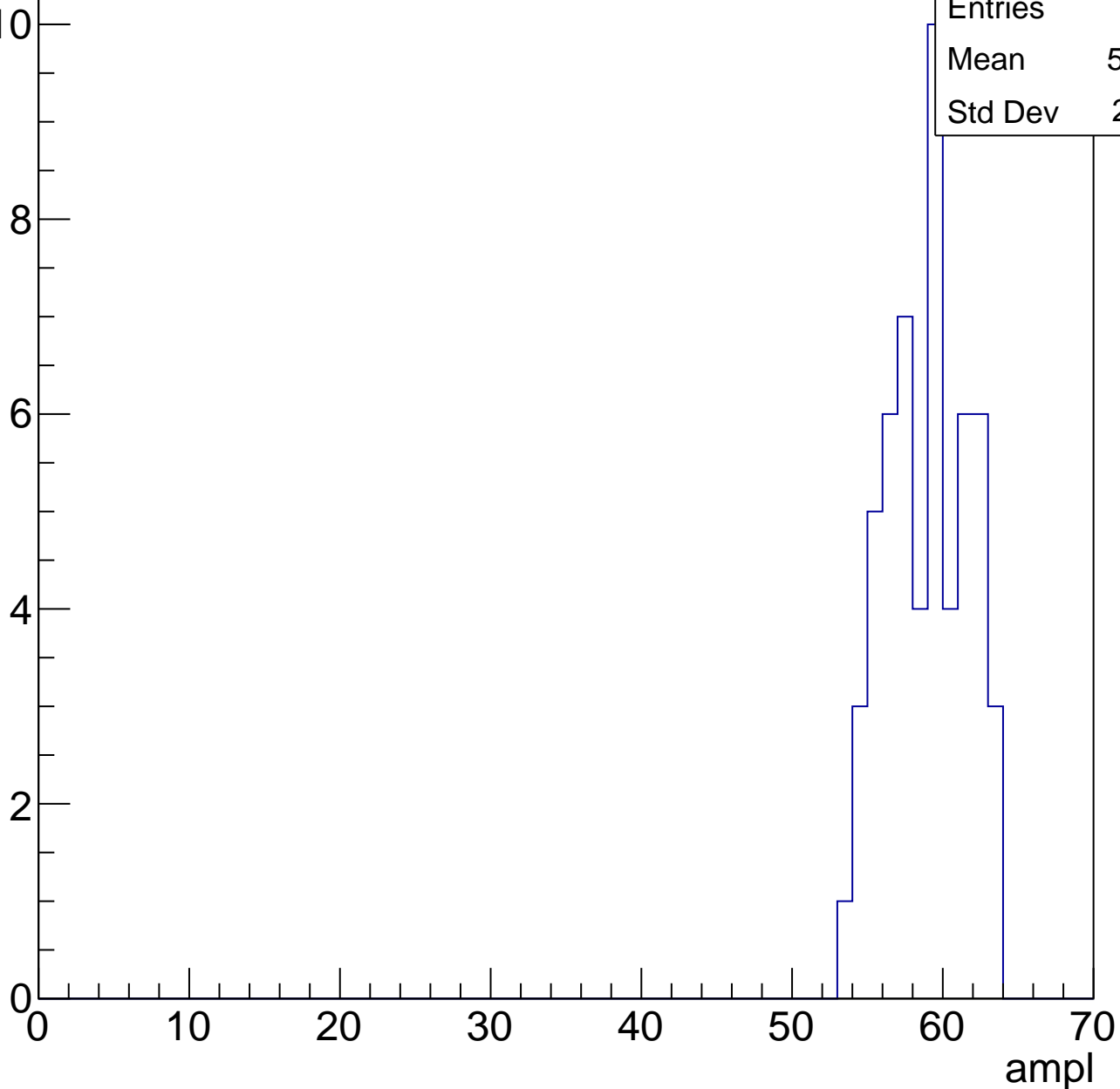


B1L103S, U12-ch94, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

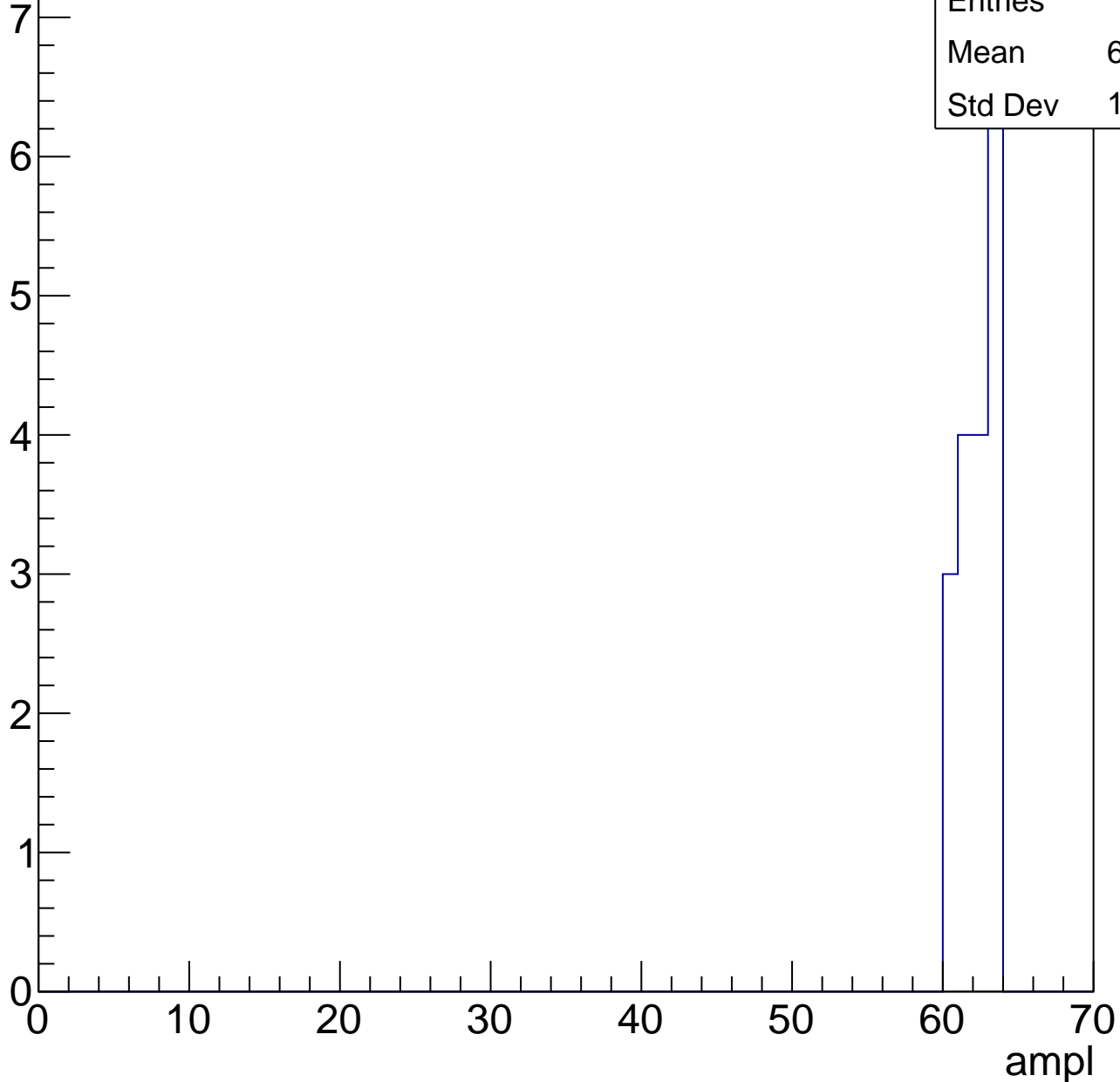
Entries	55
Mean	58.44
Std Dev	2.661



B1L103S, U12-ch94, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

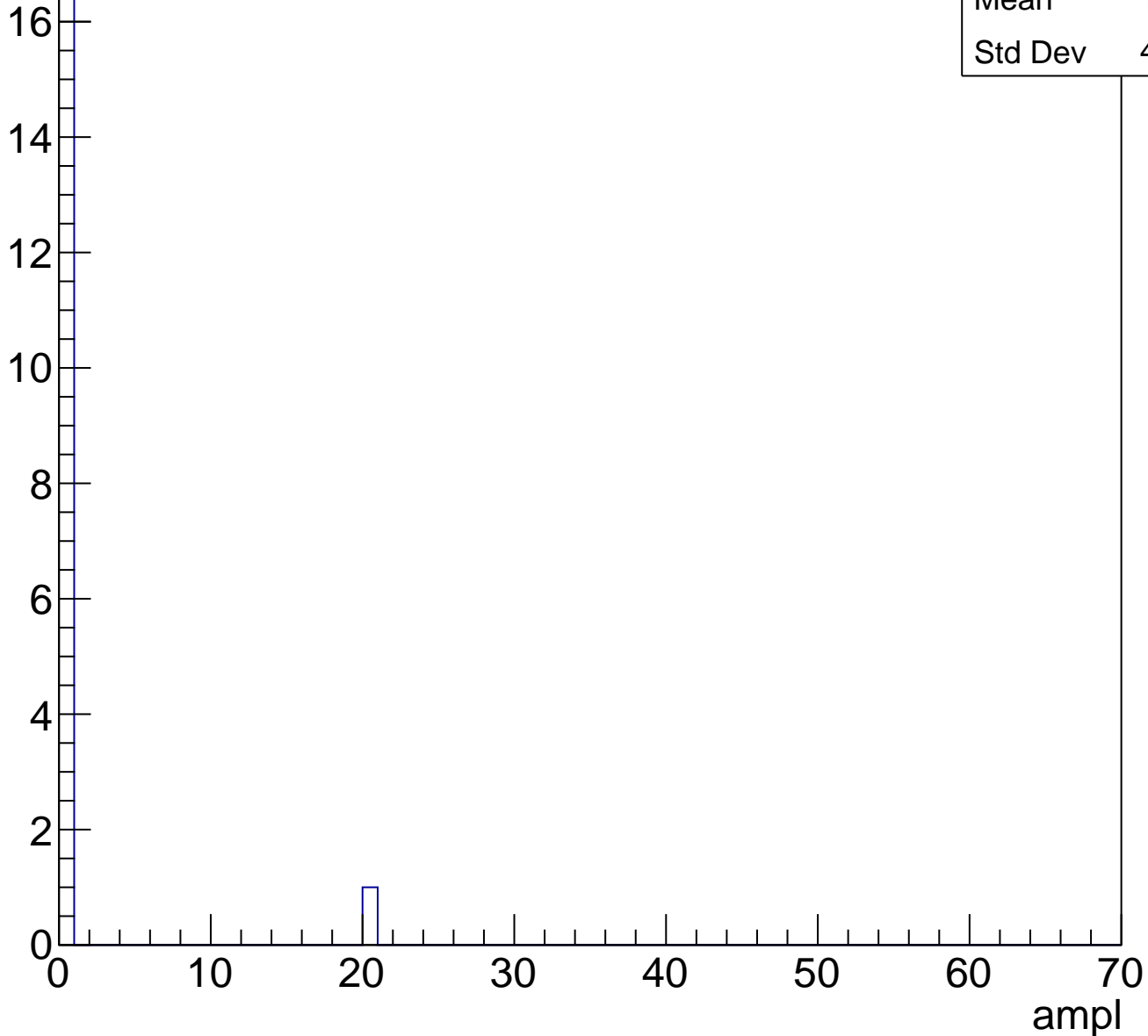


B1L103S, U12-ch94, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	18
Mean	1.111
Std Dev	4.581

Entry

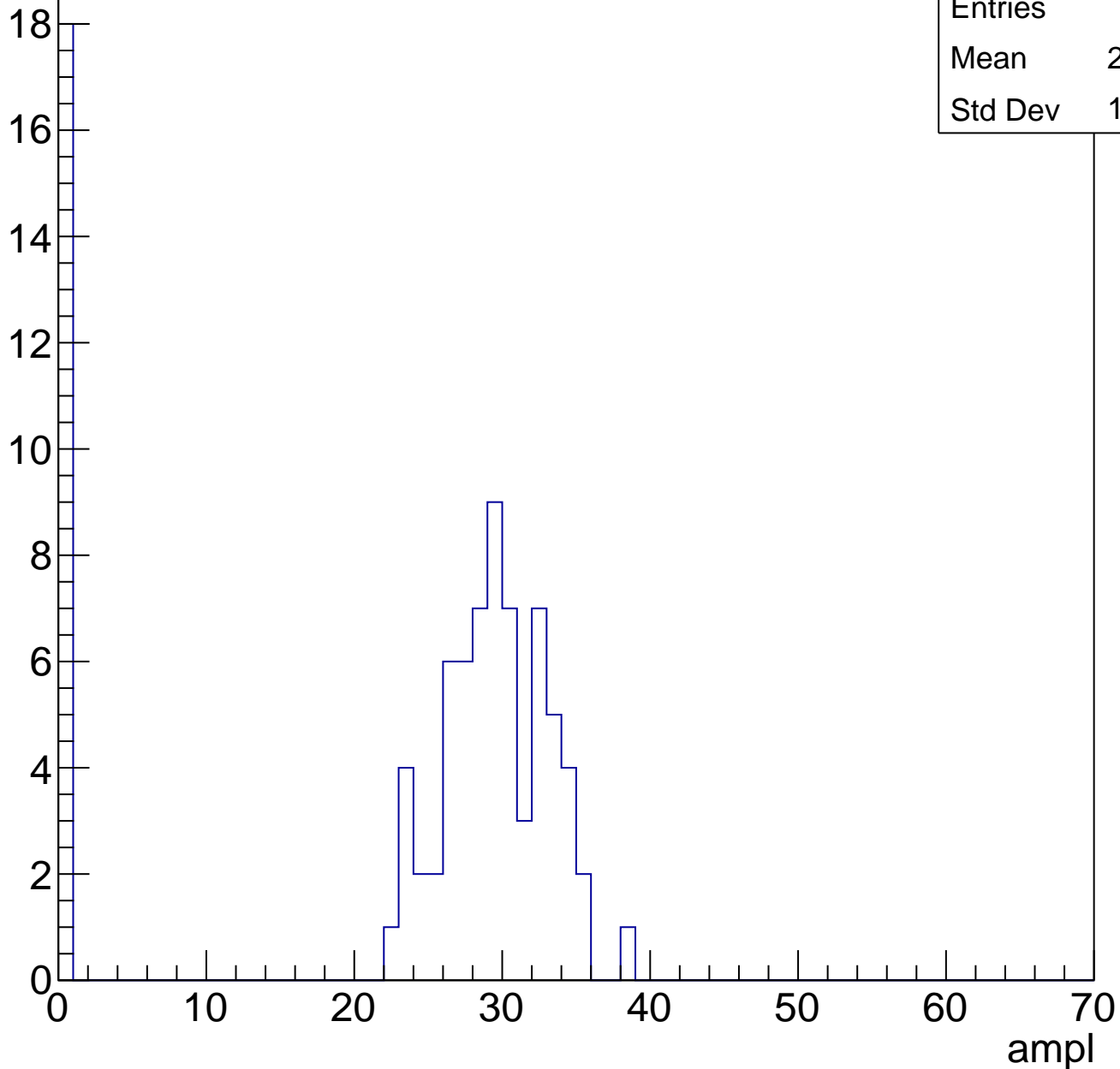


B1L103S, U12-ch95, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	84
Mean	22.89
Std Dev	12.33

Entry

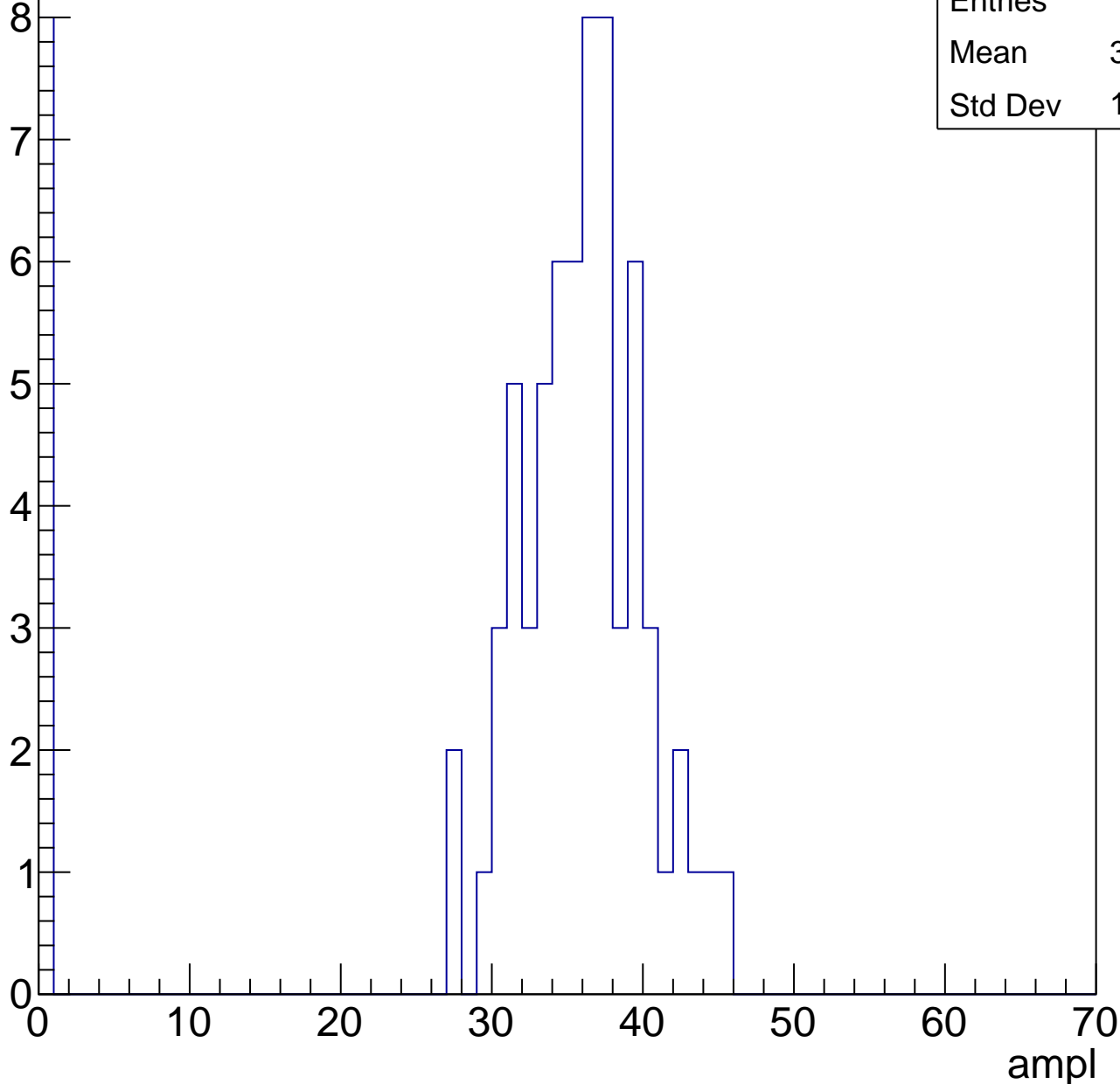


B1L103S, U12-ch95, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

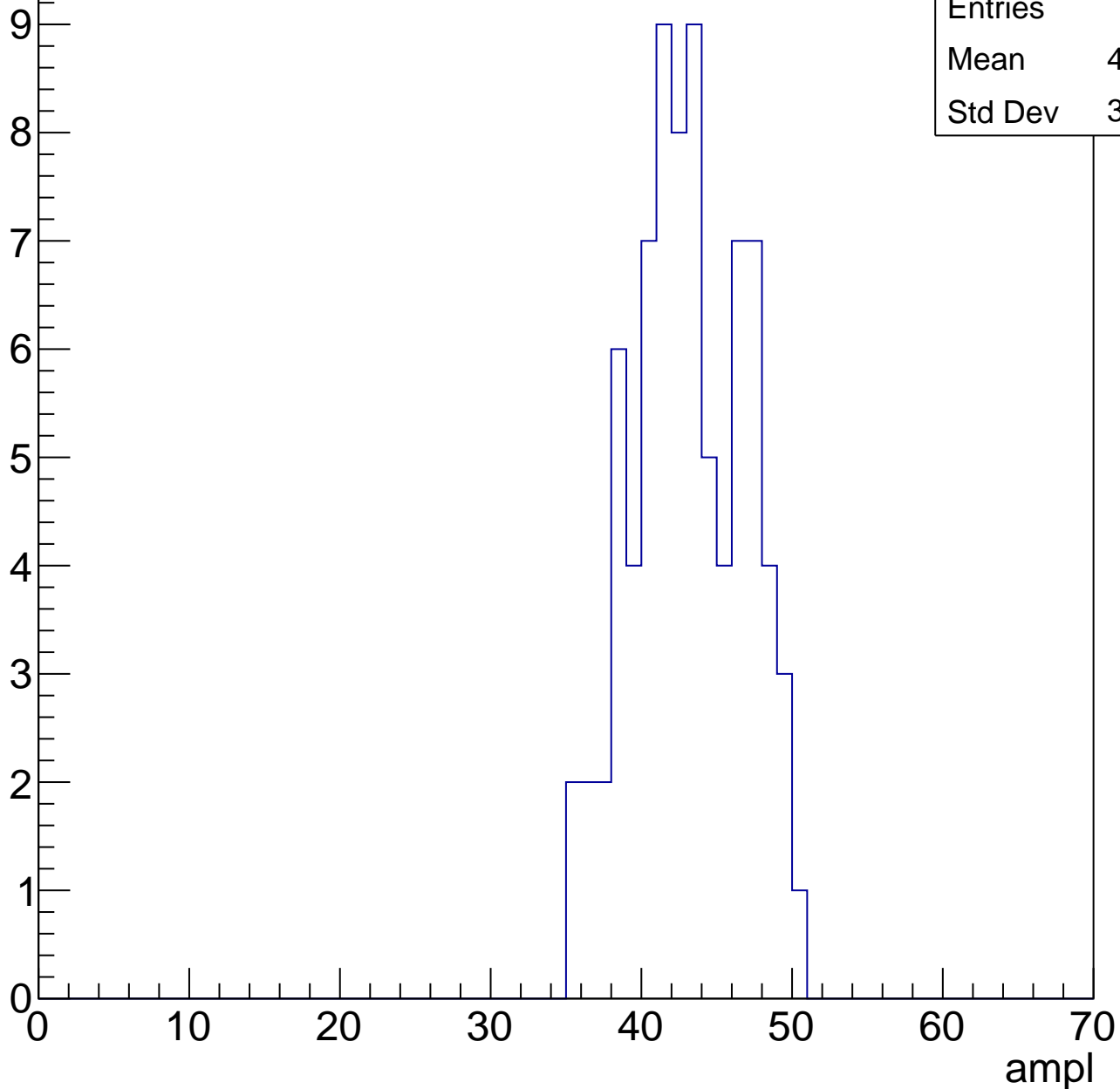
Entries	73
Mean	31.67
Std Dev	11.69



B1L103S, U12-ch95, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

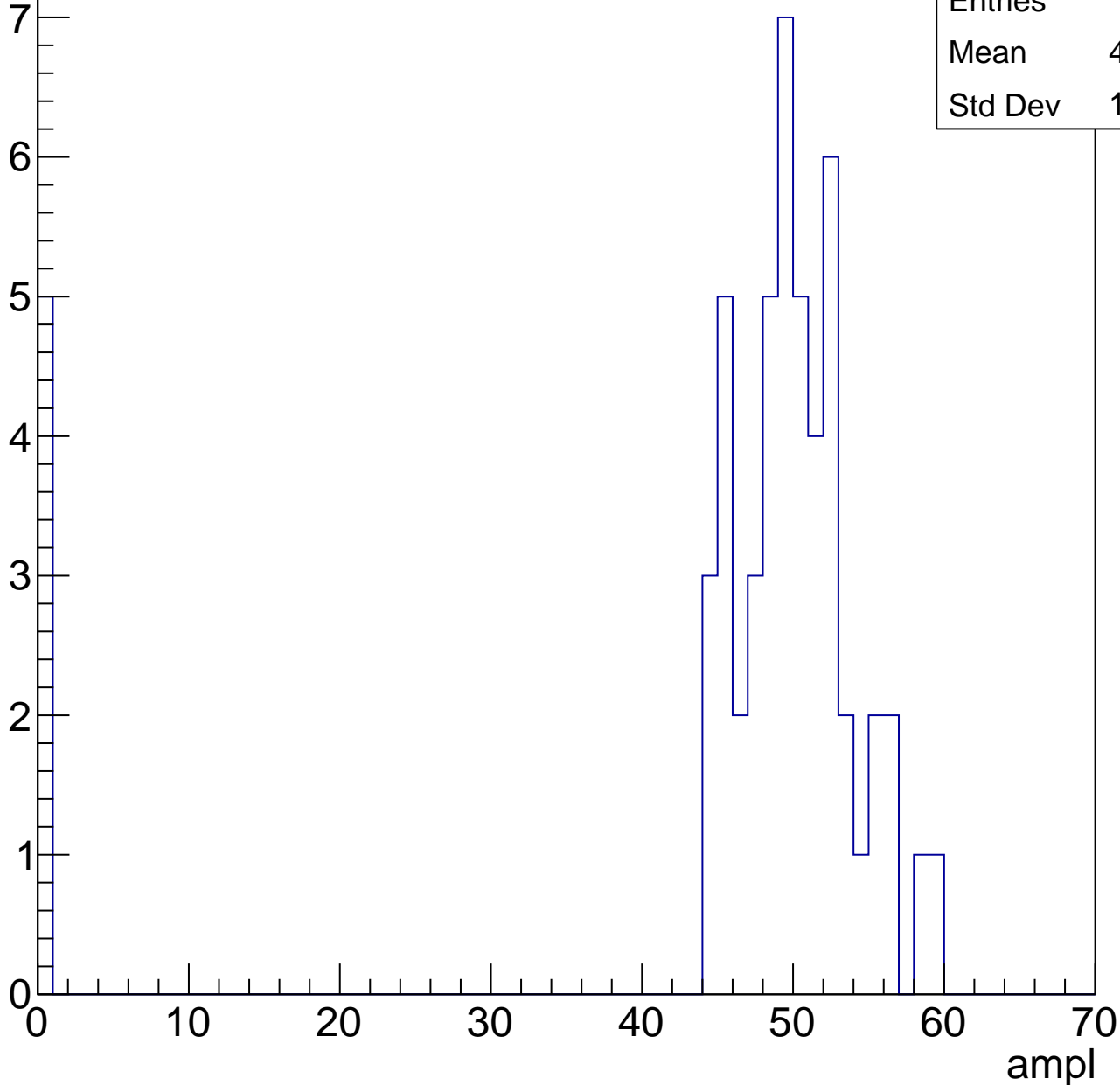


B1L103S, U12-ch95, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	54
Mean	45.15
Std Dev	14.83

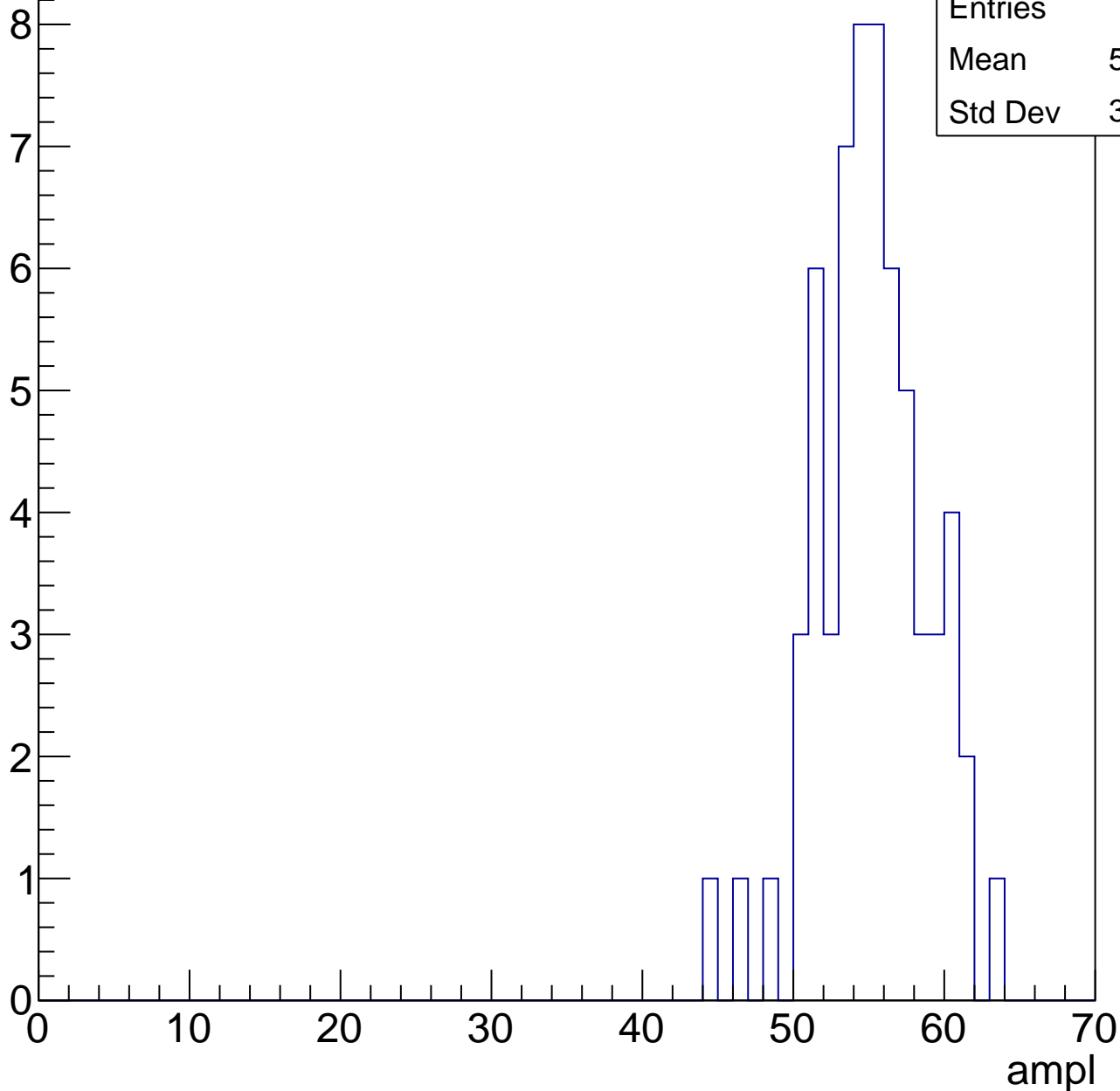


B1L103S, U12-ch95, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

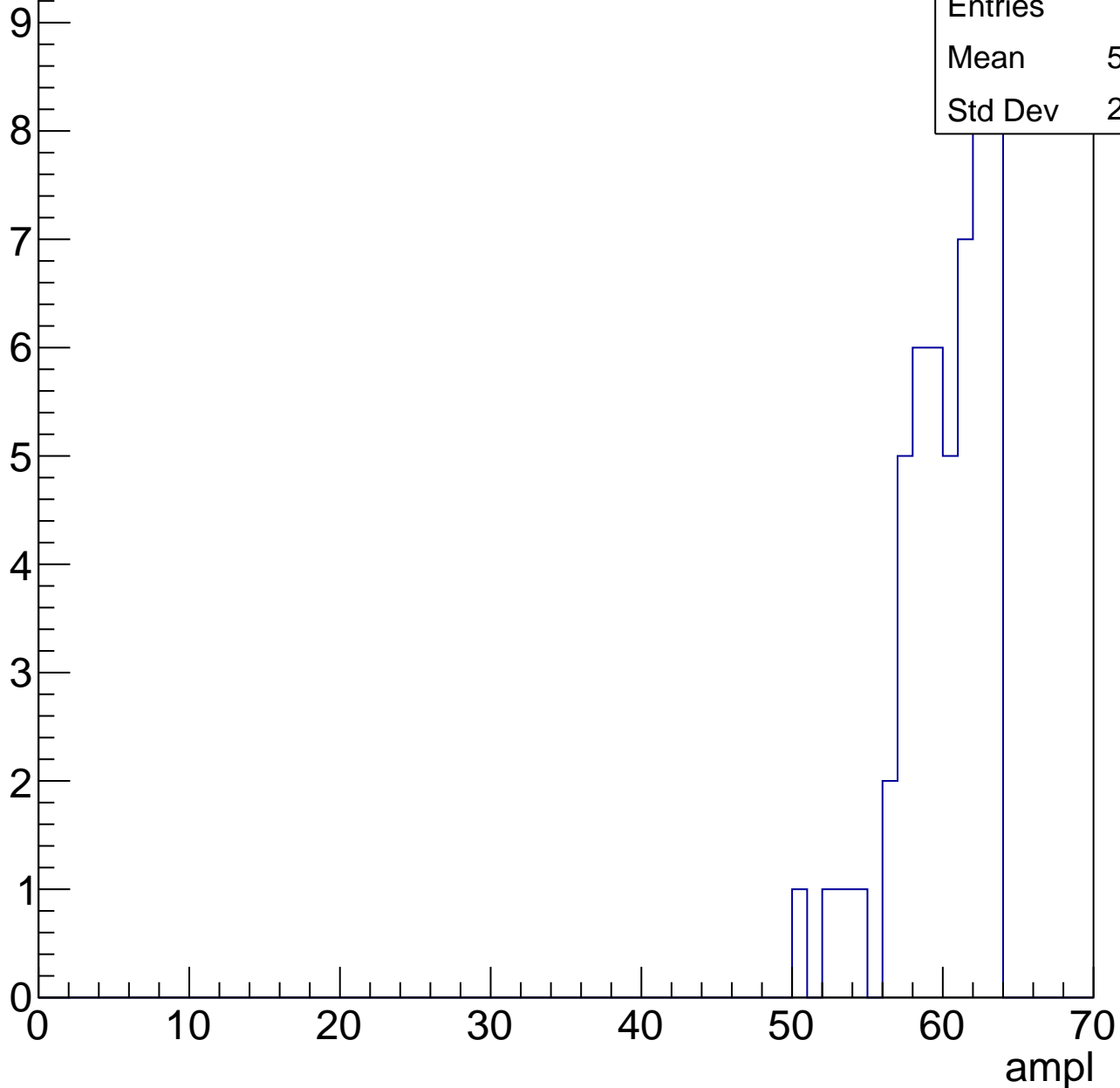
Entries	62
Mean	54.68
Std Dev	3.627



B1L103S, U12-ch95, adc5

calib_packv5_041523_1651.root, FC#0, port C2

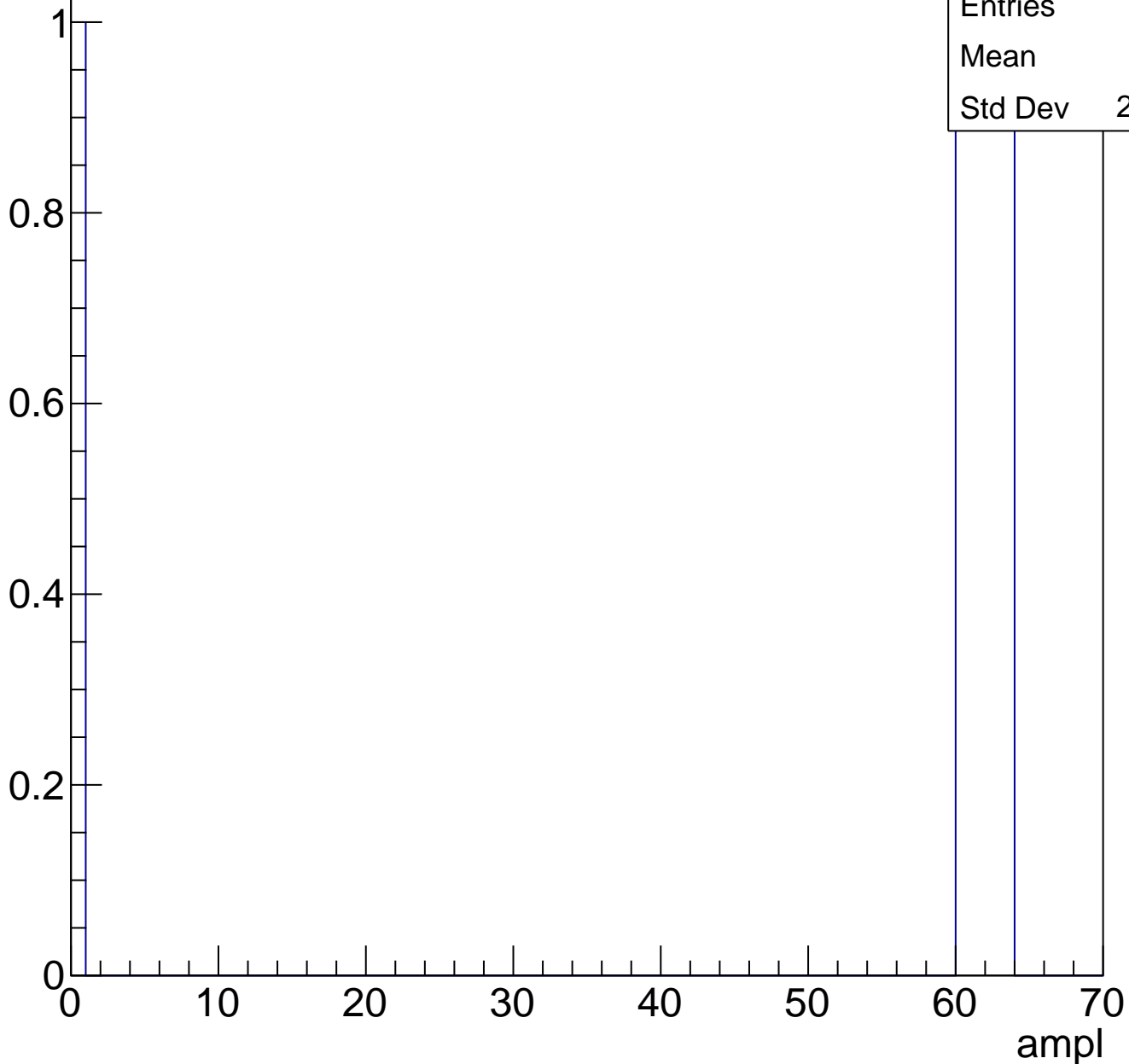
Entry



B1L103S, U12-ch95, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch95, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch96, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	69
Mean	23.58
Std Dev	10.75

Entry

10

8

6

4

2

0

0

10

20

30

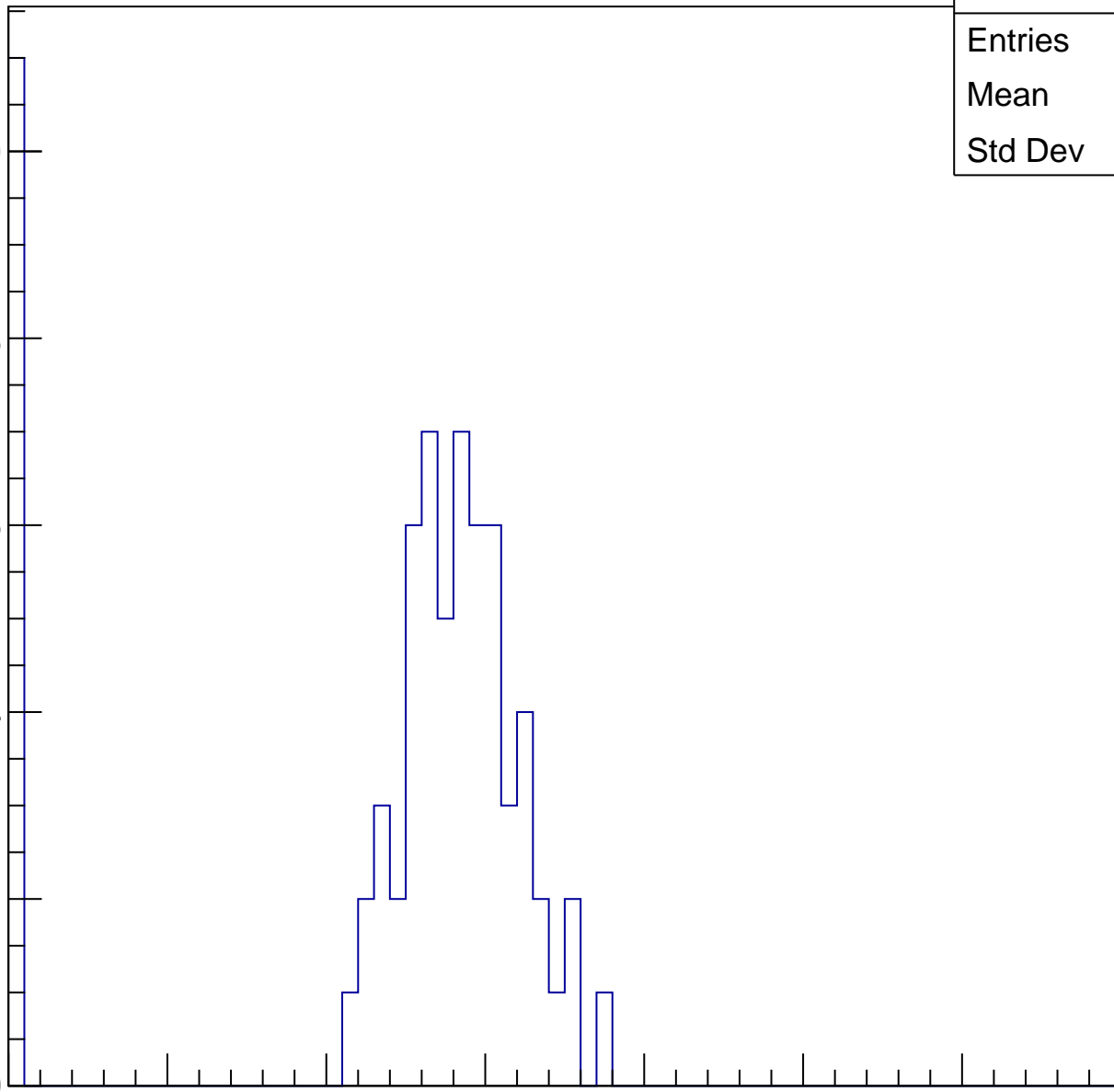
40

50

60

70

ampl

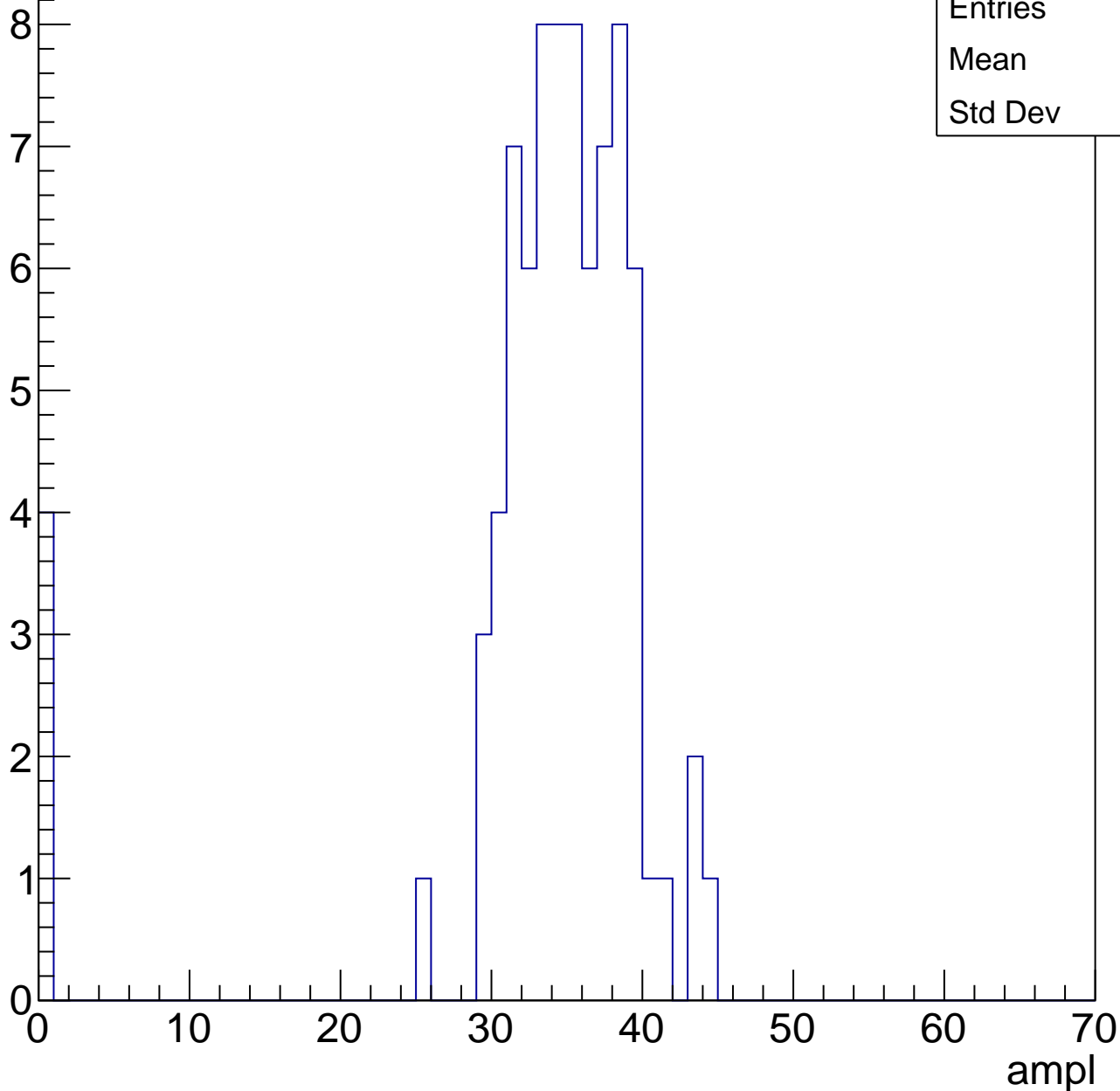


B1L103S, U12-ch96, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	81
Mean	33.1
Std Dev	8.31

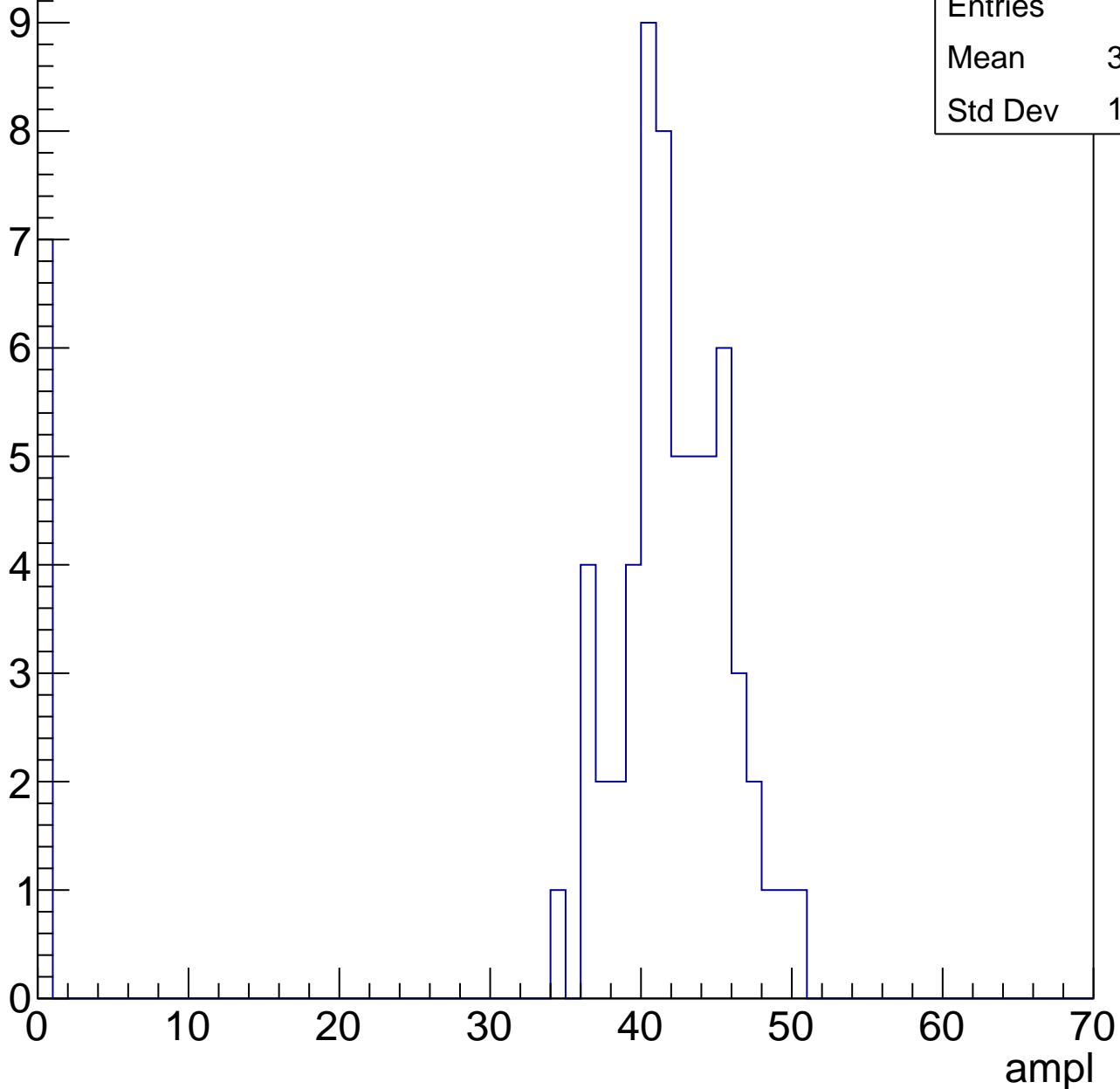


B1L103S, U12-ch96, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	37.36
Std Dev	13.27

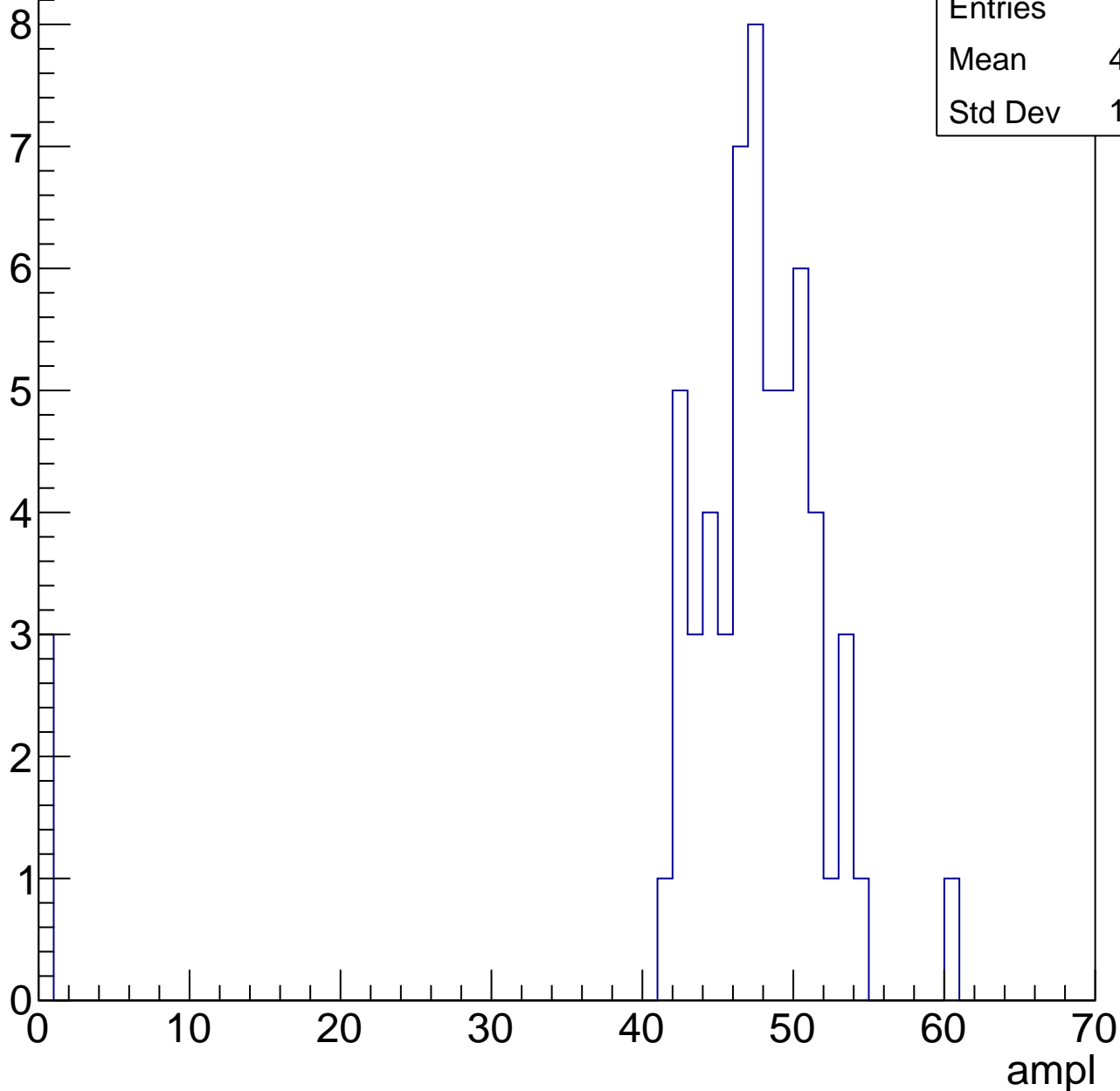


B1L103S, U12-ch96, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	45.05
Std Dev	10.92

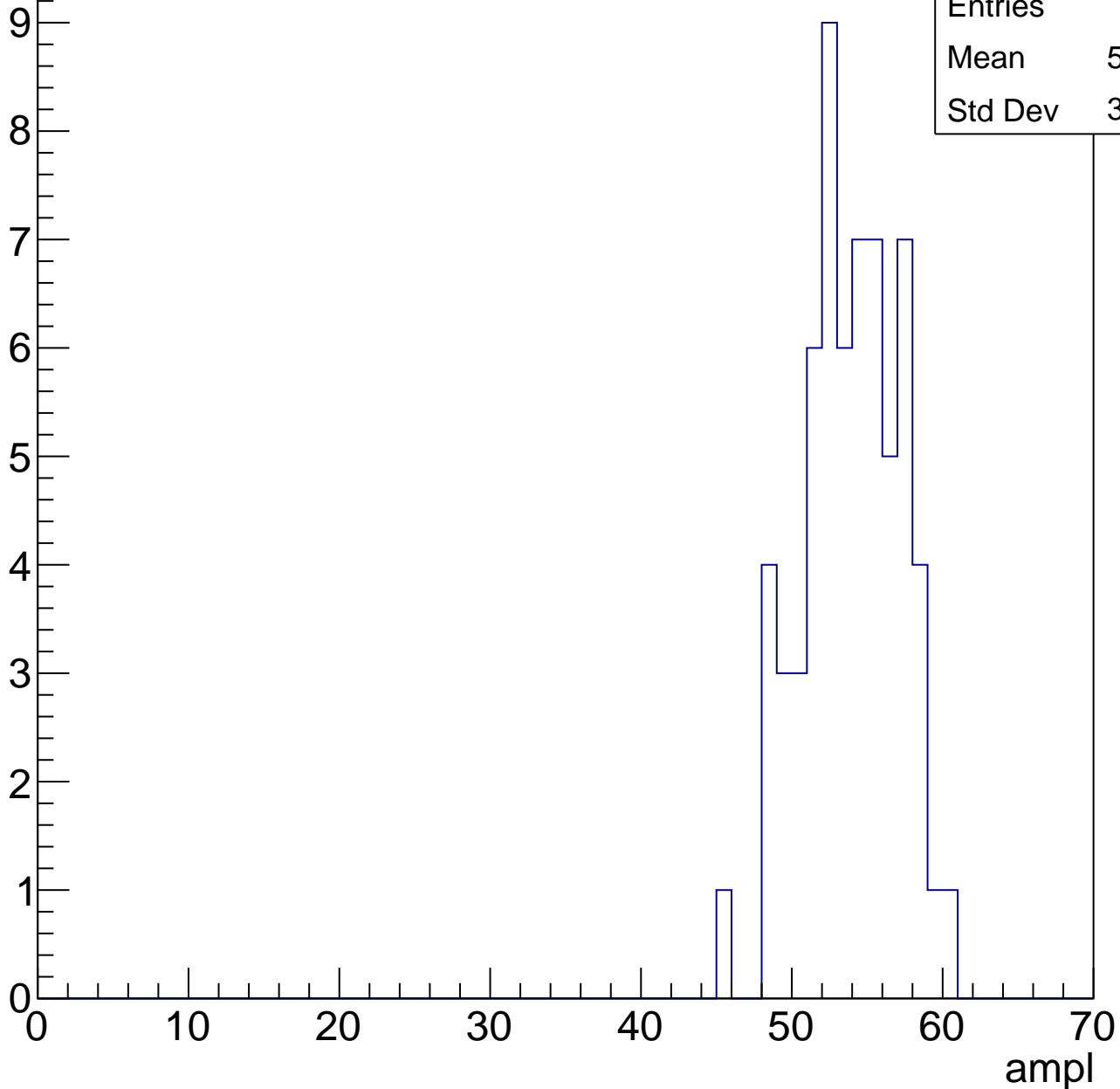


B1L103S, U12-ch96, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

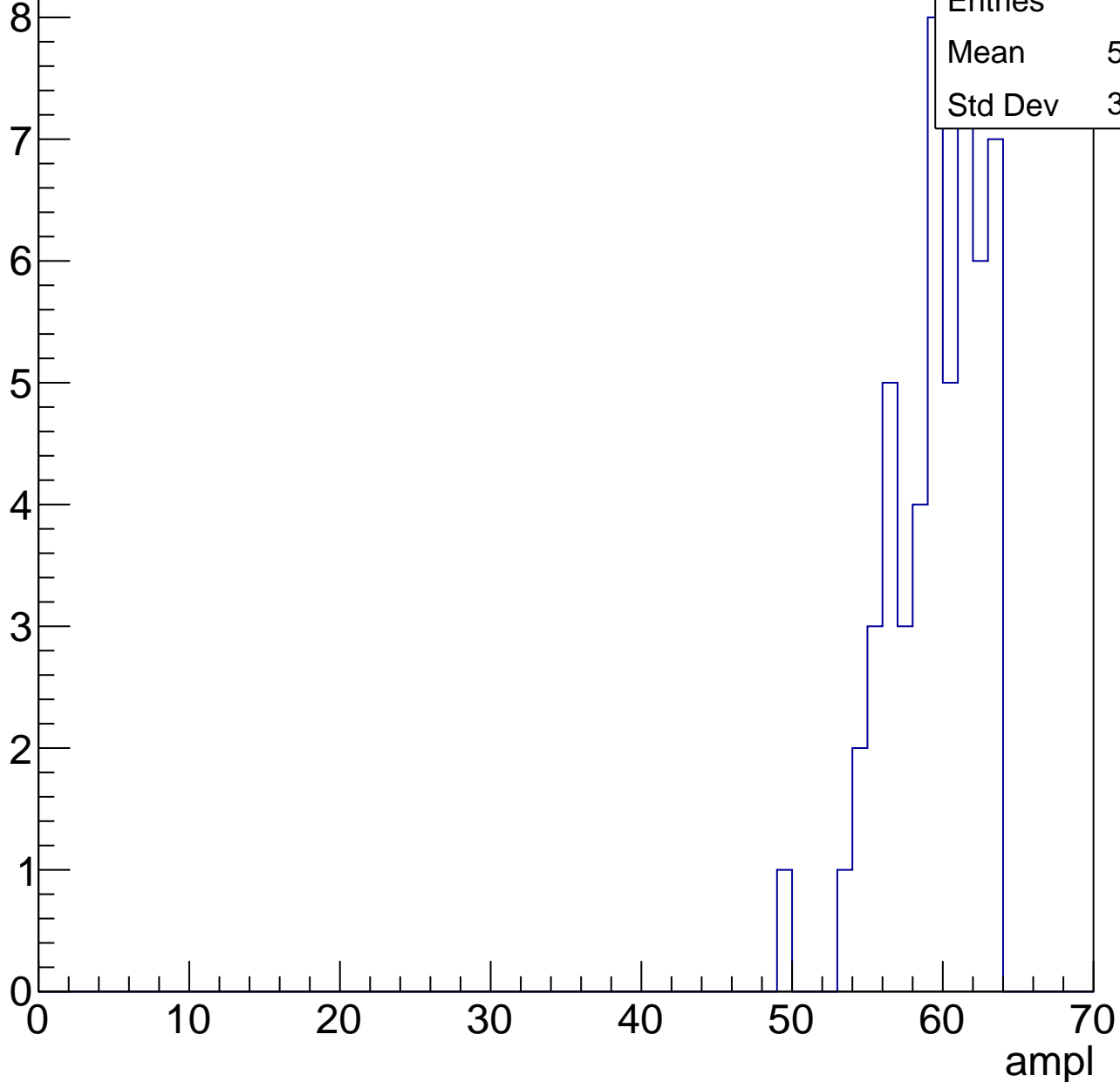
Entries	64
Mean	53.42
Std Dev	3.156



B1L103S, U12-ch96, adc5

calib_packv5_041523_1651.root, FC#0, port C2

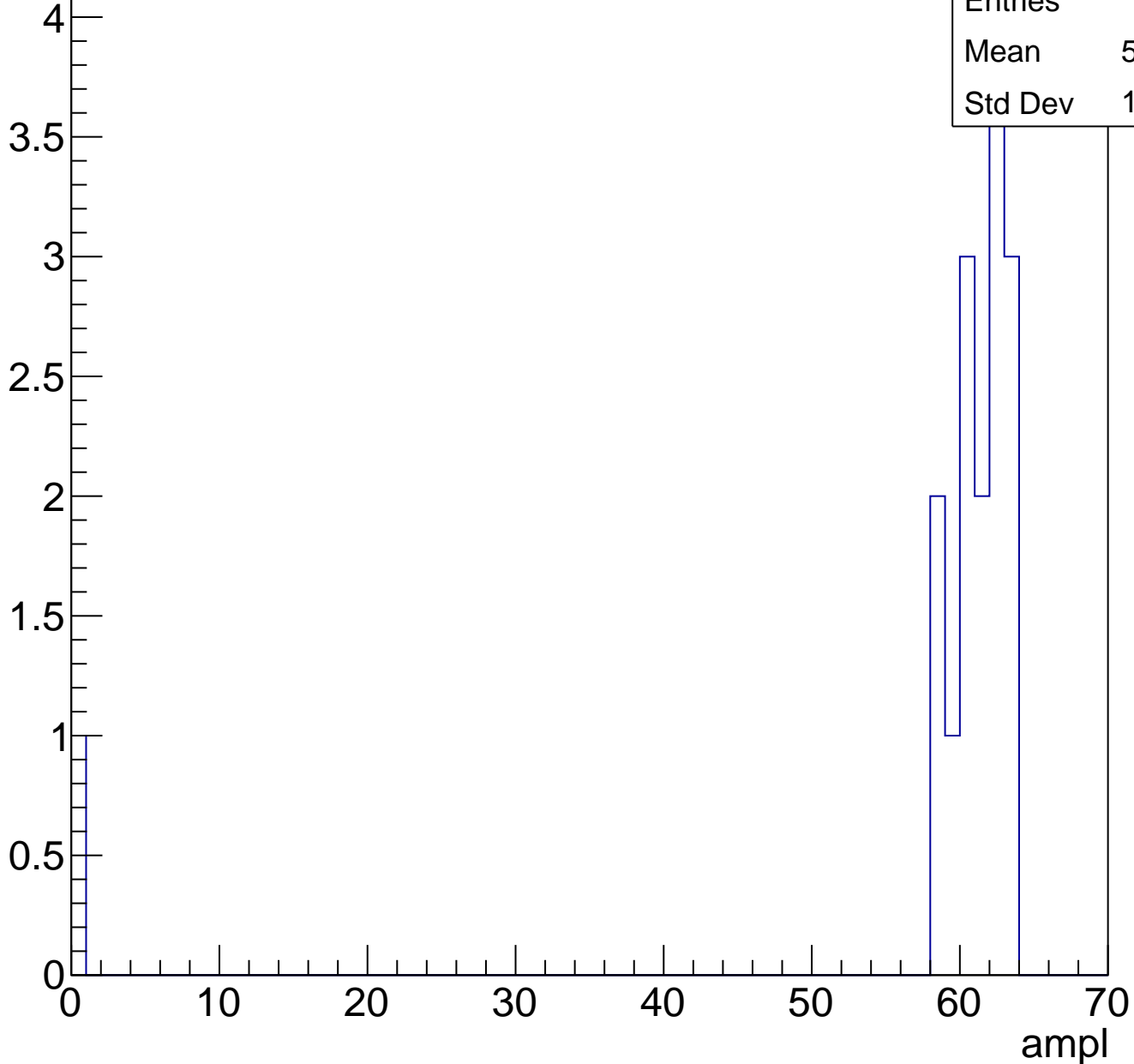
Entry



B1L103S, U12-ch96, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch96, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

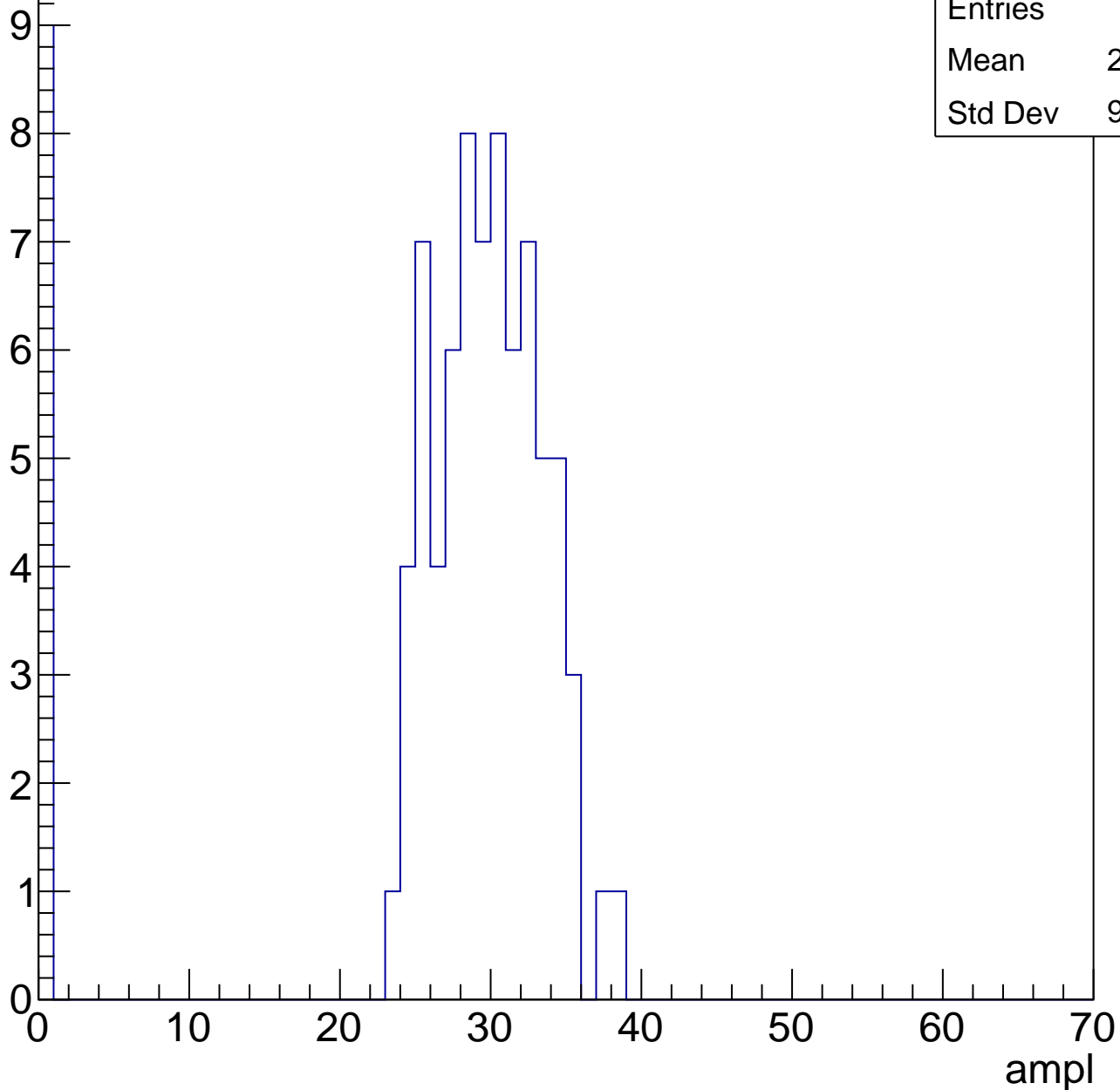
Entries	19
Mean	0
Std Dev	0

B1L103S, U12-ch97, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	82
Mean	26.24
Std Dev	9.762

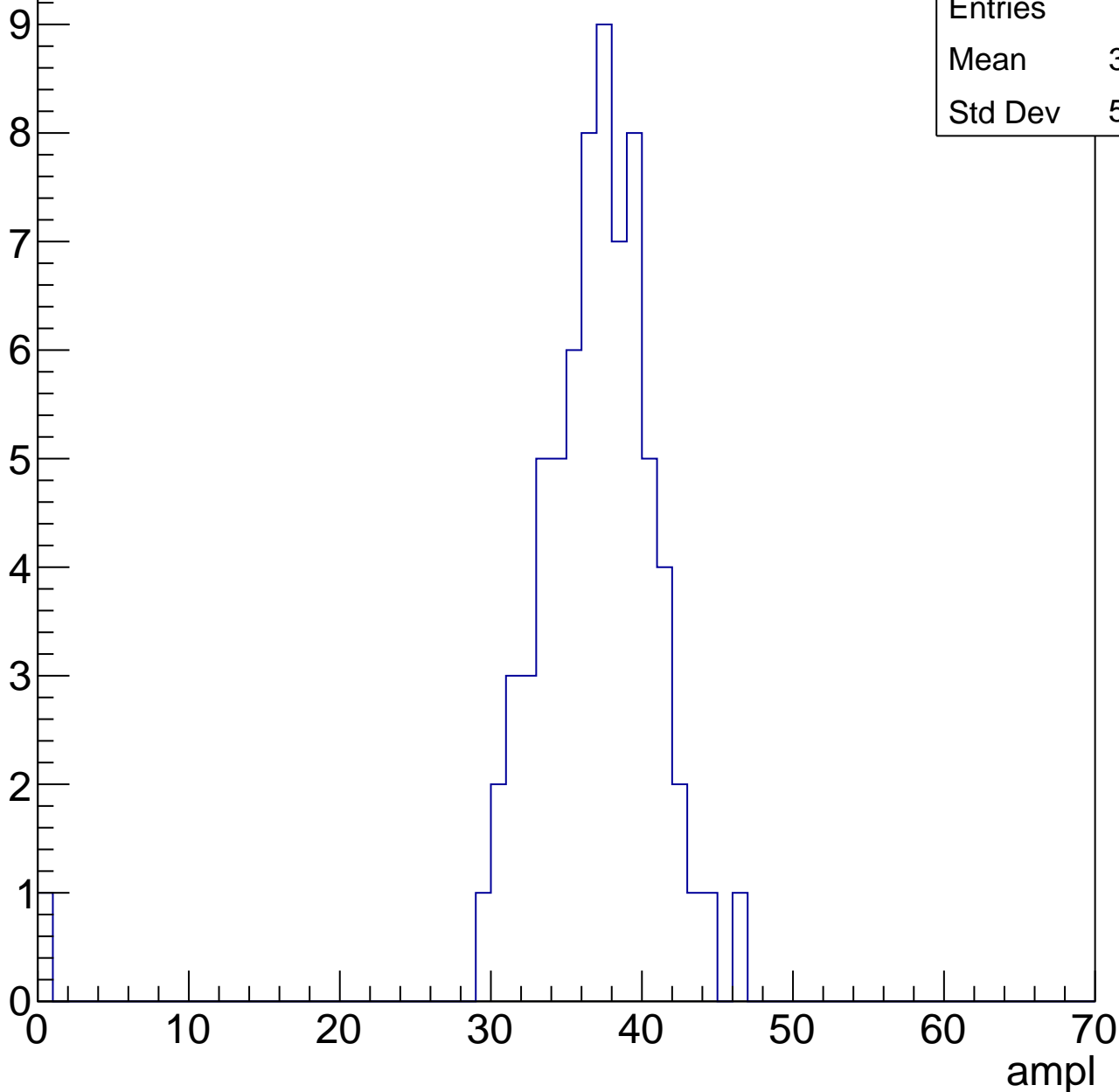


B1L103S, U12-ch97, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	72
Mean	36.15
Std Dev	5.507

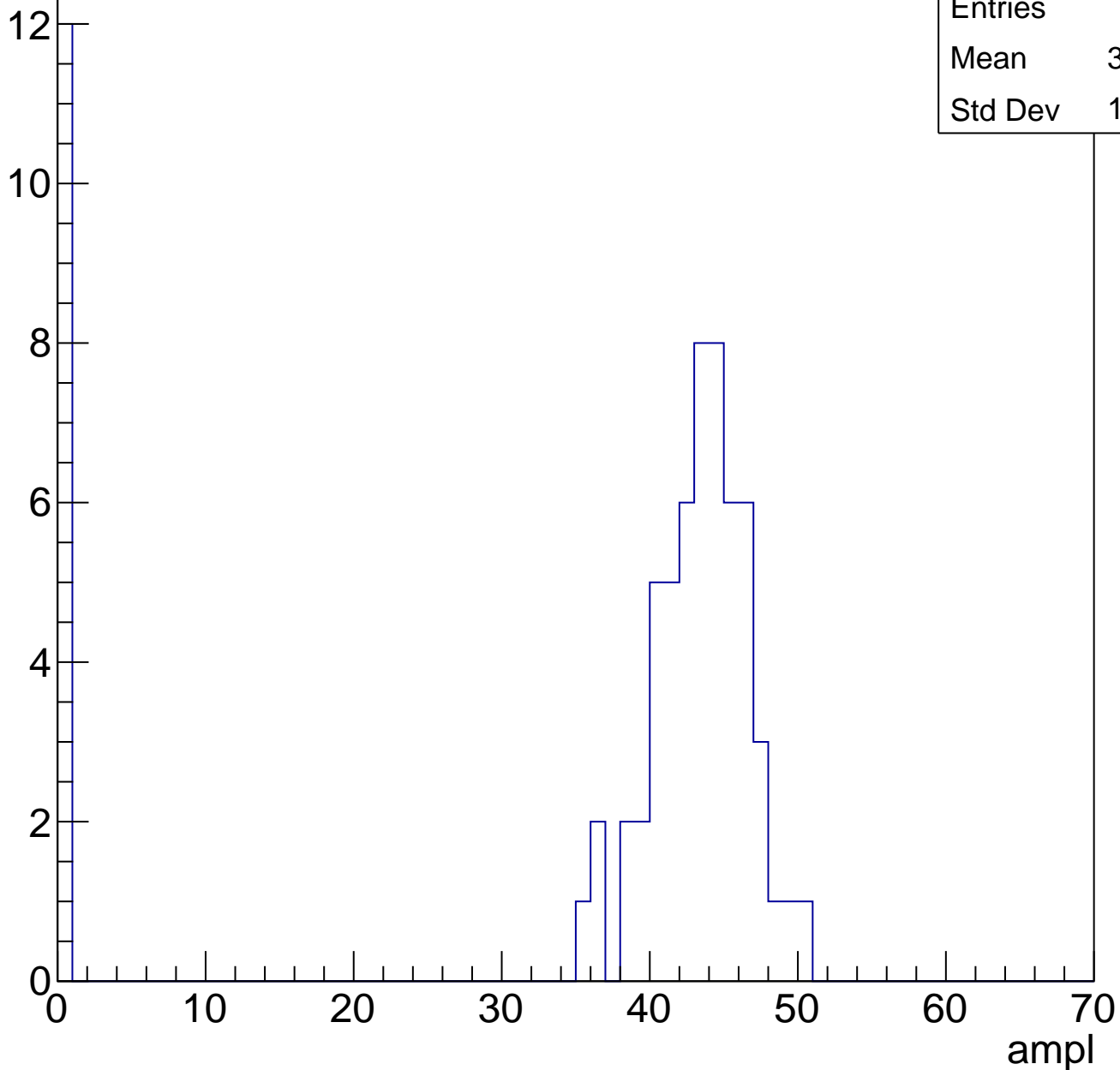


B1L103S, U12-ch97, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	69
Mean	35.48
Std Dev	16.53

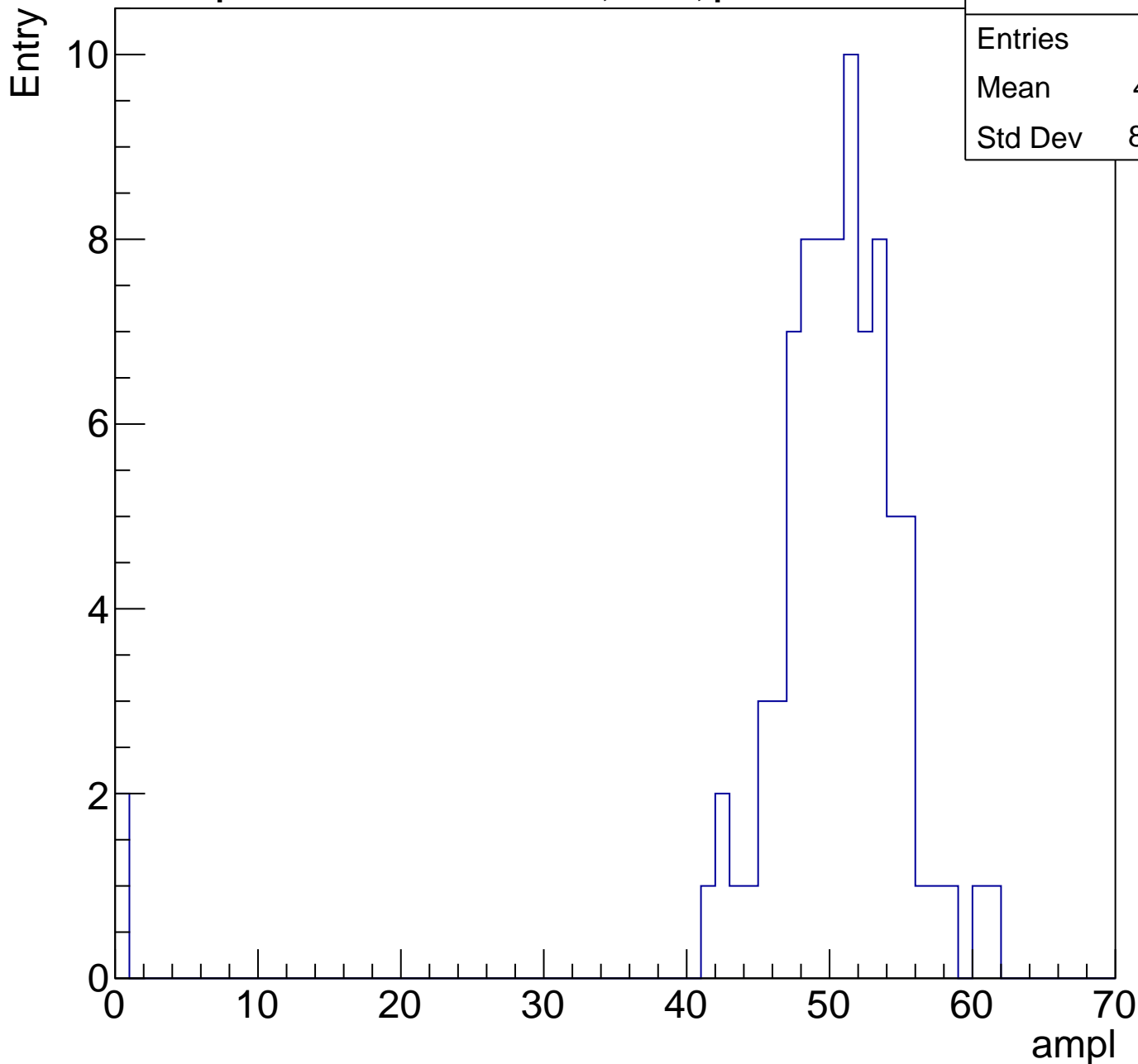
Entry



B1L103S, U12-ch97, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	84
Mean	49.11
Std Dev	8.548

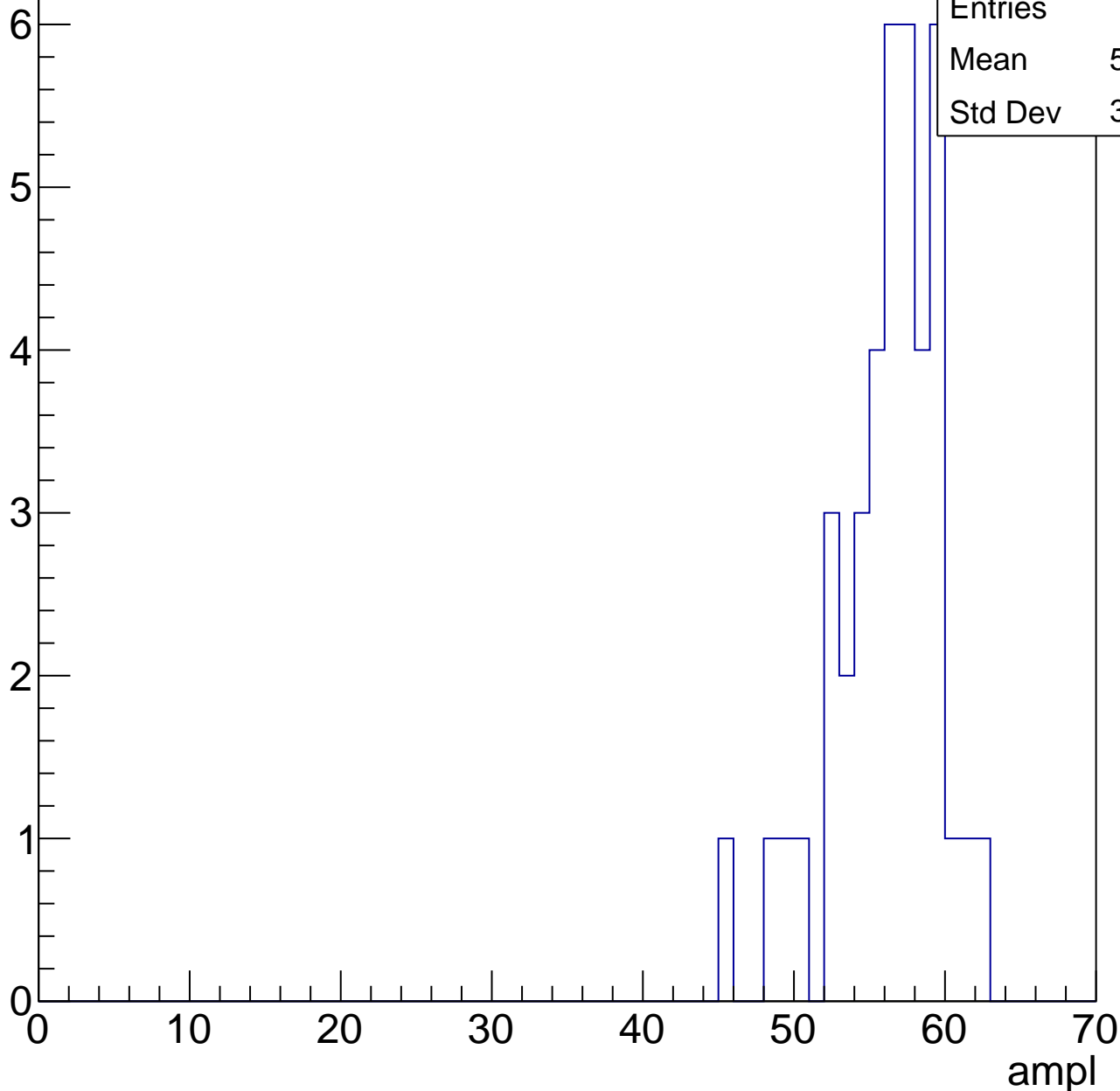


B1L103S, U12-ch97, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

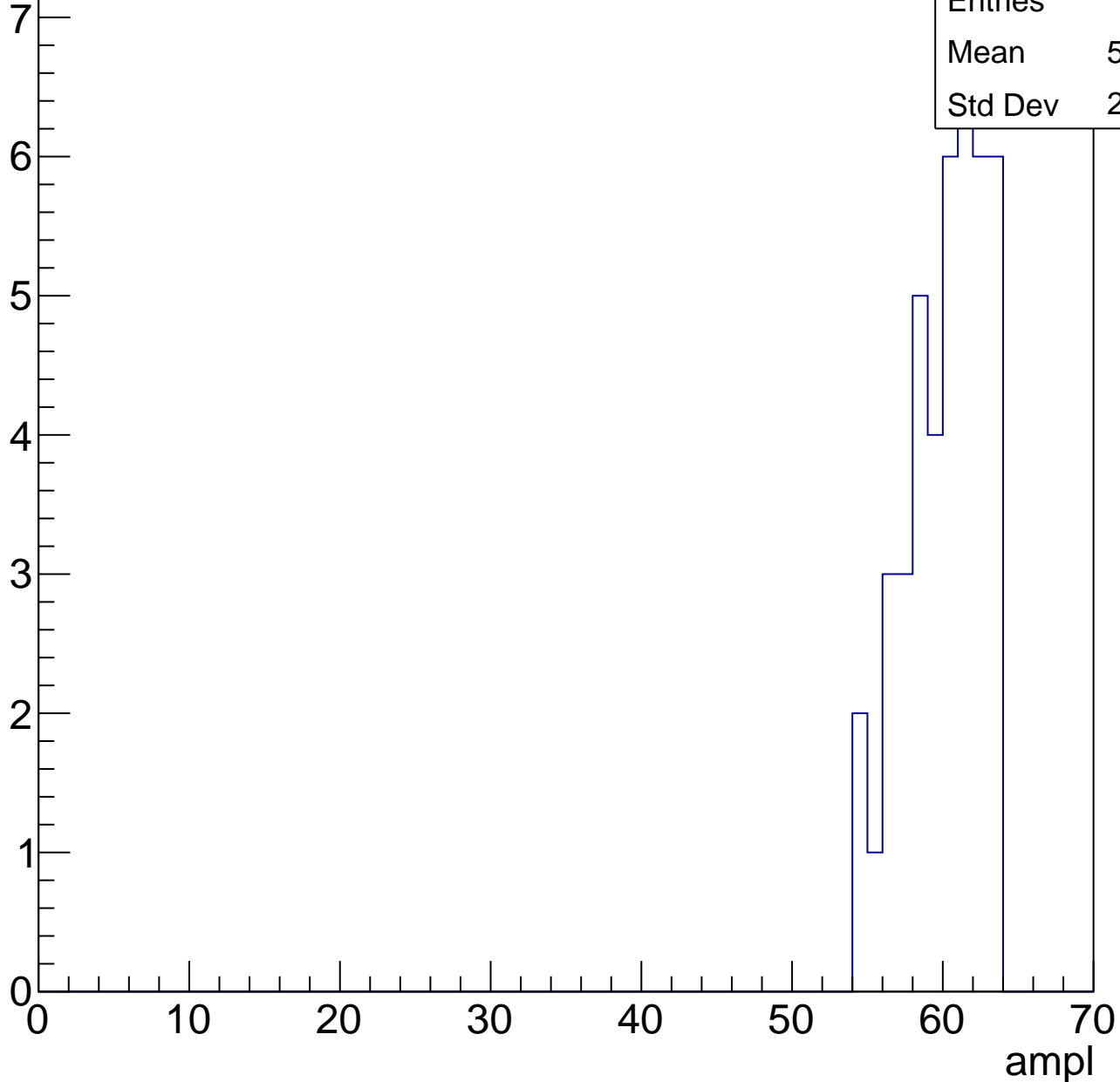
Entries	41
Mean	55.68
Std Dev	3.495



B1L103S, U12-ch97, adc5

calib_packv5_041523_1651.root, FC#0, port C2

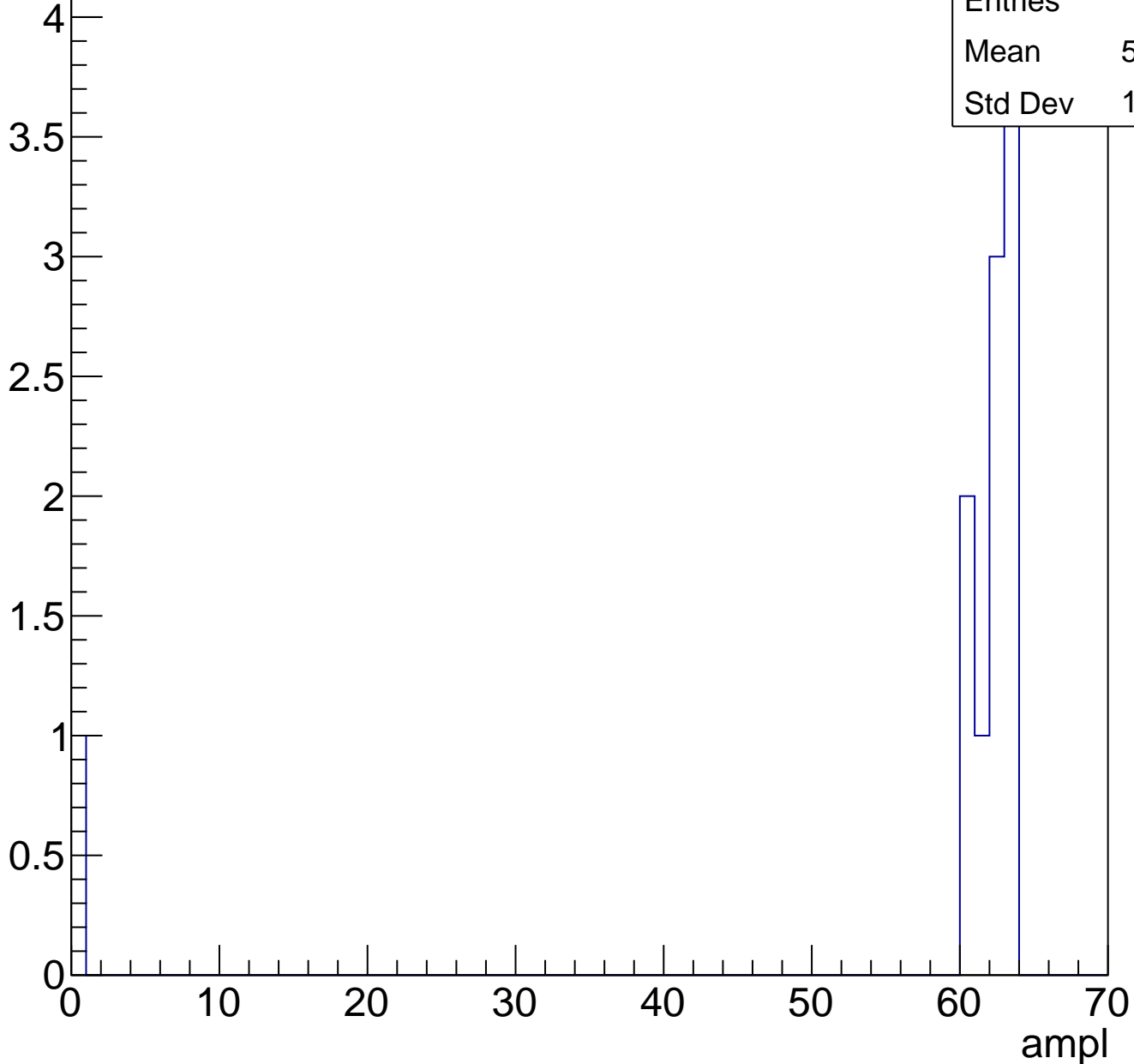
Entry



B1L103S, U12-ch97, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch97, adc7

calib_packv5_041523_1651.root, FC#0, port C2

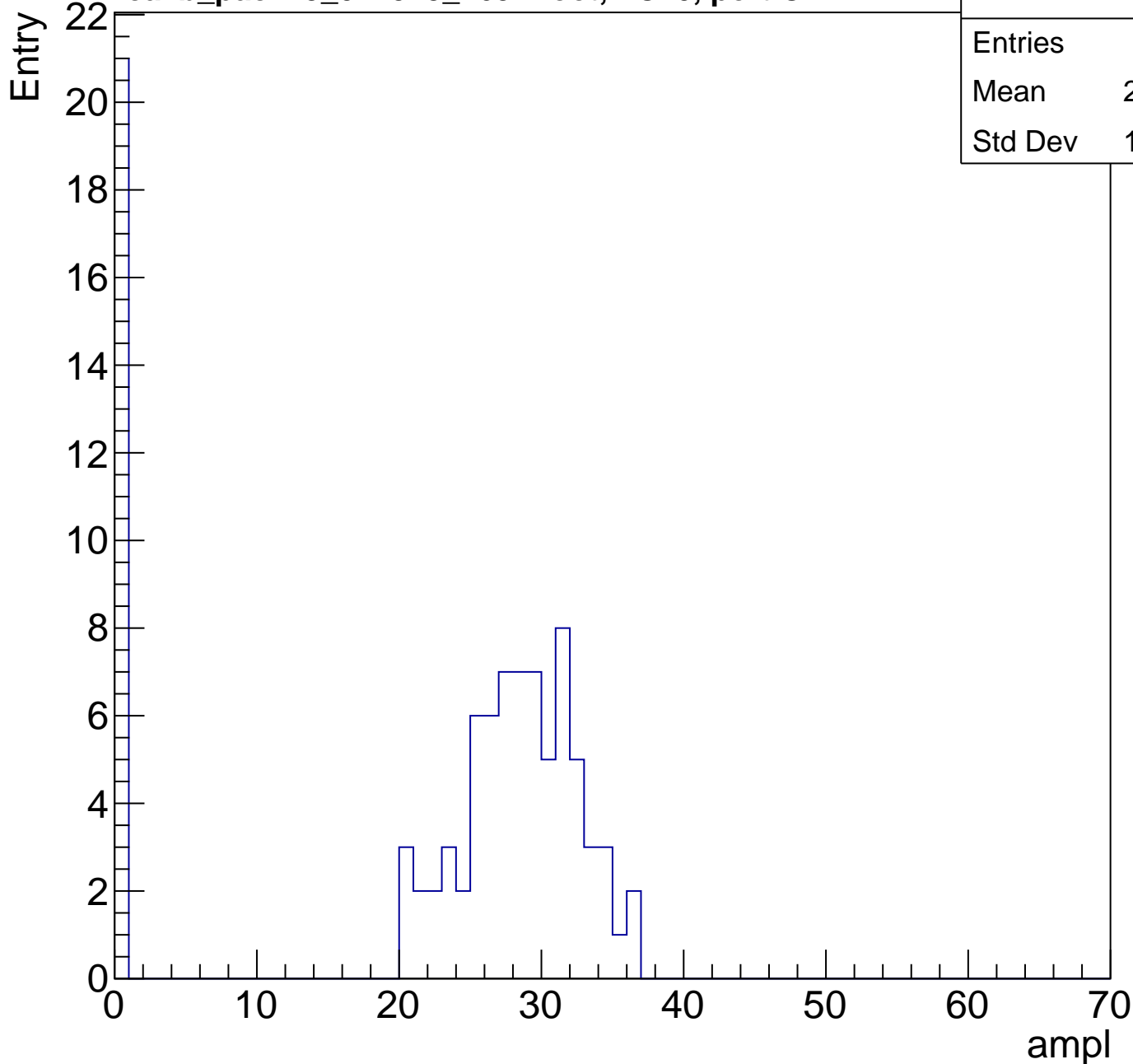
Entry



B1L103S, U12-ch98, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	93
Mean	21.75
Std Dev	12.24

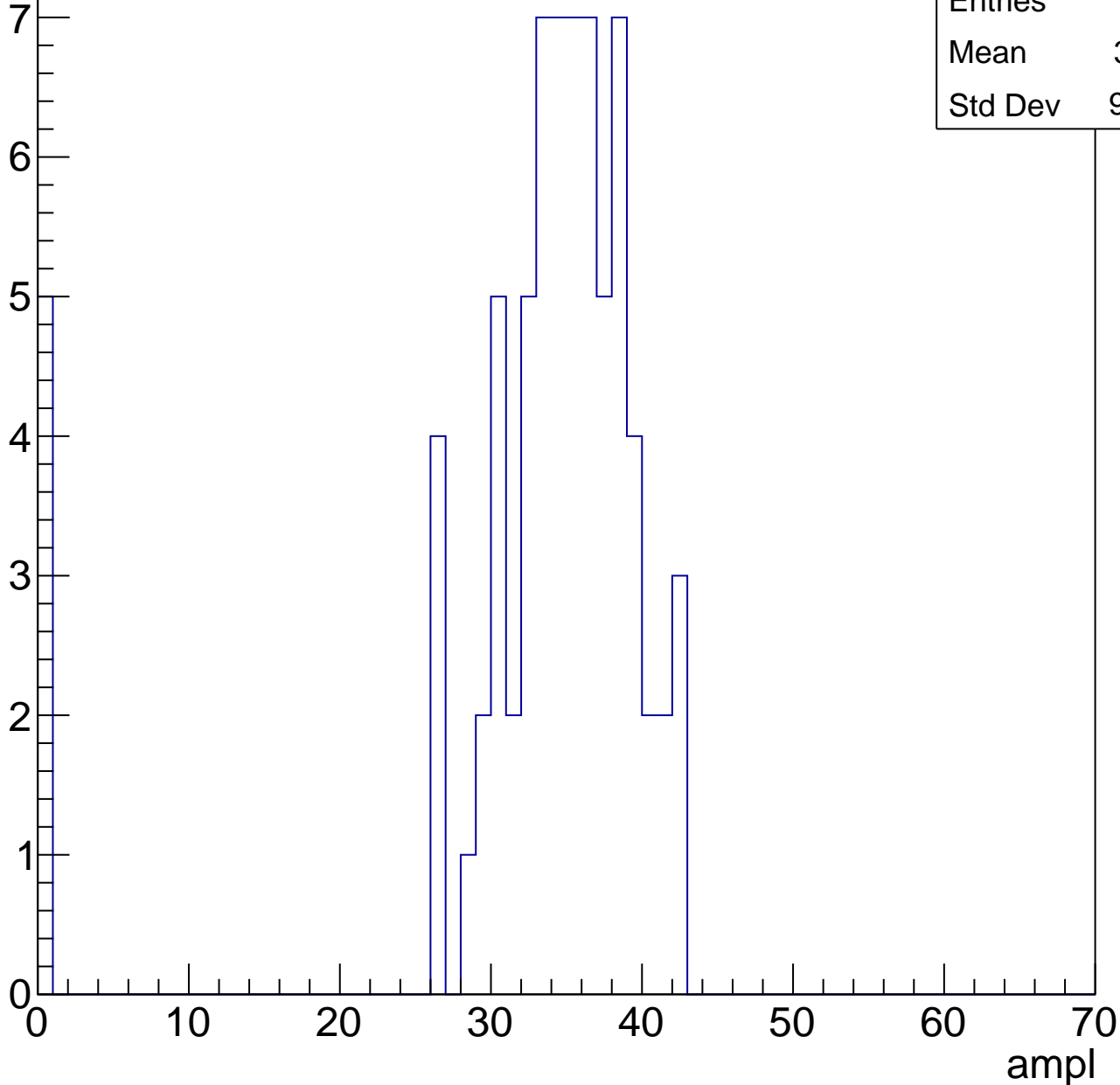


B1L103S, U12-ch98, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	75
Mean	32.31
Std Dev	9.442

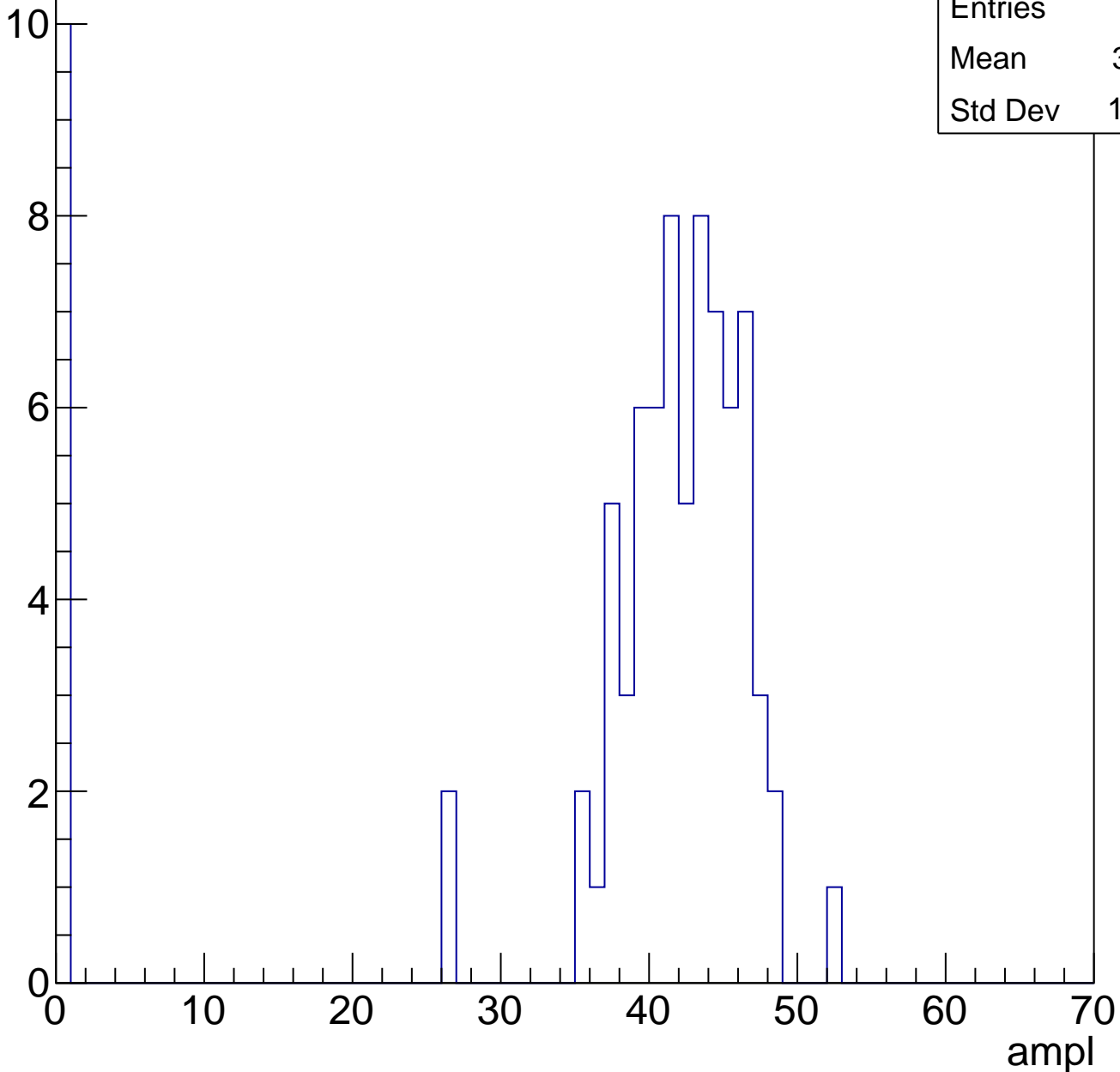


B1L103S, U12-ch98, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	82
Mean	36.61
Std Dev	14.23

Entry



B1L103S, U12-ch98, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	64
Mean	48.83
Std Dev	3.71

Entry

10

8

6

4

2

0

0

10

20

30

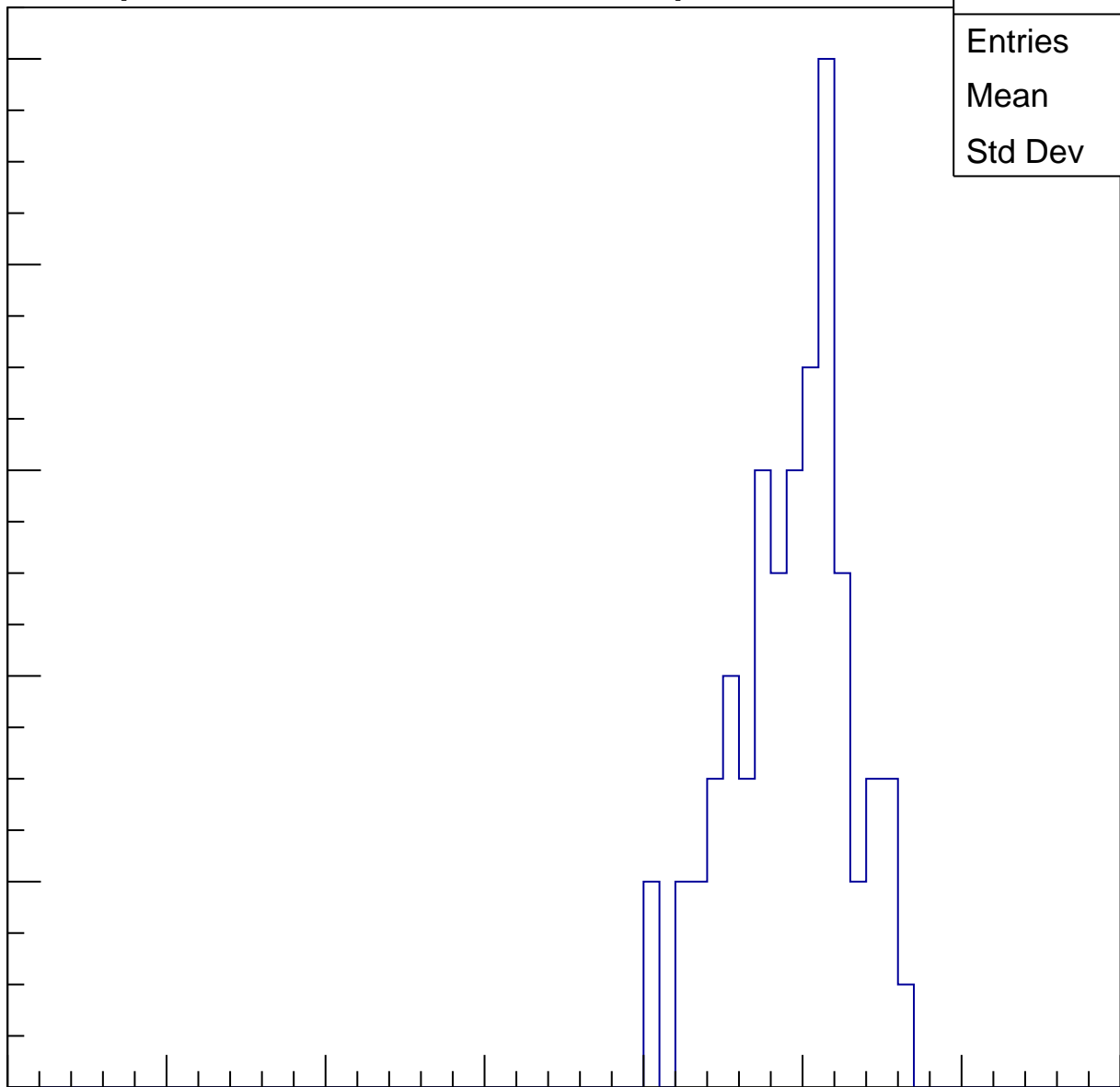
40

50

60

70

ampl

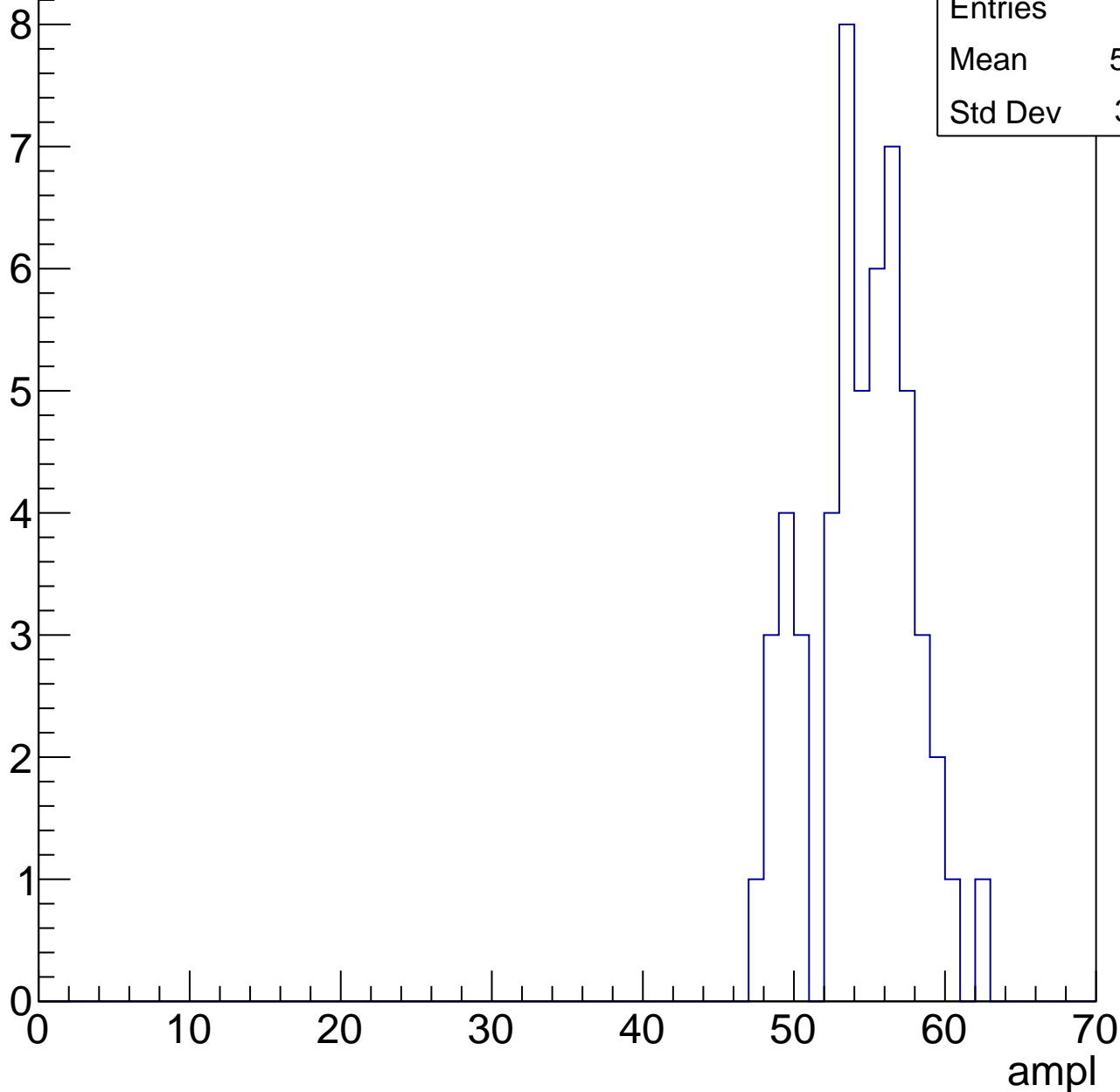


B1L103S, U12-ch98, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

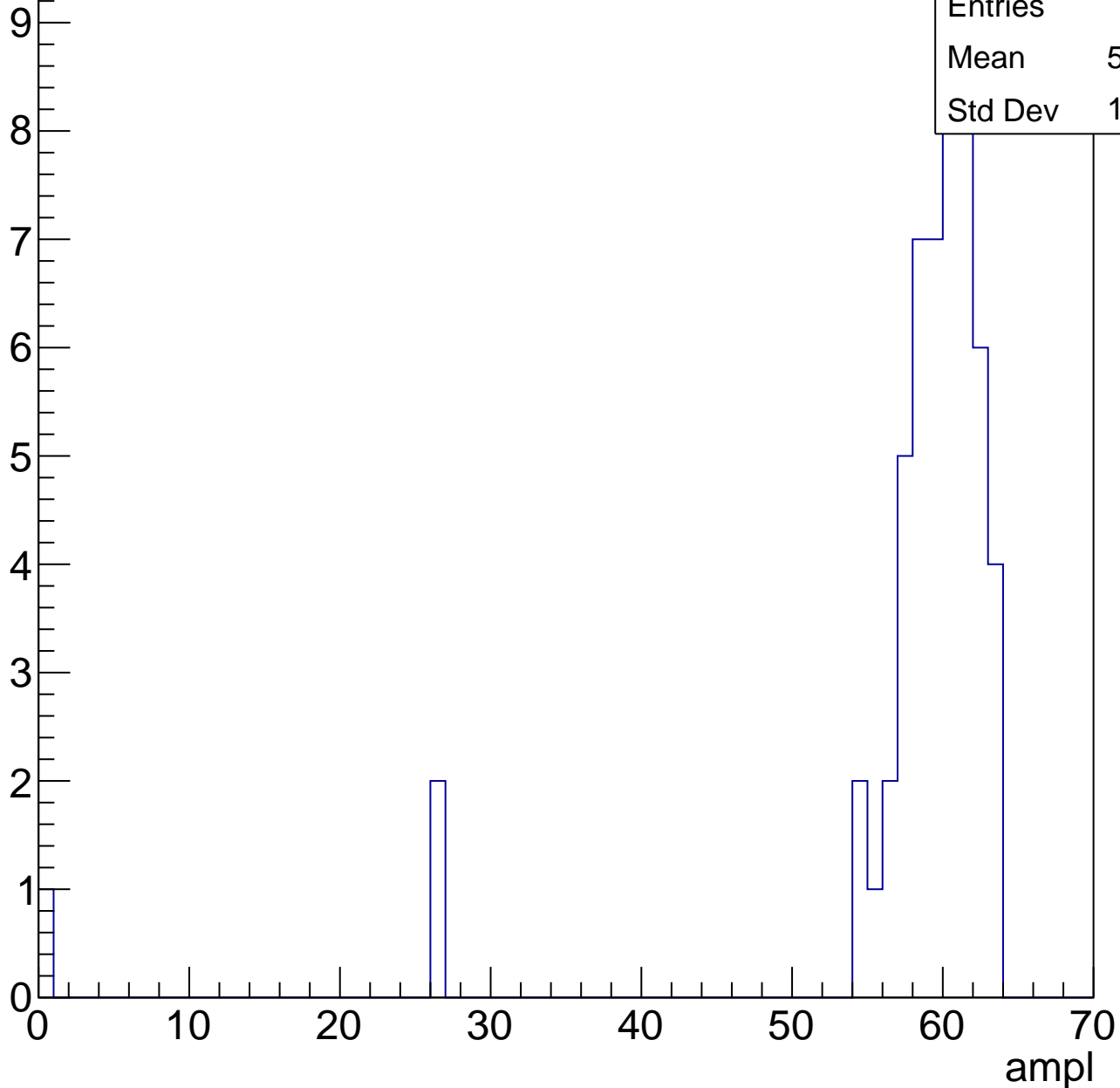
Entries	53
Mean	53.96
Std Dev	3.381



B1L103S, U12-ch98, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

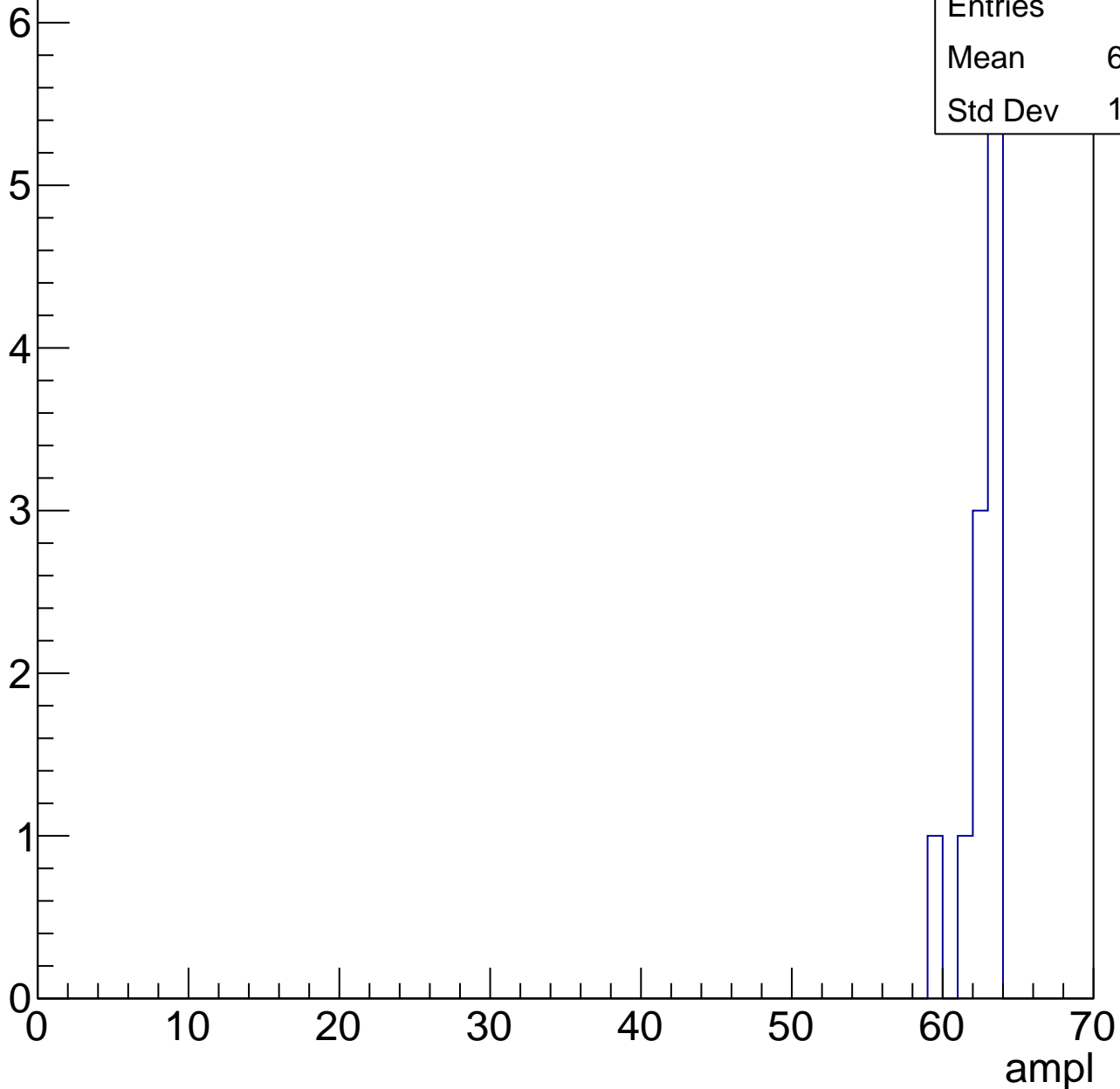


B1L103S, U12-ch98, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	11
Mean	62.18
Std Dev	1.192



B1L103S, U12-ch98, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

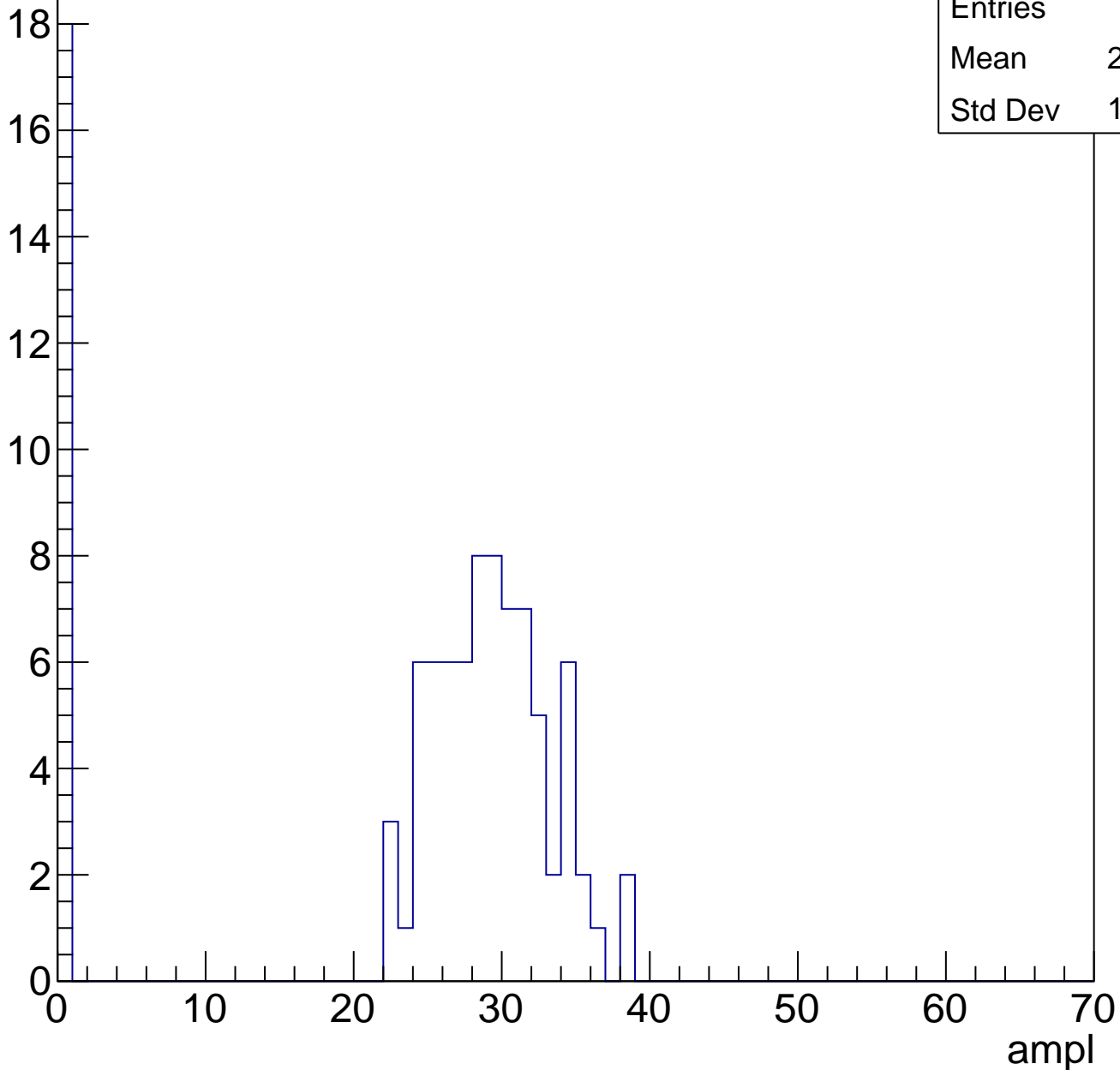
Entries	19
Mean	0
Std Dev	0

B1L103S, U12-ch99, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	94
Mean	23.36
Std Dev	11.85

Entry



B1L103S, U12-ch99, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	81
Mean	31.37
Std Dev	12.87

Entry

10

8

6

4

2

0

0

10

20

30

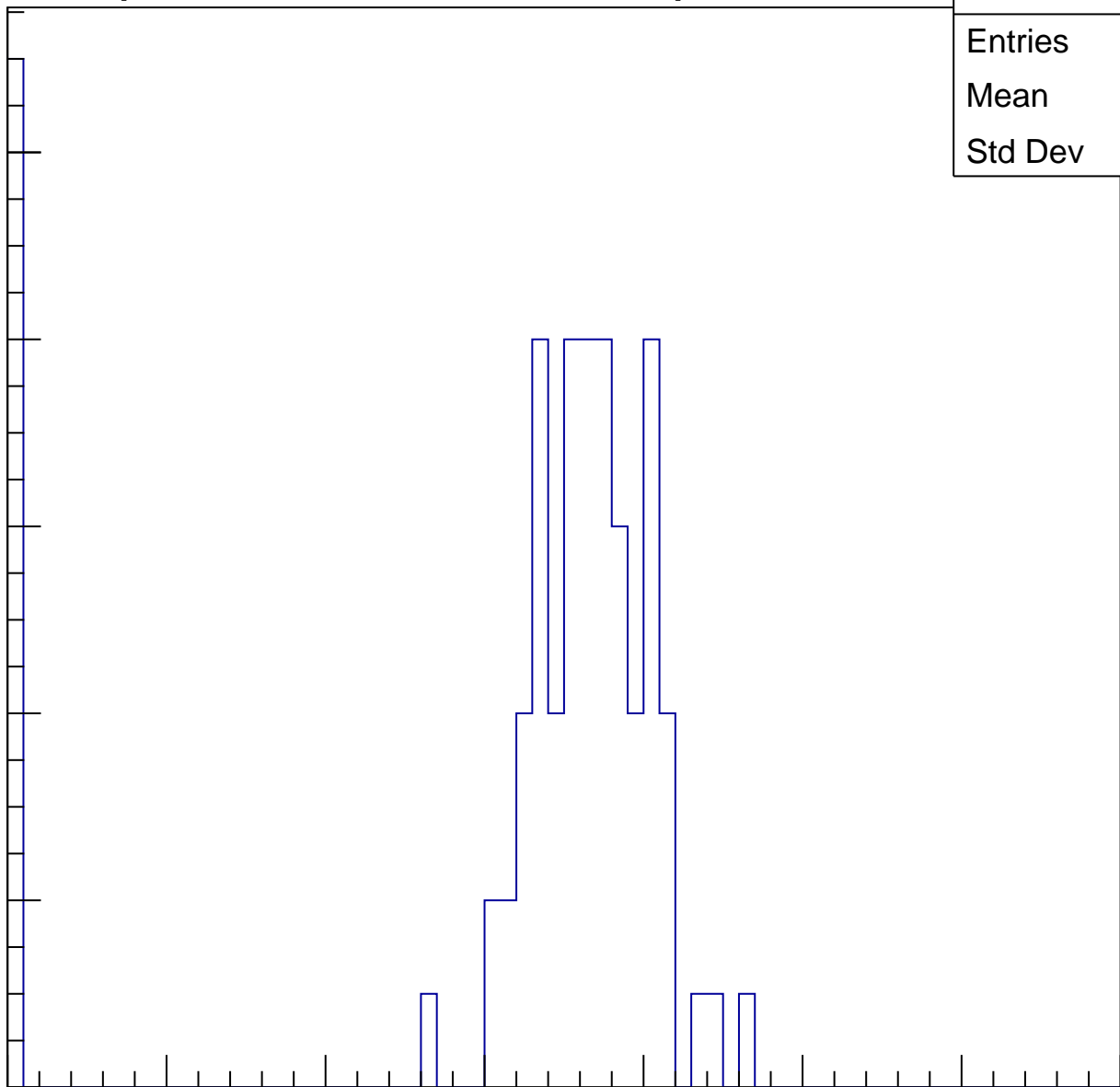
40

50

60

70

ampl

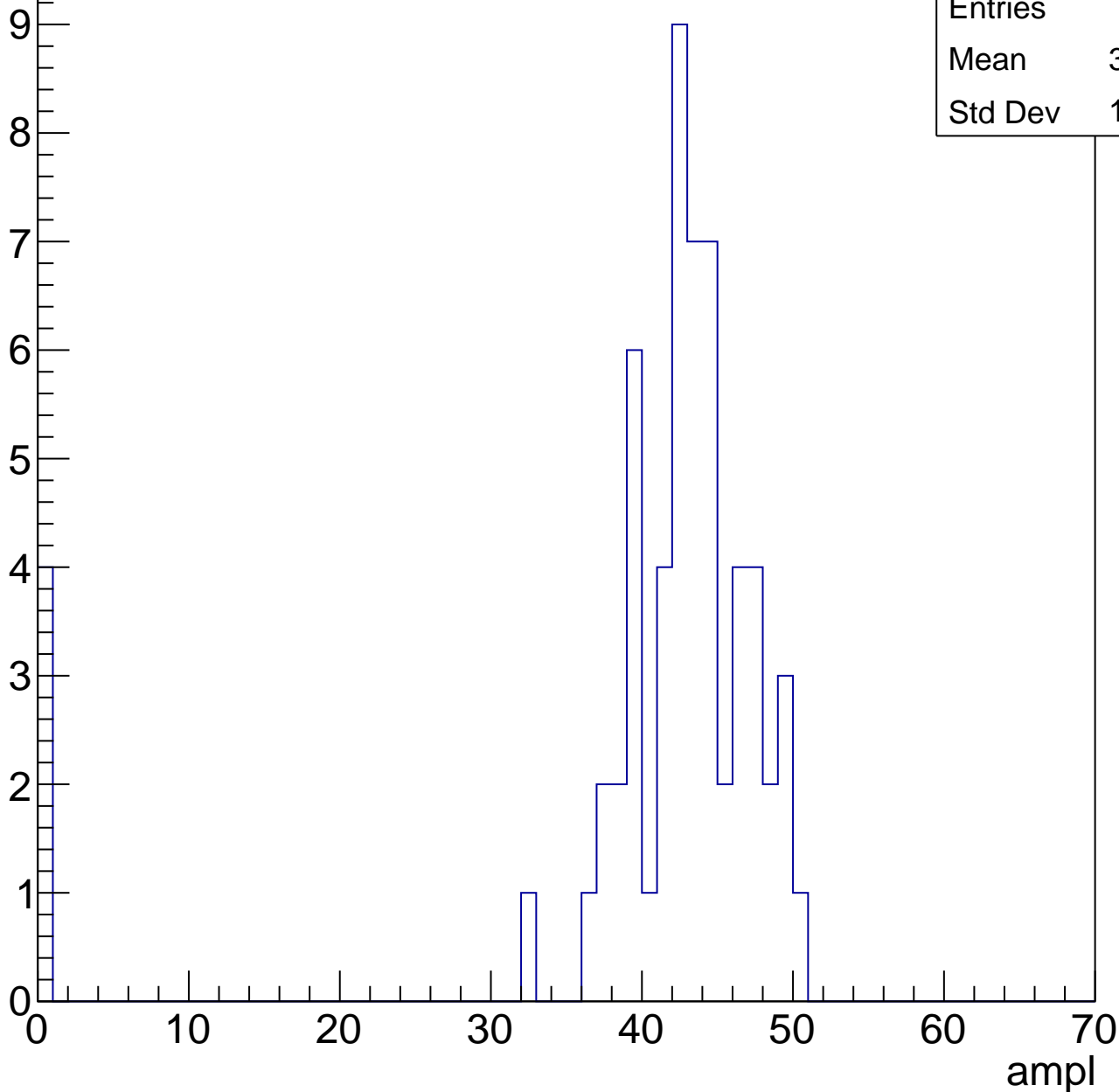


B1L103S, U12-ch99, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	39.97
Std Dev	11.25



B1L103S, U12-ch99, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	78
Mean	49.1
Std Dev	3.855

Entry

10

8

6

4

2

0

0

10

20

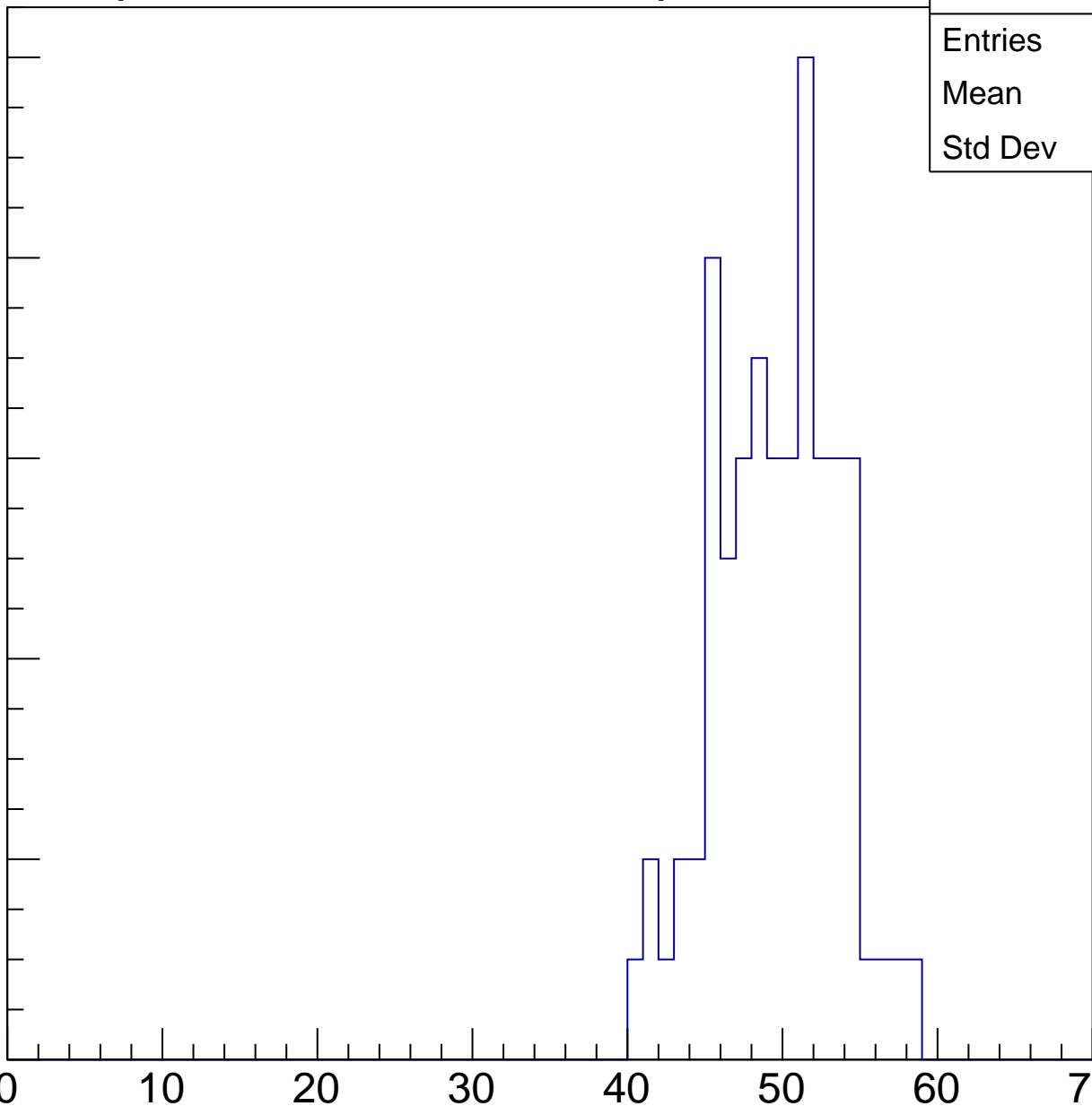
30

40

50

60

ampl

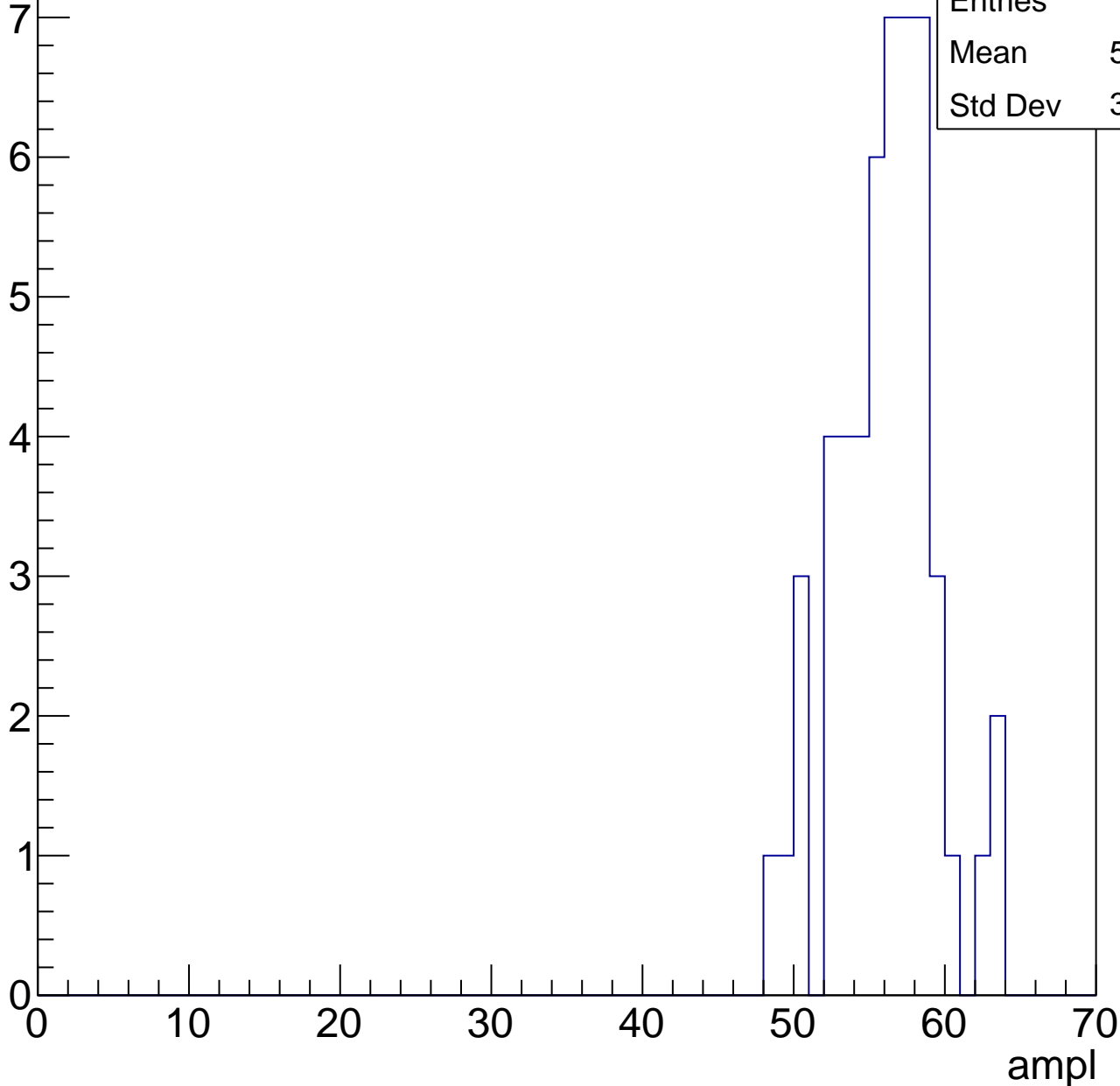


B1L103S, U12-ch99, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	51
Mean	55.59
Std Dev	3.273

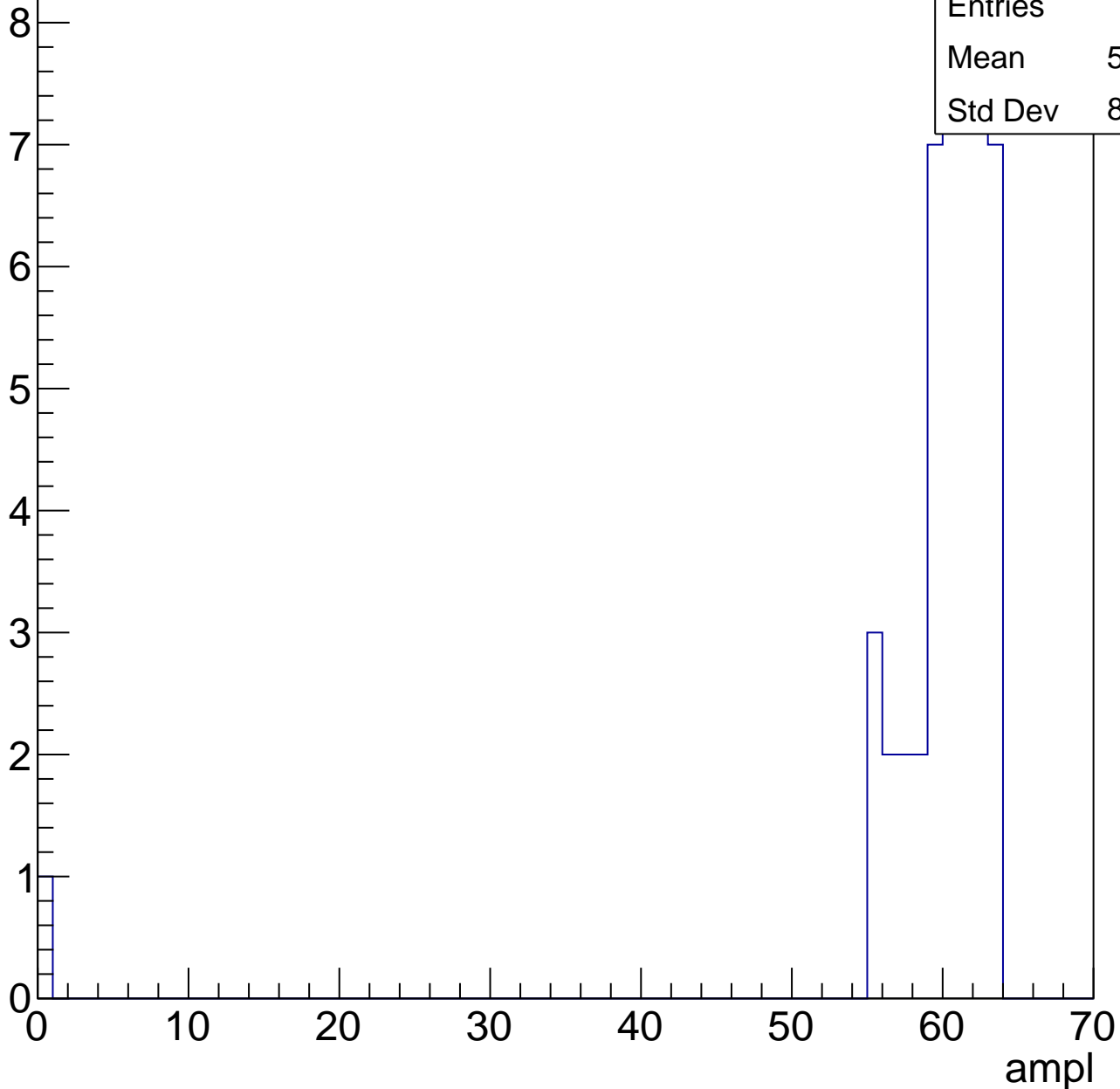


B1L103S, U12-ch99, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	48
Mean	58.85
Std Dev	8.874



B1L103S, U12-ch99, adc6

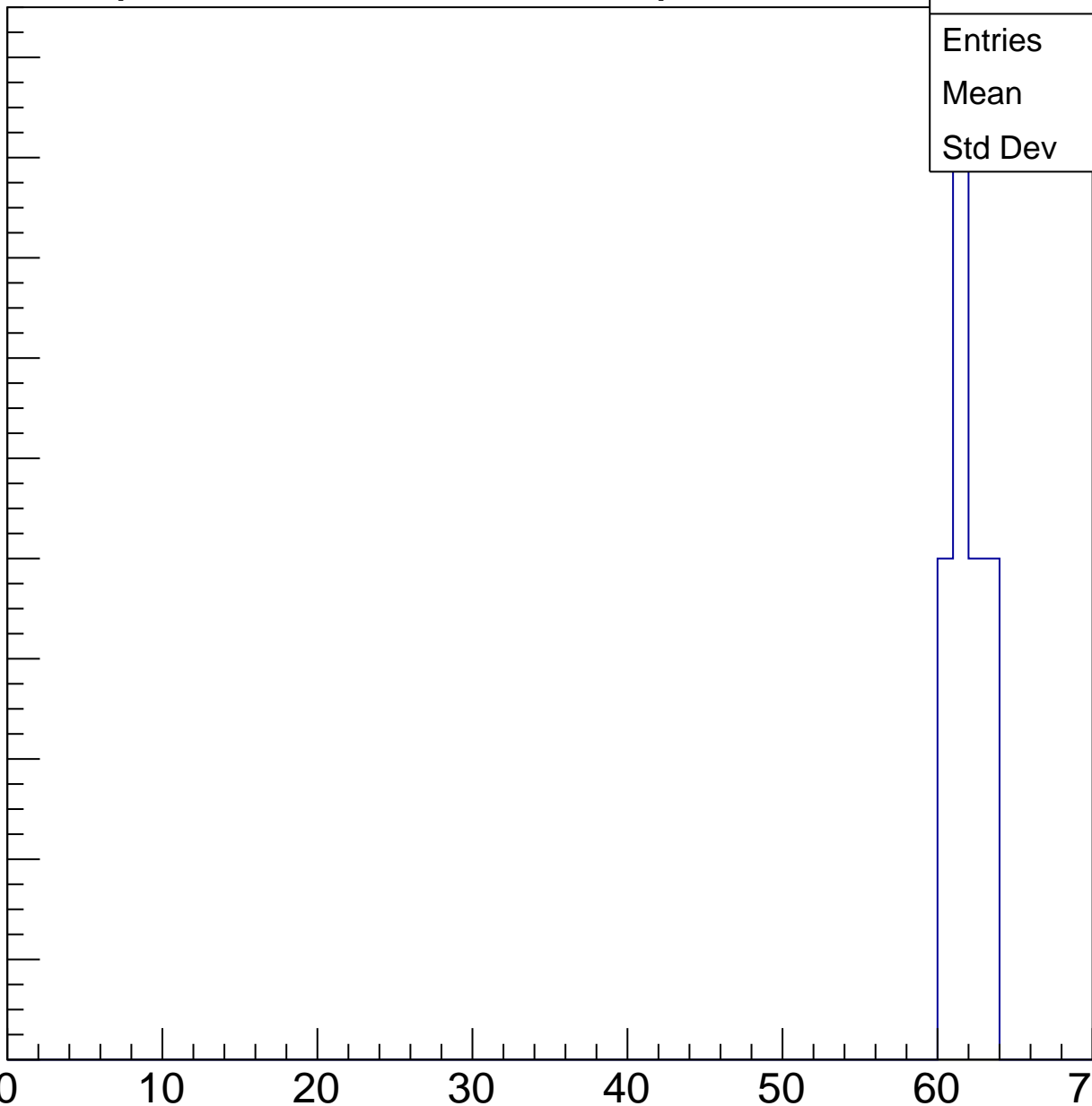
calib_packv5_041523_1651.root, FC#0, port C2

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	5
Mean	61.4
Std Dev	1.02

ampl

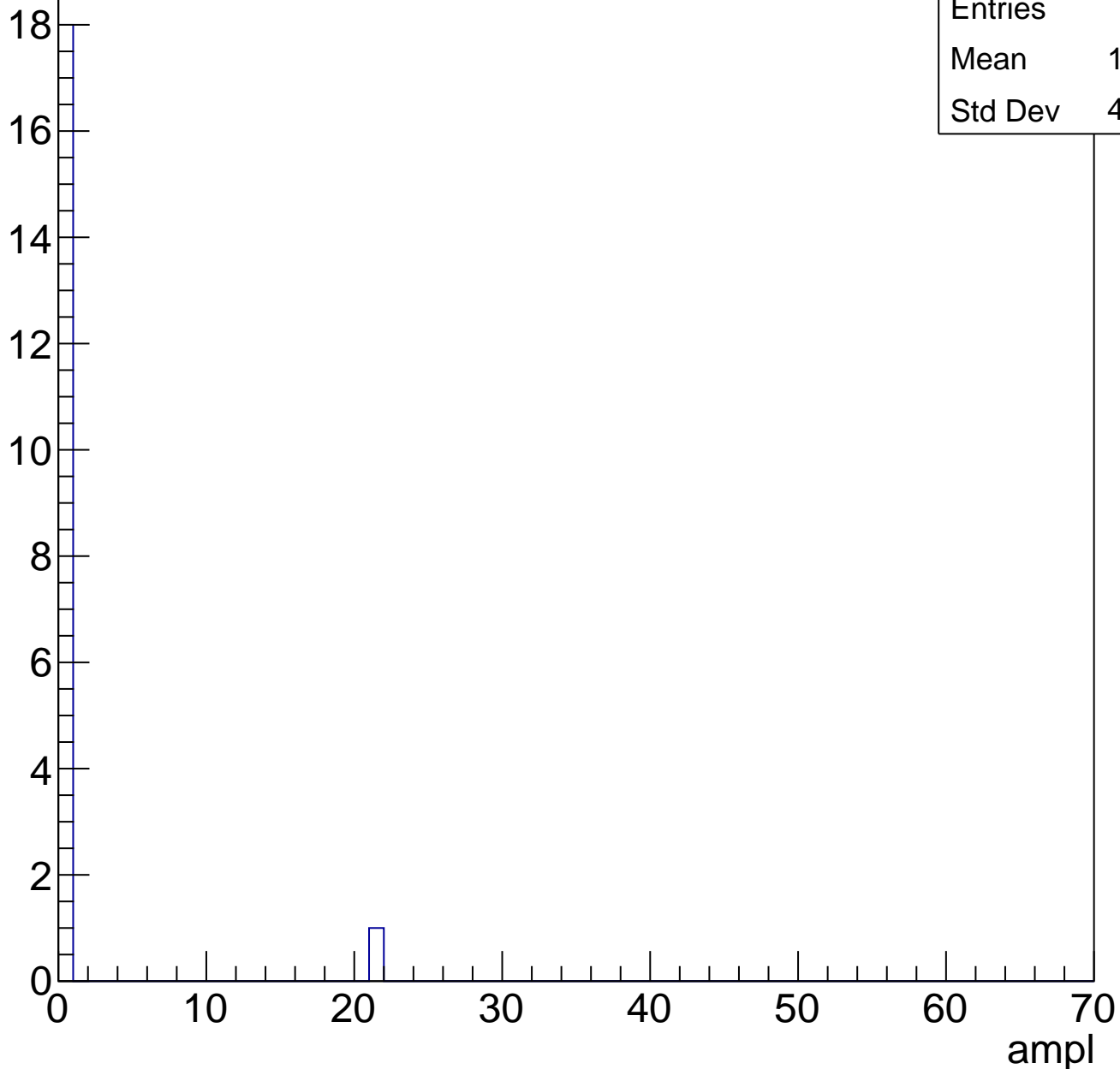


B1L103S, U12-ch99, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.105
Std Dev	4.689

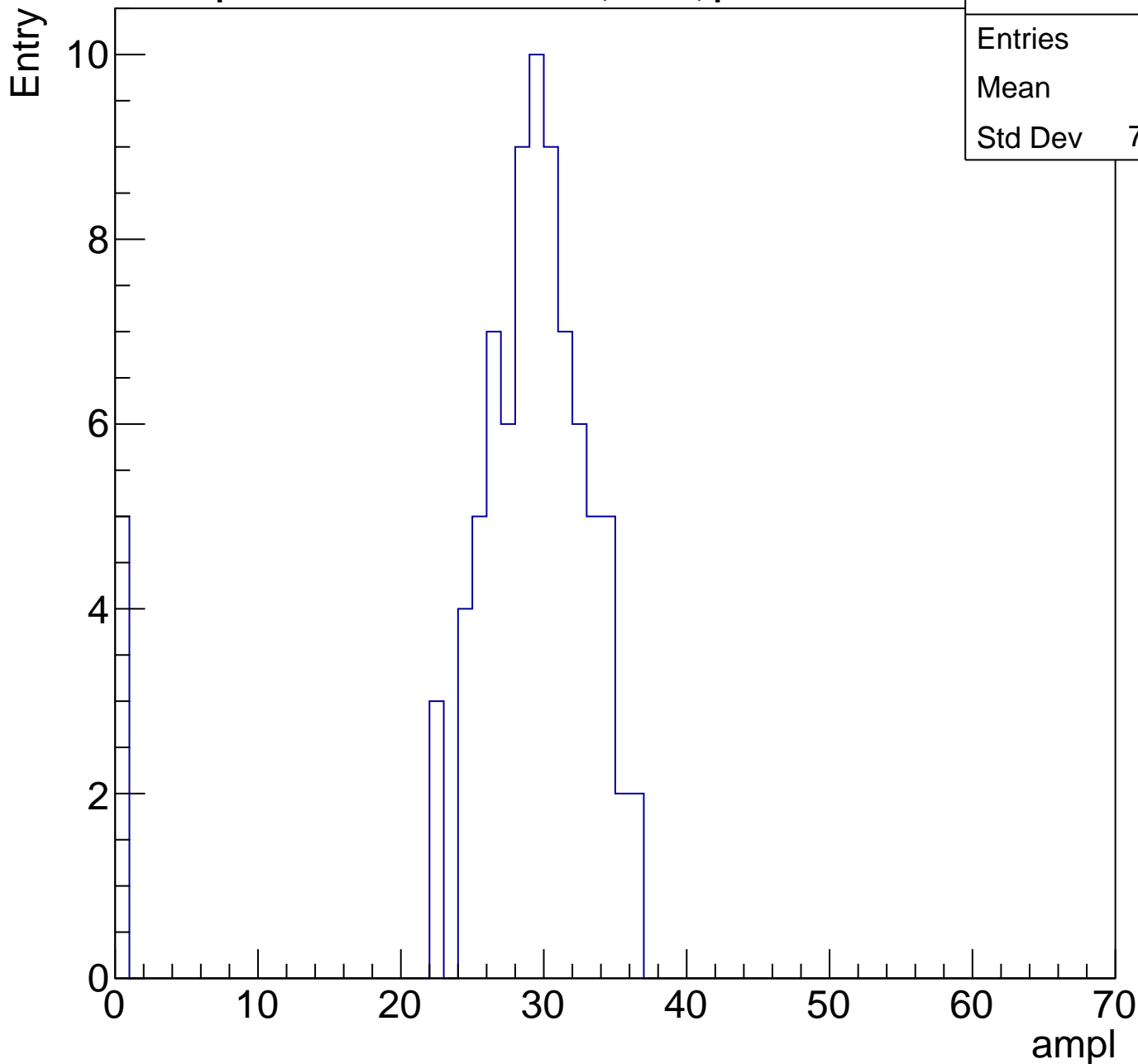
Entry



B1L103S, U12-ch100, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	85
Mean	27.4
Std Dev	7.574

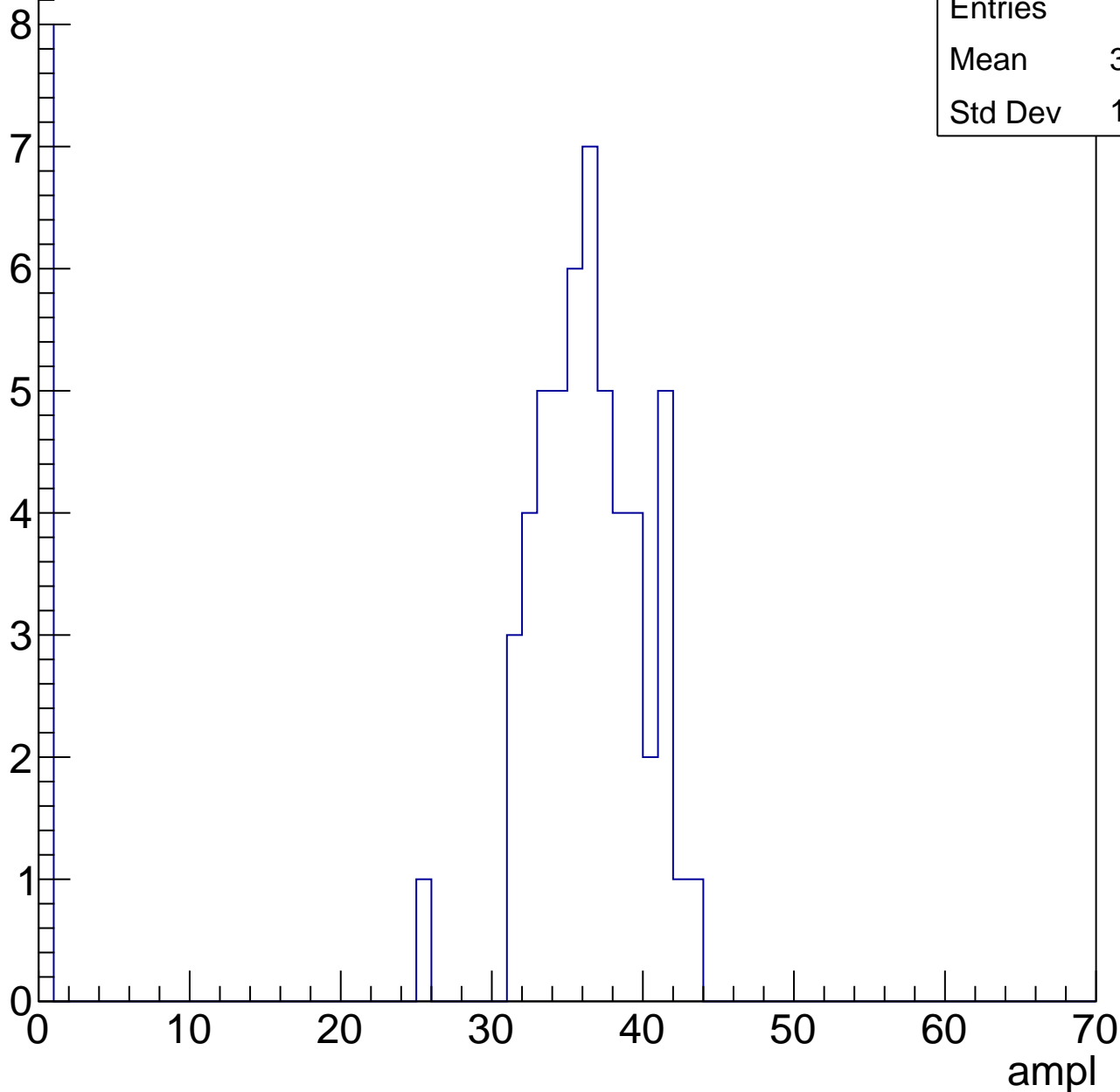


B1L103S, U12-ch100, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	31.25
Std Dev	12.56

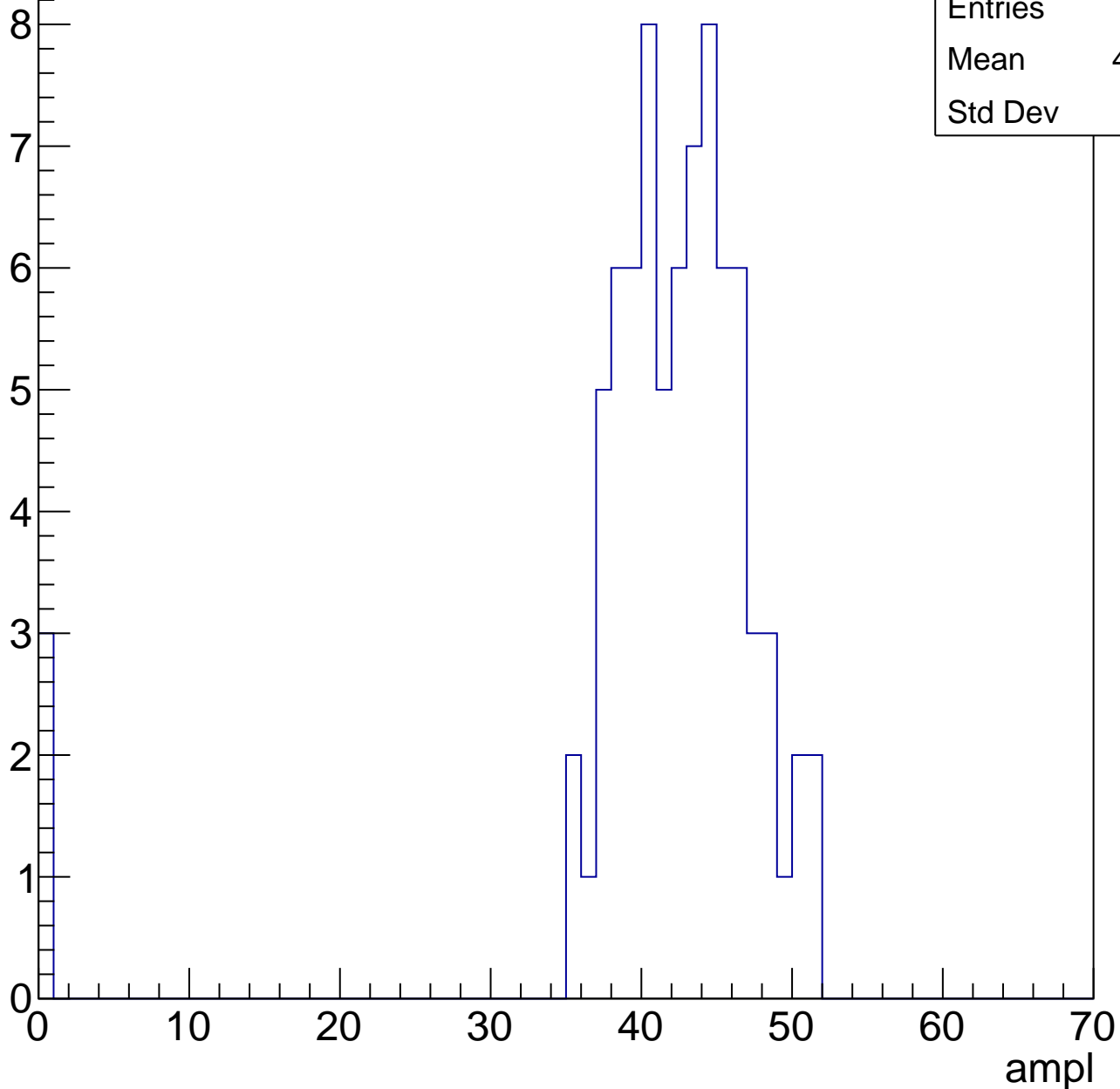


B1L103S, U12-ch100, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	80
Mean	40.81
Std Dev	8.9

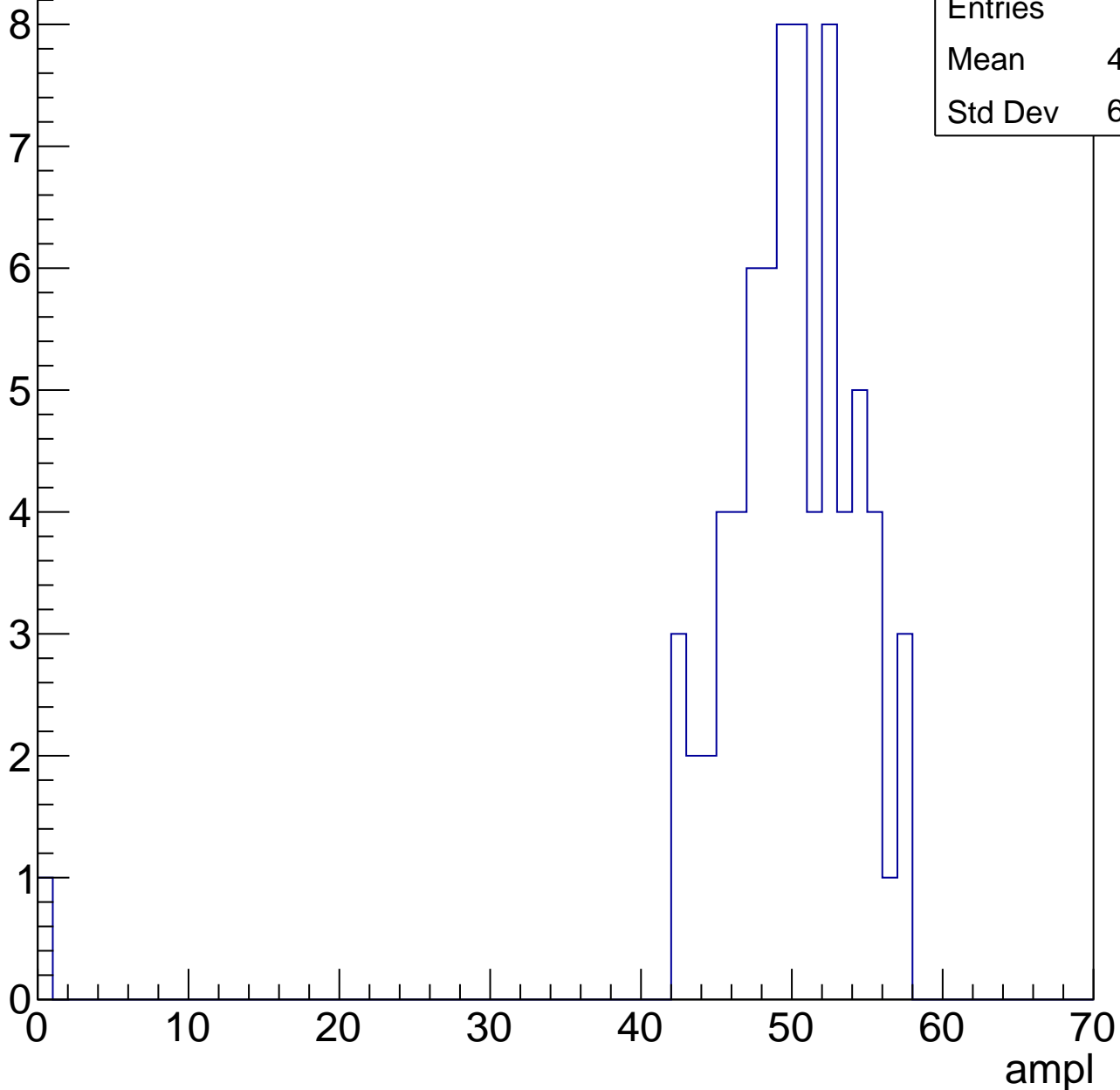


B1L103S, U12-ch100, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	73
Mean	48.97
Std Dev	6.894

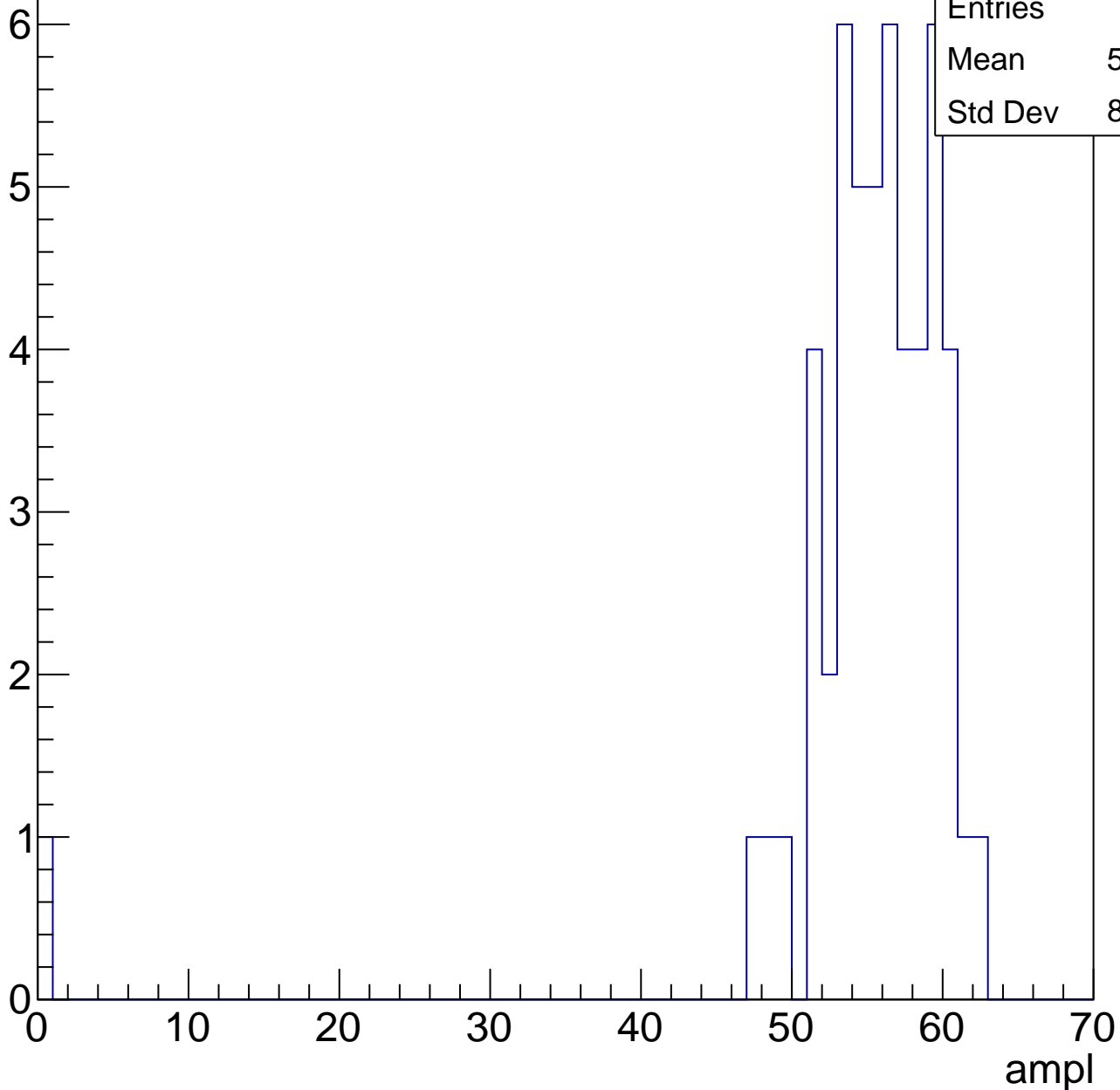


B1L103S, U12-ch100, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	52
Mean	54.38
Std Dev	8.325

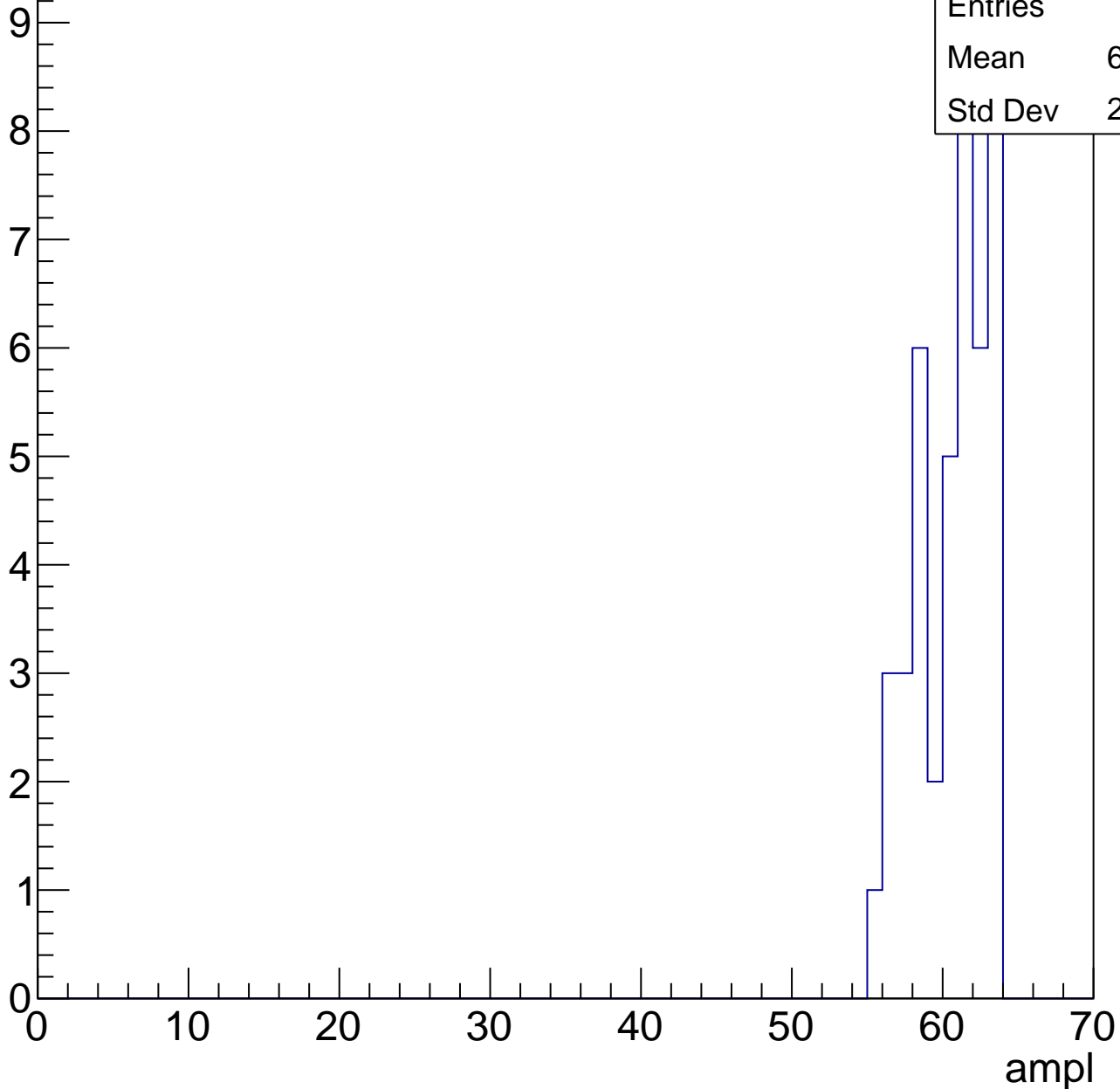


B1L103S, U12-ch100, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

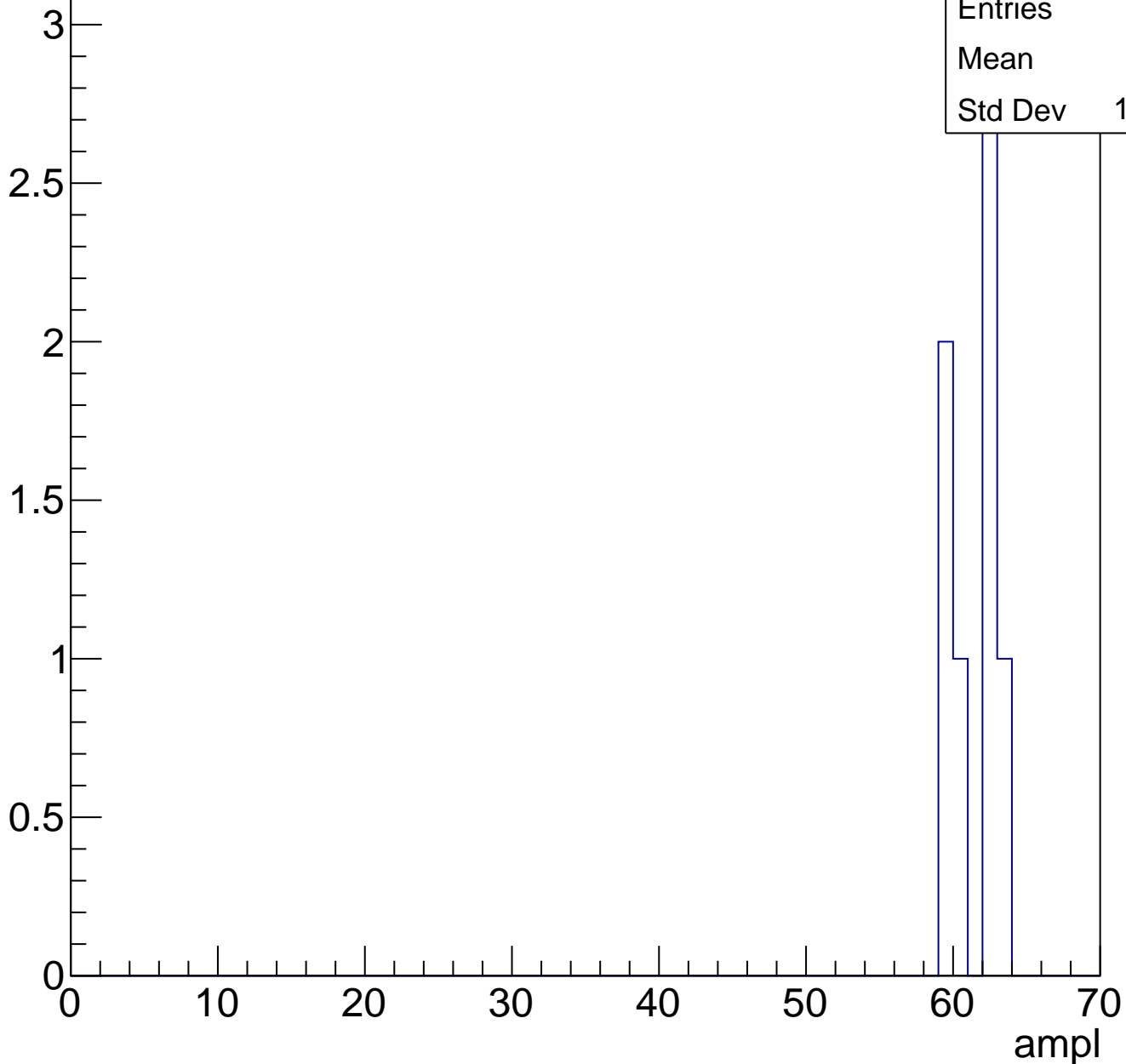
Entries	43
Mean	60.12
Std Dev	2.315



B1L103S, U12-ch100, adc6

calib_packv5_041523_1651.root, FC#0, port C2

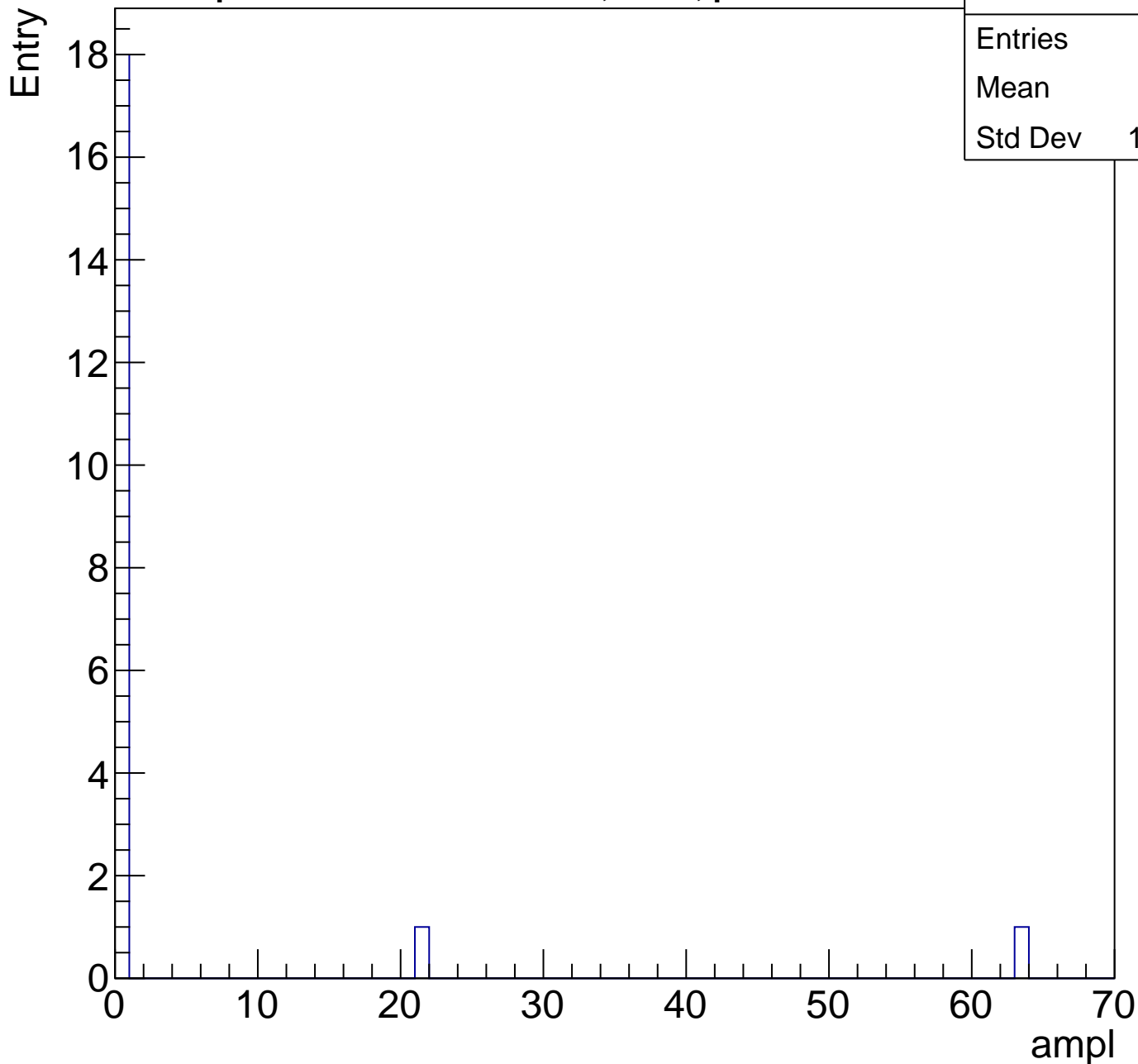
Entry



B1L103S, U12-ch100, adc7

calib_packv5_041523_1651.root, FC#0, port C2

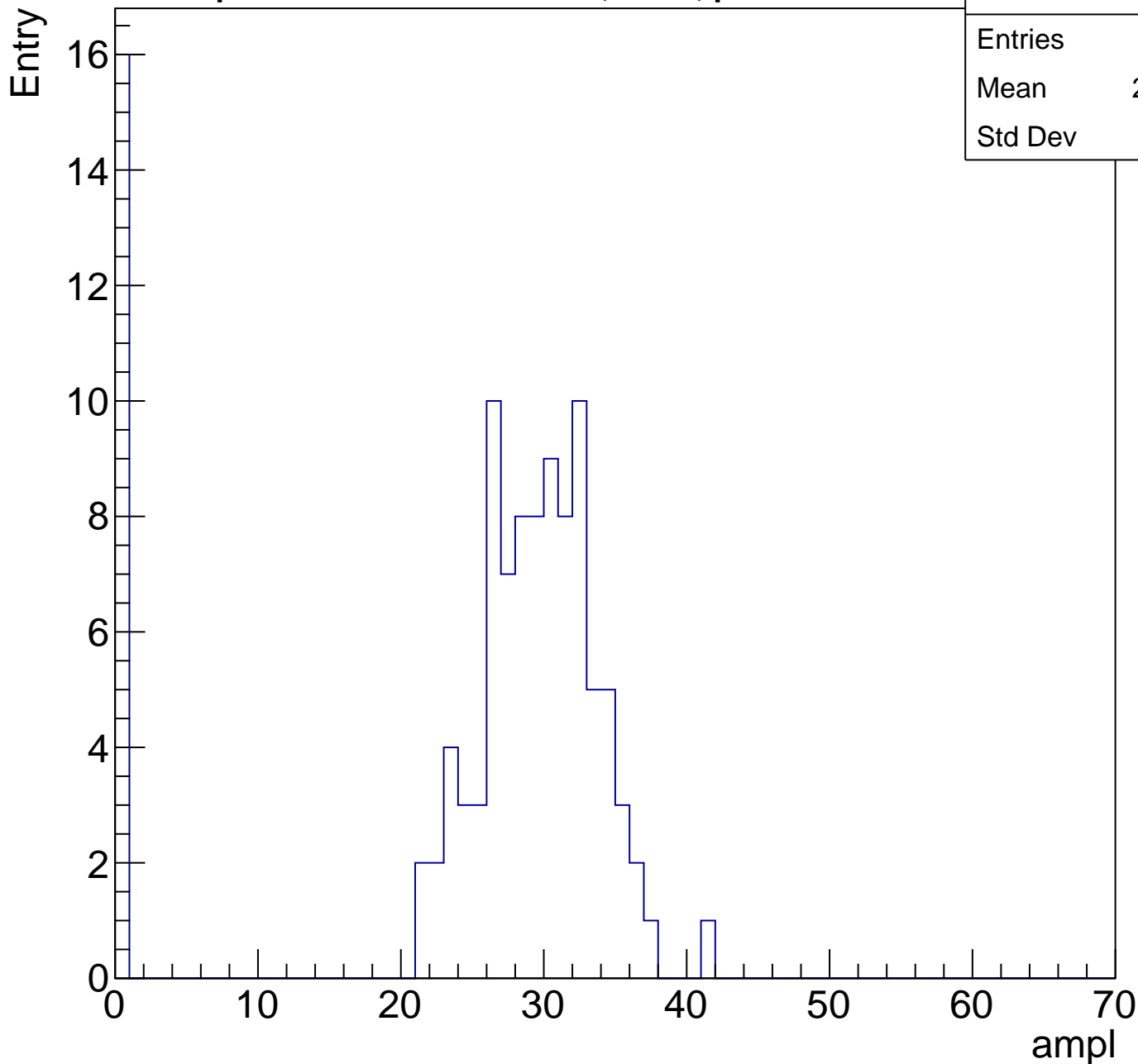
Entries	20
Mean	4.2
Std Dev	14.24



B1L103S, U12-ch101, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	107
Mean	24.84
Std Dev	11.01



B1L103S, U12-ch101, adc1

calib_packv5_041523_1651.root, FC#0, port C2

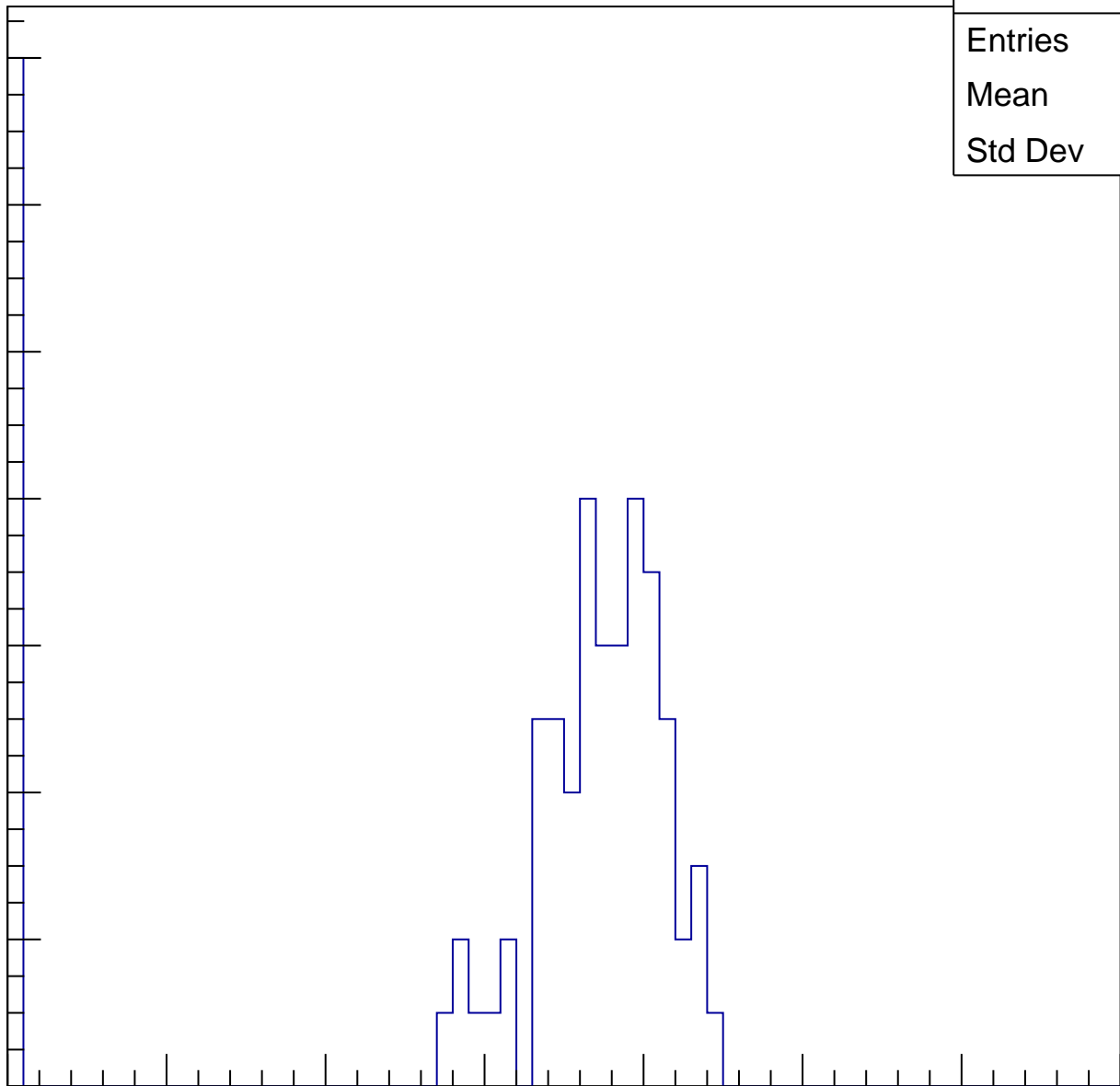
Entries	81
Mean	30.51
Std Dev	14.37

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70

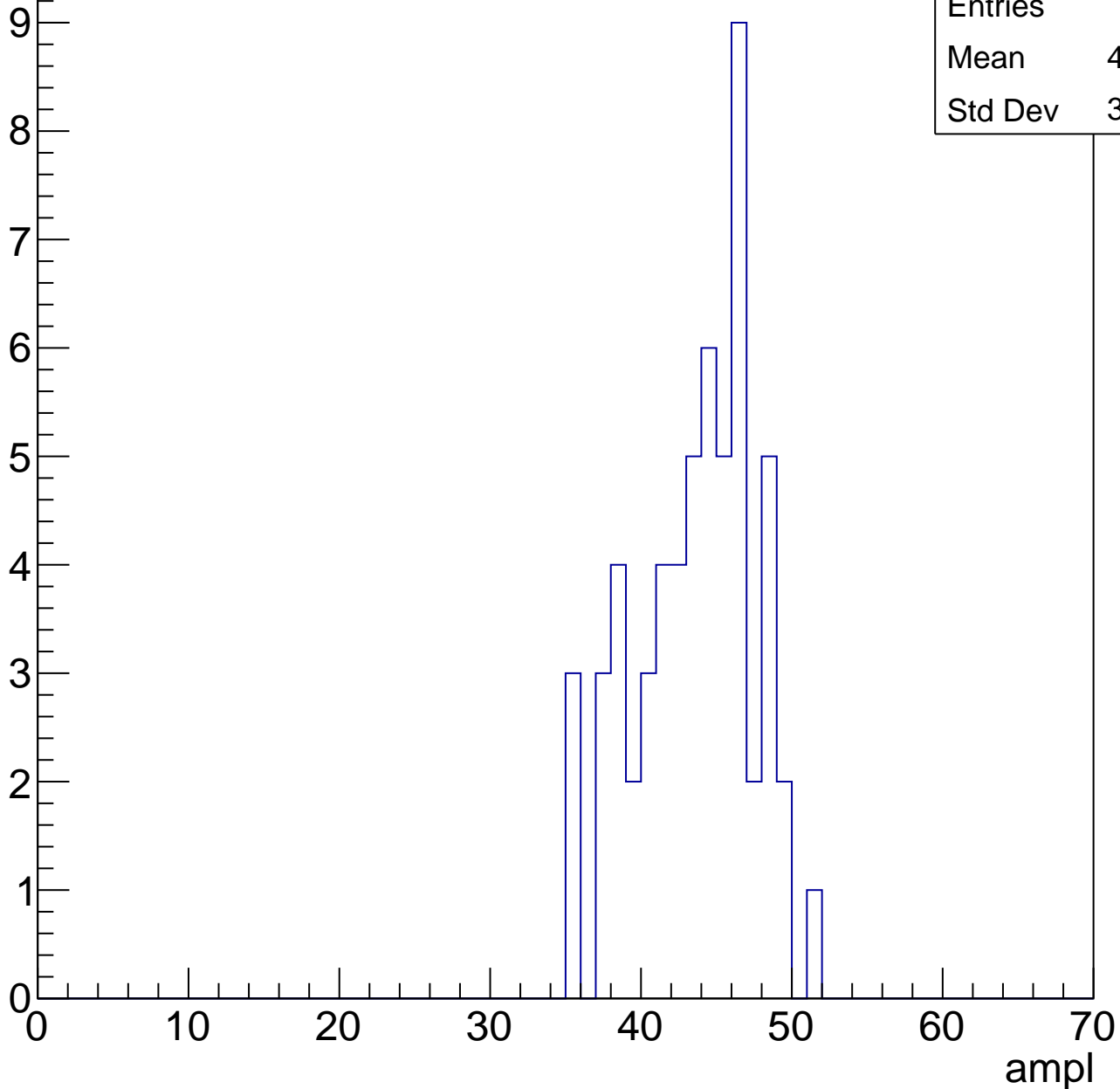


B1L103S, U12-ch101, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	43.09
Std Dev	3.892

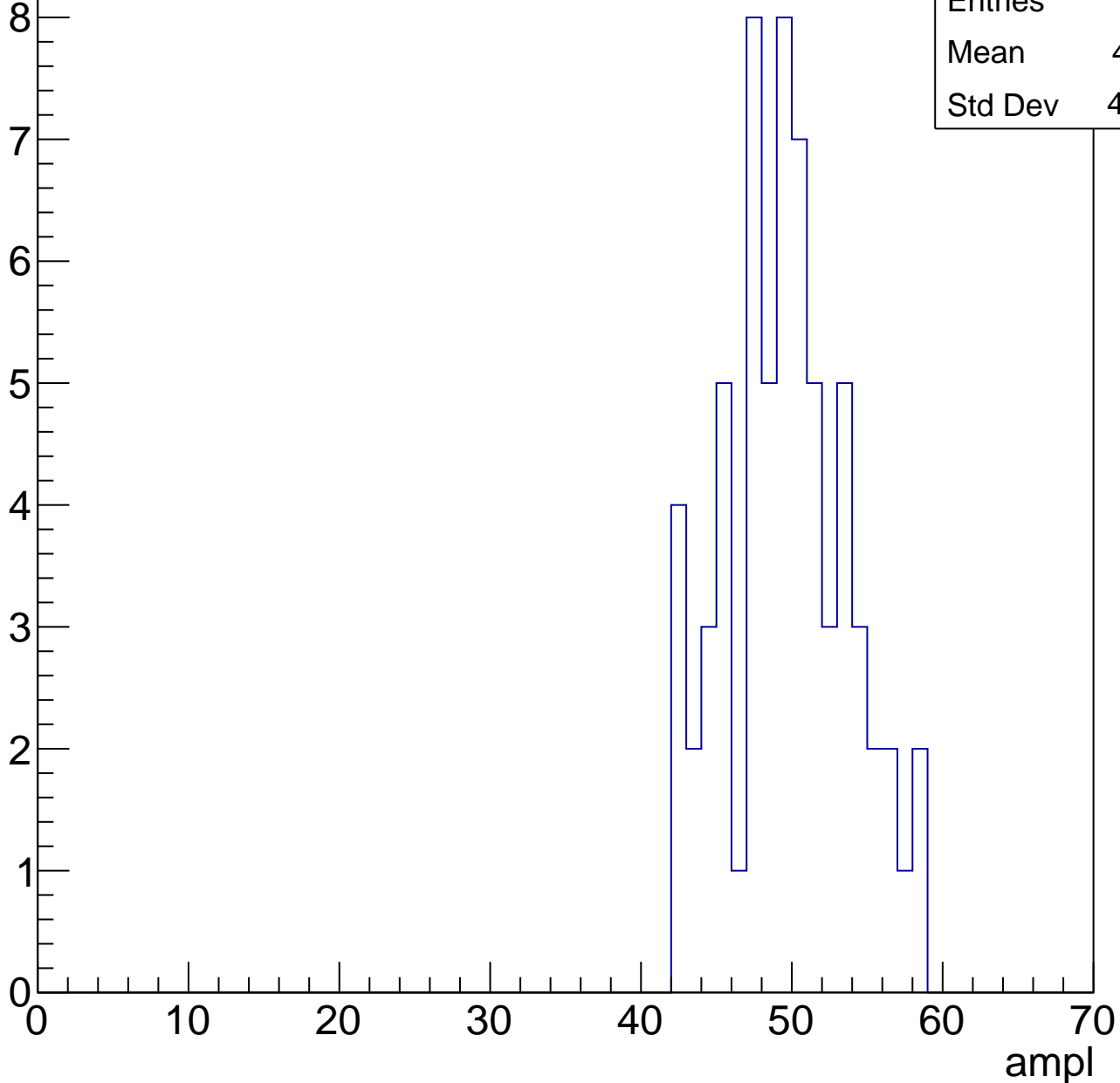


B1L103S, U12-ch101, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

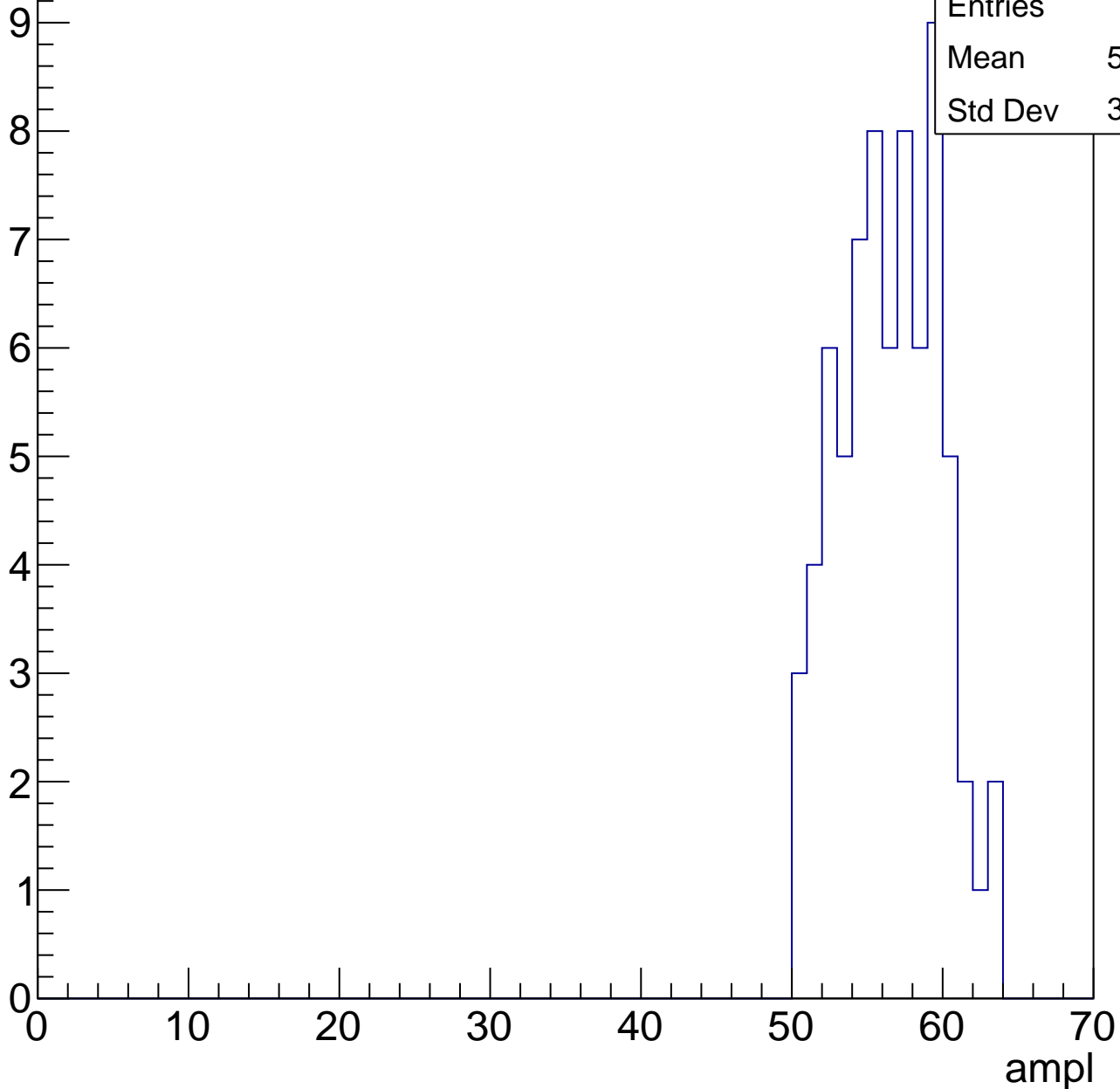
Entries	66
Mean	49.21
Std Dev	4.028



B1L103S, U12-ch101, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

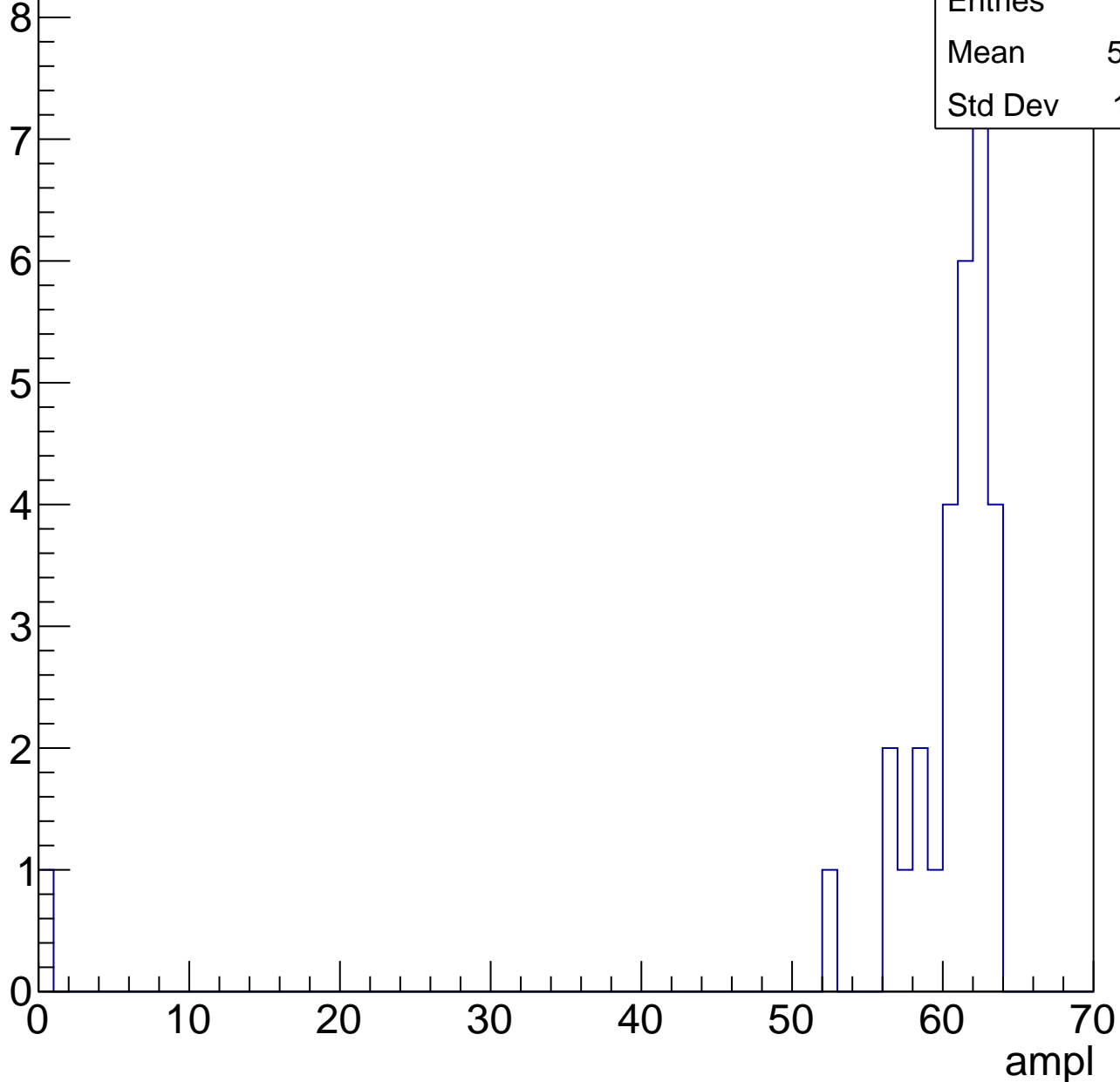


B1L103S, U12-ch101, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

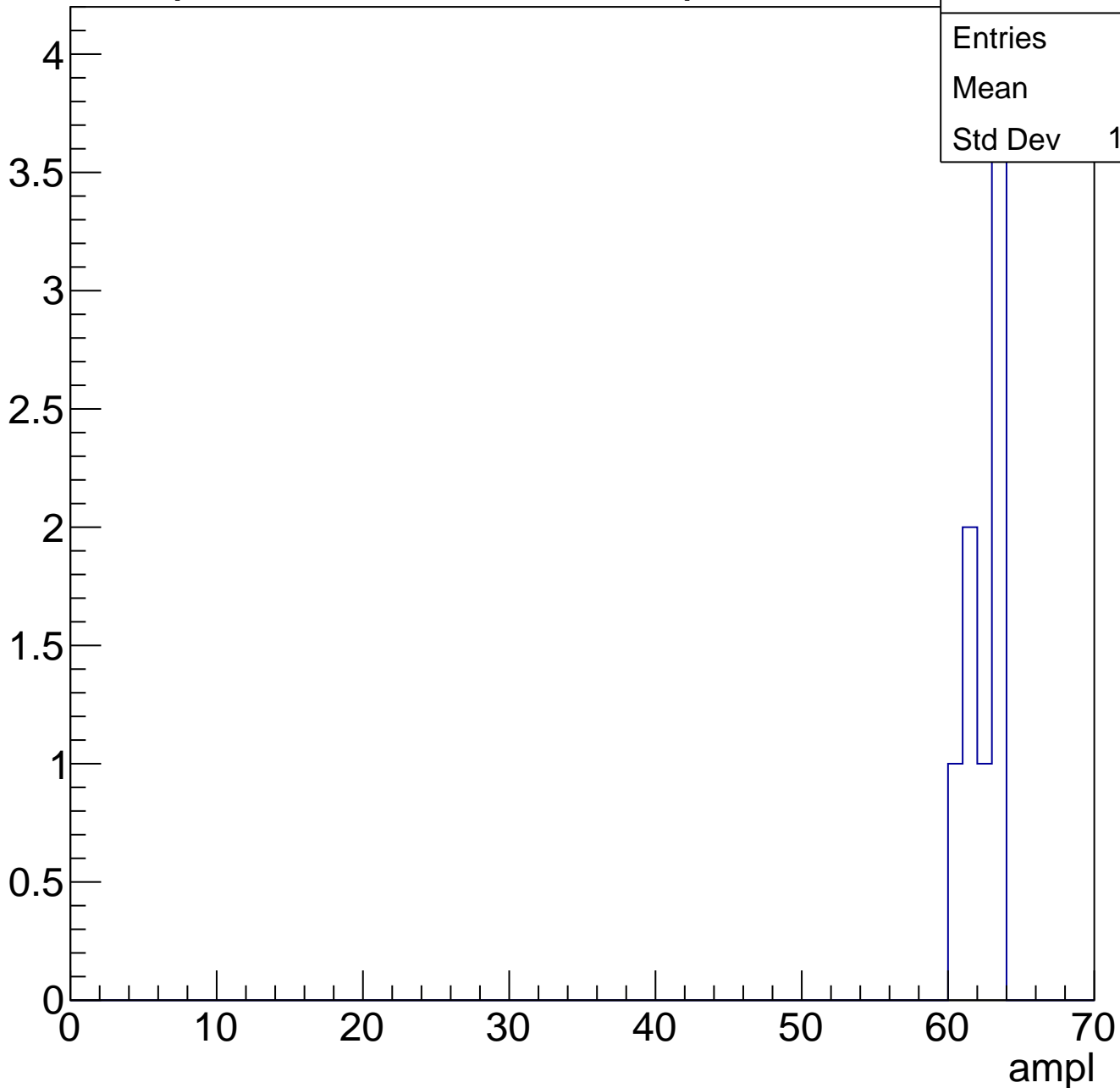
Entries	30
Mean	58.33
Std Dev	11.11



B1L103S, U12-ch101, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch101, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

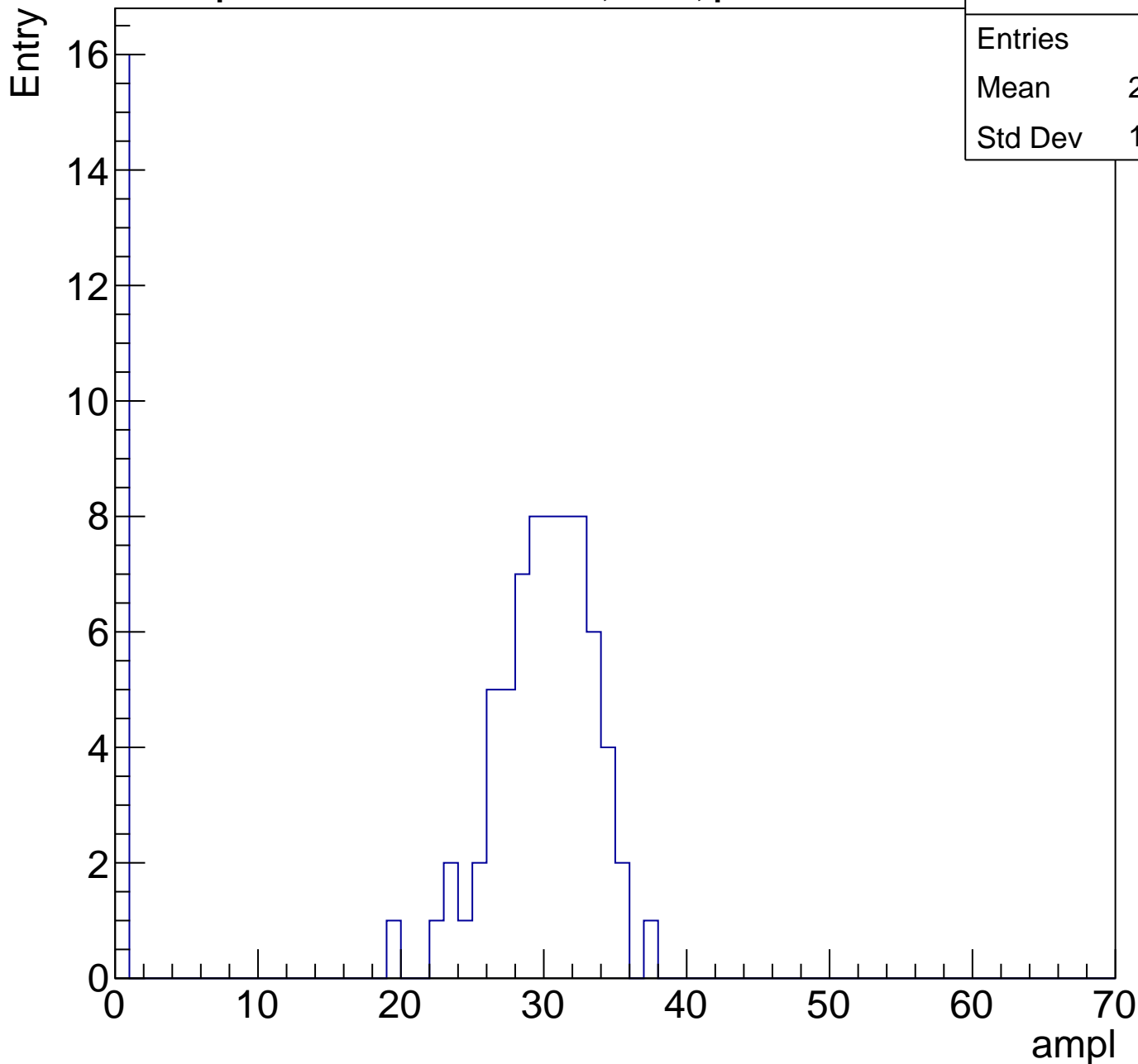
Entries	19
Mean	0
Std Dev	0

ampl

B1L103S, U12-ch102, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	85
Mean	23.99
Std Dev	11.94

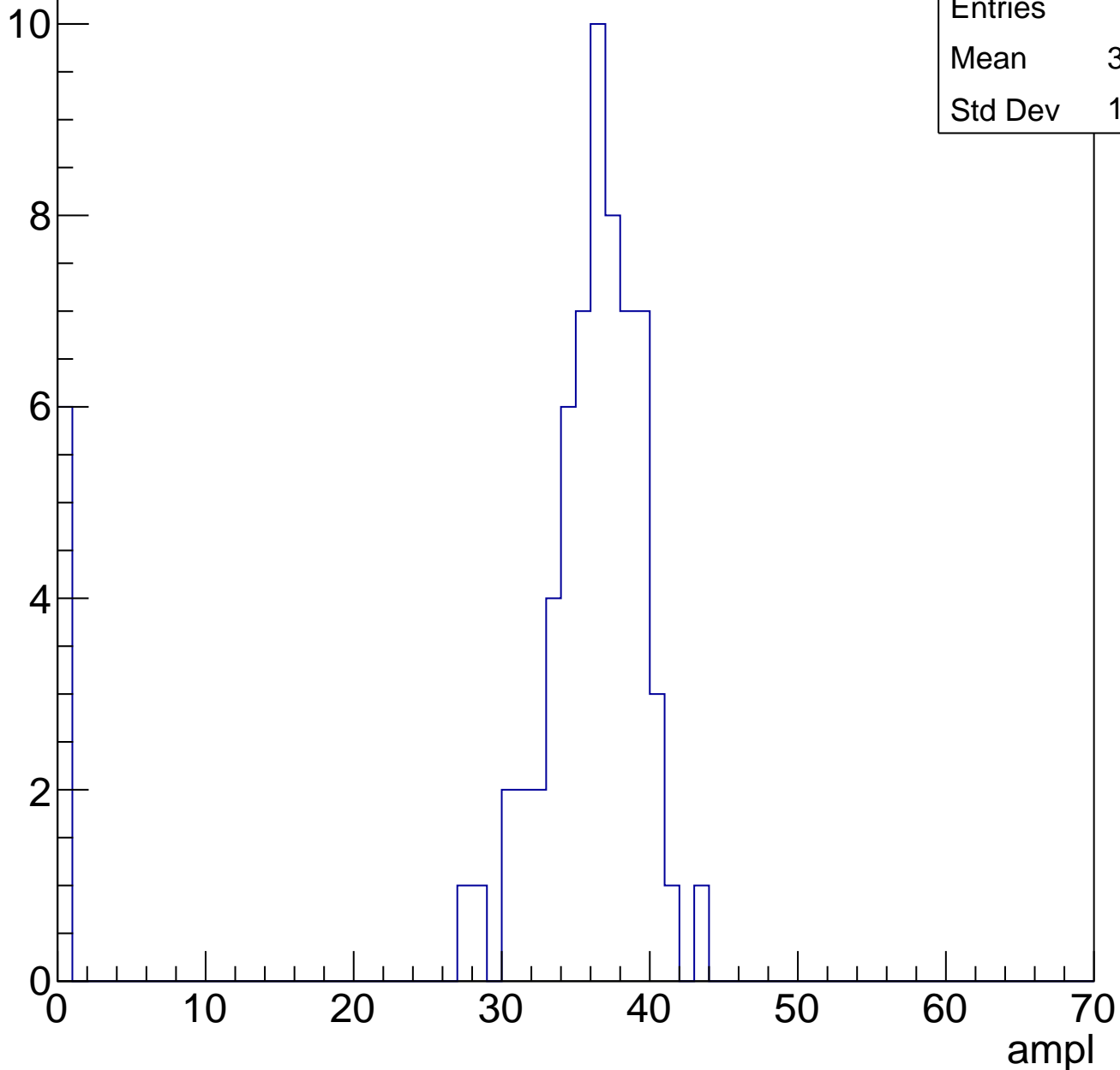


B1L103S, U12-ch102, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	68
Mean	32.66
Std Dev	10.58

Entry

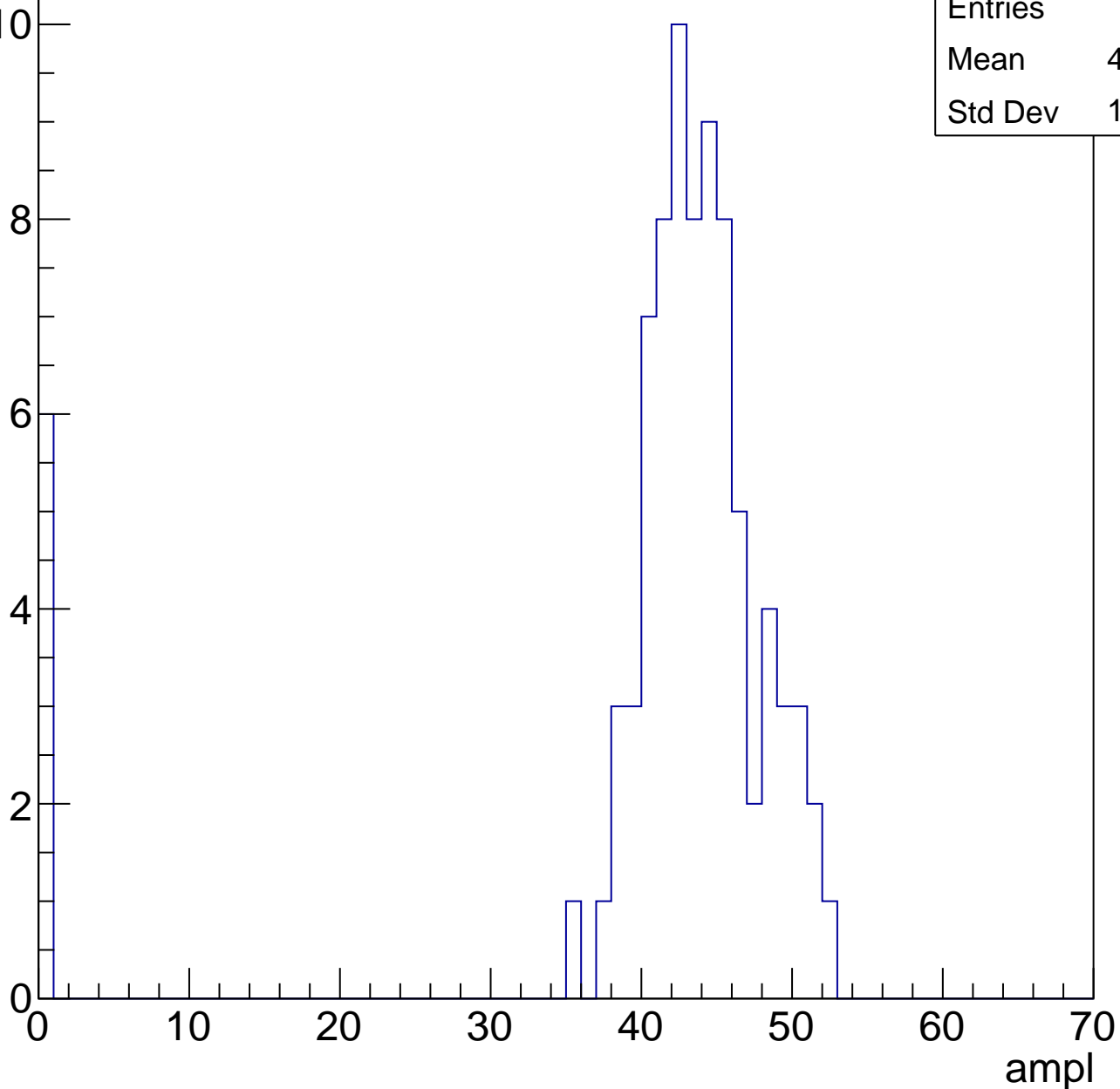


B1L103S, U12-ch102, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	84
Mean	40.45
Std Dev	11.73

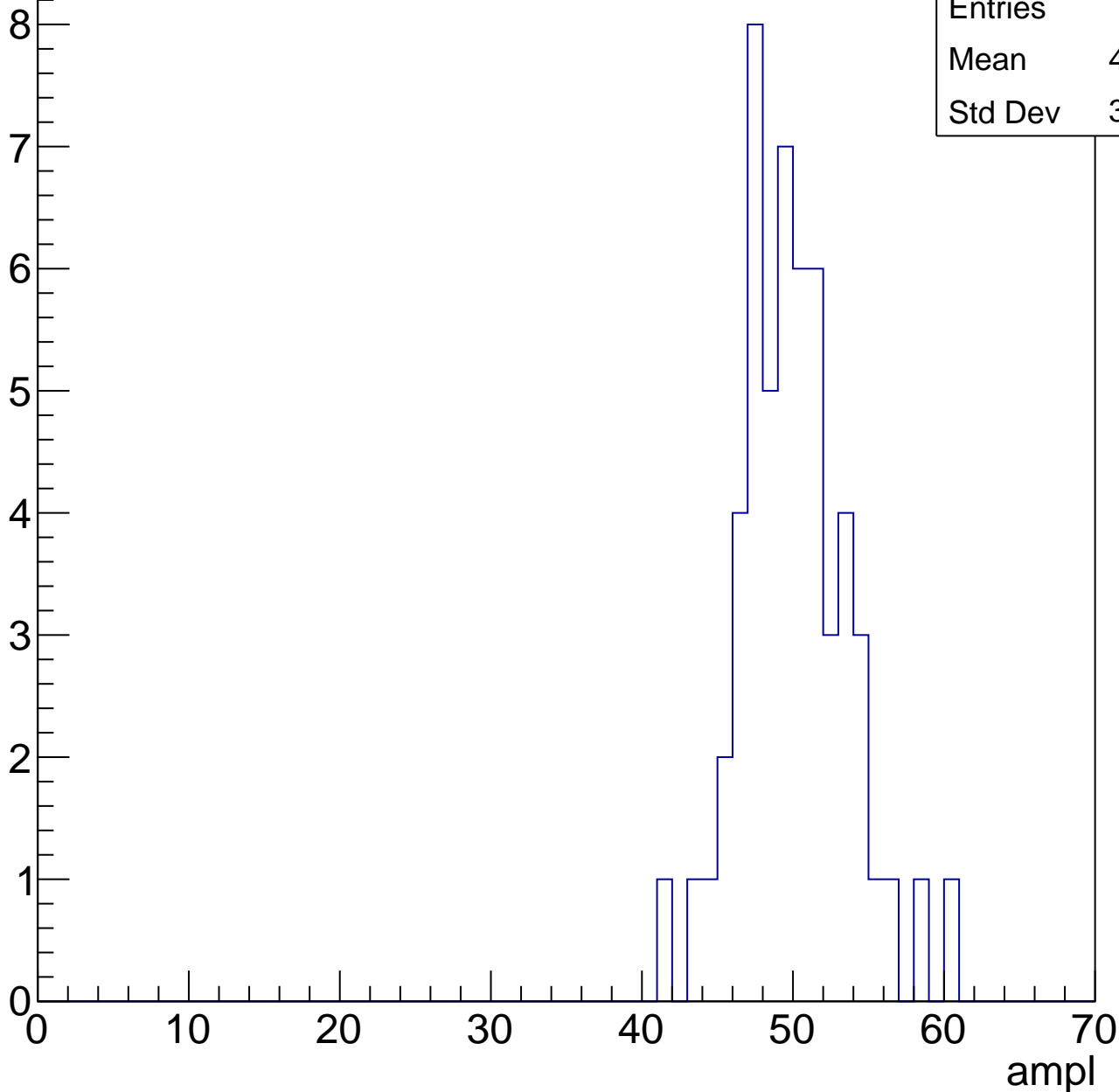


B1L103S, U12-ch102, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	49.56
Std Dev	3.556

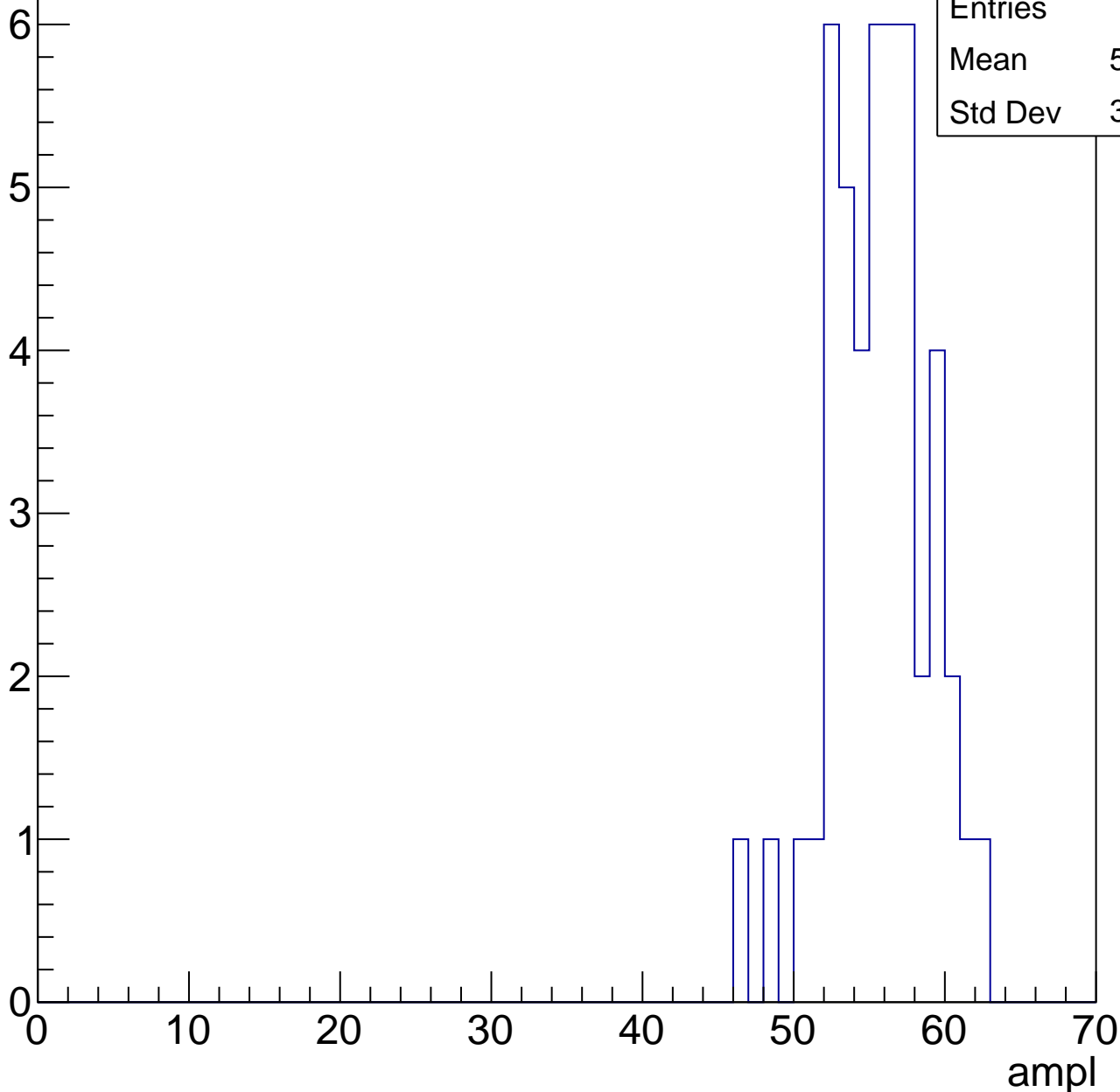


B1L103S, U12-ch102, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	47
Mean	55.13
Std Dev	3.246

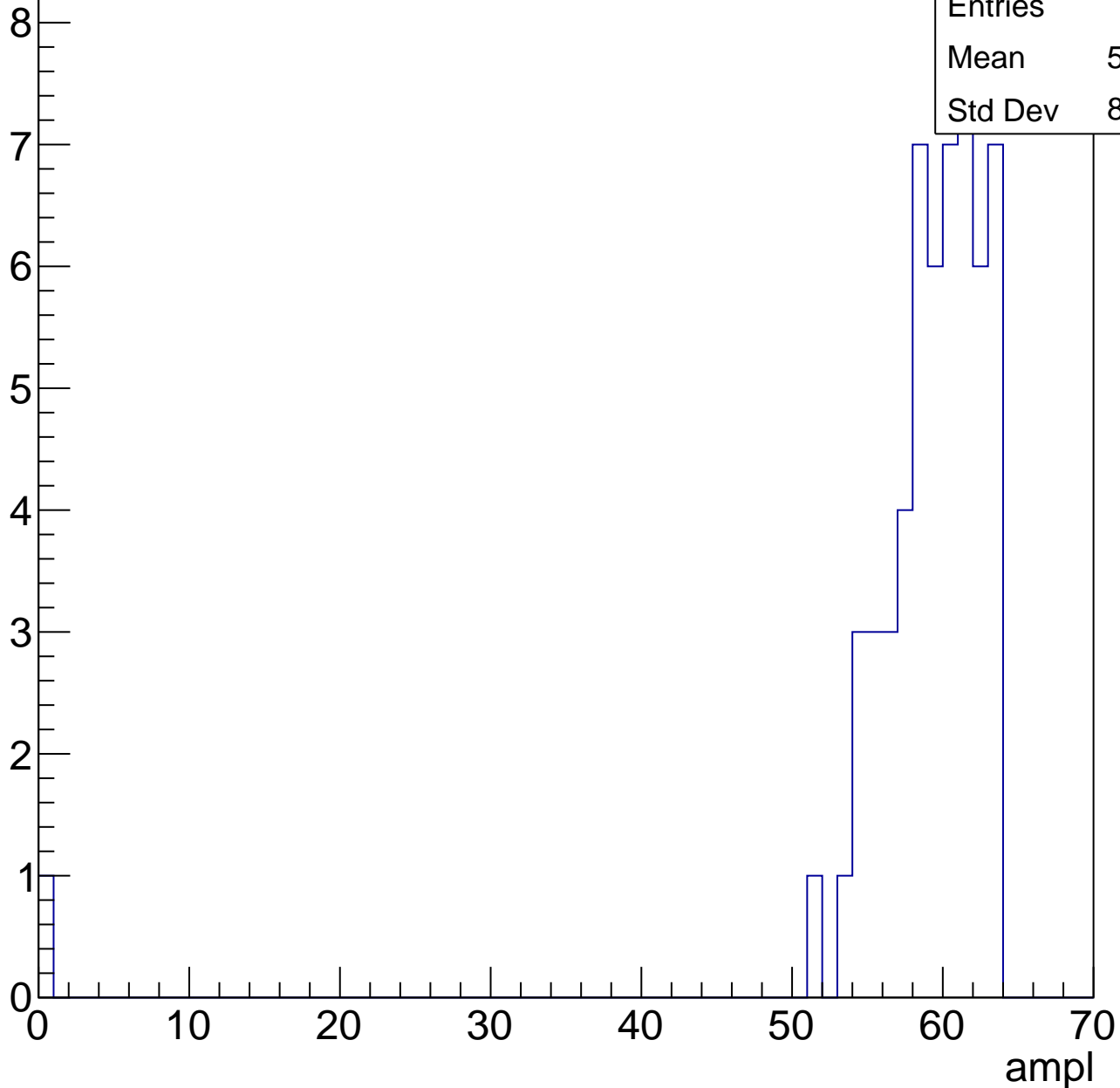


B1L103S, U12-ch102, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	57
Mean	58.04
Std Dev	8.278



B1L103S, U12-ch102, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch102, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	18
Mean	0
Std Dev	0

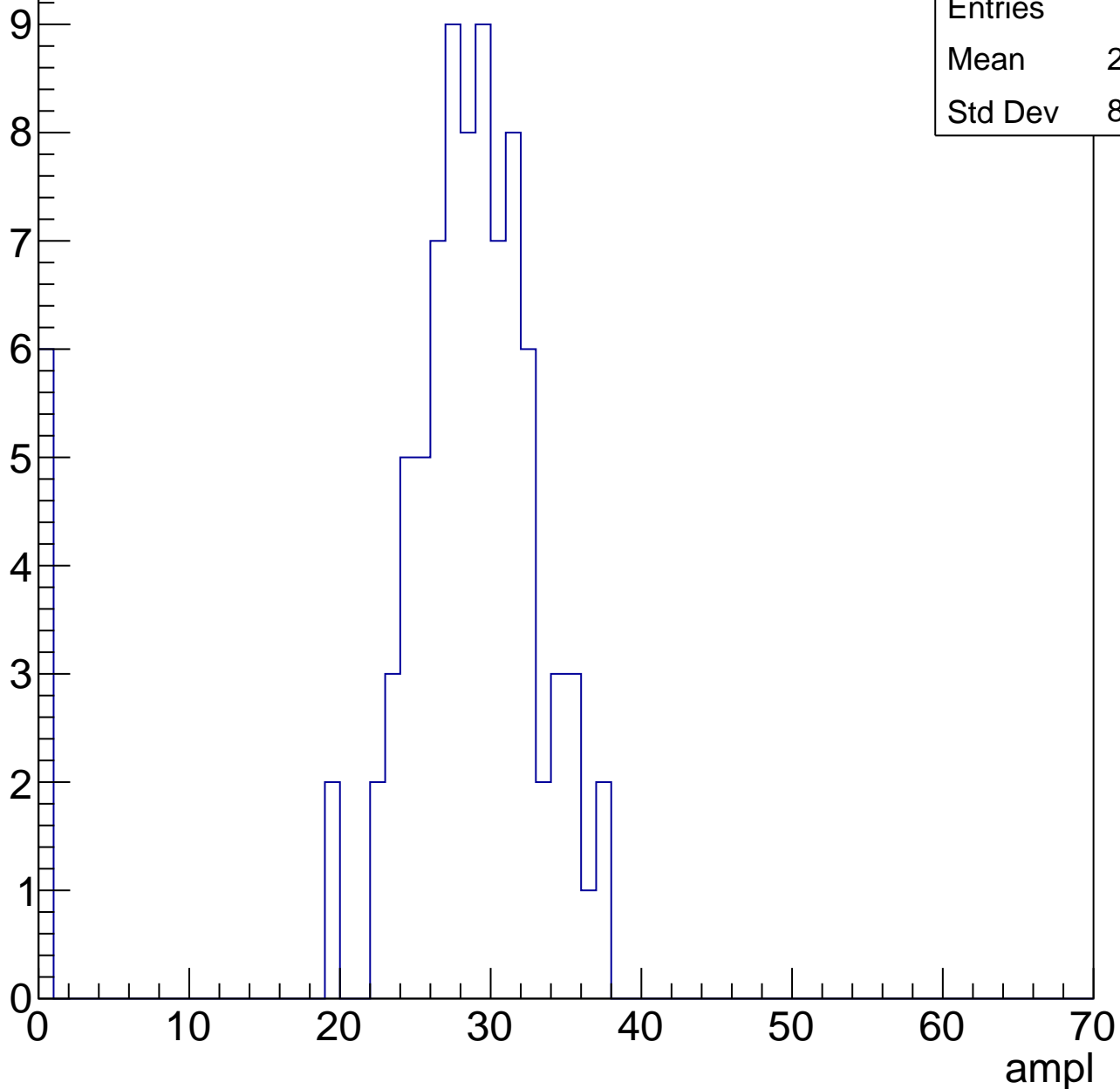
ampl

B1L103S, U12-ch103, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	88
Mean	26.58
Std Dev	8.072

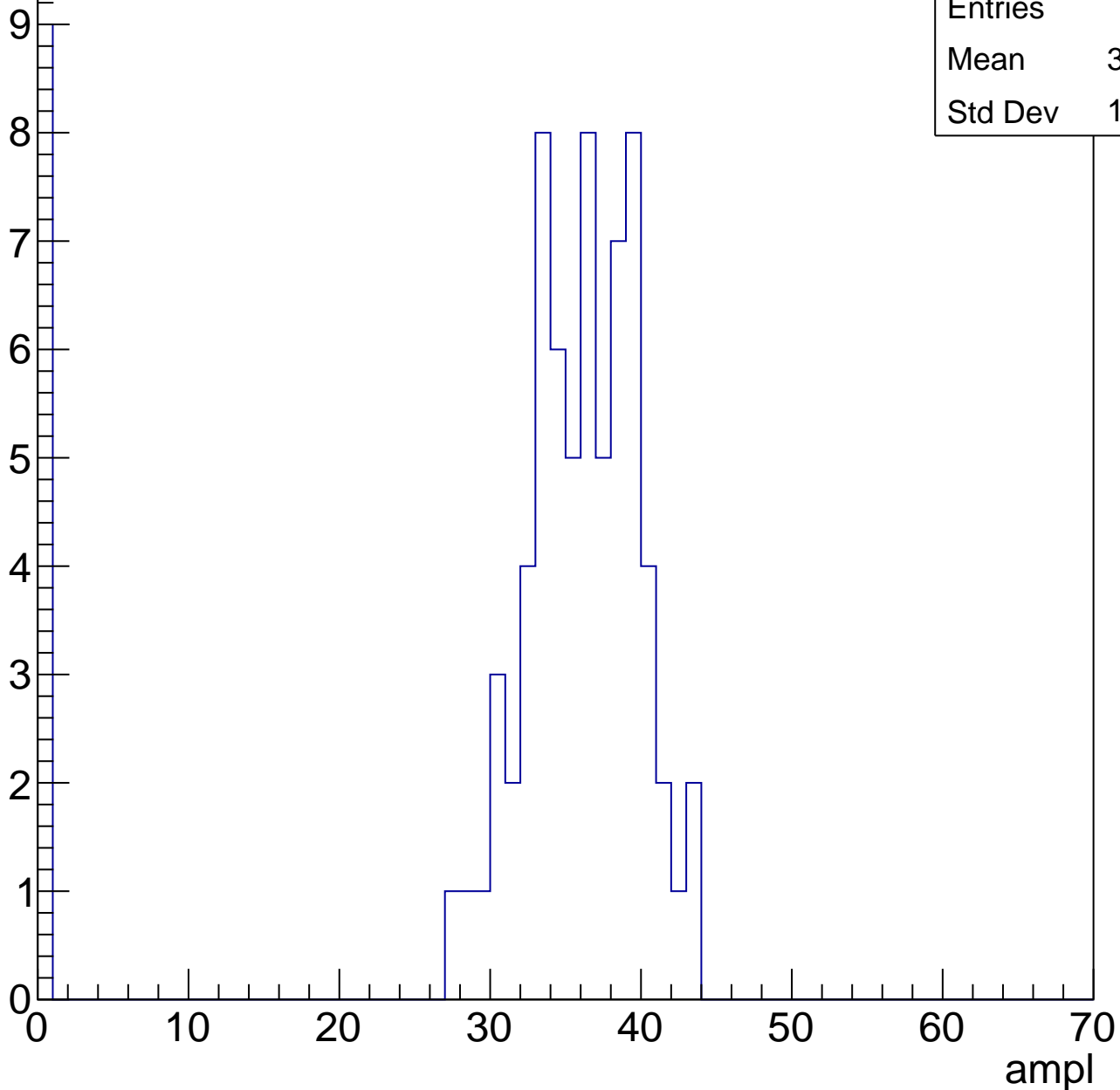


B1L103S, U12-ch103, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	77
Mean	31.53
Std Dev	11.95

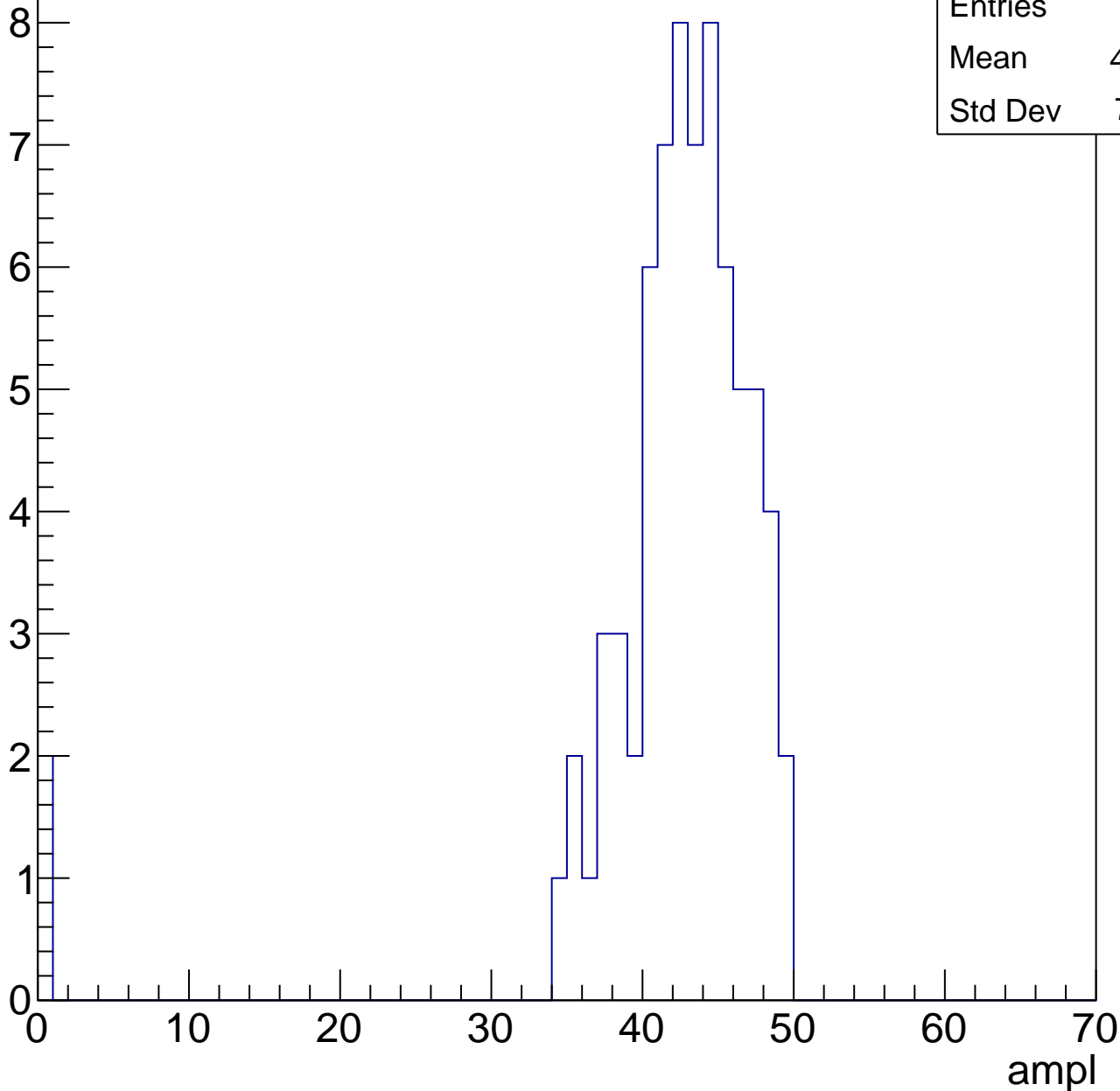


B1L103S, U12-ch103, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	72
Mean	41.44
Std Dev	7.831

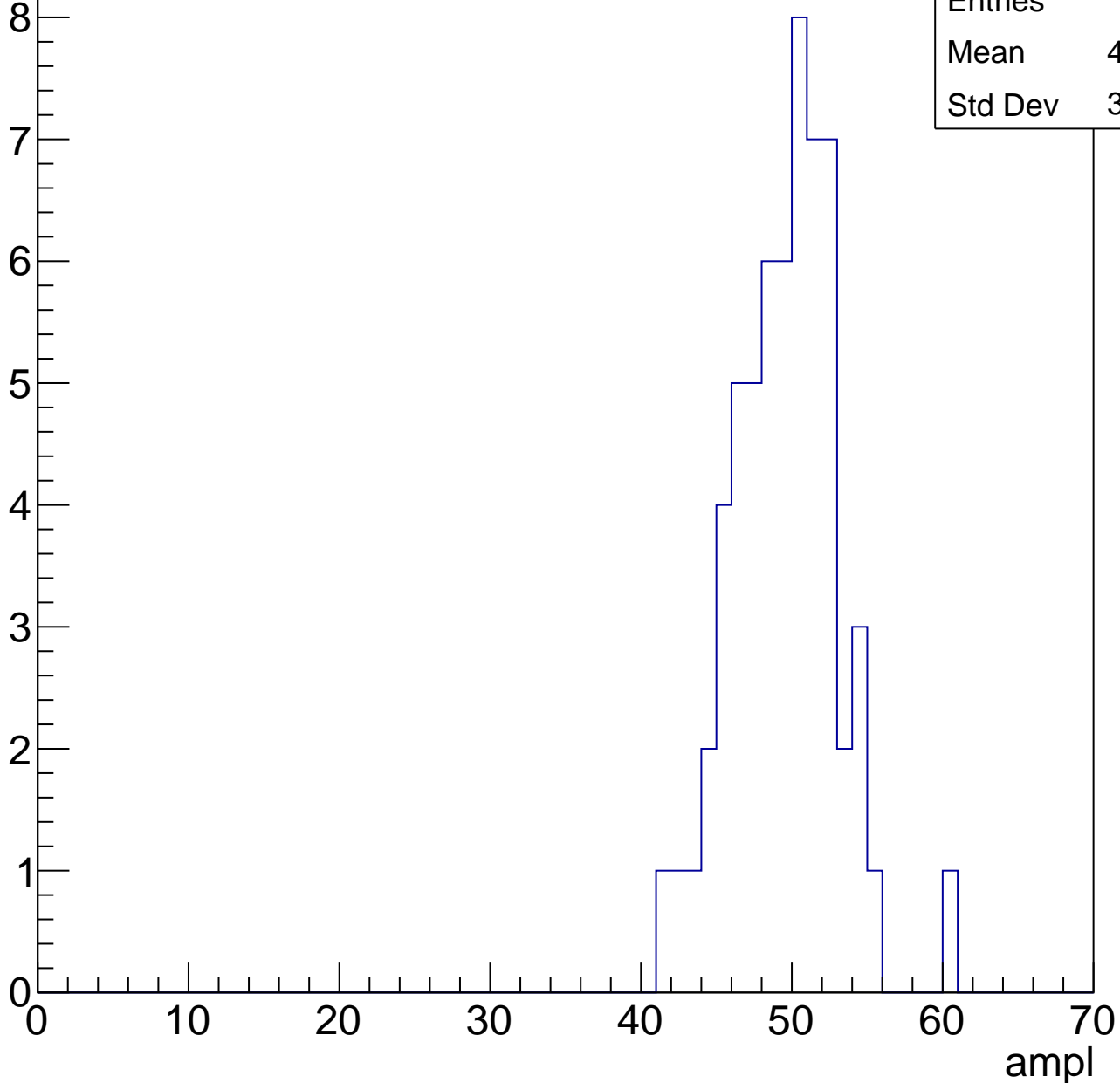


B1L103S, U12-ch103, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	49.08
Std Dev	3.407

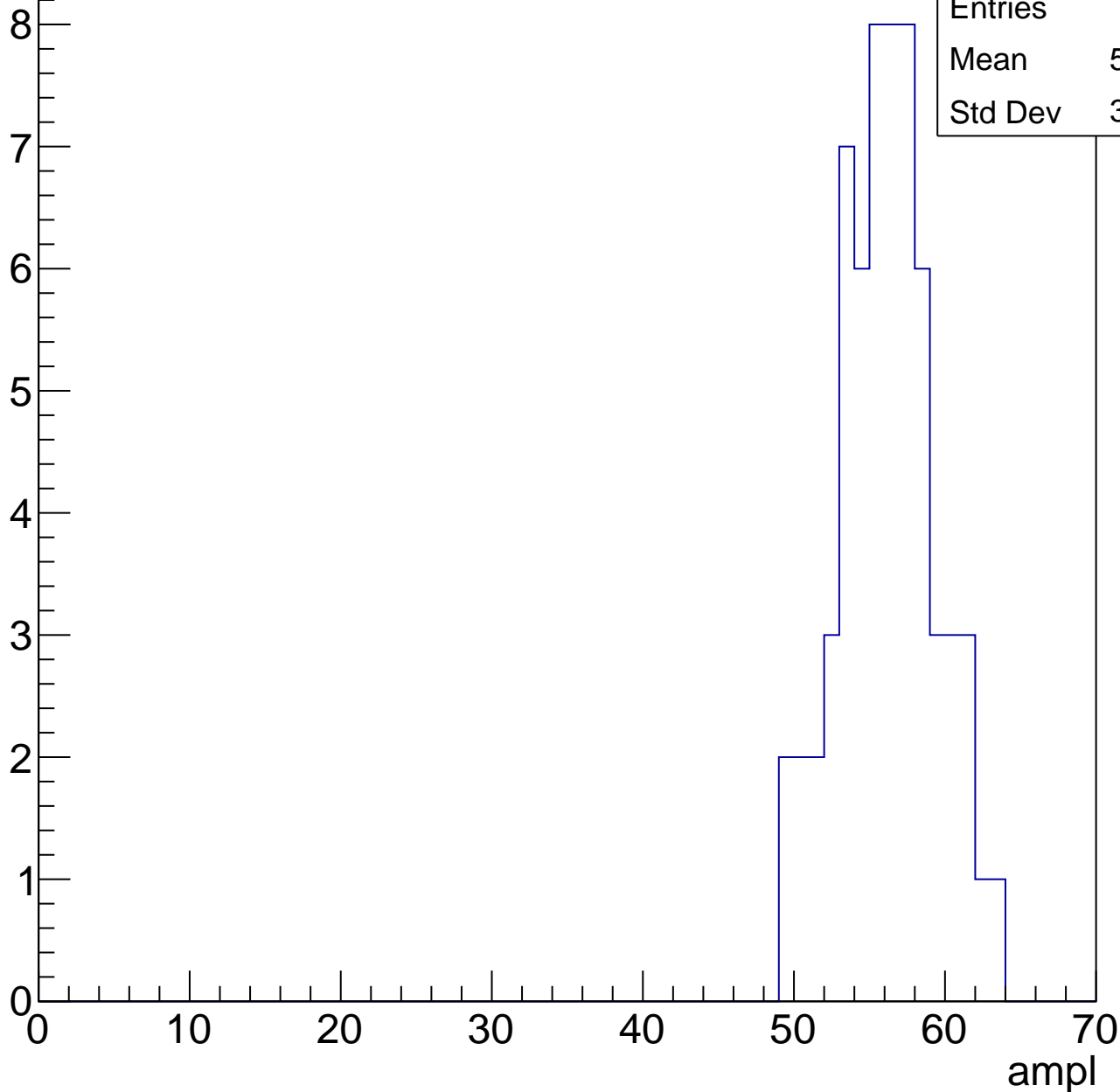


B1L103S, U12-ch103, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	63
Mean	55.68
Std Dev	3.146

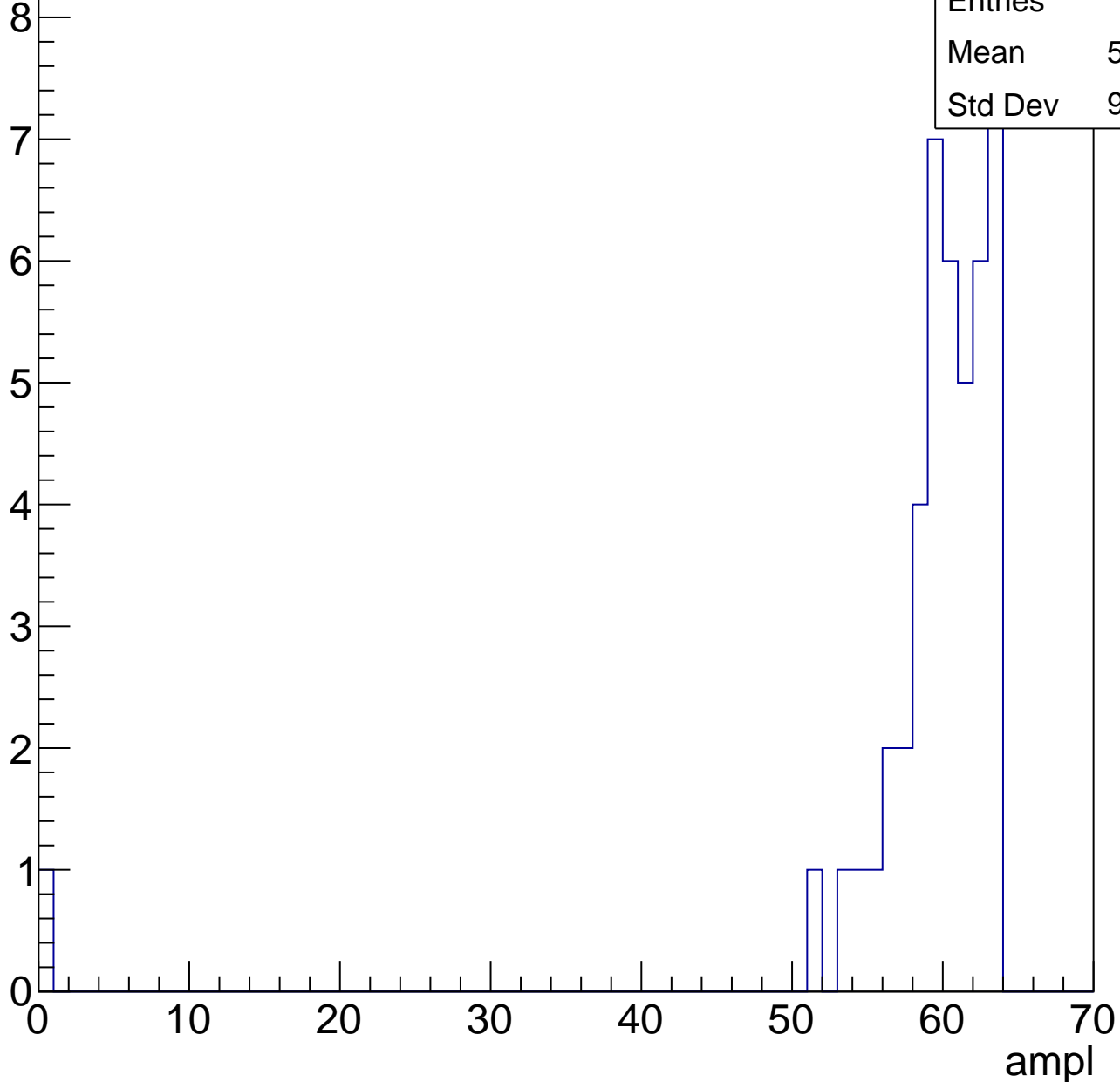


B1L103S, U12-ch103, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

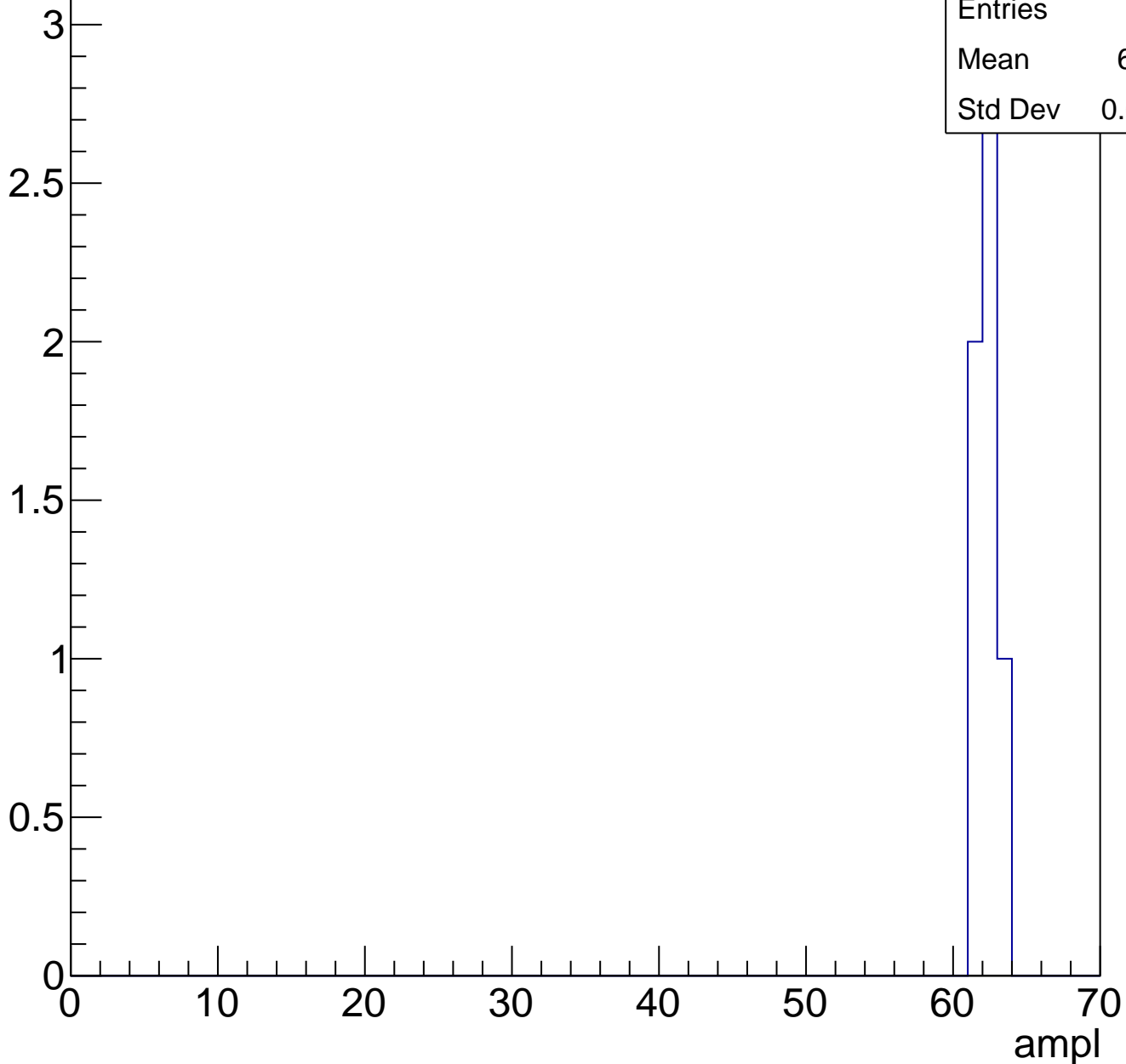
Entries	45
Mean	58.33
Std Dev	9.238



B1L103S, U12-ch103, adc6

calib_packv5_041523_1651.root, FC#0, port C2

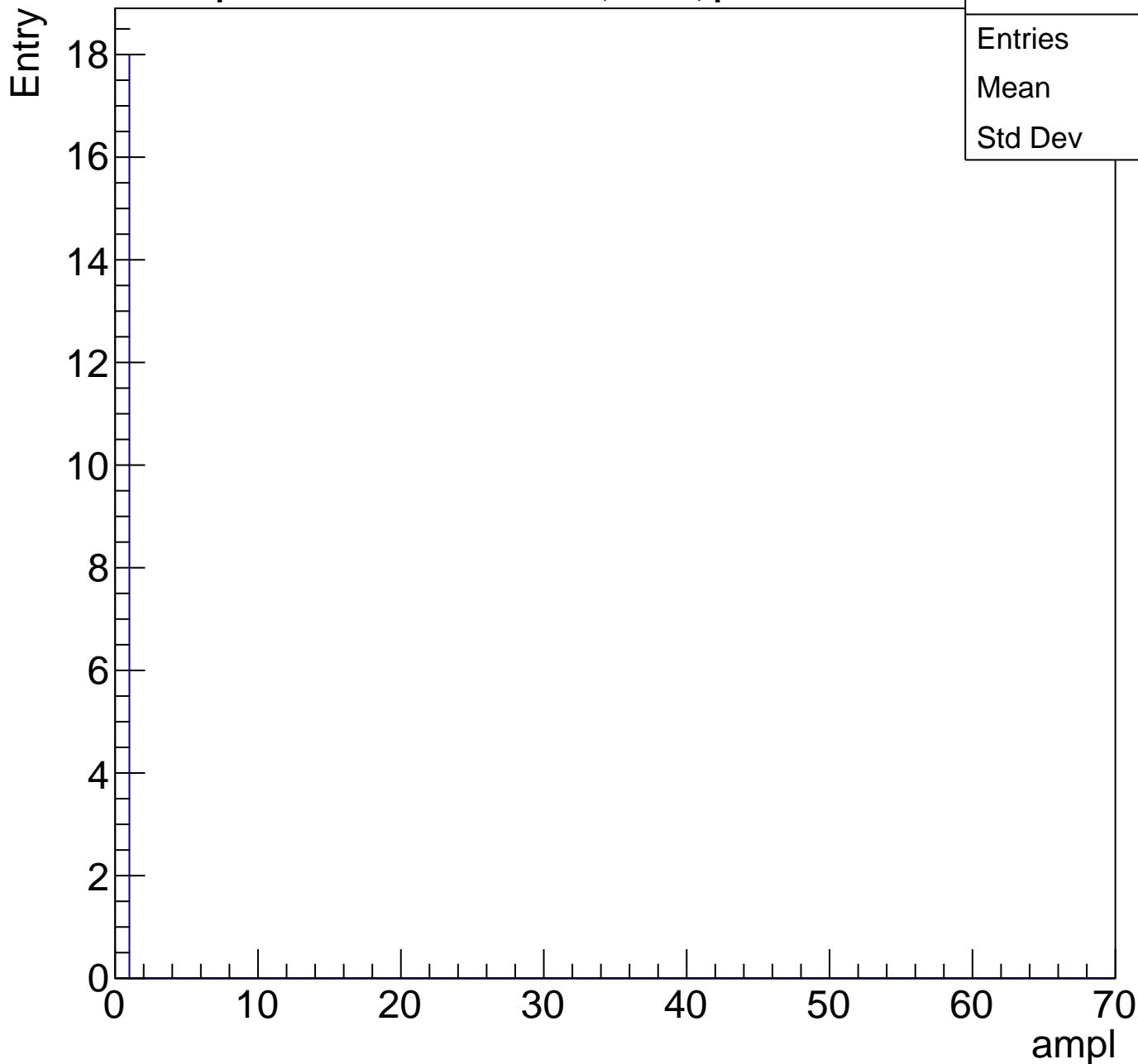
Entry



B1L103S, U12-ch103, adc7

calib_packv5_041523_1651.root, FC#0, port C2

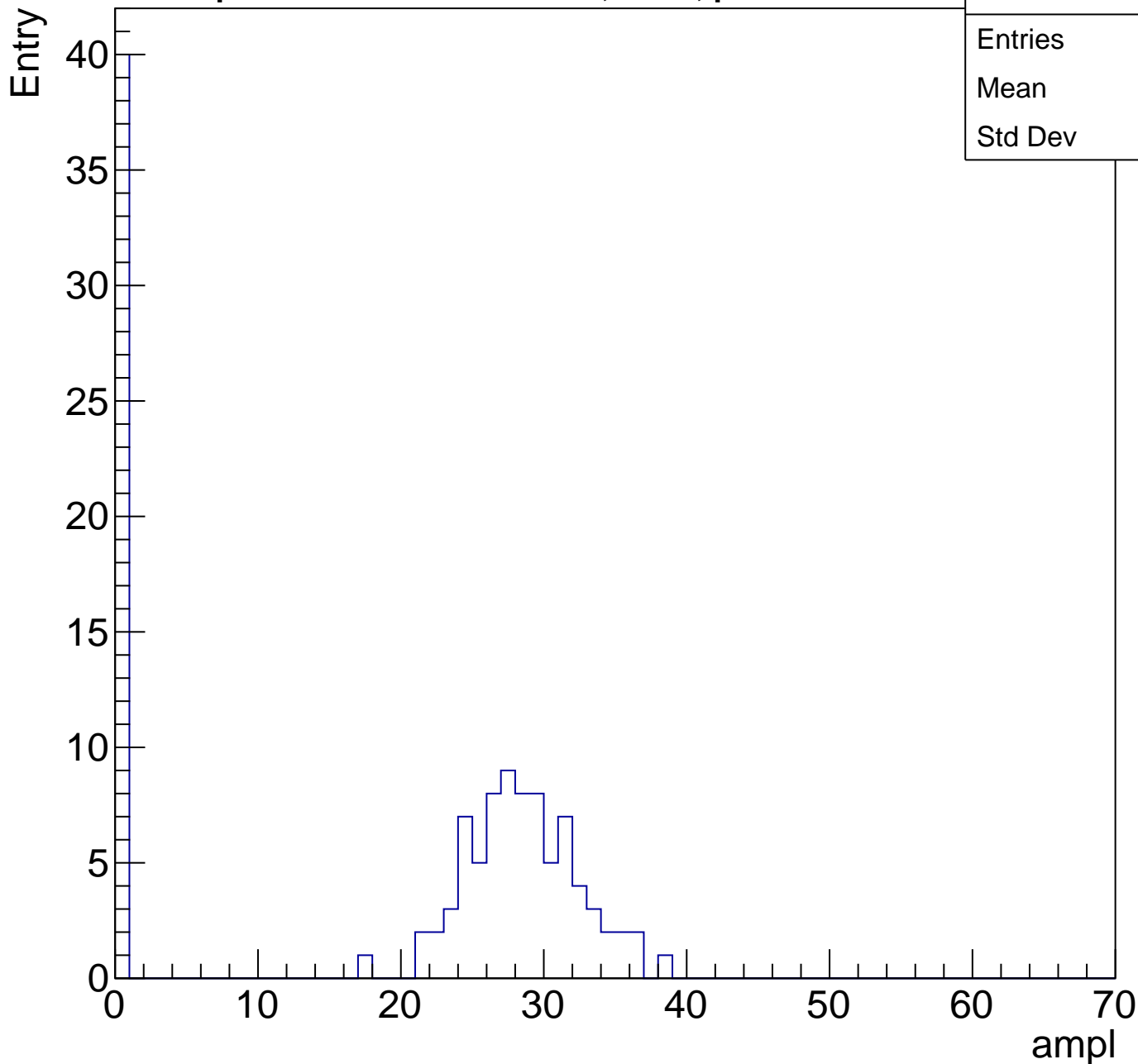
Entries	18
Mean	0
Std Dev	0



B1L103S, U12-ch104, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	119
Mean	18.61
Std Dev	13.61

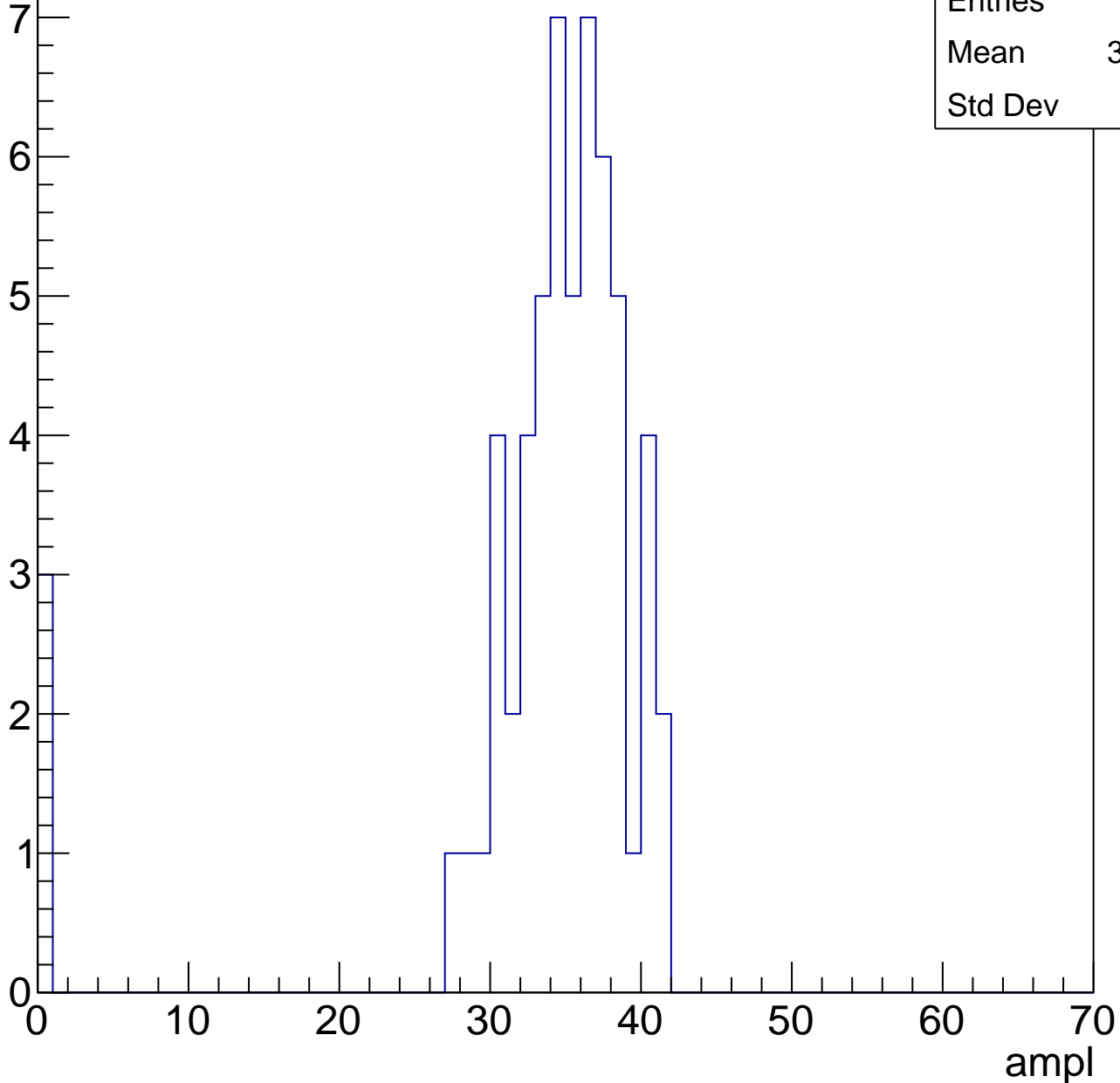


B1L103S, U12-ch104, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	33.05
Std Dev	8.37

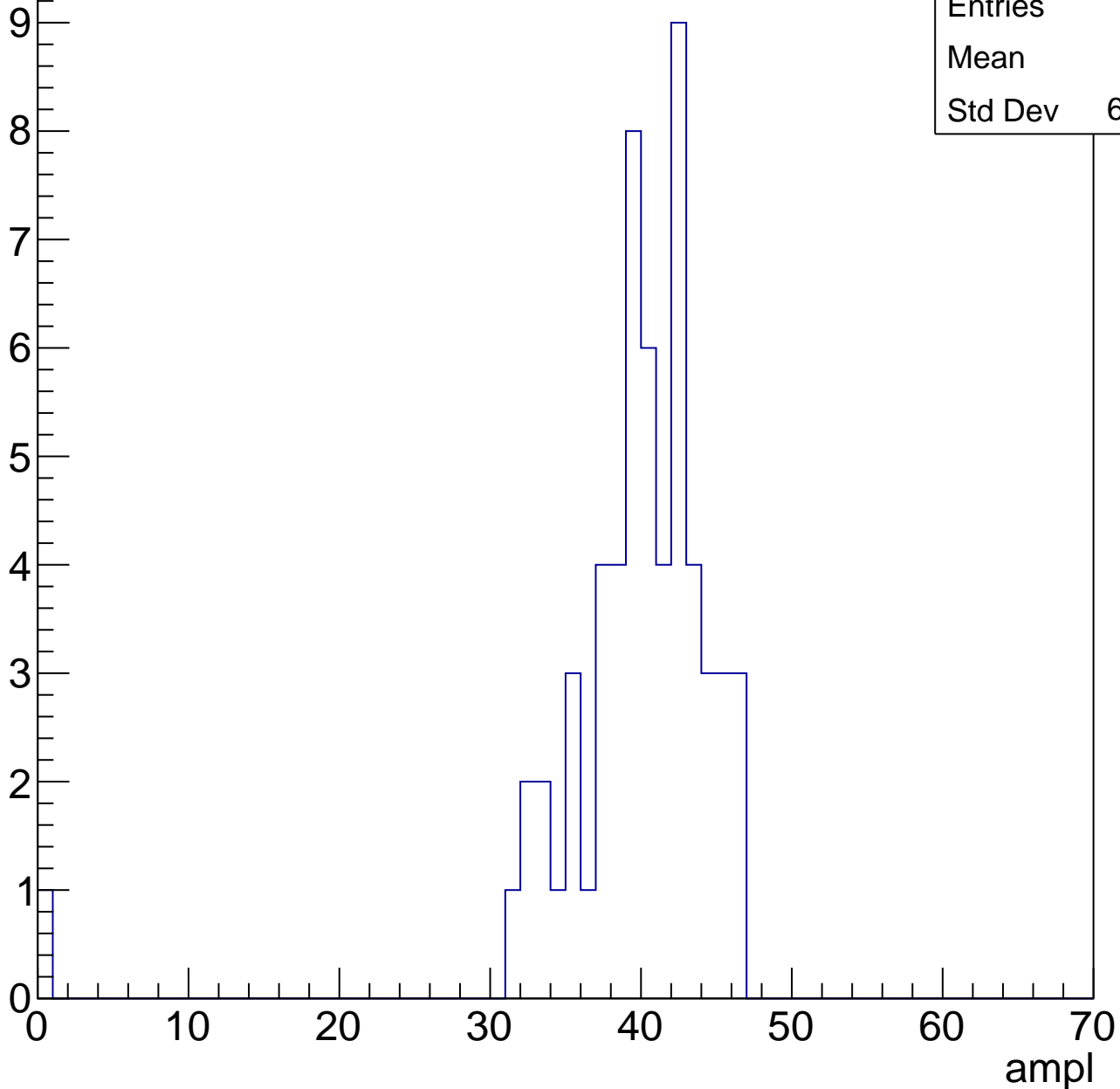


B1L103S, U12-ch104, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	39.1
Std Dev	6.316

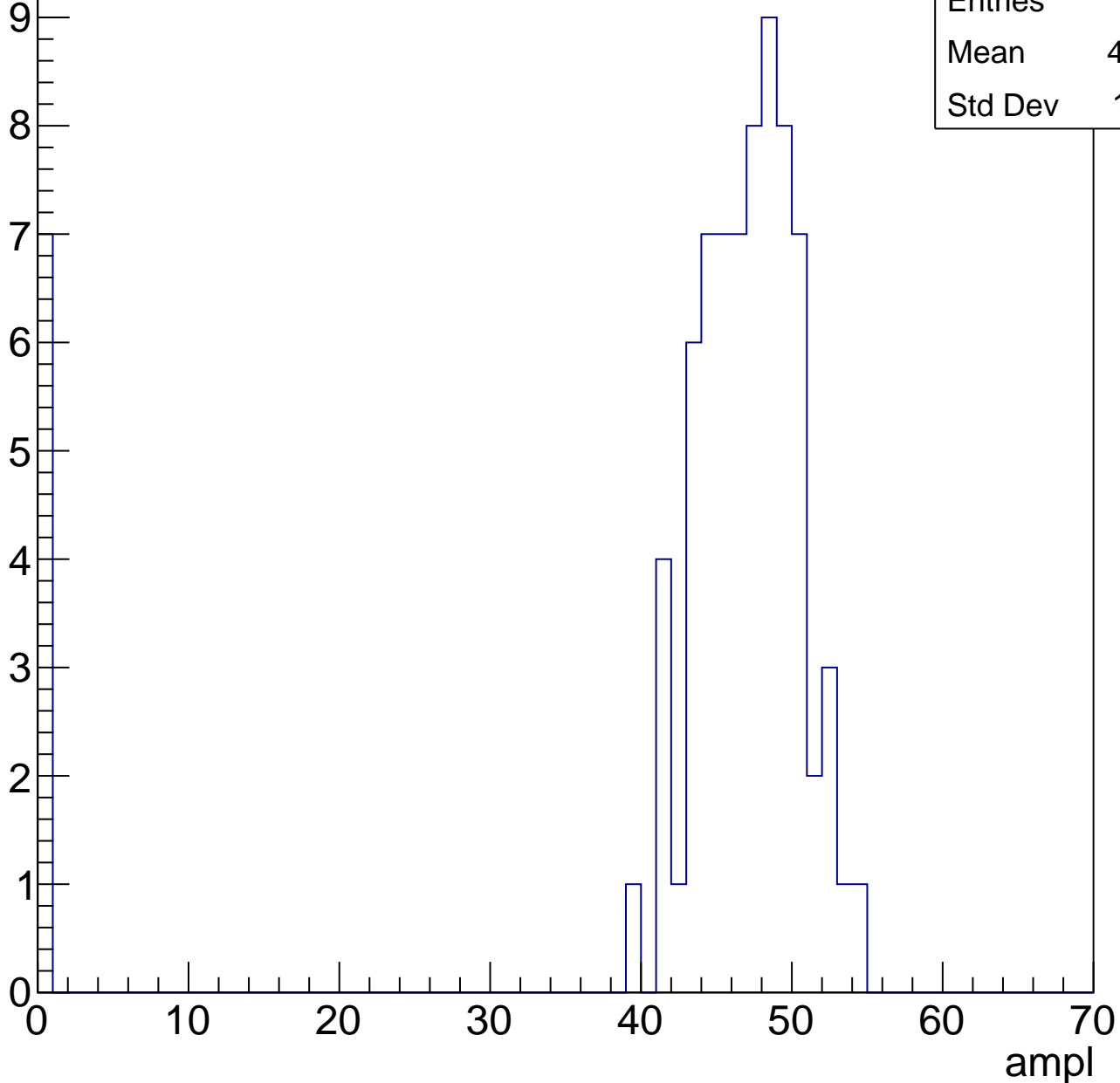


B1L103S, U12-ch104, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	79
Mean	42.57
Std Dev	13.61

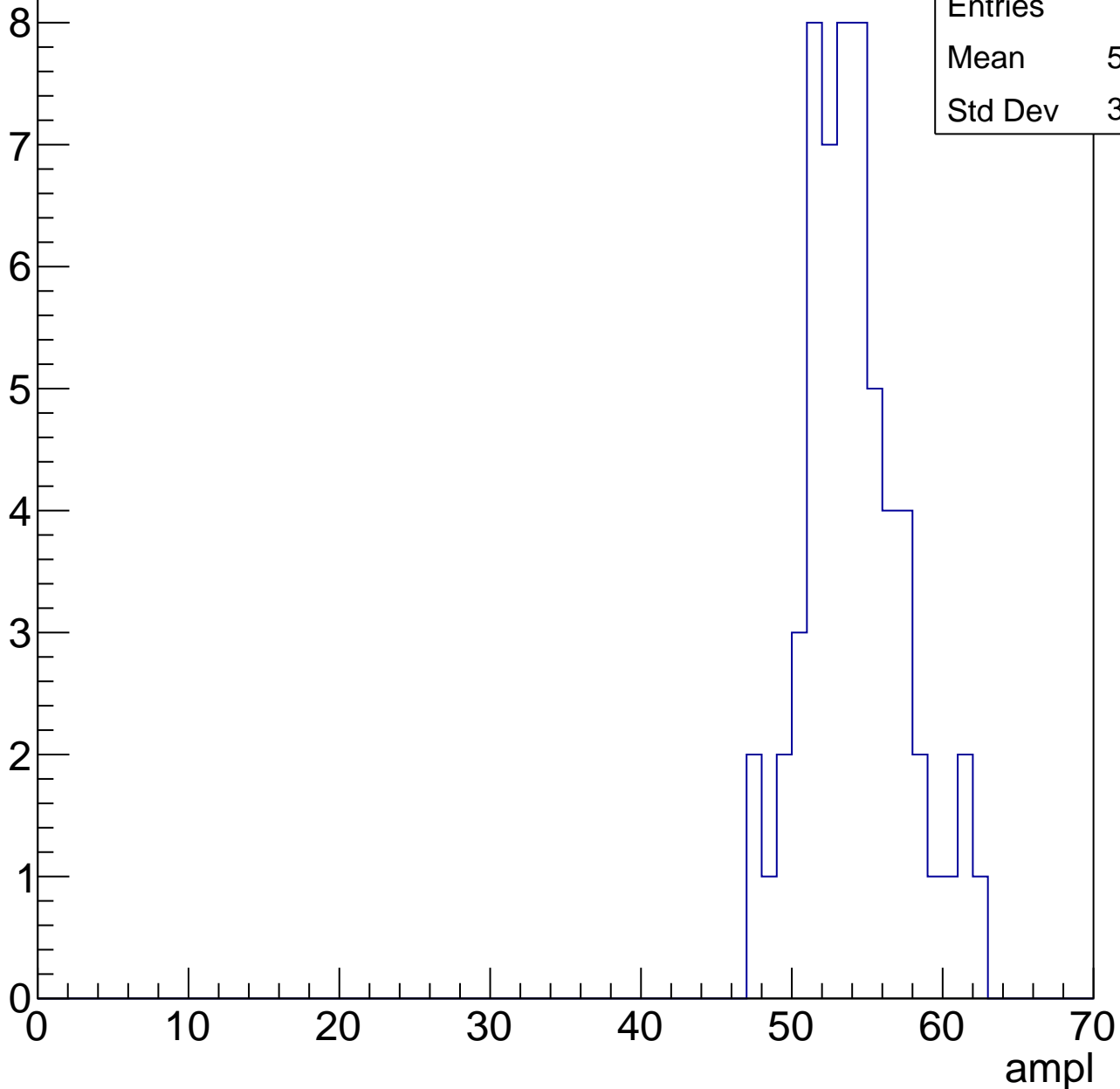


B1L103S, U12-ch104, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	53.63
Std Dev	3.303

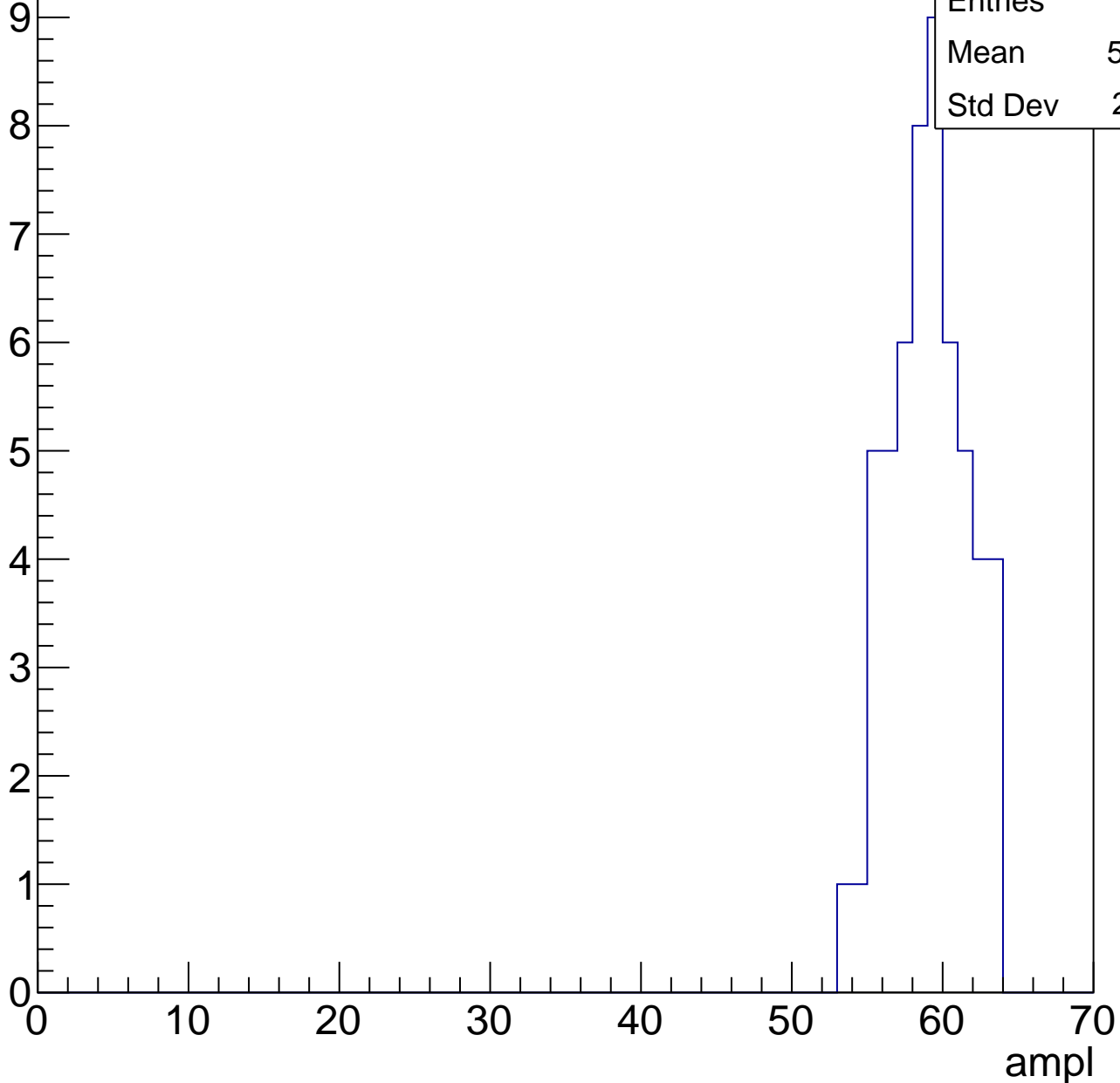


B1L103S, U12-ch104, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	54
Mean	58.59
Std Dev	2.491

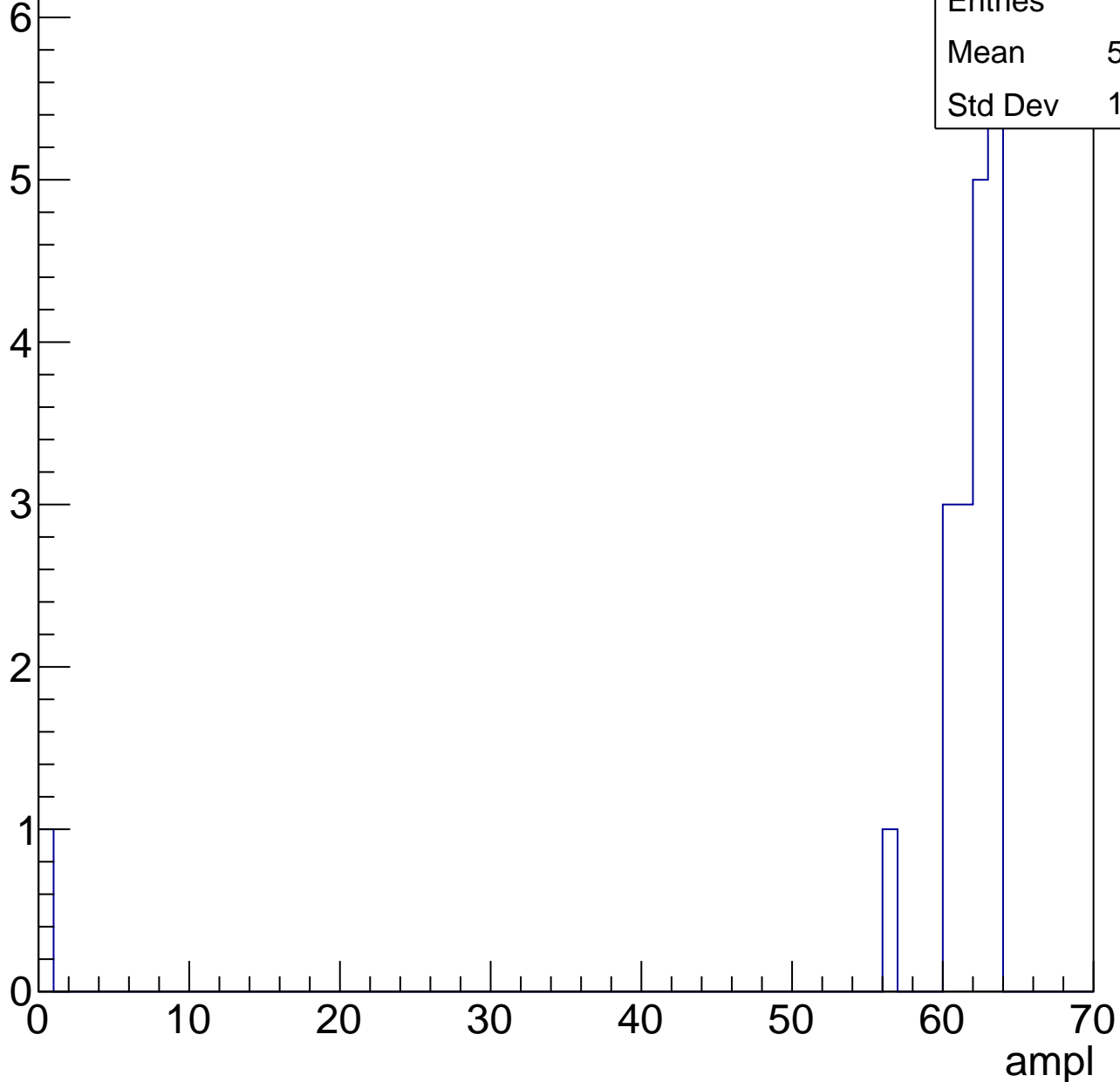


B1L103S, U12-ch104, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	19
Mean	58.26
Std Dev	13.83



B1L103S, U12-ch104, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

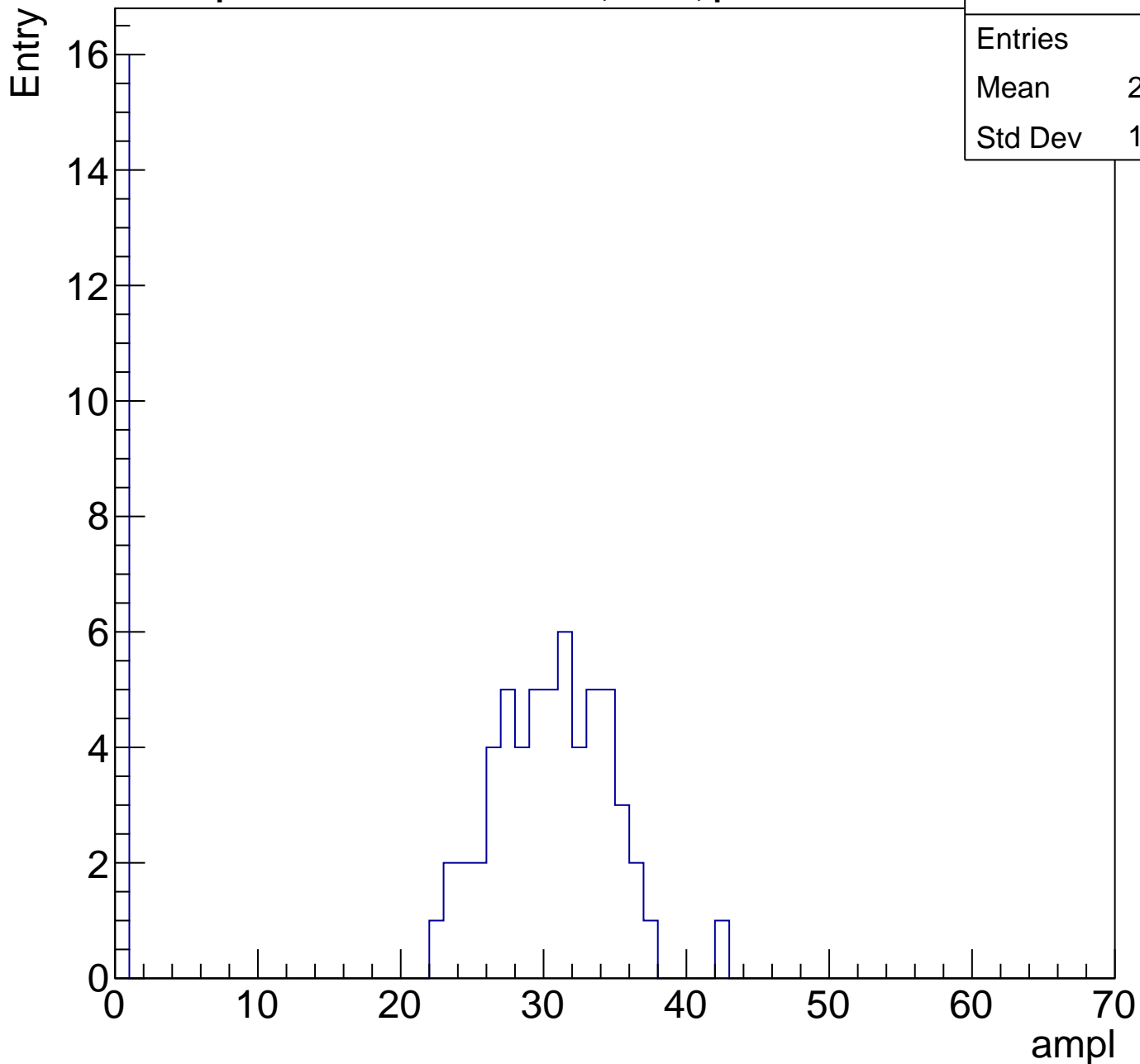
Entries	19
Mean	0
Std Dev	0

ampl

B1L103S, U12-ch105, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	73
Mean	23.52
Std Dev	12.95

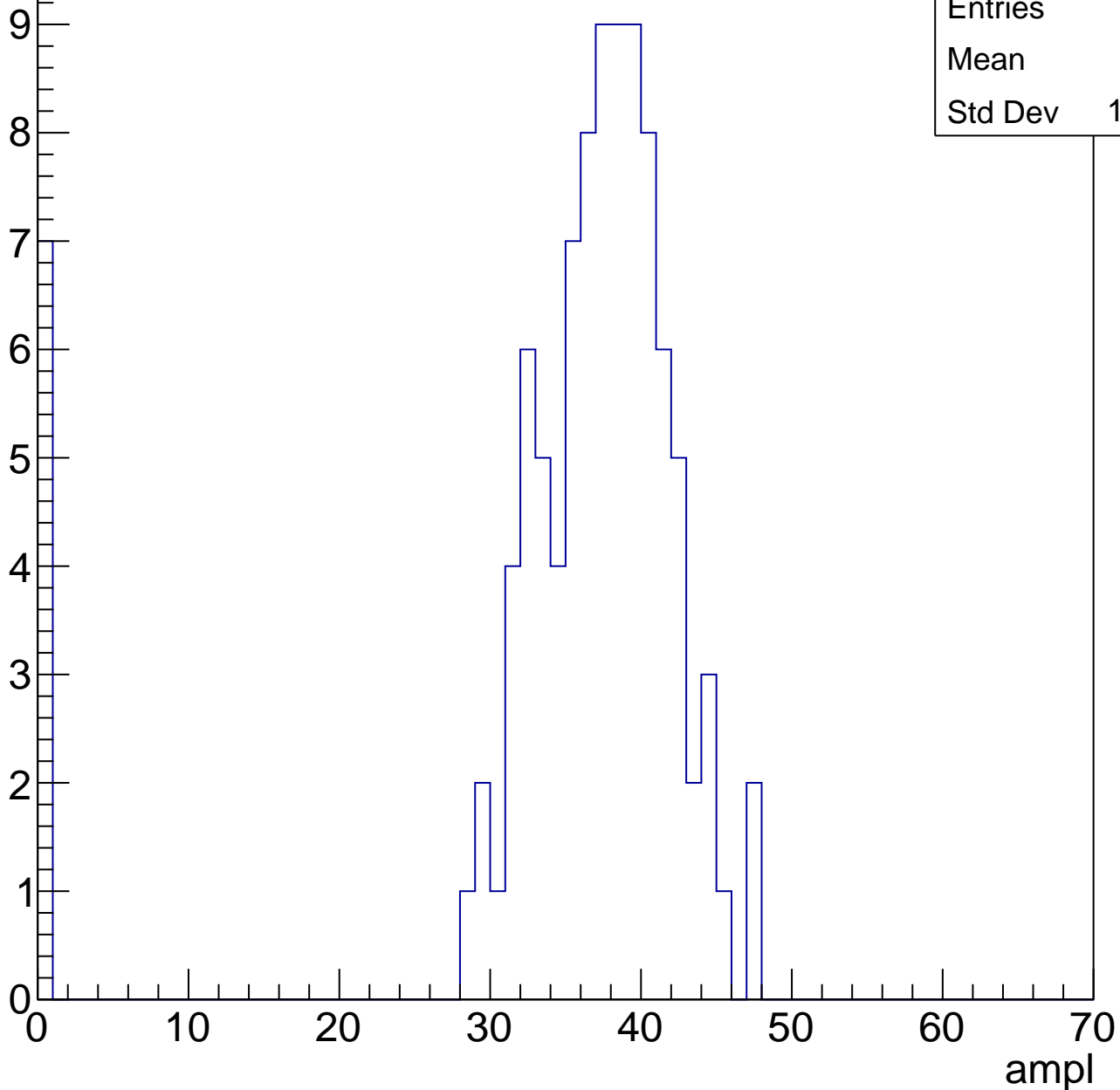


B1L103S, U12-ch105, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	99
Mean	34.6
Std Dev	10.32

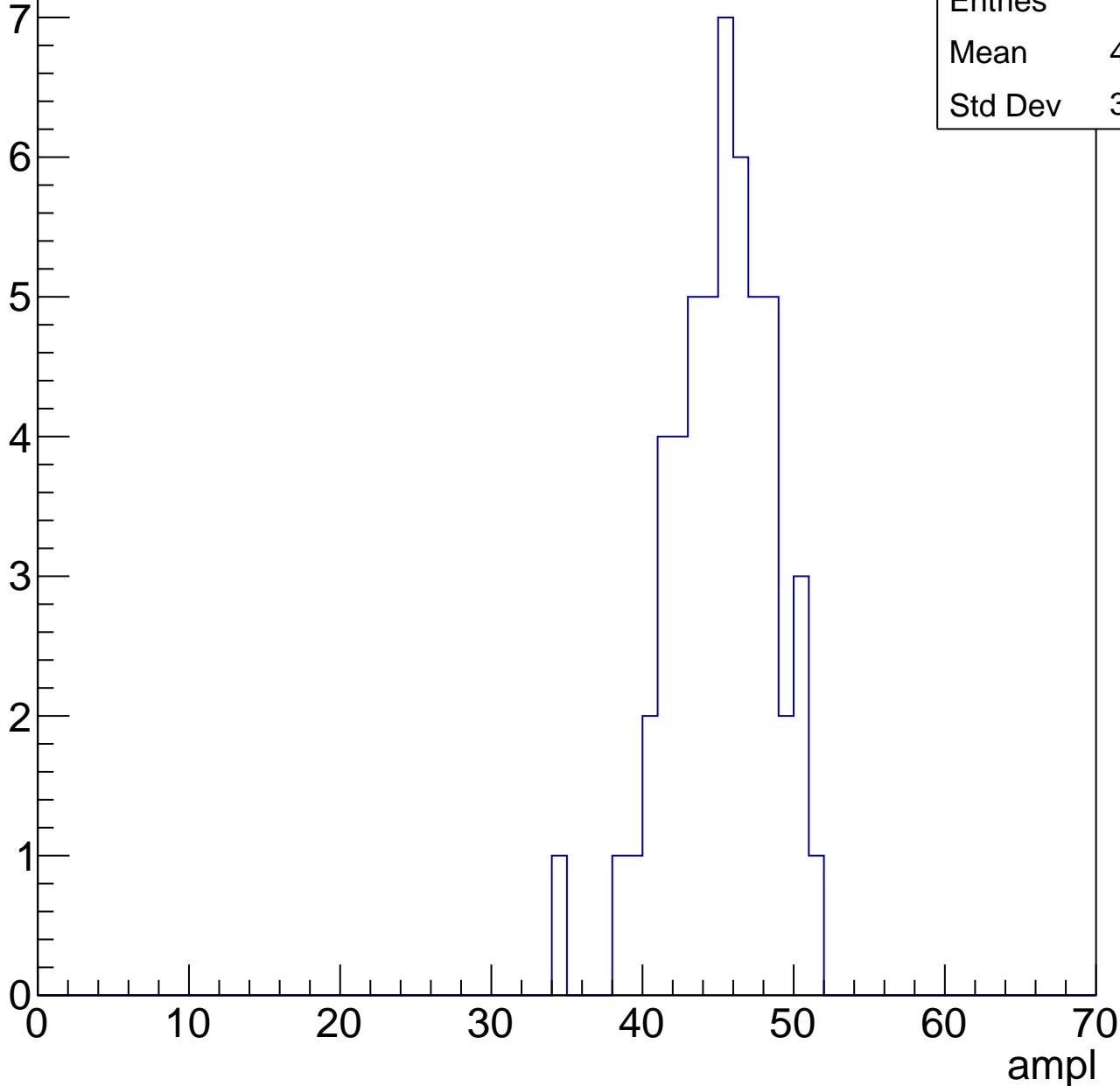


B1L103S, U12-ch105, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	52
Mean	44.67
Std Dev	3.367

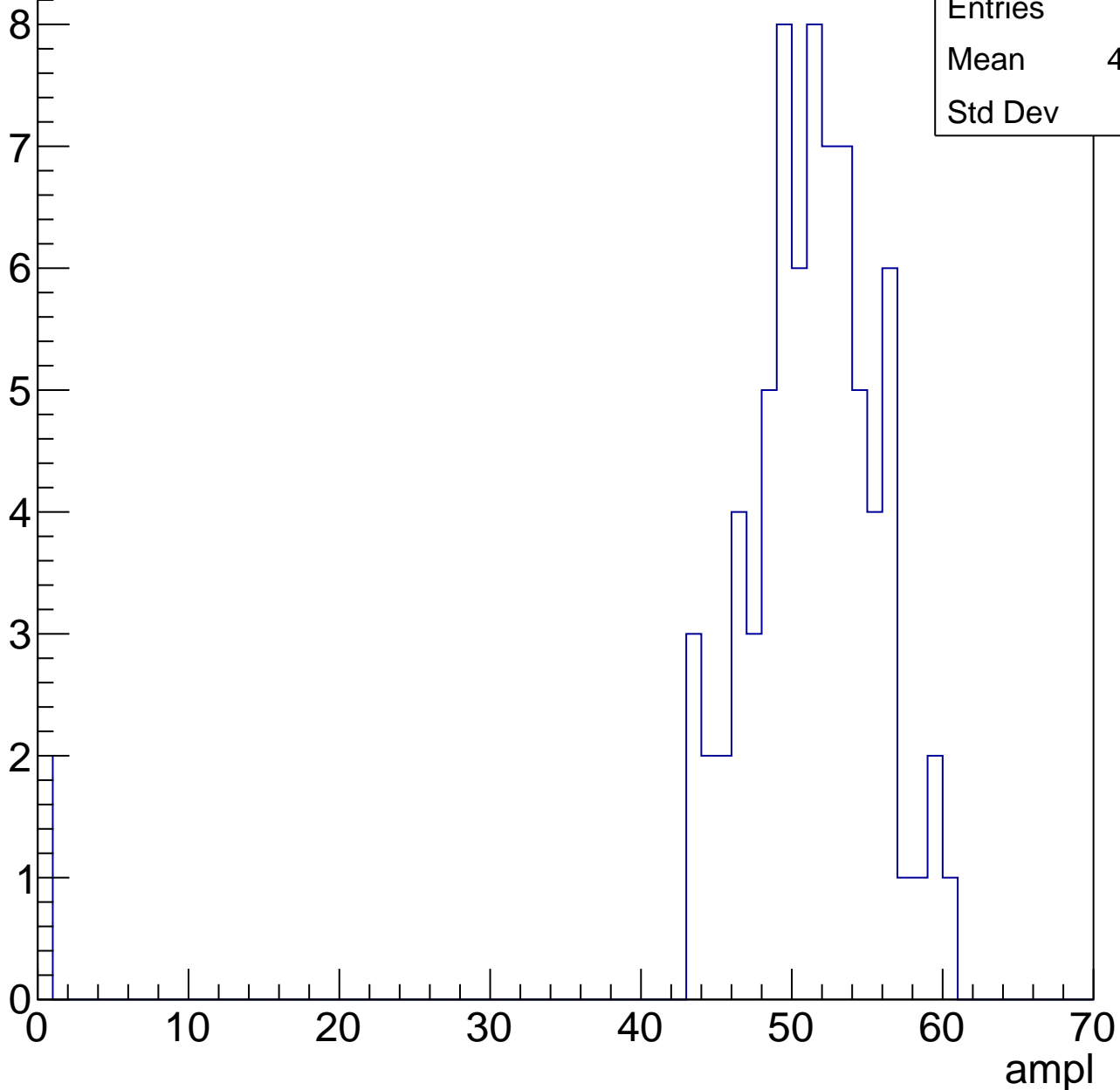


B1L103S, U12-ch105, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	77
Mean	49.69
Std Dev	9.01

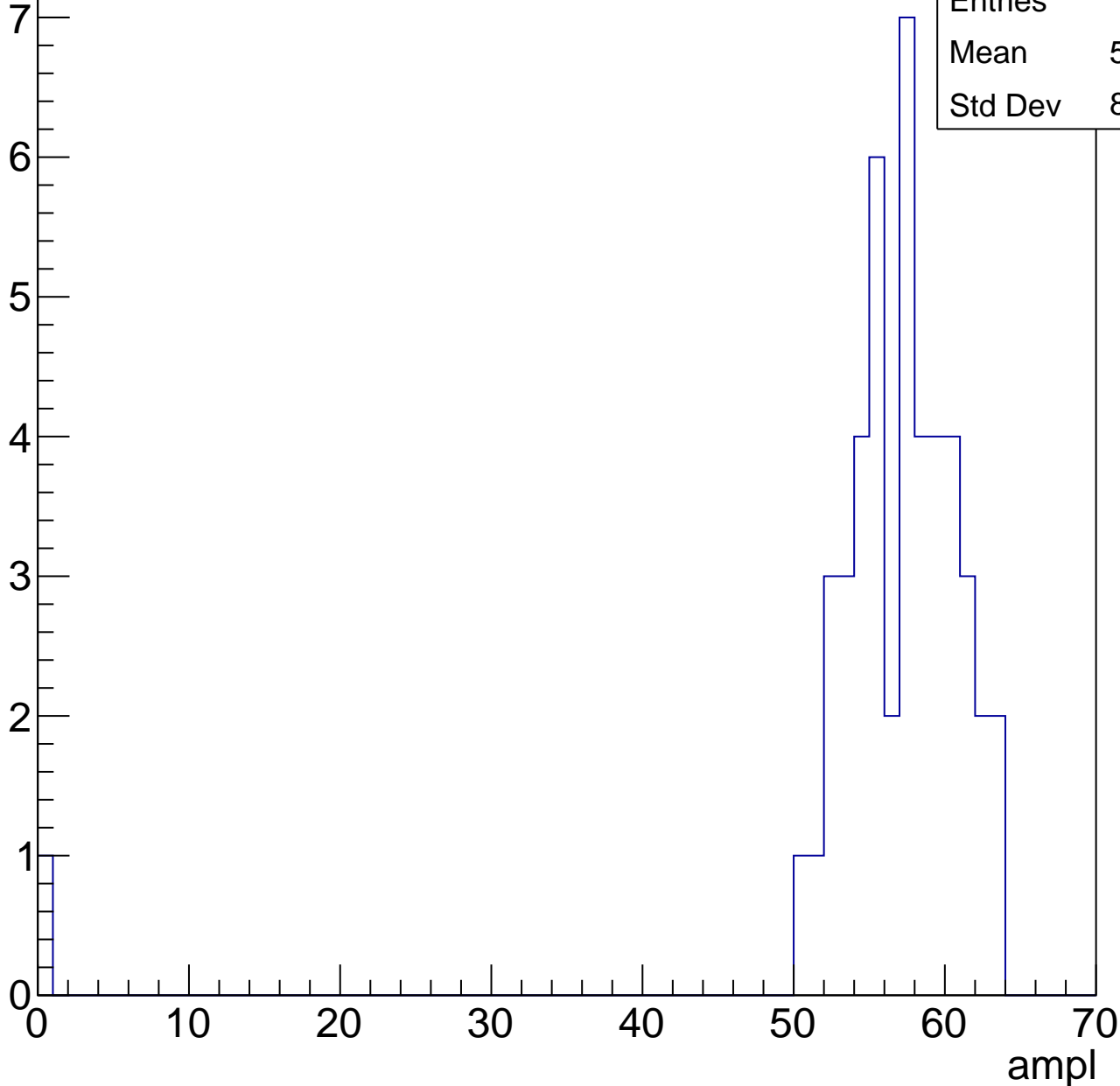


B1L103S, U12-ch105, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	47
Mean	55.62
Std Dev	8.819

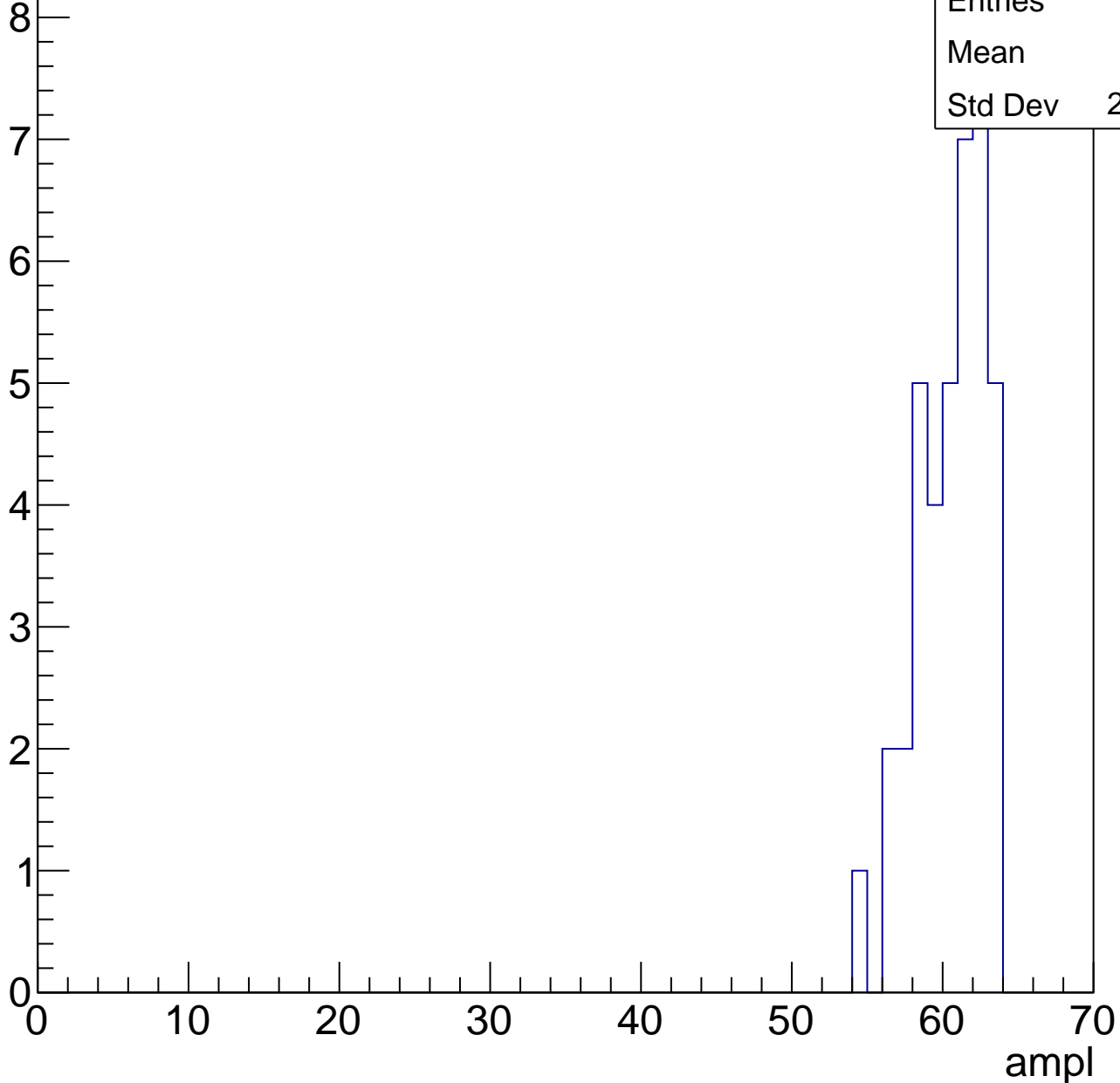


B1L103S, U12-ch105, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	39
Mean	60.1
Std Dev	2.228



B1L103S, U12-ch105, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch105, adc7

calib_packv5_041523_1651.root, FC#0, port C2

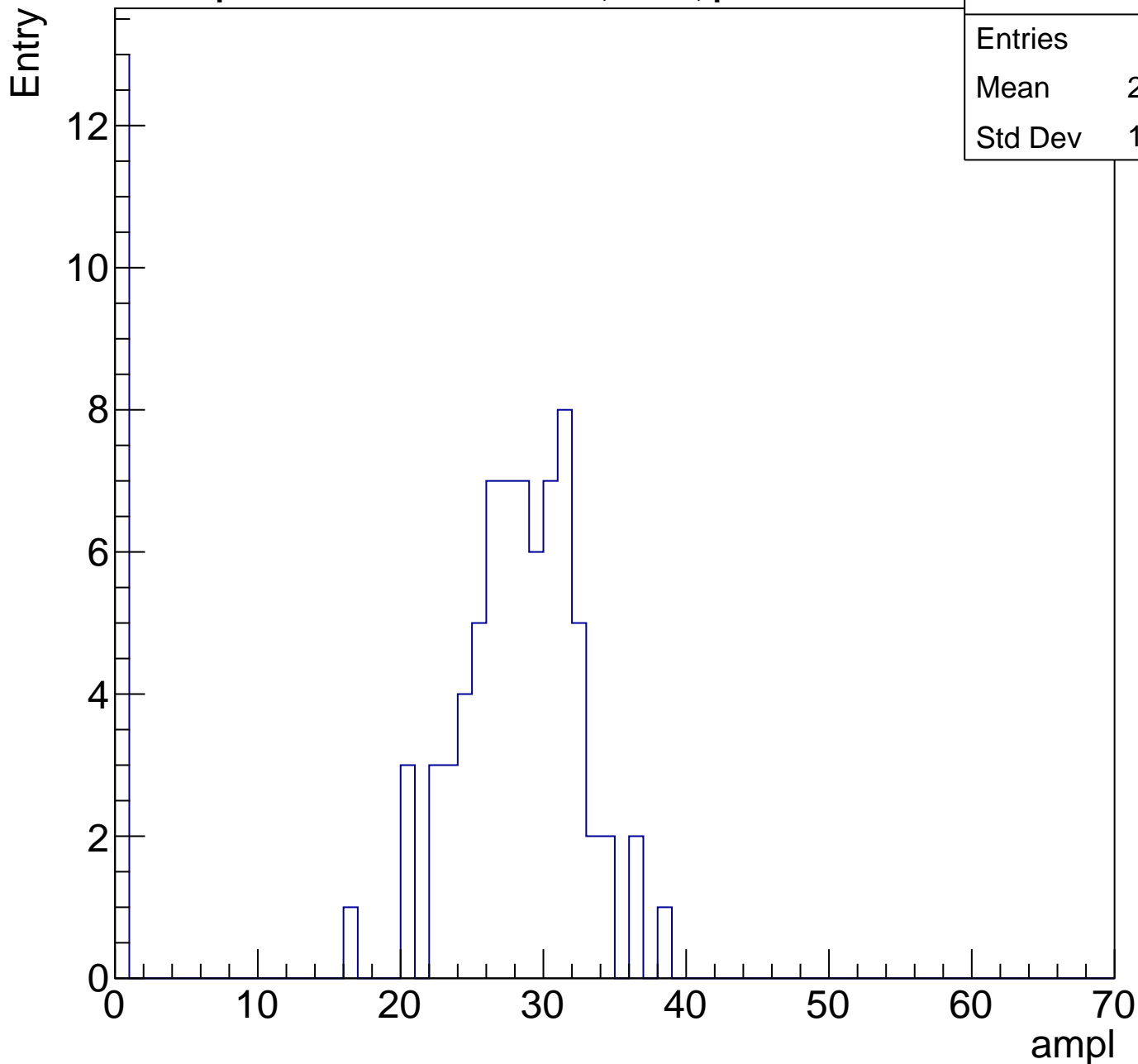
Entries	19
Mean	0
Std Dev	0



B1L103S, U12-ch106, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	86
Mean	23.66
Std Dev	10.66



B1L103S, U12-ch106, adc1

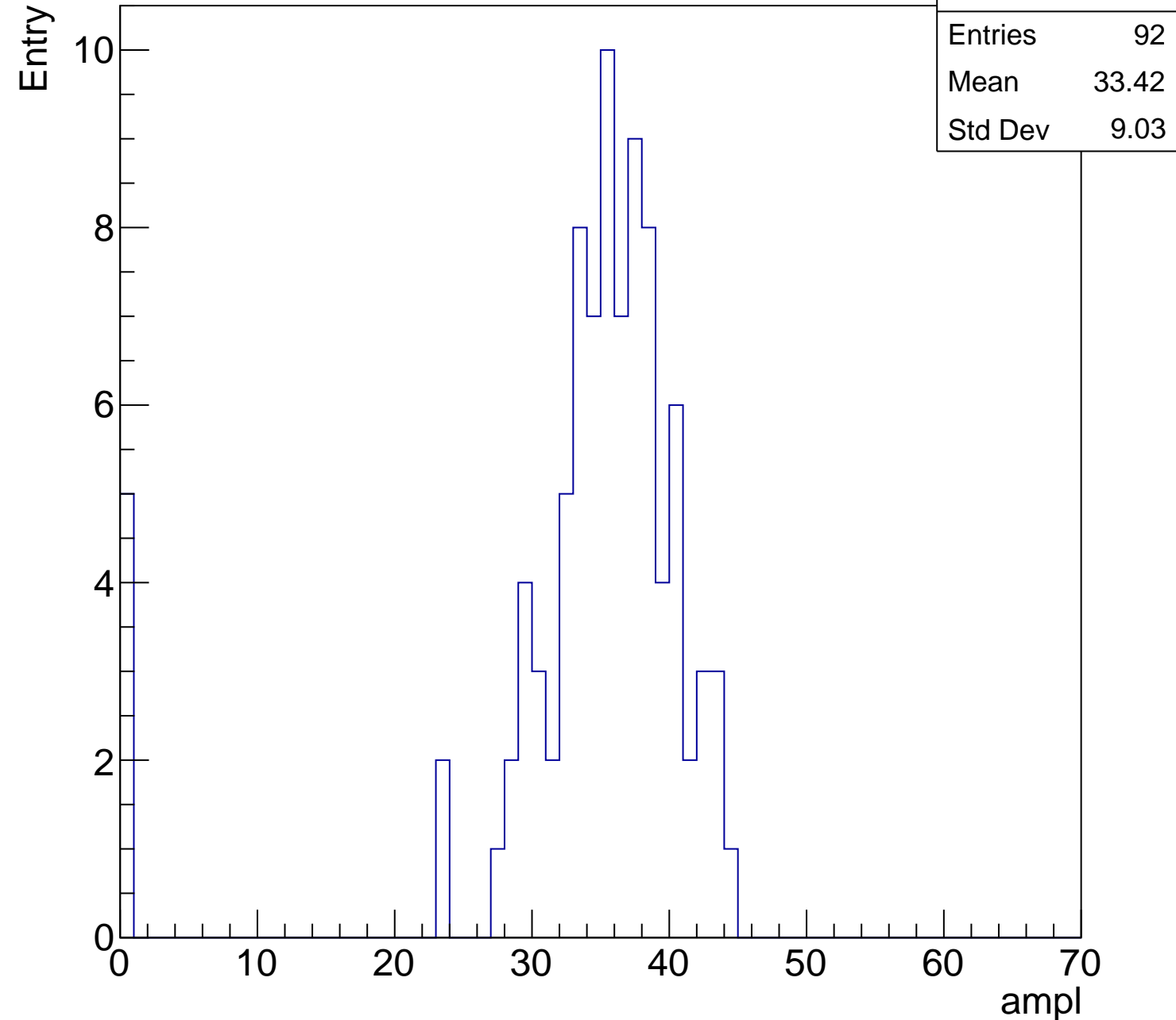
calib_packv5_041523_1651.root, FC#0, port C2

Entries	92
Mean	33.42
Std Dev	9.03

Entry

10
8
6
4
2
0

ampl

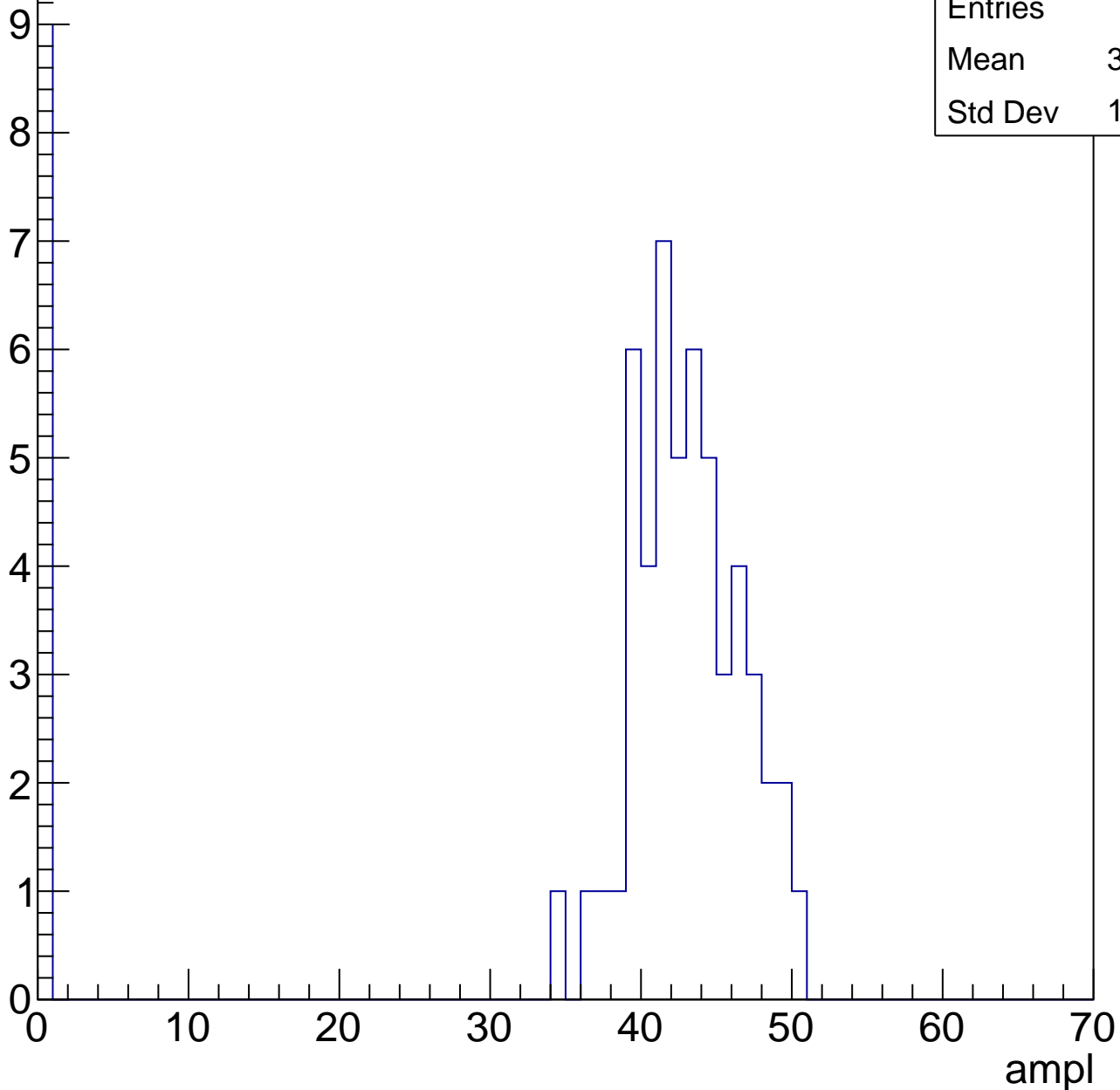


B1L103S, U12-ch106, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	36.36
Std Dev	15.46

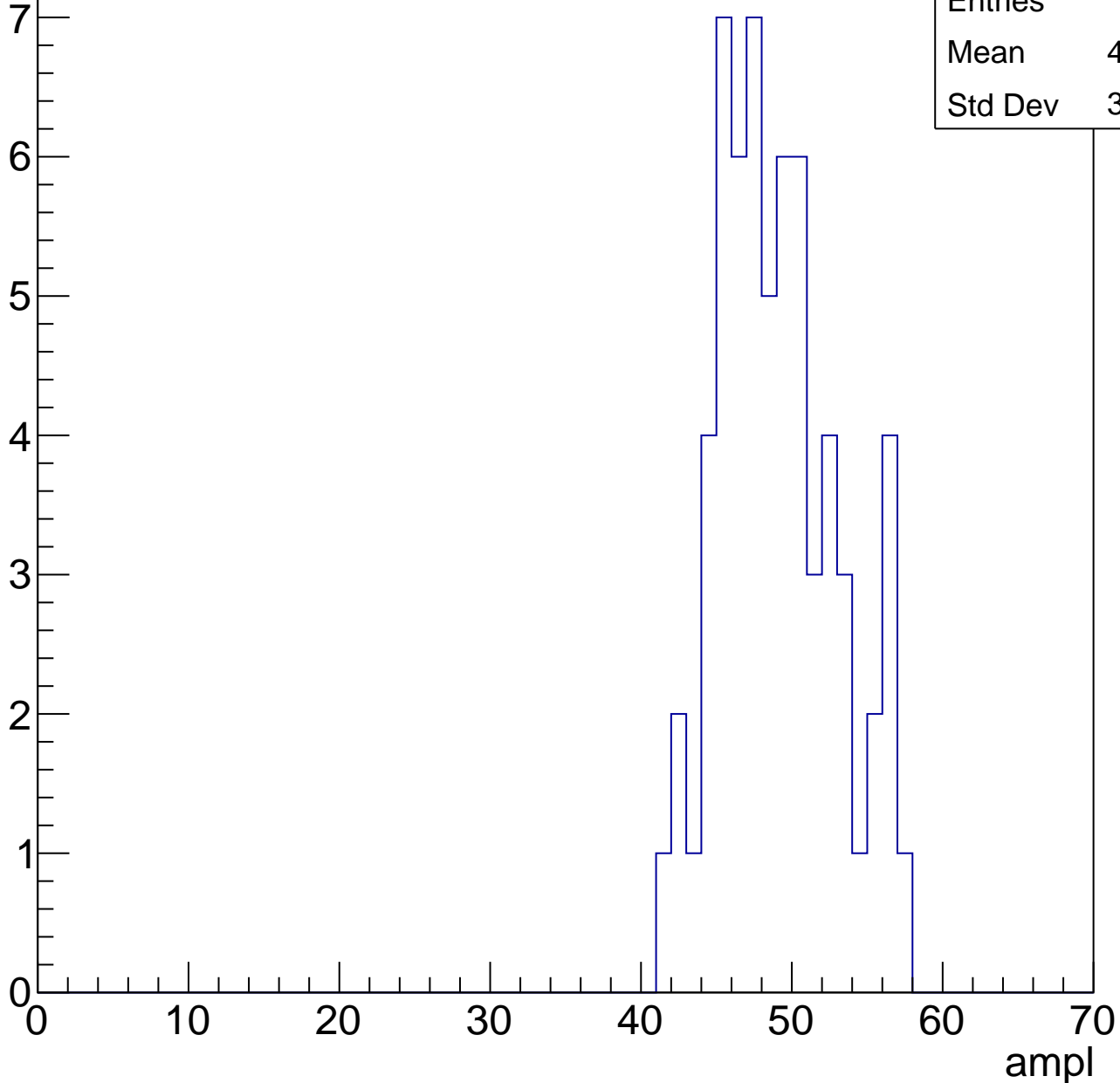


B1L103S, U12-ch106, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	63
Mean	48.62
Std Dev	3.877

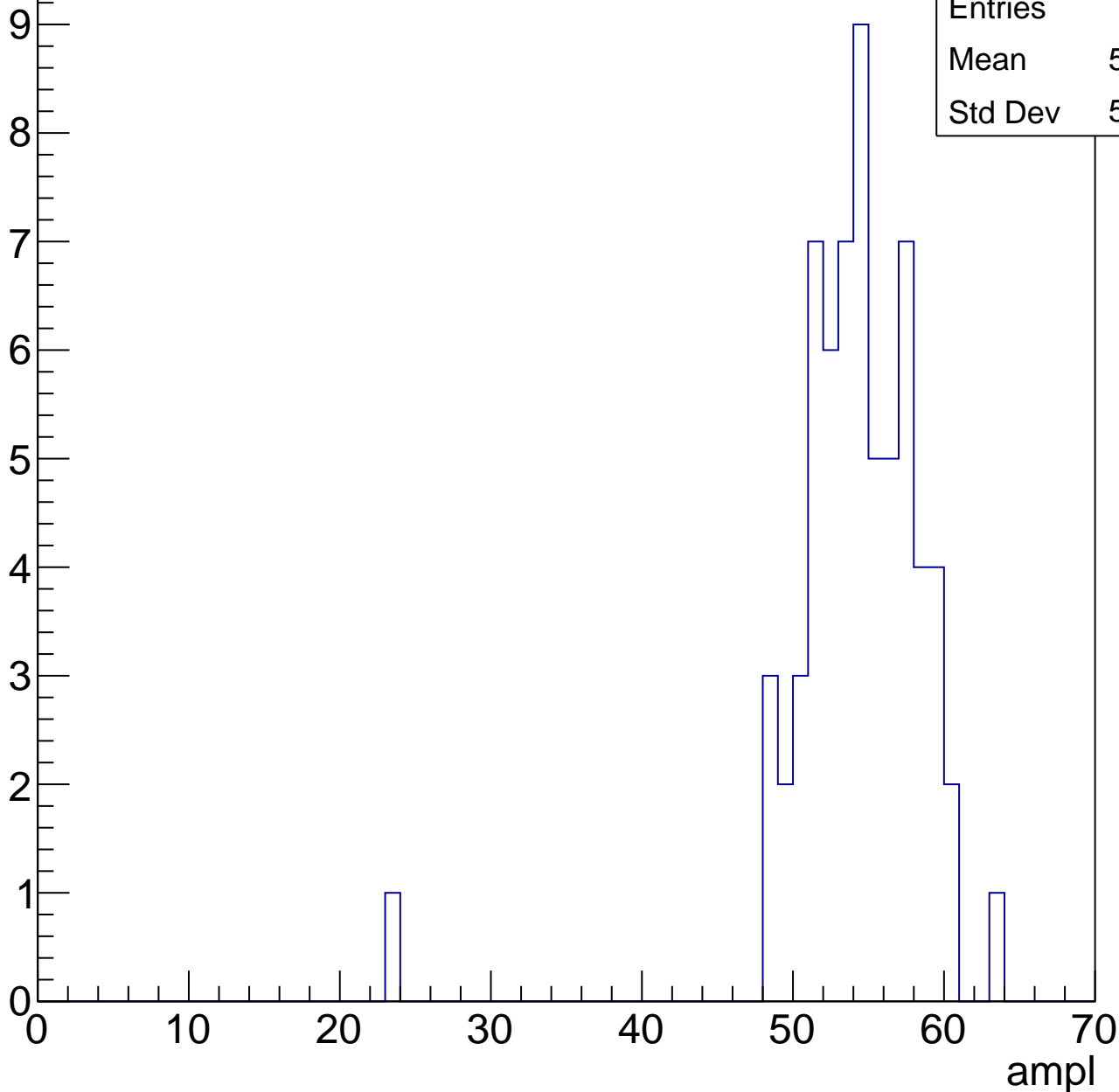


B1L103S, U12-ch106, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	53.73
Std Dev	5.017

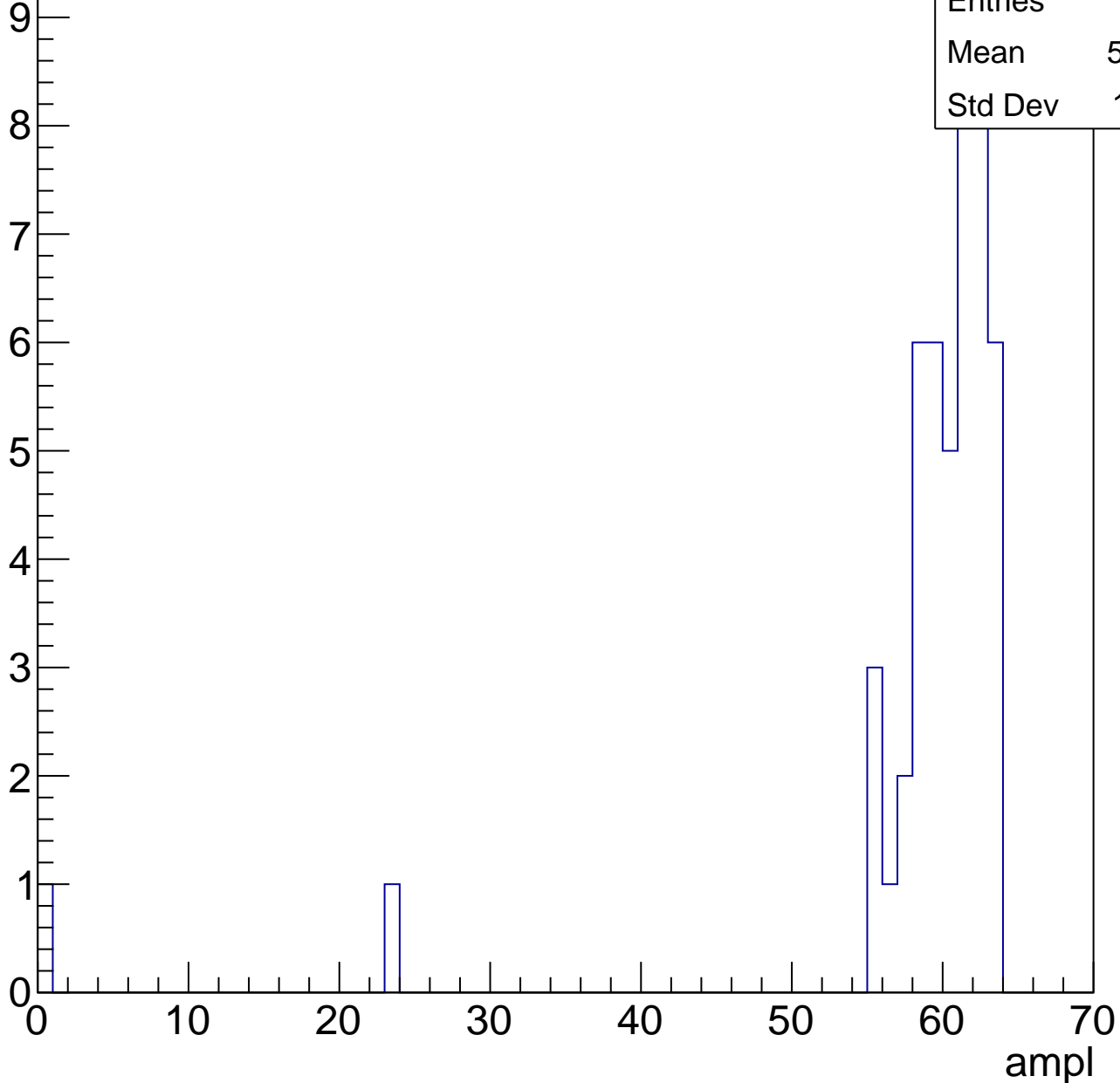


B1L103S, U12-ch106, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

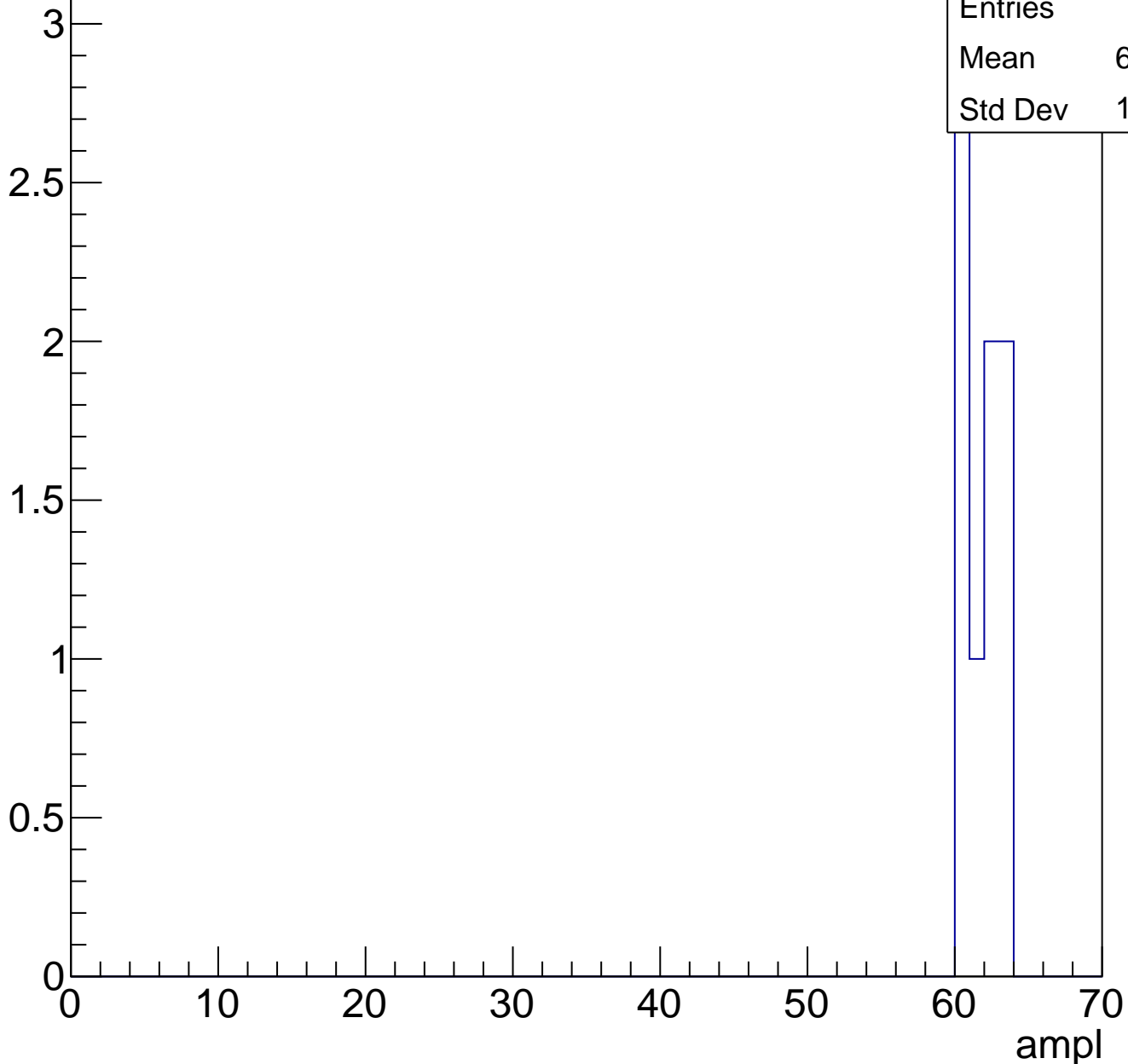
Entries	48
Mean	57.98
Std Dev	10.21



B1L103S, U12-ch106, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch106, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.15
Std Dev	13.73



B1L103S, U12-ch107, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	90
Mean	25.72
Std Dev	10.18

Entry

10

8

6

4

2

0

0

10

20

30

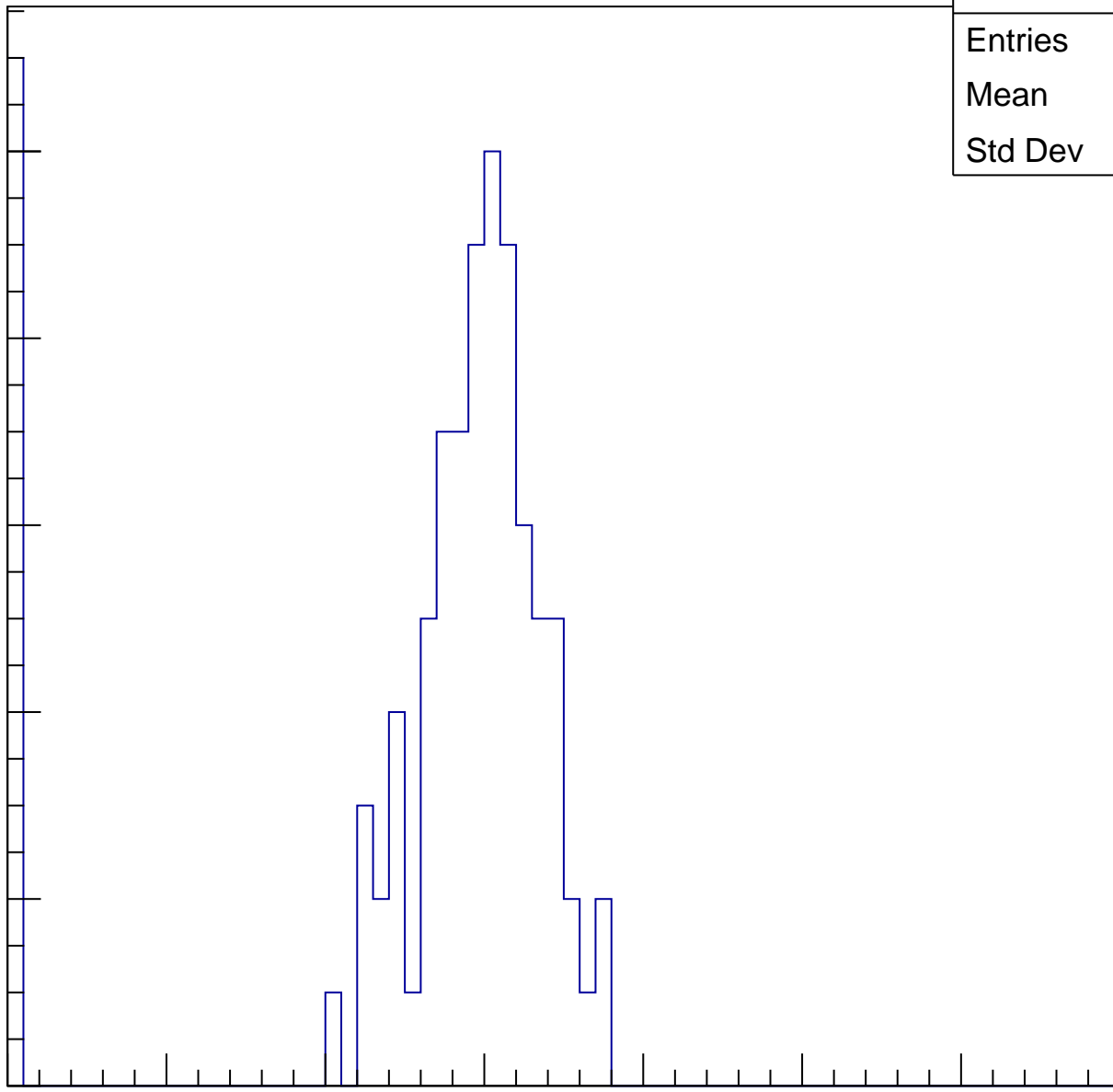
40

50

60

70

ampl



B1L103S, U12-ch107, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	83
Mean	32.37
Std Dev	13.08

Entry

10

8

6

4

2

0

0

10

20

30

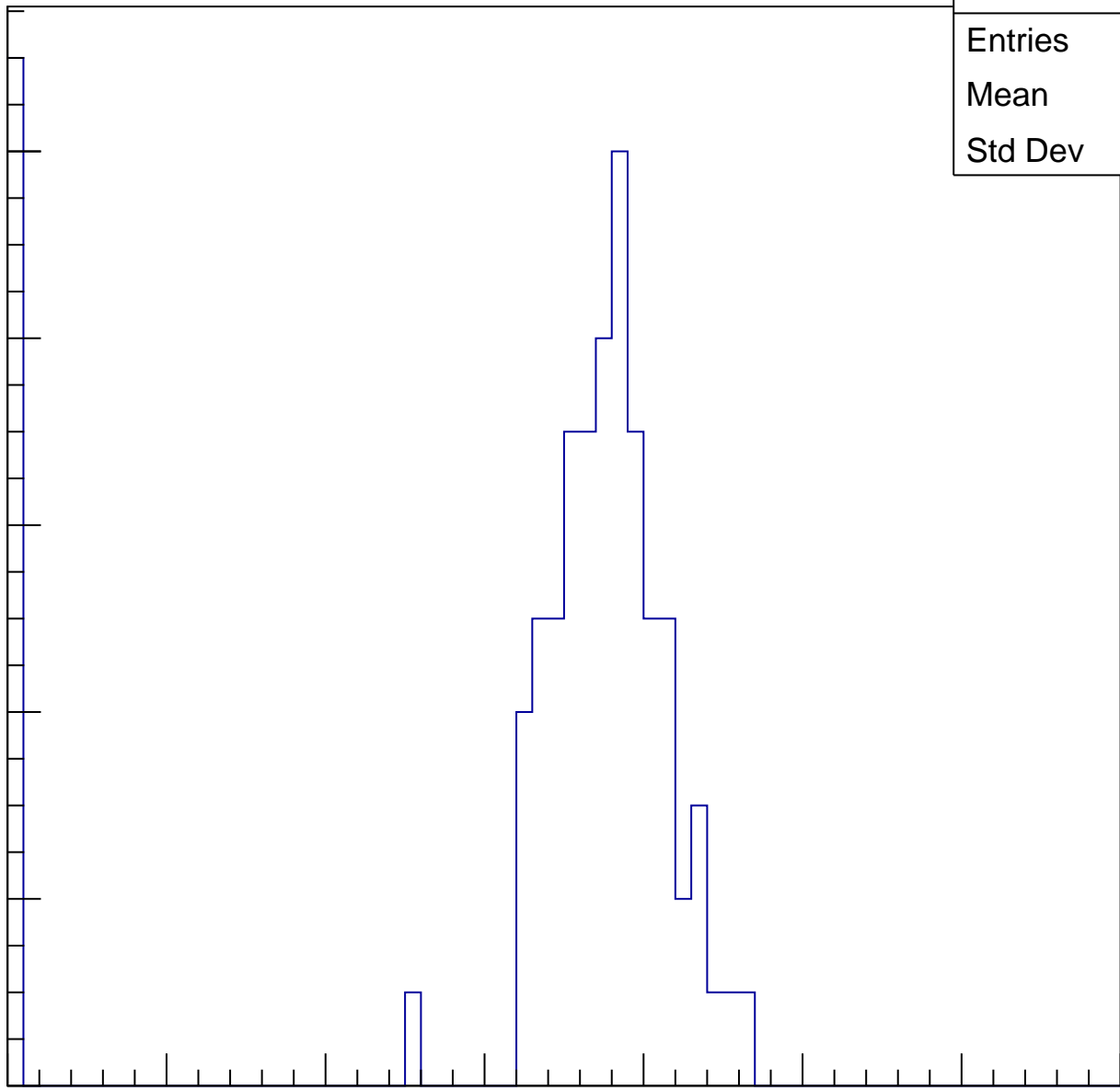
40

50

60

70

ampl

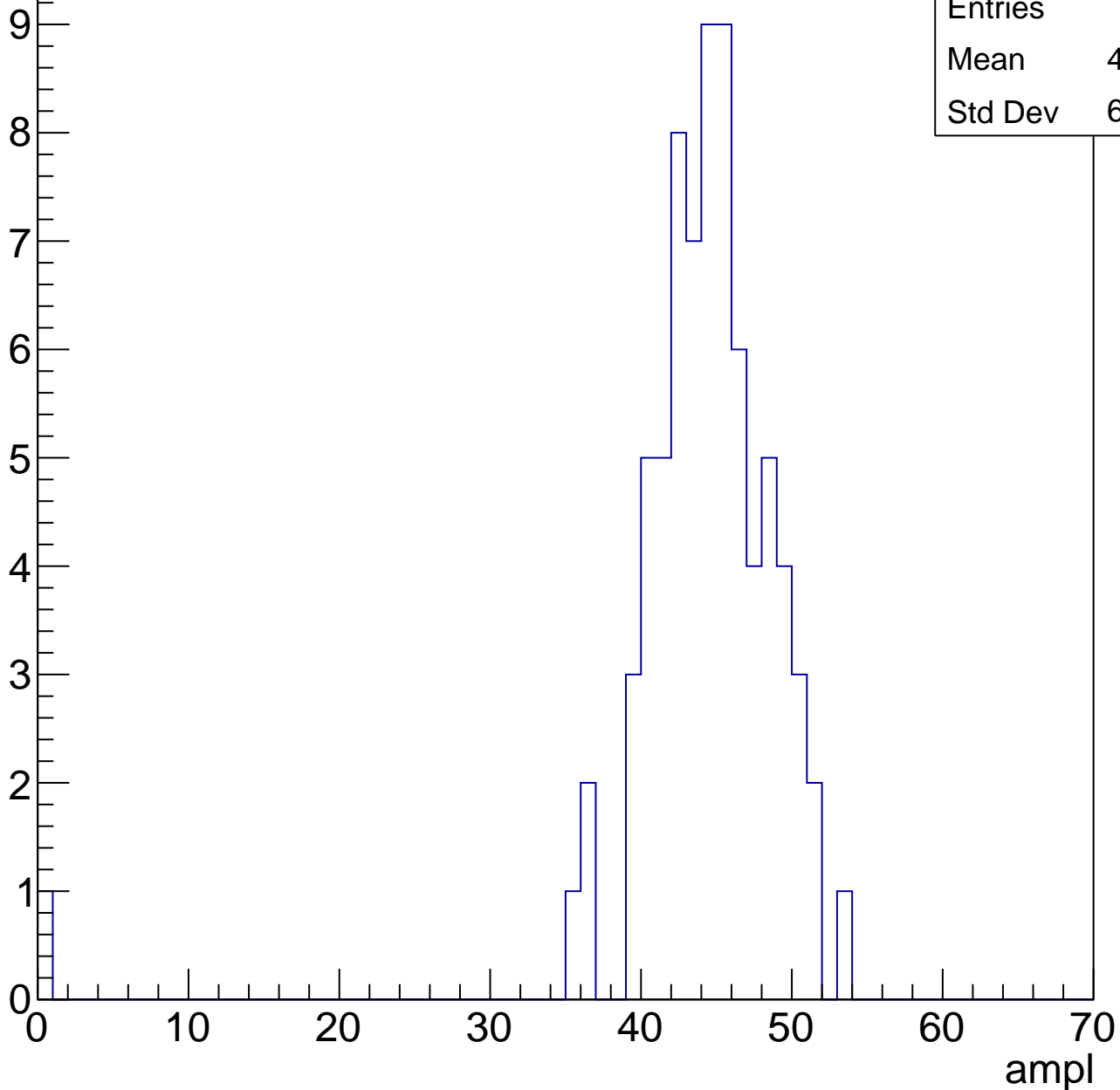


B1L103S, U12-ch107, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	75
Mean	43.63
Std Dev	6.228

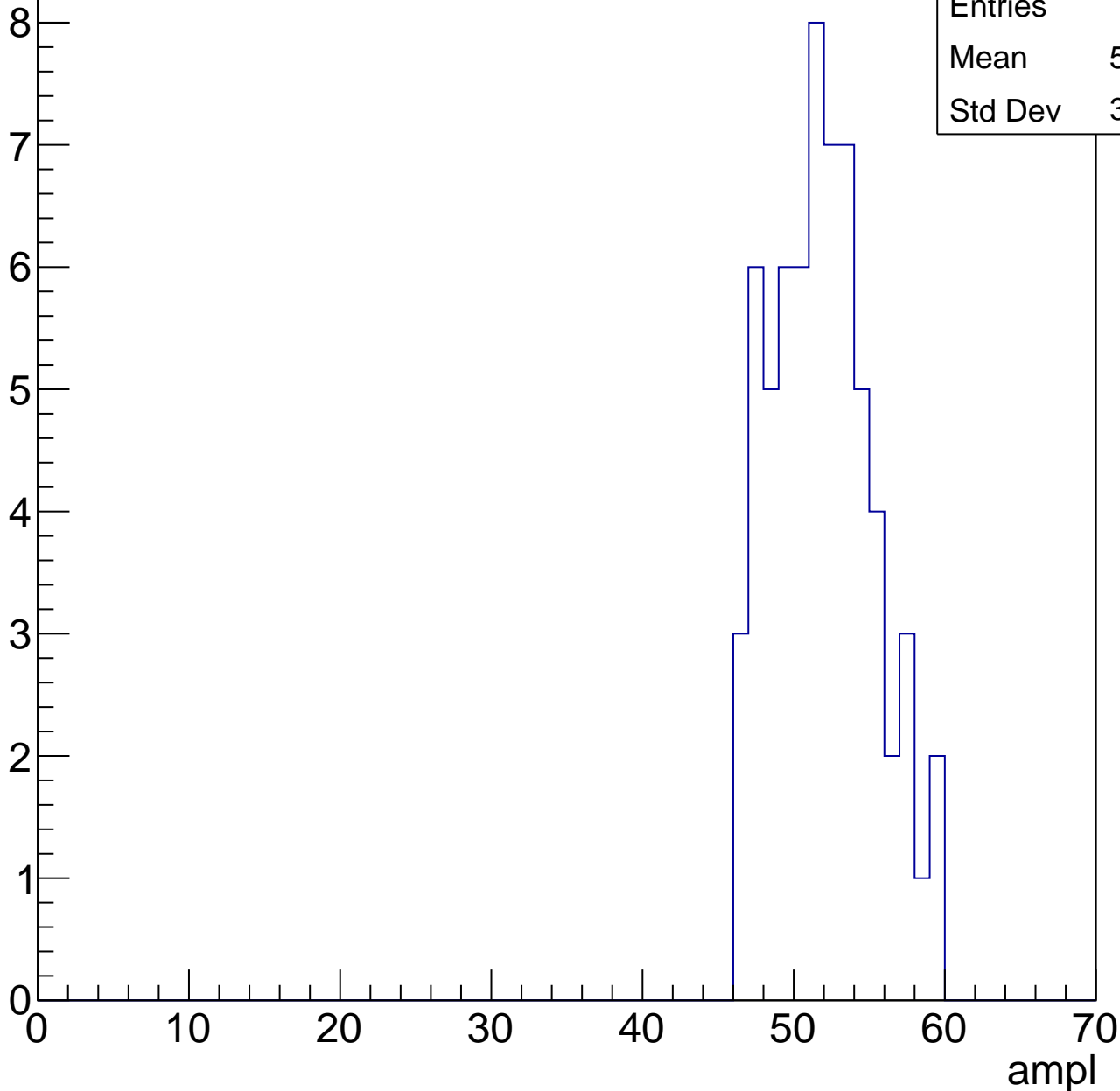


B1L103S, U12-ch107, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	51.48
Std Dev	3.306

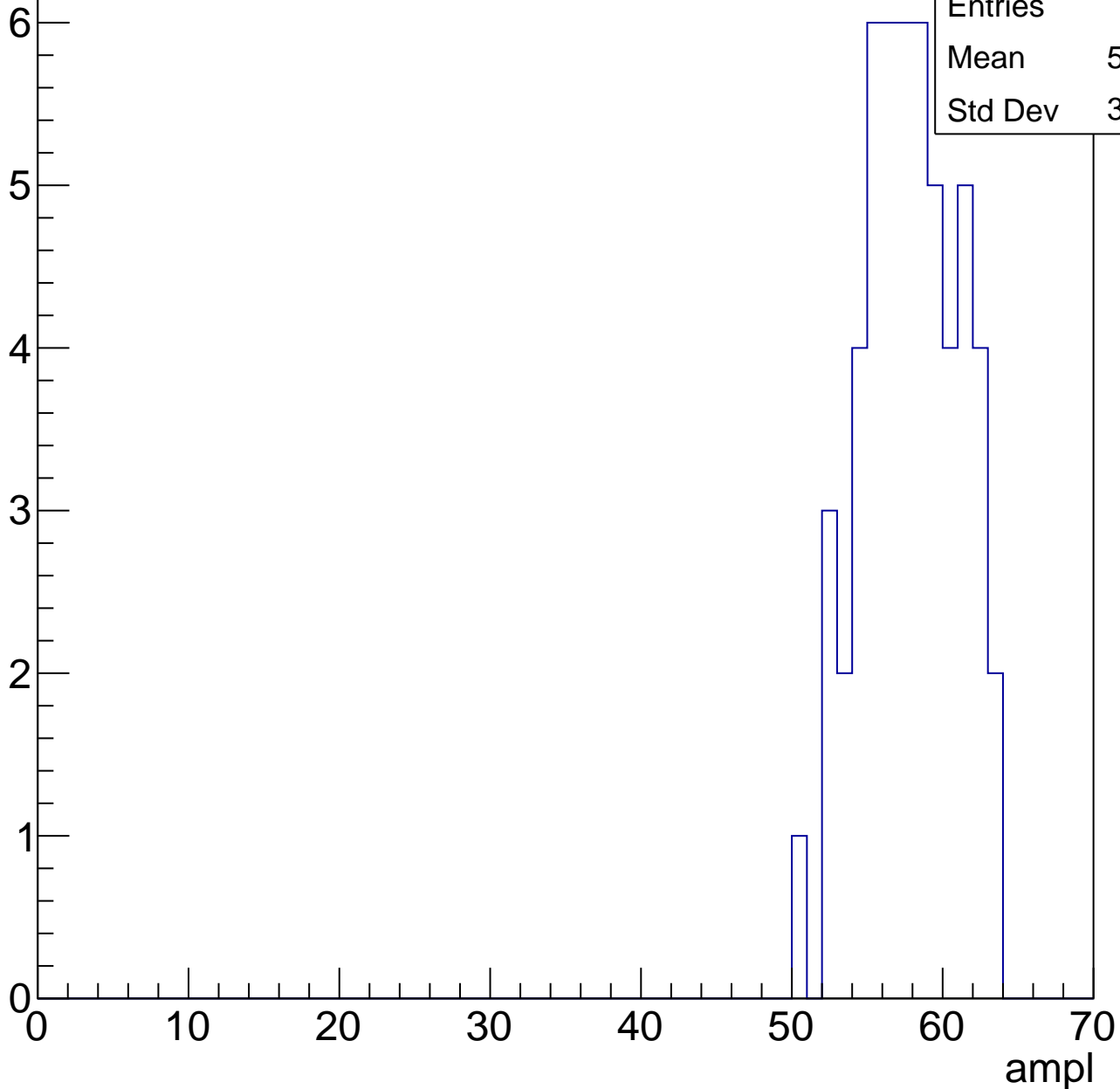


B1L103S, U12-ch107, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	54
Mean	57.37
Std Dev	3.129



B1L103S, U12-ch107, adc5

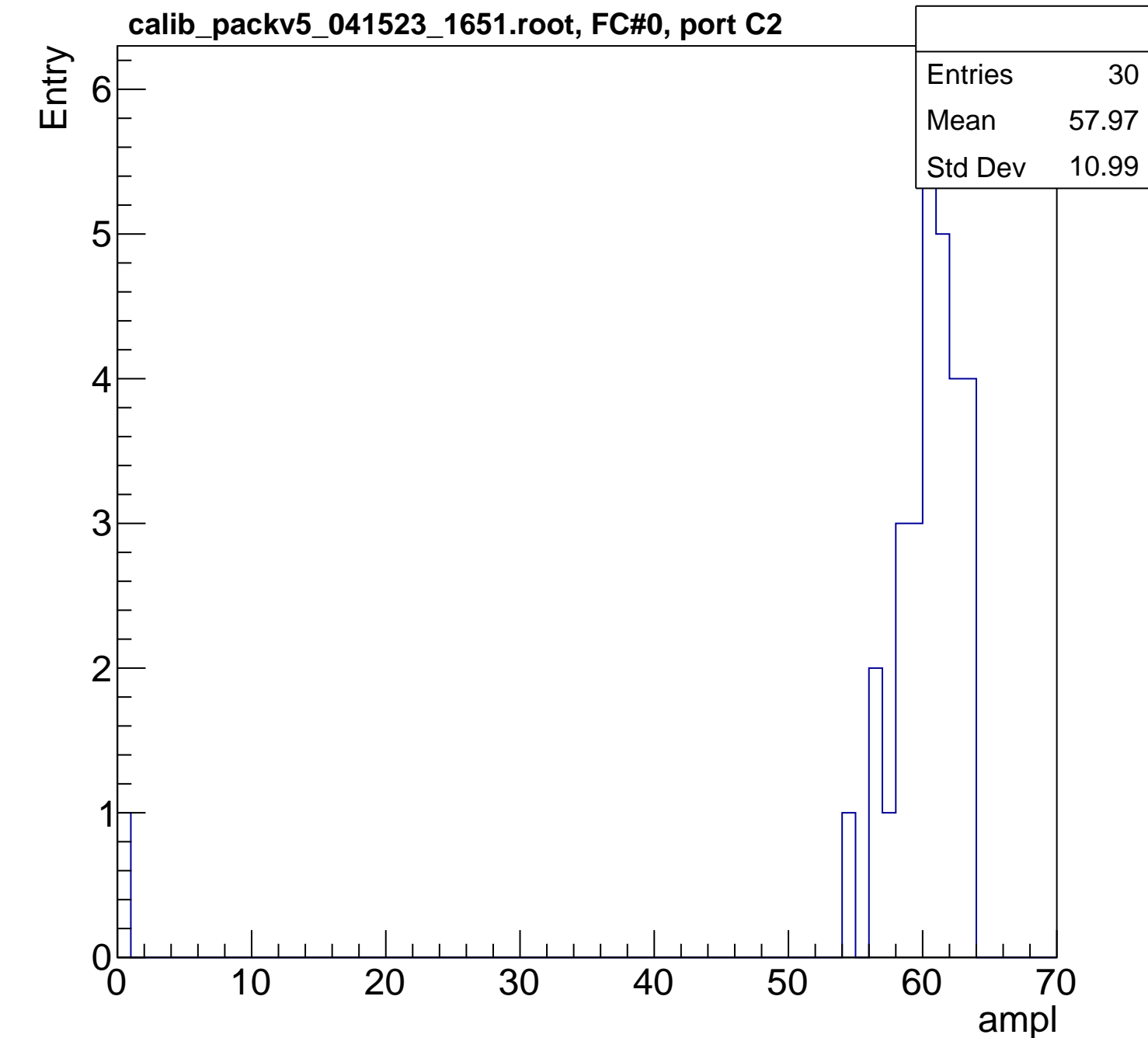
calib_packv5_041523_1651.root, FC#0, port C2

Entry

6
5
4
3
2
1
0

Entries	30
Mean	57.97
Std Dev	10.99

ampl



B1L103S, U12-ch107, adc6

calib_packv5_041523_1651.root, FC#0, port C2

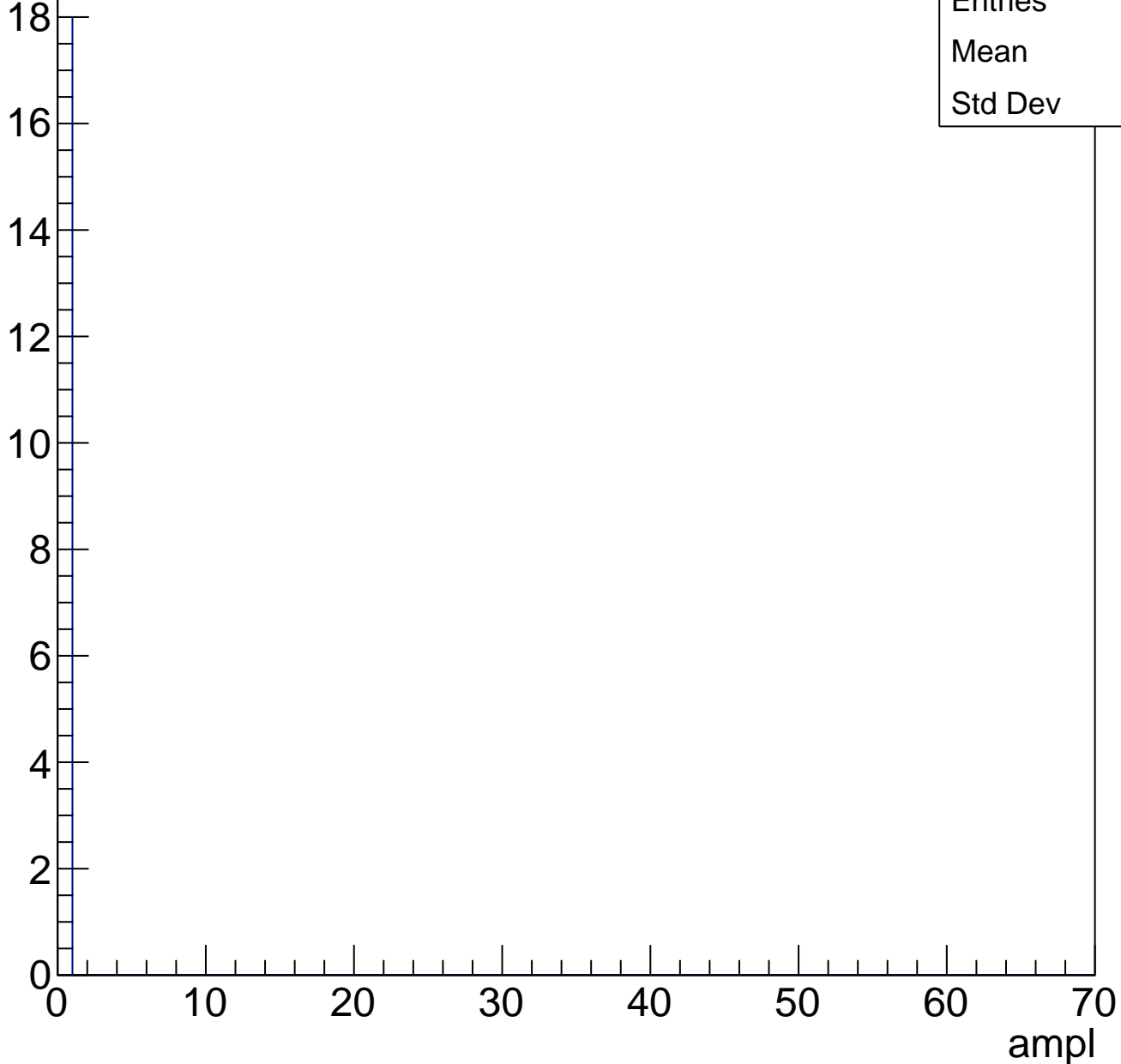
Entry



B1L103S, U12-ch107, adc7

calib_packv5_041523_1651.root, FC#0, port C2

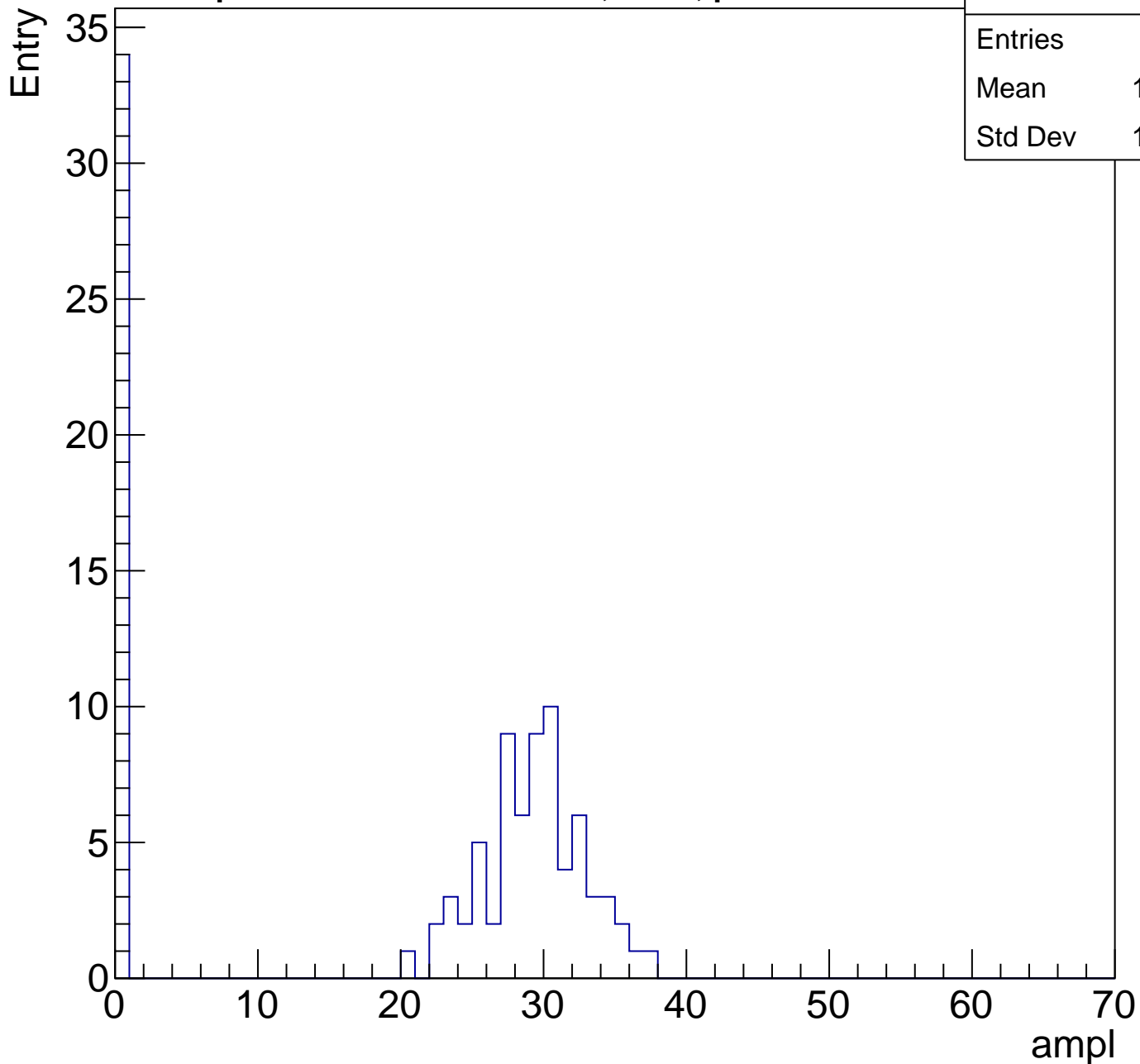
Entry



B1L103S, U12-ch108, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	103
Mean	19.32
Std Dev	13.87



B1L103S, U12-ch108, adc1

calib_packv5_041523_1651.root, FC#0, port C2

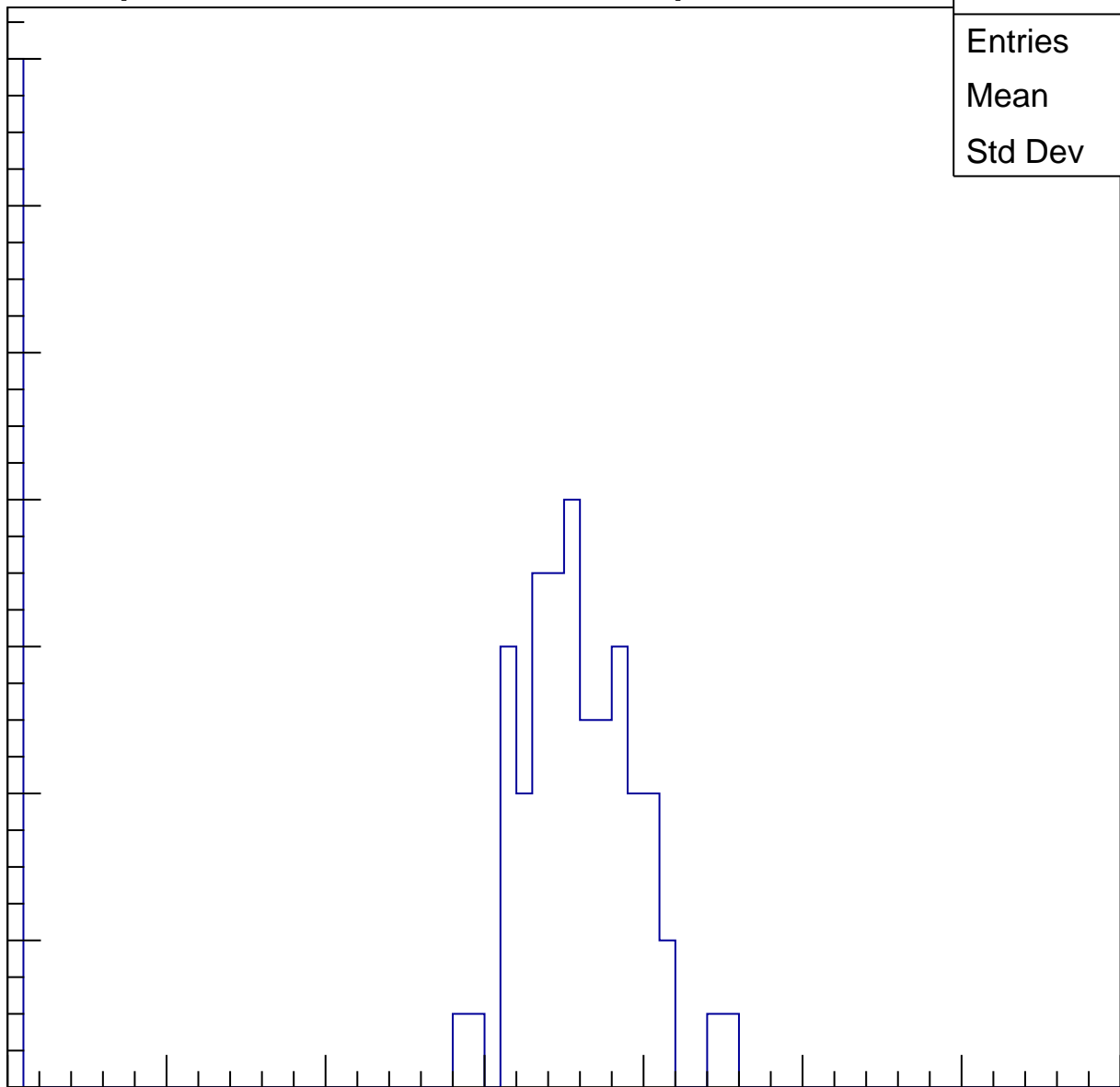
Entries	76
Mean	28.95
Std Dev	14.1

Entry

14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

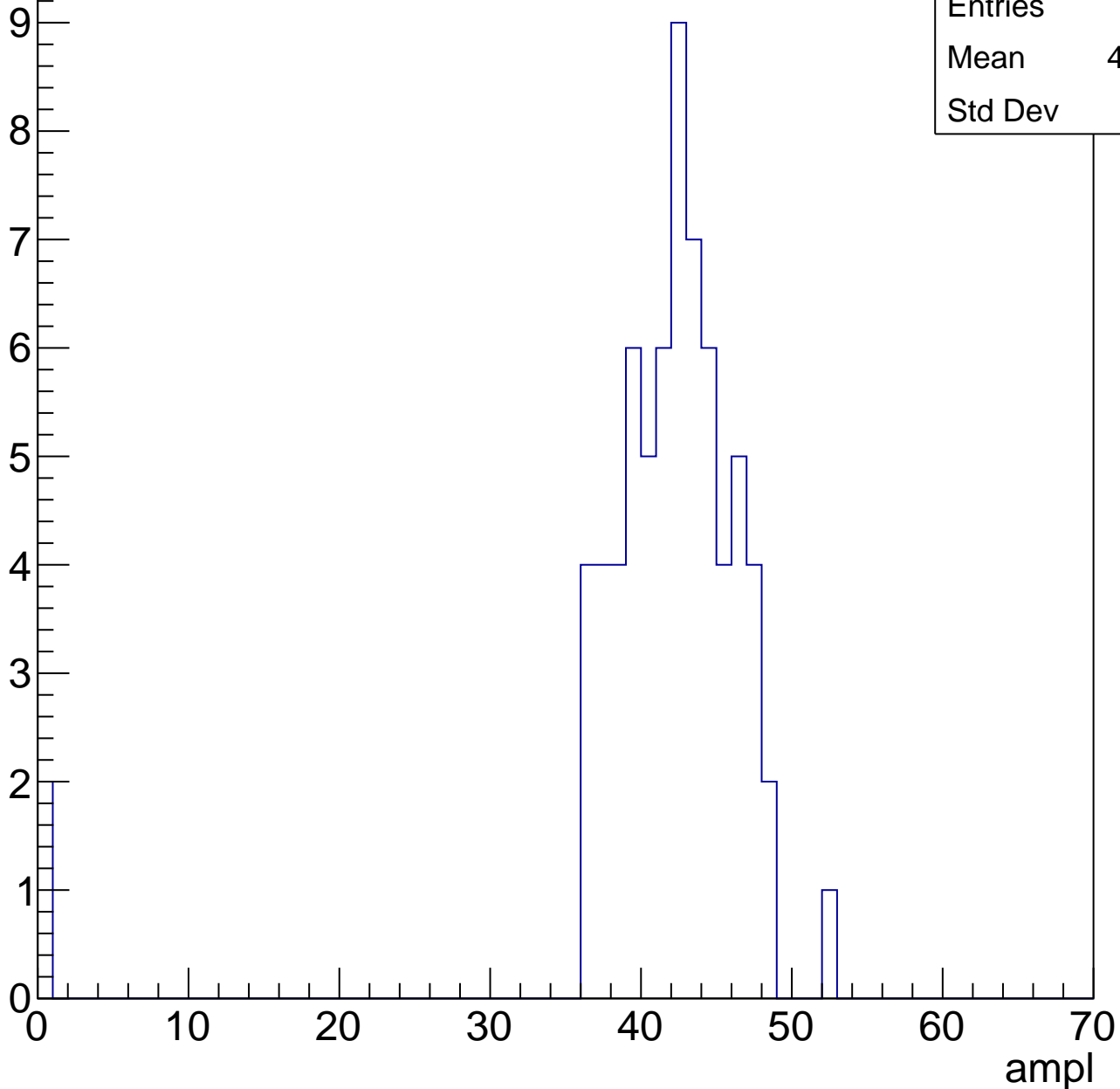


B1L103S, U12-ch108, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	40.77
Std Dev	7.83

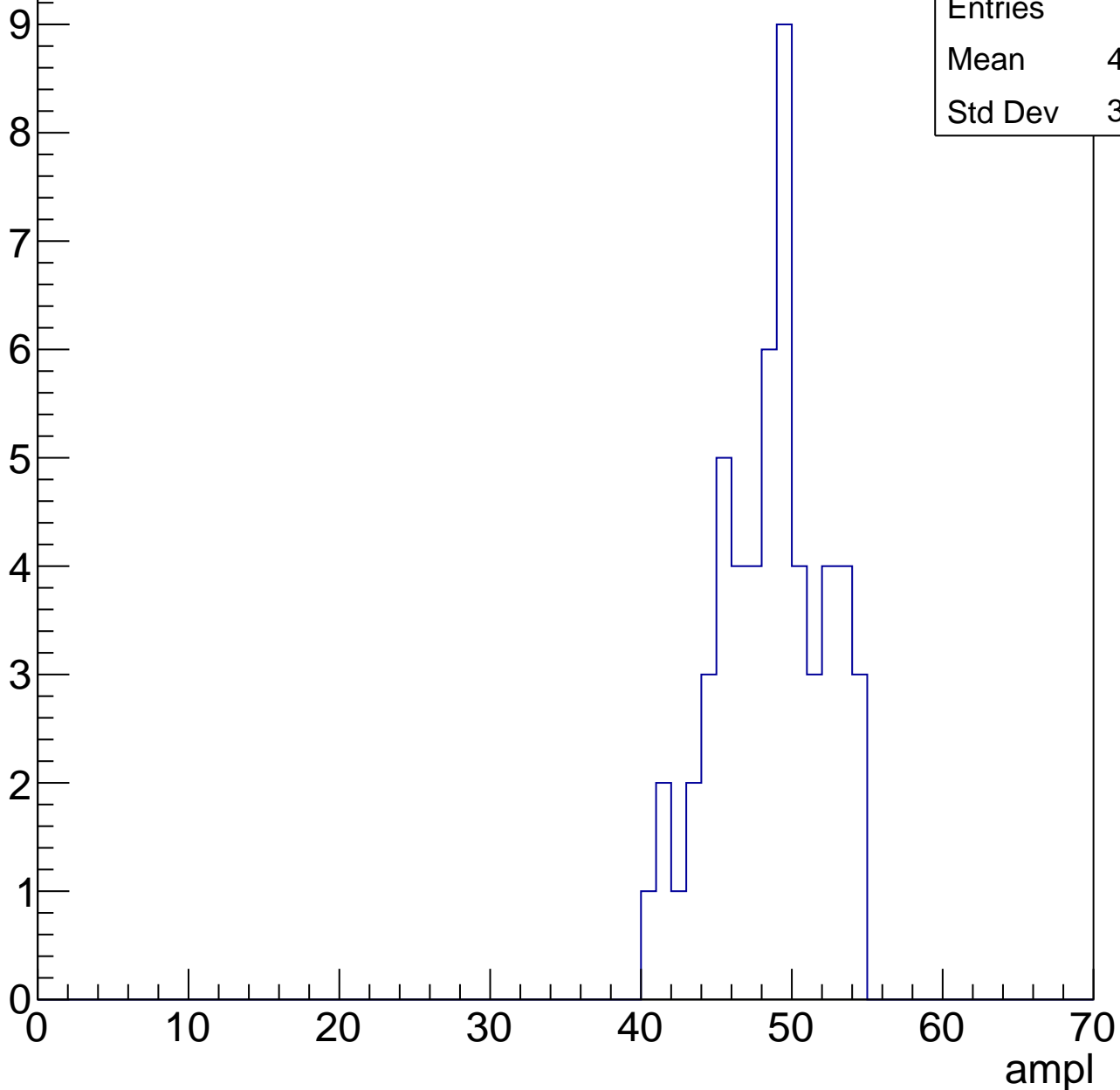


B1L103S, U12-ch108, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	48.05
Std Dev	3.529

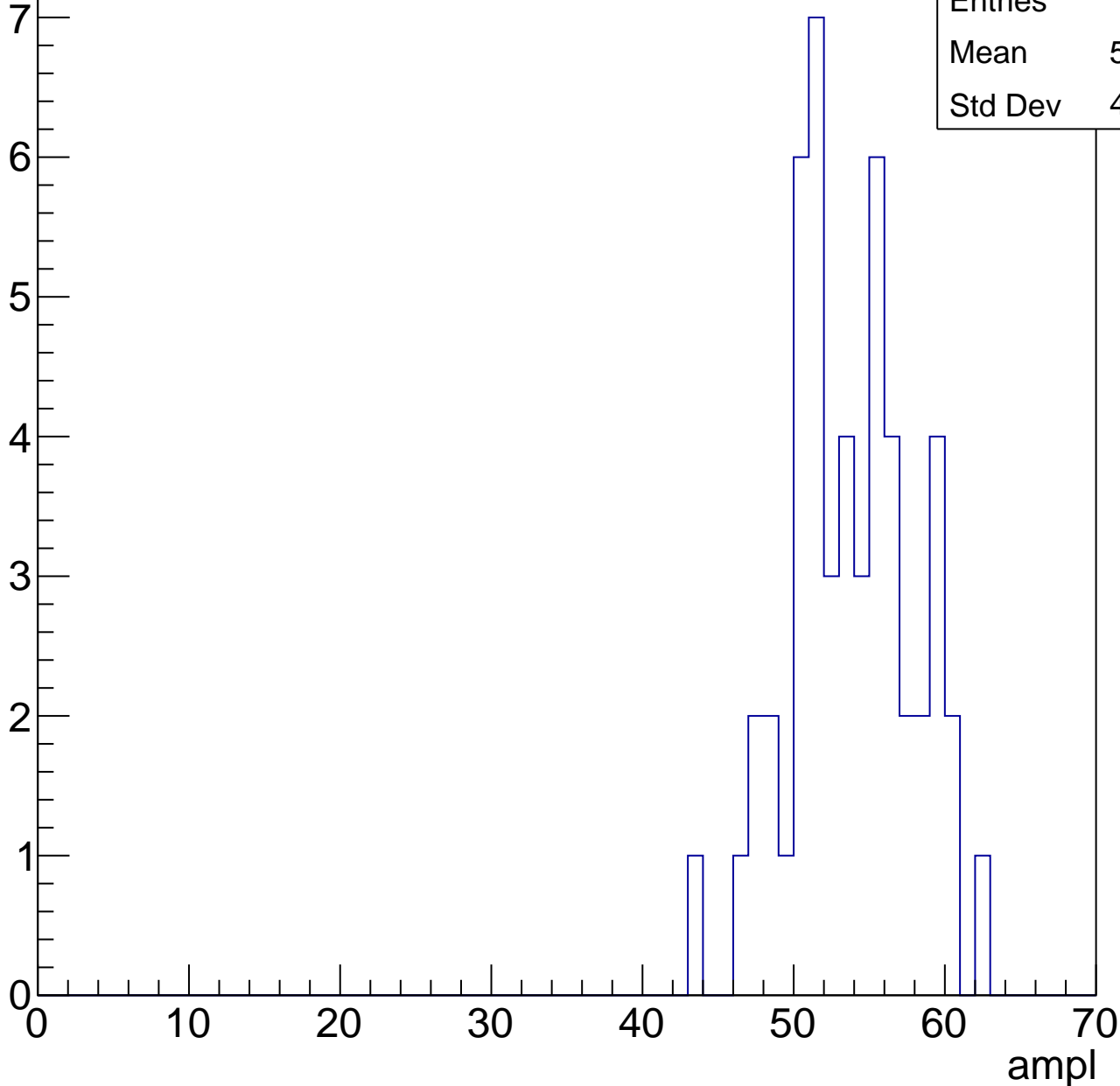


B1L103S, U12-ch108, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	51
Mean	53.27
Std Dev	4.049

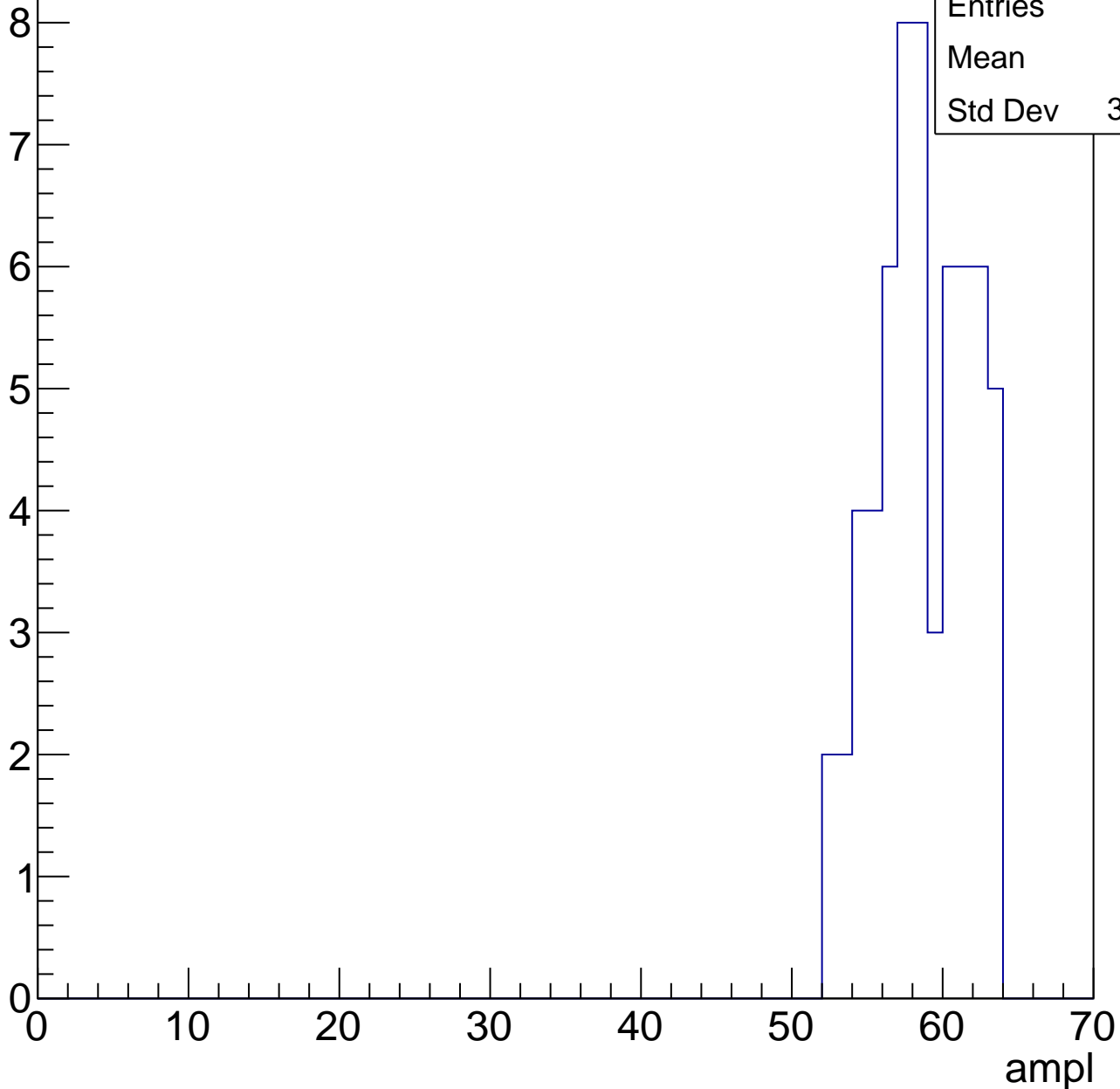


B1L103S, U12-ch108, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	58.2
Std Dev	3.038

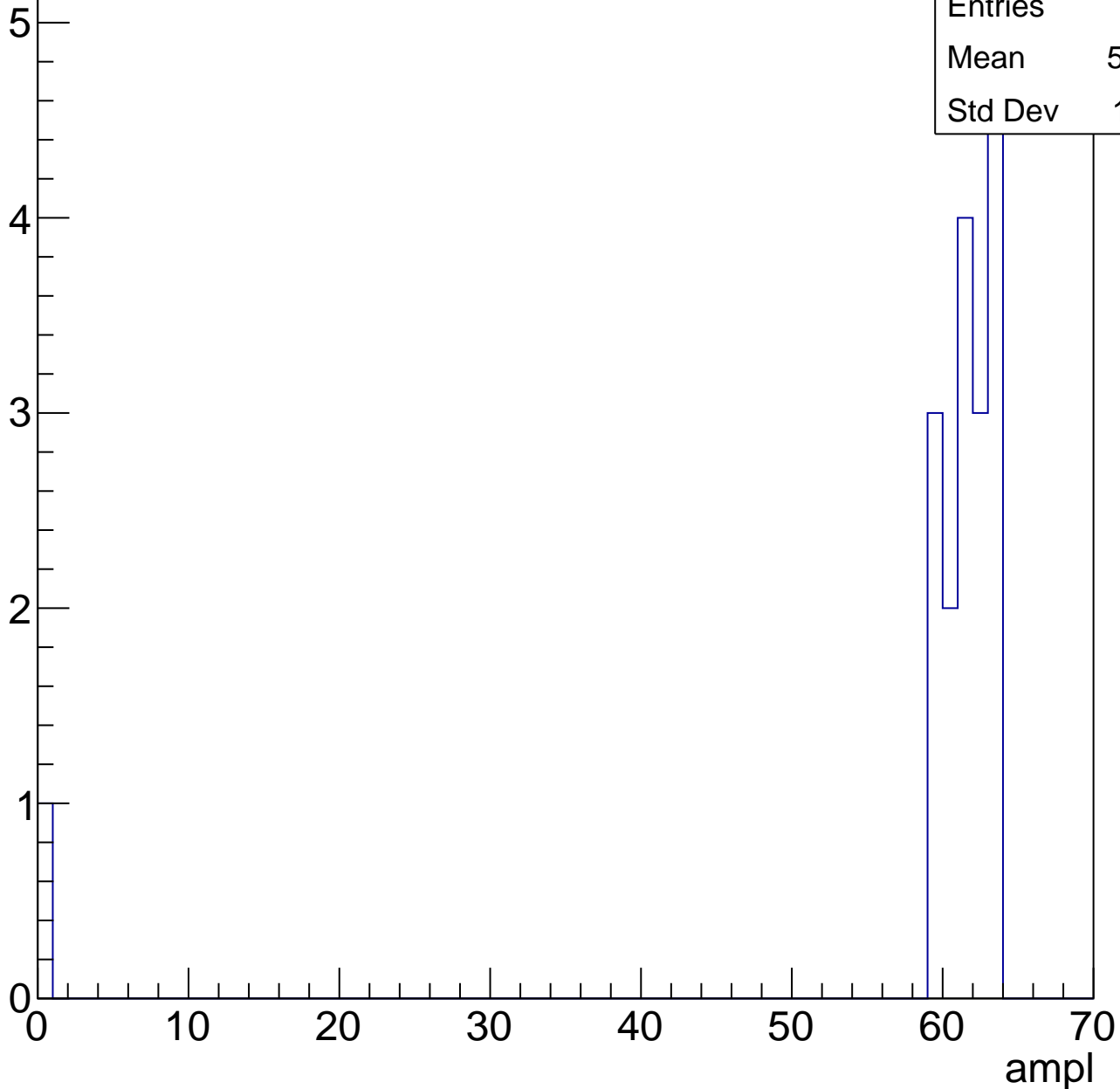


B1L103S, U12-ch108, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	18
Mean	57.89
Std Dev	14.11



B1L103S, U12-ch108, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

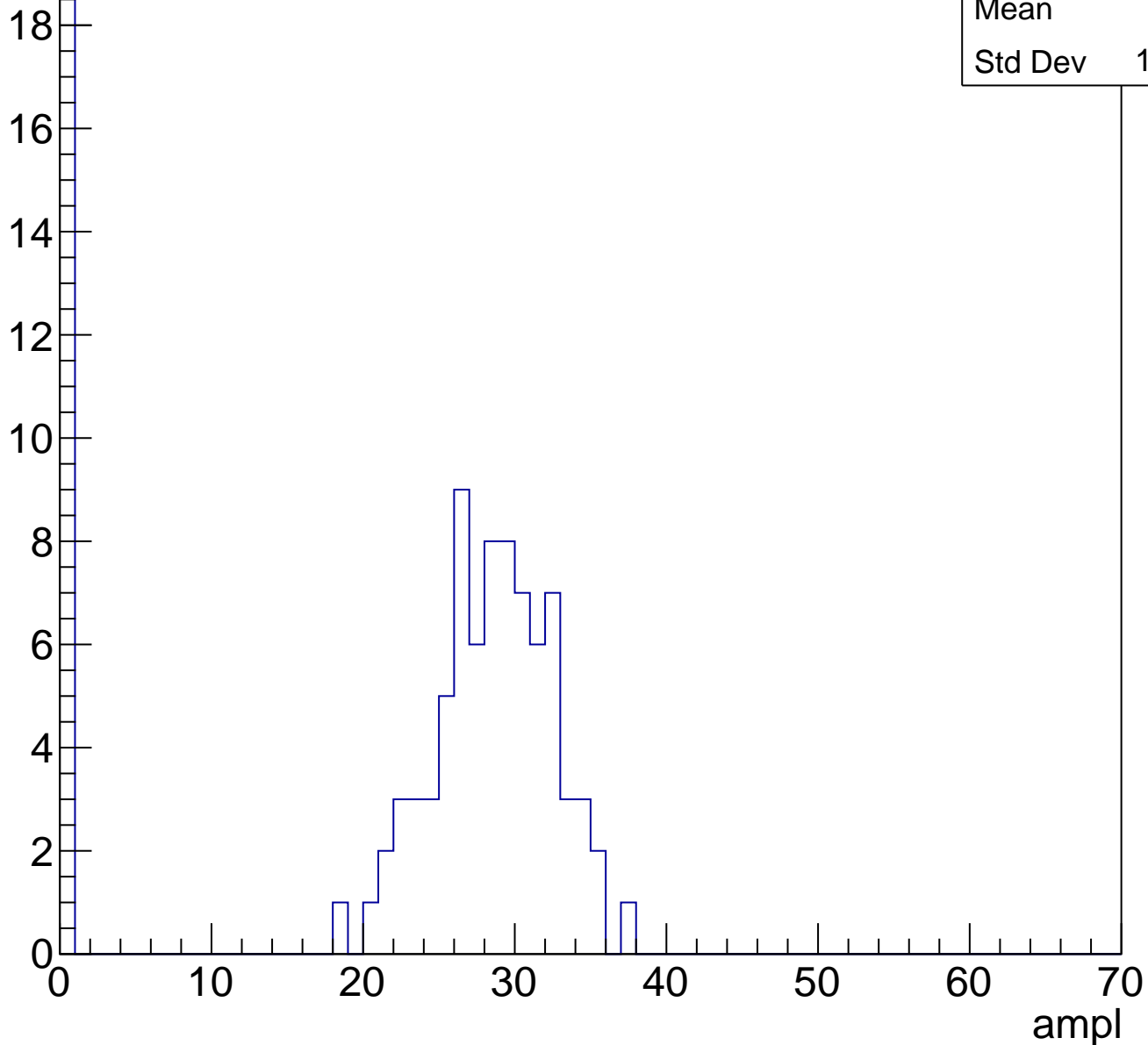


B1L103S, U12-ch109, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	97
Mean	22.6
Std Dev	11.67

Entry

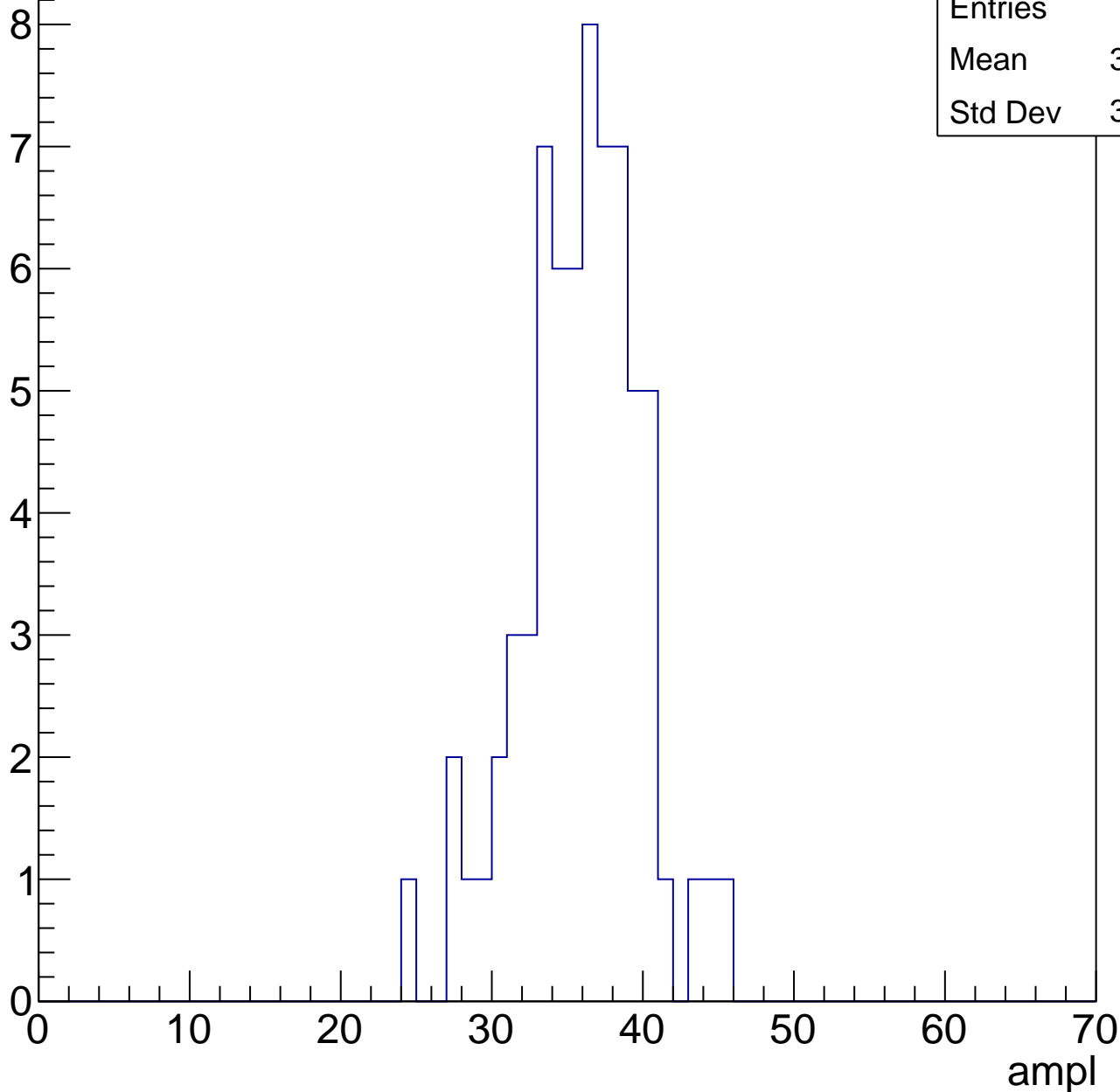


B1L103S, U12-ch109, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	35.44
Std Dev	3.957

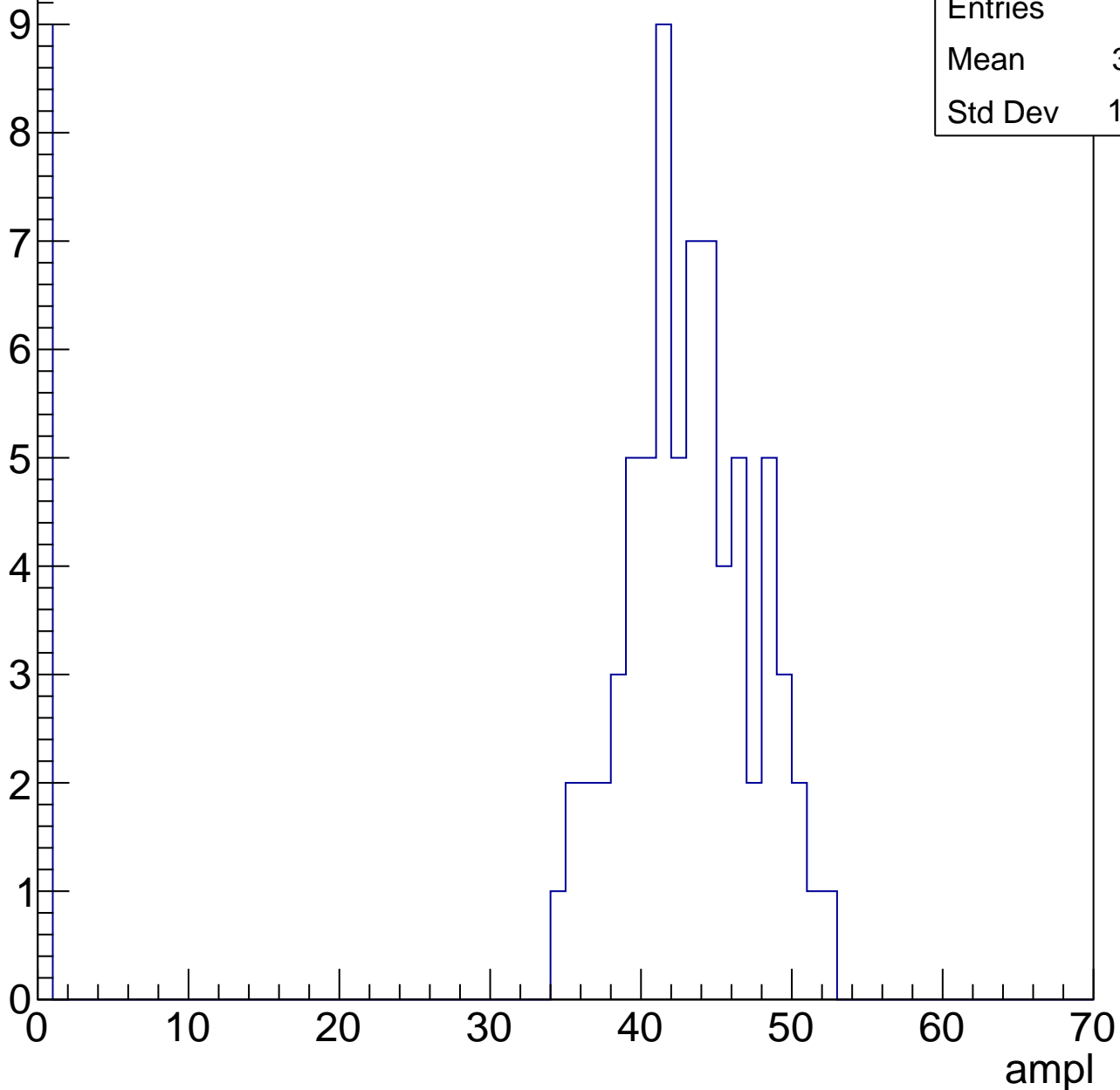


B1L103S, U12-ch109, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	80
Mean	38.01
Std Dev	14.07

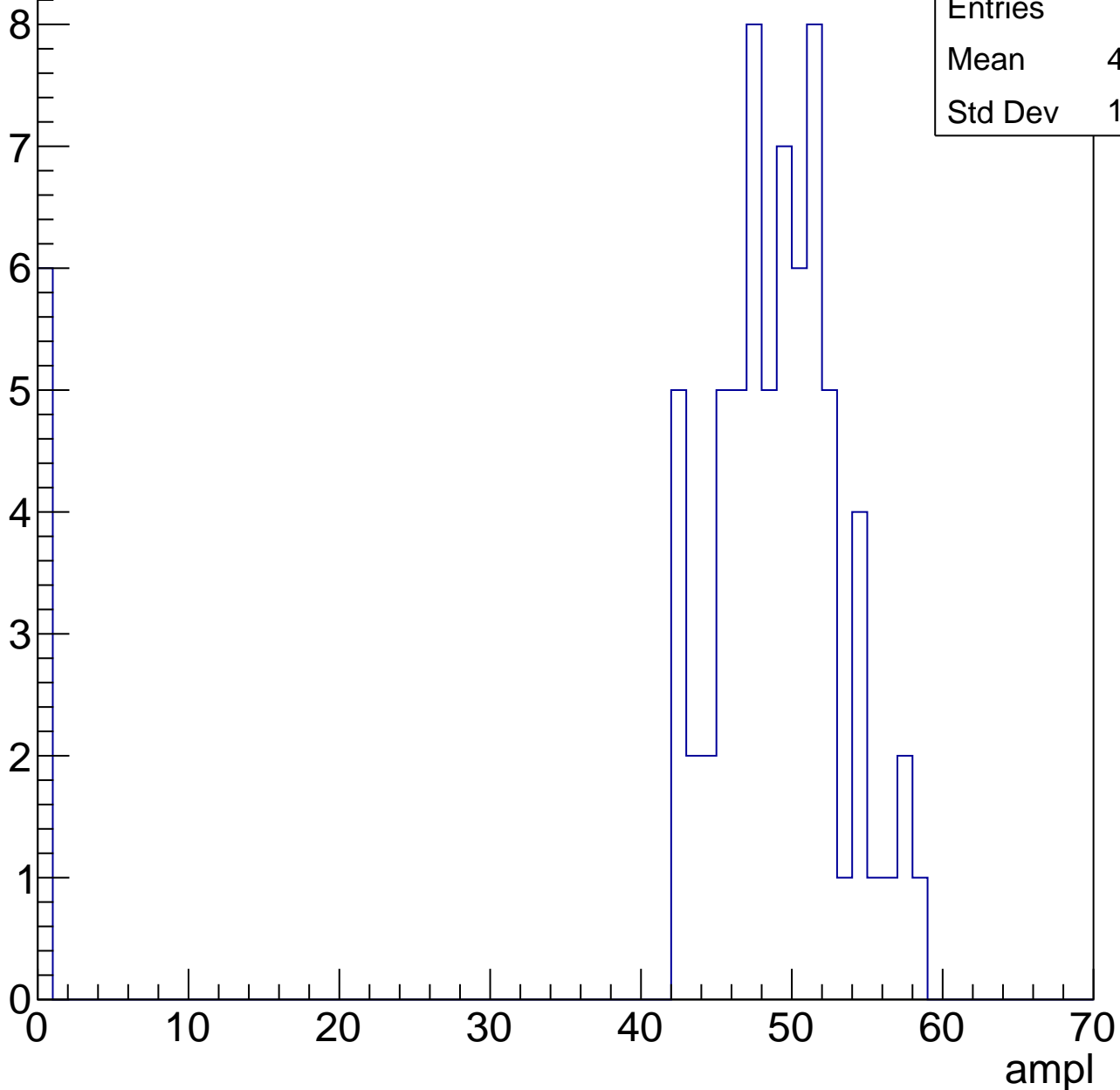


B1L103S, U12-ch109, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	74
Mean	44.84
Std Dev	13.83

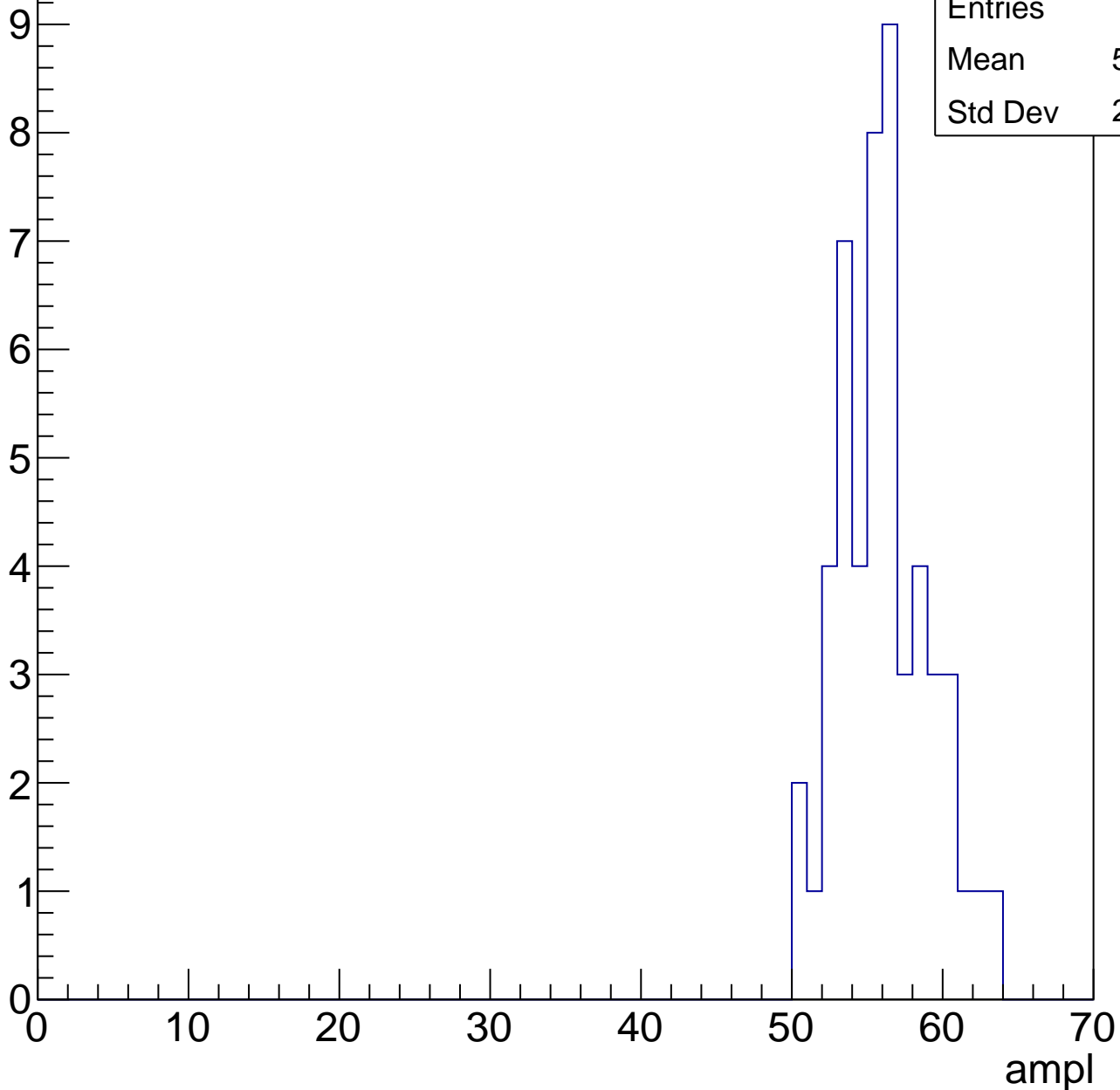


B1L103S, U12-ch109, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	51
Mean	55.61
Std Dev	2.951

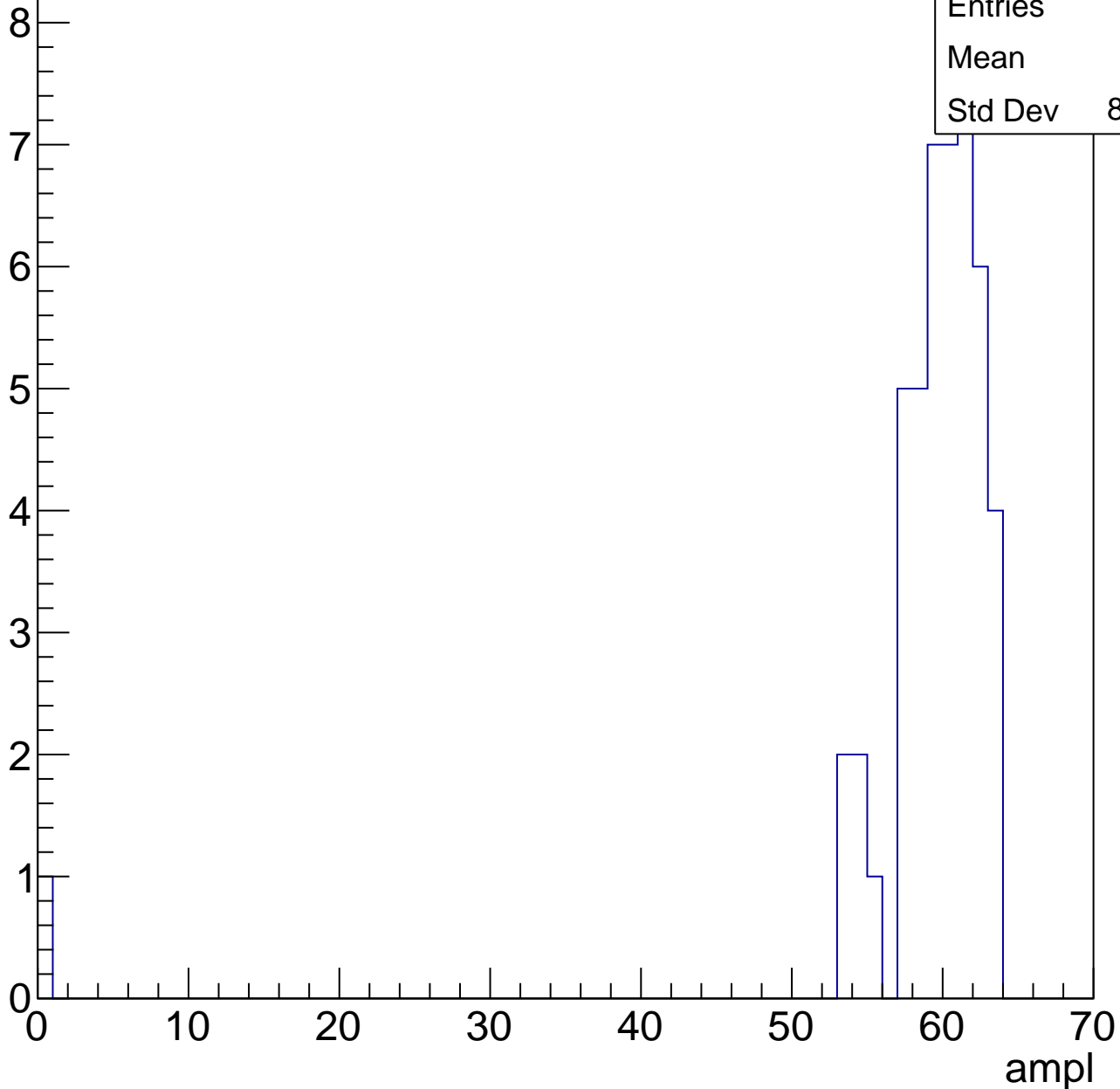


B1L103S, U12-ch109, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	48
Mean	58.1
Std Dev	8.854



B1L103S, U12-ch109, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

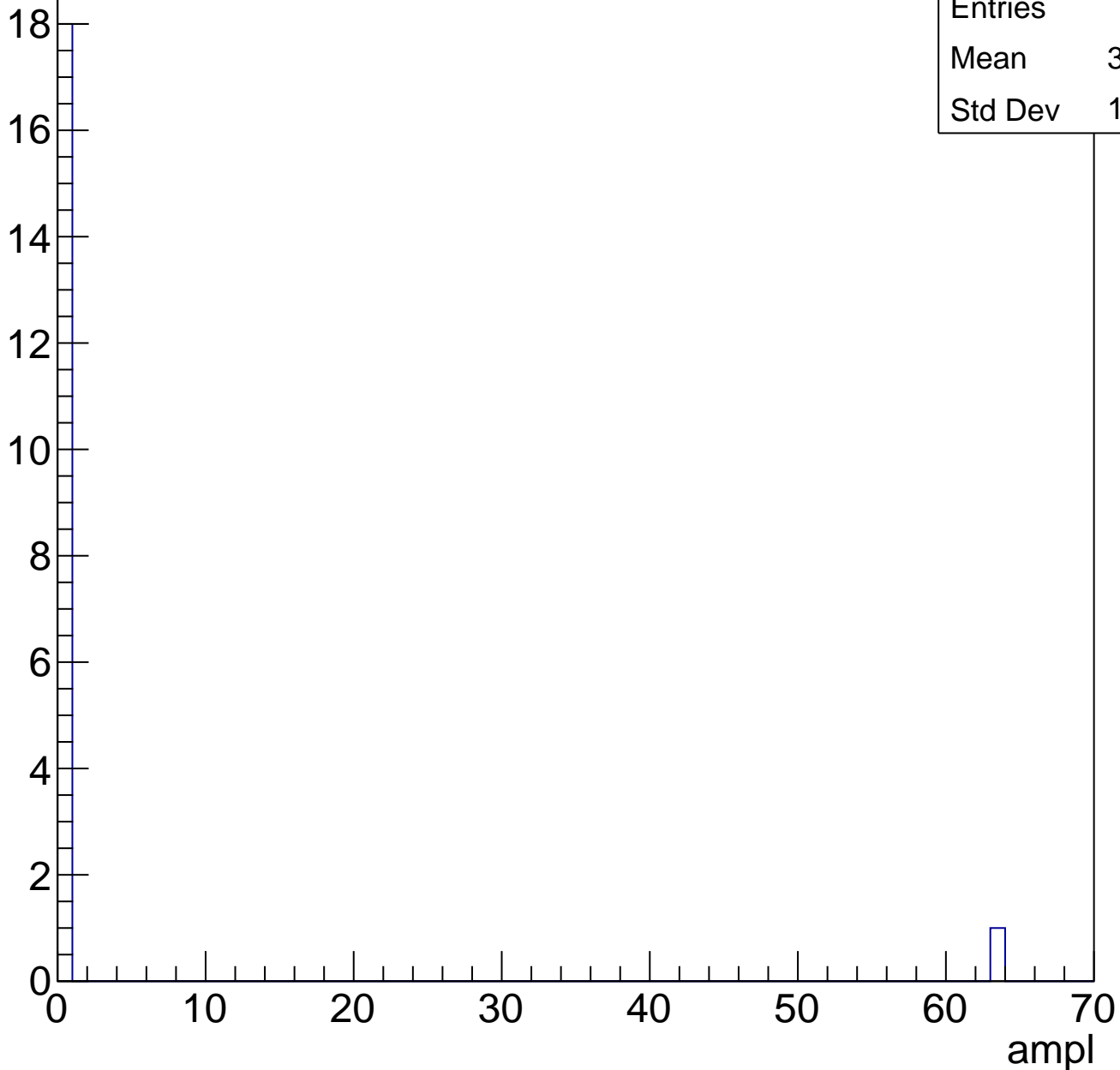


B1L103S, U12-ch109, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	3.316
Std Dev	14.07

Entry

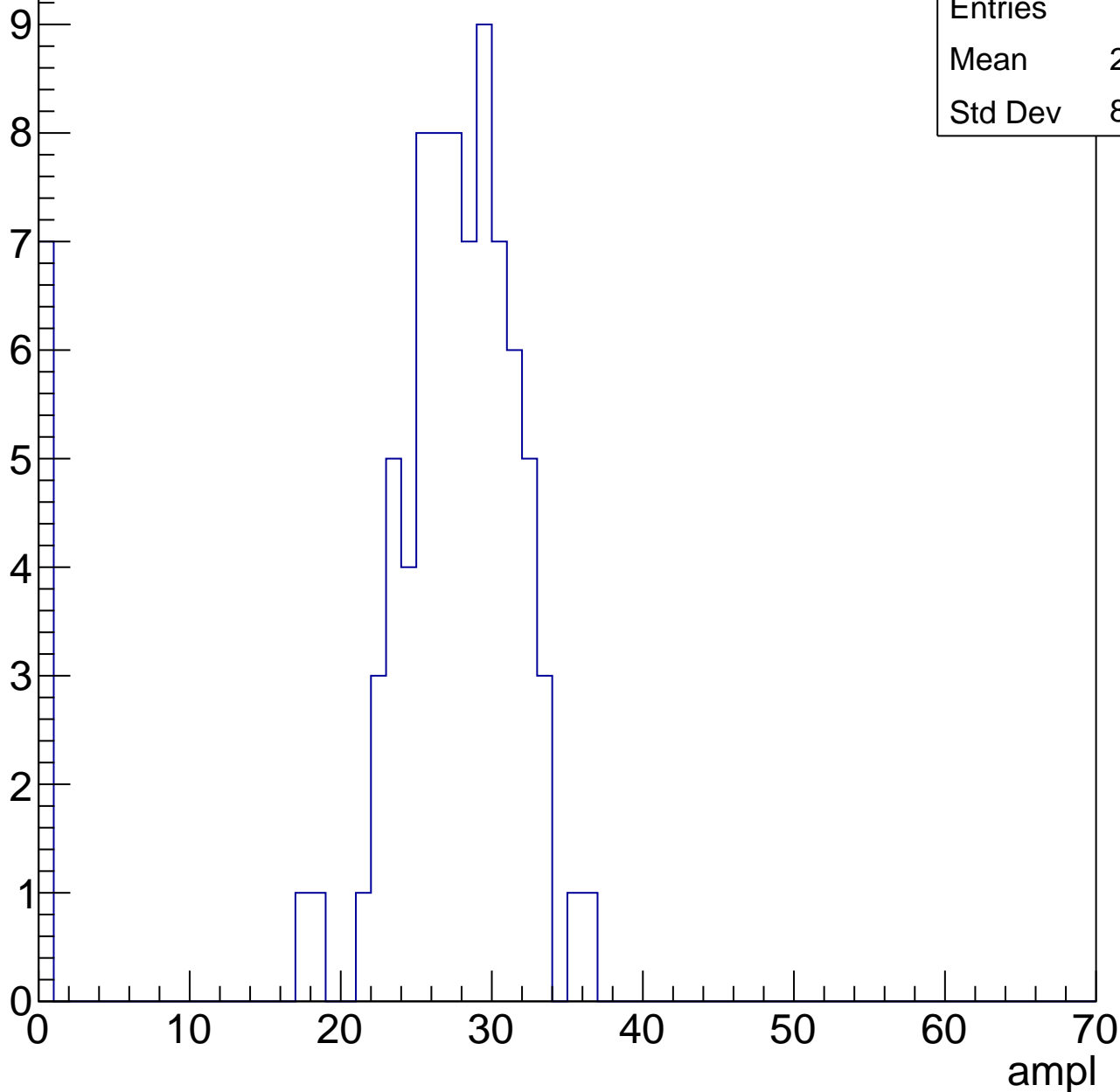


B1L103S, U12-ch110, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	85
Mean	25.18
Std Dev	8.295

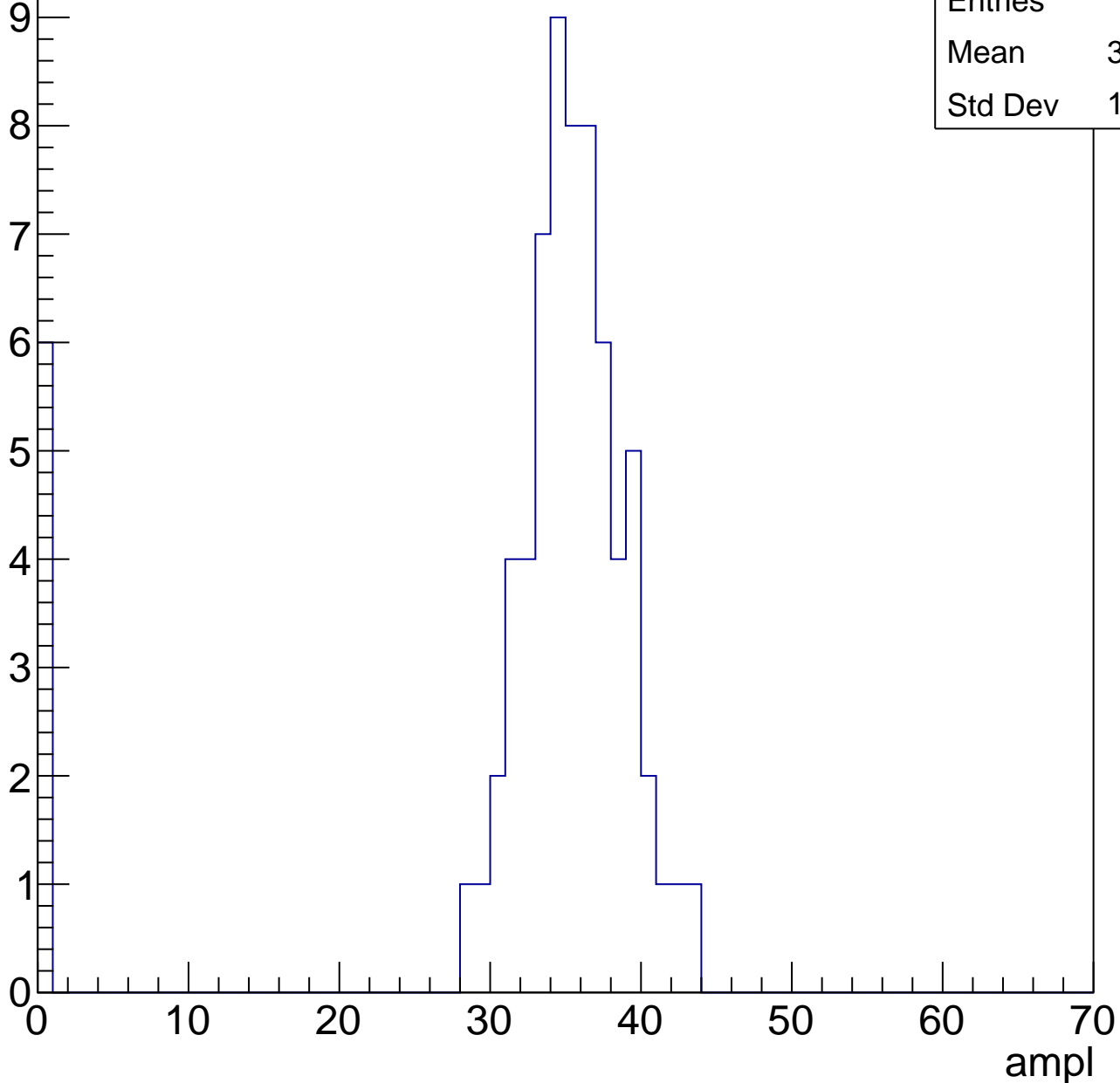


B1L103S, U12-ch110, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	32.13
Std Dev	10.28

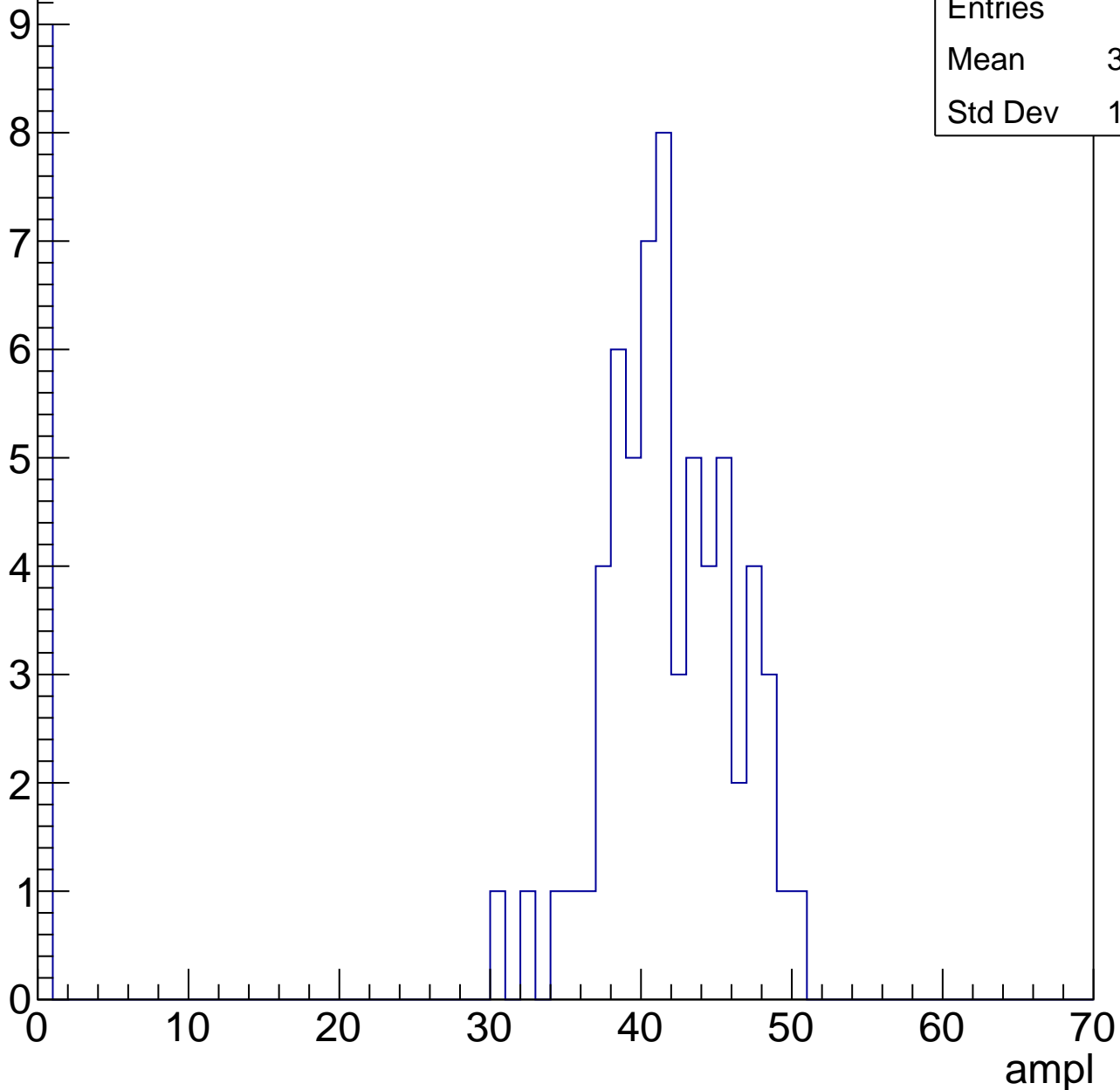


B1L103S, U12-ch110, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	72
Mean	36.26
Std Dev	14.24

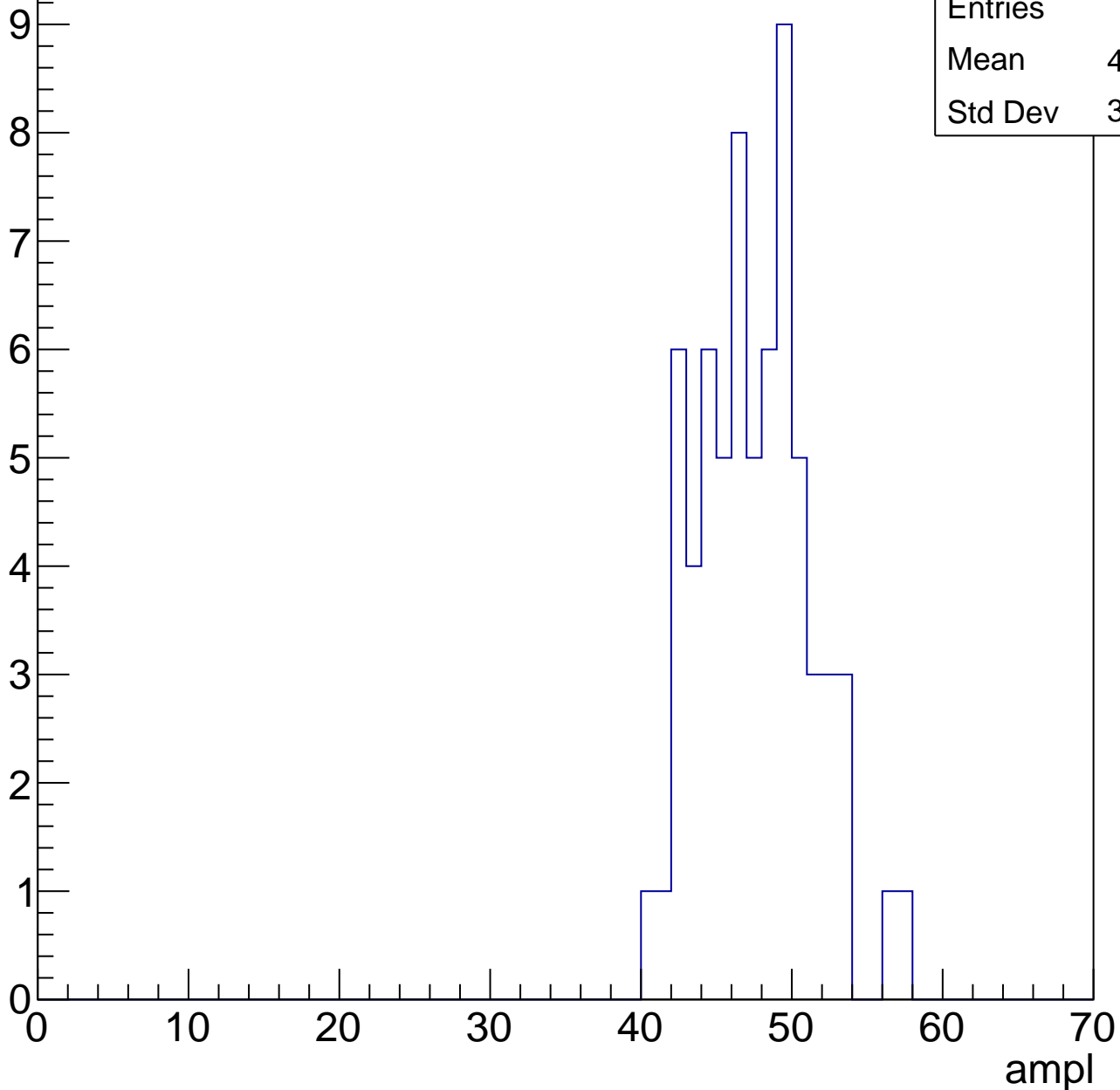


B1L103S, U12-ch110, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	47.12
Std Dev	3.622

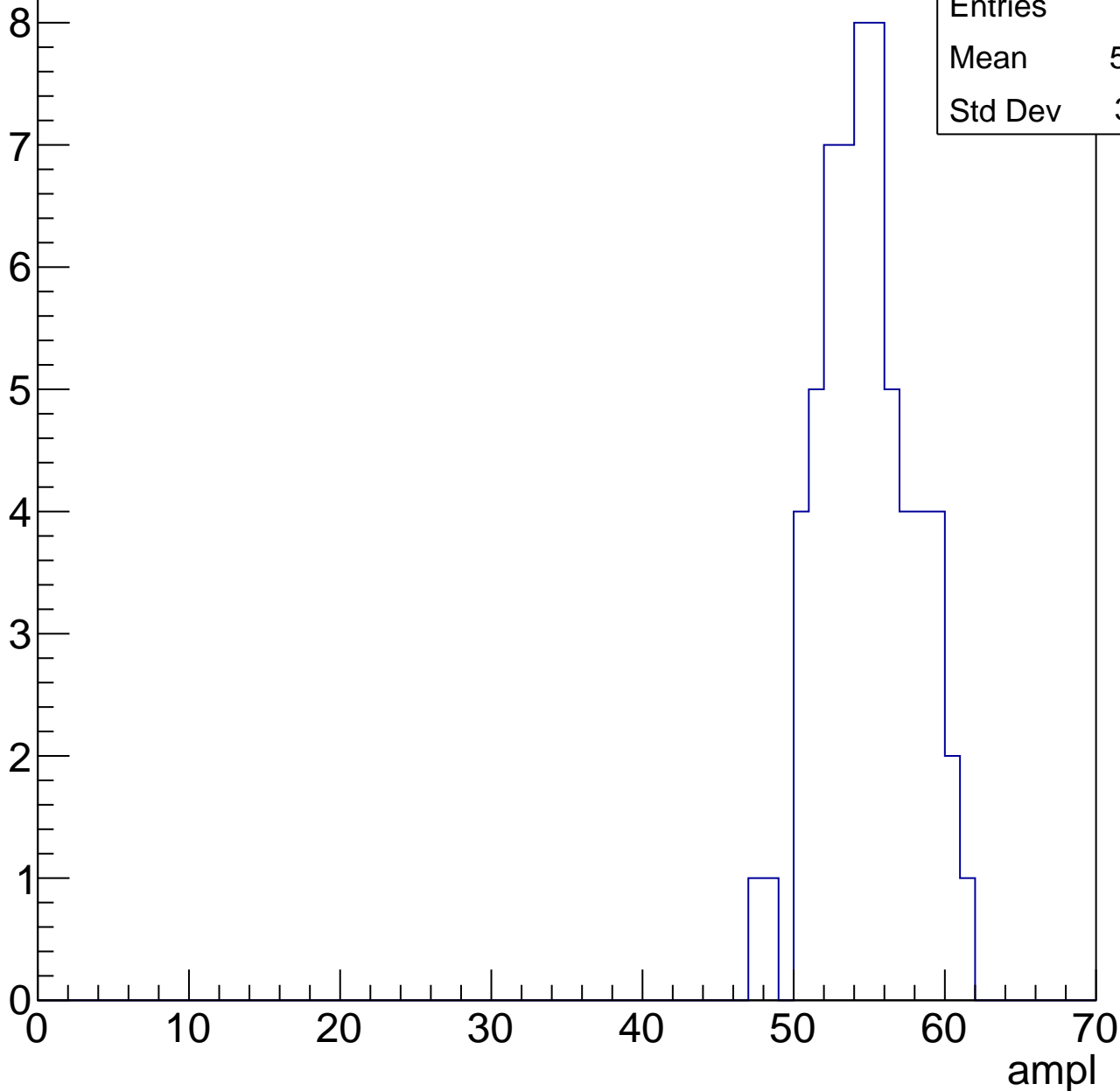


B1L103S, U12-ch110, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	54.33
Std Dev	3.061

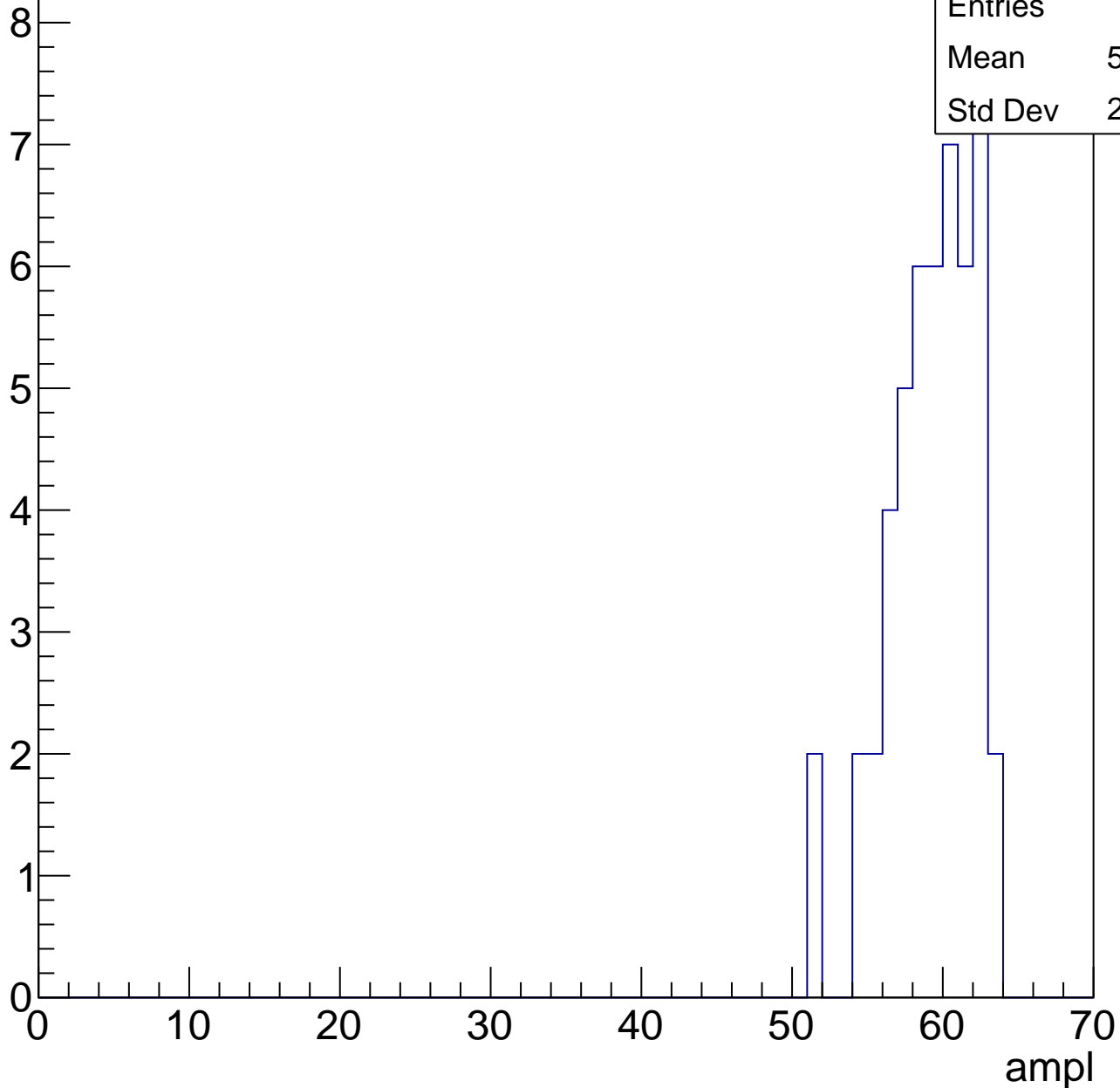


B1L103S, U12-ch110, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

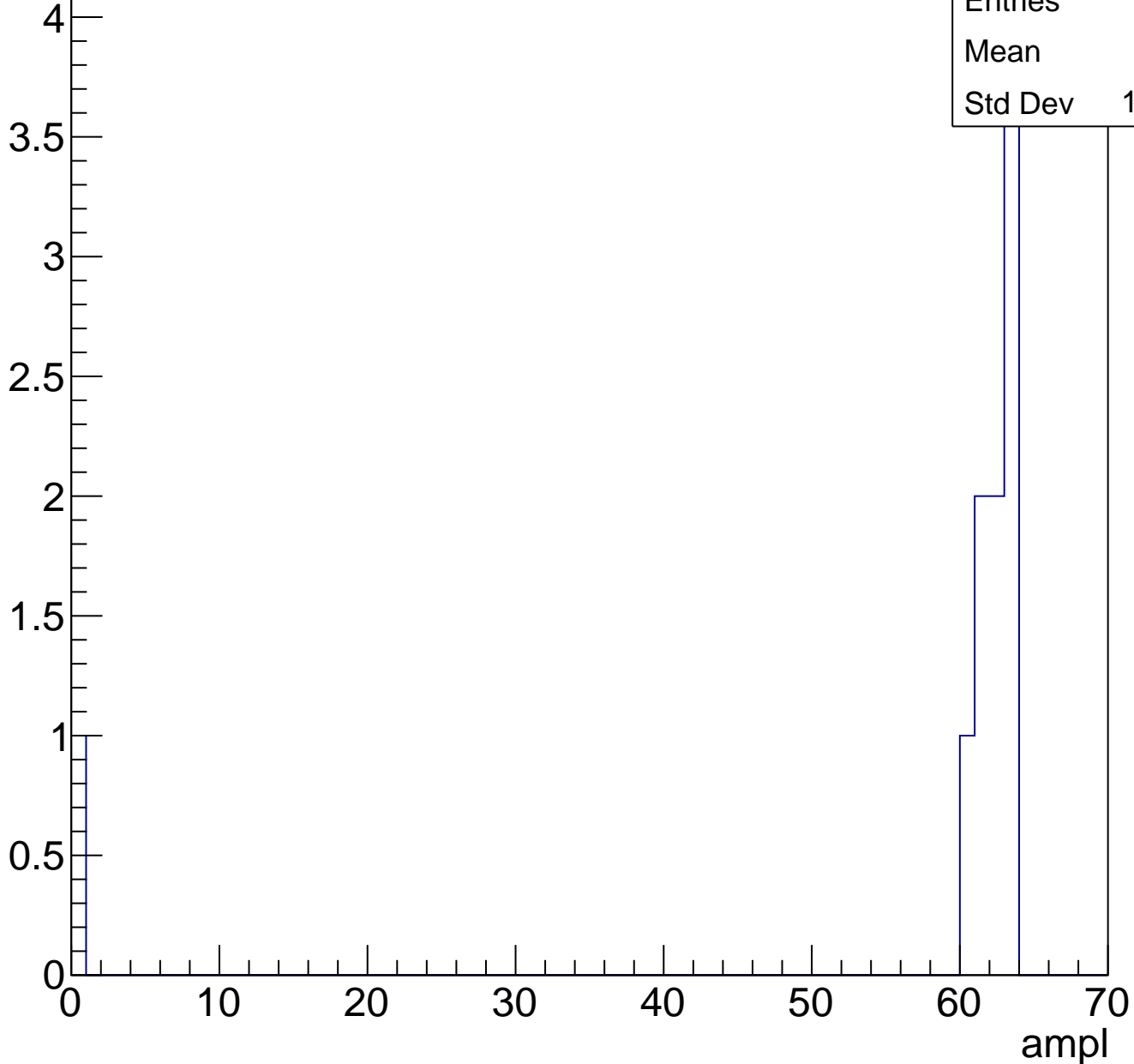
Entries	50
Mean	58.78
Std Dev	2.845



B1L103S, U12-ch110, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

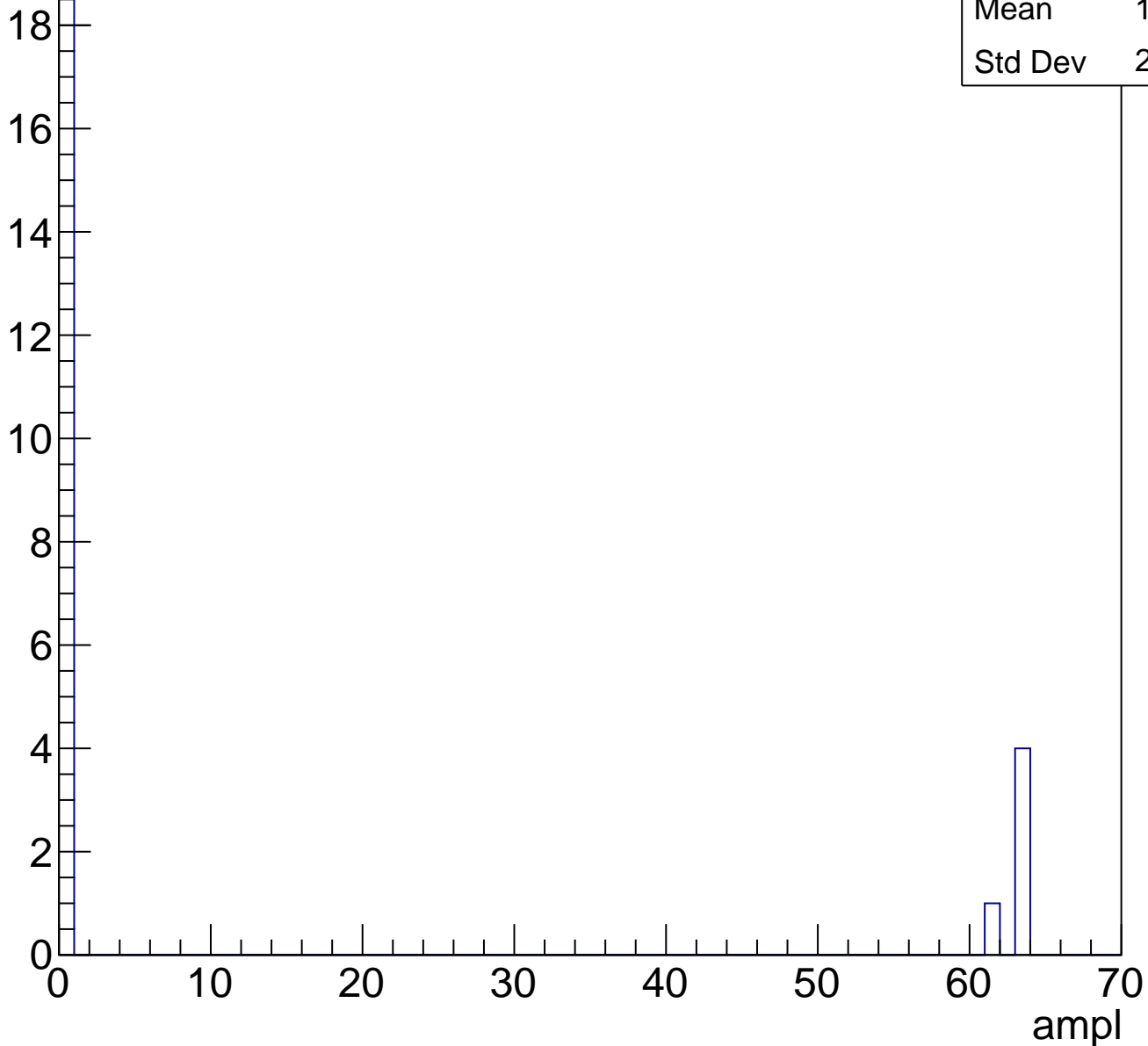


B1L103S, U12-ch110, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	24
Mean	13.04
Std Dev	25.43

Entry



B1L103S, U12-ch111, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	82
Mean	20.26
Std Dev	14.56

Entry

25

20

15

10

5

0

0

10

20

30

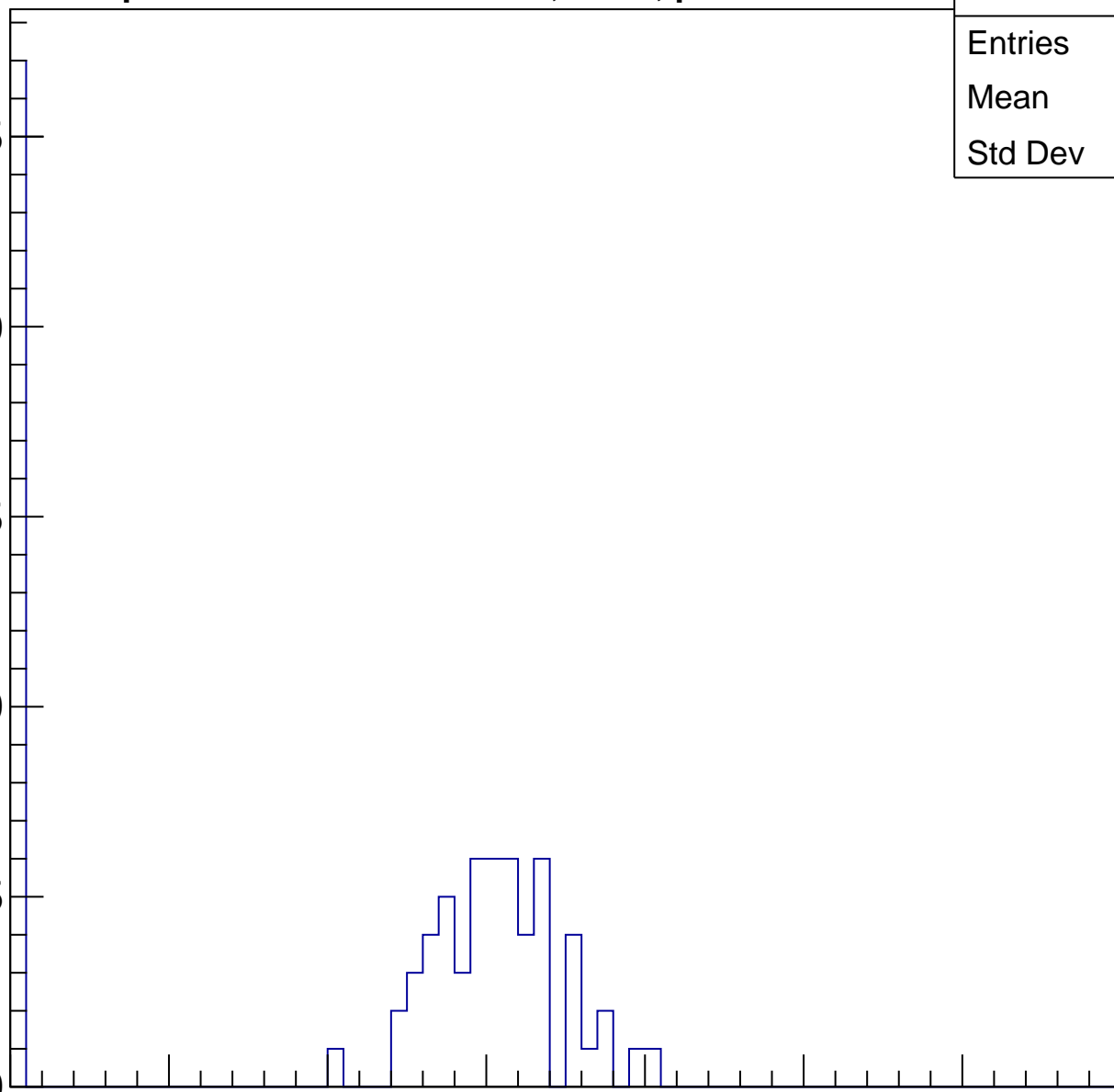
40

50

60

70

ampl

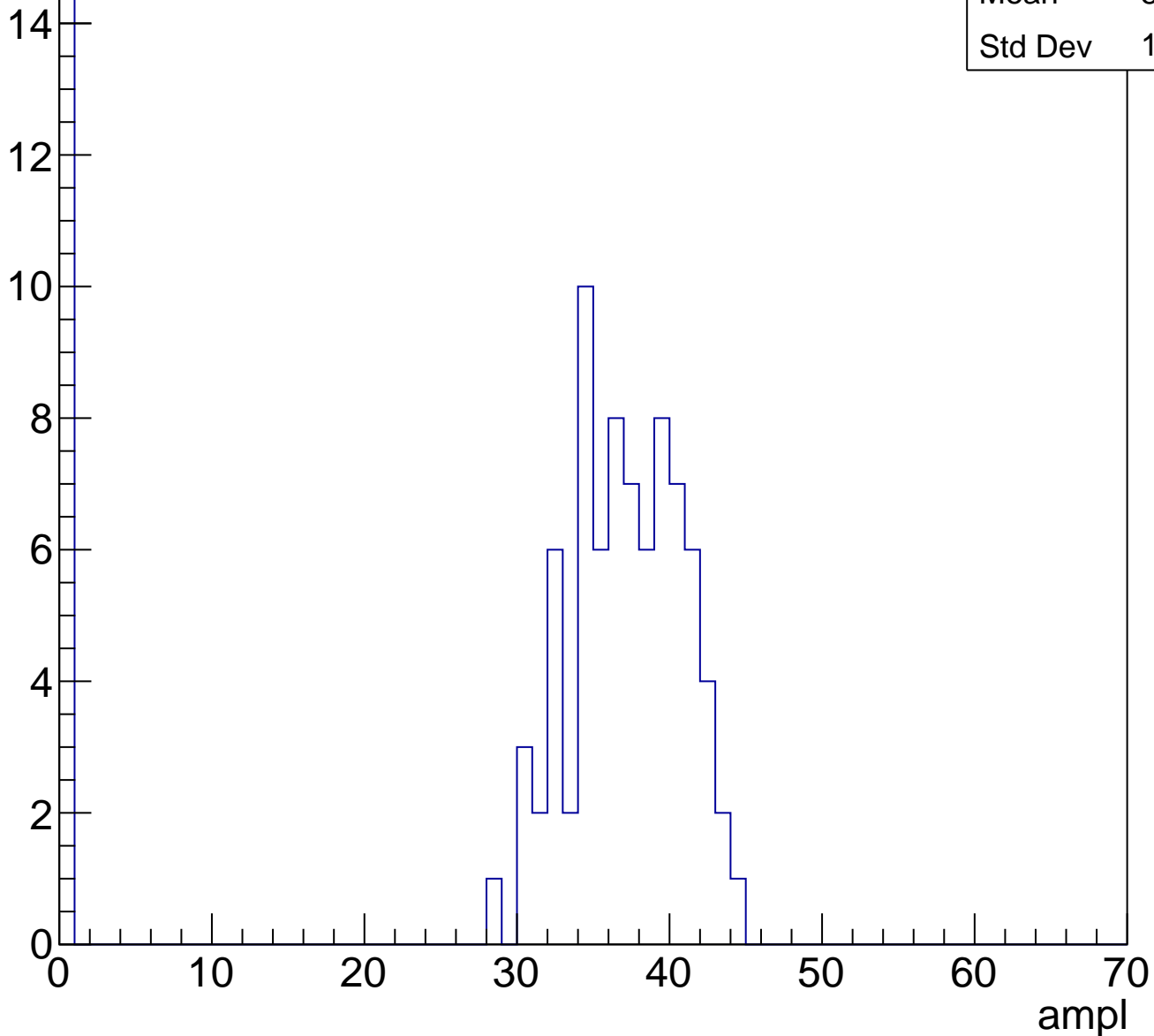


B1L103S, U12-ch111, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	94
Mean	30.84
Std Dev	13.83

Entry

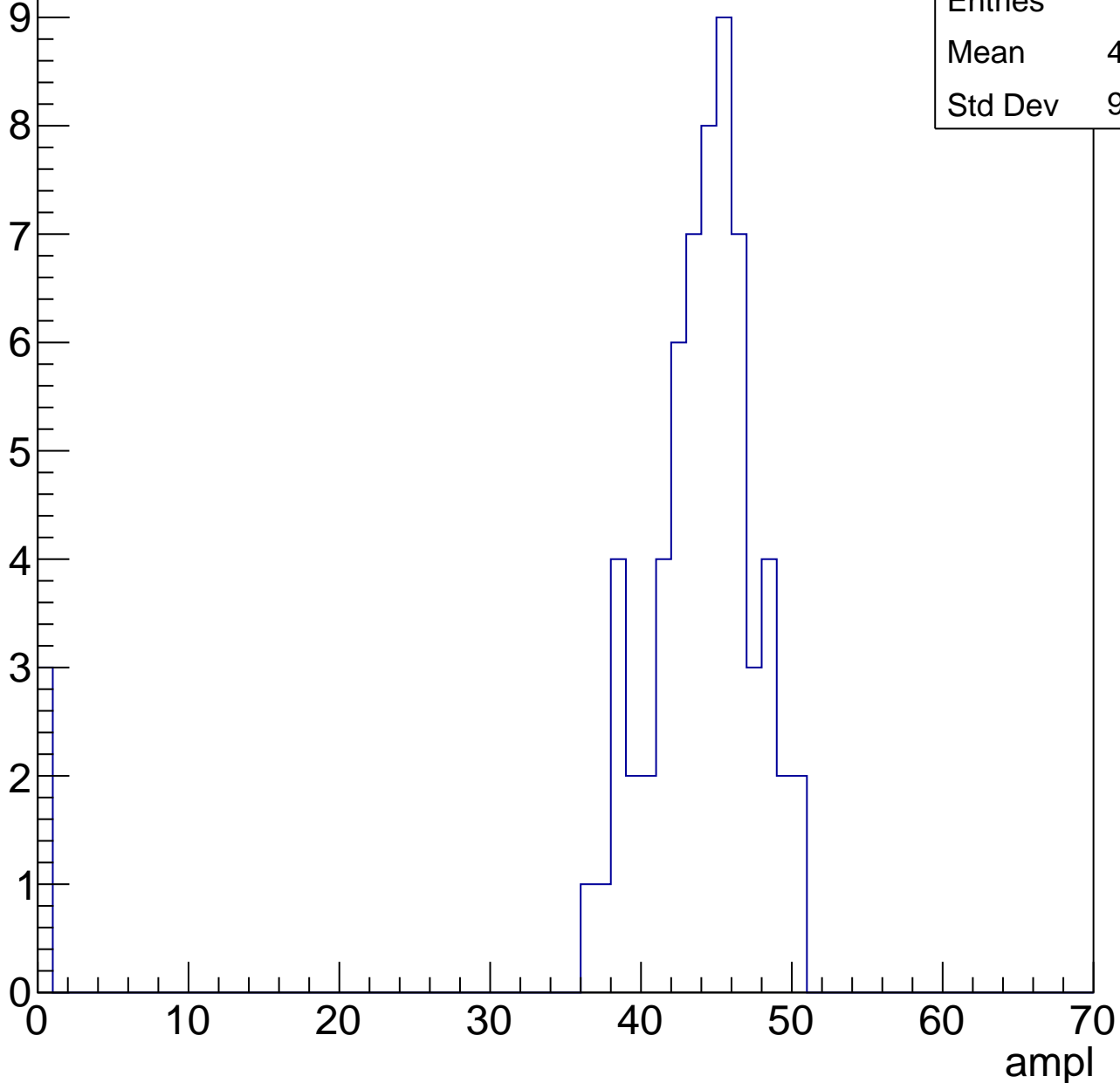


B1L103S, U12-ch111, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	41.69
Std Dev	9.702

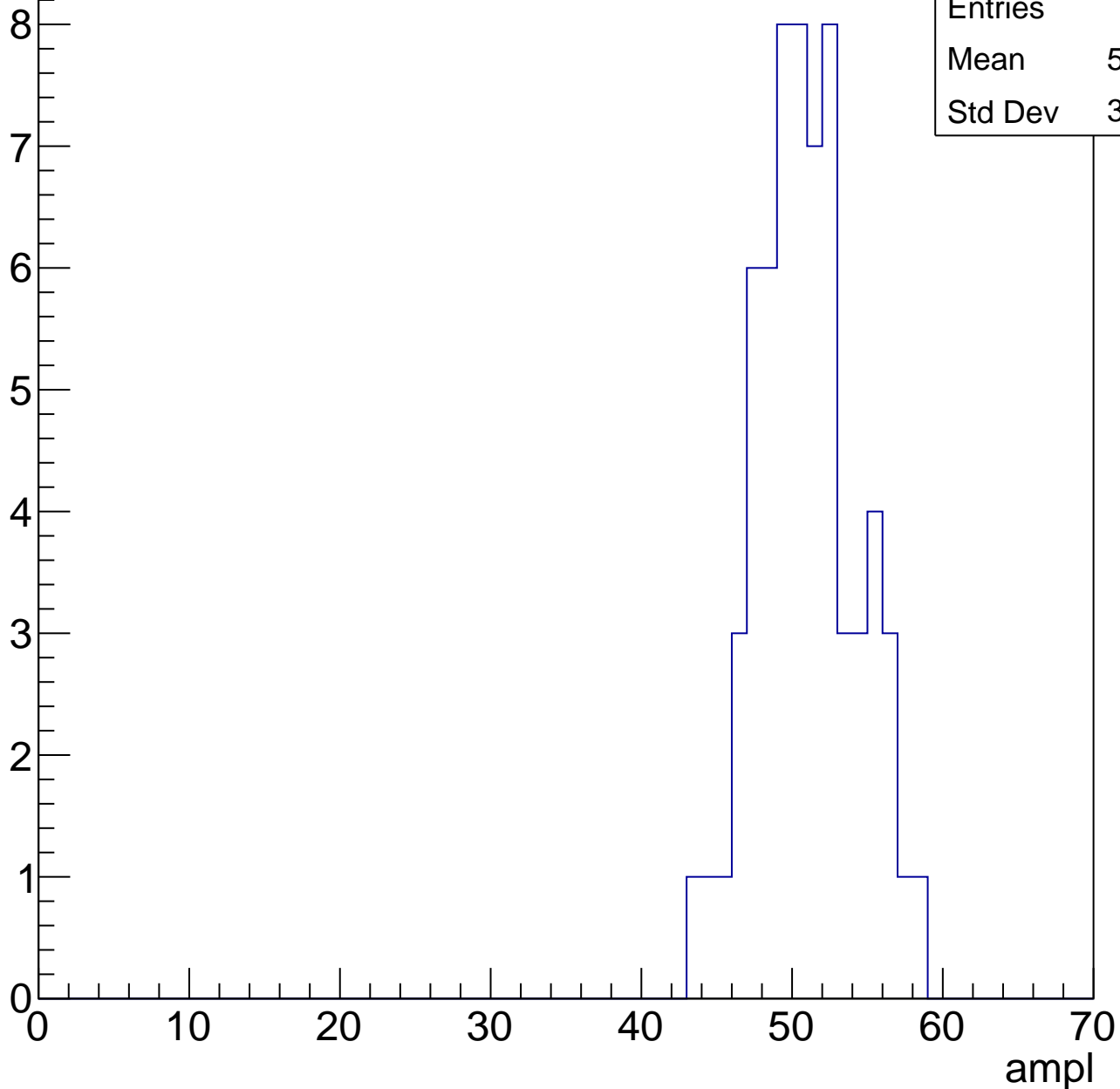


B1L103S, U12-ch111, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	50.45
Std Dev	3.226

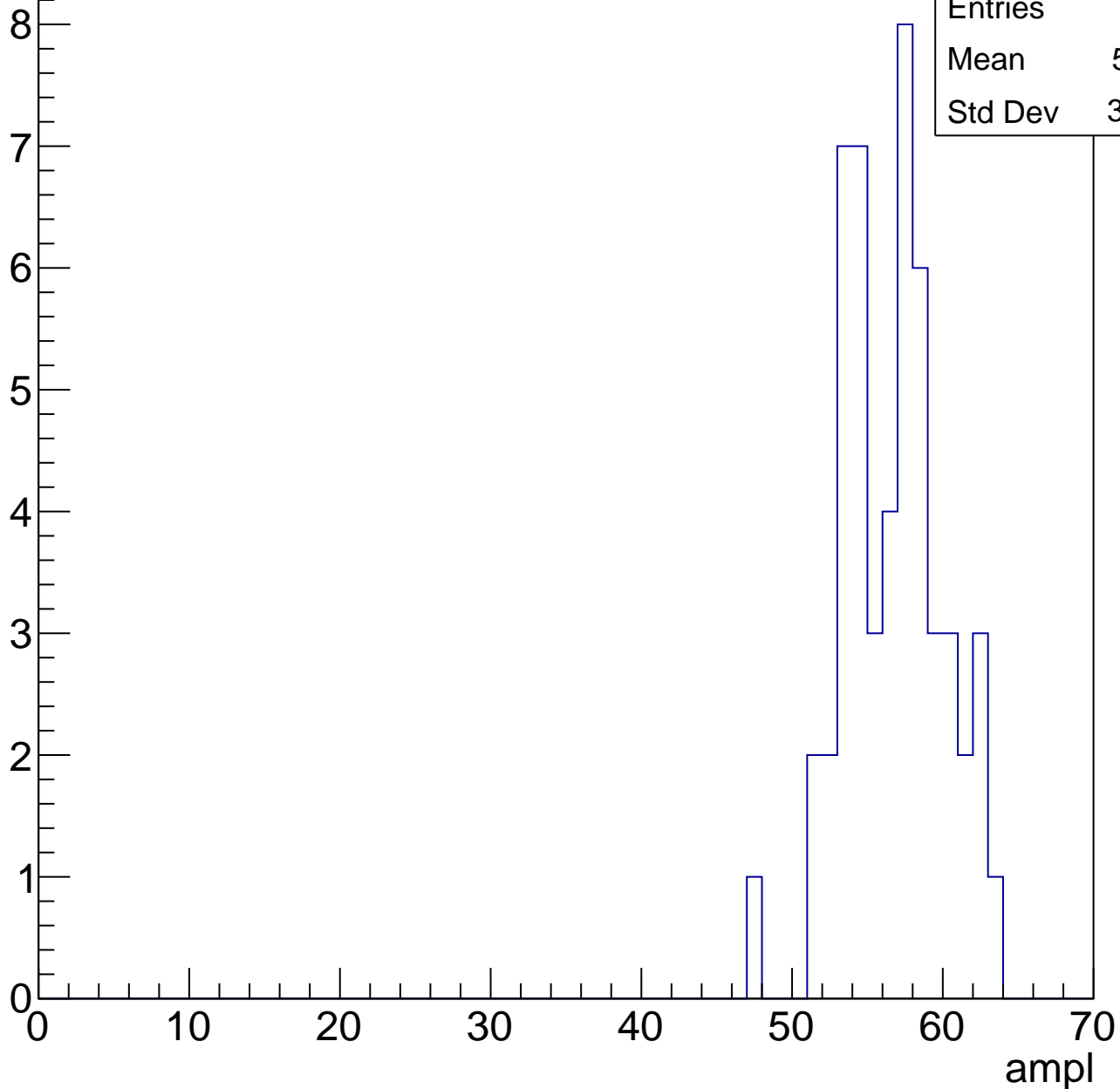


B1L103S, U12-ch111, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	52
Mean	56.21
Std Dev	3.307

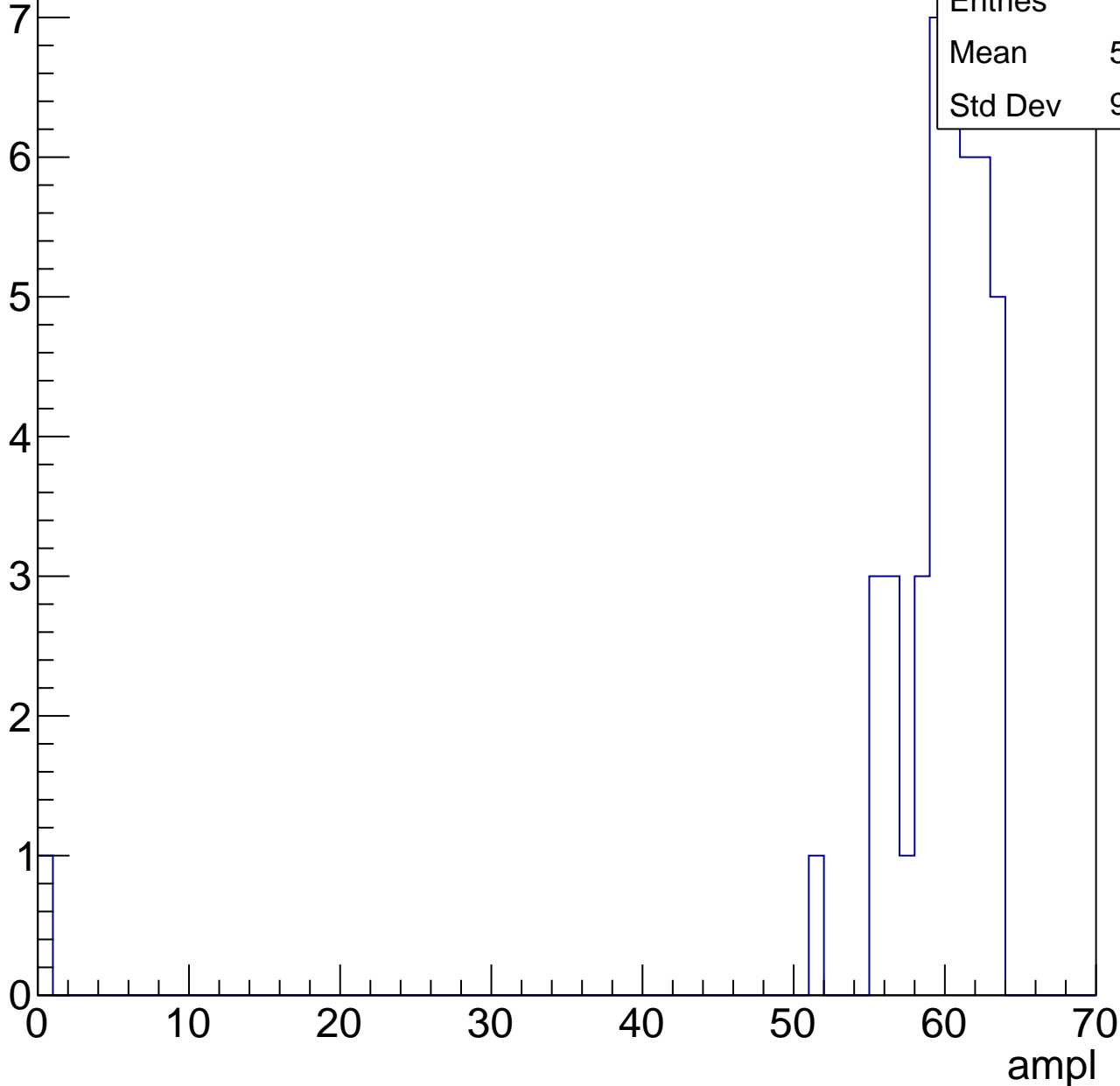


B1L103S, U12-ch111, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

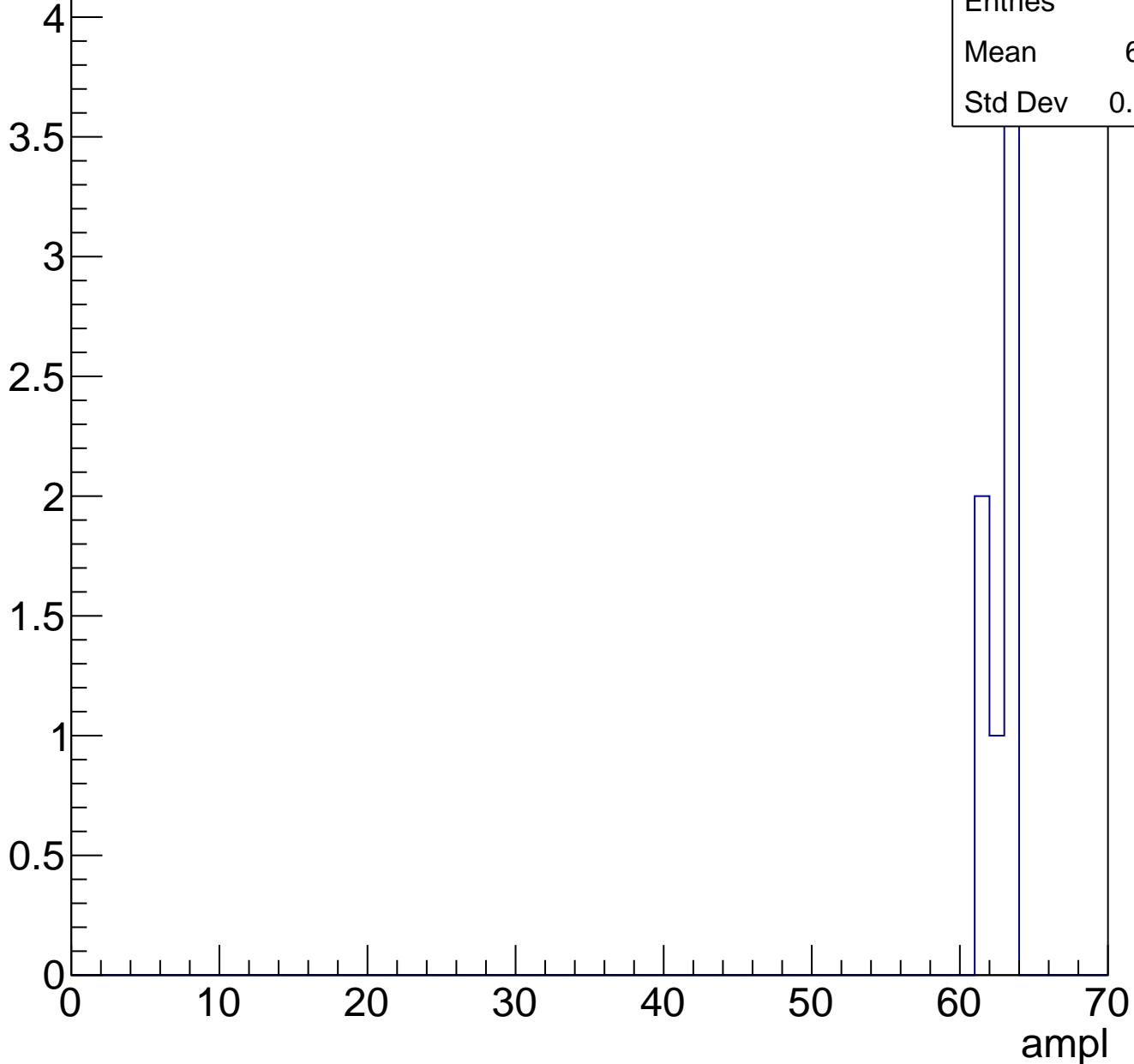
Entries	43
Mean	58.16
Std Dev	9.353



B1L103S, U12-ch111, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



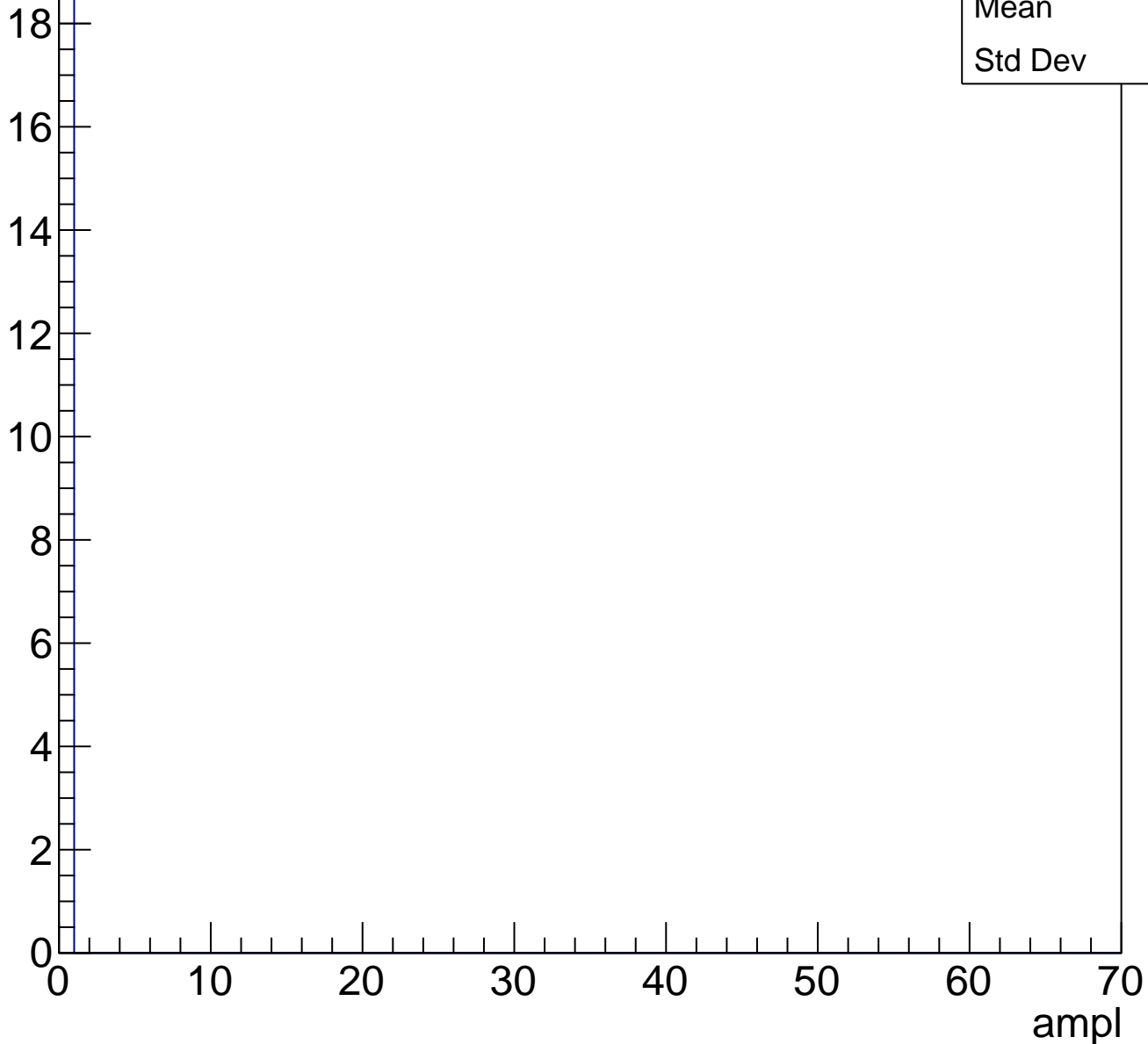
Entries	7
Mean	62.29
Std Dev	0.8806

B1L103S, U12-ch111, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	0
Std Dev	0

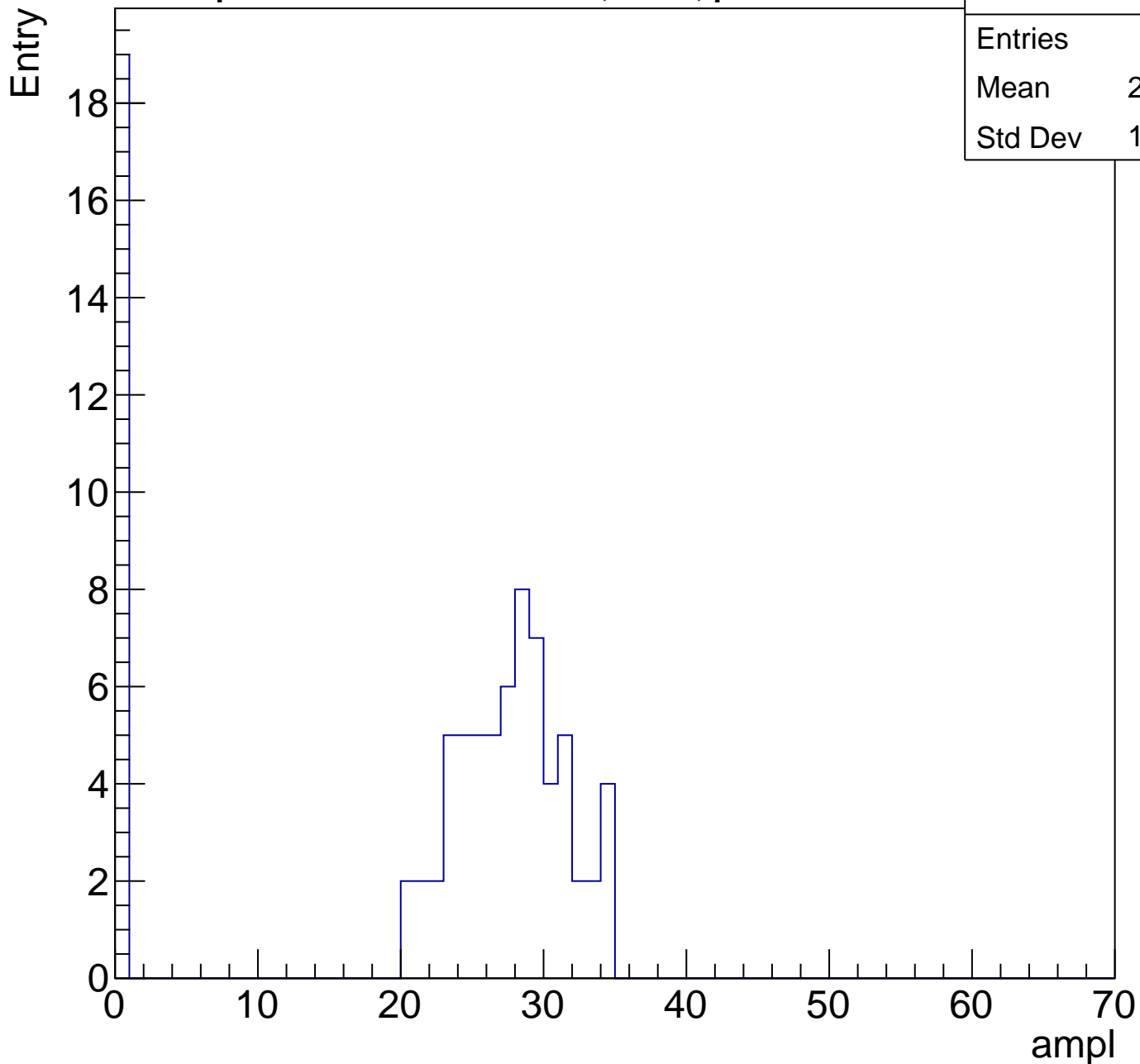
Entry



B1L103S, U12-ch112, adc0

calib_packv5_041523_1651.root, FC#0, port C2

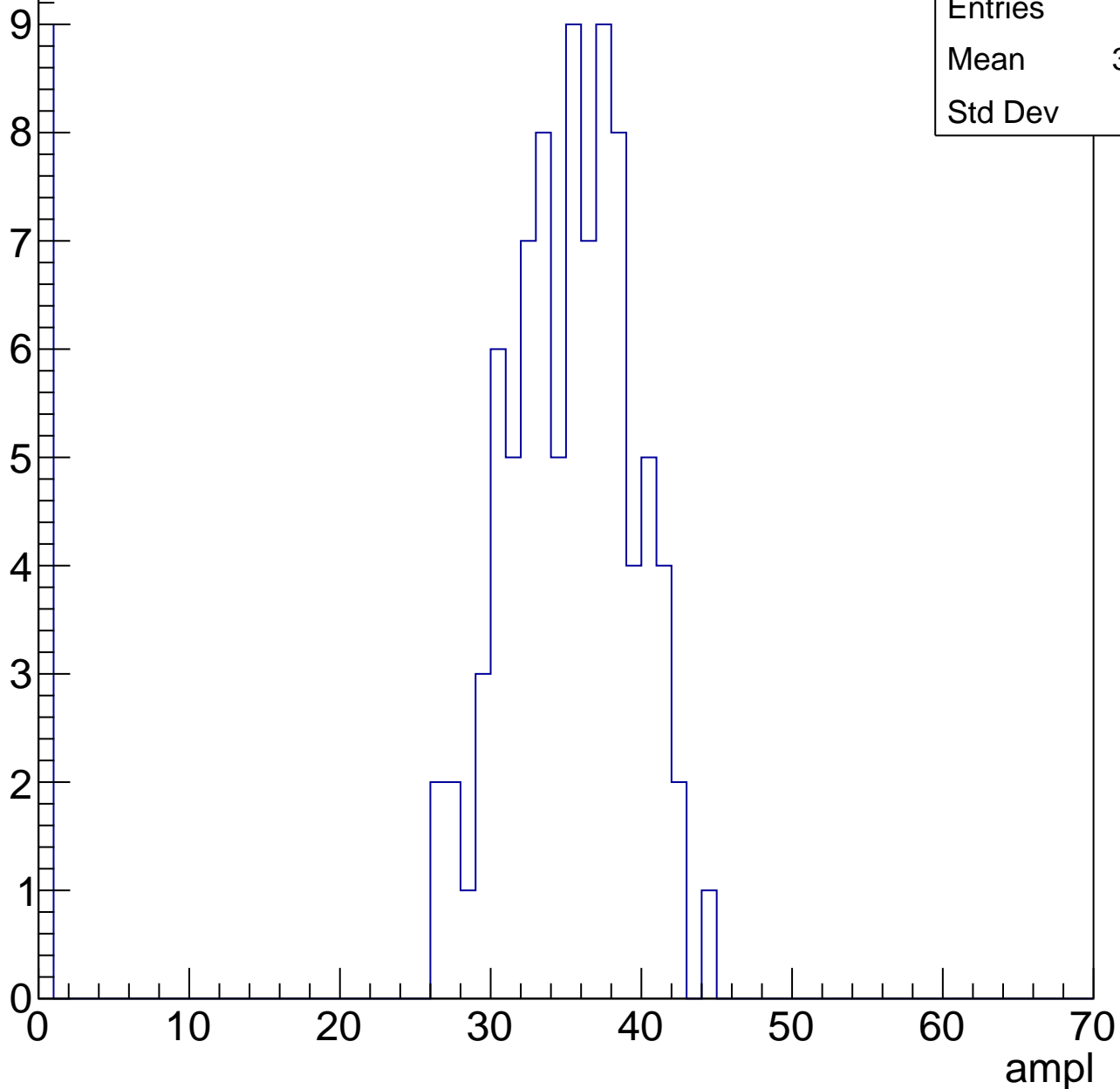
Entries	83
Mean	21.04
Std Dev	11.89



B1L103S, U12-ch112, adc1

calib_packv5_041523_1651.root, FC#0, port C2

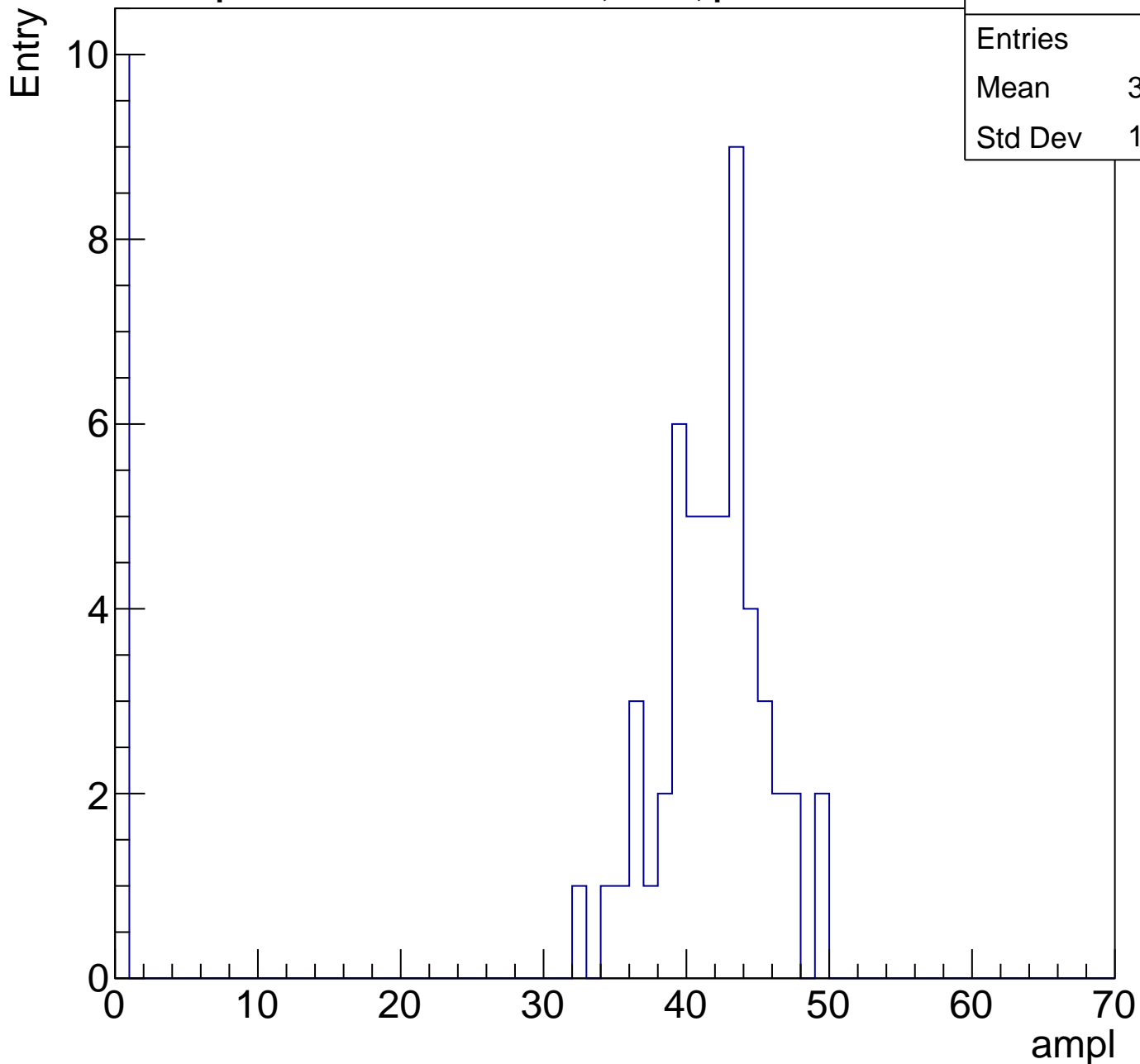
Entry



B1L103S, U12-ch112, adc2

calib_packv5_041523_1651.root, FC#0, port C2

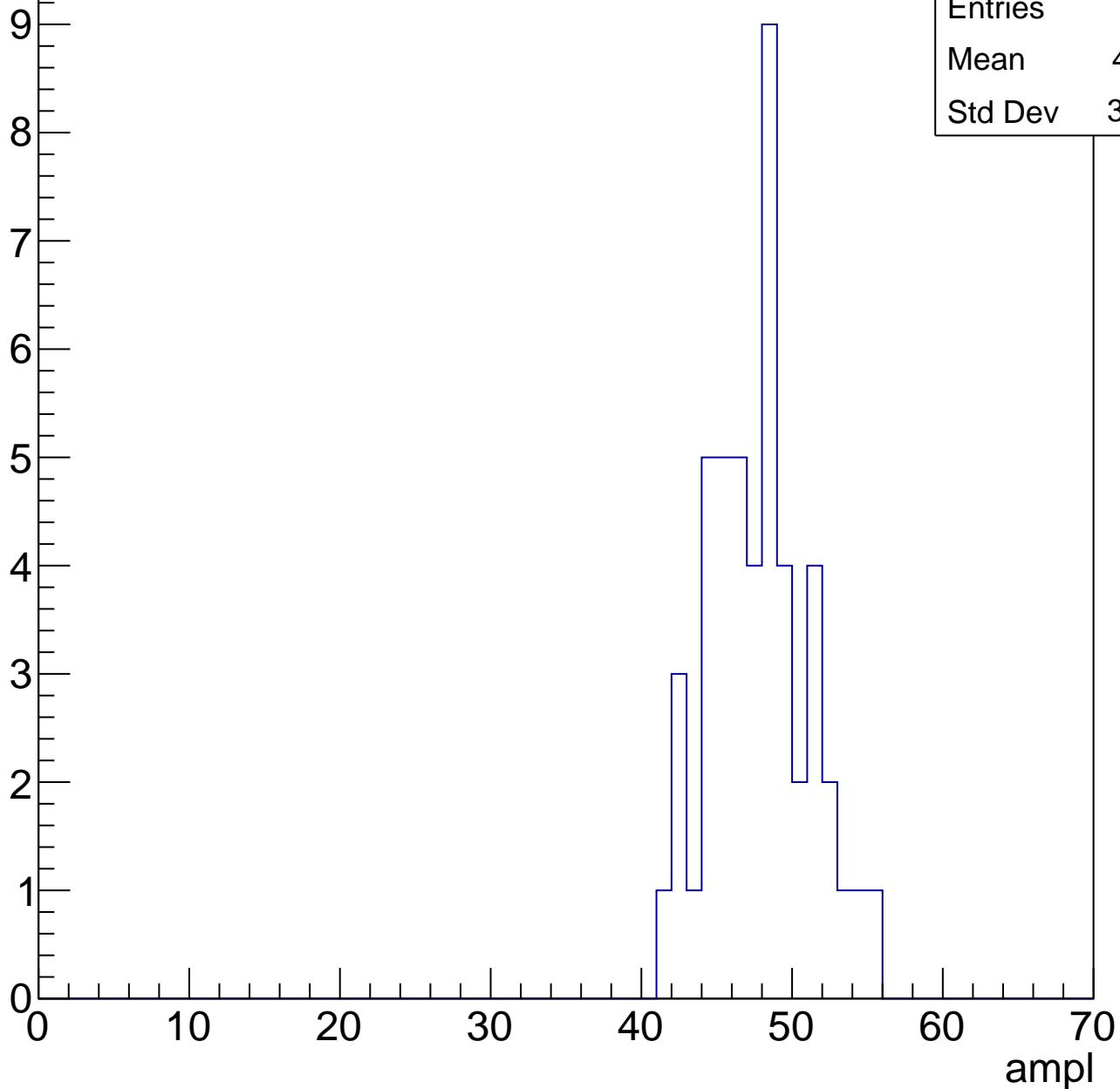
Entries	62
Mean	34.73
Std Dev	15.58



B1L103S, U12-ch112, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

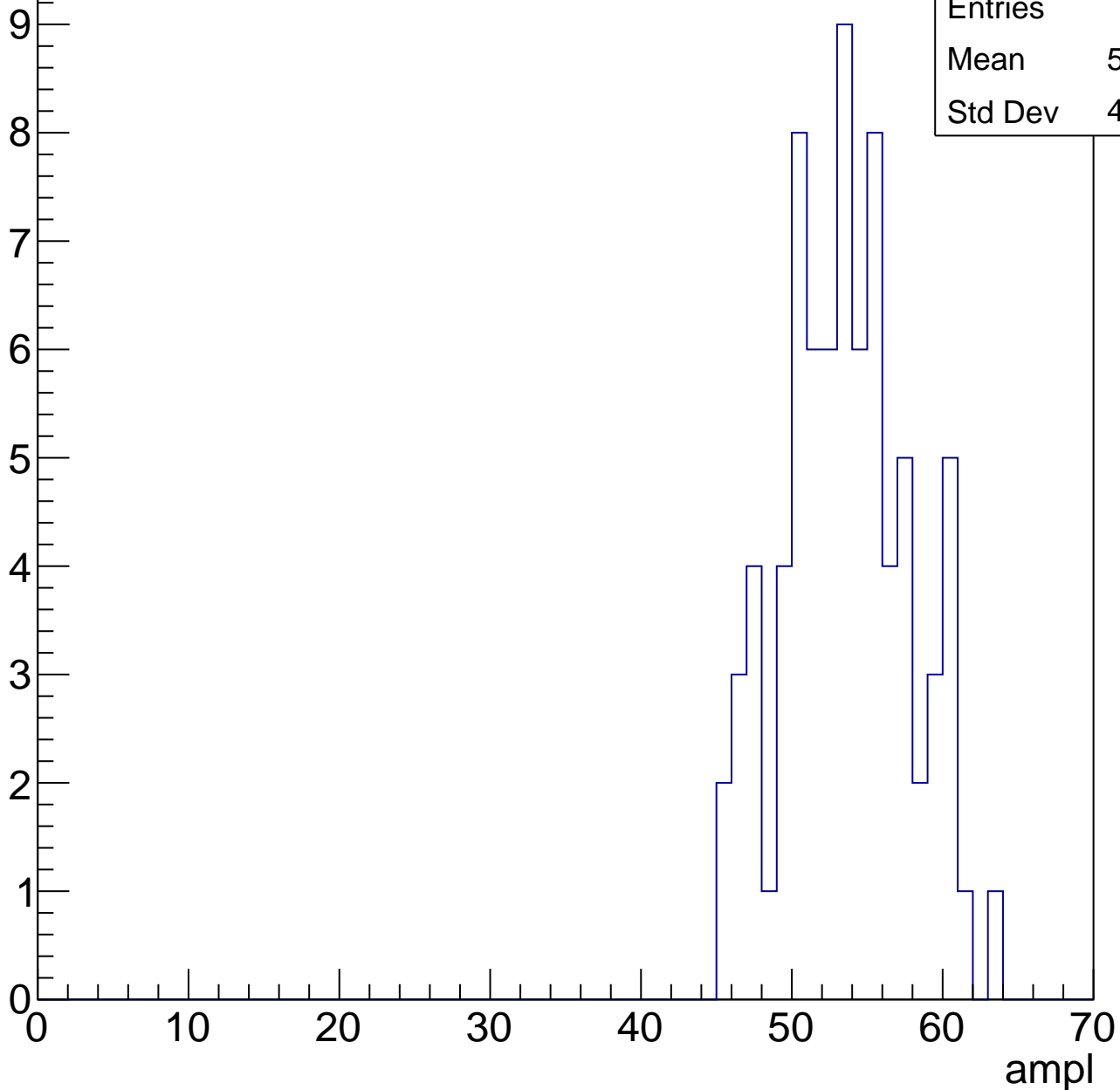


B1L103S, U12-ch112, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	78
Mean	53.14
Std Dev	4.128

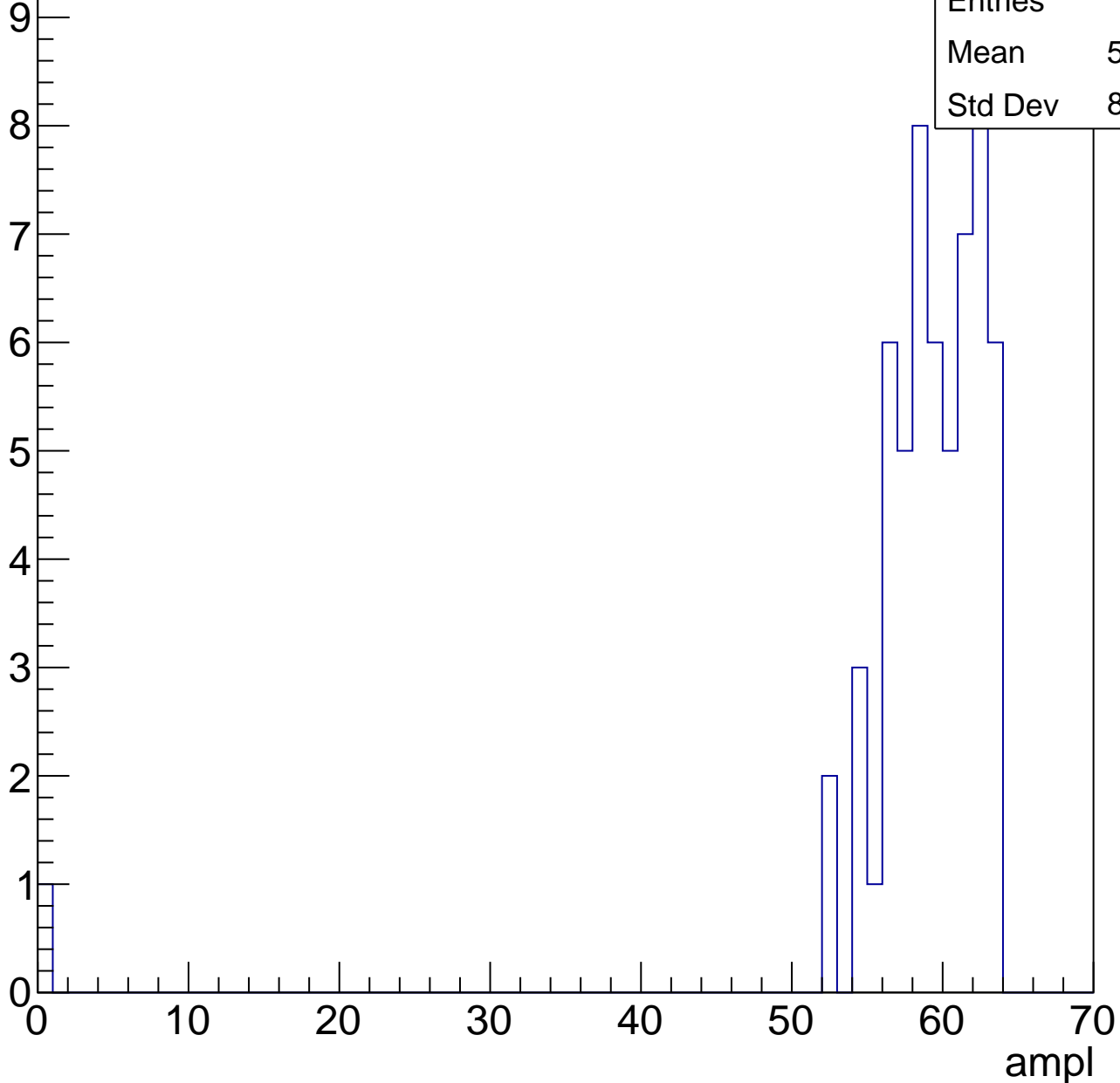


B1L103S, U12-ch112, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

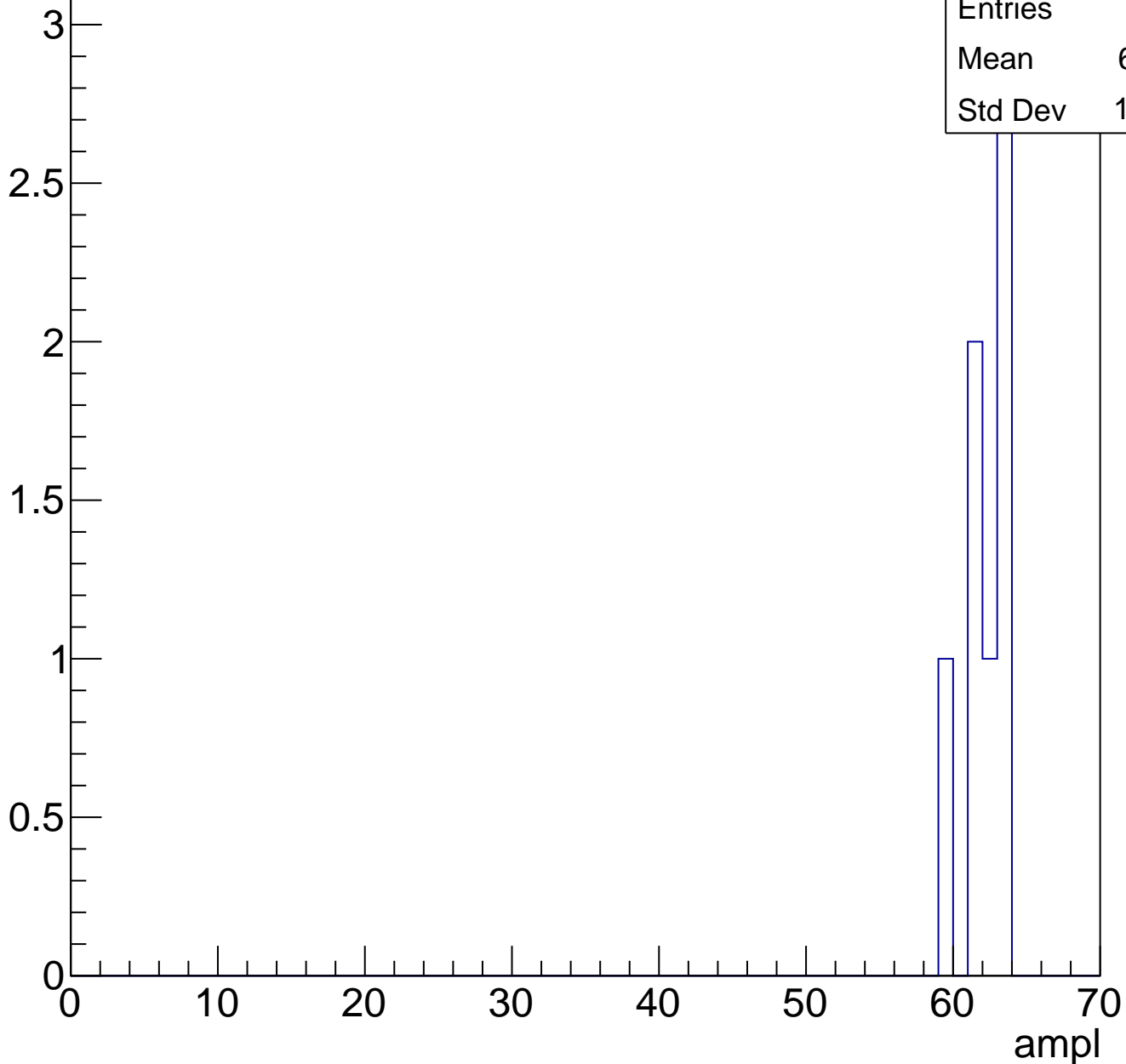
Entries	59
Mean	58.02
Std Dev	8.135



B1L103S, U12-ch112, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch112, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

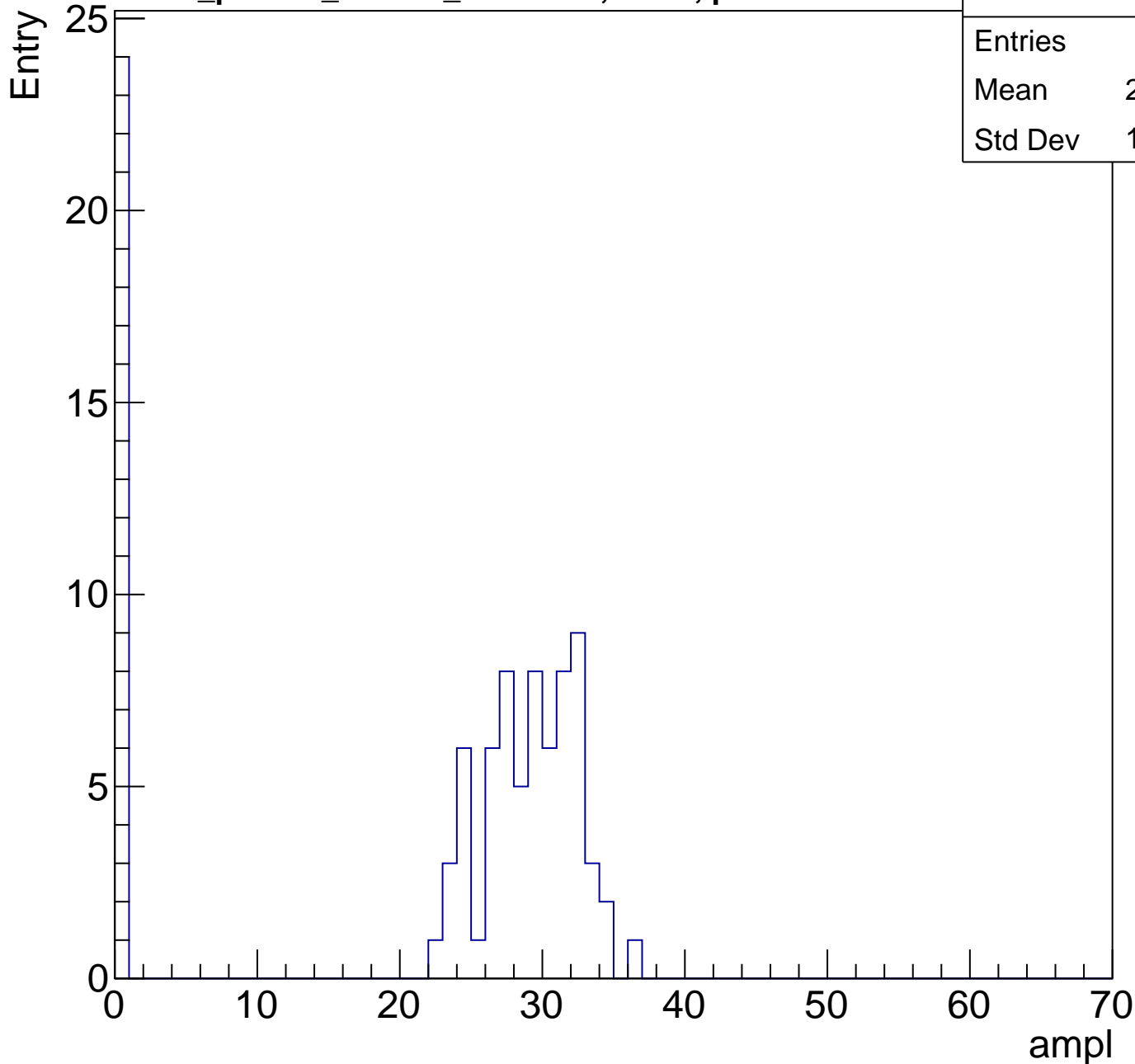
Entries	19
Mean	0
Std Dev	0

ampl

B1L103S, U12-ch113, adc0

calib_packv5_041523_1651.root, FC#0, port C2

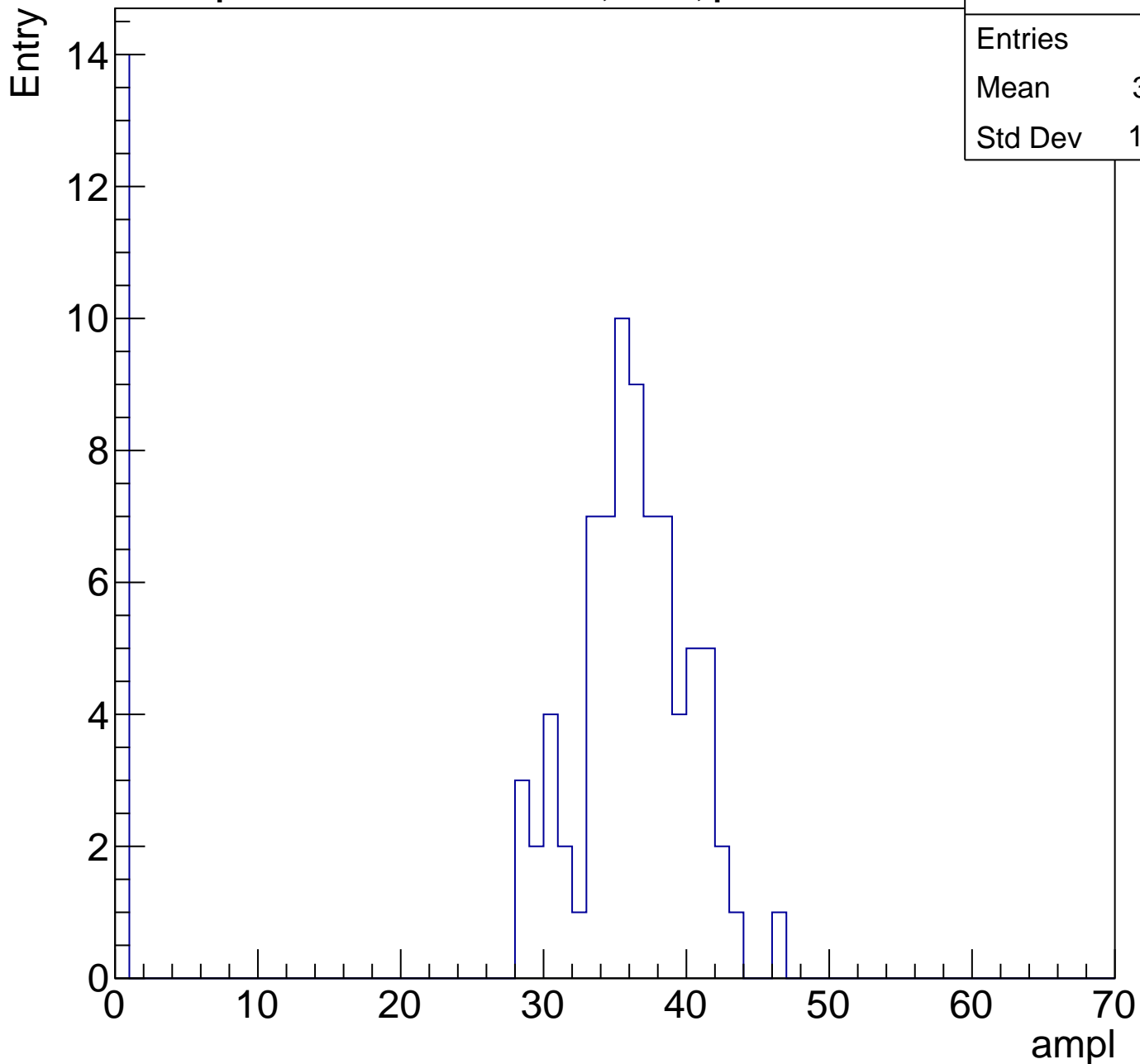
Entries	91
Mean	21.13
Std Dev	12.94



B1L103S, U12-ch113, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	91
Mean	30.31
Std Dev	13.38

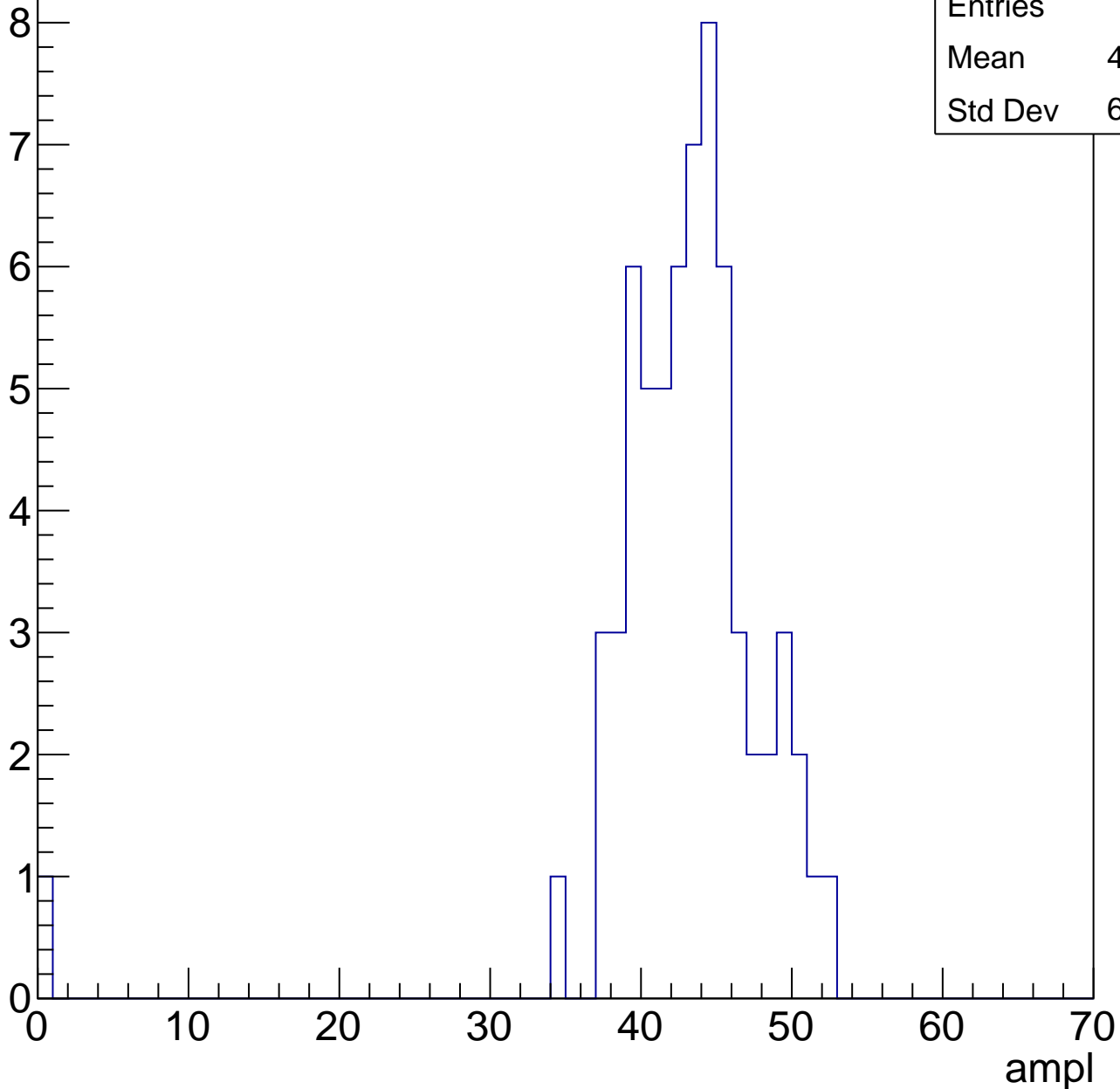


B1L103S, U12-ch113, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	42.32
Std Dev	6.495

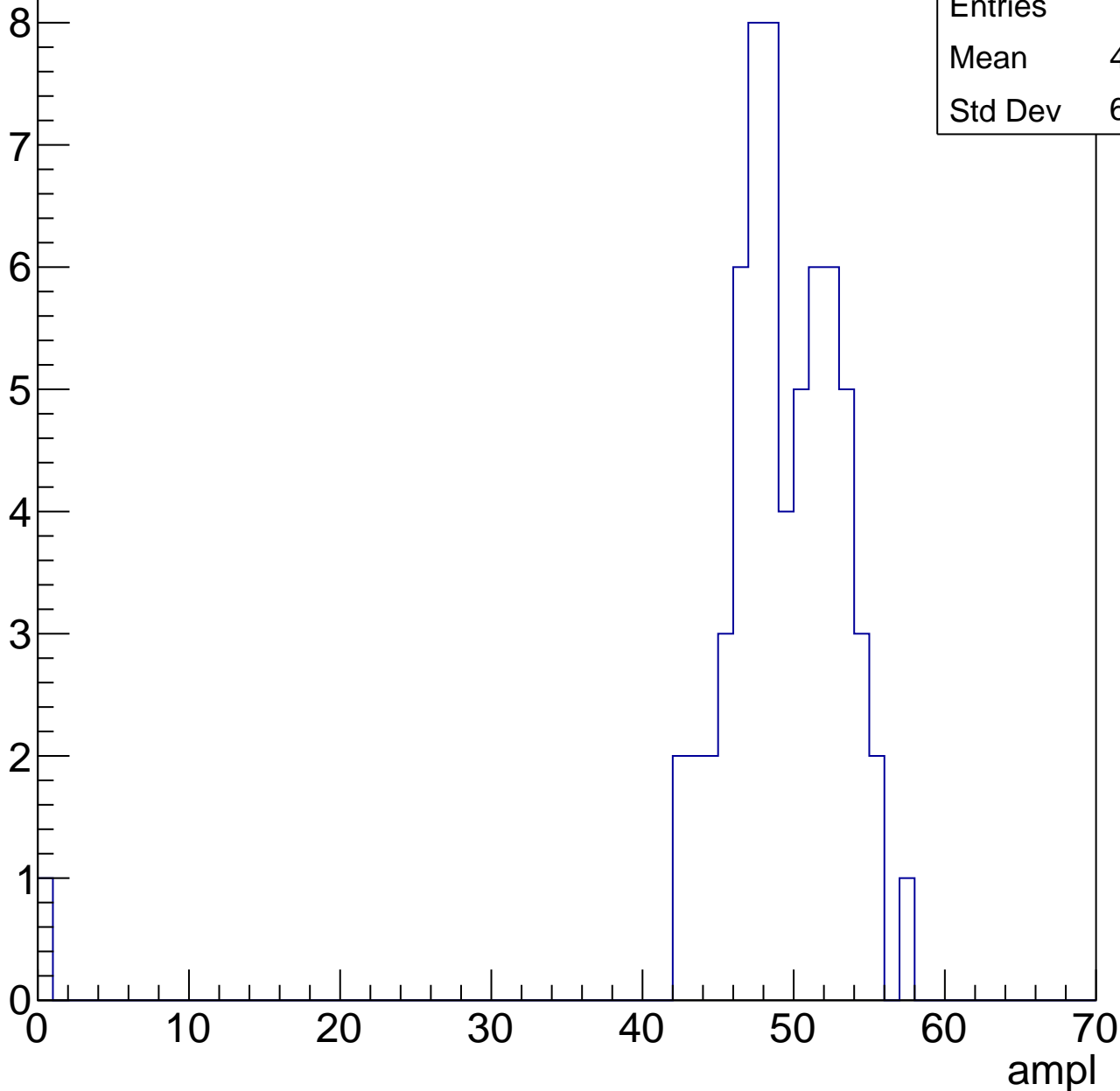


B1L103S, U12-ch113, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	48.23
Std Dev	6.959

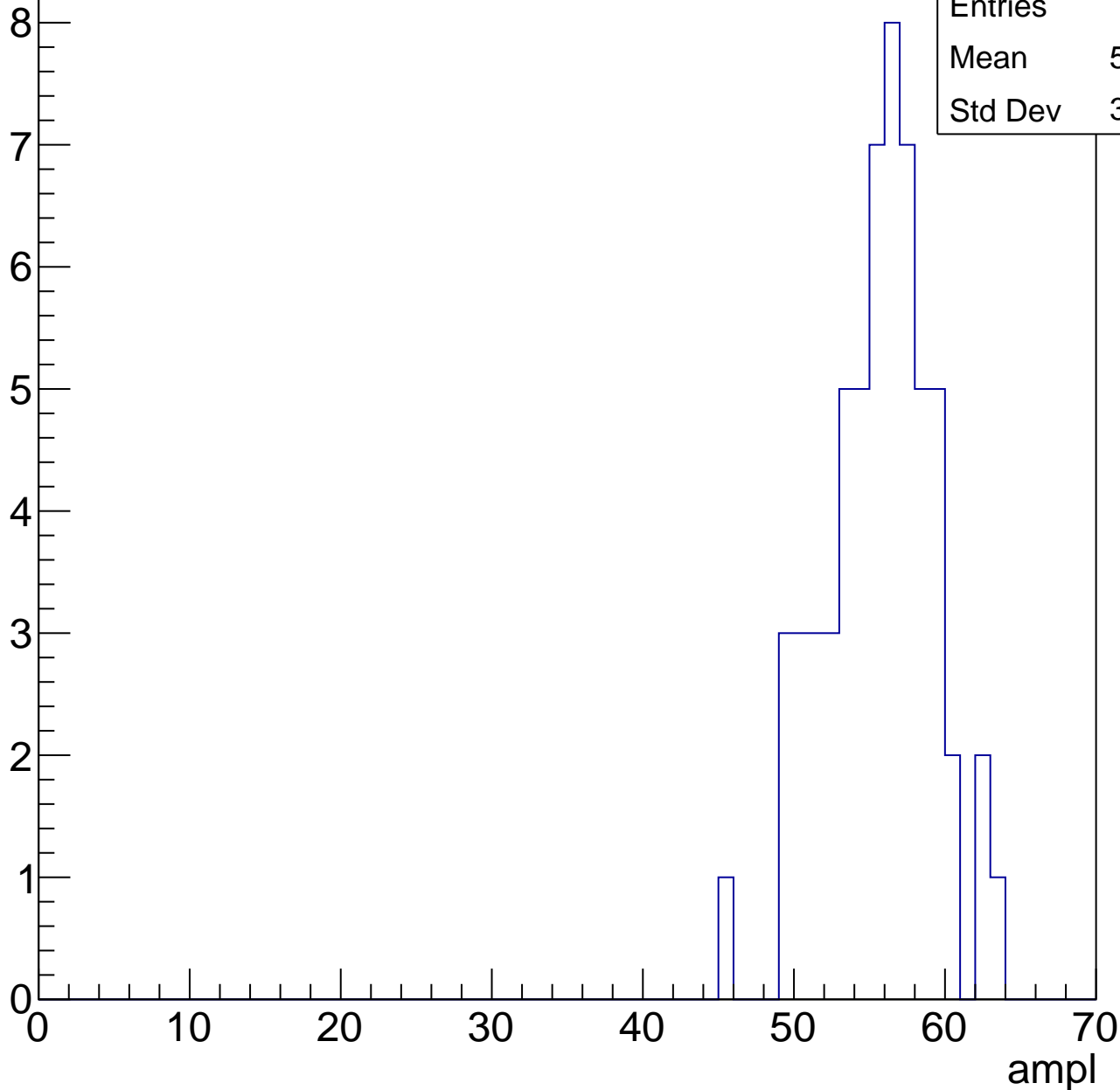


B1L103S, U12-ch113, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	55.17
Std Dev	3.546

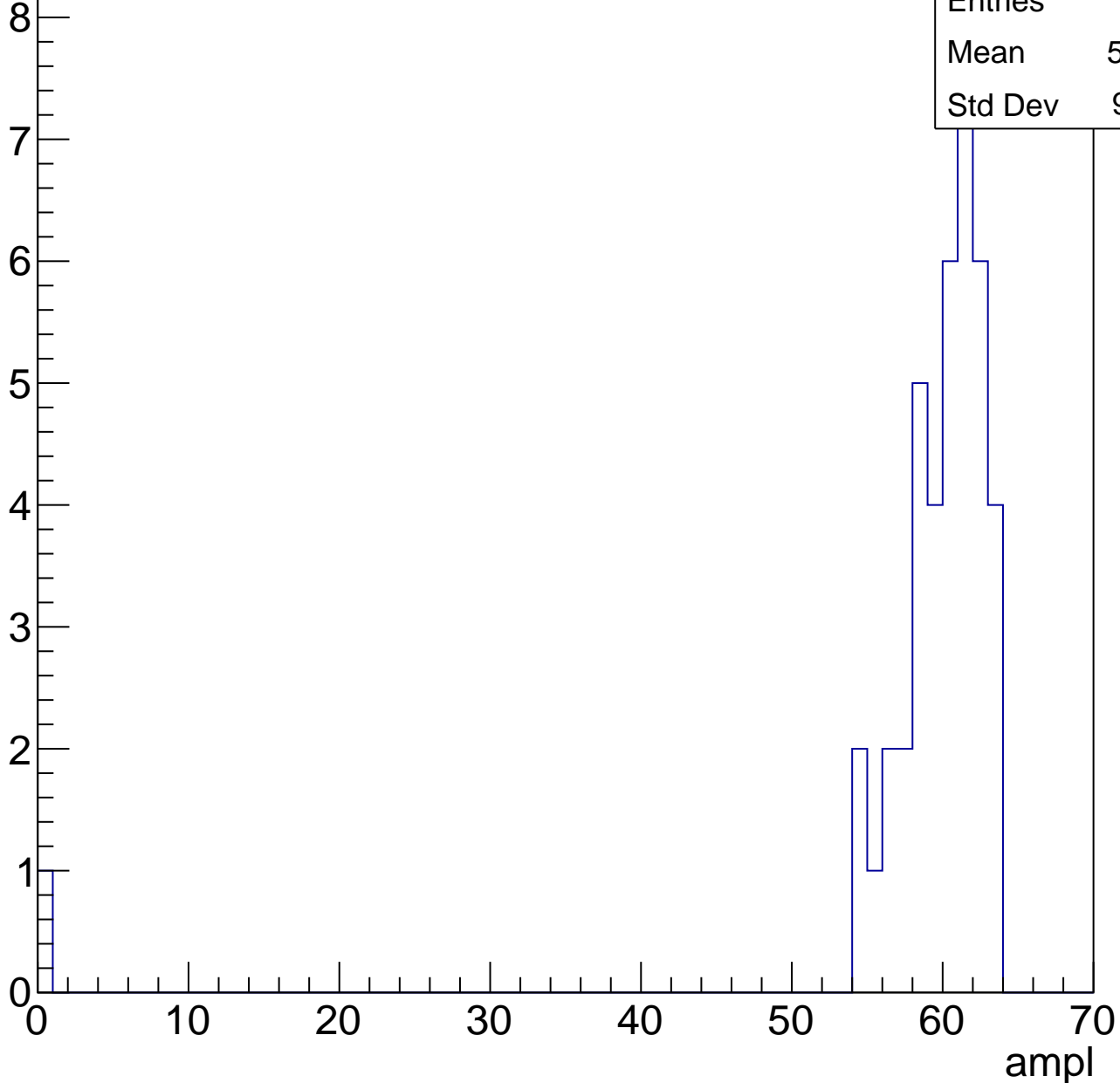


B1L103S, U12-ch113, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	41
Mean	58.22
Std Dev	9.511

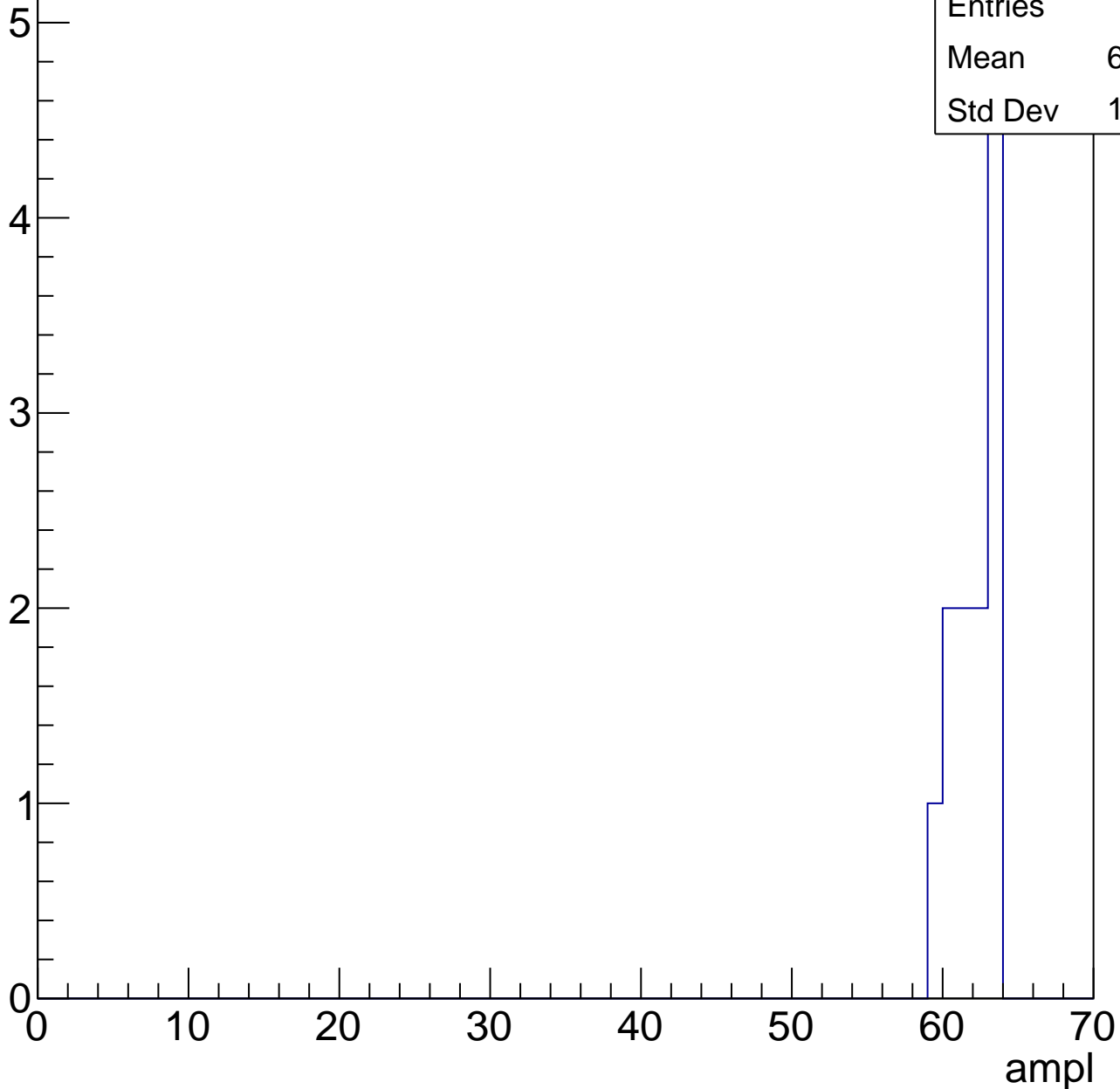


B1L103S, U12-ch113, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	12
Mean	61.67
Std Dev	1.374



B1L103S, U12-ch113, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

ampl

B1L103S, U12-ch114, adc0

calib_packv5_041523_1651.root, FC#0, port C2

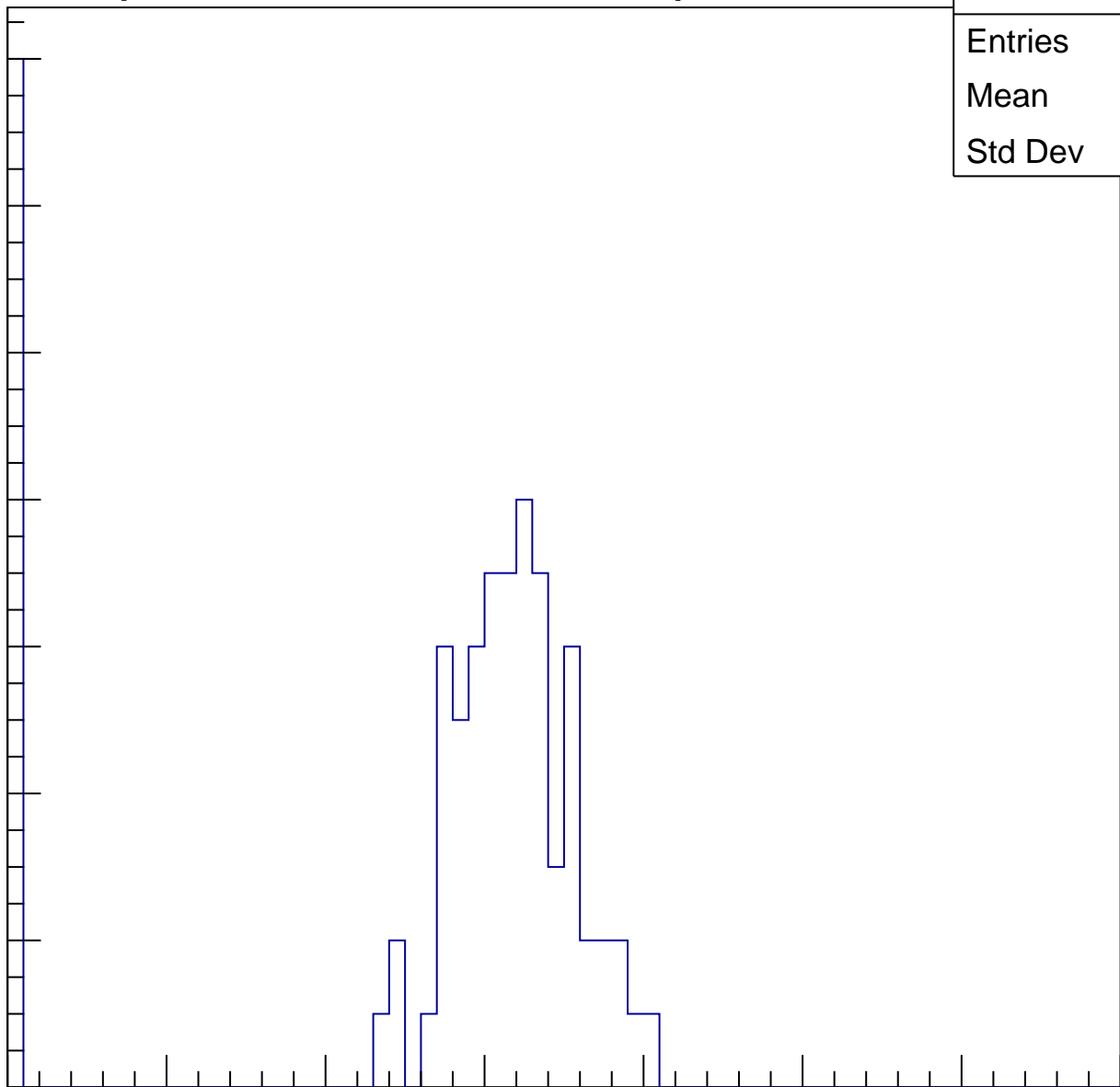
Entries	81
Mean	25.93
Std Dev	12.3

Entry

14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

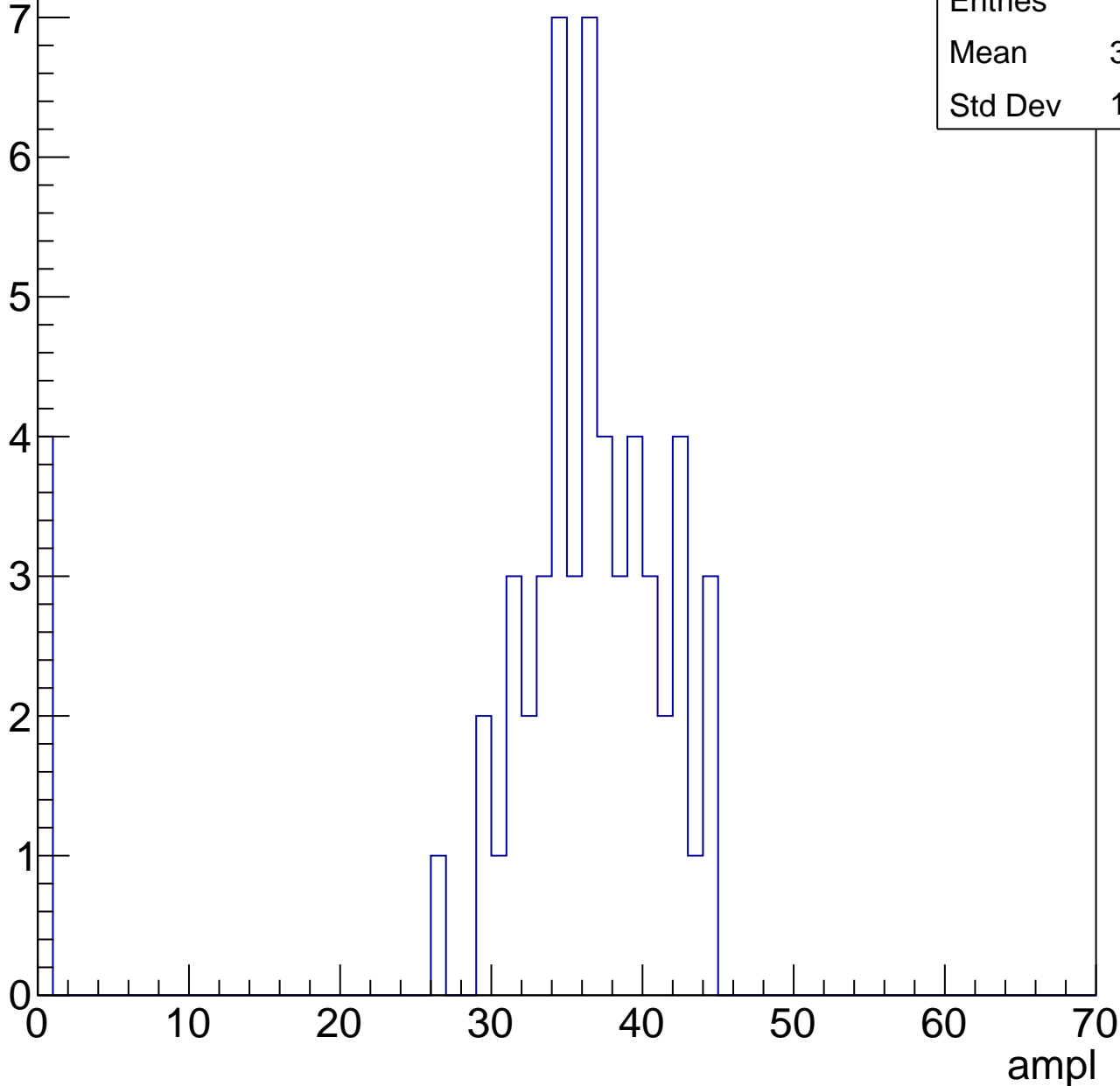


B1L103S, U12-ch114, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	57
Mean	33.82
Std Dev	10.13

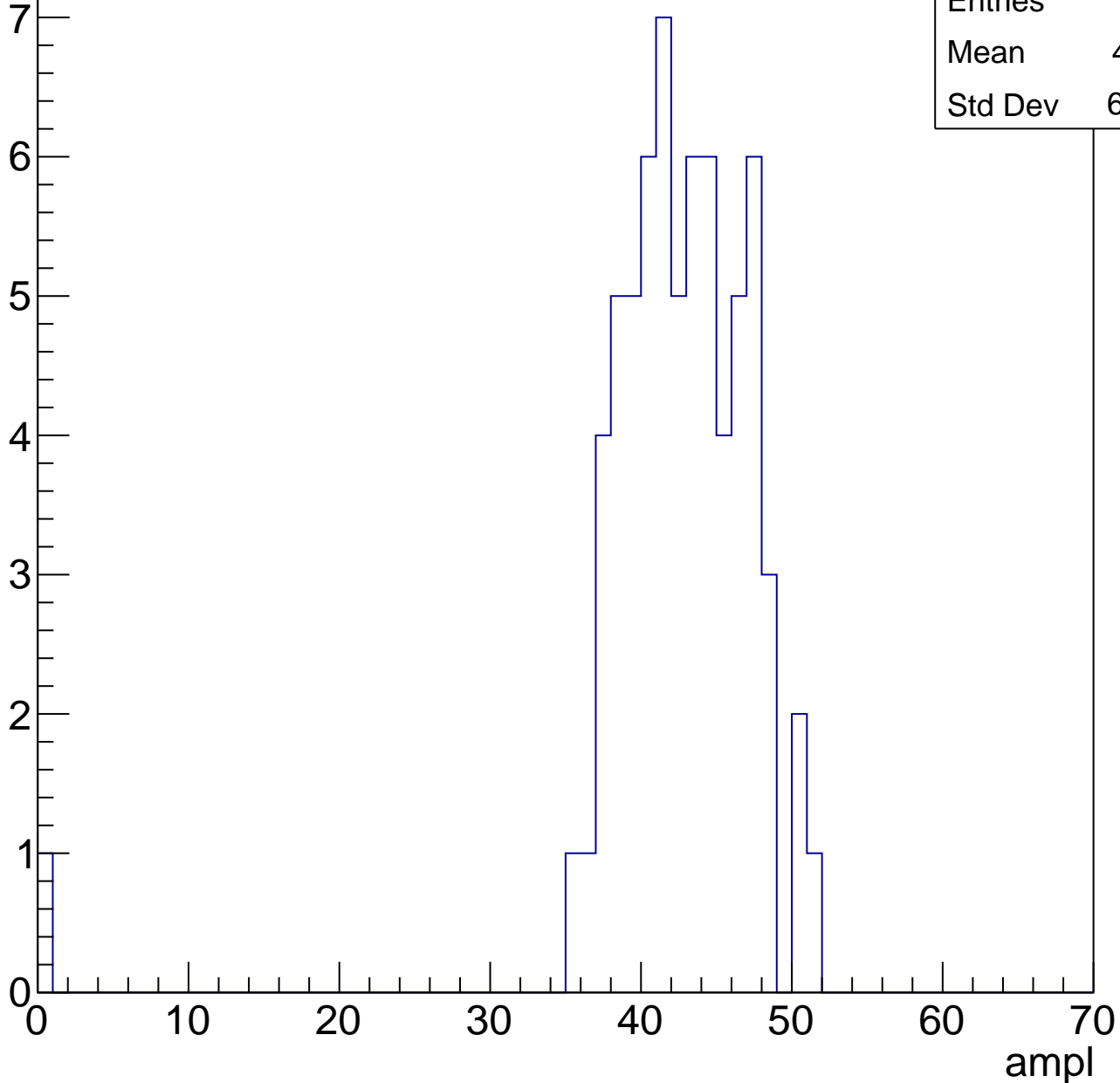


B1L103S, U12-ch114, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

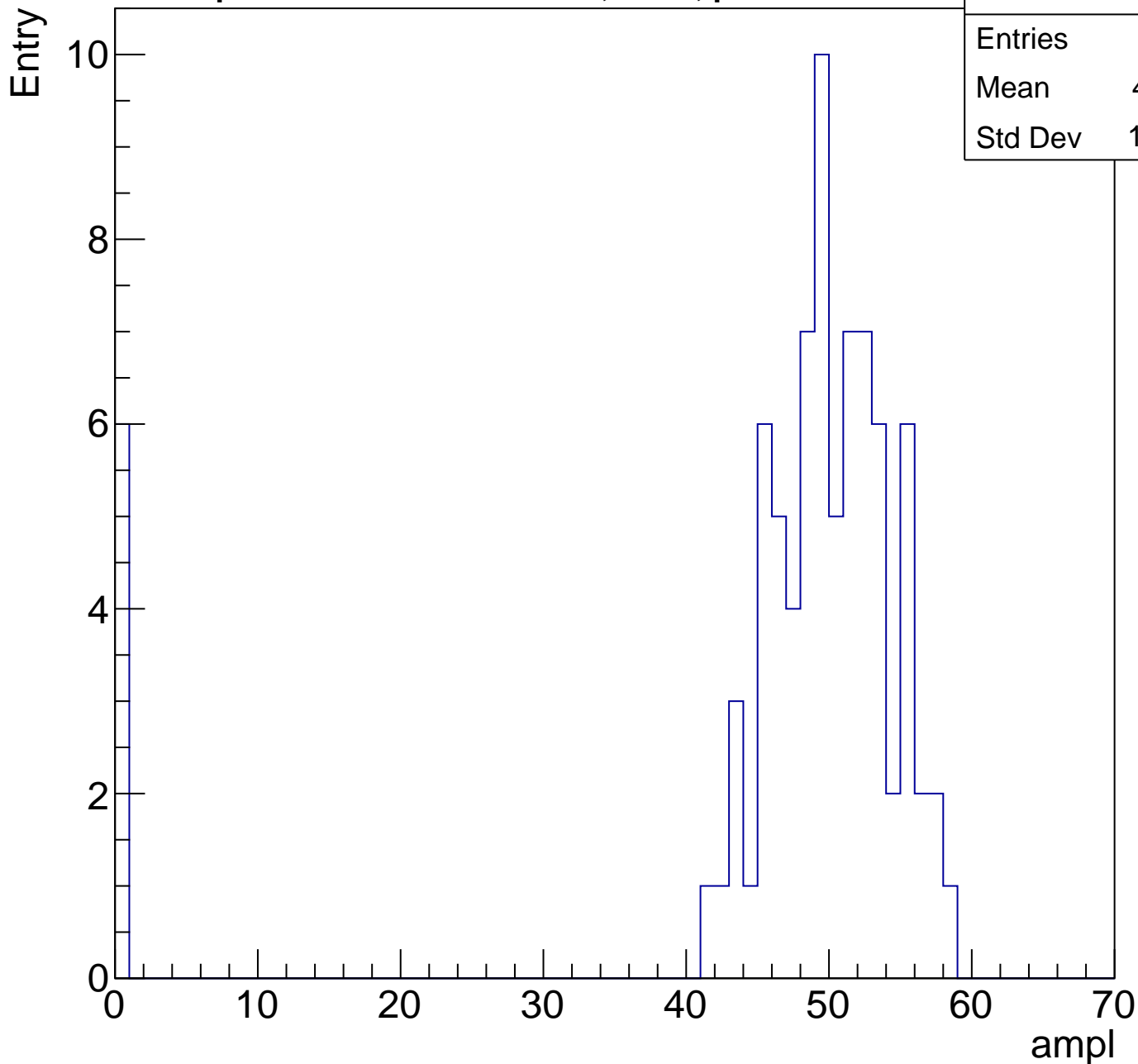
Entries	68
Mean	41.91
Std Dev	6.322



B1L103S, U12-ch114, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	82
Mean	46.11
Std Dev	13.48

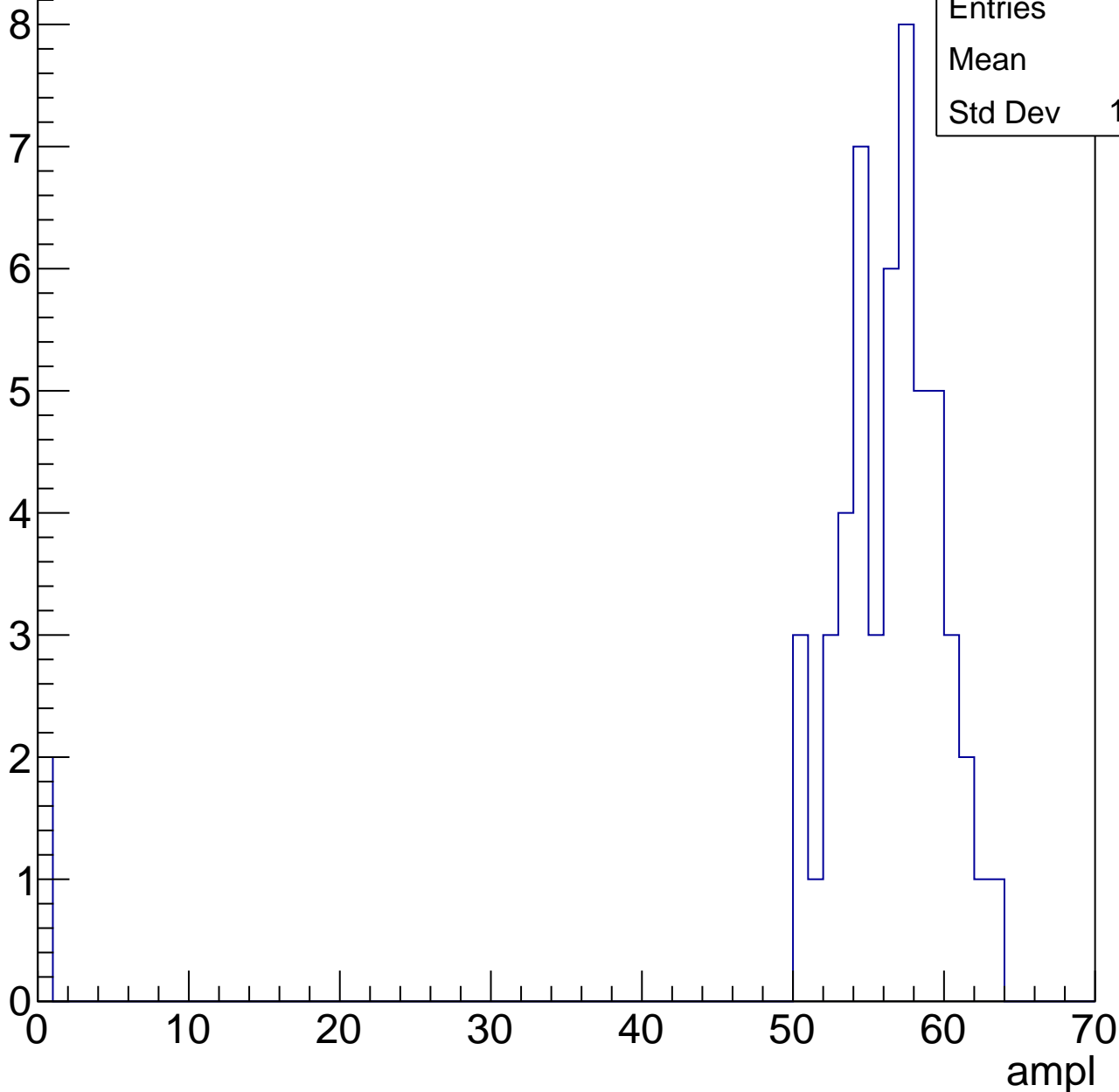


B1L103S, U12-ch114, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	54
Mean	54
Std Dev	11.02

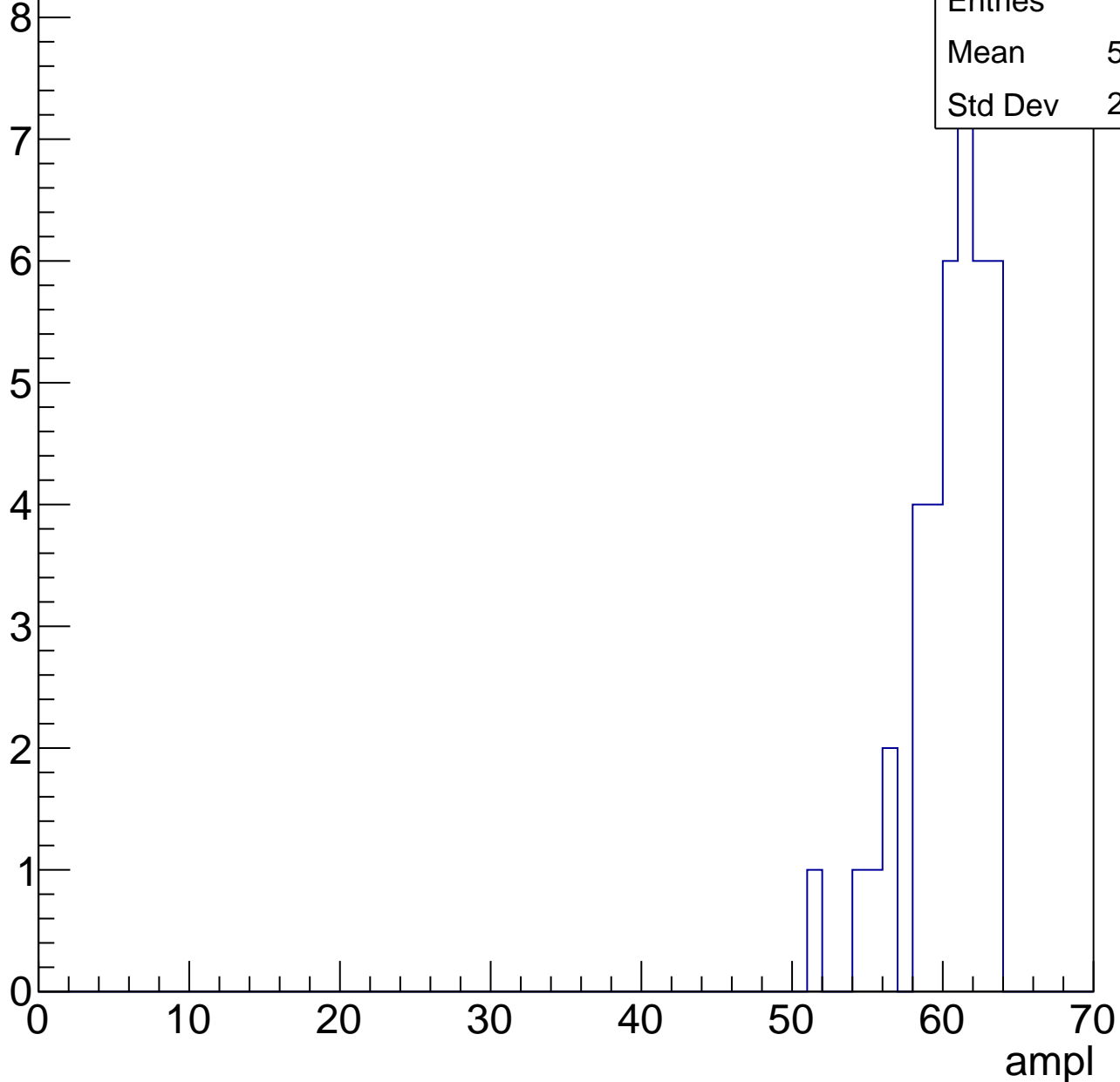


B1L103S, U12-ch114, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

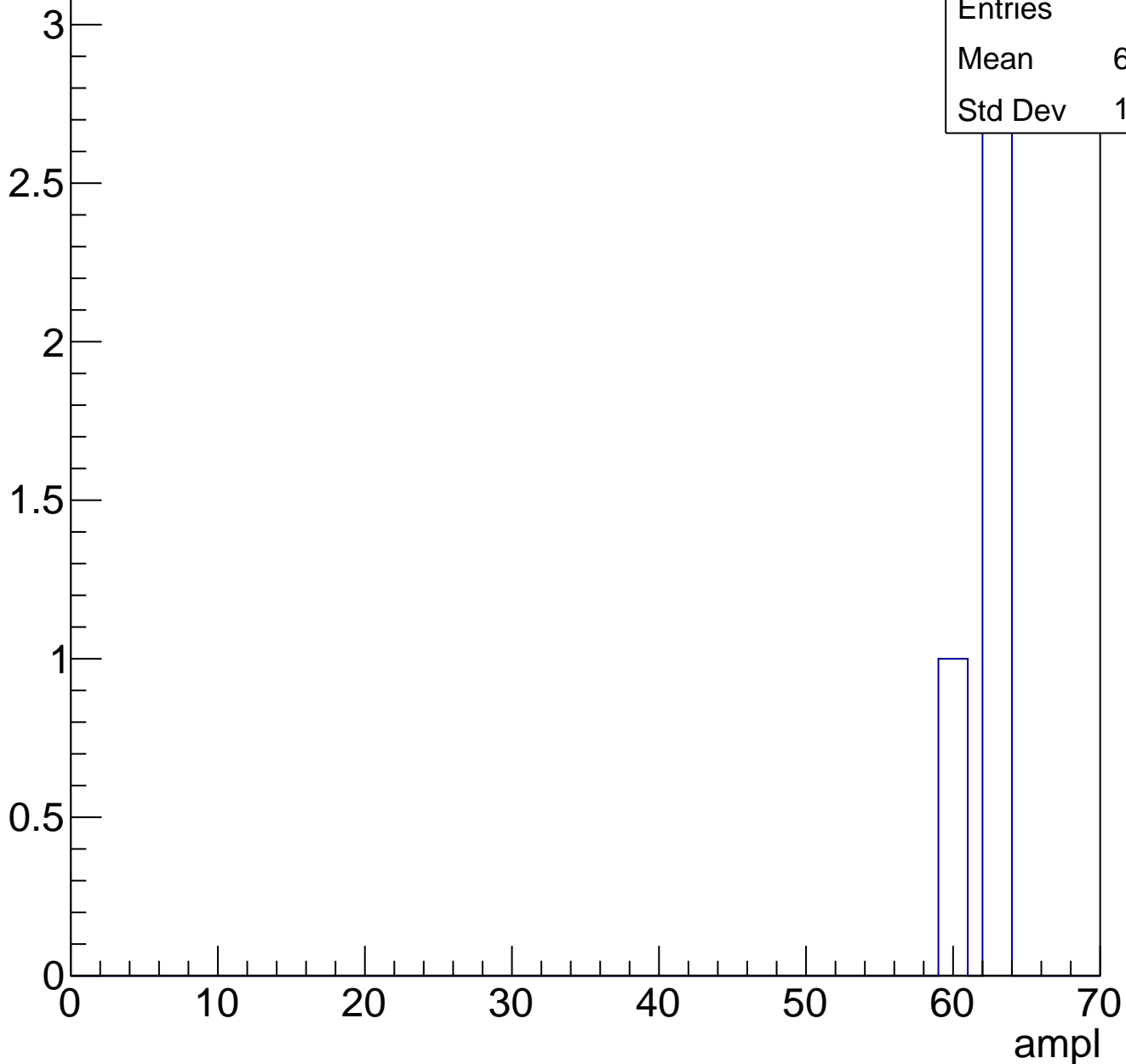
Entries	39
Mean	59.95
Std Dev	2.679



B1L103S, U12-ch114, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch114, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

20
18
16
14
12
10
8
6
4
2
0

Entries	20
Mean	0
Std Dev	0

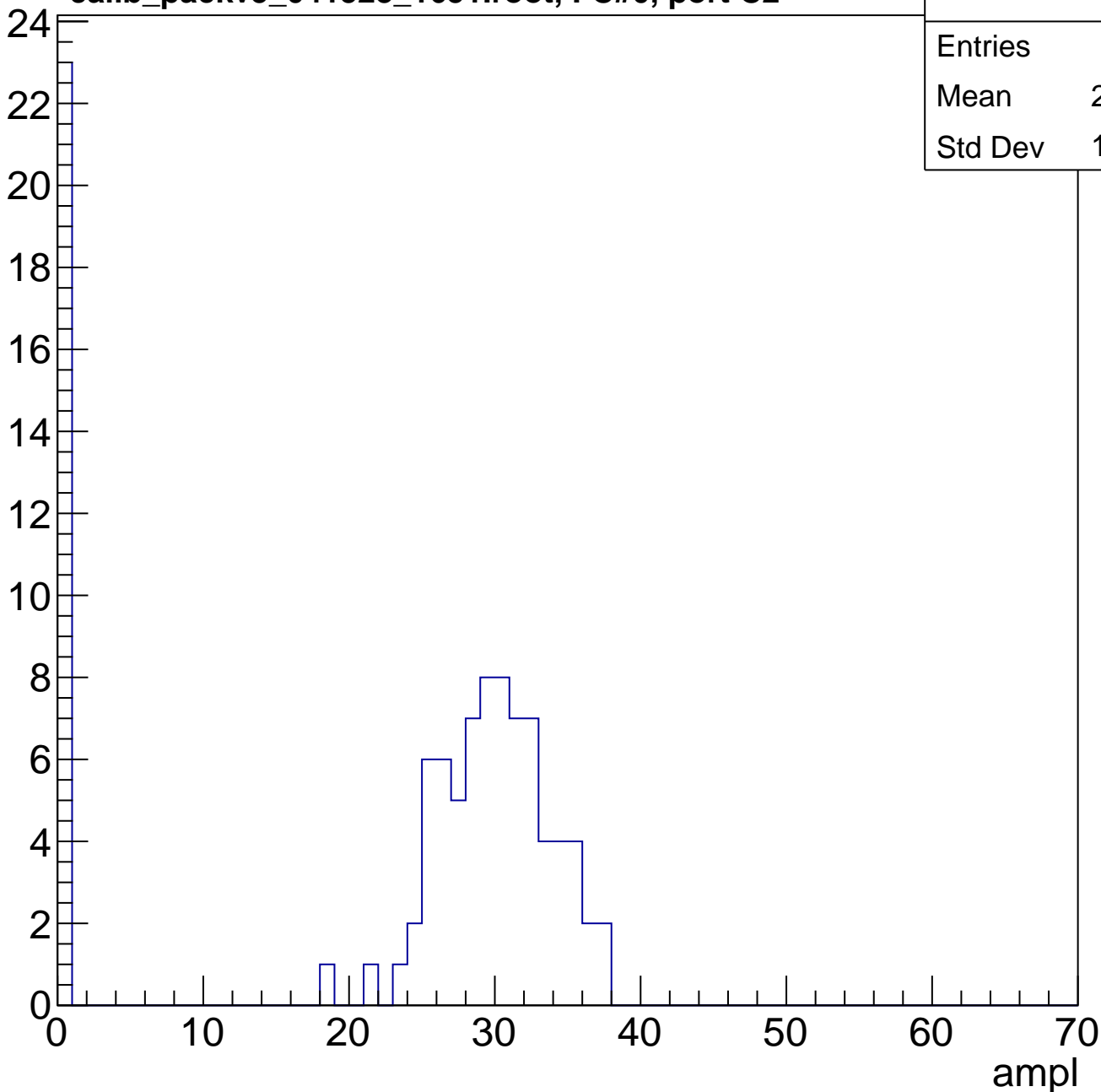
ampl

B1L103S, U12-ch115, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	98
Mean	22.59
Std Dev	12.94

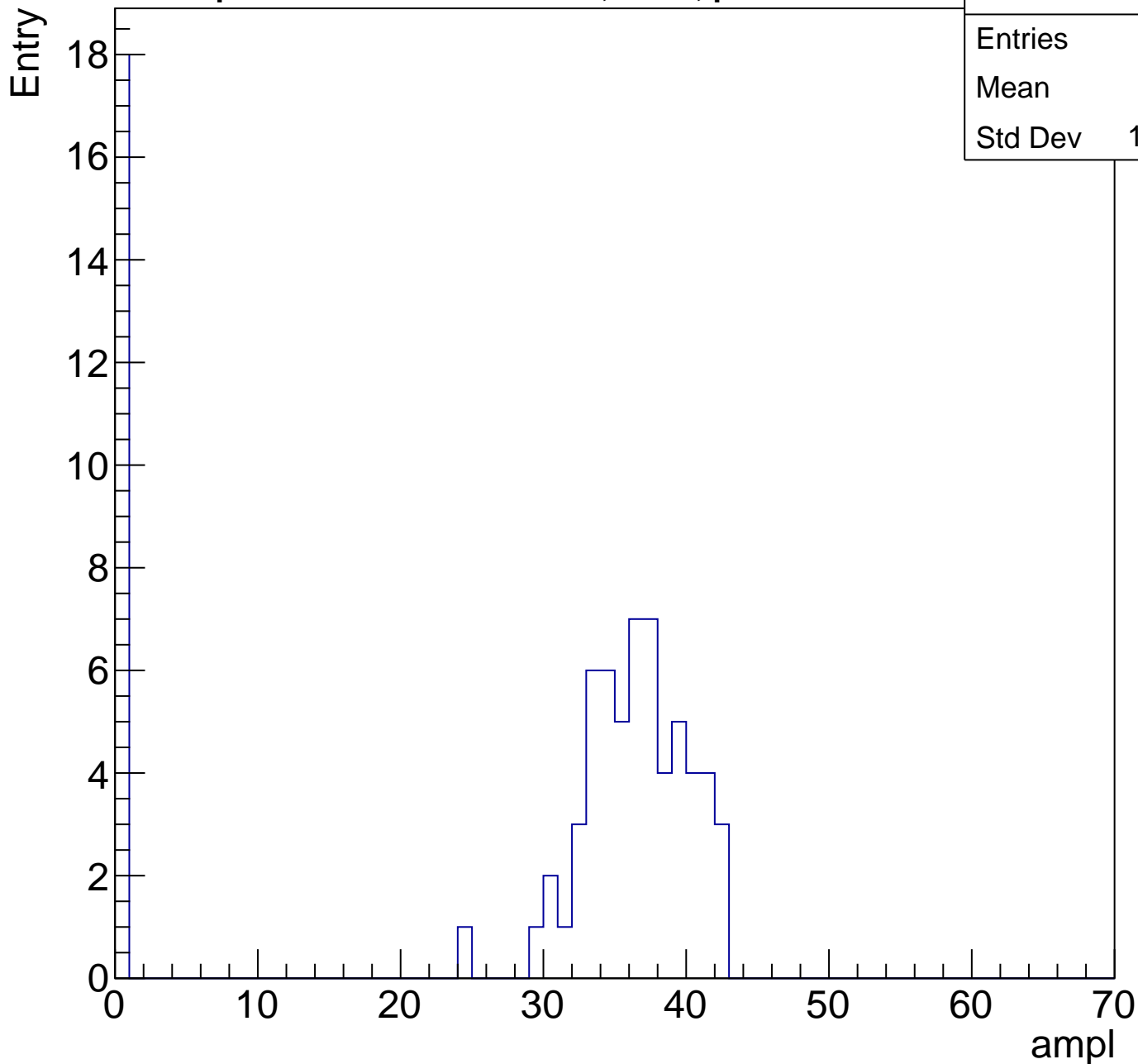
Entry



B1L103S, U12-ch115, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	77
Mean	27.6
Std Dev	15.56

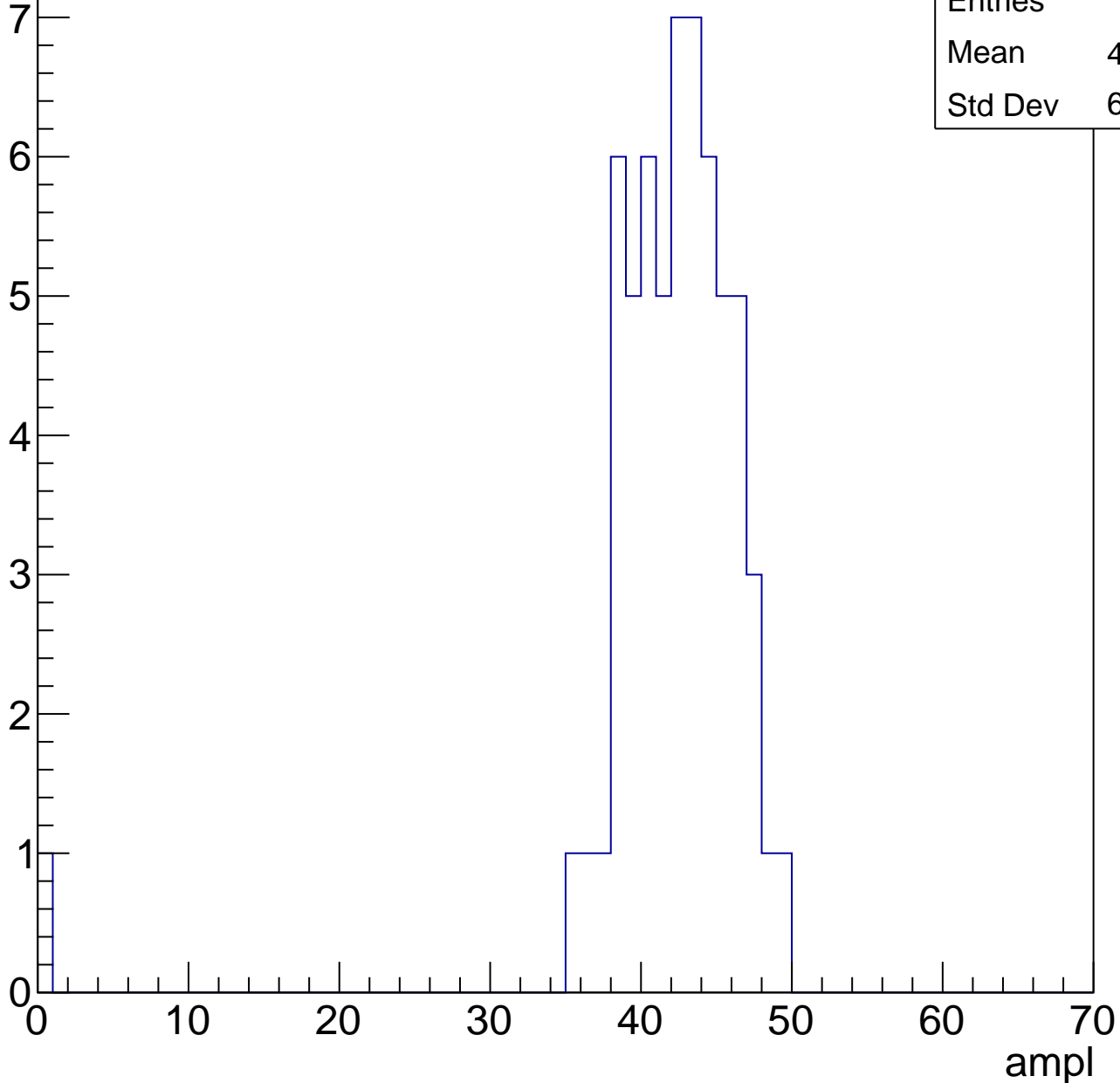


B1L103S, U12-ch115, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	41.44
Std Dev	6.195

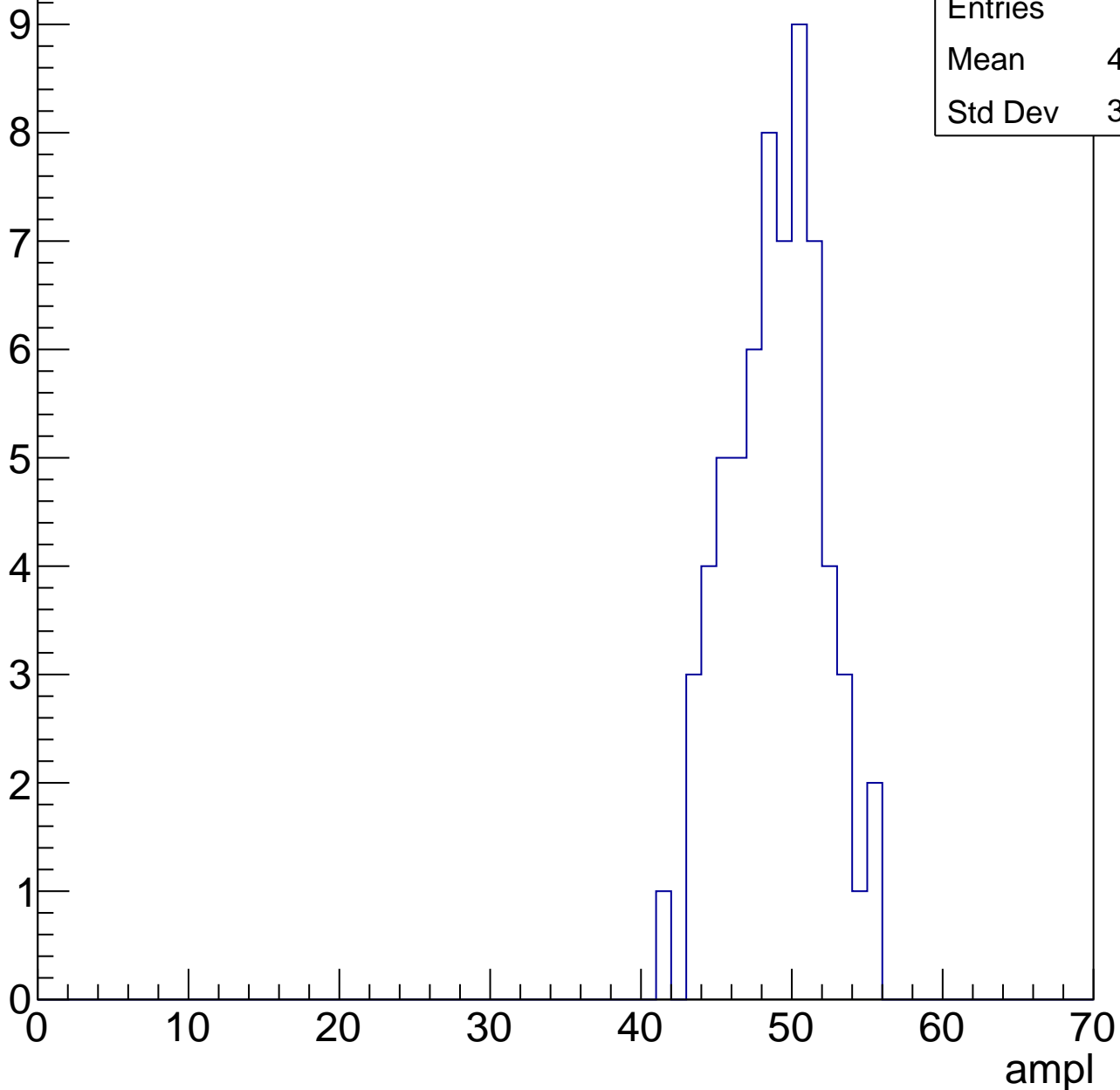


B1L103S, U12-ch115, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	48.43
Std Dev	3.103

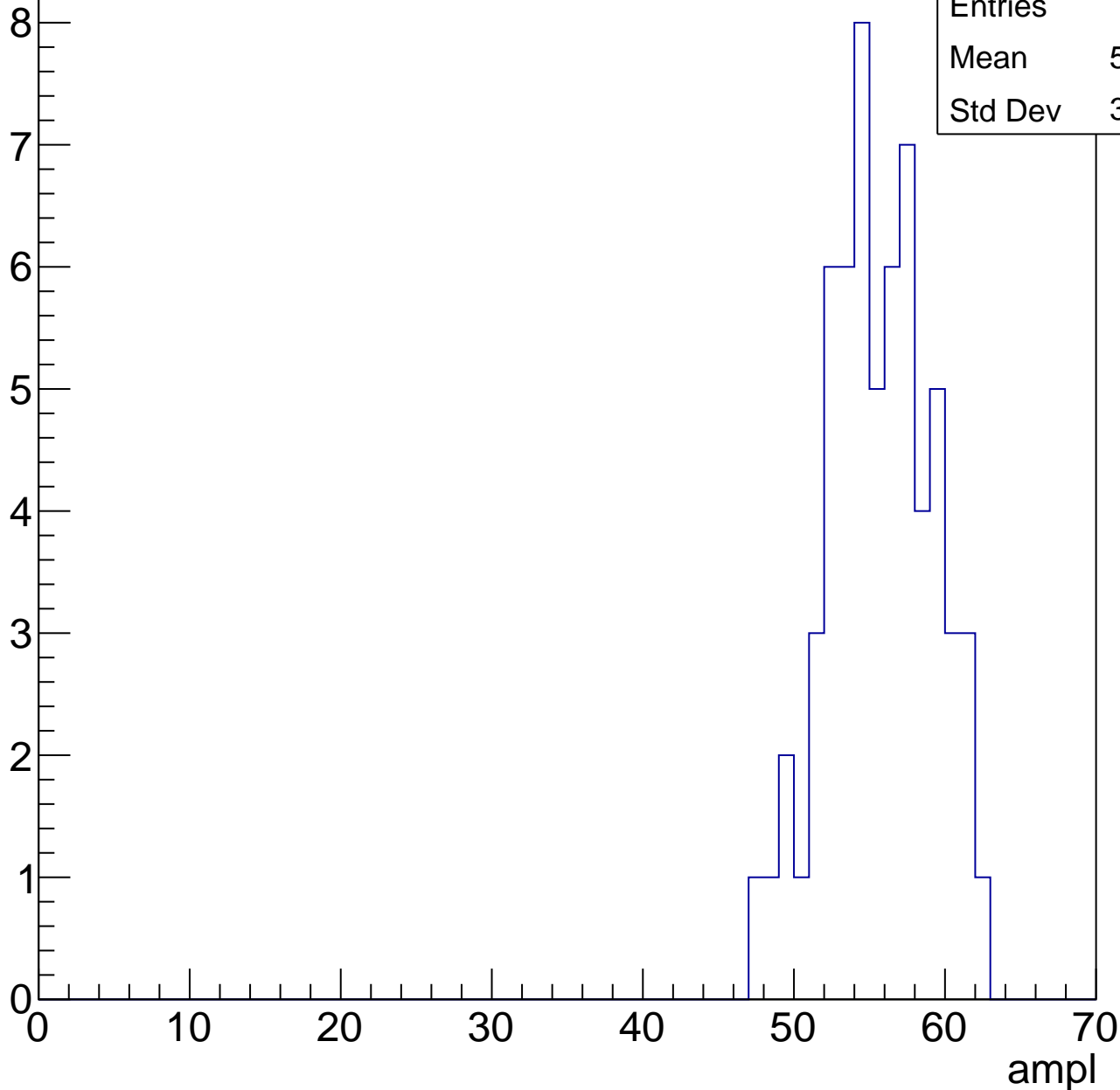


B1L103S, U12-ch115, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	55.16
Std Dev	3.418

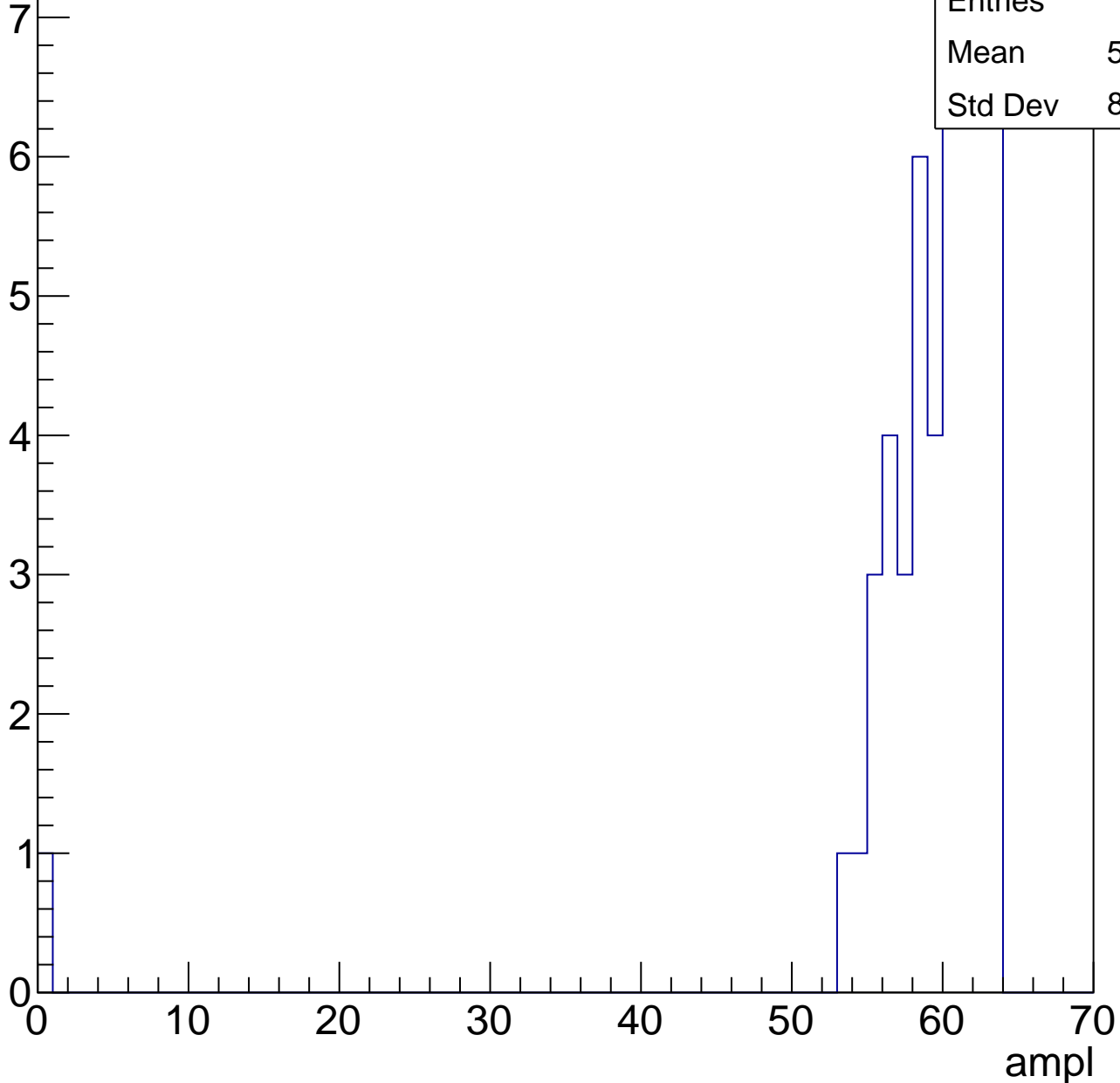


B1L103S, U12-ch115, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	51
Mean	58.29
Std Dev	8.664



B1L103S, U12-ch115, adc6

calib_packv5_041523_1651.root, FC#0, port C2

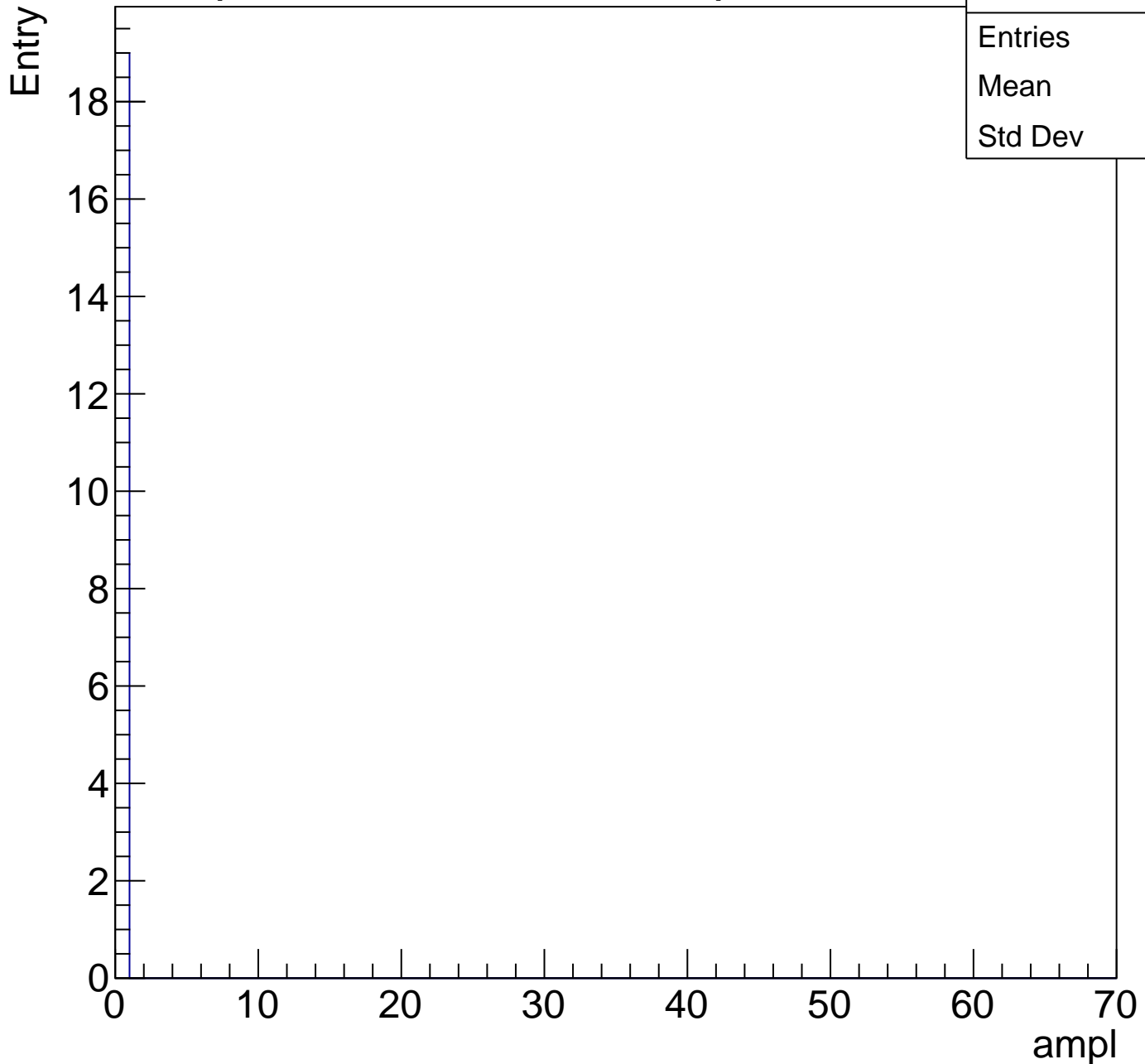
Entry



B1L103S, U12-ch115, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	0
Std Dev	0



B1L103S, U12-ch116, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	87
Mean	27
Std Dev	10.25

Entry

10
8
6
4
2
0

0

10

20

30

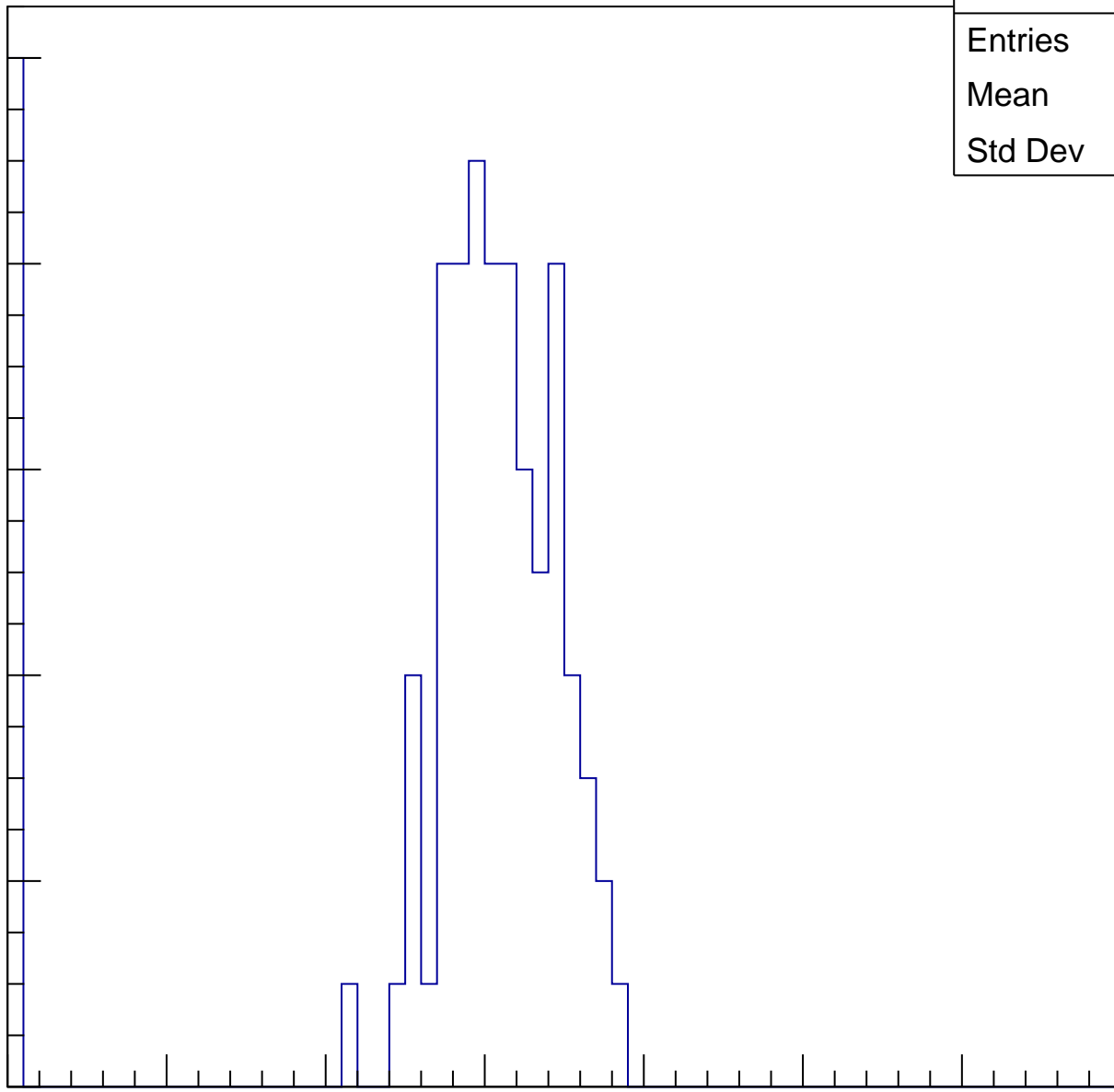
40

50

60

70

ampl

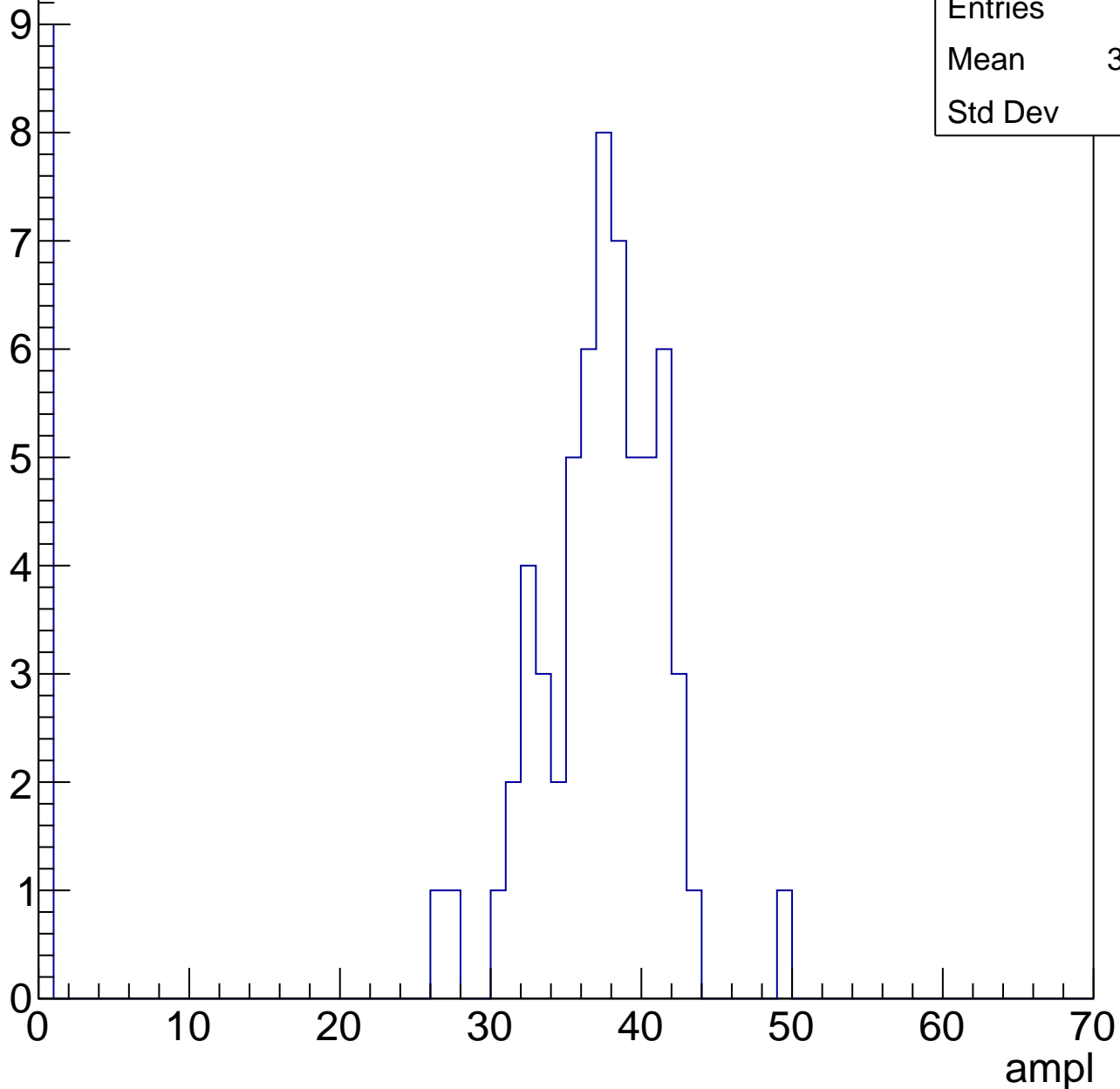


B1L103S, U12-ch116, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	32.17
Std Dev	12.9

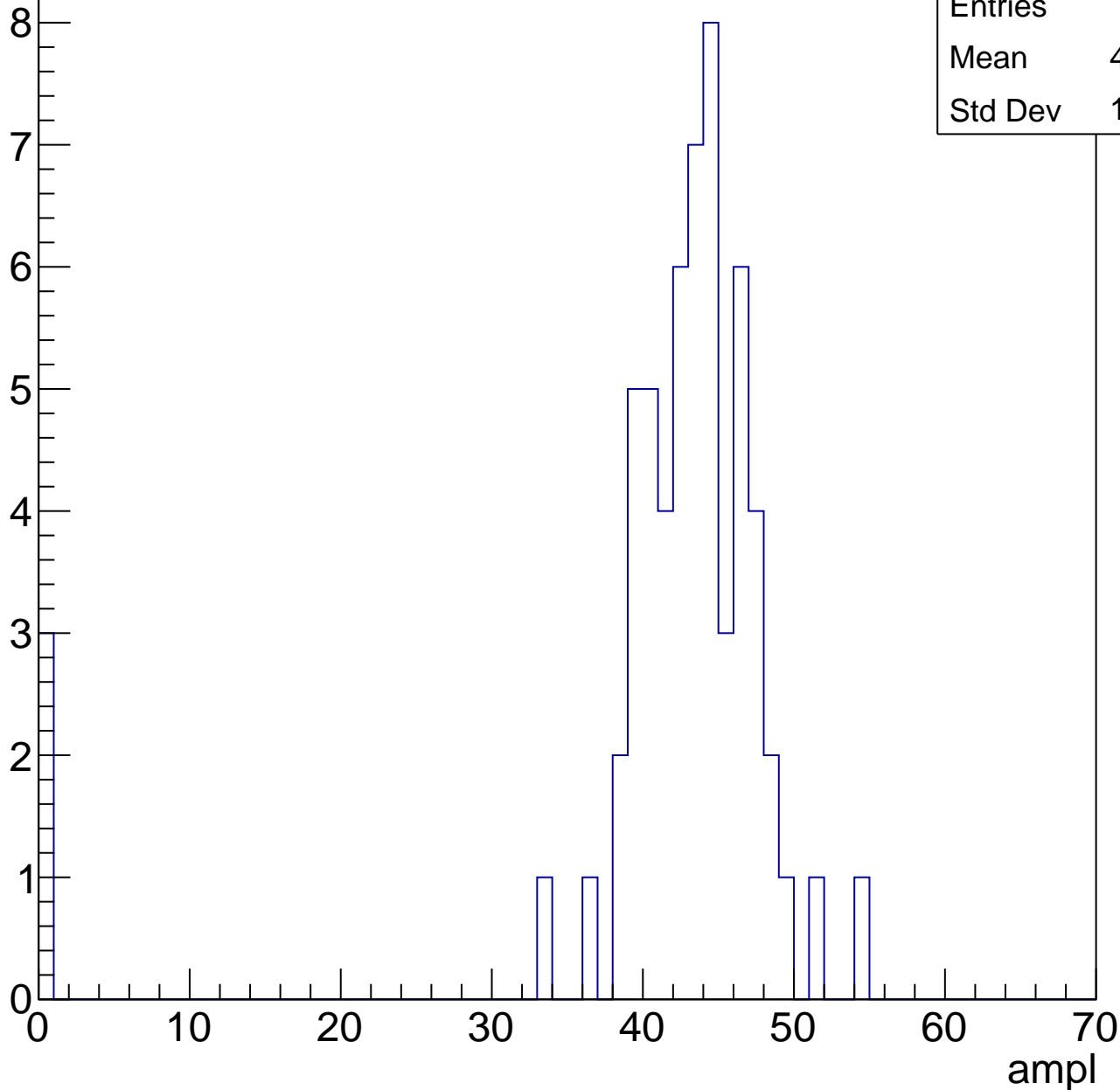


B1L103S, U12-ch116, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	40.97
Std Dev	10.04

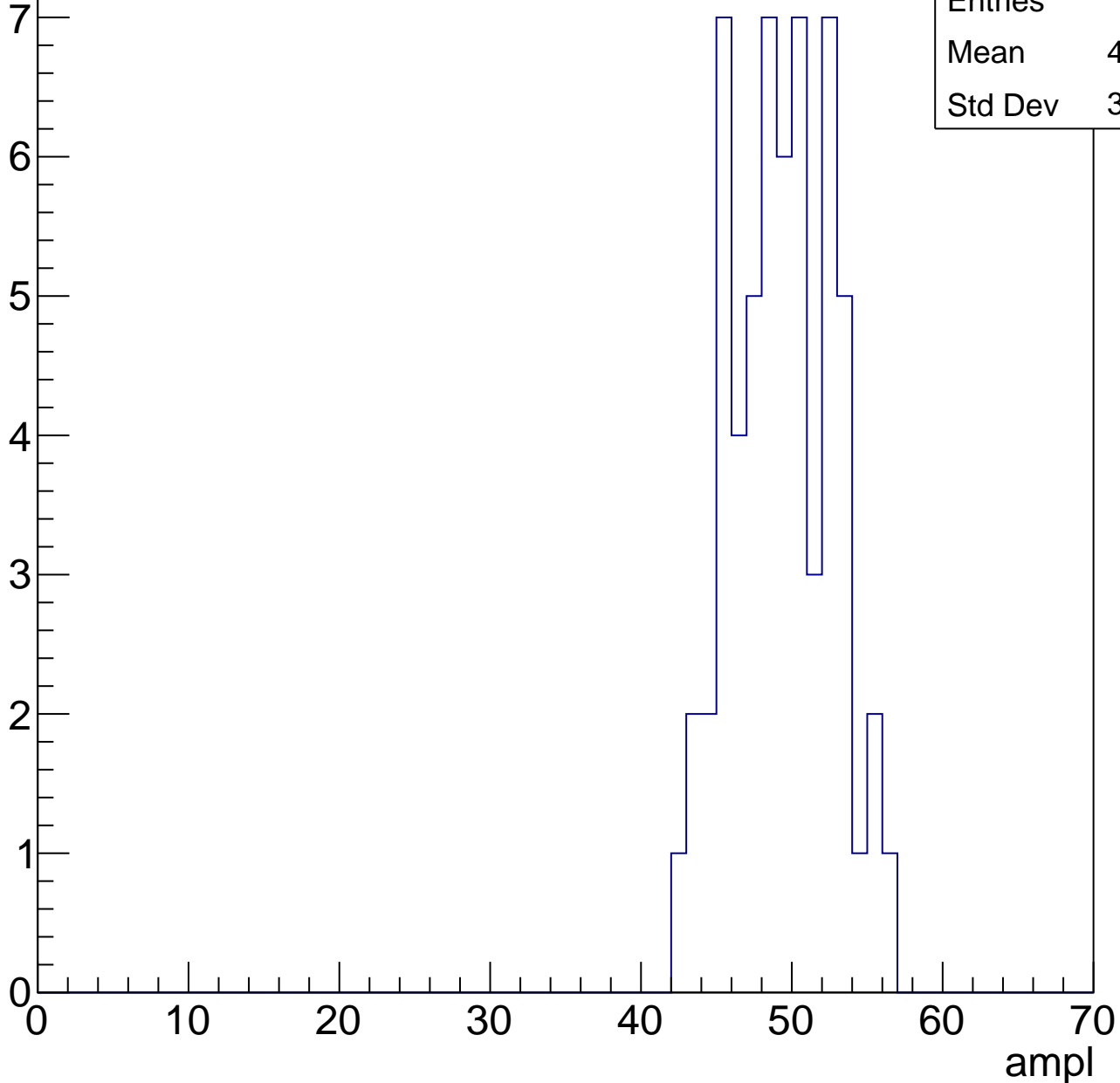


B1L103S, U12-ch116, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	48.87
Std Dev	3.299

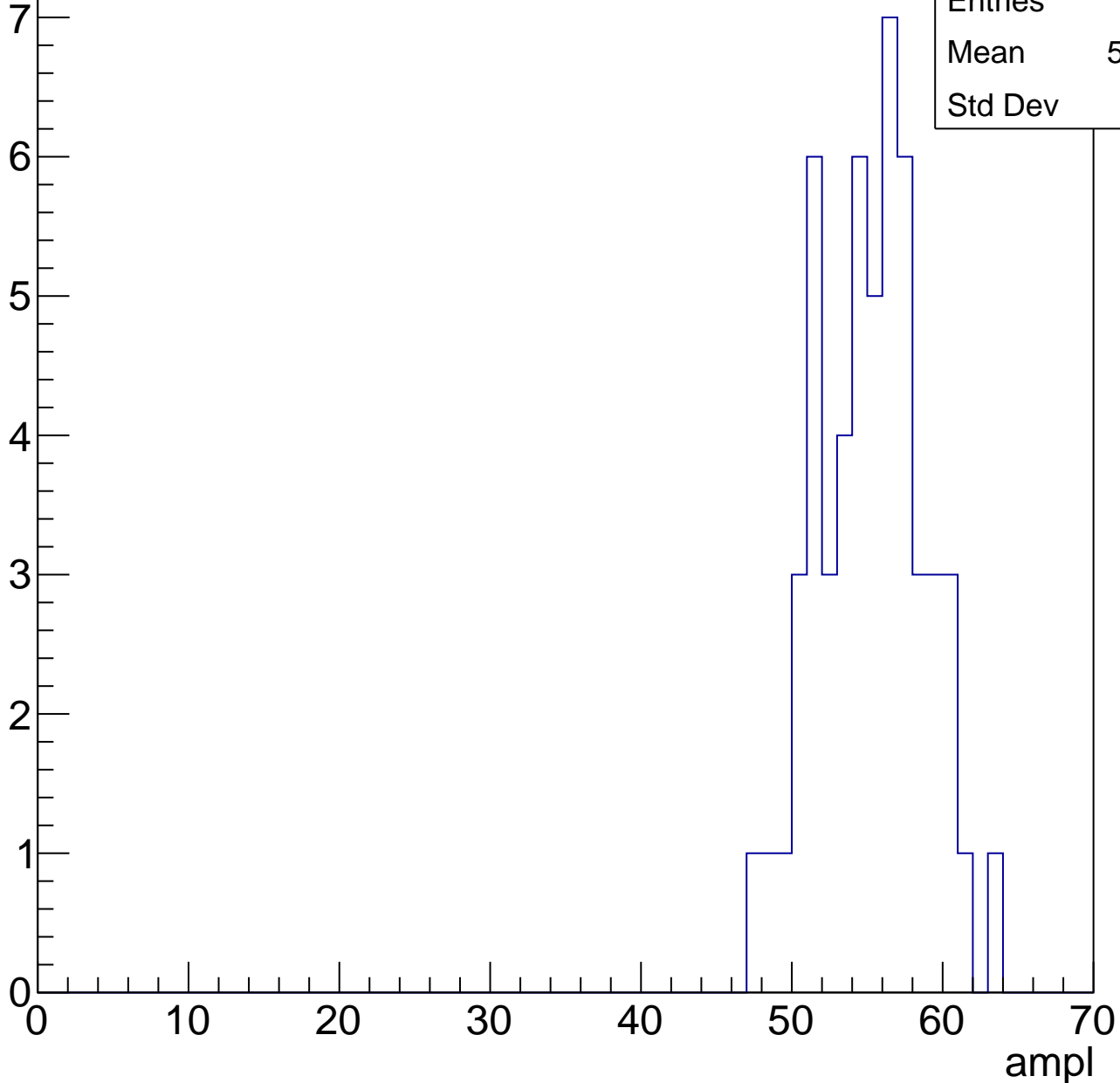


B1L103S, U12-ch116, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	54
Mean	54.74
Std Dev	3.46

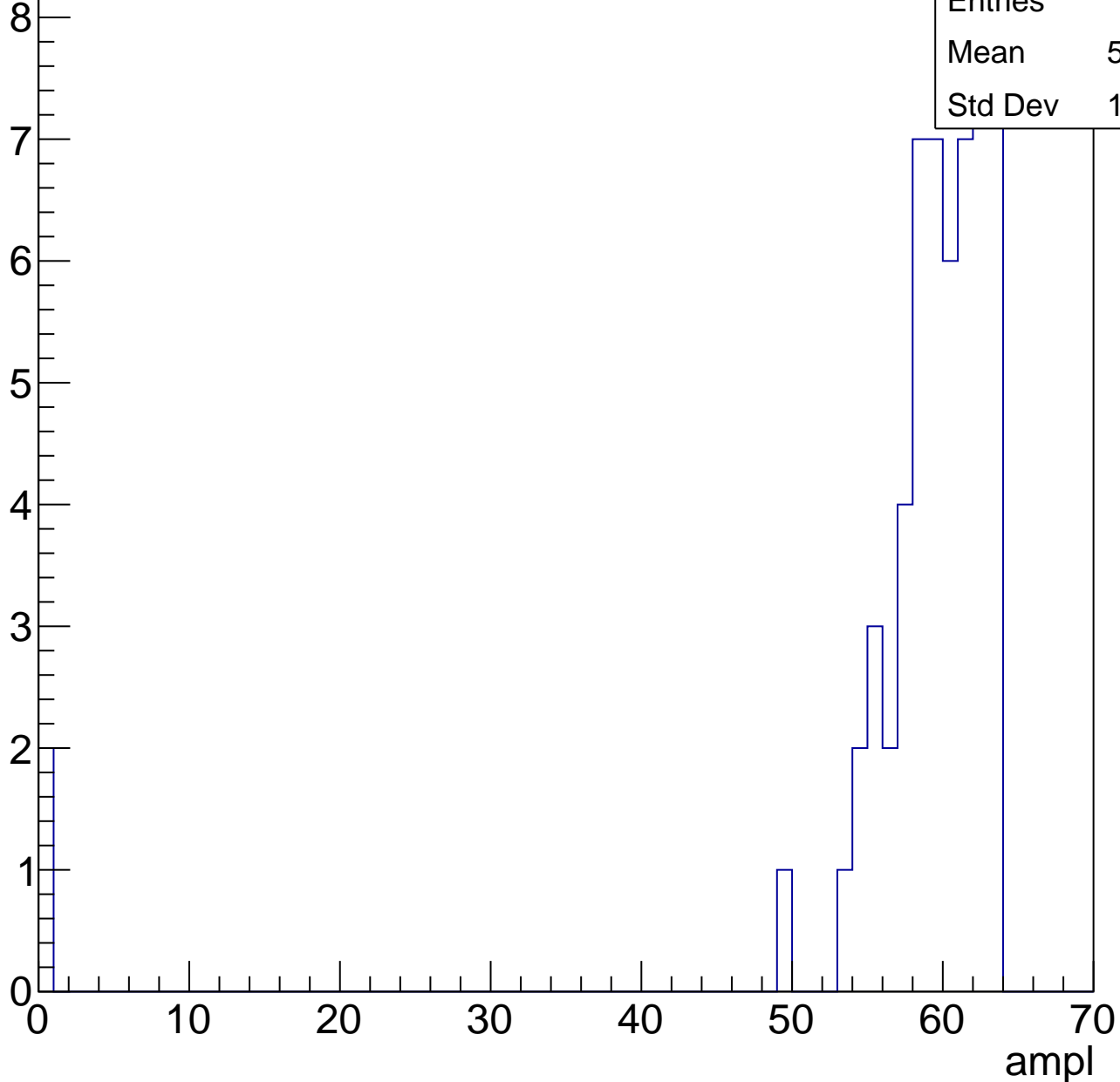


B1L103S, U12-ch116, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	57.26
Std Dev	11.22



B1L103S, U12-ch116, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	5
Mean	61.8
Std Dev	0.7483

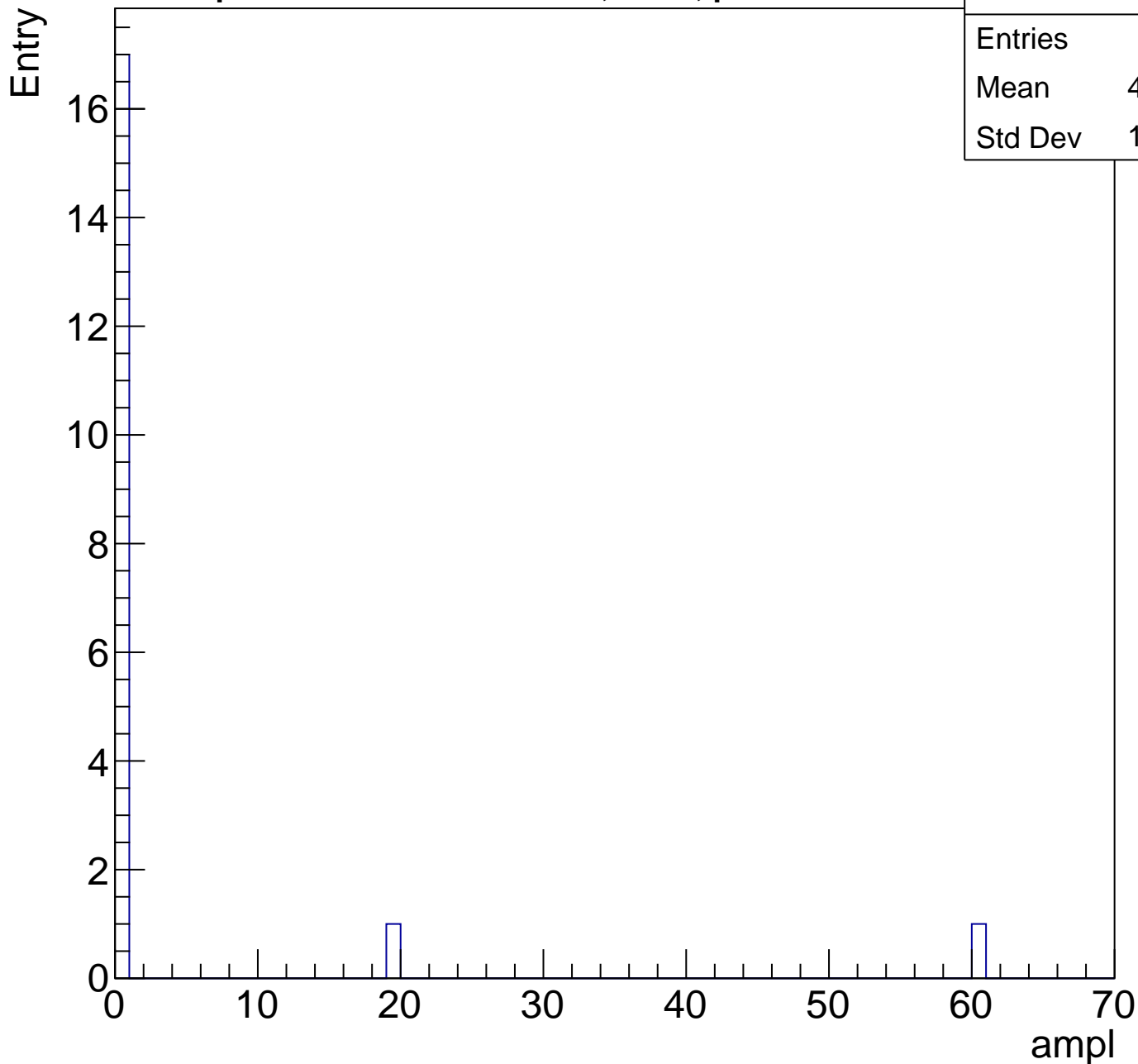
ampl

0 10 20 30 40 50 60 70

B1L103S, U12-ch116, adc7

calib_packv5_041523_1651.root, FC#0, port C2

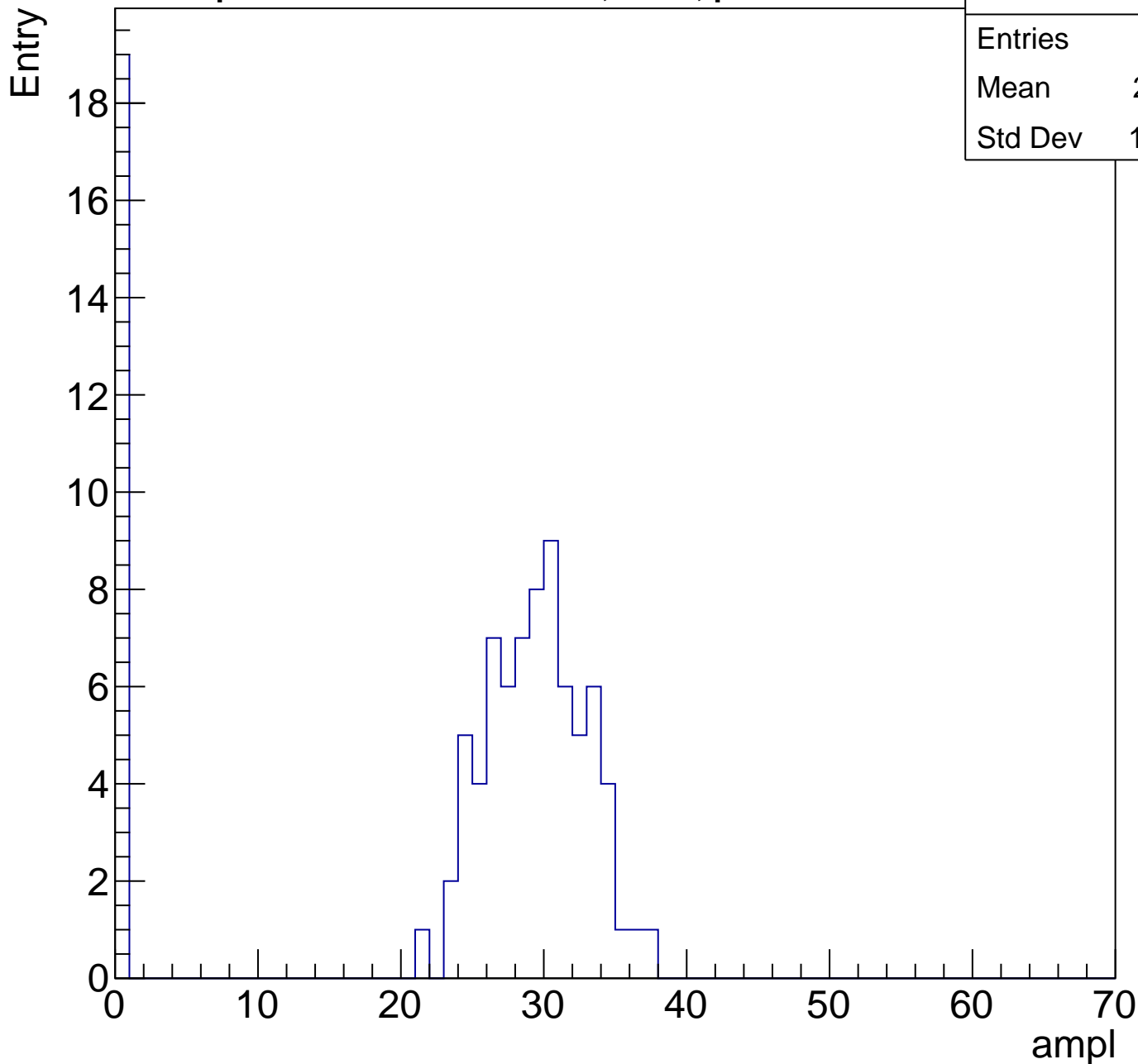
Entries	19
Mean	4.158
Std Dev	13.83



B1L103S, U12-ch117, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	92
Mean	23.01
Std Dev	12.12

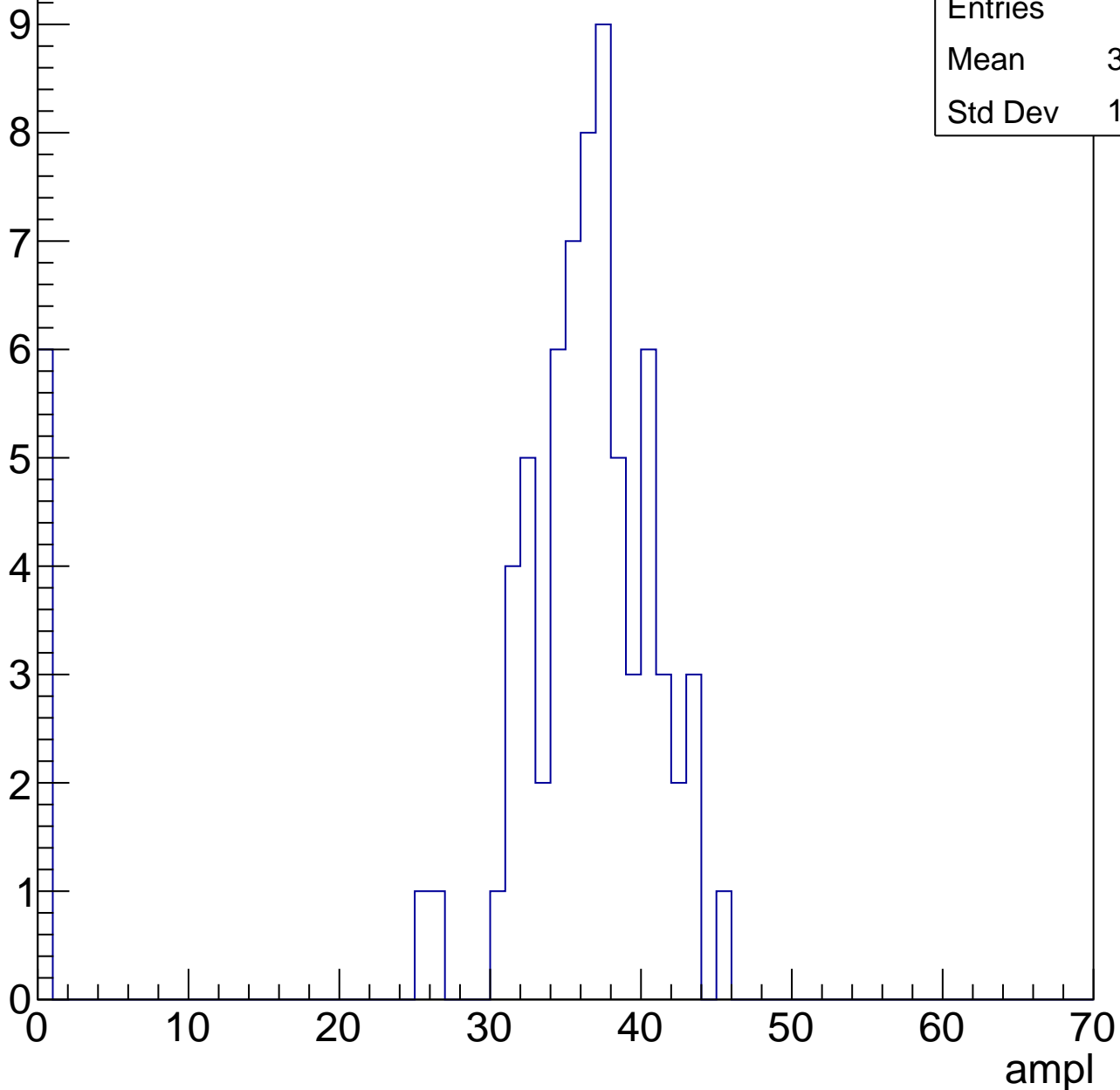


B1L103S, U12-ch117, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	73
Mean	33.27
Std Dev	10.63

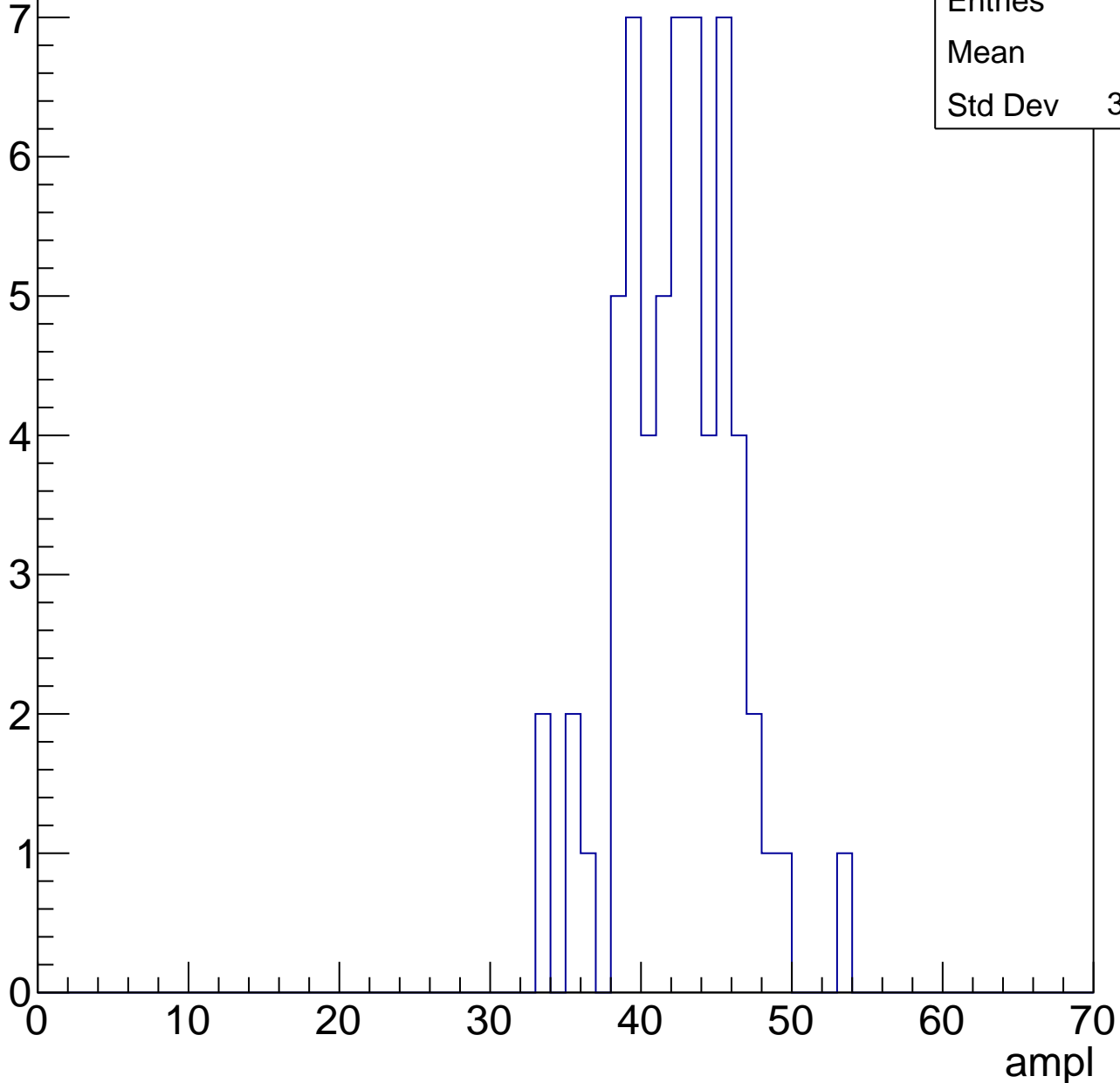


B1L103S, U12-ch117, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	41.9
Std Dev	3.798

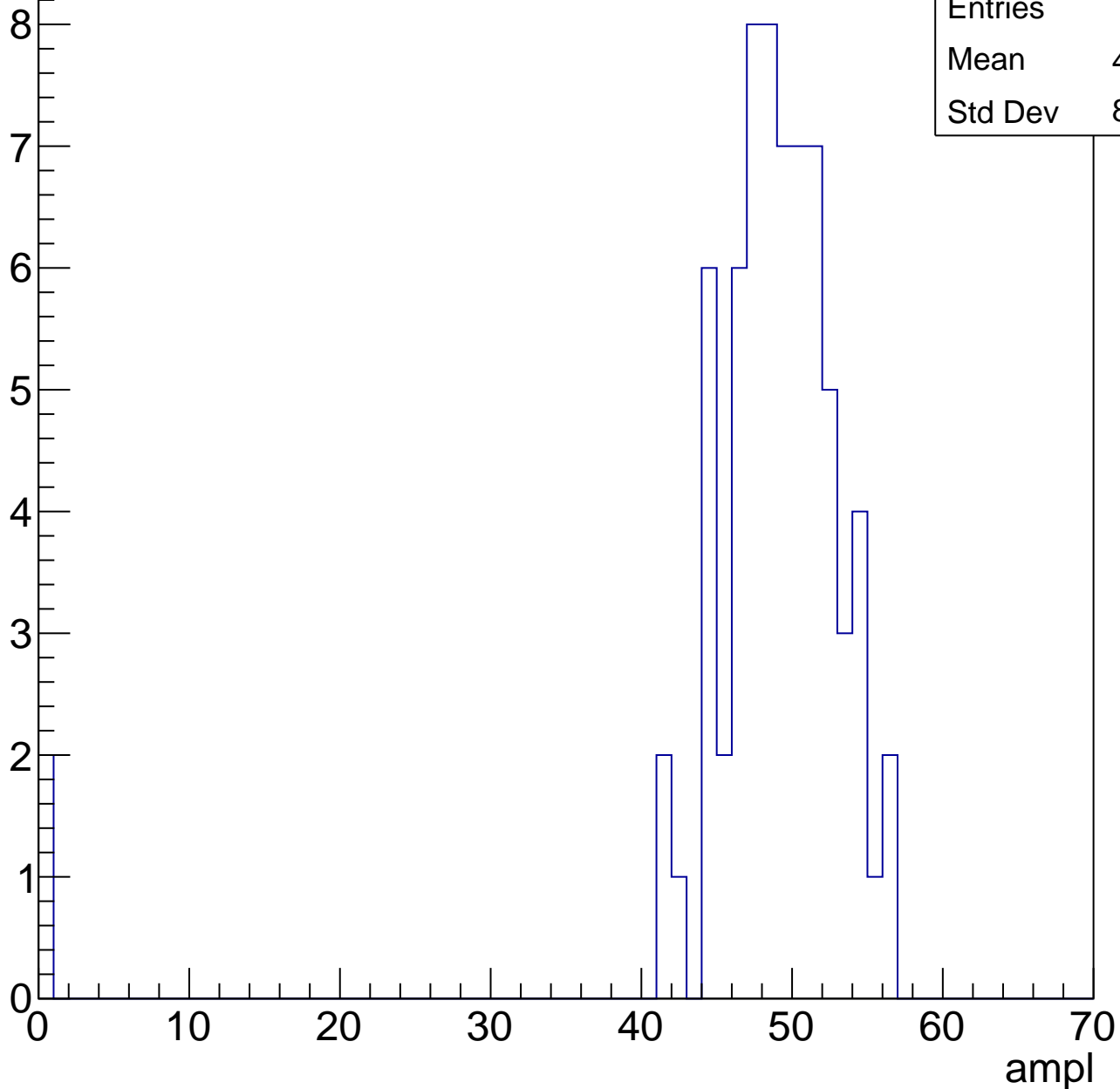


B1L103S, U12-ch117, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	47.41
Std Dev	8.751

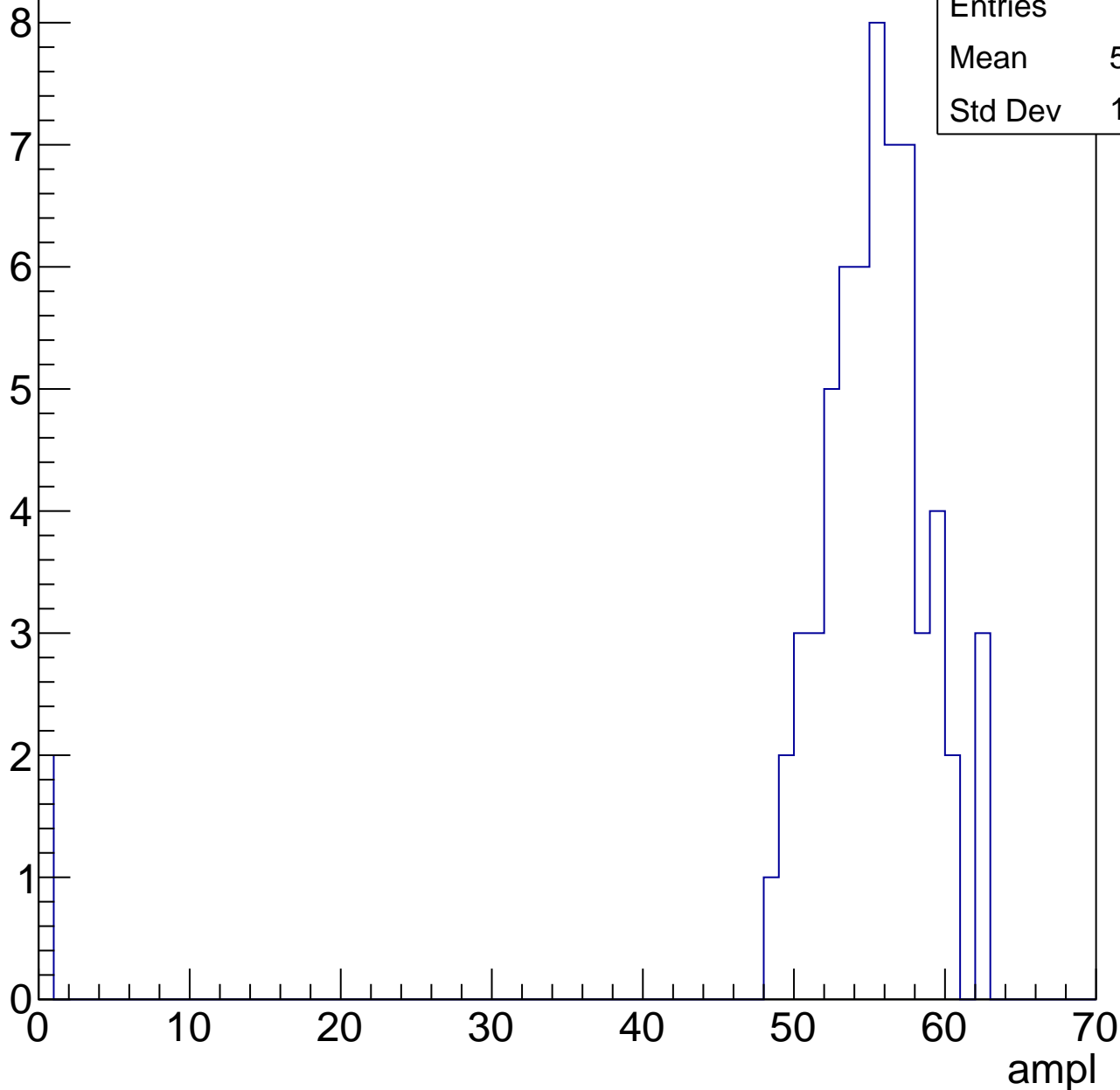


B1L103S, U12-ch117, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	53.19
Std Dev	10.23

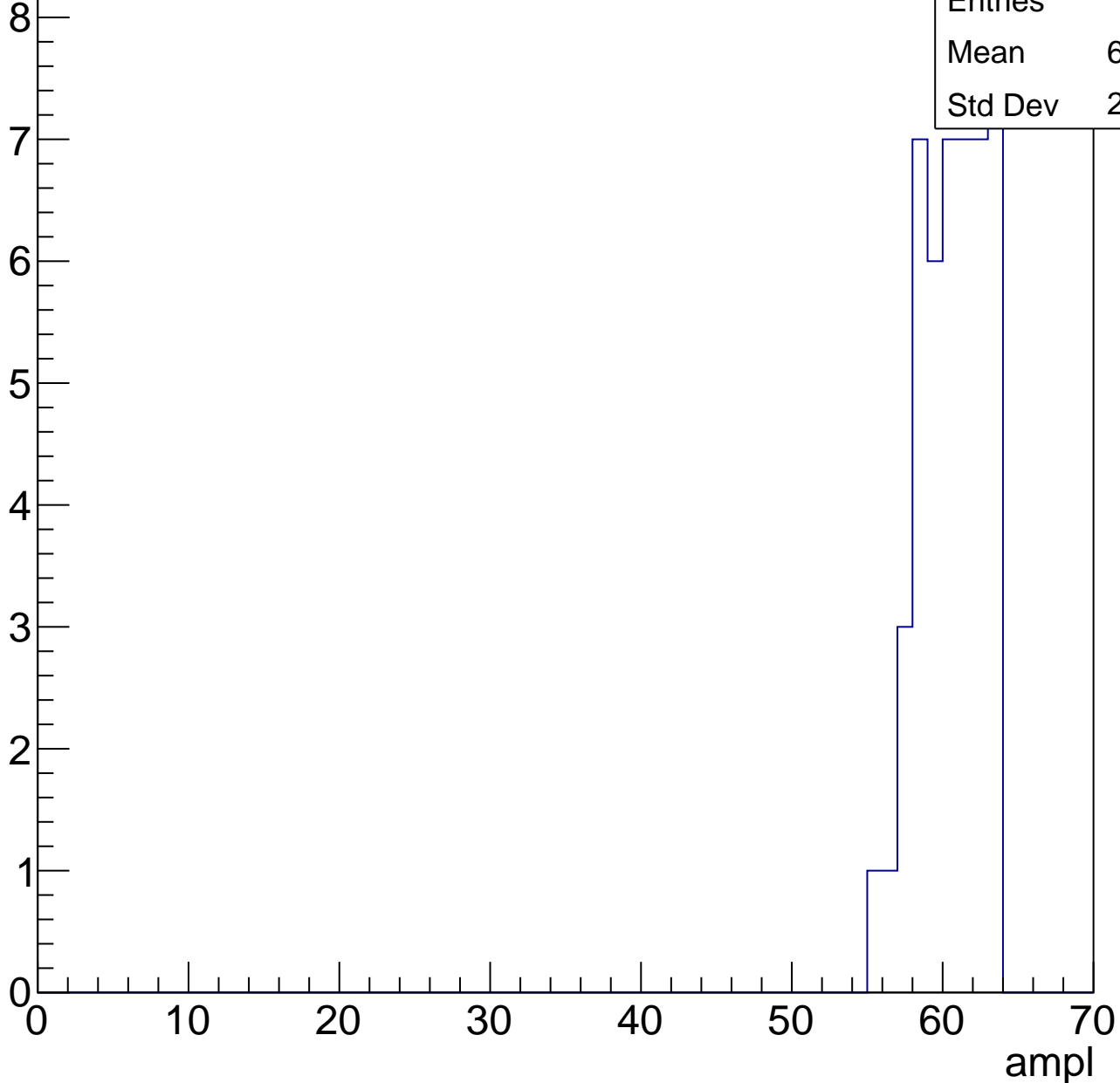


B1L103S, U12-ch117, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

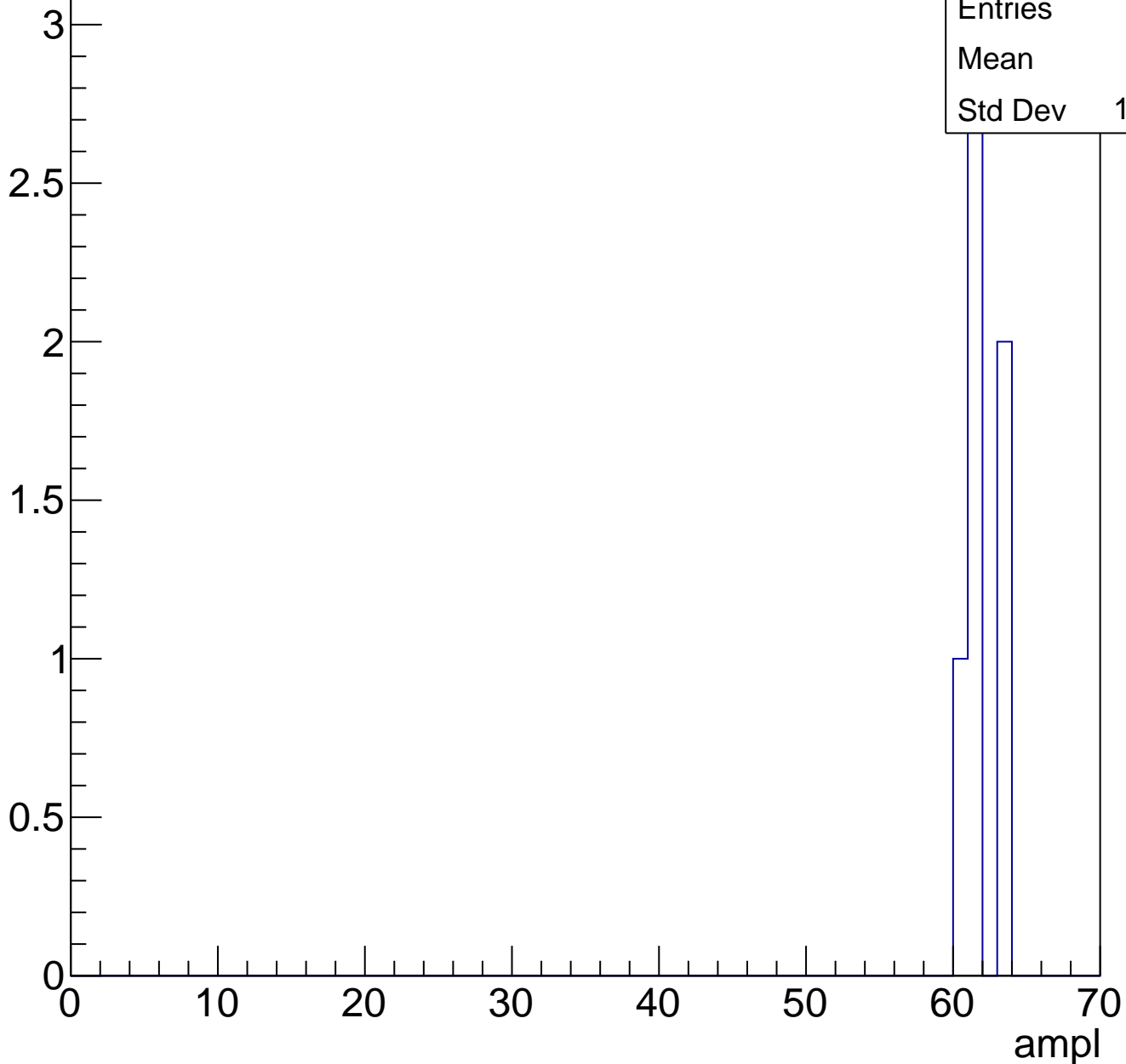
Entries	47
Mean	60.15
Std Dev	2.103



B1L103S, U12-ch117, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch117, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

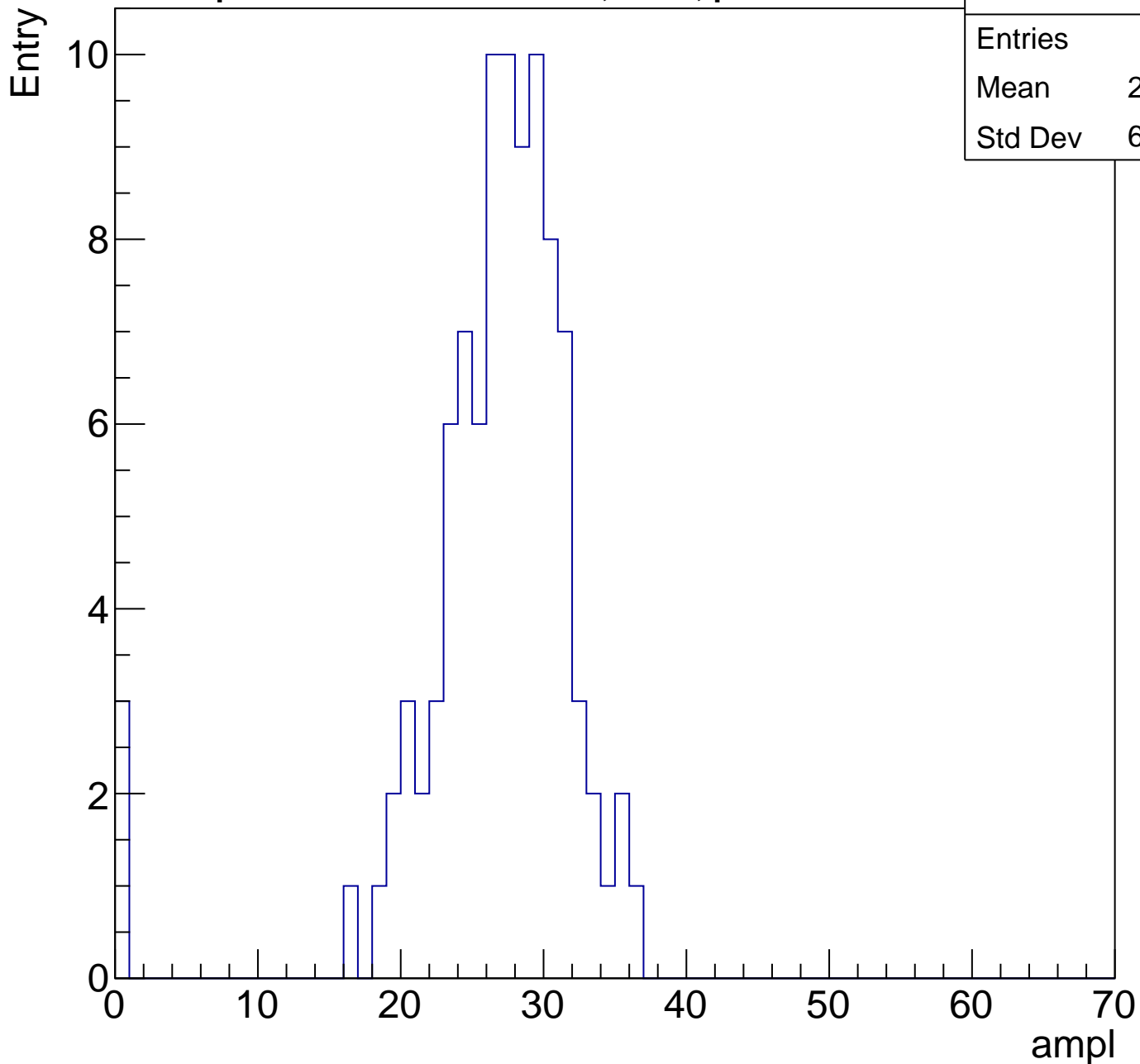
Entries	19
Mean	0
Std Dev	0

ampl

B1L103S, U12-ch118, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	97
Mean	26.05
Std Dev	6.054

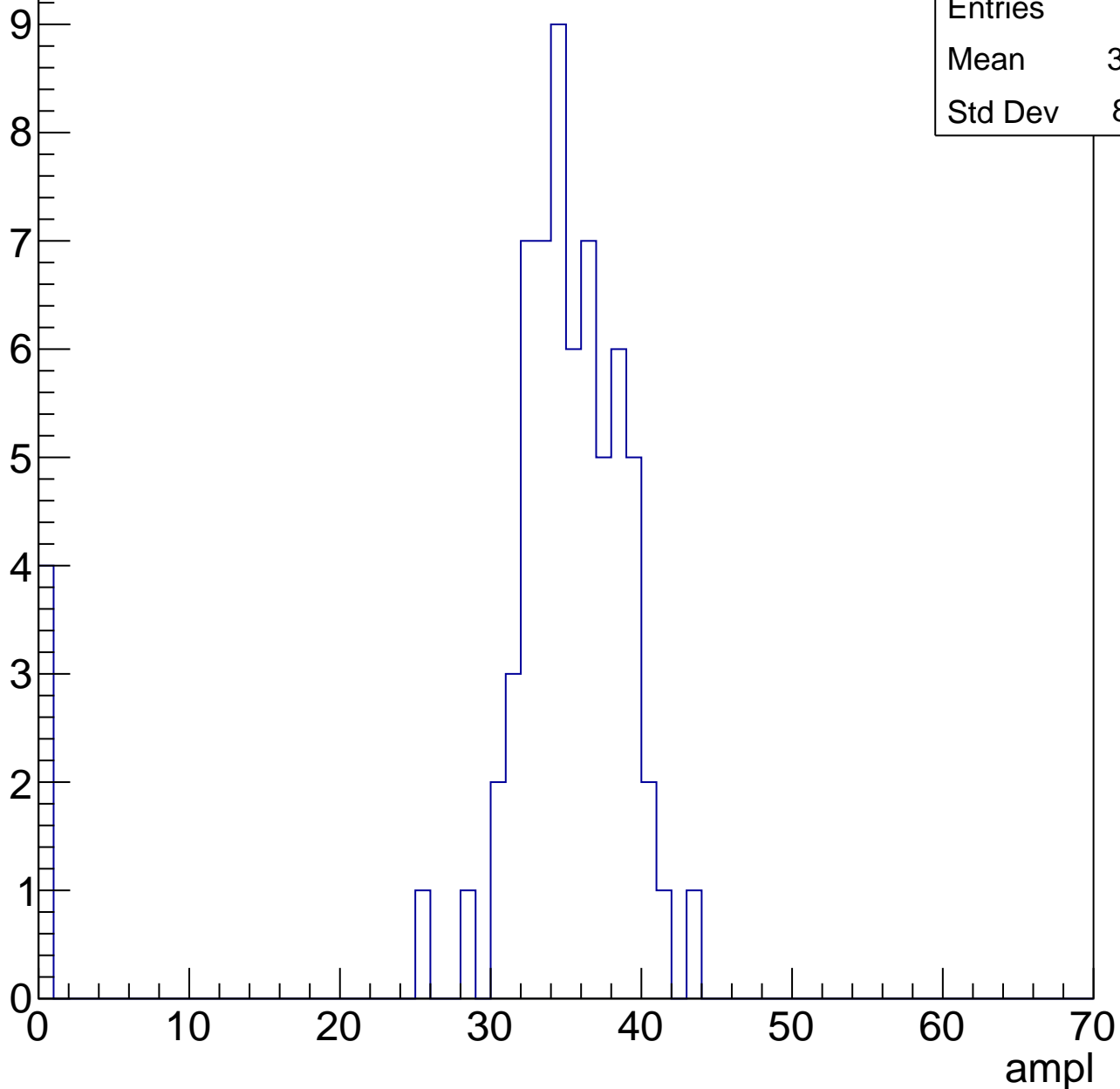


B1L103S, U12-ch118, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	32.85
Std Dev	8.851

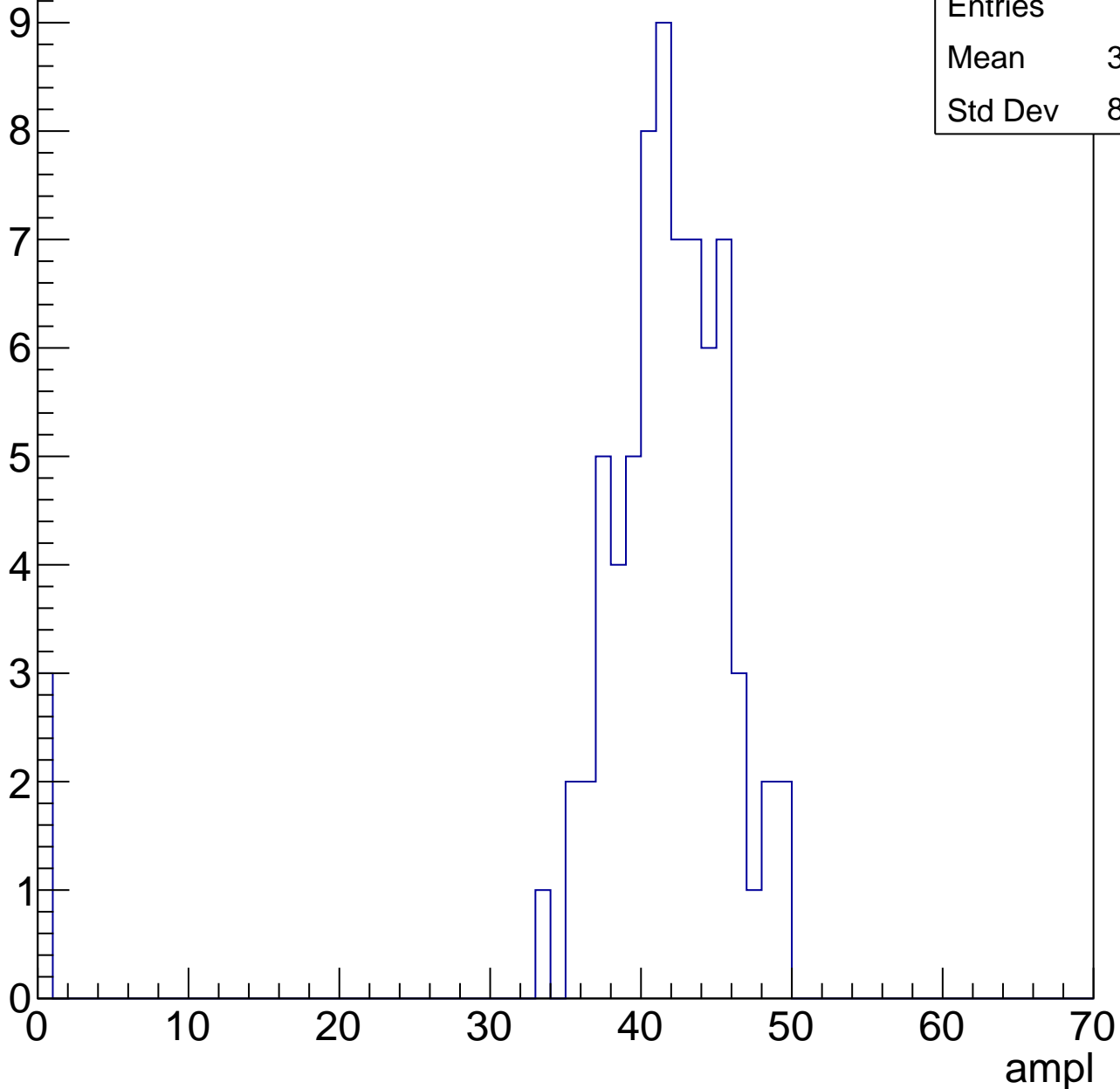


B1L103S, U12-ch118, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	74
Mean	39.85
Std Dev	8.863

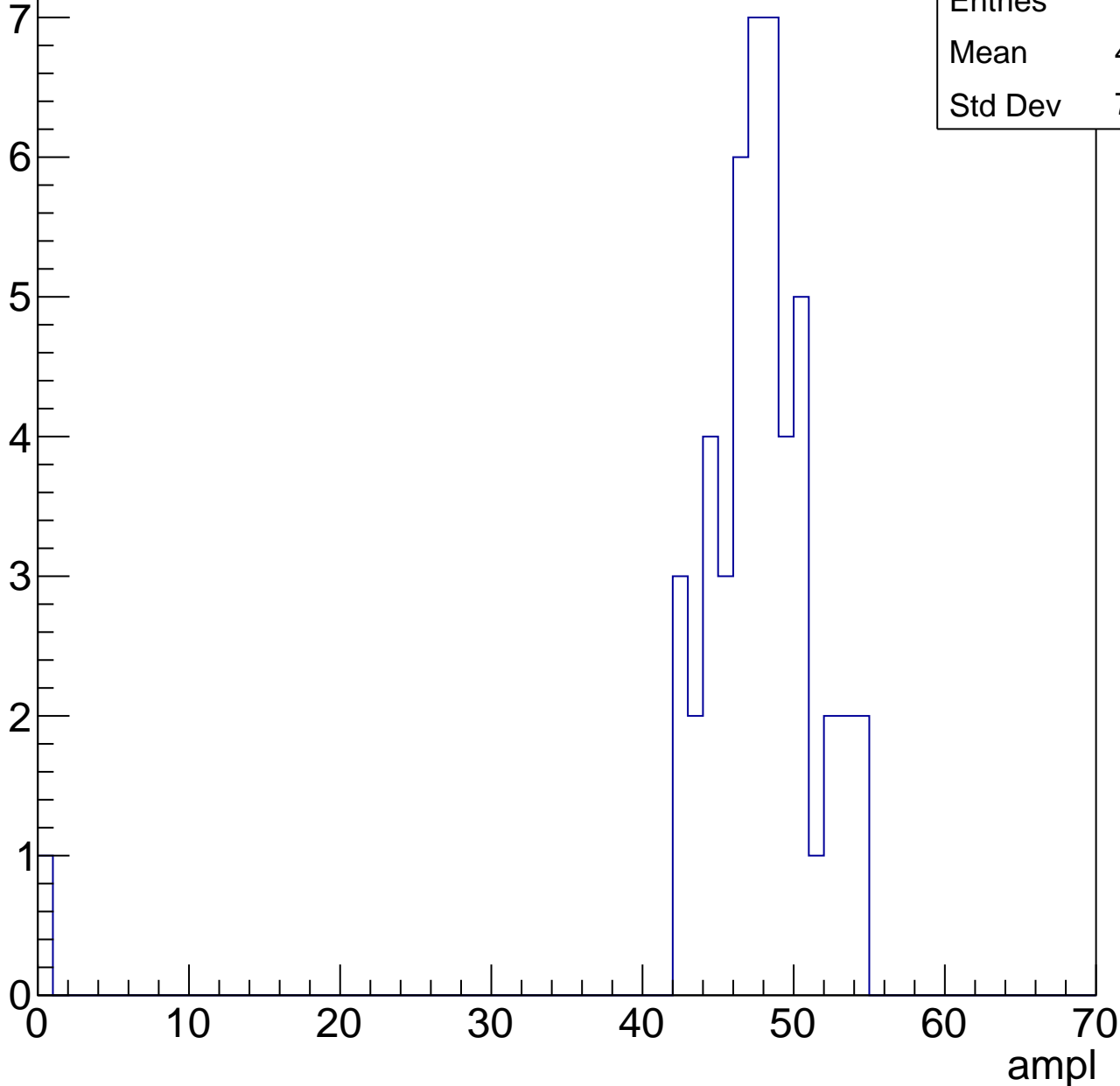


B1L103S, U12-ch118, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	49
Mean	46.51
Std Dev	7.371

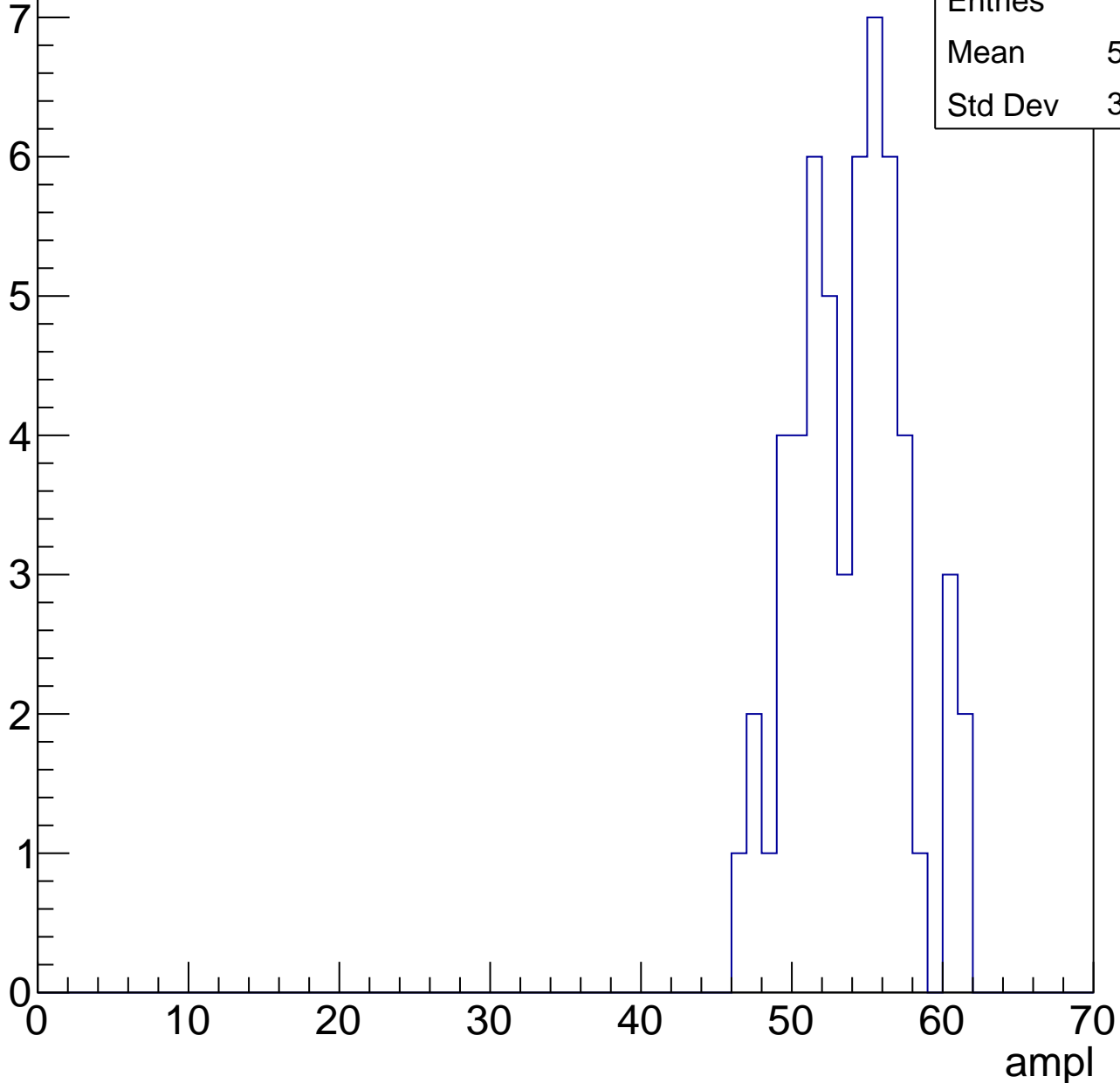


B1L103S, U12-ch118, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	53.49
Std Dev	3.602

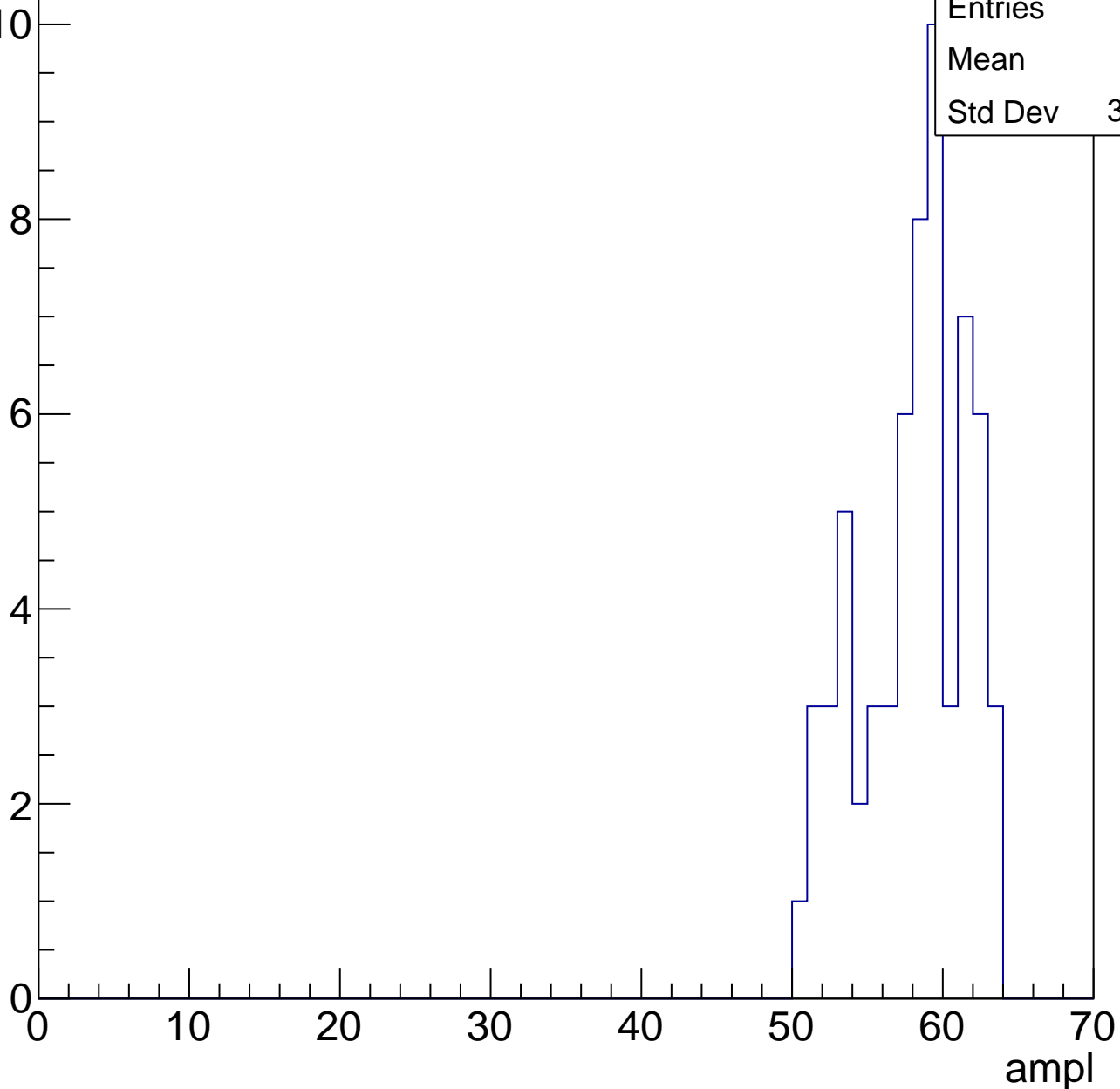


B1L103S, U12-ch118, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	63
Mean	57.6
Std Dev	3.489

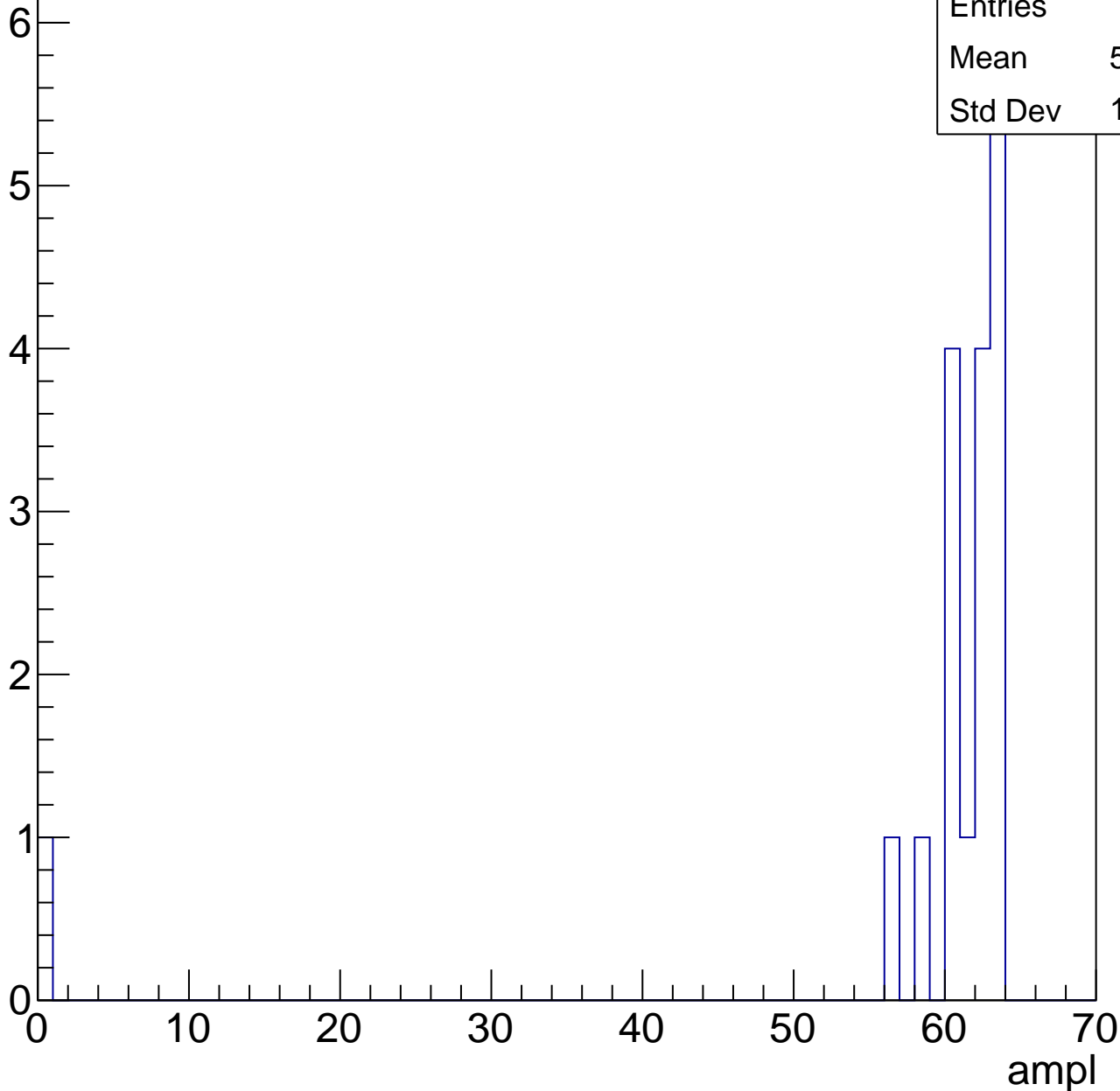


B1L103S, U12-ch118, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

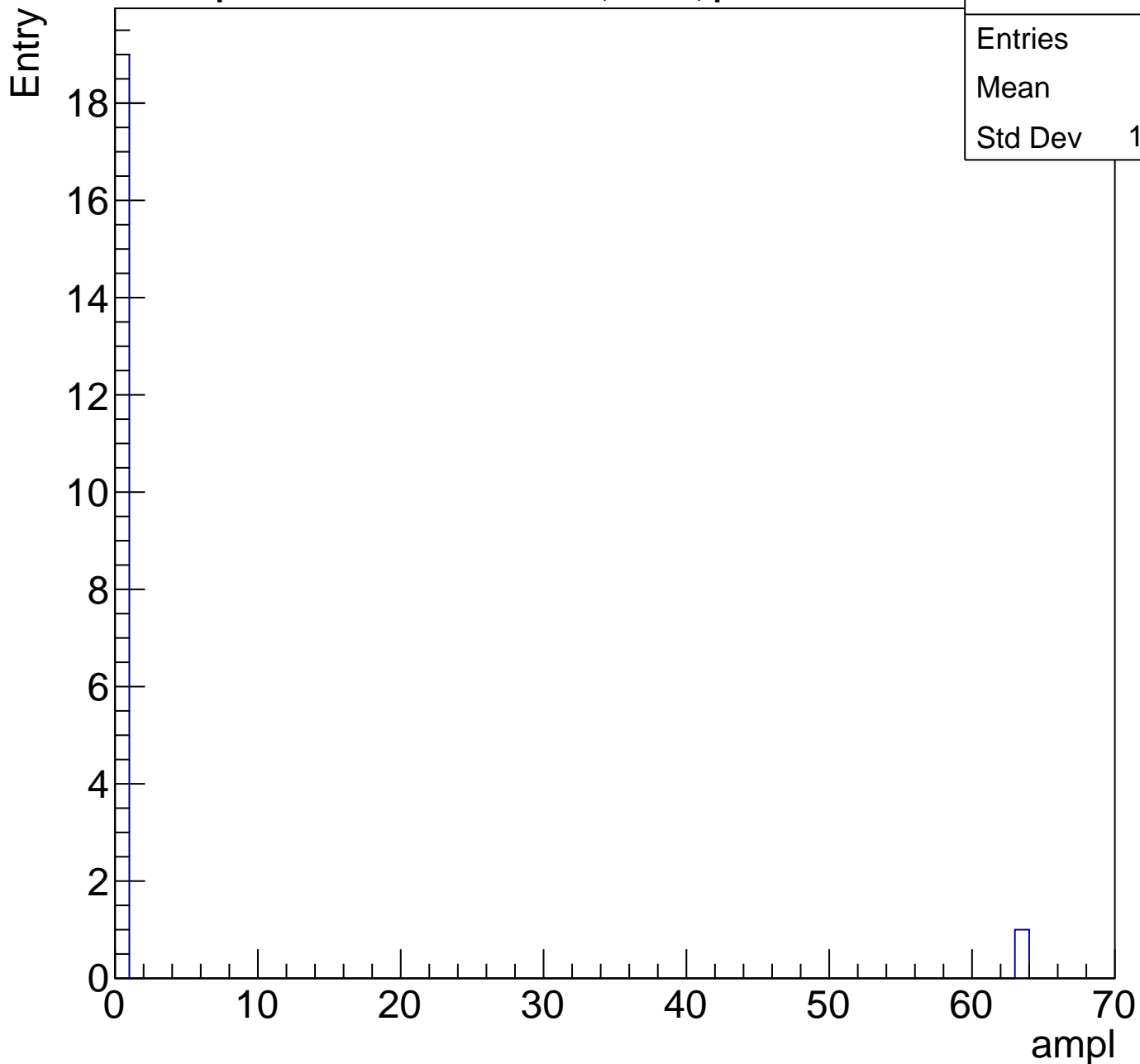
Entries	18
Mean	57.83
Std Dev	14.15



B1L103S, U12-ch118, adc7

calib_packv5_041523_1651.root, FC#0, port C2

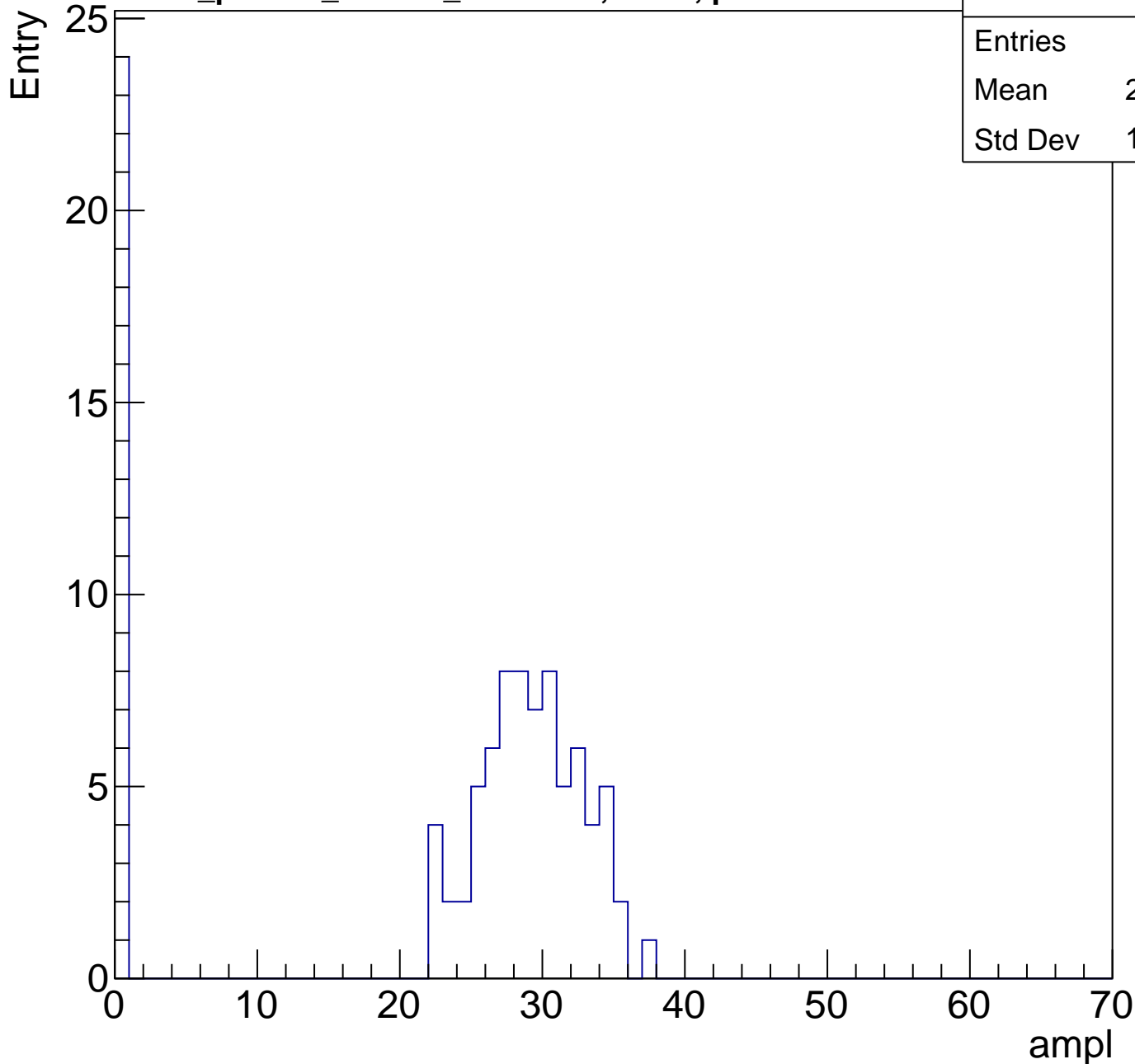
Entries	20
Mean	3.15
Std Dev	13.73



B1L103S, U12-ch119, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	97
Mean	21.67
Std Dev	12.79

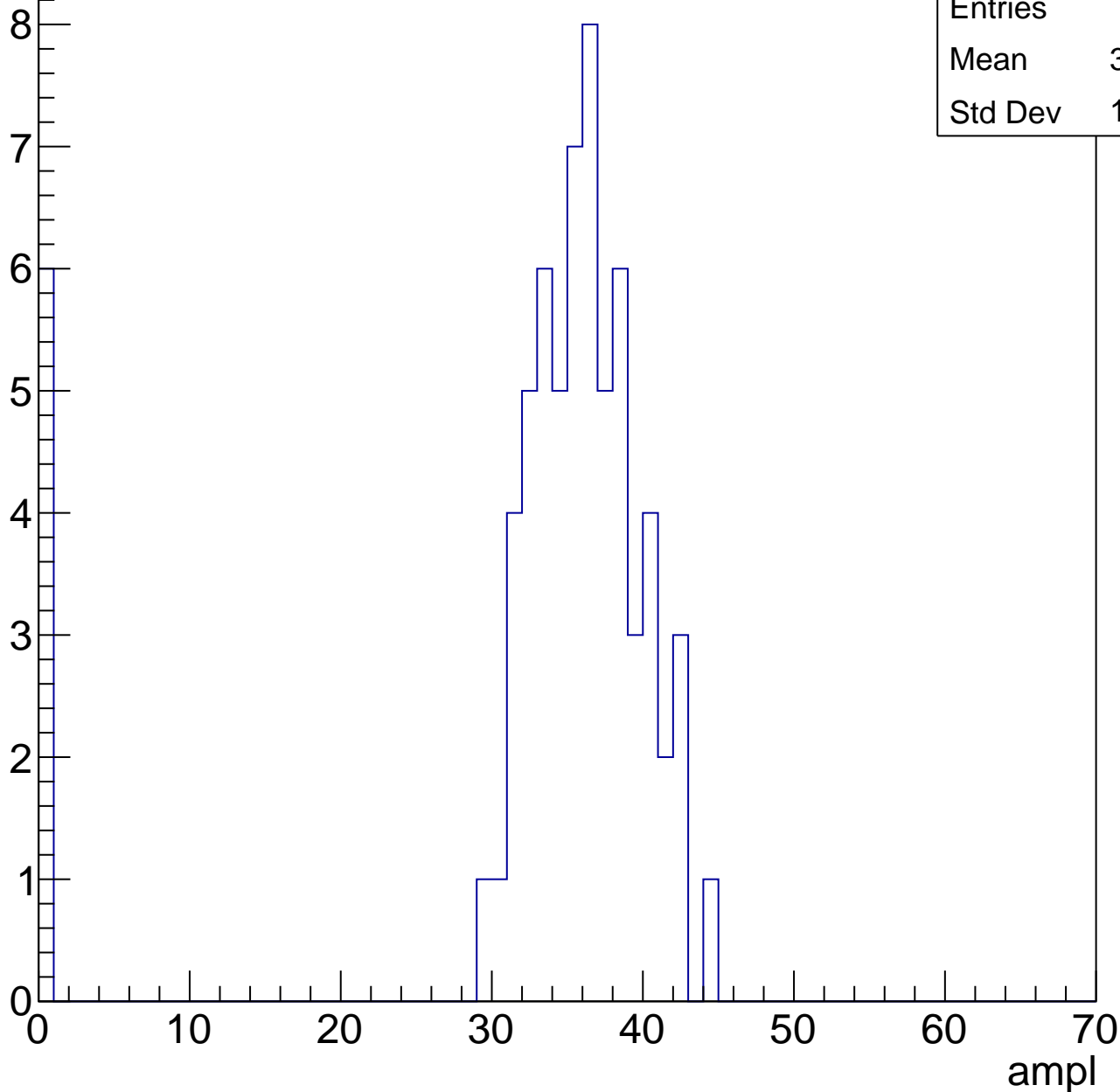


B1L103S, U12-ch119, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

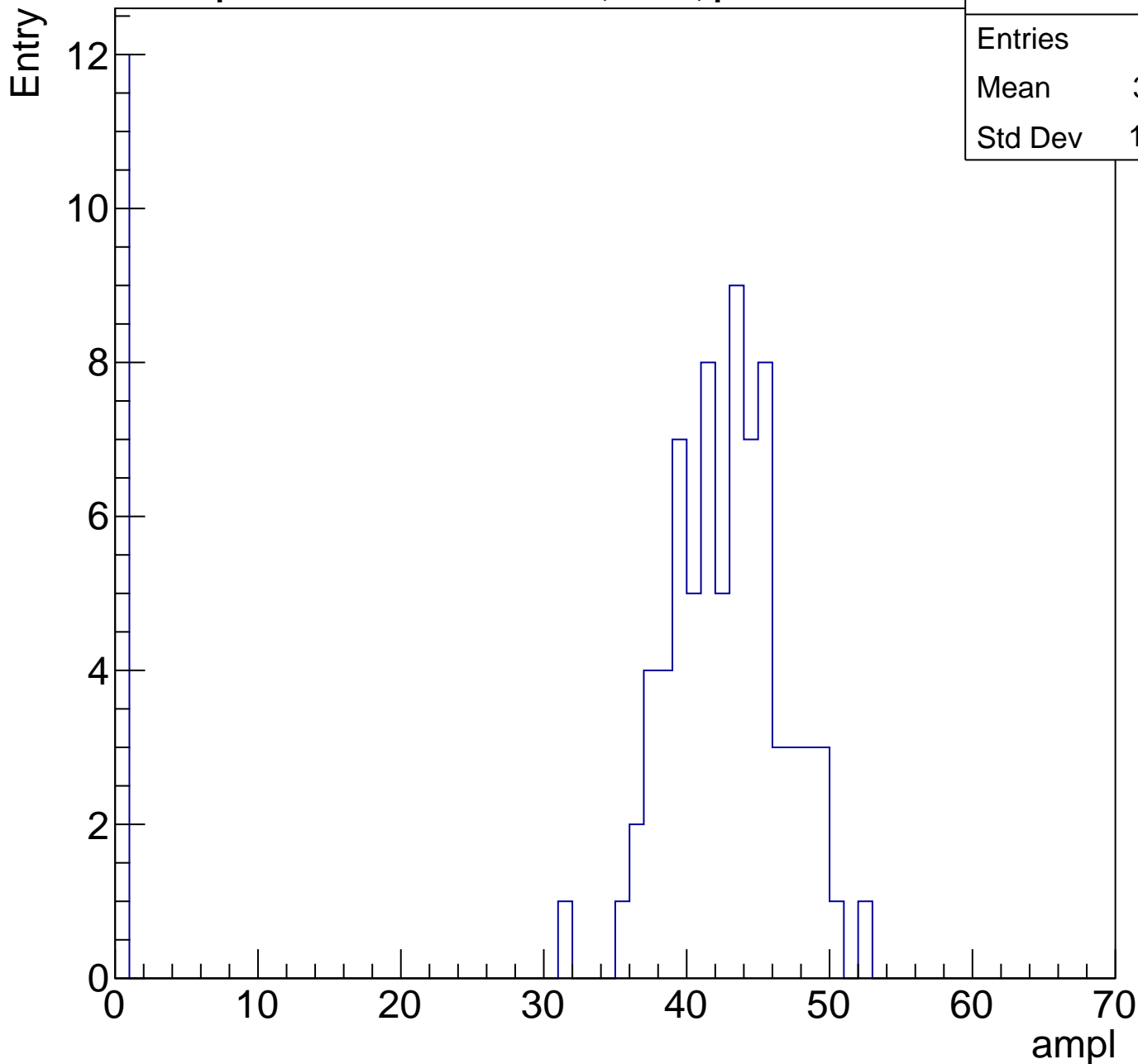
Entries	67
Mean	32.63
Std Dev	10.72



B1L103S, U12-ch119, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	87
Mean	36.51
Std Dev	15.04

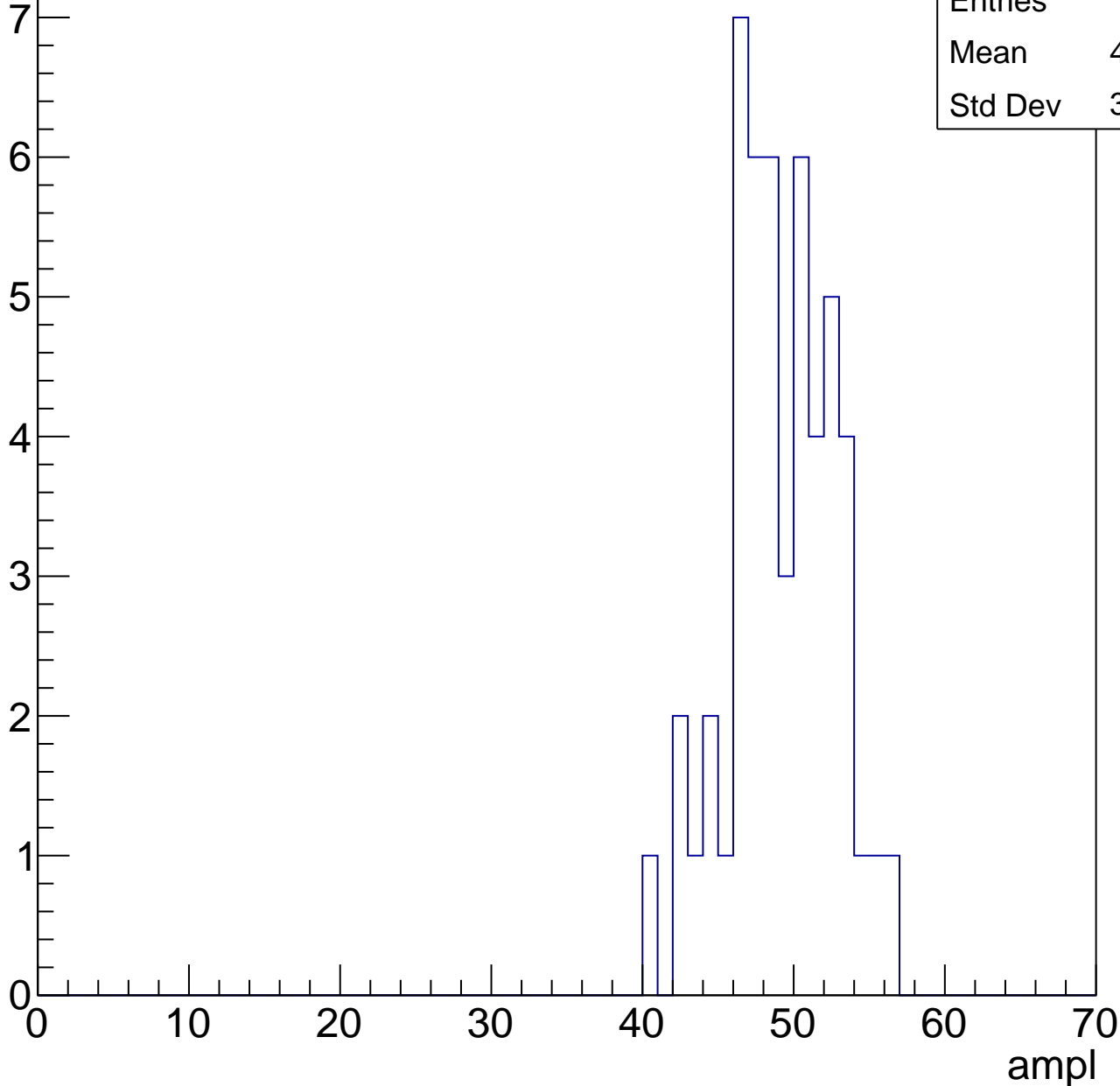


B1L103S, U12-ch119, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	51
Mean	48.63
Std Dev	3.453

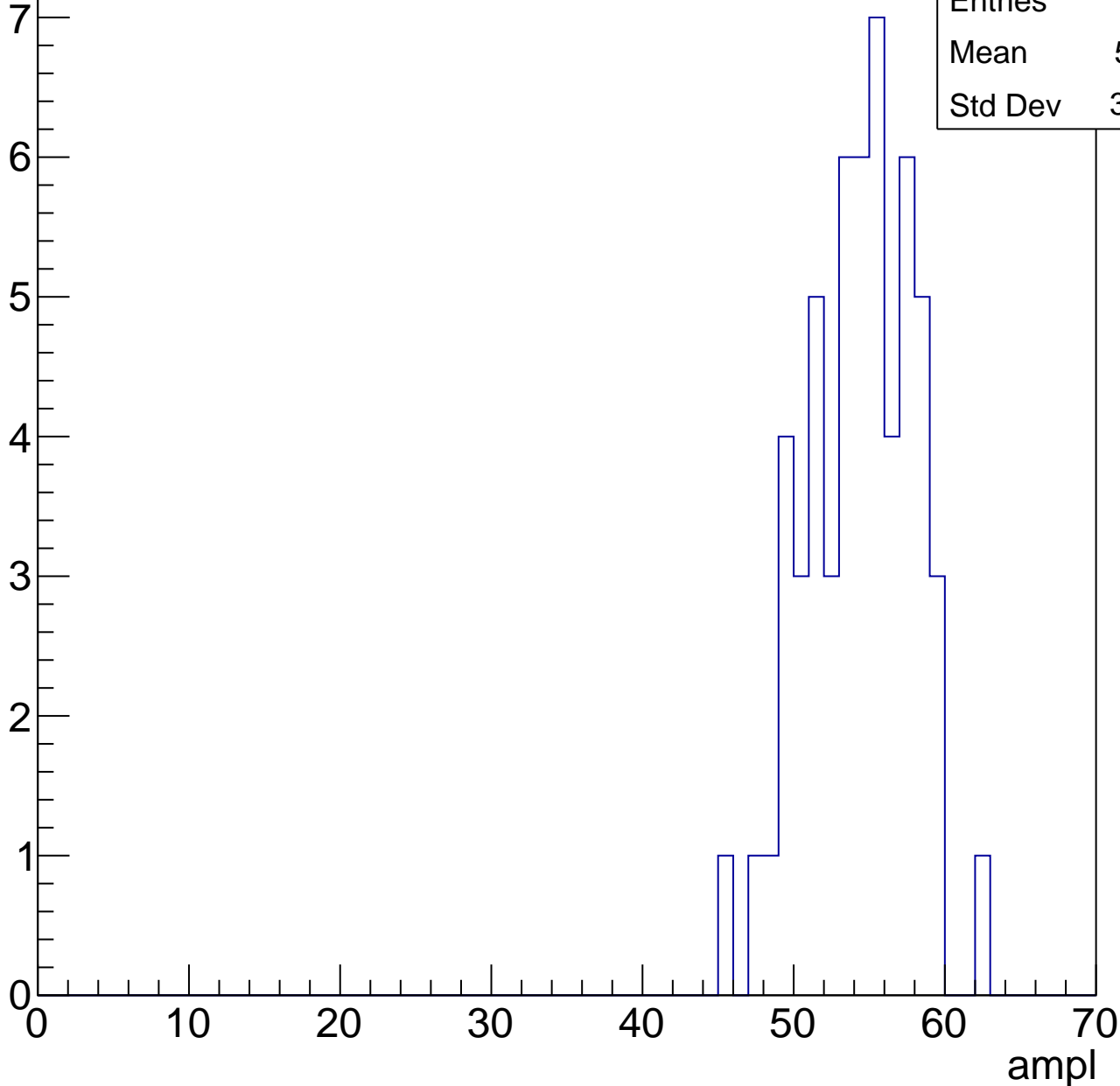


B1L103S, U12-ch119, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

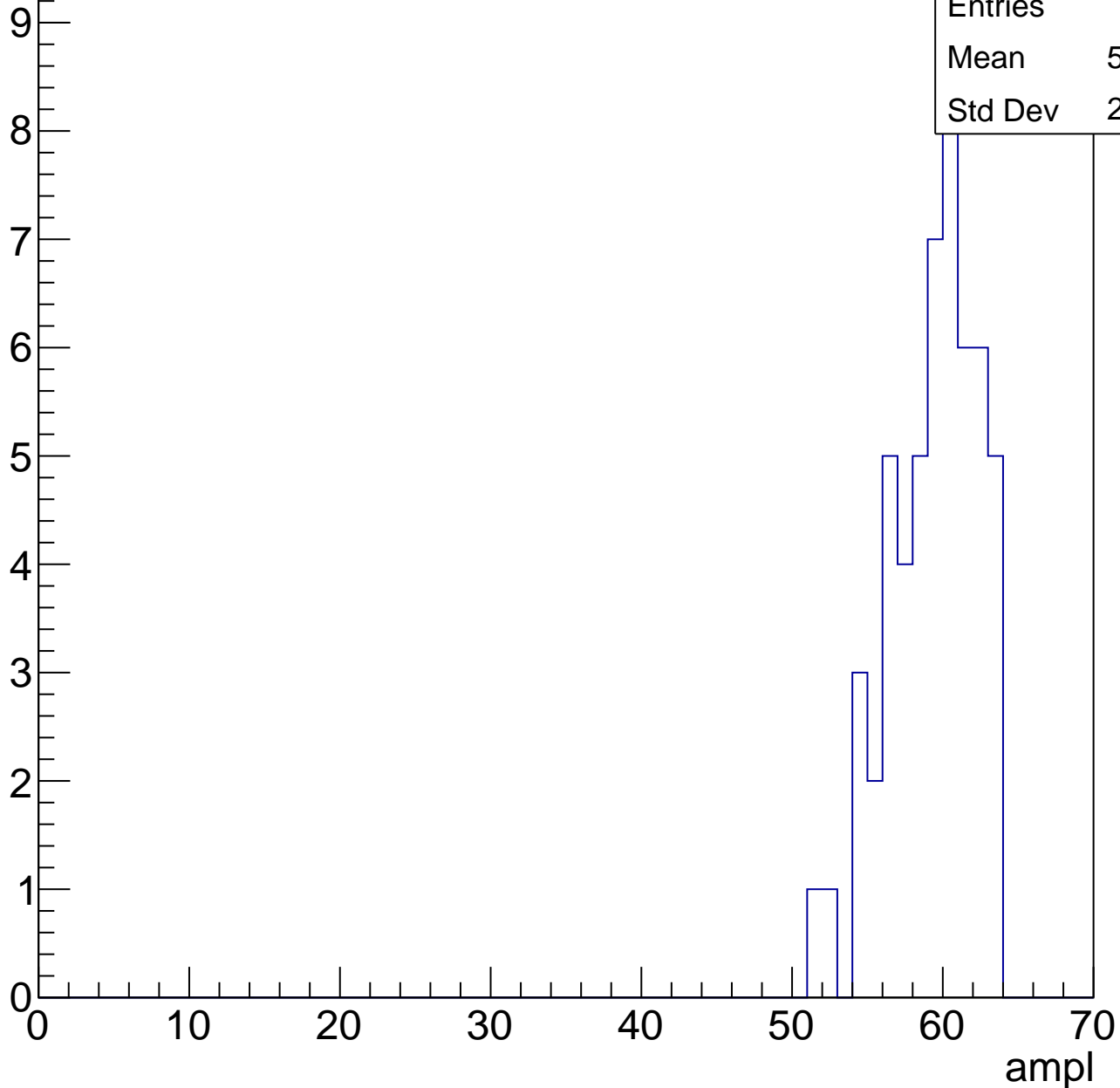
Entries	56
Mean	53.91
Std Dev	3.466



B1L103S, U12-ch119, adc5

calib_packv5_041523_1651.root, FC#0, port C2

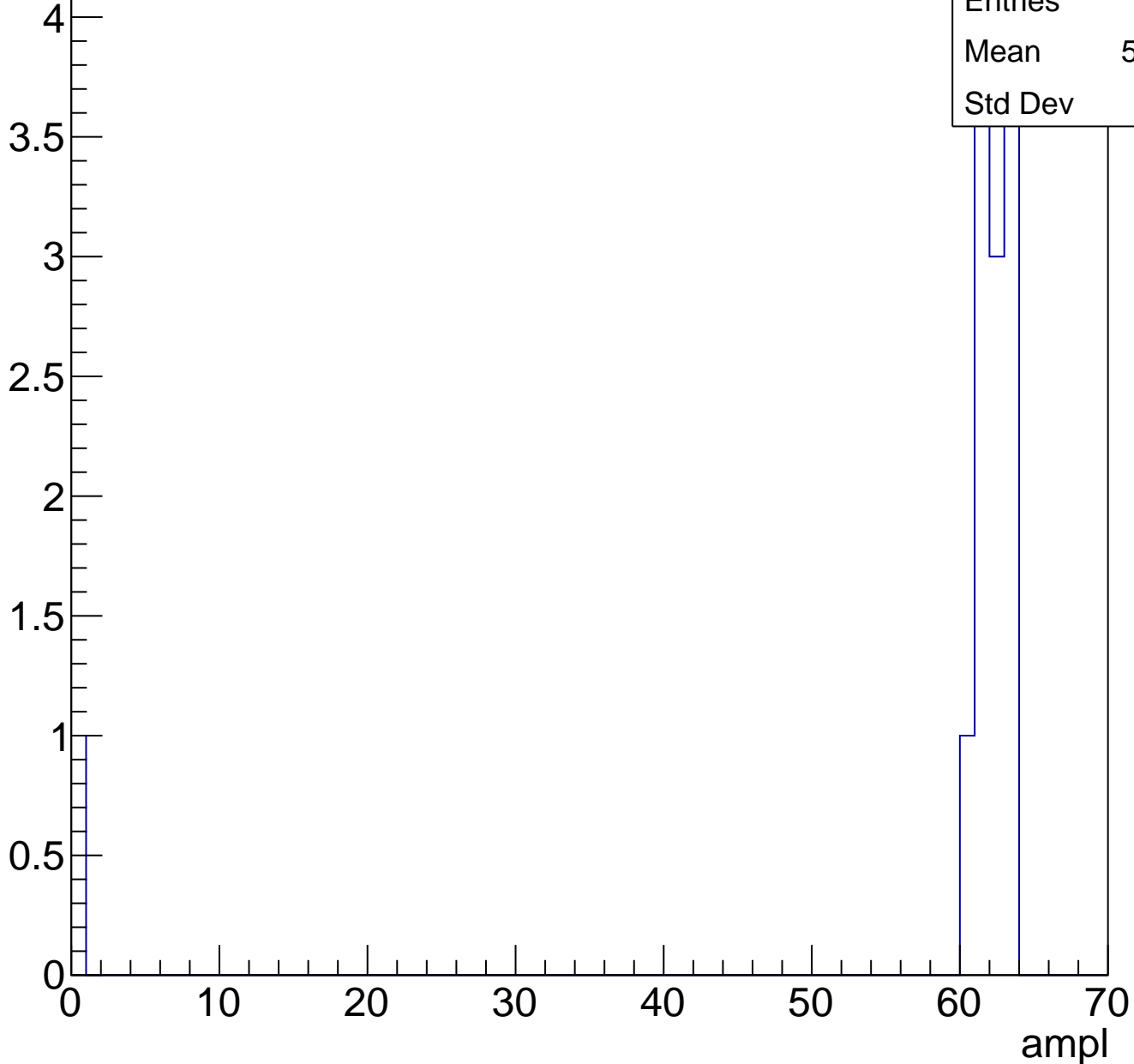
Entry



B1L103S, U12-ch119, adc6

calib_packv5_041523_1651.root, FC#0, port C2

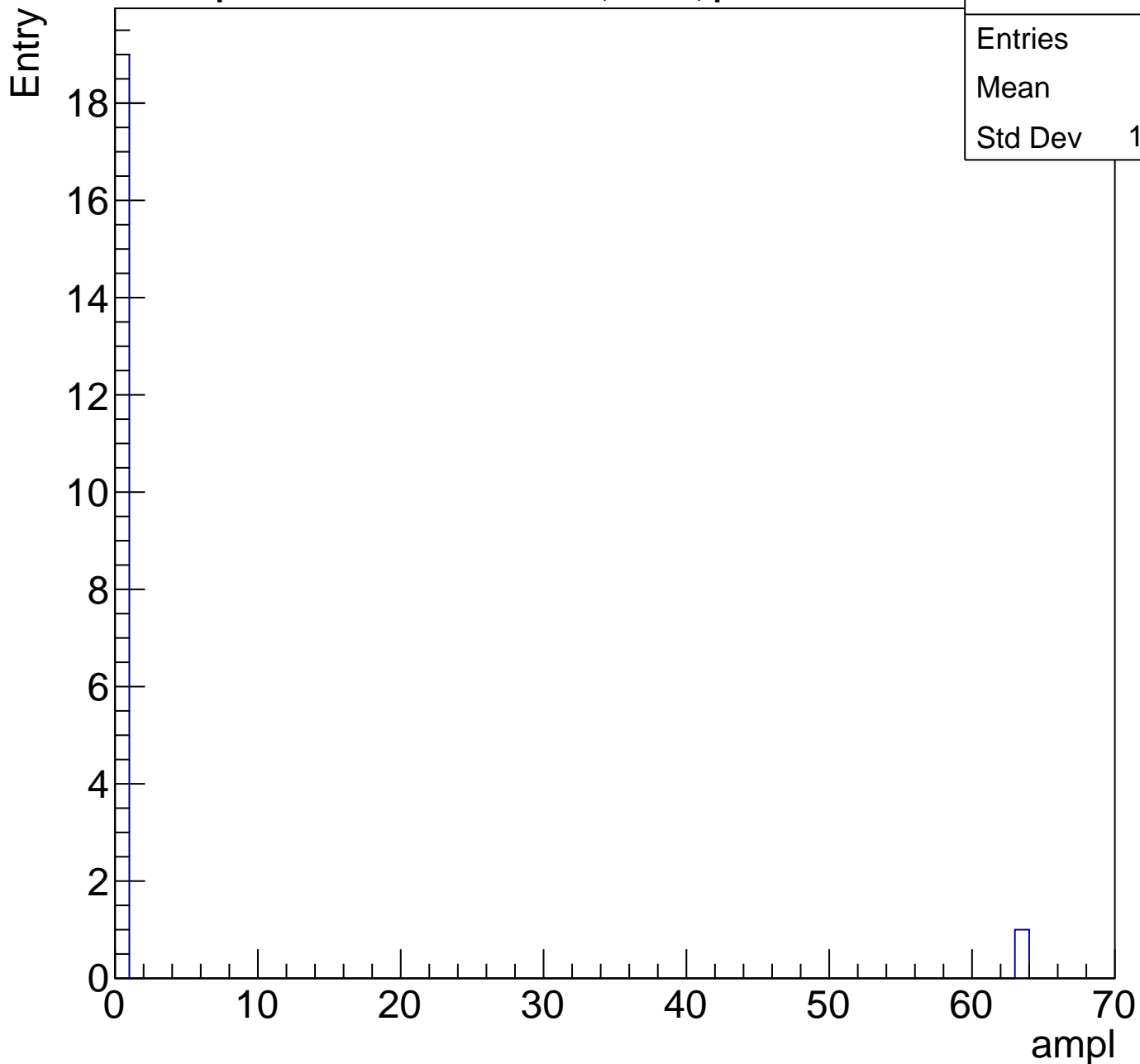
Entry



B1L103S, U12-ch119, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.15
Std Dev	13.73



B1L103S, U12-ch120, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	98
Mean	23.74
Std Dev	11.43

Entry

16
14
12
10
8
6
4
2
0

0

10

20

30

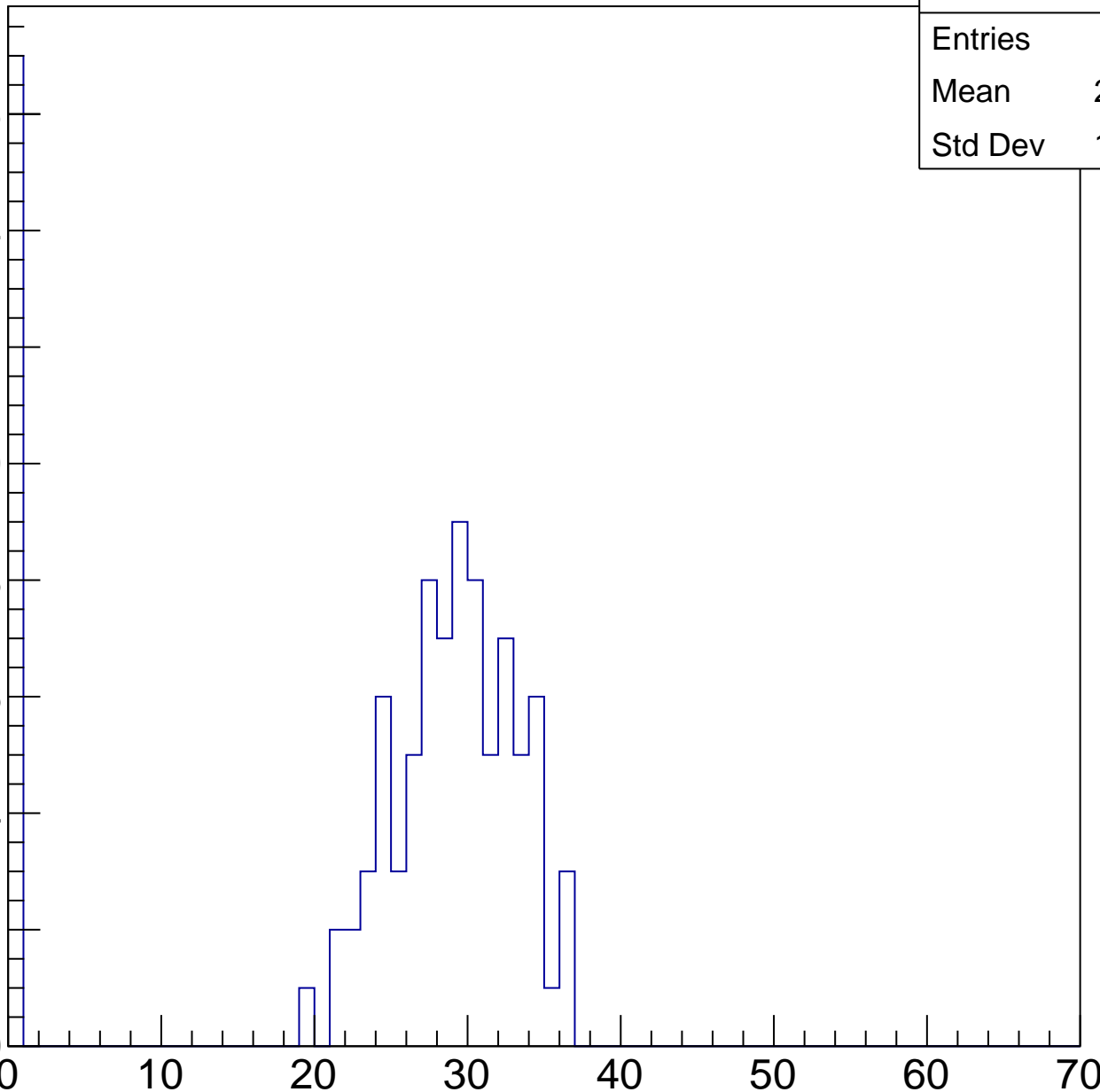
40

50

60

70

ampl

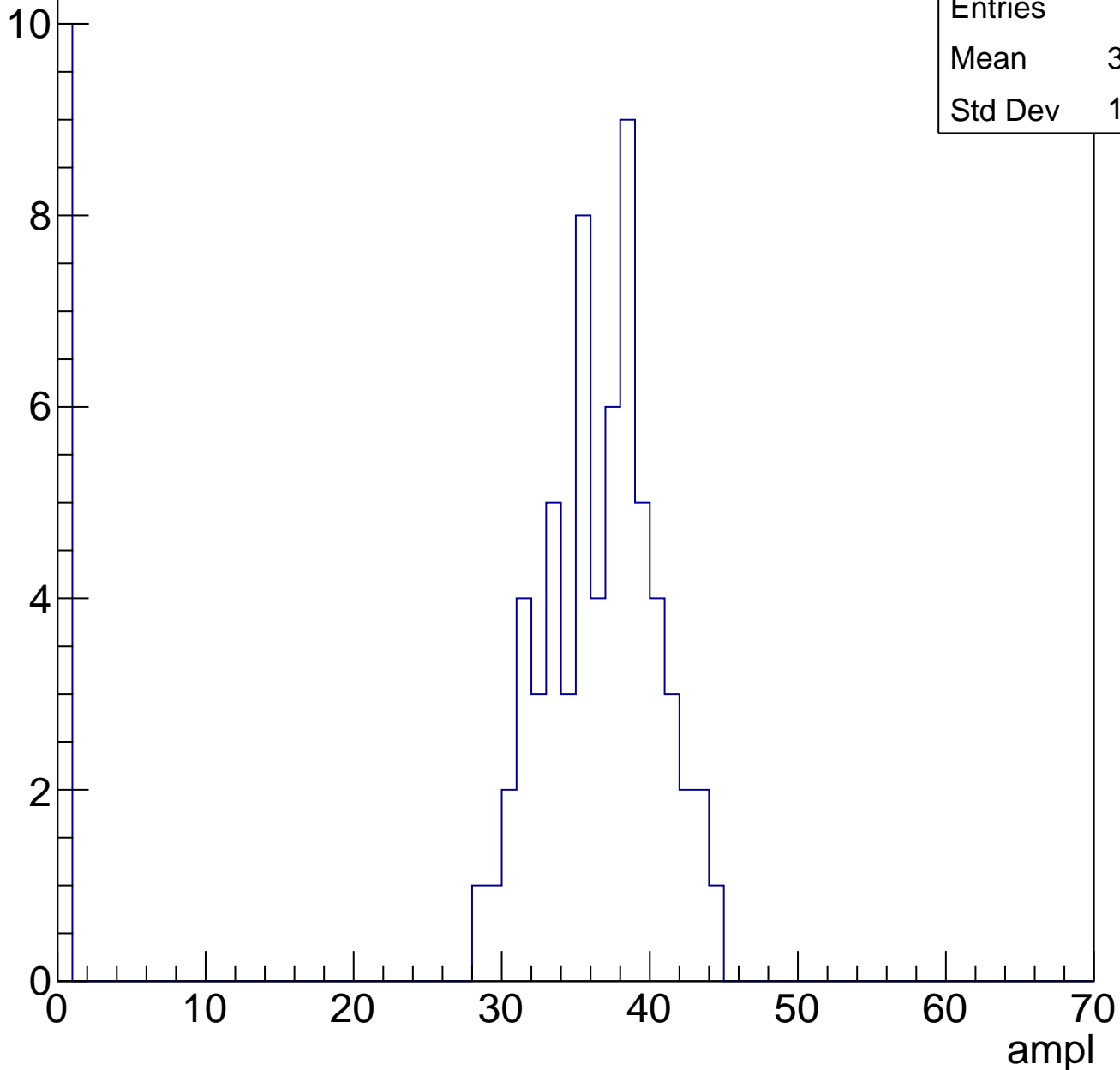


B1L103S, U12-ch120, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	73
Mean	31.29
Std Dev	12.93

Entry

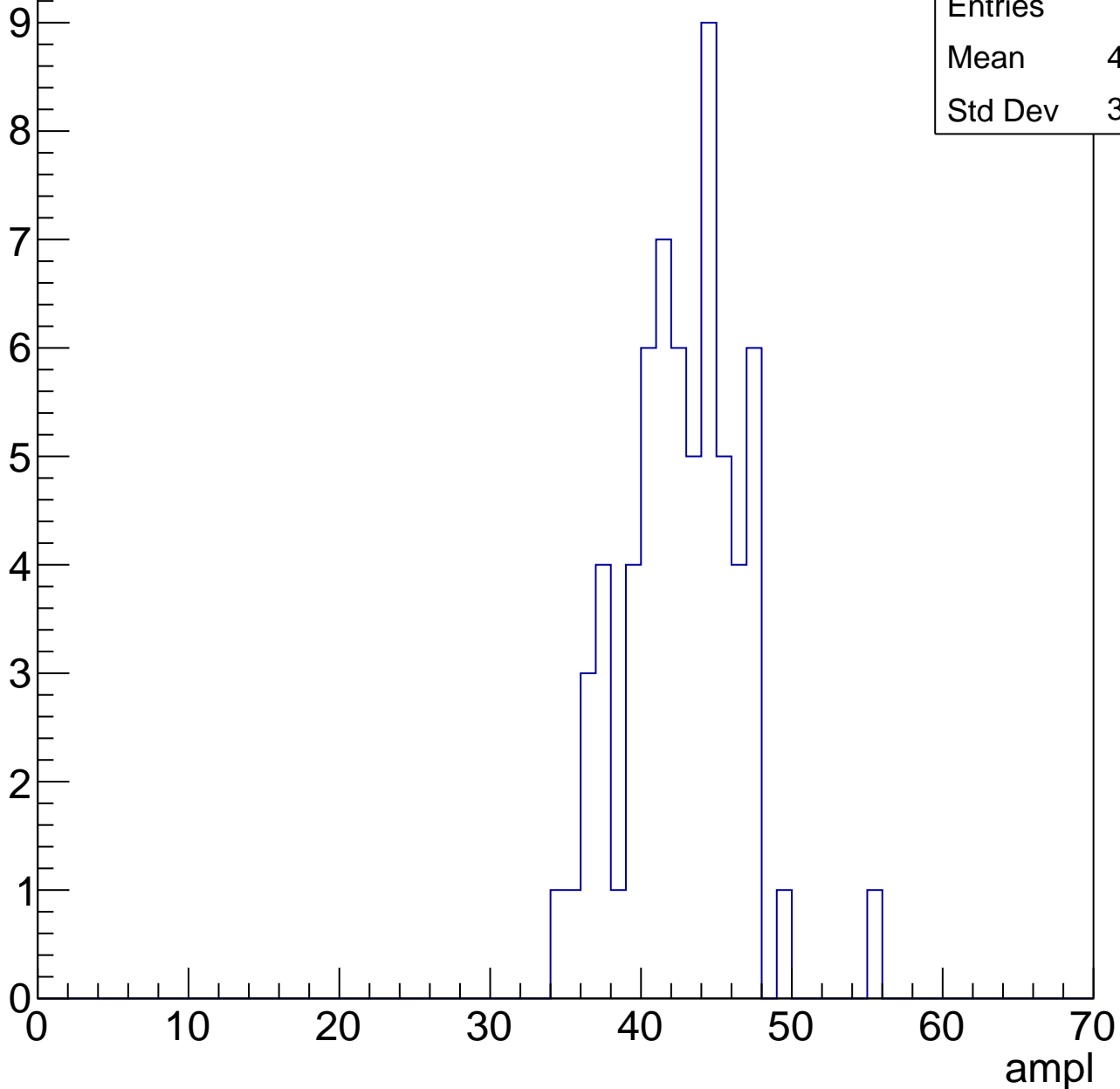


B1L103S, U12-ch120, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	42.25
Std Dev	3.787

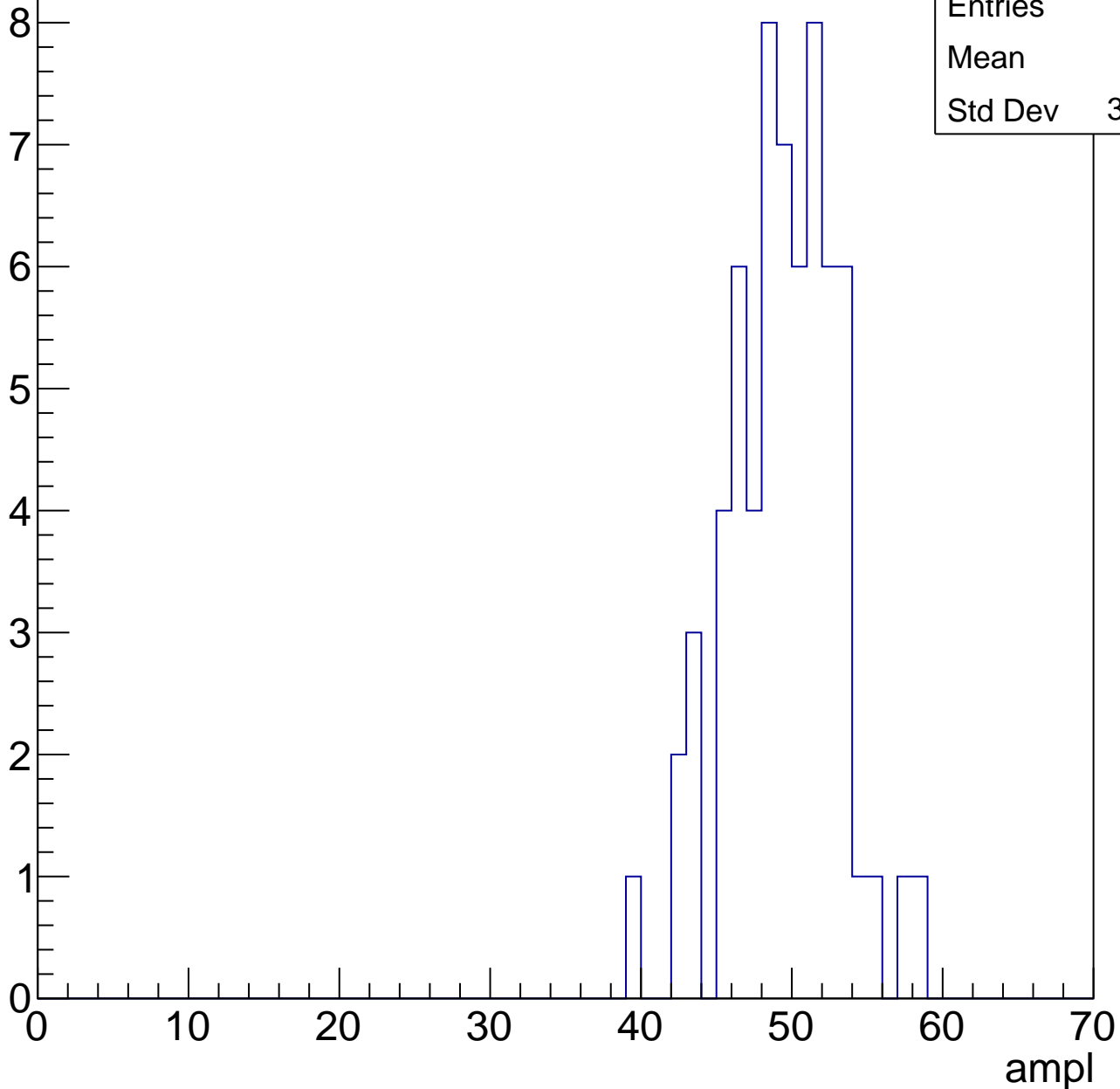


B1L103S, U12-ch120, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	49
Std Dev	3.599

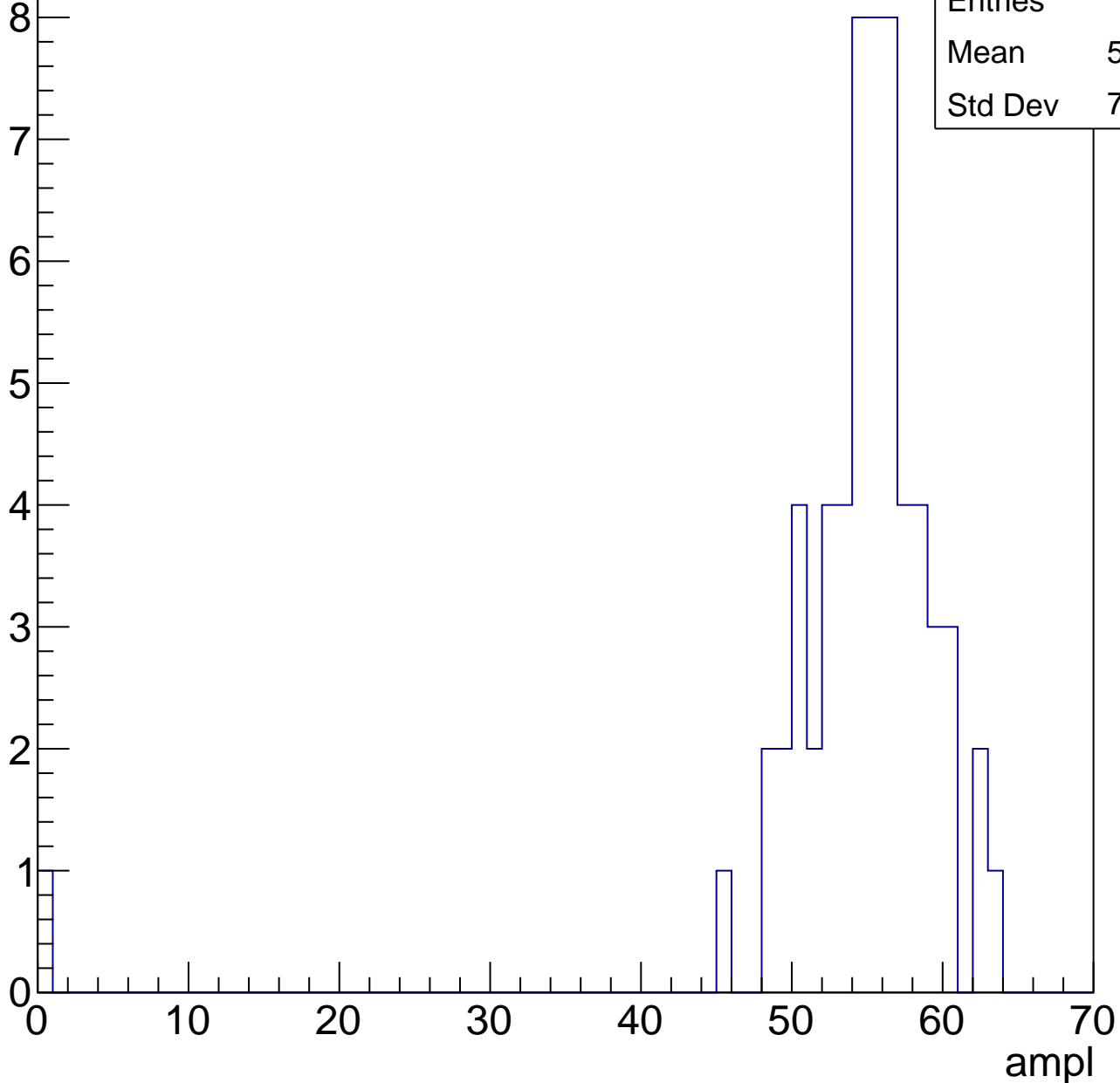


B1L103S, U12-ch120, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	53.85
Std Dev	7.842

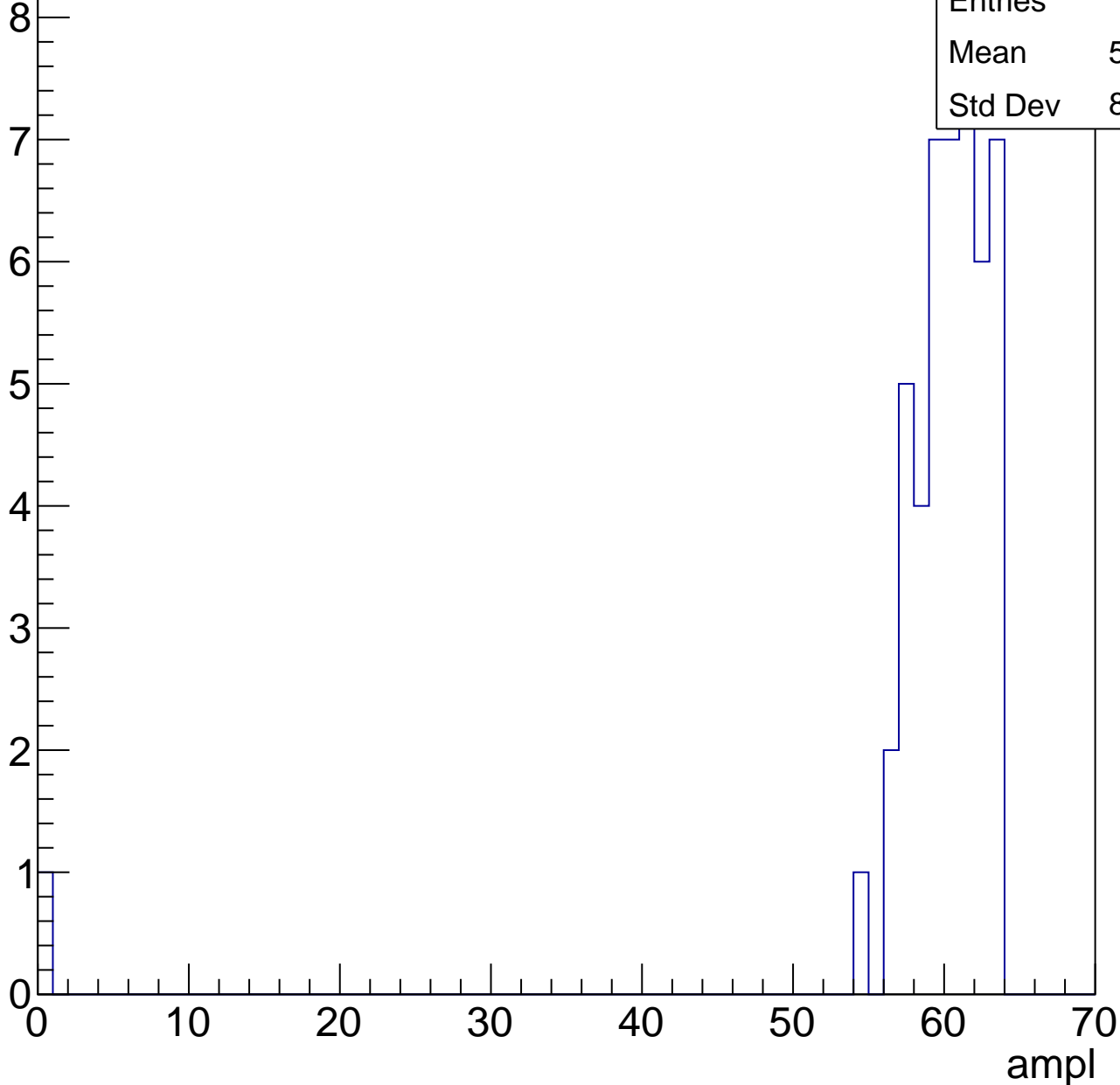


B1L103S, U12-ch120, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

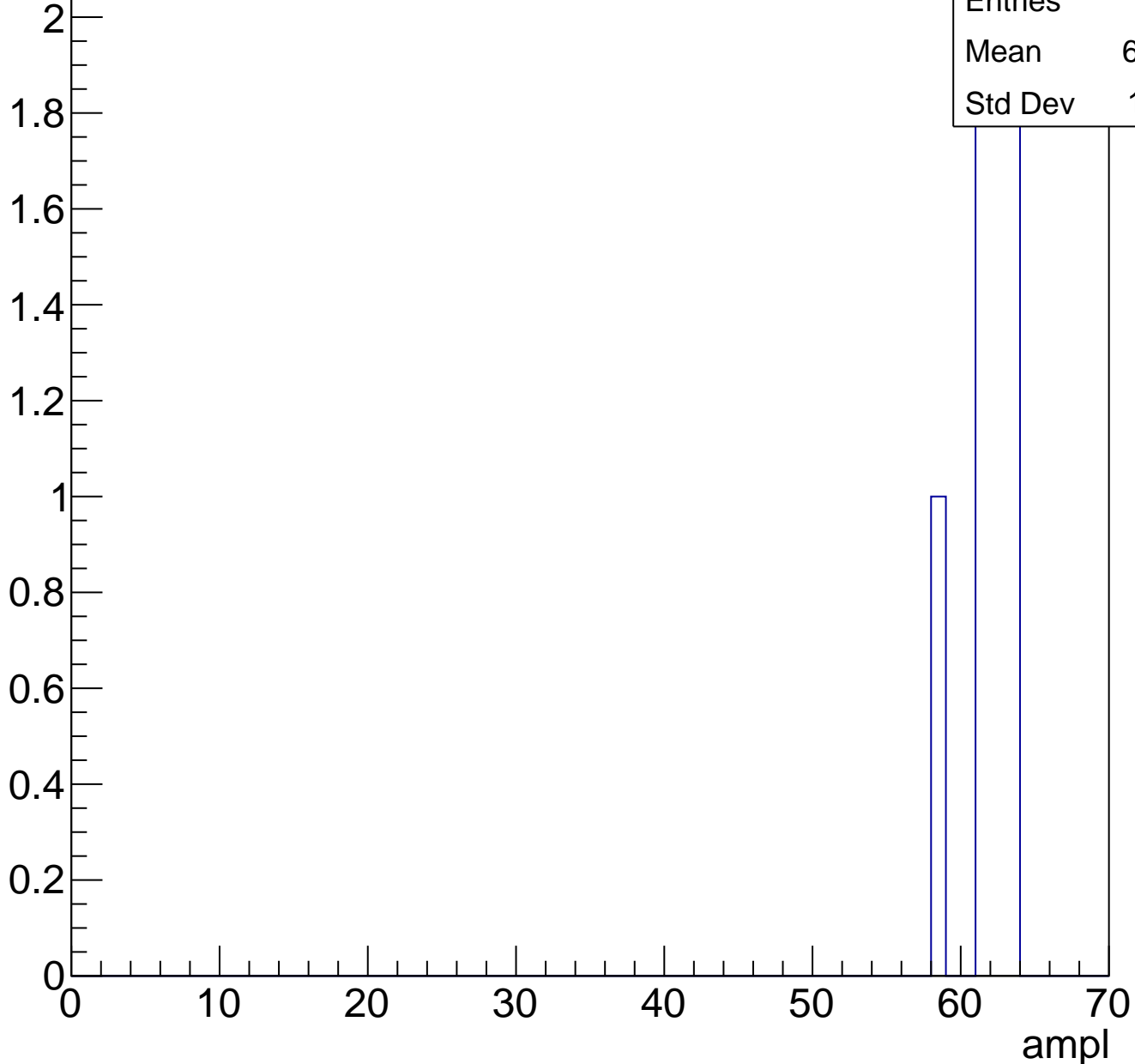
Entries	48
Mean	58.69
Std Dev	8.837



B1L103S, U12-ch120, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch120, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	18
Mean	0
Std Dev	0

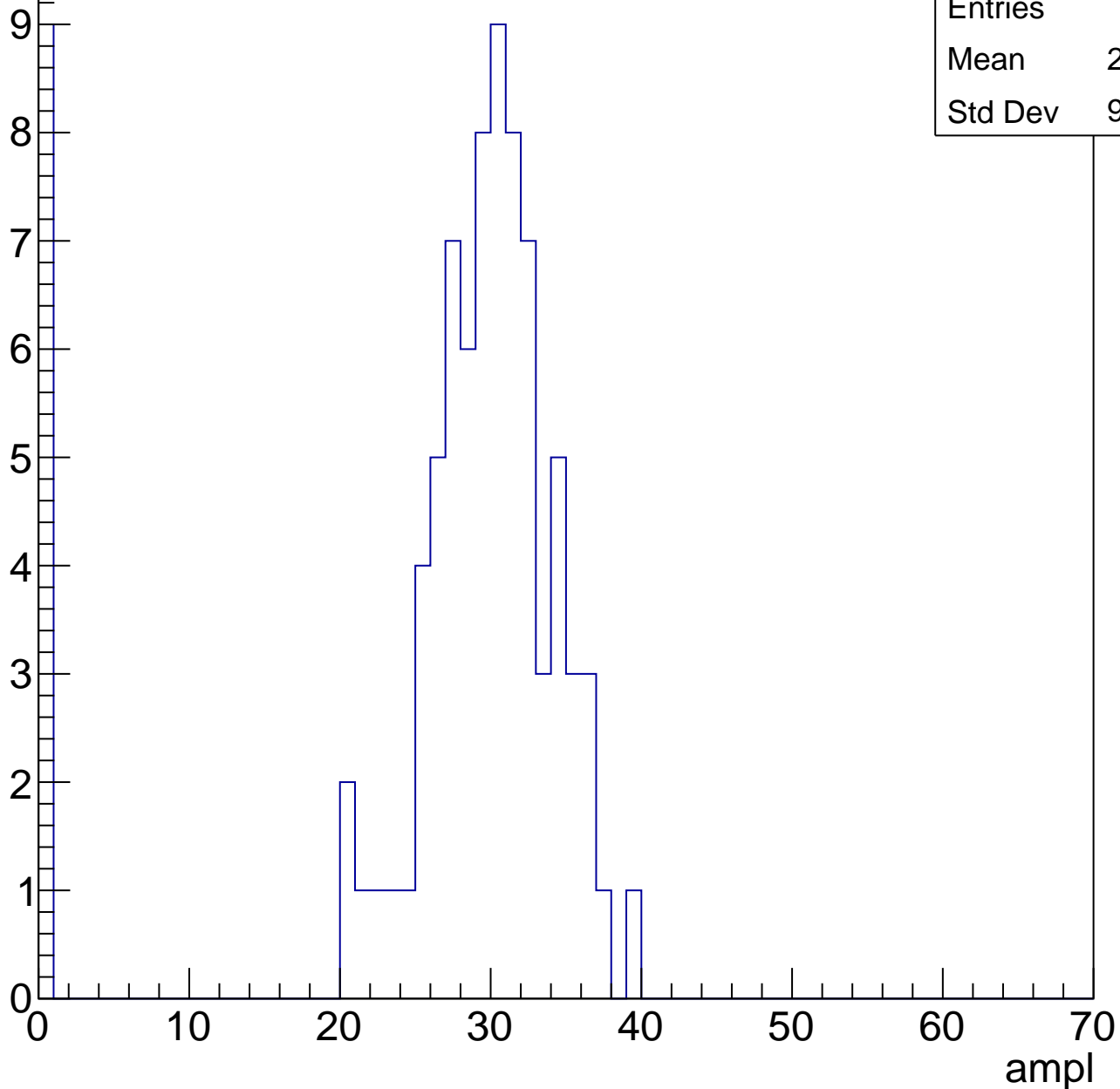
ampl

B1L103S, U12-ch121, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	85
Mean	26.46
Std Dev	9.819

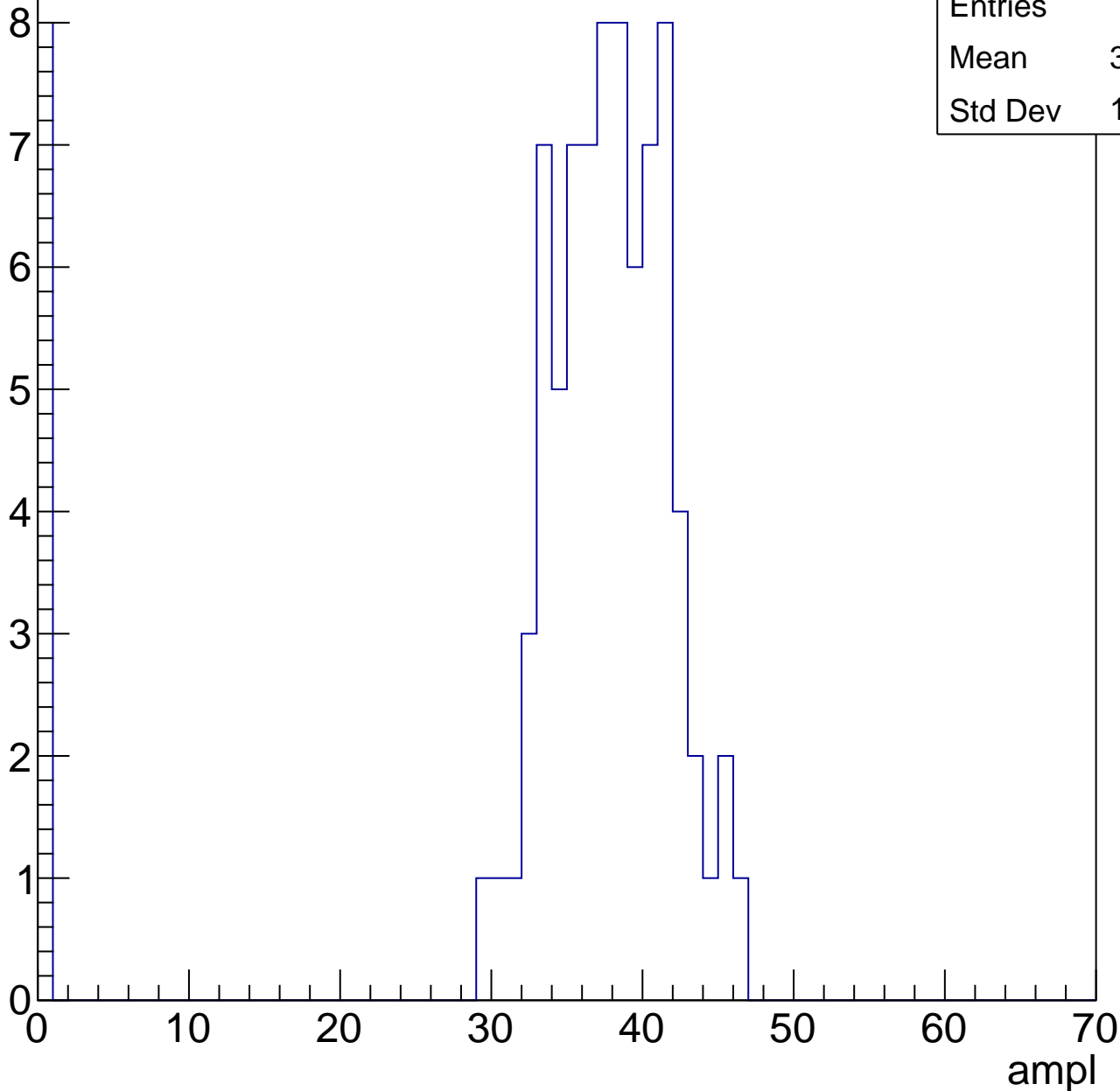


B1L103S, U12-ch121, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	87
Mean	34.02
Std Dev	11.37

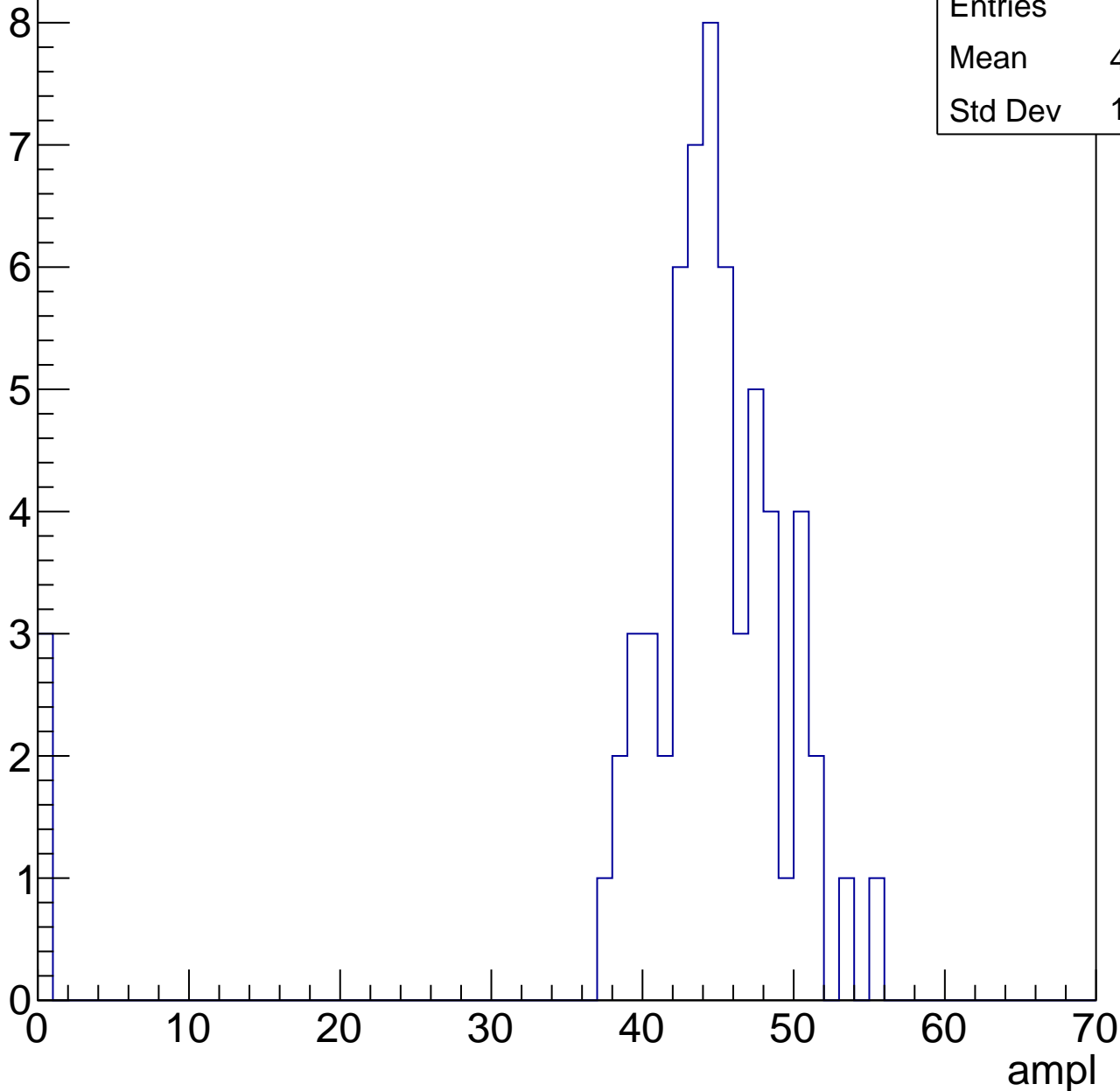


B1L103S, U12-ch121, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	42.44
Std Dev	10.27

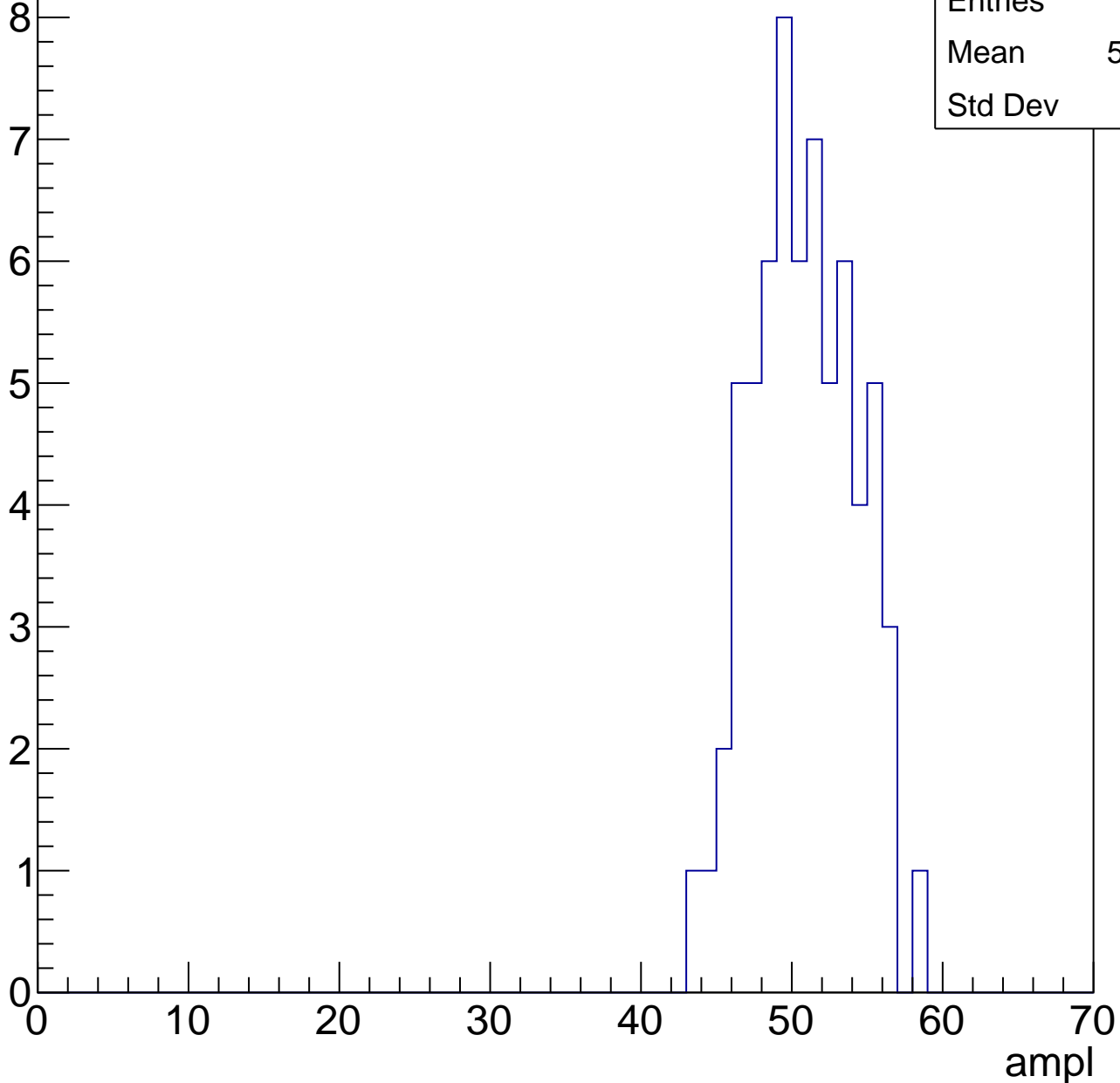


B1L103S, U12-ch121, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	50.37
Std Dev	3.34

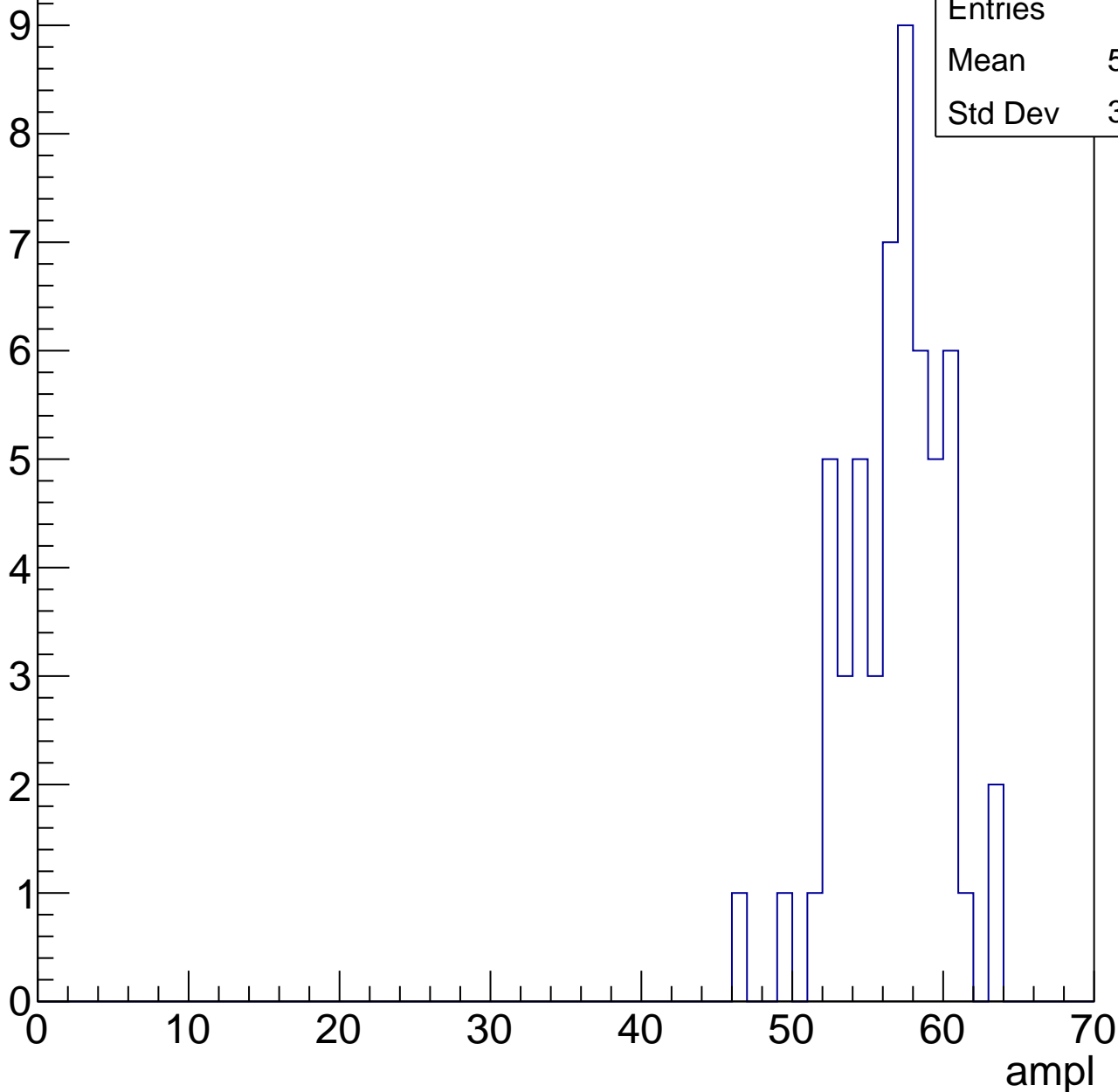


B1L103S, U12-ch121, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	56.27
Std Dev	3.294

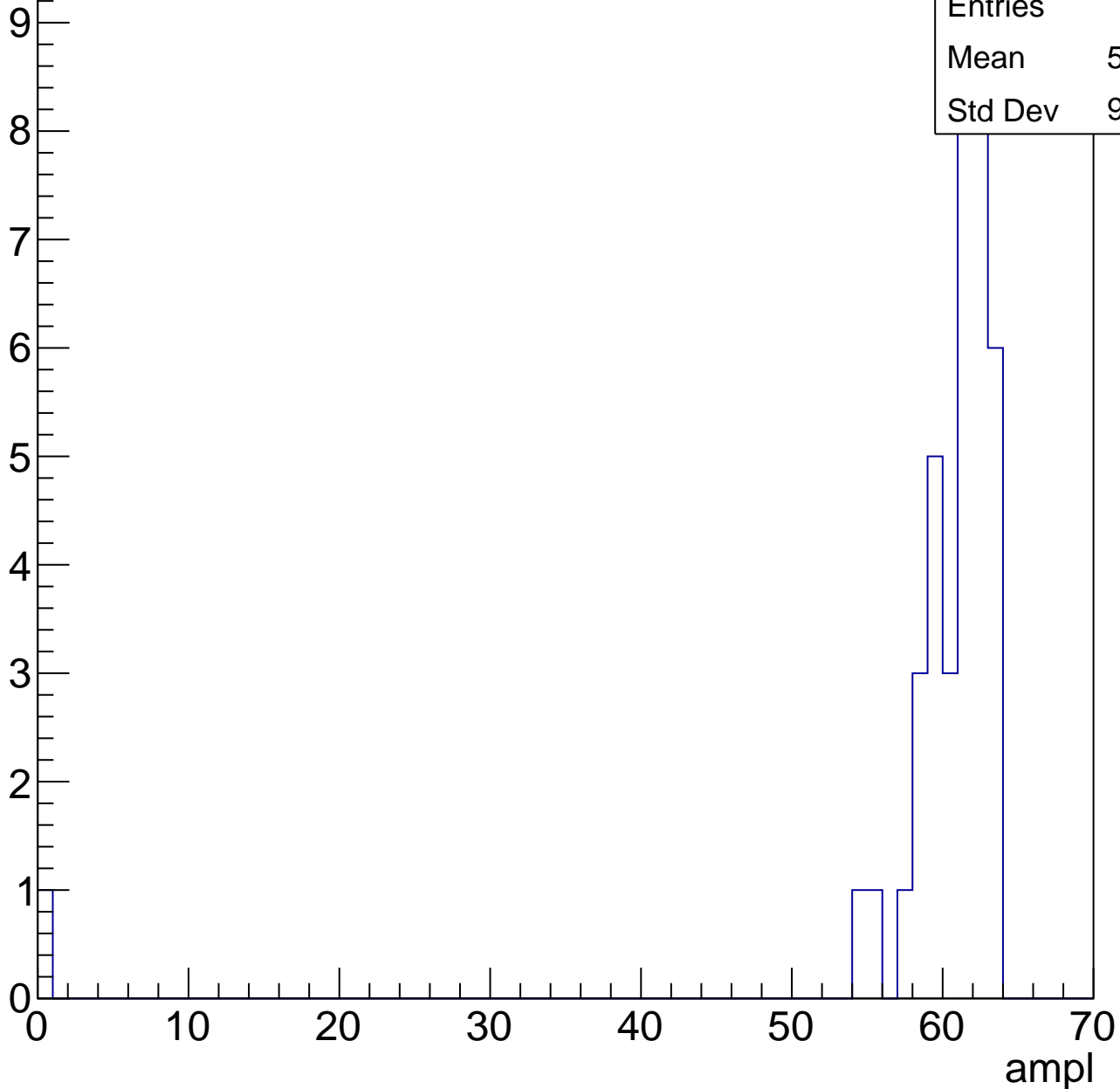


B1L103S, U12-ch121, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	39
Mean	58.97
Std Dev	9.799



B1L103S, U12-ch121, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	4
Mean	62
Std Dev	1.225

ampl

0 10 20 30 40 50 60 70

B1L103S, U12-ch121, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

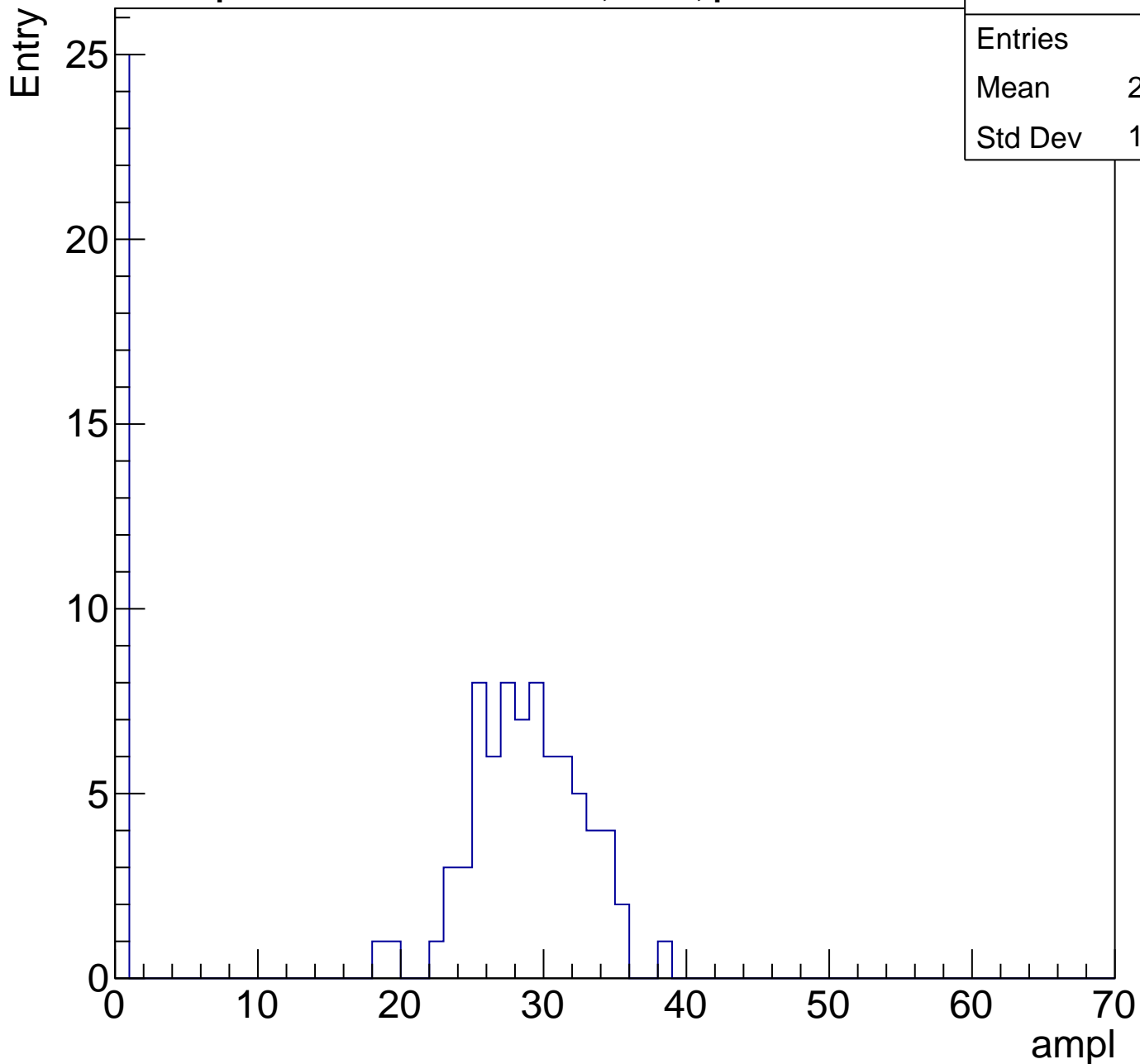
Entries	19
Mean	0
Std Dev	0

ampl

B1L103S, U12-ch122, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	99
Mean	21.23
Std Dev	12.76



B1L103S, U12-ch122, adc1

calib_packv5_041523_1651.root, FC#0, port C2

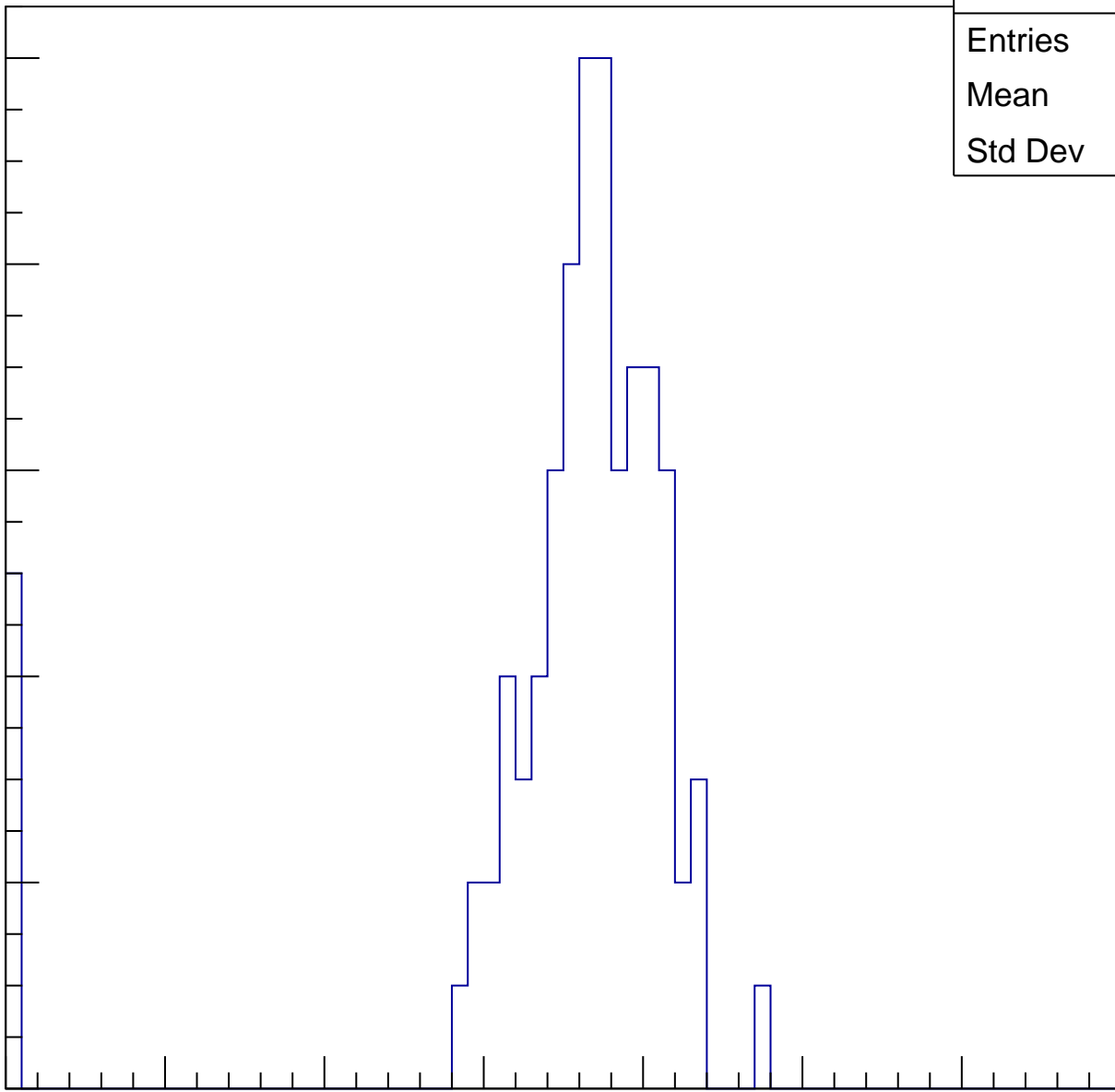
Entries	87
Mean	34.47
Std Dev	9.239

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

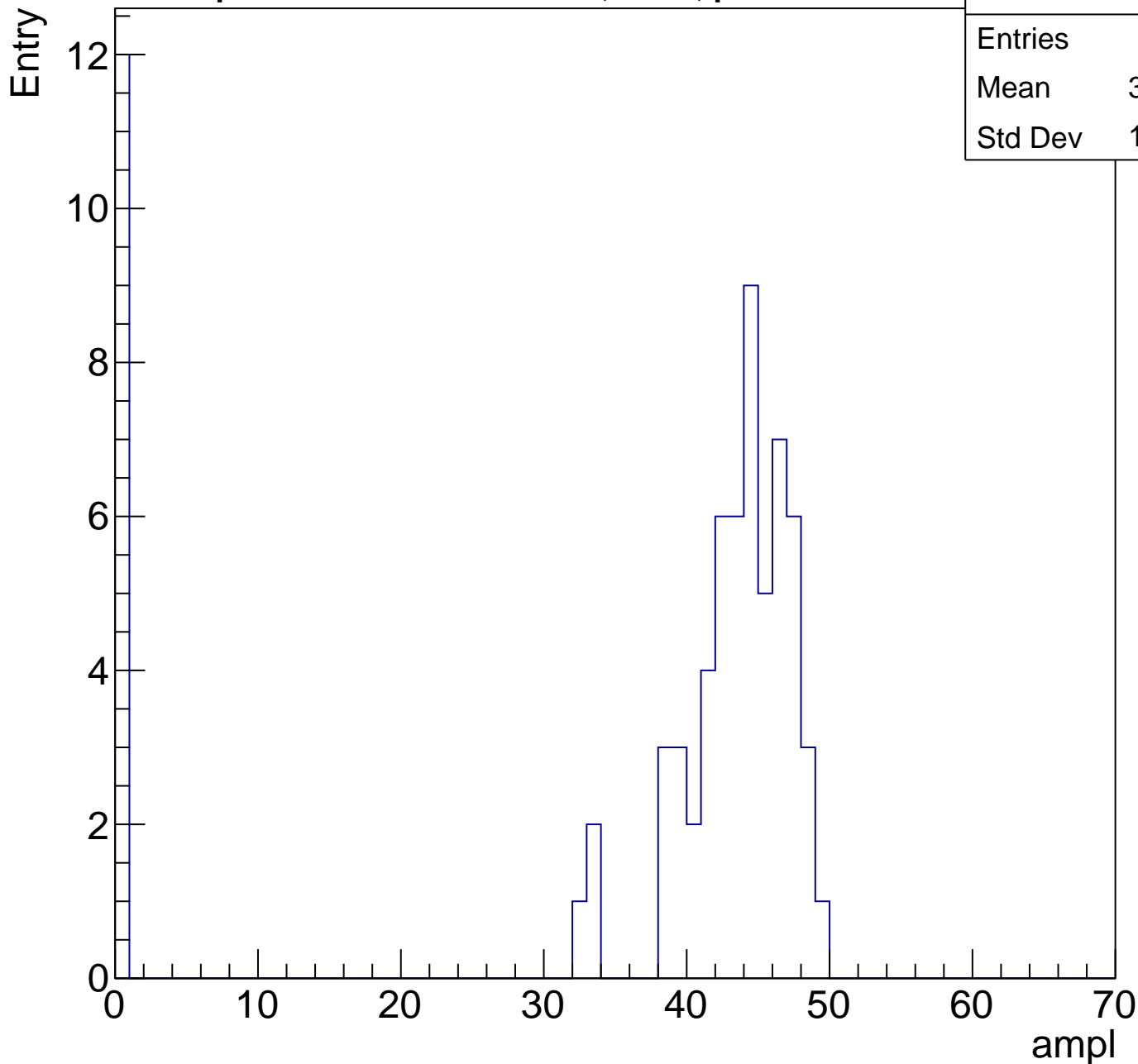
ampl



B1L103S, U12-ch122, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	70
Mean	35.73
Std Dev	16.59

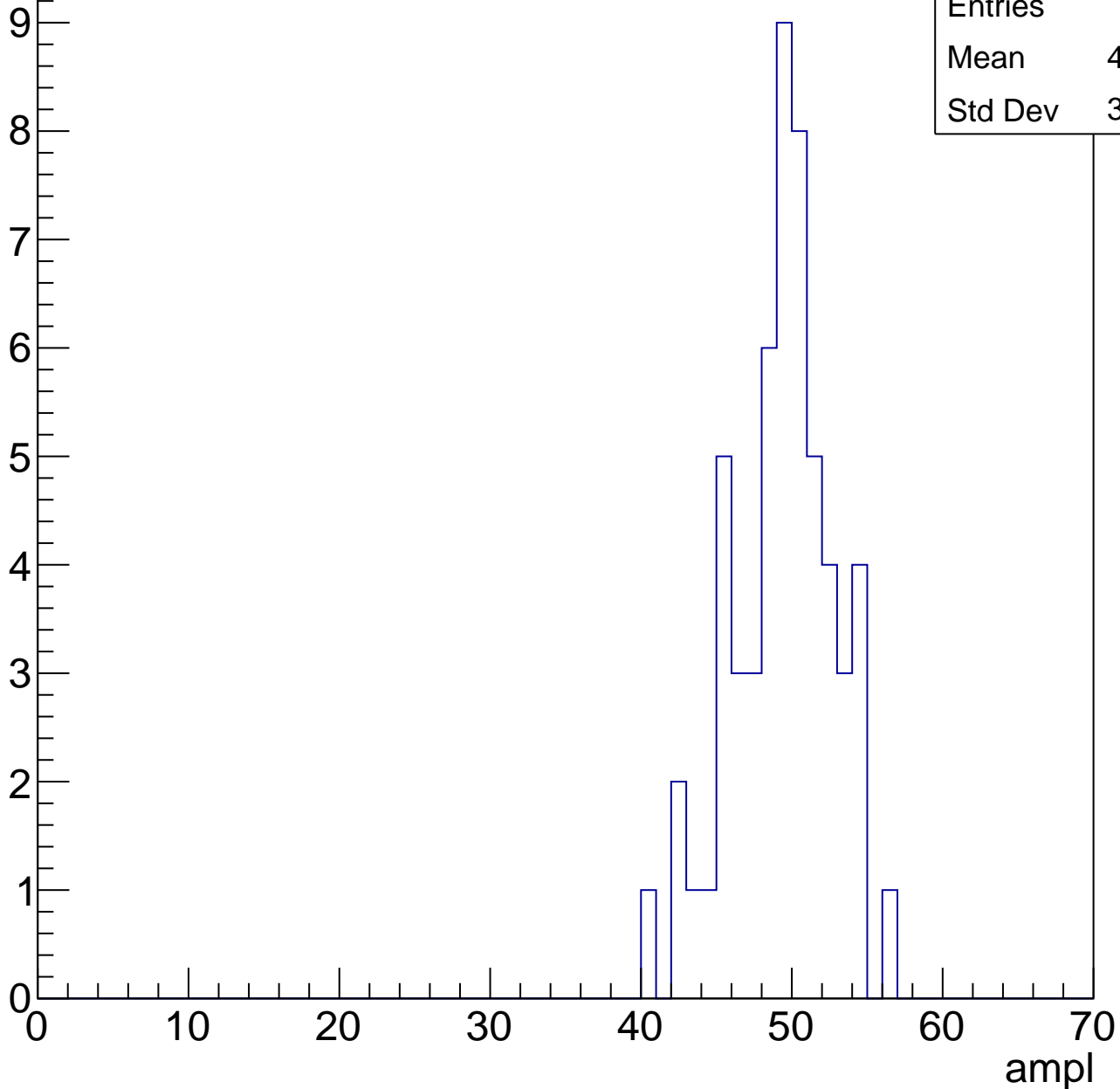


B1L103S, U12-ch122, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	56
Mean	48.89
Std Dev	3.342

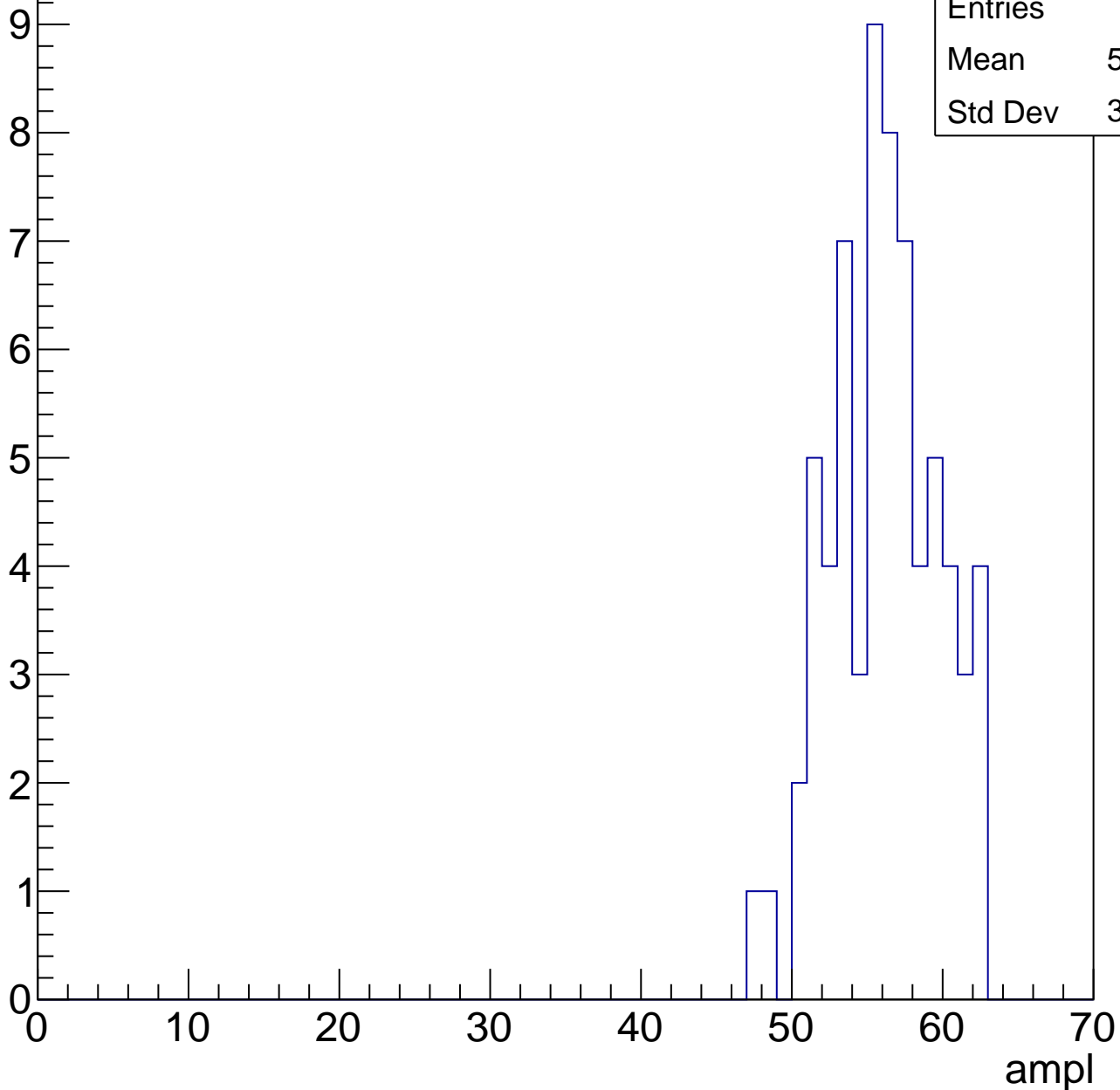


B1L103S, U12-ch122, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	55.69
Std Dev	3.529

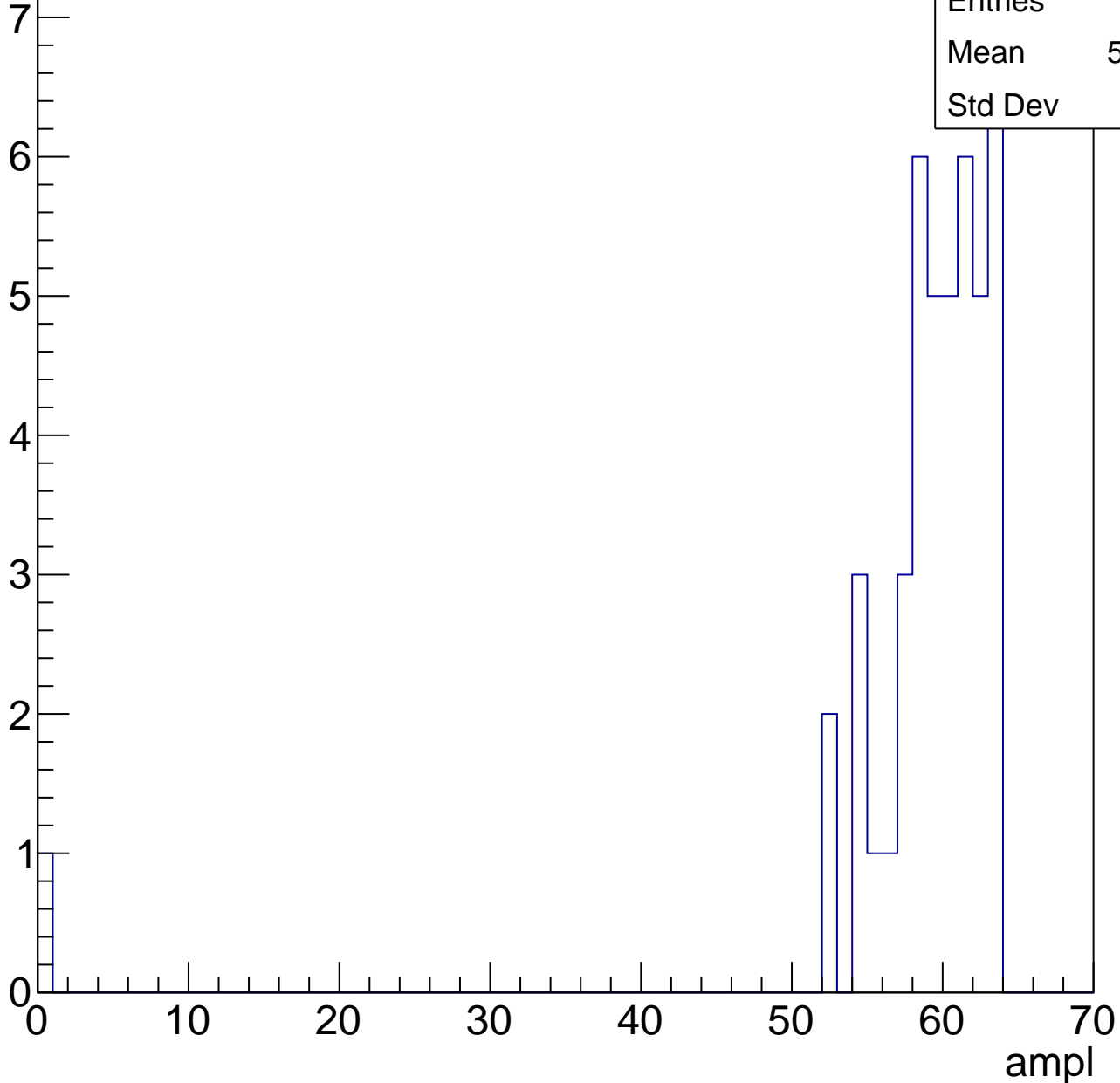


B1L103S, U12-ch122, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

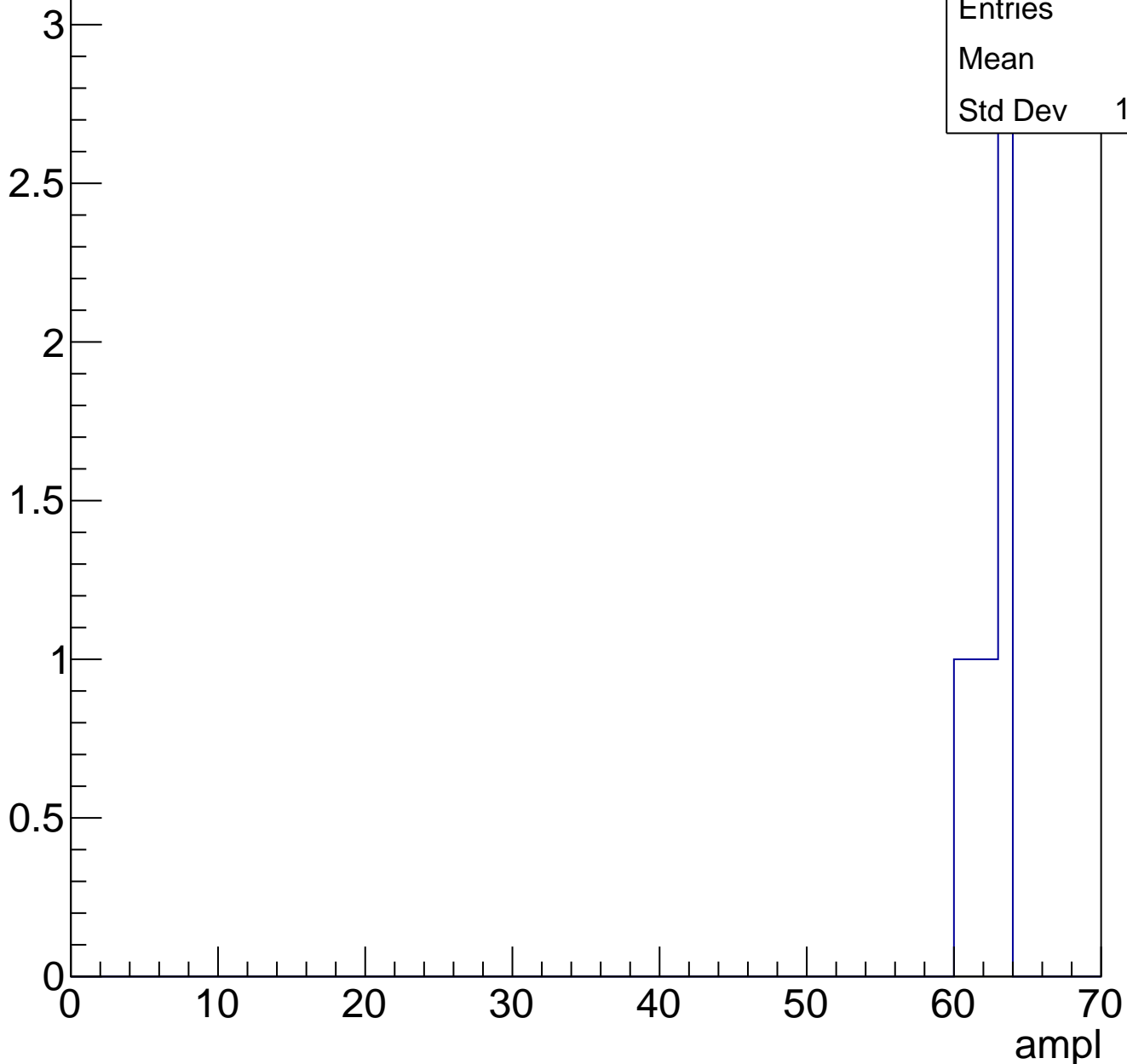
Entries	45
Mean	57.96
Std Dev	9.23



B1L103S, U12-ch122, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch122, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

ampl

B1L103S, U12-ch123, adc0

calib_packv5_041523_1651.root, FC#0, port C2

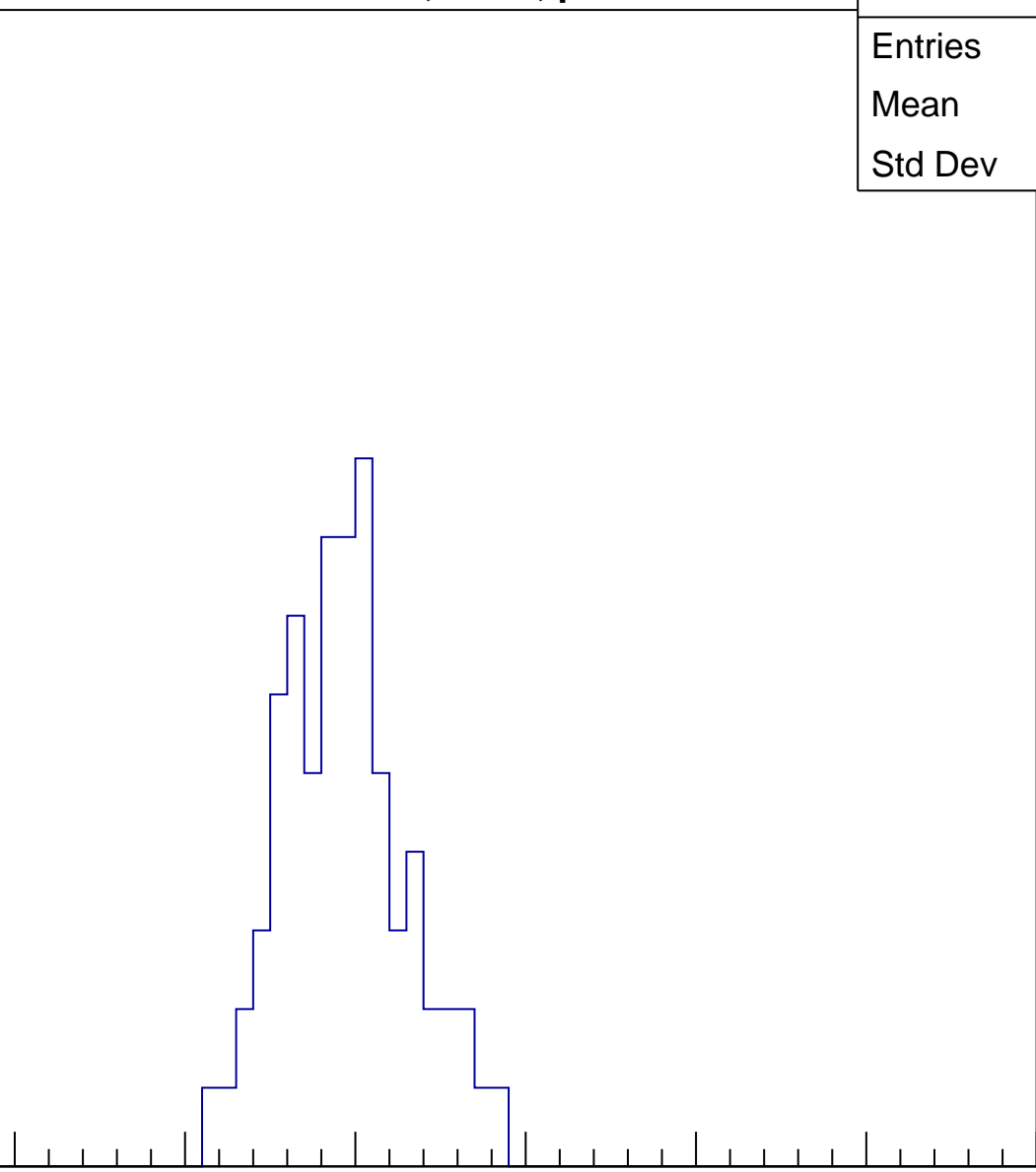
Entries	84
Mean	24.07
Std Dev	11.27

Entry

14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

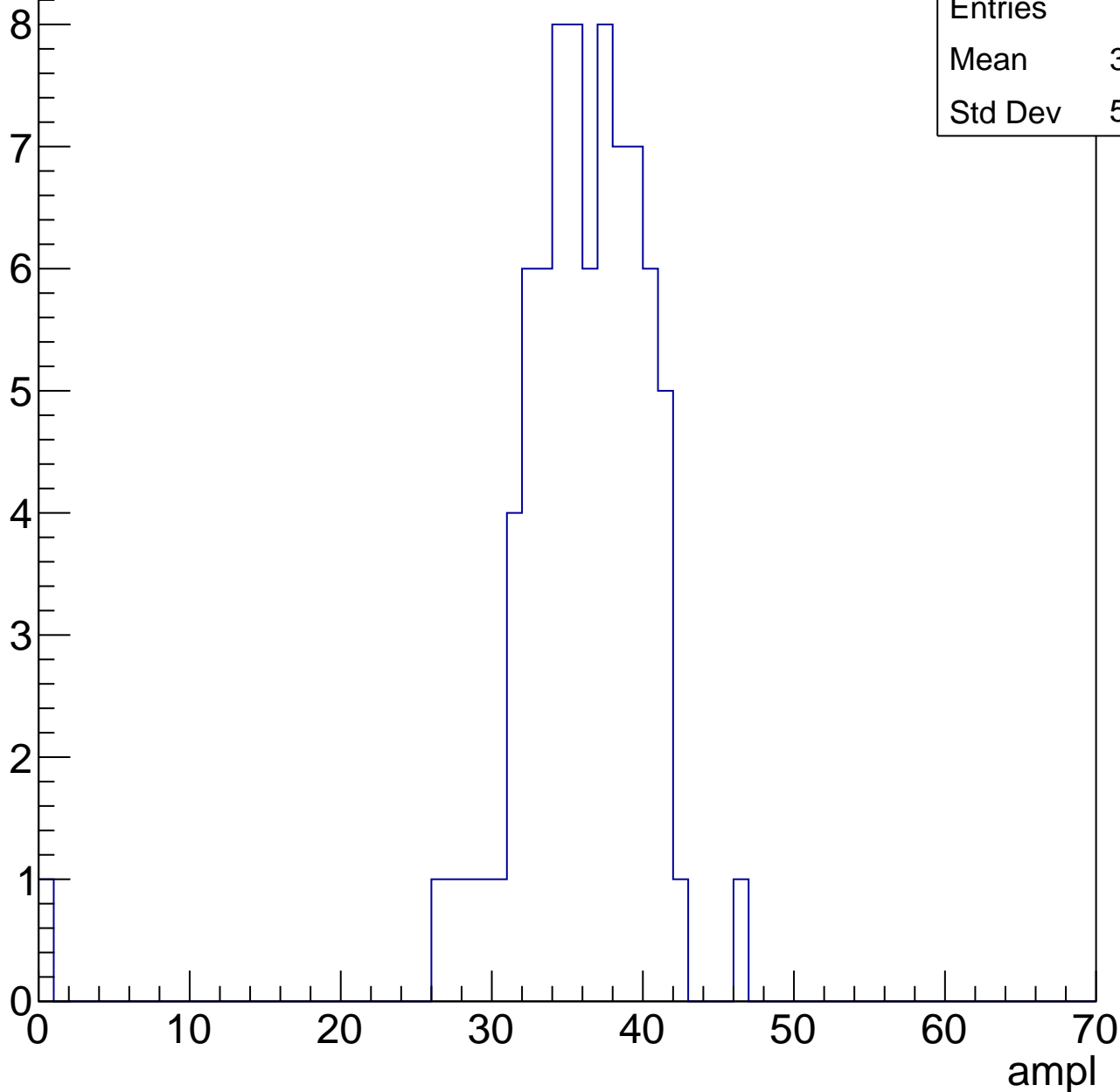


B1L103S, U12-ch123, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	79
Mean	35.32
Std Dev	5.437

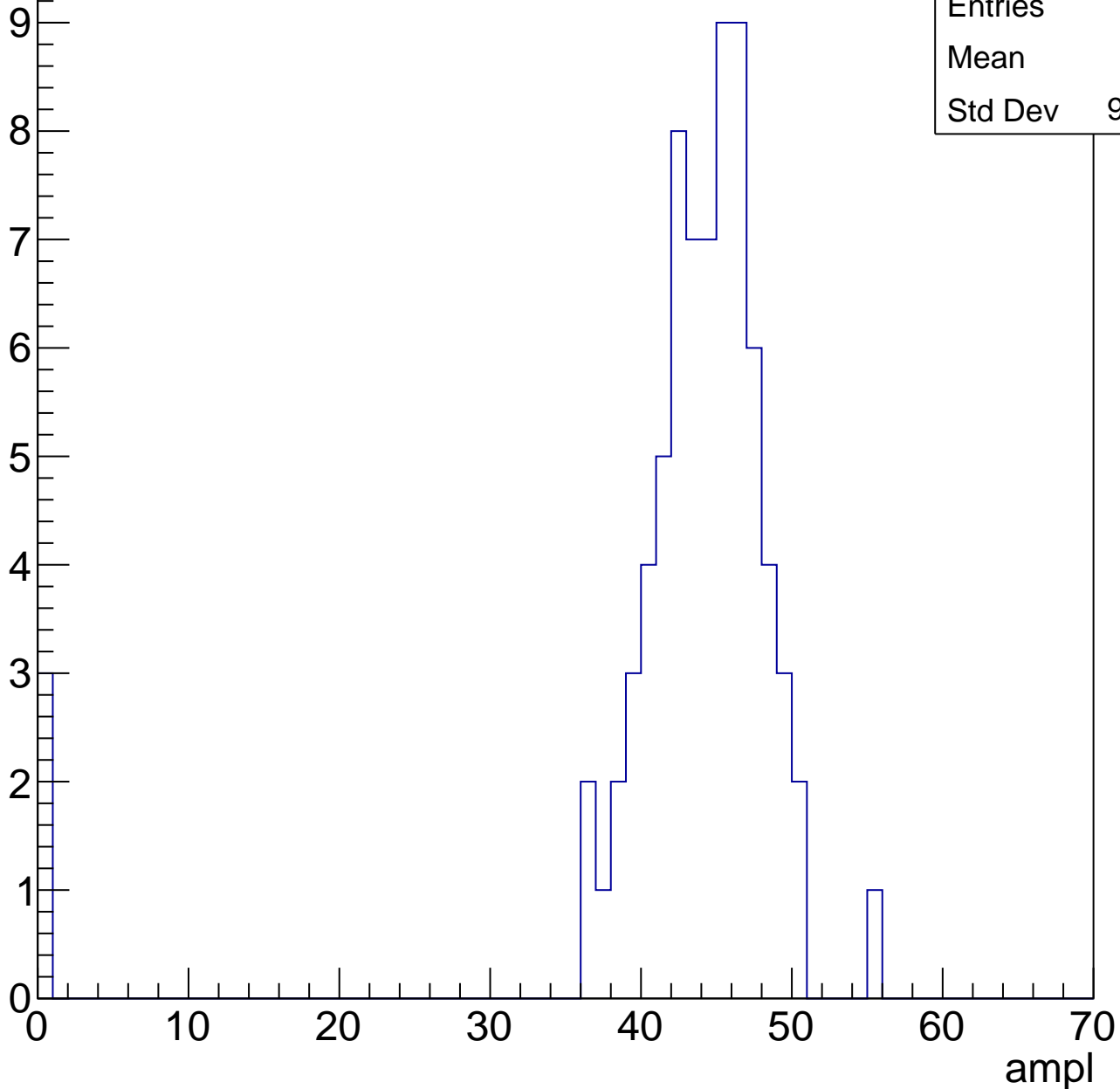


B1L103S, U12-ch123, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	76
Mean	42.2
Std Dev	9.222



B1L103S, U12-ch123, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	66
Mean	41.42
Std Dev	18.78

Entry

10

8

6

4

2

0

0

10

20

30

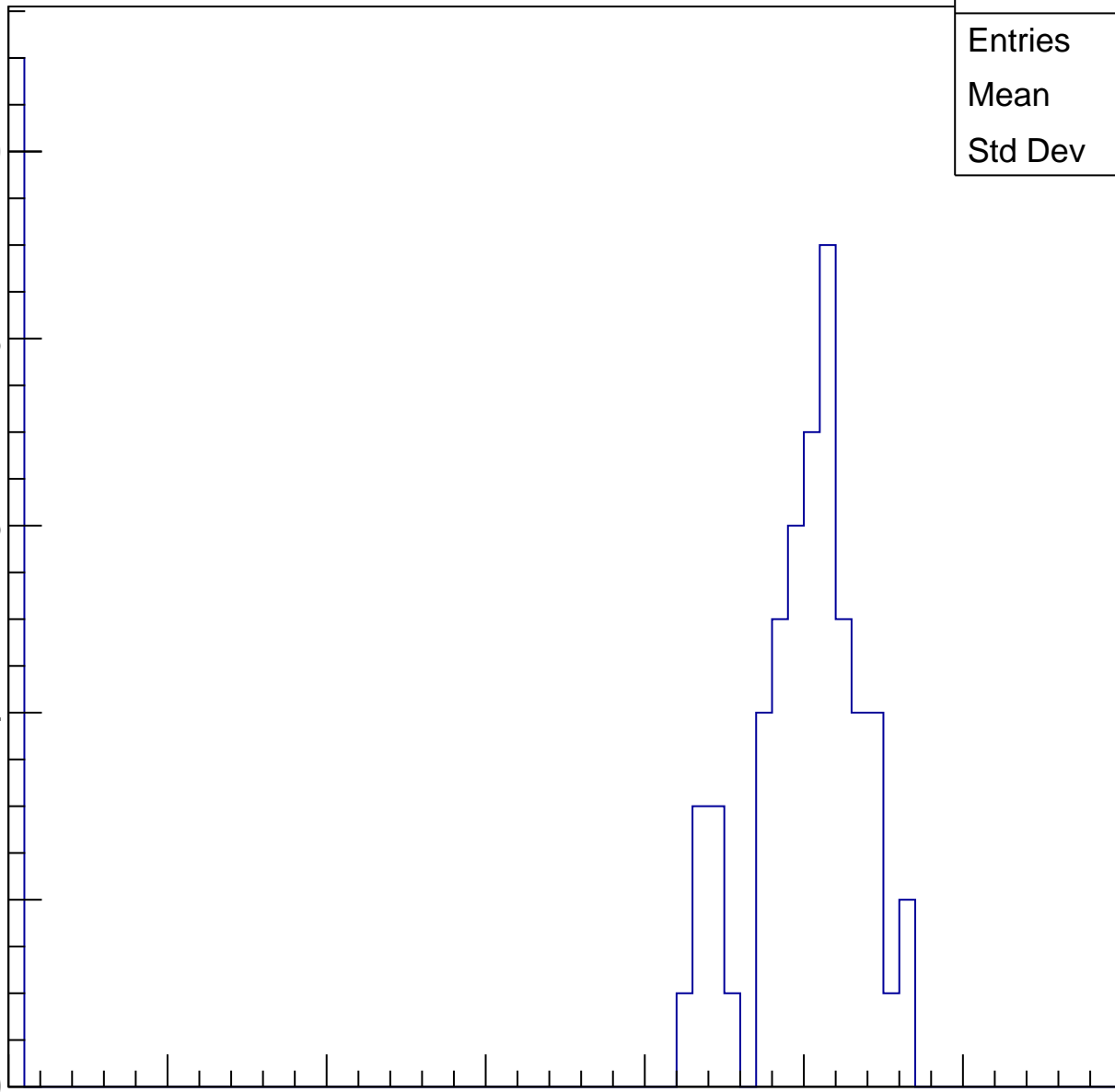
40

50

60

70

ampl

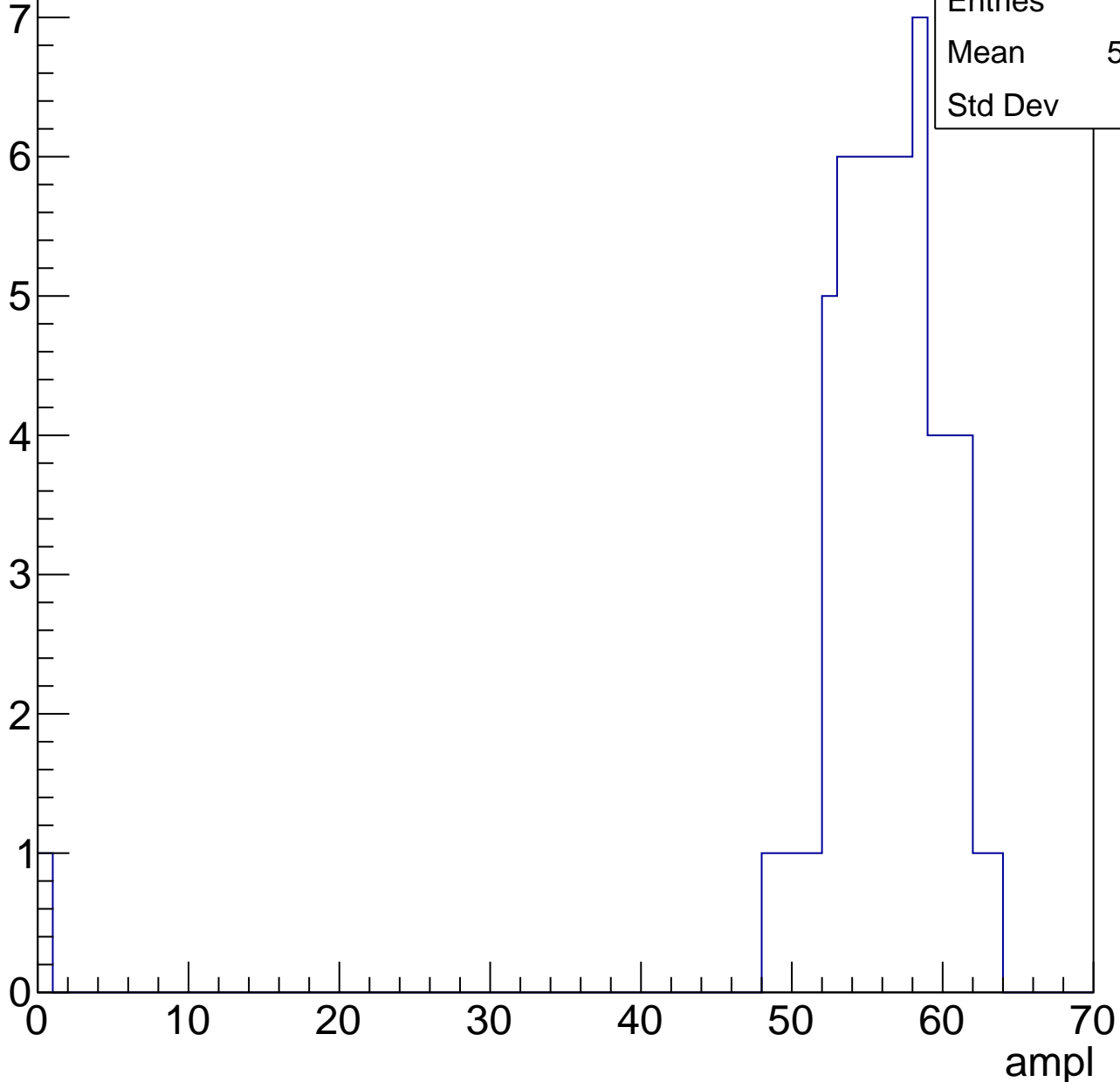


B1L103S, U12-ch123, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	55.07
Std Dev	7.83

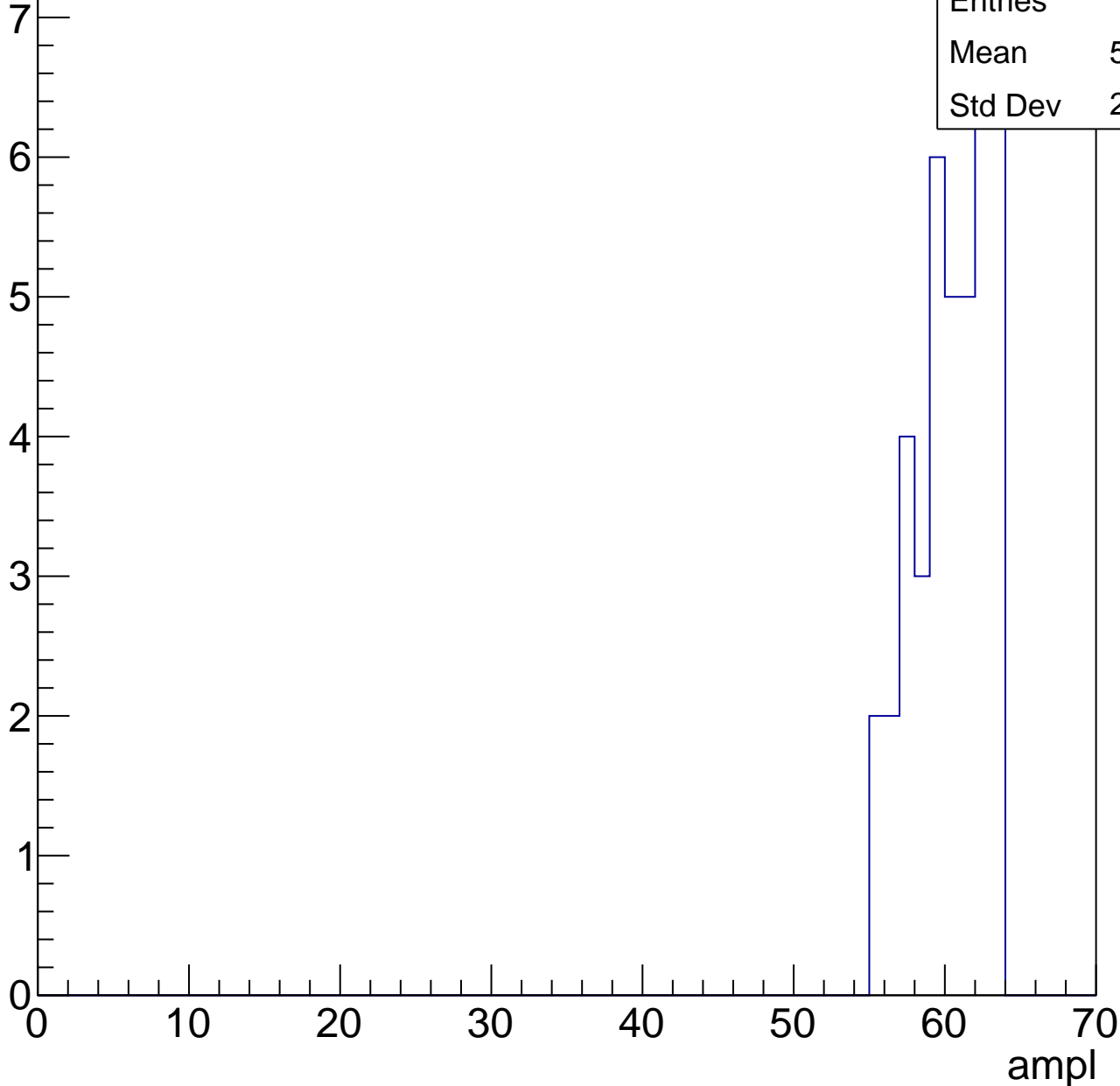


B1L103S, U12-ch123, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	41
Mean	59.95
Std Dev	2.378



B1L103S, U12-ch123, adc6

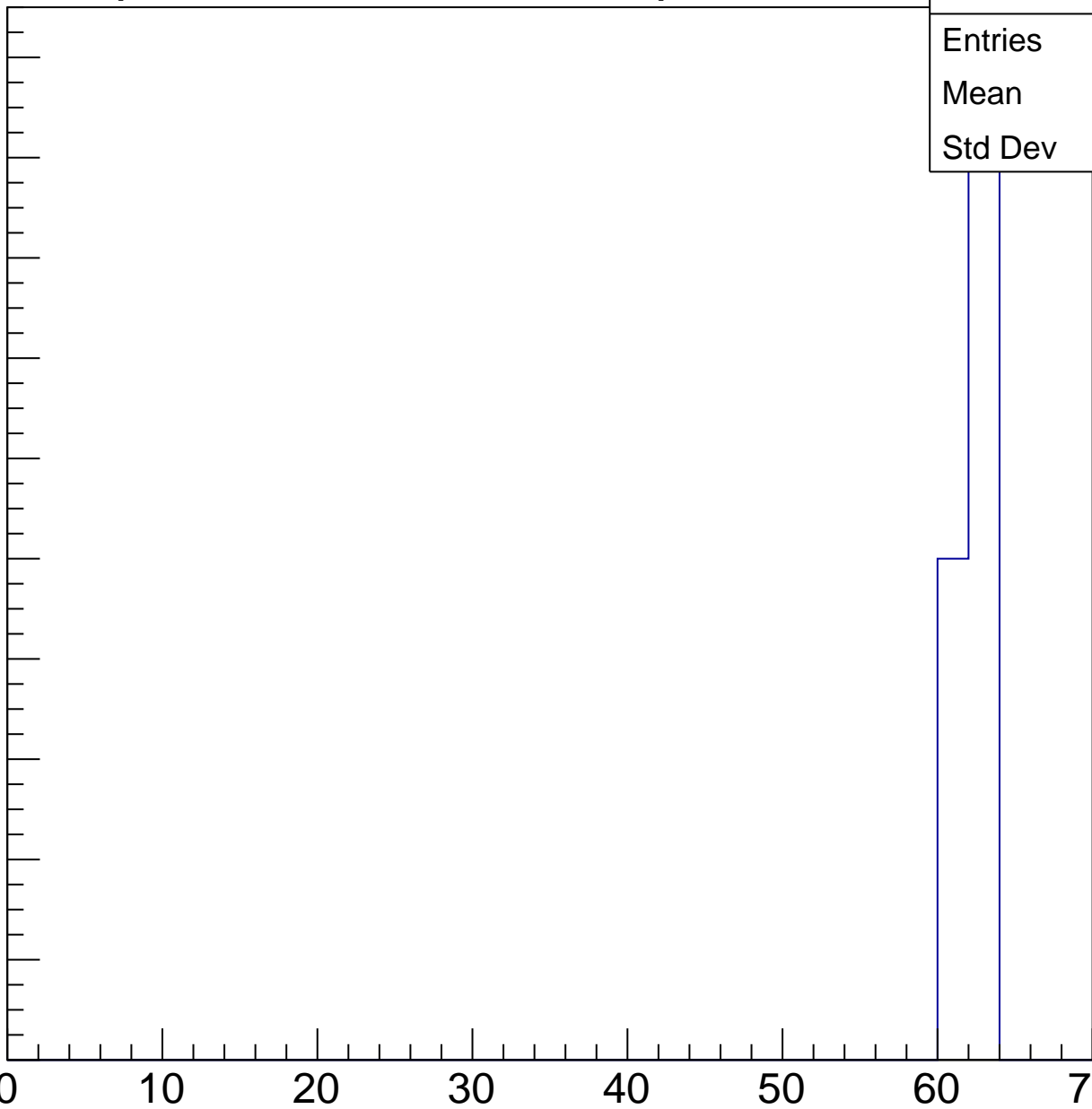
calib_packv5_041523_1651.root, FC#0, port C2

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	6
Mean	61.83
Std Dev	1.067

ampl

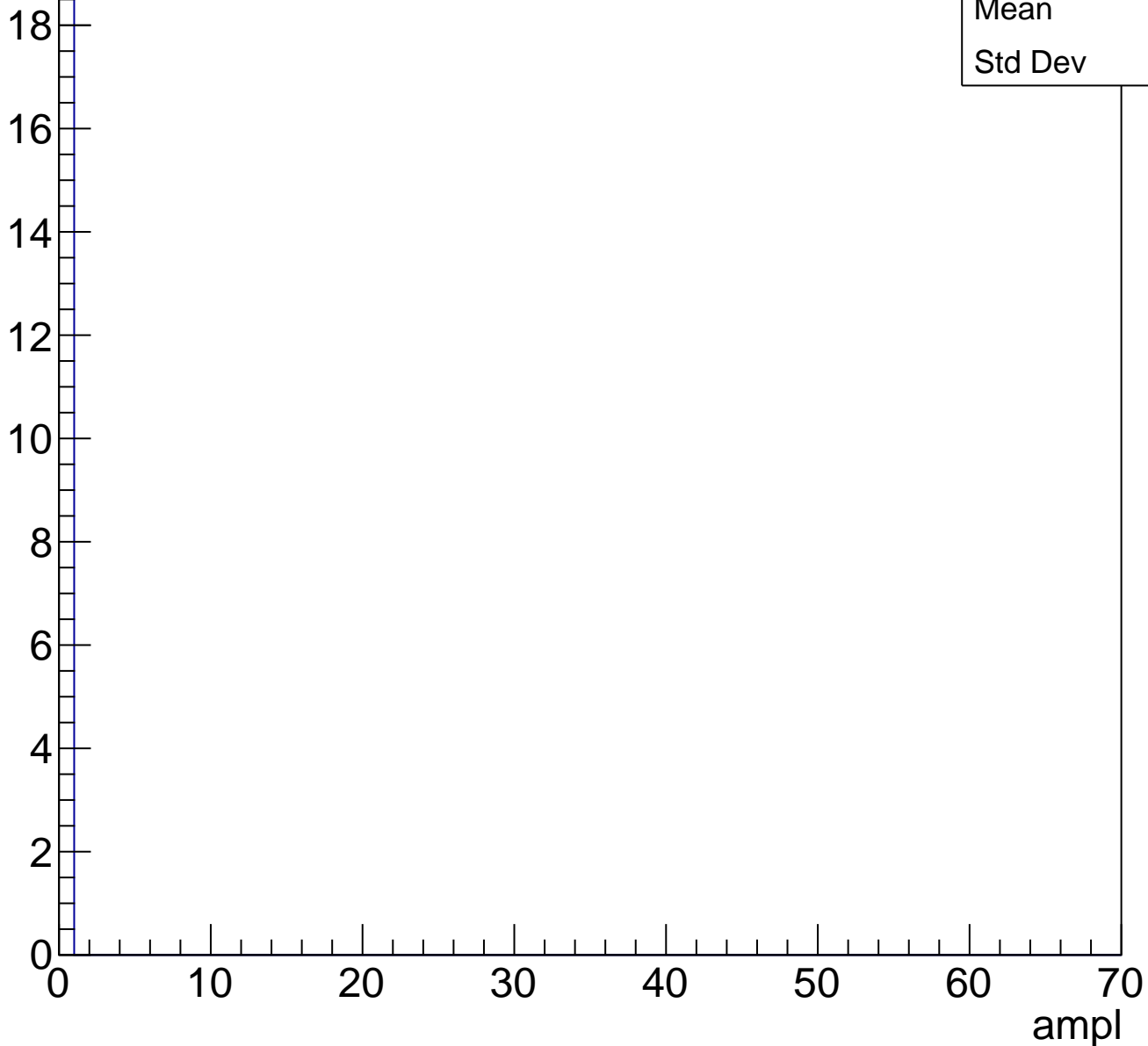


B1L103S, U12-ch123, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	0
Std Dev	0

Entry

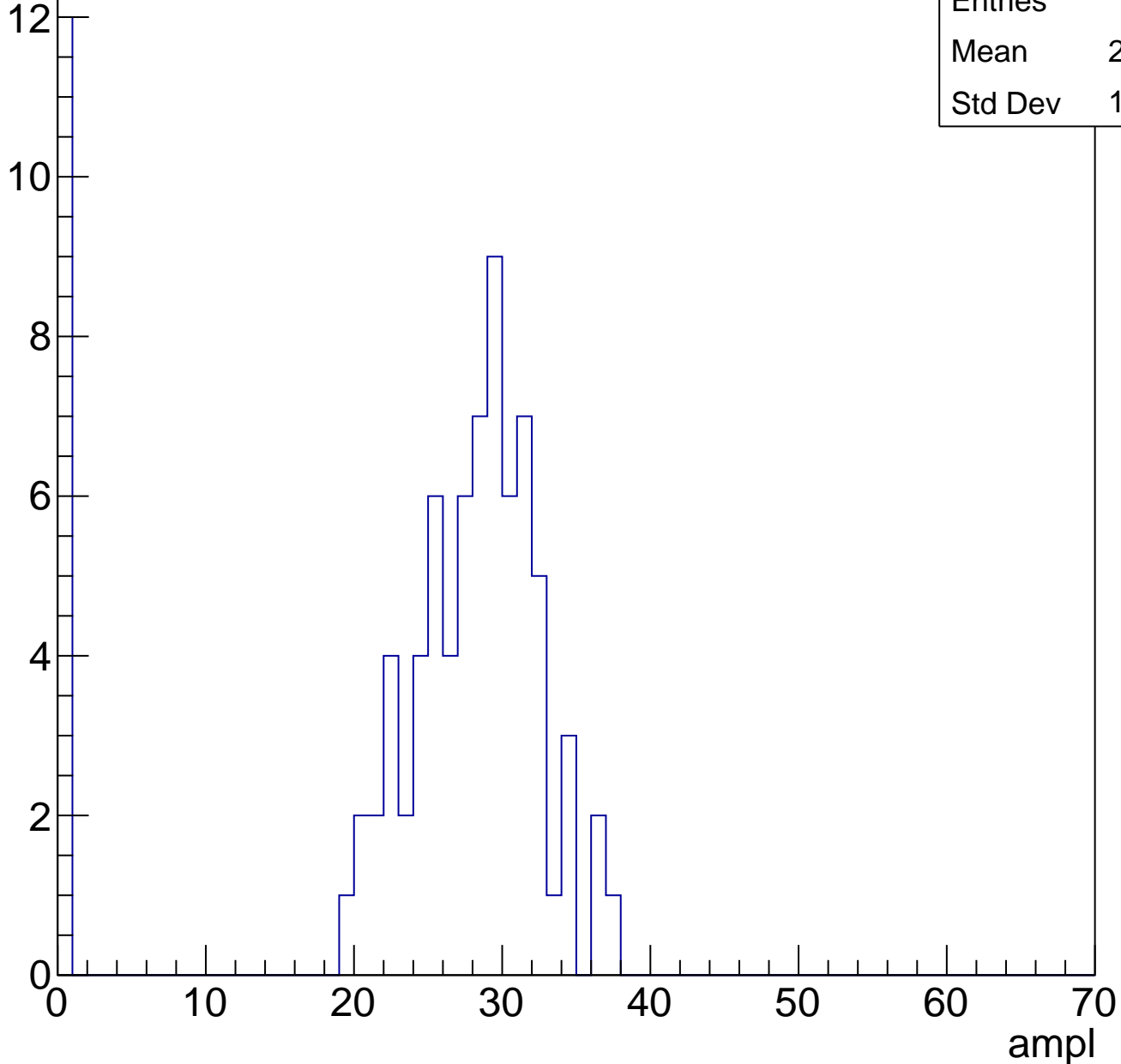


B1L103S, U12-ch124, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	84
Mean	23.87
Std Dev	10.43

Entry

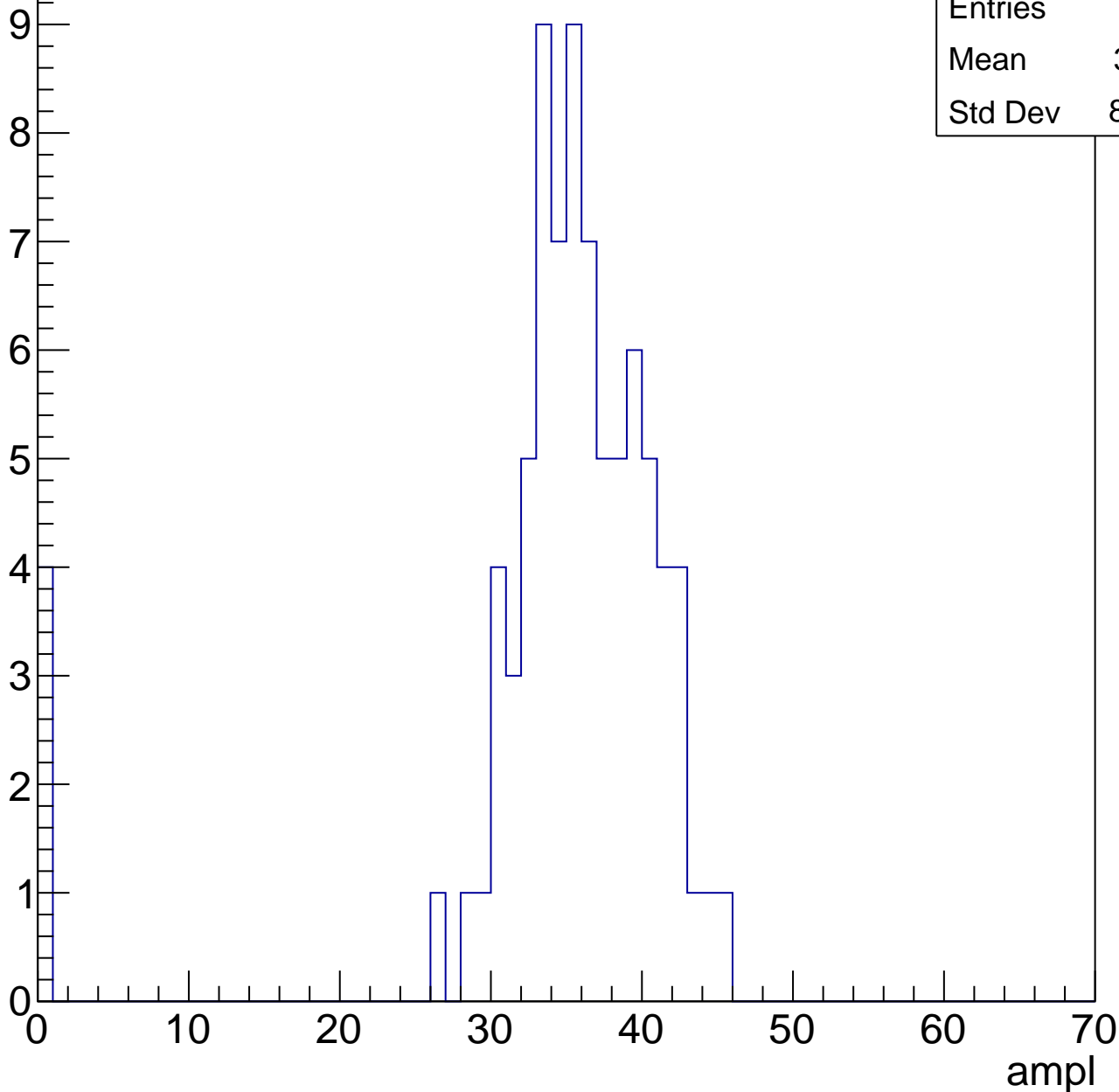


B1L103S, U12-ch124, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	83
Mean	34.11
Std Dev	8.583

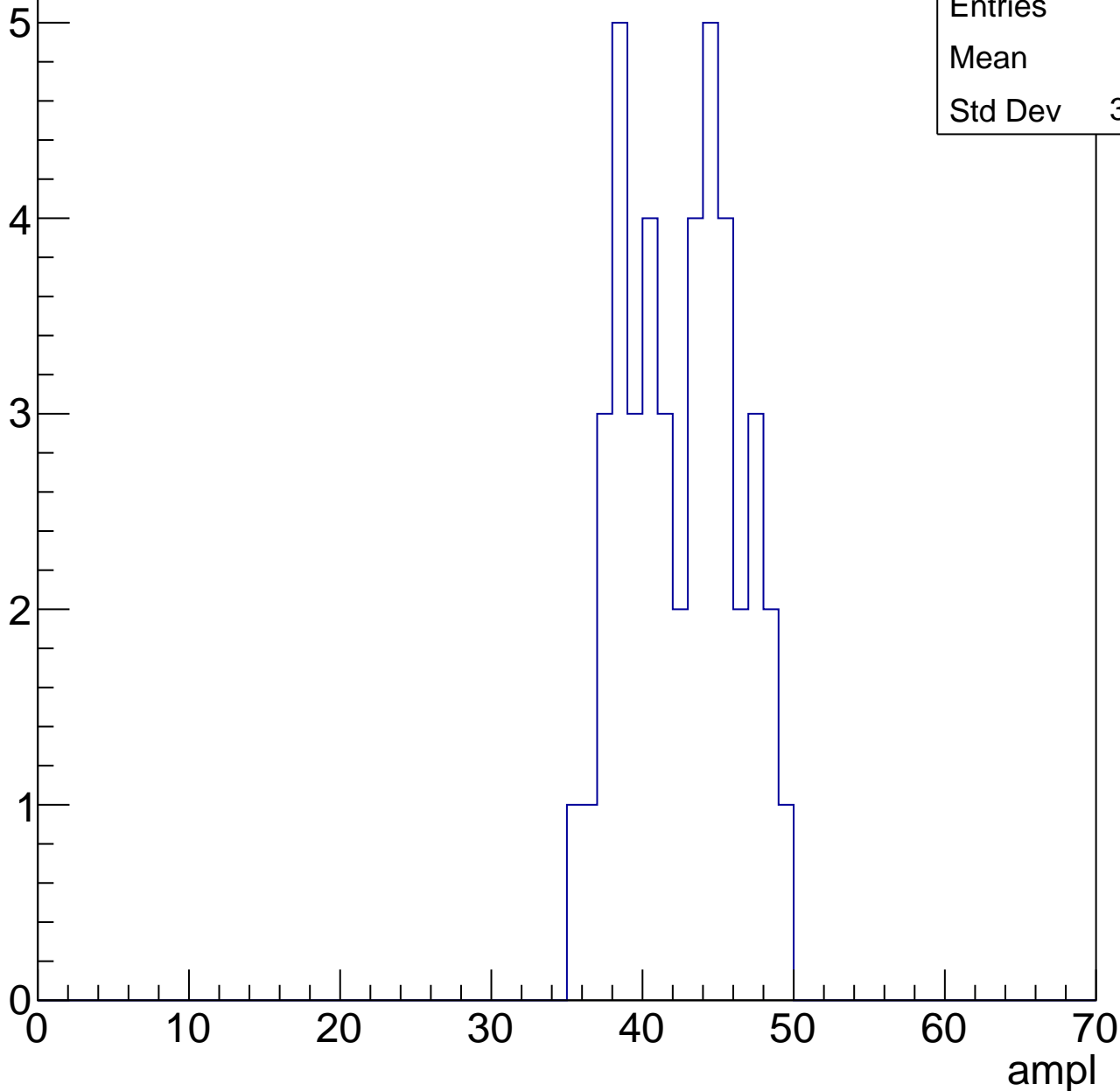


B1L103S, U12-ch124, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	43
Mean	42
Std Dev	3.654

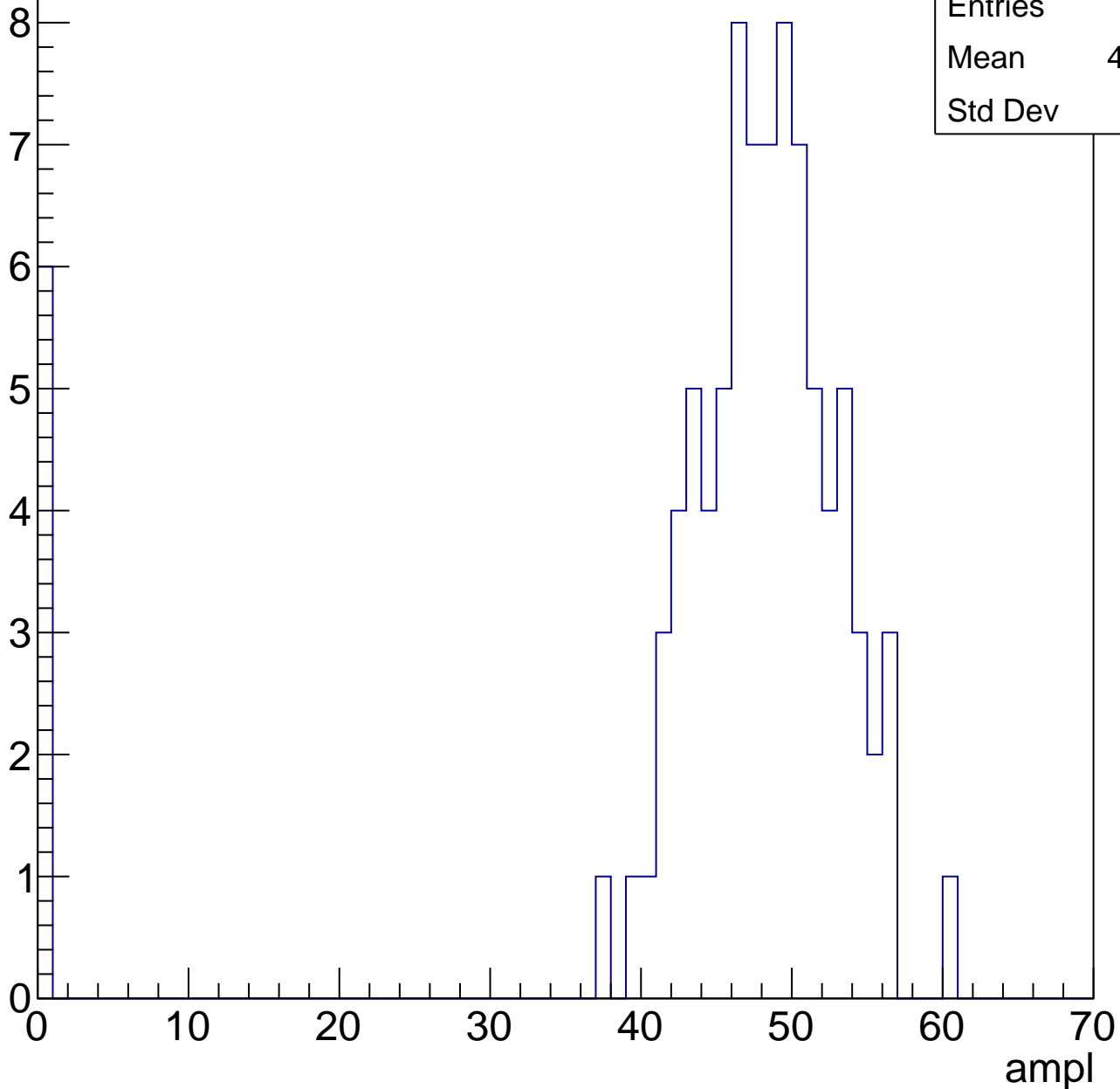


B1L103S, U12-ch124, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	90
Mean	44.73
Std Dev	12.7

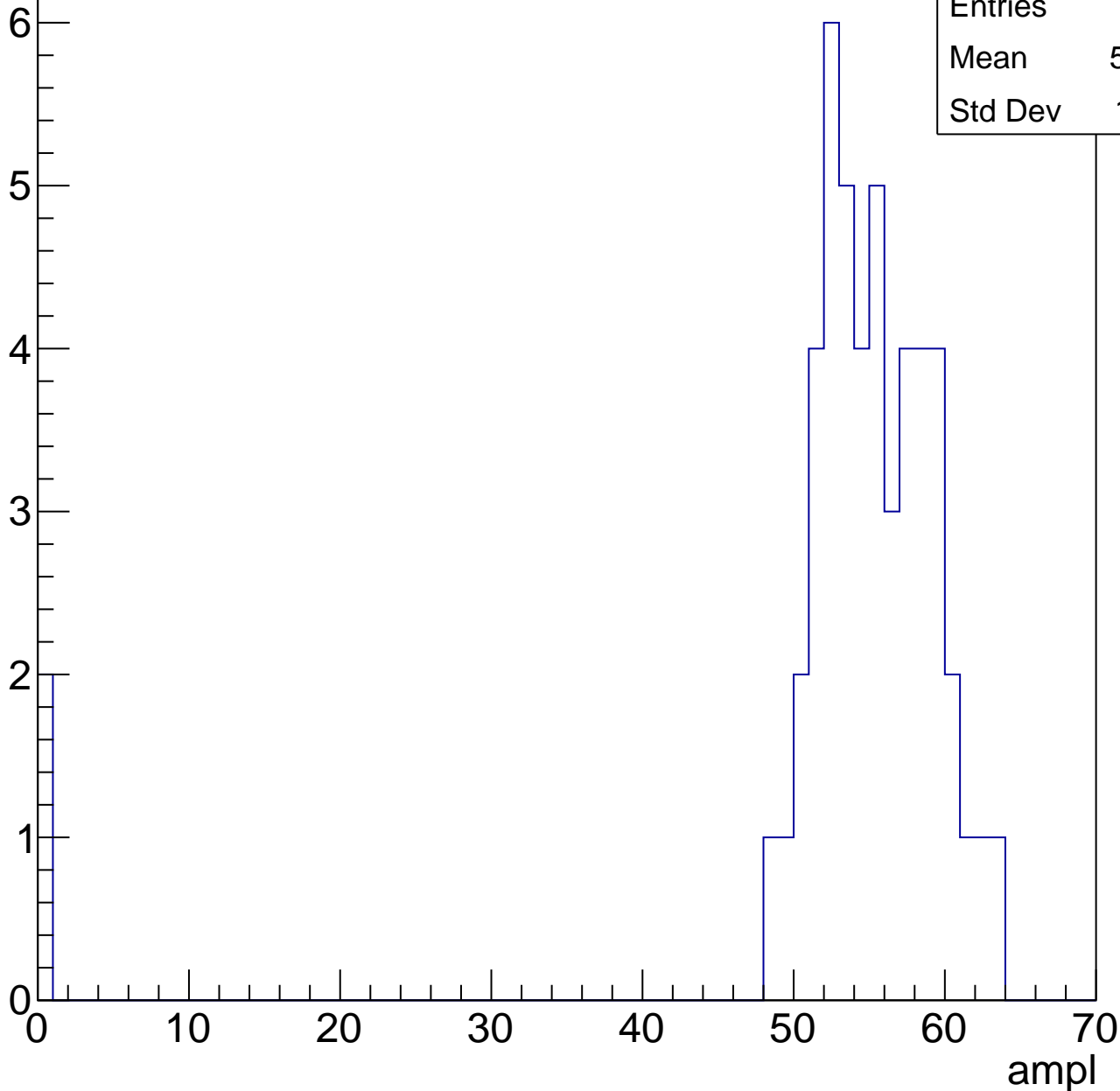


B1L103S, U12-ch124, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	50
Mean	52.78
Std Dev	11.31

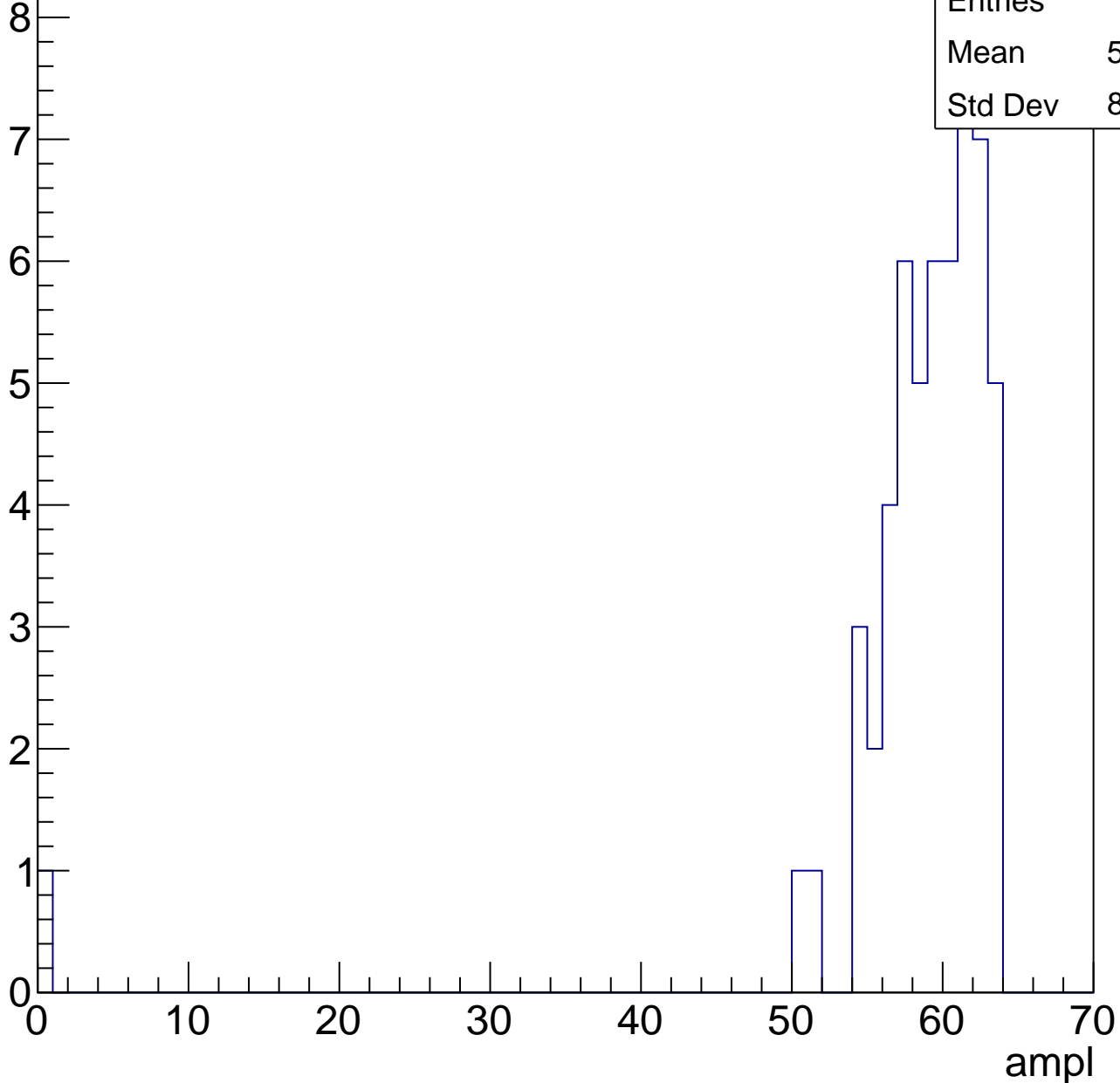


B1L103S, U12-ch124, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

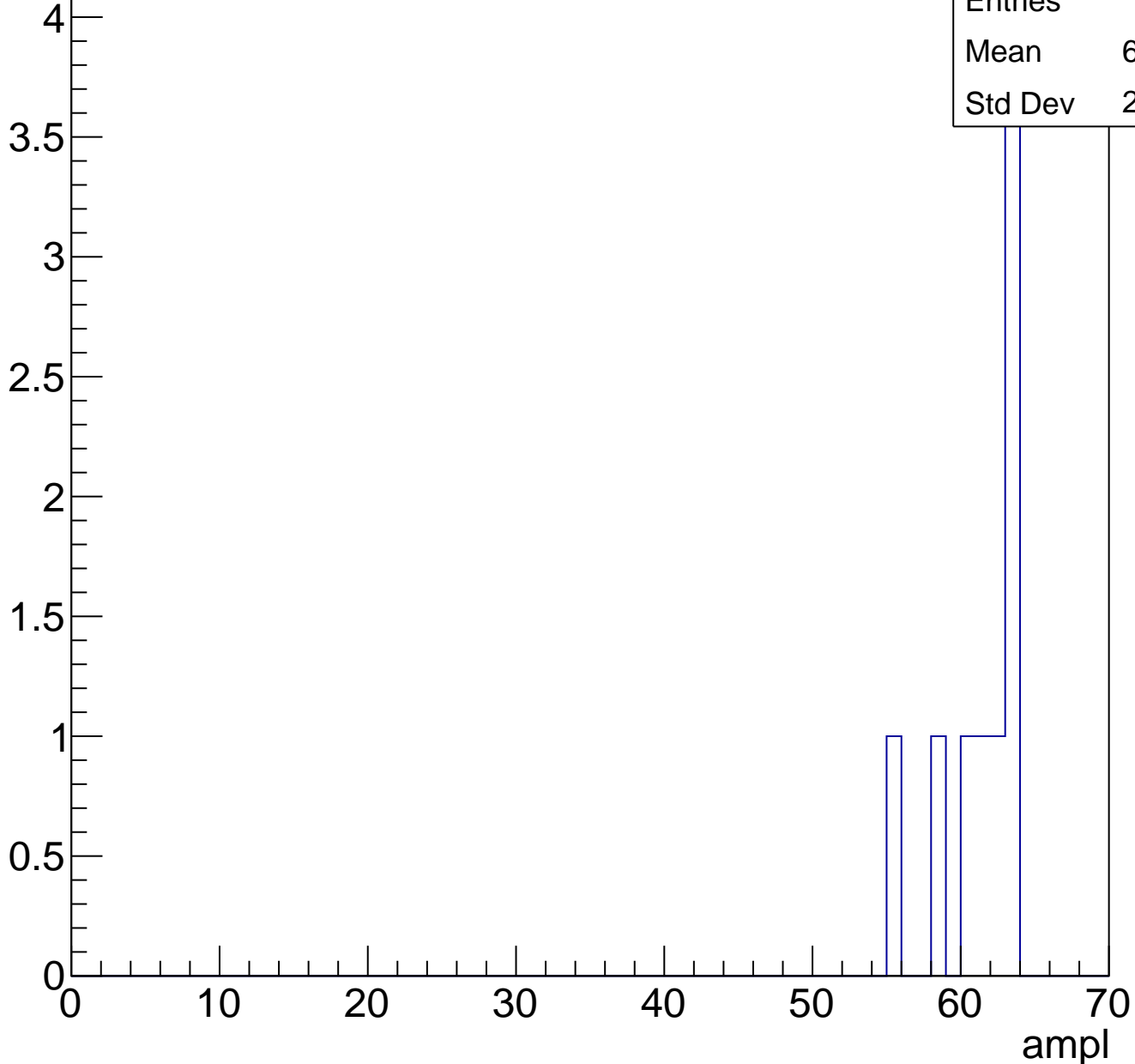
Entries	55
Mean	57.82
Std Dev	8.423



B1L103S, U12-ch124, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	9
Mean	60.89
Std Dev	2.643

B1L103S, U12-ch124, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.1
Std Dev	13.51

Entry



B1L103S, U12-ch125, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	90
Mean	25.98
Std Dev	11.2

Entry

12

10

8

6

4

2

0

0

10

20

30

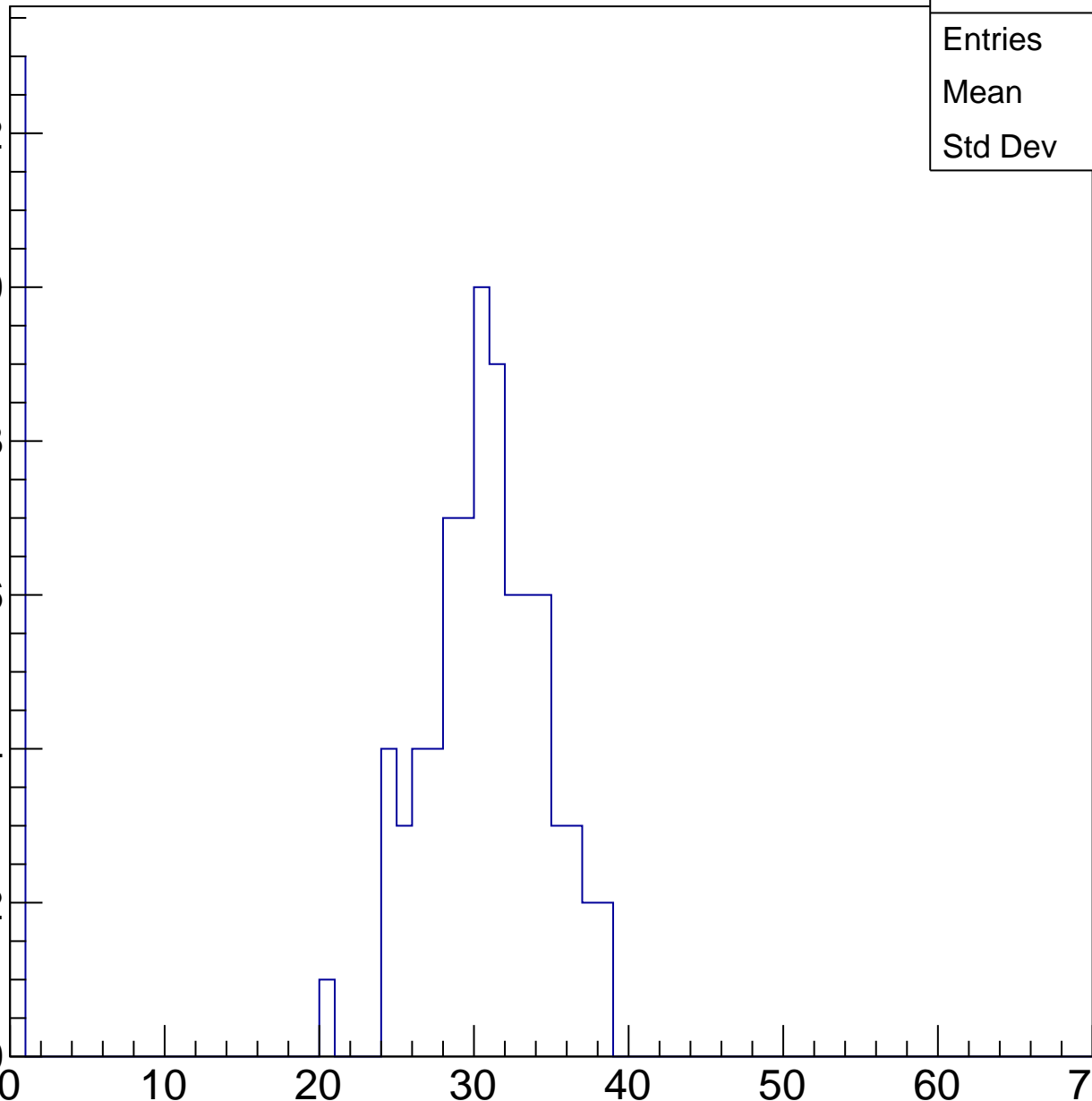
40

50

60

70

ampl



B1L103S, U12-ch125, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	79
Mean	32.43
Std Dev	13.43

Entry

10

8

6

4

2

0

0

10

20

30

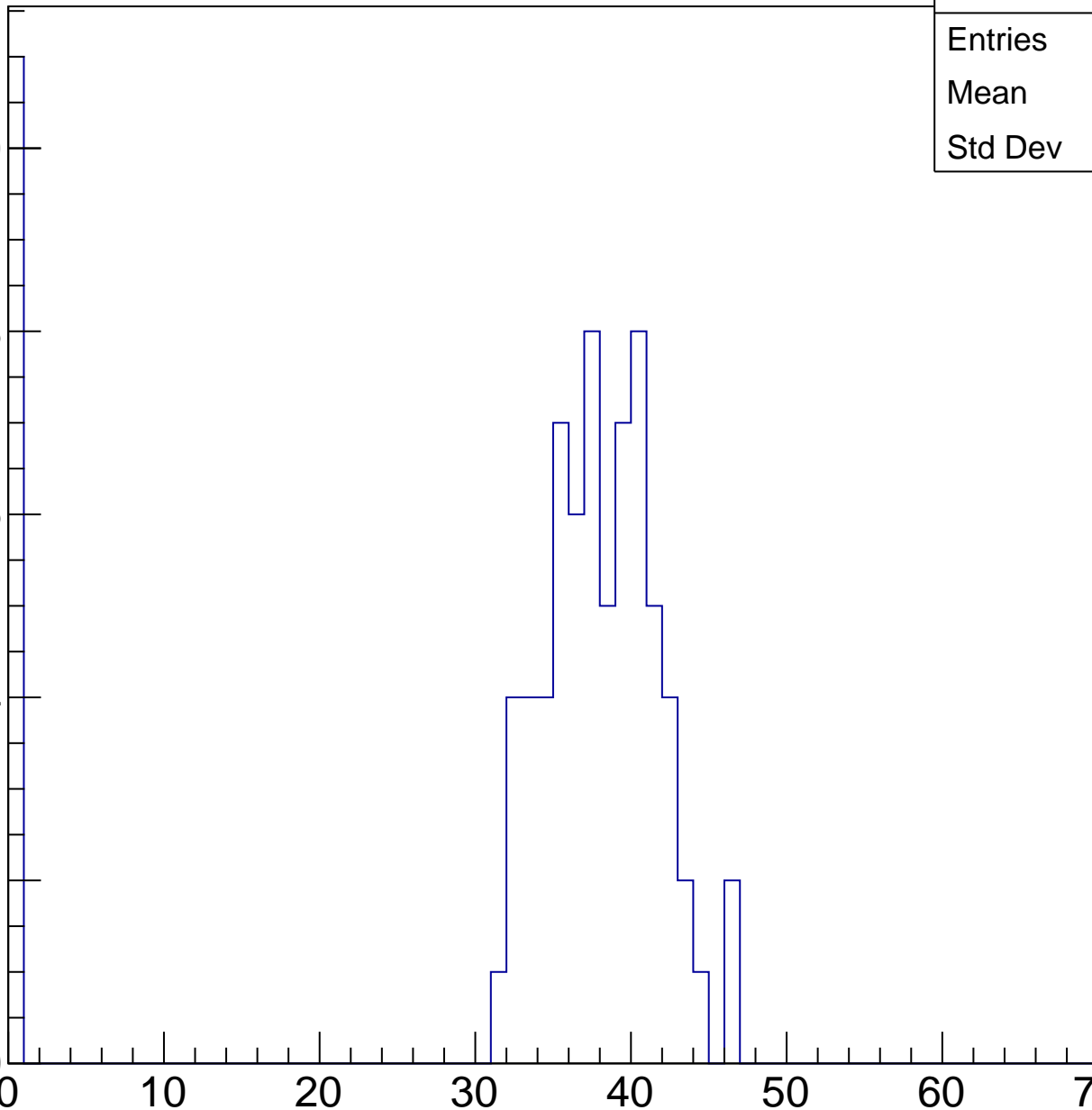
40

50

60

70

ampl

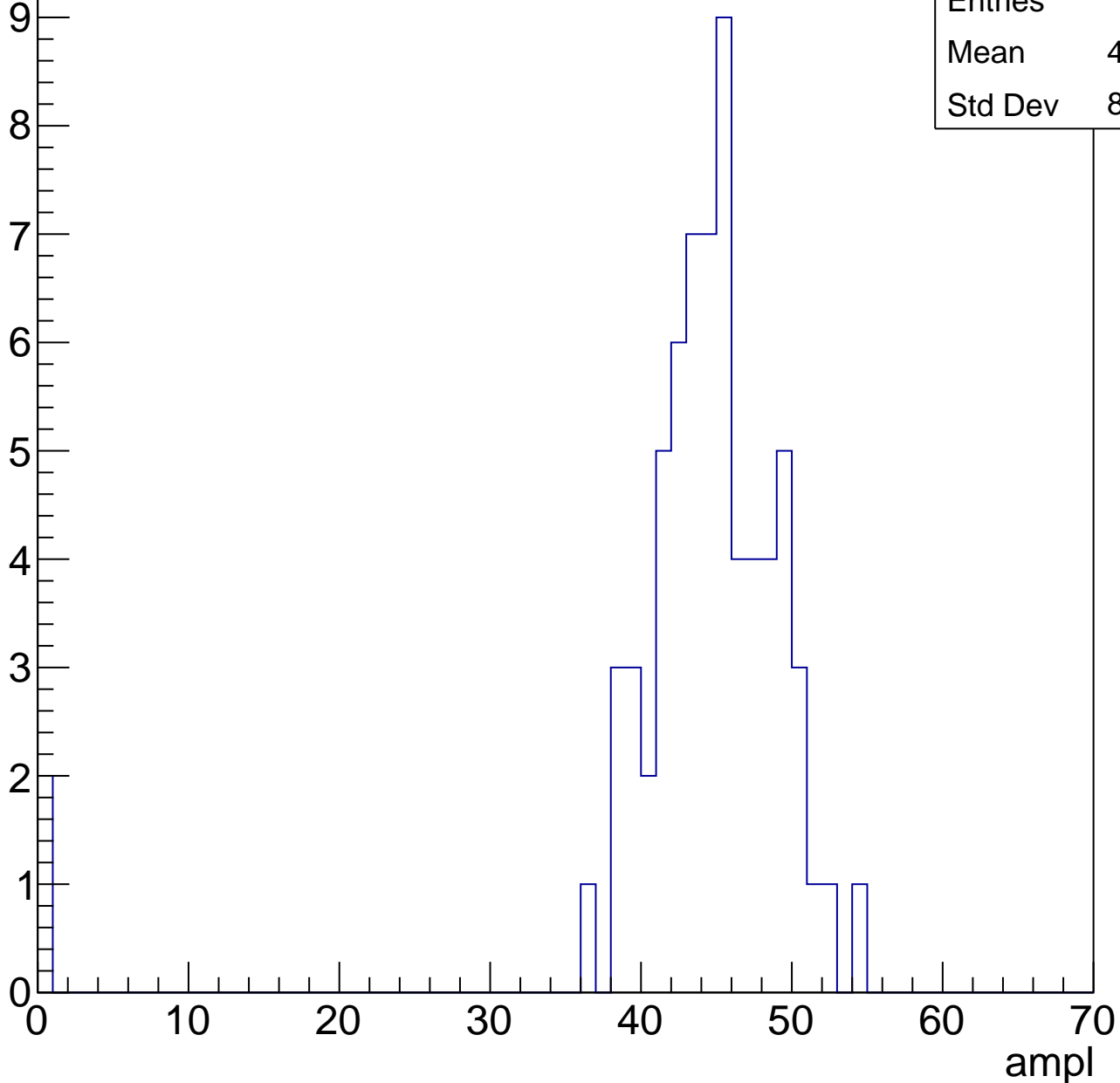


B1L103S, U12-ch125, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	43.15
Std Dev	8.357

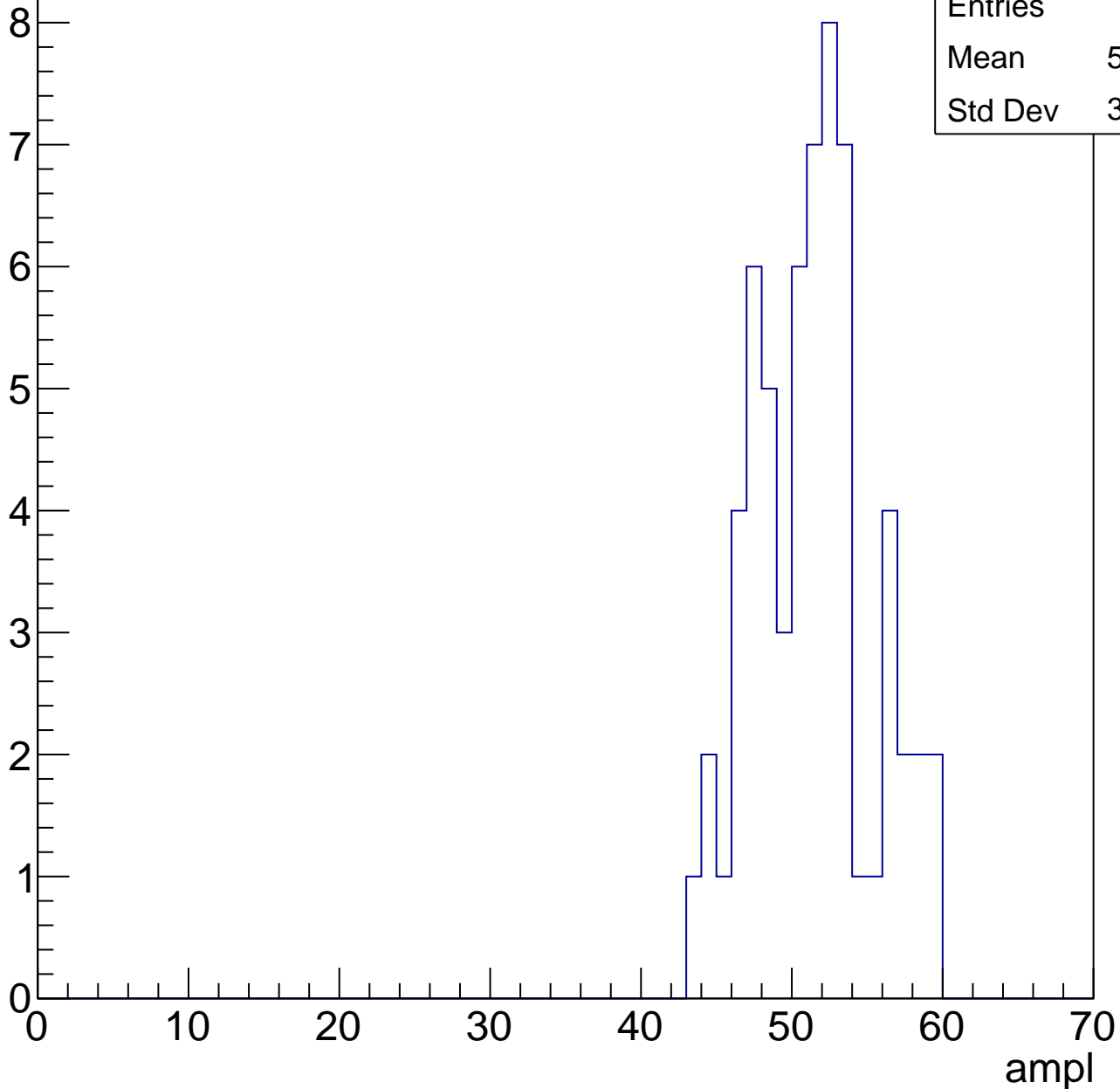


B1L103S, U12-ch125, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	50.87
Std Dev	3.842

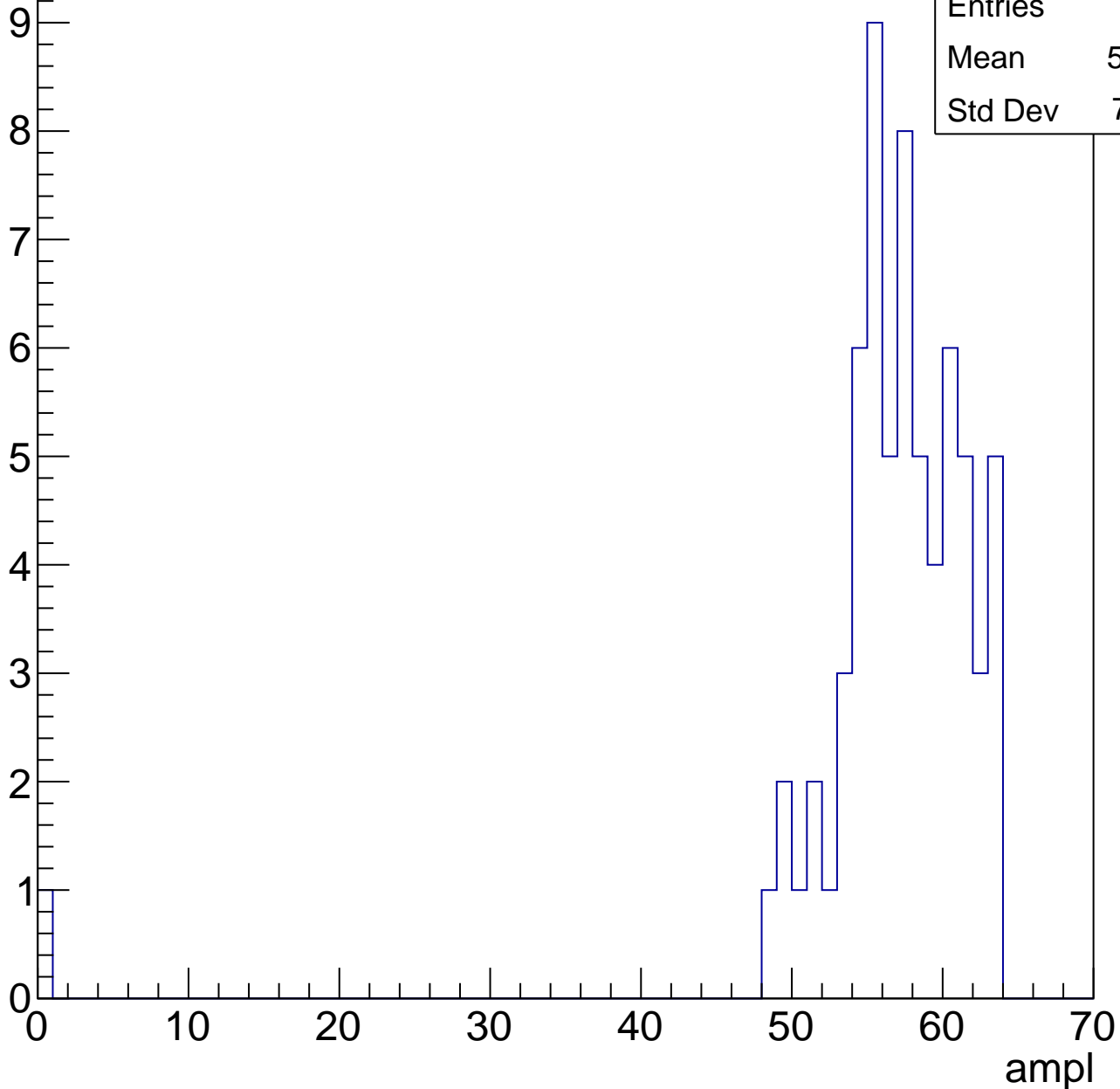


B1L103S, U12-ch125, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	56.06
Std Dev	7.821

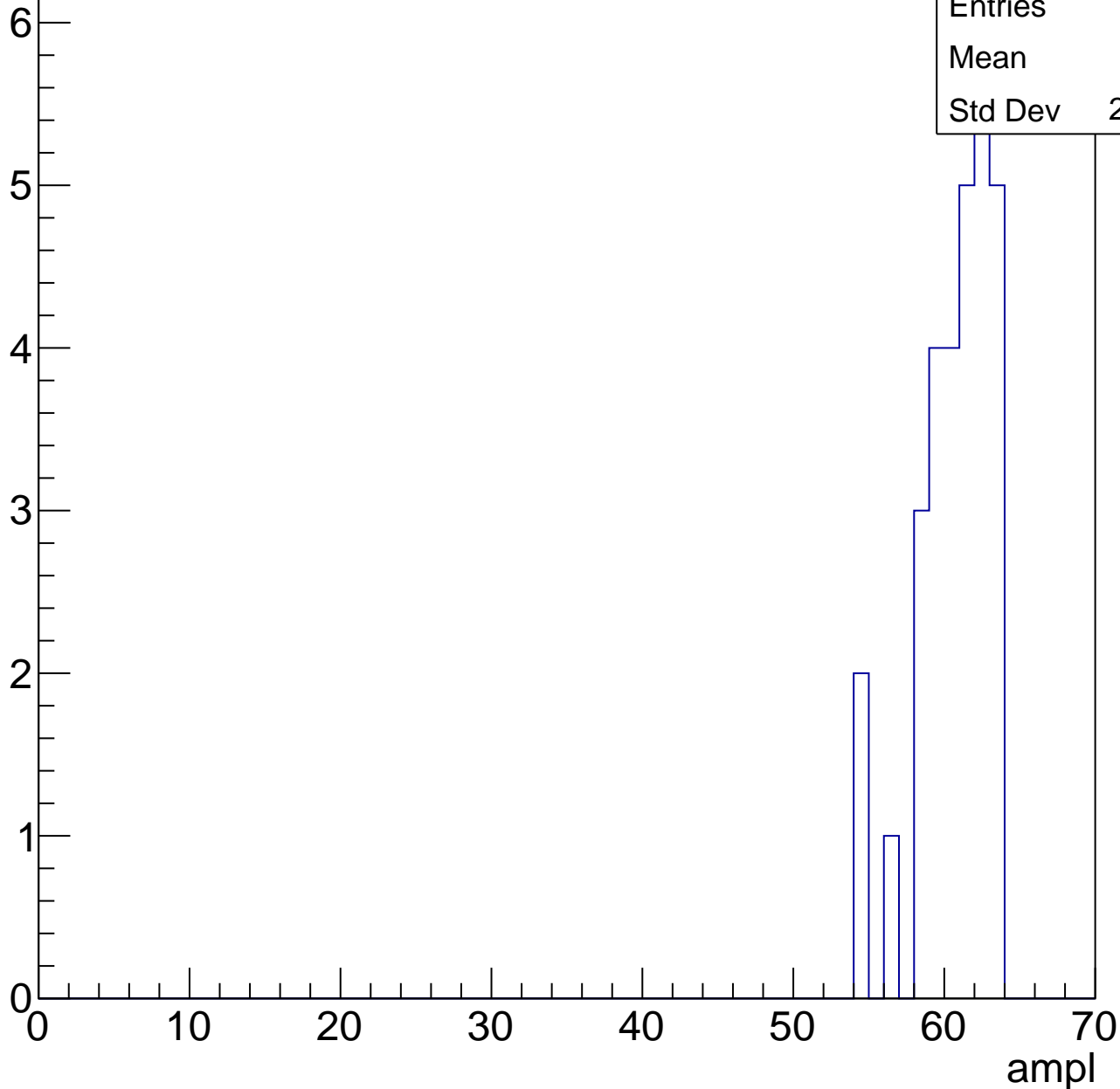


B1L103S, U12-ch125, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	30
Mean	60.2
Std Dev	2.428



B1L103S, U12-ch125, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	1
Mean	62
Std Dev	0

B1L103S, U12-ch125, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

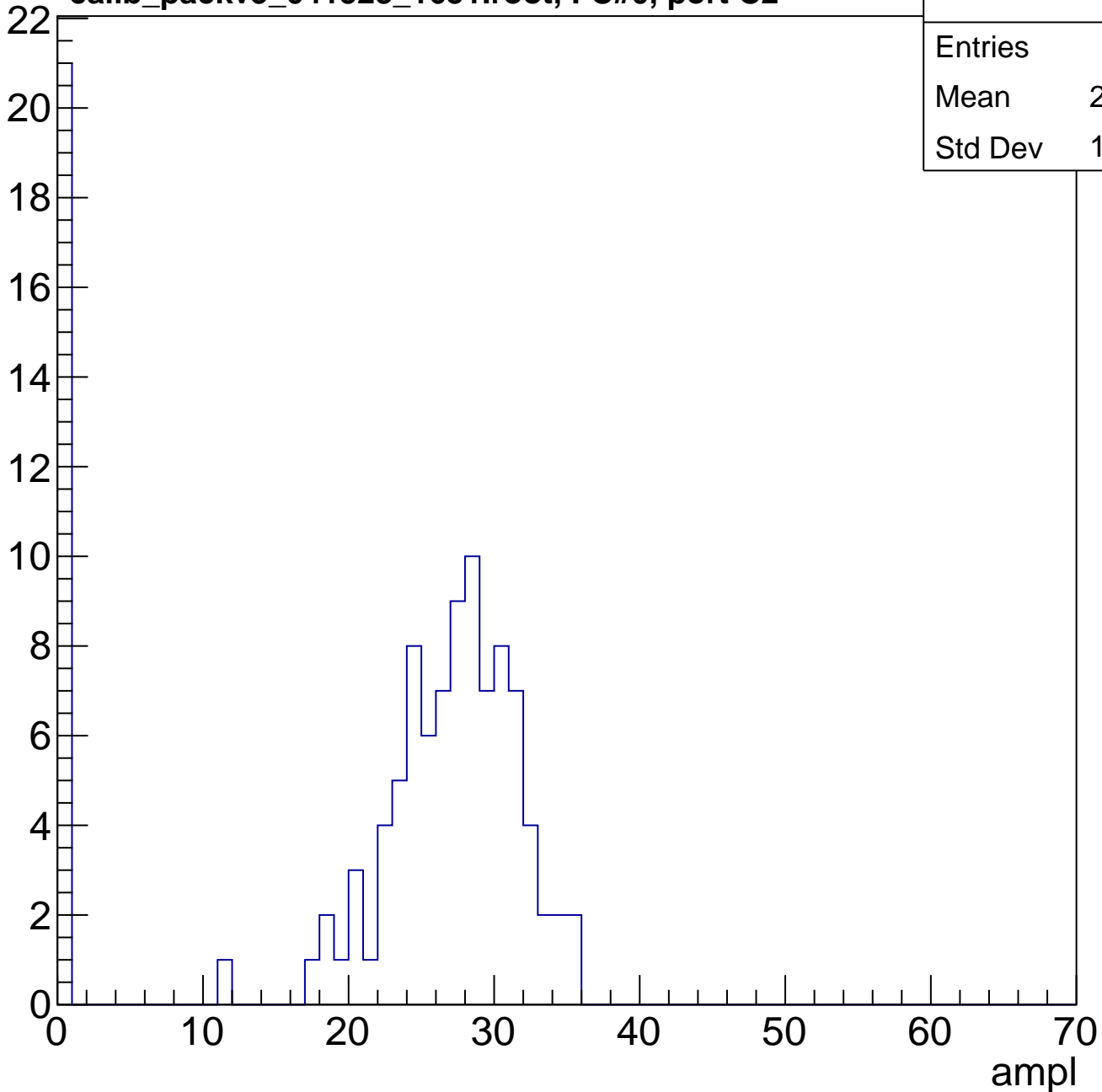
ampl

B1L103S, U12-ch126, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	111
Mean	21.68
Std Dev	11.16

Entry

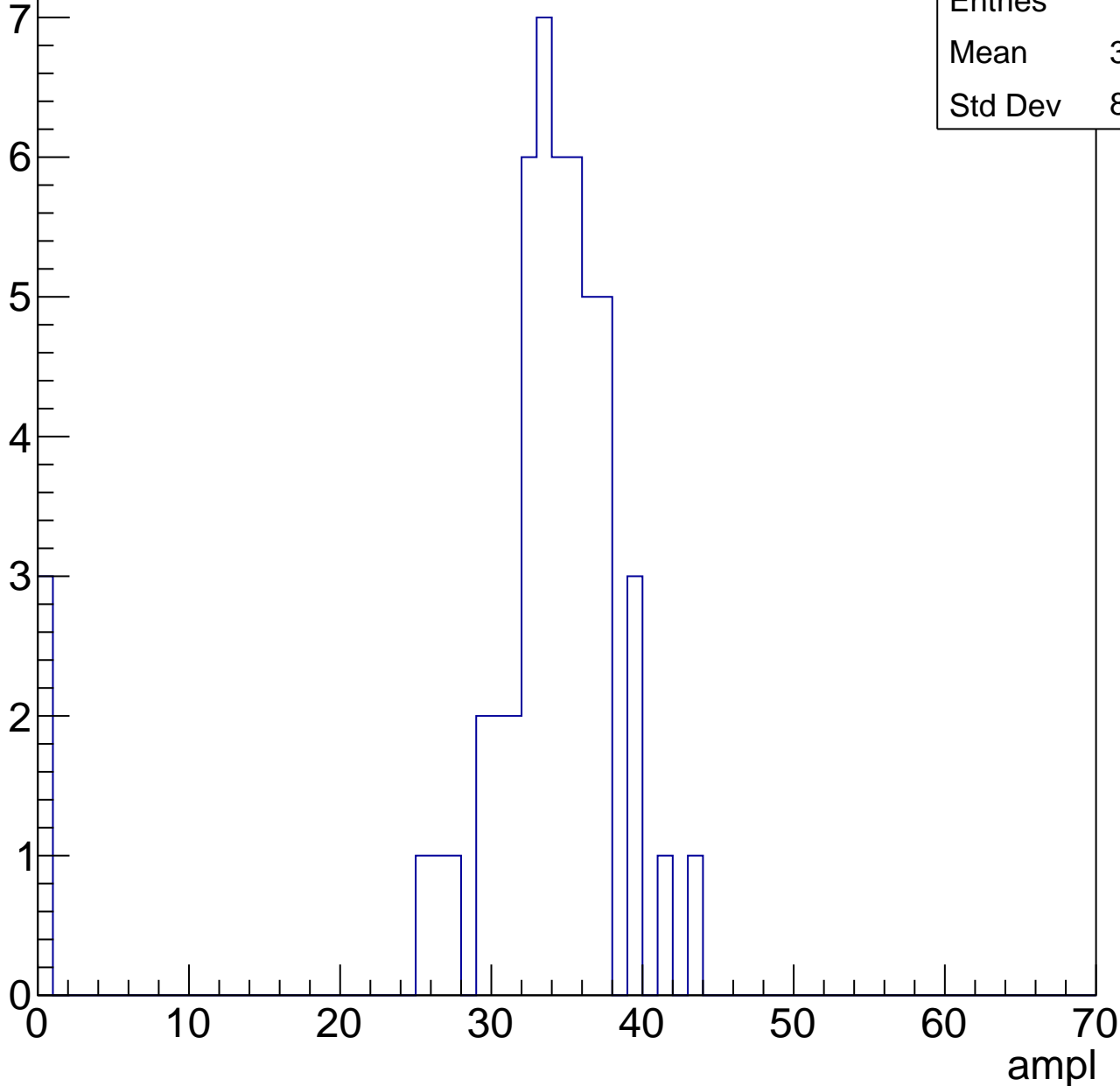


B1L103S, U12-ch126, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	52
Mean	31.94
Std Dev	8.603

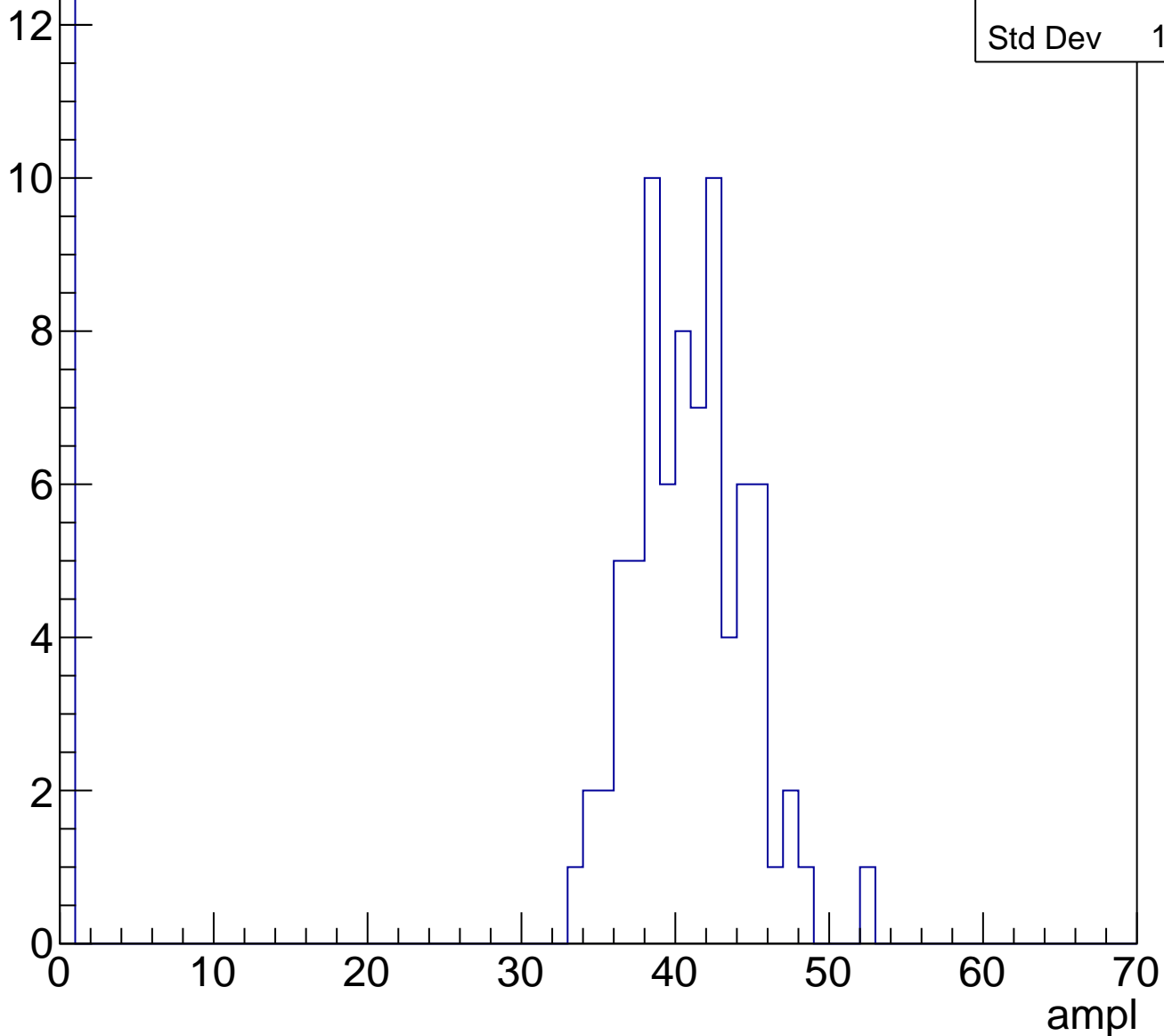


B1L103S, U12-ch126, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	90
Mean	34.7
Std Dev	14.64

Entry

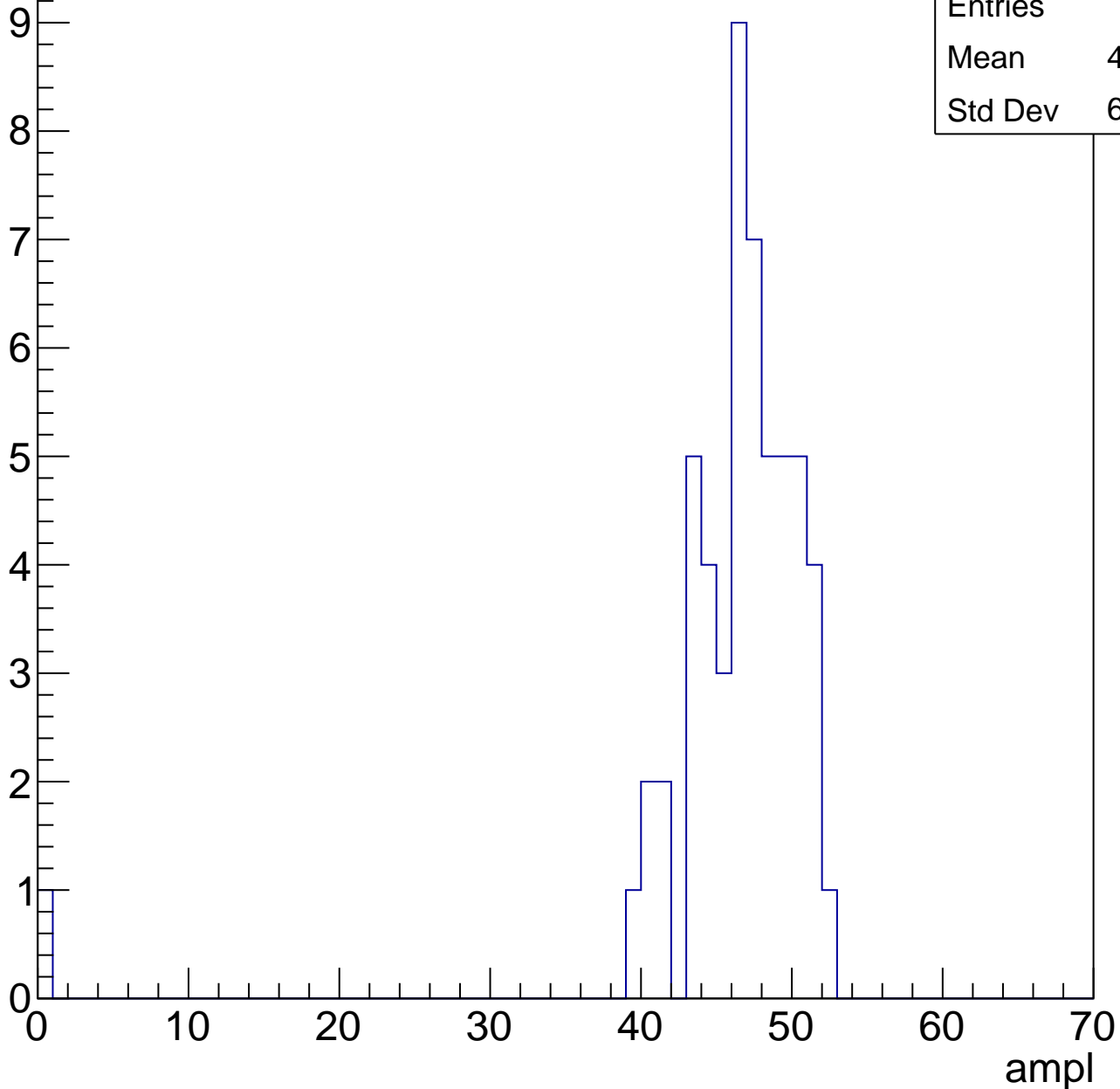


B1L103S, U12-ch126, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	54
Mean	45.57
Std Dev	6.978

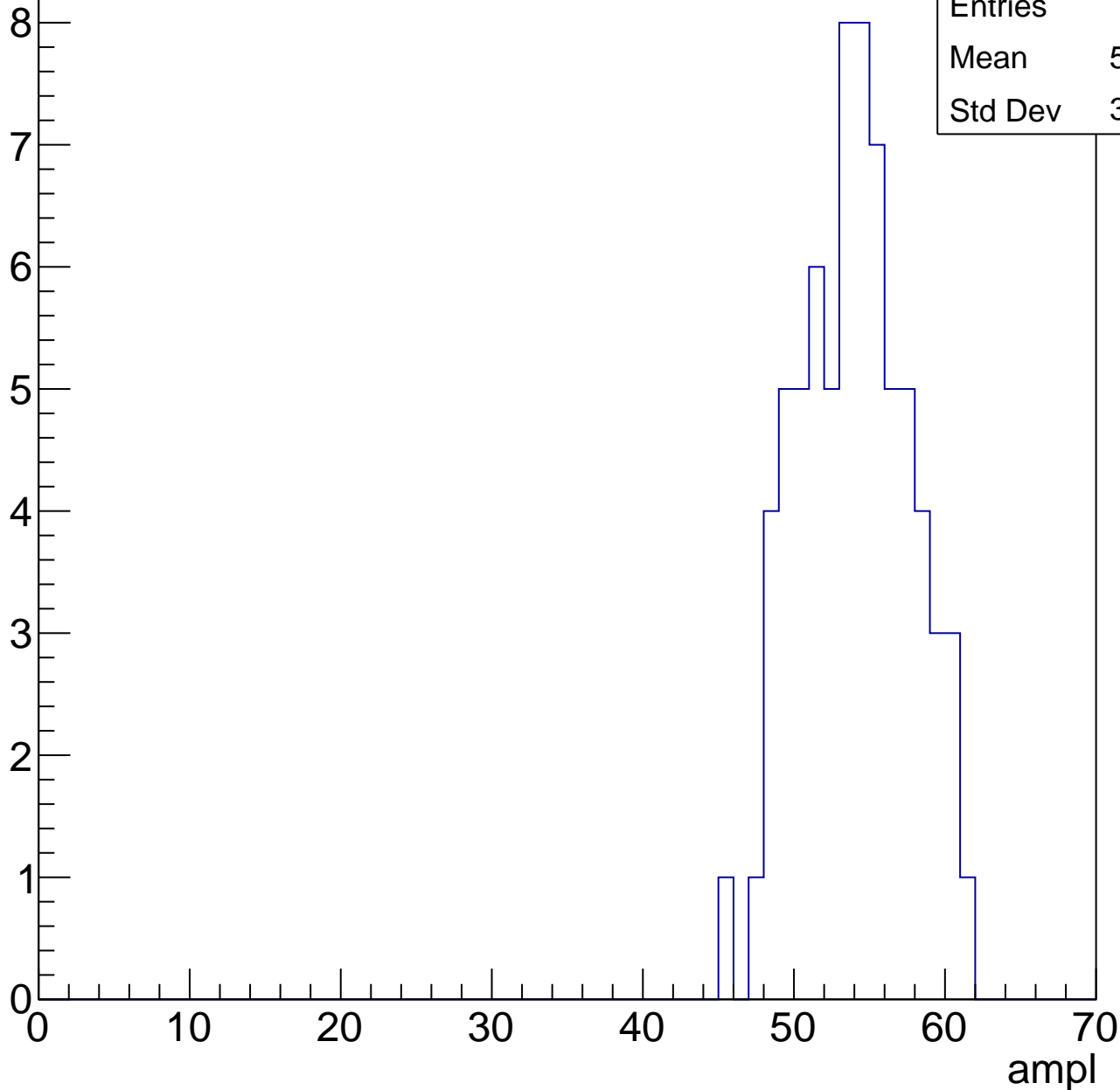


B1L103S, U12-ch126, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	53.54
Std Dev	3.587

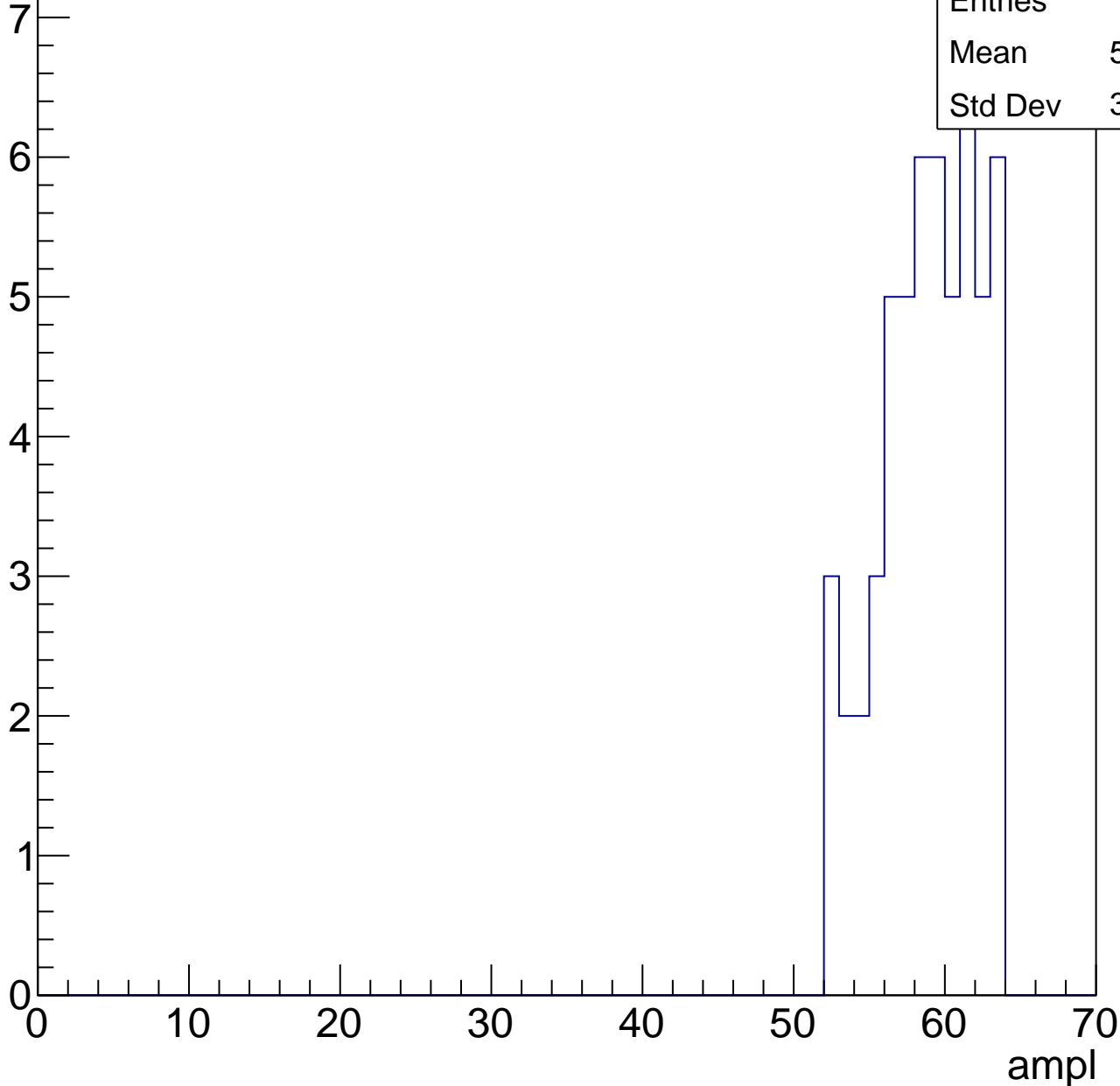


B1L103S, U12-ch126, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

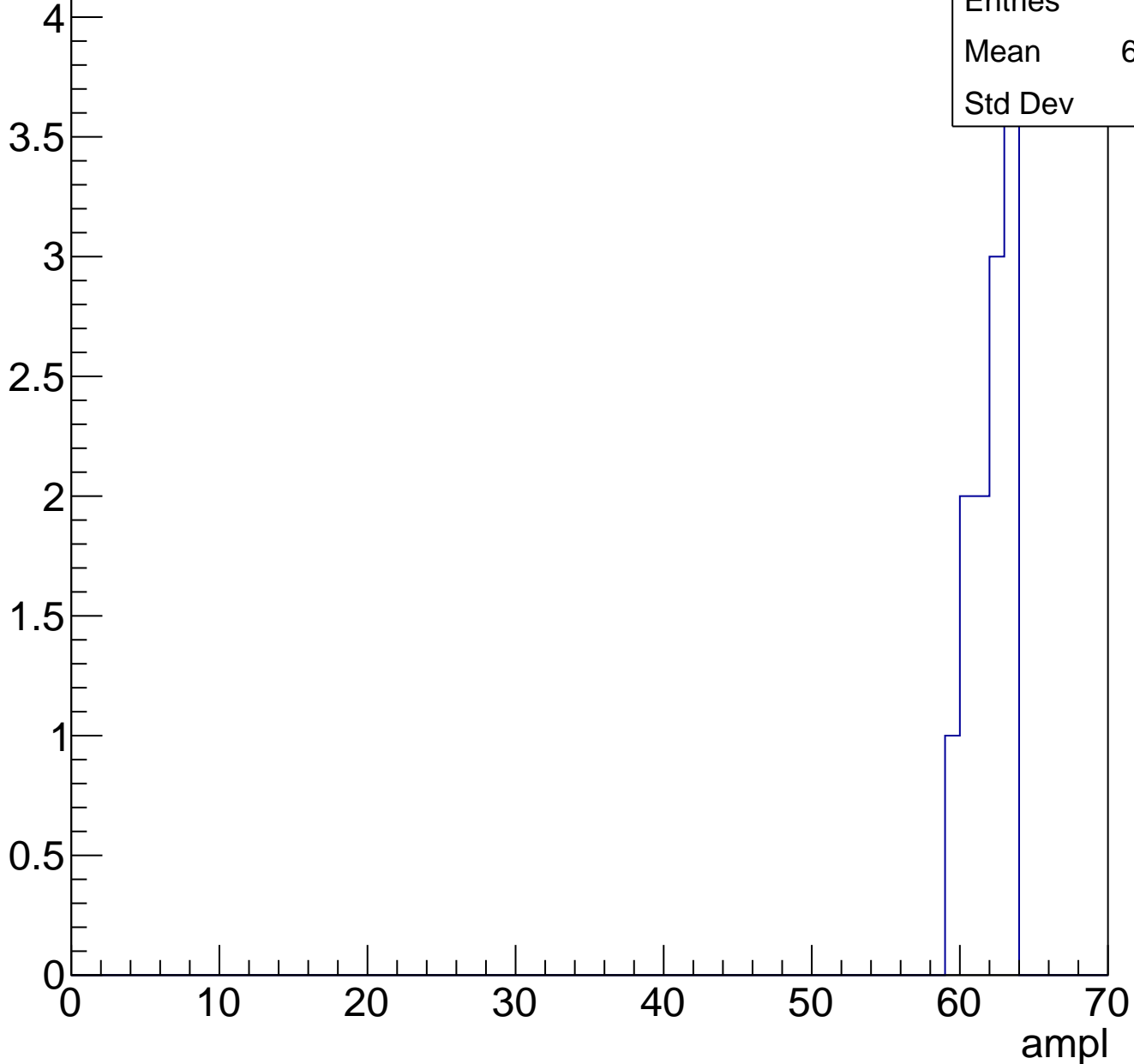
Entries	55
Mean	58.49
Std Dev	3.156



B1L103S, U12-ch126, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch126, adc7

calib_packv5_041523_1651.root, FC#0, port C2

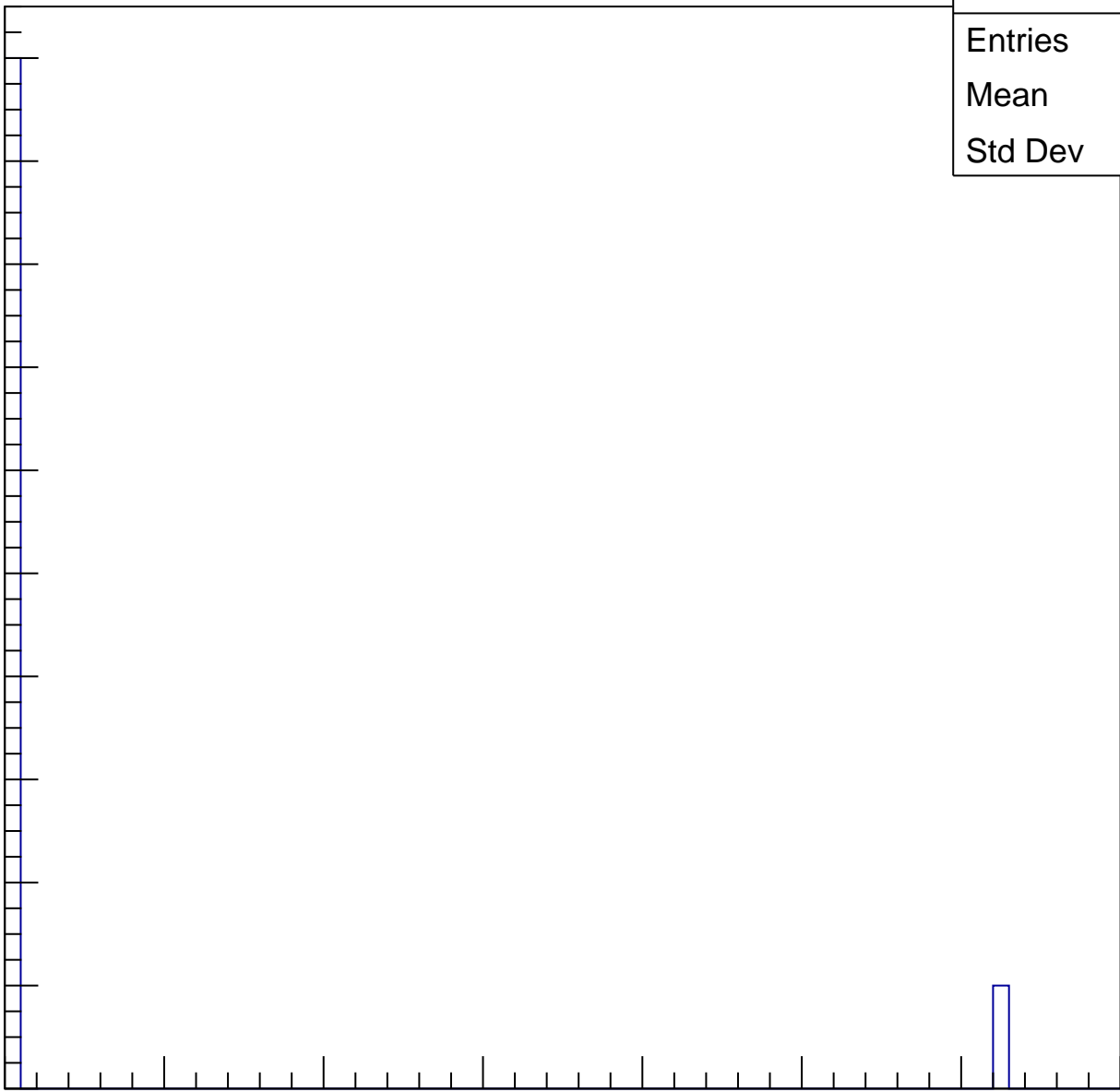
Entries	22
Mean	5.636
Std Dev	17.82

Entry

20
18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

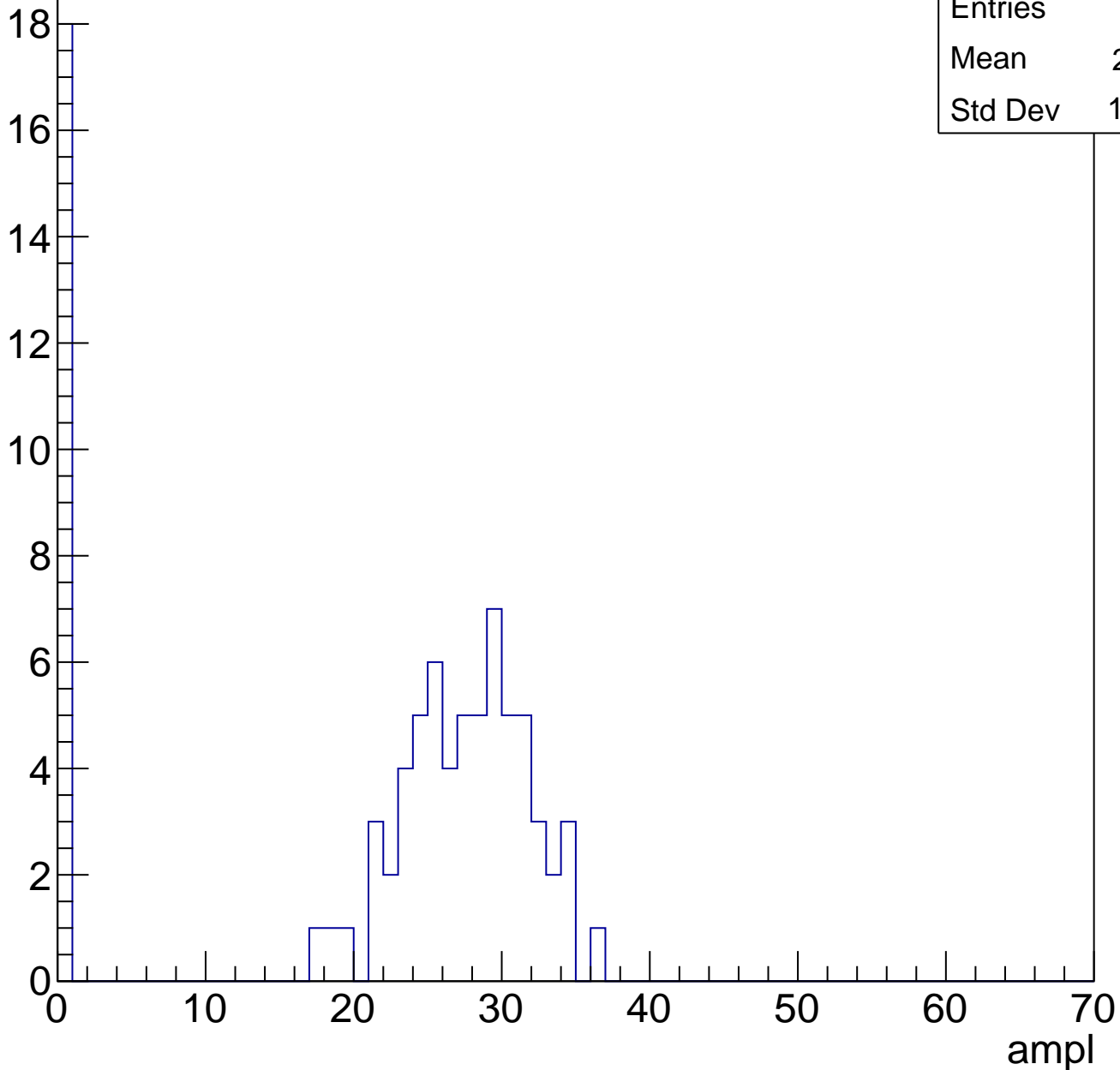


B1L103S, U12-ch127, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	81
Mean	21.11
Std Dev	11.86

Entry



B1L103S, U12-ch127, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	95
Mean	29.93
Std Dev	12.49

Entry

12

10

8

6

4

2

0

0

10

20

30

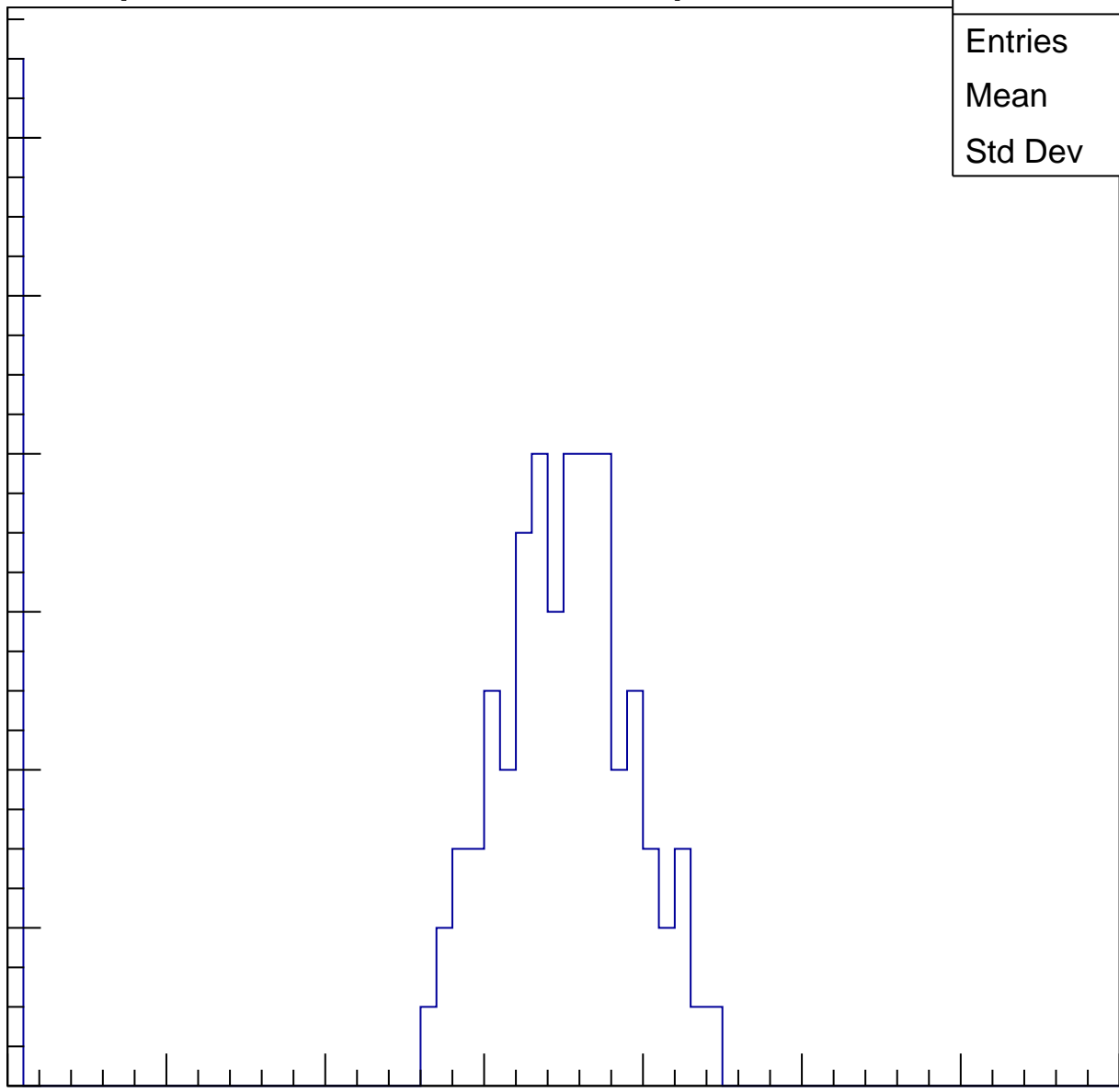
40

50

60

70

ampl

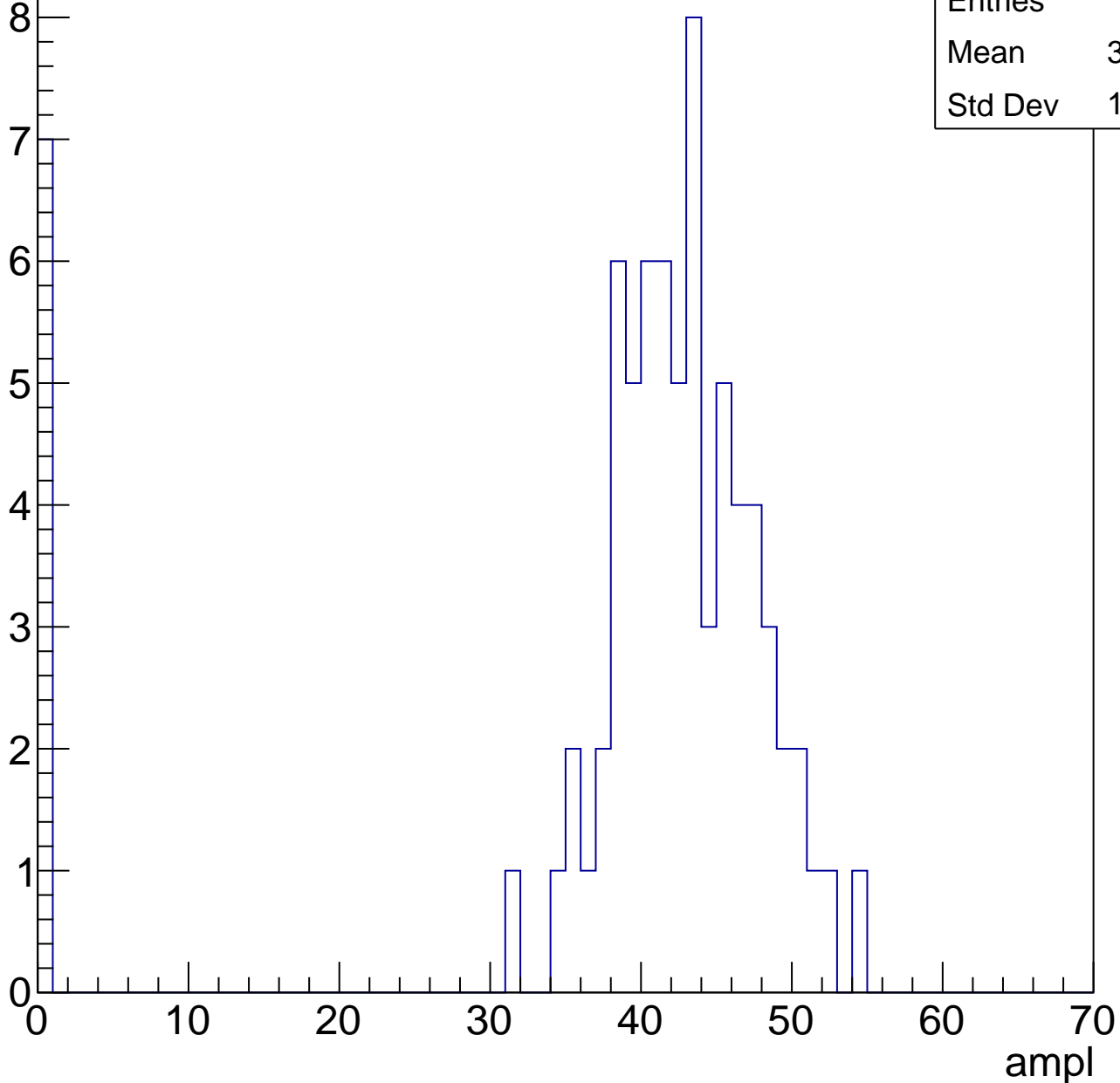


B1L103S, U12-ch127, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	76
Mean	38.63
Std Dev	13.04

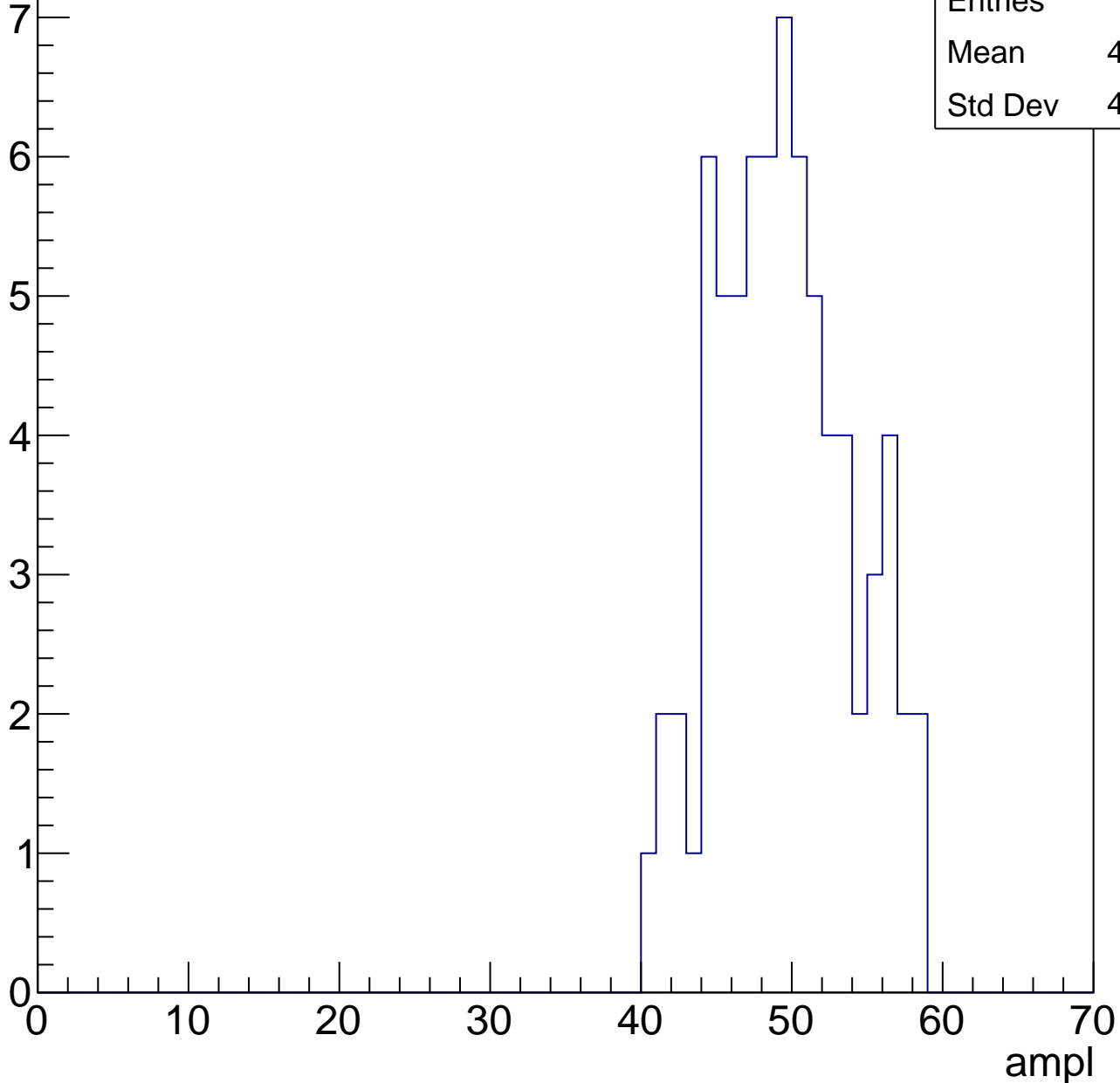


B1L103S, U12-ch127, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	73
Mean	49.08
Std Dev	4.407

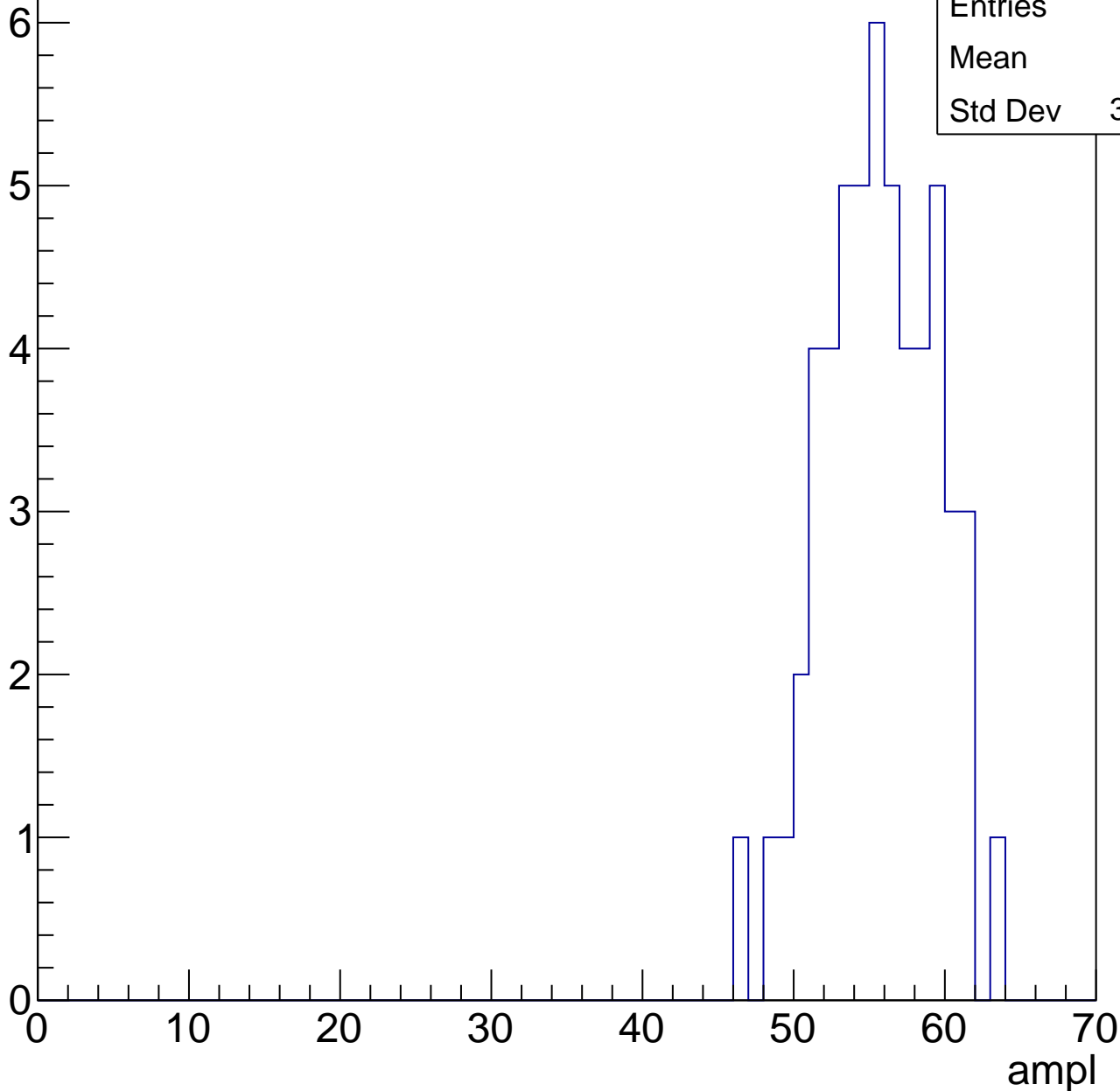


B1L103S, U12-ch127, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	54
Mean	55.2
Std Dev	3.658

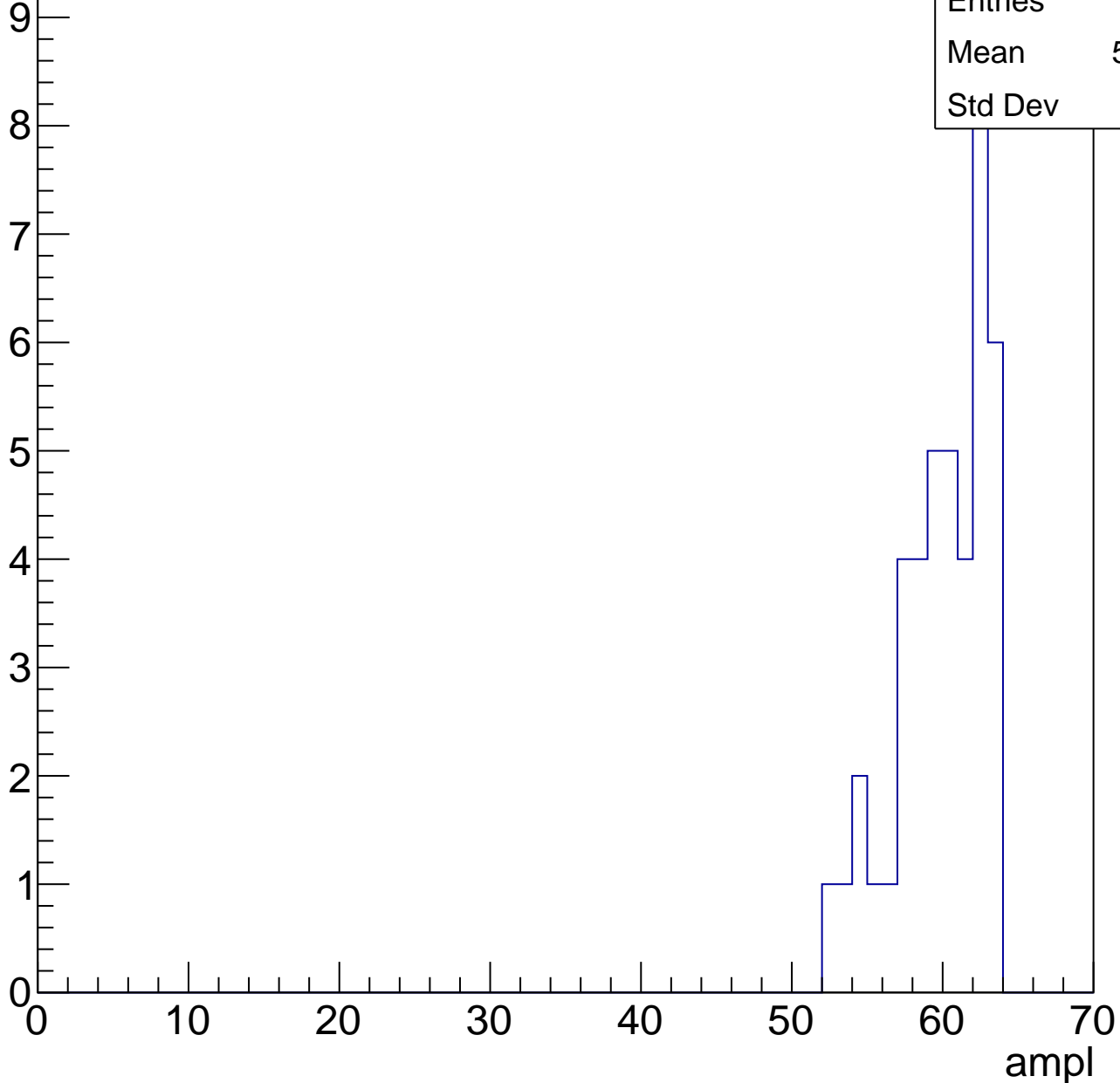


B1L103S, U12-ch127, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

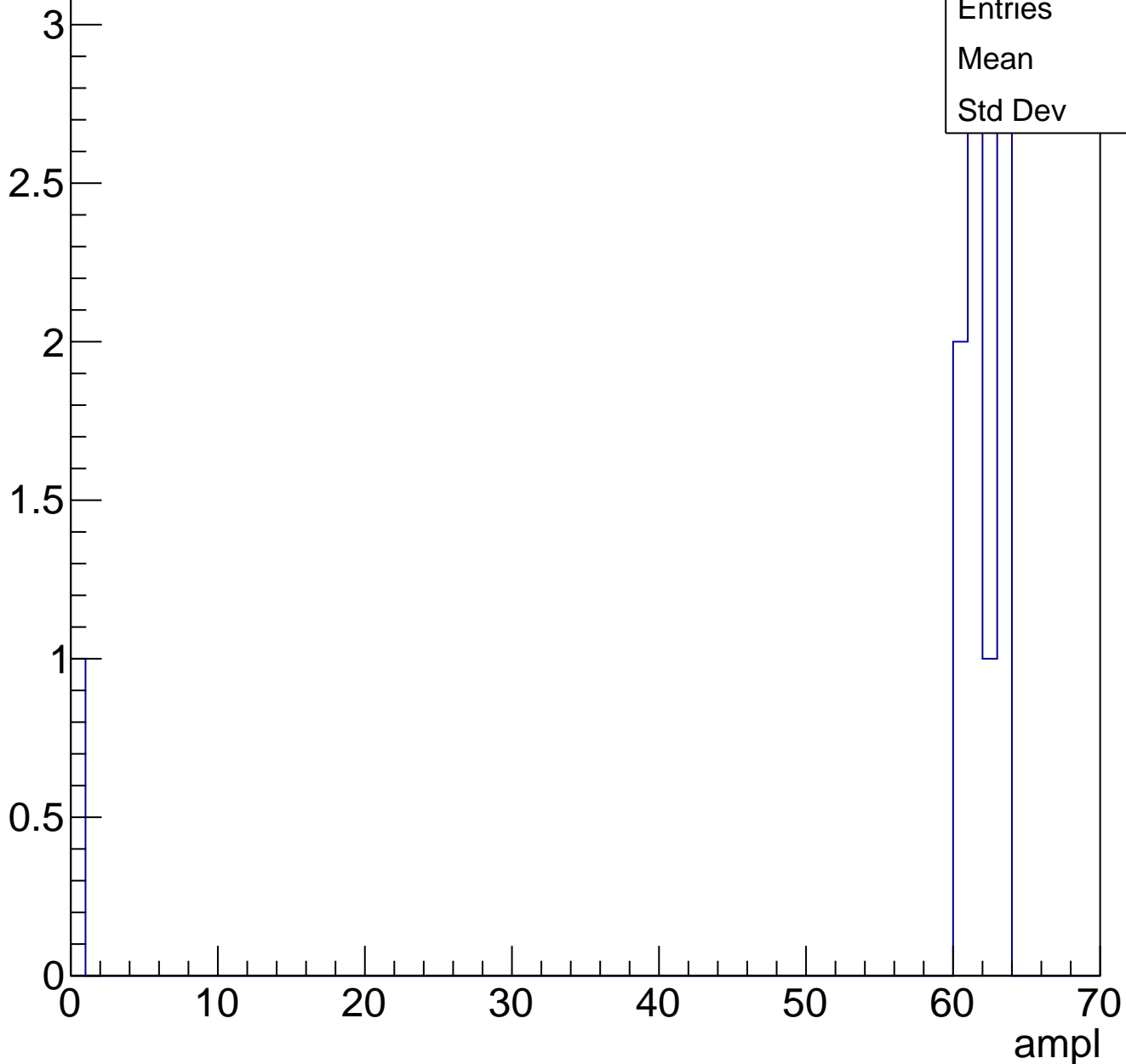
Entries	43
Mean	59.51
Std Dev	2.92



B1L103S, U12-ch127, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U12-ch127, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

ampl

B1L103S, U12-ch127, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

