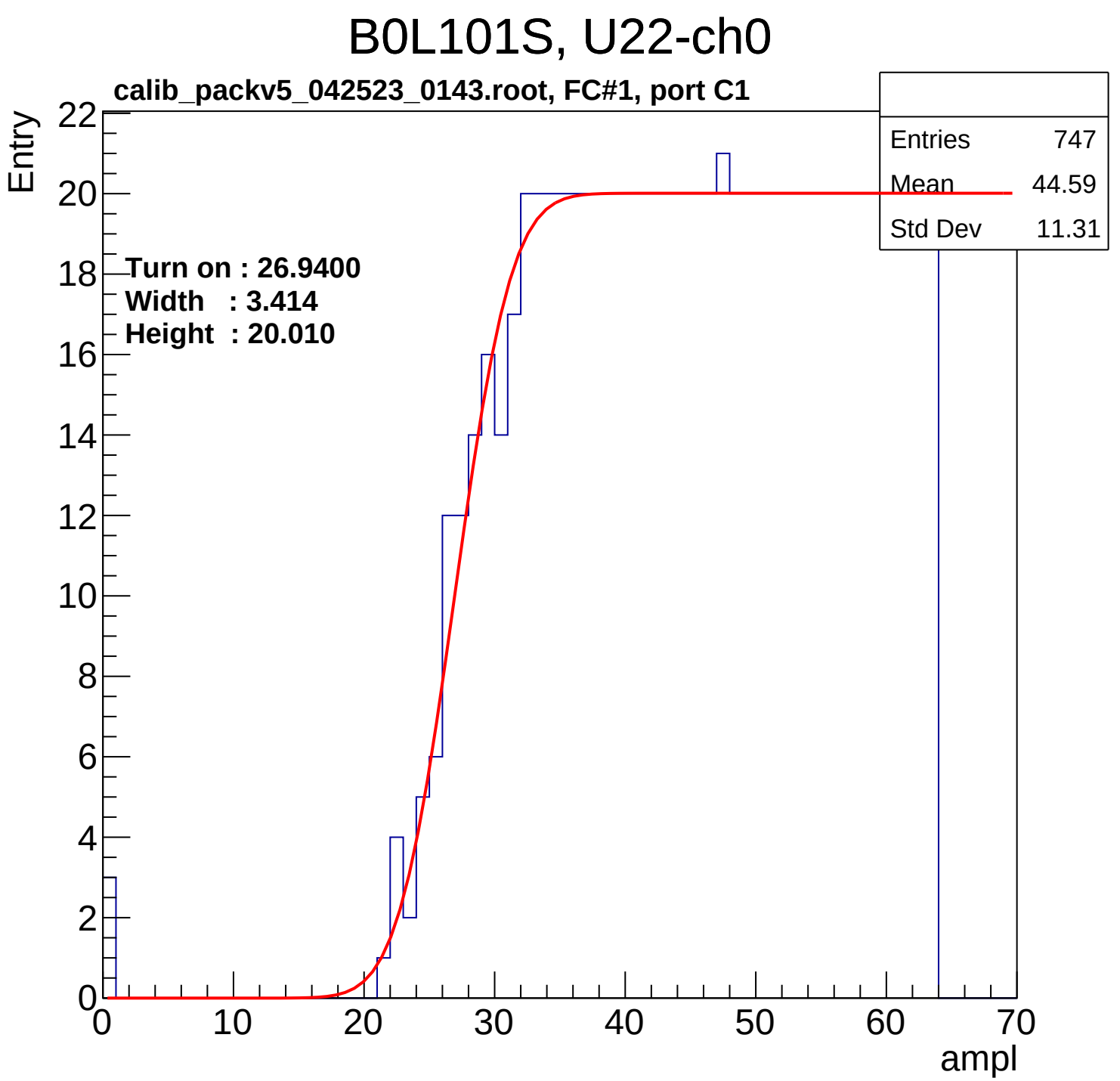
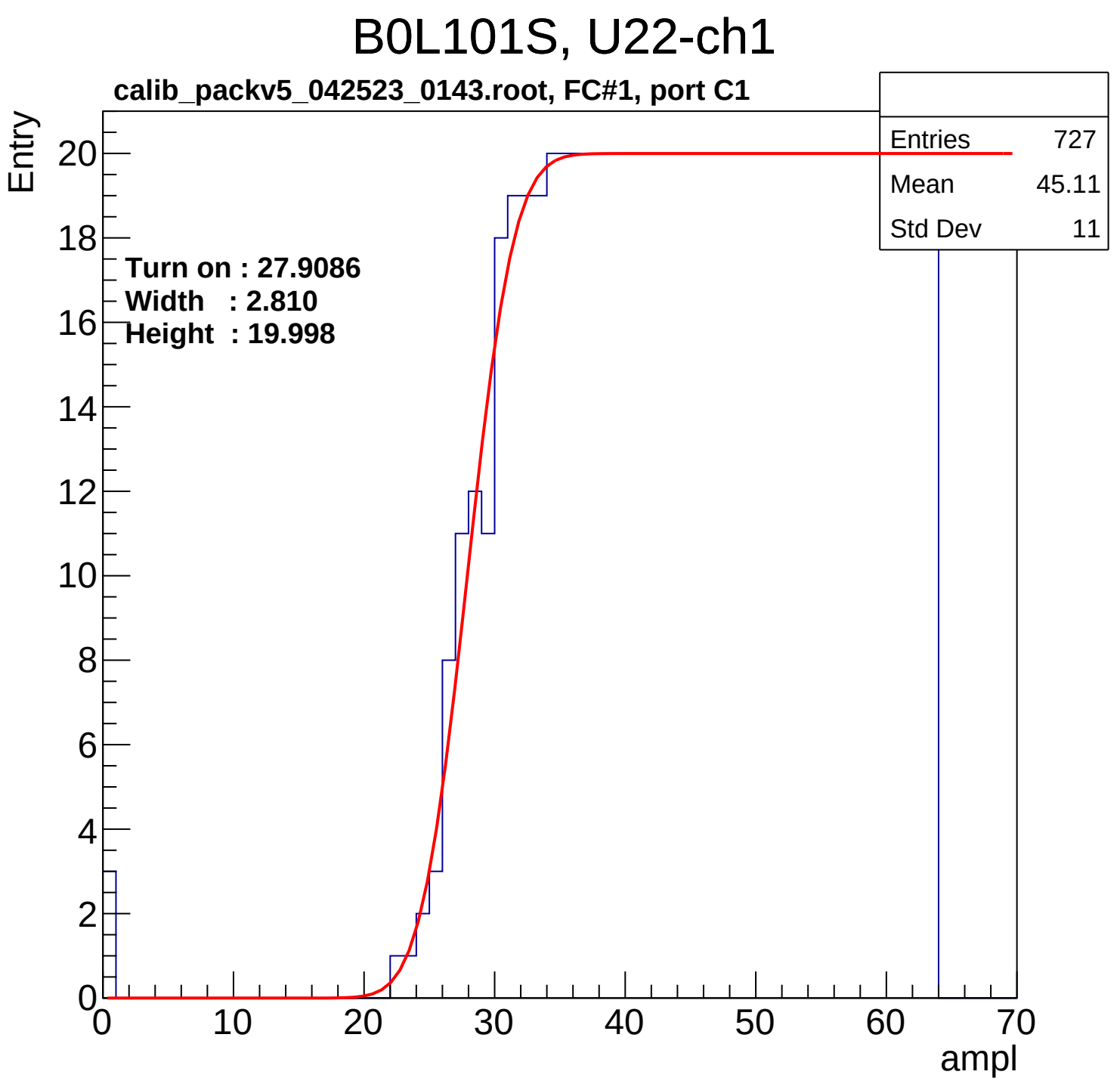
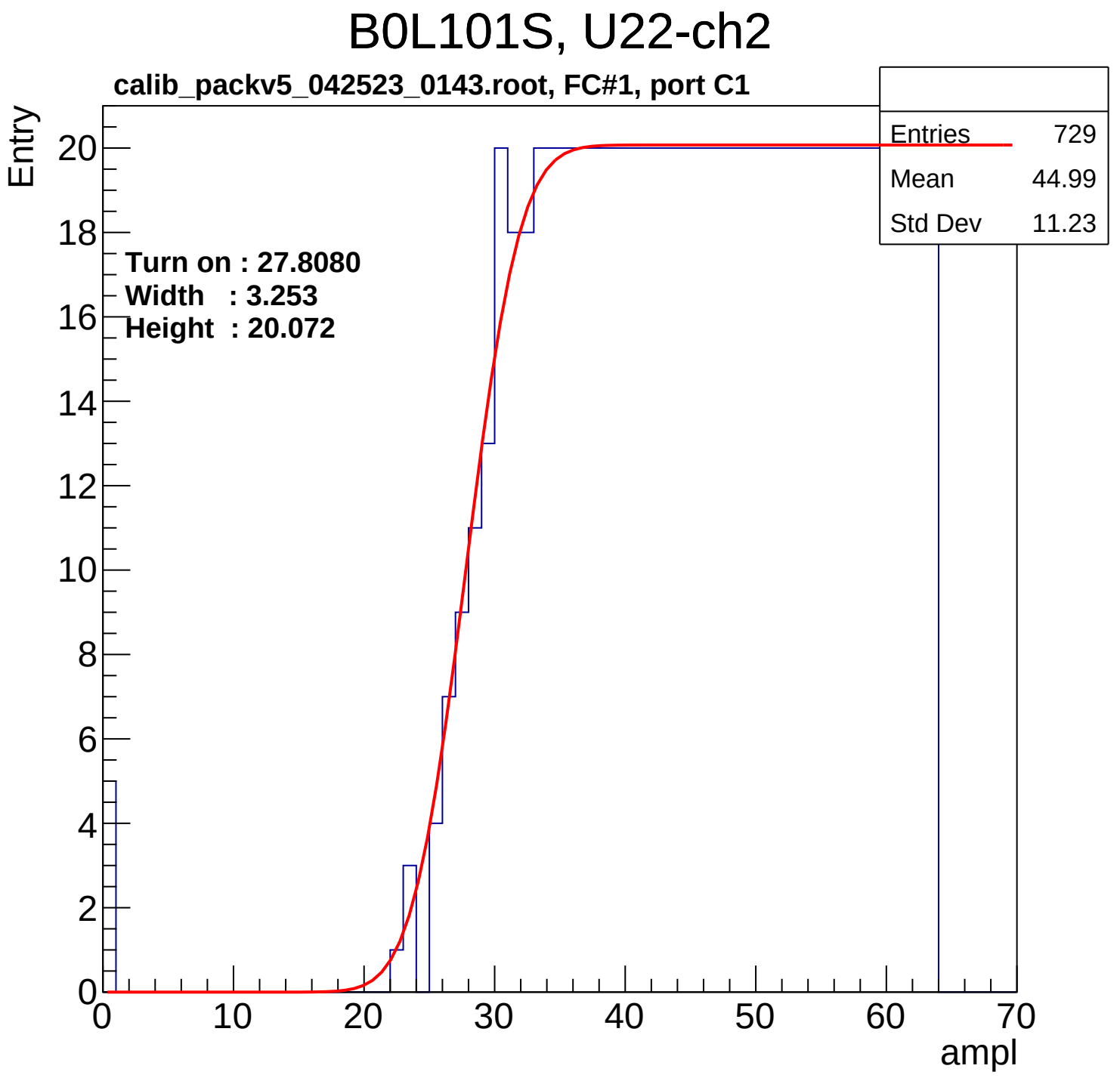
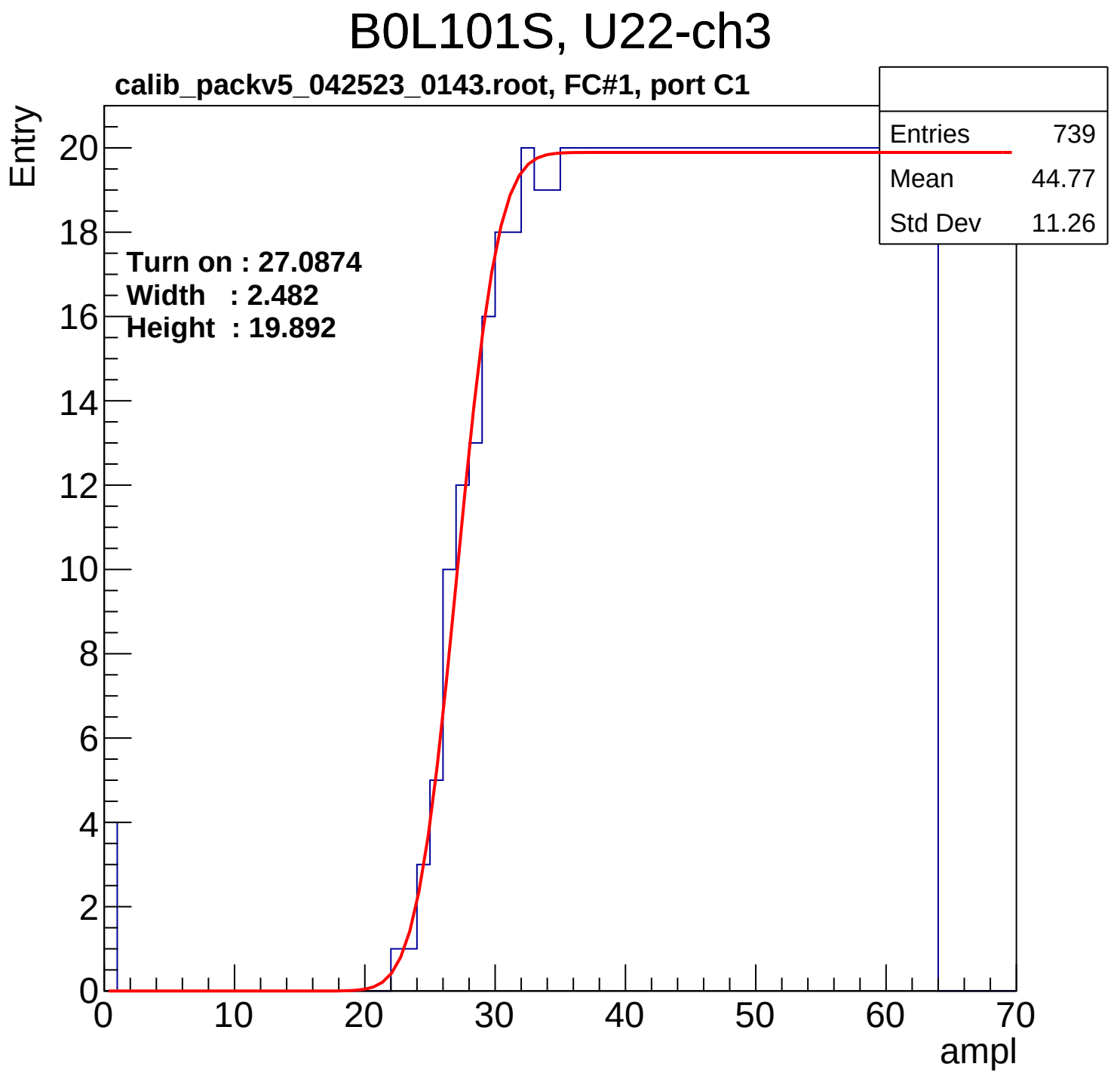
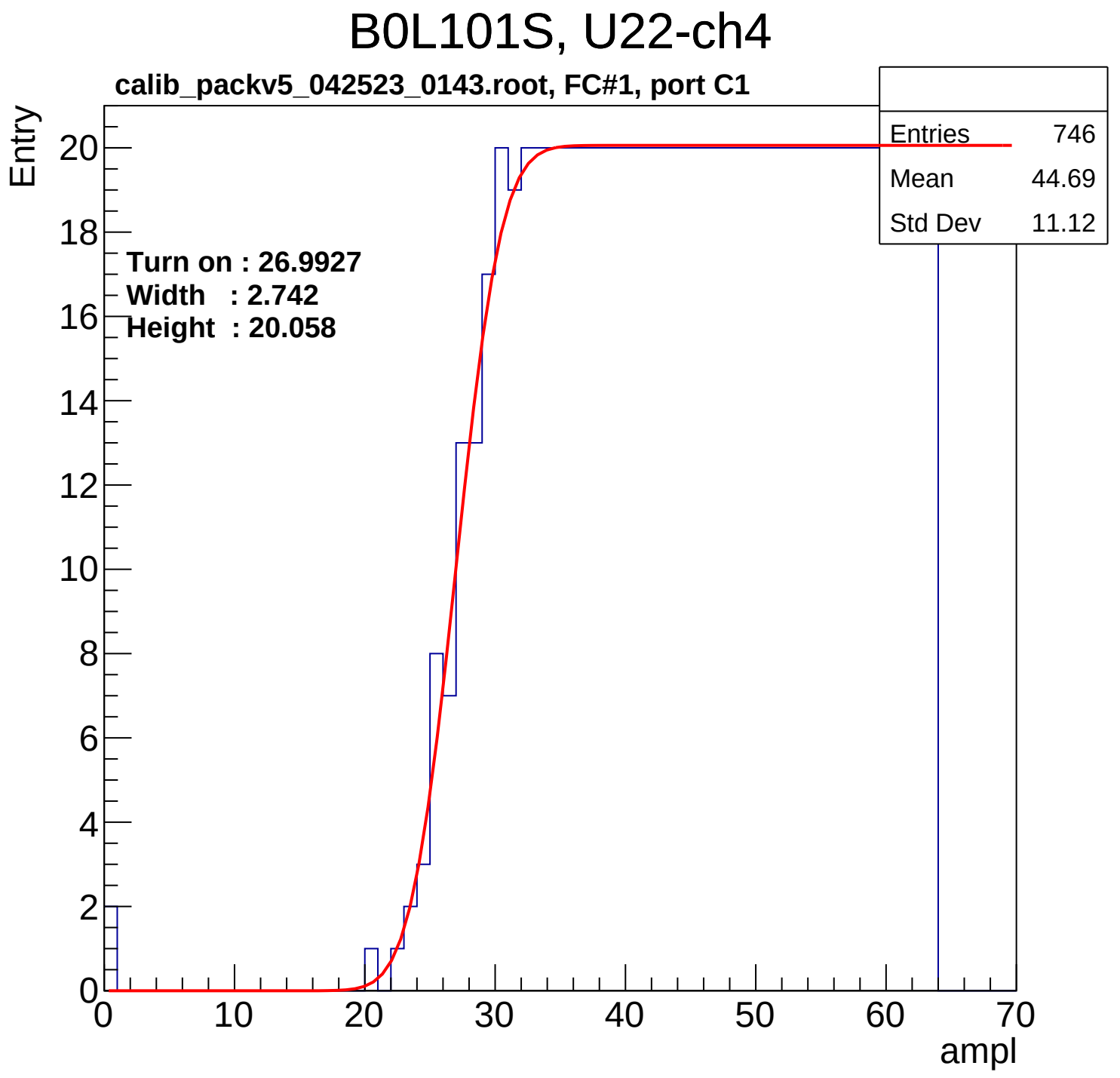
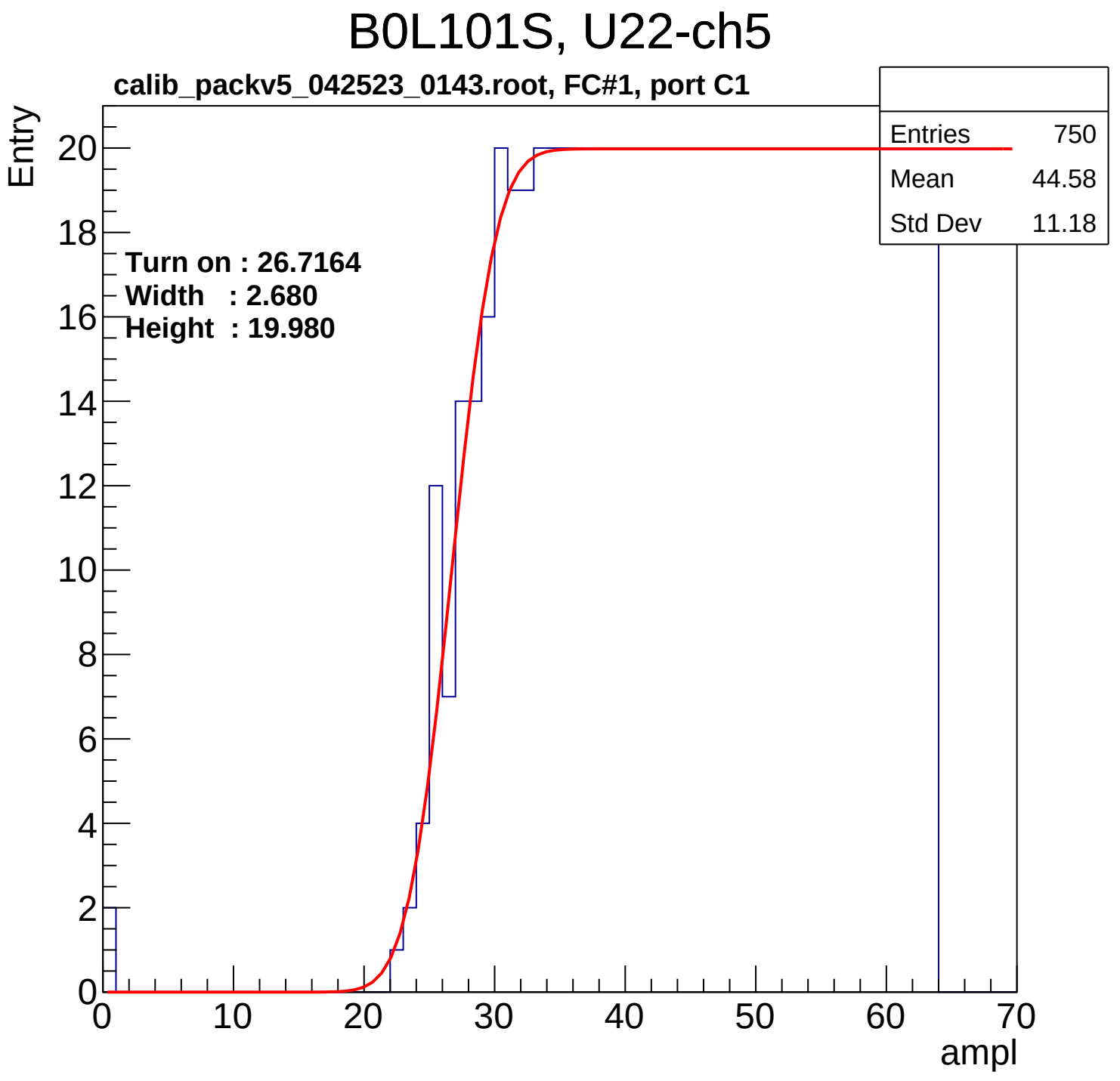

B0L101S, U22-ch0
calib_packv5_042523_0143.root, FC#1, port C1
Entries 747
Mean 44.59
Std Dev 11.31
Turn on : 26.9400
Width : 3.414
Height : 20.010
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70

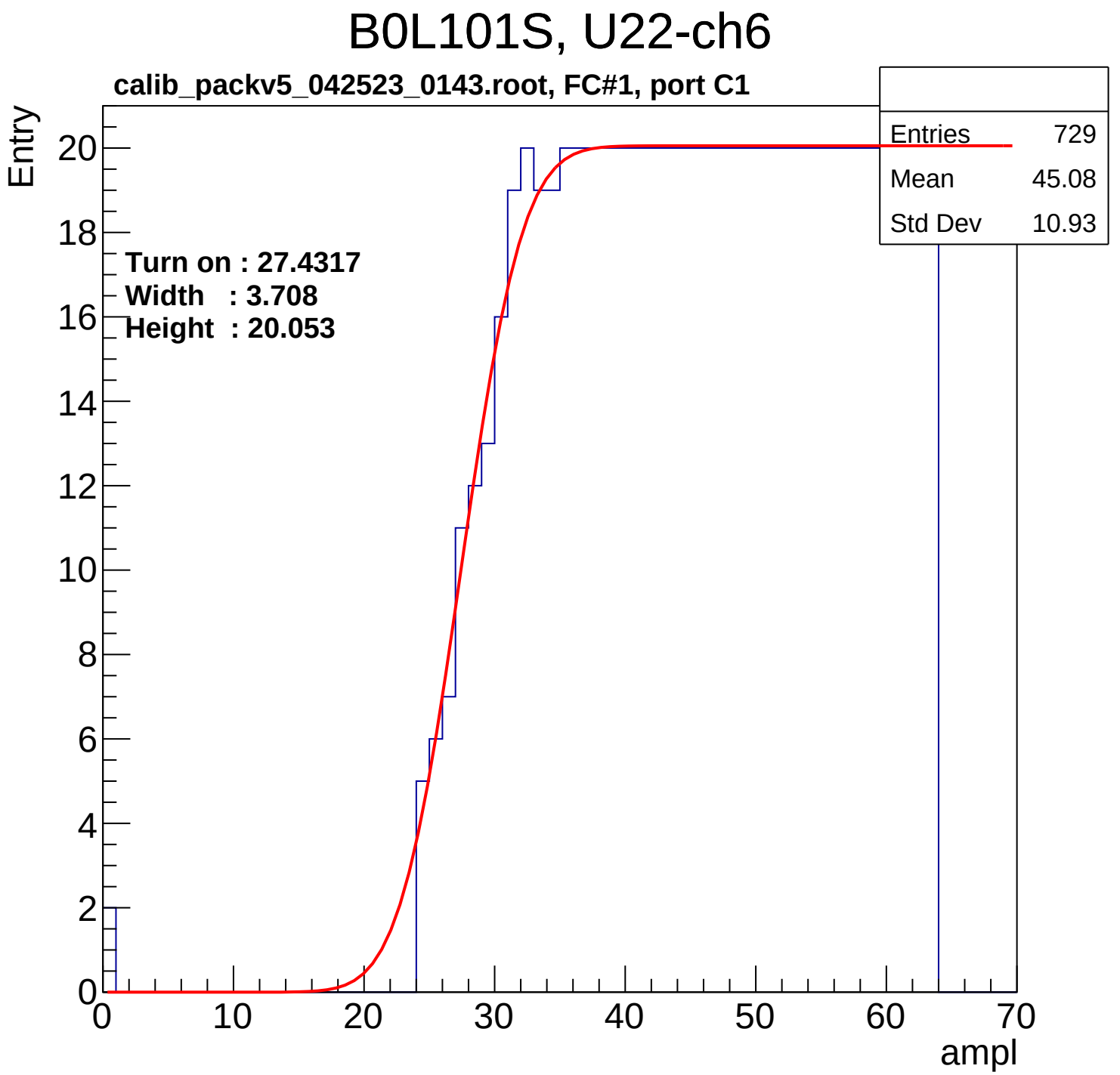

B0L101S, U22-ch1
calib_packv5_042523_0143.root, FC#1, port C1
Entries 727
Mean 45.11
Std Dev 11
Turn on : 27.9086
Width : 2.810
Height : 19.998
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

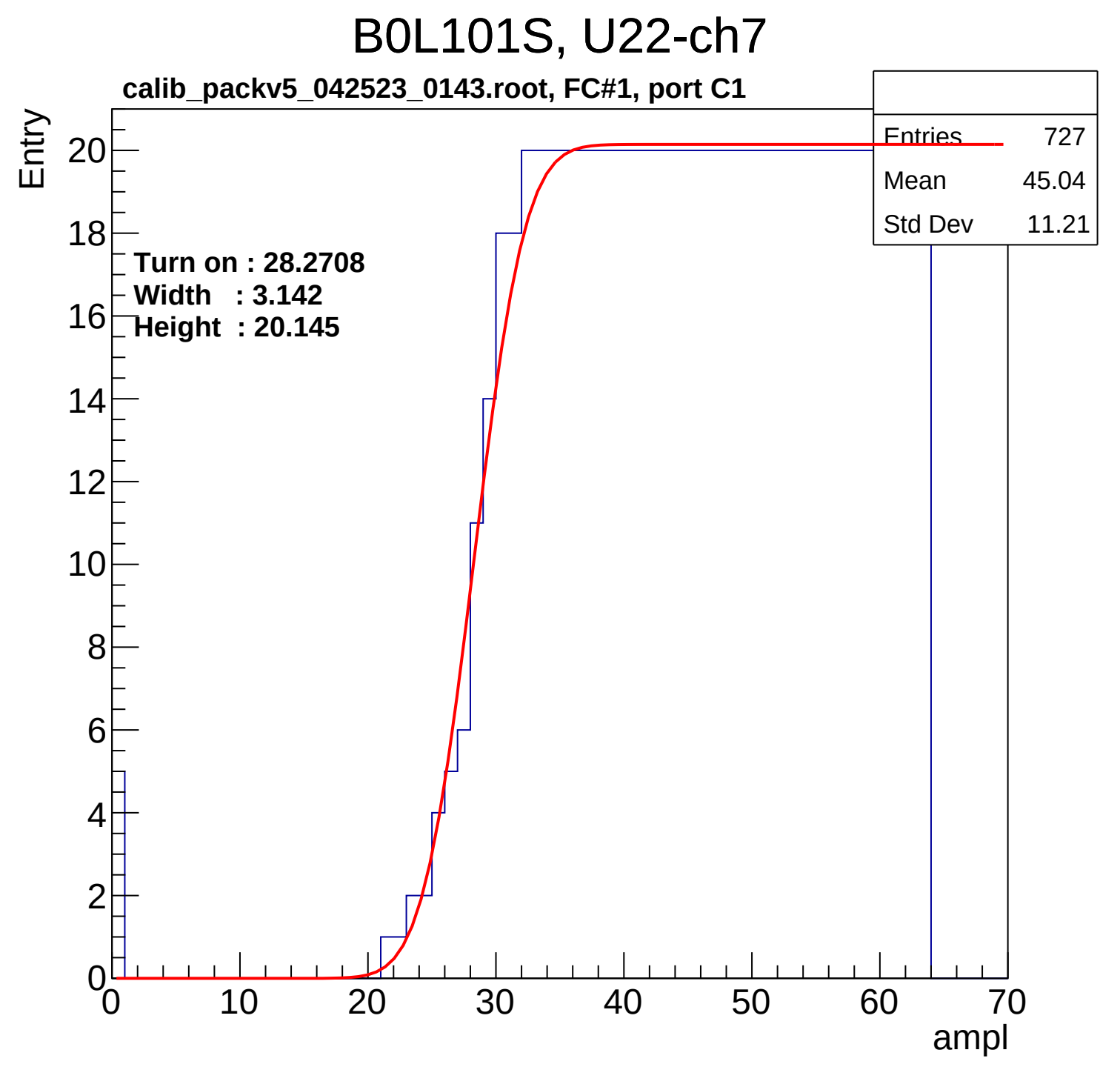

B0L101S, U22-ch2
calib_packv5_042523_0143.root, FC#1, port C1
Entries 729
Mean 44.99
Std Dev 11.23
Turn on : 27.8080
Width : 3.253
Height : 20.072
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

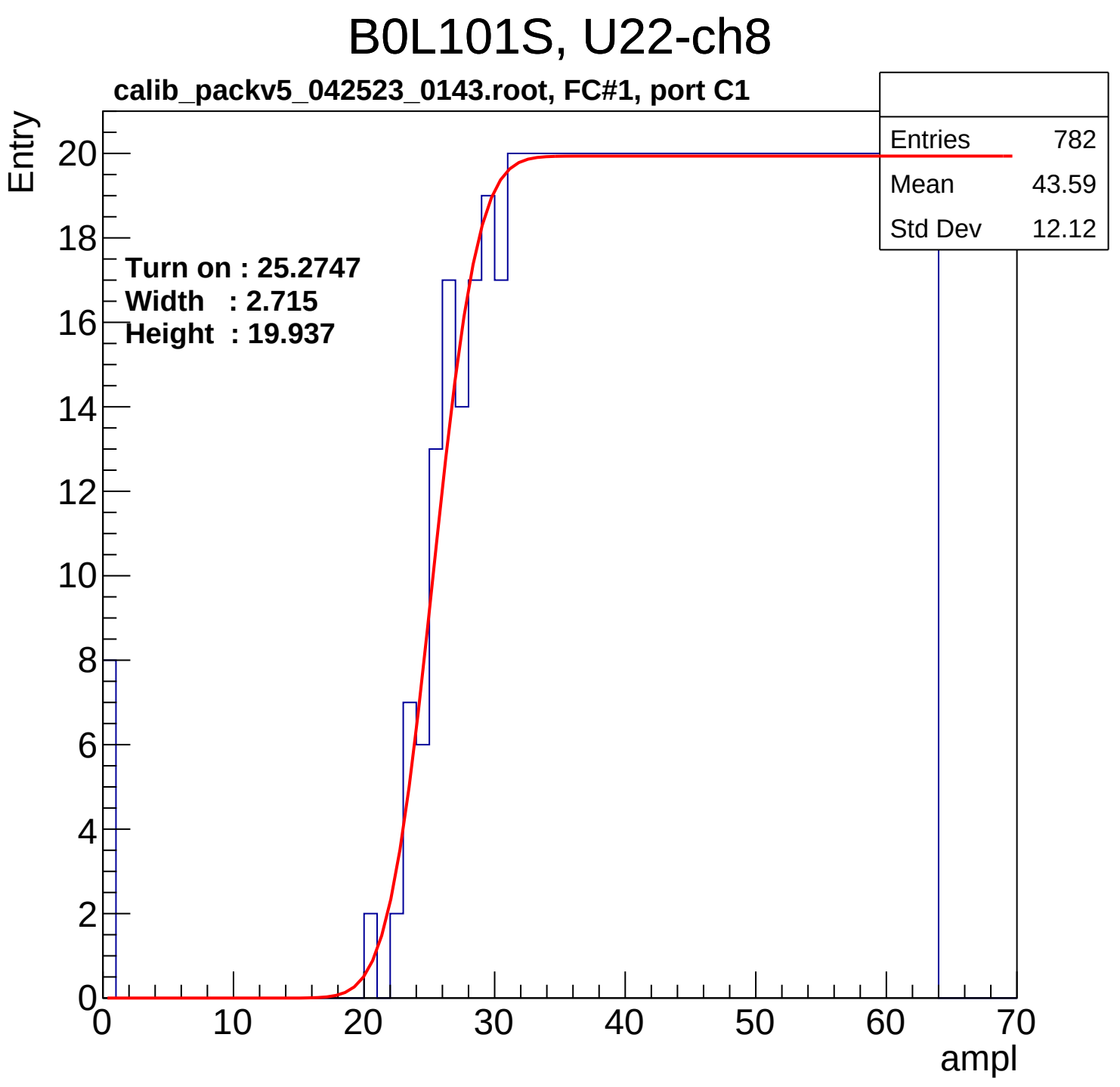

B0L101S, U22-ch3
calib_packv5_042523_0143.root, FC#1, port C1
Entries 739
Mean 44.77
Std Dev 11.26
Turn on : 27.0874
Width : 2.482
Height : 19.892
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

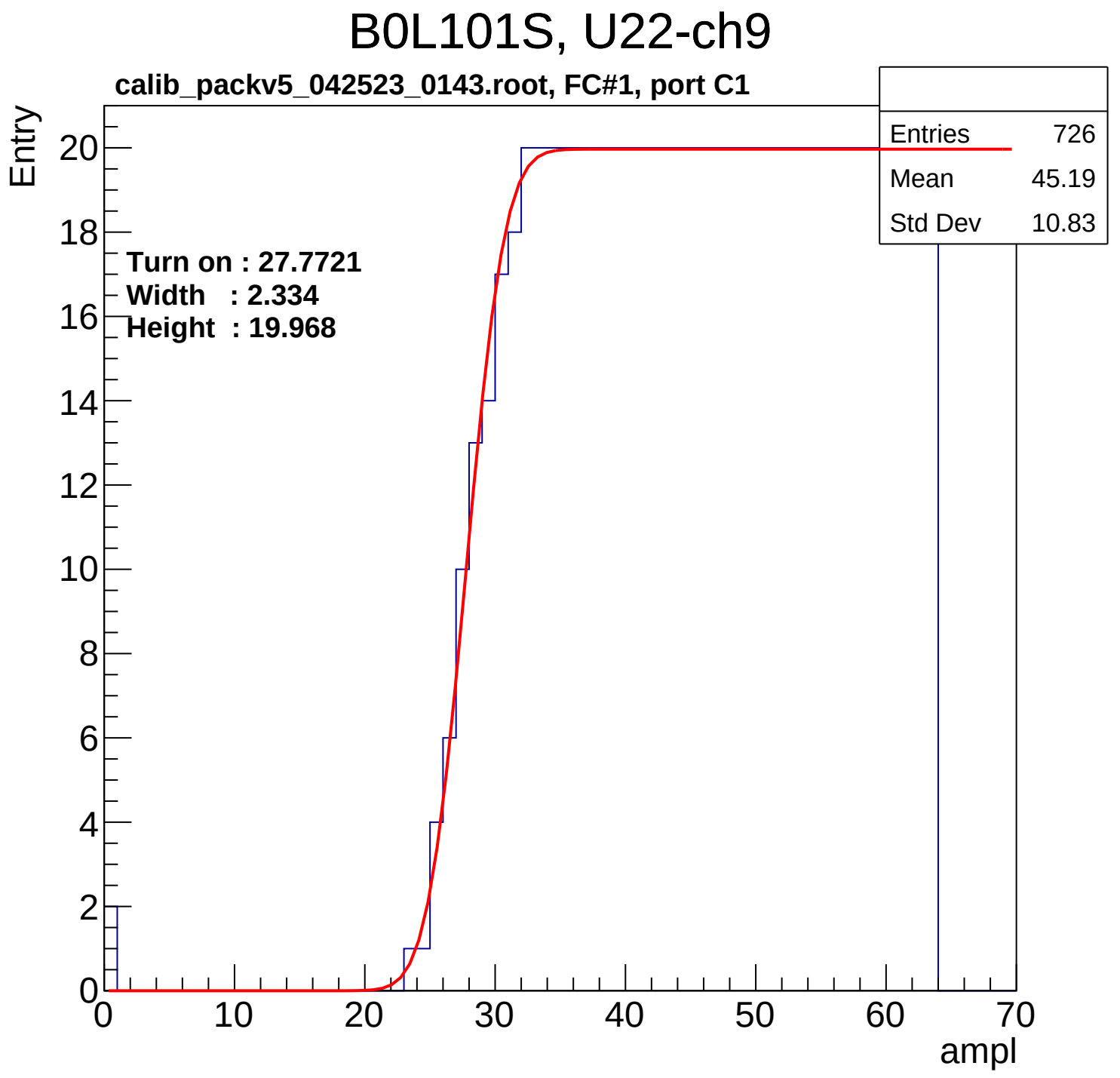

B0L101S, U22-ch4
calib_packv5_042523_0143.root, FC#1, port C1
Entries 746
Mean 44.69
Std Dev 11.12
Turn on : 26.9927
Width : 2.742
Height : 20.058
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

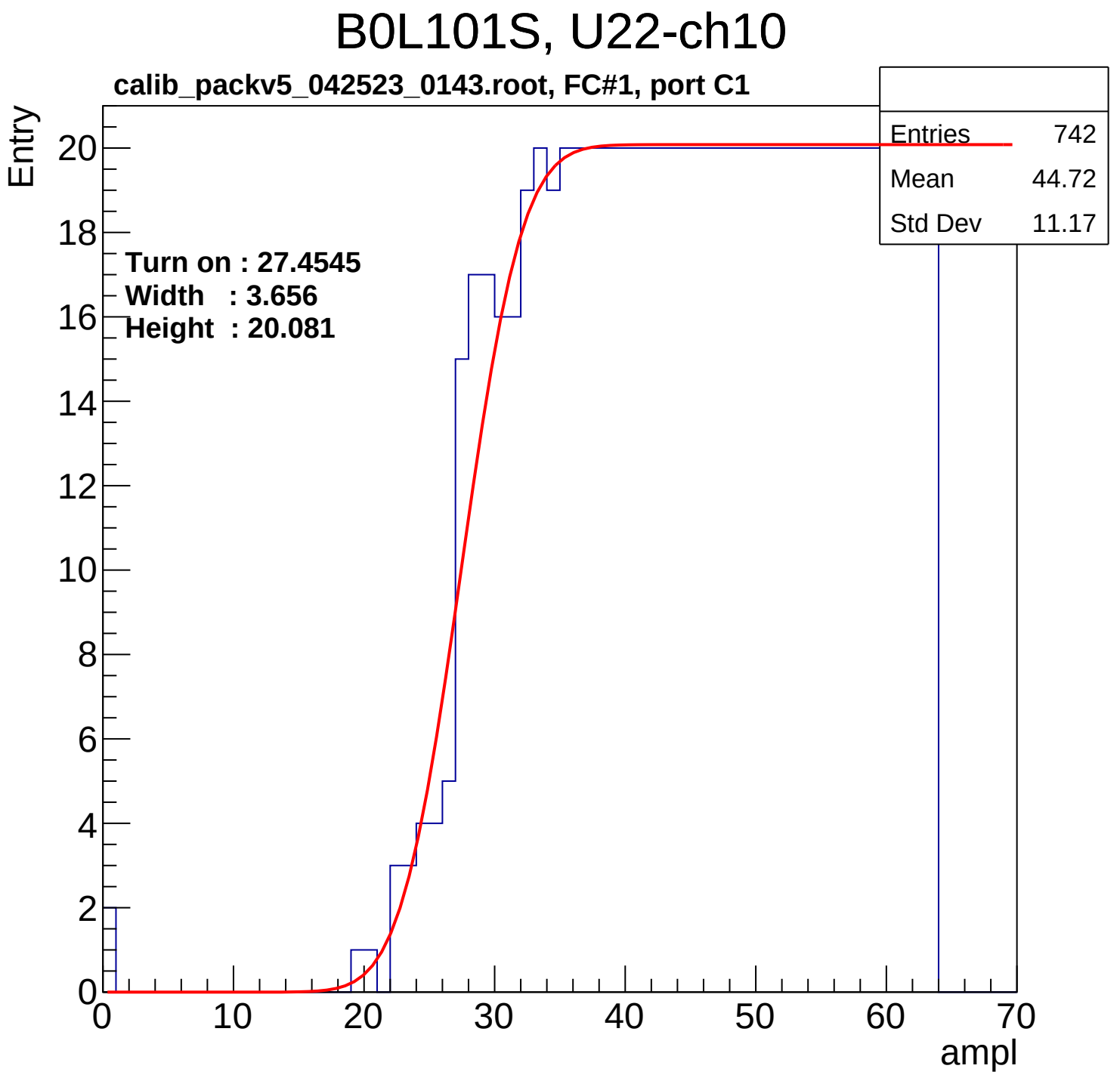

B0L101S, U22-ch5
calib_packv5_042523_0143.root, FC#1, port C1
Entries 750
Mean 44.58
Std Dev 11.18
Turn on : 26.7164
Width : 2.680
Height : 19.980
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

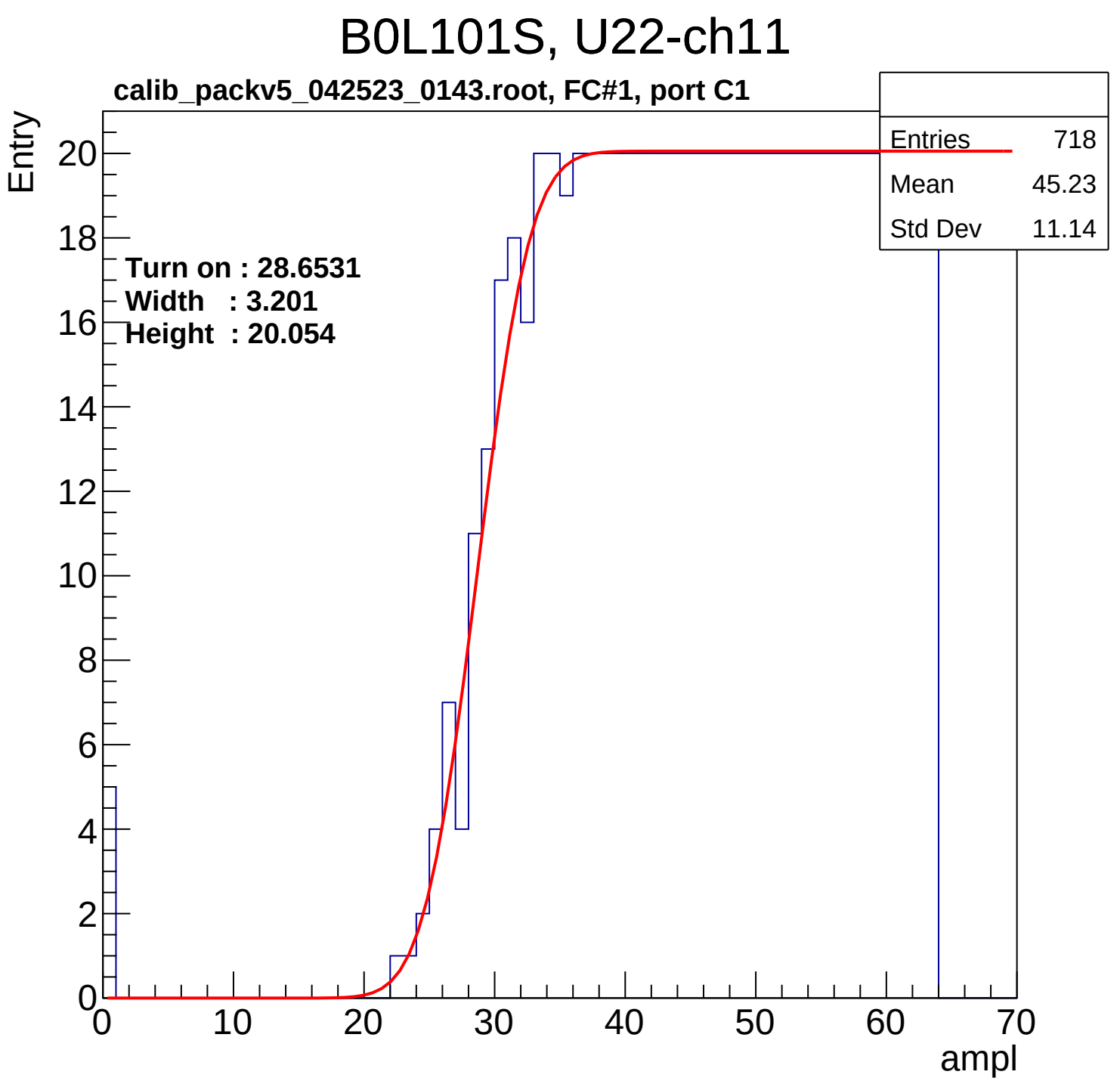

B0L101S, U22-ch6
calib_packv5_042523_0143.root, FC#1, port C1
Entries 729
Mean 45.08
Std Dev 10.93
Turn on : 27.4317
Width : 3.708
Height : 20.053
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

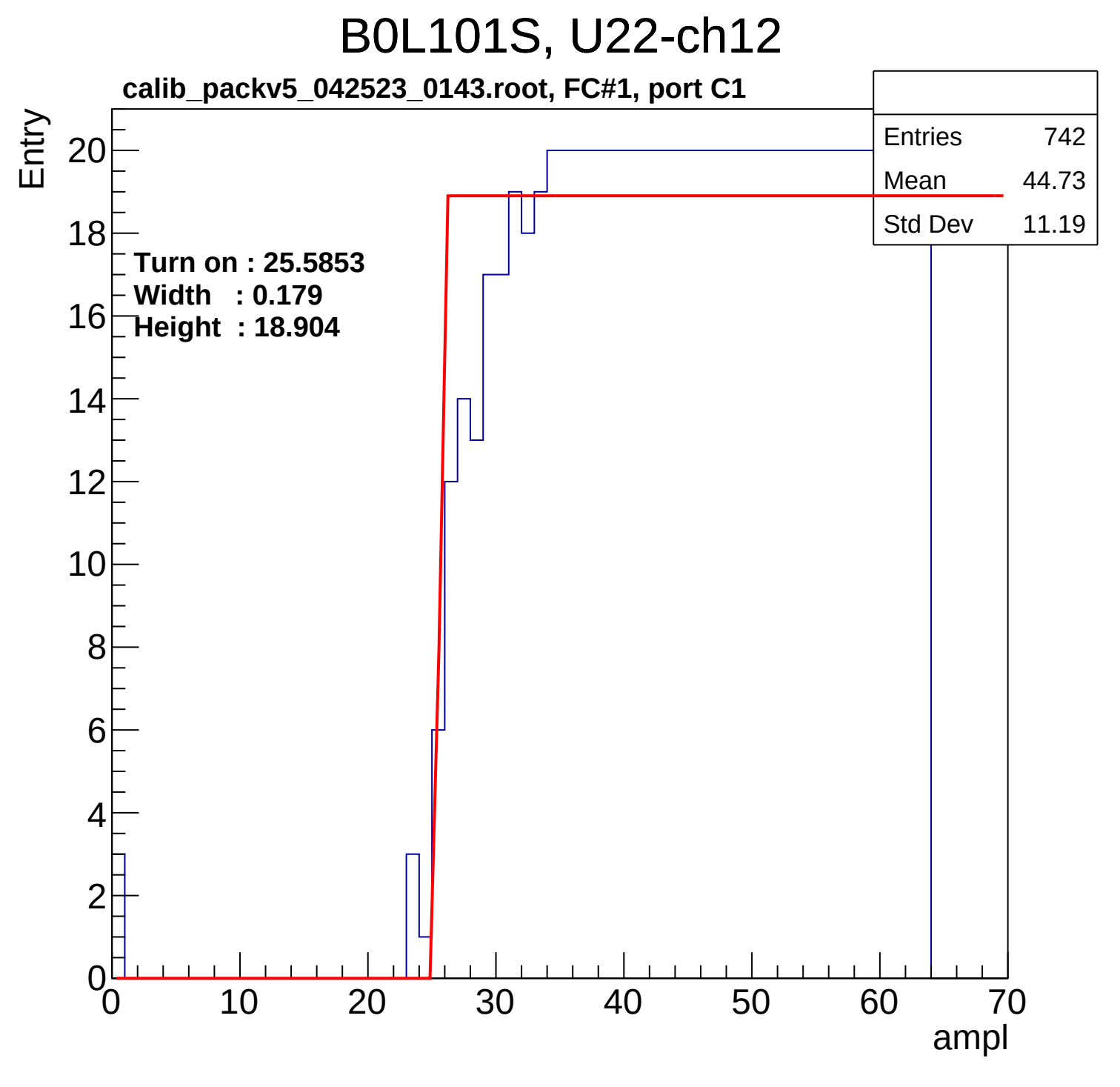

B0L101S, U22-ch7
calib_packv5_042523_0143.root, FC#1, port C1
Entries 727
Mean 45.04
Std Dev 11.21
Turn on : 28.2708
Width : 3.142
Height : 20.145
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

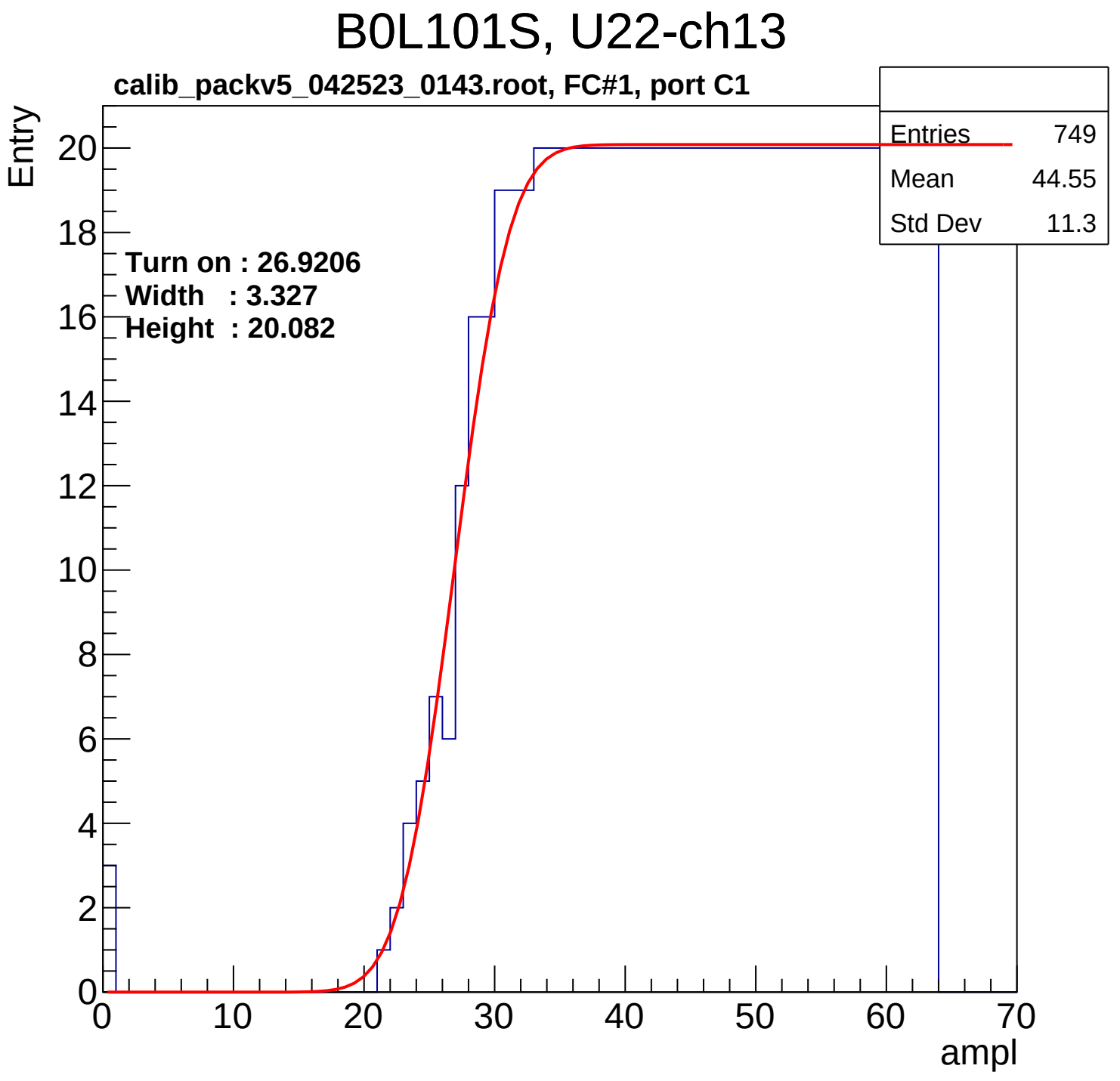

B0L101S, U22-ch8
calib_packv5_042523_0143.root, FC#1, port C1
Entries 782
Mean 43.59
Std Dev 12.12
Turn on : 25.2747
Width : 2.715
Height : 19.937
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

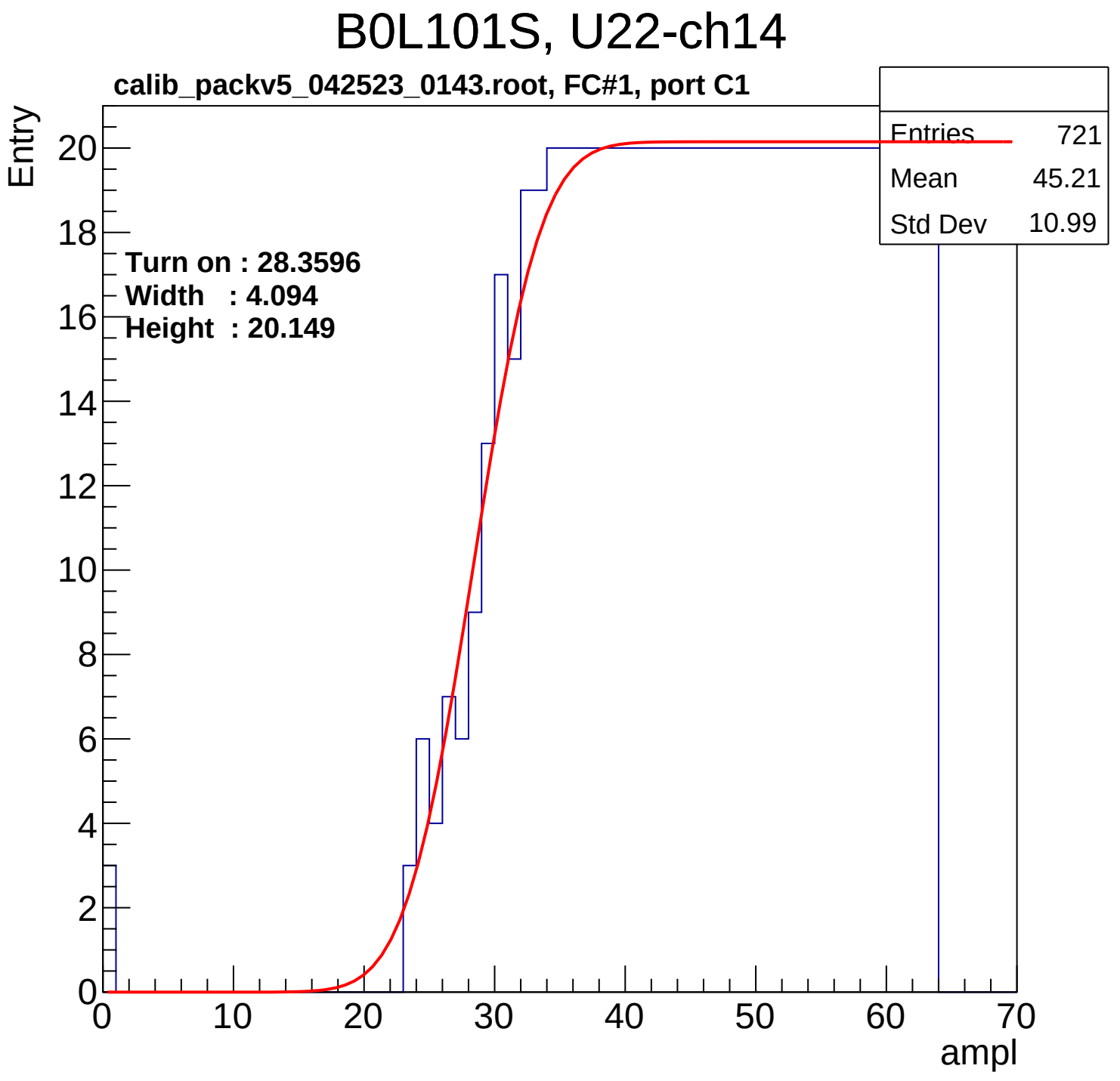

B0L101S, U22-ch9
calib_packv5_042523_0143.root, FC#1, port C1
Entries 726
Mean 45.19
Std Dev 10.83
Turn on : 27.7721
Width : 2.334
Height : 19.968
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

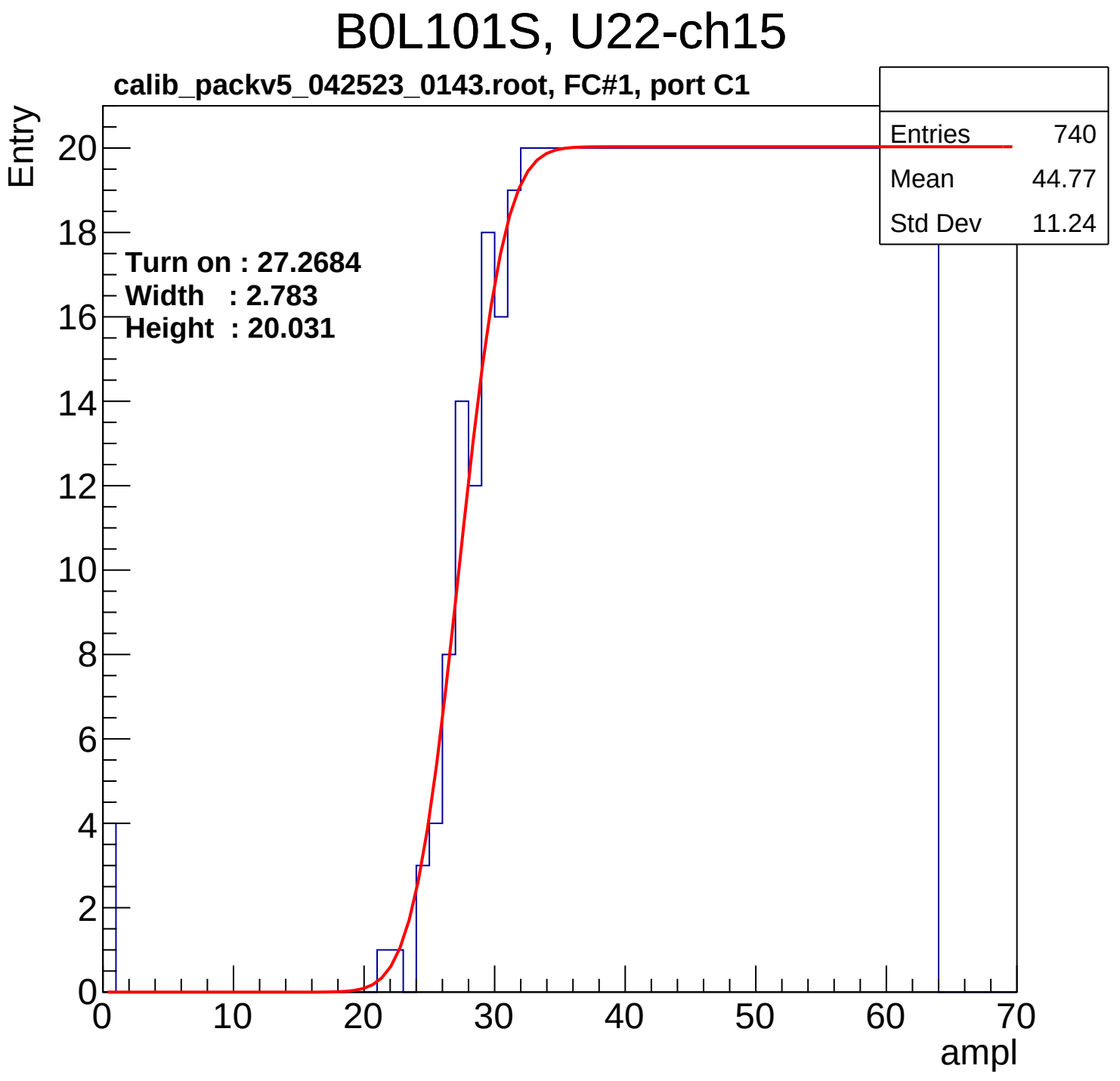

B0L101S, U22-ch10
calib_packv5_042523_0143.root, FC#1, port C1
Entries 742
Mean 44.72
Std Dev 11.17
Turn on : 27.4545
Width : 3.656
Height : 20.081
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

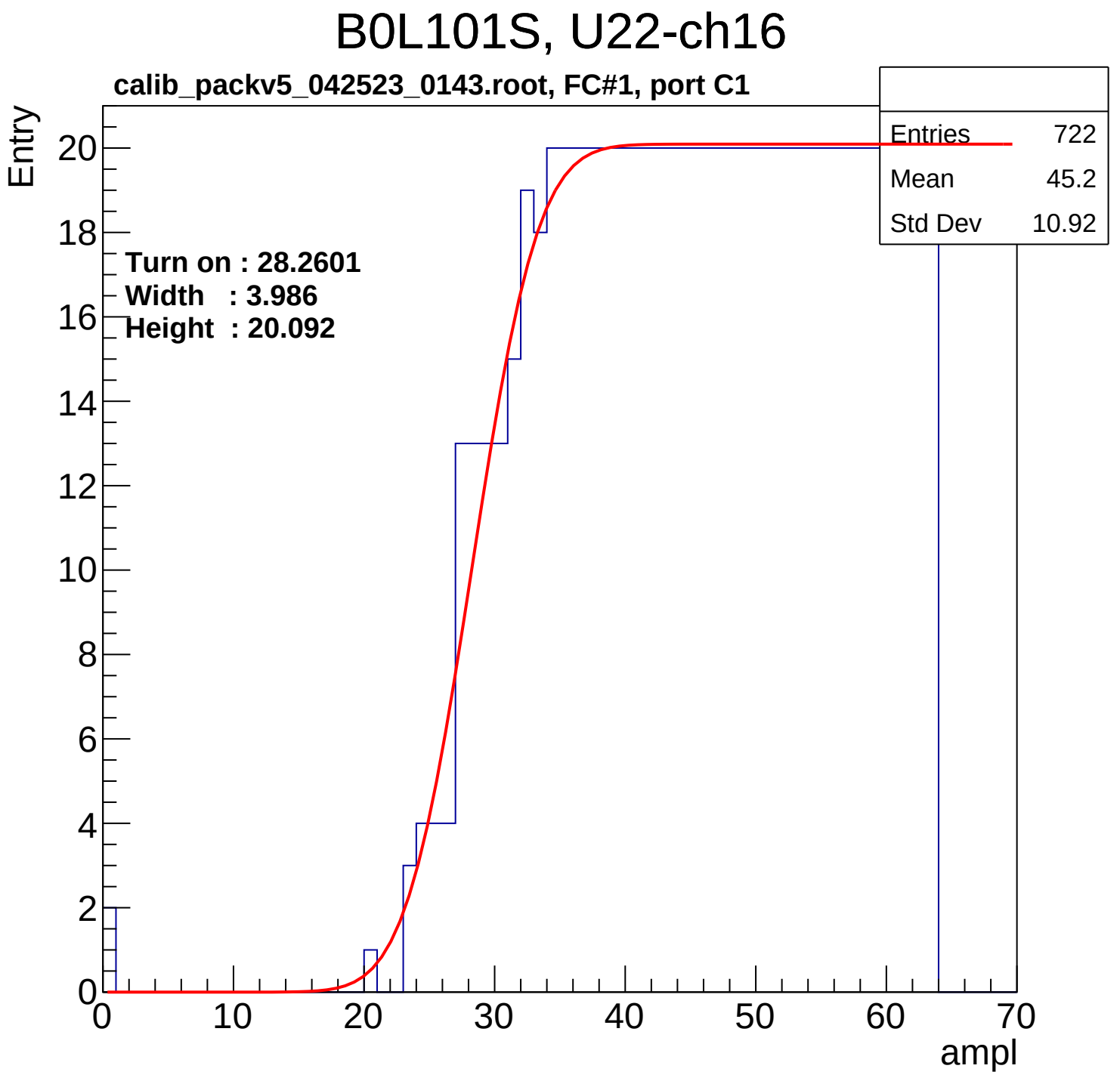

B0L101S, U22-ch11
calib_packv5_042523_0143.root, FC#1, port C1
Entries 718
Mean 45.23
Std Dev 11.14
Turn on : 28.6531
Width : 3.201
Height : 20.054
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

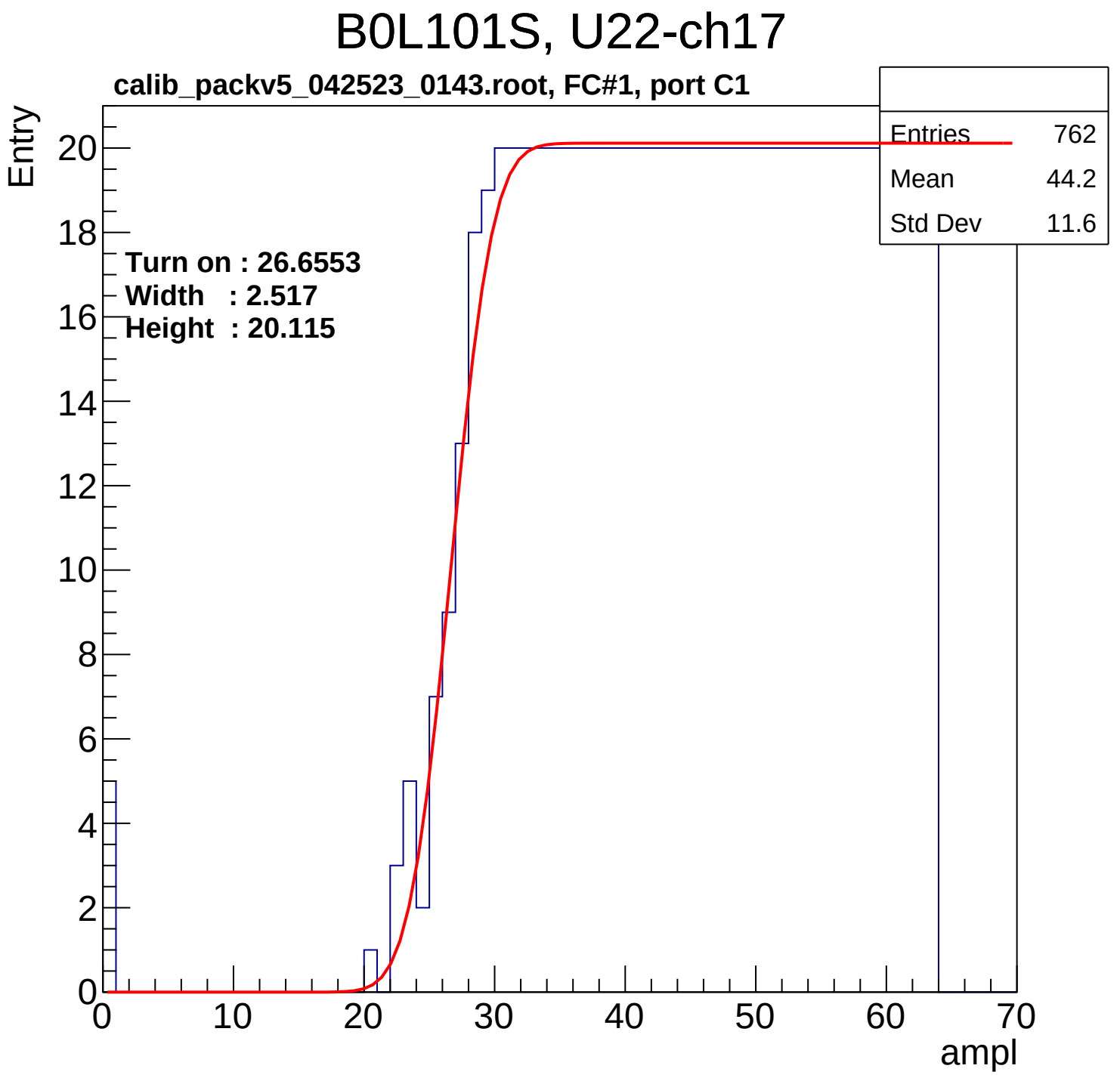

B0L101S, U22-ch12
calib_packv5_042523_0143.root, FC#1, port C1
Entries 742
Mean 44.73
Std Dev 11.19
Turn on : 25.5853
Width : 0.179
Height : 18.904
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

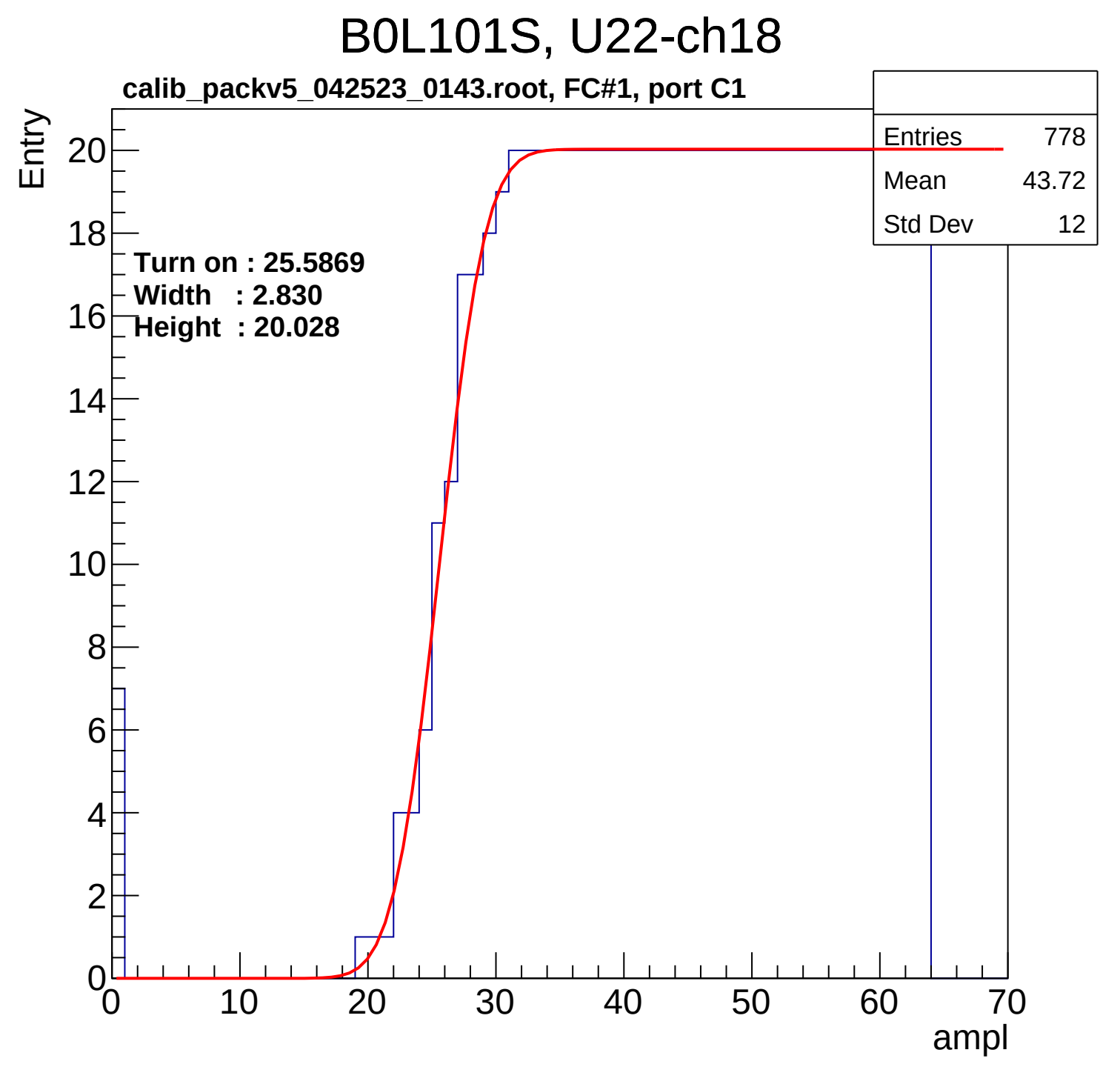

B0L101S, U22-ch13
calib_packv5_042523_0143.root, FC#1, port C1
Entries 749
Mean 44.55
Std Dev 11.3
Turn on : 26.9206
Width : 3.327
Height : 20.082
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

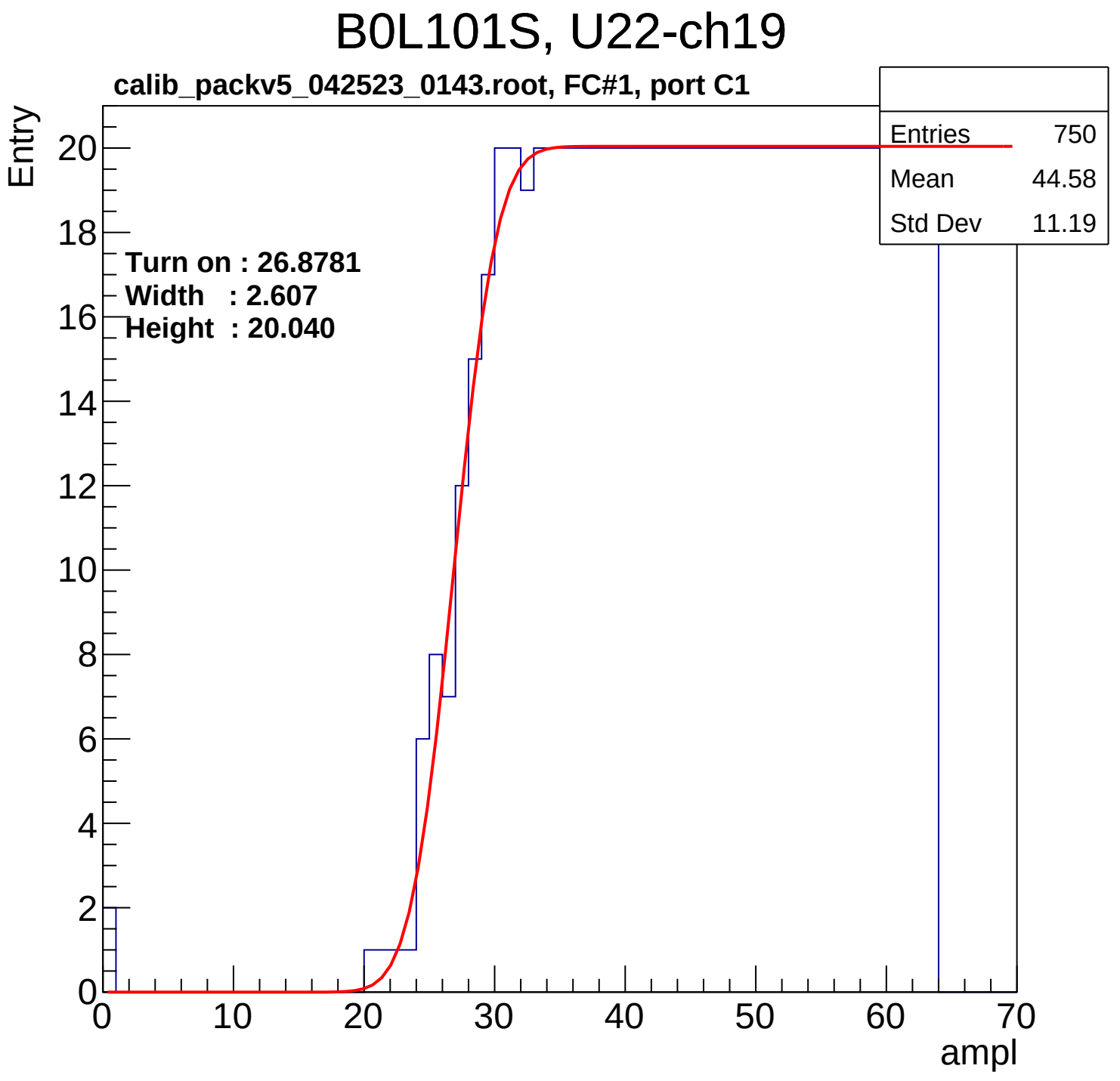

B0L101S, U22-ch14
calib_packv5_042523_0143.root, FC#1, port C1
Entries 721
Mean 45.21
Std Dev 10.99
Turn on : 28.3596
Width : 4.094
Height : 20.149
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

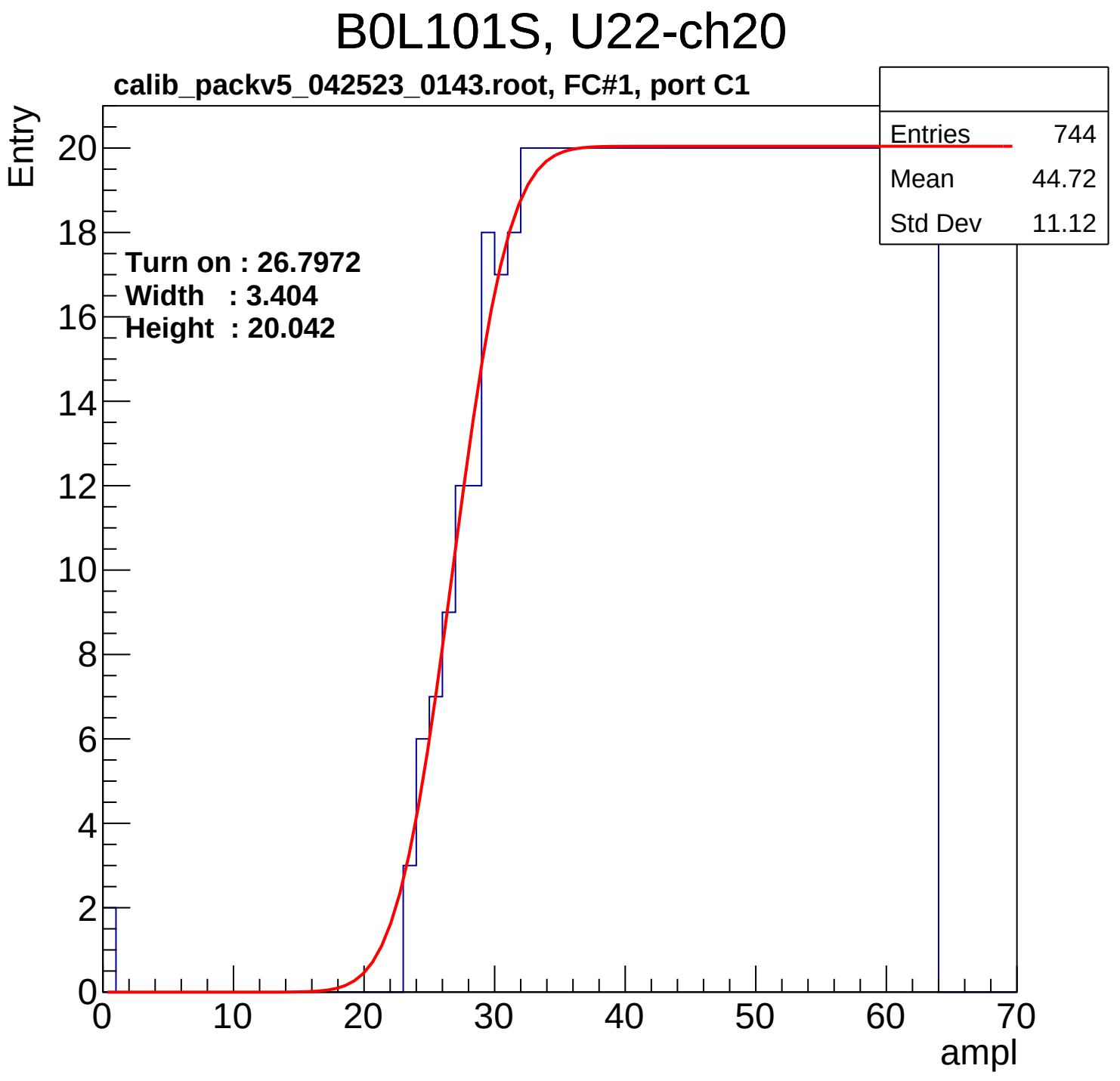

B0L101S, U22-ch15
calib_packv5_042523_0143.root, FC#1, port C1
Entries 740
Mean 44.77
Std Dev 11.24
Turn on : 27.2684
Width : 2.783
Height : 20.031
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

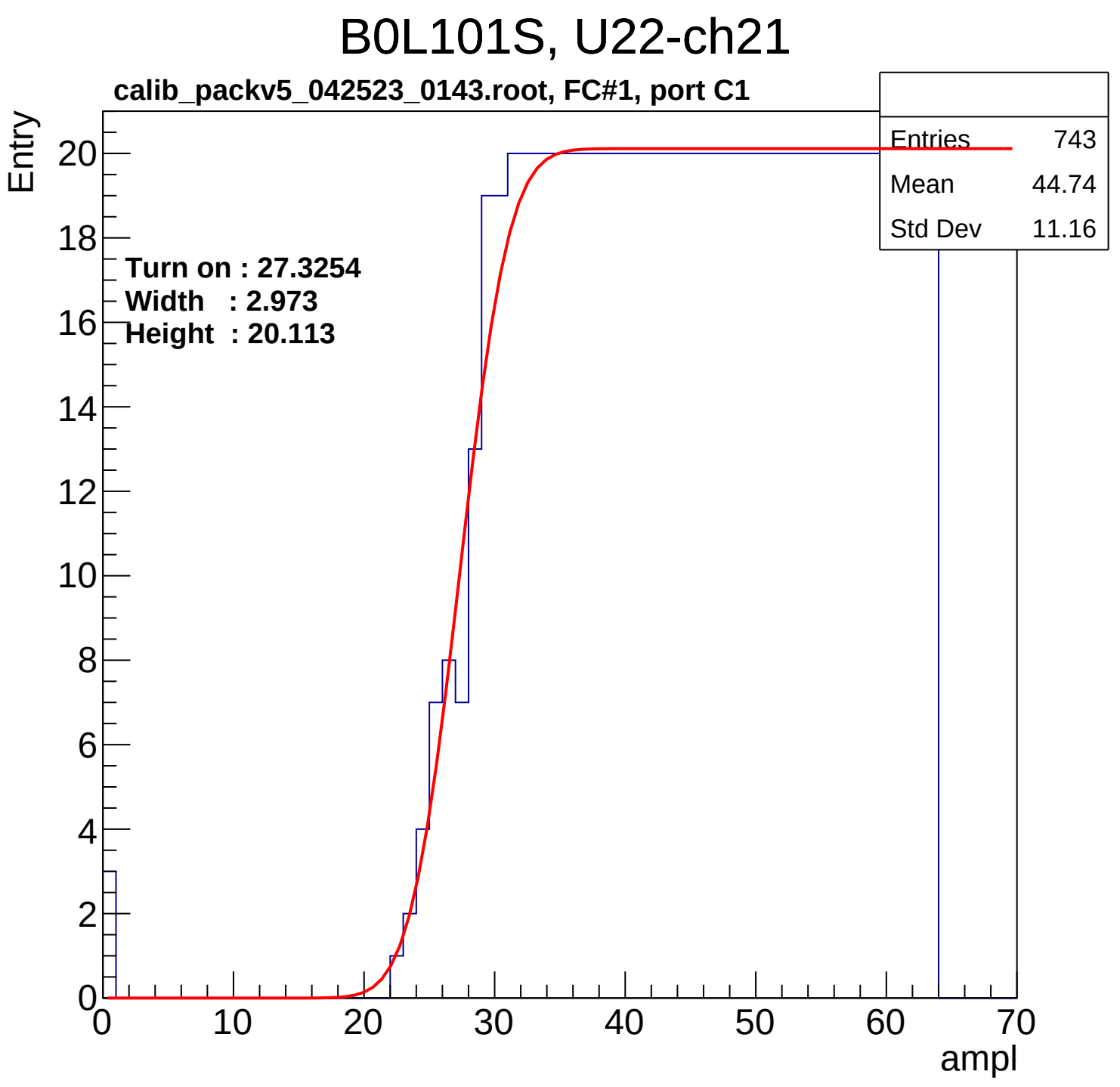

B0L101S, U22-ch16
calib_packv5_042523_0143.root, FC#1, port C1
Entries 722
Mean 45.2
Std Dev 10.92
Turn on : 28.2601
Width : 3.986
Height : 20.092
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

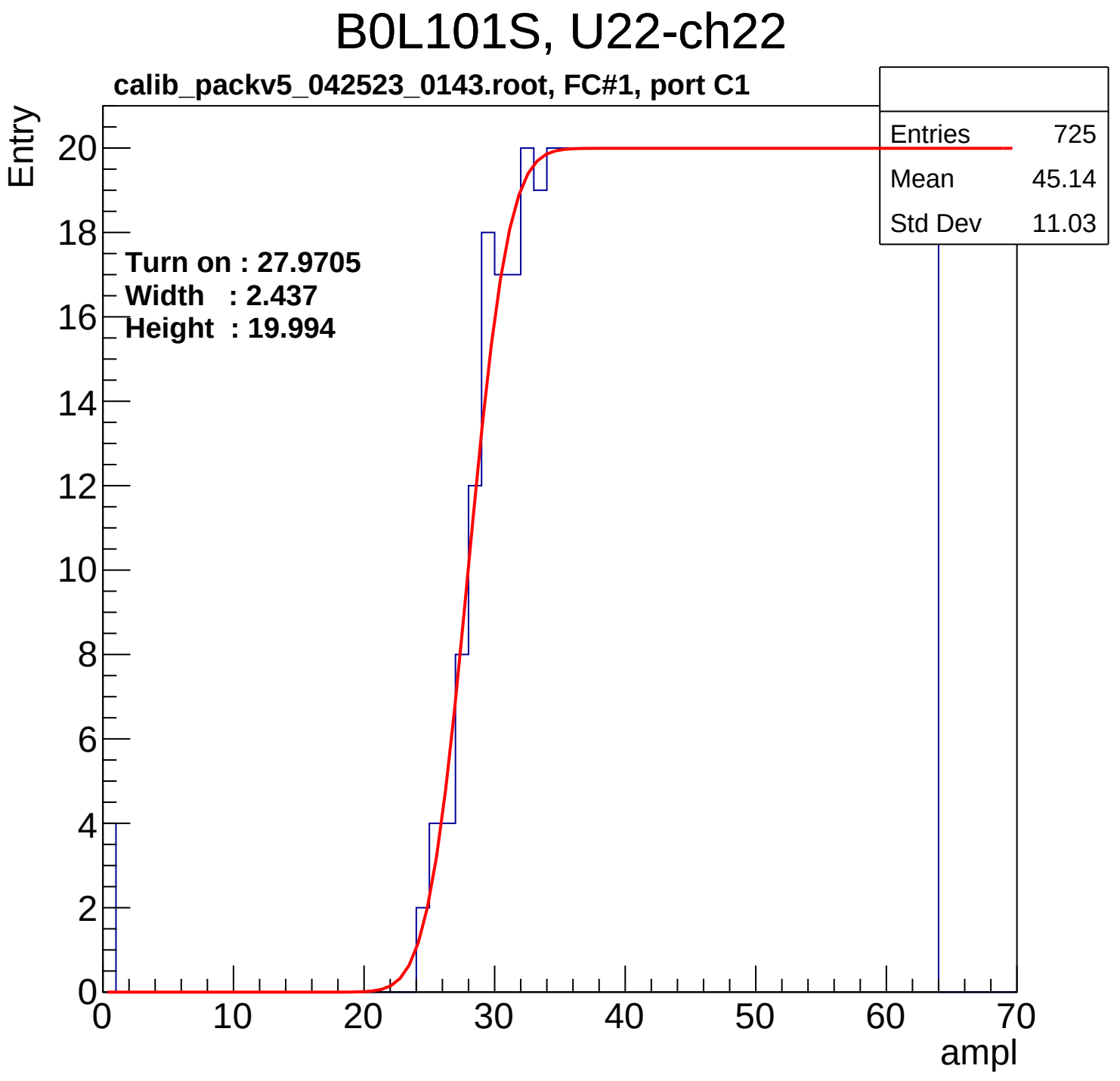

B0L101S, U22-ch17
calib_packv5_042523_0143.root, FC#1, port C1
Entries 762
Mean 44.2
Std Dev 11.6
Turn on : 26.6553
Width : 2.517
Height : 20.115
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

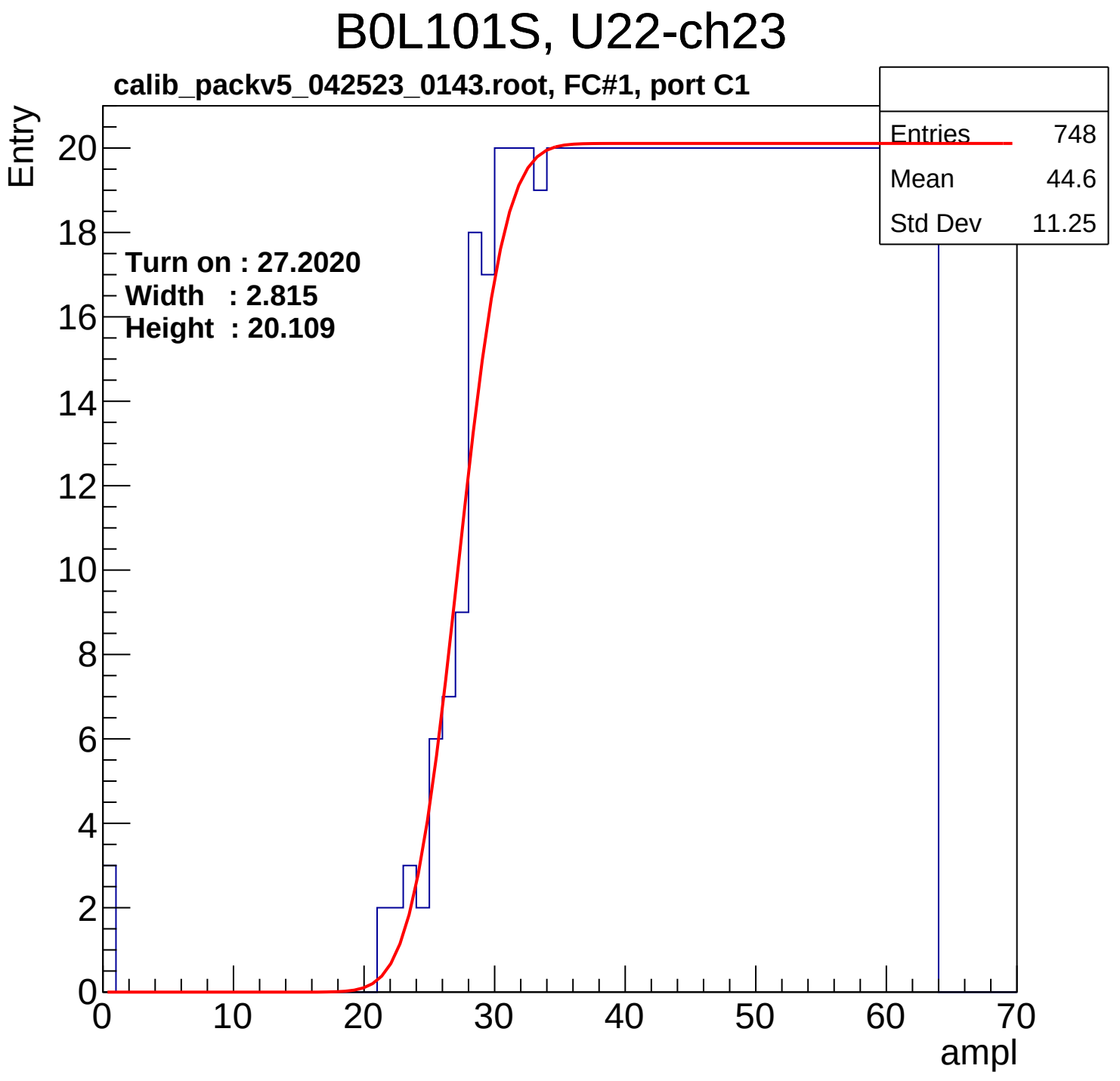

B0L101S, U22-ch18
calib_packv5_042523_0143.root, FC#1, port C1
Entries 778
Mean 43.72
Std Dev 12
Turn on : 25.5869
Width : 2.830
Height : 20.028
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

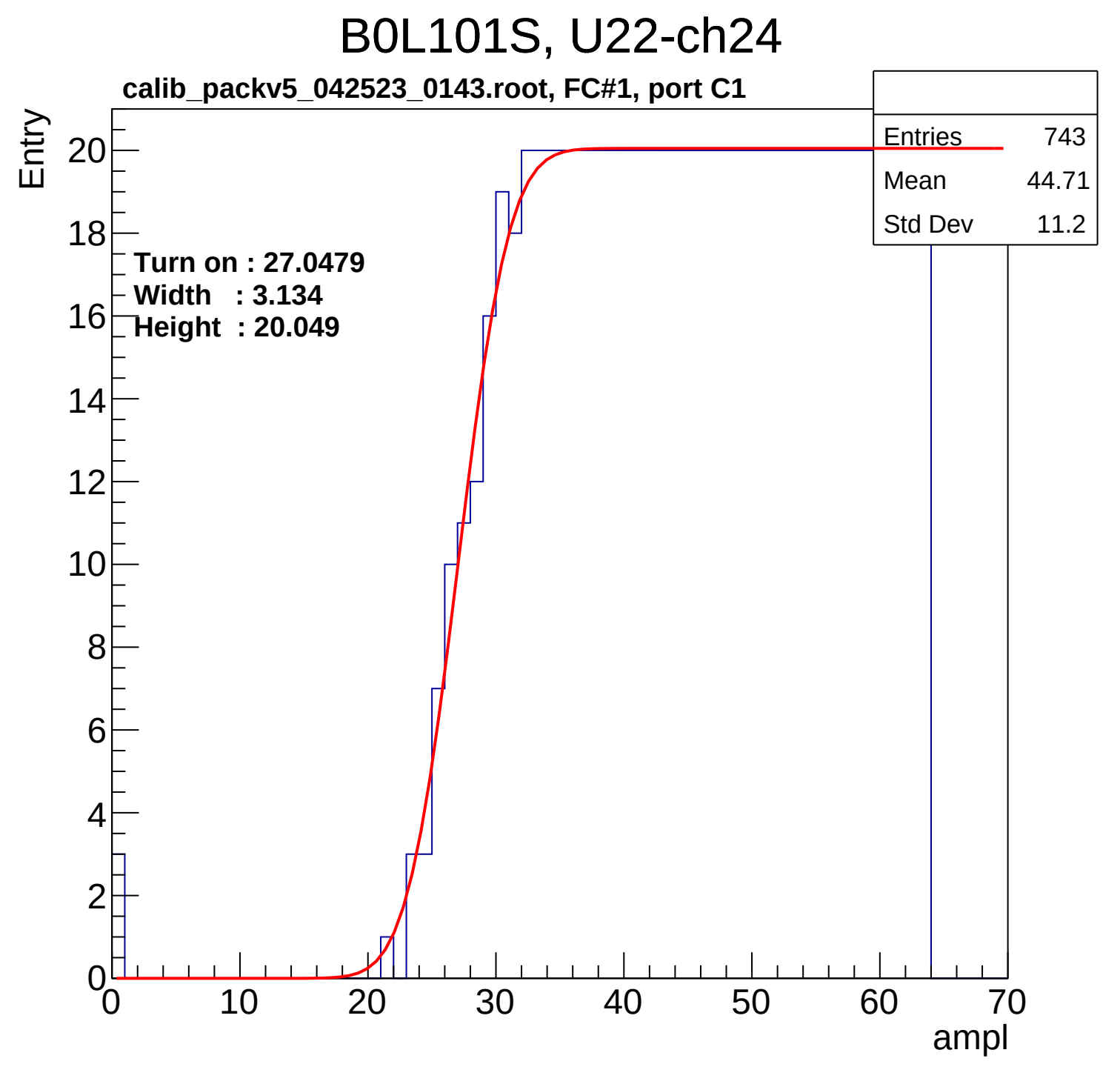

B0L101S, U22-ch19
calib_packv5_042523_0143.root, FC#1, port C1
Entries 750
Mean 44.58
Std Dev 11.19
Turn on : 26.8781
Width : 2.607
Height : 20.040
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

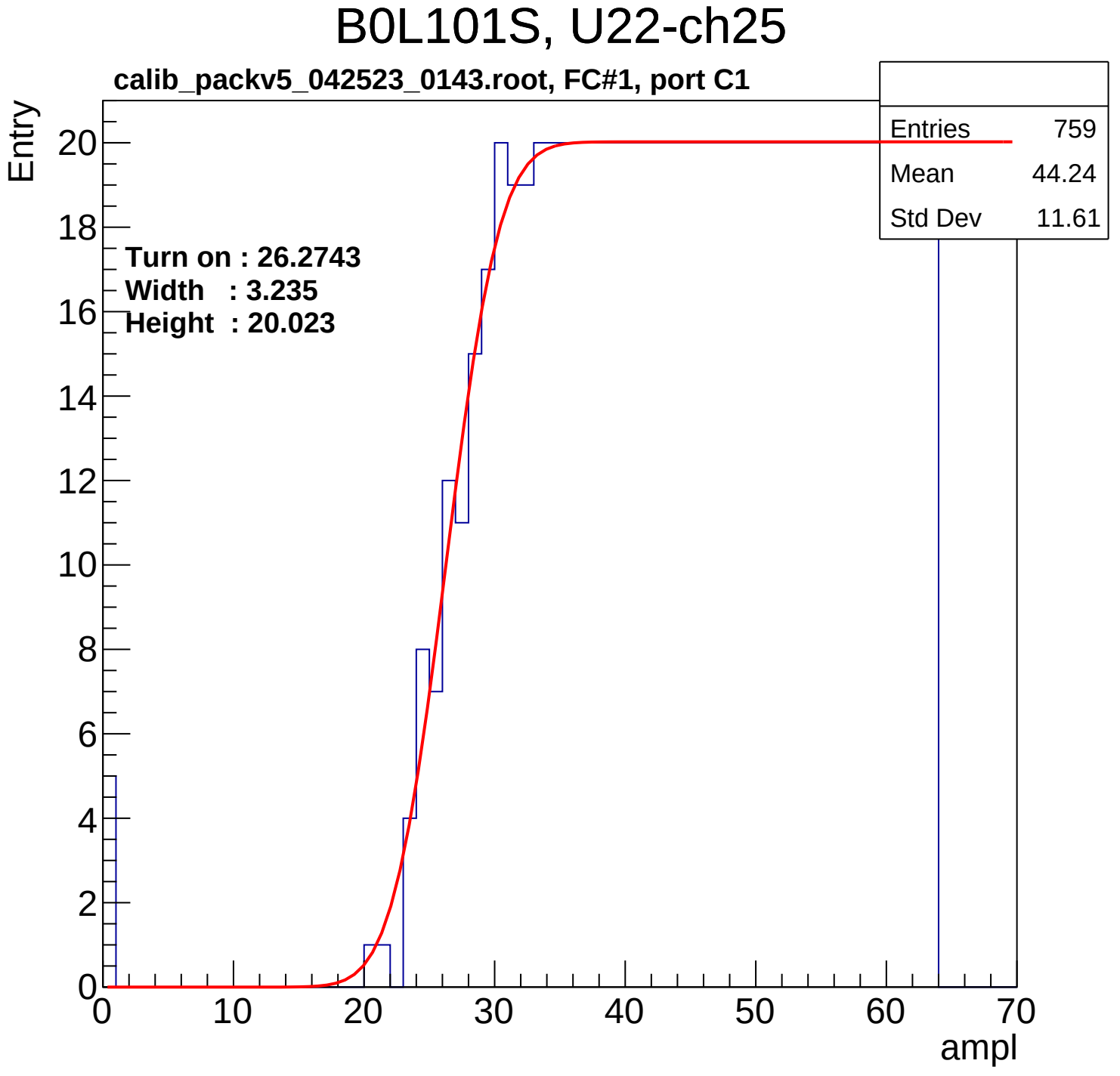

B0L101S, U22-ch20
calib_packv5_042523_0143.root, FC#1, port C1
Entries 744
Mean 44.72
Std Dev 11.12
Turn on : 26.7972
Width : 3.404
Height : 20.042
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

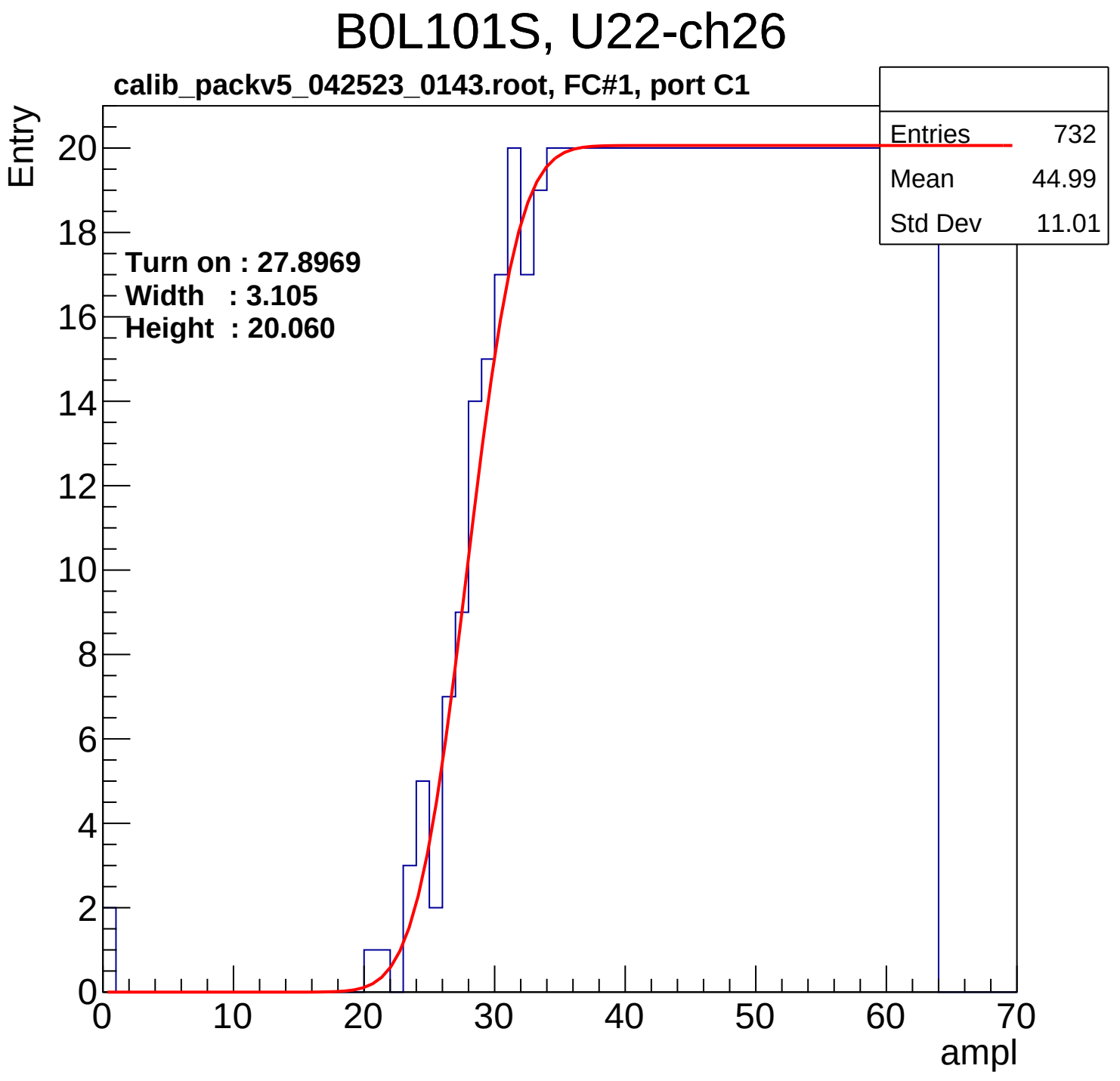

B0L101S, U22-ch21
calib_packv5_042523_0143.root, FC#1, port C1
Entries 743
Mean 44.74
Std Dev 11.16
Turn on : 27.3254
Width : 2.973
Height : 20.113
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

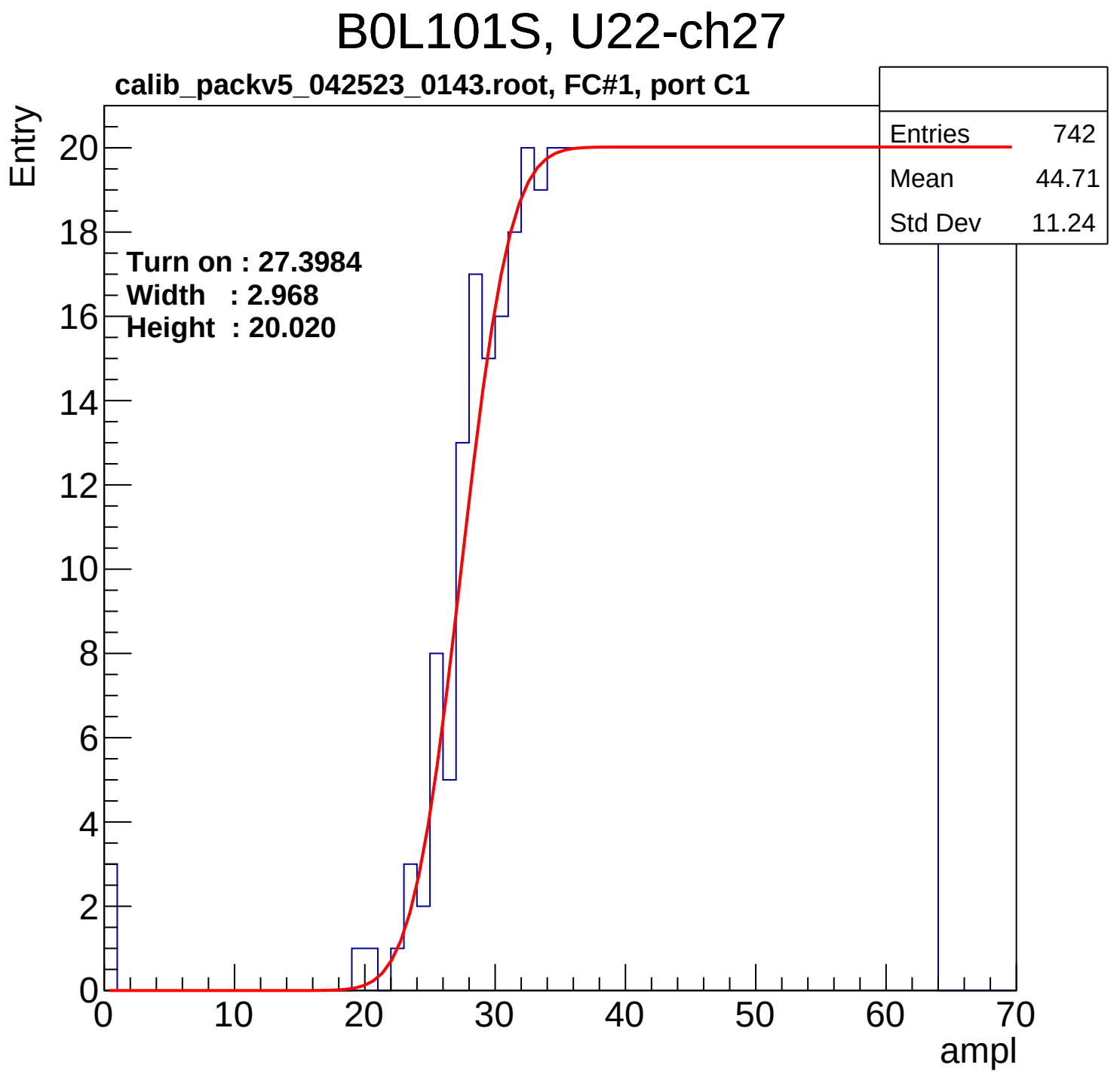

B0L101S, U22-ch22
calib_packv5_042523_0143.root, FC#1, port C1
Entries 725
Mean 45.14
Std Dev 11.03
Turn on : 27.9705
Width : 2.437
Height : 19.994
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

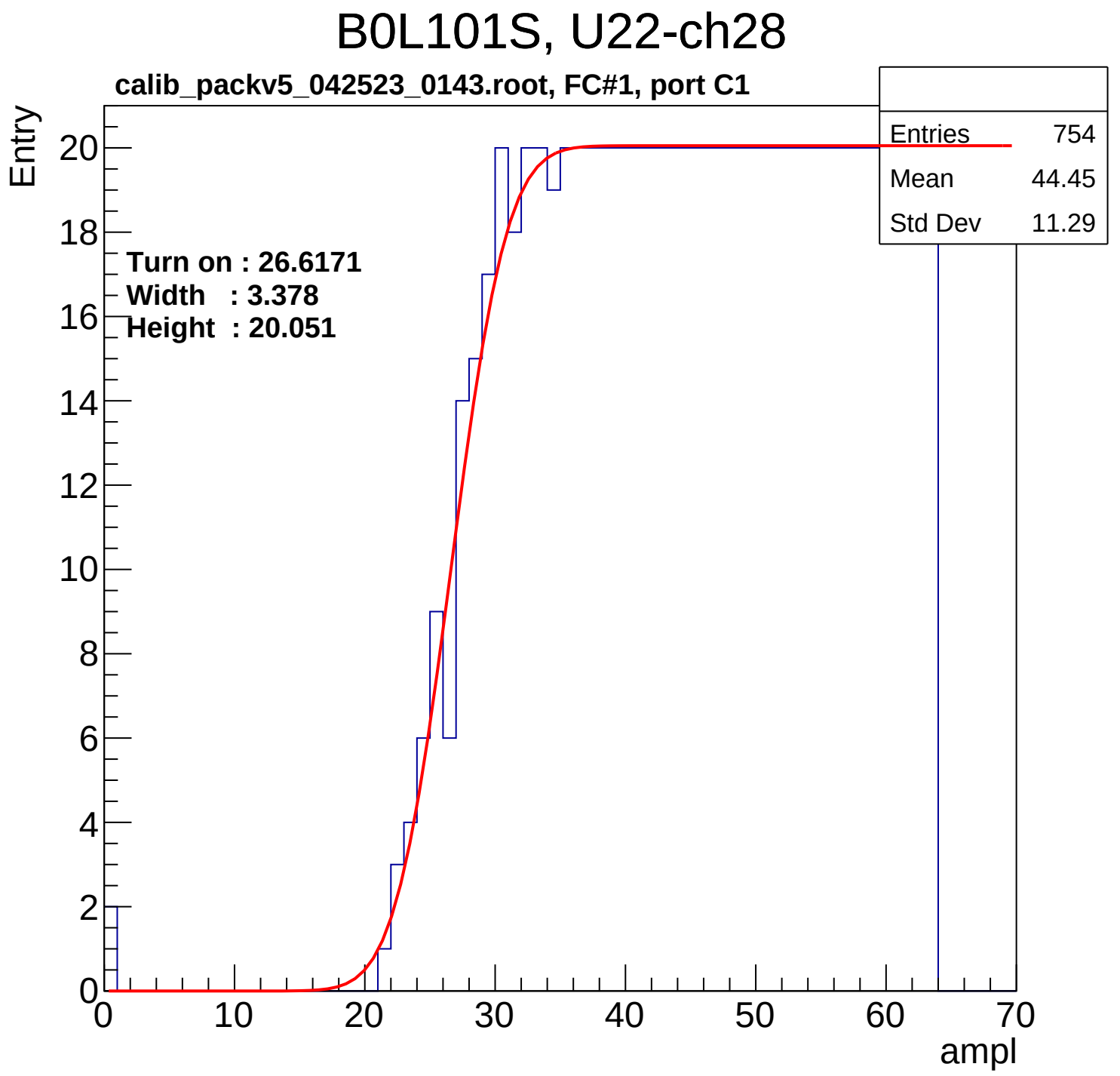

B0L101S, U22-ch23
calib_packv5_042523_0143.root, FC#1, port C1
Entries 748
Mean 44.6
Std Dev 11.25
Turn on : 27.2020
Width : 2.815
Height : 20.109
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

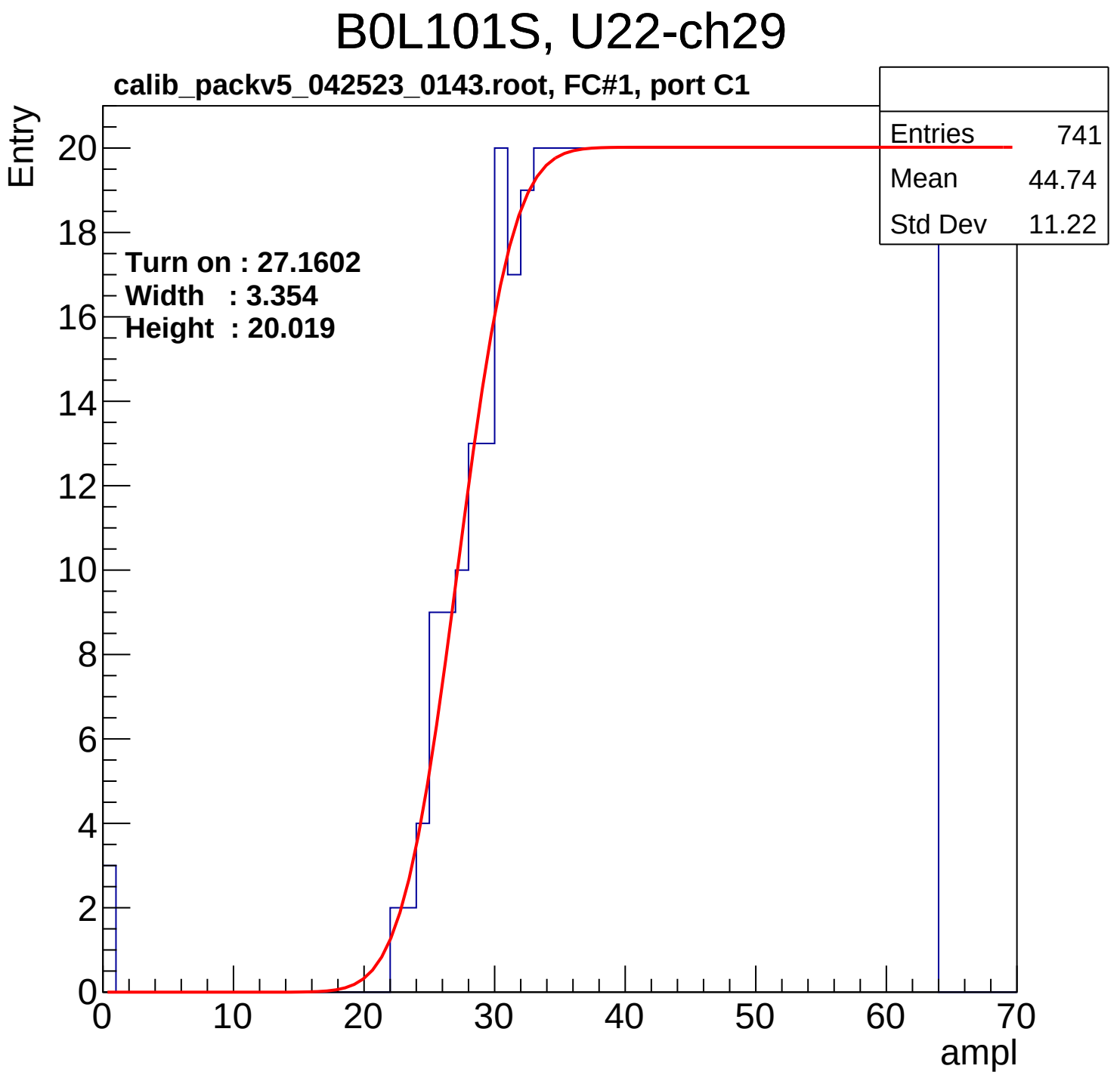

B0L101S, U22-ch24
calib_packv5_042523_0143.root, FC#1, port C1
Entries 743
Mean 44.71
Std Dev 11.2
Turn on : 27.0479
Width : 3.134
Height : 20.049
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

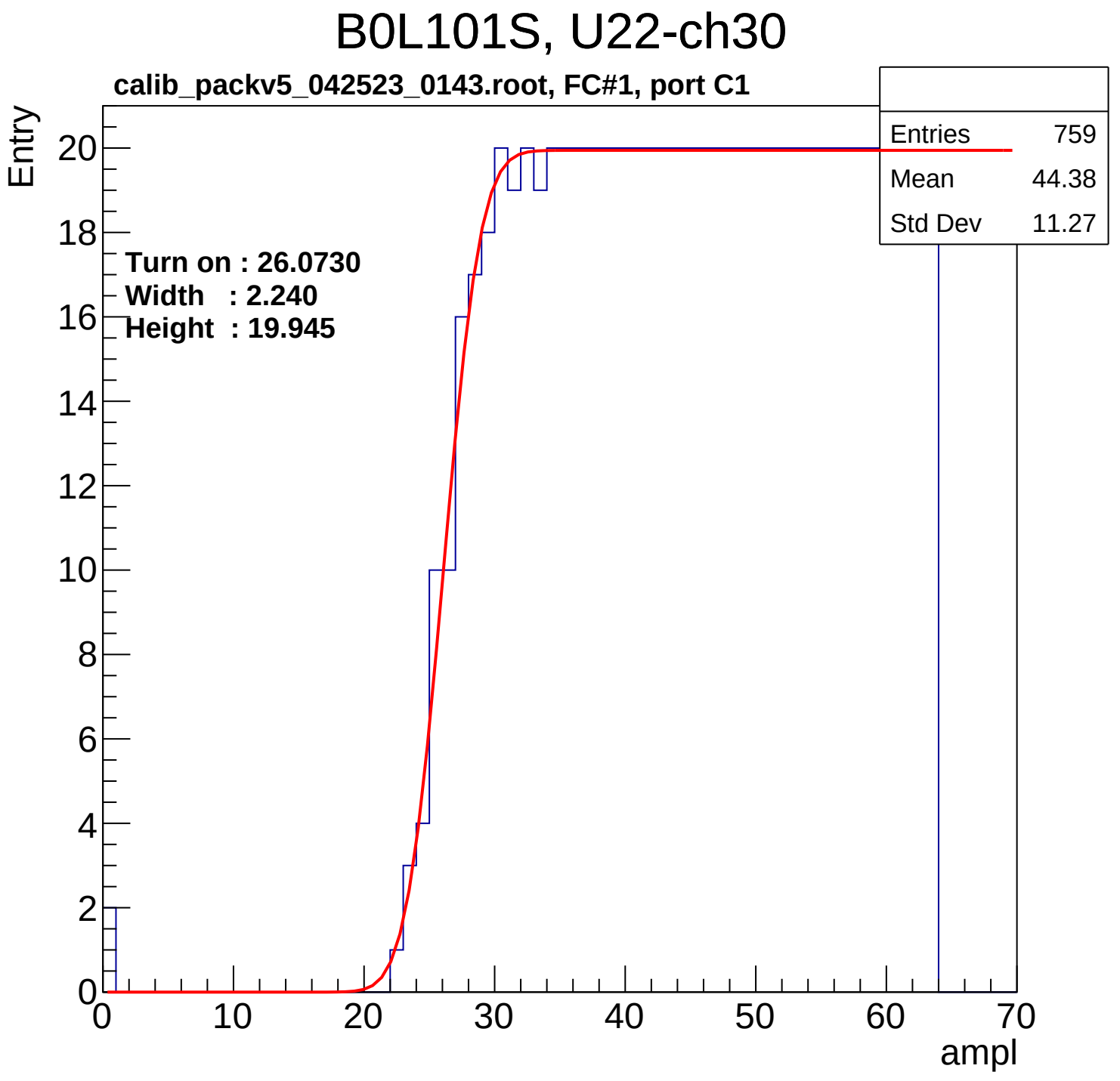

B0L101S, U22-ch25
calib_packv5_042523_0143.root, FC#1, port C1
Entries 759
Mean 44.24
Std Dev 11.61
Turn on : 26.2743
Width : 3.235
Height : 20.023
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

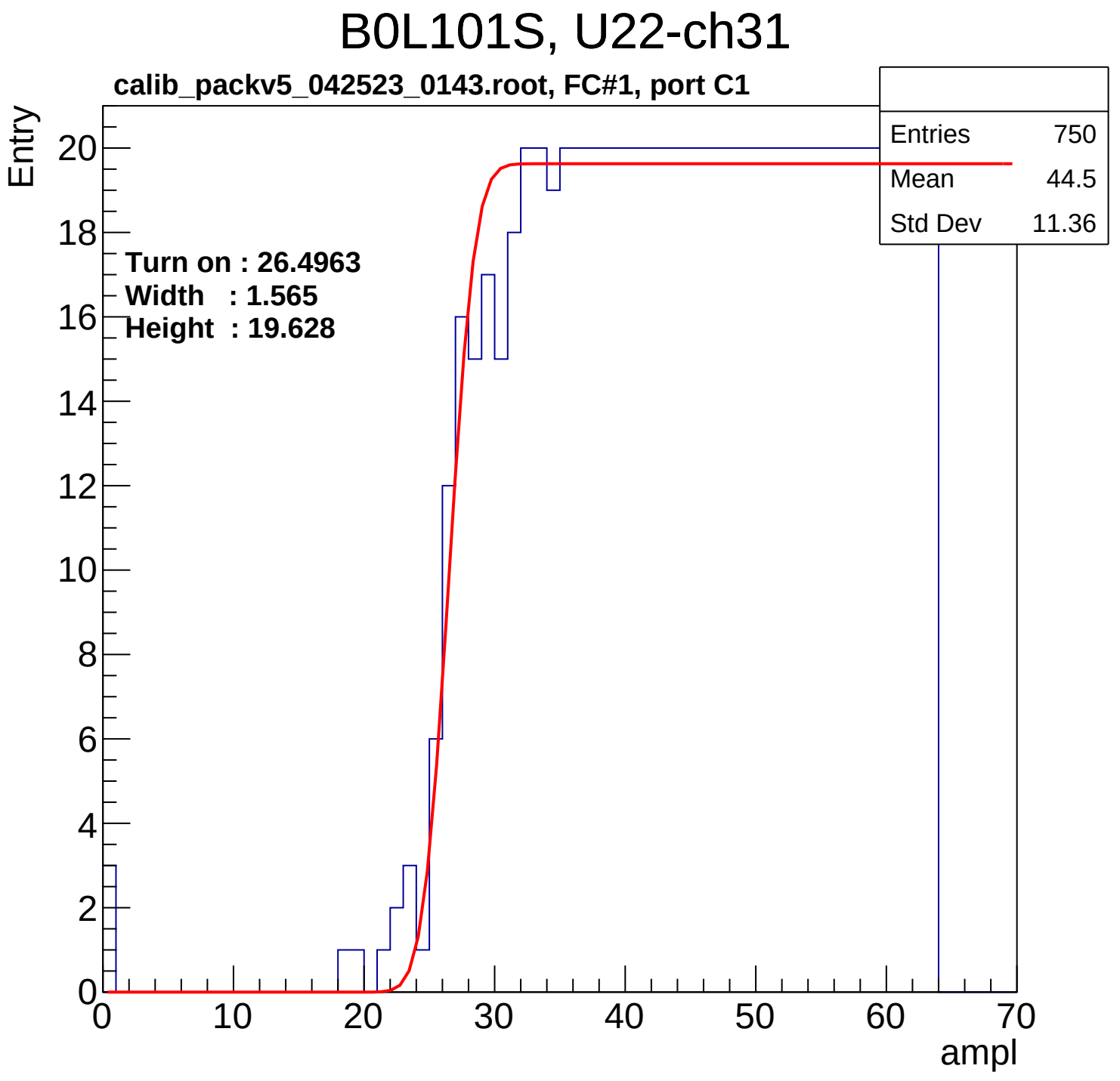

B0L101S, U22-ch26
calib_packv5_042523_0143.root, FC#1, port C1
Entries 732
Mean 44.99
Std Dev 11.01
Turn on : 27.8969
Width : 3.105
Height : 20.060
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

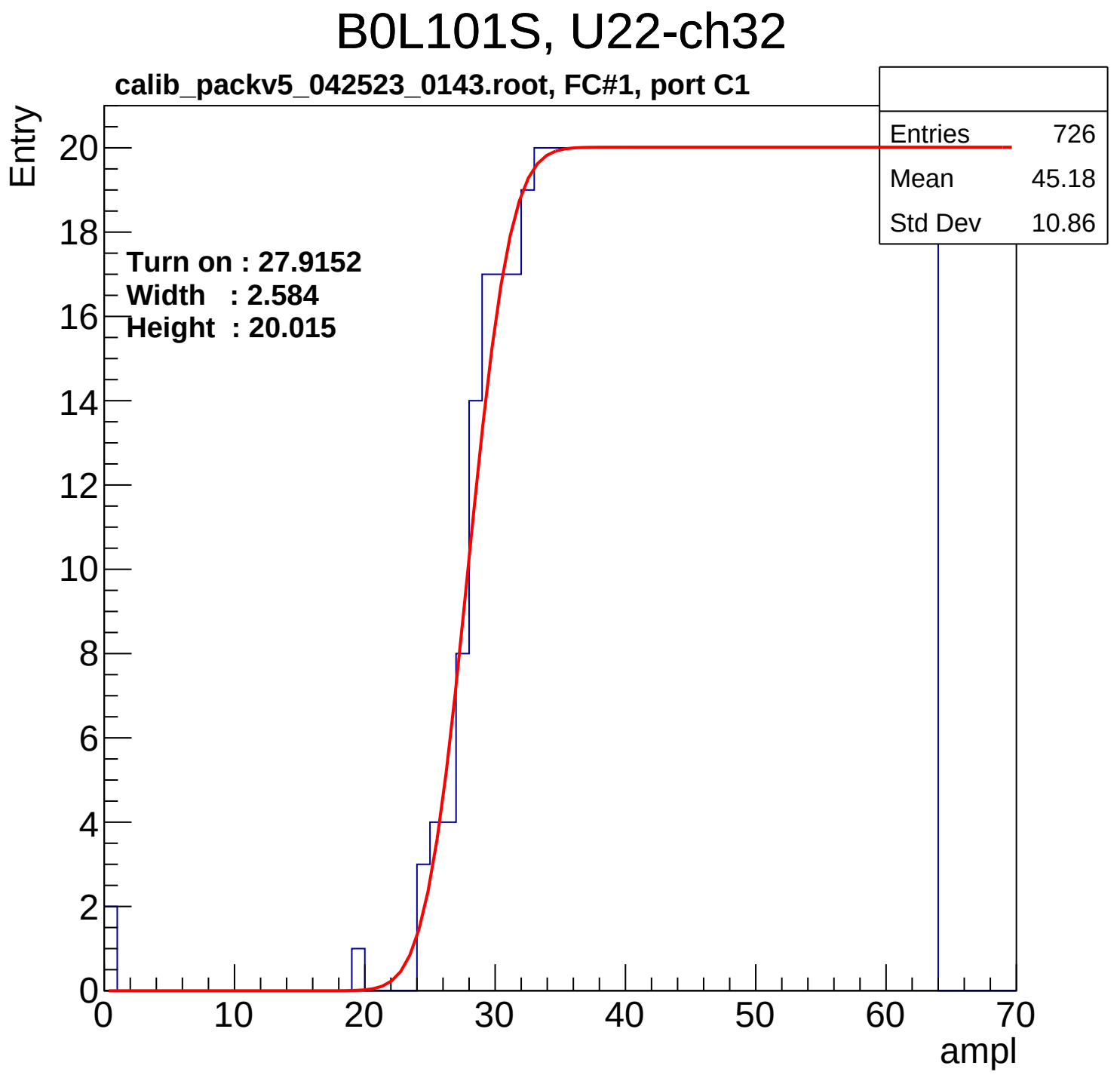

B0L101S, U22-ch27
calib_packv5_042523_0143.root, FC#1, port C1
Entries 742
Mean 44.71
Std Dev 11.24
Turn on : 27.3984
Width : 2.968
Height : 20.020
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

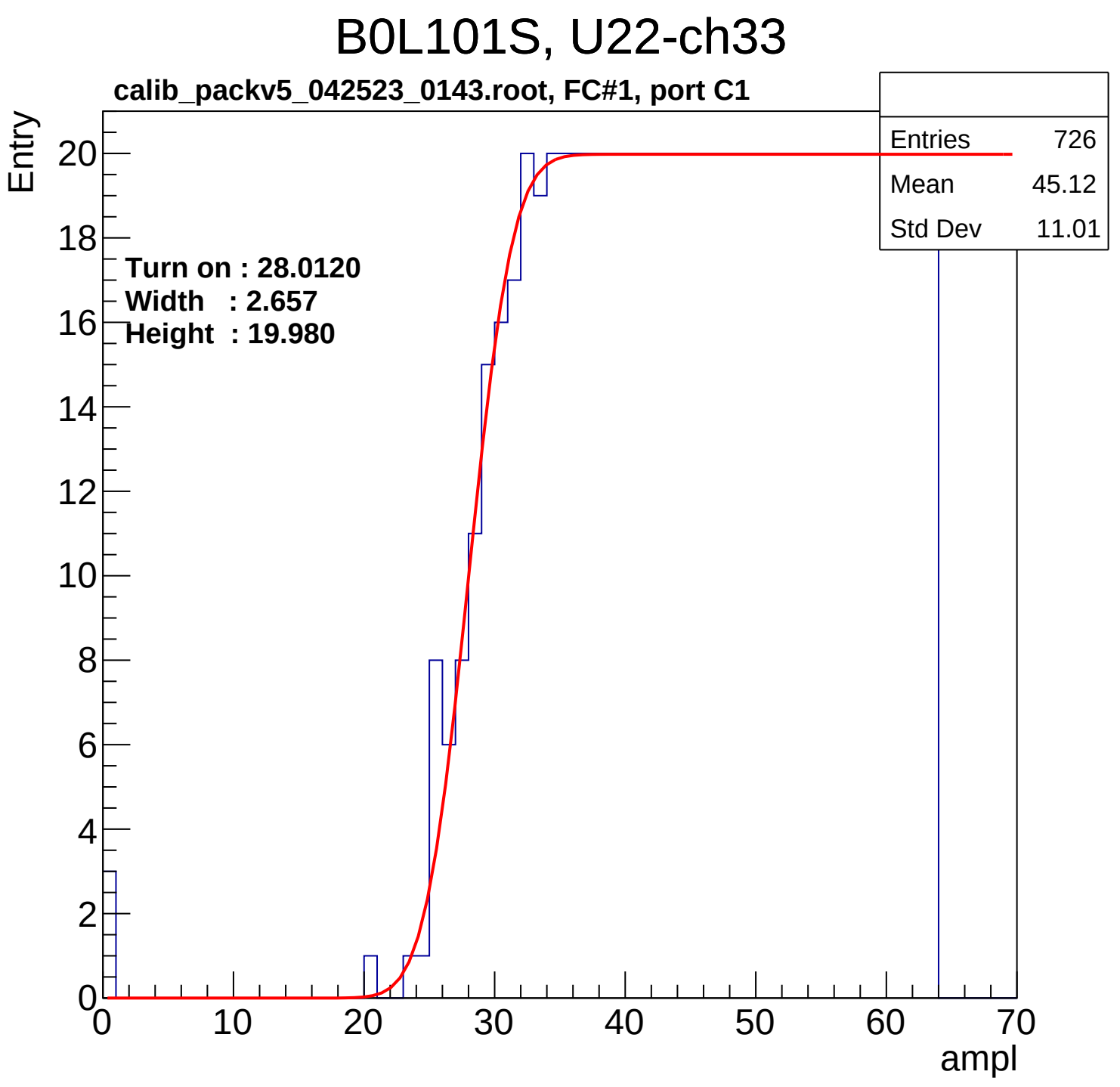

B0L101S, U22-ch28
calib_packv5_042523_0143.root, FC#1, port C1
Entries 754
Mean 44.45
Std Dev 11.29
Turn on : 26.6171
Width : 3.378
Height : 20.051
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

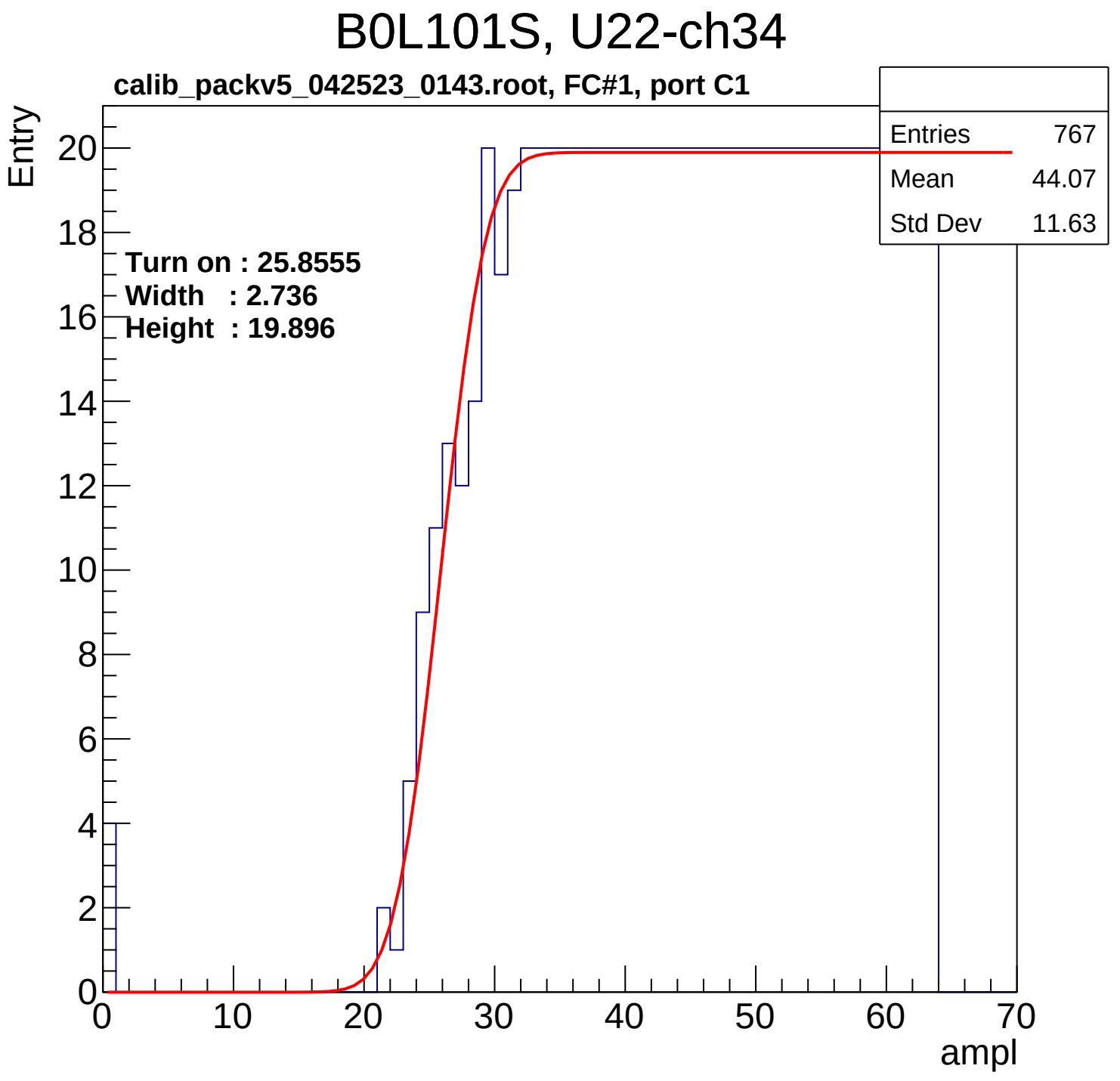

B0L101S, U22-ch29
calib_packv5_042523_0143.root, FC#1, port C1
Entries 741
Mean 44.74
Std Dev 11.22
Turn on : 27.1602
Width : 3.354
Height : 20.019
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

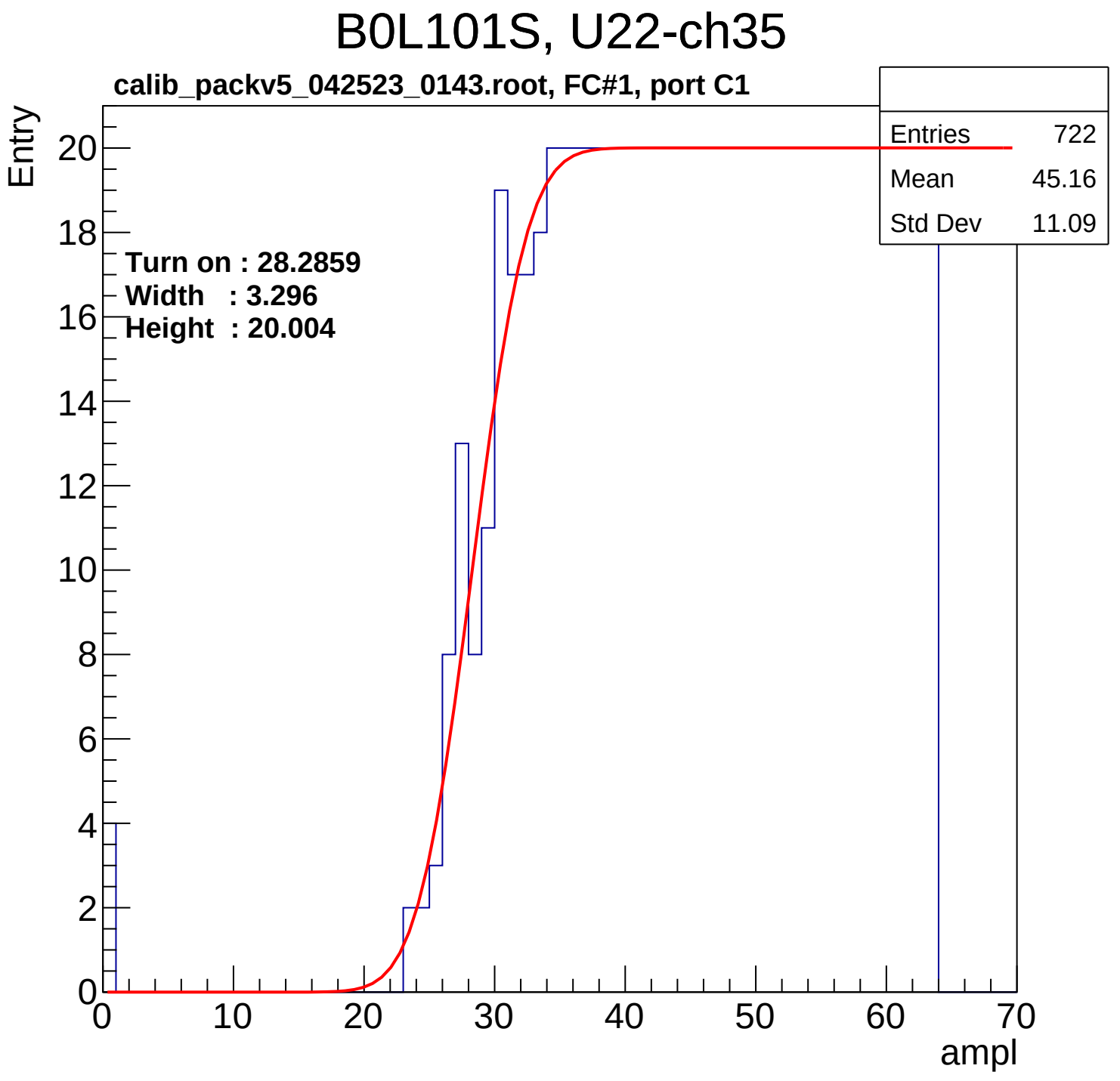

B0L101S, U22-ch30
calib_packv5_042523_0143.root, FC#1, port C1
Entries 759
Mean 44.38
Std Dev 11.27
Turn on : 26.0730
Width : 2.240
Height : 19.945
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

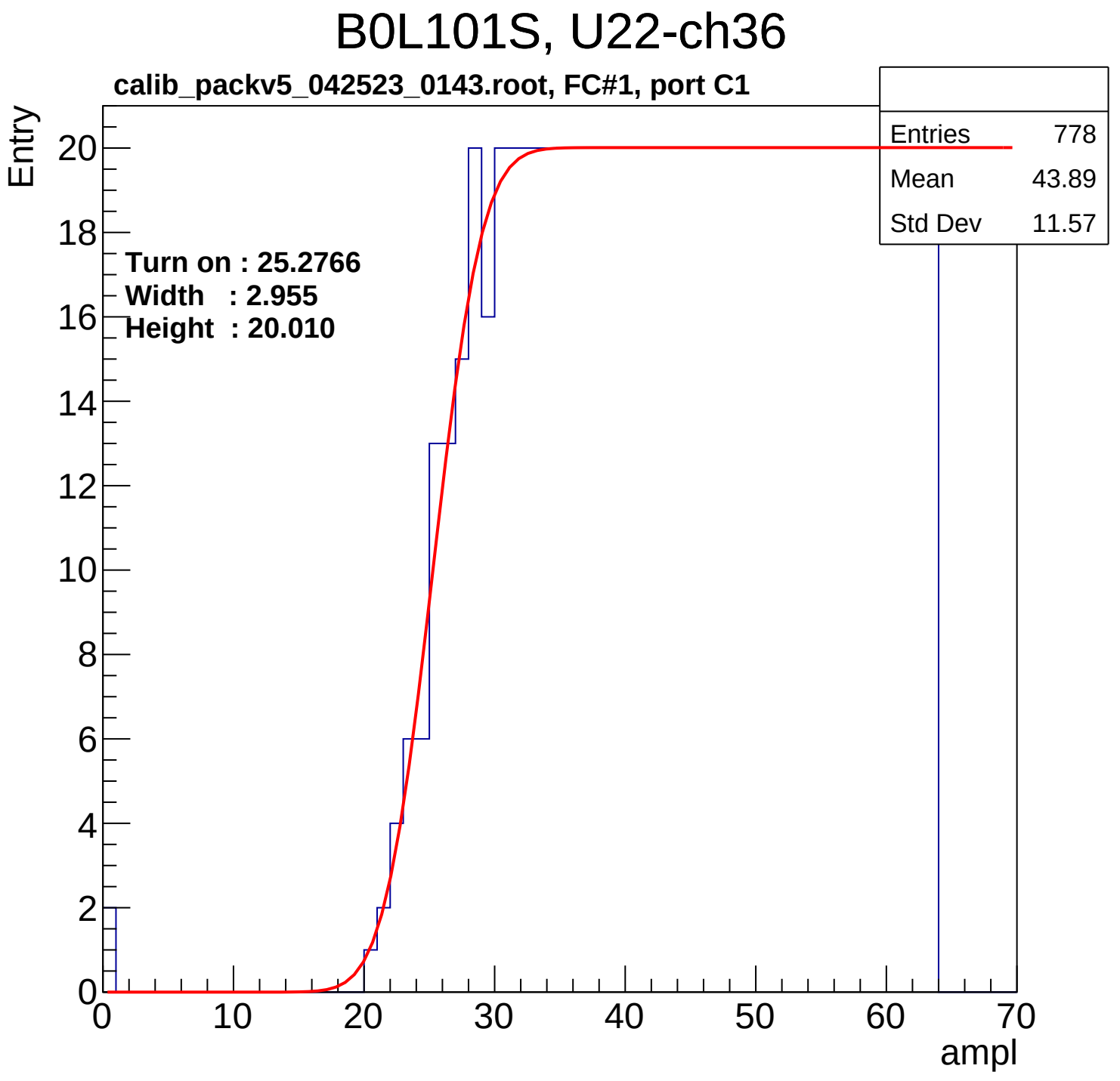

B0L101S, U22-ch31
calib_packv5_042523_0143.root, FC#1, port C1
Entries 750
Mean 44.5
Std Dev 11.36
Turn on : 26.4963
Width : 1.565
Height : 19.628
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

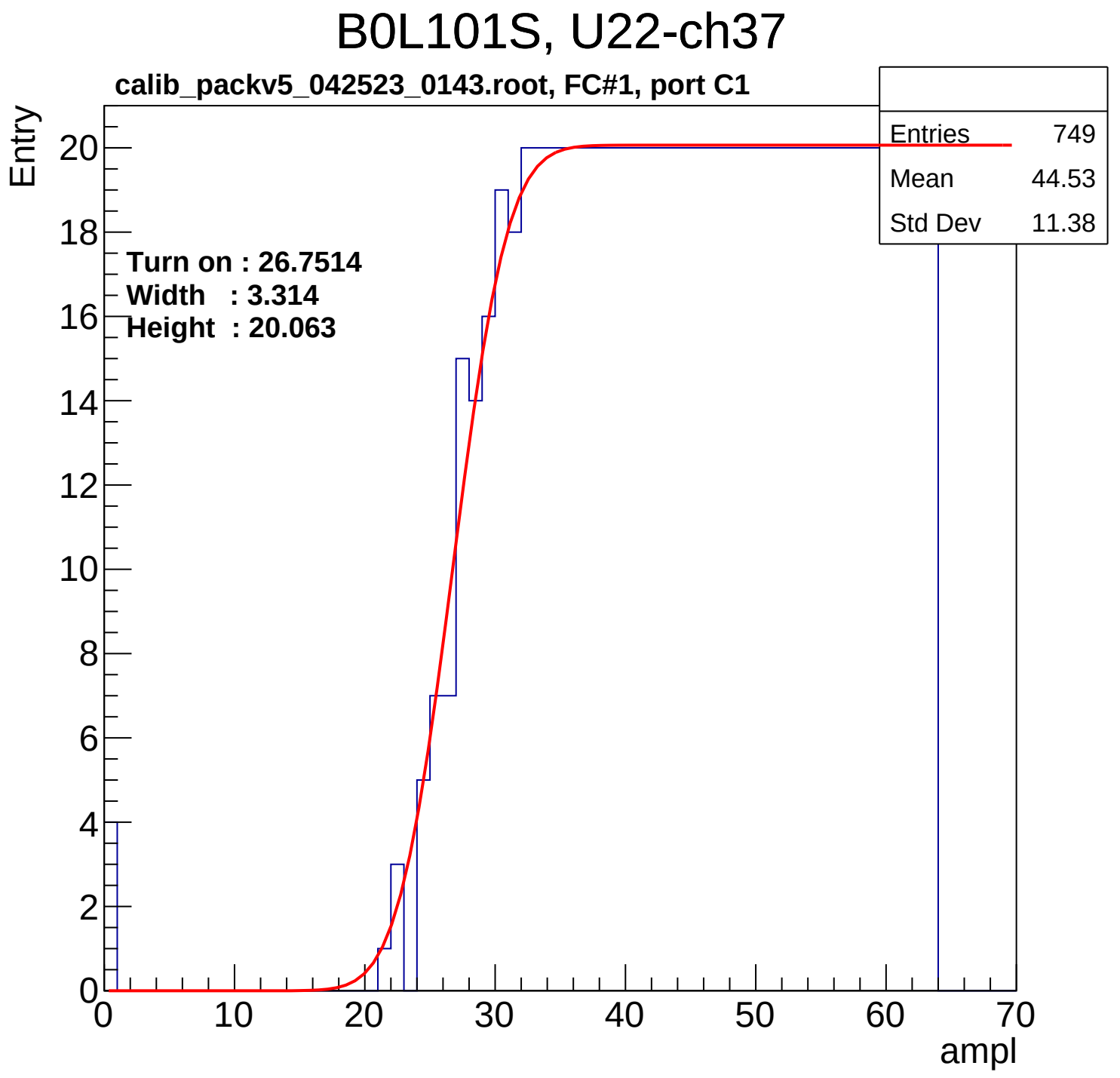

B0L101S, U22-ch32
calib_packv5_042523_0143.root, FC#1, port C1
Entries 726
Mean 45.18
Std Dev 10.86
Turn on : 27.9152
Width : 2.584
Height : 20.015
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

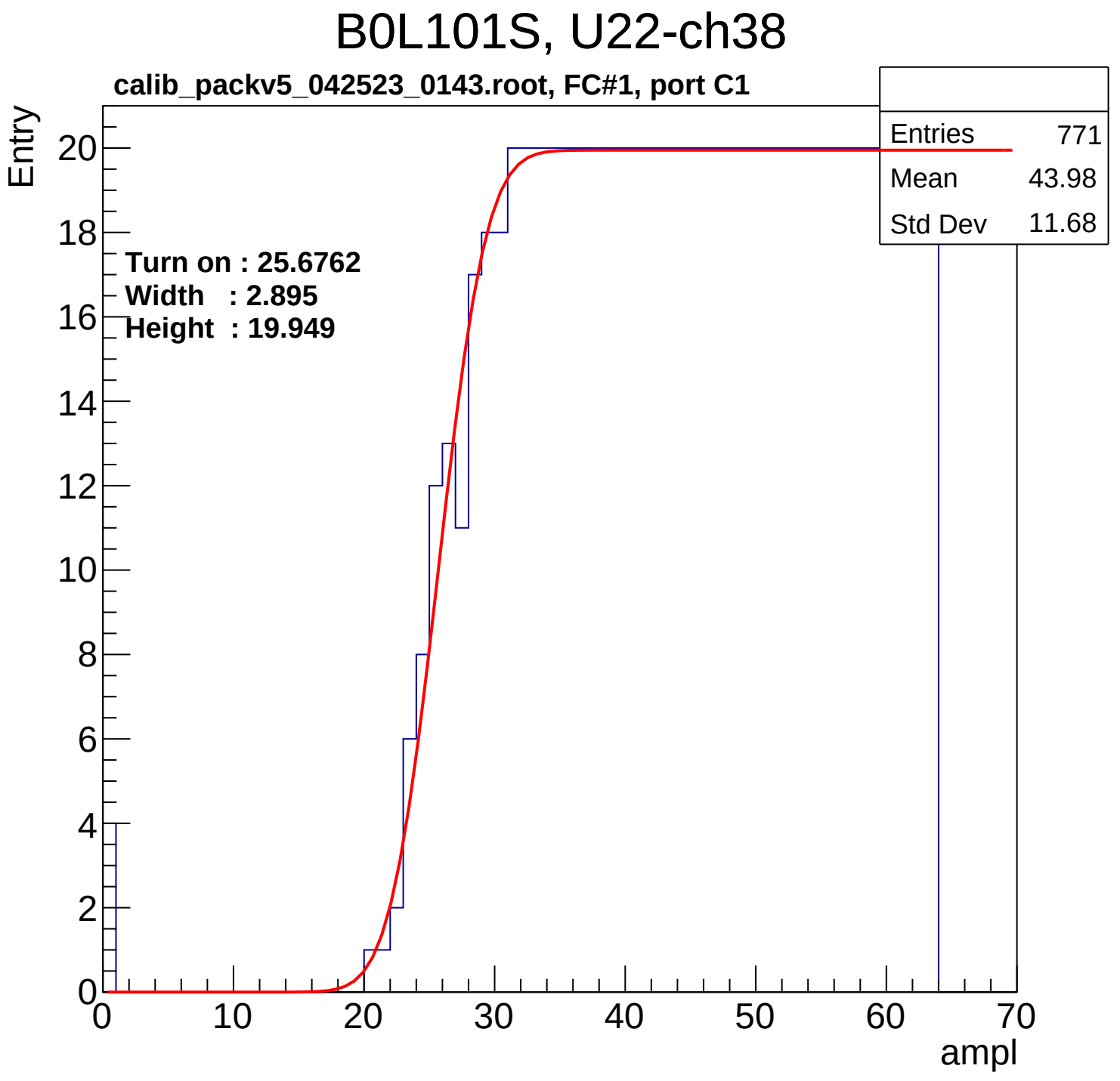

B0L101S, U22-ch33
calib_packv5_042523_0143.root, FC#1, port C1
Entries 726
Mean 45.12
Std Dev 11.01
Turn on : 28.0120
Width : 2.657
Height : 19.980
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

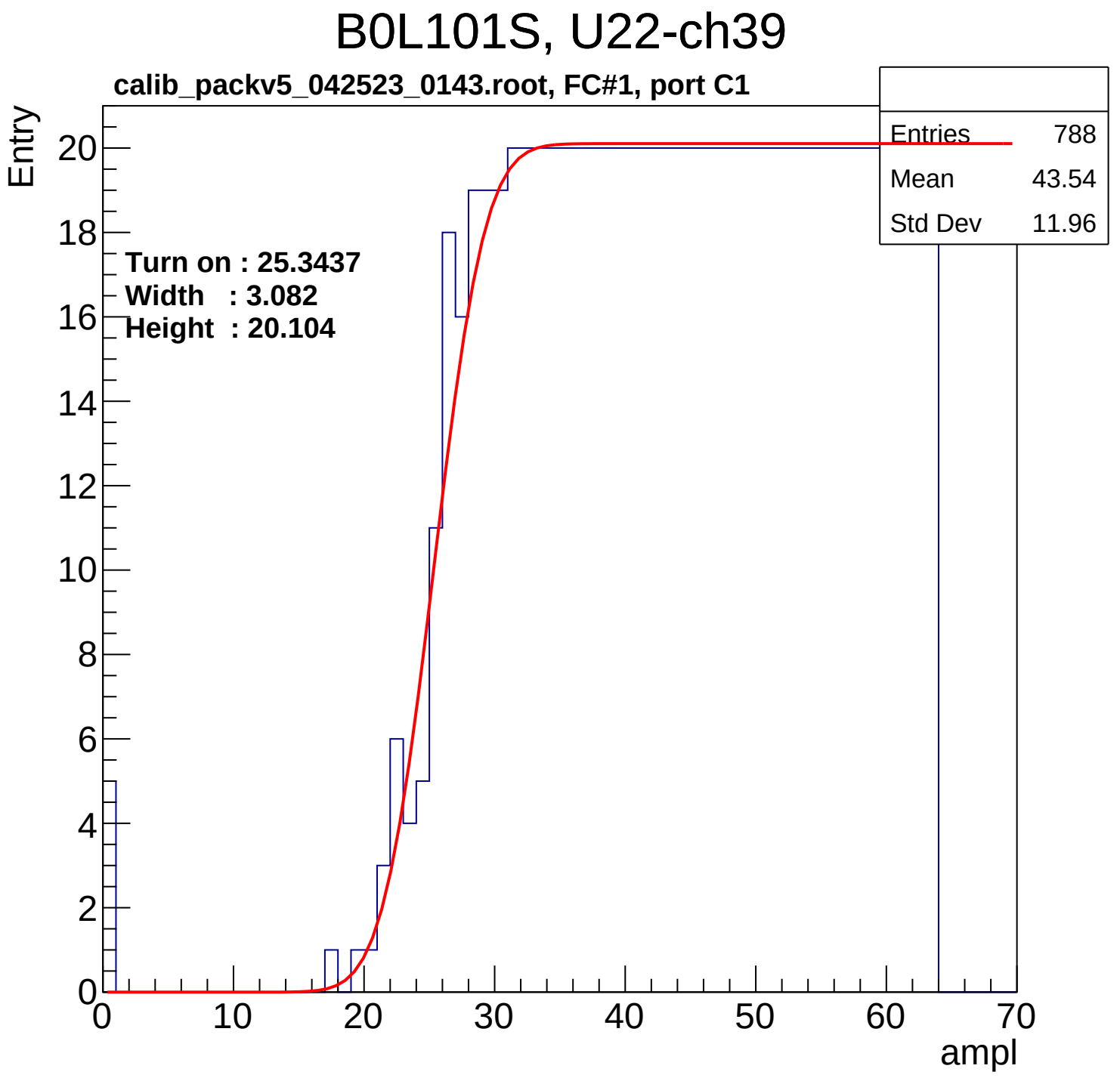

B0L101S, U22-ch34
calib_packv5_042523_0143.root, FC#1, port C1
Entries 767
Mean 44.07
Std Dev 11.63
Turn on : 25.8555
Width : 2.736
Height : 19.896
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

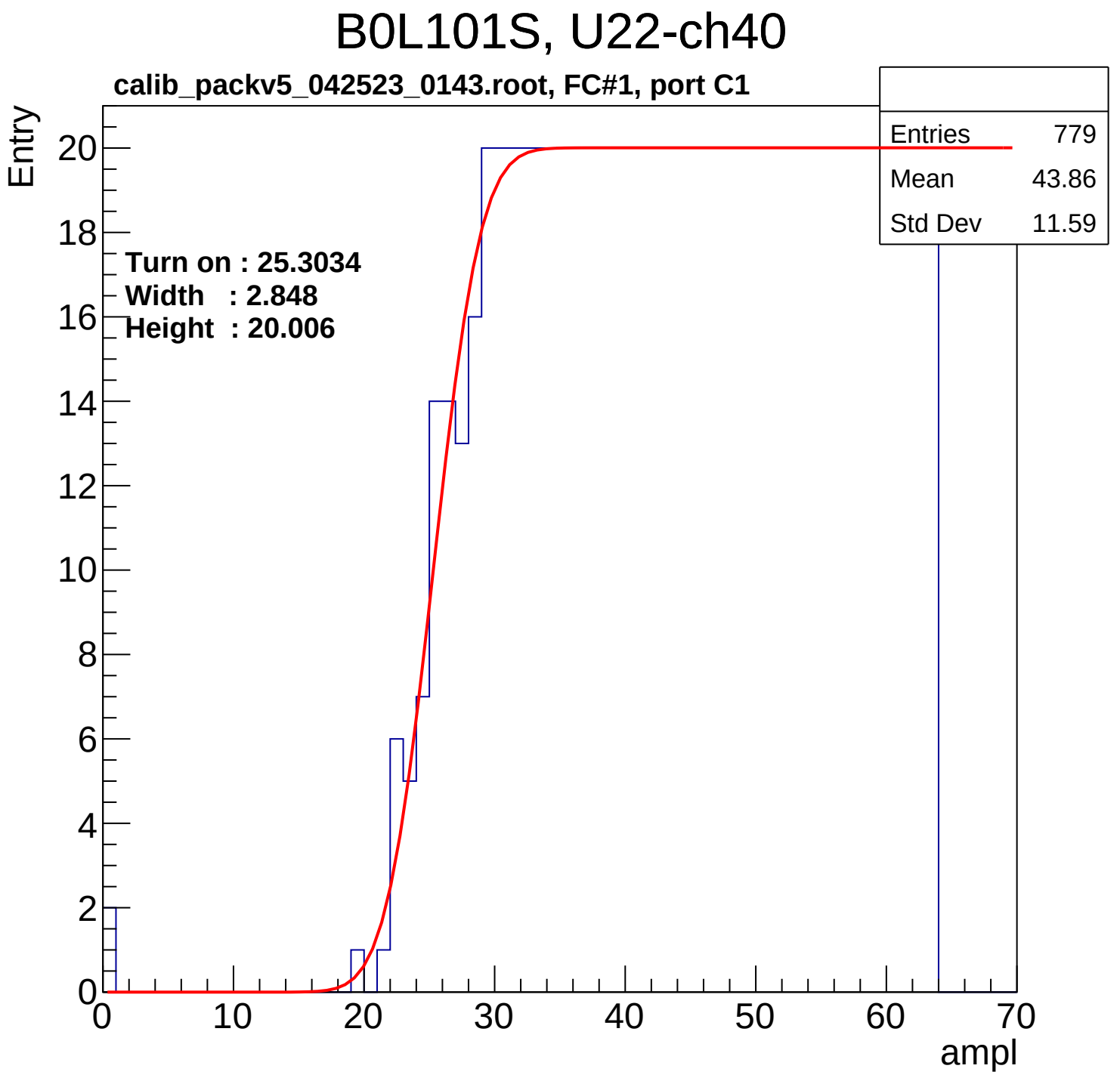

B0L101S, U22-ch35
calib_packv5_042523_0143.root, FC#1, port C1
Entries 722
Mean 45.16
Std Dev 11.09
Turn on : 28.2859
Width : 3.296
Height : 20.004
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

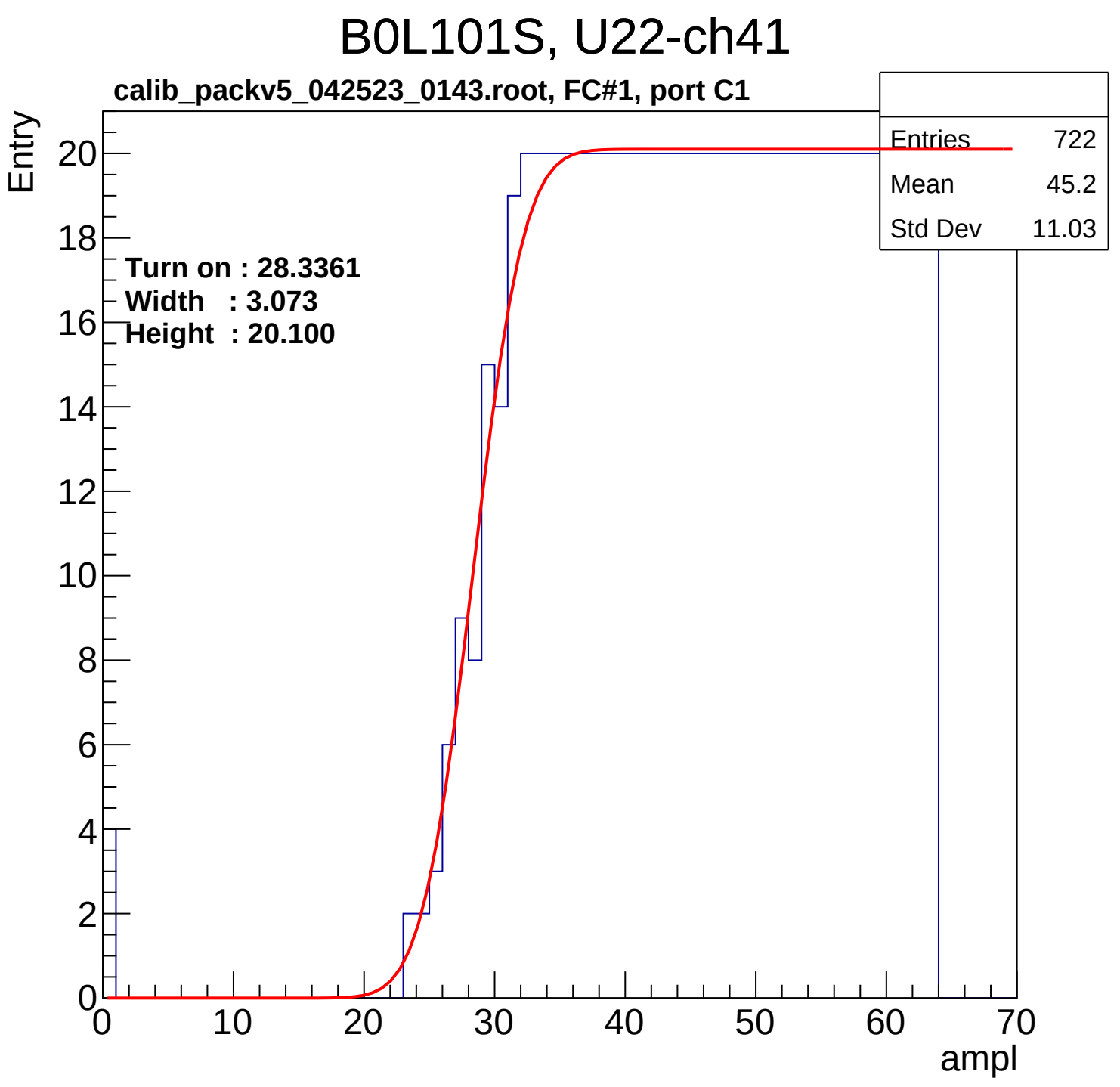

B0L101S, U22-ch36
calib_packv5_042523_0143.root, FC#1, port C1
Entries 778
Mean 43.89
Std Dev 11.57
Turn on : 25.2766
Width : 2.955
Height : 20.010
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

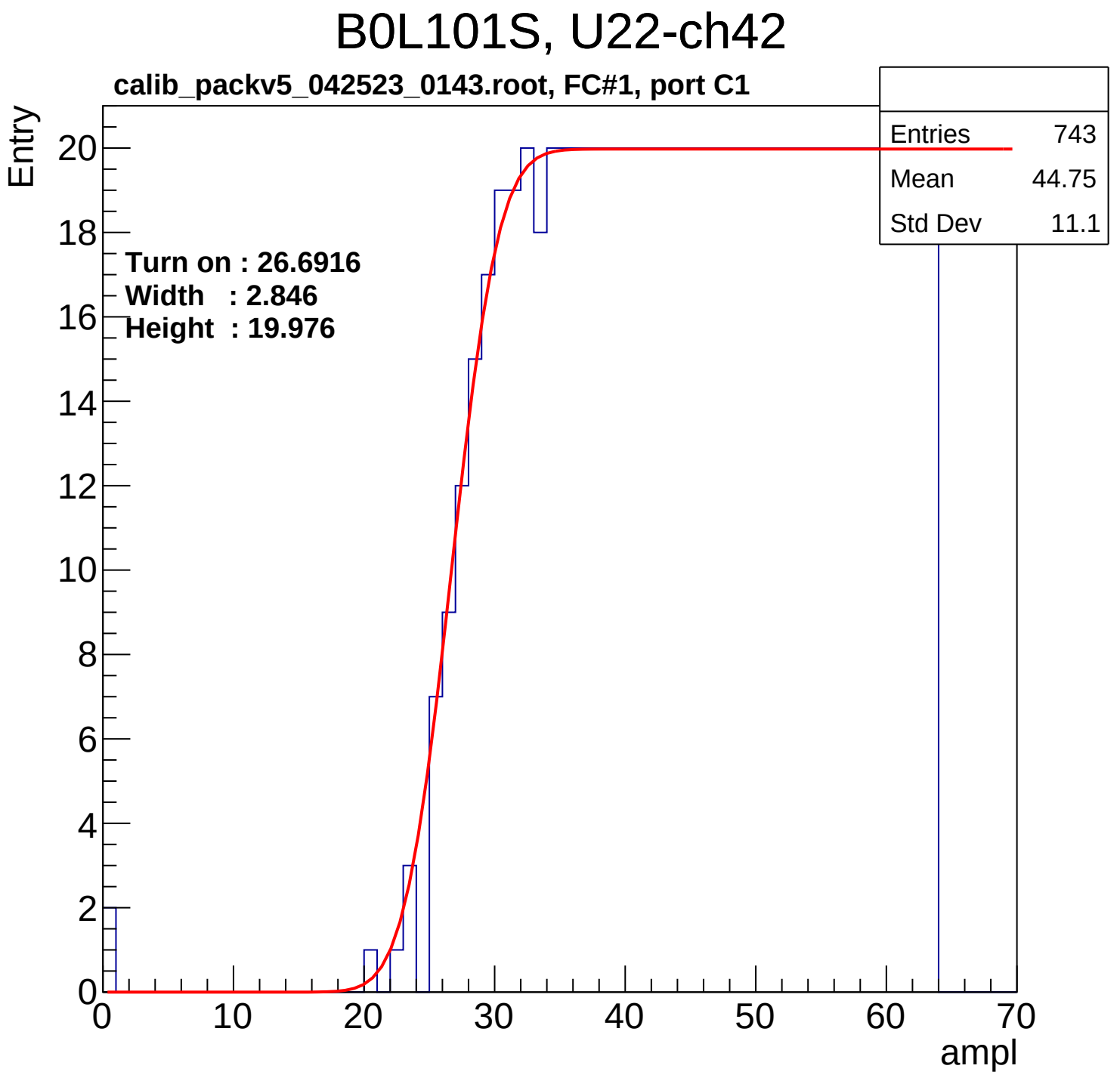

B0L101S, U22-ch37
calib_packv5_042523_0143.root, FC#1, port C1
Entries 749
Mean 44.53
Std Dev 11.38
Turn on : 26.7514
Width : 3.314
Height : 20.063
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

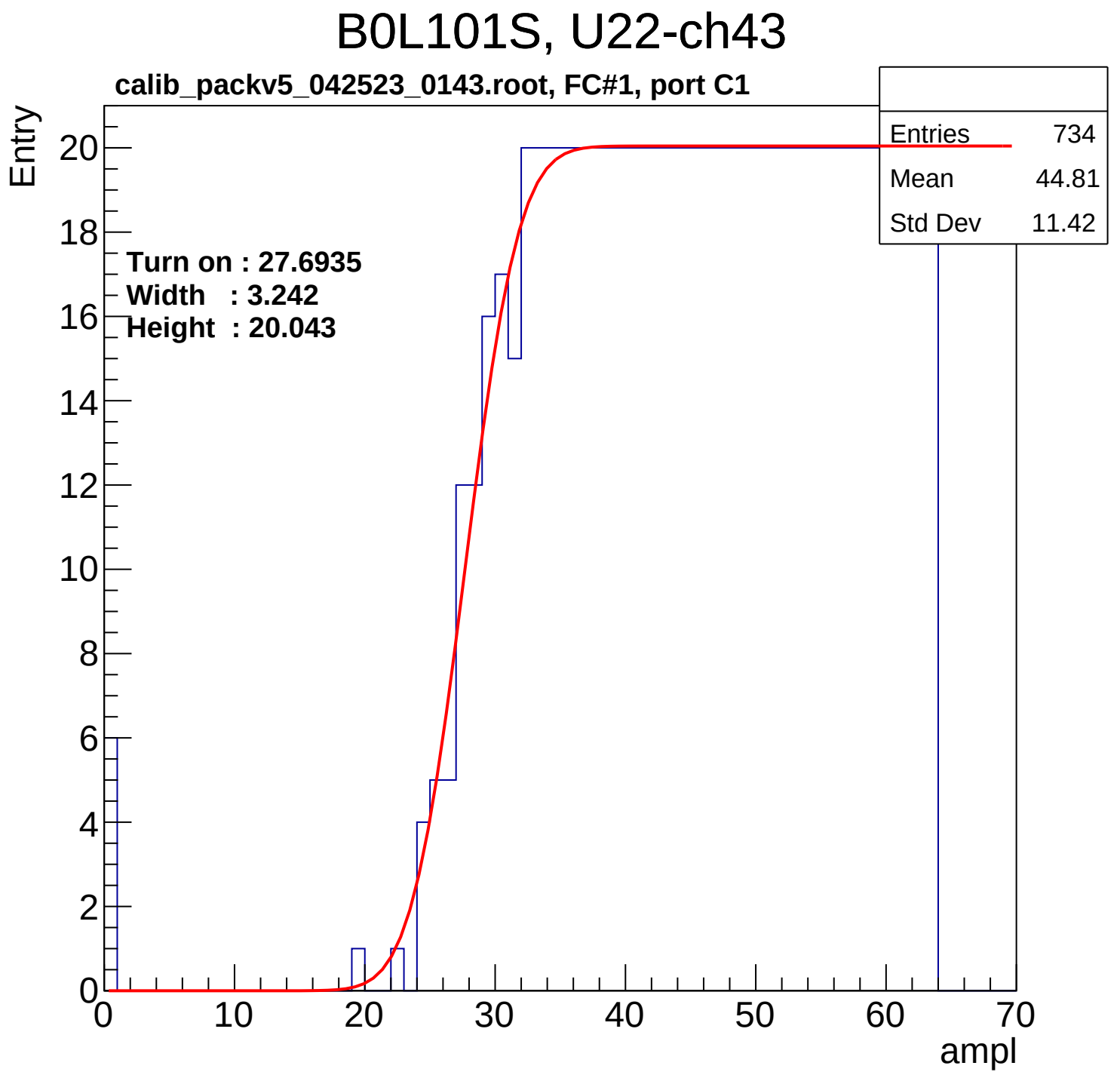

B0L101S, U22-ch38
calib_packv5_042523_0143.root, FC#1, port C1
Entries 771
Mean 43.98
Std Dev 11.68
Turn on : 25.6762
Width : 2.895
Height : 19.949
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

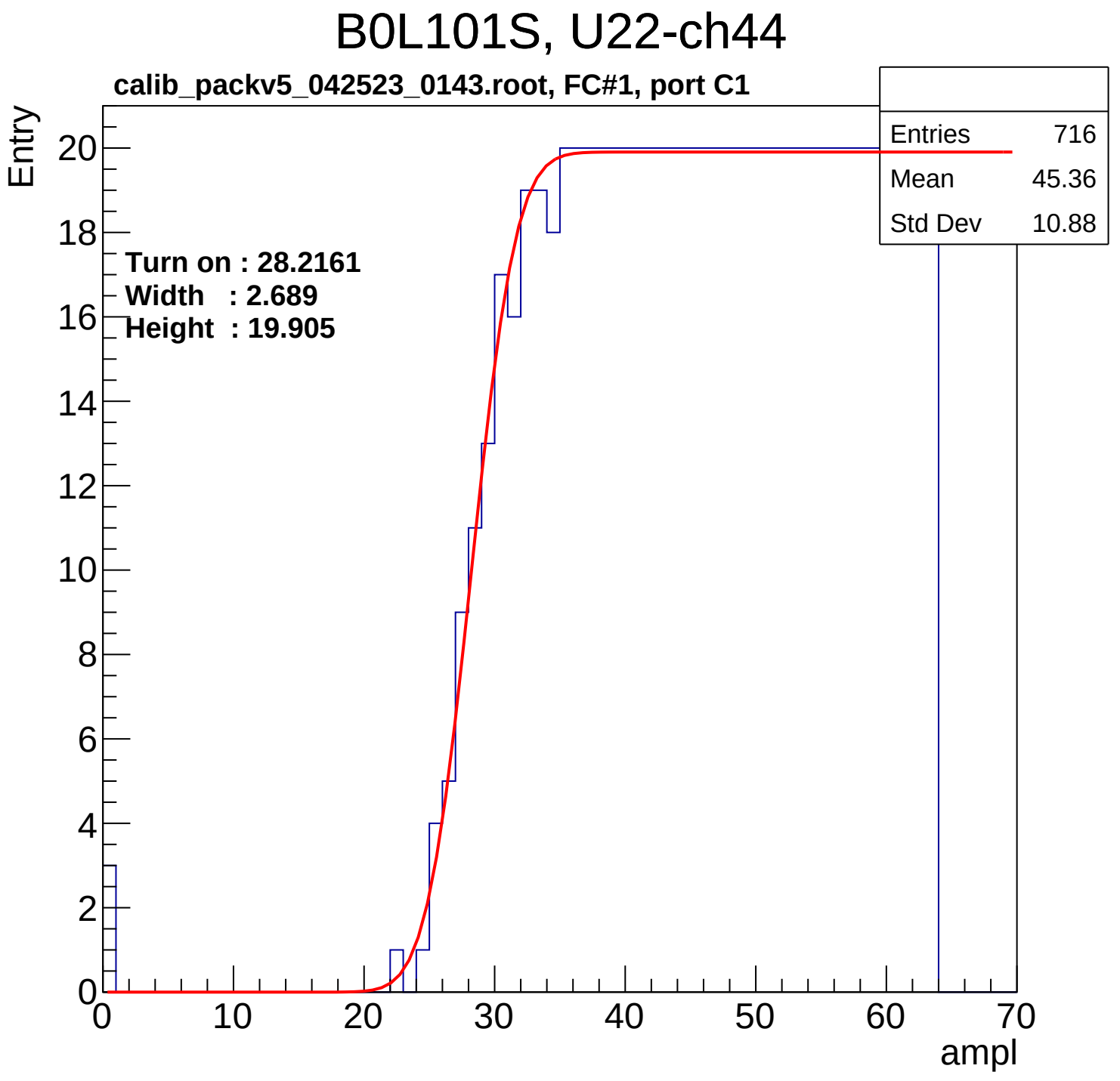

B0L101S, U22-ch39
calib_packv5_042523_0143.root, FC#1, port C1
Entries 788
Mean 43.54
Std Dev 11.96
Turn on : 25.3437
Width : 3.082
Height : 20.104
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

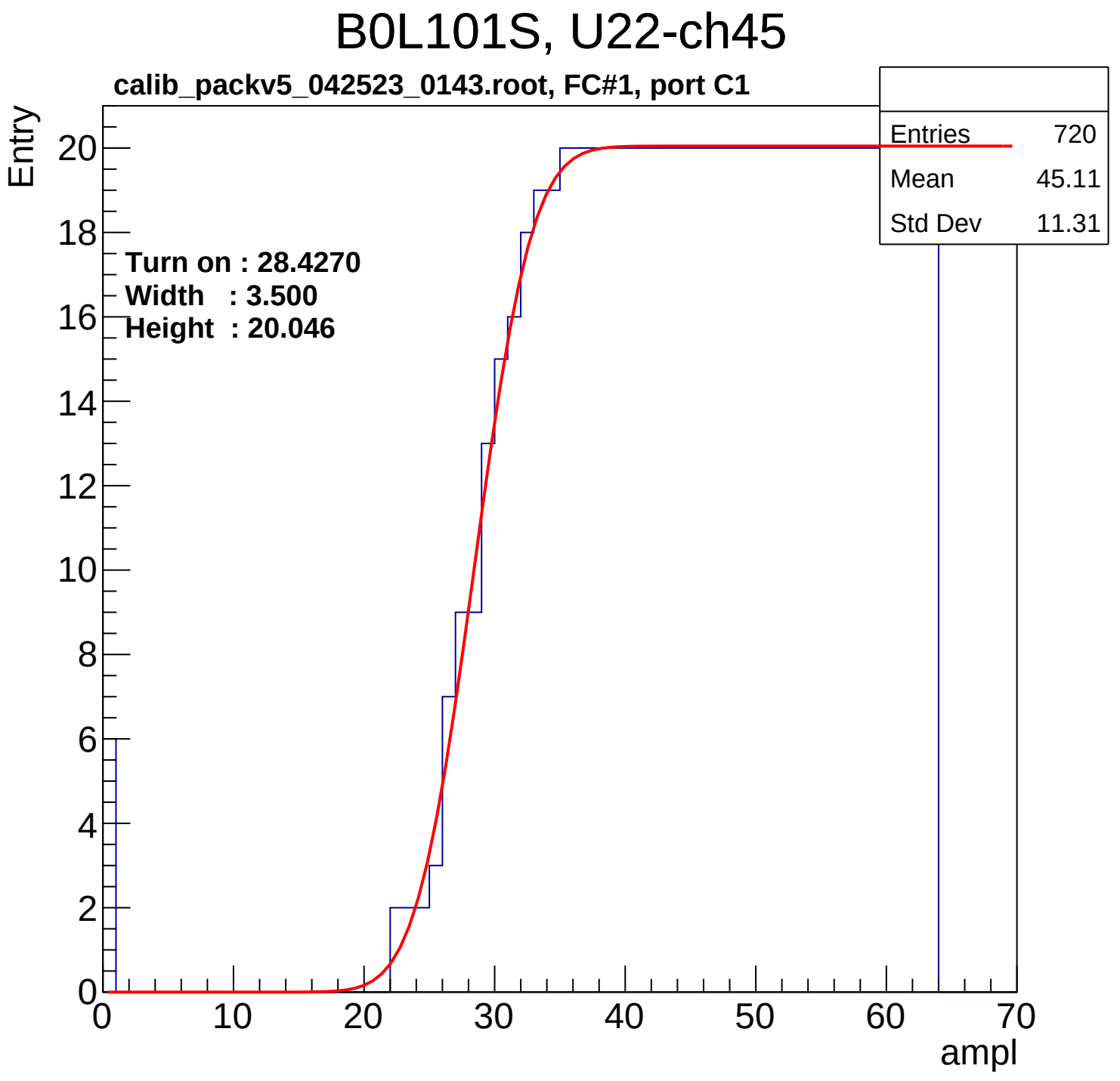

B0L101S, U22-ch40
calib_packv5_042523_0143.root, FC#1, port C1
Entries 779
Mean 43.86
Std Dev 11.59
Turn on : 25.3034
Width : 2.848
Height : 20.006
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

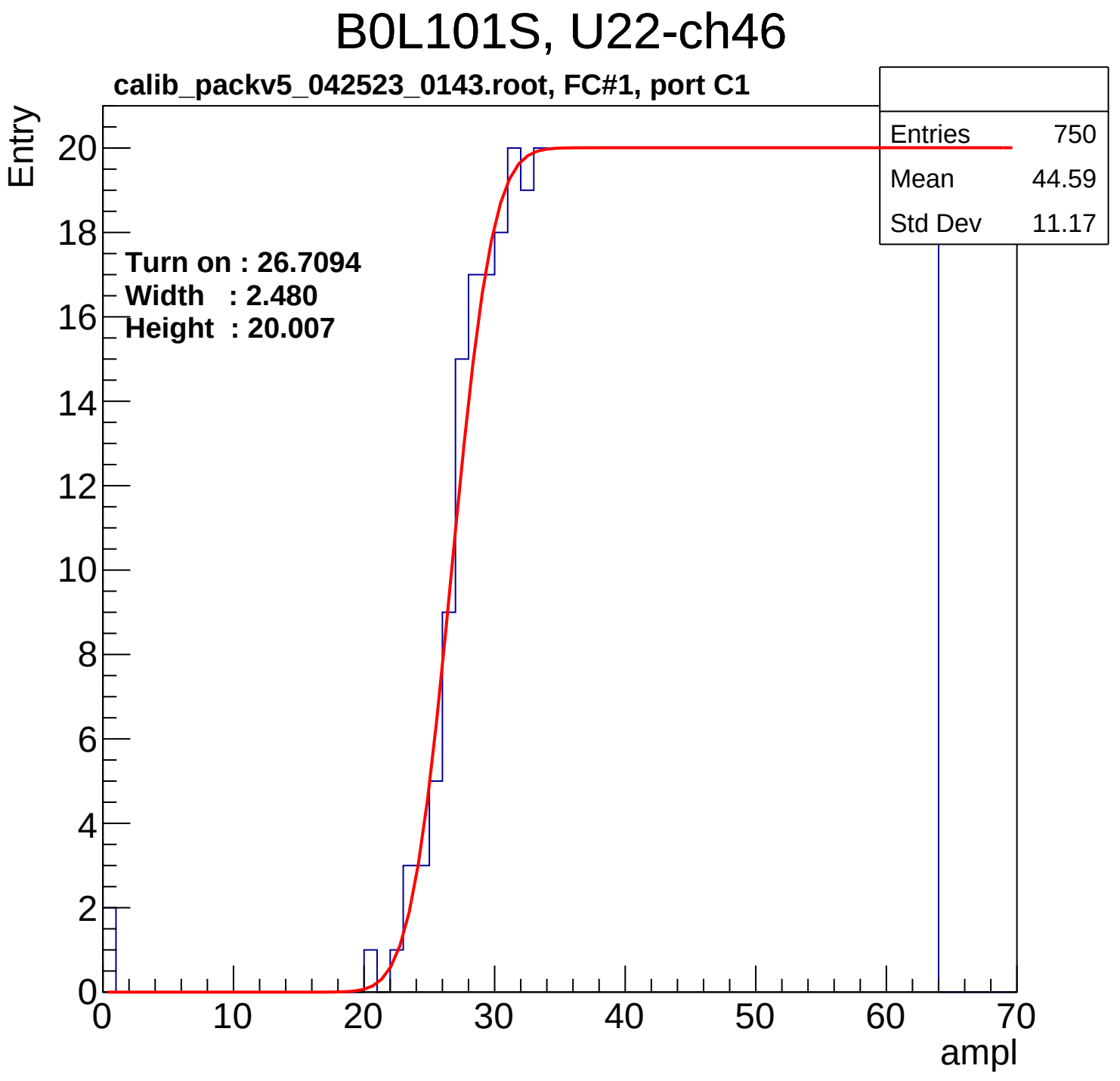

B0L101S, U22-ch41
calib_packv5_042523_0143.root, FC#1, port C1
Entries 722
Mean 45.2
Std Dev 11.03
Turn on : 28.3361
Width : 3.073
Height : 20.100
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

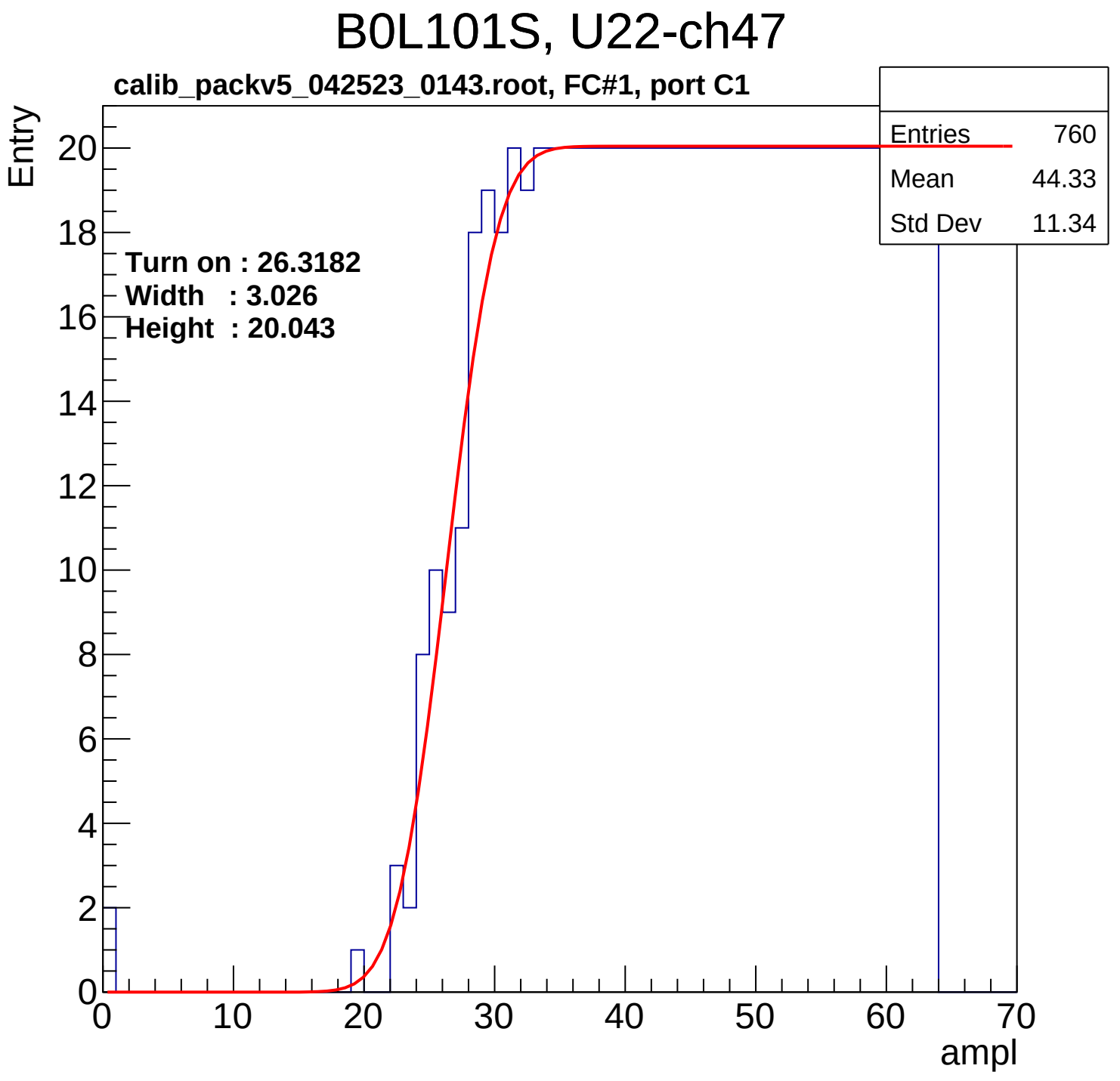

B0L101S, U22-ch42
calib_packv5_042523_0143.root, FC#1, port C1
Entries 743
Mean 44.75
Std Dev 11.1
Turn on : 26.6916
Width : 2.846
Height : 19.976
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

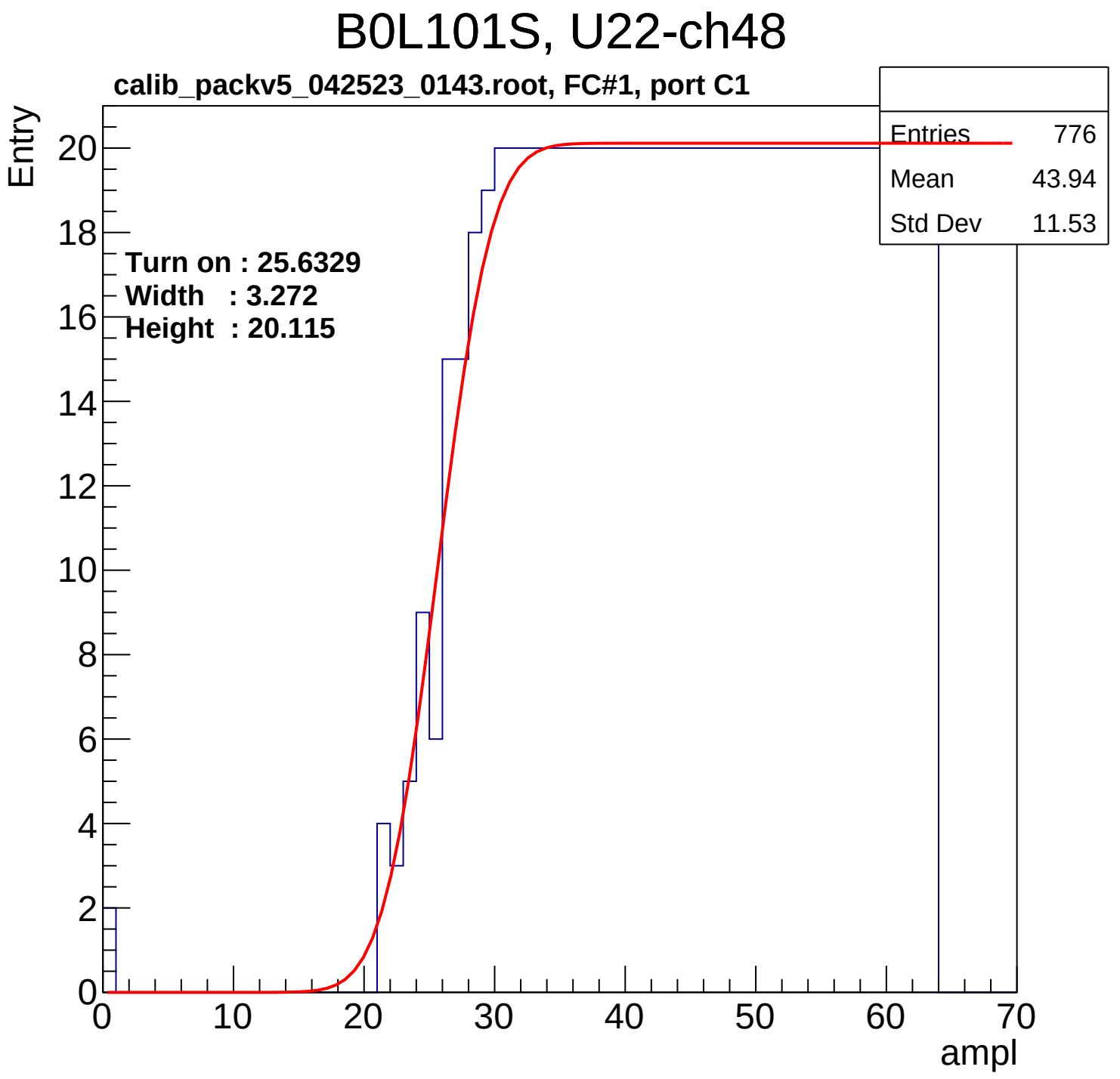

B0L101S, U22-ch43
calib_packv5_042523_0143.root, FC#1, port C1
Entries 734
Mean 44.81
Std Dev 11.42
Turn on : 27.6935
Width : 3.242
Height : 20.043
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

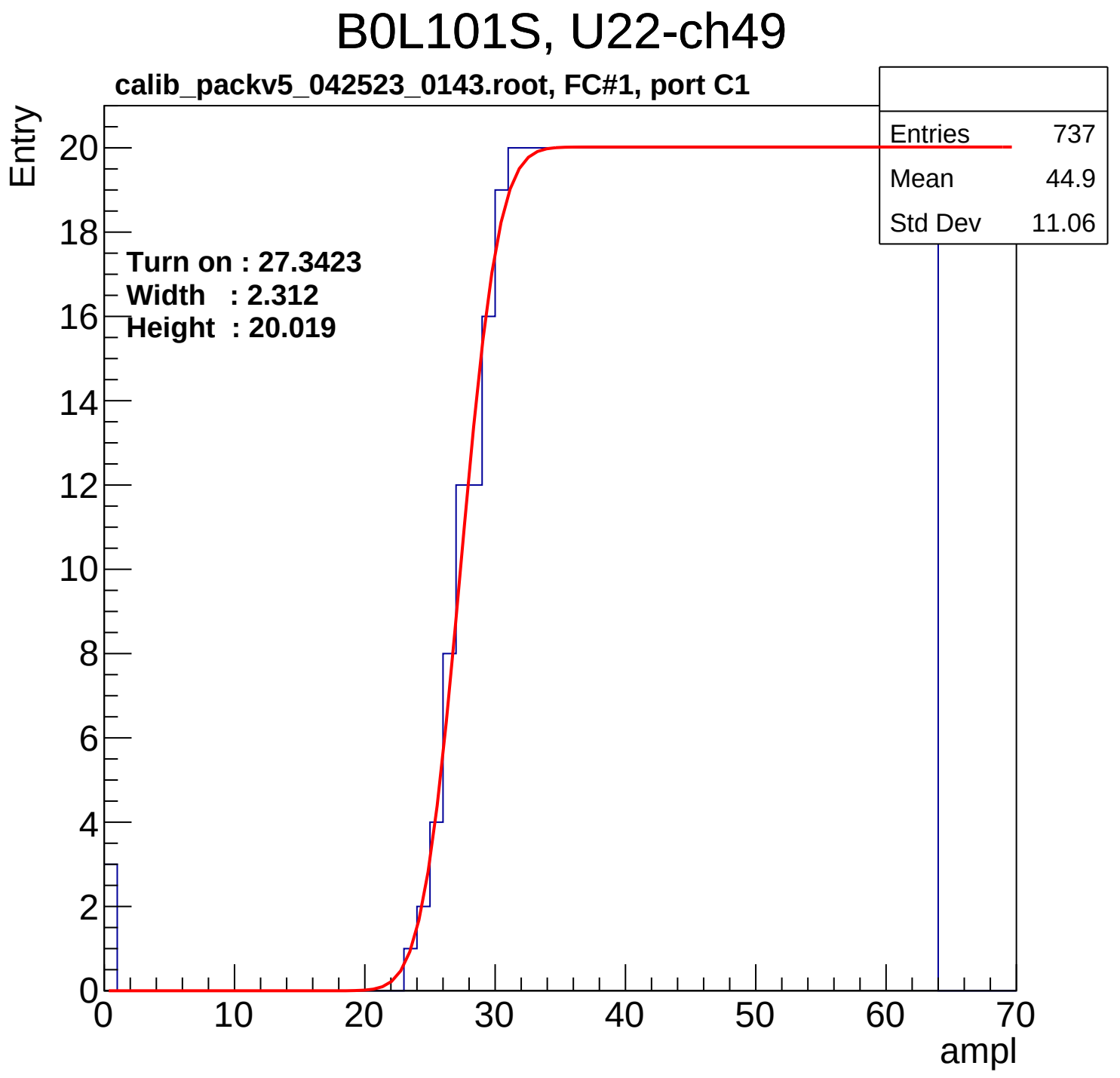

B0L101S, U22-ch44
calib_packv5_042523_0143.root, FC#1, port C1
Entries 716
Mean 45.36
Std Dev 10.88
Turn on : 28.2161
Width : 2.689
Height : 19.905
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

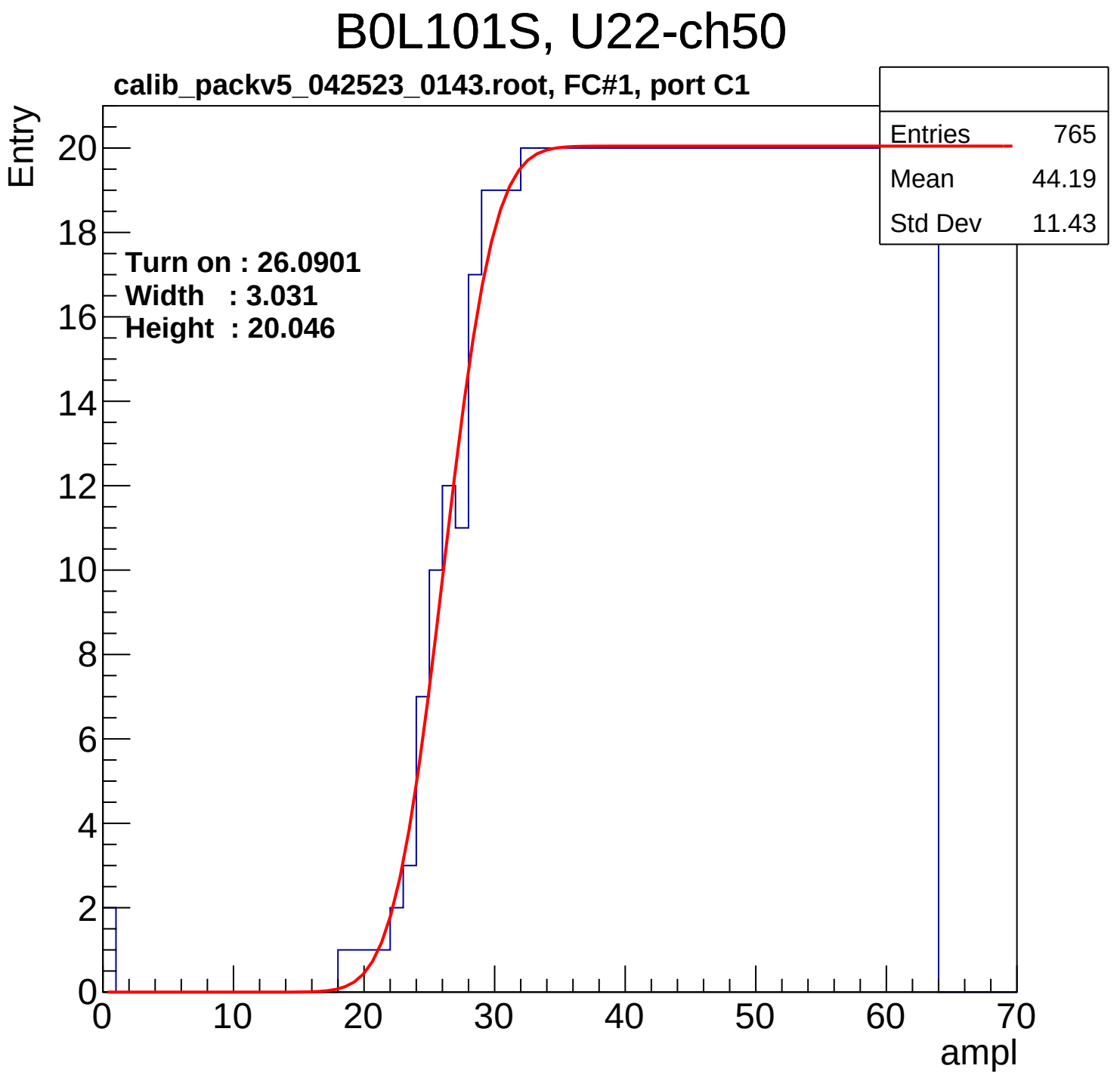

B0L101S, U22-ch45
calib_packv5_042523_0143.root, FC#1, port C1
Entries 720
Mean 45.11
Std Dev 11.31
Turn on : 28.4270
Width : 3.500
Height : 20.046
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

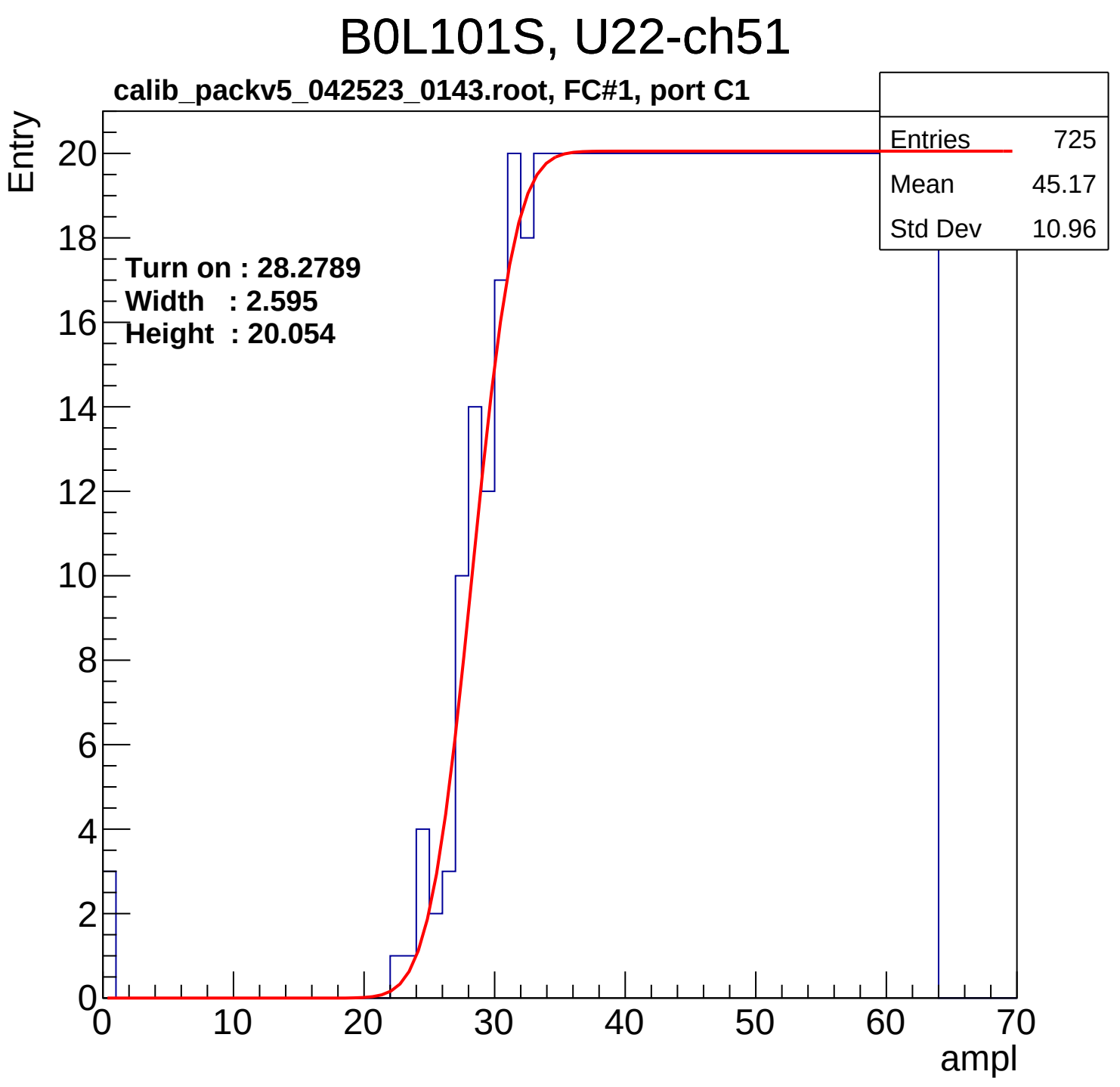

B0L101S, U22-ch46
calib_packv5_042523_0143.root, FC#1, port C1
Entries 750
Mean 44.59
Std Dev 11.17
Turn on : 26.7094
Width : 2.480
Height : 20.007
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

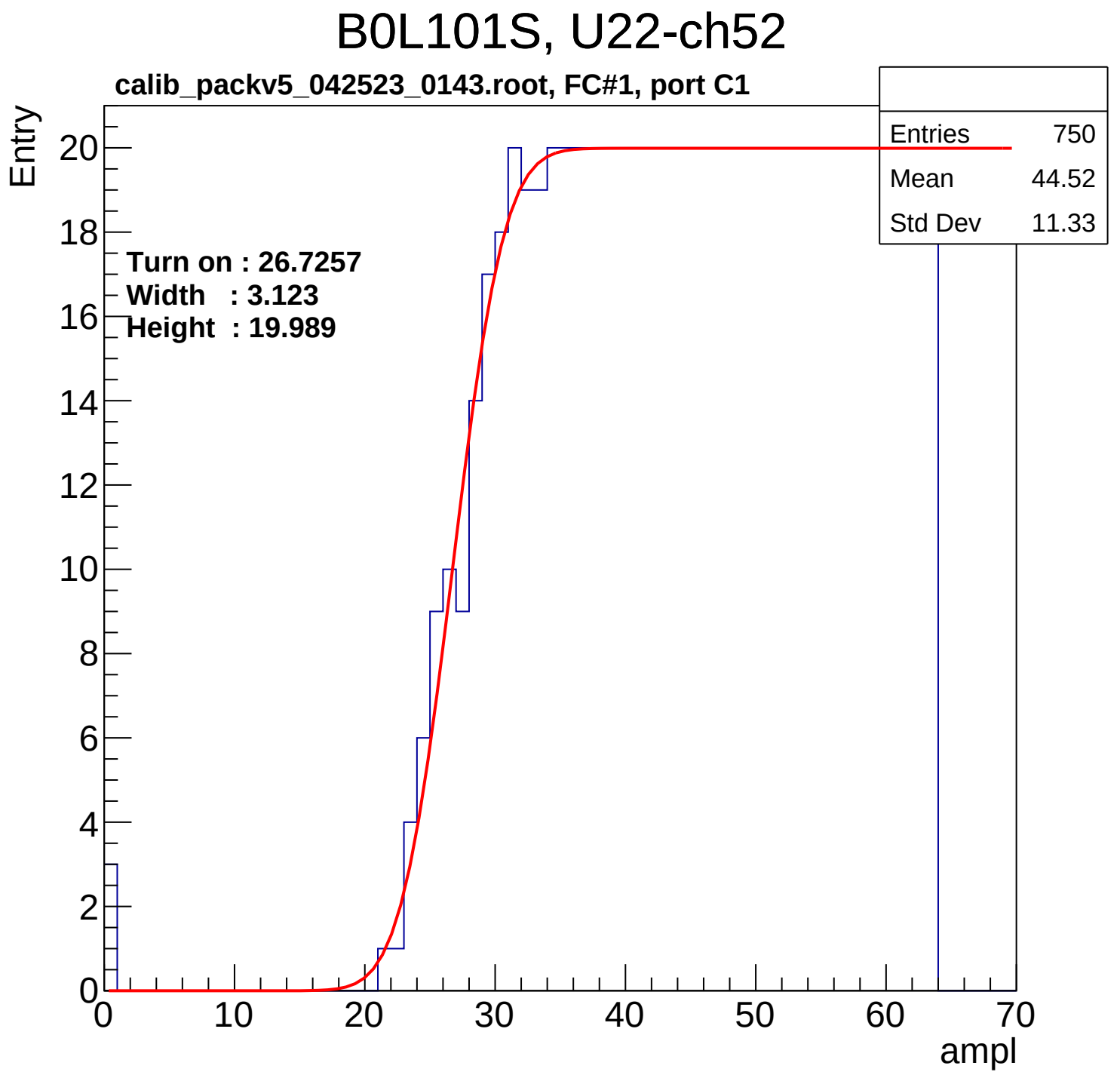

B0L101S, U22-ch47
calib_packv5_042523_0143.root, FC#1, port C1
Entries 760
Mean 44.33
Std Dev 11.34
Turn on : 26.3182
Width : 3.026
Height : 20.043
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

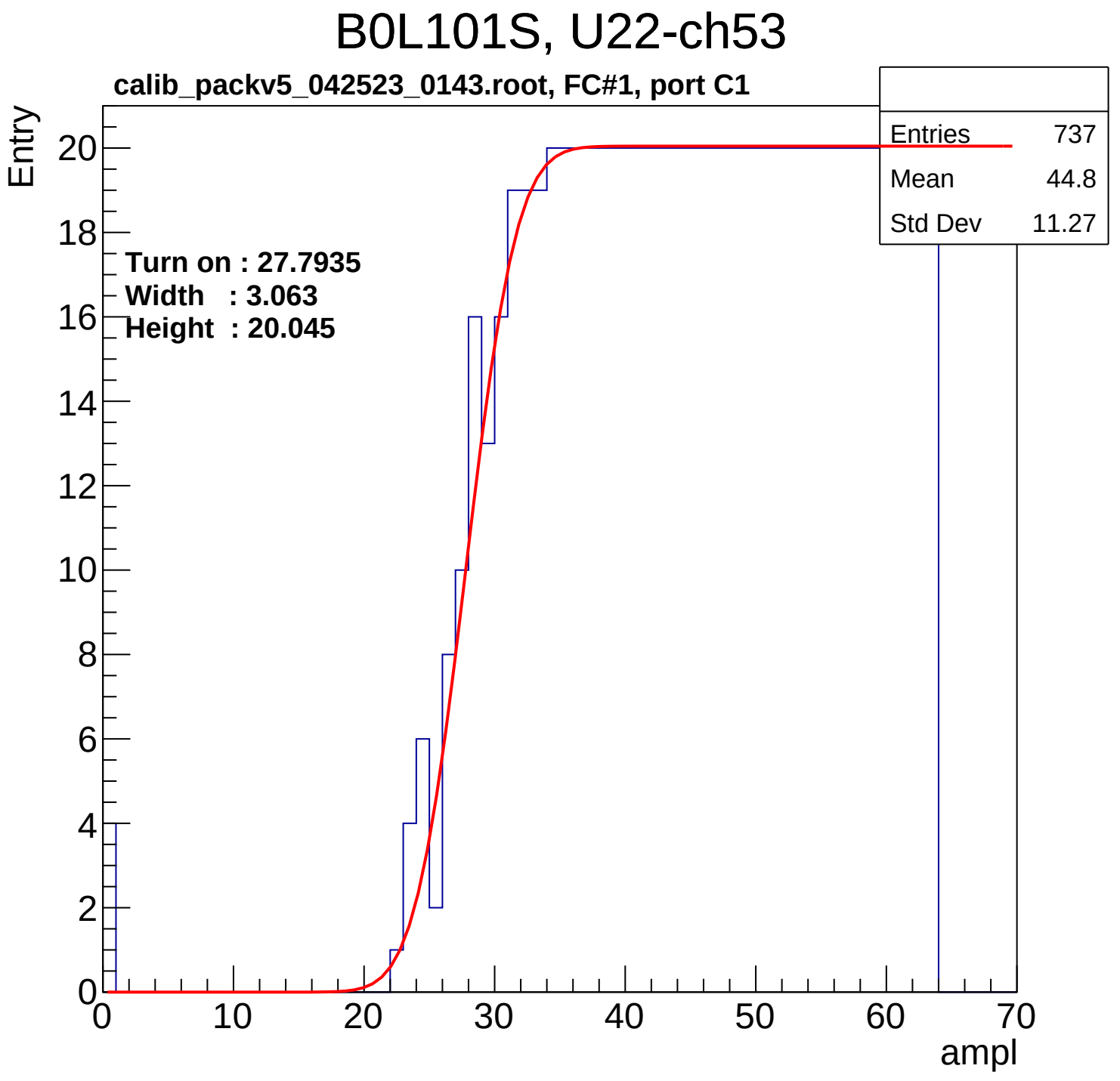

B0L101S, U22-ch48
calib_packv5_042523_0143.root, FC#1, port C1
Entries 776
Mean 43.94
Std Dev 11.53
Turn on : 25.6329
Width : 3.272
Height : 20.115
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

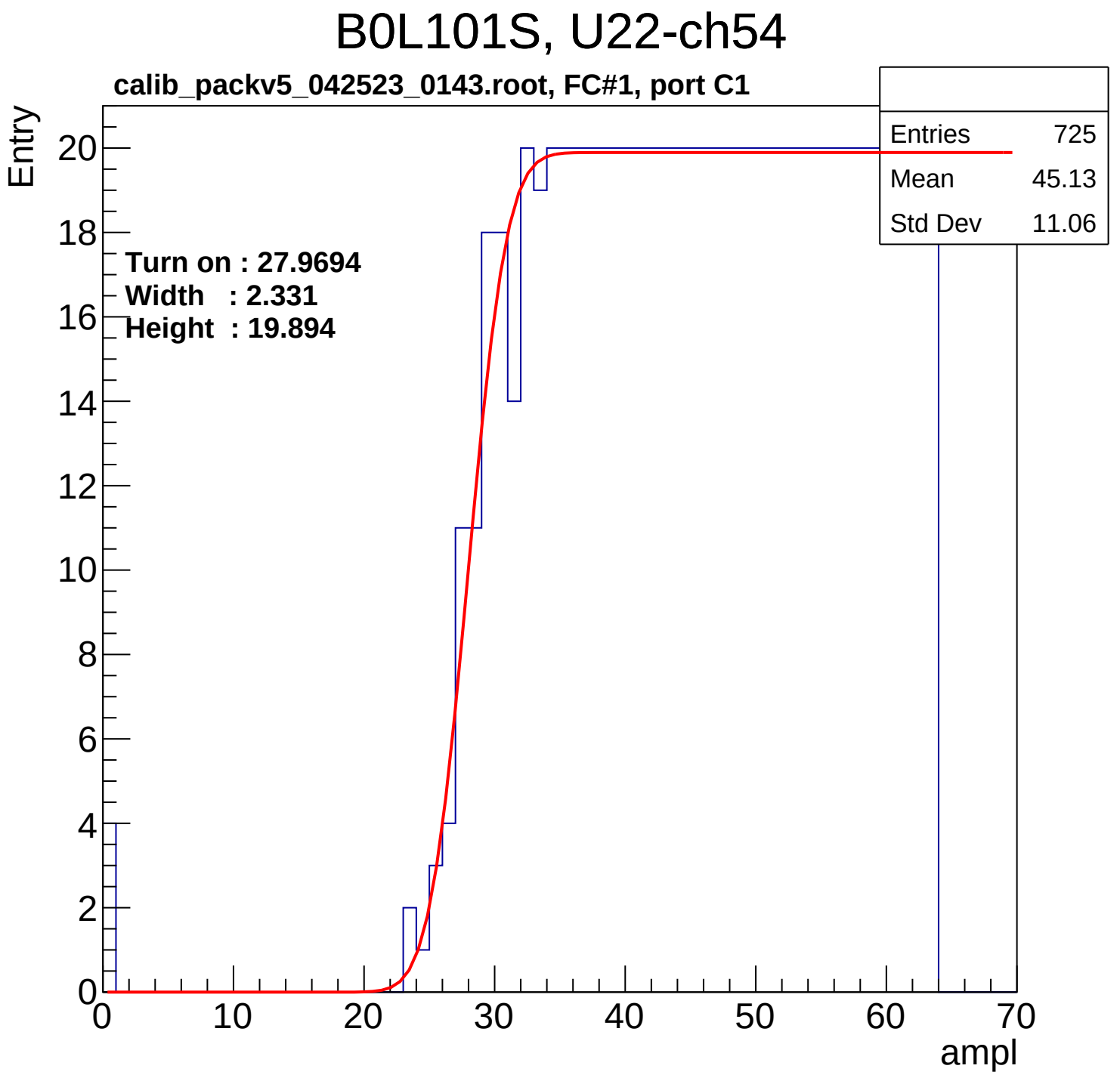

B0L101S, U22-ch49
calib_packv5_042523_0143.root, FC#1, port C1
Entries 737
Mean 44.9
Std Dev 11.06
Turn on : 27.3423
Width : 2.312
Height : 20.019
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

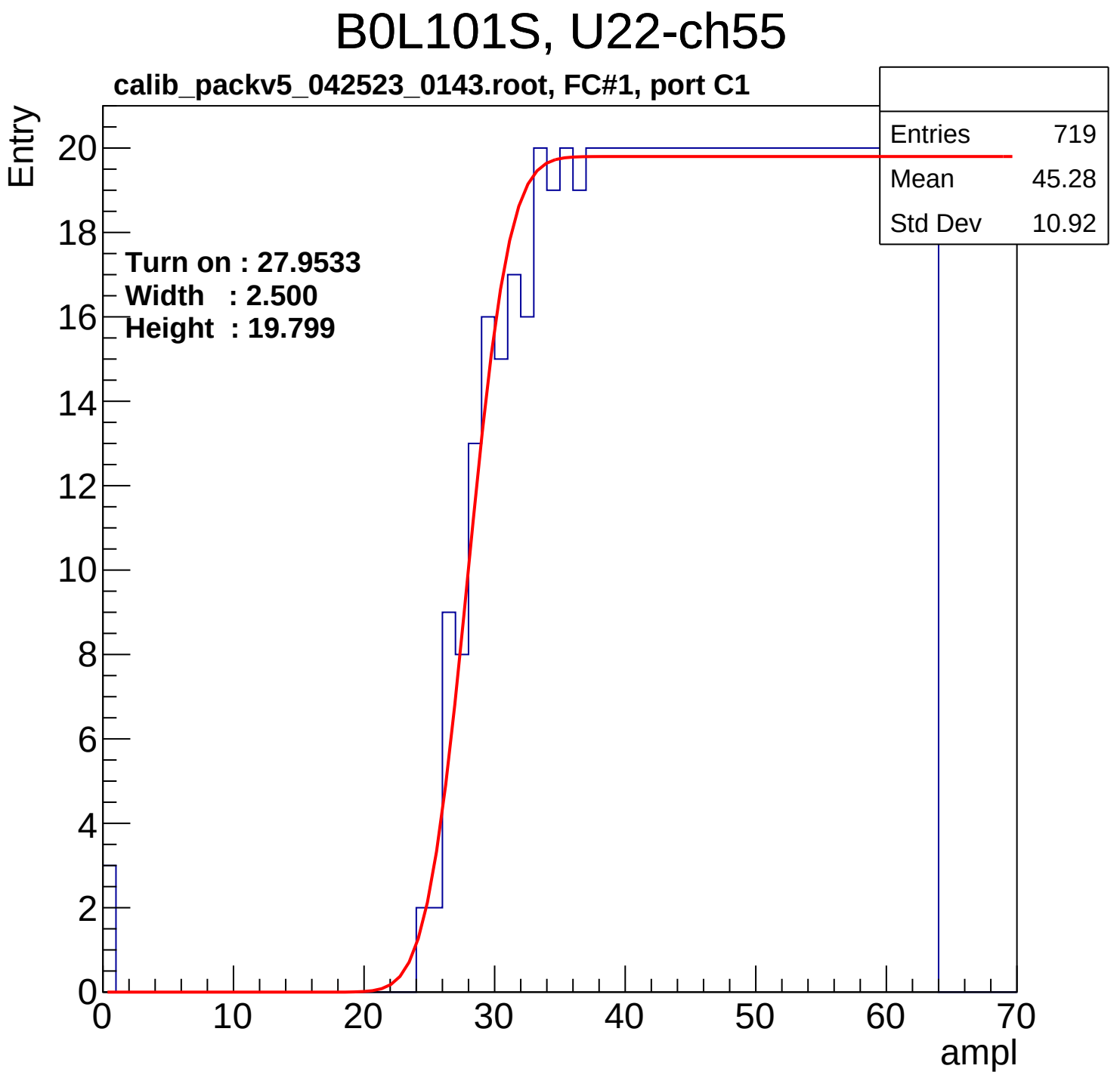

B0L101S, U22-ch50
calib_packv5_042523_0143.root, FC#1, port C1
Entries 765
Mean 44.19
Std Dev 11.43
Turn on : 26.0901
Width : 3.031
Height : 20.046
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

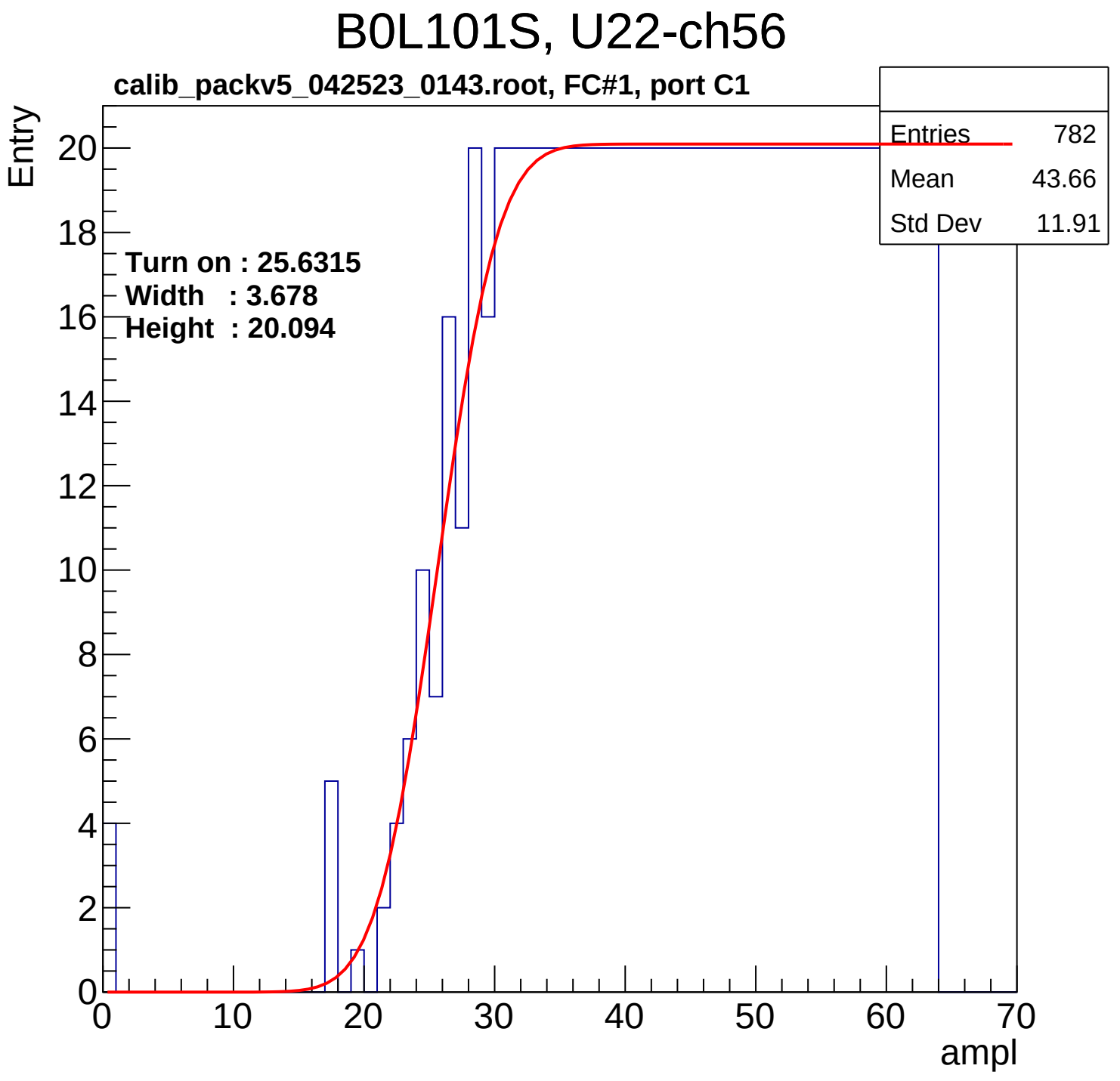

B0L101S, U22-ch51
calib_packv5_042523_0143.root, FC#1, port C1
Entries 725
Mean 45.17
Std Dev 10.96
Turn on : 28.2789
Width : 2.595
Height : 20.054
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

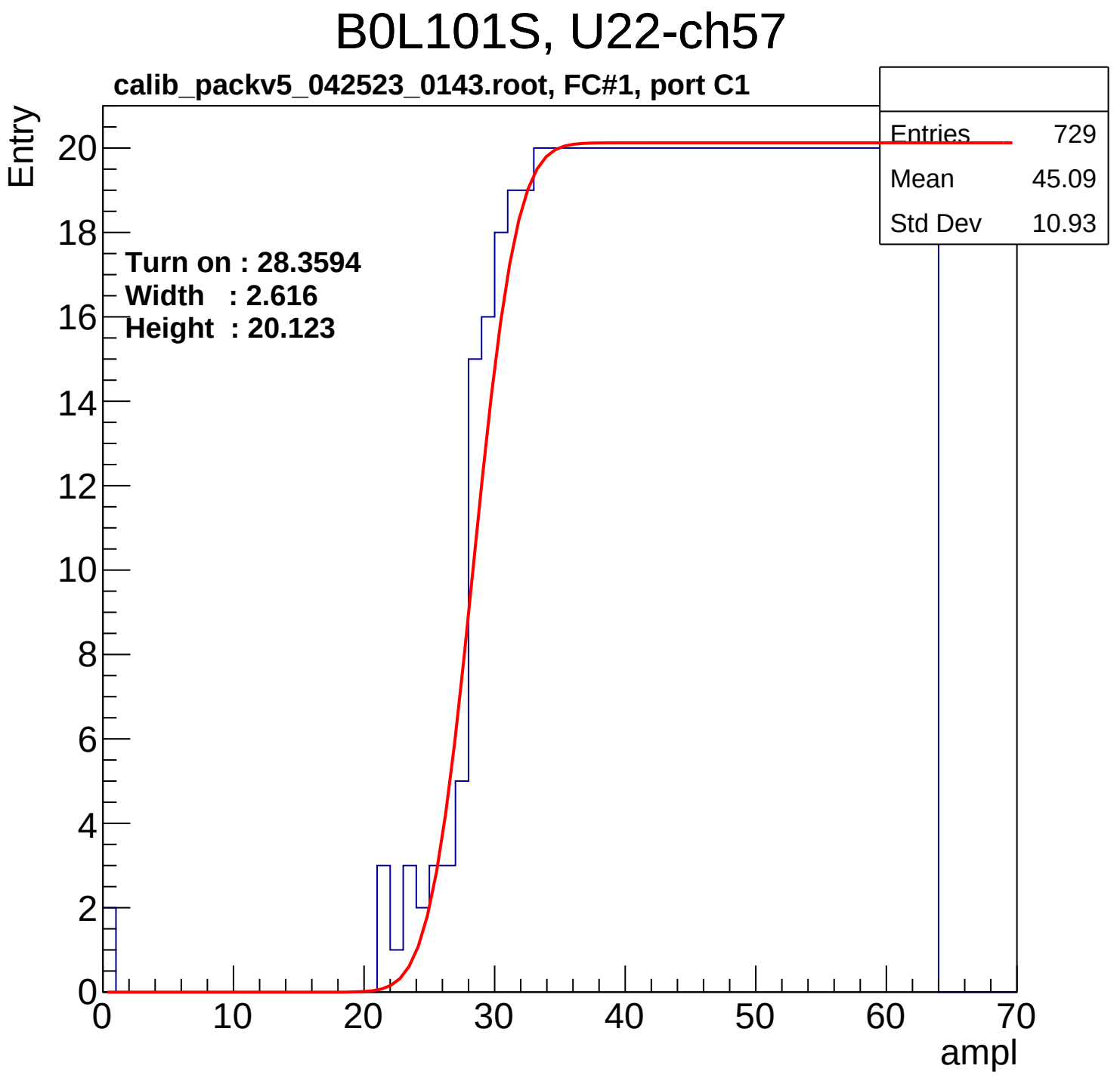

B0L101S, U22-ch52
calib_packv5_042523_0143.root, FC#1, port C1
Entries 750
Mean 44.52
Std Dev 11.33
Turn on : 26.7257
Width : 3.123
Height : 19.989
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

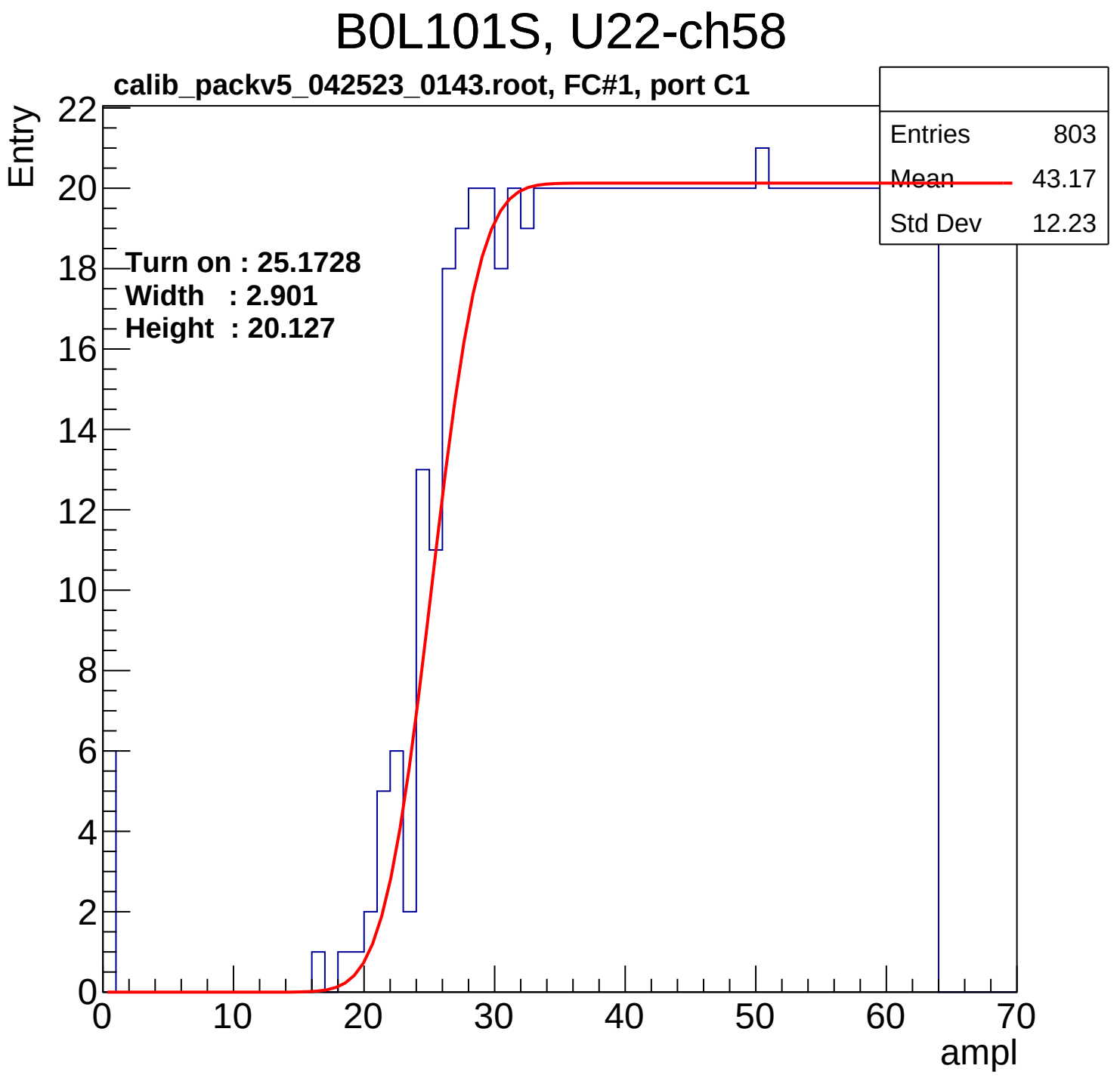

B0L101S, U22-ch53
calib_packv5_042523_0143.root, FC#1, port C1
Entries 737
Mean 44.8
Std Dev 11.27
Turn on : 27.7935
Width : 3.063
Height : 20.045
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

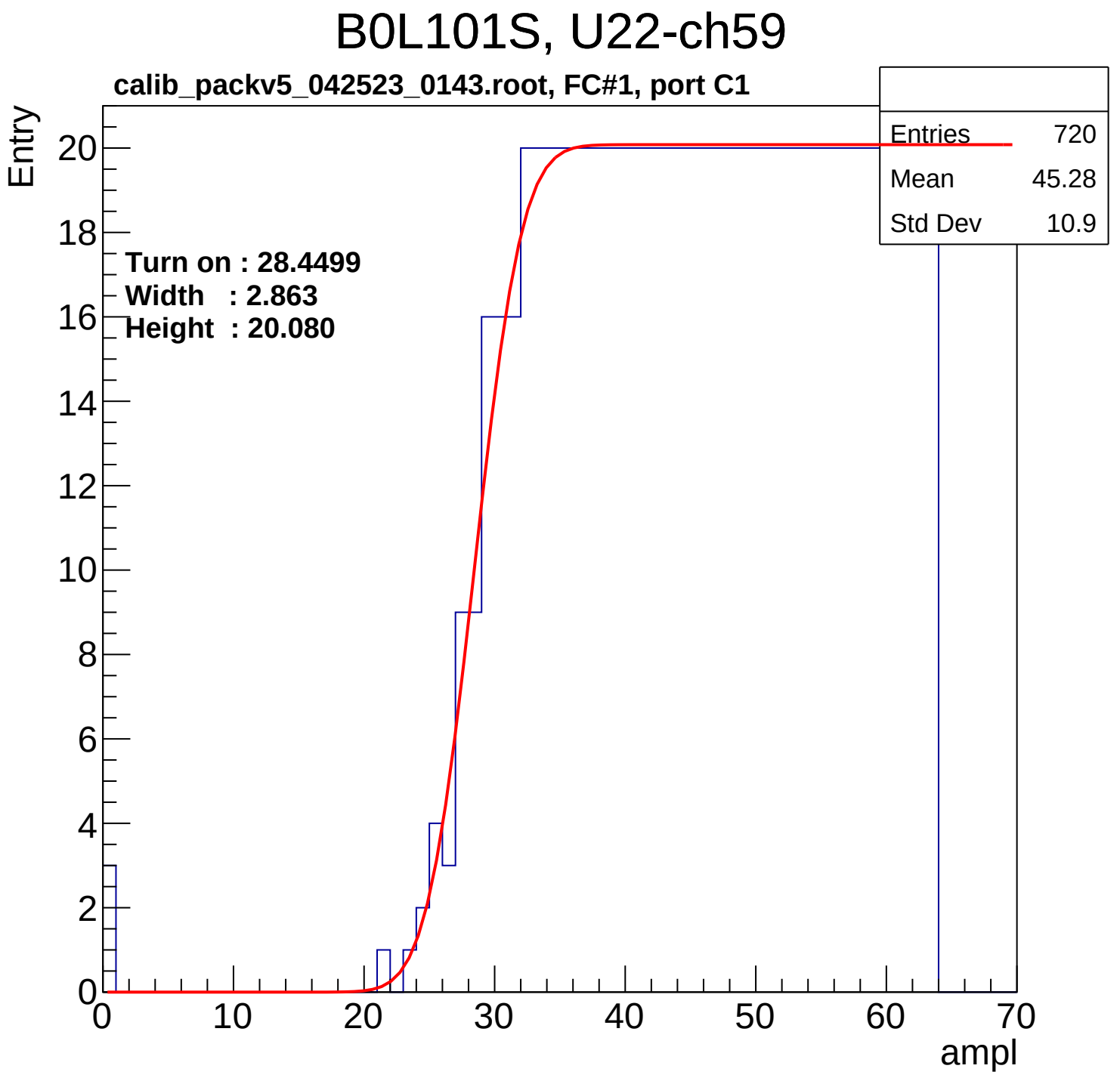

B0L101S, U22-ch54
calib_packv5_042523_0143.root, FC#1, port C1
Entries 725
Mean 45.13
Std Dev 11.06
Turn on : 27.9694
Width : 2.331
Height : 19.894
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

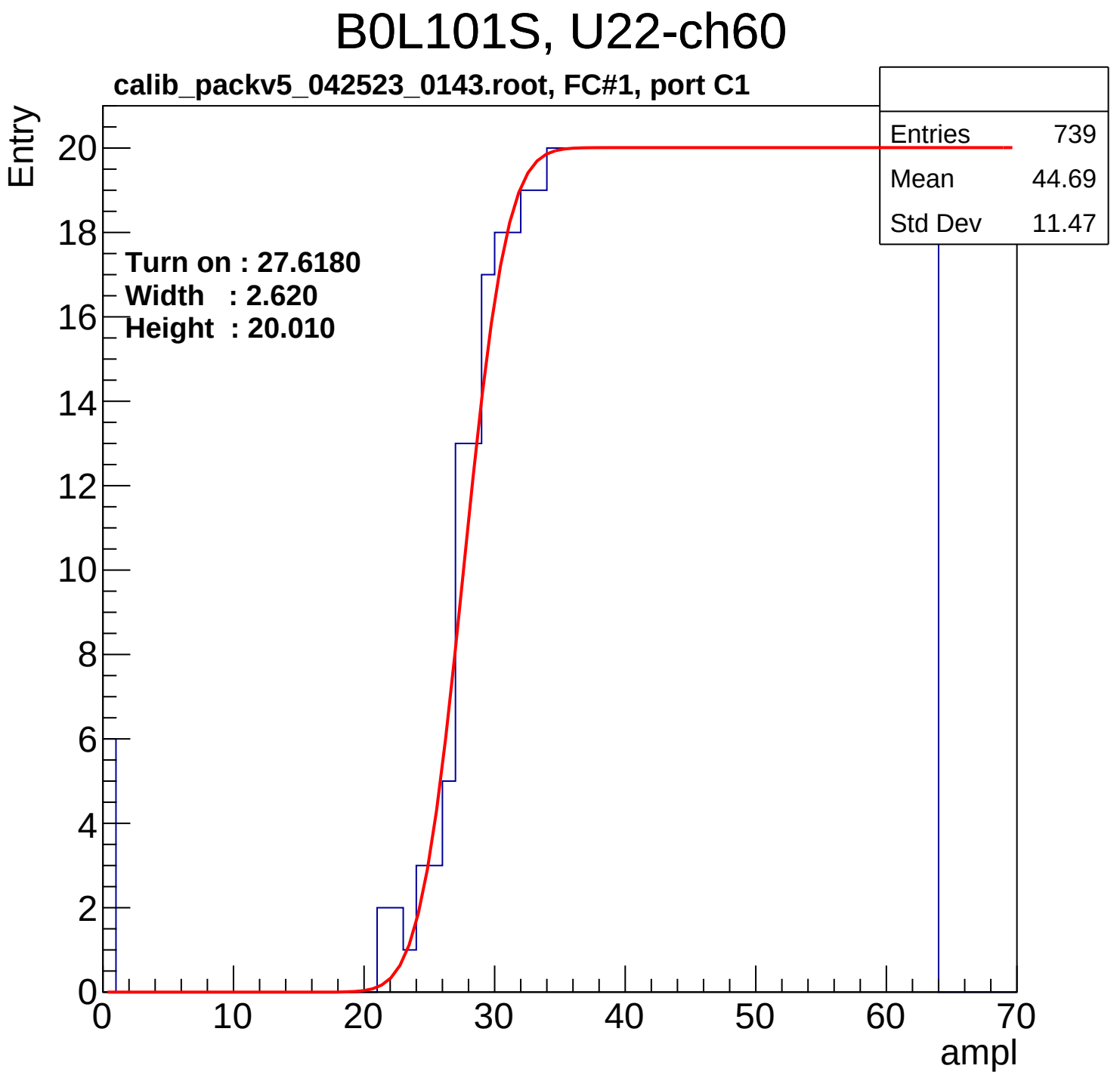

B0L101S, U22-ch55
calib_packv5_042523_0143.root, FC#1, port C1
Entries 719
Mean 45.28
Std Dev 10.92
Turn on : 27.9533
Width : 2.500
Height : 19.799
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

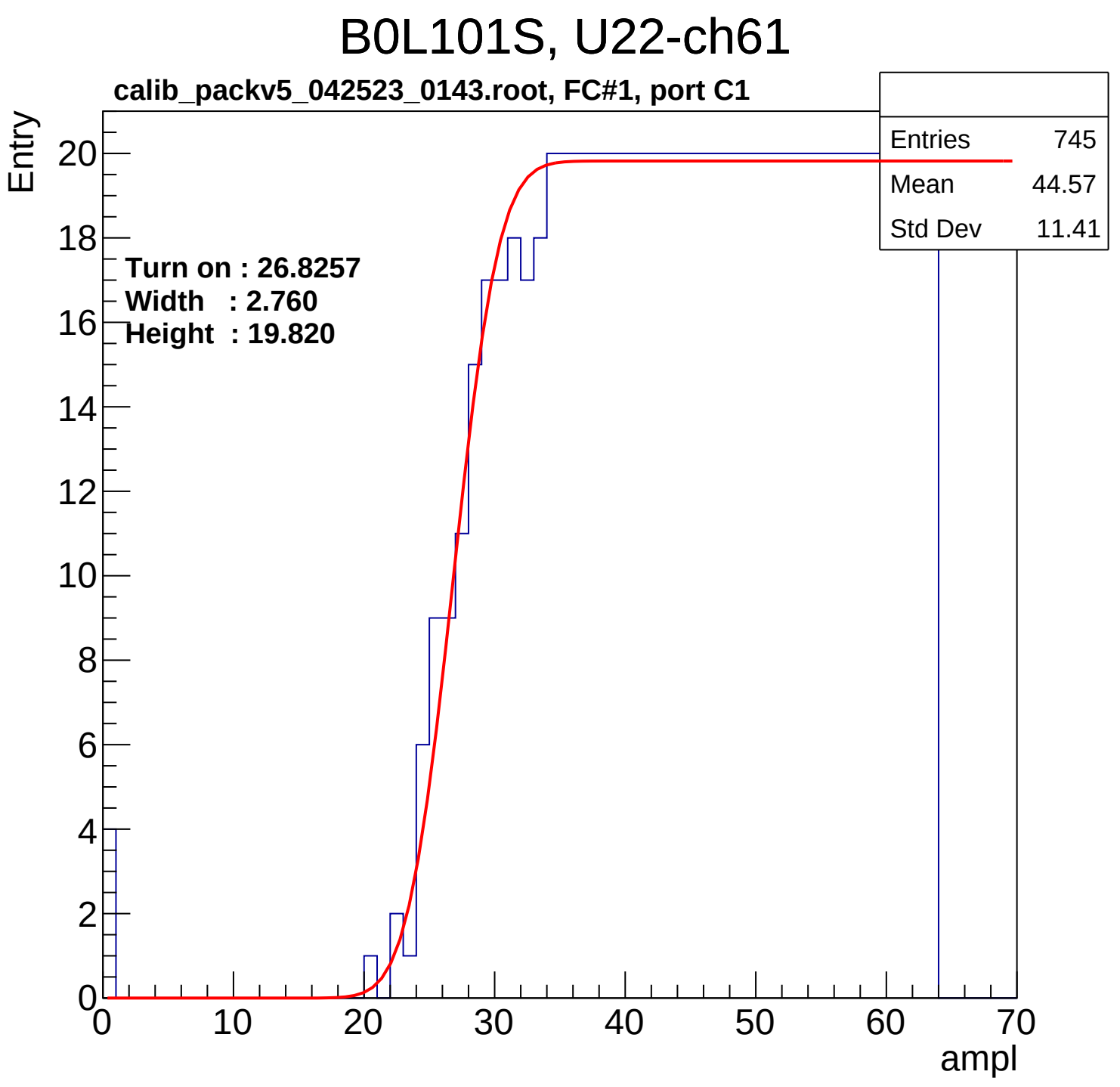

B0L101S, U22-ch56
calib_packv5_042523_0143.root, FC#1, port C1
Entries 782
Mean 43.66
Std Dev 11.91
Turn on : 25.6315
Width : 3.678
Height : 20.094
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

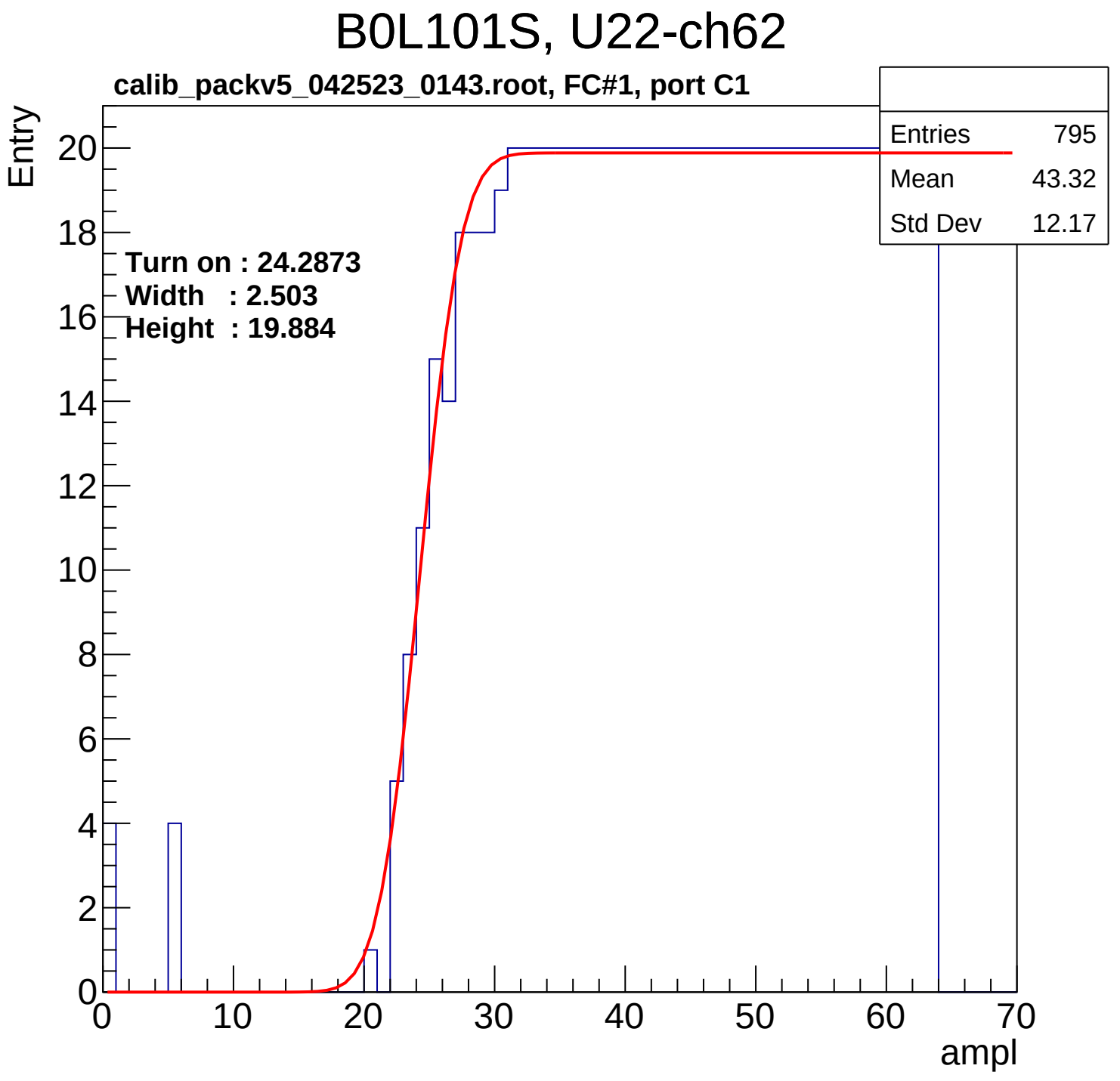

B0L101S, U22-ch57
calib_packv5_042523_0143.root, FC#1, port C1
Entries 729
Mean 45.09
Std Dev 10.93
Turn on : 28.3594
Width : 2.616
Height : 20.123
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

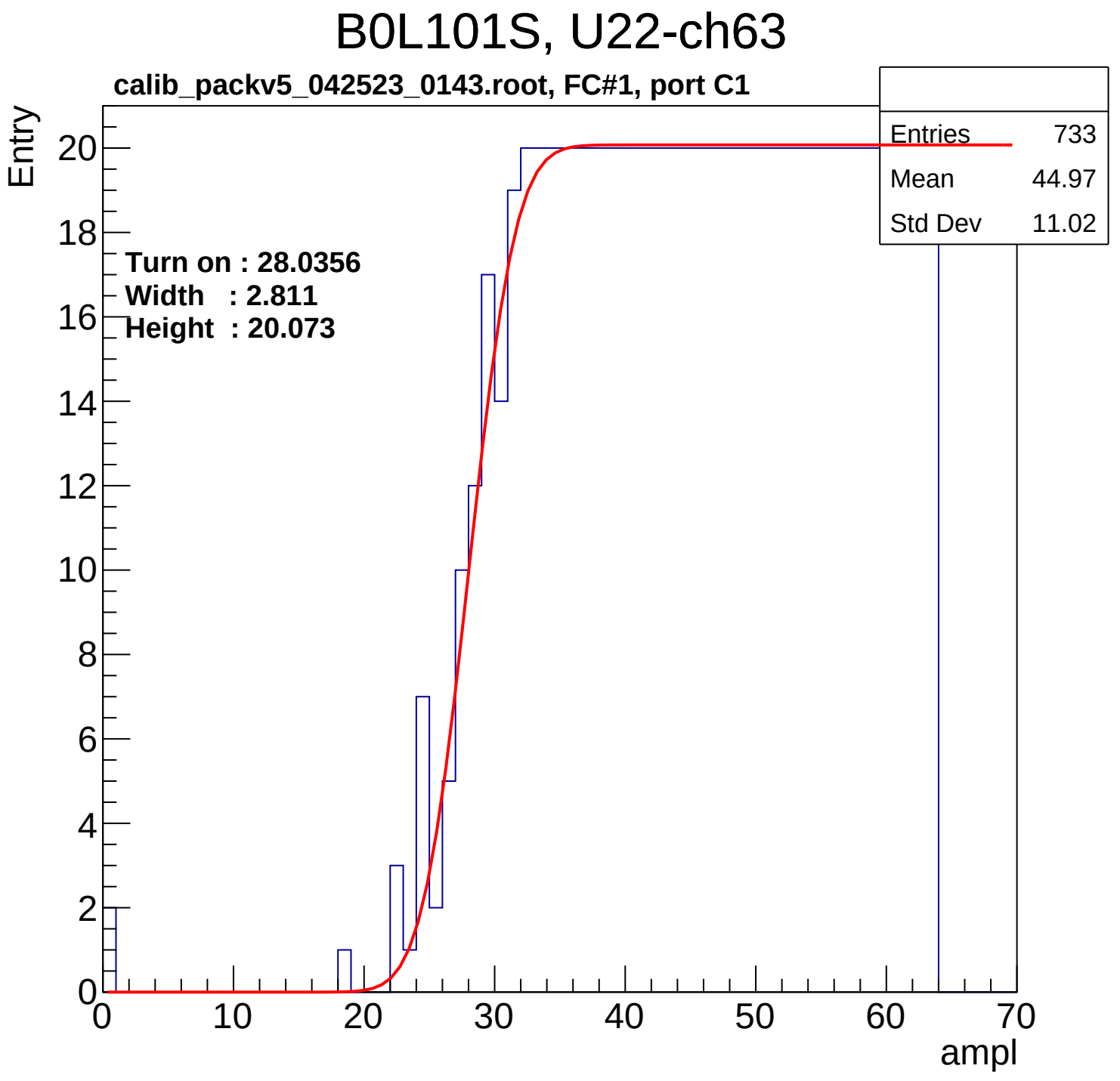

B0L101S, U22-ch58
calib_packv5_042523_0143.root, FC#1, port C1
Entries 803
Mean 43.17
Std Dev 12.23
Turn on : 25.1728
Width : 2.901
Height : 20.127
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70

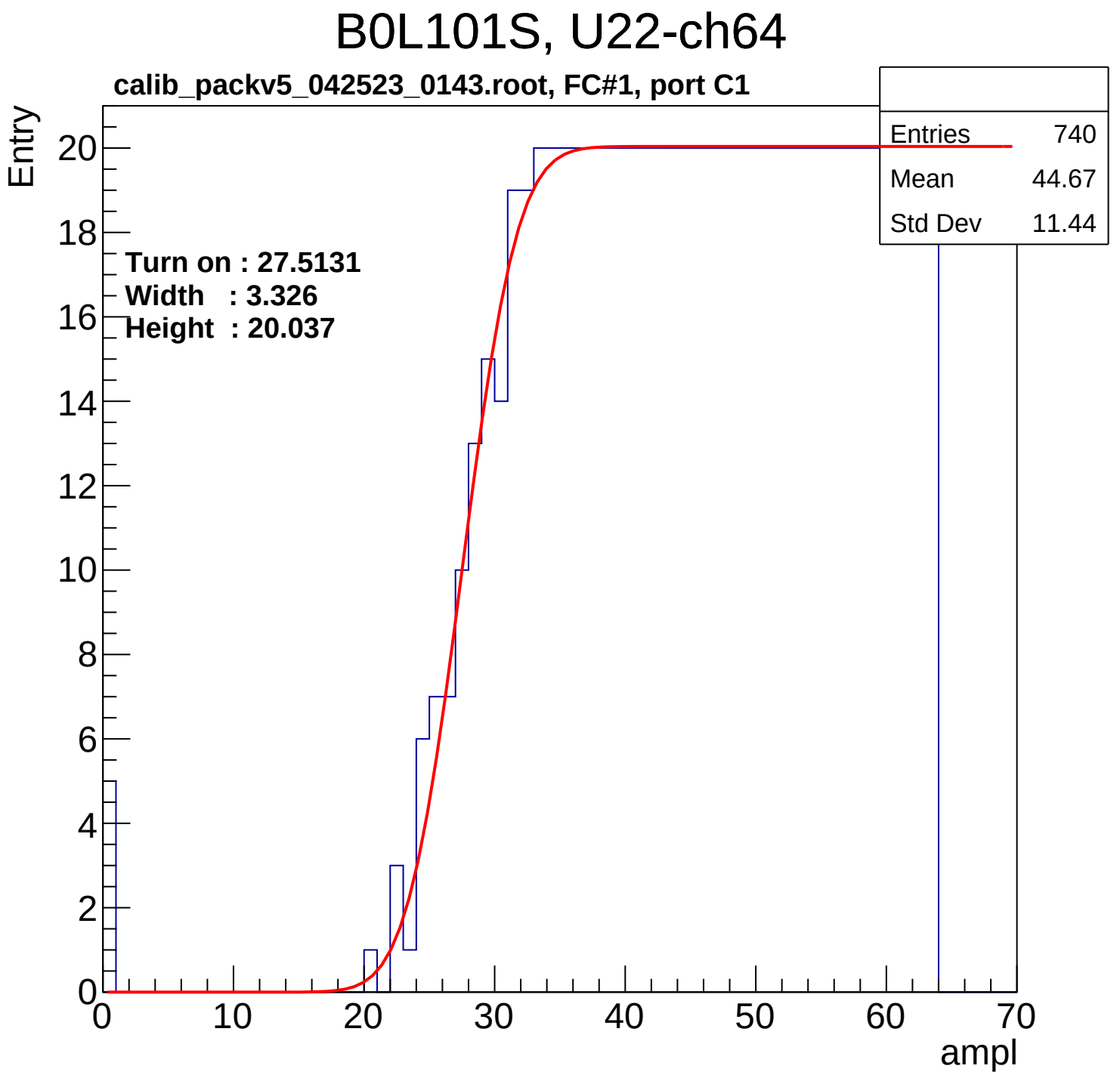

B0L101S, U22-ch59
calib_packv5_042523_0143.root, FC#1, port C1
Entries 720
Mean 45.28
Std Dev 10.9
Turn on : 28.4499
Width : 2.863
Height : 20.080
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

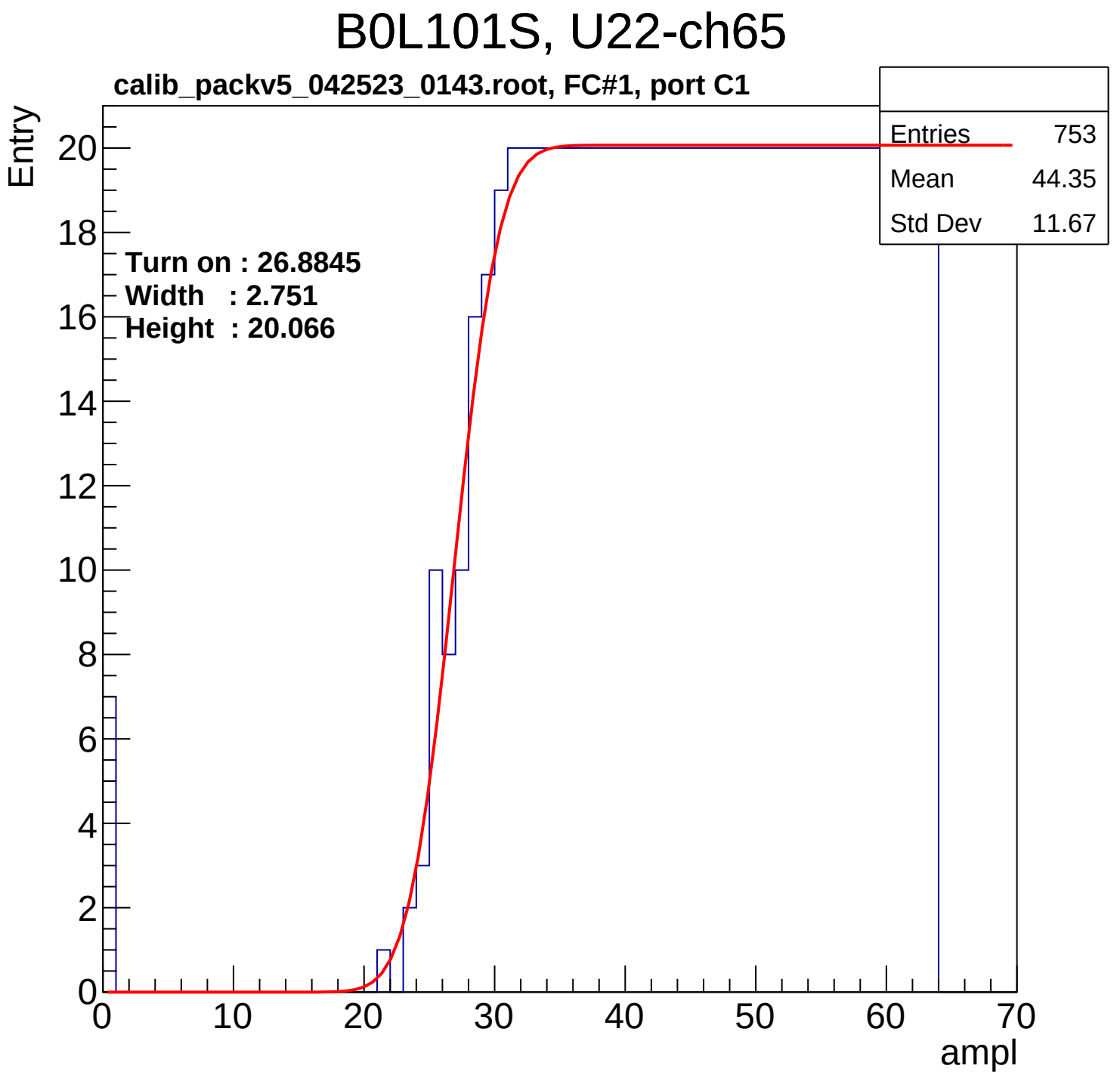

B0L101S, U22-ch60
calib_packv5_042523_0143.root, FC#1, port C1
Entries 739
Mean 44.69
Std Dev 11.47
Turn on : 27.6180
Width : 2.620
Height : 20.010
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

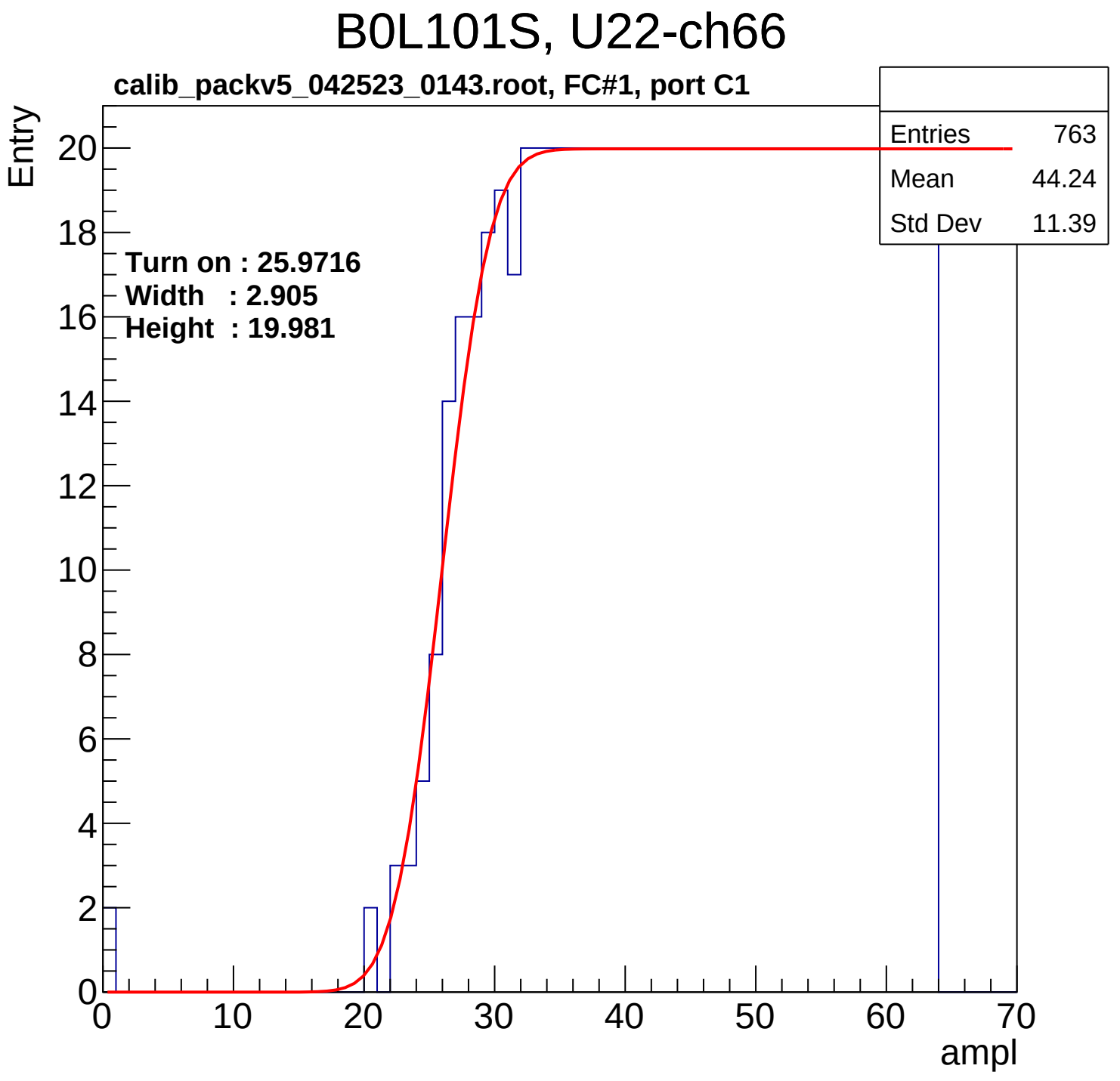

B0L101S, U22-ch61
calib_packv5_042523_0143.root, FC#1, port C1
Entries 745
Mean 44.57
Std Dev 11.41
Turn on : 26.8257
Width : 2.760
Height : 19.820
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

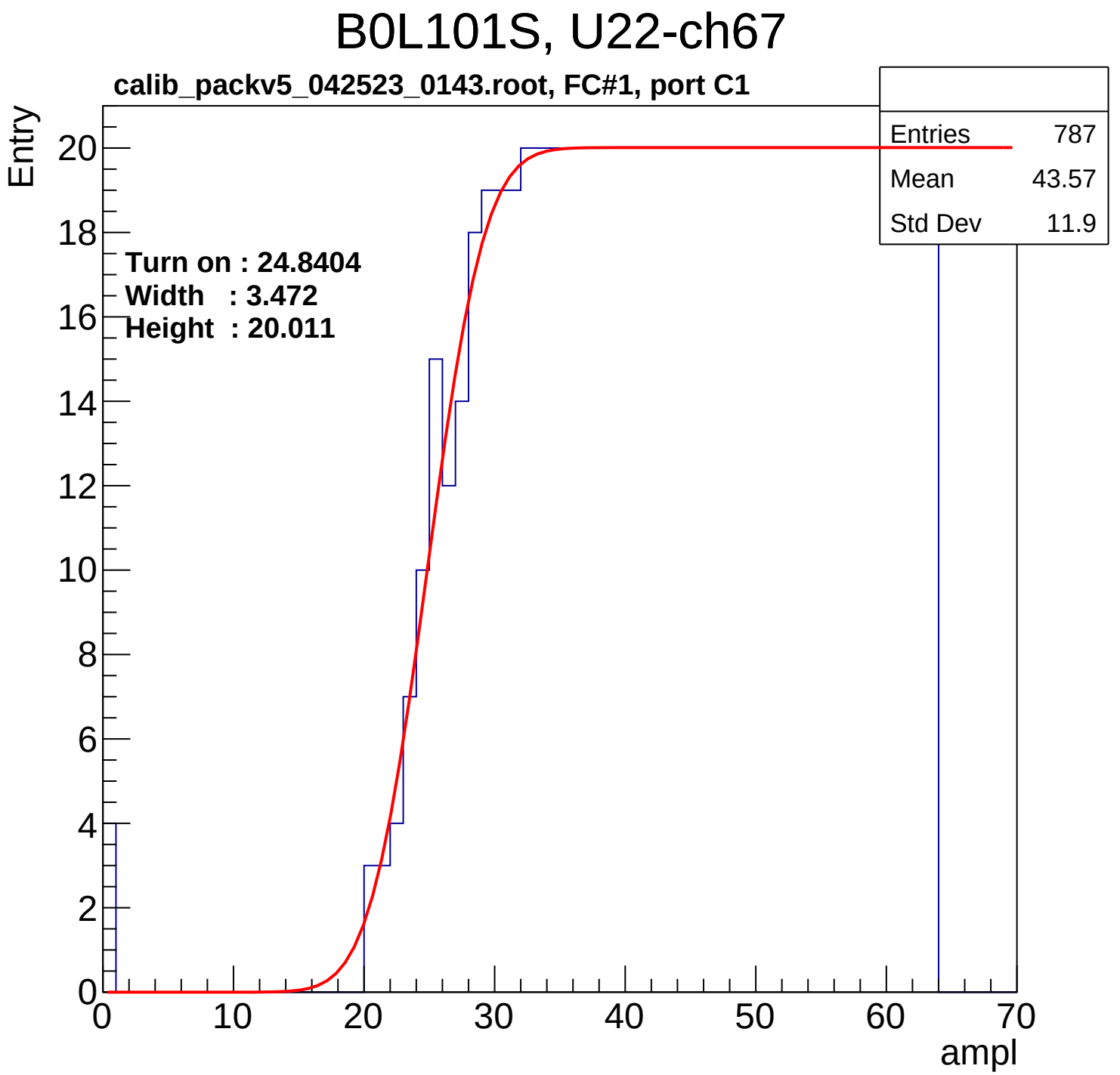

B0L101S, U22-ch62
calib_packv5_042523_0143.root, FC#1, port C1
Entries 795
Mean 43.32
Std Dev 12.17
Turn on : 24.2873
Width : 2.503
Height : 19.884
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

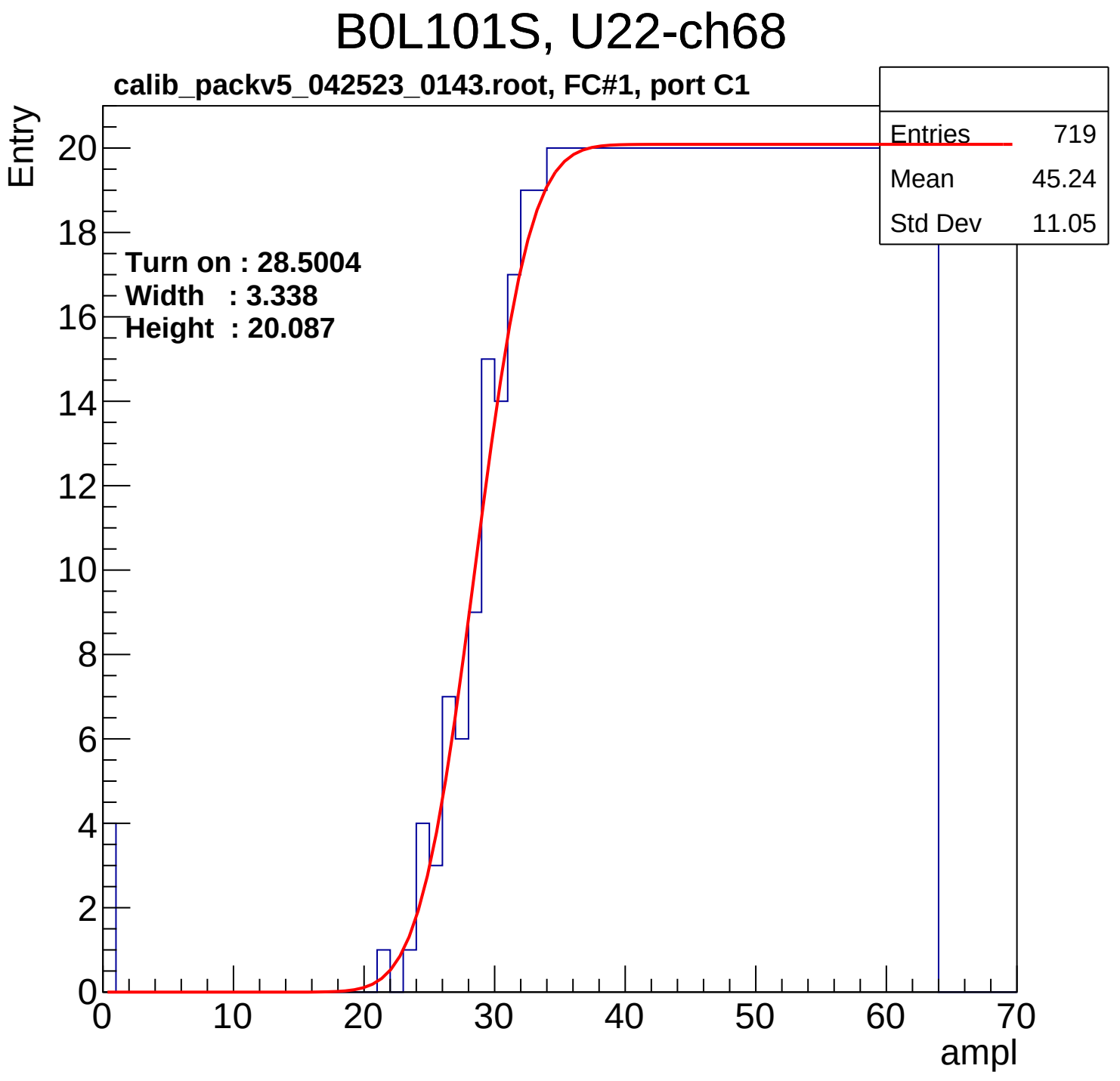

B0L101S, U22-ch63
calib_packv5_042523_0143.root, FC#1, port C1
Entries 733
Mean 44.97
Std Dev 11.02
Turn on : 28.0356
Width : 2.811
Height : 20.073
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

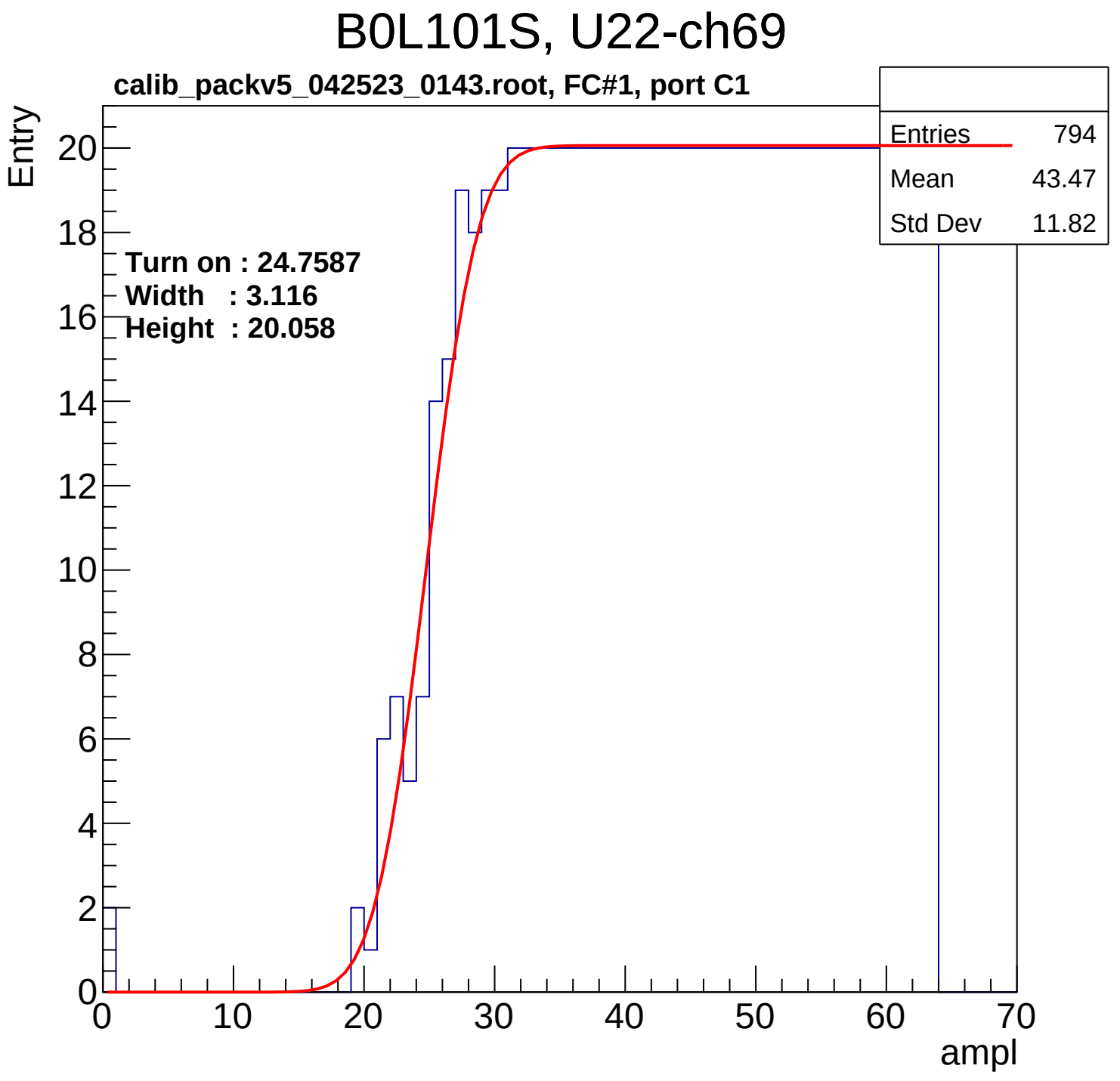

B0L101S, U22-ch64
calib_packv5_042523_0143.root, FC#1, port C1
Entries 740
Mean 44.67
Std Dev 11.44
Turn on : 27.5131
Width : 3.326
Height : 20.037
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

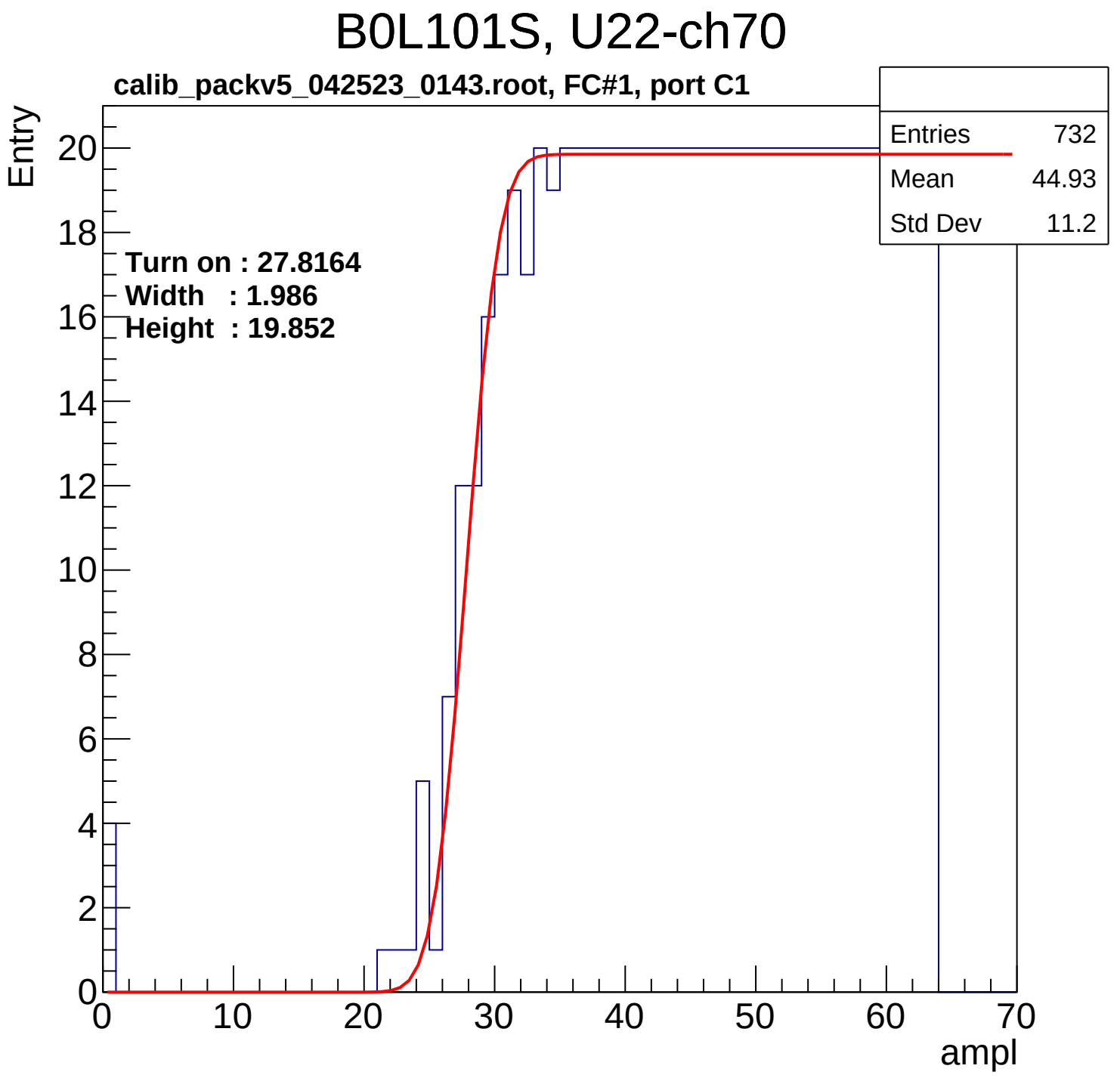

B0L101S, U22-ch65
calib_packv5_042523_0143.root, FC#1, port C1
Entries 753
Mean 44.35
Std Dev 11.67
Turn on : 26.8845
Width : 2.751
Height : 20.066
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

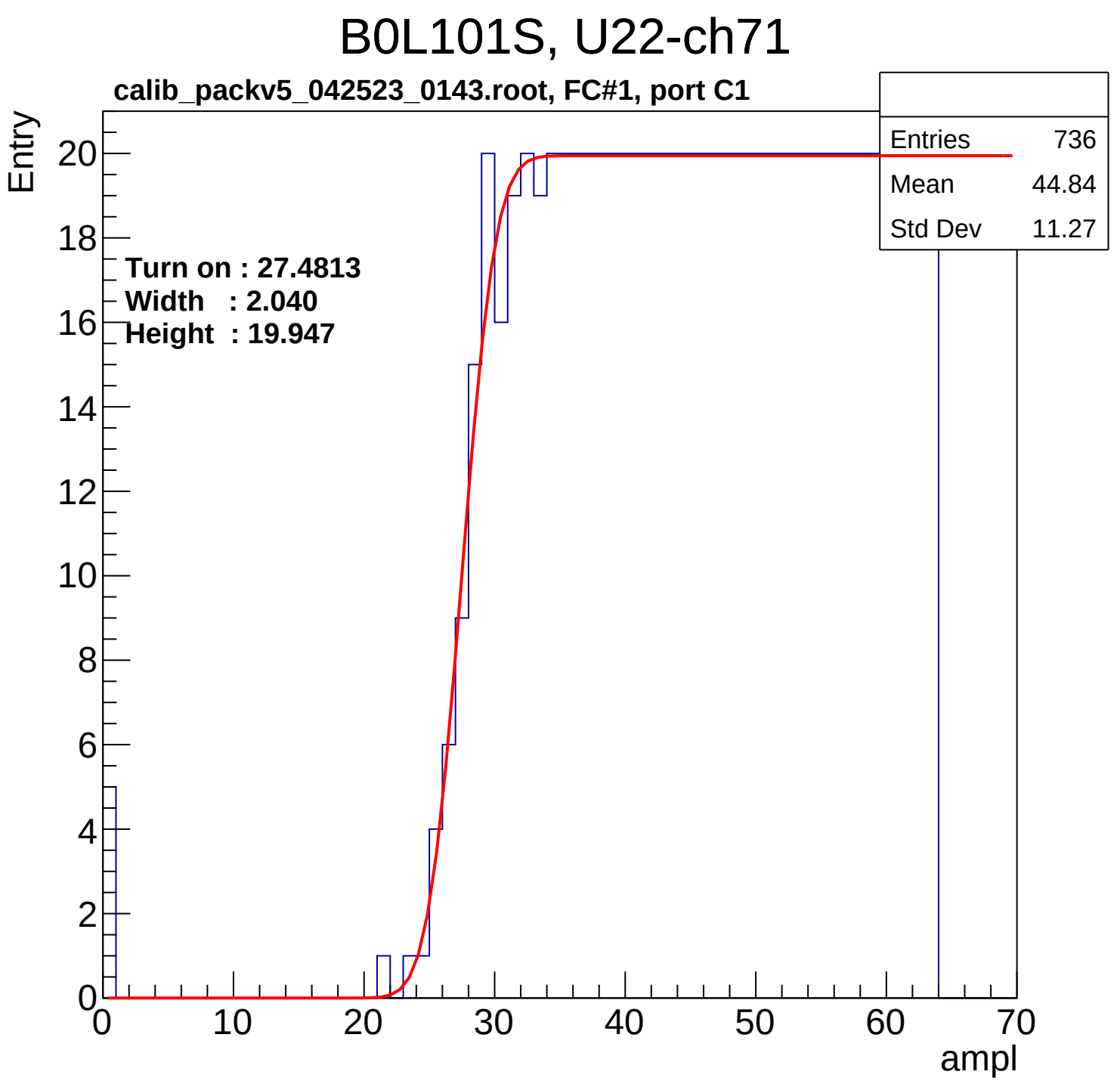

B0L101S, U22-ch66
calib_packv5_042523_0143.root, FC#1, port C1
Entries 763
Mean 44.24
Std Dev 11.39
Turn on : 25.9716
Width : 2.905
Height : 19.981
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

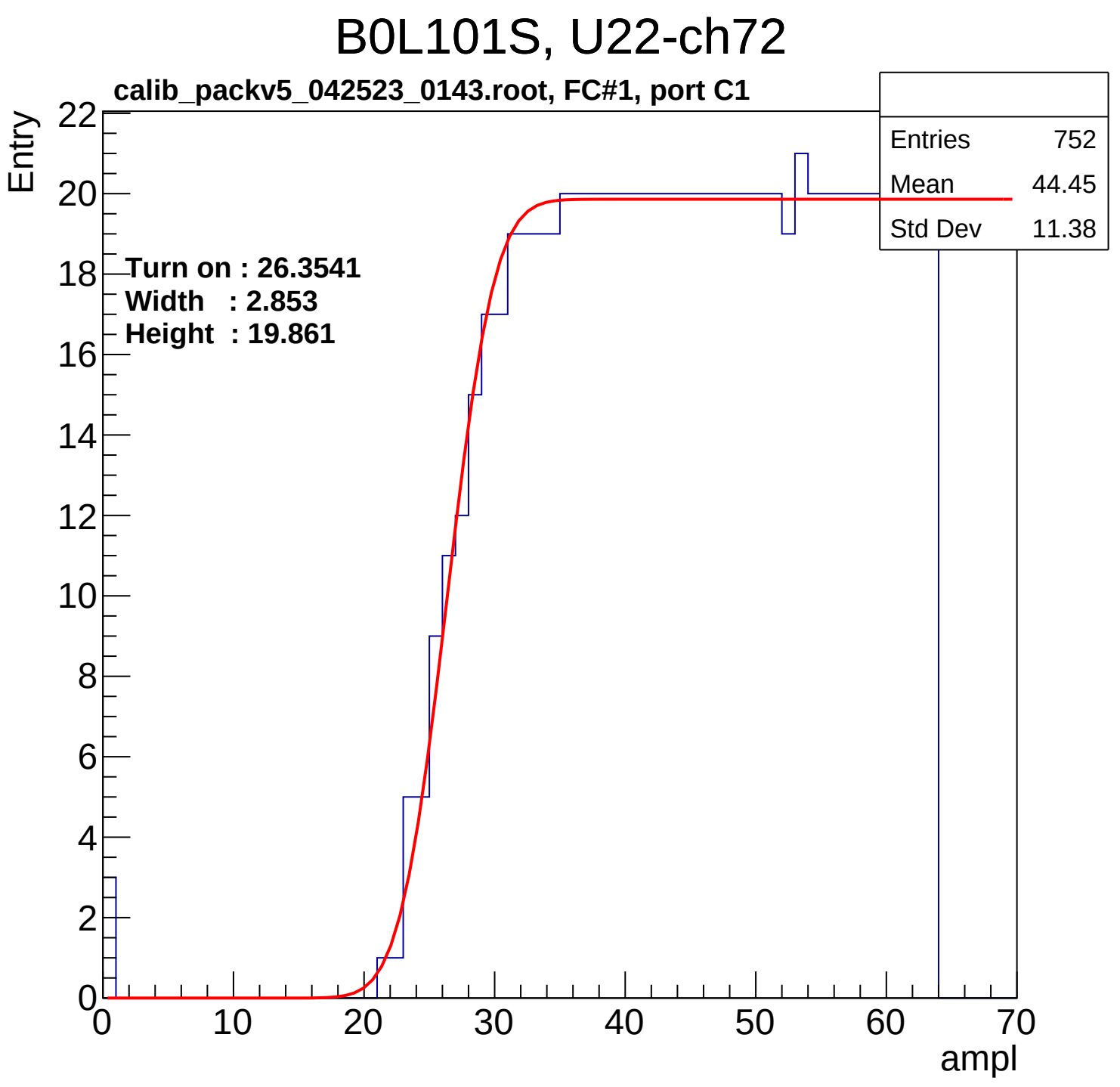

B0L101S, U22-ch67
calib_packv5_042523_0143.root, FC#1, port C1
Entries 787
Mean 43.57
Std Dev 11.9
Turn on : 24.8404
Width : 3.472
Height : 20.011
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

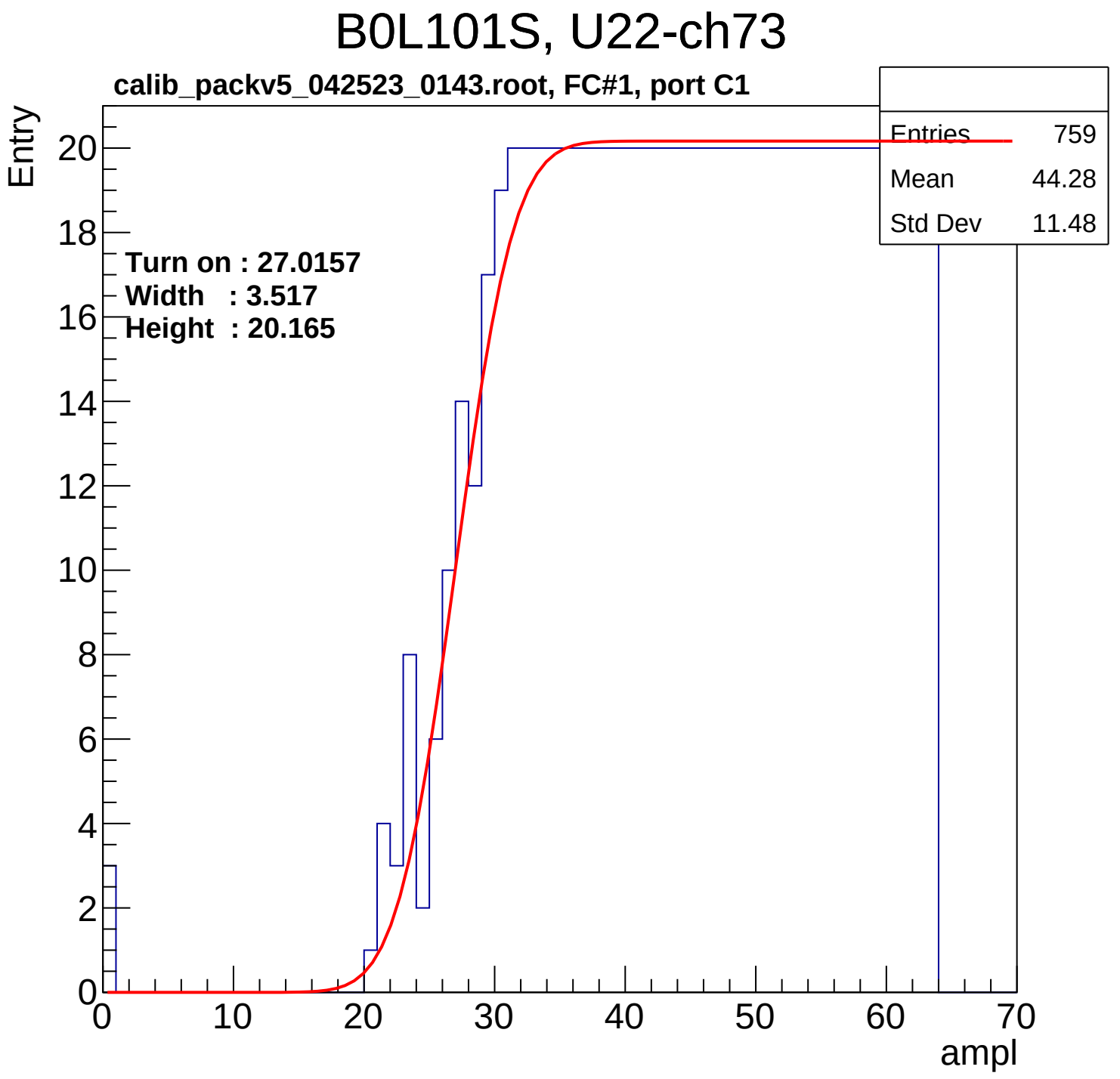

B0L101S, U22-ch68
calib_packv5_042523_0143.root, FC#1, port C1
Entries 719
Mean 45.24
Std Dev 11.05
Turn on : 28.5004
Width : 3.338
Height : 20.087
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

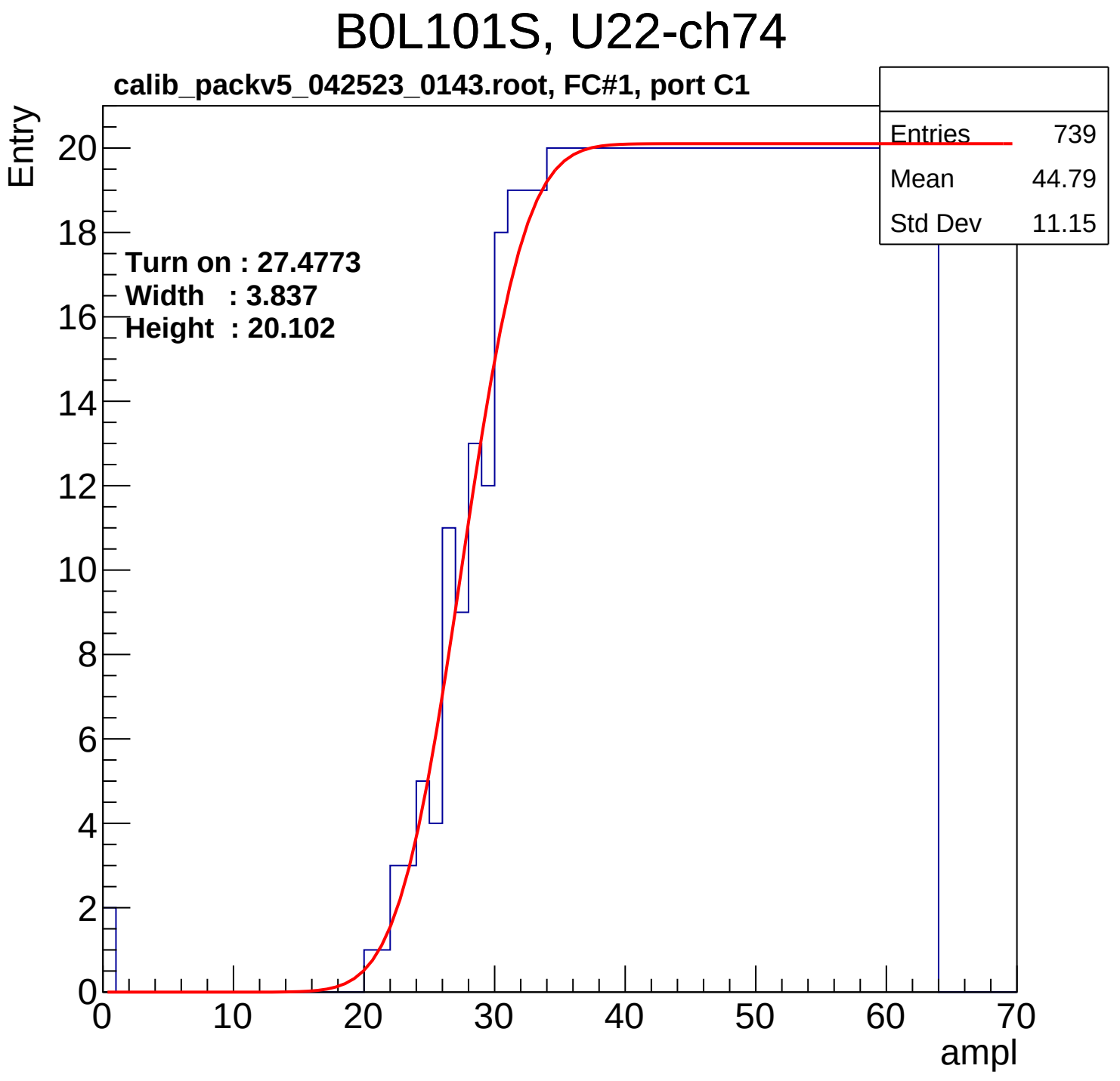

B0L101S, U22-ch69
calib_packv5_042523_0143.root, FC#1, port C1
Entries 794
Mean 43.47
Std Dev 11.82
Turn on : 24.7587
Width : 3.116
Height : 20.058
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

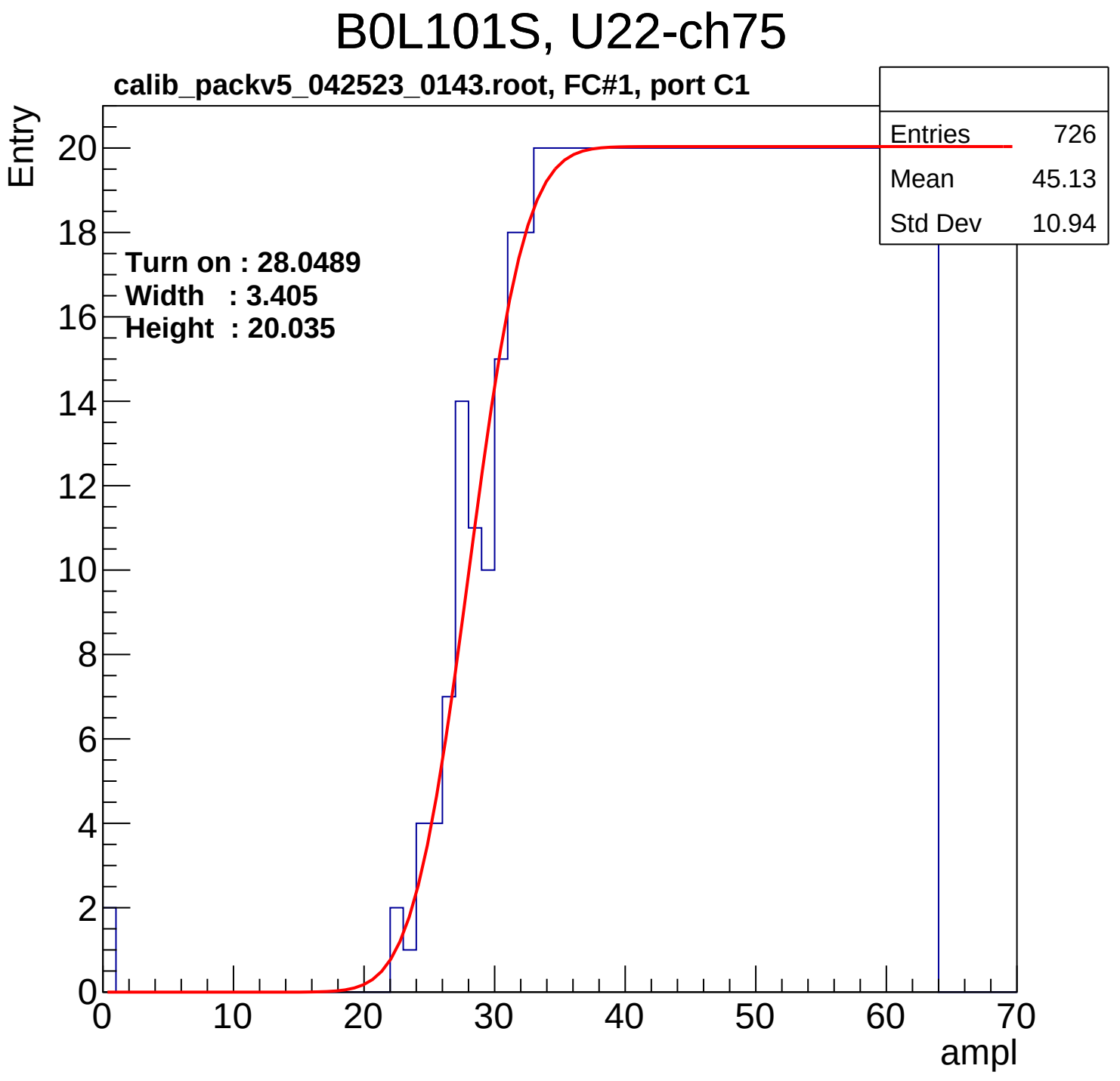

B0L101S, U22-ch70
calib_packv5_042523_0143.root, FC#1, port C1
Entries 732
Mean 44.93
Std Dev 11.2
Turn on : 27.8164
Width : 1.986
Height : 19.852
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

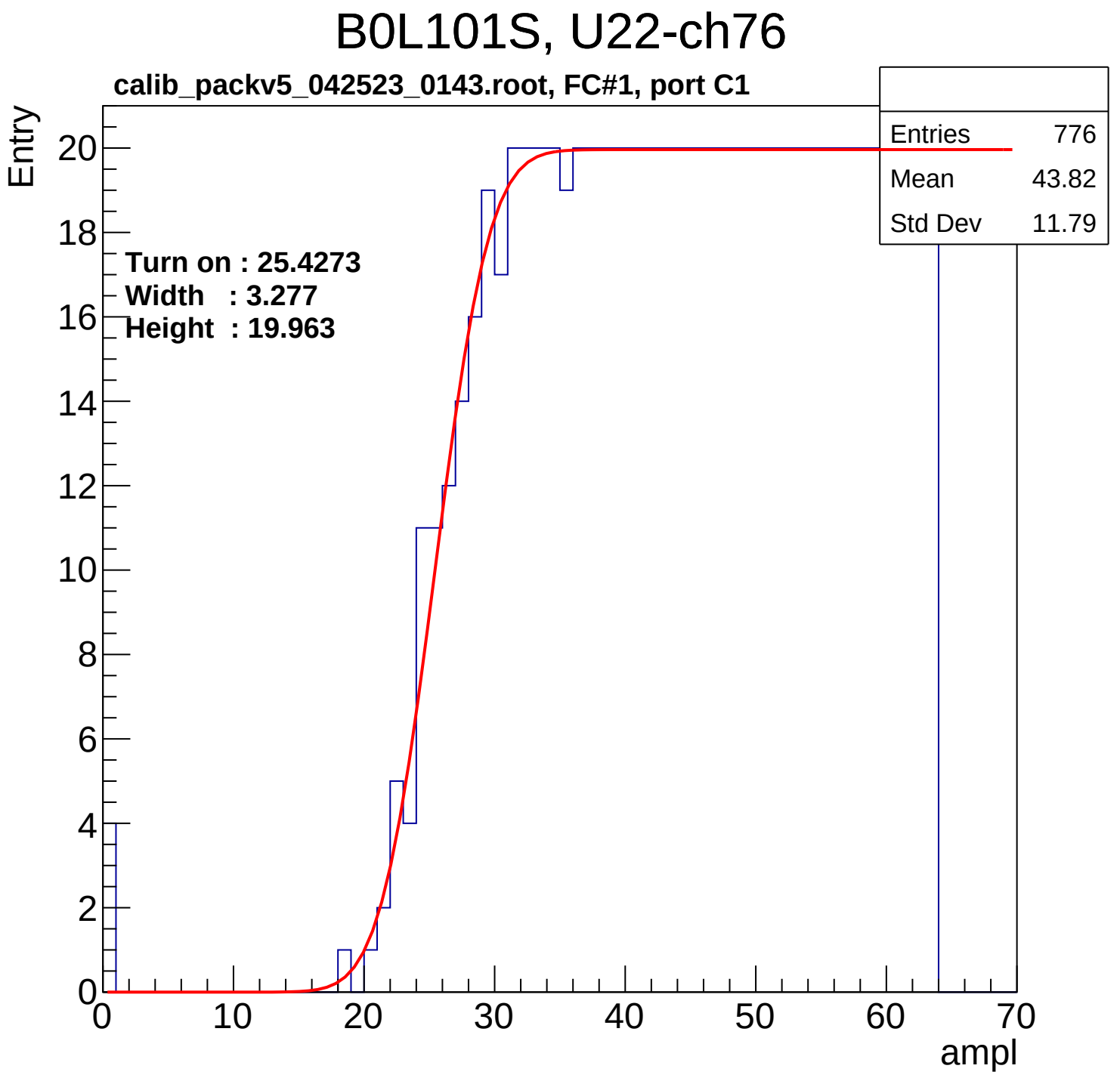

B0L101S, U22-ch71
calib_packv5_042523_0143.root, FC#1, port C1
Entries 736
Mean 44.84
Std Dev 11.27
Turn on : 27.4813
Width : 2.040
Height : 19.947
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

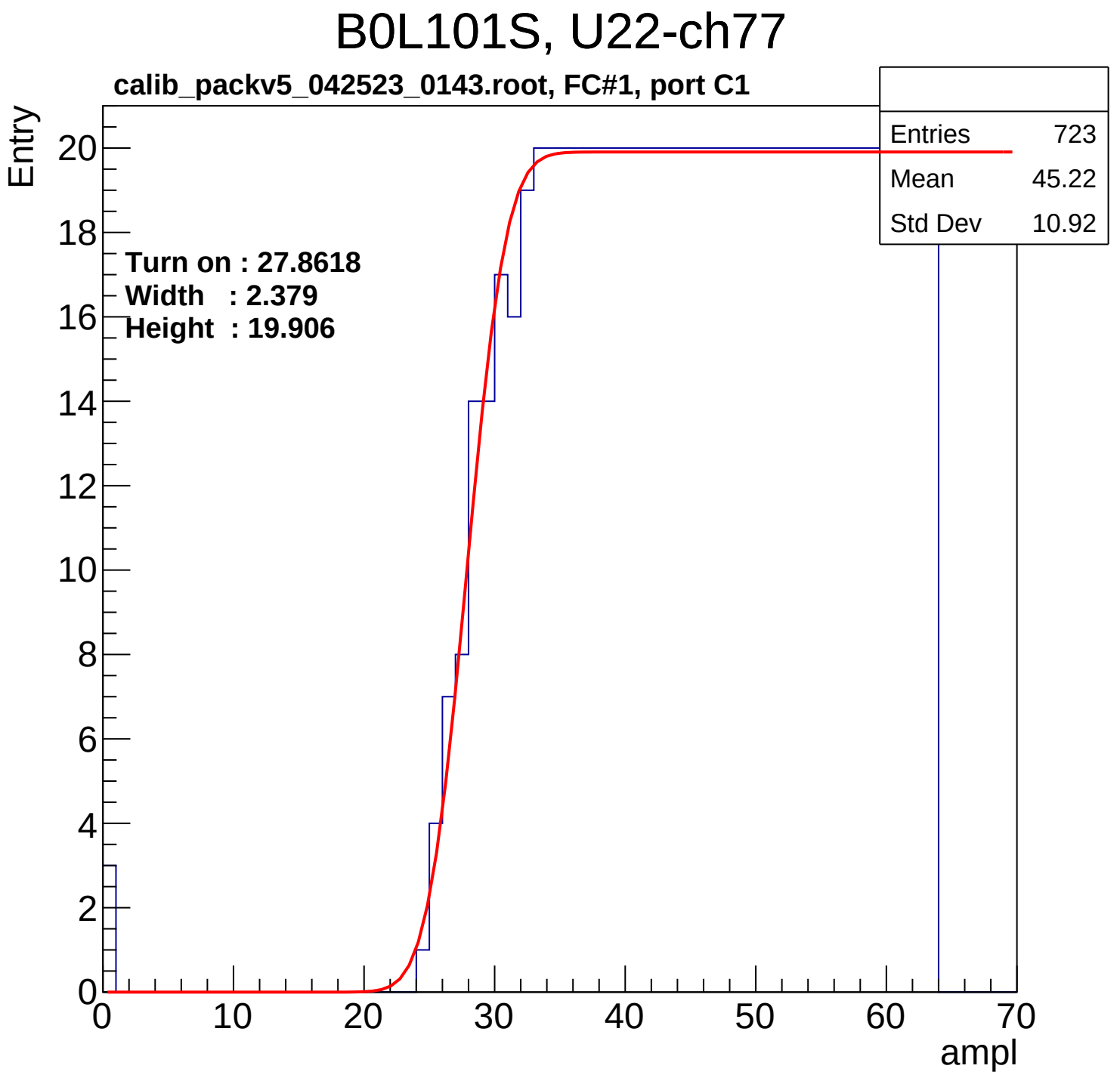

B0L101S, U22-ch72
calib_packv5_042523_0143.root, FC#1, port C1
Entries 752
Mean 44.45
Std Dev 11.38
Turn on : 26.3541
Width : 2.853
Height : 19.861
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70

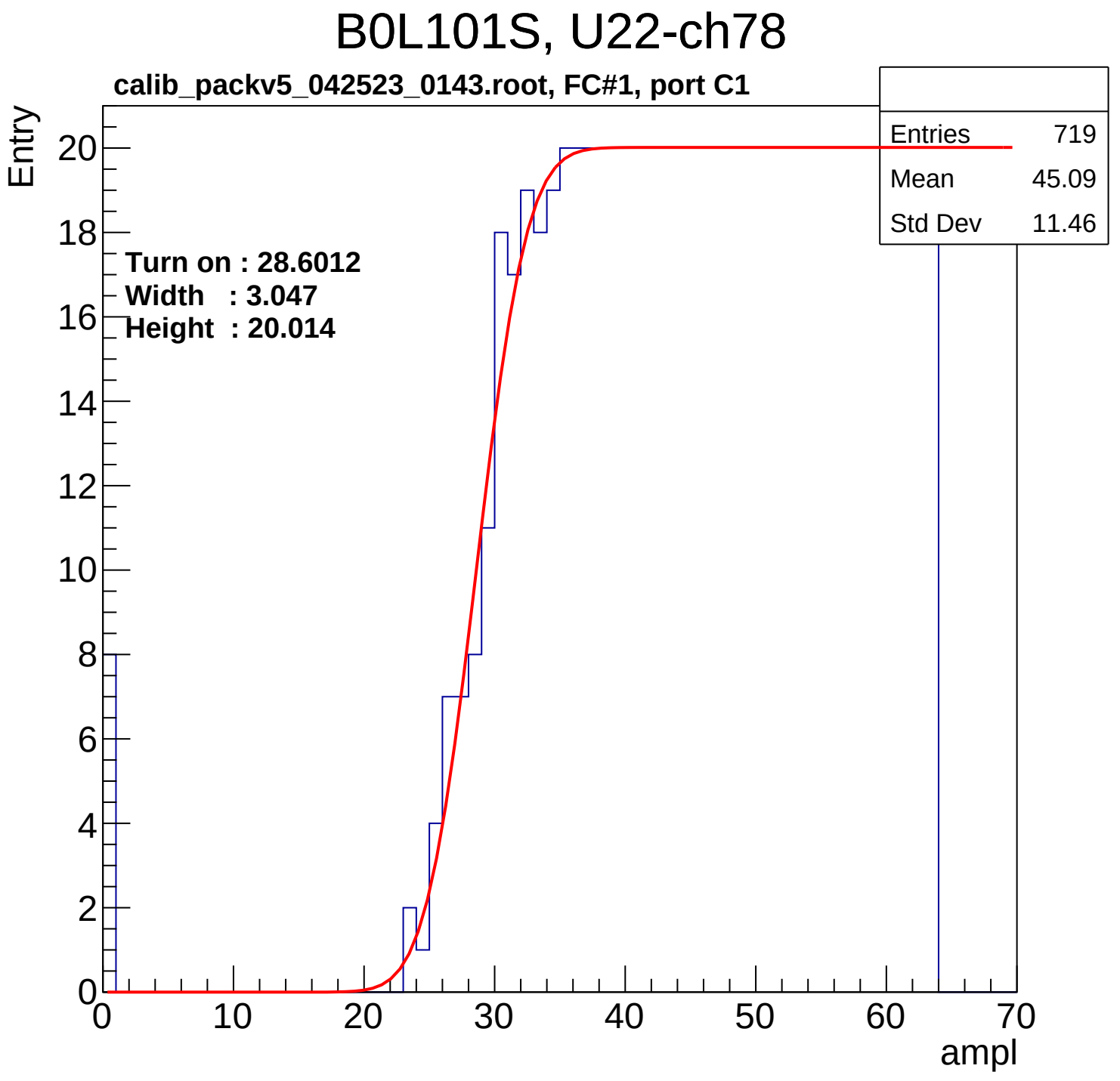

B0L101S, U22-ch73
calib_packv5_042523_0143.root, FC#1, port C1
Entries 759
Mean 44.28
Std Dev 11.48
Turn on : 27.0157
Width : 3.517
Height : 20.165
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

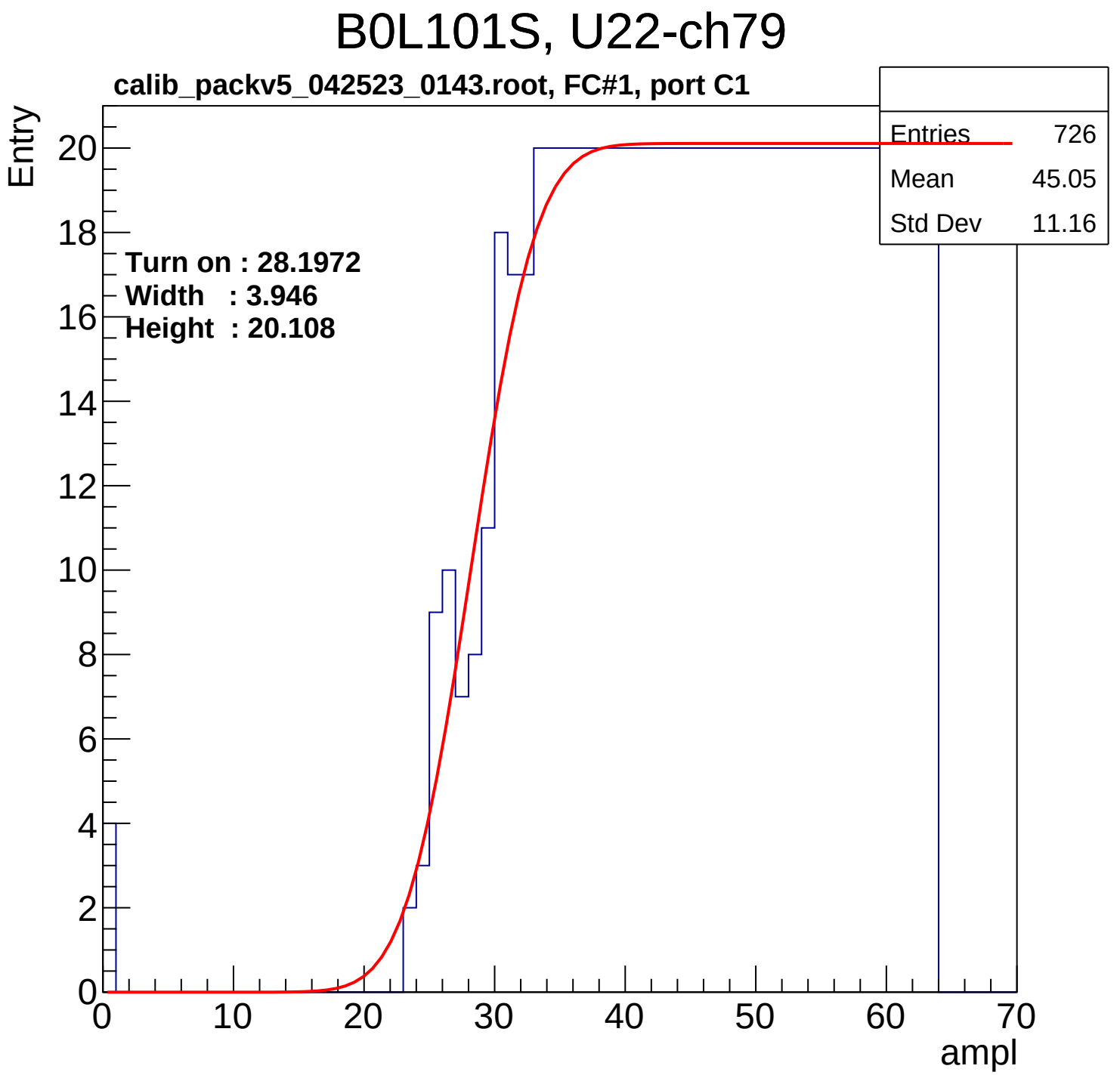

B0L101S, U22-ch74
calib_packv5_042523_0143.root, FC#1, port C1
Entries 739
Mean 44.79
Std Dev 11.15
Turn on : 27.4773
Width : 3.837
Height : 20.102
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

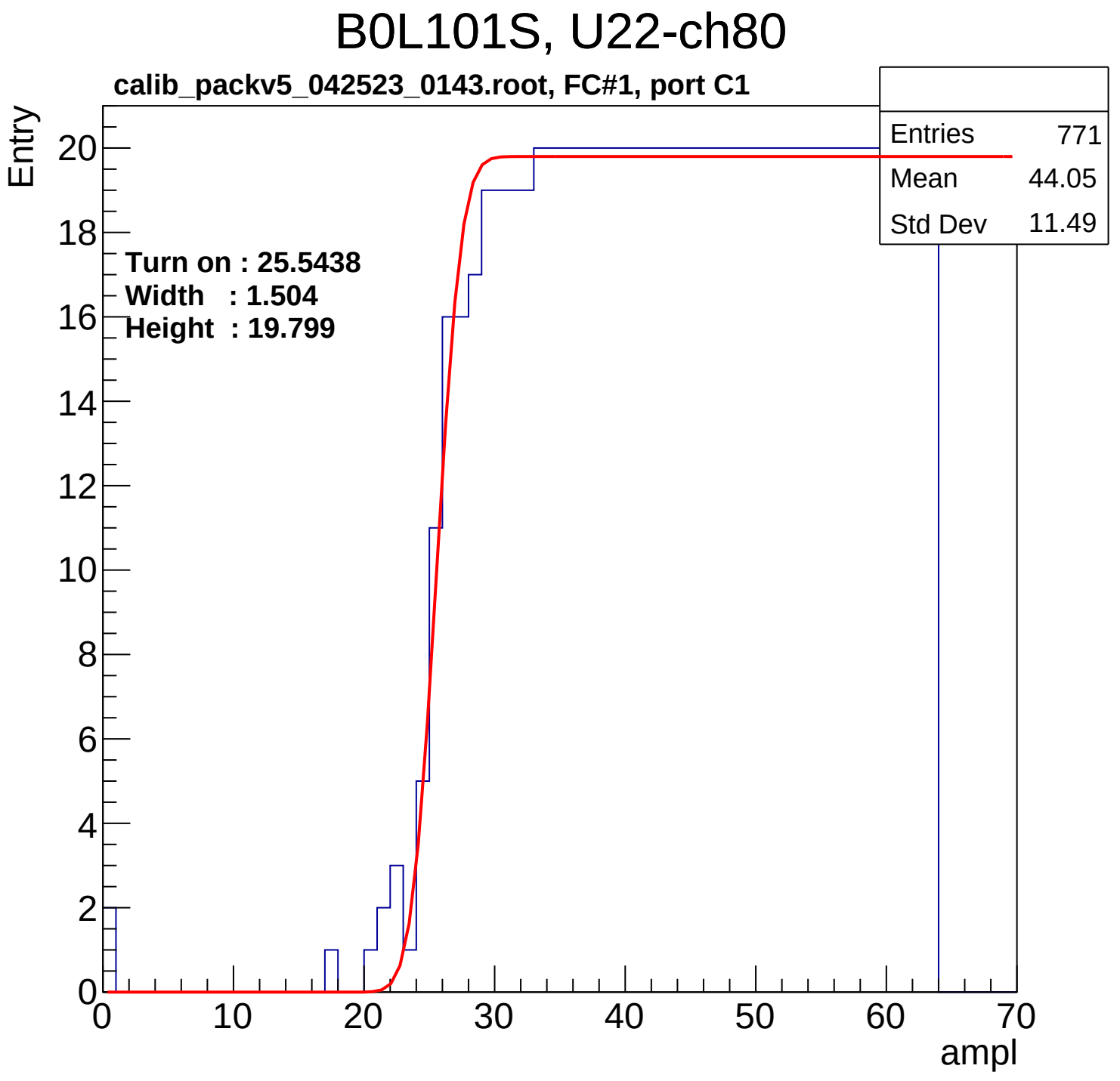

B0L101S, U22-ch75
calib_packv5_042523_0143.root, FC#1, port C1
Entries 726
Mean 45.13
Std Dev 10.94
Turn on : 28.0489
Width : 3.405
Height : 20.035
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

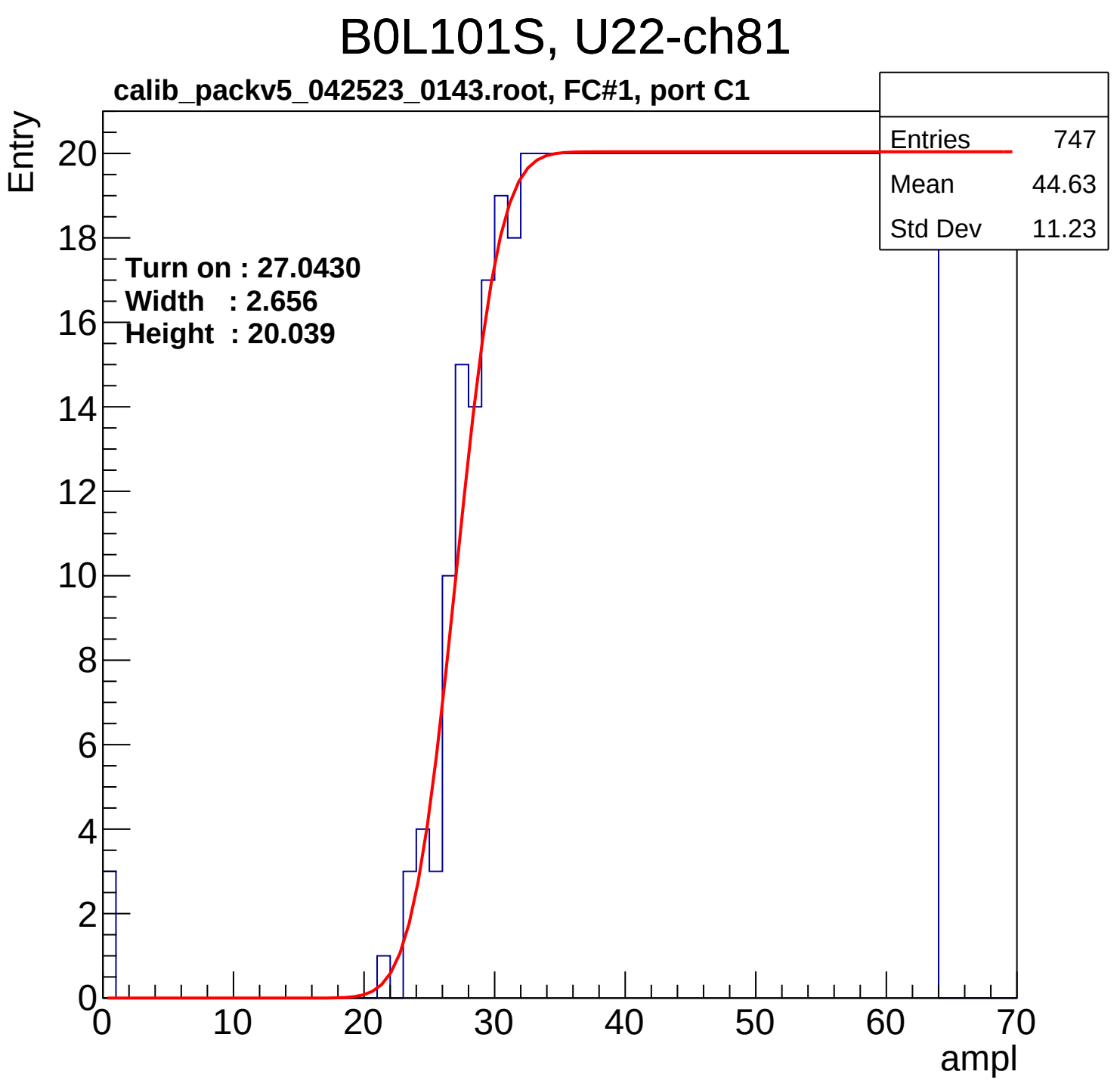

B0L101S, U22-ch76
calib_packv5_042523_0143.root, FC#1, port C1
Entries 776
Mean 43.82
Std Dev 11.79
Turn on : 25.4273
Width : 3.277
Height : 19.963
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

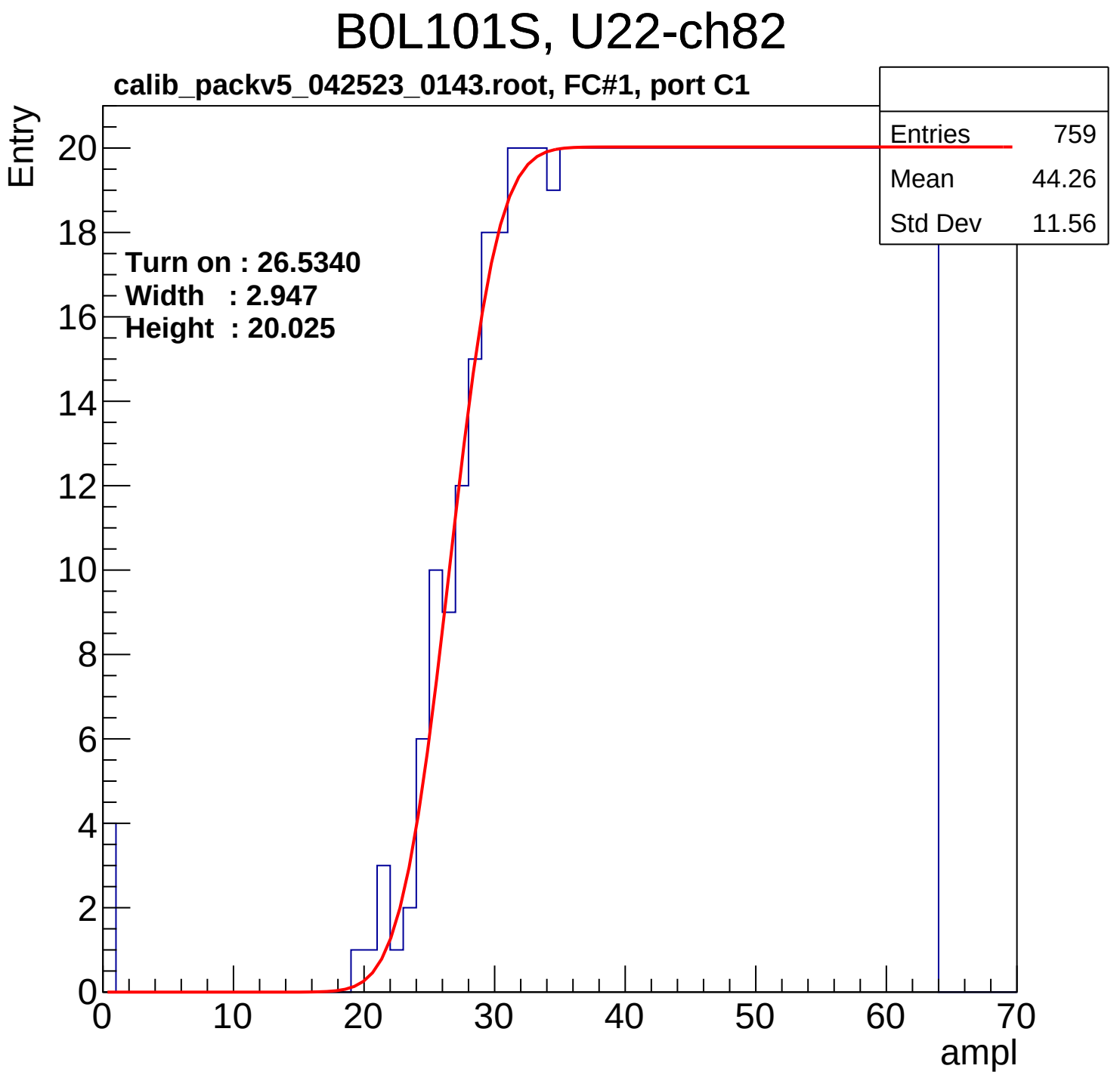

B0L101S, U22-ch77
calib_packv5_042523_0143.root, FC#1, port C1
Entries 723
Mean 45.22
Std Dev 10.92
Turn on : 27.8618
Width : 2.379
Height : 19.906
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

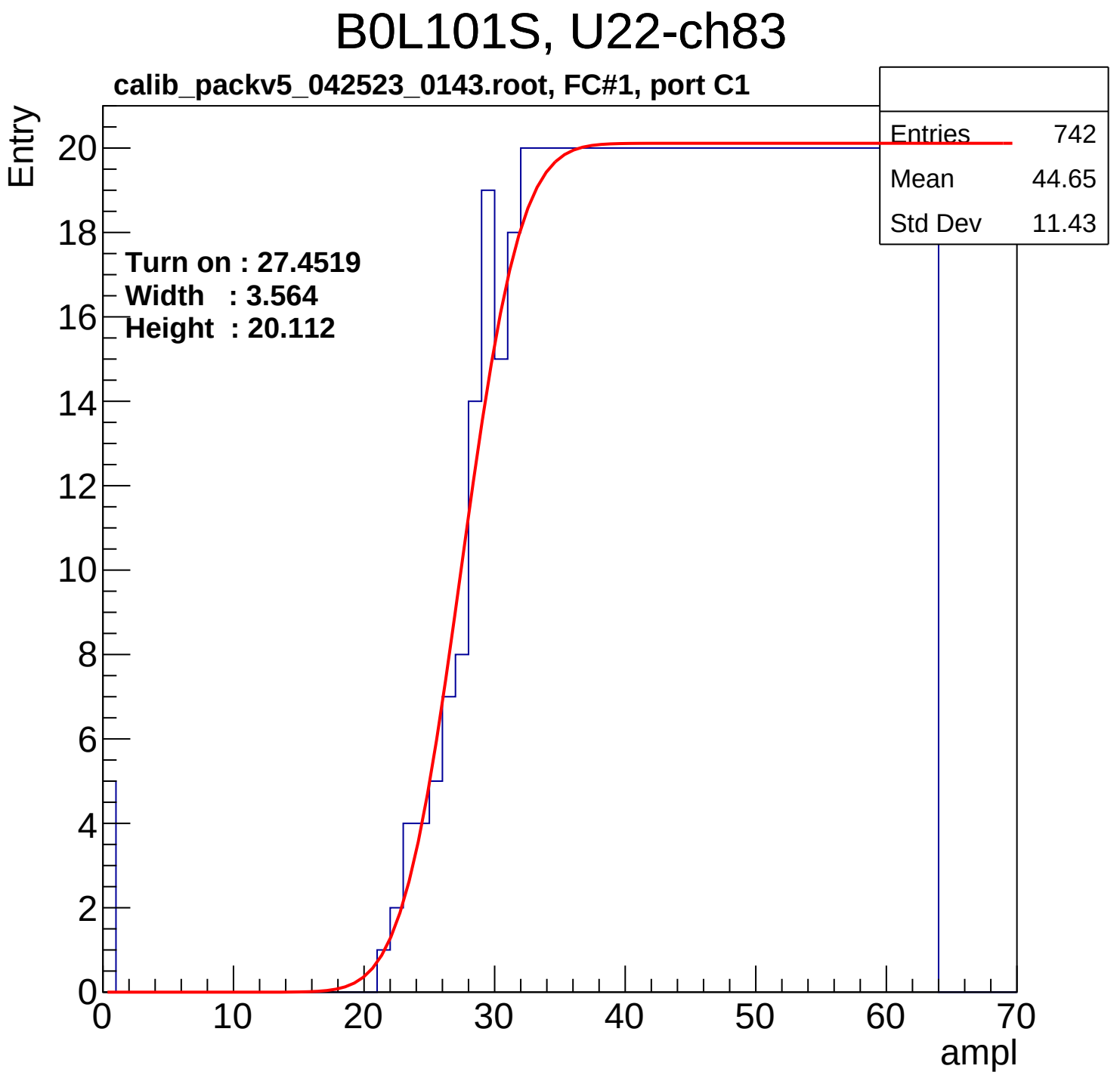

B0L101S, U22-ch78
calib_packv5_042523_0143.root, FC#1, port C1
Entries 719
Mean 45.09
Std Dev 11.46
Turn on : 28.6012
Width : 3.047
Height : 20.014
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

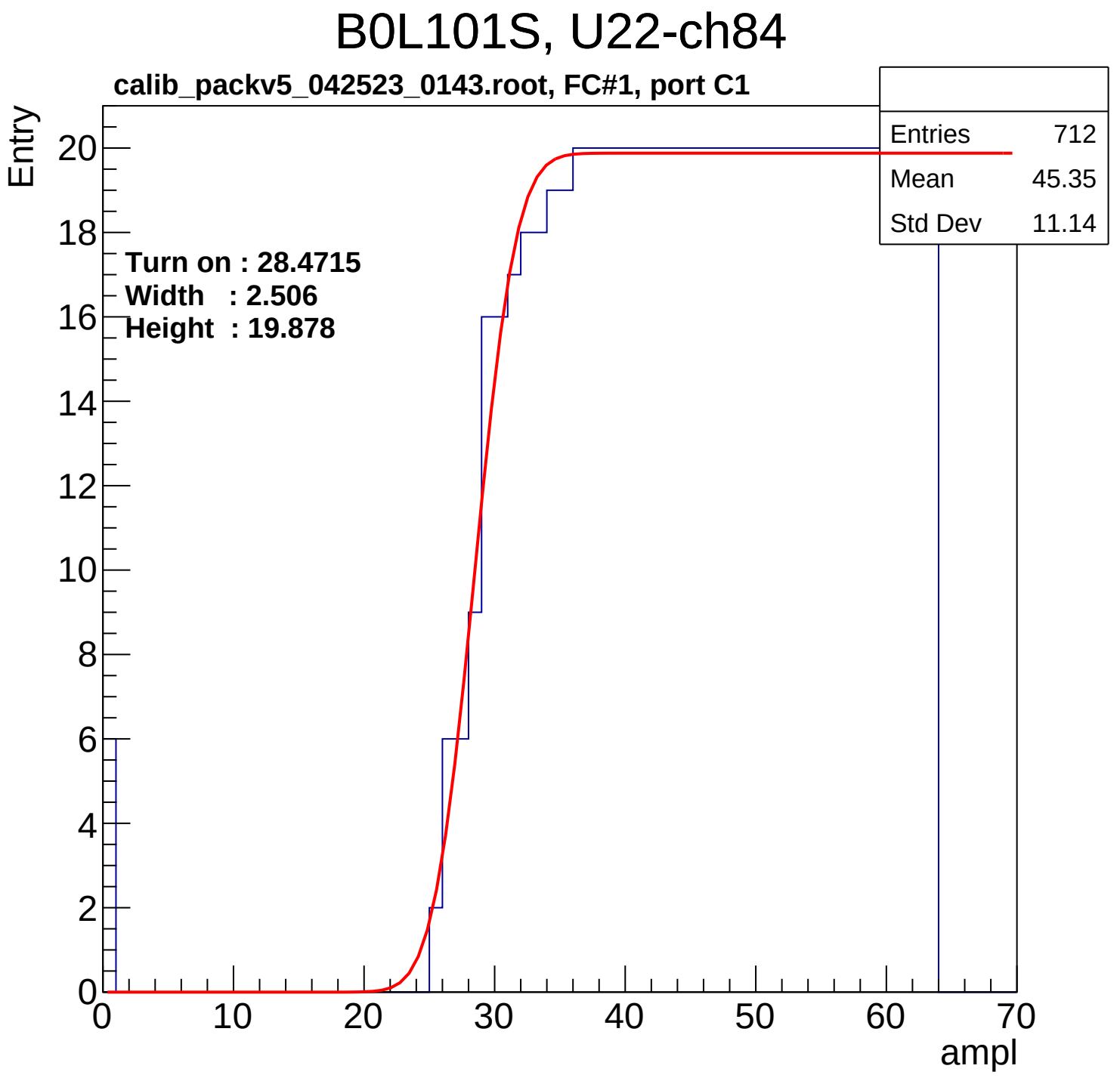

B0L101S, U22-ch79
calib_packv5_042523_0143.root, FC#1, port C1
Entries 726
Mean 45.05
Std Dev 11.16
Turn on : 28.1972
Width : 3.946
Height : 20.108
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

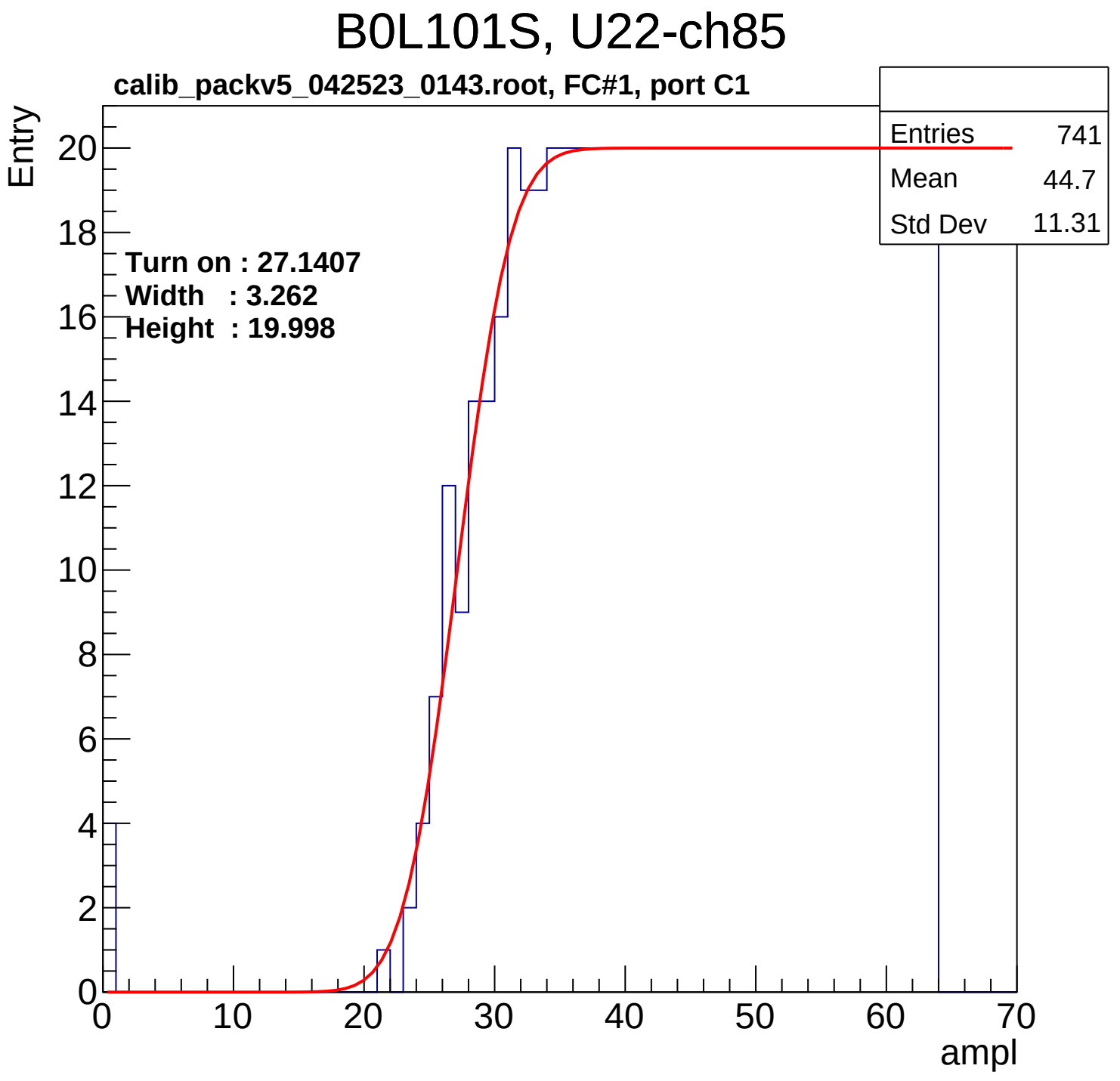

B0L101S, U22-ch80
calib_packv5_042523_0143.root, FC#1, port C1
Entries 771
Mean 44.05
Std Dev 11.49
Turn on : 25.5438
Width : 1.504
Height : 19.799
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

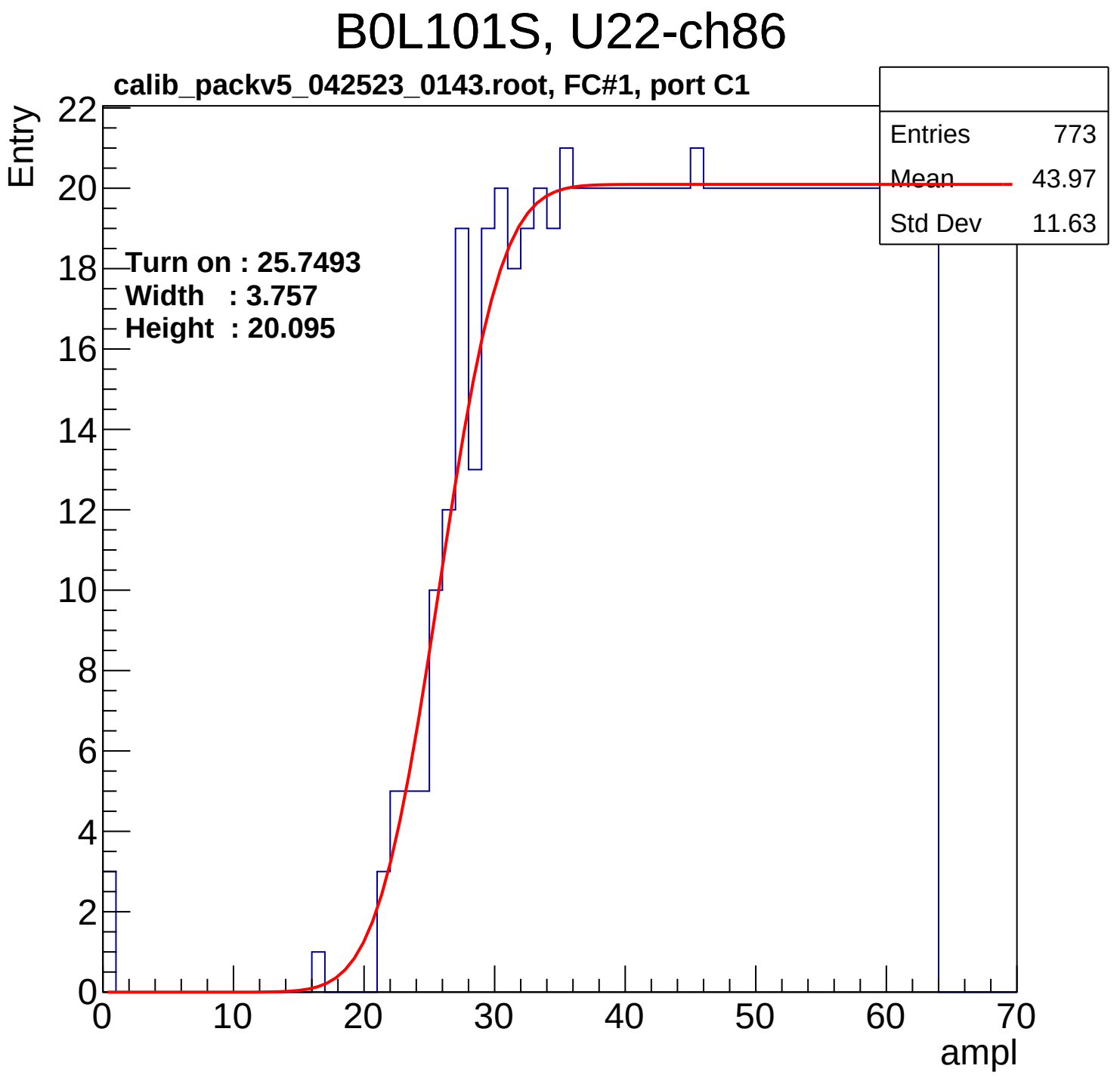

B0L101S, U22-ch81
calib_packv5_042523_0143.root, FC#1, port C1
Entries 747
Mean 44.63
Std Dev 11.23
Turn on : 27.0430
Width : 2.656
Height : 20.039
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

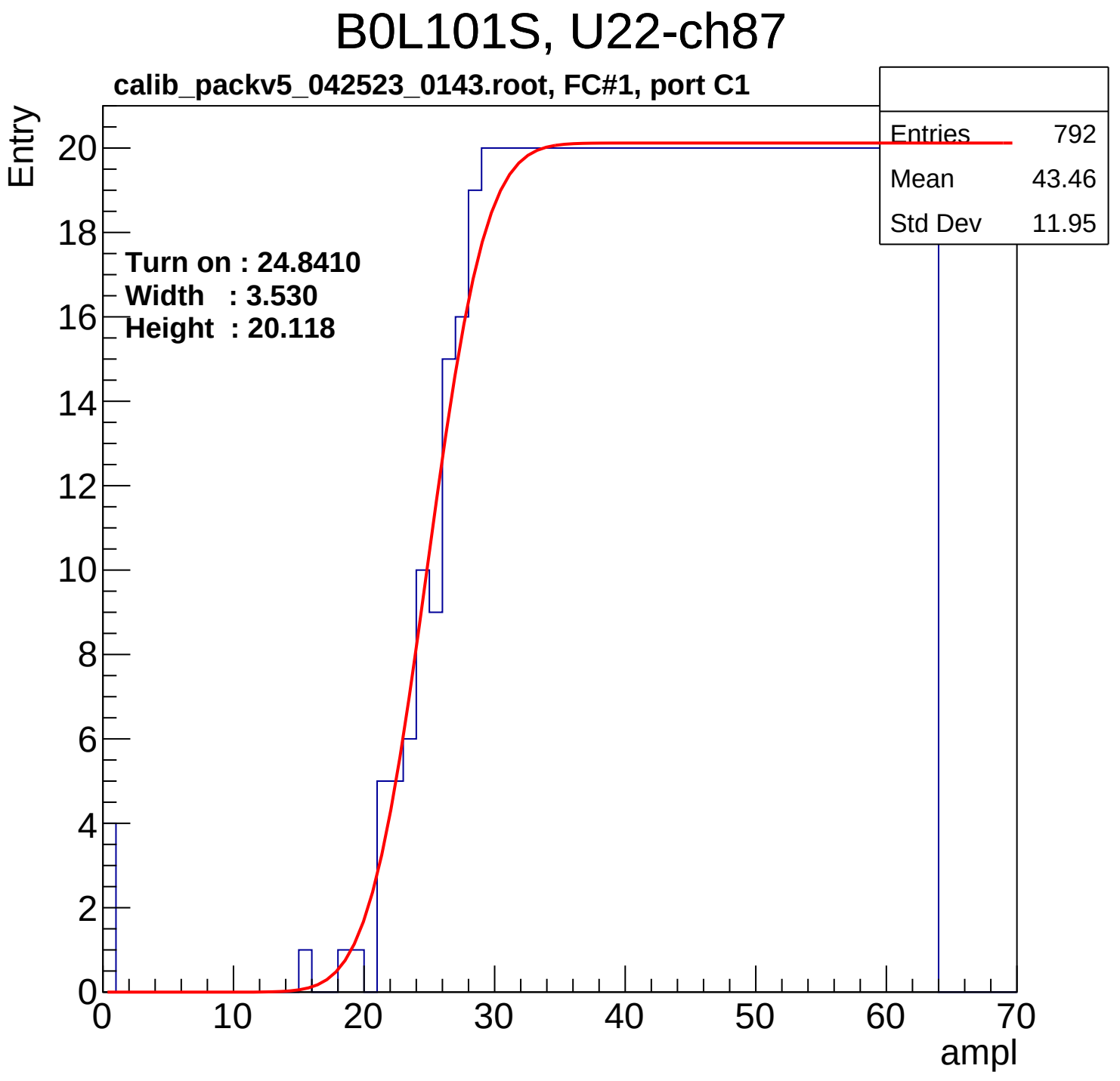

B0L101S, U22-ch82
calib_packv5_042523_0143.root, FC#1, port C1
Entries 759
Mean 44.26
Std Dev 11.56
Turn on : 26.5340
Width : 2.947
Height : 20.025
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

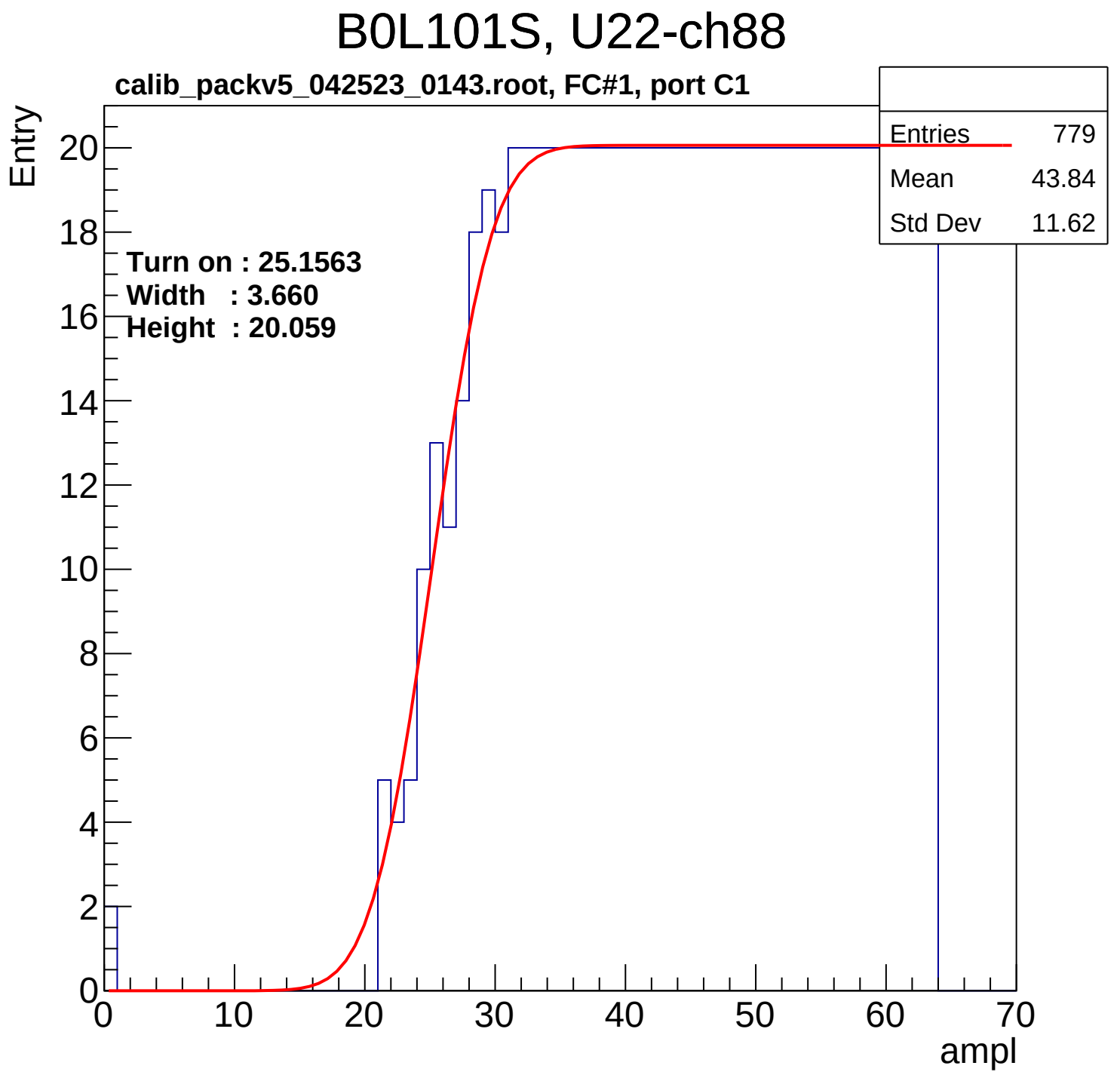

B0L101S, U22-ch83
calib_packv5_042523_0143.root, FC#1, port C1
Entries 742
Mean 44.65
Std Dev 11.43
Turn on : 27.4519
Width : 3.564
Height : 20.112
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

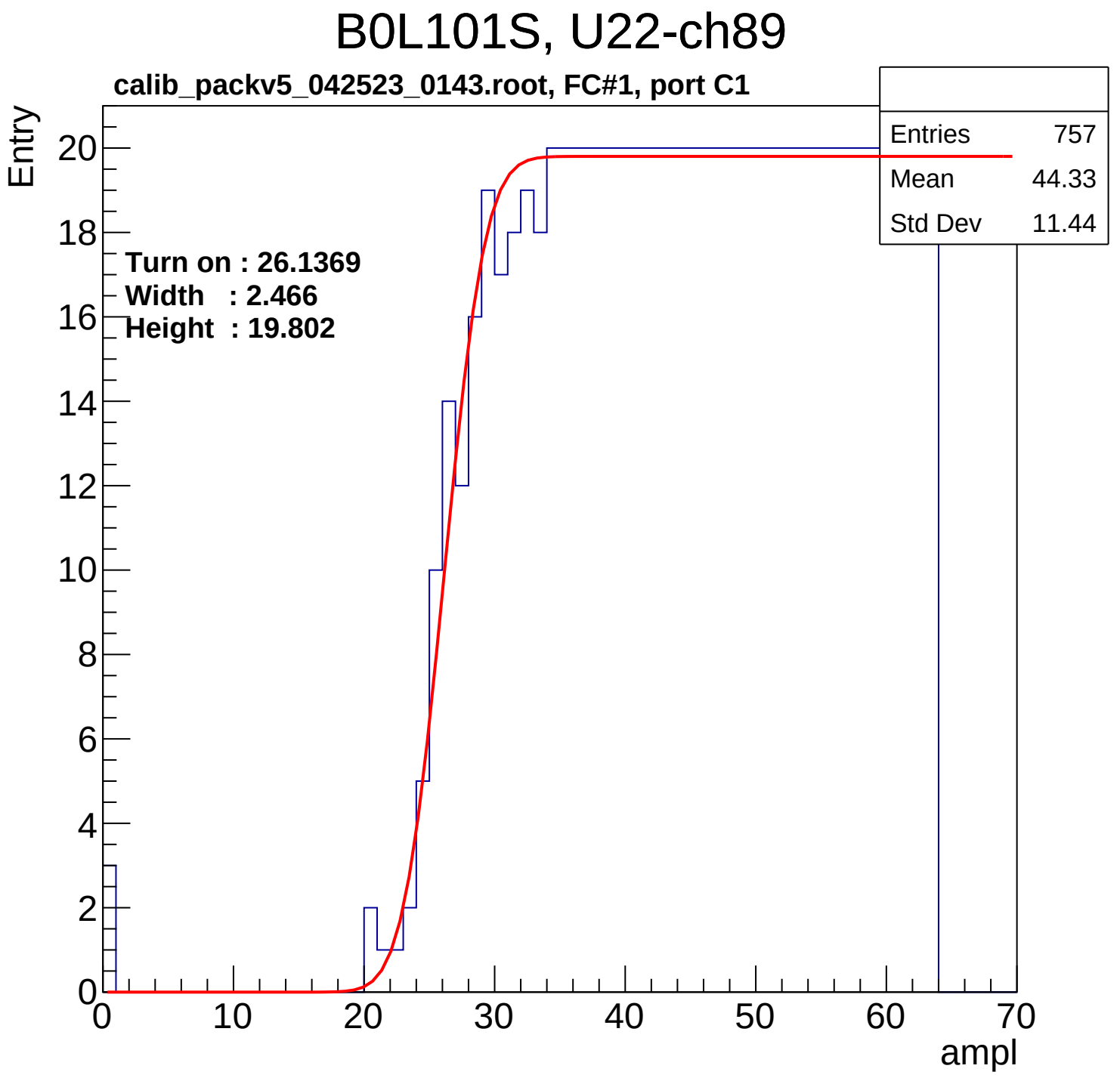

B0L101S, U22-ch84
calib_packv5_042523_0143.root, FC#1, port C1
Entries 712
Mean 45.35
Std Dev 11.14
Turn on : 28.4715
Width : 2.506
Height : 19.878
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

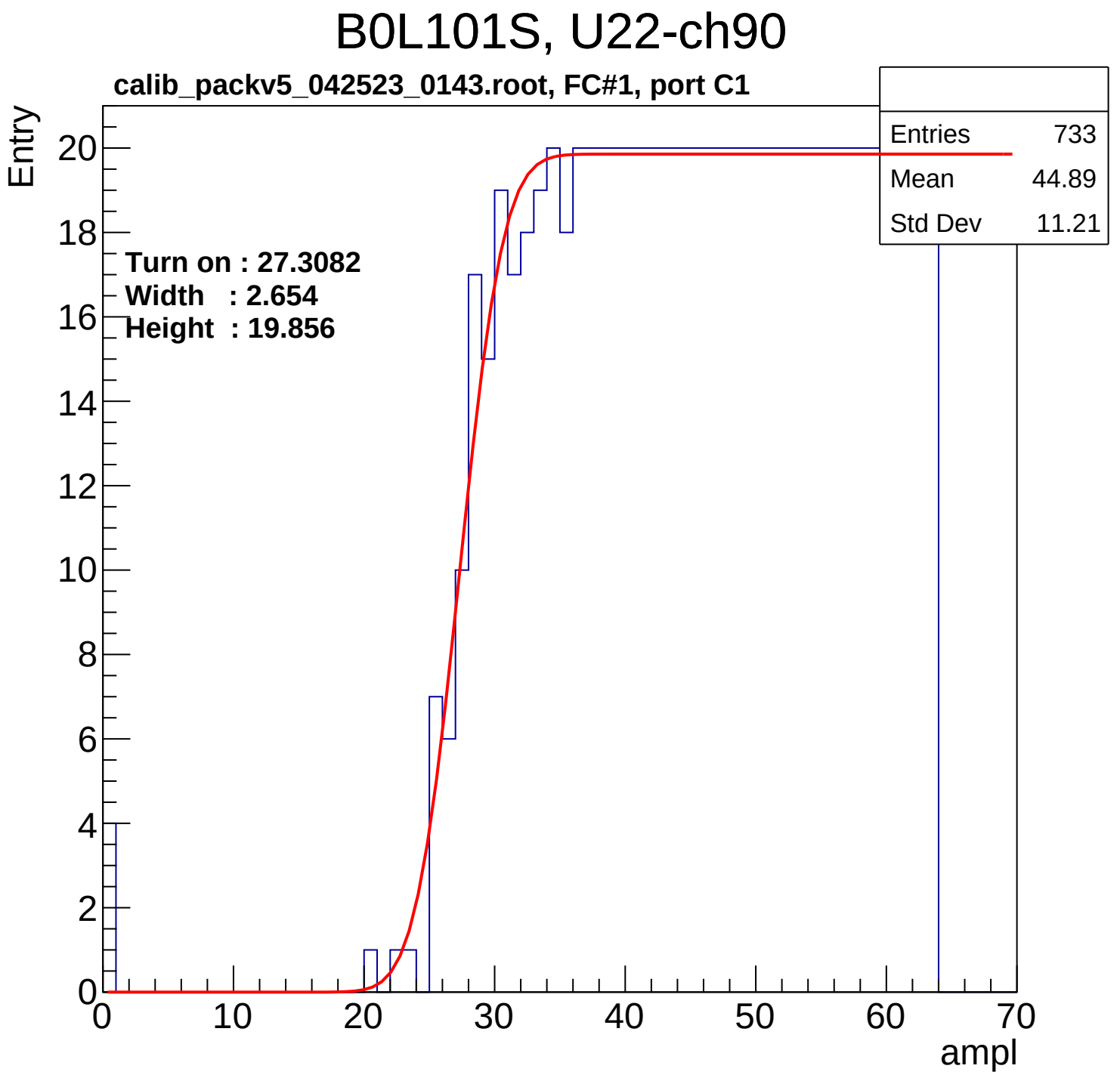

B0L101S, U22-ch85
calib_packv5_042523_0143.root, FC#1, port C1
Entries 741
Mean 44.7
Std Dev 11.31
Turn on : 27.1407
Width : 3.262
Height : 19.998
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

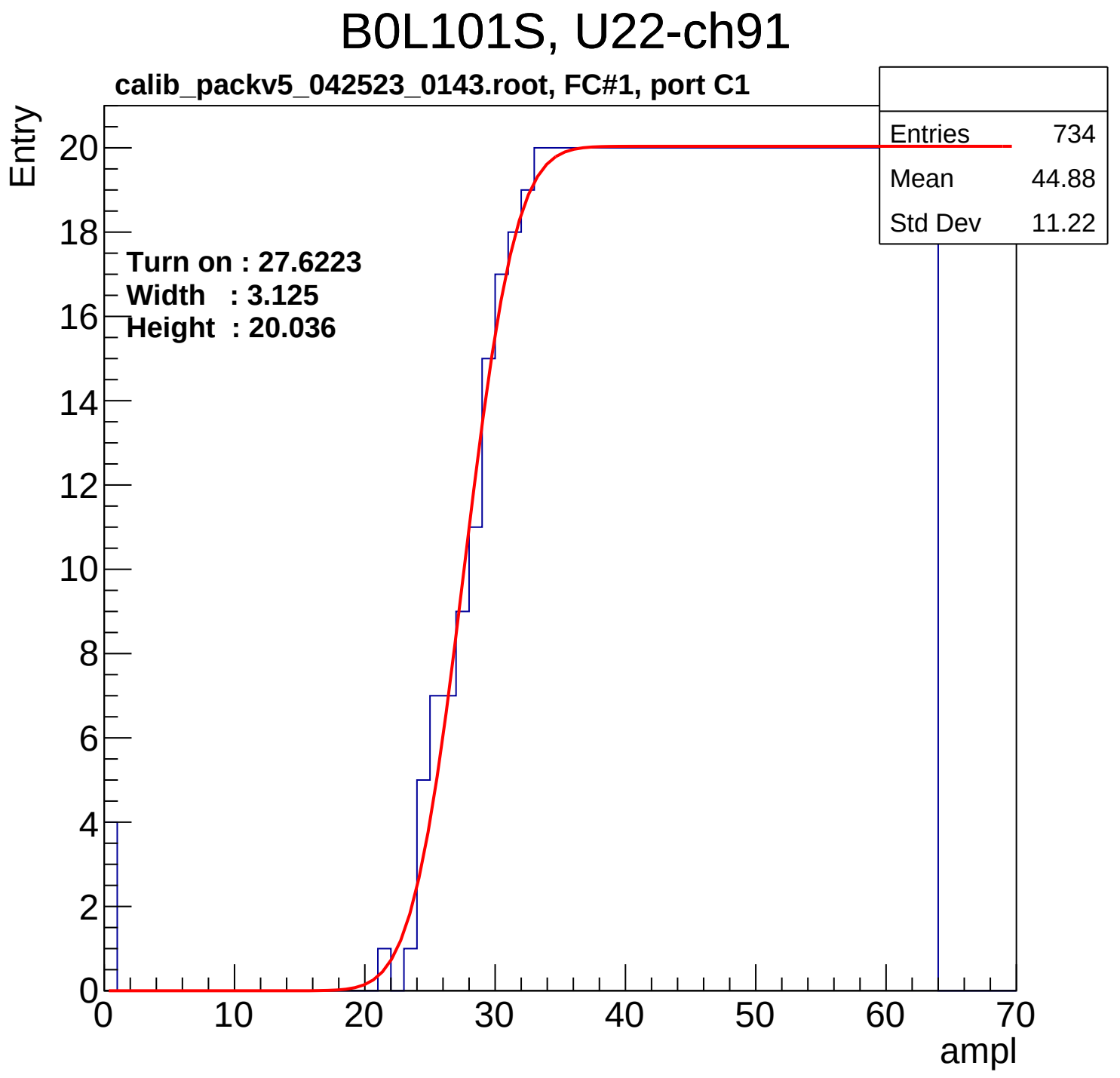

B0L101S, U22-ch86
calib_packv5_042523_0143.root, FC#1, port C1
Entries 773
Mean 43.97
Std Dev 11.63
Turn on : 25.7493
Width : 3.757
Height : 20.095
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70

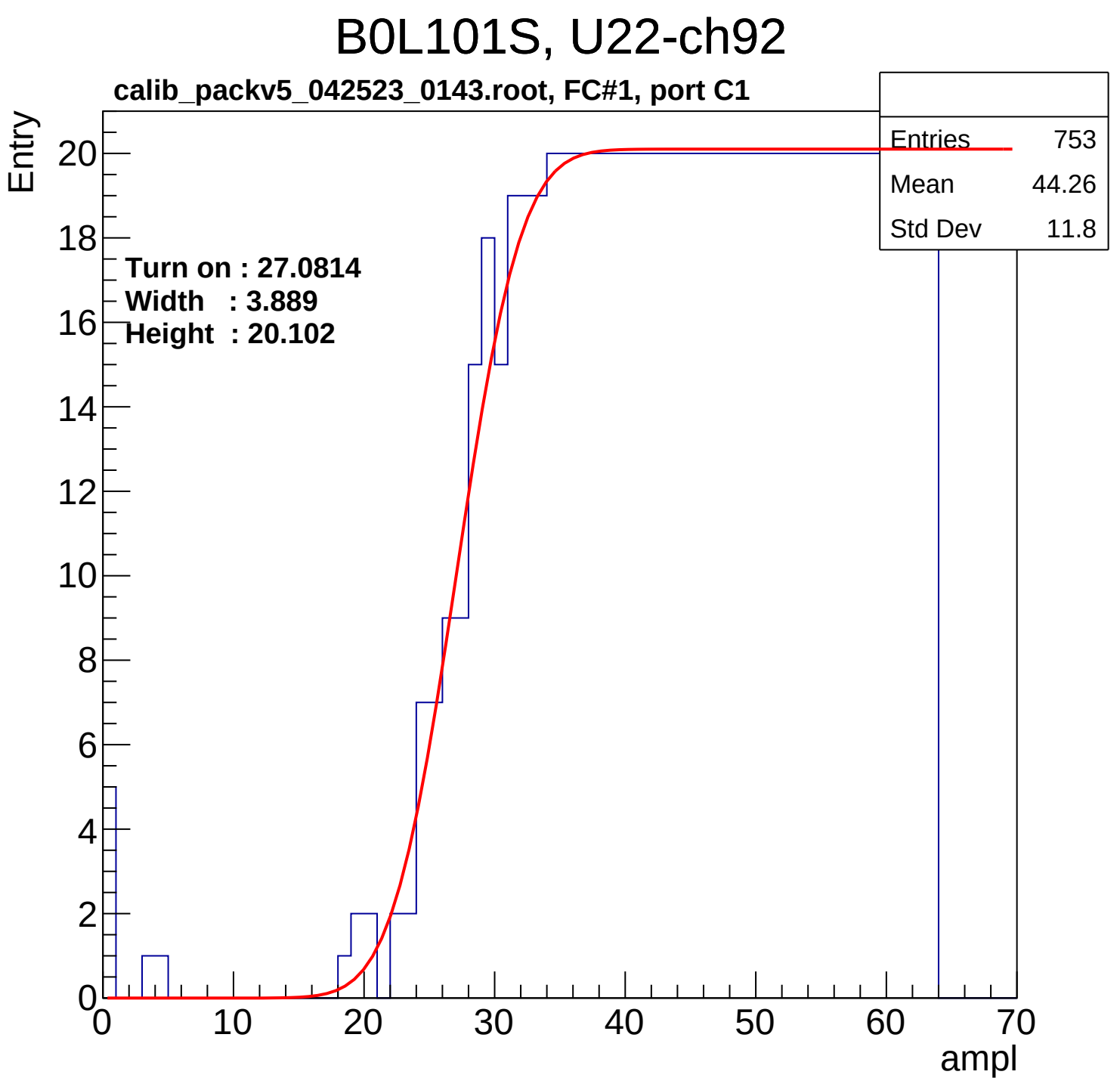

B0L101S, U22-ch87
calib_packv5_042523_0143.root, FC#1, port C1
Entries 792
Mean 43.46
Std Dev 11.95
Turn on : 24.8410
Width : 3.530
Height : 20.118
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

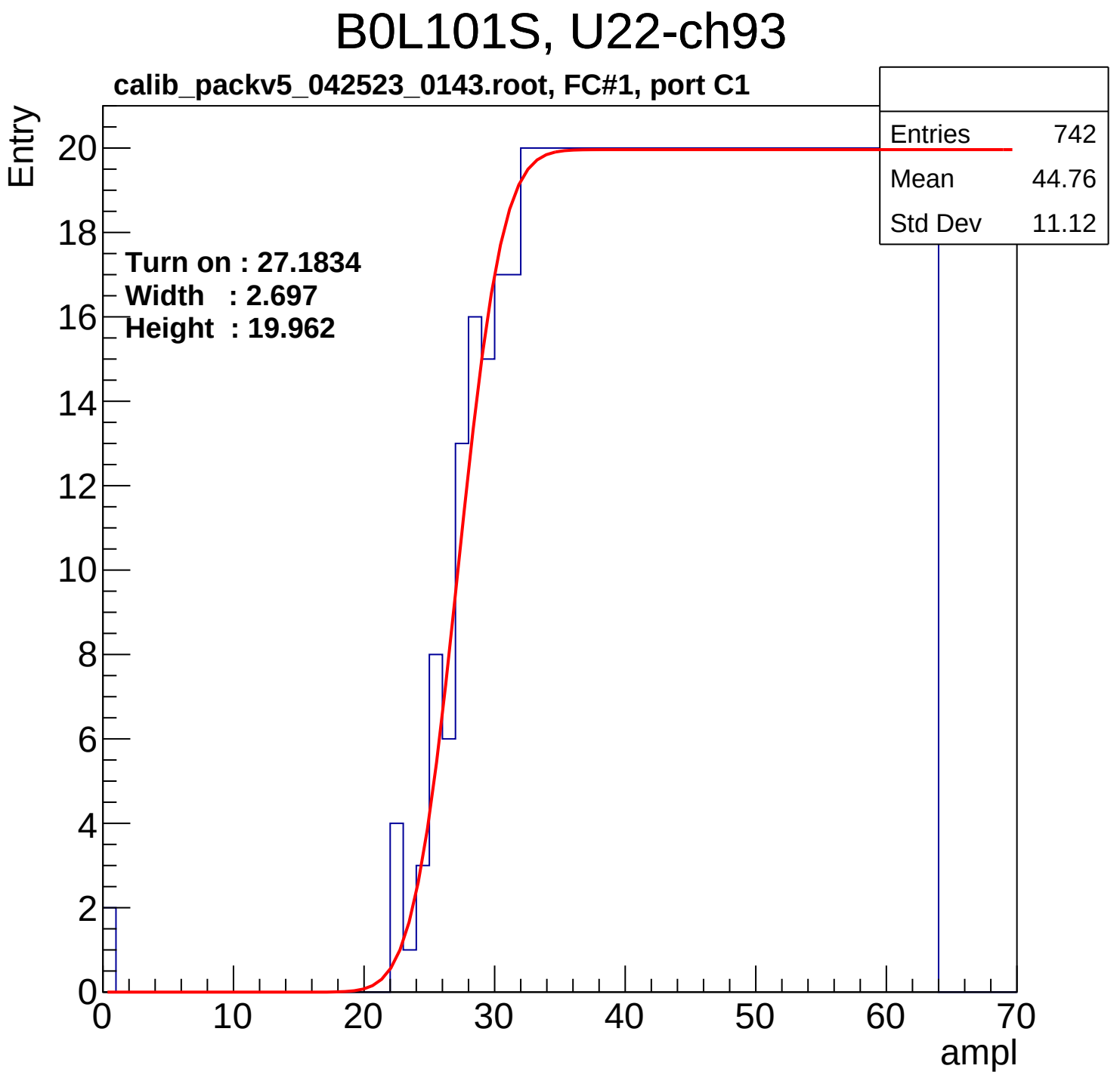

B0L101S, U22-ch88
calib_packv5_042523_0143.root, FC#1, port C1
Entries 779
Mean 43.84
Std Dev 11.62
Turn on : 25.1563
Width : 3.660
Height : 20.059
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

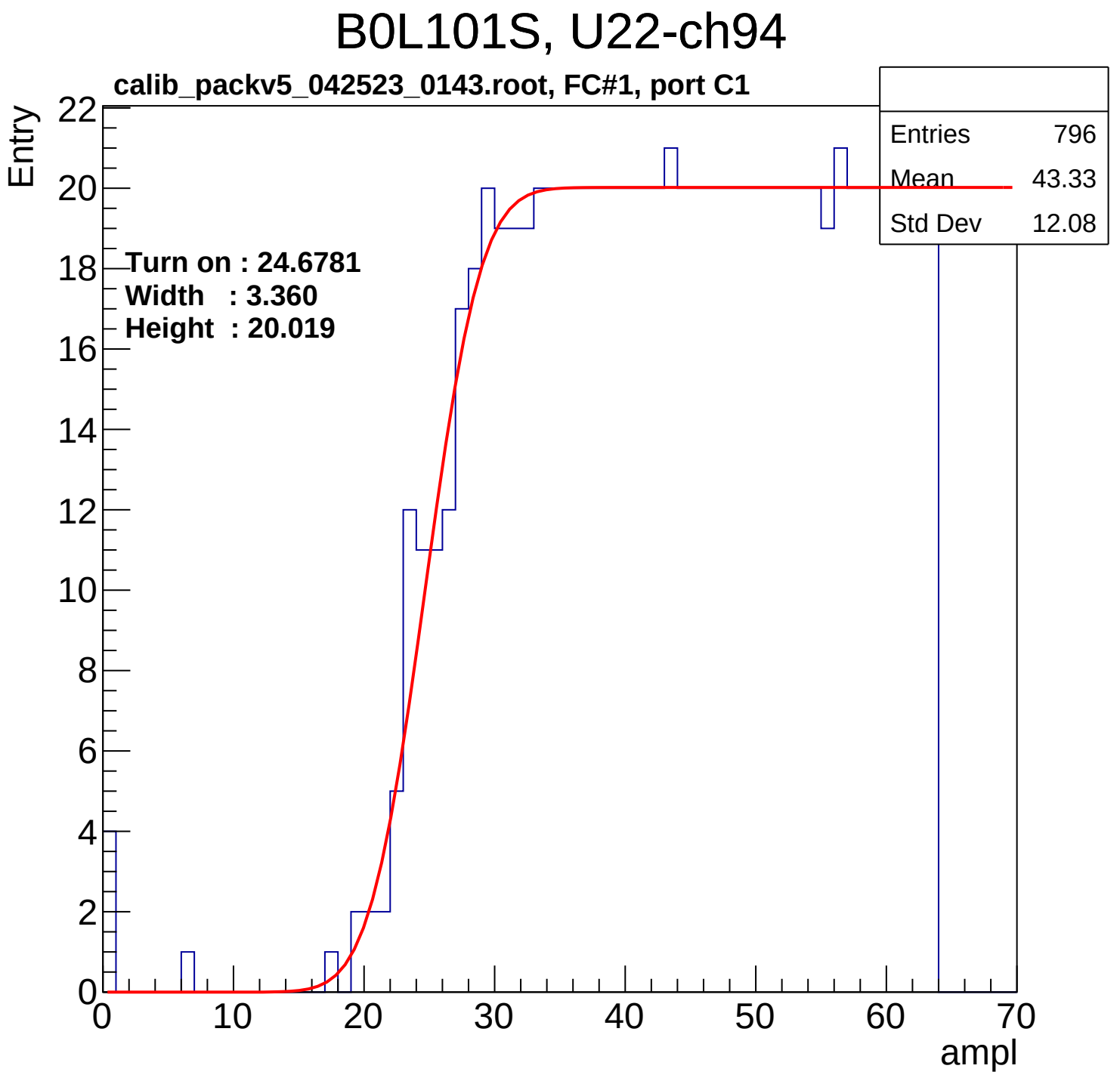

B0L101S, U22-ch89
calib_packv5_042523_0143.root, FC#1, port C1
Entries 757
Mean 44.33
Std Dev 11.44
Turn on : 26.1369
Width : 2.466
Height : 19.802
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

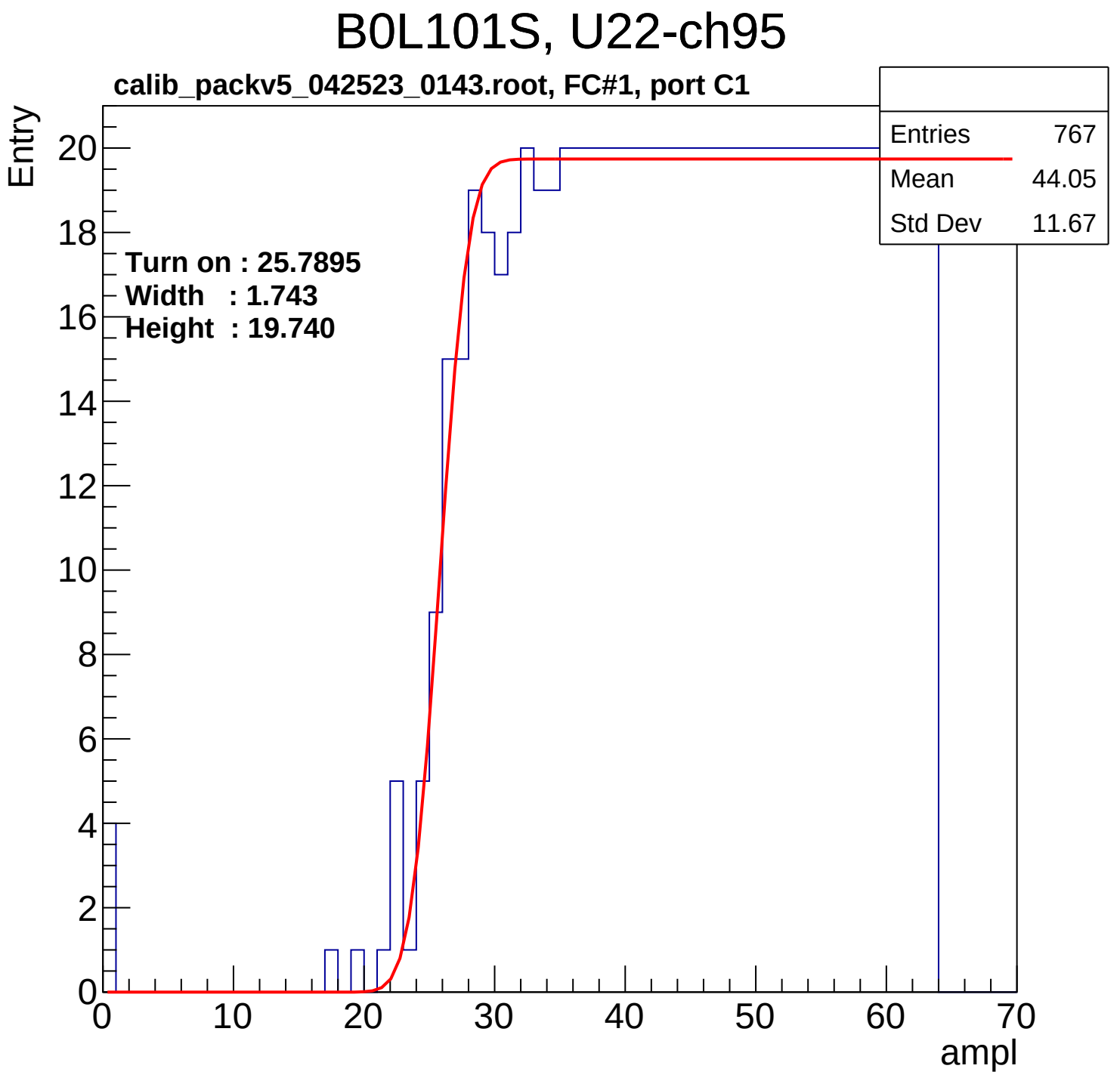

B0L101S, U22-ch90
calib_packv5_042523_0143.root, FC#1, port C1
Entries 733
Mean 44.89
Std Dev 11.21
Turn on : 27.3082
Width : 2.654
Height : 19.856
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

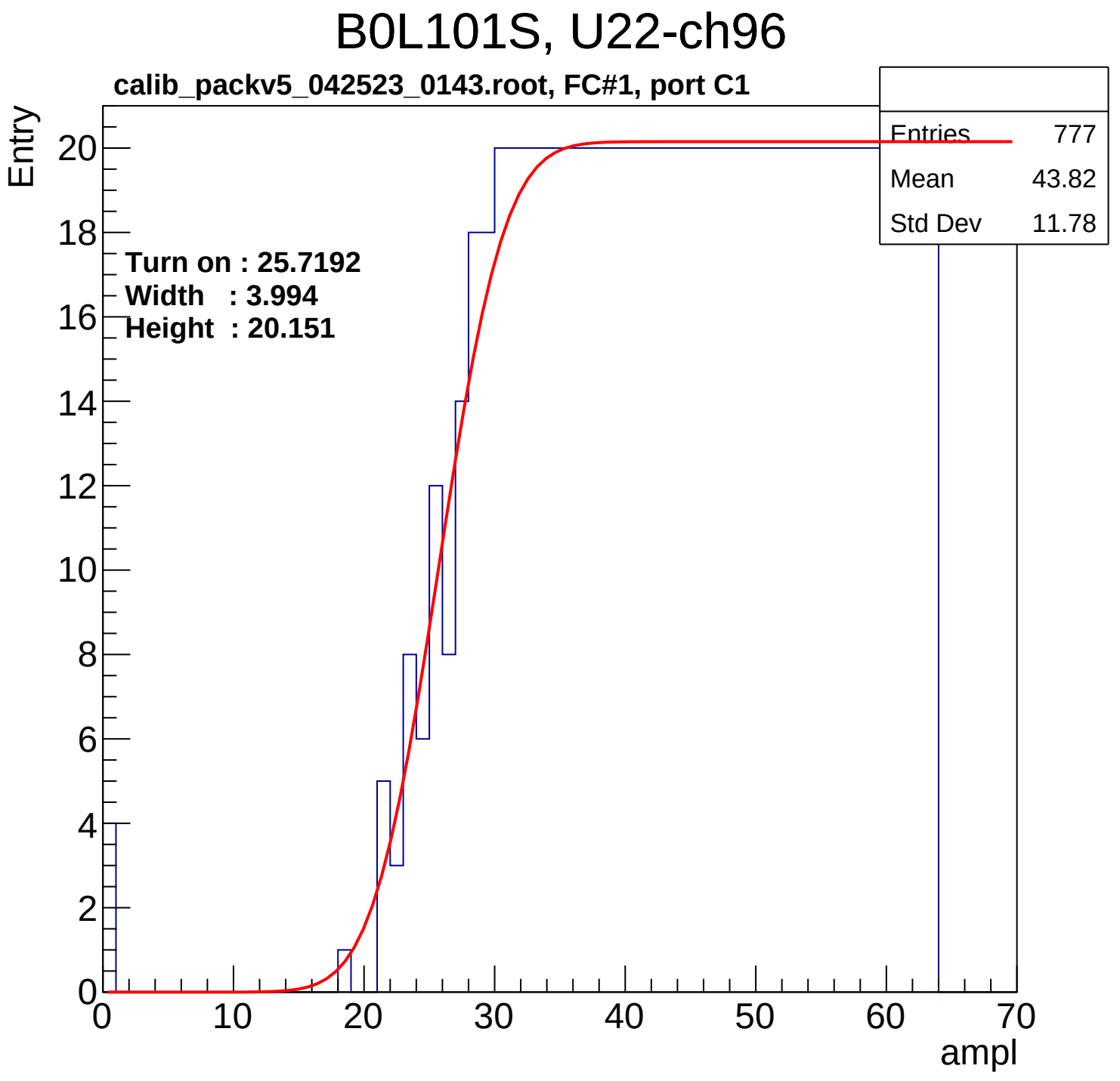

B0L101S, U22-ch91
calib_packv5_042523_0143.root, FC#1, port C1
Entries 734
Mean 44.88
Std Dev 11.22
Turn on : 27.6223
Width : 3.125
Height : 20.036
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

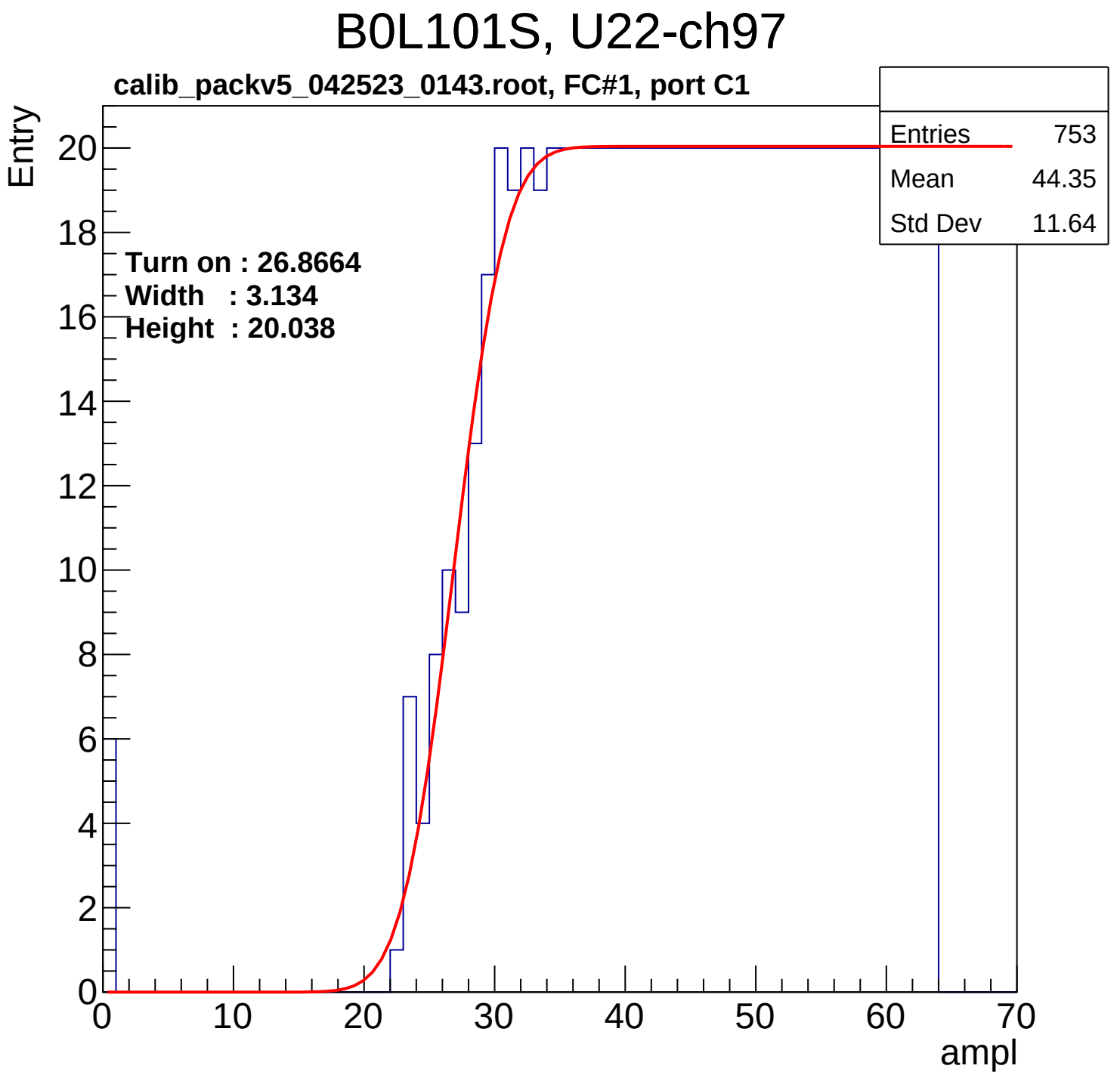

B0L101S, U22-ch92
calib_packv5_042523_0143.root, FC#1, port C1
Entries 753
Mean 44.26
Std Dev 11.8
Turn on : 27.0814
Width : 3.889
Height : 20.102
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

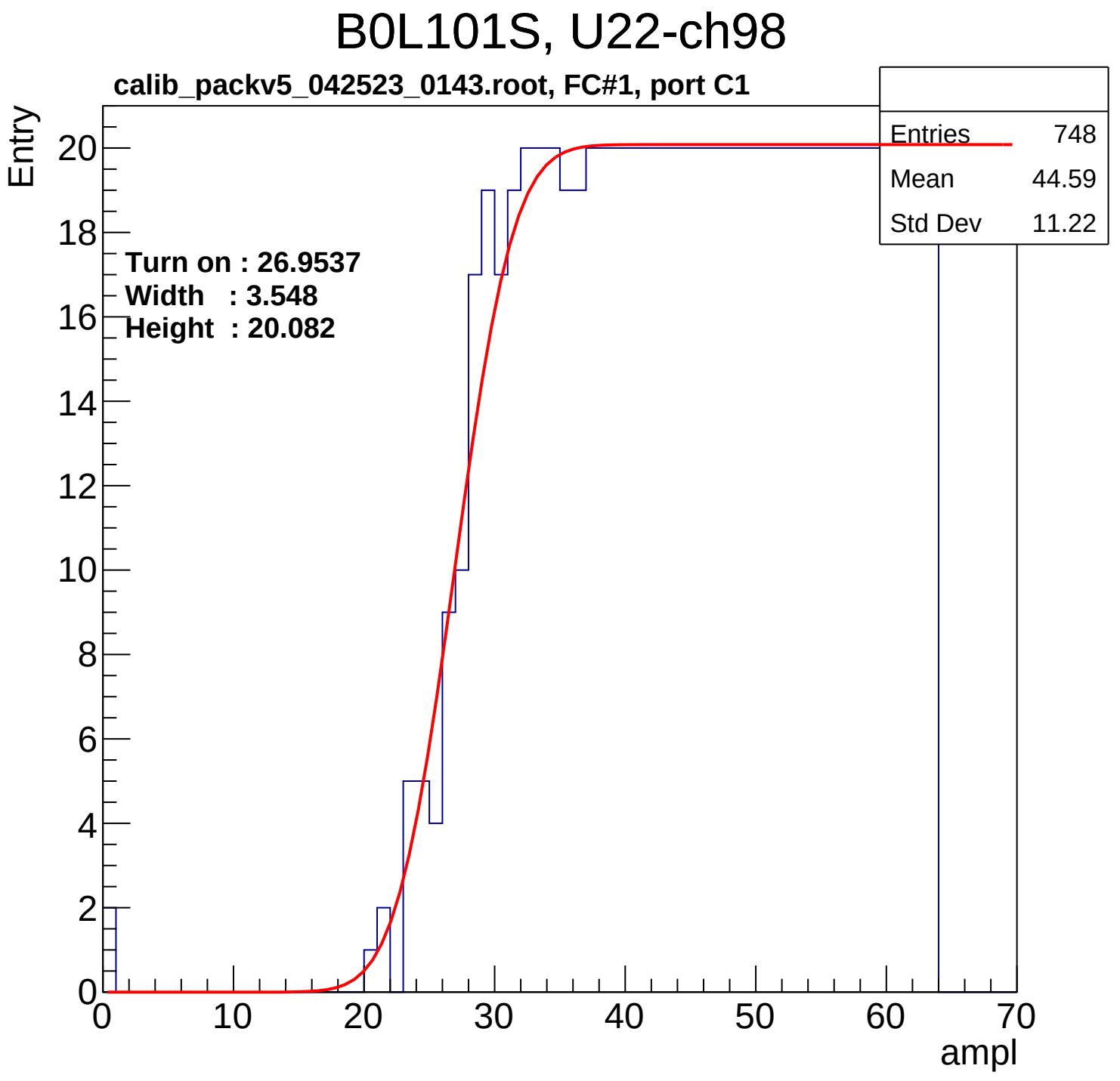

B0L101S, U22-ch93
calib_packv5_042523_0143.root, FC#1, port C1
Entries 742
Mean 44.76
Std Dev 11.12
Turn on : 27.1834
Width : 2.697
Height : 19.962
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

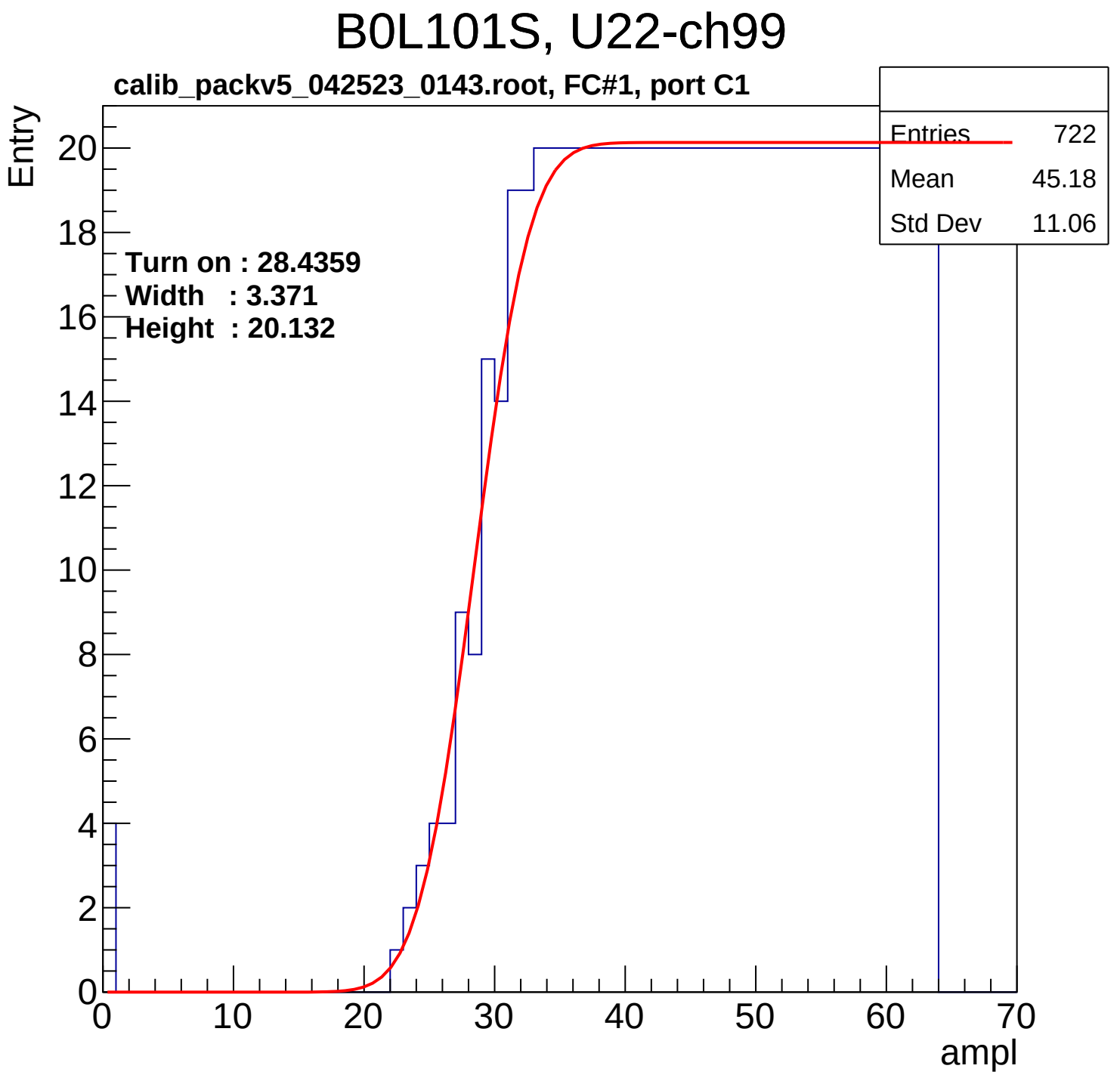

B0L101S, U22-ch94
calib_packv5_042523_0143.root, FC#1, port C1
Entries 796
Mean 43.33
Std Dev 12.08
Turn on : 24.6781
Width : 3.360
Height : 20.019
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70

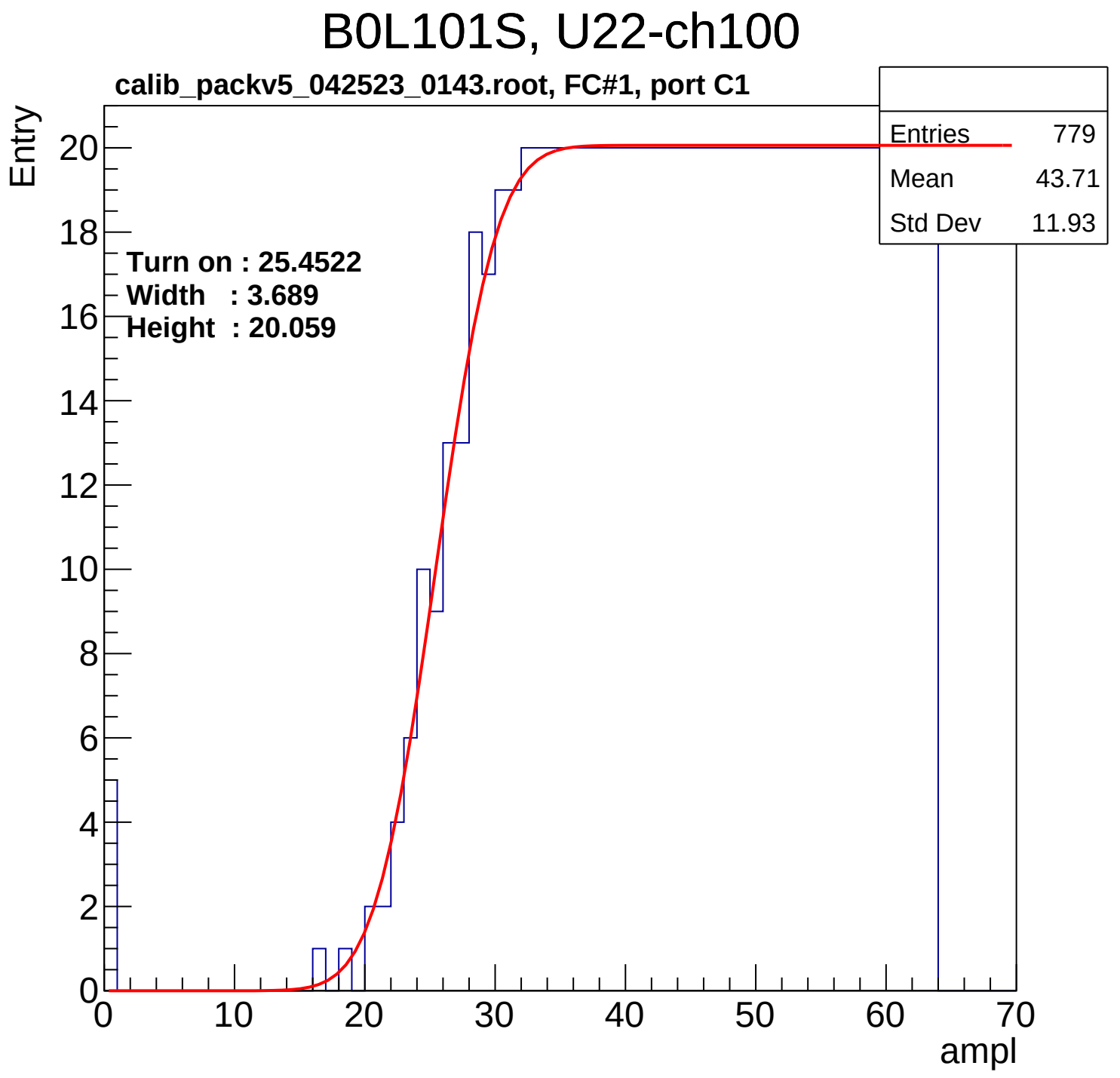

B0L101S, U22-ch95
calib_packv5_042523_0143.root, FC#1, port C1
Entries 767
Mean 44.05
Std Dev 11.67
Turn on : 25.7895
Width : 1.743
Height : 19.740
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

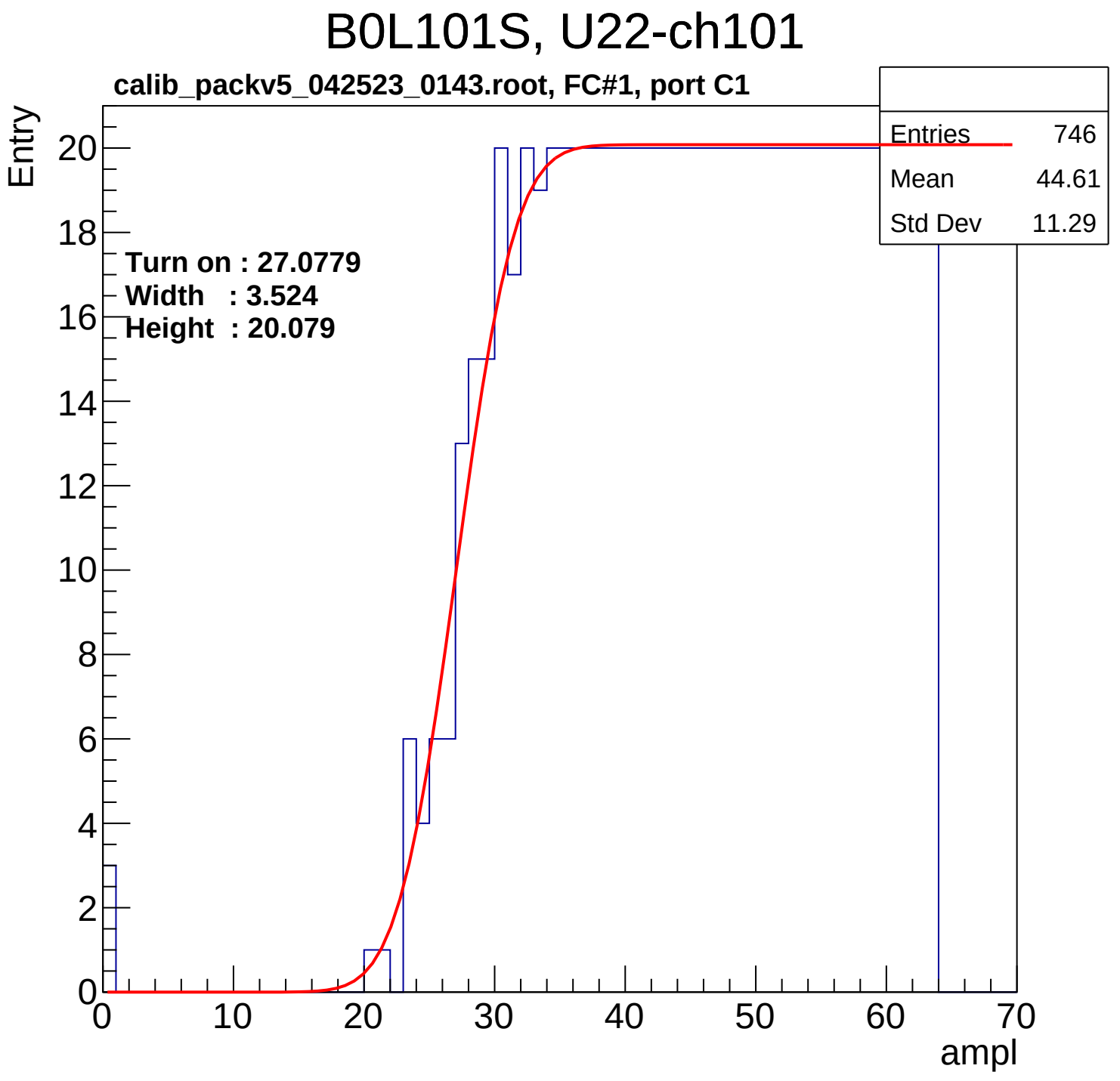

B0L101S, U22-ch96
calib_packv5_042523_0143.root, FC#1, port C1
Entries 777
Mean 43.82
Std Dev 11.78
Turn on : 25.7192
Width : 3.994
Height : 20.151
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

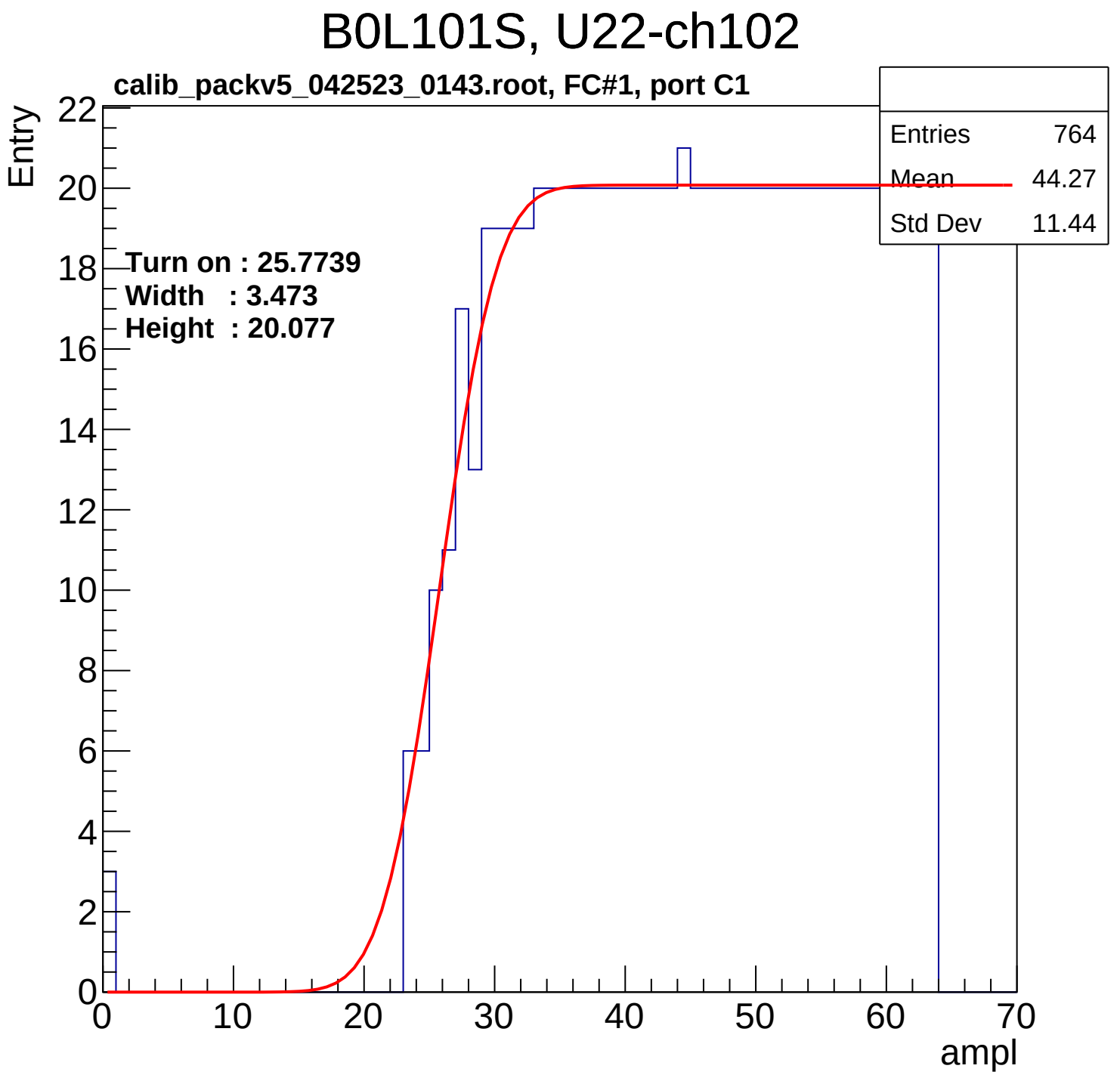

B0L101S, U22-ch97
calib_packv5_042523_0143.root, FC#1, port C1
Entries 753
Mean 44.35
Std Dev 11.64
Turn on : 26.8664
Width : 3.134
Height : 20.038
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

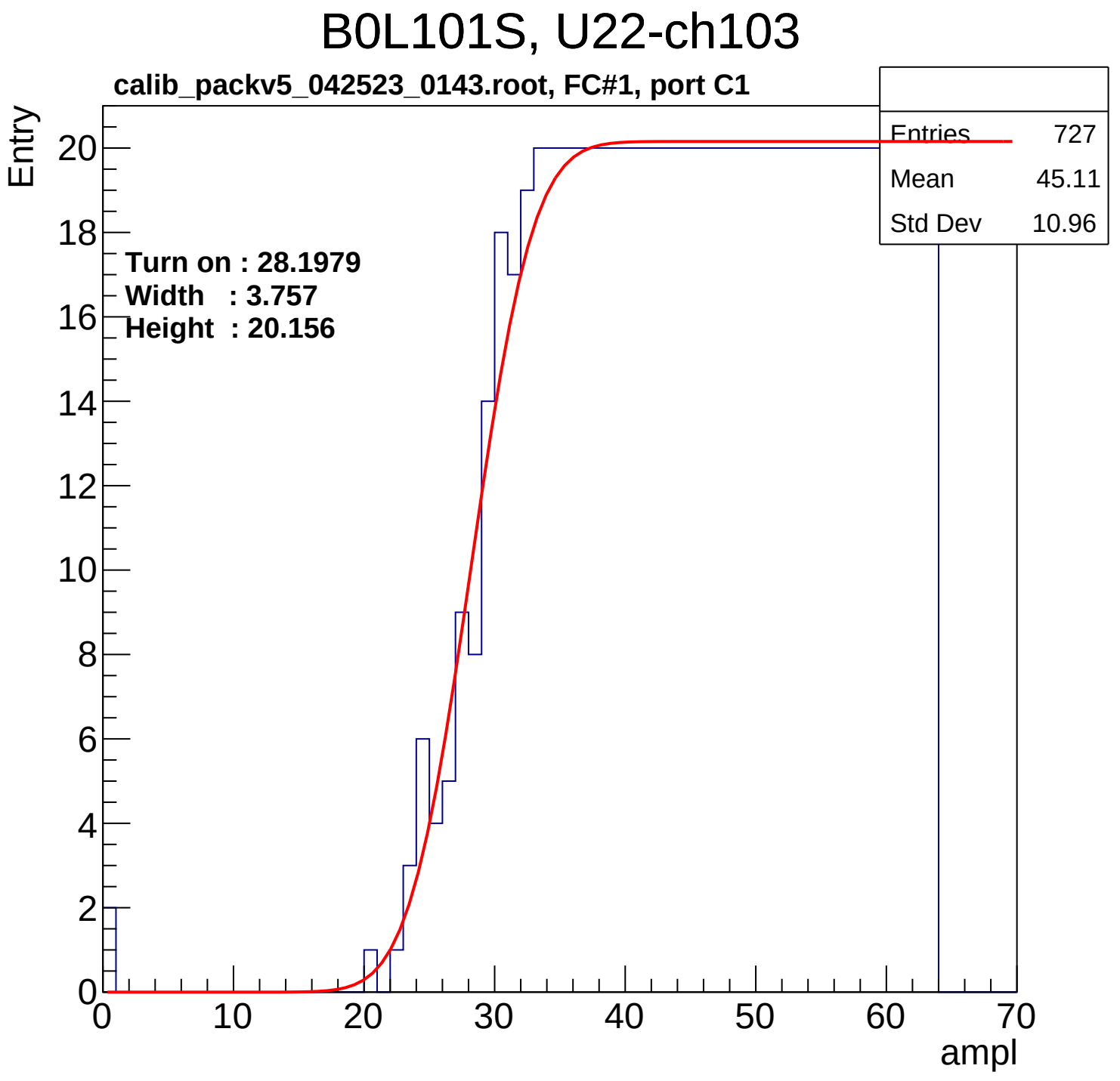

B0L101S, U22-ch98
calib_packv5_042523_0143.root, FC#1, port C1
Entries 748
Mean 44.59
Std Dev 11.22
Turn on : 26.9537
Width : 3.548
Height : 20.082
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

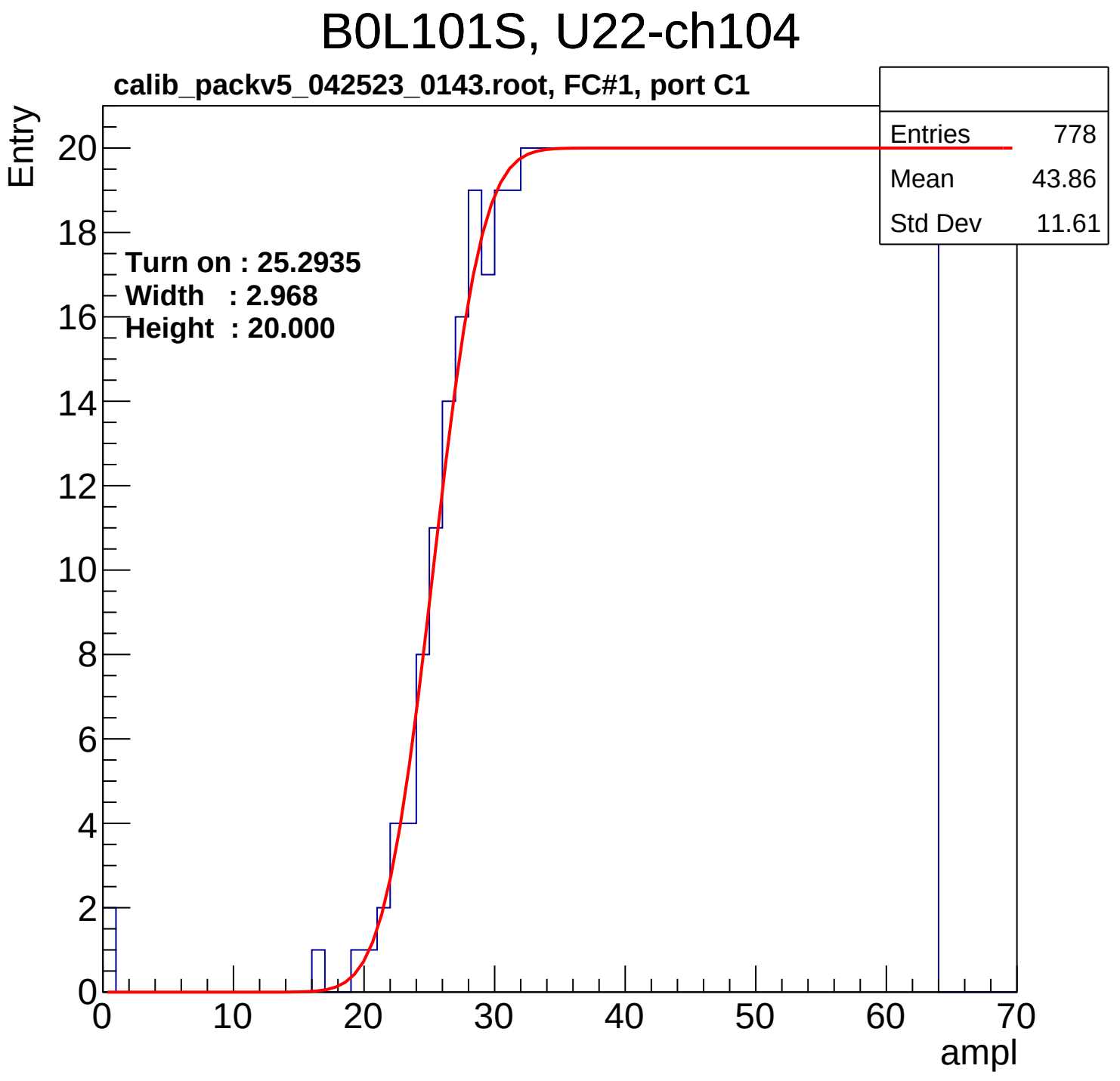

B0L101S, U22-ch99
calib_packv5_042523_0143.root, FC#1, port C1
Entries 722
Mean 45.18
Std Dev 11.06
Turn on : 28.4359
Width : 3.371
Height : 20.132
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

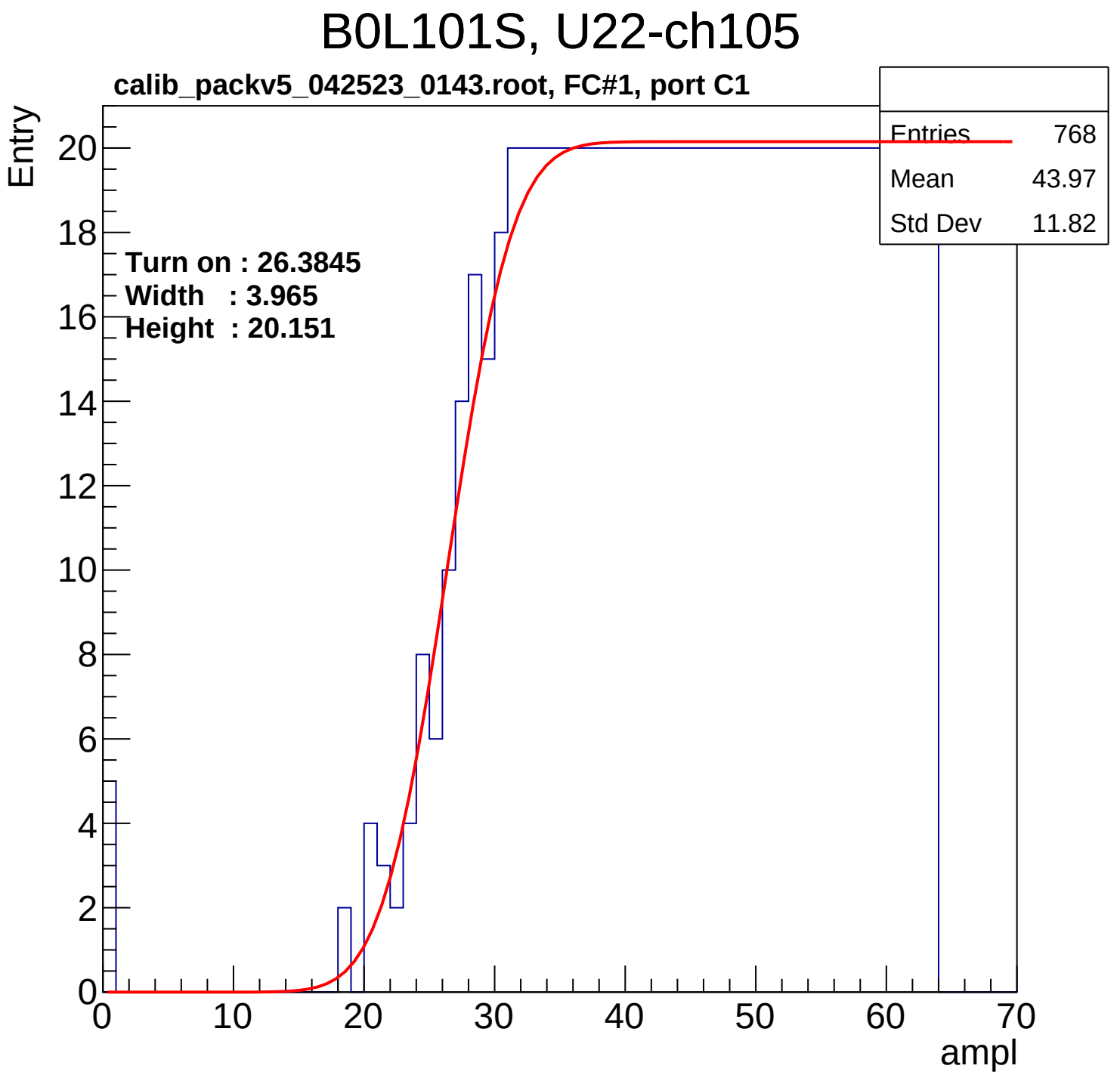

B0L101S, U22-ch100
calib_packv5_042523_0143.root, FC#1, port C1
Entries 779
Mean 43.71
Std Dev 11.93
Turn on : 25.4522
Width : 3.689
Height : 20.059
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

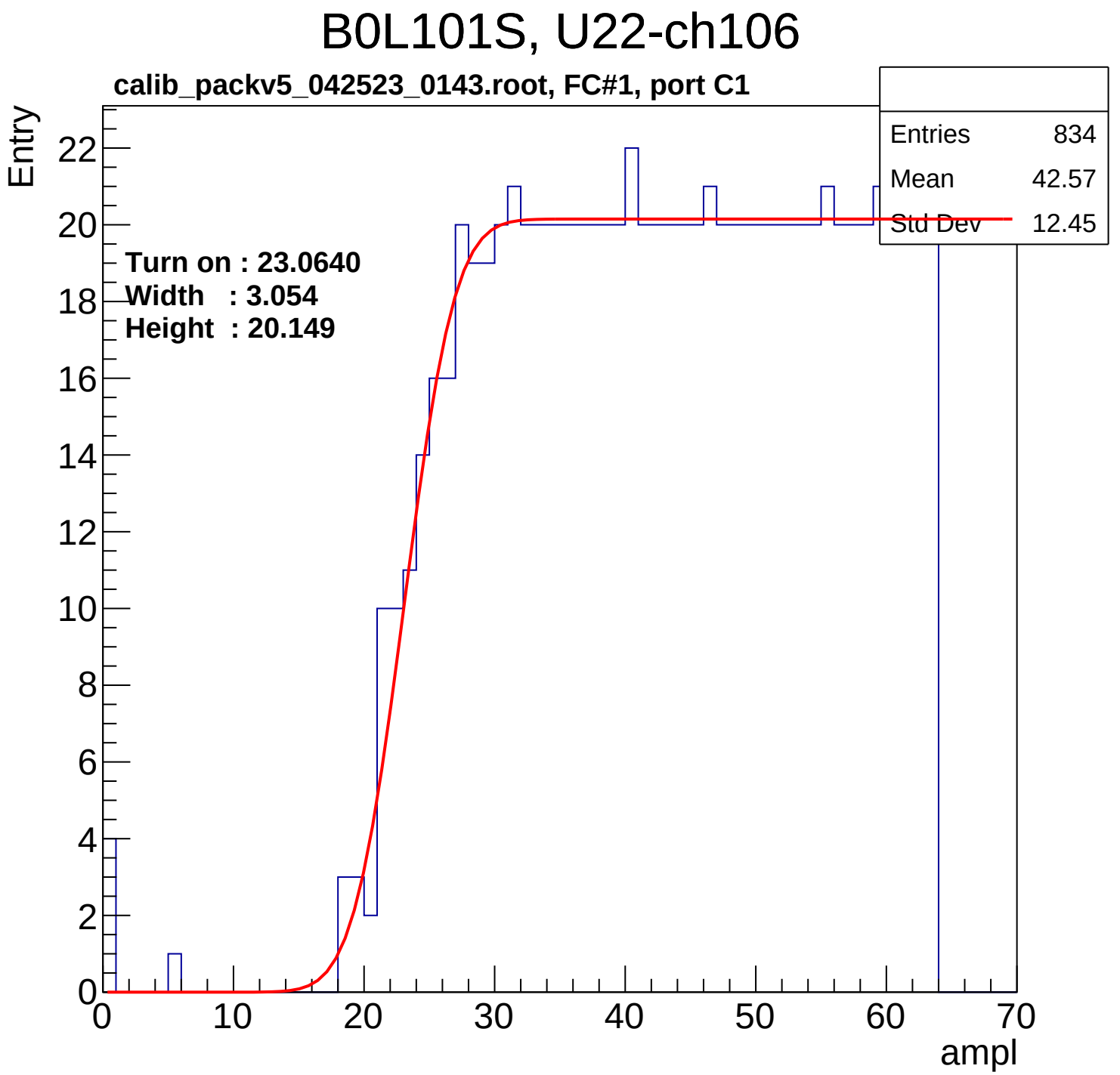

B0L101S, U22-ch101
calib_packv5_042523_0143.root, FC#1, port C1
Entries 746
Mean 44.61
Std Dev 11.29
Turn on : 27.0779
Width : 3.524
Height : 20.079
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

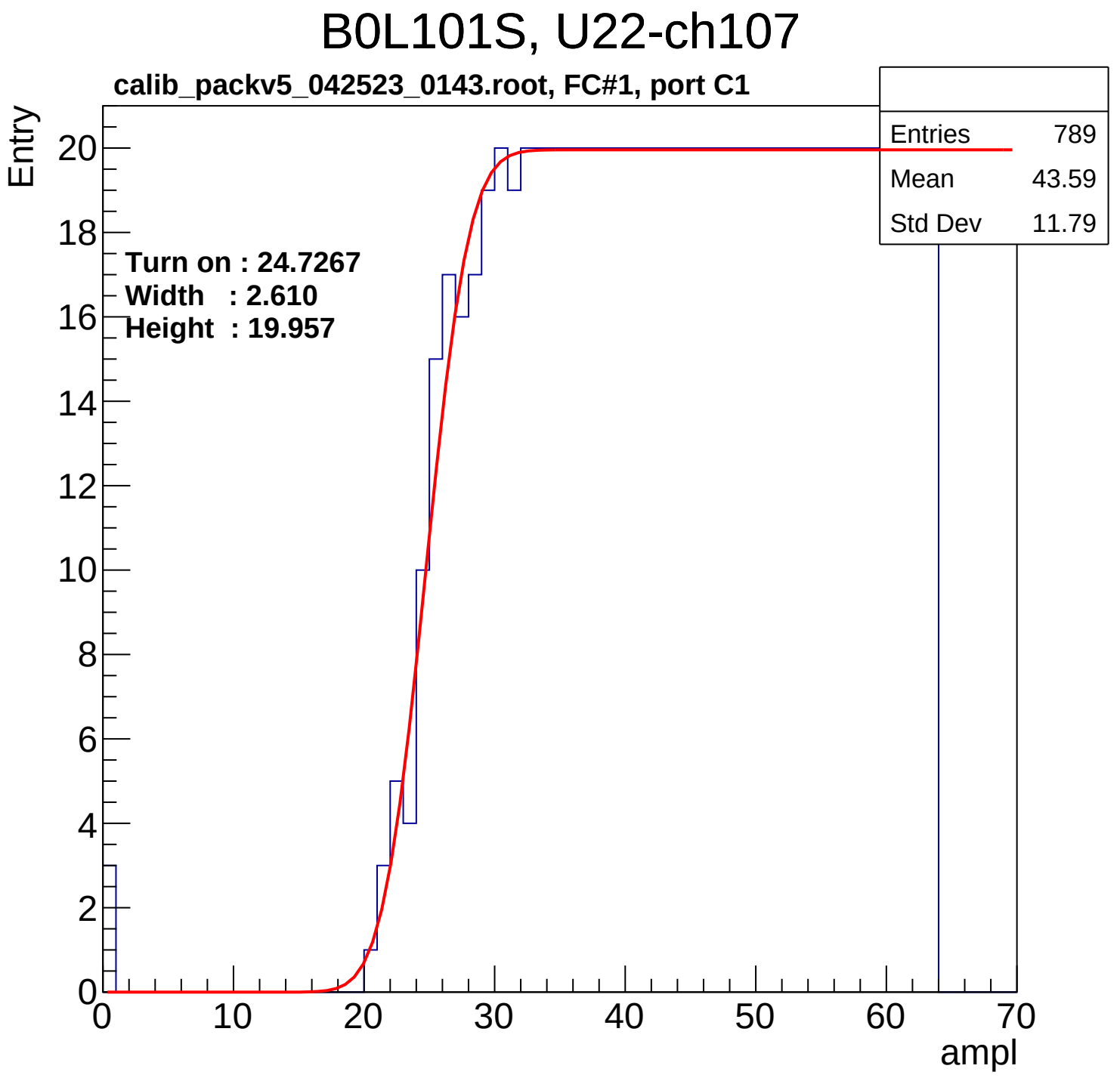

B0L101S, U22-ch102
calib_packv5_042523_0143.root, FC#1, port C1
Entries 764
Mean 44.27
Std Dev 11.44
Turn on : 25.7739
Width : 3.473
Height : 20.077
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70

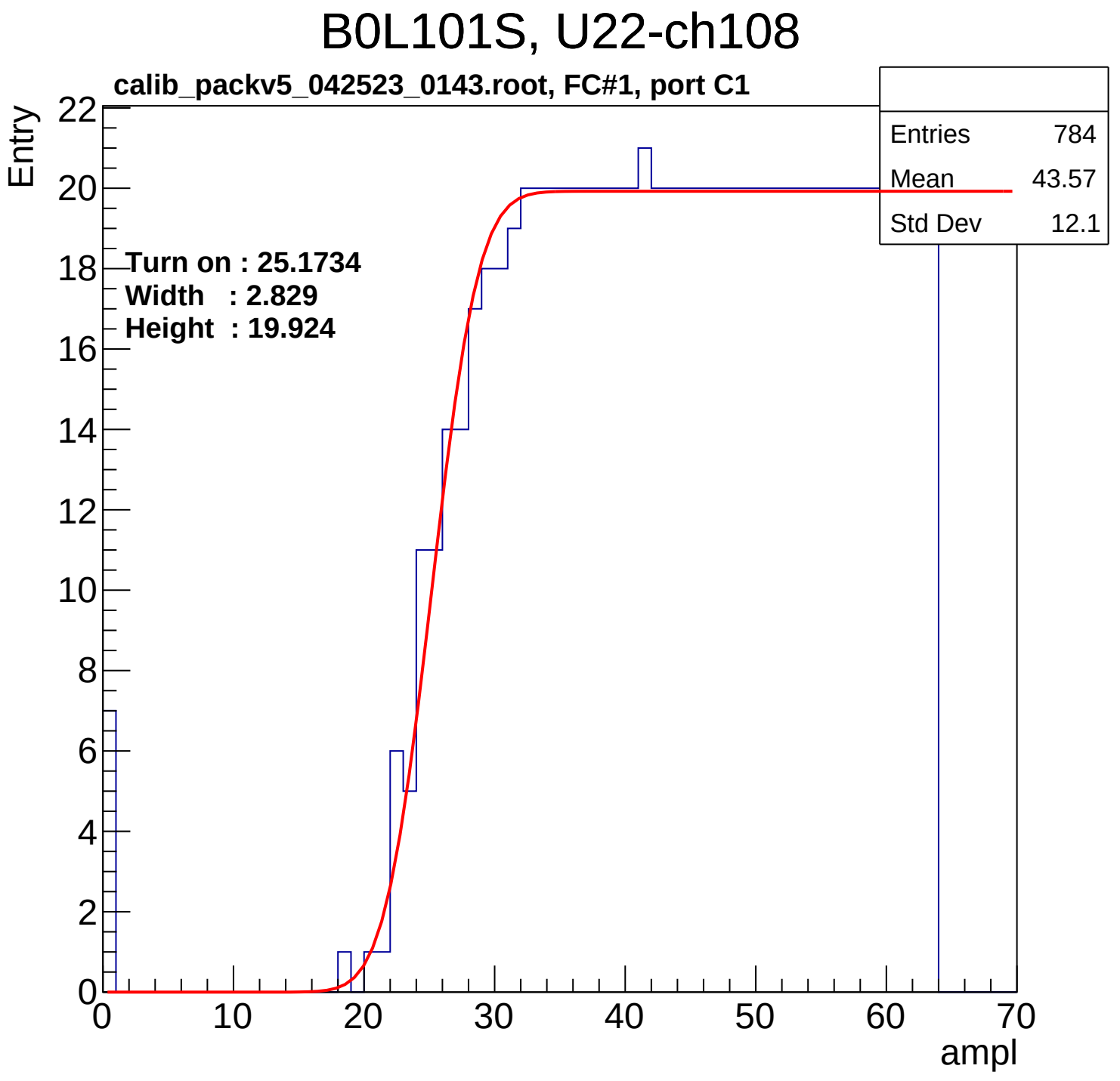

B0L101S, U22-ch103
calib_packv5_042523_0143.root, FC#1, port C1
Entries 727
Mean 45.11
Std Dev 10.96
Turn on : 28.1979
Width : 3.757
Height : 20.156
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

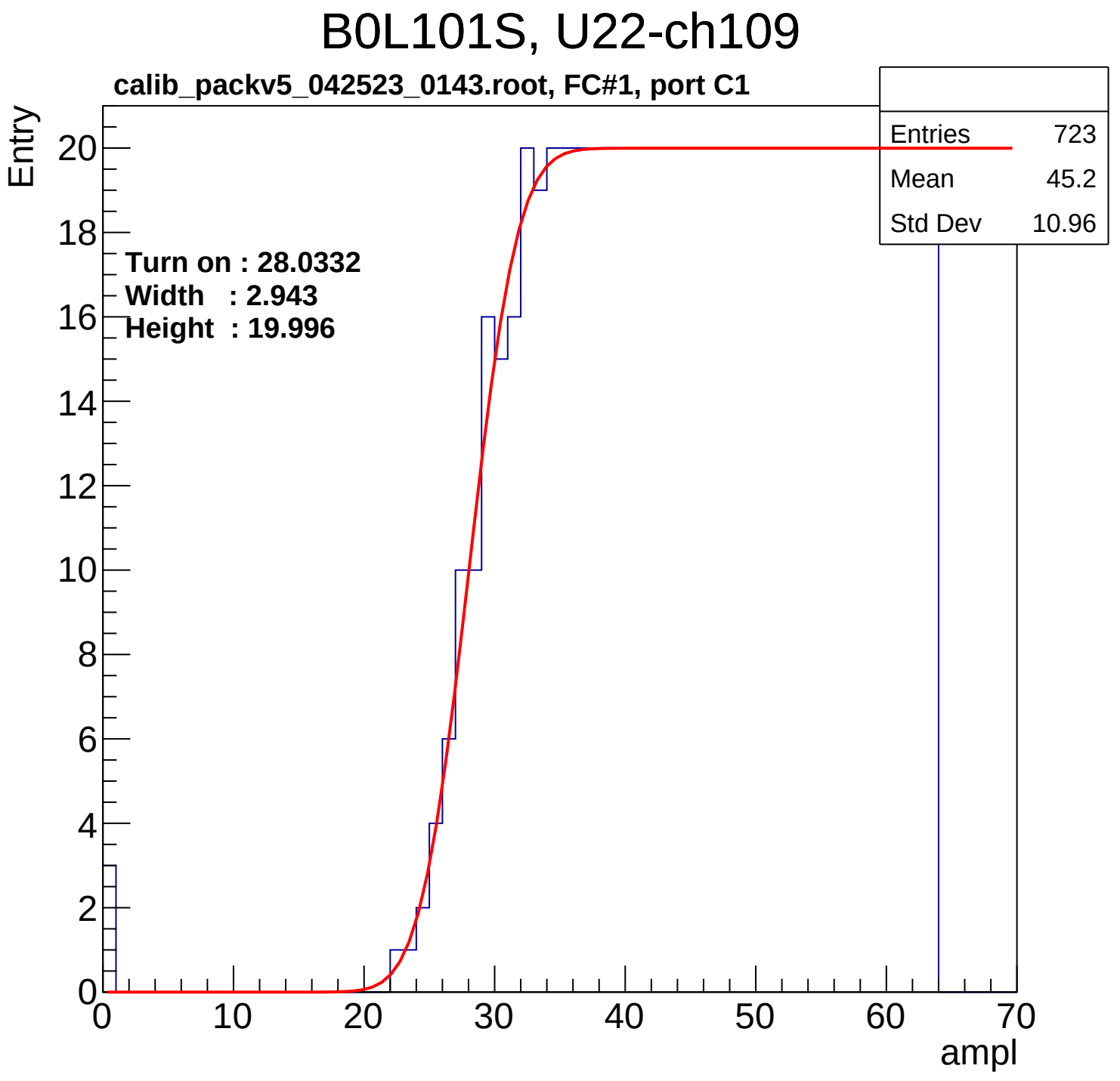

B0L101S, U22-ch104
calib_packv5_042523_0143.root, FC#1, port C1
Entries 778
Mean 43.86
Std Dev 11.61
Turn on : 25.2935
Width : 2.968
Height : 20.000
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

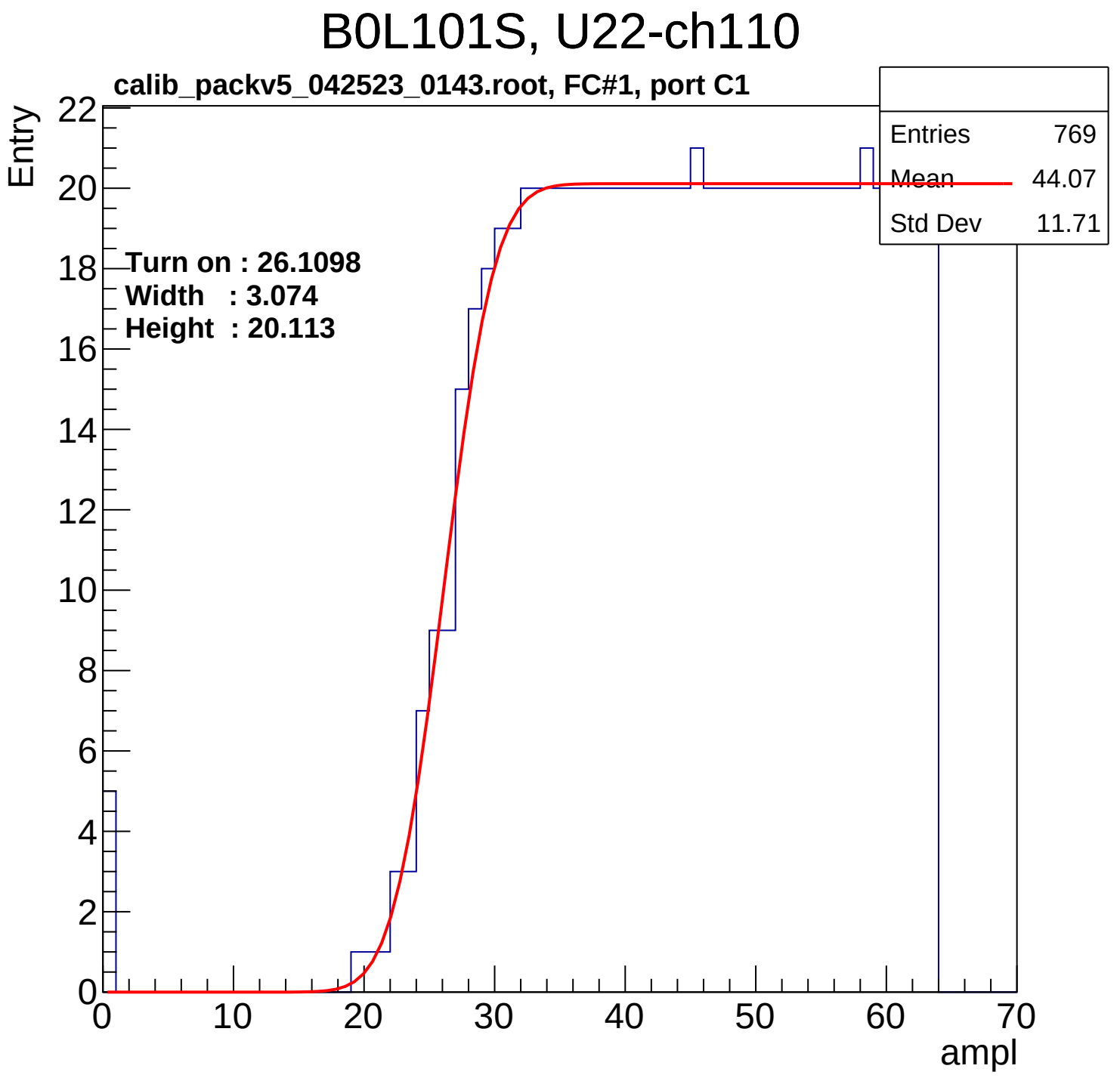

B0L101S, U22-ch105
calib_packv5_042523_0143.root, FC#1, port C1
Entries 768
Mean 43.97
Std Dev 11.82
Turn on : 26.3845
Width : 3.965
Height : 20.151
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

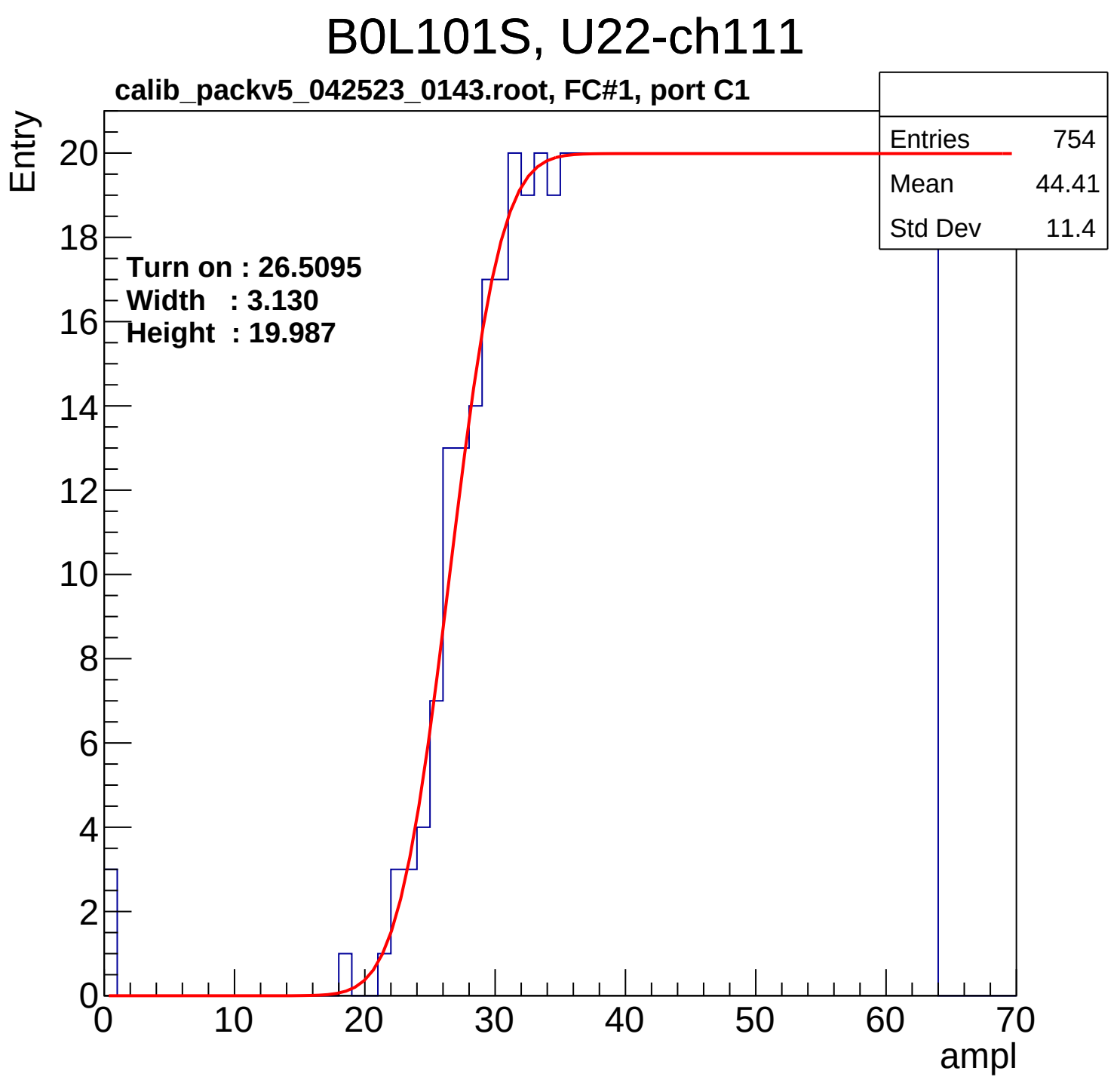

B0L101S, U22-ch106
calib_packv5_042523_0143.root, FC#1, port C1
Entries 834
Mean 42.57
Std Dev 12.45
Turn on : 23.0640
Width : 3.054
Height : 20.149
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70

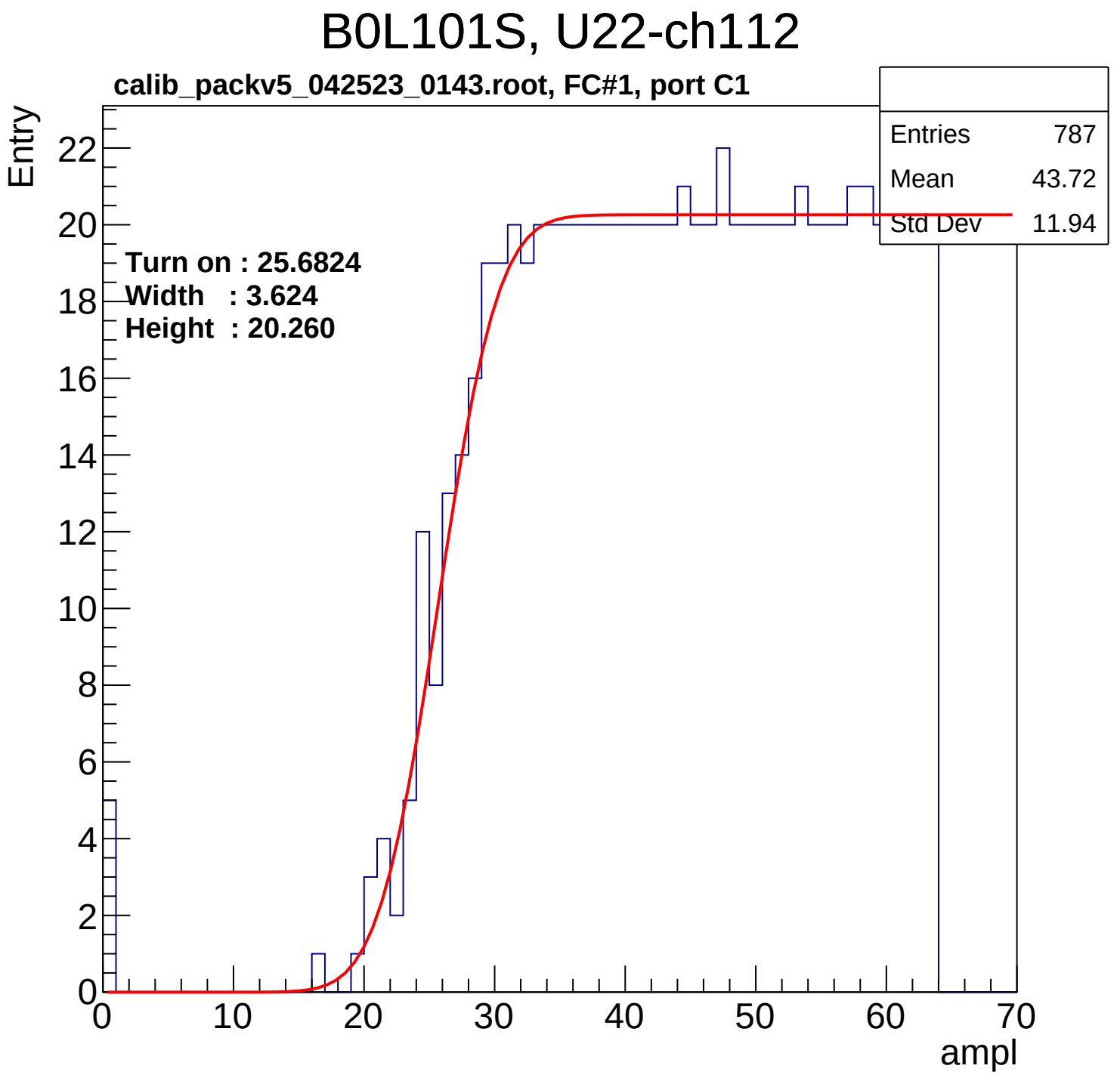

B0L101S, U22-ch107
calib_packv5_042523_0143.root, FC#1, port C1
Entries 789
Mean 43.59
Std Dev 11.79
Turn on : 24.7267
Width : 2.610
Height : 19.957
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

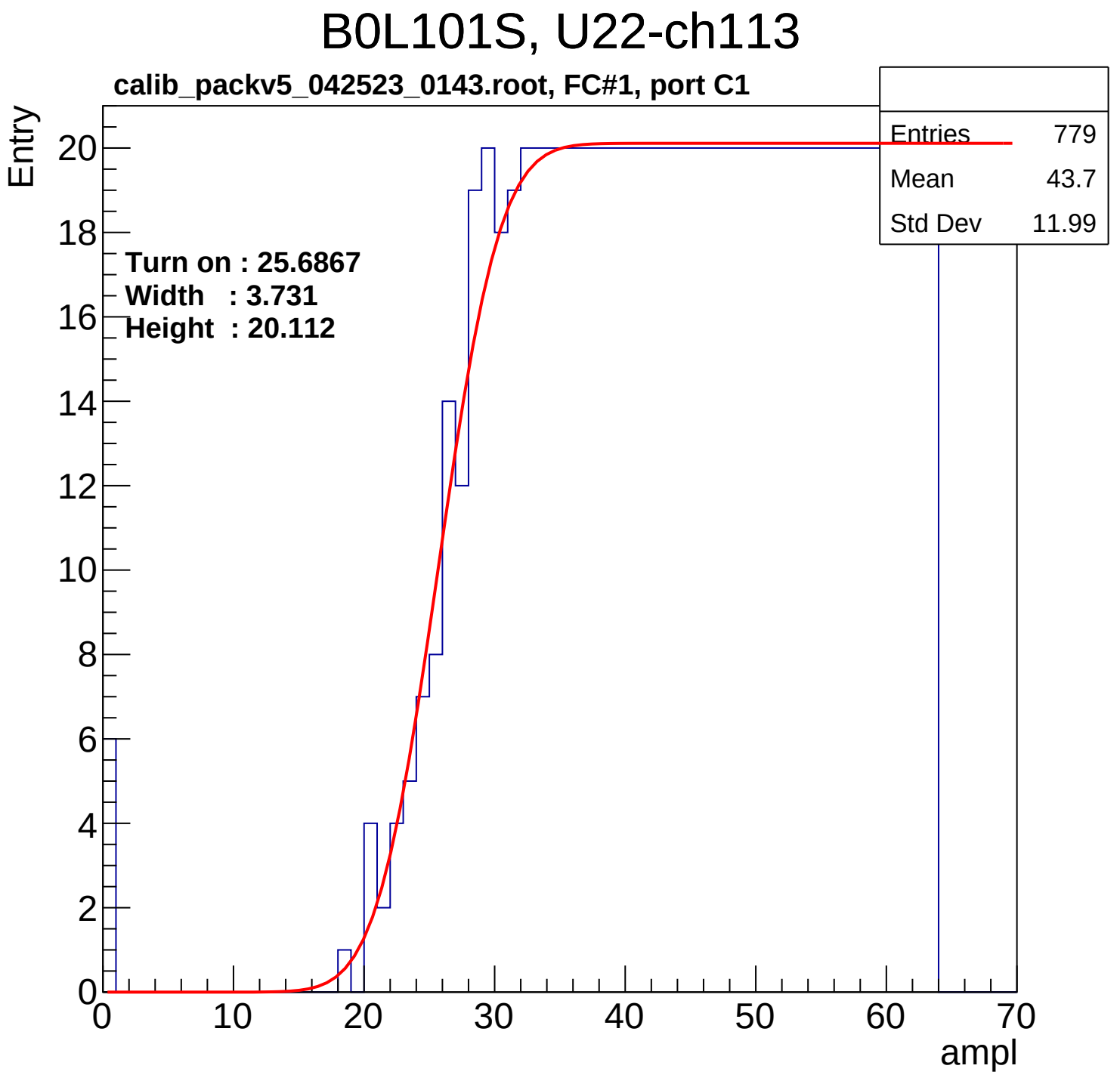

B0L101S, U22-ch108
calib_packv5_042523_0143.root, FC#1, port C1
Entries 784
Mean 43.57
Std Dev 12.1
Turn on : 25.1734
Width : 2.829
Height : 19.924
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70

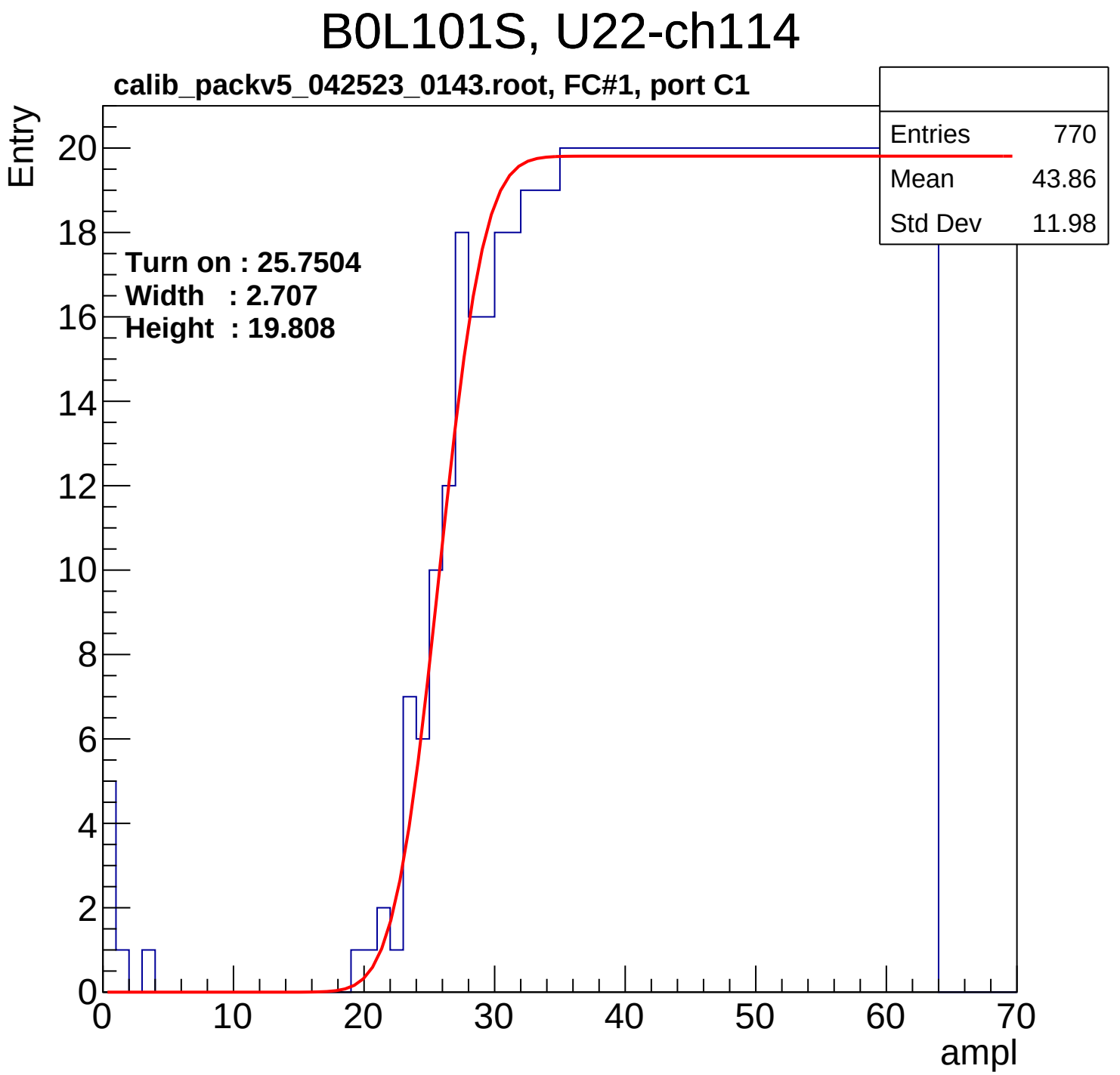

B0L101S, U22-ch109
calib_packv5_042523_0143.root, FC#1, port C1
Entries 723
Mean 45.2
Std Dev 10.96
Turn on : 28.0332
Width : 2.943
Height : 19.996
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

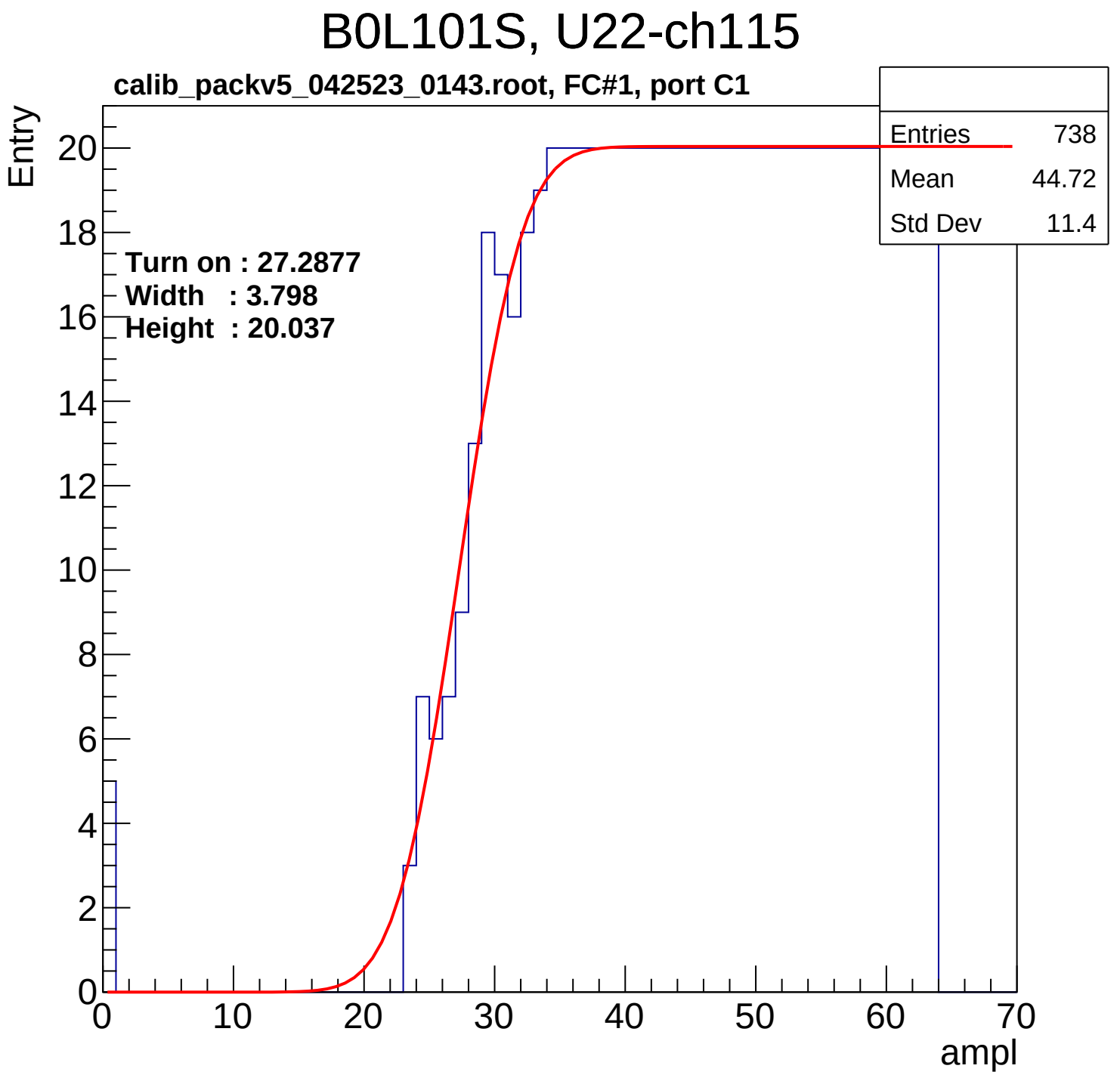

B0L101S, U22-ch110
calib_packv5_042523_0143.root, FC#1, port C1
Entries 769
Mean 44.07
Std Dev 11.71
Turn on : 26.1098
Width : 3.074
Height : 20.113
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70

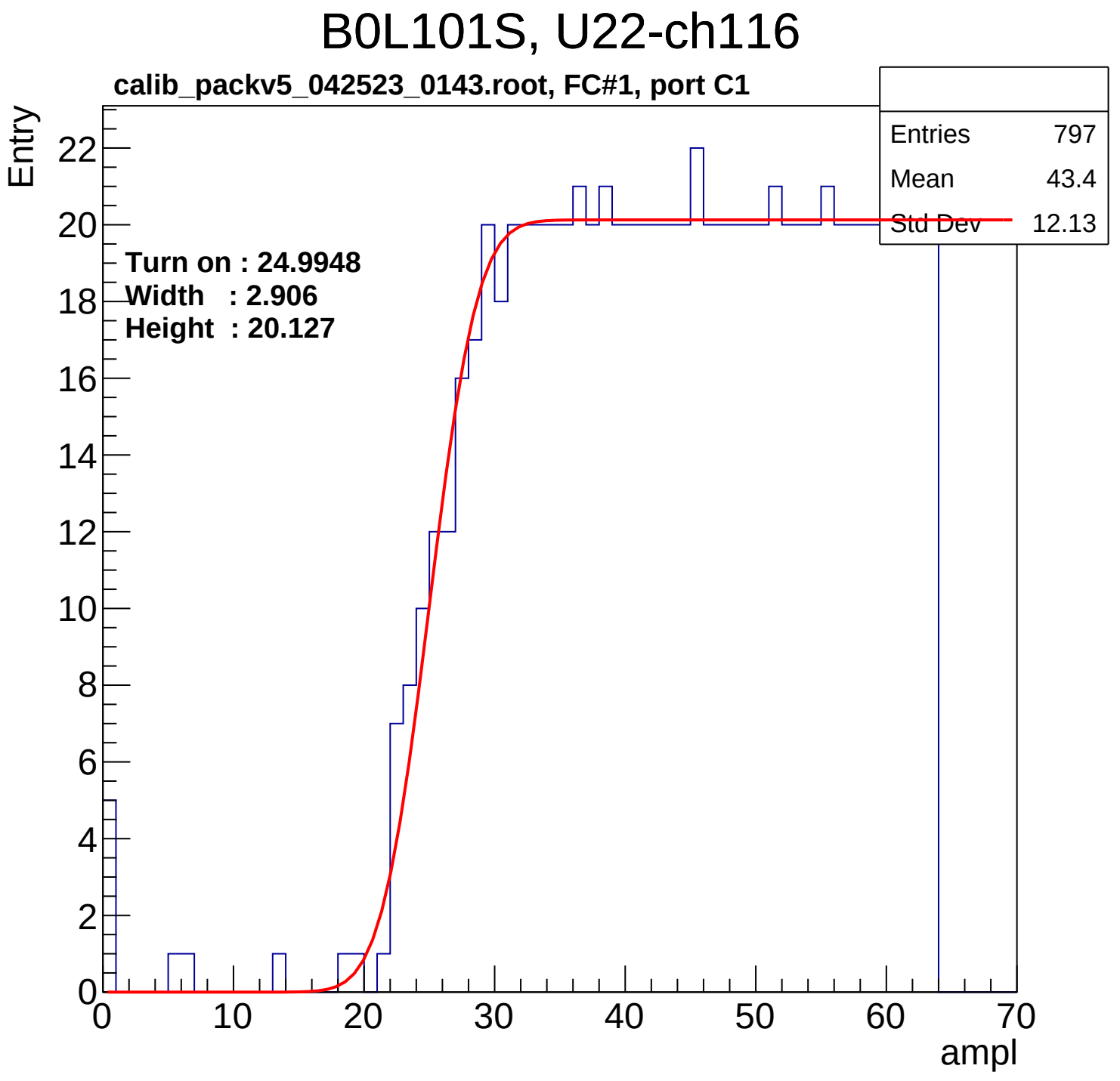

B0L101S, U22-ch111
calib_packv5_042523_0143.root, FC#1, port C1
Entries 754
Mean 44.41
Std Dev 11.4
Turn on : 26.5095
Width : 3.130
Height : 19.987
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

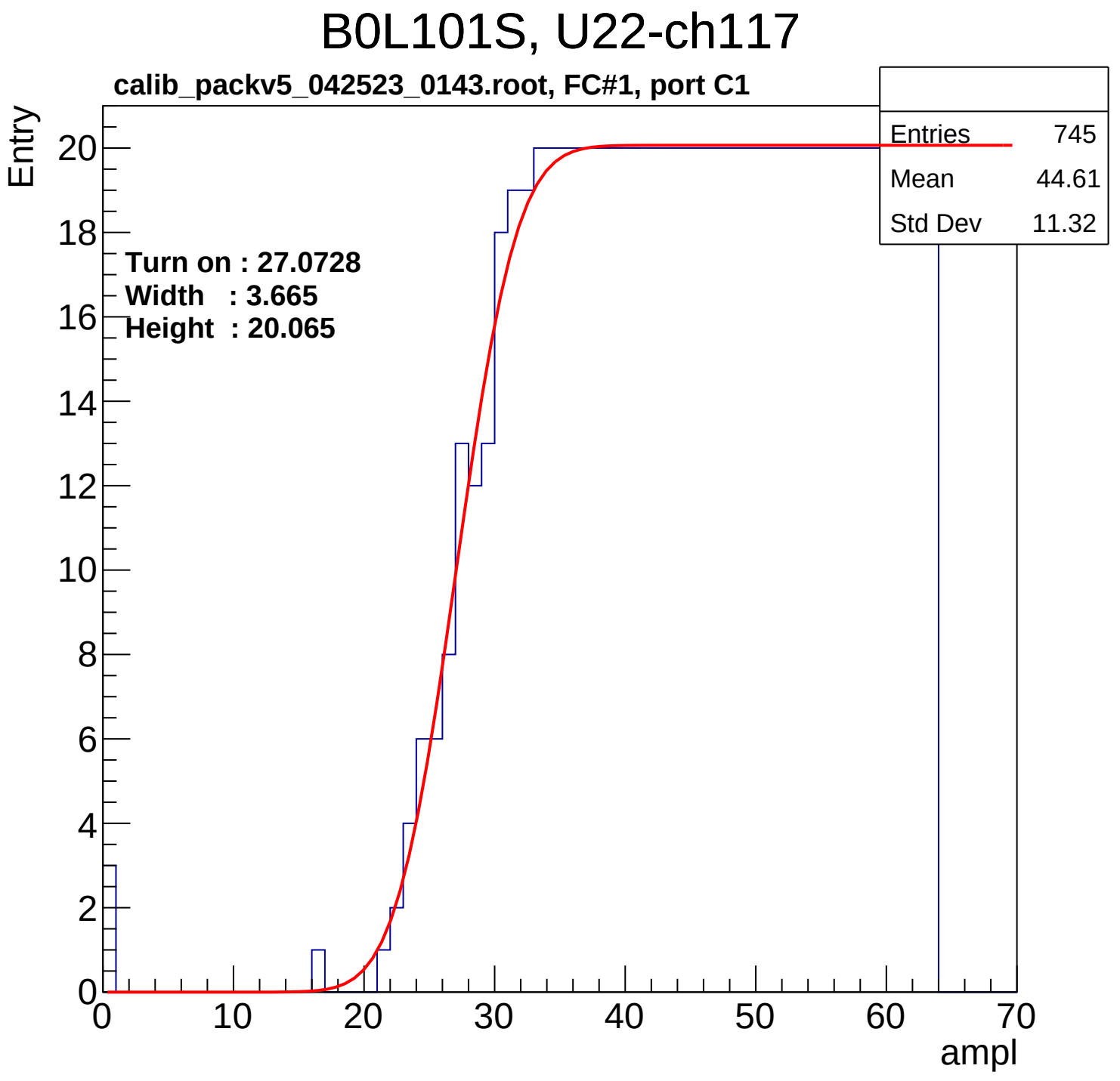

B0L101S, U22-ch112
calib_packv5_042523_0143.root, FC#1, port C1
Entries 787
Mean 43.72
Std Dev 11.94
Turn on : 25.6824
Width : 3.624
Height : 20.260
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70

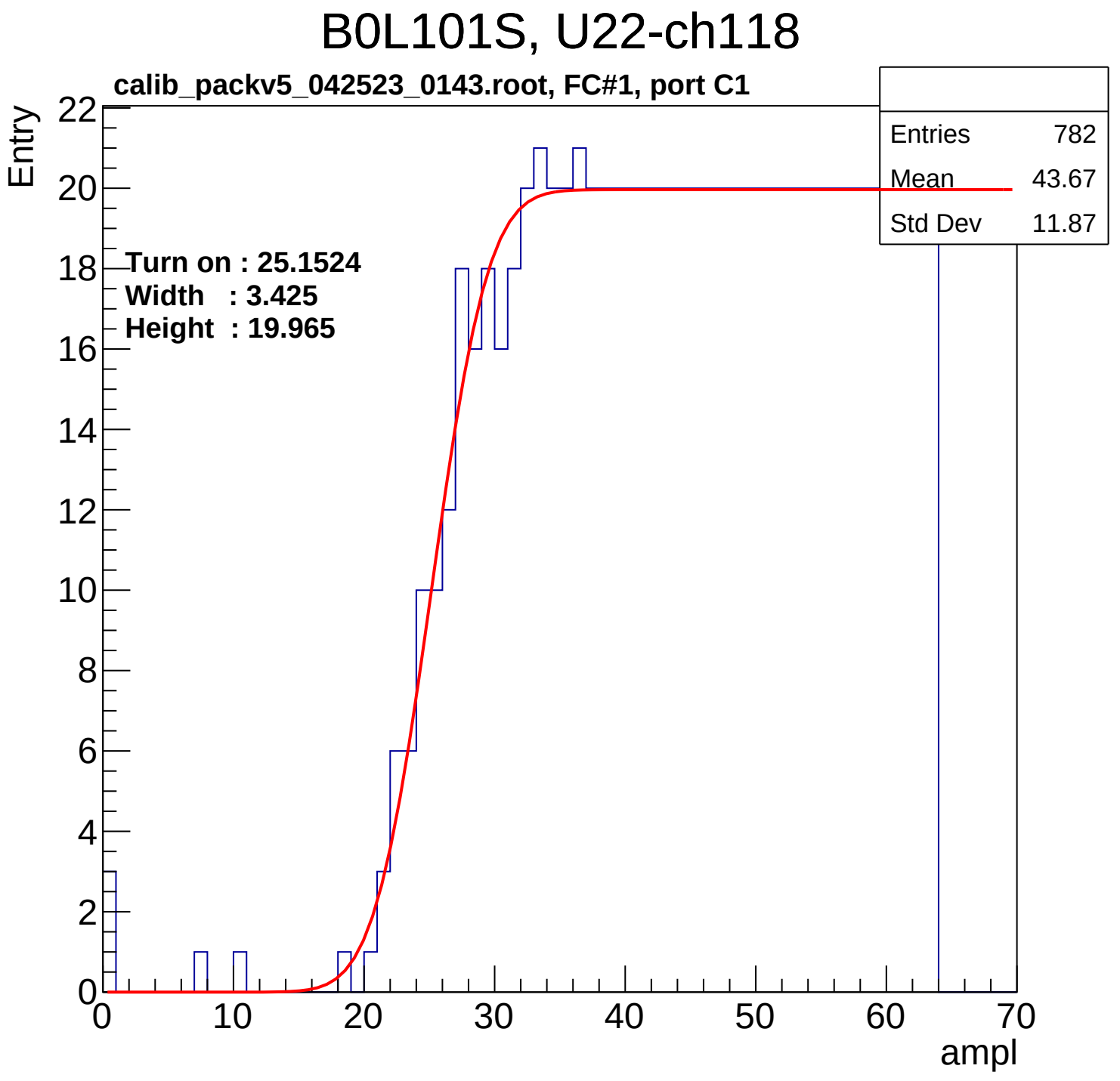

B0L101S, U22-ch113
calib_packv5_042523_0143.root, FC#1, port C1
Entries 779
Mean 43.7
Std Dev 11.99
Turn on : 25.6867
Width : 3.731
Height : 20.112
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

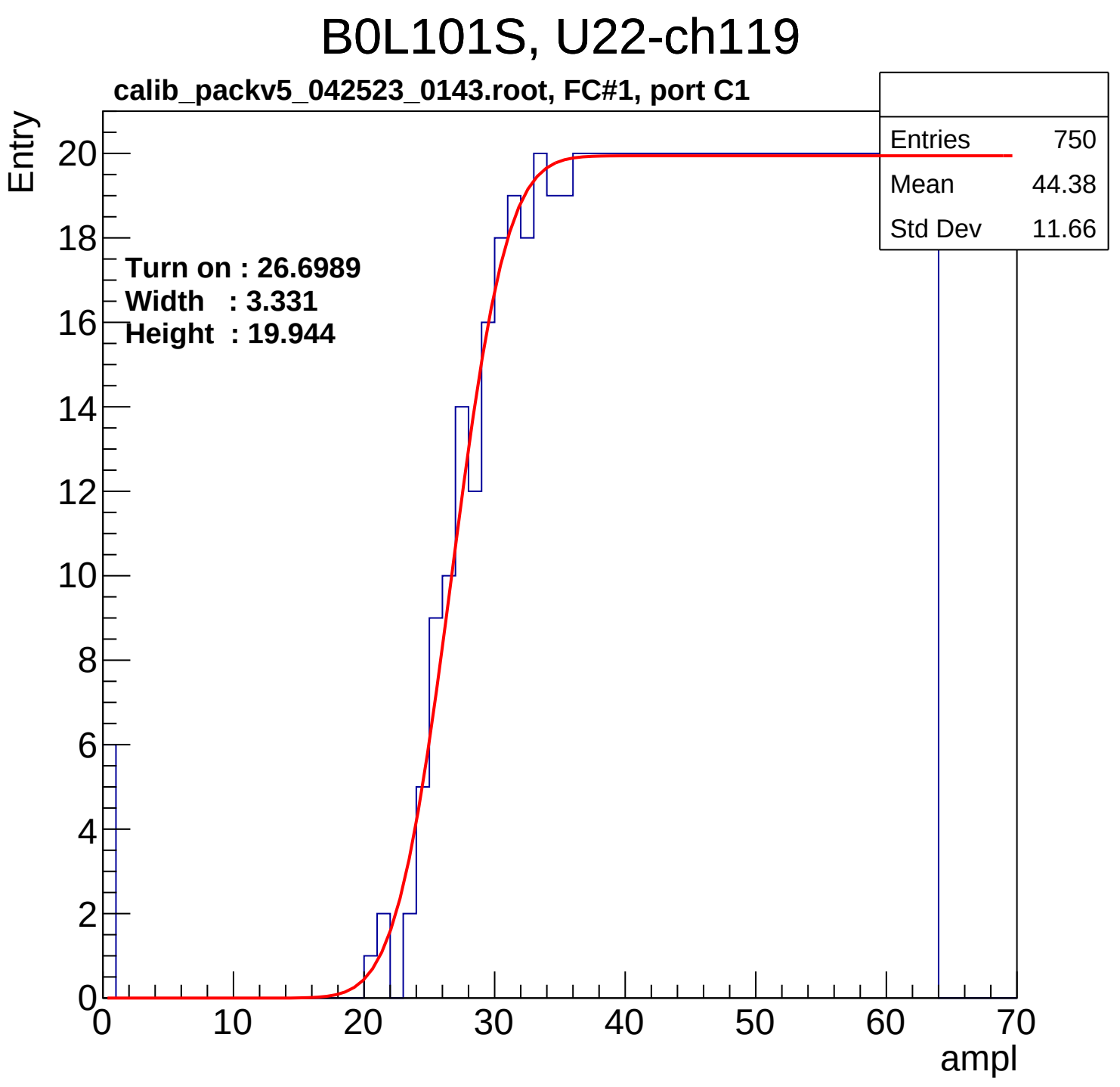

B0L101S, U22-ch114
calib_packv5_042523_0143.root, FC#1, port C1
Entries 770
Mean 43.86
Std Dev 11.98
Turn on : 25.7504
Width : 2.707
Height : 19.808
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

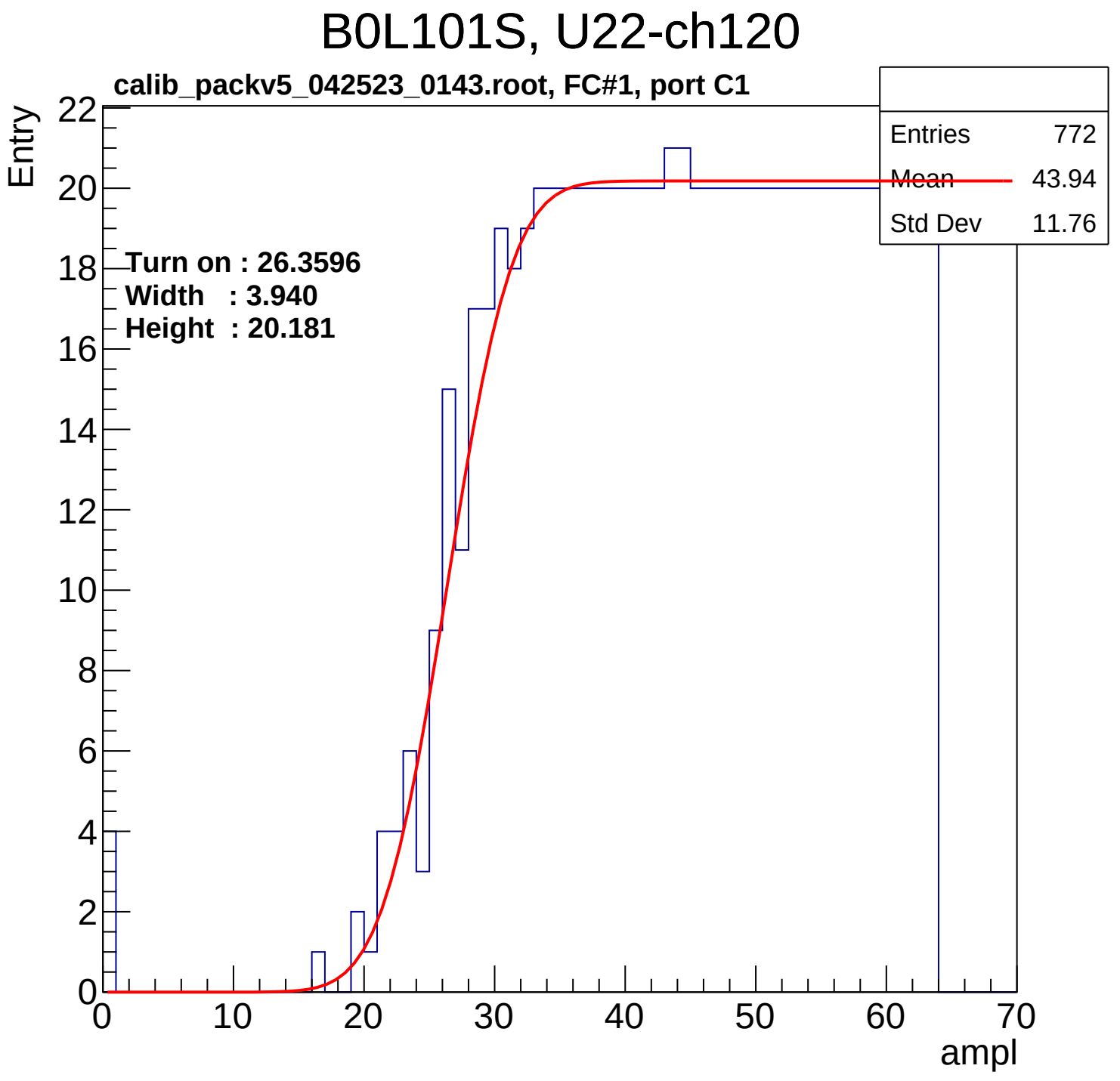

B0L101S, U22-ch115
calib_packv5_042523_0143.root, FC#1, port C1
Entries 738
Mean 44.72
Std Dev 11.4
Turn on : 27.2877
Width : 3.798
Height : 20.037
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

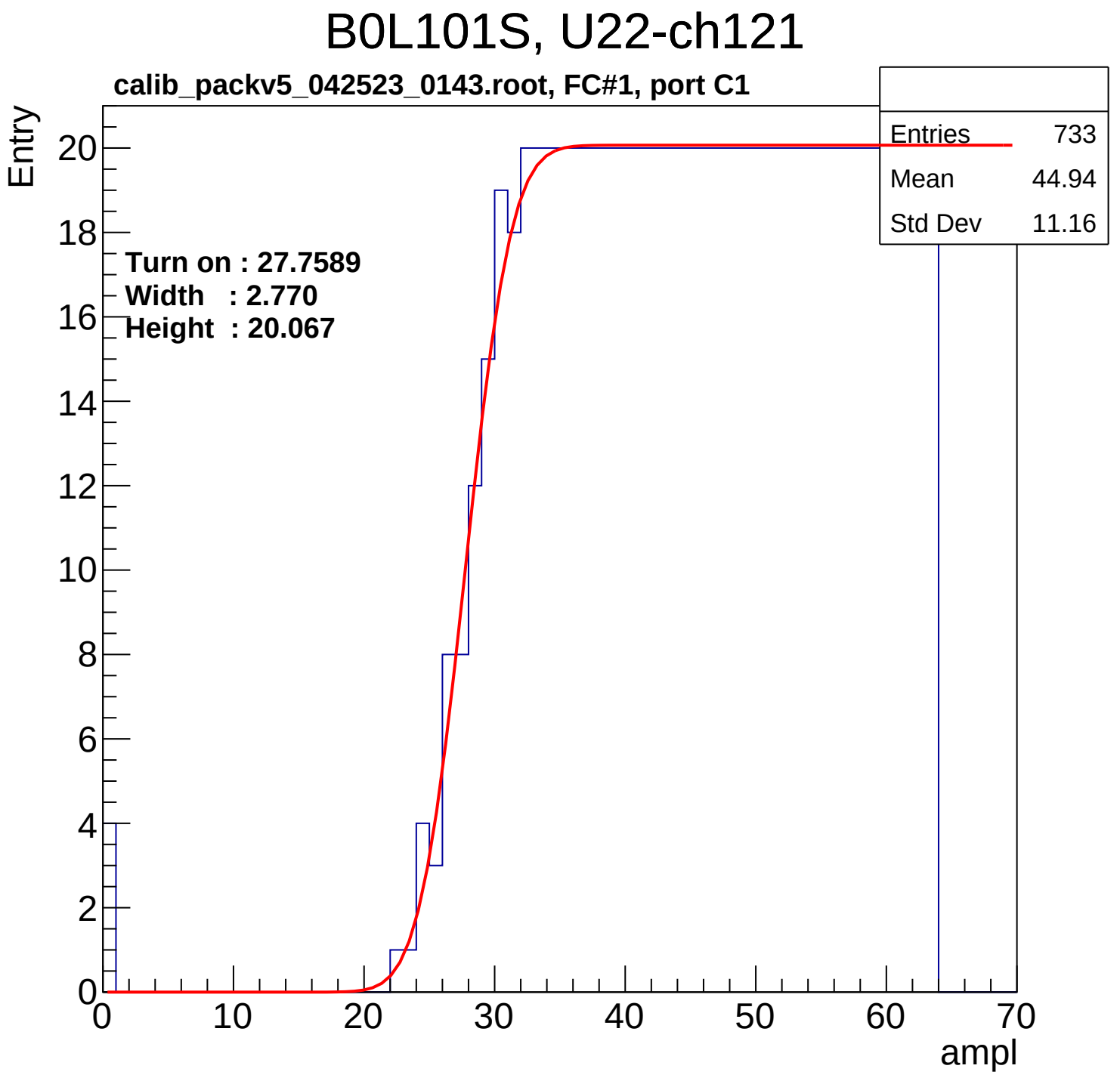

B0L101S, U22-ch116
calib_packv5_042523_0143.root, FC#1, port C1
Entries 797
Mean 43.4
Std Dev 12.13
Turn on : 24.9948
Width : 2.906
Height : 20.127
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70

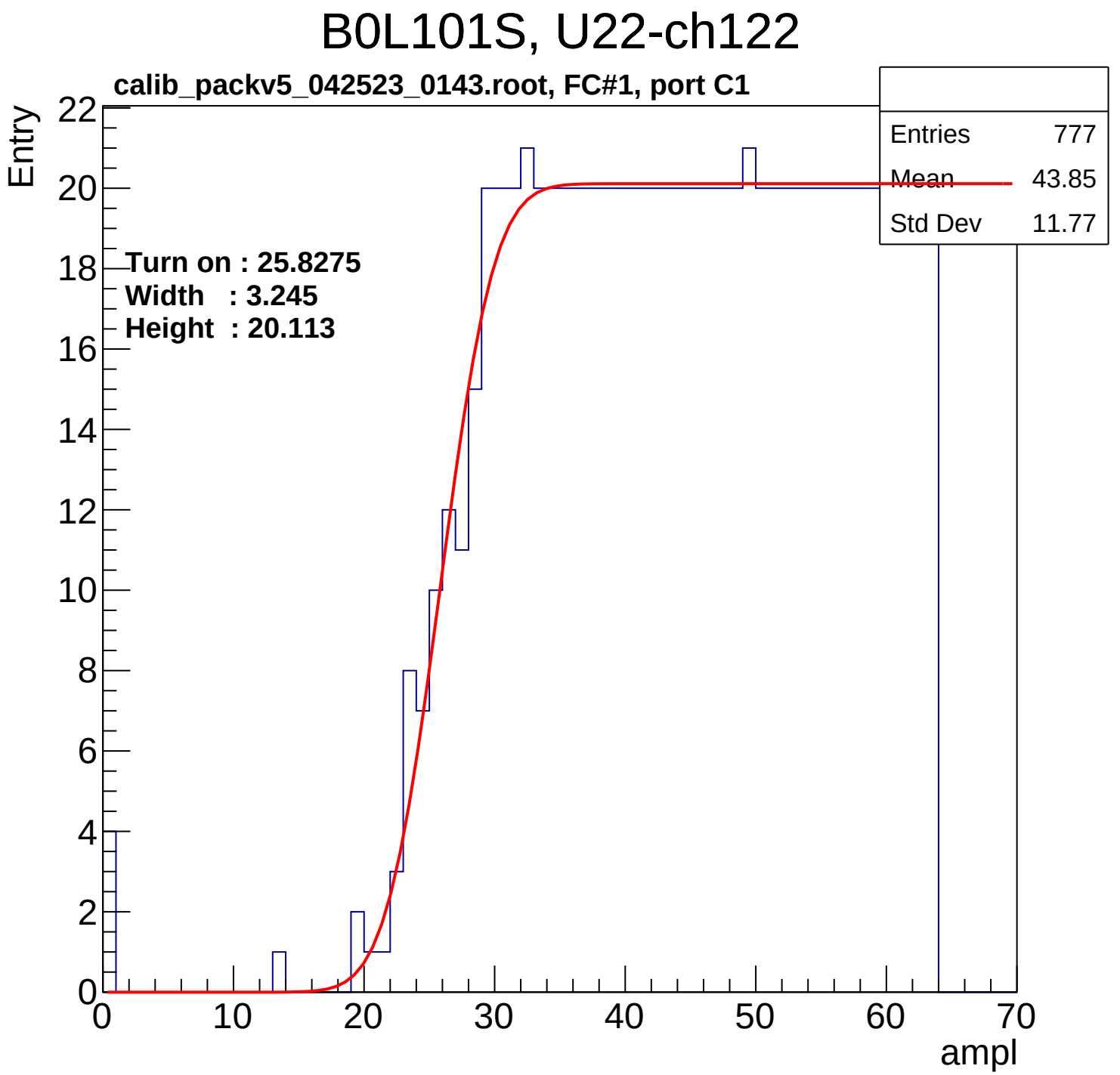

B0L101S, U22-ch117
calib_packv5_042523_0143.root, FC#1, port C1
Entries 745
Mean 44.61
Std Dev 11.32
Turn on : 27.0728
Width : 3.665
Height : 20.065
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

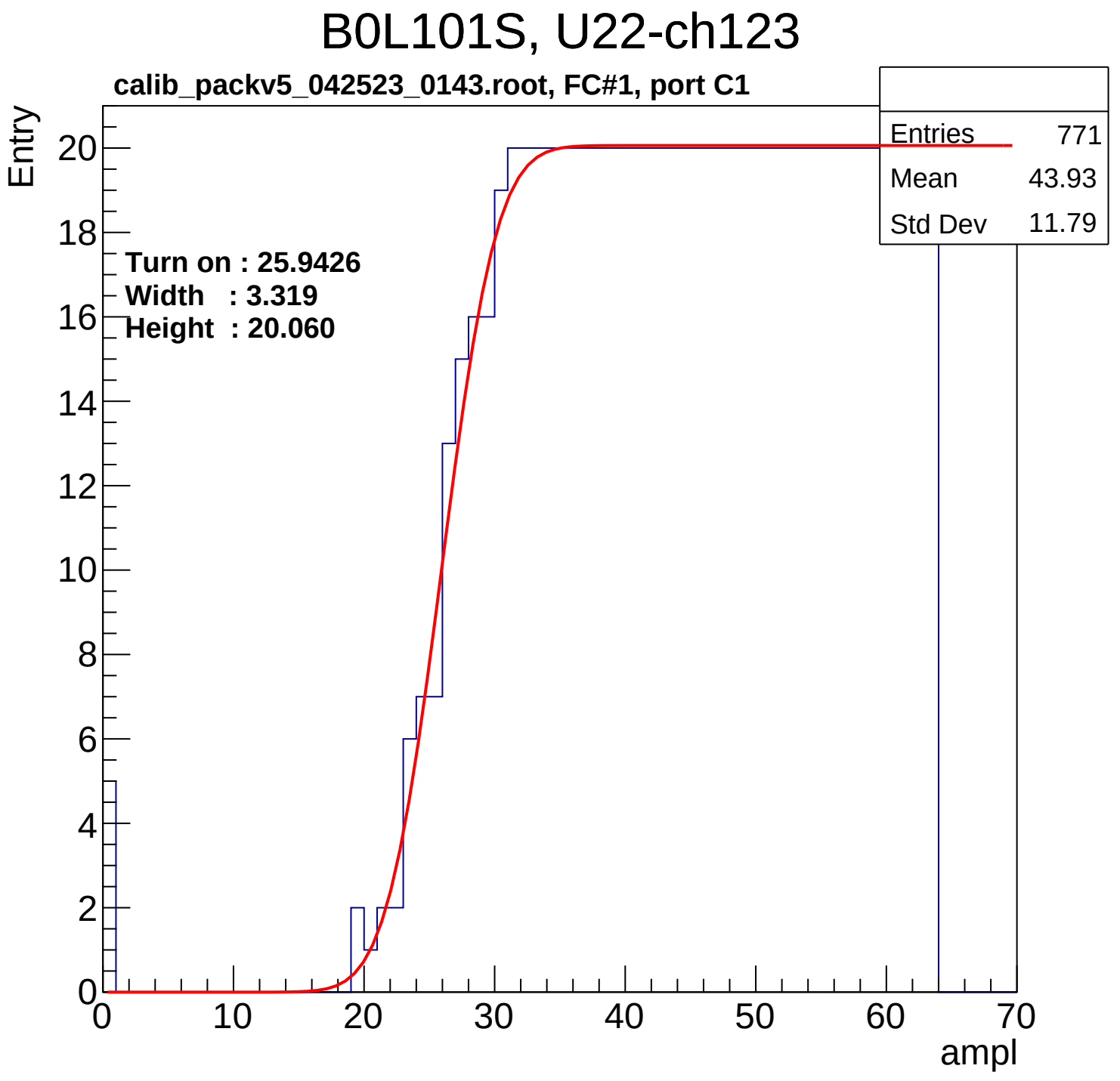

B0L101S, U22-ch118
calib_packv5_042523_0143.root, FC#1, port C1
Entries 782
Mean 43.67
Std Dev 11.87
Turn on : 25.1524
Width : 3.425
Height : 19.965
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70

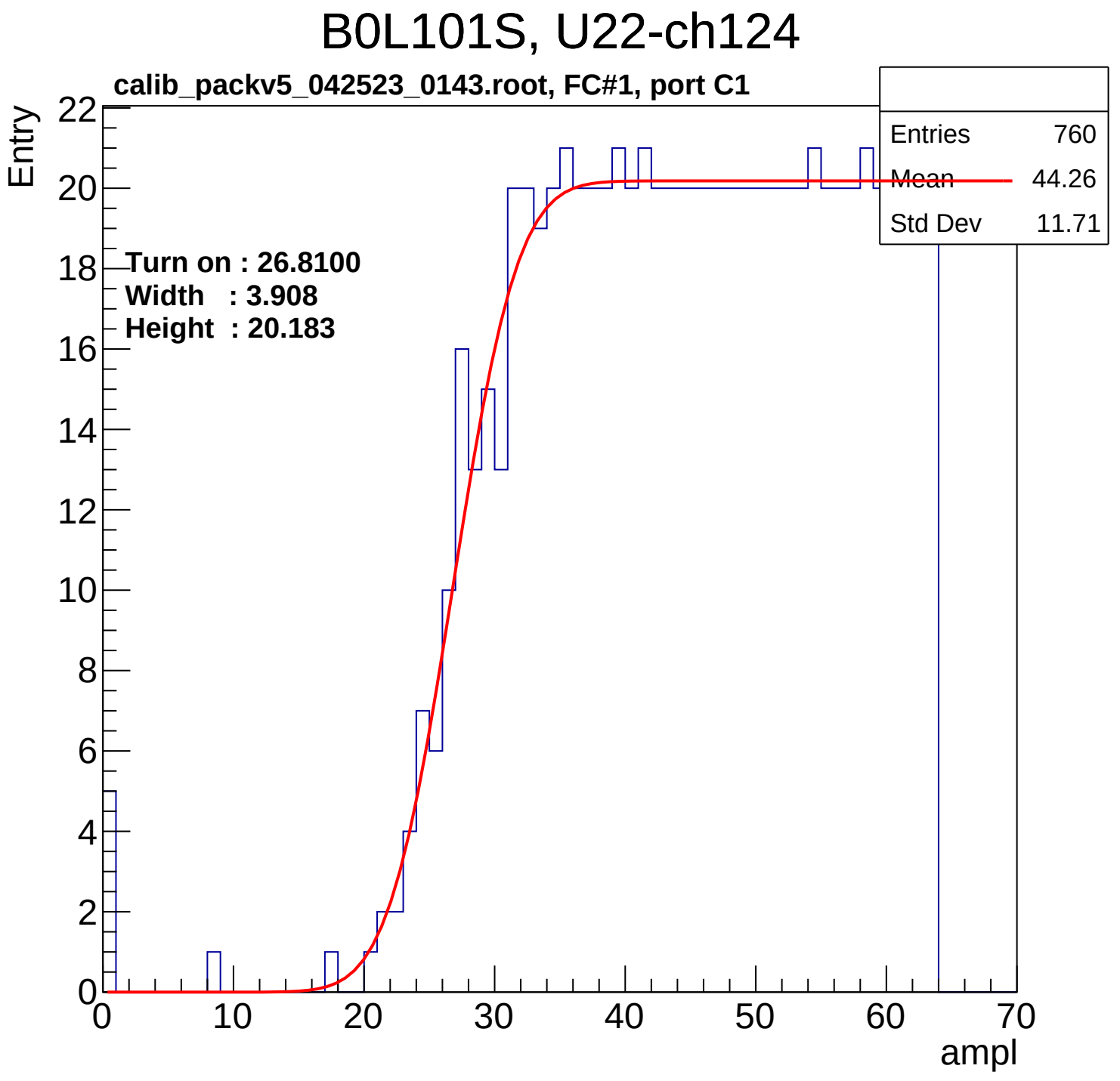

B0L101S, U22-ch119
calib_packv5_042523_0143.root, FC#1, port C1
Entries 750
Mean 44.38
Std Dev 11.66
Turn on : 26.6989
Width : 3.331
Height : 19.944
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

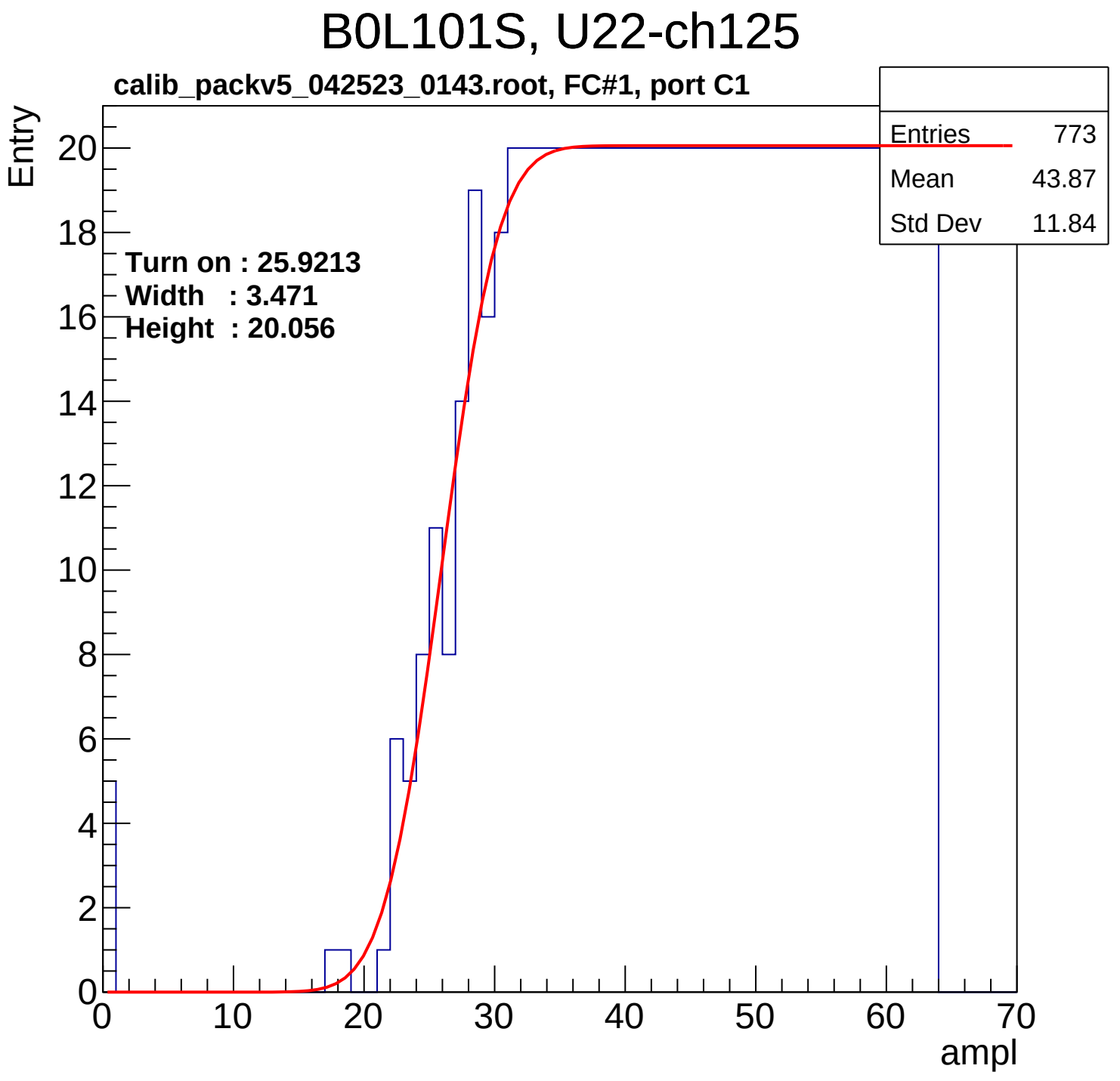

B0L101S, U22-ch120
calib_packv5_042523_0143.root, FC#1, port C1
Entries 772
Mean 43.94
Std Dev 11.76
Turn on : 26.3596
Width : 3.940
Height : 20.181
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70

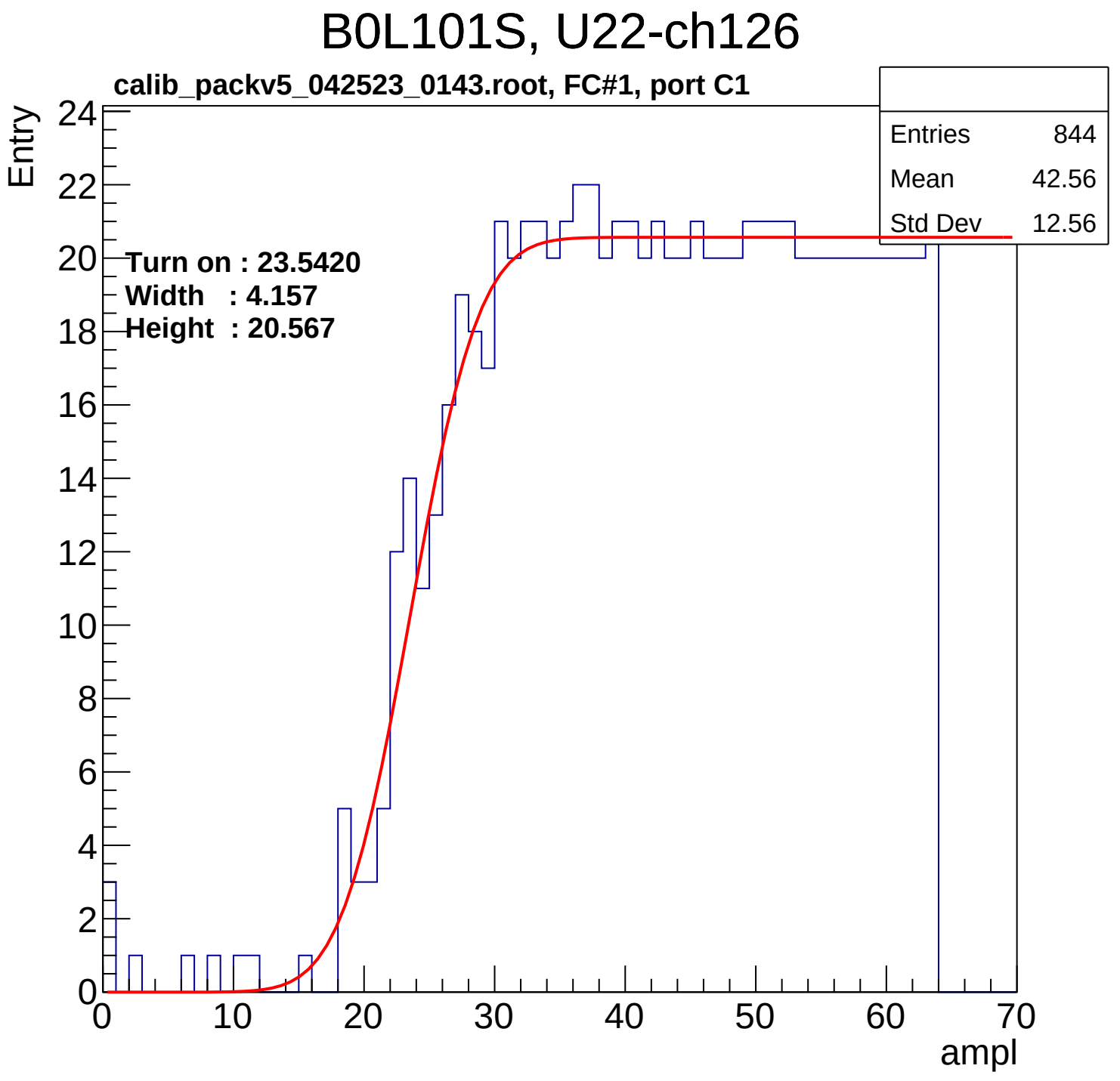

B0L101S, U22-ch121
calib_packv5_042523_0143.root, FC#1, port C1
Entries 733
Mean 44.94
Std Dev 11.16
Turn on : 27.7589
Width : 2.770
Height : 20.067
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

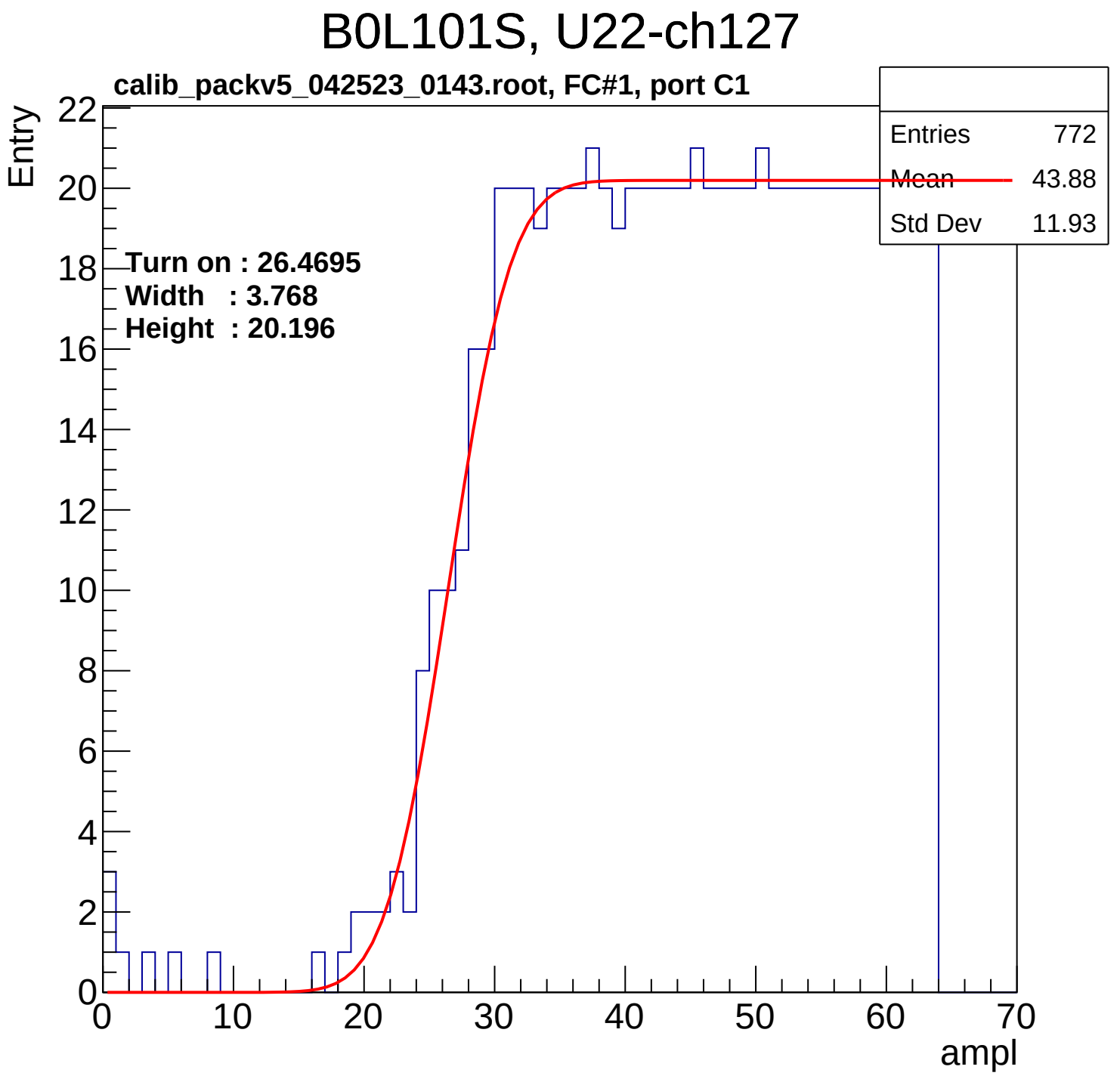

B0L101S, U22-ch122
calib_packv5_042523_0143.root, FC#1, port C1
Entries 777
Mean 43.85
Std Dev 11.77
Turn on : 25.8275
Width : 3.245
Height : 20.113
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70

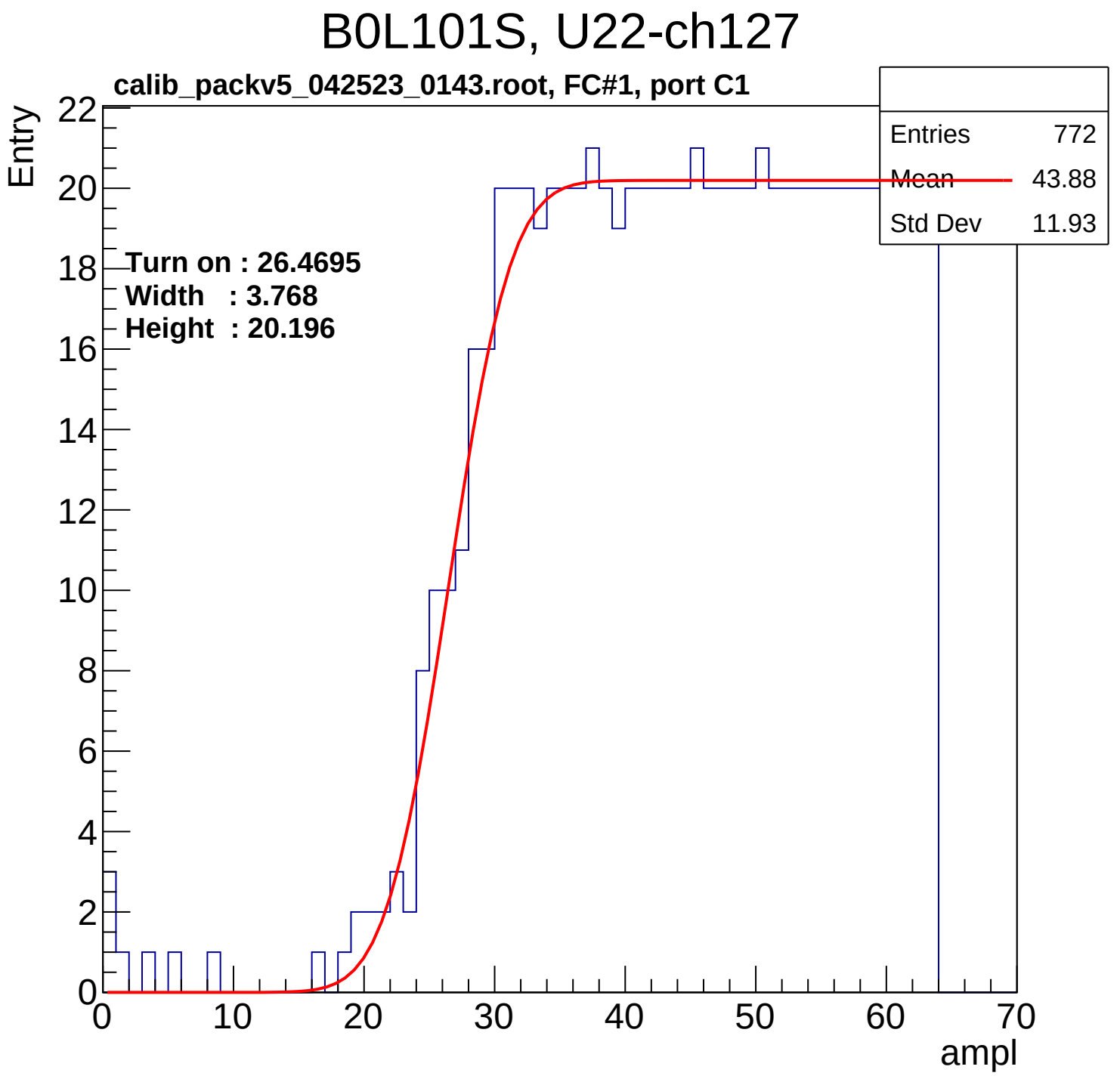

B0L101S, U22-ch123
calib_packv5_042523_0143.root, FC#1, port C1
Entries 771
Mean 43.93
Std Dev 11.79
Turn on : 25.9426
Width : 3.319
Height : 20.060
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70


B0L101S, U22-ch124
calib_packv5_042523_0143.root, FC#1, port C1
Entries 760
Mean 44.26
Std Dev 11.71
Turn on : 26.8100
Width : 3.908
Height : 20.183
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70


B0L101S, U22-ch125
calib_packv5_042523_0143.root, FC#1, port C1
Entries 773
Mean 43.87
Std Dev 11.84
Turn on : 25.9213
Width : 3.471
Height : 20.056
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70


B0L101S, U22-ch126
calib_packv5_042523_0143.root, FC#1, port C1
Entries 844
Mean 42.56
Std Dev 12.56
Turn on : 23.5420
Width : 4.157
Height : 20.567
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
24
0
10
20
30
40
50
60
70


B0L101S, U22-ch127
calib_packv5_042523_0143.root, FC#1, port C1
Entries 772
Mean 43.88
Std Dev 11.93
Turn on : 26.4695
Width : 3.768
Height : 20.196
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70


B0L101S, U22-ch127
calib_packv5_042523_0143.root, FC#1, port C1
Entries 772
Mean 43.88
Std Dev 11.93
Turn on : 26.4695
Width : 3.768
Height : 20.196
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70