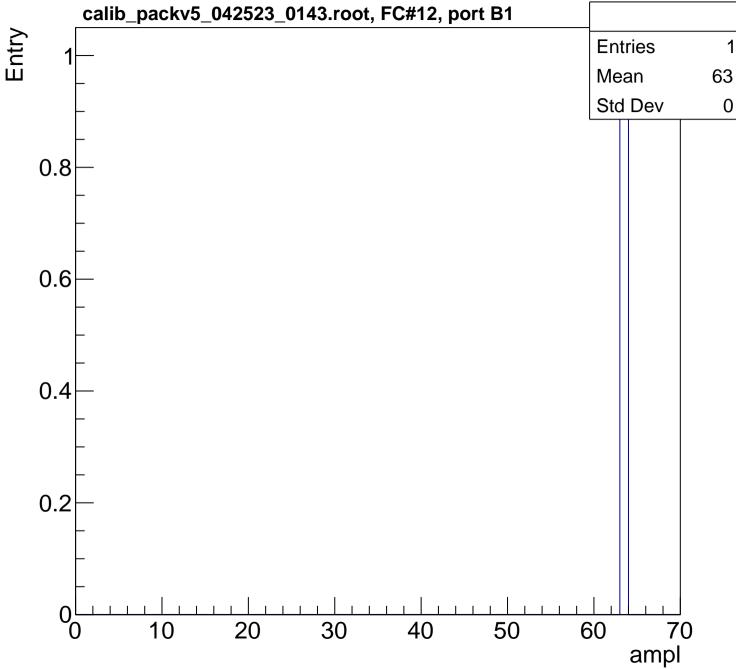
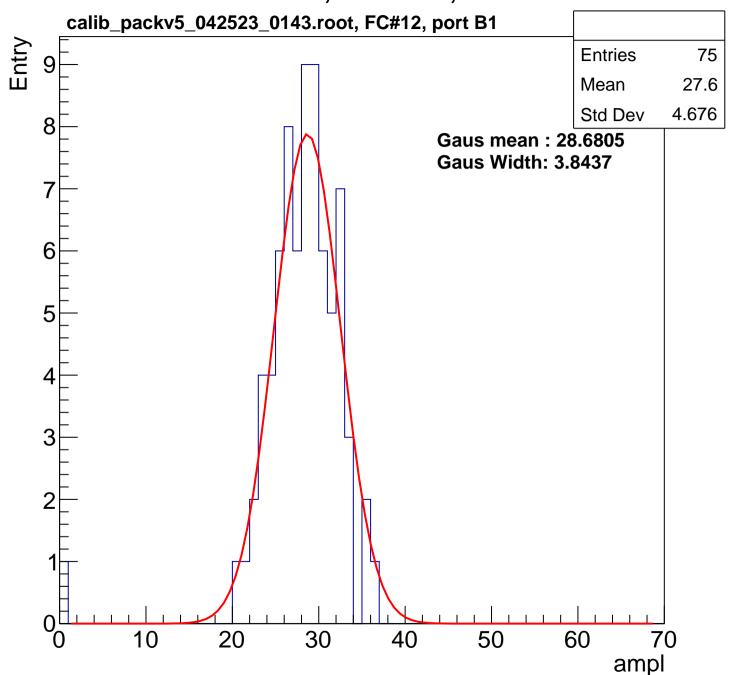
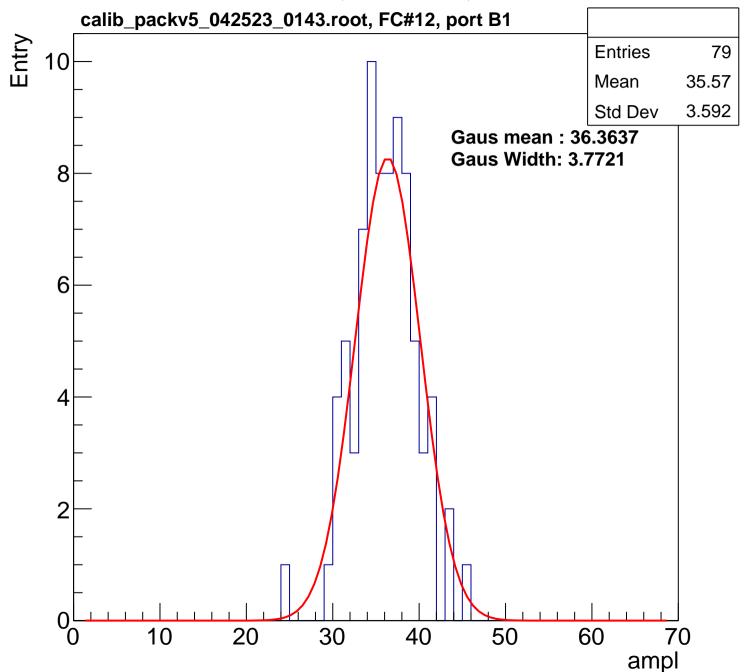
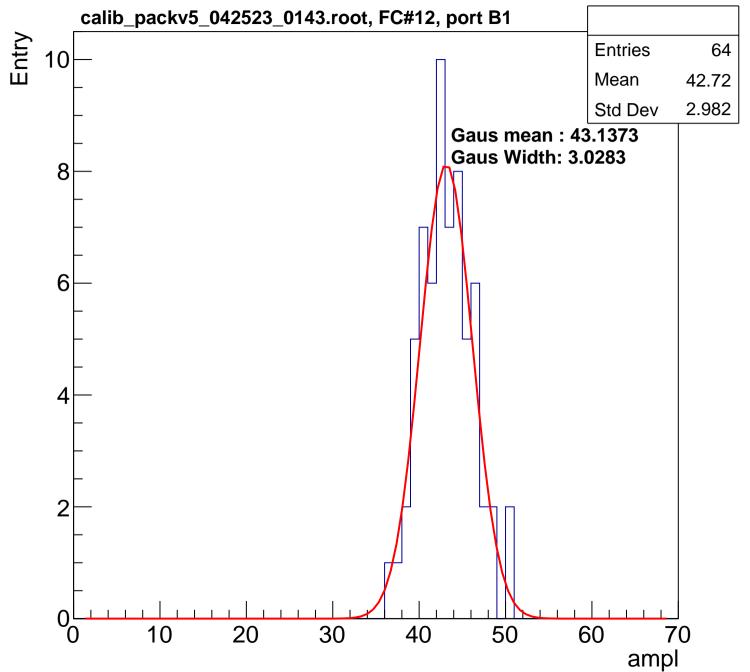


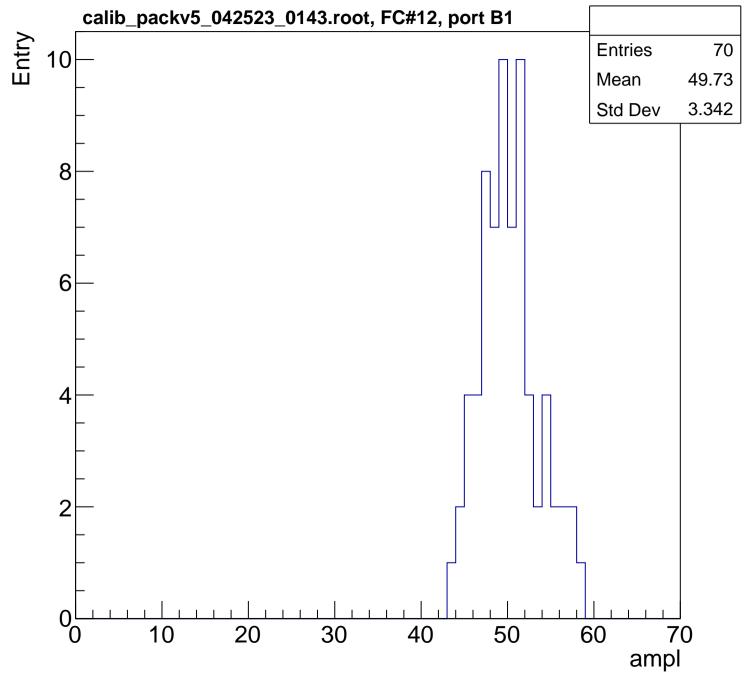
0

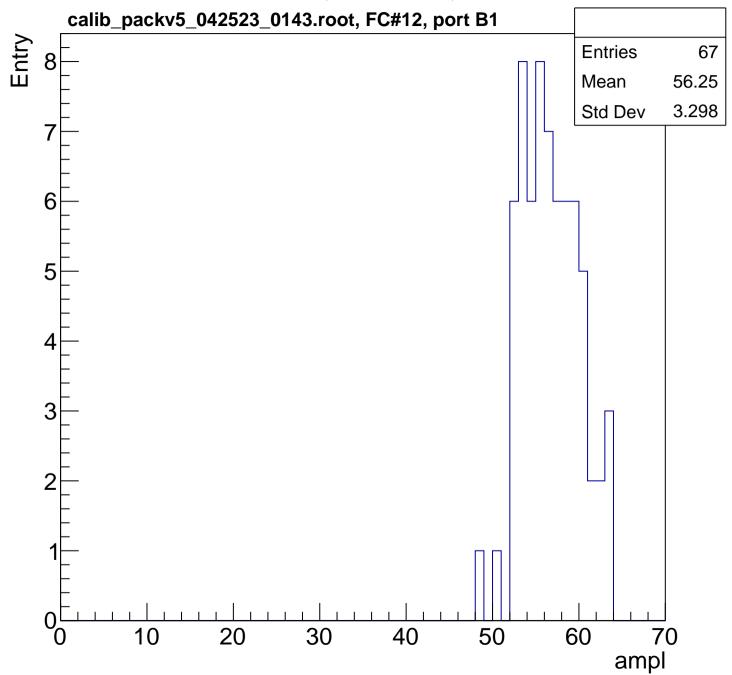


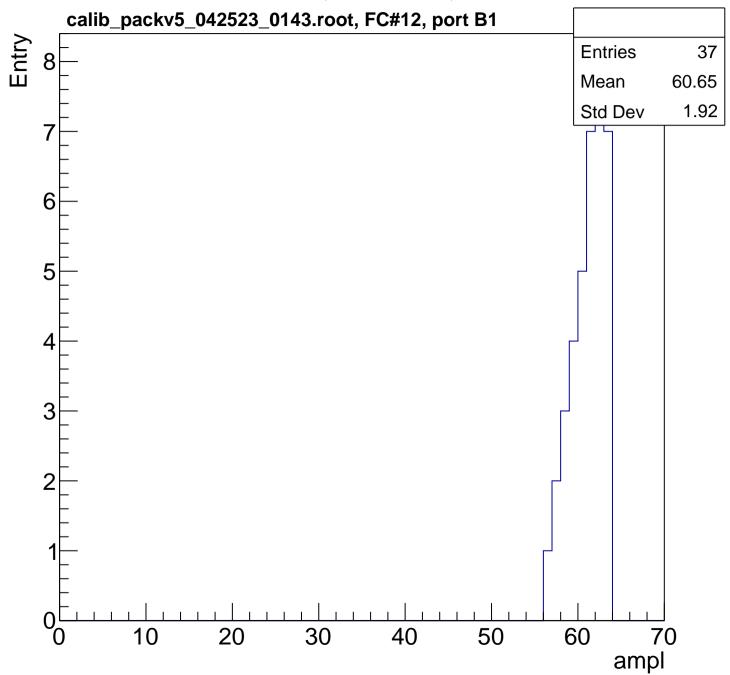


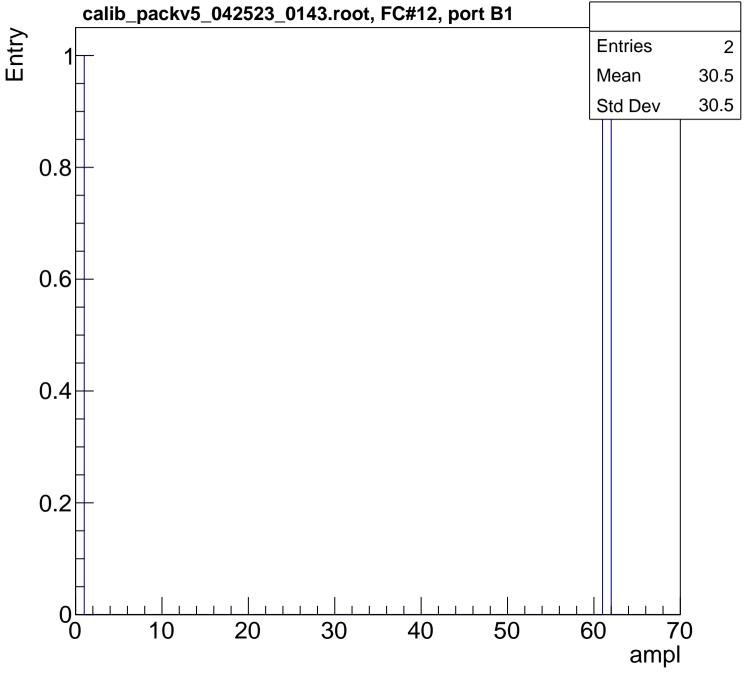




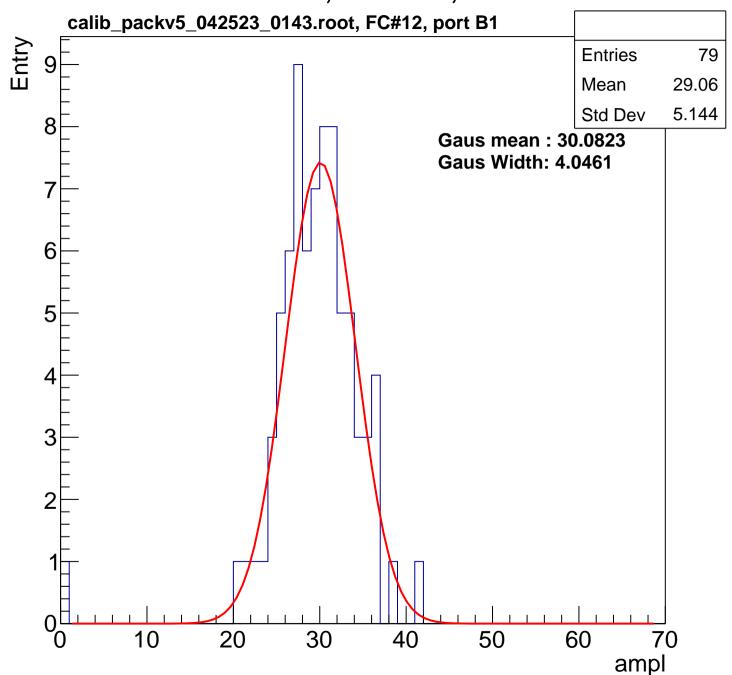


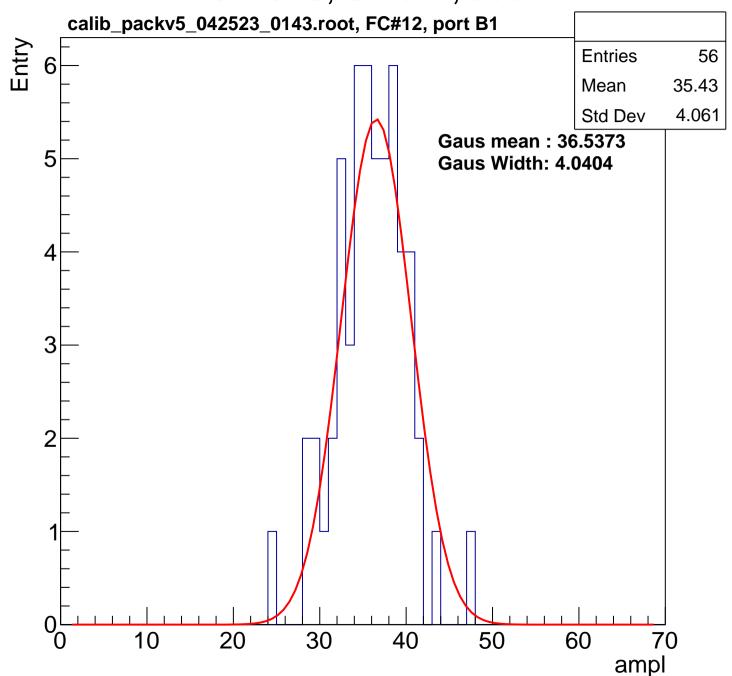


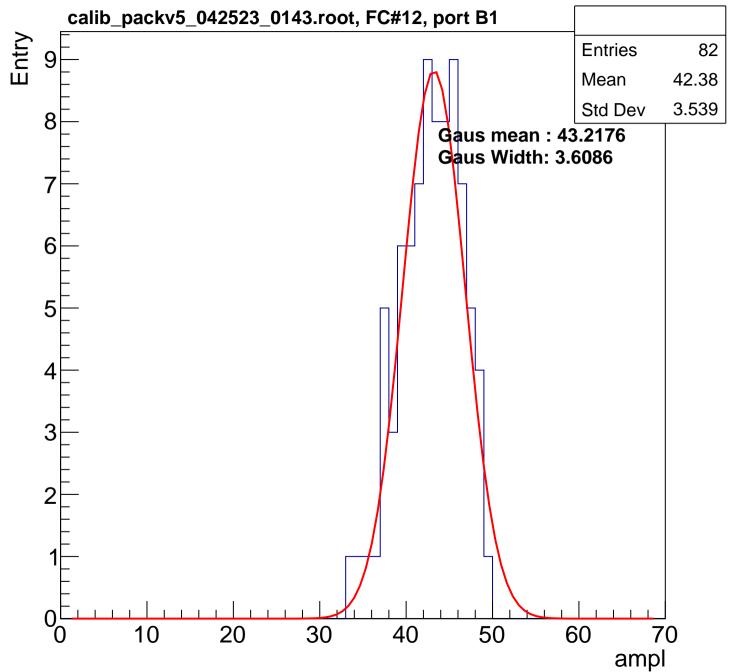


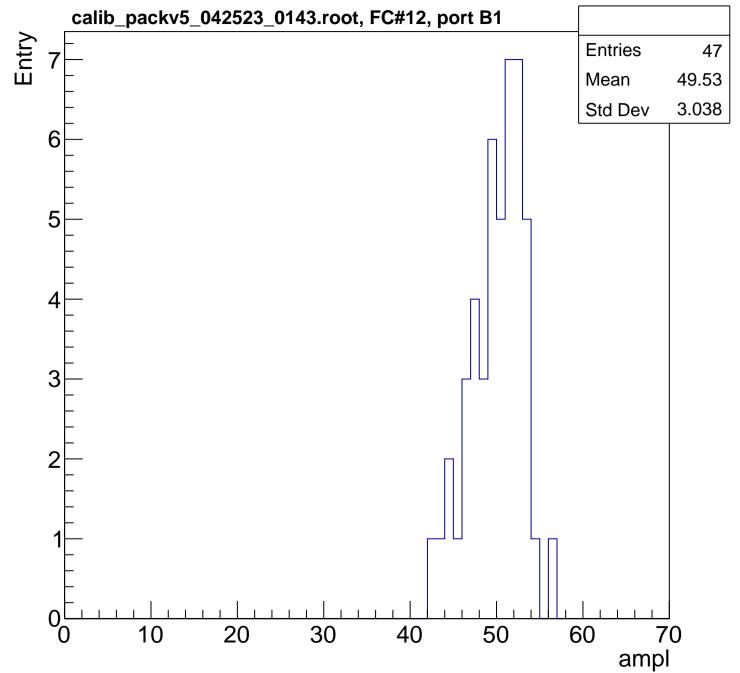


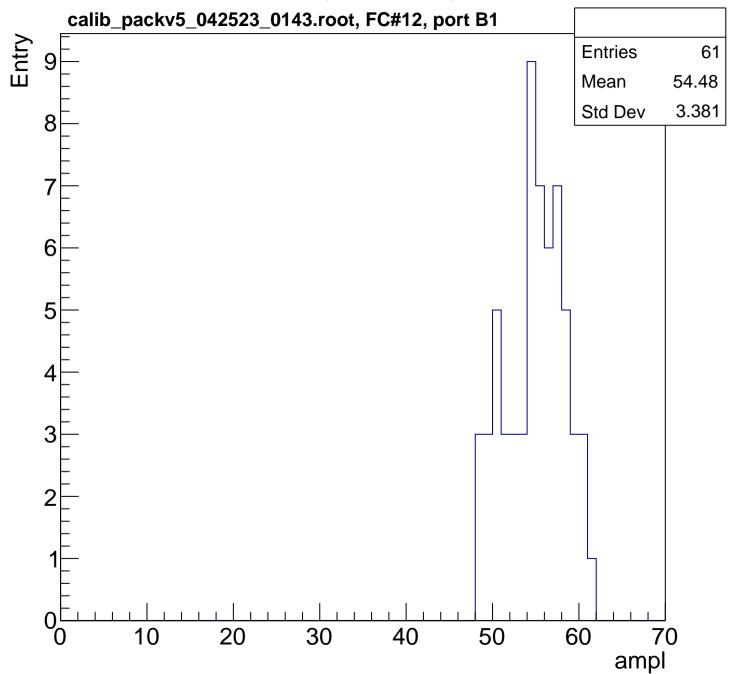


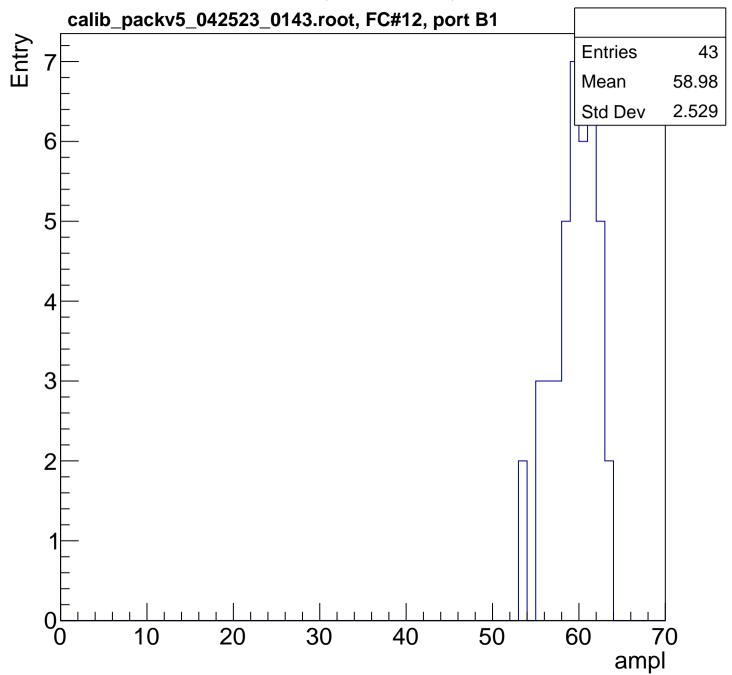


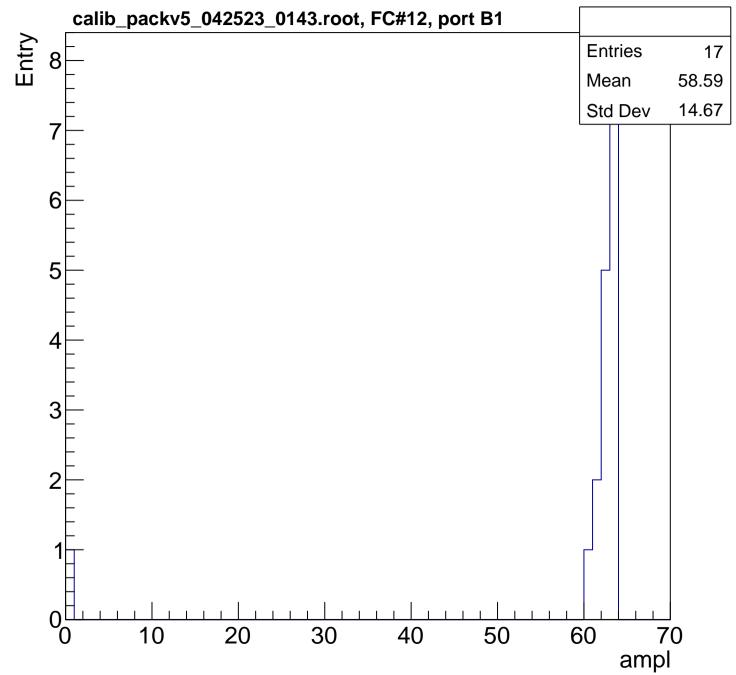


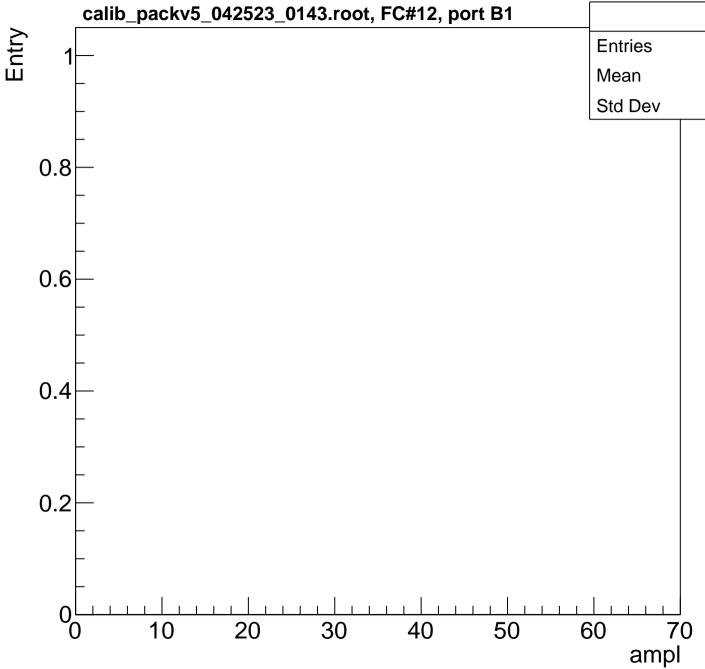


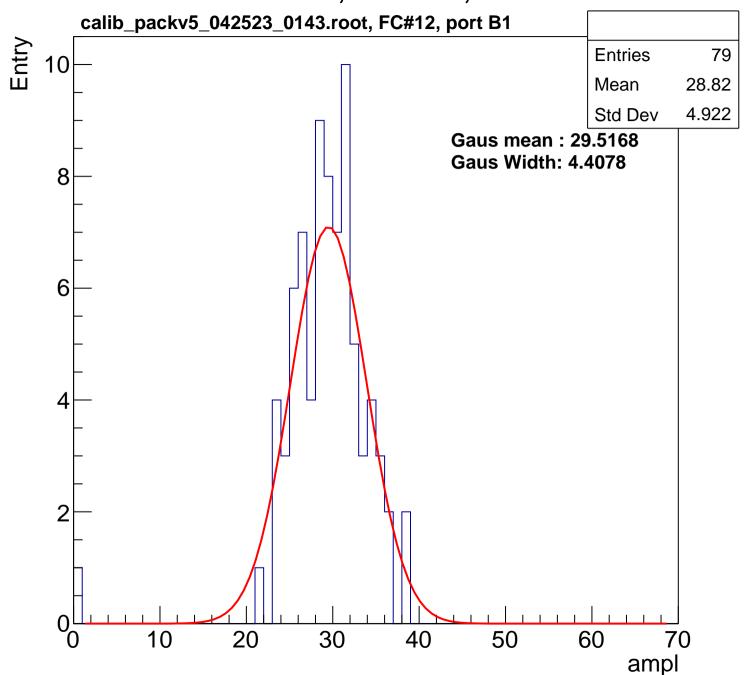


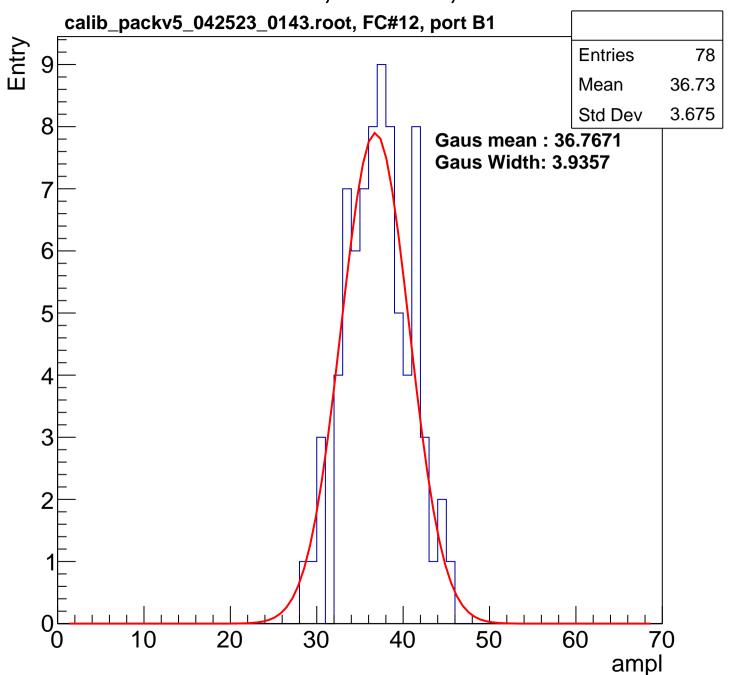


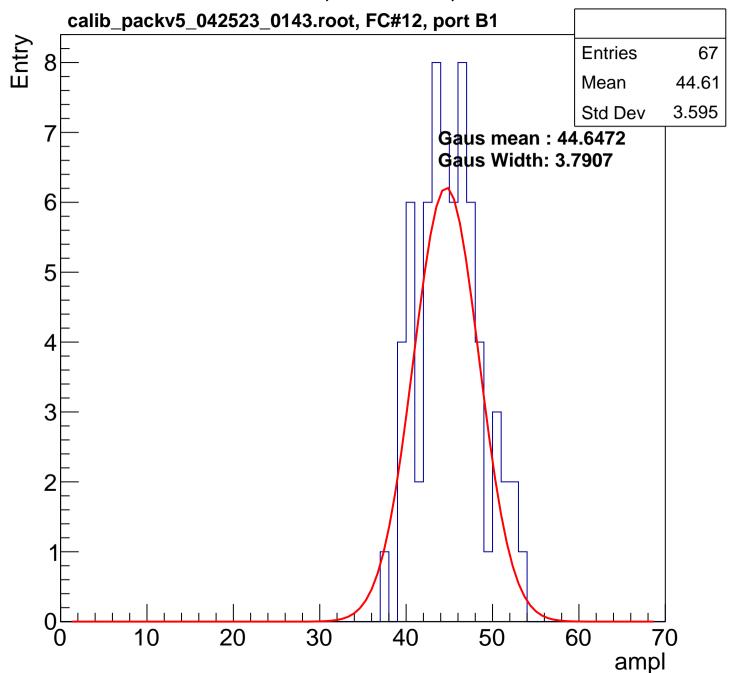


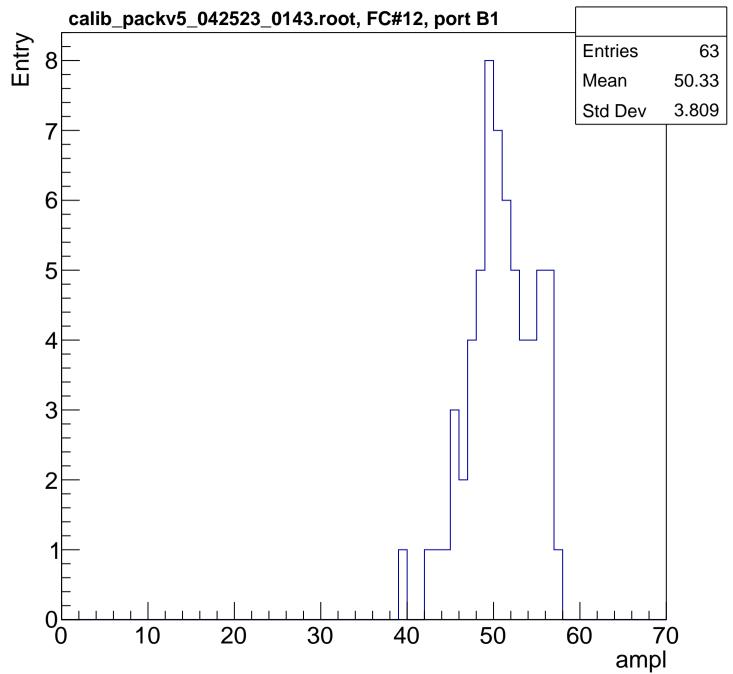


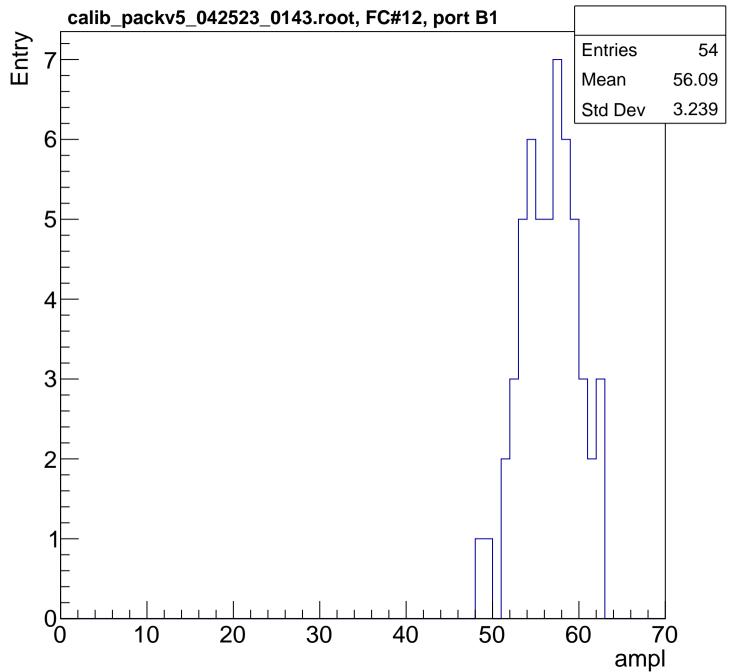


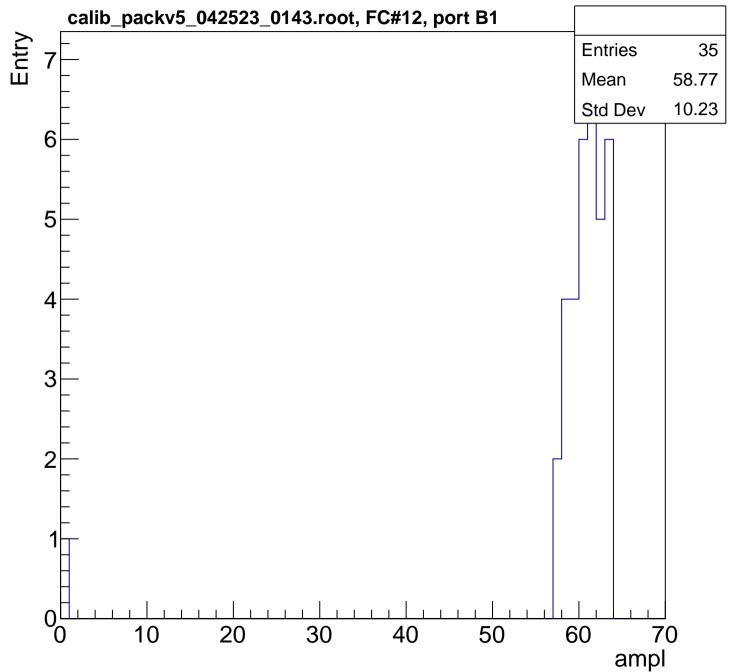


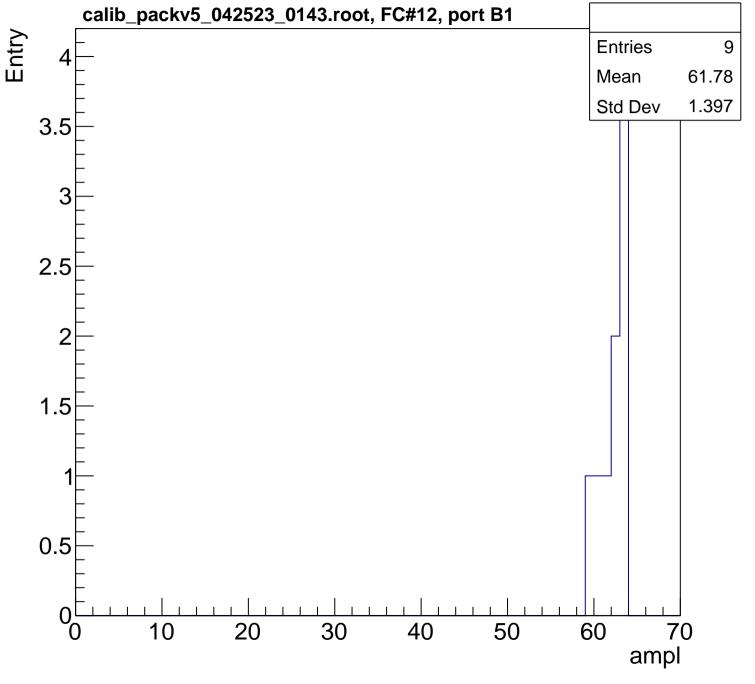


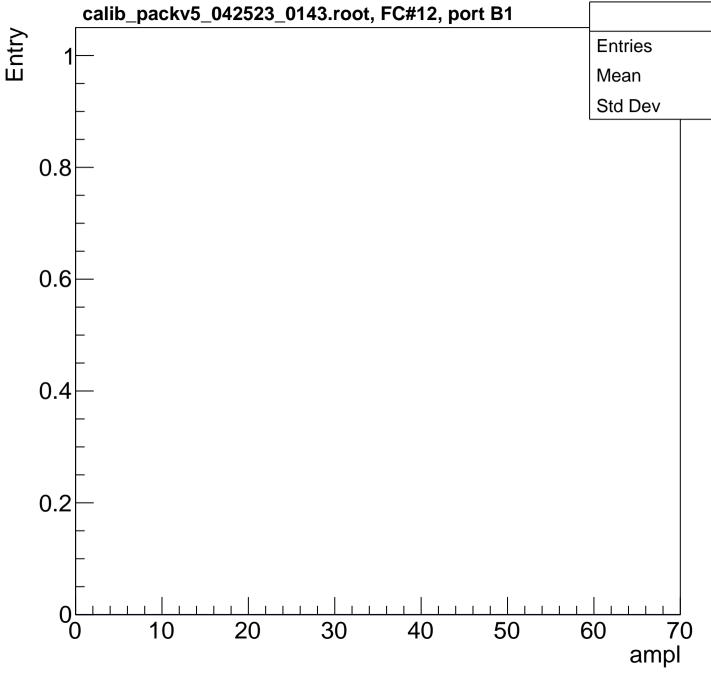


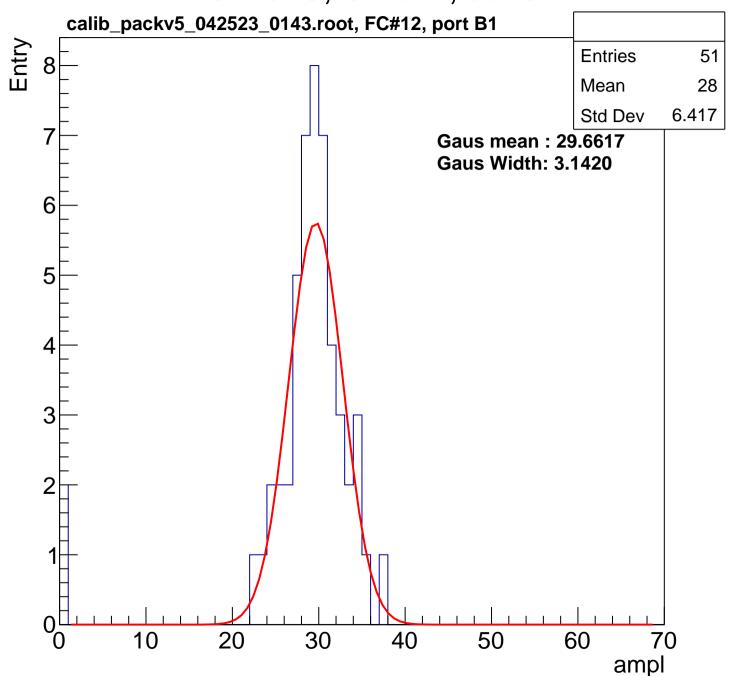


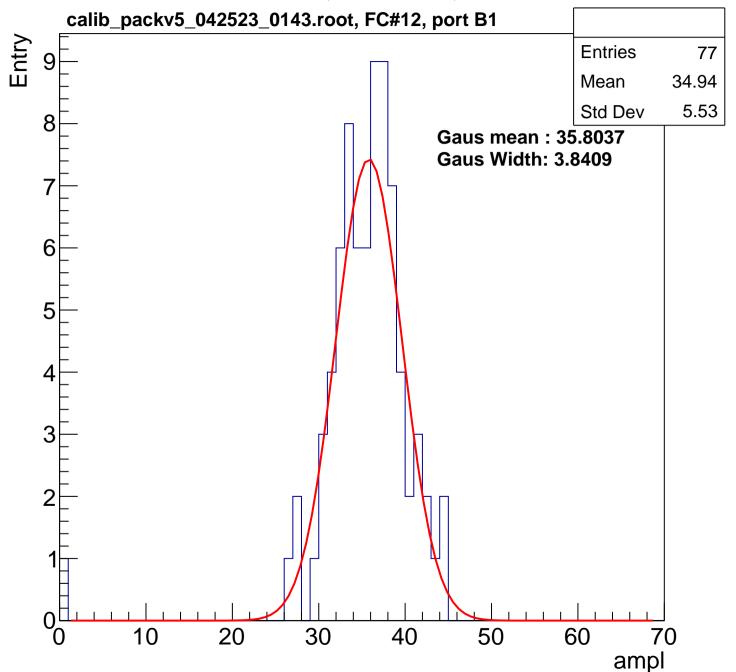


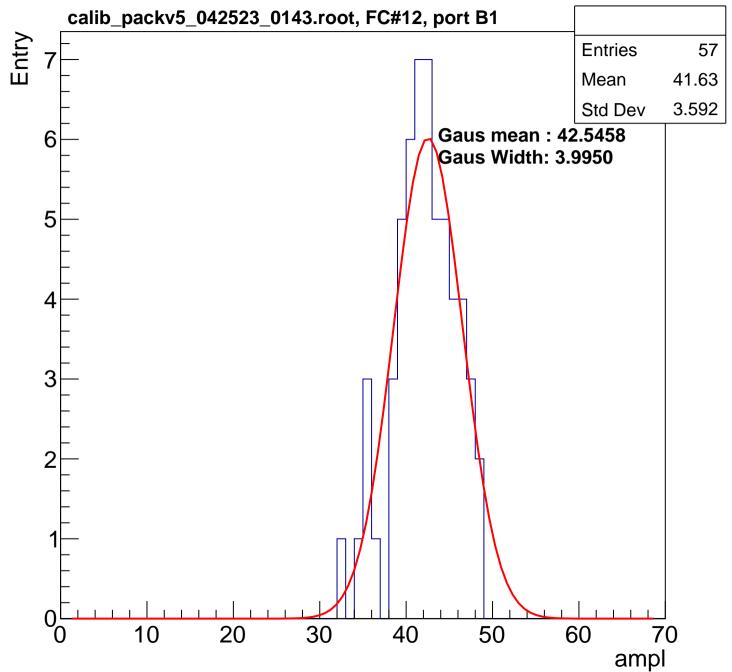


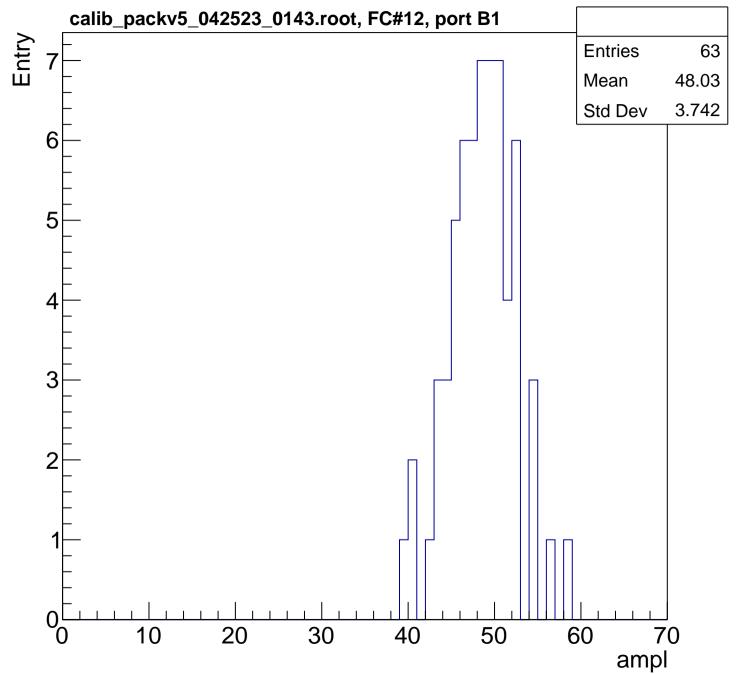


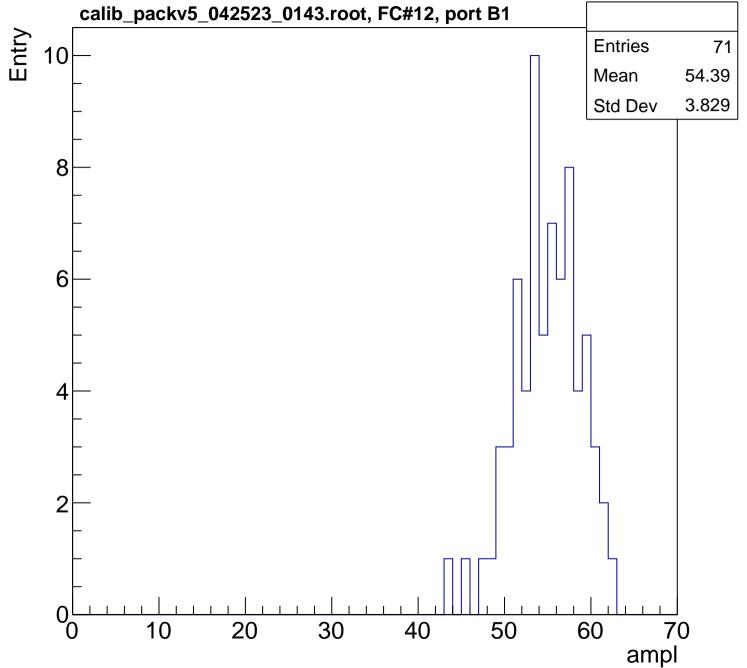


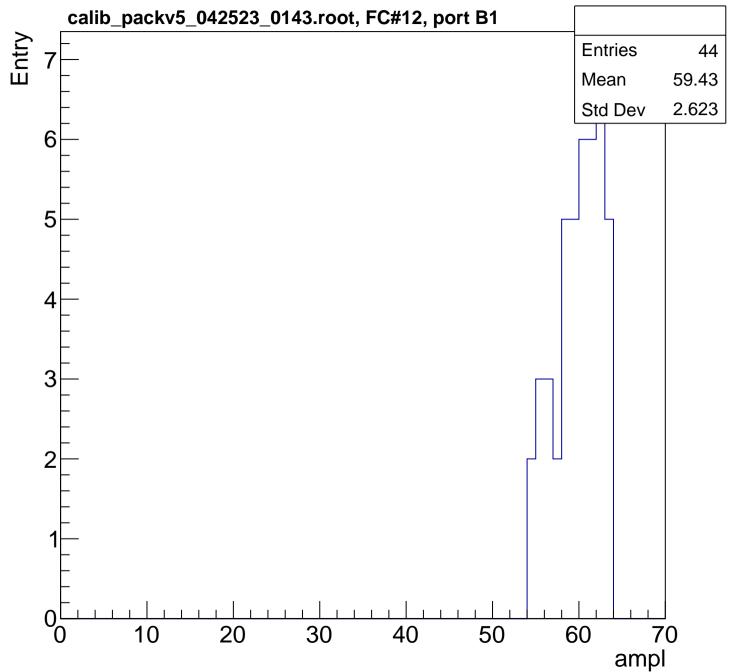


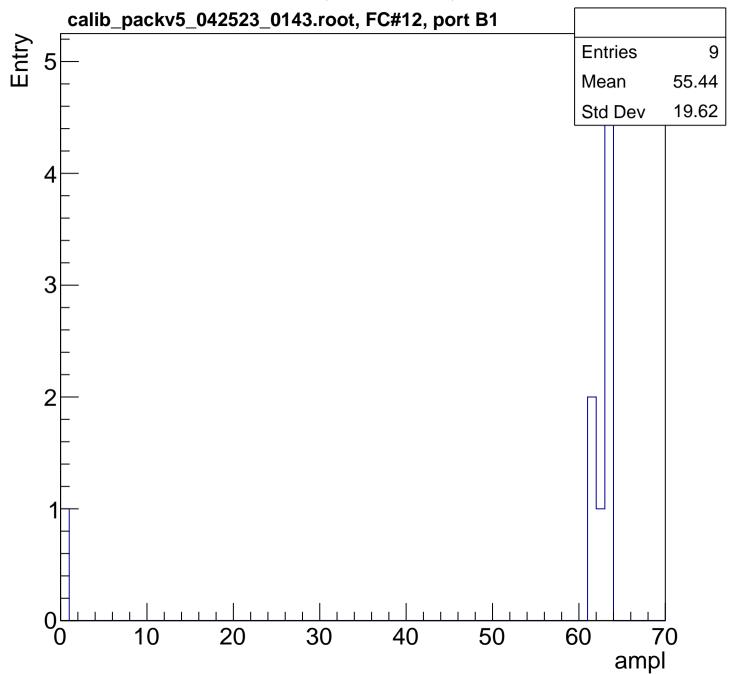


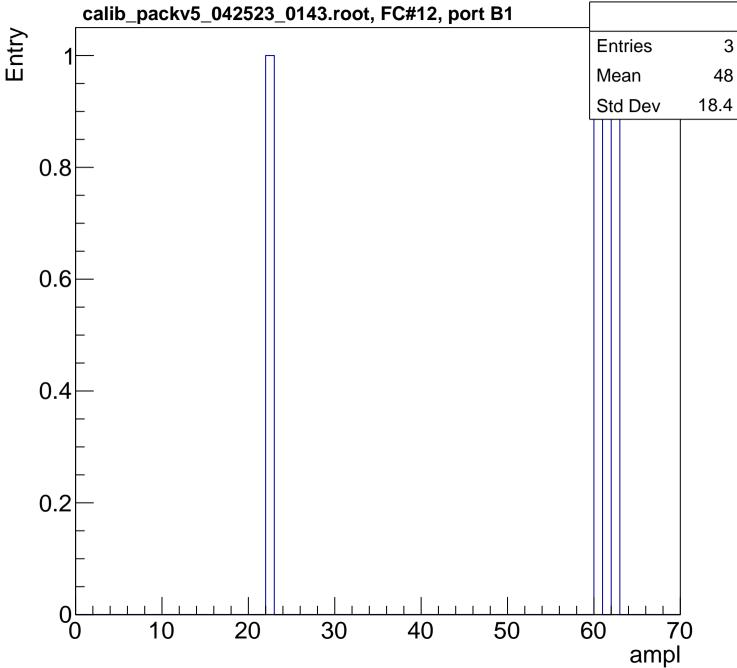


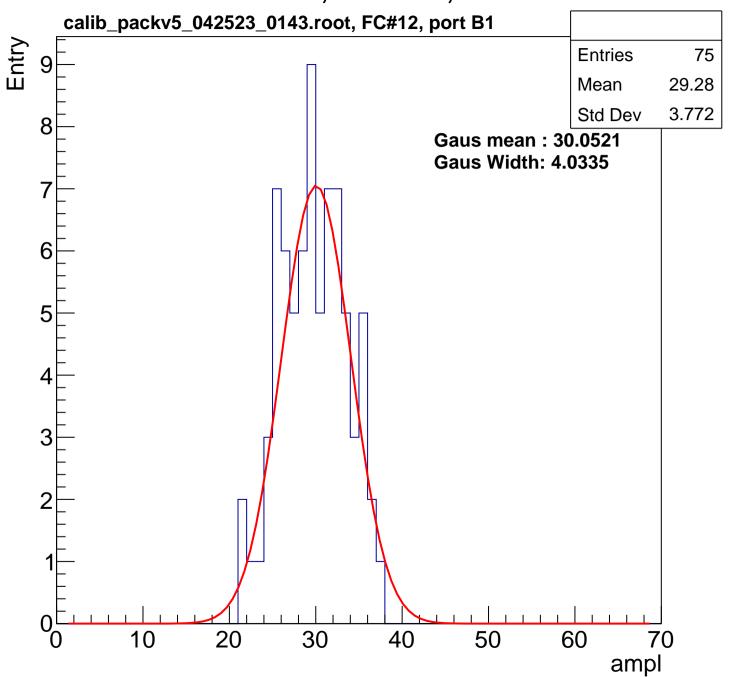


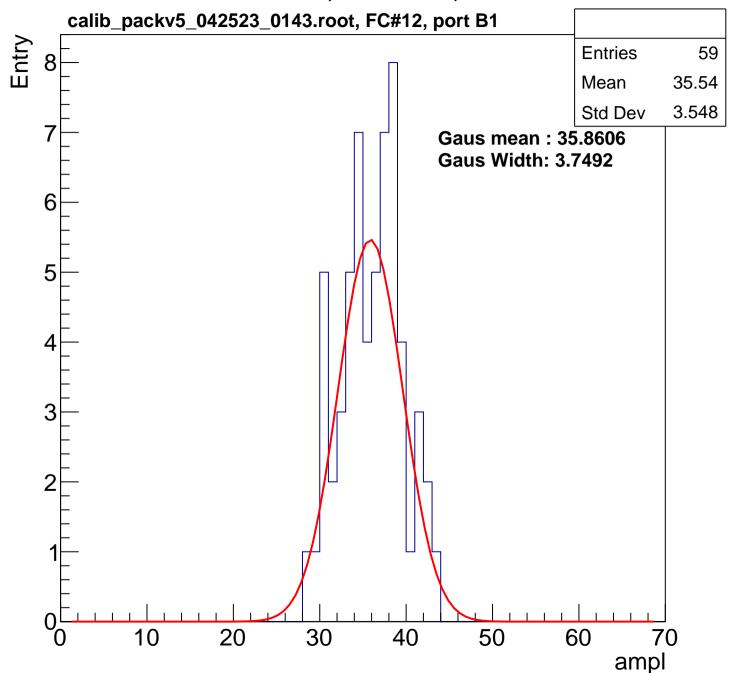


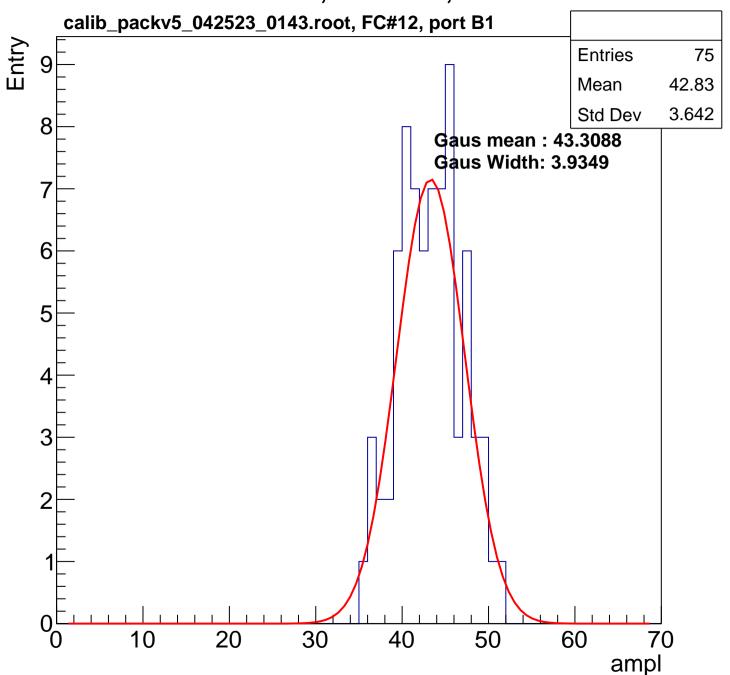


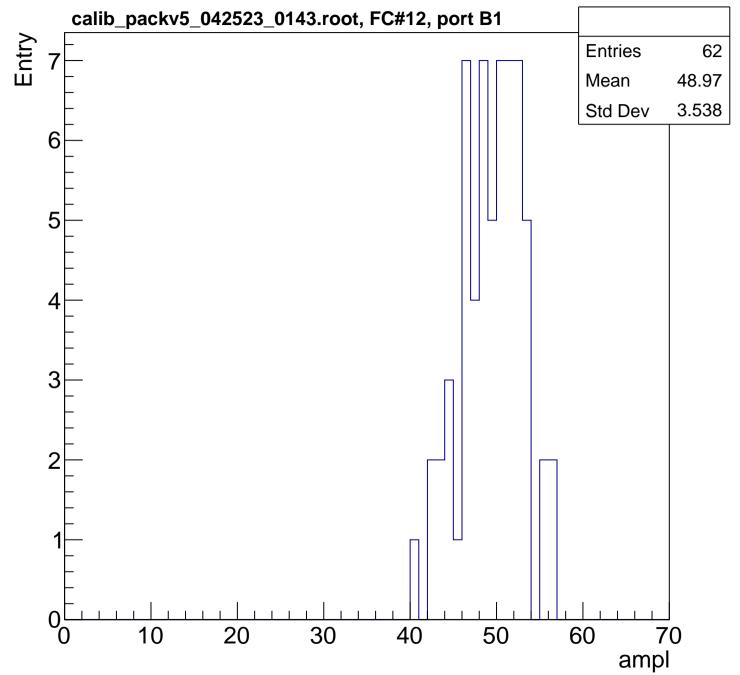


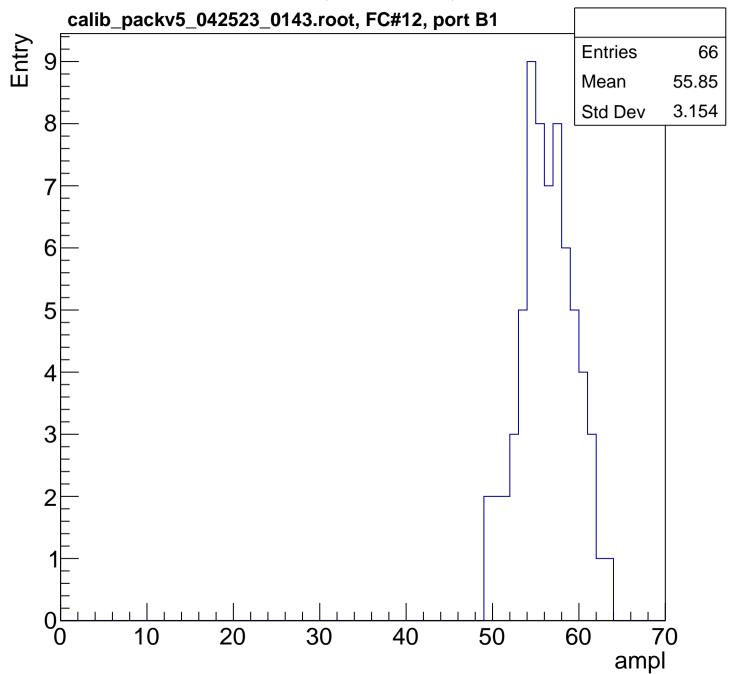


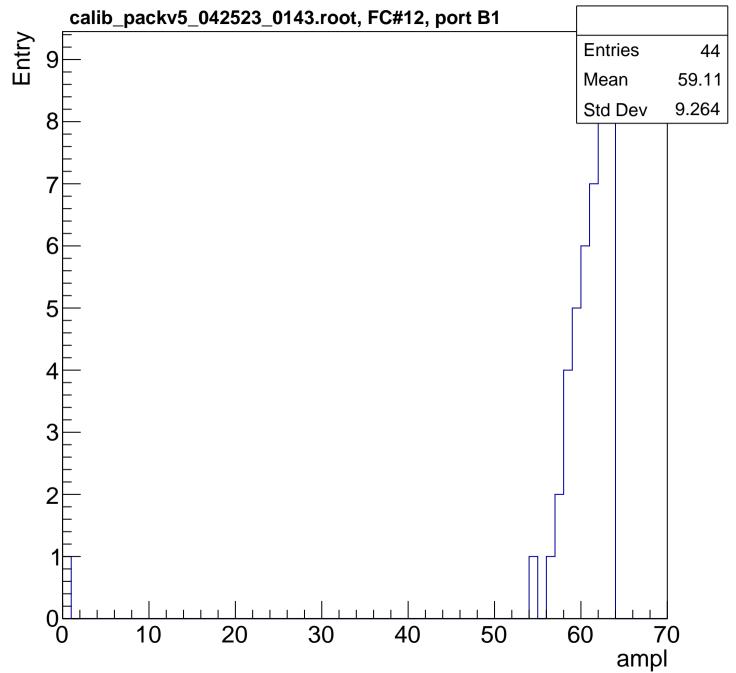


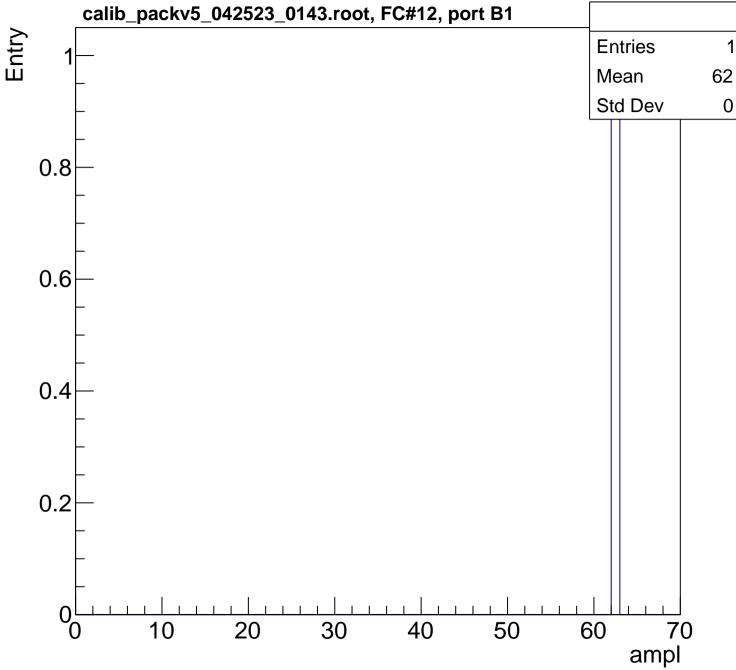


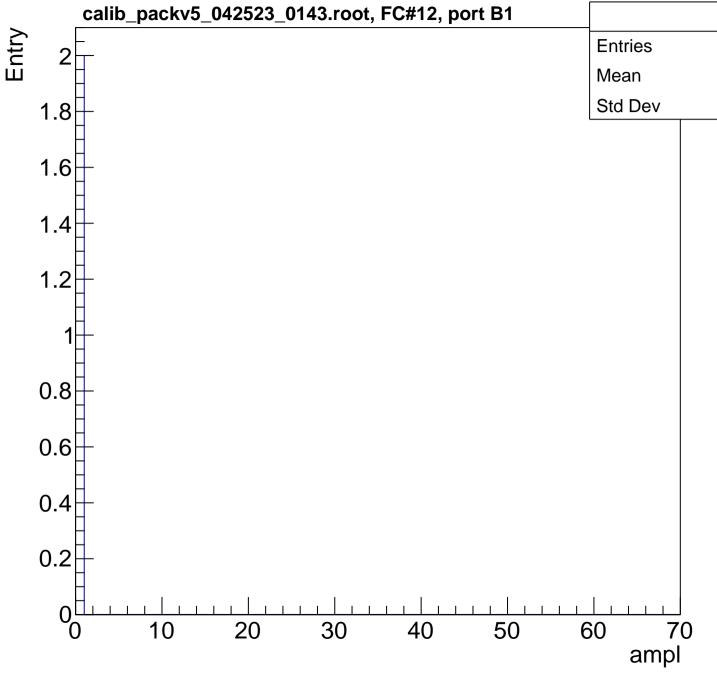


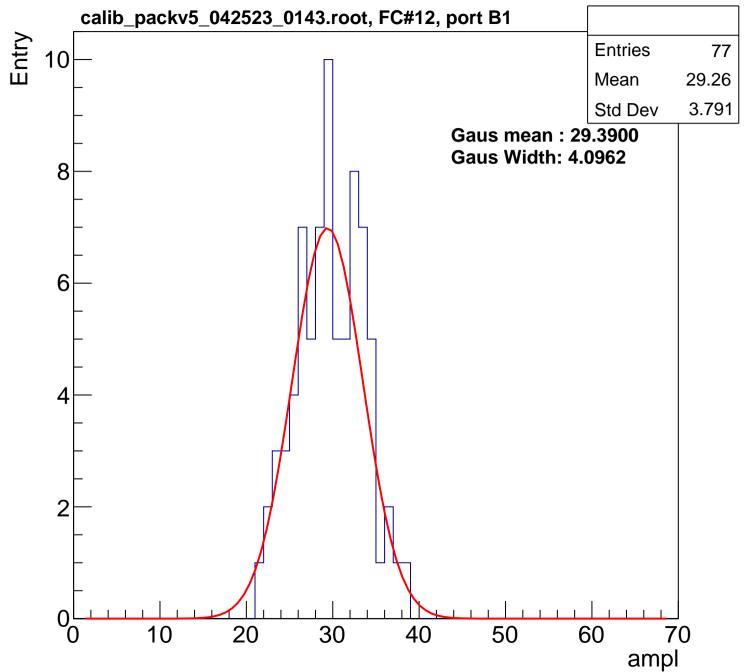


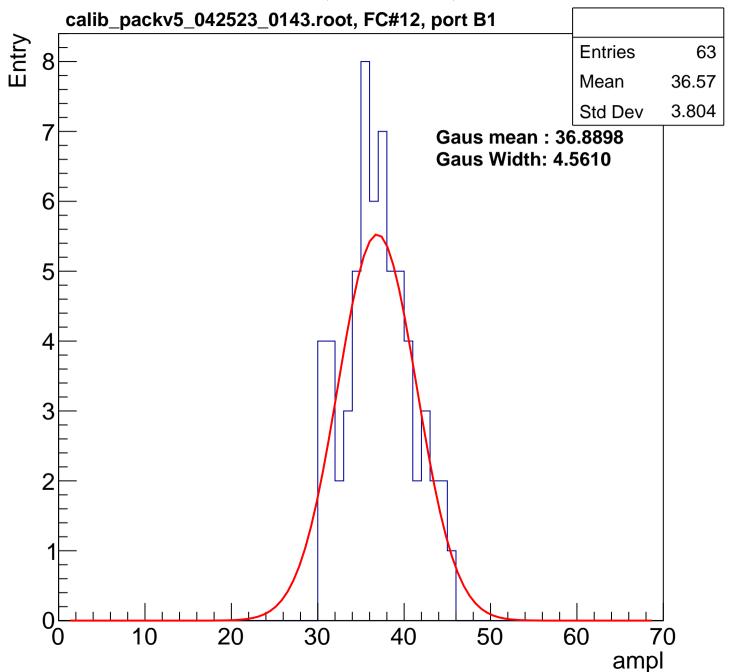


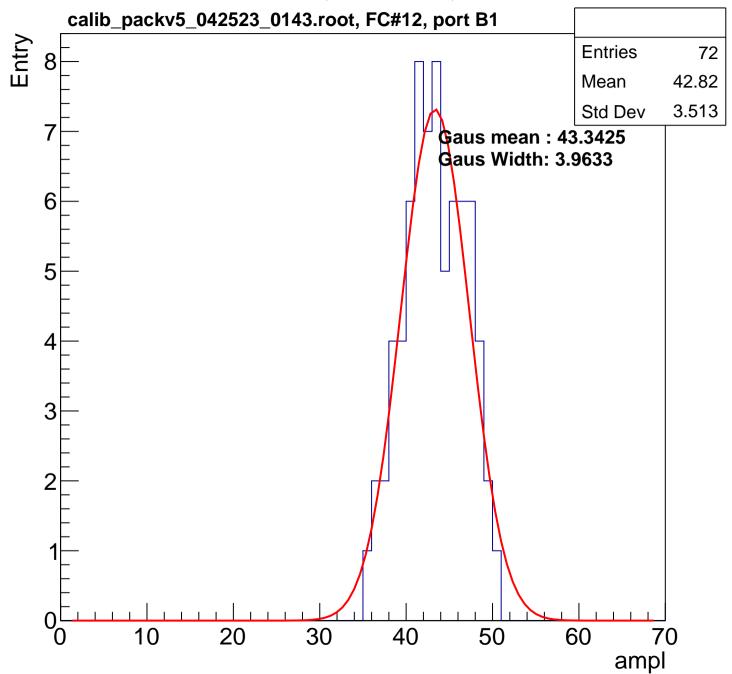


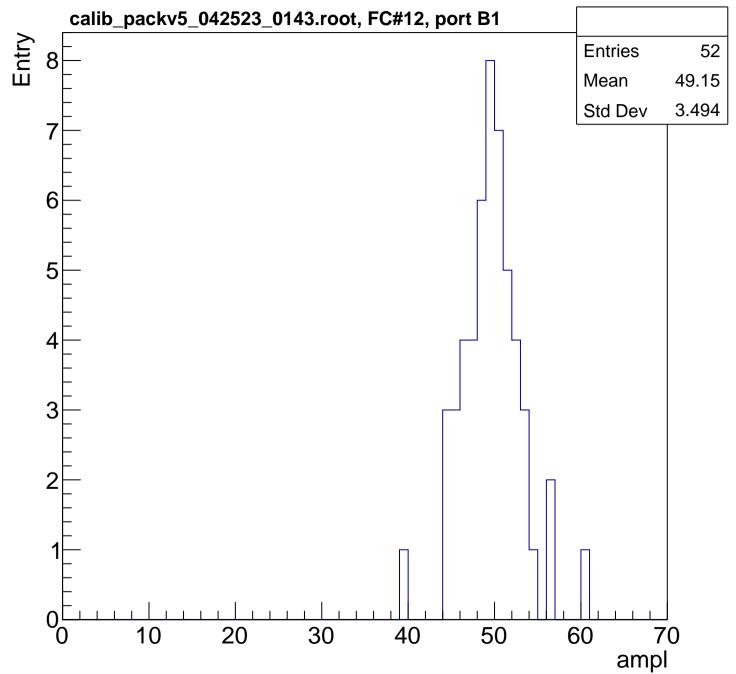


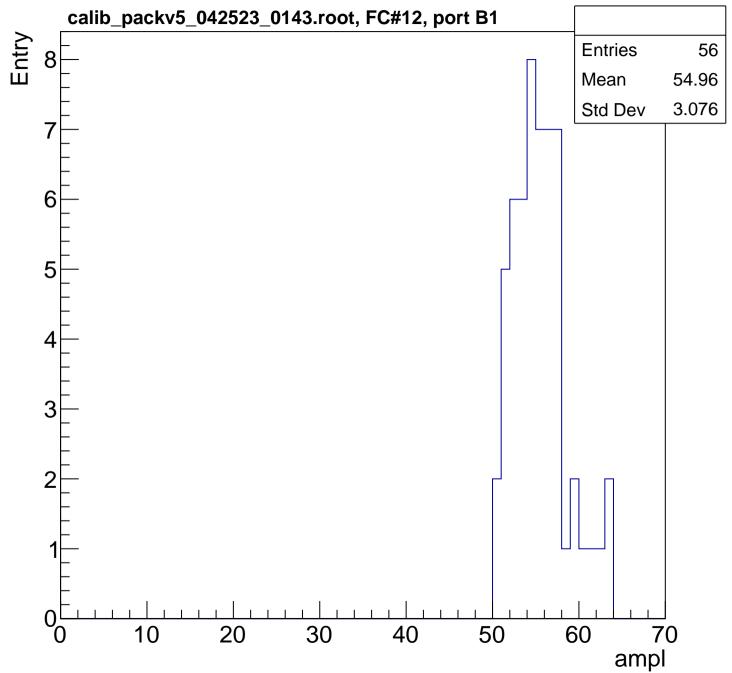


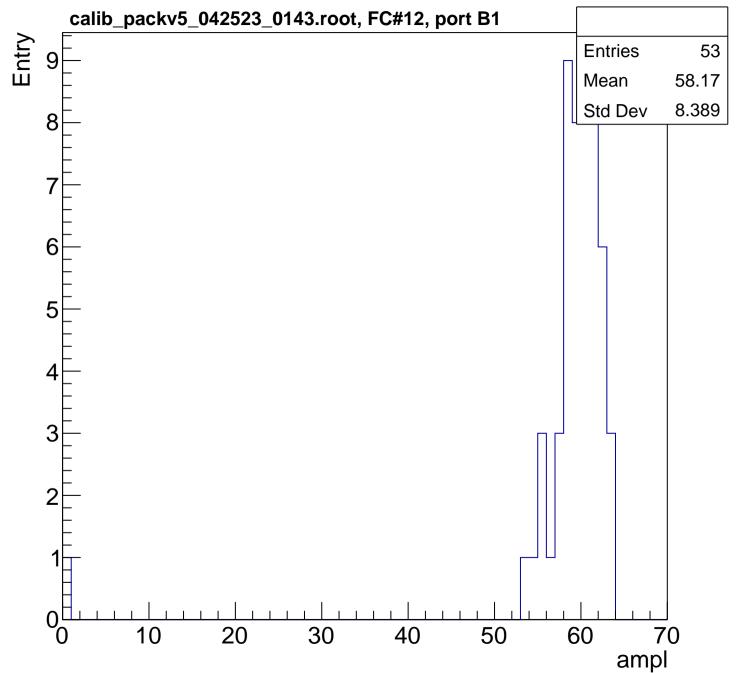


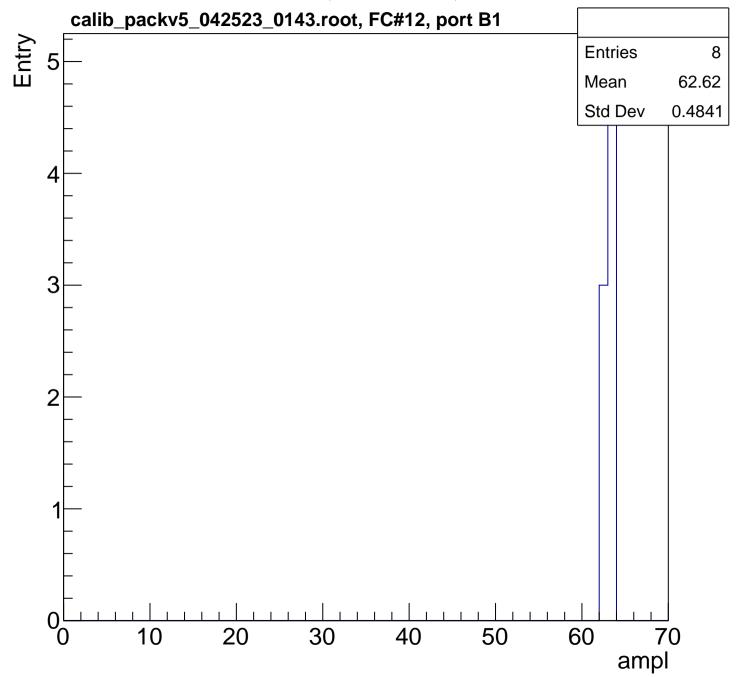




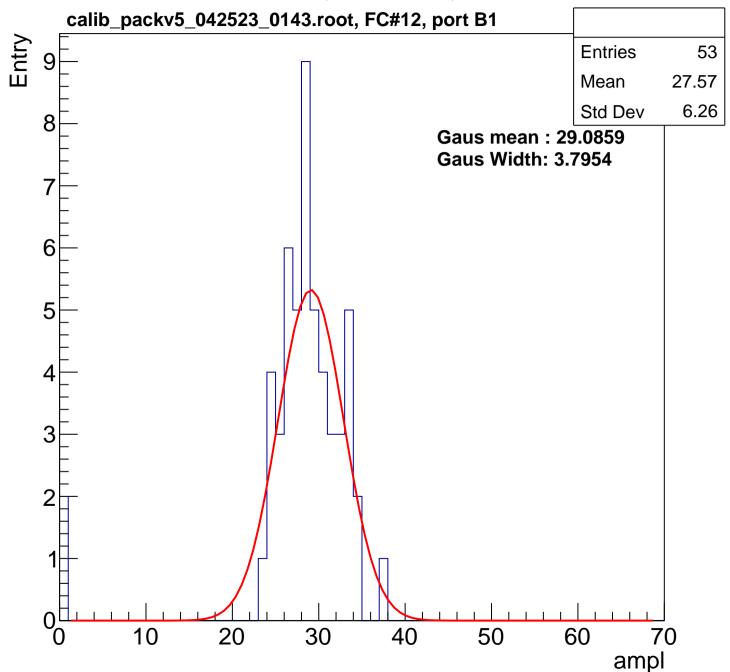


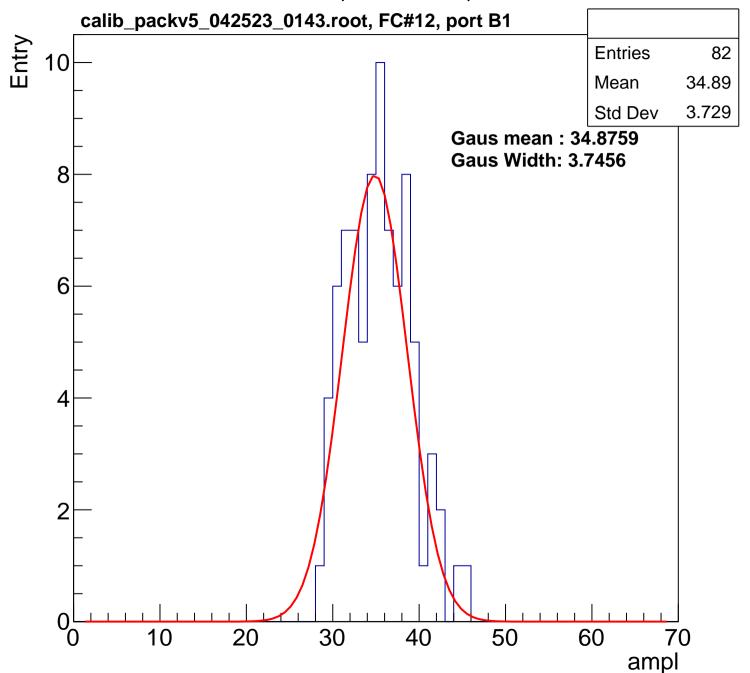


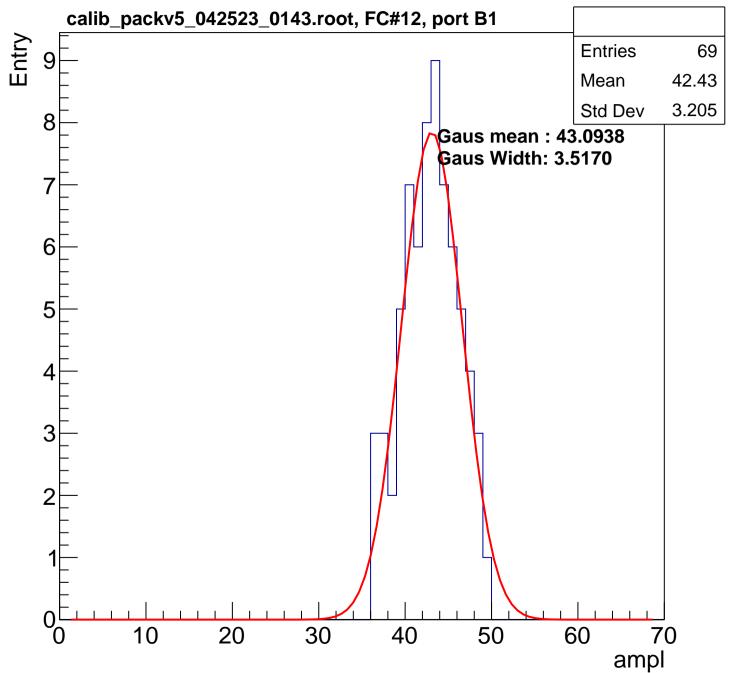


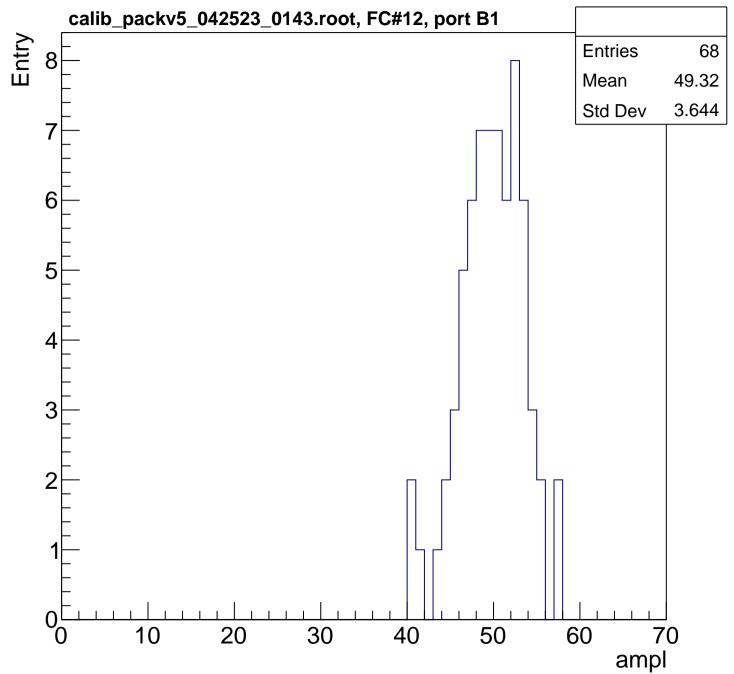


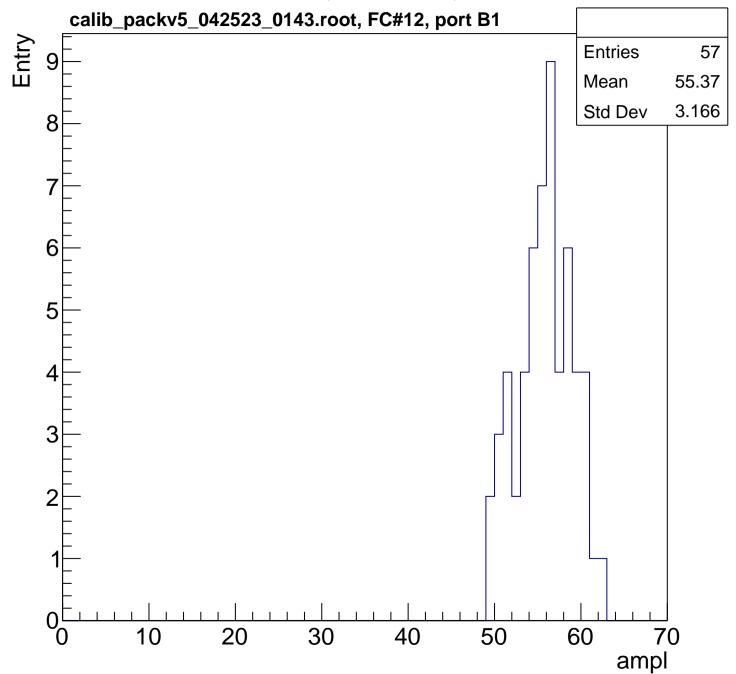
B0L102S, U4-ch6, adc7 calib_packv5_042523_0143.root, FC#12, port B1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

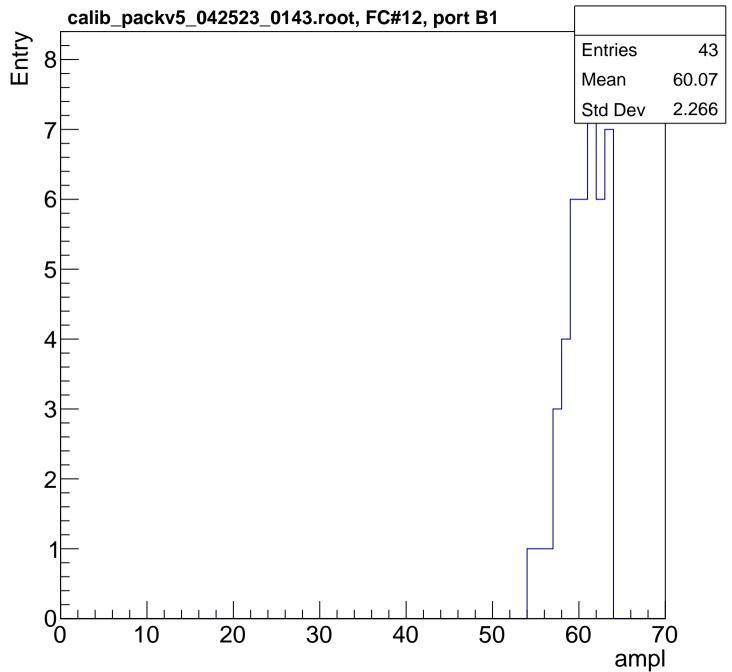


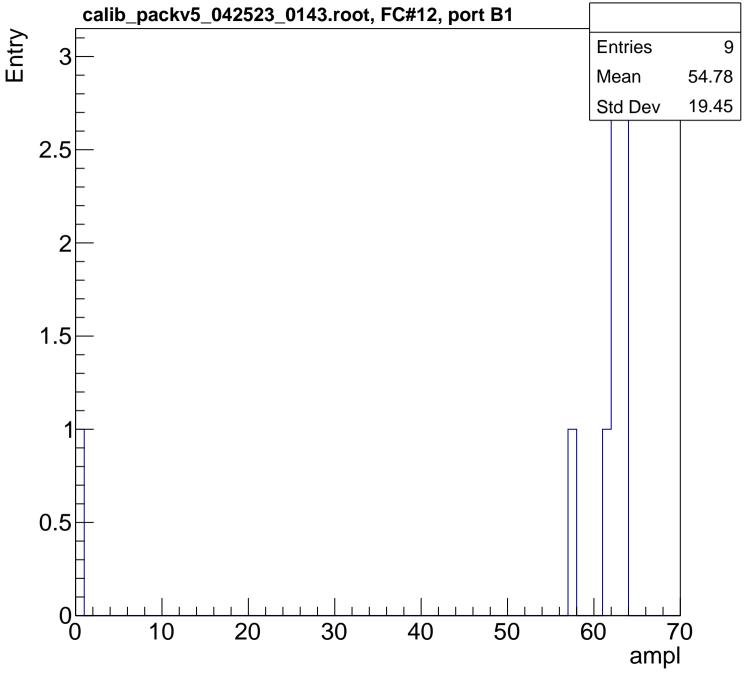




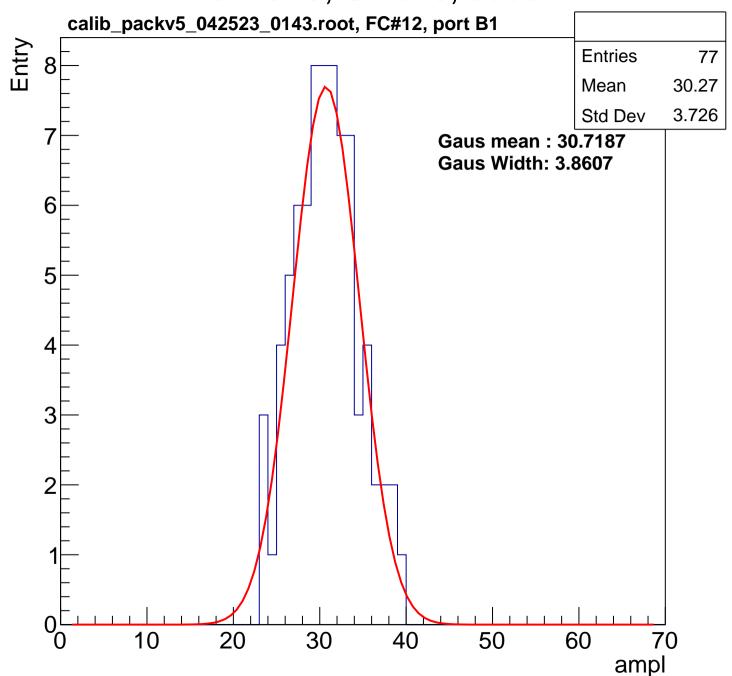


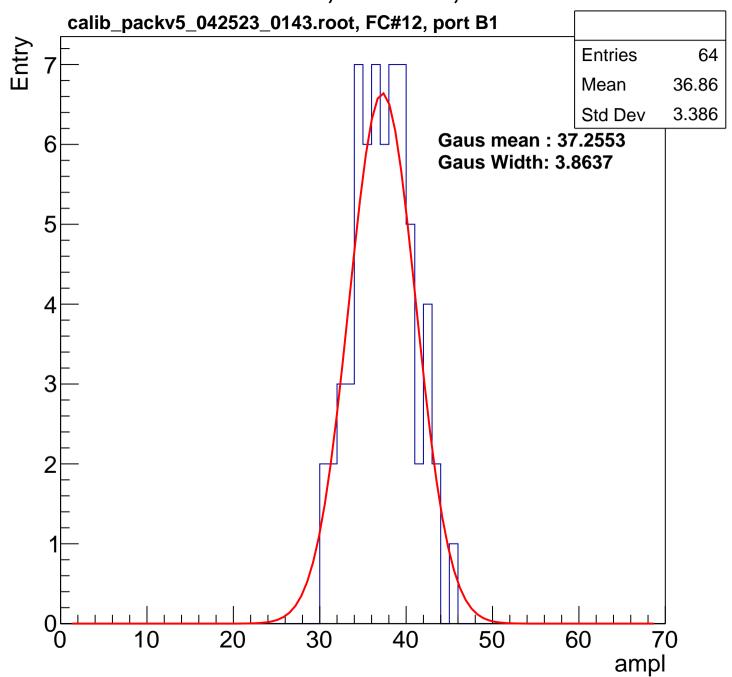


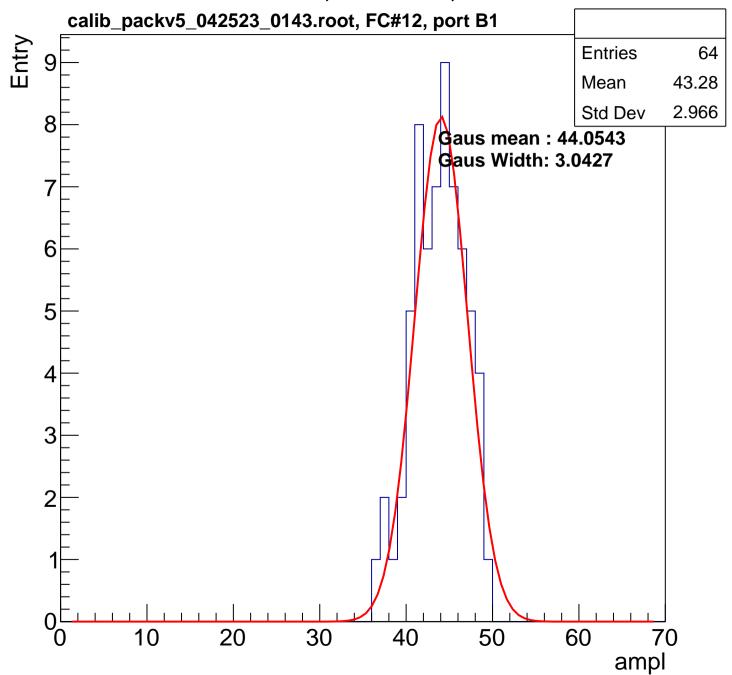


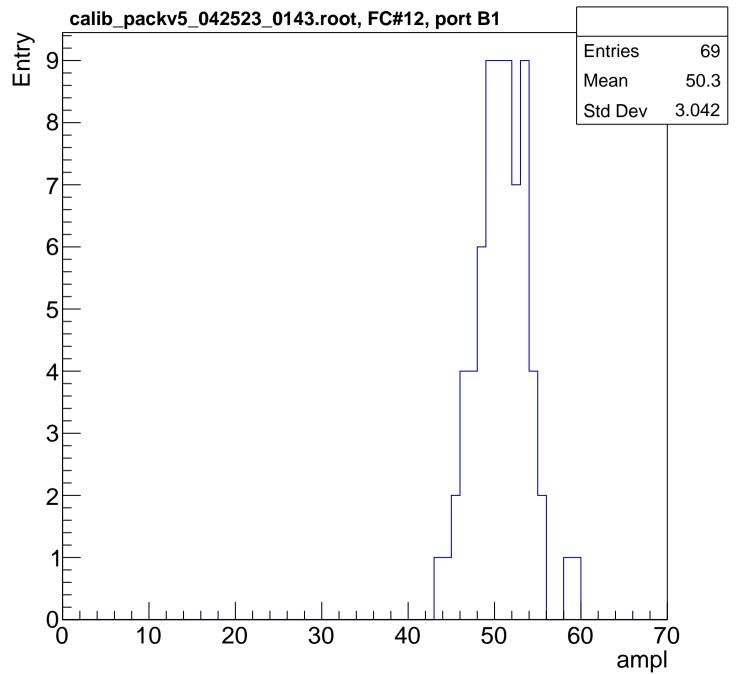


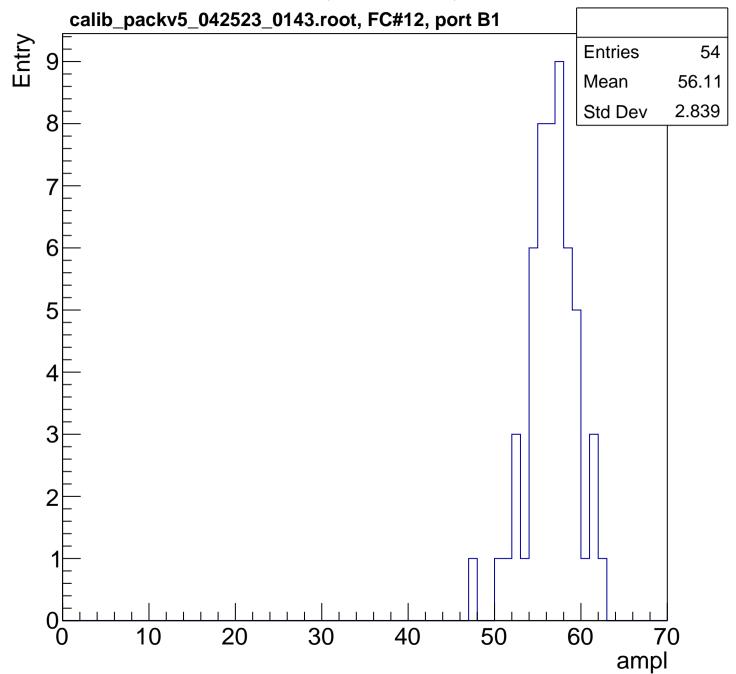


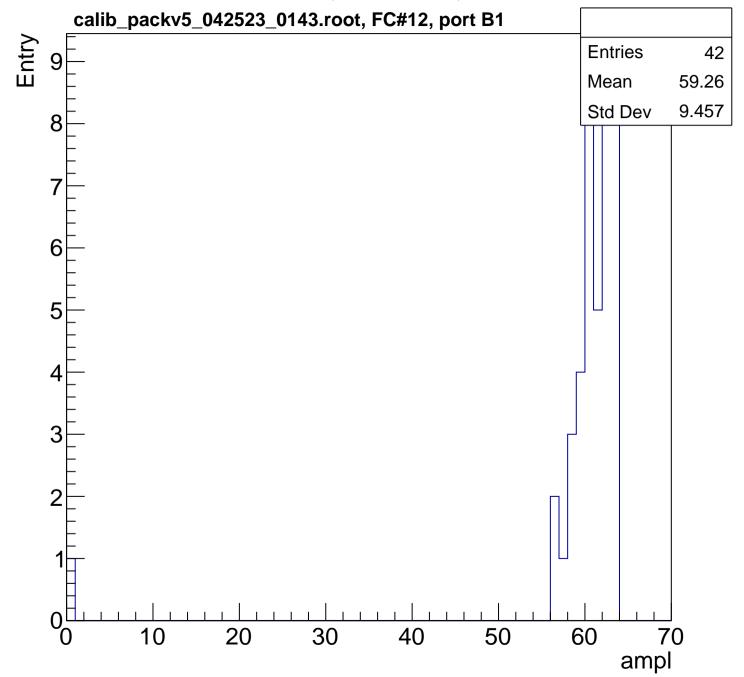


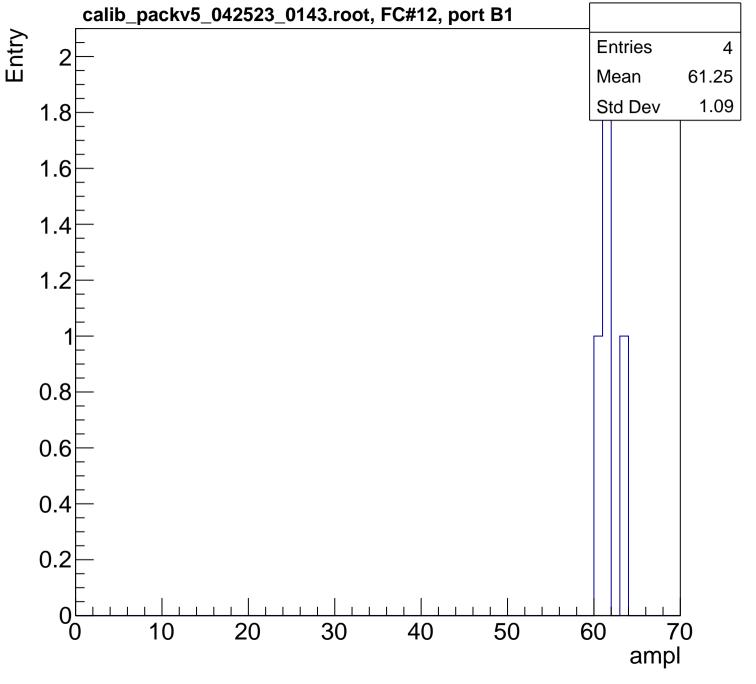


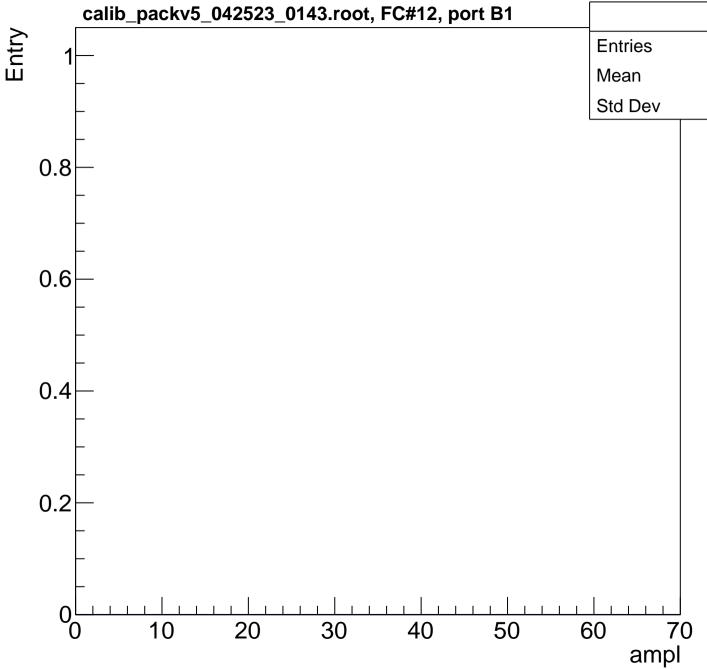


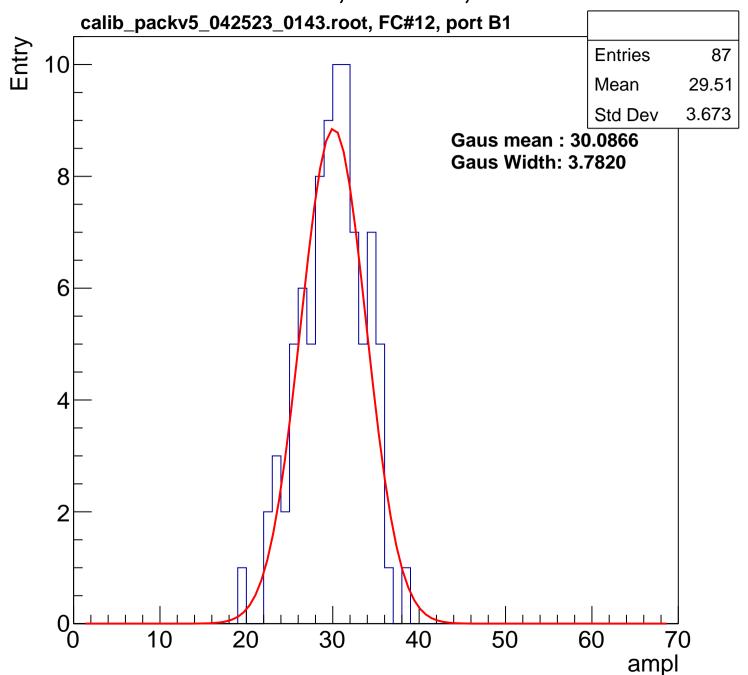


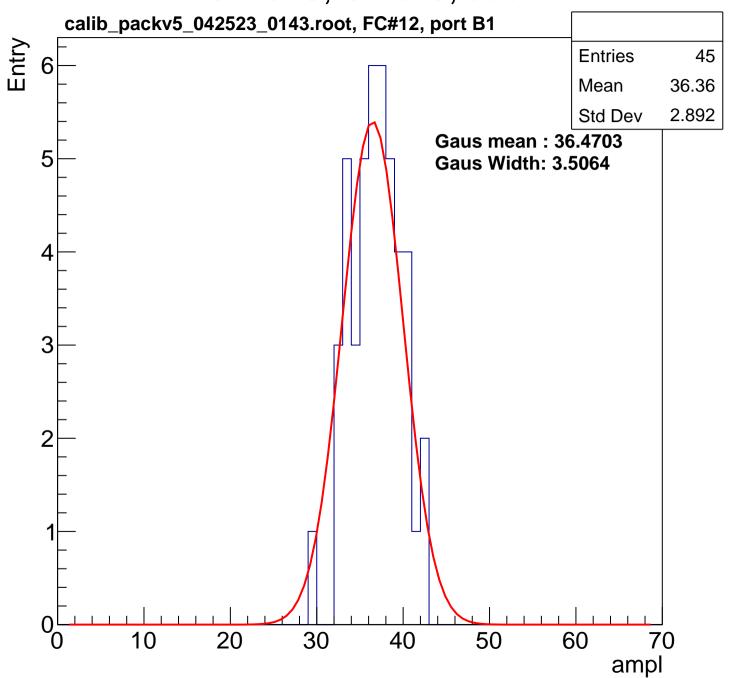


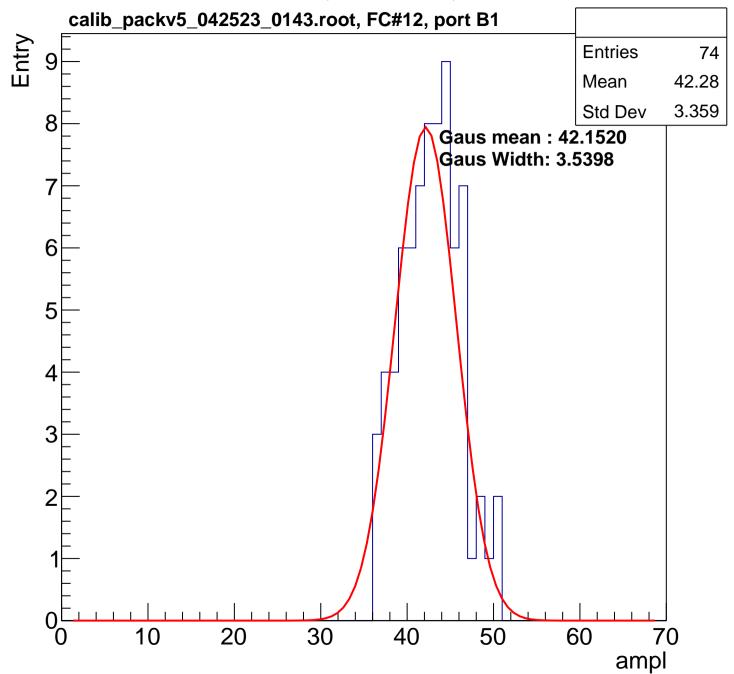


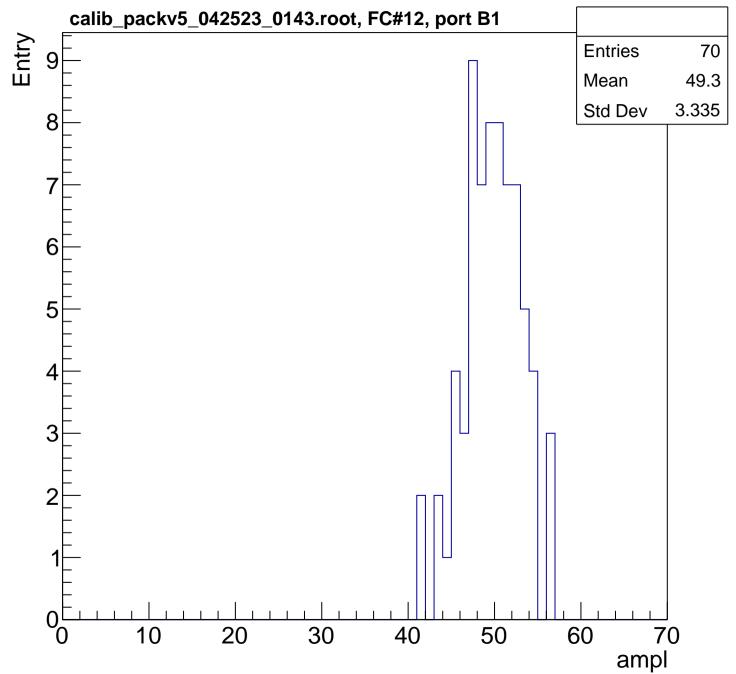


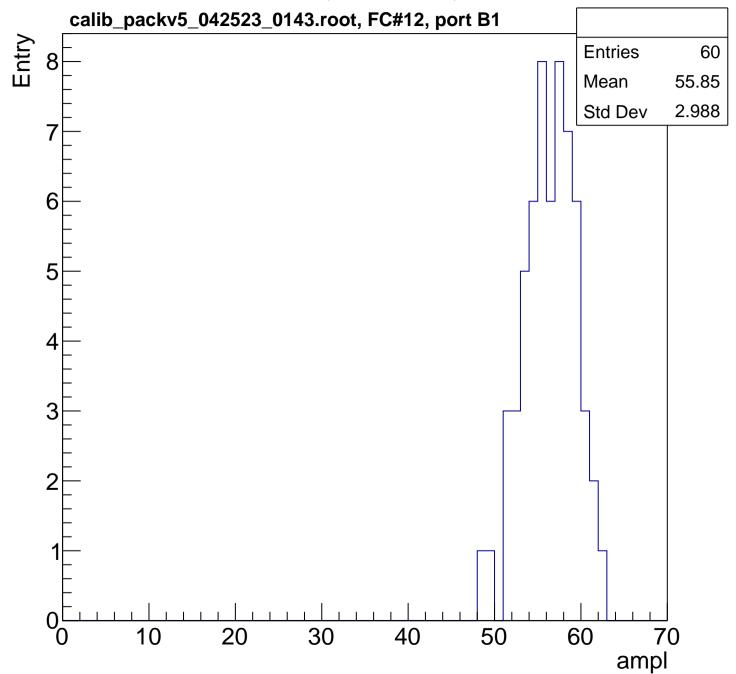


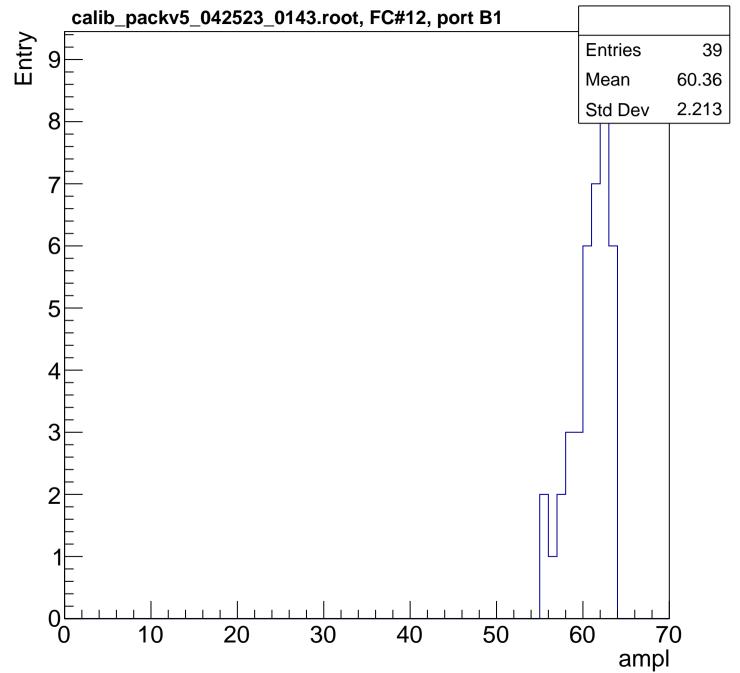


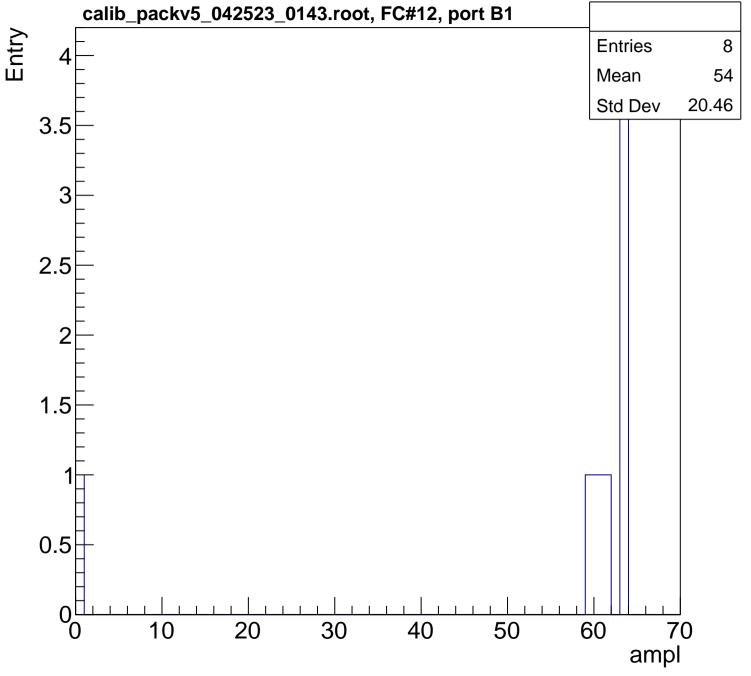




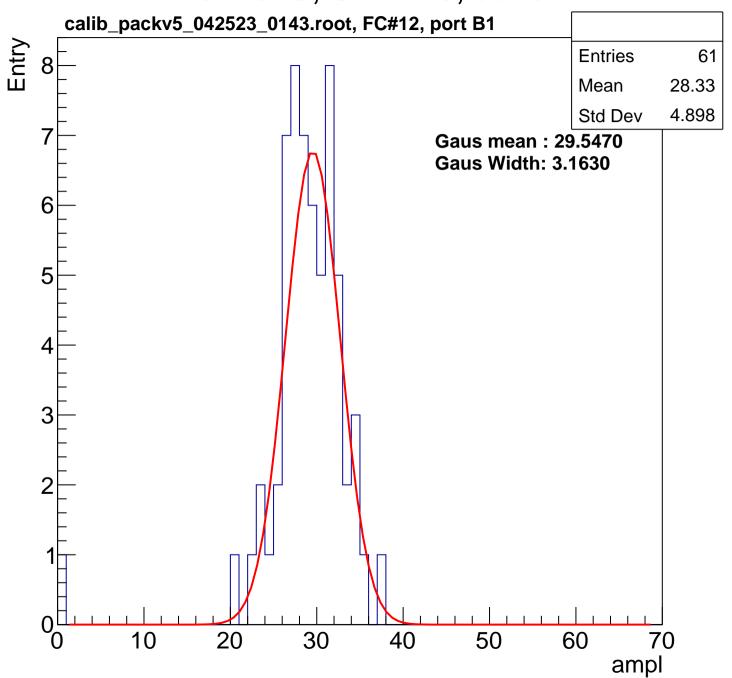


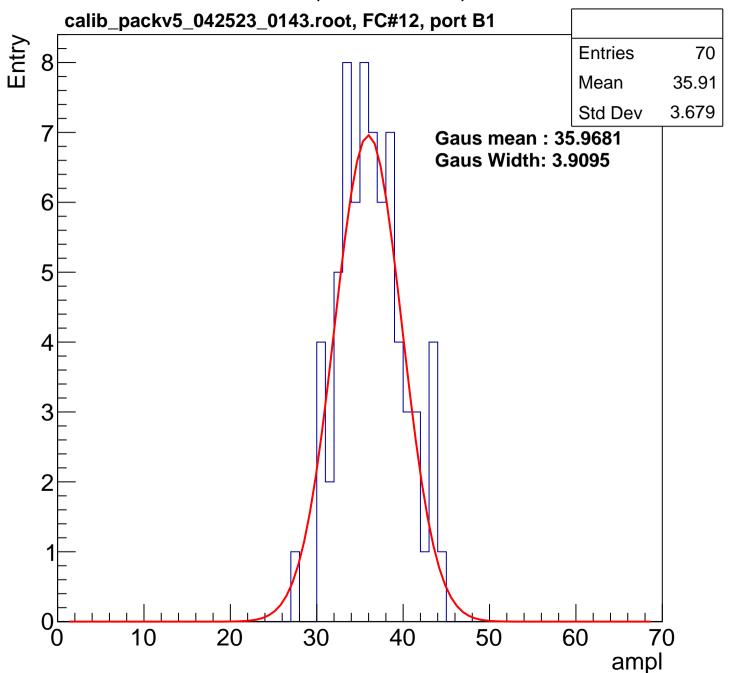


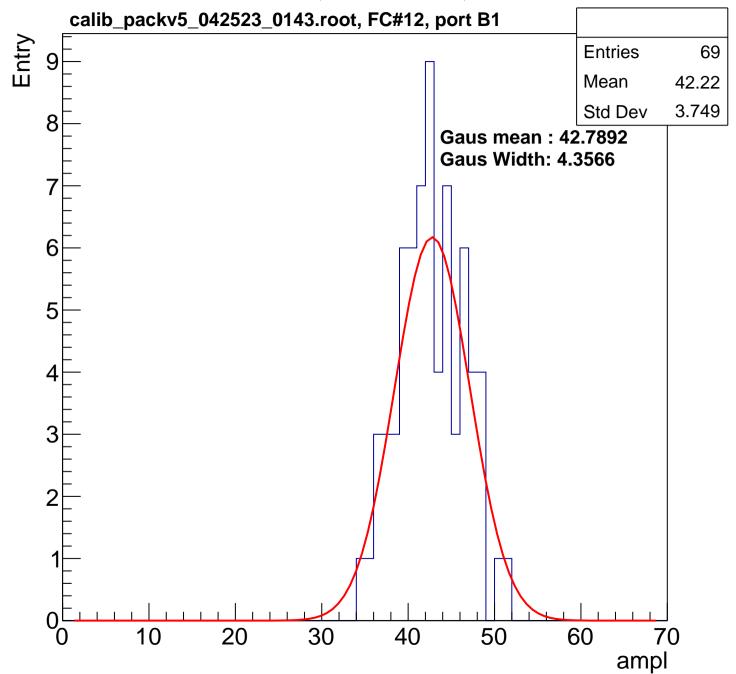


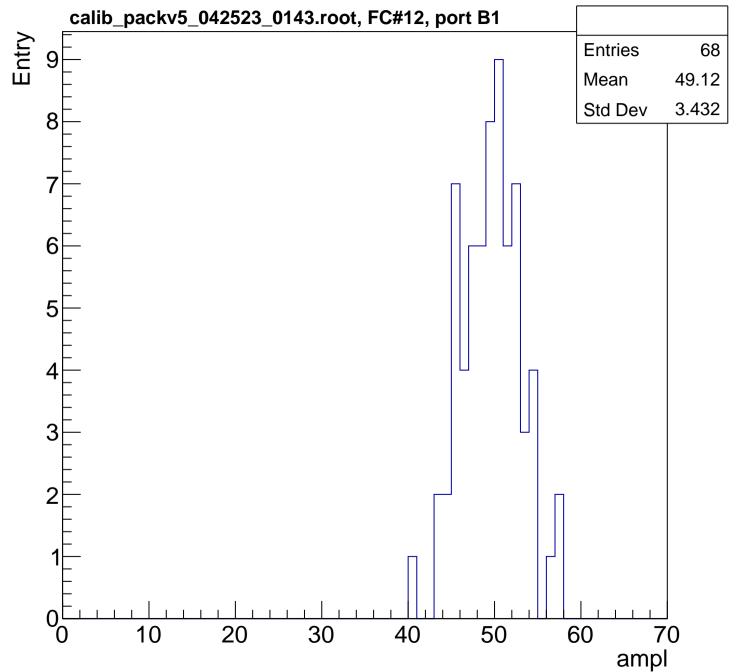


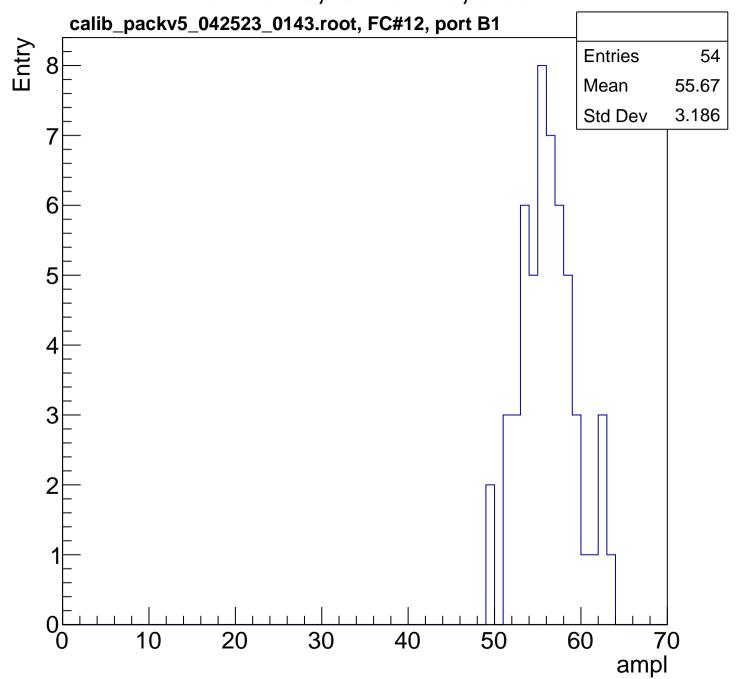


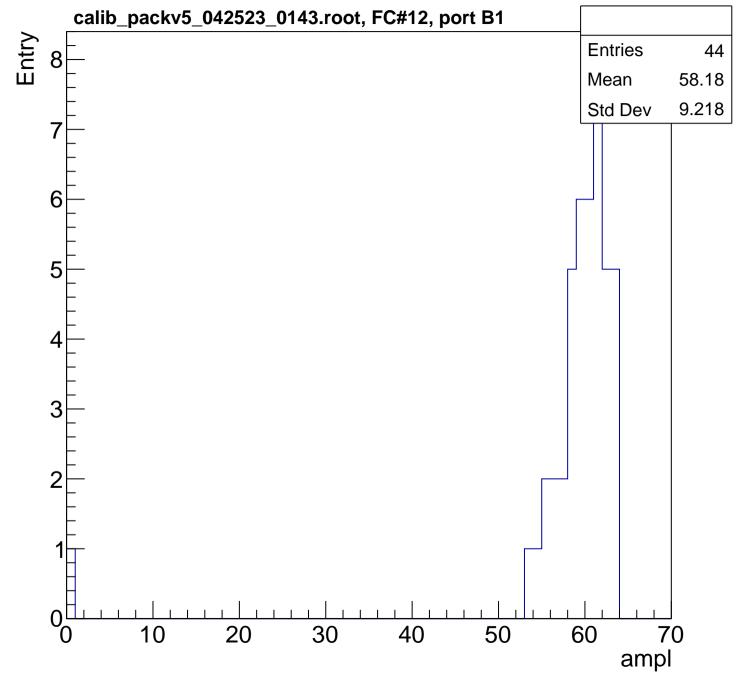


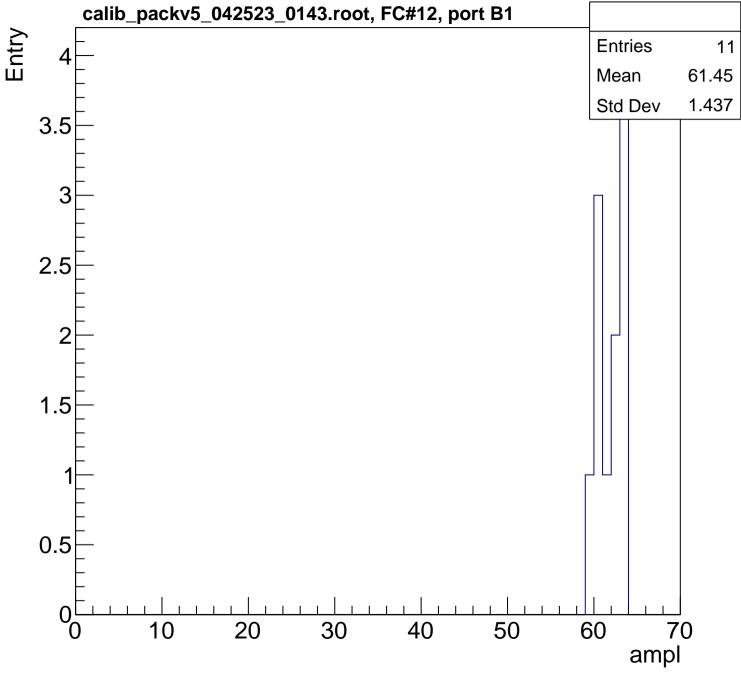


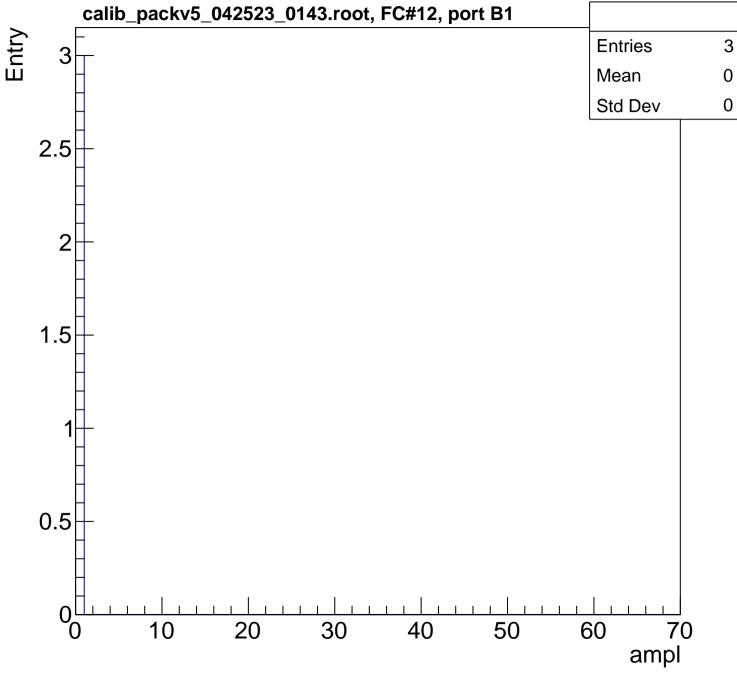


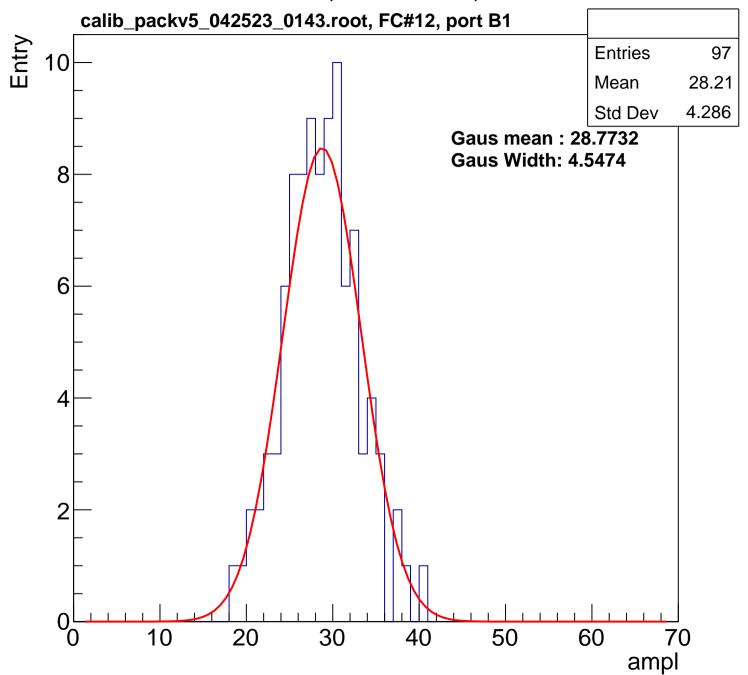


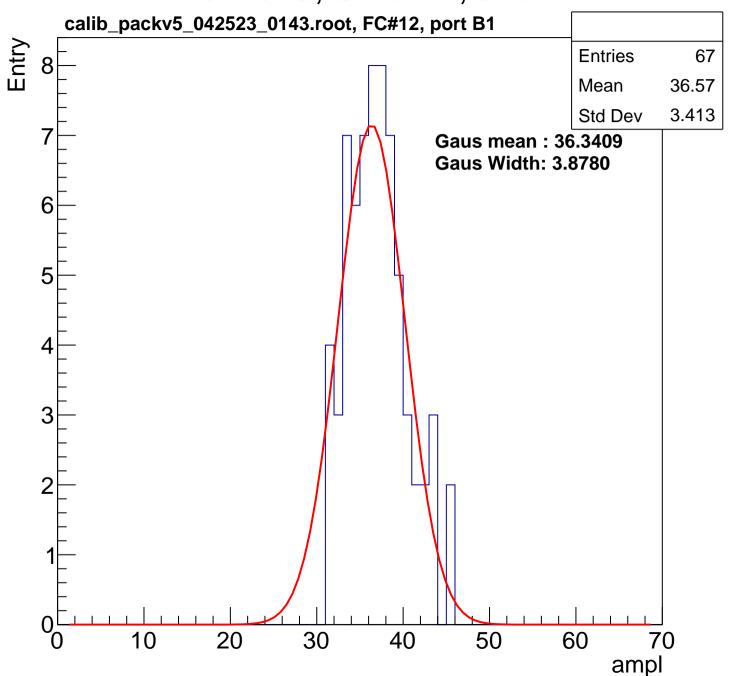


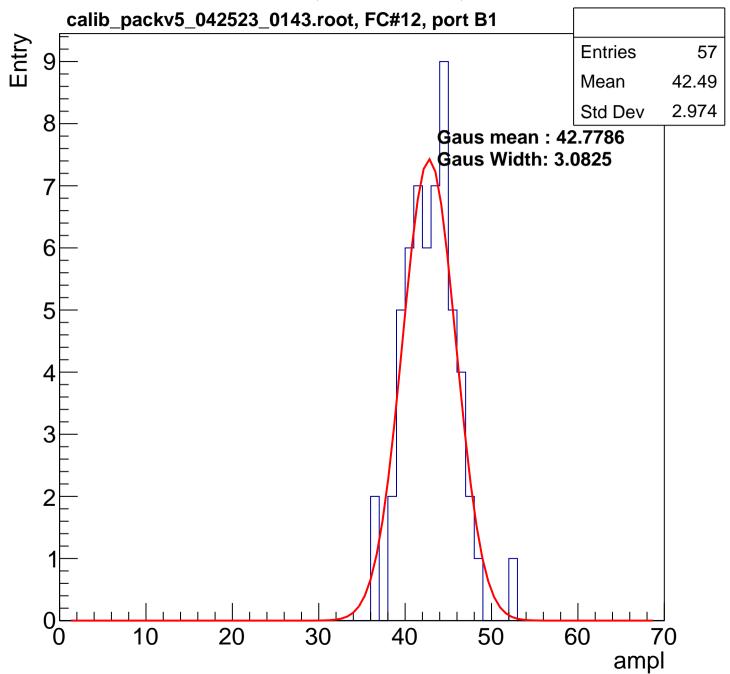


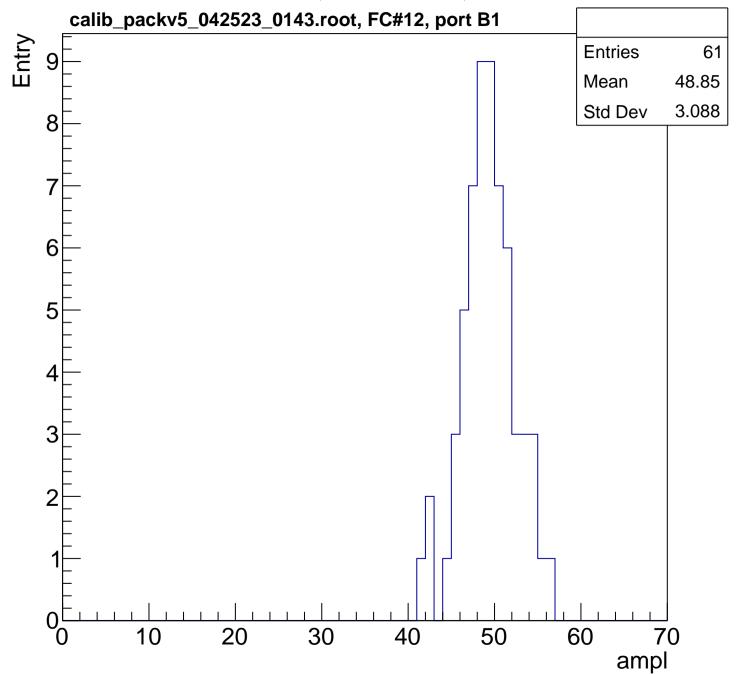


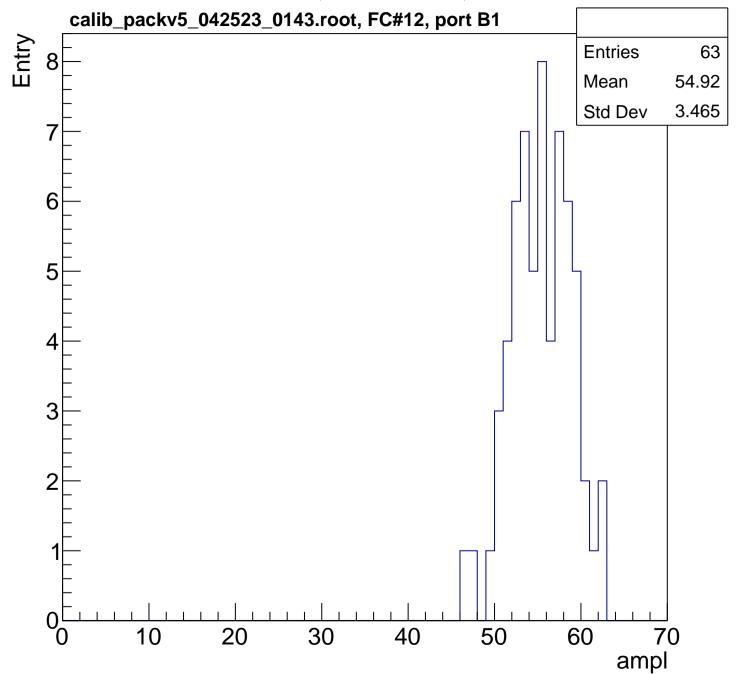


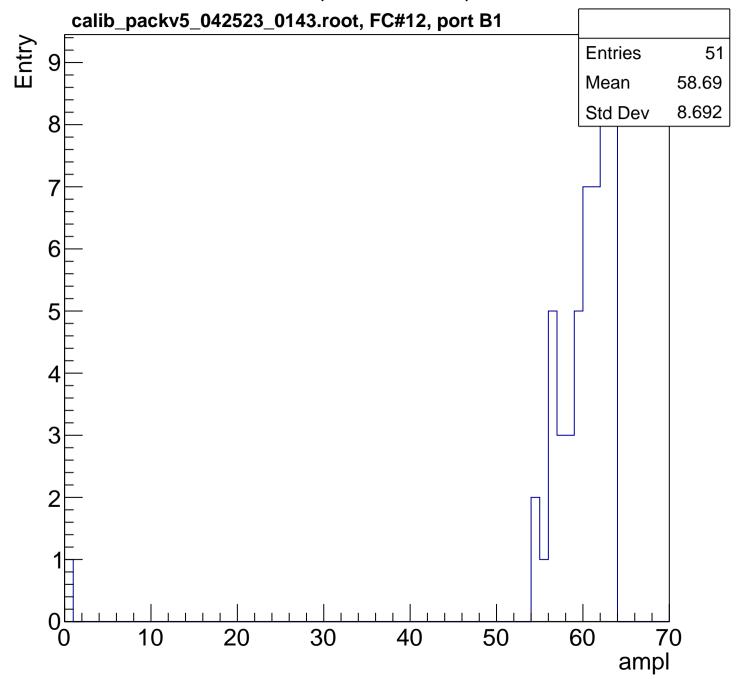


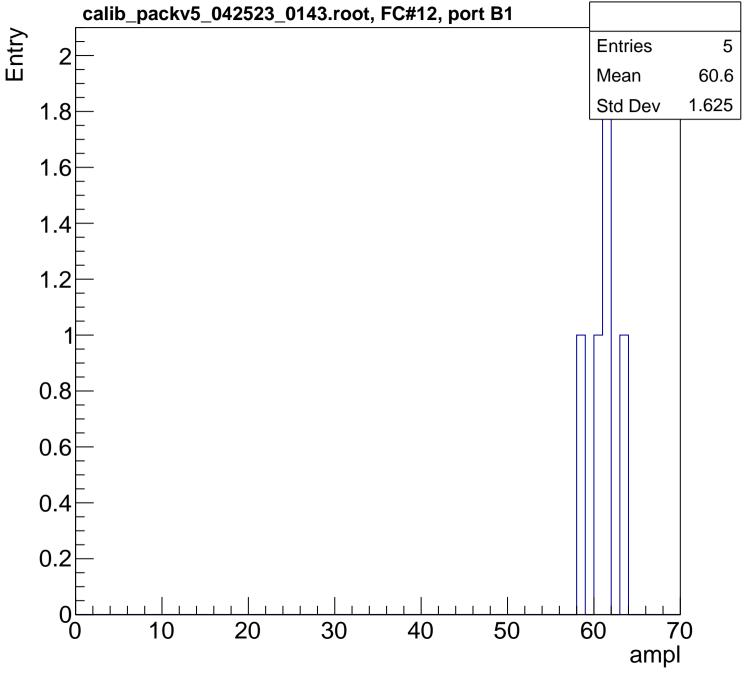




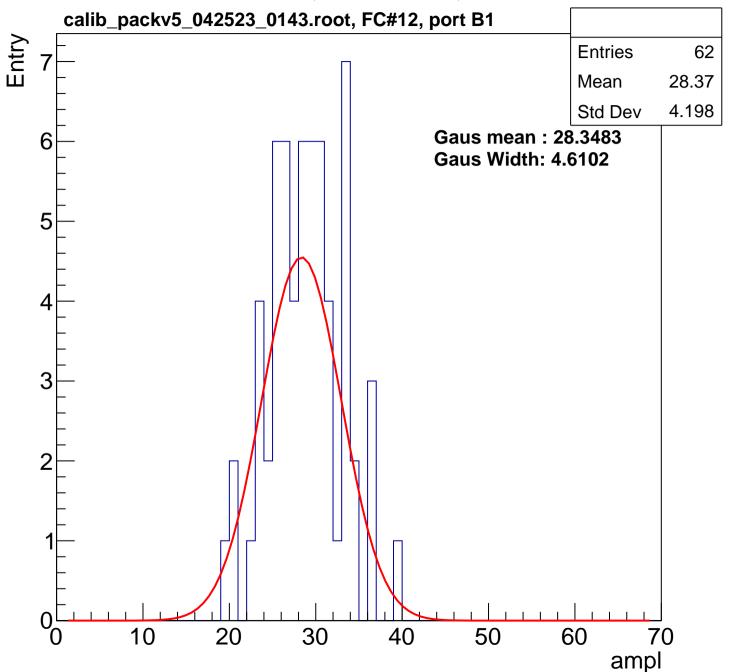


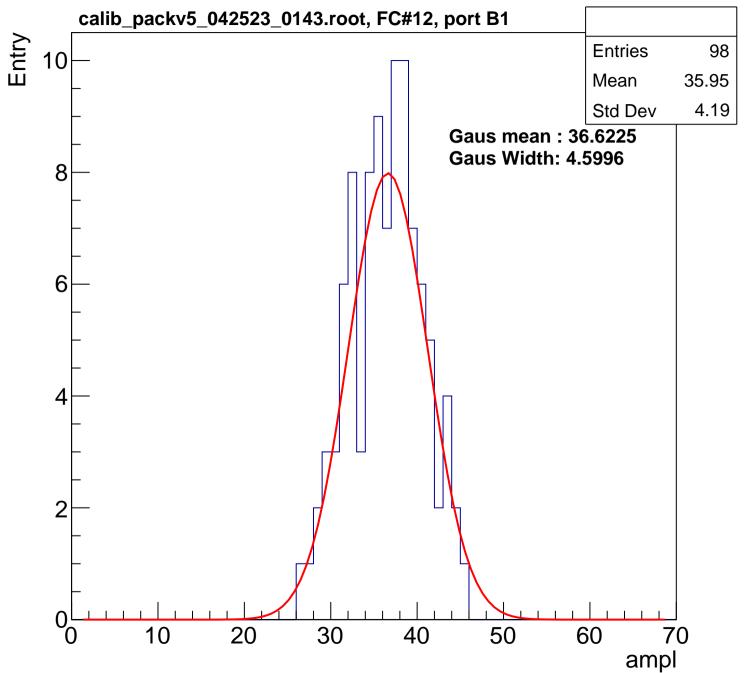


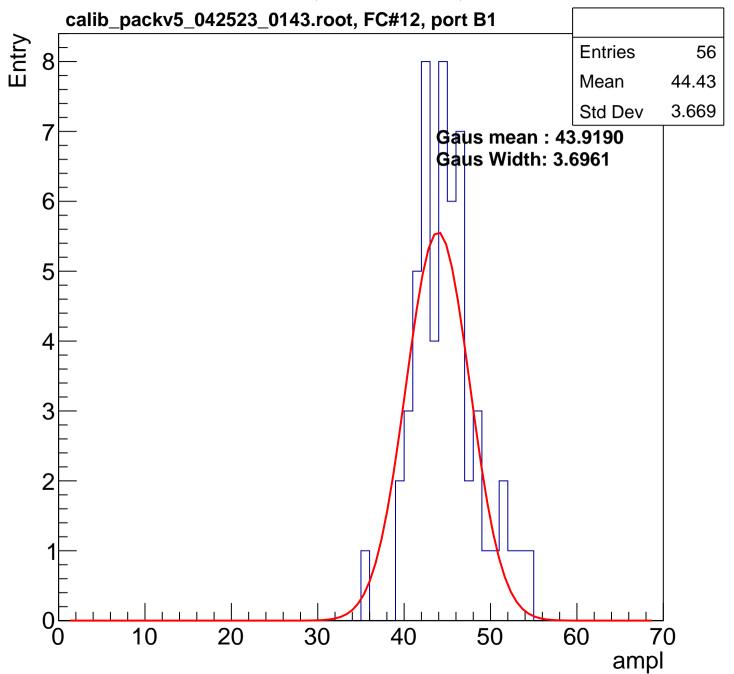


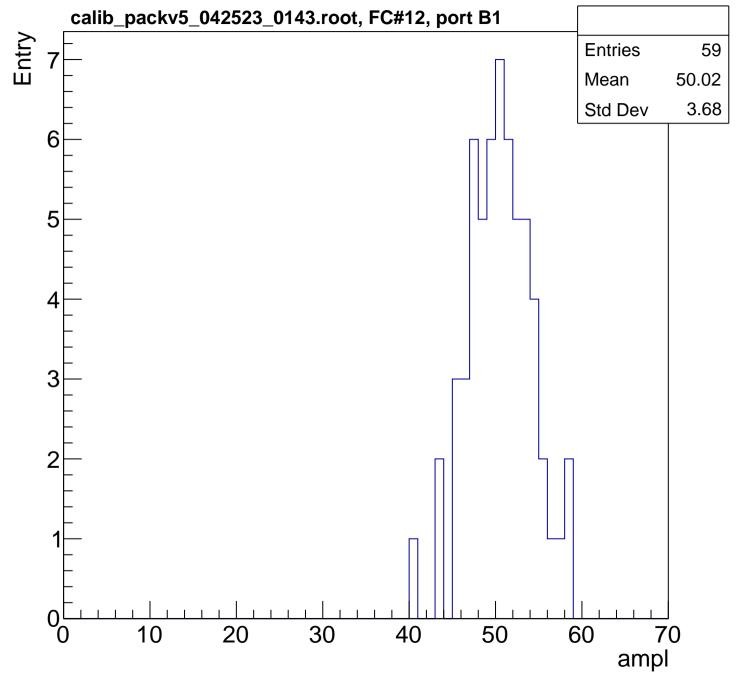


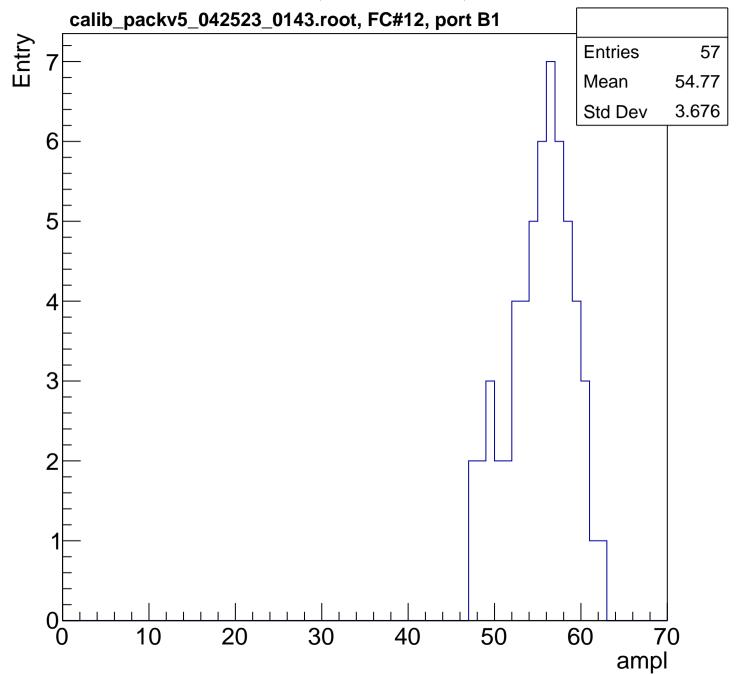
B0L102S, U4-ch11, adc7 calib_packv5_042523_0143.root, FC#12, port B1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

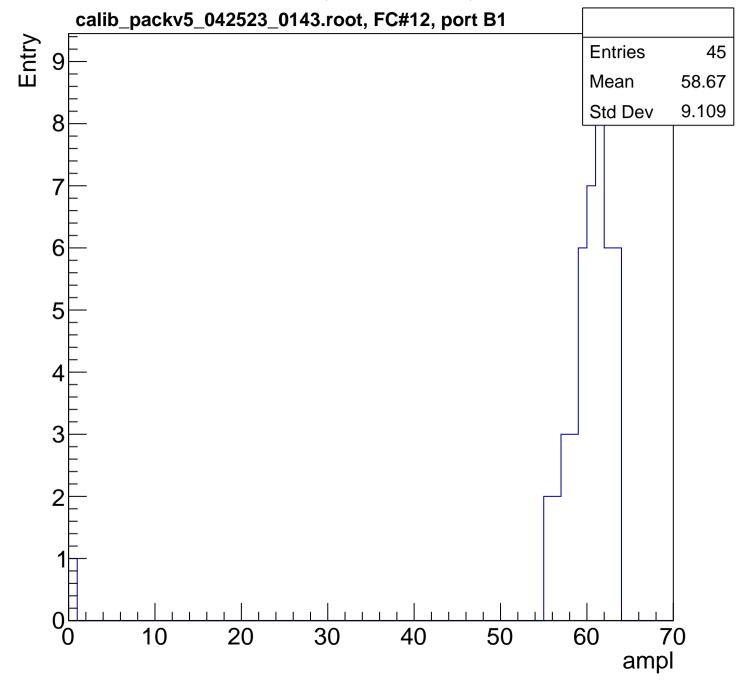


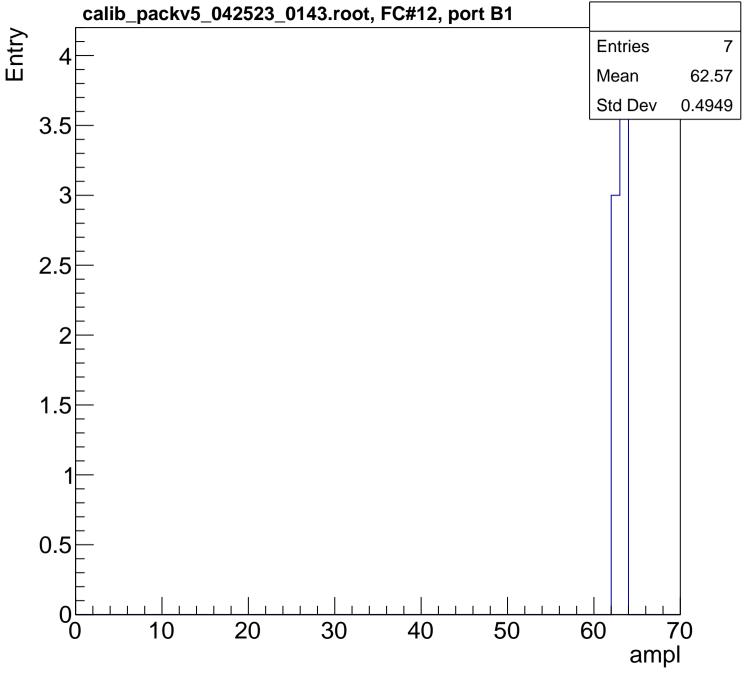




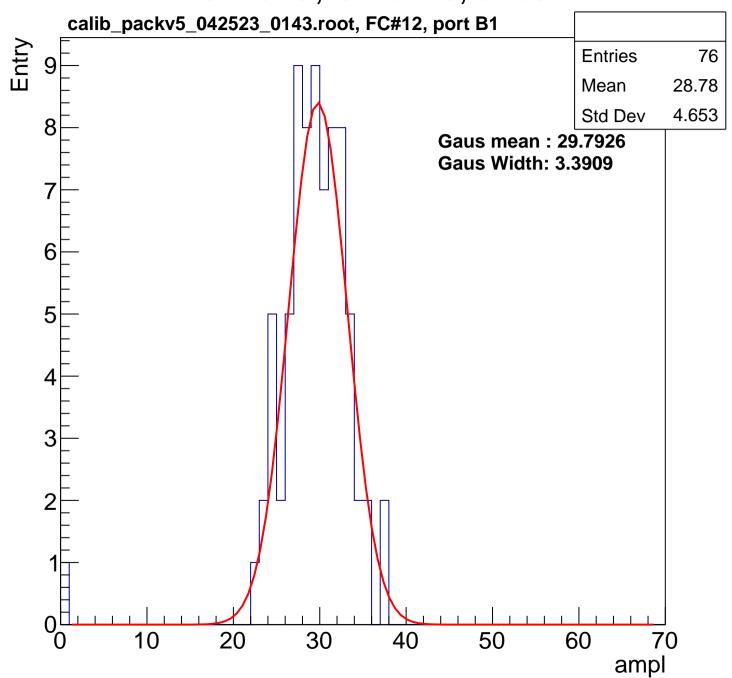


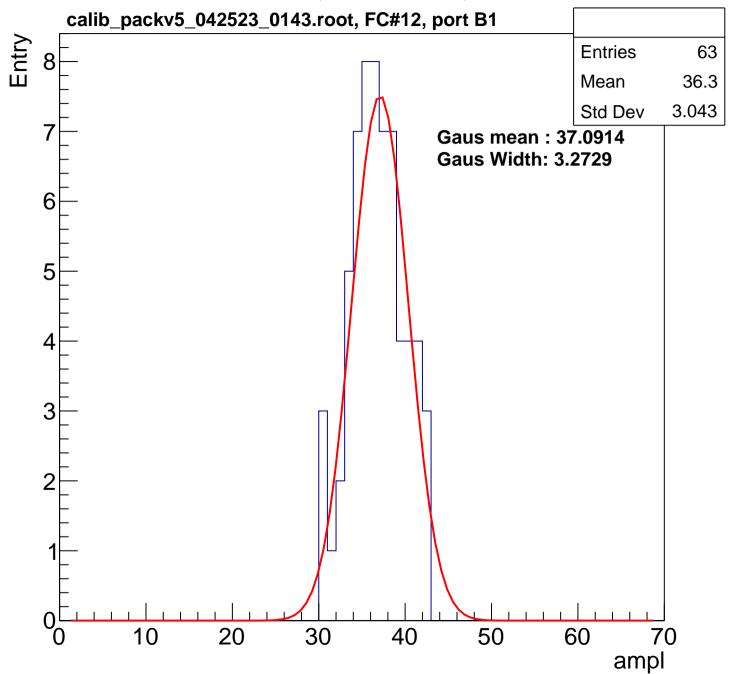


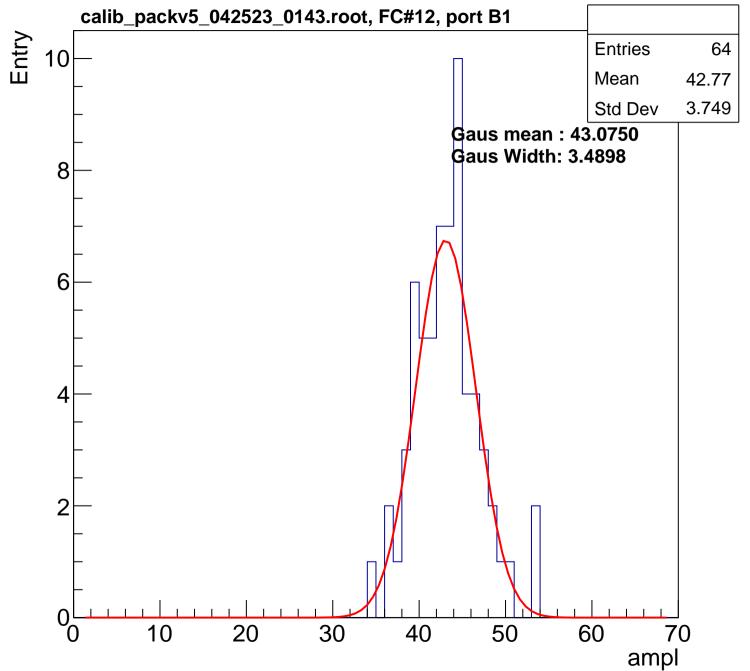


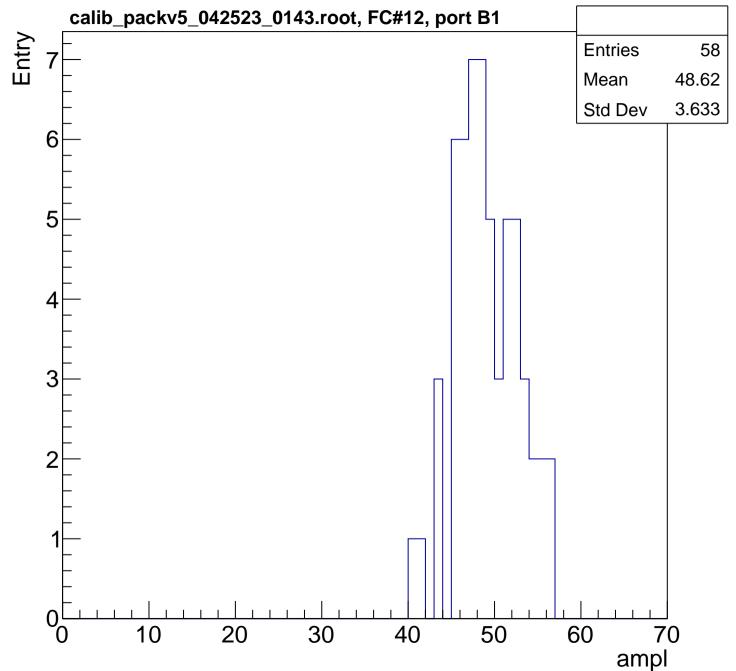


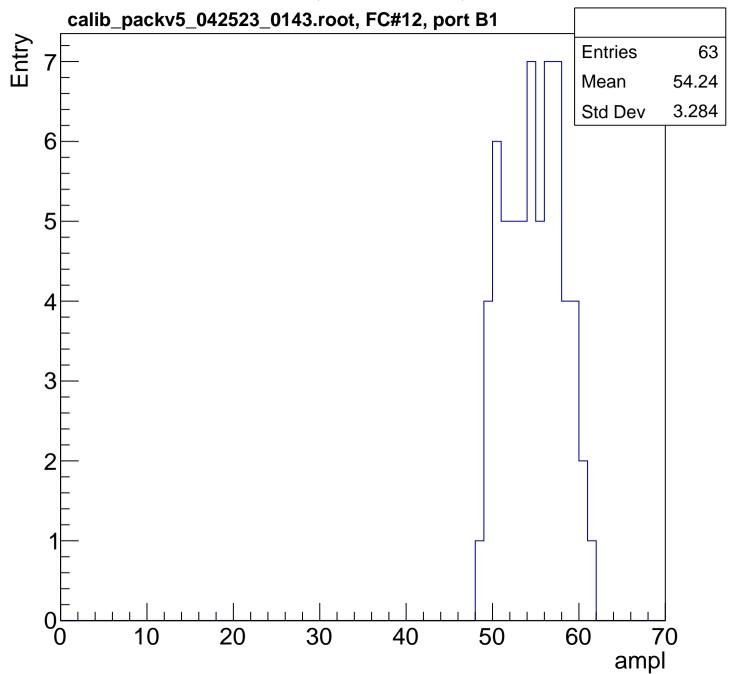
B0L102S, U4-ch12, adc7 calib_packv5_042523_0143.root, FC#12, port B1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

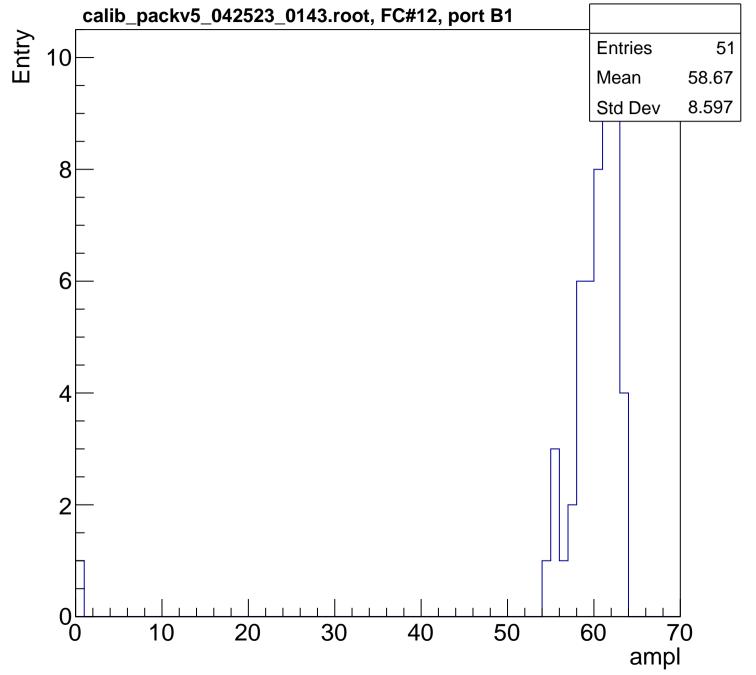


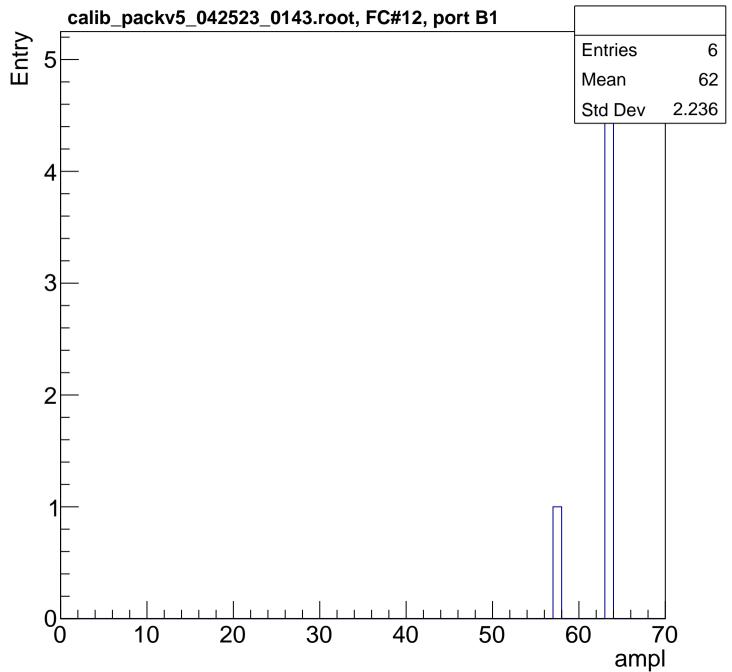


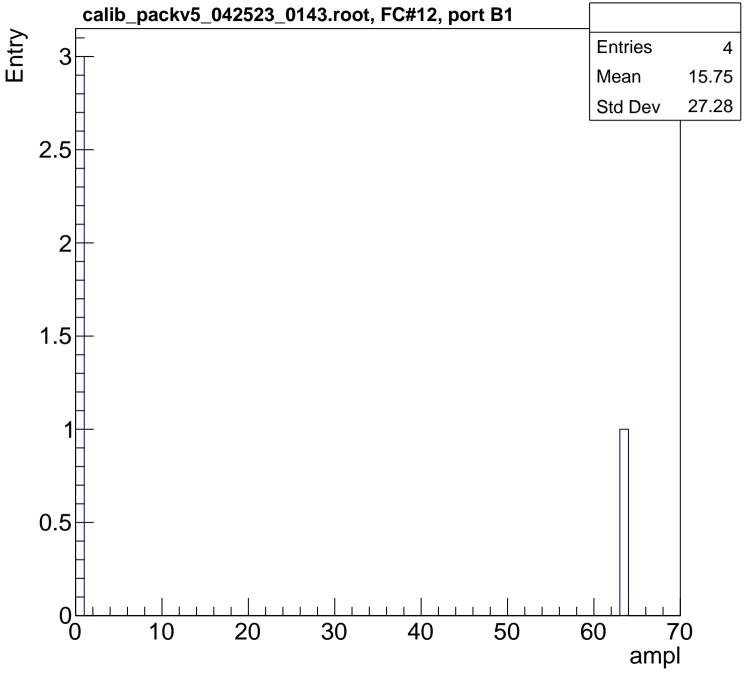


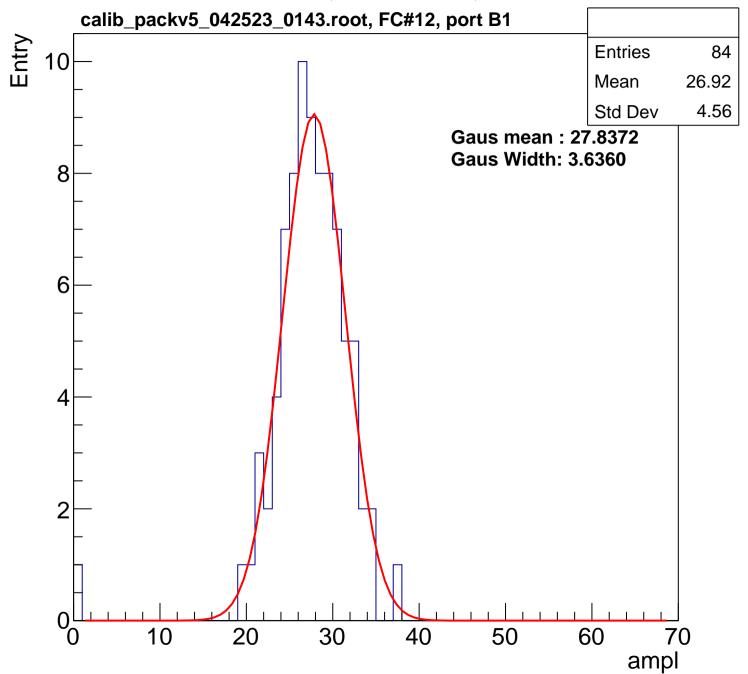


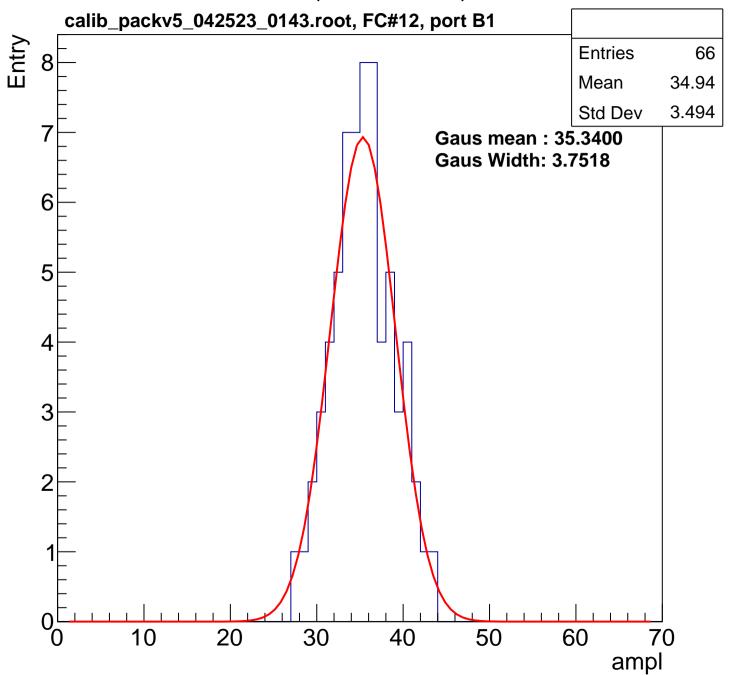


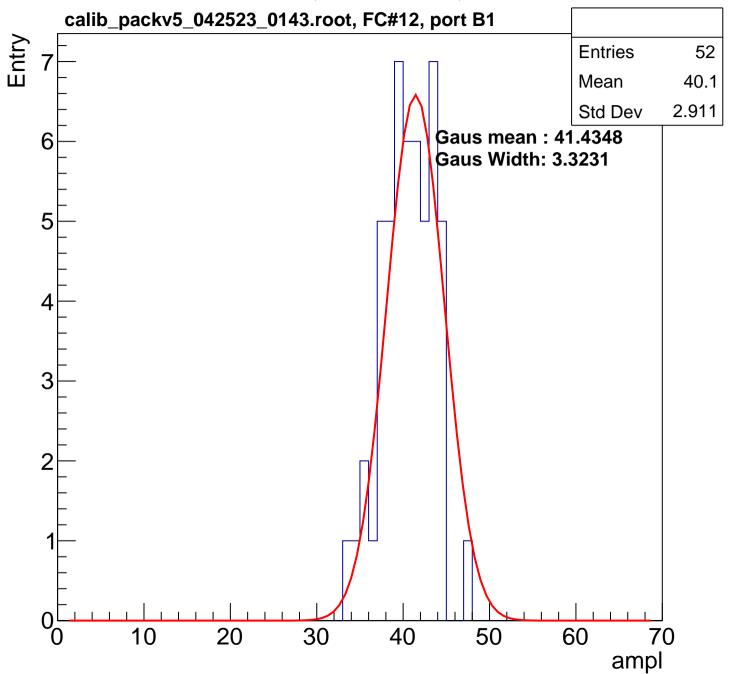


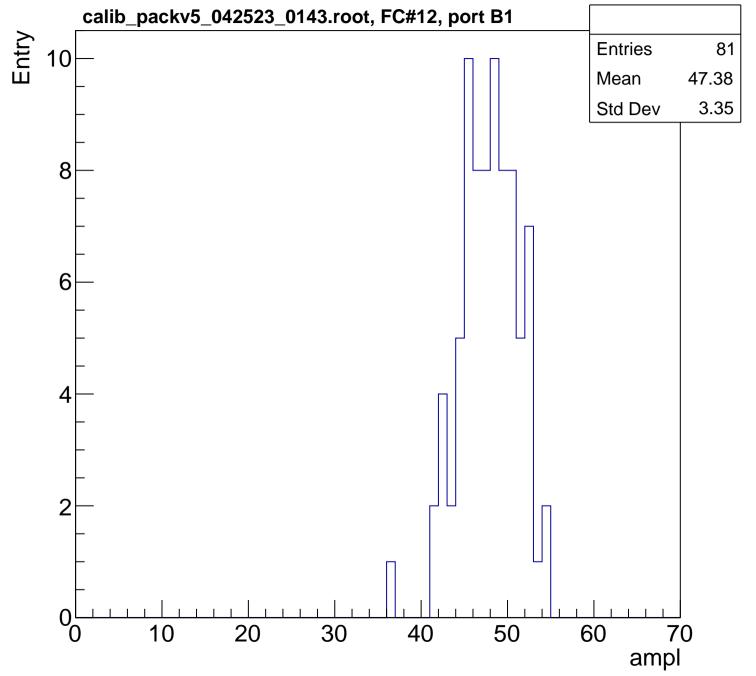


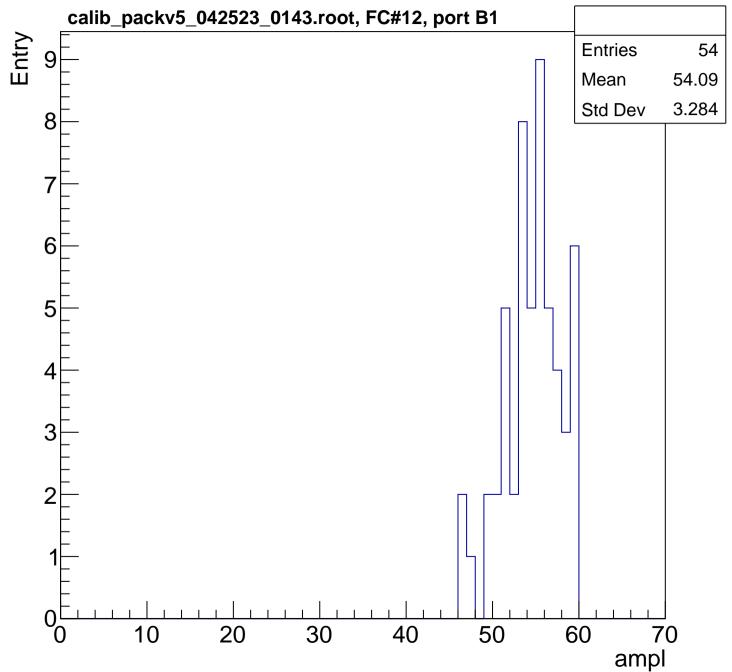


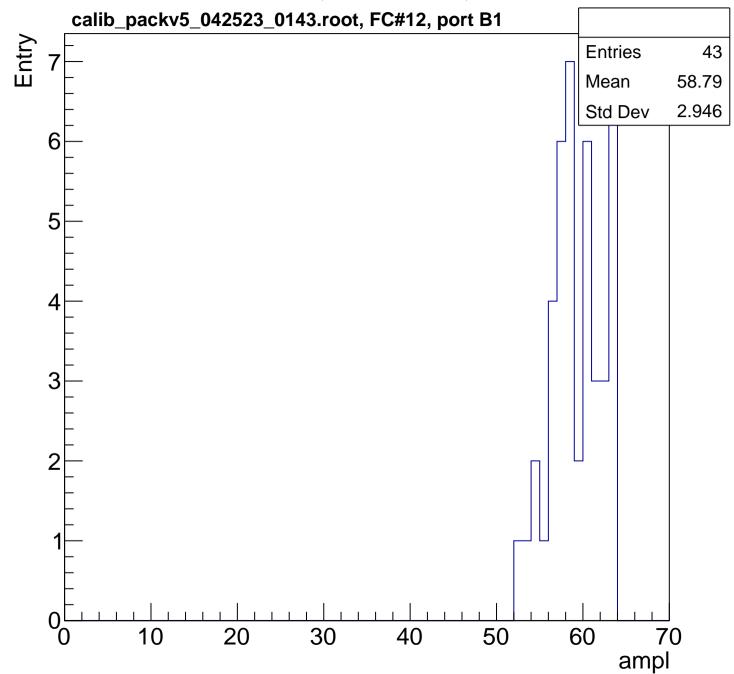


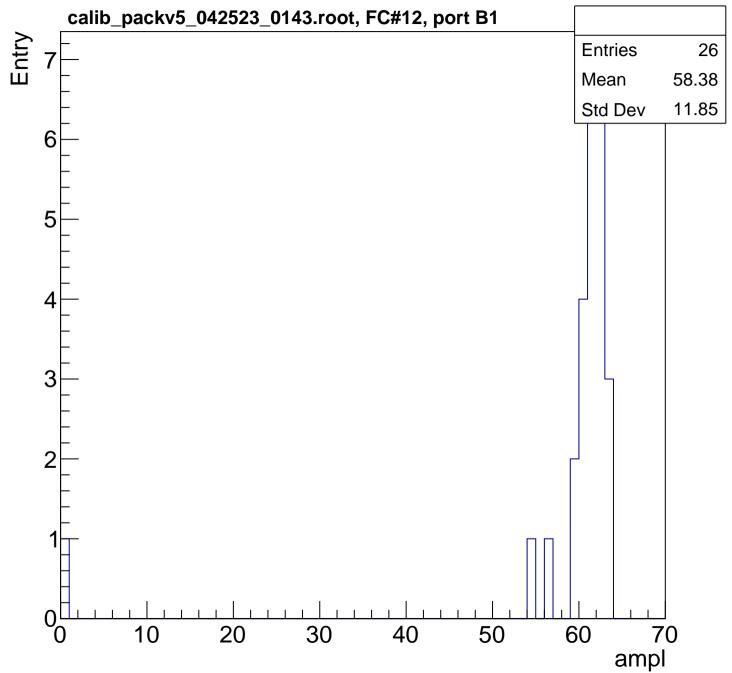




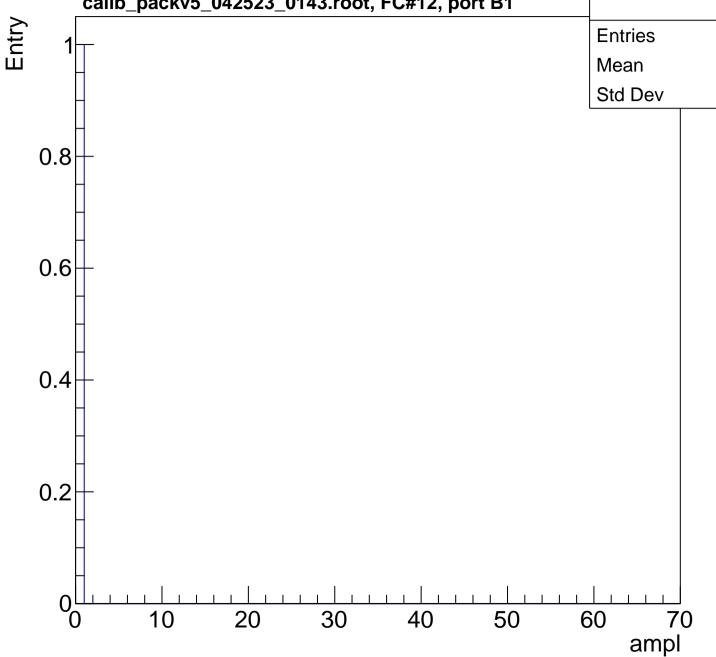


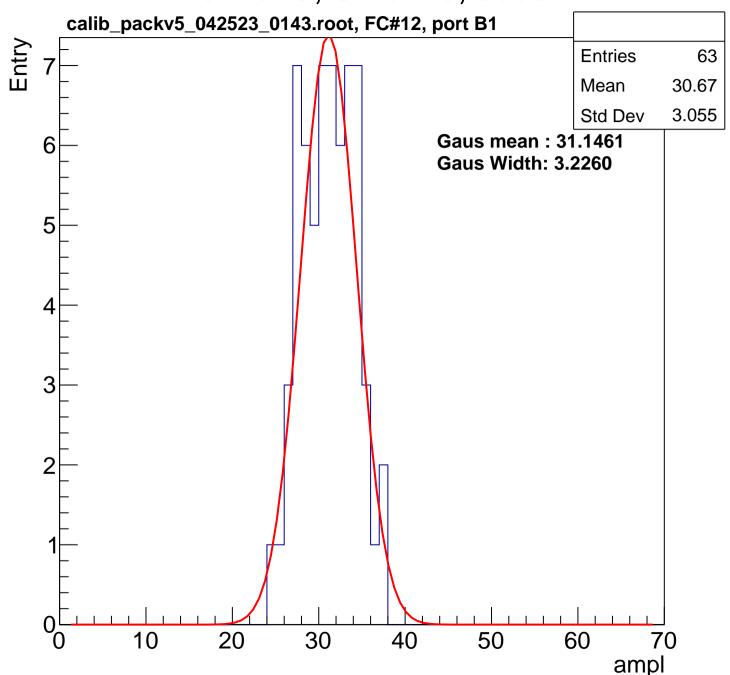


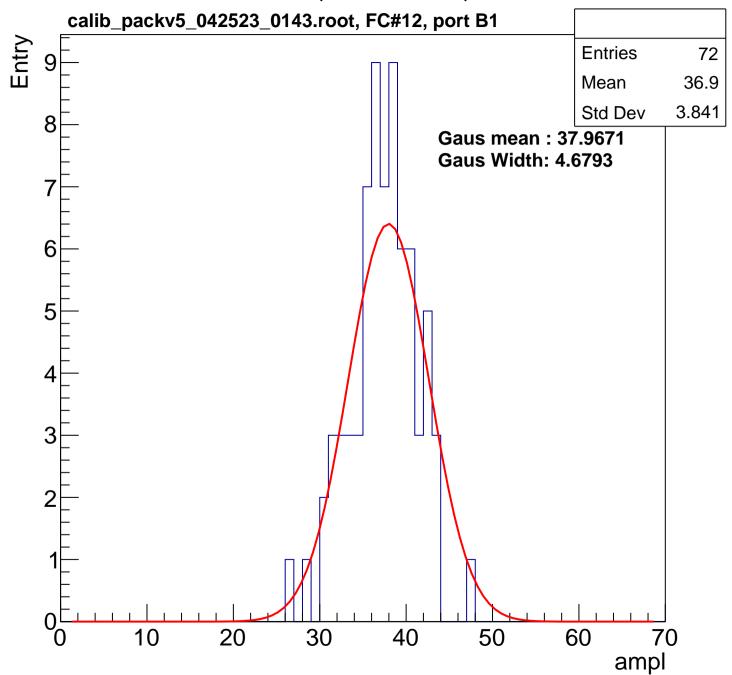


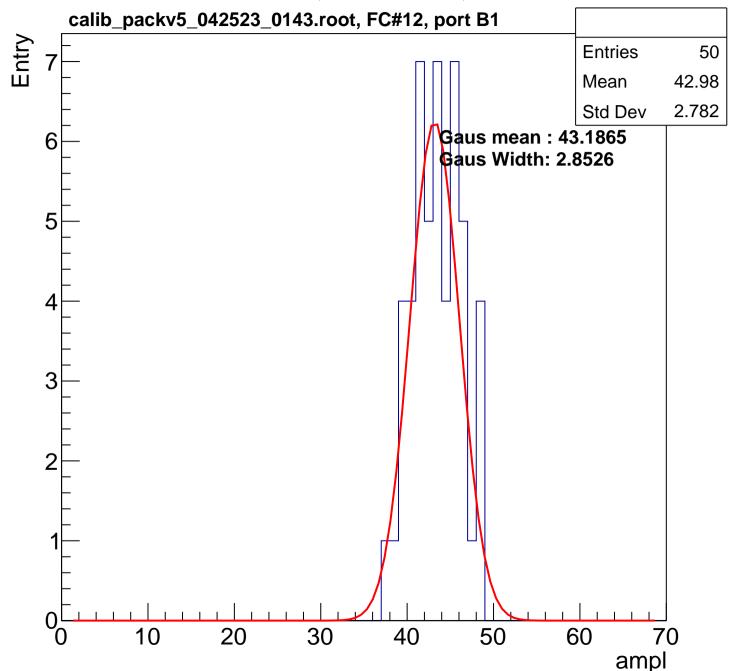


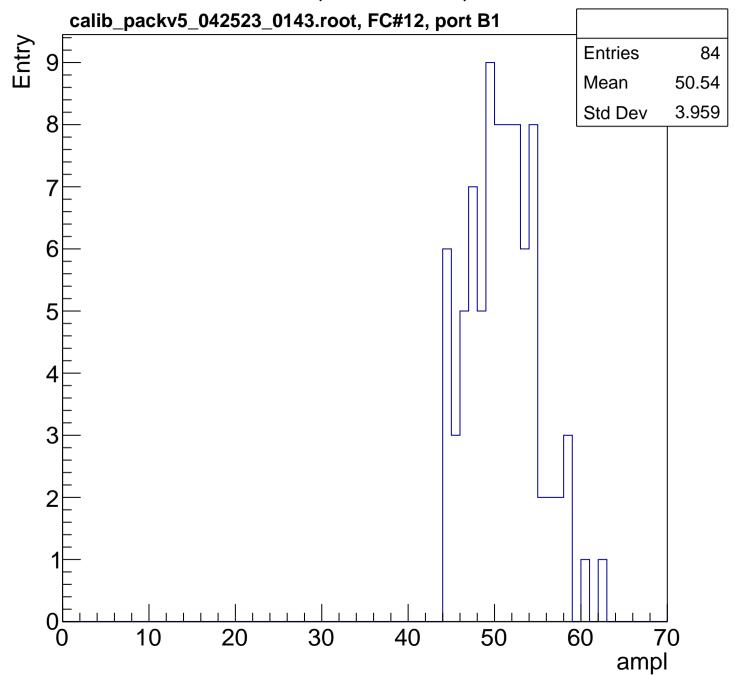
B0L102S, U4-ch14, adc7 calib_packv5_042523_0143.root, FC#12, port B1

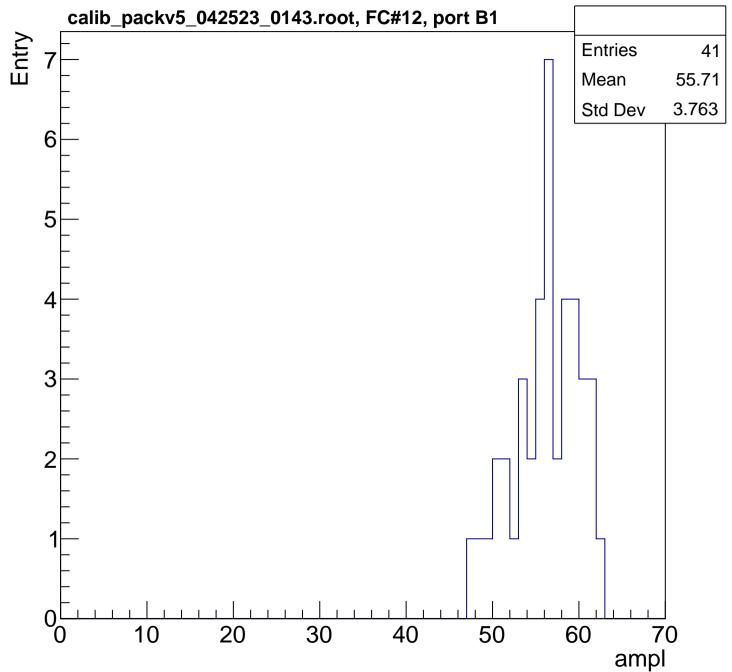


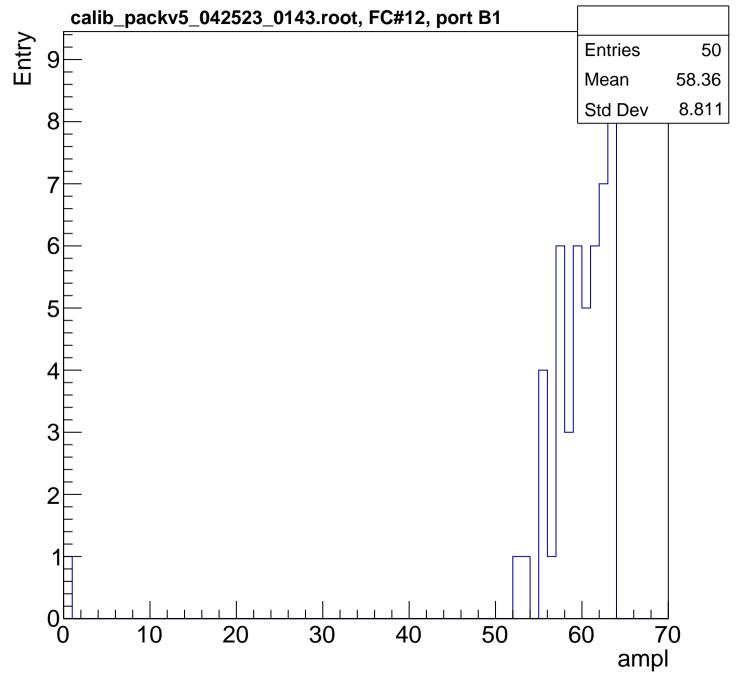


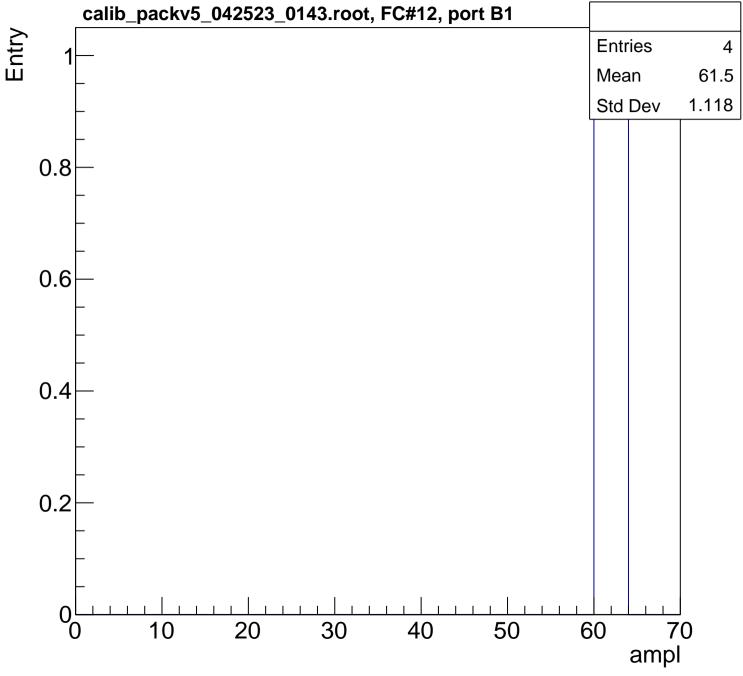




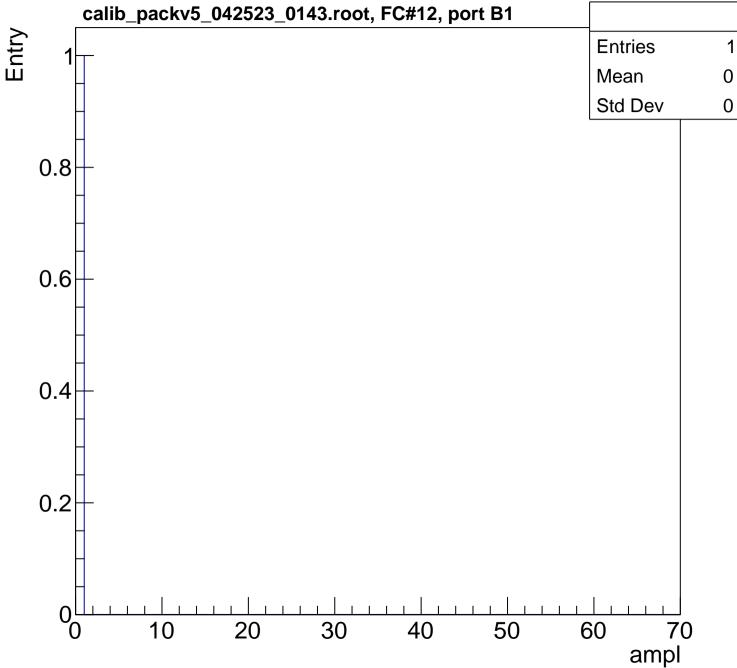


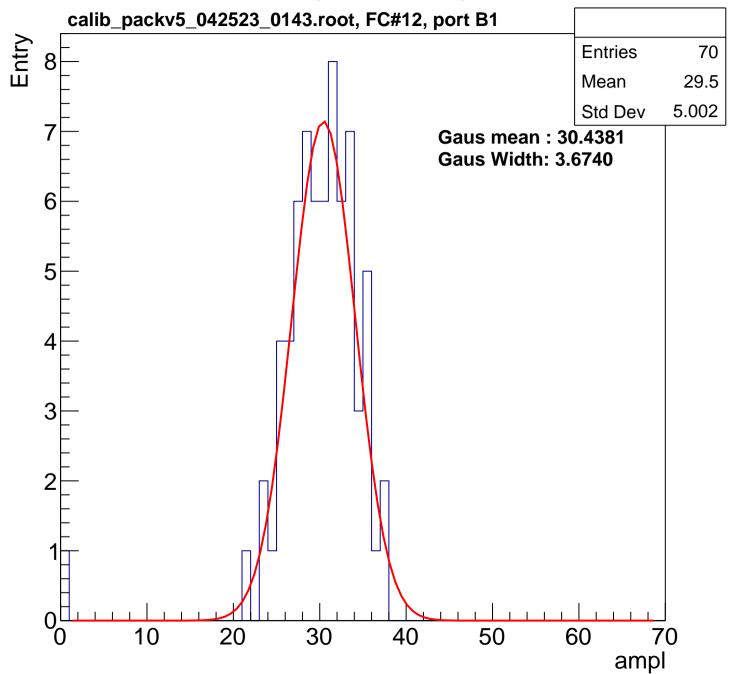


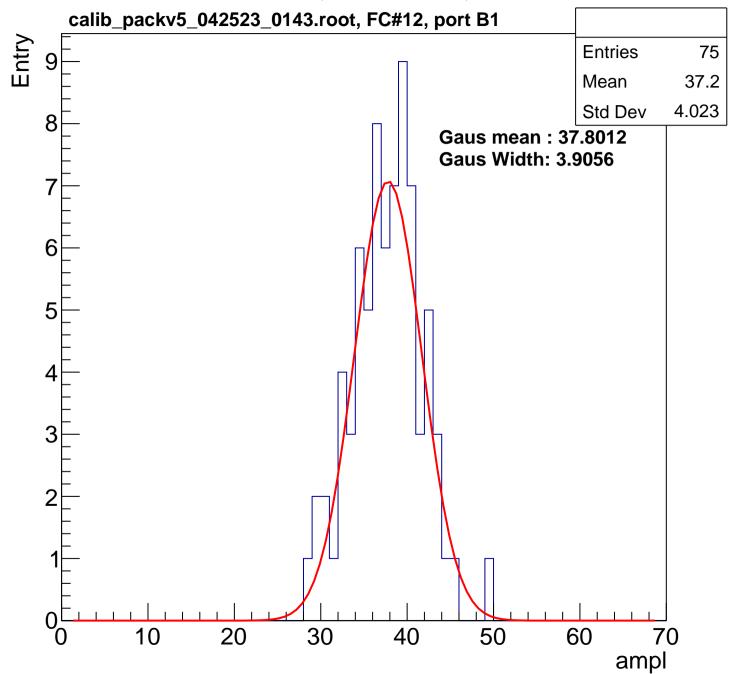


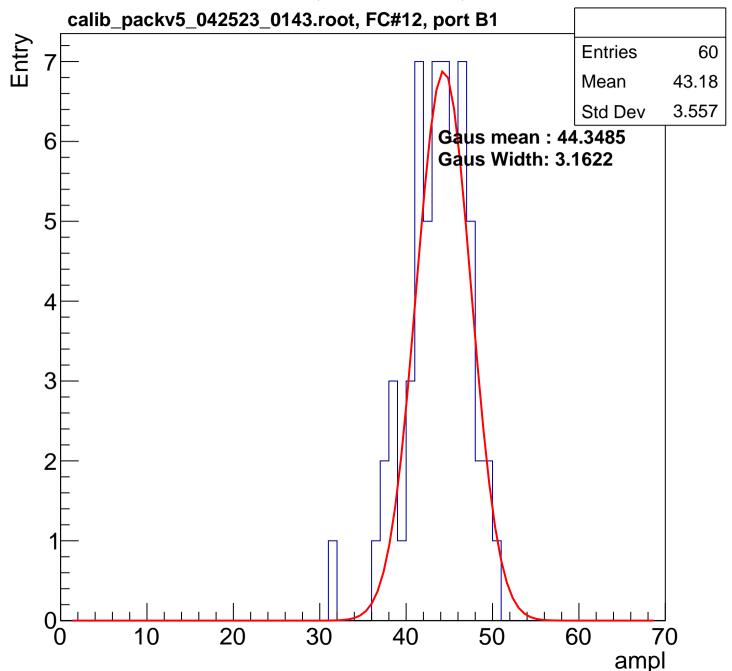


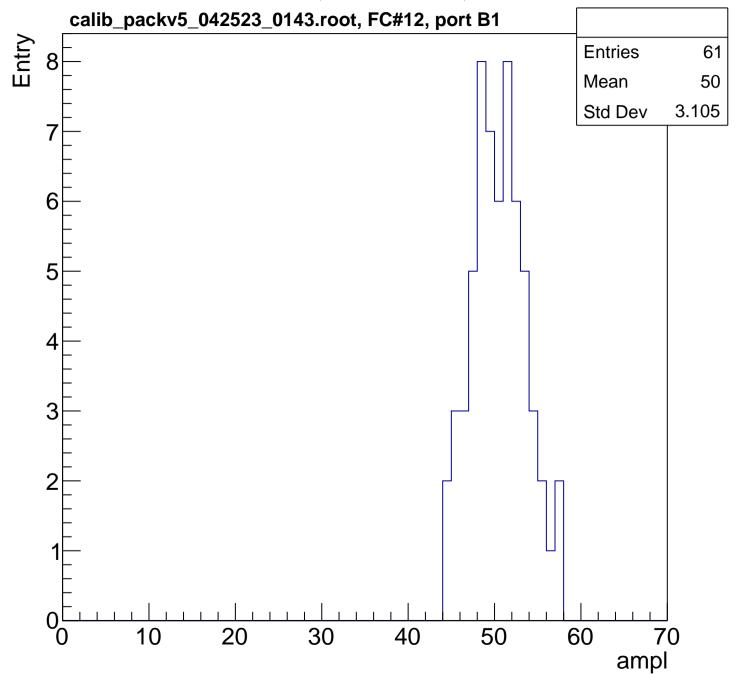
B0L102S, U4-ch15, adc7 5_042523_0143.root, FC#12, port B1

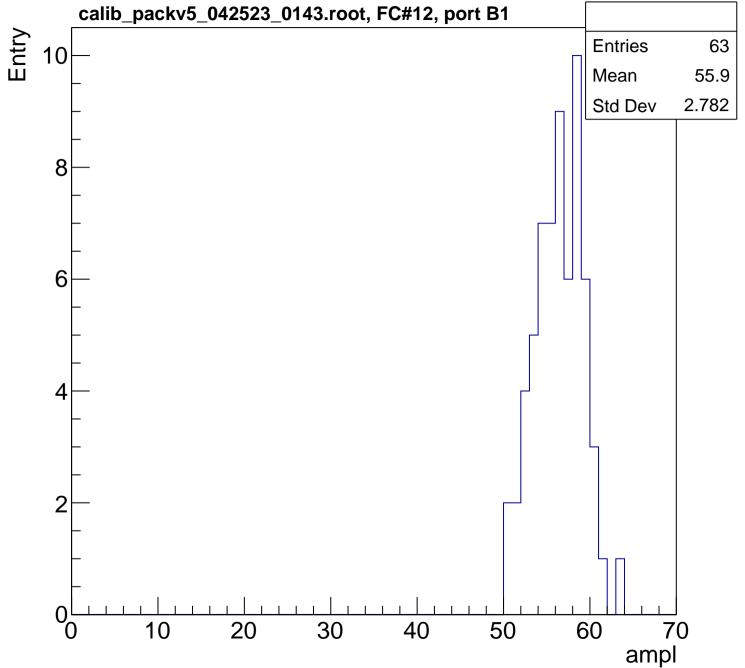


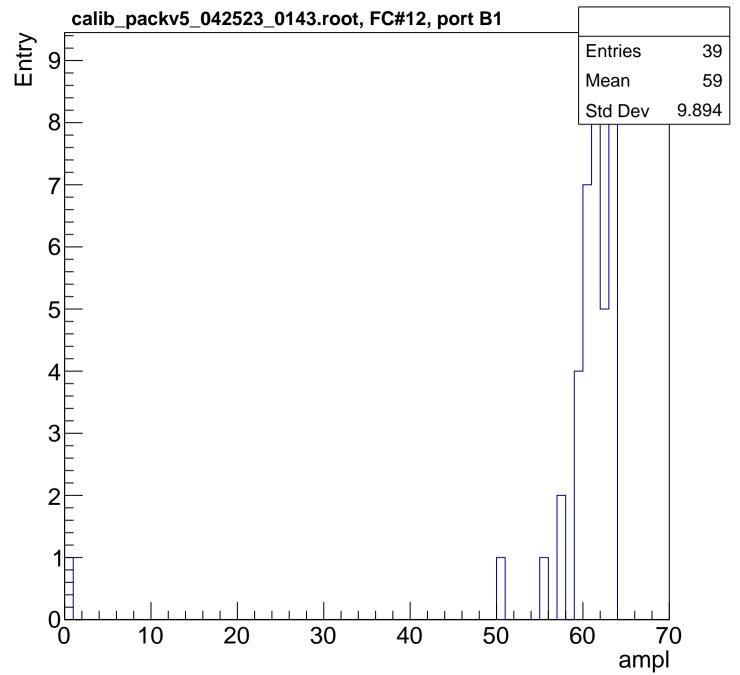


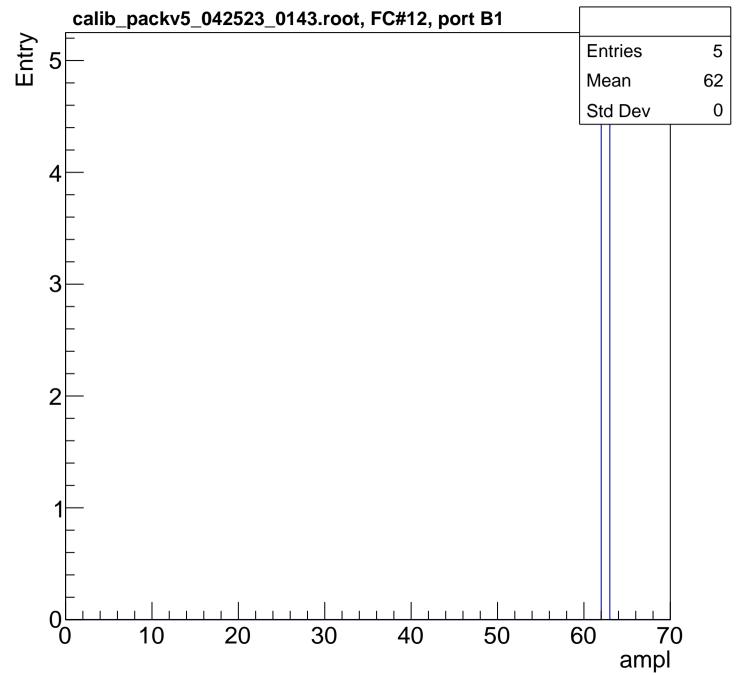




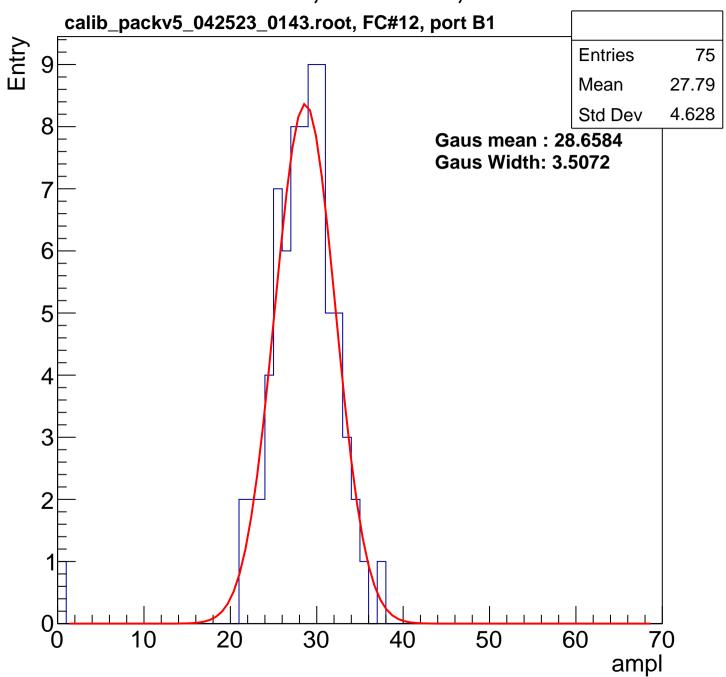


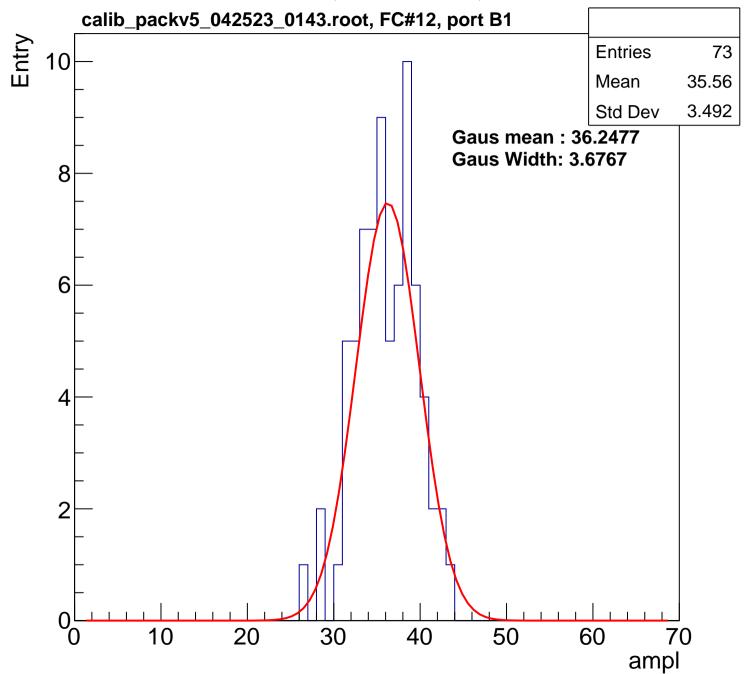


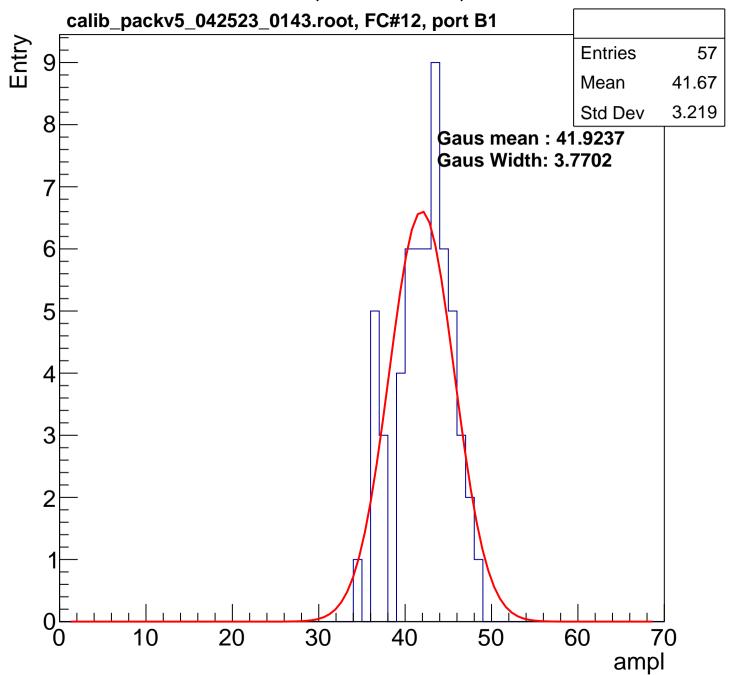


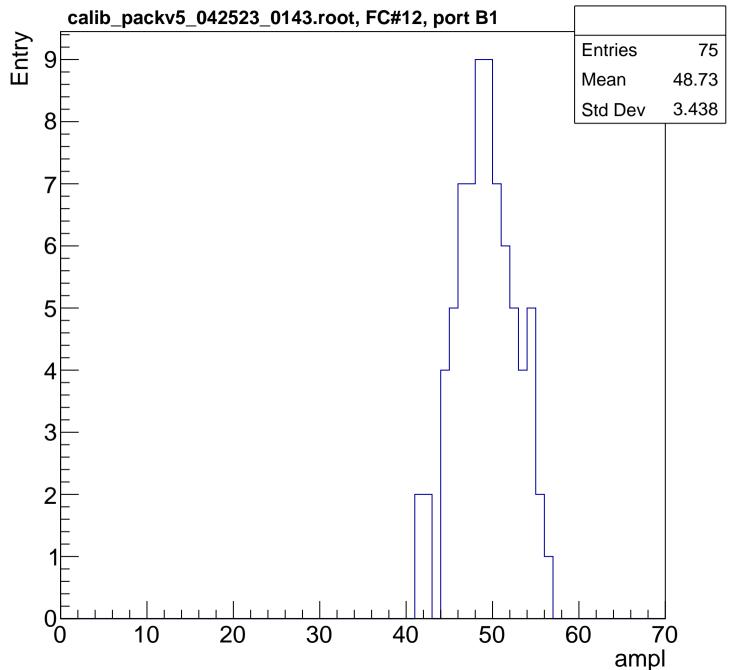


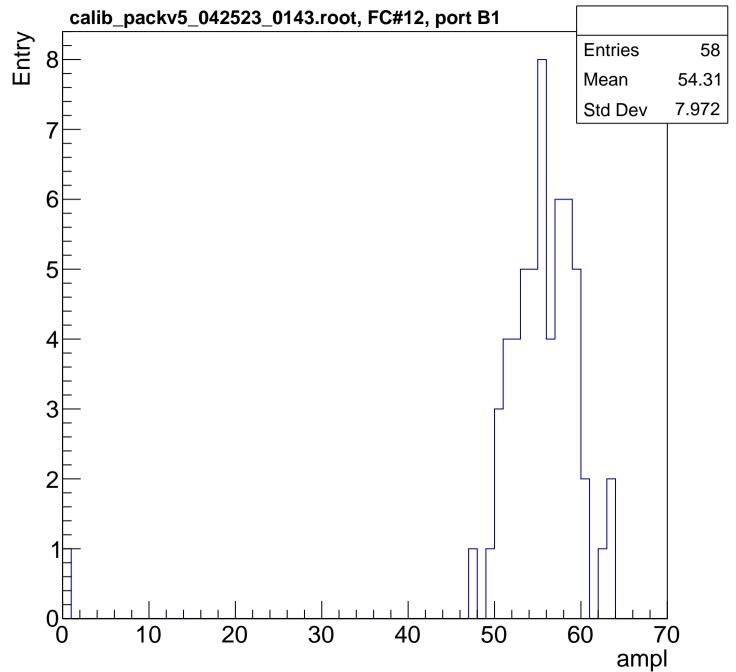


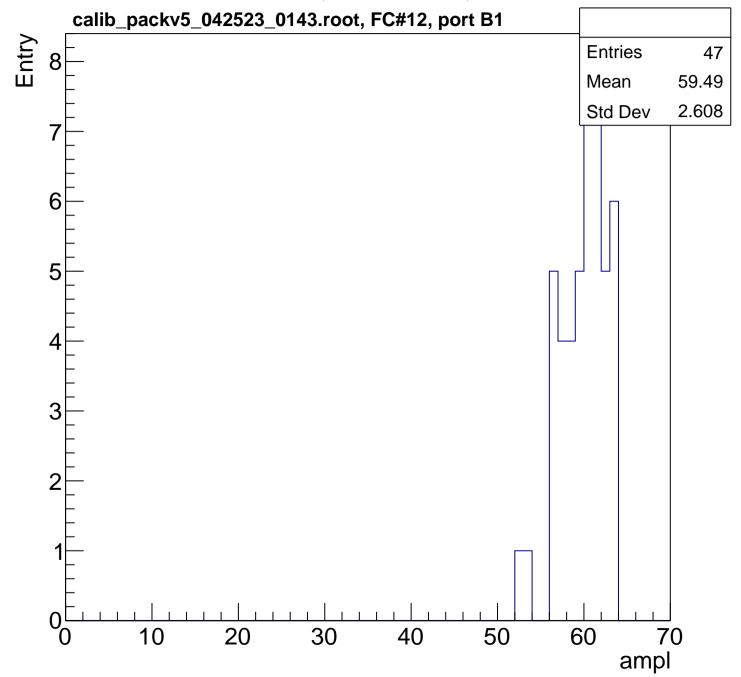


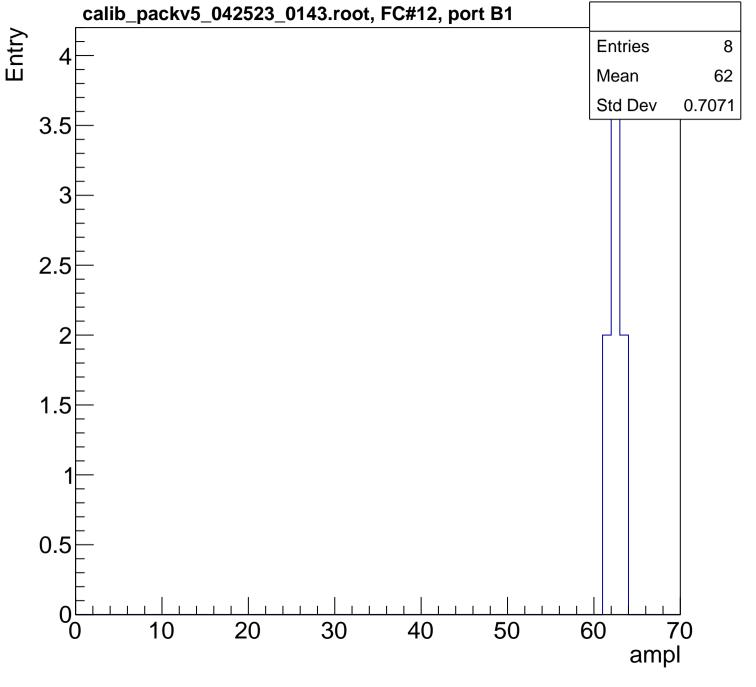




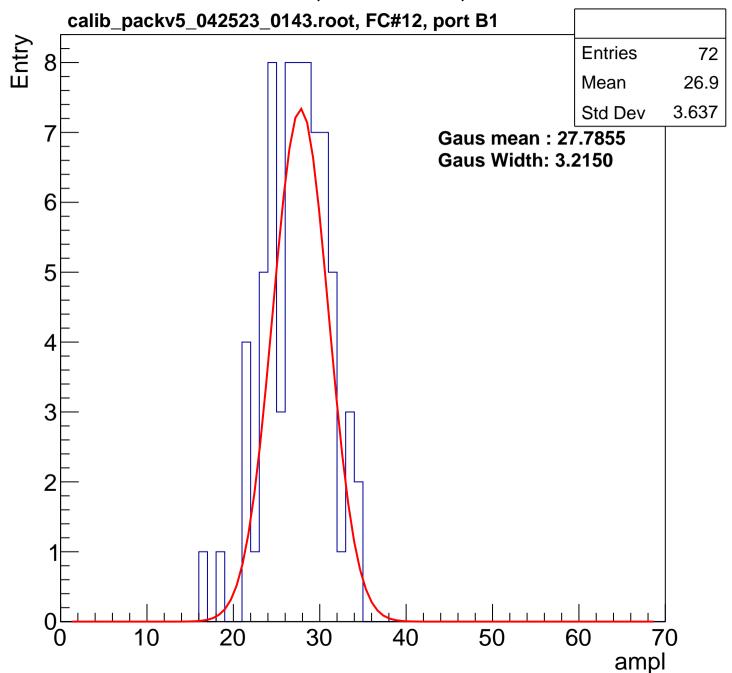


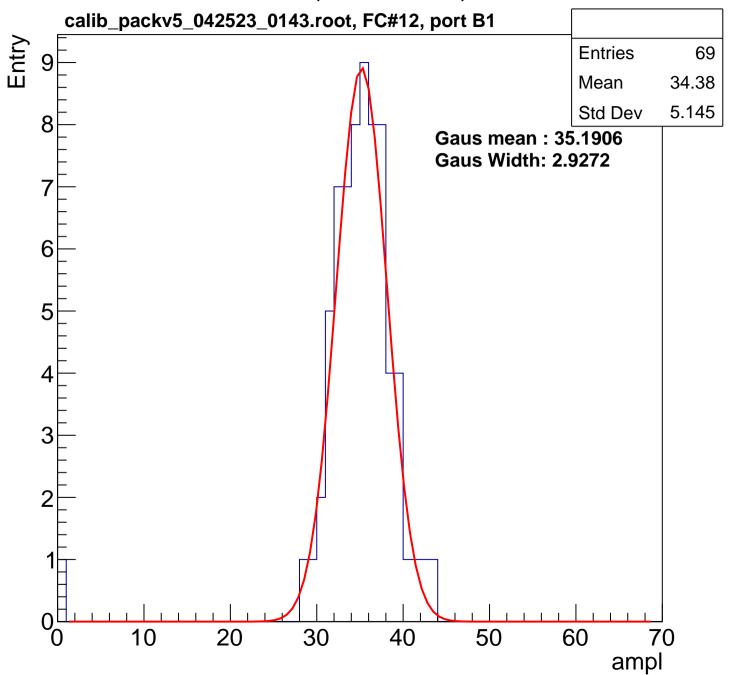


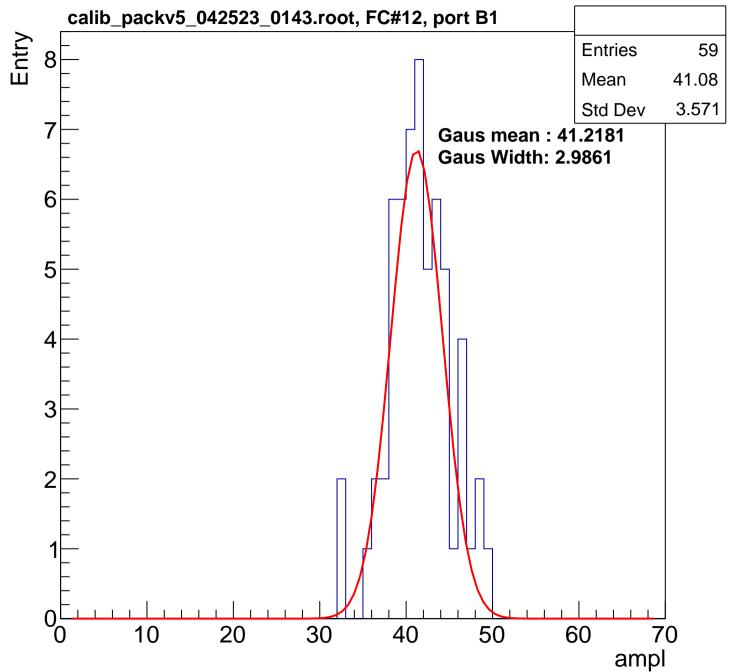


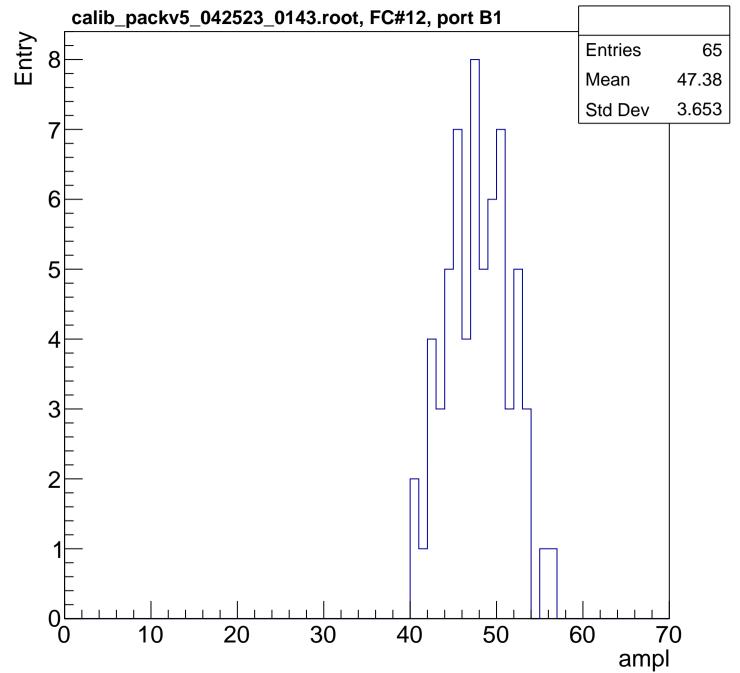


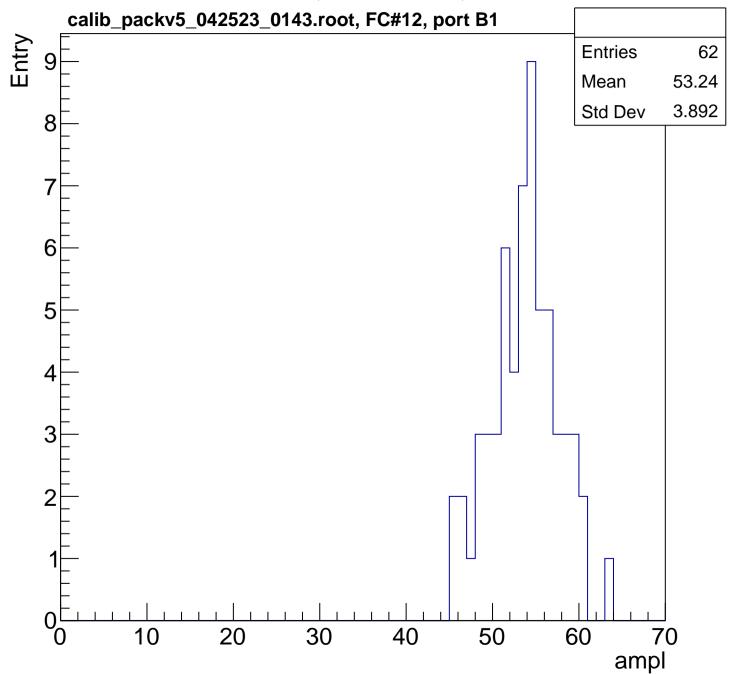
B0L102S, U4-ch17, adc7 calib_packv5_042523_0143.root, FC#12, port B1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

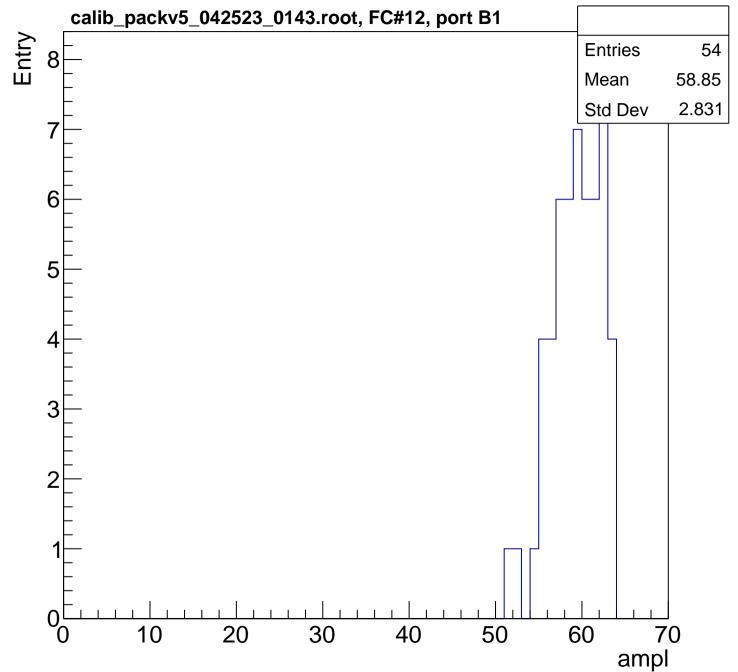


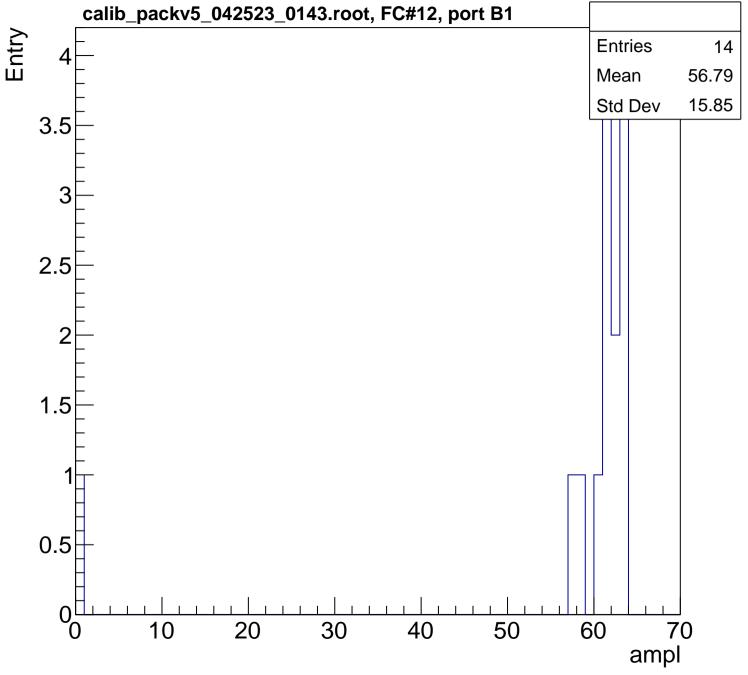


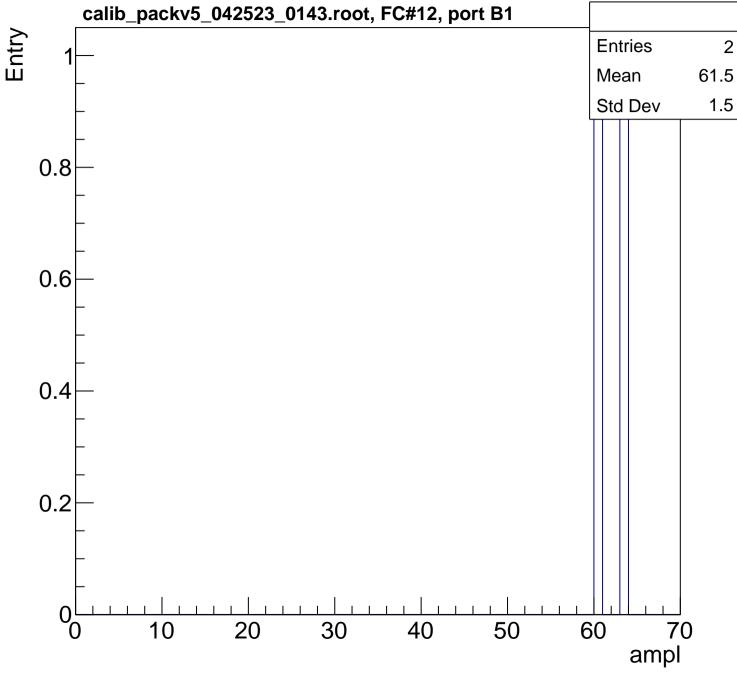


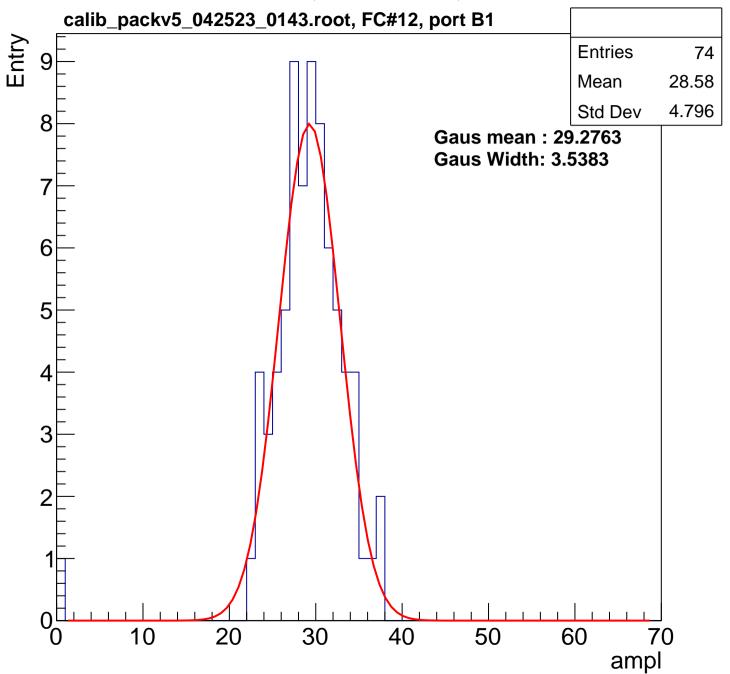


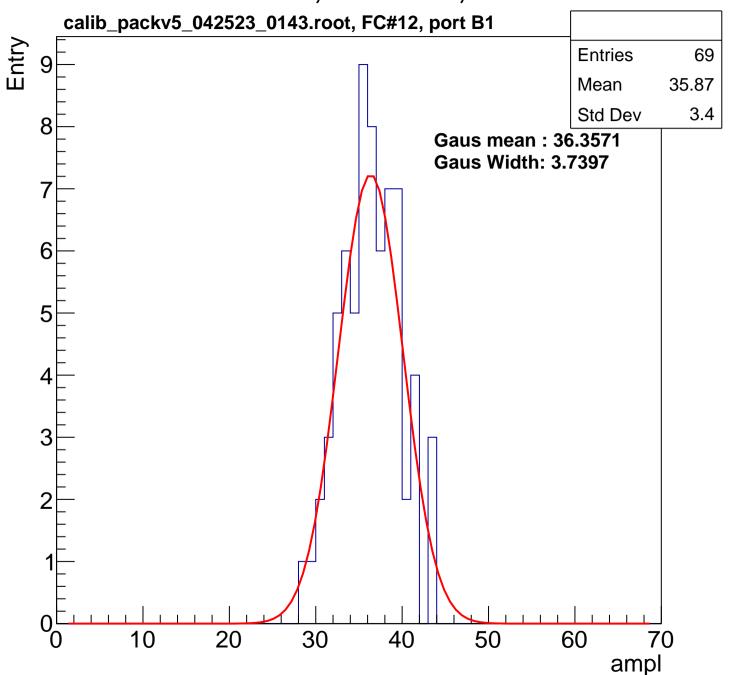


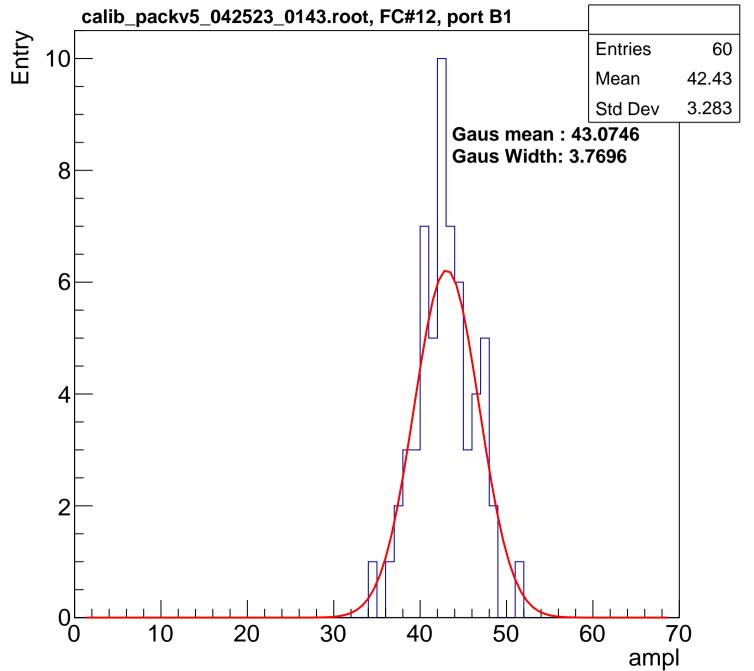


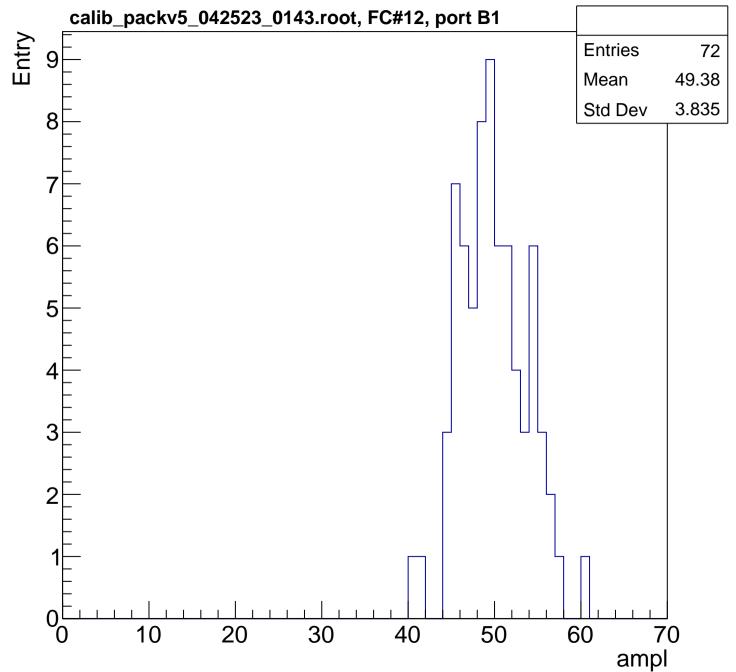


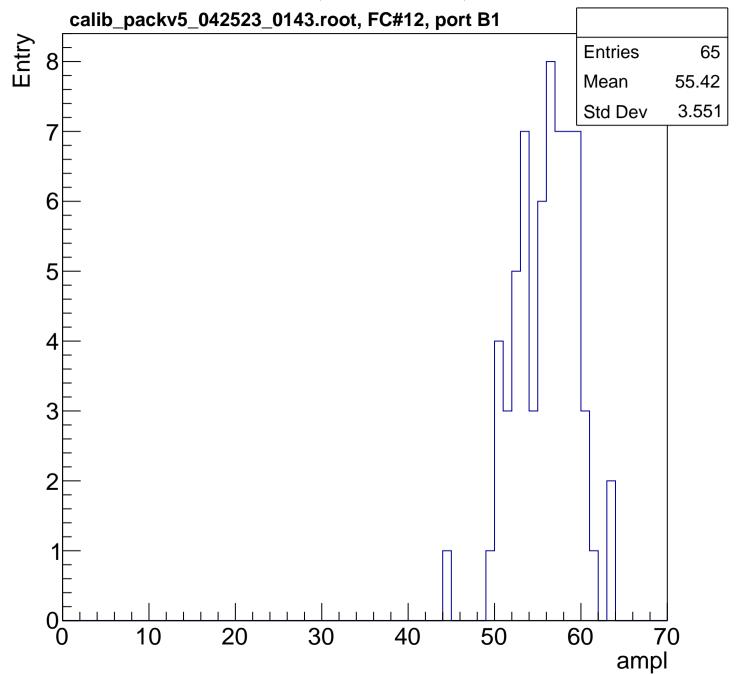


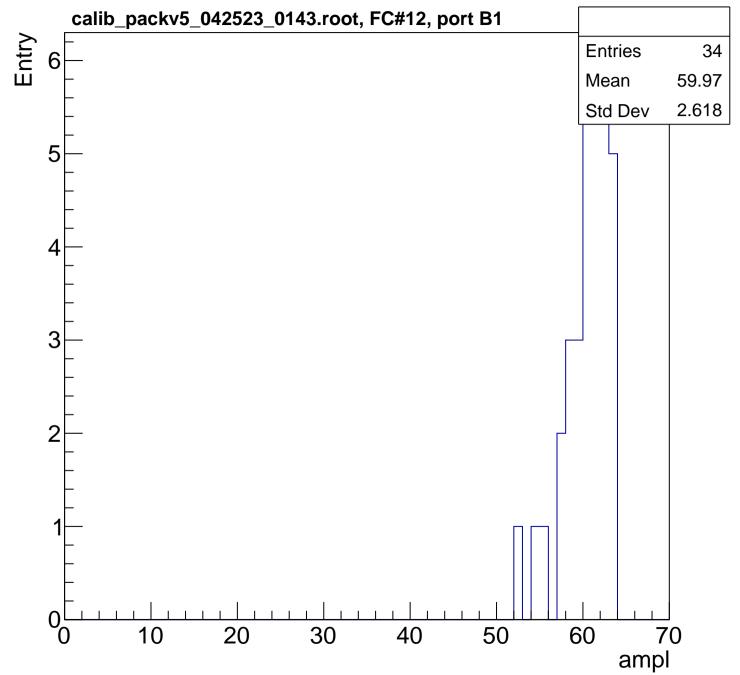


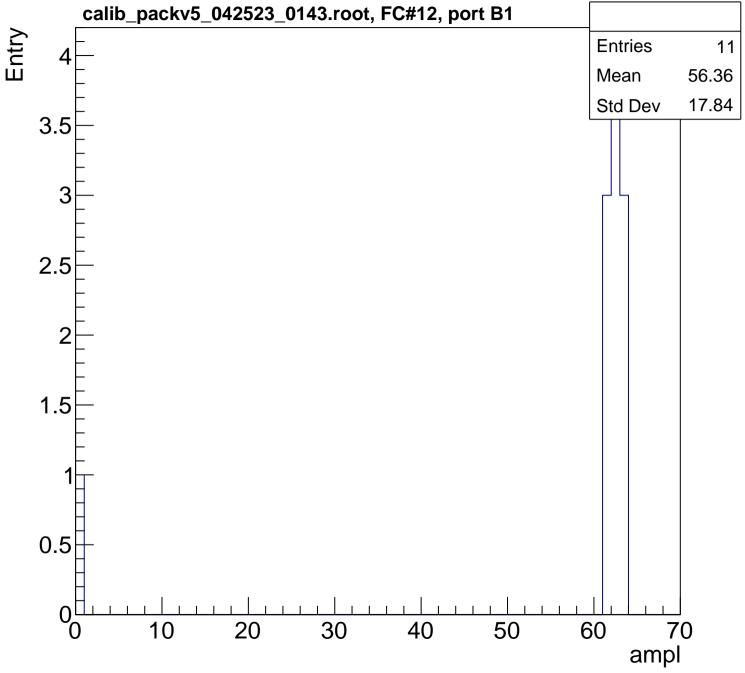




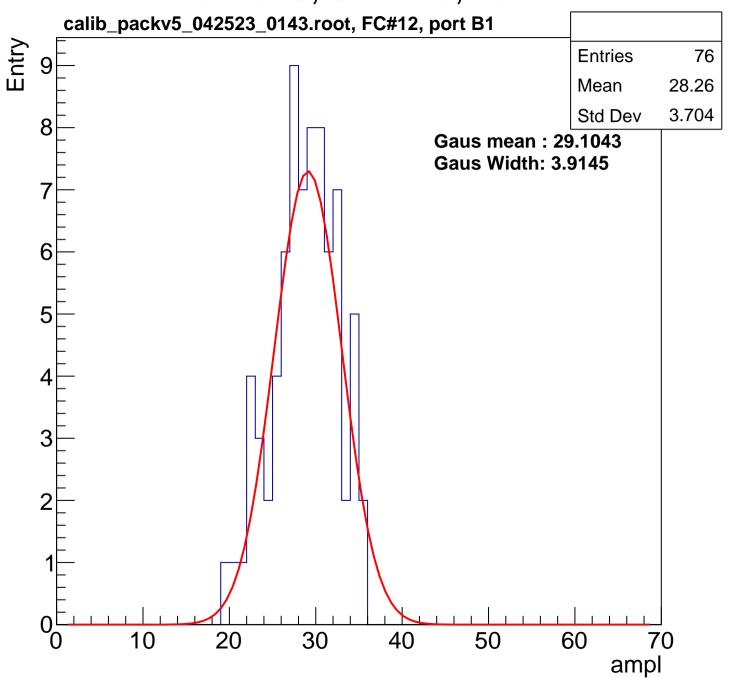


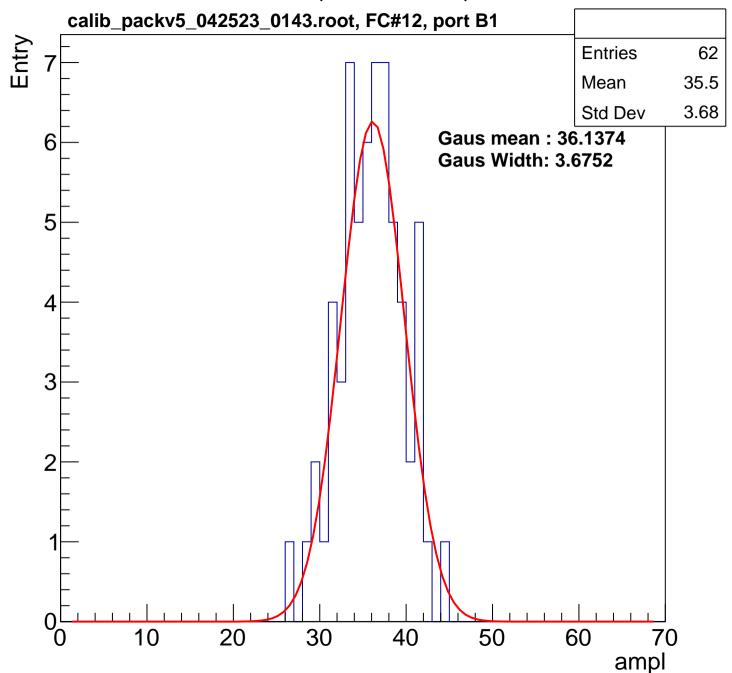


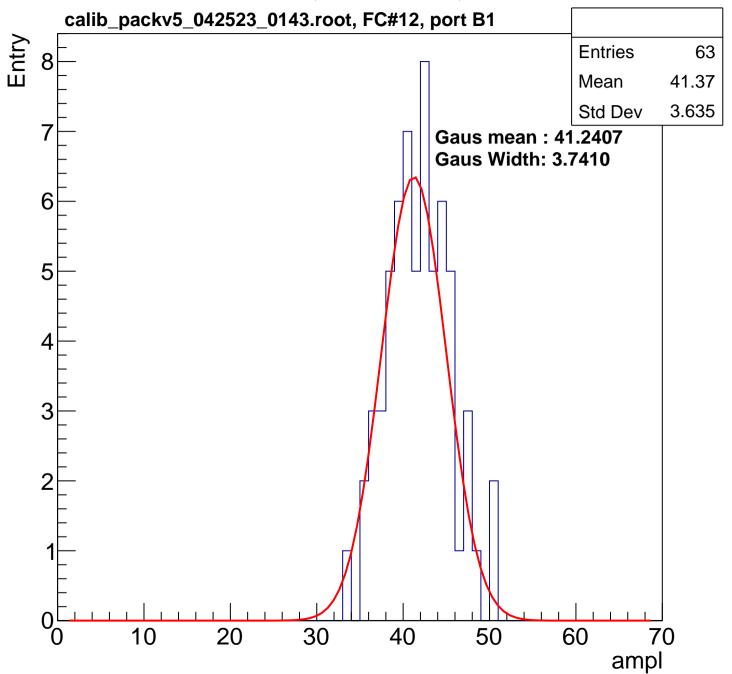


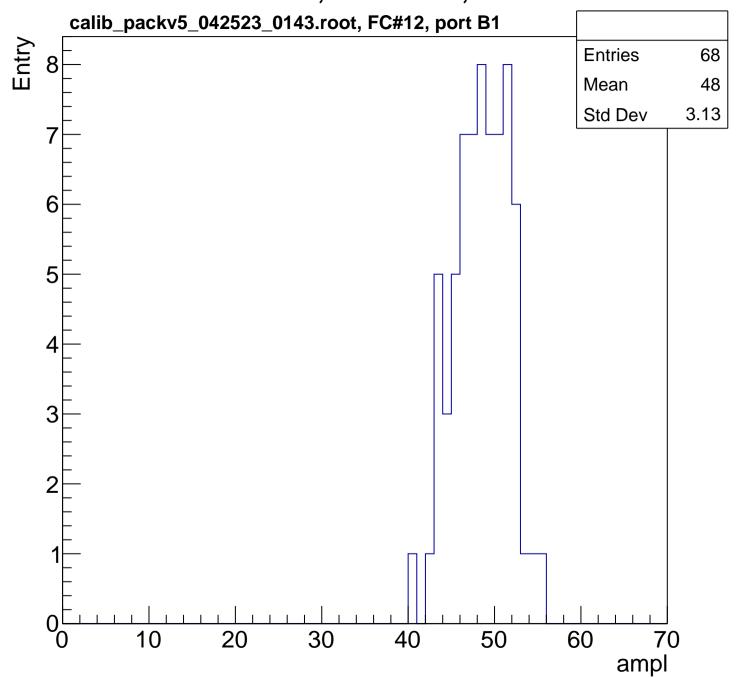


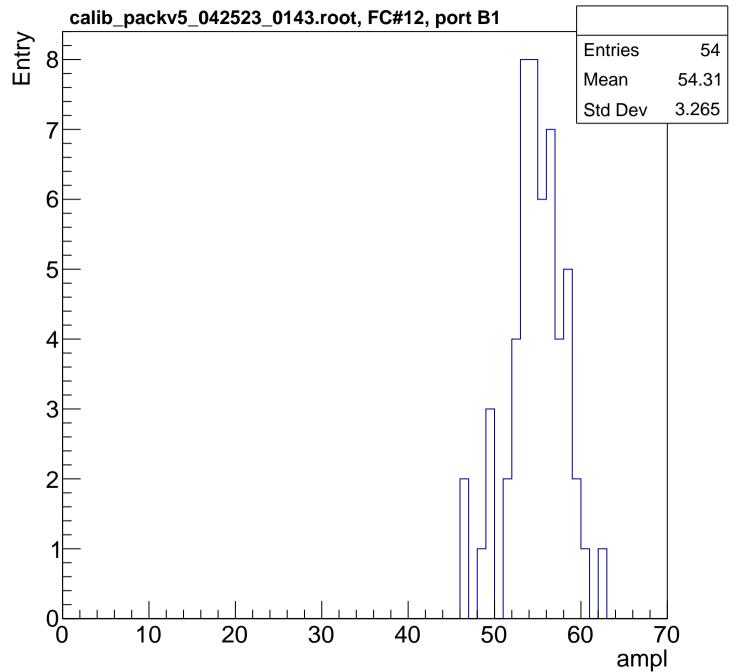


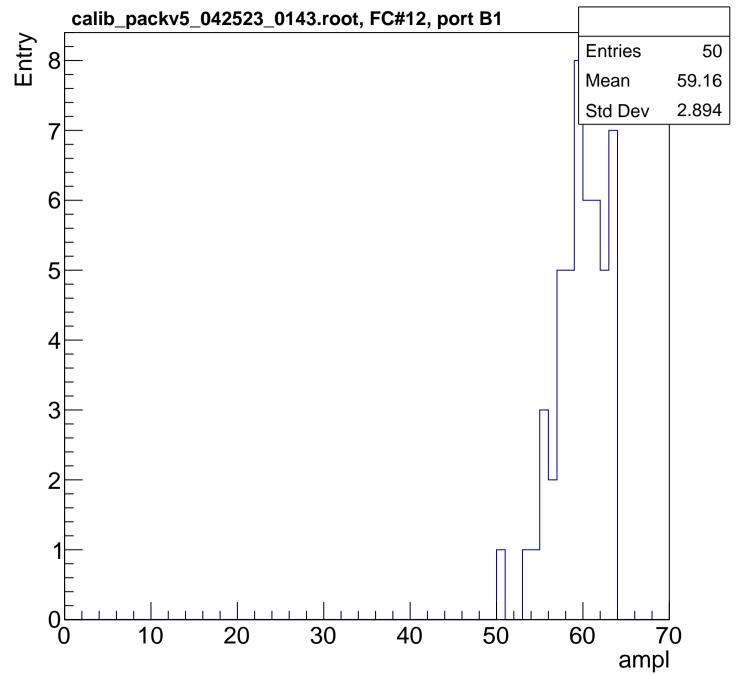


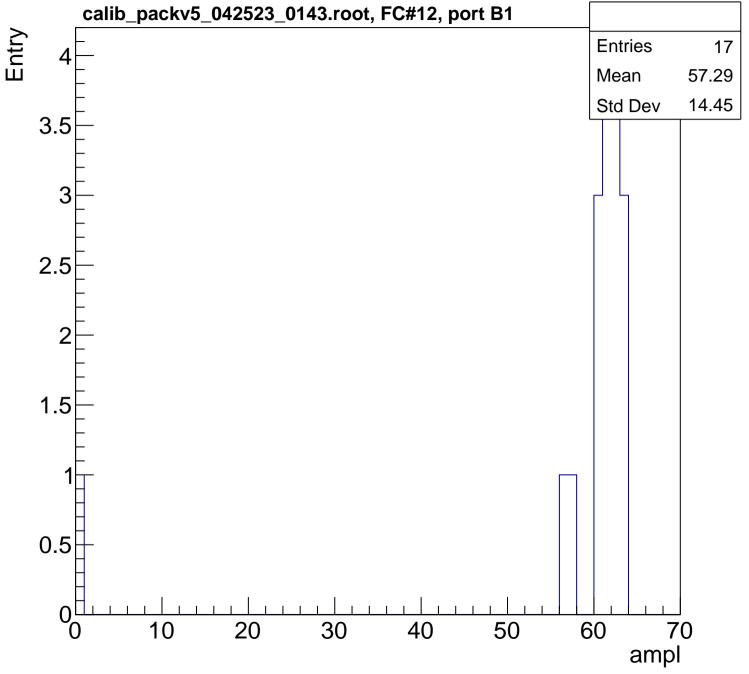


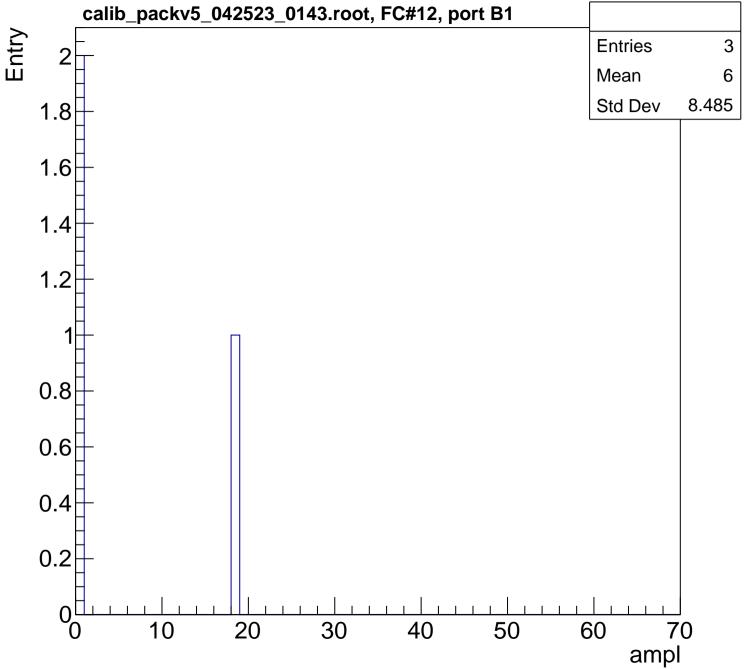


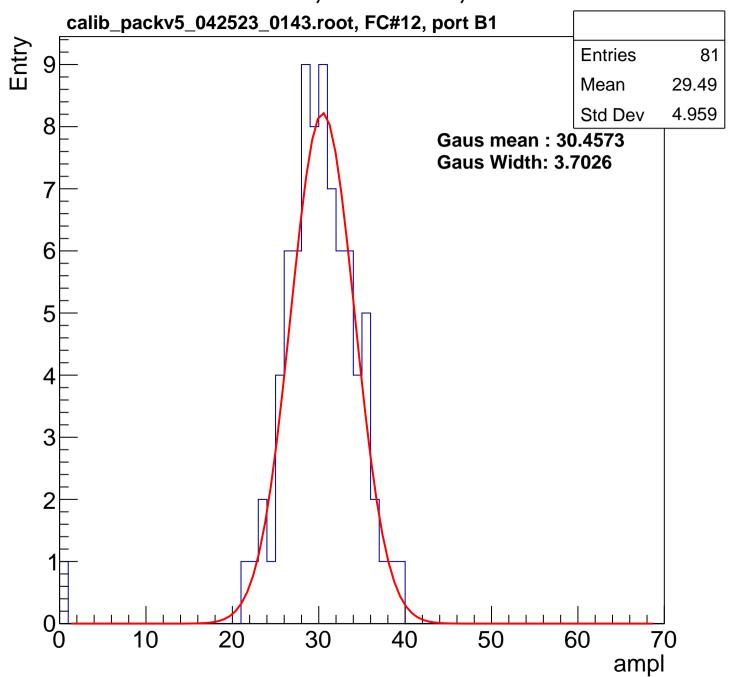


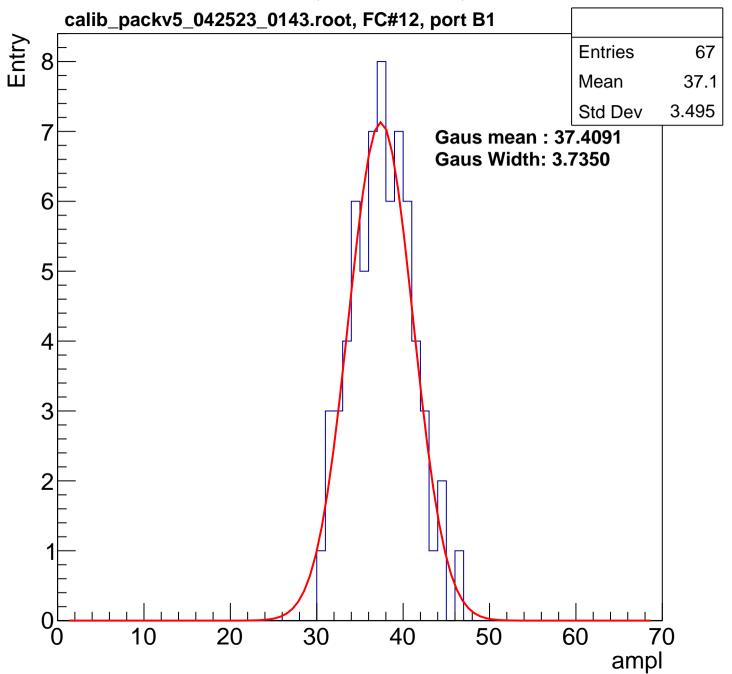


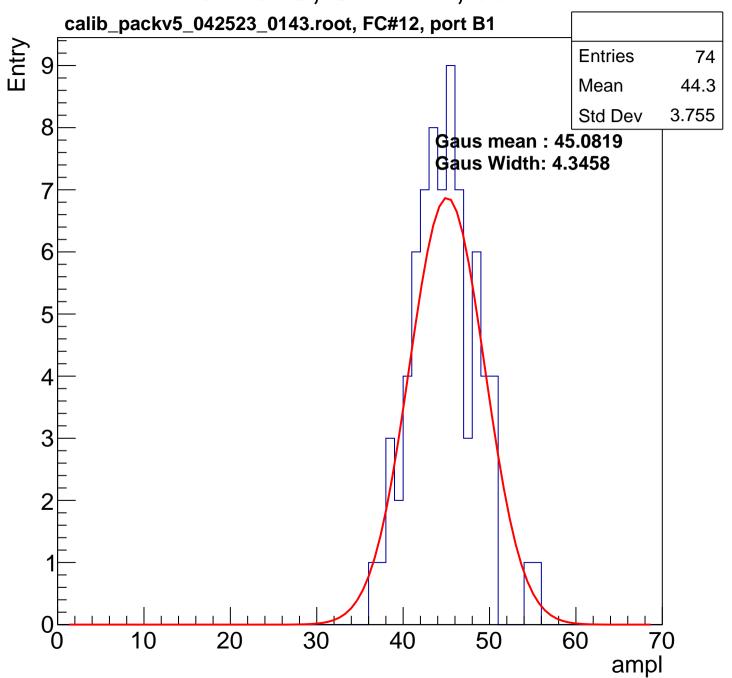


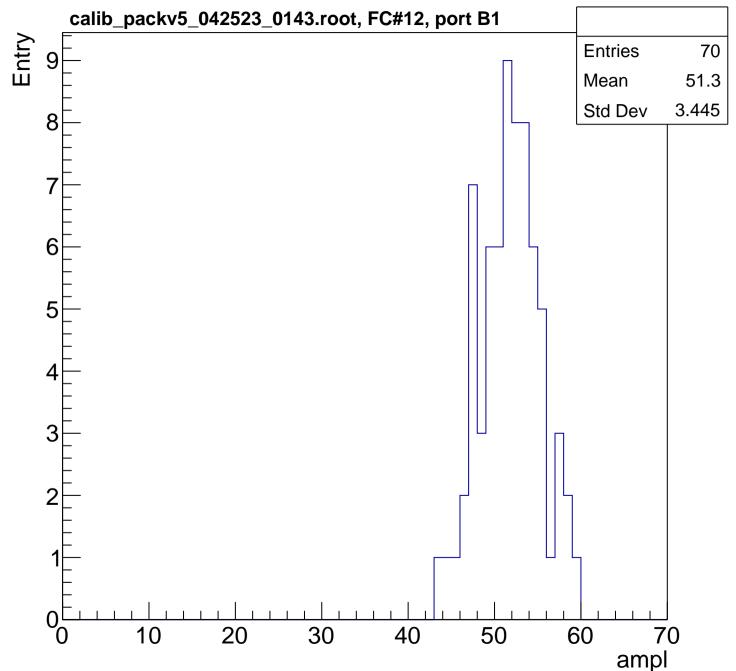


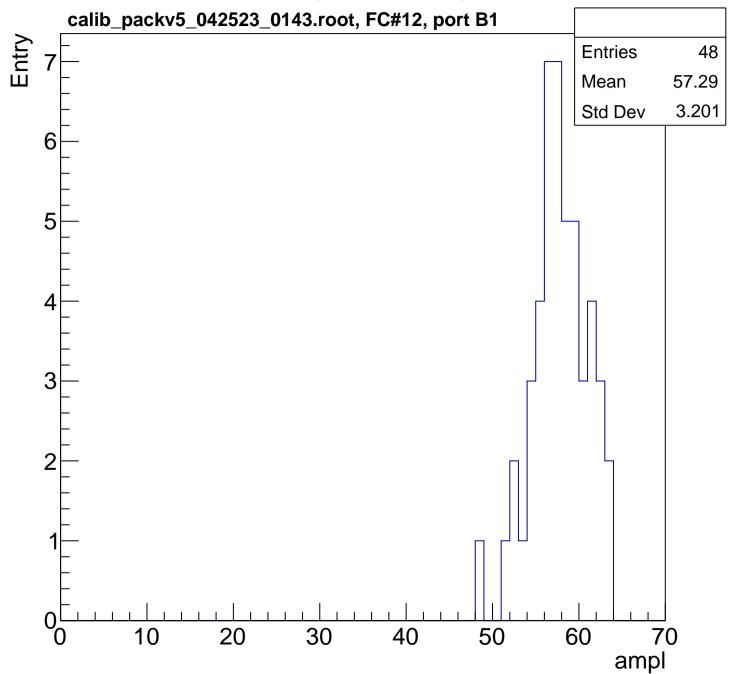


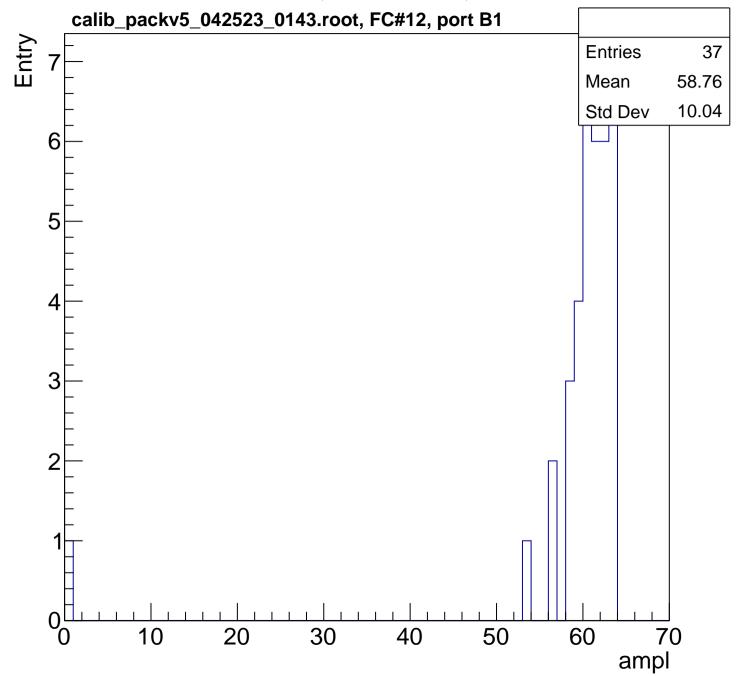


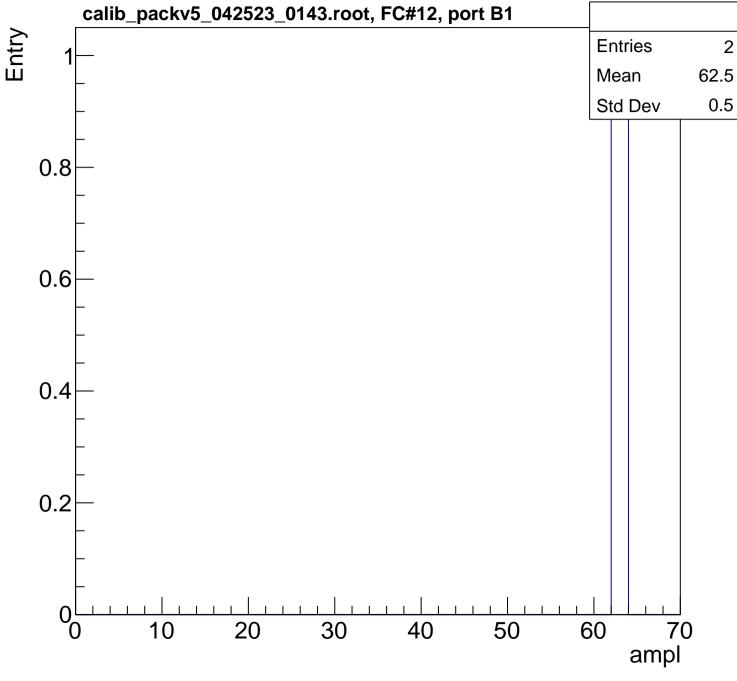


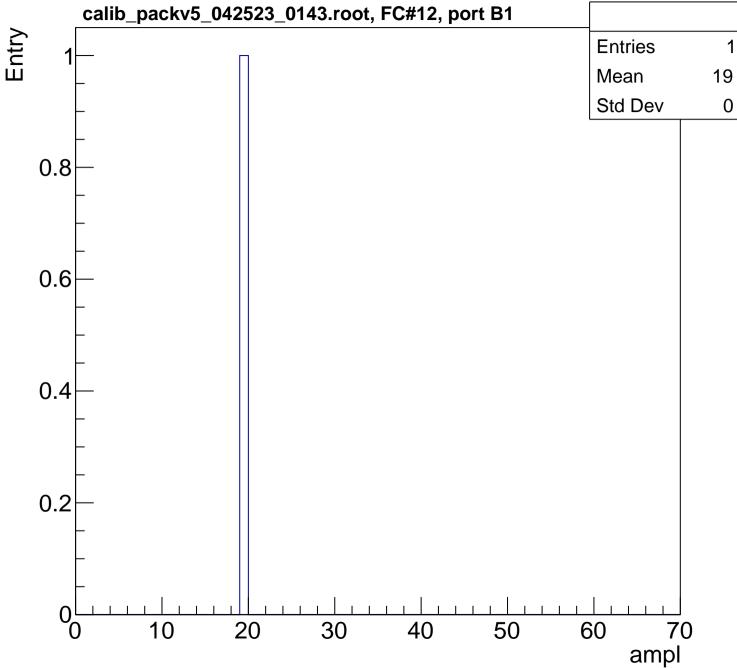


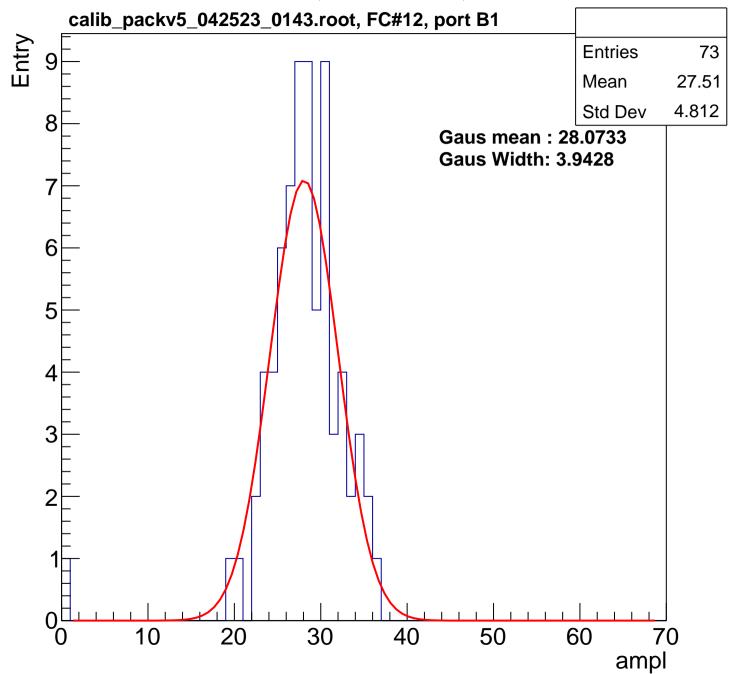


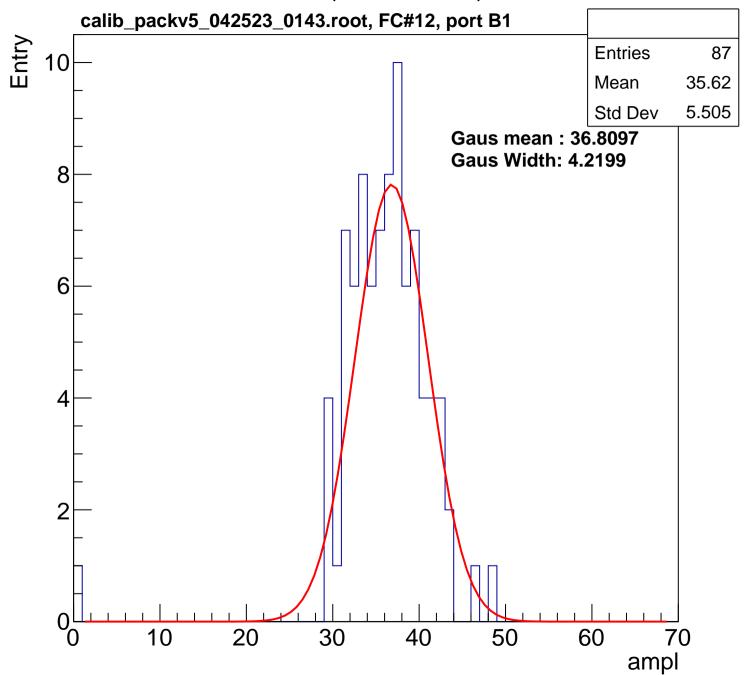


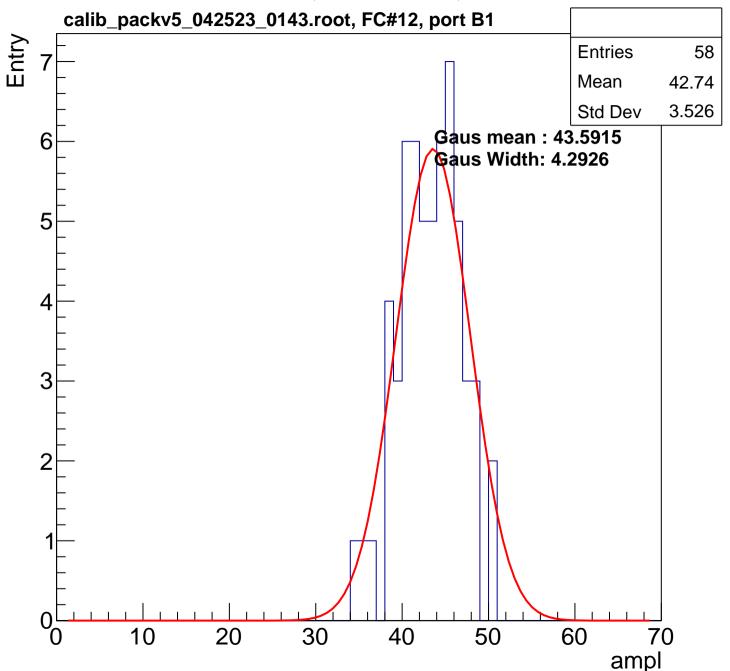


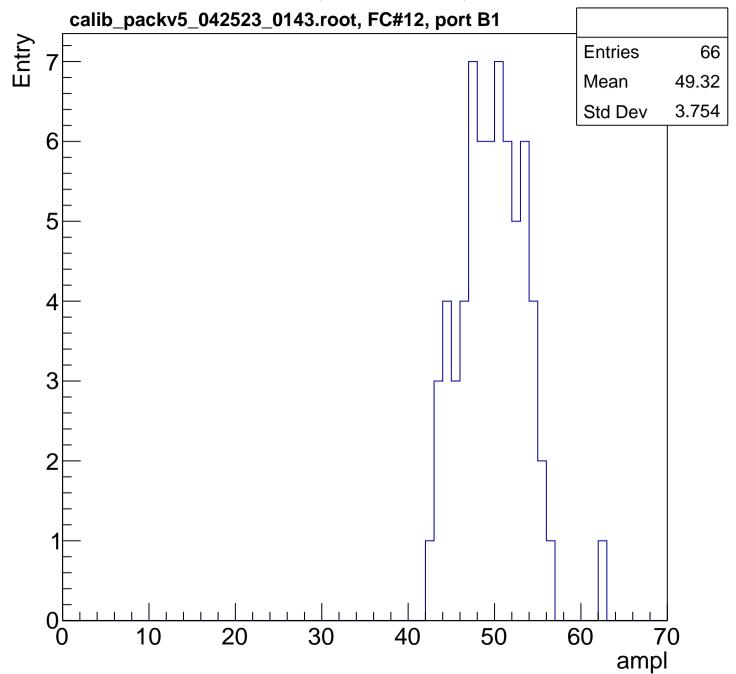


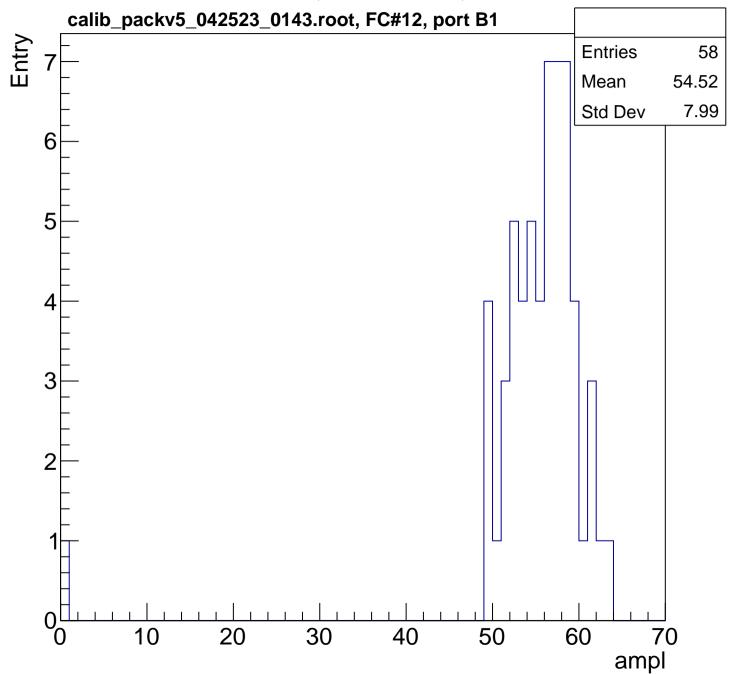


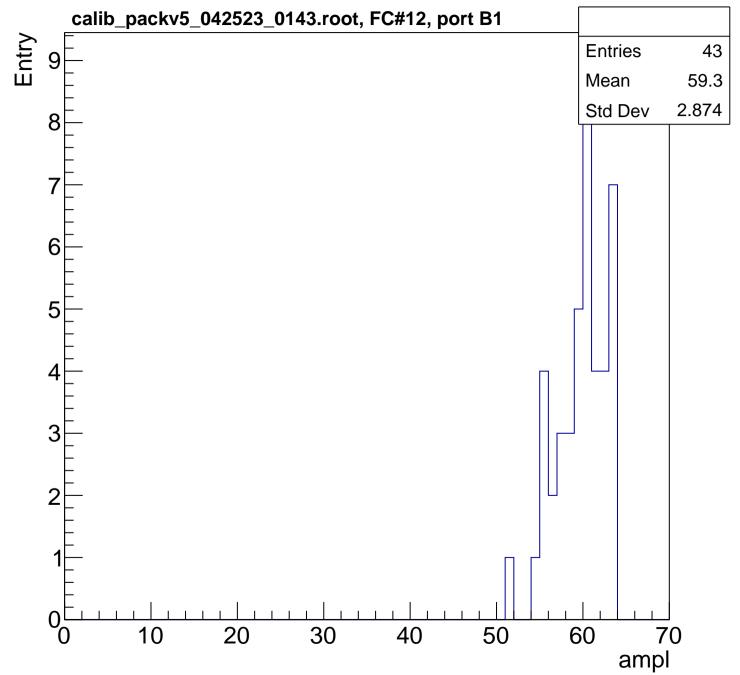


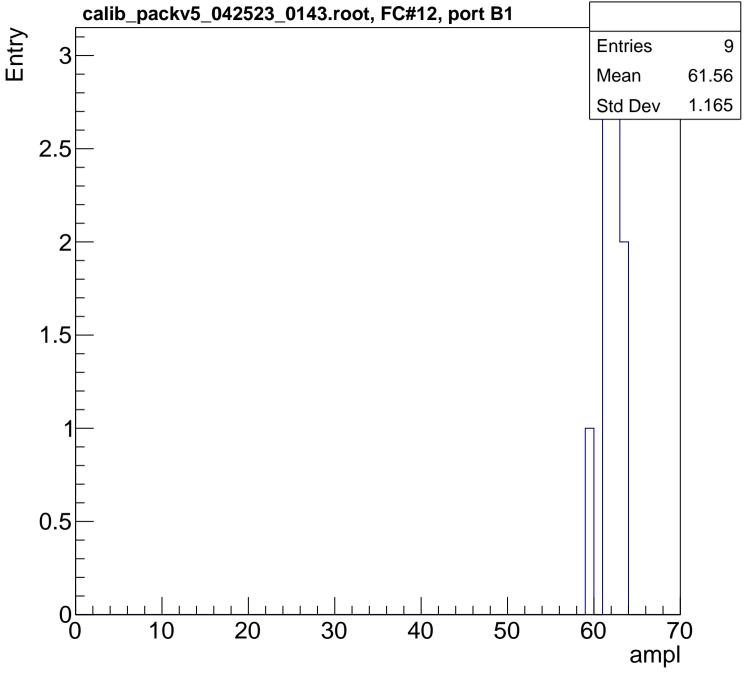




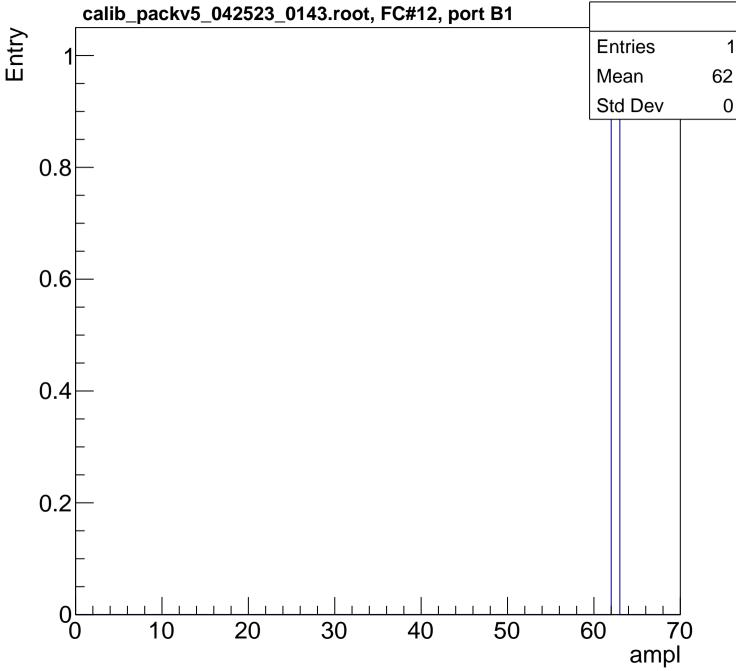


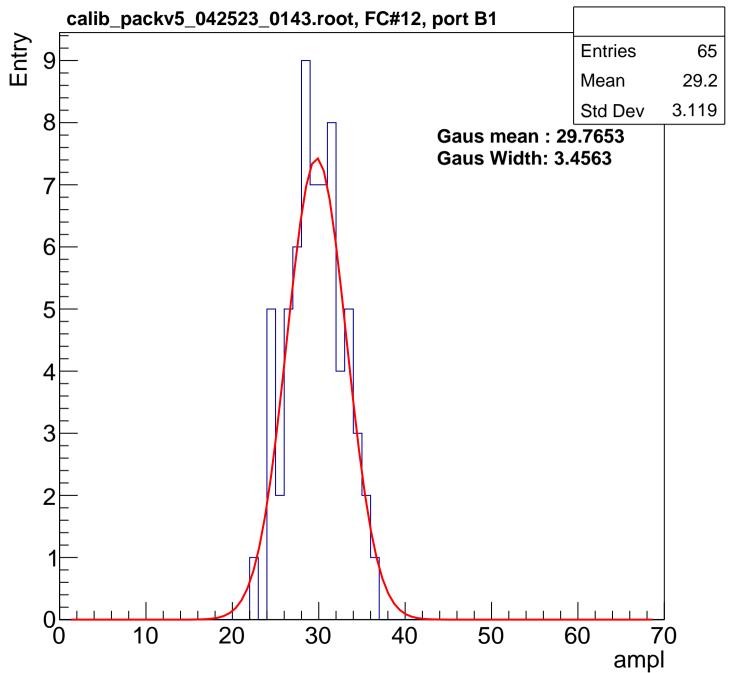


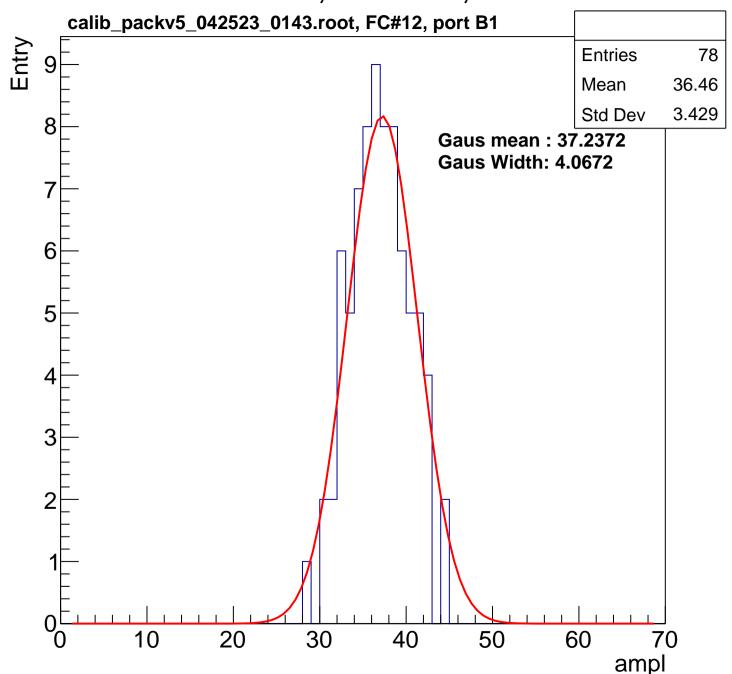


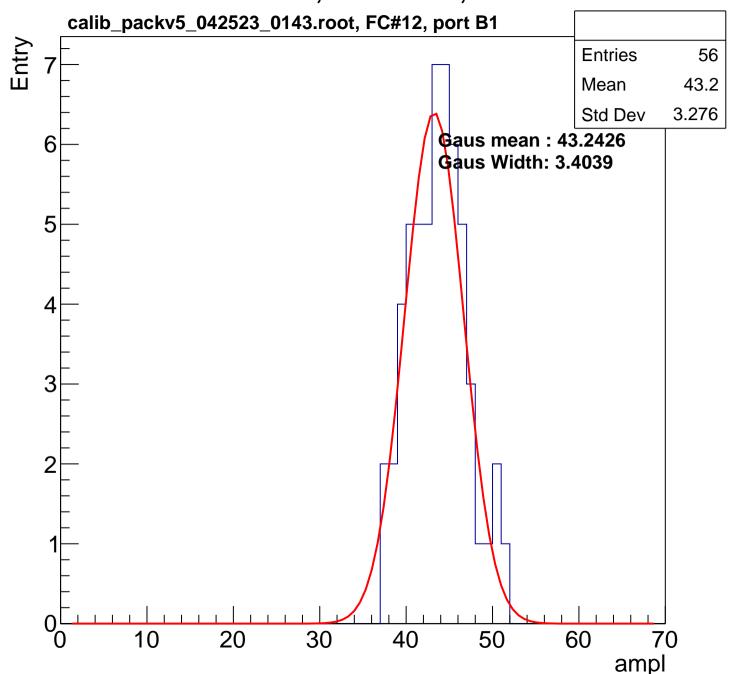


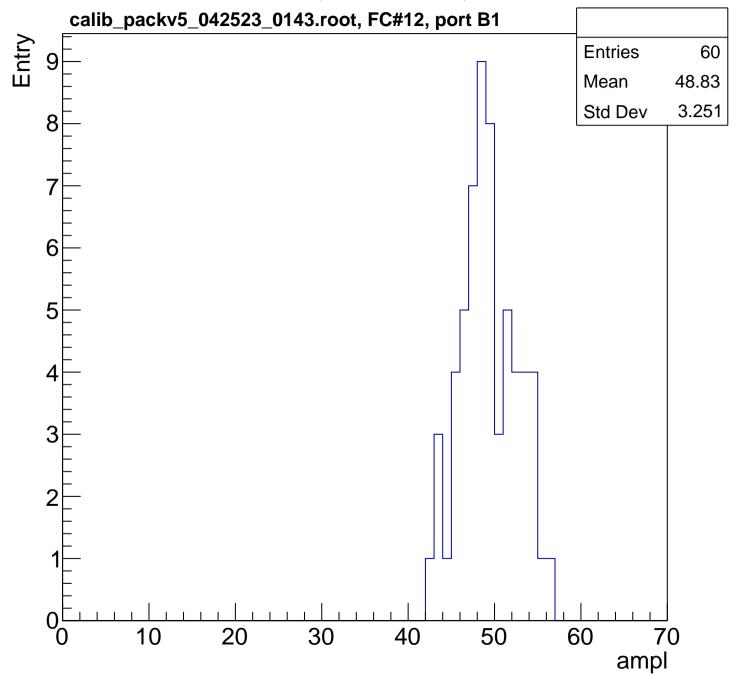
0

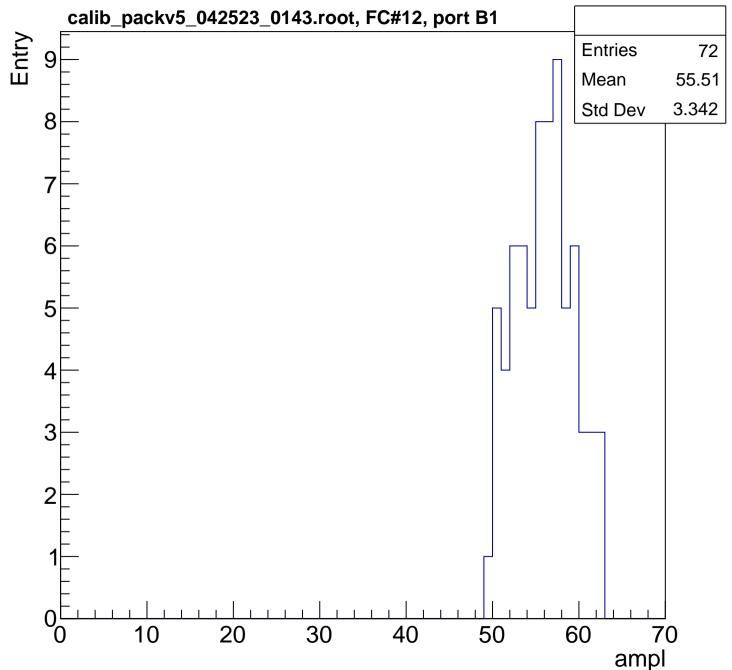


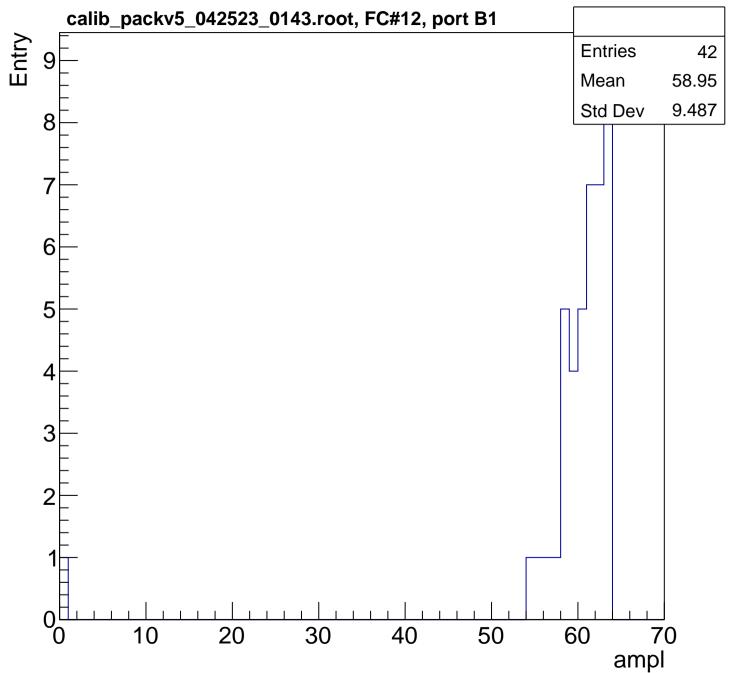


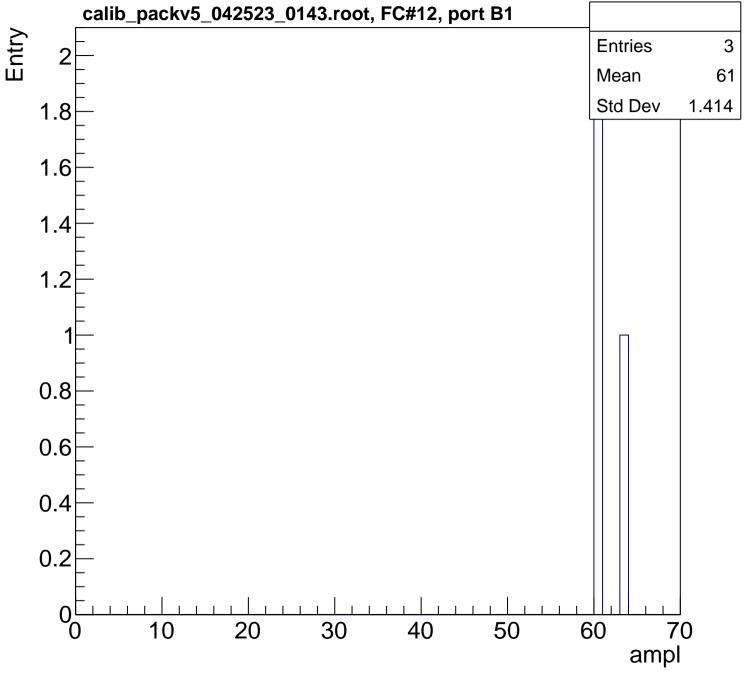


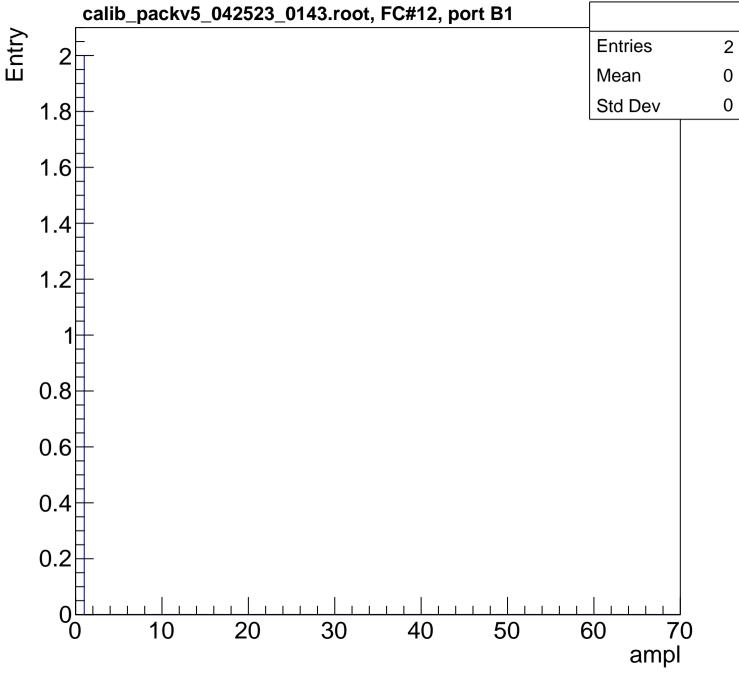


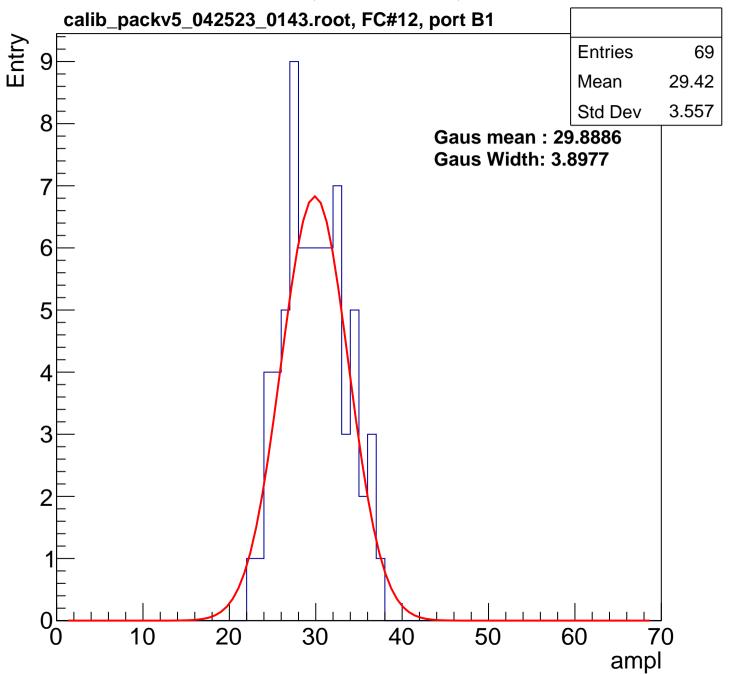


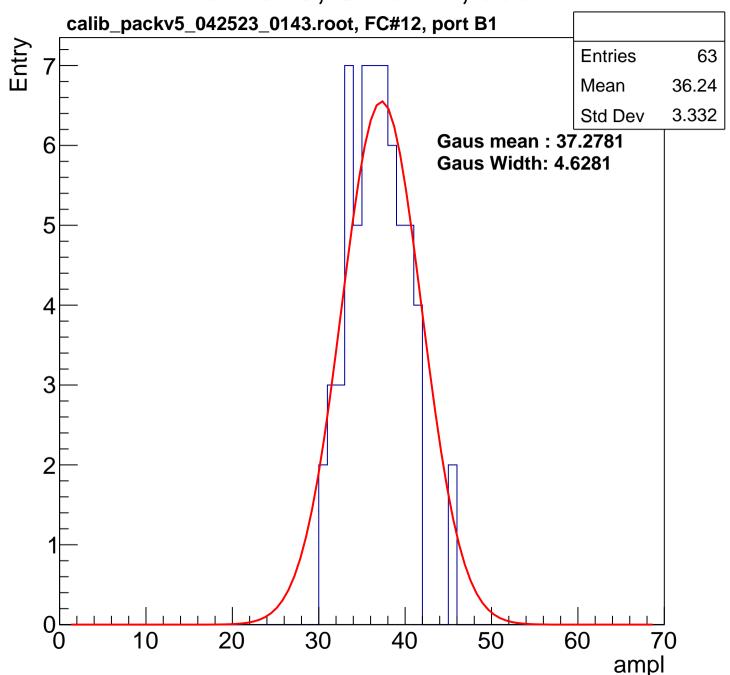


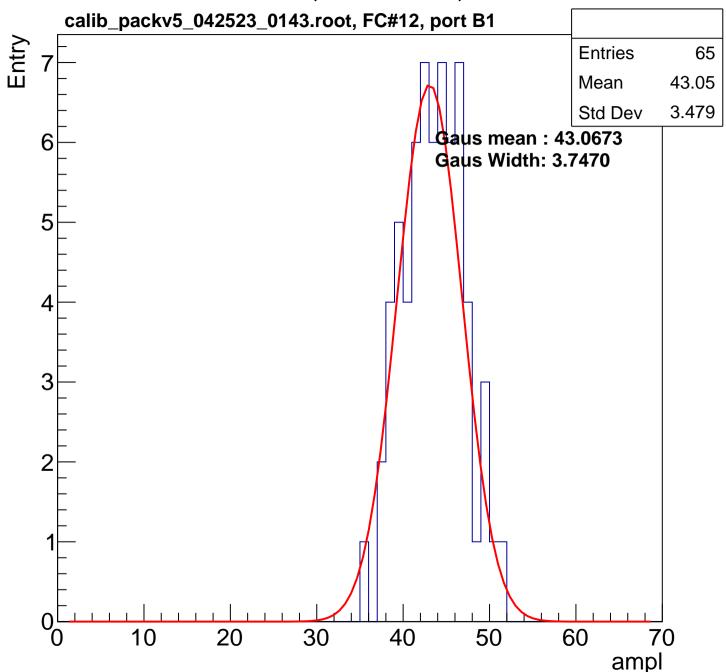


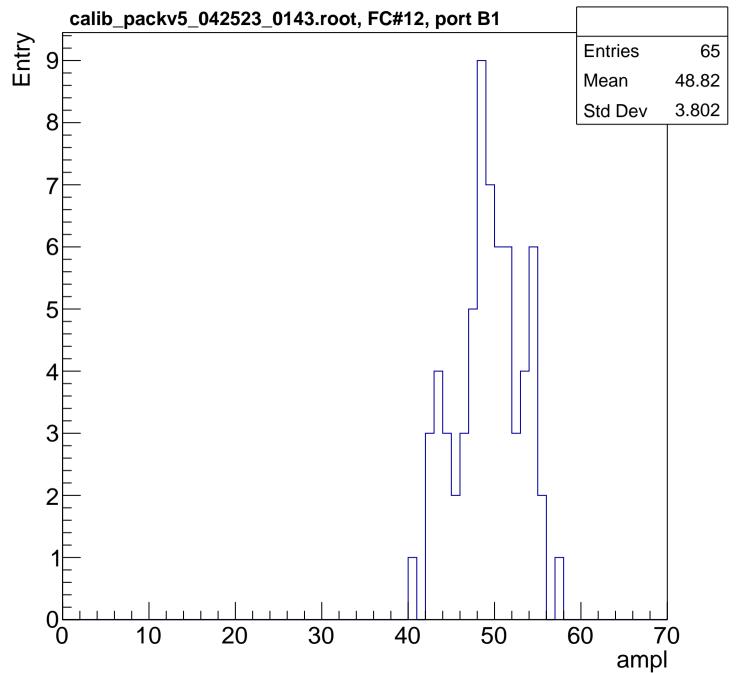


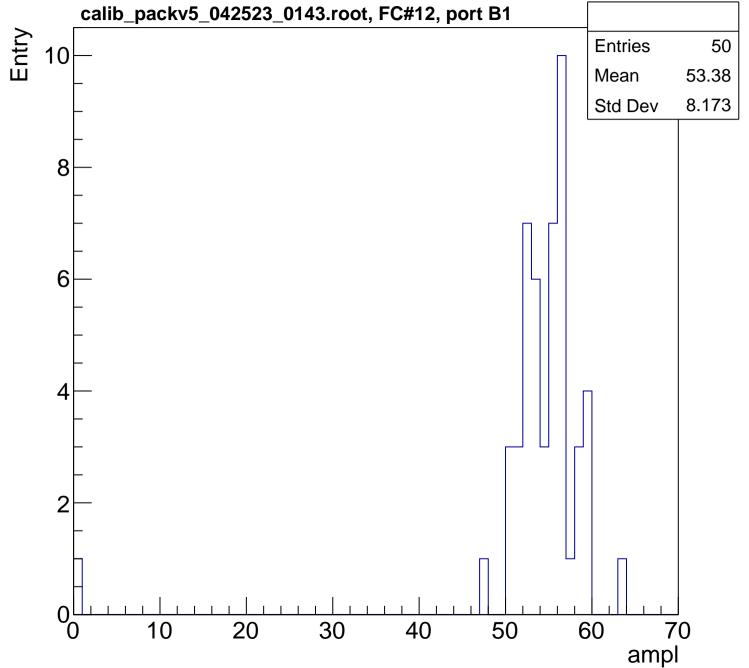


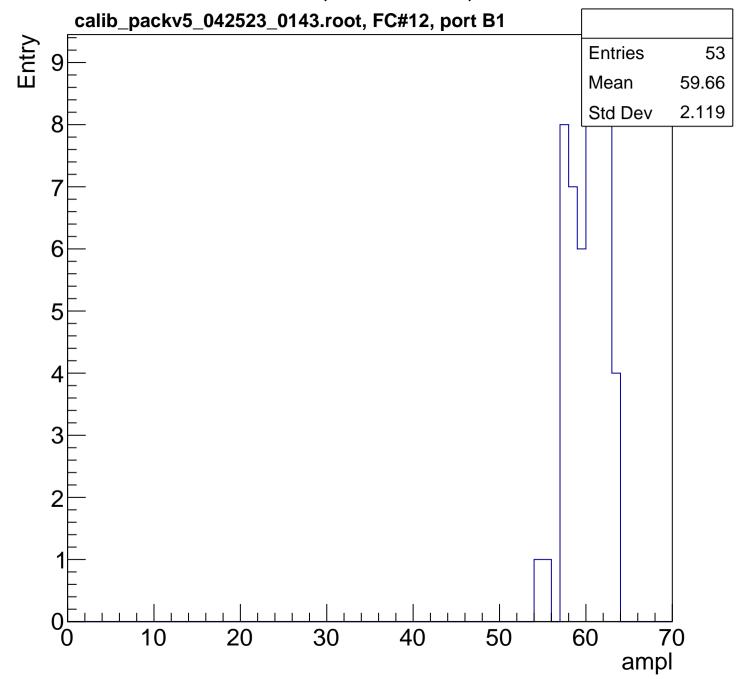


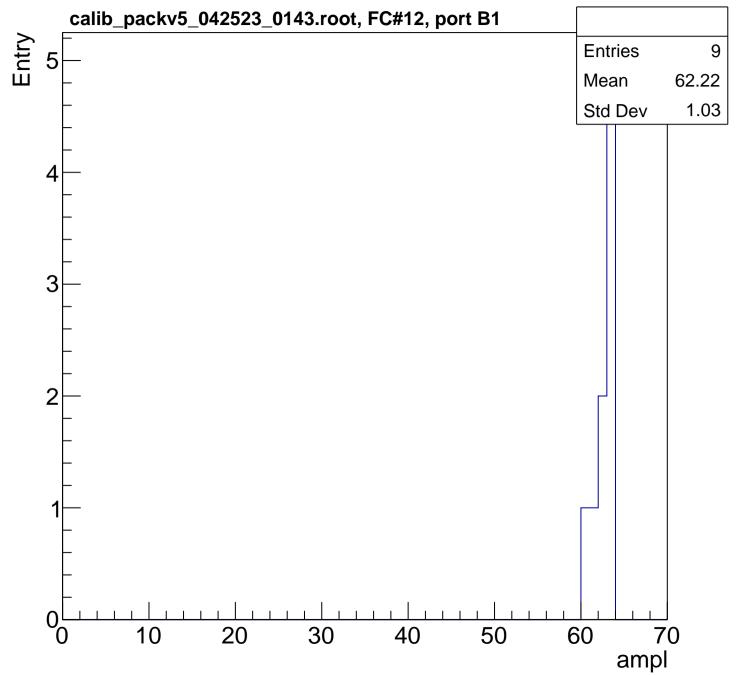




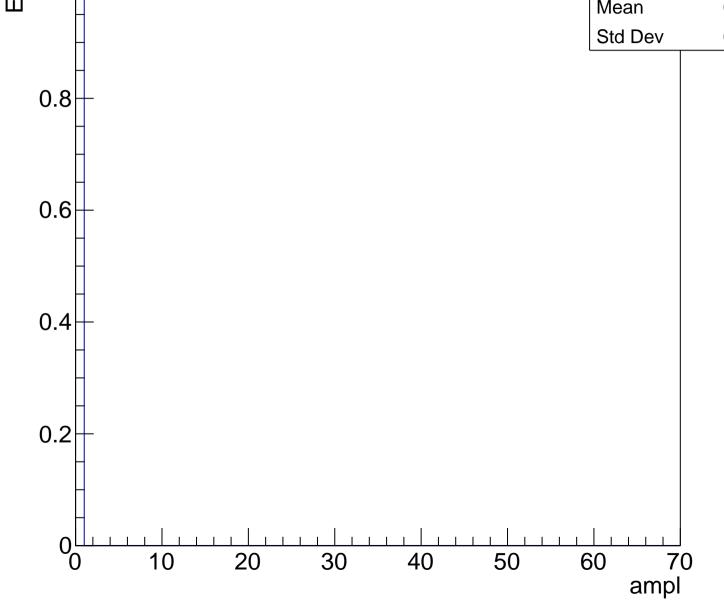


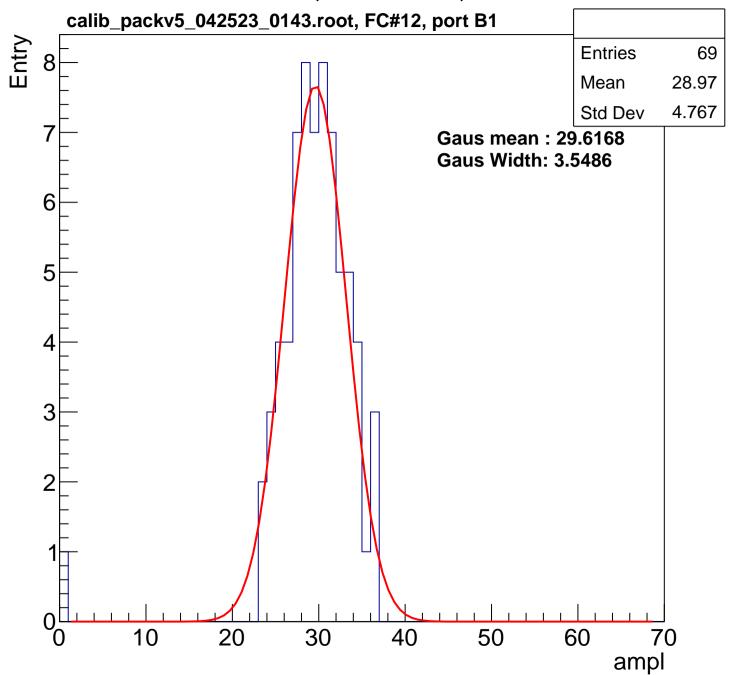


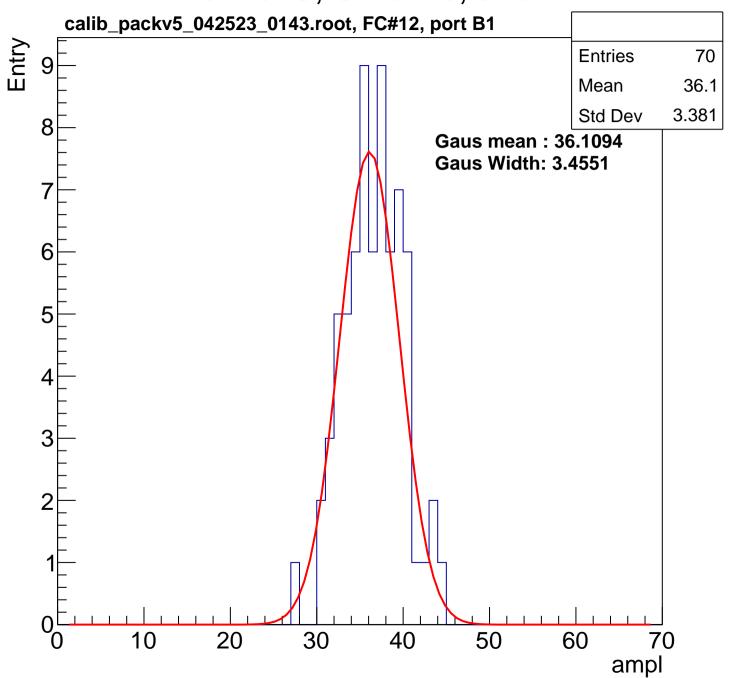


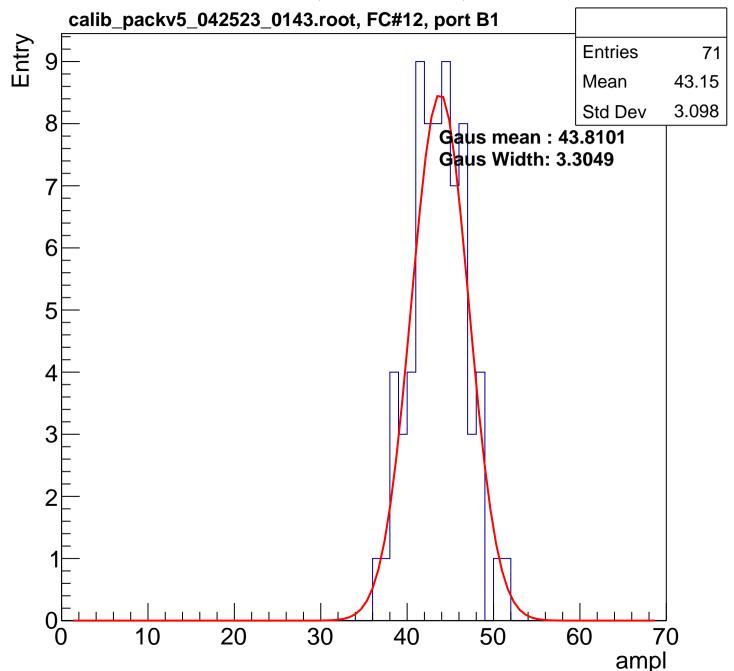


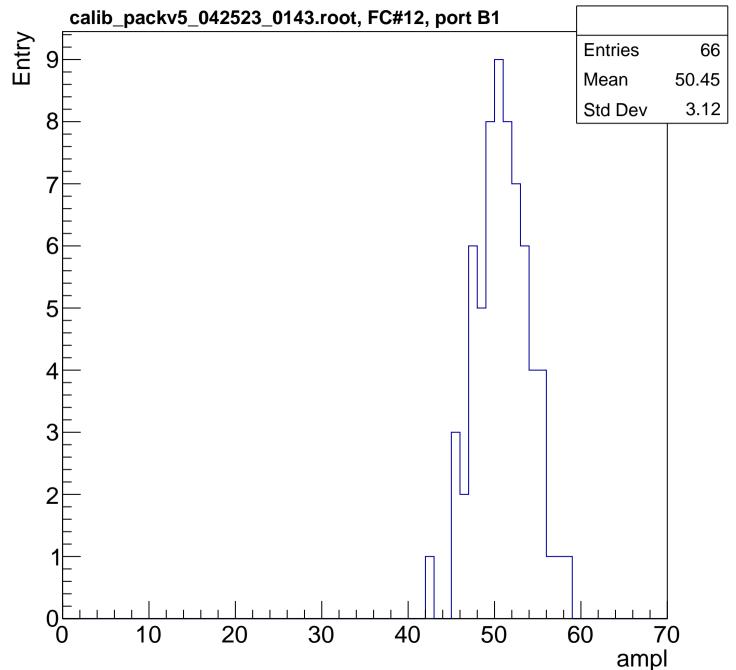
B0L102S, U4-ch24, adc7 calib_packv5_042523_0143.root, FC#12, port B1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4

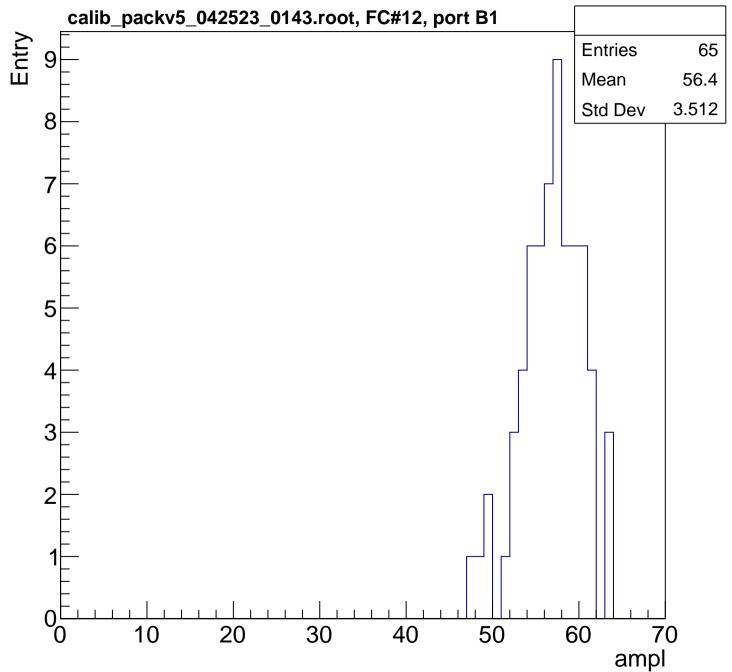


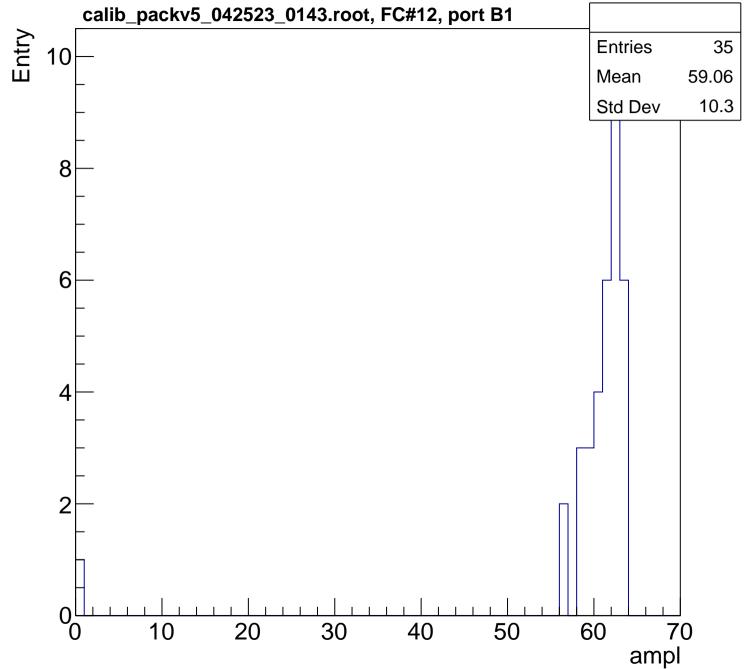


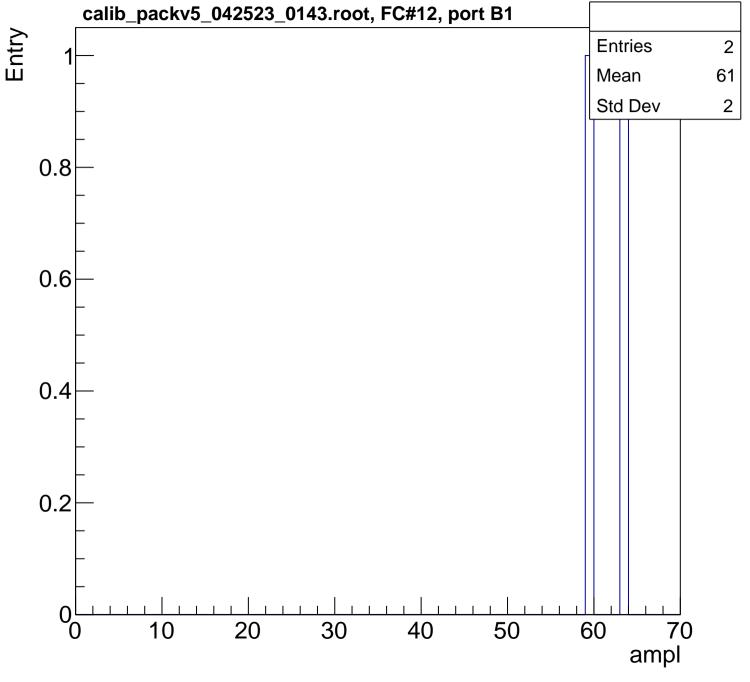


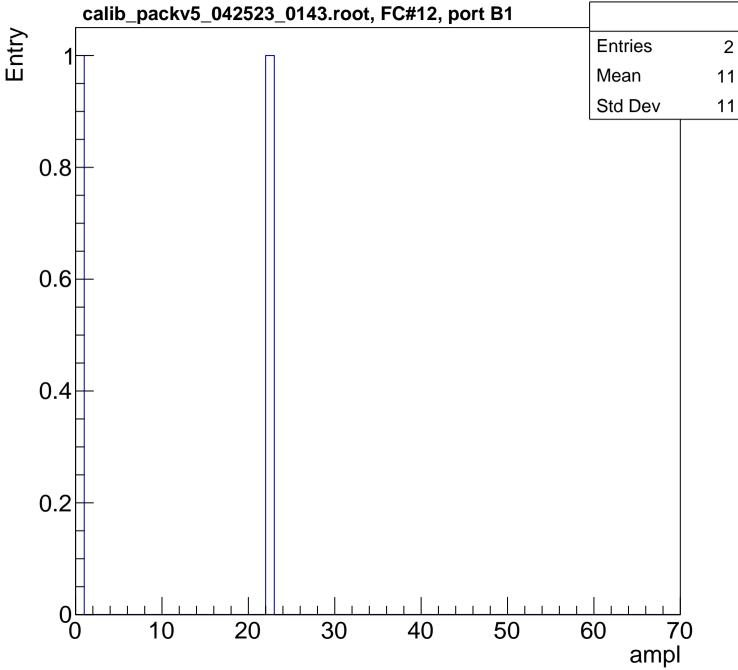


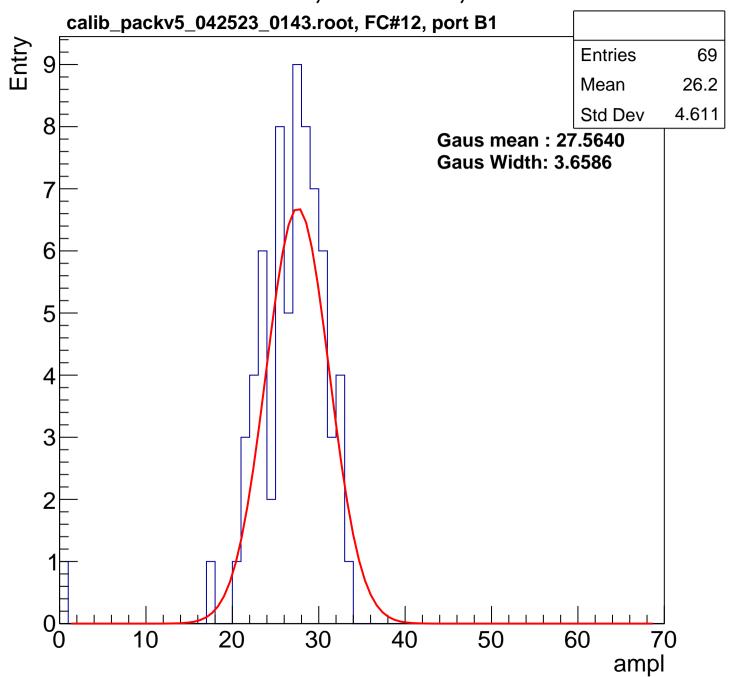


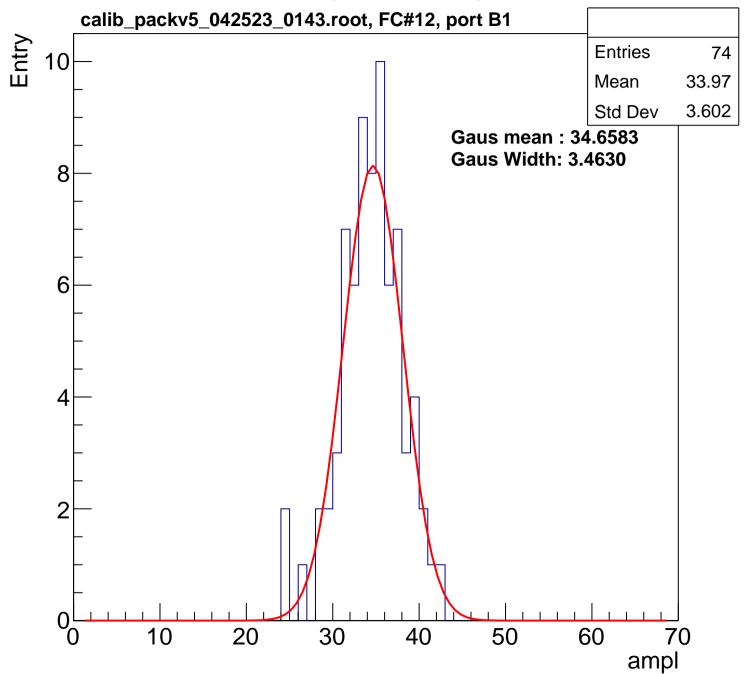


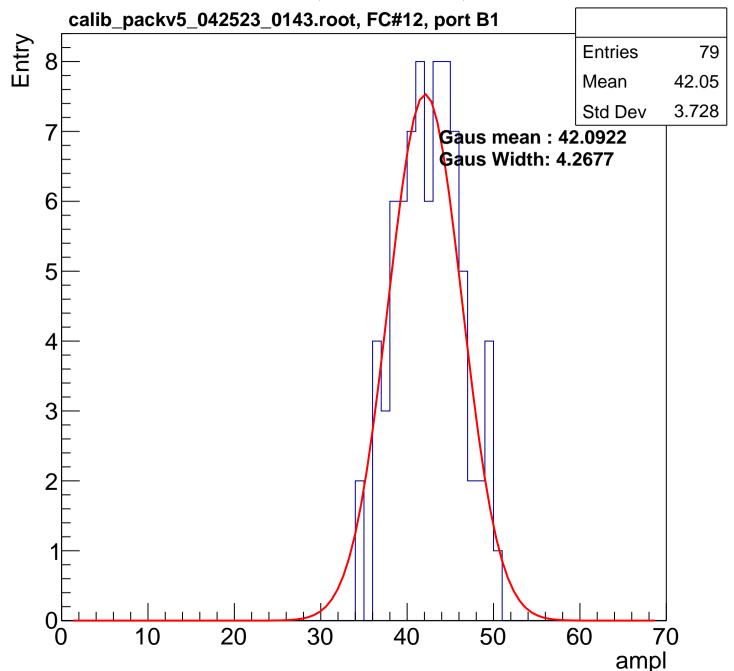


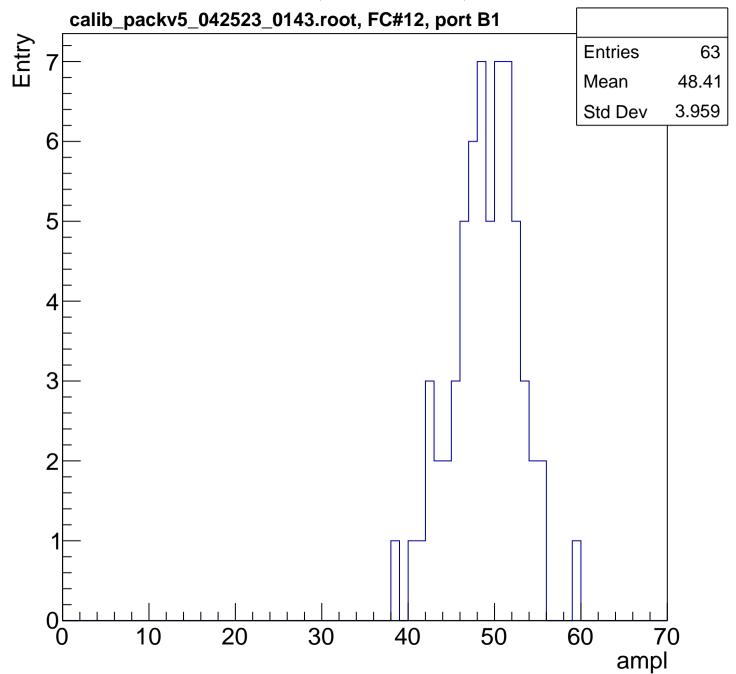


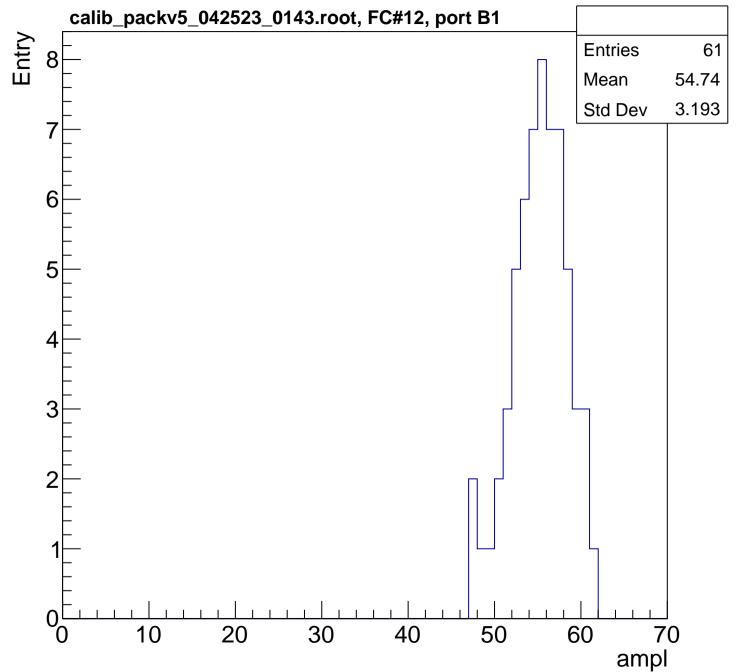


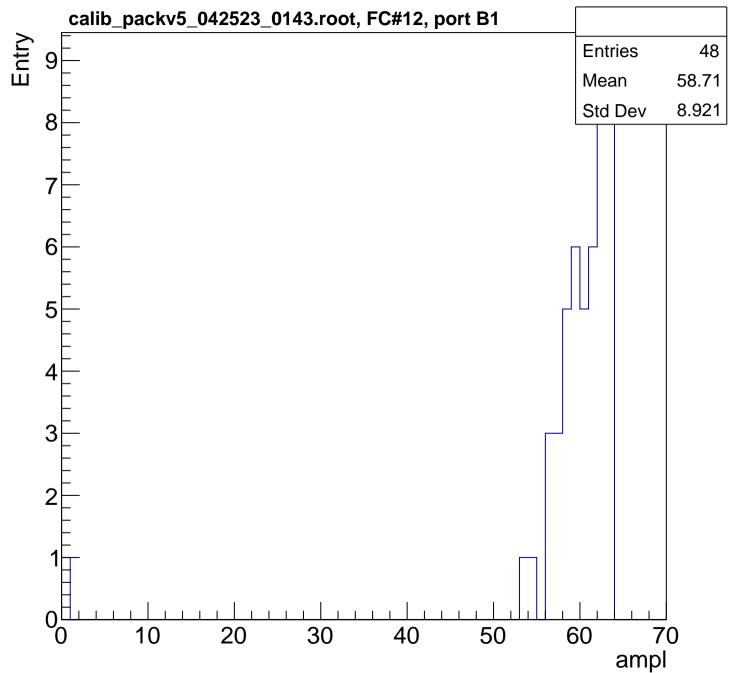


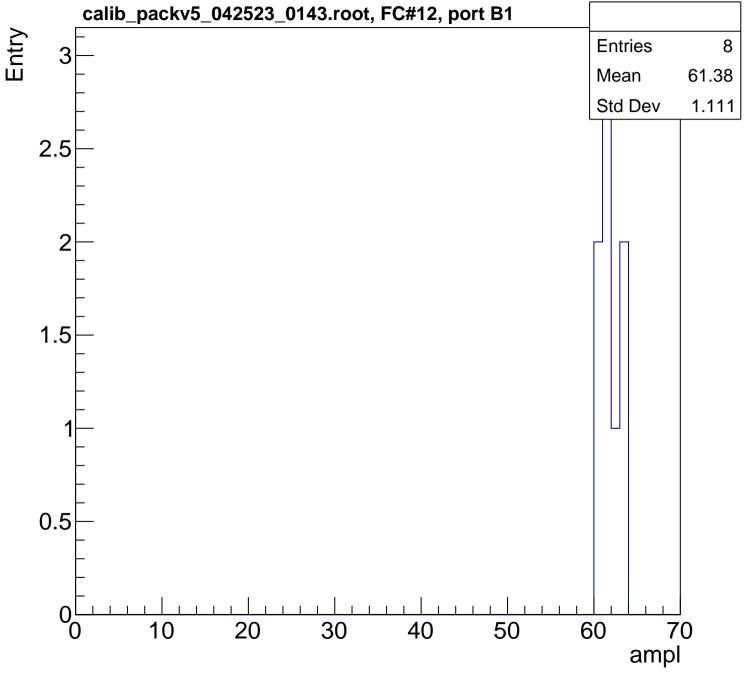


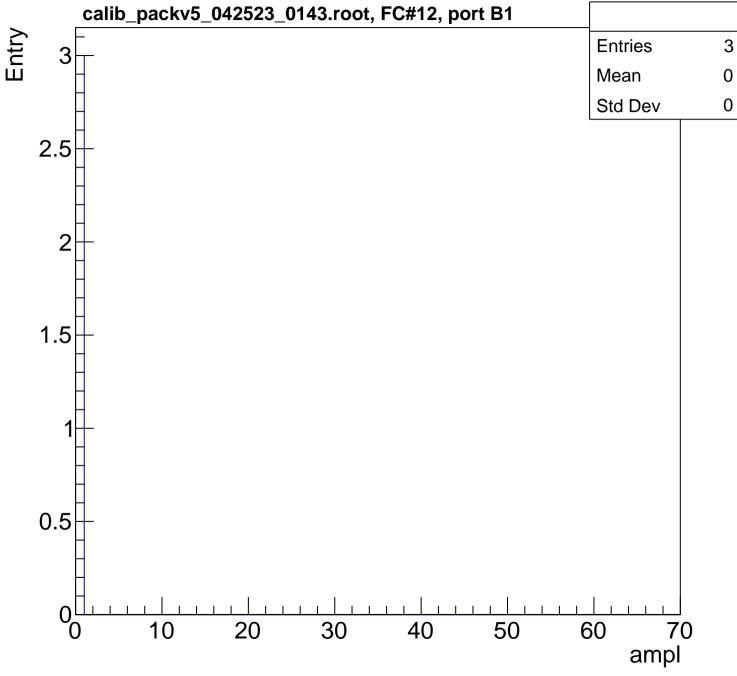


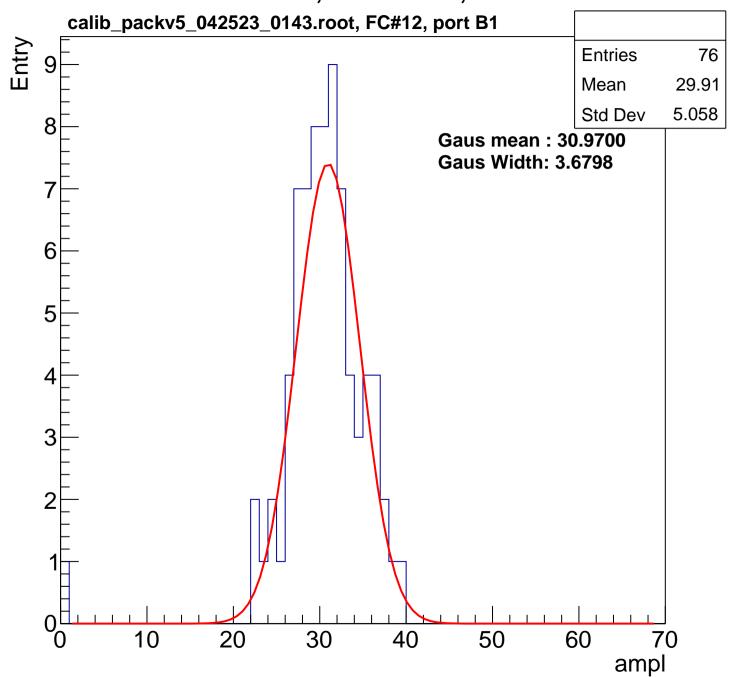


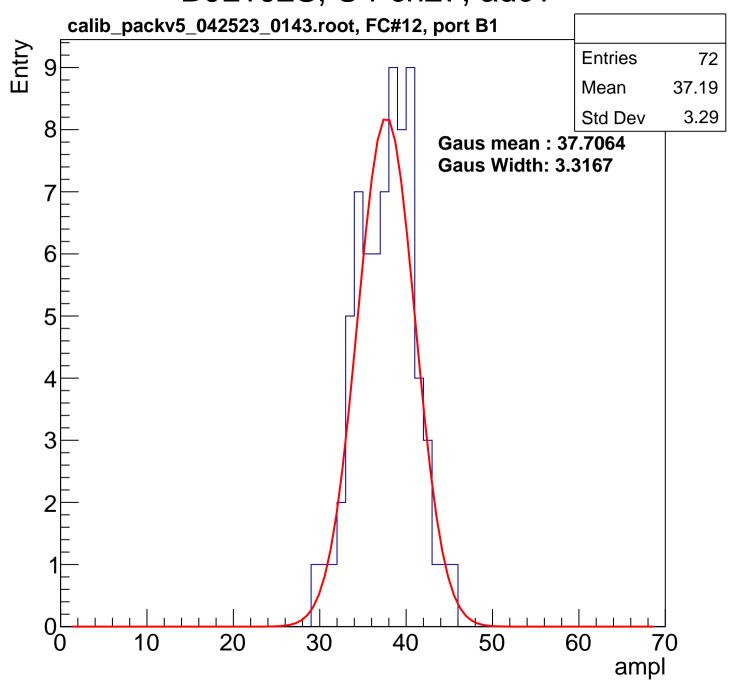


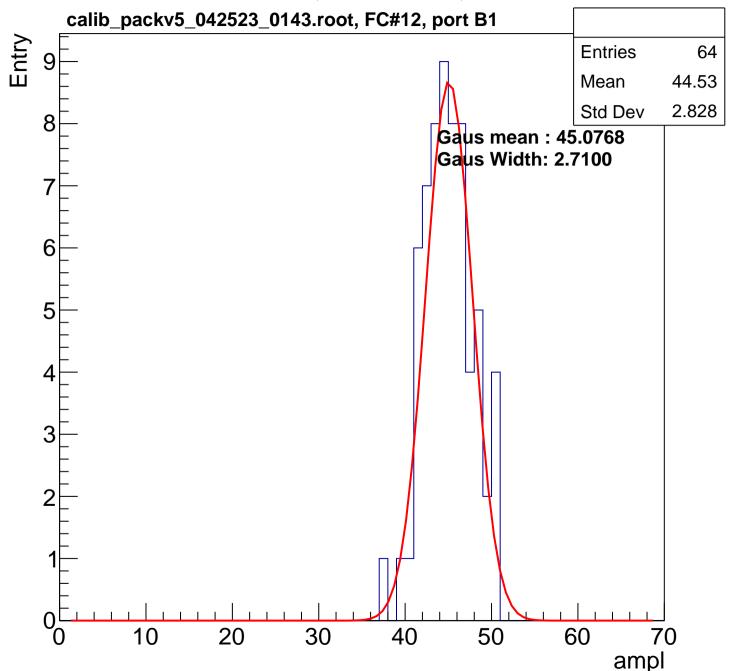


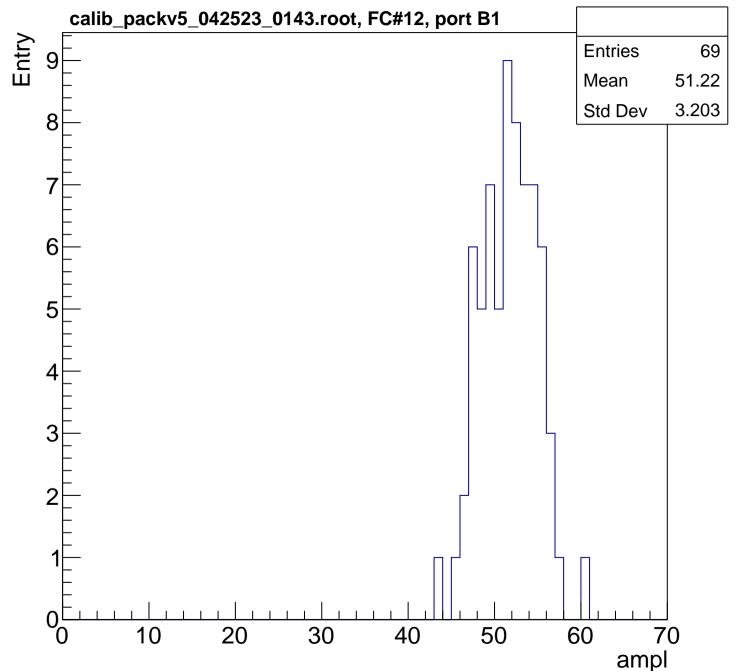


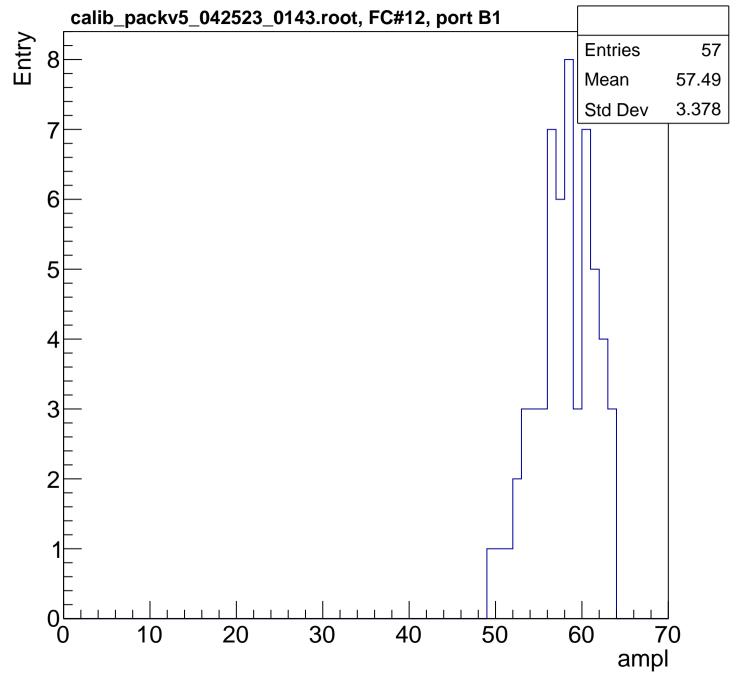


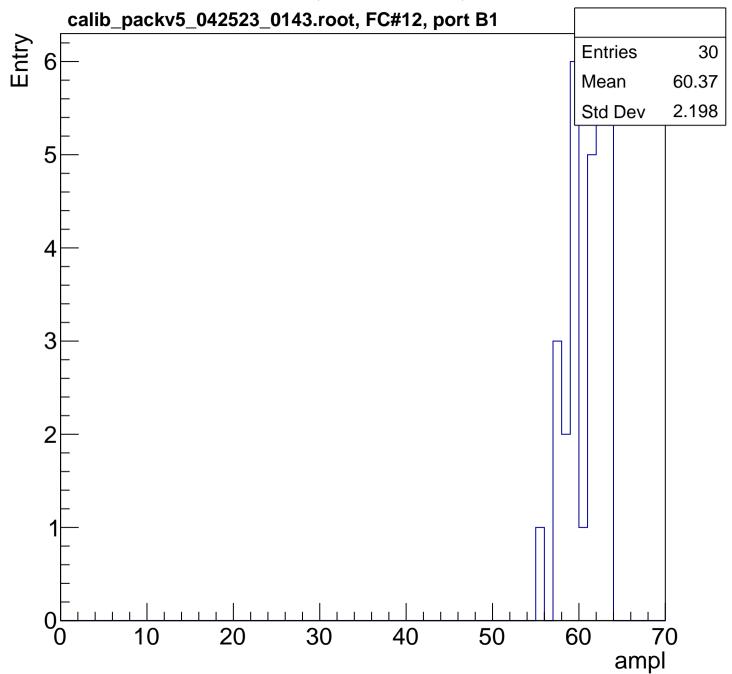


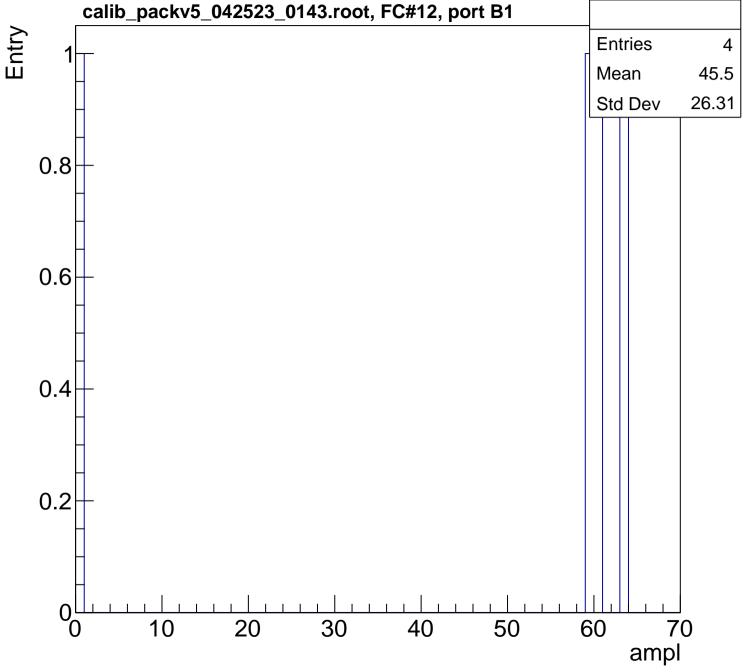




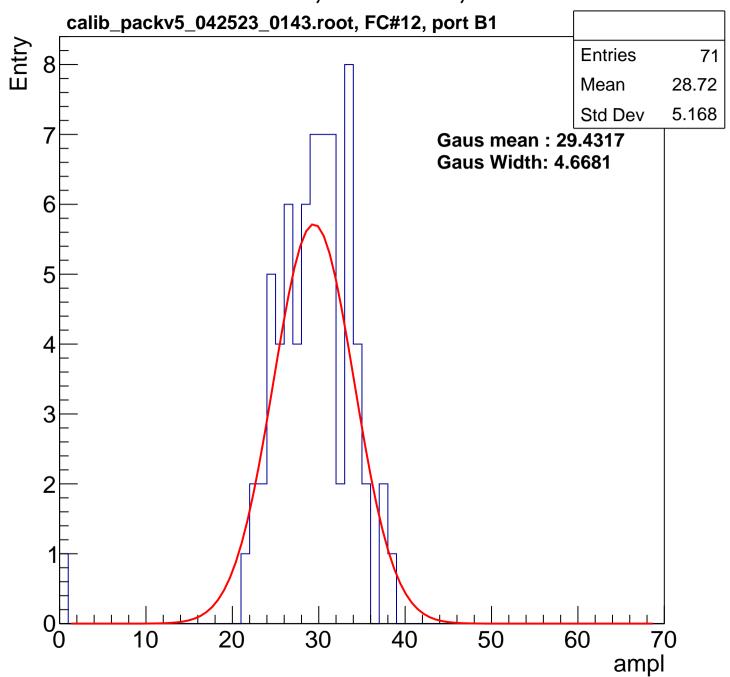


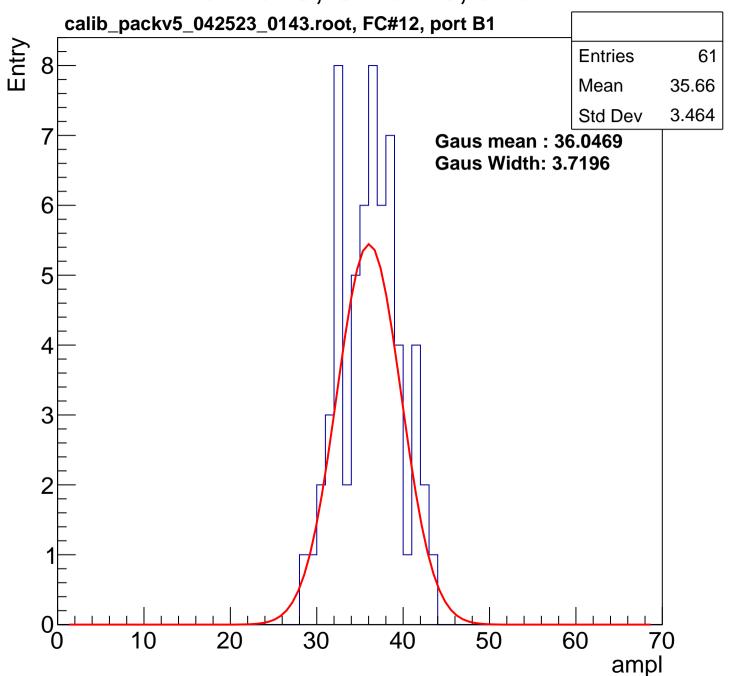


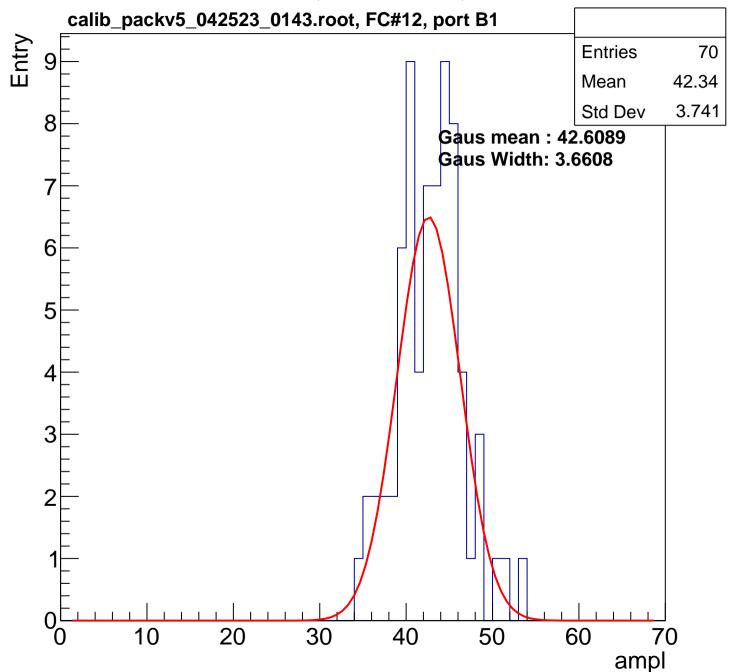


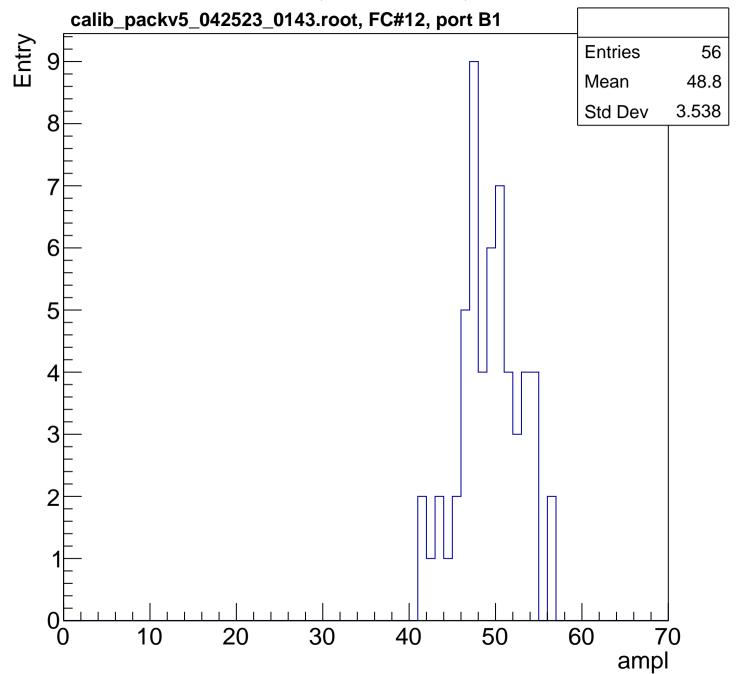


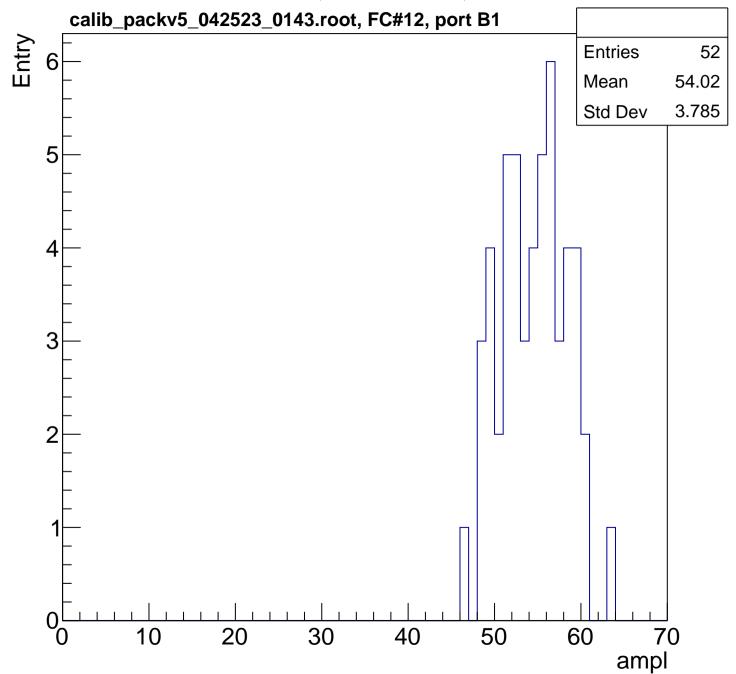


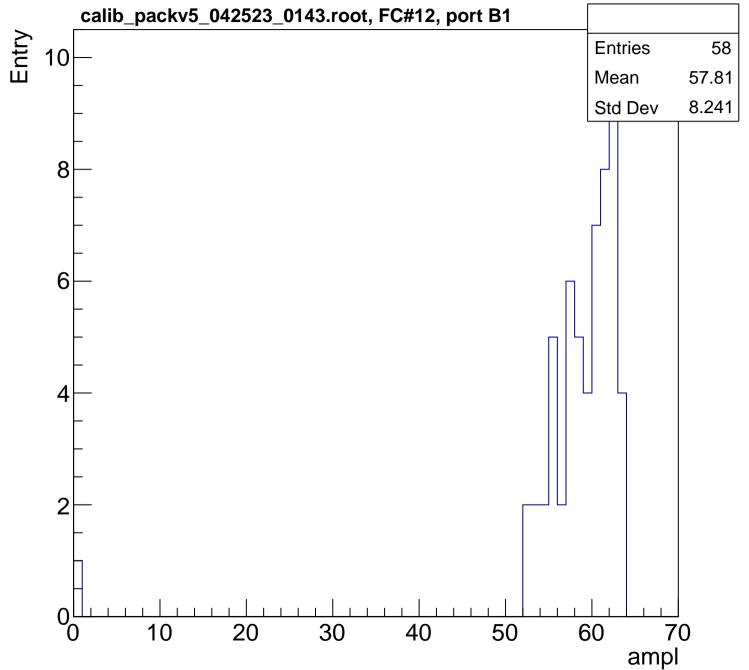


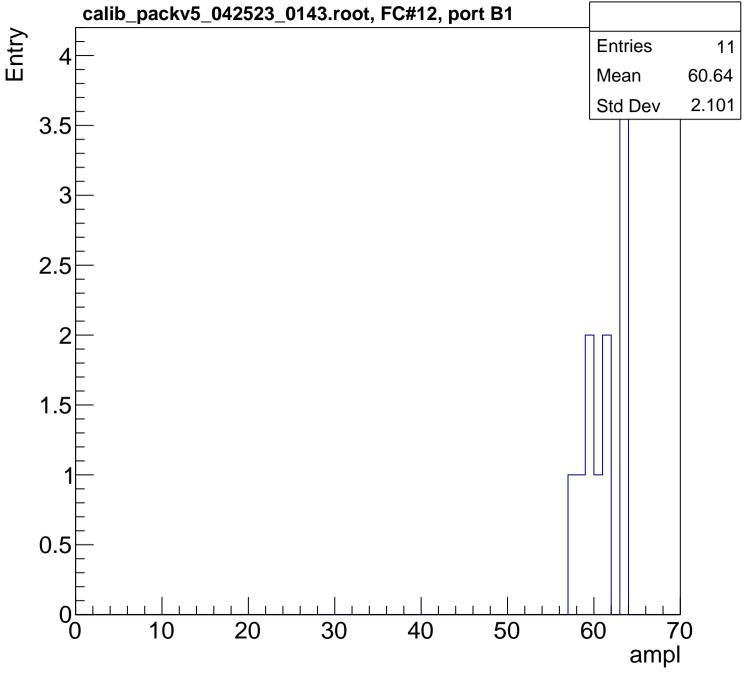


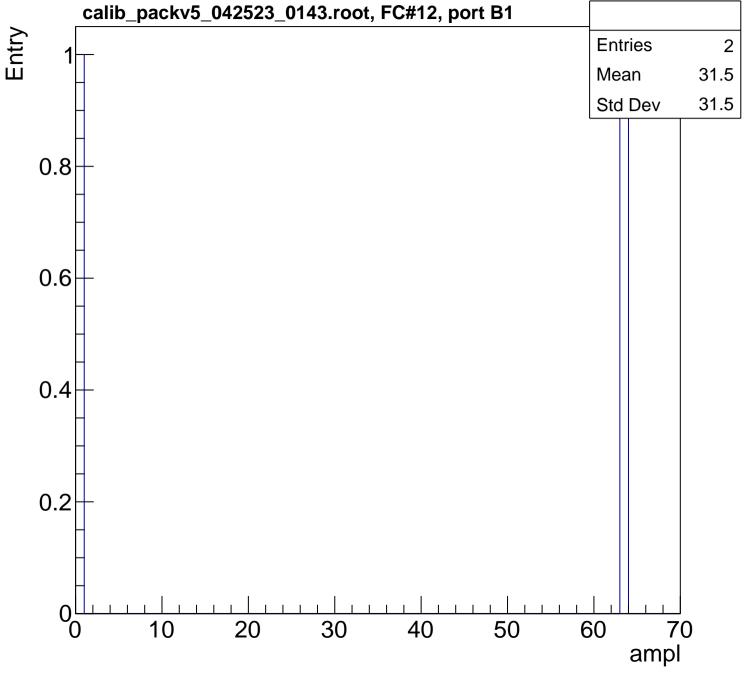


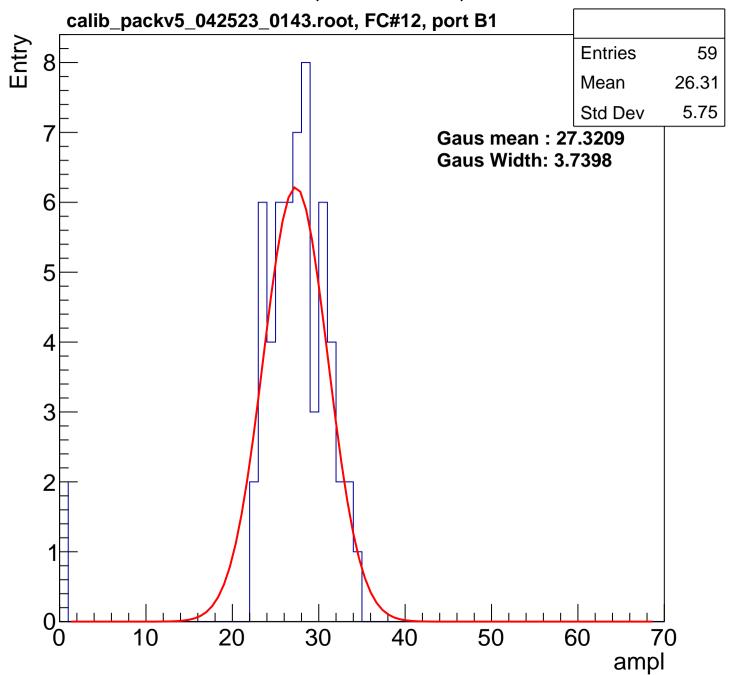


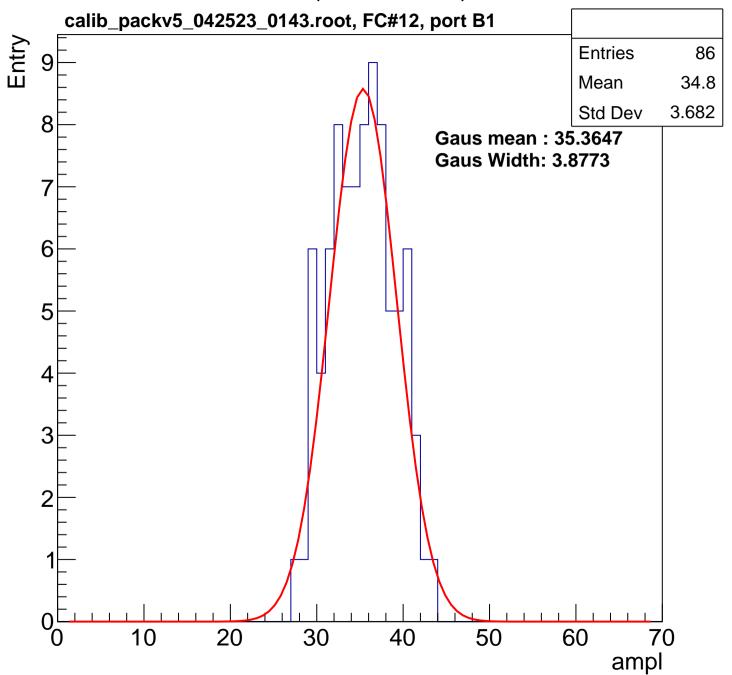


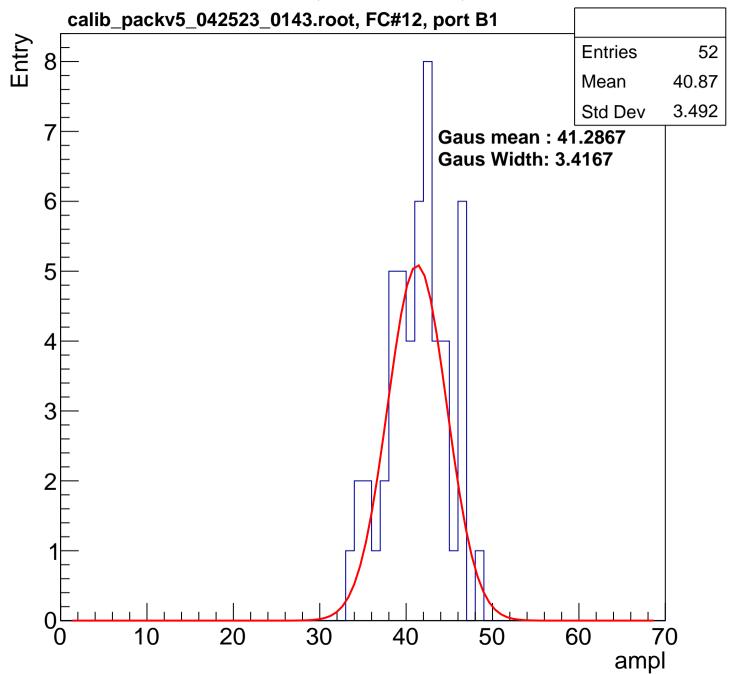


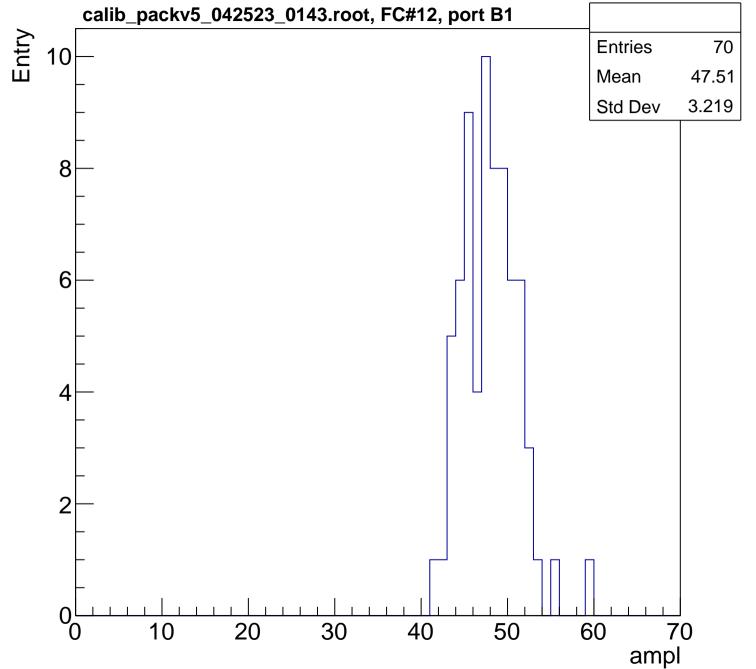


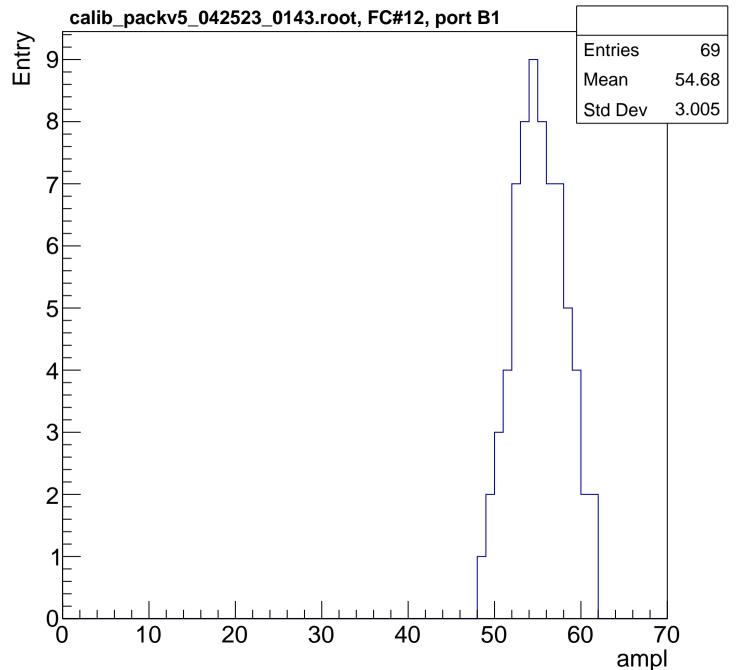


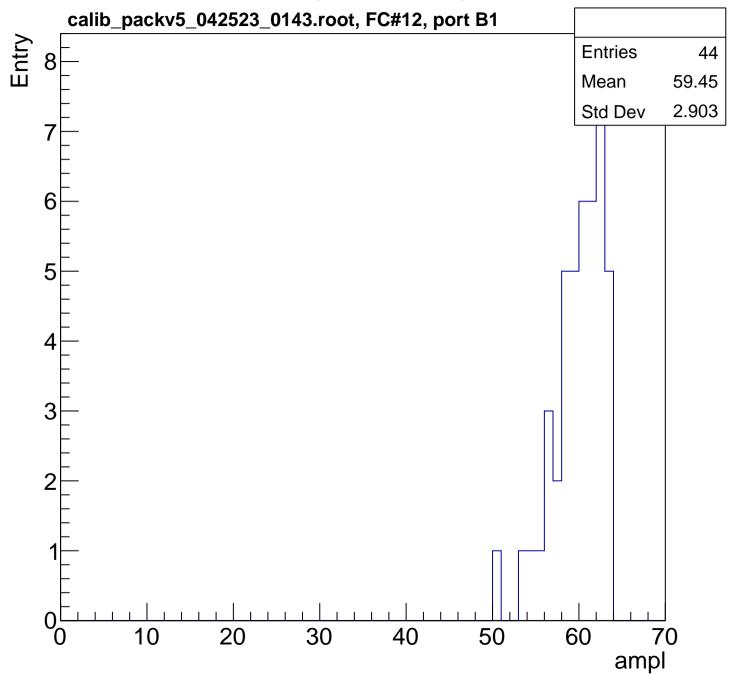


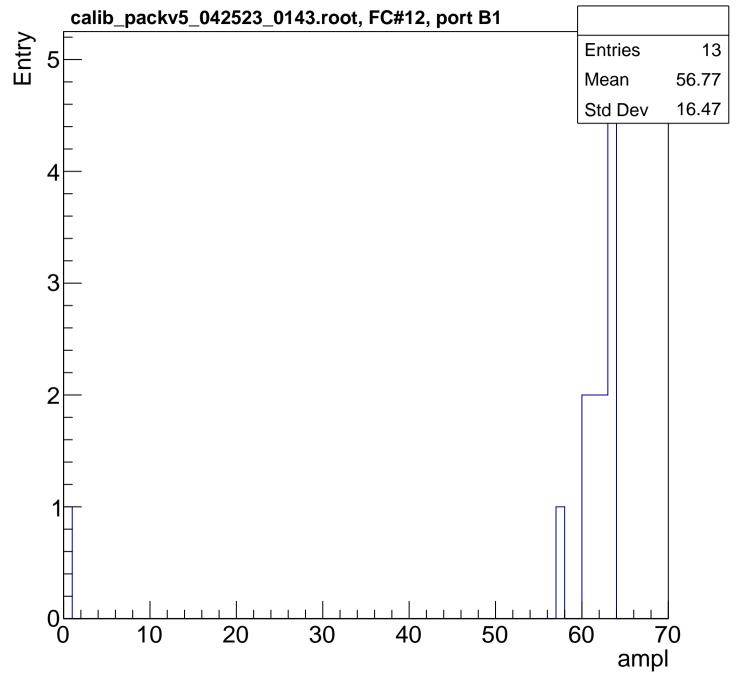




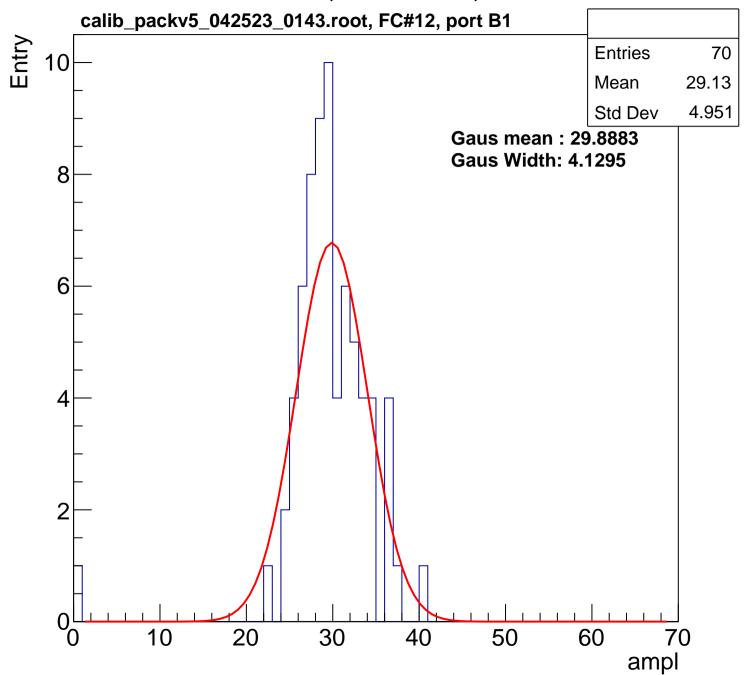


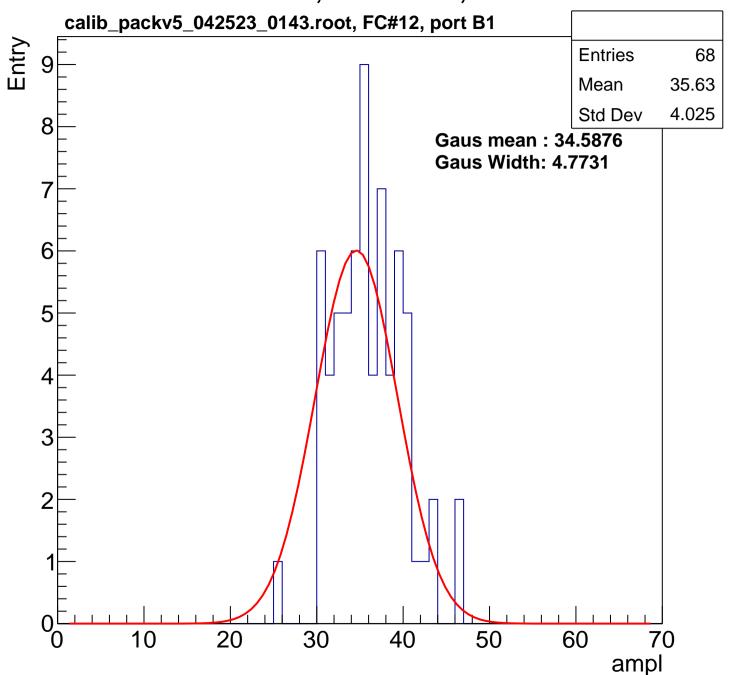


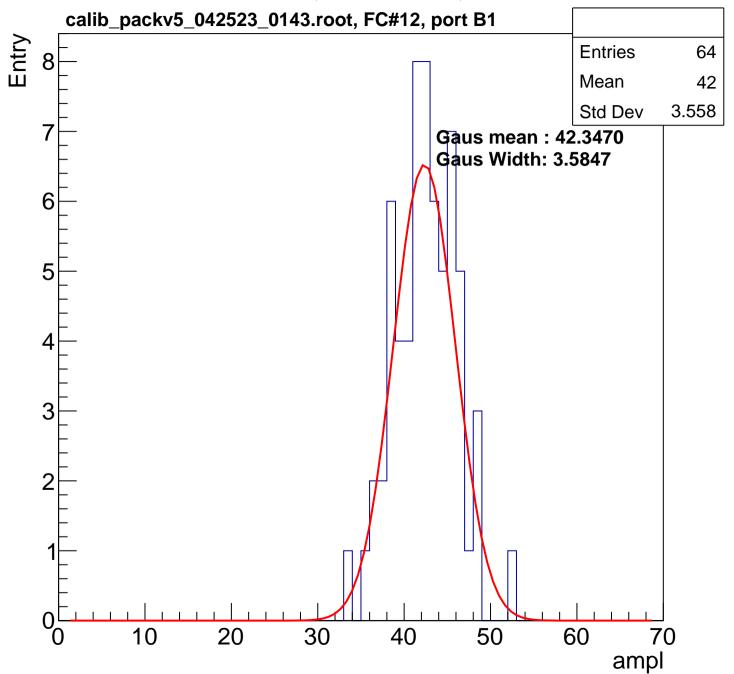


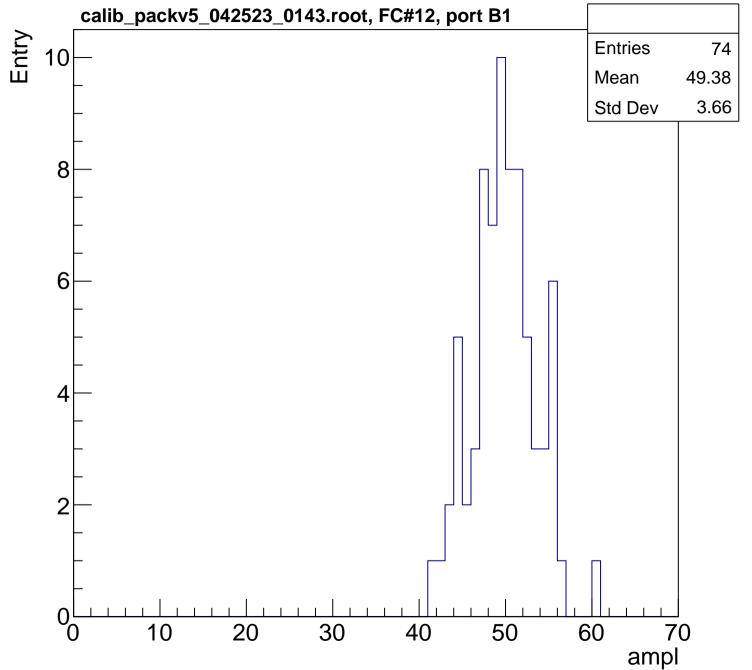


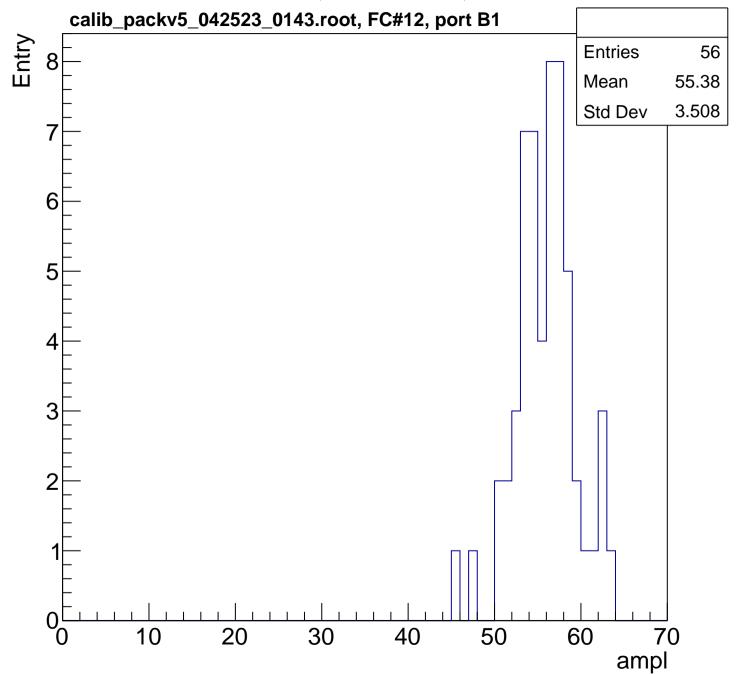


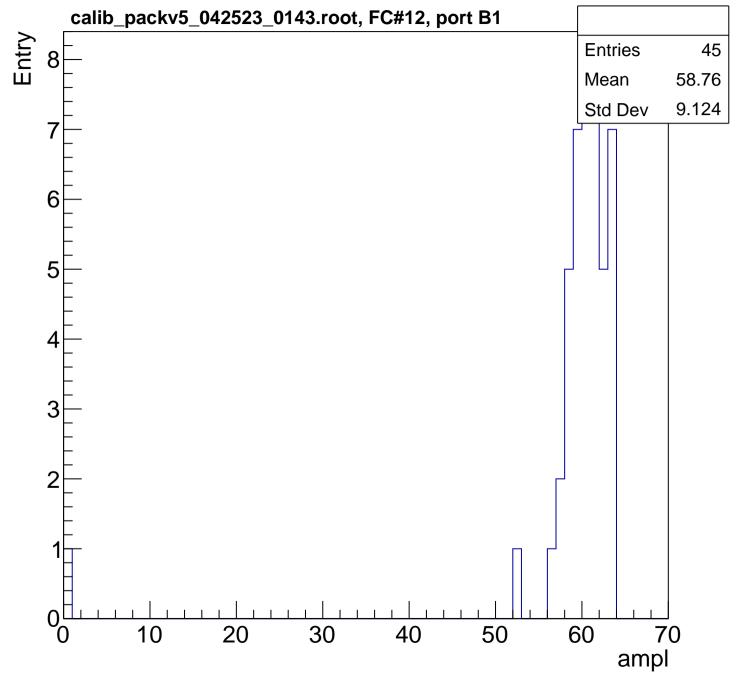


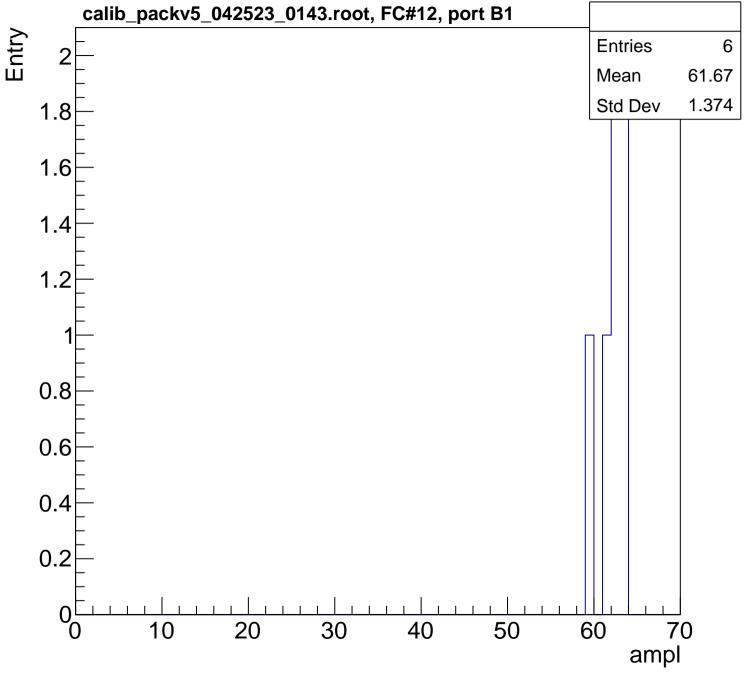




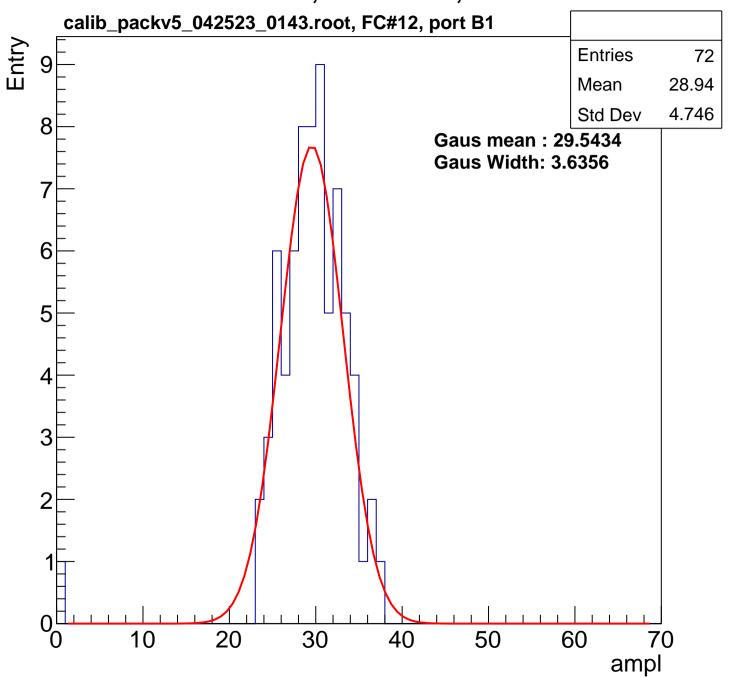


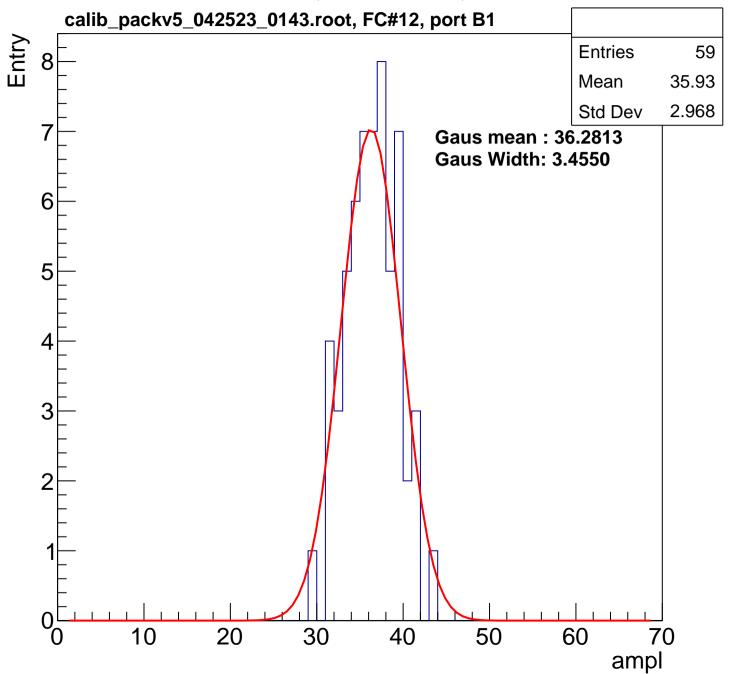


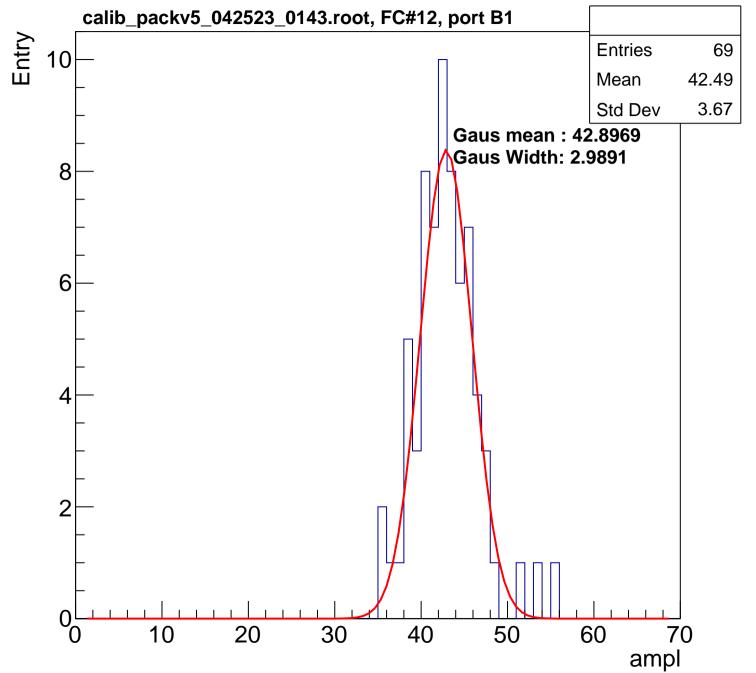


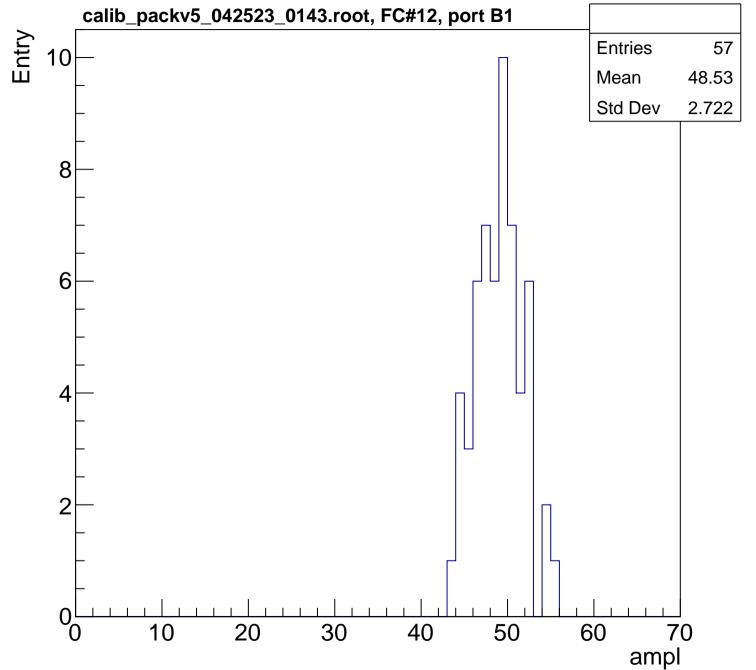


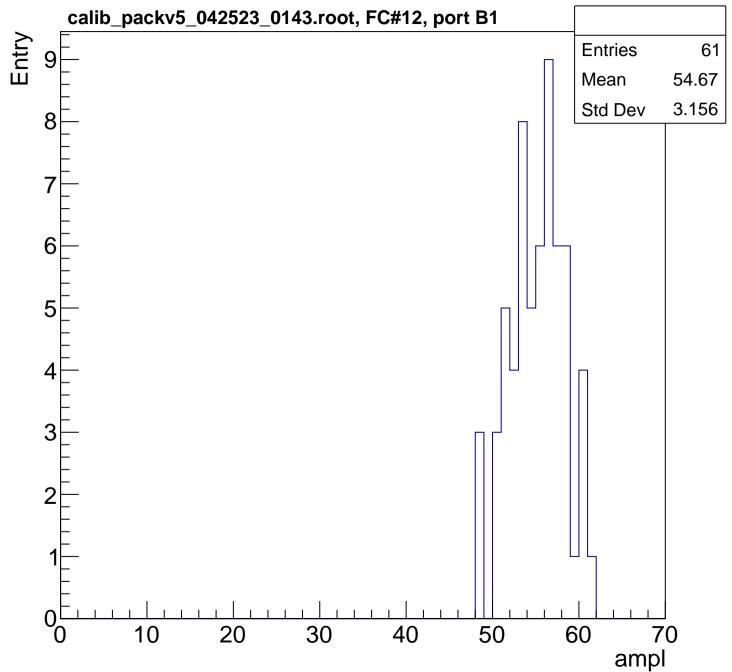
B0L102S, U4-ch30, adc7 calib_packv5_042523_0143.root, FC#12, port B1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

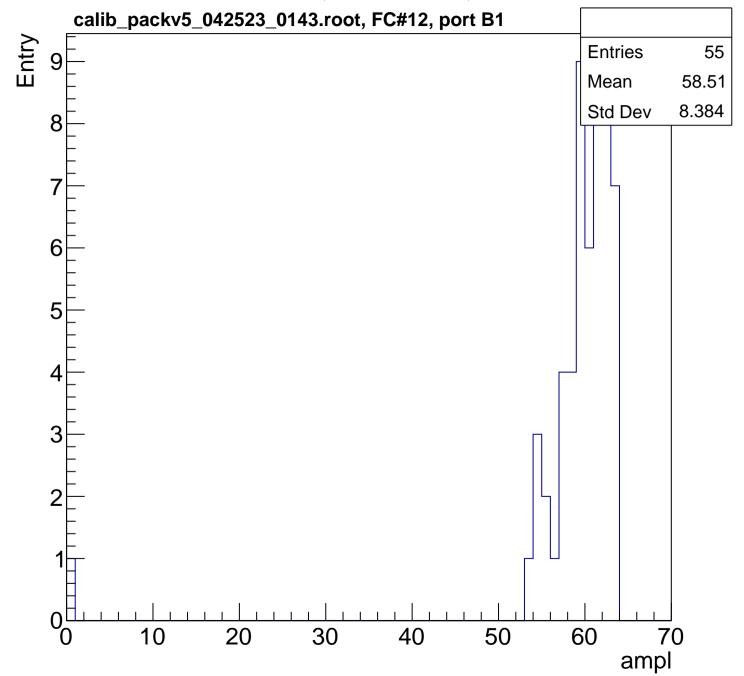


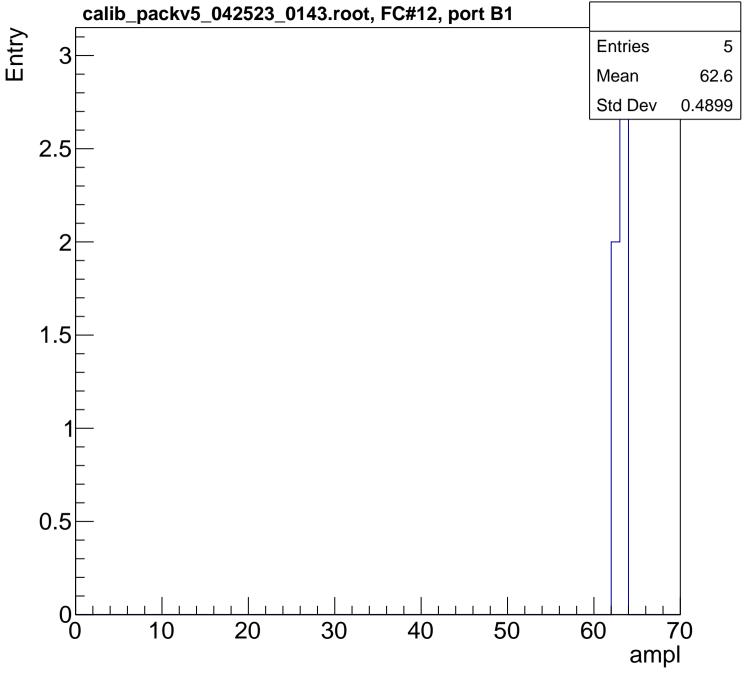


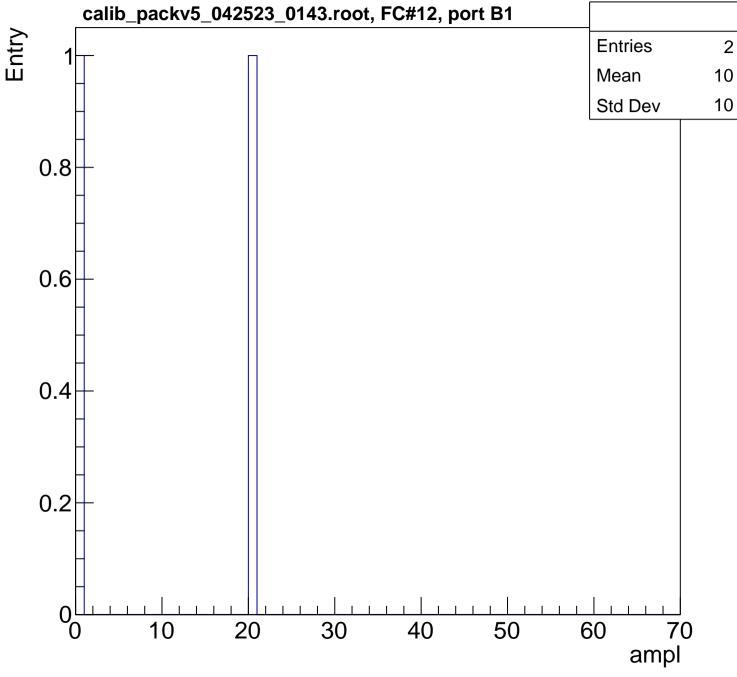


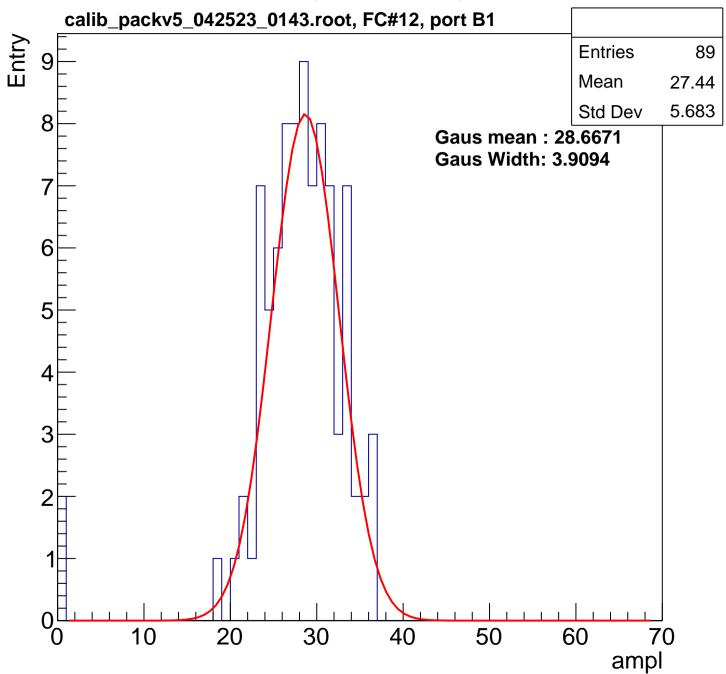


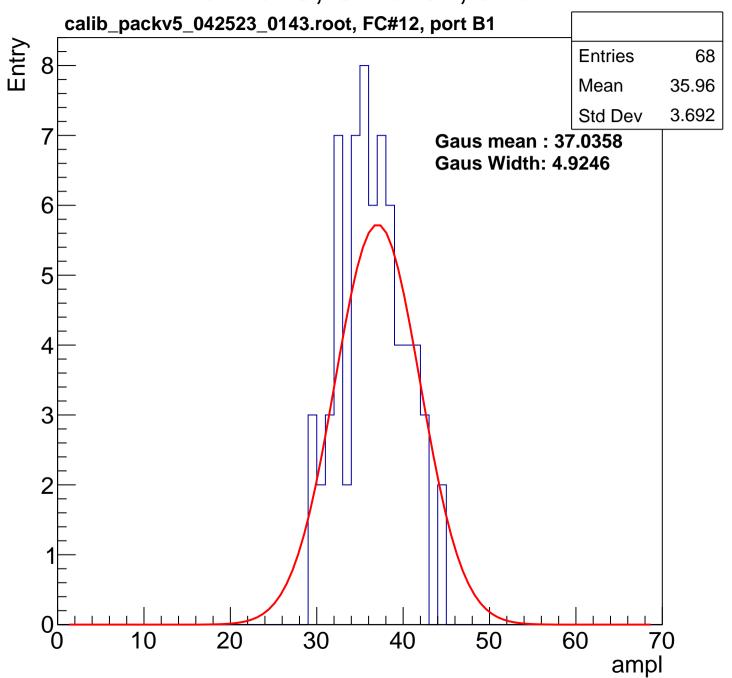


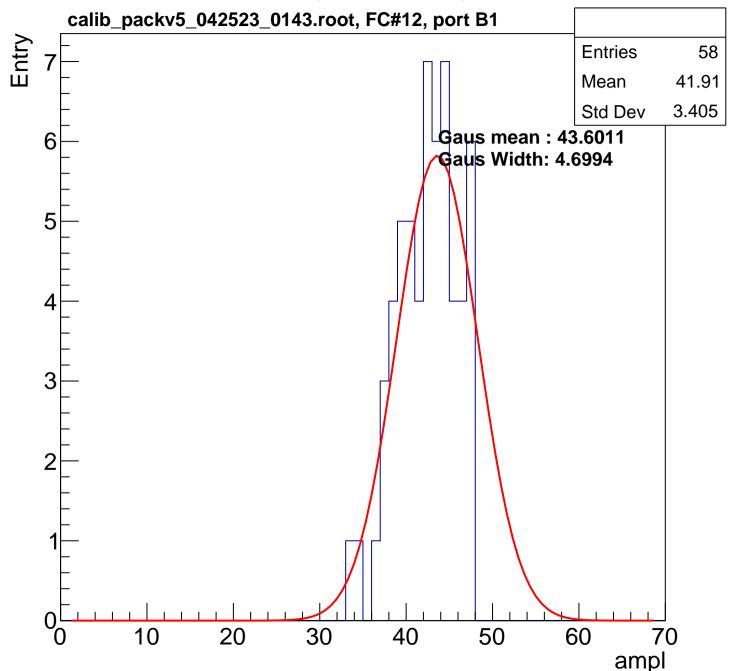


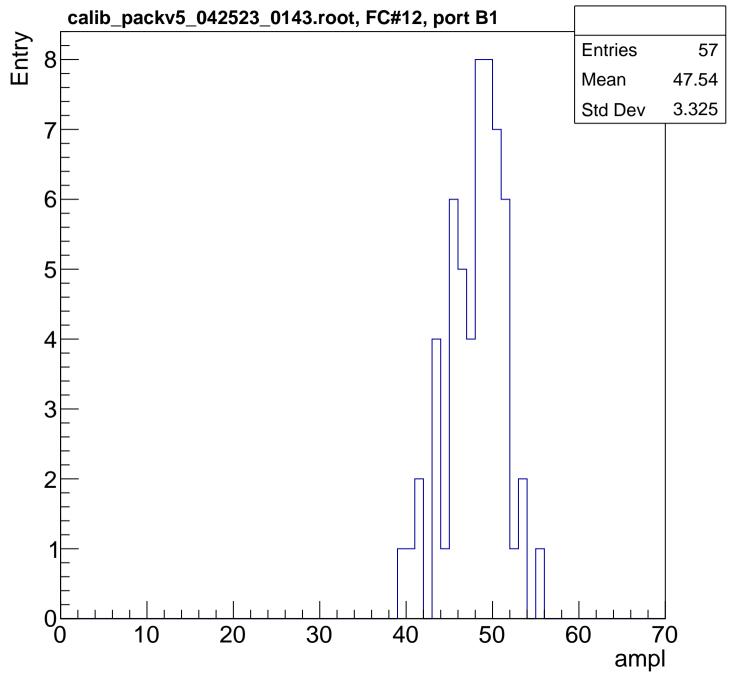


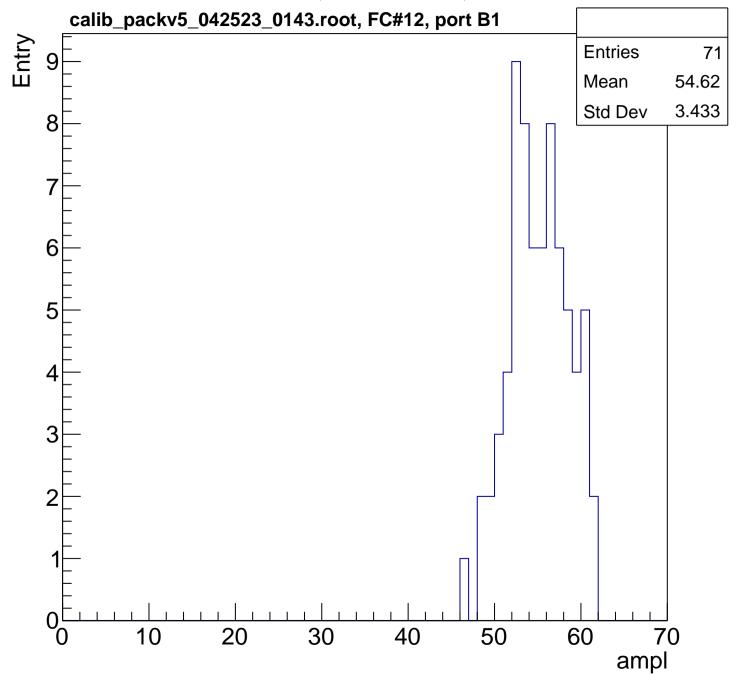


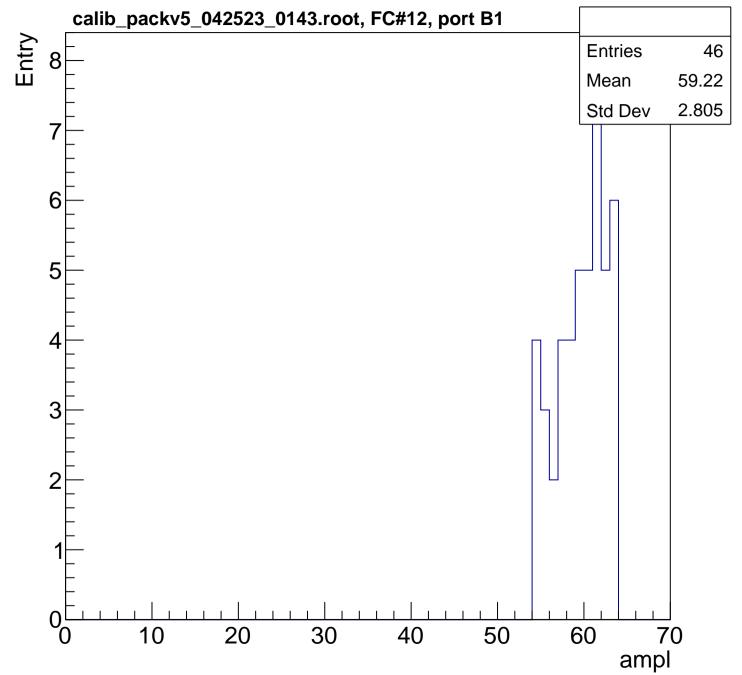


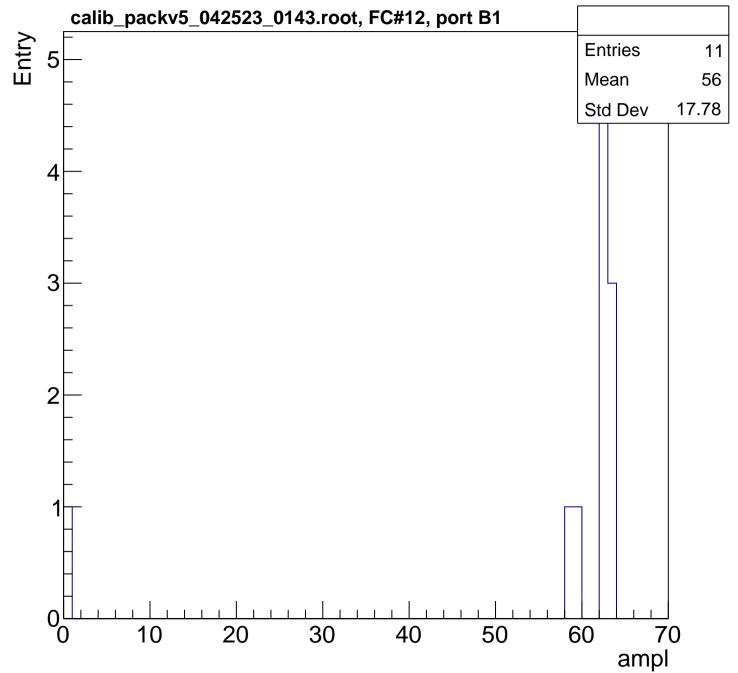


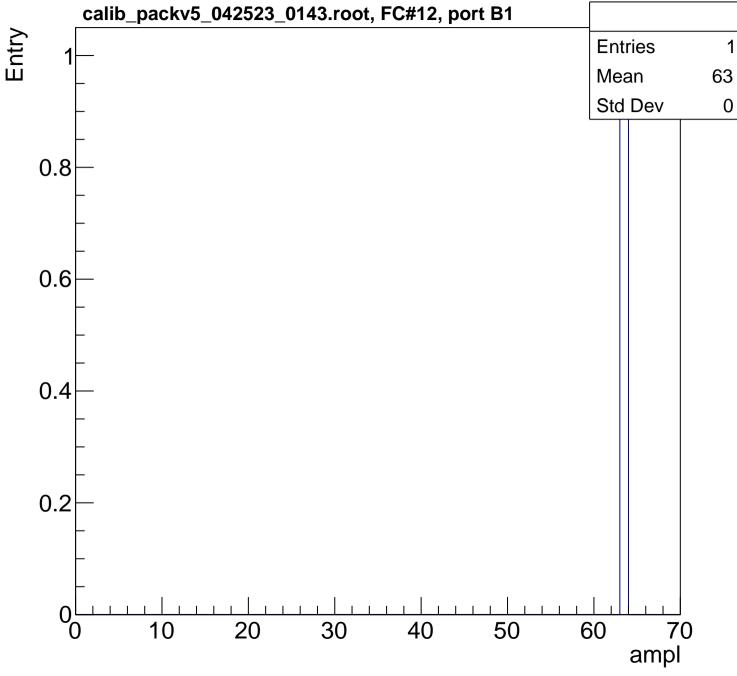


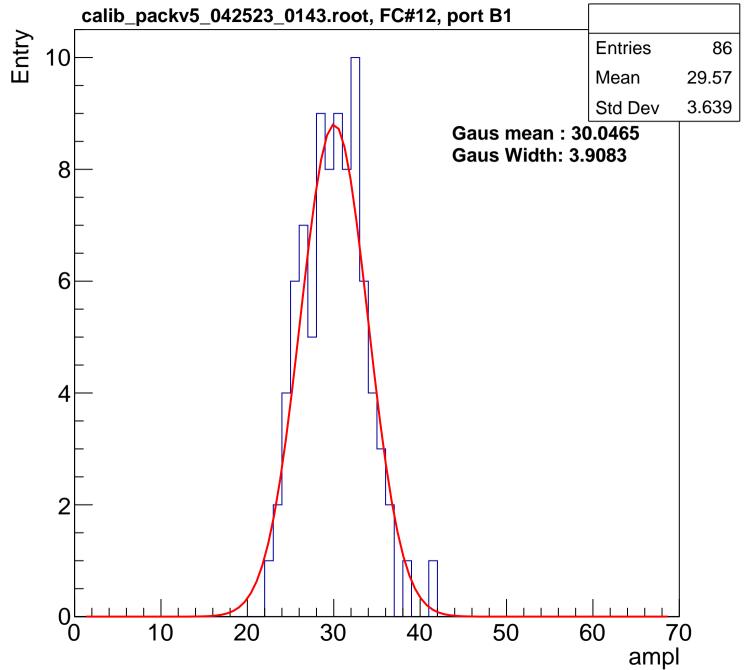


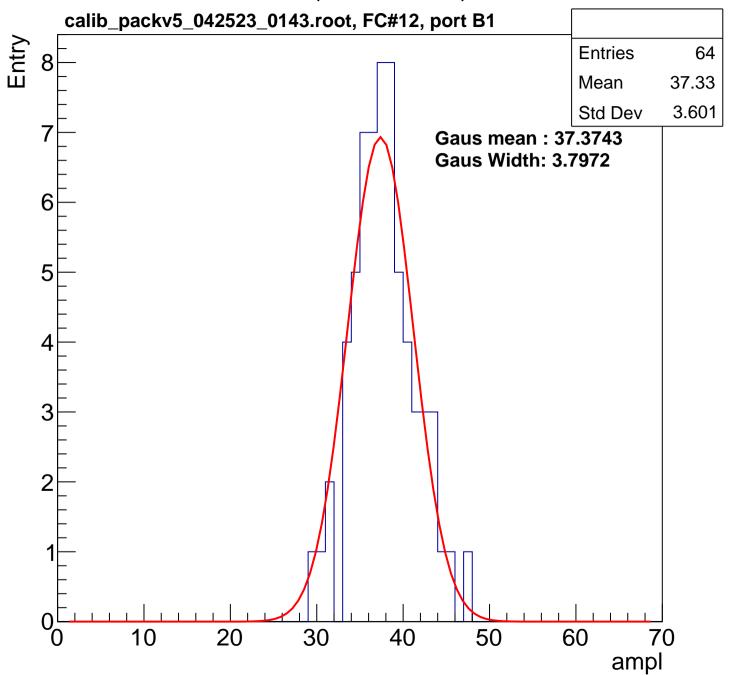


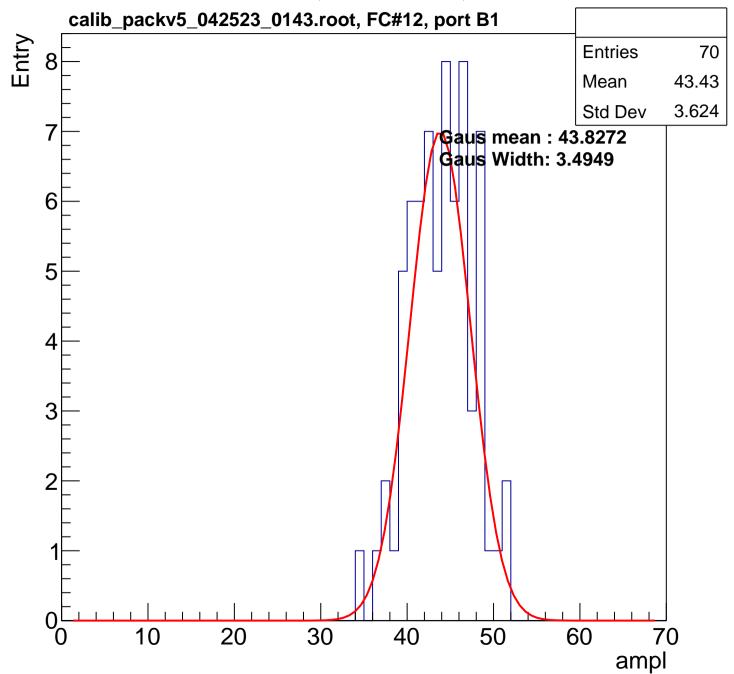


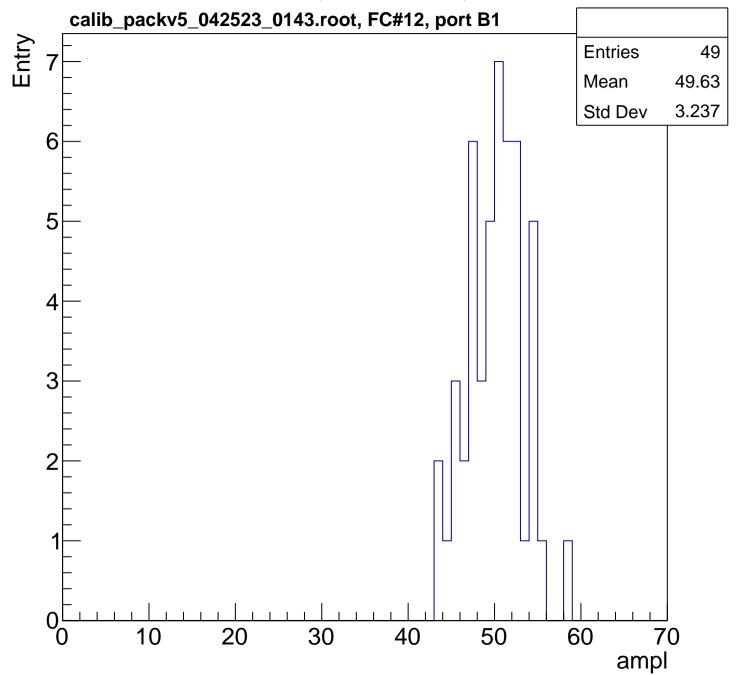


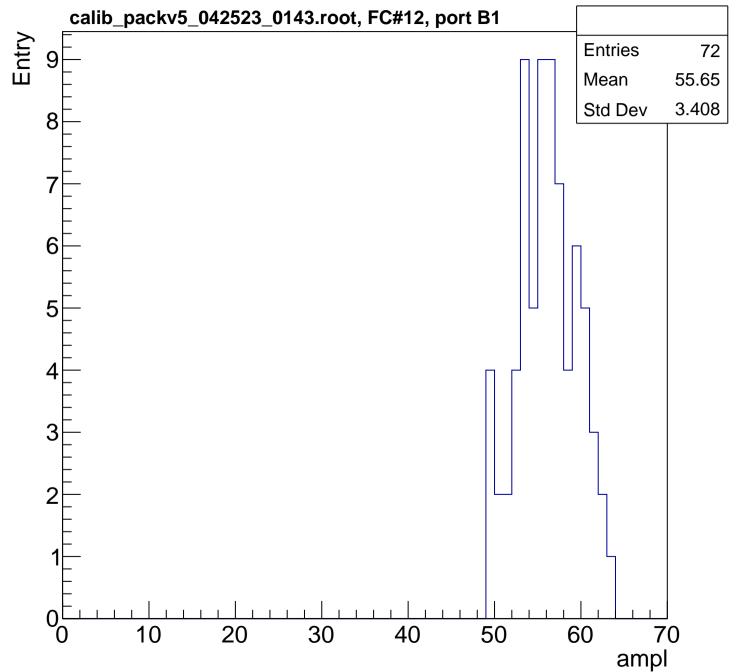


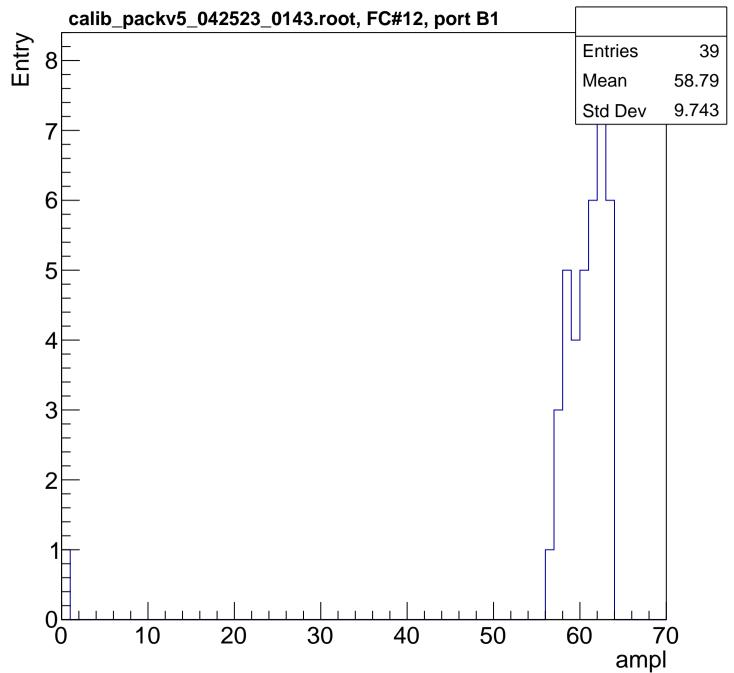


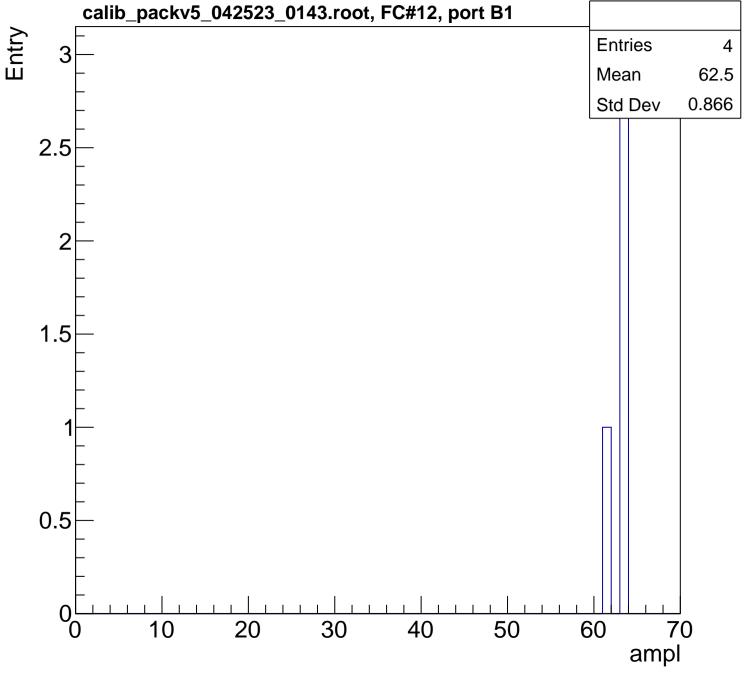


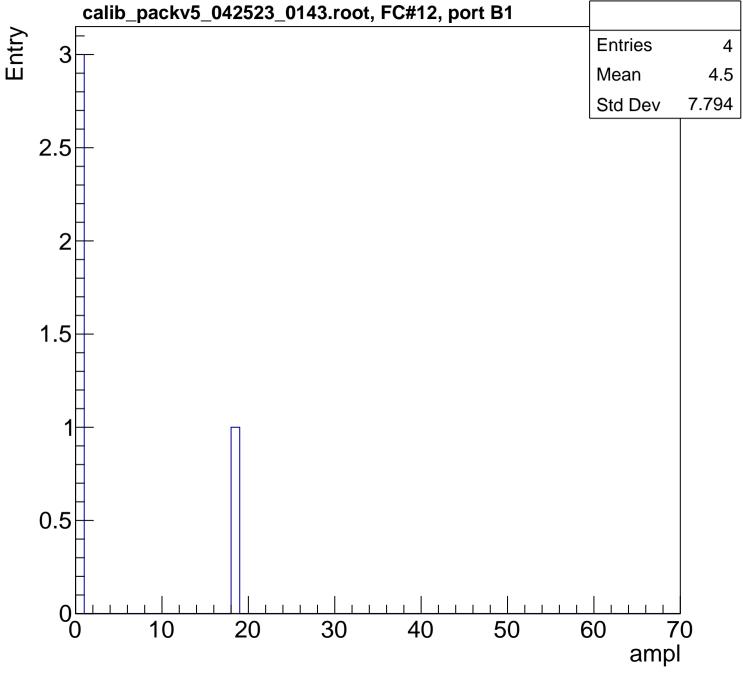


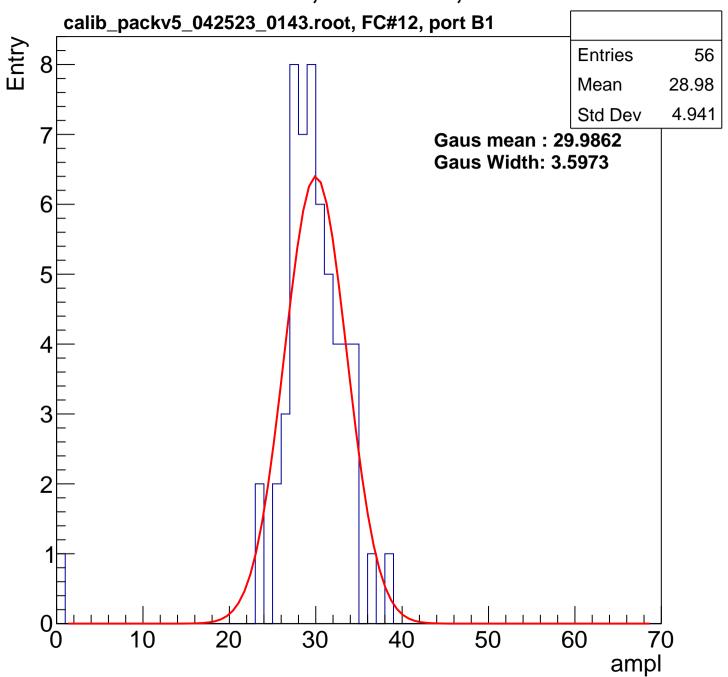


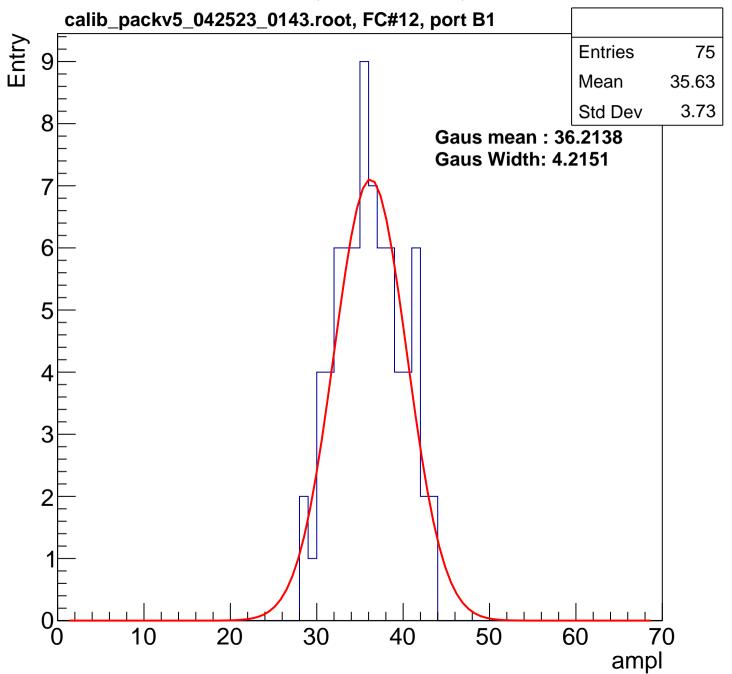


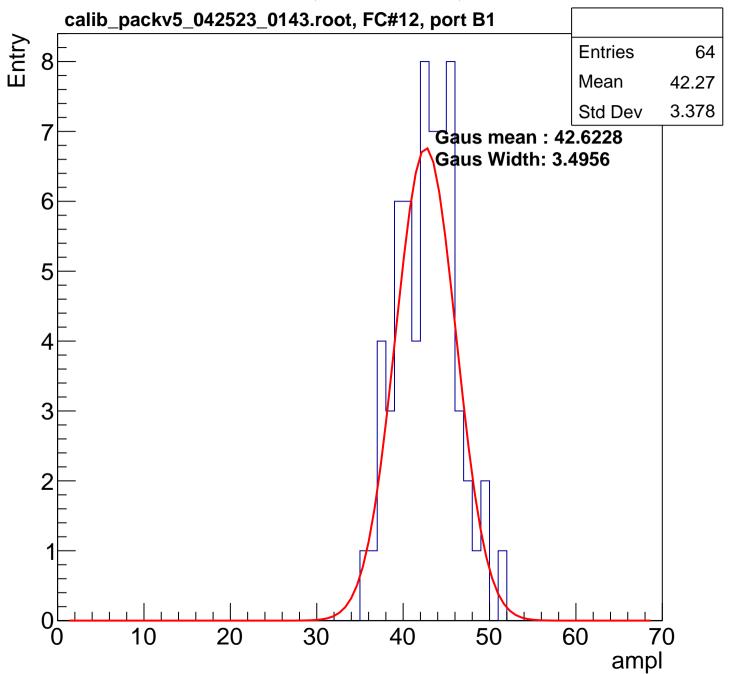


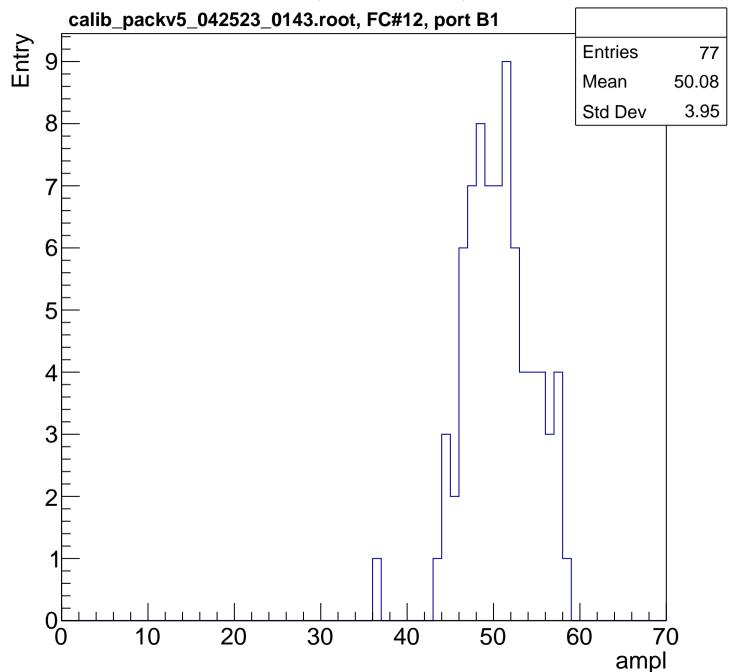


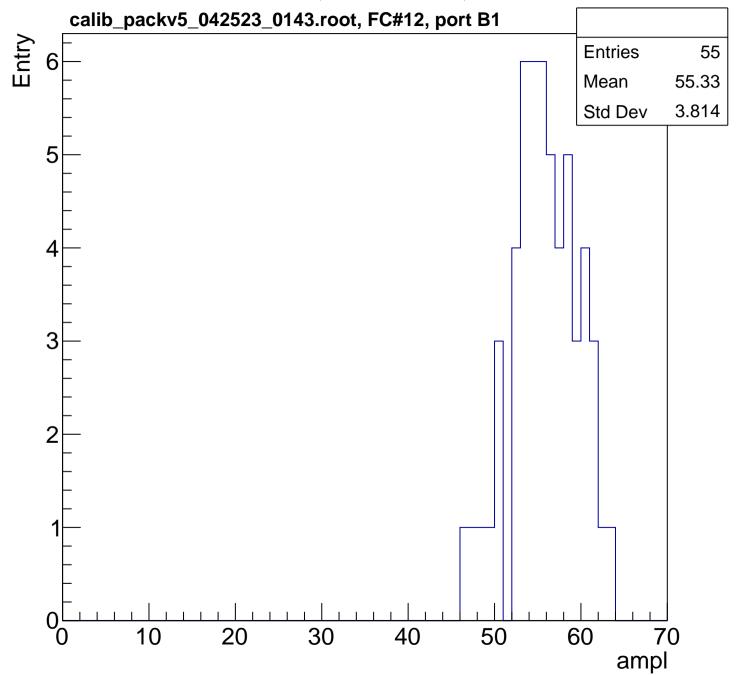


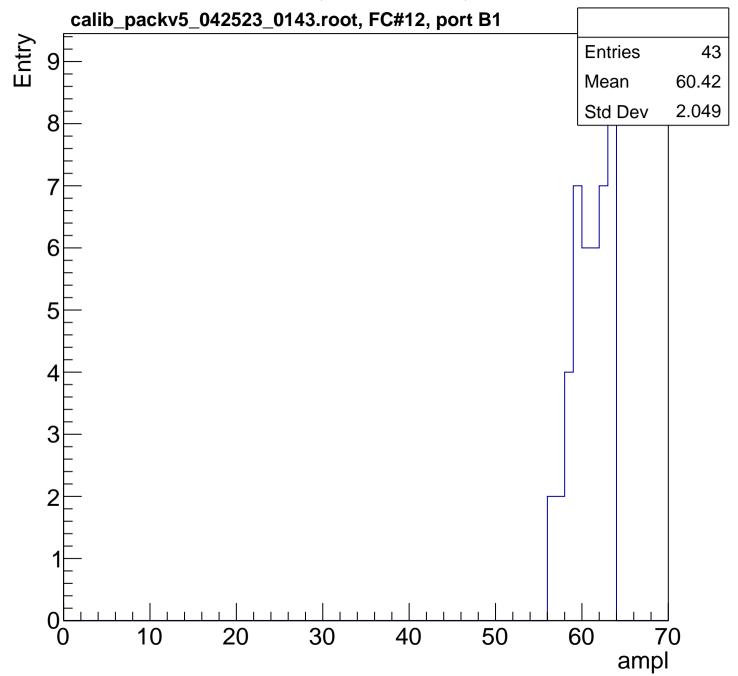


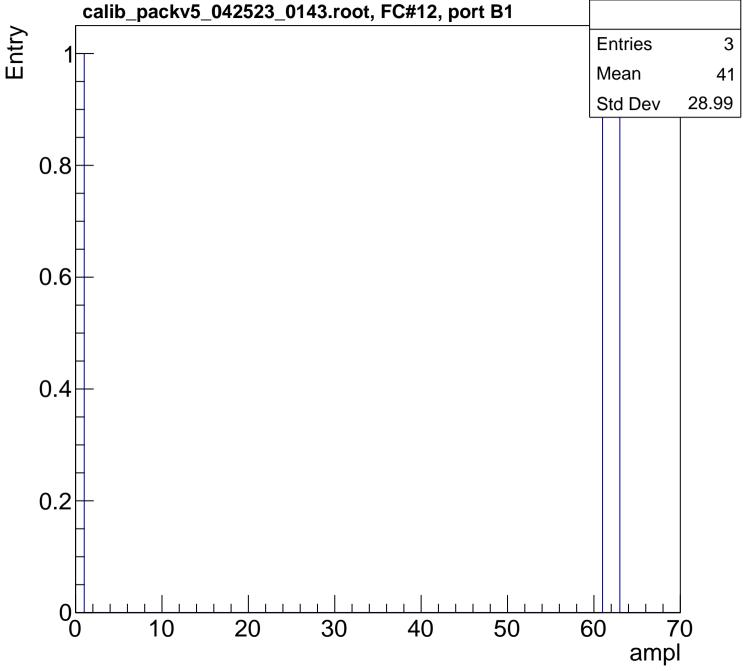


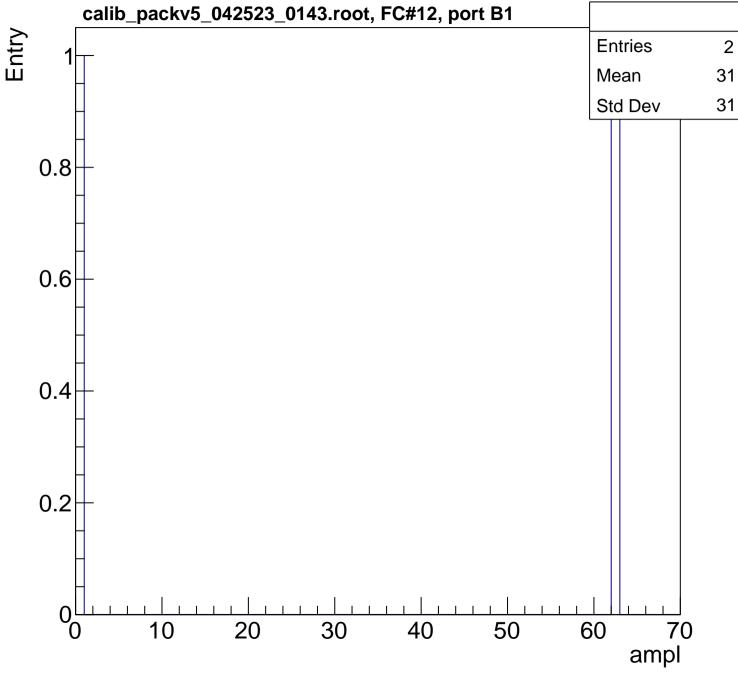


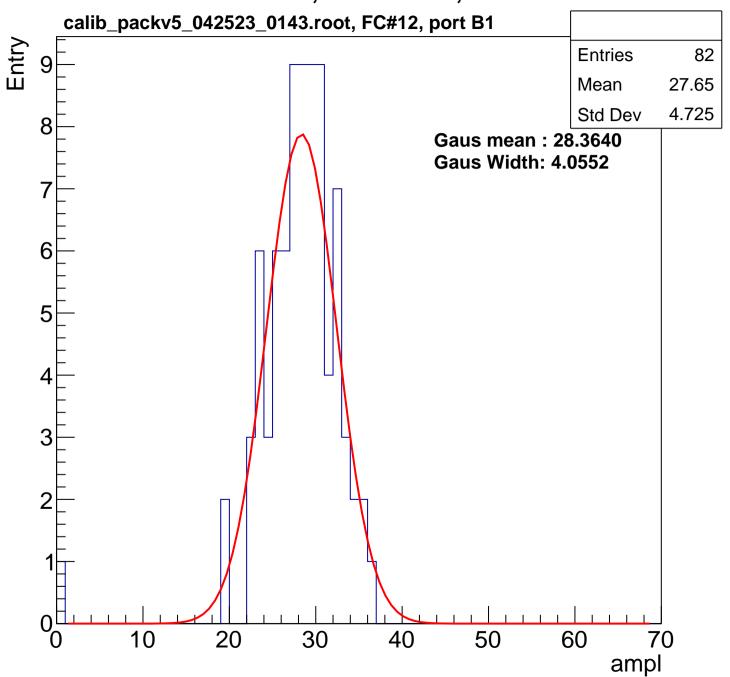


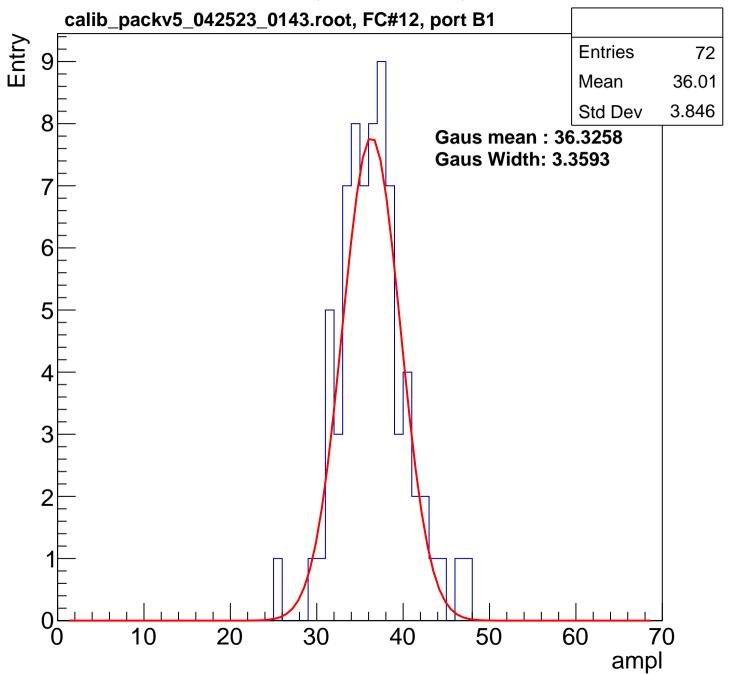


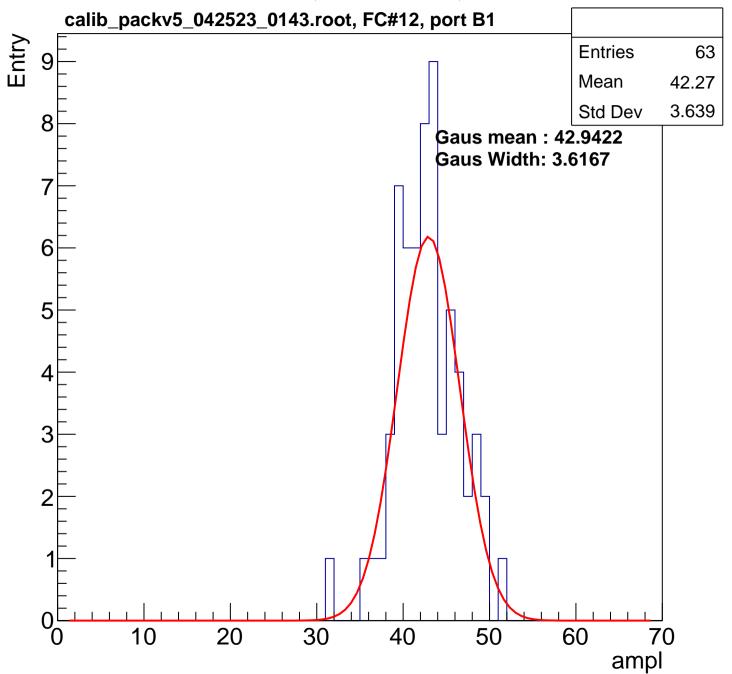


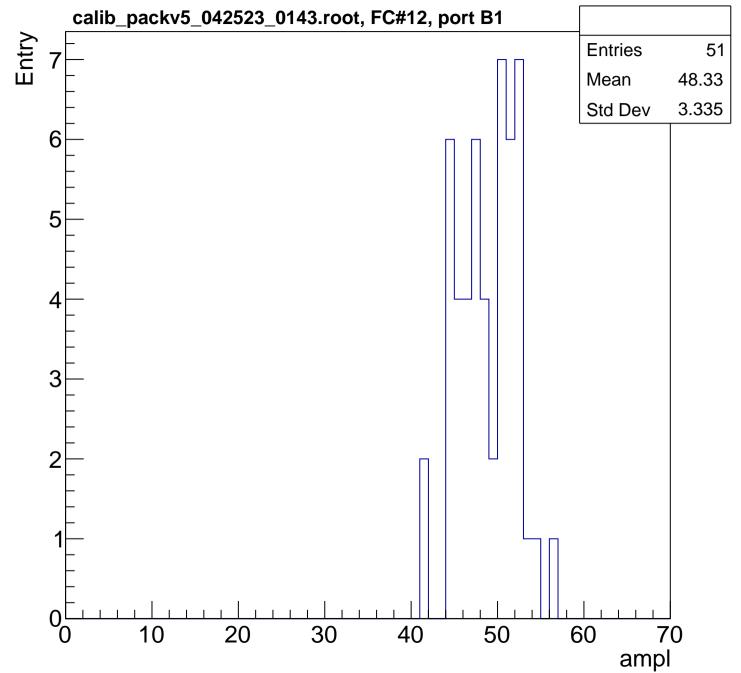


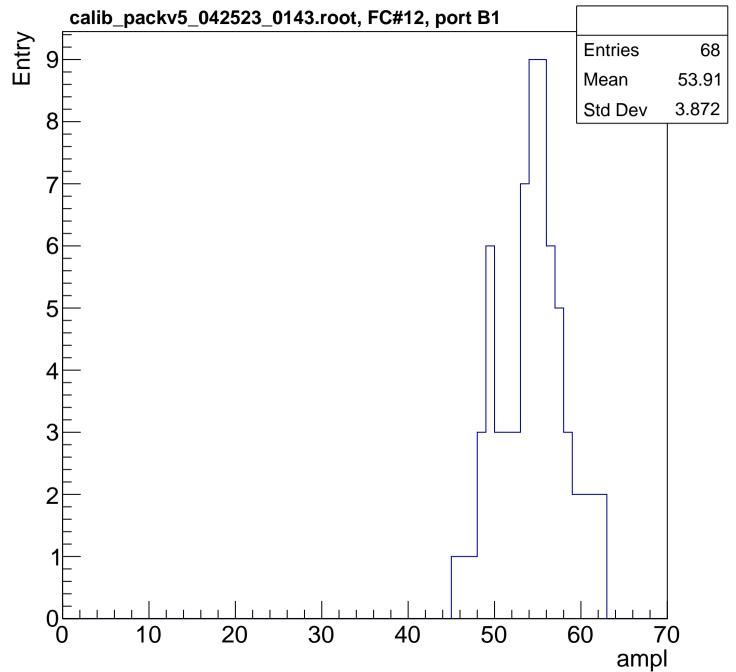


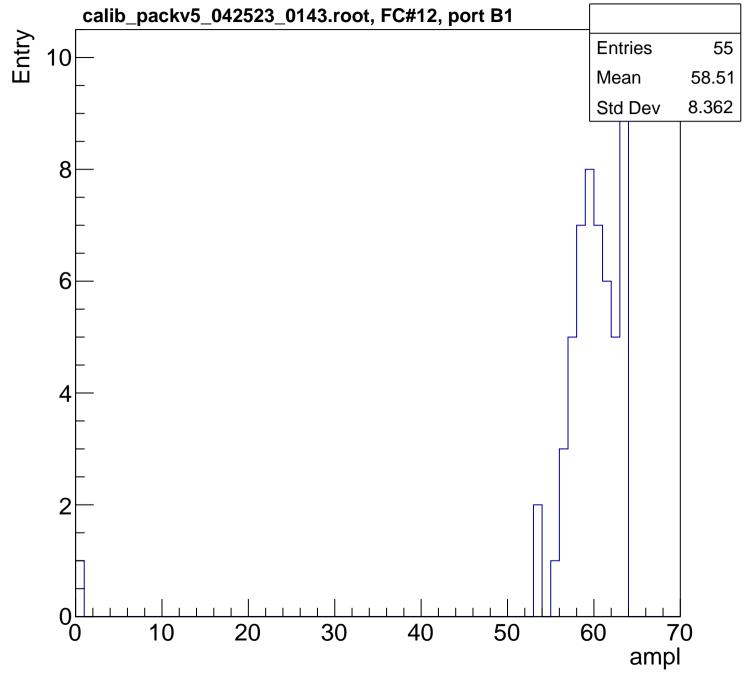


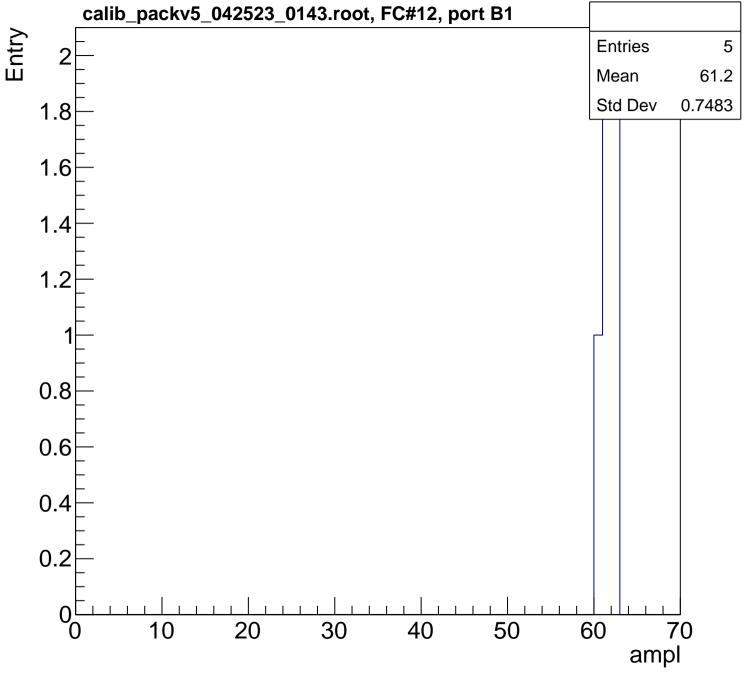


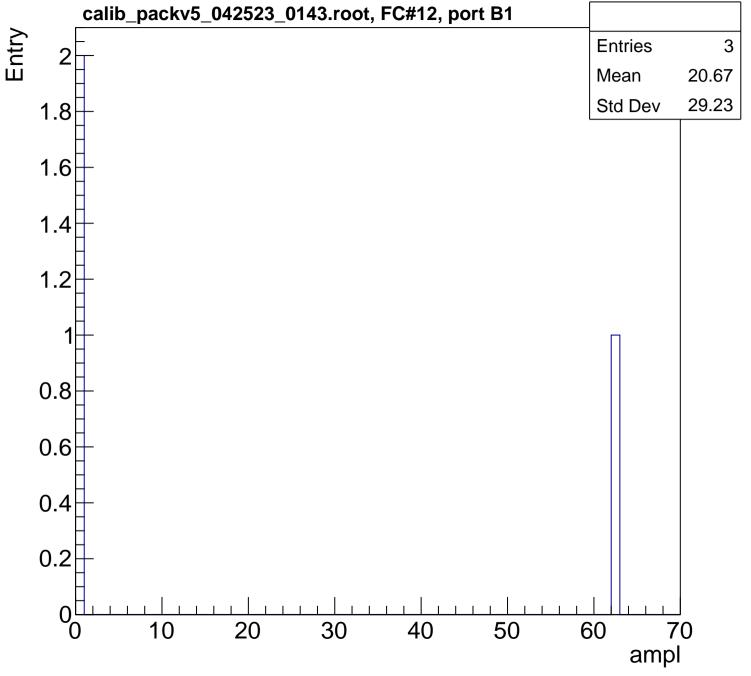


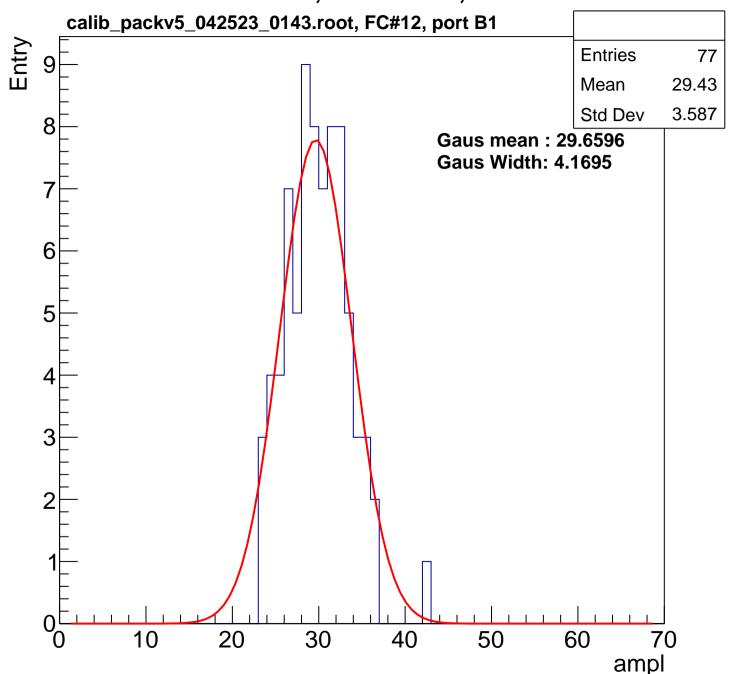


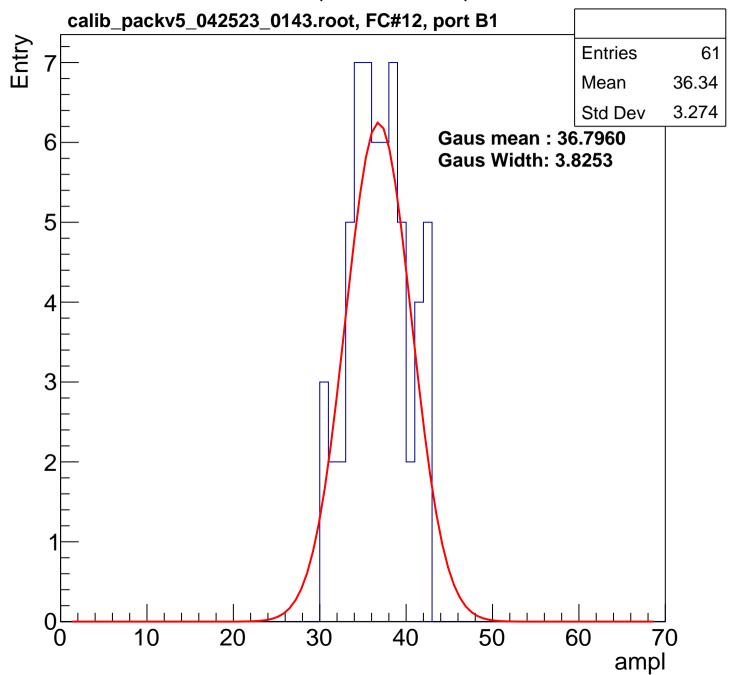


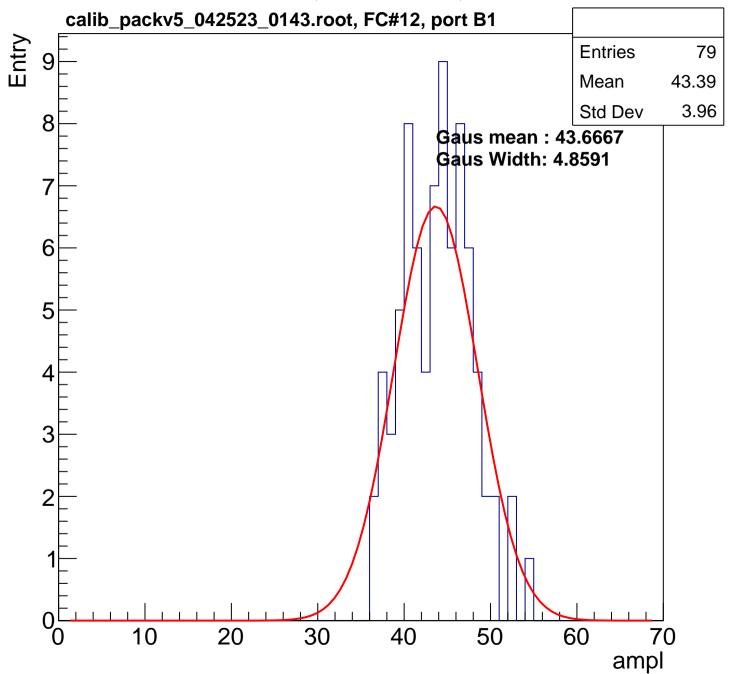


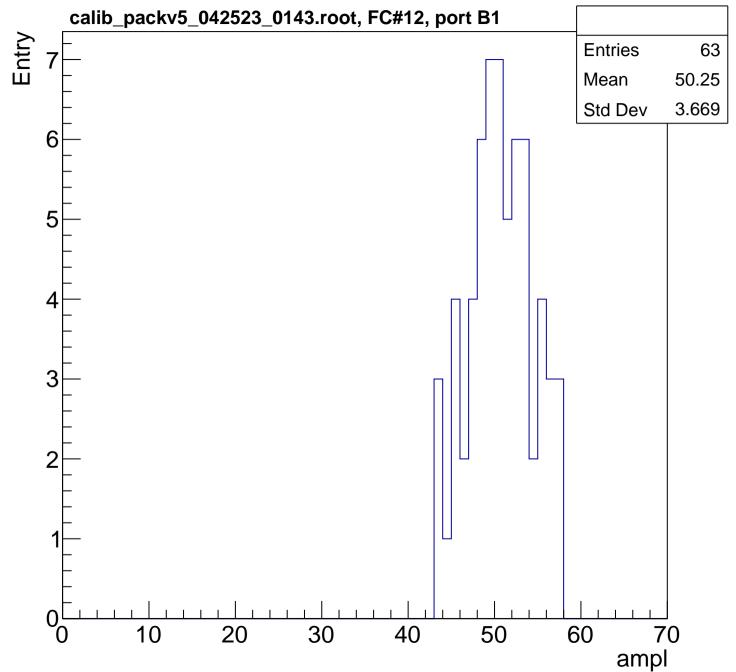


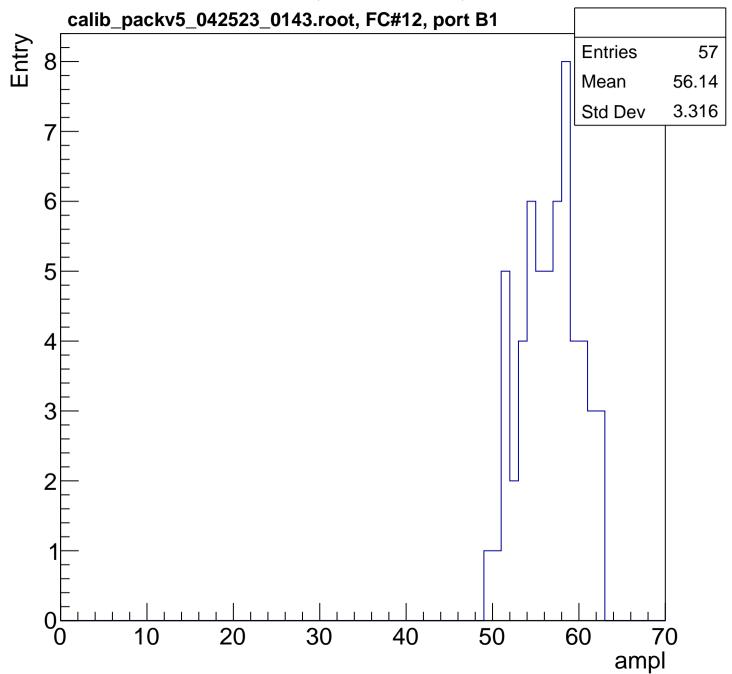


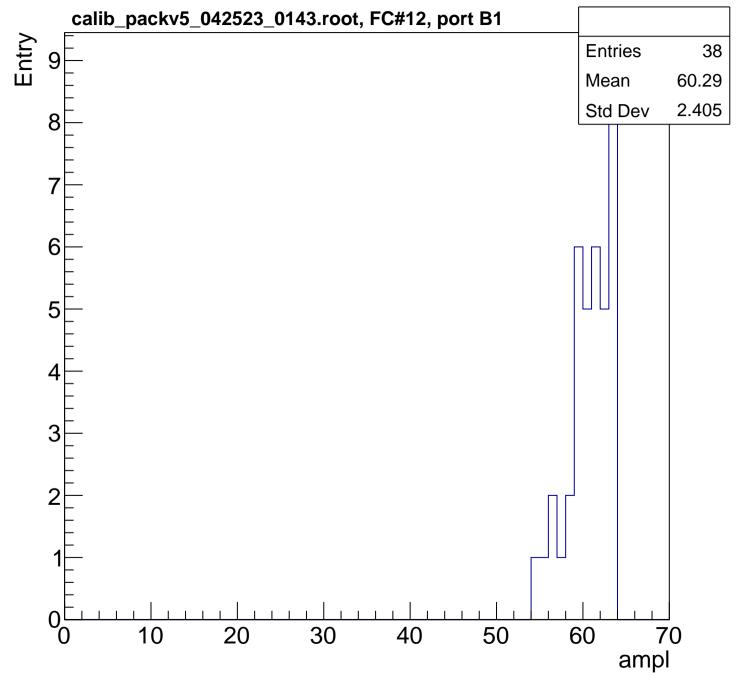


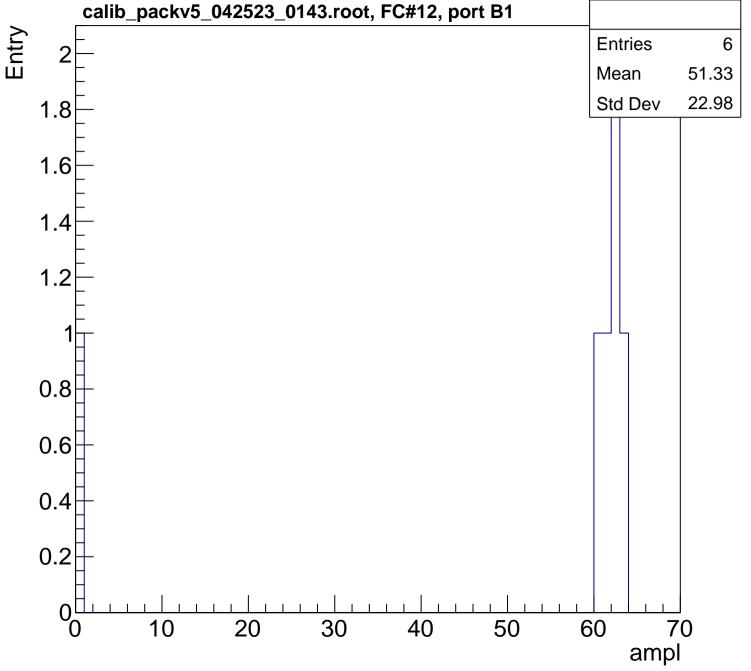




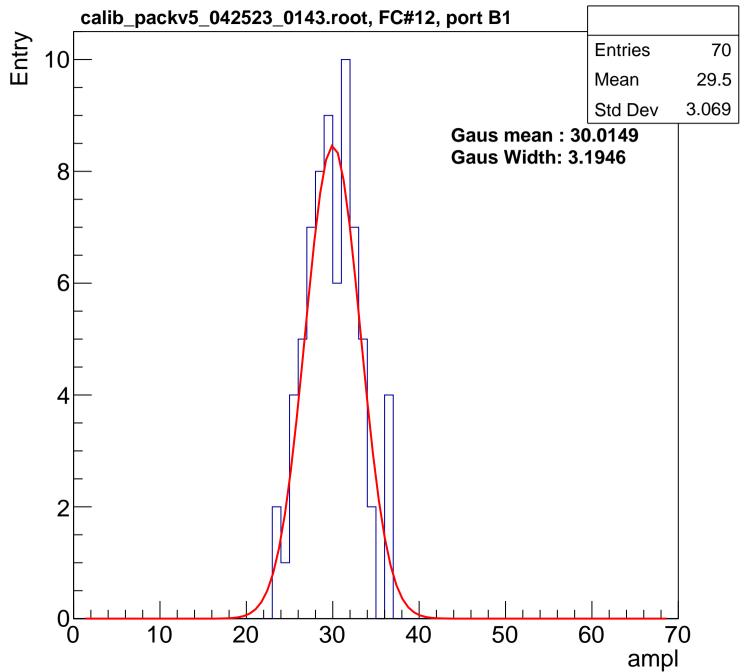


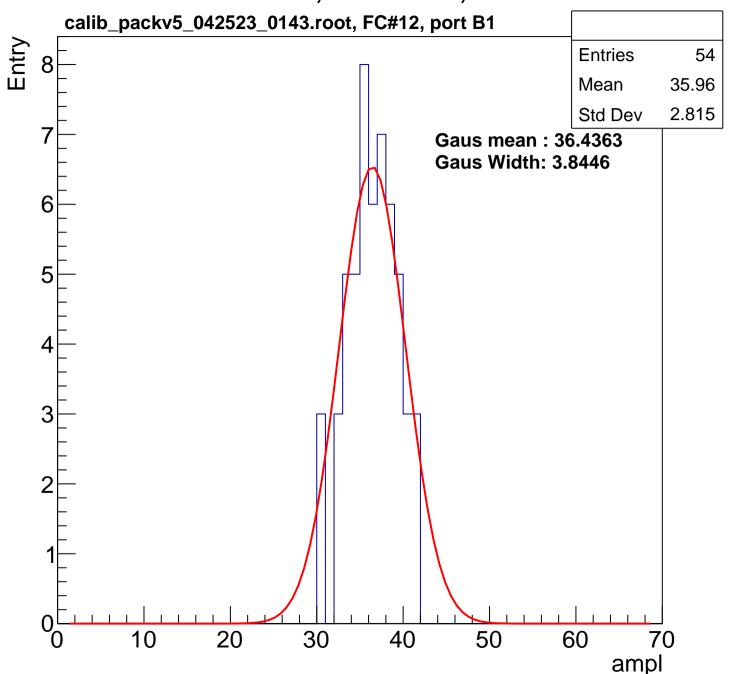


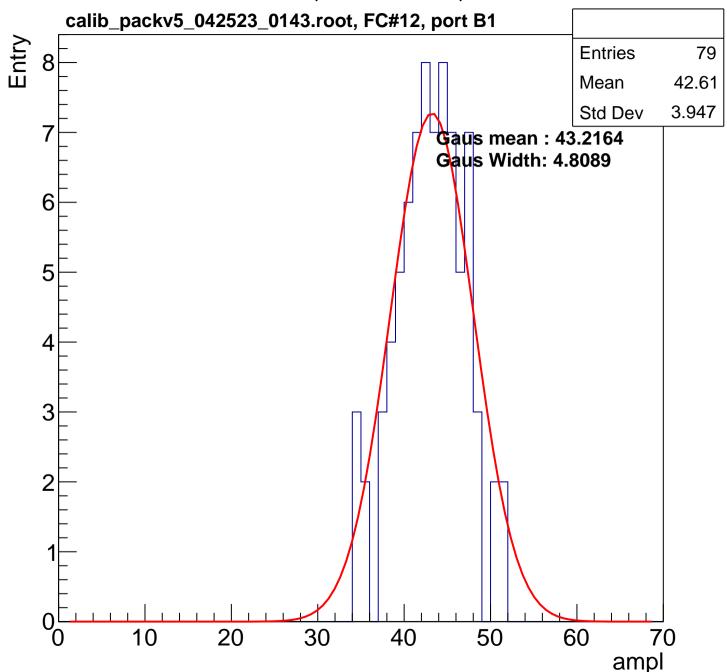


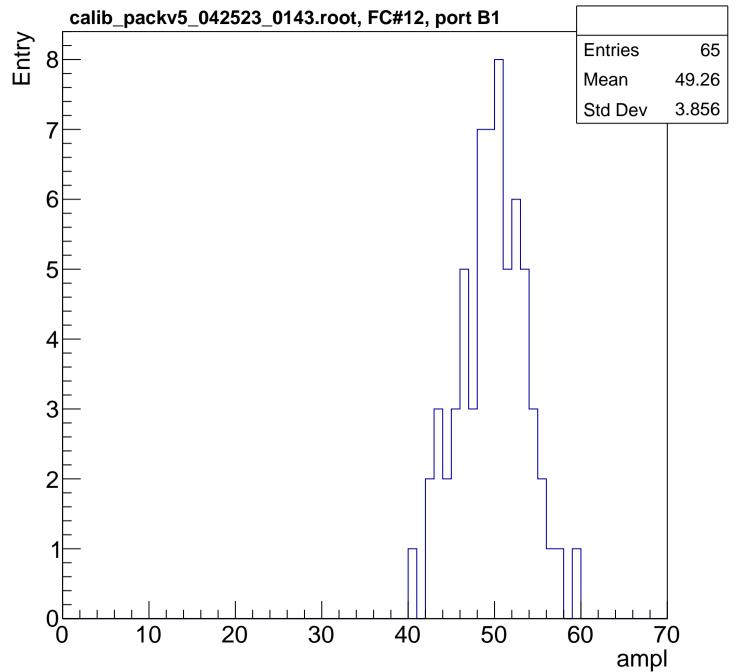


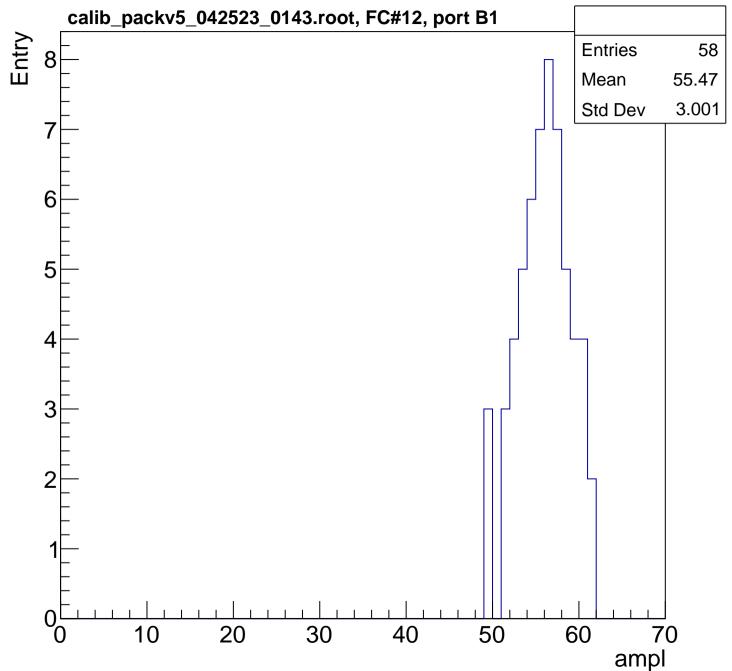
B0L102S, U4-ch36, adc7 calib_packv5_042523_0143.root, FC#12, port B1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

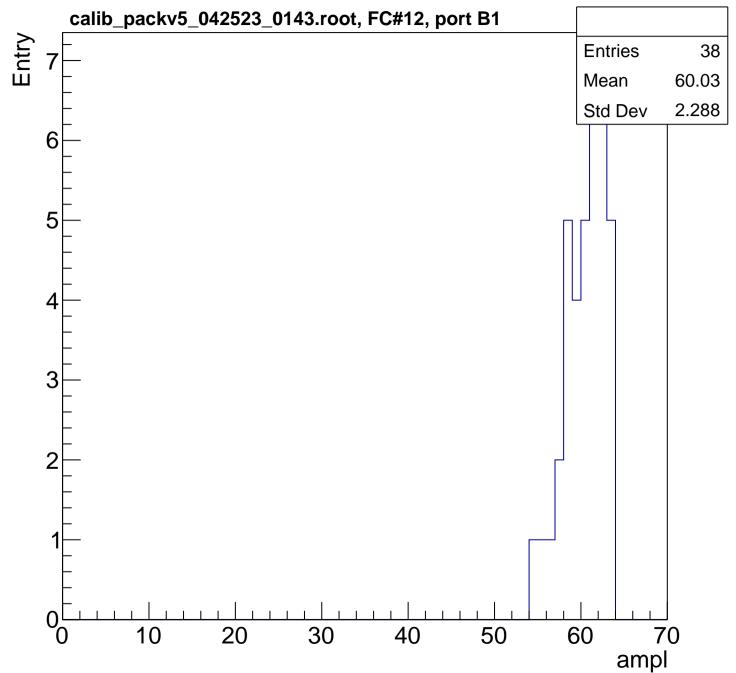


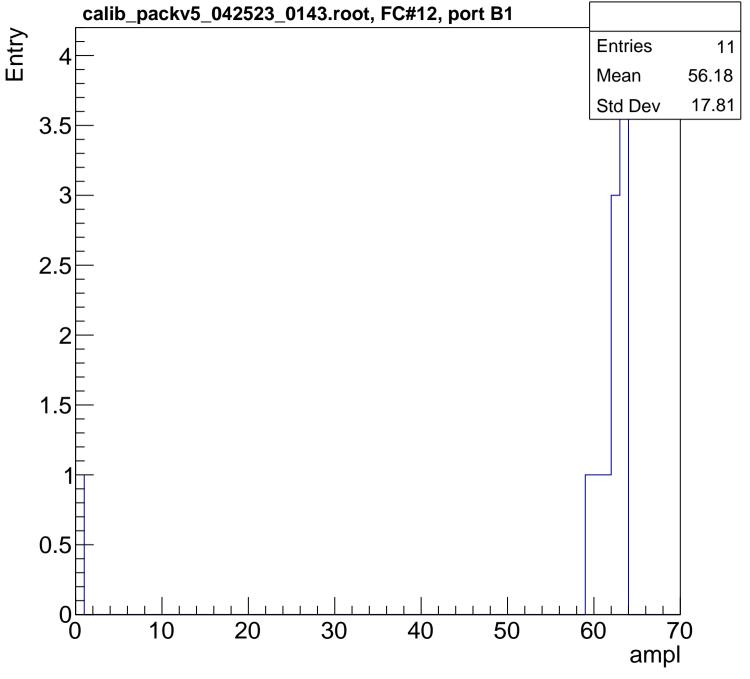


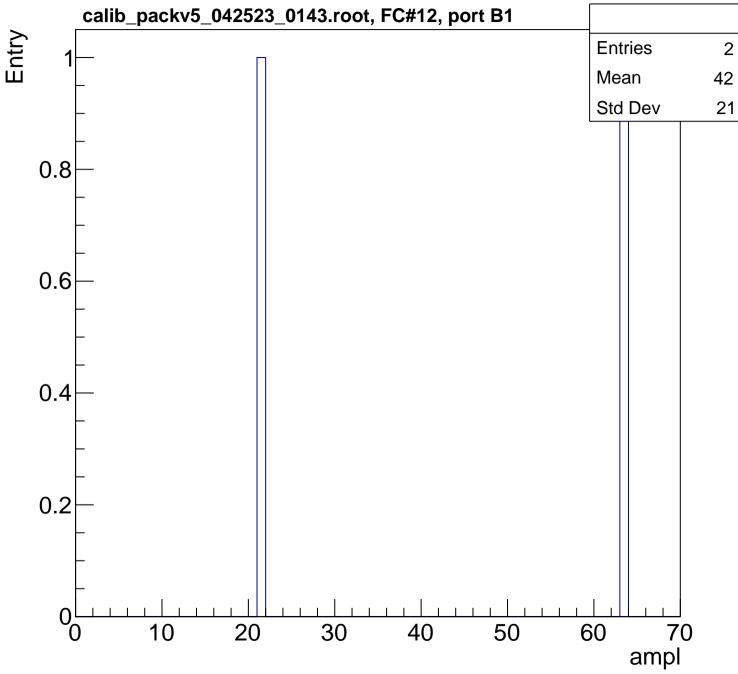


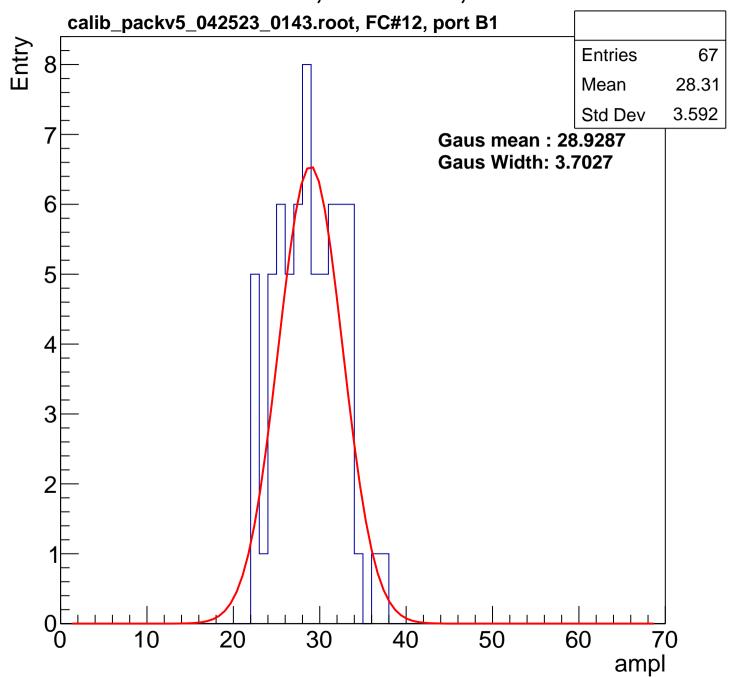


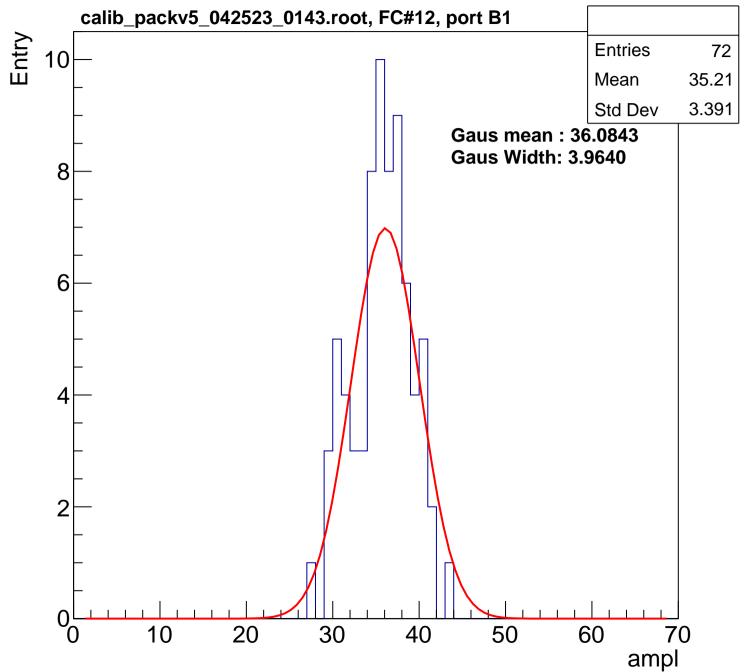


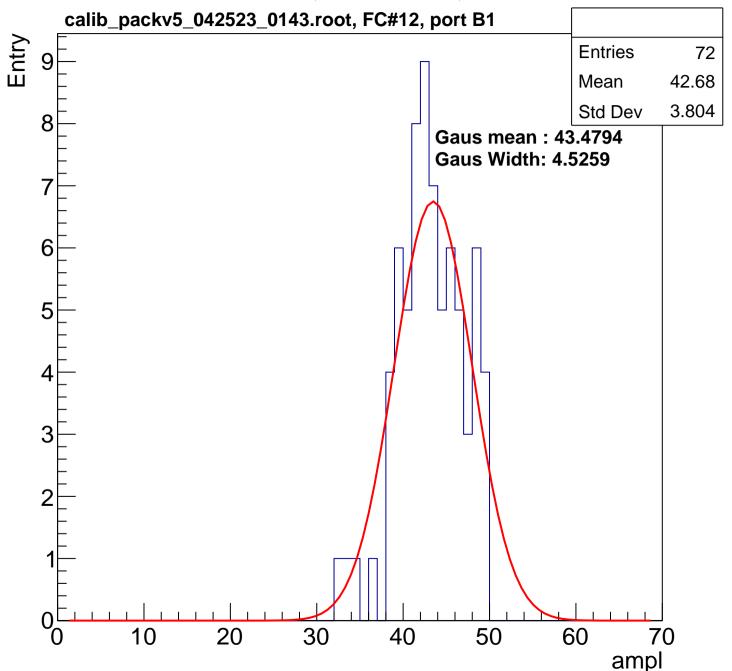


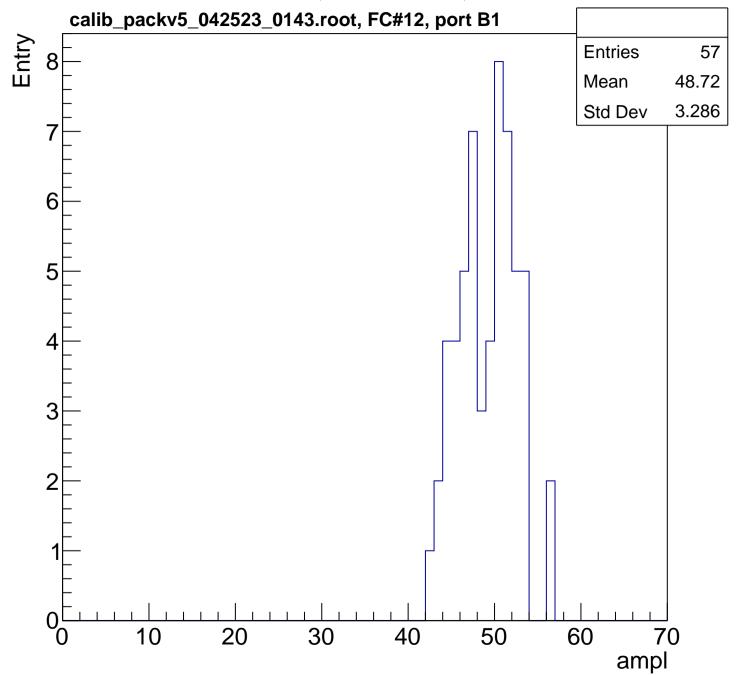


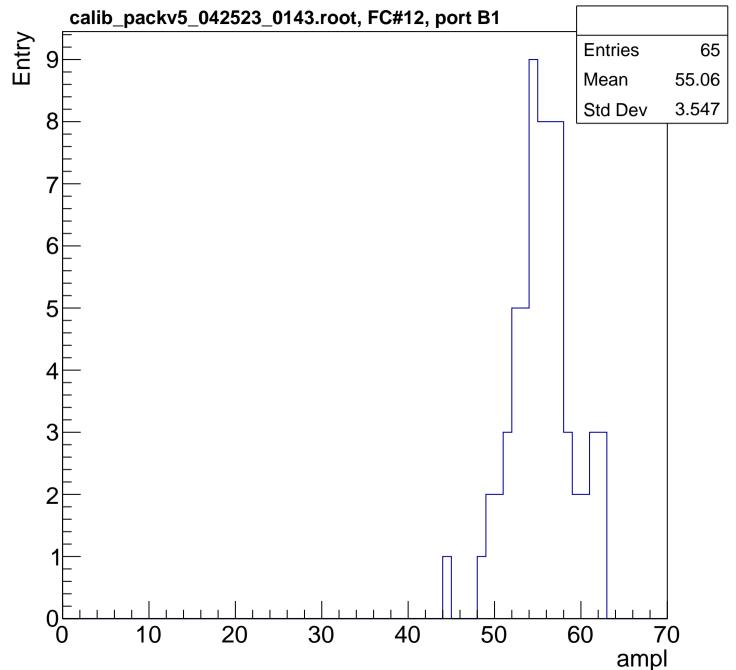


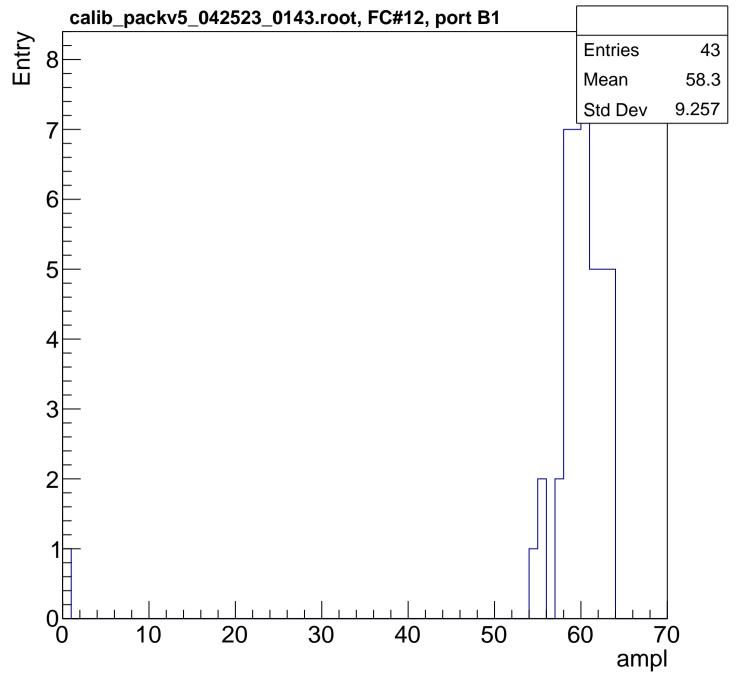


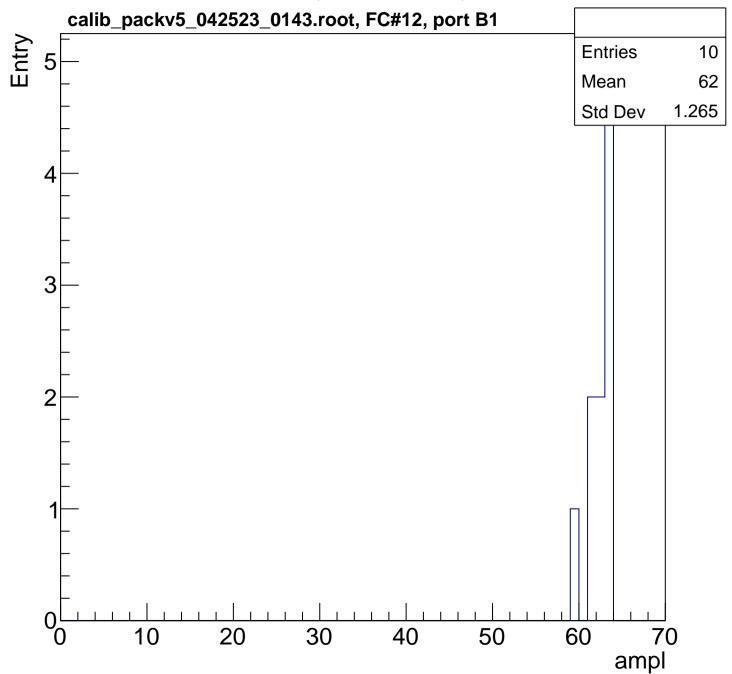






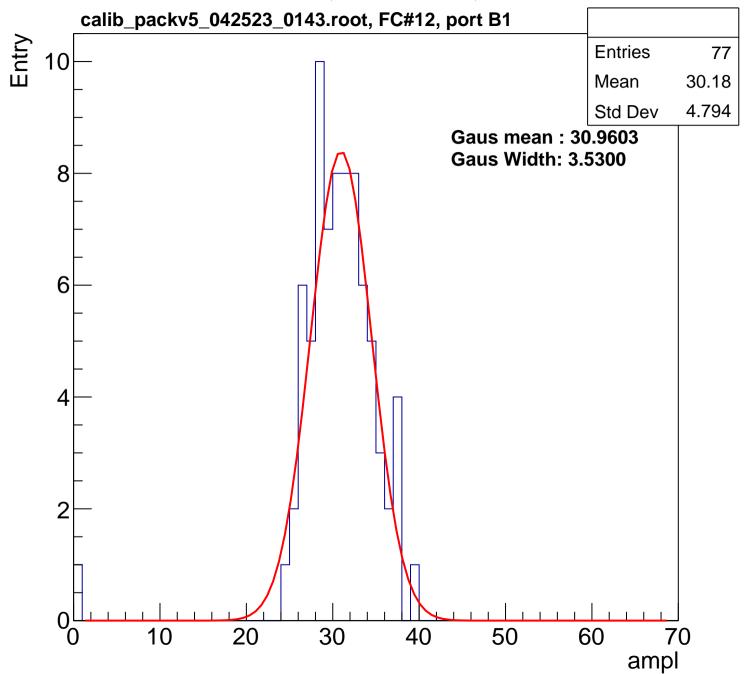


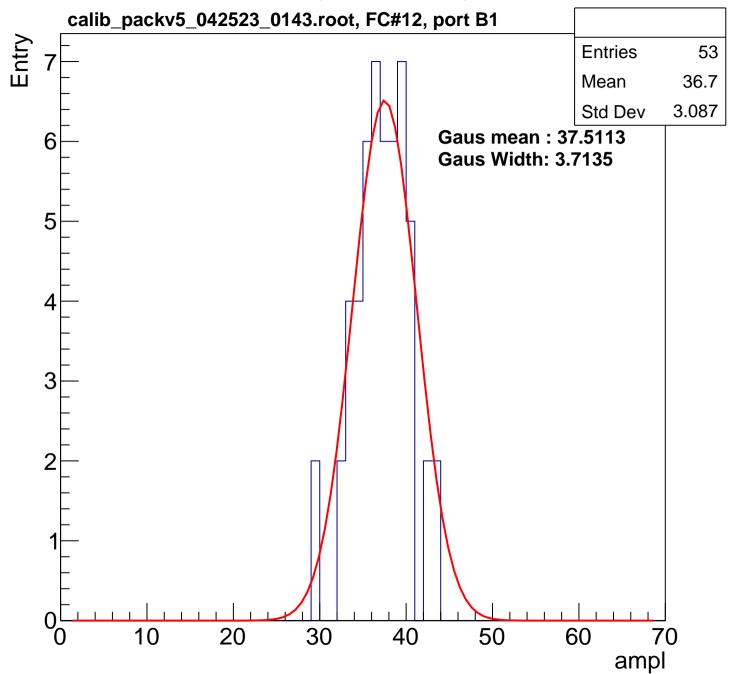


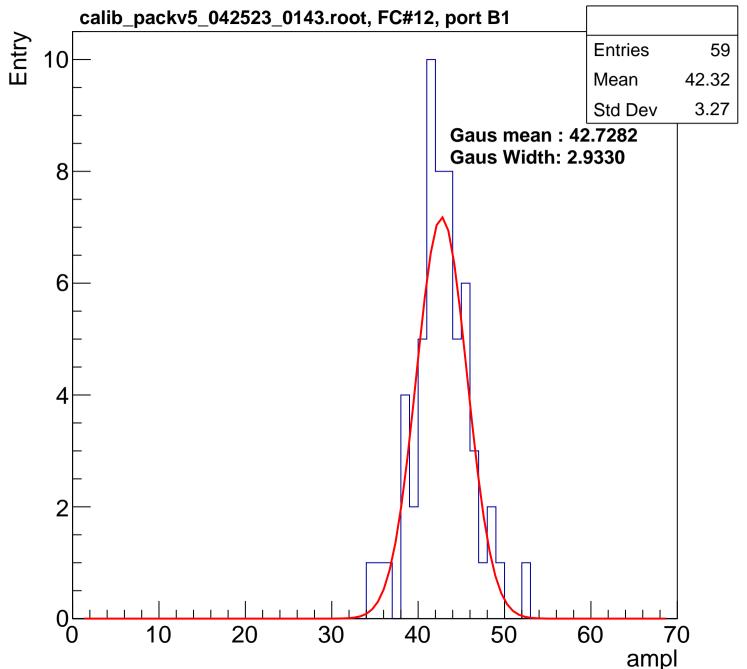


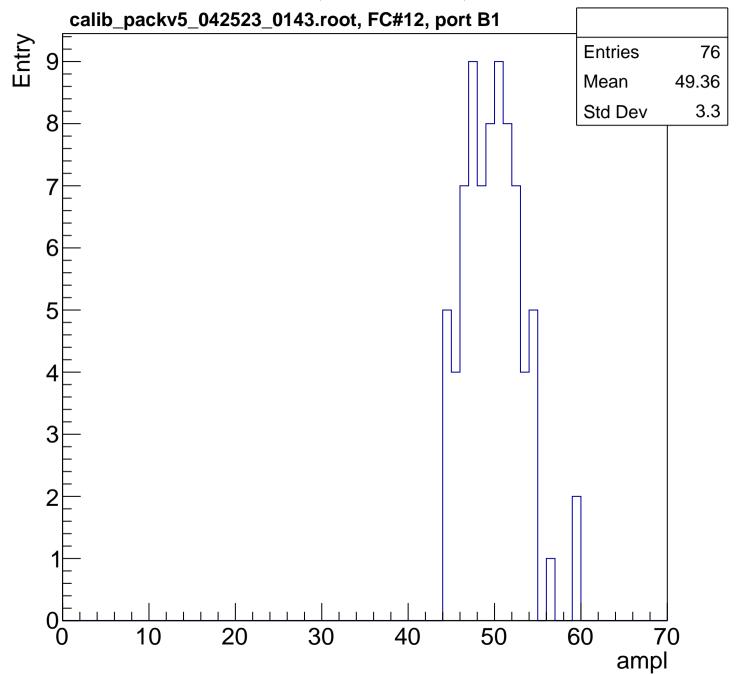
B0L102S, U4-ch38, adc7 calib_packv5_042523_0143.root, FC#12, port B1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70

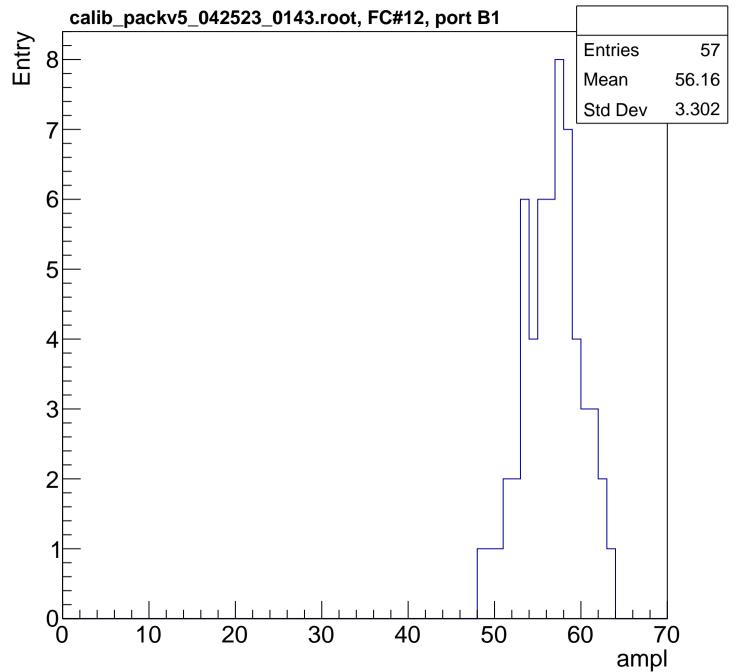
ampl

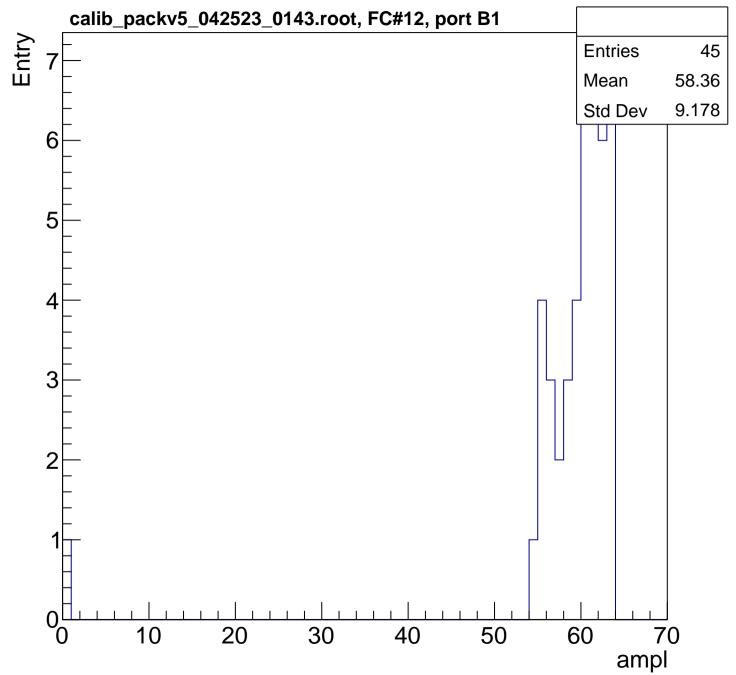


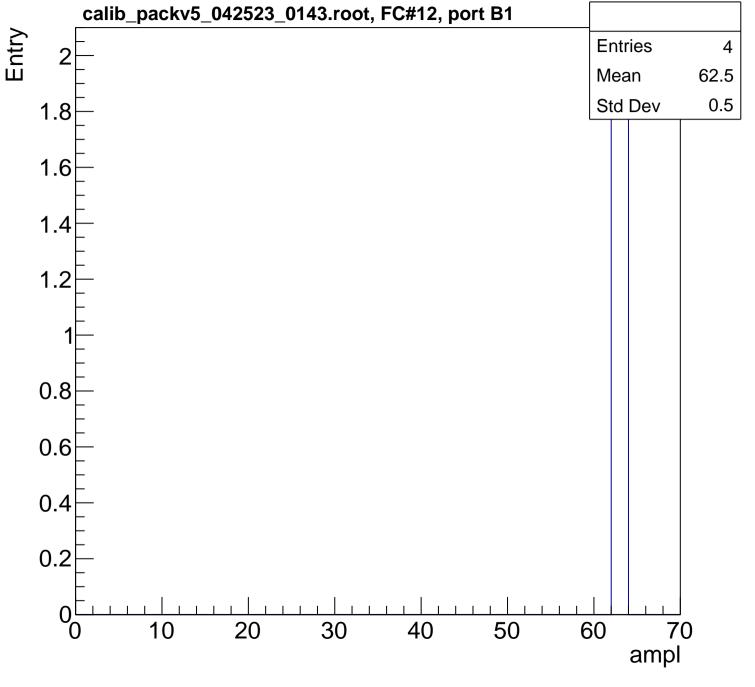


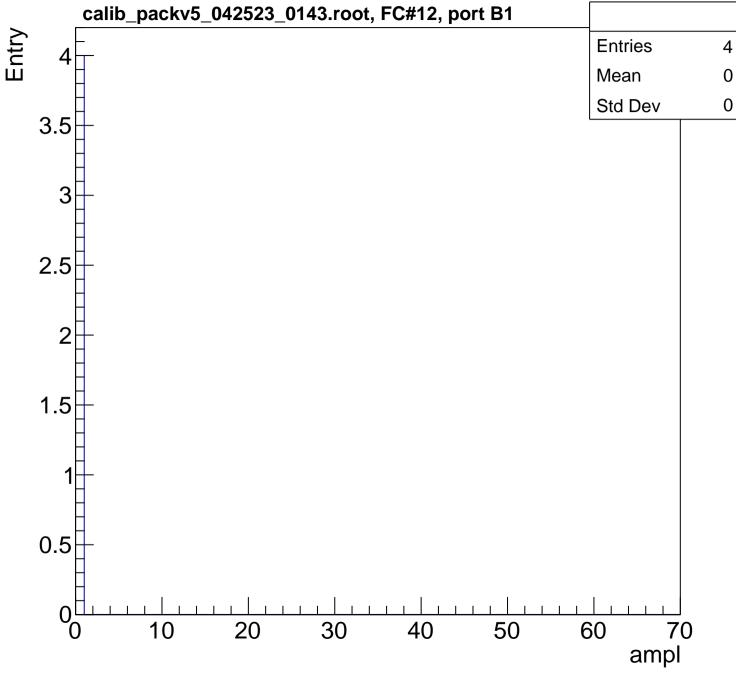


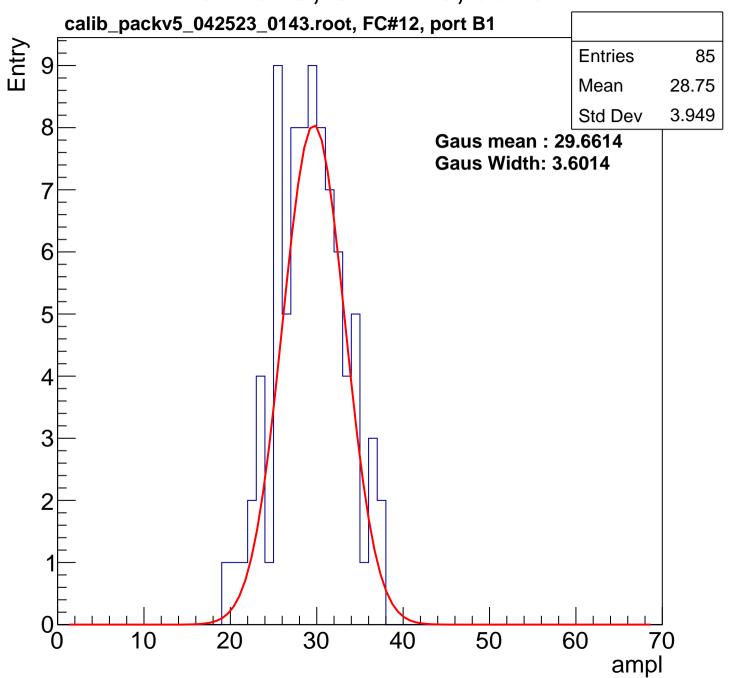


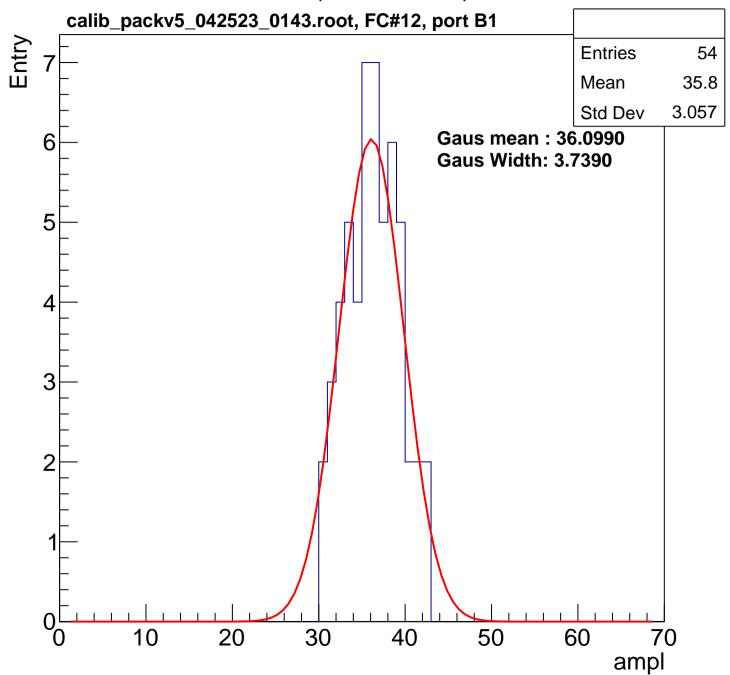


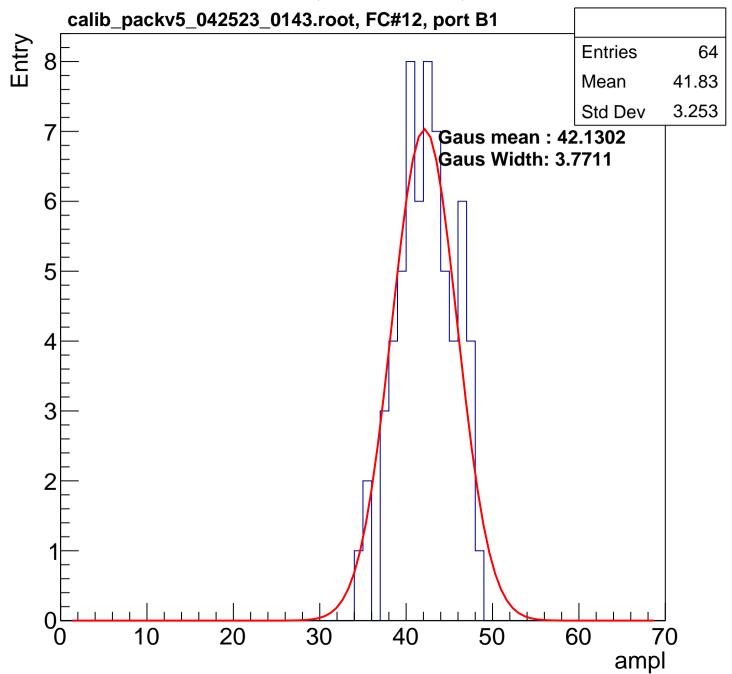


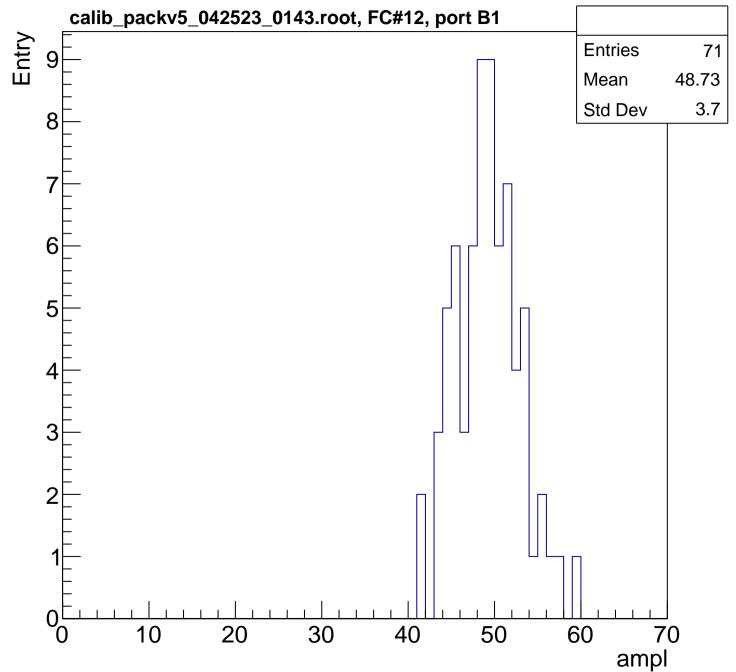


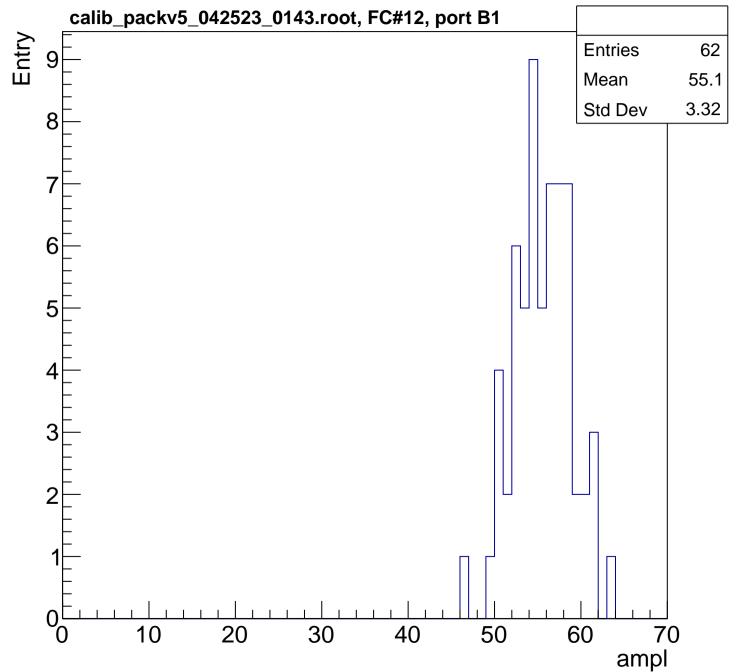


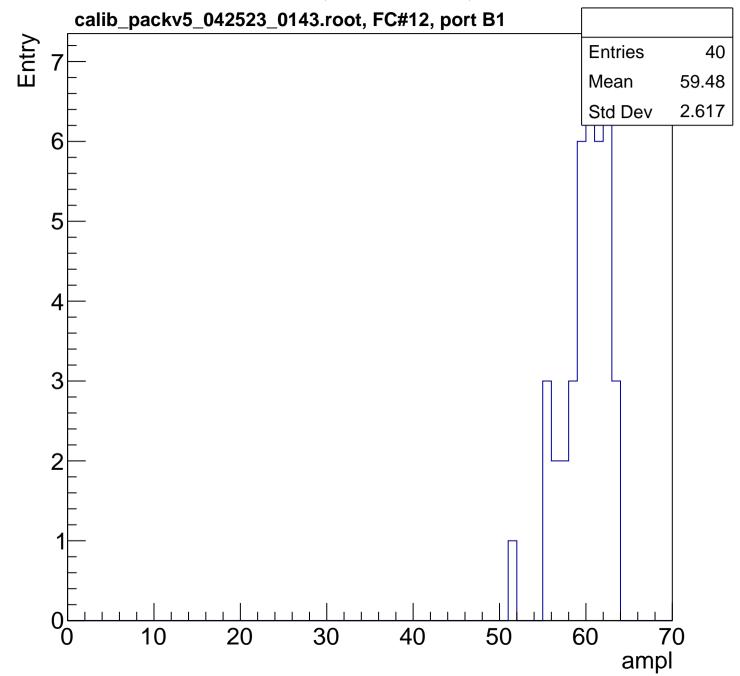


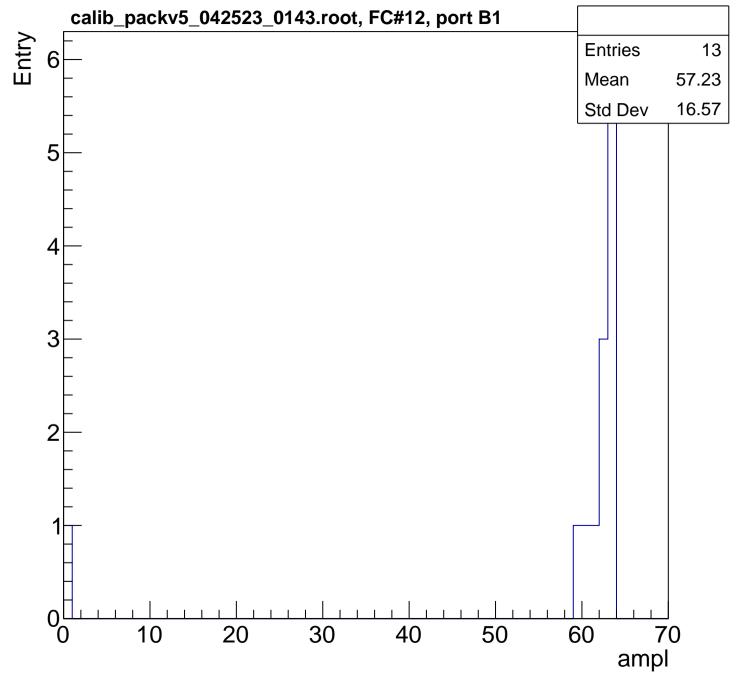




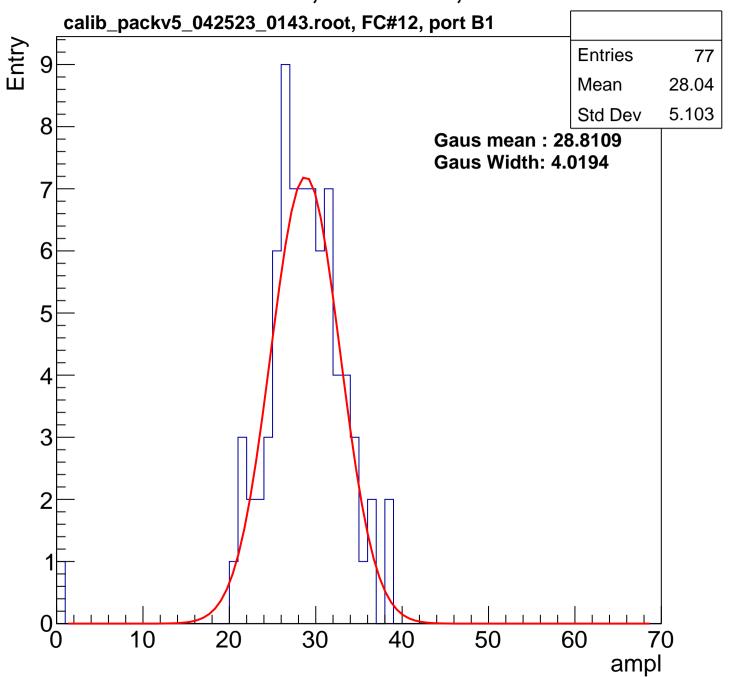


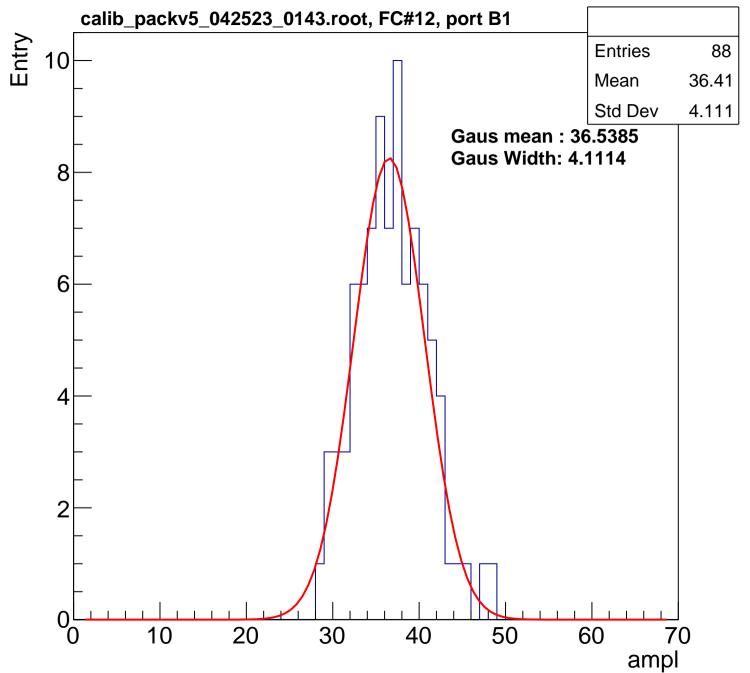


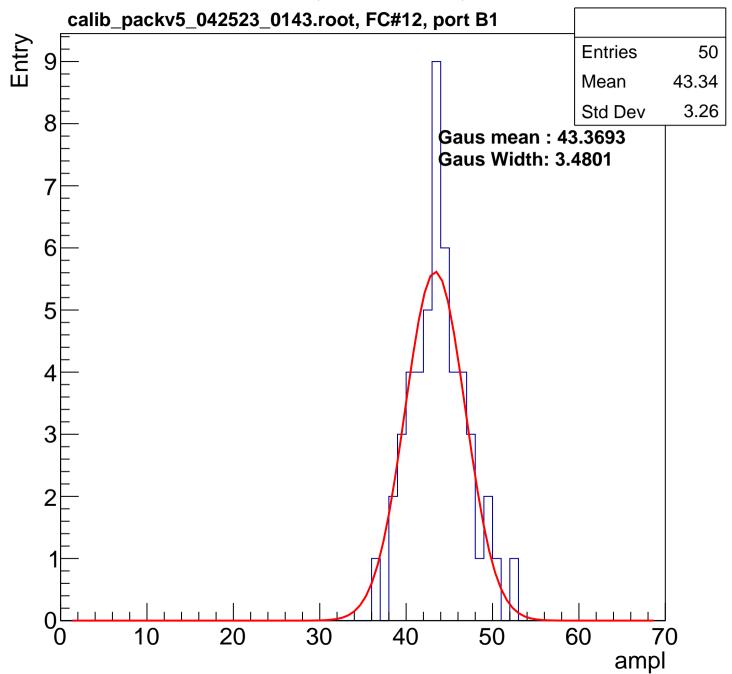


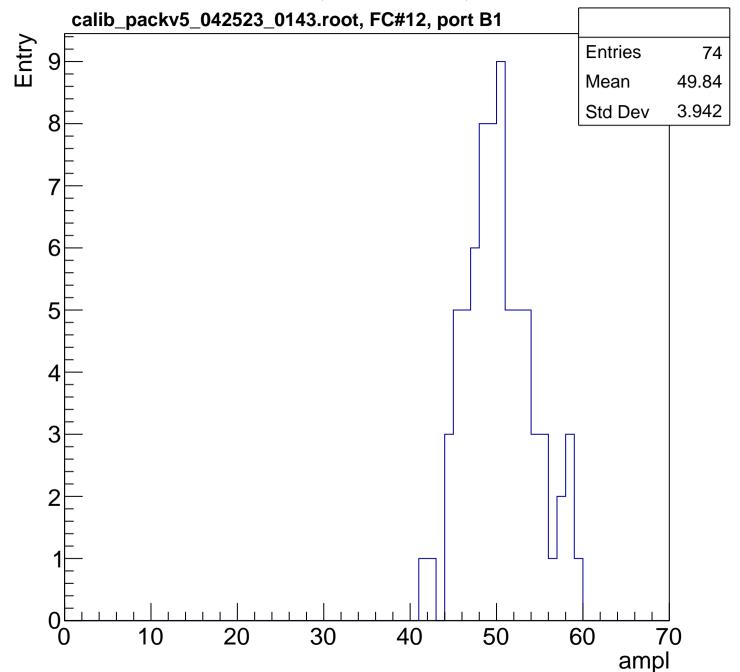


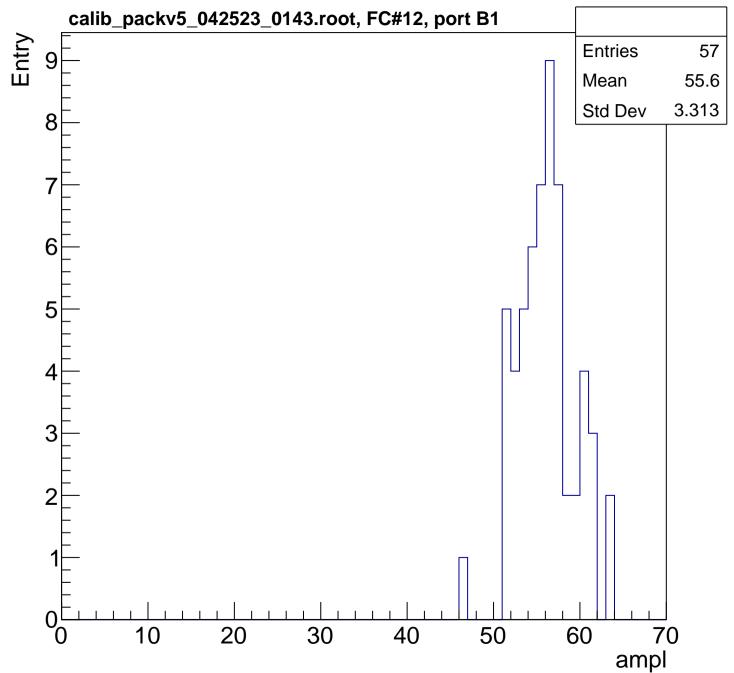


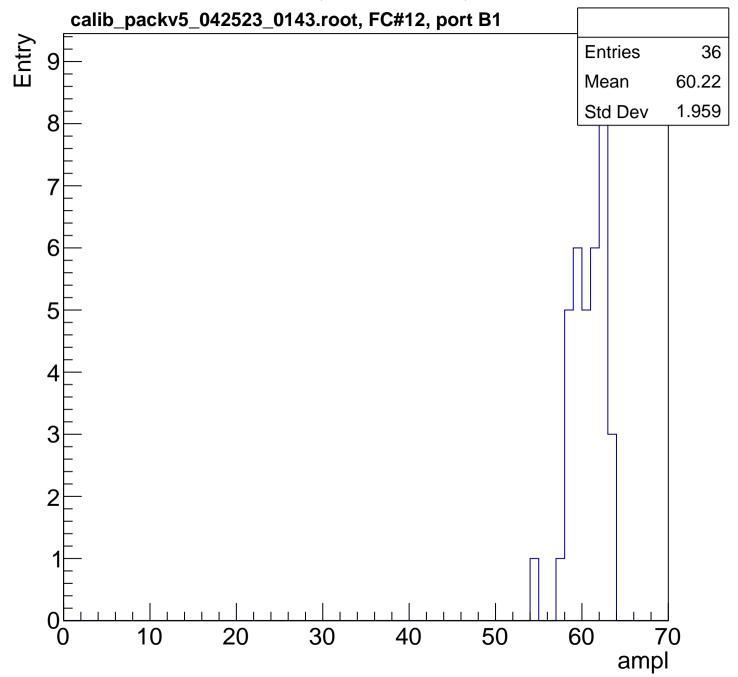


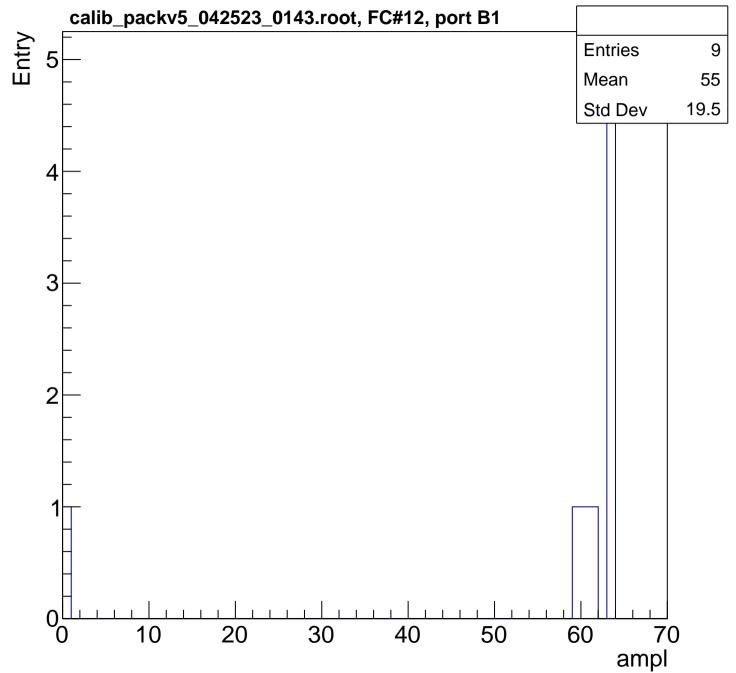


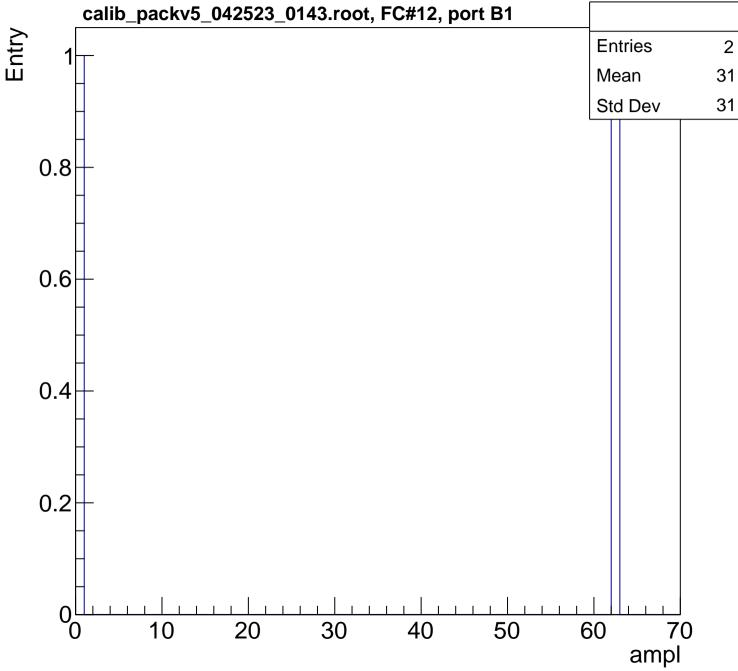


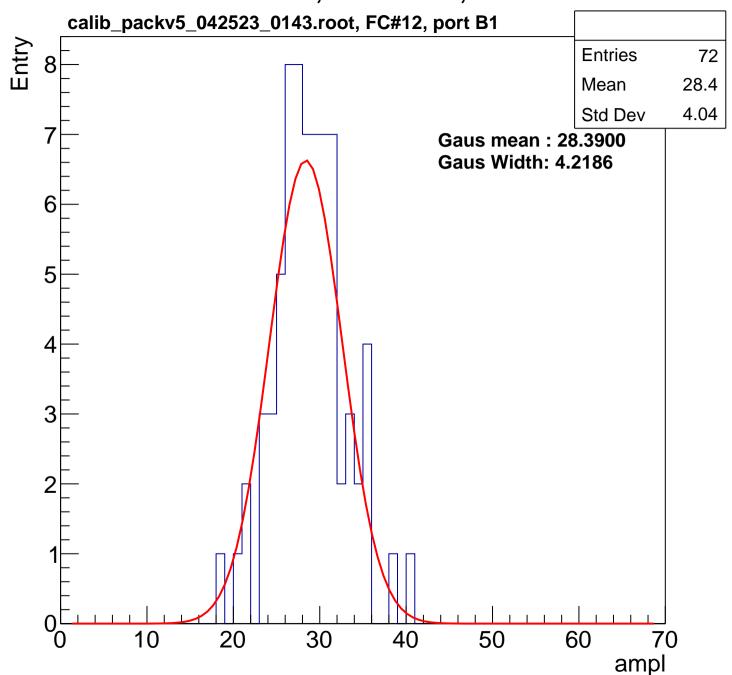


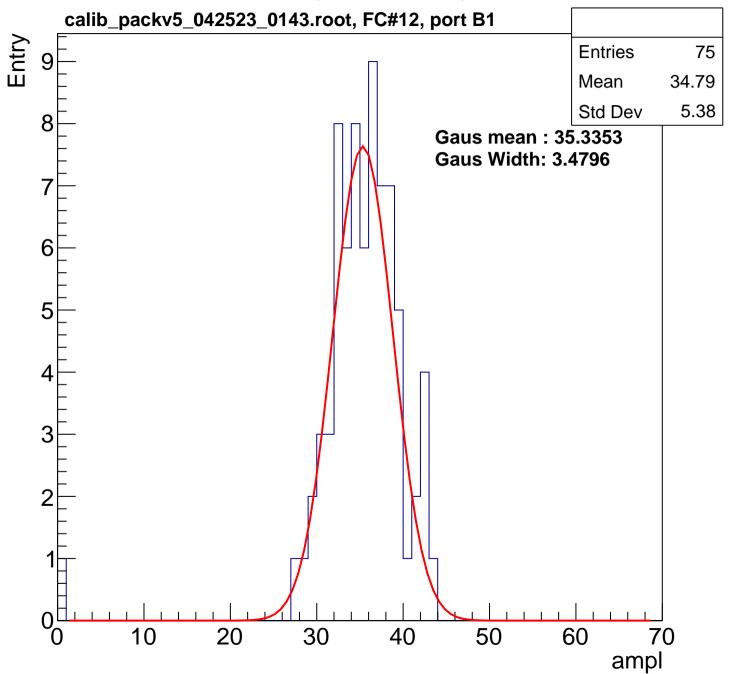


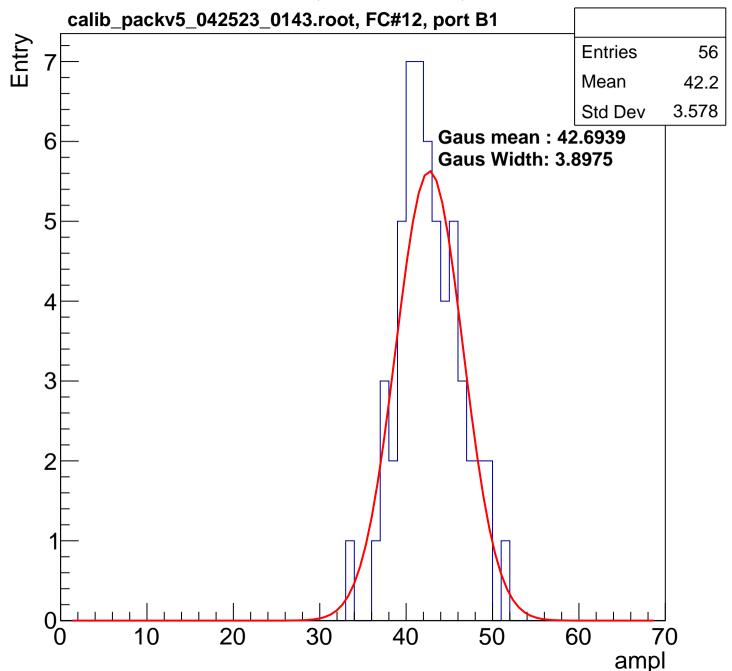


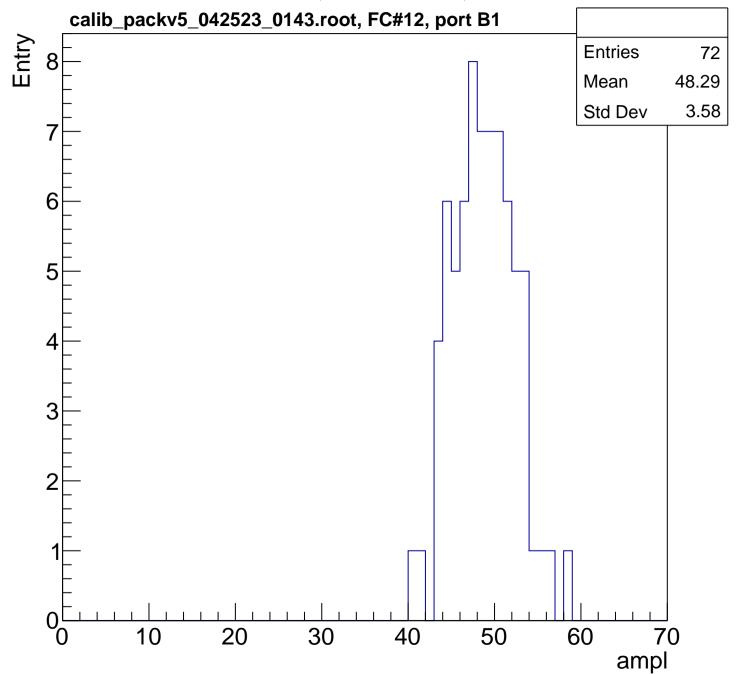


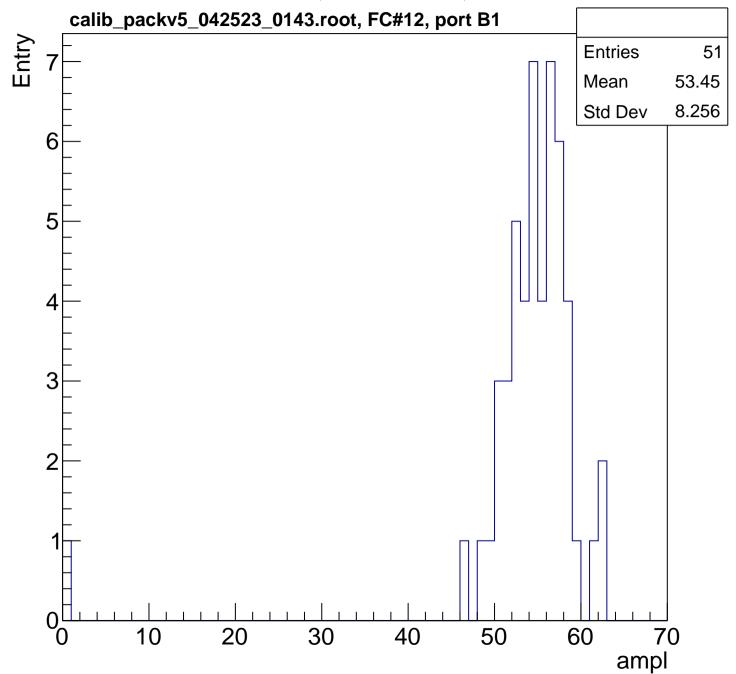


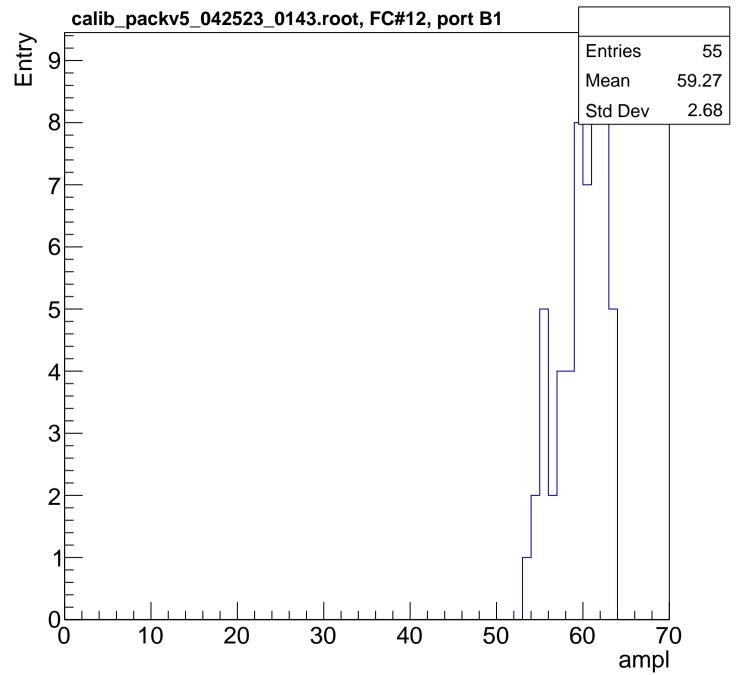


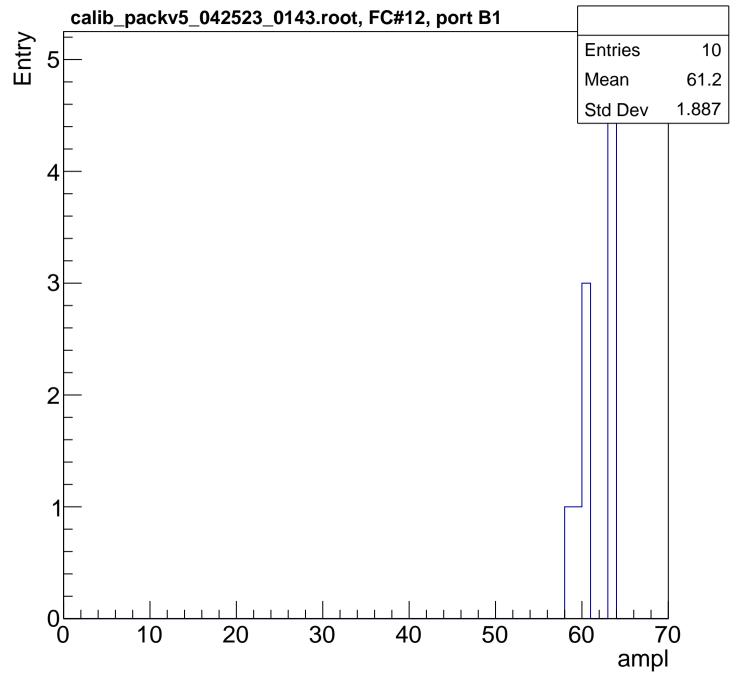


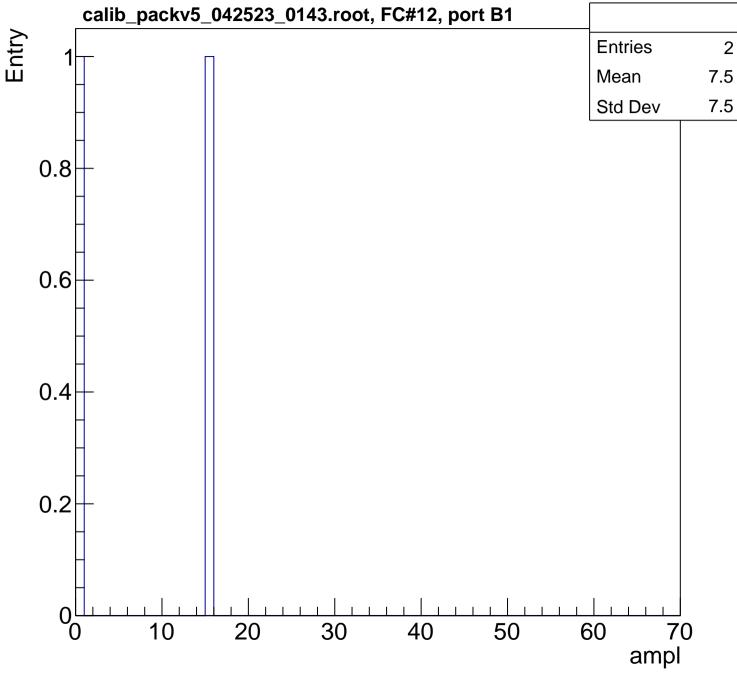


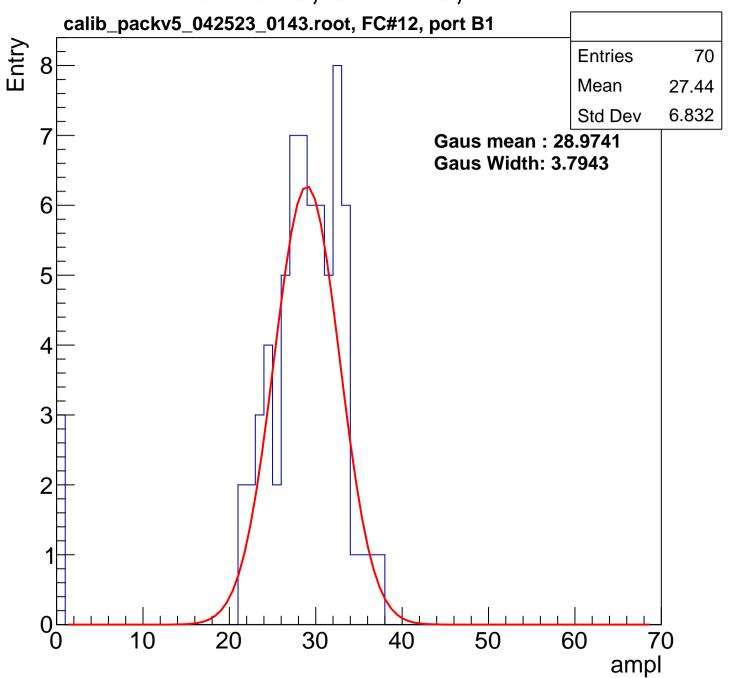


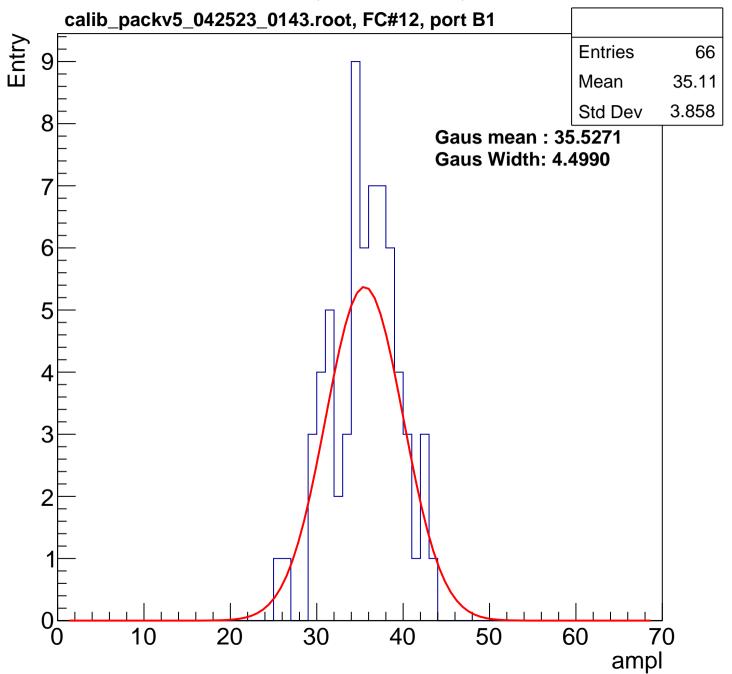


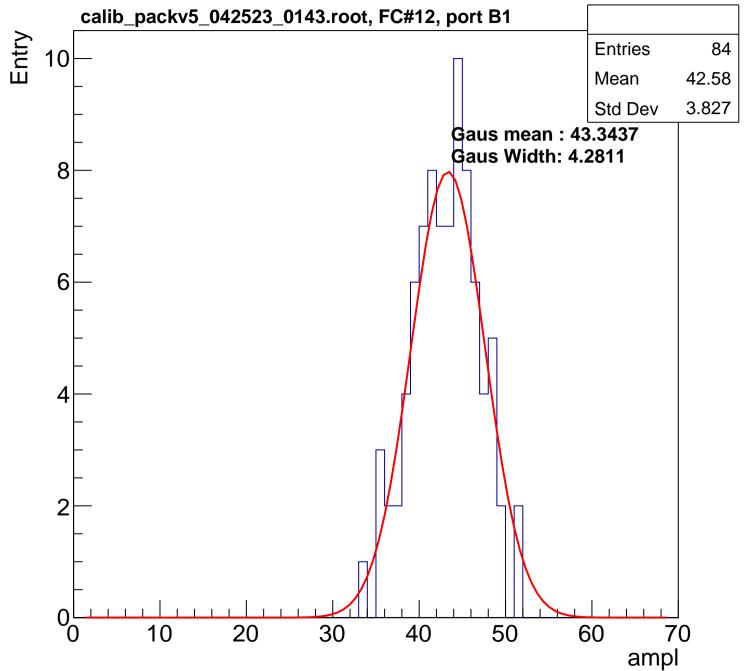


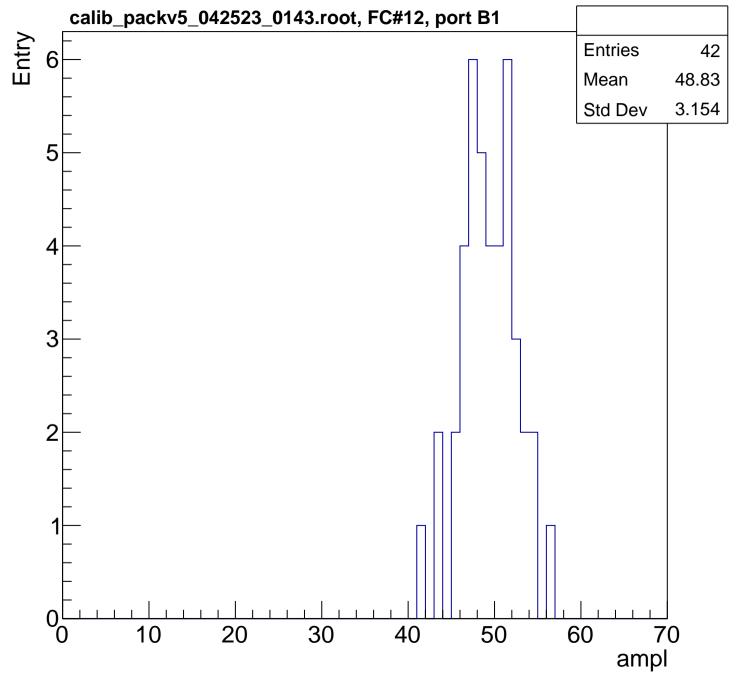


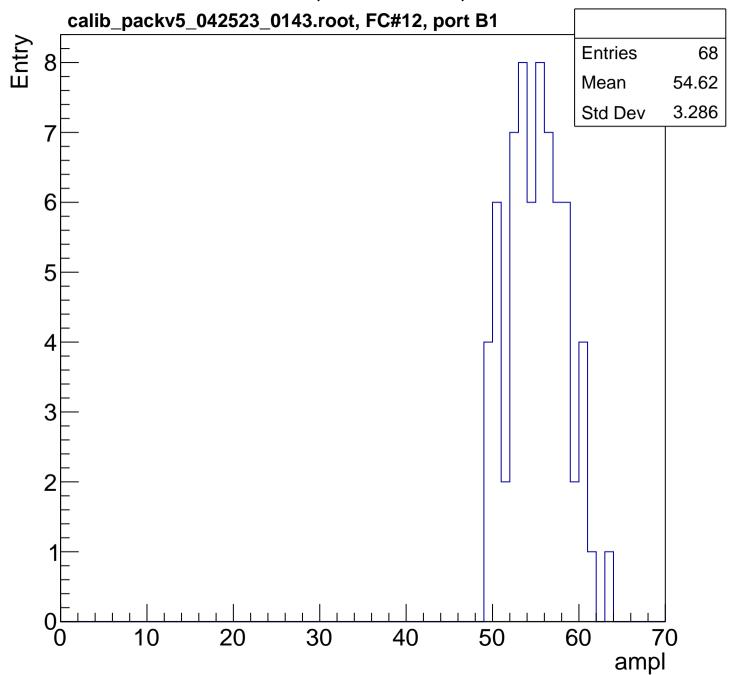


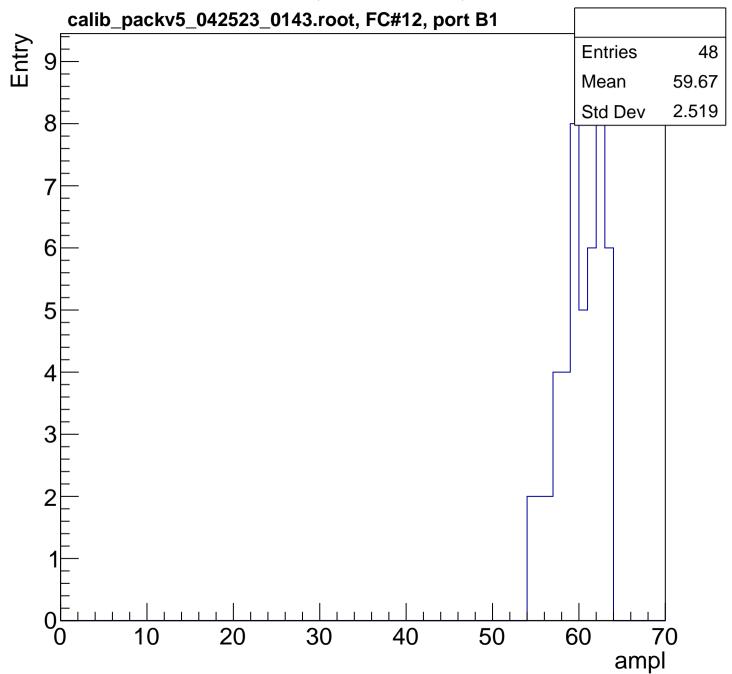


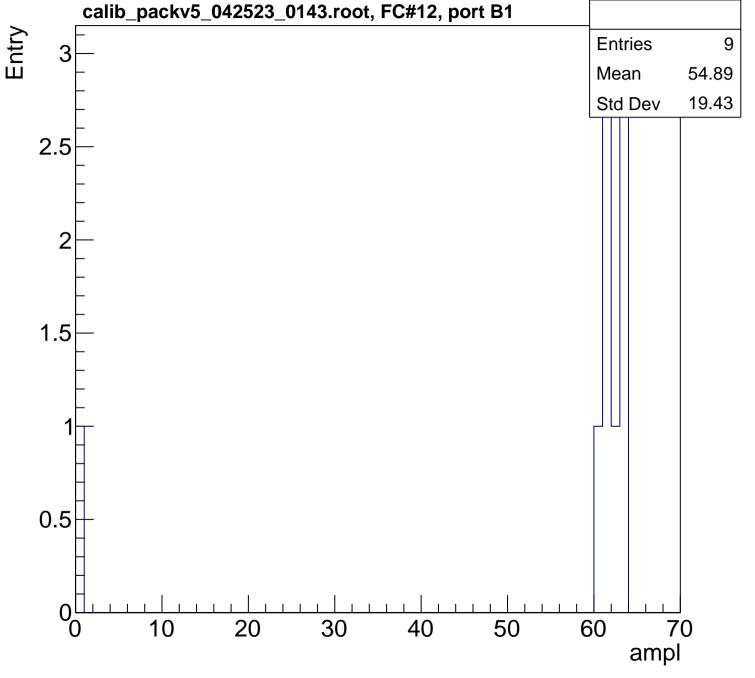


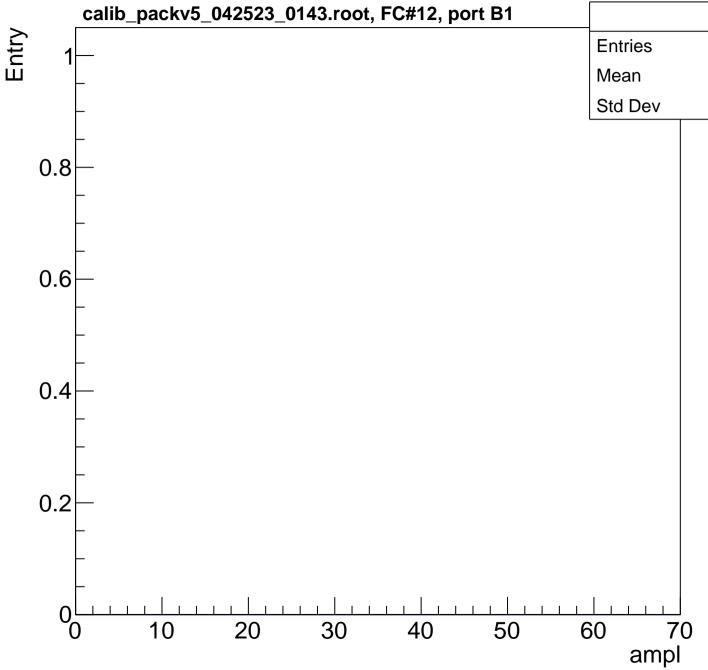


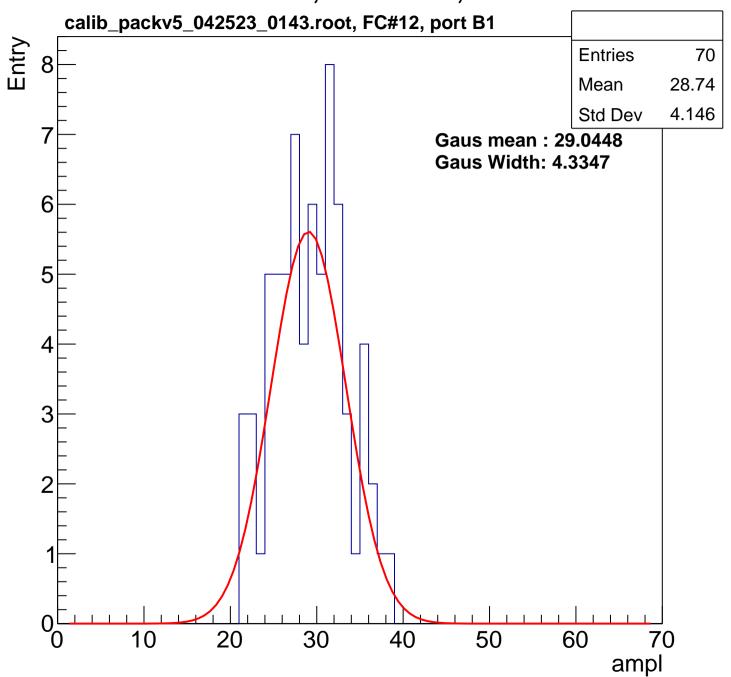


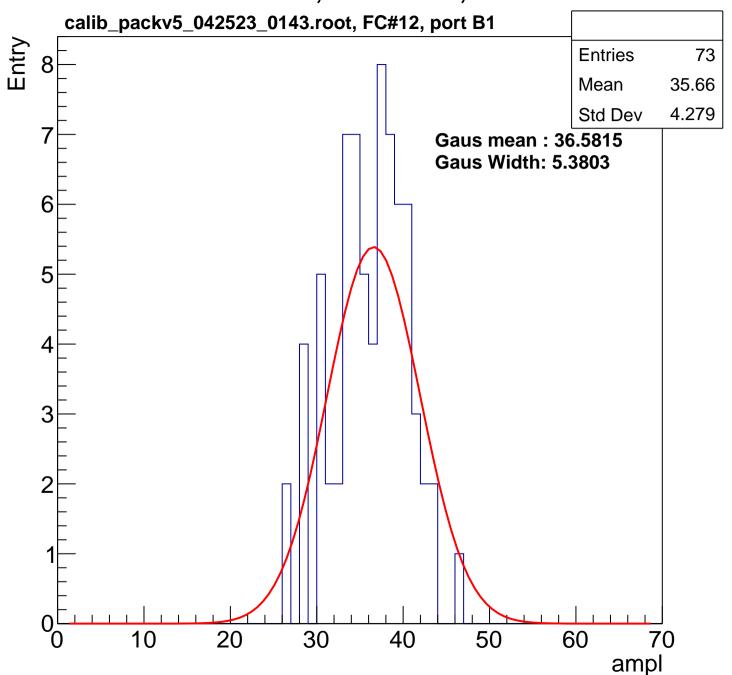


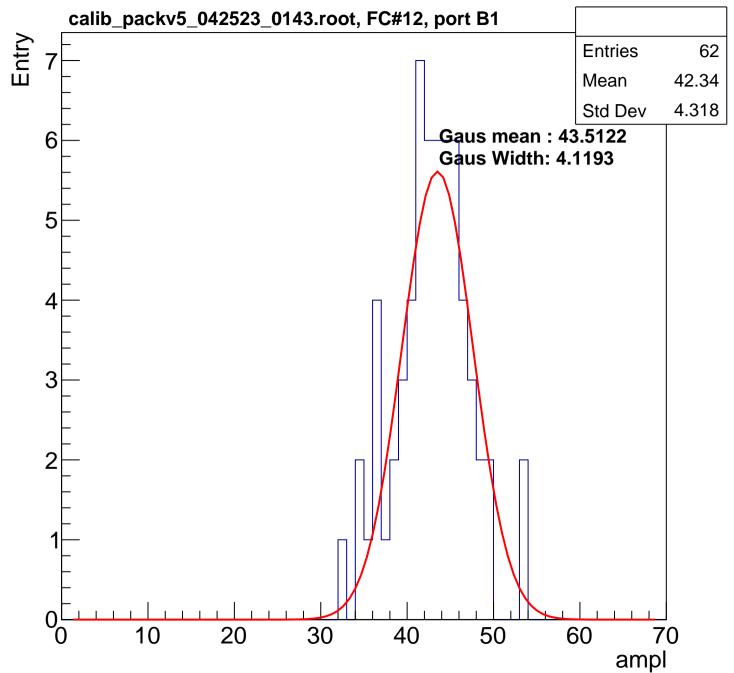


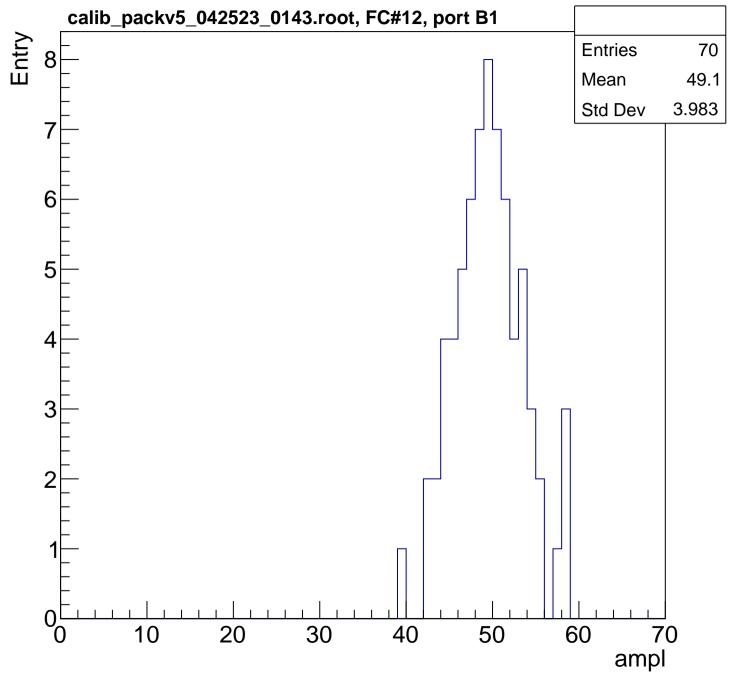


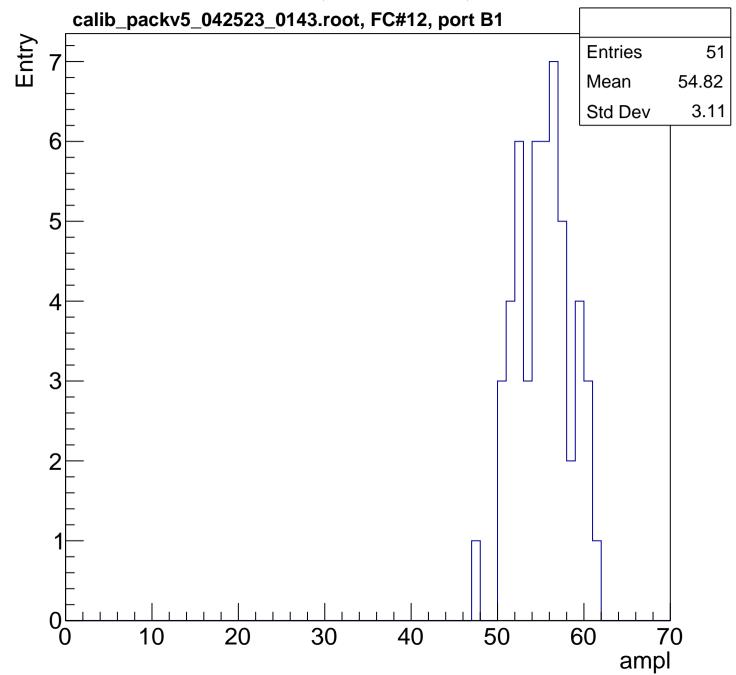


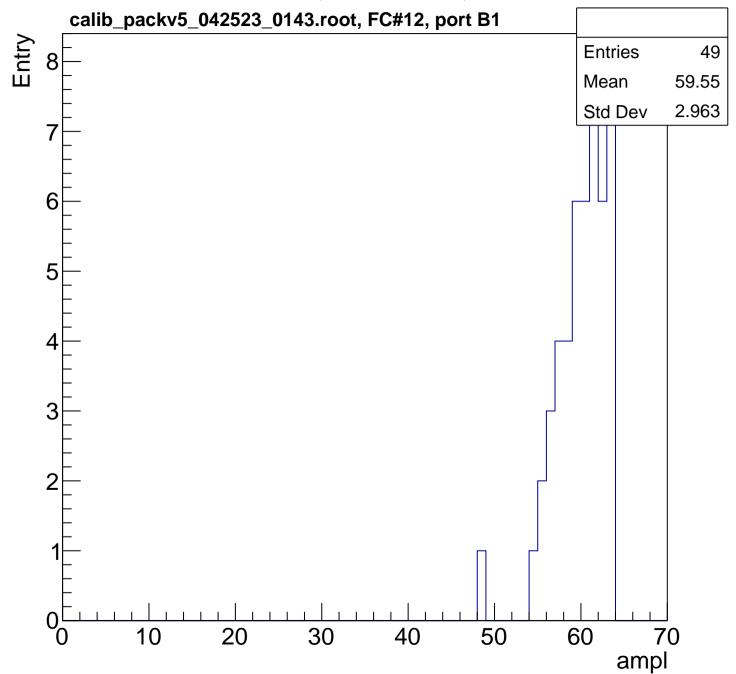


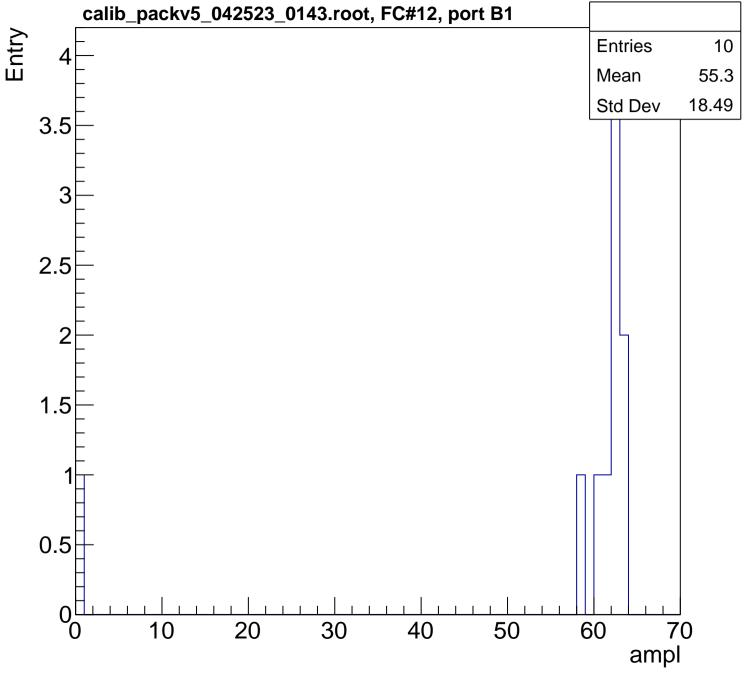












B0L102S, U4-ch44, adc7 calib_packv5_042523_0143.root, FC#12, port B1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2

30

40

50

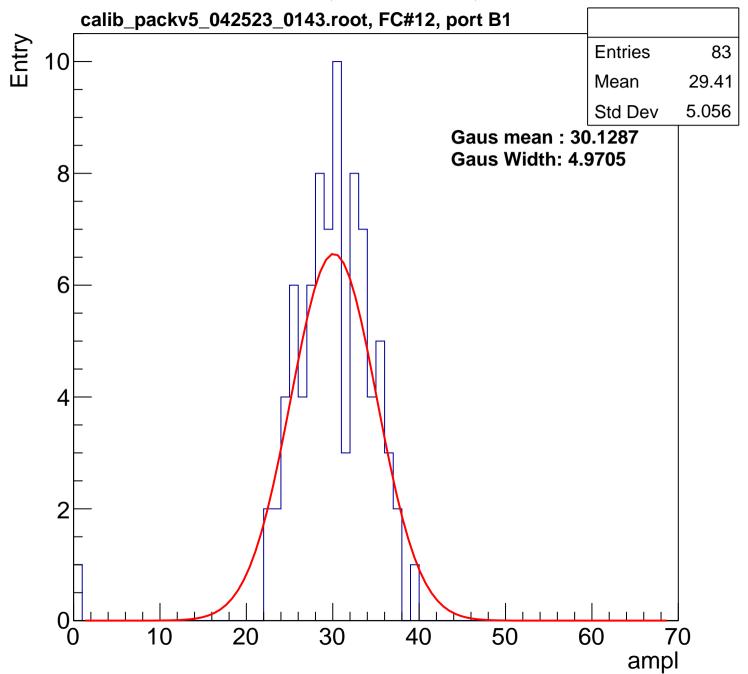
60

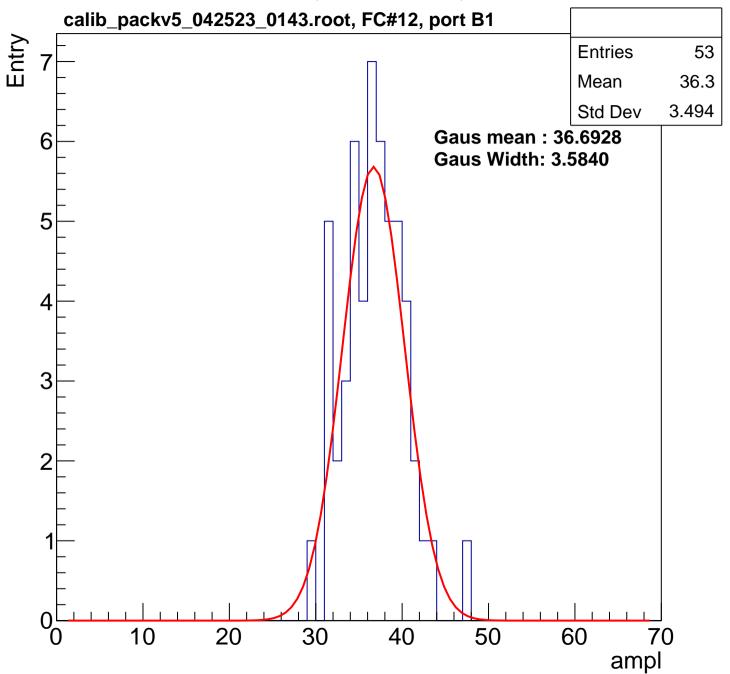
70

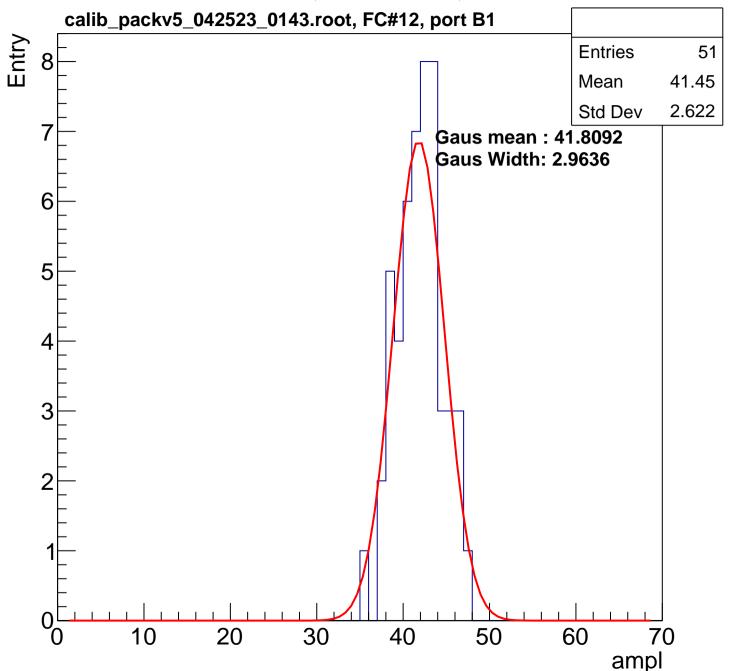
ampl

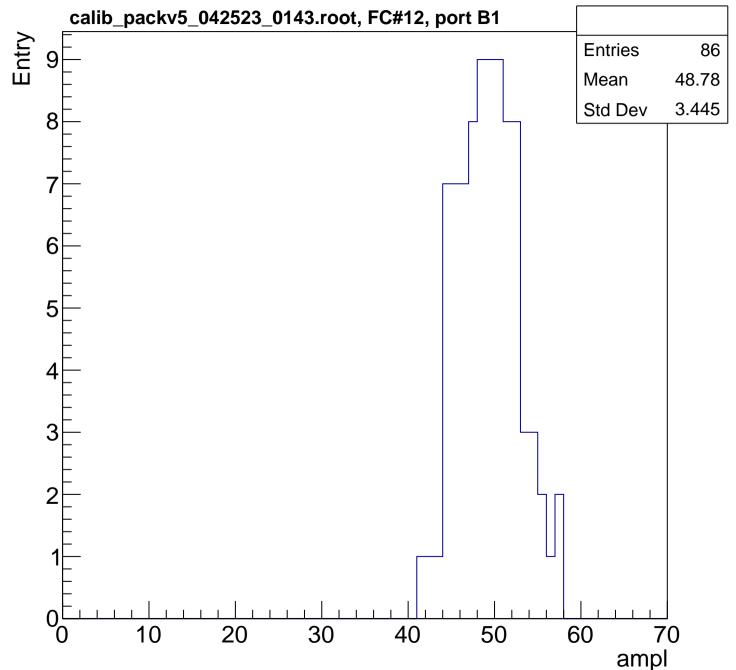
10

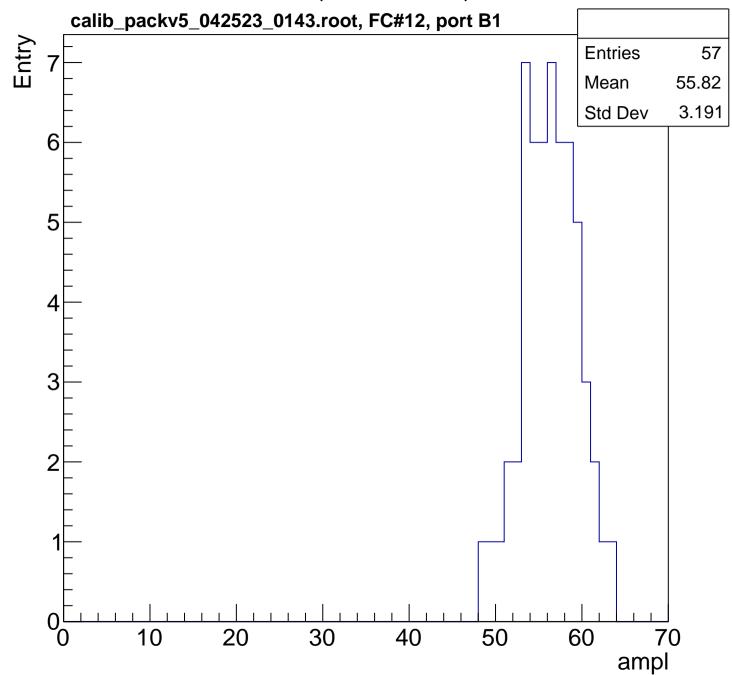
20

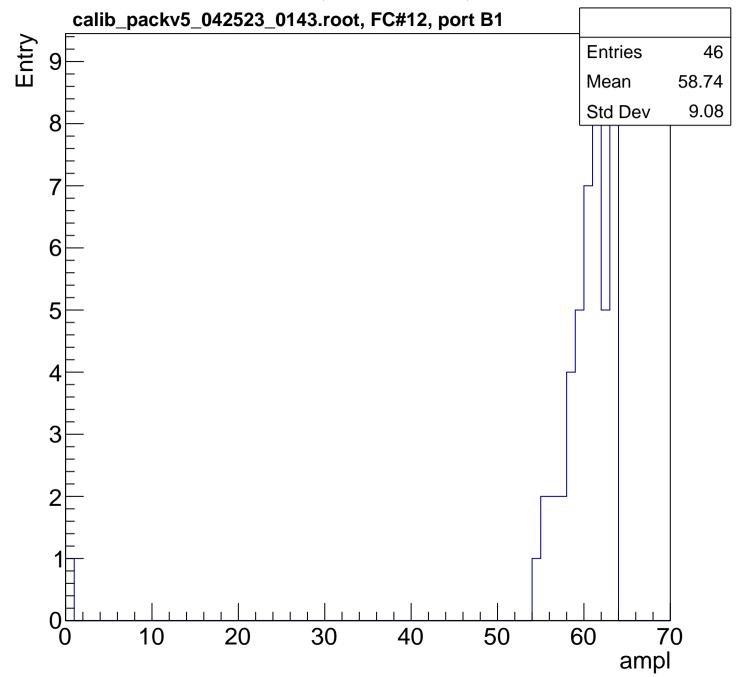


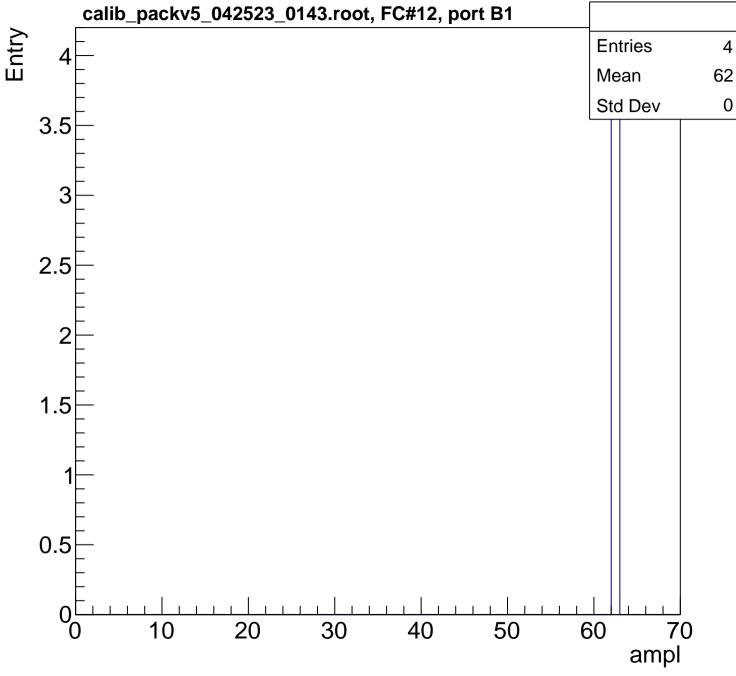




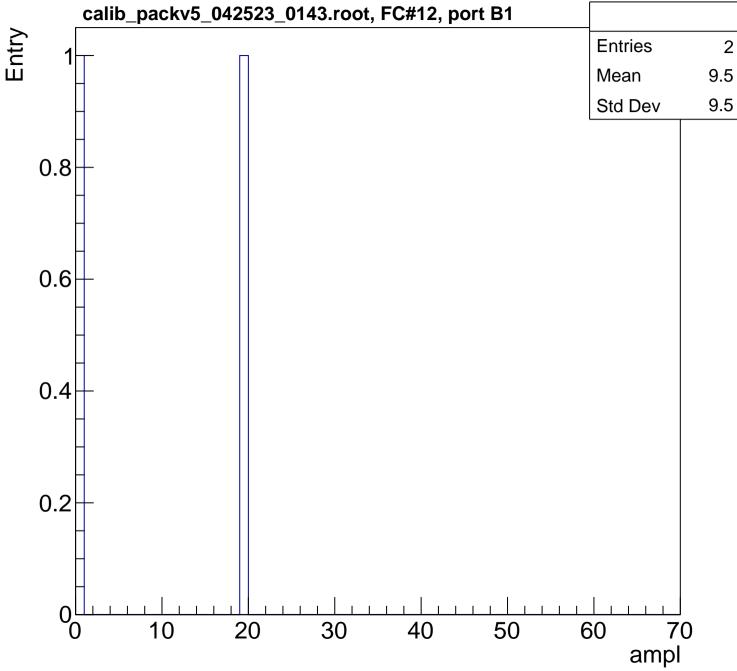


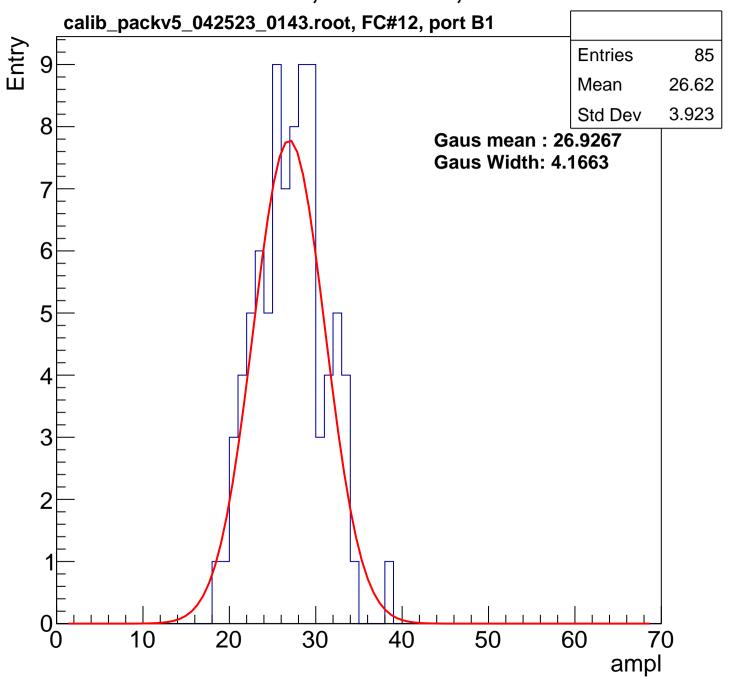


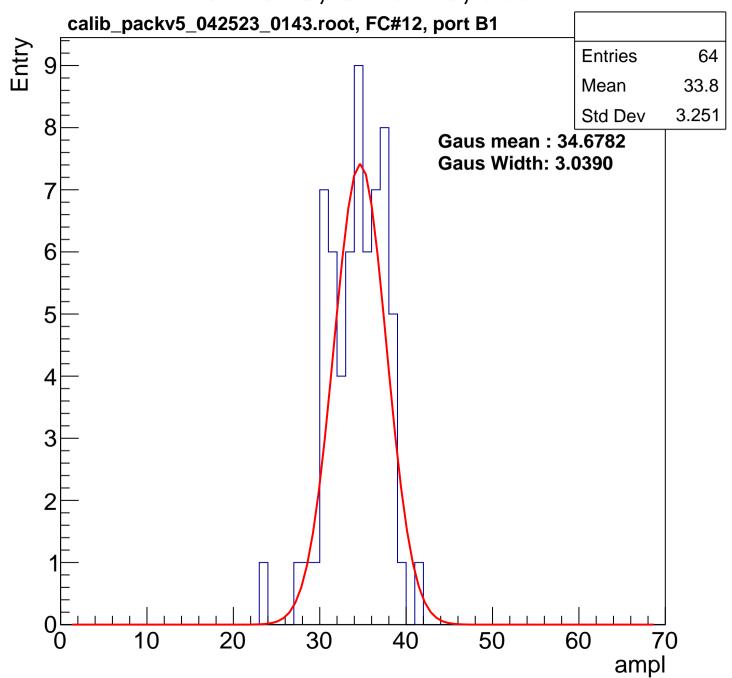


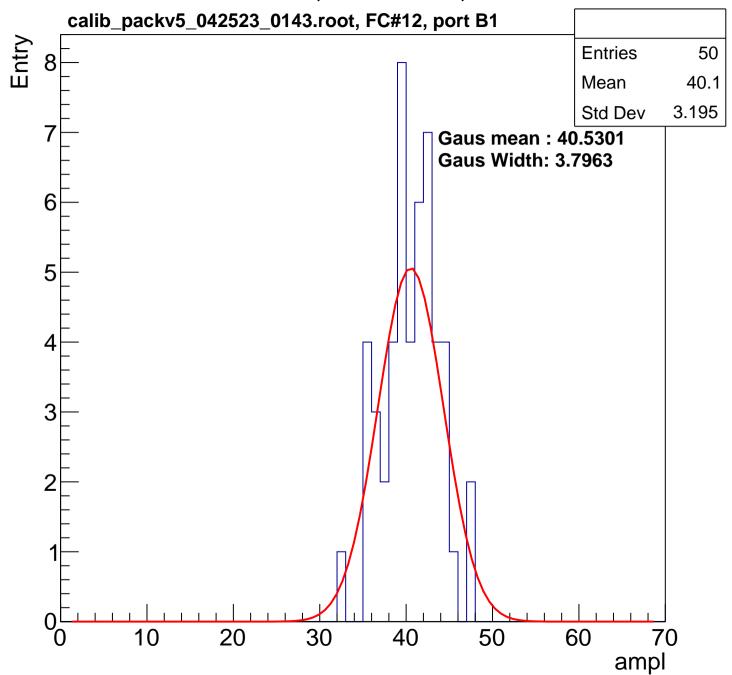


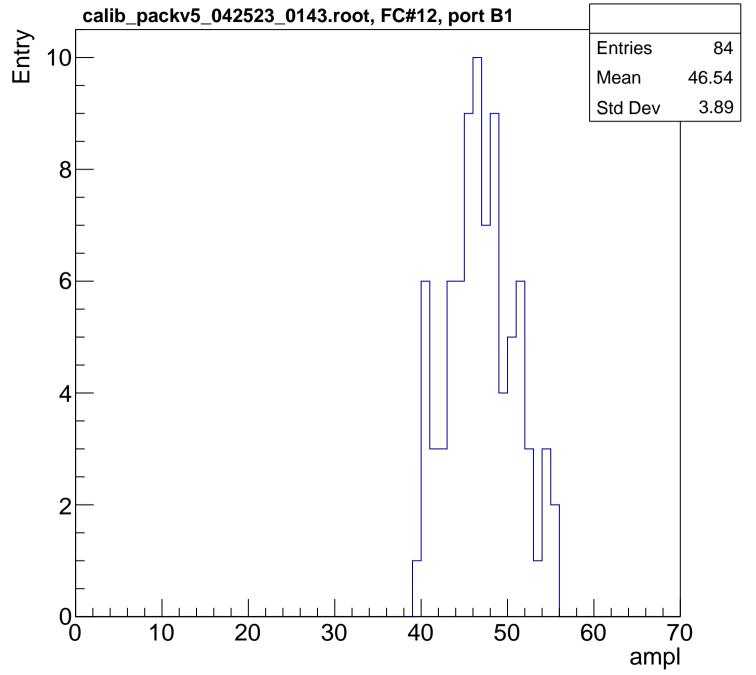
2

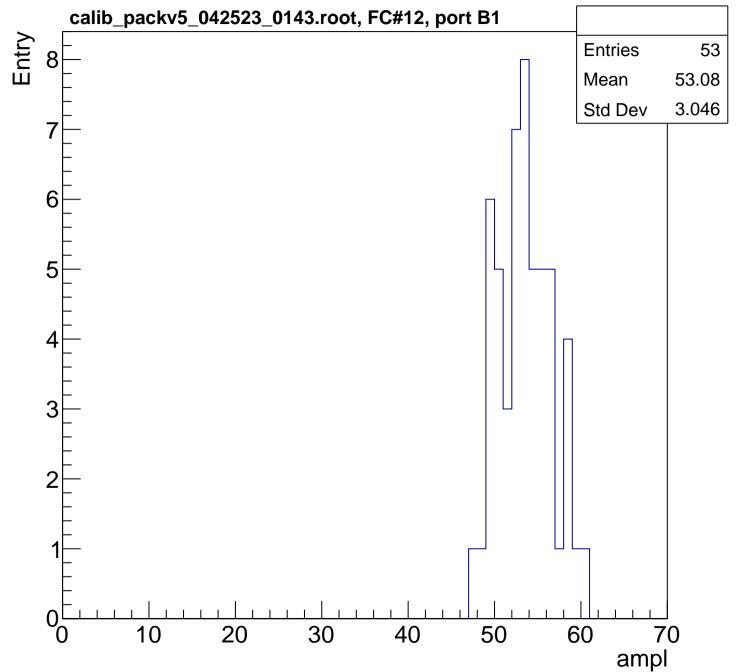


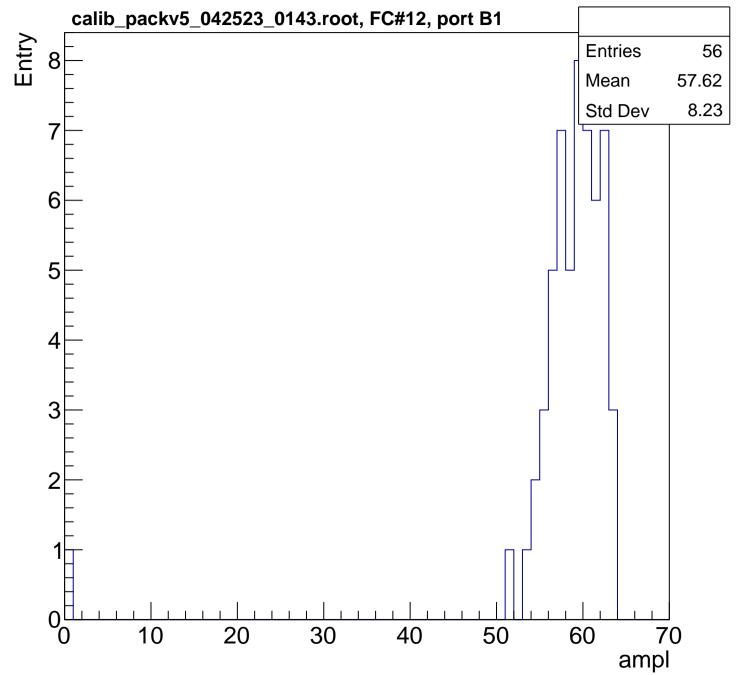


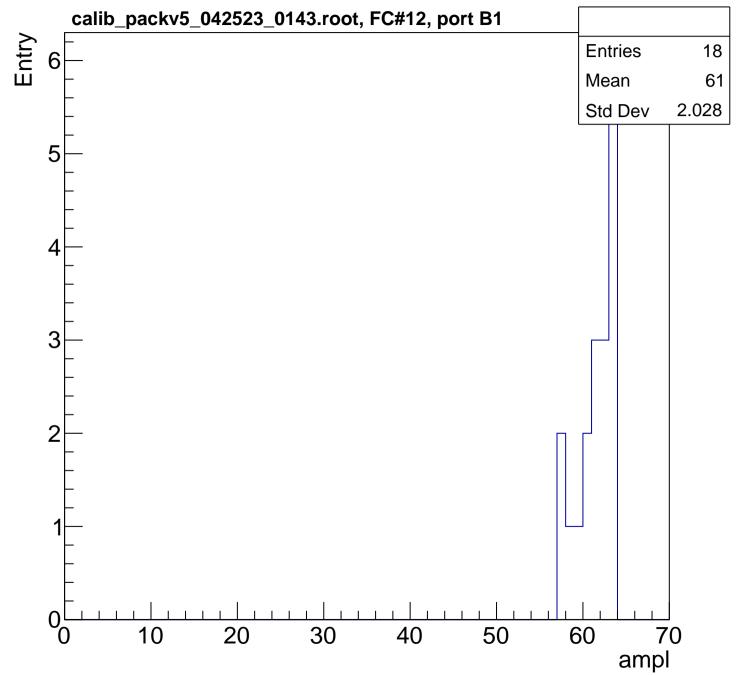


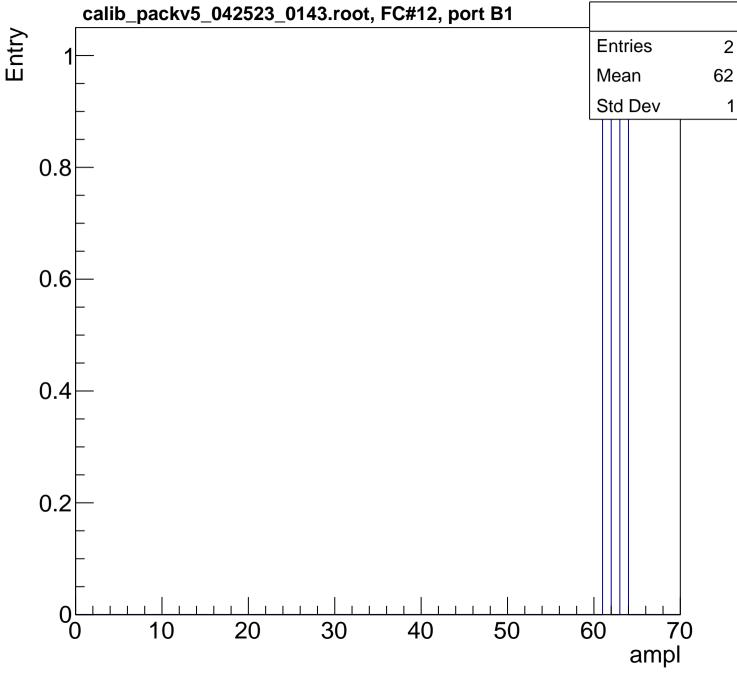


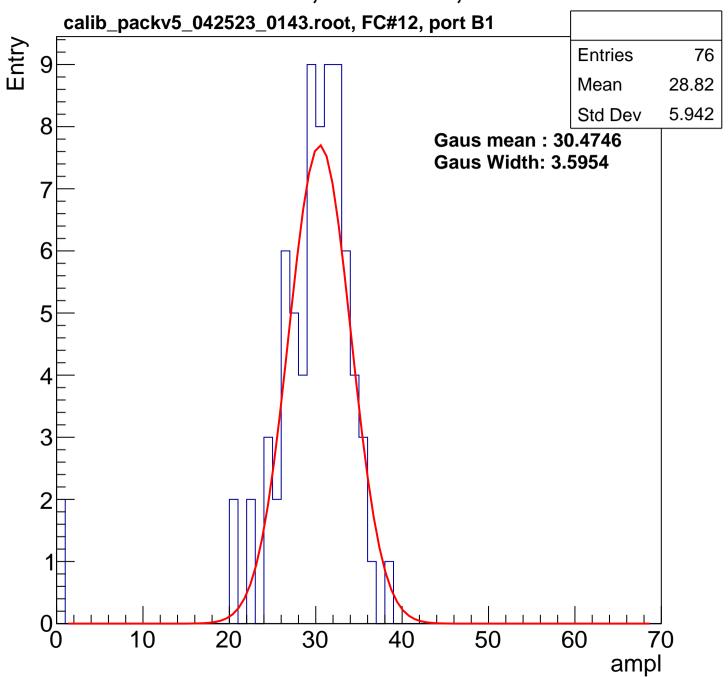


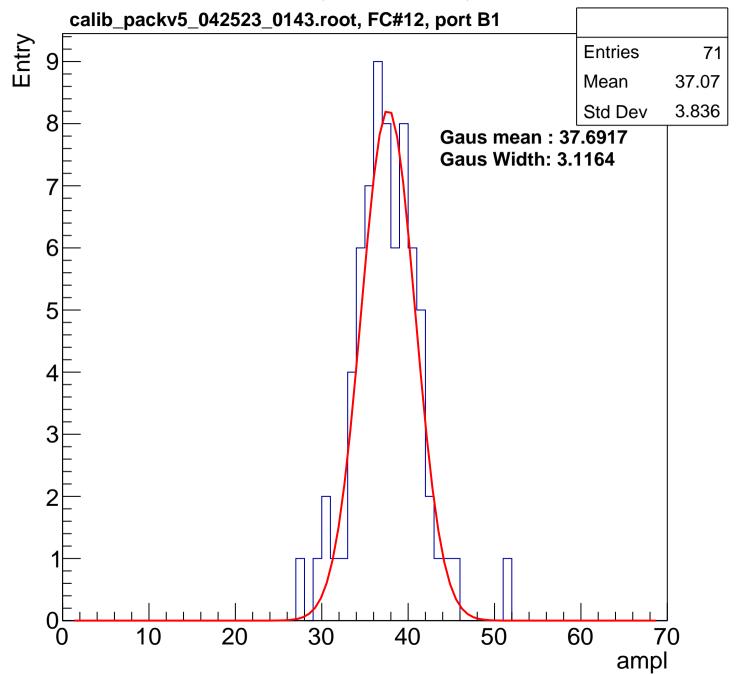


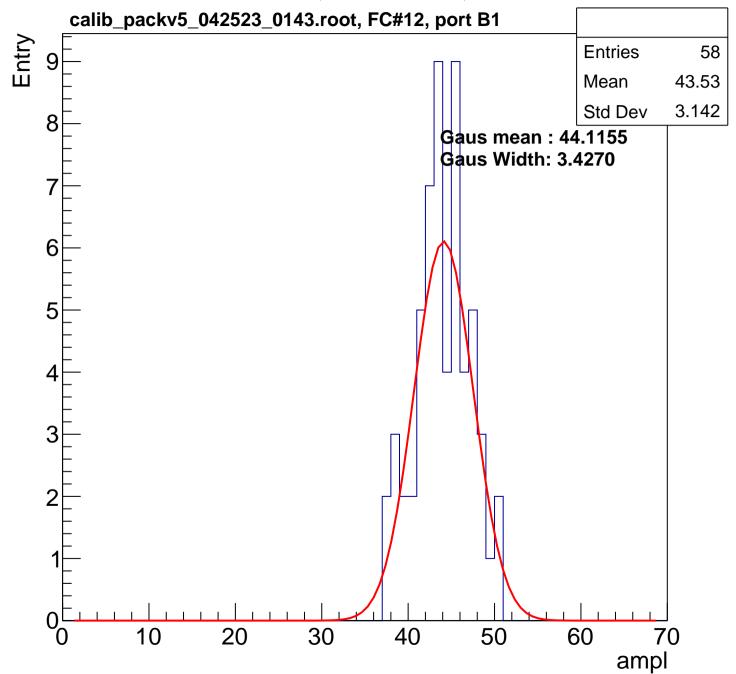


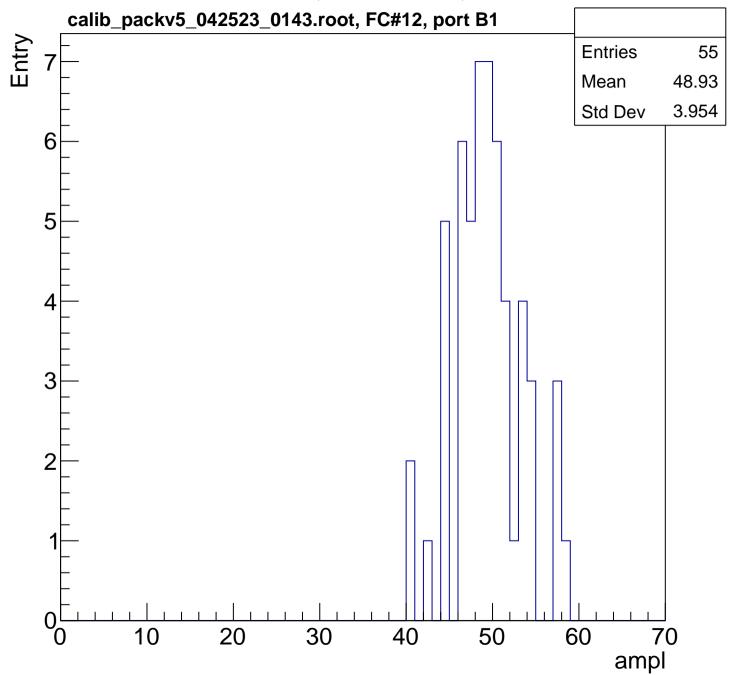


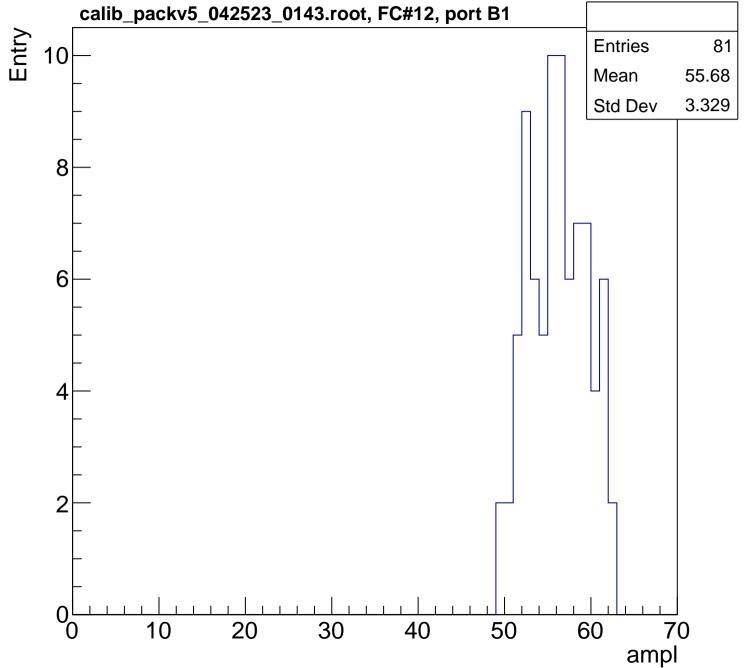


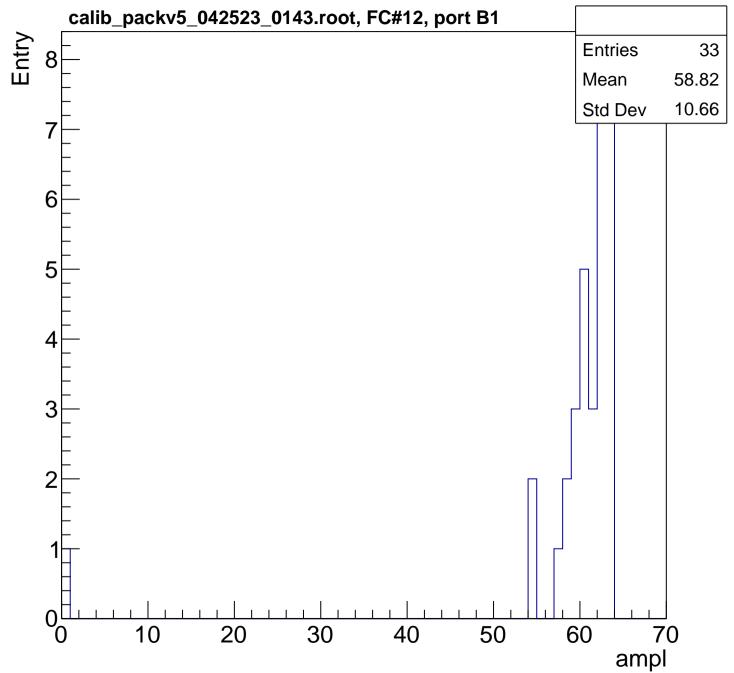


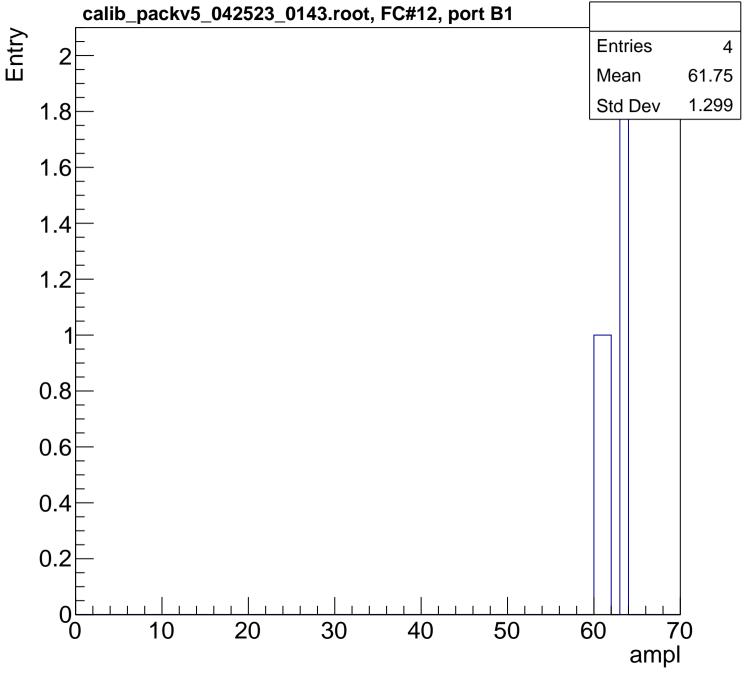


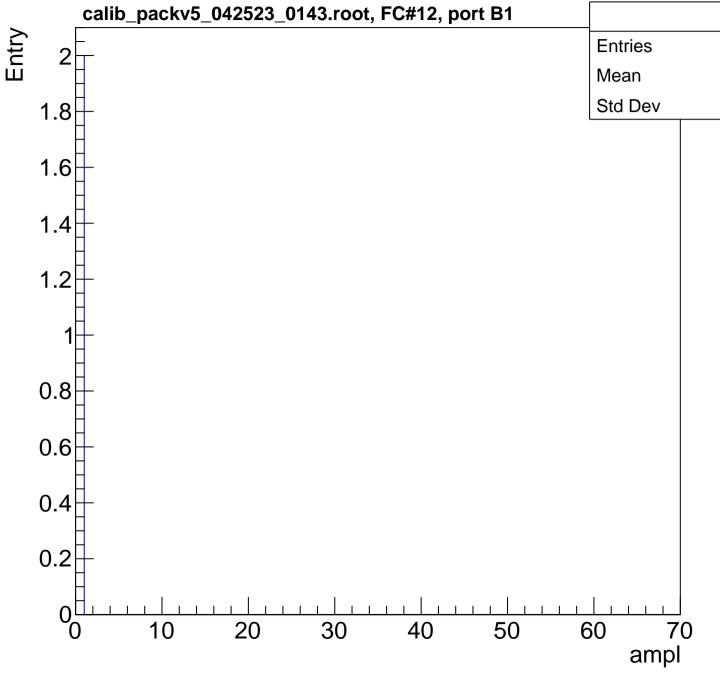


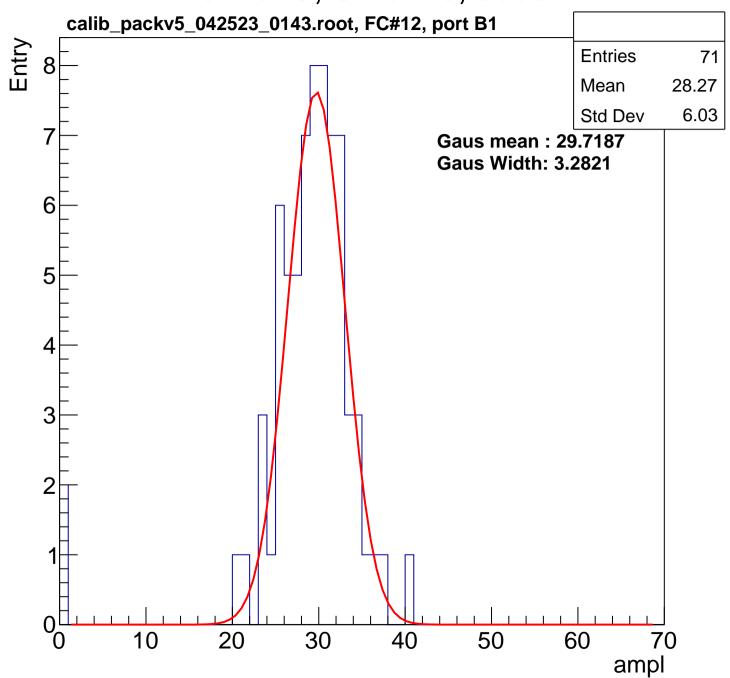


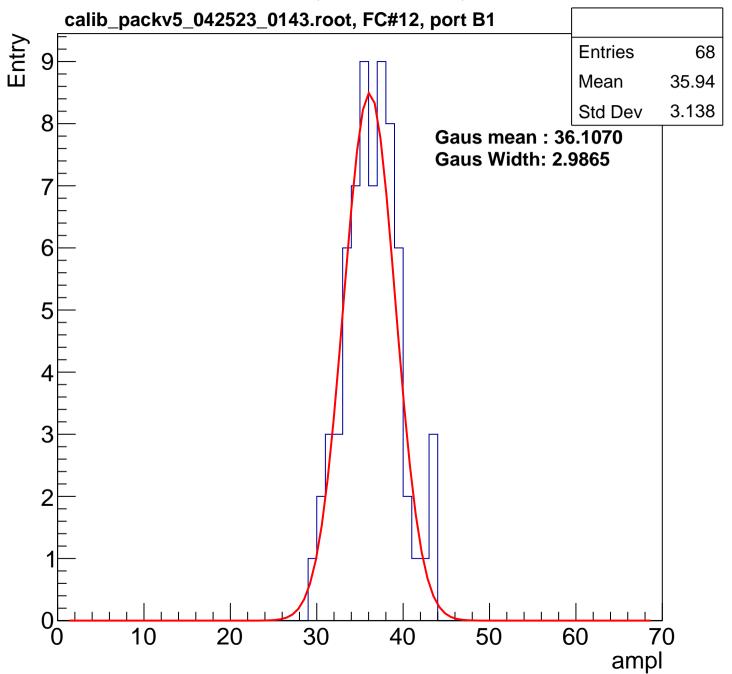


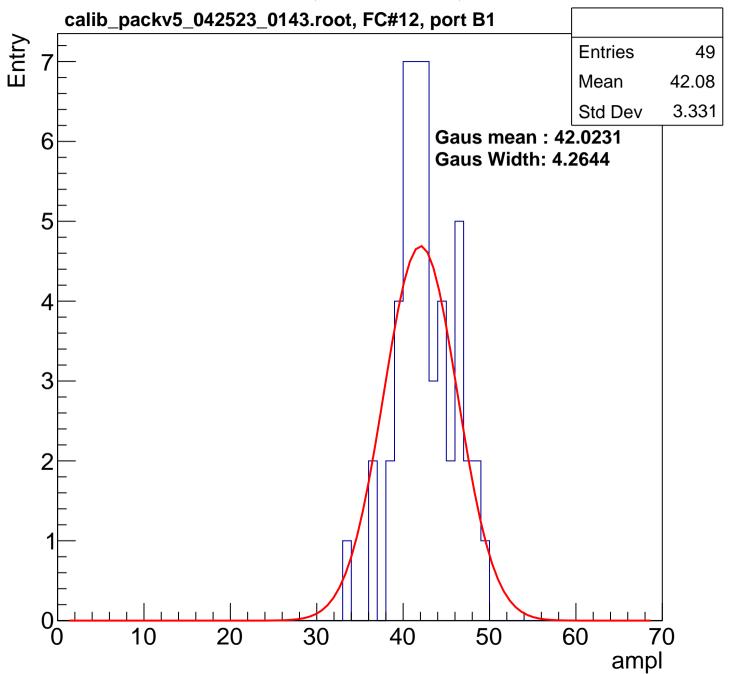


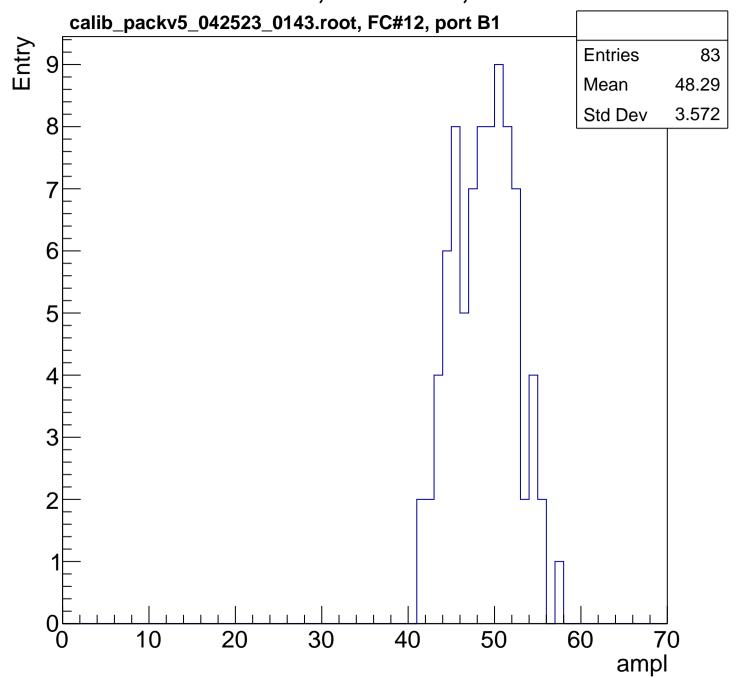


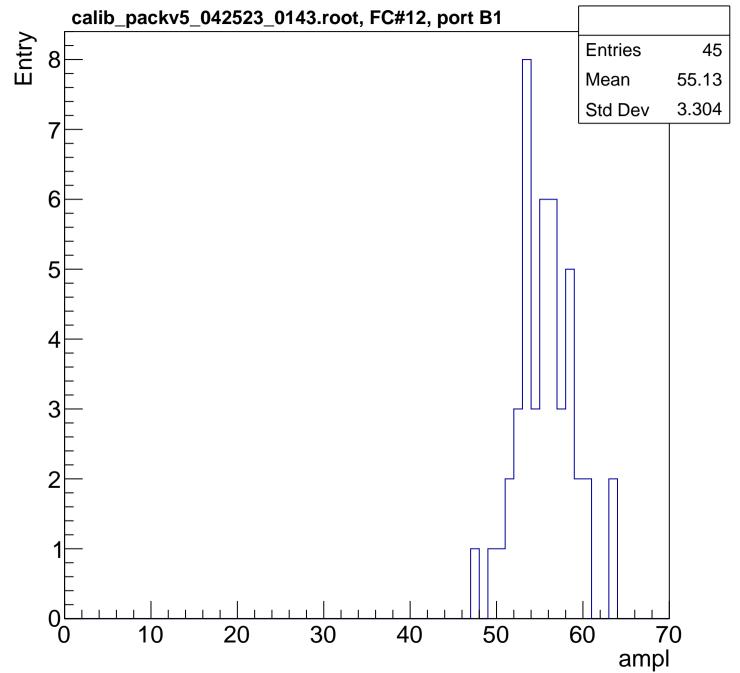


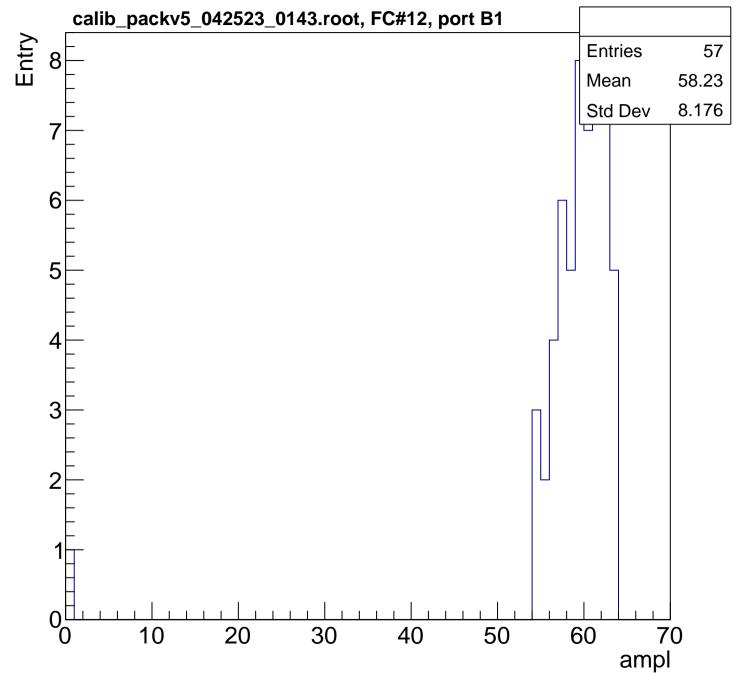


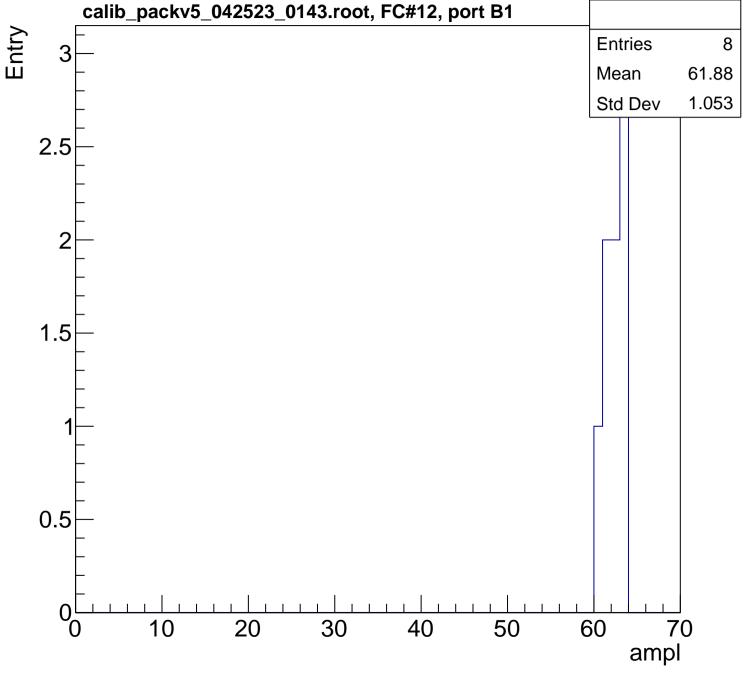


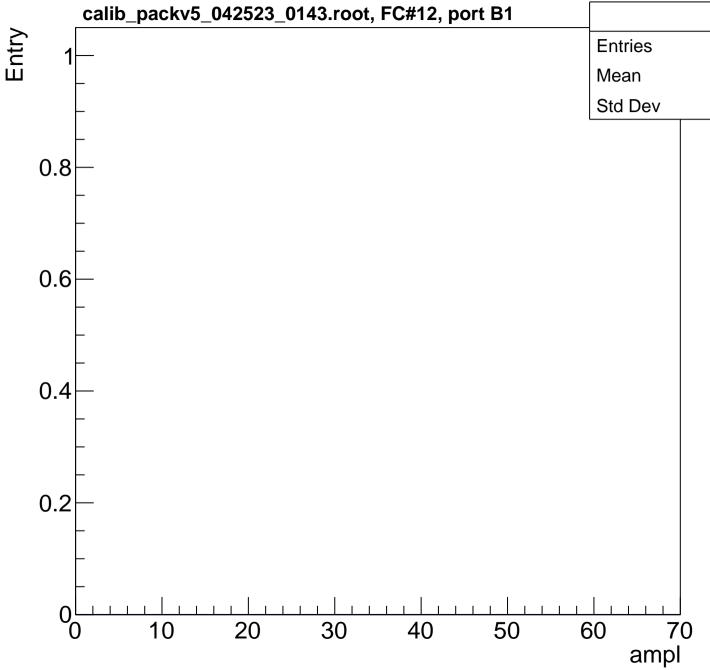


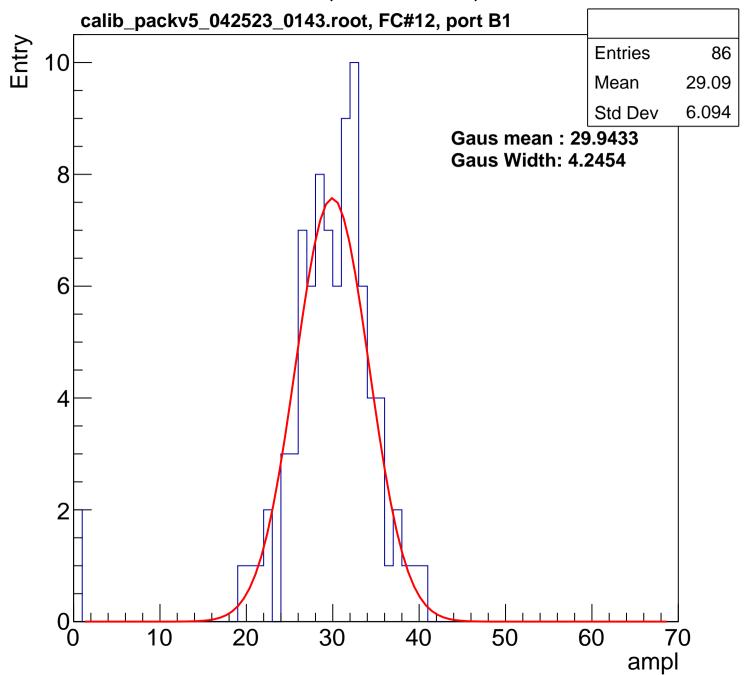


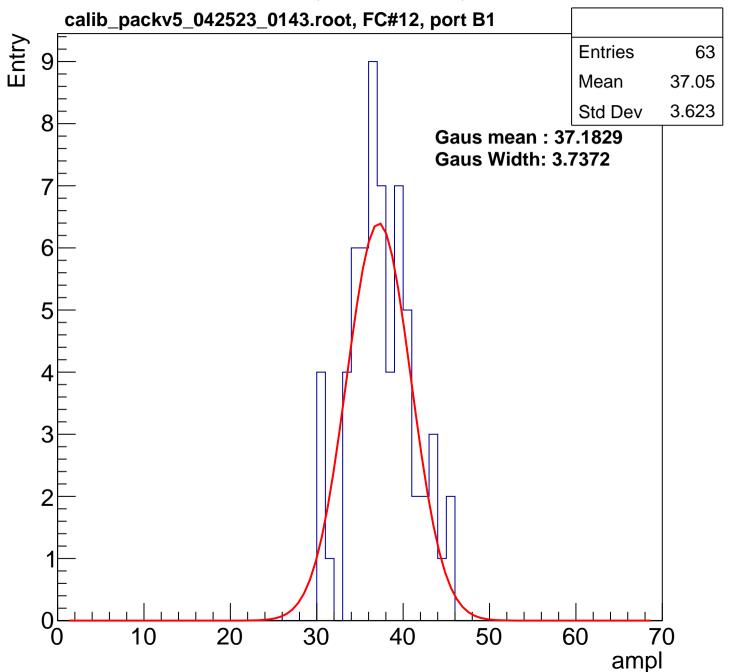


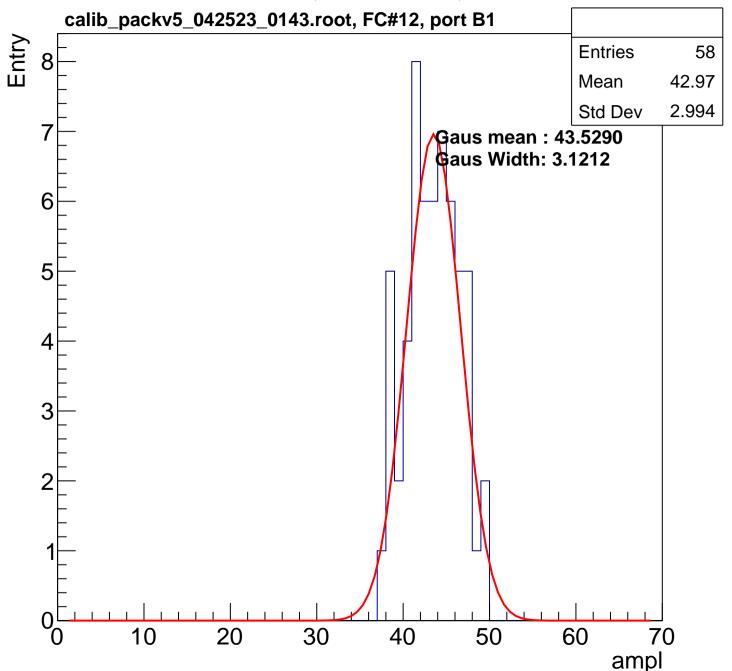


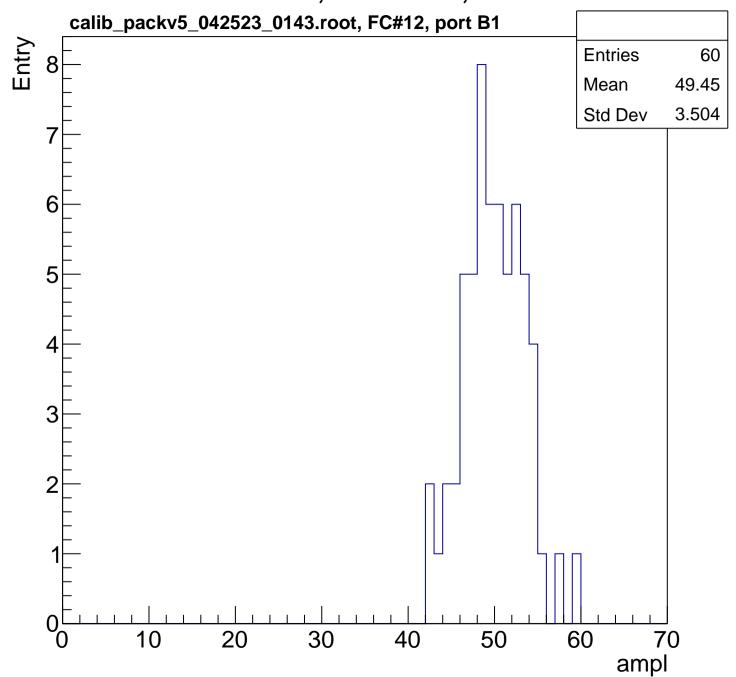


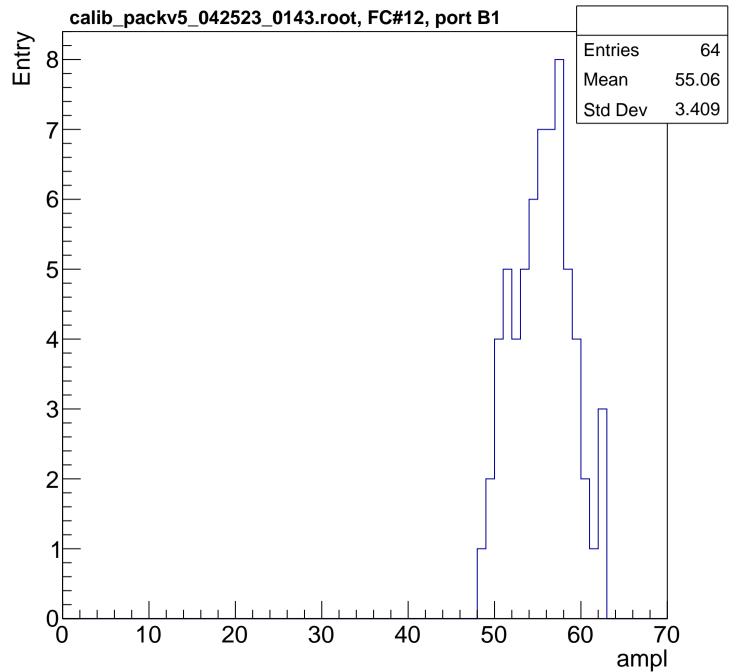


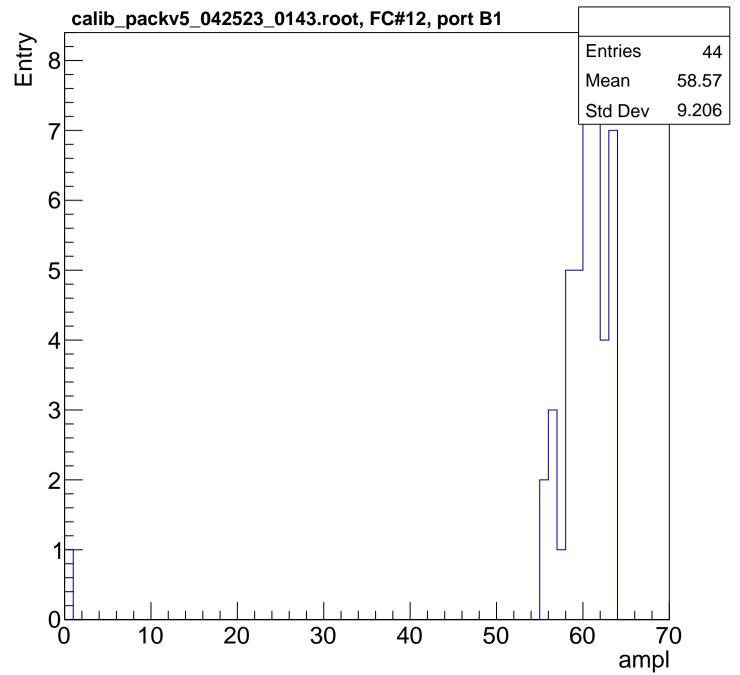


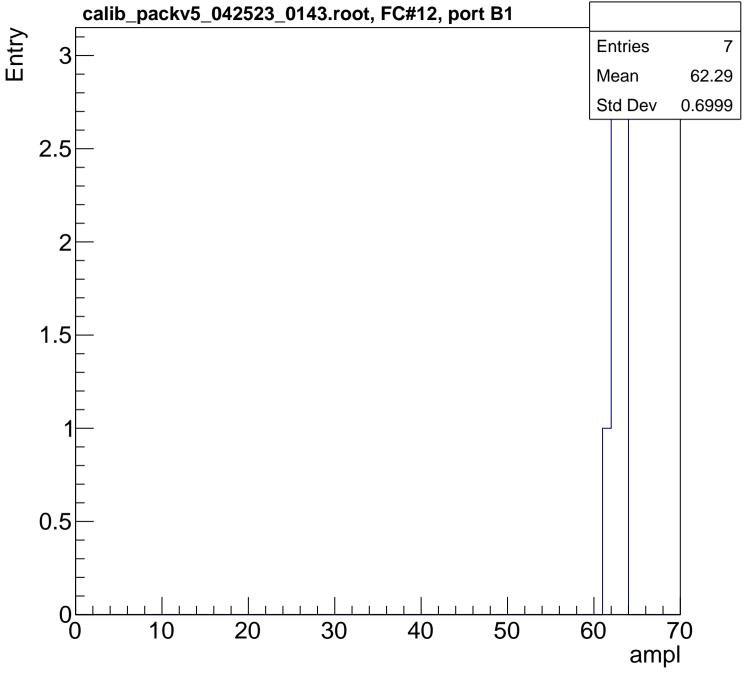


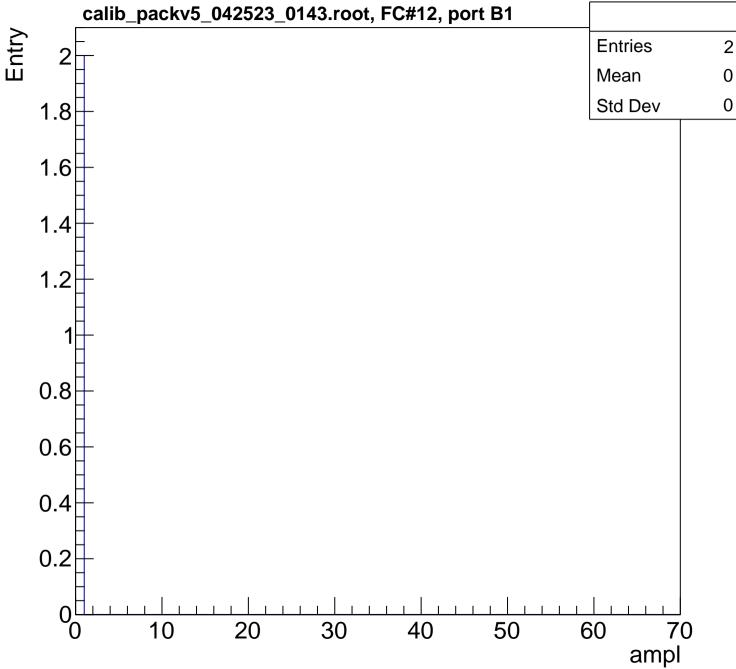


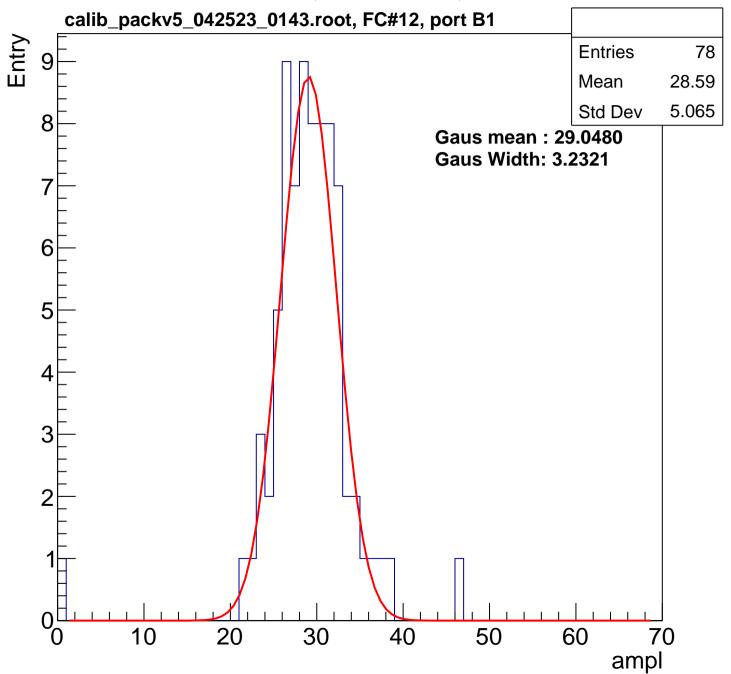


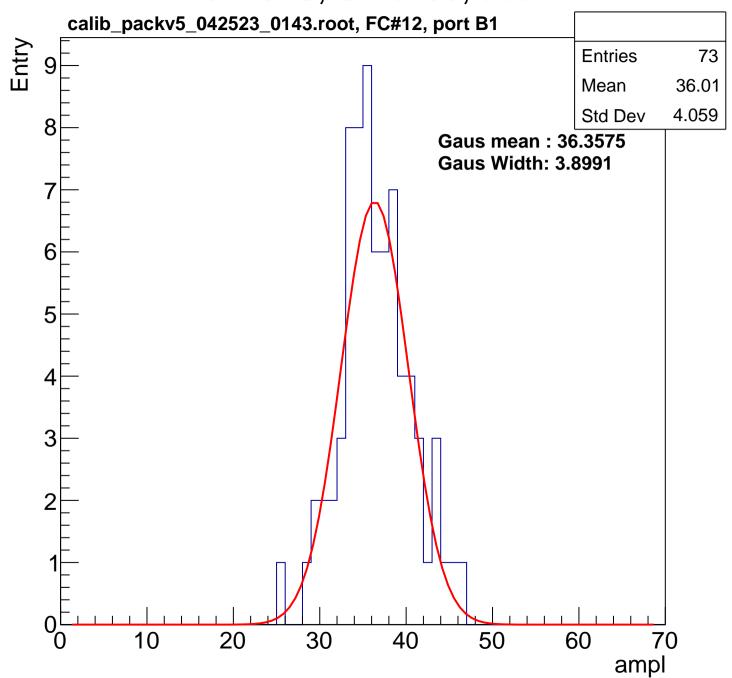


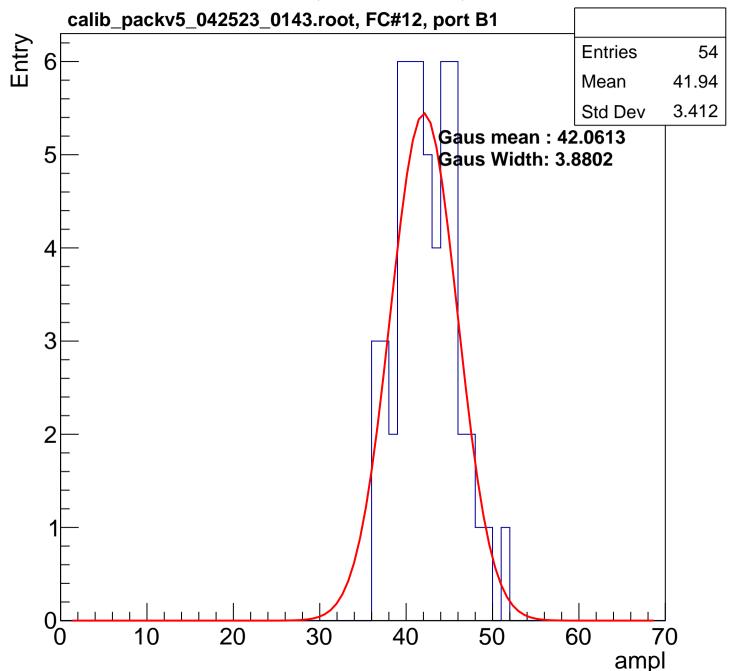


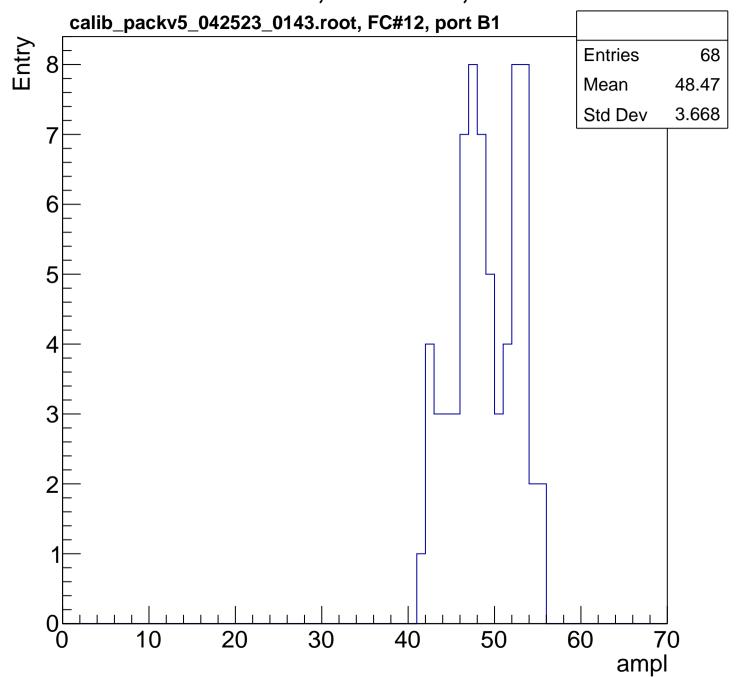


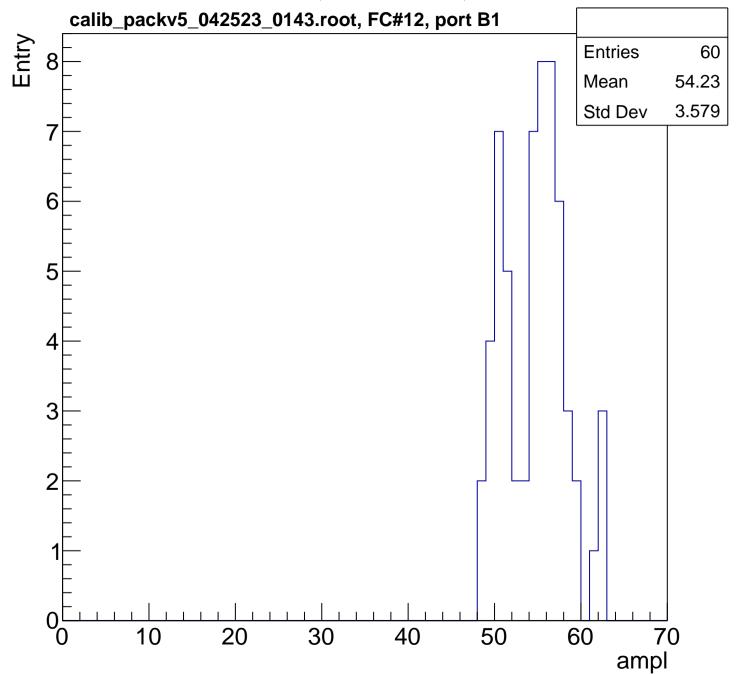


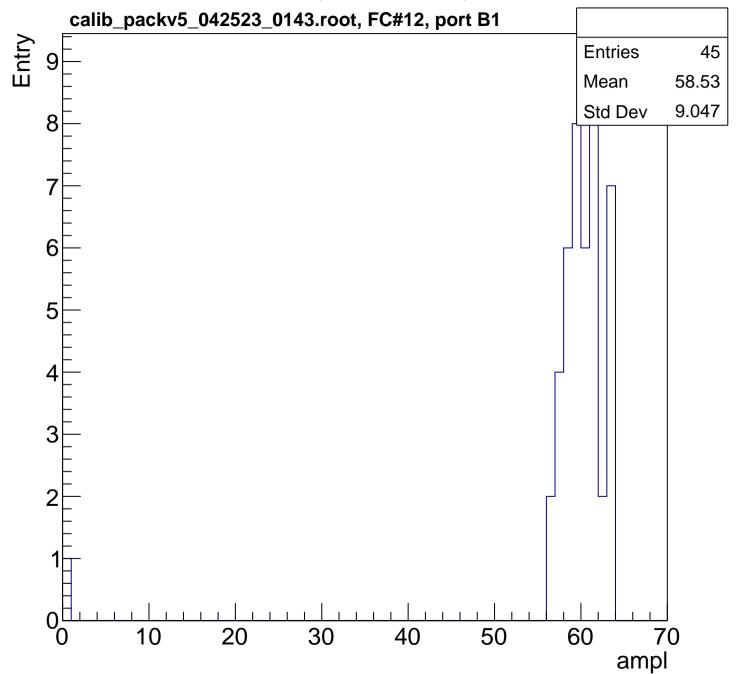


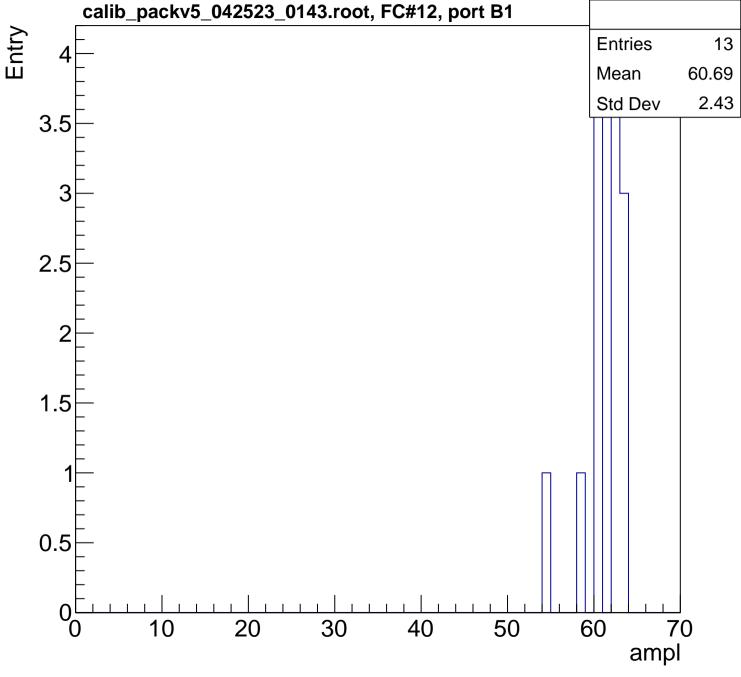




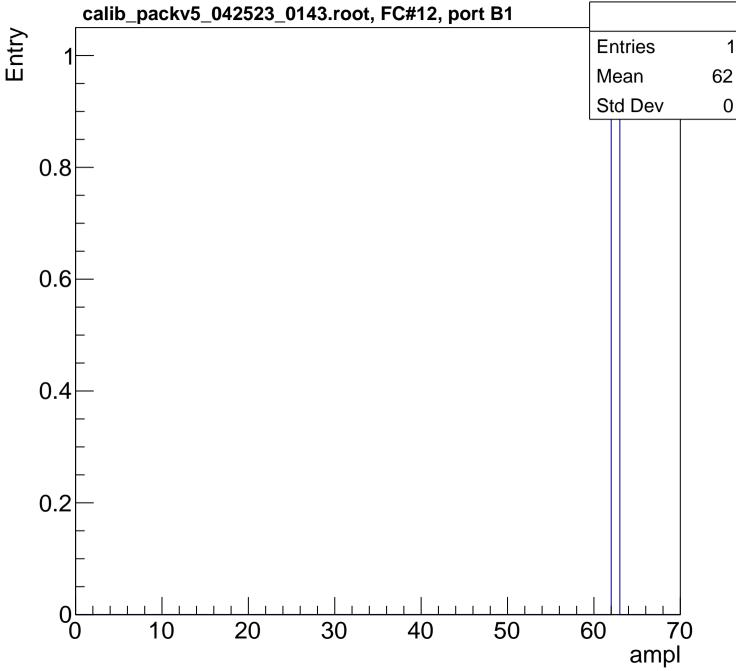


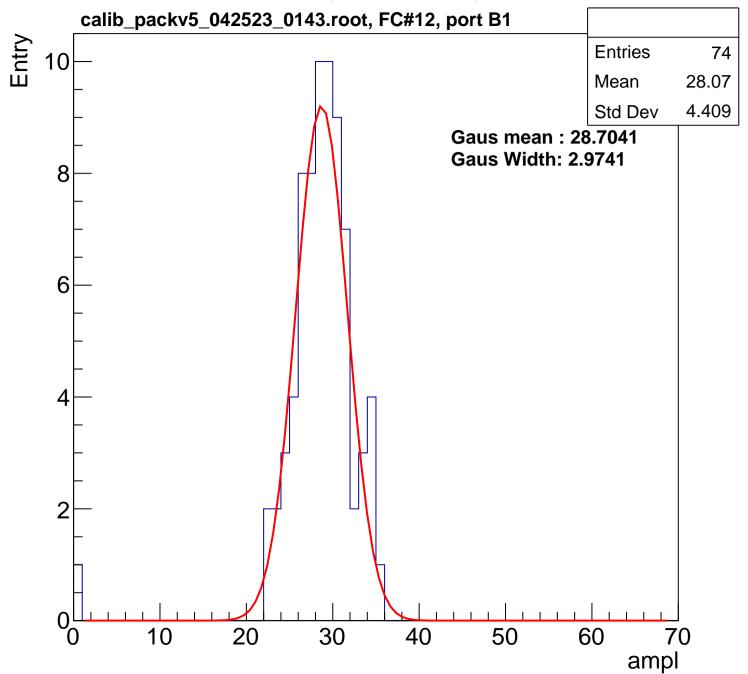


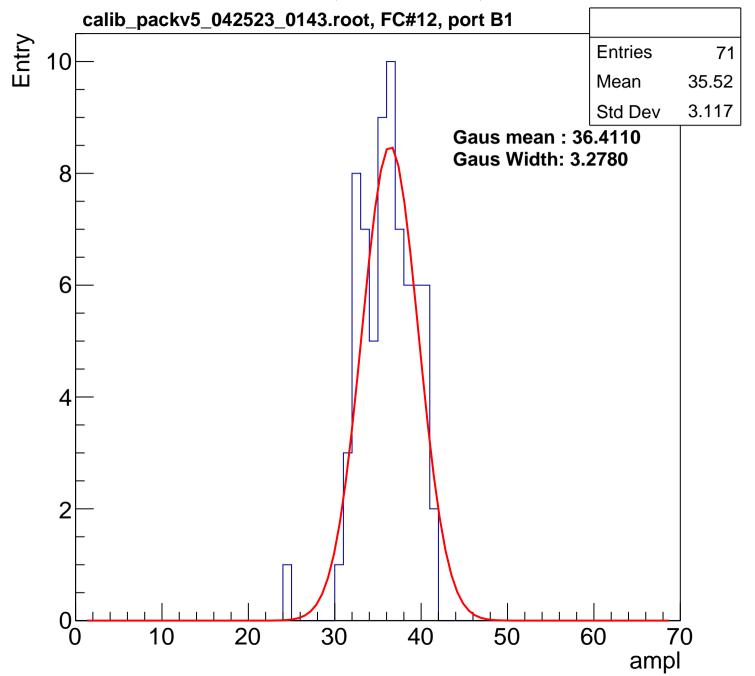


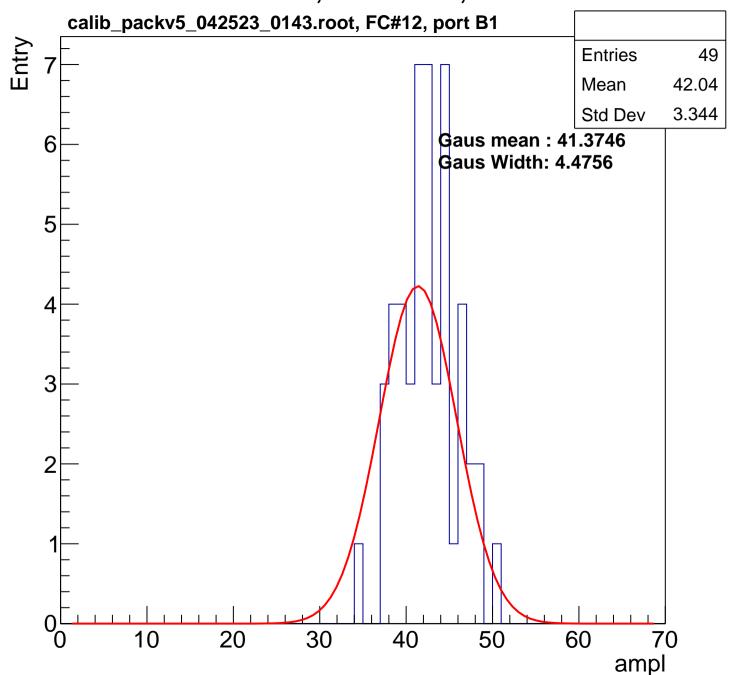


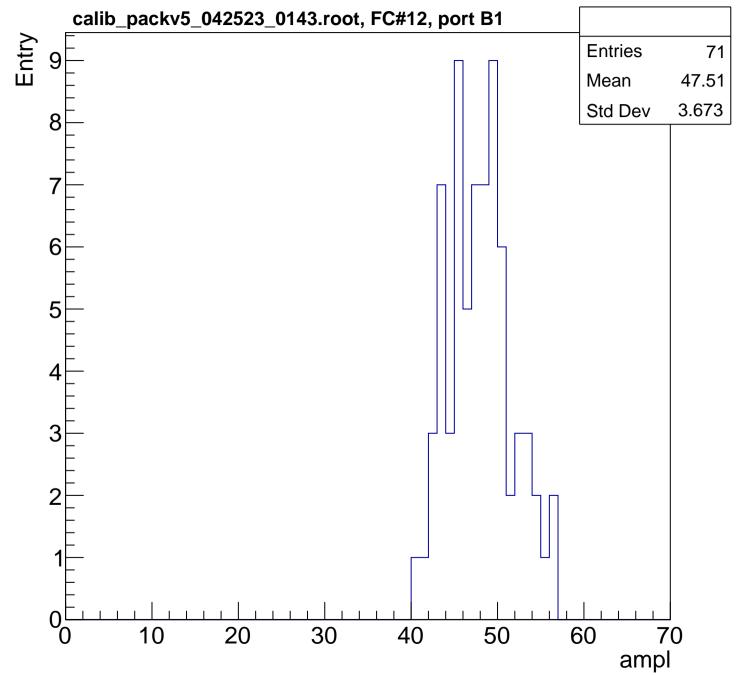
0

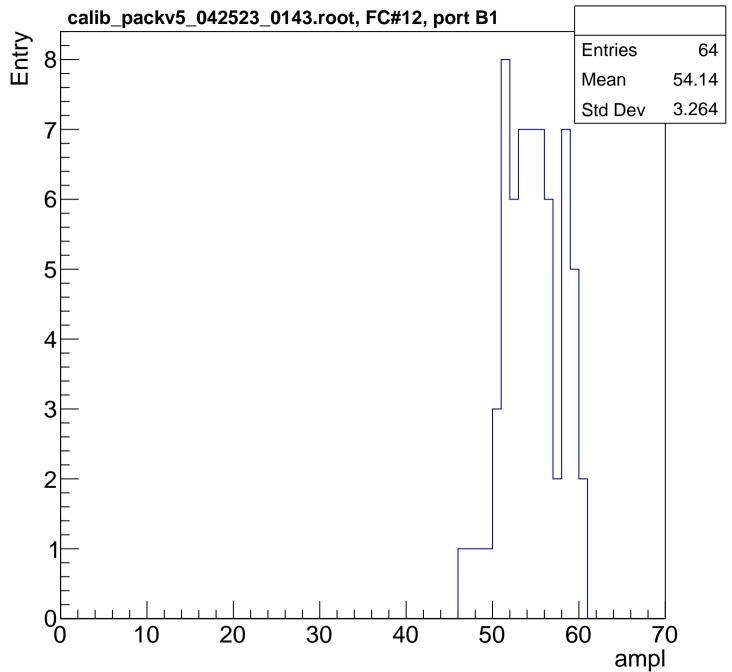


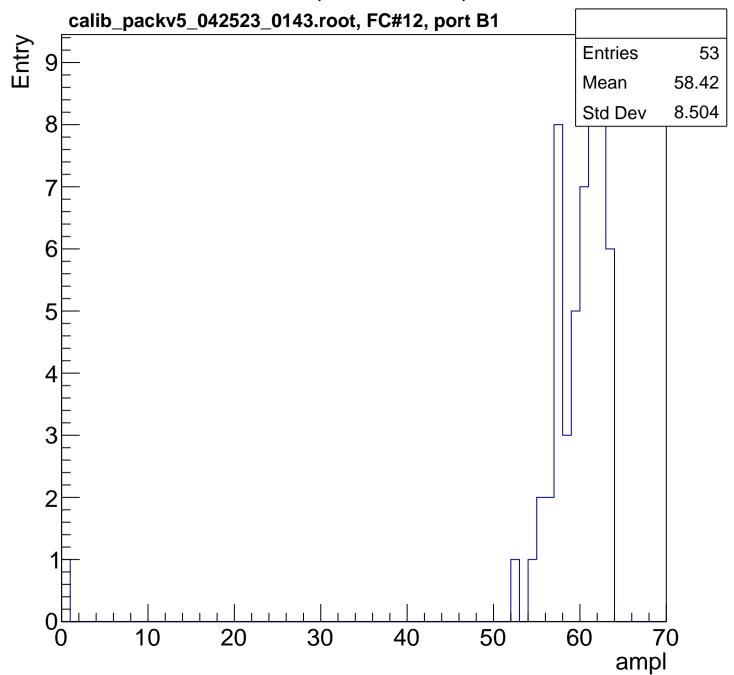


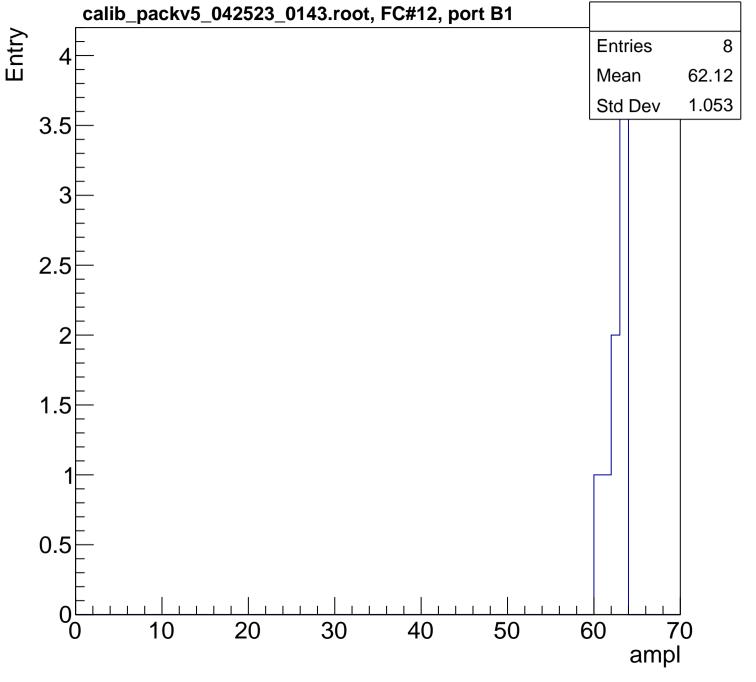


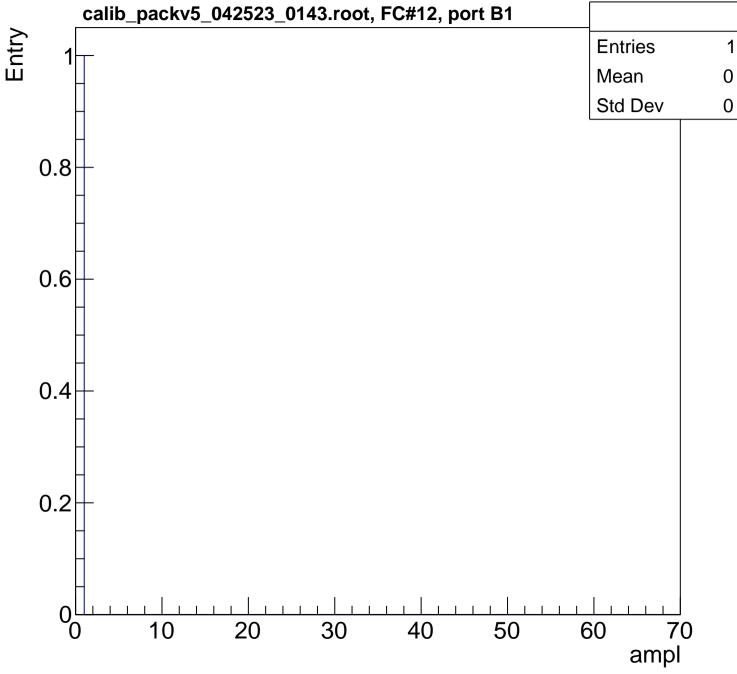


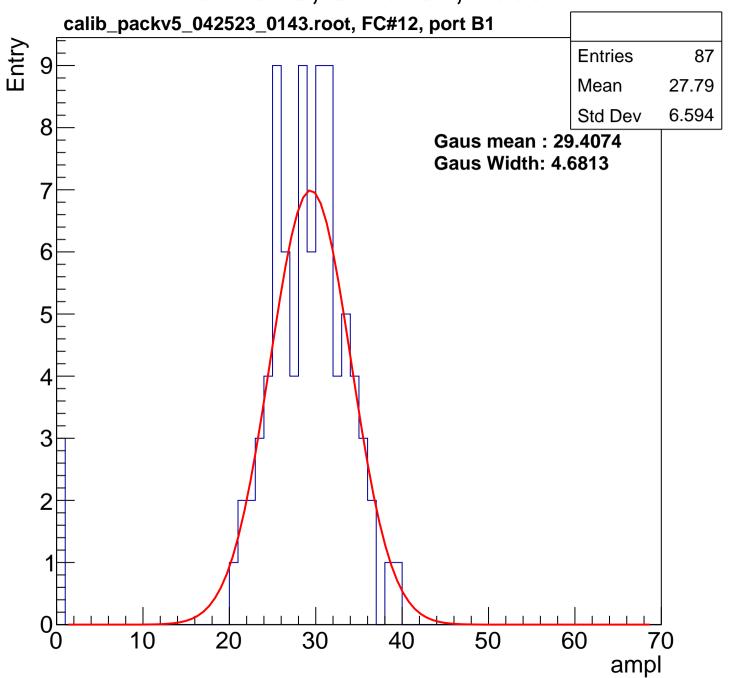


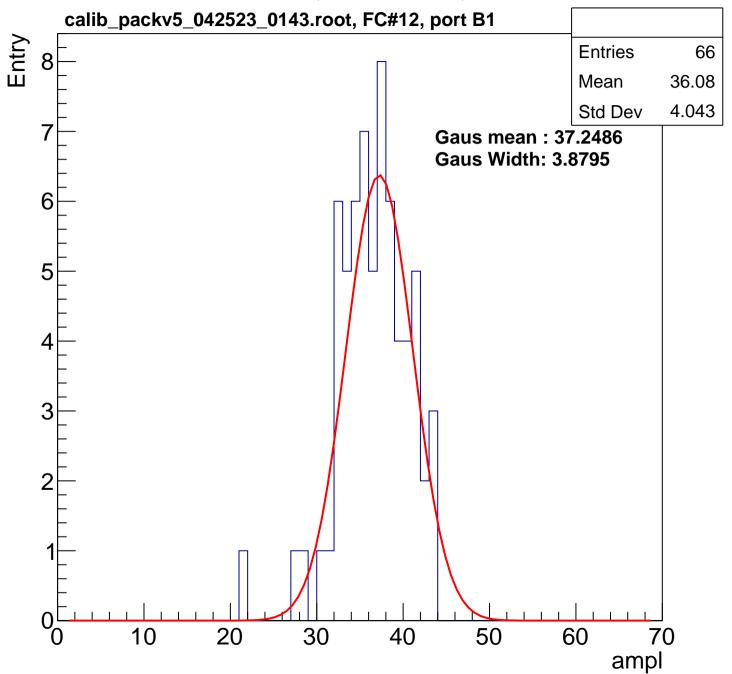


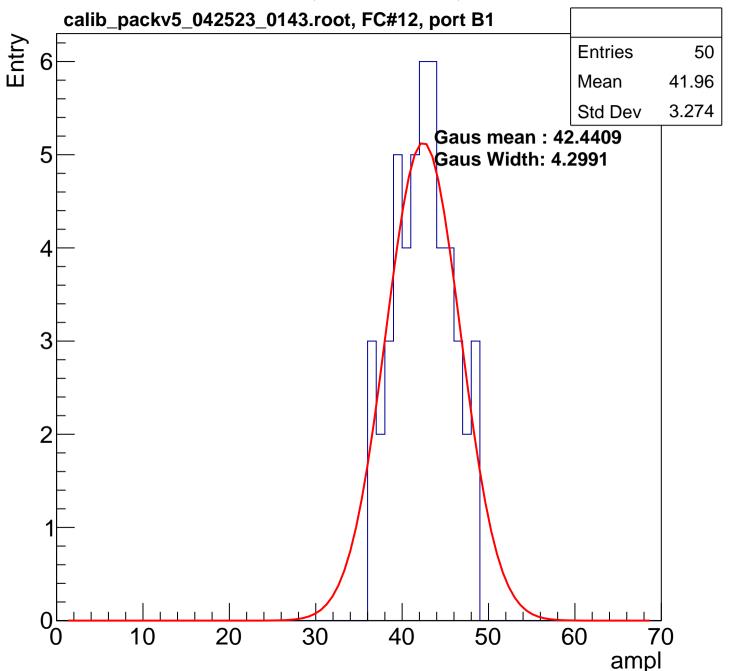


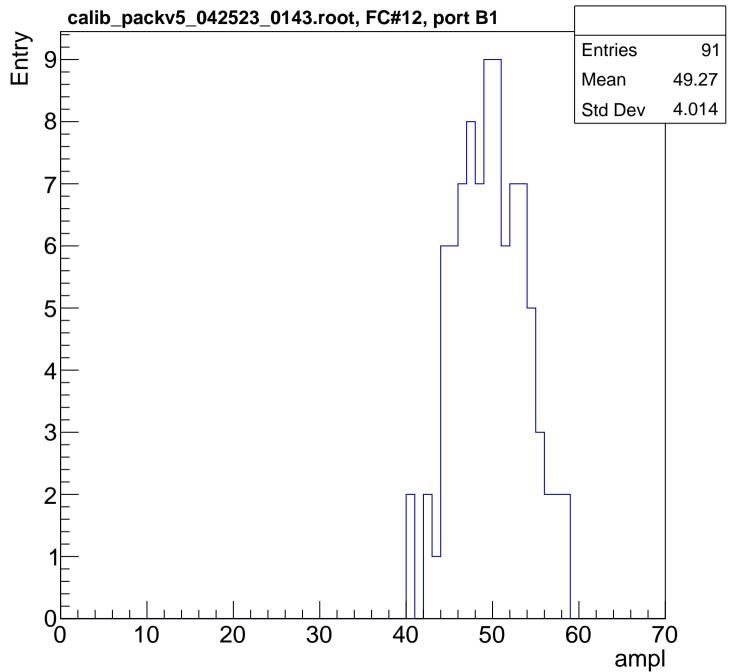


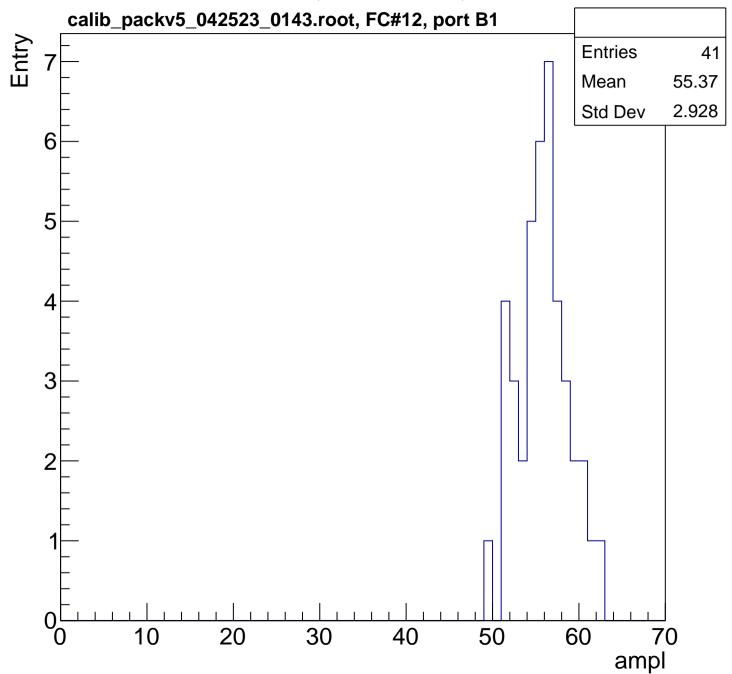


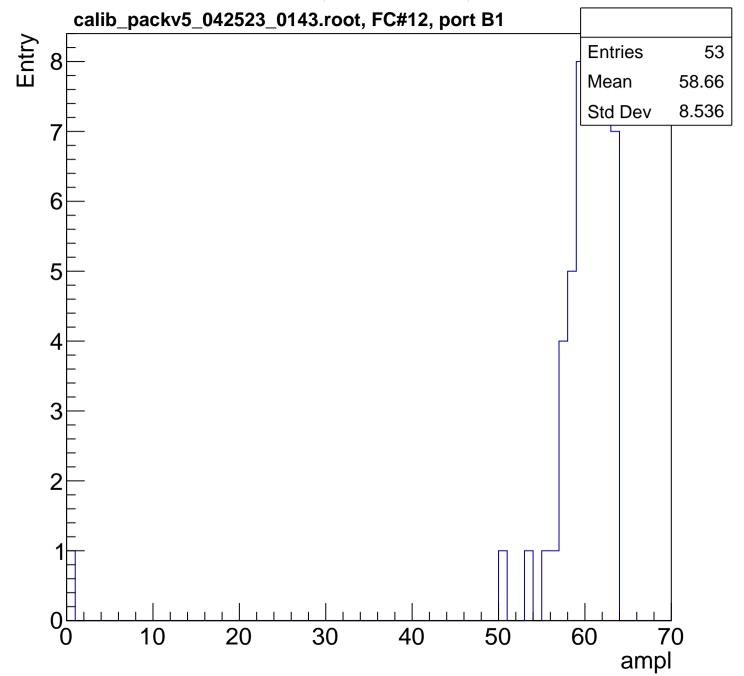


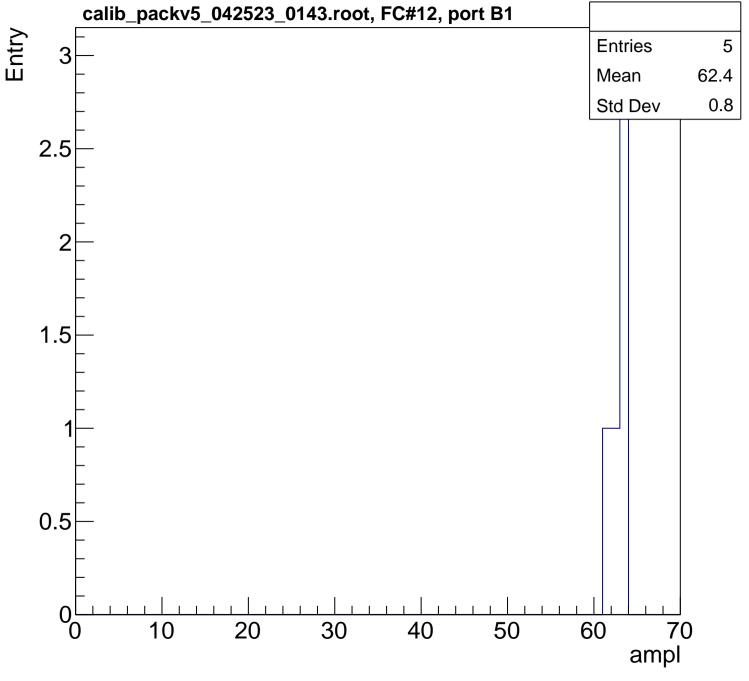




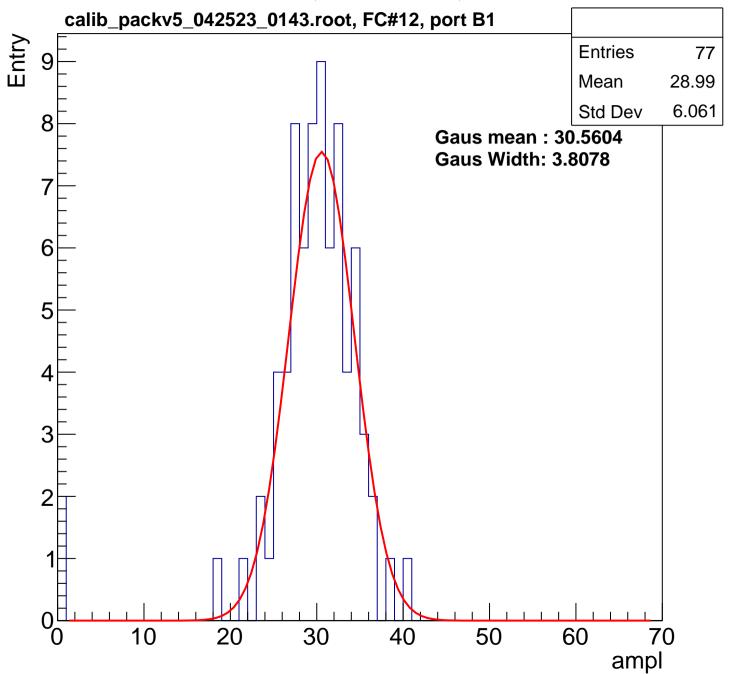


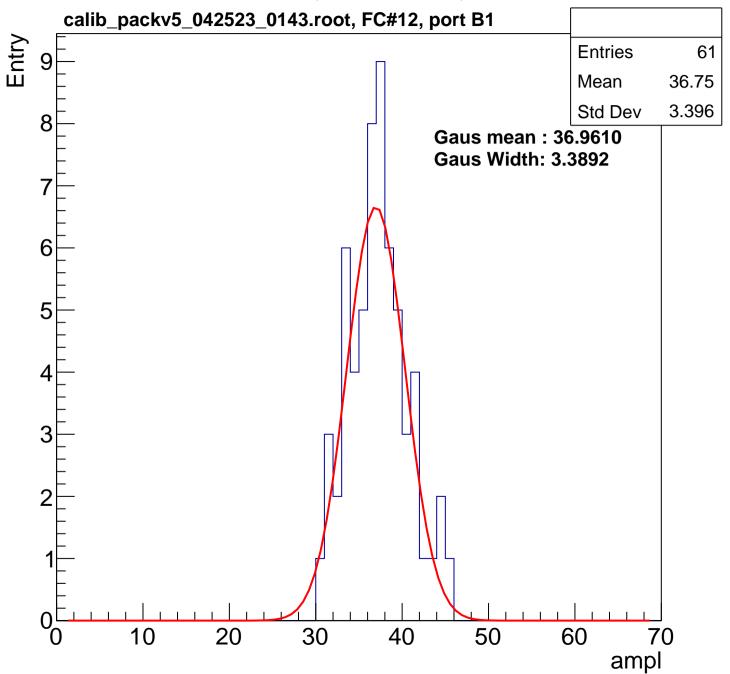


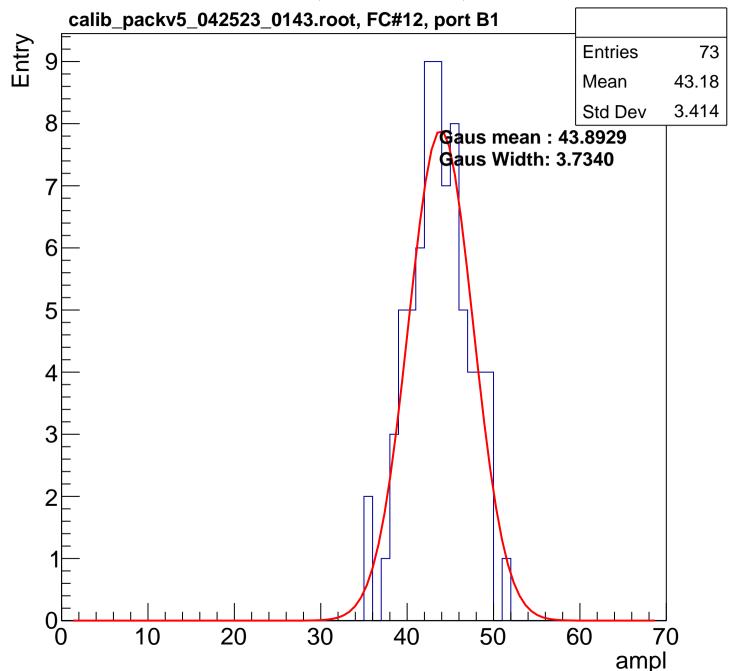


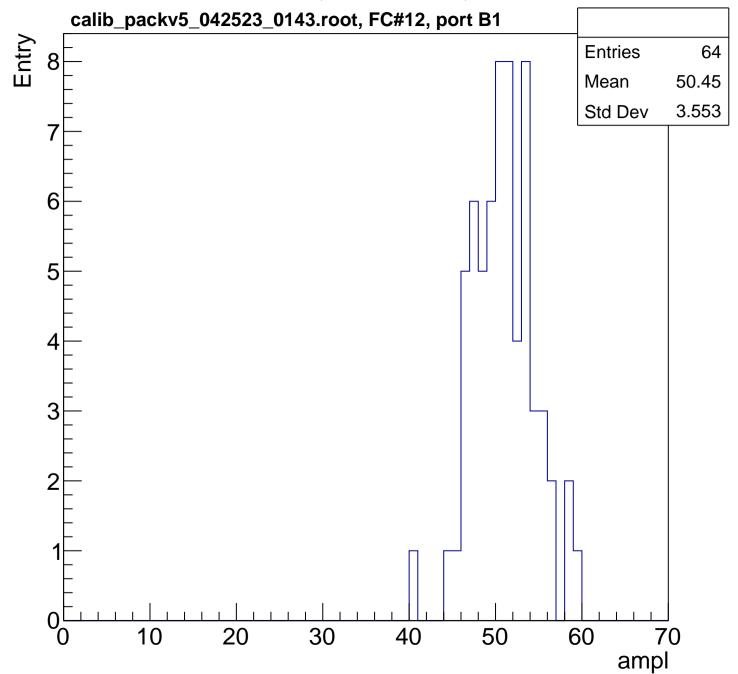


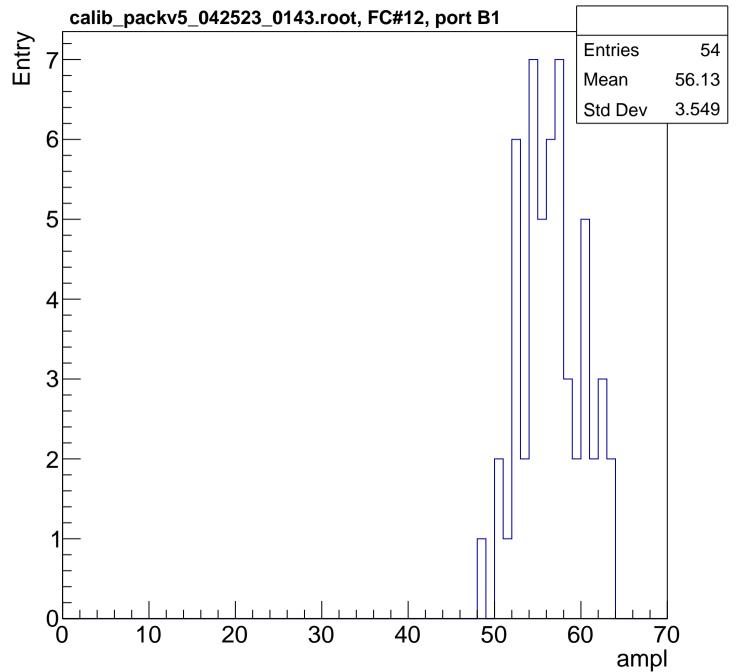


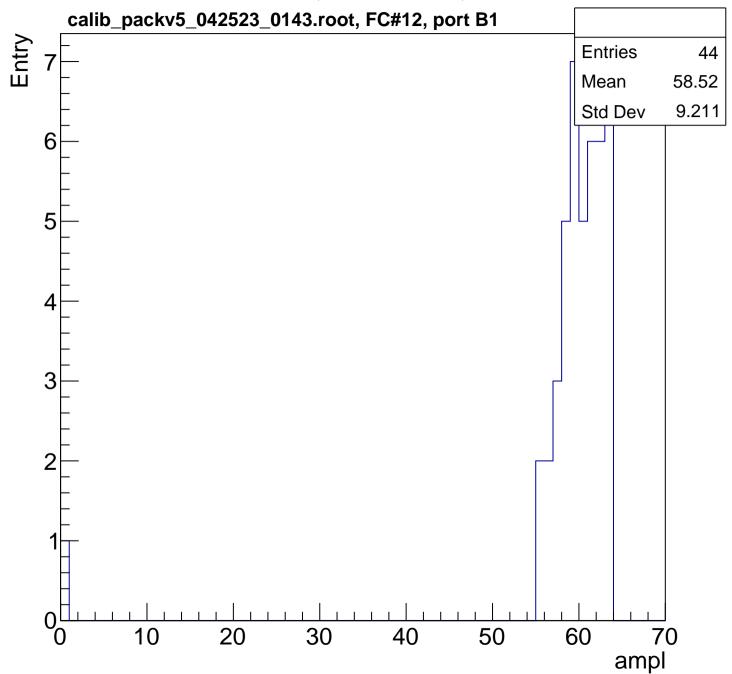


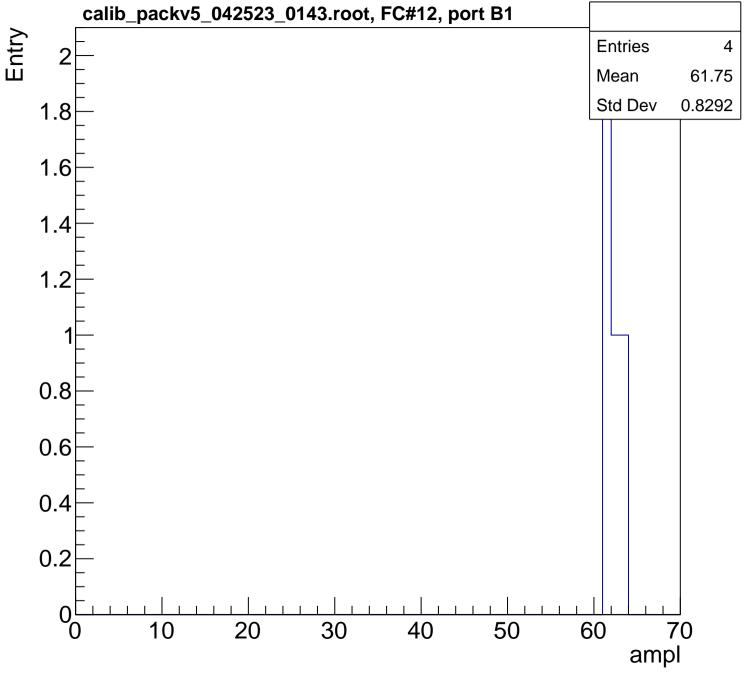




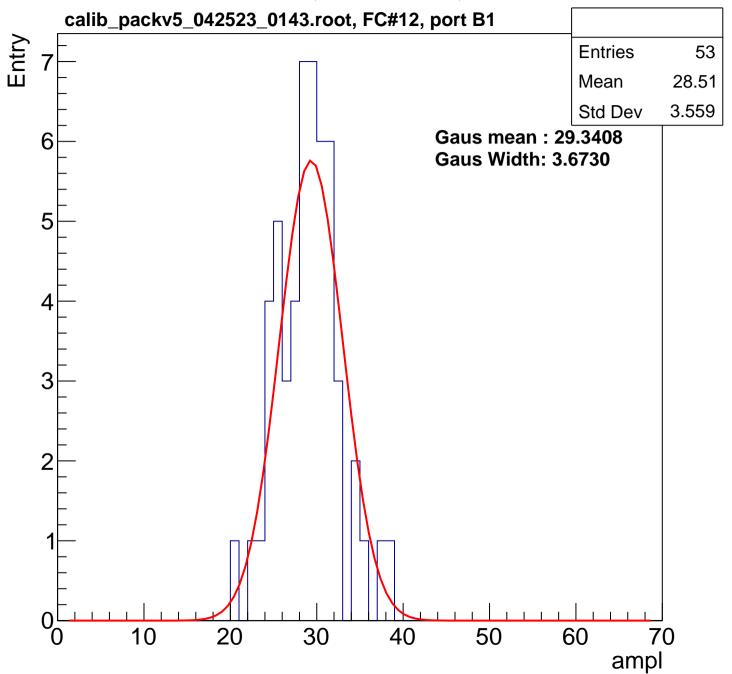


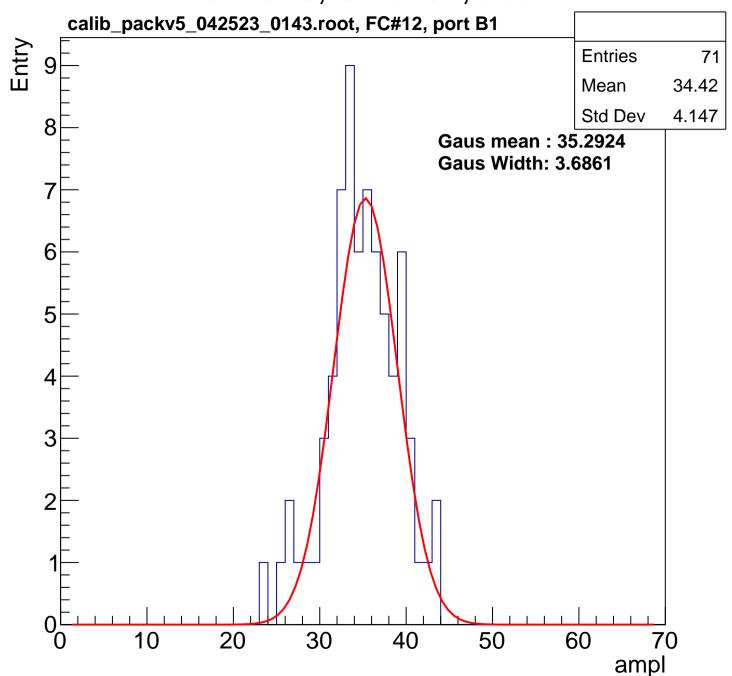


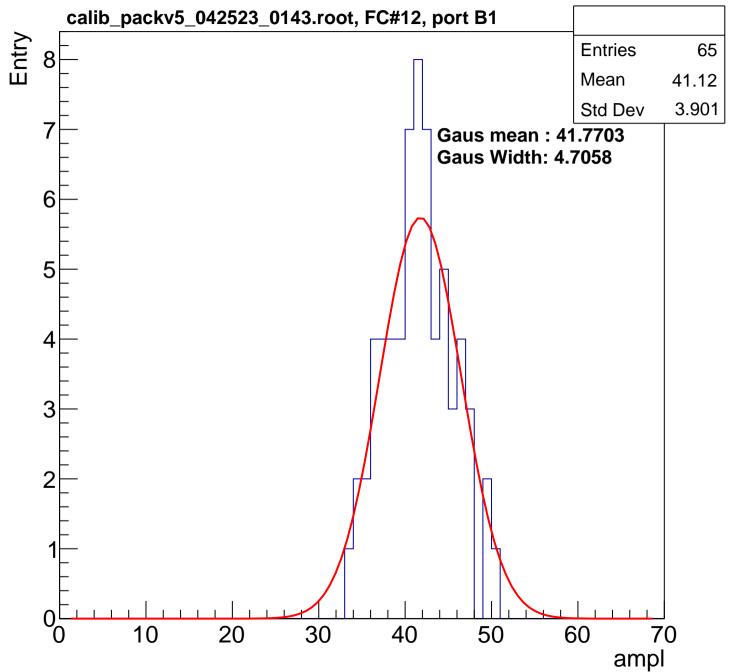


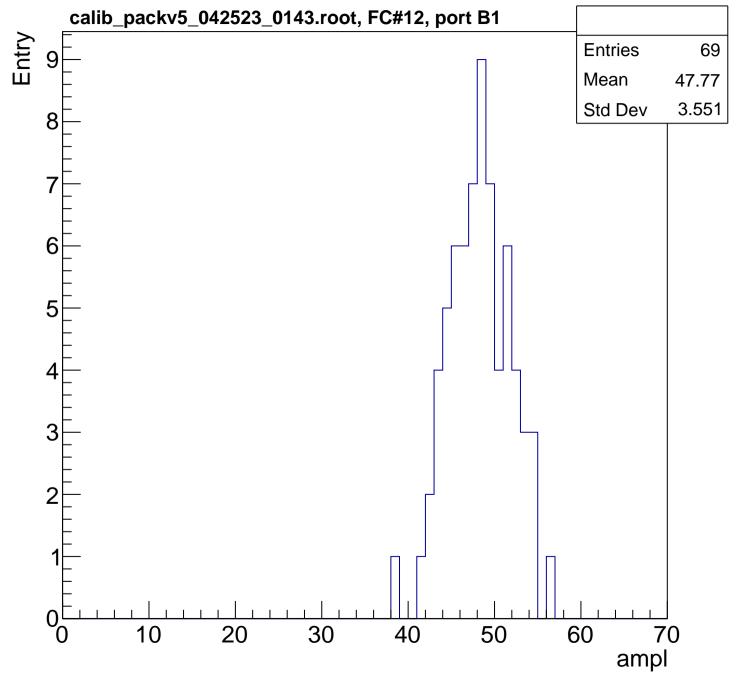


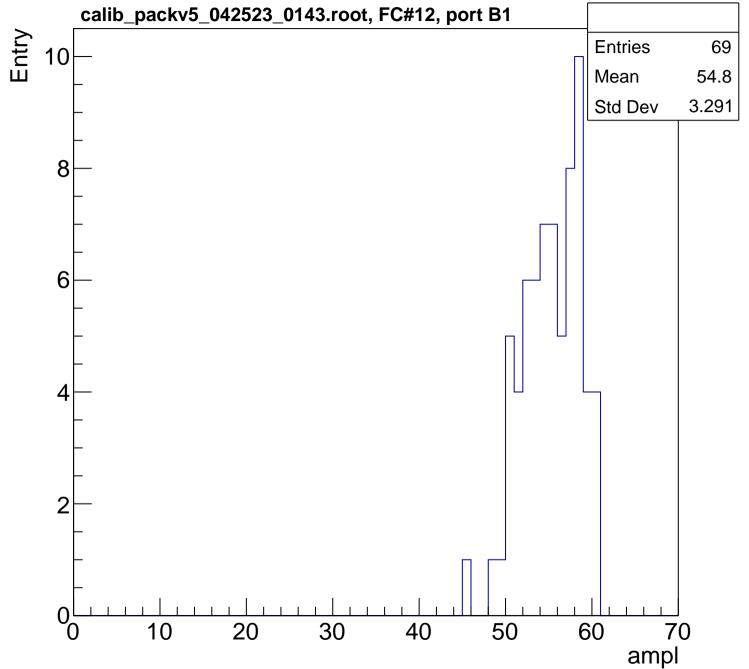
B0L102S, U4-ch53, adc7 calib_packv5_042523_0143.root, FC#12, port B1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

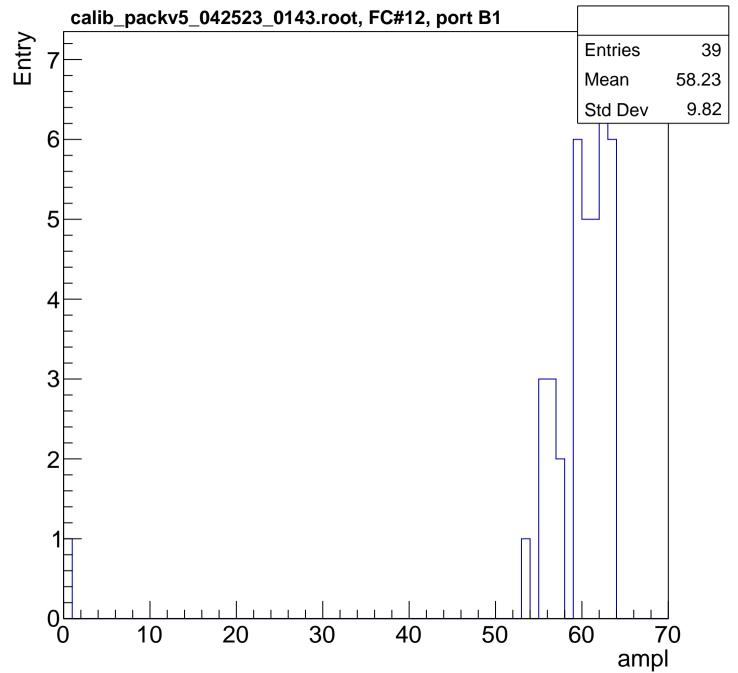


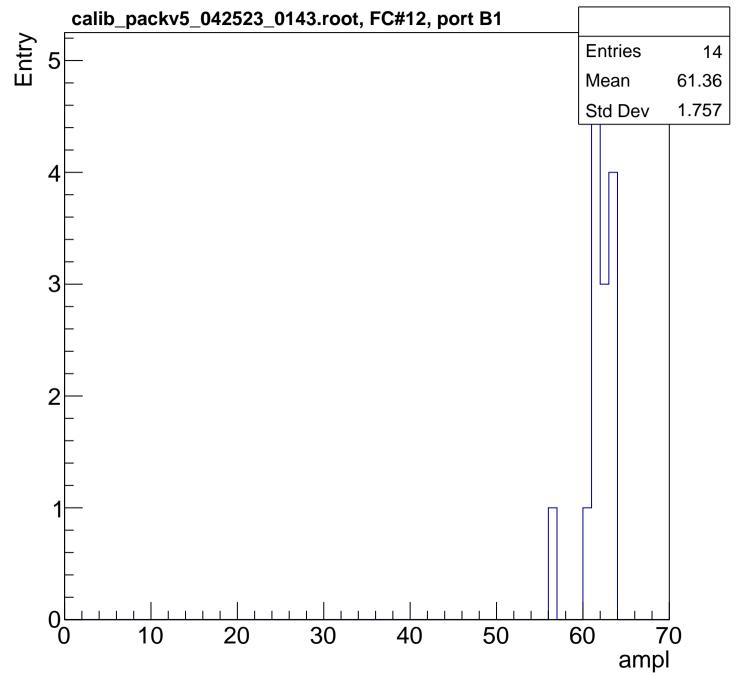




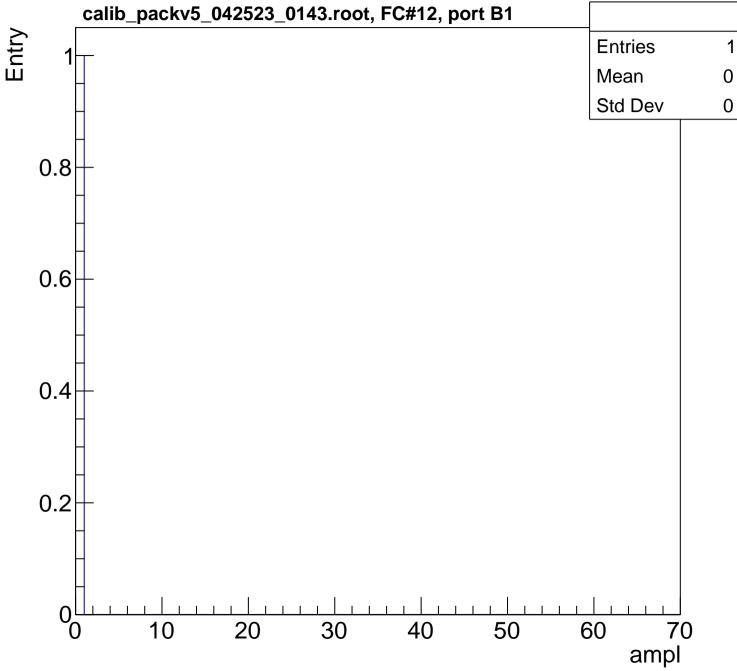


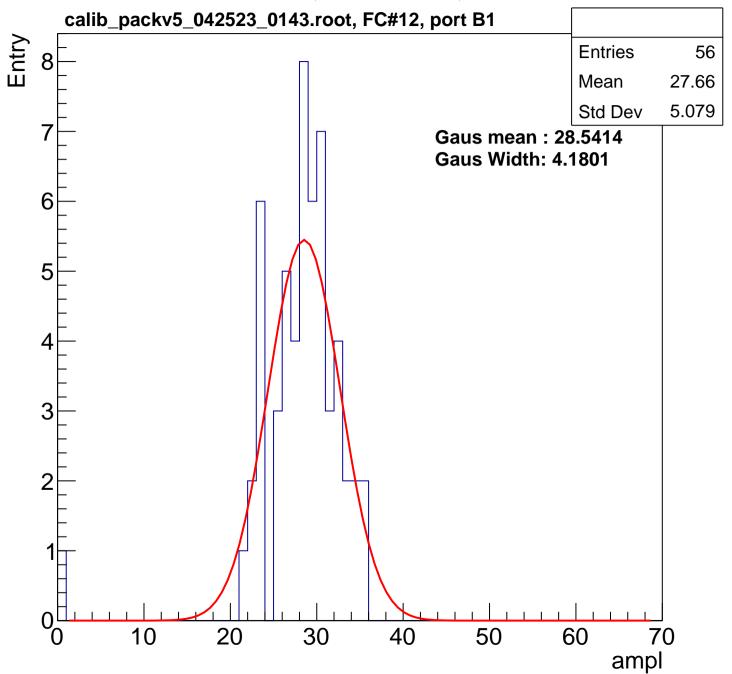


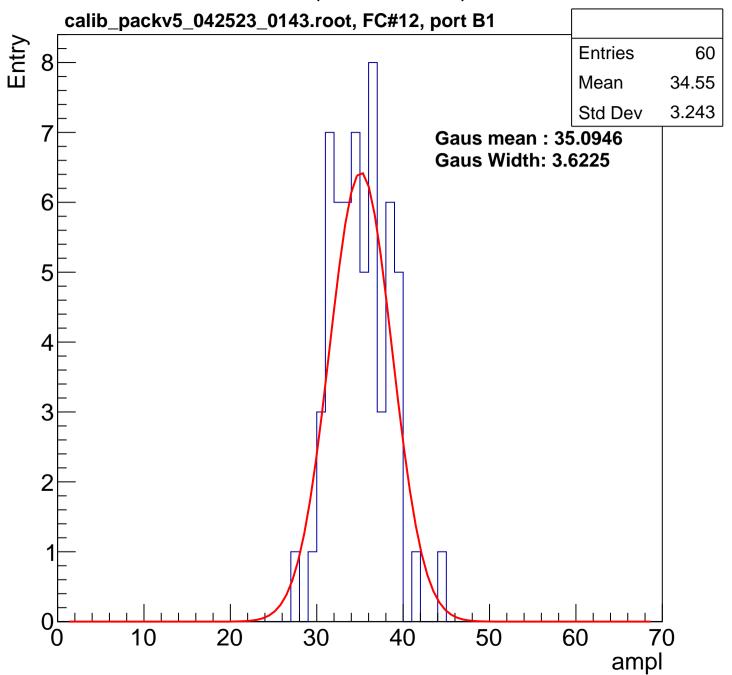


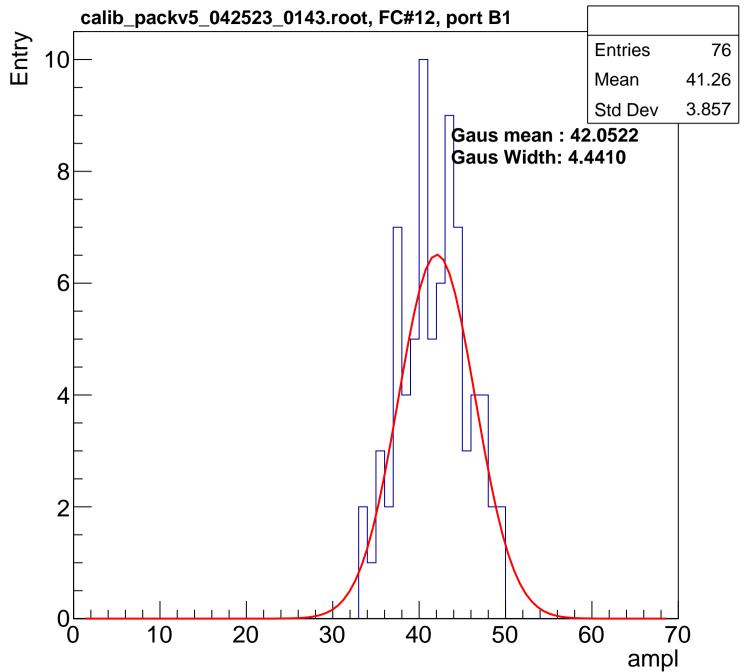


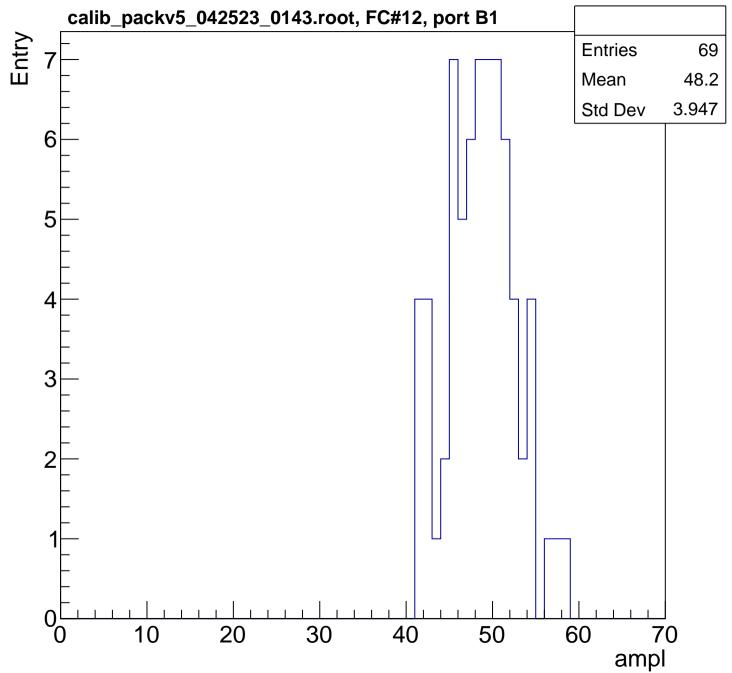
1

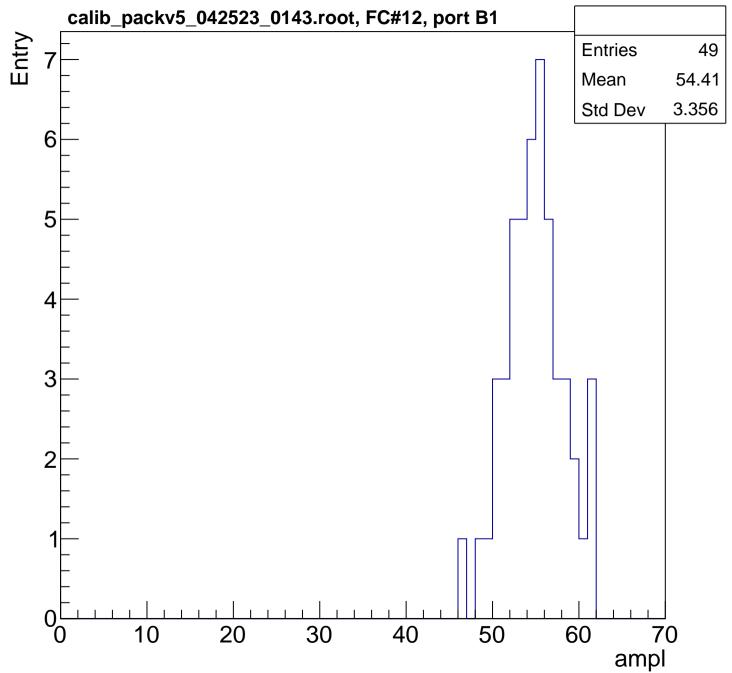


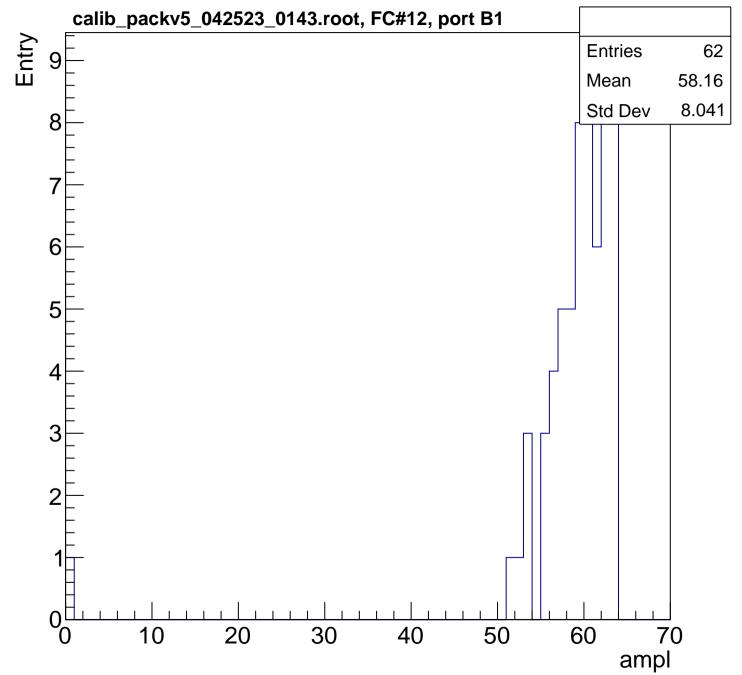


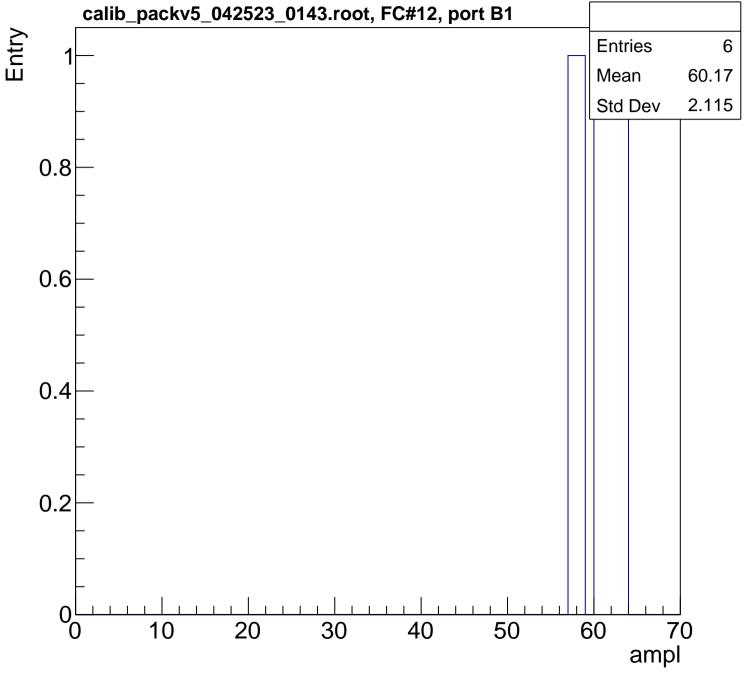


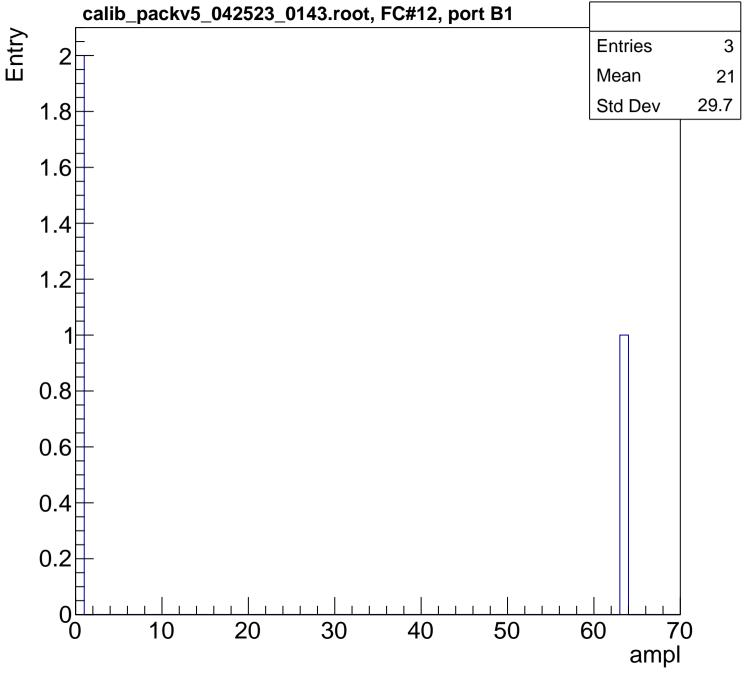


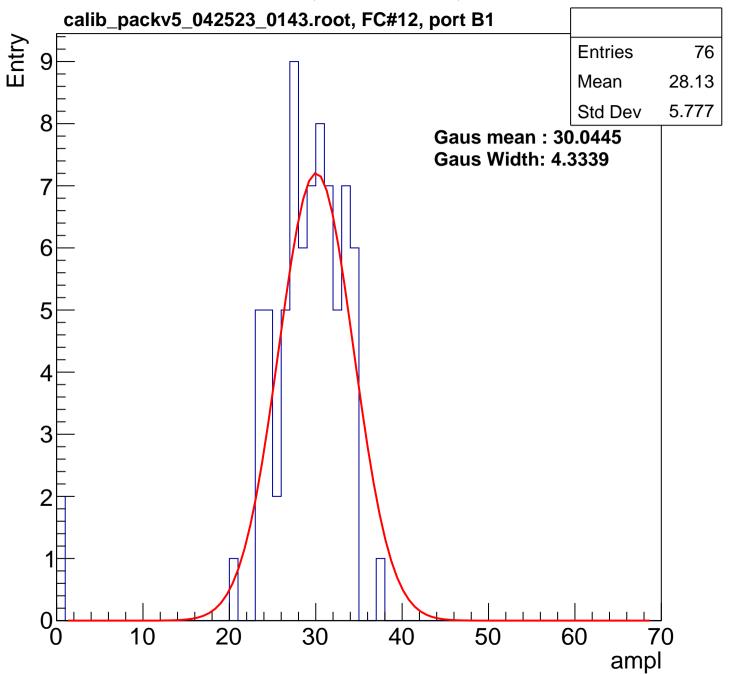


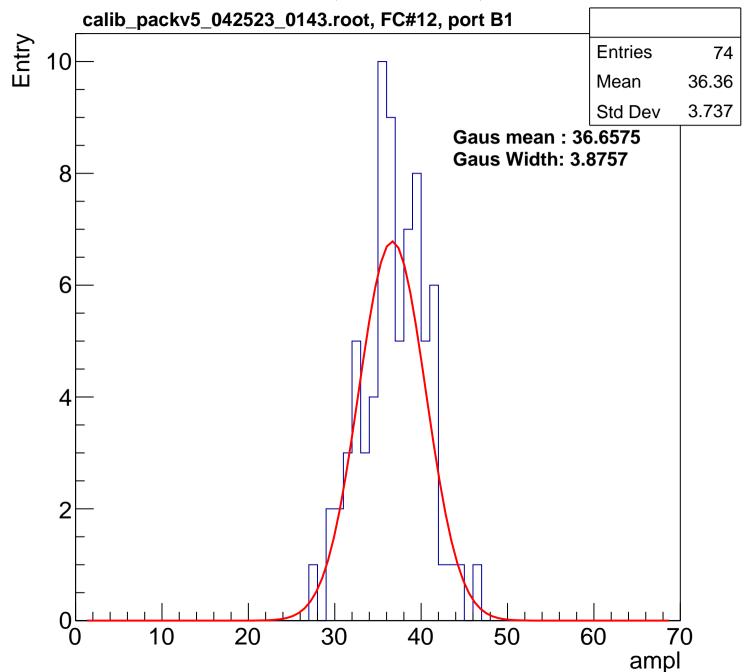


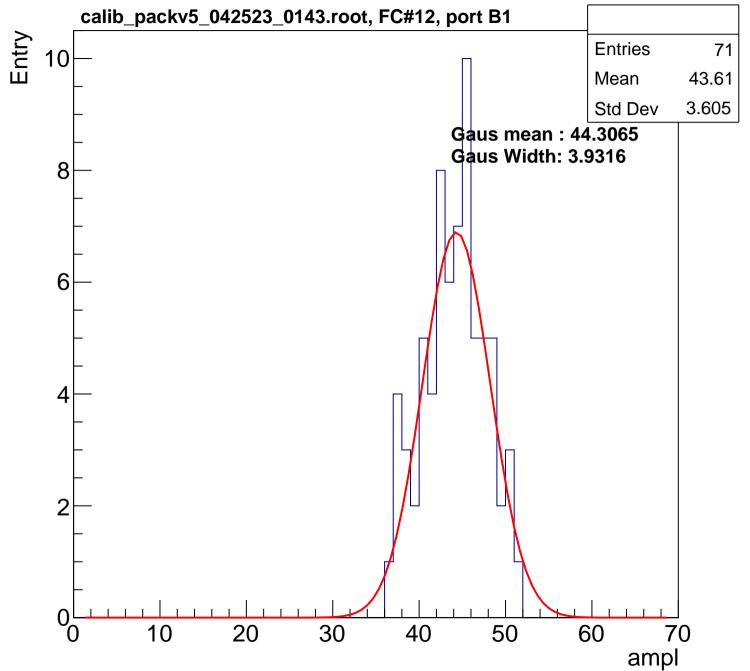


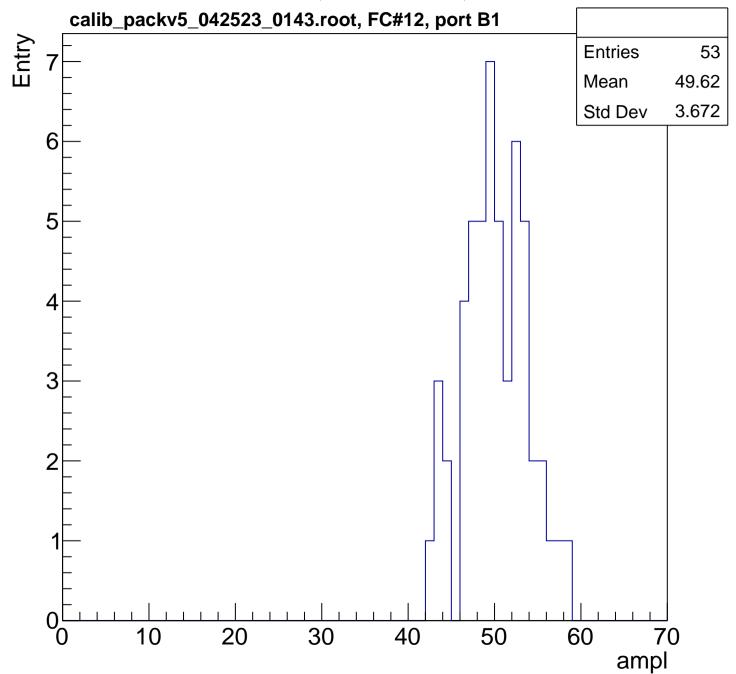


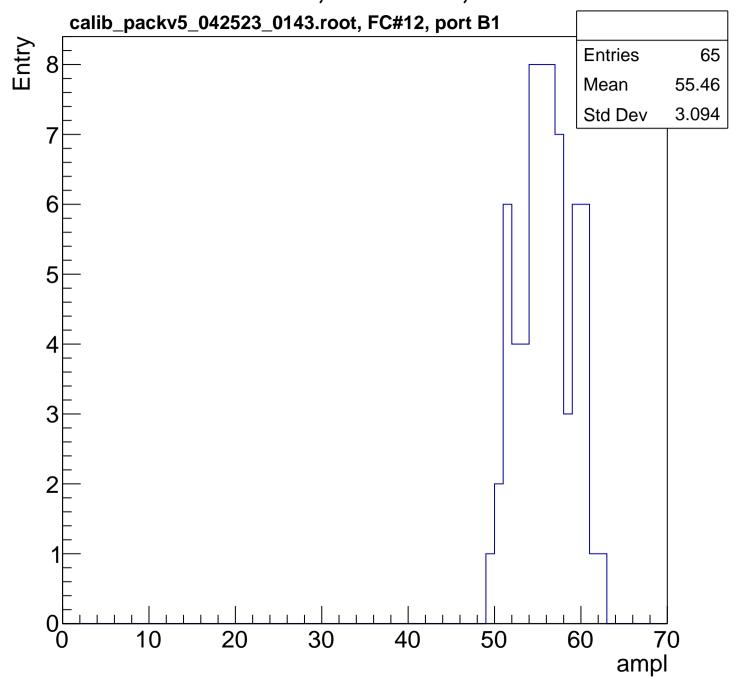


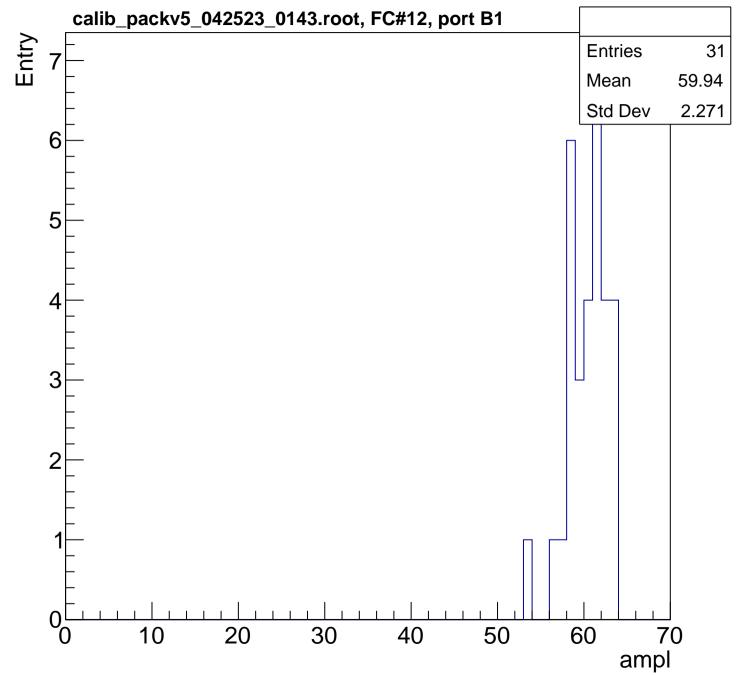


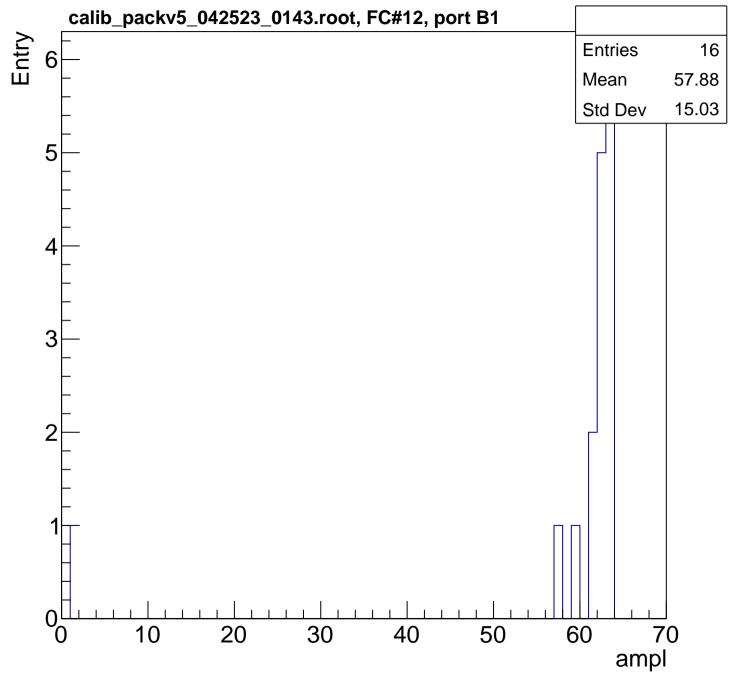


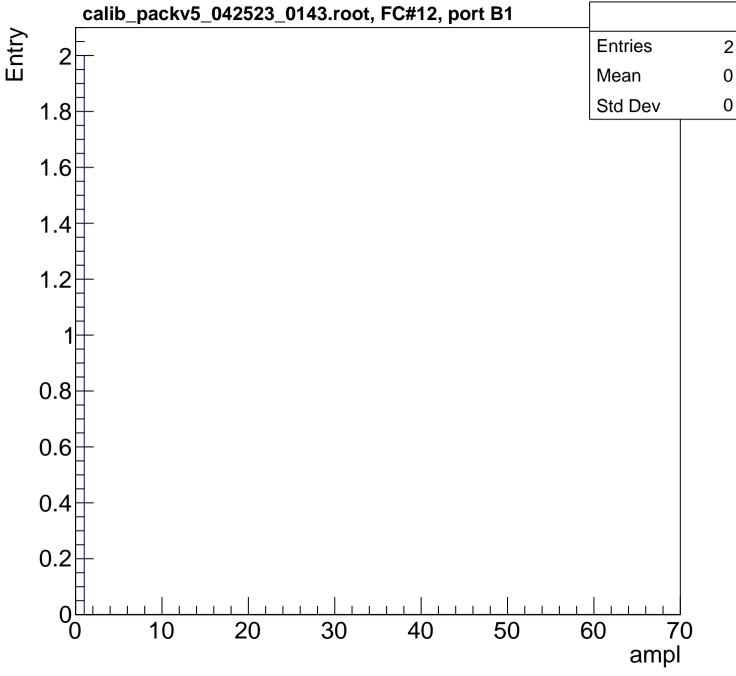


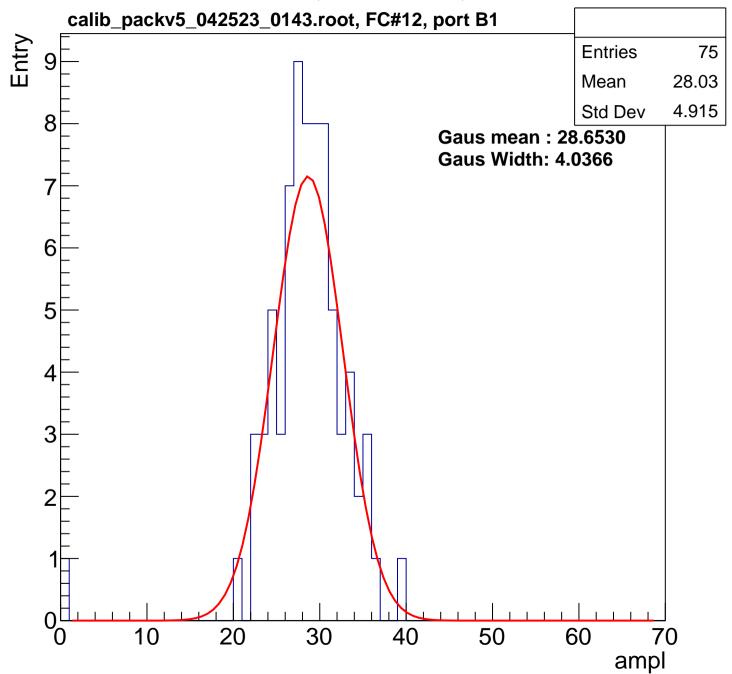


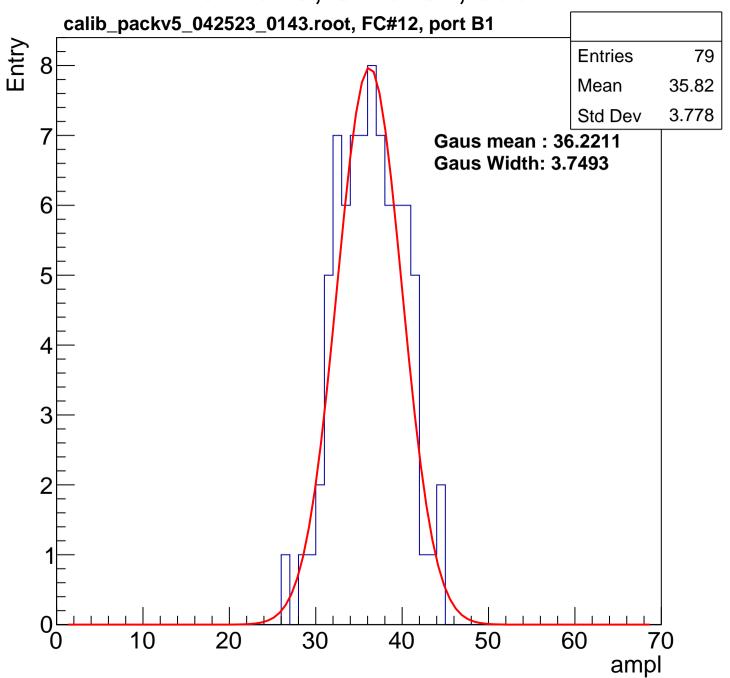


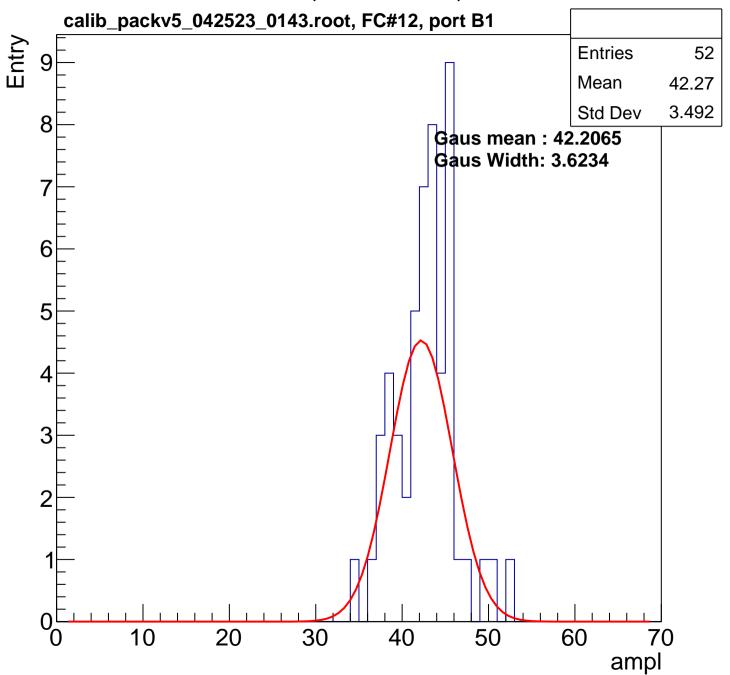


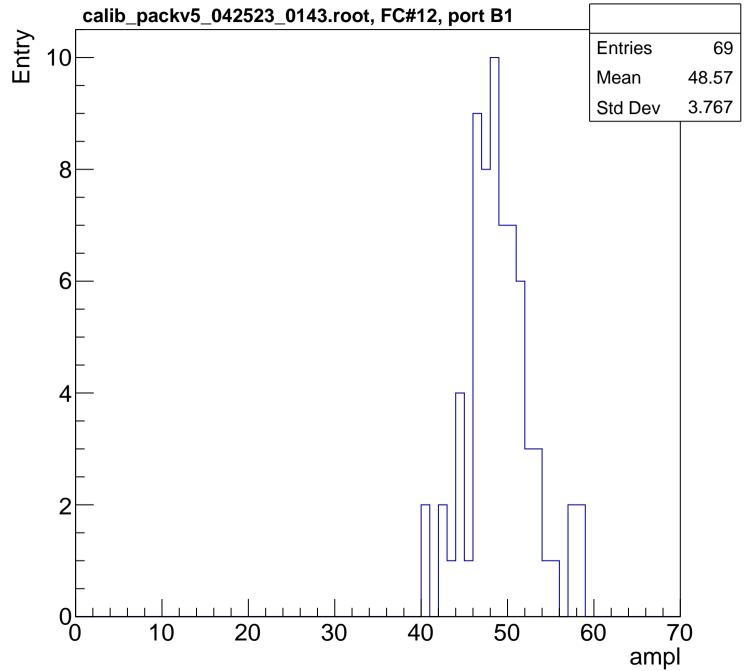


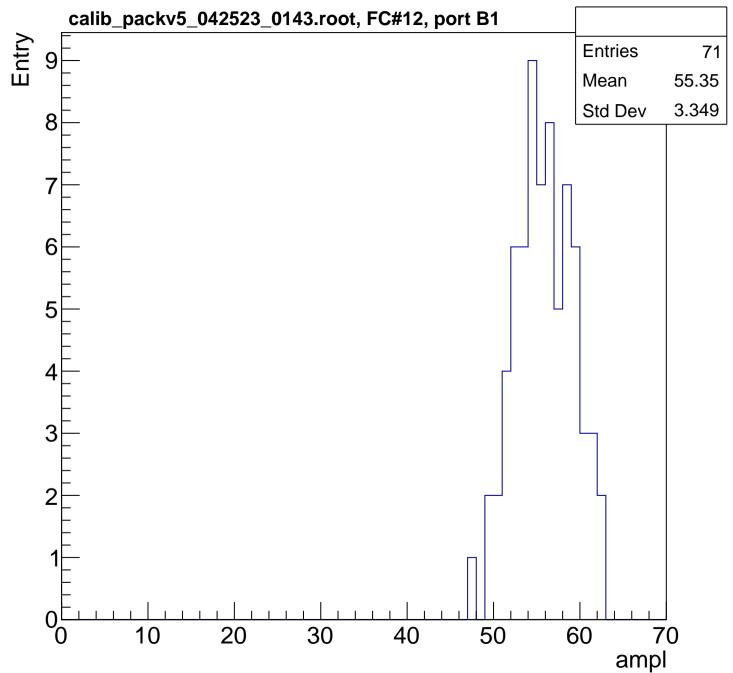


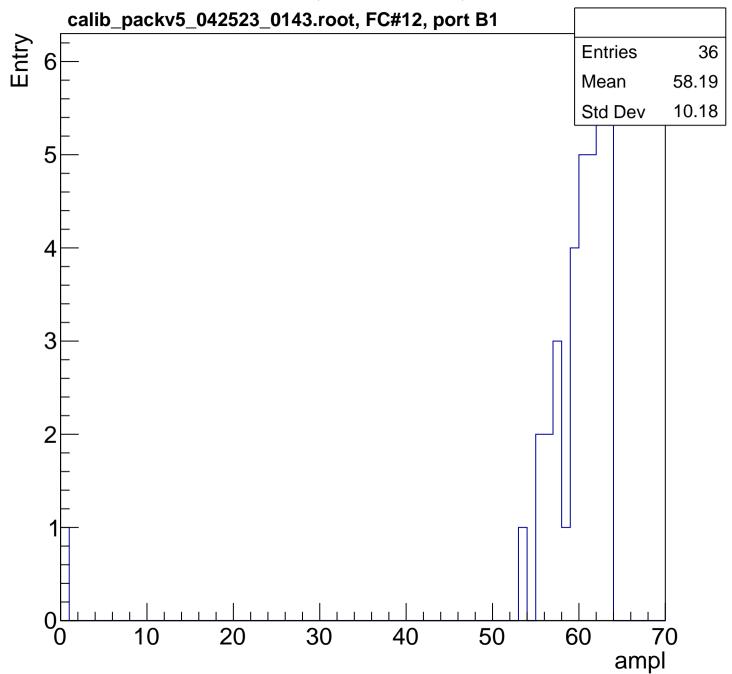


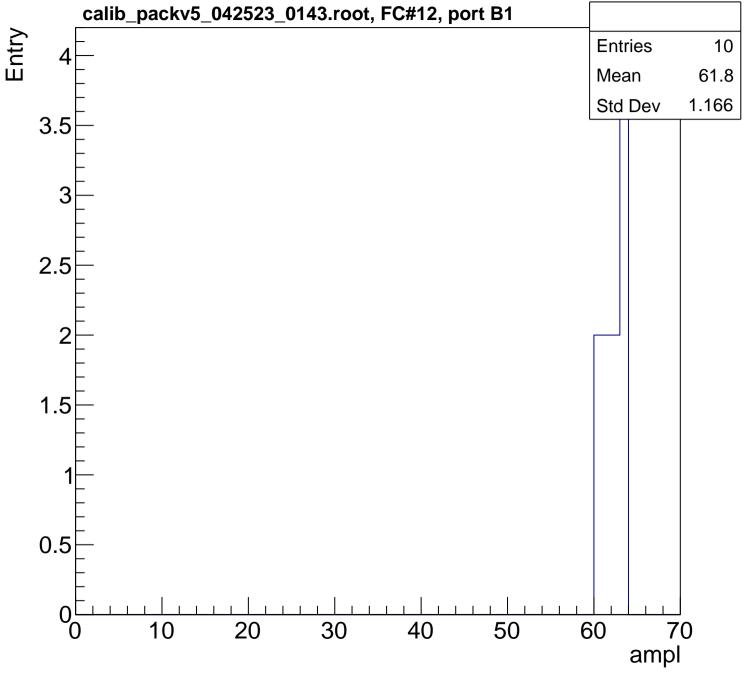




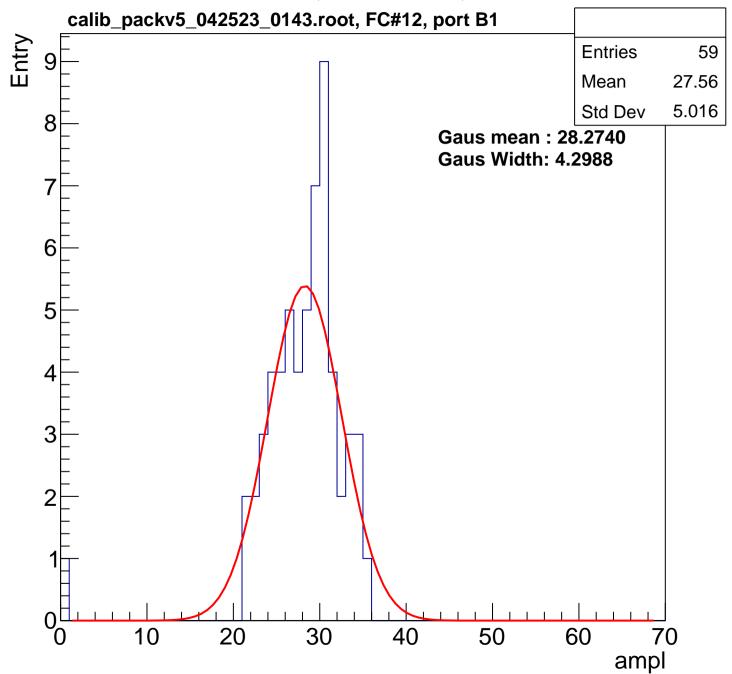


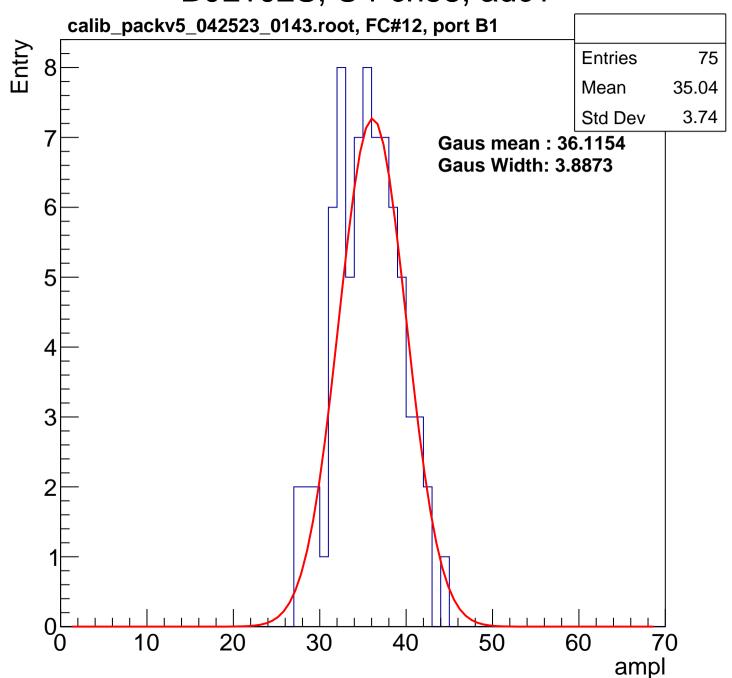


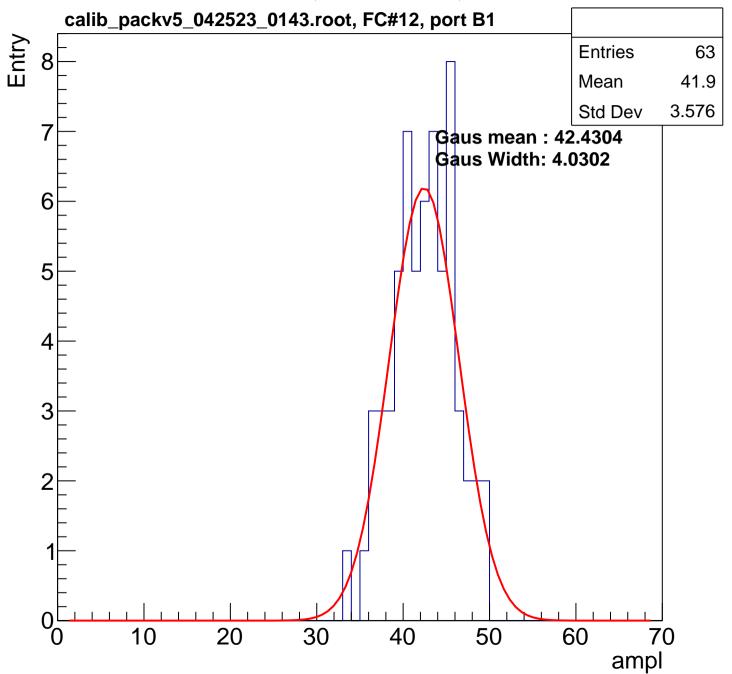


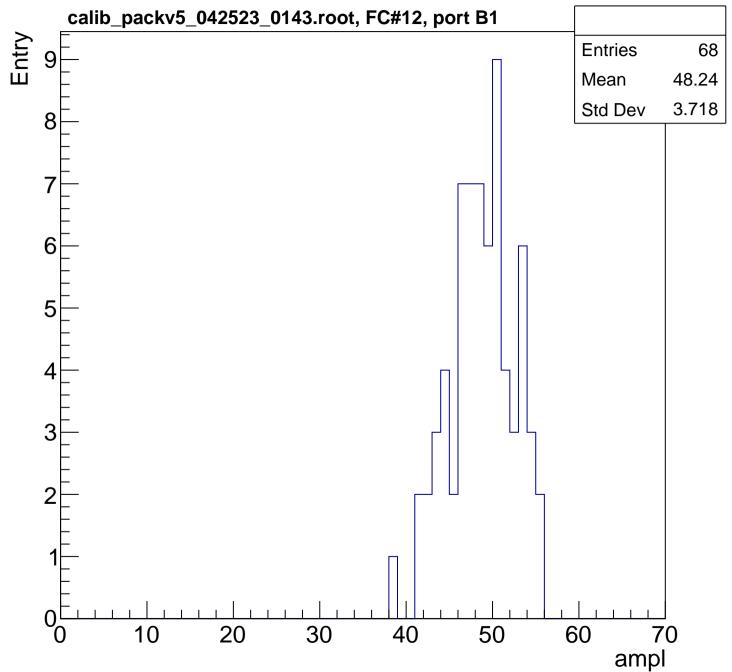


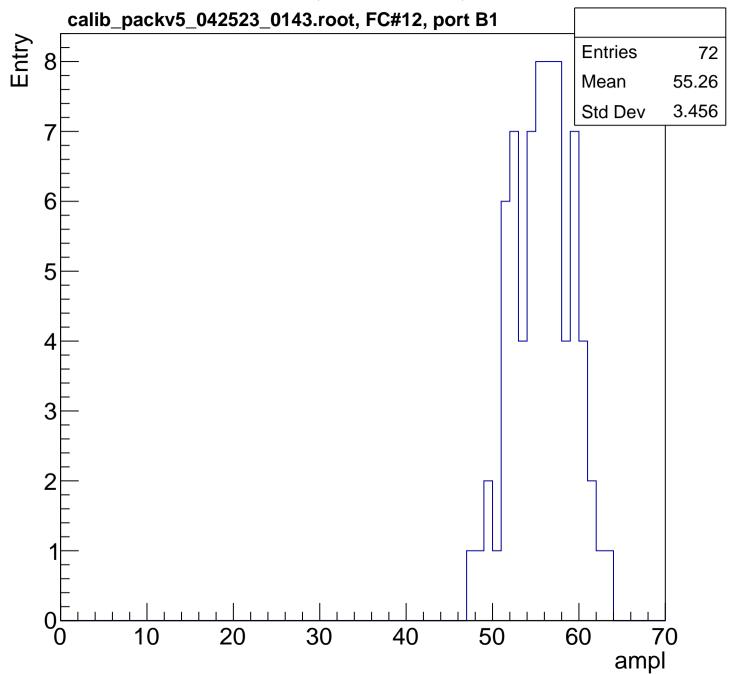
B0L102S, U4-ch57, adc7 calib_packv5_042523_0143.root, FC#12, port B1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

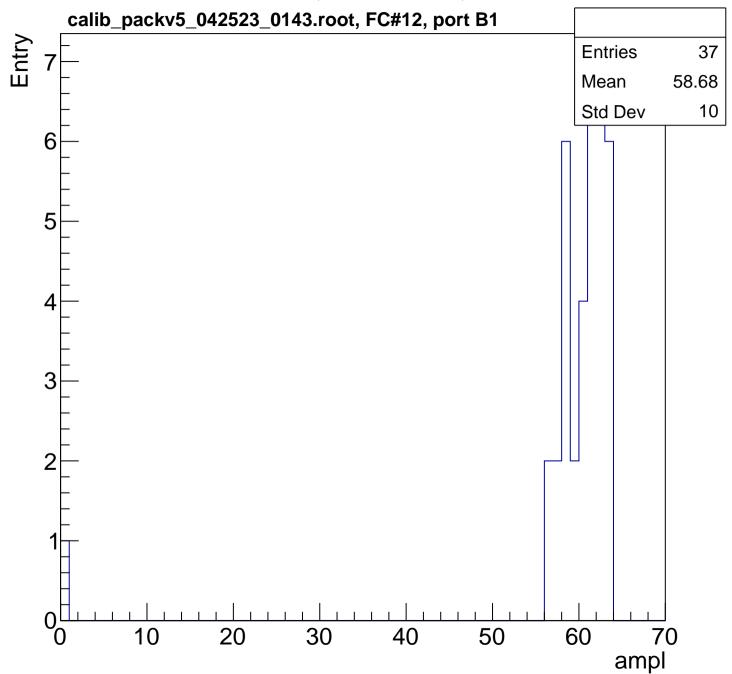


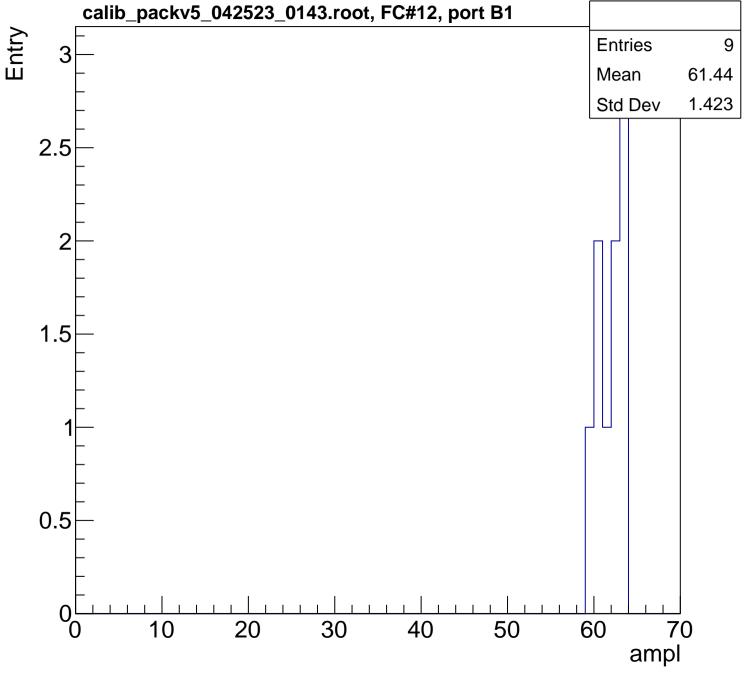




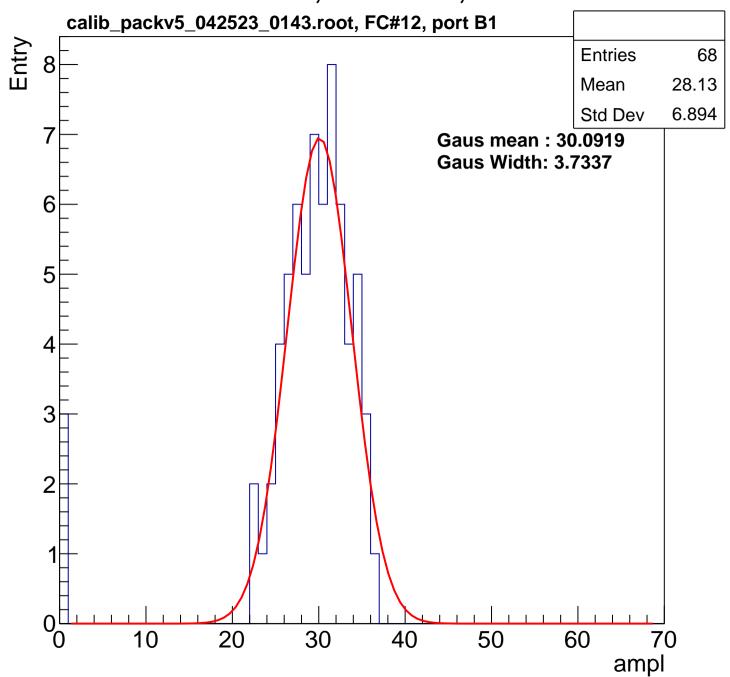


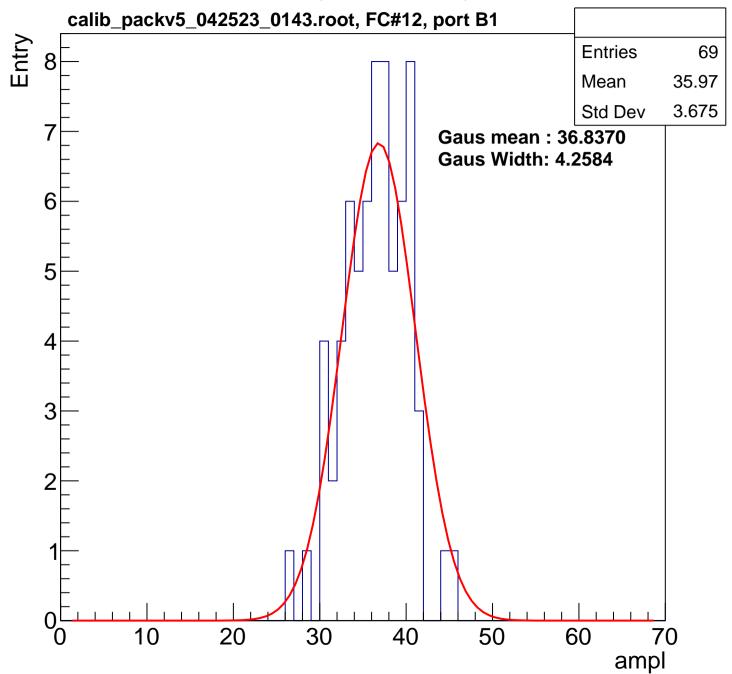


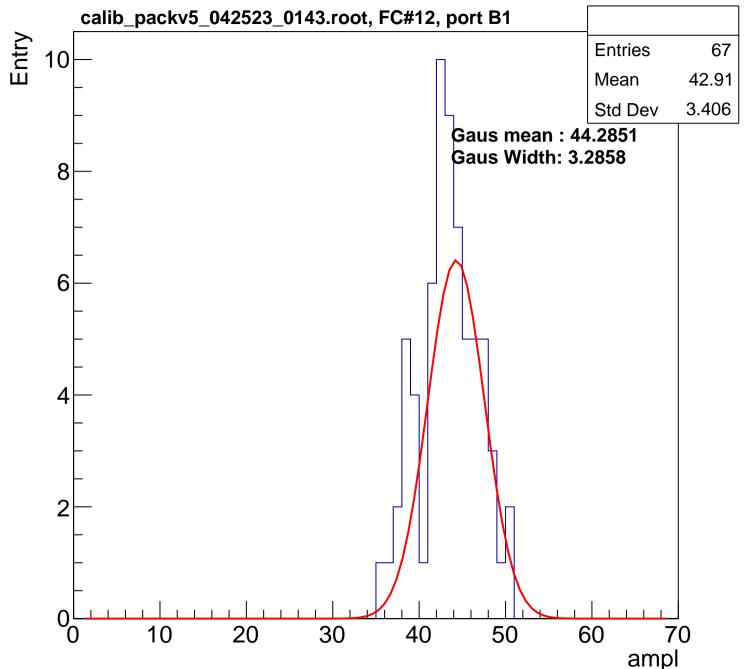


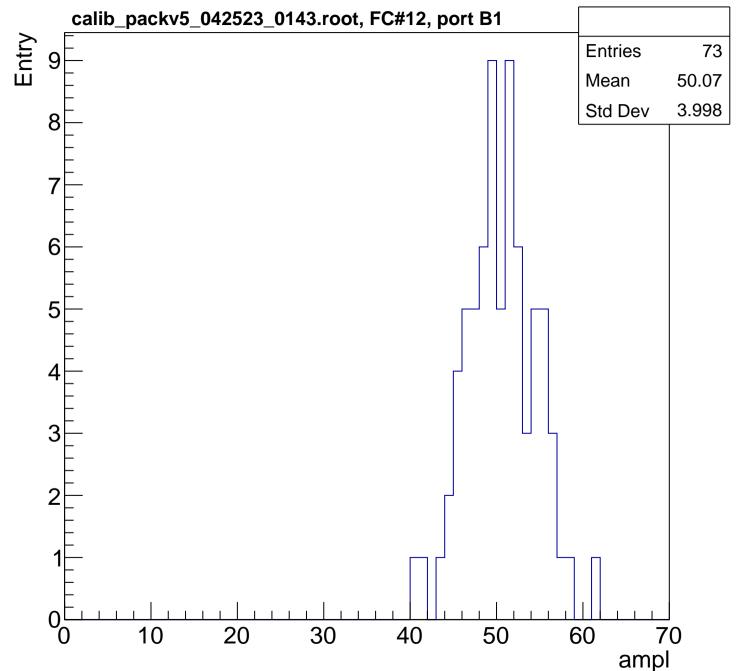


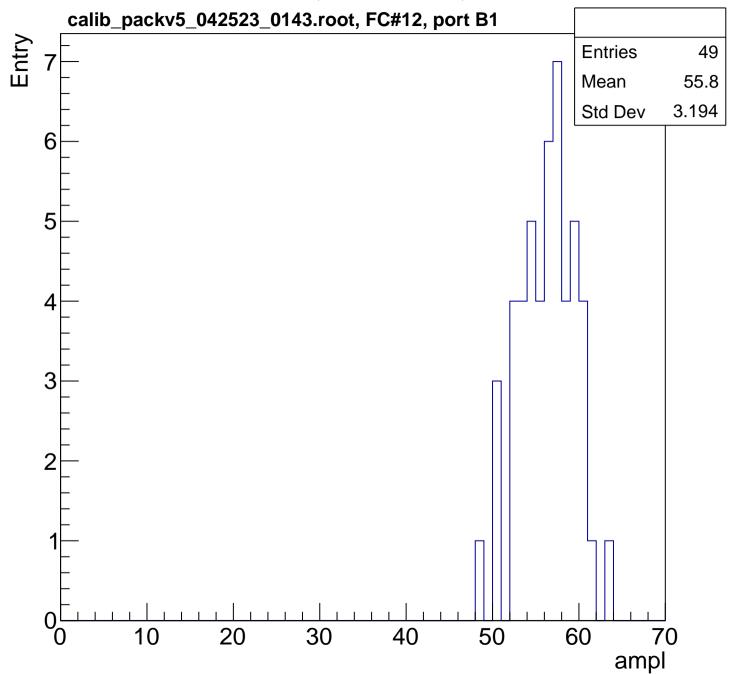


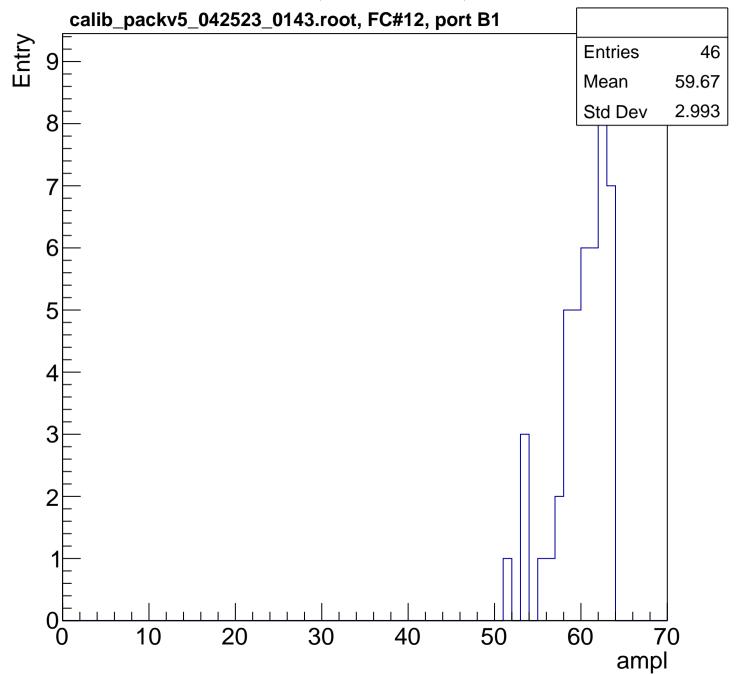


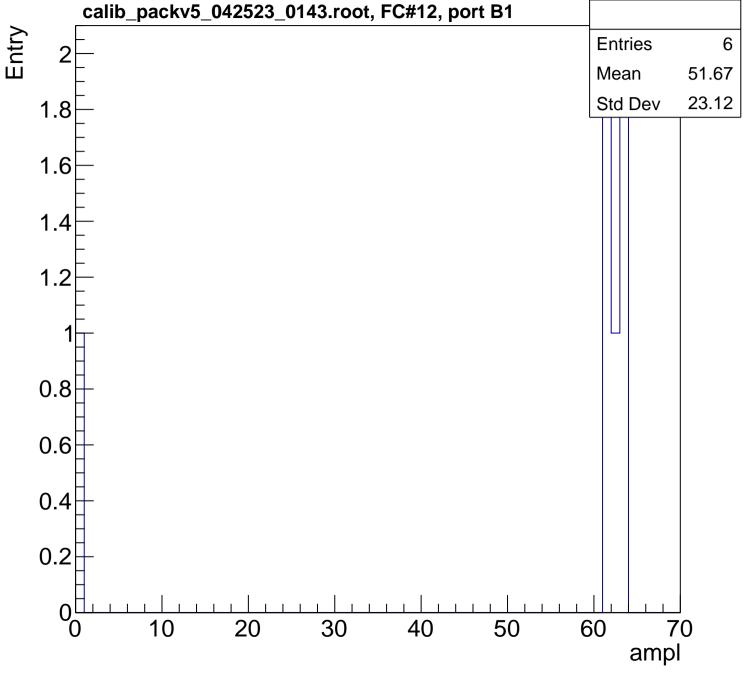


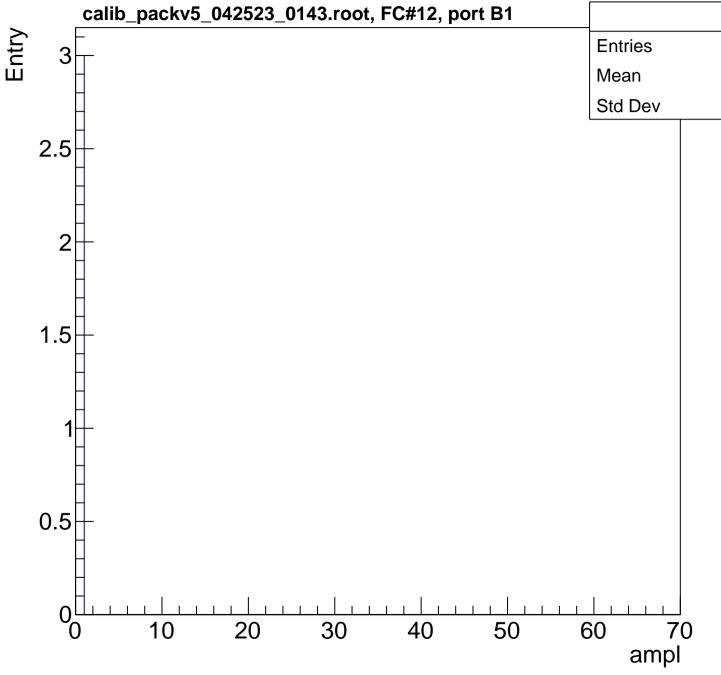


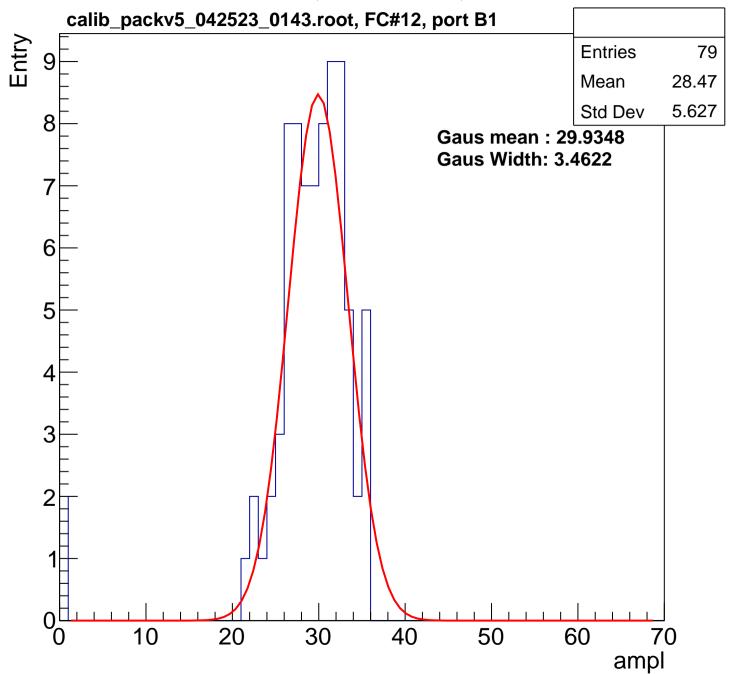


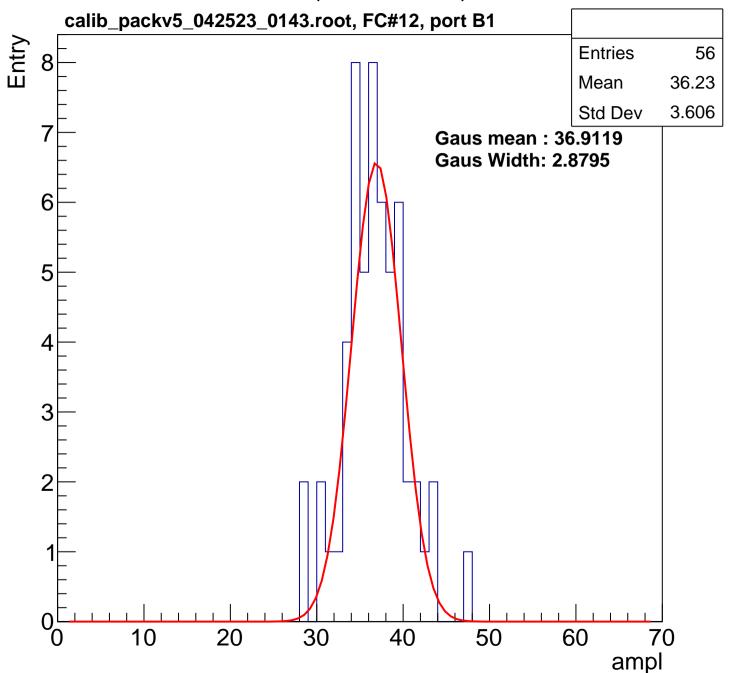


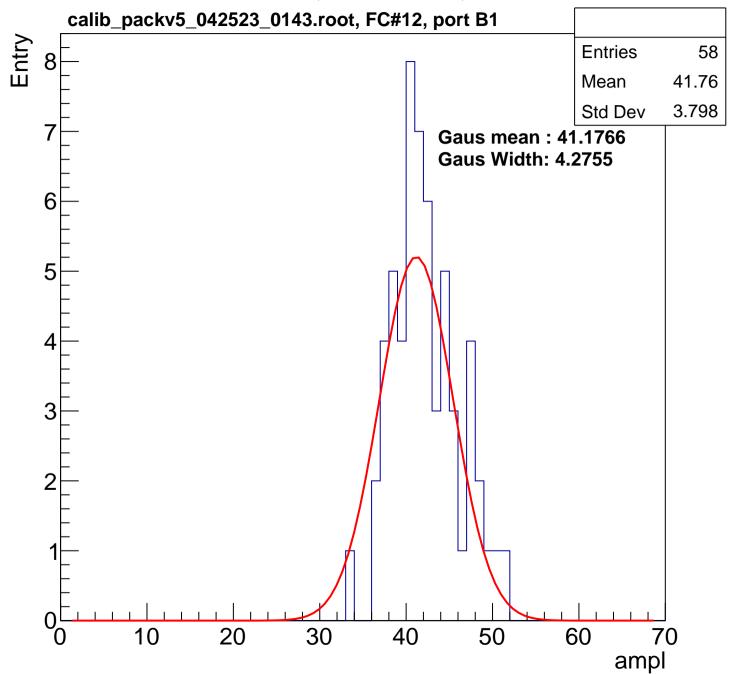


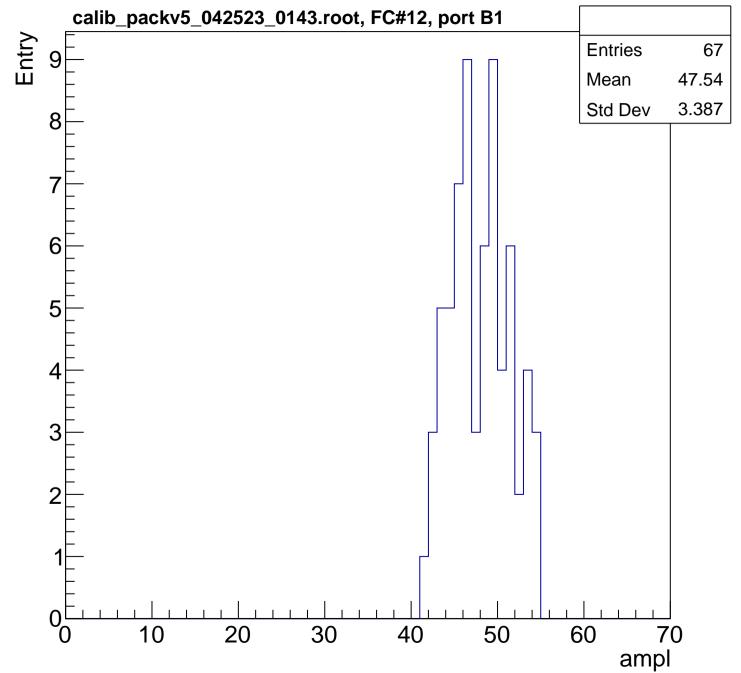


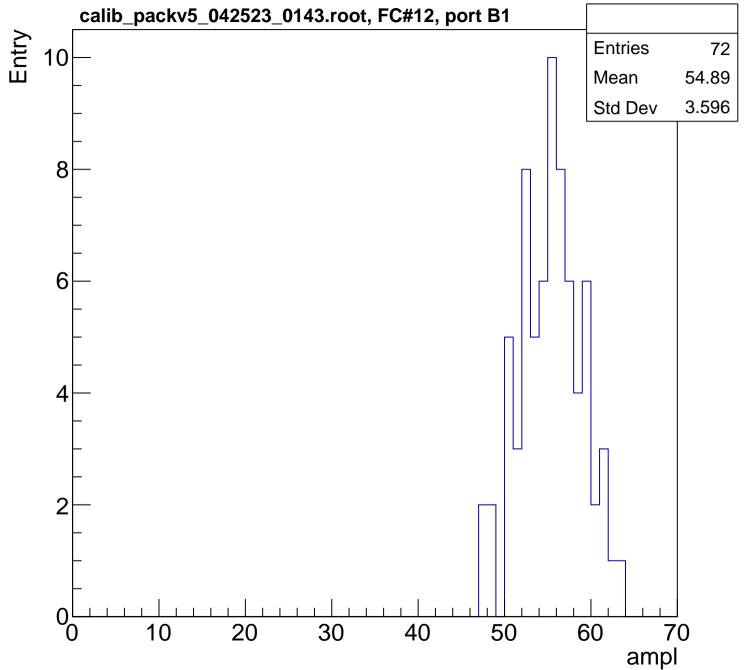


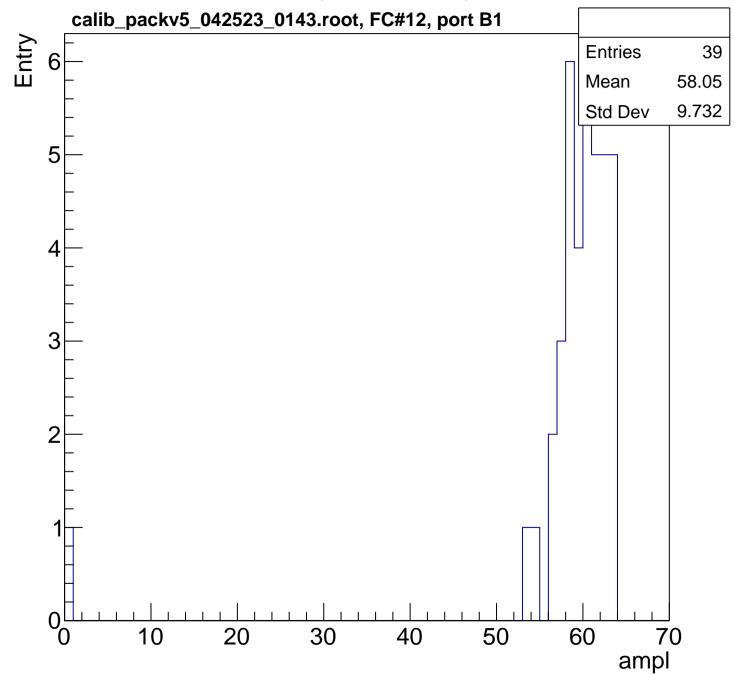


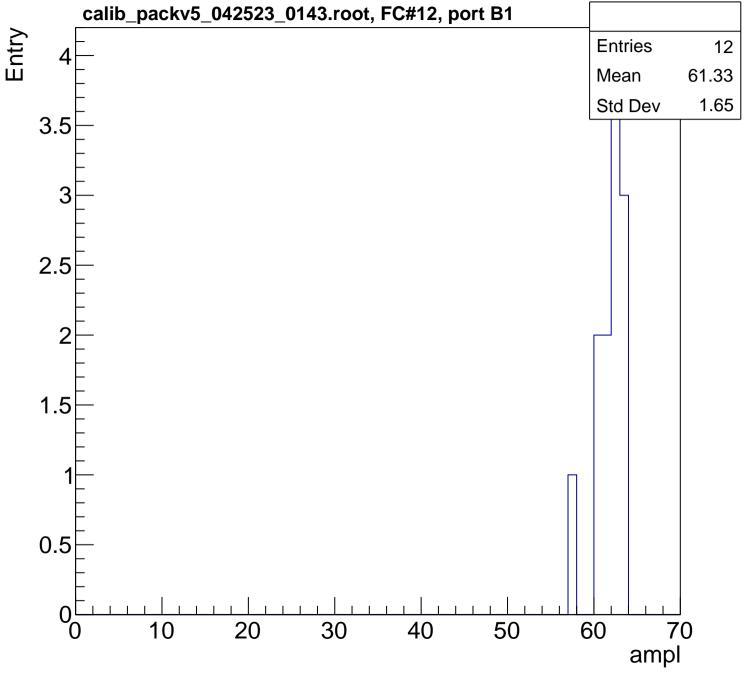


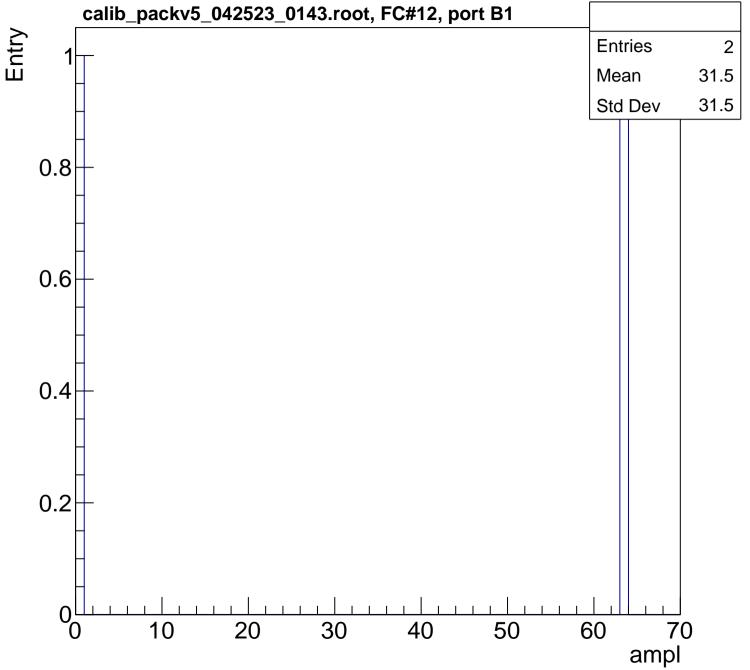


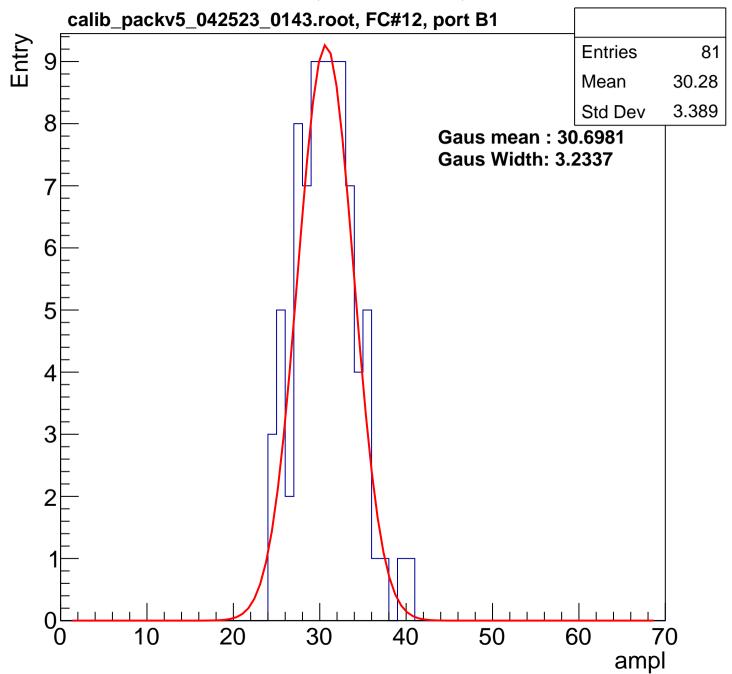


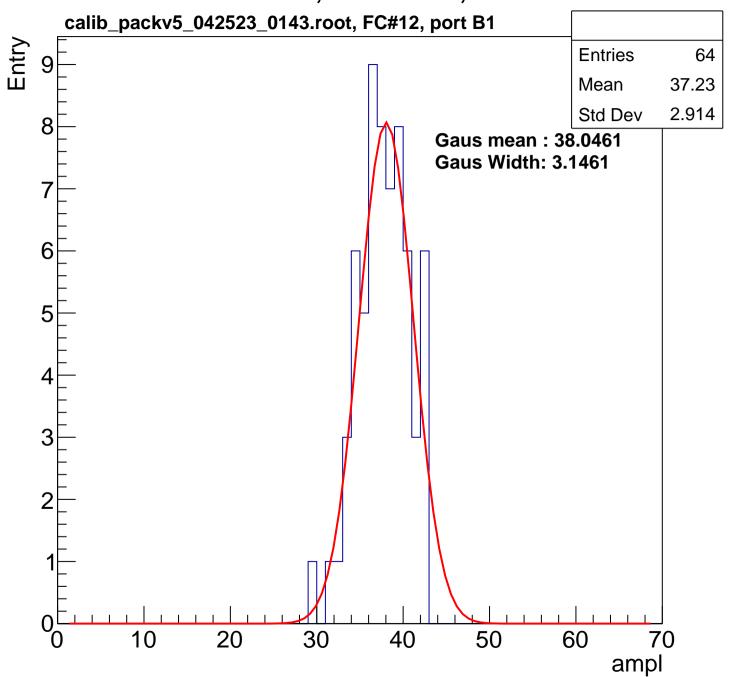


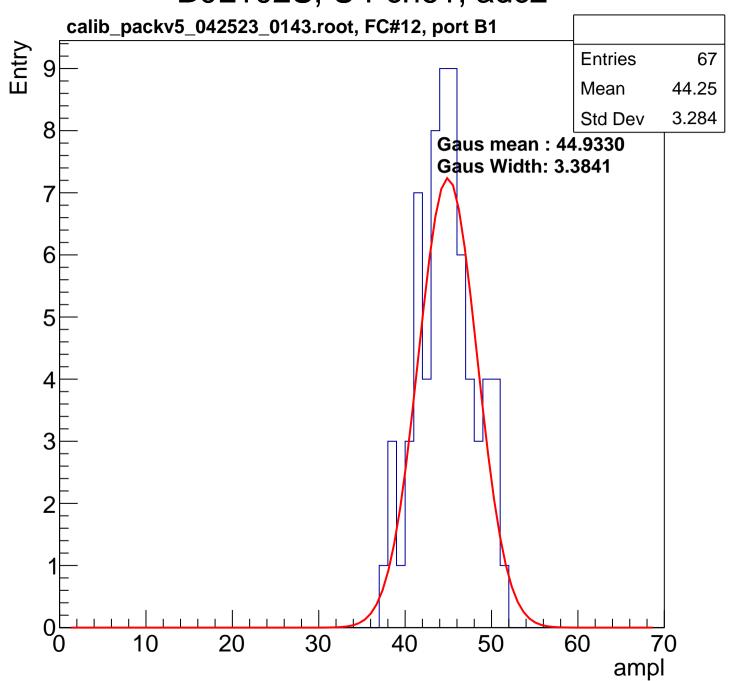


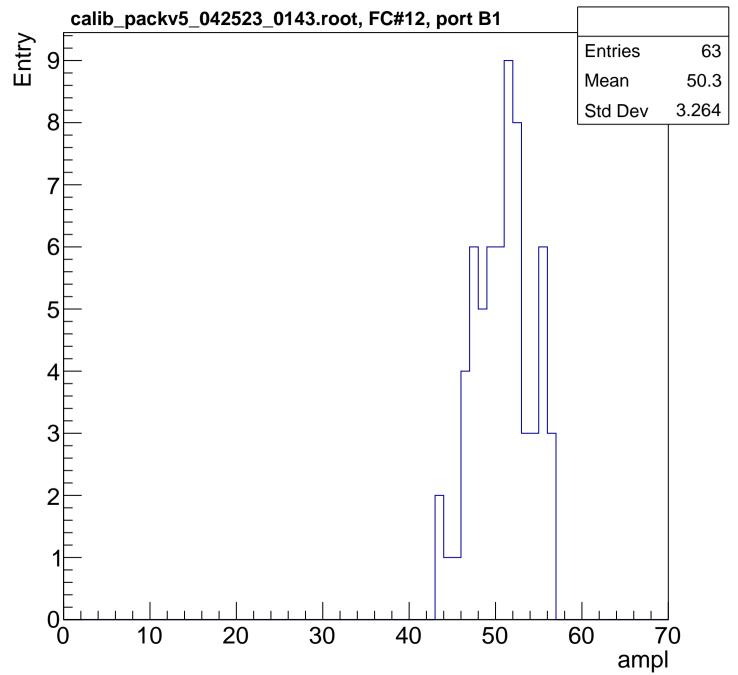


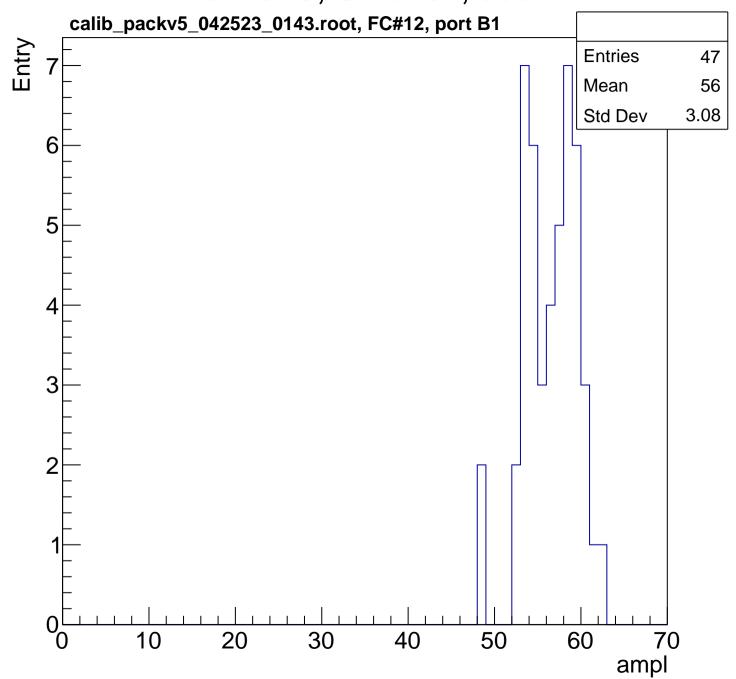


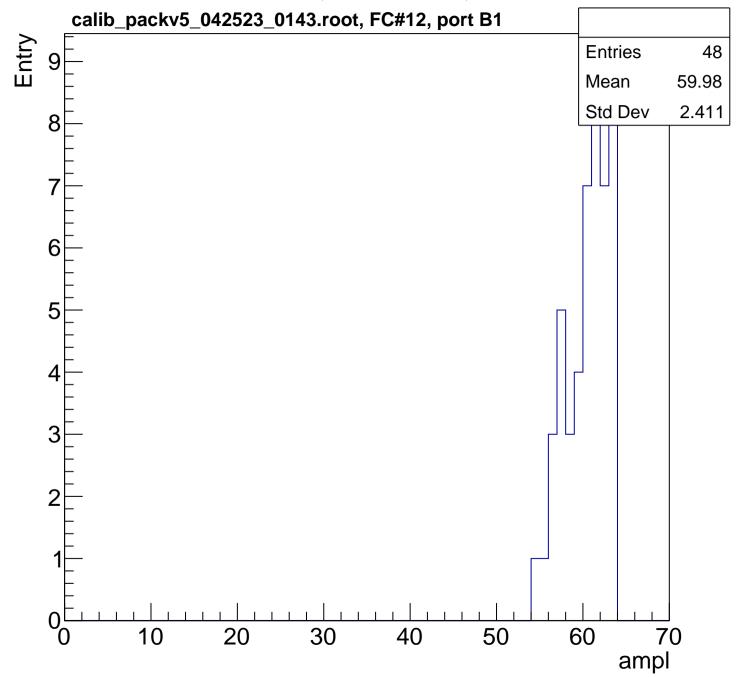


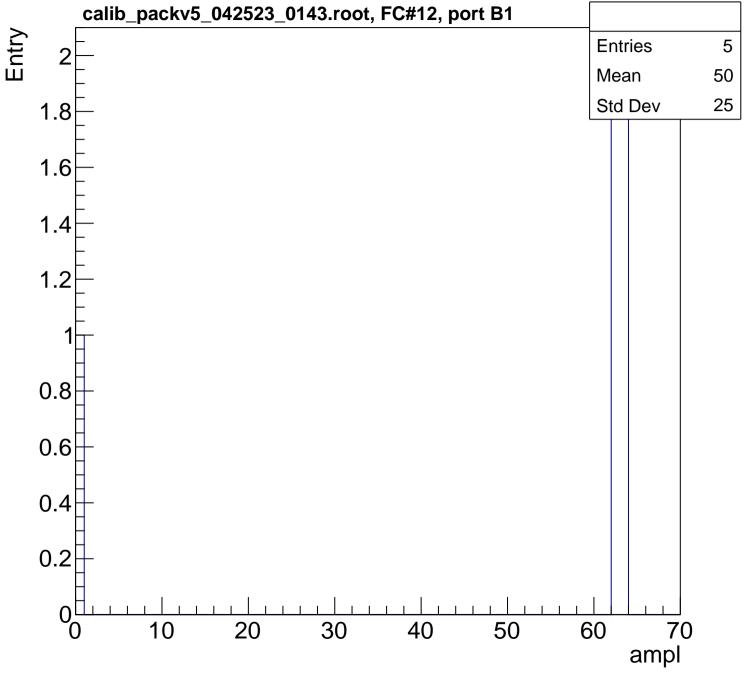


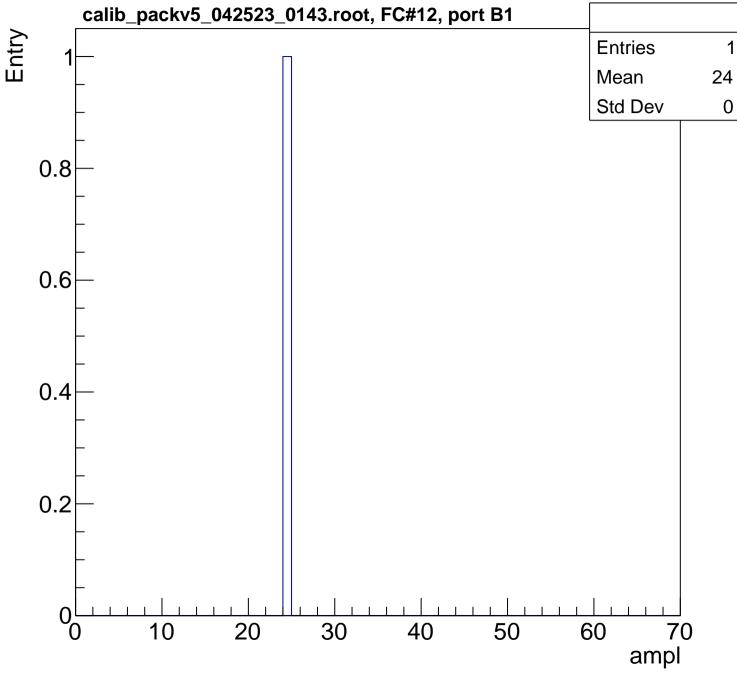


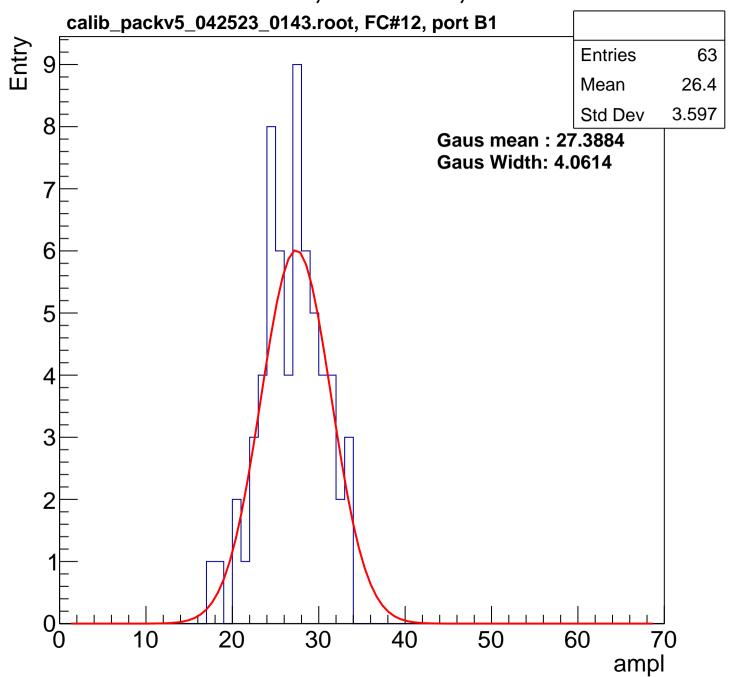


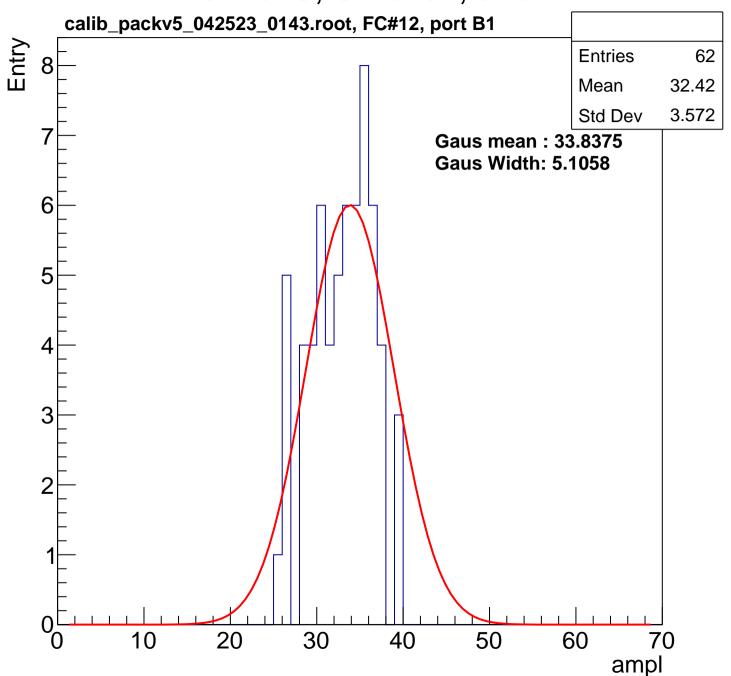


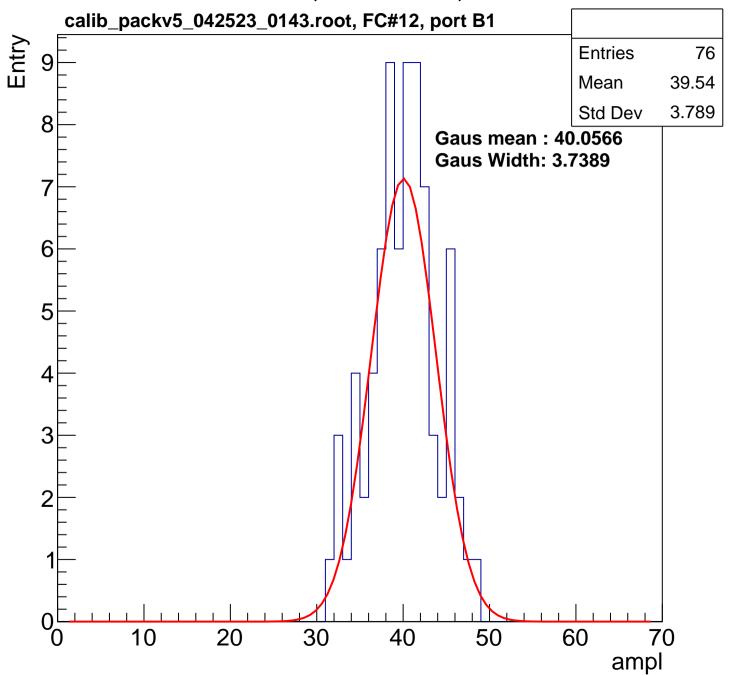


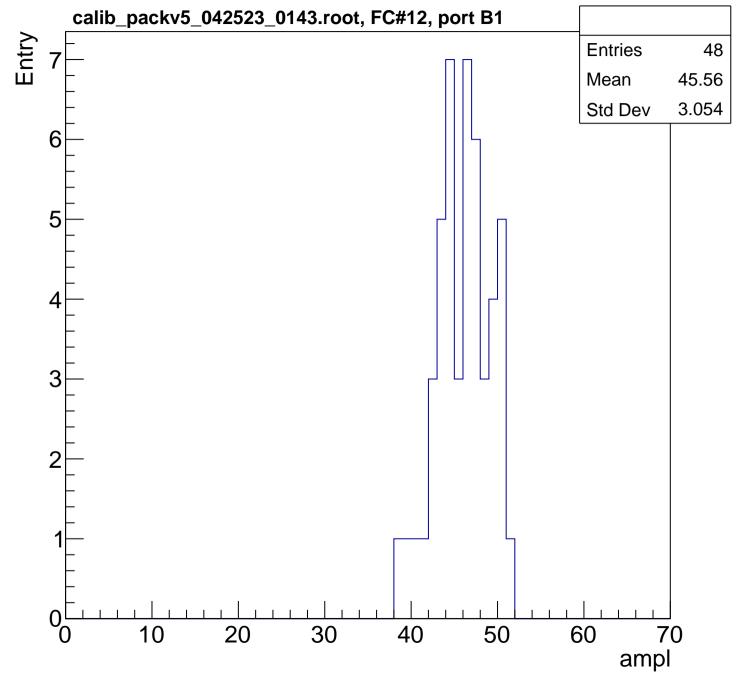


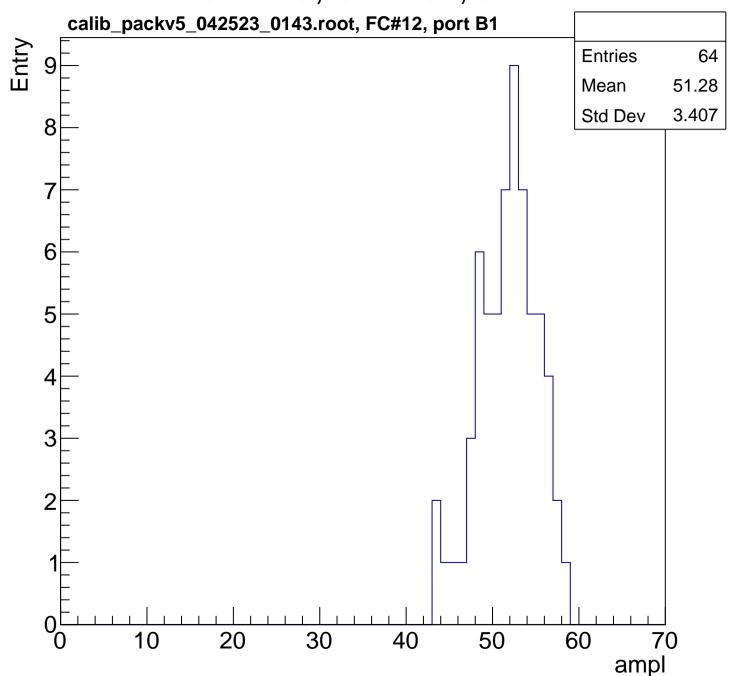


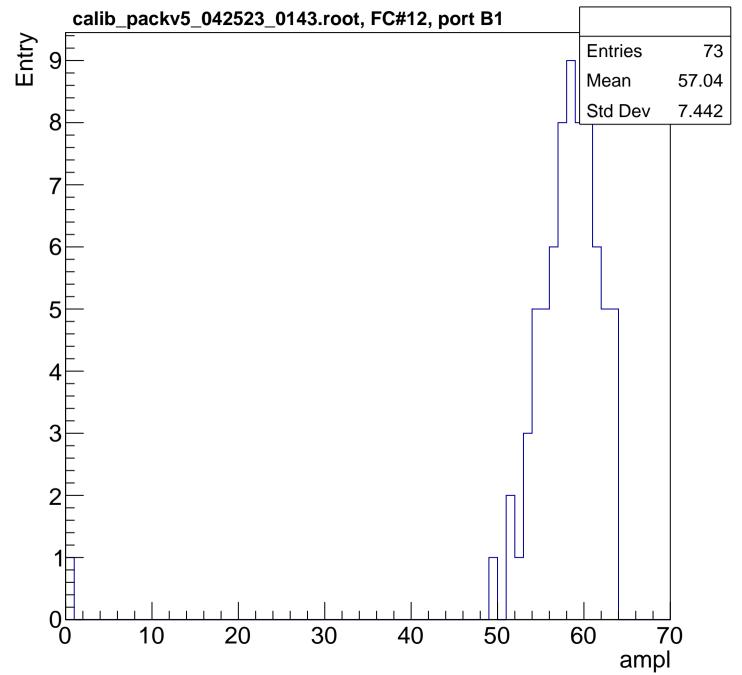


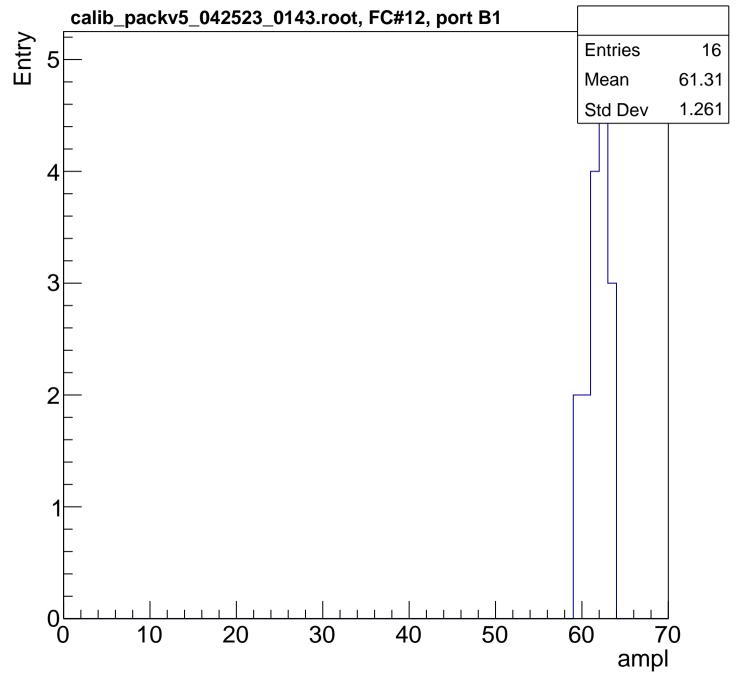


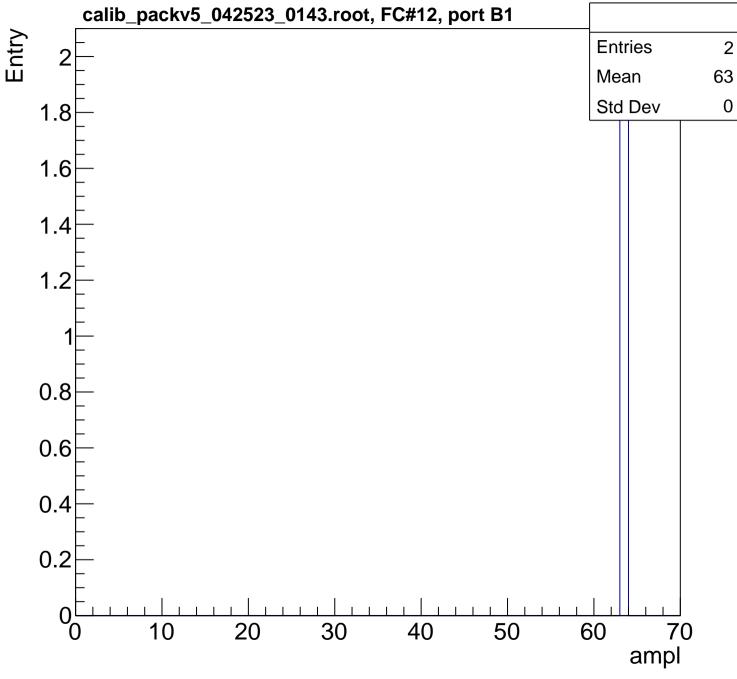


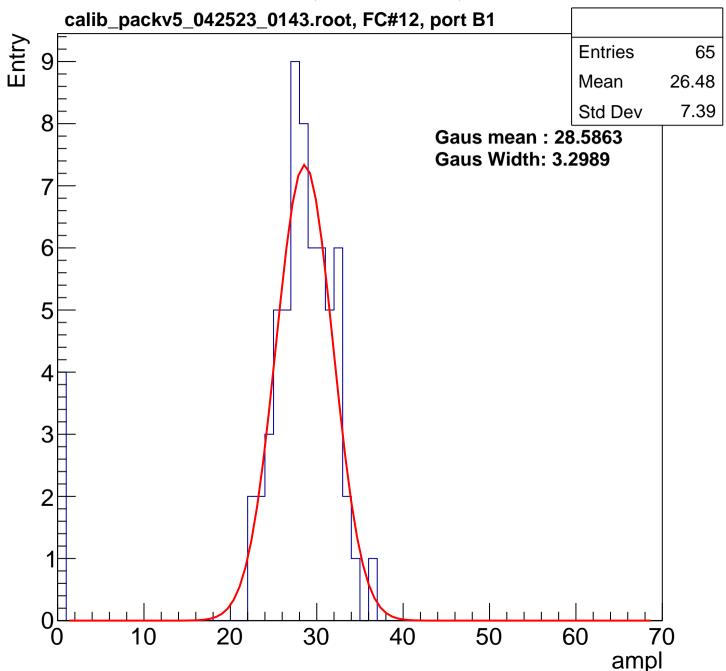


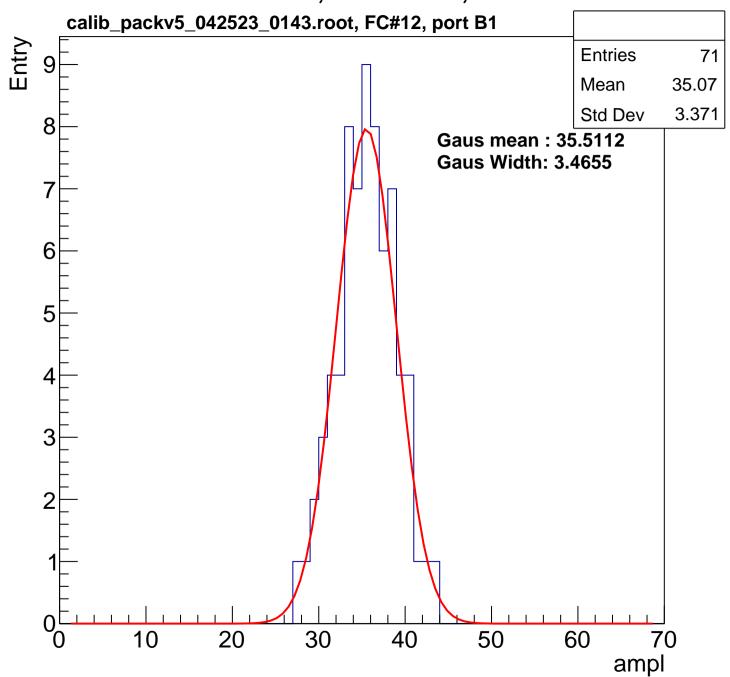


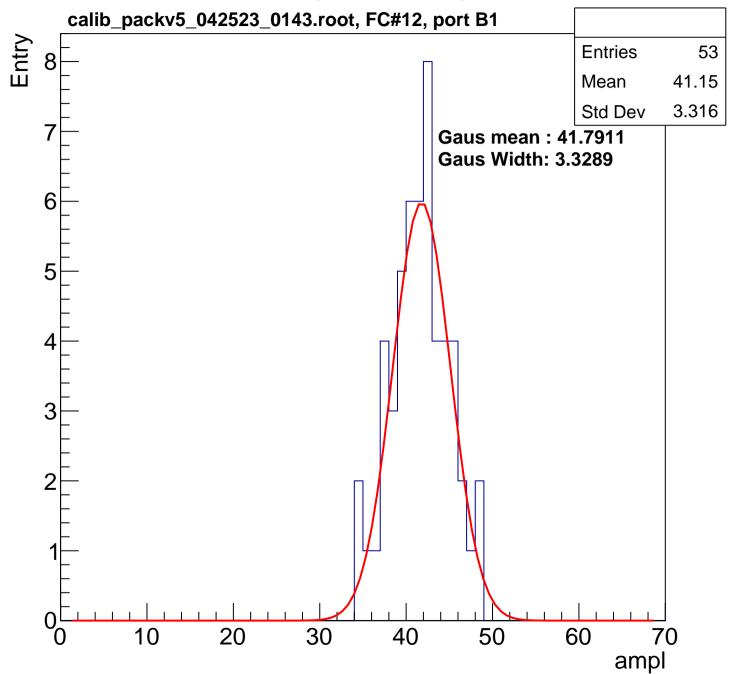


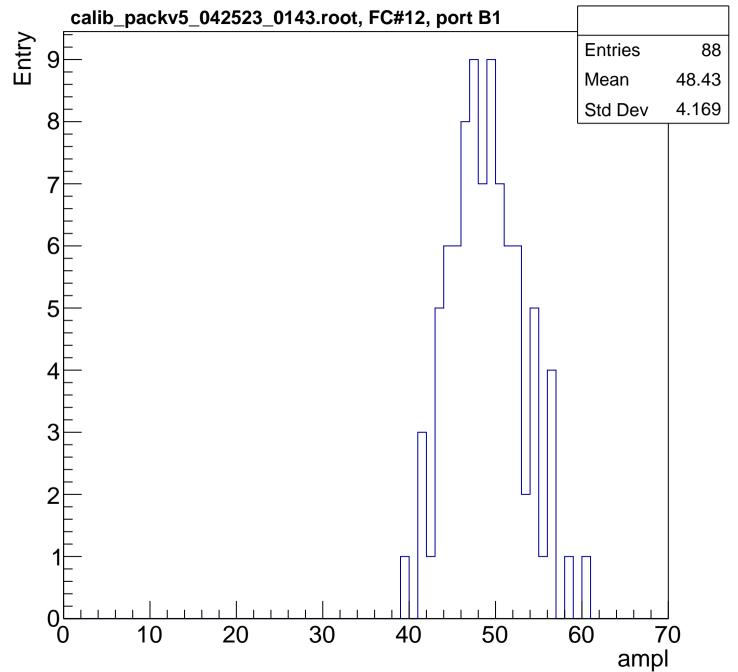


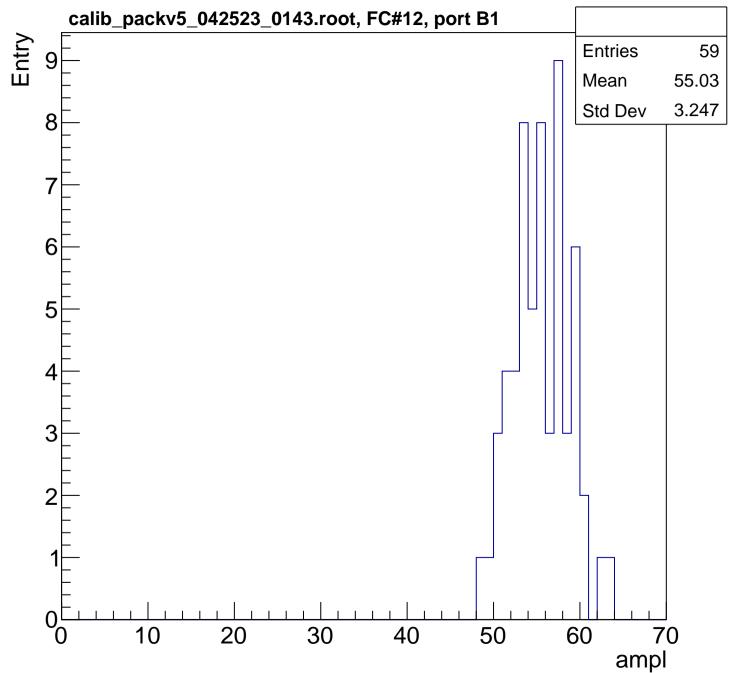


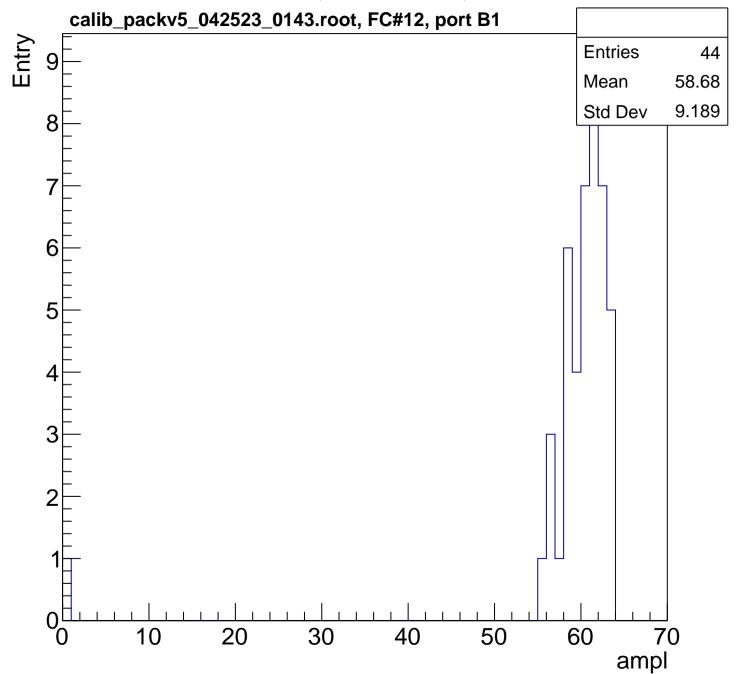


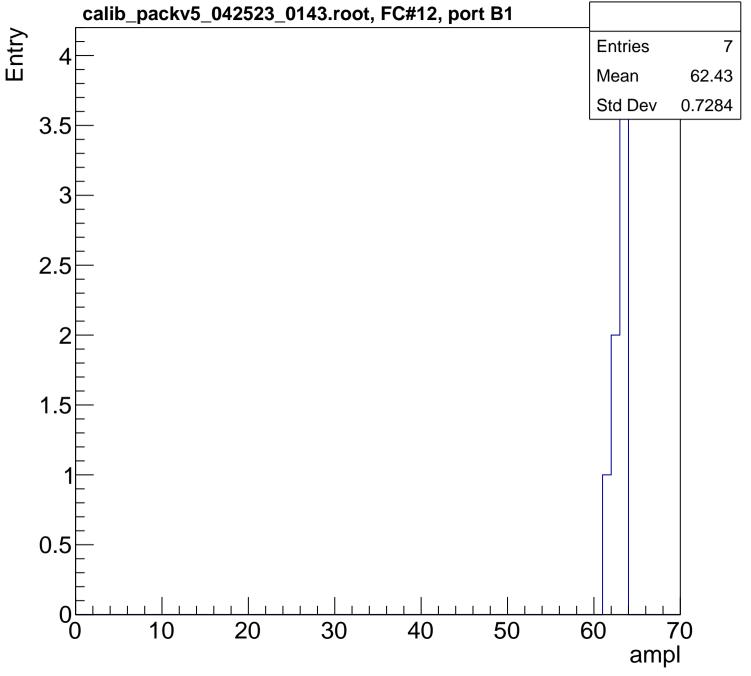


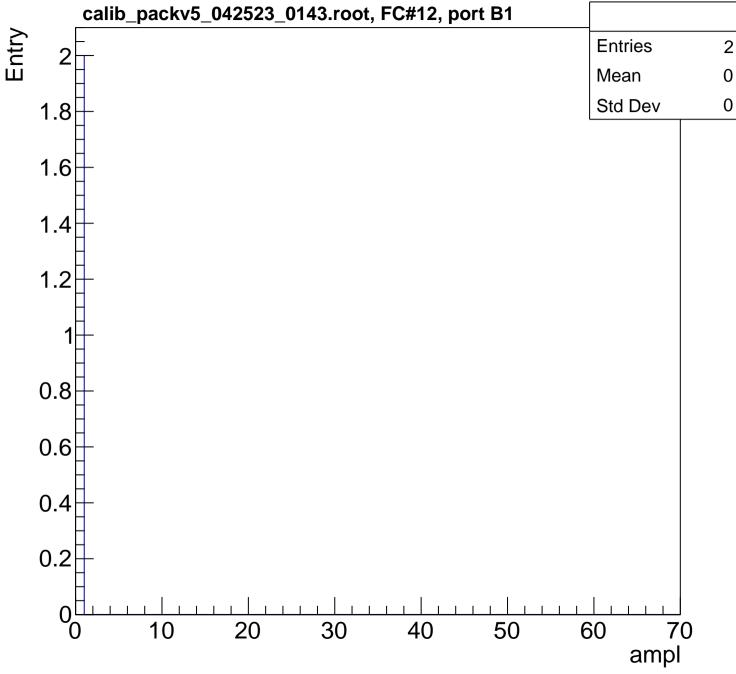


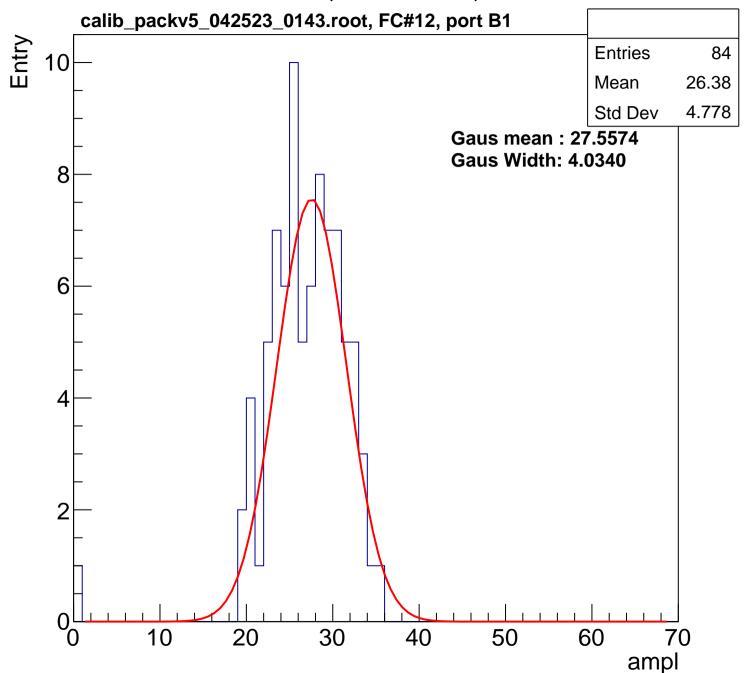


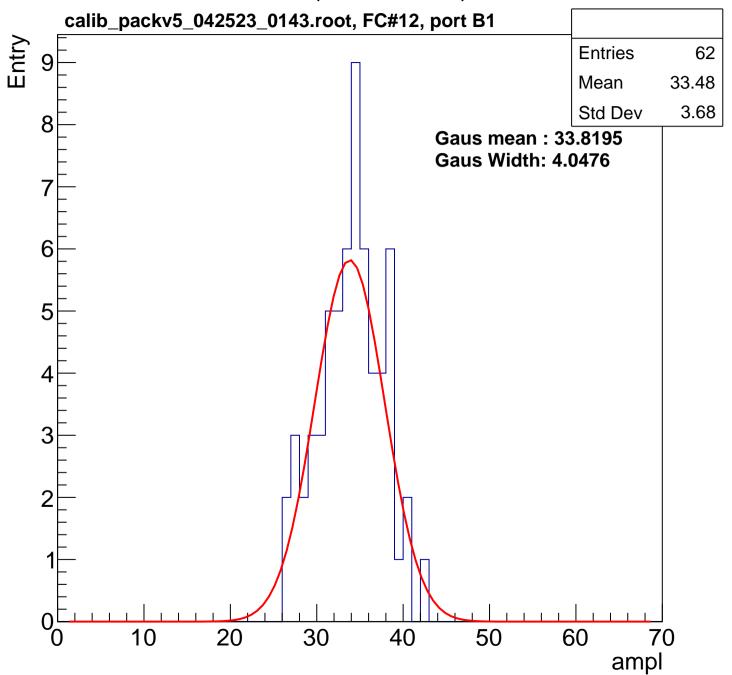


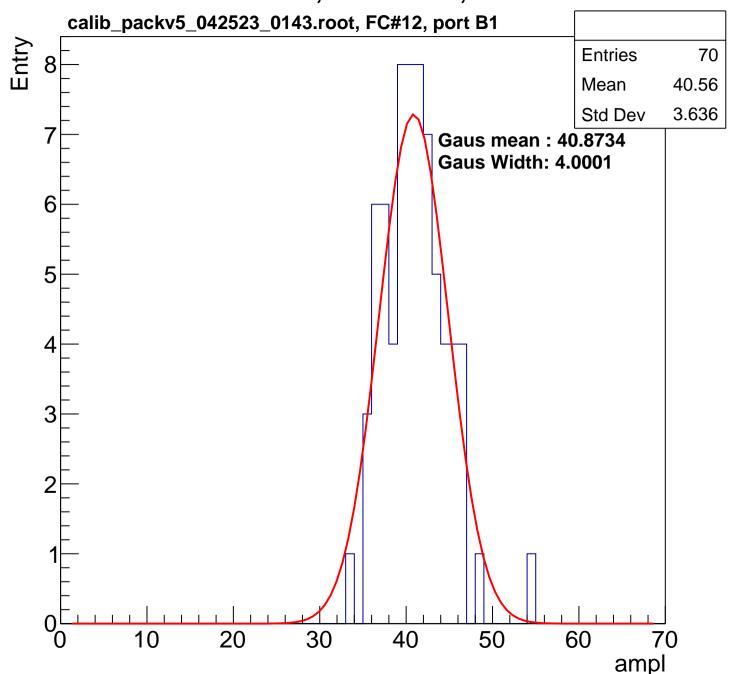


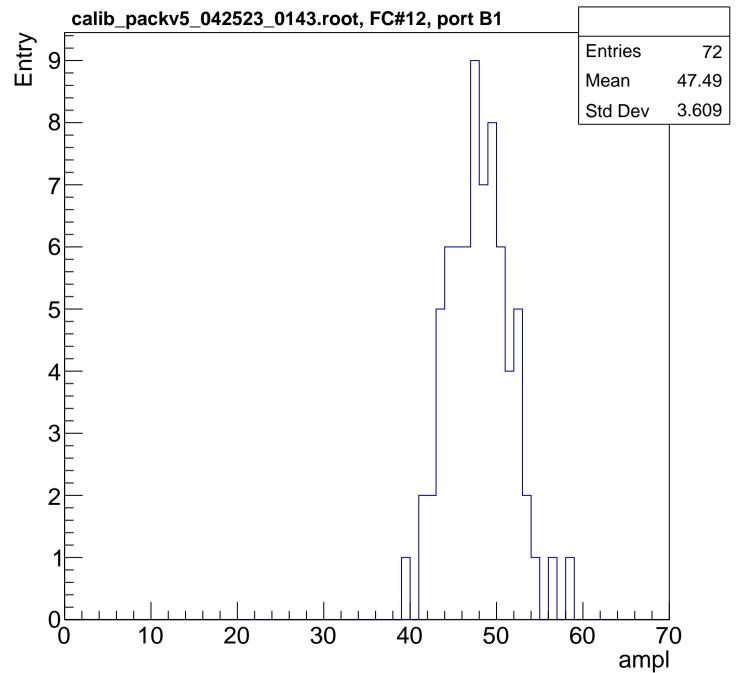


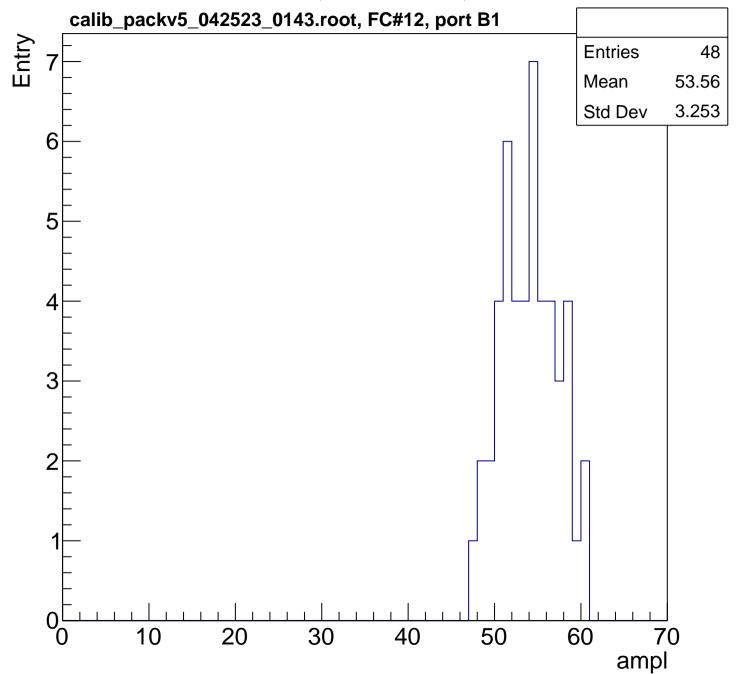


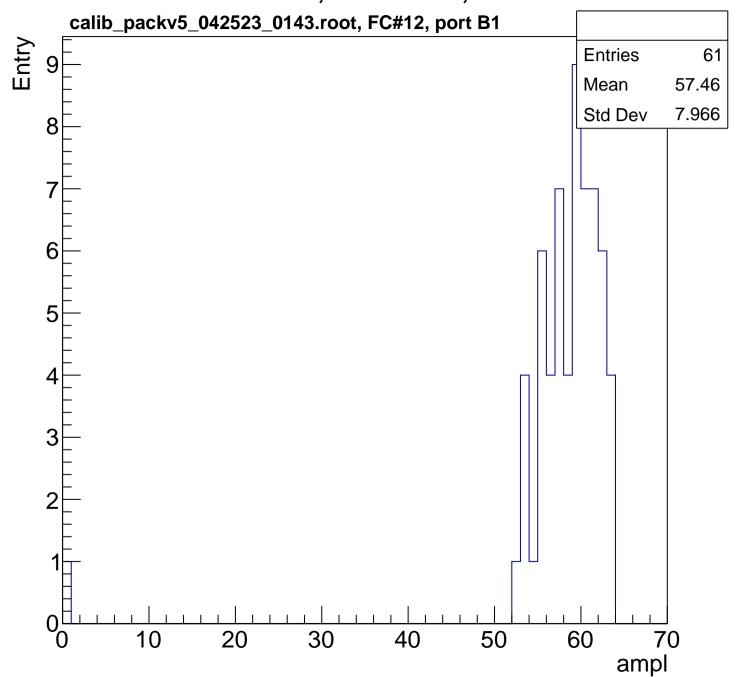


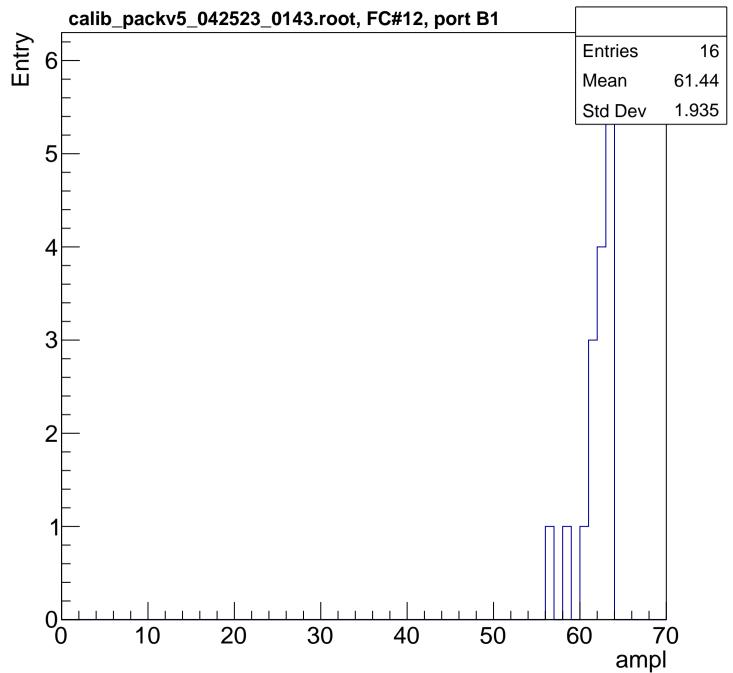




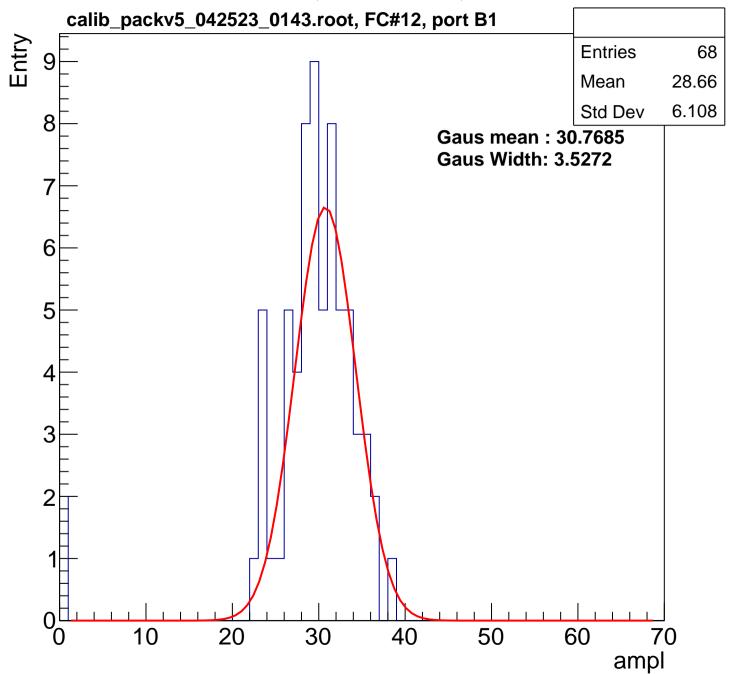


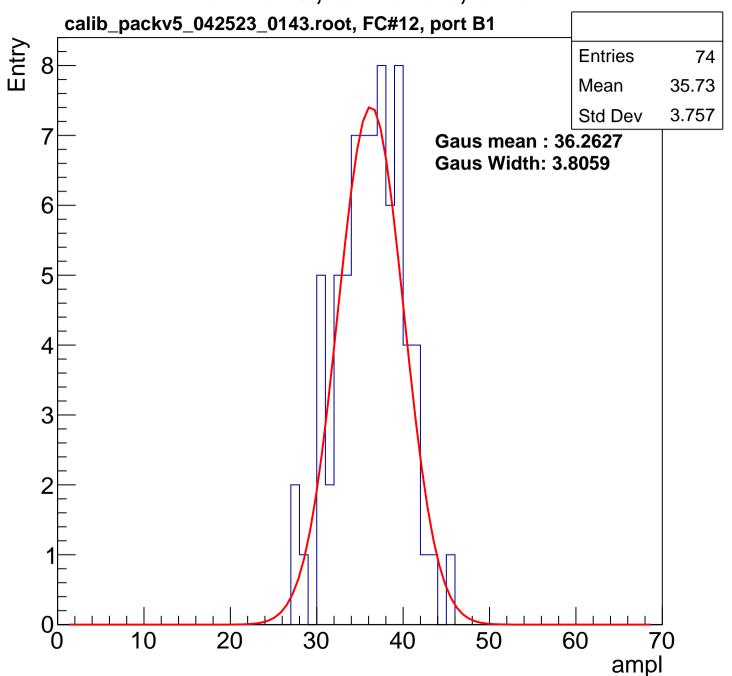


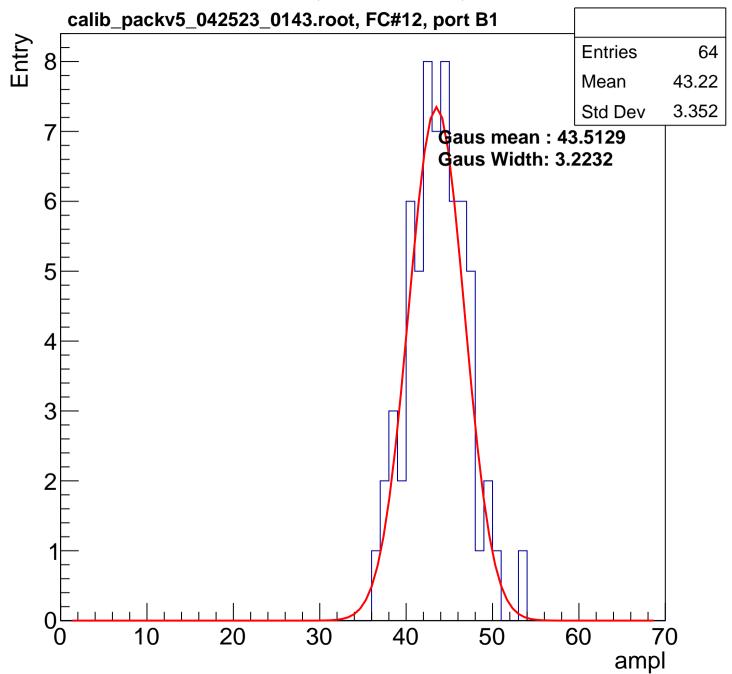


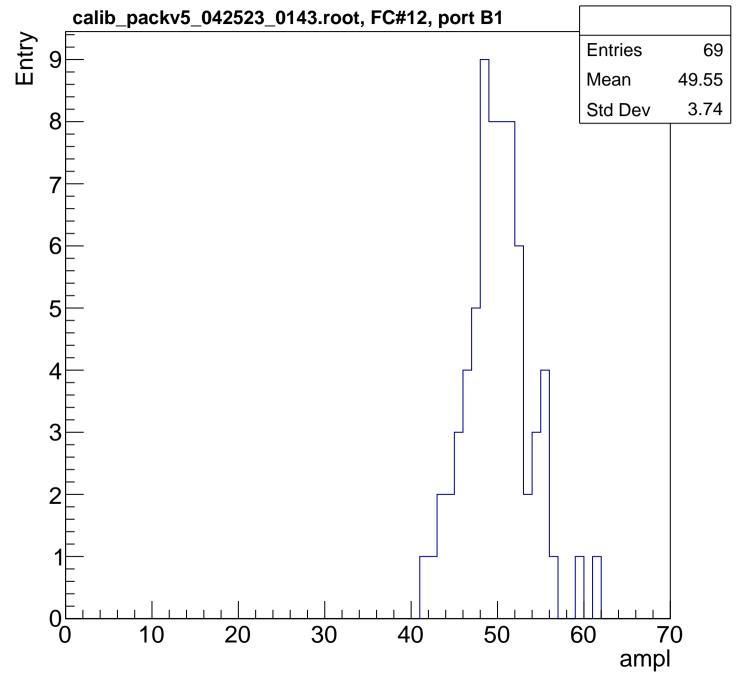


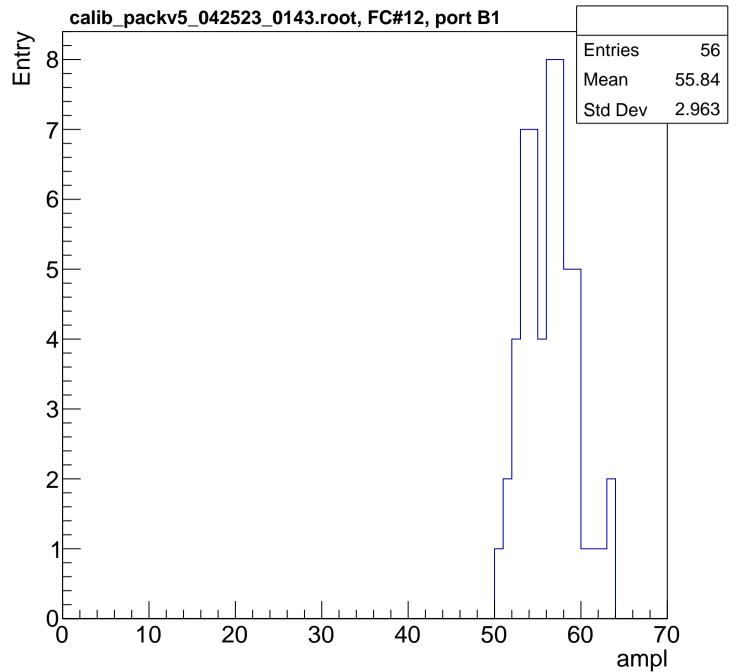


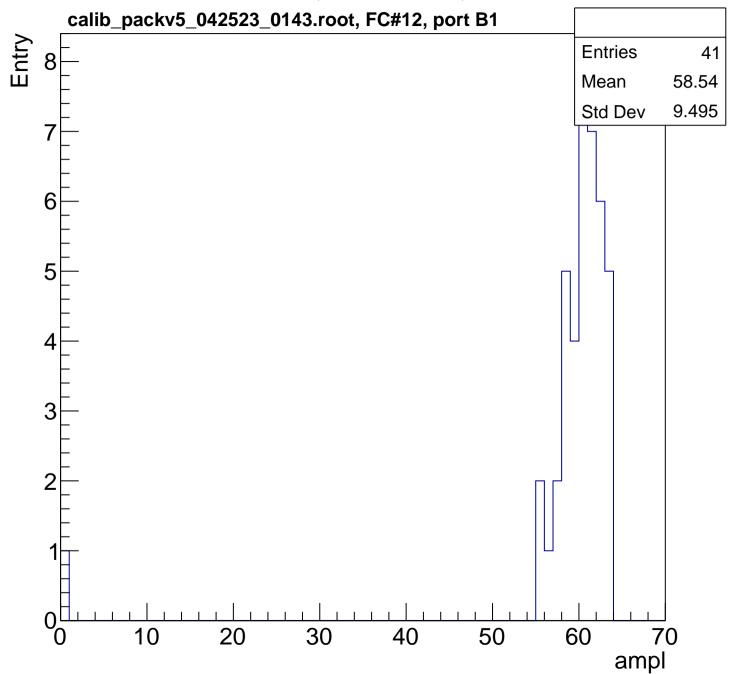


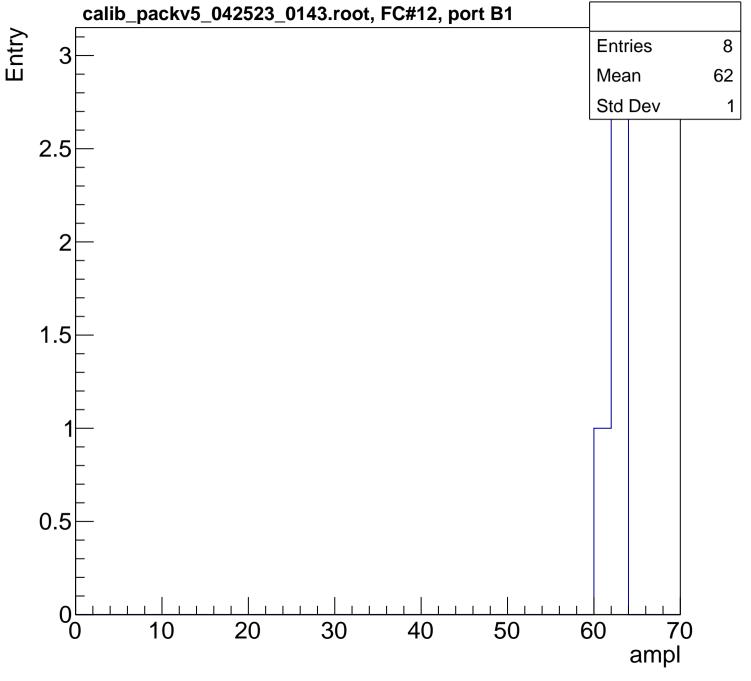




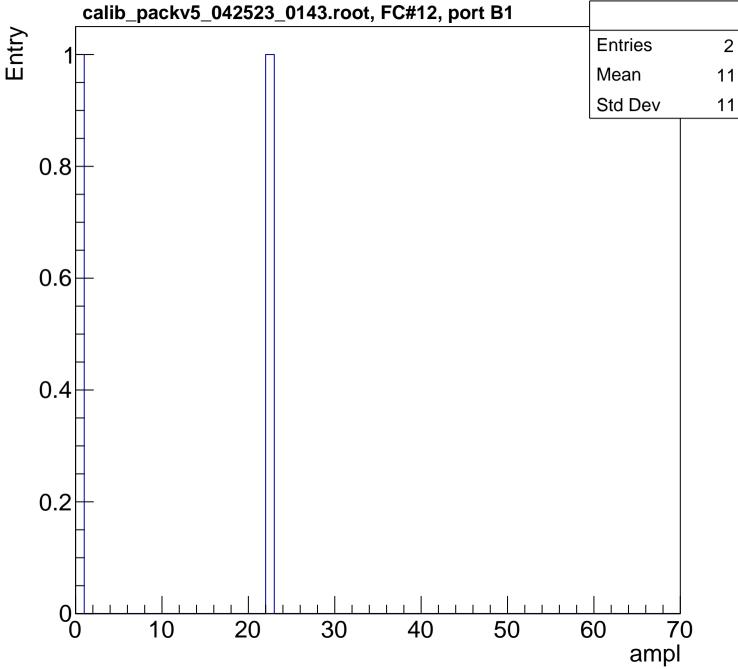


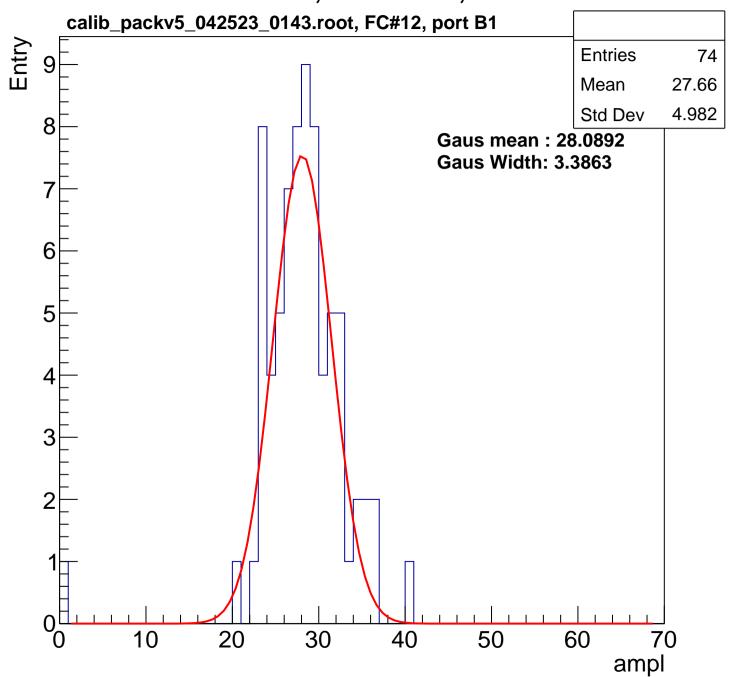


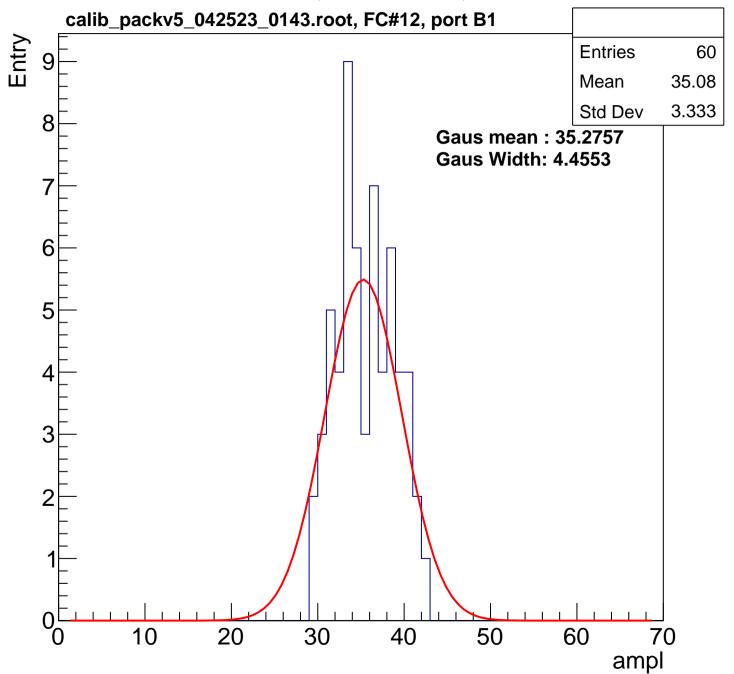


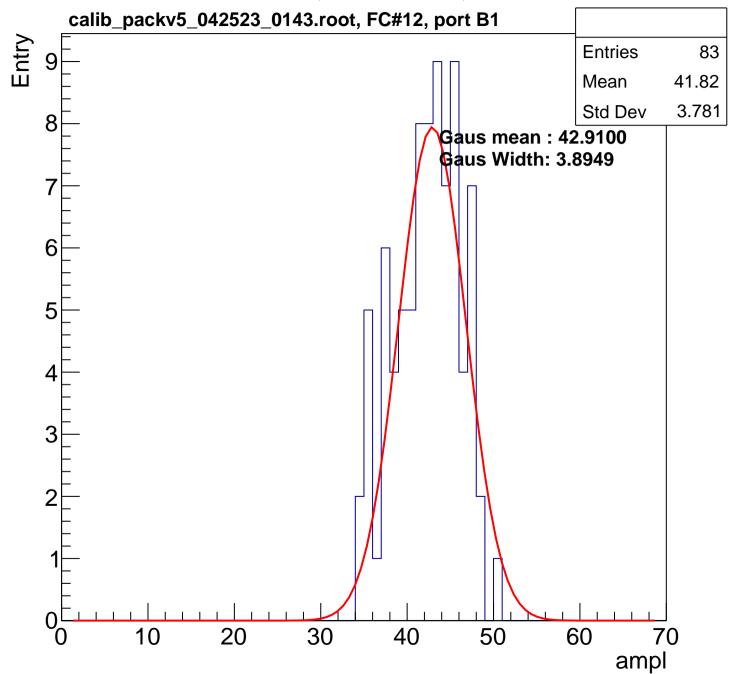


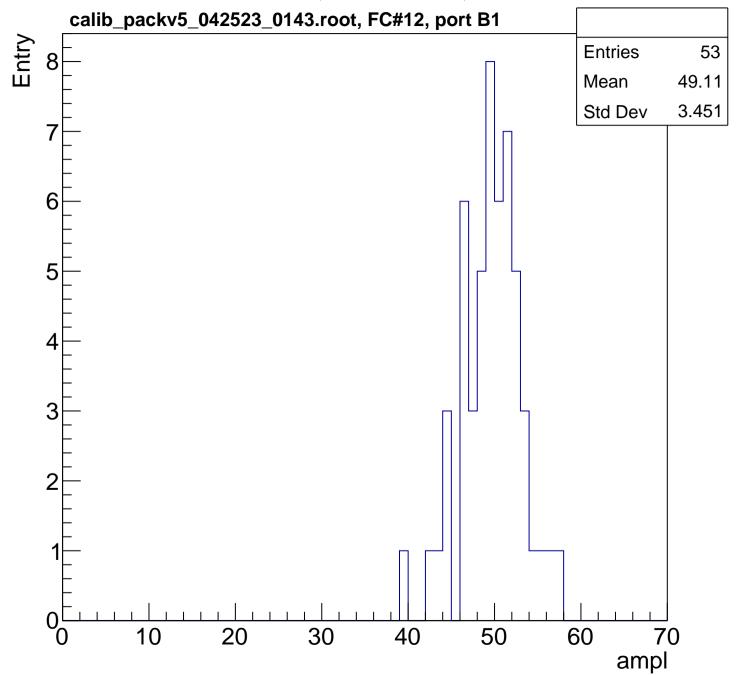
2

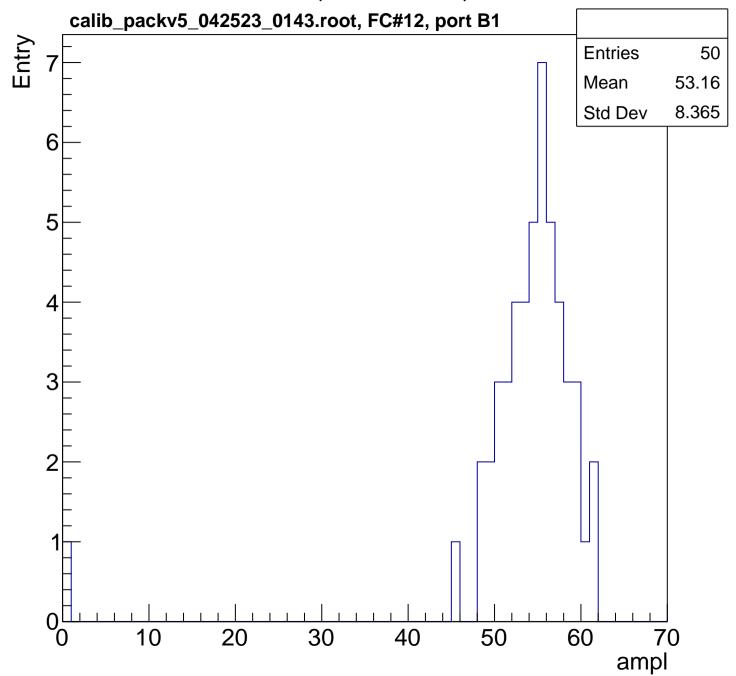


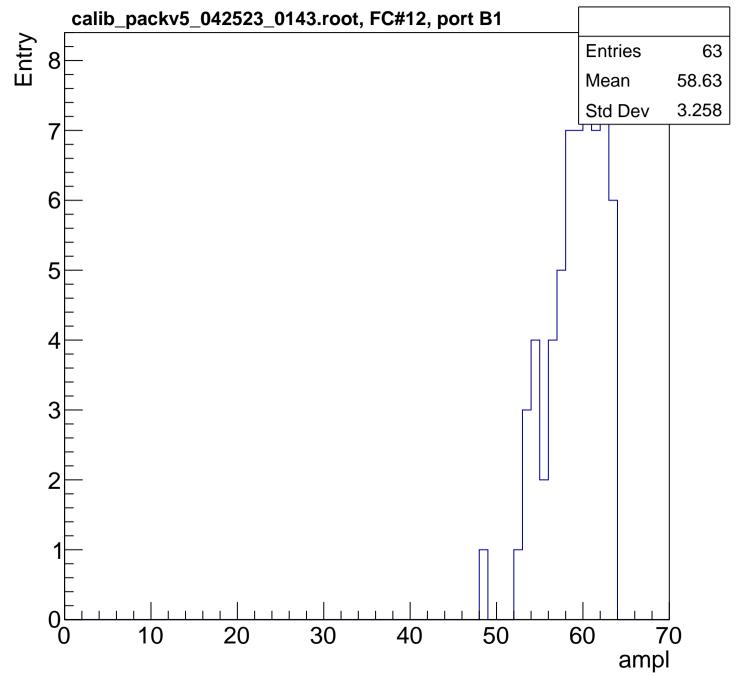


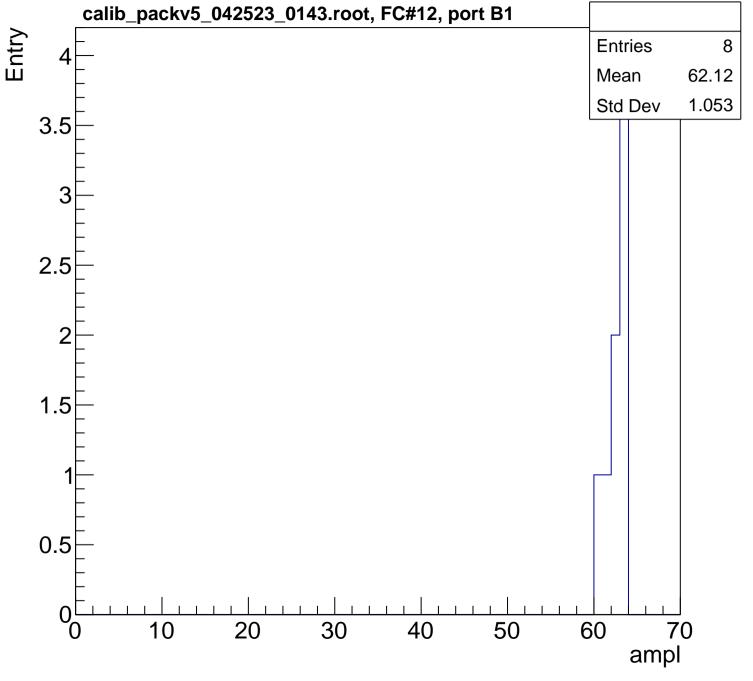




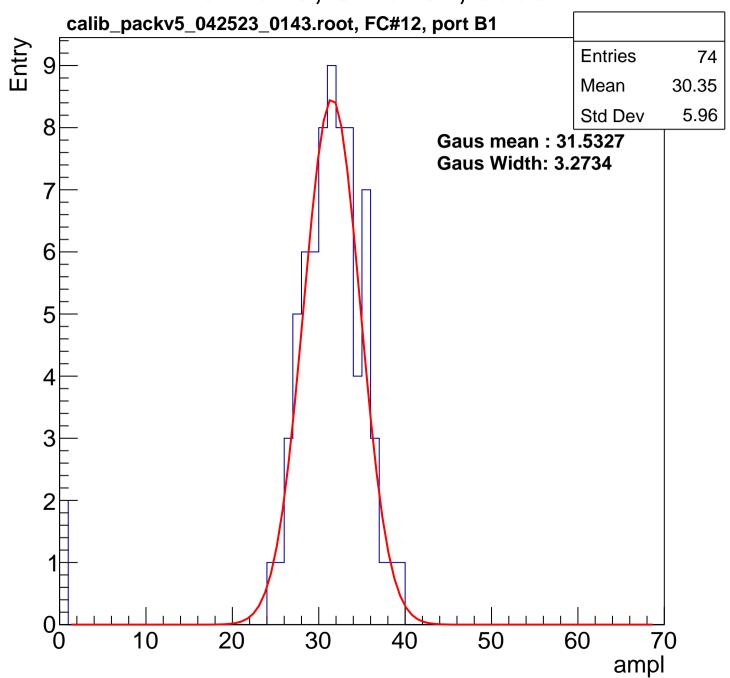


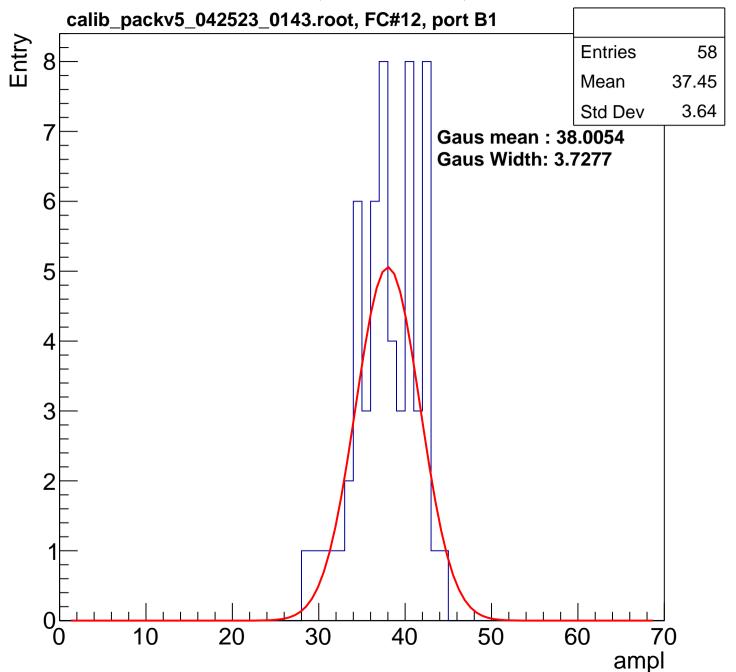


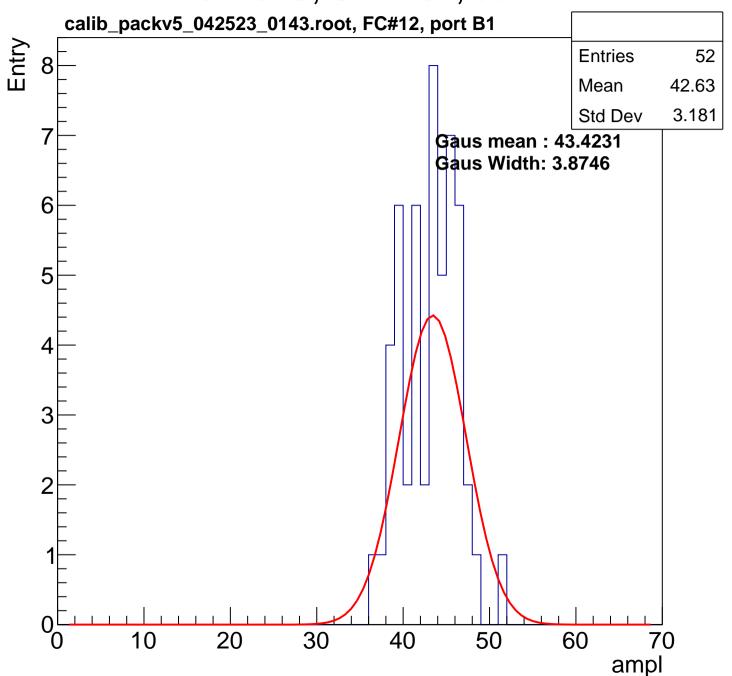


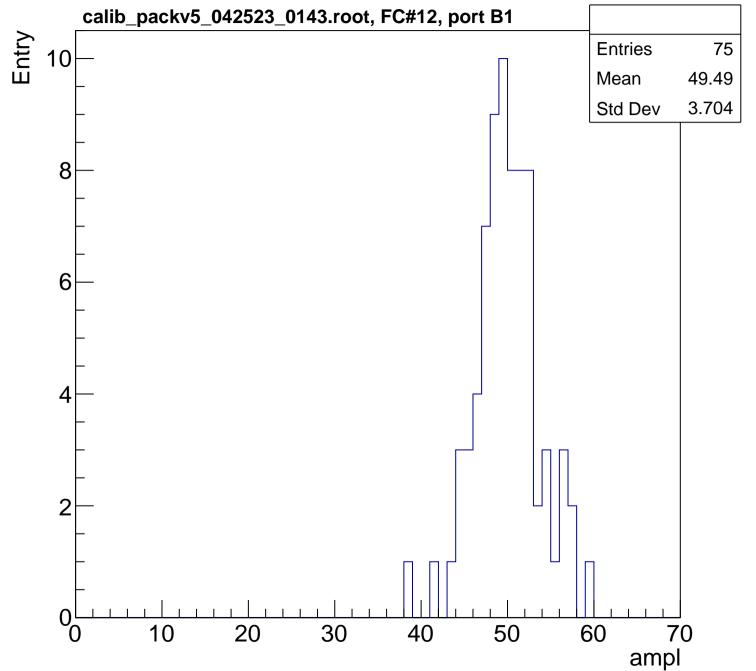


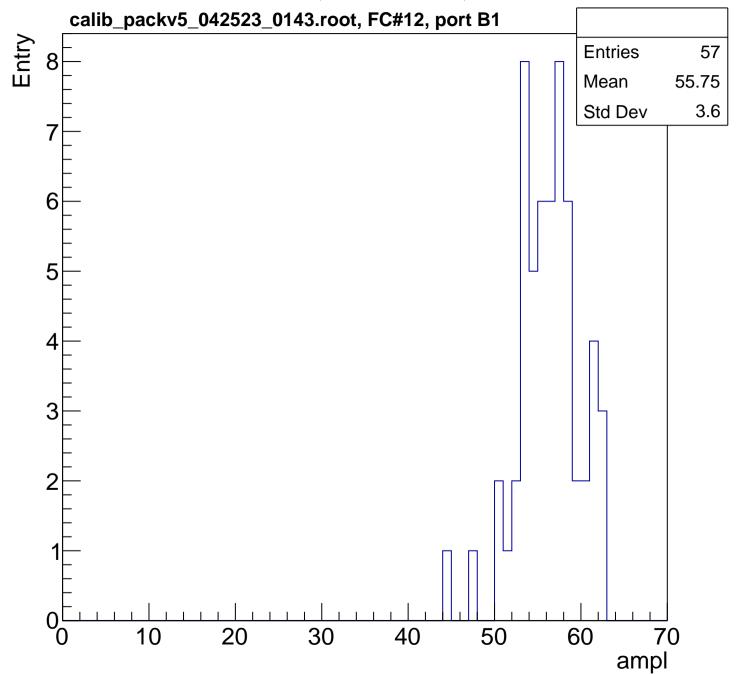


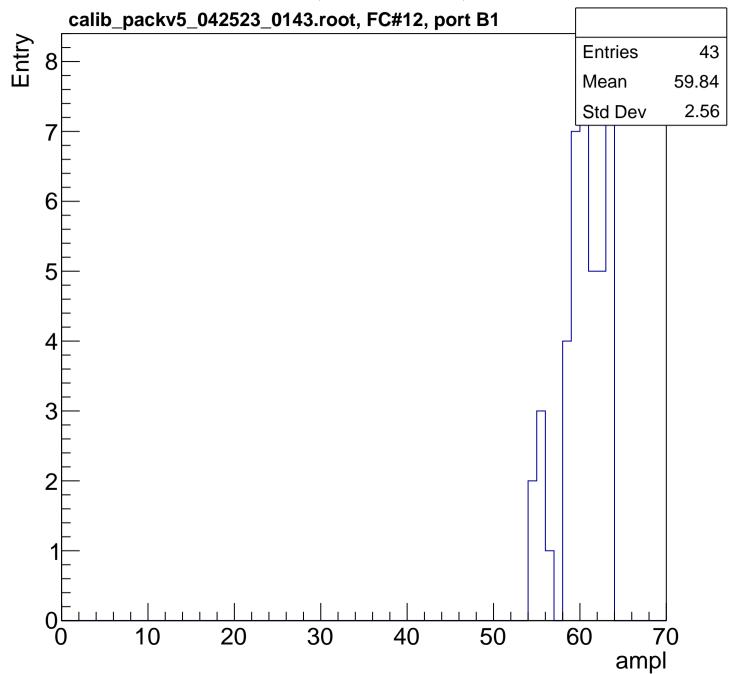


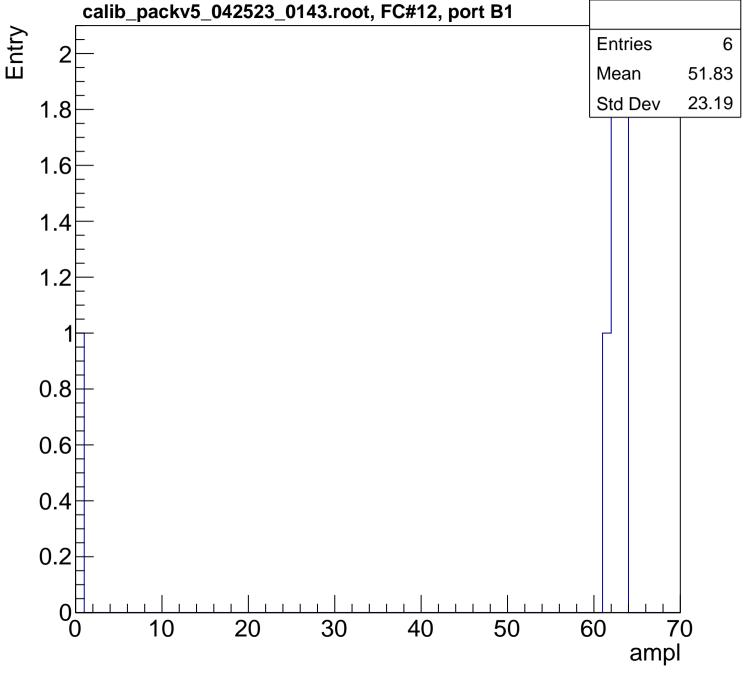




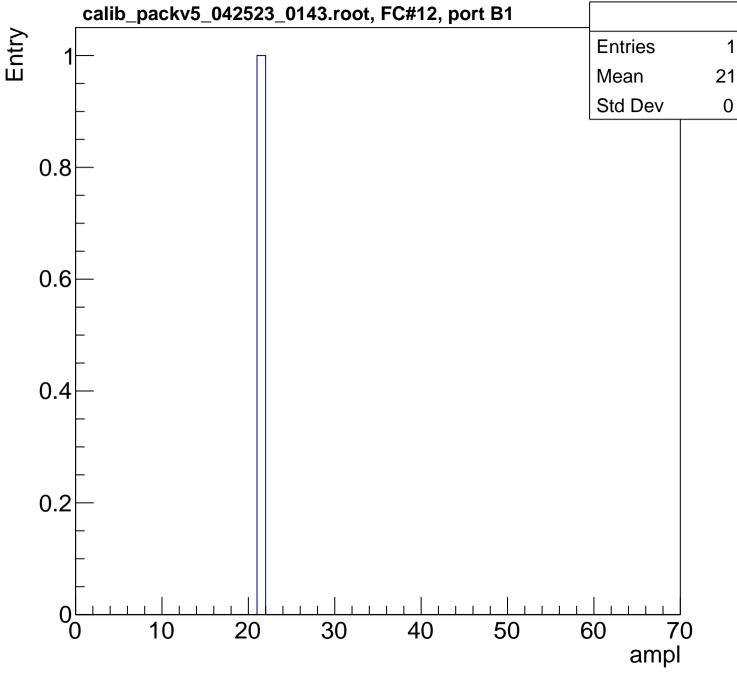


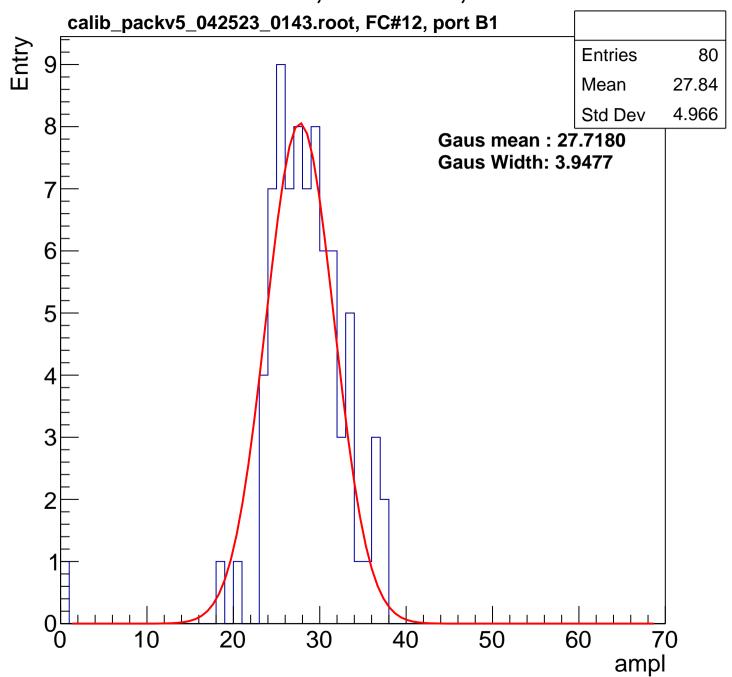


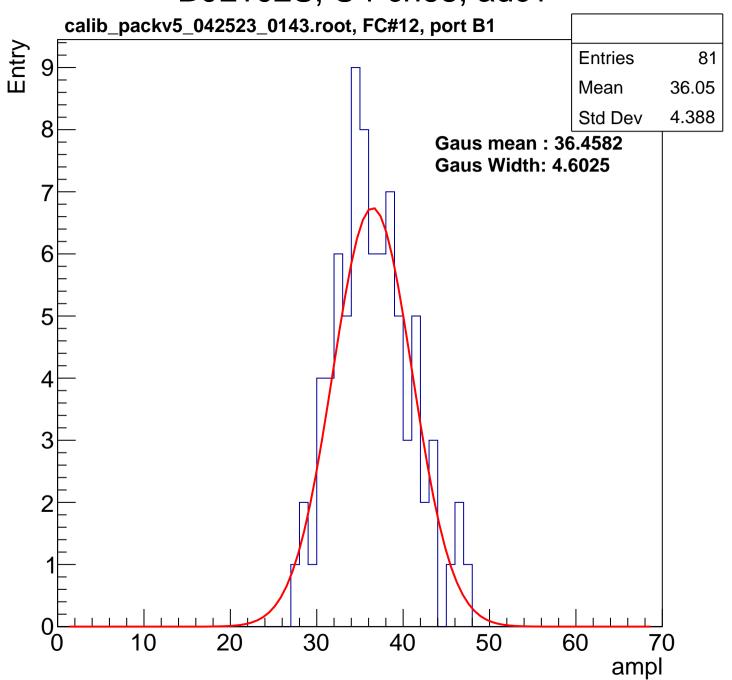


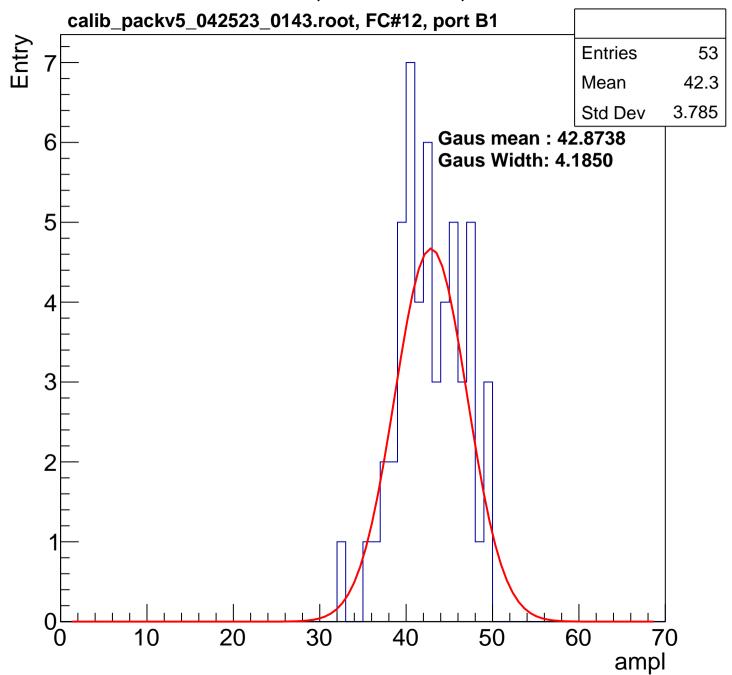


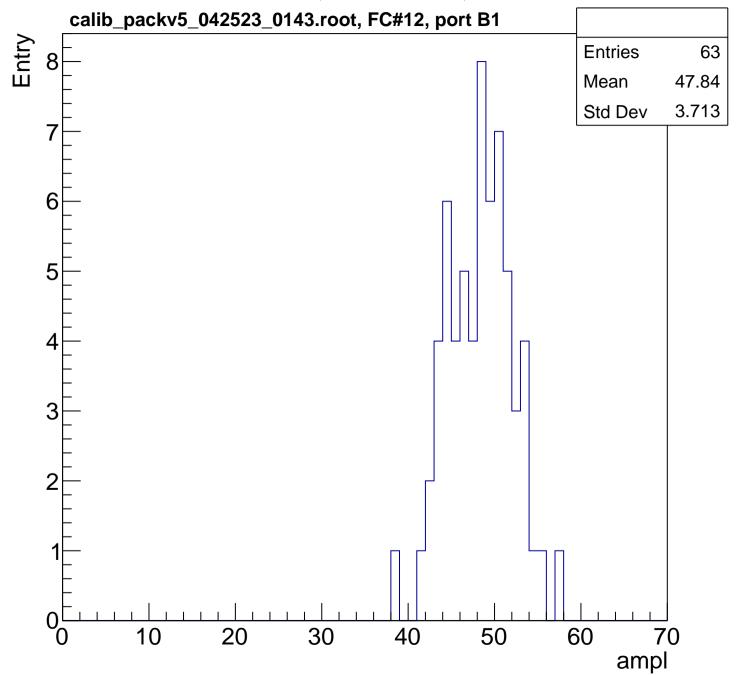
0

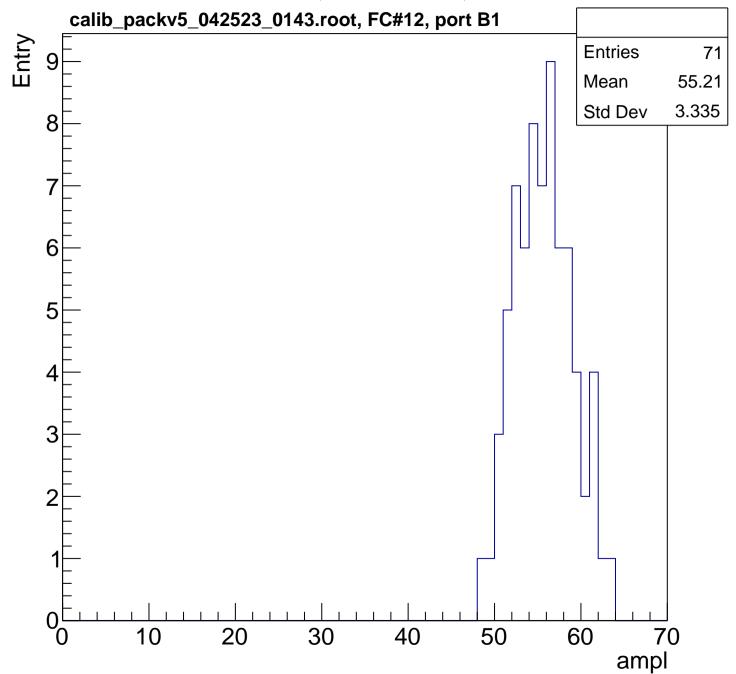


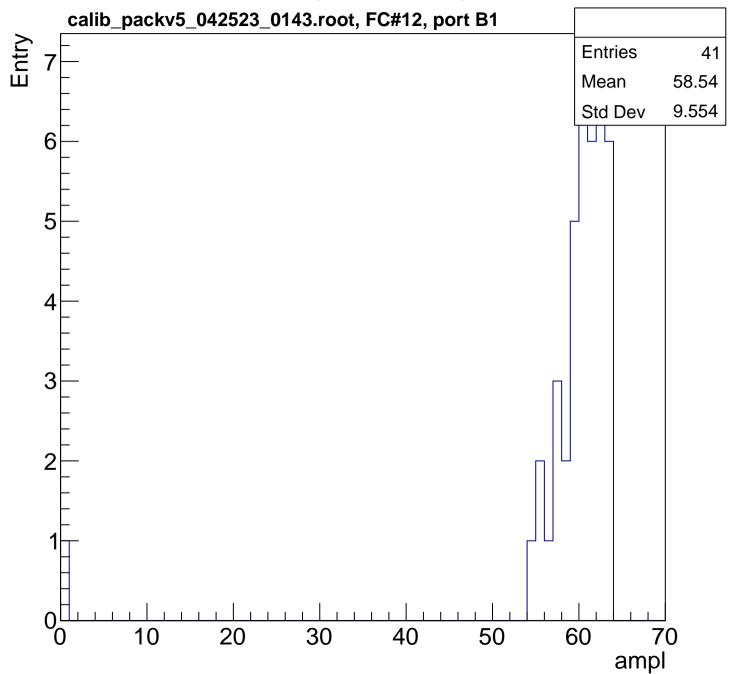


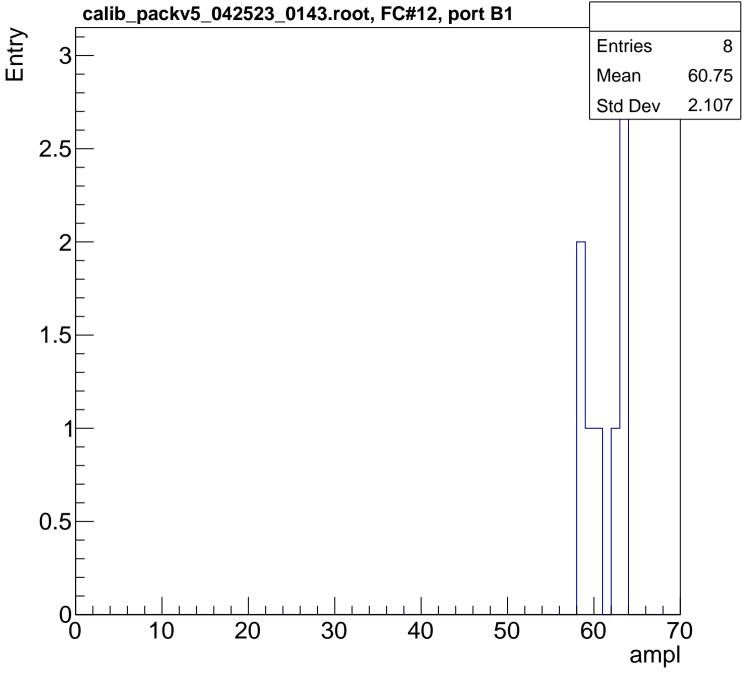


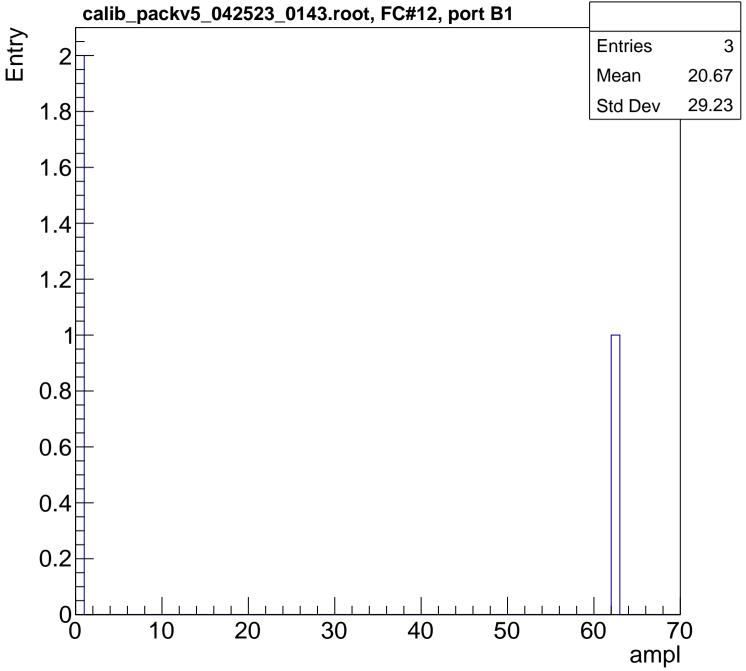


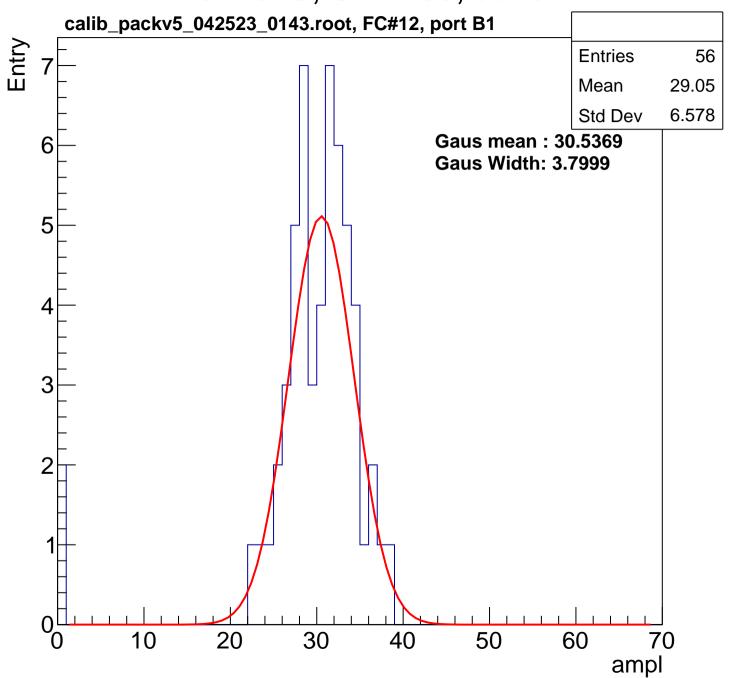


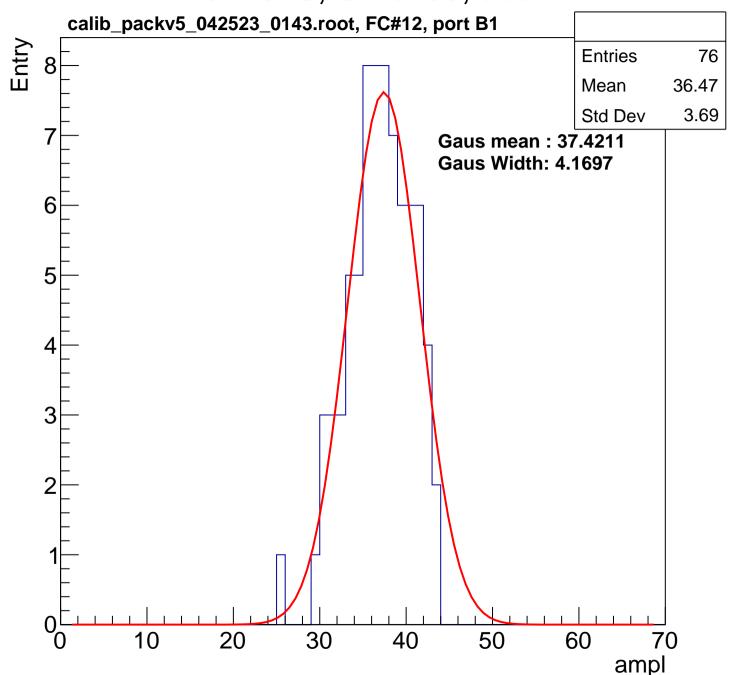


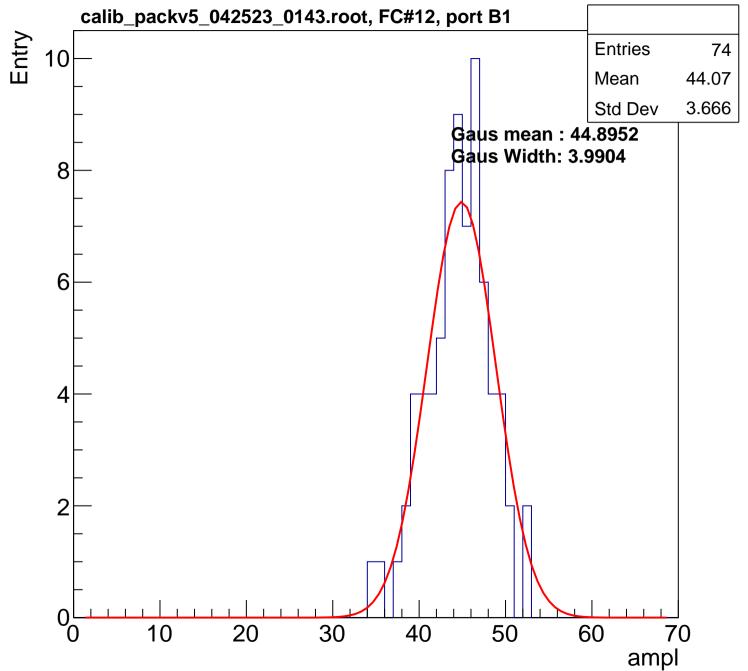


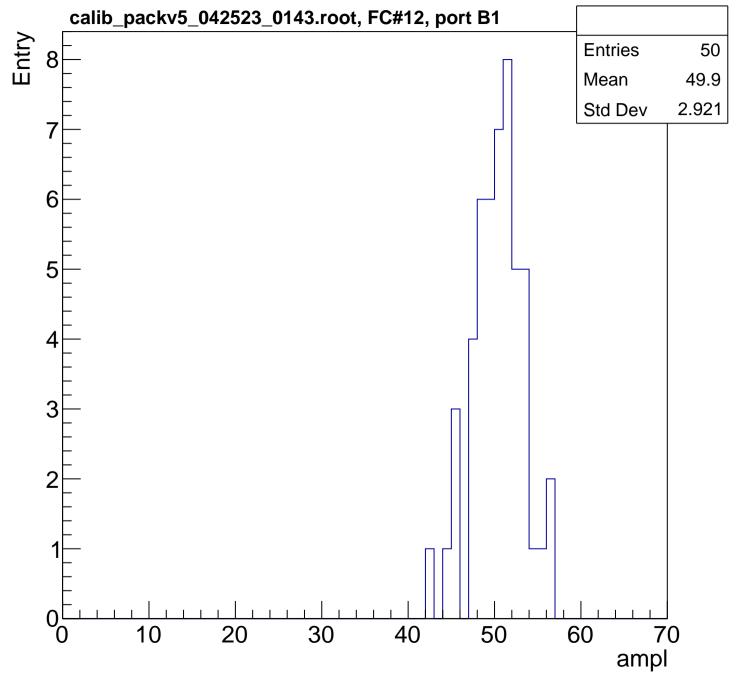


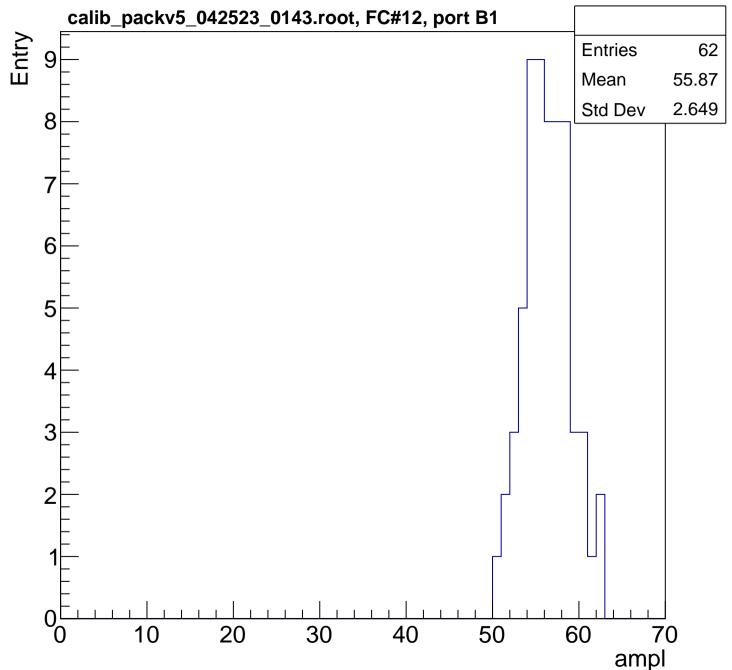


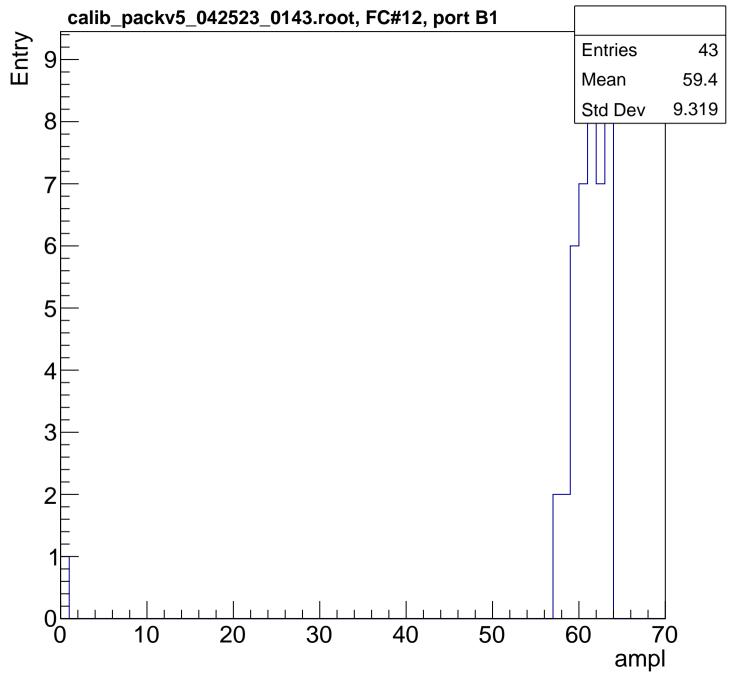


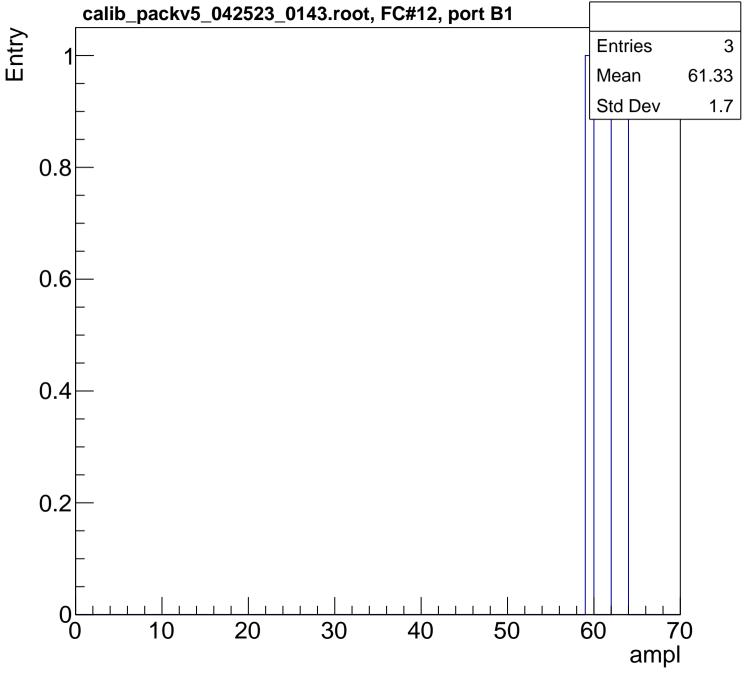




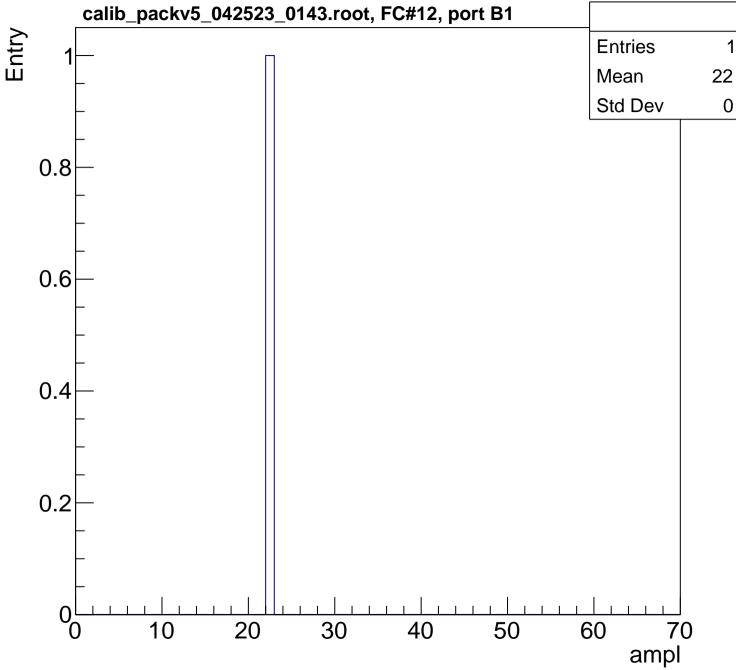


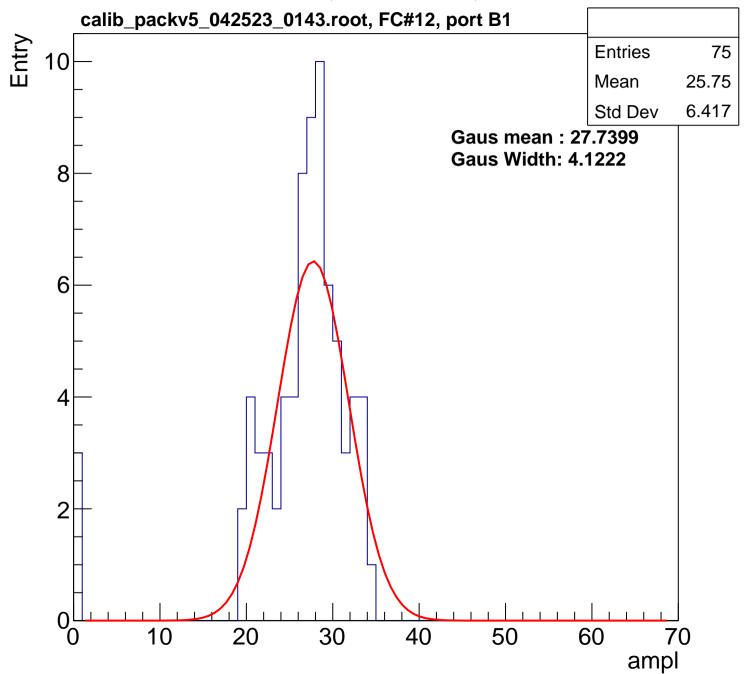


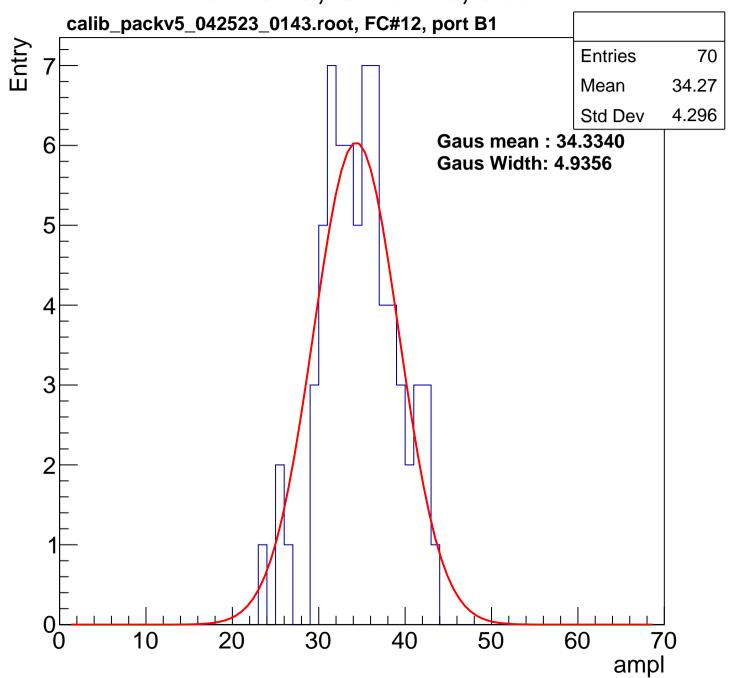


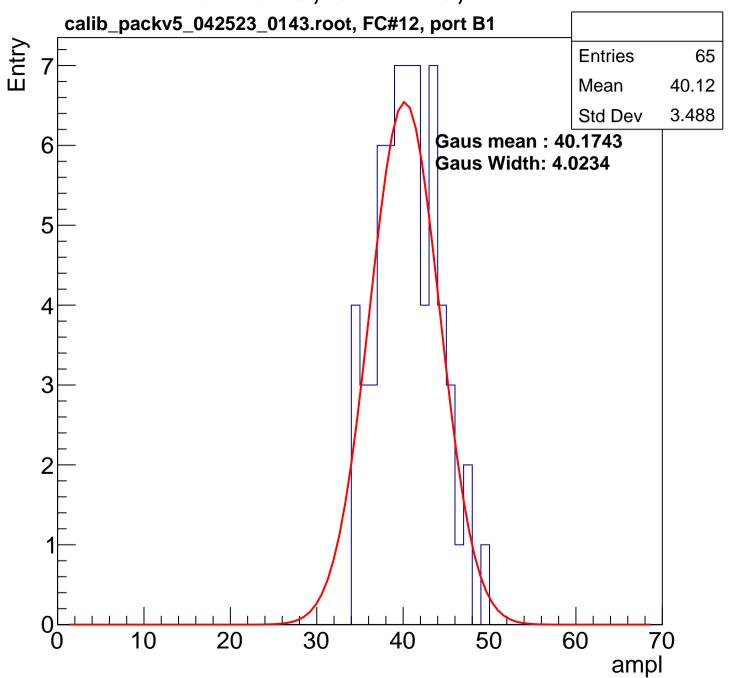


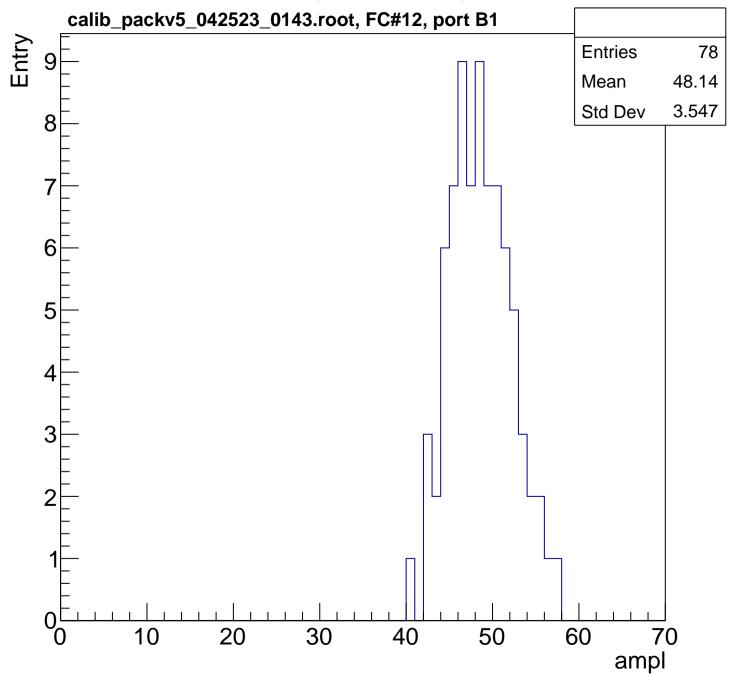
0

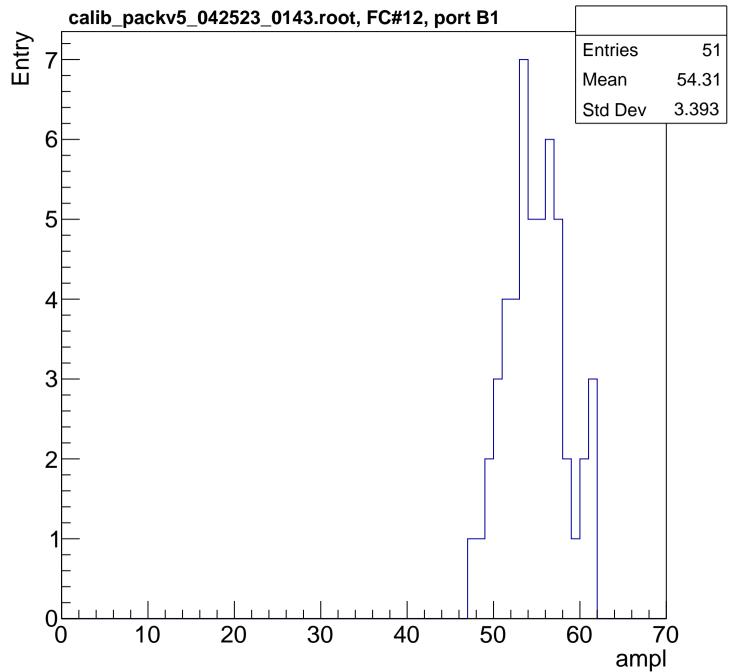


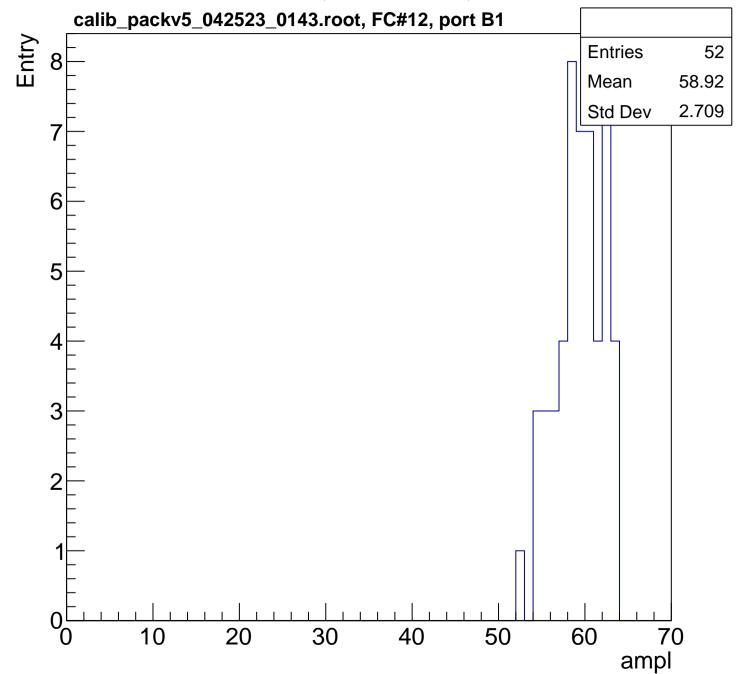


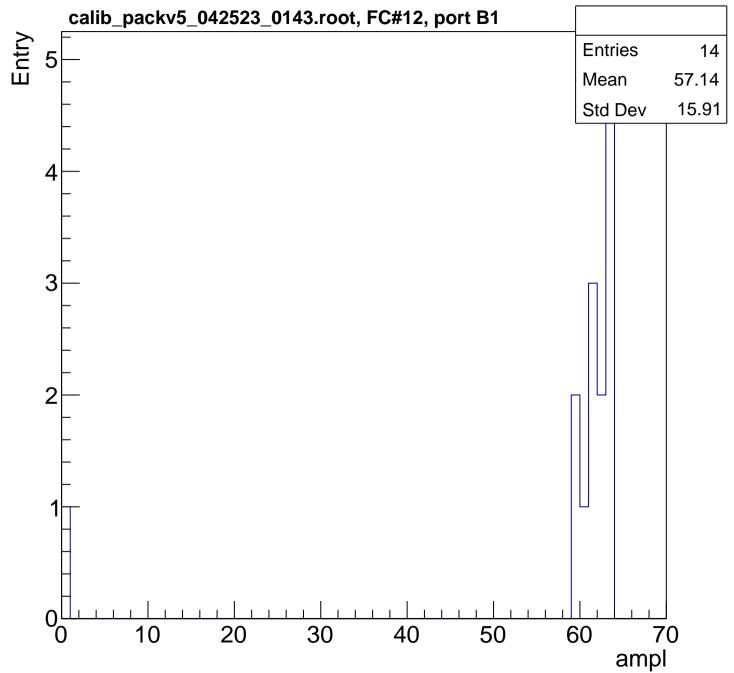


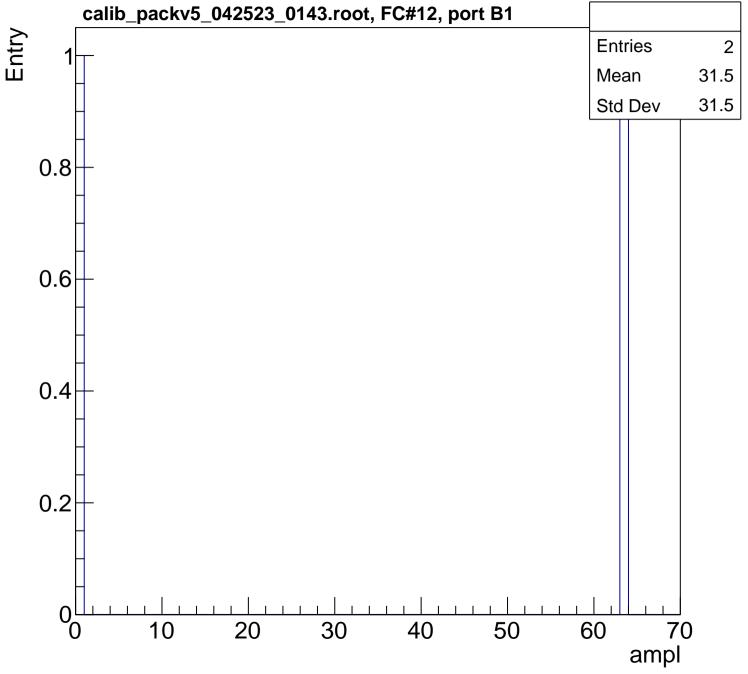


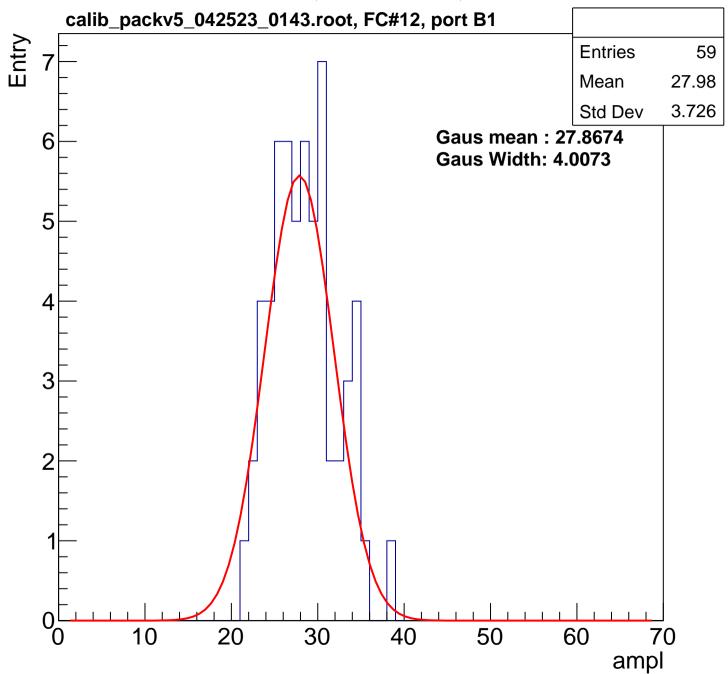


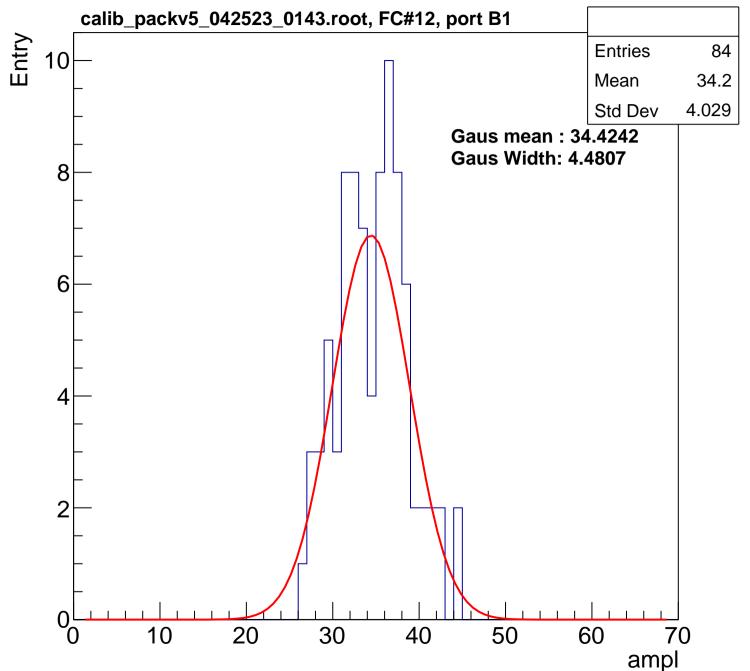


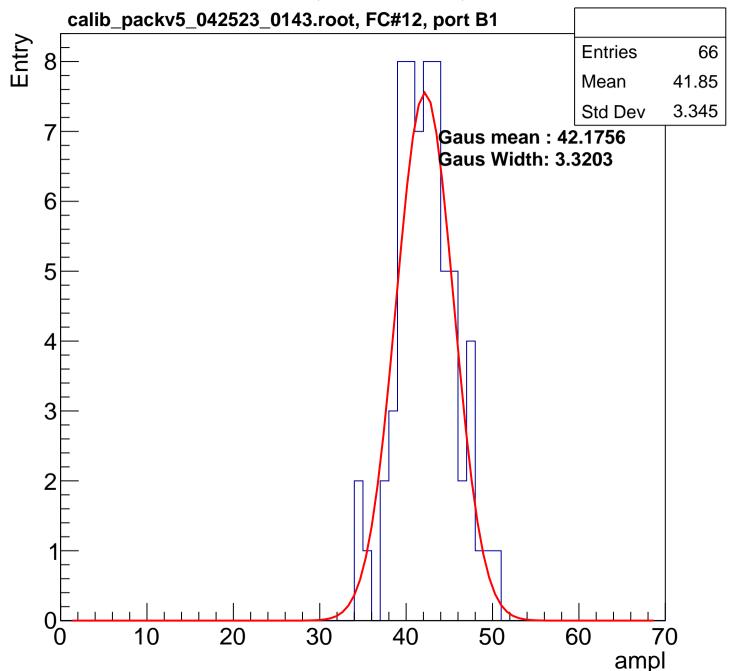


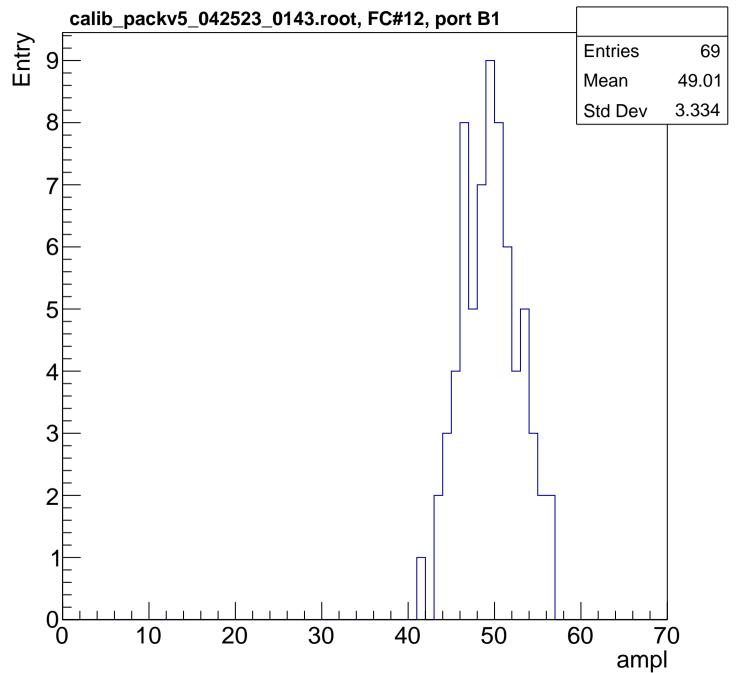


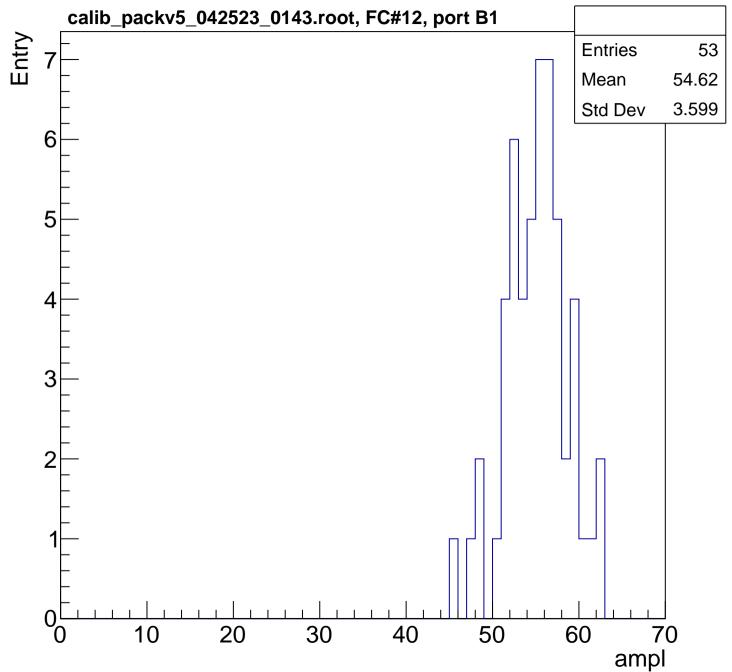


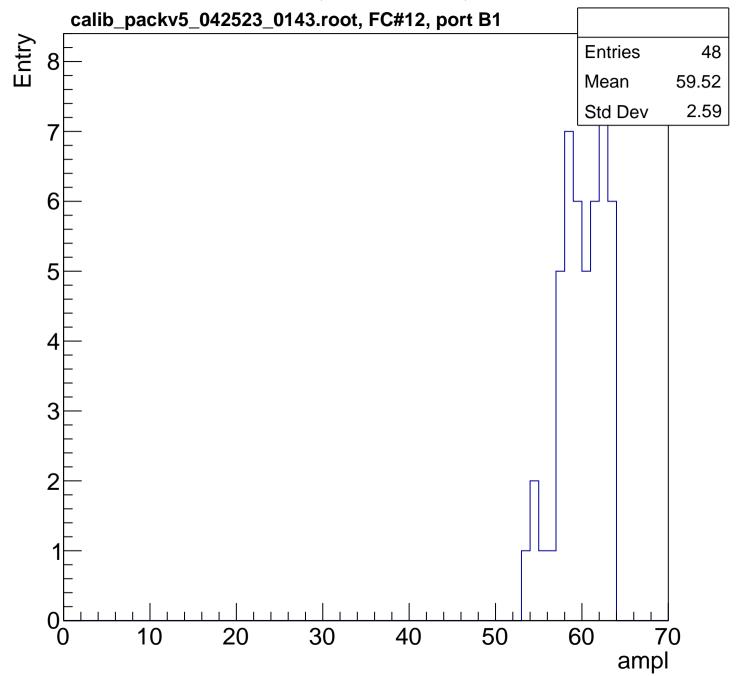


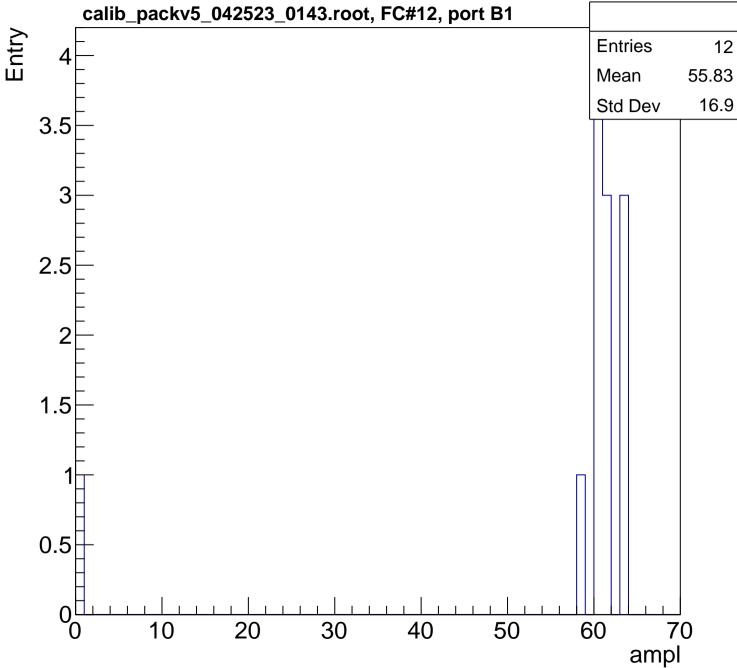


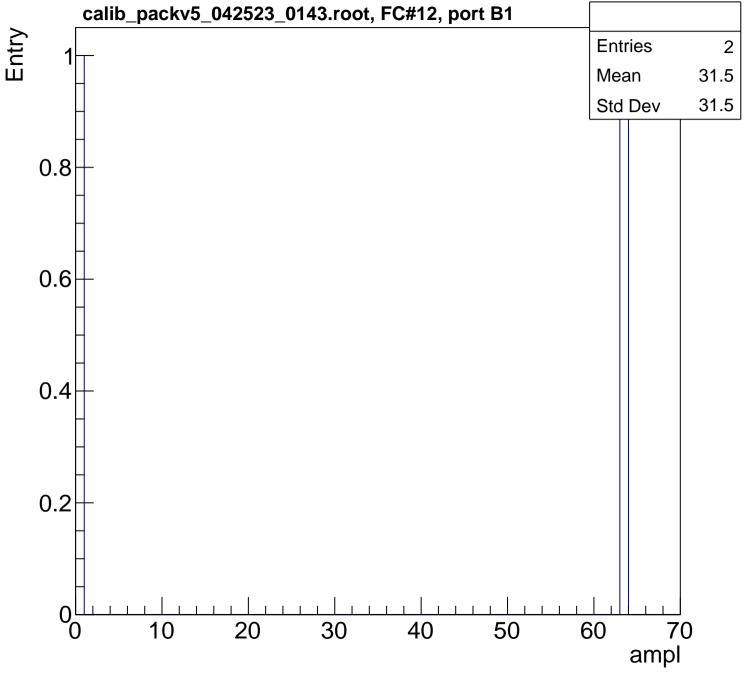


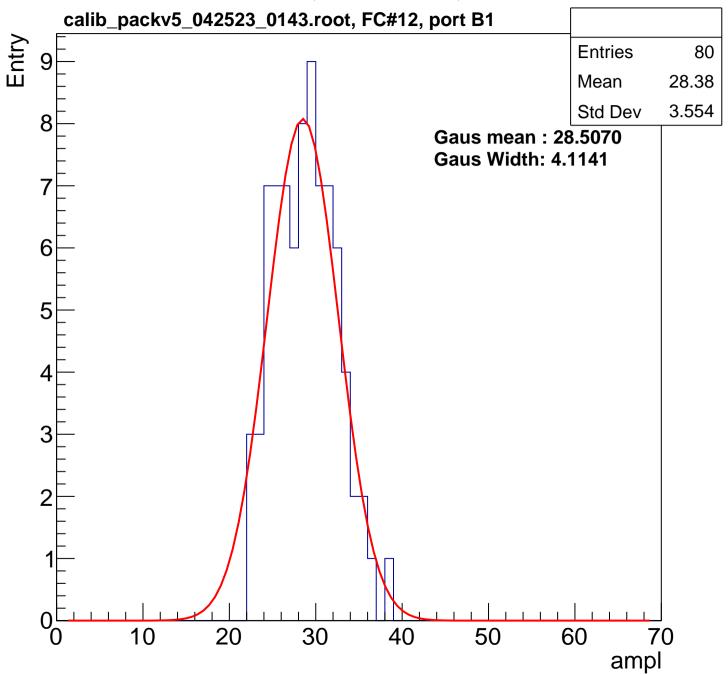


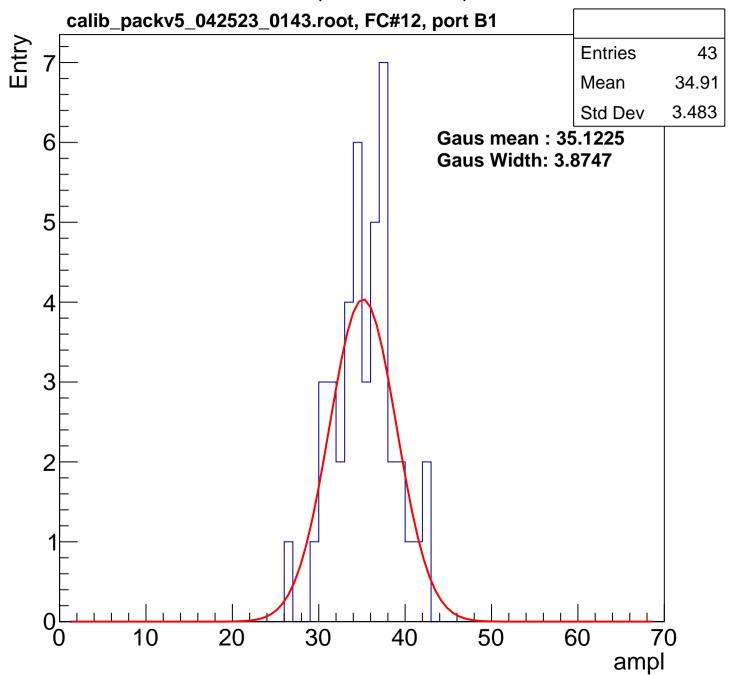


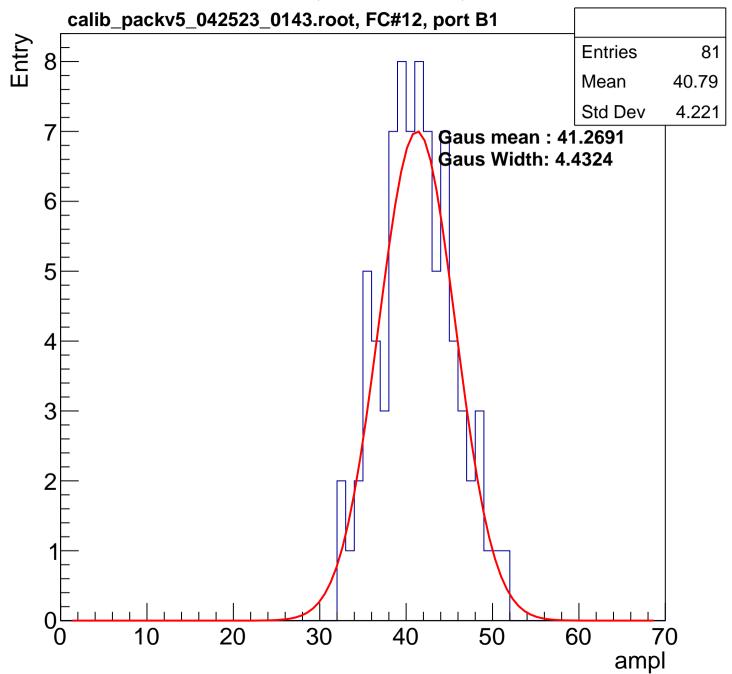


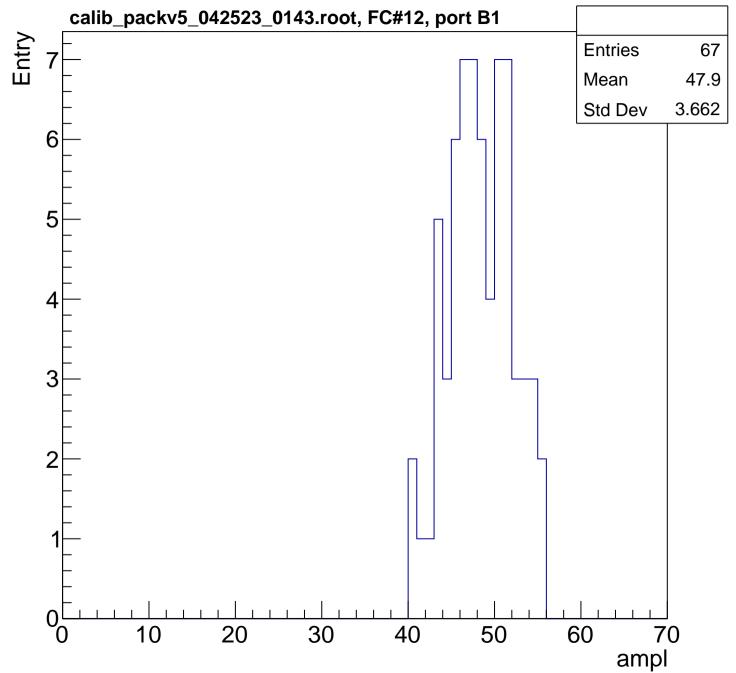


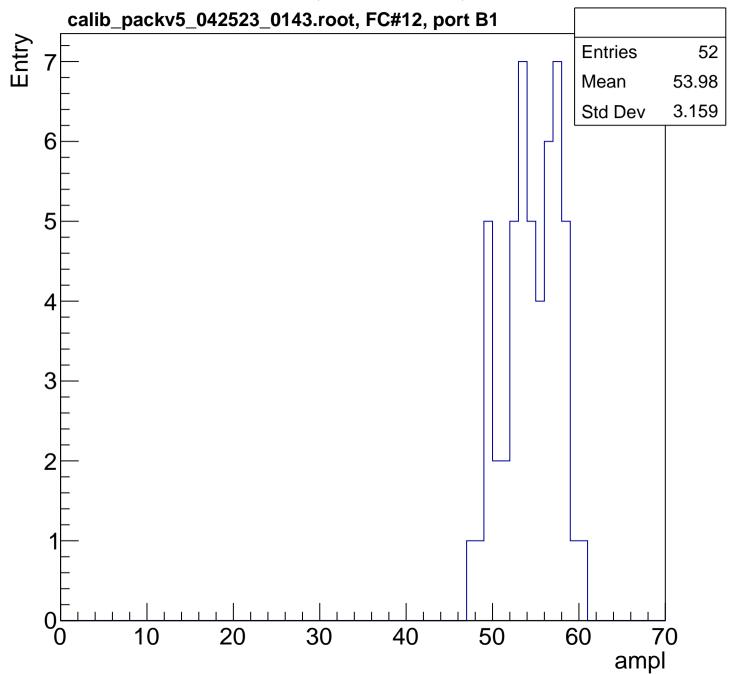


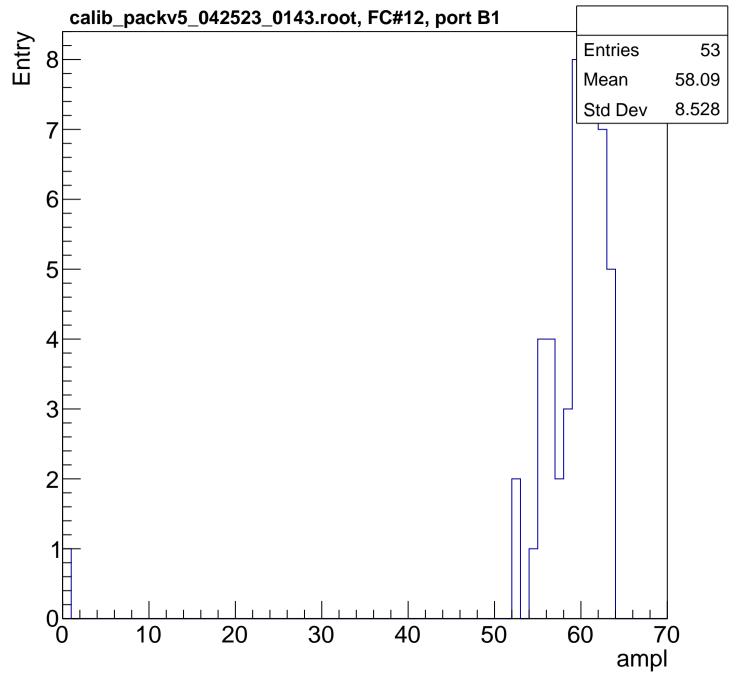


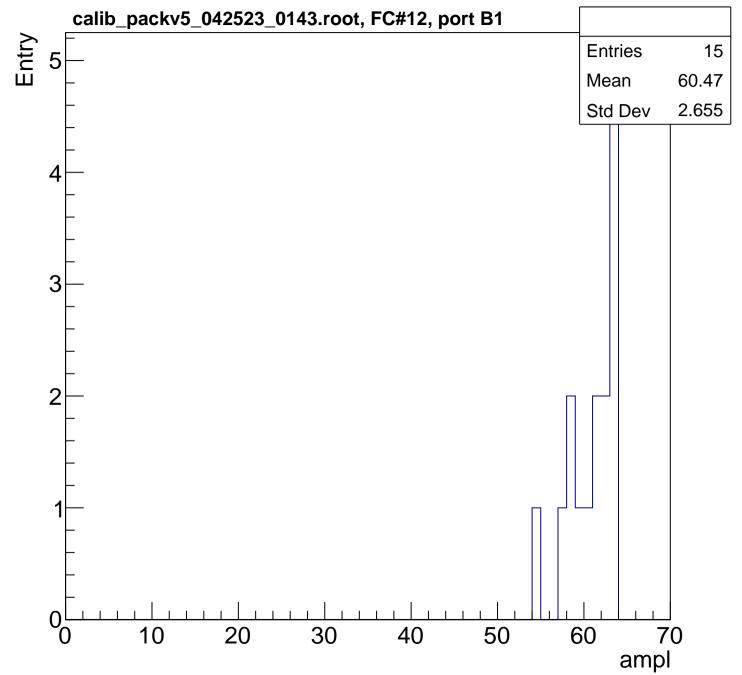


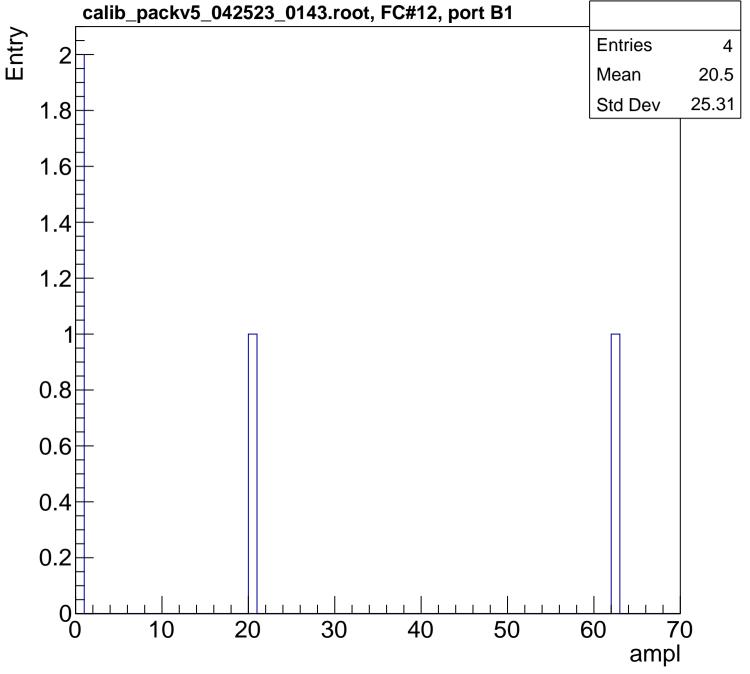


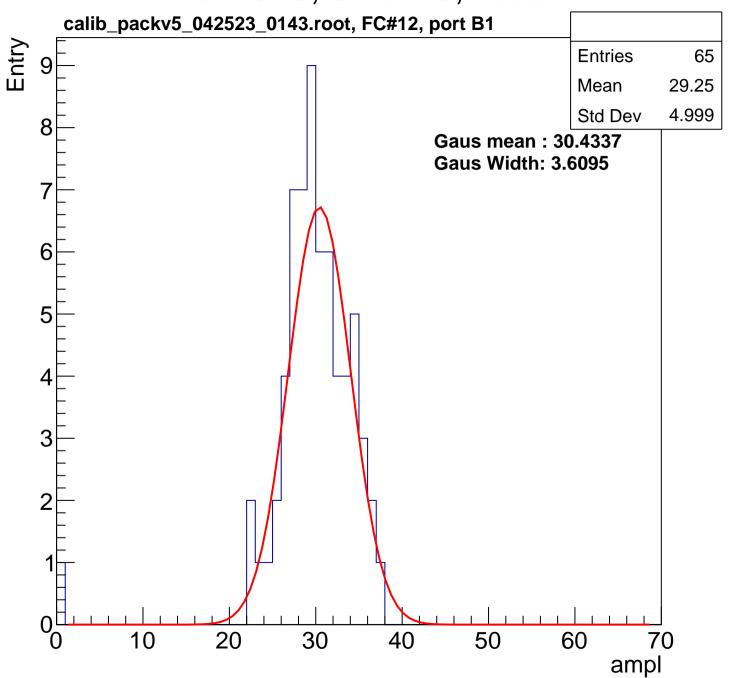


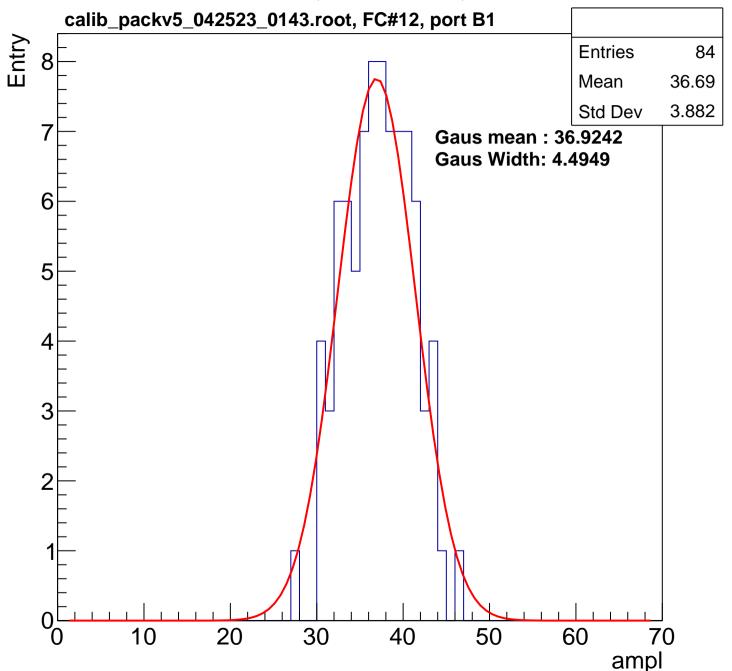


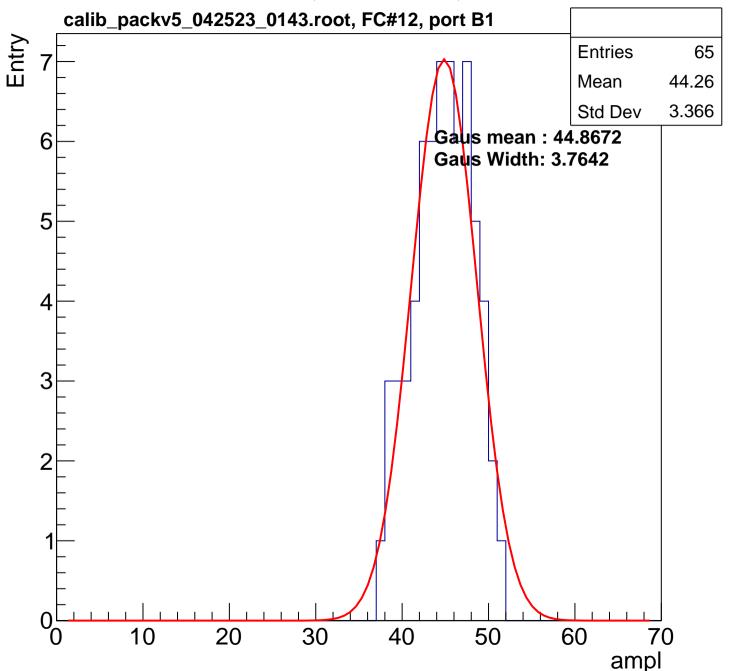


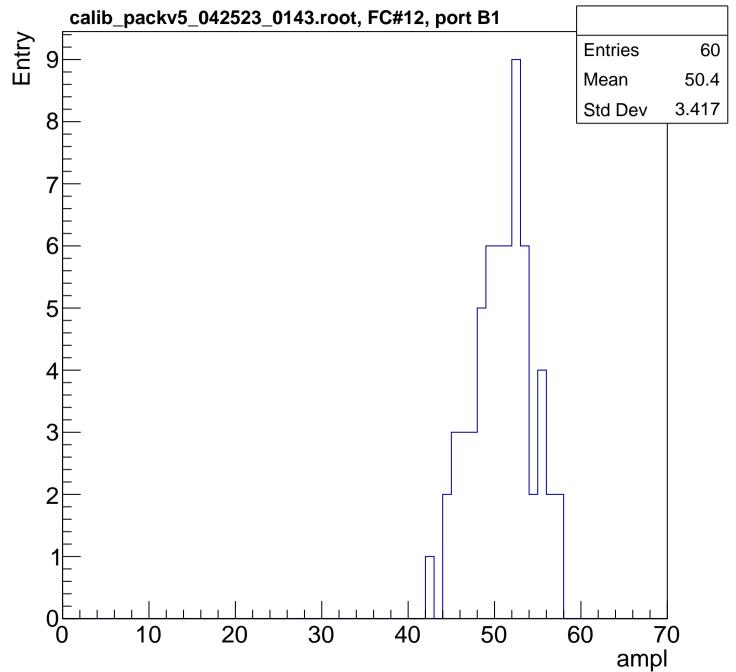


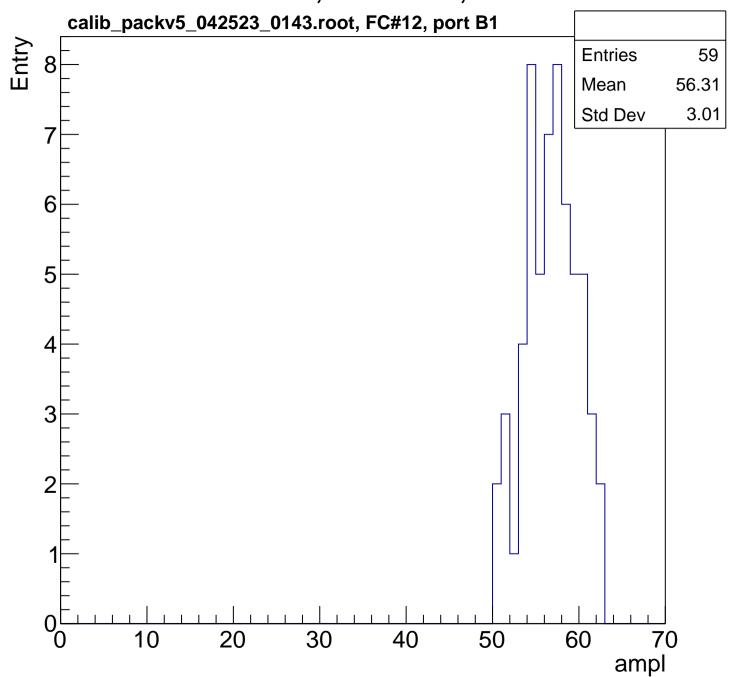


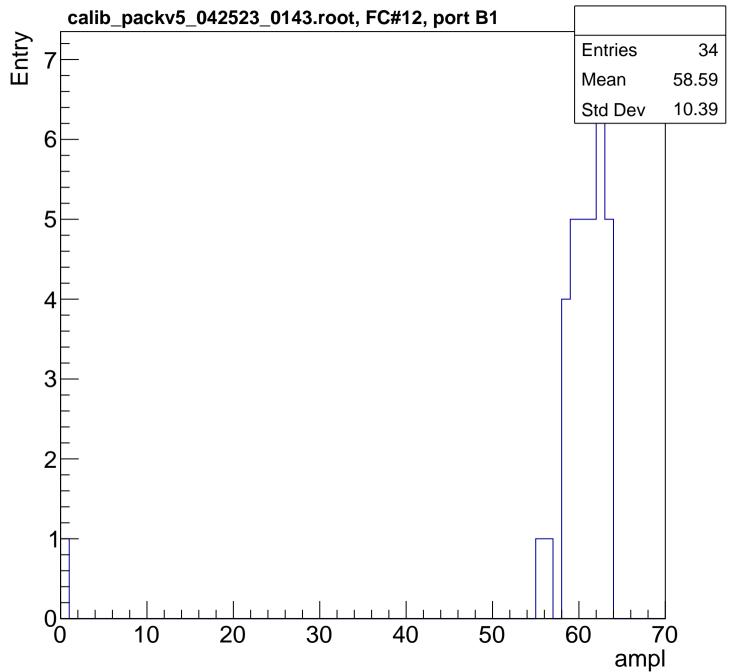


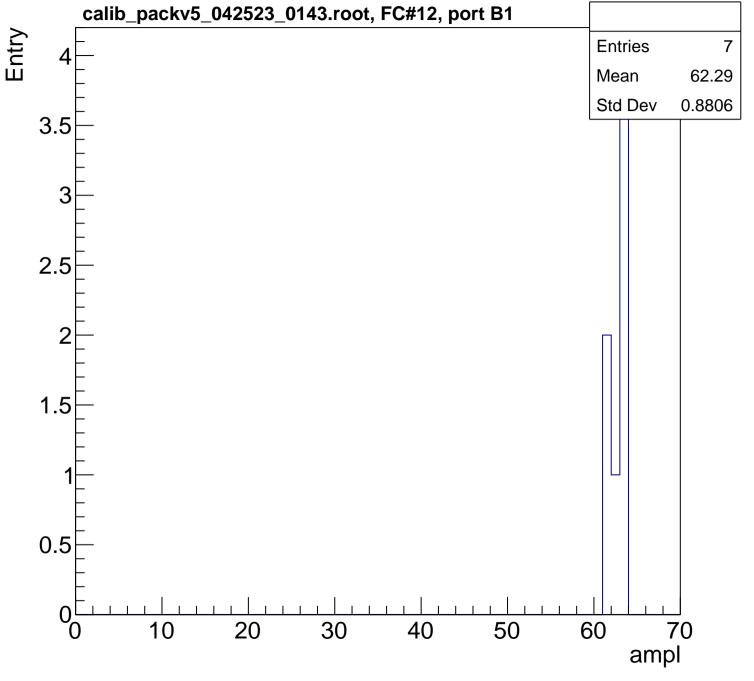


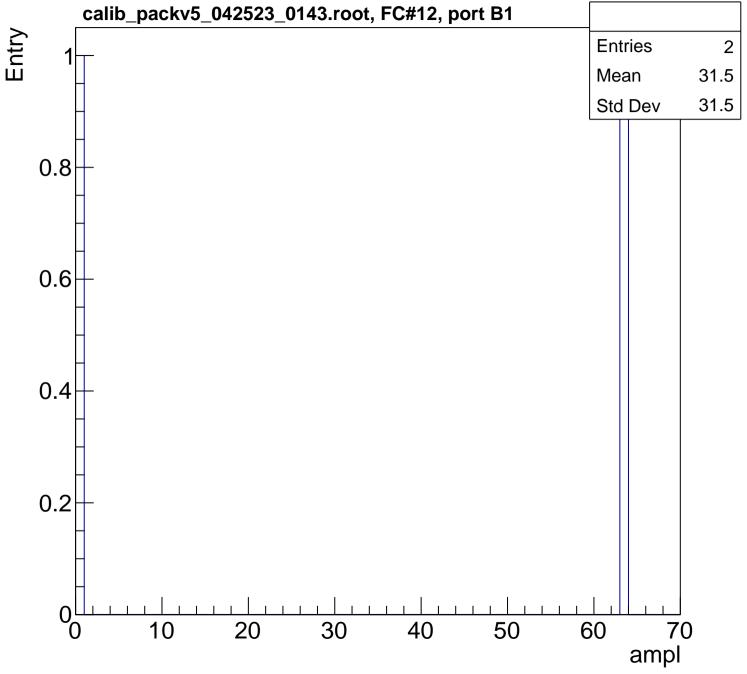


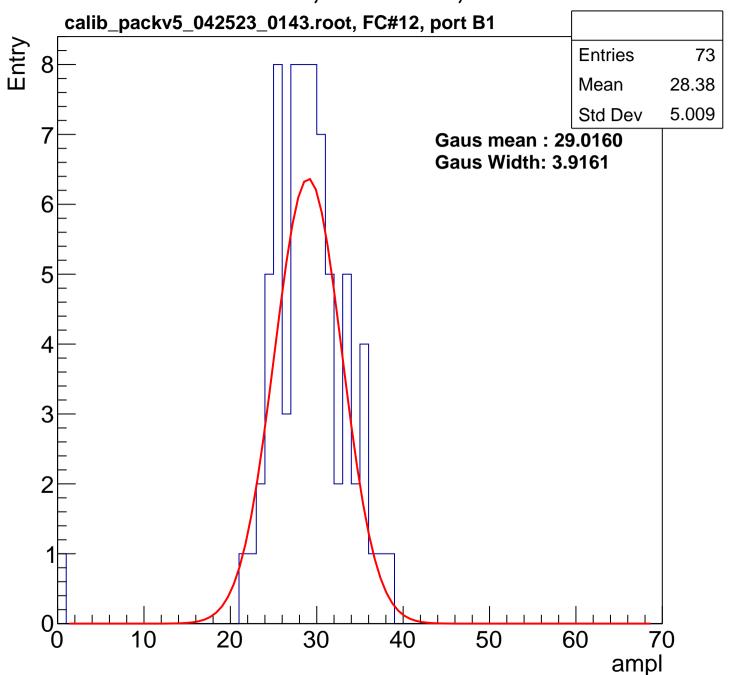


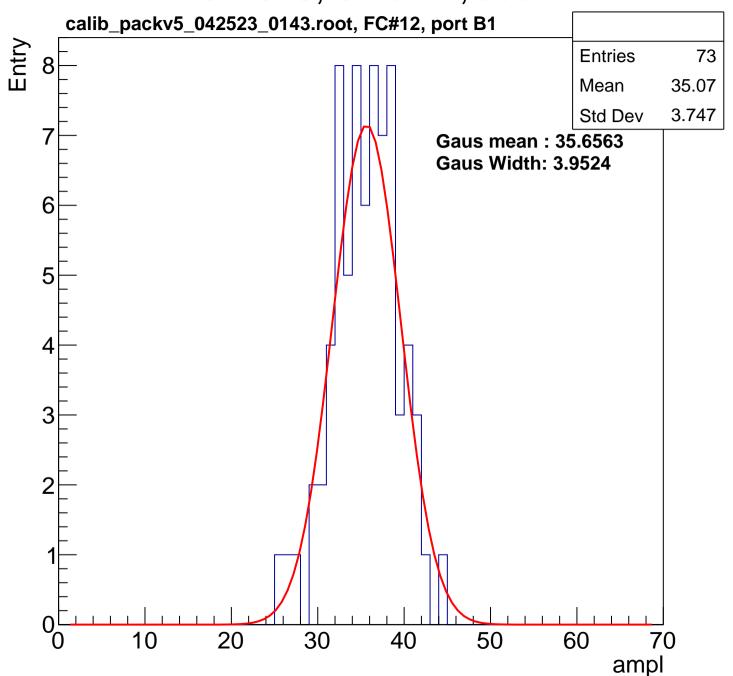


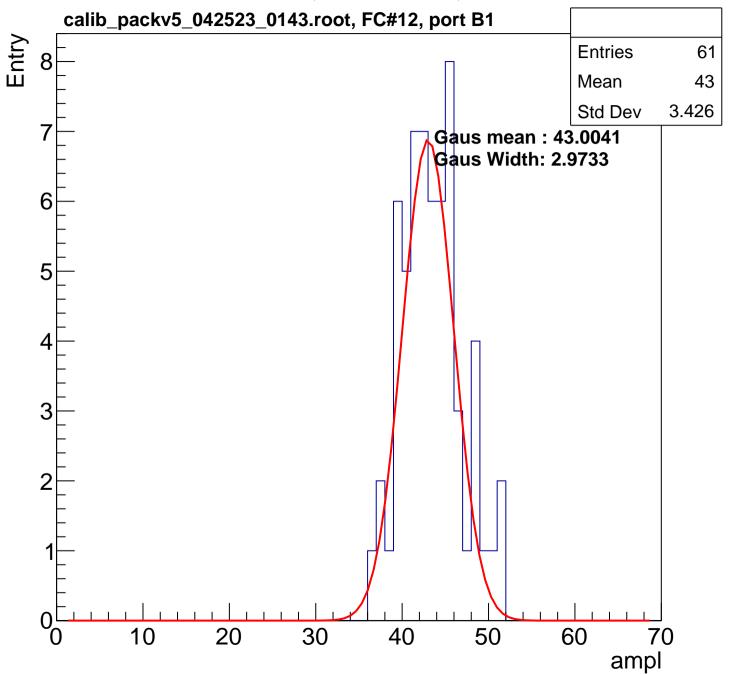


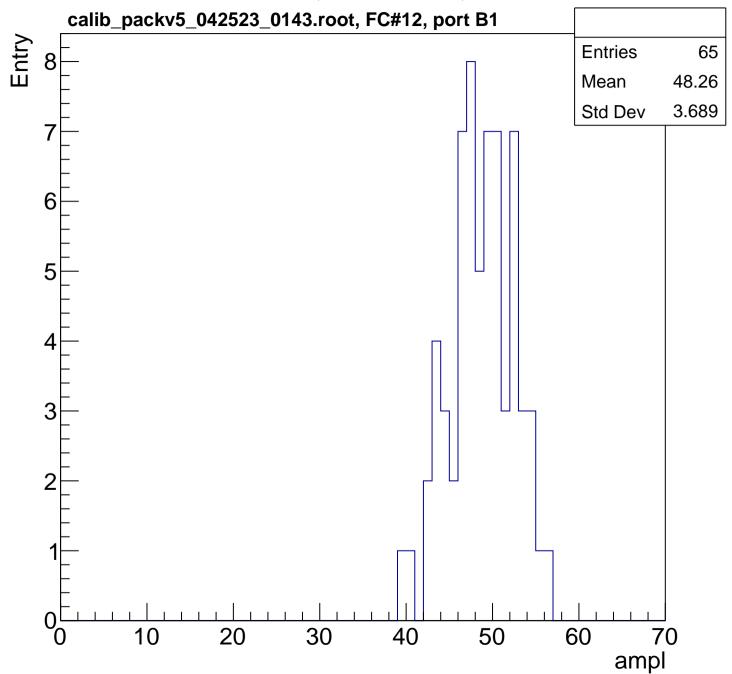


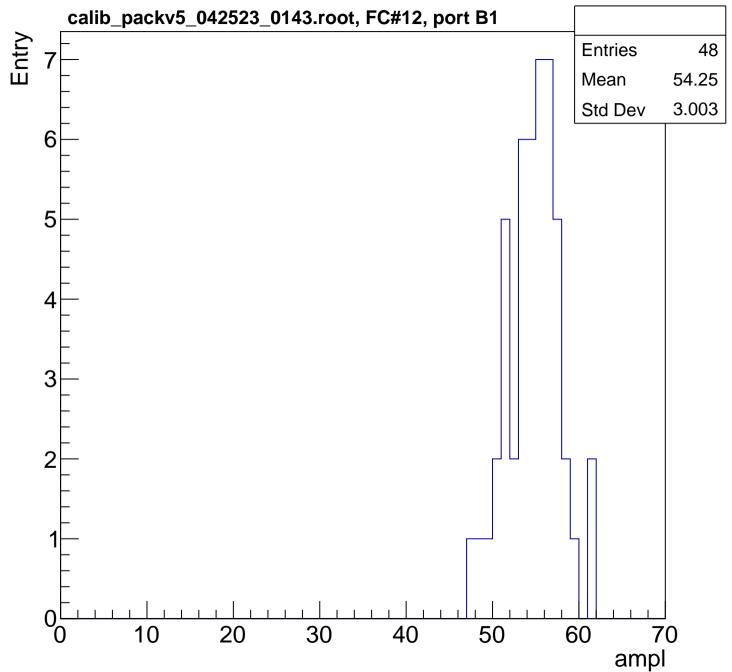


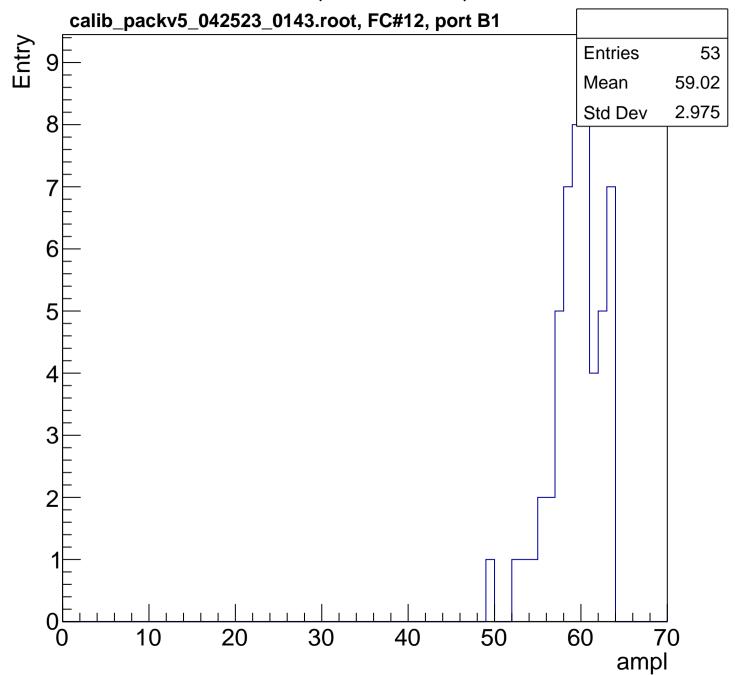


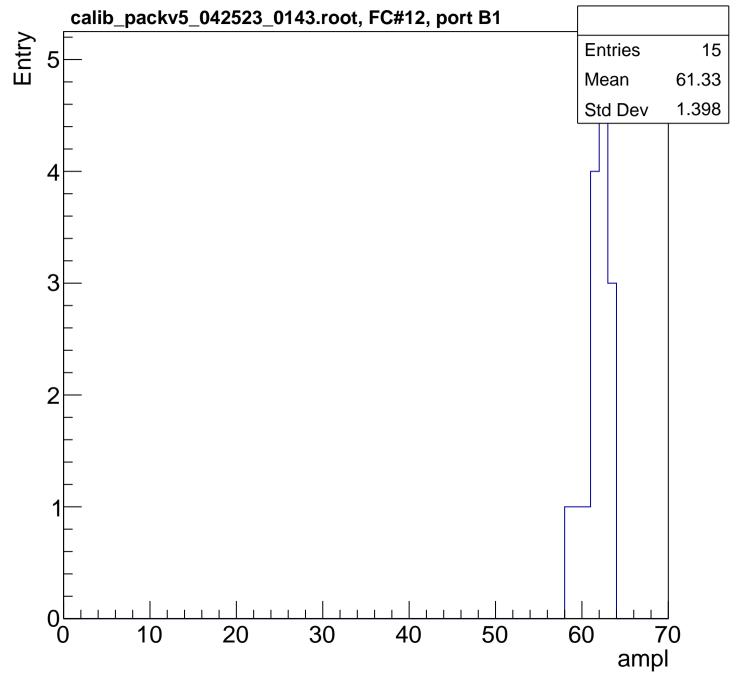




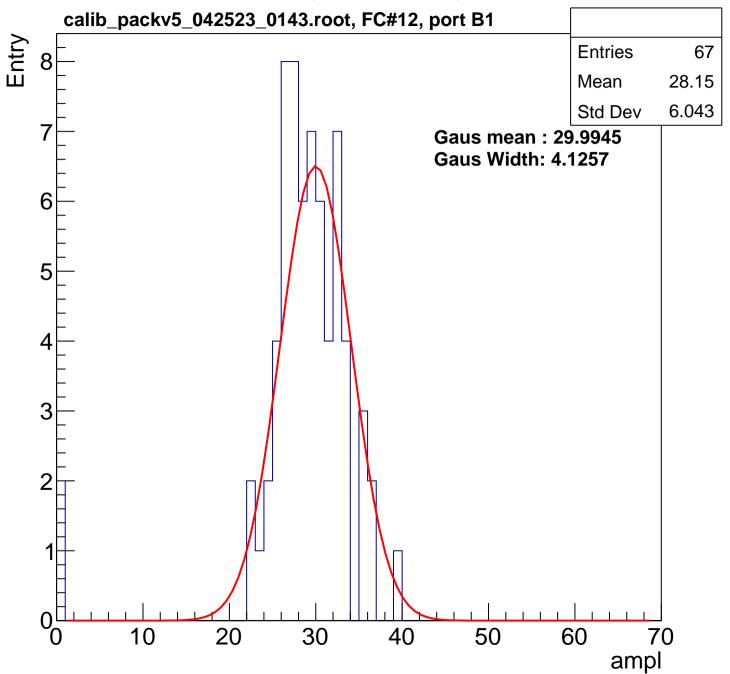


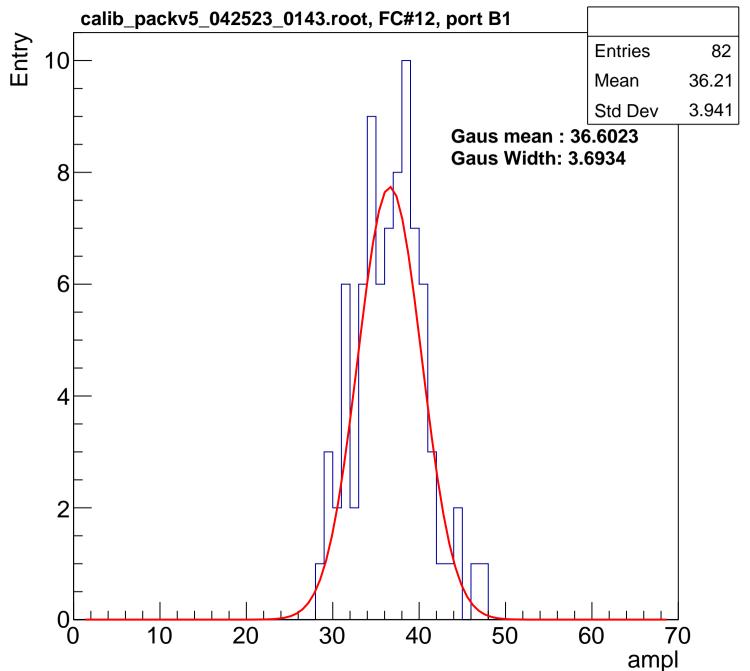


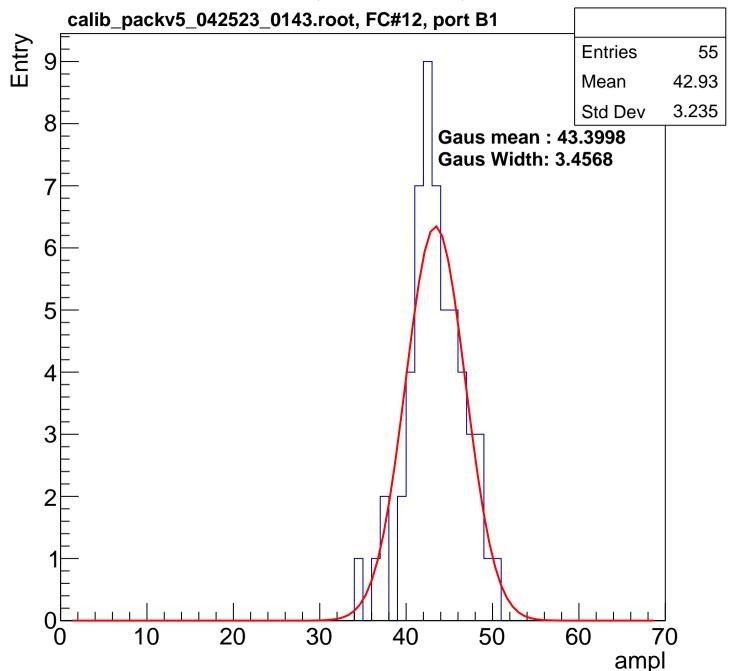


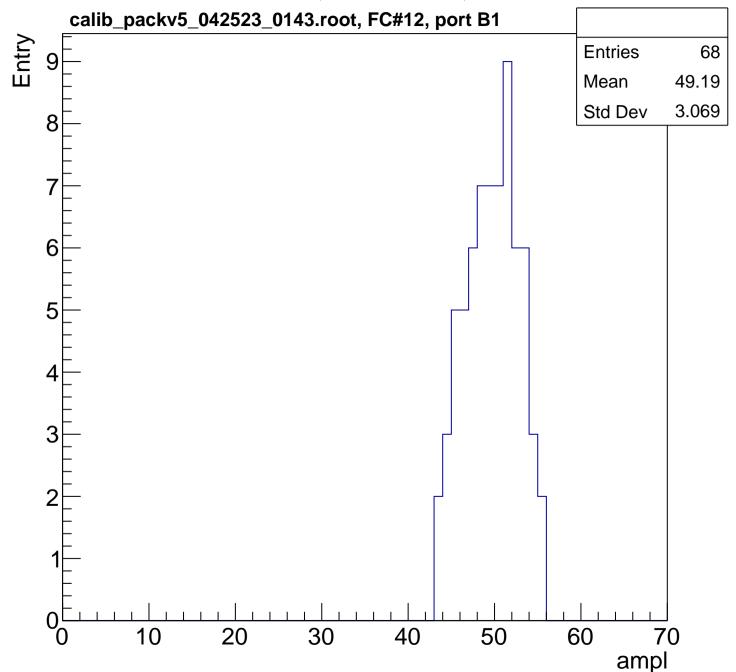


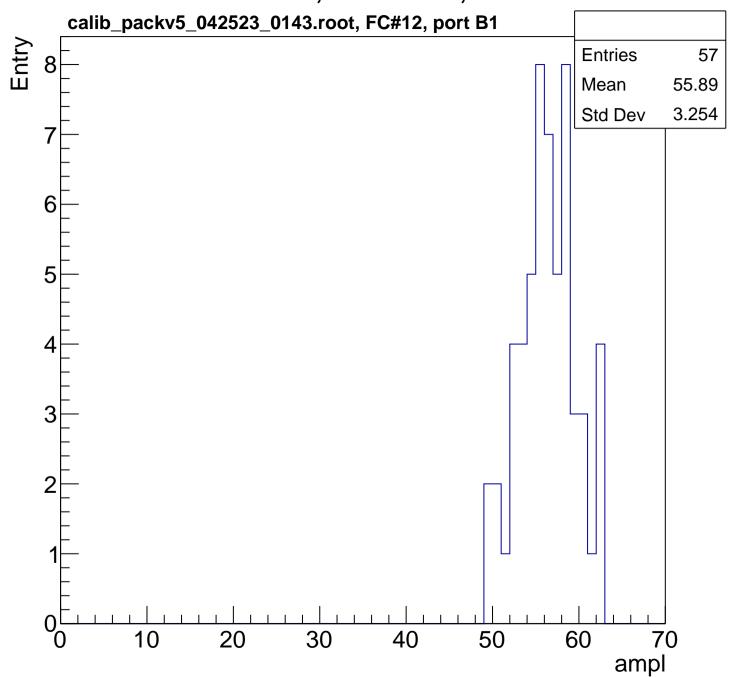
B0L102S, U4-ch74, adc7 calib_packv5_042523_0143.root, FC#12, port B1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

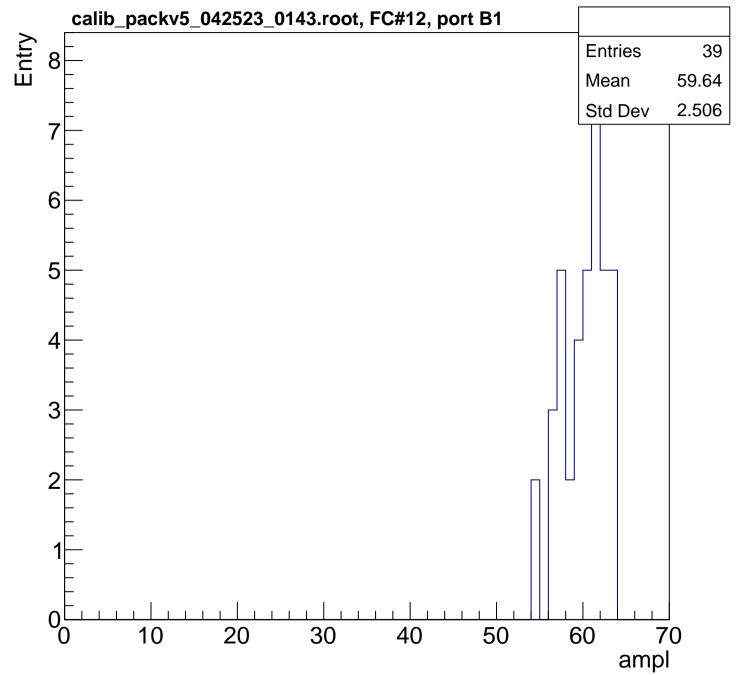


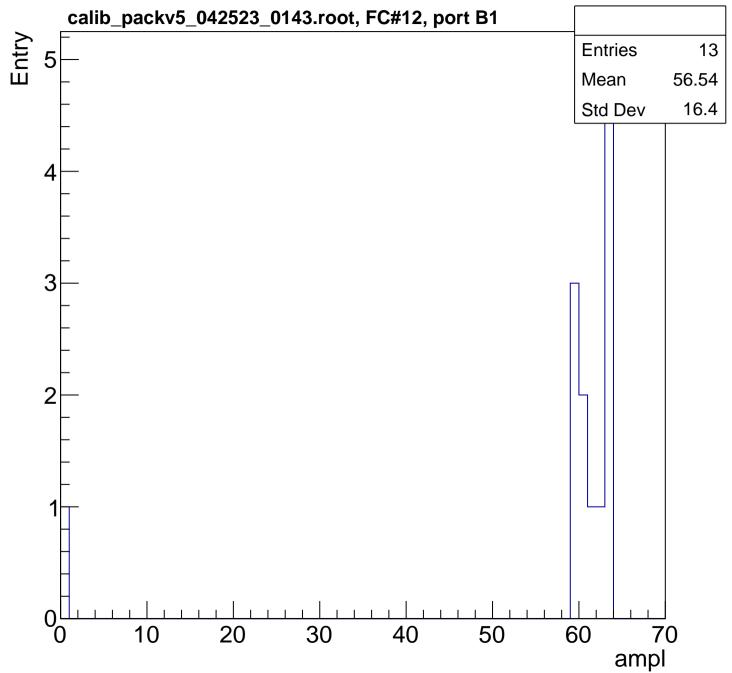


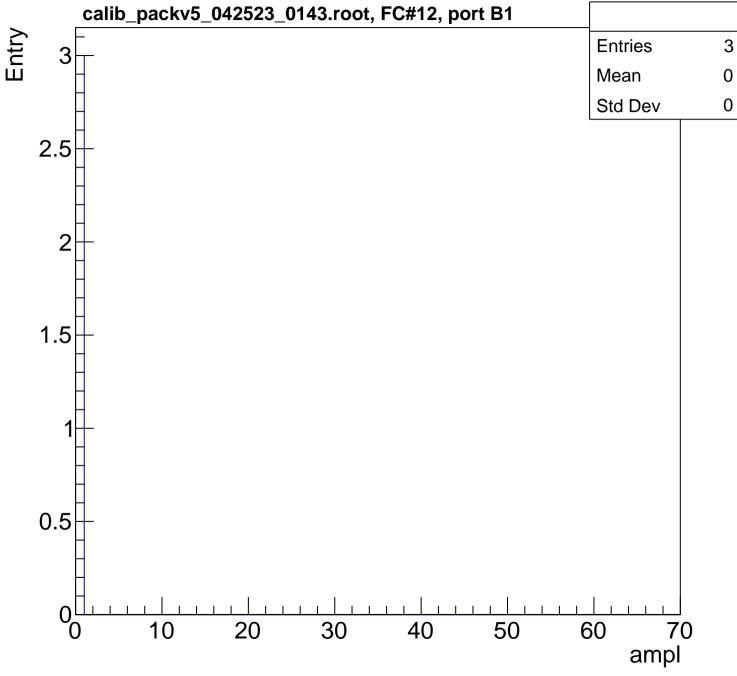


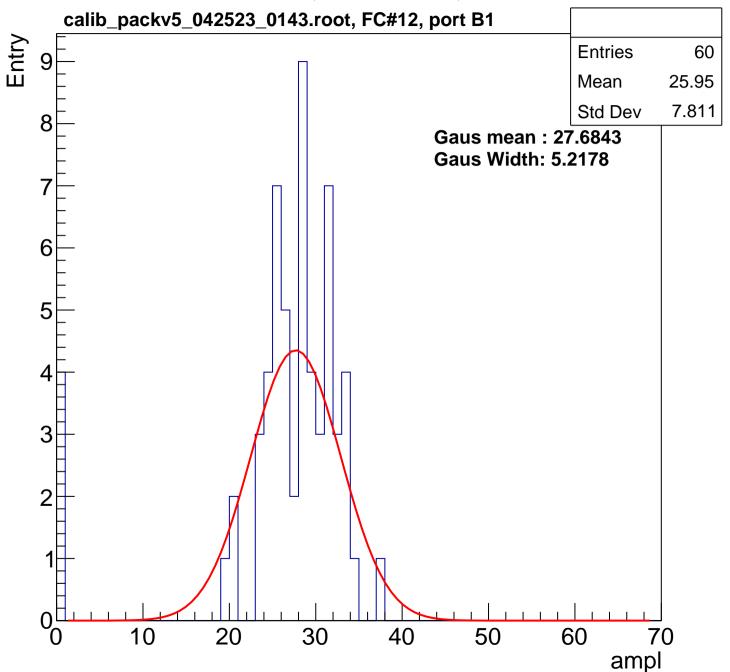


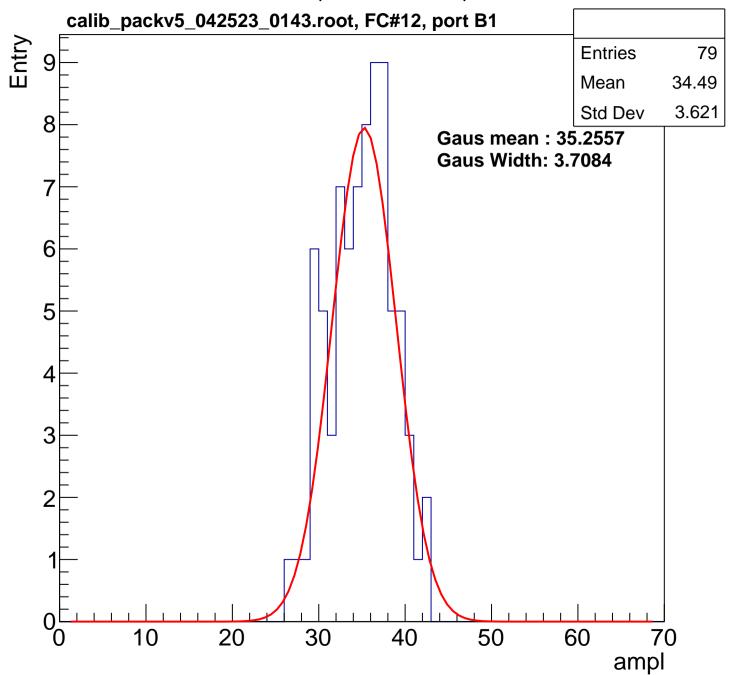


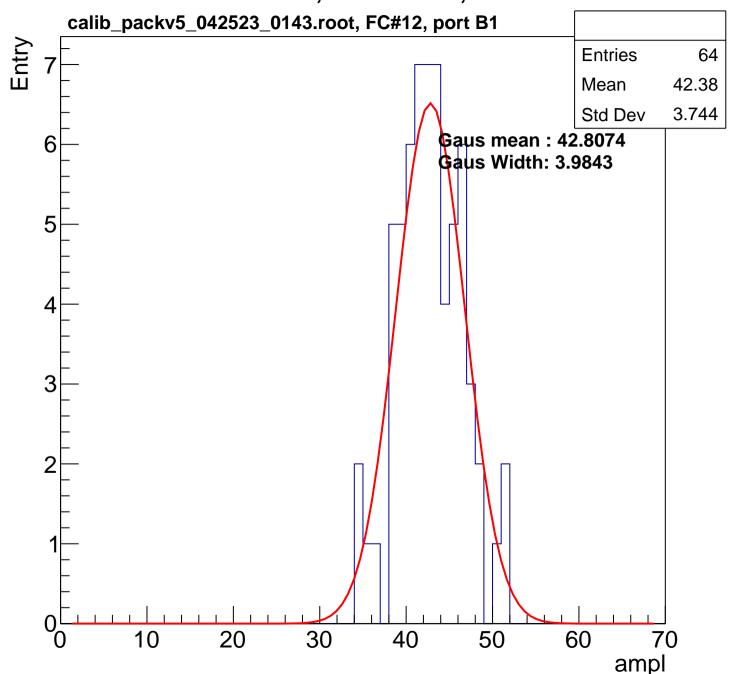


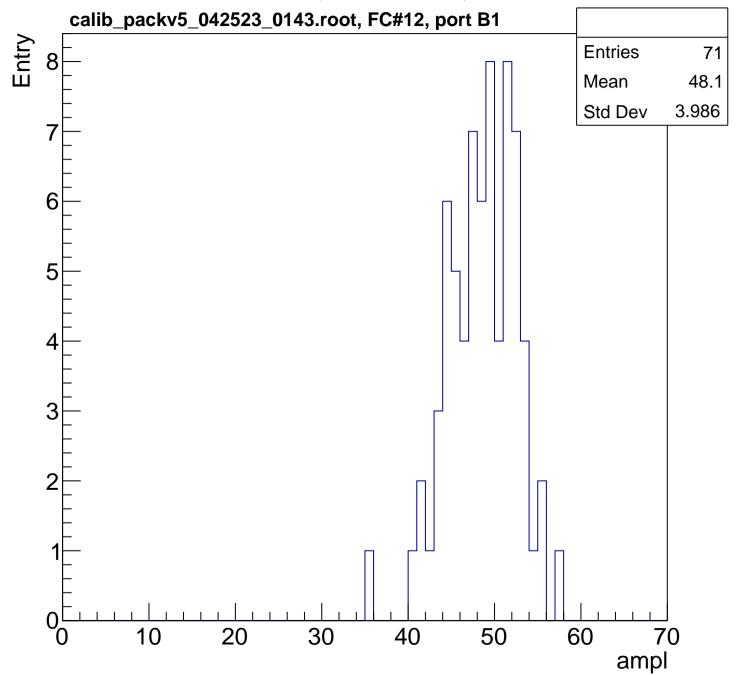


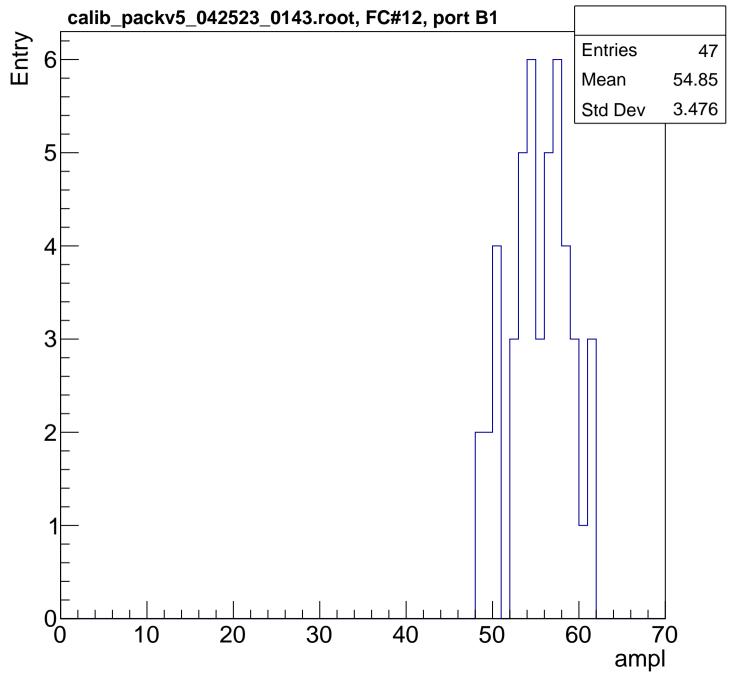


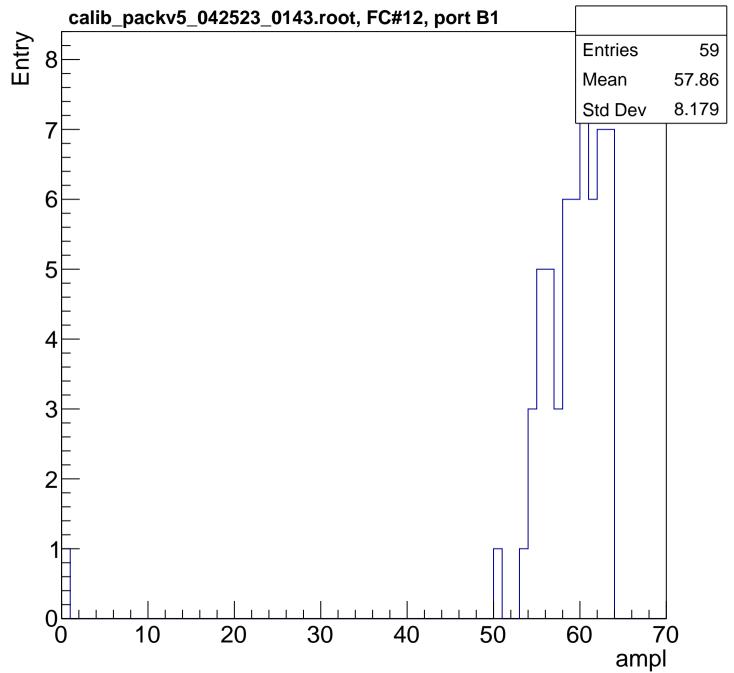


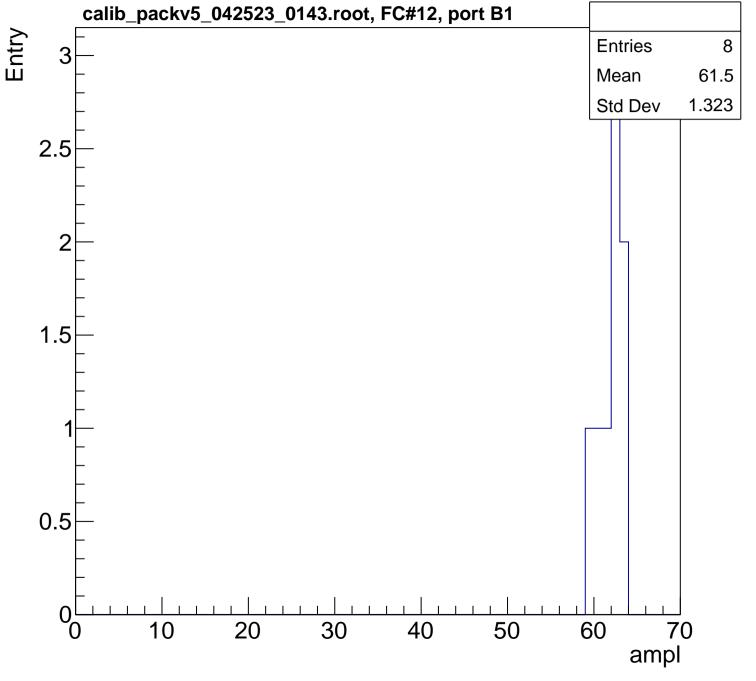


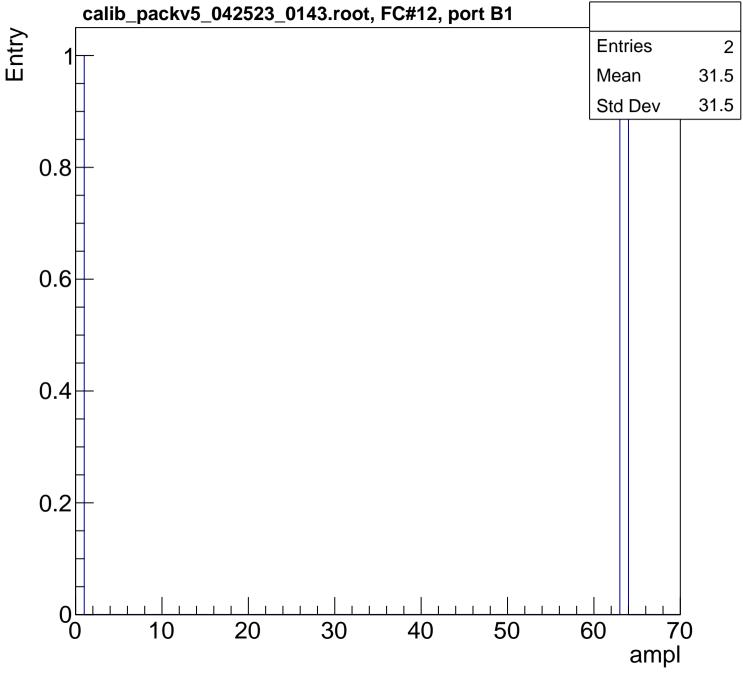


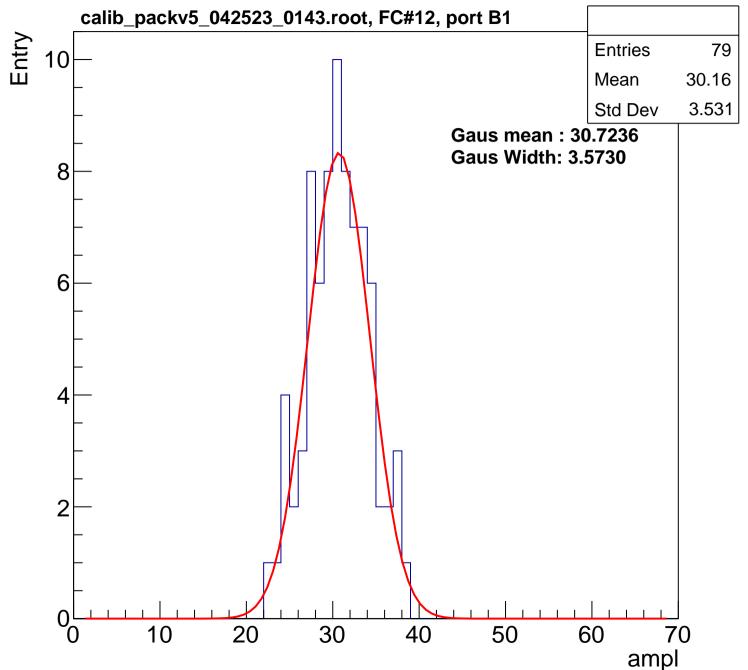


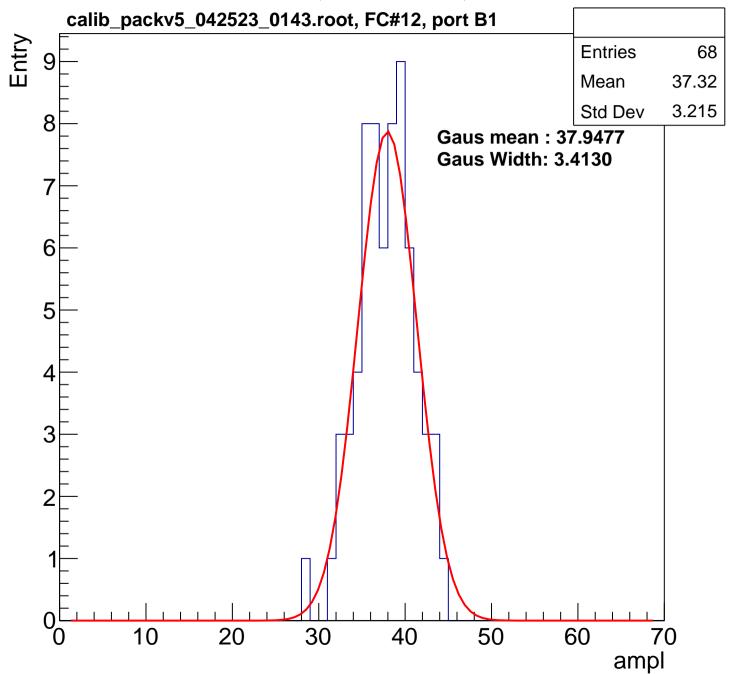


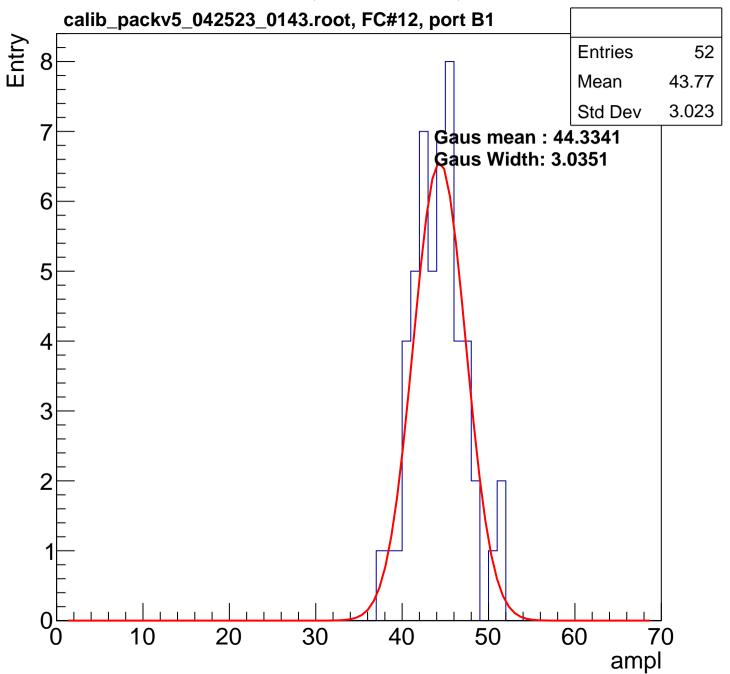


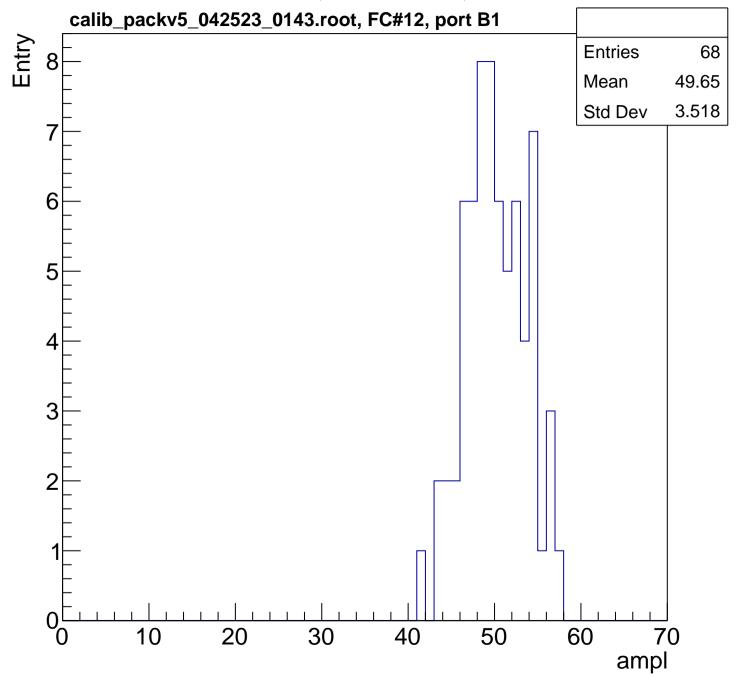


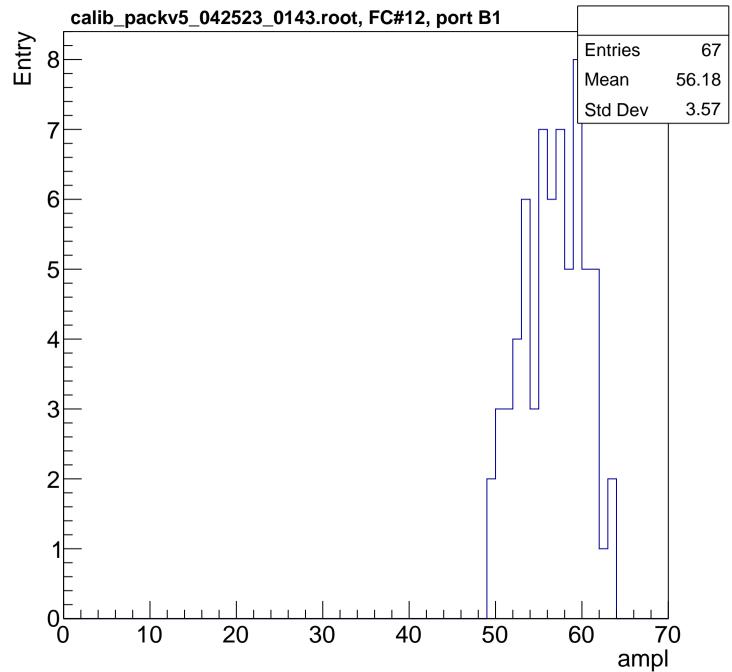


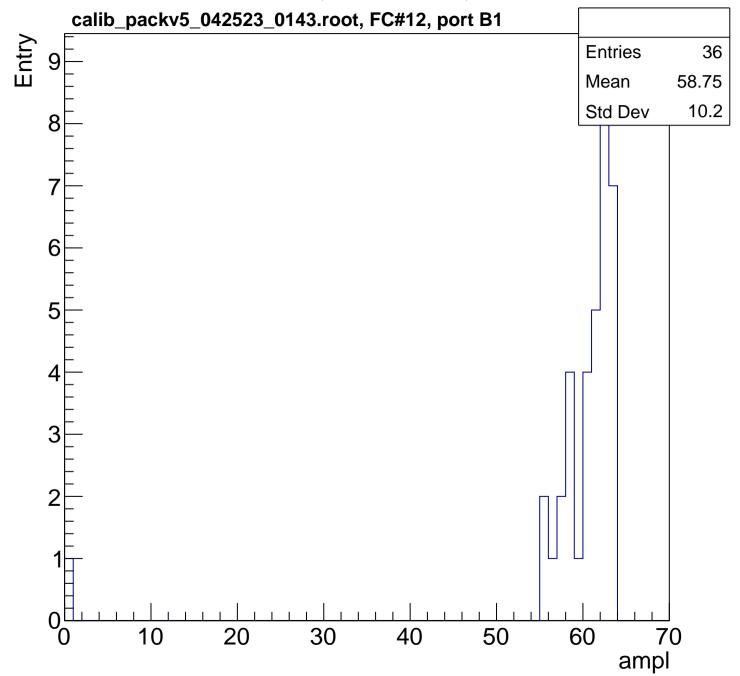


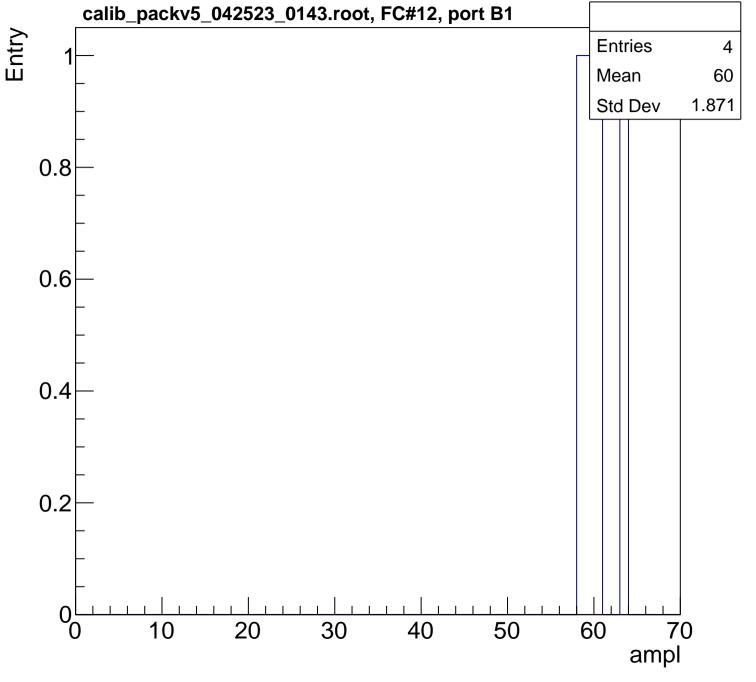


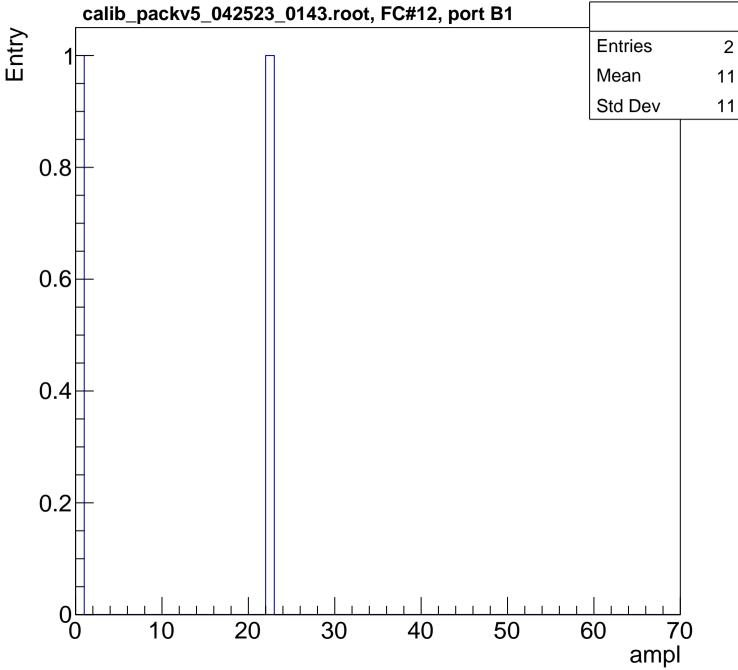


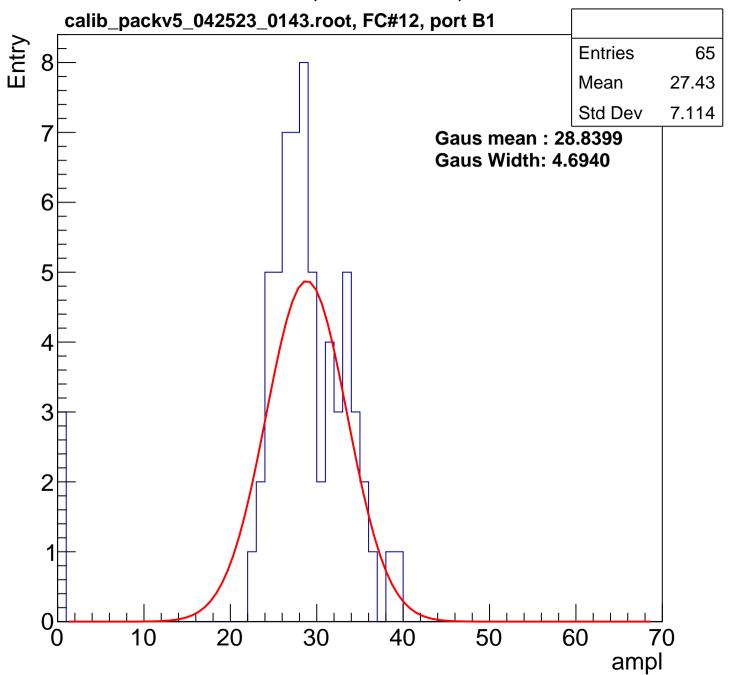


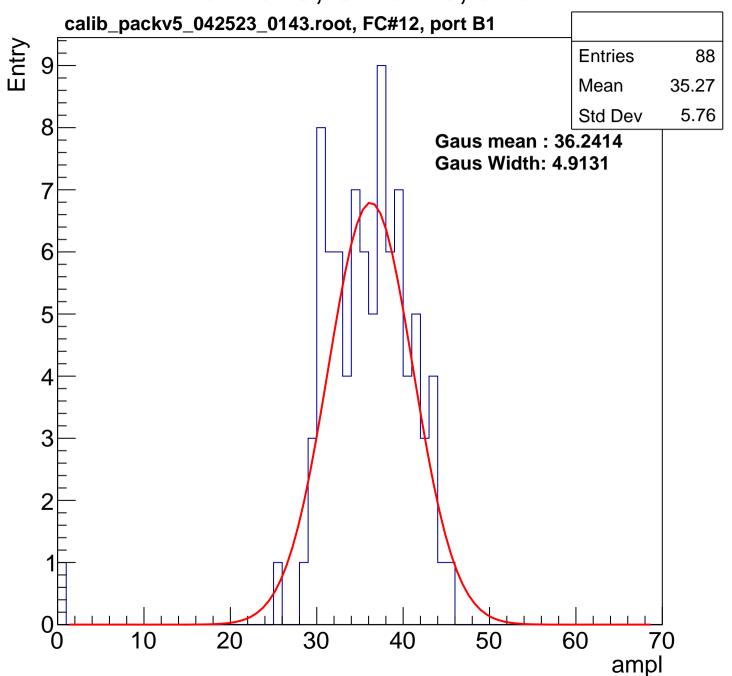


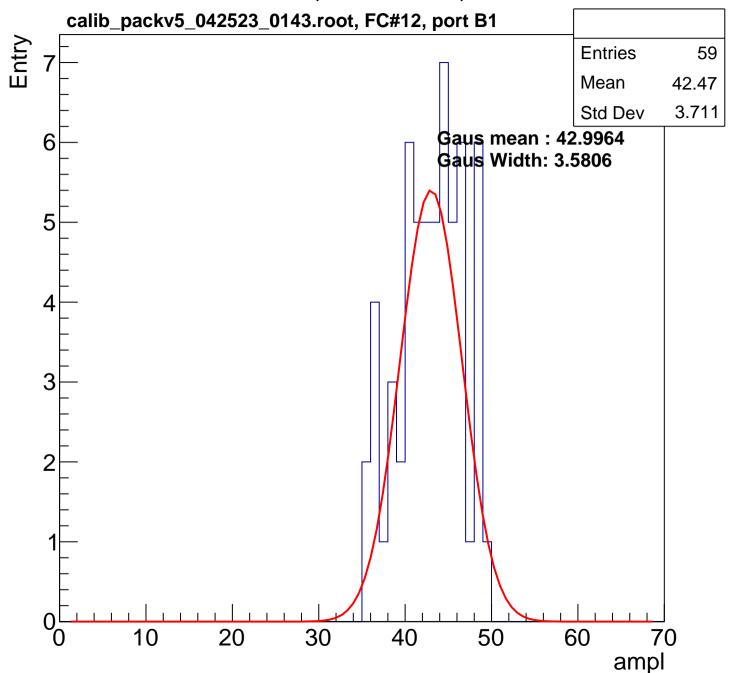


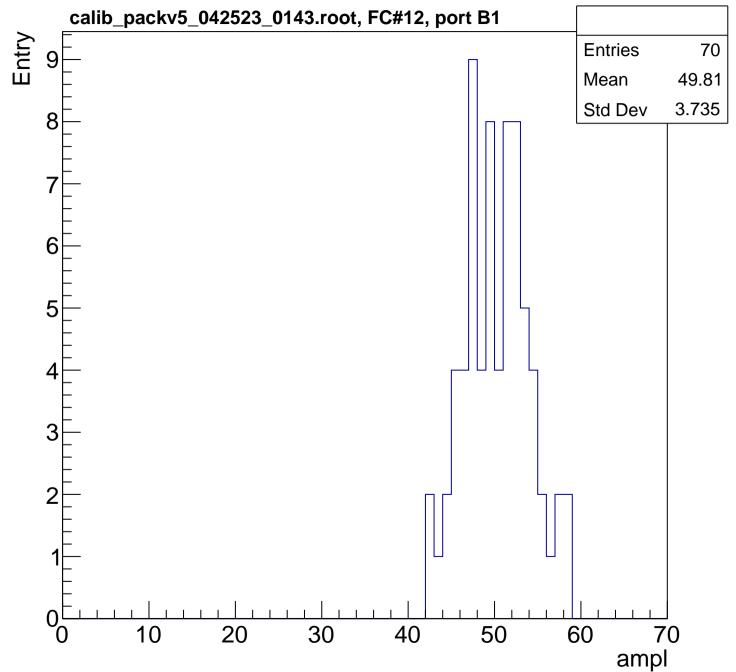


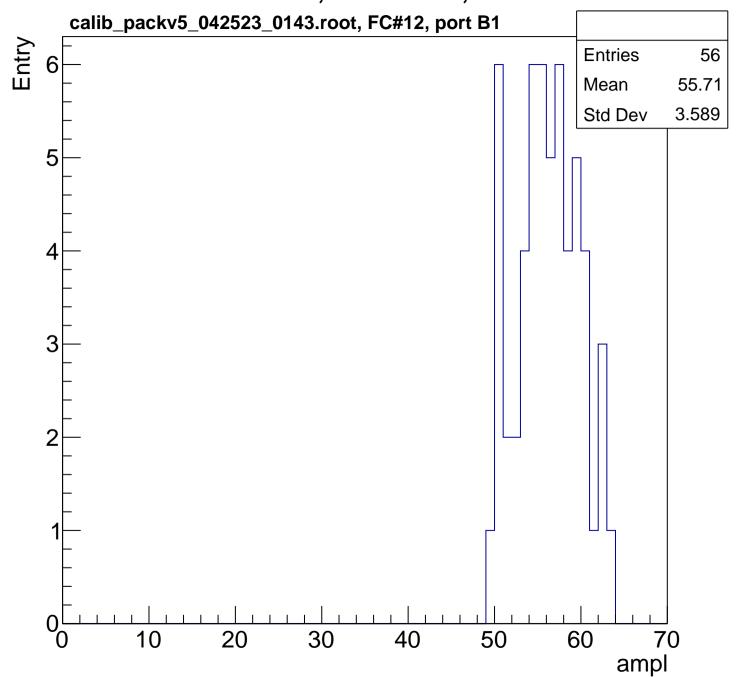


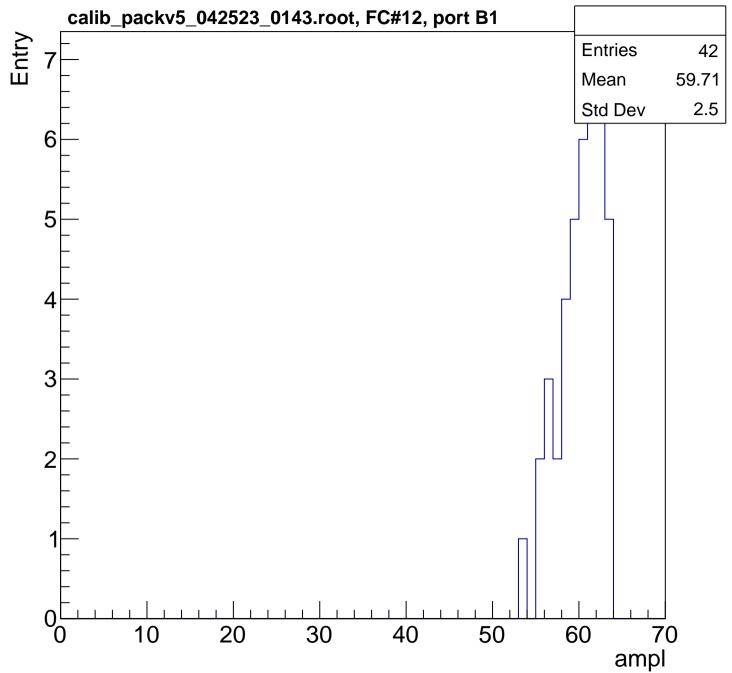


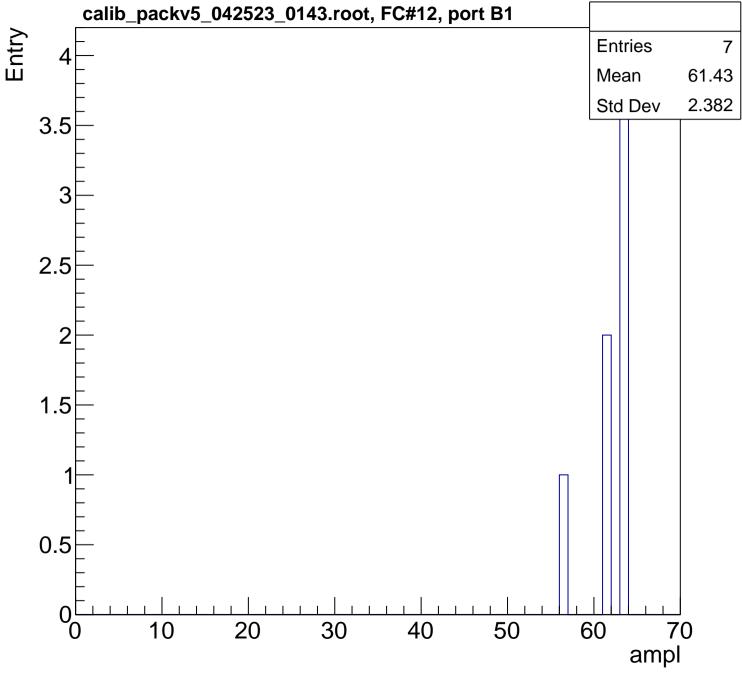




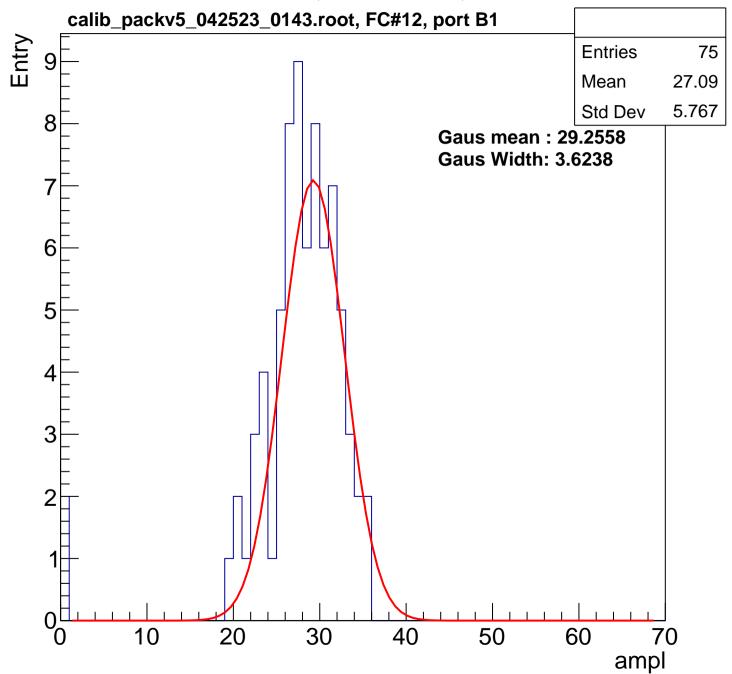


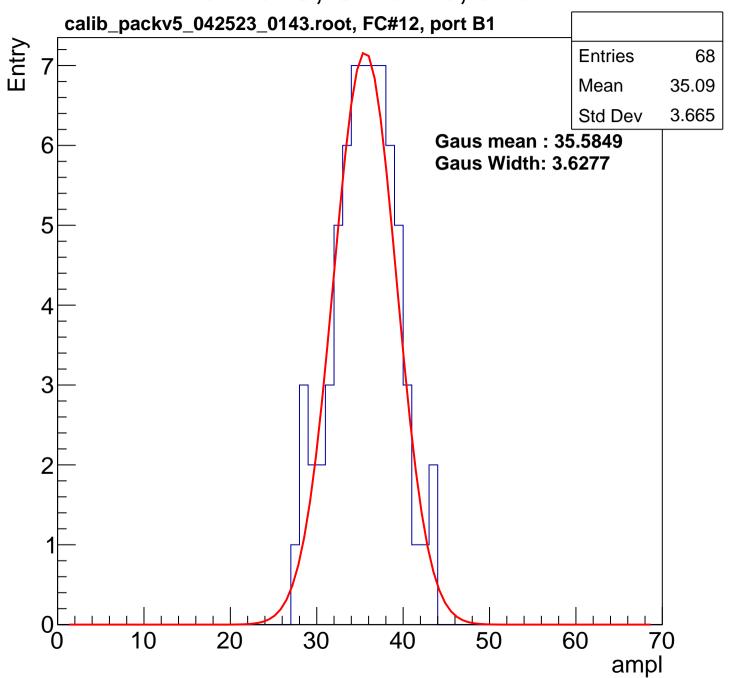


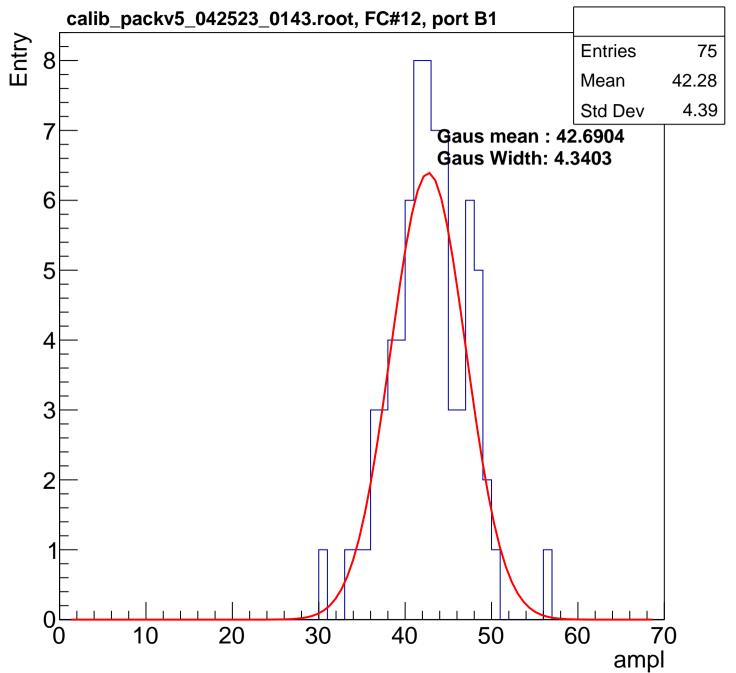


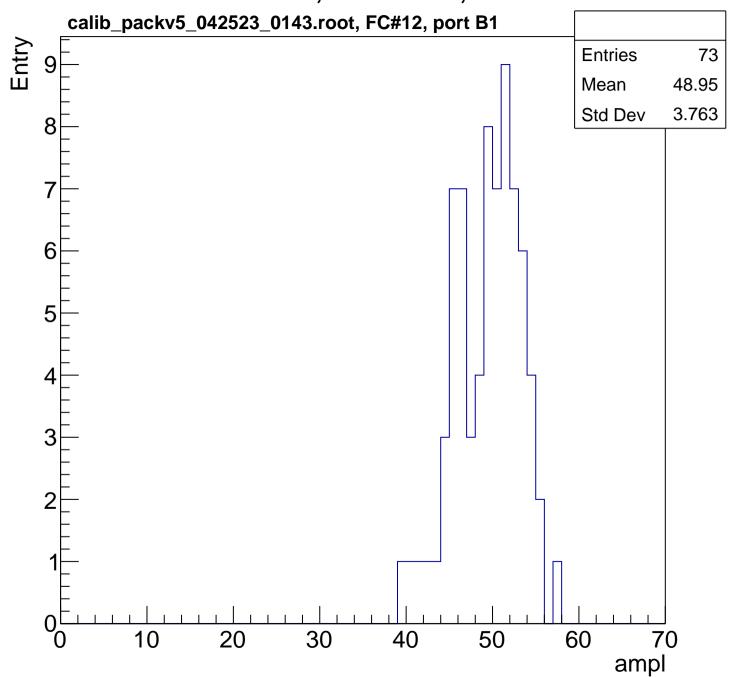


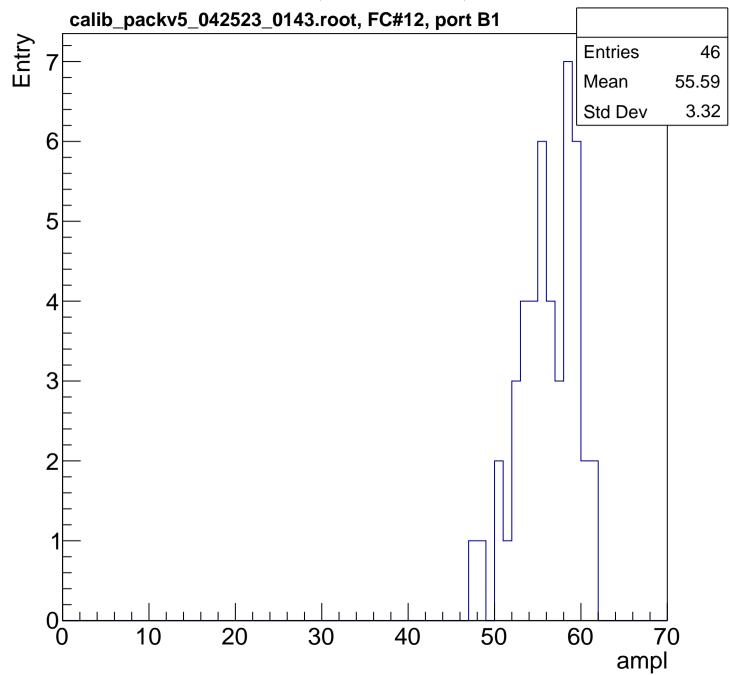


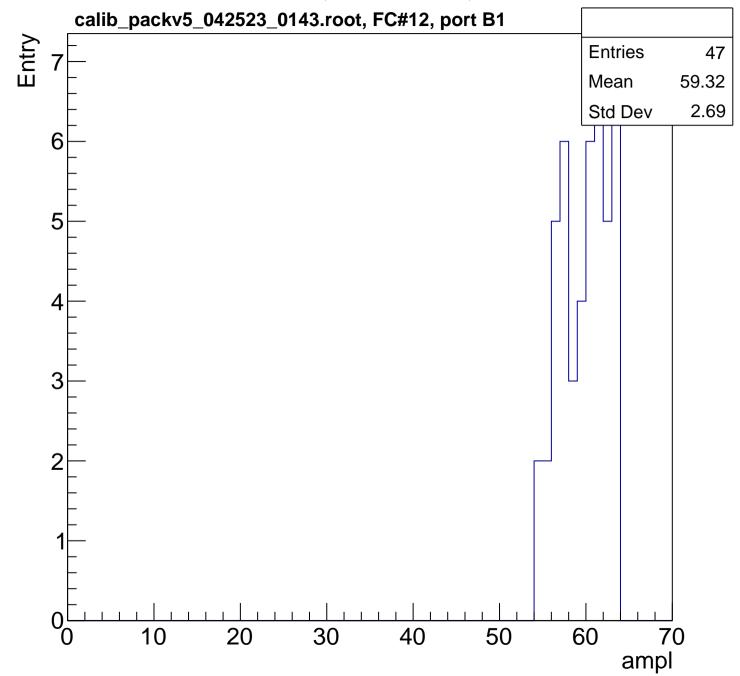


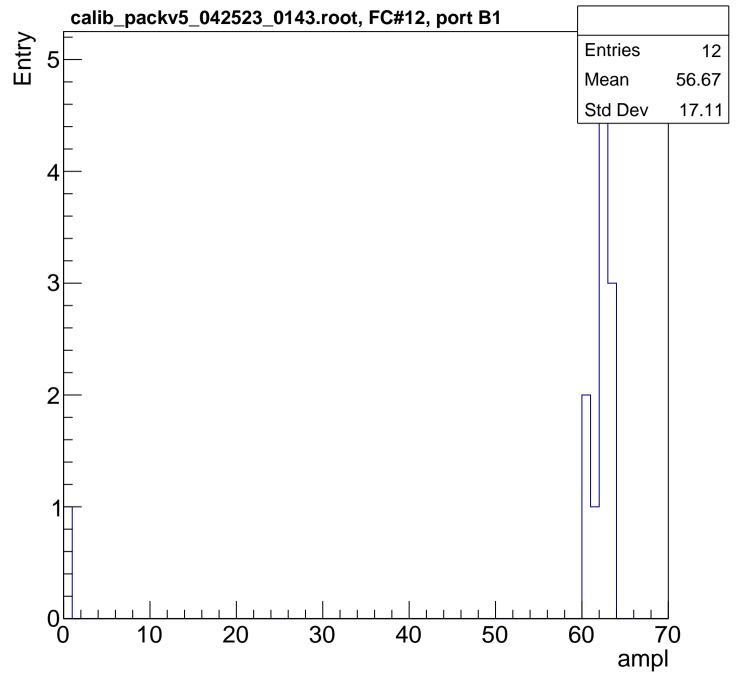




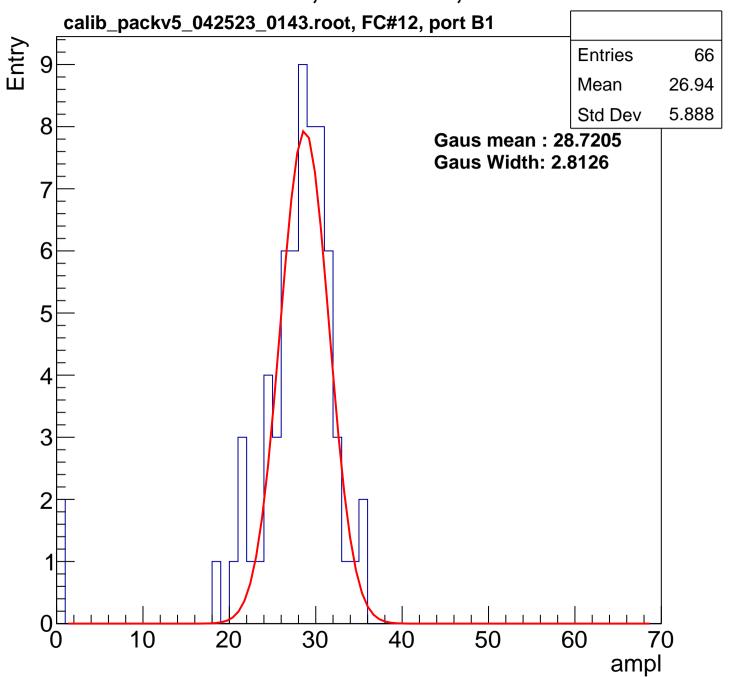


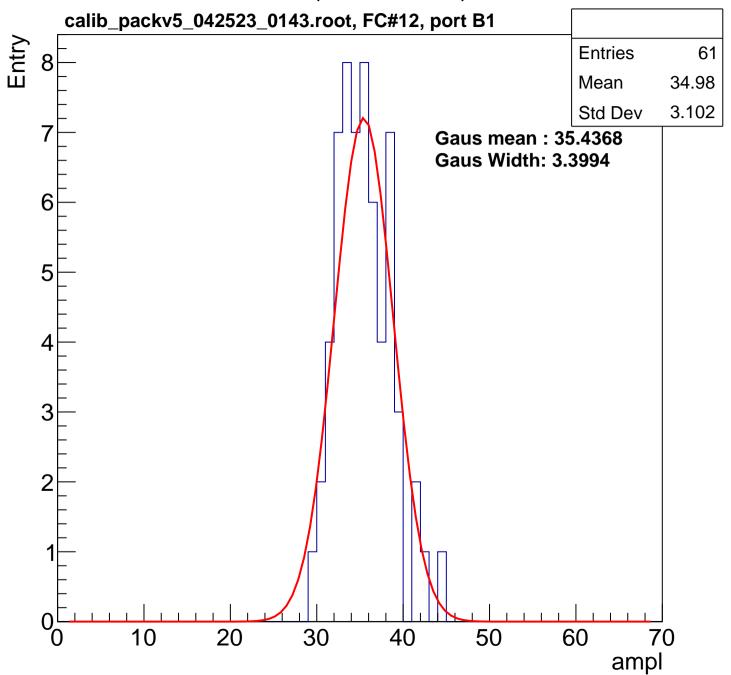


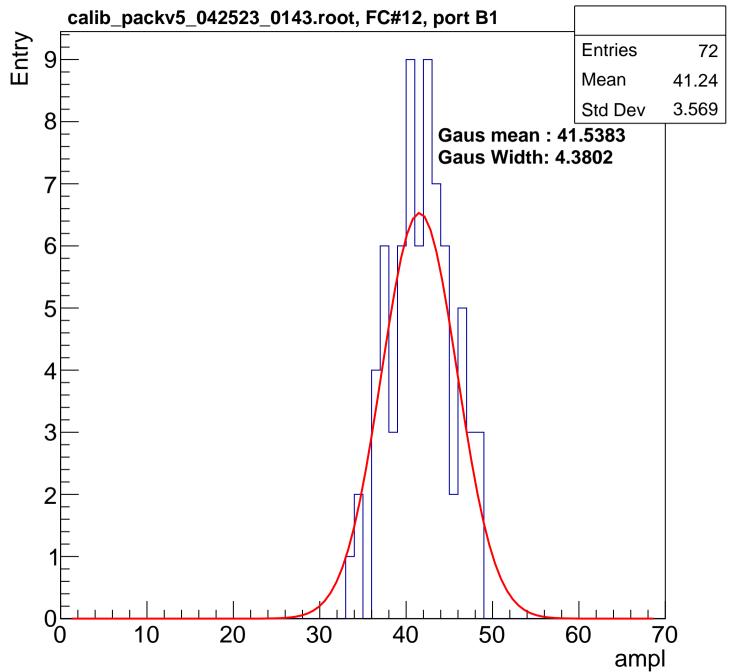


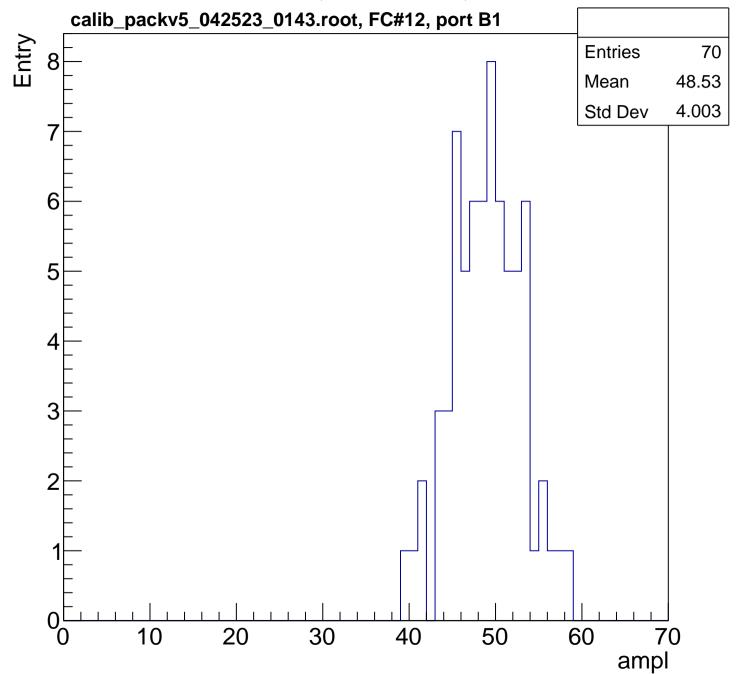


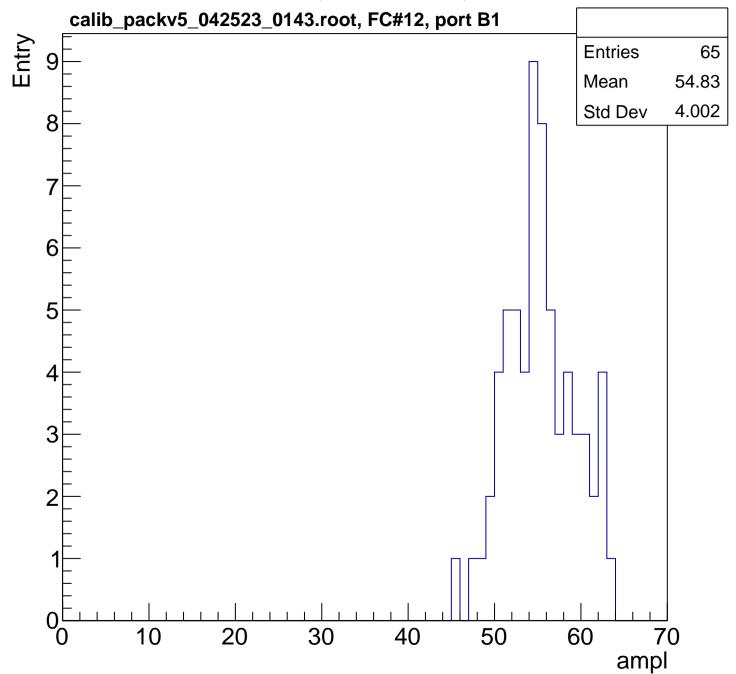


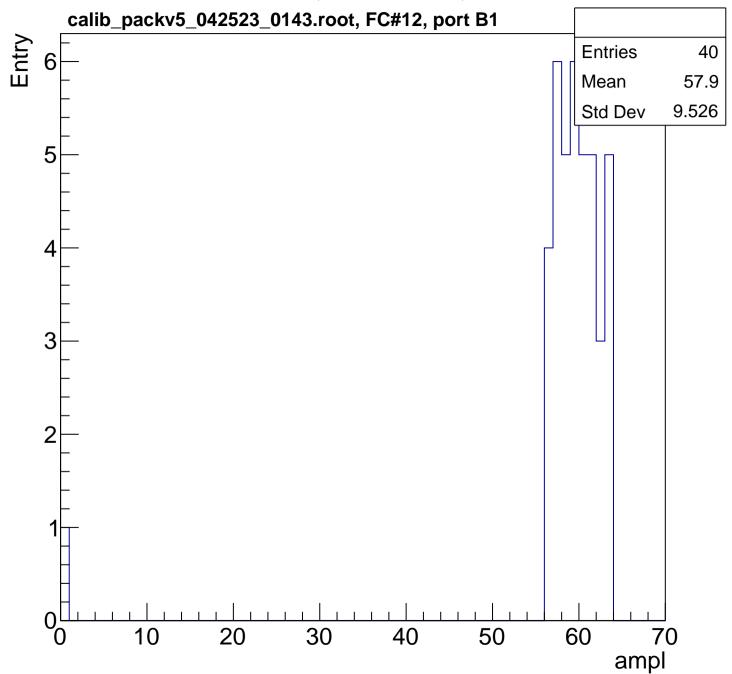


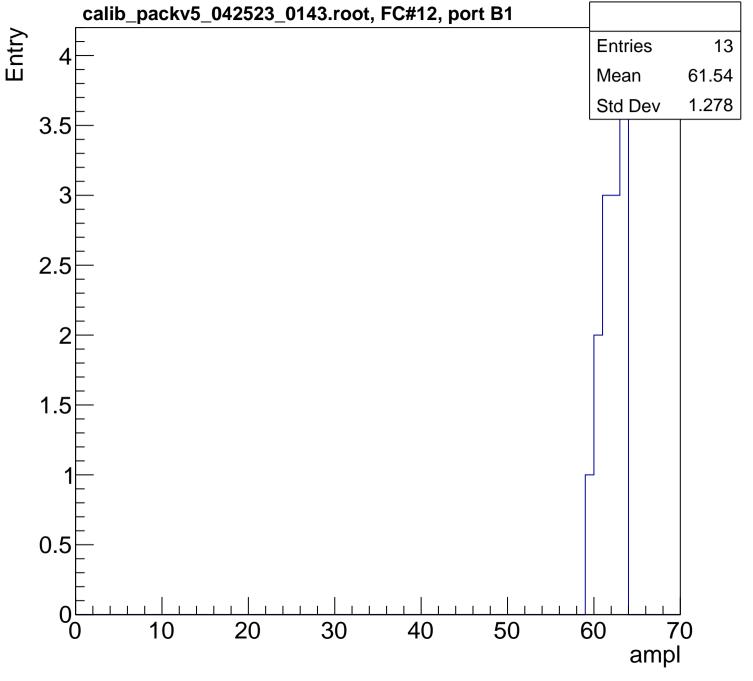




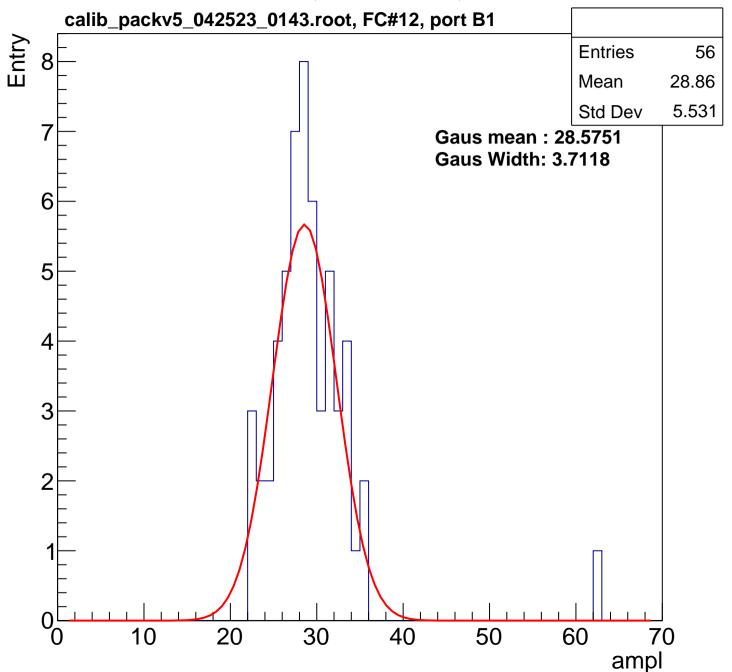


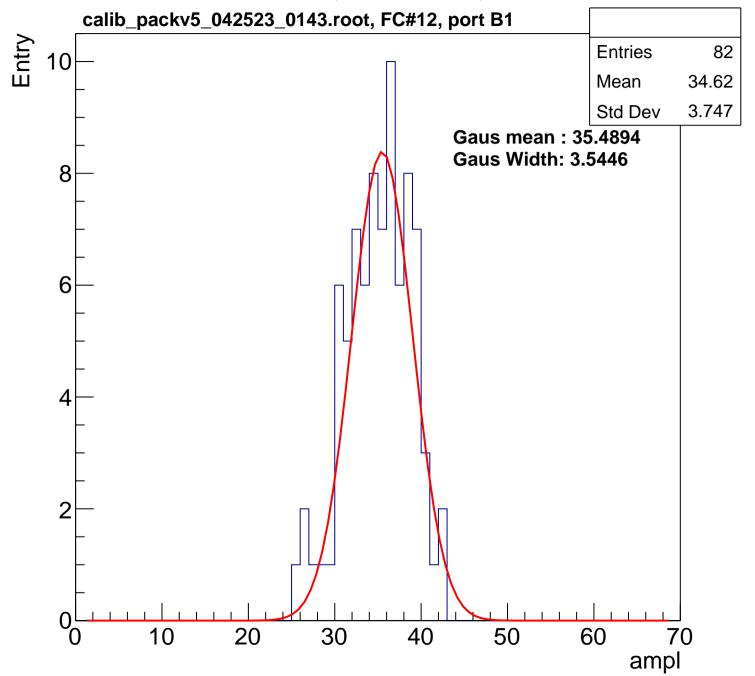


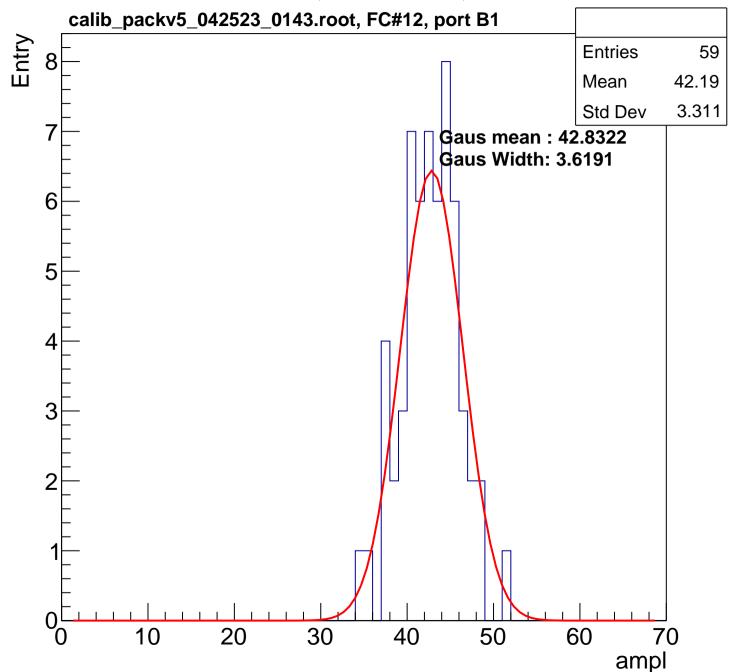


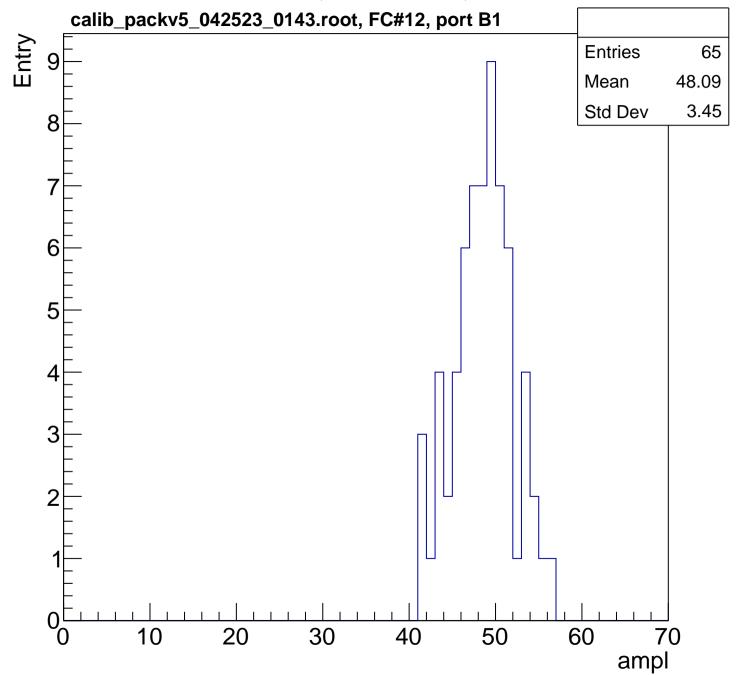


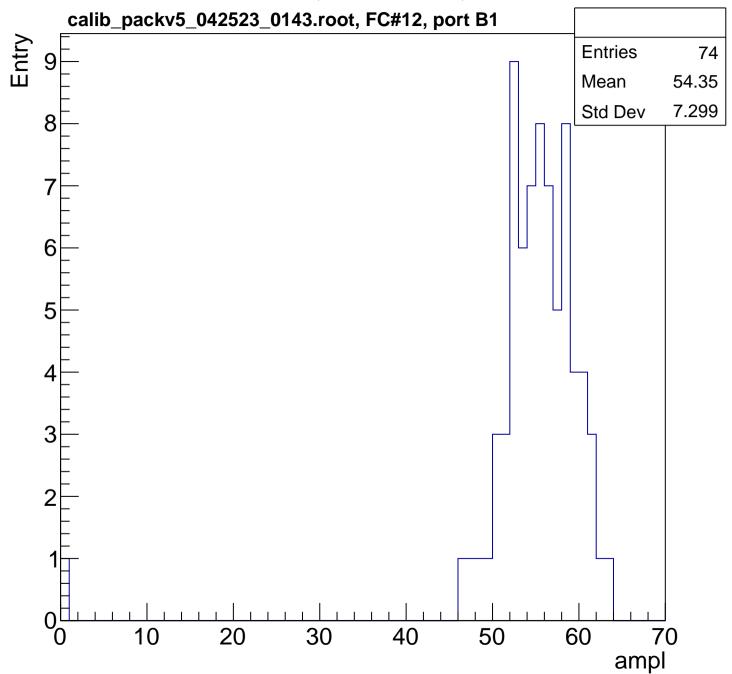
B0L102S, U4-ch80, adc7 calib_packv5_042523_0143.root, FC#12, port B1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

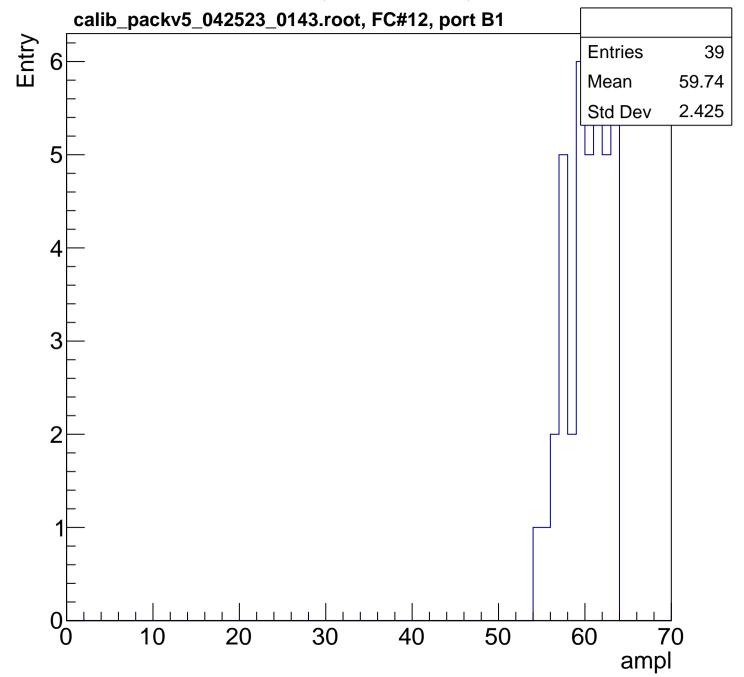


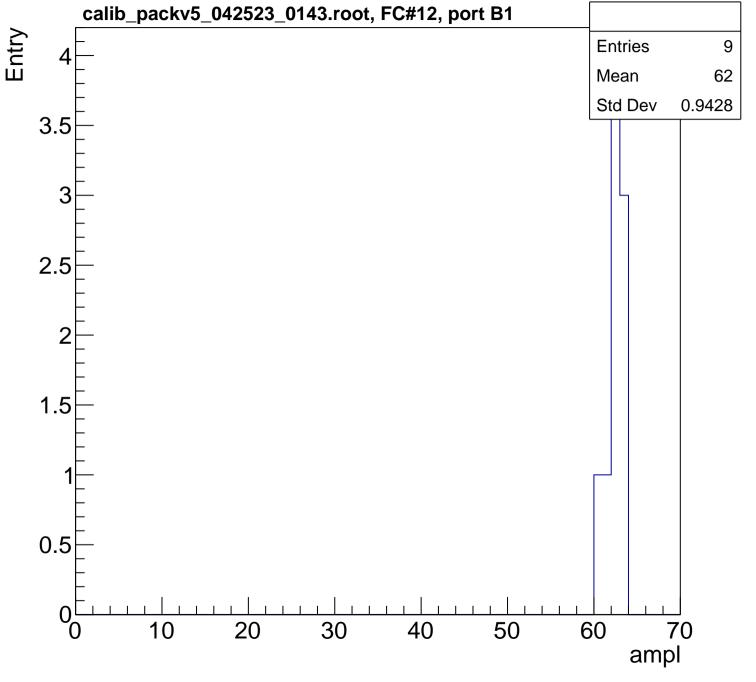


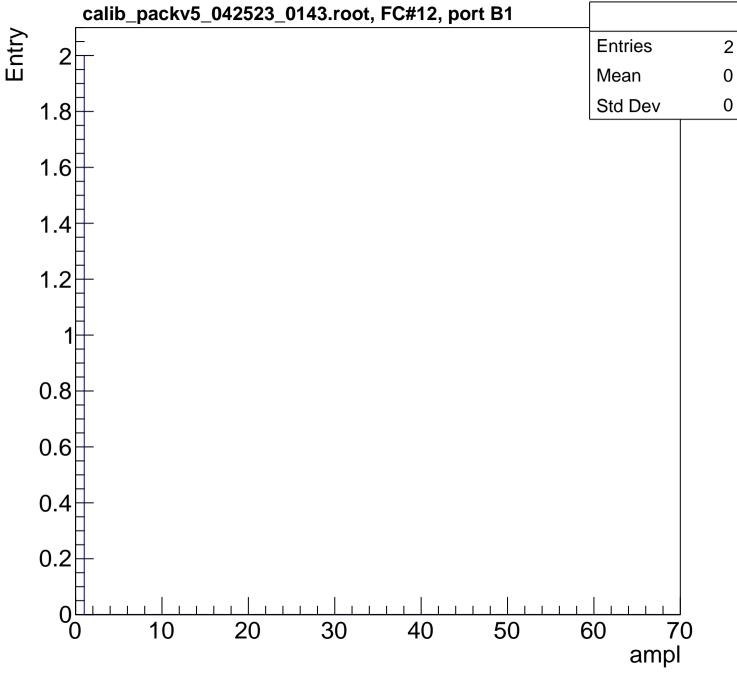


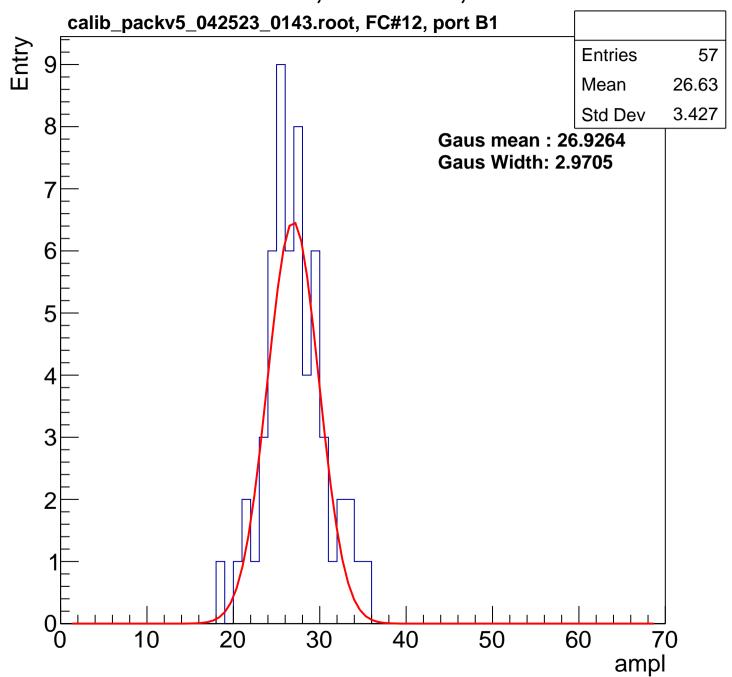


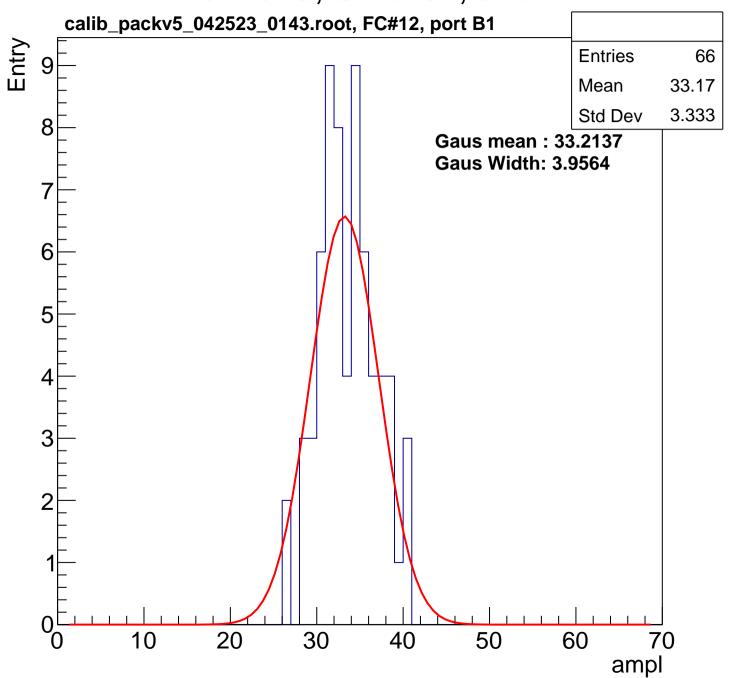


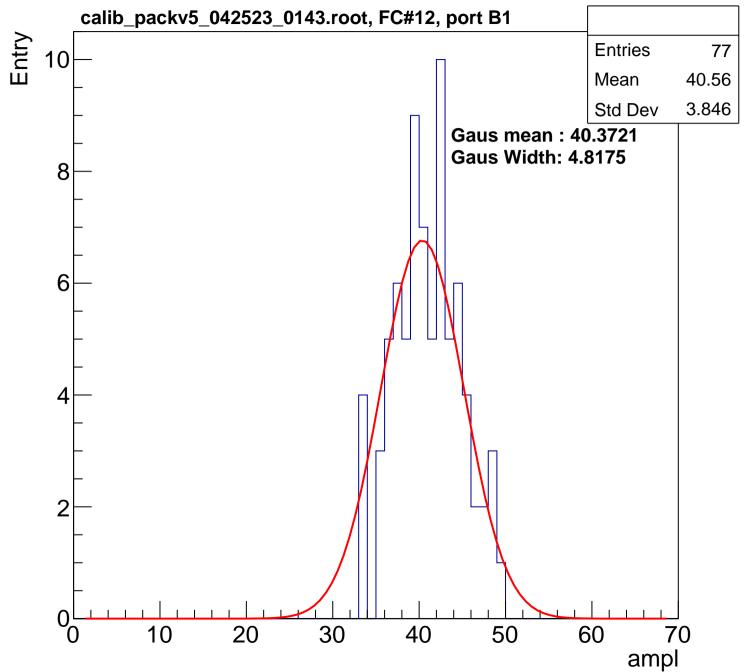


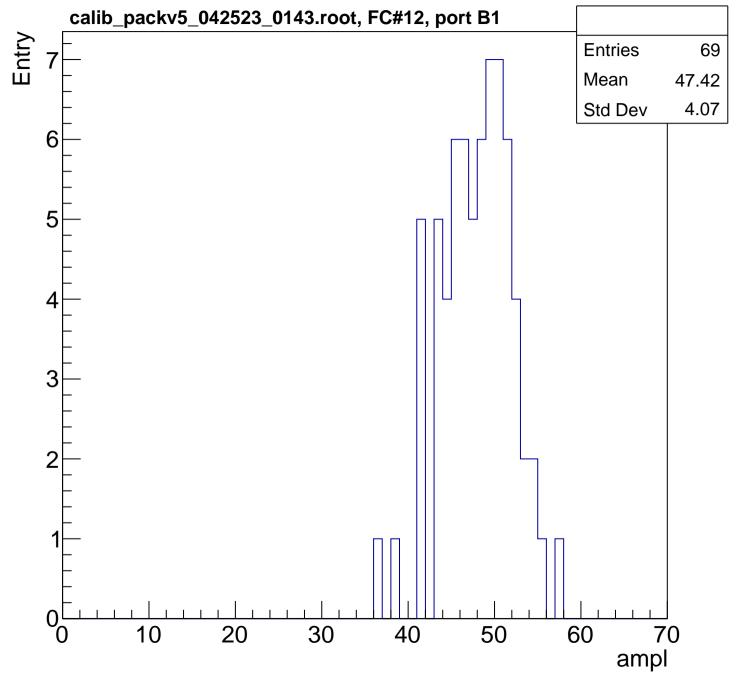


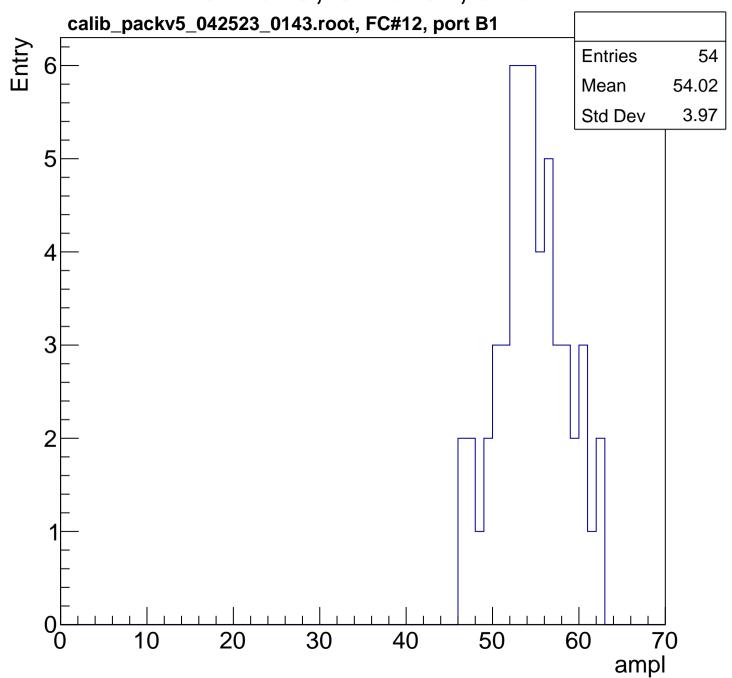


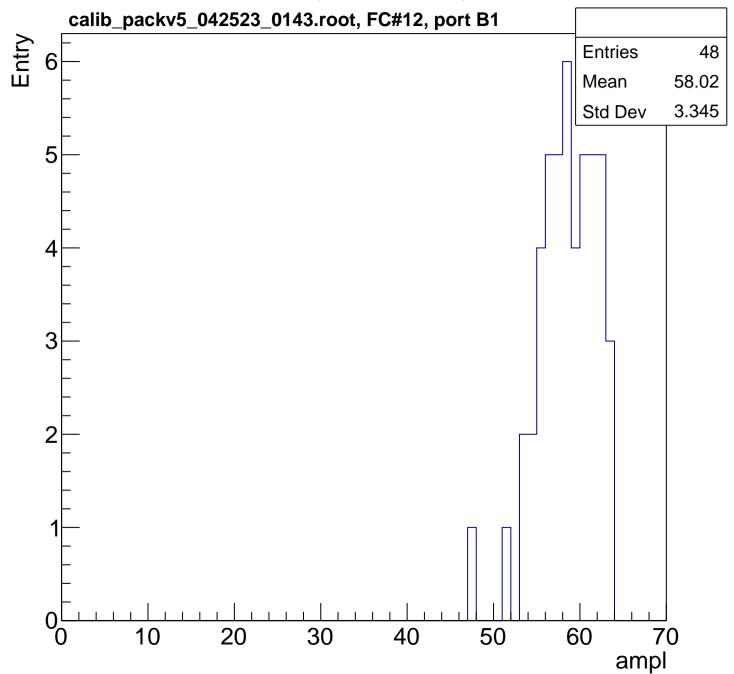


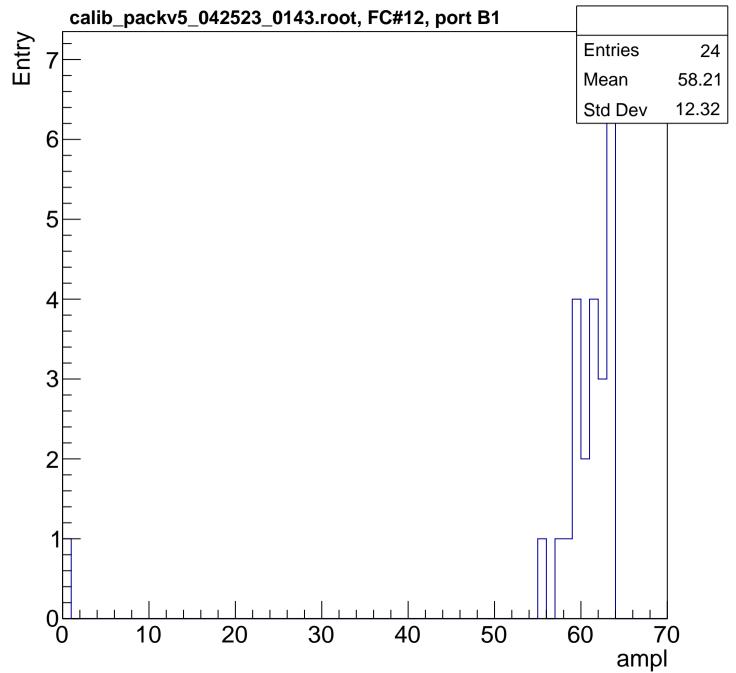




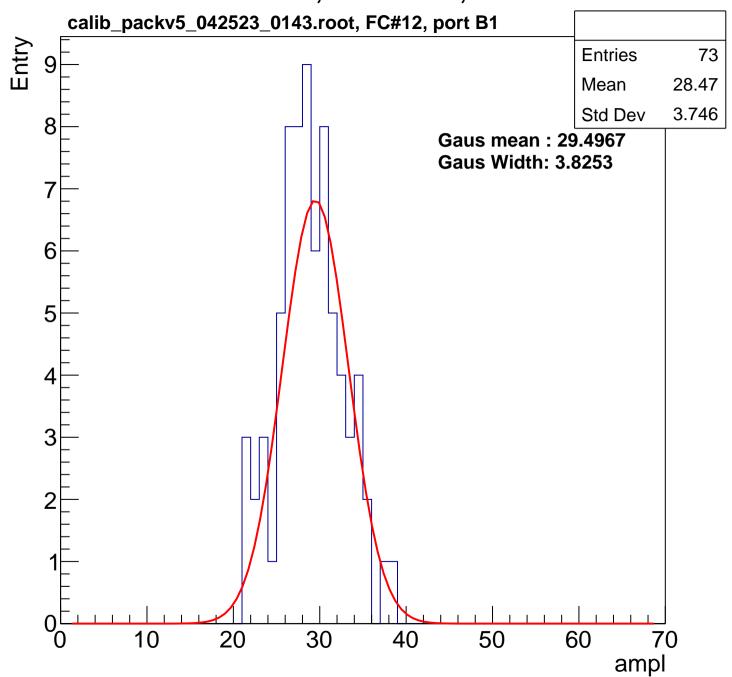


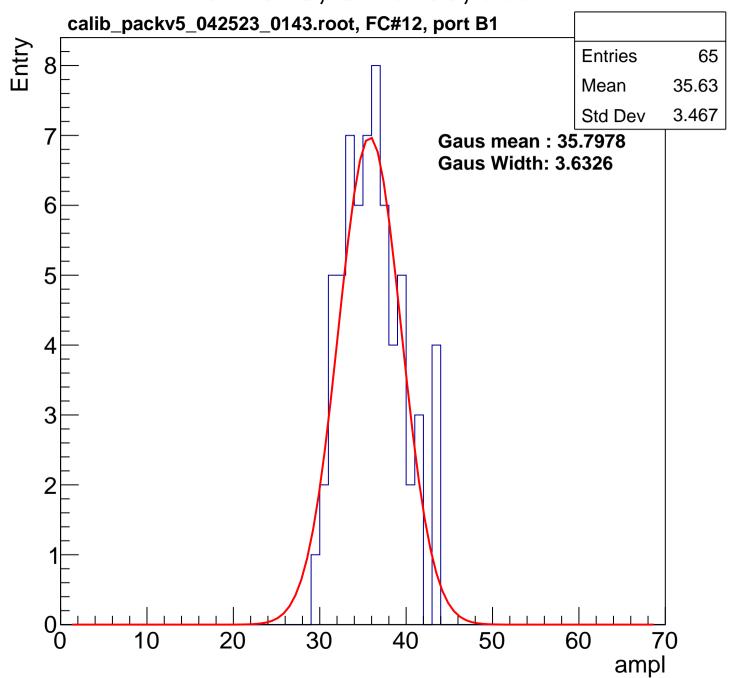


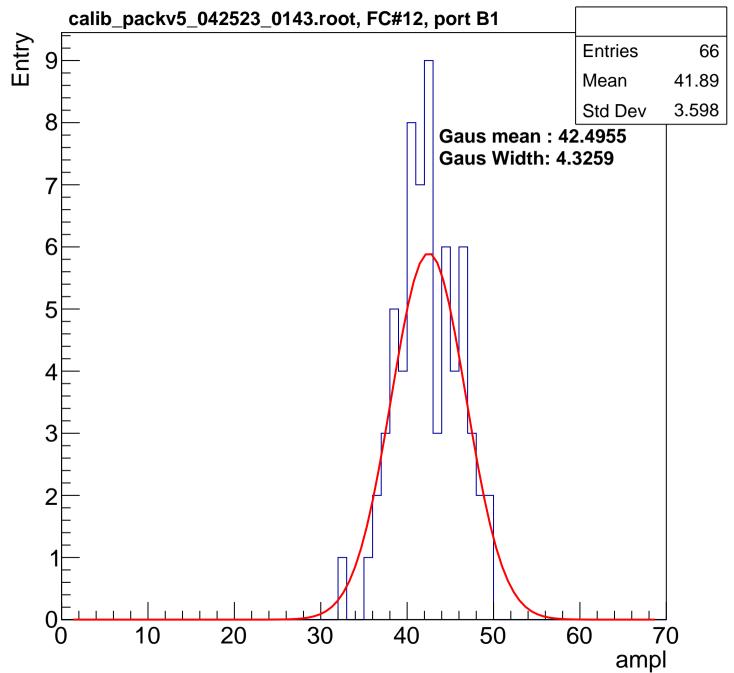


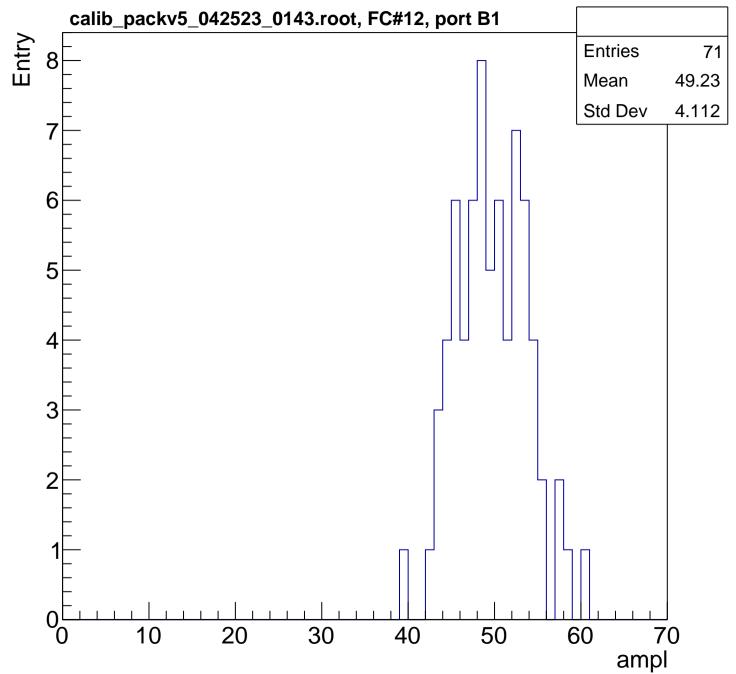


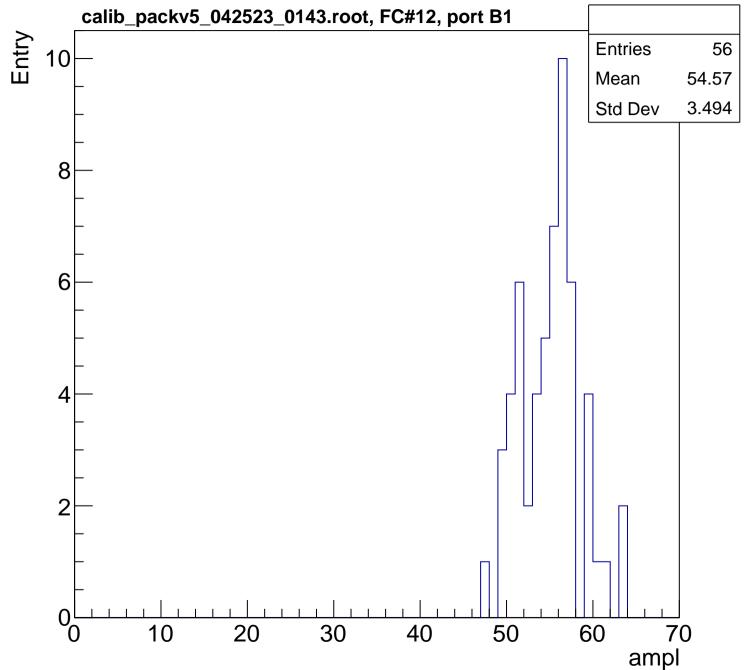


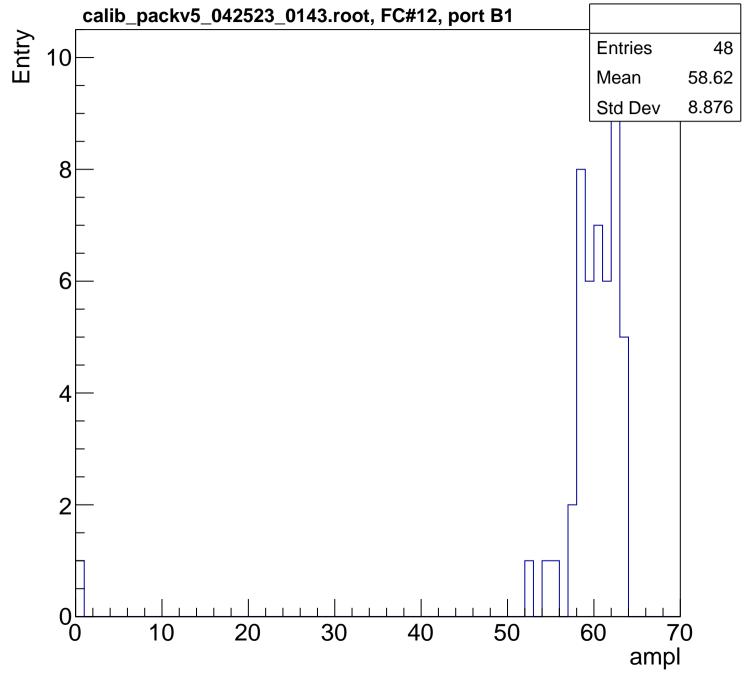


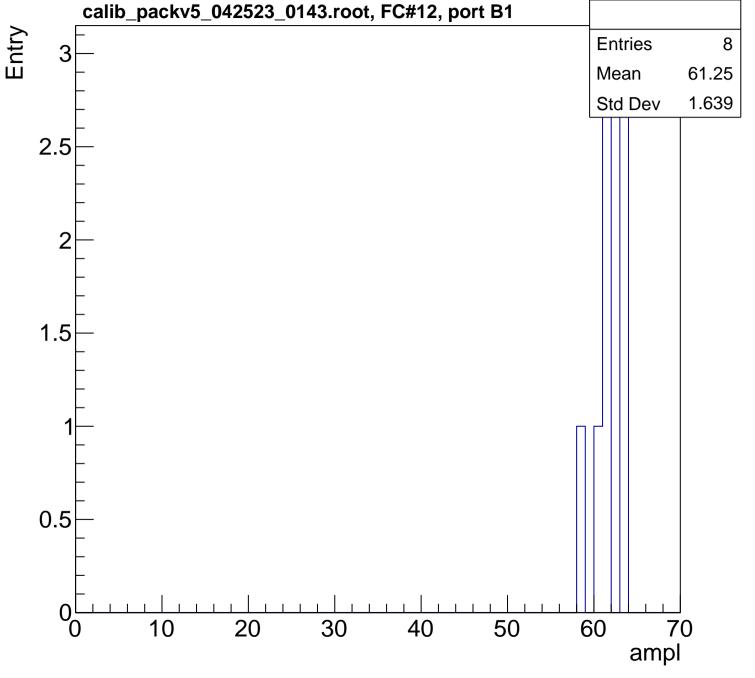




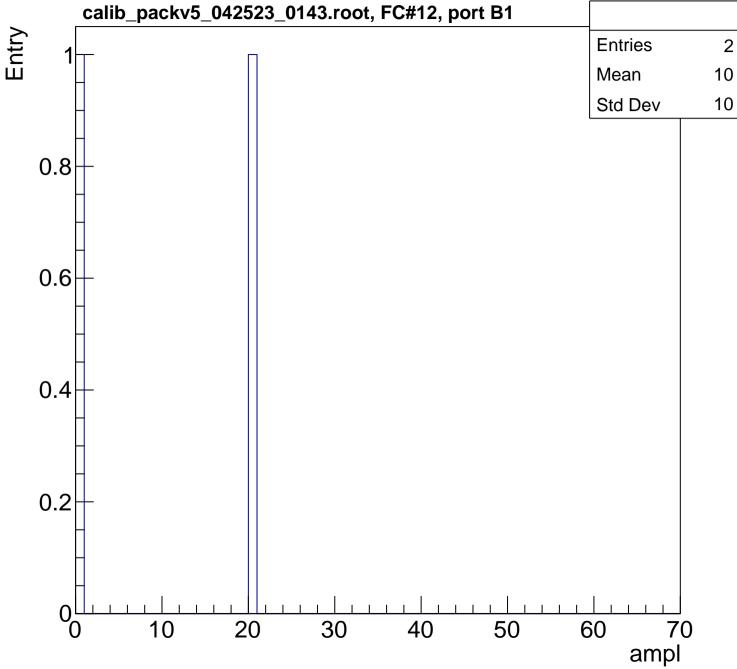


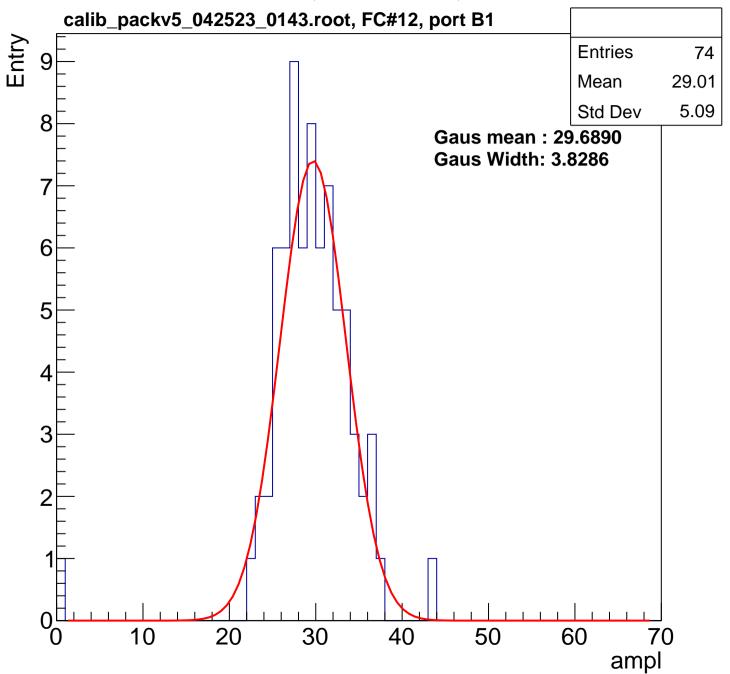


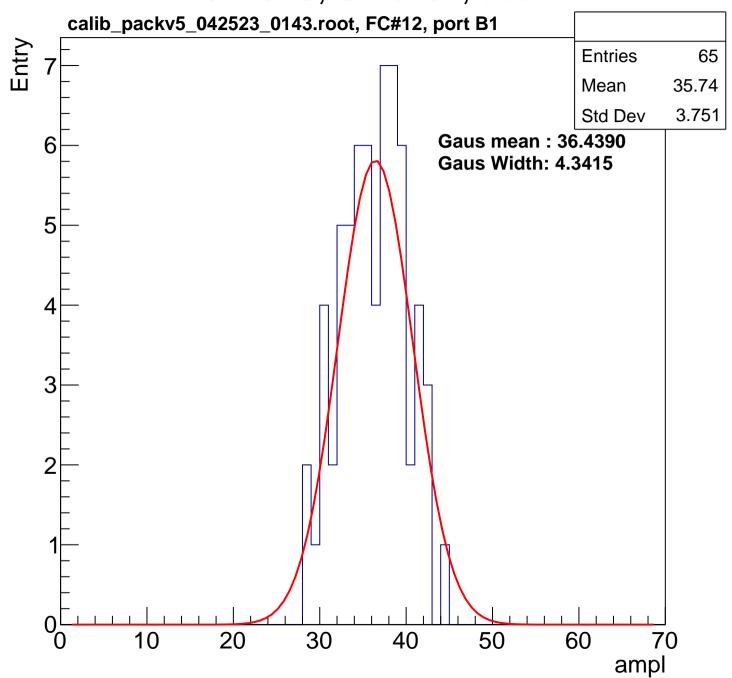


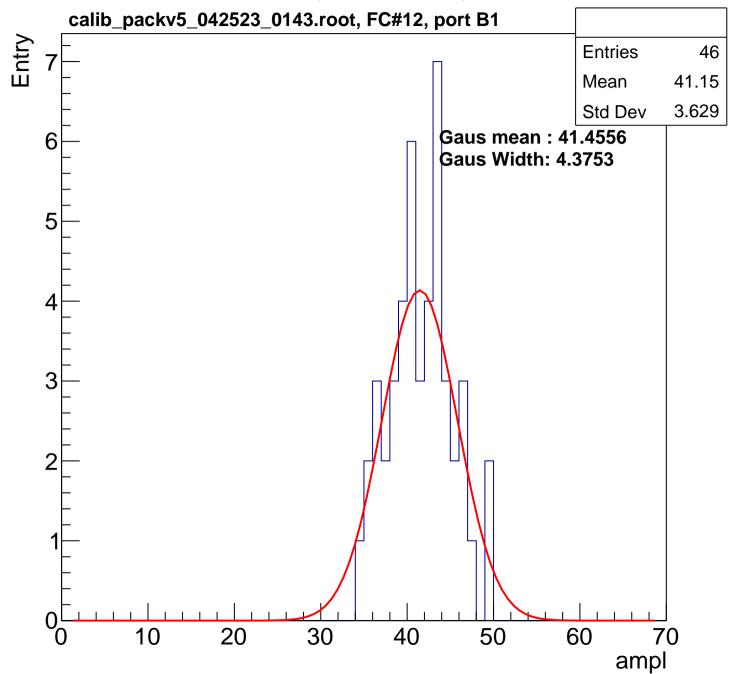


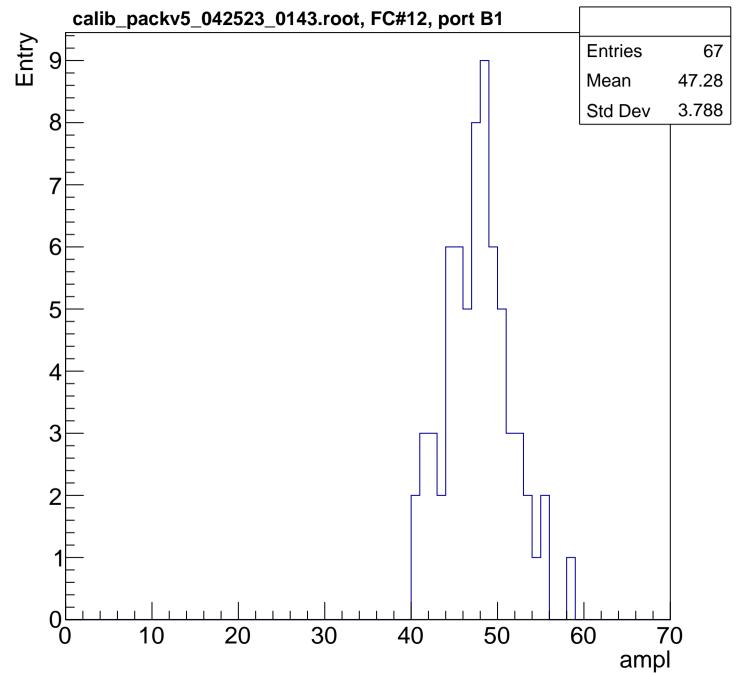
2

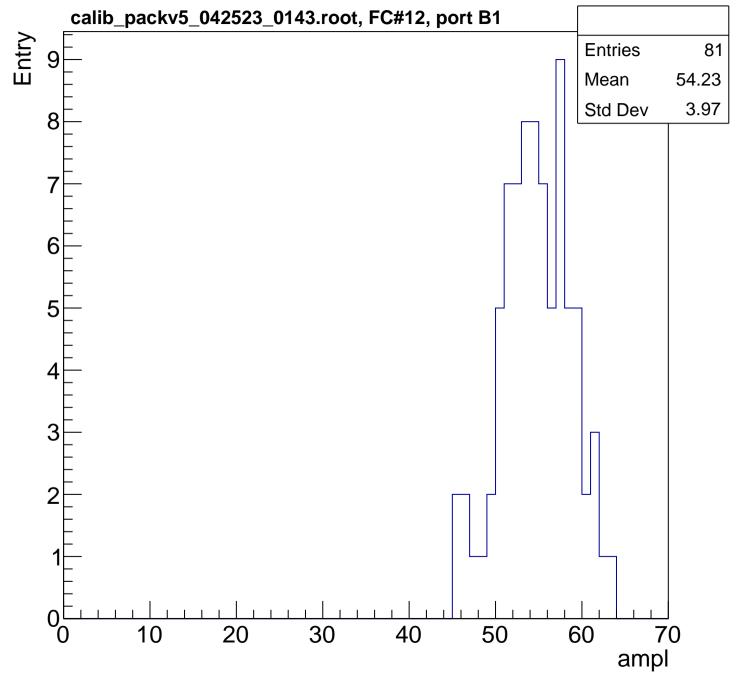


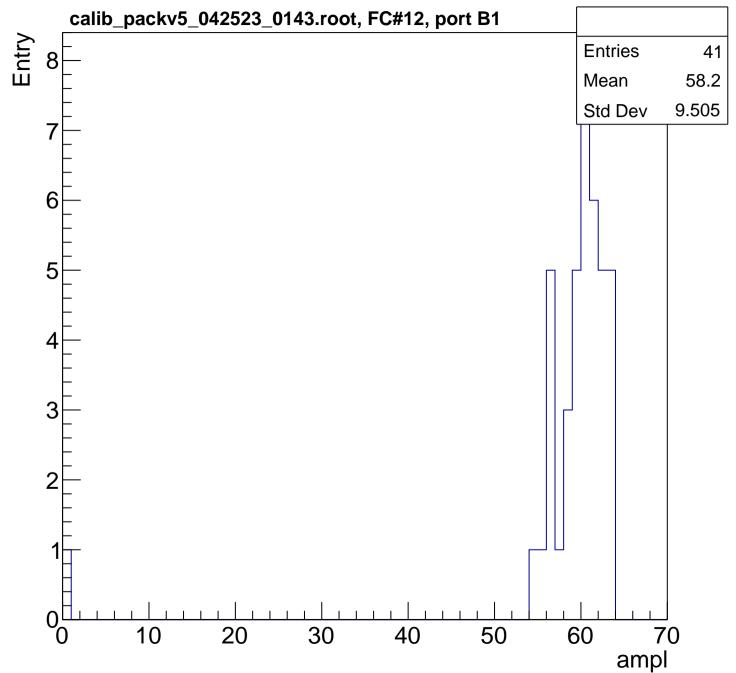


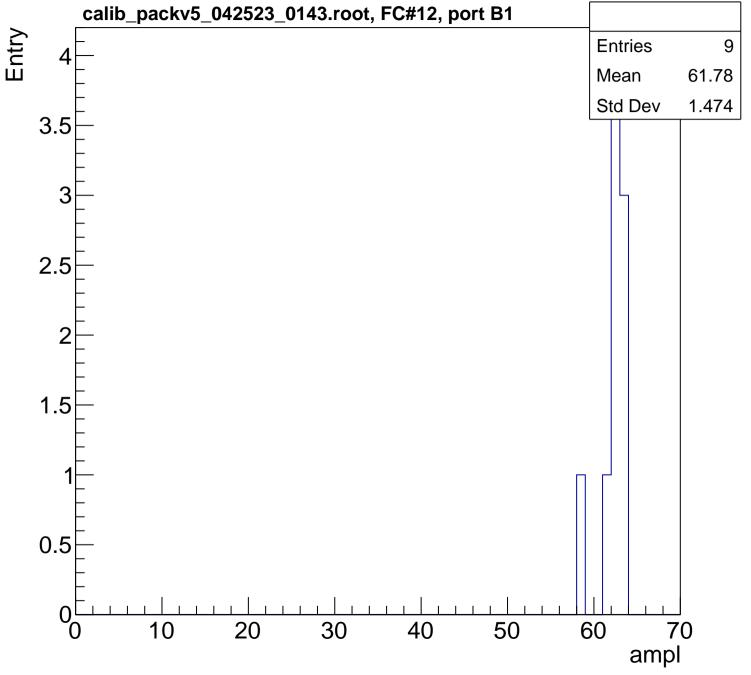




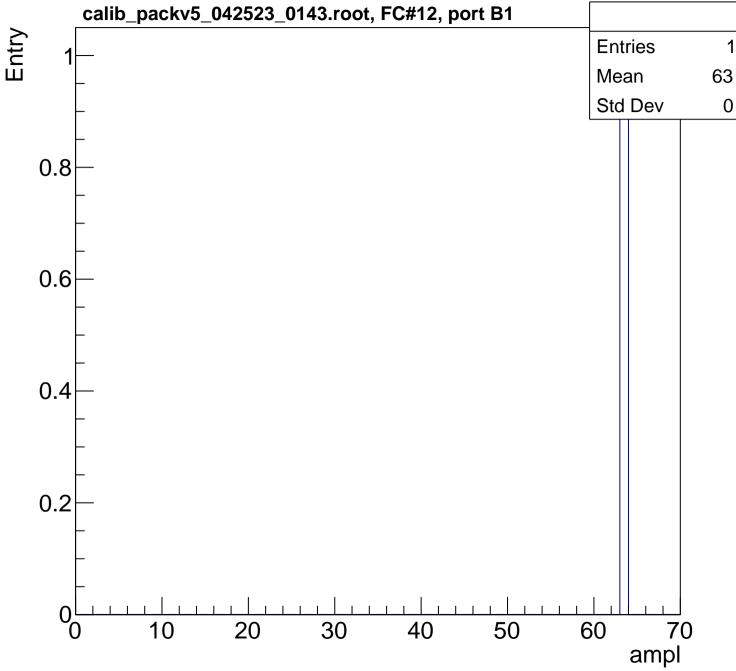


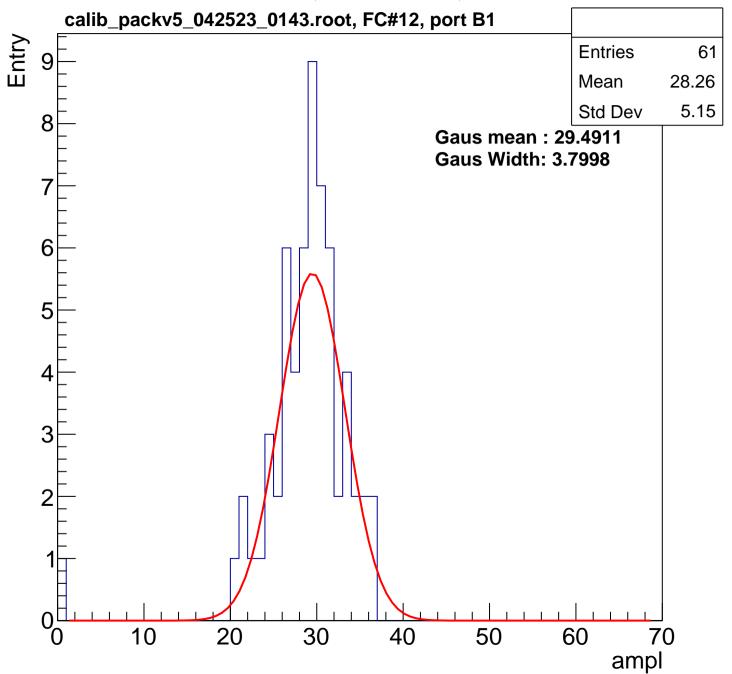


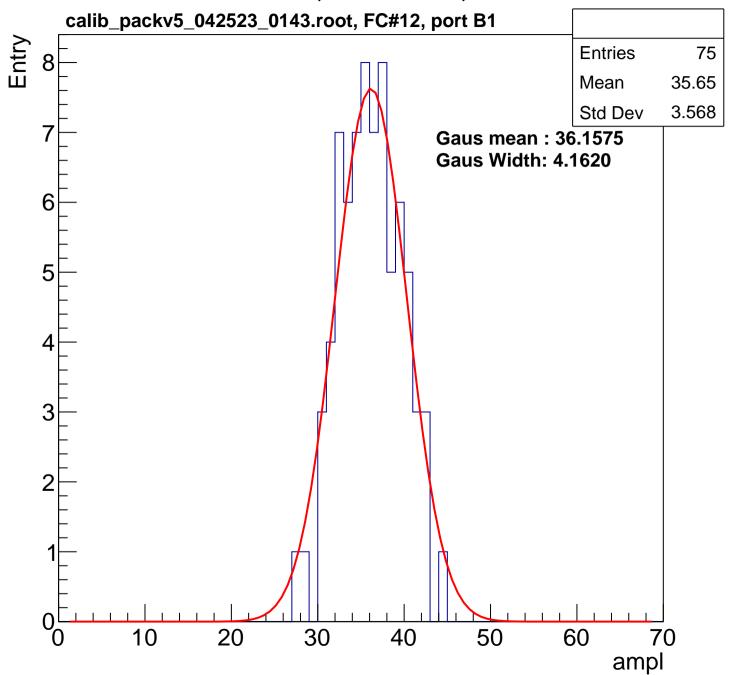


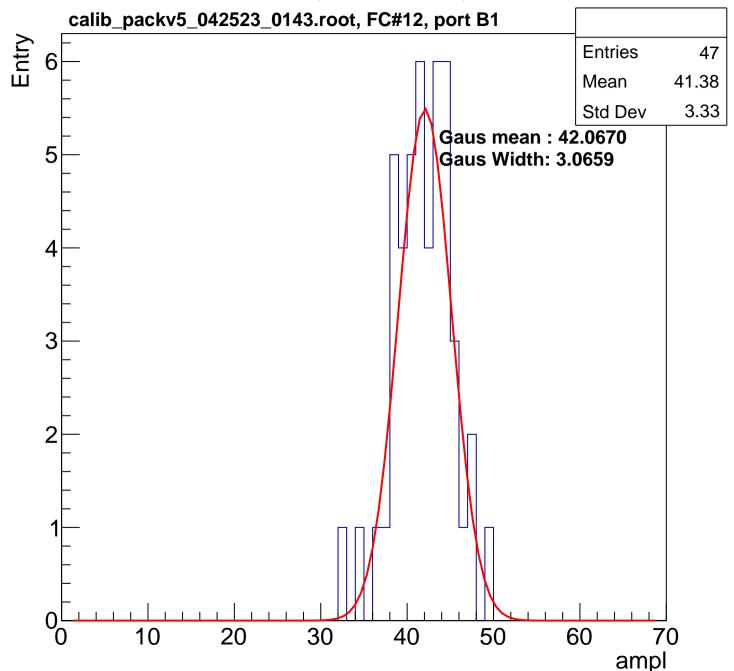


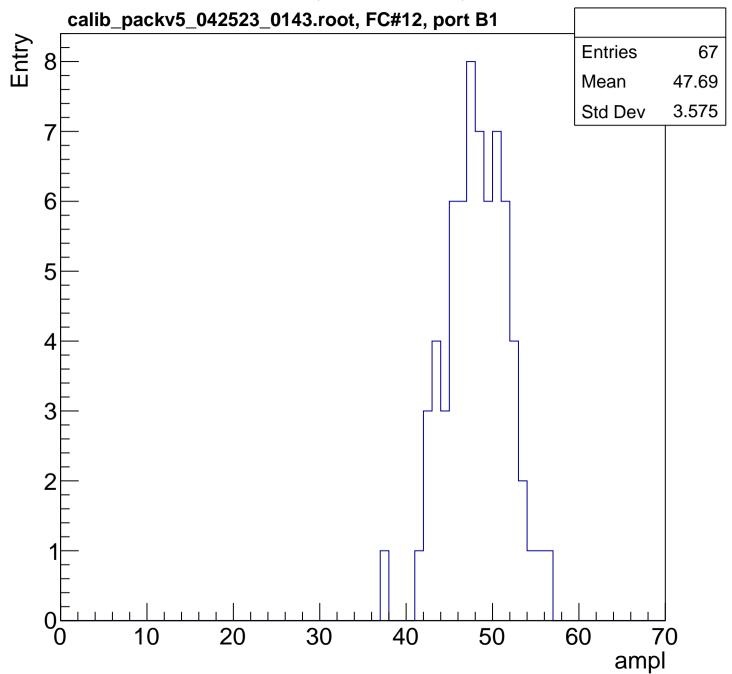
0

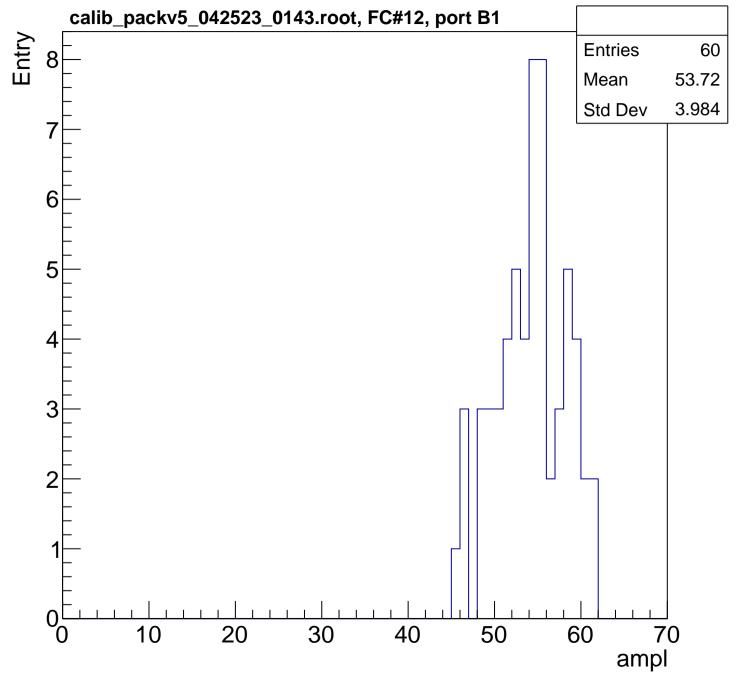


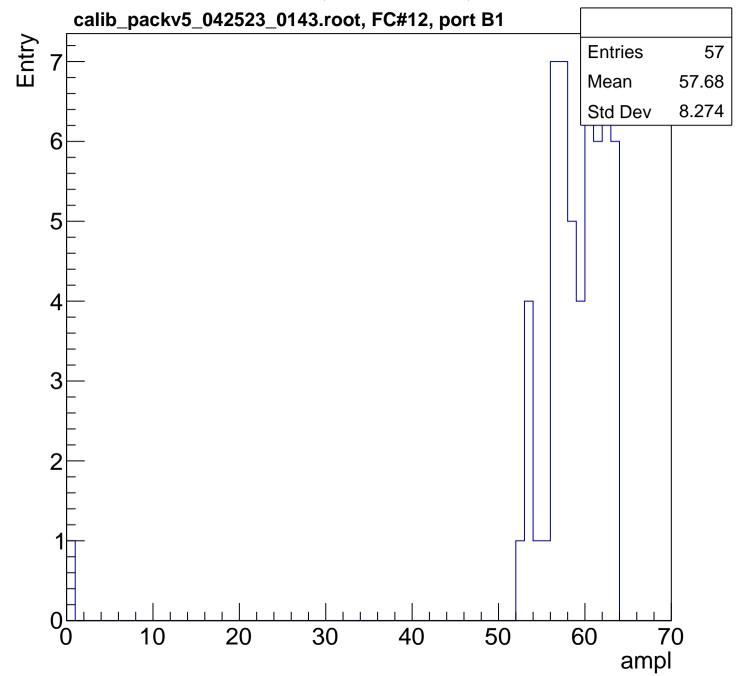


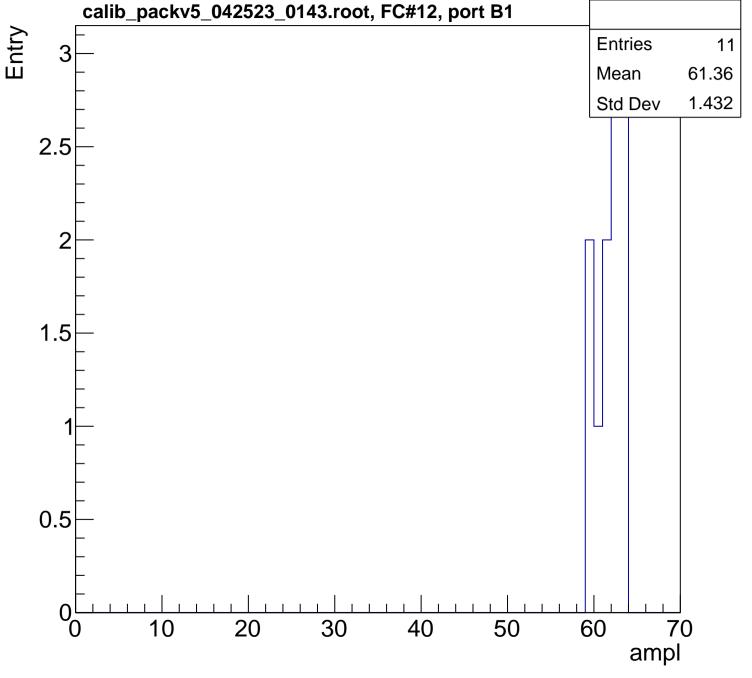




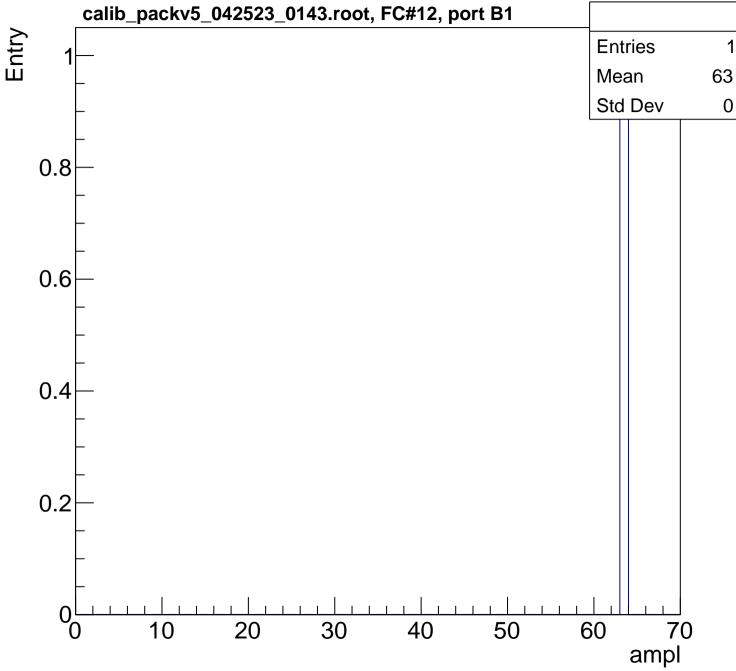


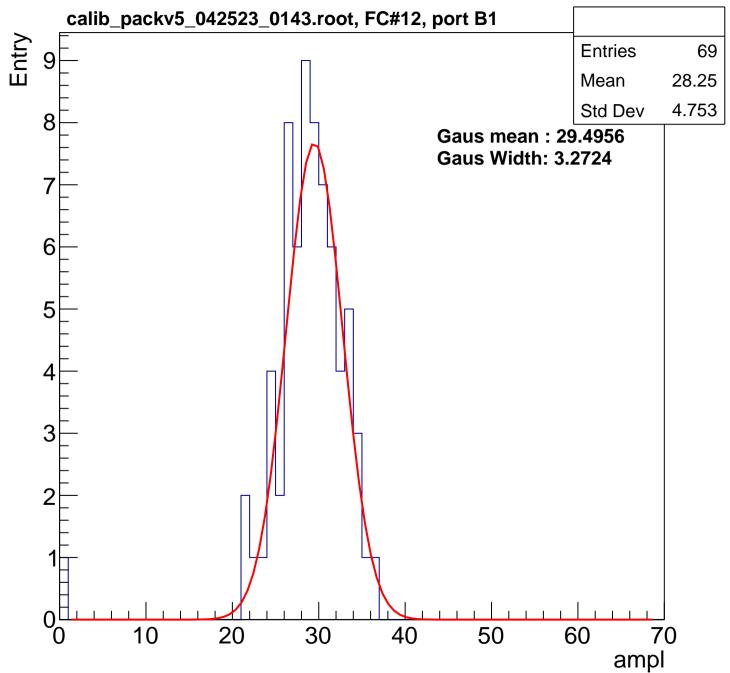


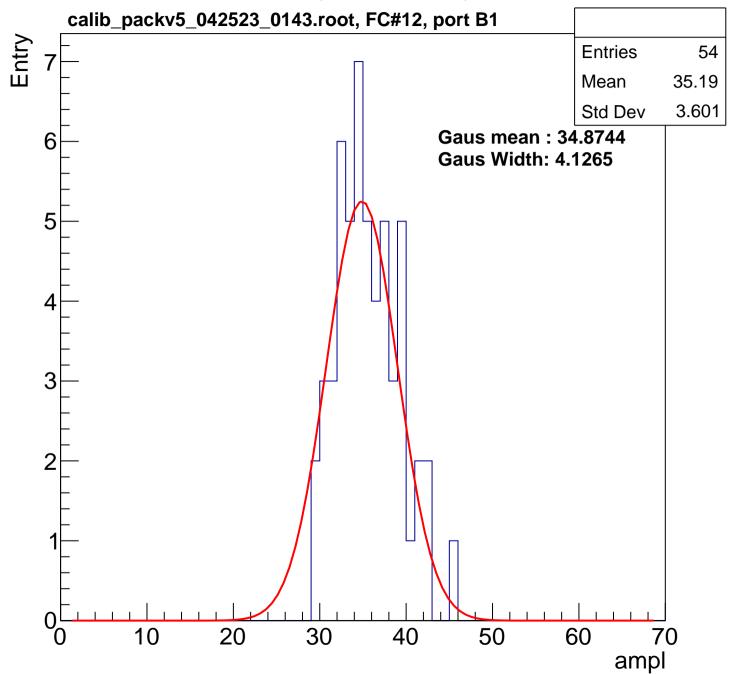


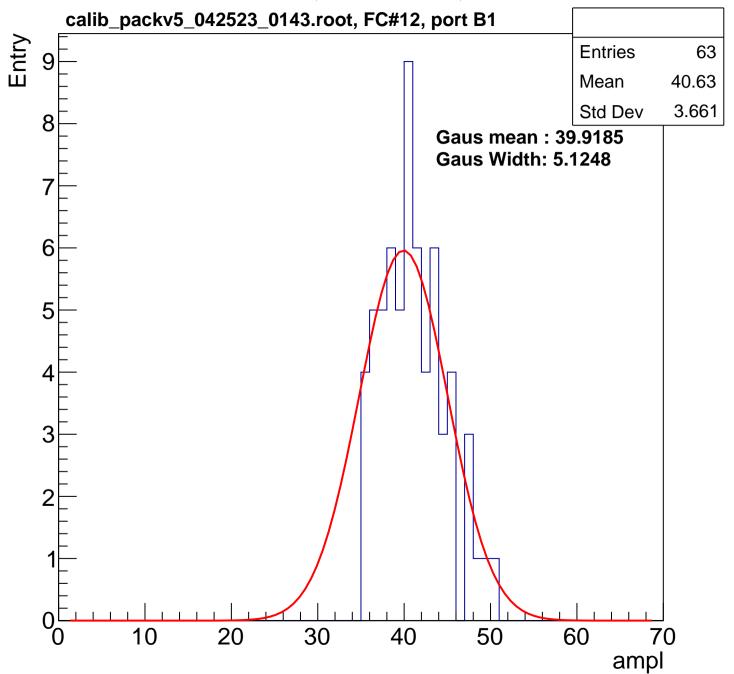


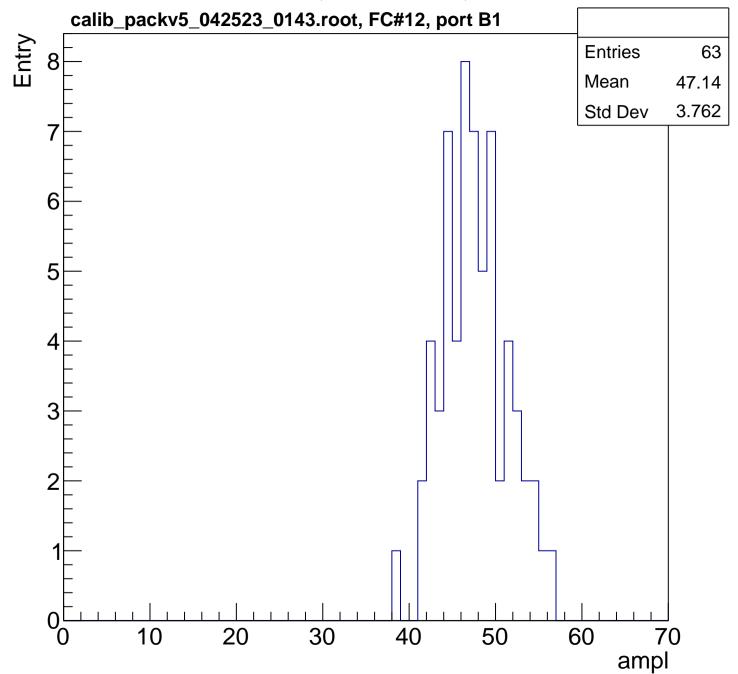
0

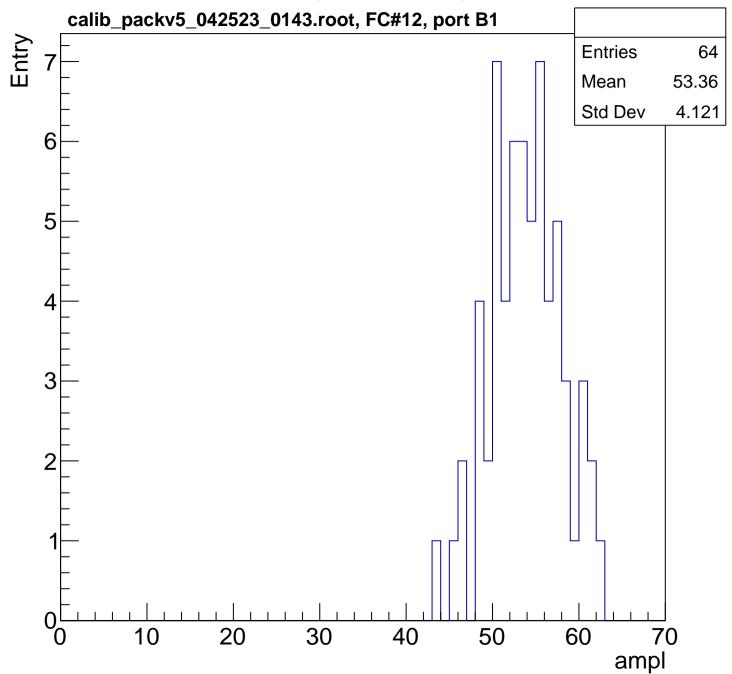


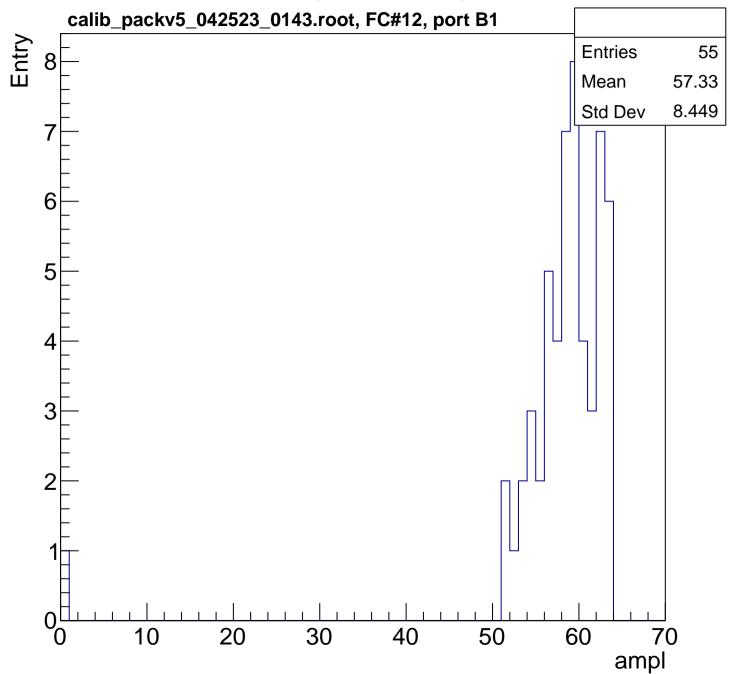


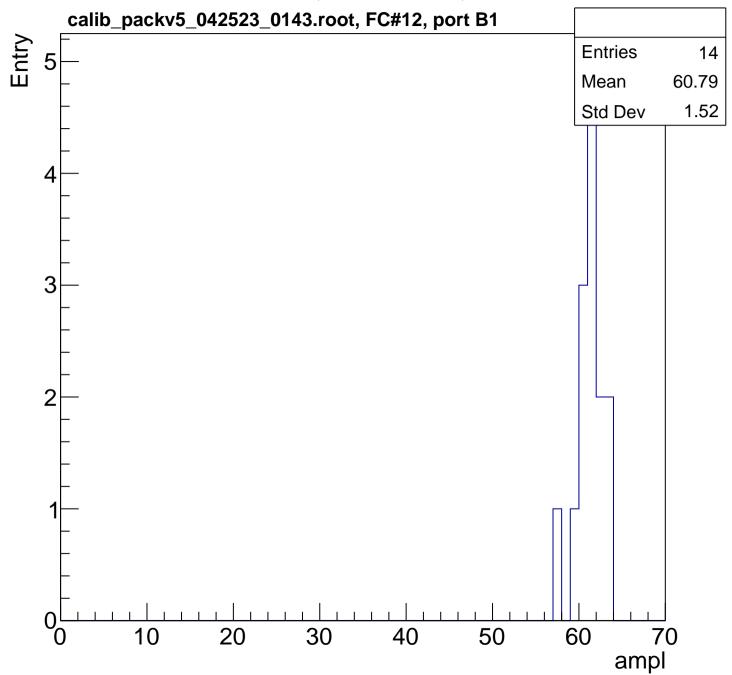


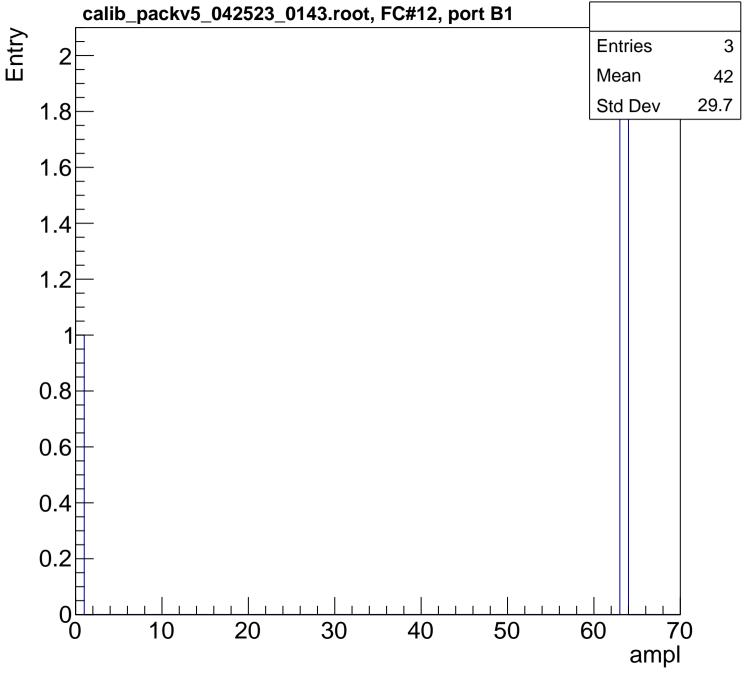


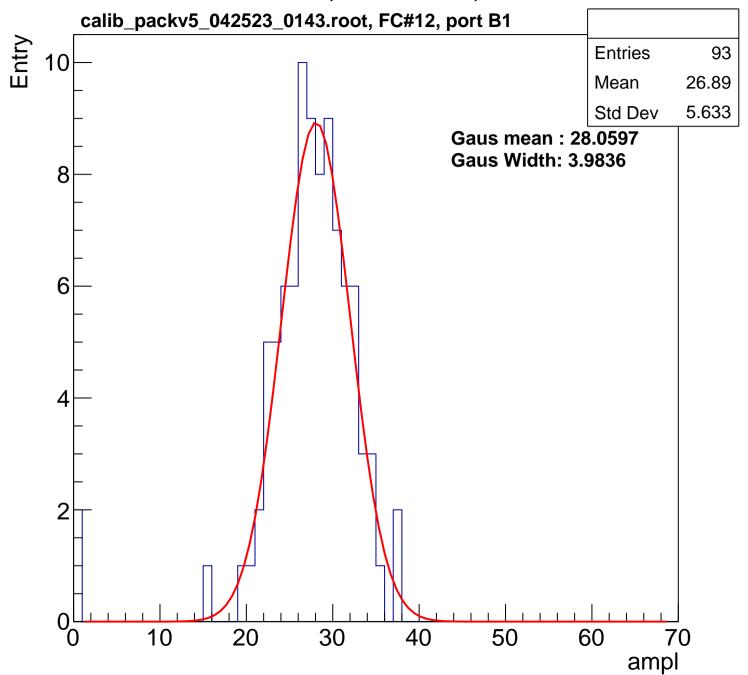


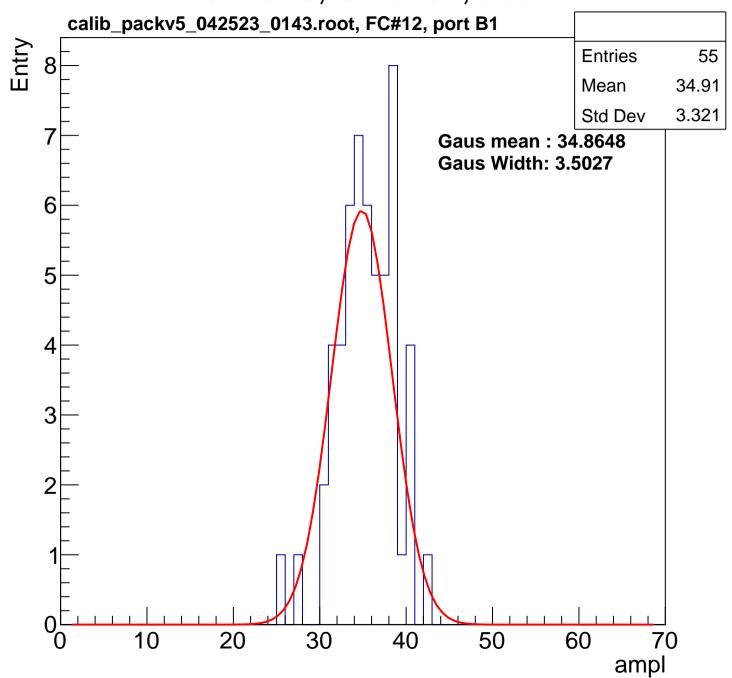


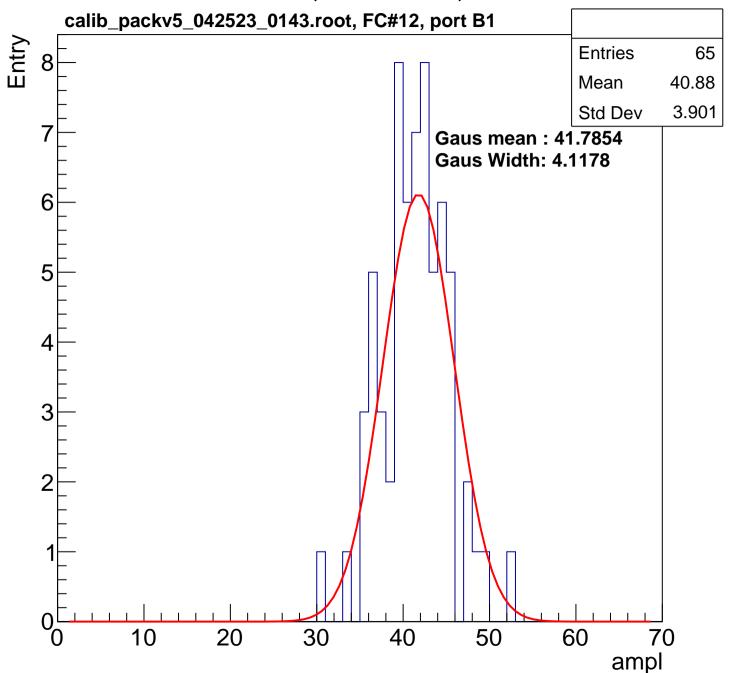


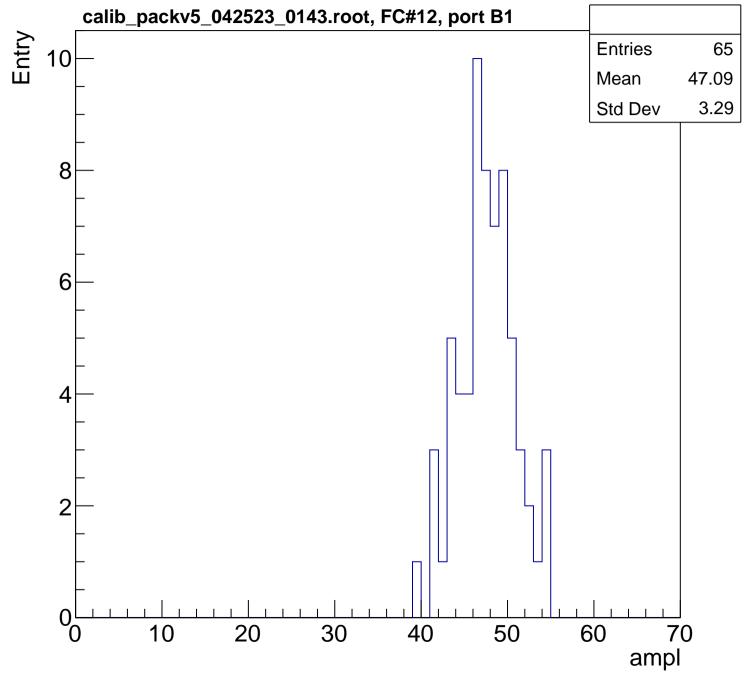


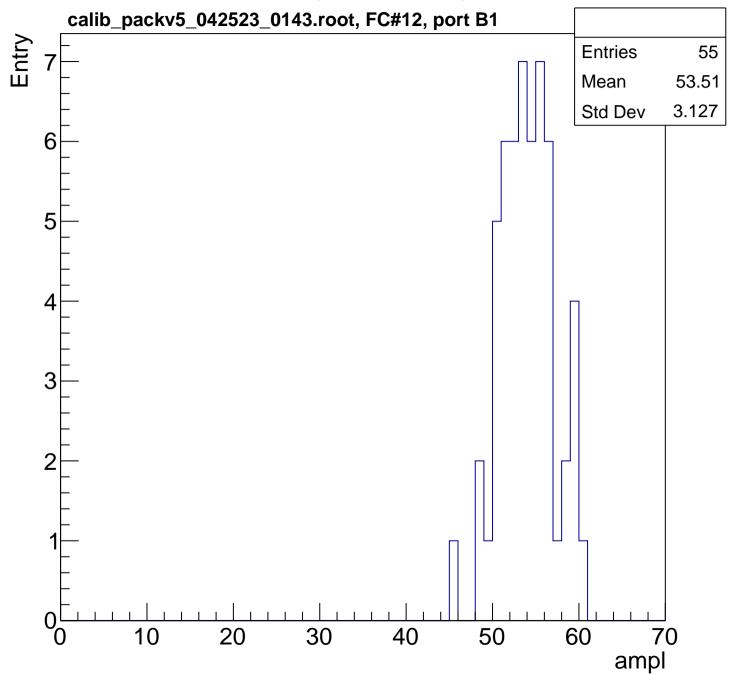


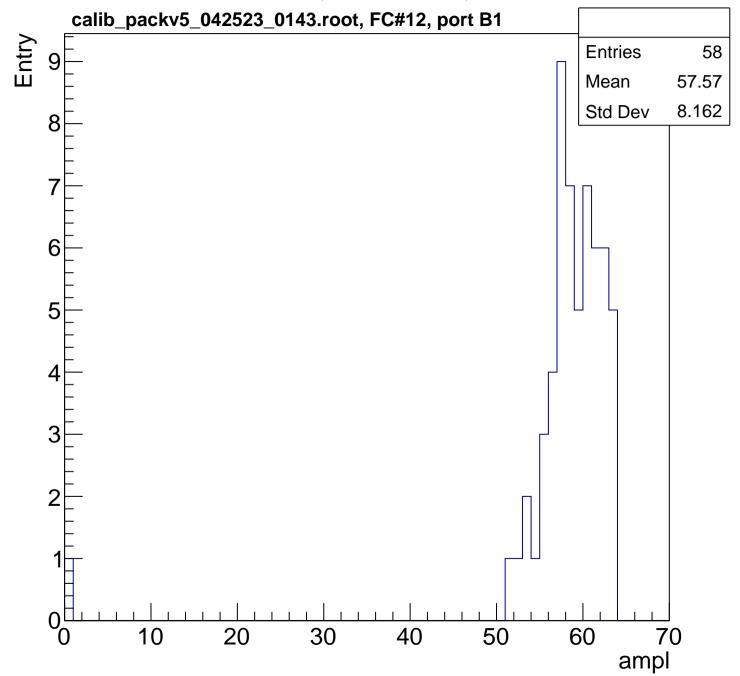


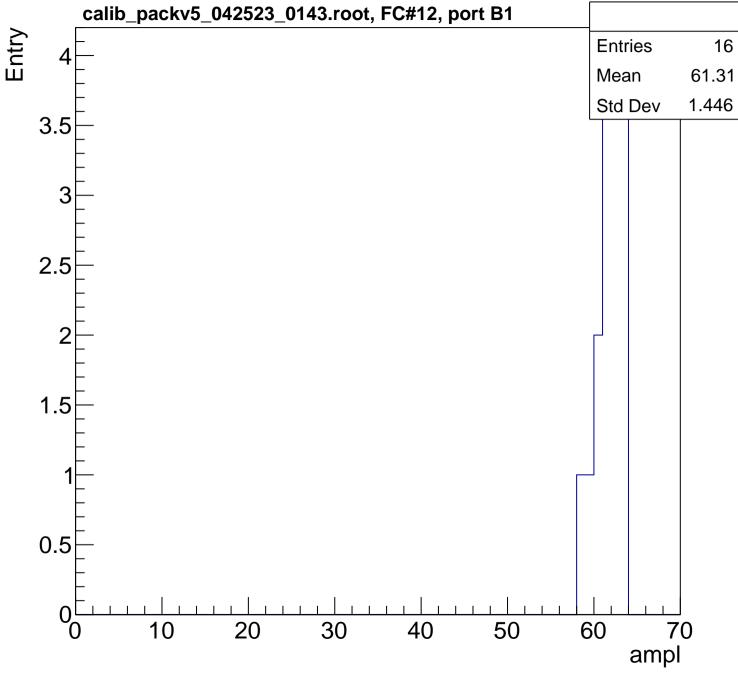


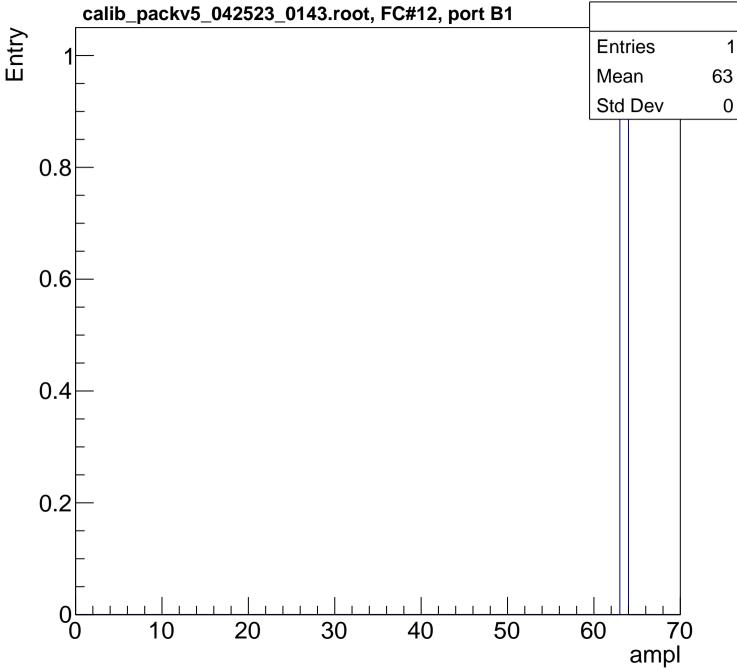


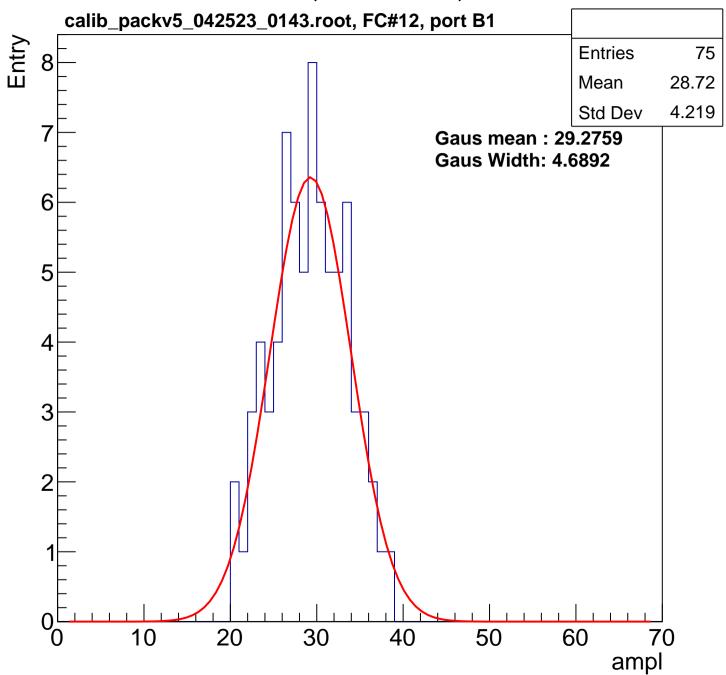


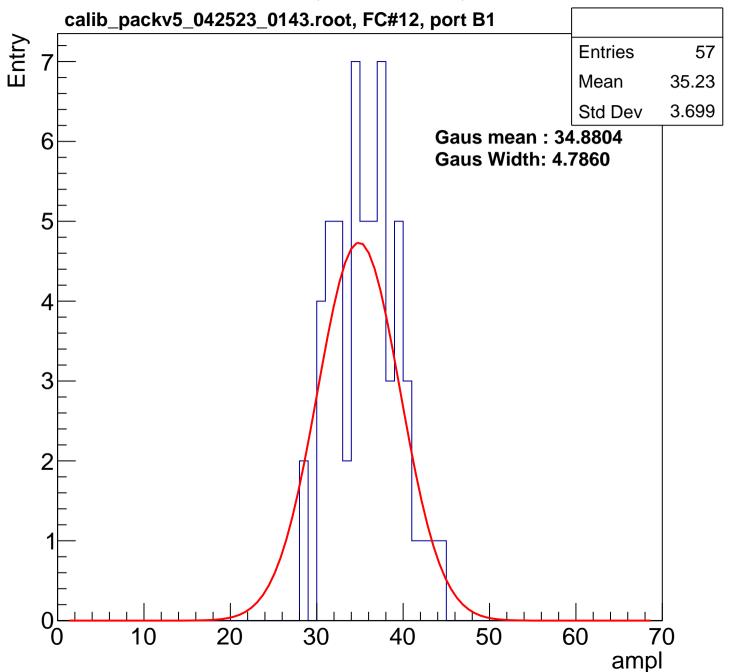


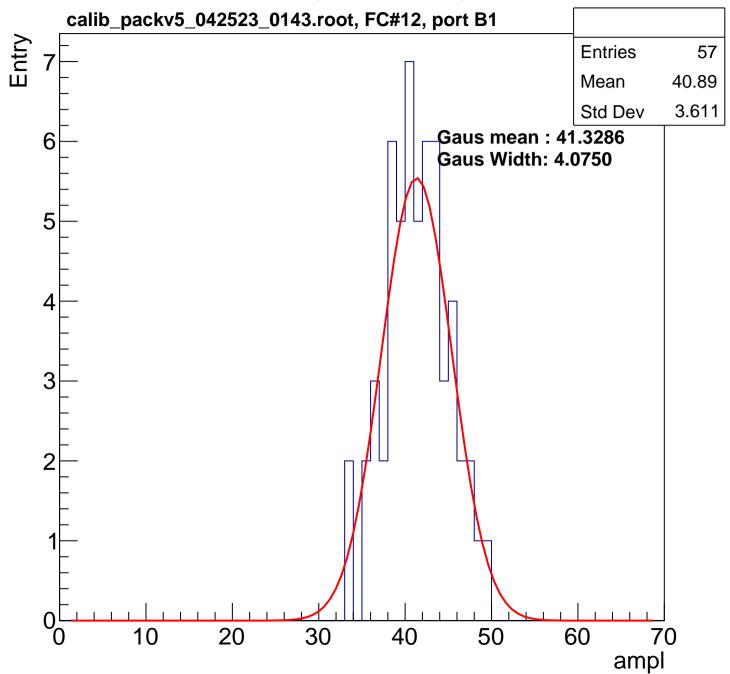


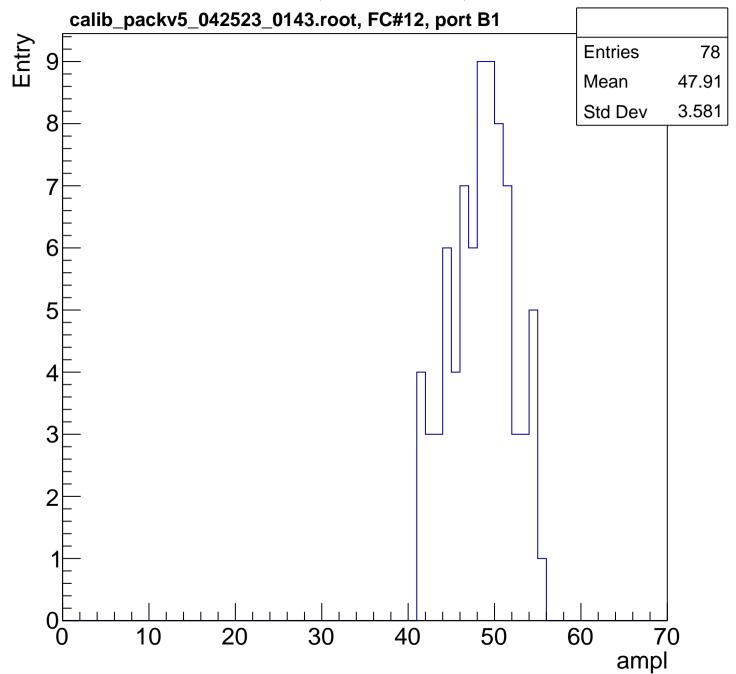


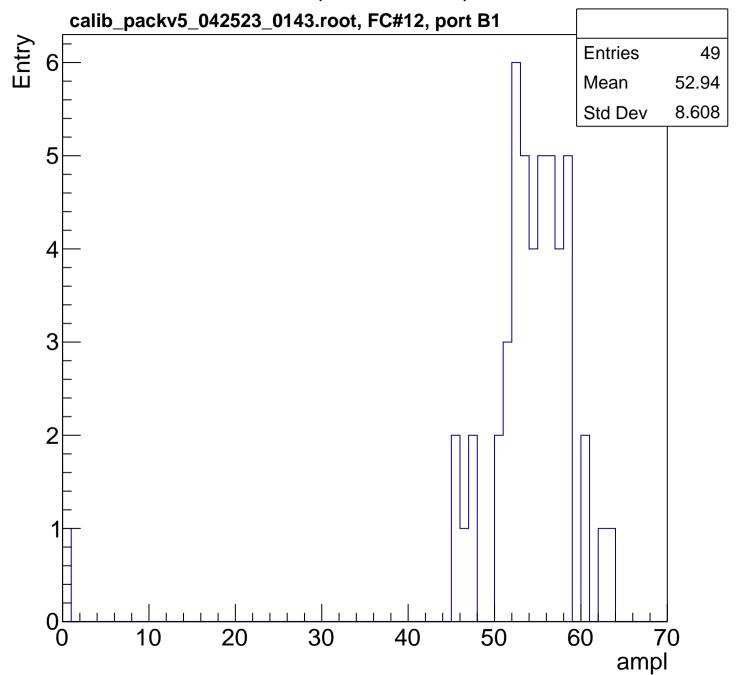


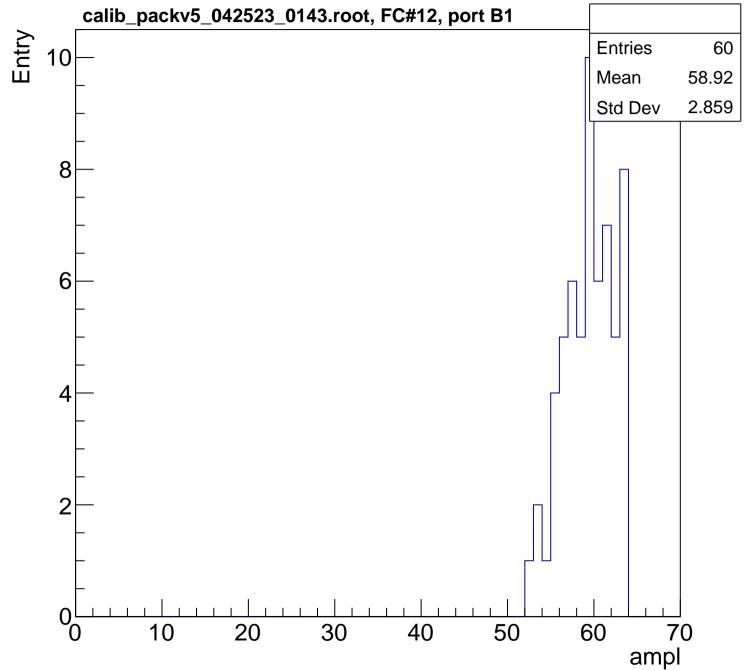


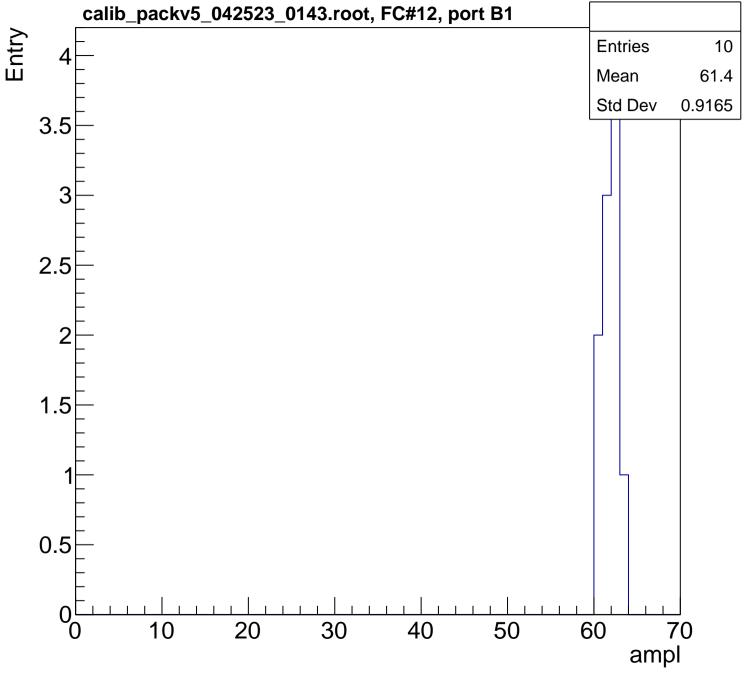


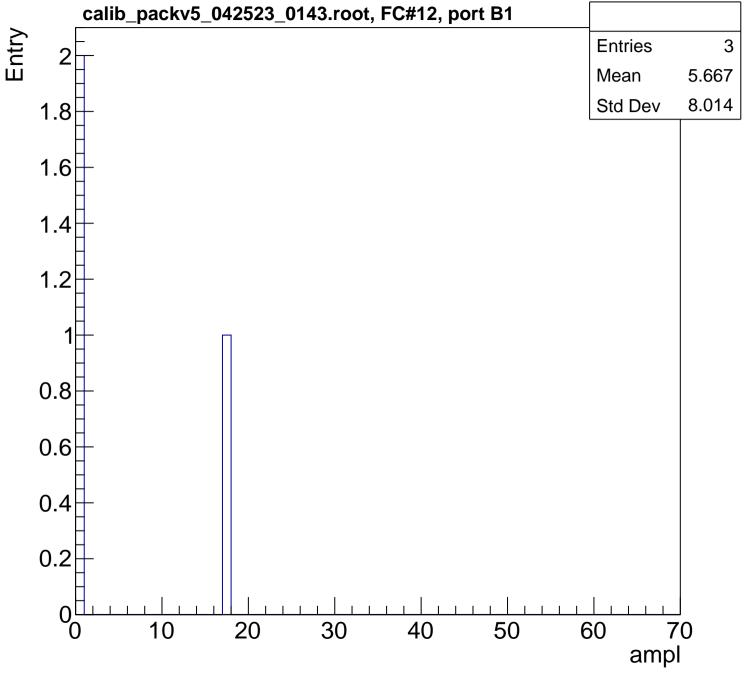


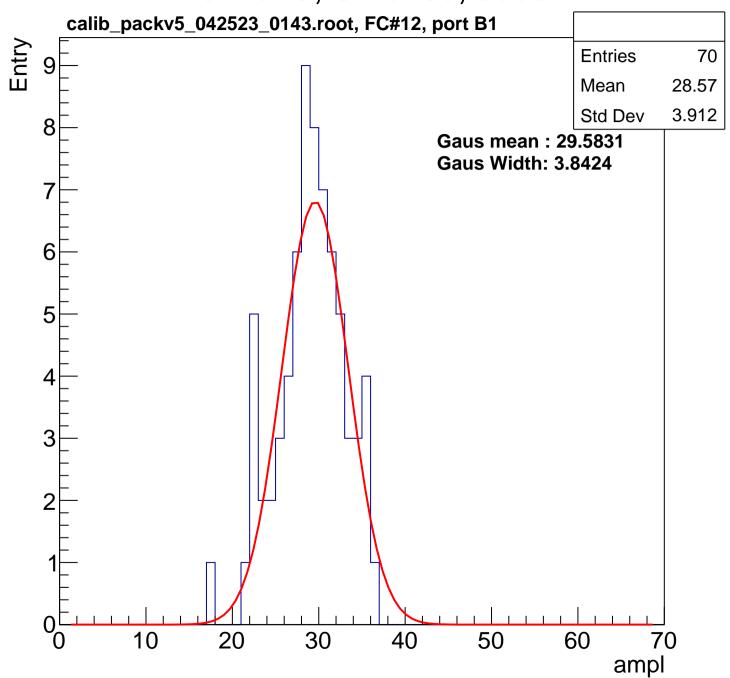


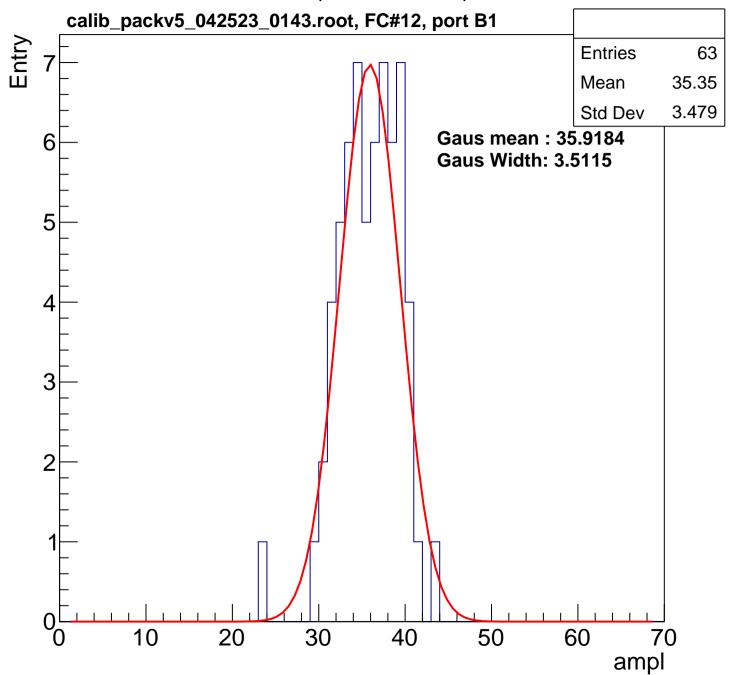


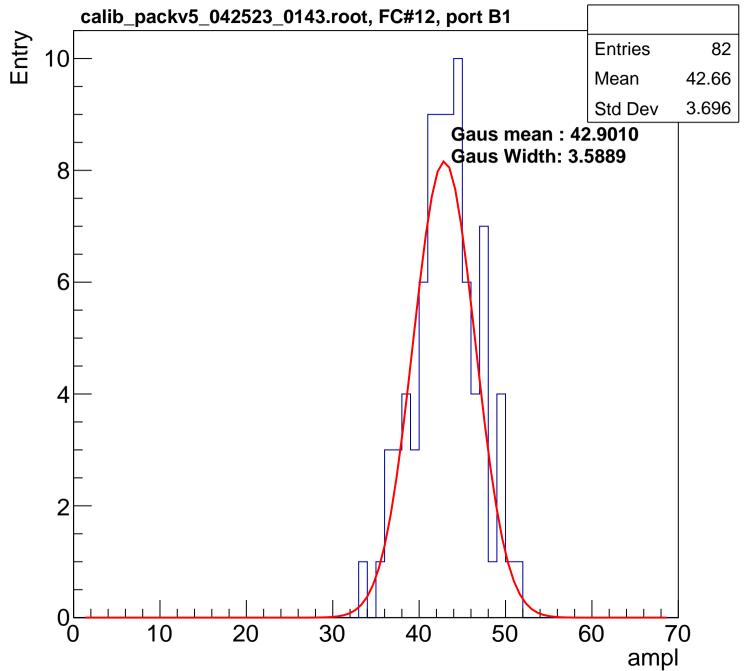


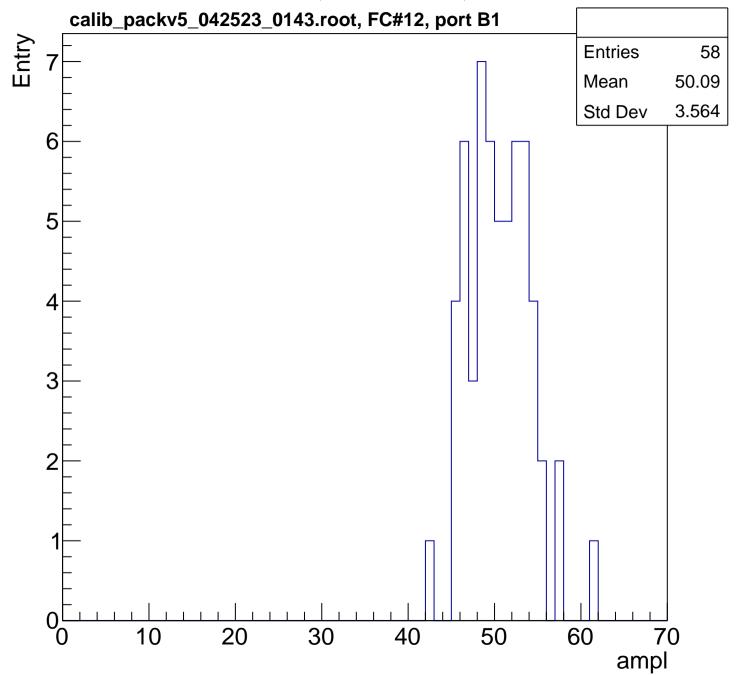


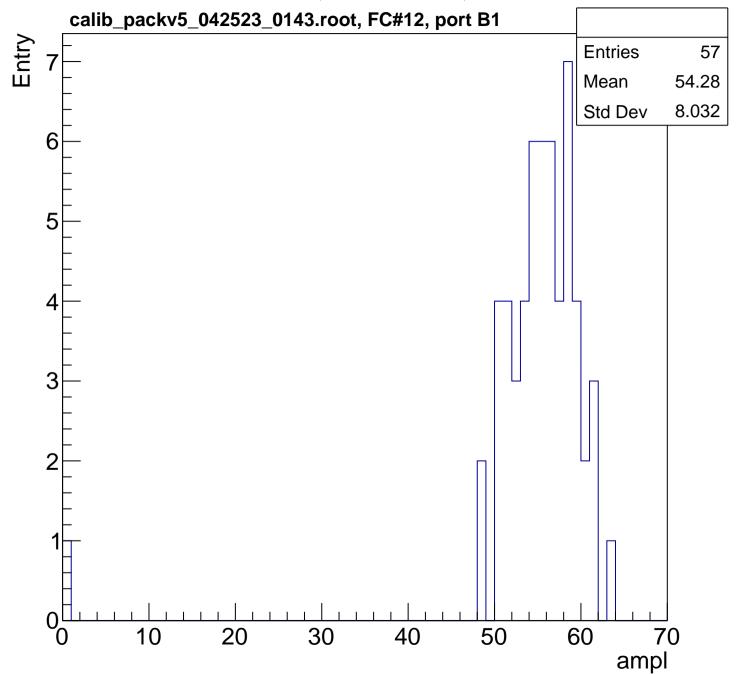


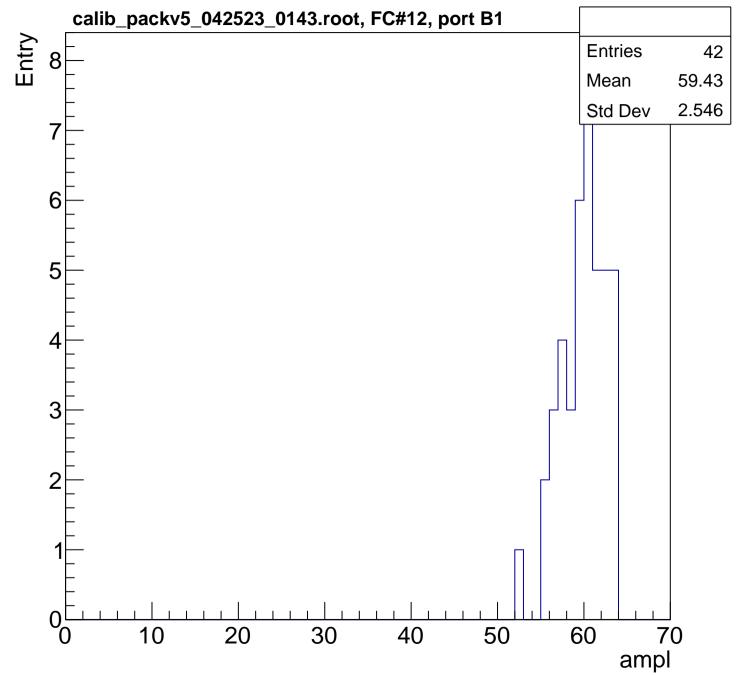


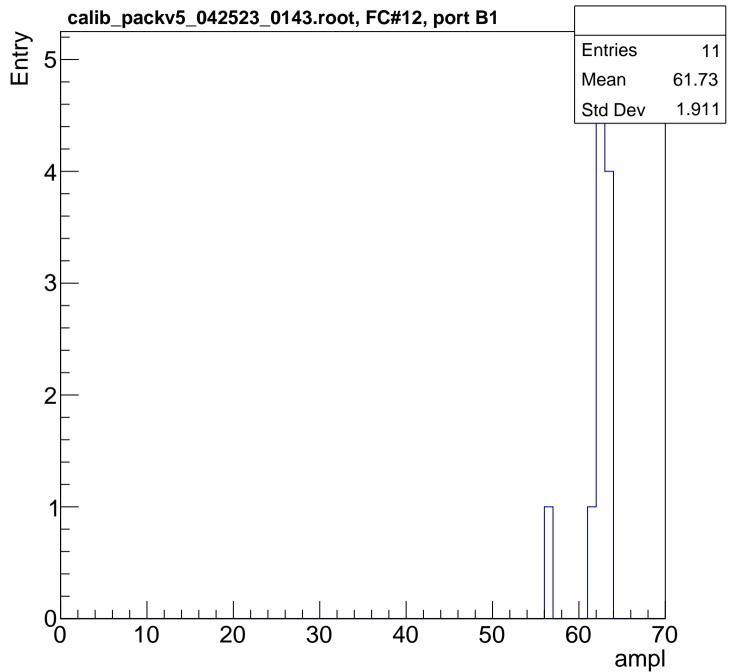




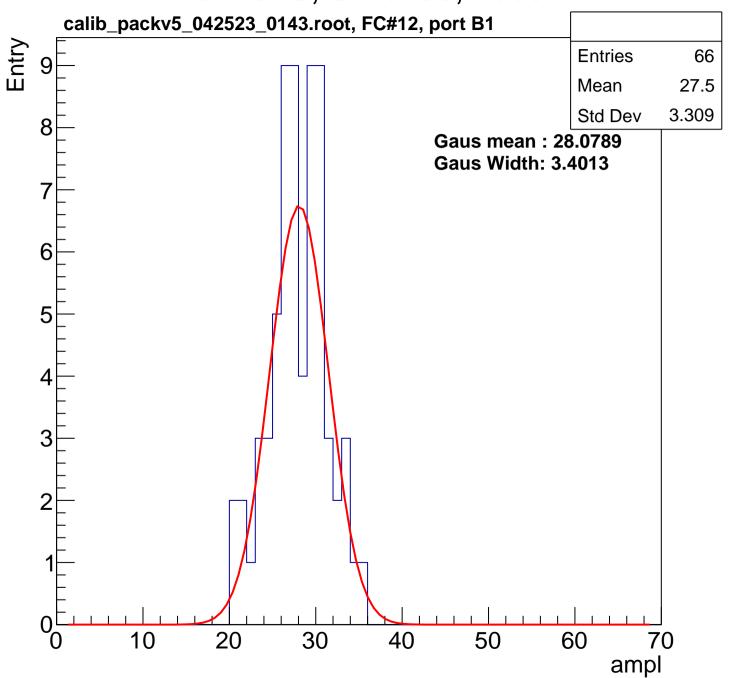


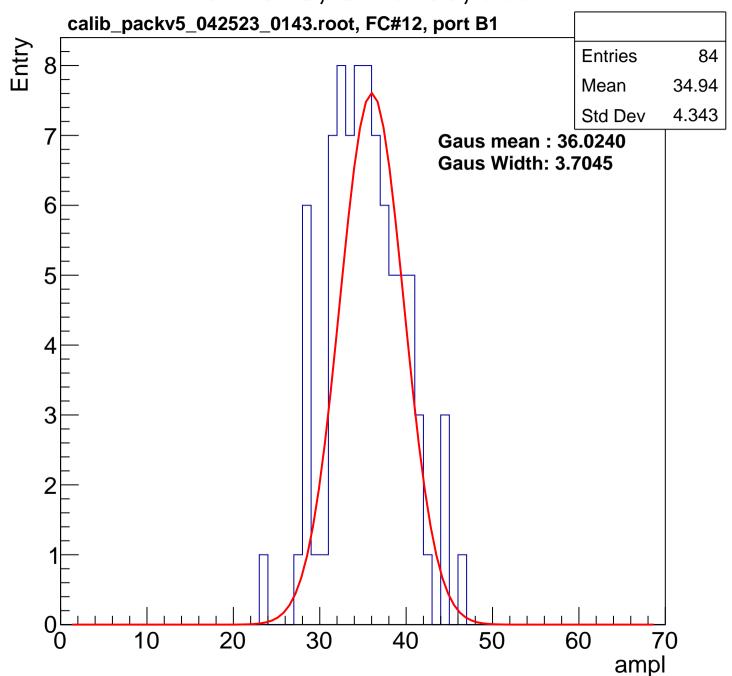


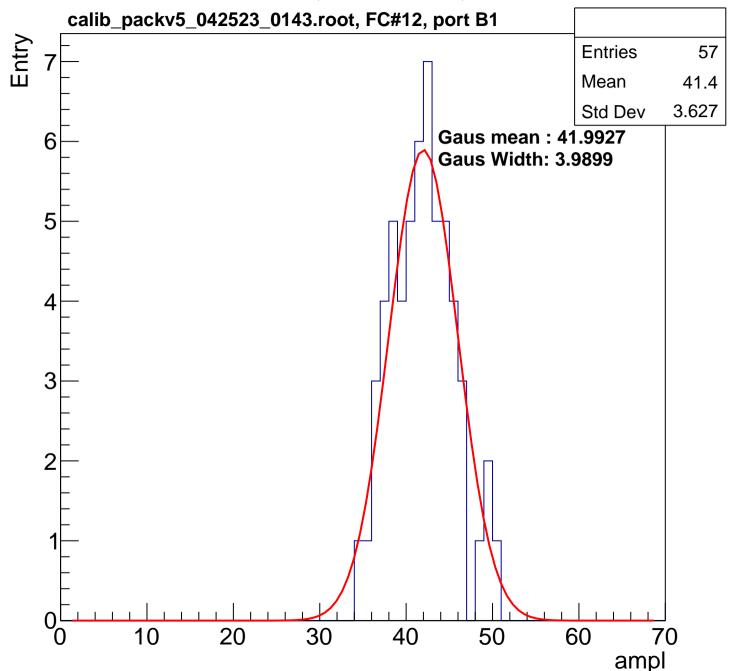


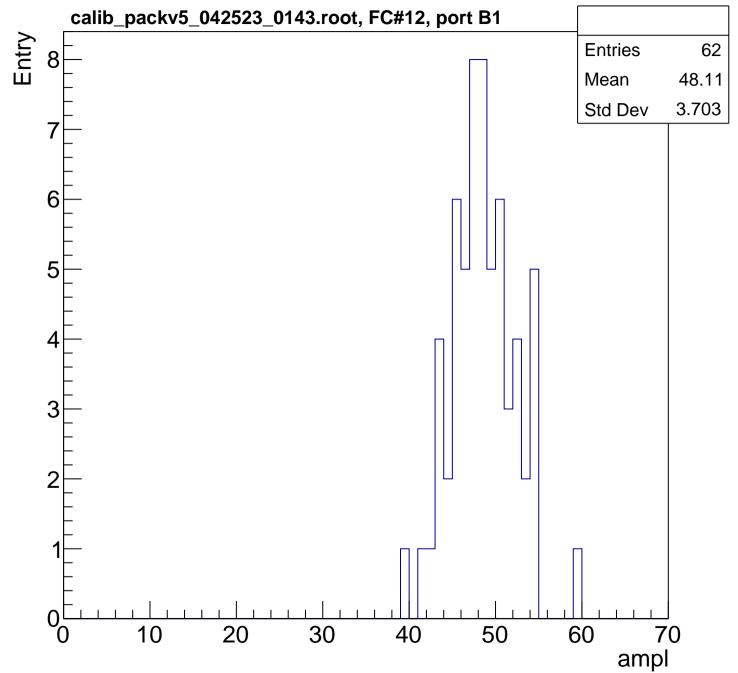


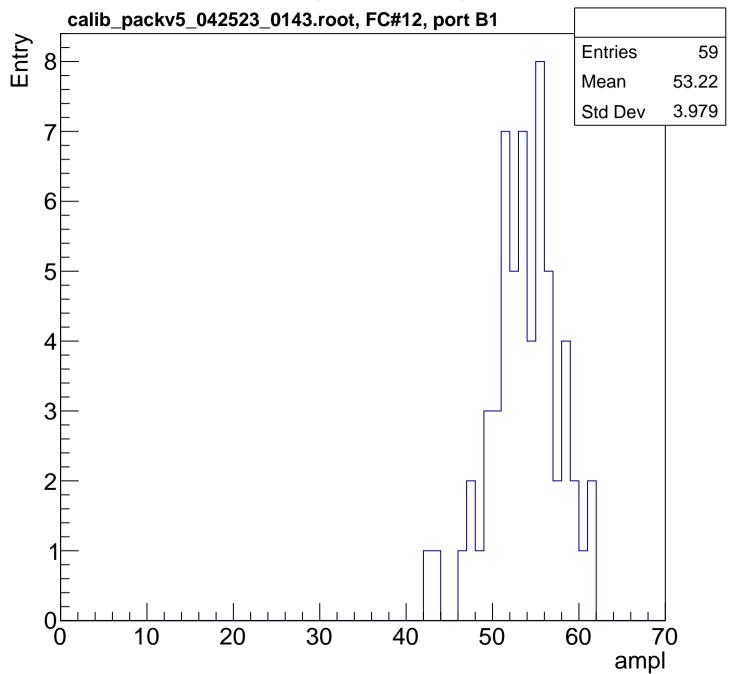
B0L102S, U4-ch89, adc7 calib_packv5_042523_0143.root, FC#12, port B1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

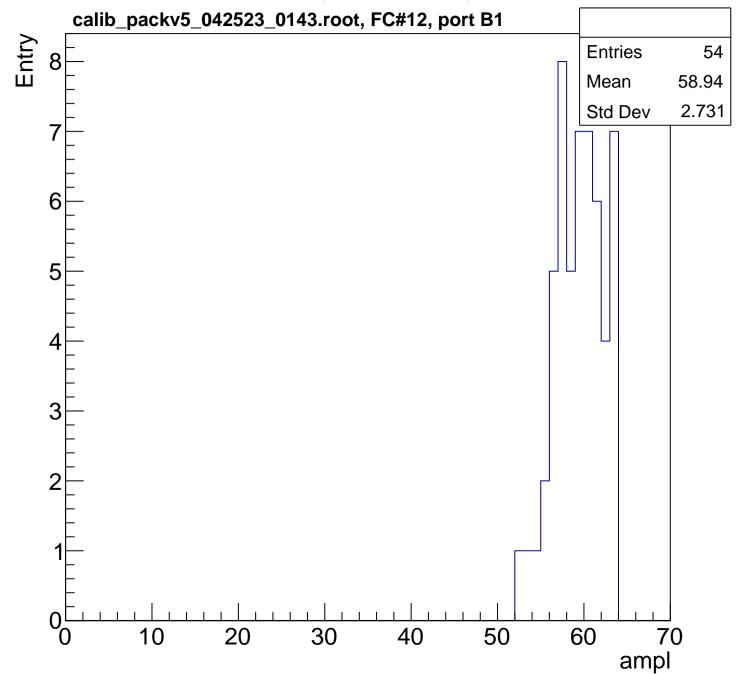


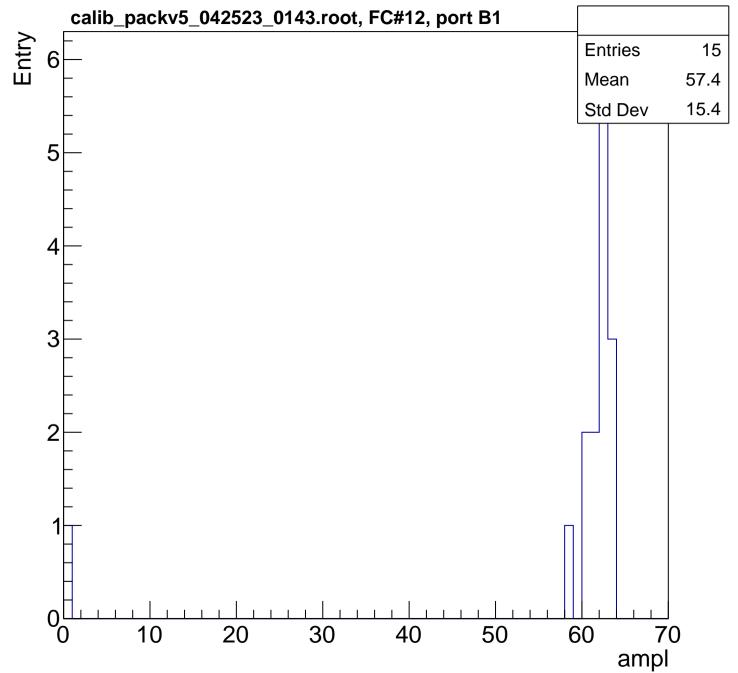


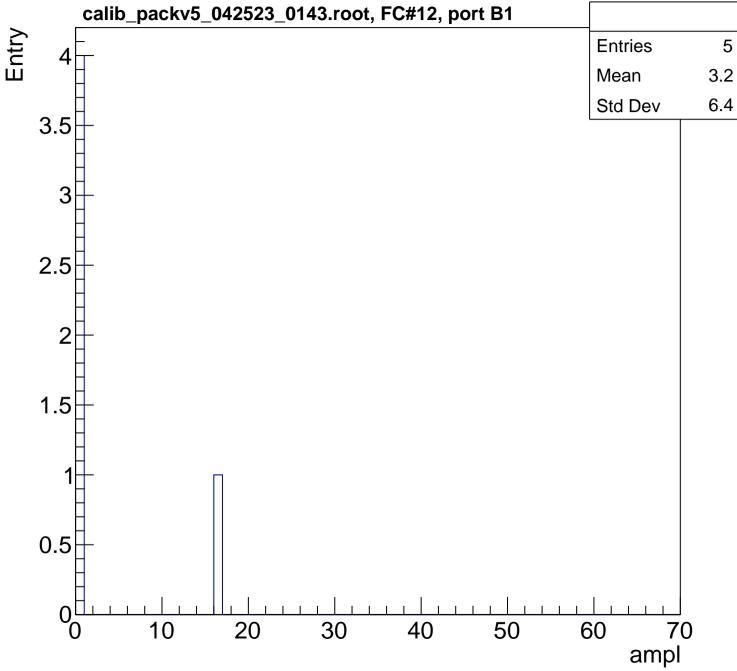


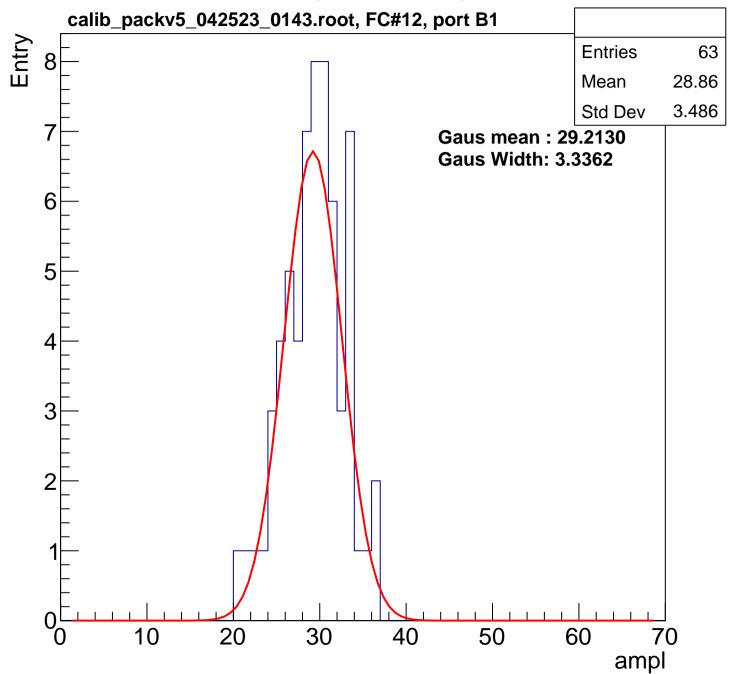


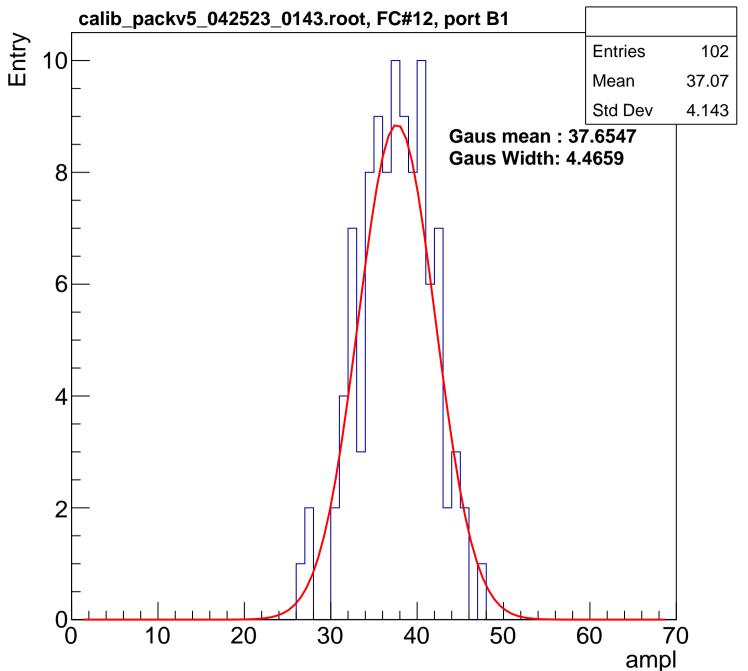


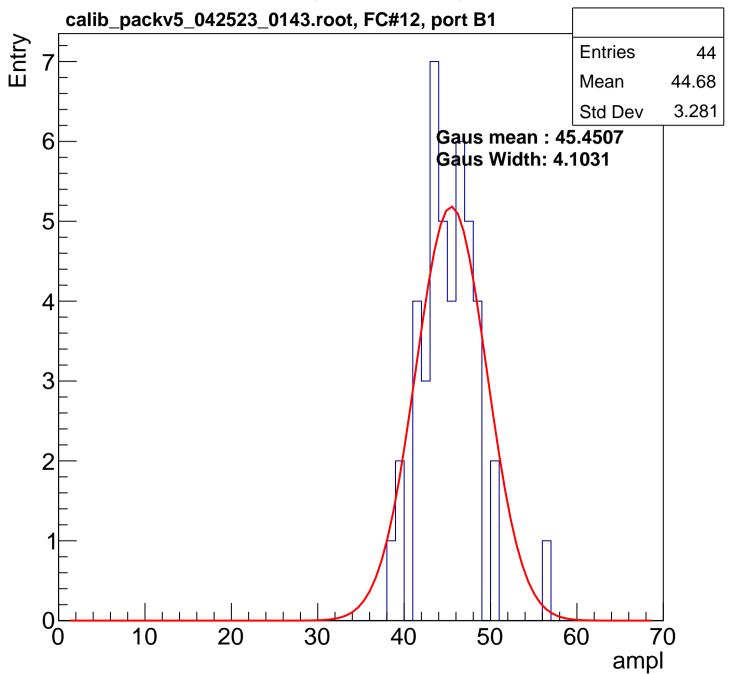


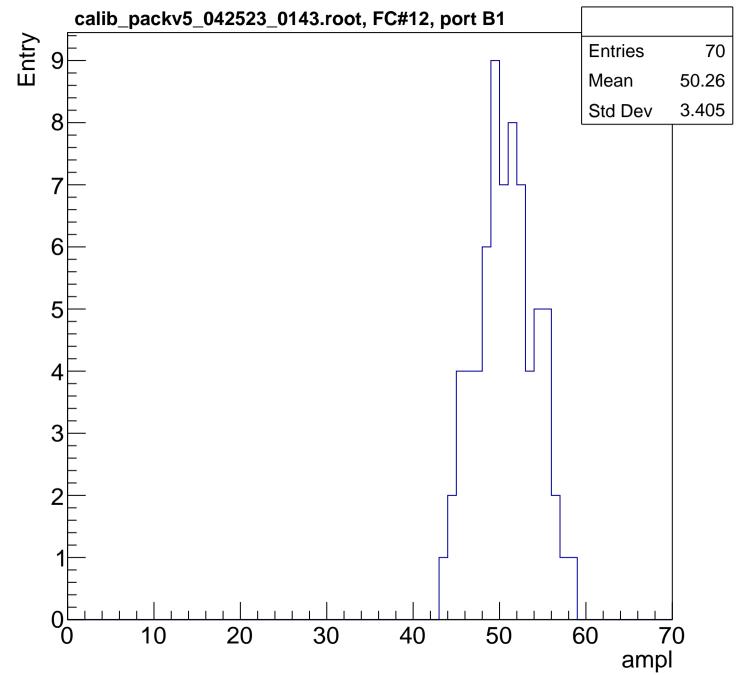


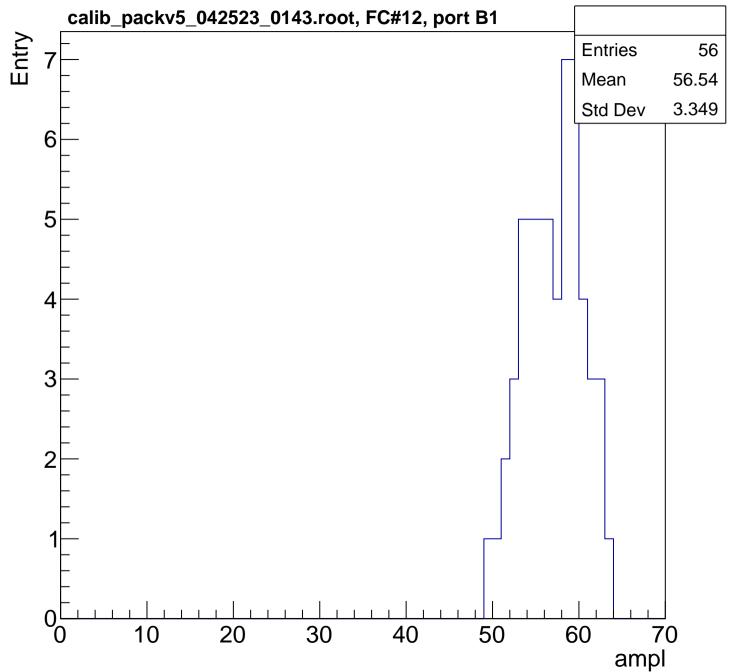


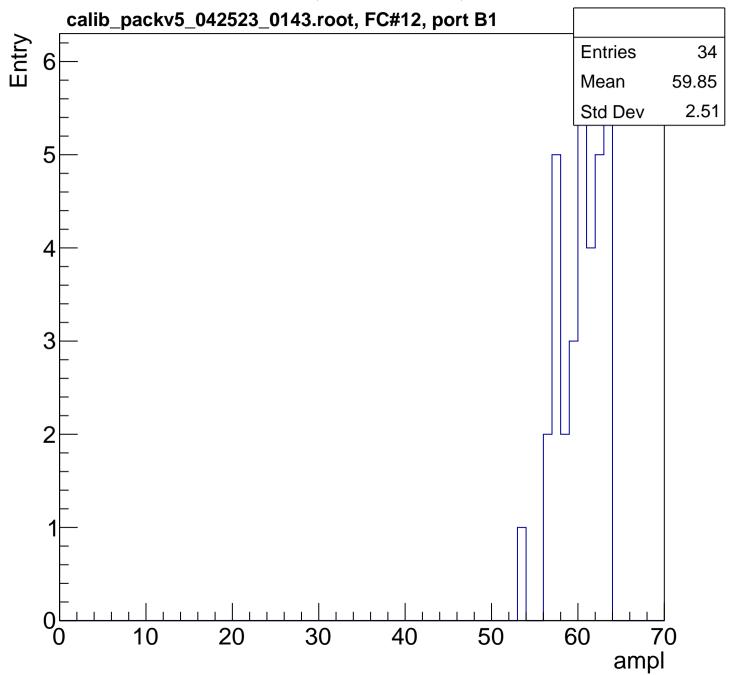


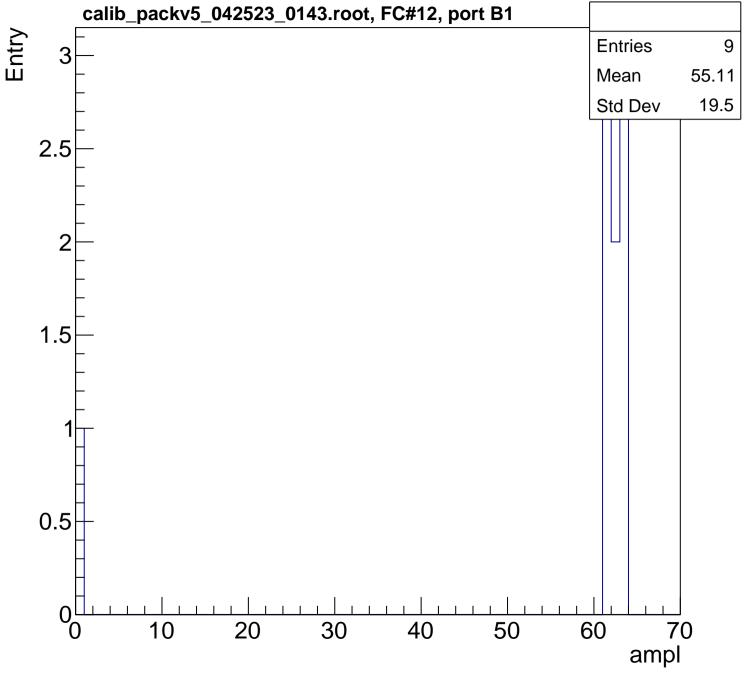


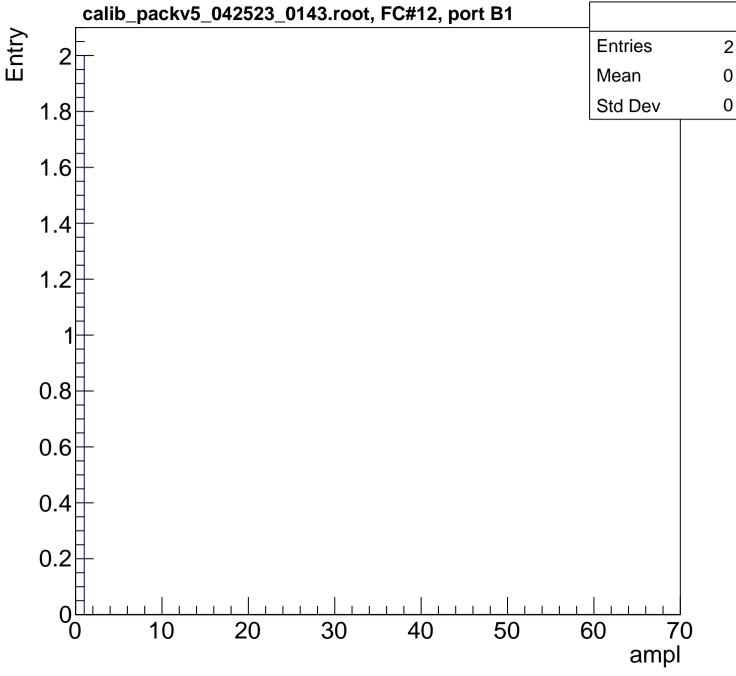


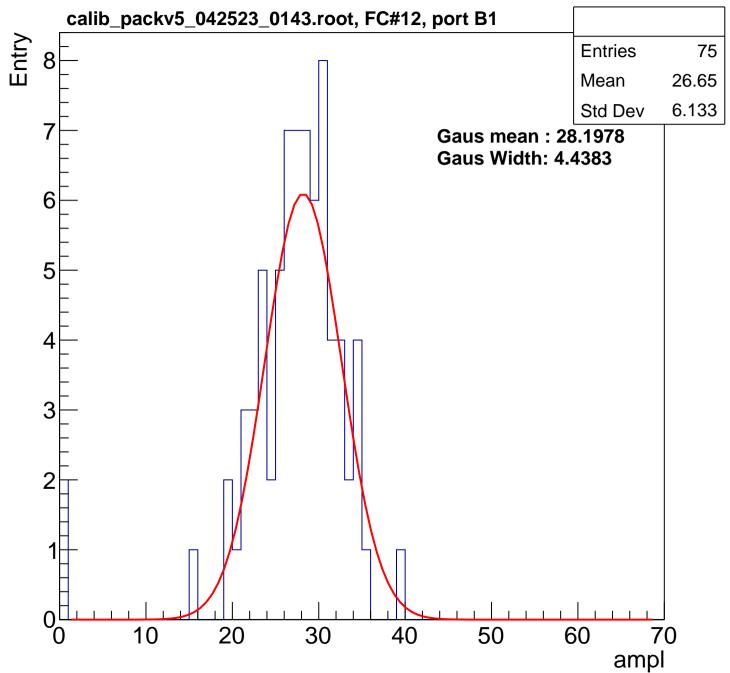


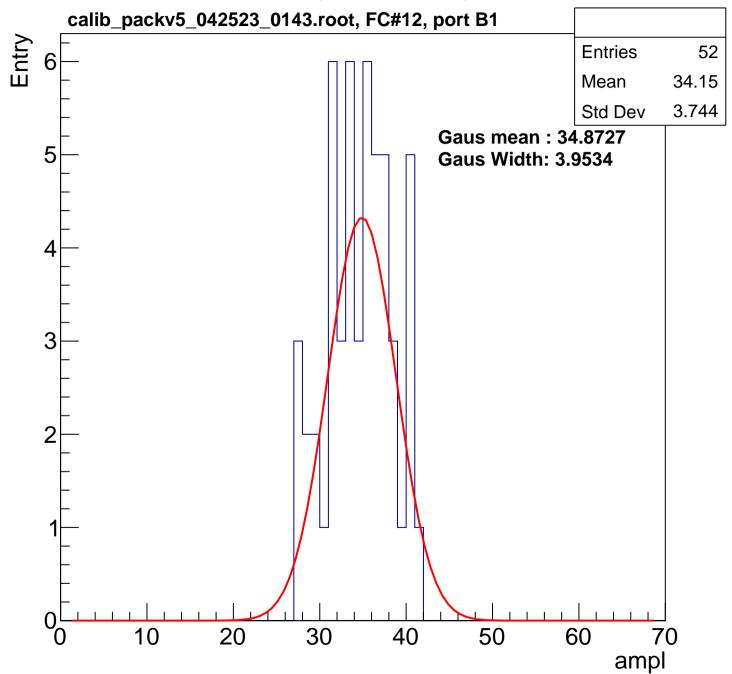


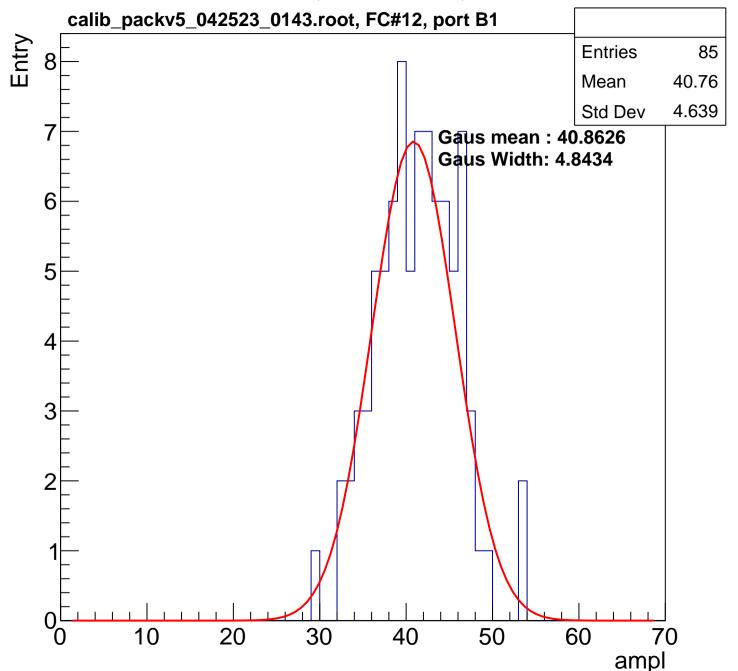


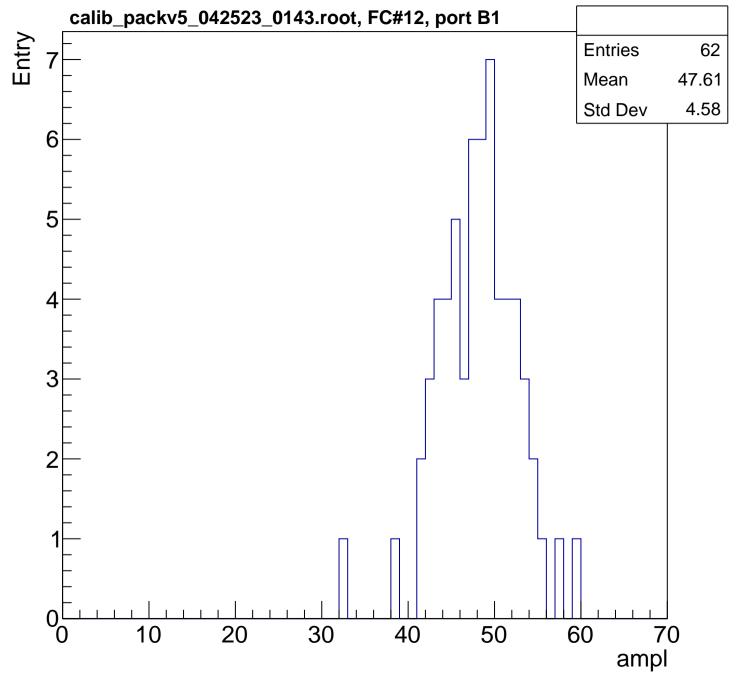


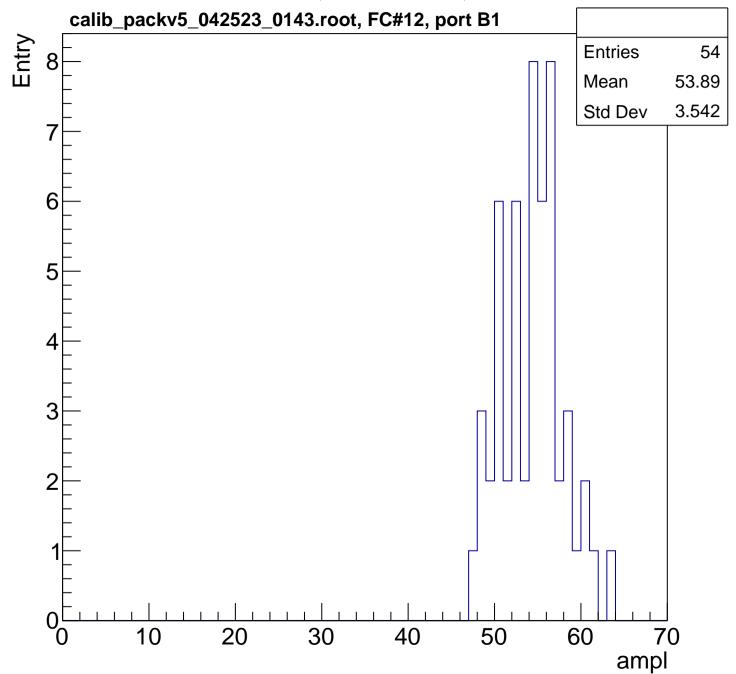


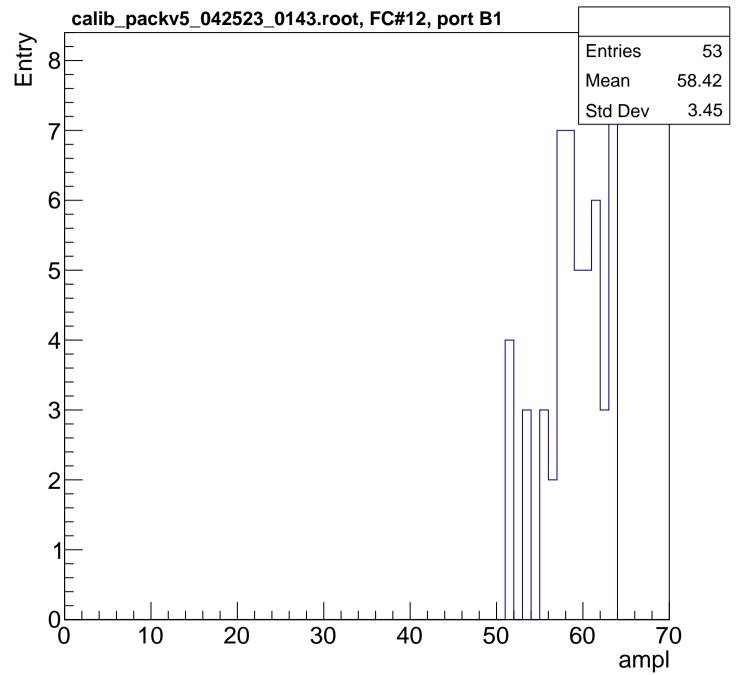


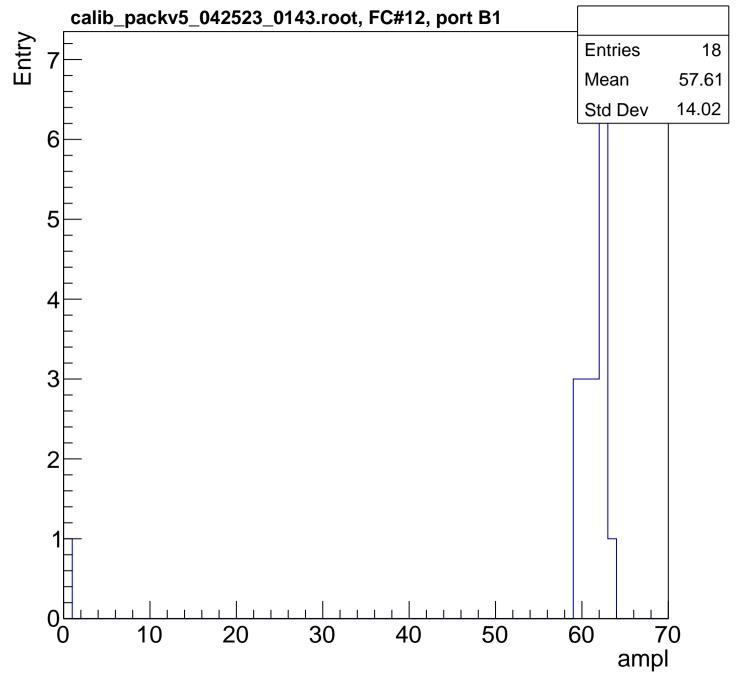




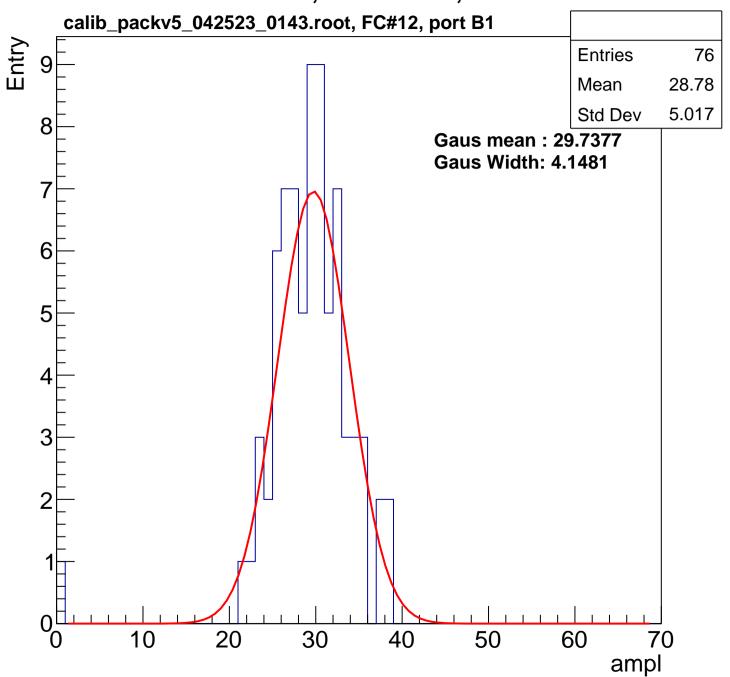


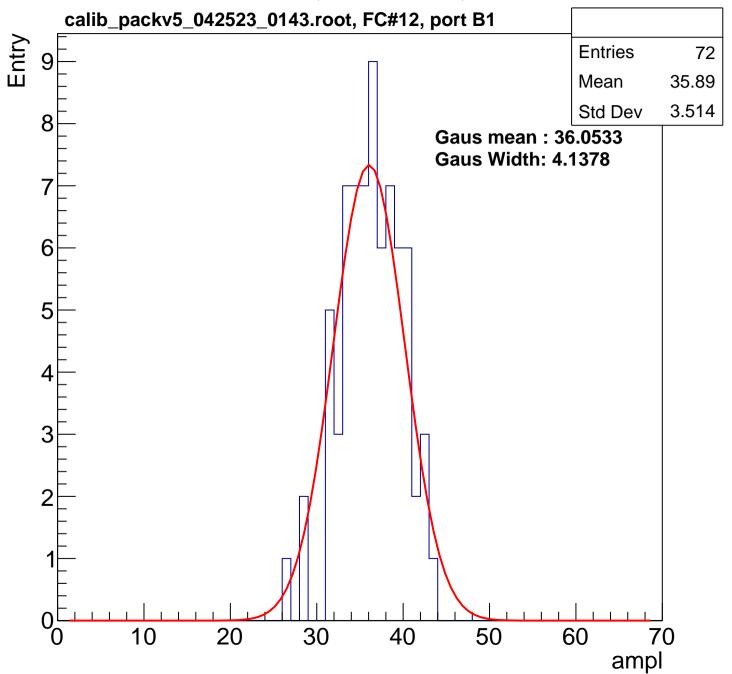


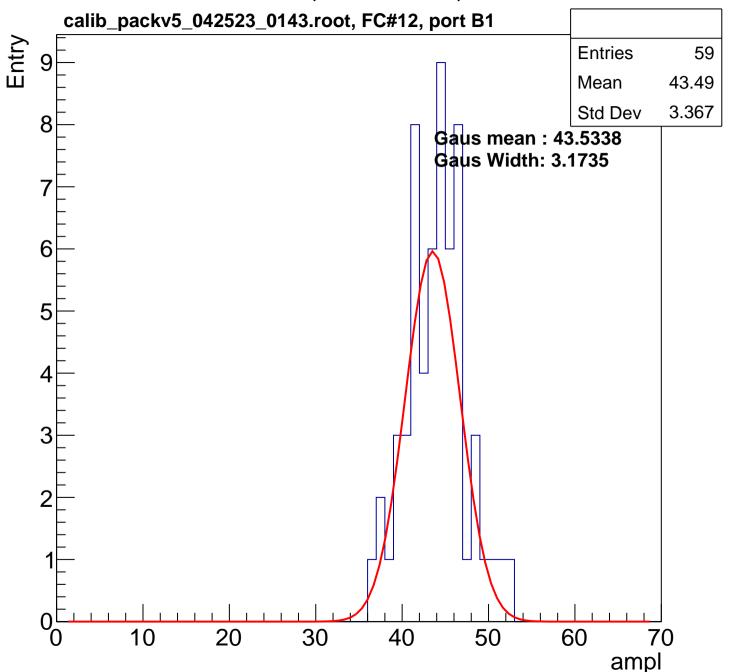


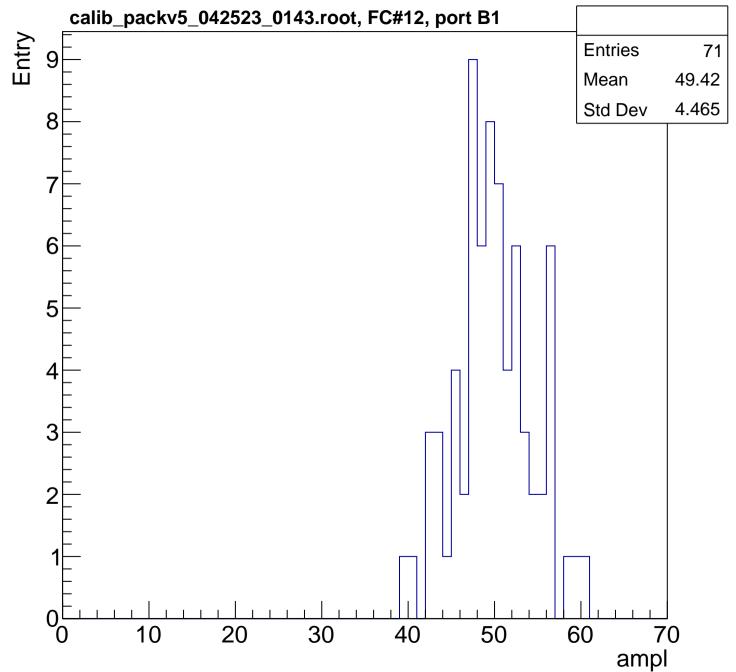


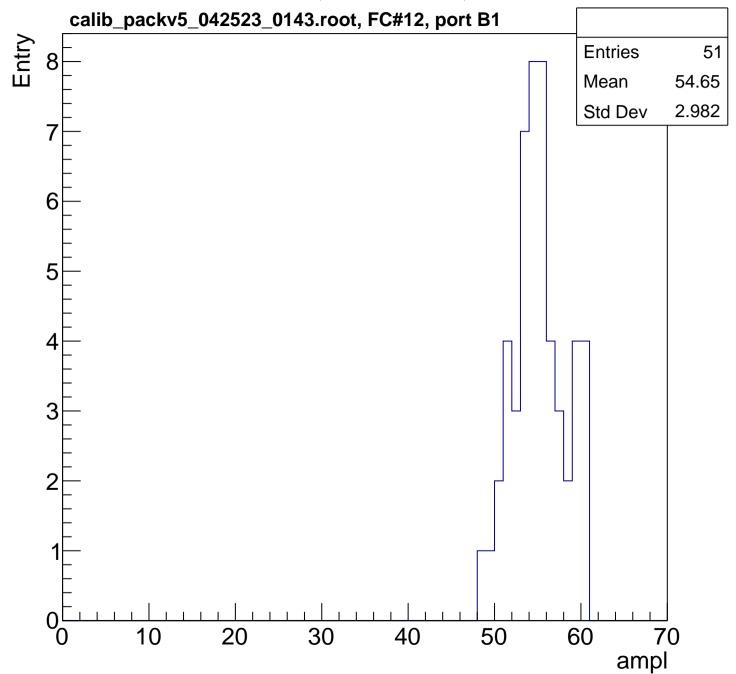


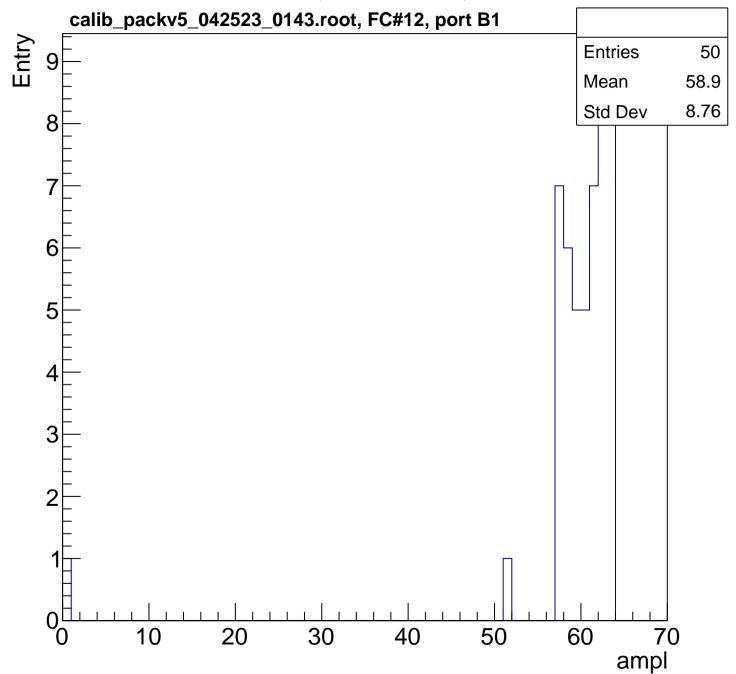


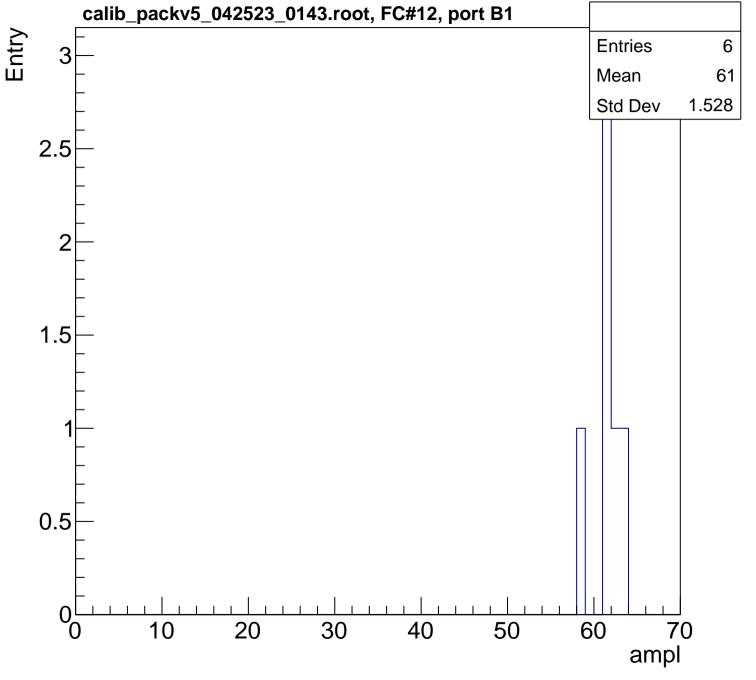












B0L102S, U4-ch93, adc7 calib_packv5_042523_0143.root, FC#12, port B1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70

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