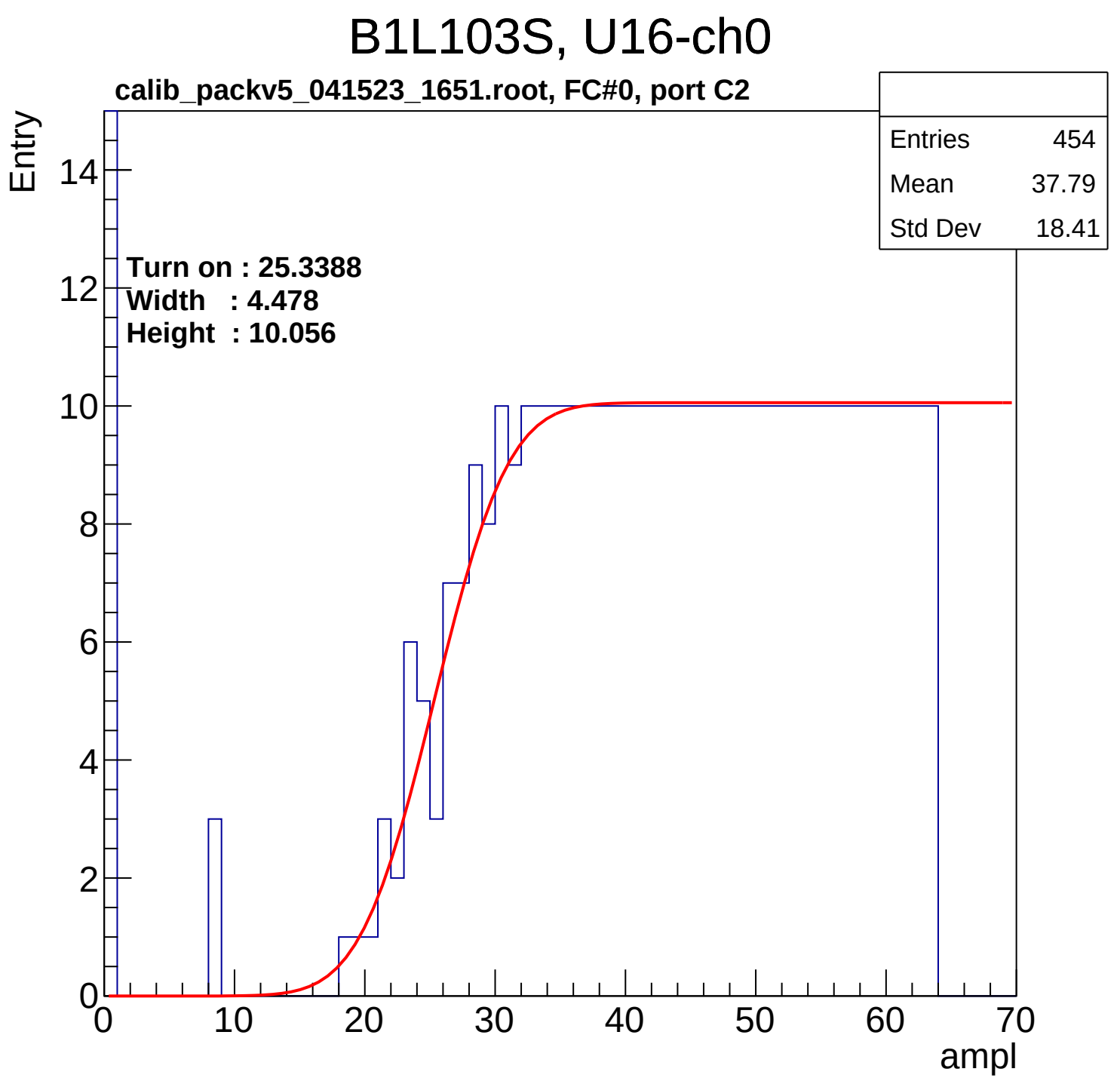
B1L103S, U16-ch0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 454
Mean 37.79
Std Dev 18.41
Turn on : 25.3388
Width : 4.478
Height : 10.056
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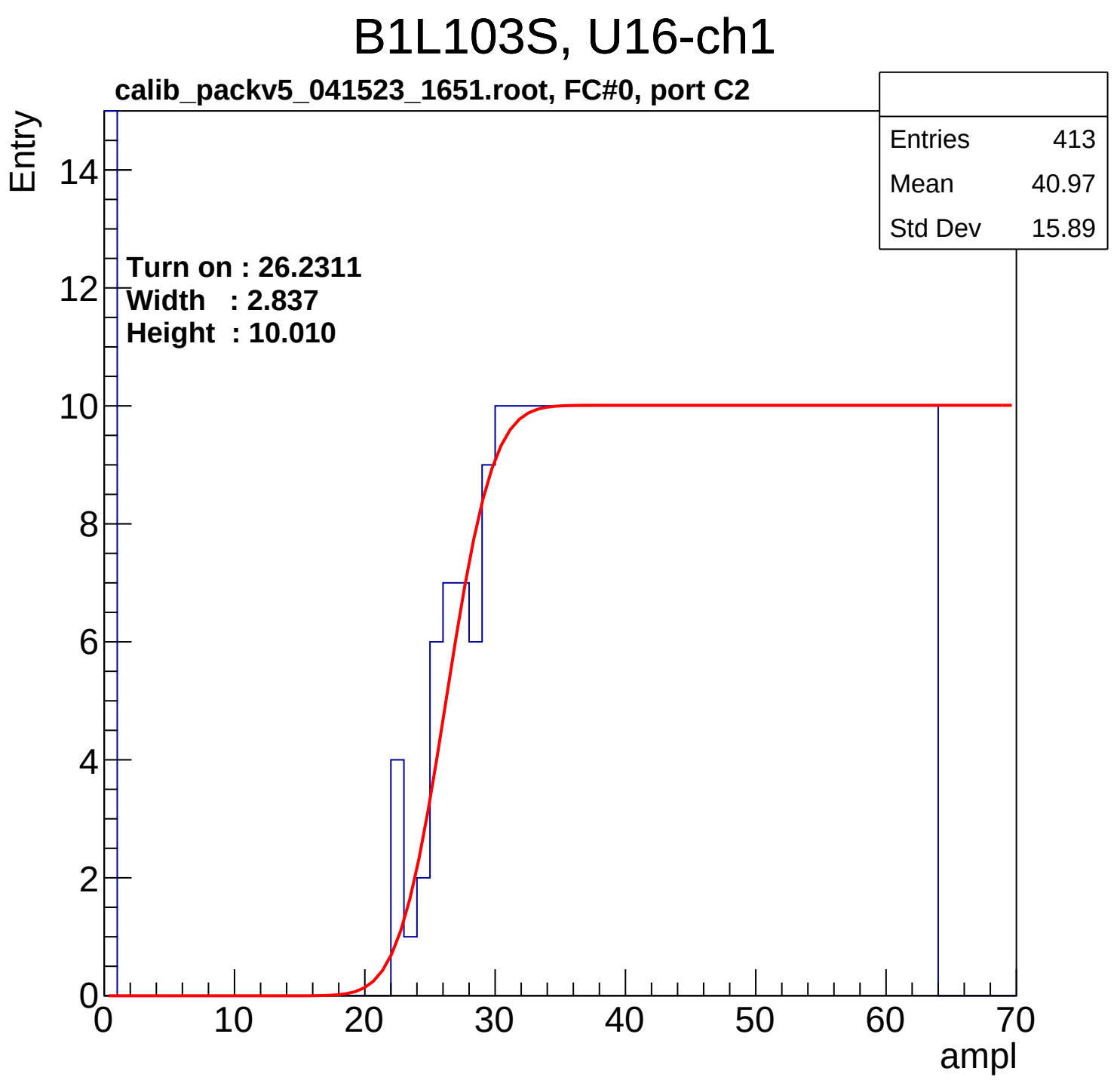
B1L103S, U16-ch1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 413
Mean 40.97
Std Dev 15.89
Turn on : 26.2311
Width : 2.837
Height : 10.010
Entry
ampl
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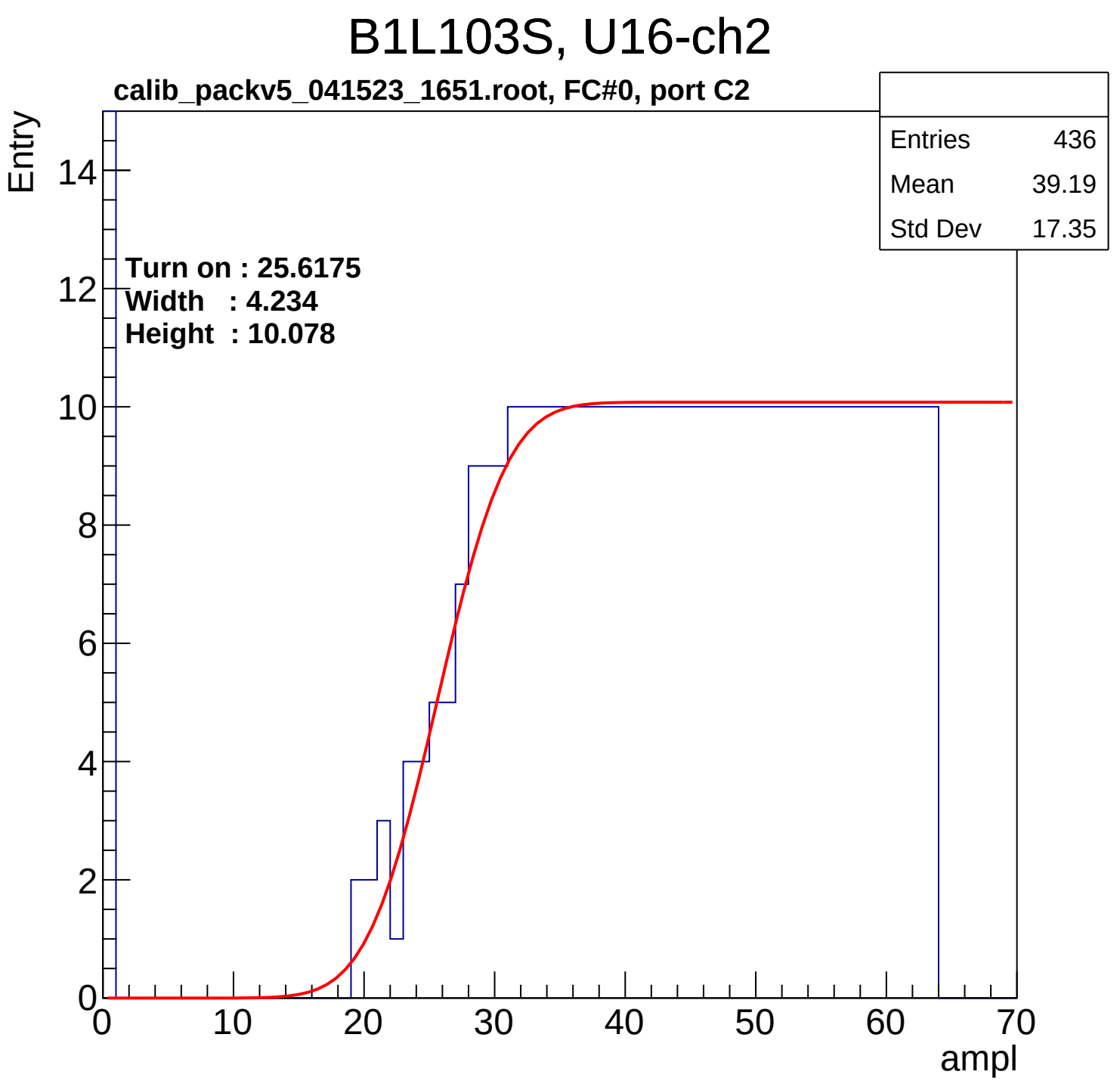
B1L103S, U16-ch2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 436
Mean 39.19
Std Dev 17.35
Turn on : 25.6175
Width : 4.234
Height : 10.078
Entry
ampl
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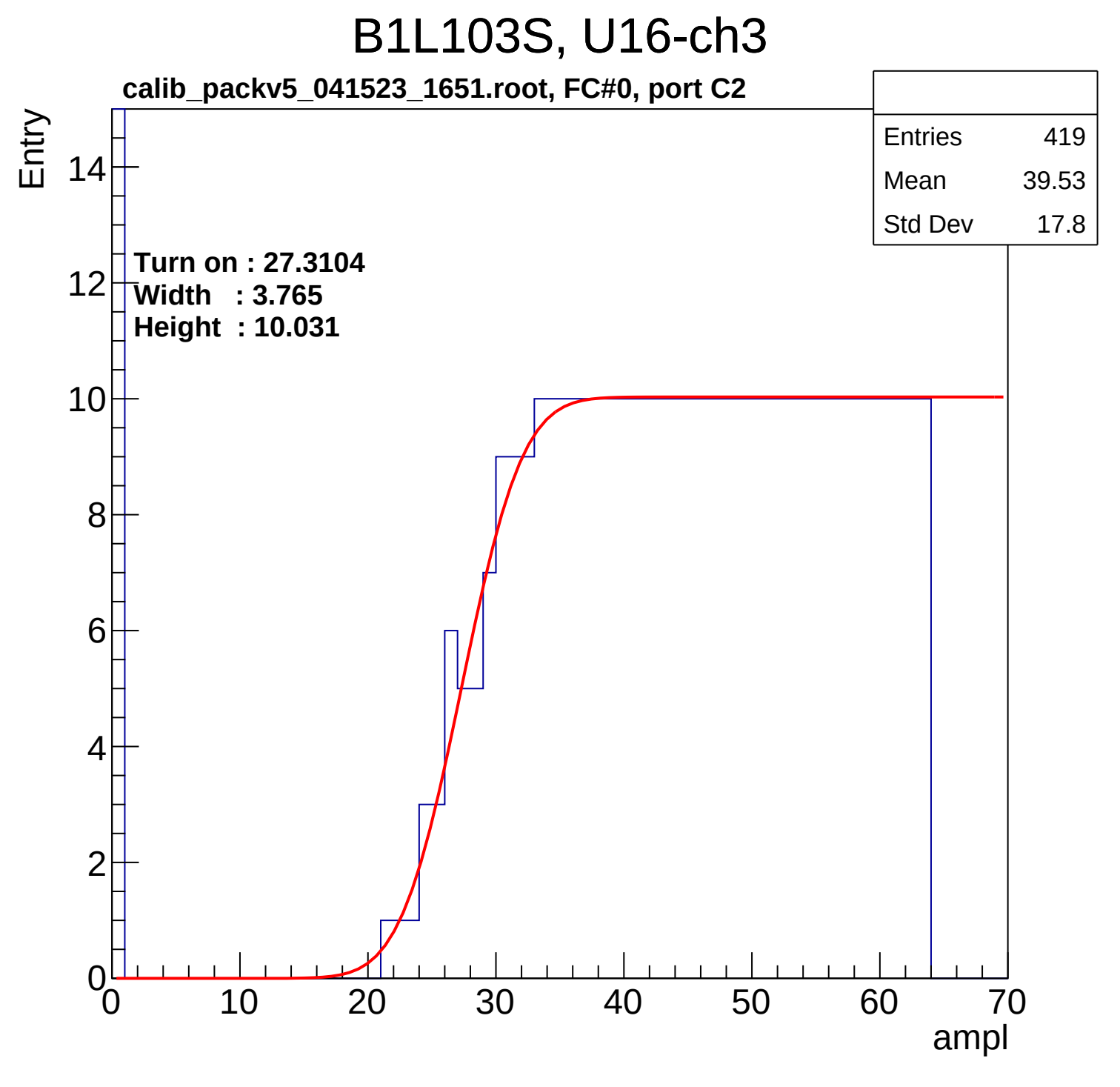
B1L103S, U16-ch3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 419
Mean 39.53
Std Dev 17.8
Turn on : 27.3104
Width : 3.765
Height : 10.031
Entry
ampl
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2
4
6
8
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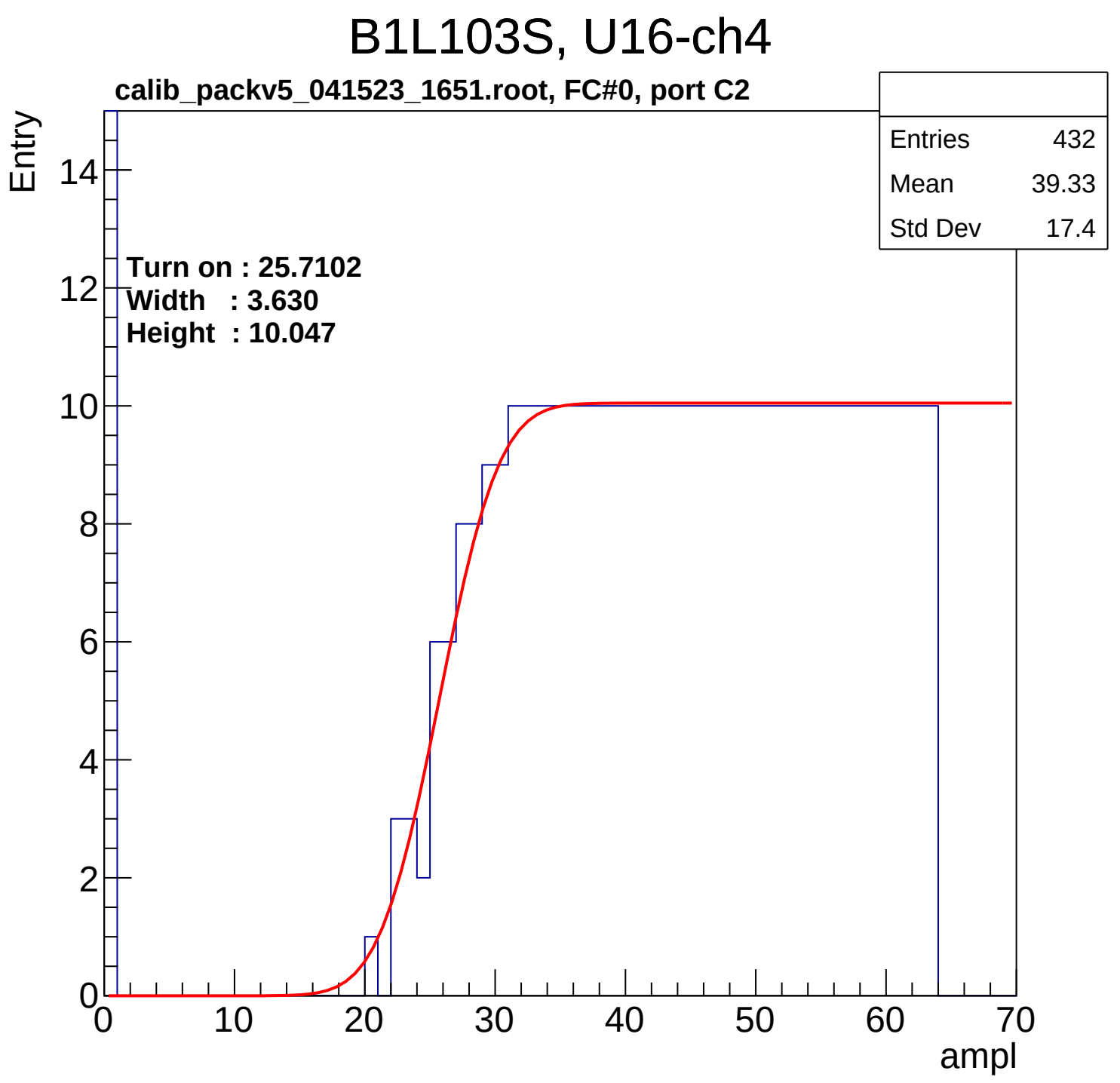
B1L103S, U16-ch4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 432
Mean 39.33
Std Dev 17.4
Turn on : 25.7102
Width : 3.630
Height : 10.047
Entry
ampl
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2
4
6
8
10
12
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0
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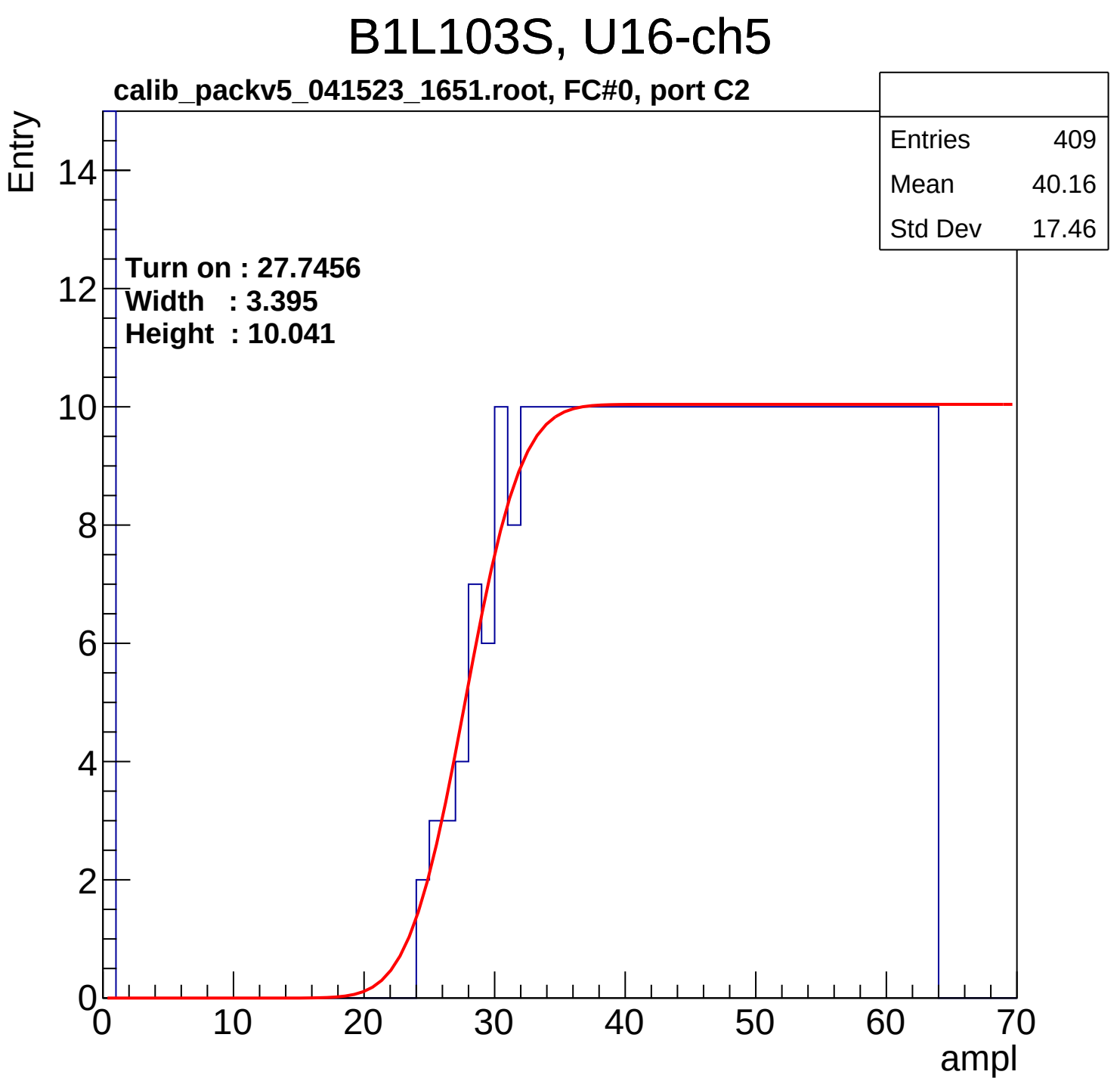
B1L103S, U16-ch5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 409
Mean 40.16
Std Dev 17.46
Turn on : 27.7456
Width : 3.395
Height : 10.041
Entry
ampl
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6
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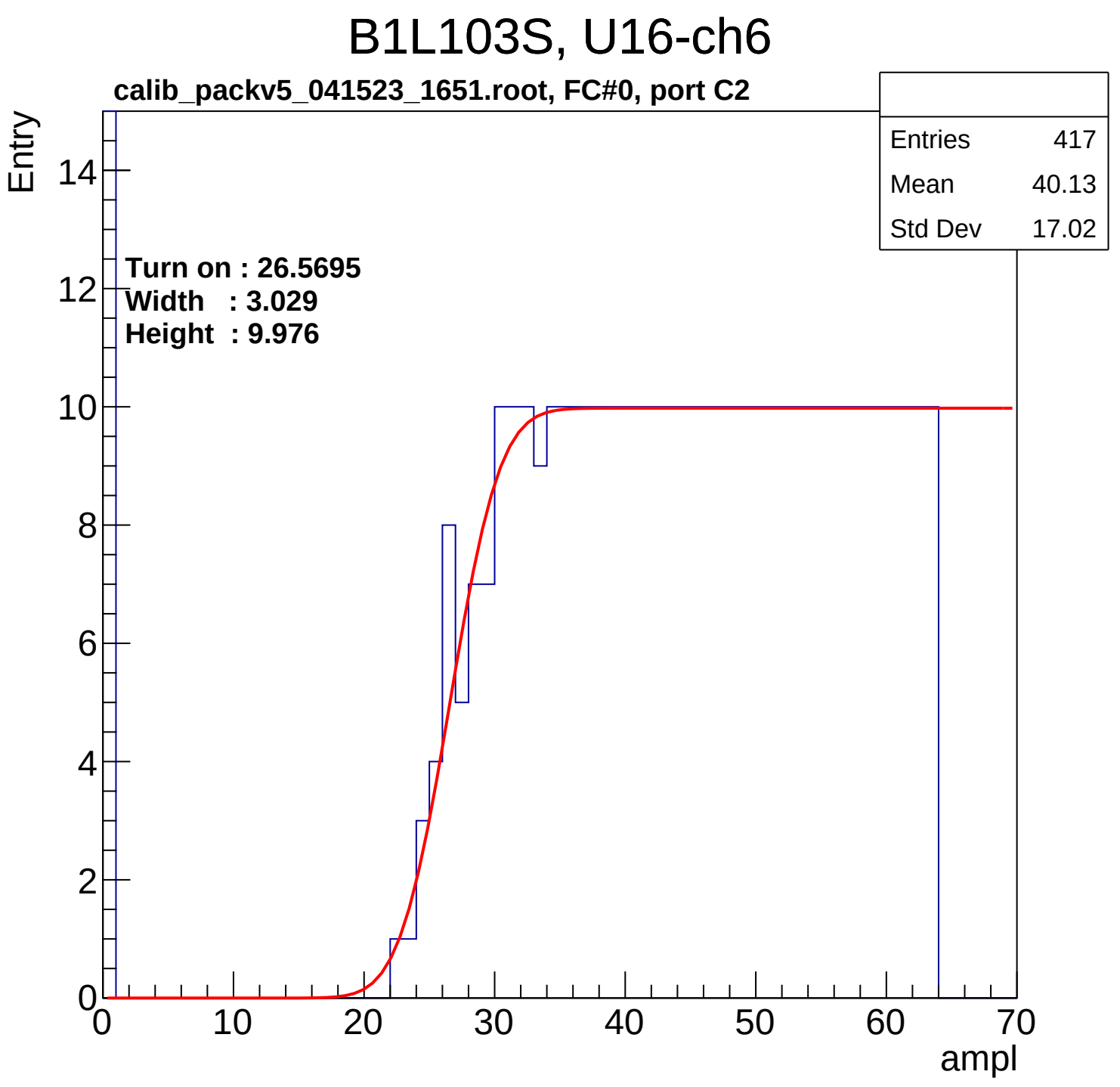
B1L103S, U16-ch6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 417
Mean 40.13
Std Dev 17.02
Turn on : 26.5695
Width : 3.029
Height : 9.976
Entry
ampl
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2
4
6
8
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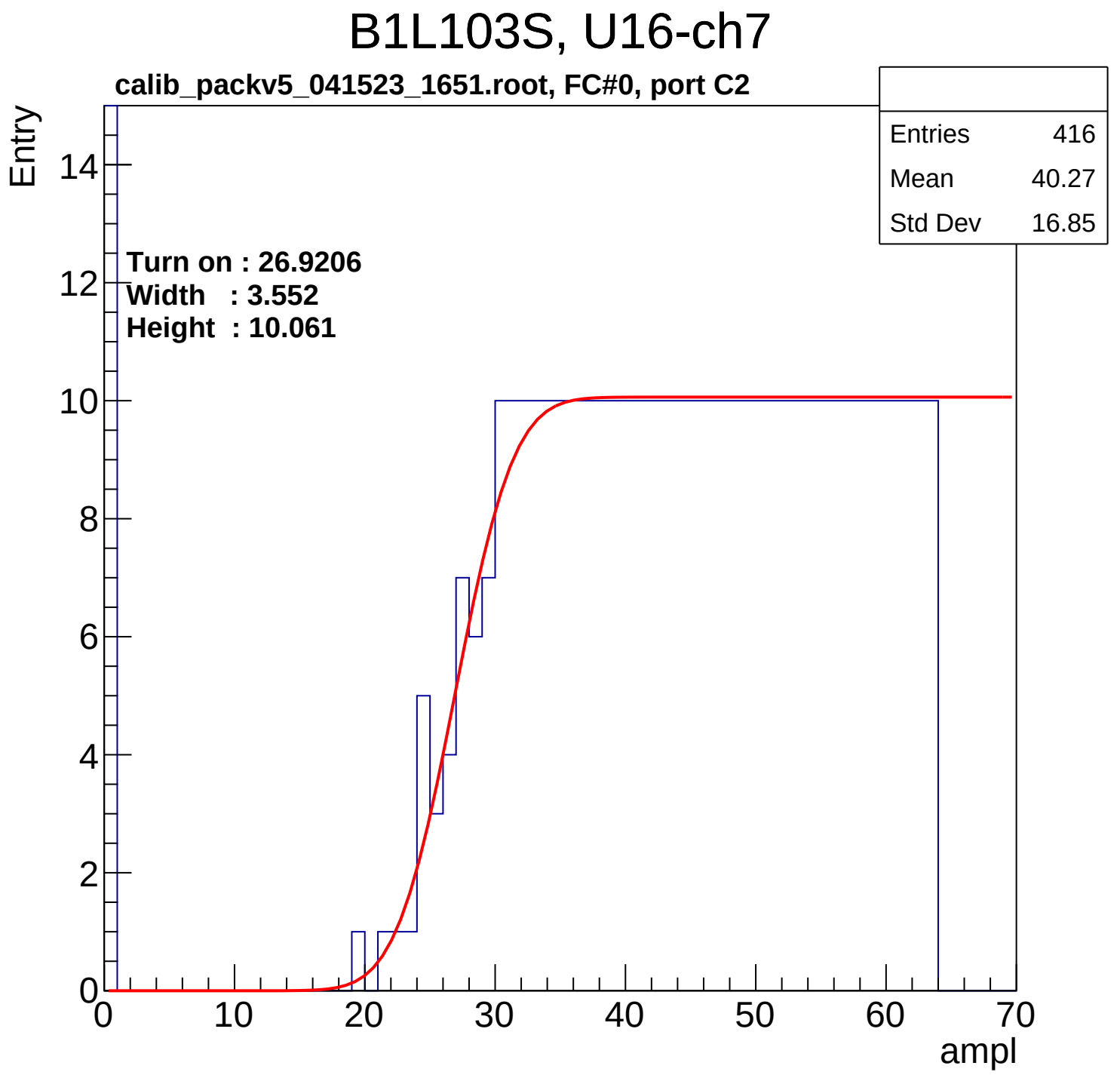
B1L103S, U16-ch7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 416
Mean 40.27
Std Dev 16.85
Turn on : 26.9206
Width : 3.552
Height : 10.061
Entry
ampl
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6
8
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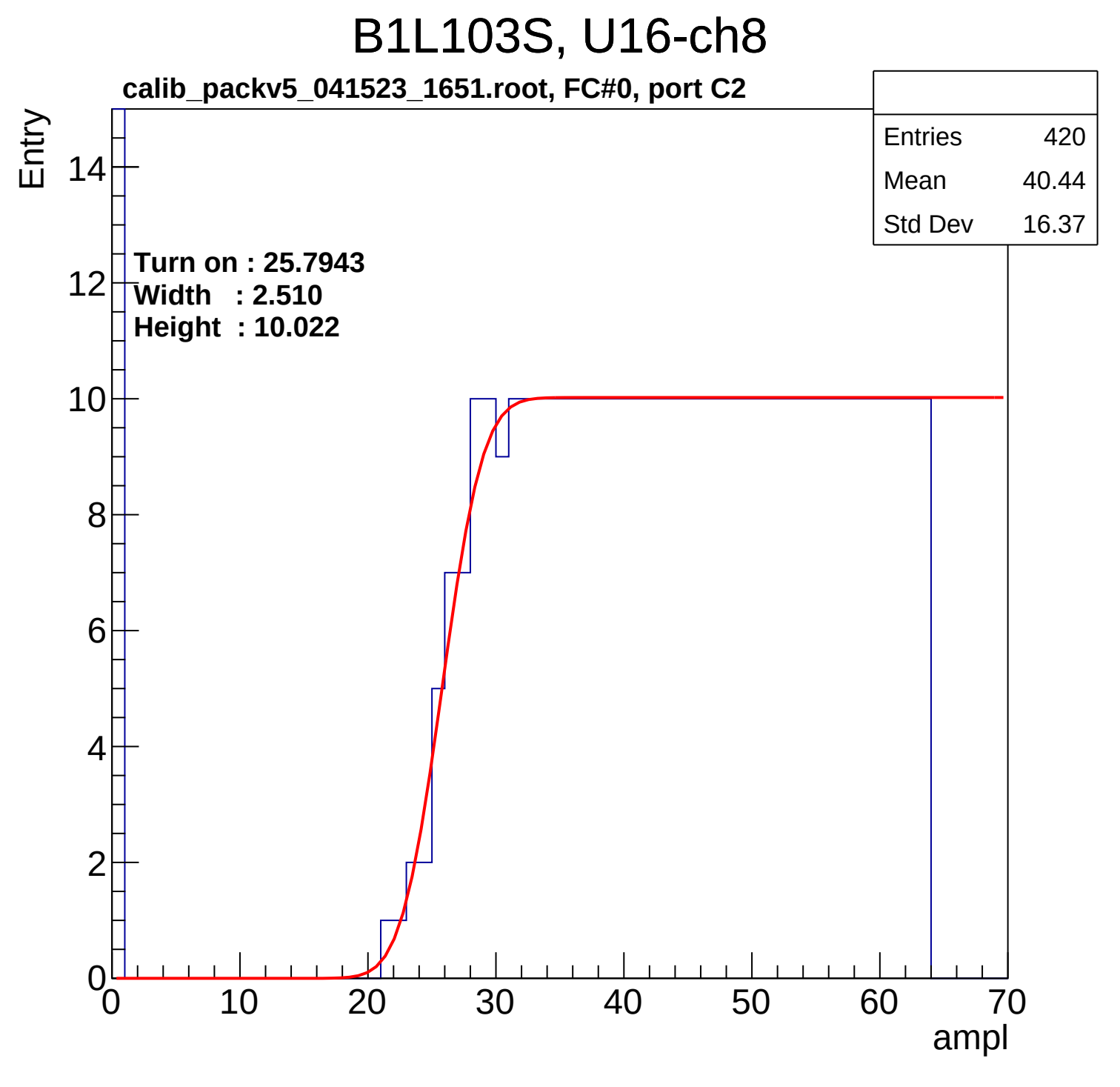
B1L103S, U16-ch8
calib_packv5_041523_1651.root, FC#0, port C2
Entries 420
Mean 40.44
Std Dev 16.37
Turn on : 25.7943
Width : 2.510
Height : 10.022
Entry
ampl
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6
8
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0
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60
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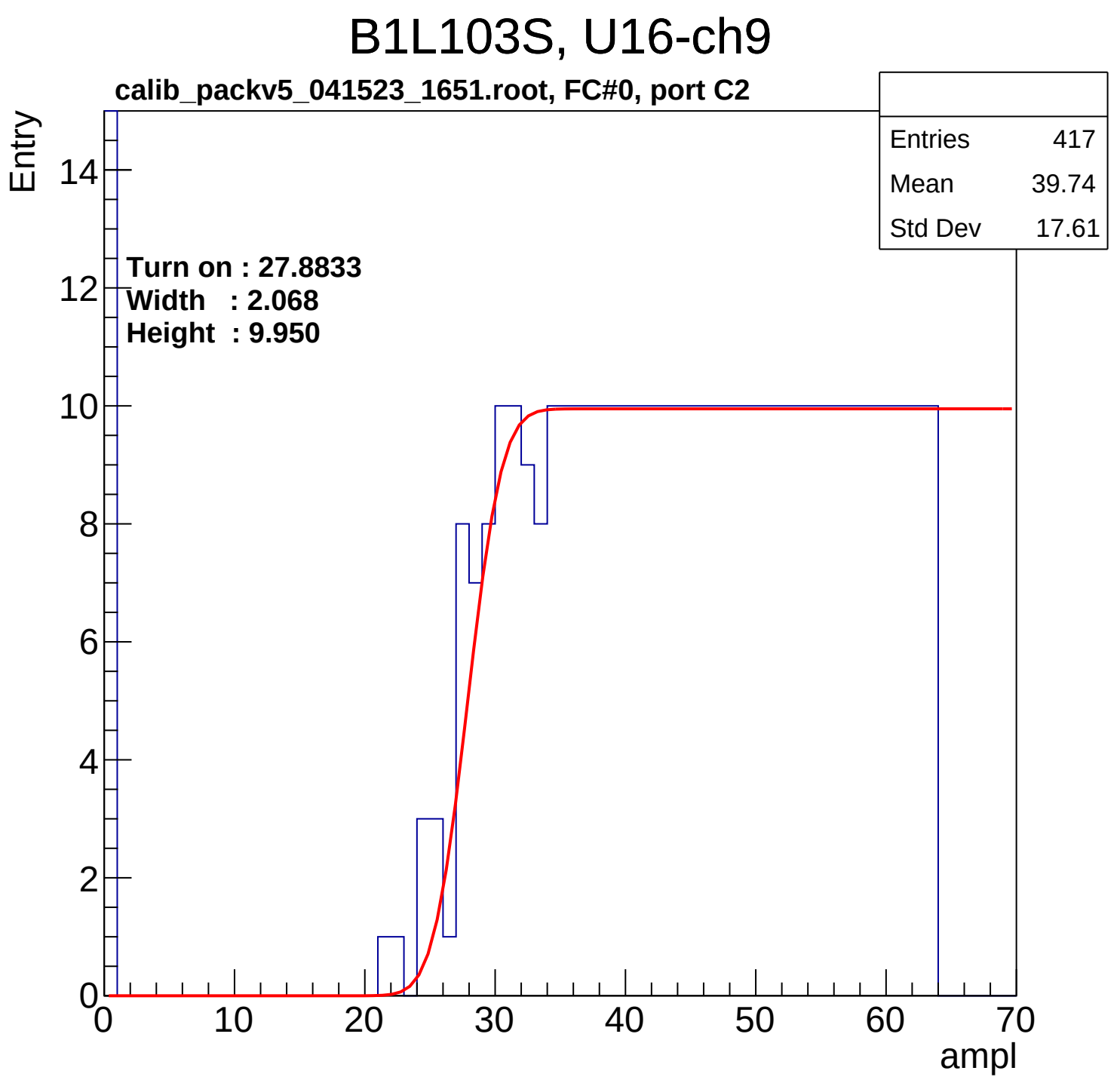
B1L103S, U16-ch9
calib_packv5_041523_1651.root, FC#0, port C2
Entries 417
Mean 39.74
Std Dev 17.61
Turn on : 27.8833
Width : 2.068
Height : 9.950
Entry
ampl
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4
6
8
10
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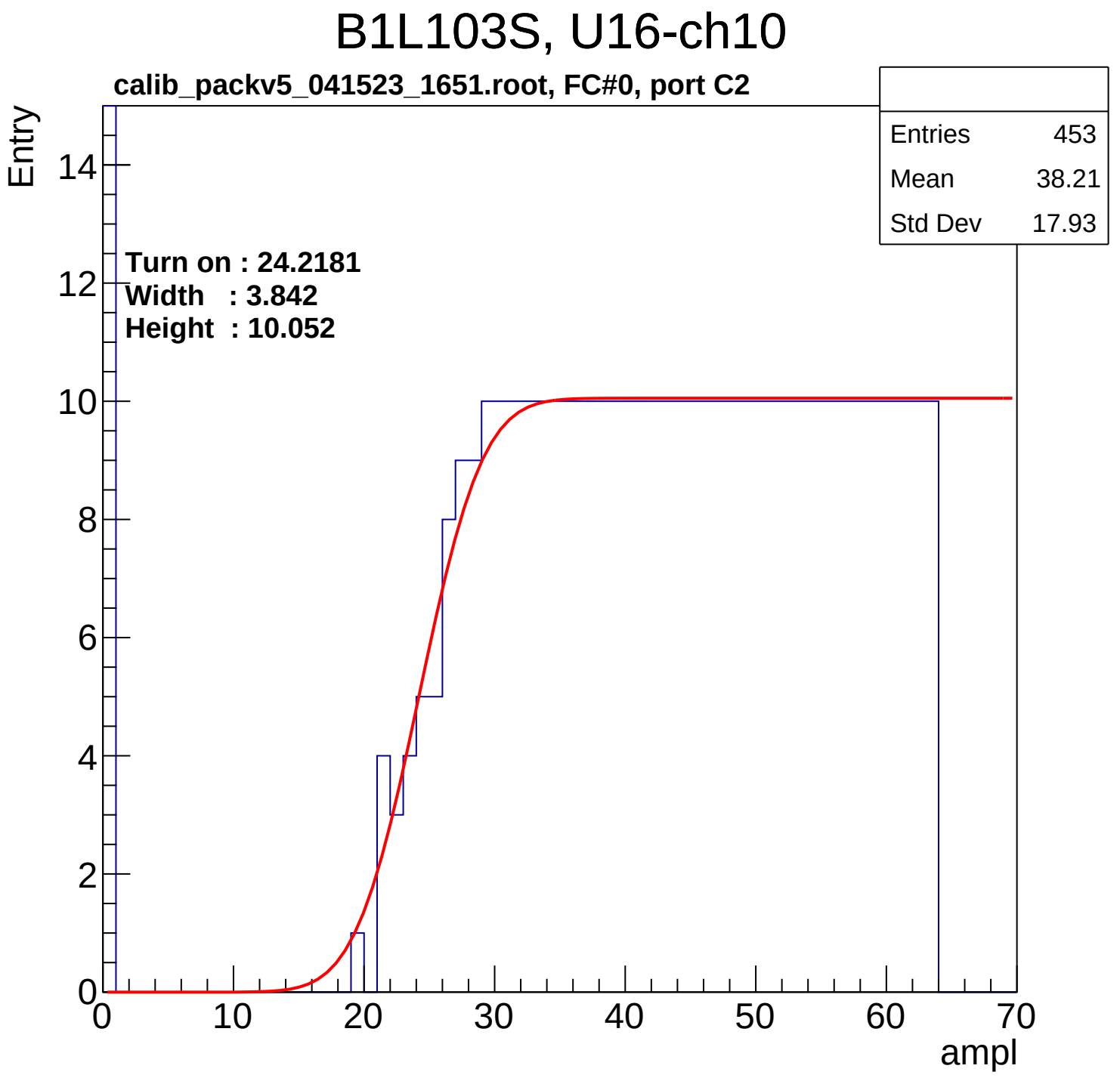
B1L103S, U16-ch10
calib_packv5_041523_1651.root, FC#0, port C2
Entries 453
Mean 38.21
Std Dev 17.93
Turn on : 24.2181
Width : 3.842
Height : 10.052
Entry
ampl
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8
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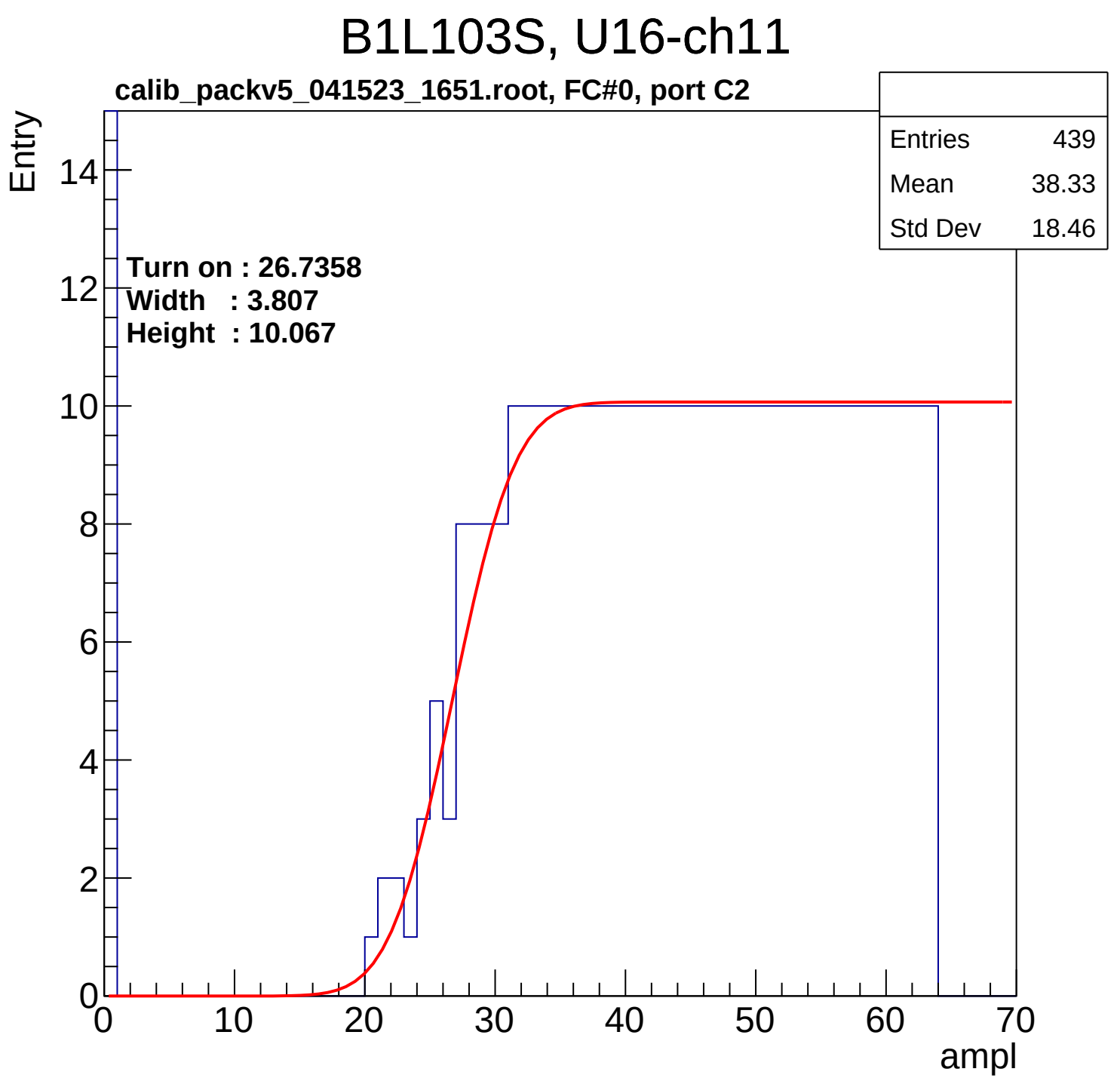
B1L103S, U16-ch11
calib_packv5_041523_1651.root, FC#0, port C2
Entries 439
Mean 38.33
Std Dev 18.46
Turn on : 26.7358
Width : 3.807
Height : 10.067
Entry
ampl
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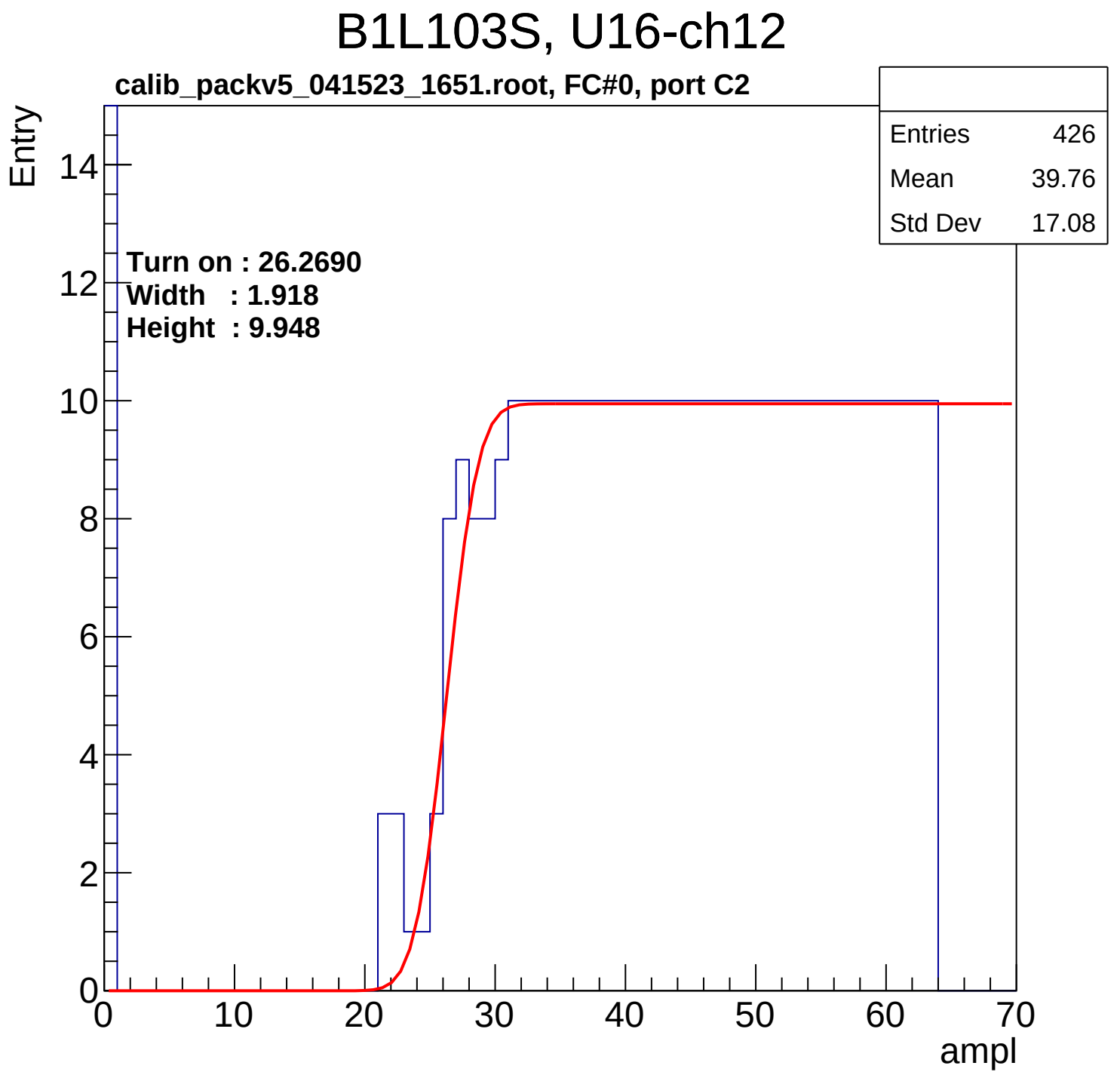
B1L103S, U16-ch12
calib_packv5_041523_1651.root, FC#0, port C2
Entries 426
Mean 39.76
Std Dev 17.08
Turn on : 26.2690
Width : 1.918
Height : 9.948
Entry
ampl
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6
8
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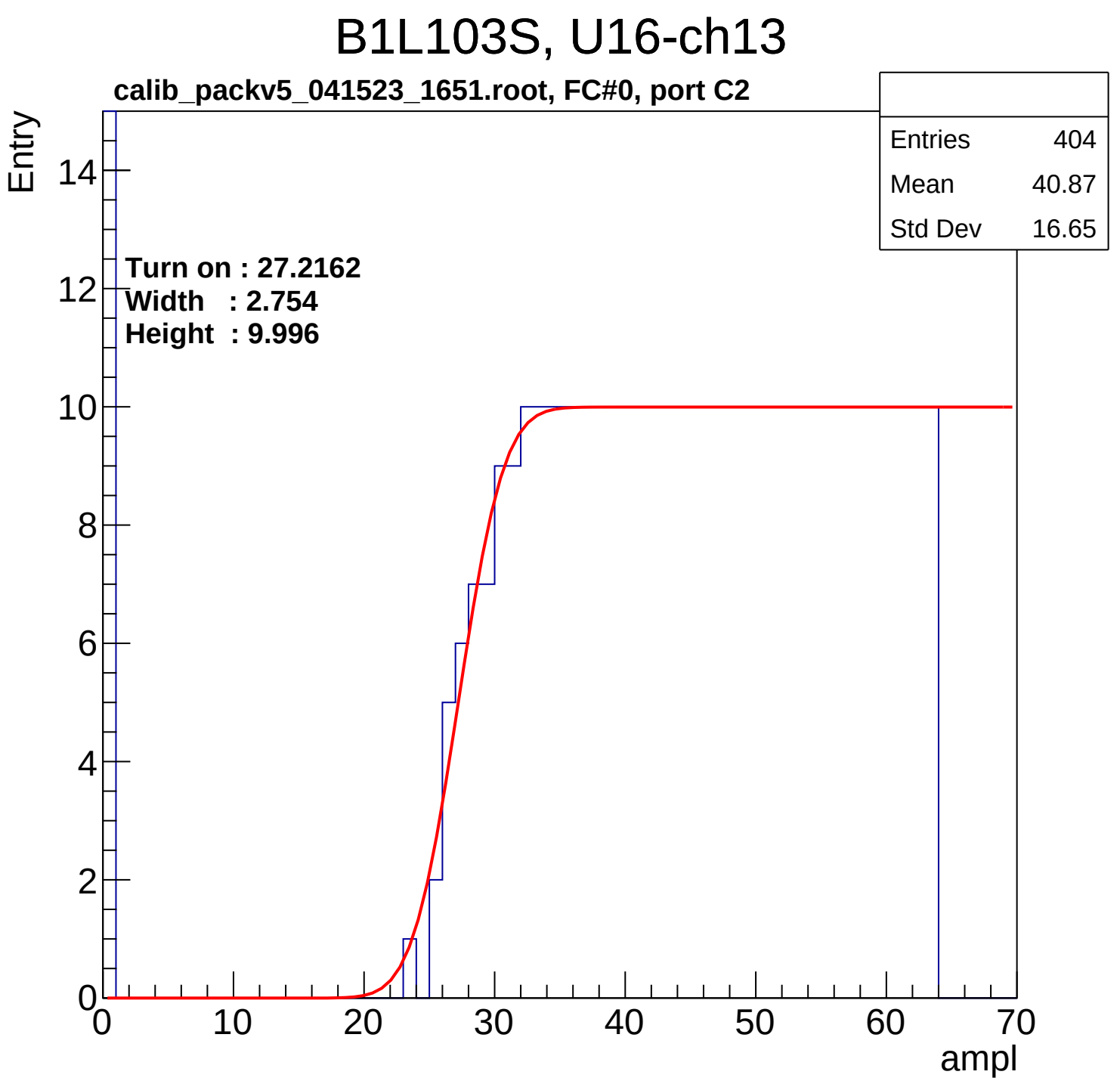
B1L103S, U16-ch13
calib_packv5_041523_1651.root, FC#0, port C2
Entries 404
Mean 40.87
Std Dev 16.65
Turn on : 27.2162
Width : 2.754
Height : 9.996
Entry
ampl
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8
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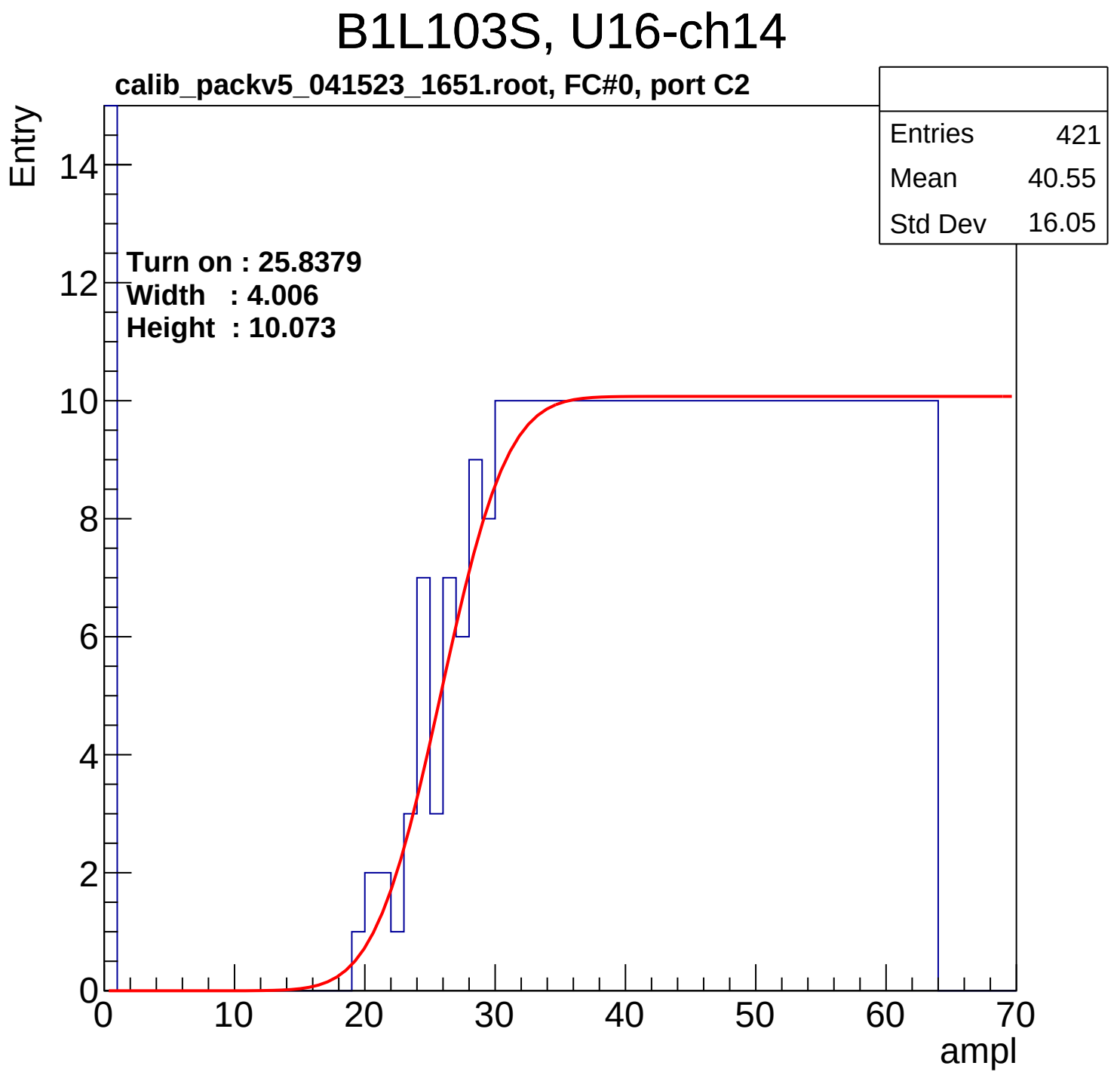
B1L103S, U16-ch14
calib_packv5_041523_1651.root, FC#0, port C2
Entries 421
Mean 40.55
Std Dev 16.05
Turn on : 25.8379
Width : 4.006
Height : 10.073
Entry
ampl
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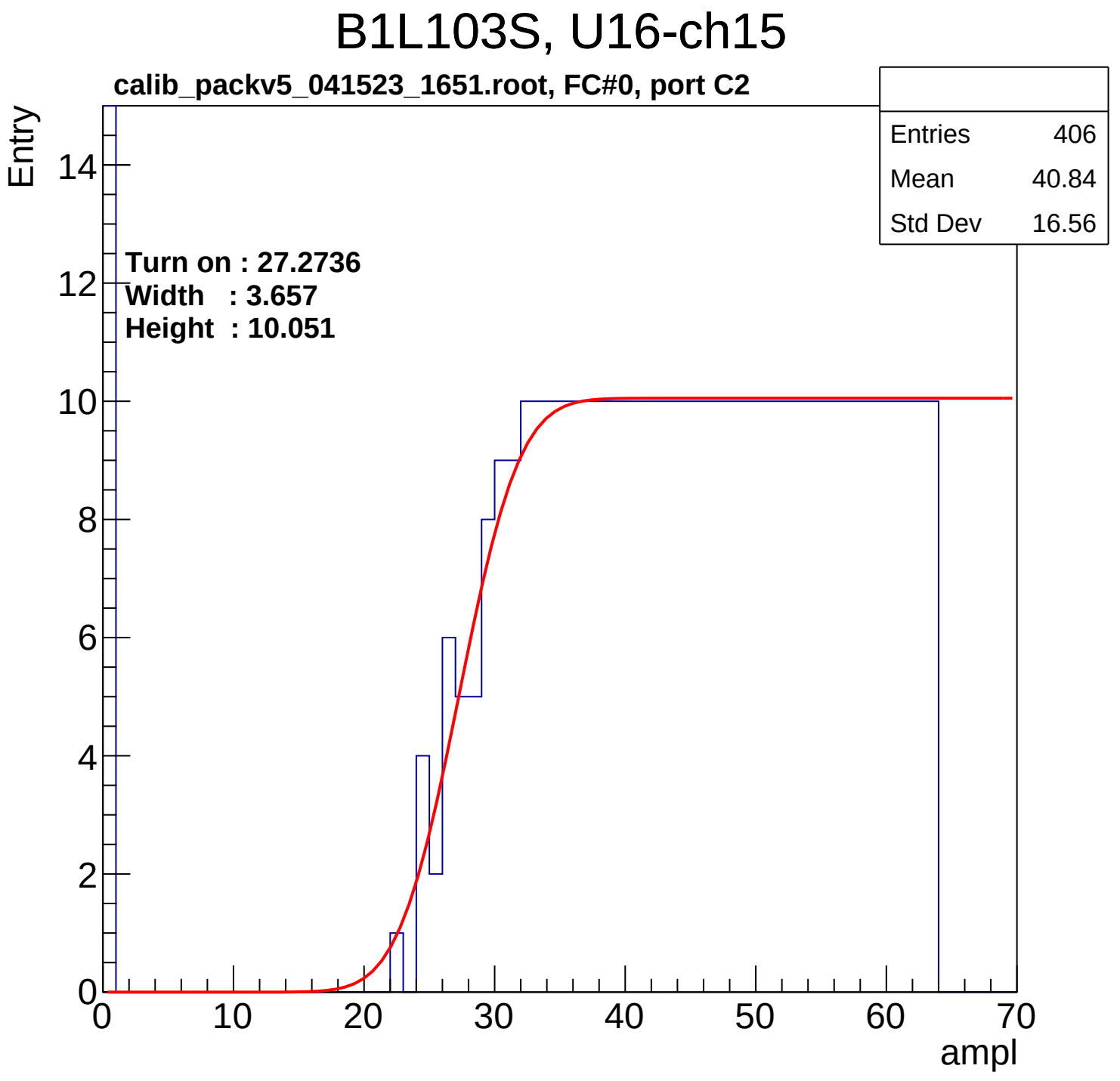
B1L103S, U16-ch15
calib_packv5_041523_1651.root, FC#0, port C2
Entries 406
Mean 40.84
Std Dev 16.56
Turn on : 27.2736
Width : 3.657
Height : 10.051
Entry
ampl
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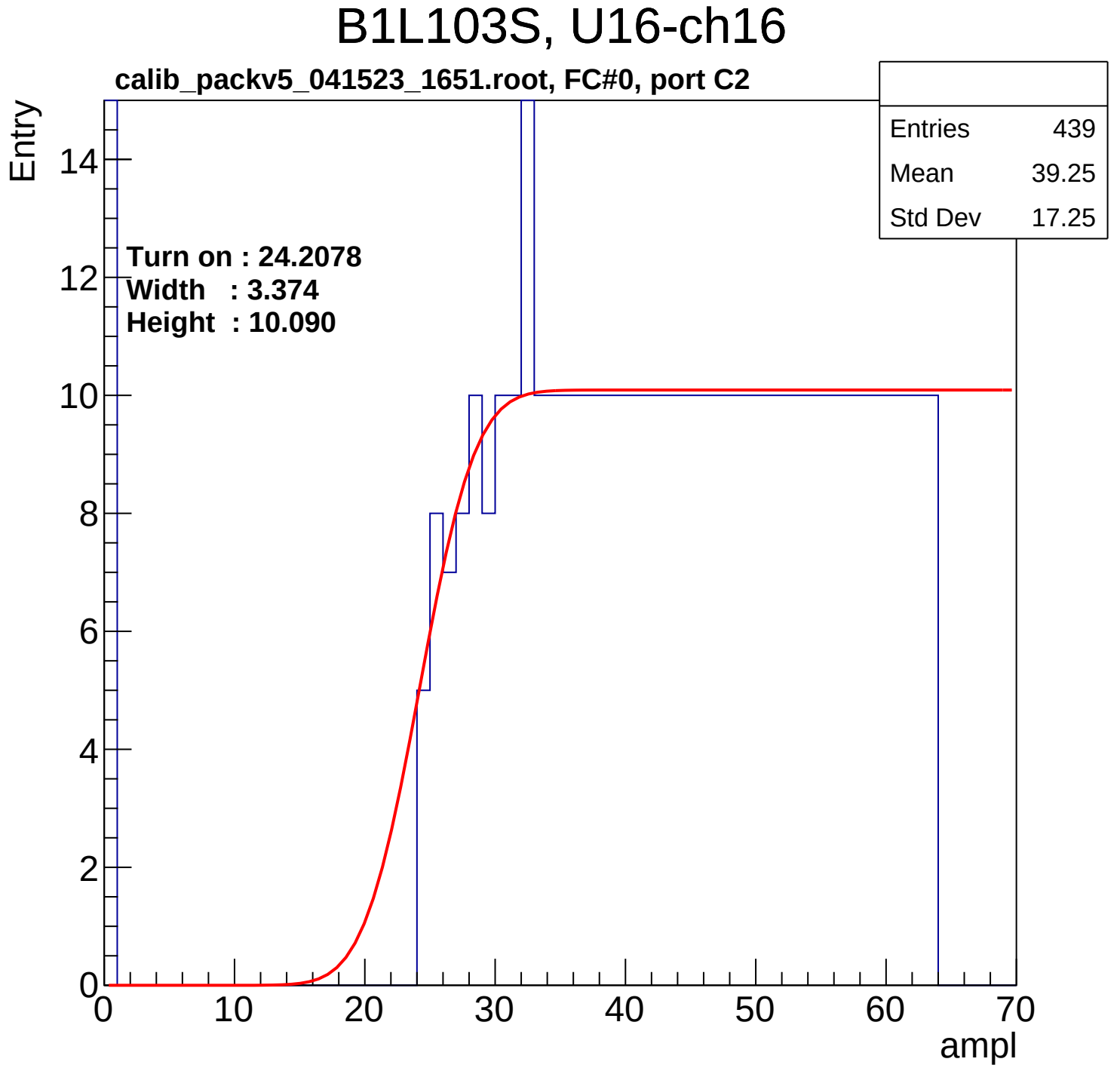
B1L103S, U16-ch16
calib_packv5_041523_1651.root, FC#0, port C2
Entries 439
Mean 39.25
Std Dev 17.25
Turn on : 24.2078
Width : 3.374
Height : 10.090
Entry
ampl
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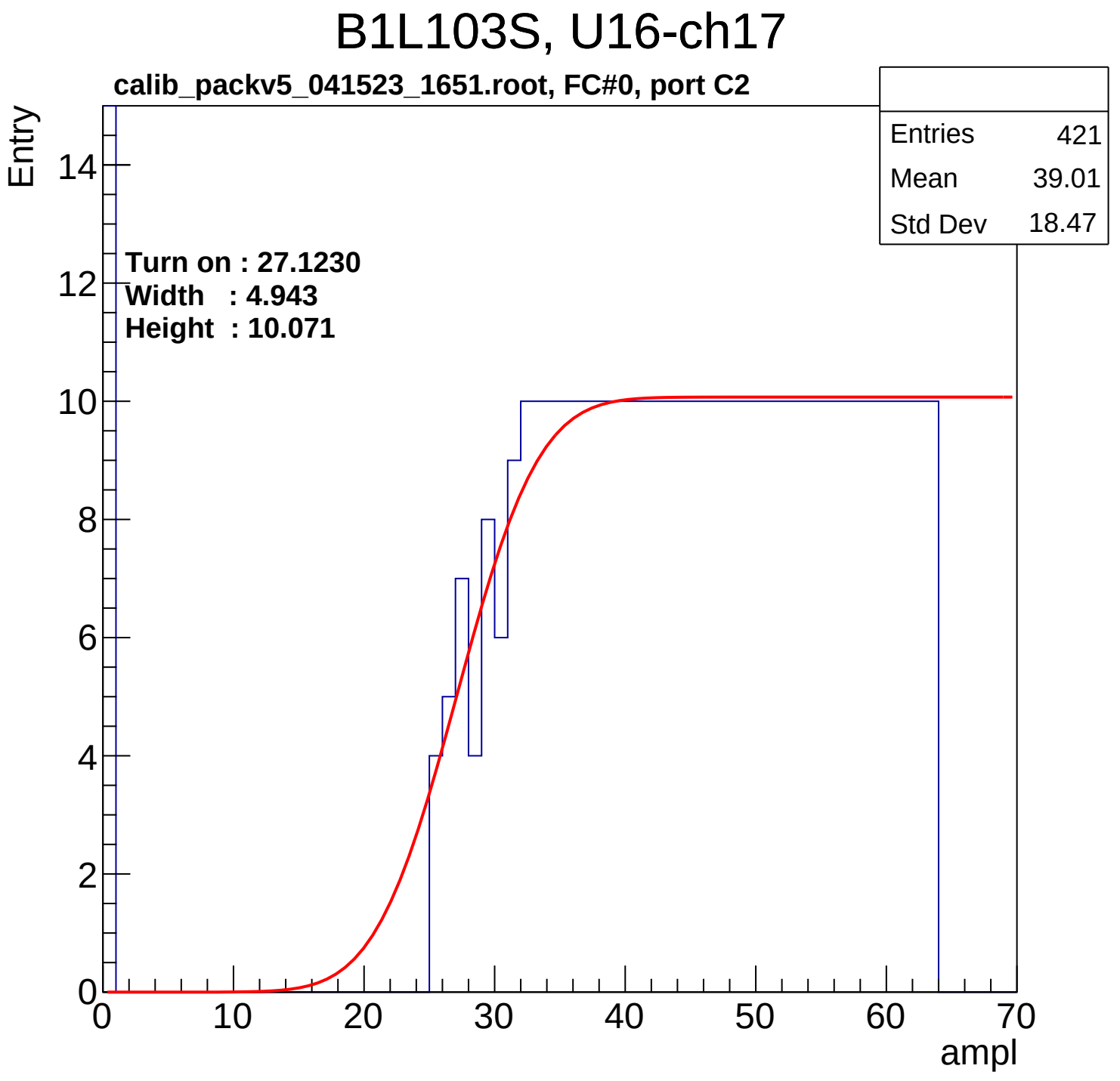
B1L103S, U16-ch17
calib_packv5_041523_1651.root, FC#0, port C2
Entries 421
Mean 39.01
Std Dev 18.47
Turn on : 27.1230
Width : 4.943
Height : 10.071
Entry
ampl
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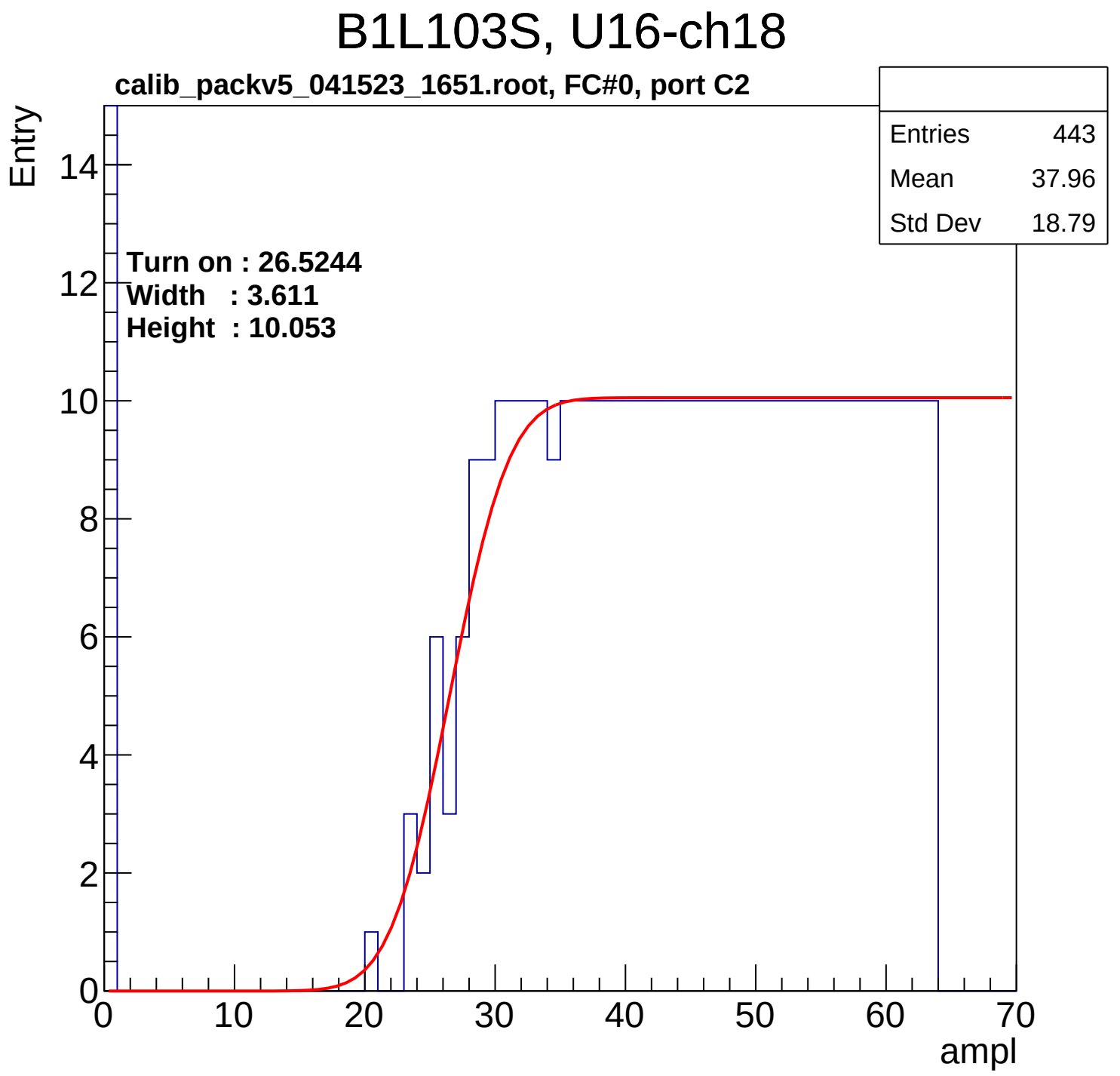
B1L103S, U16-ch18
calib_packv5_041523_1651.root, FC#0, port C2
Entries 443
Mean 37.96
Std Dev 18.79
Turn on : 26.5244
Width : 3.611
Height : 10.053
Entry
ampl
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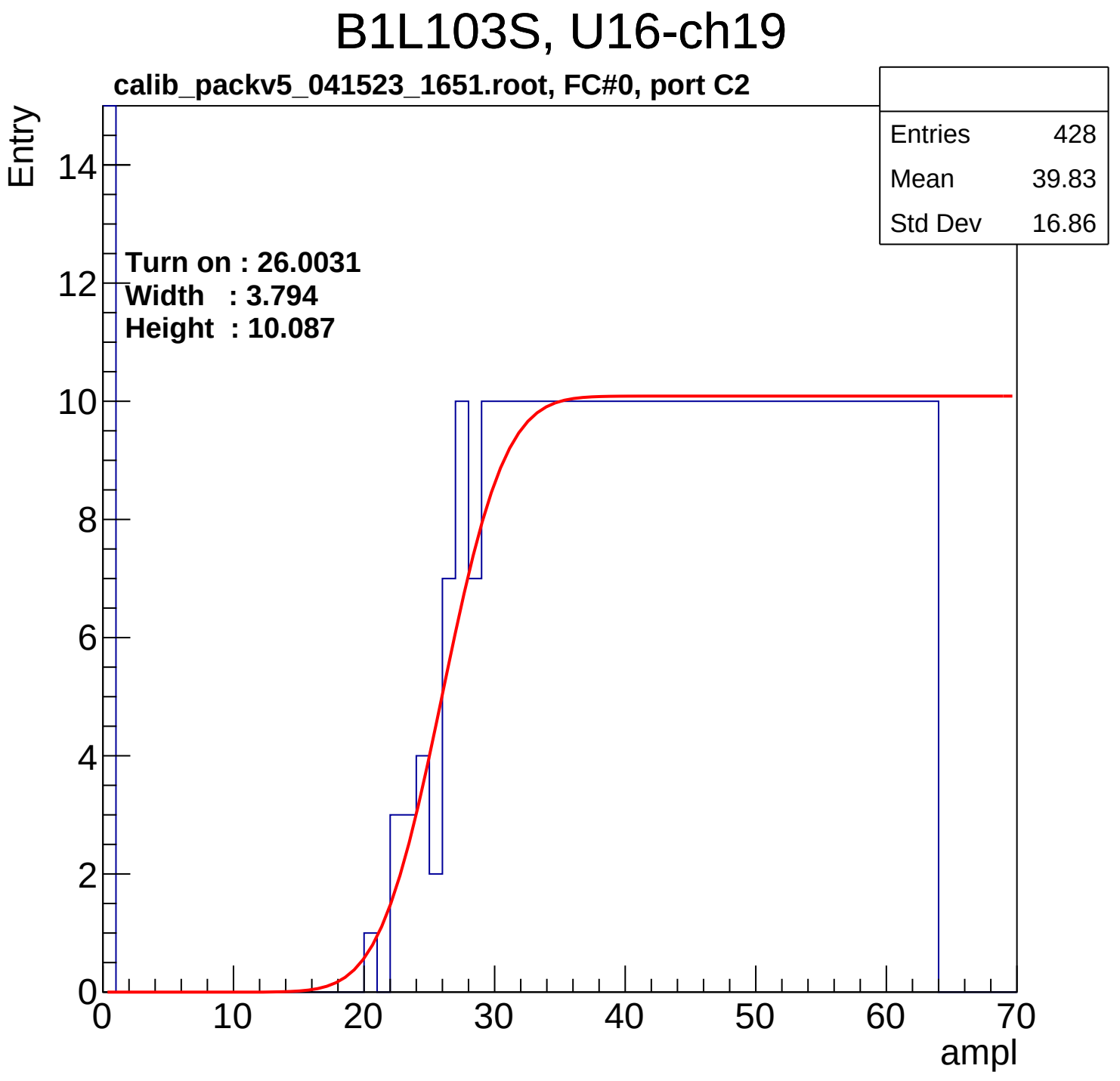
B1L103S, U16-ch19
calib_packv5_041523_1651.root, FC#0, port C2
Entries 428
Mean 39.83
Std Dev 16.86
Turn on : 26.0031
Width : 3.794
Height : 10.087
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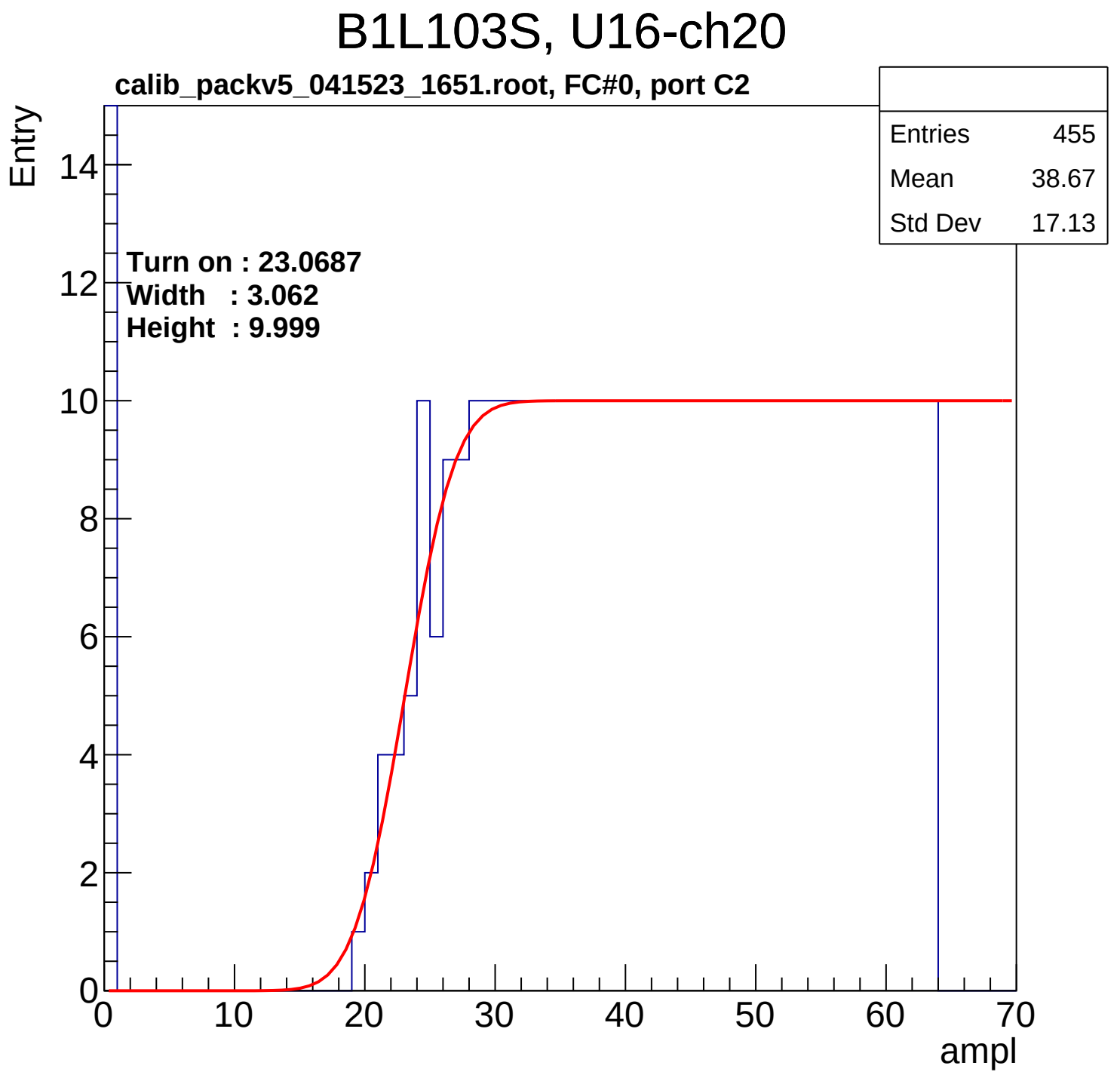
B1L103S, U16-ch20
calib_packv5_041523_1651.root, FC#0, port C2
Entries 455
Mean 38.67
Std Dev 17.13
Turn on : 23.0687
Width : 3.062
Height : 9.999
Entry
ampl
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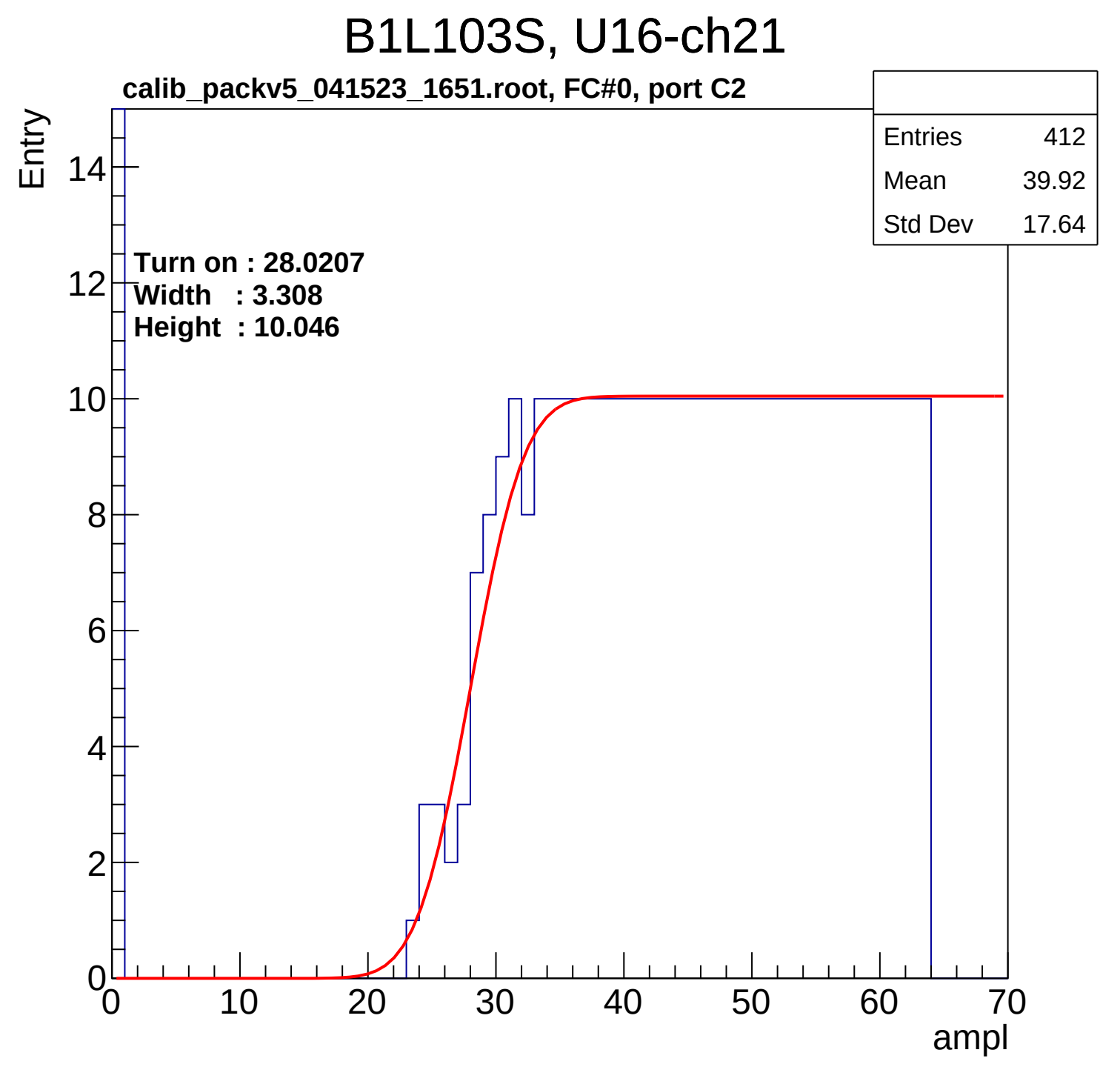
B1L103S, U16-ch21
calib_packv5_041523_1651.root, FC#0, port C2
Entries 412
Mean 39.92
Std Dev 17.64
Turn on : 28.0207
Width : 3.308
Height : 10.046
Entry
ampl
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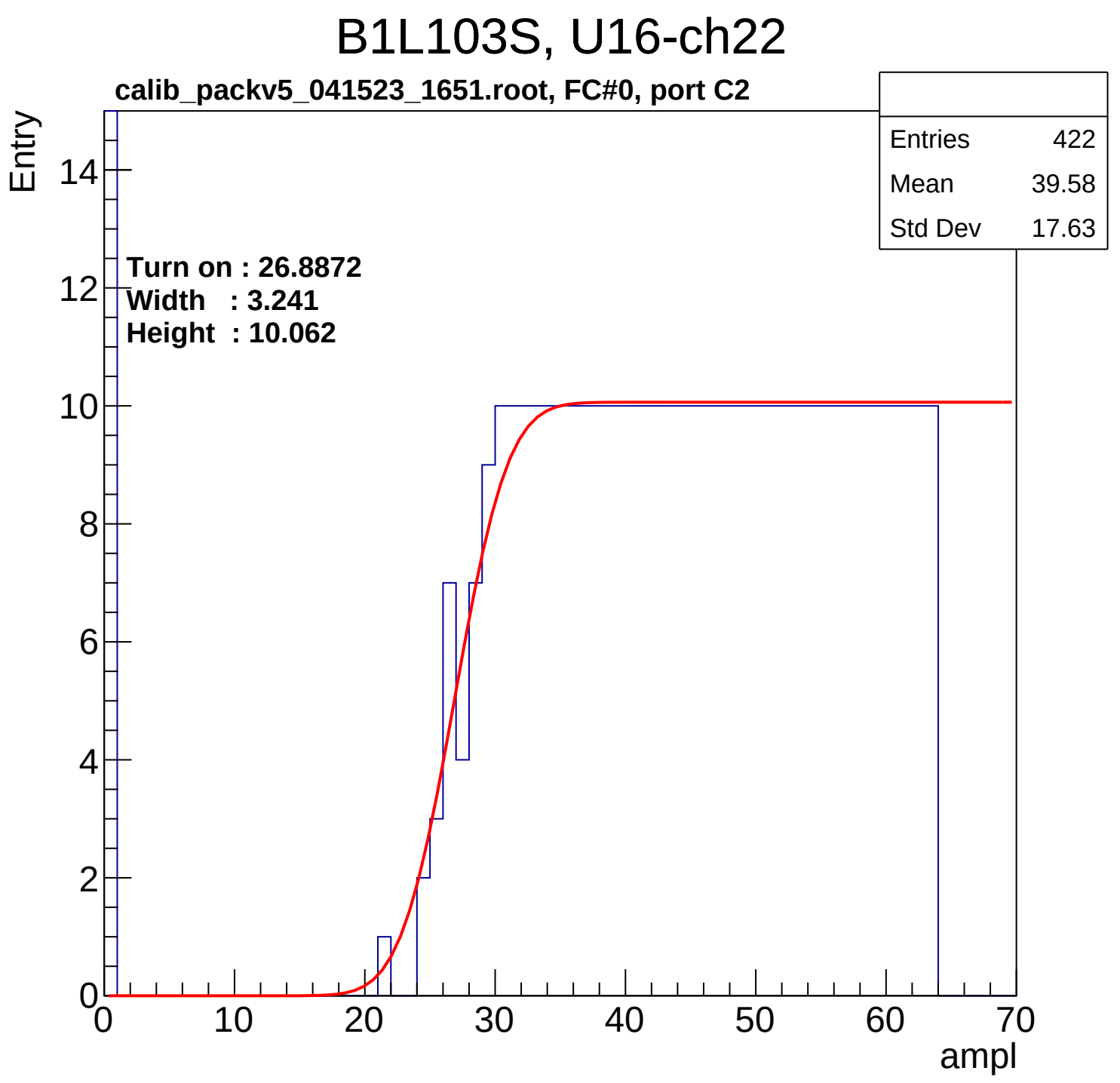
B1L103S, U16-ch22
calib_packv5_041523_1651.root, FC#0, port C2
Entries 422
Mean 39.58
Std Dev 17.63
Turn on : 26.8872
Width : 3.241
Height : 10.062
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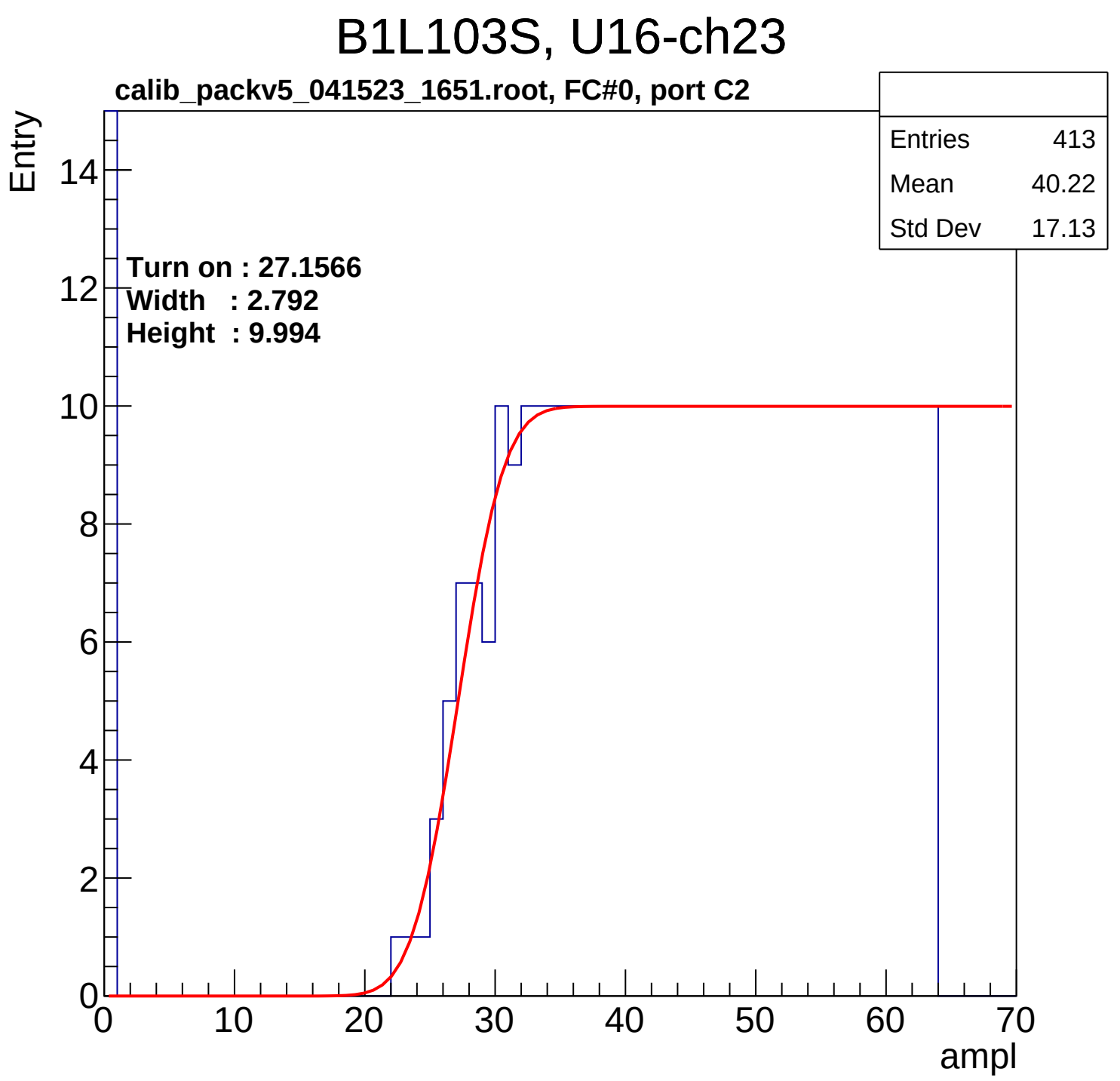
B1L103S, U16-ch23
calib_packv5_041523_1651.root, FC#0, port C2
Entries 413
Mean 40.22
Std Dev 17.13
Turn on : 27.1566
Width : 2.792
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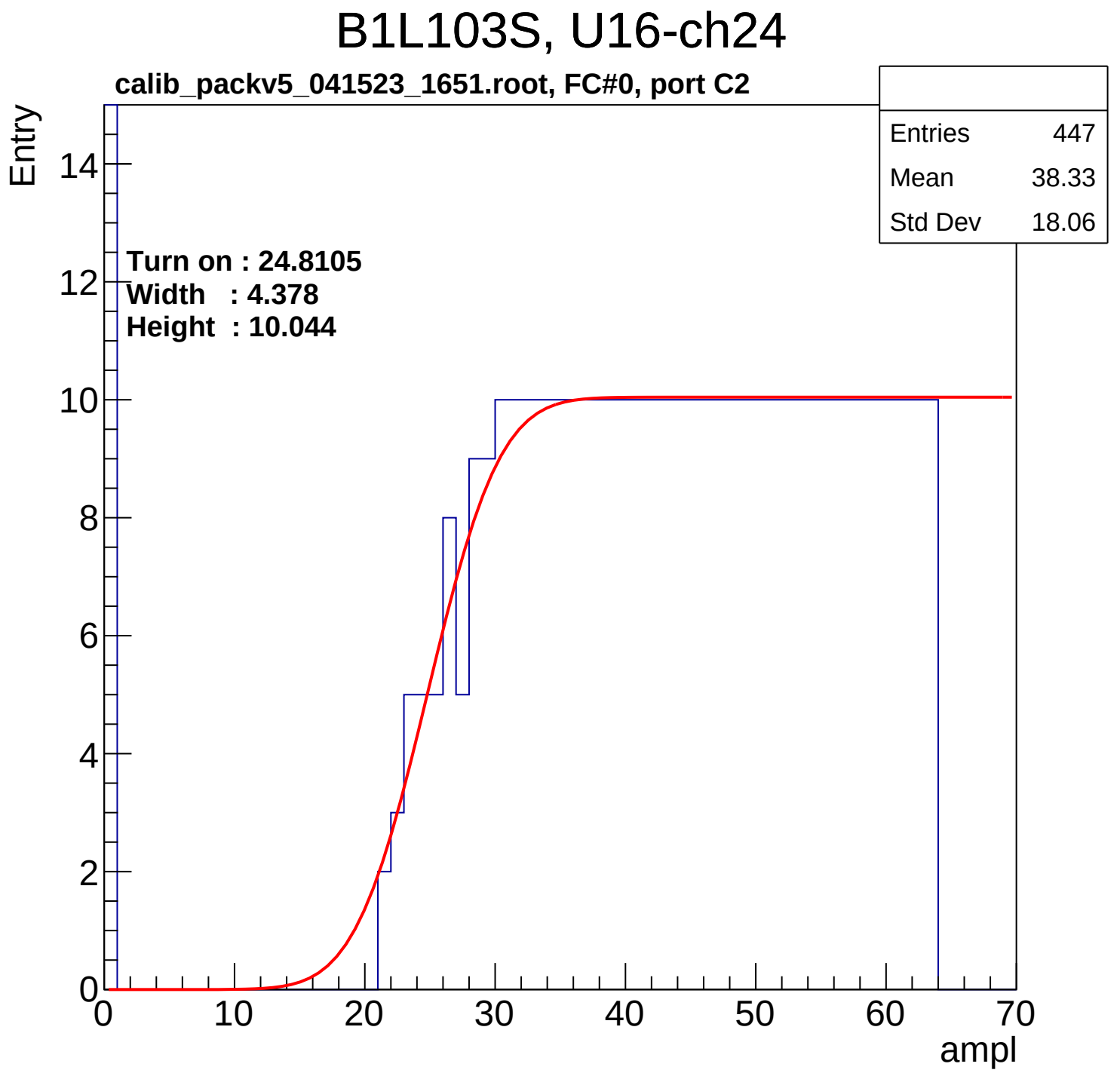
B1L103S, U16-ch24
calib_packv5_041523_1651.root, FC#0, port C2
Entries 447
Mean 38.33
Std Dev 18.06
Turn on : 24.8105
Width : 4.378
Height : 10.044
Entry
ampl
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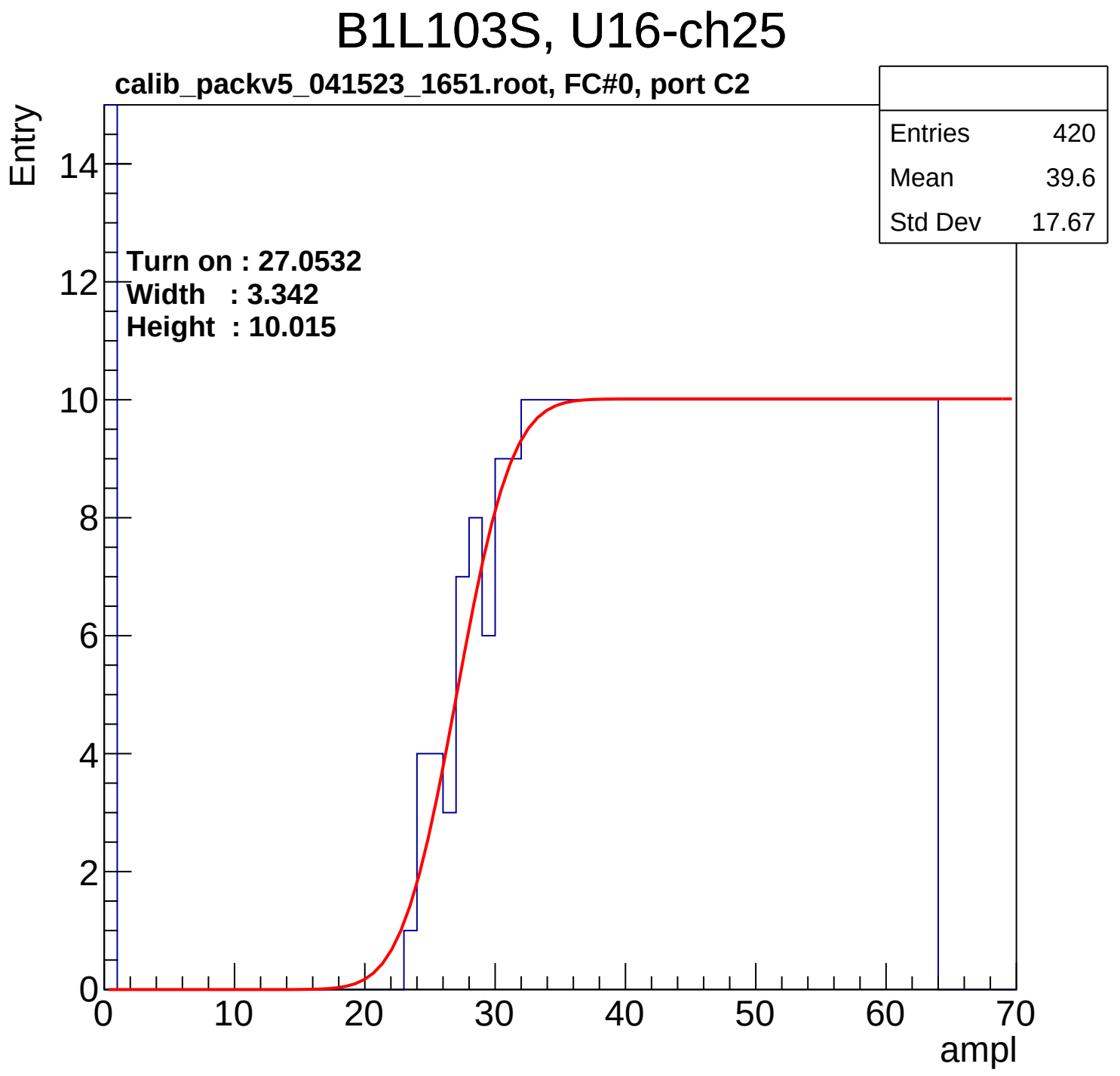
B1L103S, U16-ch25
calib_packv5_041523_1651.root, FC#0, port C2
Entries 420
Mean 39.6
Std Dev 17.67
Turn on : 27.0532
Width : 3.342
Height : 10.015
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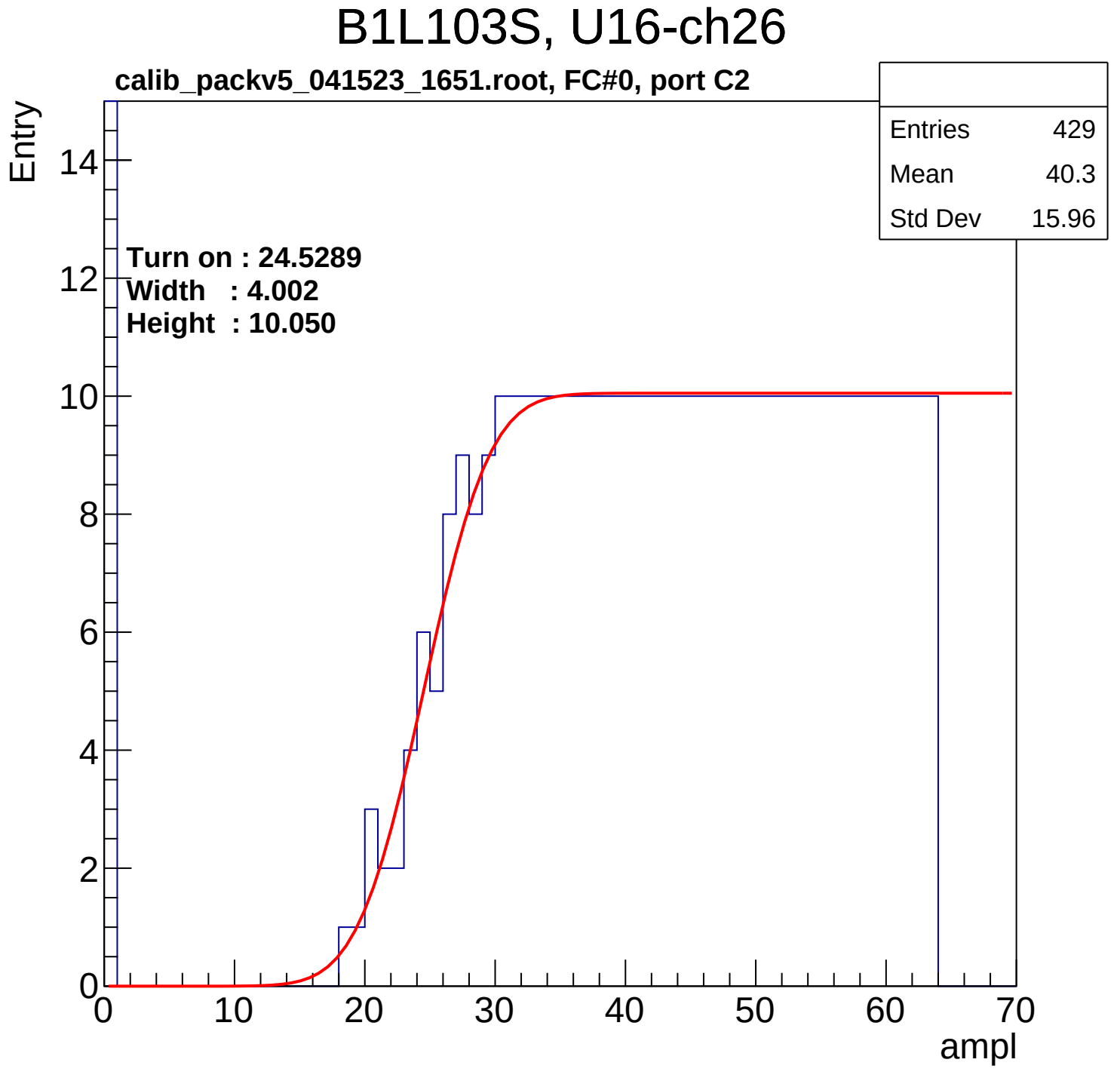
B1L103S, U16-ch26
calib_packv5_041523_1651.root, FC#0, port C2
Entries 429
Mean 40.3
Std Dev 15.96
Turn on : 24.5289
Width : 4.002
Height : 10.050
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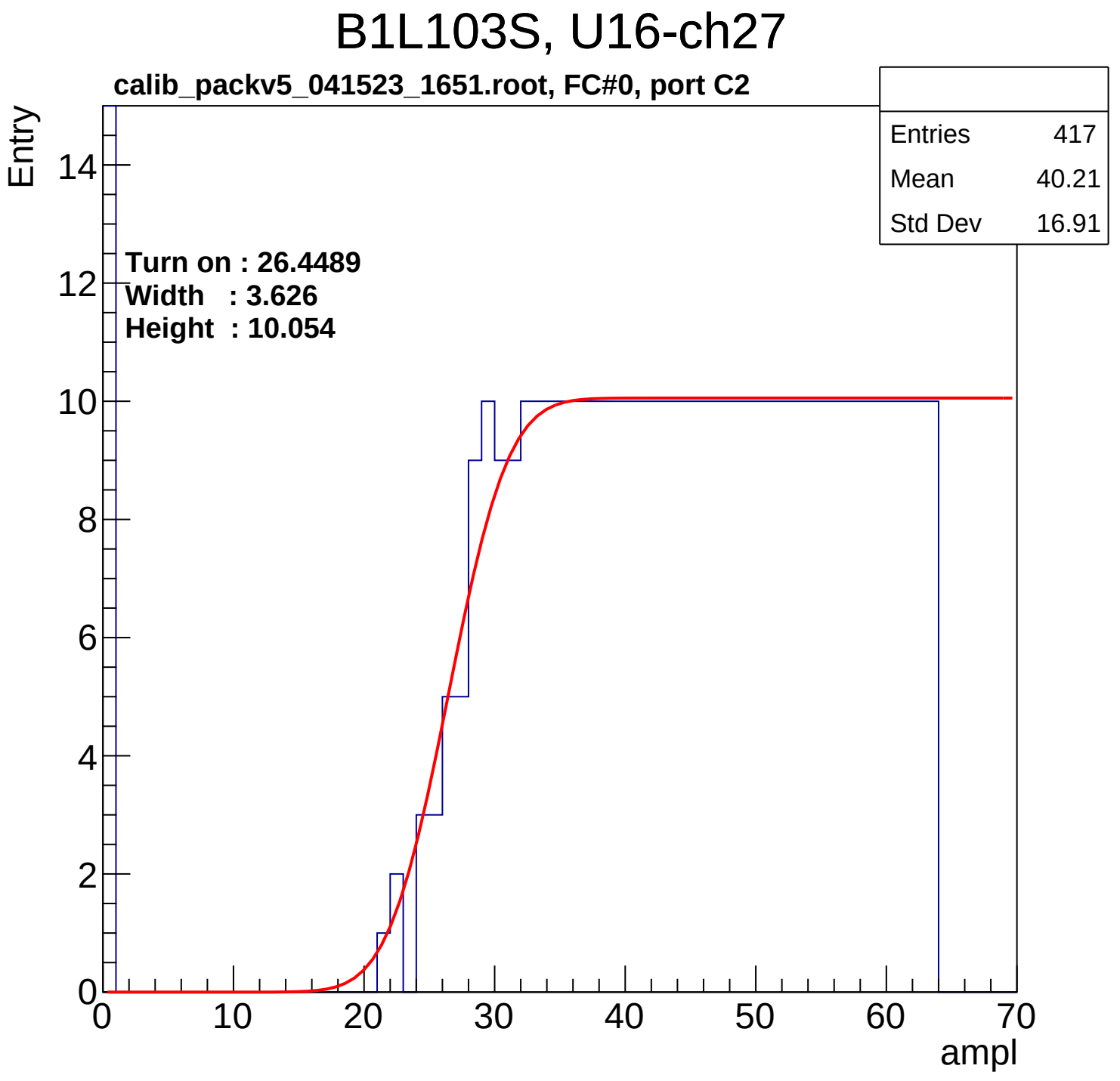
B1L103S, U16-ch27
calib_packv5_041523_1651.root, FC#0, port C2
Entries 417
Mean 40.21
Std Dev 16.91
Turn on : 26.4489
Width : 3.626
Height : 10.054
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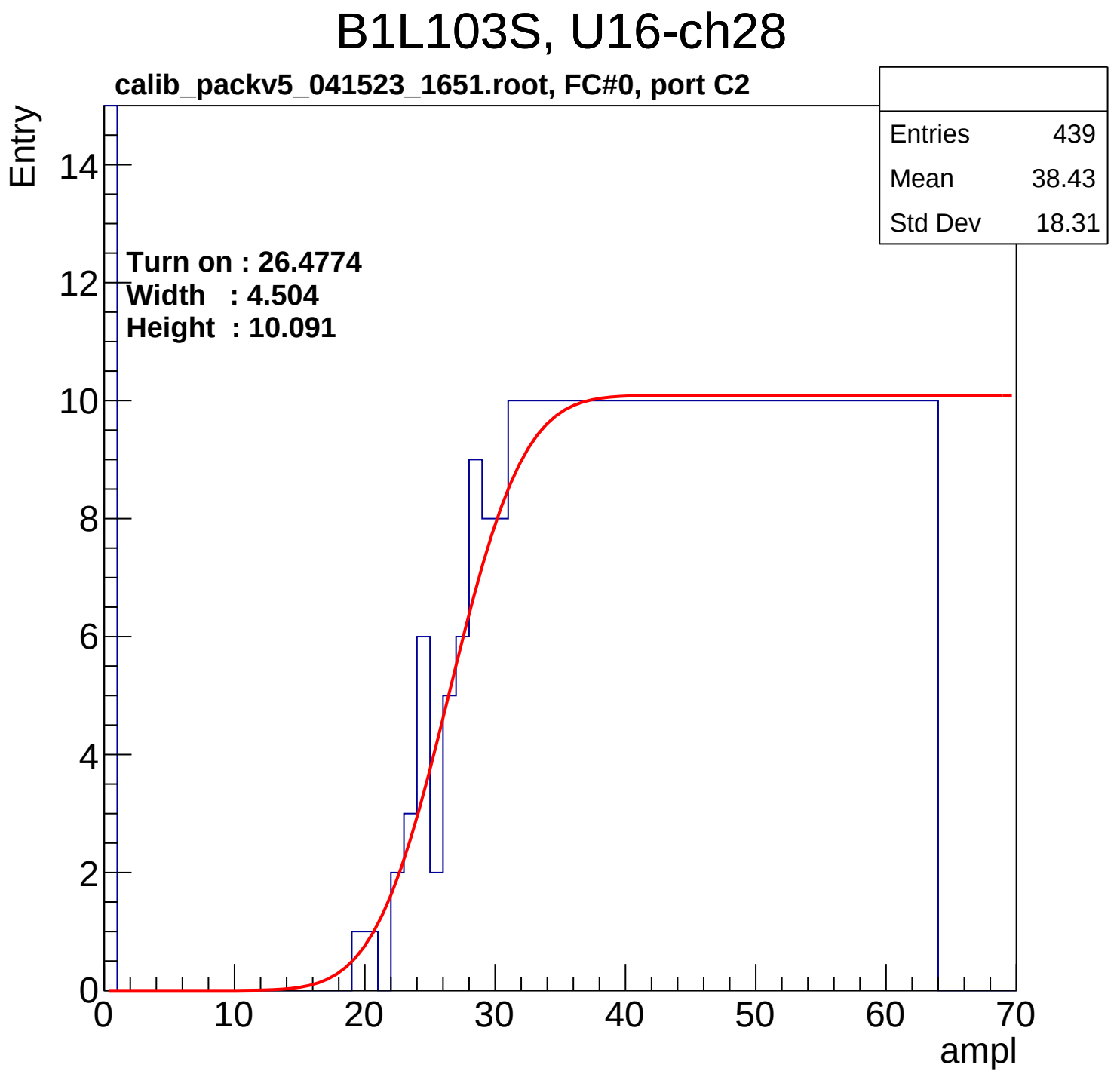
B1L103S, U16-ch28
calib_packv5_041523_1651.root, FC#0, port C2
Entries 439
Mean 38.43
Std Dev 18.31
Turn on : 26.4774
Width : 4.504
Height : 10.091
Entry
ampl
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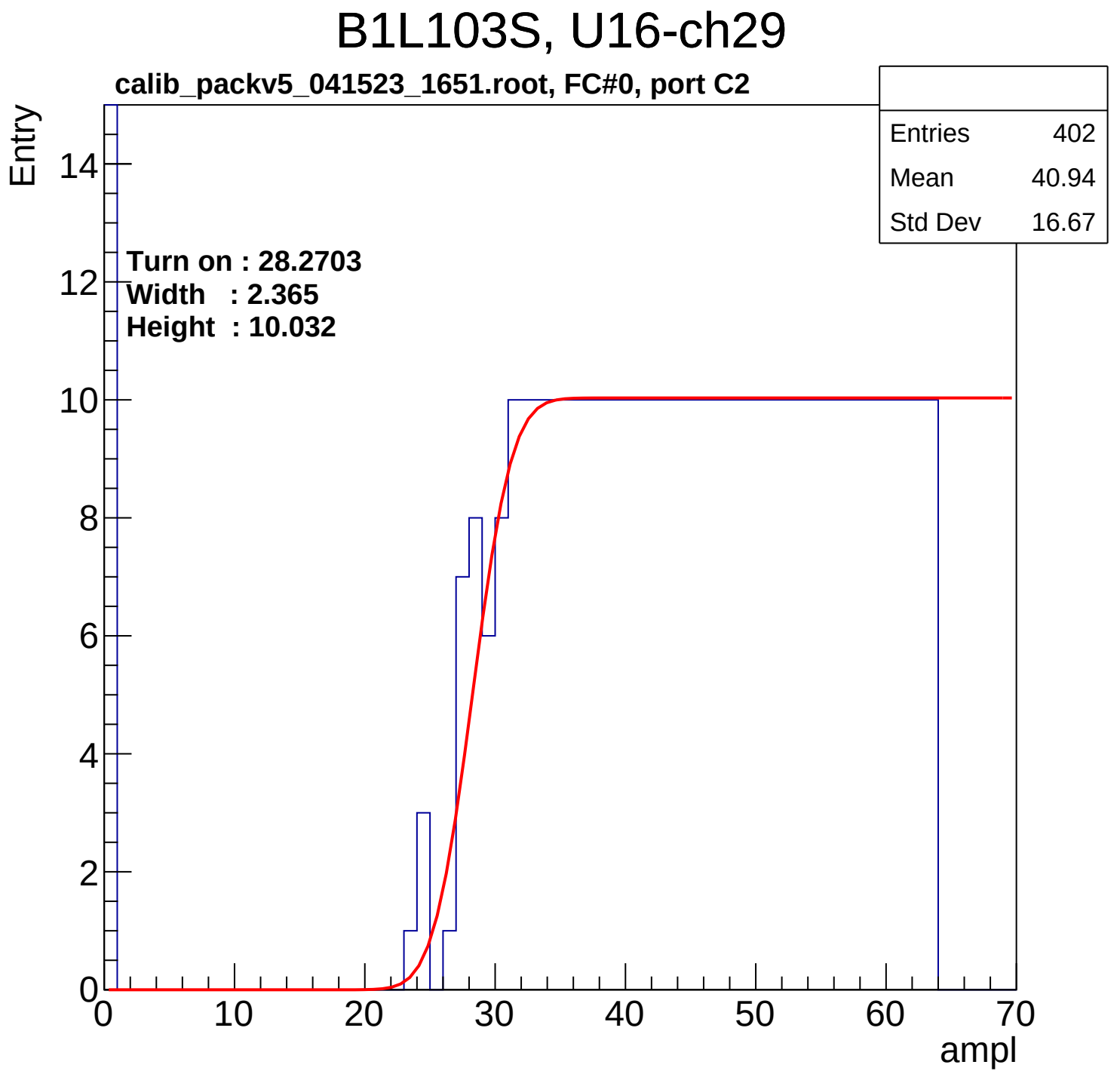
B1L103S, U16-ch29
calib_packv5_041523_1651.root, FC#0, port C2
Entries 402
Mean 40.94
Std Dev 16.67
Turn on : 28.2703
Width : 2.365
Height : 10.032
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ampl
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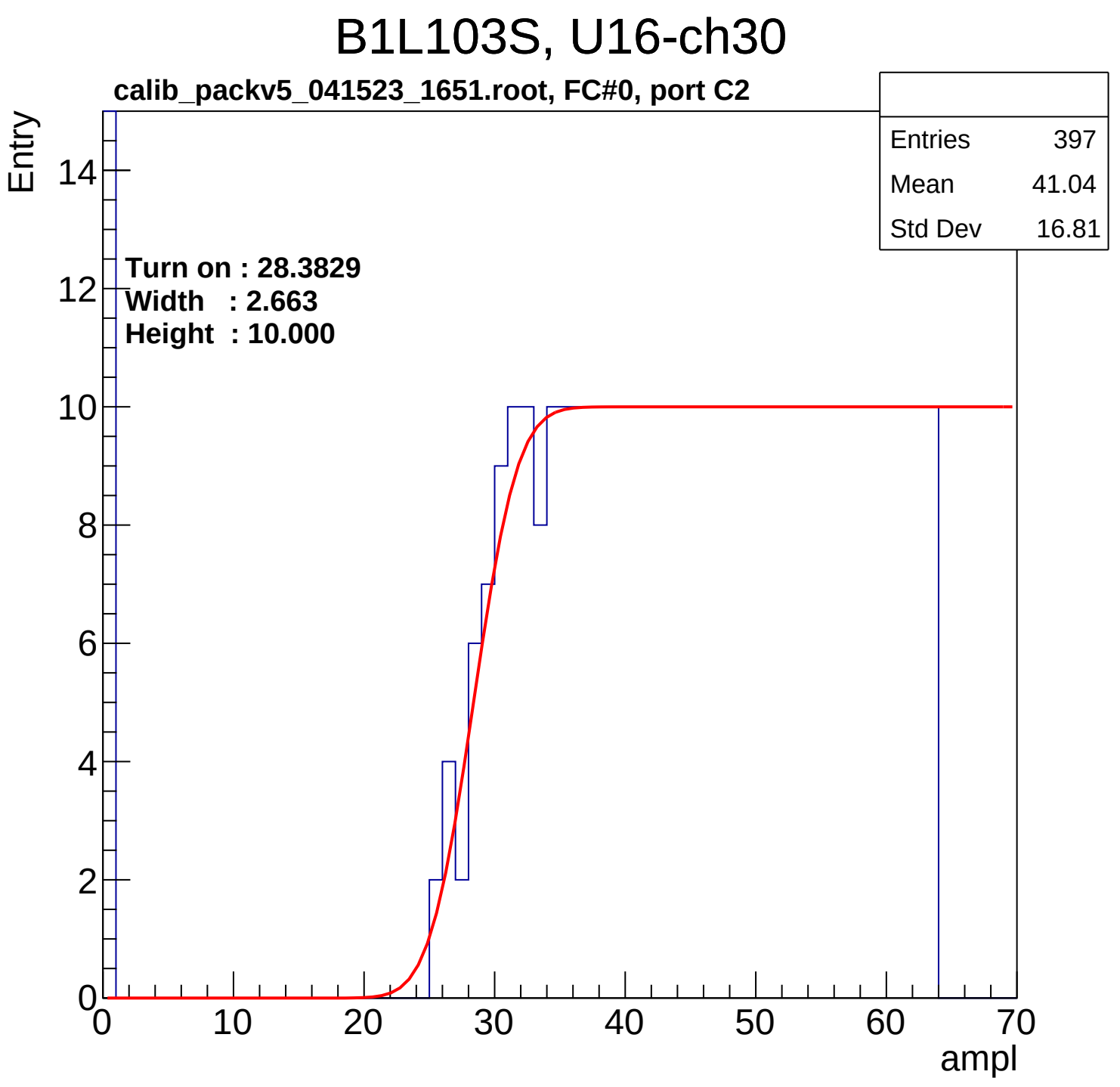
B1L103S, U16-ch30
calib_packv5_041523_1651.root, FC#0, port C2
Entries 397
Mean 41.04
Std Dev 16.81
Turn on : 28.3829
Width : 2.663
Height : 10.000
Entry
ampl
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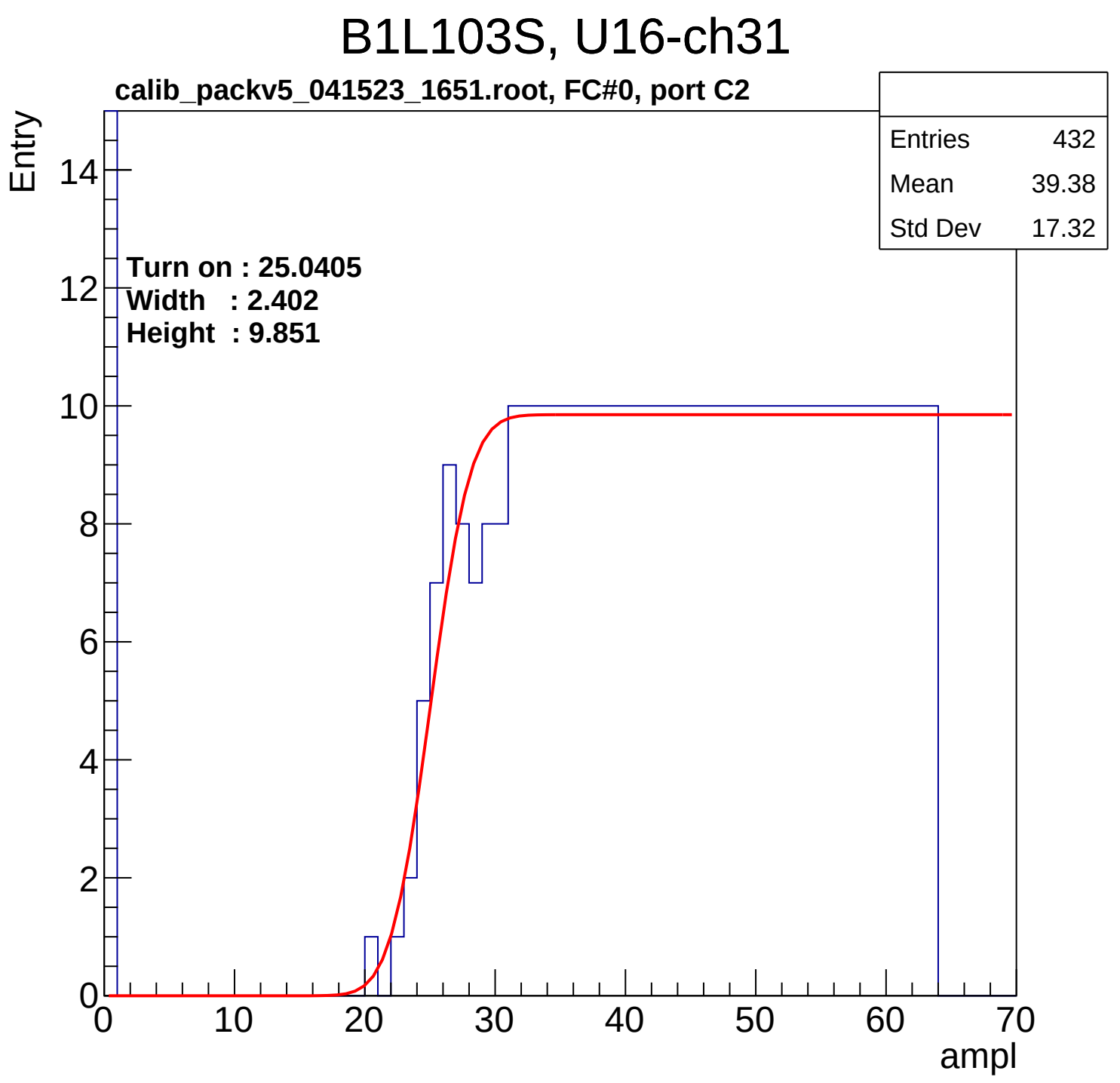
B1L103S, U16-ch31
calib_packv5_041523_1651.root, FC#0, port C2
Entries 432
Mean 39.38
Std Dev 17.32
Turn on : 25.0405
Width : 2.402
Height : 9.851
Entry
ampl
0
2
4
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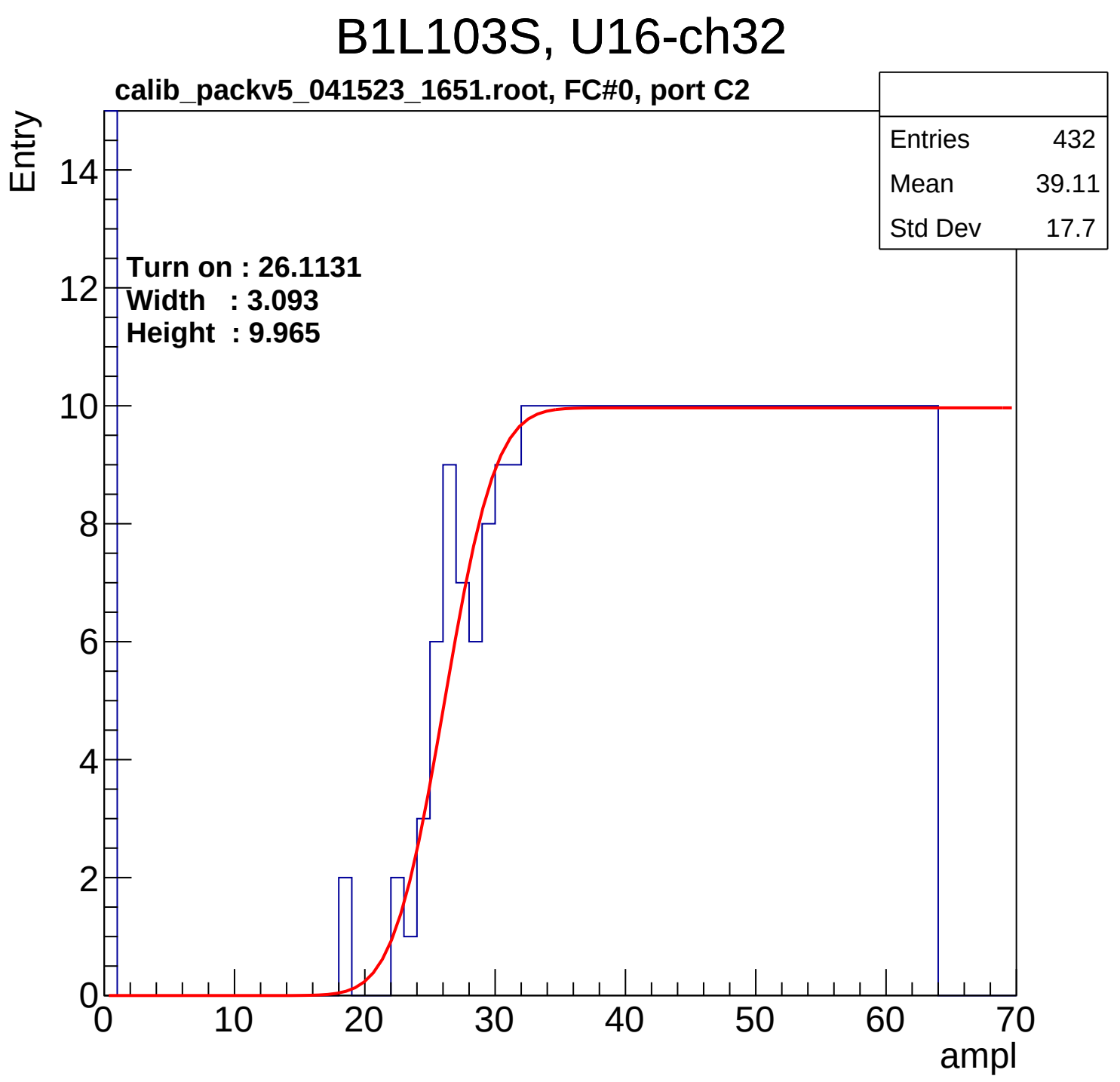
B1L103S, U16-ch32
calib_packv5_041523_1651.root, FC#0, port C2
Entries 432
Mean 39.11
Std Dev 17.7
Turn on : 26.1131
Width : 3.093
Height : 9.965
Entry
ampl
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6
8
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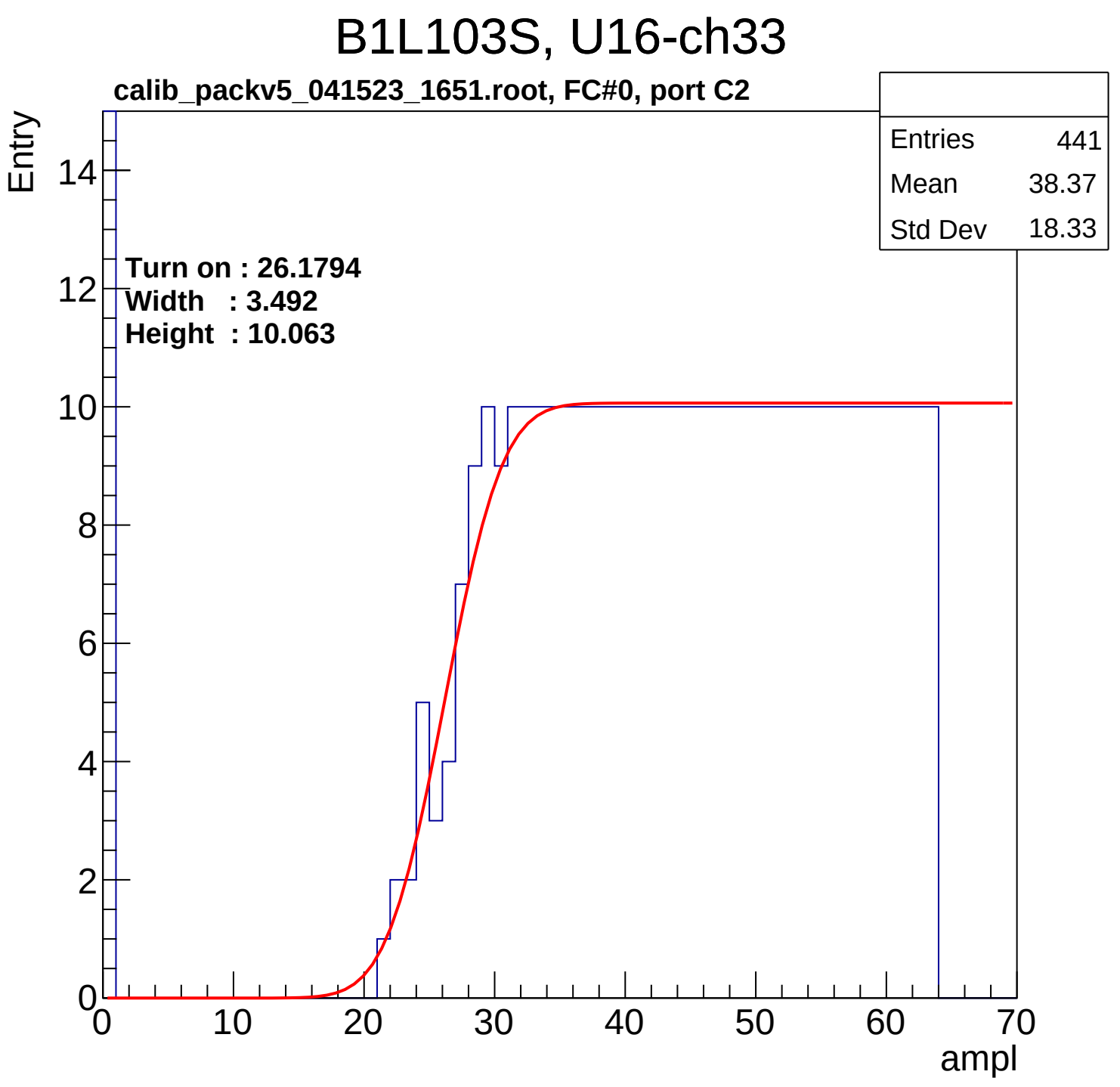
B1L103S, U16-ch33
calib_packv5_041523_1651.root, FC#0, port C2
Entries 441
Mean 38.37
Std Dev 18.33
Turn on : 26.1794
Width : 3.492
Height : 10.063
Entry
ampl
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4
6
8
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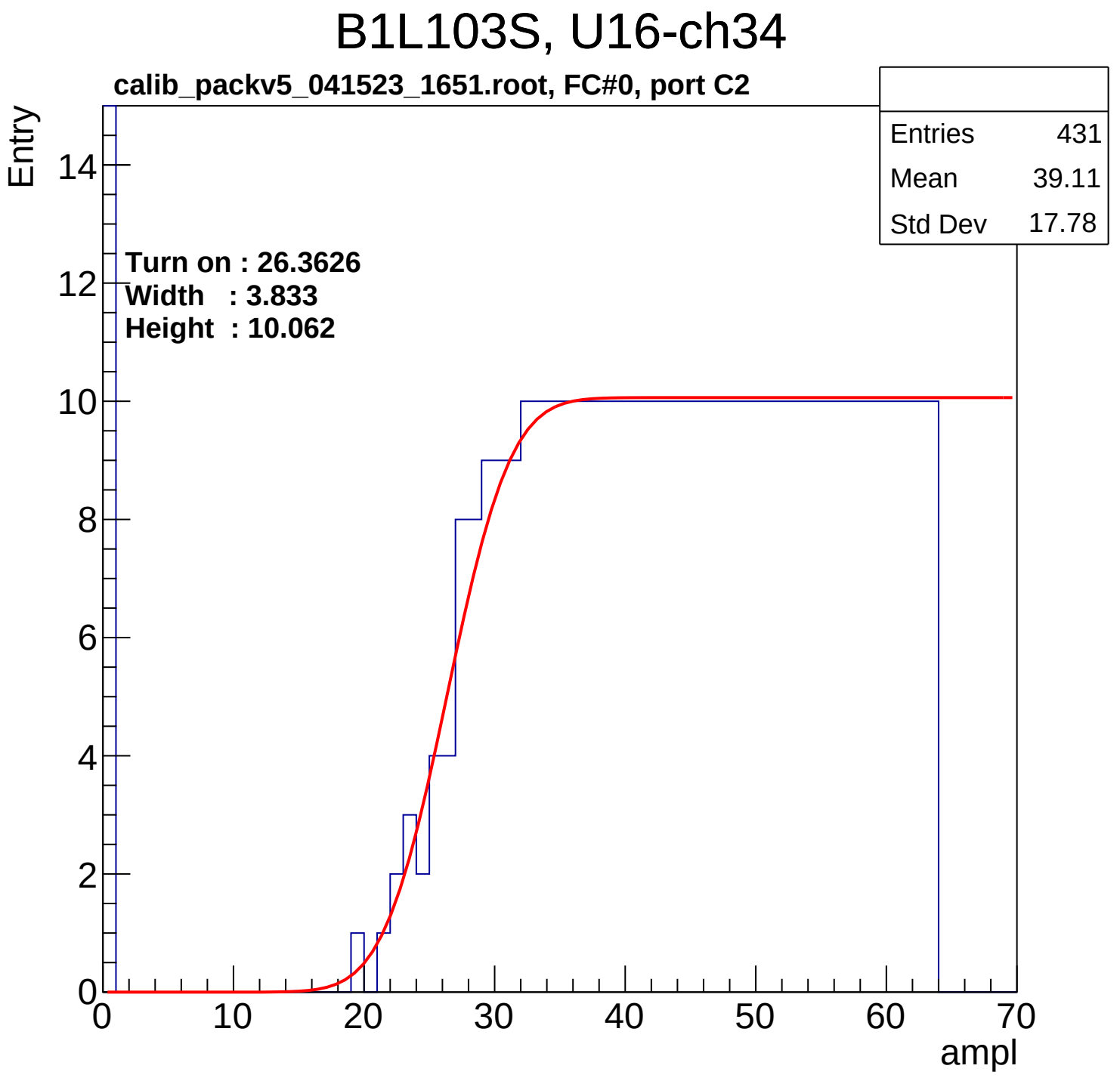
B1L103S, U16-ch34
calib_packv5_041523_1651.root, FC#0, port C2
Entries 431
Mean 39.11
Std Dev 17.78
Turn on : 26.3626
Width : 3.833
Height : 10.062
Entry
ampl
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6
8
10
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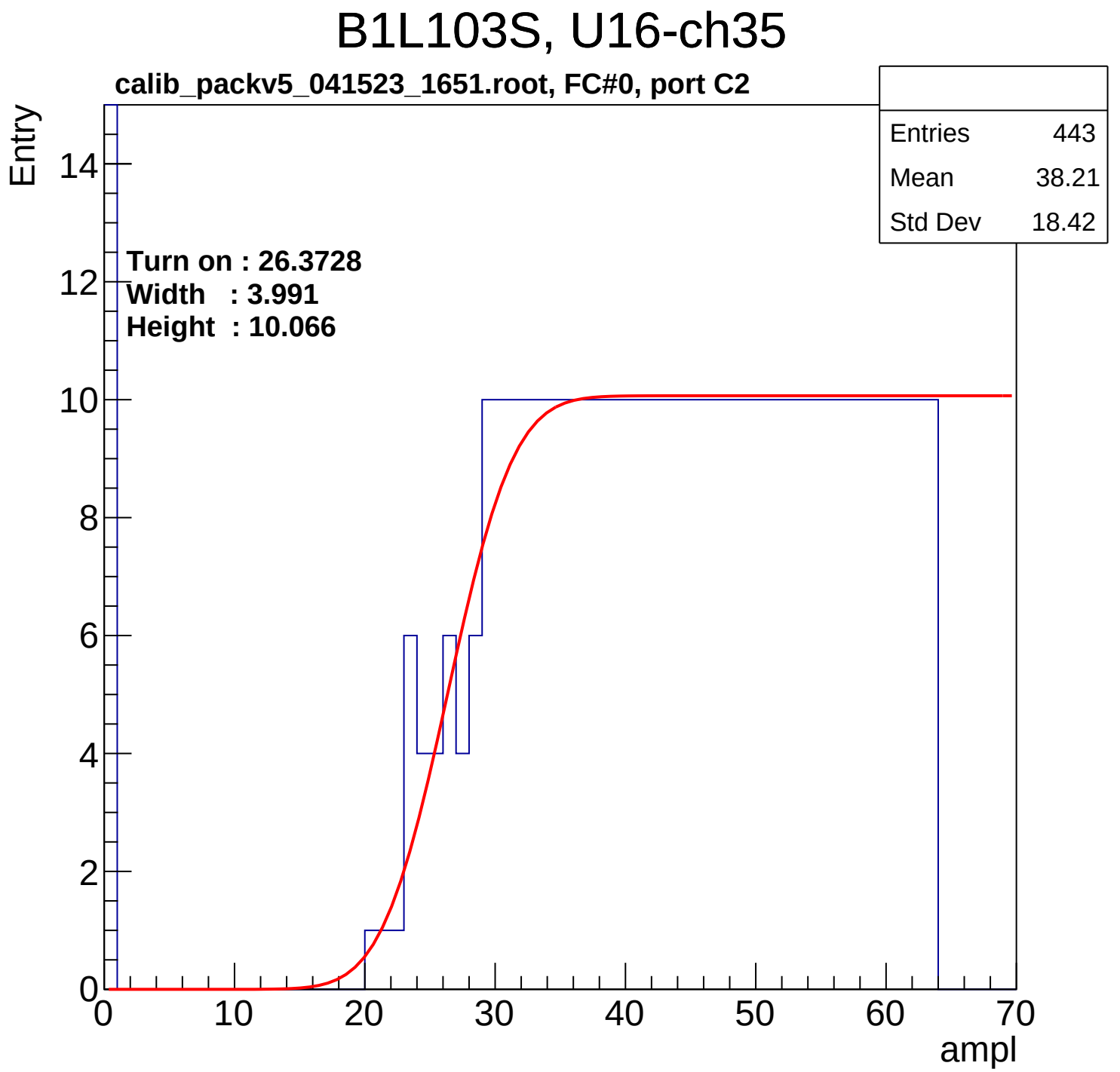
B1L103S, U16-ch35
calib_packv5_041523_1651.root, FC#0, port C2
Entries 443
Mean 38.21
Std Dev 18.42
Turn on : 26.3728
Width : 3.991
Height : 10.066
Entry
ampl
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4
6
8
10
12
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0
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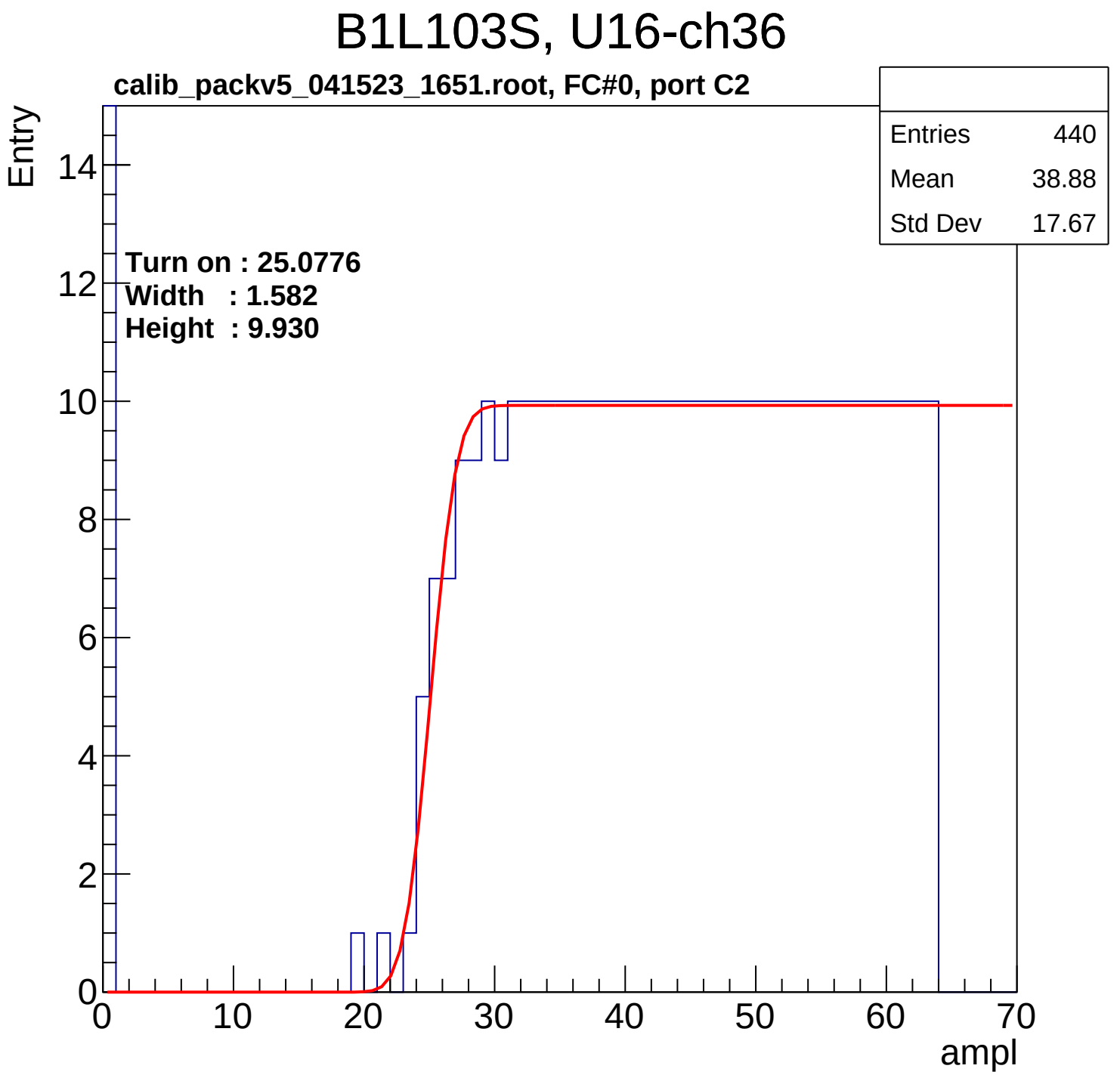
B1L103S, U16-ch36
calib_packv5_041523_1651.root, FC#0, port C2
Entries 440
Mean 38.88
Std Dev 17.67
Turn on : 25.0776
Width : 1.582
Height : 9.930
Entry
ampl
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2
4
6
8
10
12
14
0
10
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40
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60
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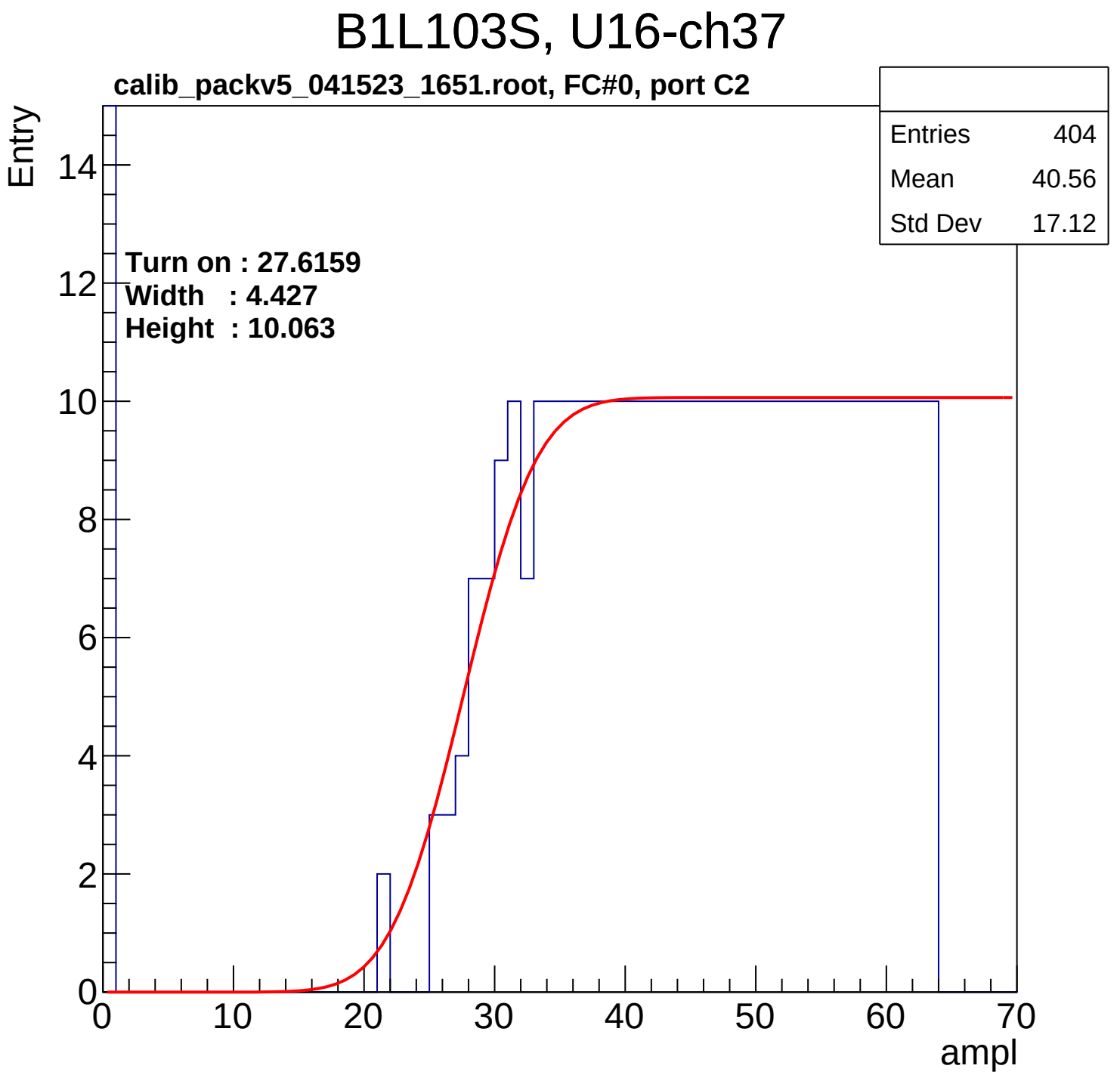
B1L103S, U16-ch37
calib_packv5_041523_1651.root, FC#0, port C2
Entries 404
Mean 40.56
Std Dev 17.12
Turn on : 27.6159
Width : 4.427
Height : 10.063
Entry
ampl
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2
4
6
8
10
12
14
0
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20
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60
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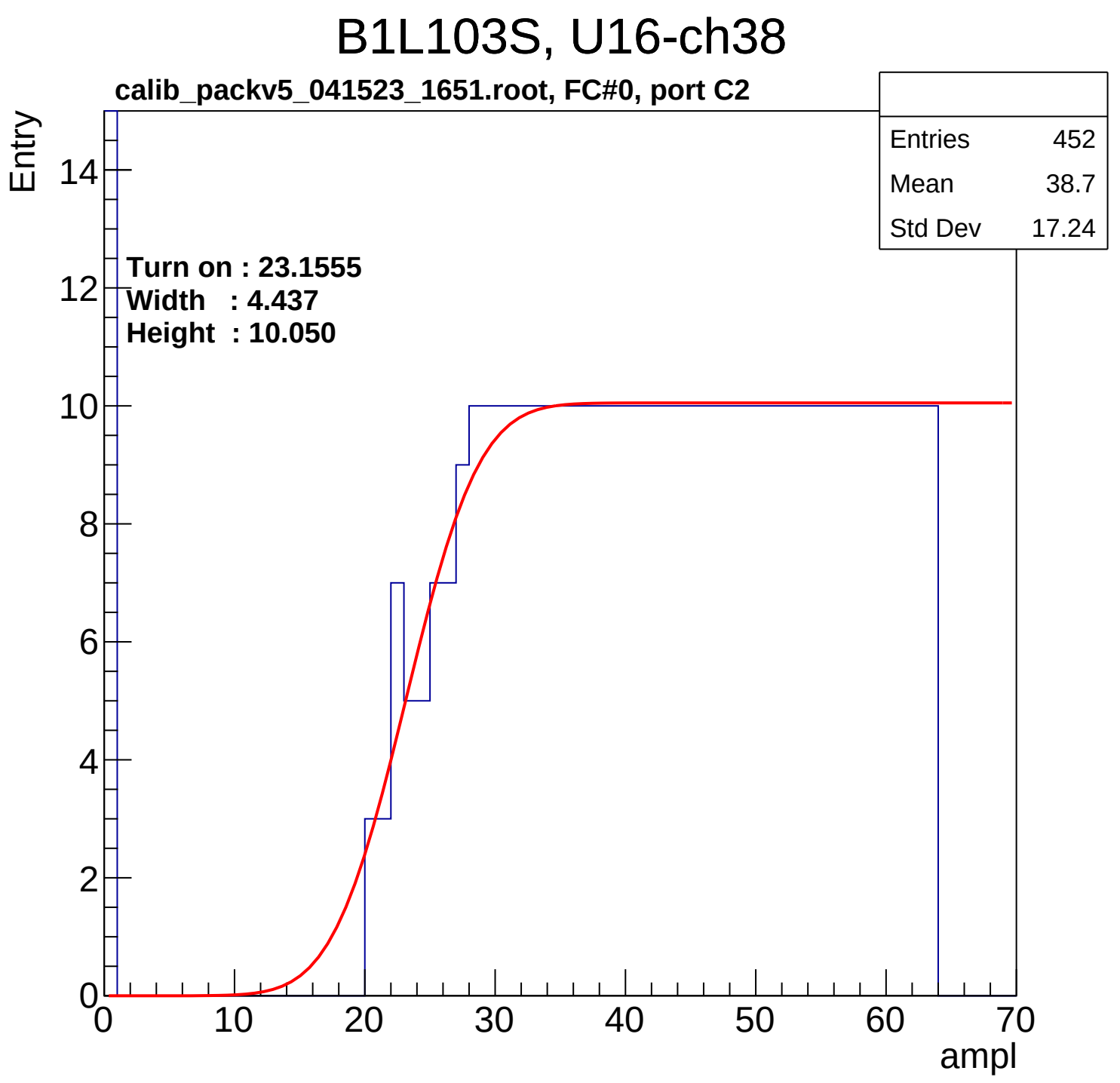
B1L103S, U16-ch38
calib_packv5_041523_1651.root, FC#0, port C2
Entries 452
Mean 38.7
Std Dev 17.24
Turn on : 23.1555
Width : 4.437
Height : 10.050
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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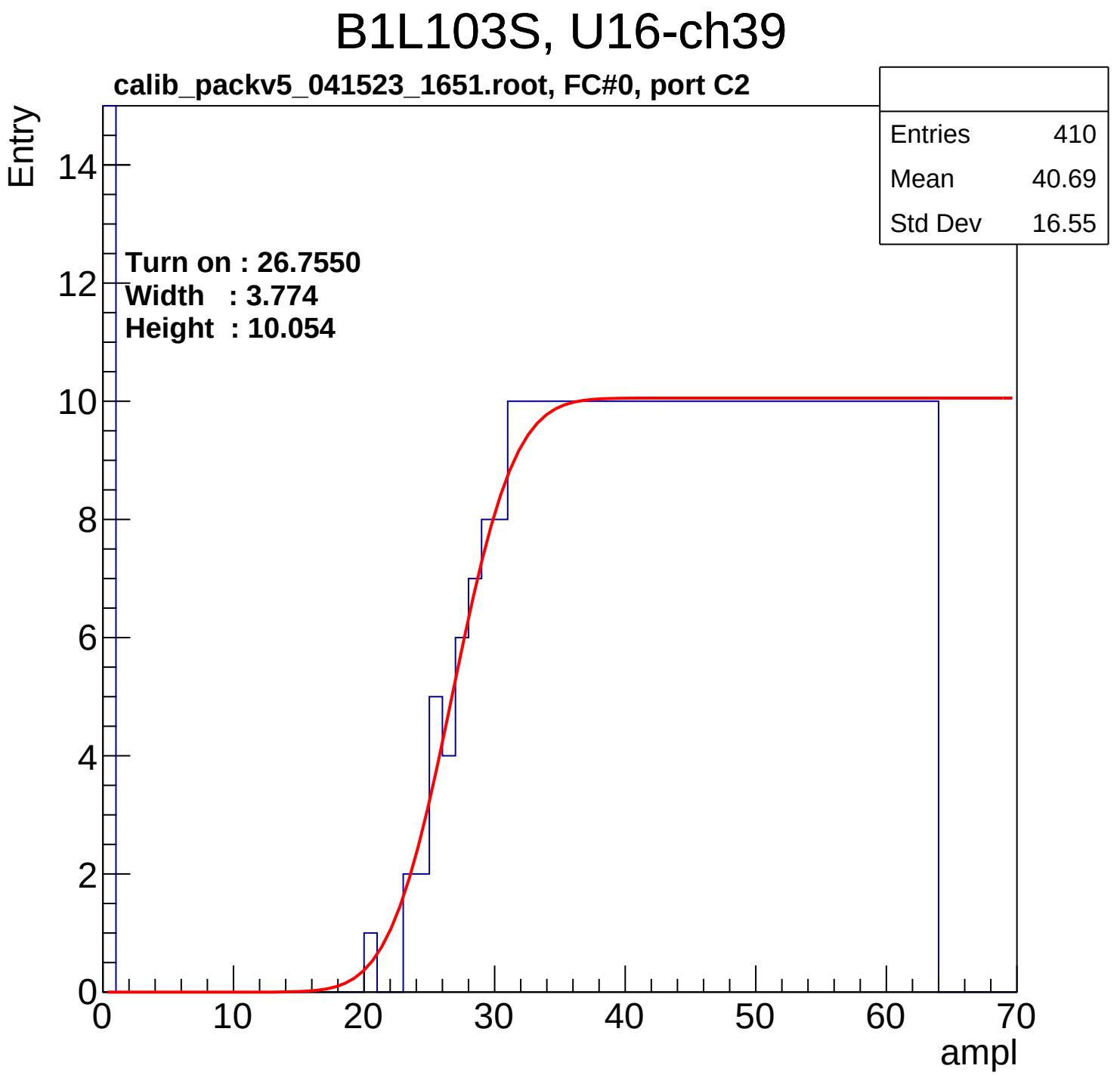
B1L103S, U16-ch39
calib_packv5_041523_1651.root, FC#0, port C2
Entries 410
Mean 40.69
Std Dev 16.55
Turn on : 26.7550
Width : 3.774
Height : 10.054
Entry
ampl
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6
8
10
12
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0
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20
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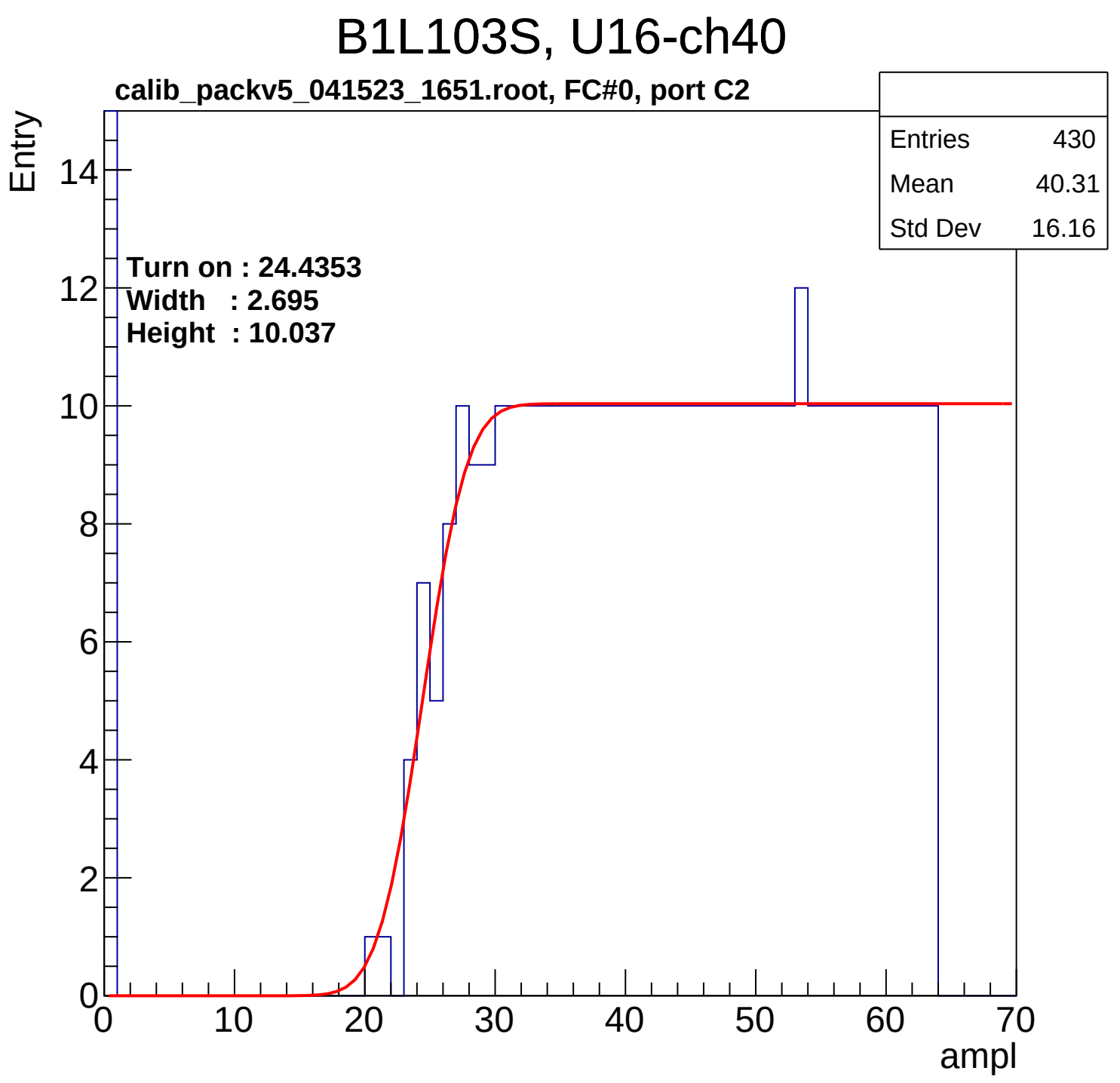
B1L103S, U16-ch40
calib_packv5_041523_1651.root, FC#0, port C2
Entries 430
Mean 40.31
Std Dev 16.16
Turn on : 24.4353
Width : 2.695
Height : 10.037
Entry
ampl
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6
8
10
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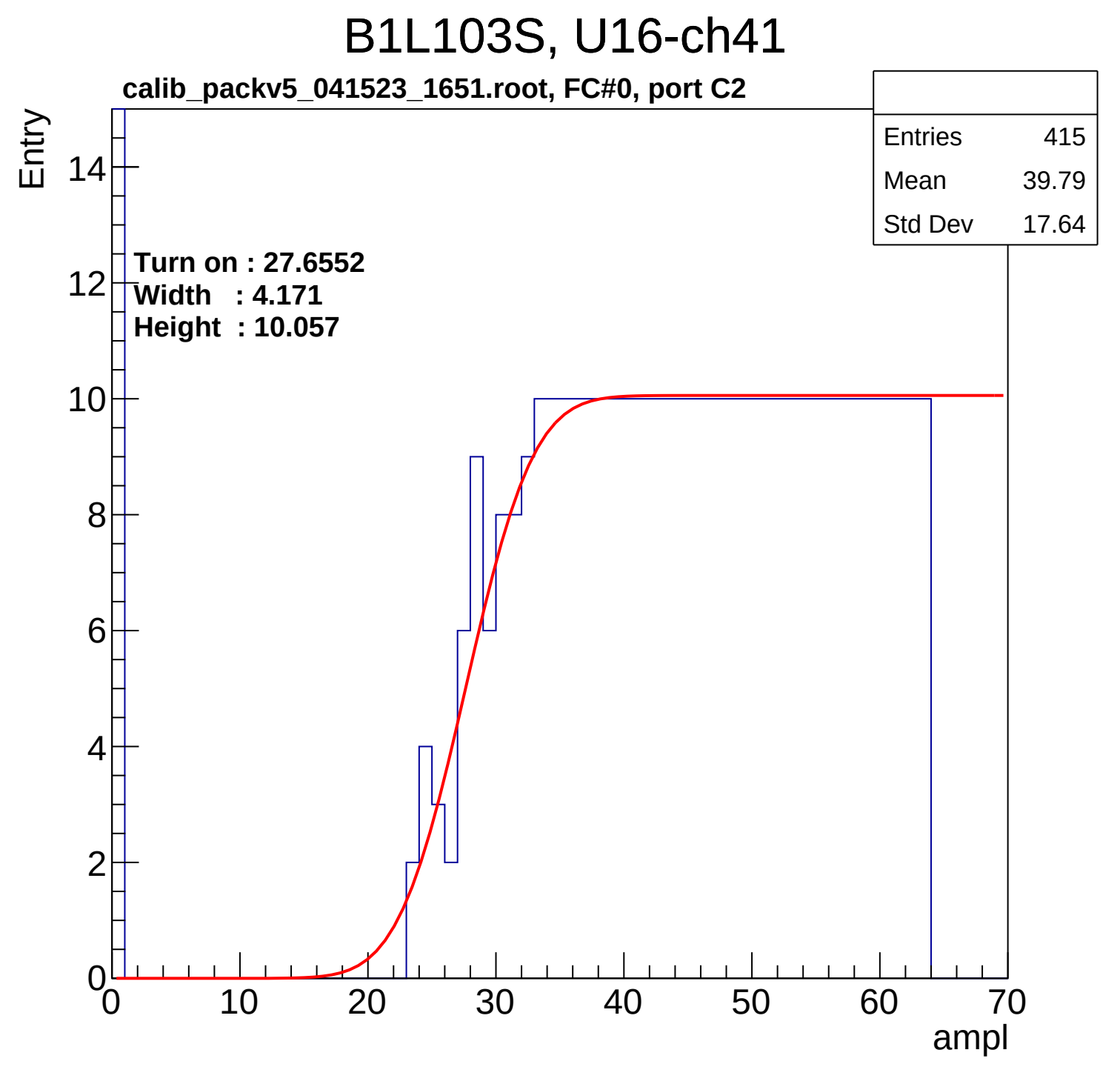
B1L103S, U16-ch41
calib_packv5_041523_1651.root, FC#0, port C2
Entries 415
Mean 39.79
Std Dev 17.64
Turn on : 27.6552
Width : 4.171
Height : 10.057
Entry
ampl
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2
4
6
8
10
12
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0
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20
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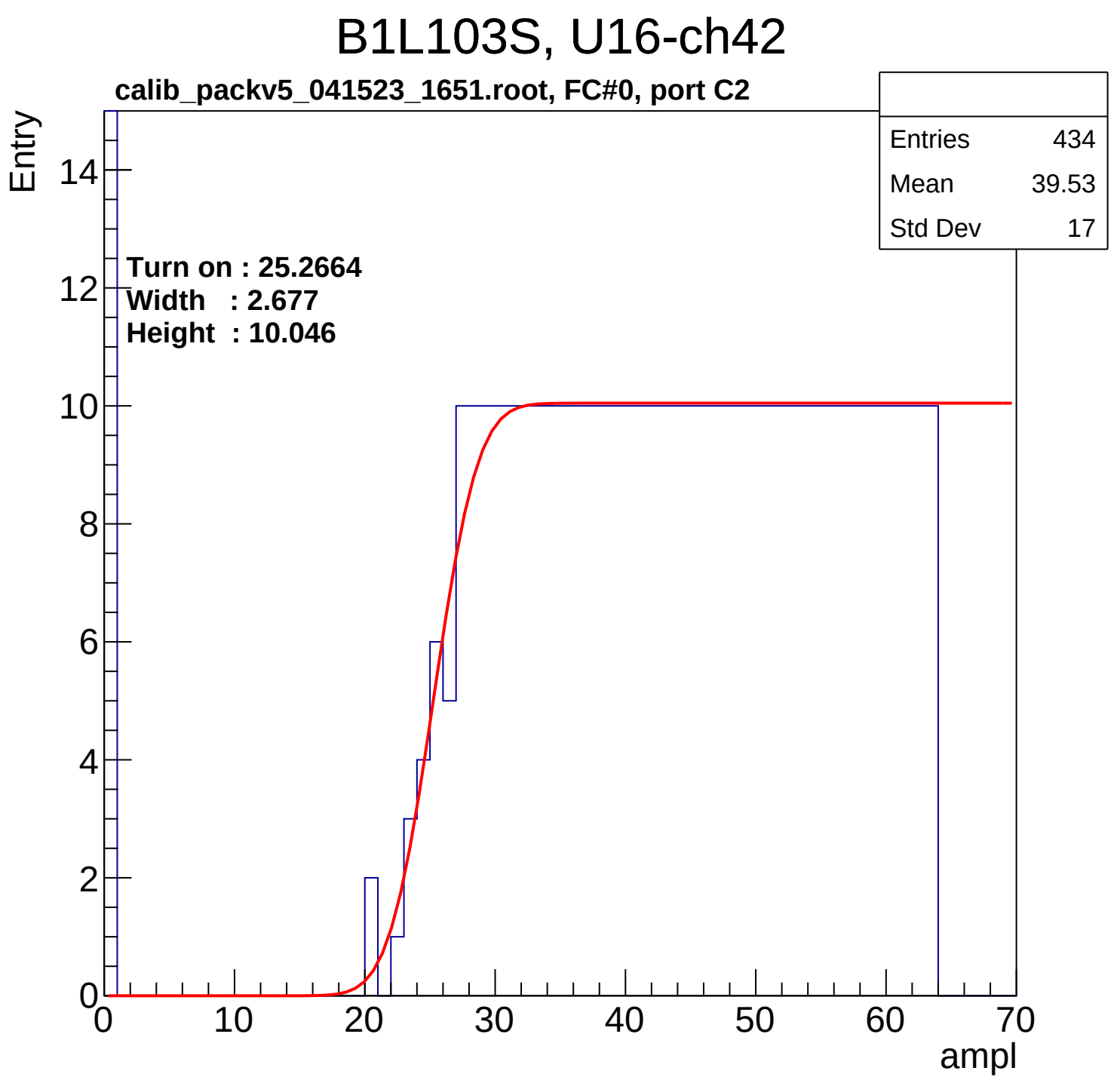
B1L103S, U16-ch42
calib_packv5_041523_1651.root, FC#0, port C2
Entries 434
Mean 39.53
Std Dev 17
Turn on : 25.2664
Width : 2.677
Height : 10.046
Entry
ampl
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6
8
10
12
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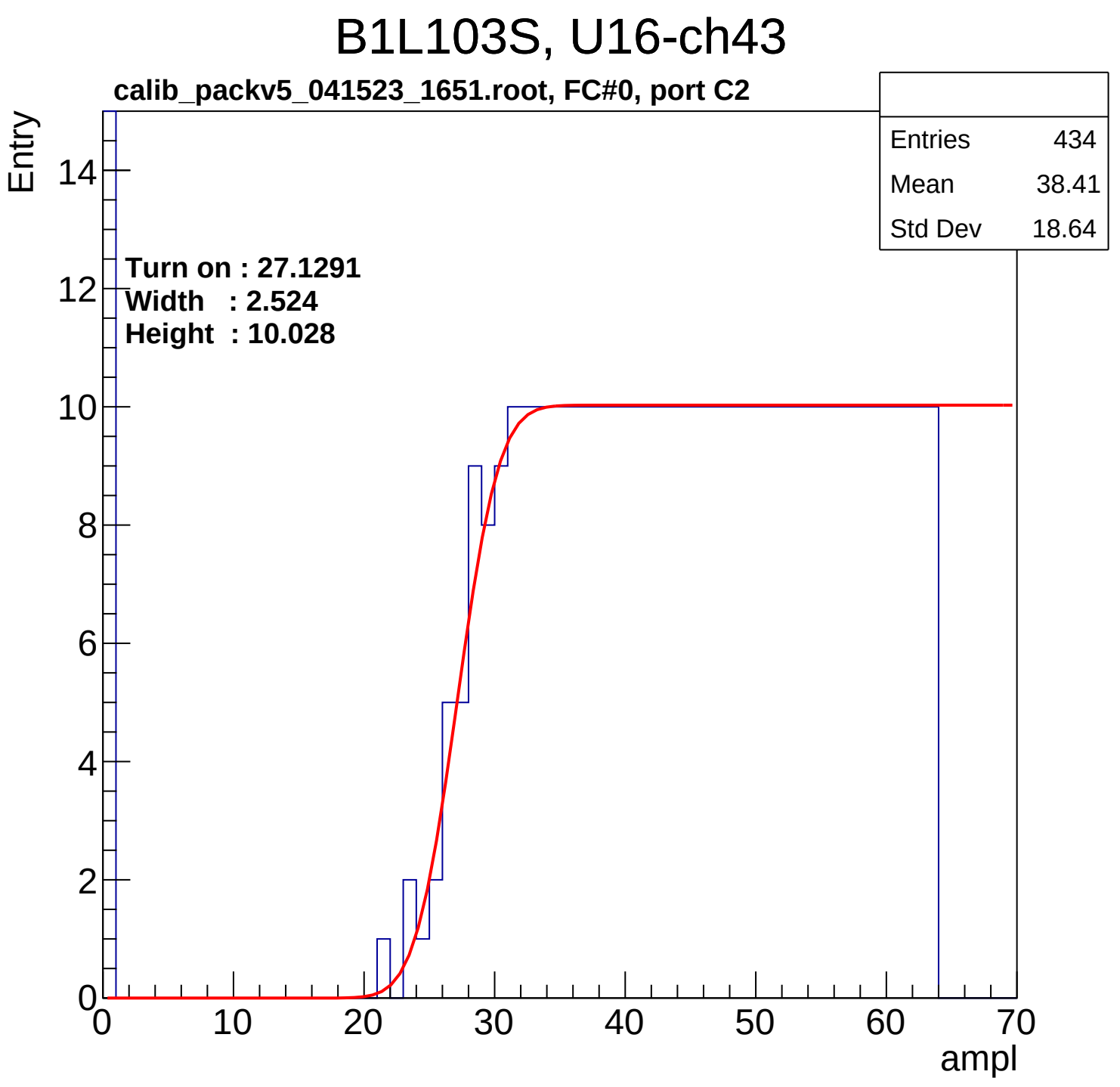
B1L103S, U16-ch43
calib_packv5_041523_1651.root, FC#0, port C2
Entries 434
Mean 38.41
Std Dev 18.64
Turn on : 27.1291
Width : 2.524
Height : 10.028
Entry
ampl
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4
6
8
10
12
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0
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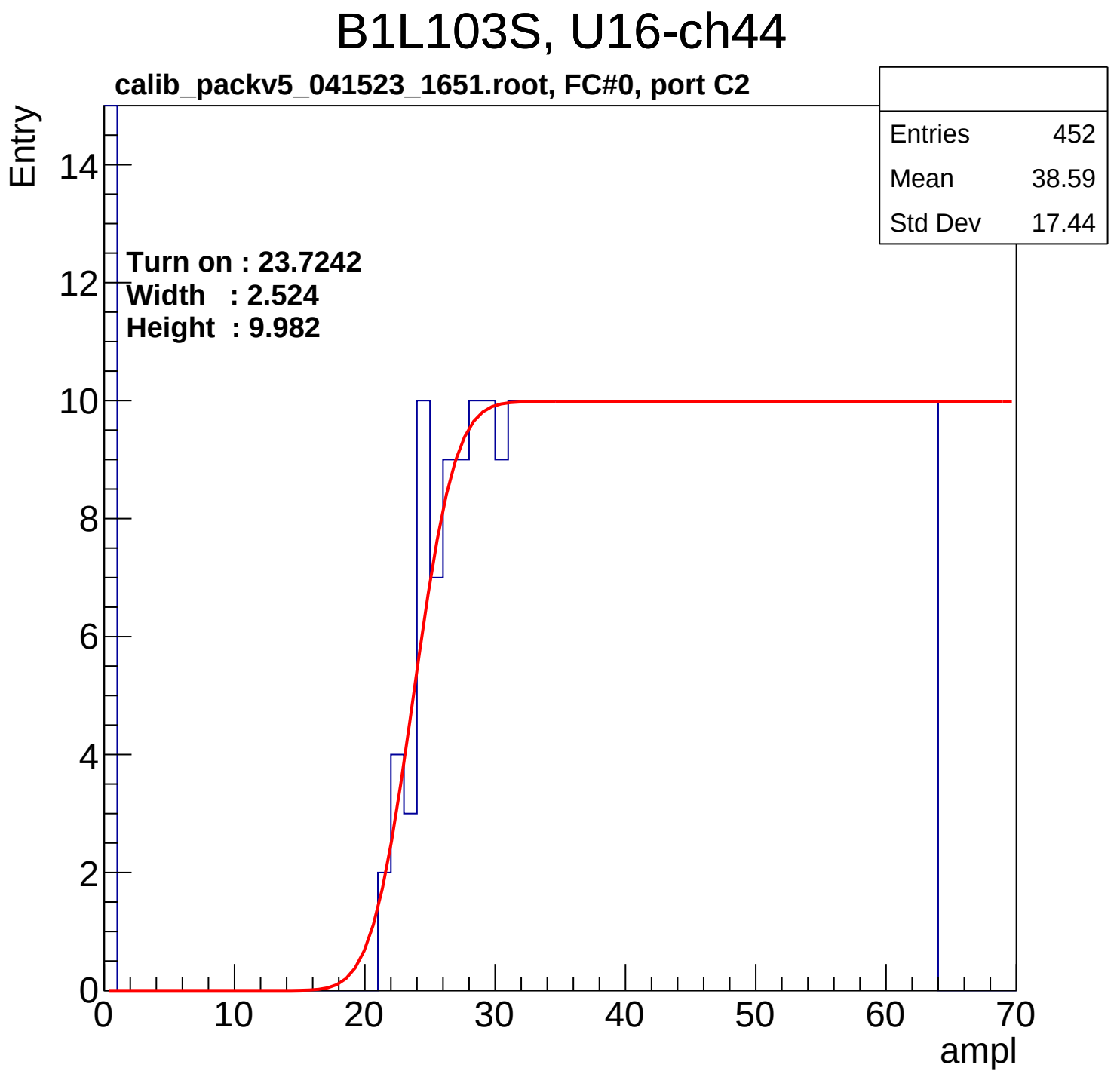
B1L103S, U16-ch44
calib_packv5_041523_1651.root, FC#0, port C2
Entries 452
Mean 38.59
Std Dev 17.44
Turn on : 23.7242
Width : 2.524
Height : 9.982
Entry
ampl
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6
8
10
12
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10
20
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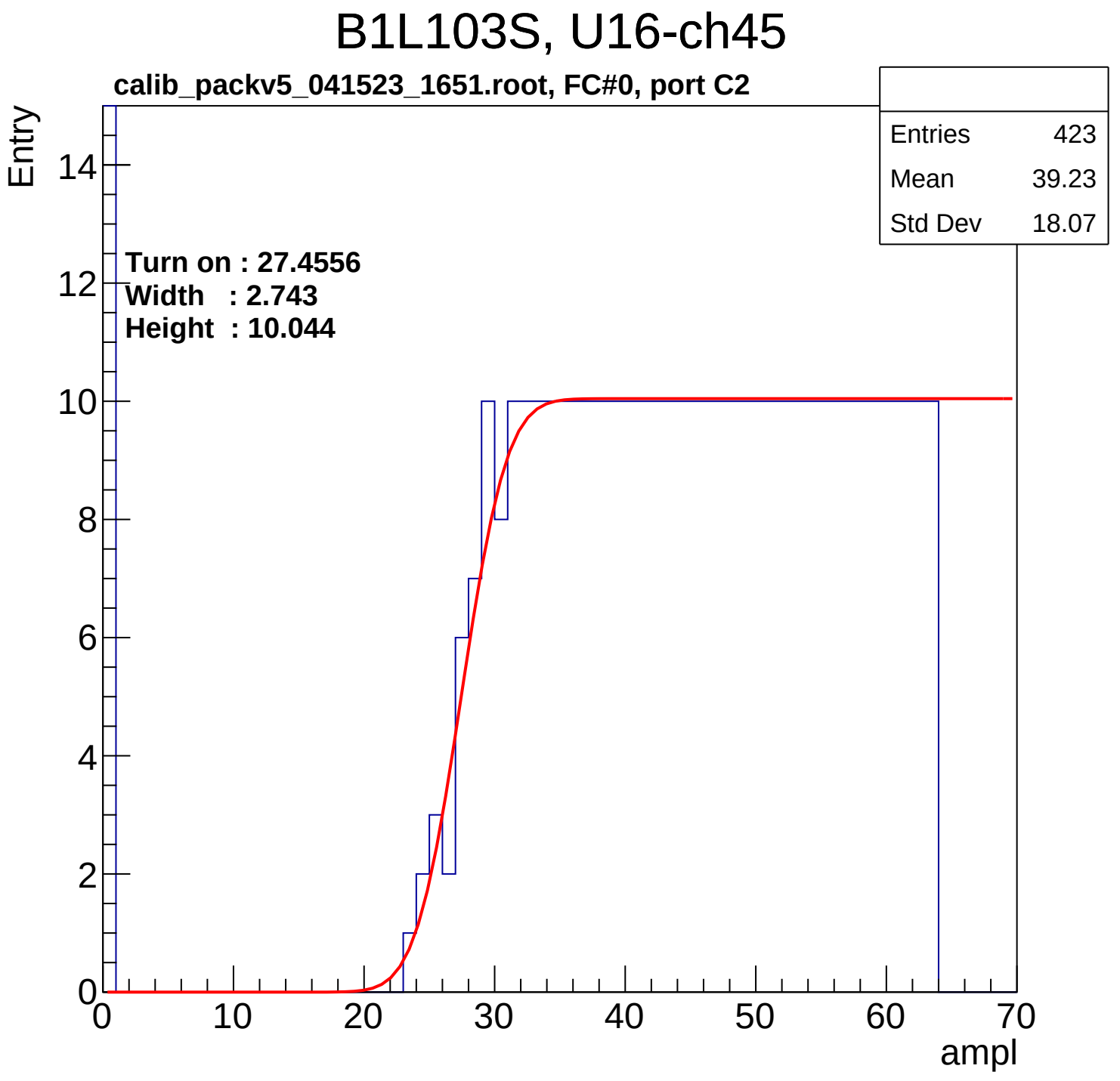
B1L103S, U16-ch45
calib_packv5_041523_1651.root, FC#0, port C2
Entries 423
Mean 39.23
Std Dev 18.07
Turn on : 27.4556
Width : 2.743
Height : 10.044
Entry
ampl
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6
8
10
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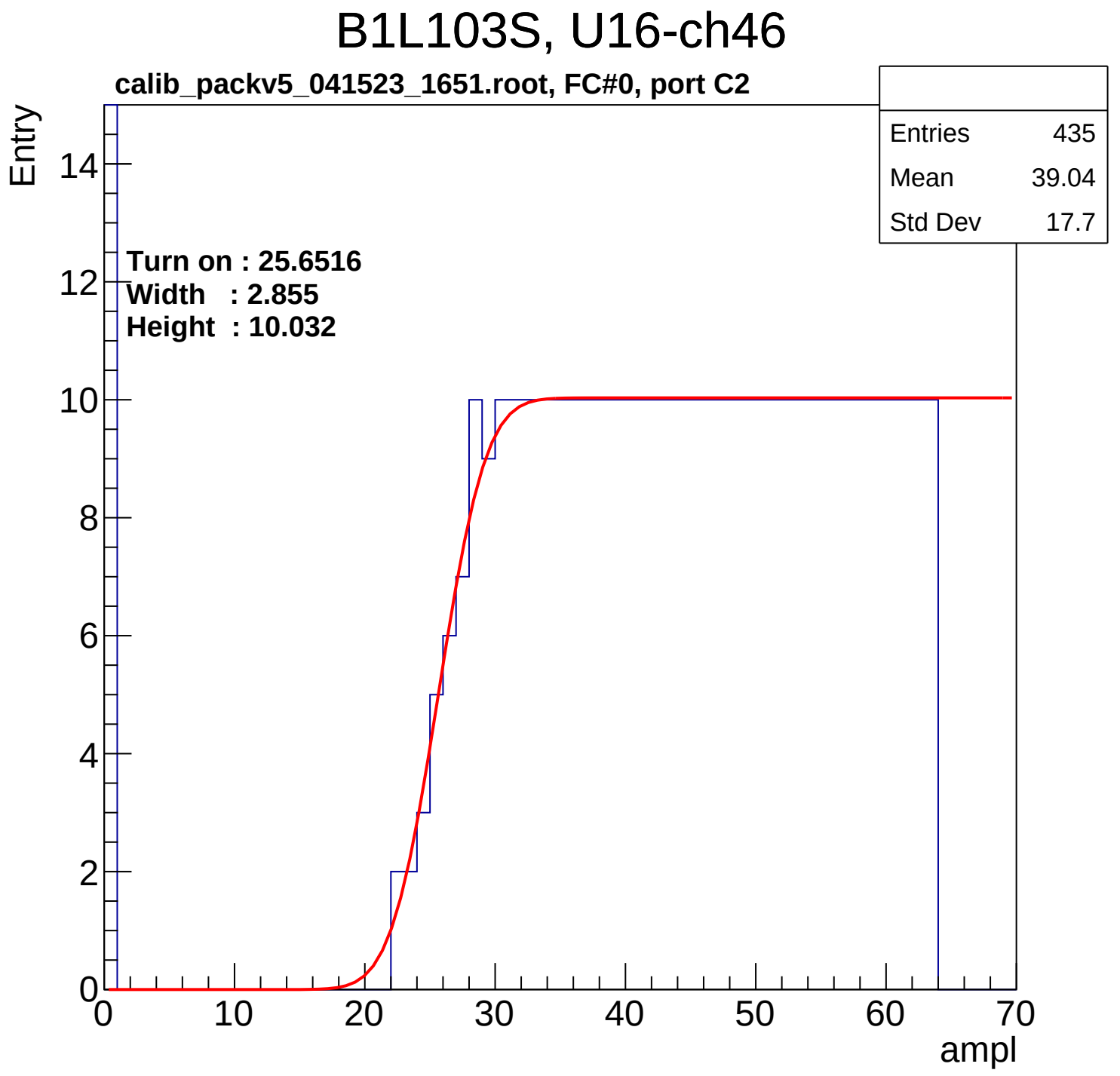
B1L103S, U16-ch46
calib_packv5_041523_1651.root, FC#0, port C2
Entries 435
Mean 39.04
Std Dev 17.7
Turn on : 25.6516
Width : 2.855
Height : 10.032
Entry
ampl
0
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6
8
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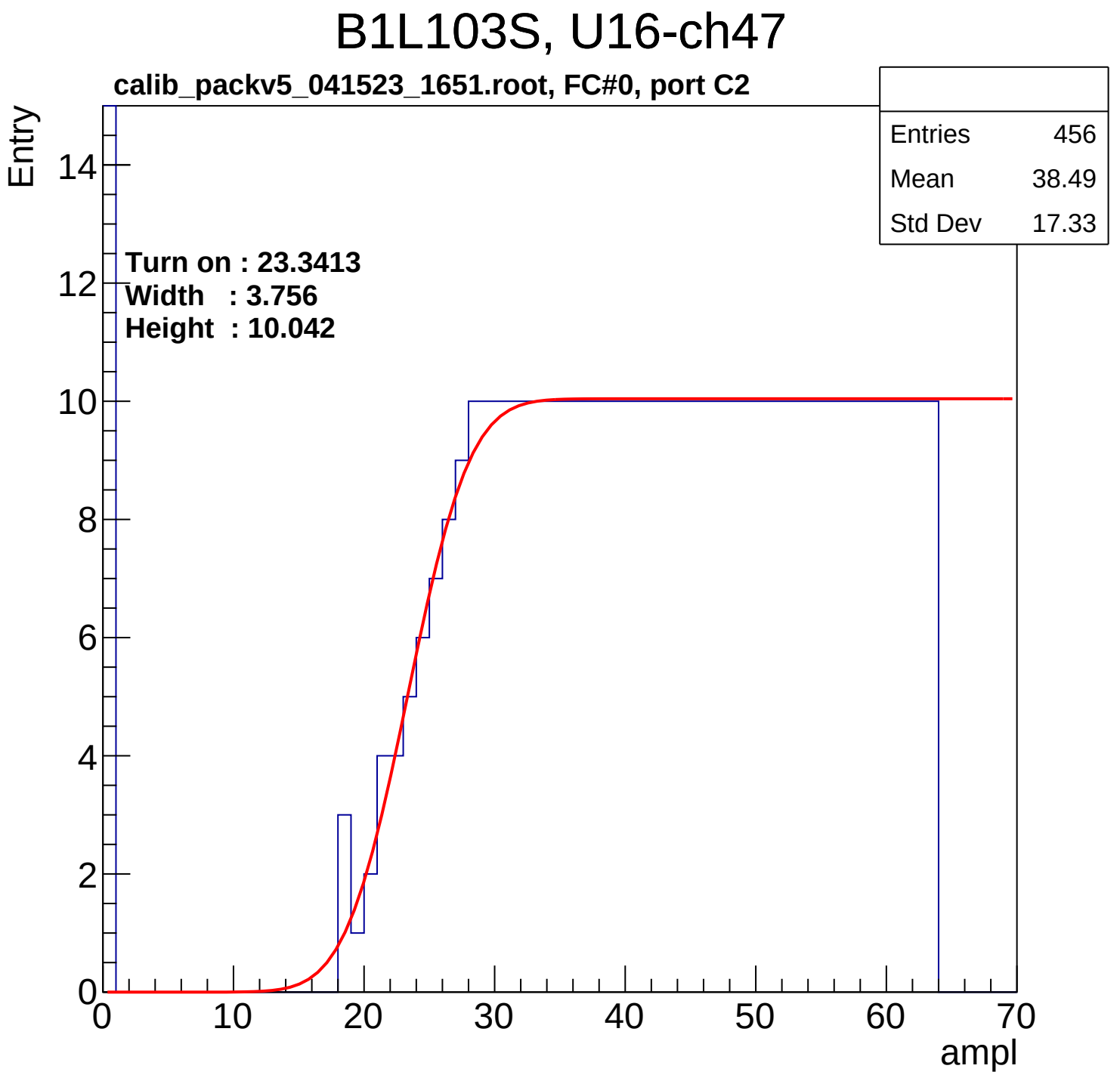
B1L103S, U16-ch47
calib_packv5_041523_1651.root, FC#0, port C2
Entries 456
Mean 38.49
Std Dev 17.33
Turn on : 23.3413
Width : 3.756
Height : 10.042
Entry
ampl
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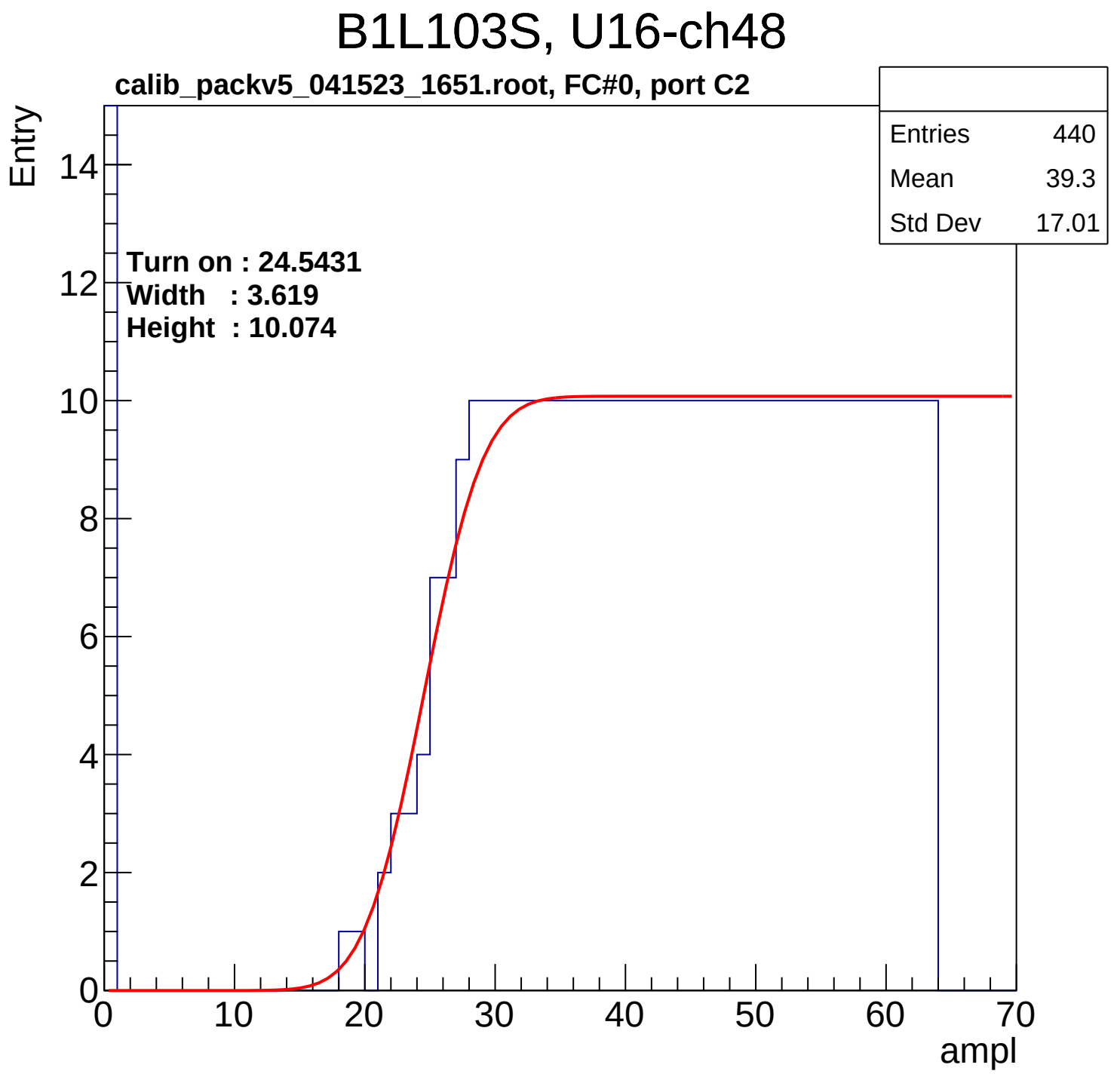
B1L103S, U16-ch48
calib_packv5_041523_1651.root, FC#0, port C2
Entries 440
Mean 39.3
Std Dev 17.01
Turn on : 24.5431
Width : 3.619
Height : 10.074
Entry
ampl
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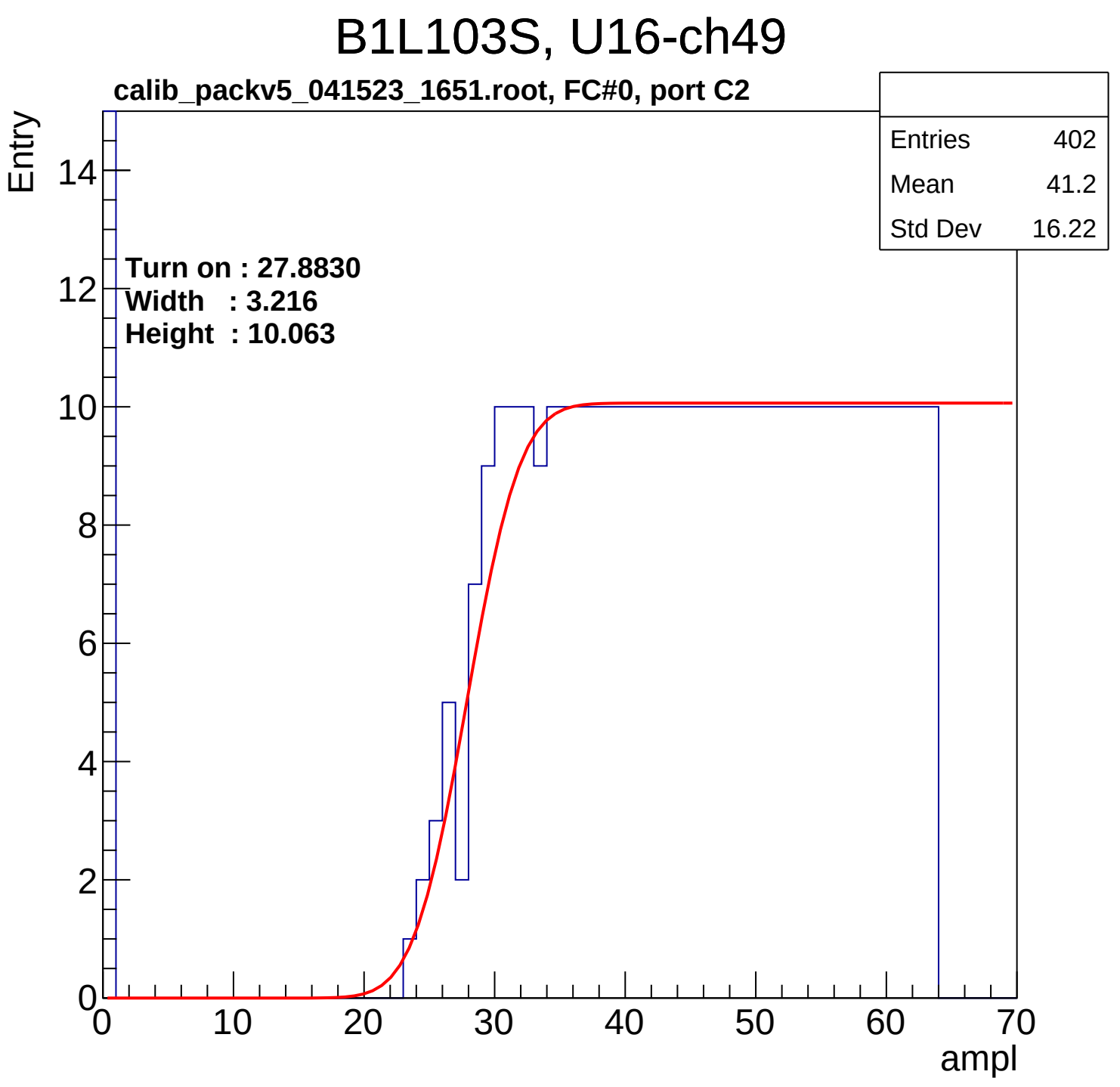
B1L103S, U16-ch49
calib_packv5_041523_1651.root, FC#0, port C2
Entries 402
Mean 41.2
Std Dev 16.22
Turn on : 27.8830
Width : 3.216
Height : 10.063
Entry
ampl
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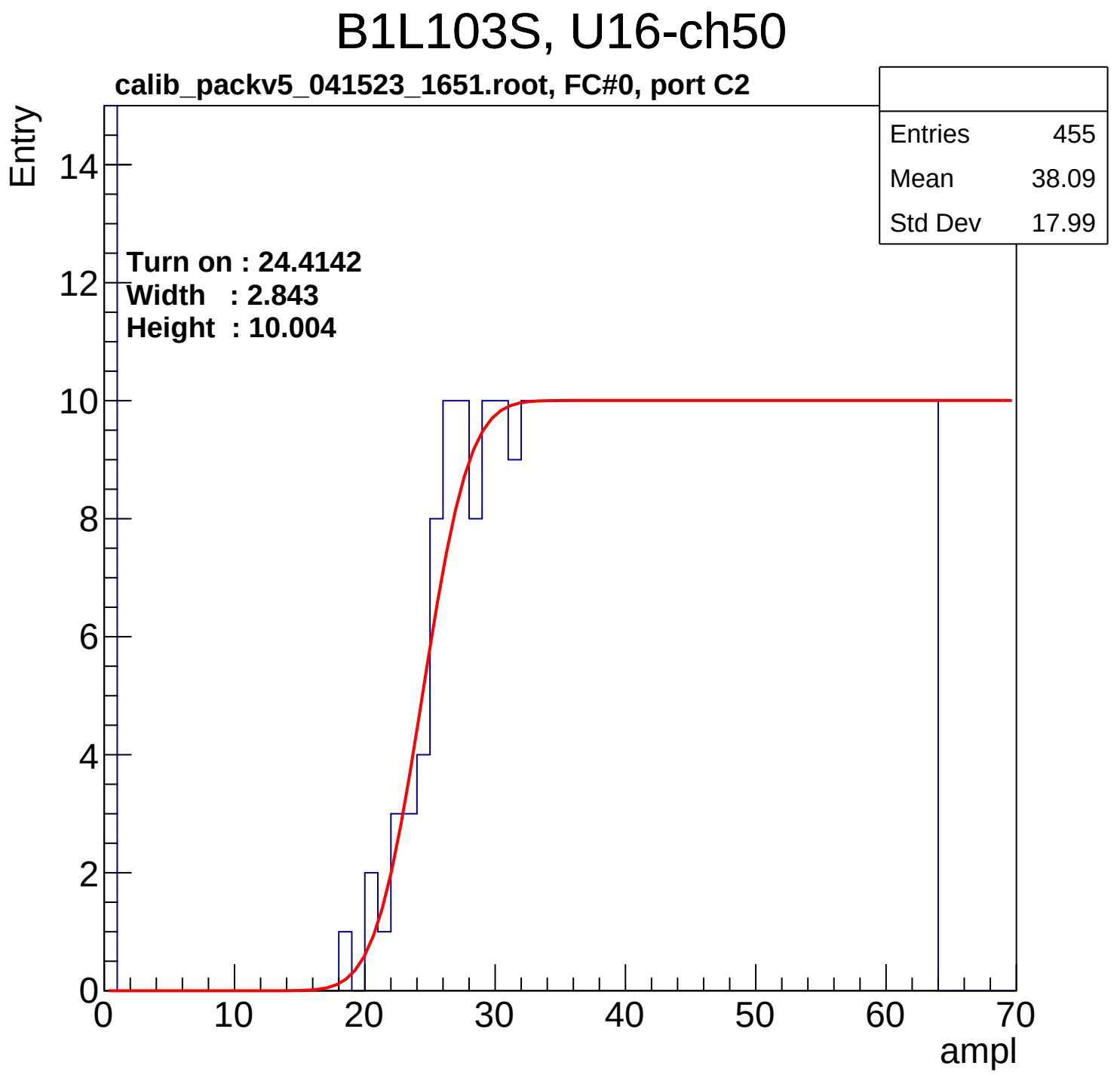
B1L103S, U16-ch50
calib_packv5_041523_1651.root, FC#0, port C2
Entries 455
Mean 38.09
Std Dev 17.99
Turn on : 24.4142
Width : 2.843
Height : 10.004
Entry
ampl
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8
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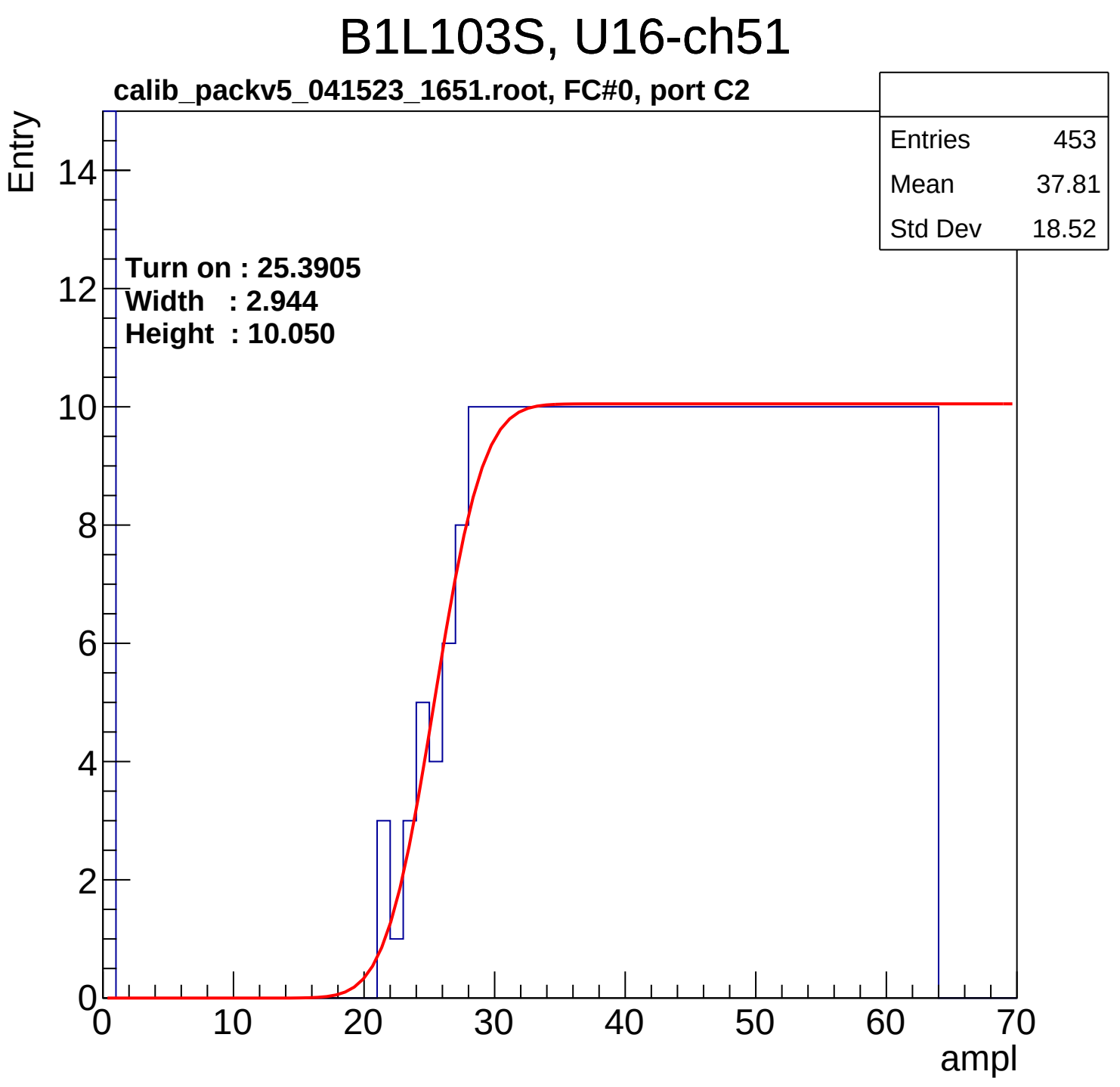
B1L103S, U16-ch51
calib_packv5_041523_1651.root, FC#0, port C2
Entries 453
Mean 37.81
Std Dev 18.52
Turn on : 25.3905
Width : 2.944
Height : 10.050
Entry
ampl
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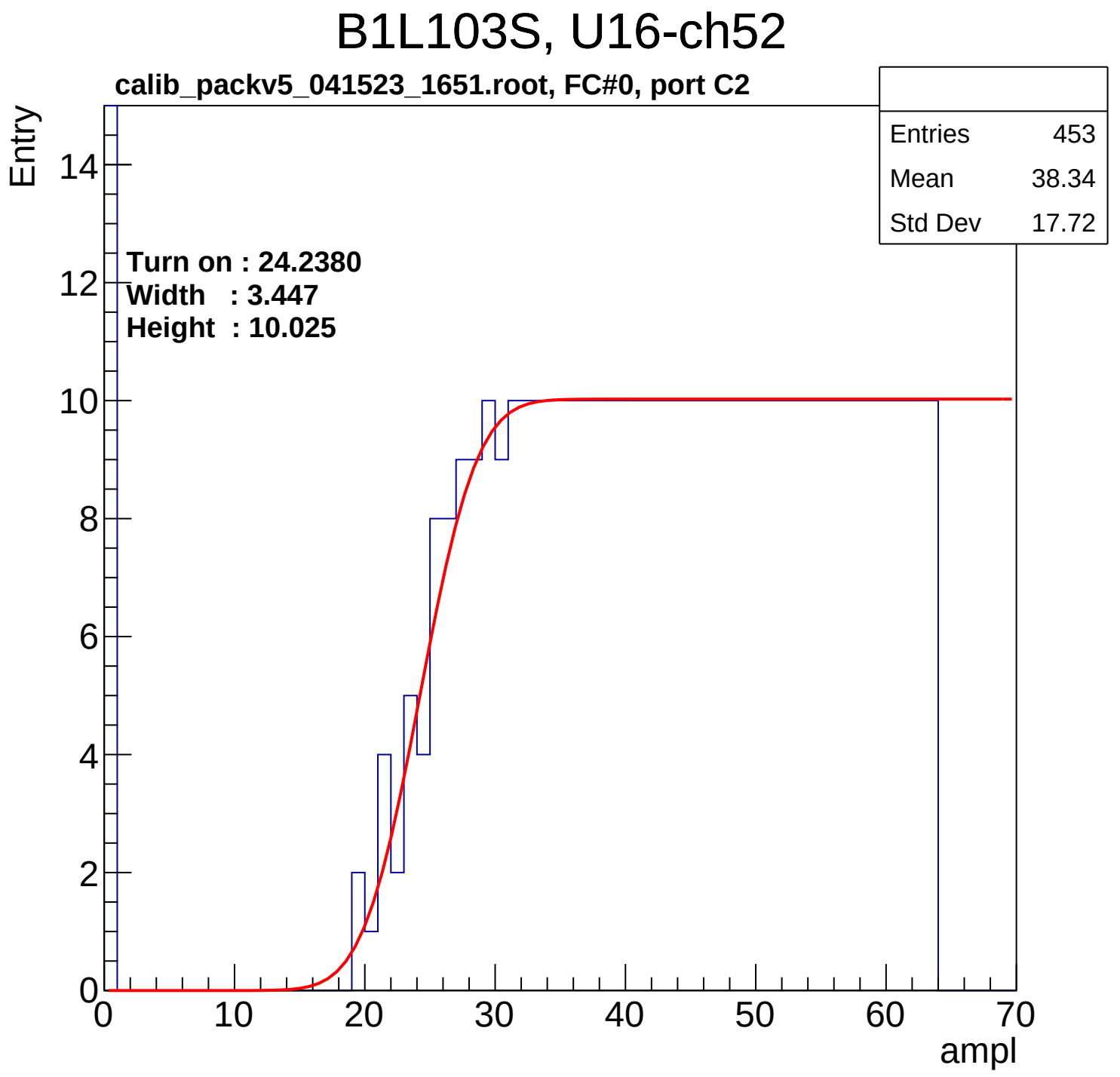
B1L103S, U16-ch52
calib_packv5_041523_1651.root, FC#0, port C2
Entries 453
Mean 38.34
Std Dev 17.72
Turn on : 24.2380
Width : 3.447
Height : 10.025
Entry
ampl
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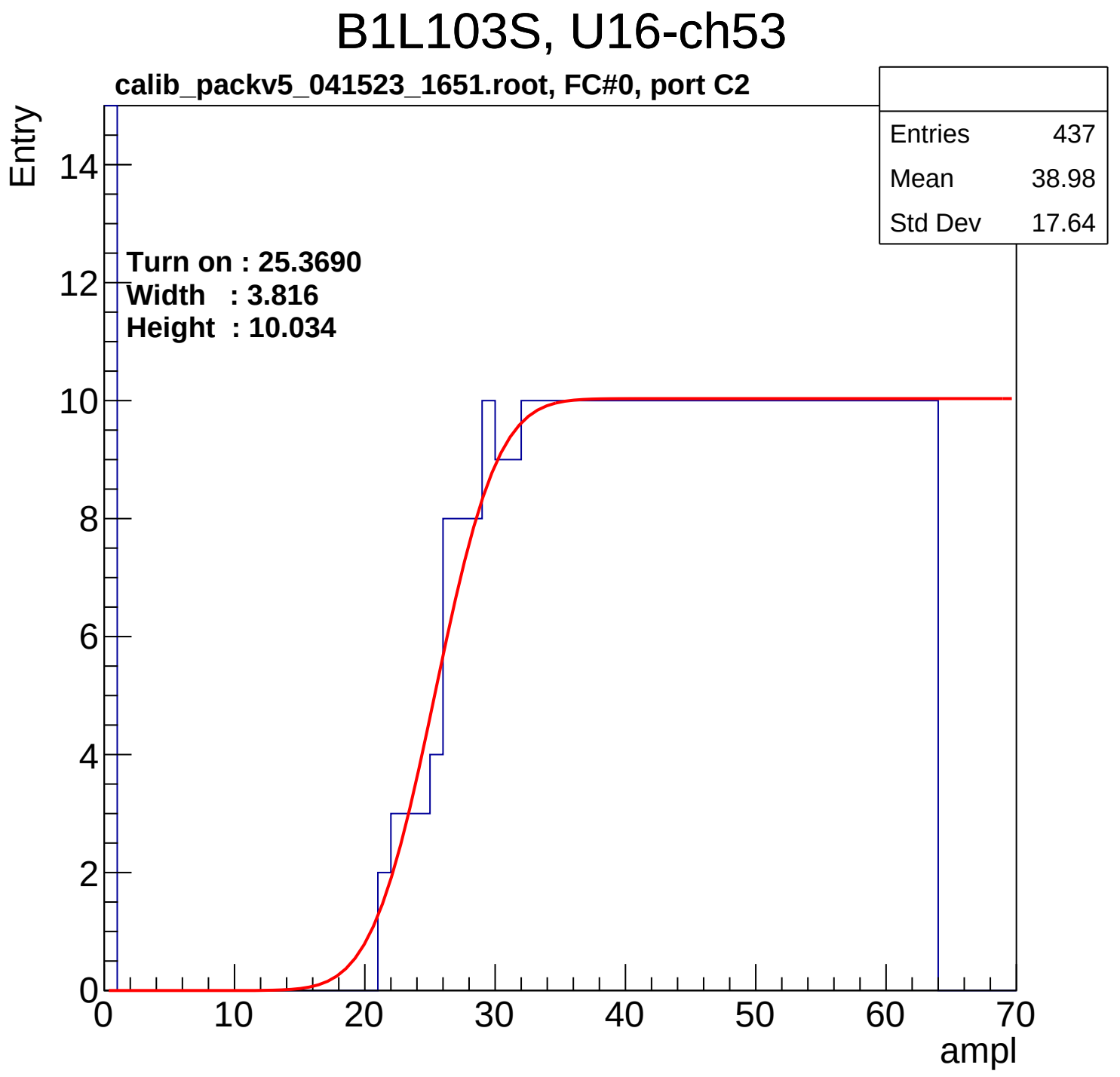
B1L103S, U16-ch53
calib_packv5_041523_1651.root, FC#0, port C2
Entries 437
Mean 38.98
Std Dev 17.64
Turn on : 25.3690
Width : 3.816
Height : 10.034
Entry
ampl
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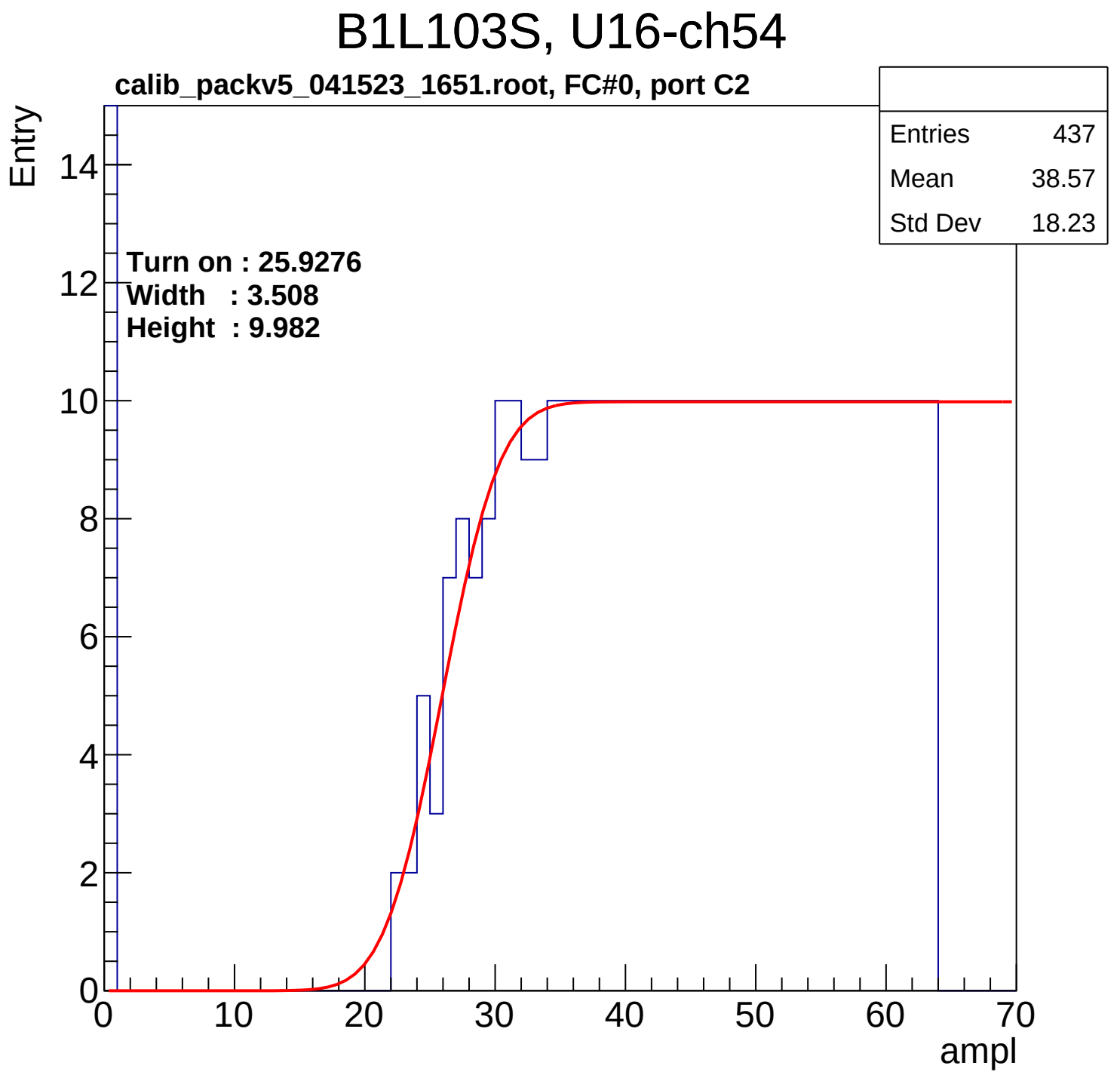
B1L103S, U16-ch54
calib_packv5_041523_1651.root, FC#0, port C2
Entries 437
Mean 38.57
Std Dev 18.23
Turn on : 25.9276
Width : 3.508
Height : 9.982
Entry
ampl
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6
8
10
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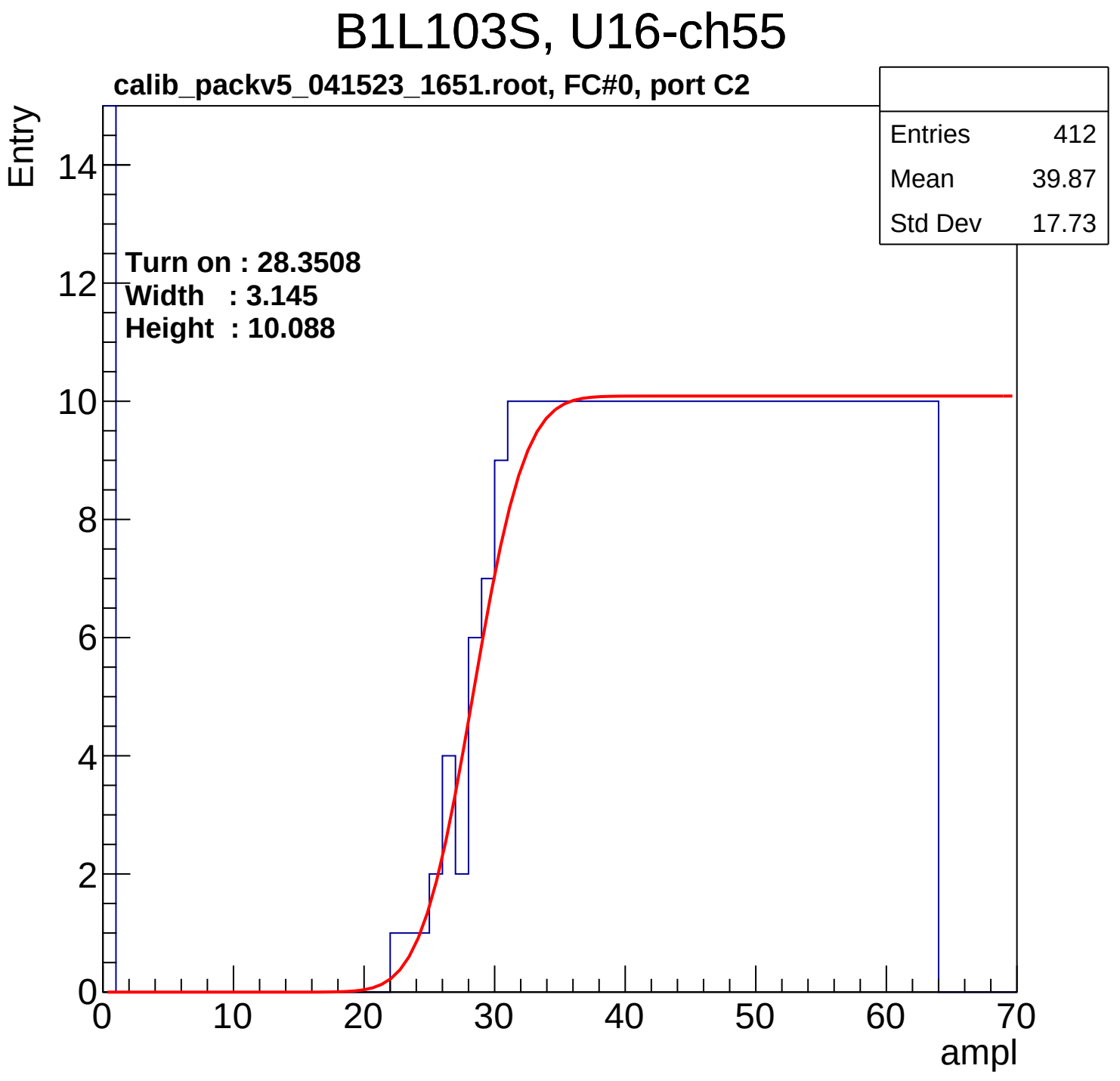
B1L103S, U16-ch55
calib_packv5_041523_1651.root, FC#0, port C2
Entries 412
Mean 39.87
Std Dev 17.73
Turn on : 28.3508
Width : 3.145
Height : 10.088
Entry
ampl
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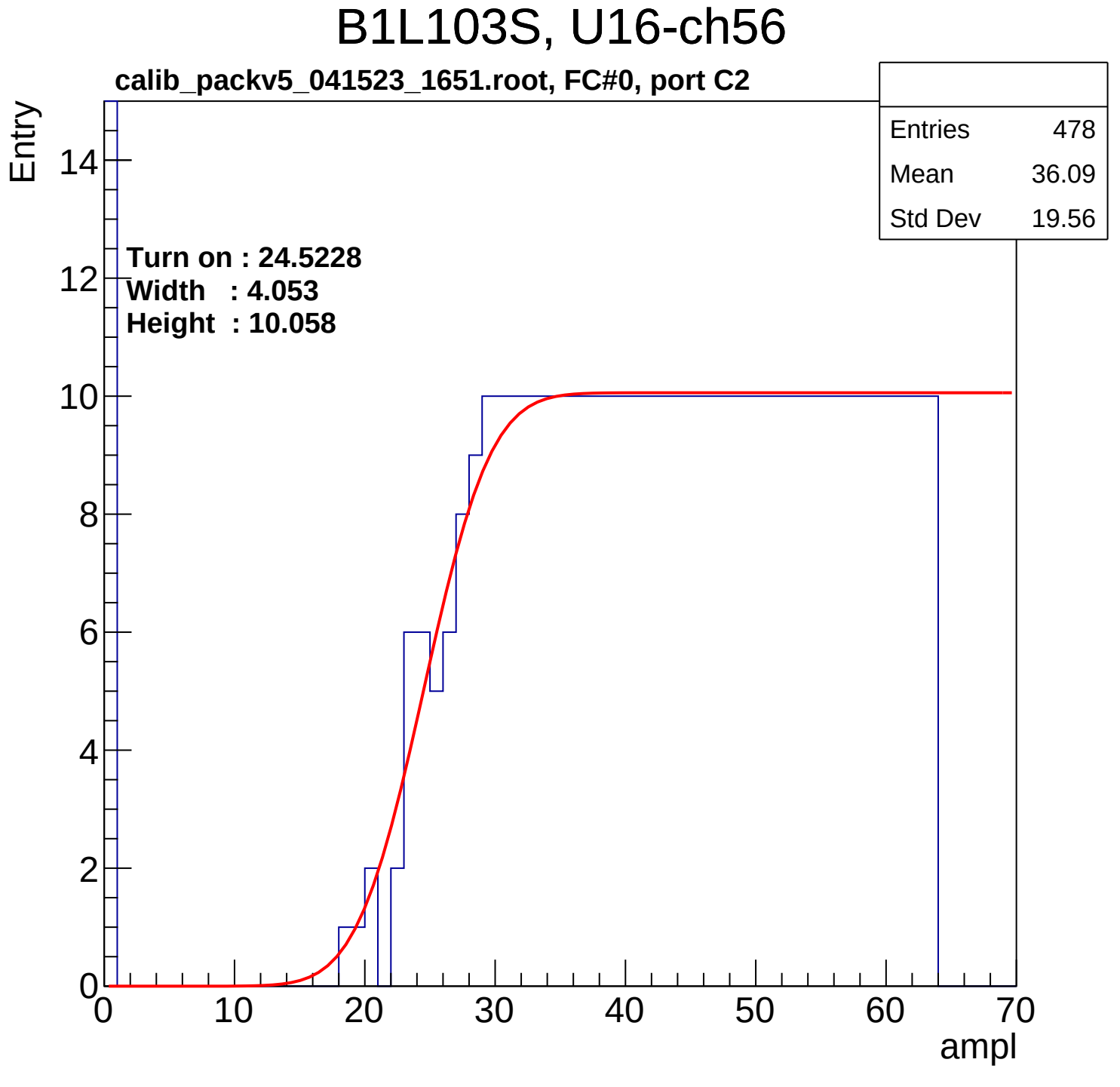
B1L103S, U16-ch56
calib_packv5_041523_1651.root, FC#0, port C2
Entries 478
Mean 36.09
Std Dev 19.56
Turn on : 24.5228
Width : 4.053
Height : 10.058
Entry
ampl
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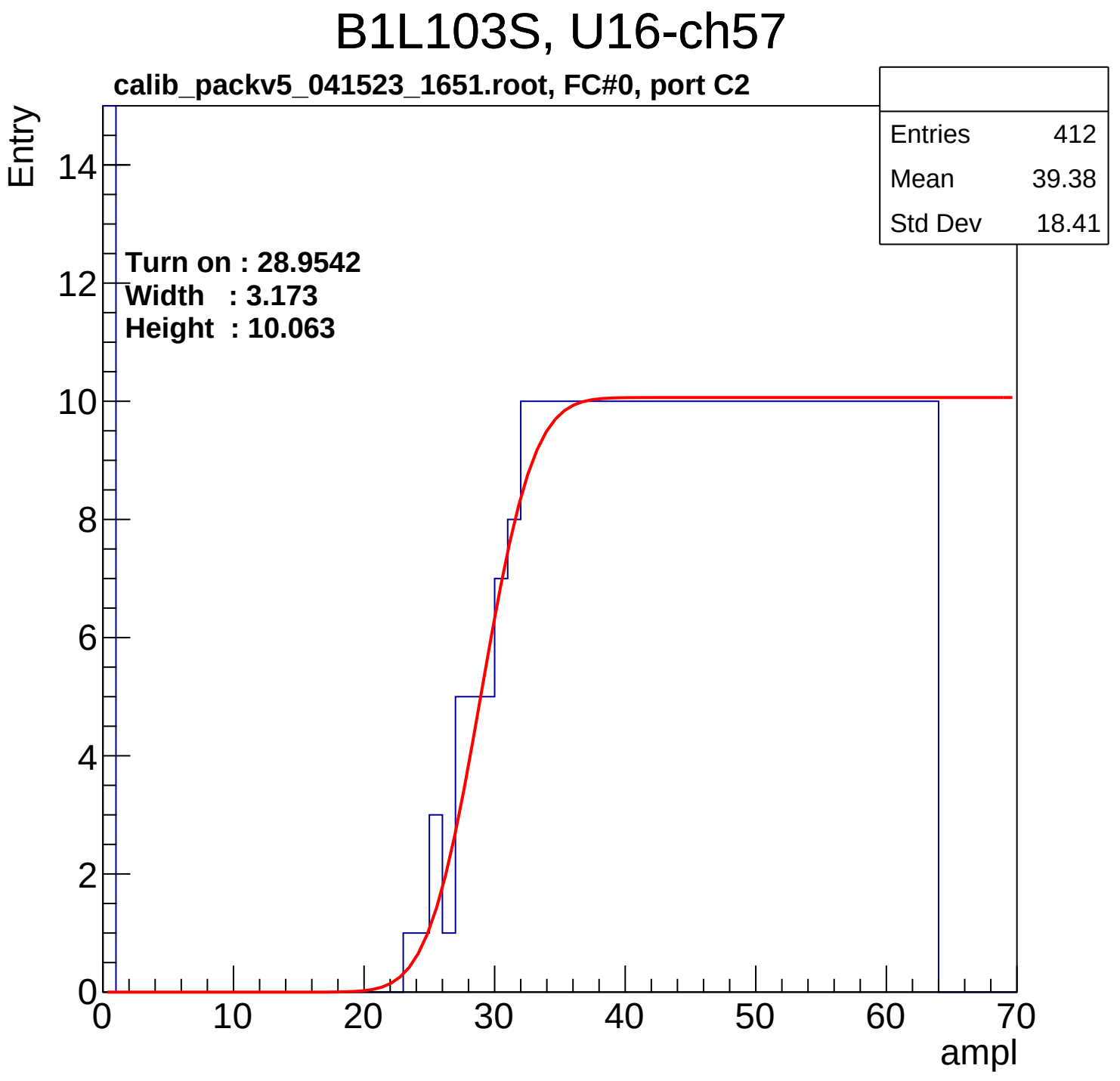
B1L103S, U16-ch57
calib_packv5_041523_1651.root, FC#0, port C2
Entries 412
Mean 39.38
Std Dev 18.41
Turn on : 28.9542
Width : 3.173
Height : 10.063
Entry
ampl
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4
6
8
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20
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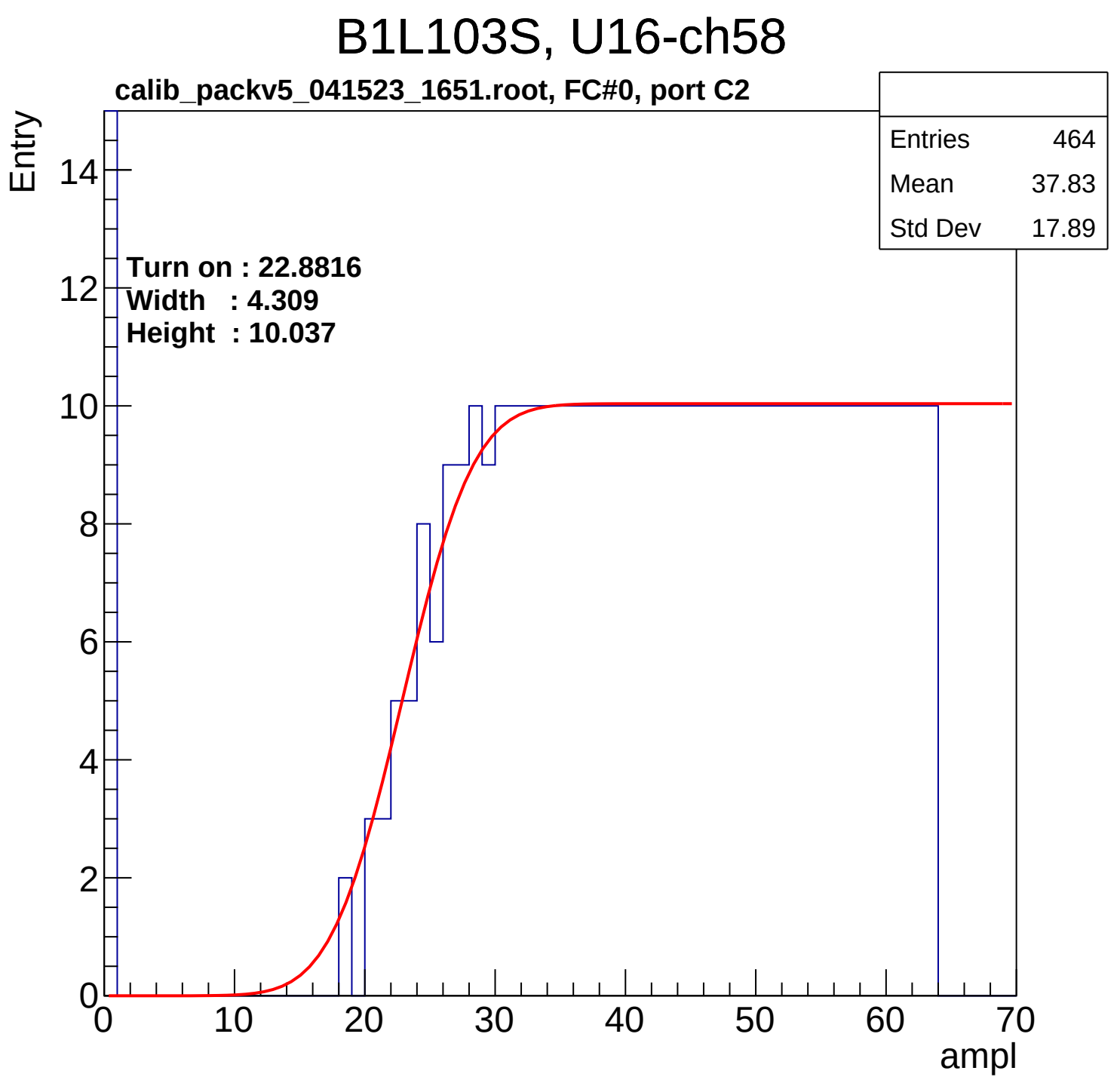
B1L103S, U16-ch58
calib_packv5_041523_1651.root, FC#0, port C2
Entries 464
Mean 37.83
Std Dev 17.89
Turn on : 22.8816
Width : 4.309
Height : 10.037
Entry
ampl
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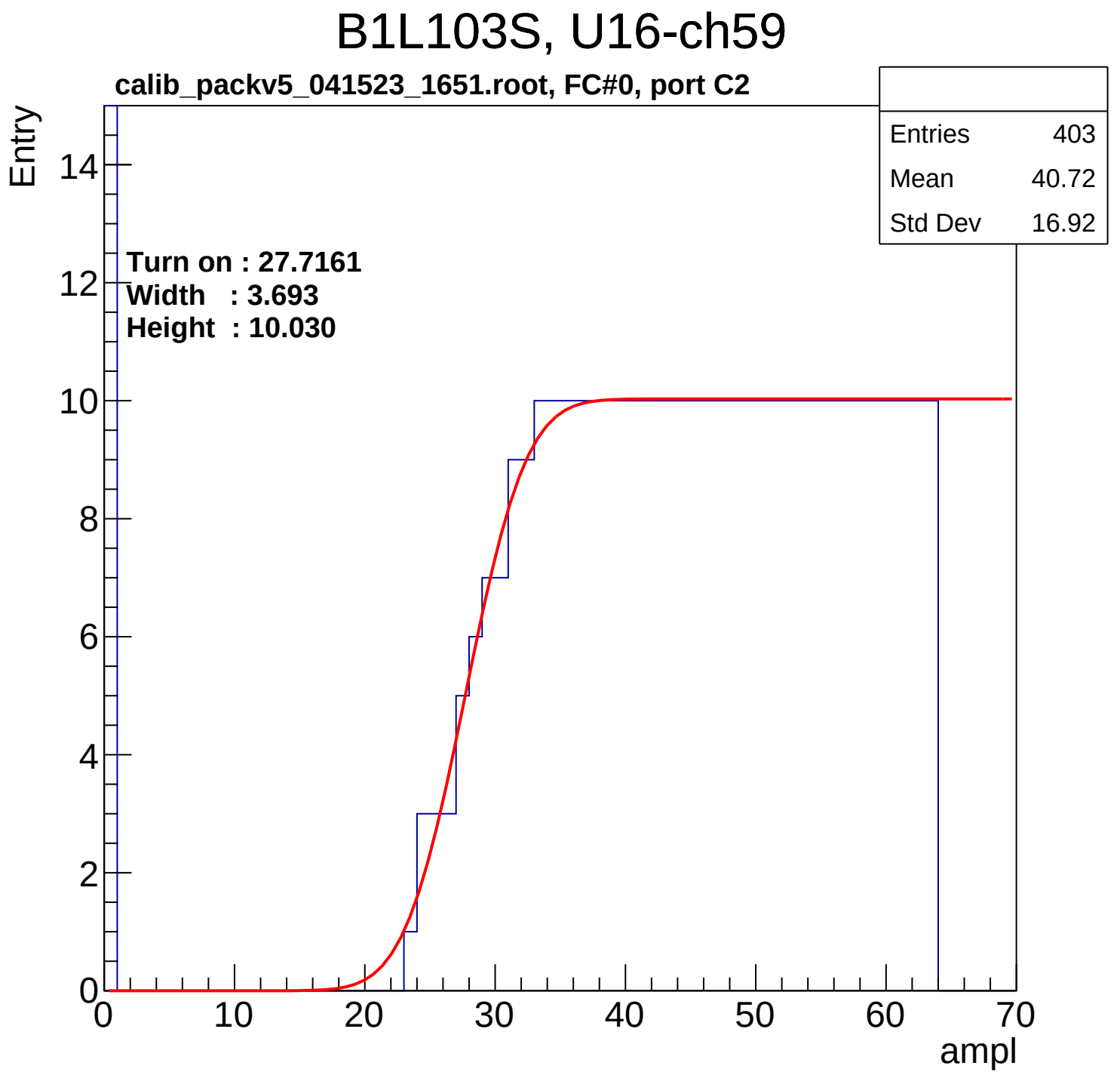
B1L103S, U16-ch59
calib_packv5_041523_1651.root, FC#0, port C2
Entries 403
Mean 40.72
Std Dev 16.92
Turn on : 27.7161
Width : 3.693
Height : 10.030
Entry
ampl
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2
4
6
8
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0
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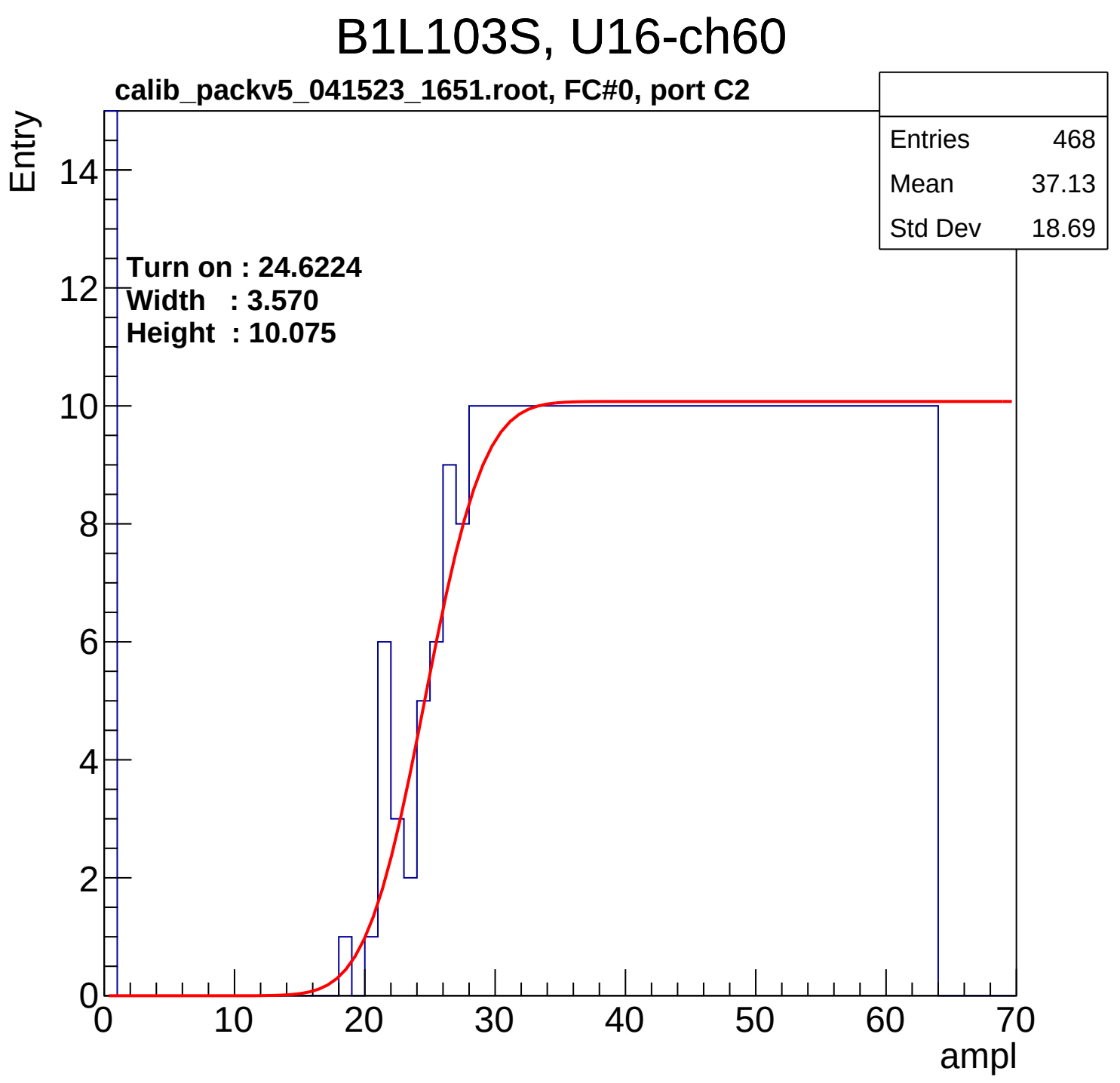
B1L103S, U16-ch60
calib_packv5_041523_1651.root, FC#0, port C2
Entries 468
Mean 37.13
Std Dev 18.69
Turn on : 24.6224
Width : 3.570
Height : 10.075
Entry
ampl
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2
4
6
8
10
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0
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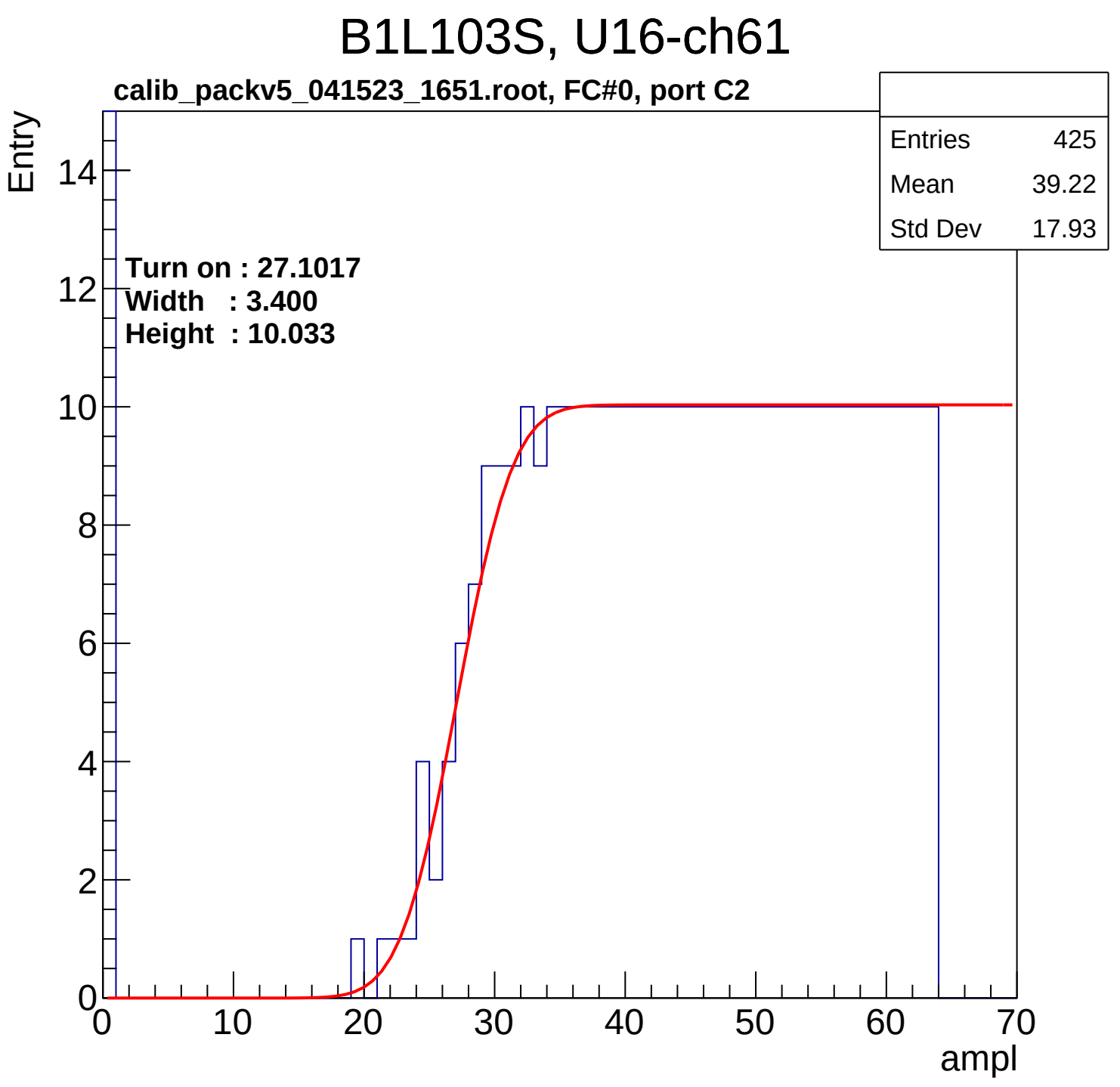
B1L103S, U16-ch61
calib_packv5_041523_1651.root, FC#0, port C2
Entries 425
Mean 39.22
Std Dev 17.93
Turn on : 27.1017
Width : 3.400
Height : 10.033
Entry
ampl
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2
4
6
8
10
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0
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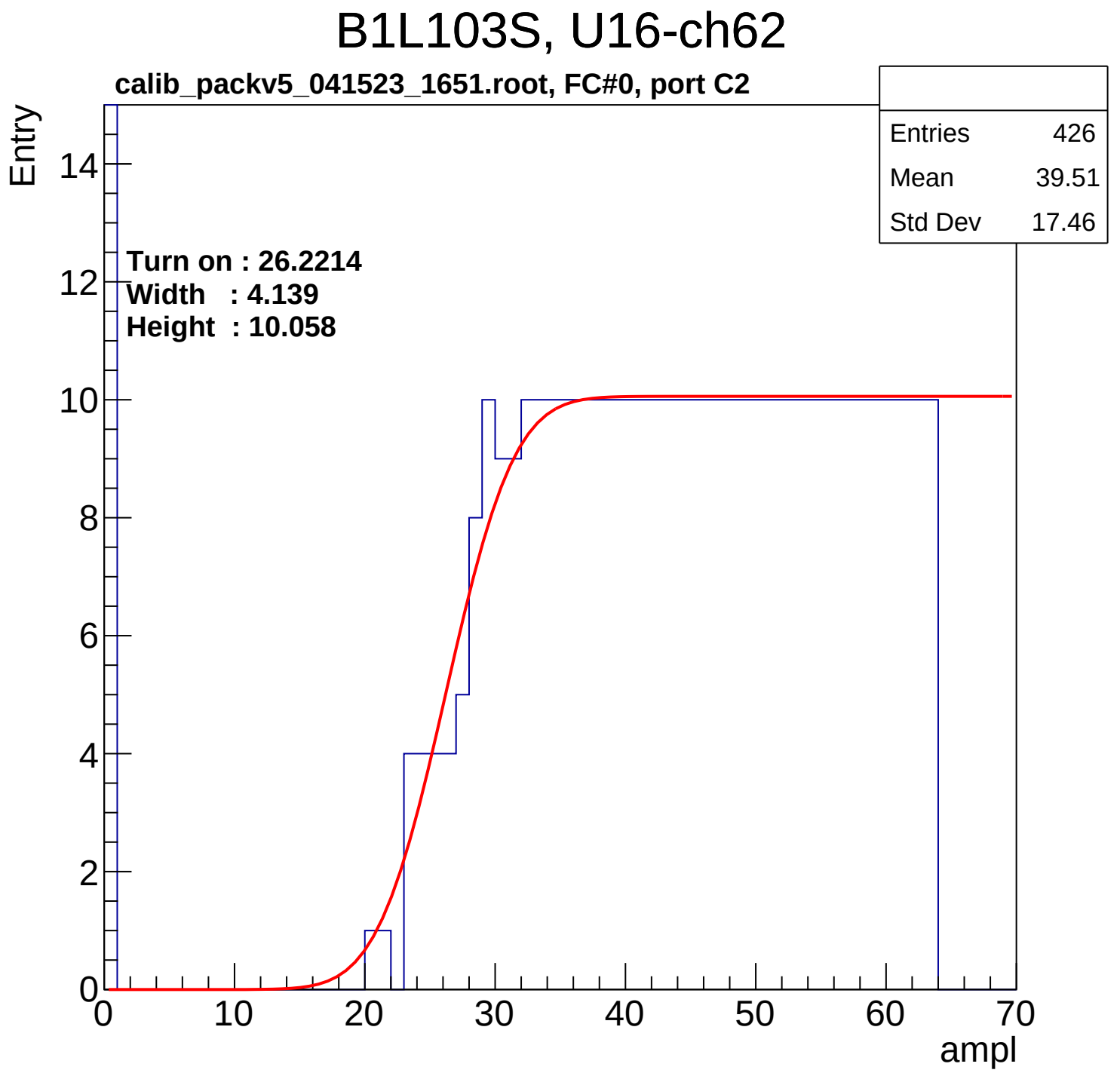
B1L103S, U16-ch62
calib_packv5_041523_1651.root, FC#0, port C2
Entries 426
Mean 39.51
Std Dev 17.46
Turn on : 26.2214
Width : 4.139
Height : 10.058
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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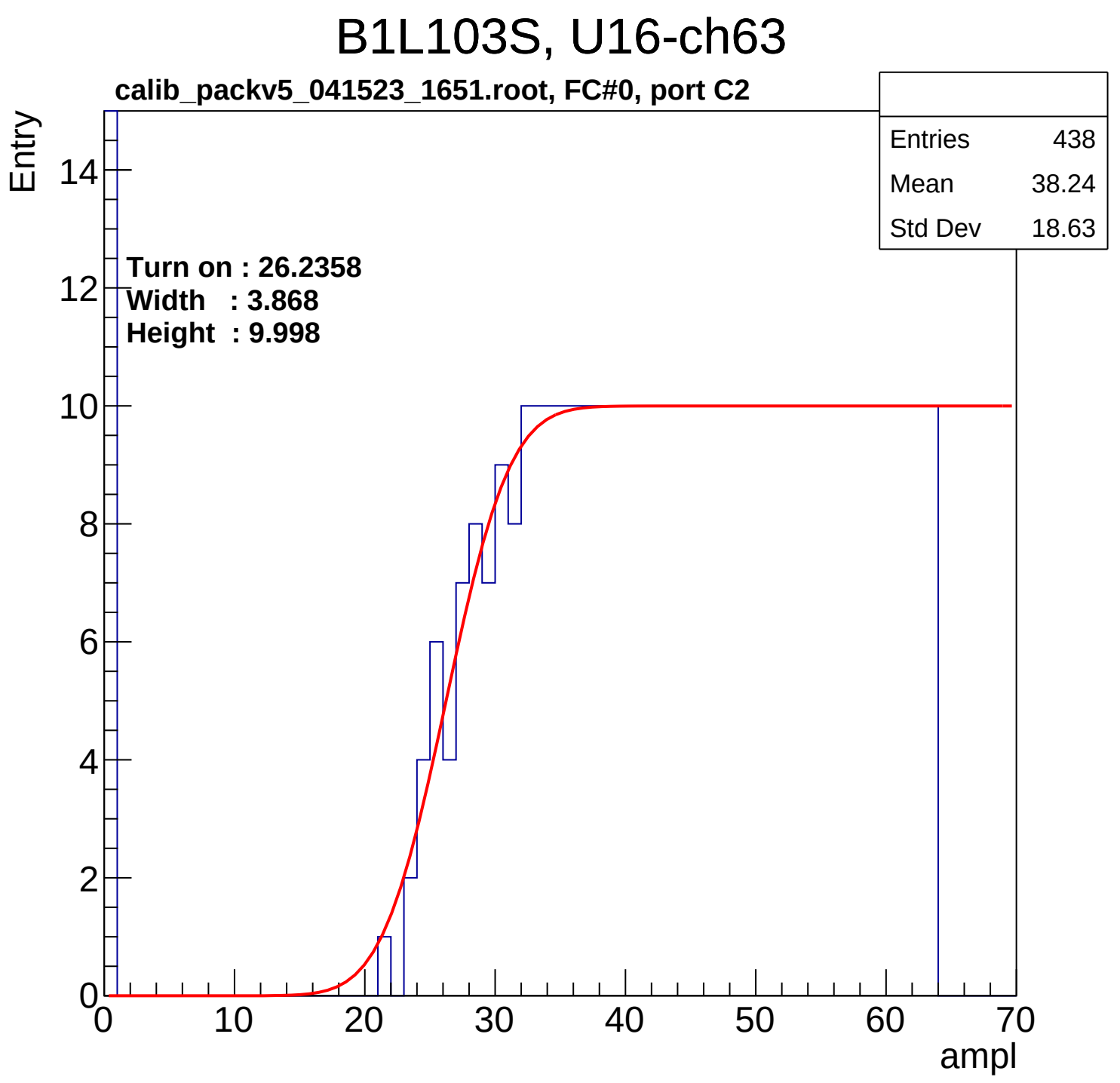
B1L103S, U16-ch63
calib_packv5_041523_1651.root, FC#0, port C2
Entries 438
Mean 38.24
Std Dev 18.63
Turn on : 26.2358
Width : 3.868
Height : 9.998
Entry
ampl
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2
4
6
8
10
12
14
0
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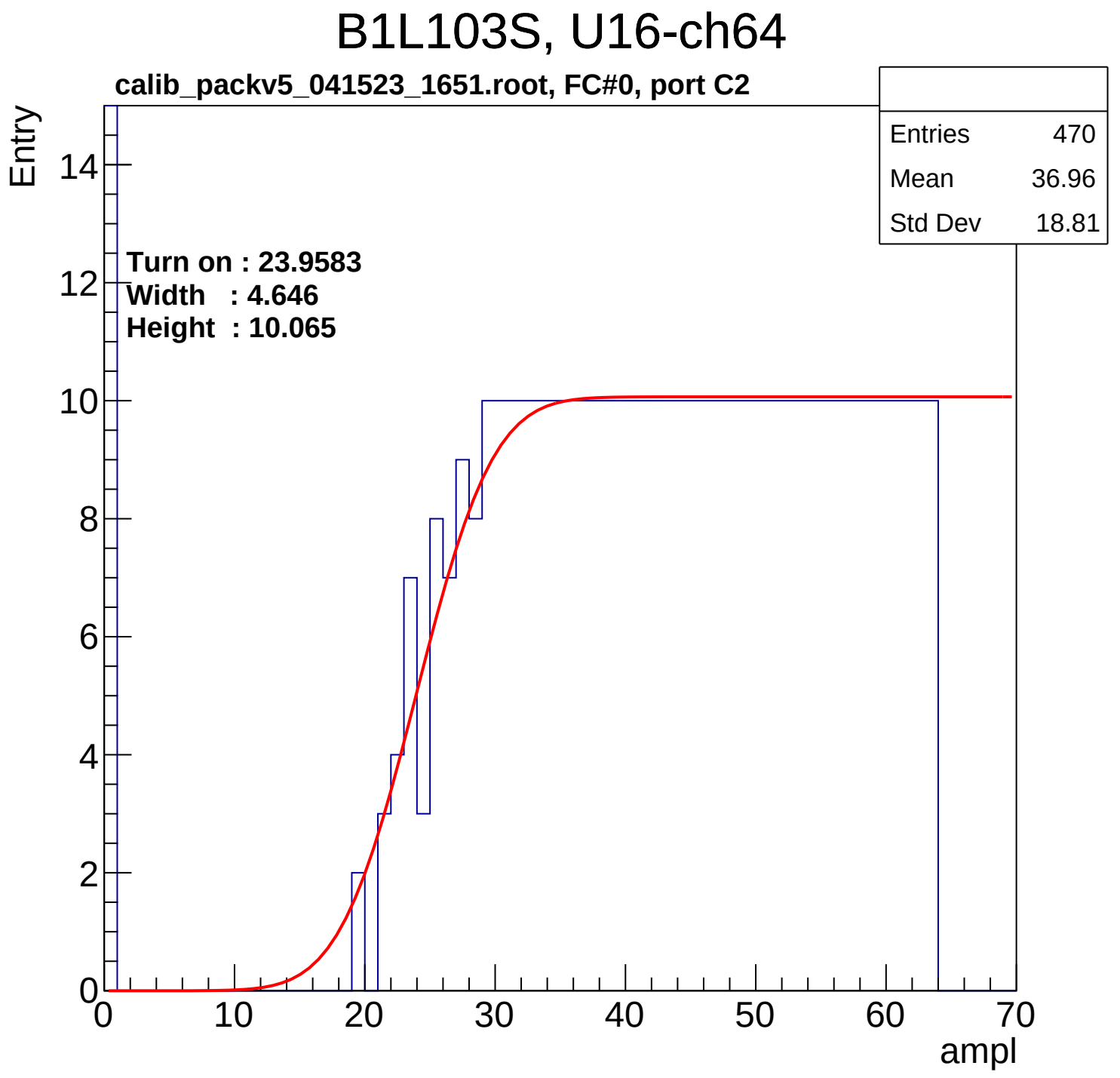
B1L103S, U16-ch64
calib_packv5_041523_1651.root, FC#0, port C2
Entries 470
Mean 36.96
Std Dev 18.81
Turn on : 23.9583
Width : 4.646
Height : 10.065
Entry
ampl
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2
4
6
8
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0
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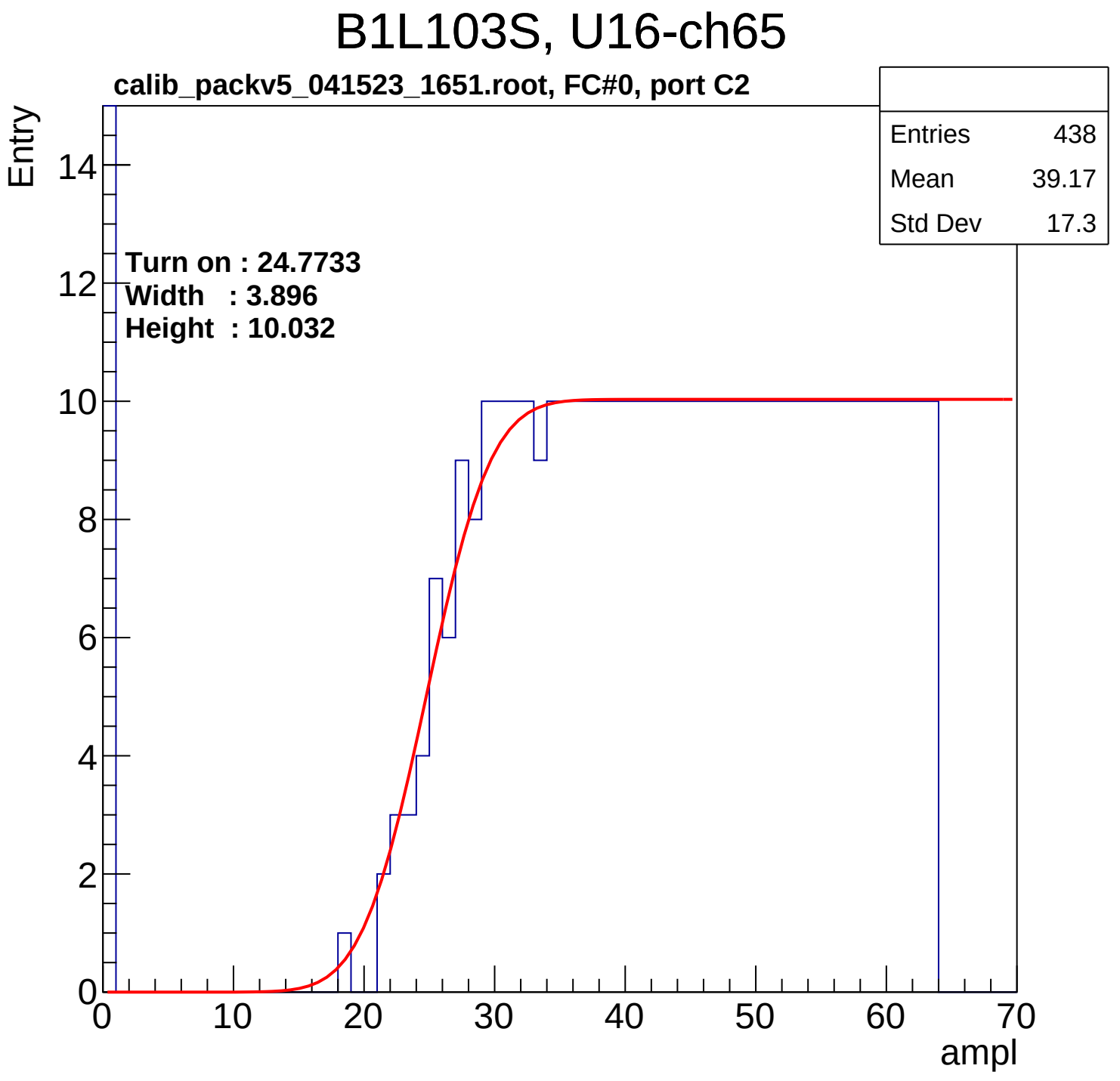
B1L103S, U16-ch65
calib_packv5_041523_1651.root, FC#0, port C2
Entries 438
Mean 39.17
Std Dev 17.3
Turn on : 24.7733
Width : 3.896
Height : 10.032
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
50
60
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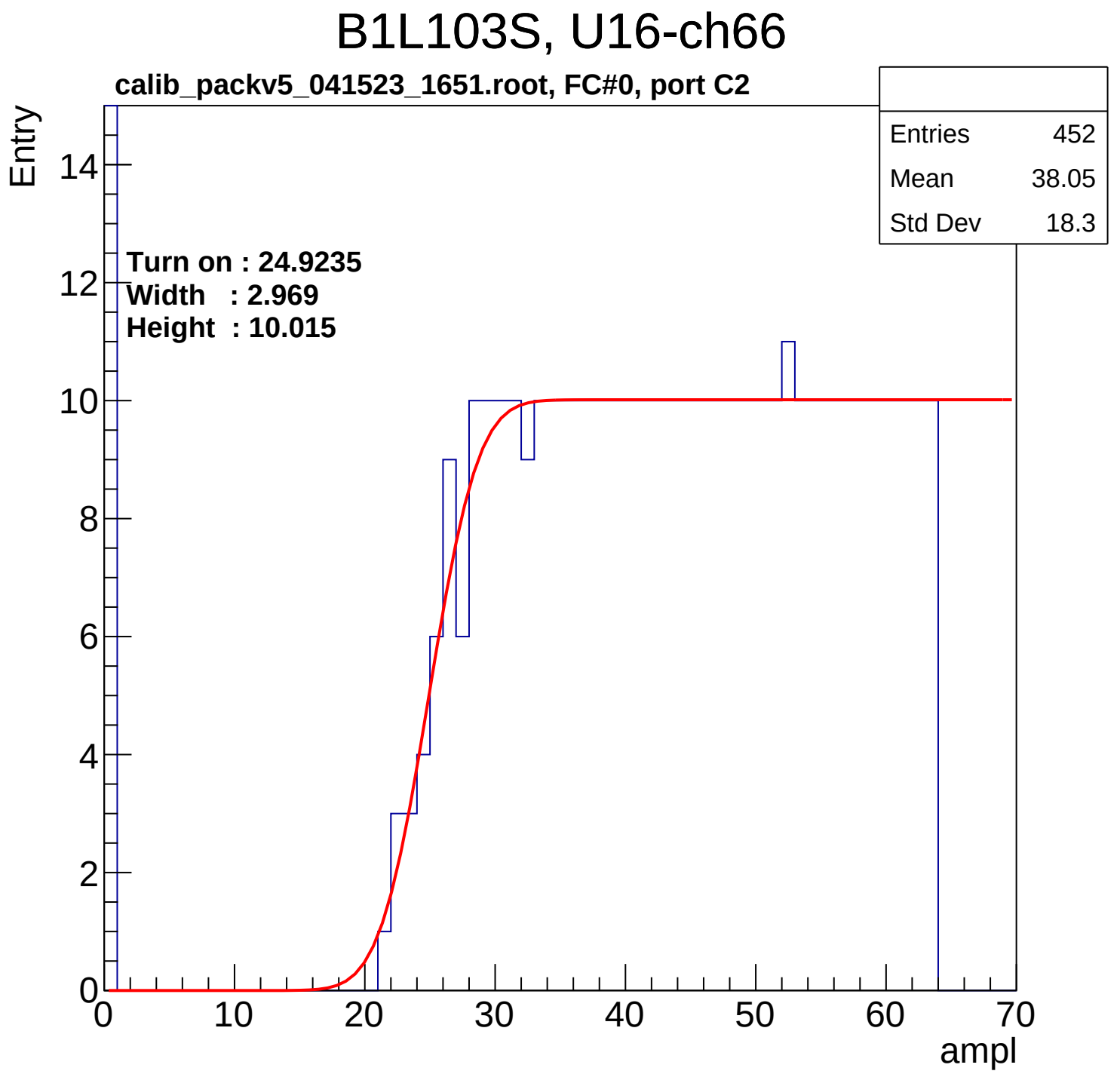
B1L103S, U16-ch66
calib_packv5_041523_1651.root, FC#0, port C2
Entries 452
Mean 38.05
Std Dev 18.3
Turn on : 24.9235
Width : 2.969
Height : 10.015
Entry
ampl
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2
4
6
8
10
12
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0
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60
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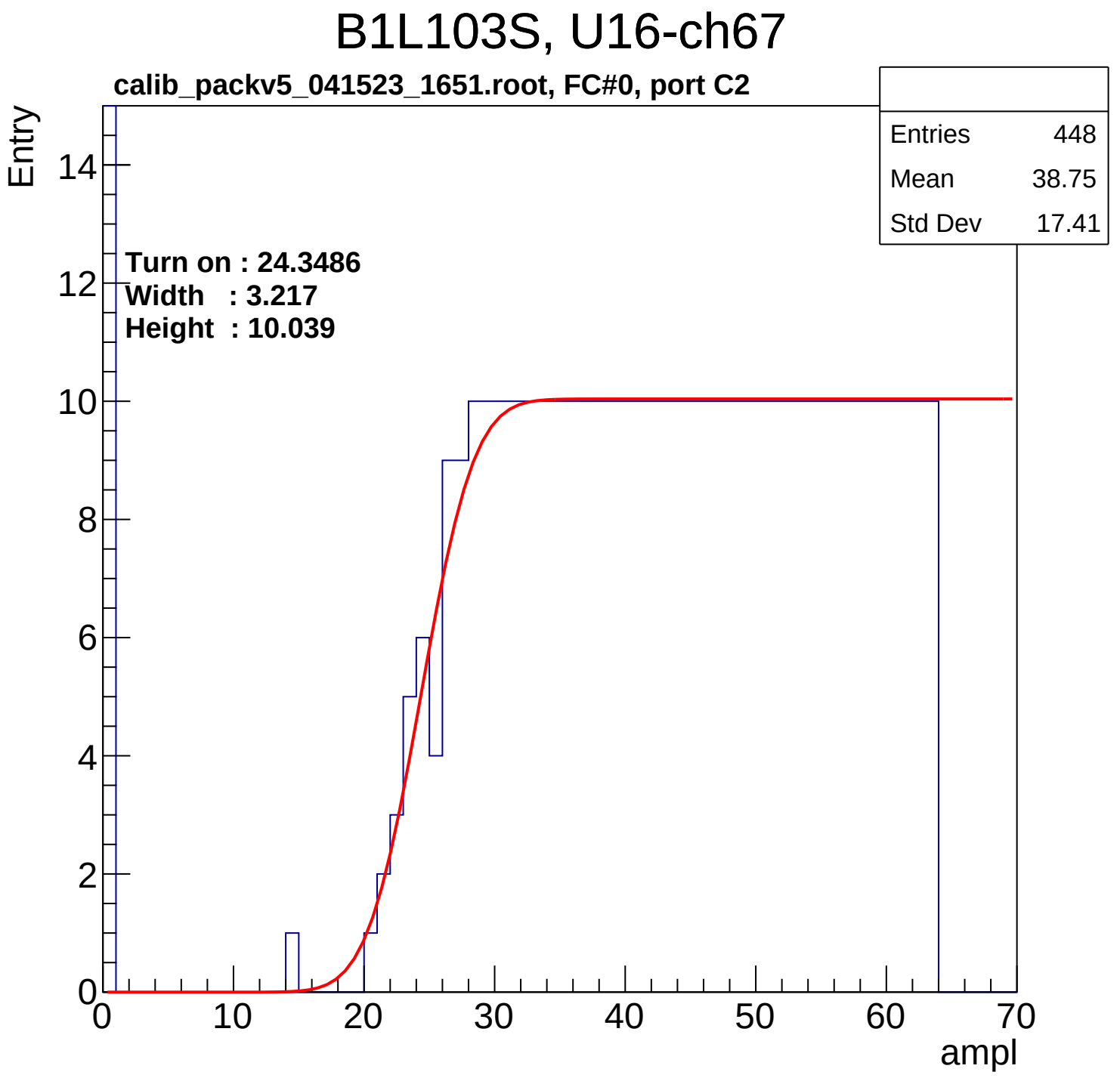
B1L103S, U16-ch67
calib_packv5_041523_1651.root, FC#0, port C2
Entries 448
Mean 38.75
Std Dev 17.41
Turn on : 24.3486
Width : 3.217
Height : 10.039
Entry
ampl
0
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6
8
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12
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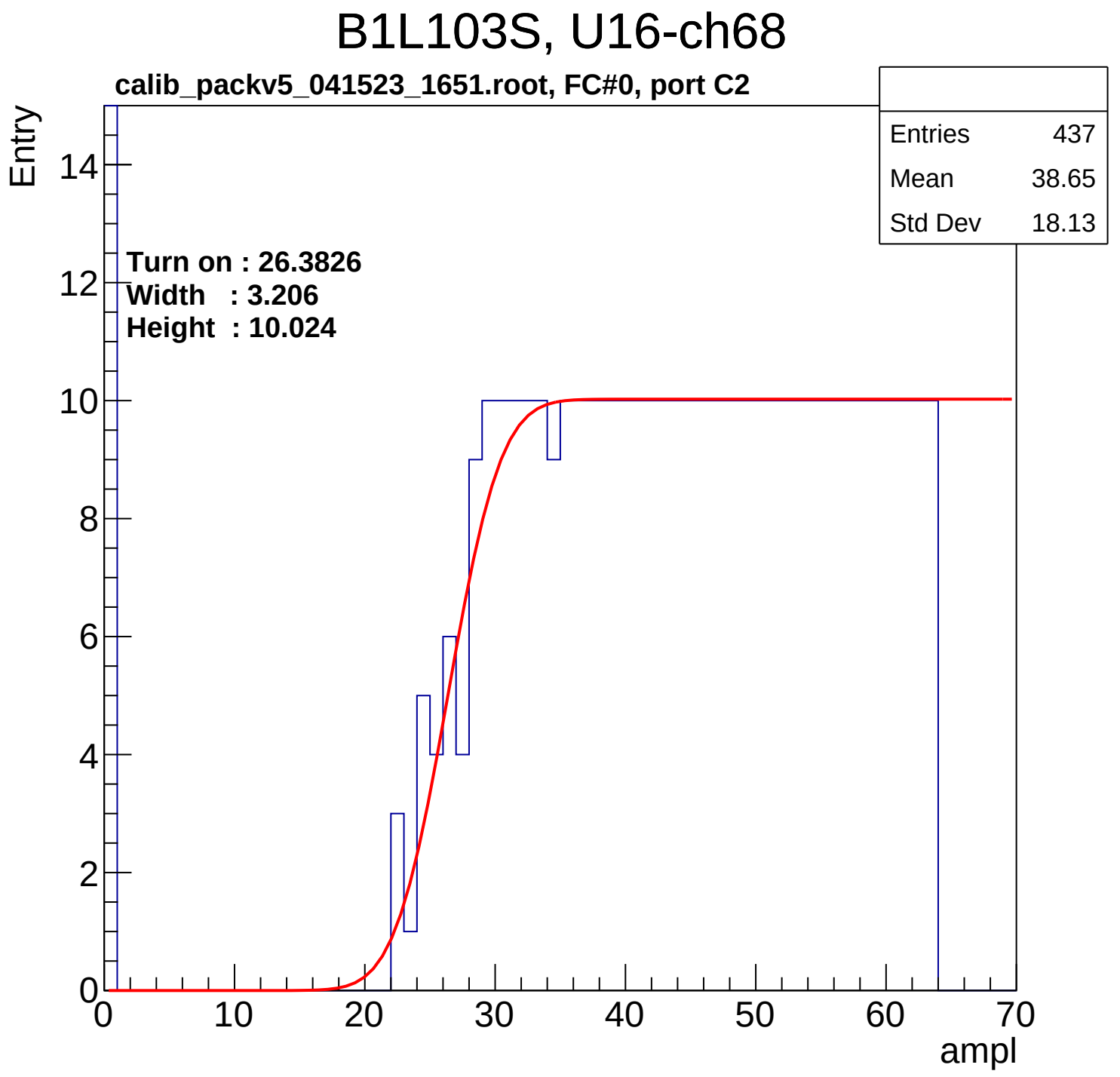
B1L103S, U16-ch68
calib_packv5_041523_1651.root, FC#0, port C2
Entries 437
Mean 38.65
Std Dev 18.13
Turn on : 26.3826
Width : 3.206
Height : 10.024
Entry
ampl
0
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4
6
8
10
12
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0
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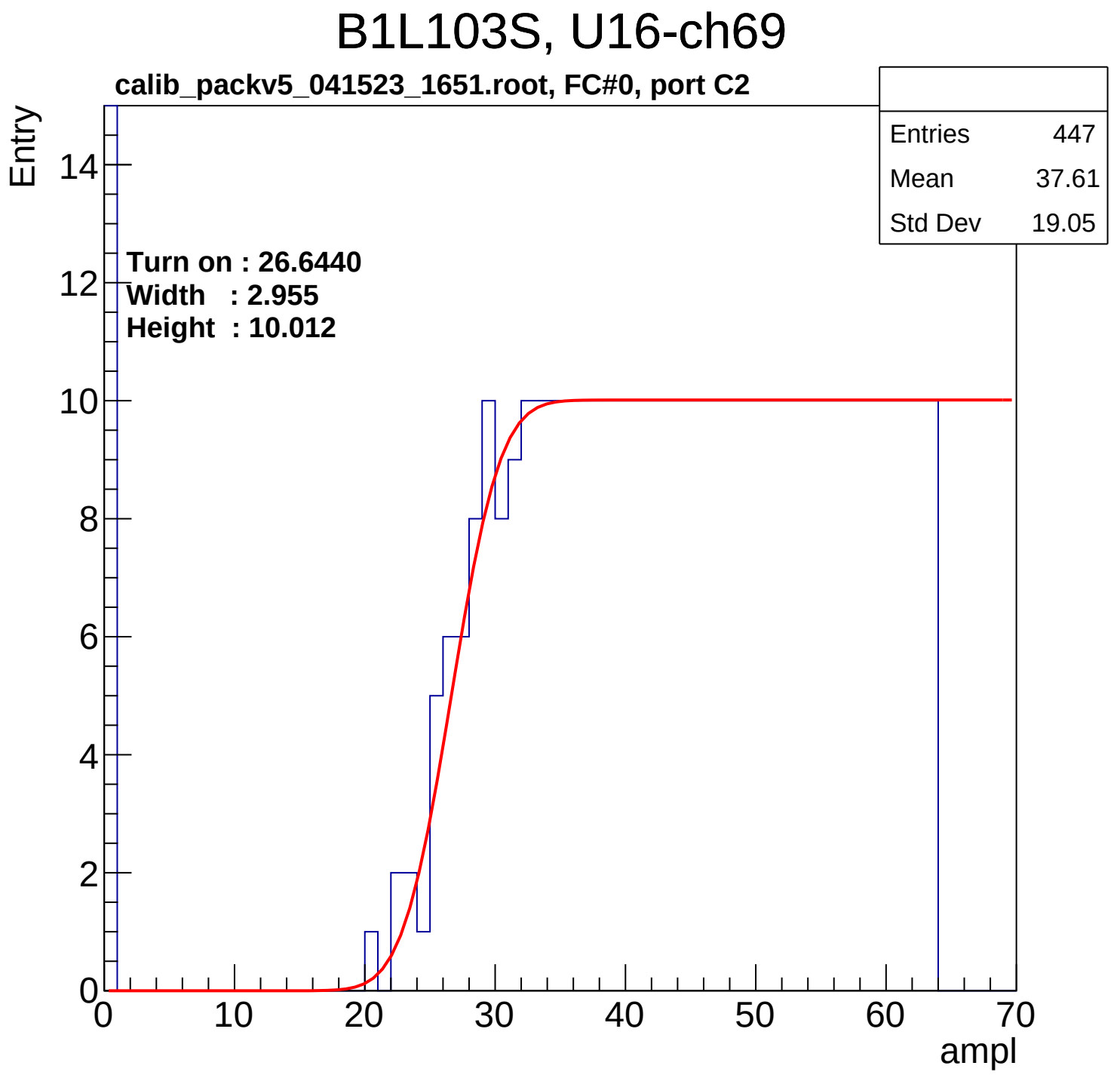
B1L103S, U16-ch69
calib_packv5_041523_1651.root, FC#0, port C2
Entries 447
Mean 37.61
Std Dev 19.05
Turn on : 26.6440
Width : 2.955
Height : 10.012
Entry
ampl
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2
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6
8
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0
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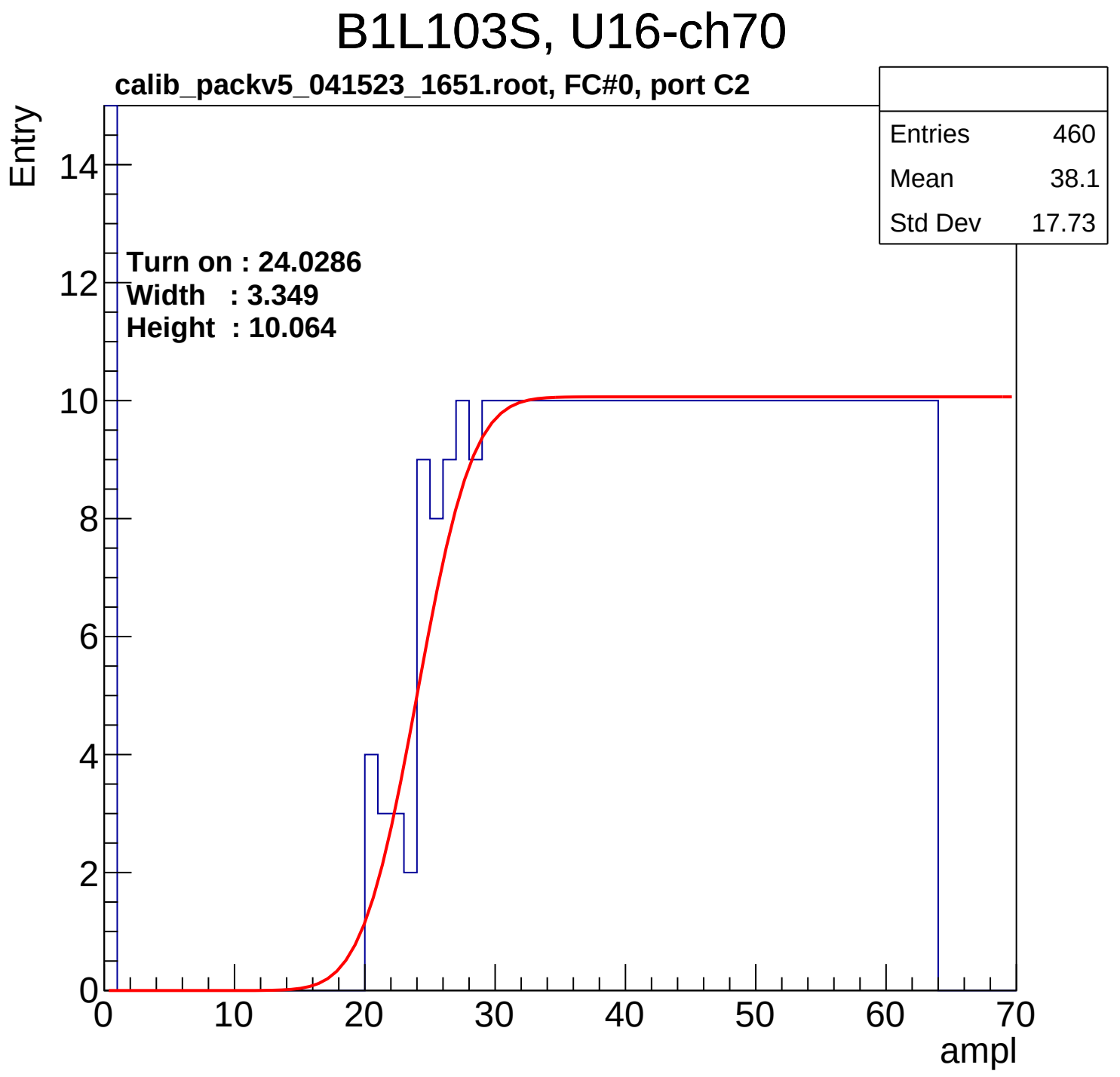
B1L103S, U16-ch70
calib_packv5_041523_1651.root, FC#0, port C2
Entries 460
Mean 38.1
Std Dev 17.73
Turn on : 24.0286
Width : 3.349
Height : 10.064
Entry
ampl
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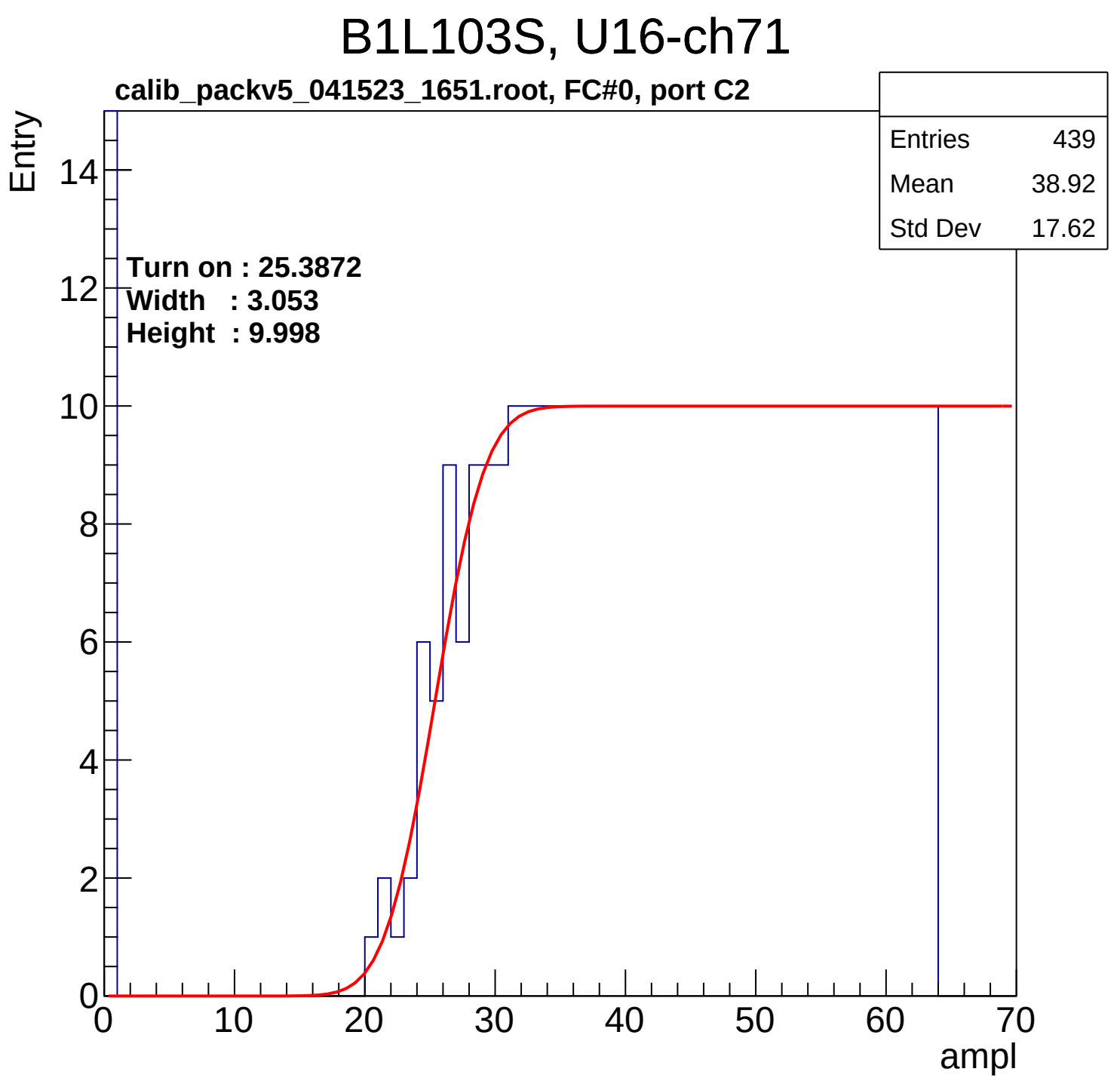
B1L103S, U16-ch71
calib_packv5_041523_1651.root, FC#0, port C2
Entries 439
Mean 38.92
Std Dev 17.62
Turn on : 25.3872
Width : 3.053
Height : 9.998
Entry
ampl
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2
4
6
8
10
12
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0
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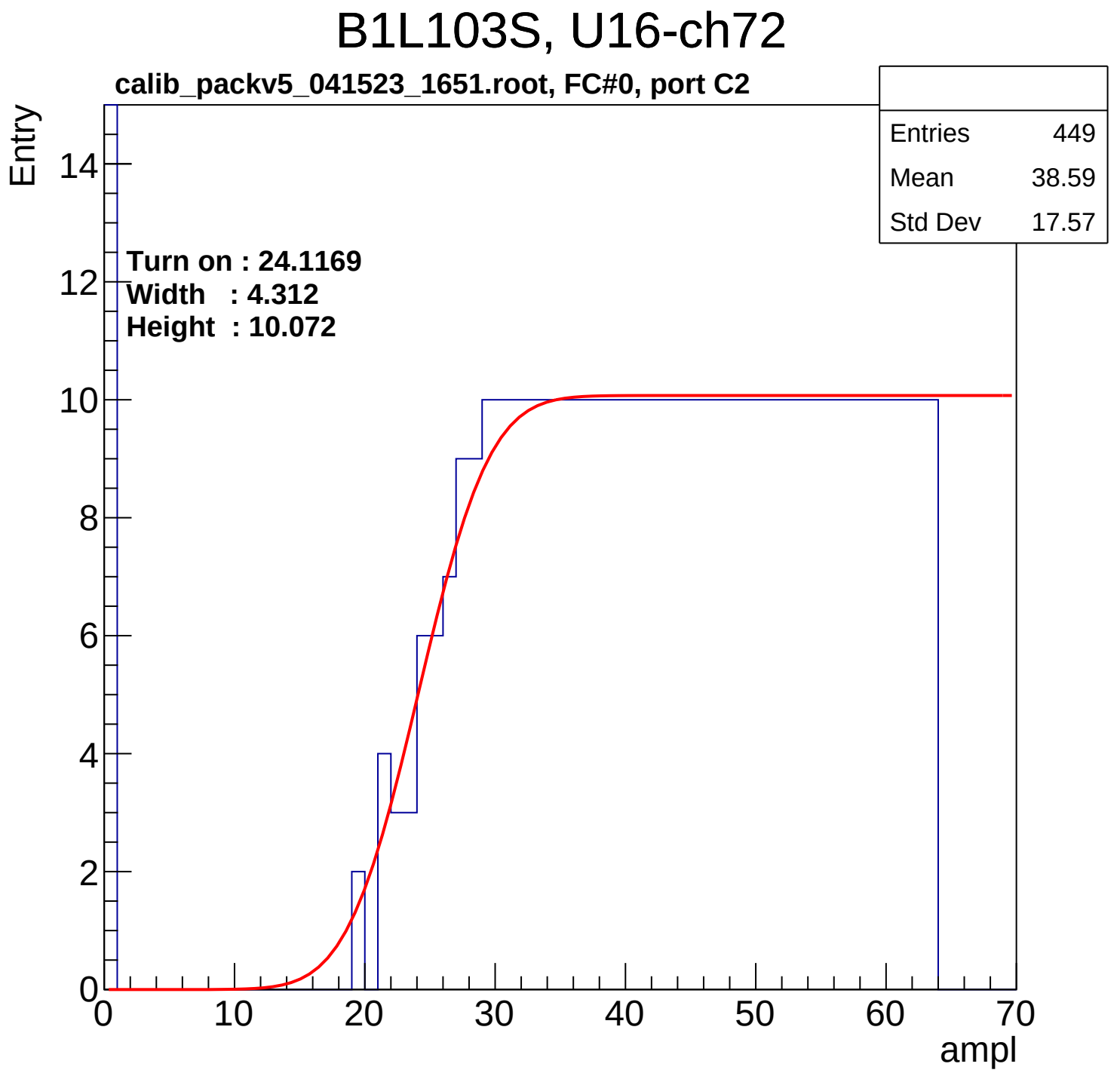
B1L103S, U16-ch72
calib_packv5_041523_1651.root, FC#0, port C2
Entries 449
Mean 38.59
Std Dev 17.57
Turn on : 24.1169
Width : 4.312
Height : 10.072
Entry
ampl
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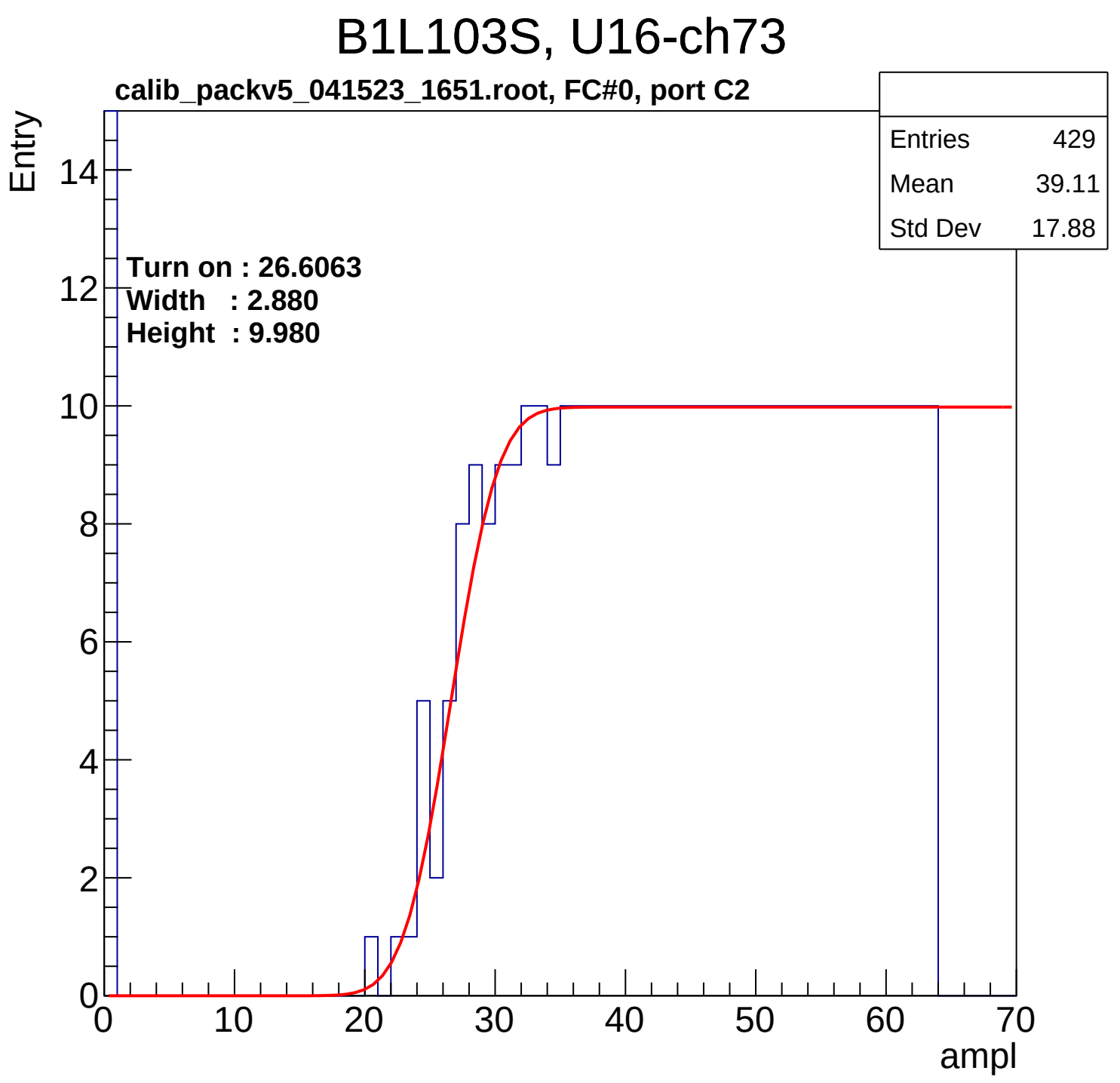
B1L103S, U16-ch73
calib_packv5_041523_1651.root, FC#0, port C2
Entries 429
Mean 39.11
Std Dev 17.88
Turn on : 26.6063
Width : 2.880
Height : 9.980
Entry
ampl
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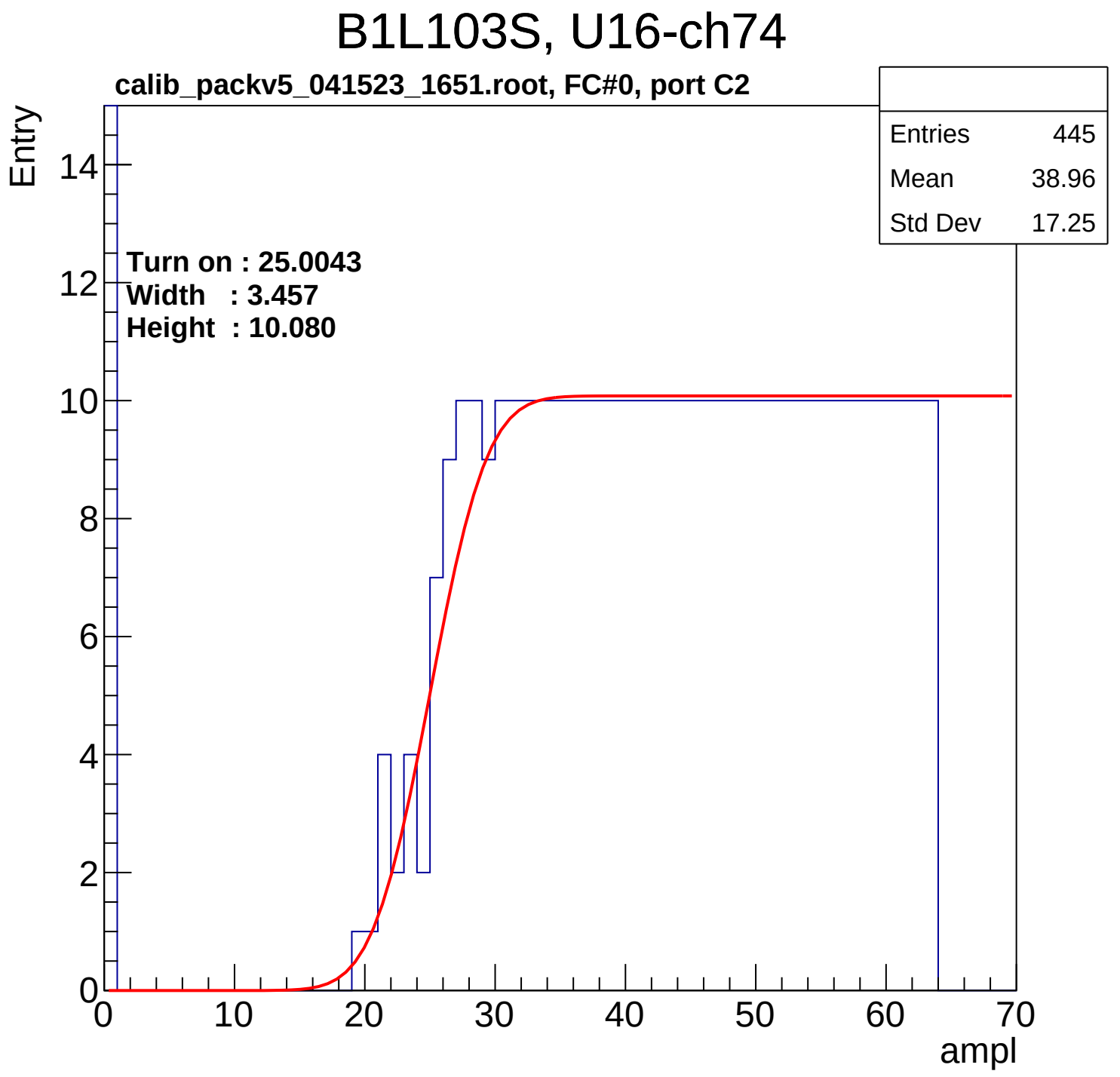
B1L103S, U16-ch74
calib_packv5_041523_1651.root, FC#0, port C2
Entries 445
Mean 38.96
Std Dev 17.25
Turn on : 25.0043
Width : 3.457
Height : 10.080
Entry
ampl
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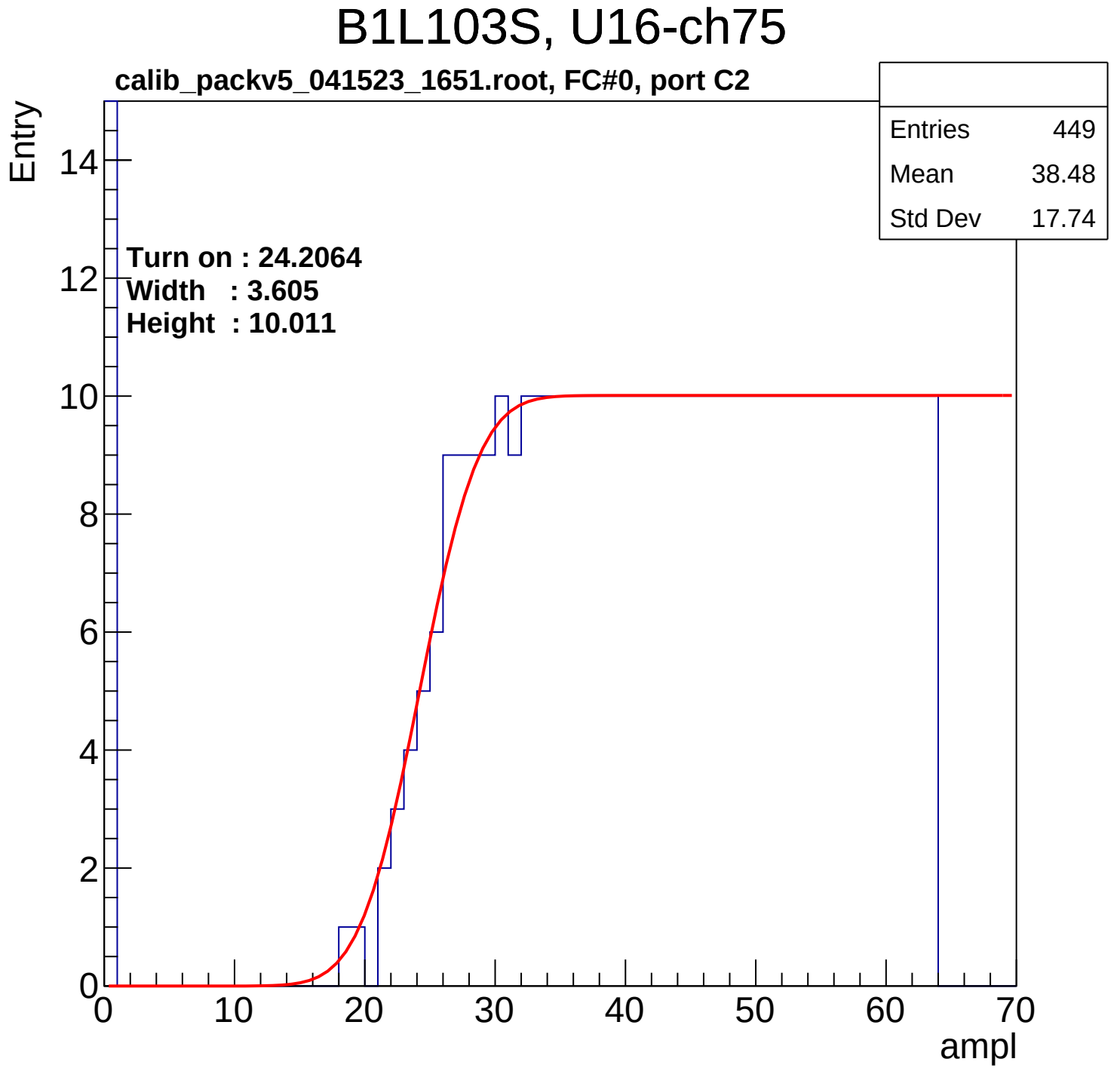
B1L103S, U16-ch75
calib_packv5_041523_1651.root, FC#0, port C2
Entries 449
Mean 38.48
Std Dev 17.74
Turn on : 24.2064
Width : 3.605
Height : 10.011
Entry
ampl
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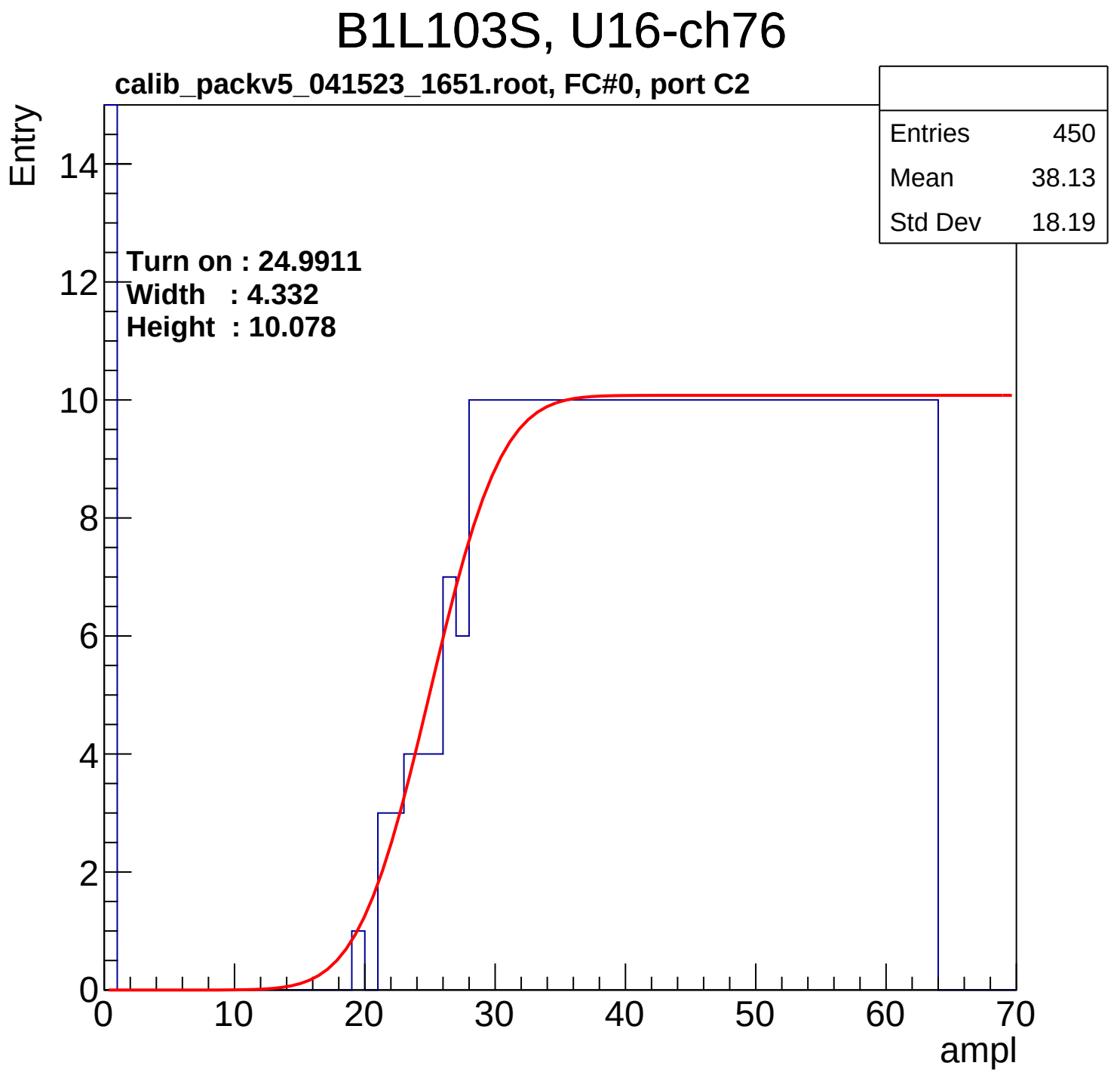
B1L103S, U16-ch76
calib_packv5_041523_1651.root, FC#0, port C2
Entries 450
Mean 38.13
Std Dev 18.19
Turn on : 24.9911
Width : 4.332
Height : 10.078
Entry
ampl
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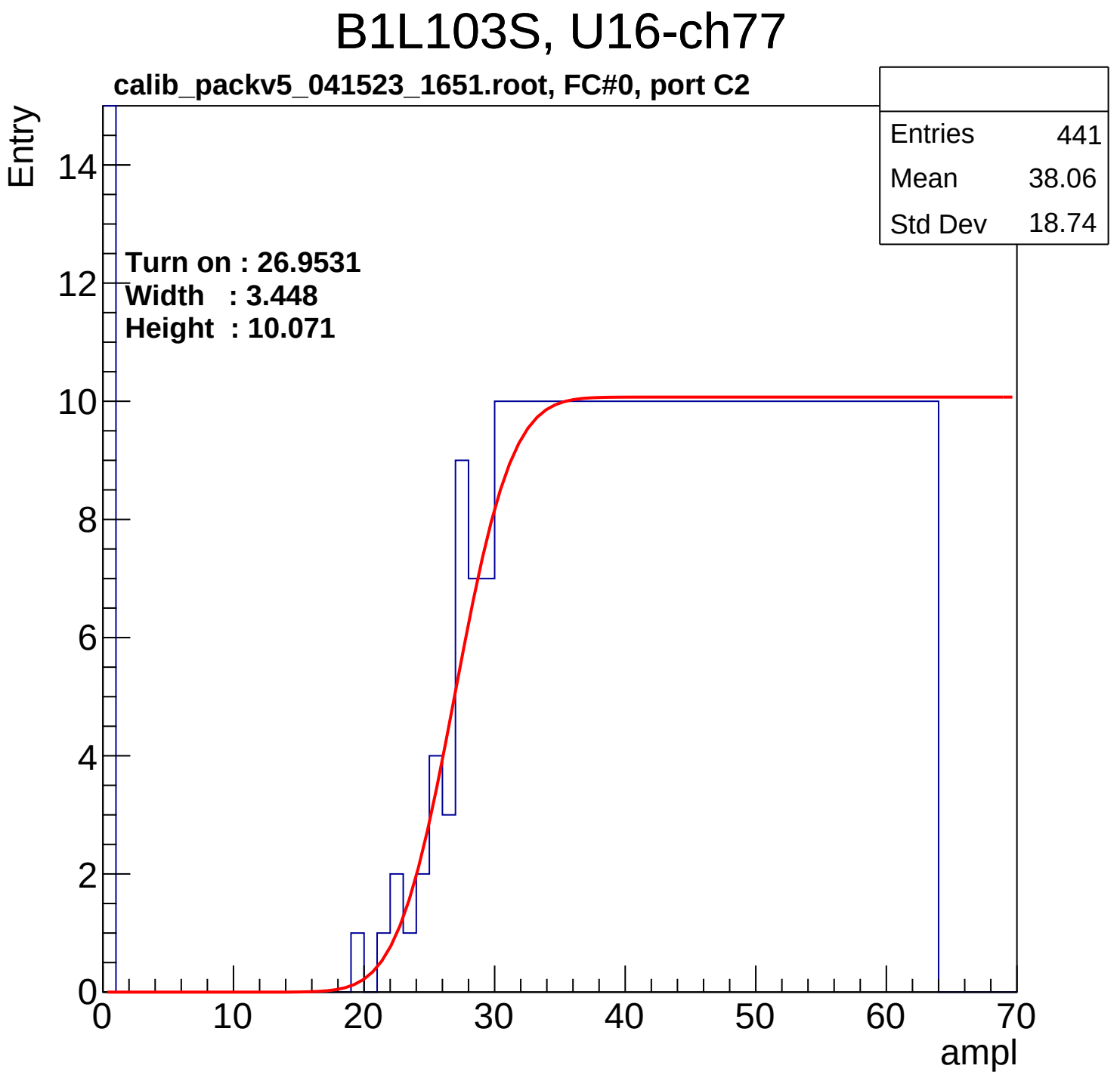
B1L103S, U16-ch77
calib_packv5_041523_1651.root, FC#0, port C2
Entries 441
Mean 38.06
Std Dev 18.74
Turn on : 26.9531
Width : 3.448
Height : 10.071
Entry
ampl
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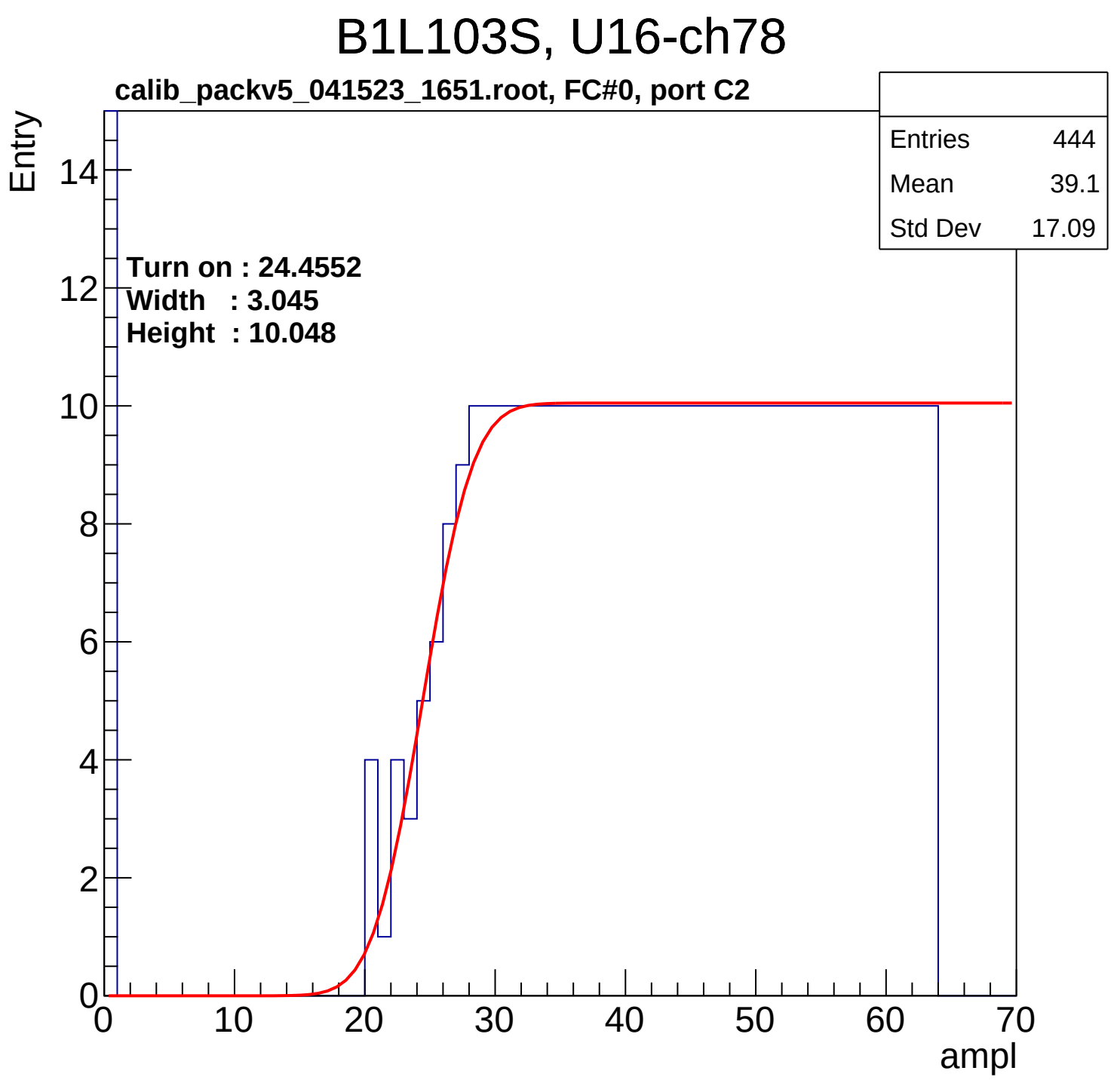
B1L103S, U16-ch78
calib_packv5_041523_1651.root, FC#0, port C2
Entries 444
Mean 39.1
Std Dev 17.09
Turn on : 24.4552
Width : 3.045
Height : 10.048
Entry
ampl
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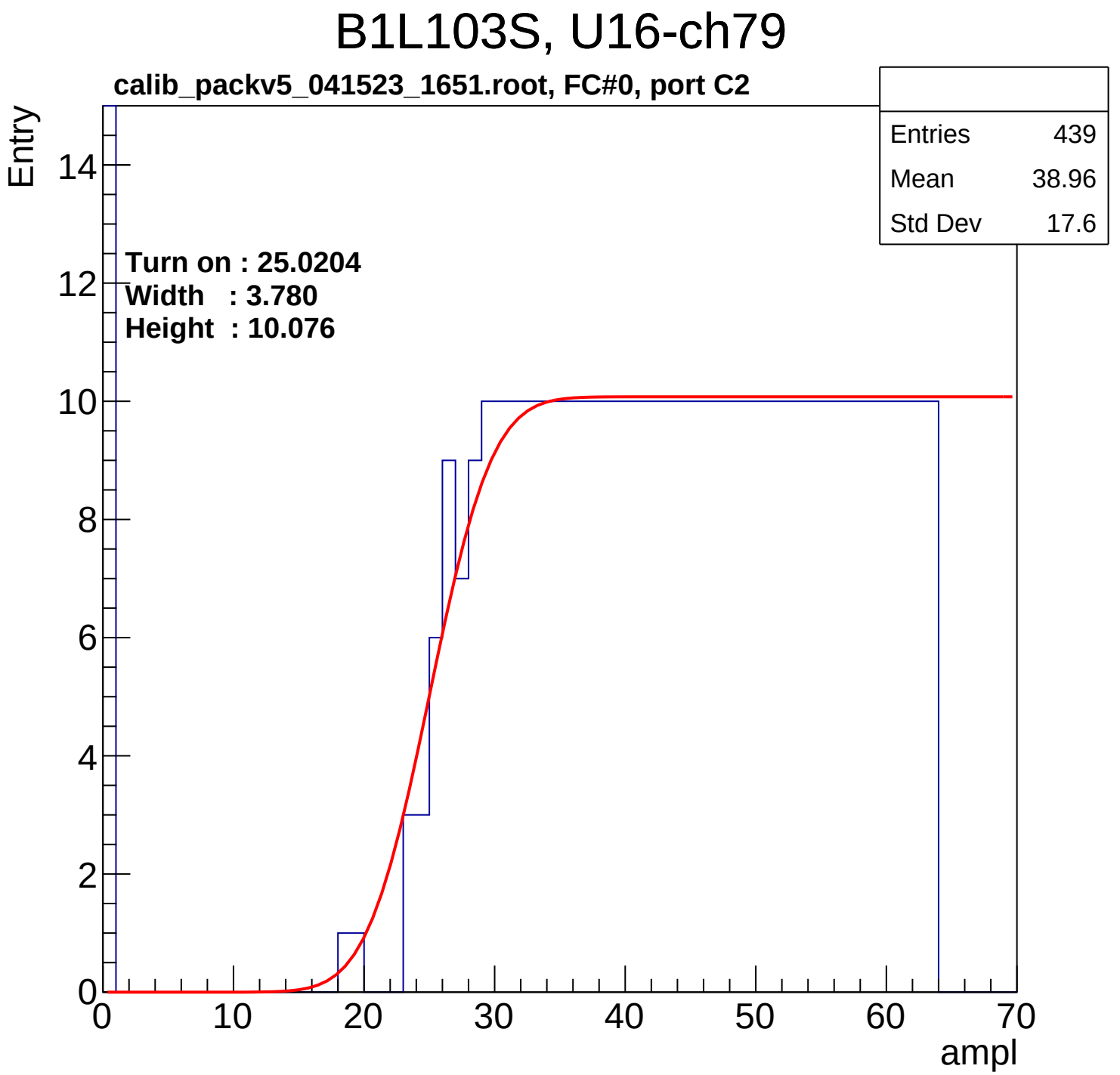
B1L103S, U16-ch79
calib_packv5_041523_1651.root, FC#0, port C2
Entries 439
Mean 38.96
Std Dev 17.6
Turn on : 25.0204
Width : 3.780
Height : 10.076
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ampl
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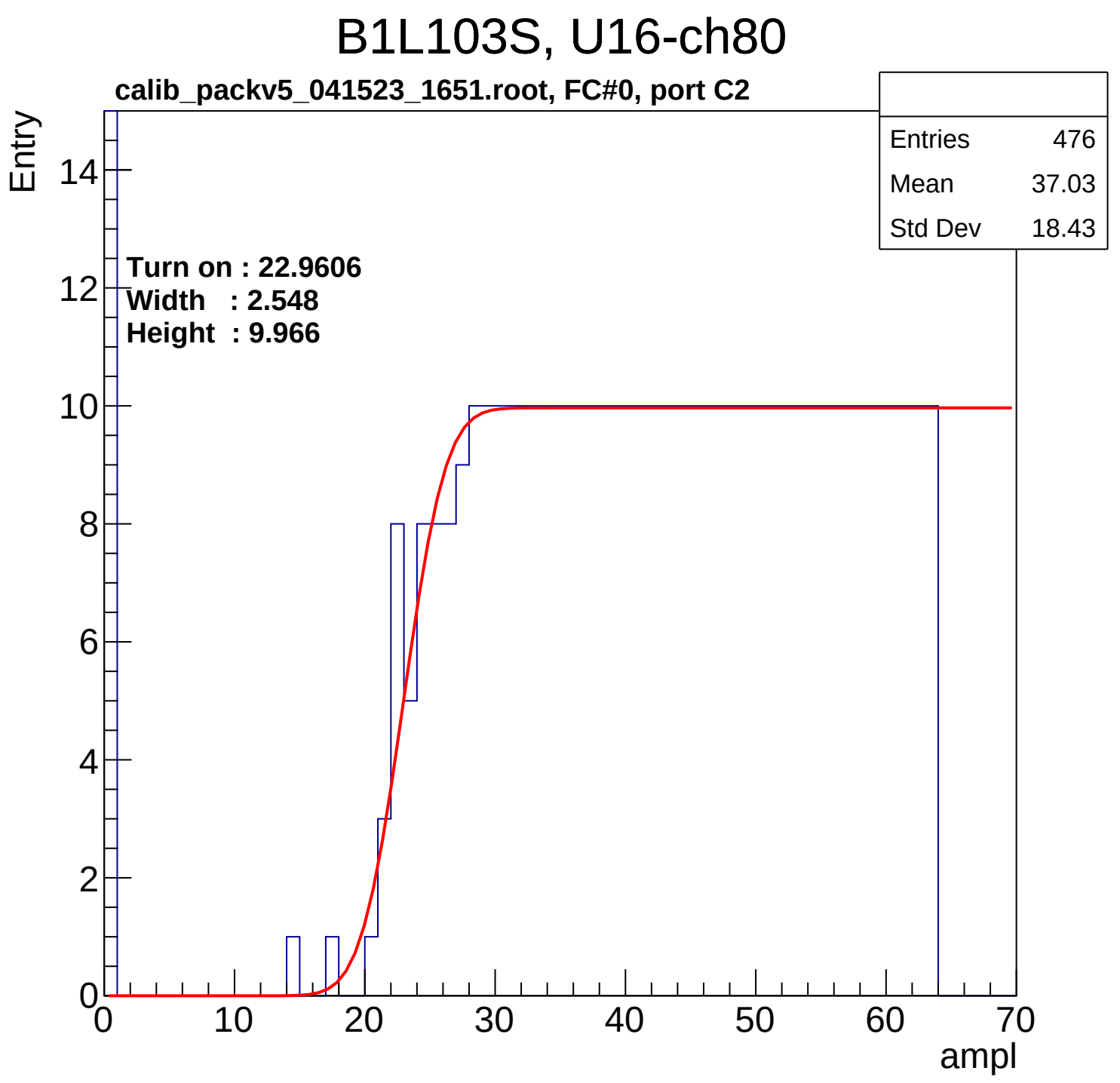
B1L103S, U16-ch80
calib_packv5_041523_1651.root, FC#0, port C2
Entries 476
Mean 37.03
Std Dev 18.43
Turn on : 22.9606
Width : 2.548
Height : 9.966
Entry
ampl
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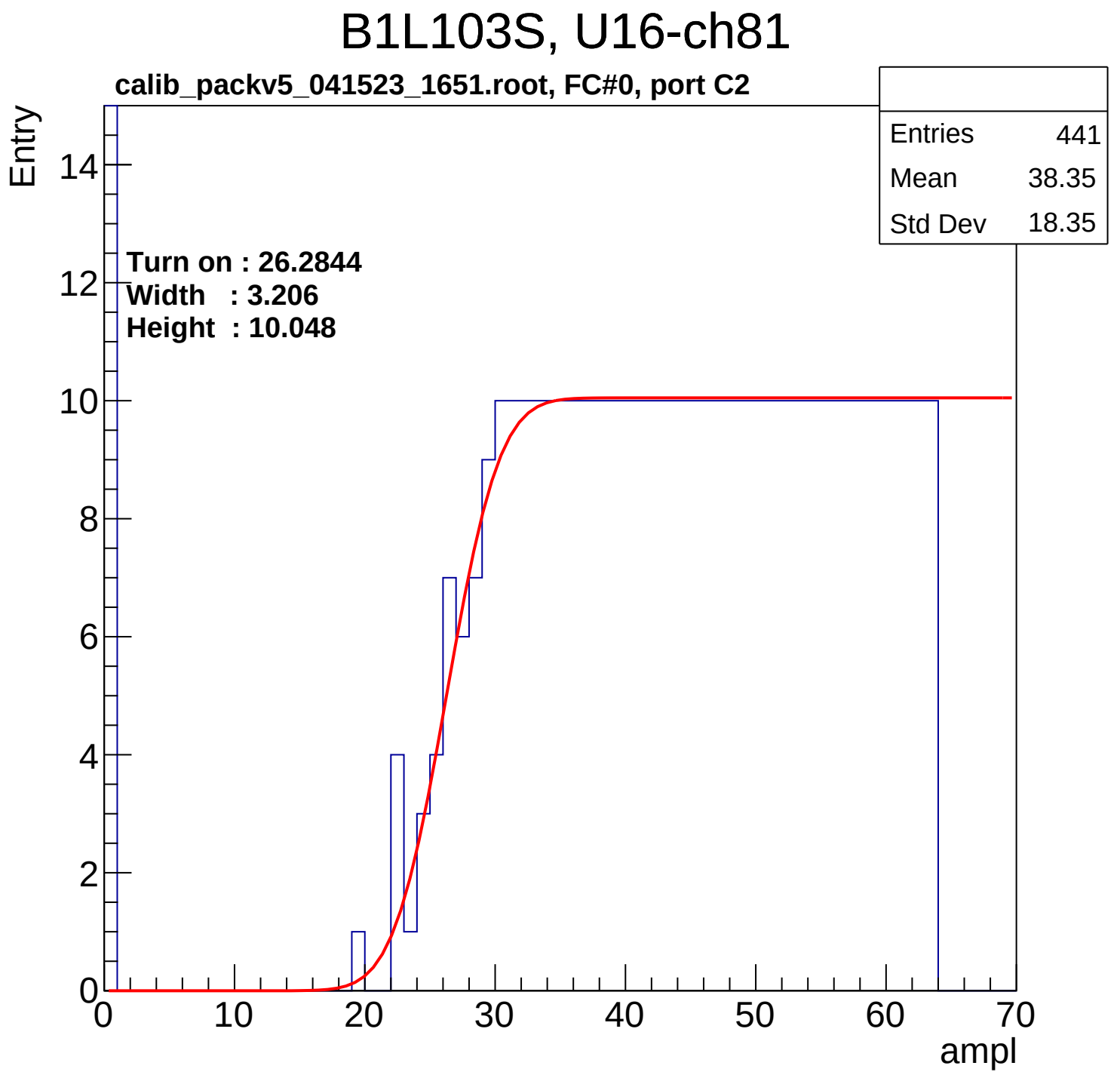
B1L103S, U16-ch81
calib_packv5_041523_1651.root, FC#0, port C2
Entries 441
Mean 38.35
Std Dev 18.35
Turn on : 26.2844
Width : 3.206
Height : 10.048
Entry
ampl
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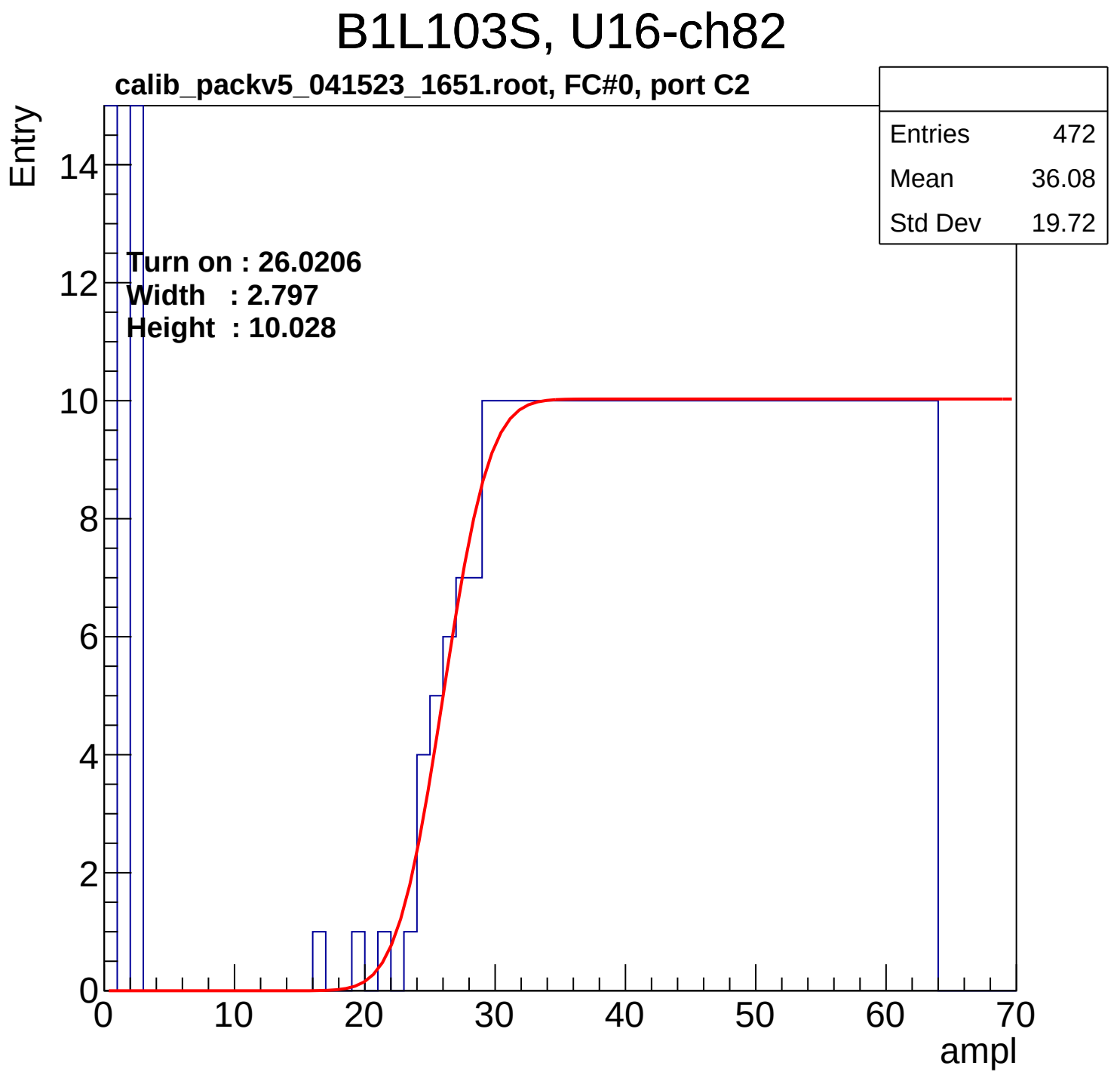
B1L103S, U16-ch82
calib_packv5_041523_1651.root, FC#0, port C2
Entries 472
Mean 36.08
Std Dev 19.72
Turn on : 26.0206
Width : 2.797
Height : 10.028
Entry
ampl
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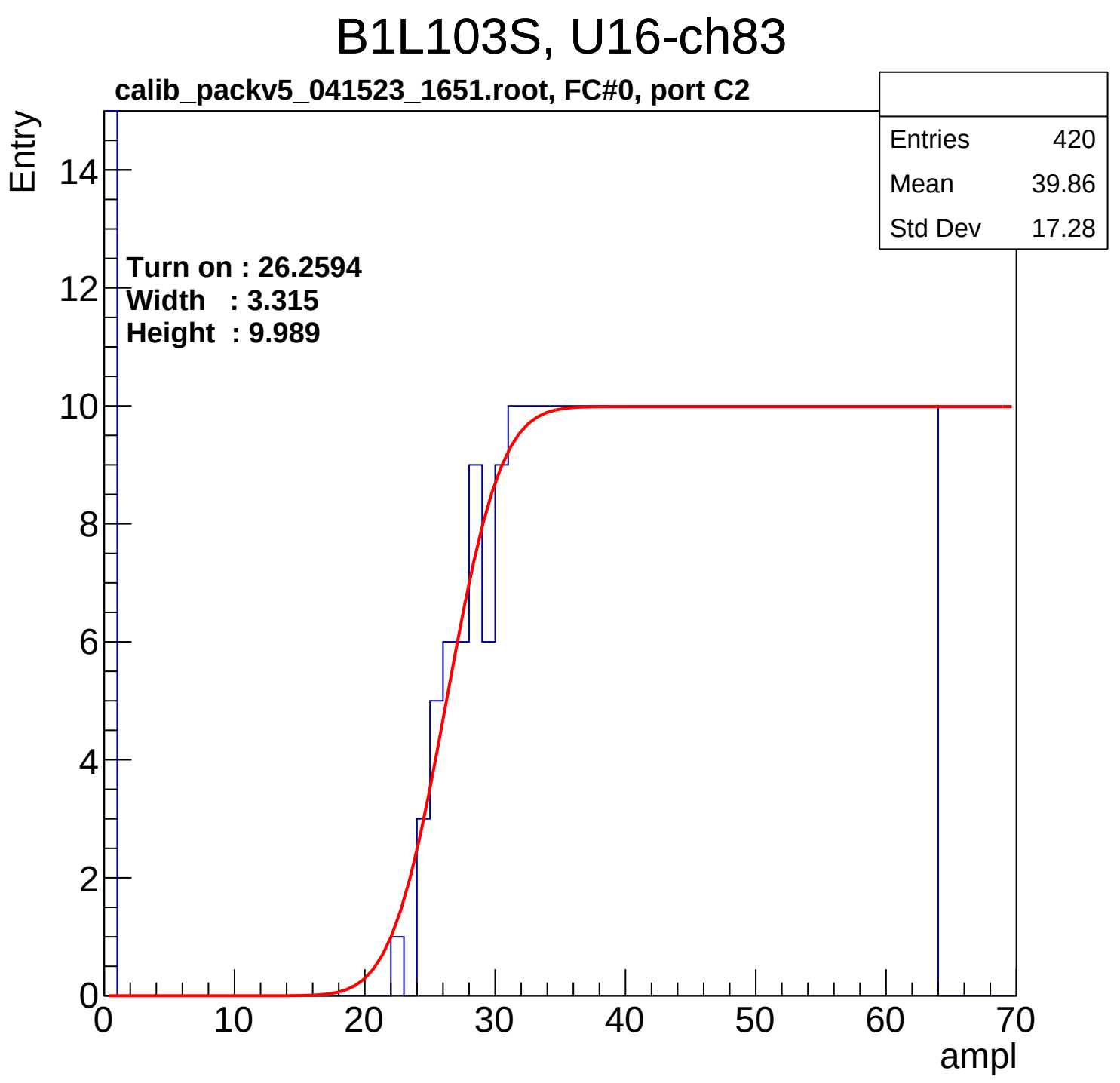
B1L103S, U16-ch83
calib_packv5_041523_1651.root, FC#0, port C2
Entries 420
Mean 39.86
Std Dev 17.28
Turn on : 26.2594
Width : 3.315
Height : 9.989
Entry
ampl
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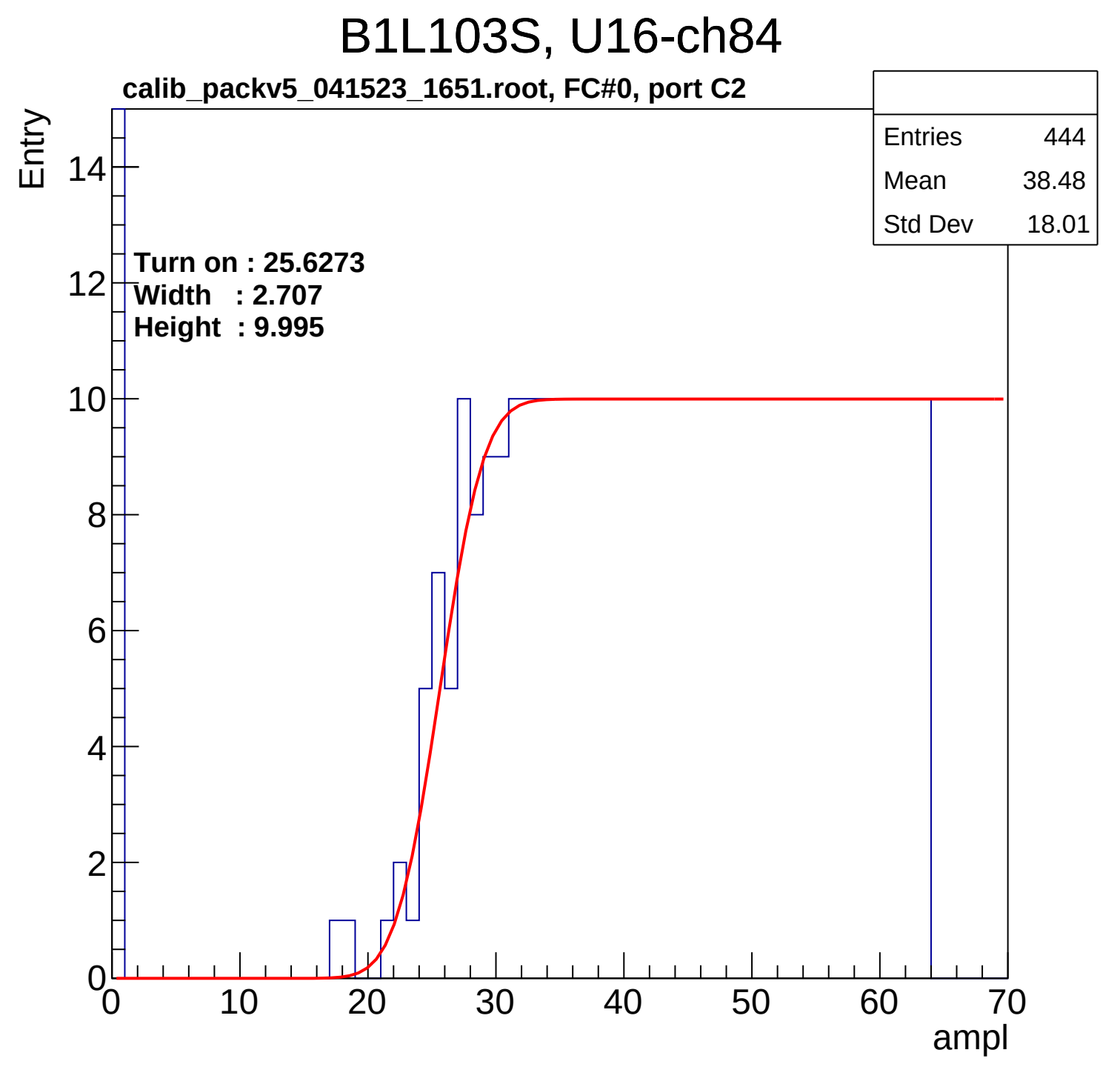
B1L103S, U16-ch84
calib_packv5_041523_1651.root, FC#0, port C2
Entries 444
Mean 38.48
Std Dev 18.01
Turn on : 25.6273
Width : 2.707
Height : 9.995
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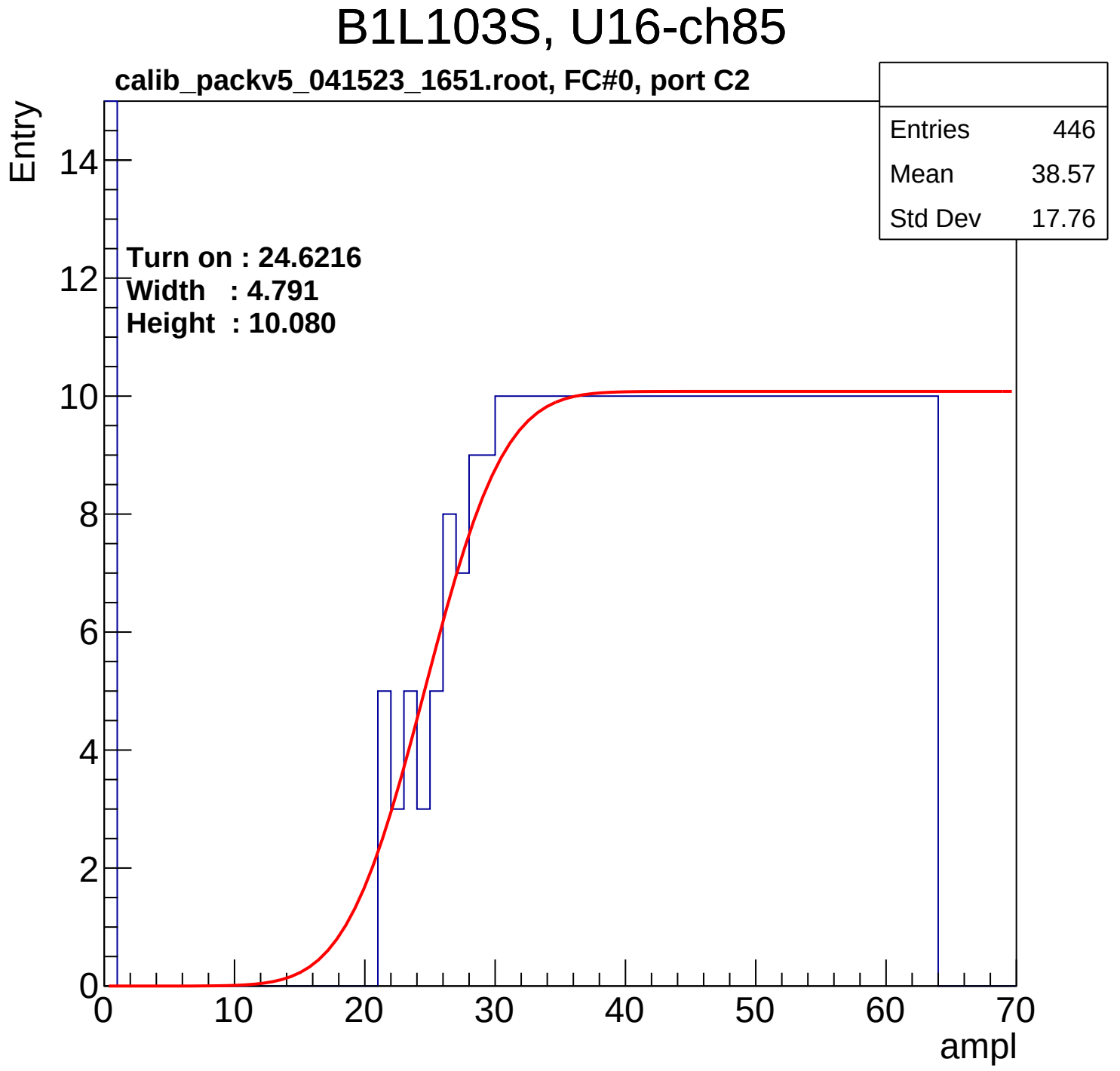
B1L103S, U16-ch85
calib_packv5_041523_1651.root, FC#0, port C2
Entries 446
Mean 38.57
Std Dev 17.76
Turn on : 24.6216
Width : 4.791
Height : 10.080
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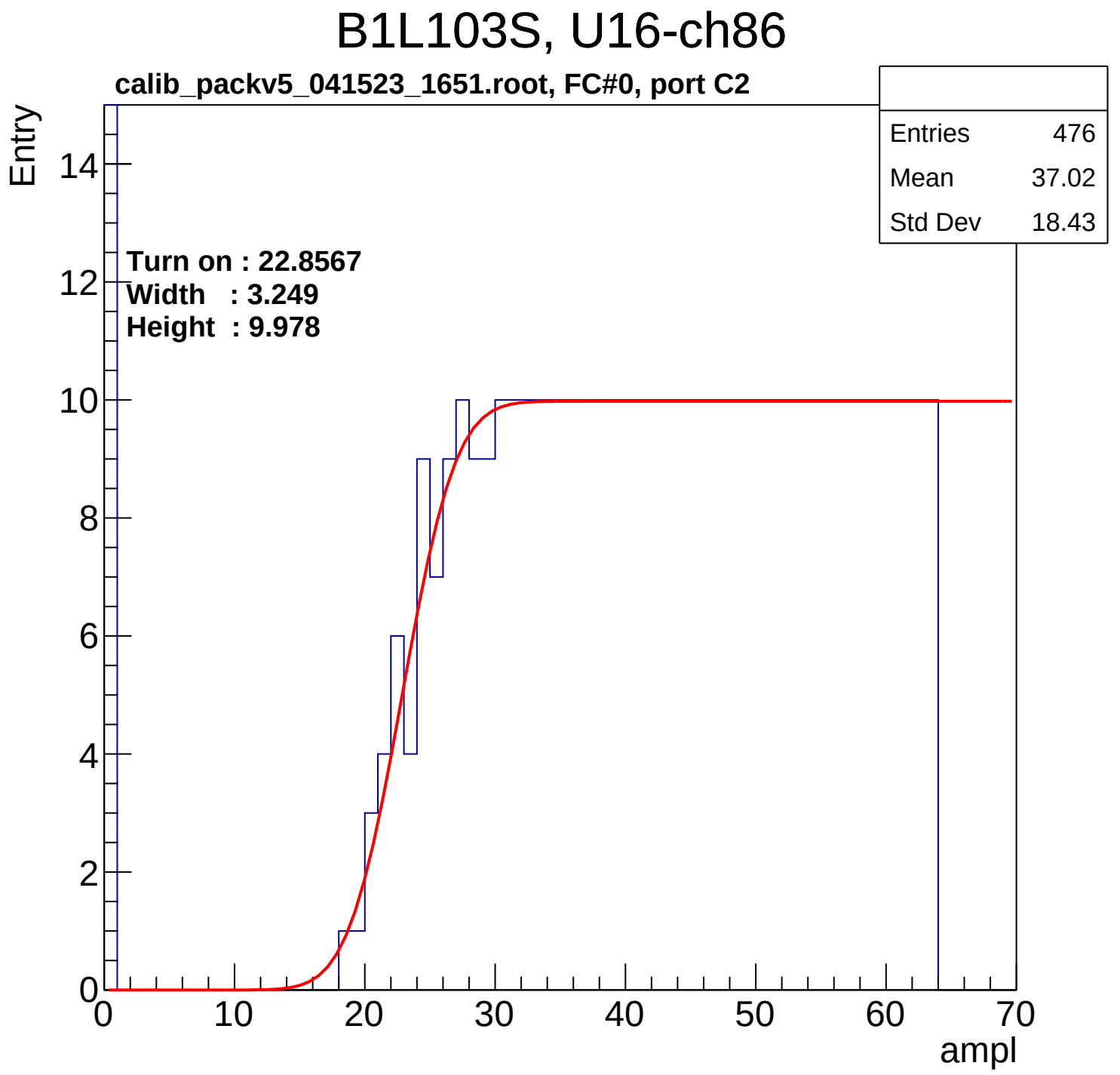
B1L103S, U16-ch86
calib_packv5_041523_1651.root, FC#0, port C2
Entries 476
Mean 37.02
Std Dev 18.43
Turn on : 22.8567
Width : 3.249
Height : 9.978
Entry
ampl
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6
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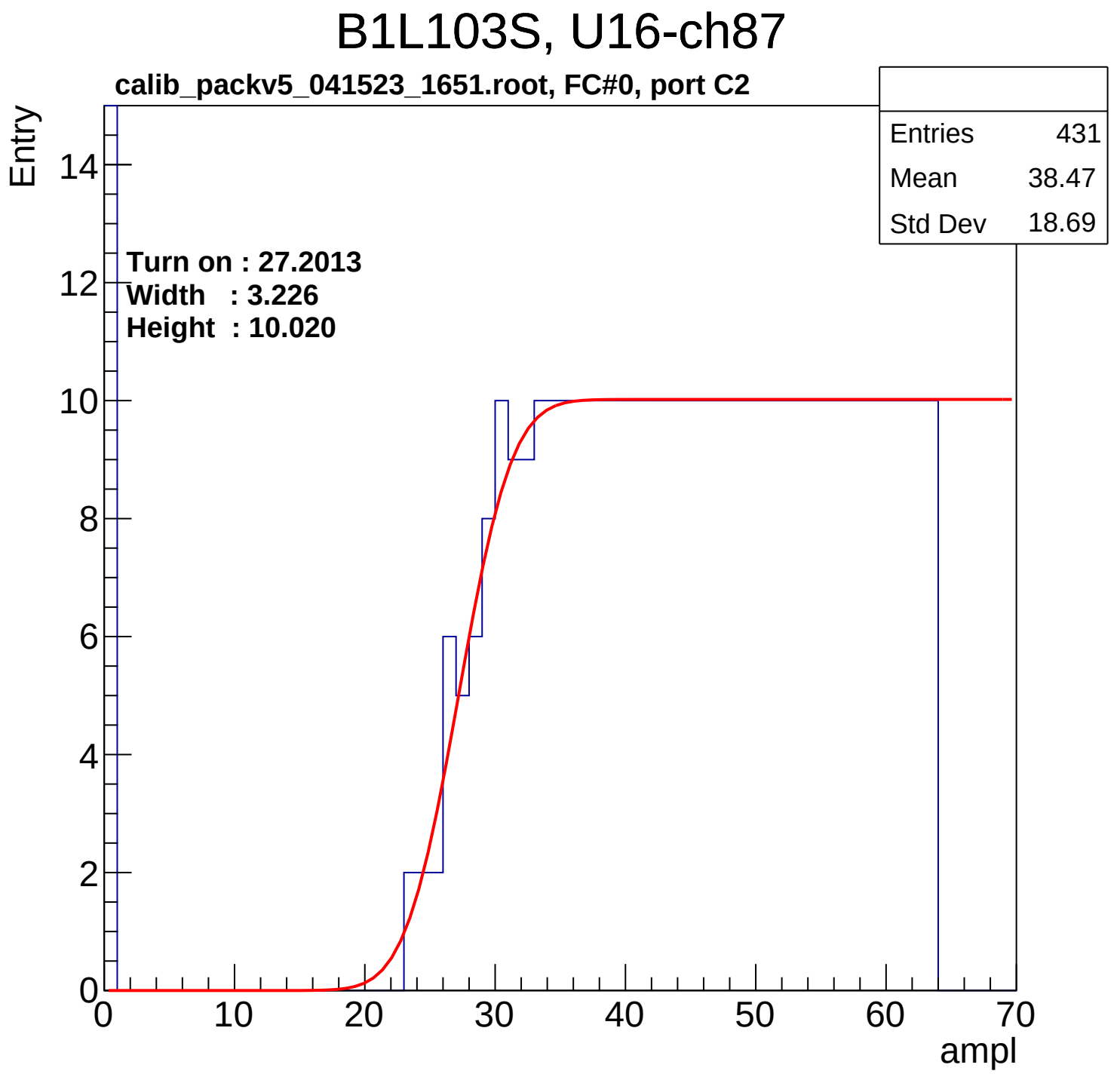
B1L103S, U16-ch87
calib_packv5_041523_1651.root, FC#0, port C2
Entries 431
Mean 38.47
Std Dev 18.69
Turn on : 27.2013
Width : 3.226
Height : 10.020
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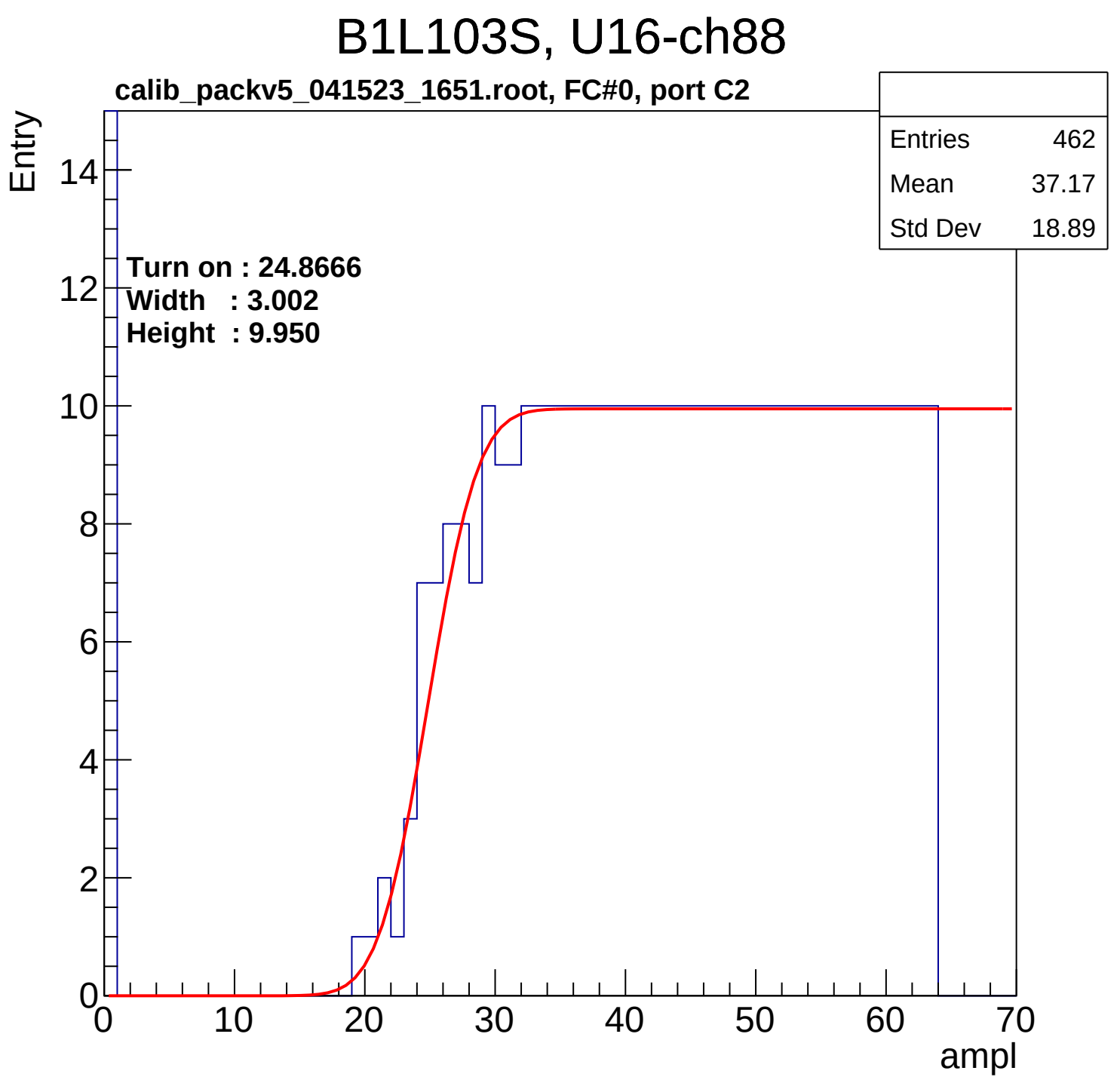
B1L103S, U16-ch88
calib_packv5_041523_1651.root, FC#0, port C2
Entries 462
Mean 37.17
Std Dev 18.89
Turn on : 24.8666
Width : 3.002
Height : 9.950
Entry
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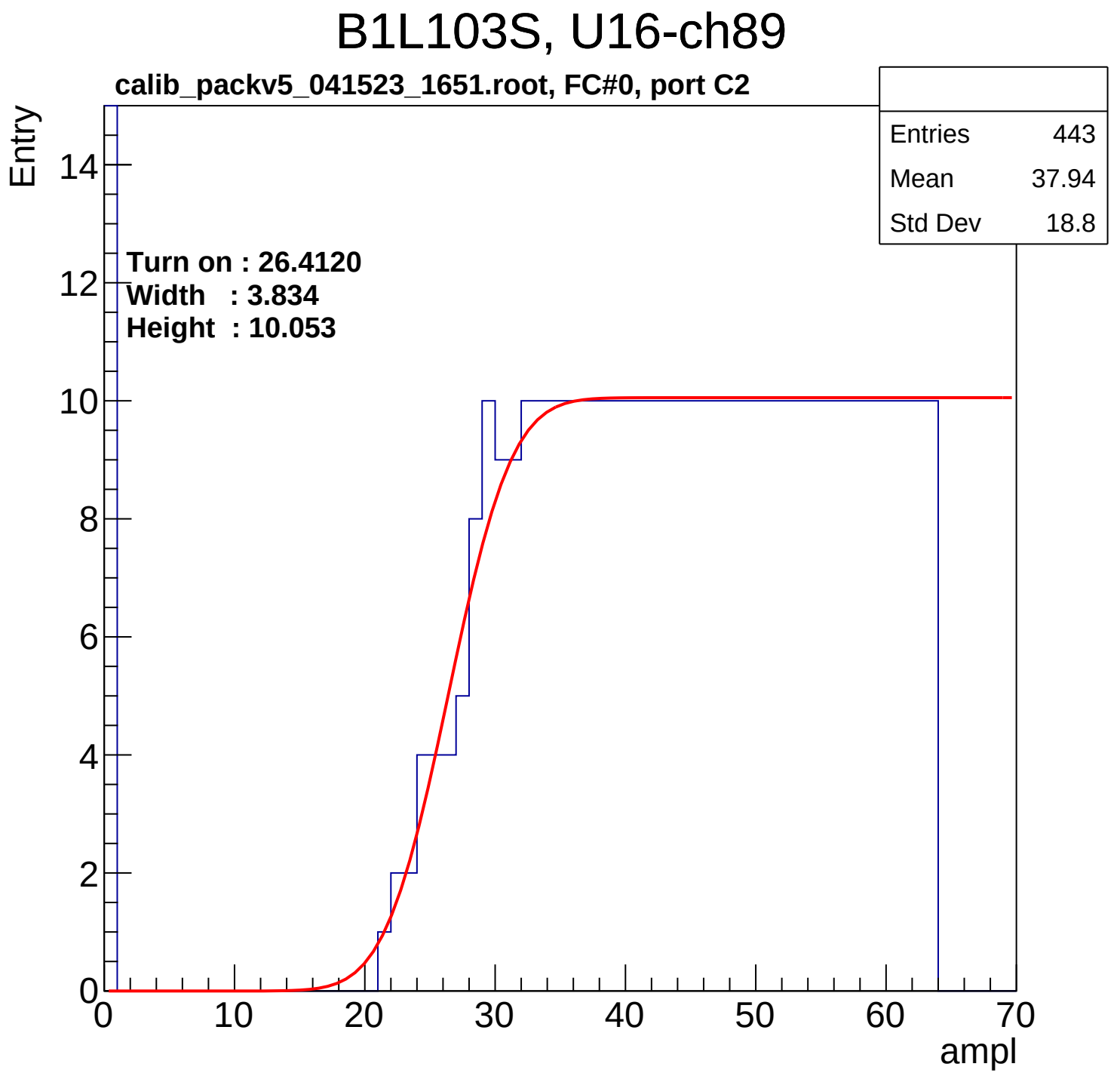
B1L103S, U16-ch89
calib_packv5_041523_1651.root, FC#0, port C2
Entries 443
Mean 37.94
Std Dev 18.8
Turn on : 26.4120
Width : 3.834
Height : 10.053
Entry
ampl
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4
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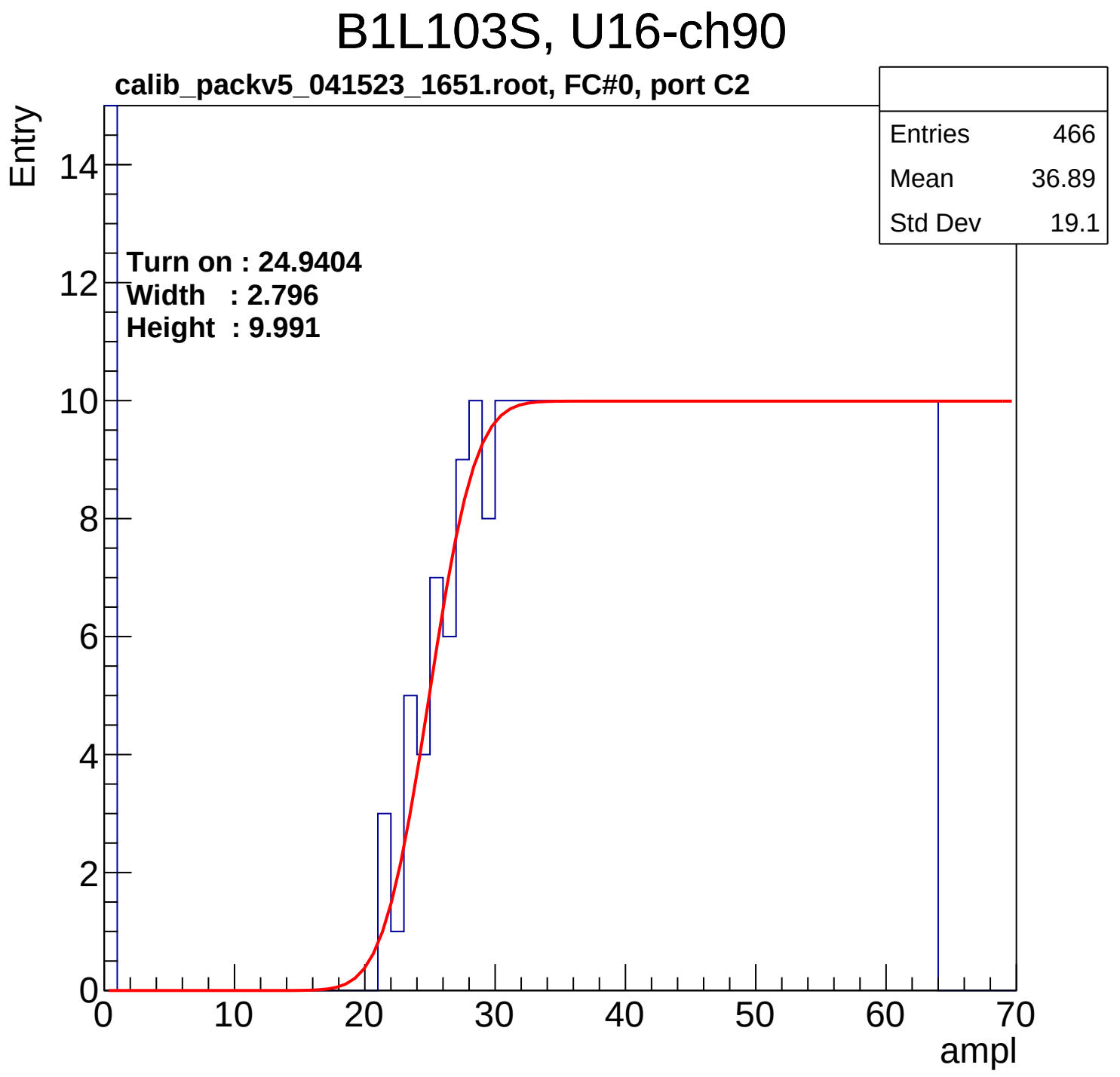
B1L103S, U16-ch90
calib_packv5_041523_1651.root, FC#0, port C2
Entries 466
Mean 36.89
Std Dev 19.1
Turn on : 24.9404
Width : 2.796
Height : 9.991
Entry
ampl
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2
4
6
8
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0
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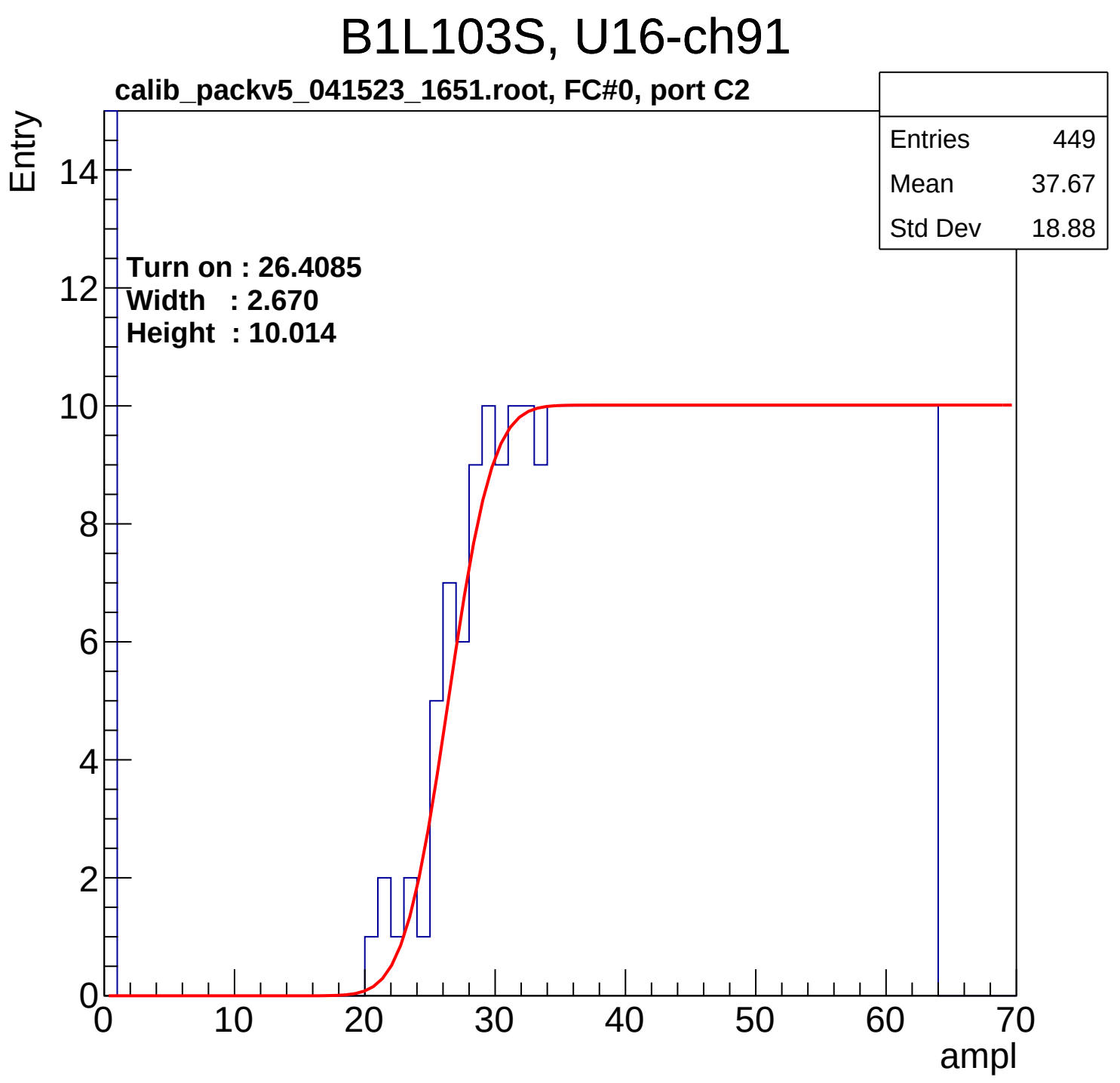
B1L103S, U16-ch91
calib_packv5_041523_1651.root, FC#0, port C2
Entries 449
Mean 37.67
Std Dev 18.88
Turn on : 26.4085
Width : 2.670
Height : 10.014
Entry
ampl
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2
4
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8
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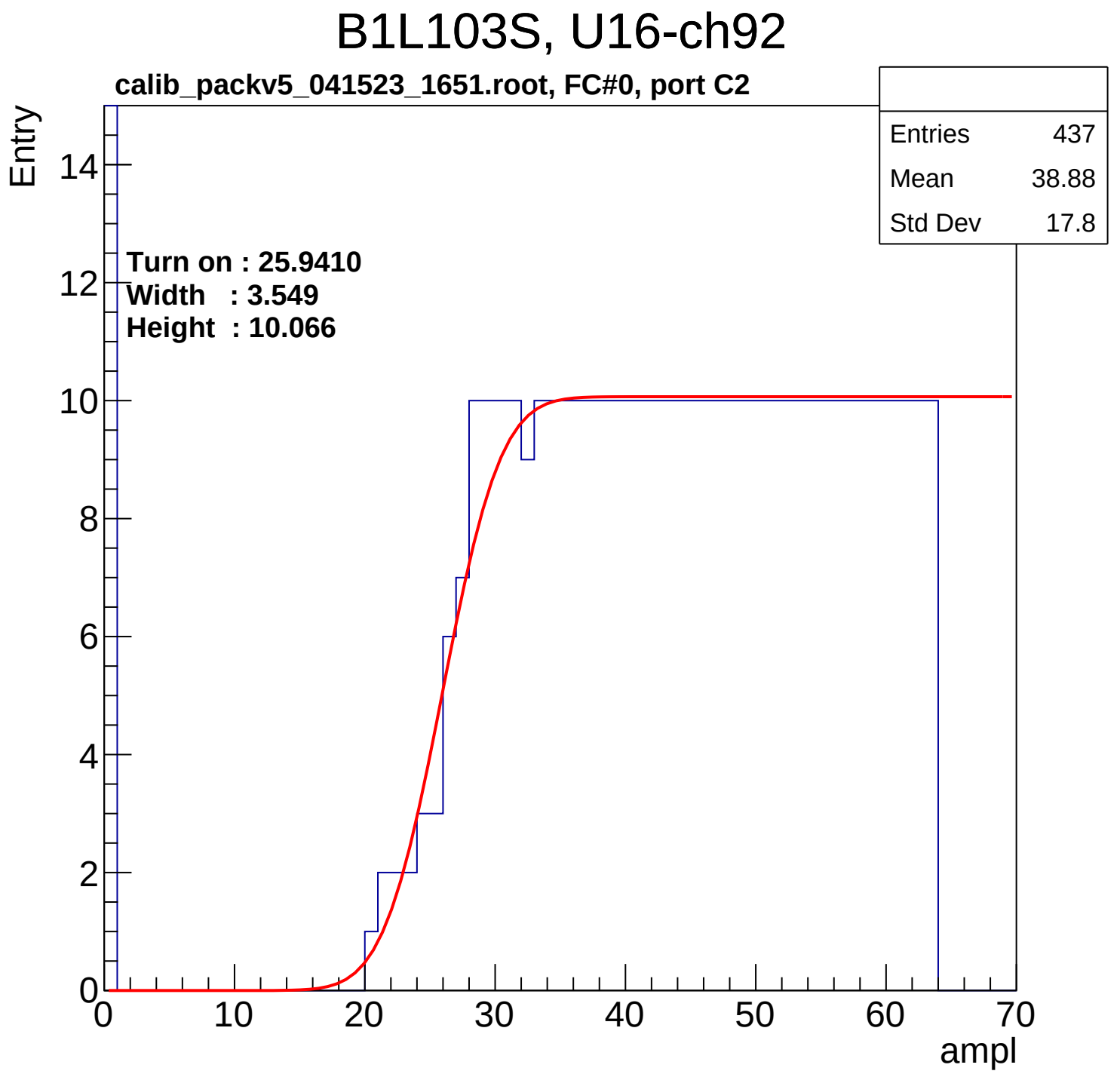
B1L103S, U16-ch92
calib_packv5_041523_1651.root, FC#0, port C2
Entries 437
Mean 38.88
Std Dev 17.8
Turn on : 25.9410
Width : 3.549
Height : 10.066
Entry
ampl
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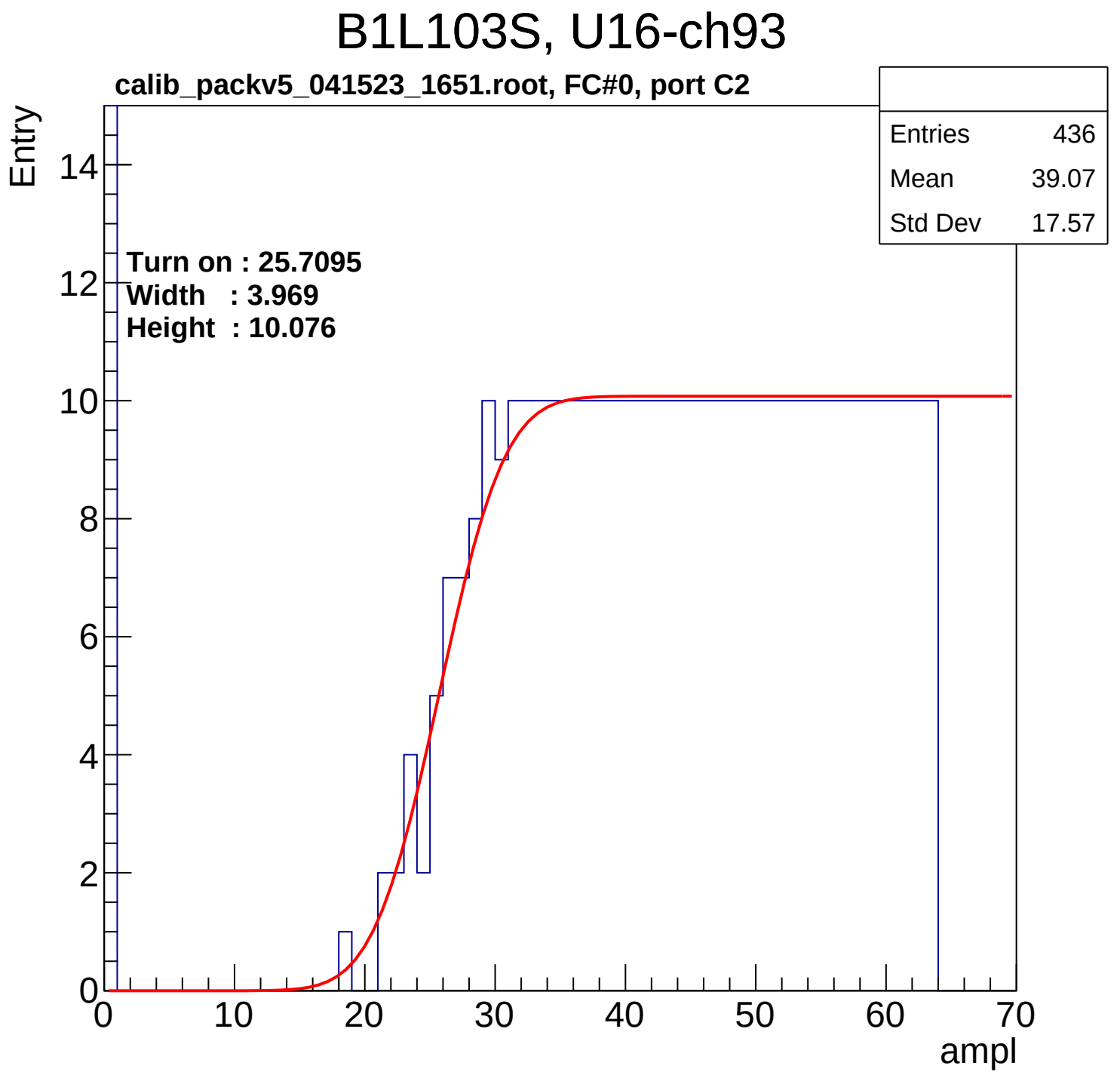
B1L103S, U16-ch93
calib_packv5_041523_1651.root, FC#0, port C2
Entries 436
Mean 39.07
Std Dev 17.57
Turn on : 25.7095
Width : 3.969
Height : 10.076
Entry
ampl
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2
4
6
8
10
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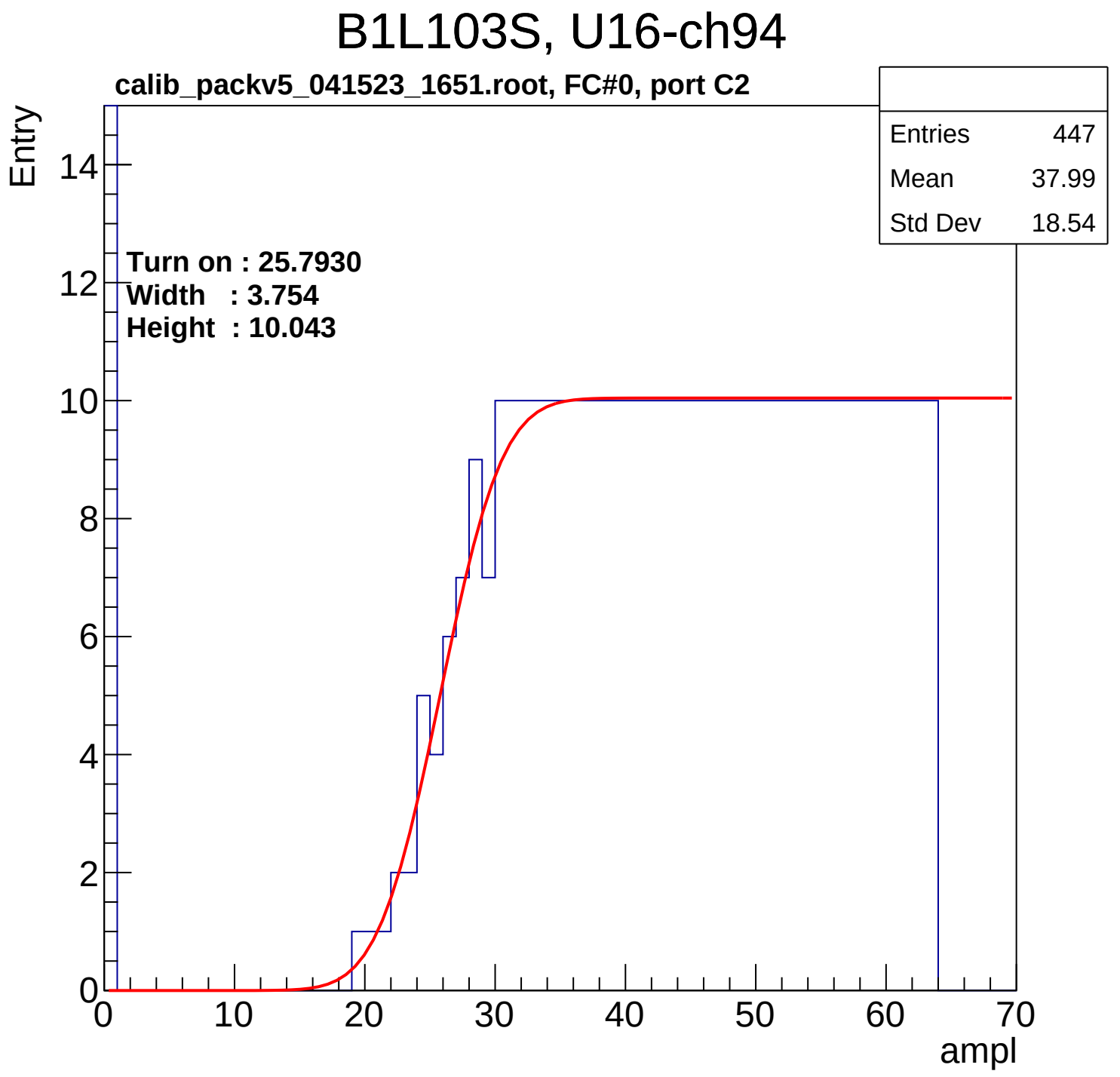
B1L103S, U16-ch94
calib_packv5_041523_1651.root, FC#0, port C2
Entries 447
Mean 37.99
Std Dev 18.54
Turn on : 25.7930
Width : 3.754
Height : 10.043
Entry
ampl
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2
4
6
8
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12
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60
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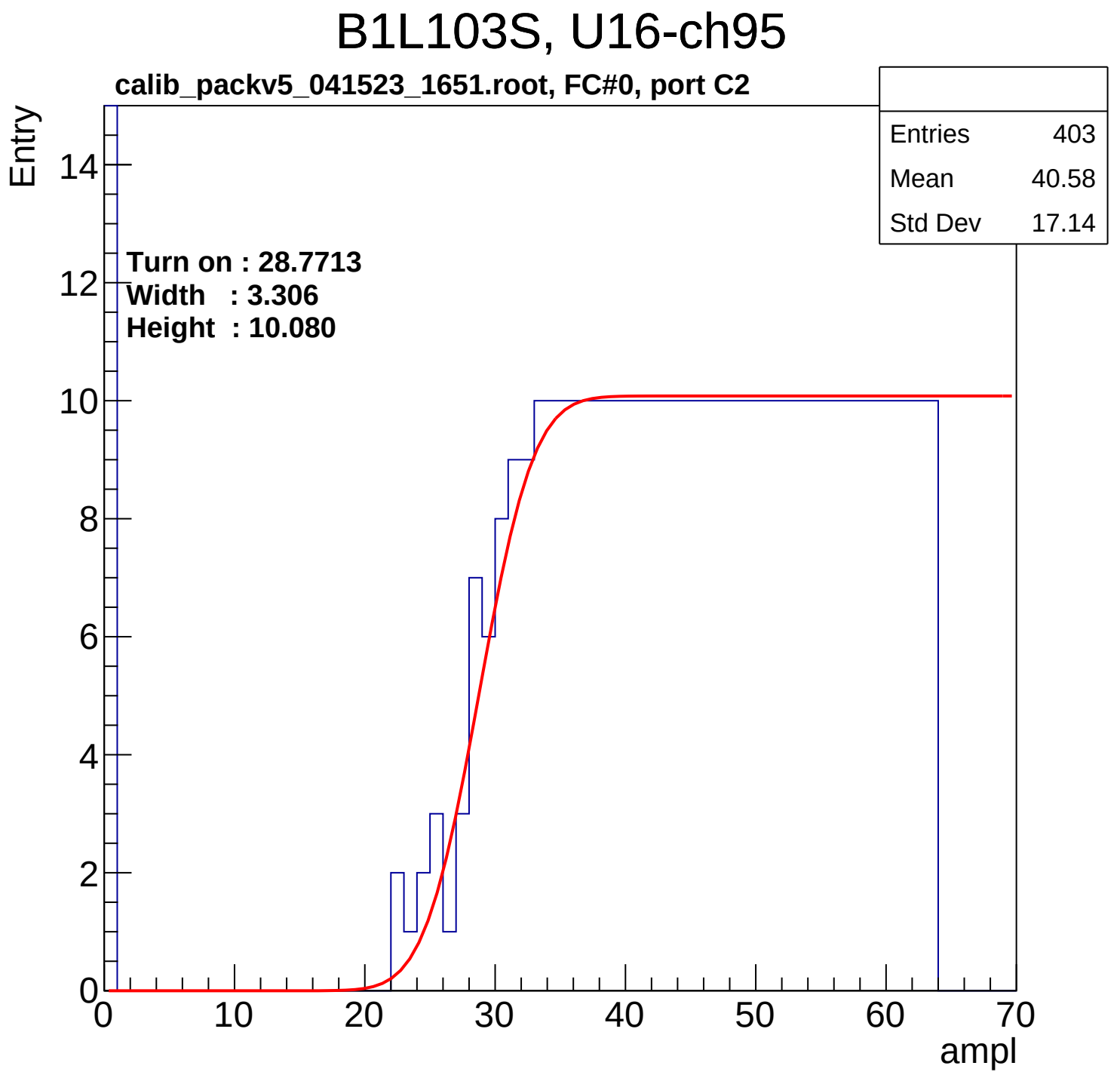
B1L103S, U16-ch95
calib_packv5_041523_1651.root, FC#0, port C2
Entries 403
Mean 40.58
Std Dev 17.14
Turn on : 28.7713
Width : 3.306
Height : 10.080
Entry
ampl
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6
8
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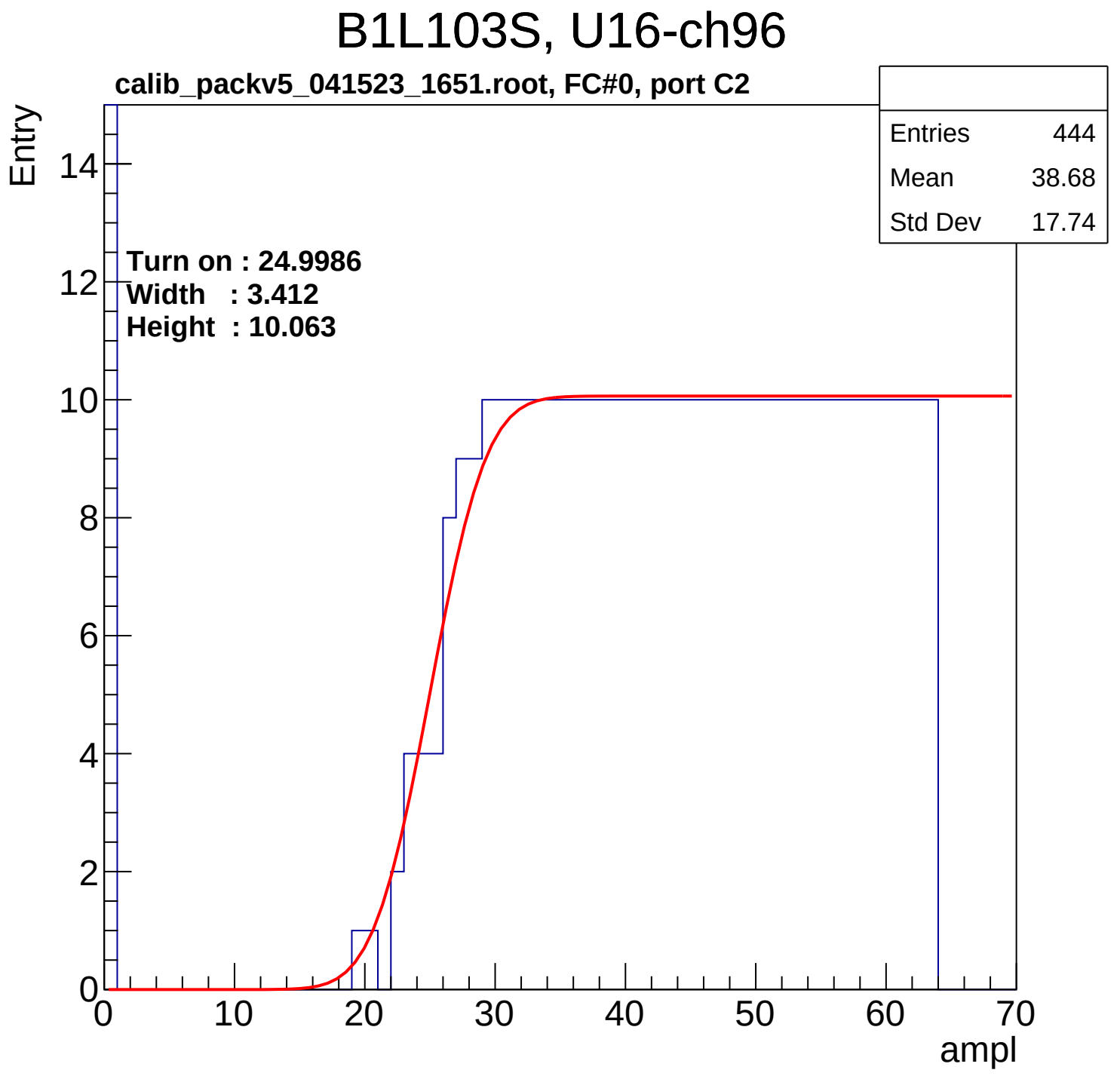
B1L103S, U16-ch96
calib_packv5_041523_1651.root, FC#0, port C2
Entries 444
Mean 38.68
Std Dev 17.74
Turn on : 24.9986
Width : 3.412
Height : 10.063
Entry
ampl
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10
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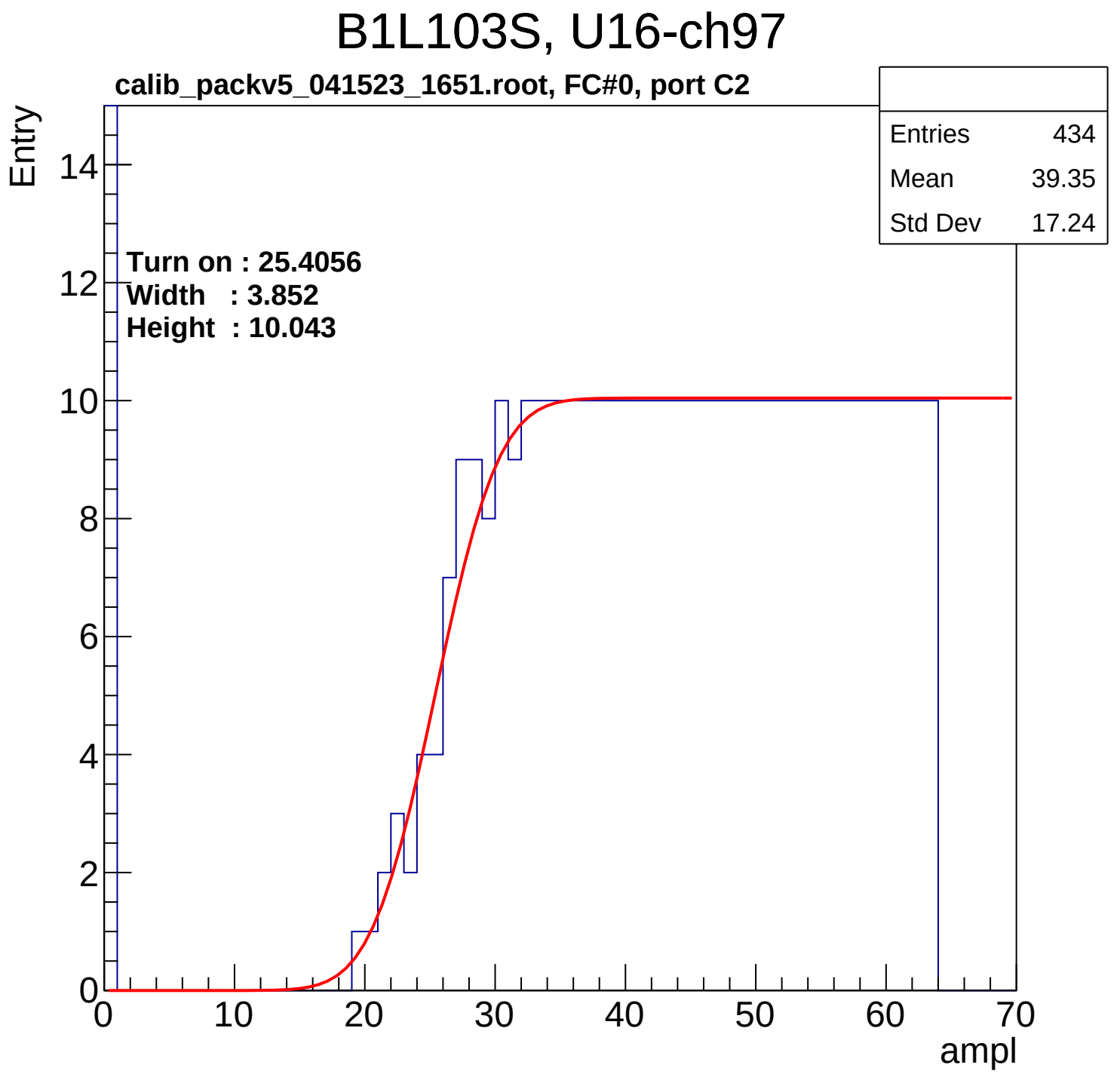
B1L103S, U16-ch97
calib_packv5_041523_1651.root, FC#0, port C2
Entries 434
Mean 39.35
Std Dev 17.24
Turn on : 25.4056
Width : 3.852
Height : 10.043
Entry
ampl
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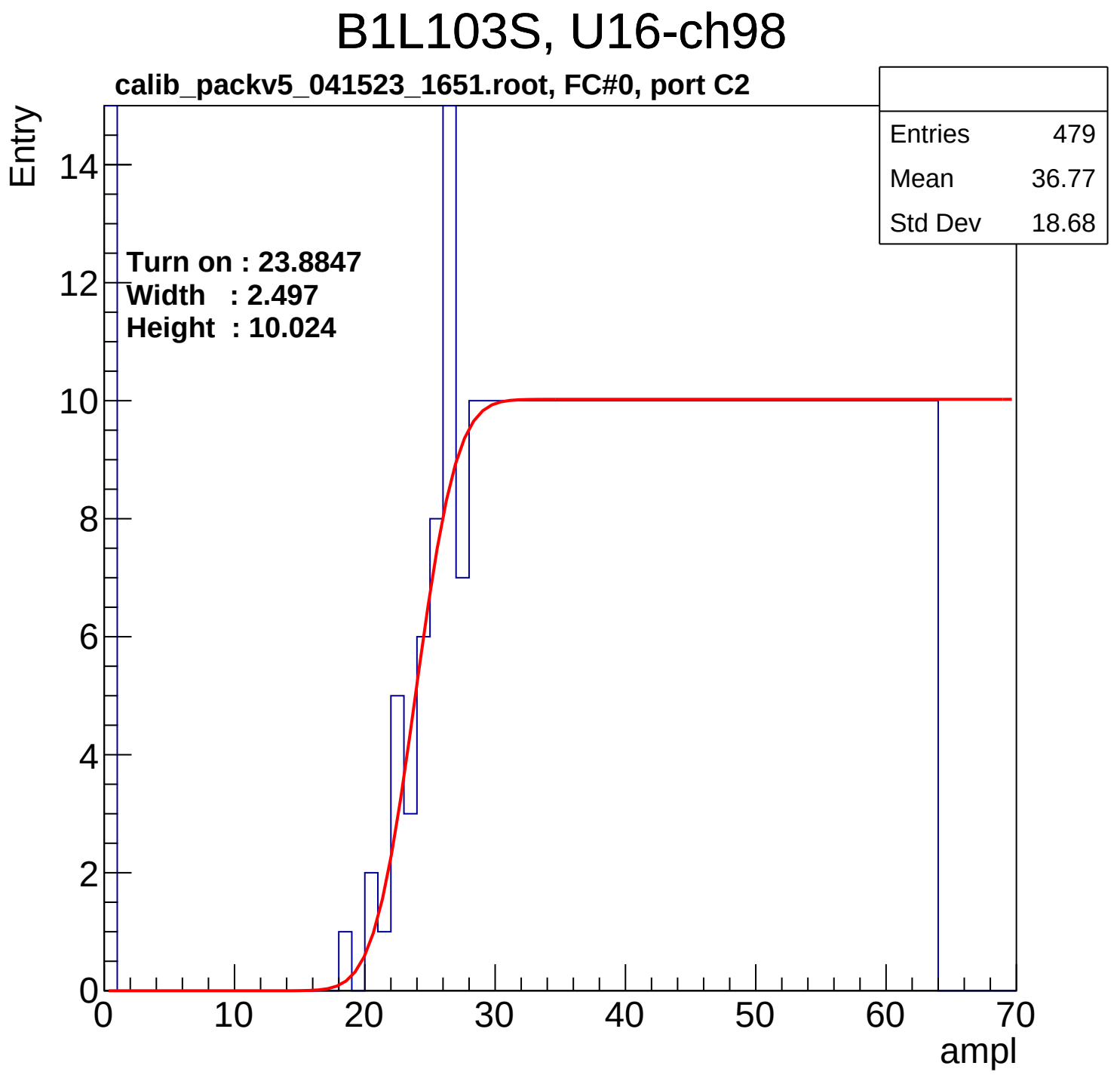
B1L103S, U16-ch98
calib_packv5_041523_1651.root, FC#0, port C2
Entries 479
Mean 36.77
Std Dev 18.68
Turn on : 23.8847
Width : 2.497
Height : 10.024
Entry
ampl
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6
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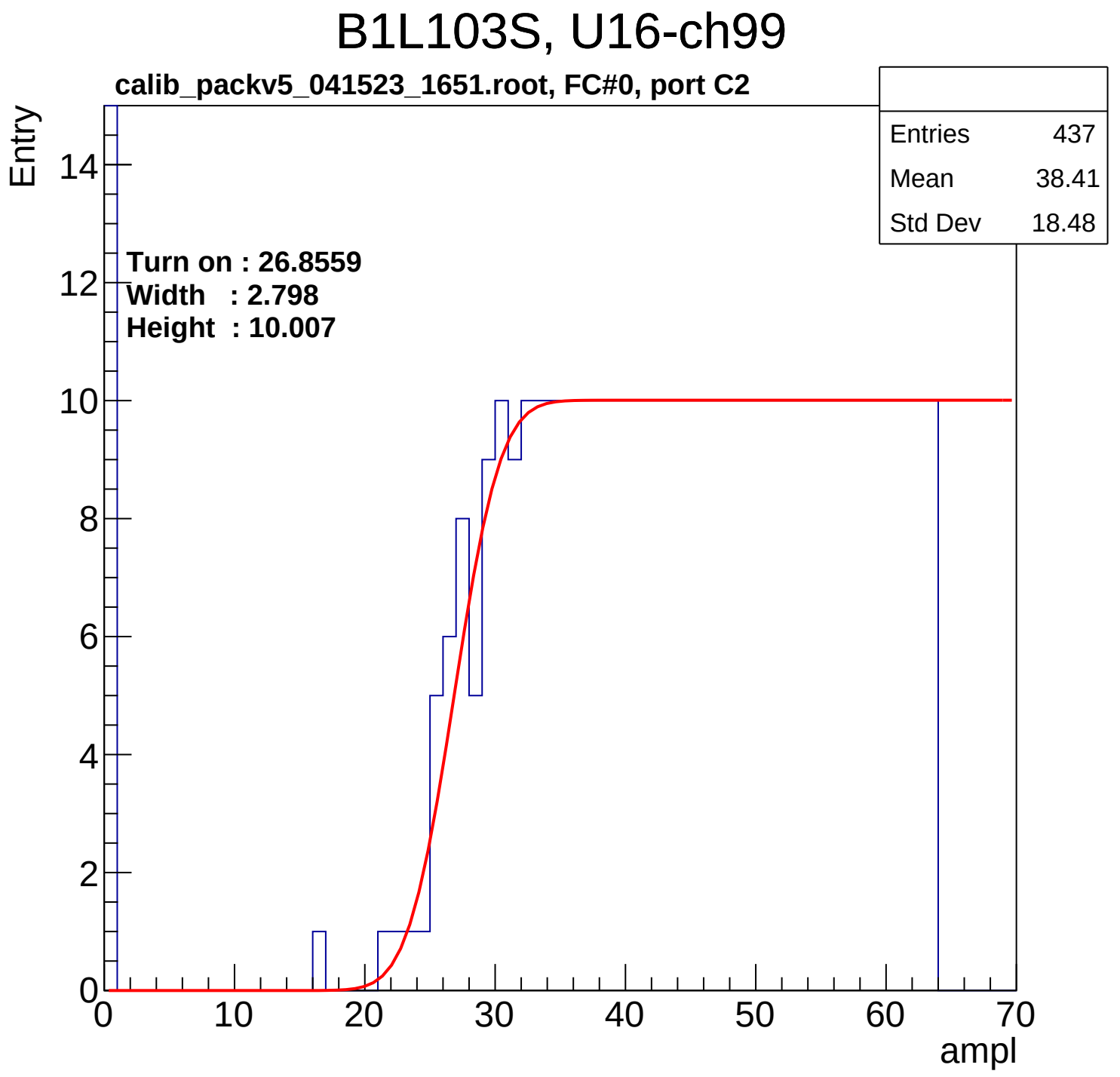
B1L103S, U16-ch99
calib_packv5_041523_1651.root, FC#0, port C2
Entries 437
Mean 38.41
Std Dev 18.48
Turn on : 26.8559
Width : 2.798
Height : 10.007
Entry
ampl
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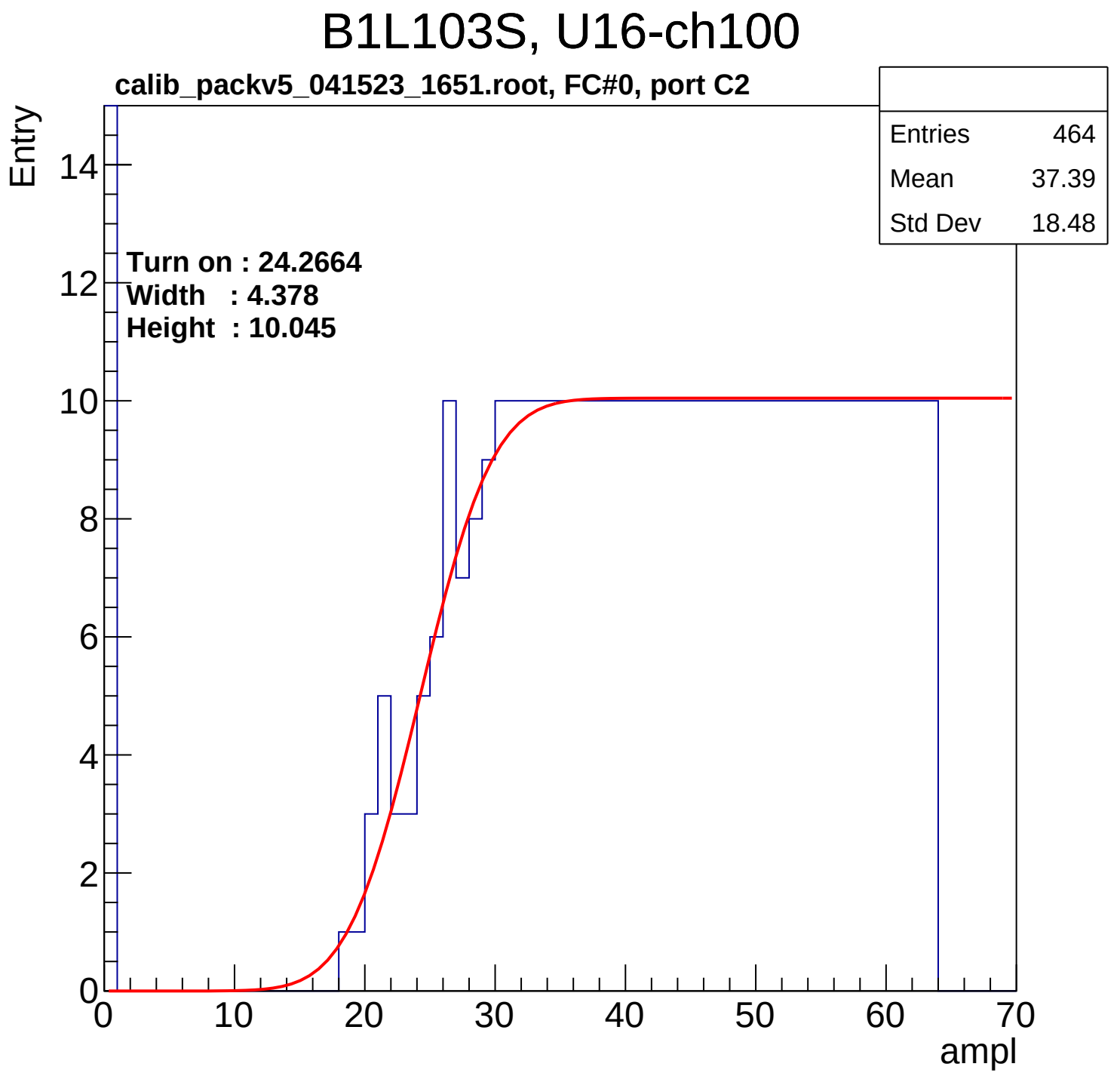
B1L103S, U16-ch100
calib_packv5_041523_1651.root, FC#0, port C2
Entries 464
Mean 37.39
Std Dev 18.48
Turn on : 24.2664
Width : 4.378
Height : 10.045
Entry
ampl
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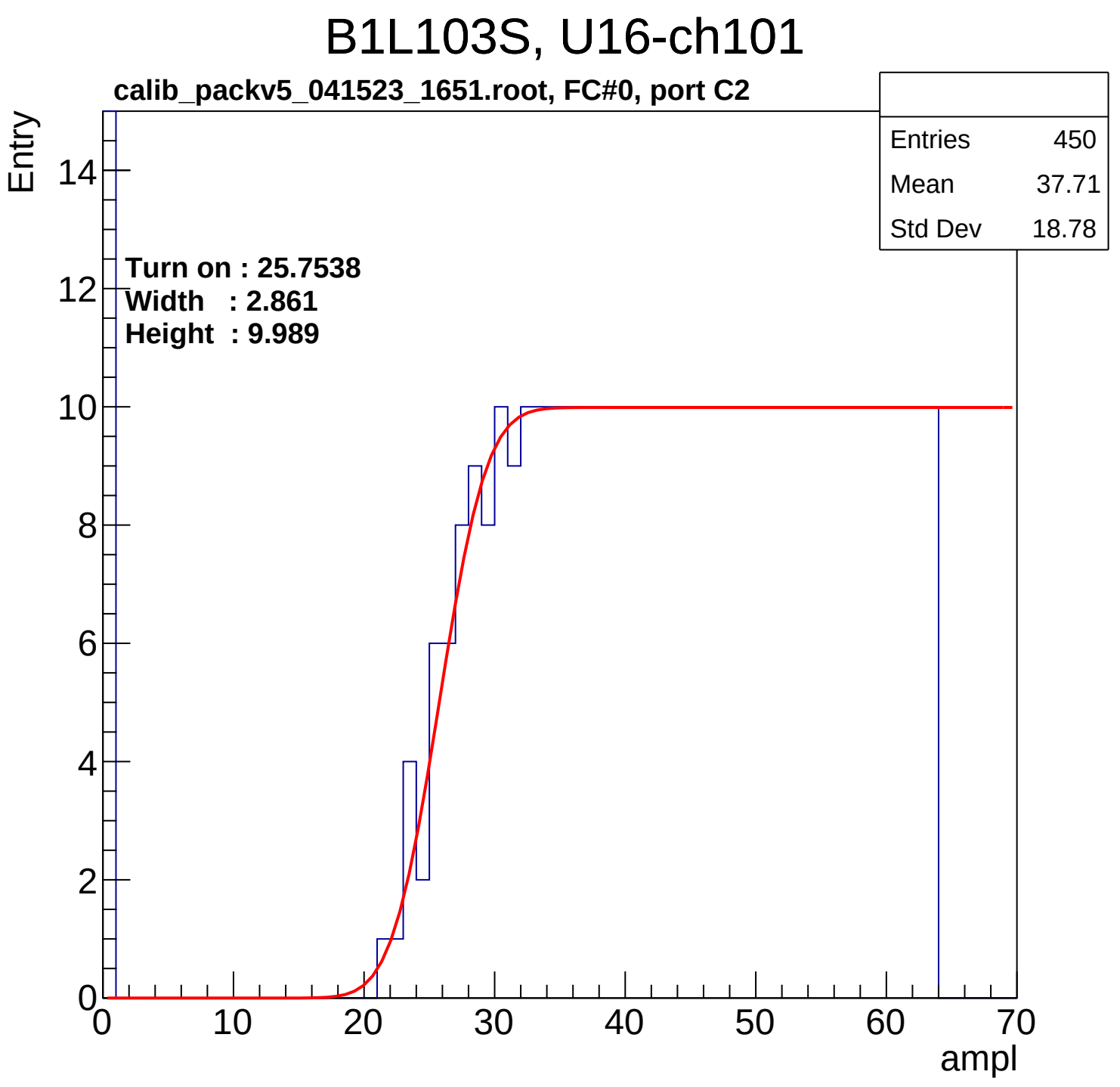
B1L103S, U16-ch101
calib_packv5_041523_1651.root, FC#0, port C2
Entries 450
Mean 37.71
Std Dev 18.78
Turn on : 25.7538
Width : 2.861
Height : 9.989
Entry
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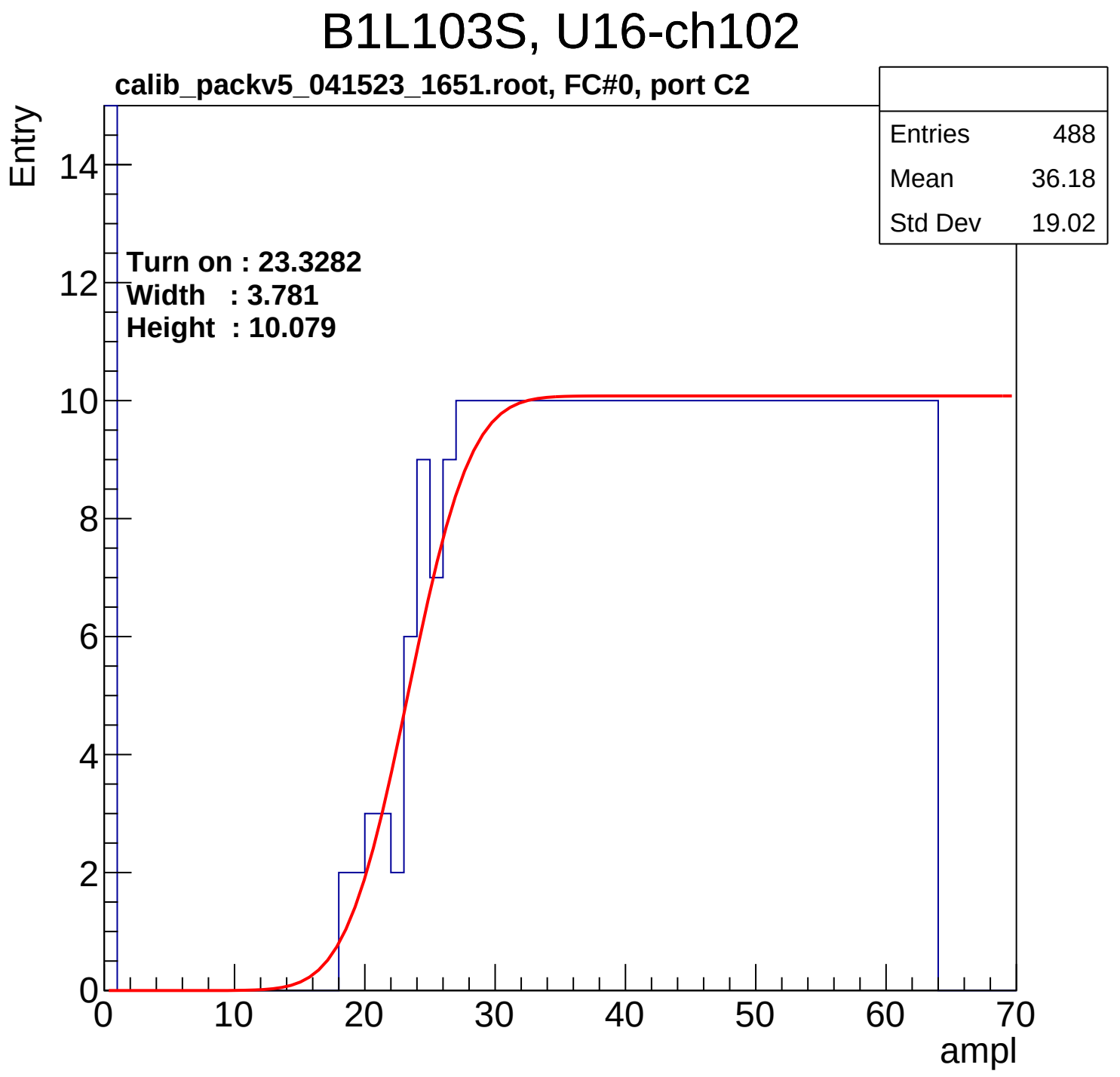
B1L103S, U16-ch102
calib_packv5_041523_1651.root, FC#0, port C2
Entries 488
Mean 36.18
Std Dev 19.02
Turn on : 23.3282
Width : 3.781
Height : 10.079
Entry
ampl
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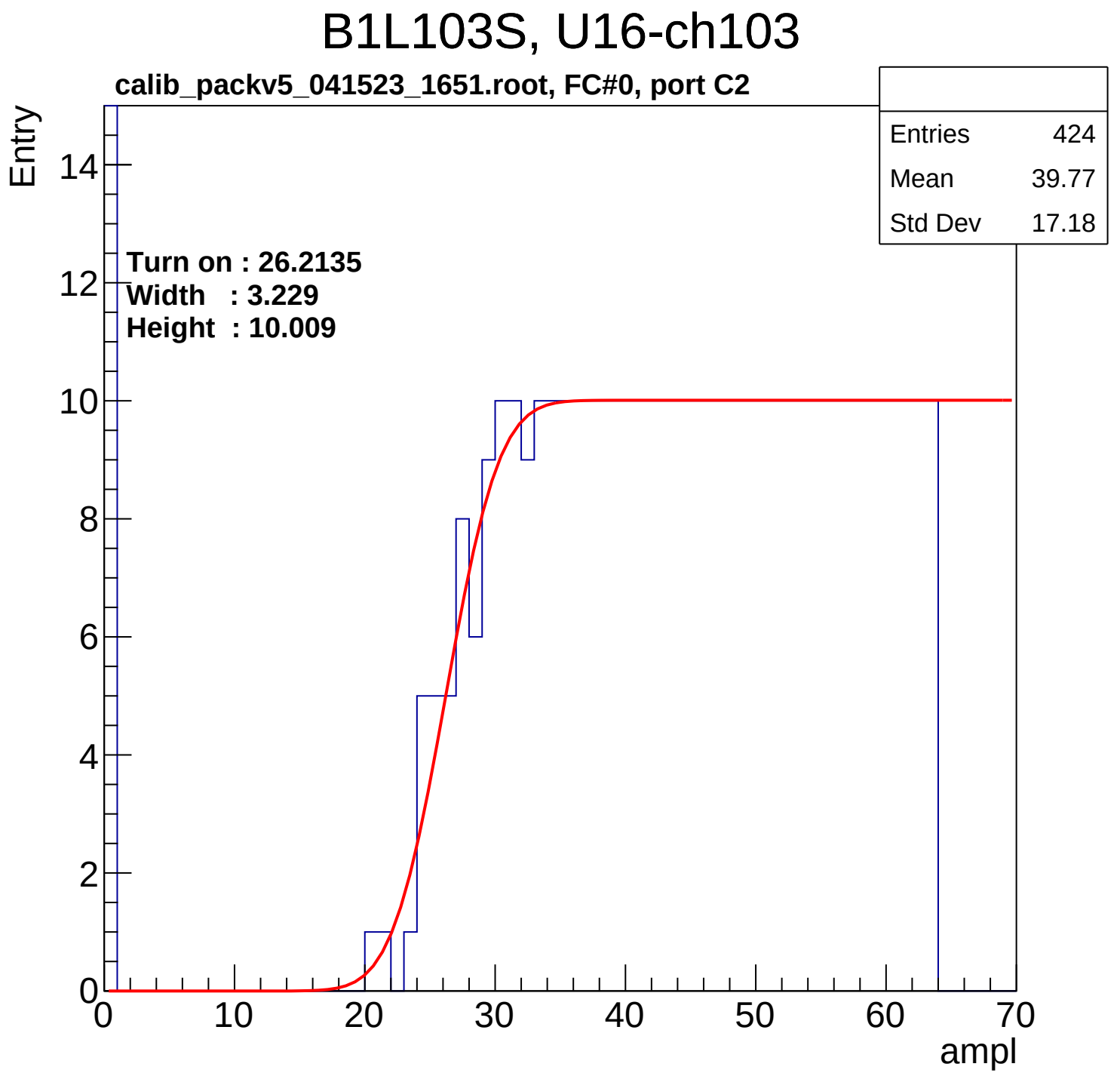
B1L103S, U16-ch103
calib_packv5_041523_1651.root, FC#0, port C2
Entries 424
Mean 39.77
Std Dev 17.18
Turn on : 26.2135
Width : 3.229
Height : 10.009
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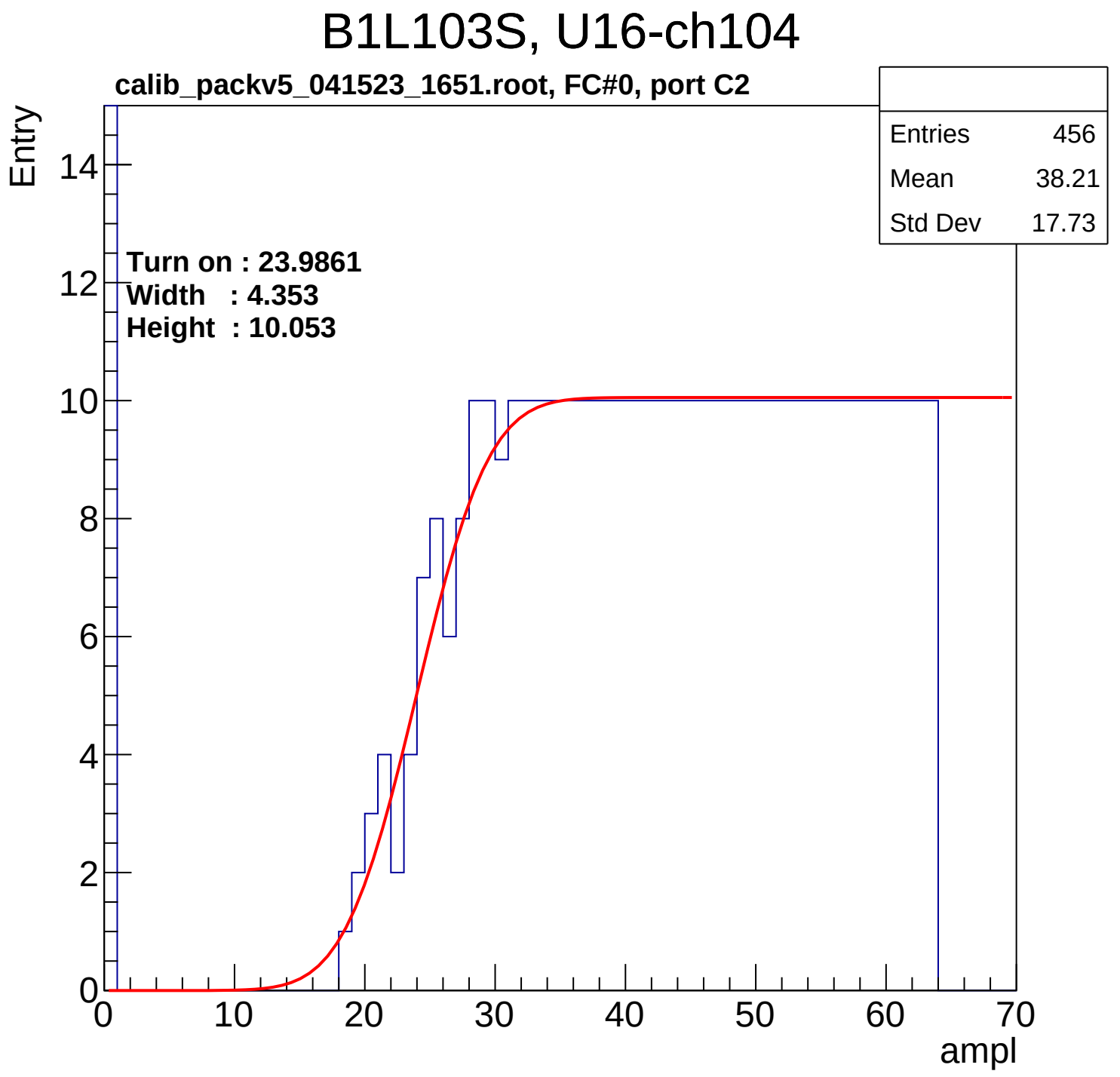
B1L103S, U16-ch104
calib_packv5_041523_1651.root, FC#0, port C2
Entries 456
Mean 38.21
Std Dev 17.73
Turn on : 23.9861
Width : 4.353
Height : 10.053
Entry
ampl
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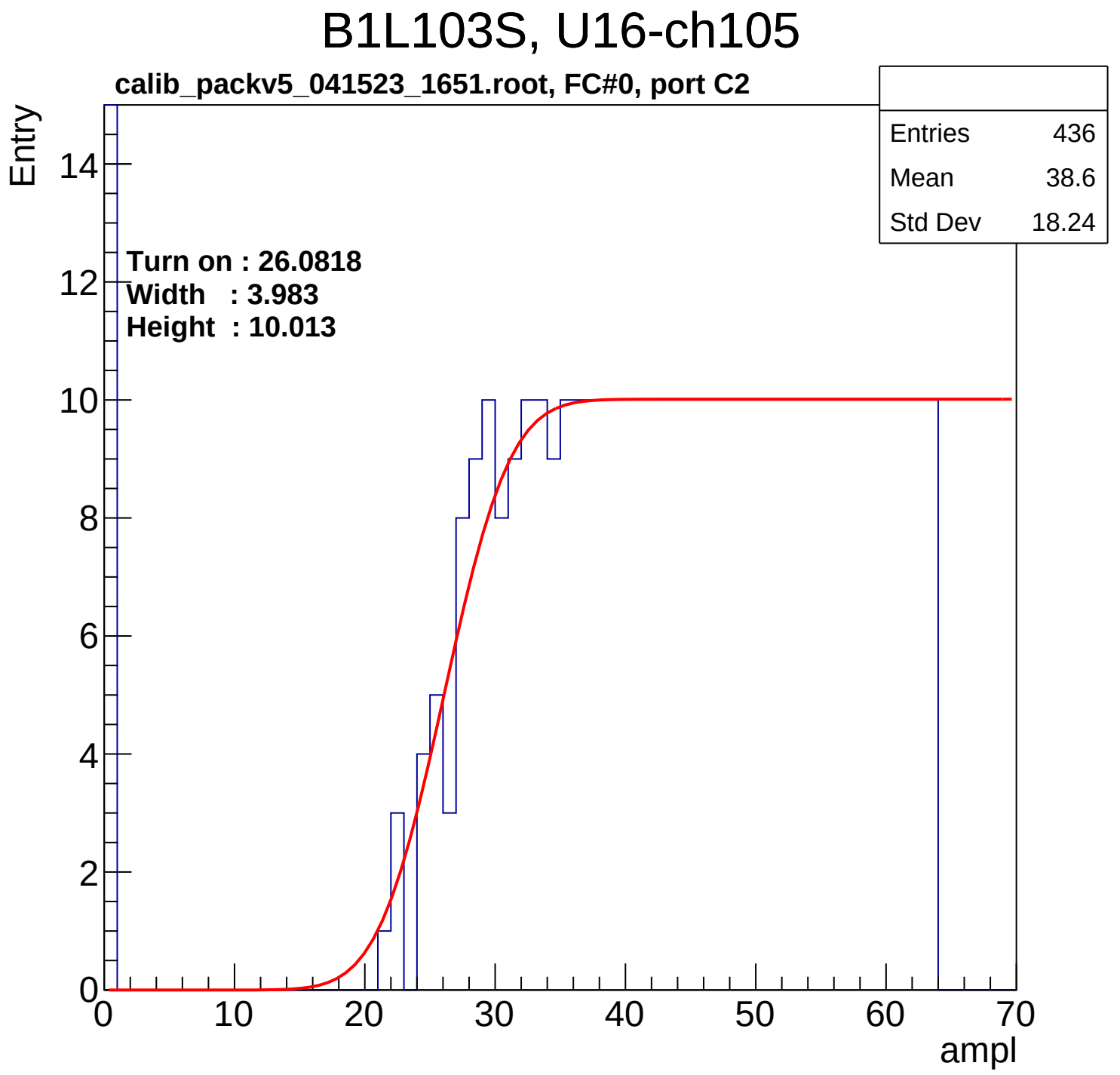
B1L103S, U16-ch105
calib_packv5_041523_1651.root, FC#0, port C2
Entries 436
Mean 38.6
Std Dev 18.24
Turn on : 26.0818
Width : 3.983
Height : 10.013
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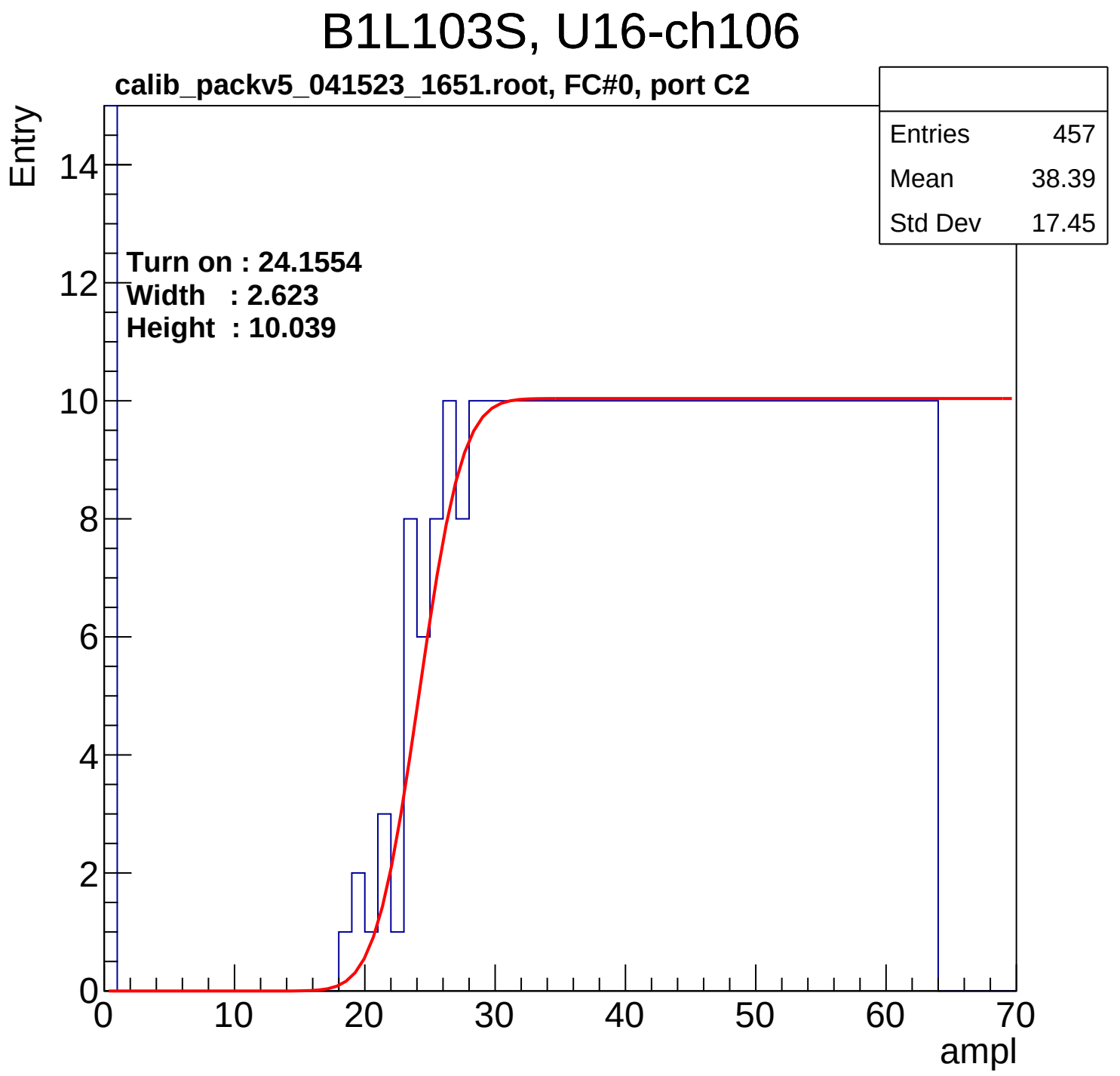
B1L103S, U16-ch106
calib_packv5_041523_1651.root, FC#0, port C2
Entries 457
Mean 38.39
Std Dev 17.45
Turn on : 24.1554
Width : 2.623
Height : 10.039
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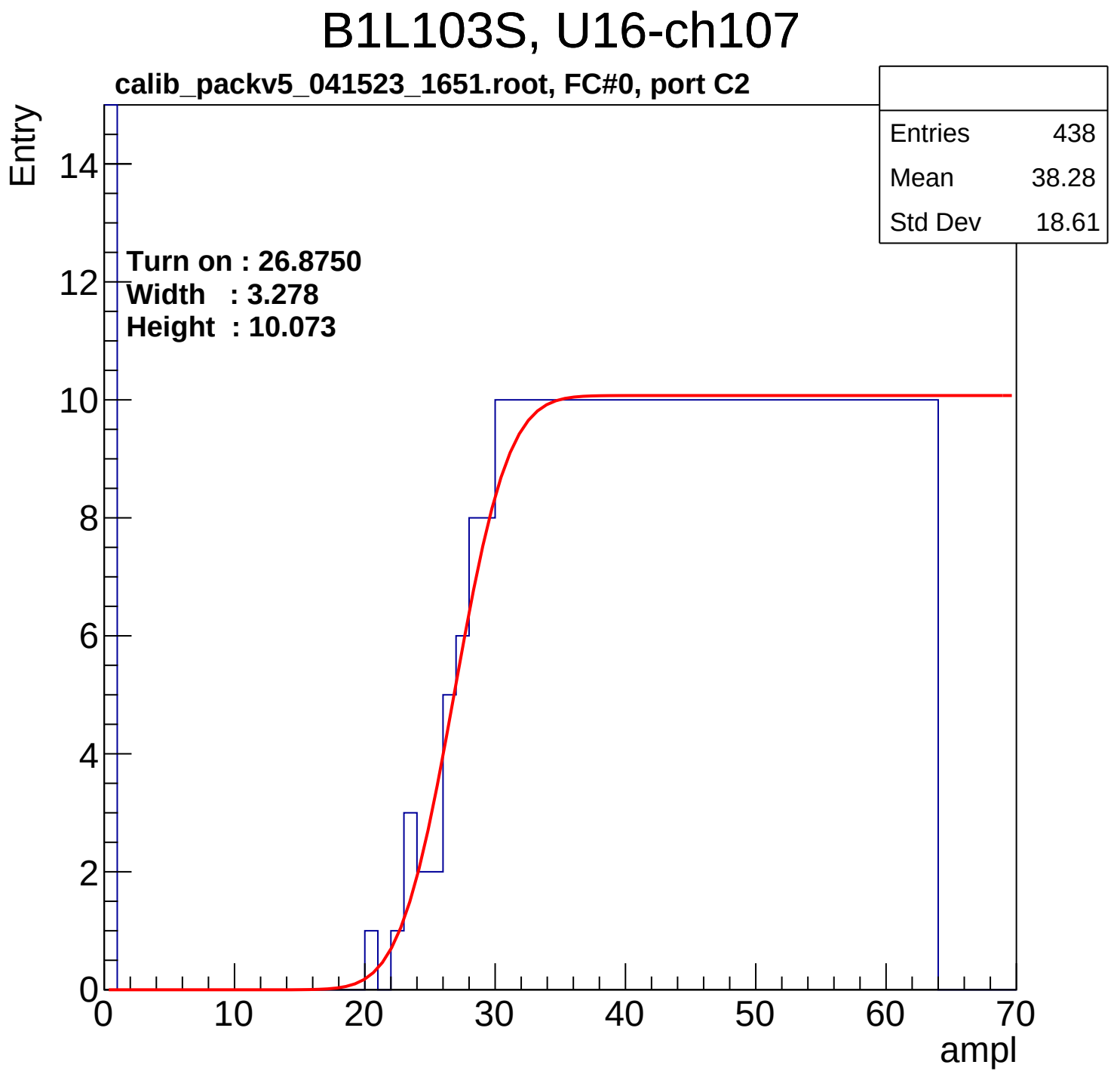
B1L103S, U16-ch107
calib_packv5_041523_1651.root, FC#0, port C2
Entries 438
Mean 38.28
Std Dev 18.61
Turn on : 26.8750
Width : 3.278
Height : 10.073
Entry
ampl
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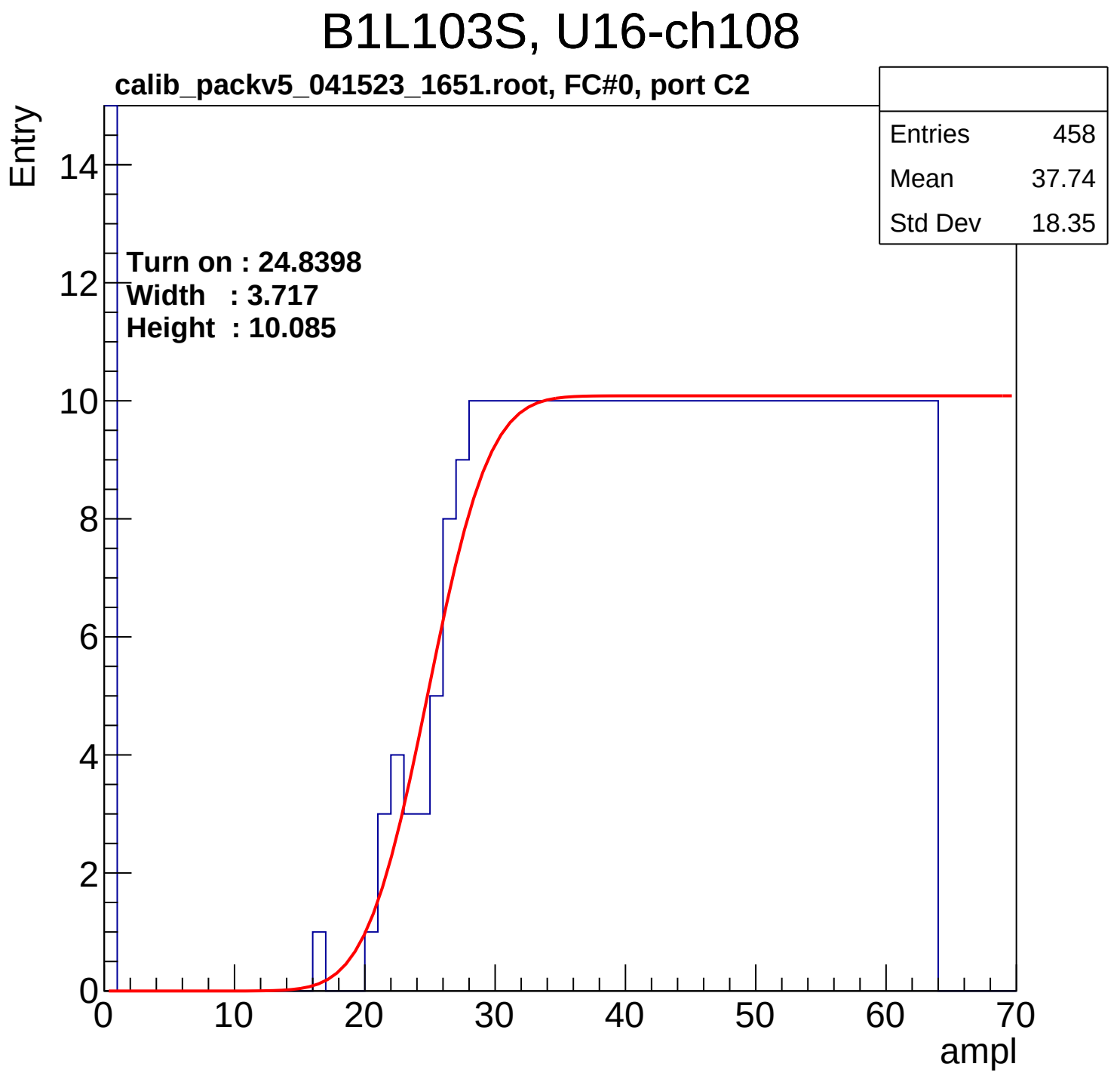
B1L103S, U16-ch108
calib_packv5_041523_1651.root, FC#0, port C2
Entries 458
Mean 37.74
Std Dev 18.35
Turn on : 24.8398
Width : 3.717
Height : 10.085
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ampl
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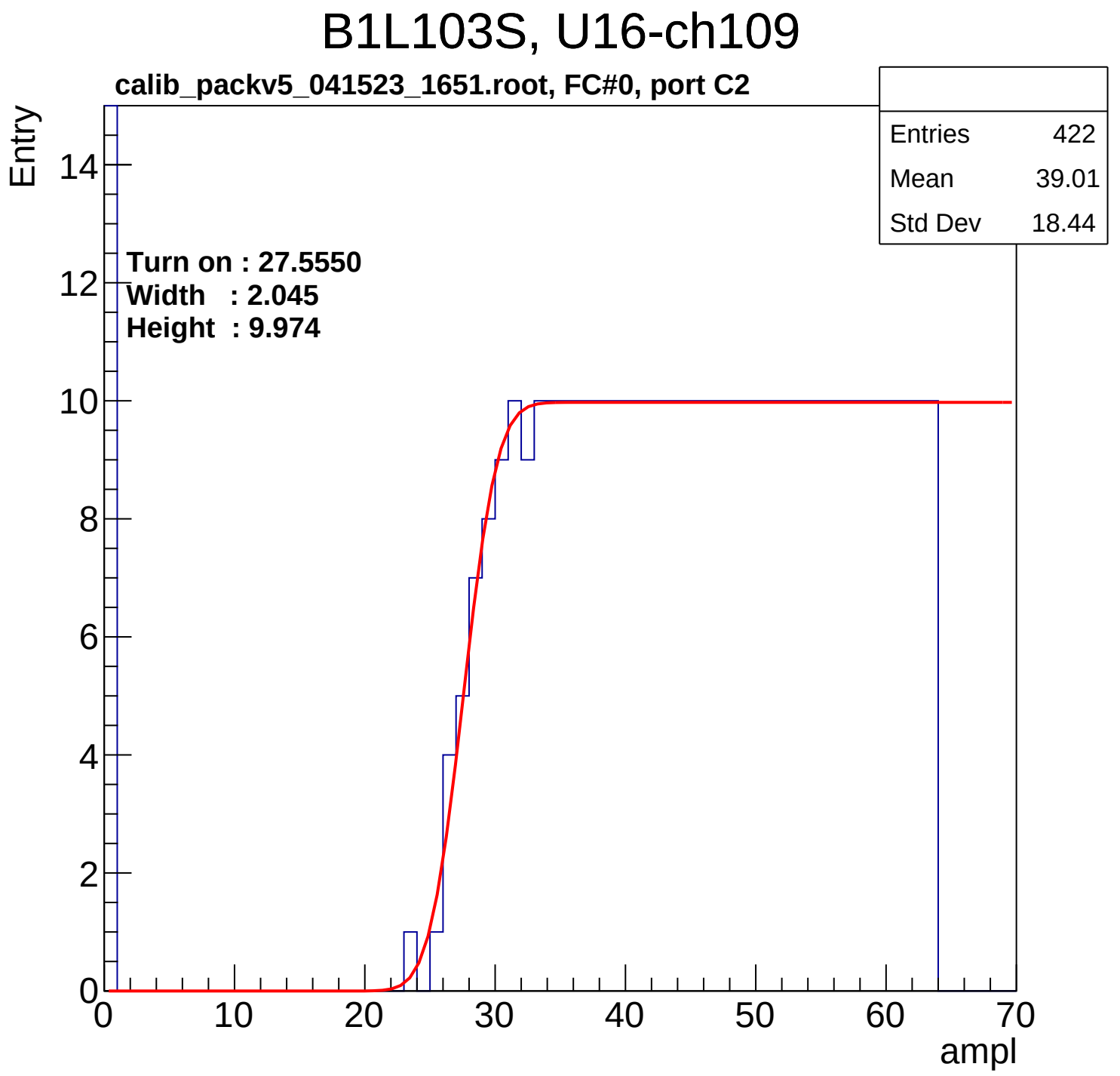
B1L103S, U16-ch109
calib_packv5_041523_1651.root, FC#0, port C2
Entries 422
Mean 39.01
Std Dev 18.44
Turn on : 27.5550
Width : 2.045
Height : 9.974
Entry
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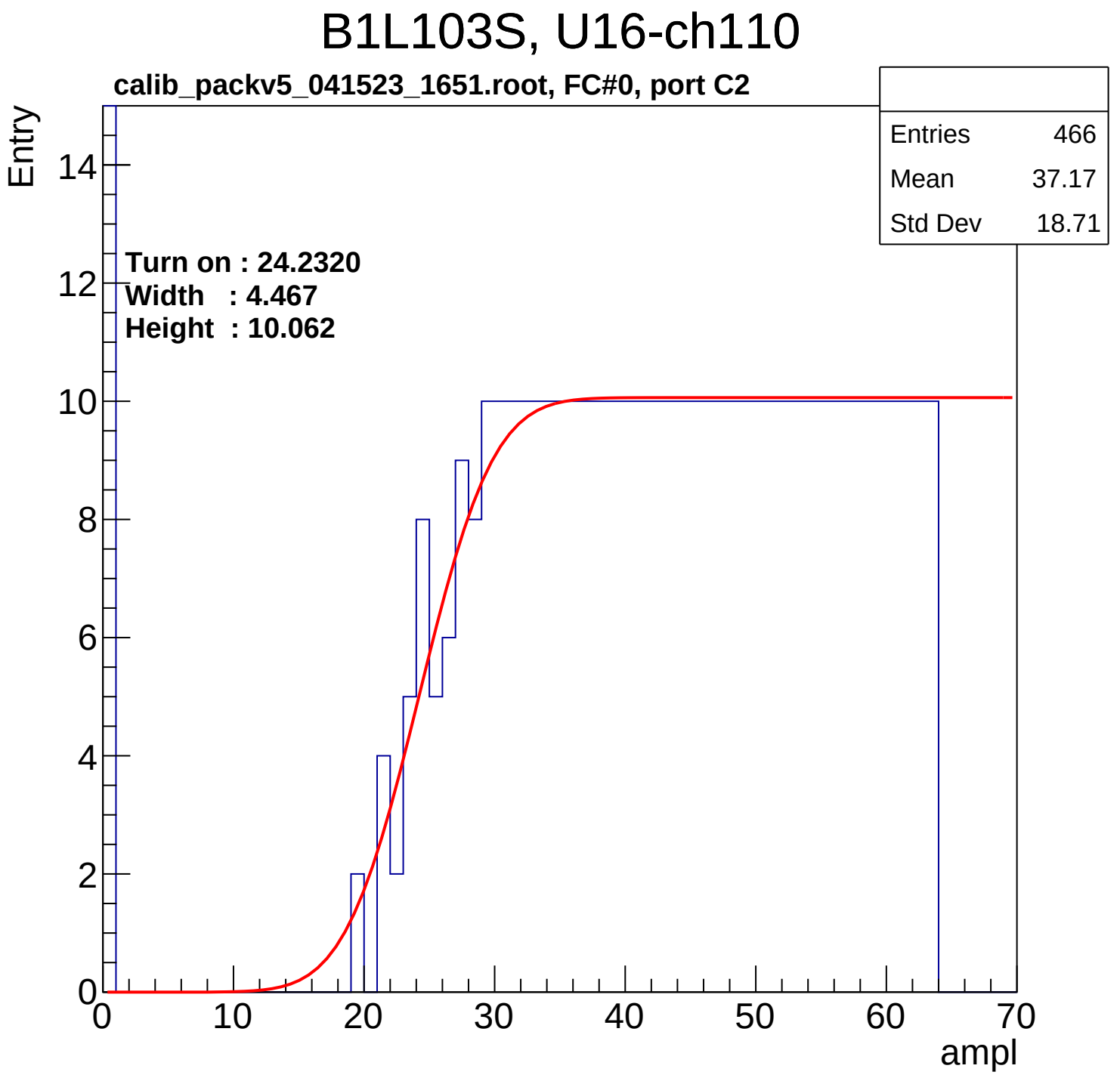
B1L103S, U16-ch110
calib_packv5_041523_1651.root, FC#0, port C2
Entries 466
Mean 37.17
Std Dev 18.71
Turn on : 24.2320
Width : 4.467
Height : 10.062
Entry
ampl
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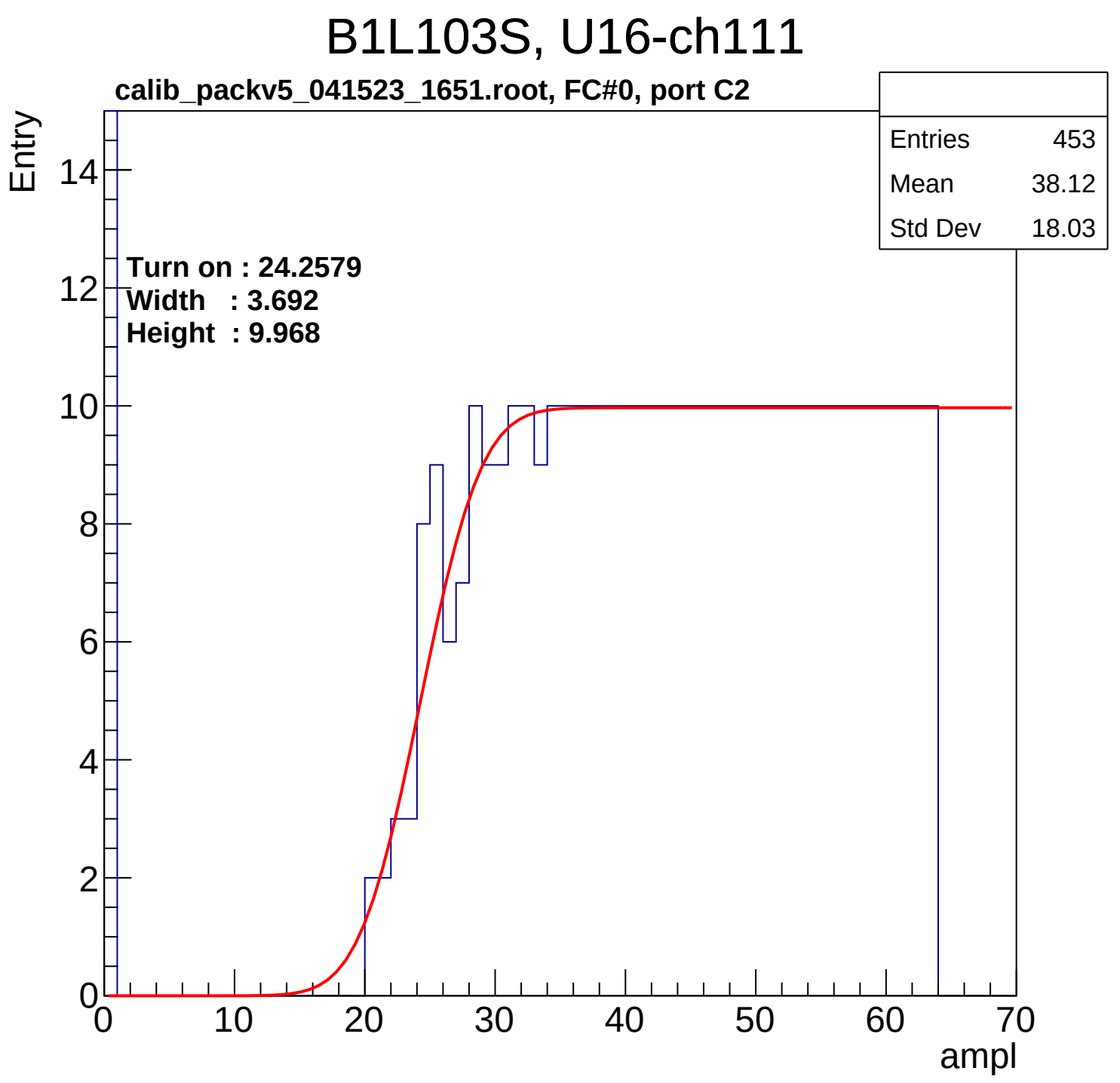
B1L103S, U16-ch111
calib_packv5_041523_1651.root, FC#0, port C2
Entries 453
Mean 38.12
Std Dev 18.03
Turn on : 24.2579
Width : 3.692
Height : 9.968
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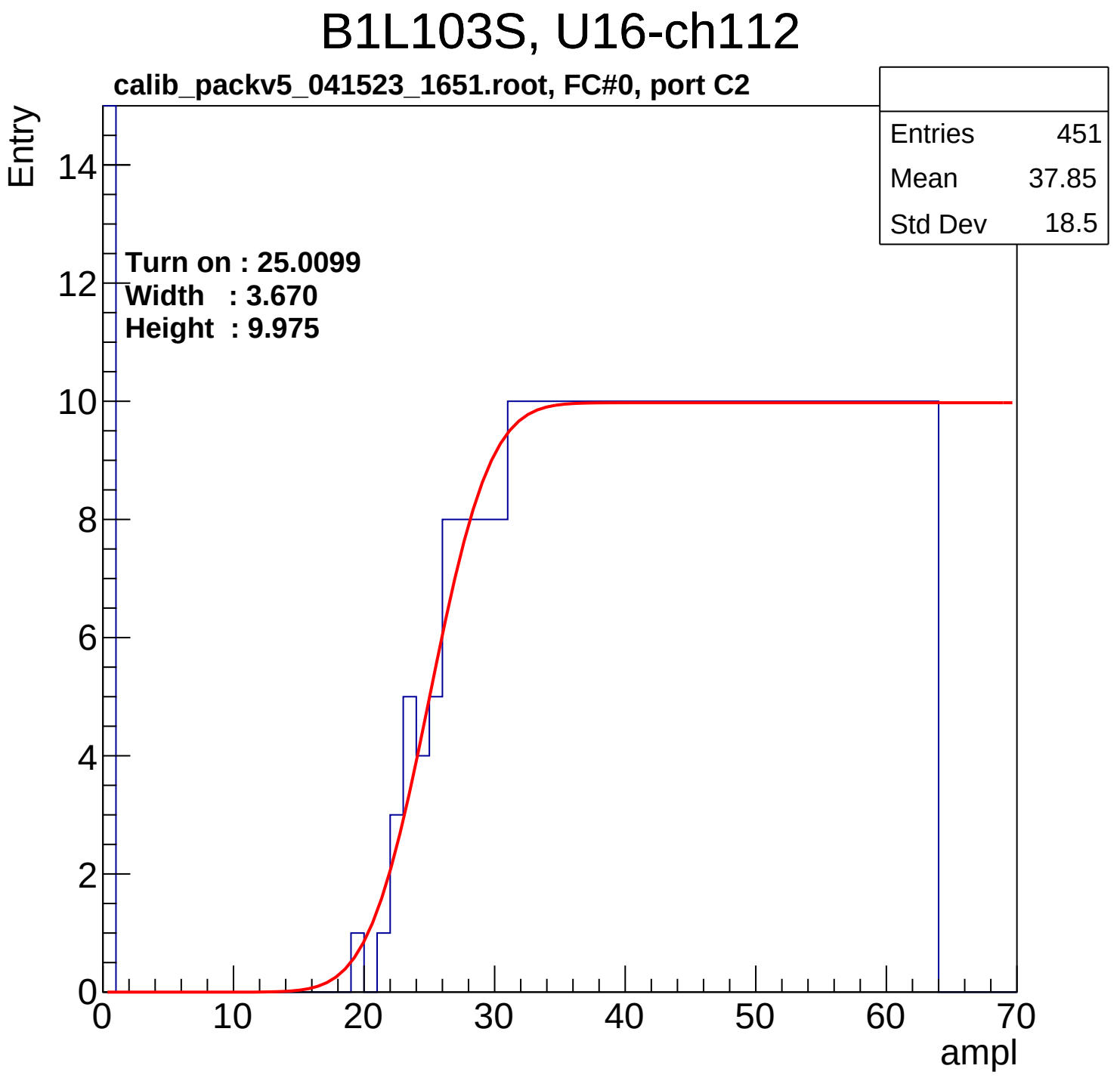
B1L103S, U16-ch112
calib_packv5_041523_1651.root, FC#0, port C2
Entries 451
Mean 37.85
Std Dev 18.5
Turn on : 25.0099
Width : 3.670
Height : 9.975
Entry
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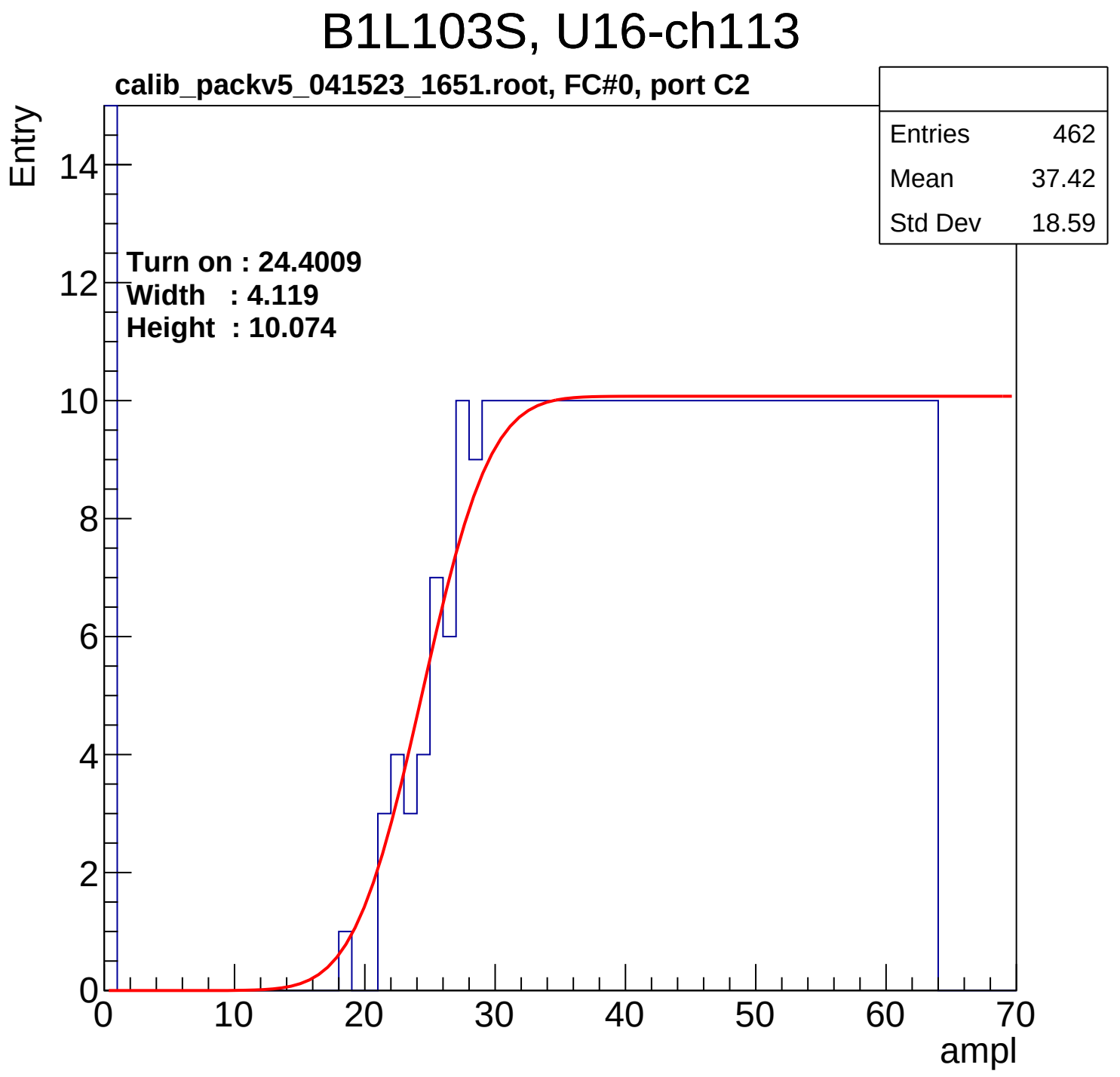
B1L103S, U16-ch113
calib_packv5_041523_1651.root, FC#0, port C2
Entries 462
Mean 37.42
Std Dev 18.59
Turn on : 24.4009
Width : 4.119
Height : 10.074
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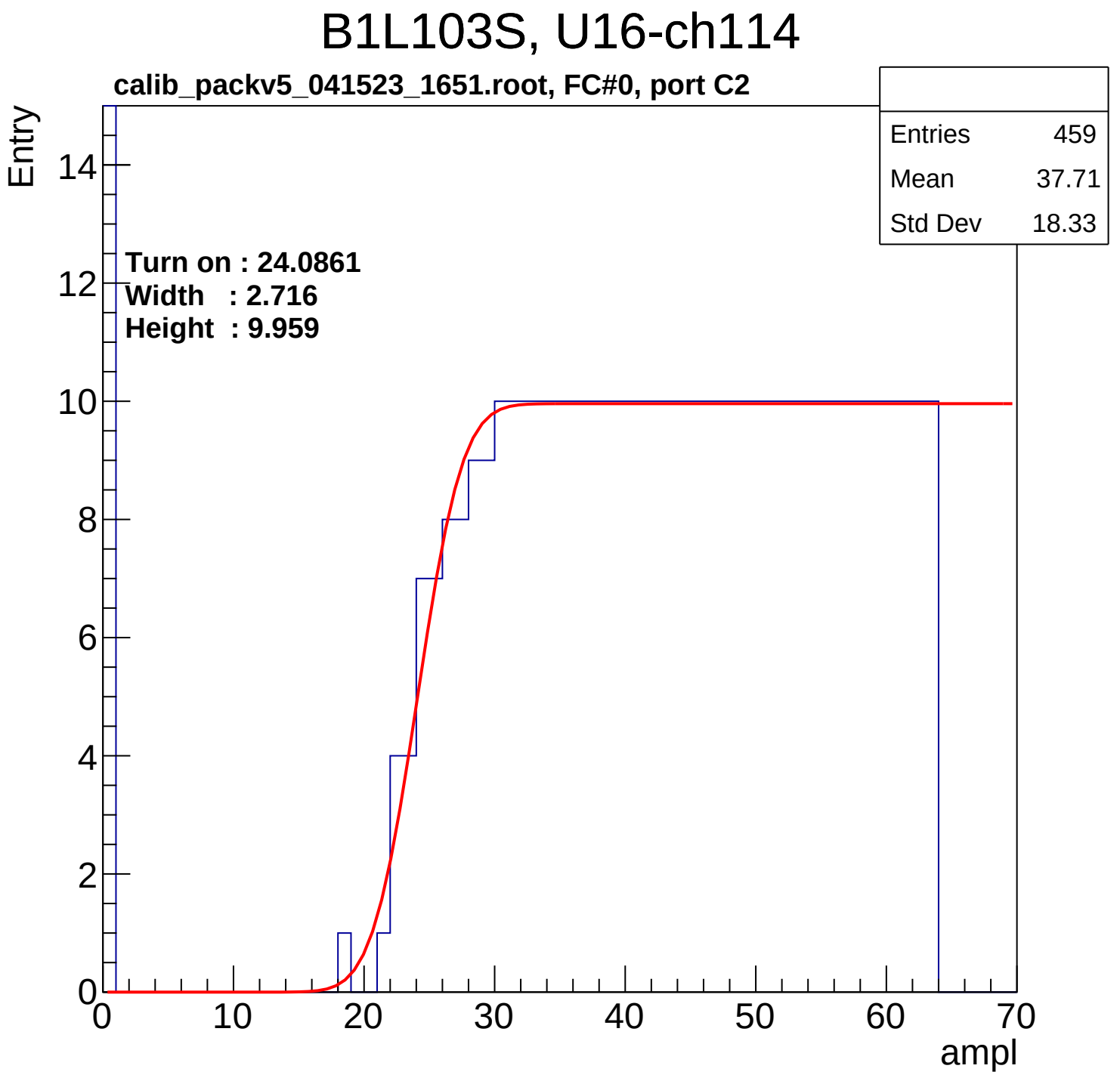
B1L103S, U16-ch114
calib_packv5_041523_1651.root, FC#0, port C2
Entries 459
Mean 37.71
Std Dev 18.33
Turn on : 24.0861
Width : 2.716
Height : 9.959
Entry
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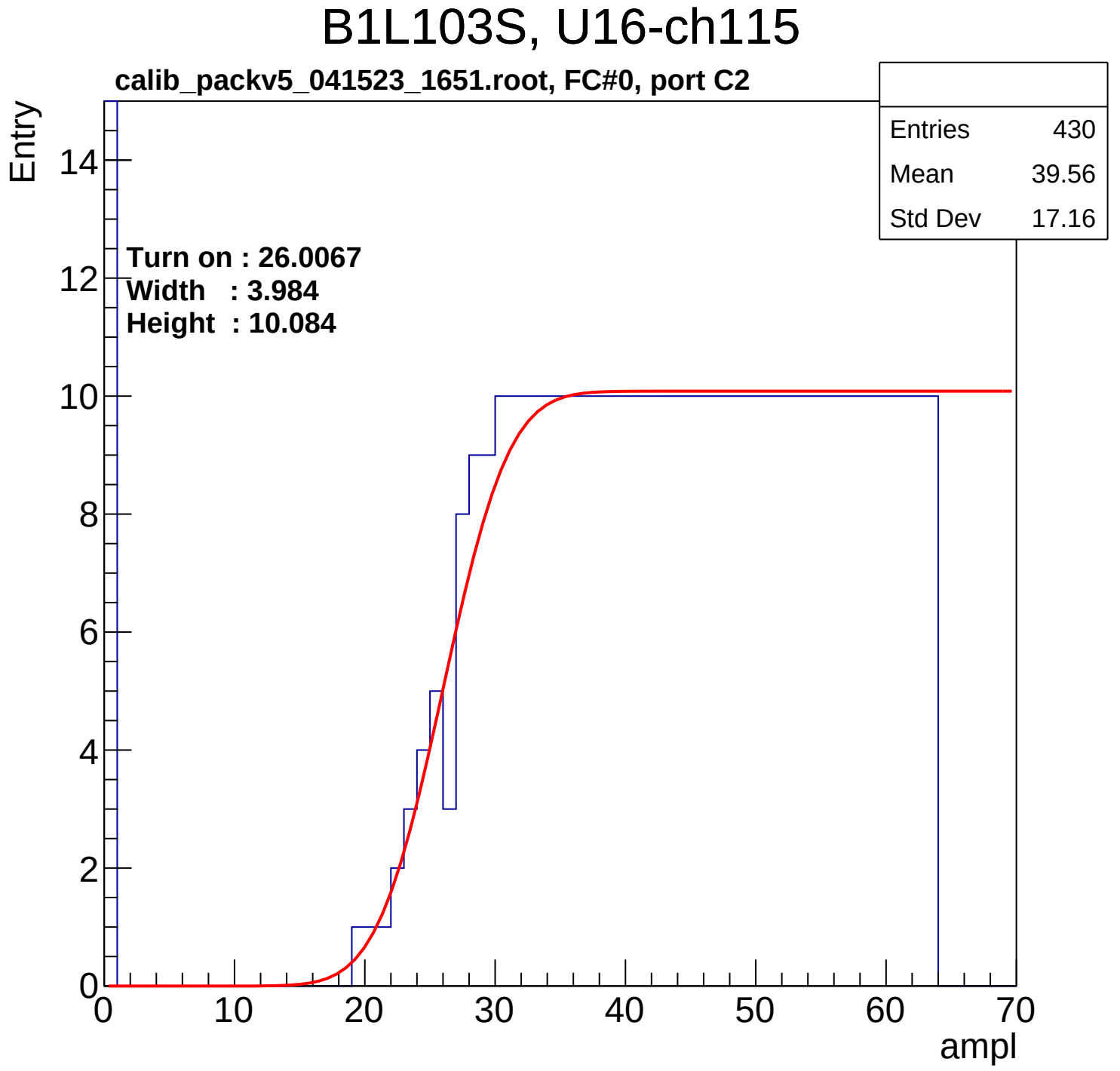
B1L103S, U16-ch115
calib_packv5_041523_1651.root, FC#0, port C2
Entries 430
Mean 39.56
Std Dev 17.16
Turn on : 26.0067
Width : 3.984
Height : 10.084
Entry
ampl
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4
6
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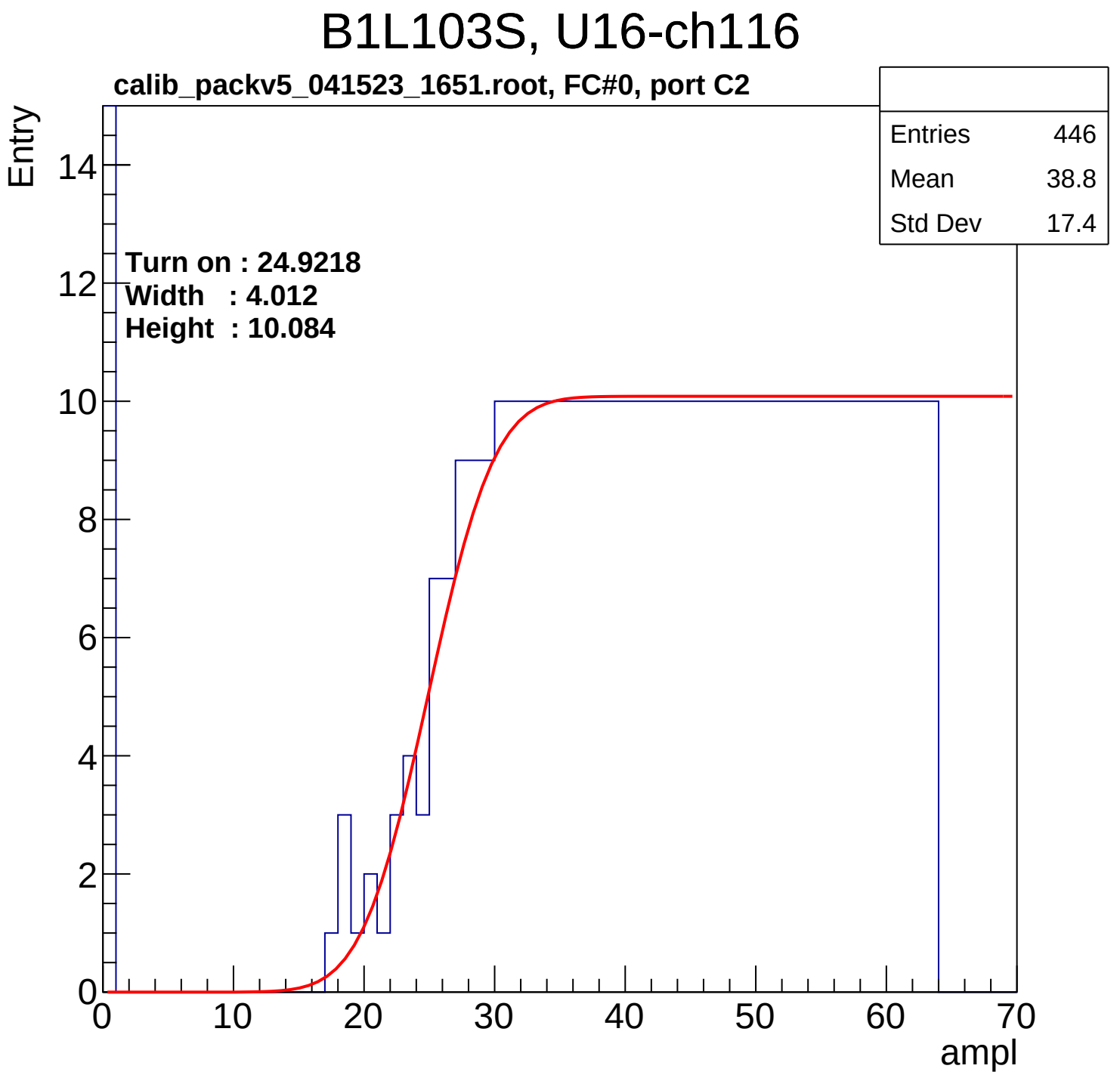
B1L103S, U16-ch116
calib_packv5_041523_1651.root, FC#0, port C2
Entries 446
Mean 38.8
Std Dev 17.4
Turn on : 24.9218
Width : 4.012
Height : 10.084
Entry
ampl
0
2
4
6
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10
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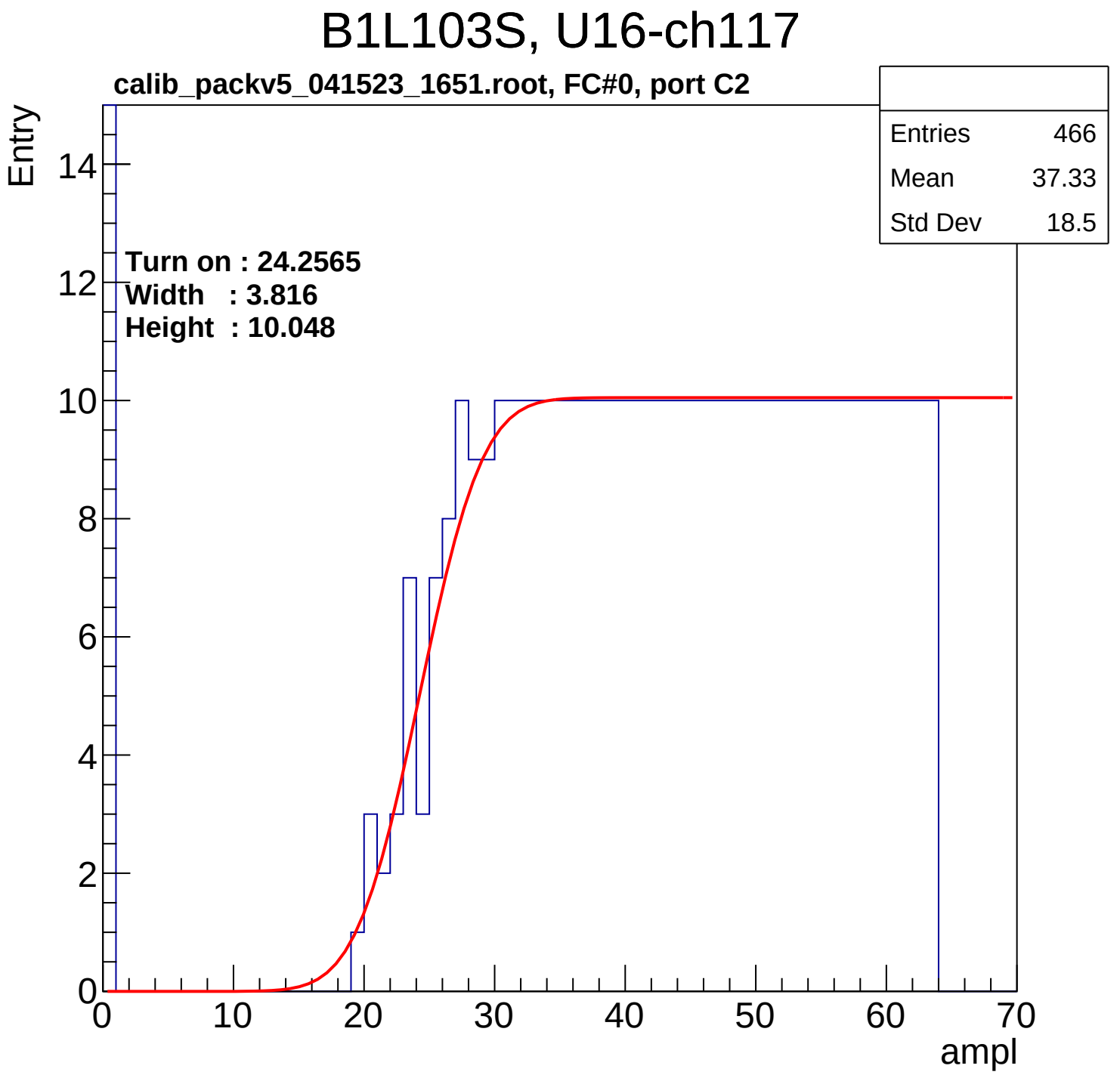
B1L103S, U16-ch117
calib_packv5_041523_1651.root, FC#0, port C2
Entries 466
Mean 37.33
Std Dev 18.5
Turn on : 24.2565
Width : 3.816
Height : 10.048
Entry
ampl
0
2
4
6
8
10
12
14
0
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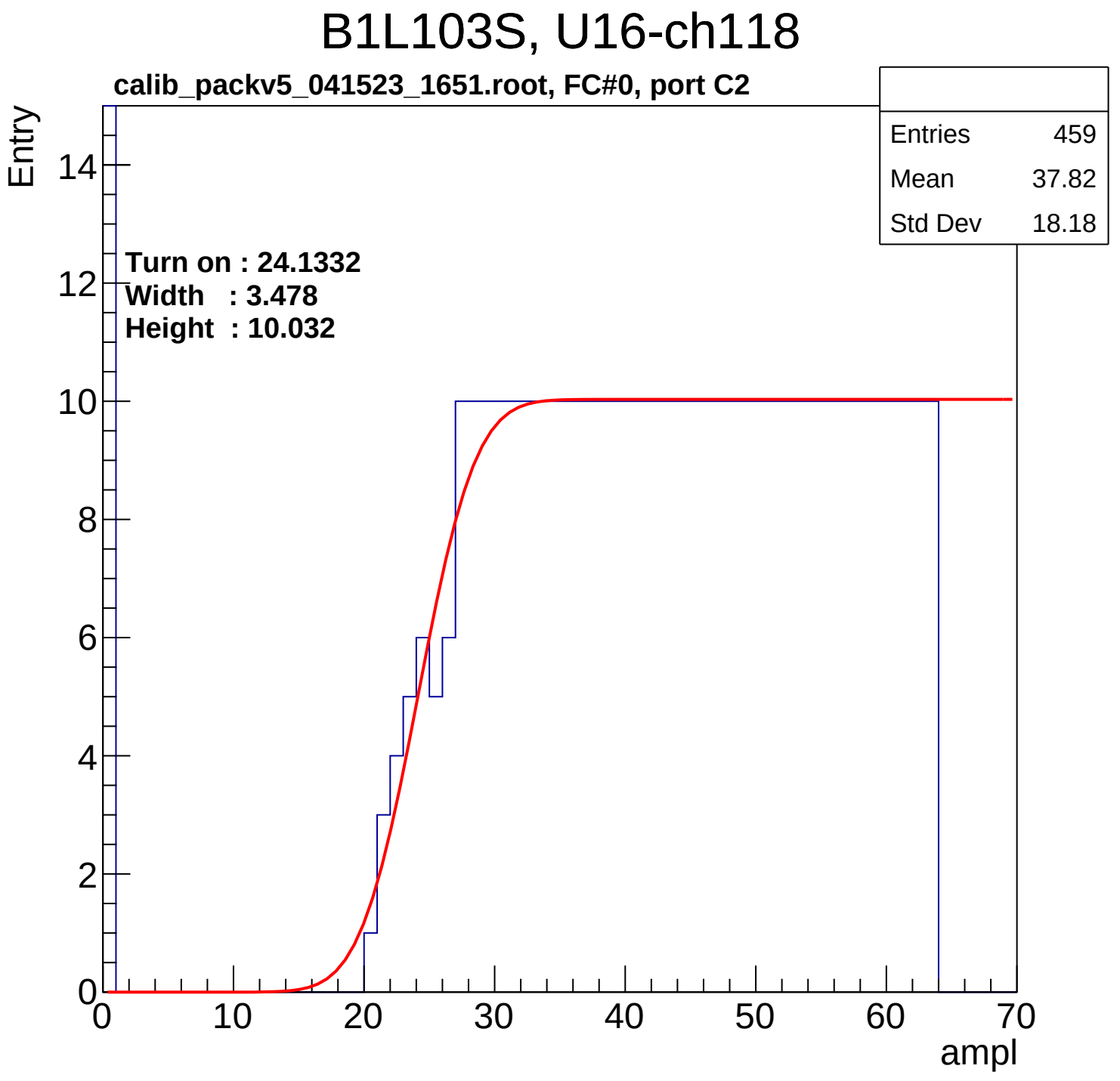
B1L103S, U16-ch118
calib_packv5_041523_1651.root, FC#0, port C2
Entries 459
Mean 37.82
Std Dev 18.18
Turn on : 24.1332
Width : 3.478
Height : 10.032
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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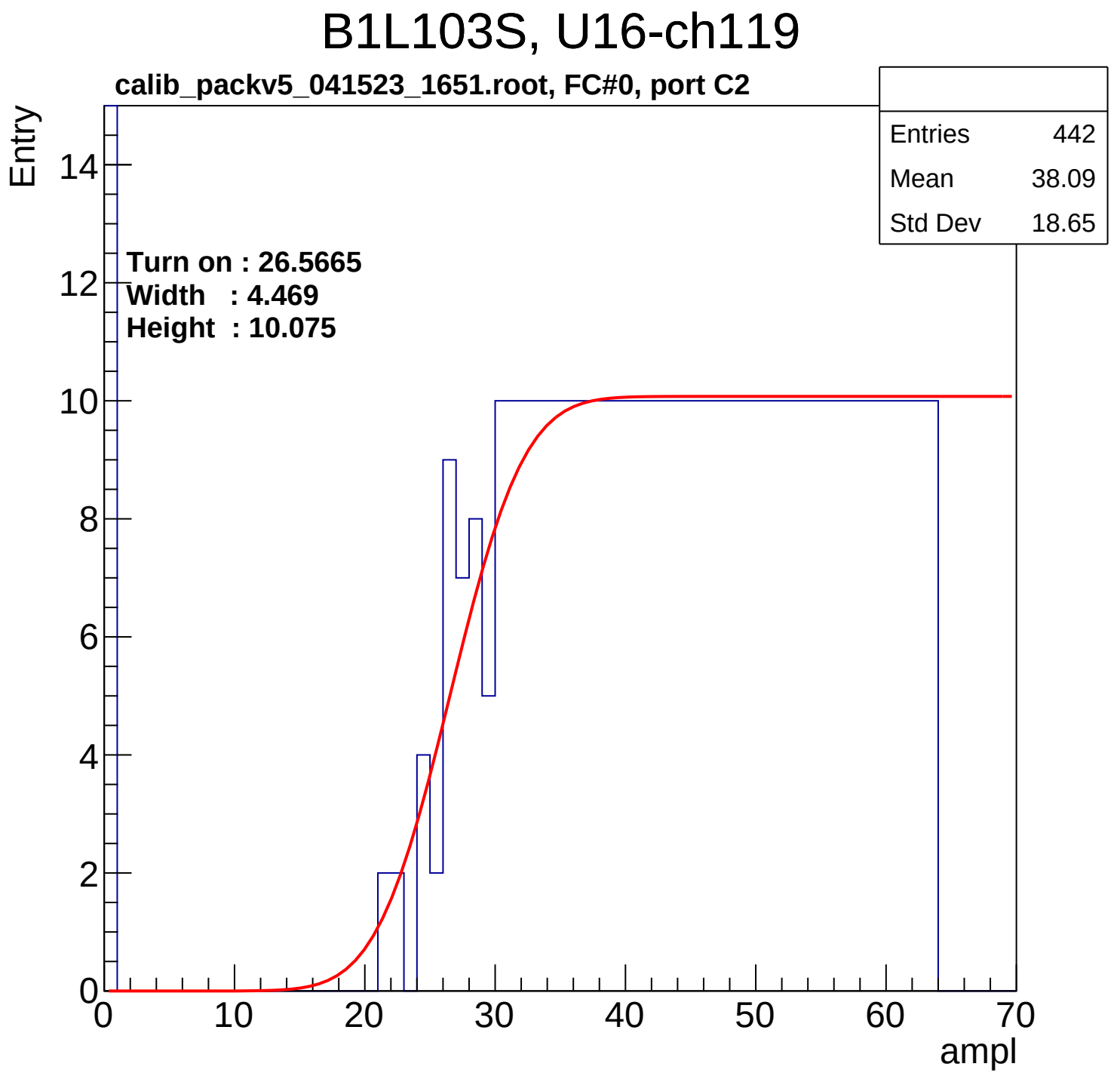
B1L103S, U16-ch119
calib_packv5_041523_1651.root, FC#0, port C2
Entries 442
Mean 38.09
Std Dev 18.65
Turn on : 26.5665
Width : 4.469
Height : 10.075
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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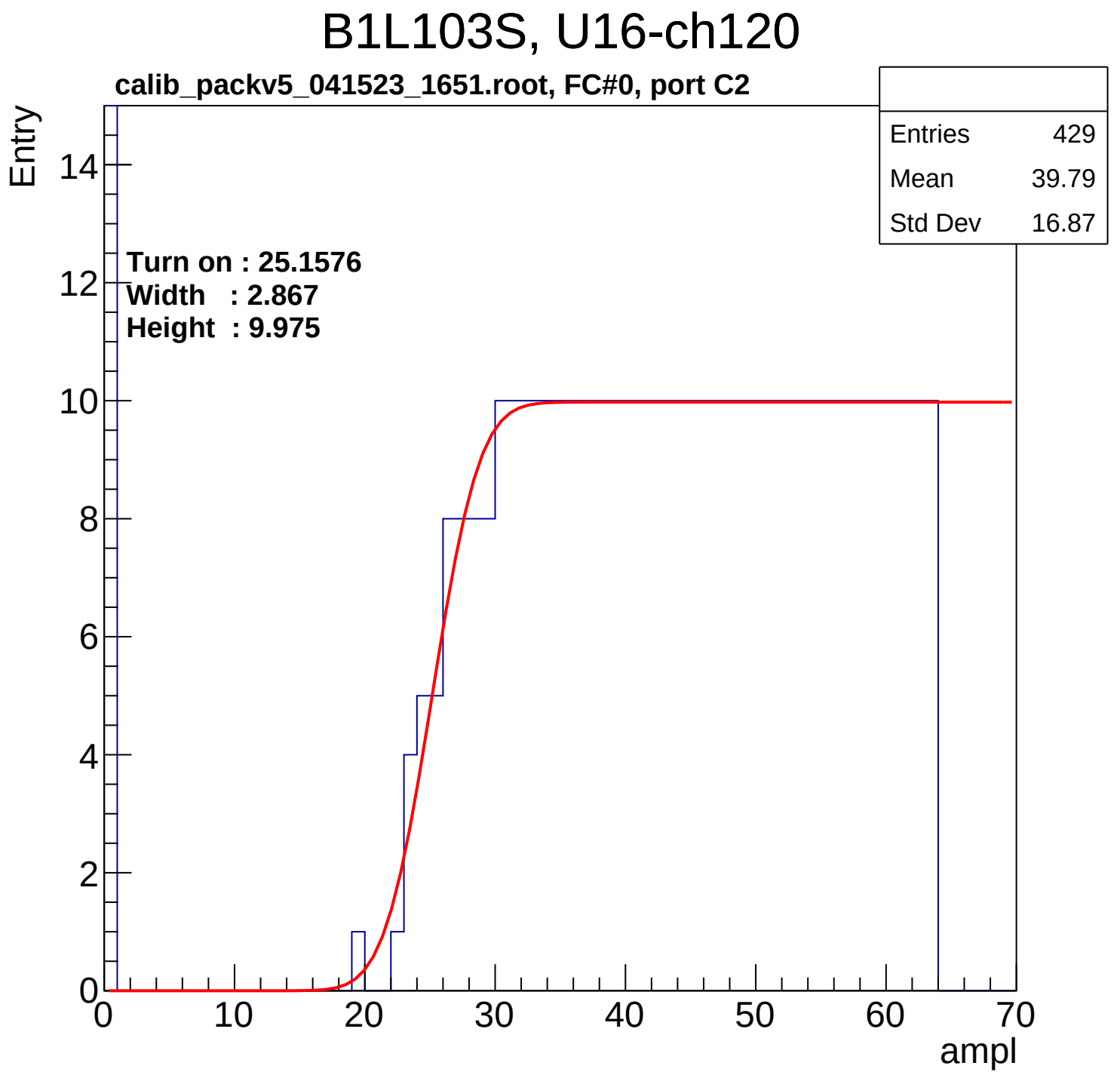
B1L103S, U16-ch120
calib_packv5_041523_1651.root, FC#0, port C2
Entries 429
Mean 39.79
Std Dev 16.87
Turn on : 25.1576
Width : 2.867
Height : 9.975
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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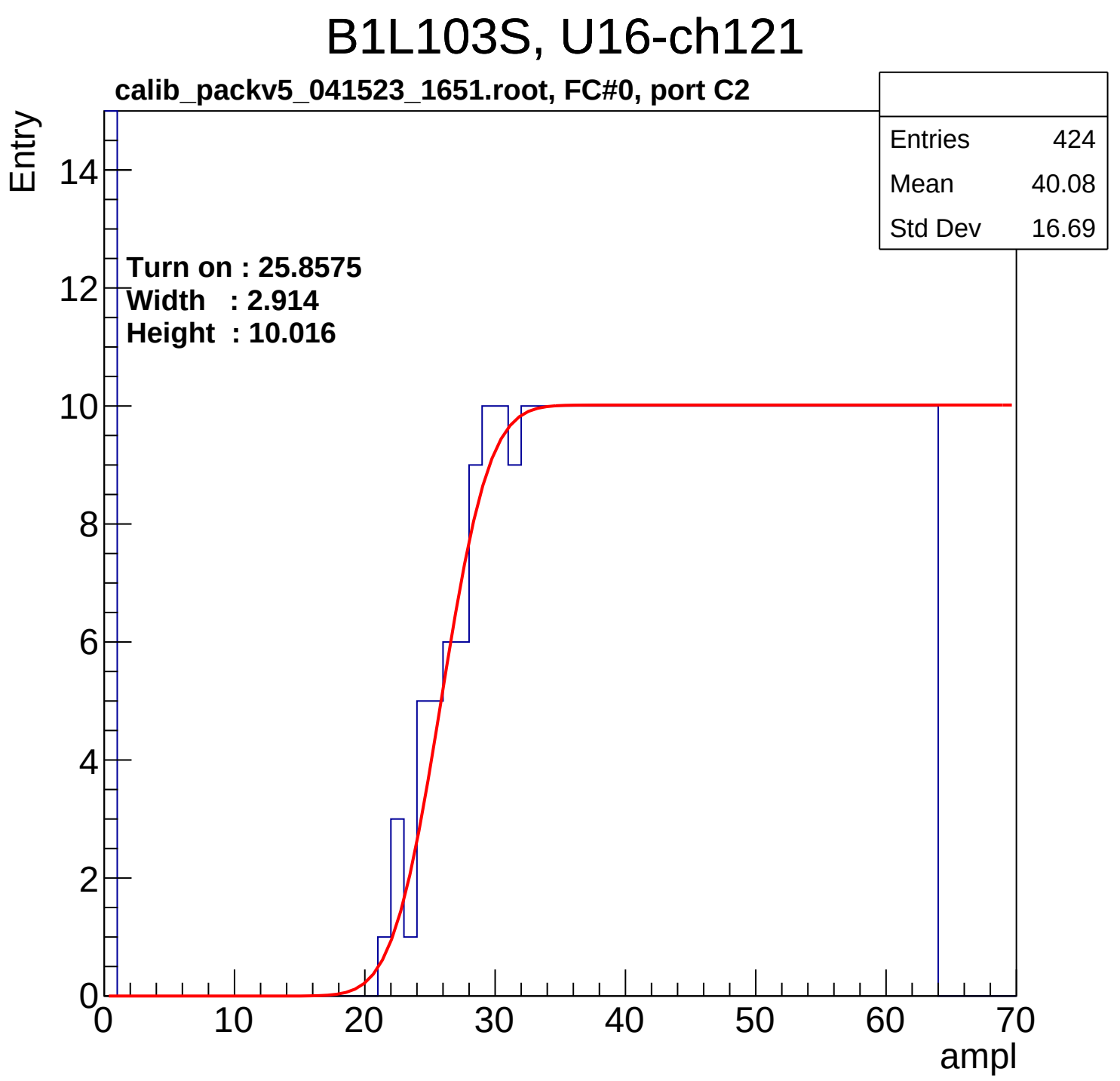
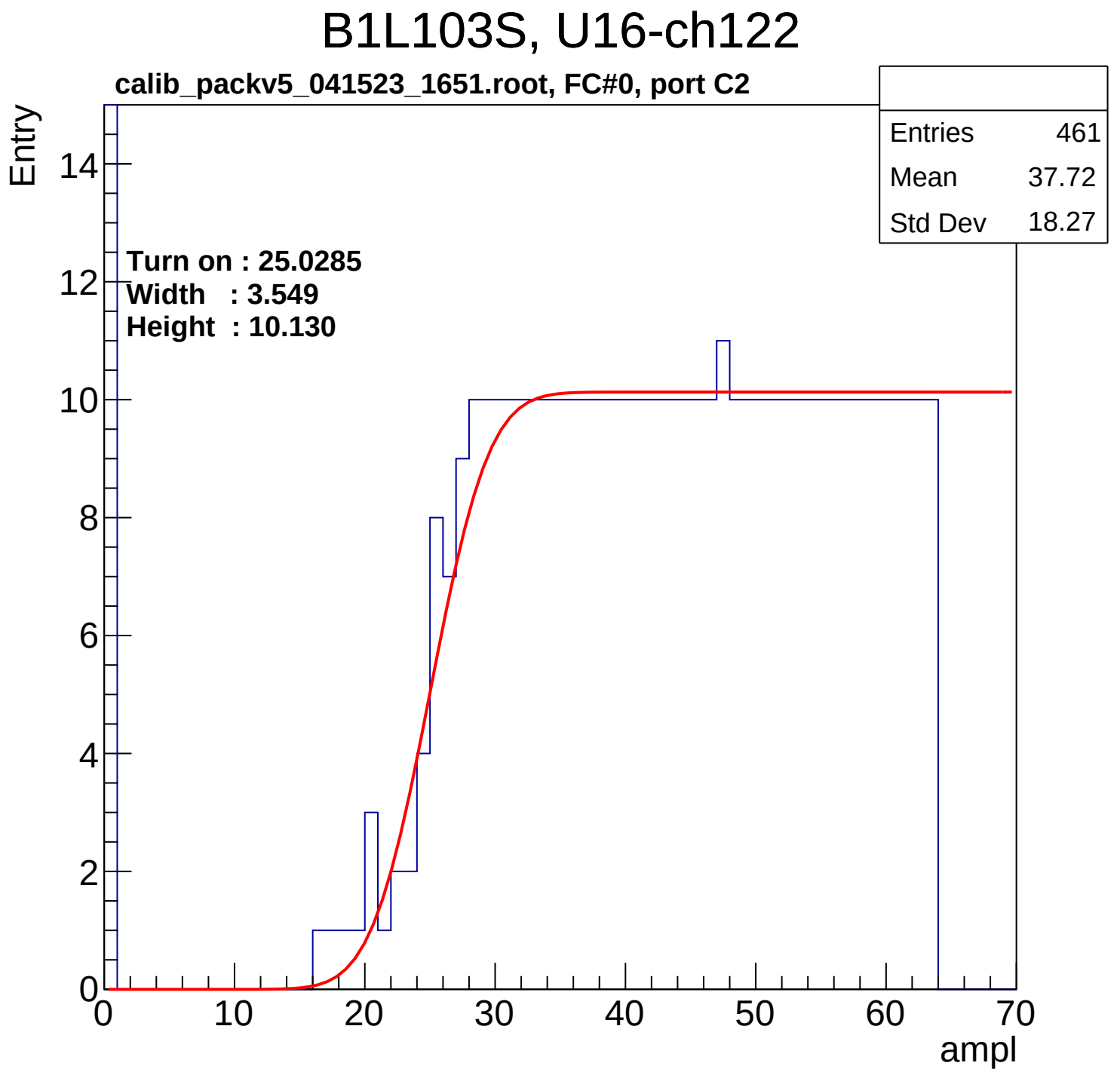

B1L103S, U16-ch121
calib_packv5_041523_1651.root, FC#0, port C2
Entries 424
Mean 40.08
Std Dev 16.69
Turn on : 25.8575
Width : 2.914
Height : 10.016
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U16-ch122
calib_packv5_041523_1651.root, FC#0, port C2
Entries 461
Mean 37.72
Std Dev 18.27
Turn on : 25.0285
Width : 3.549
Height : 10.130
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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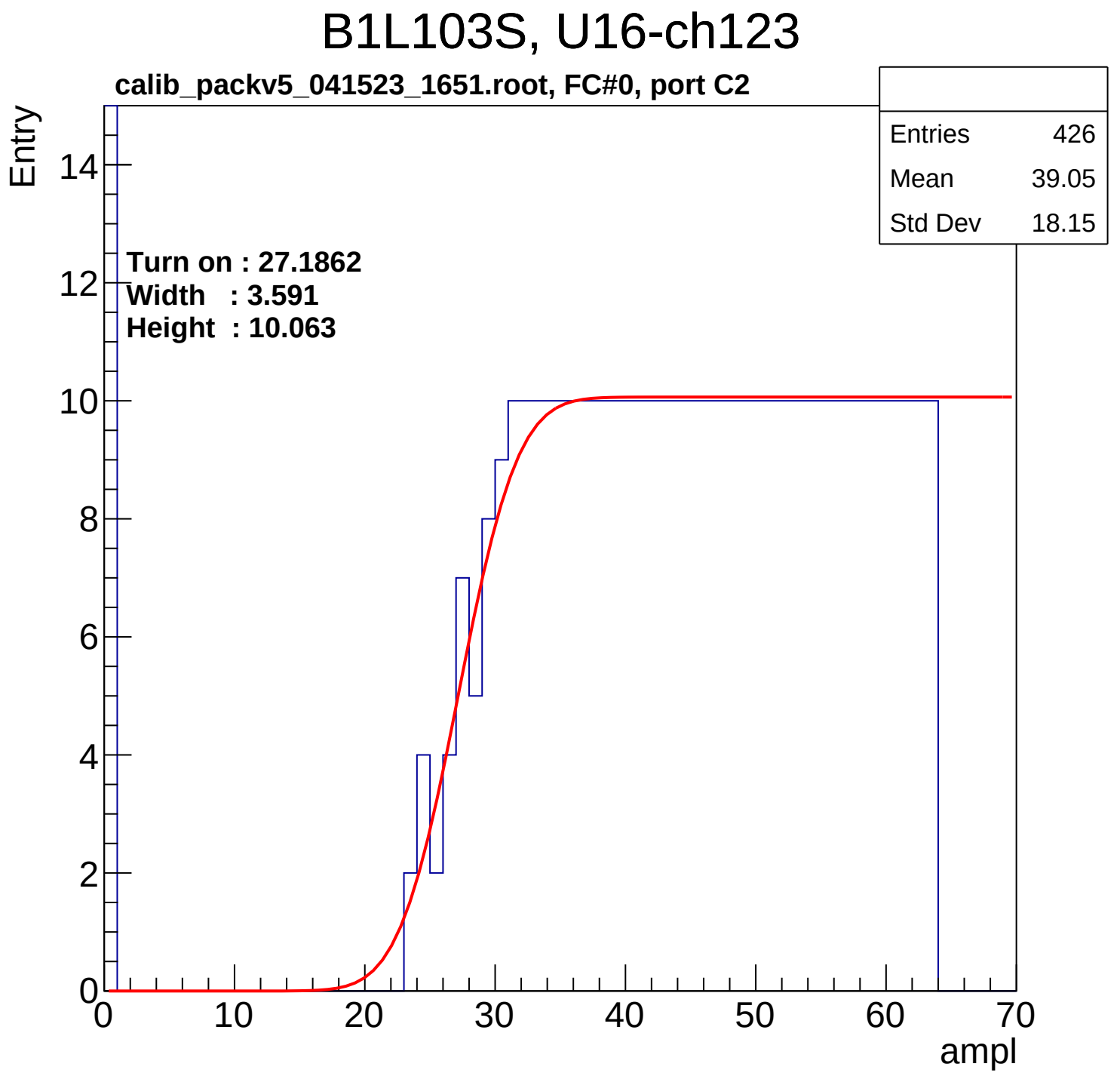
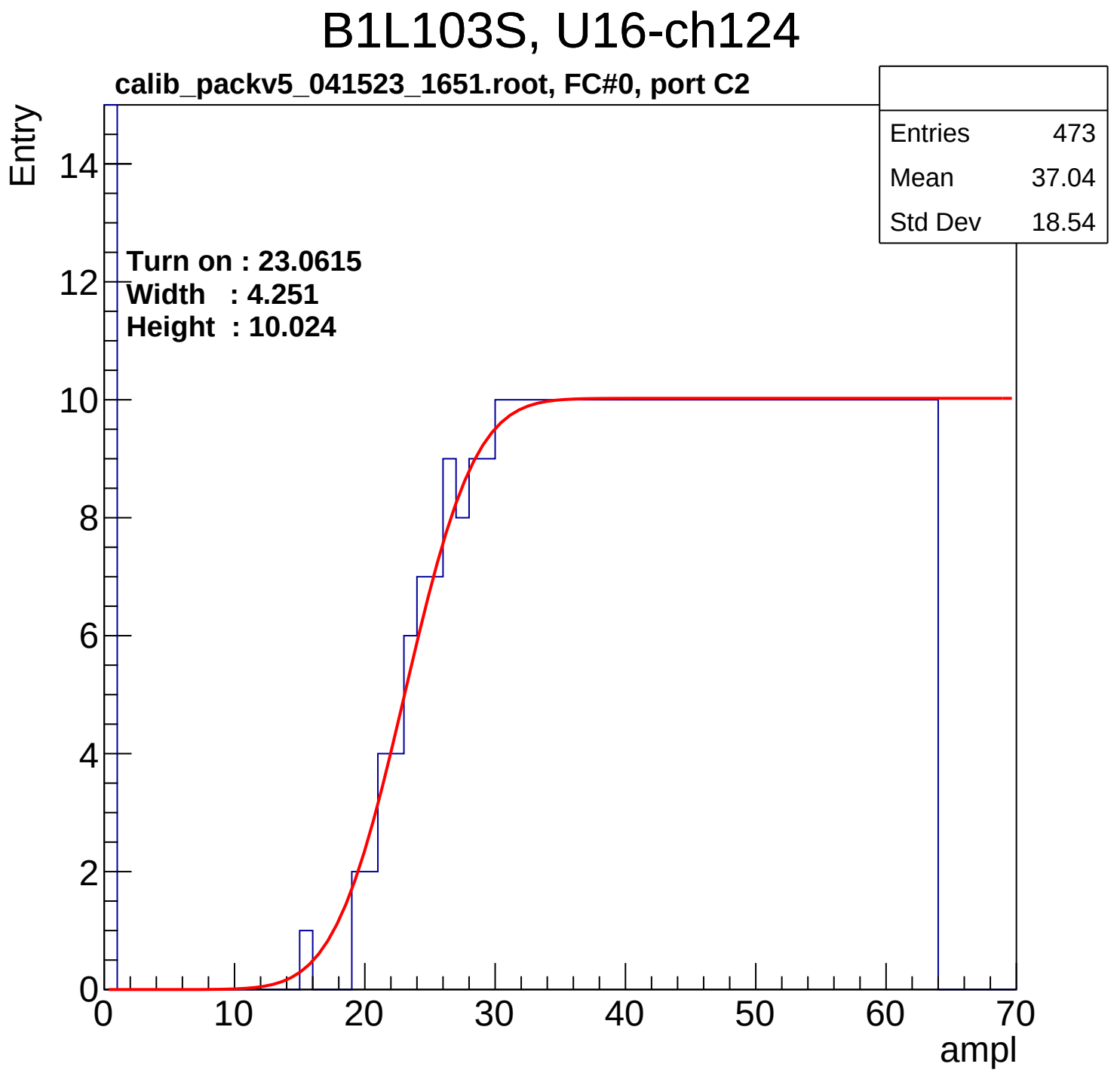

B1L103S, U16-ch123
calib_packv5_041523_1651.root, FC#0, port C2
Entries 426
Mean 39.05
Std Dev 18.15
Turn on : 27.1862
Width : 3.591
Height : 10.063
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U16-ch124
calib_packv5_041523_1651.root, FC#0, port C2
Entries 473
Mean 37.04
Std Dev 18.54
Turn on : 23.0615
Width : 4.251
Height : 10.024
Entry
ampl
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4
6
8
10
12
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0
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20
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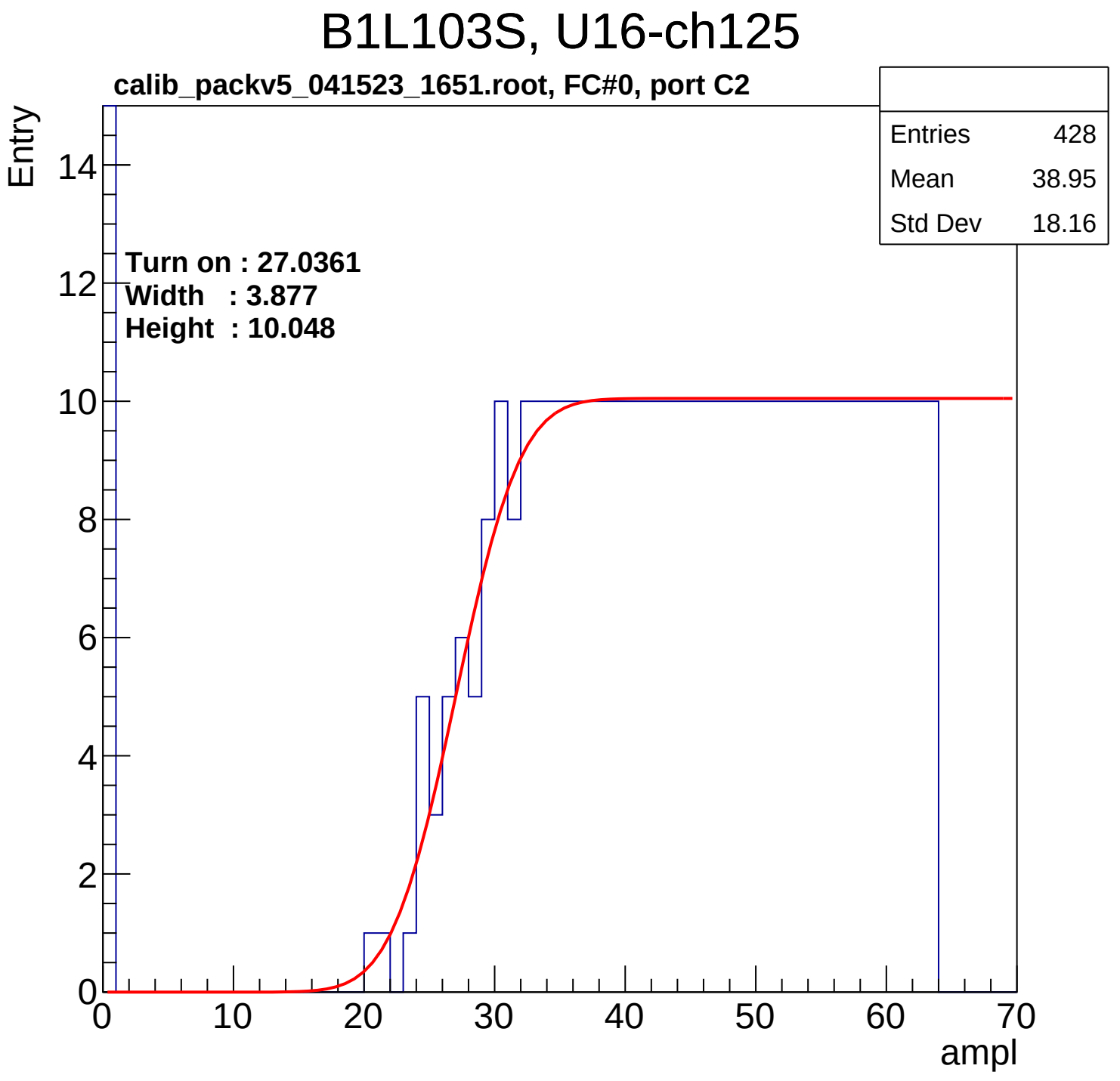
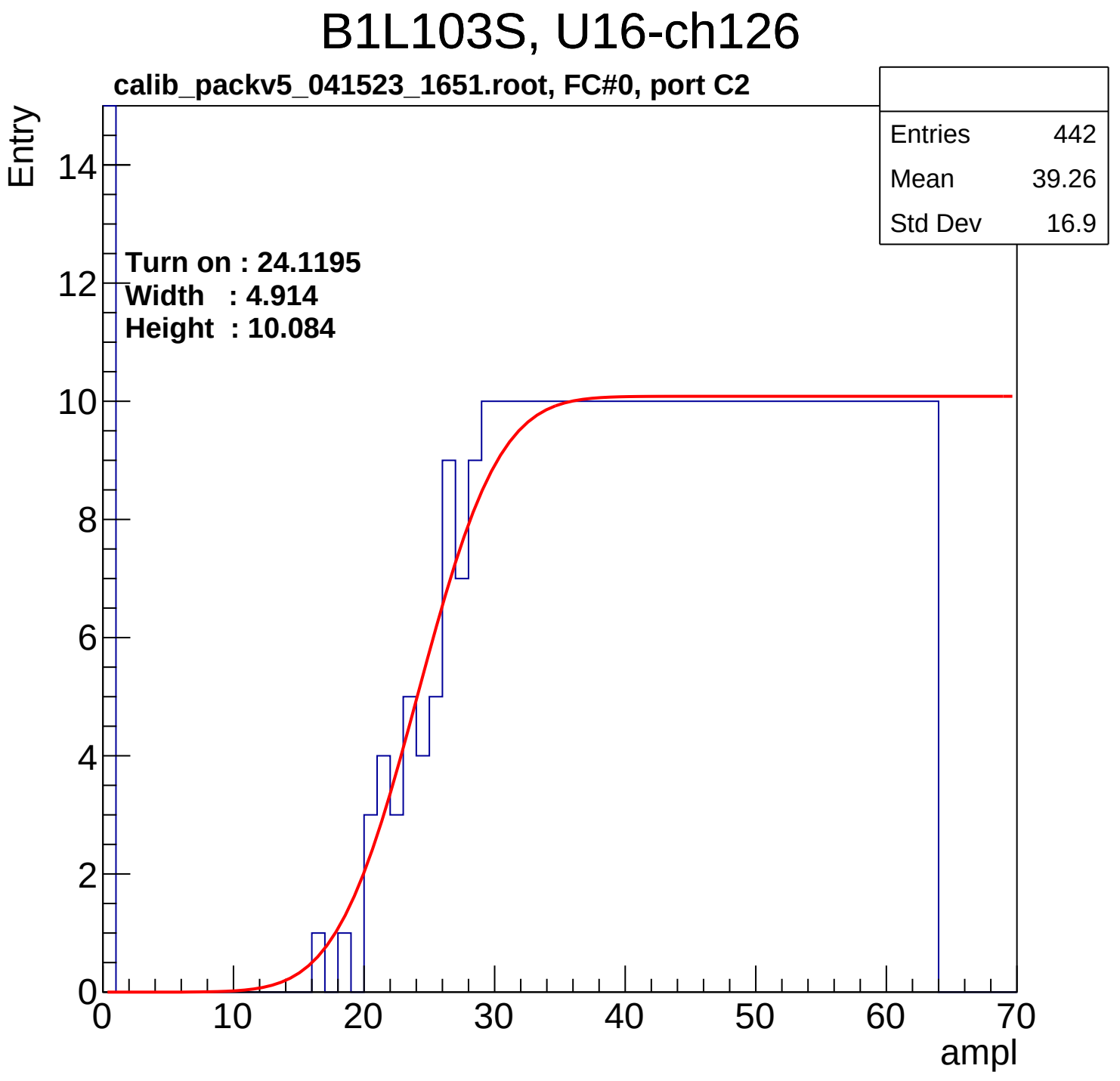
40
50
60
70


B1L103S, U16-ch125
calib_packv5_041523_1651.root, FC#0, port C2
Entries 428
Mean 38.95
Std Dev 18.16
Turn on : 27.0361
Width : 3.877
Height : 10.048
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U16-ch126
calib_packv5_041523_1651.root, FC#0, port C2
Entries 442
Mean 39.26
Std Dev 16.9
Turn on : 24.1195
Width : 4.914
Height : 10.084
Entry
ampl
0
2
4
6
8
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0
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60
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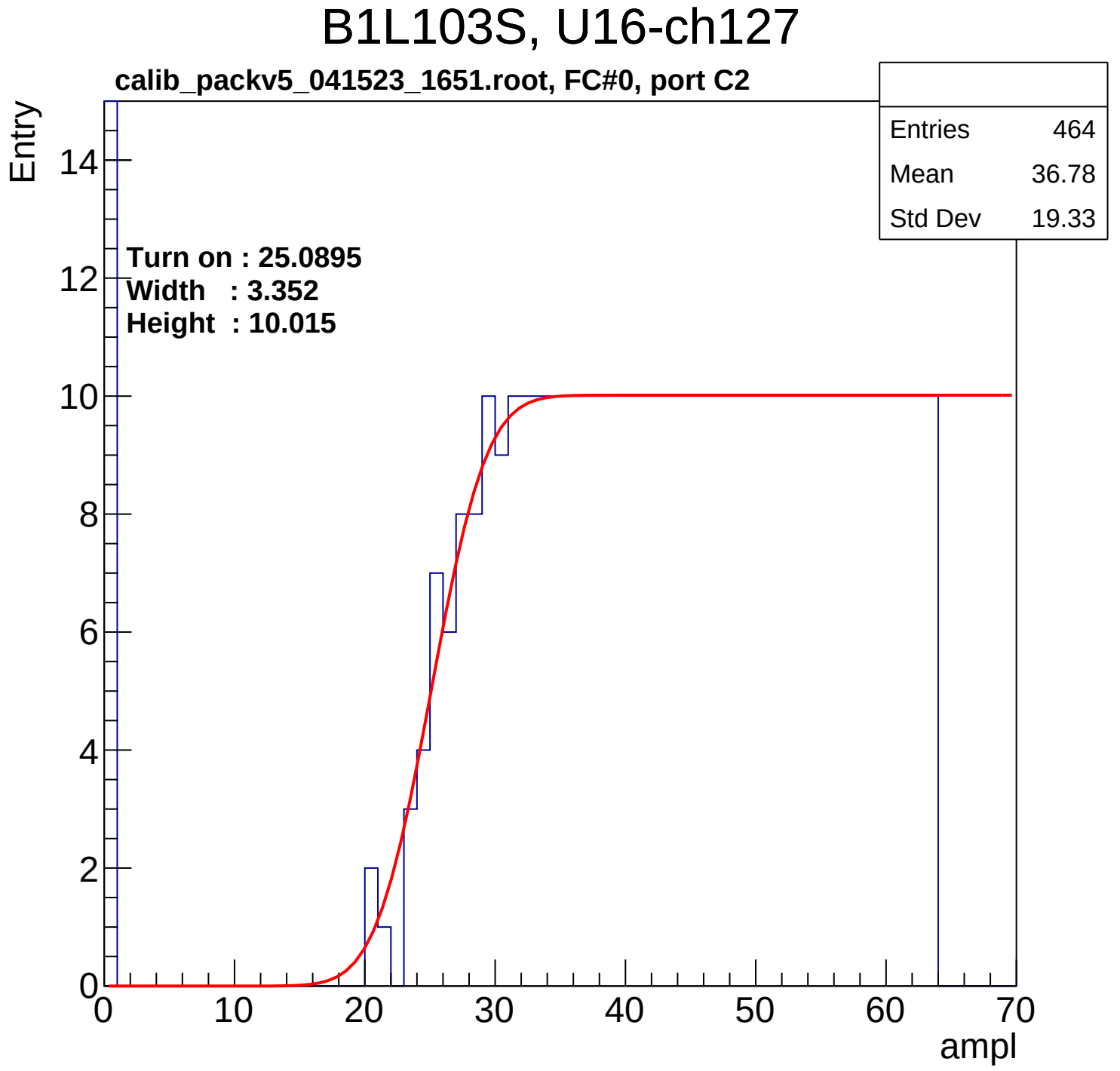
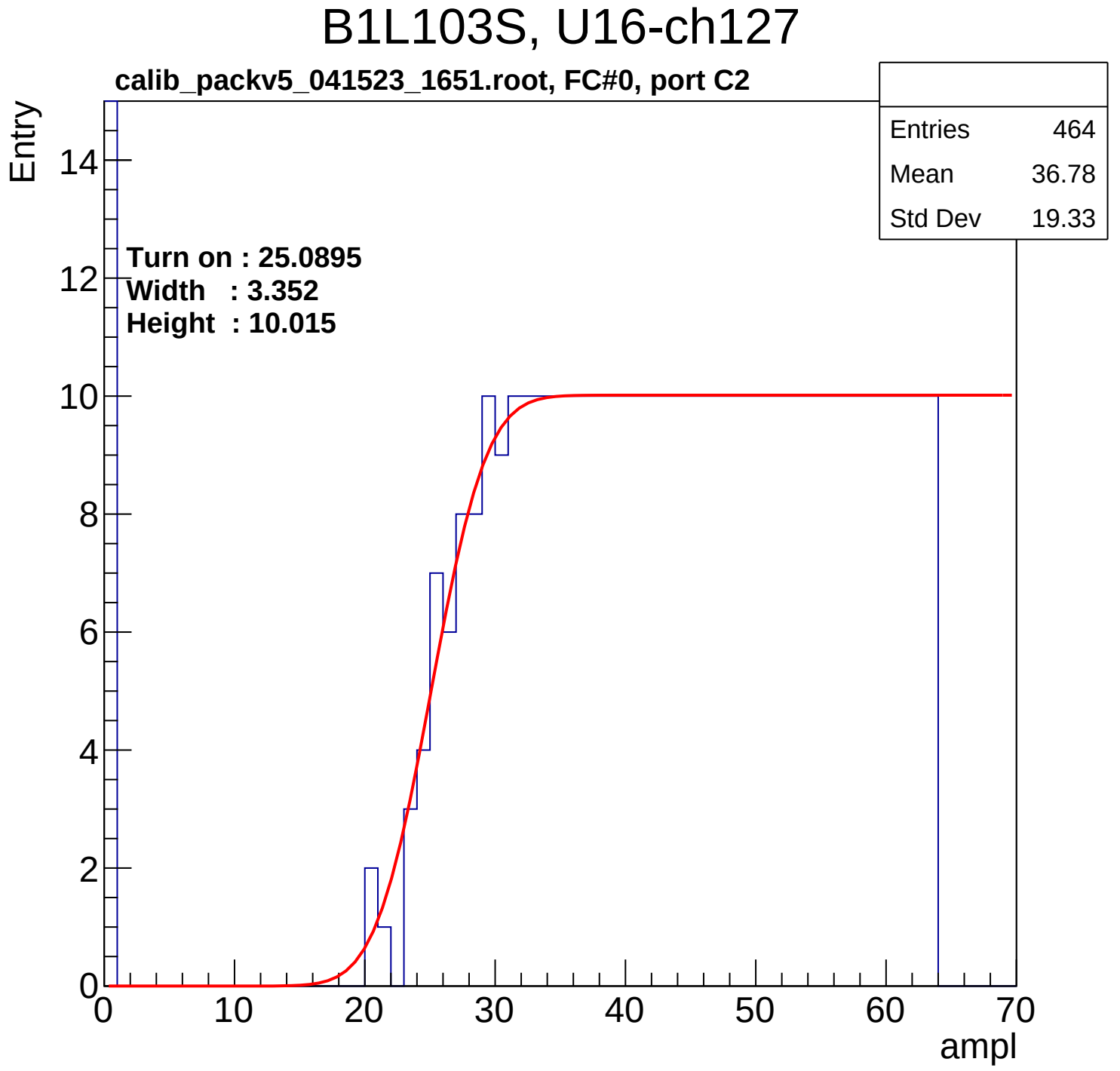

B1L103S, U16-ch127
calib_packv5_041523_1651.root, FC#0, port C2
Entries 464
Mean 36.78
Std Dev 19.33
Turn on : 25.0895
Width : 3.352
Height : 10.015
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U16-ch127
calib_packv5_041523_1651.root, FC#0, port C2
Entries 464
Mean 36.78
Std Dev 19.33
Turn on : 25.0895
Width : 3.352
Height : 10.015
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70