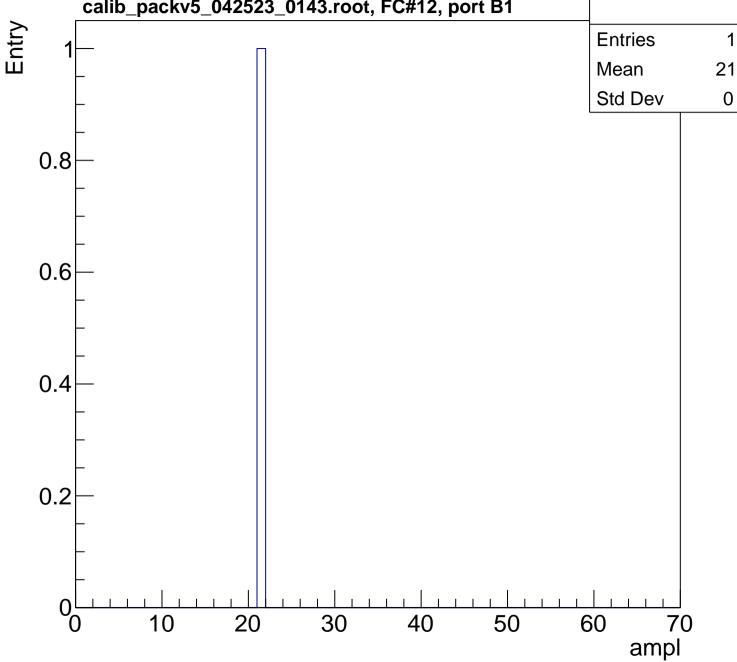
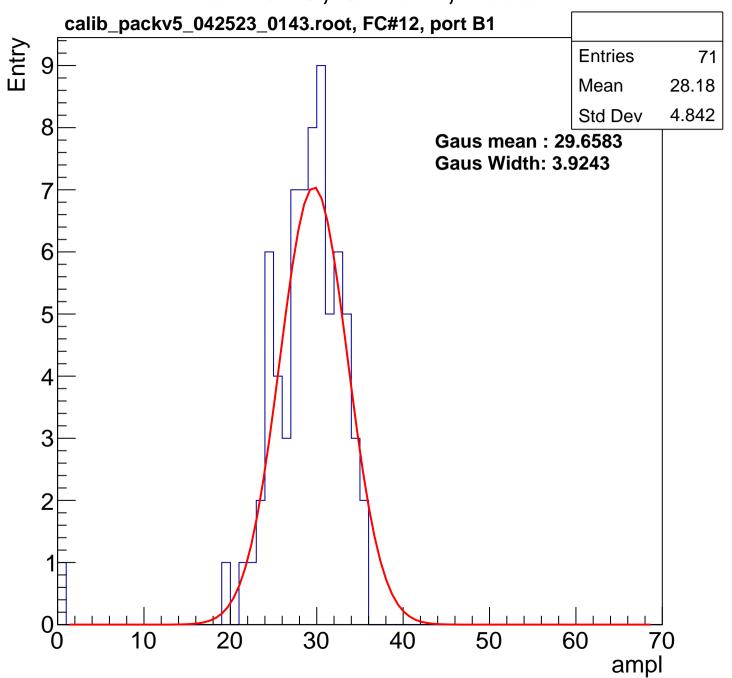


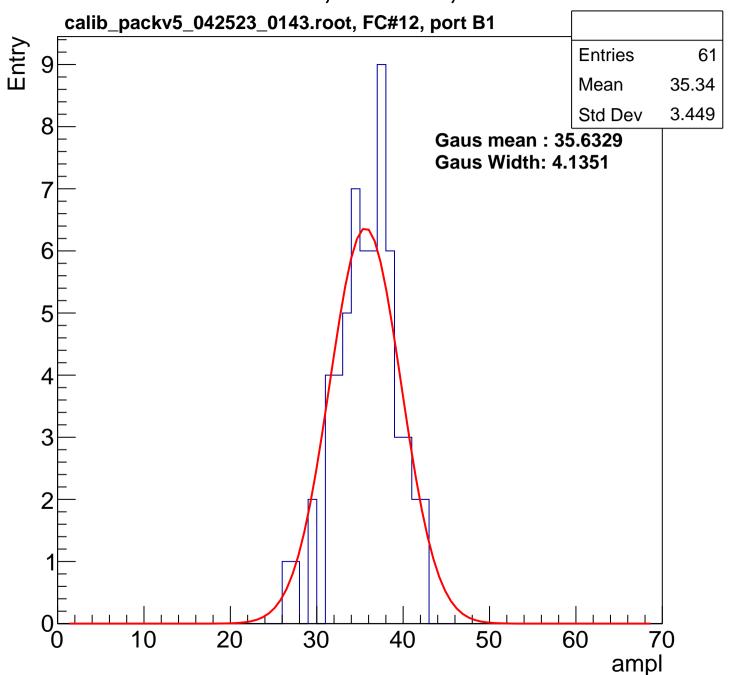
B0L102S, U2-ch3, adc7 calib_packv5_042523_0143.root, FC#12, port B1

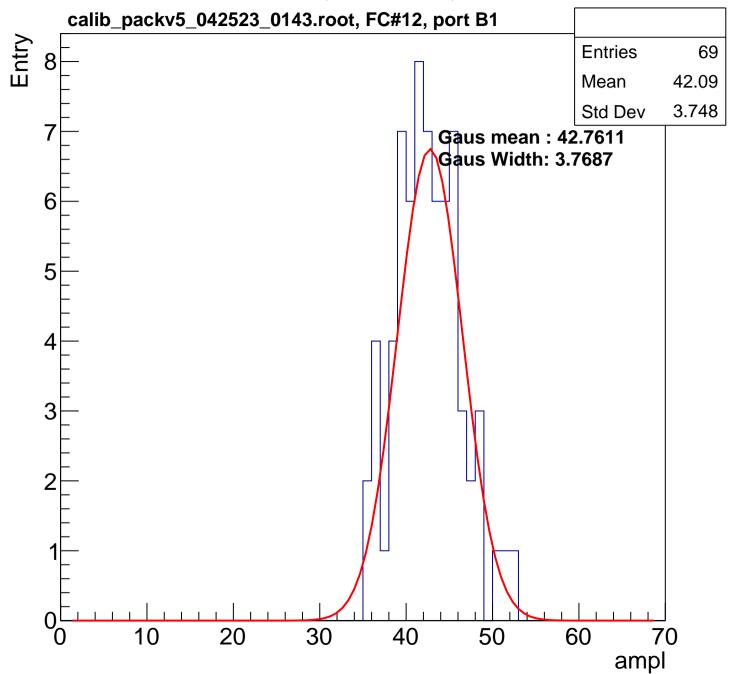
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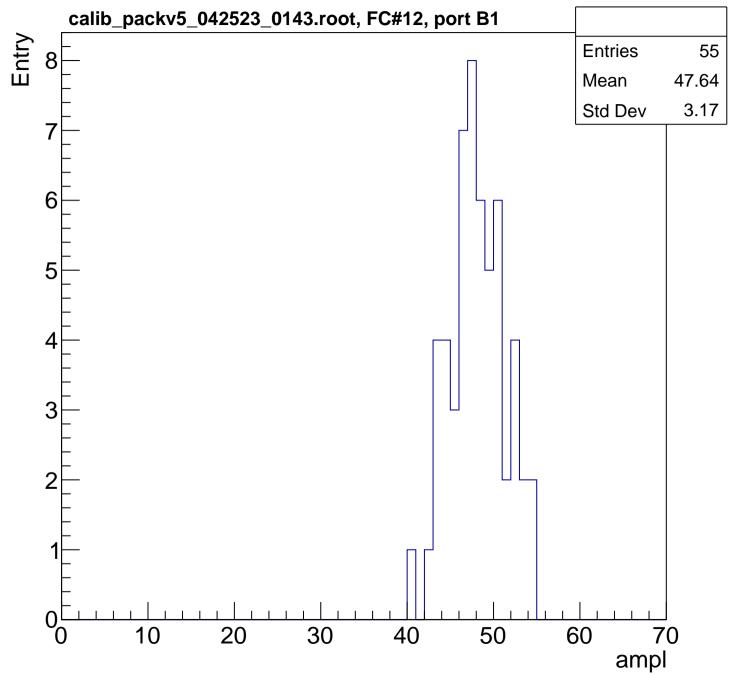
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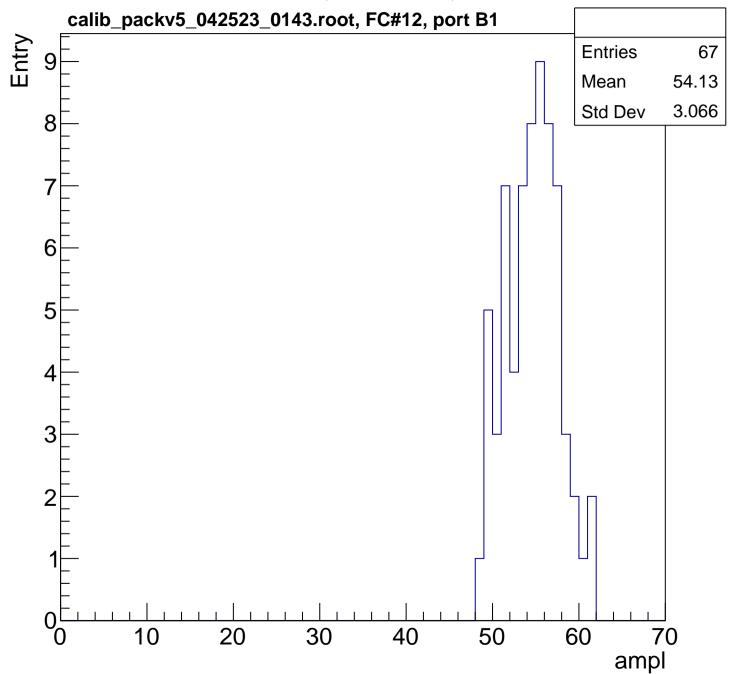


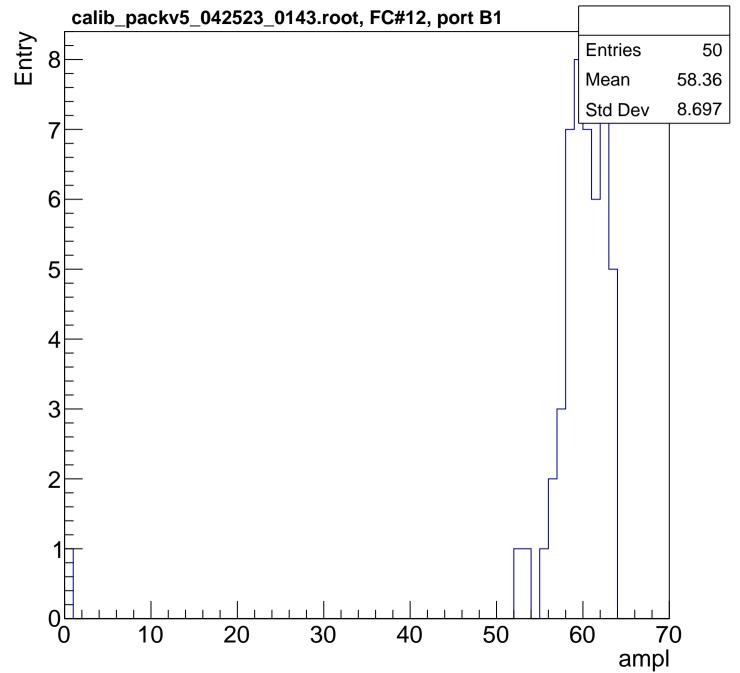


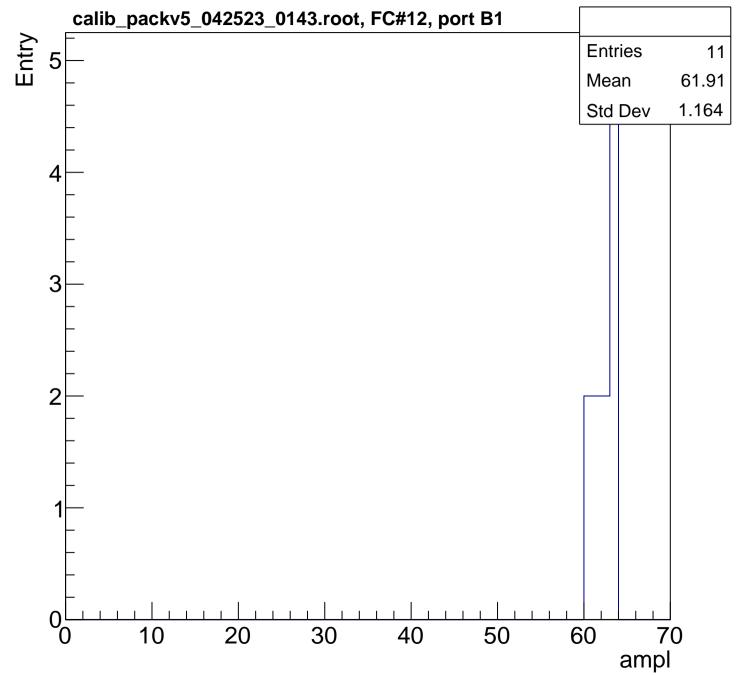


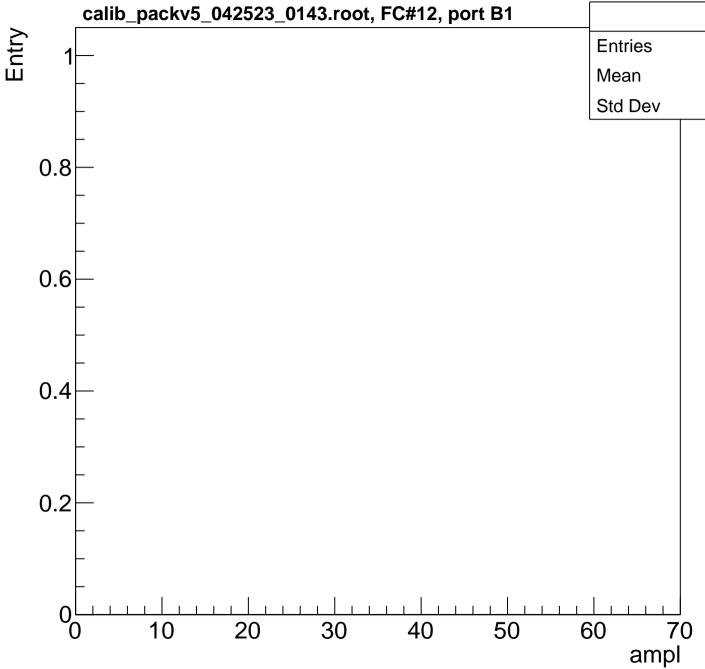


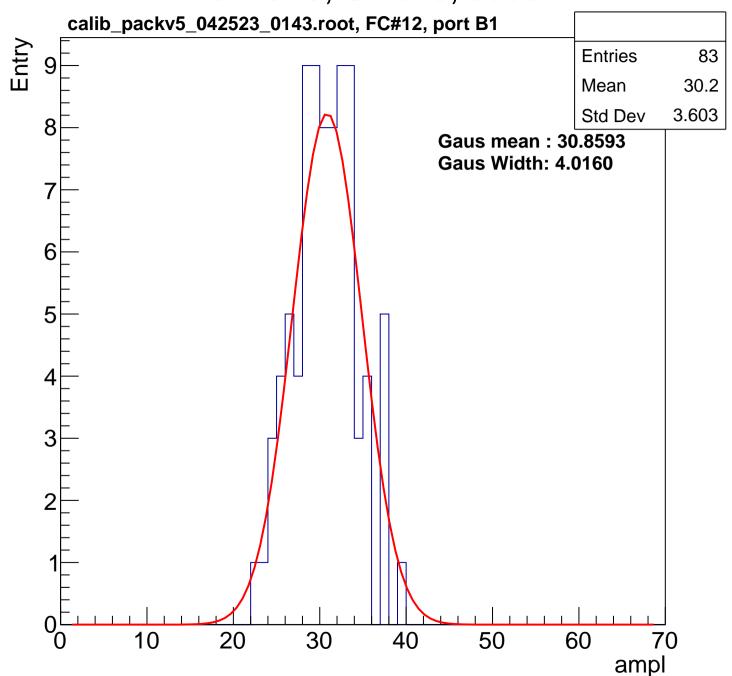


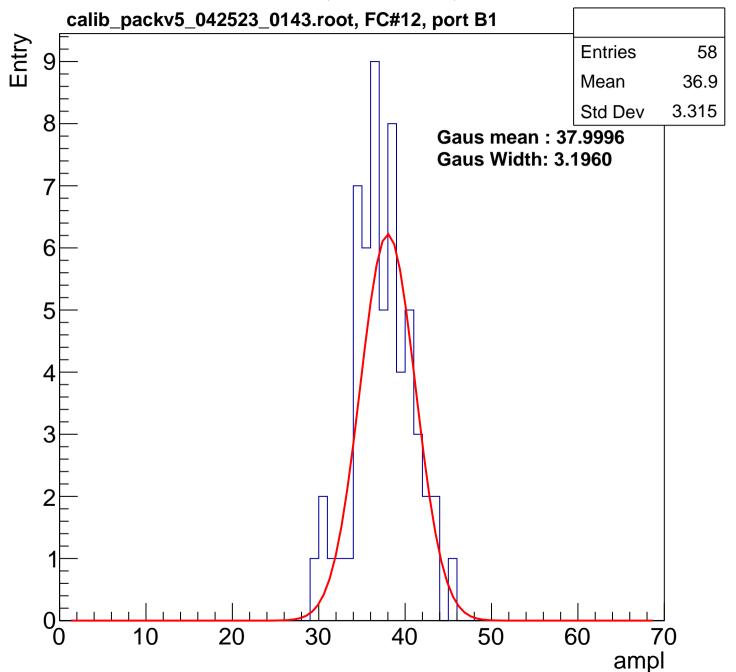


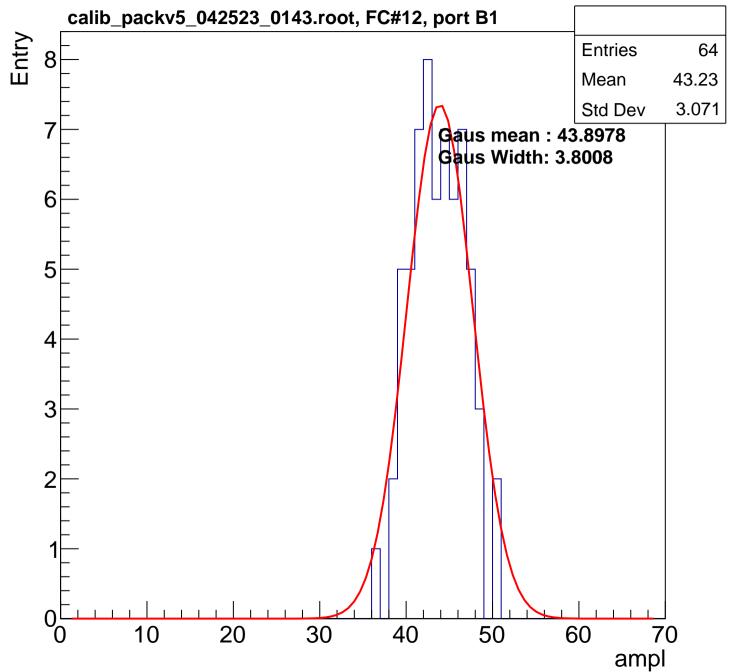


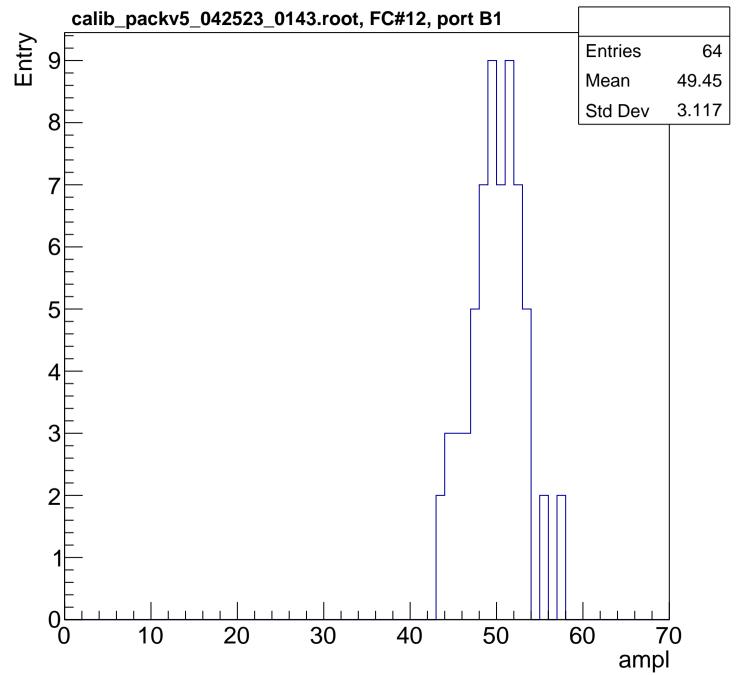


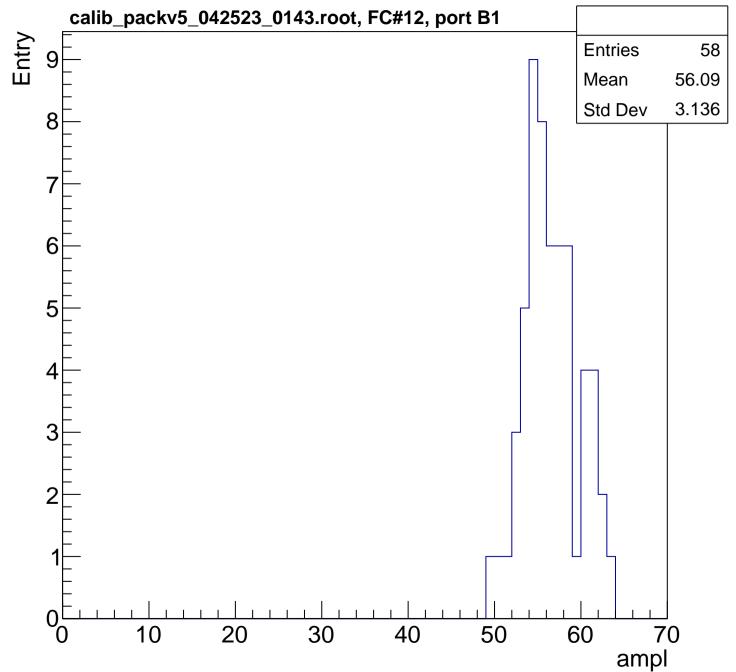


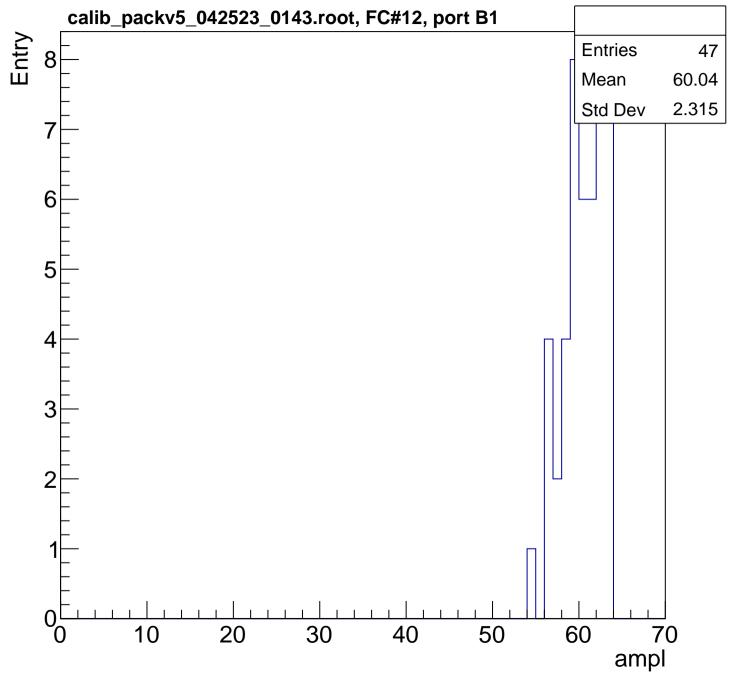


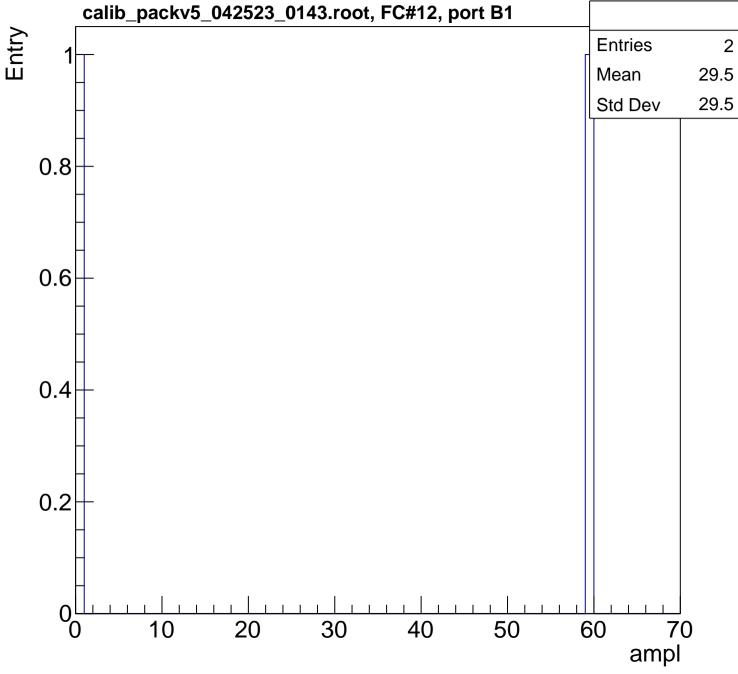


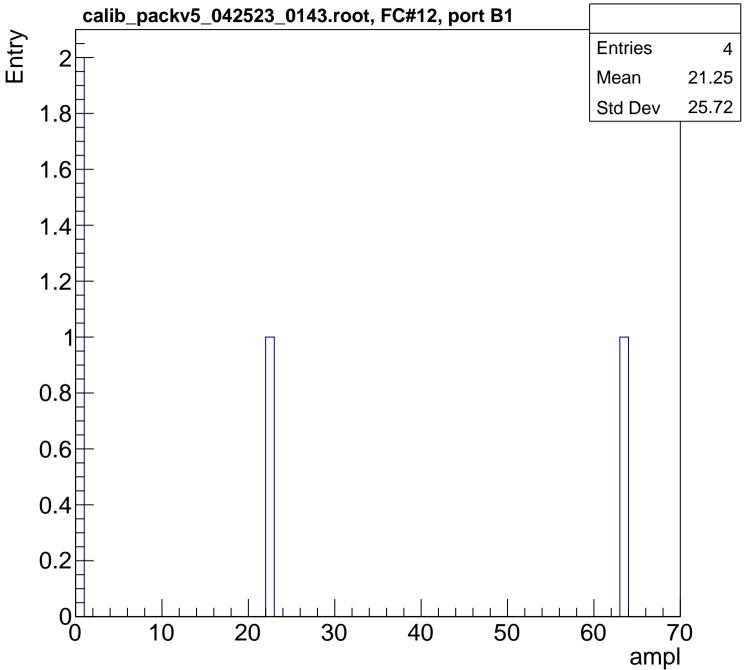


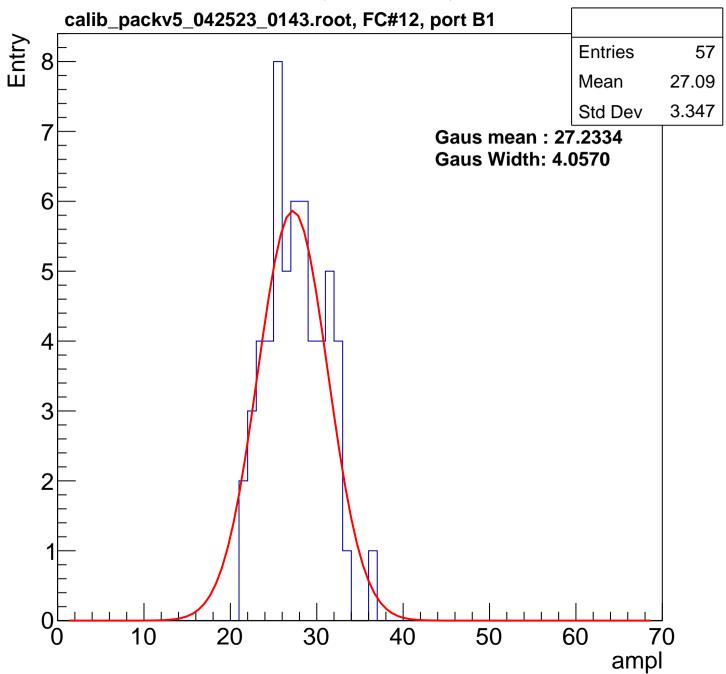


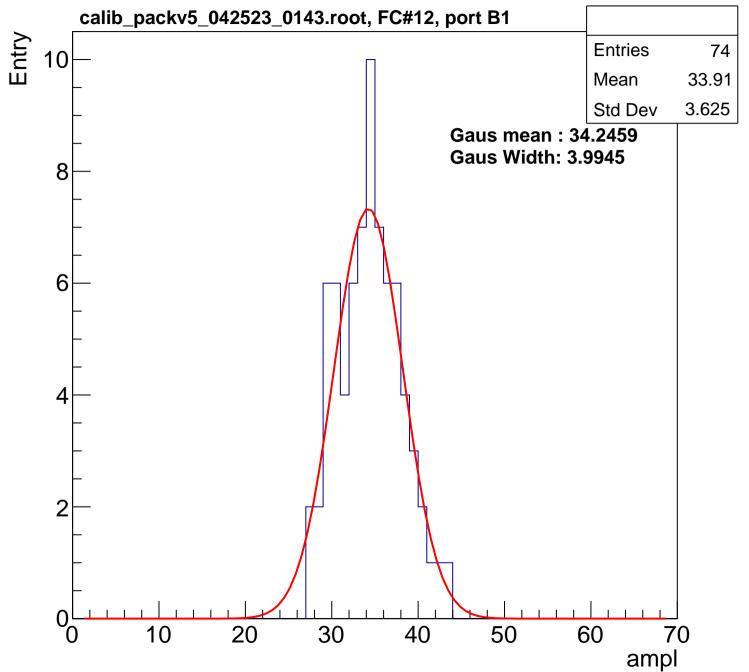


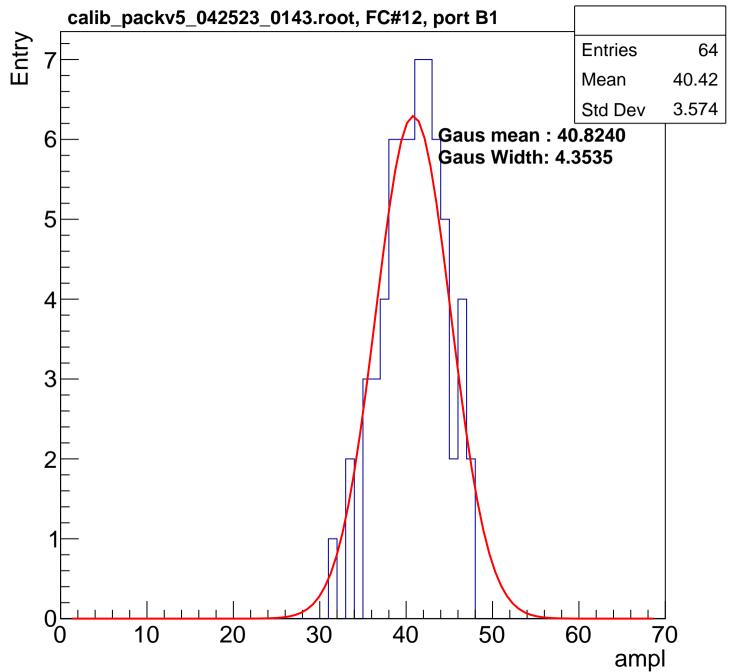


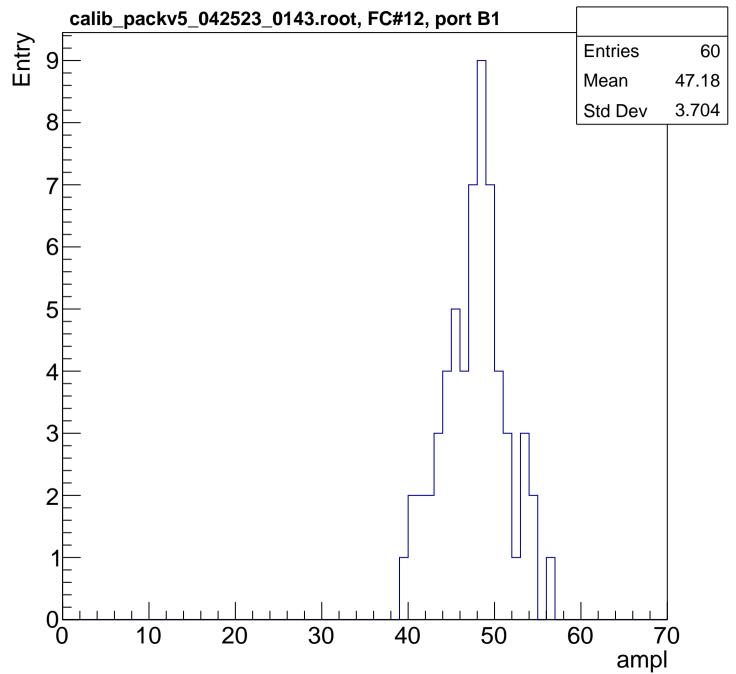


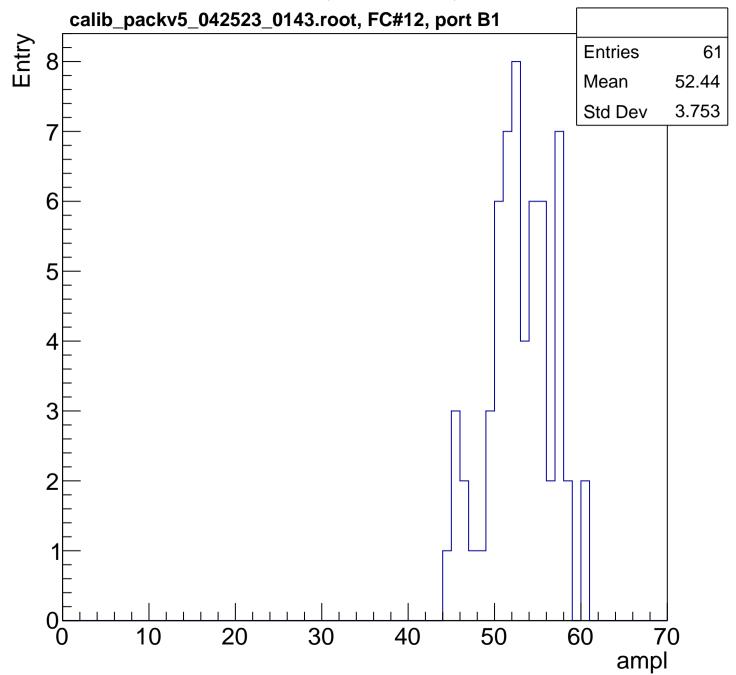


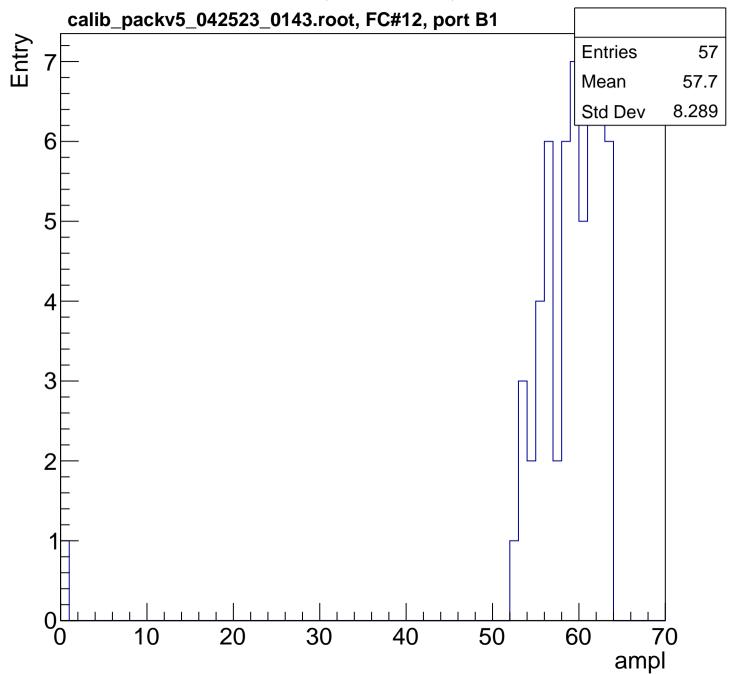


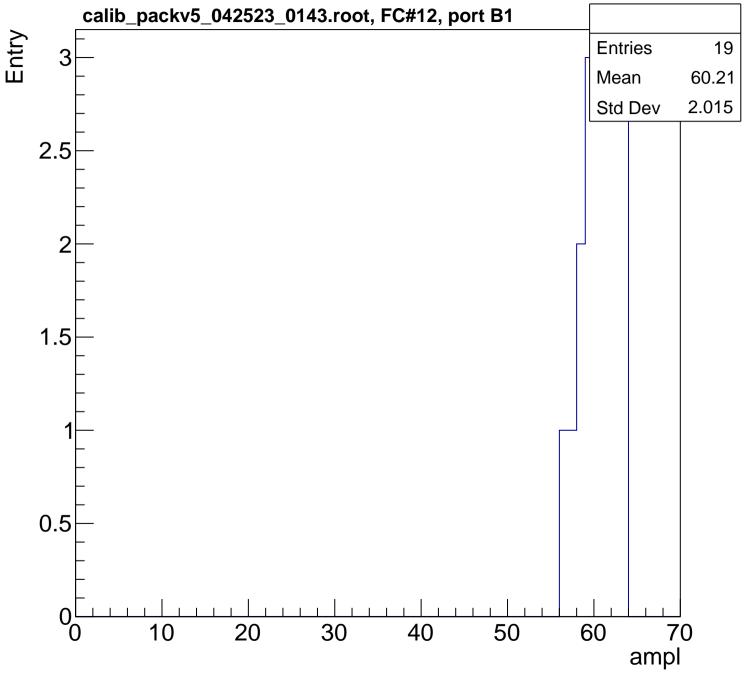




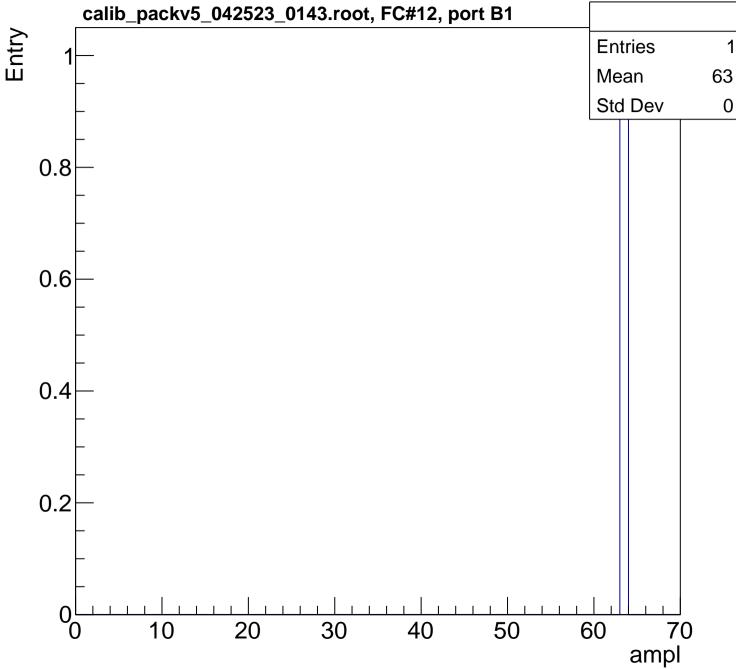


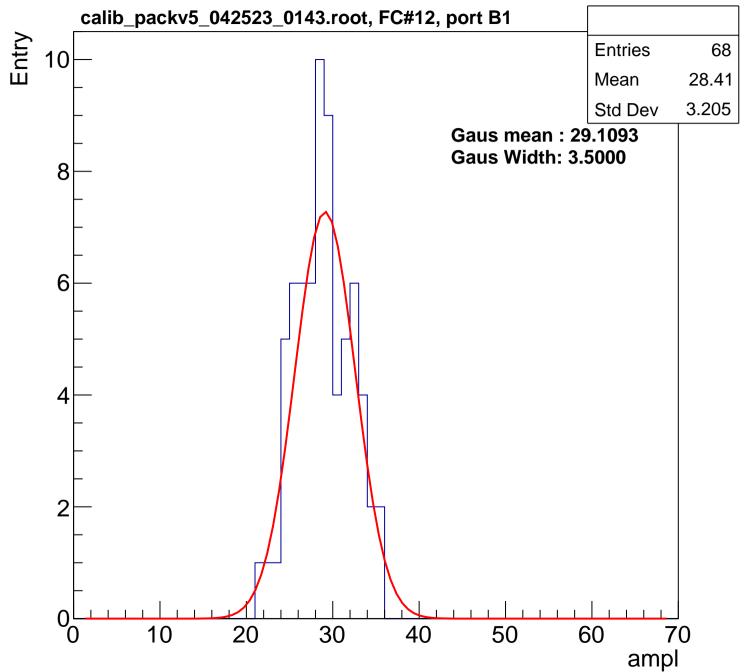


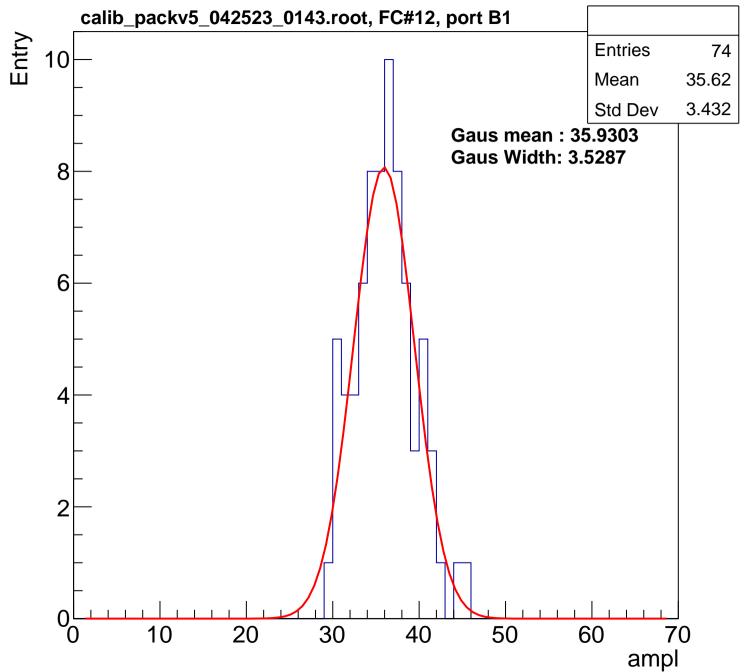


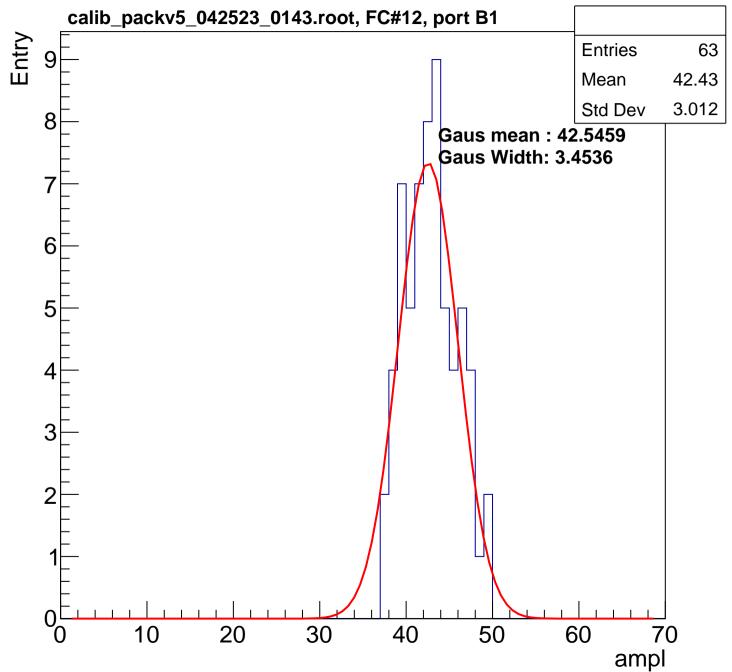


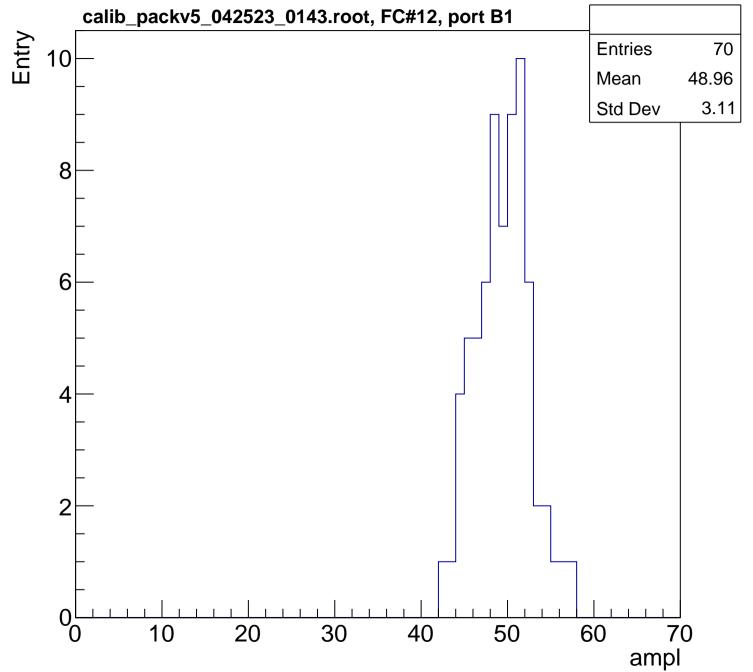
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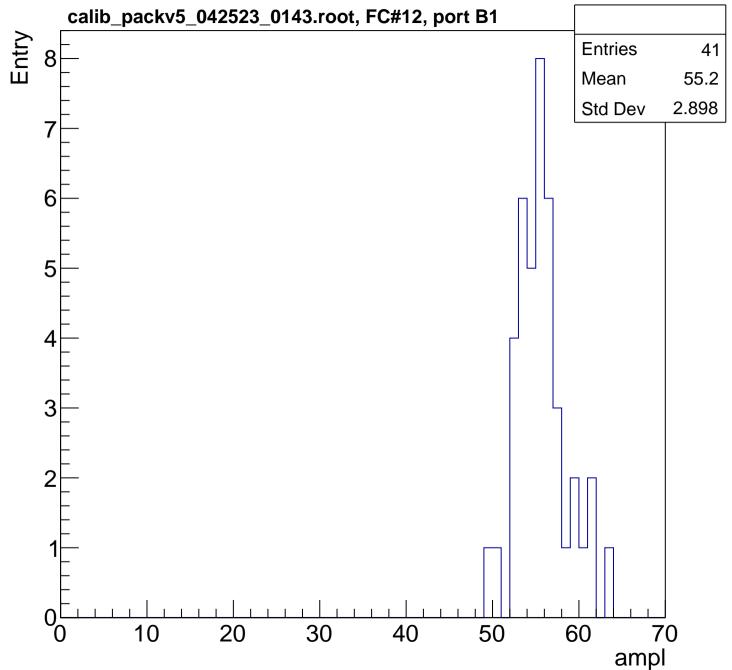


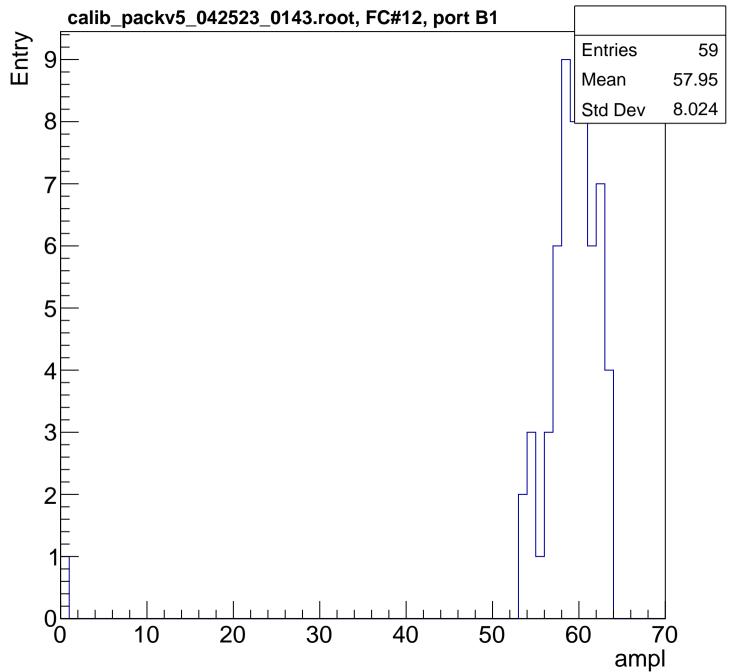


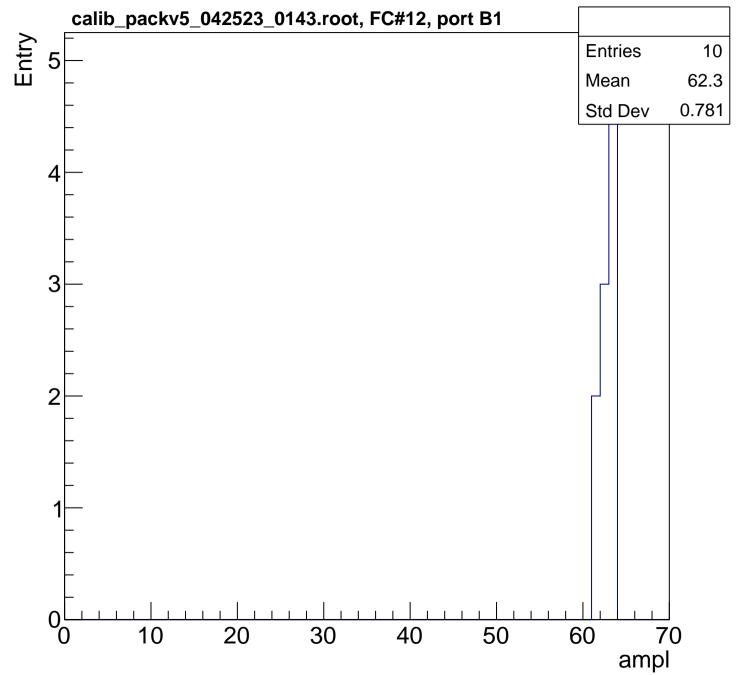


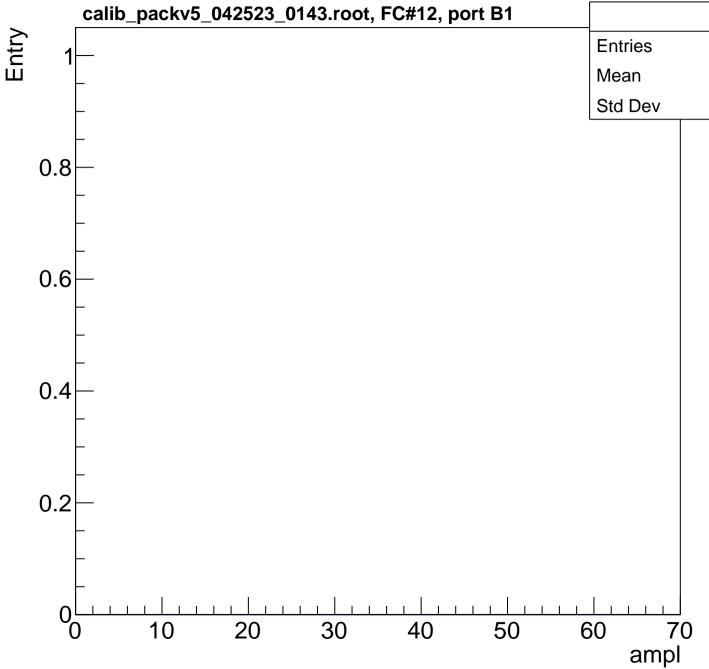


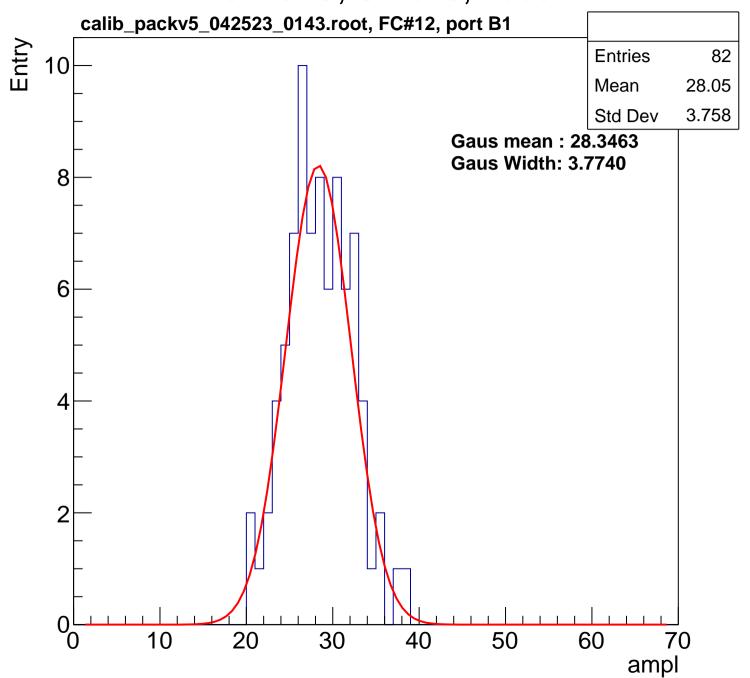


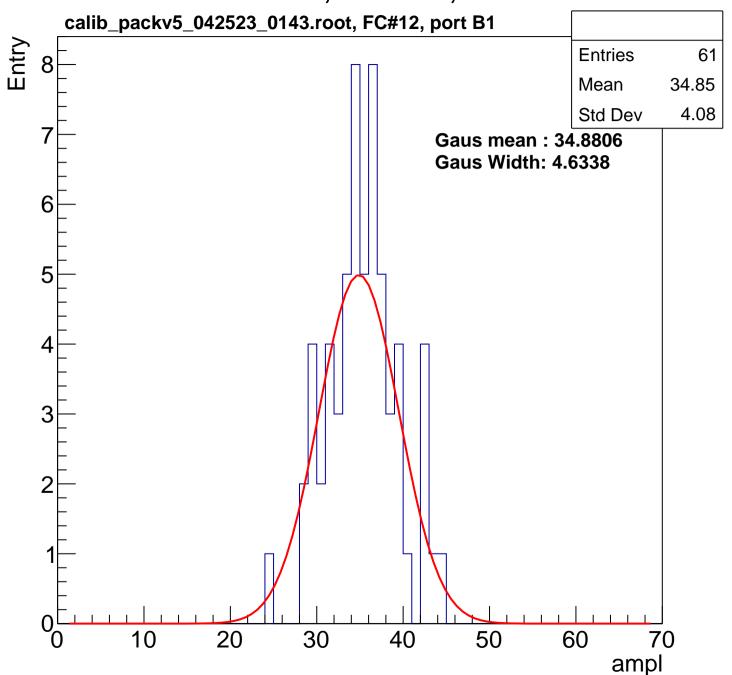


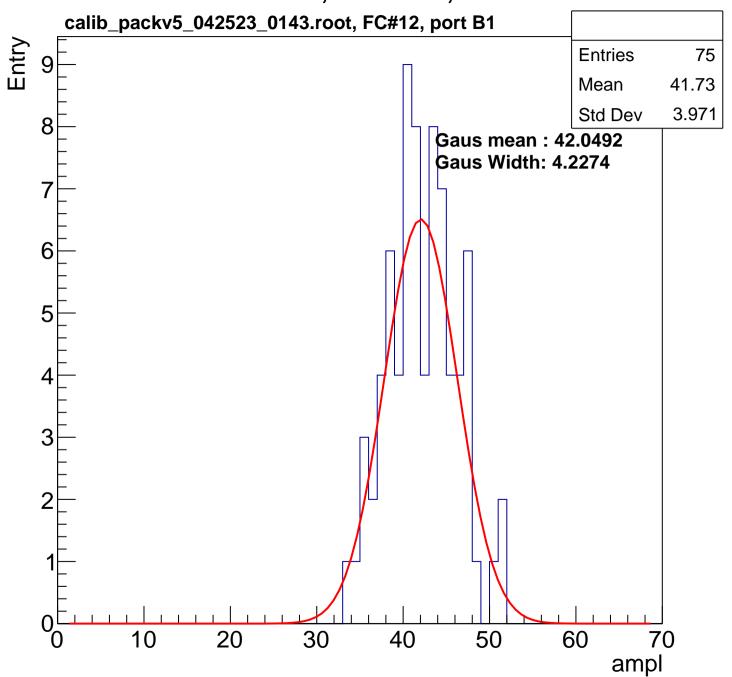


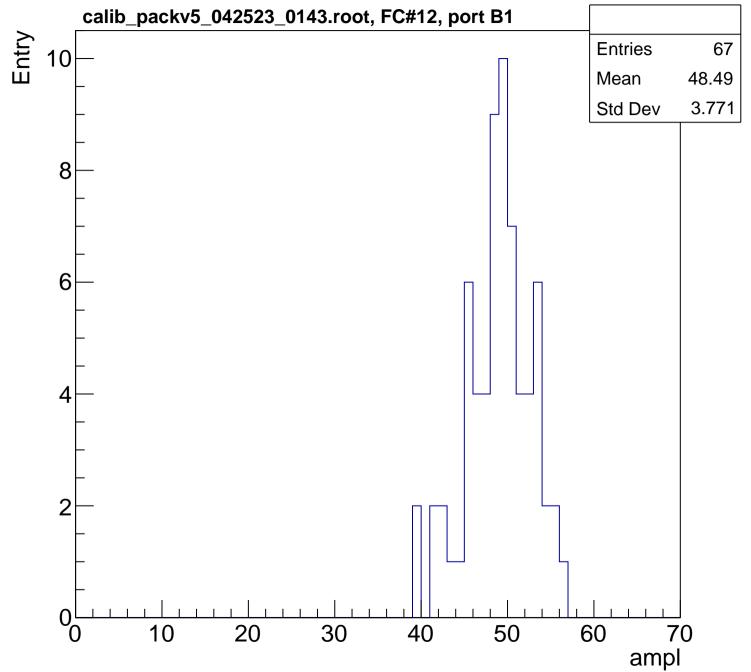


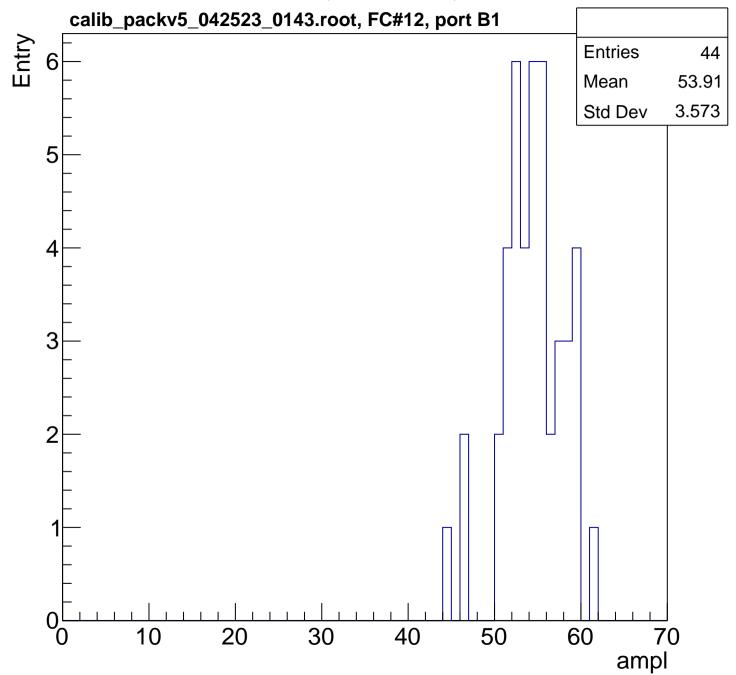


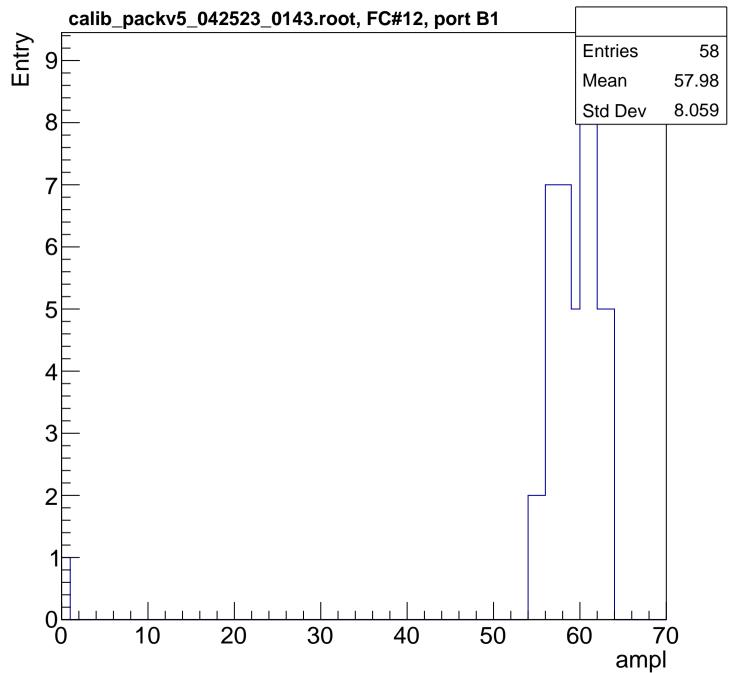


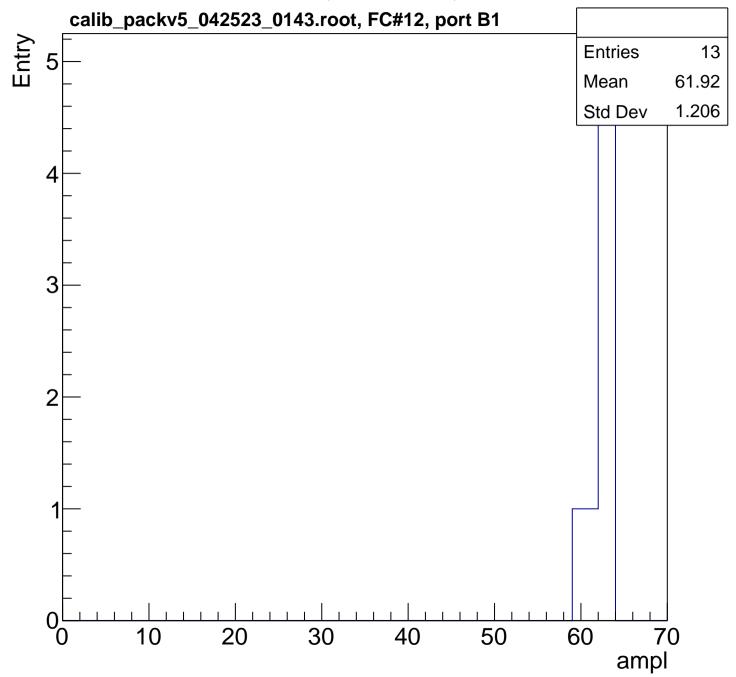




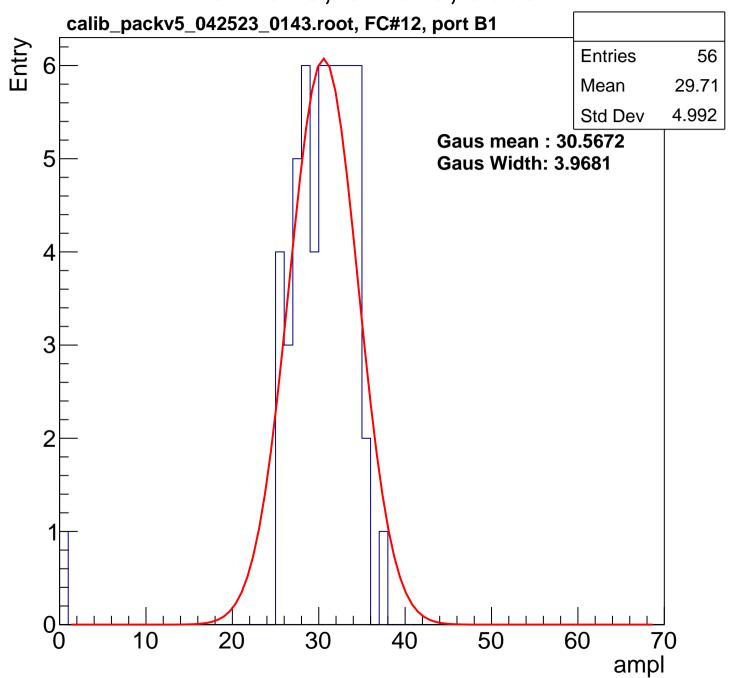


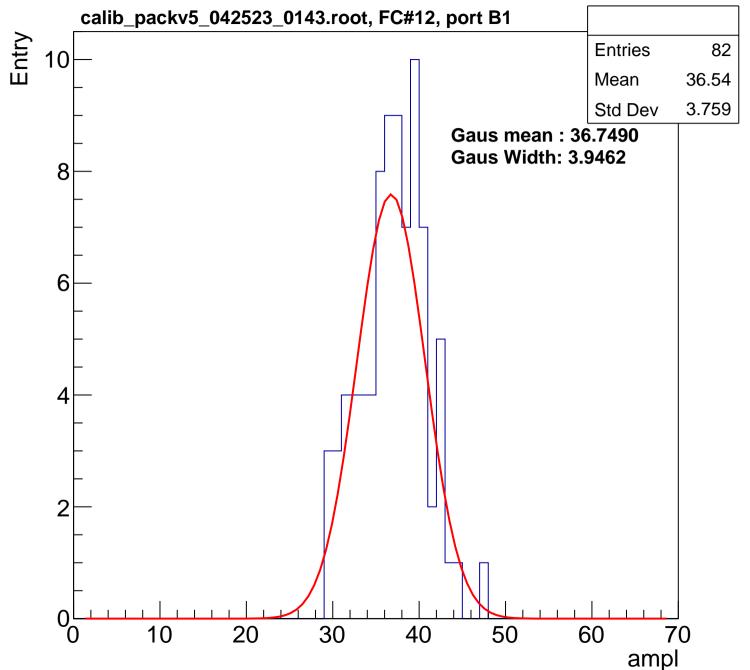


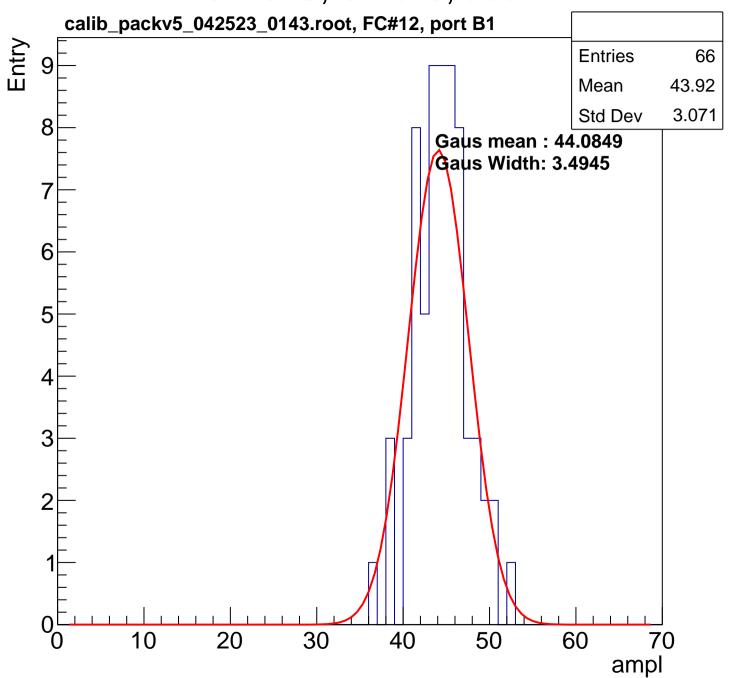


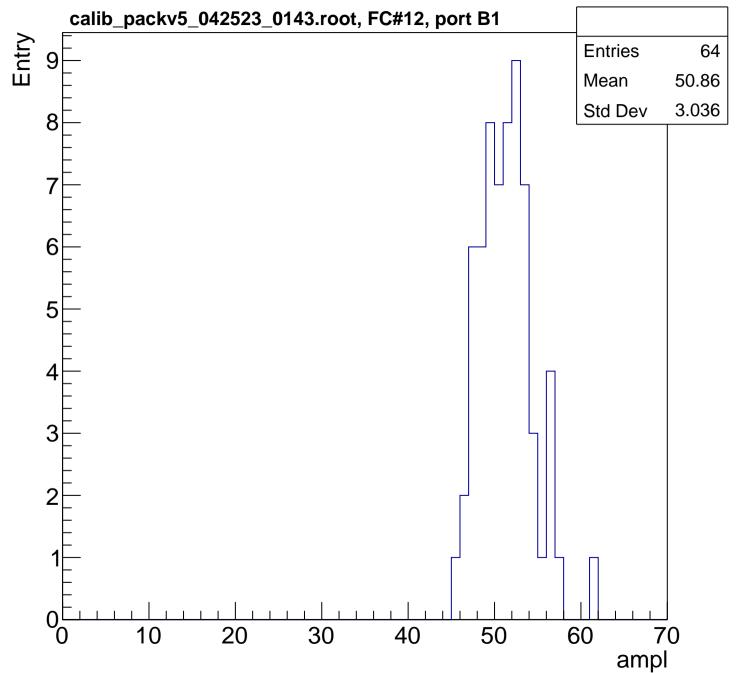


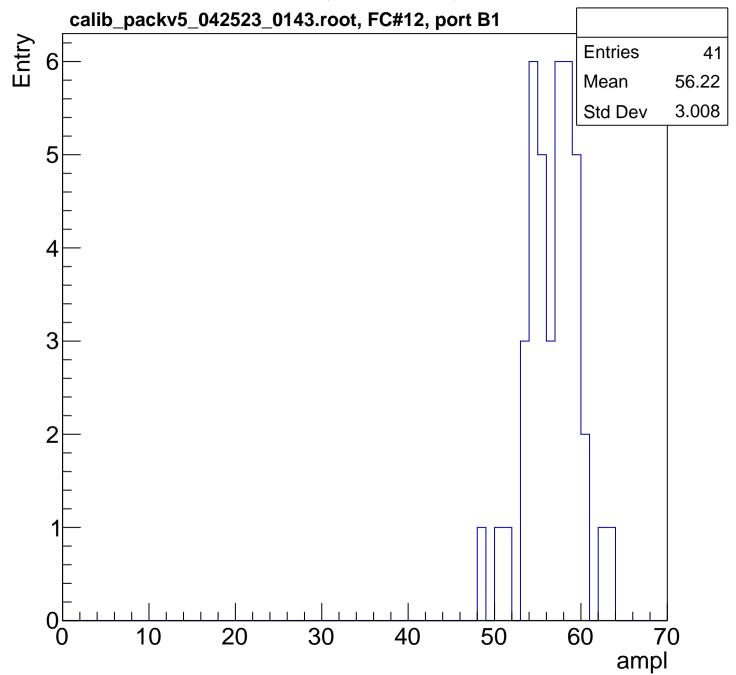
B0L102S, U2-ch8, adc7 calib_packv5_042523_0143.root, FC#12, port B1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

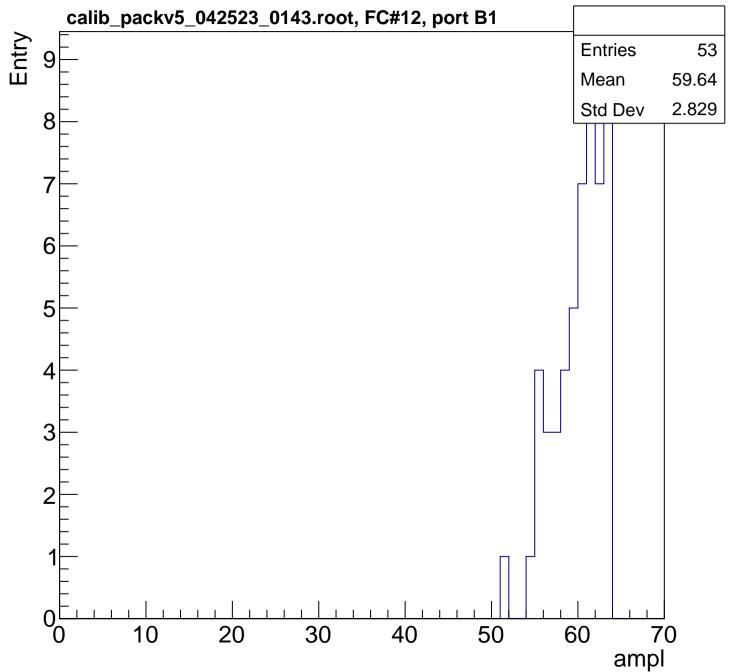


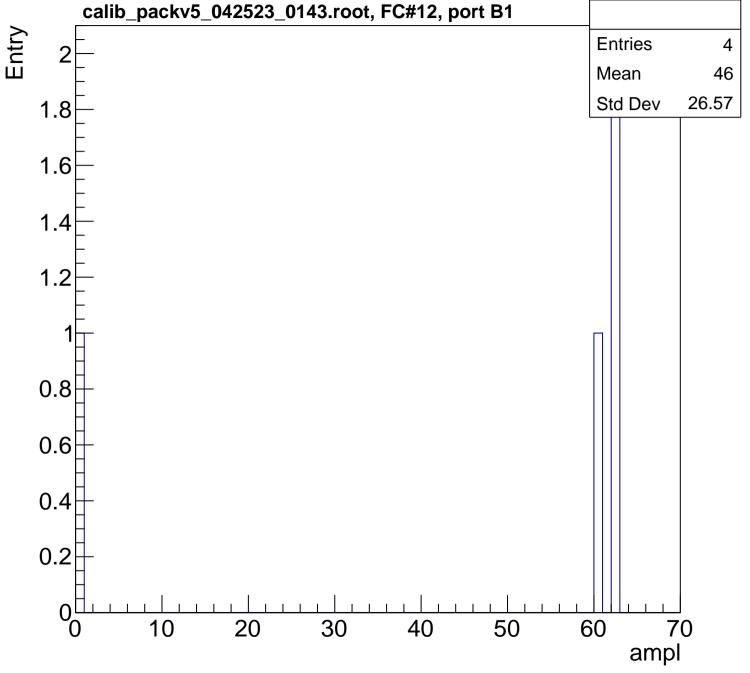




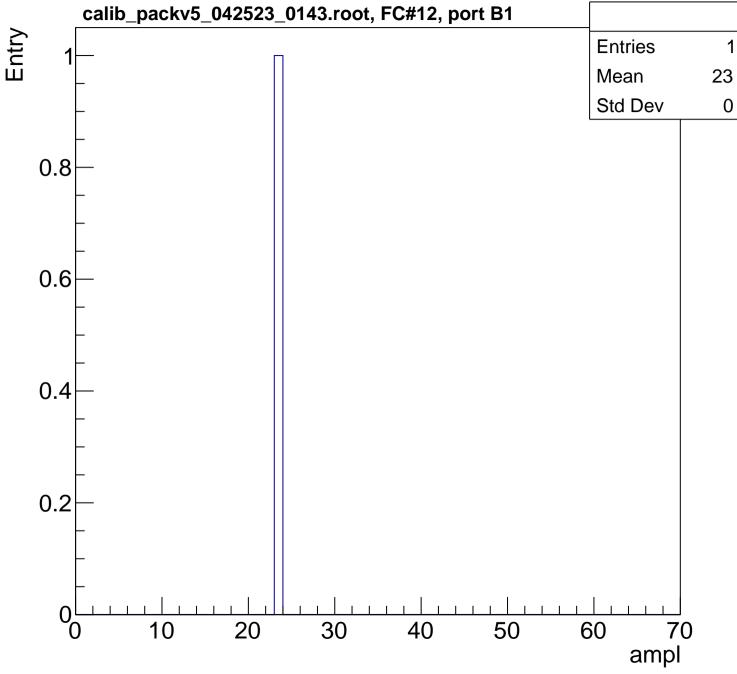


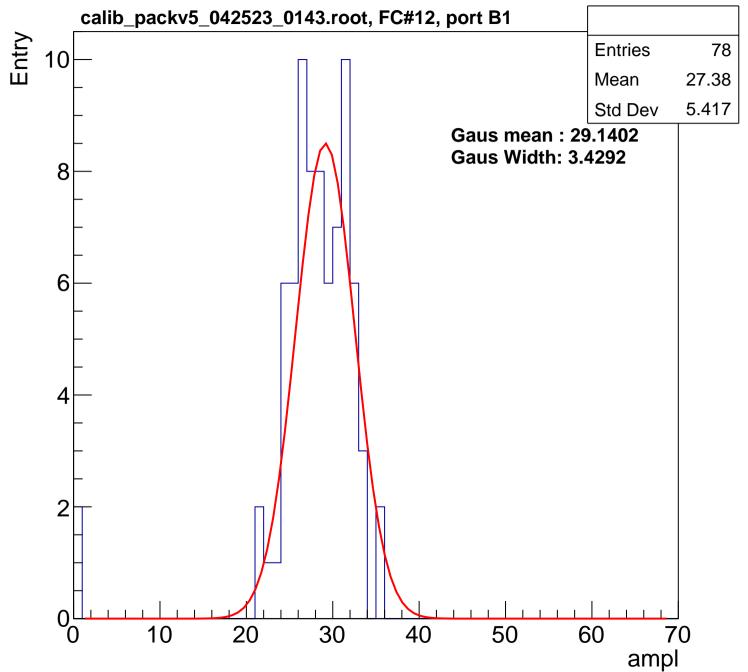


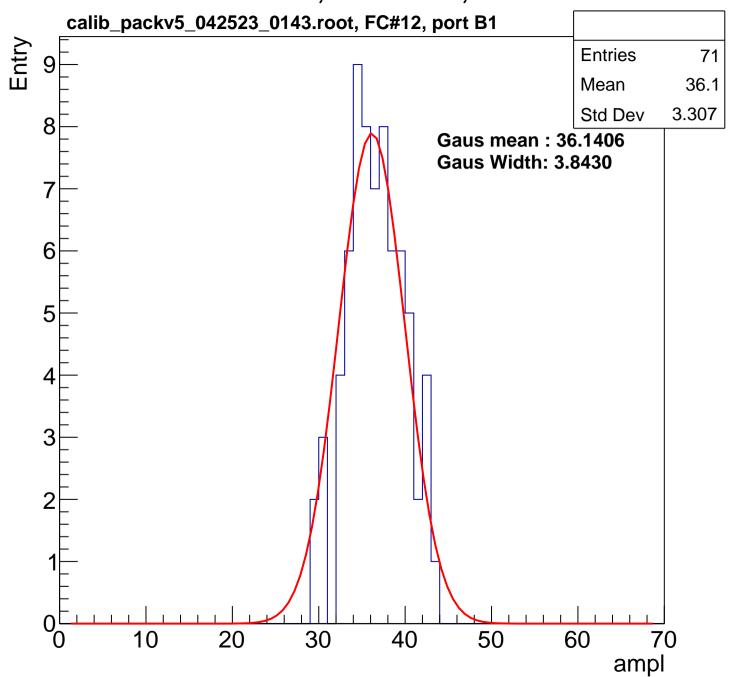


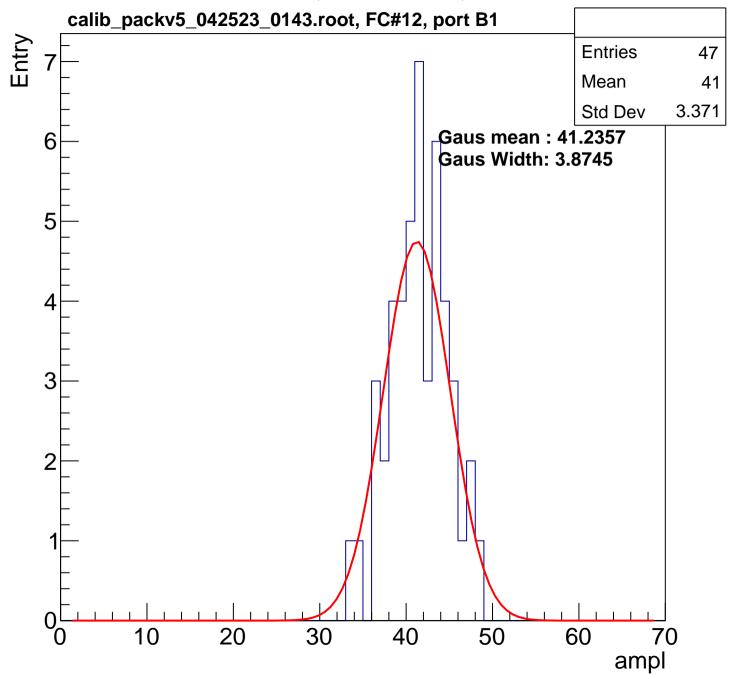


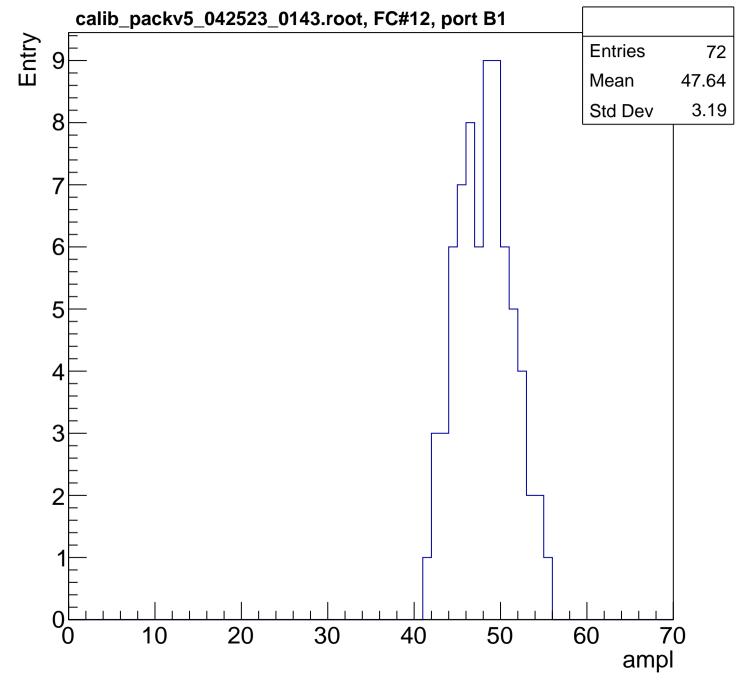
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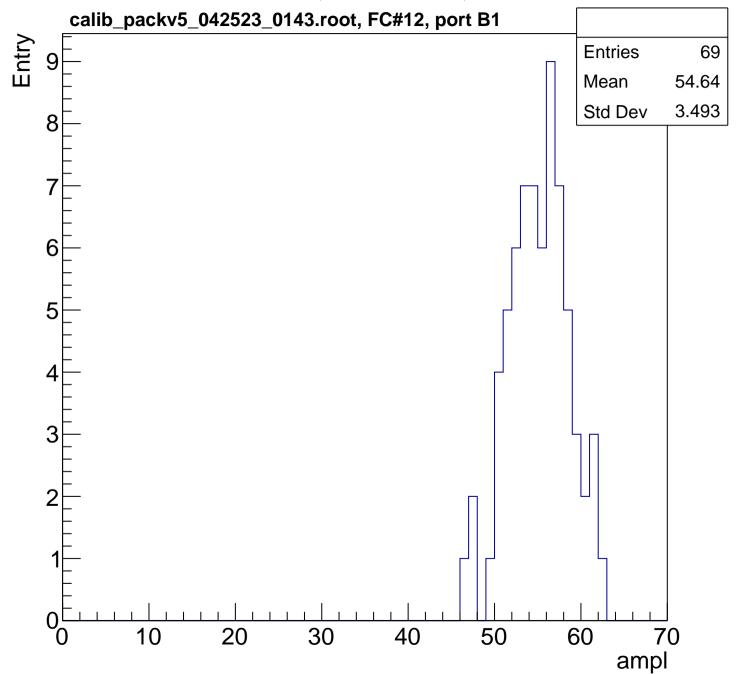


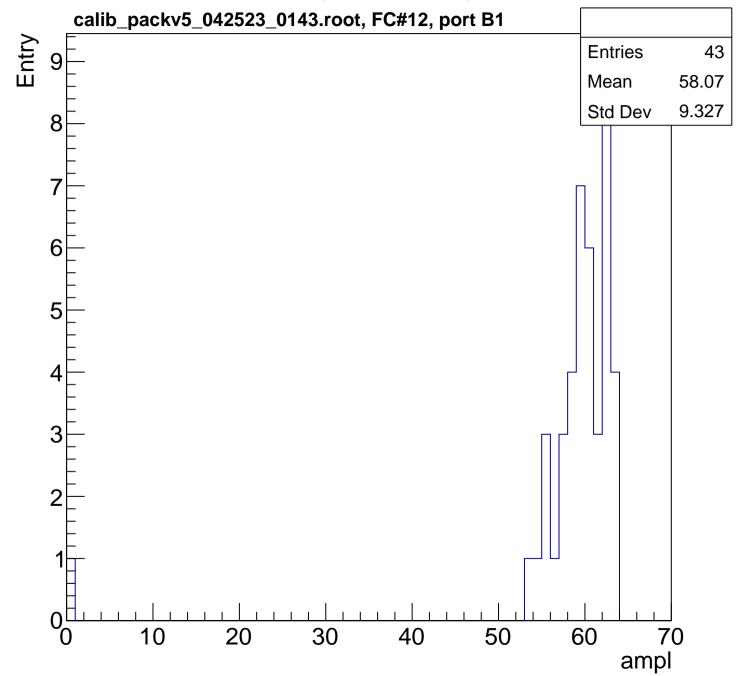


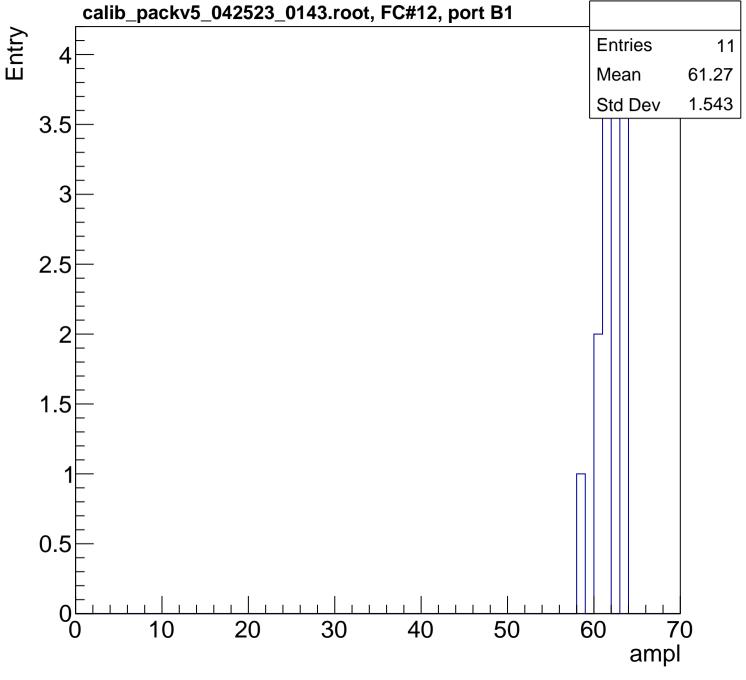


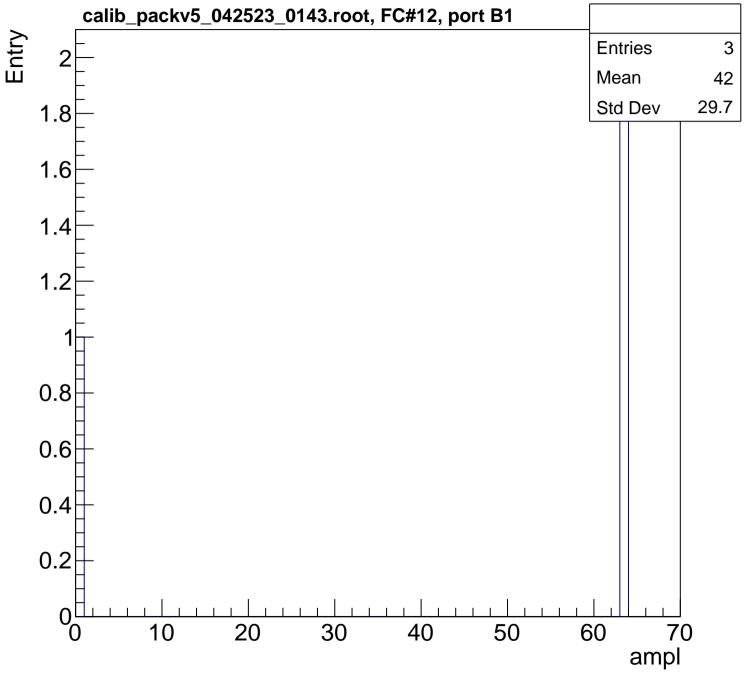


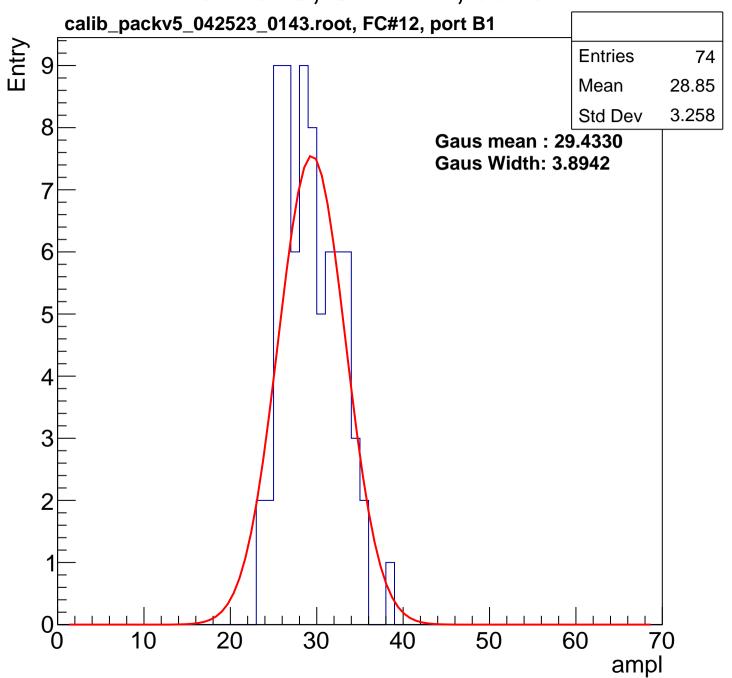


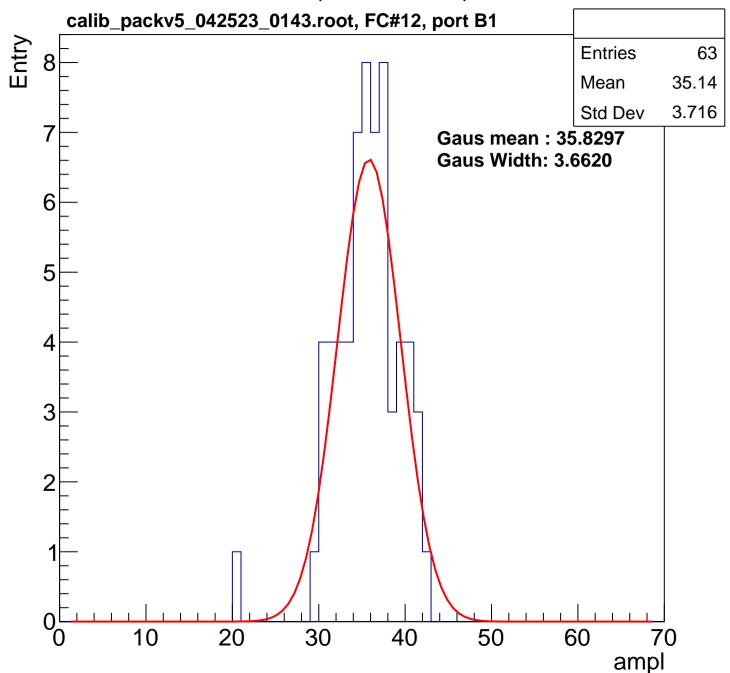


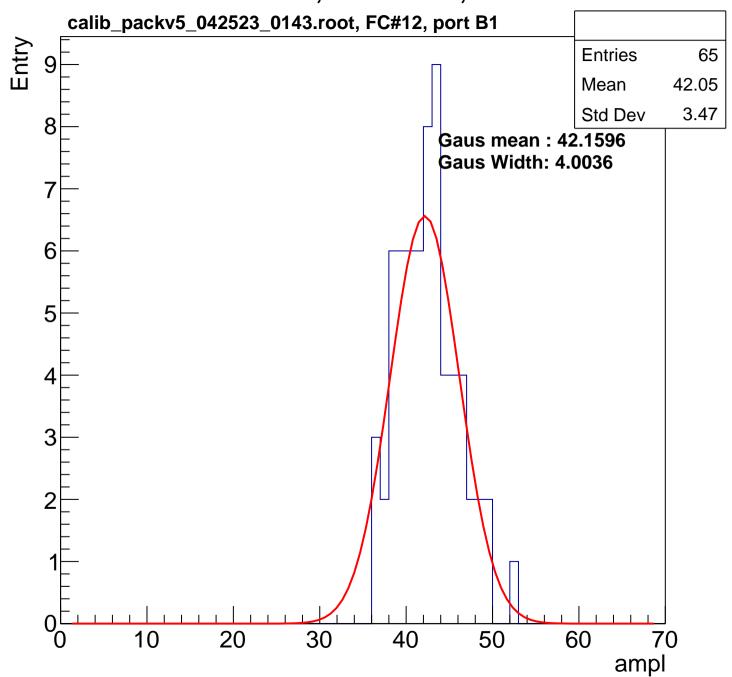


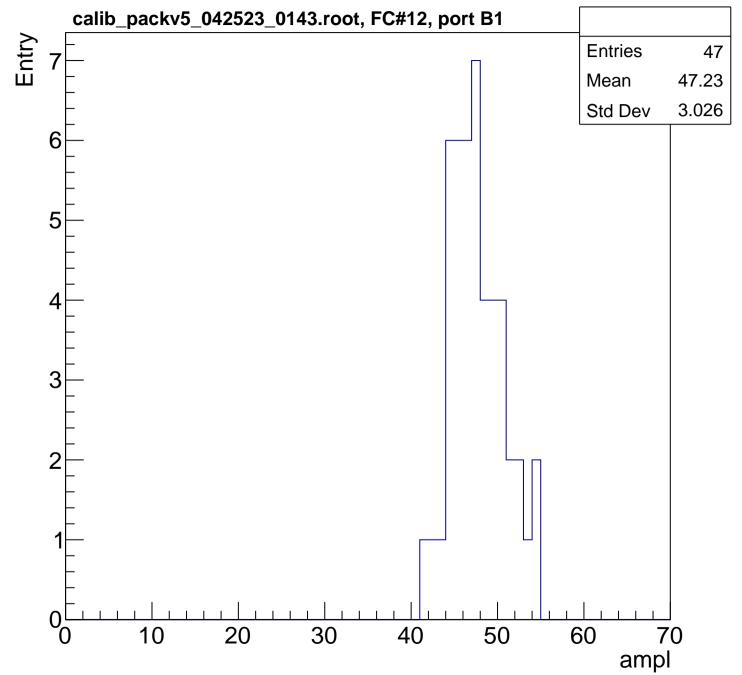


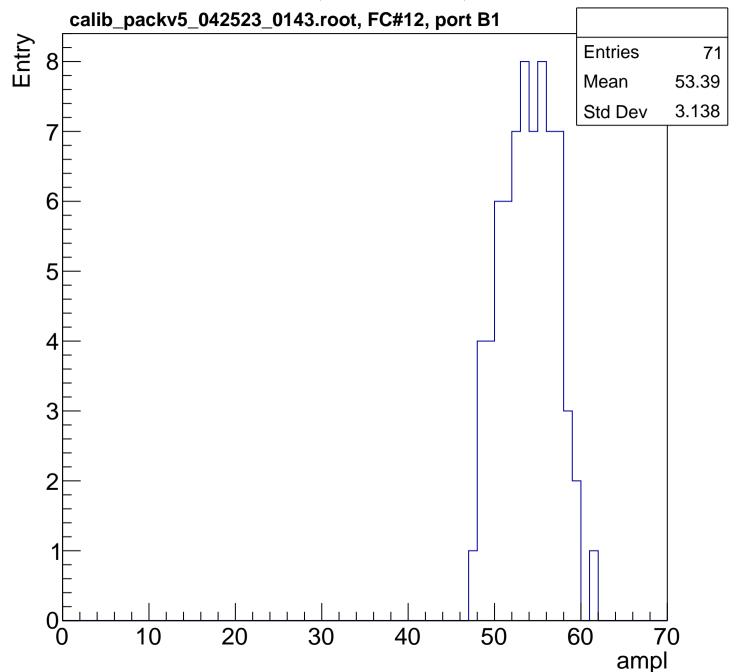


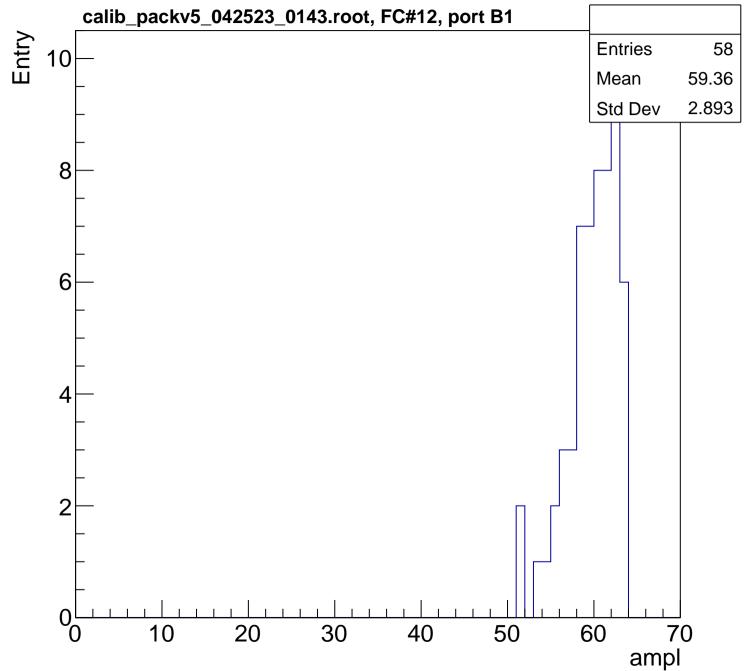


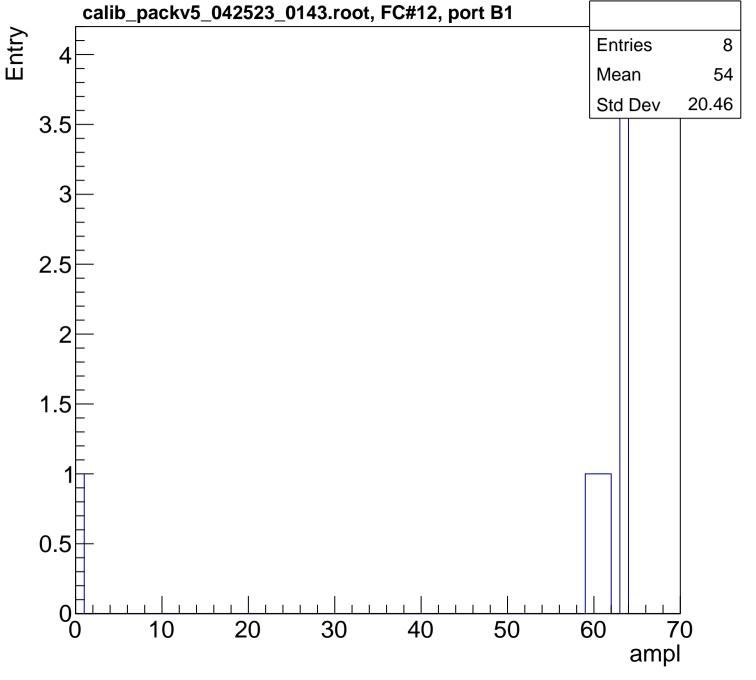


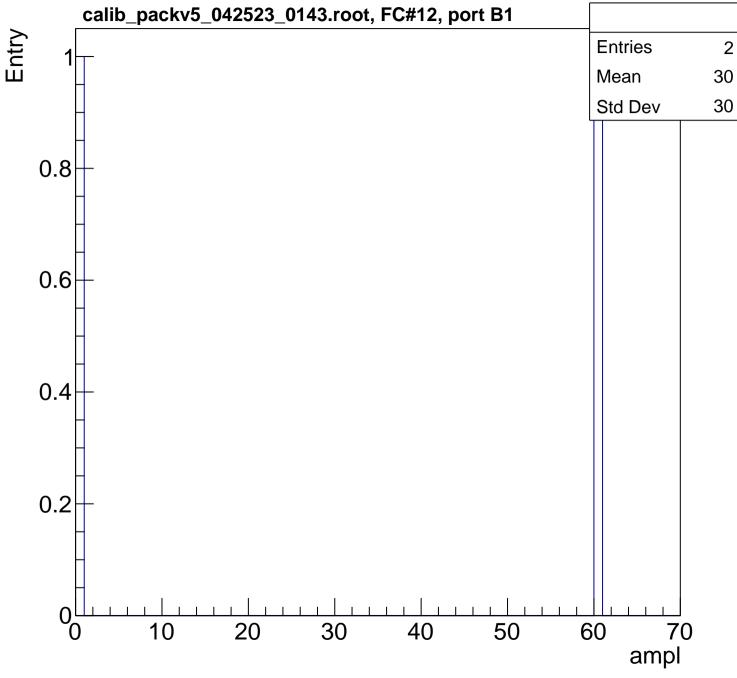


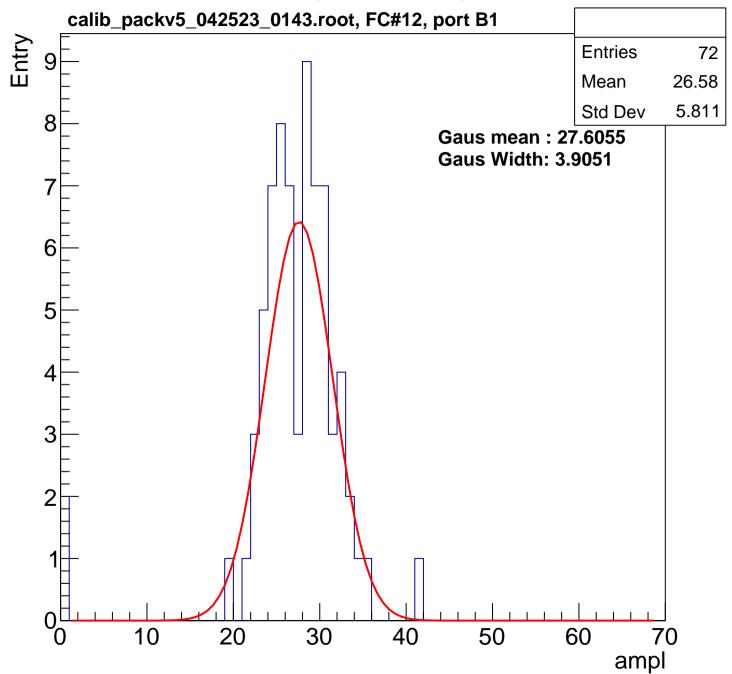


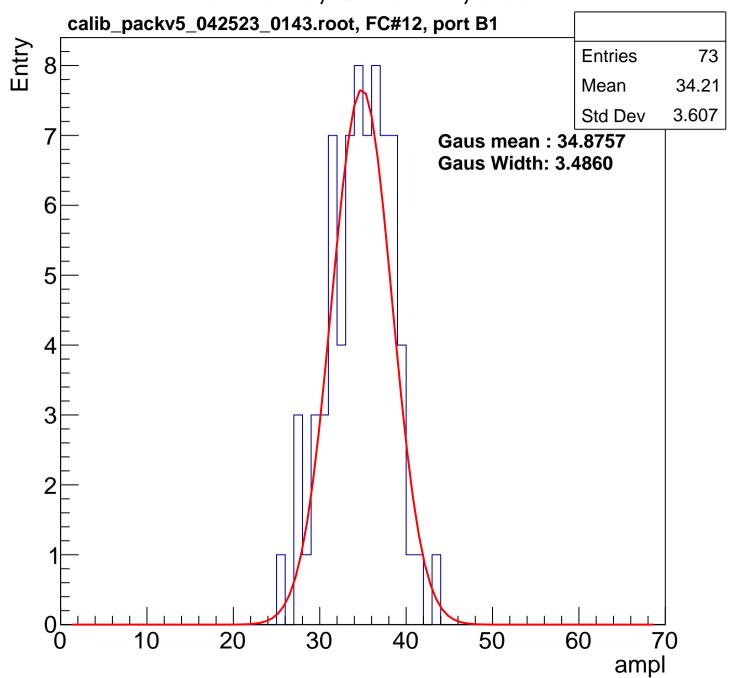


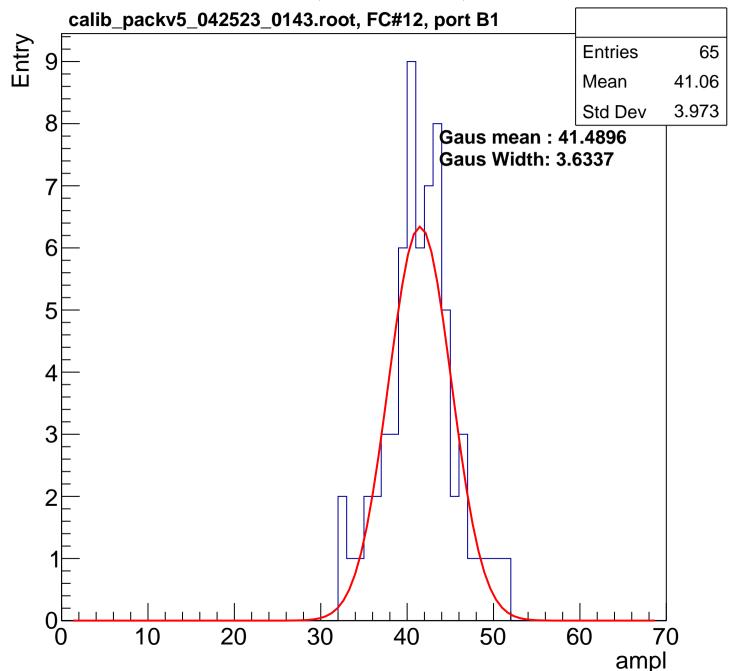


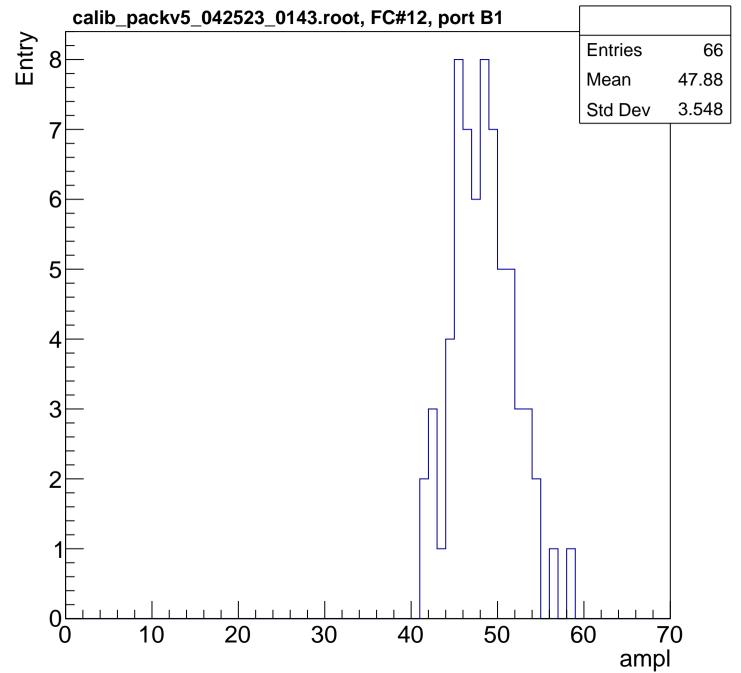


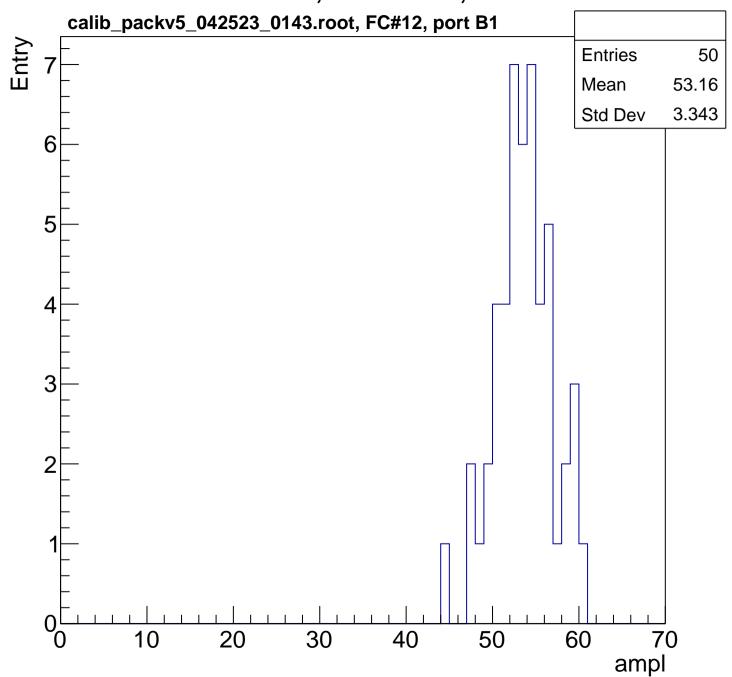


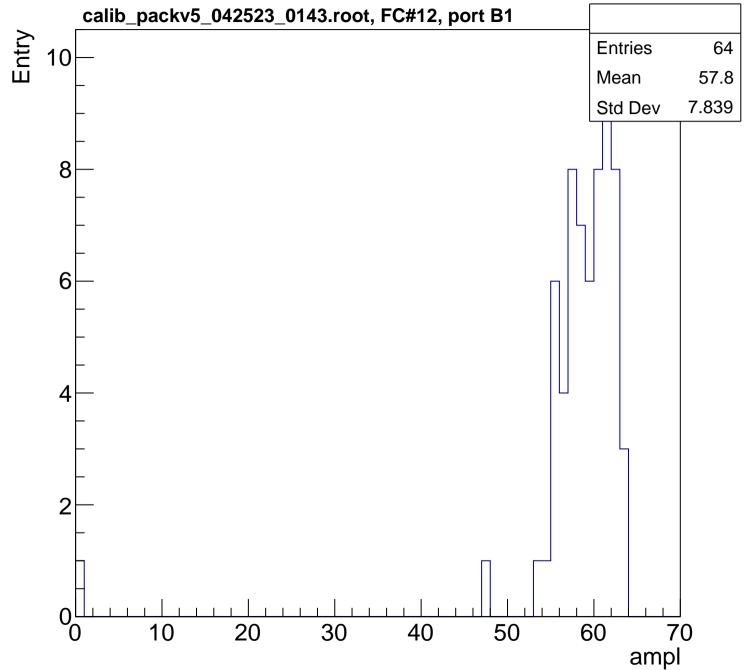


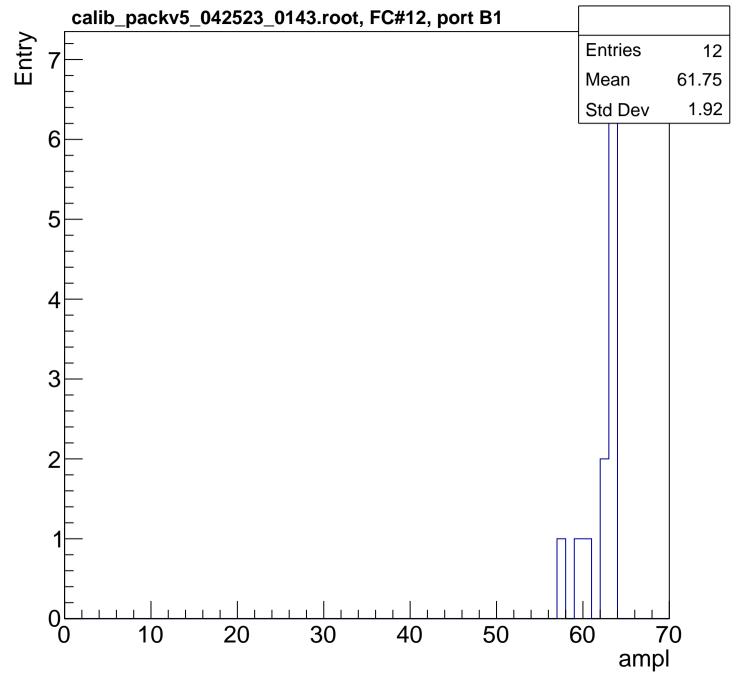


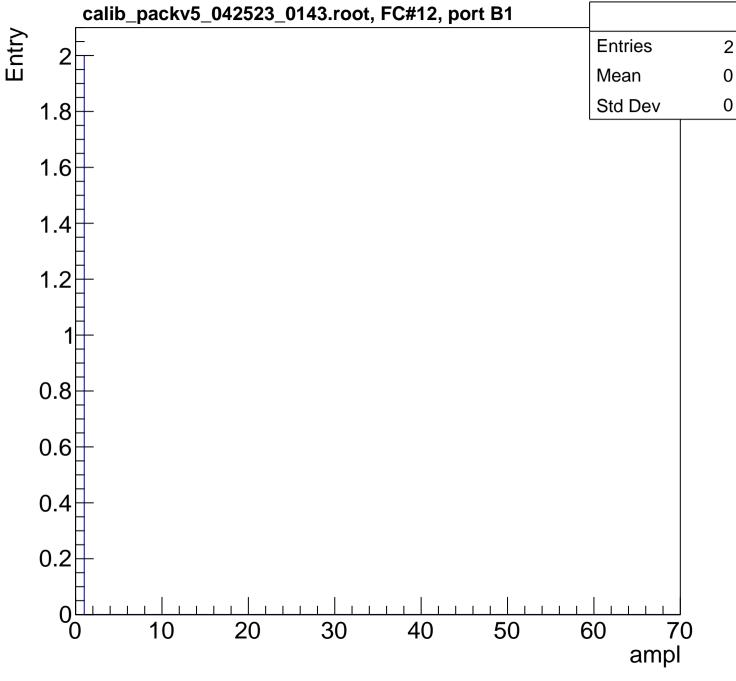


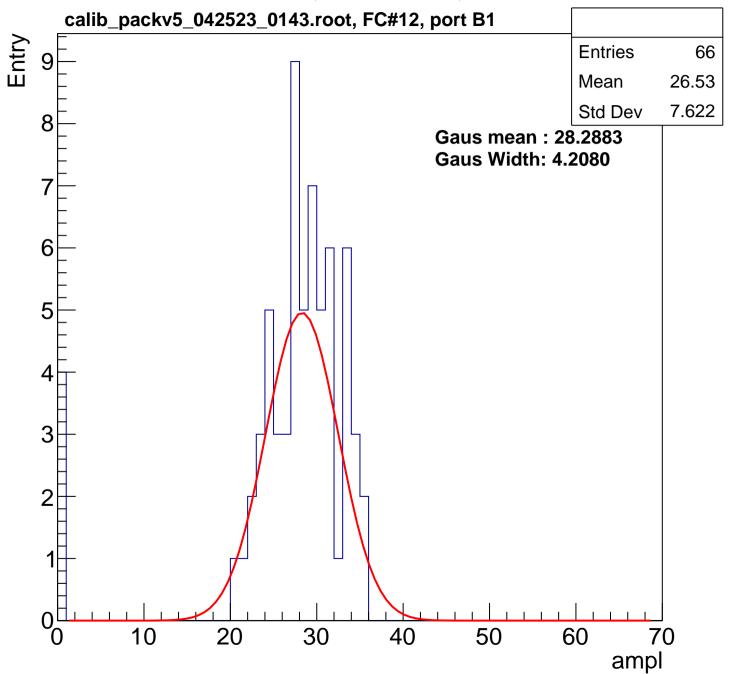


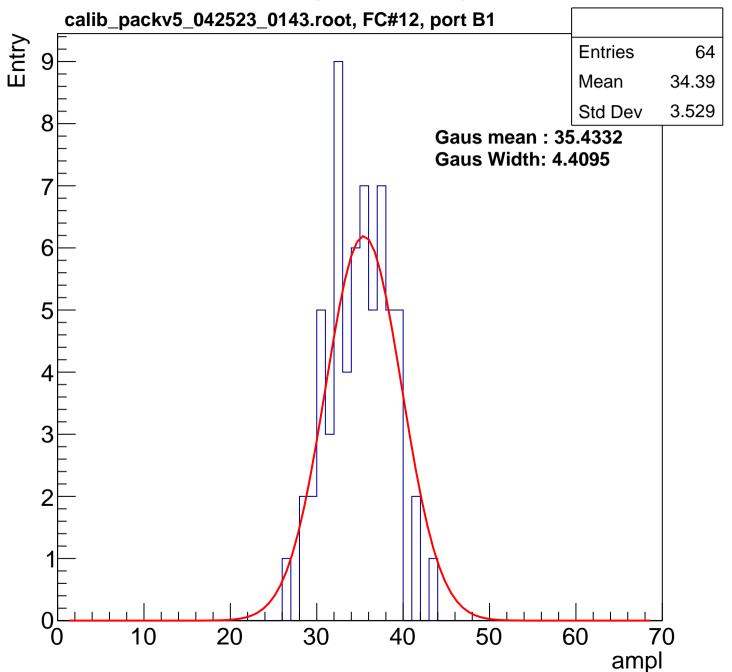


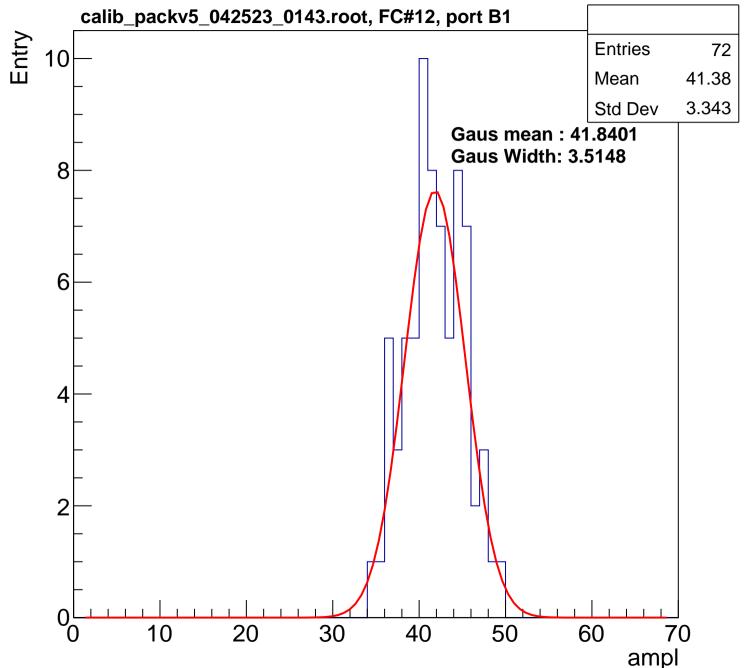


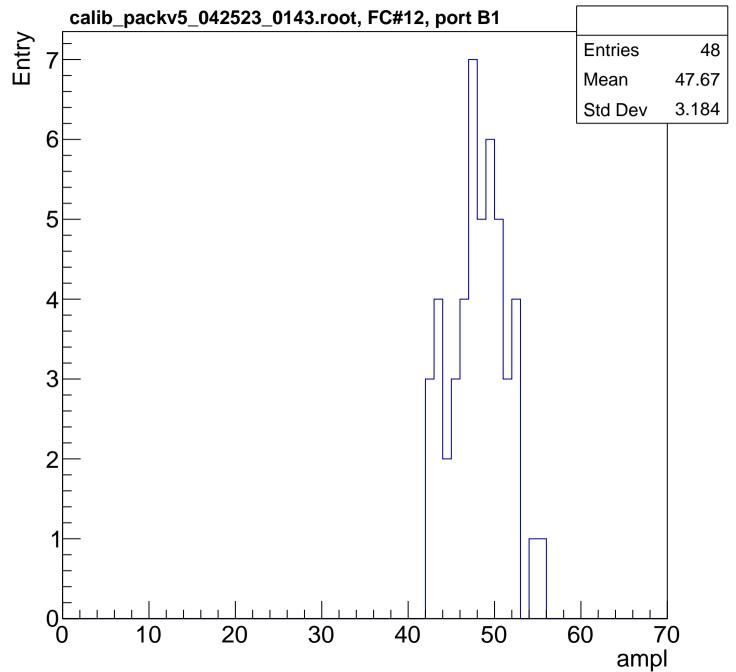


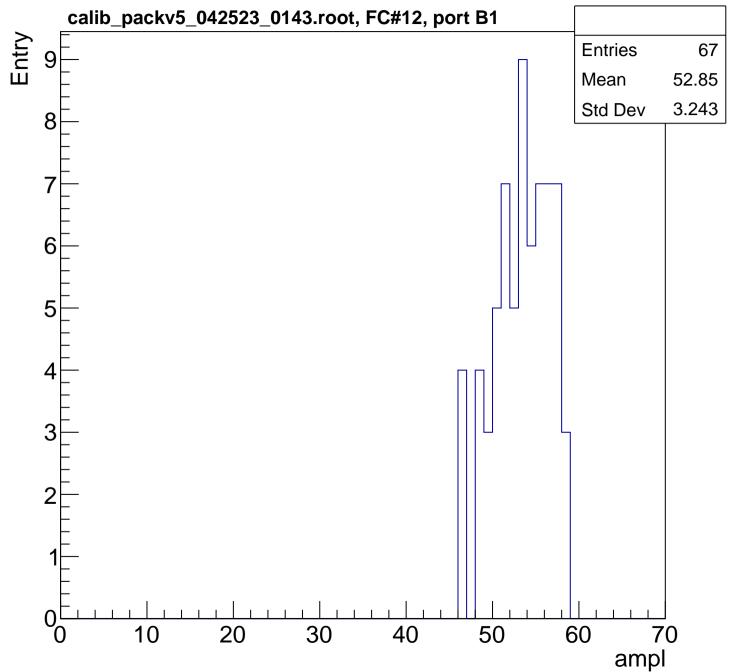


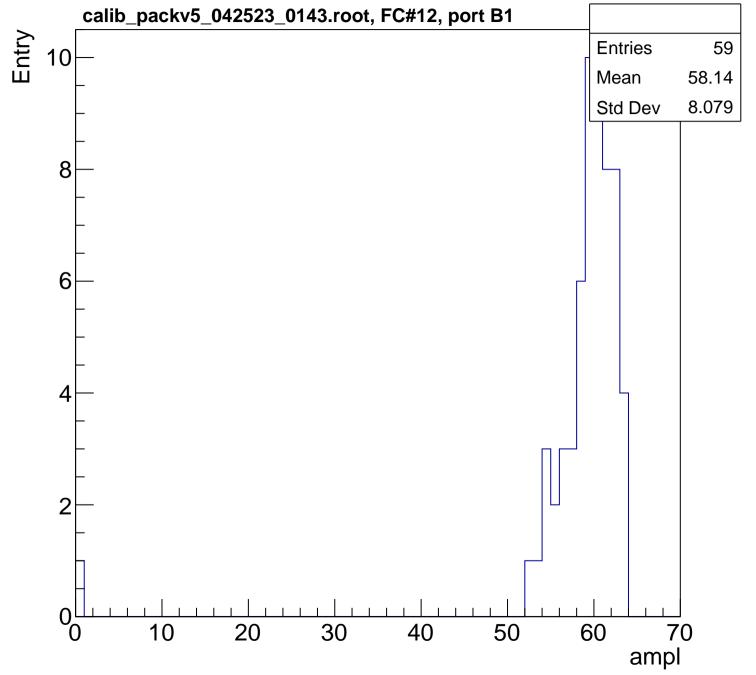


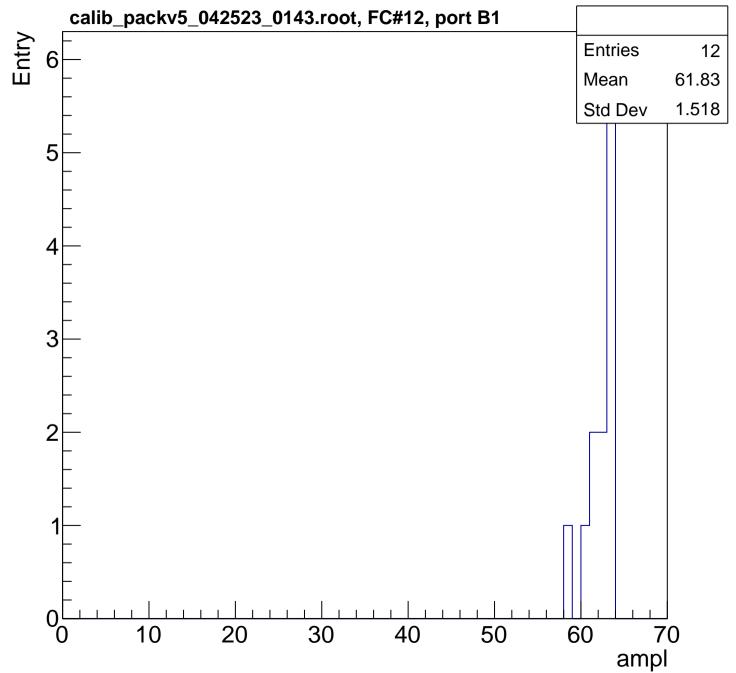


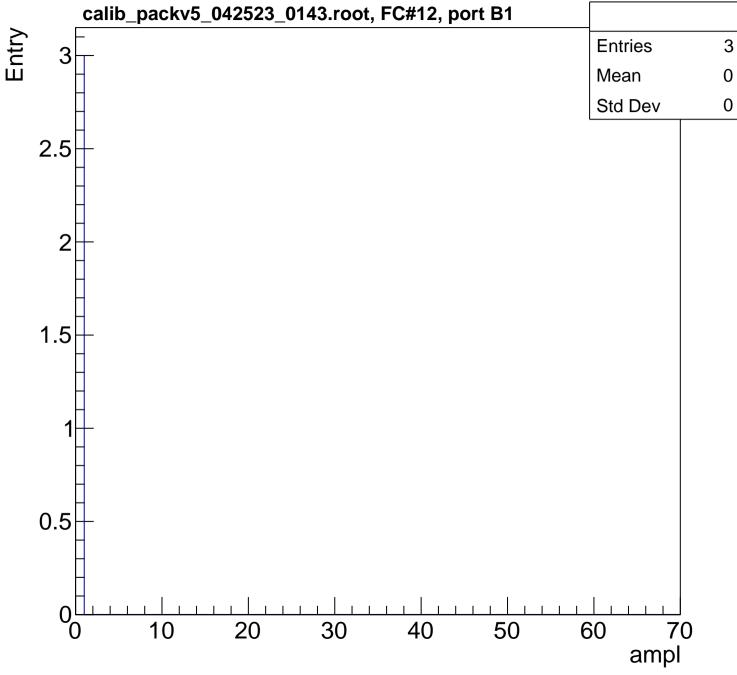


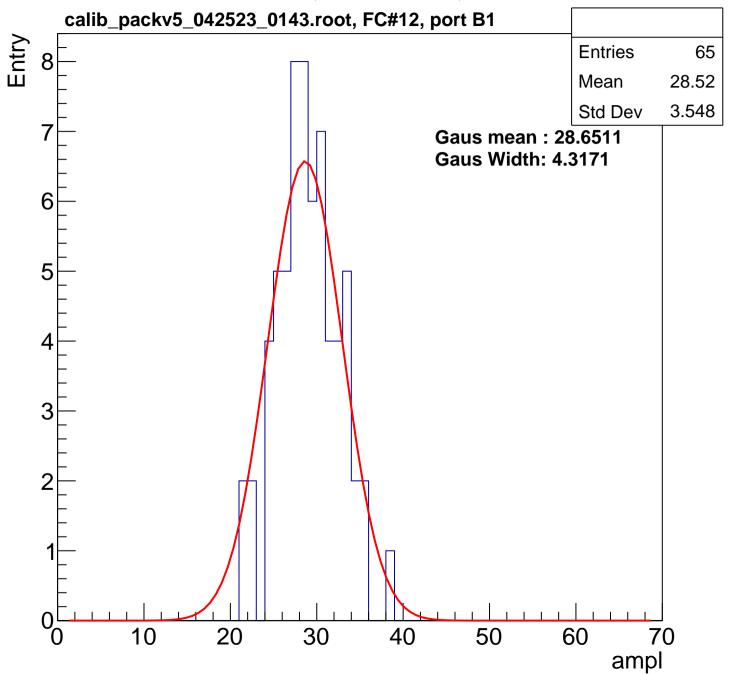


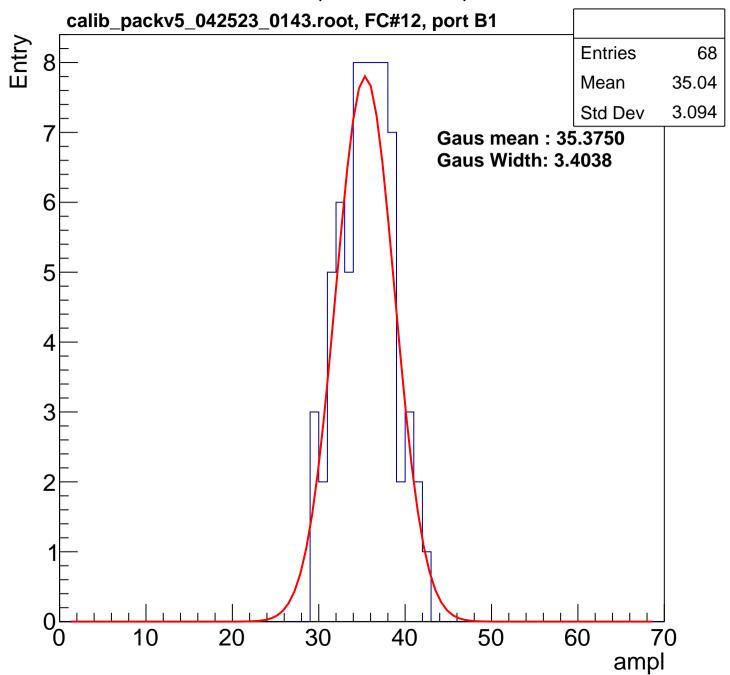


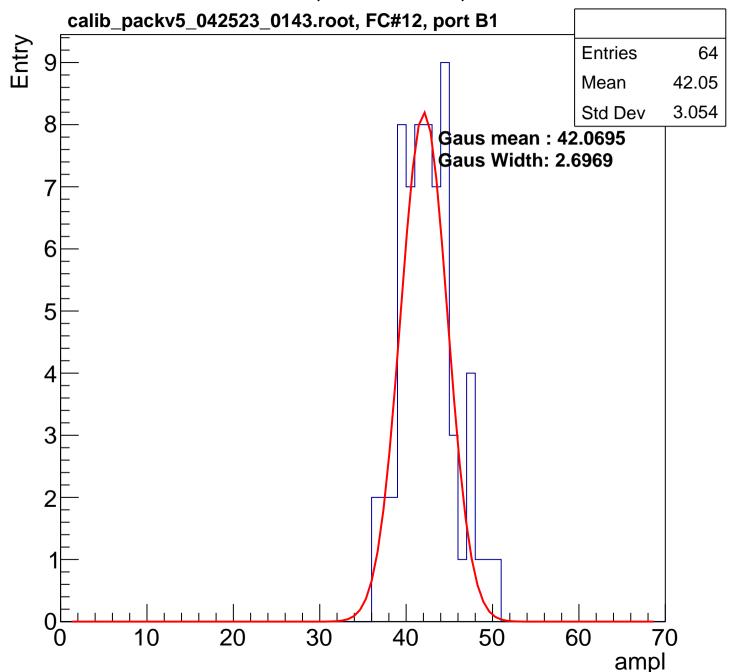


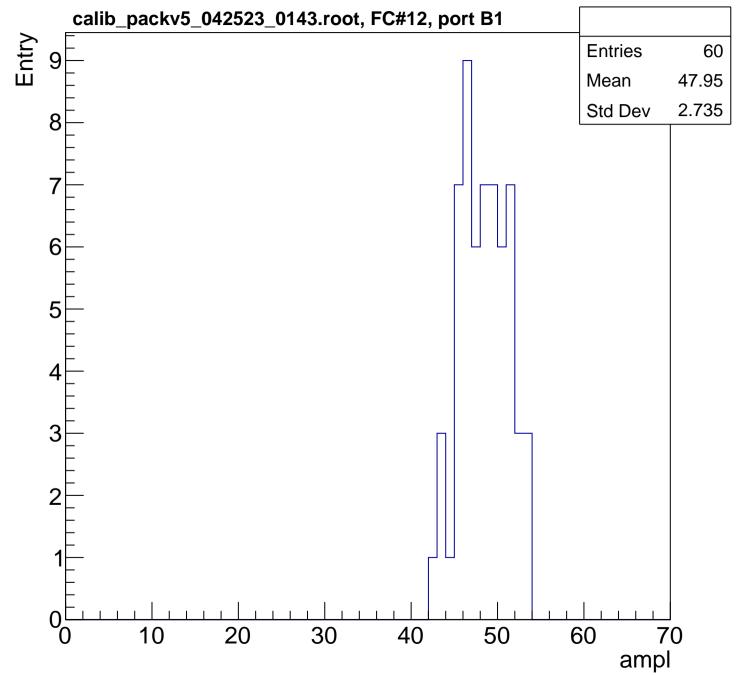


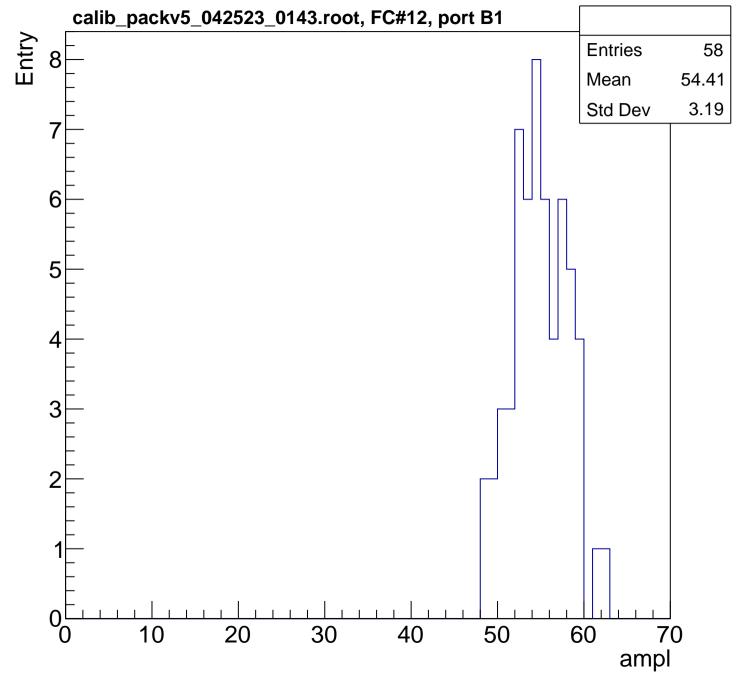


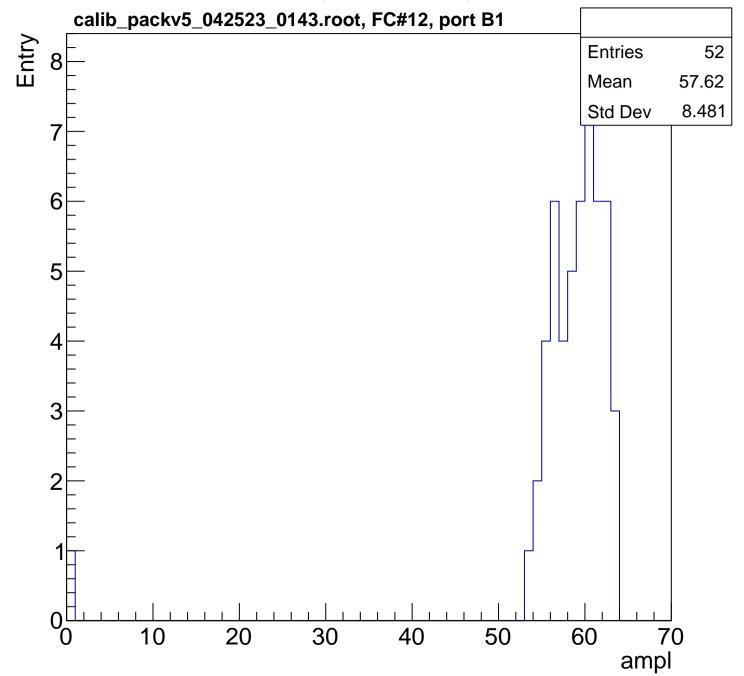


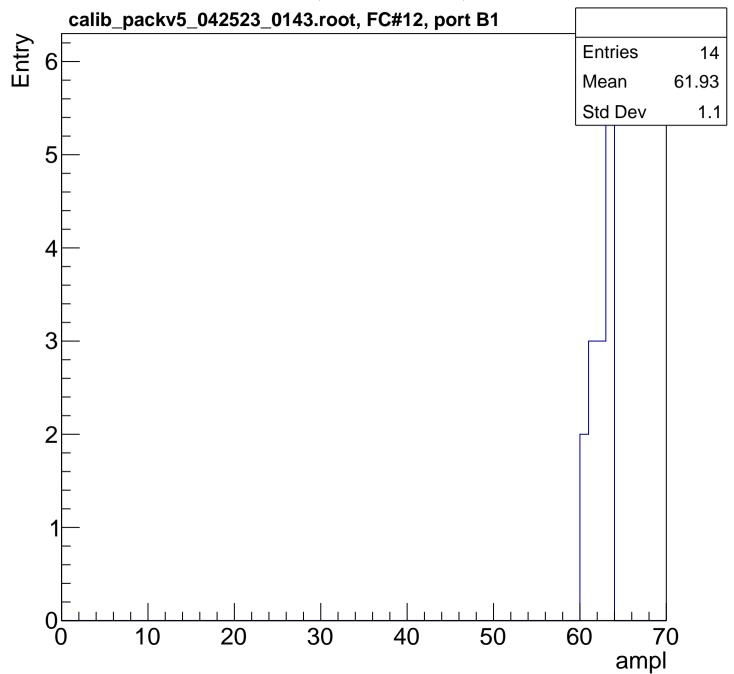




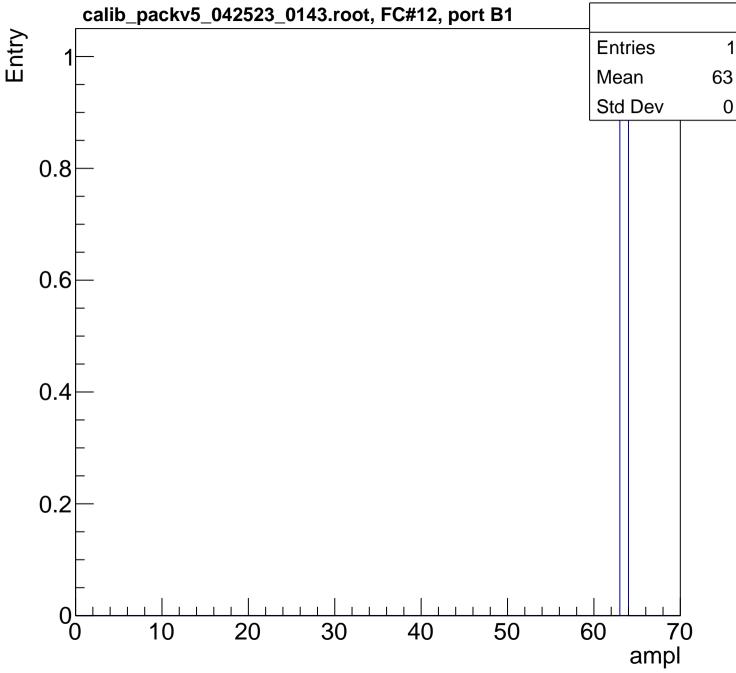


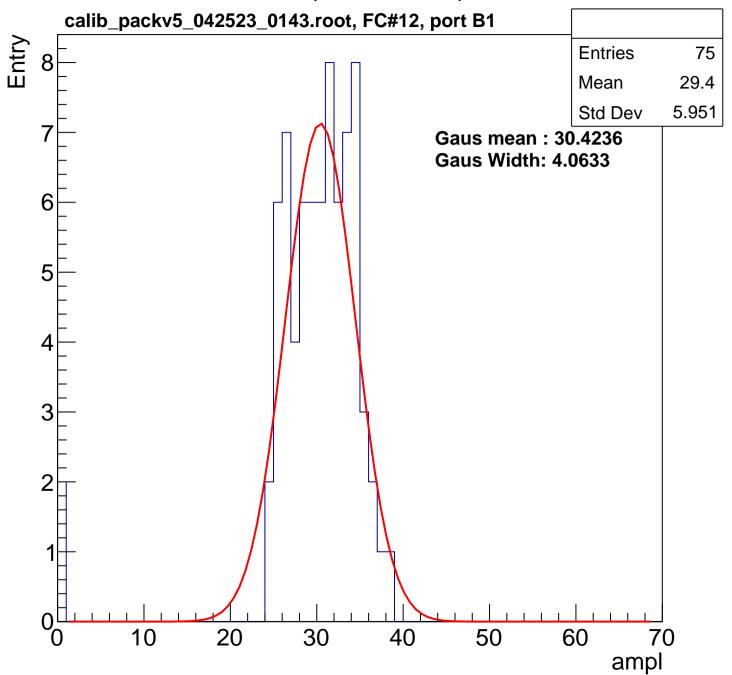


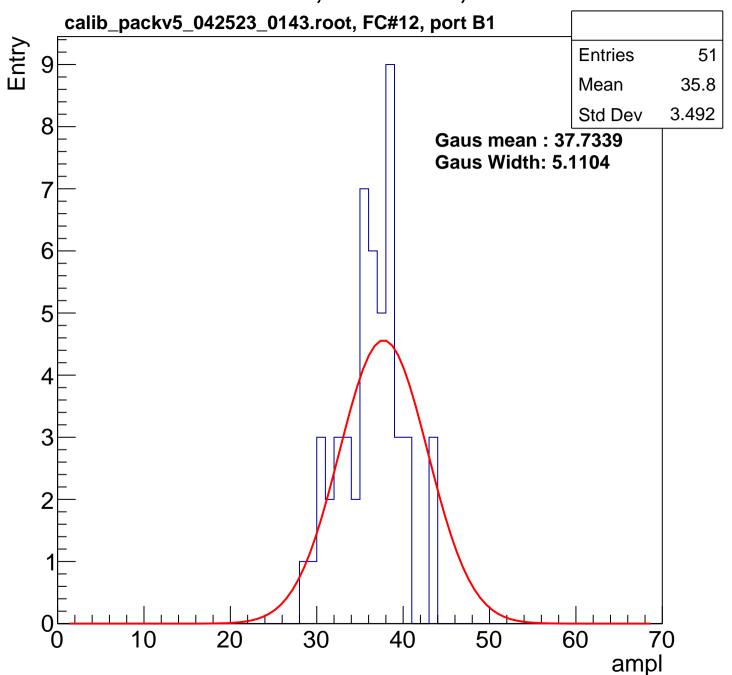


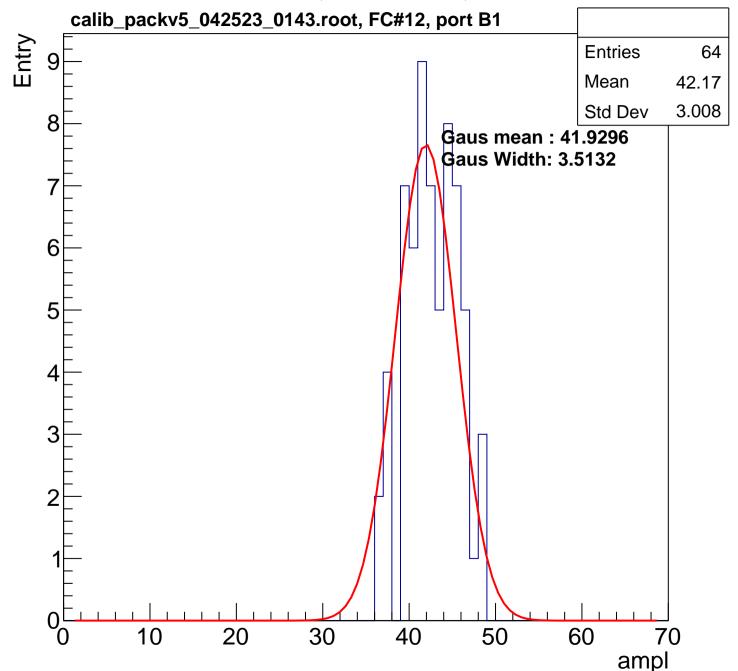


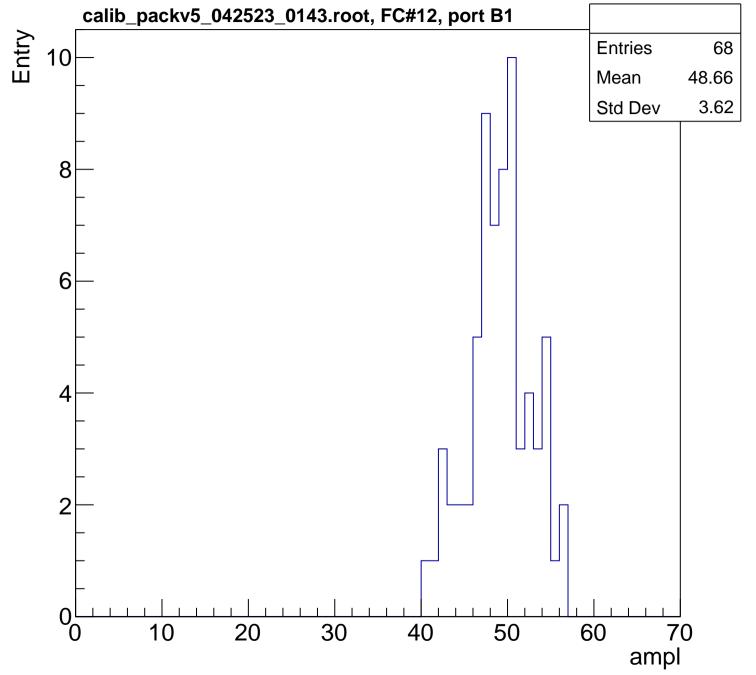
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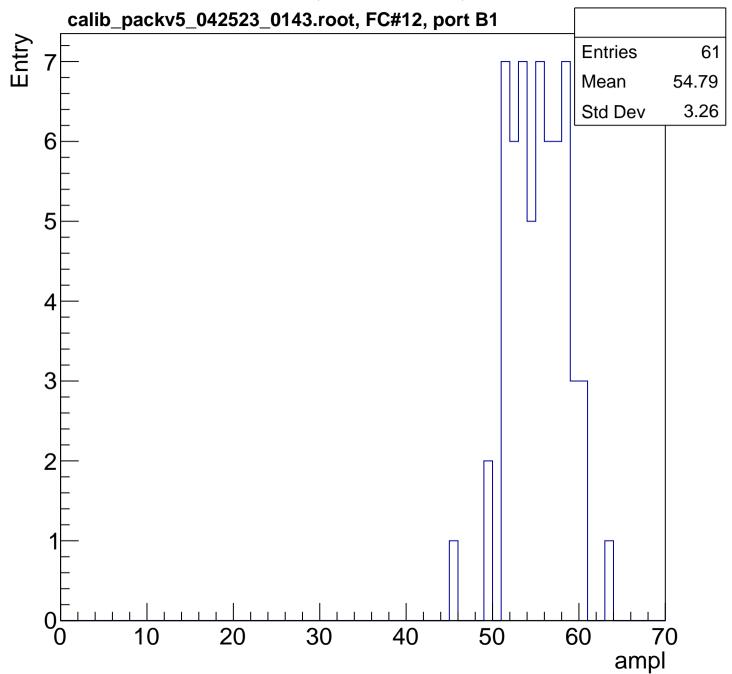


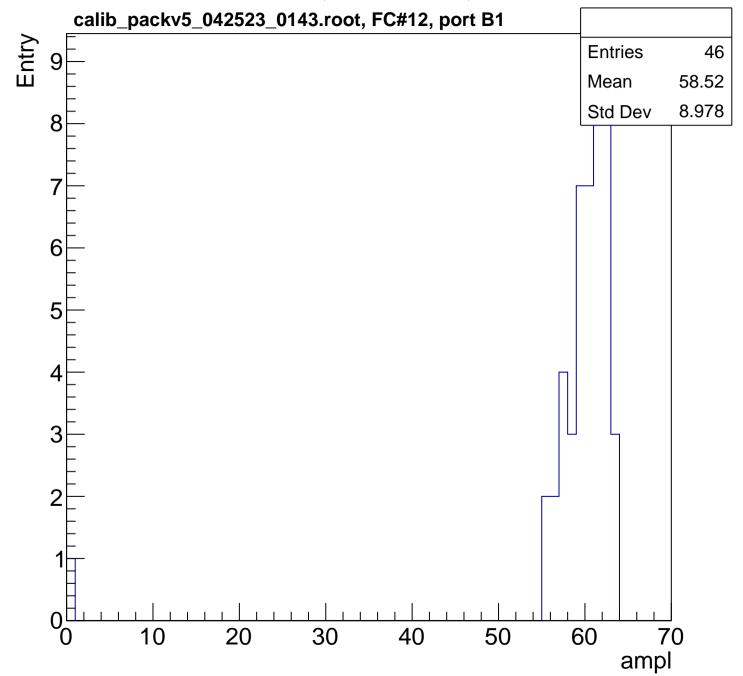


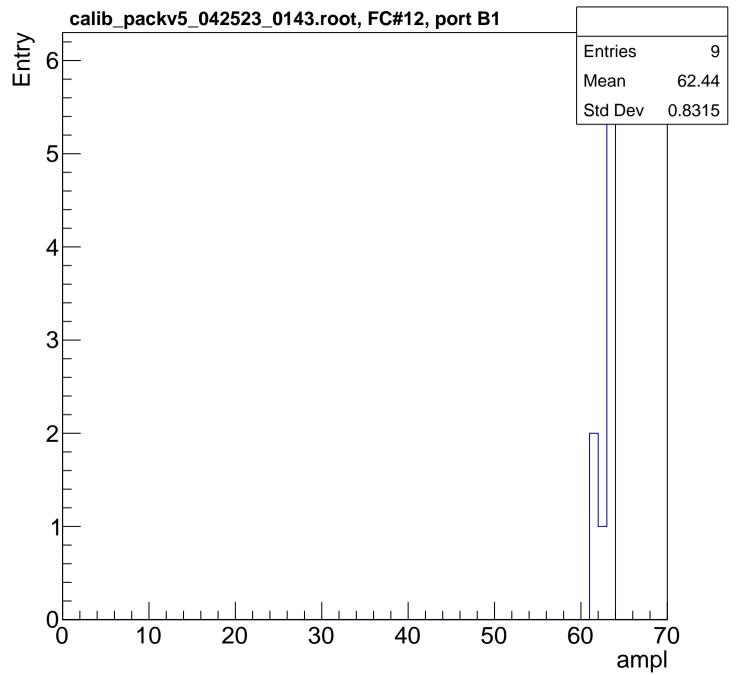




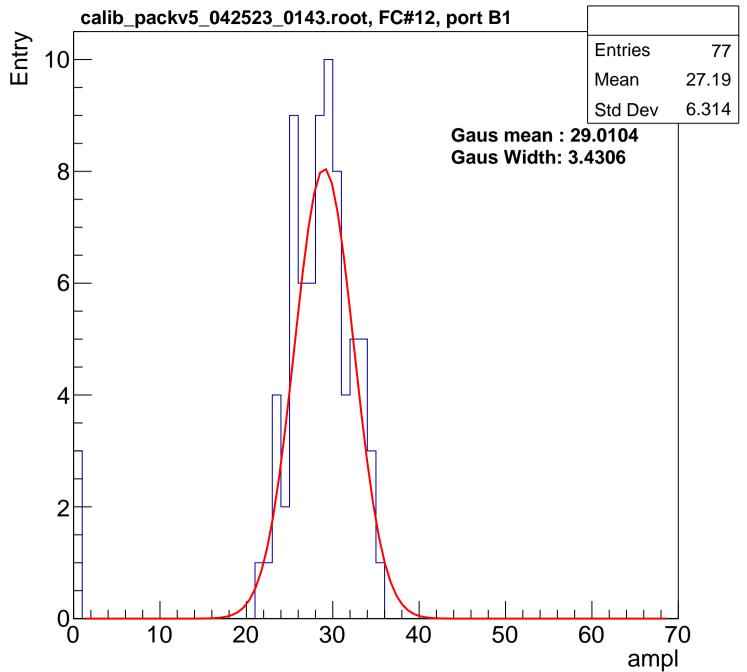


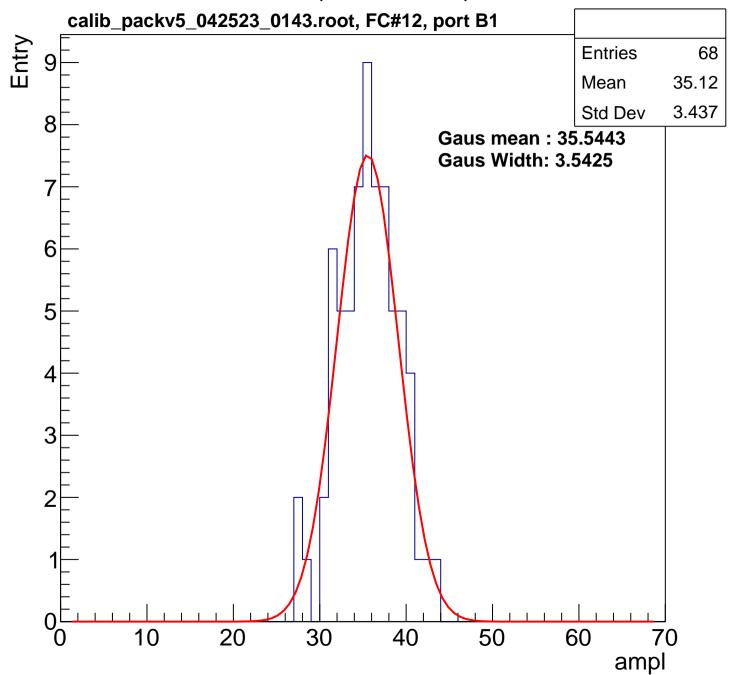


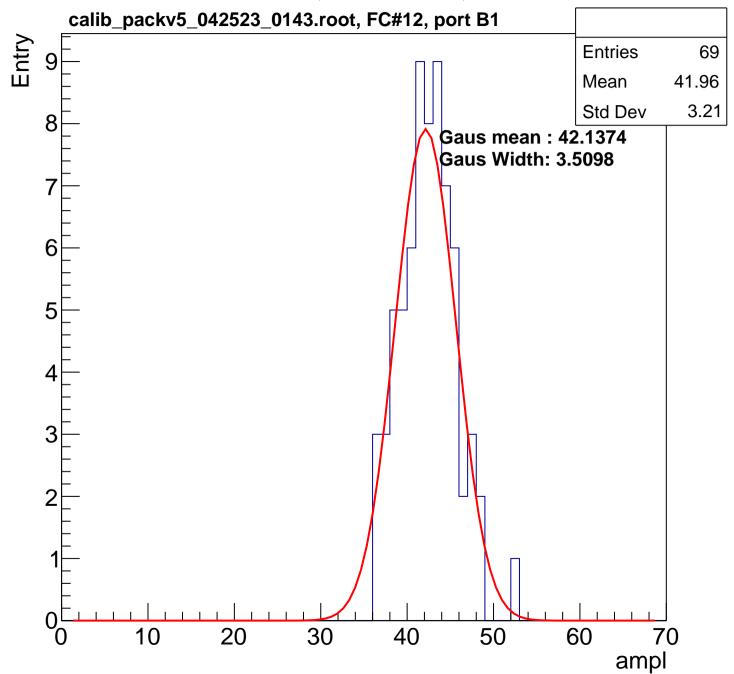


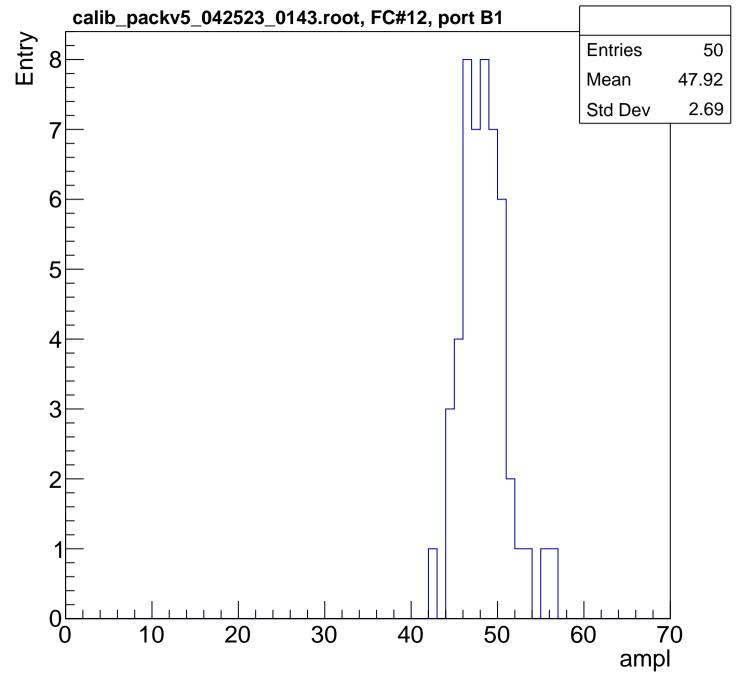


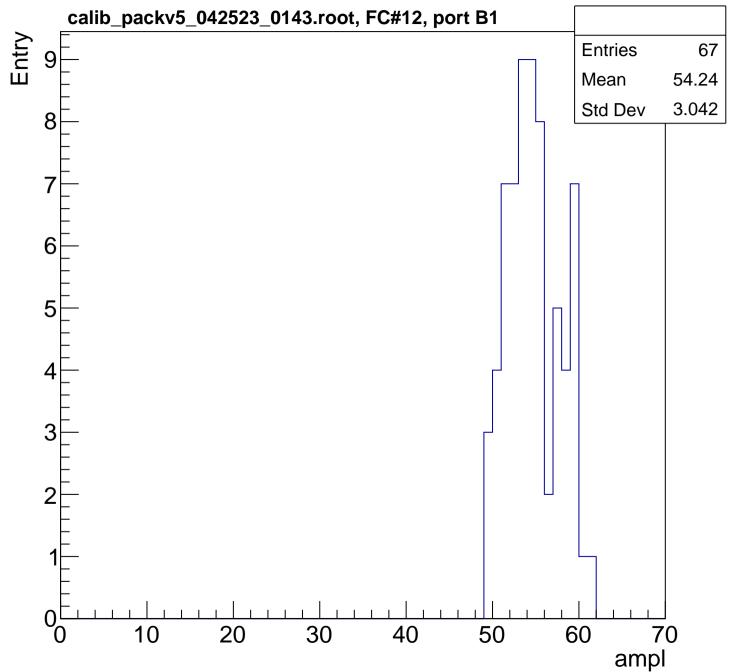


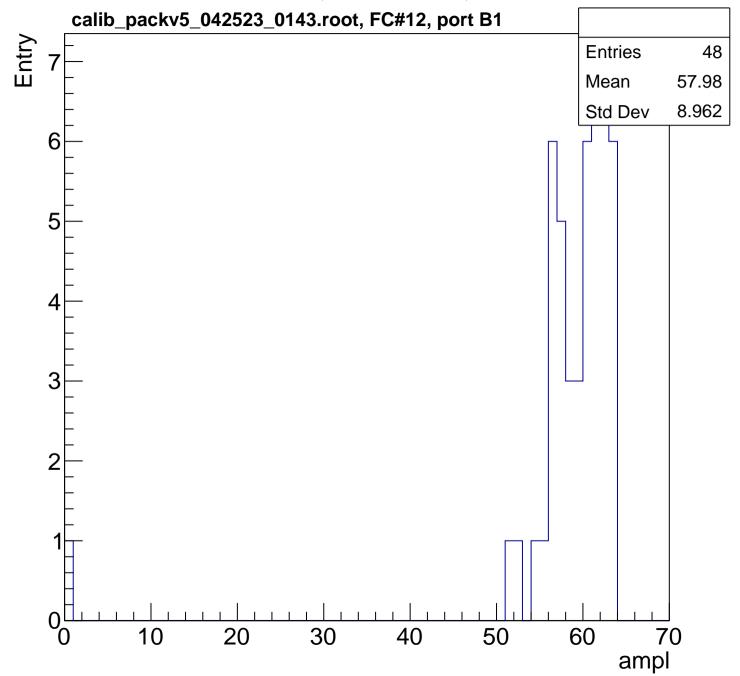


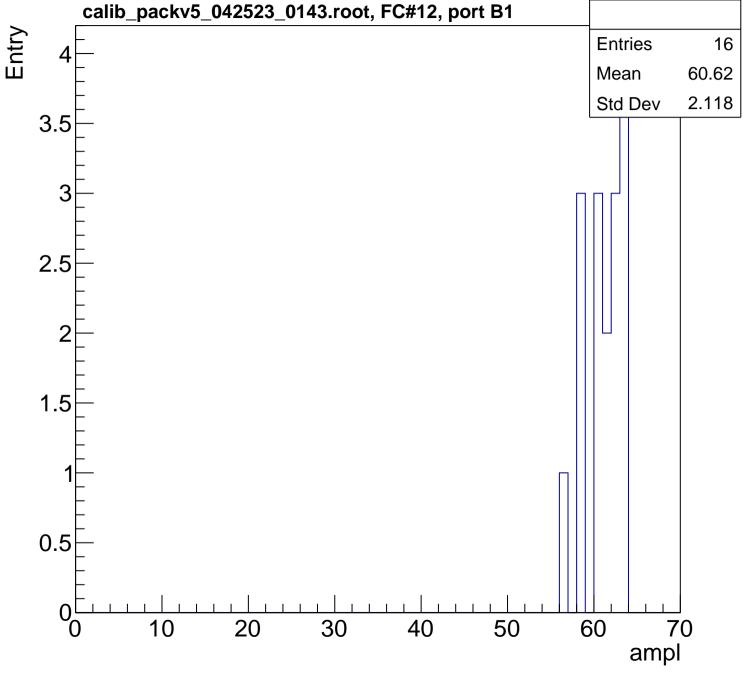




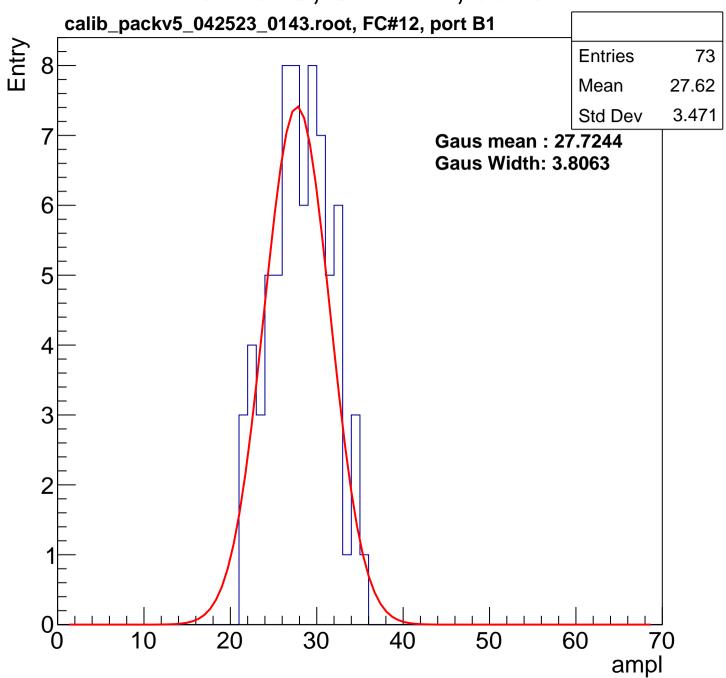


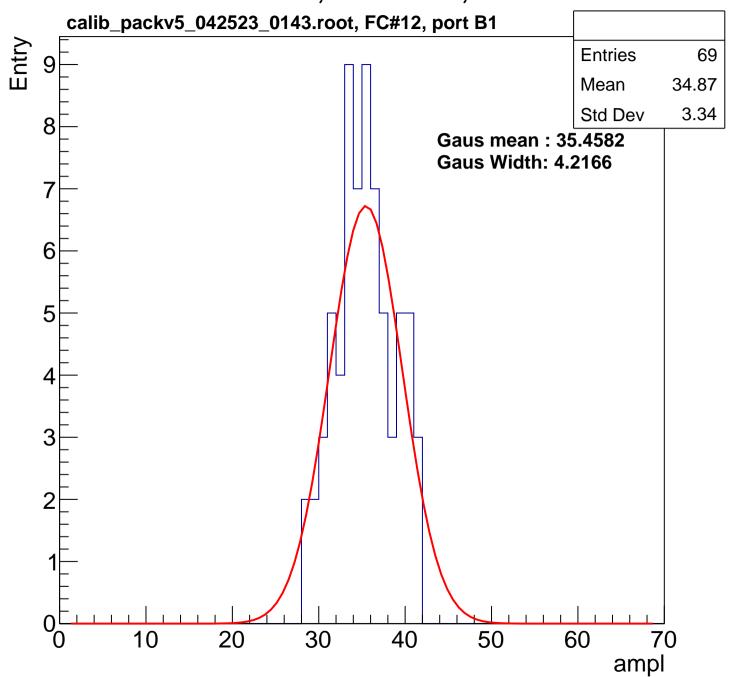


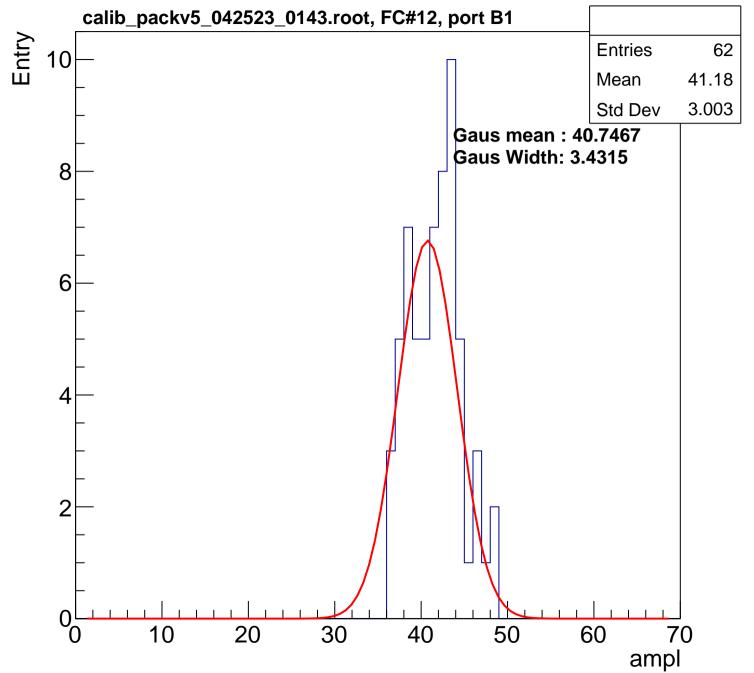


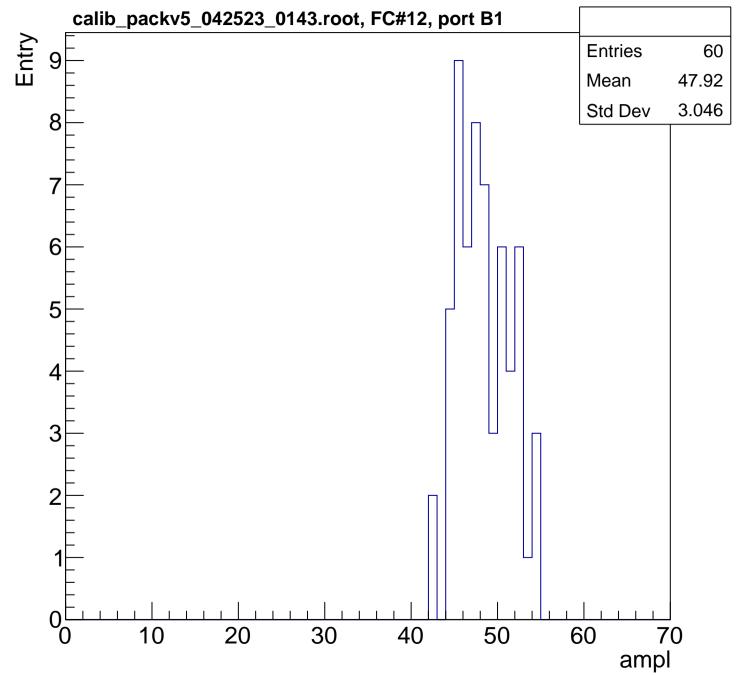


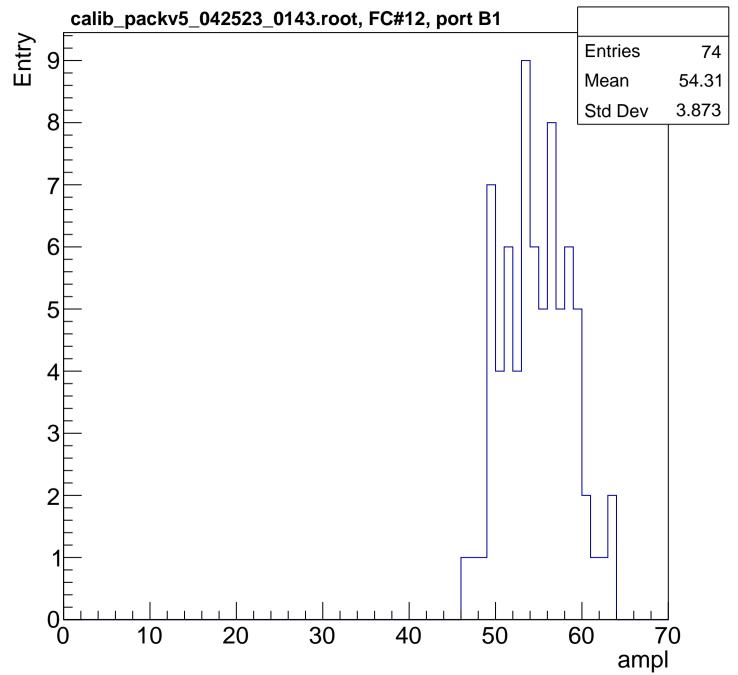
B0L102S, U2-ch16, adc7 calib_packv5_042523_0143.root, FC#12, port B1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

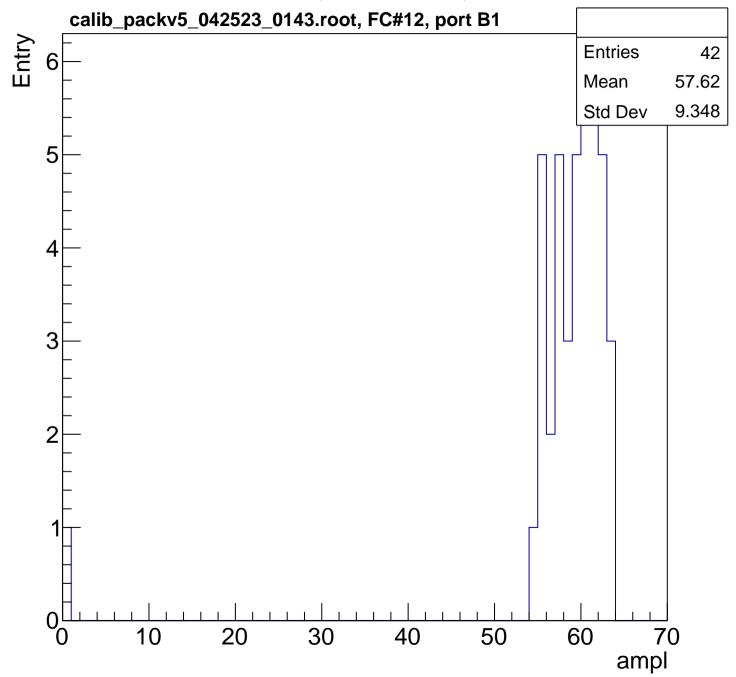


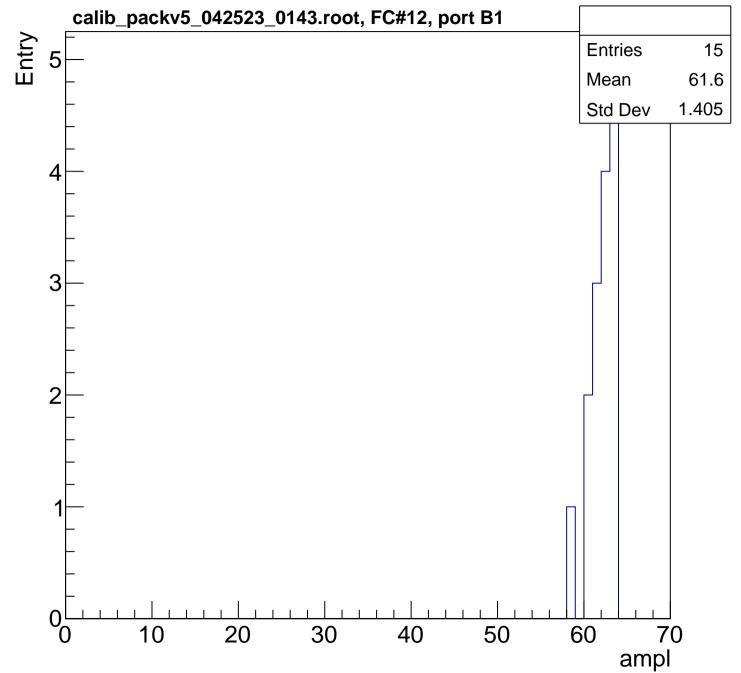


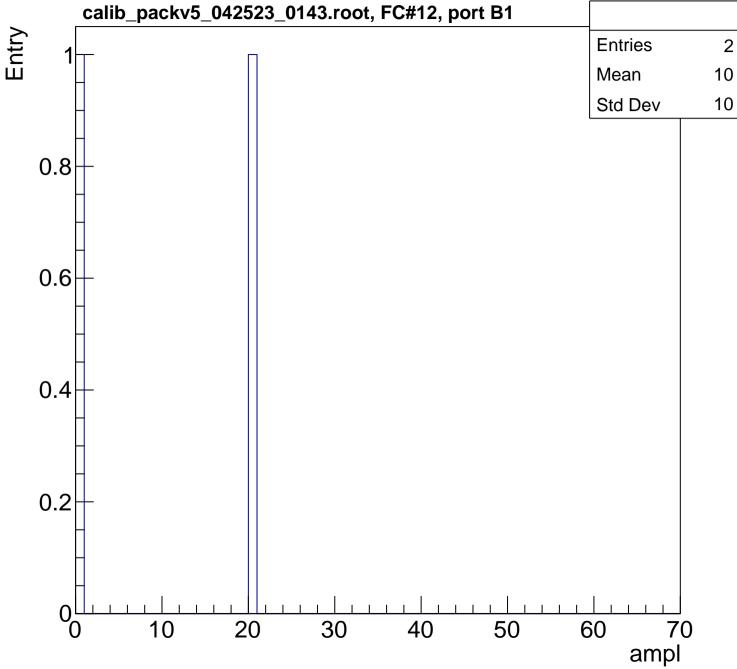


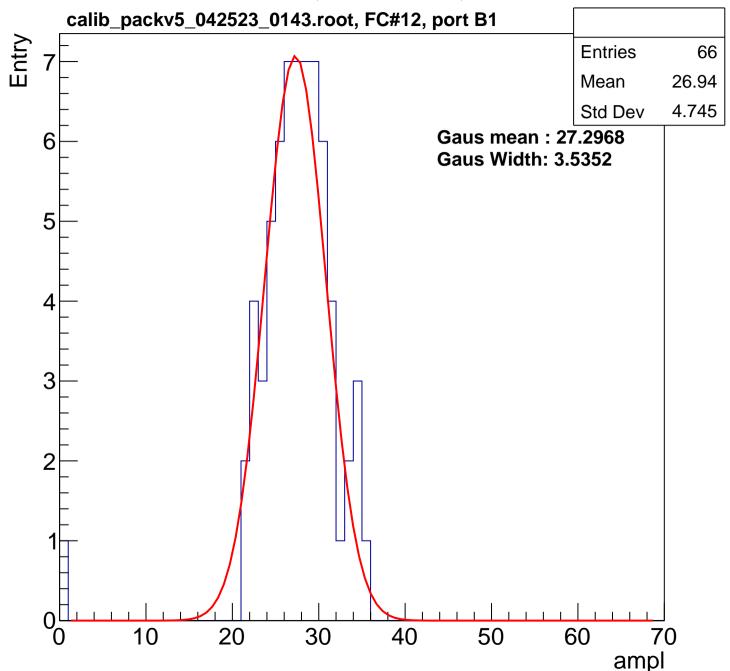


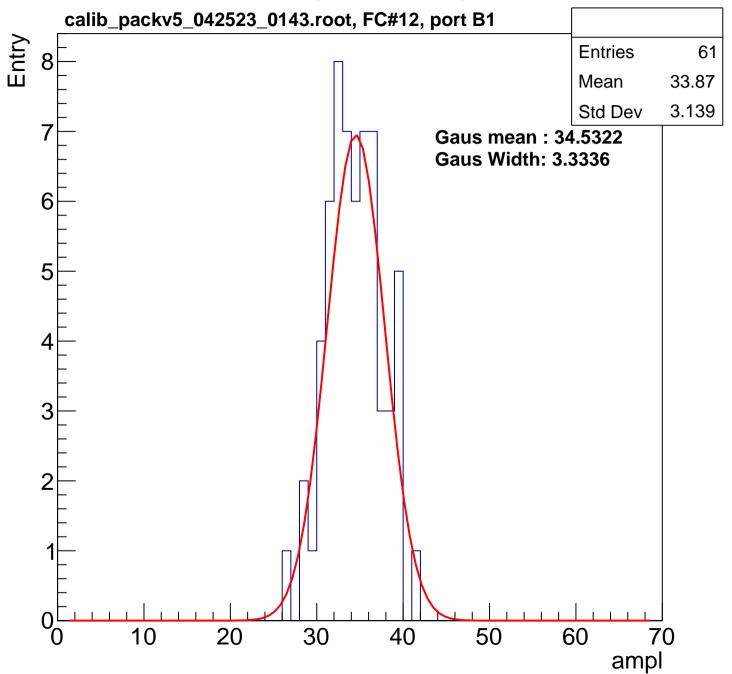


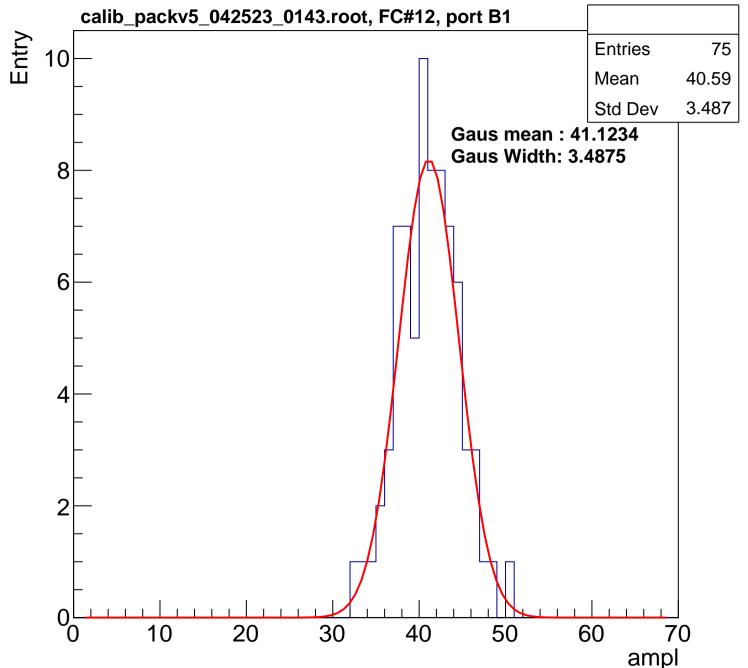


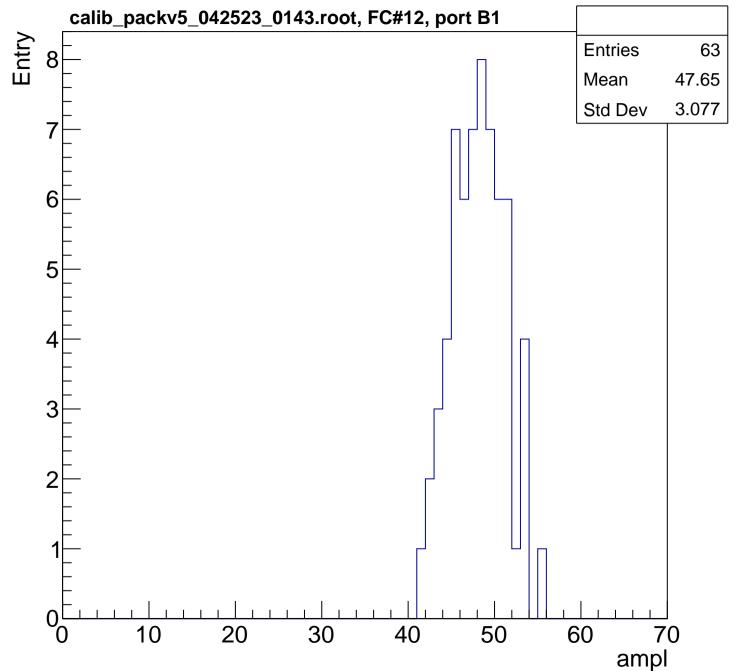


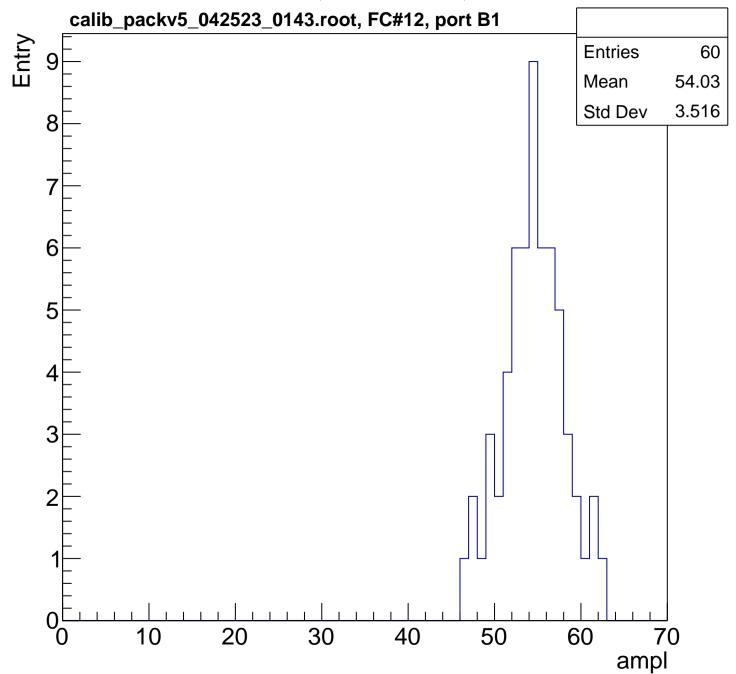


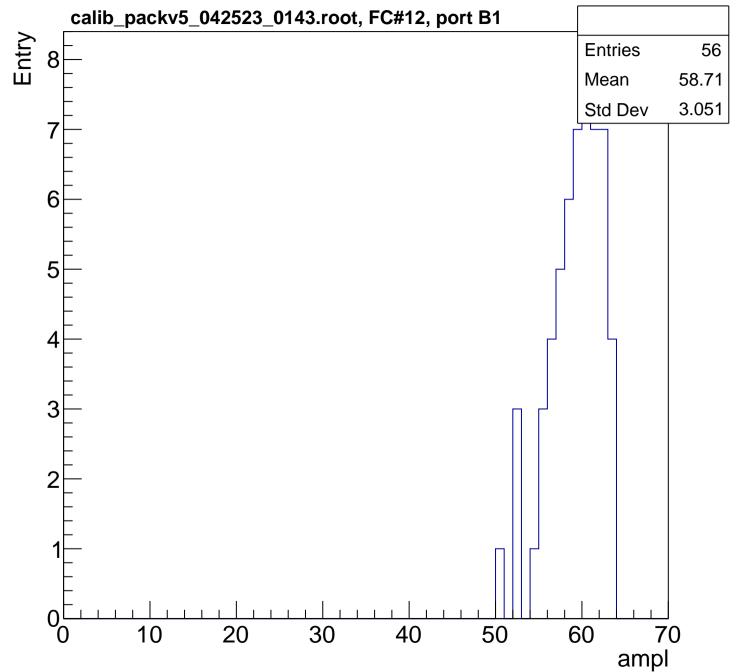


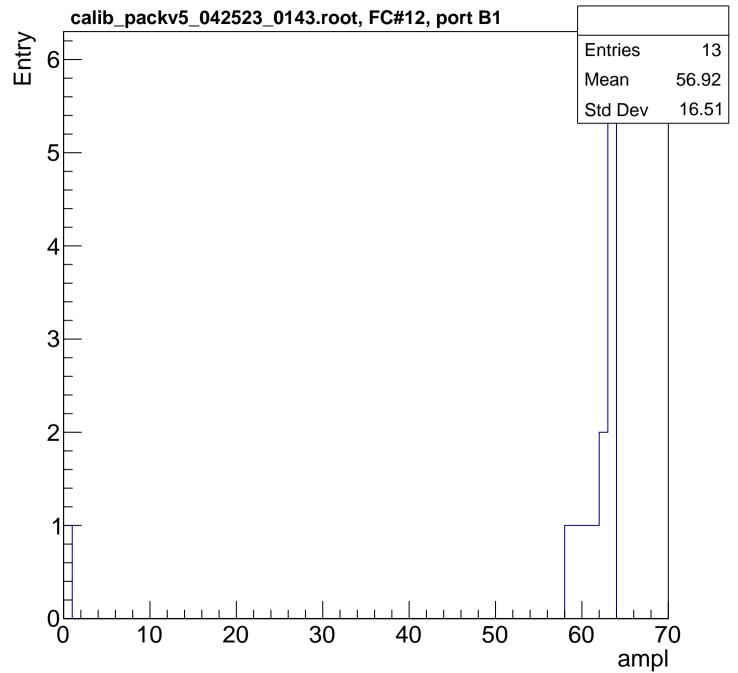


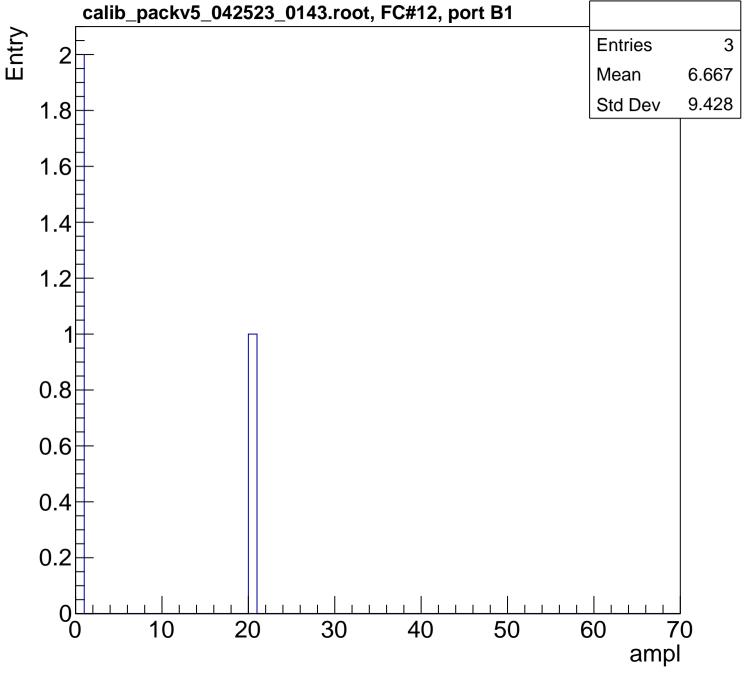


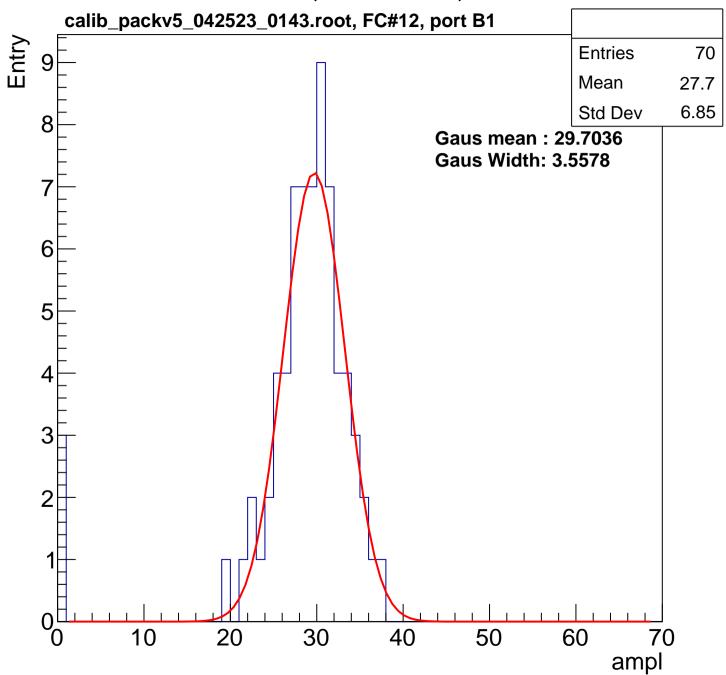


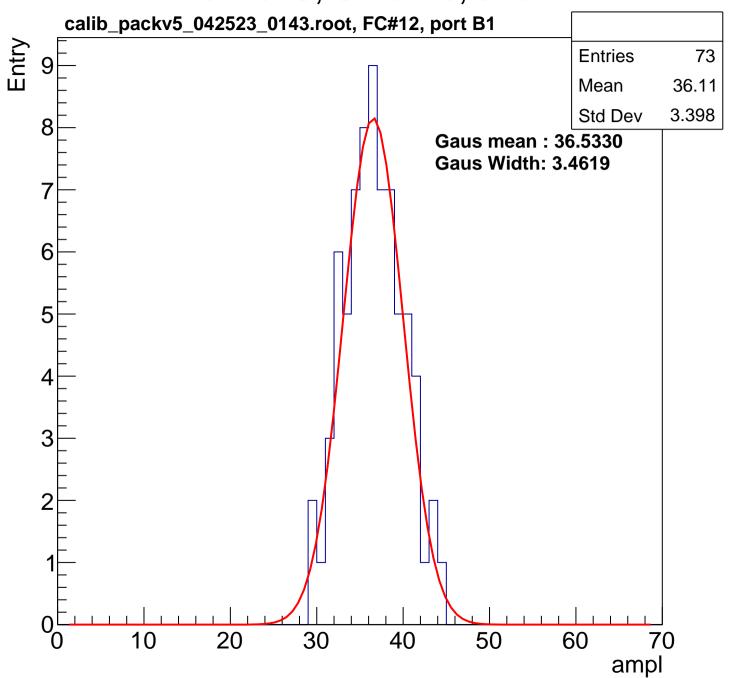


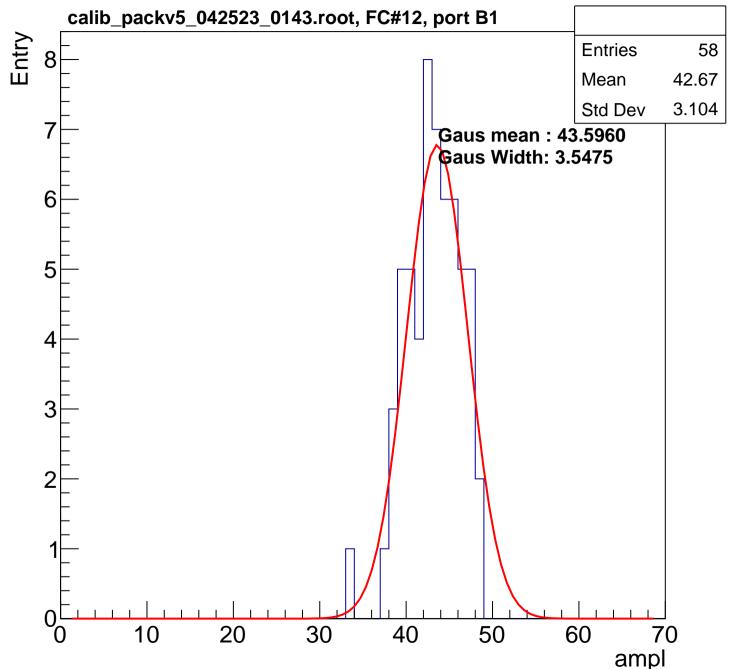


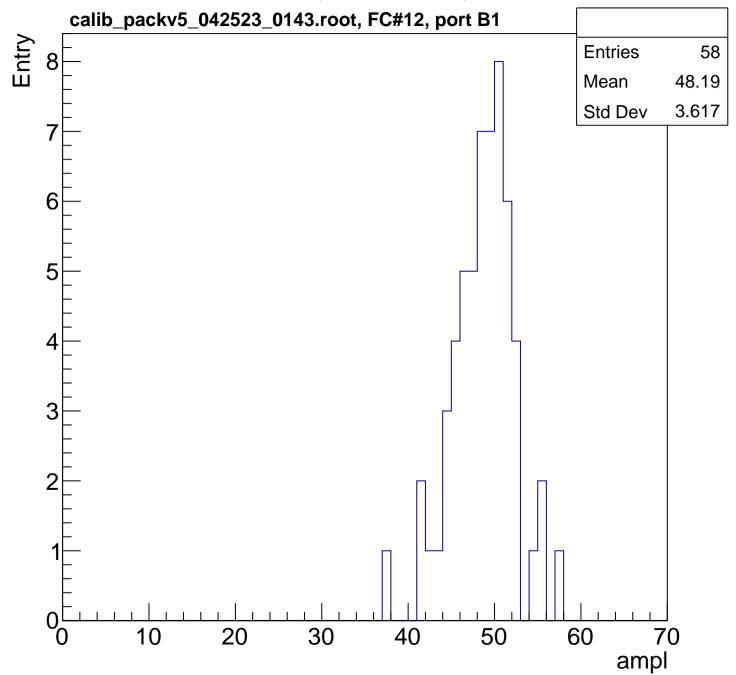


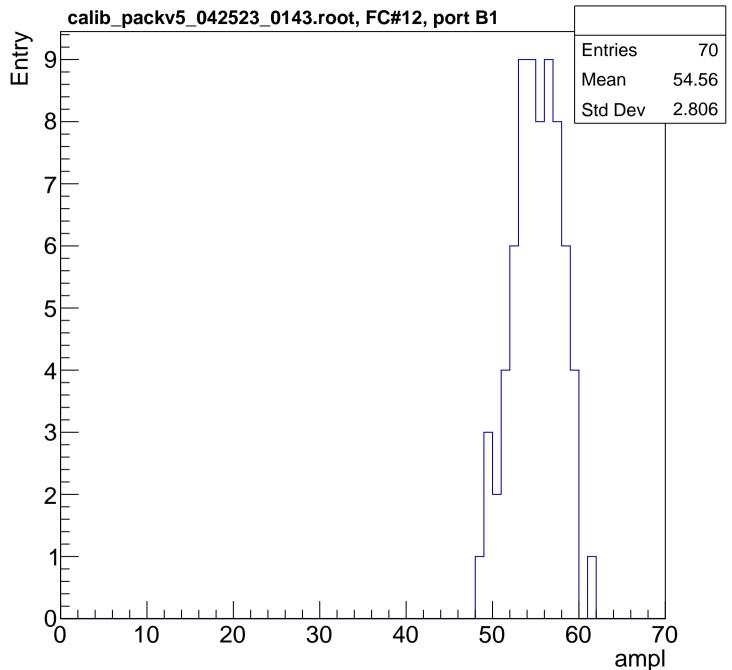


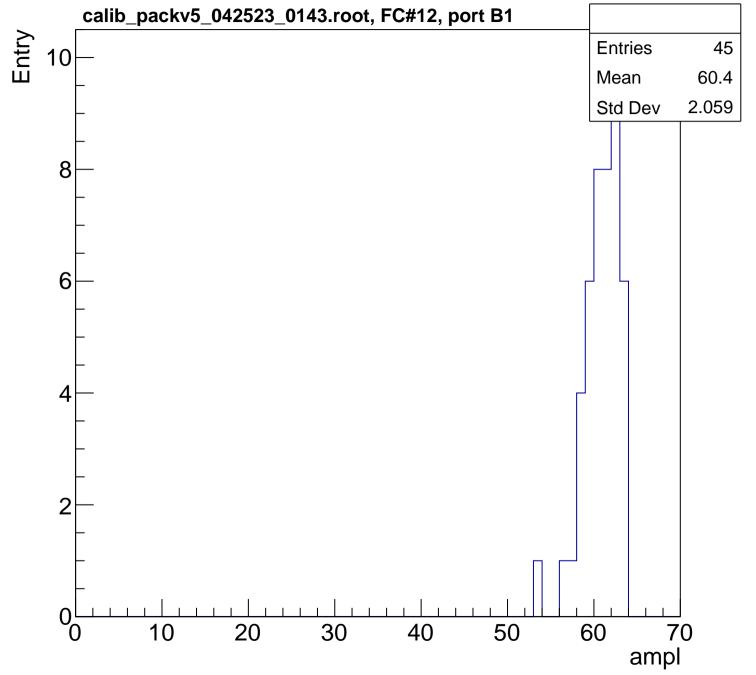


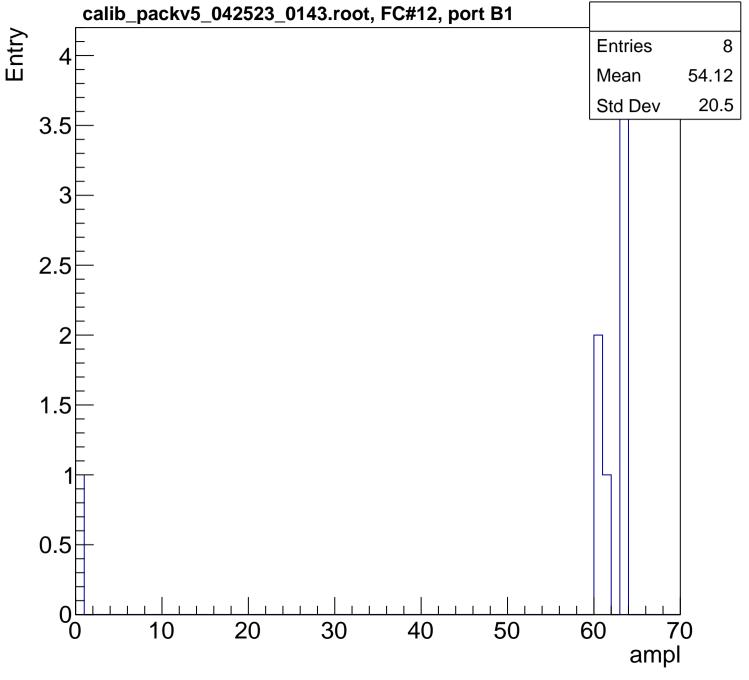




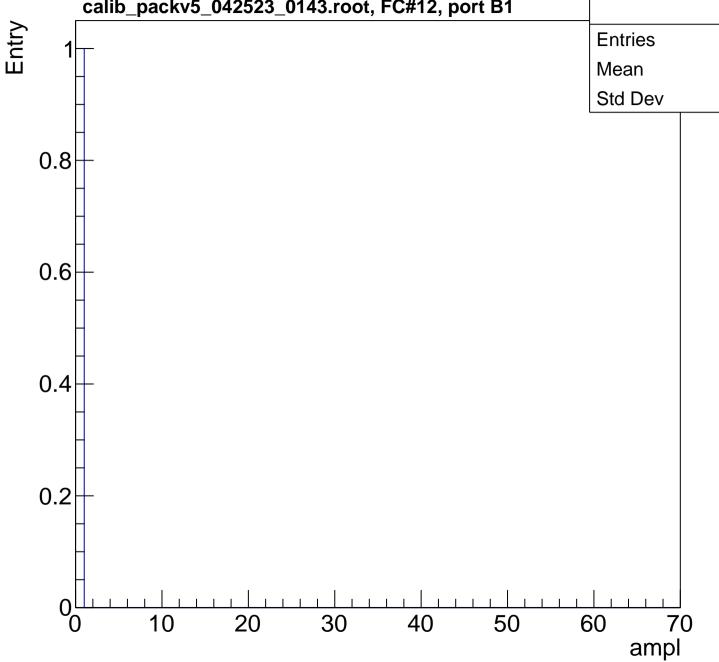


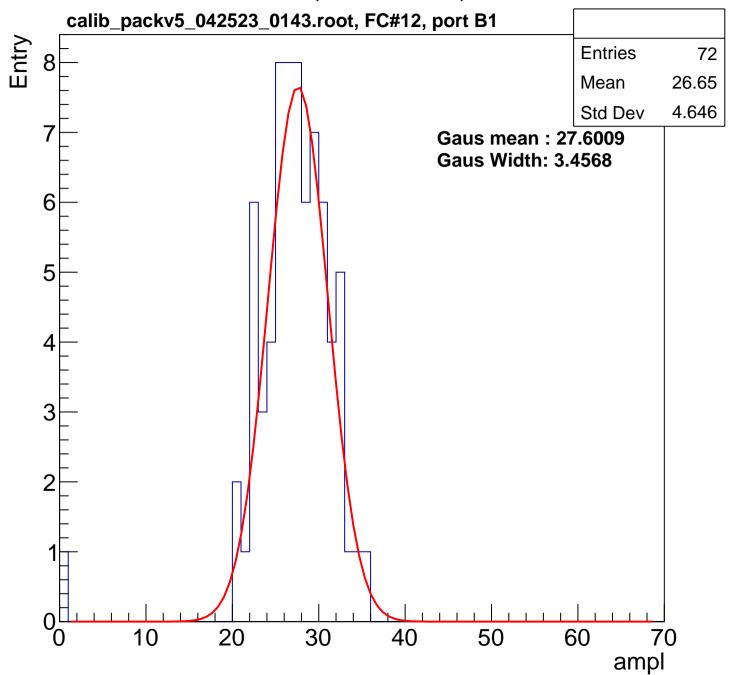


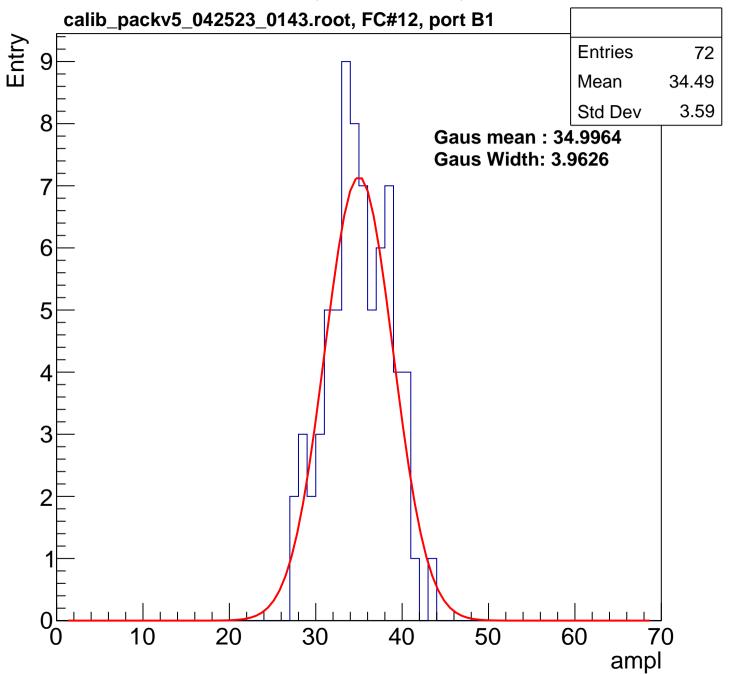


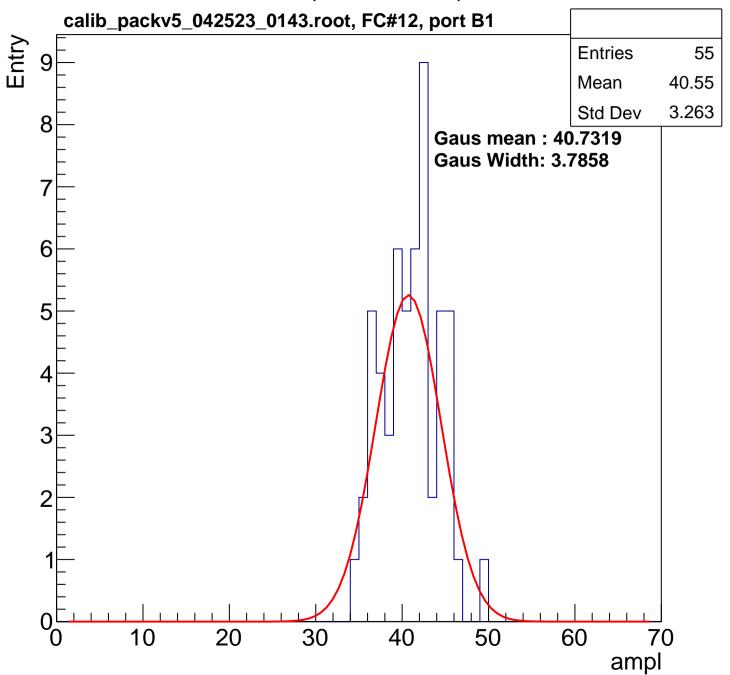


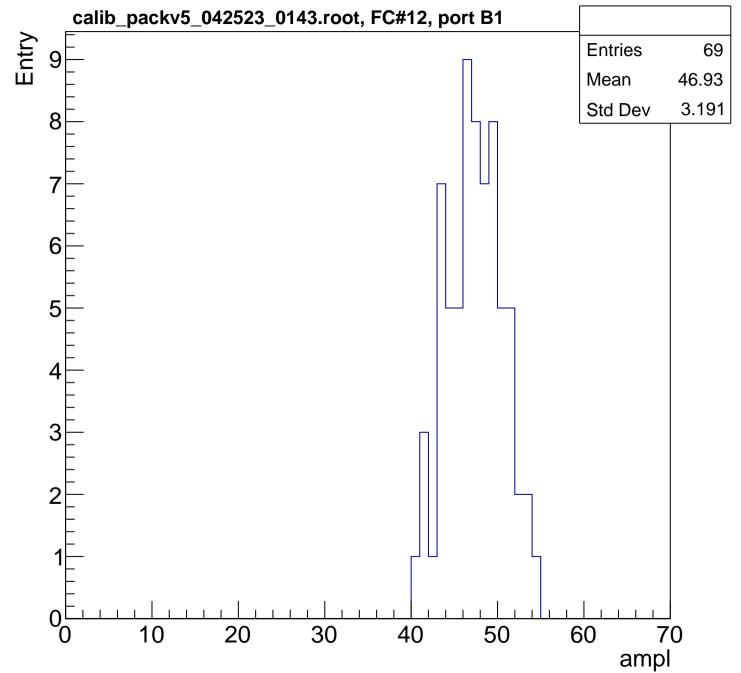
B0L102S, U2-ch19, adc7 calib_packv5_042523_0143.root, FC#12, port B1

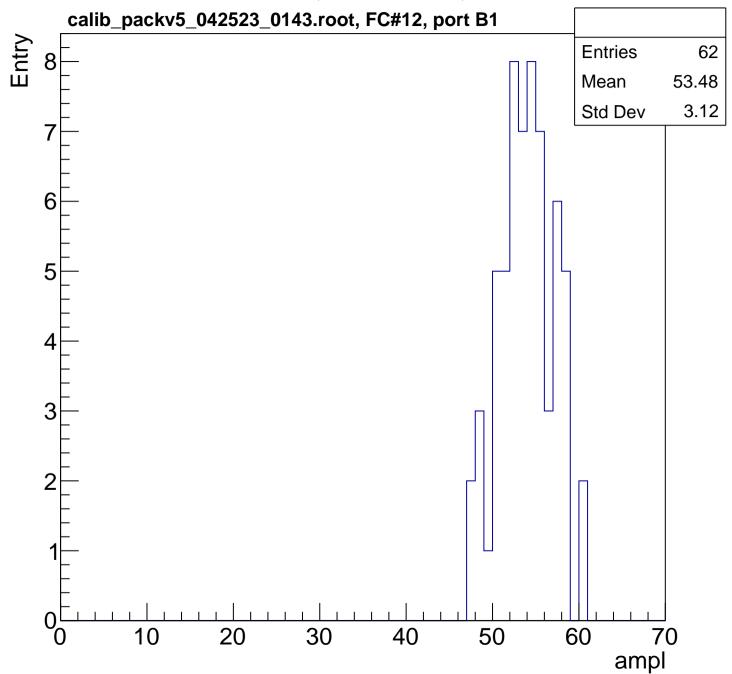


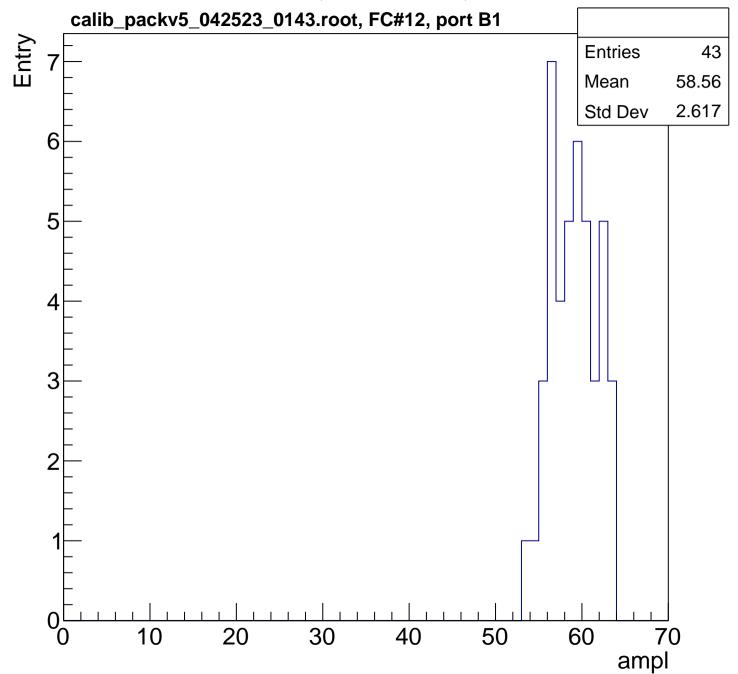


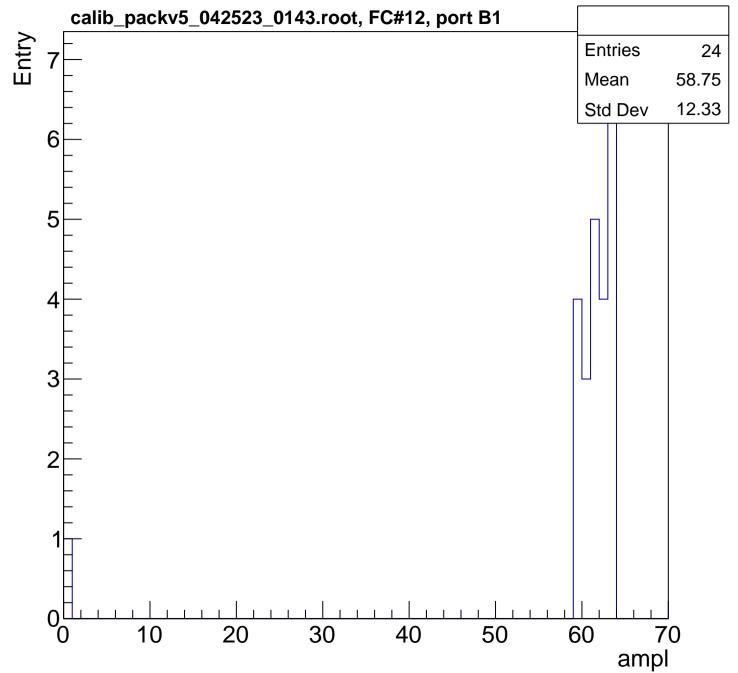


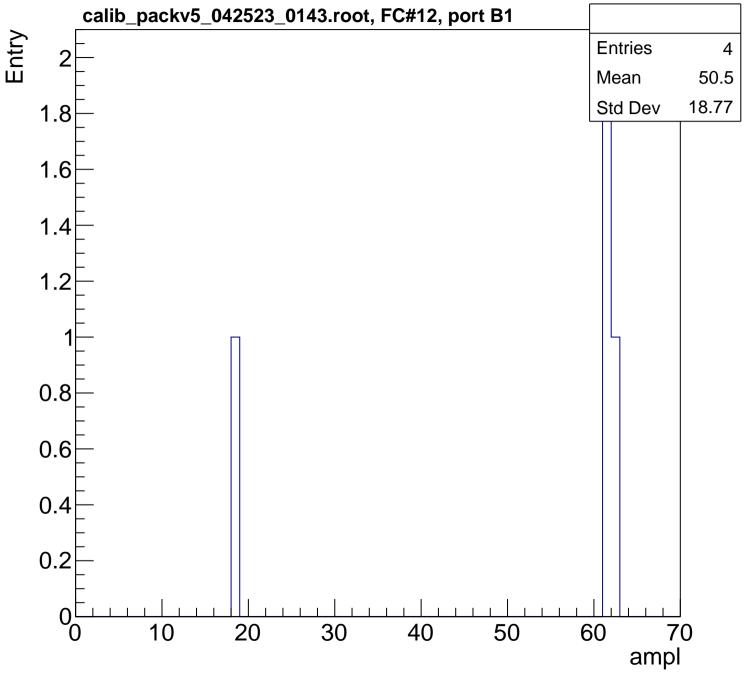


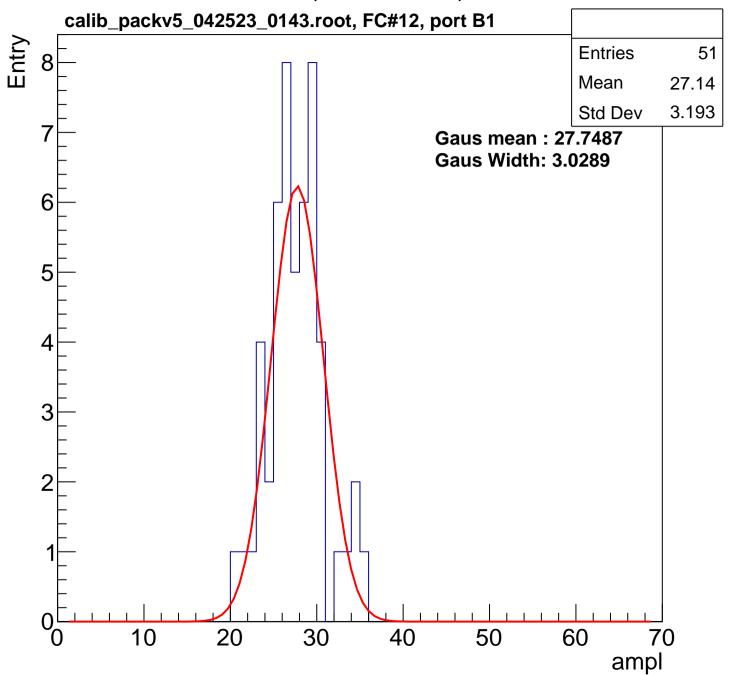


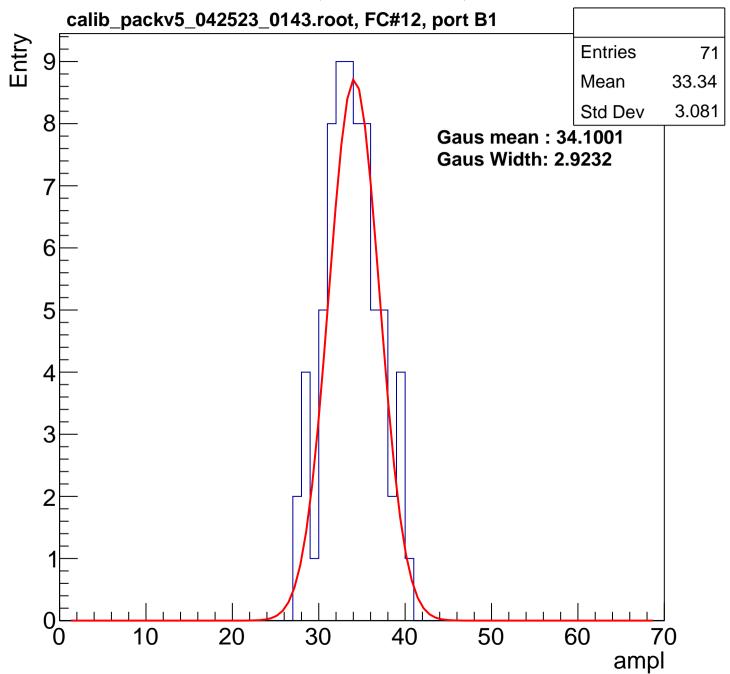


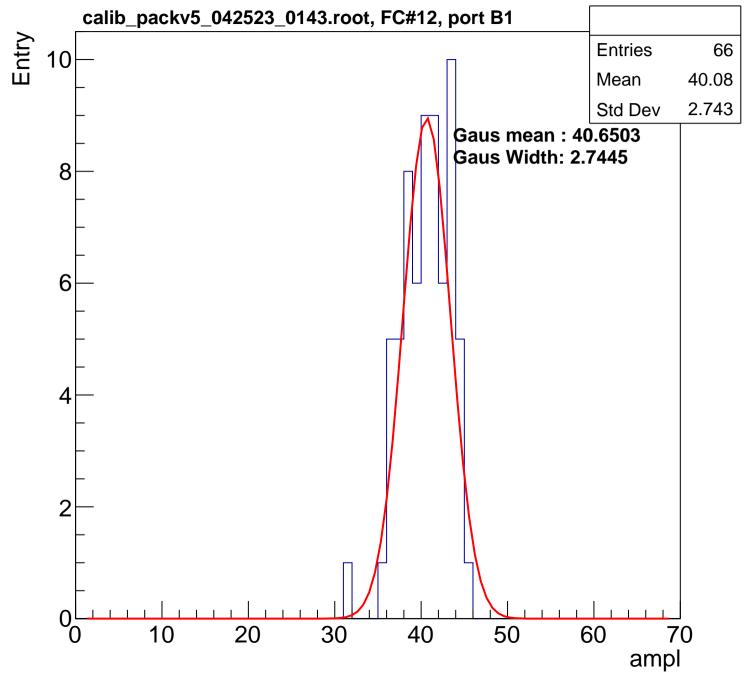


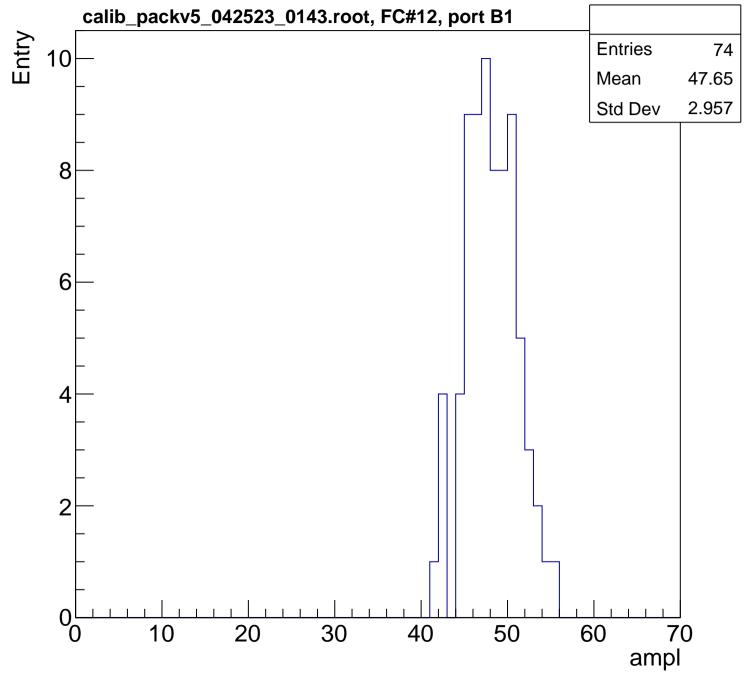


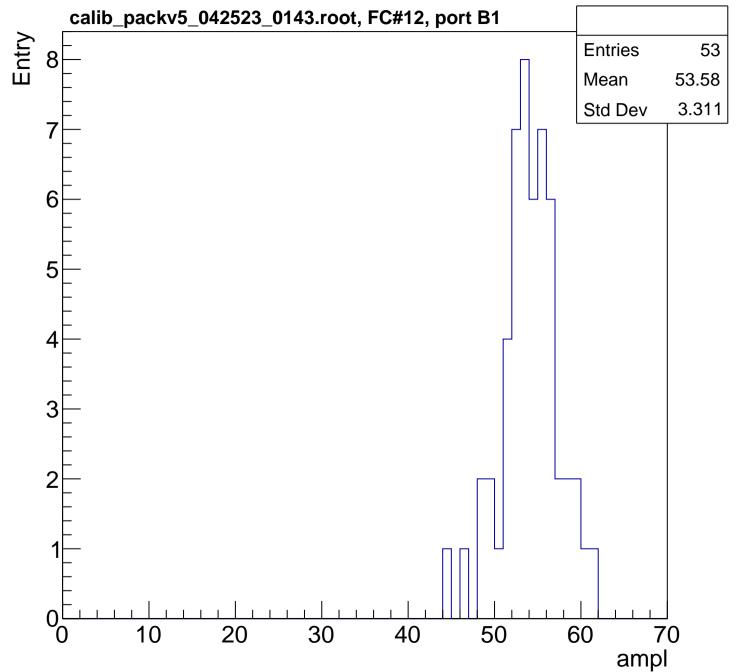


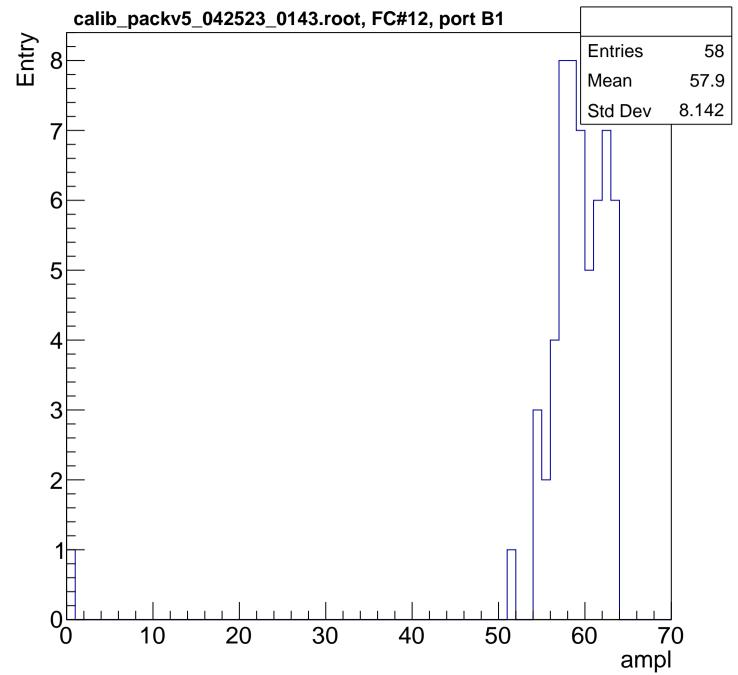


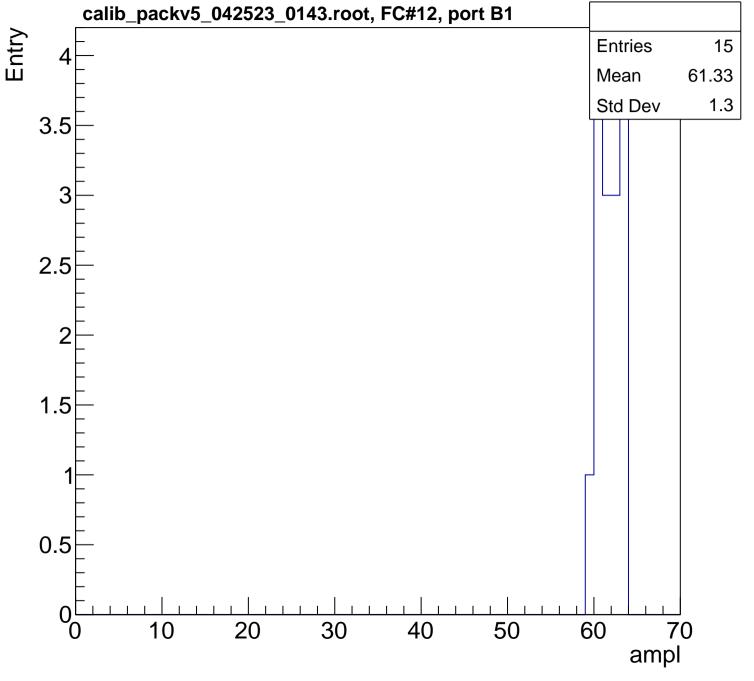




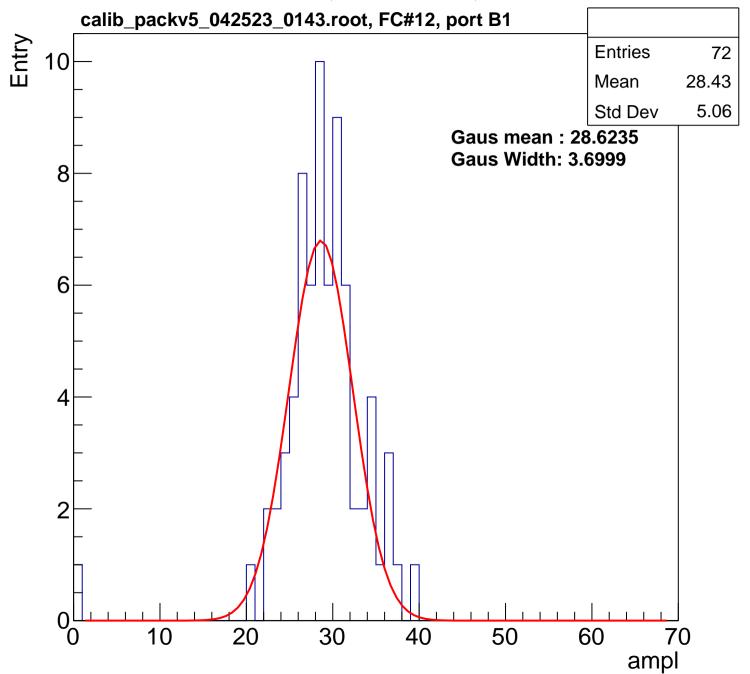


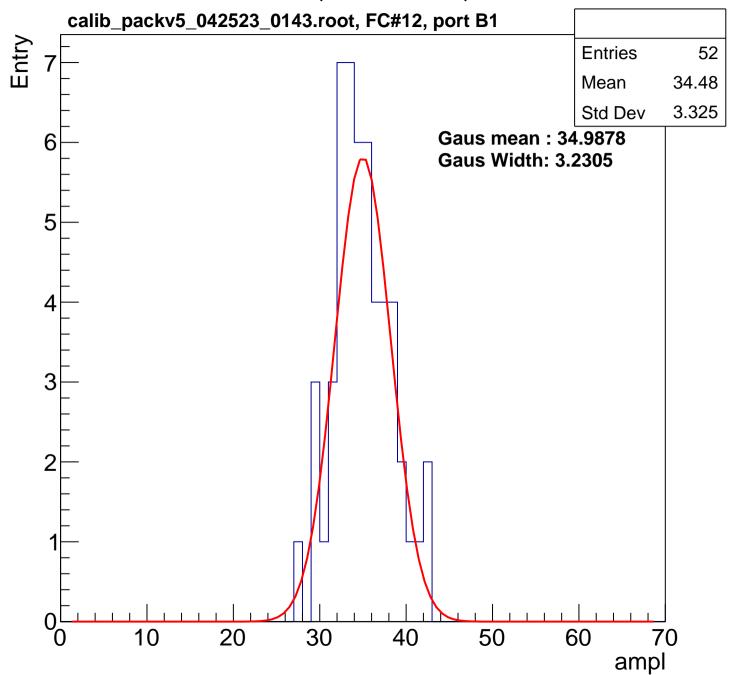


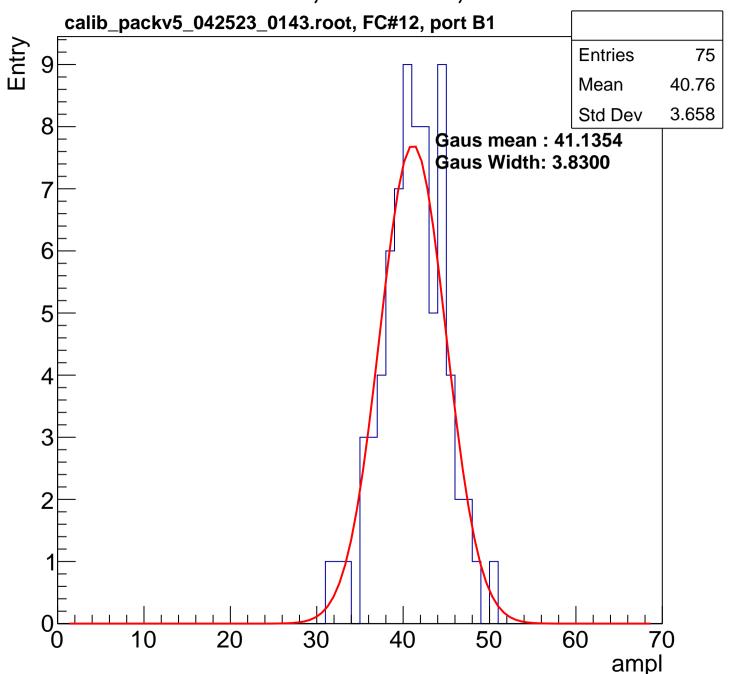


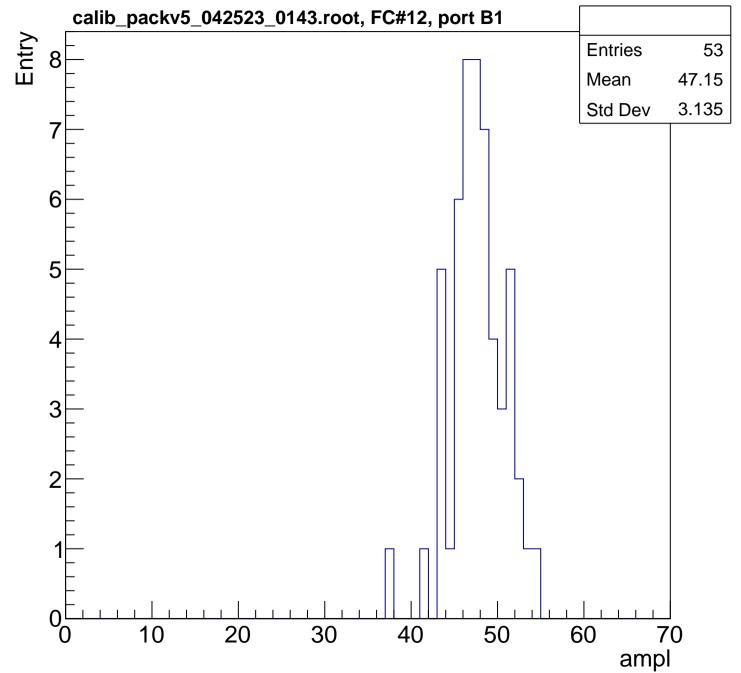


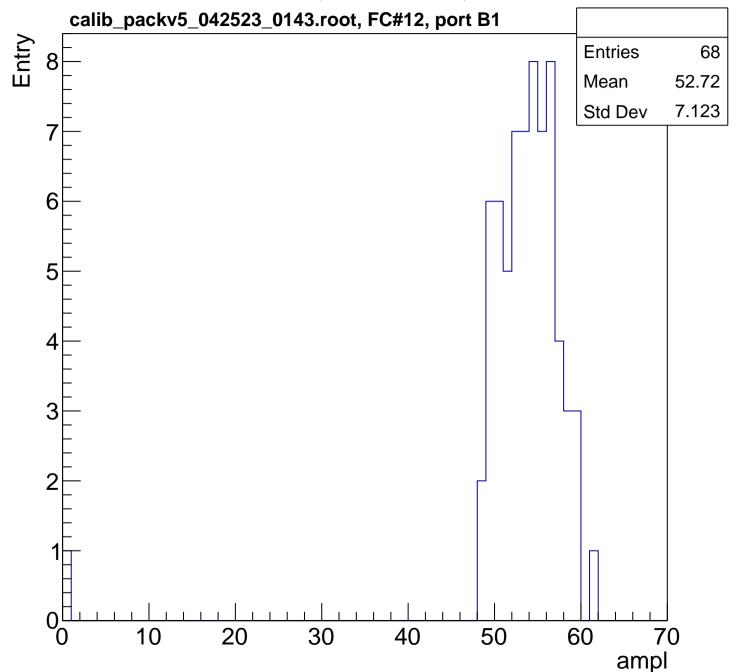


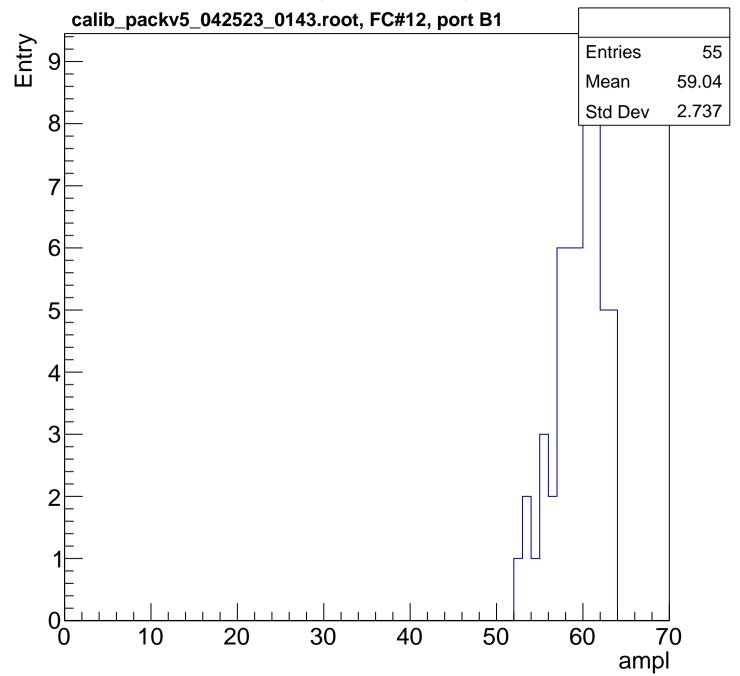


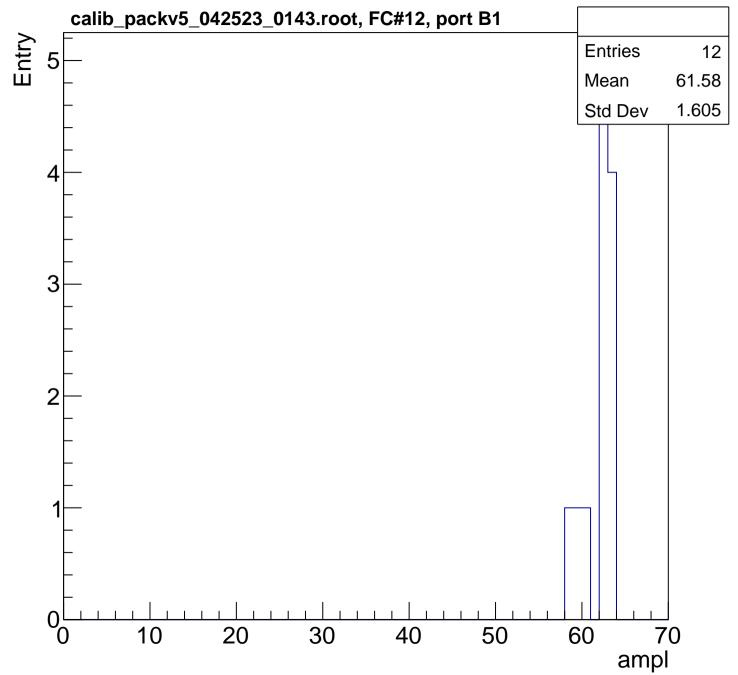


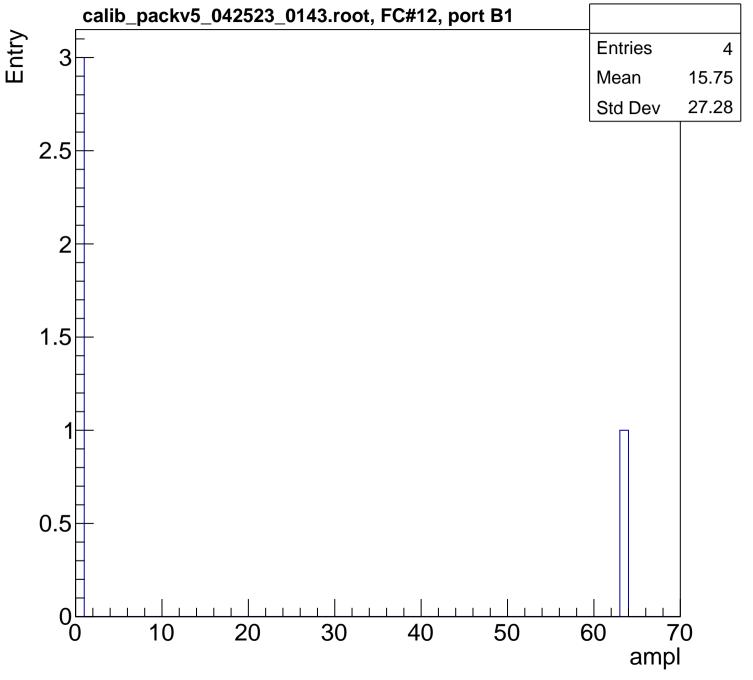


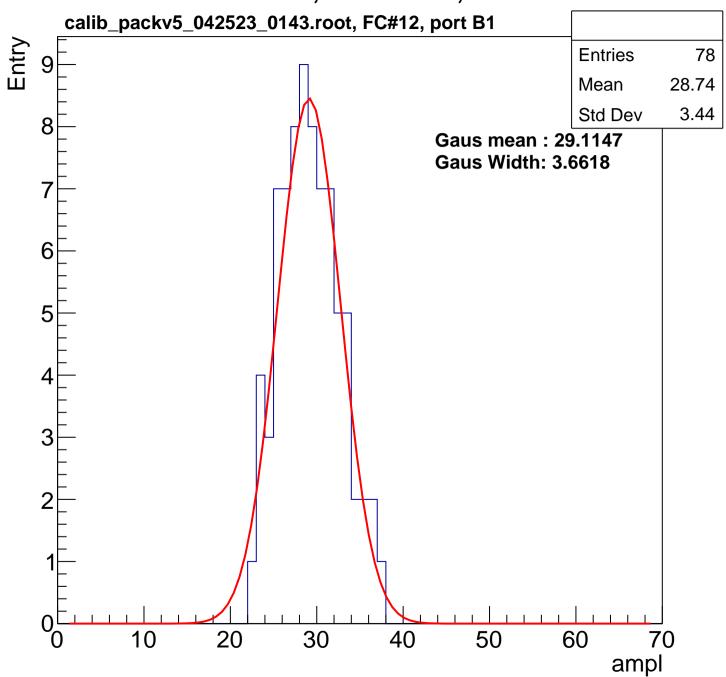


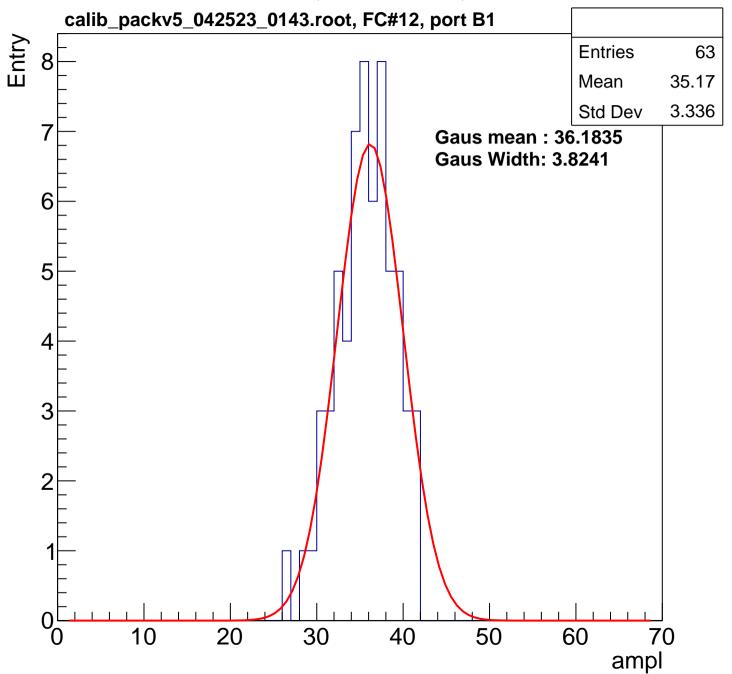


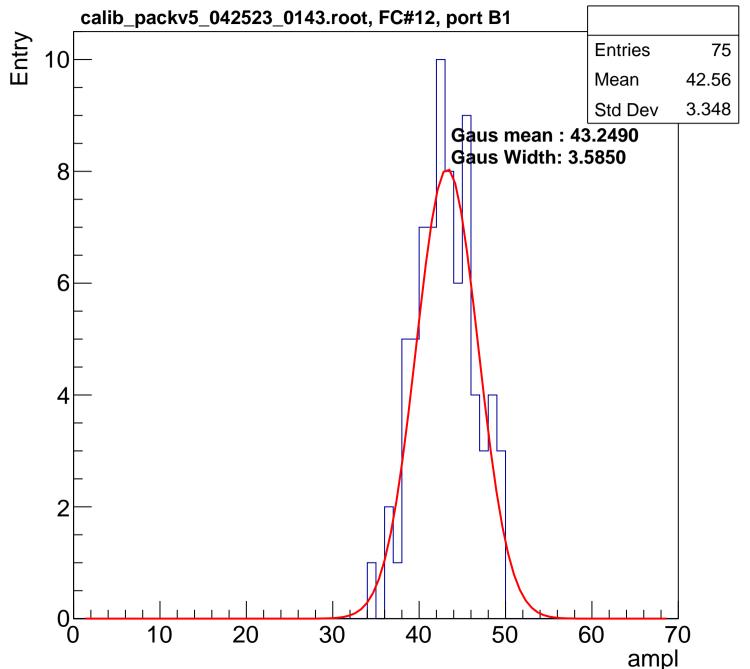


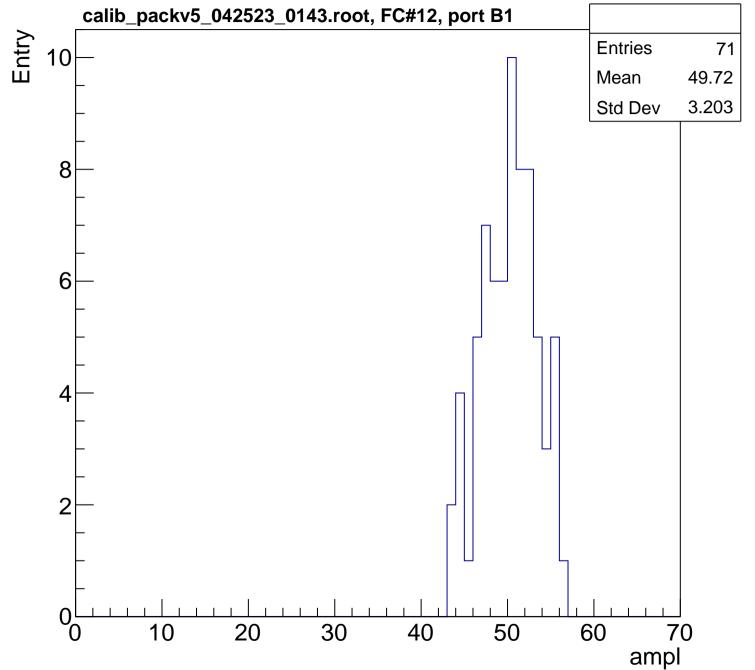


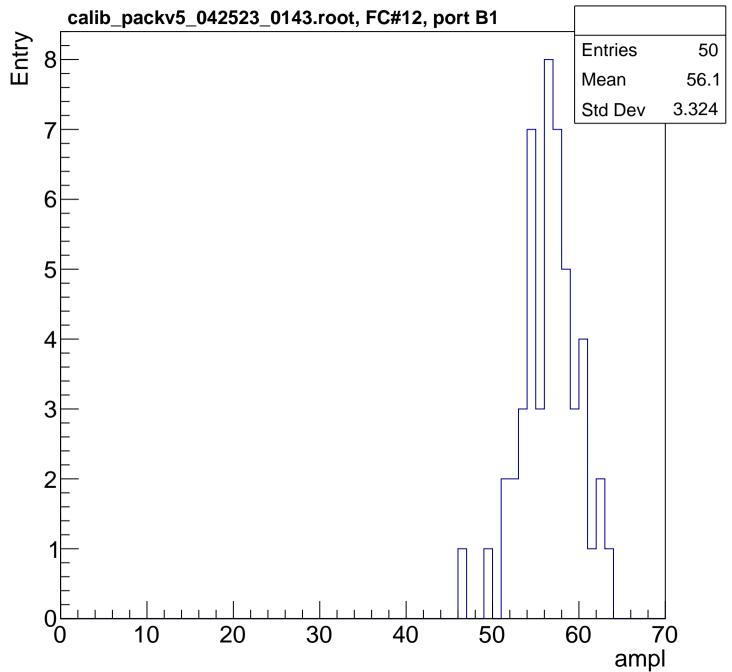


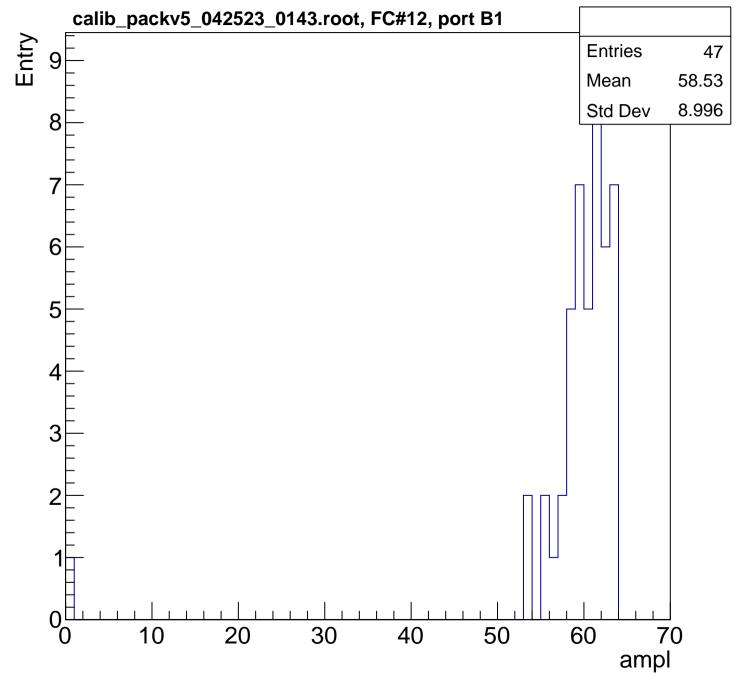


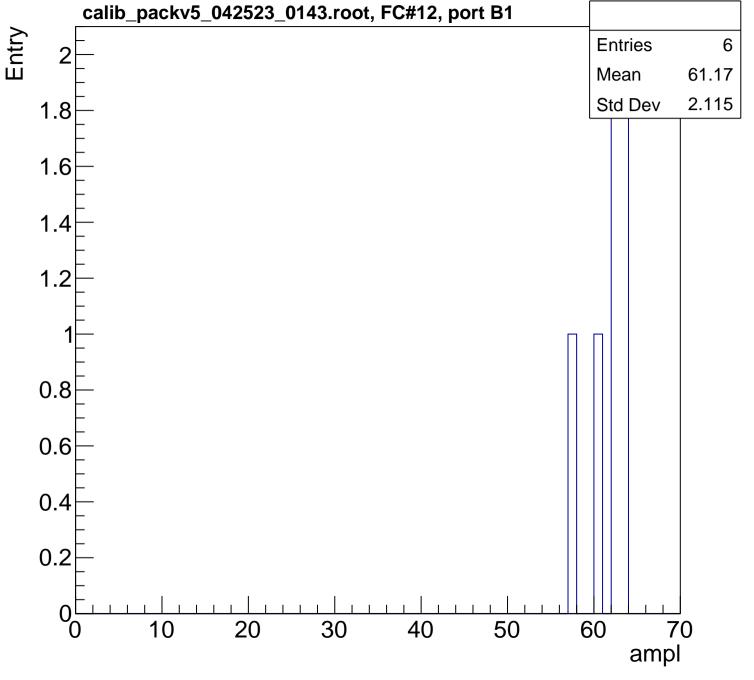




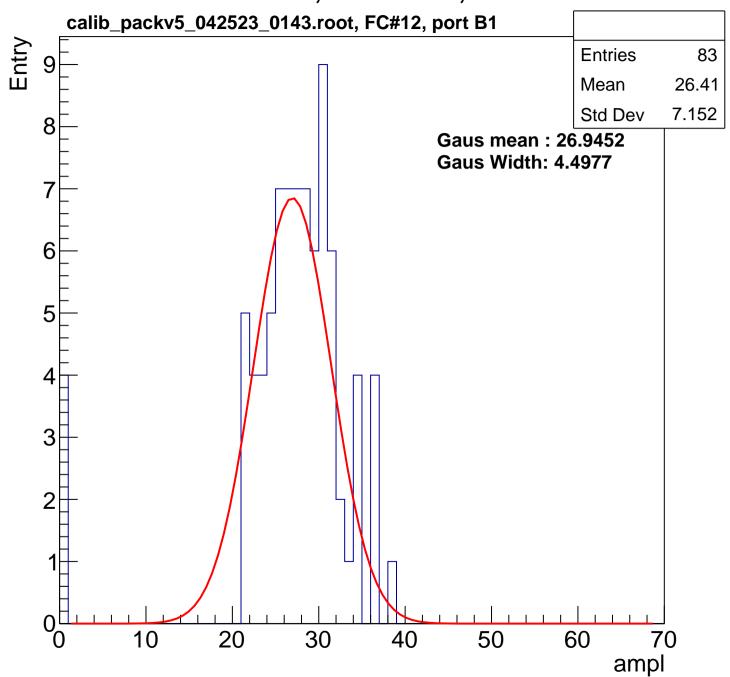


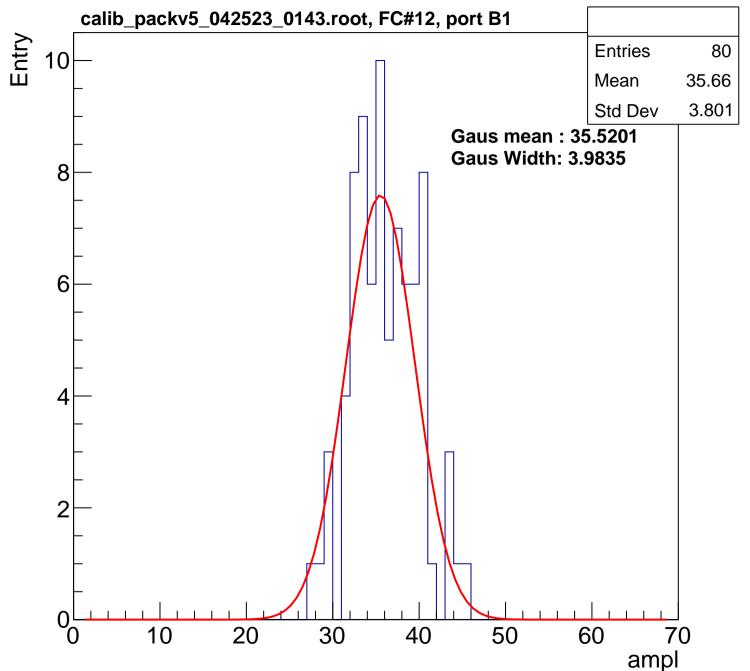


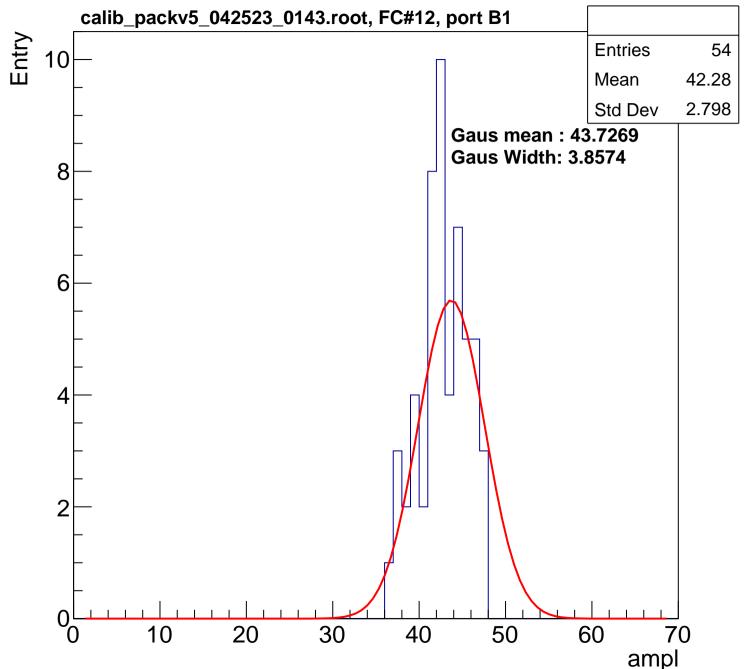


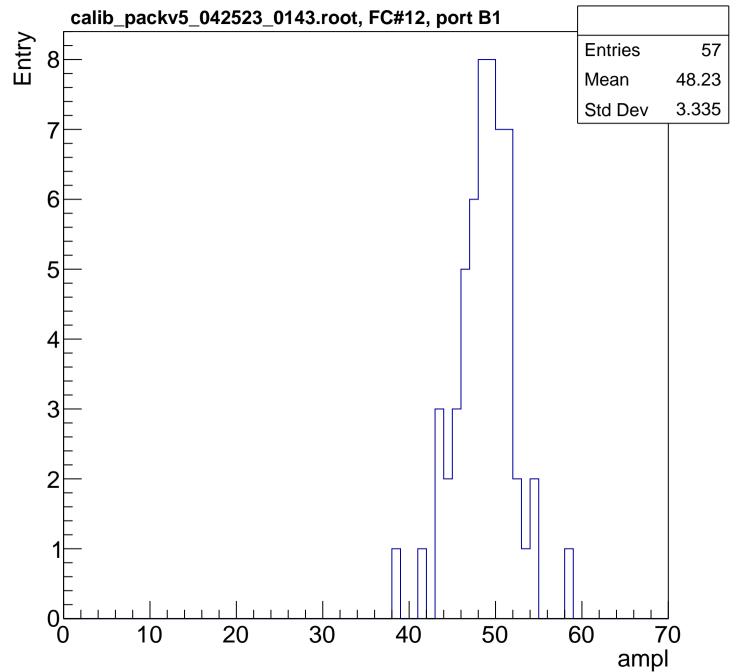


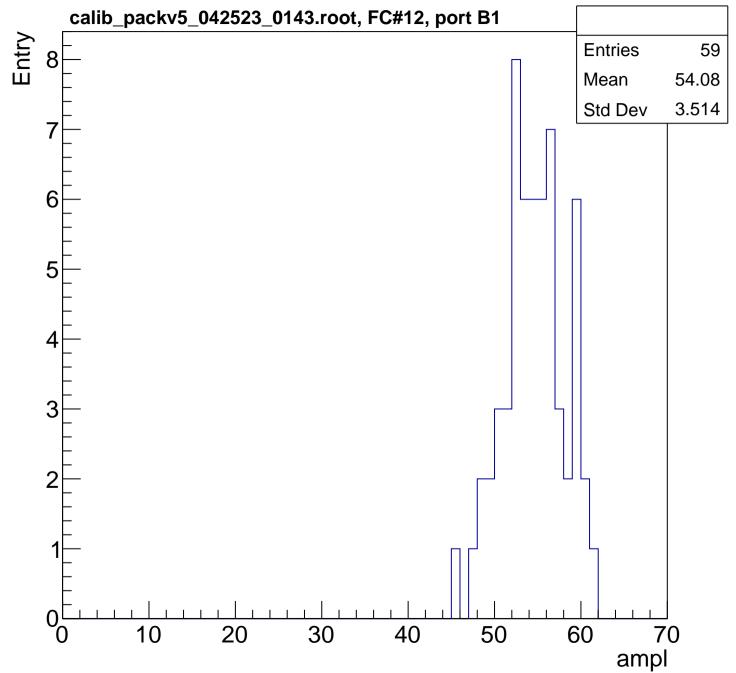
B0L102S, U2-ch23, adc7 calib_packv5_042523_0143.root, FC#12, port B1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

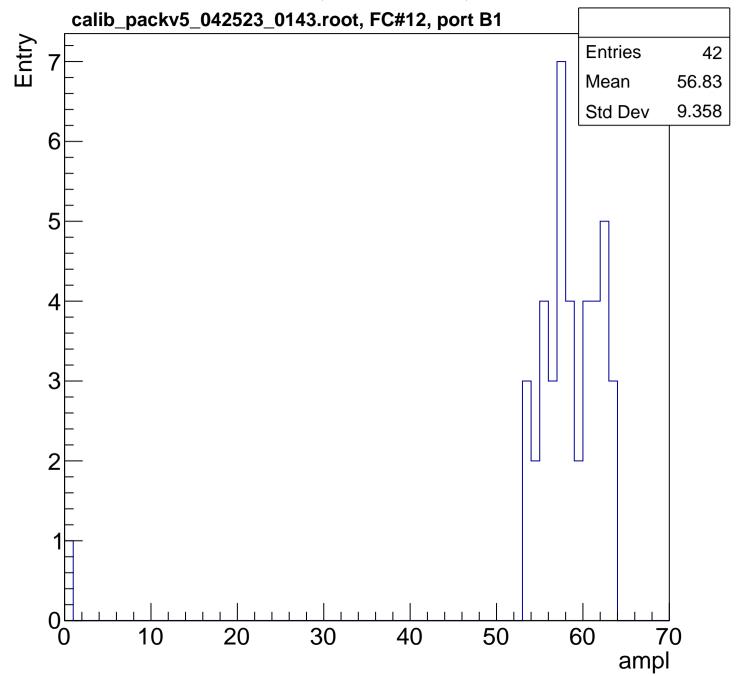


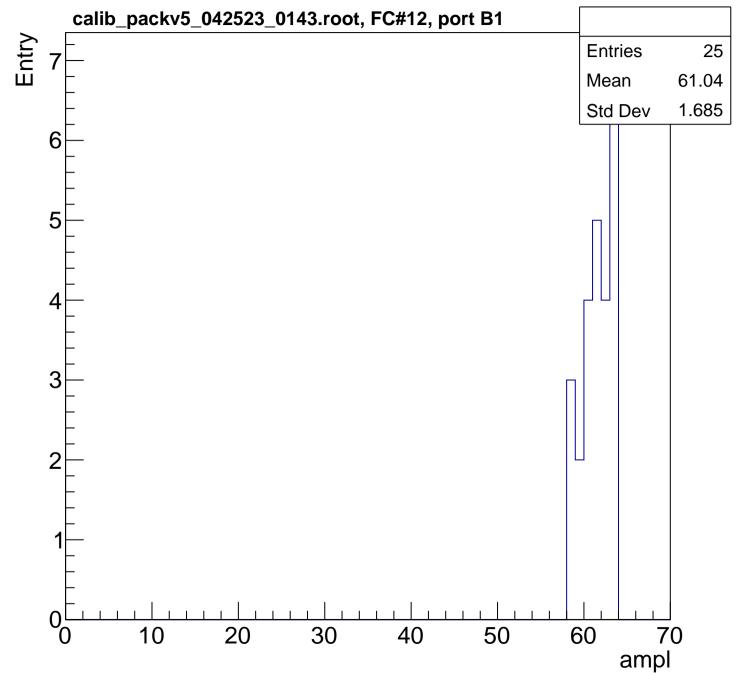


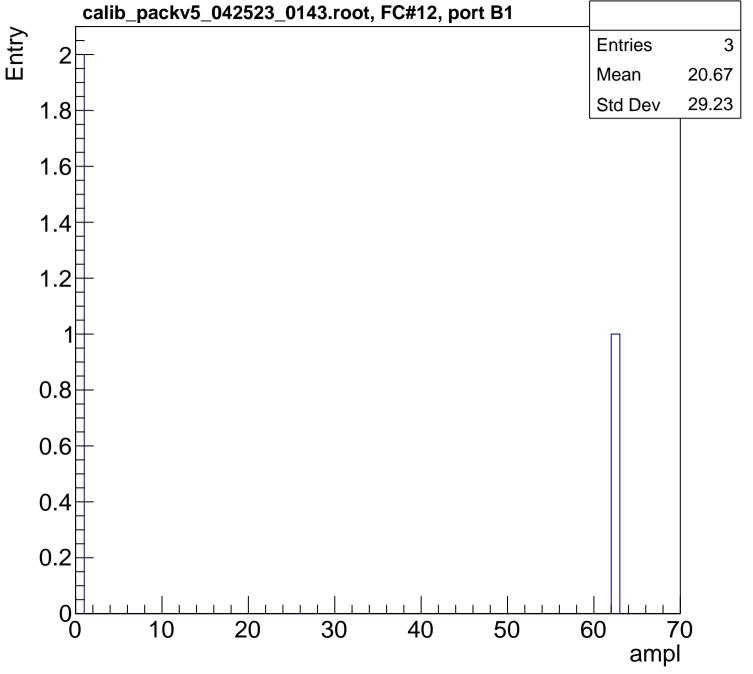


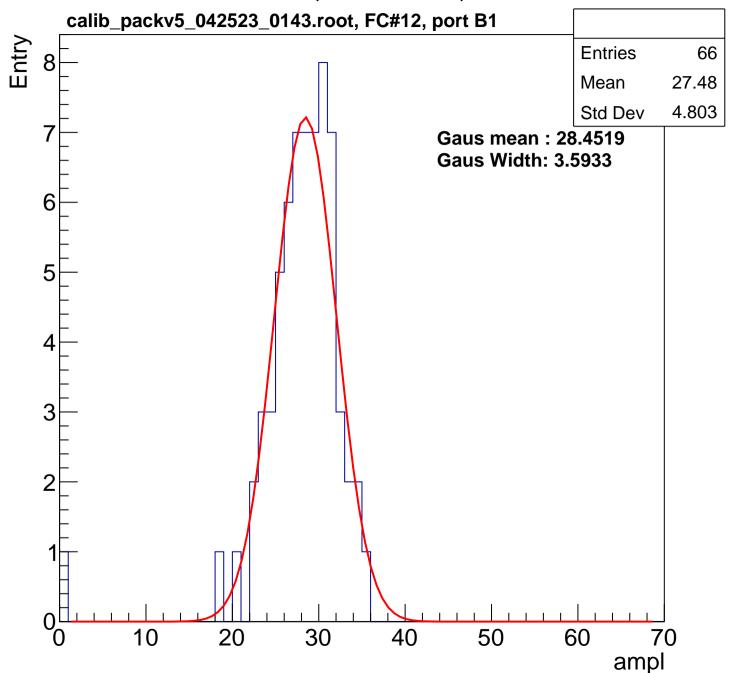


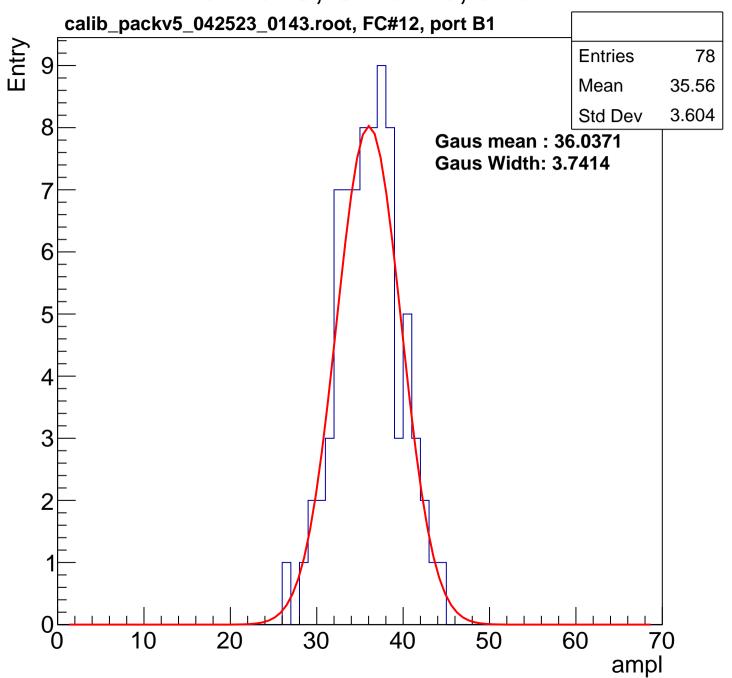


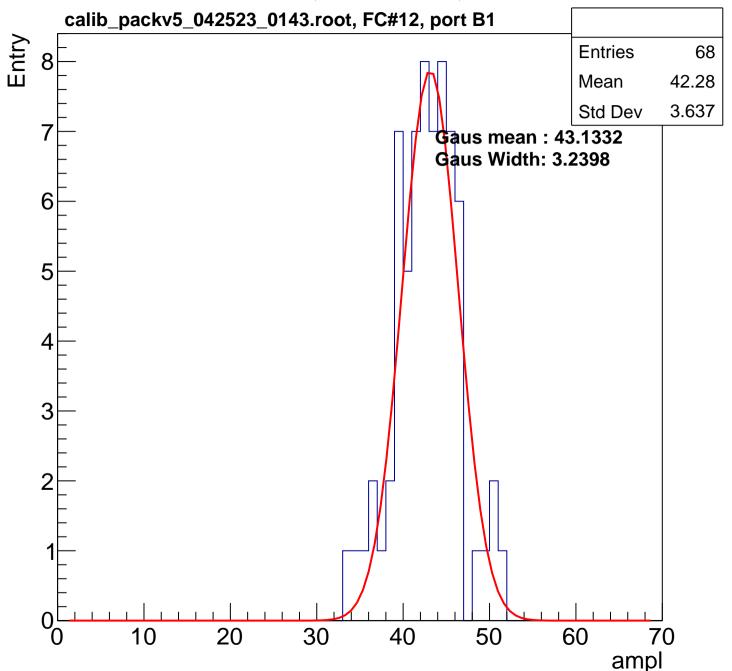


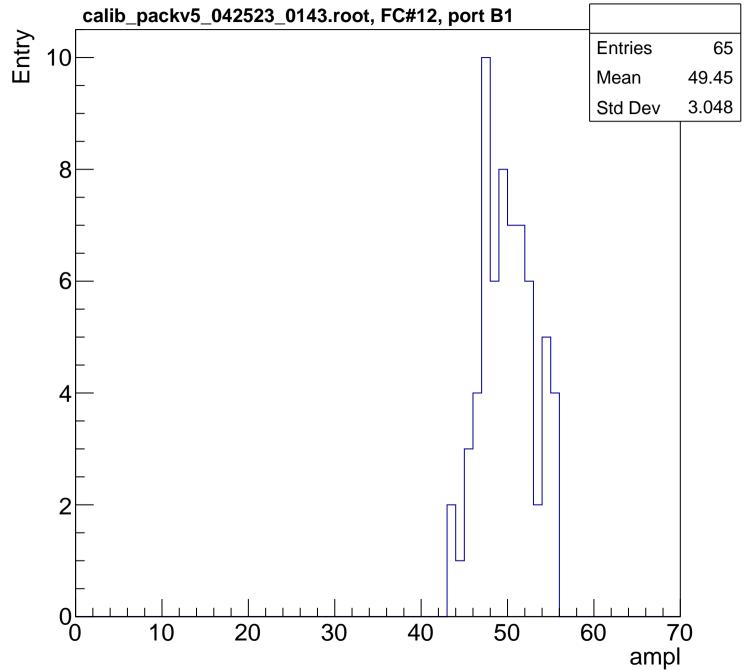


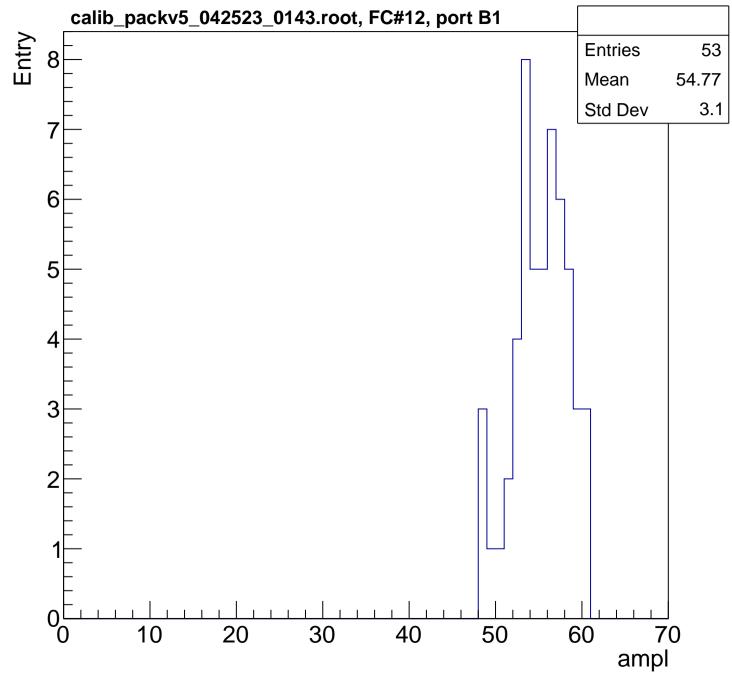


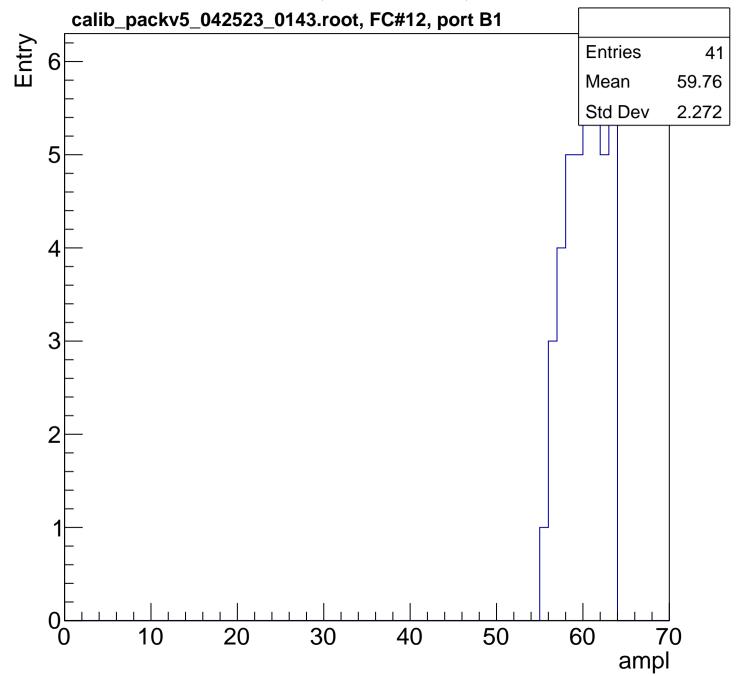


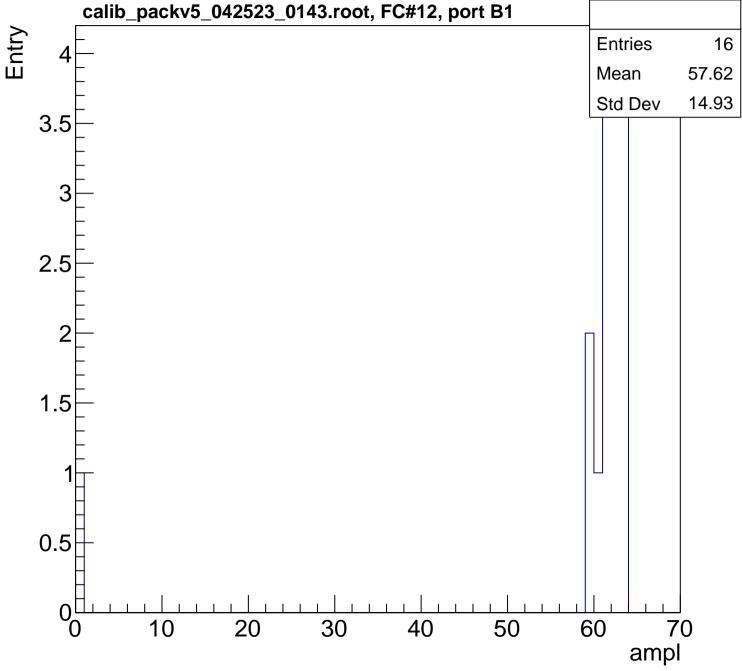


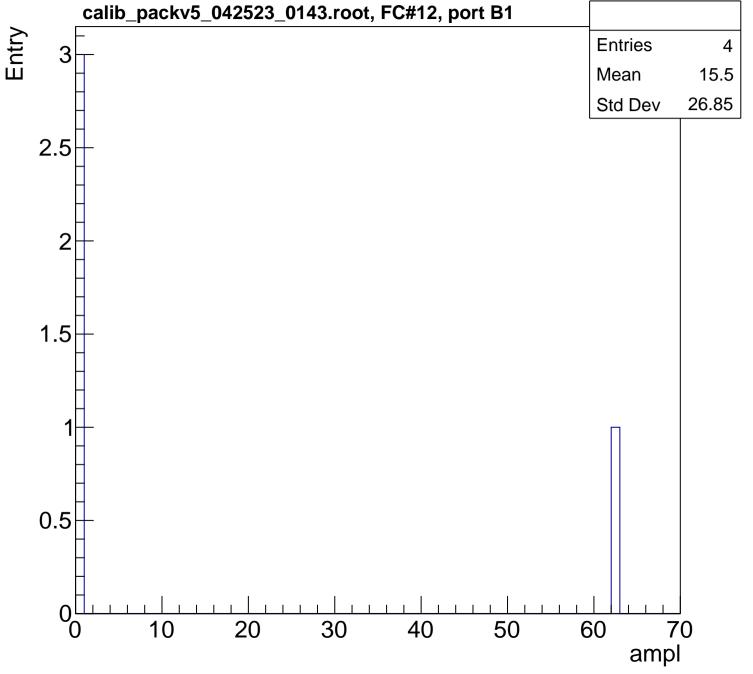


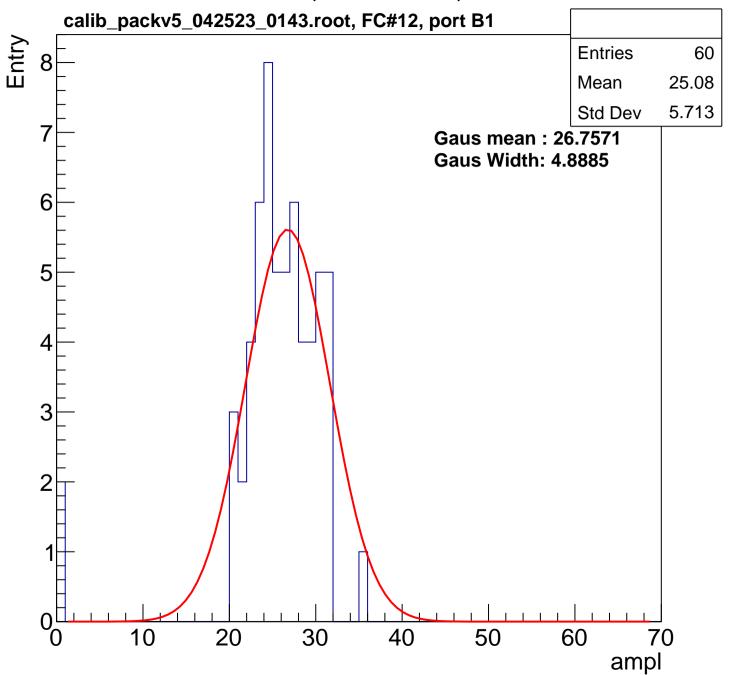


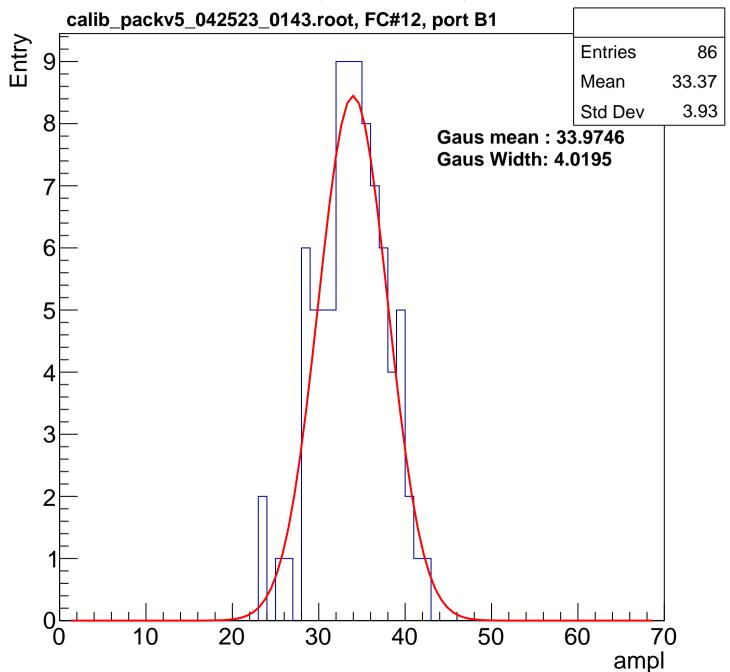


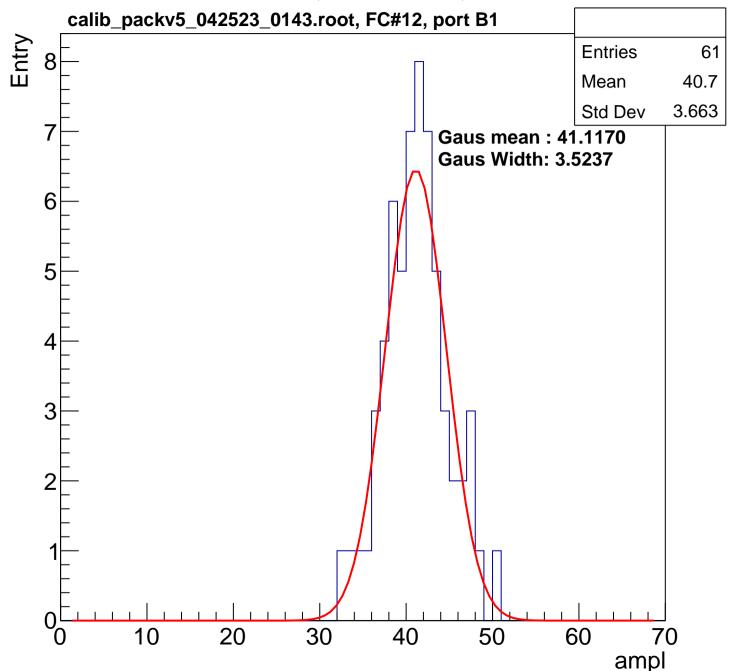


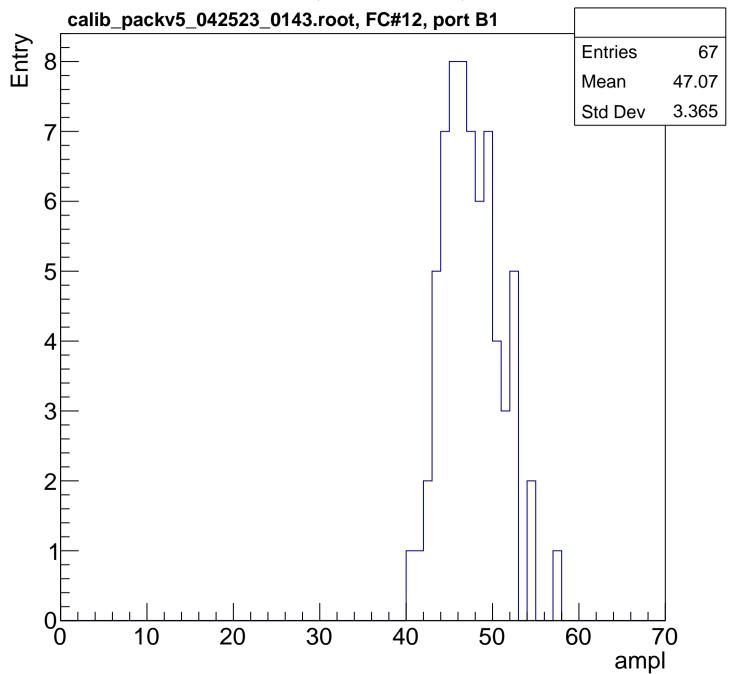


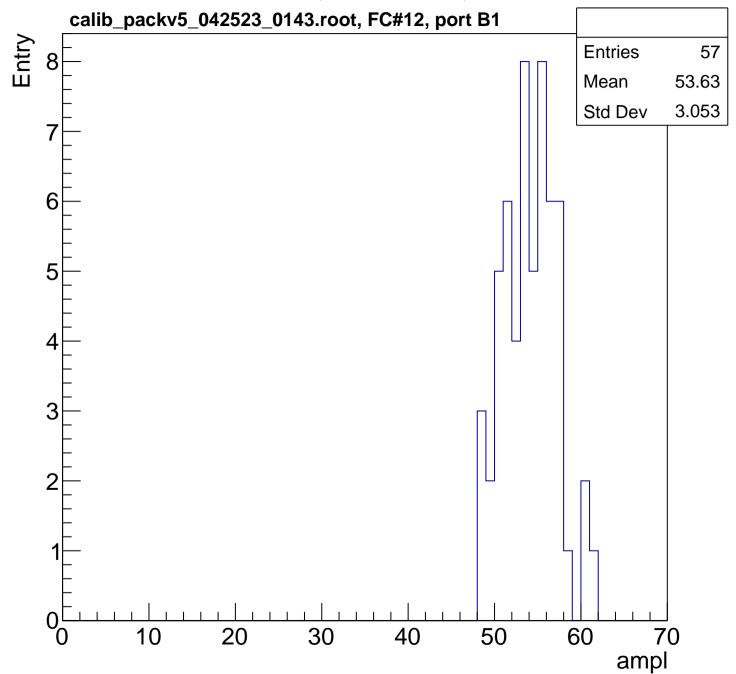


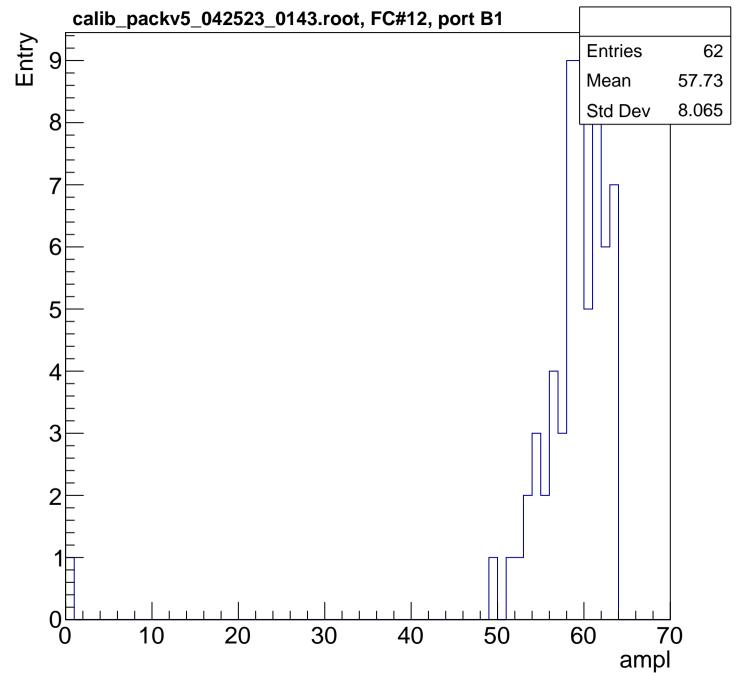


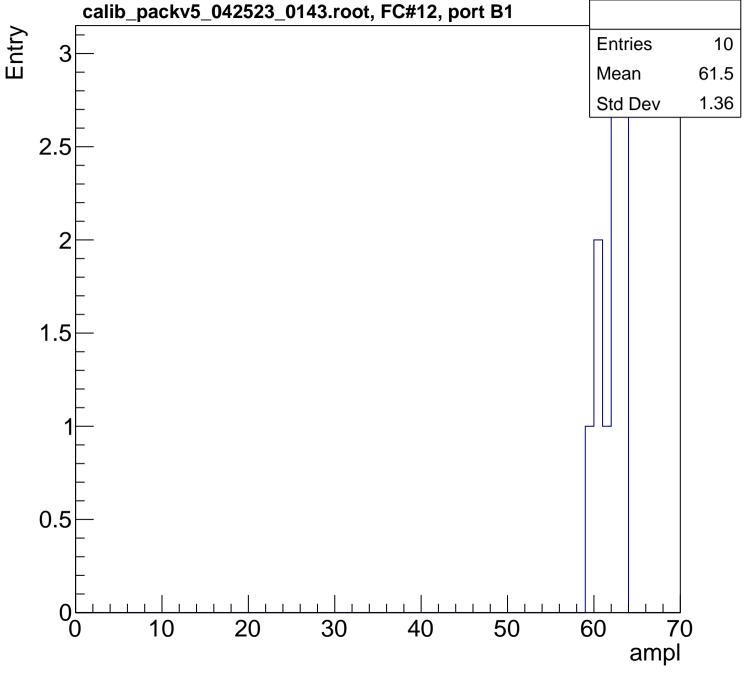


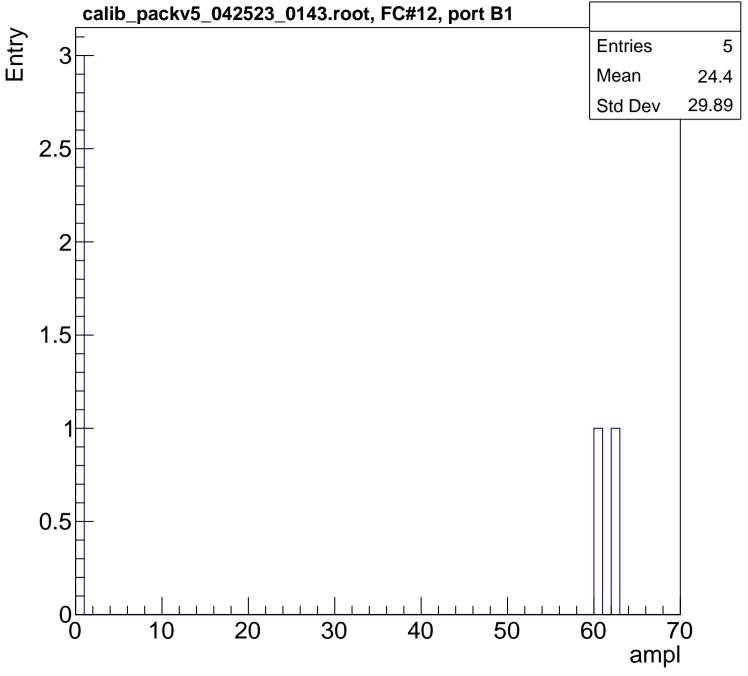


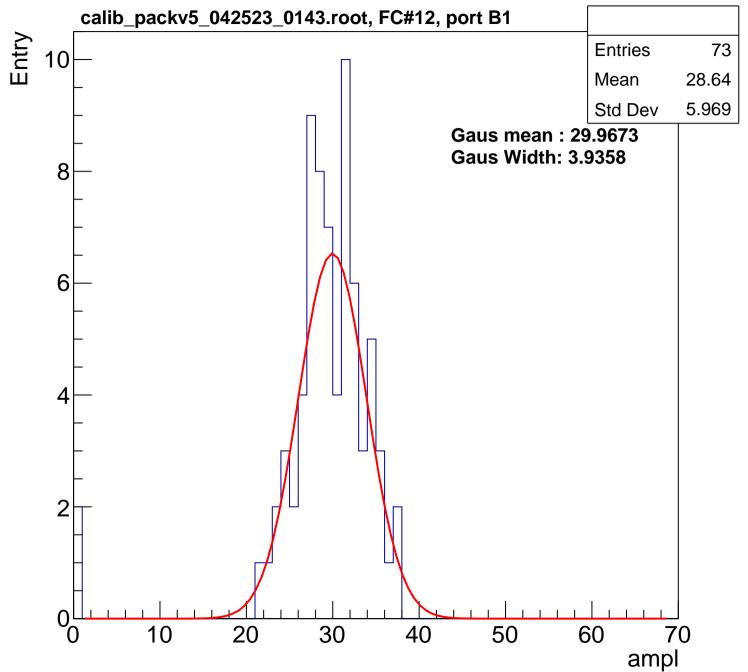


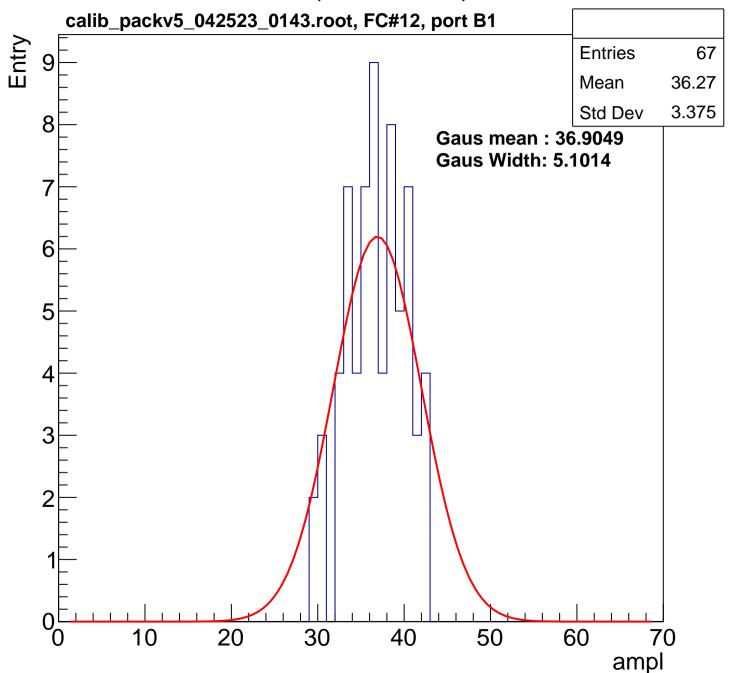


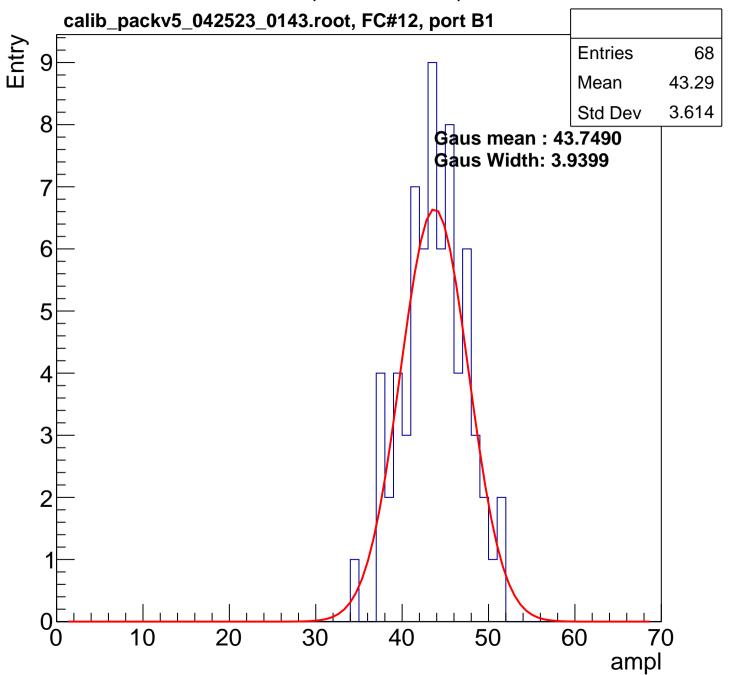


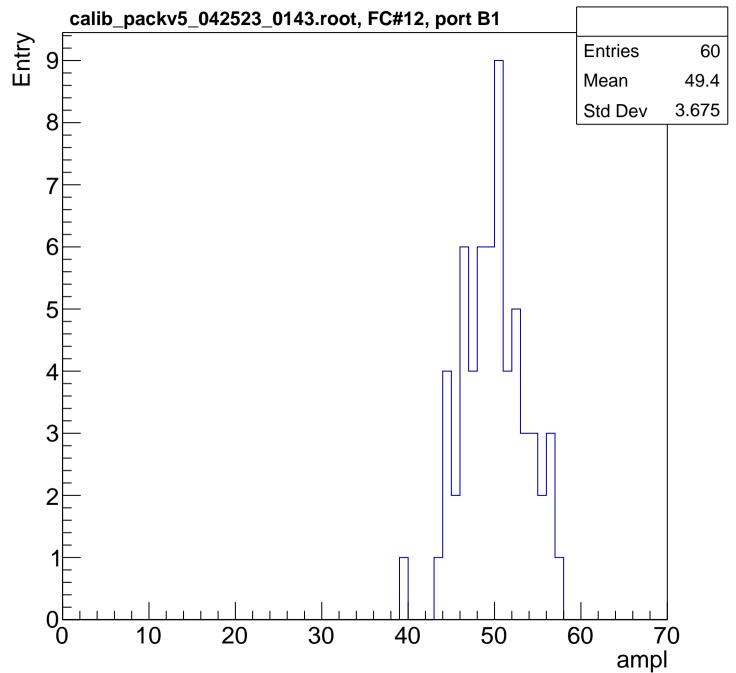


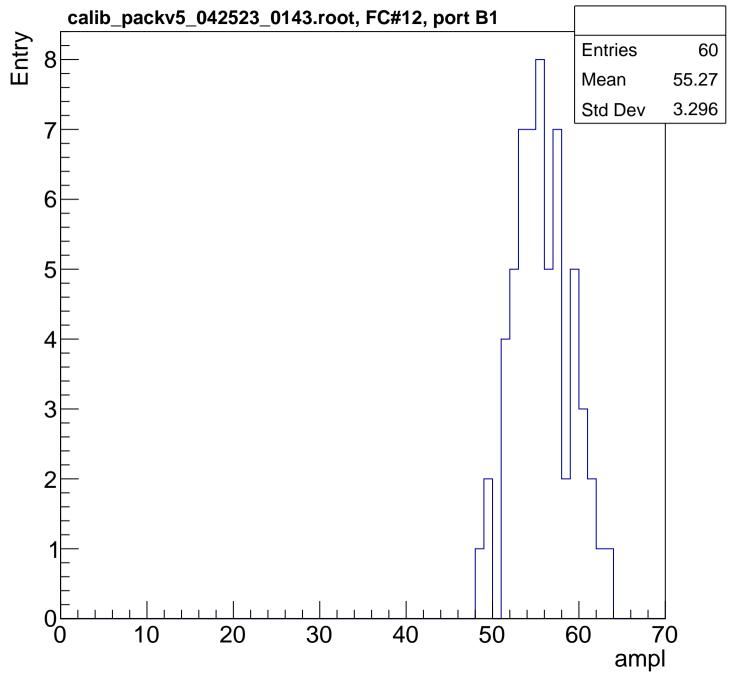


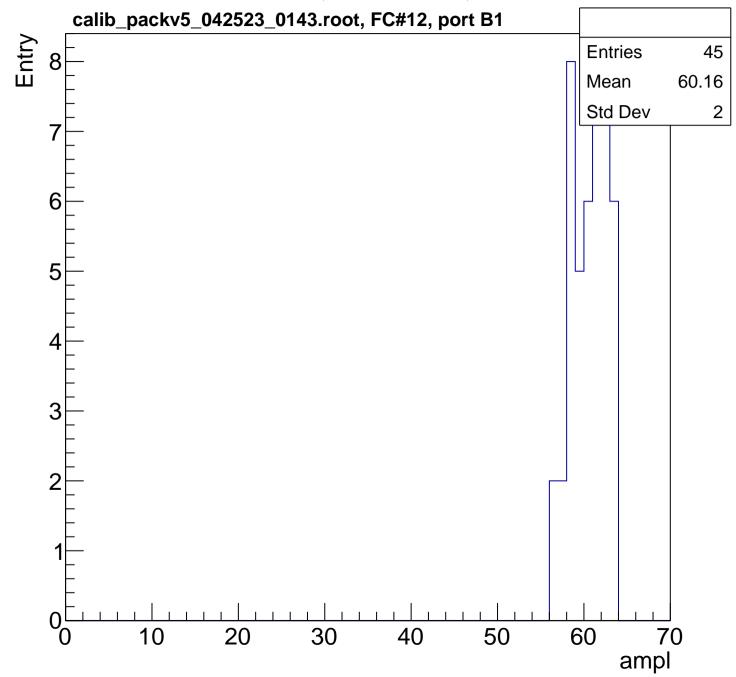


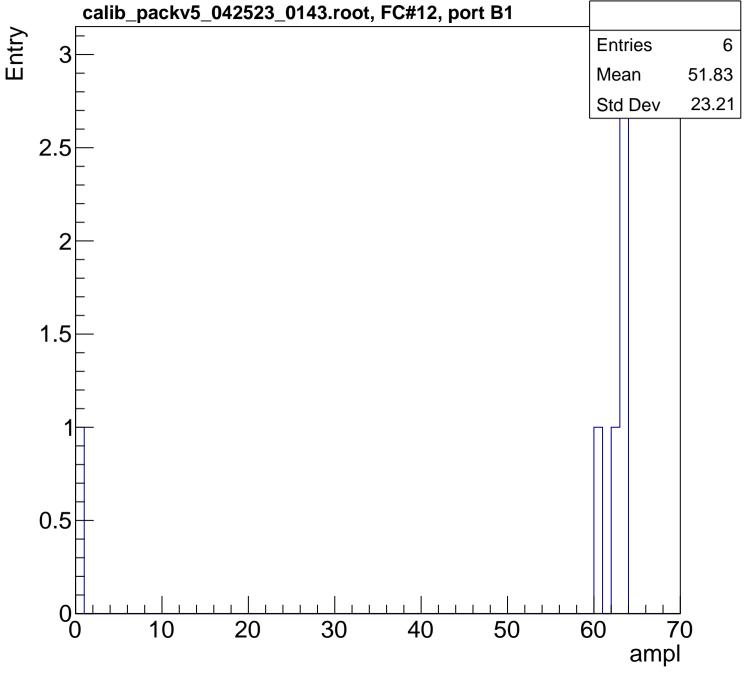




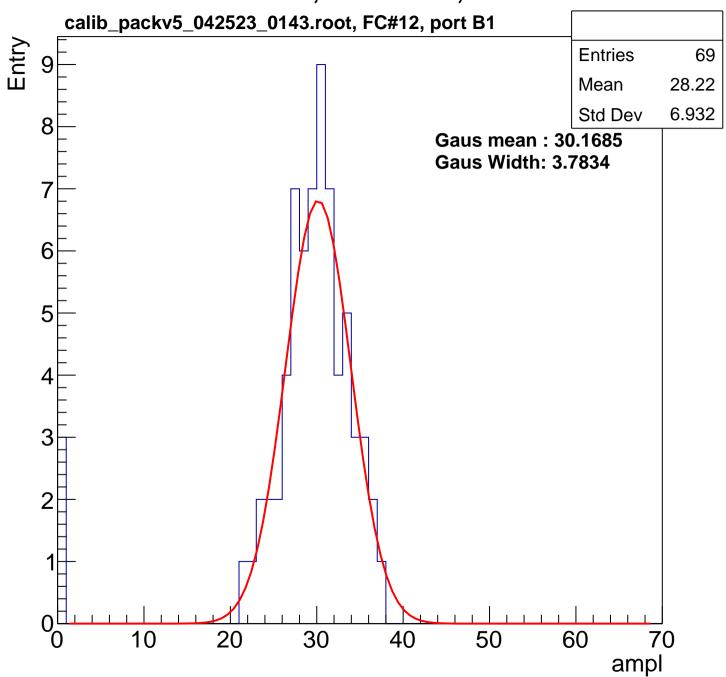


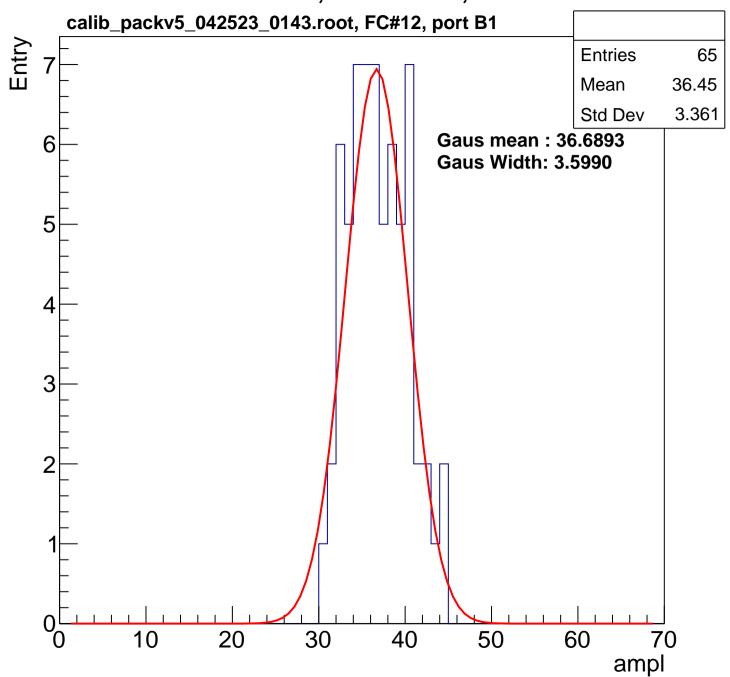


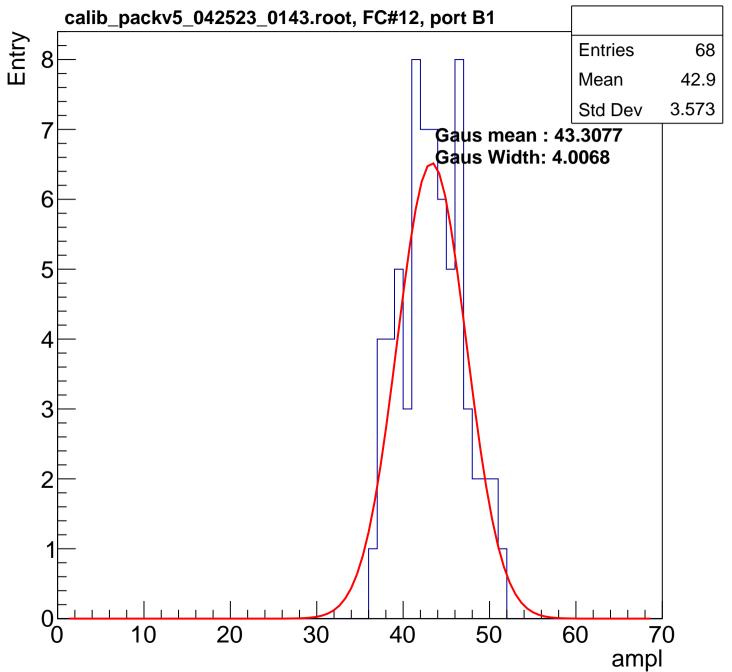


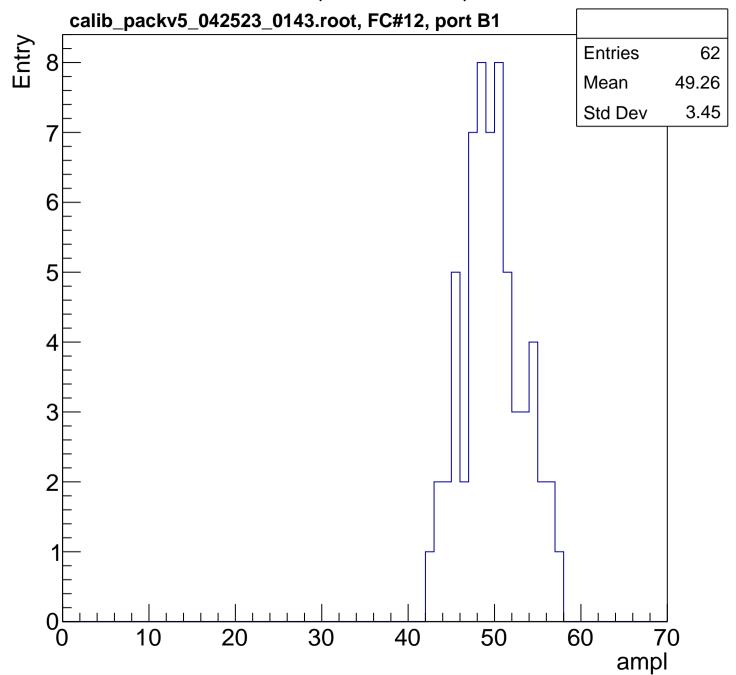


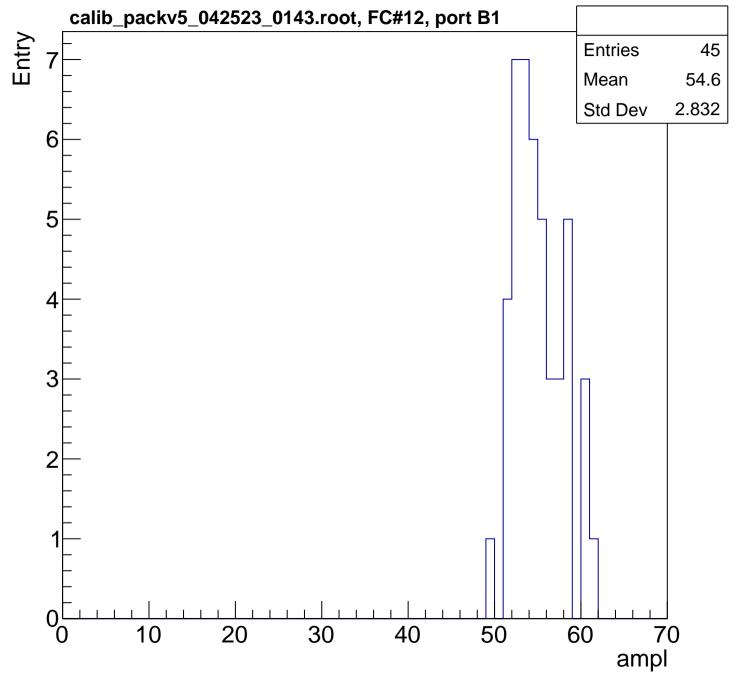


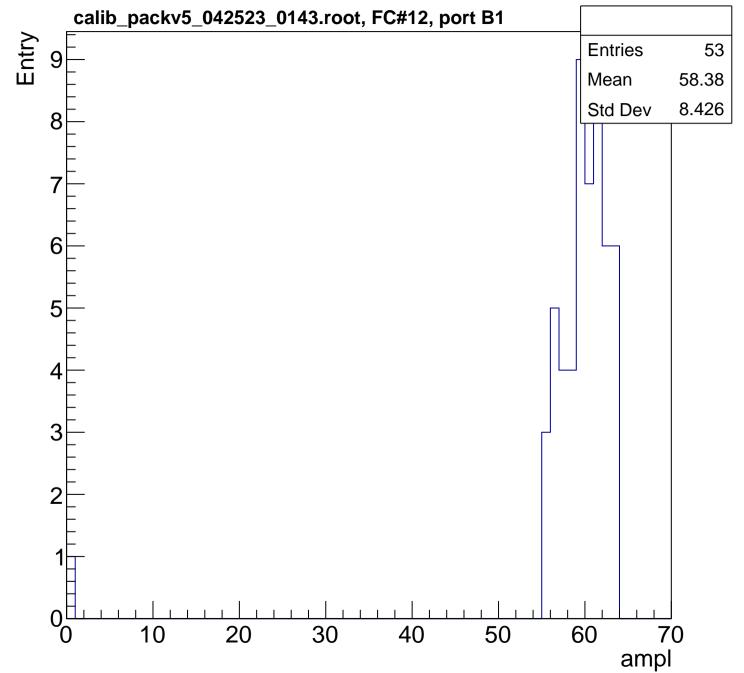


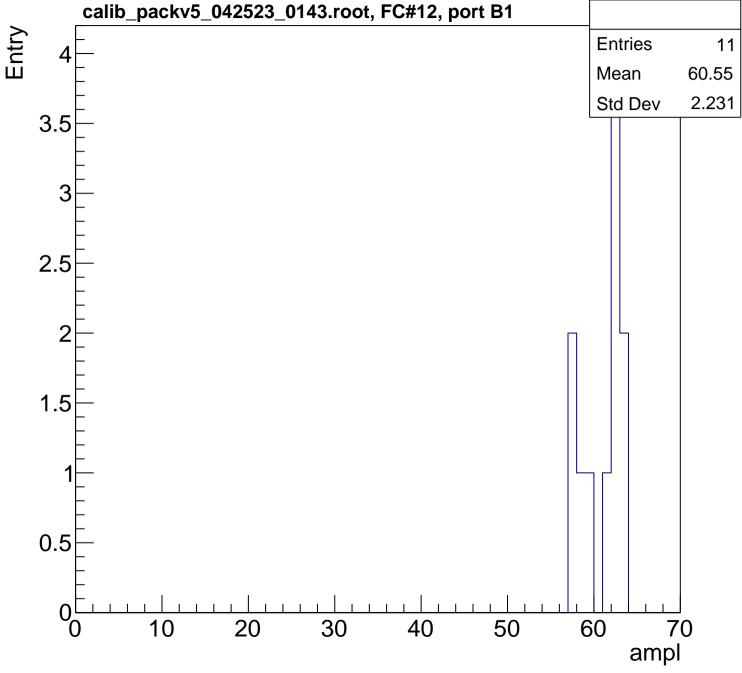


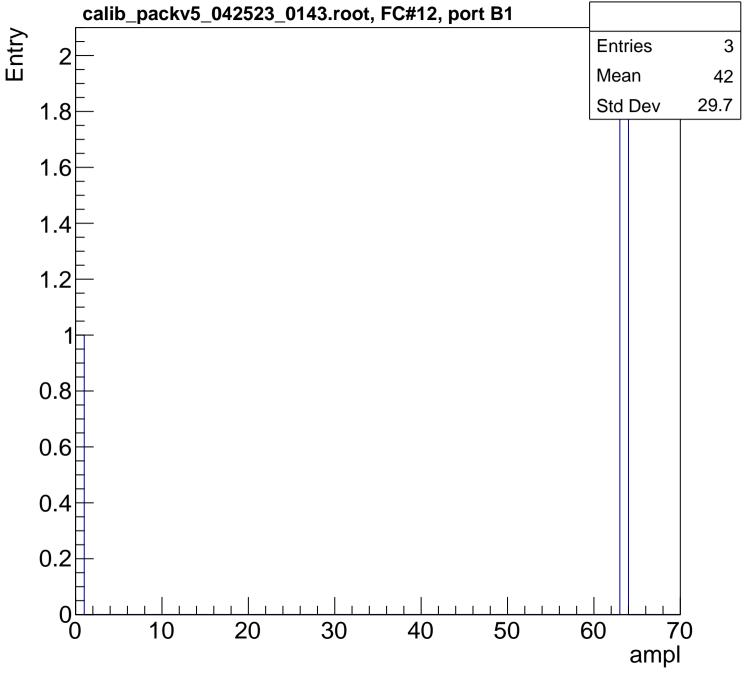


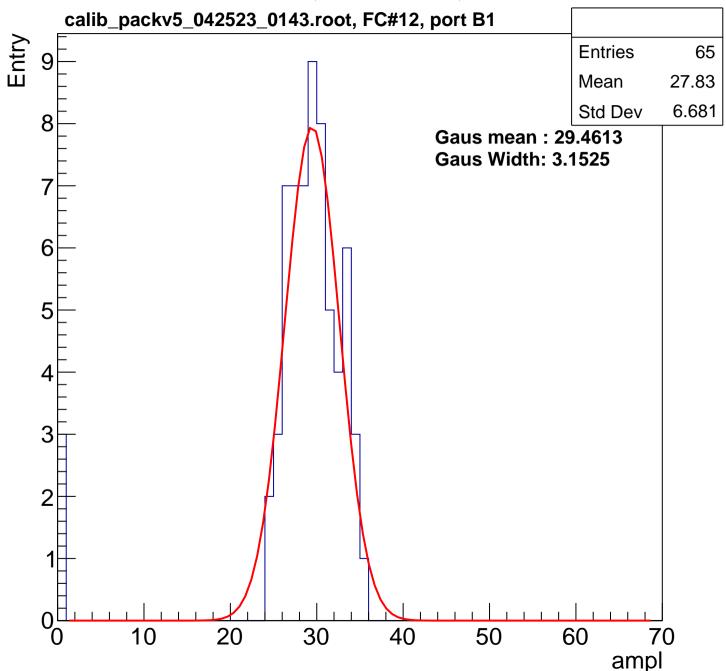


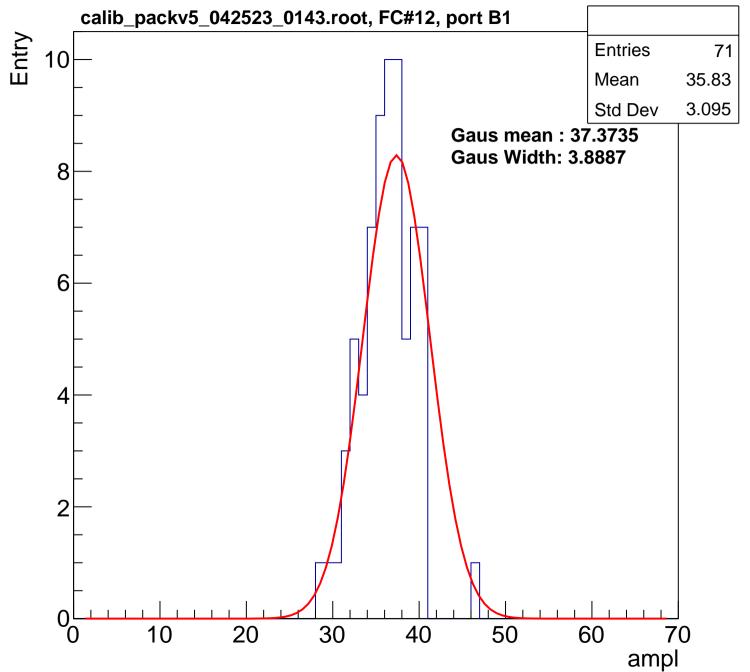


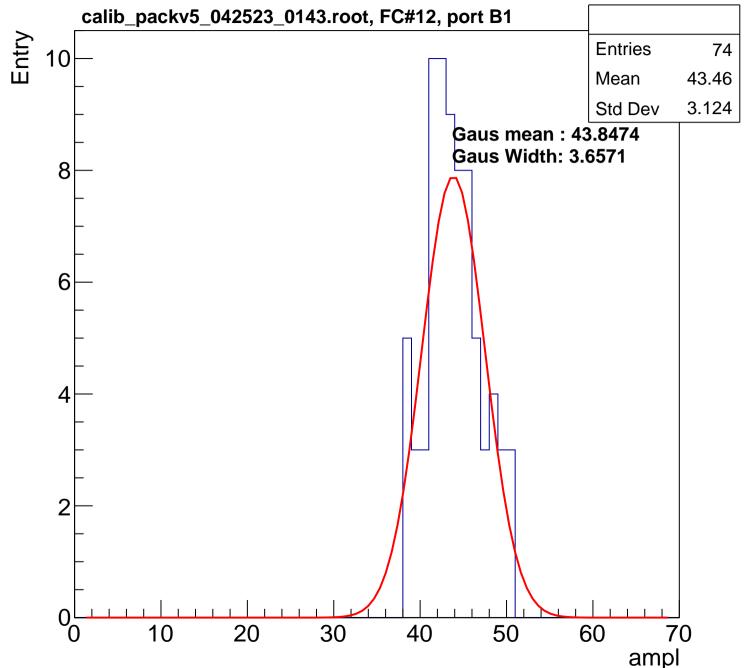


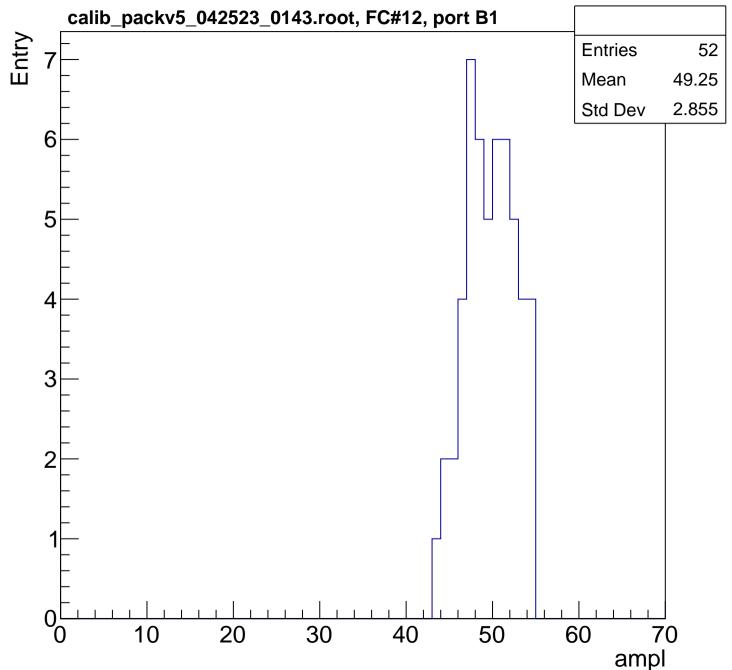


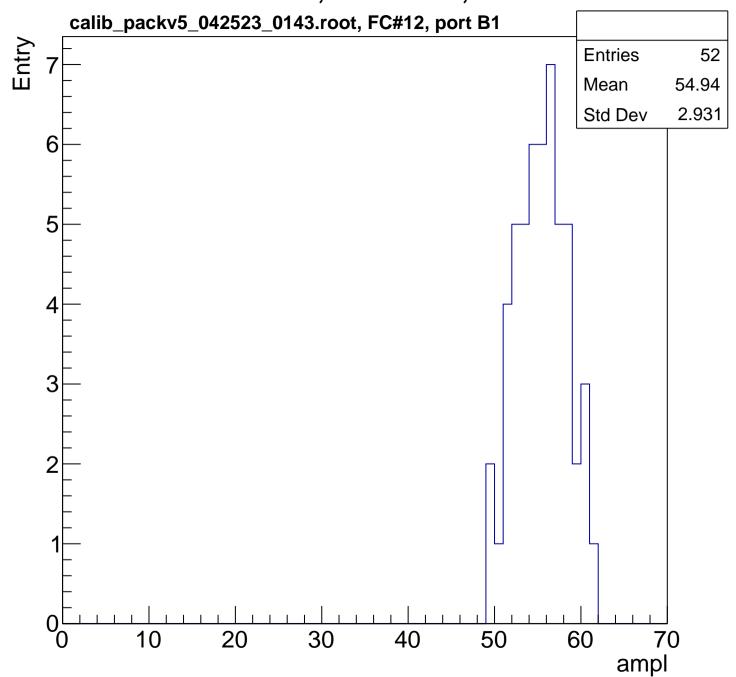


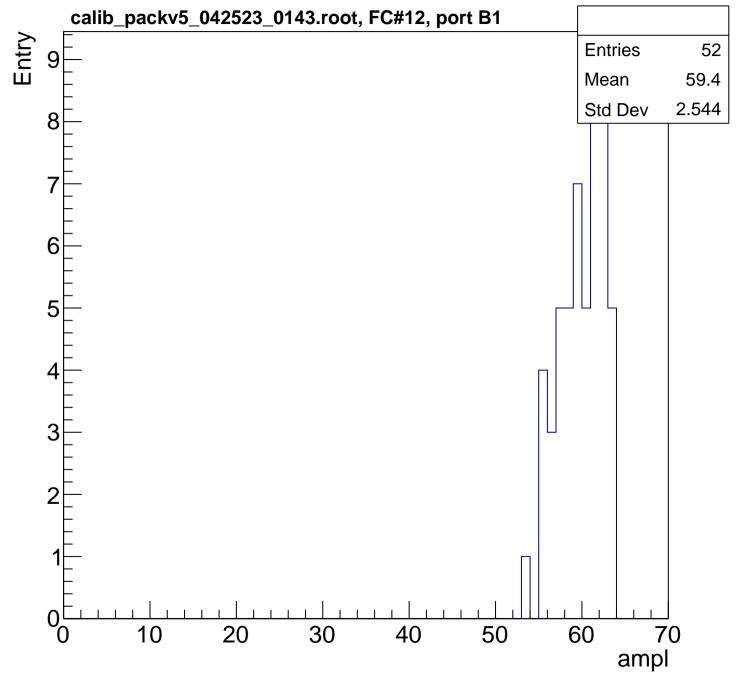


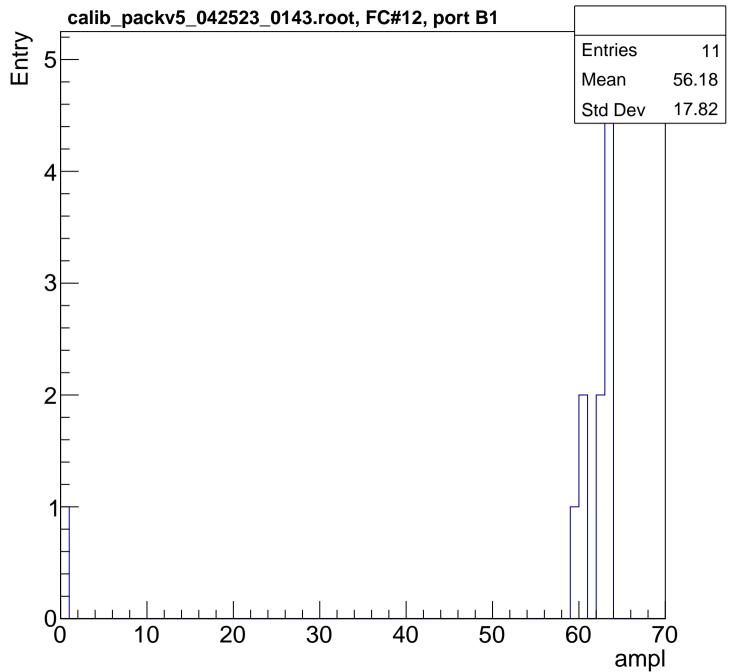




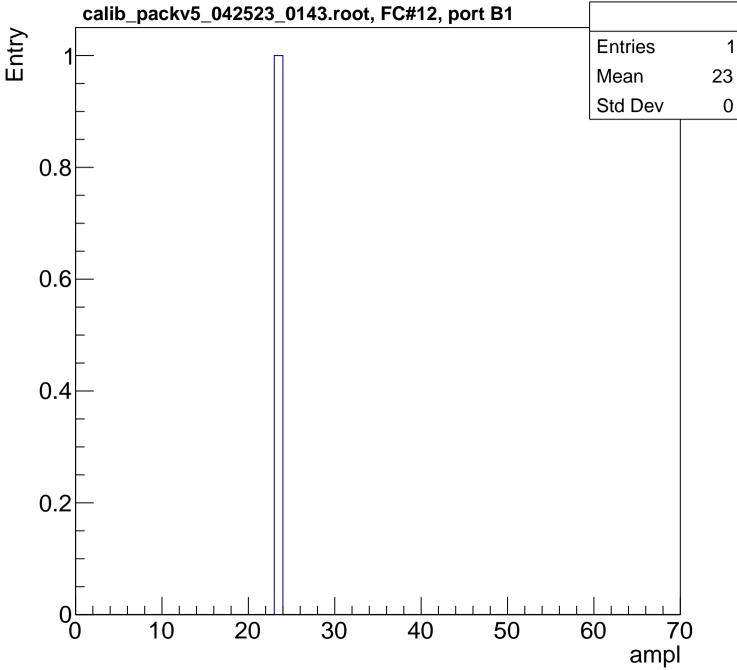


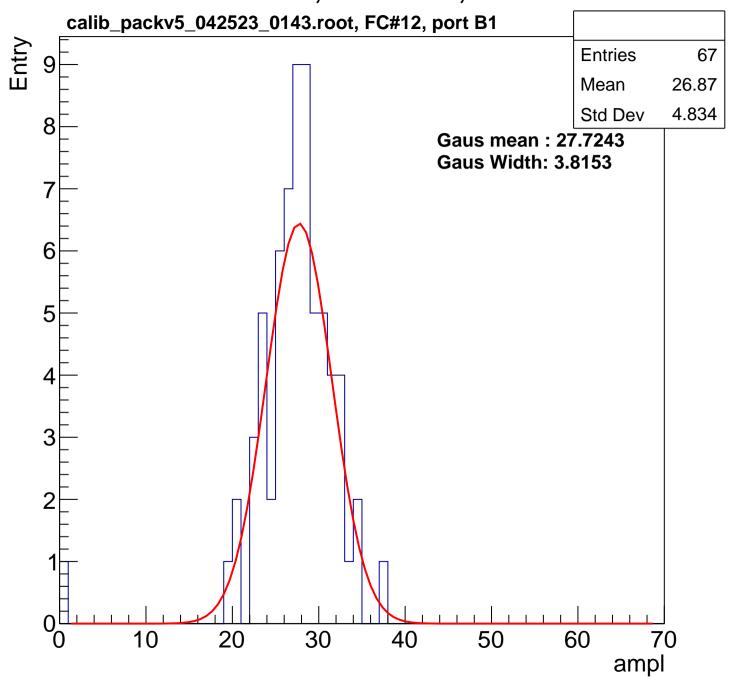


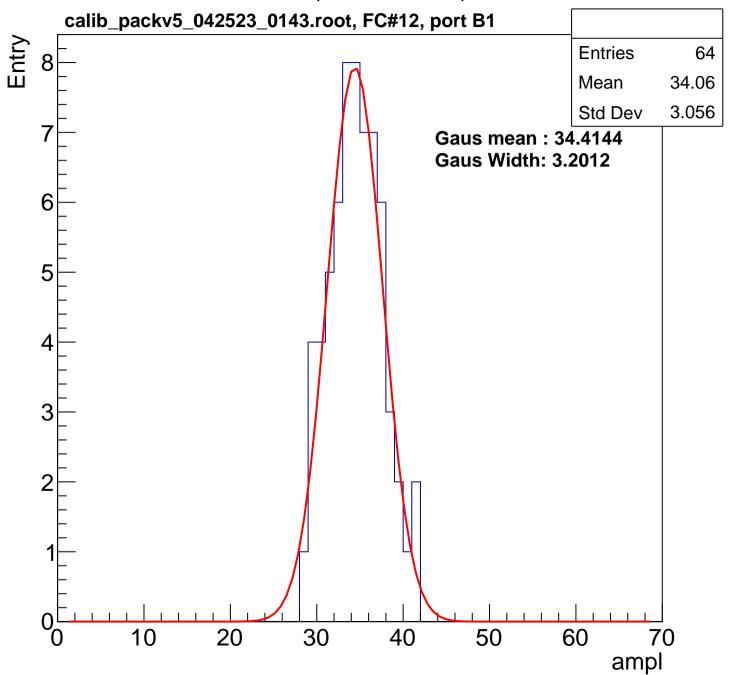


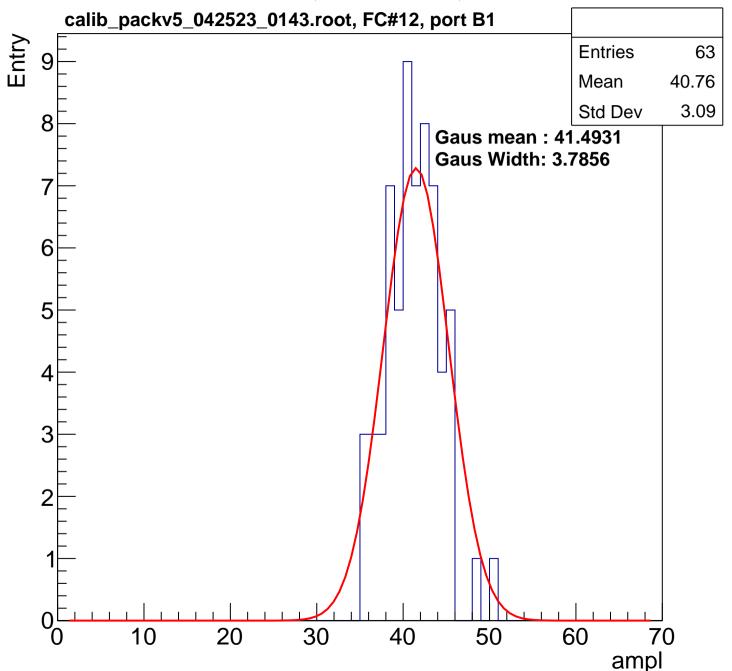


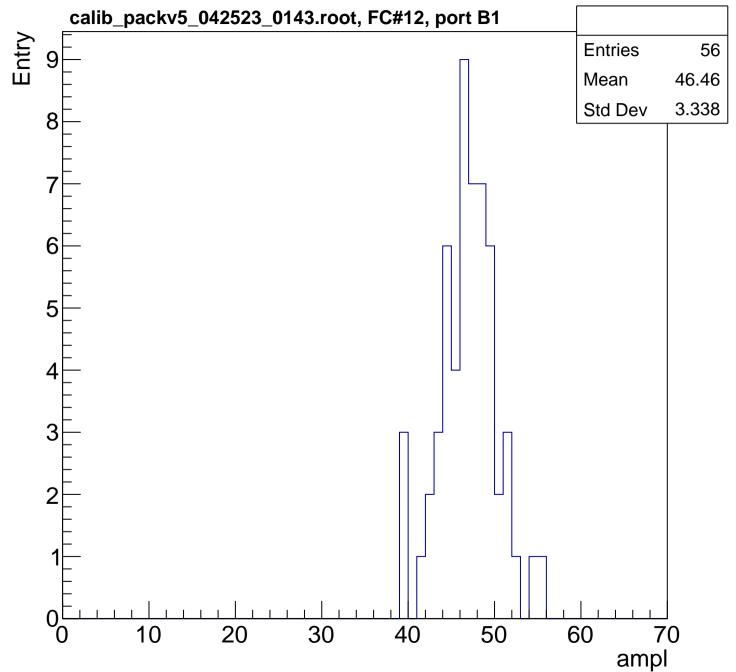
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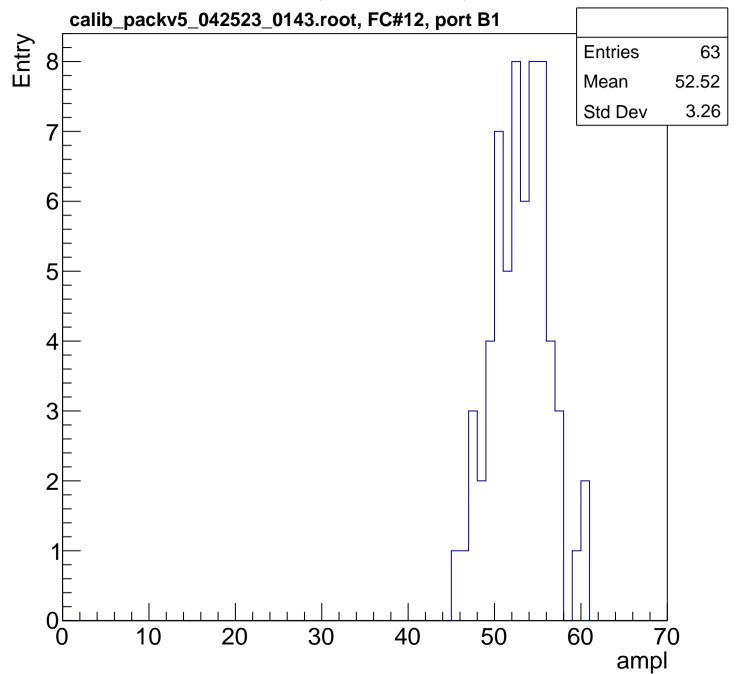


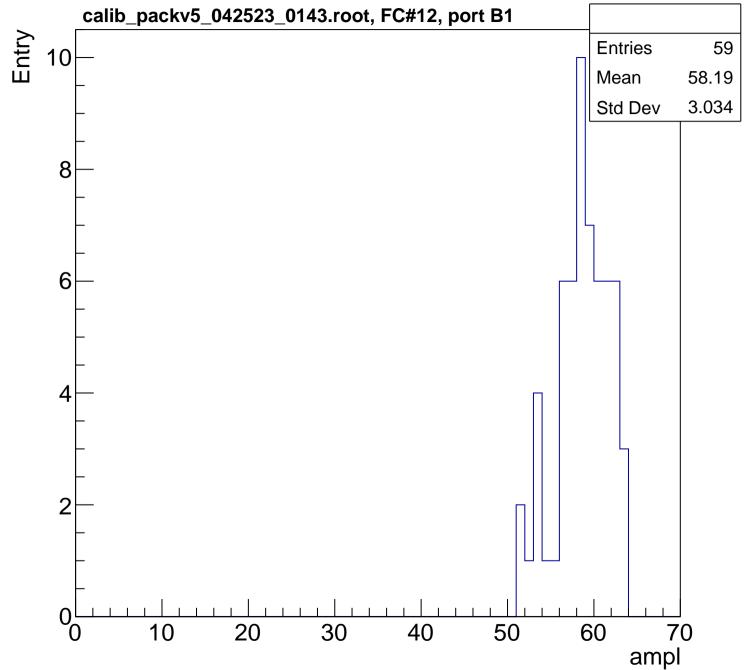


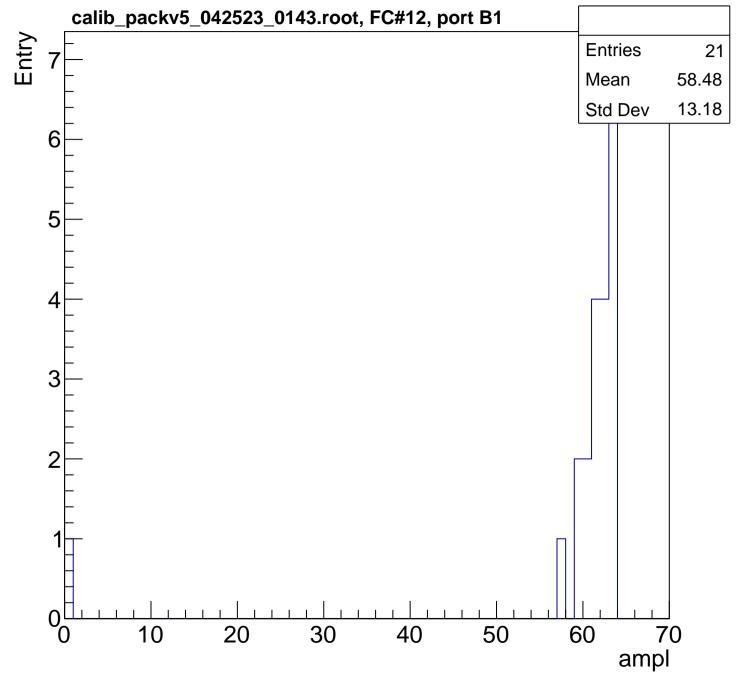




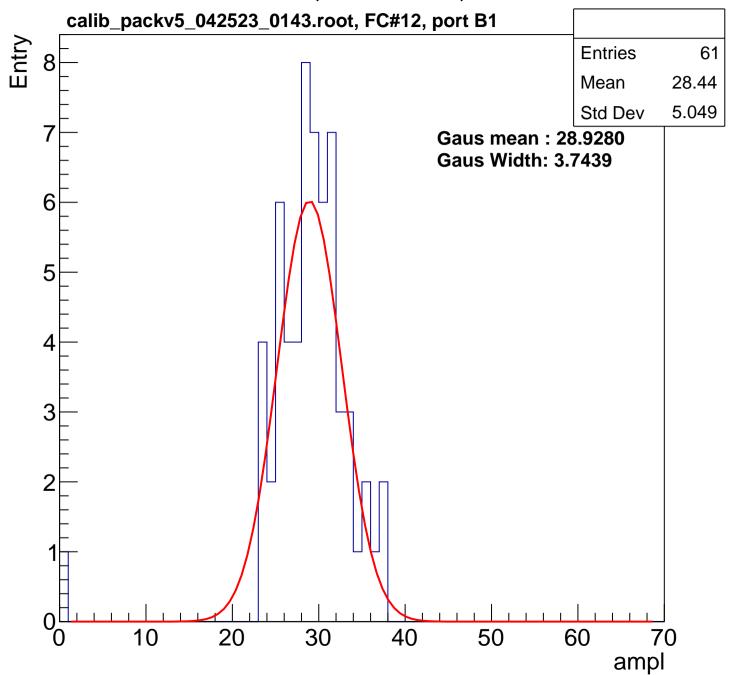


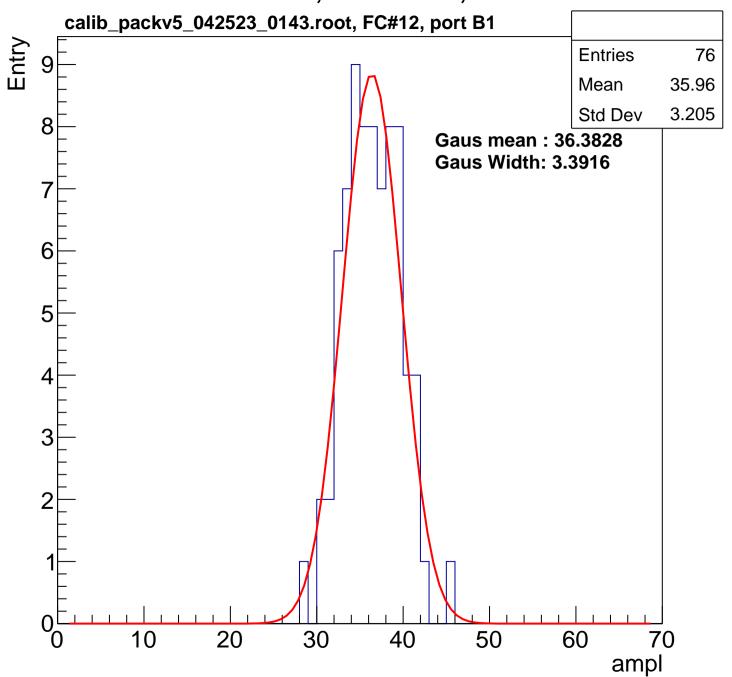


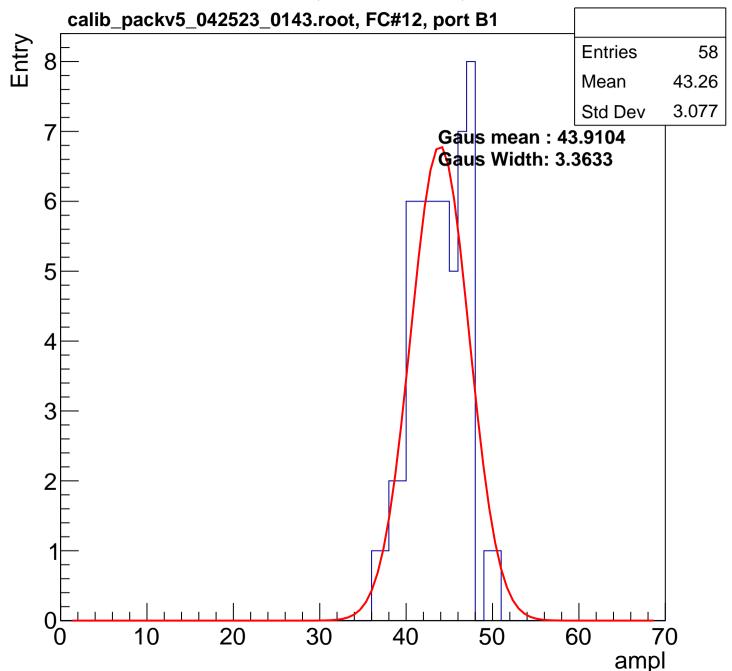


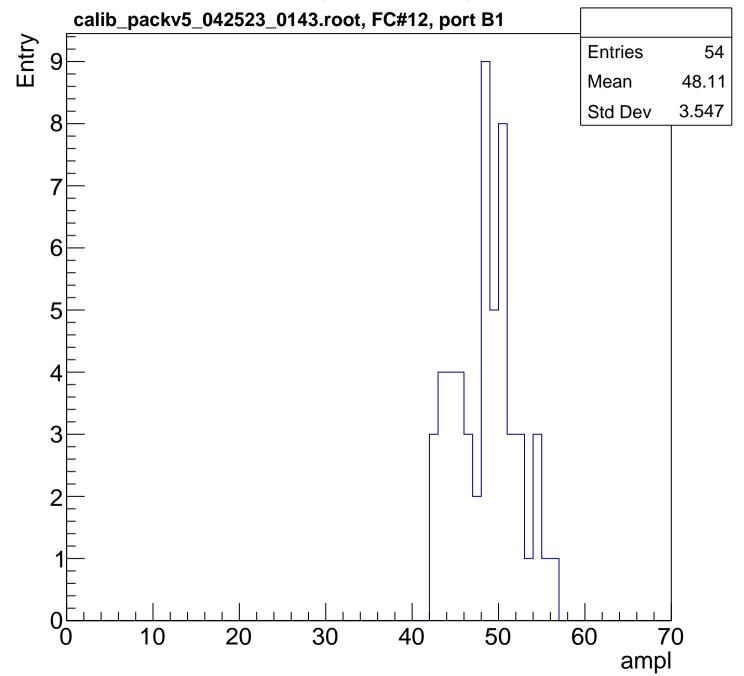


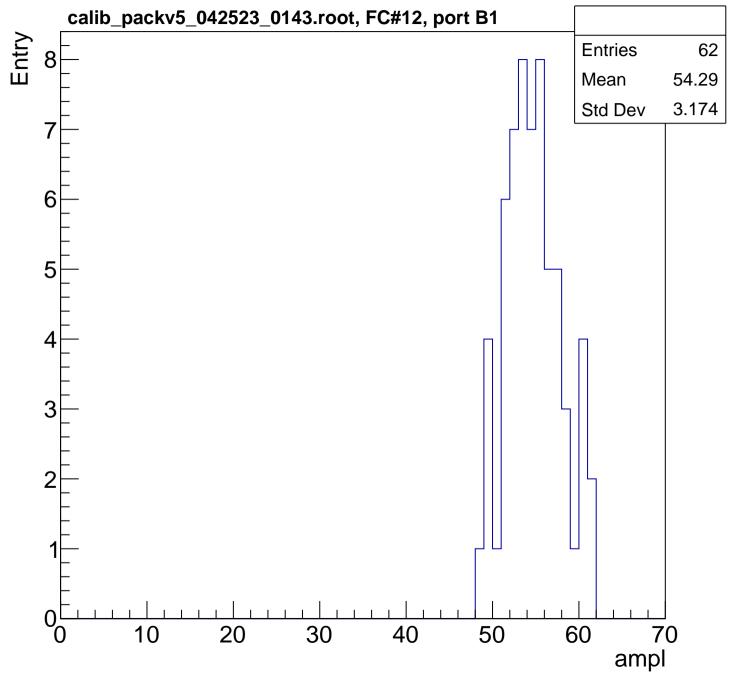
B0L102S, U2-ch30, adc7 calib_packv5_042523_0143.root, FC#12, port B1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

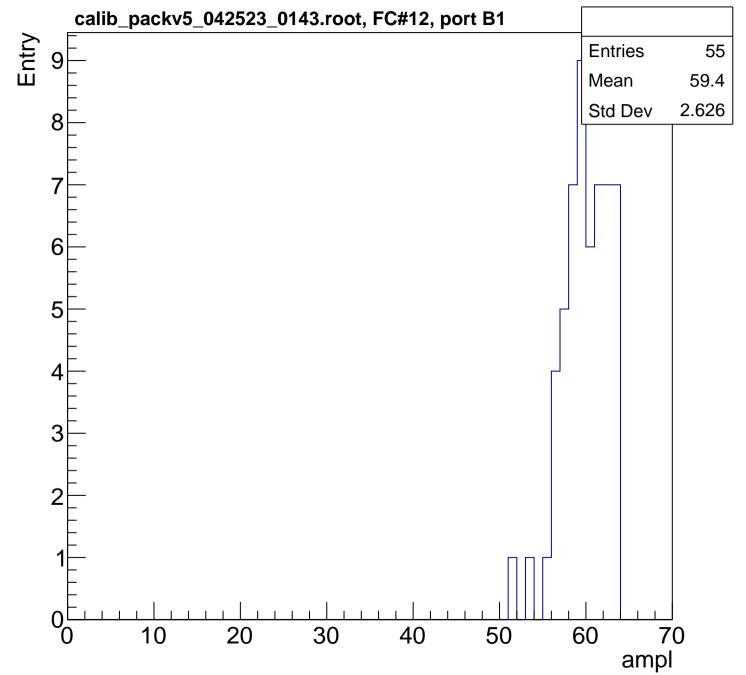


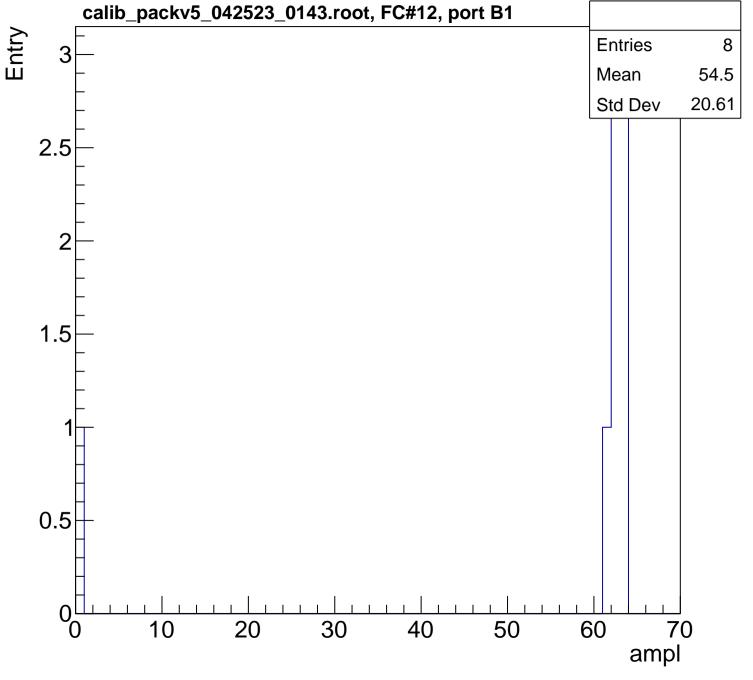


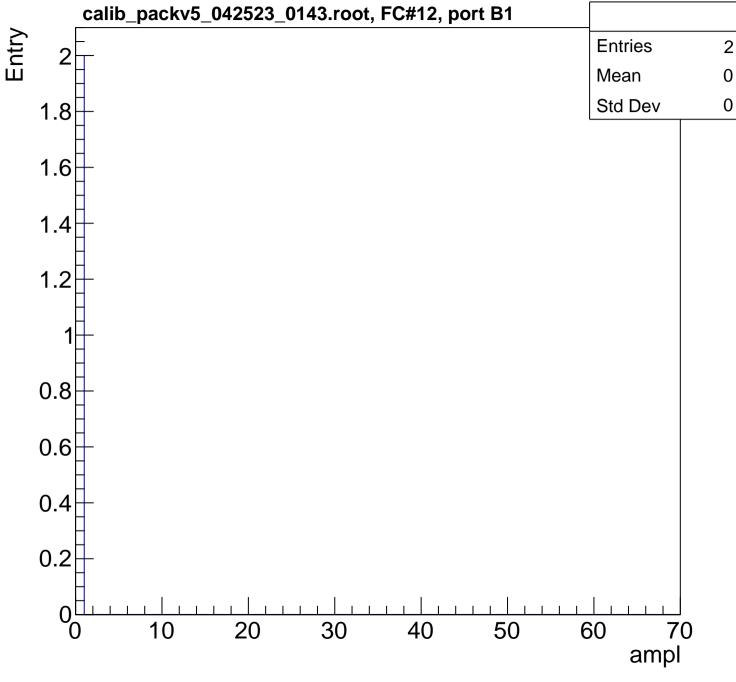


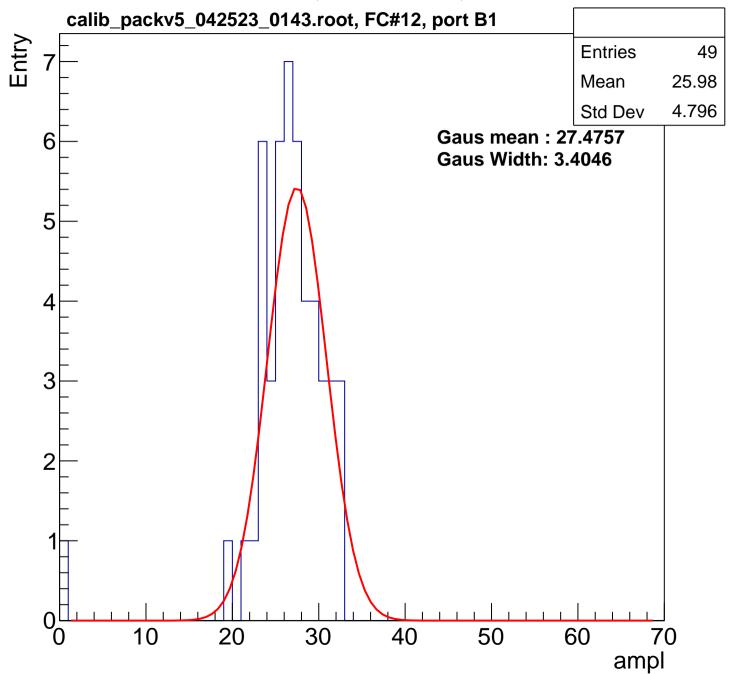


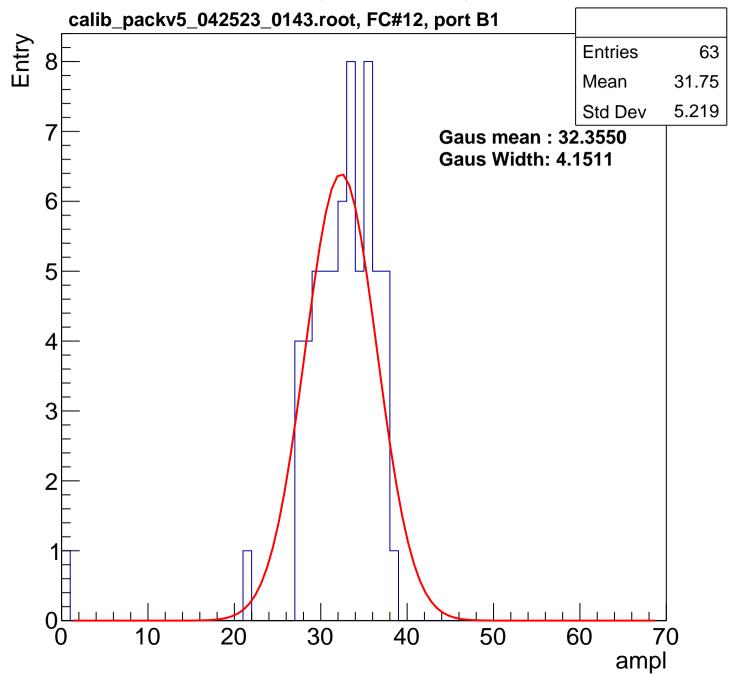


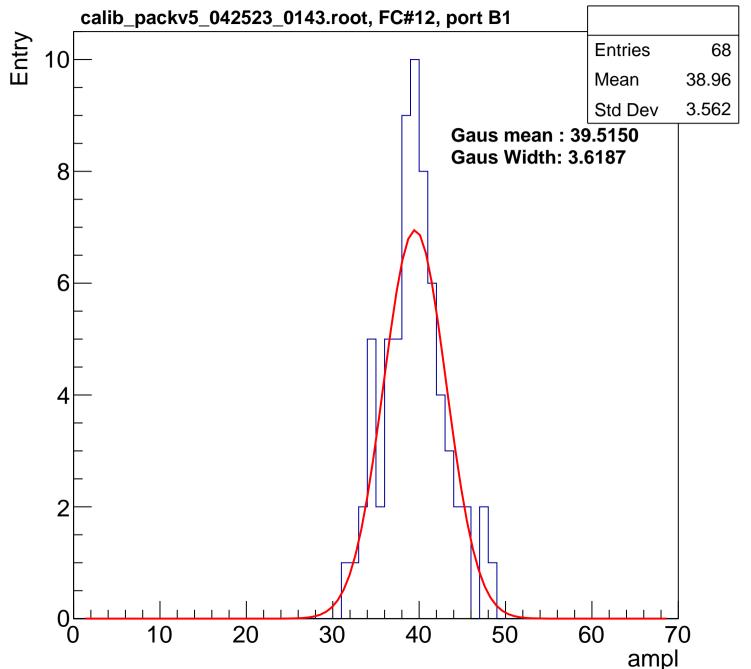


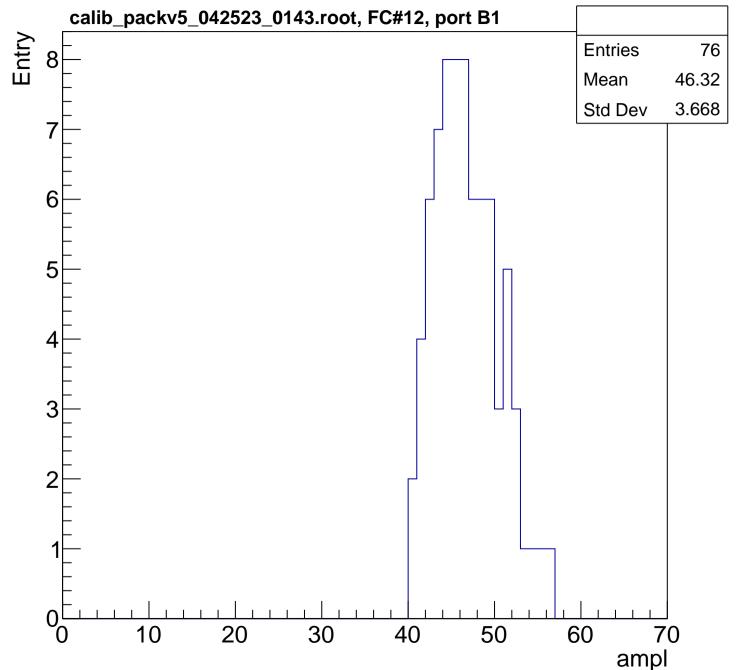


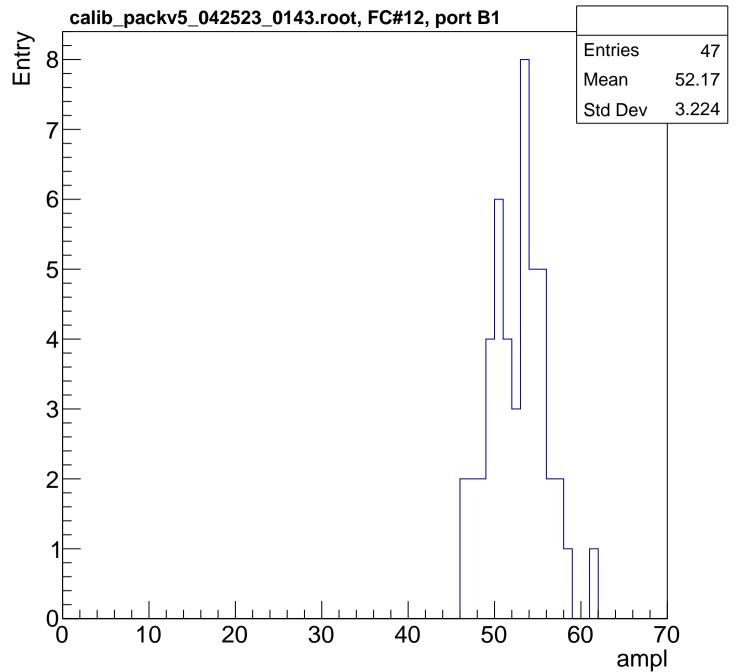


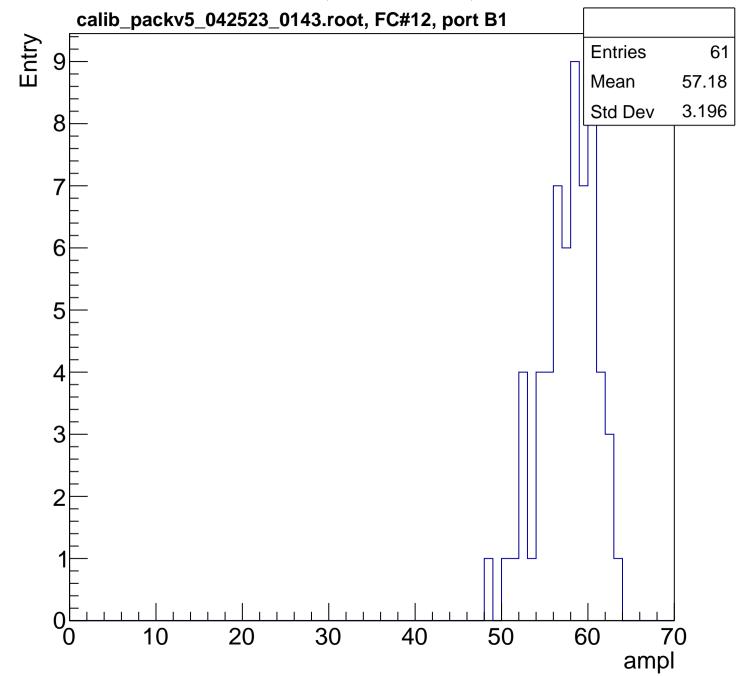


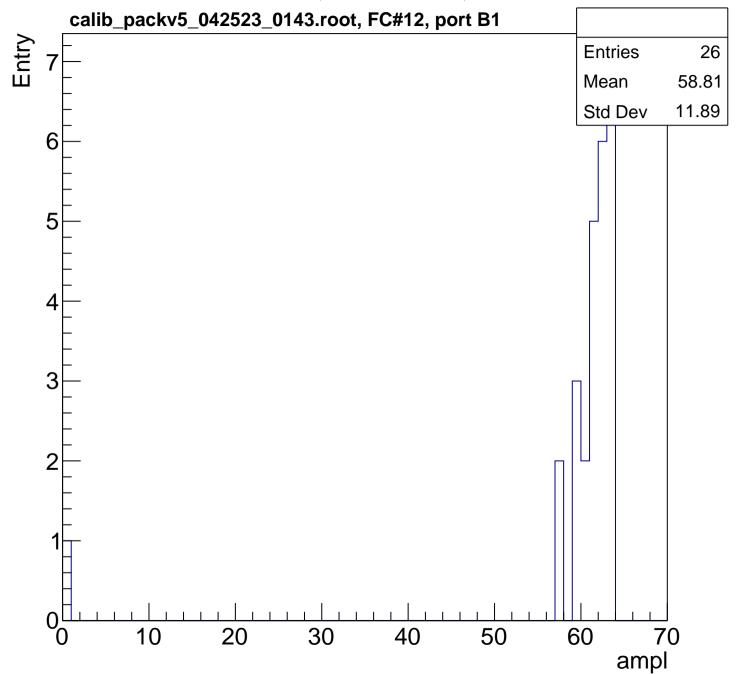


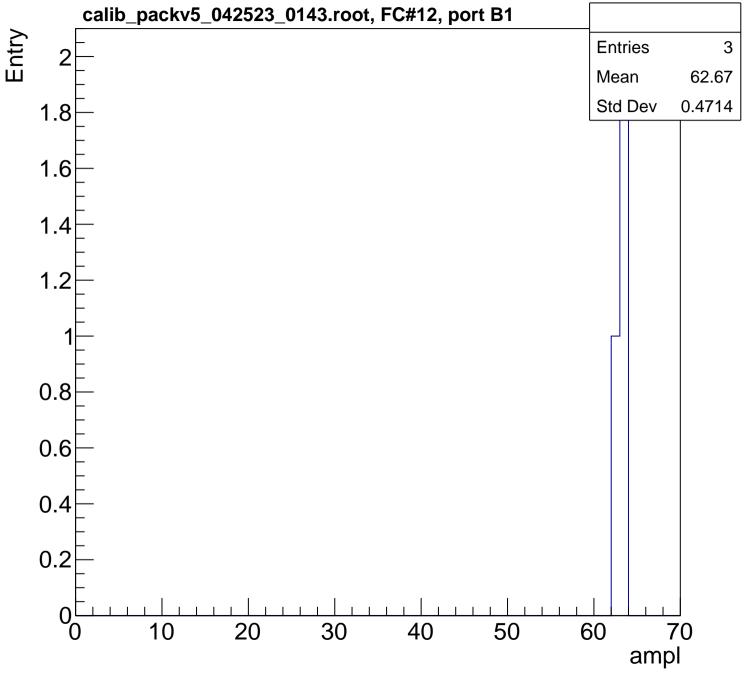


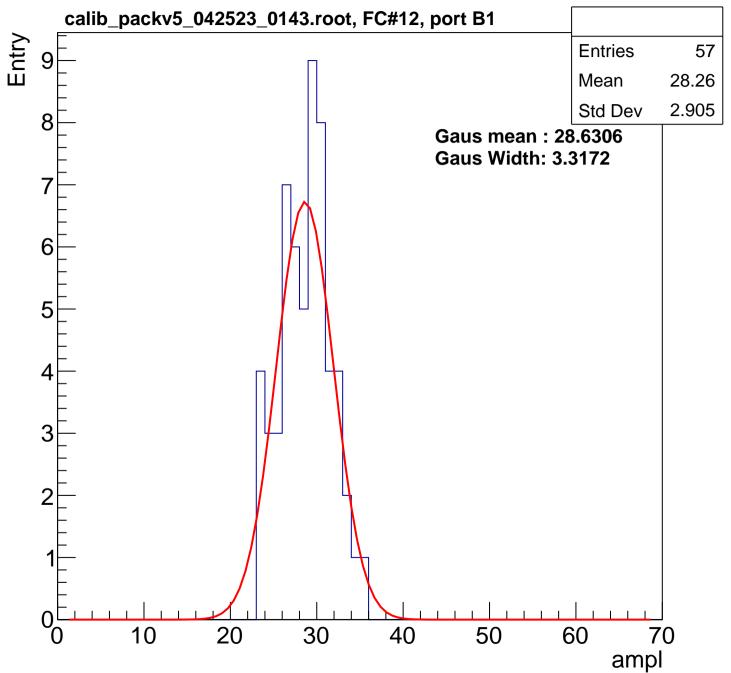


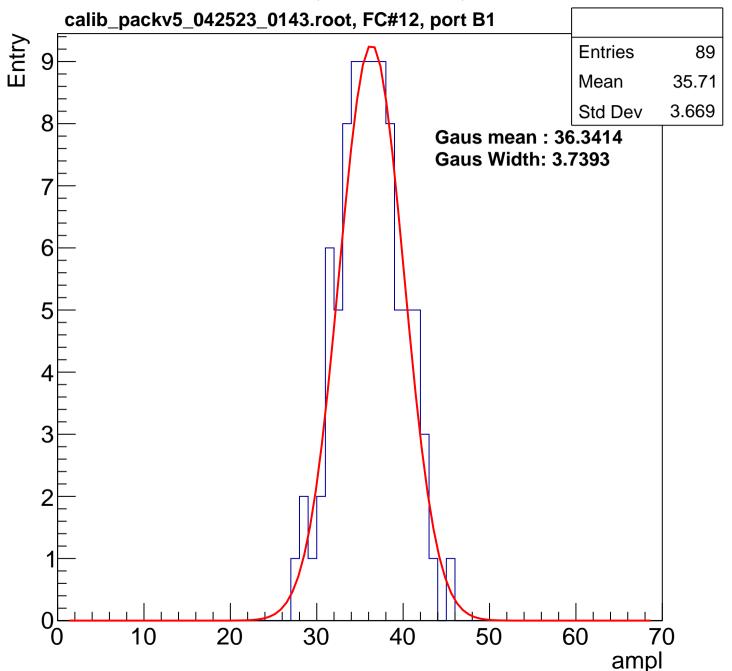


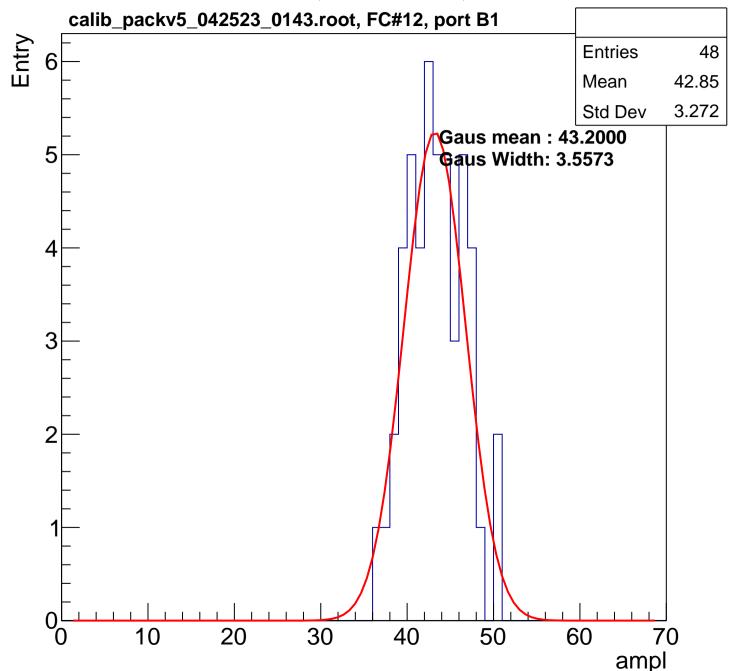


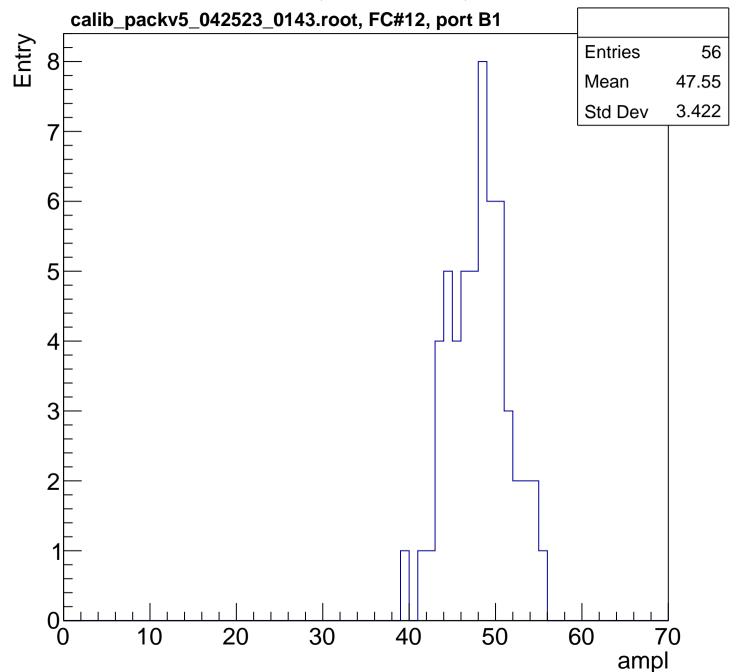


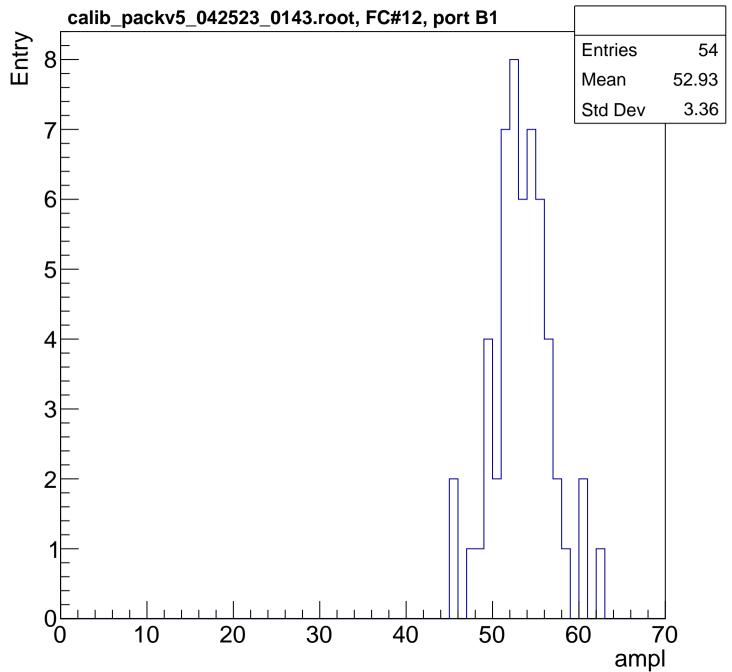


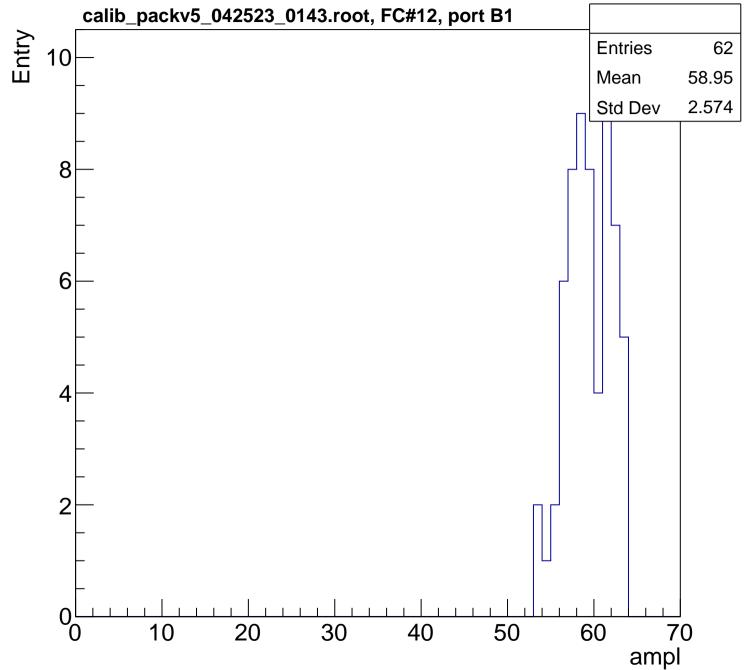


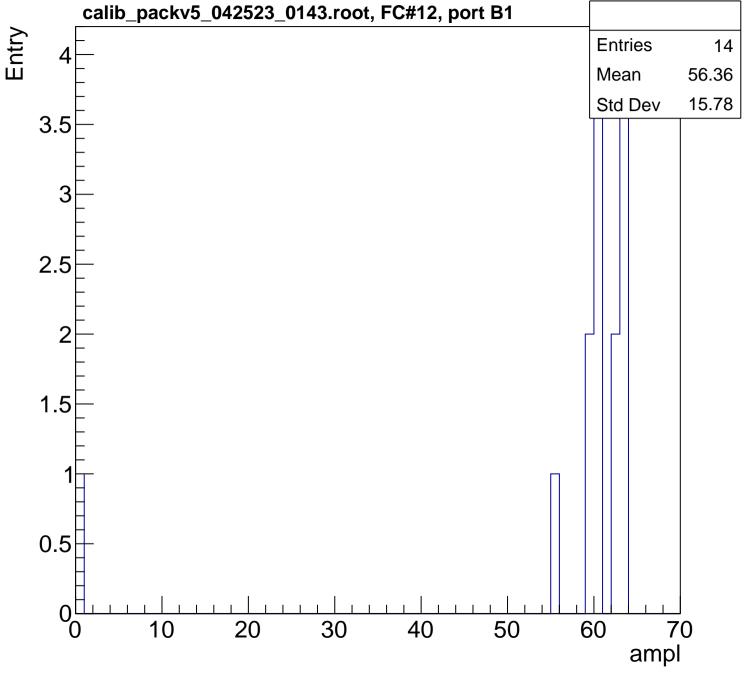


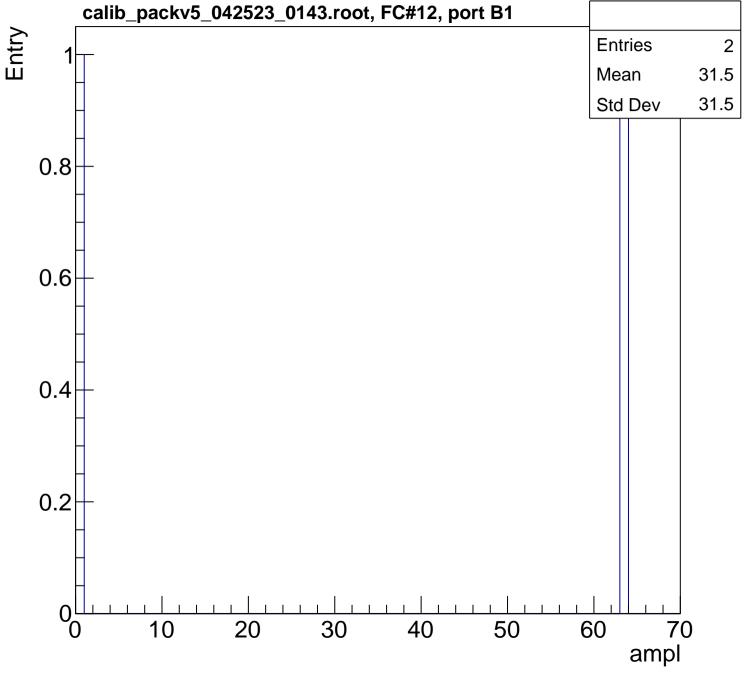


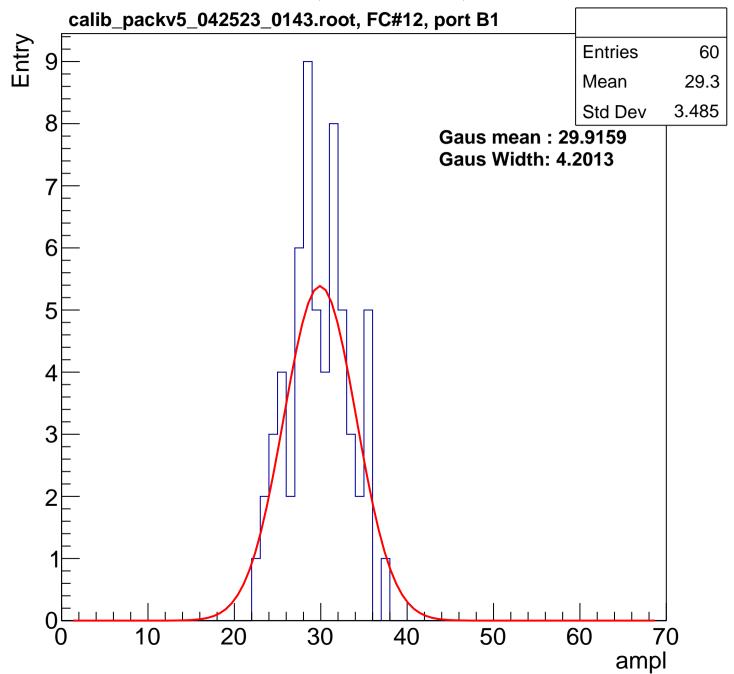


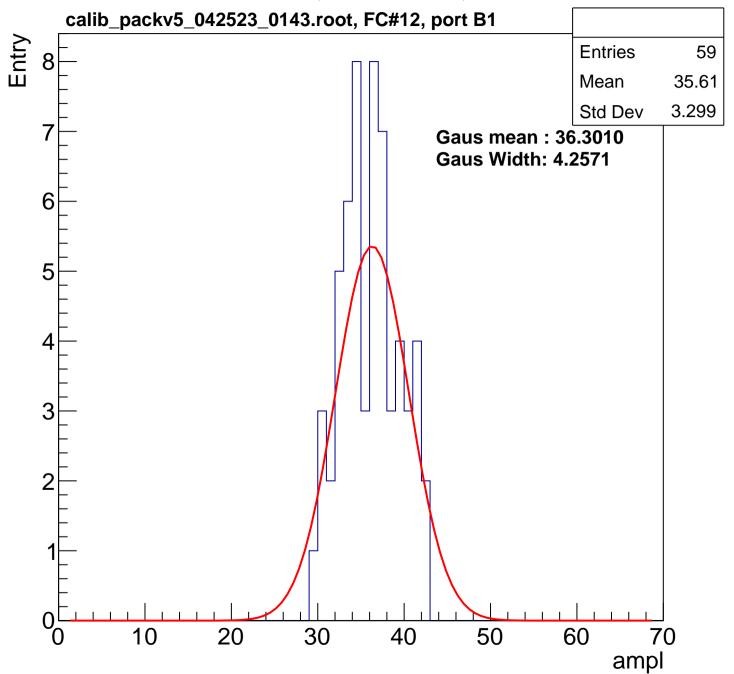


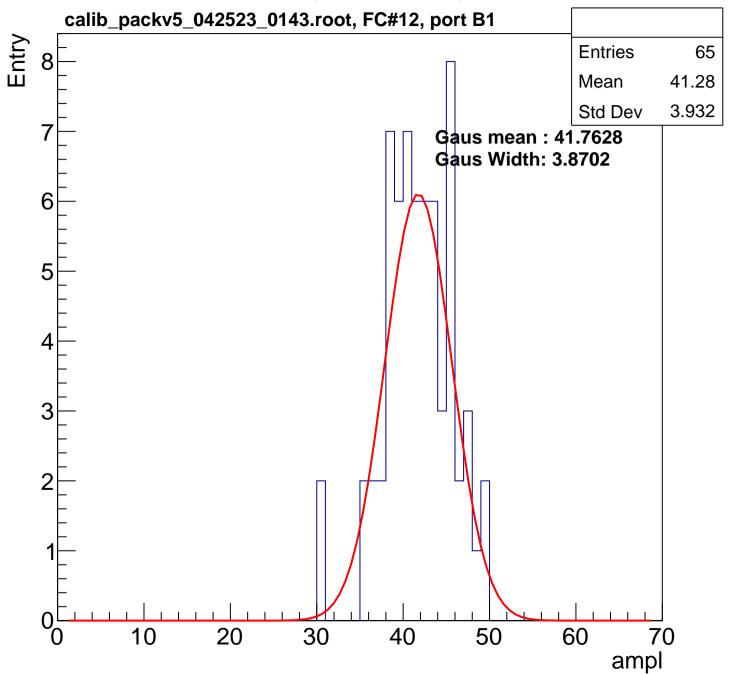


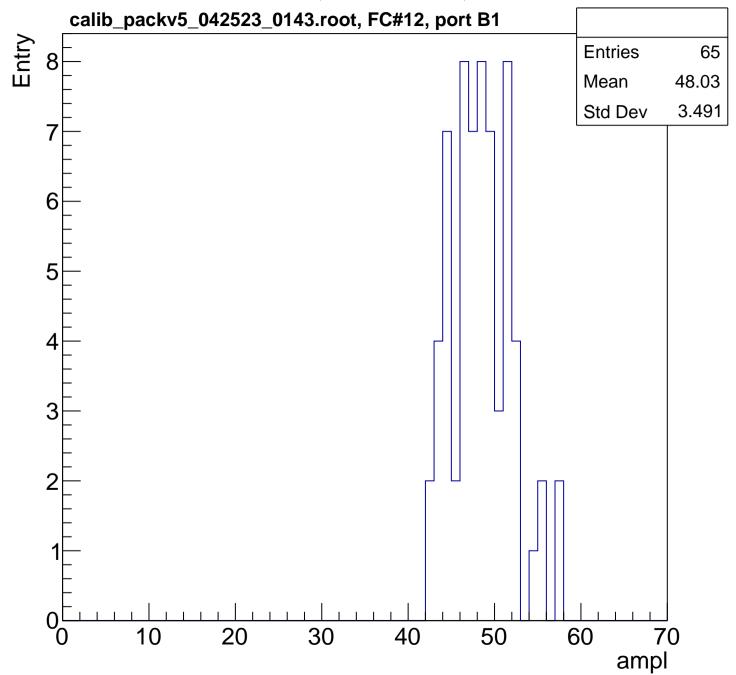


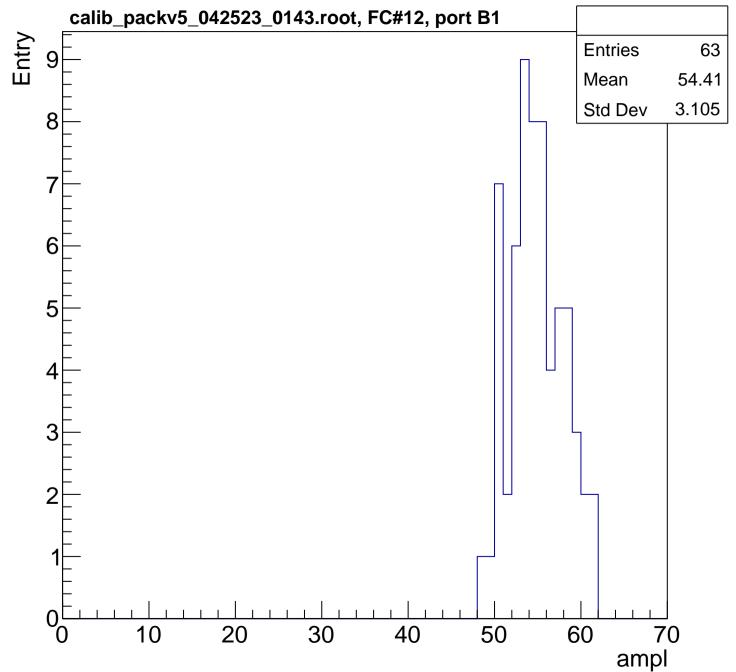


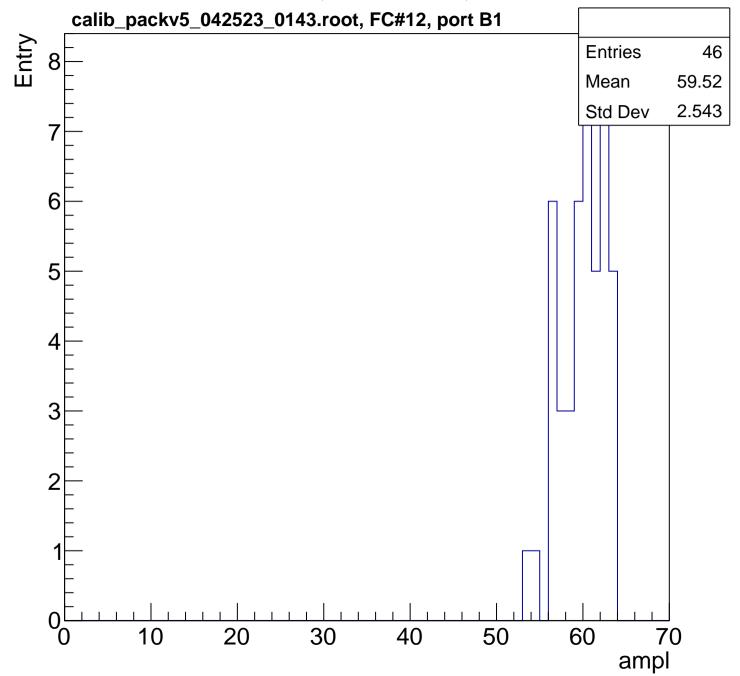


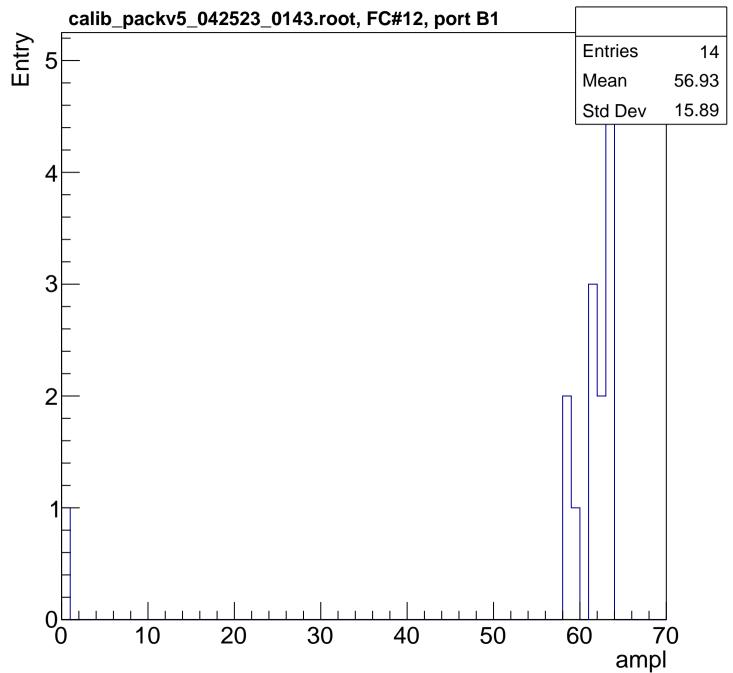




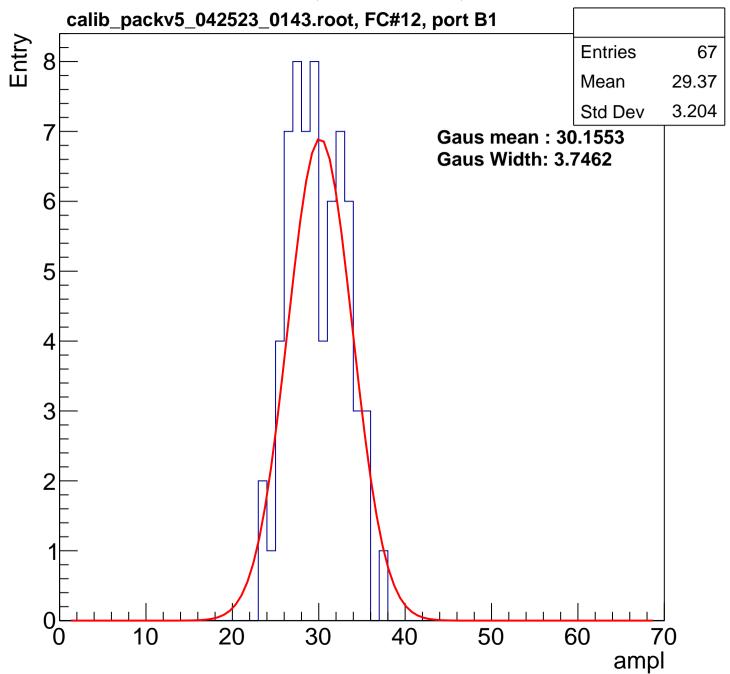


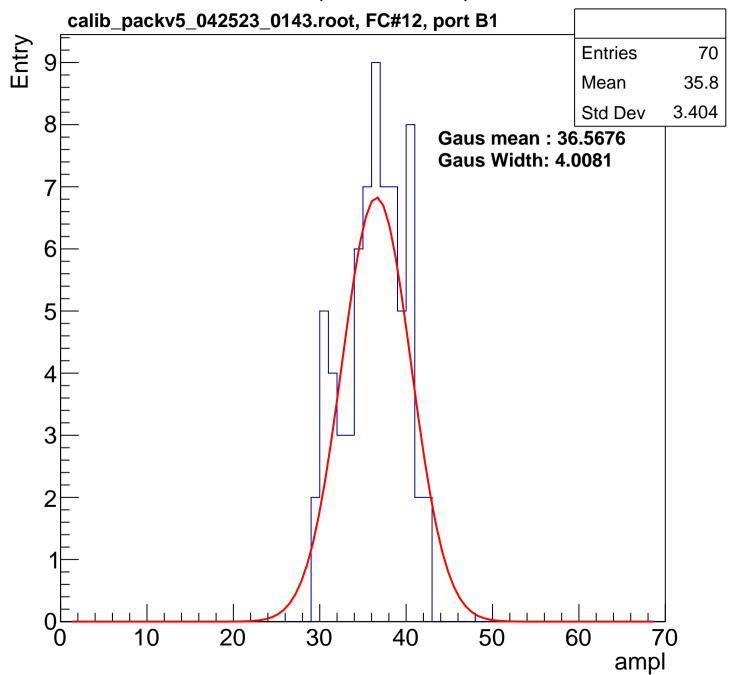


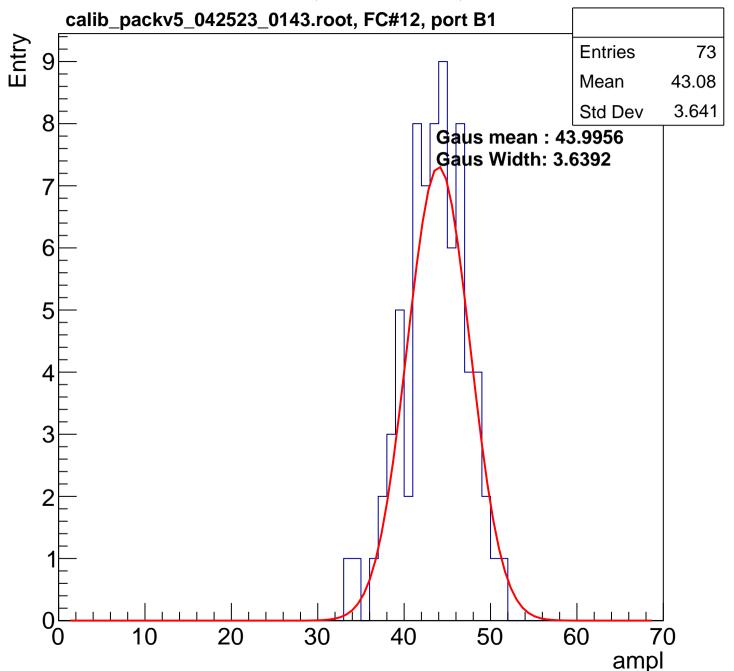


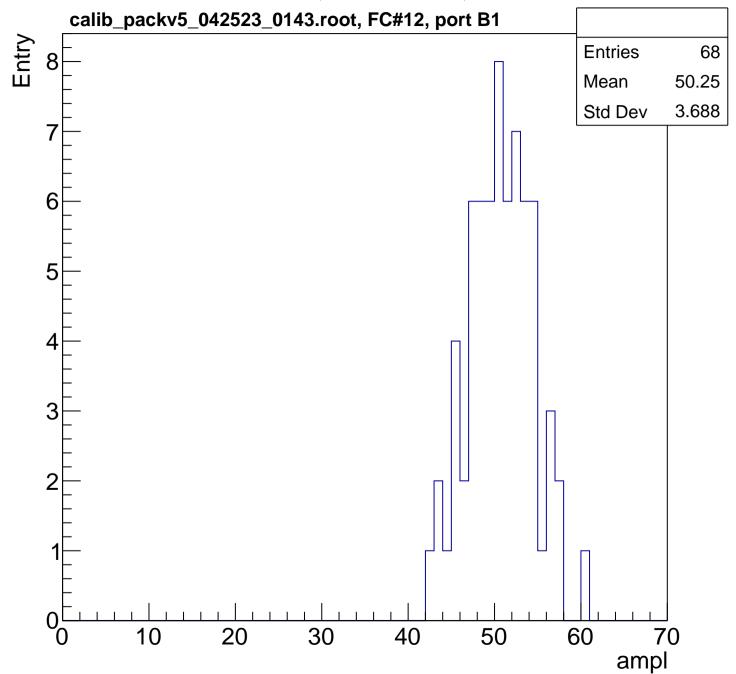


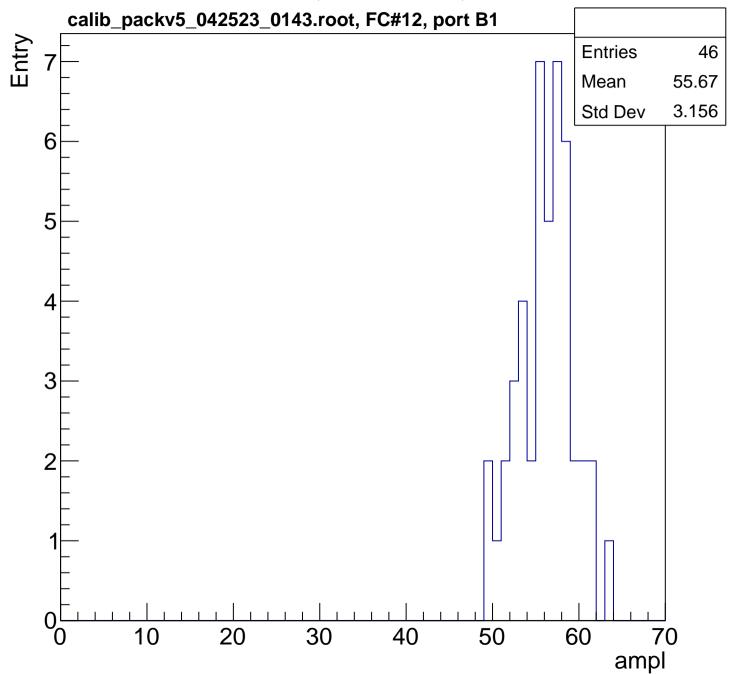


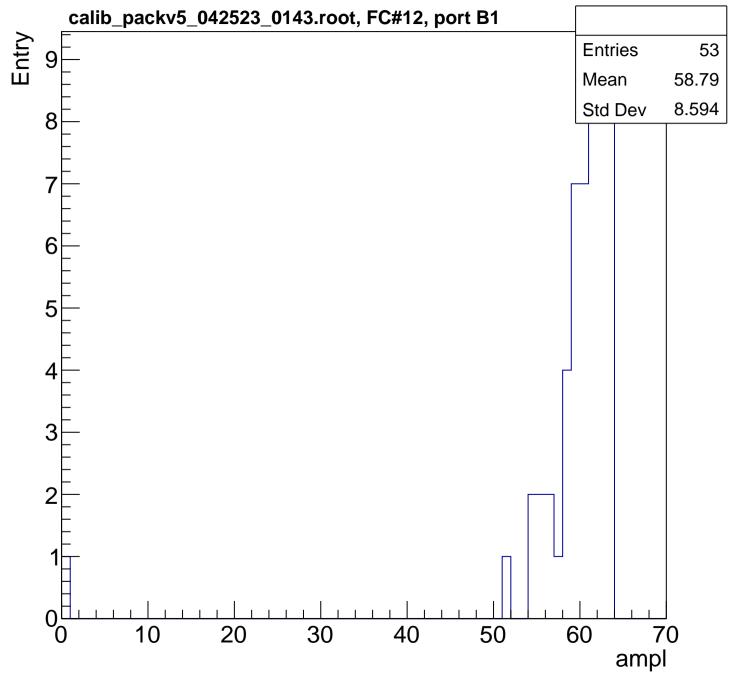


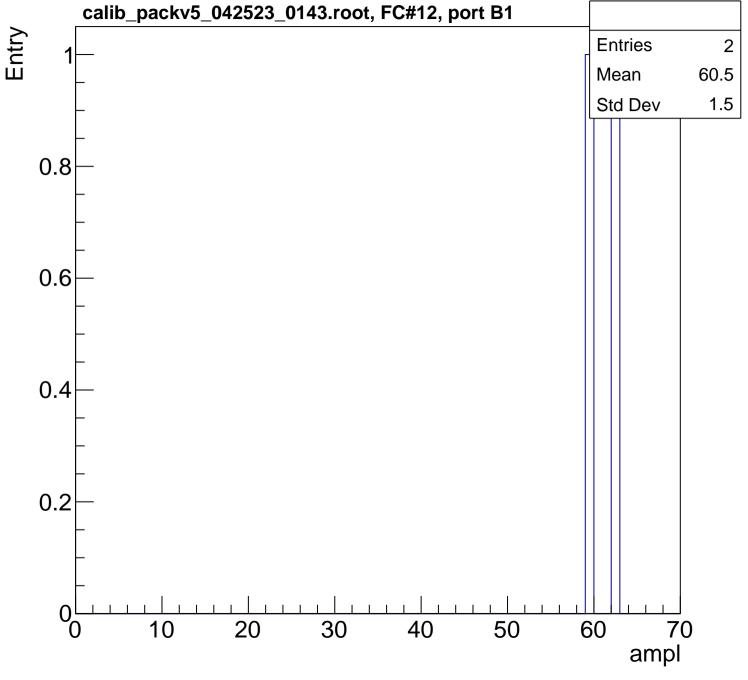




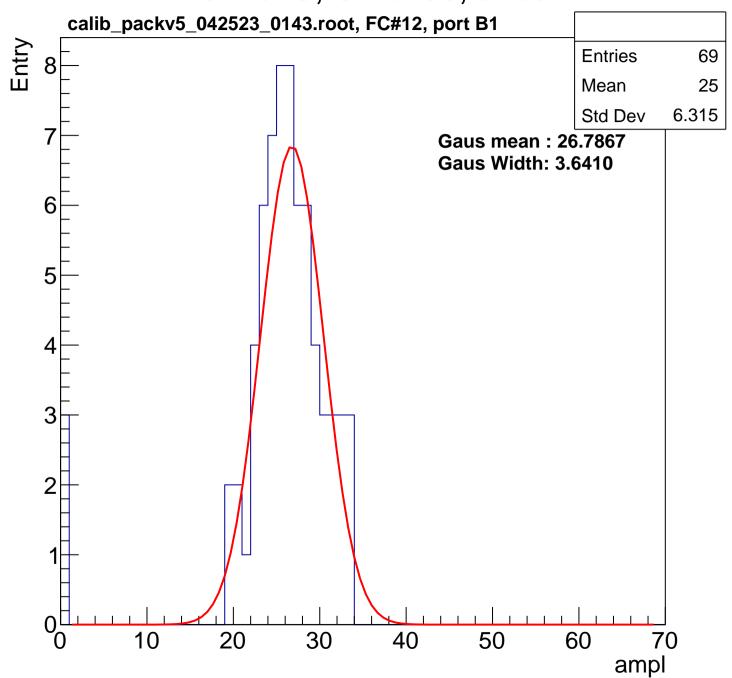


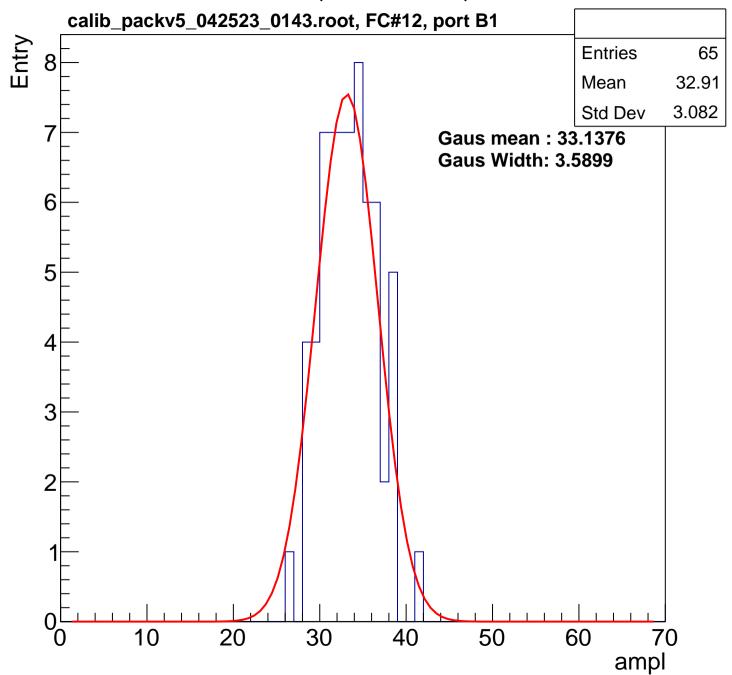


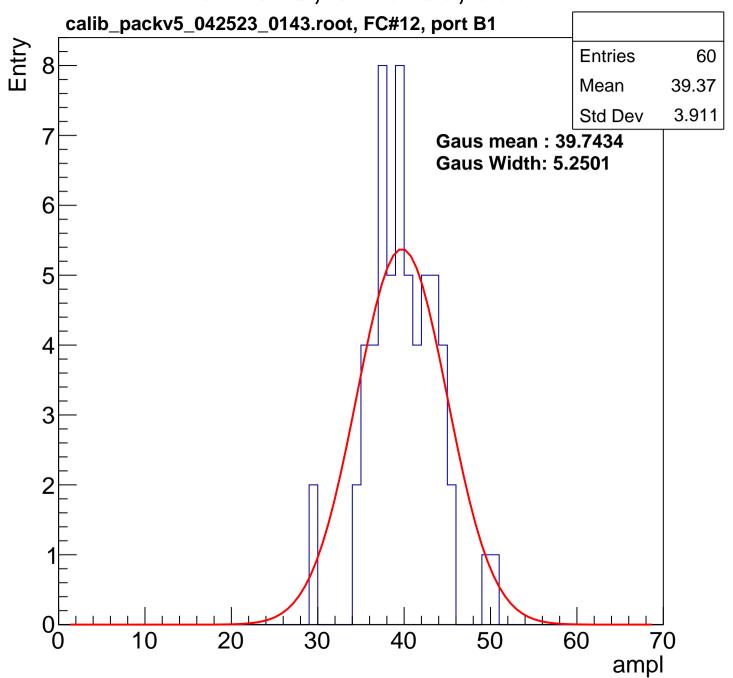


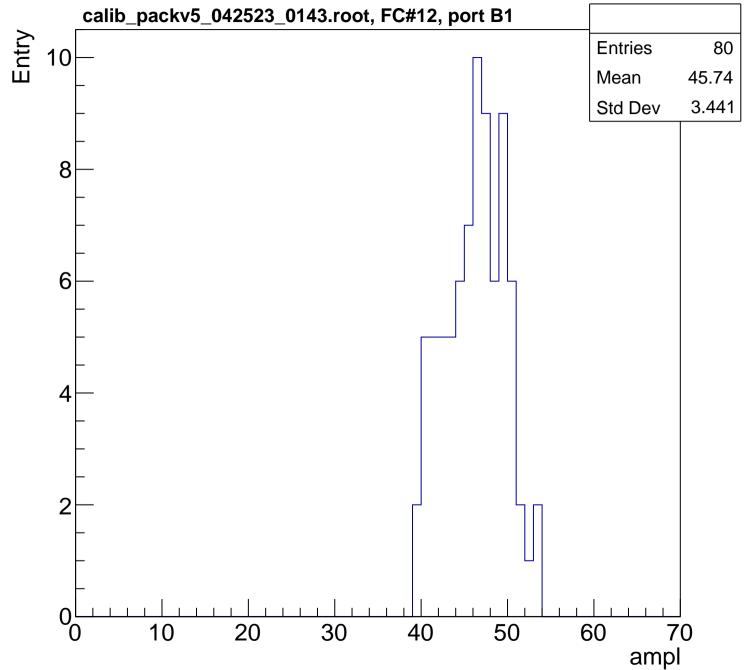


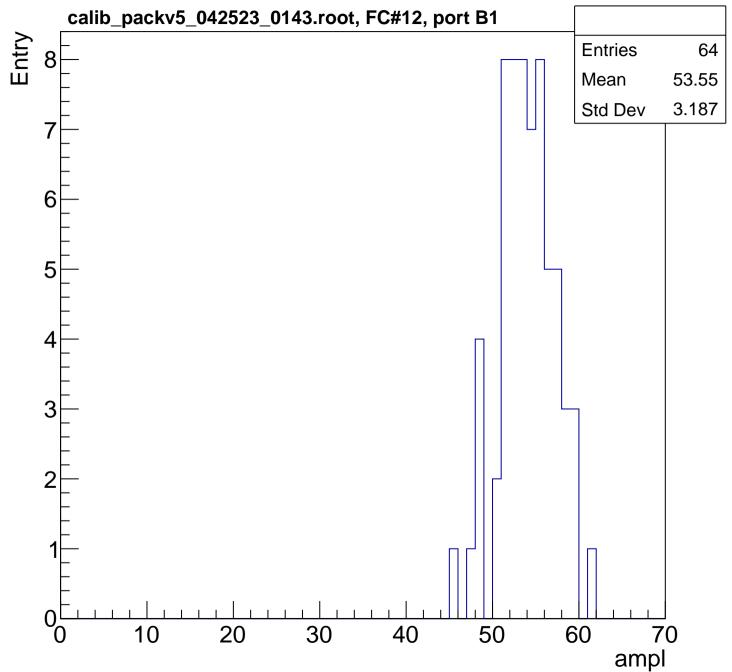
B0L102S, U2-ch35, adc7 calib_packv5_042523_0143.root, FC#12, port B1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

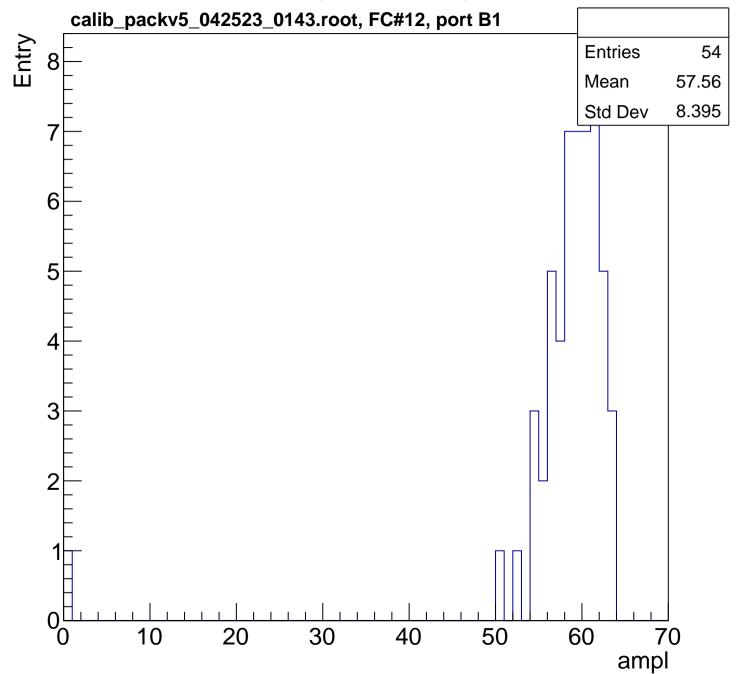


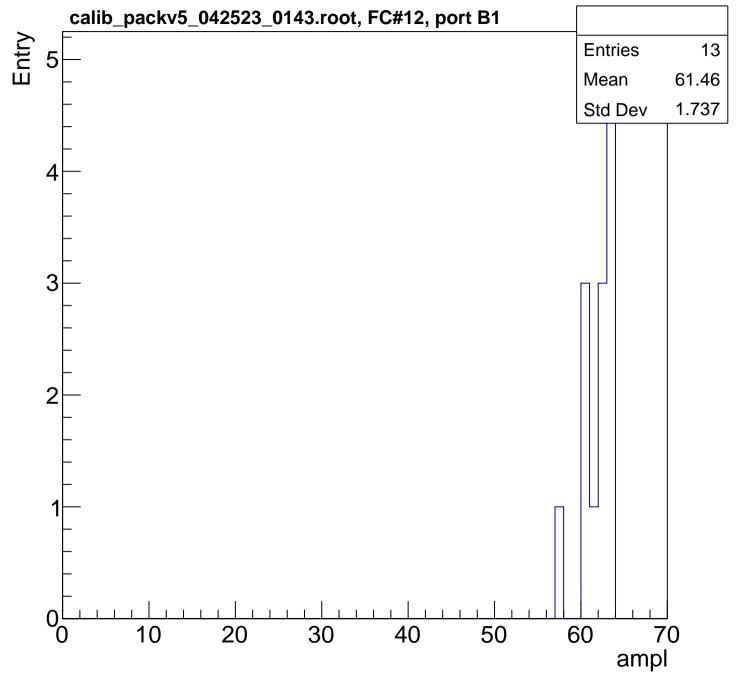


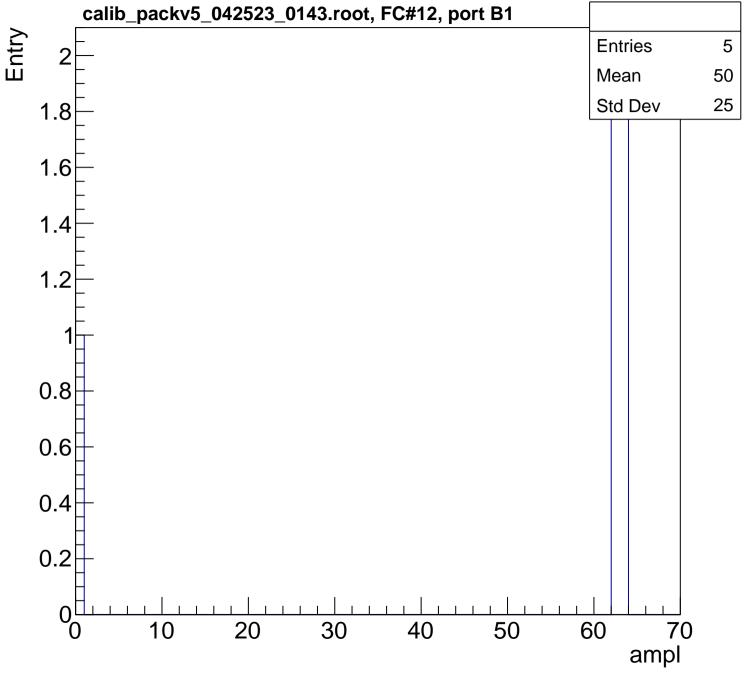


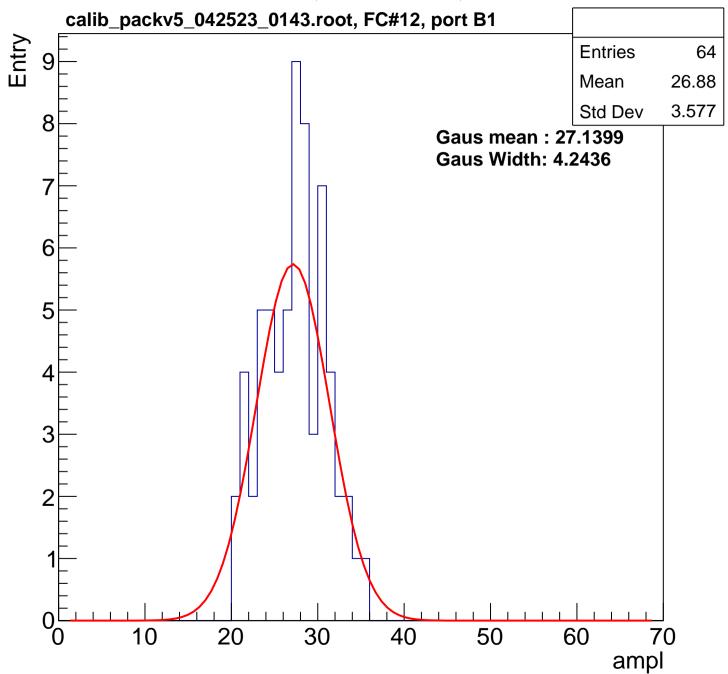


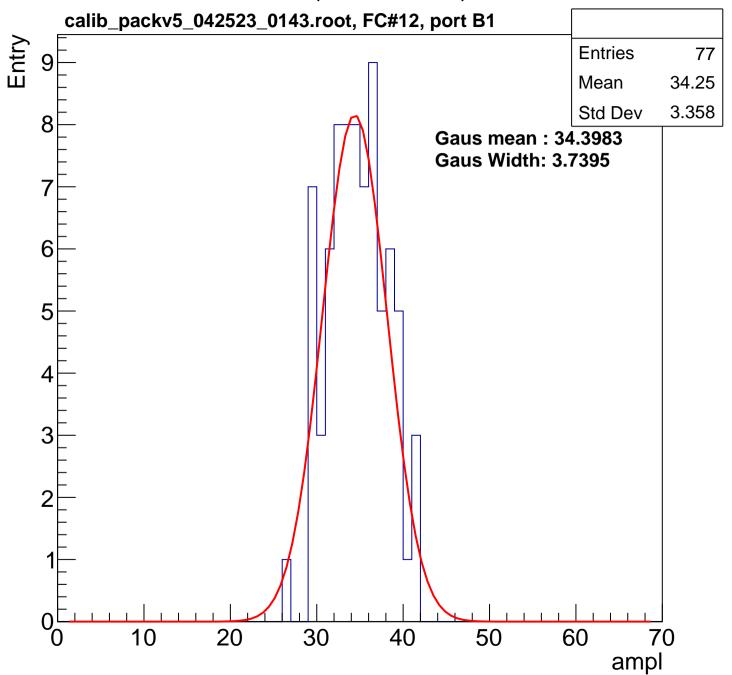


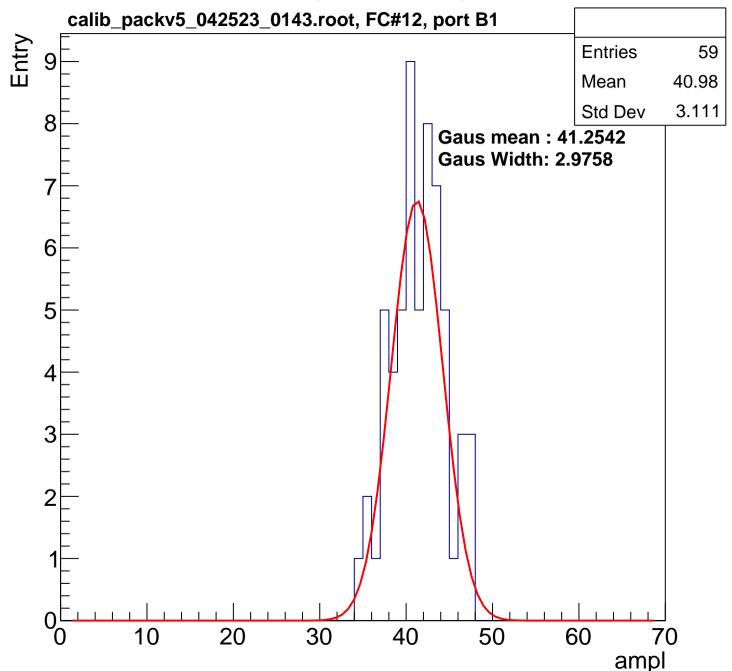


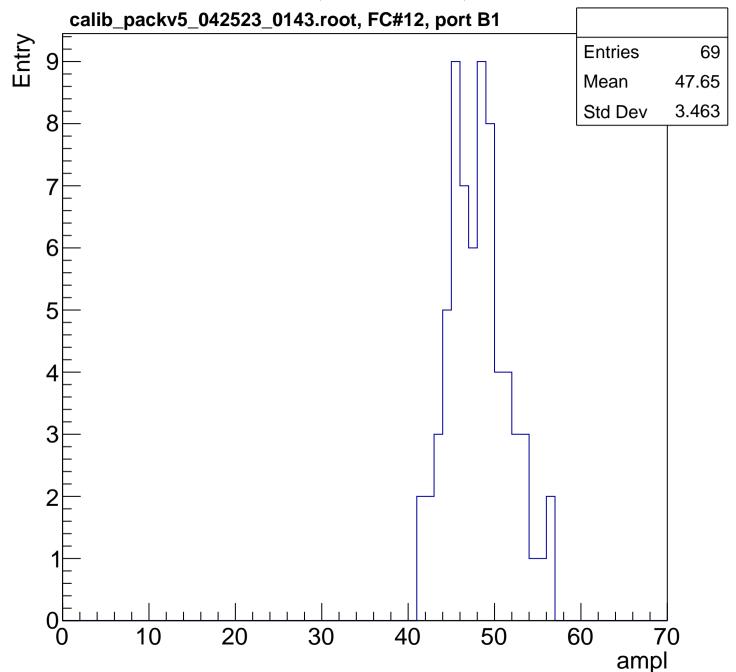


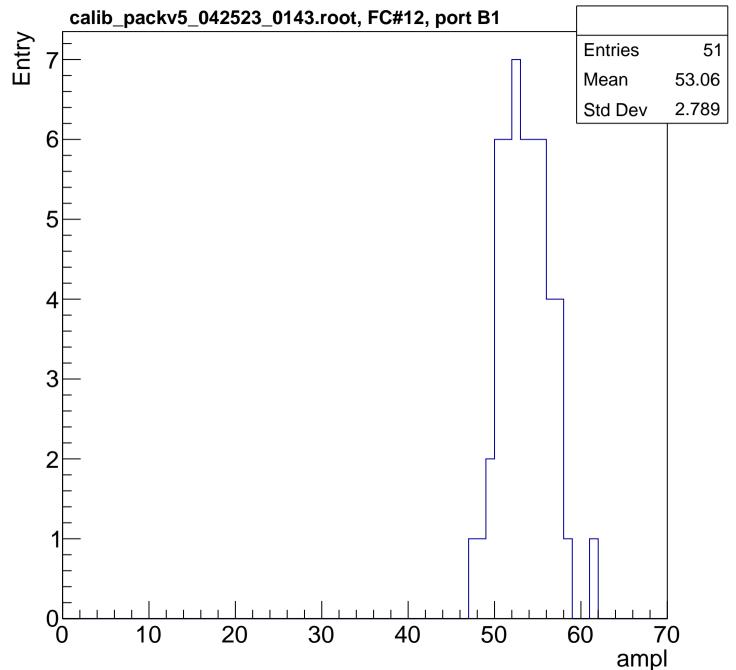


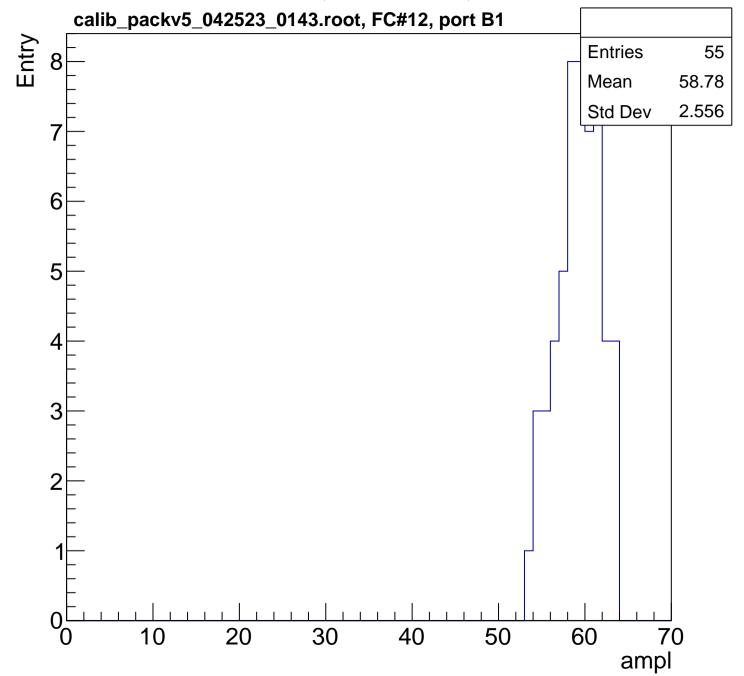


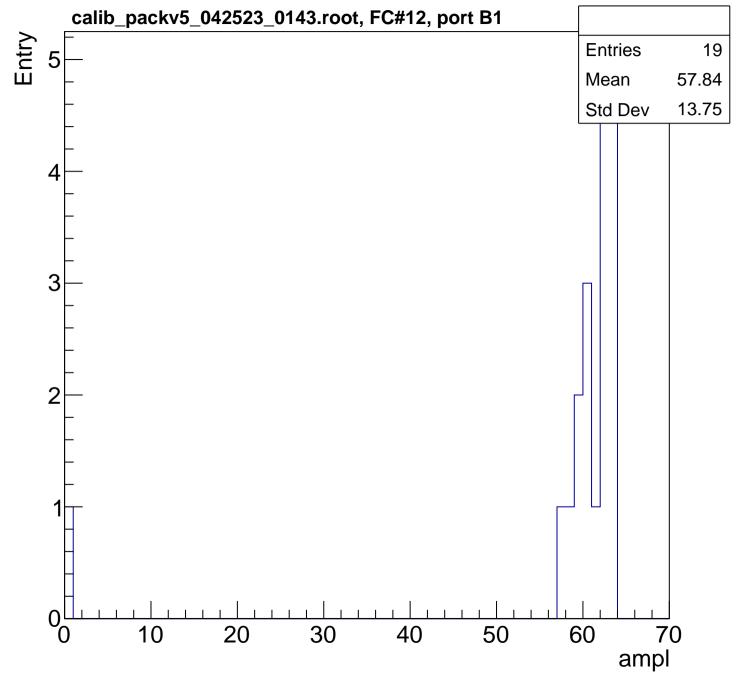


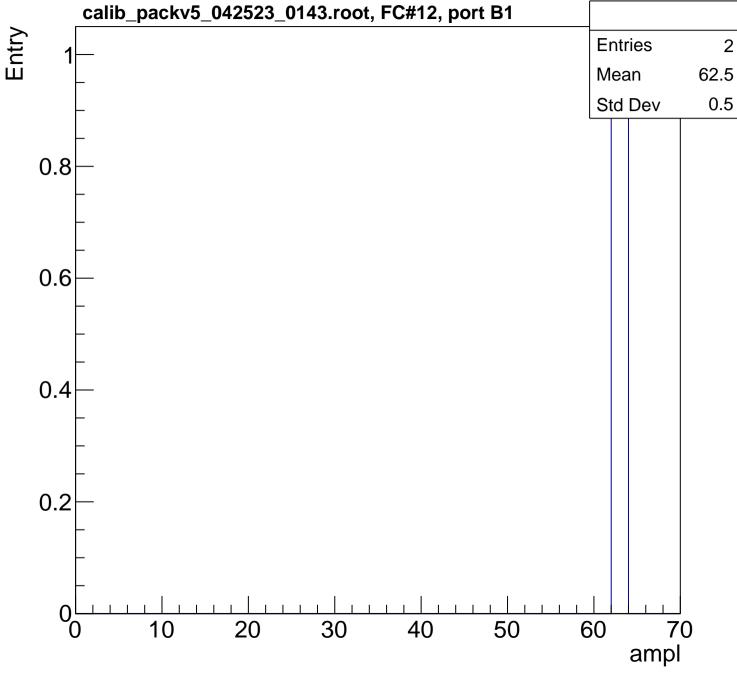


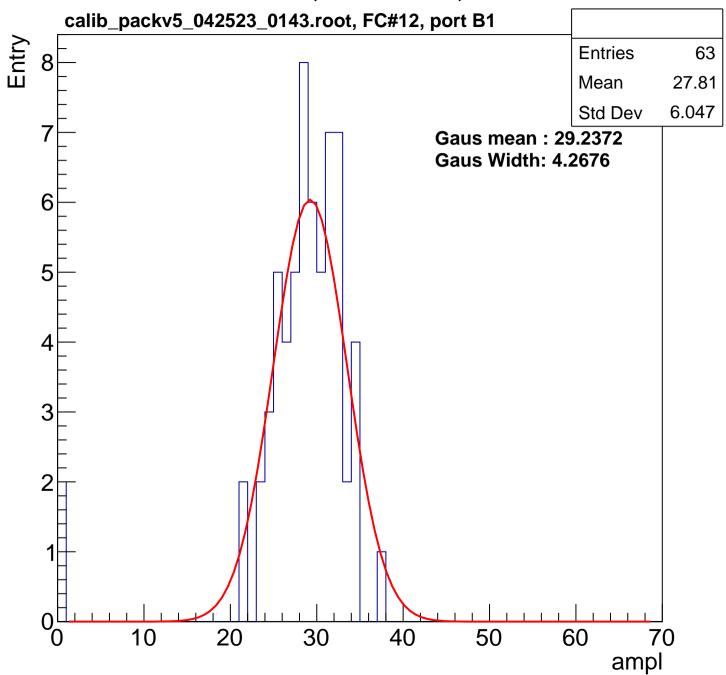


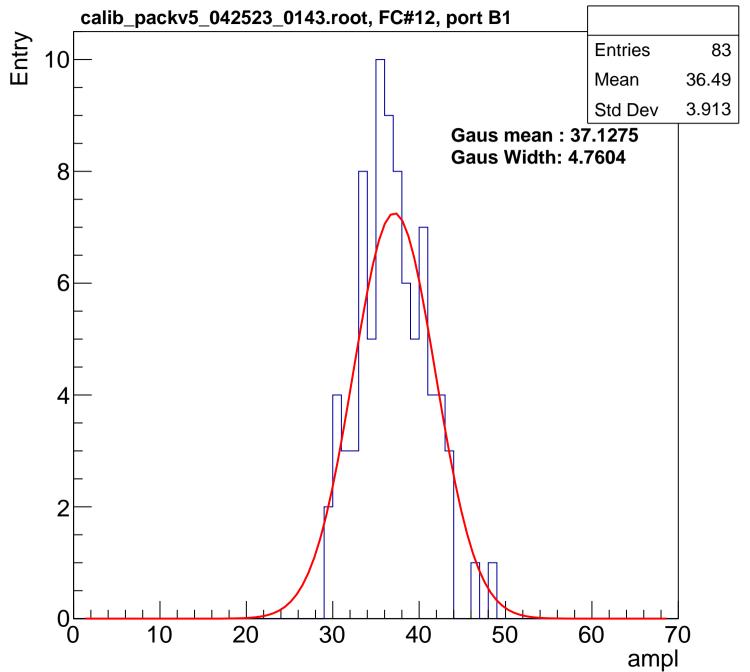


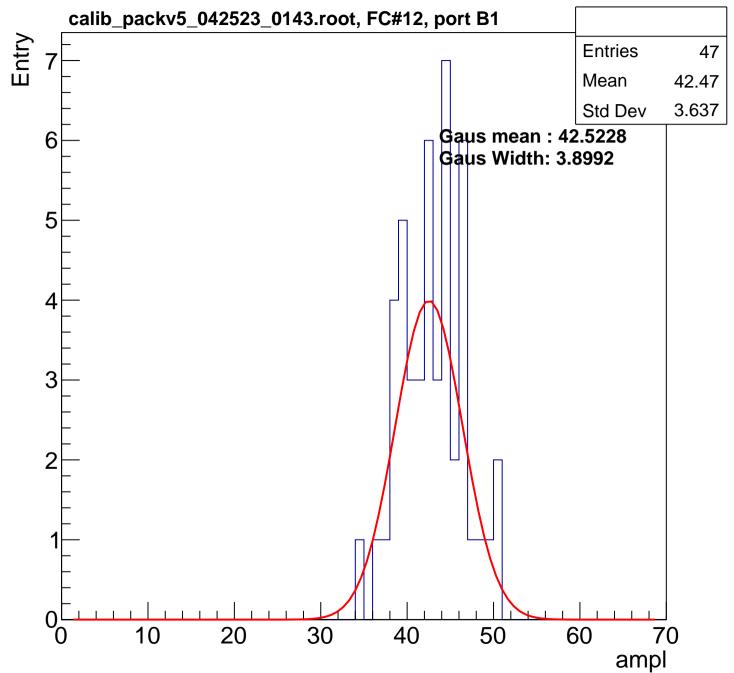


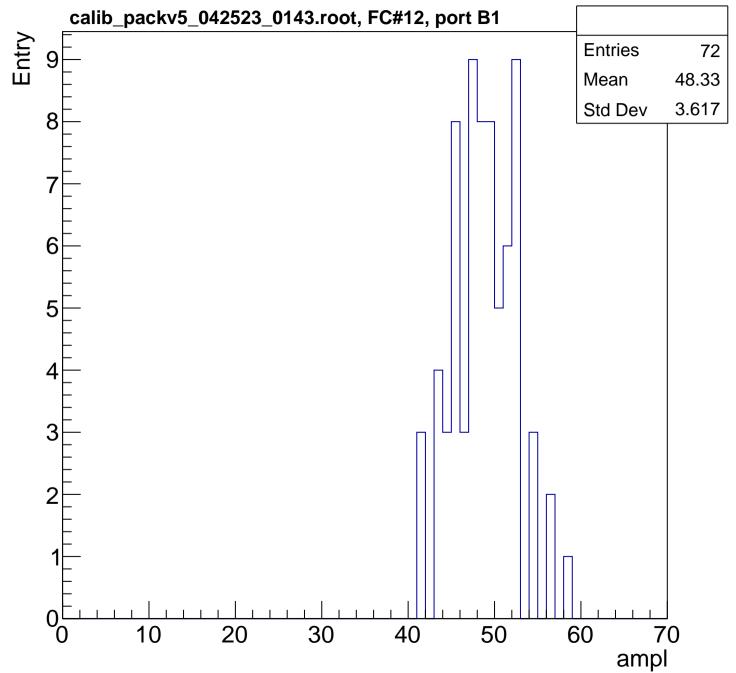


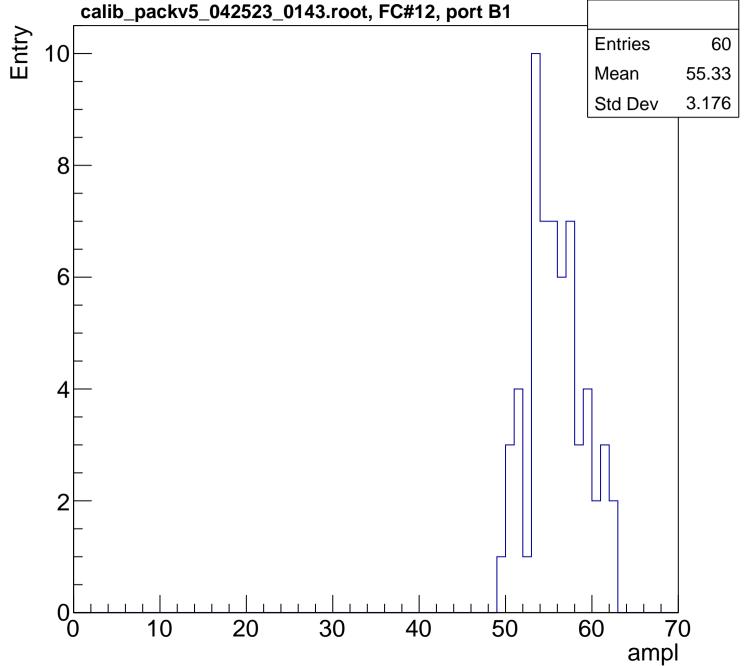


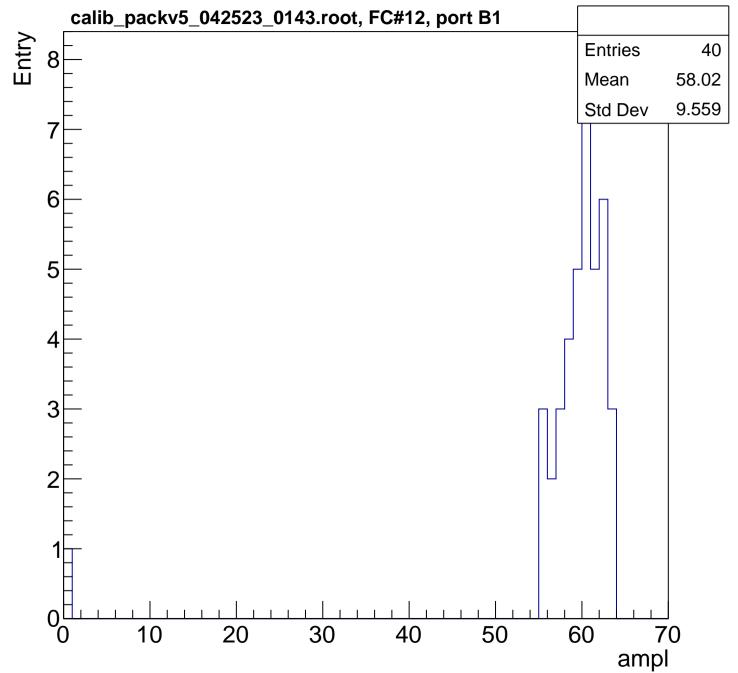


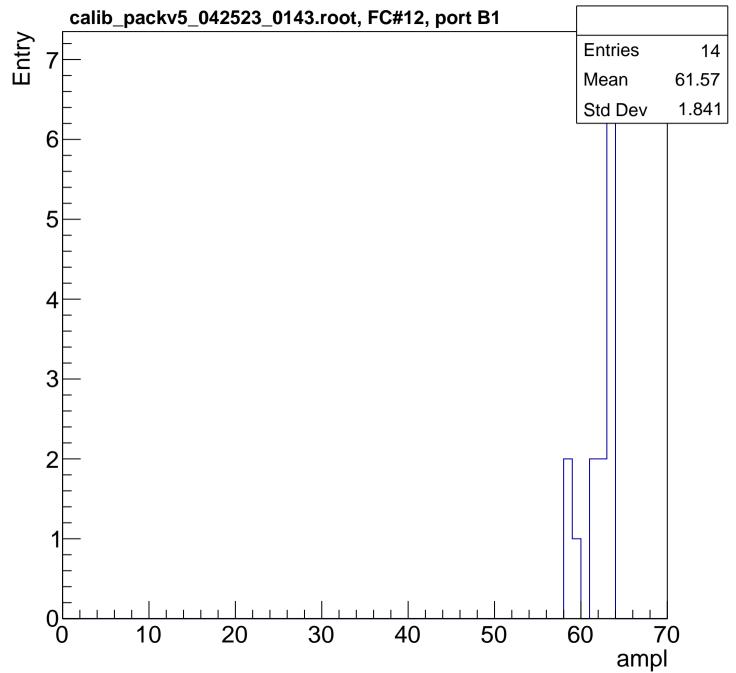




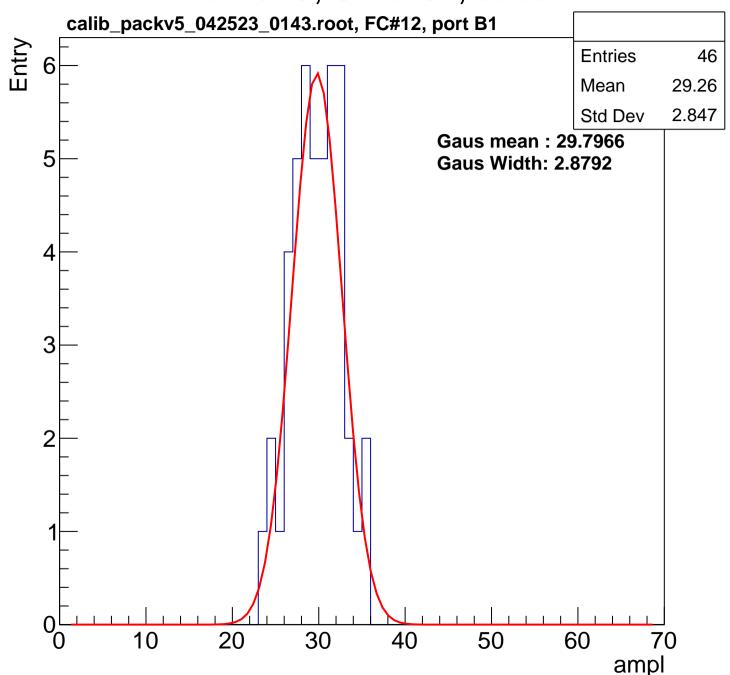


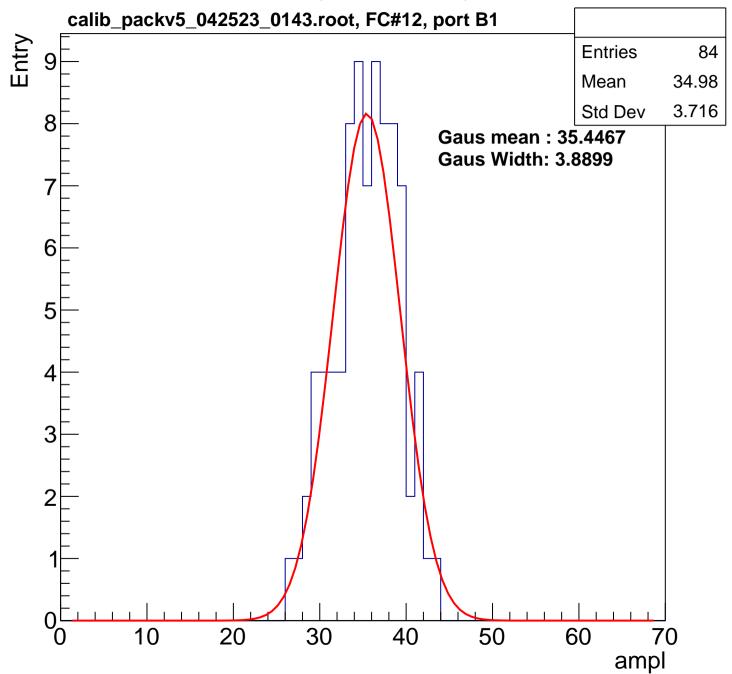


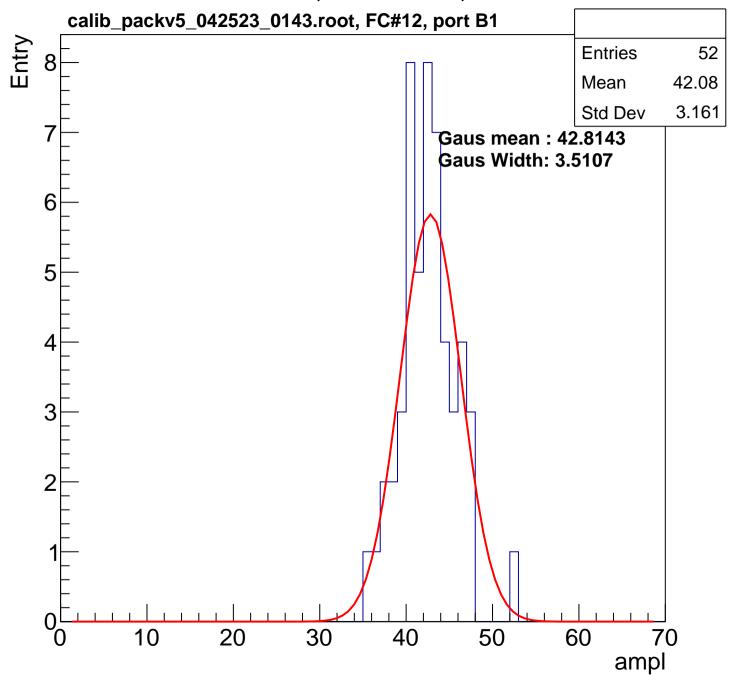


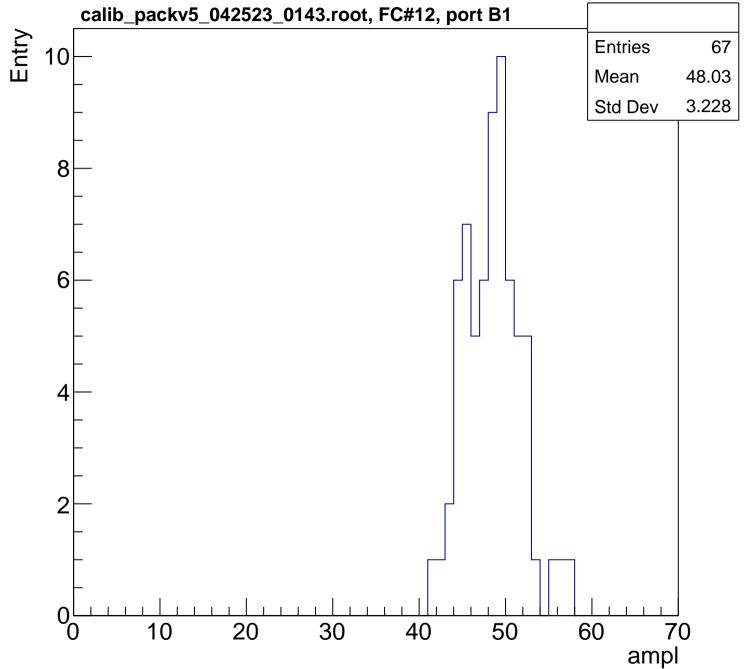


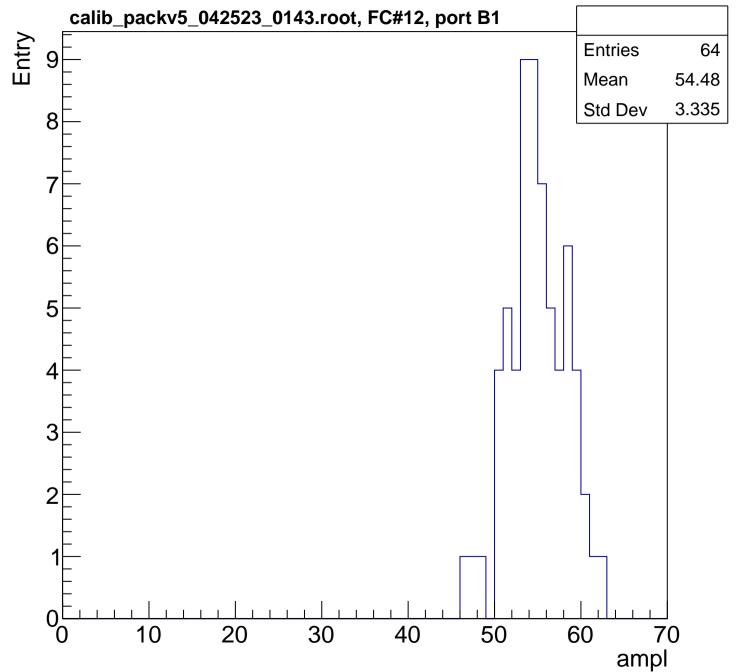
B0L102S, U2-ch38, adc7 calib_packv5_042523_0143.root, FC#12, port B1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

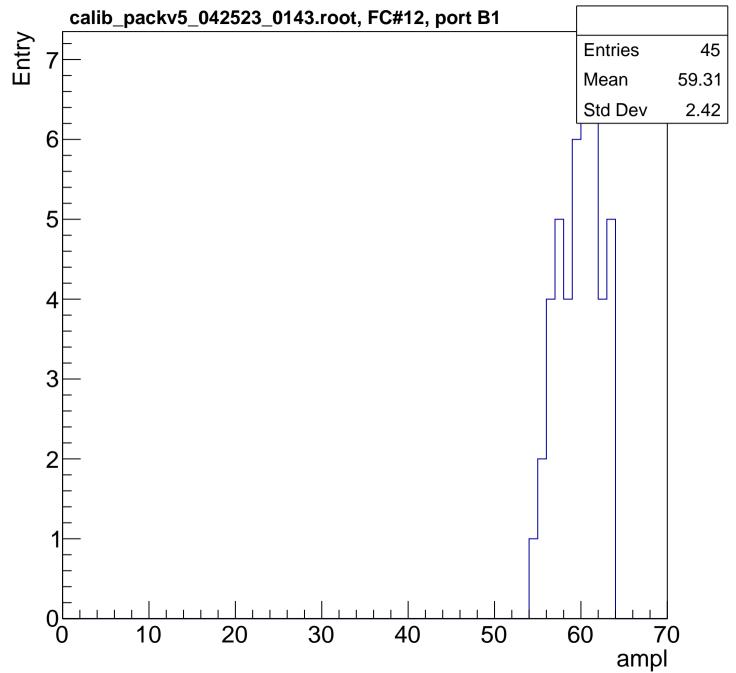


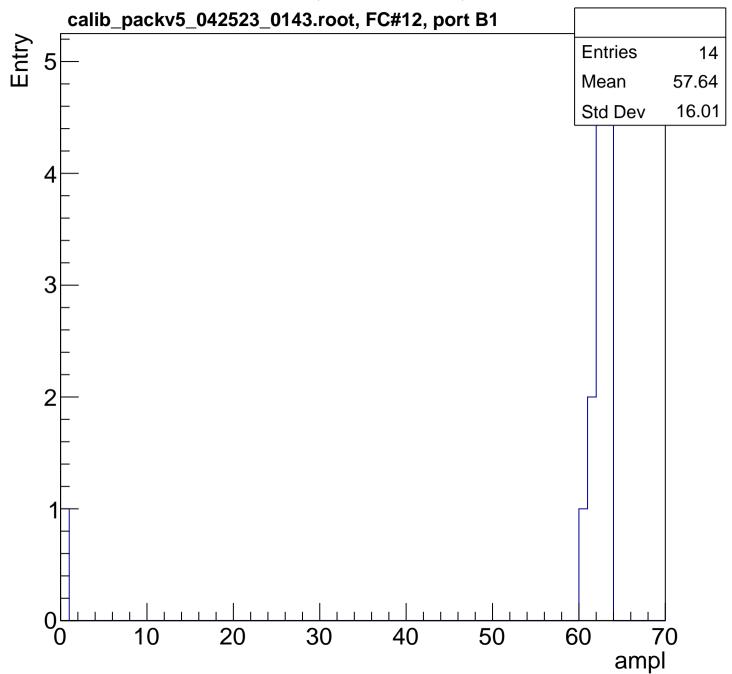




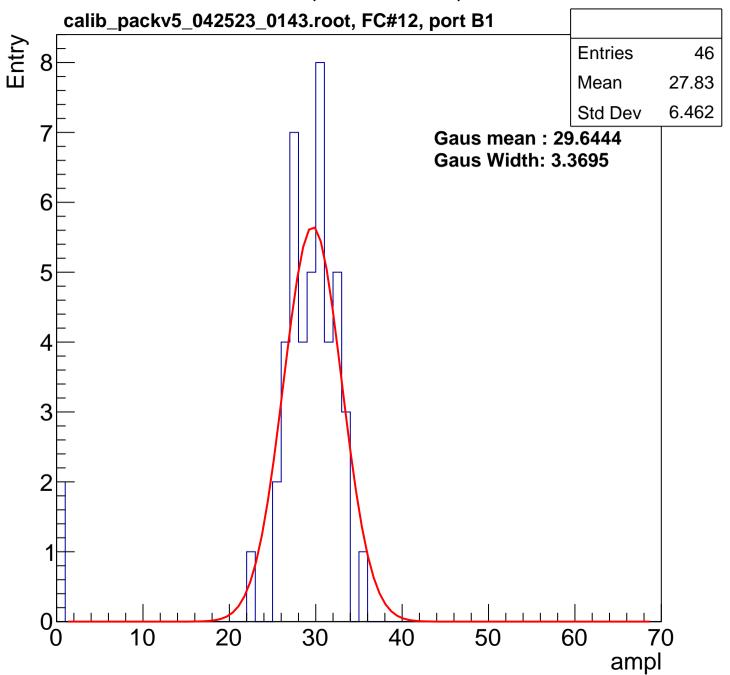


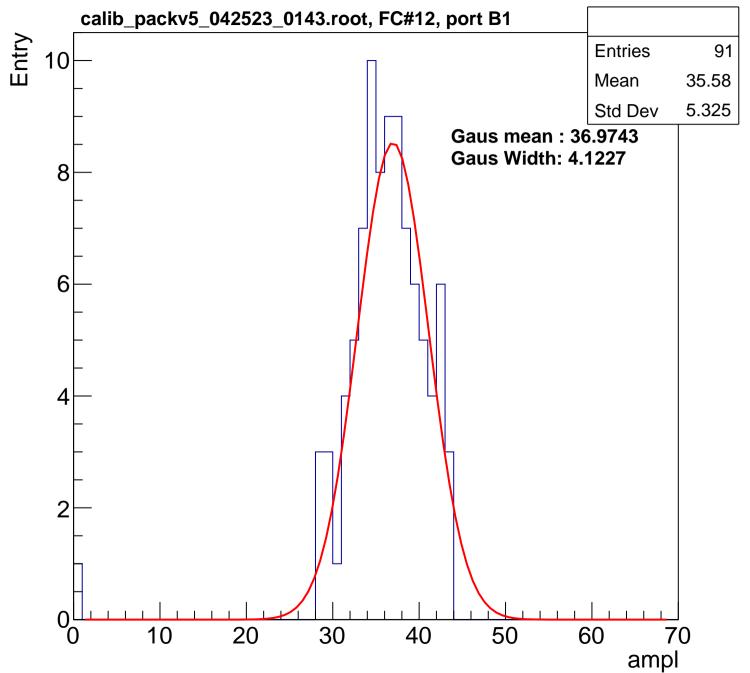


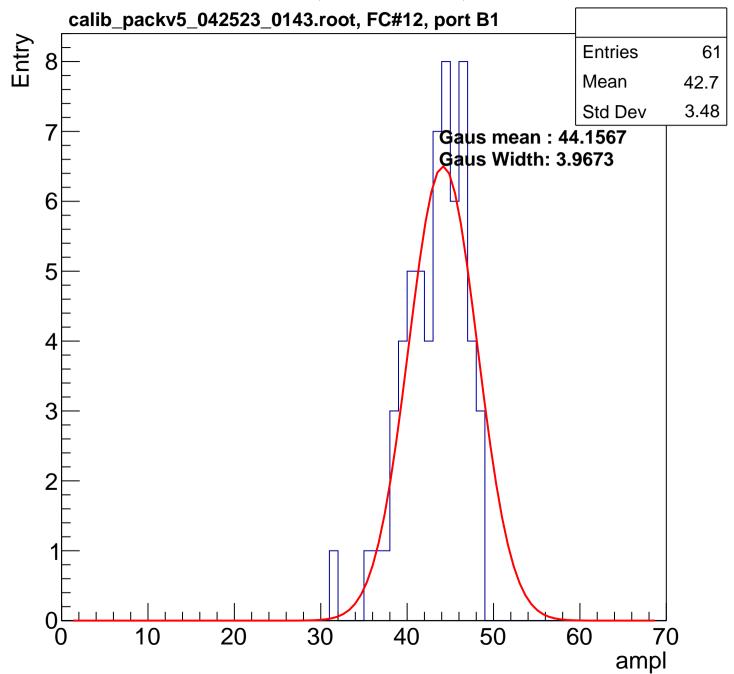


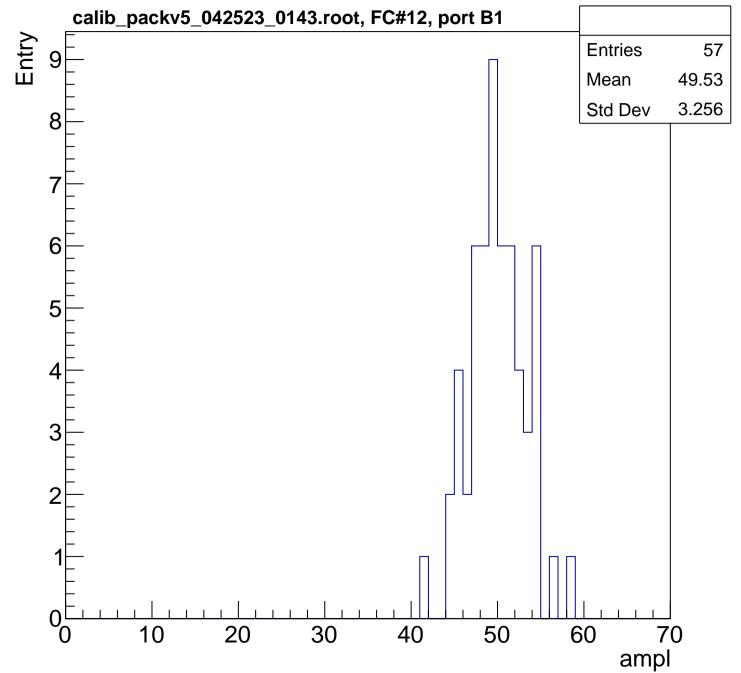


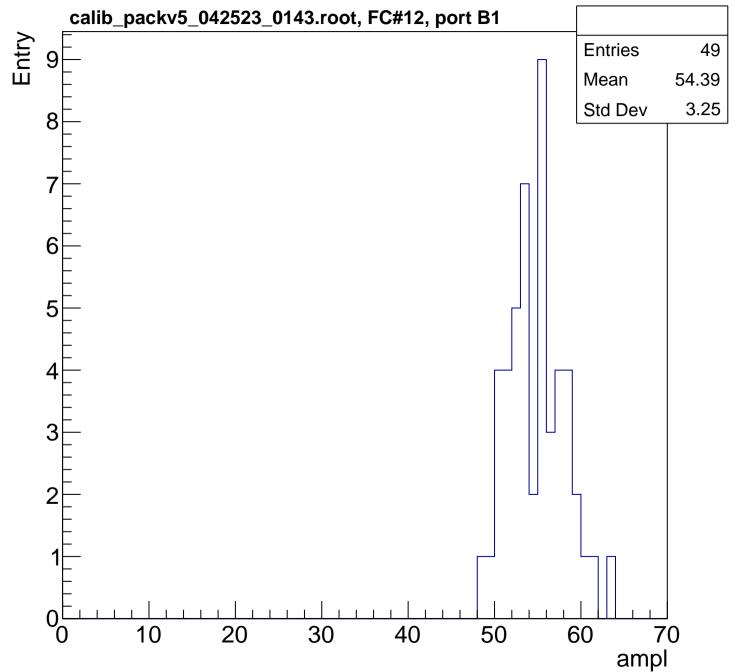
B0L102S, U2-ch39, adc7 calib_packv5_042523_0143.root, FC#12, port B1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

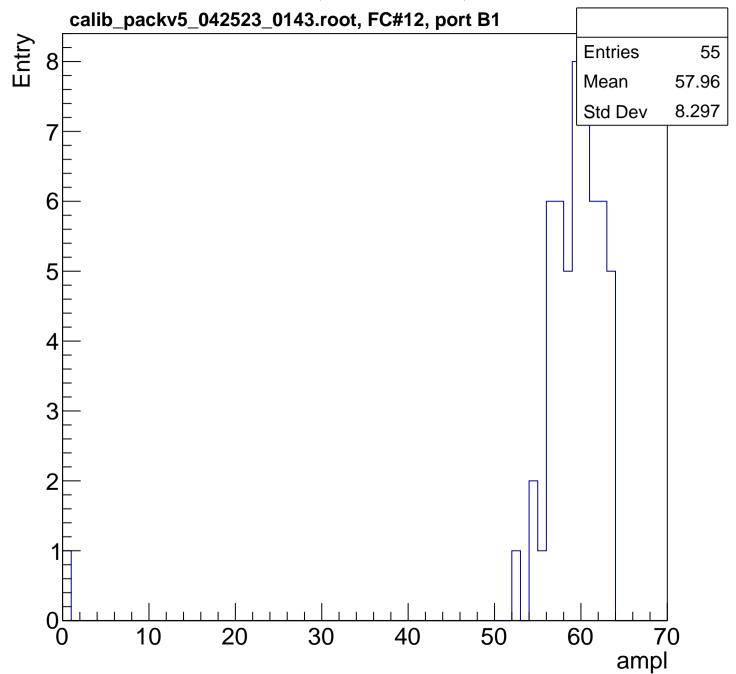


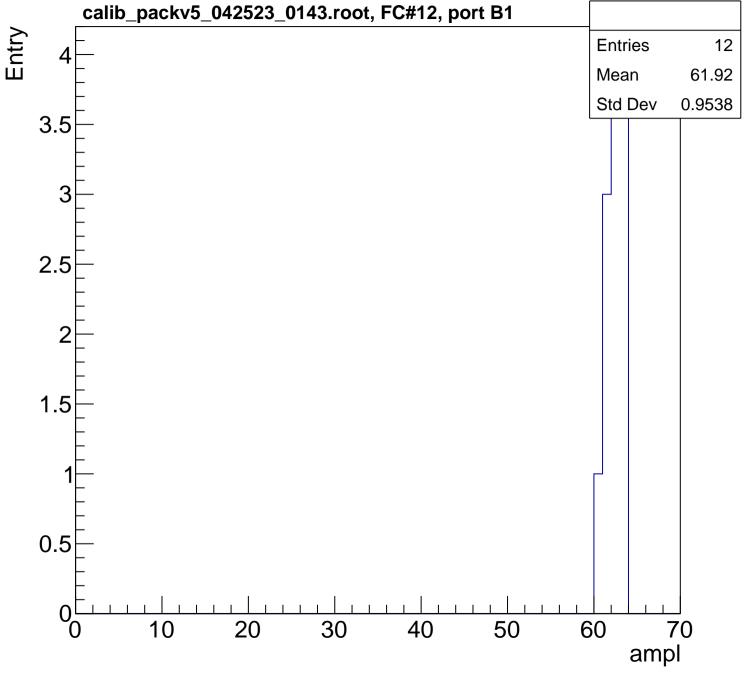




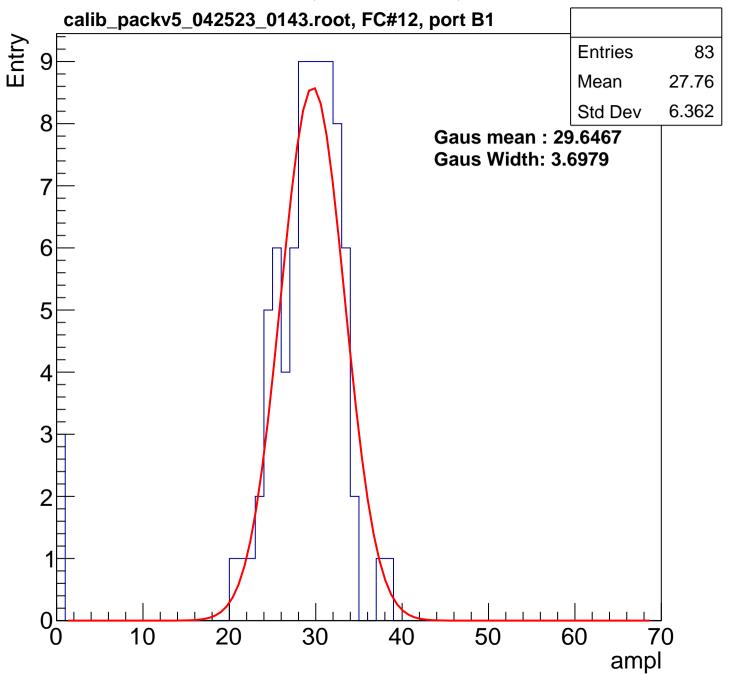


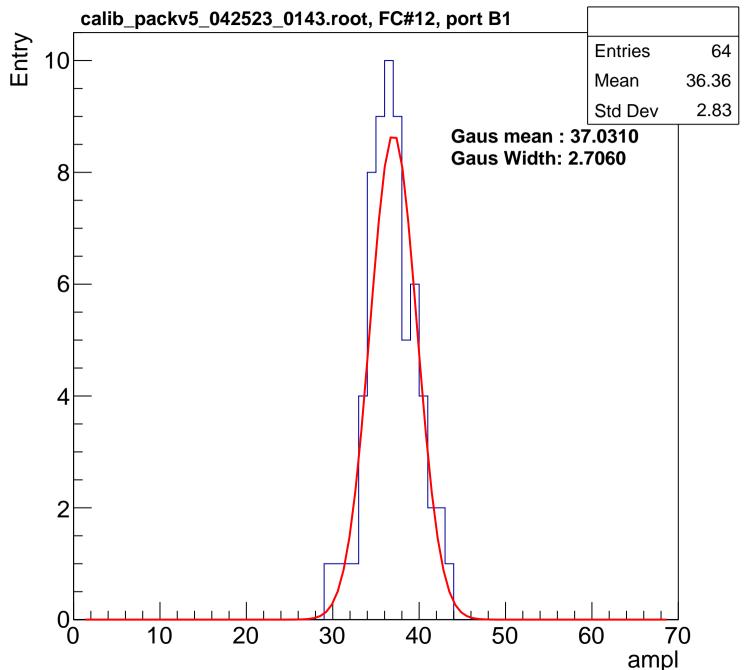


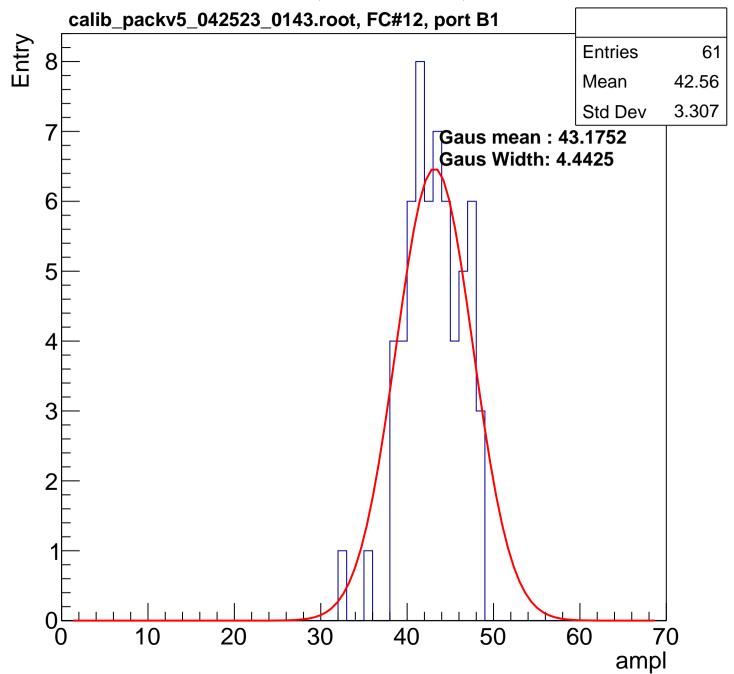


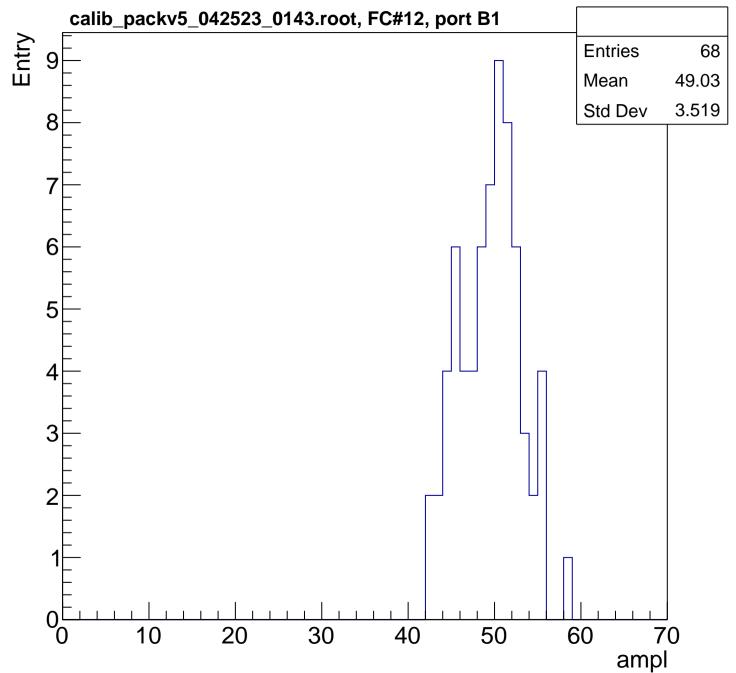


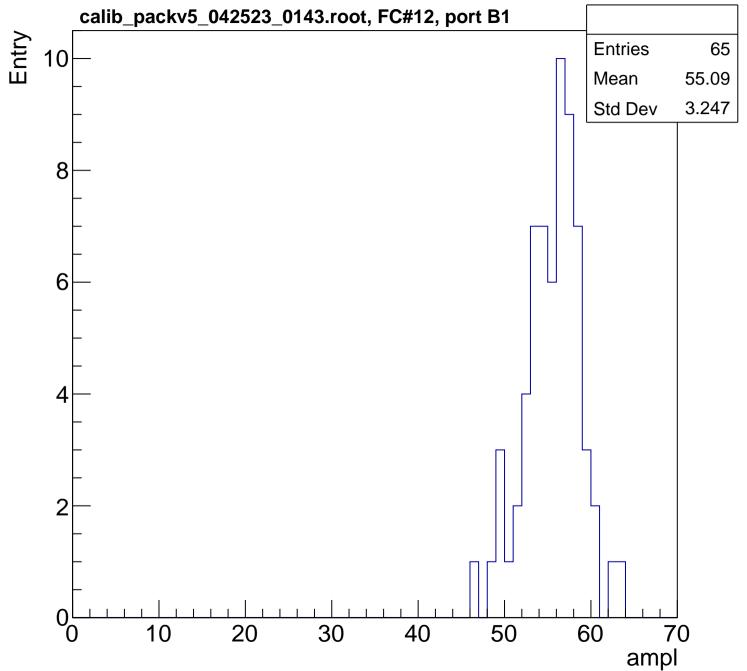


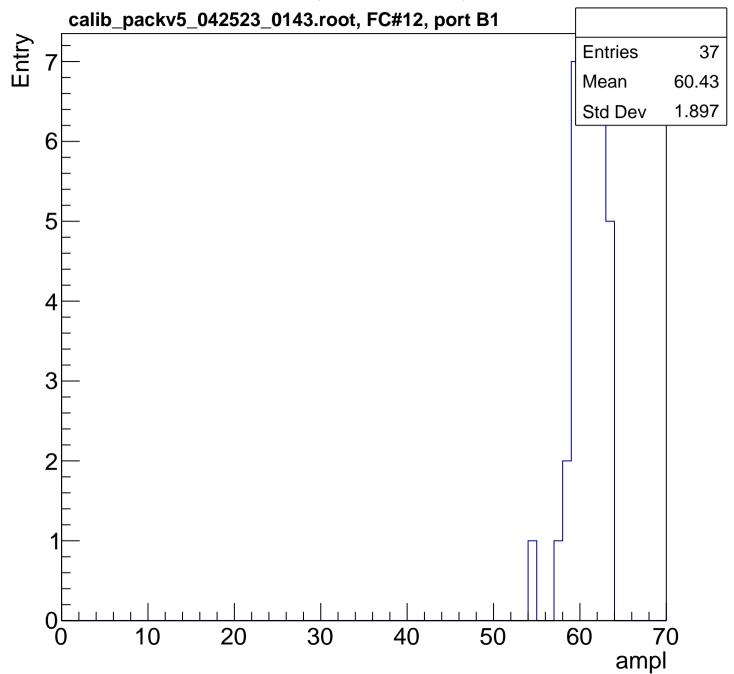


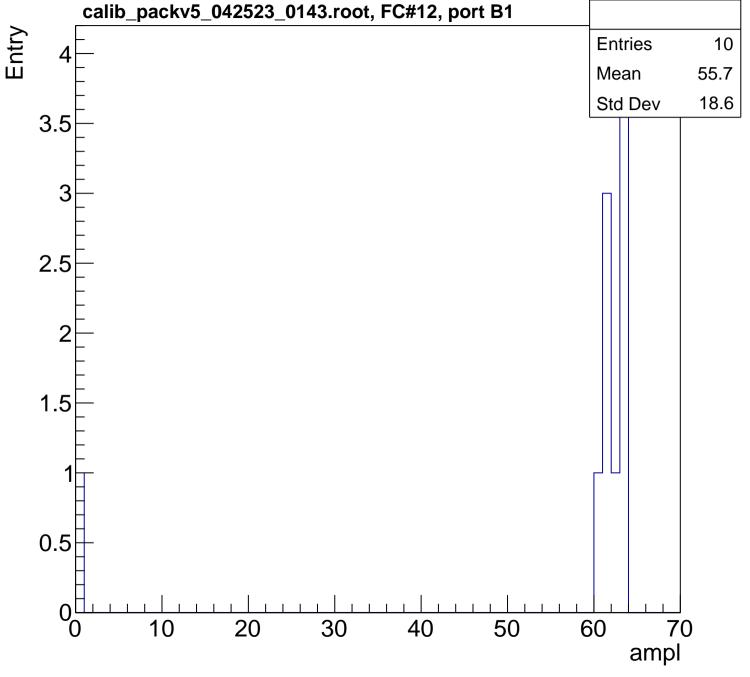




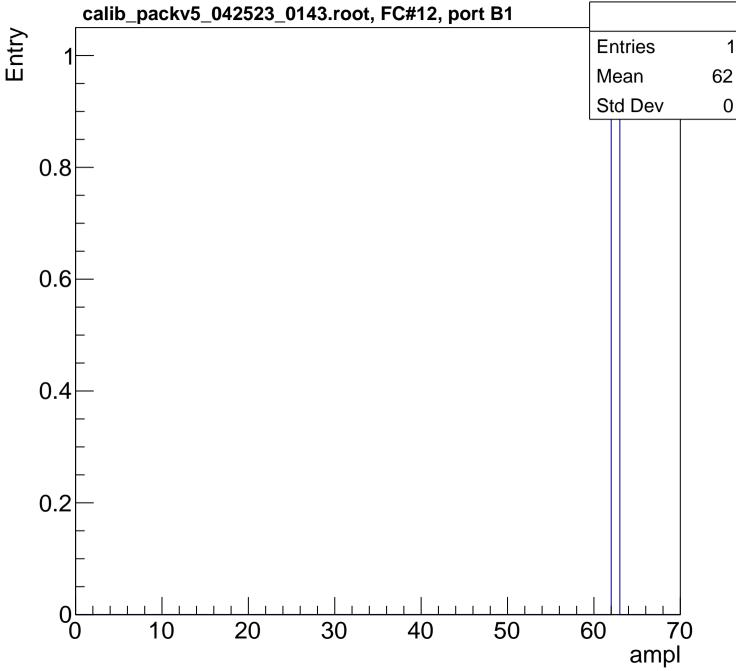


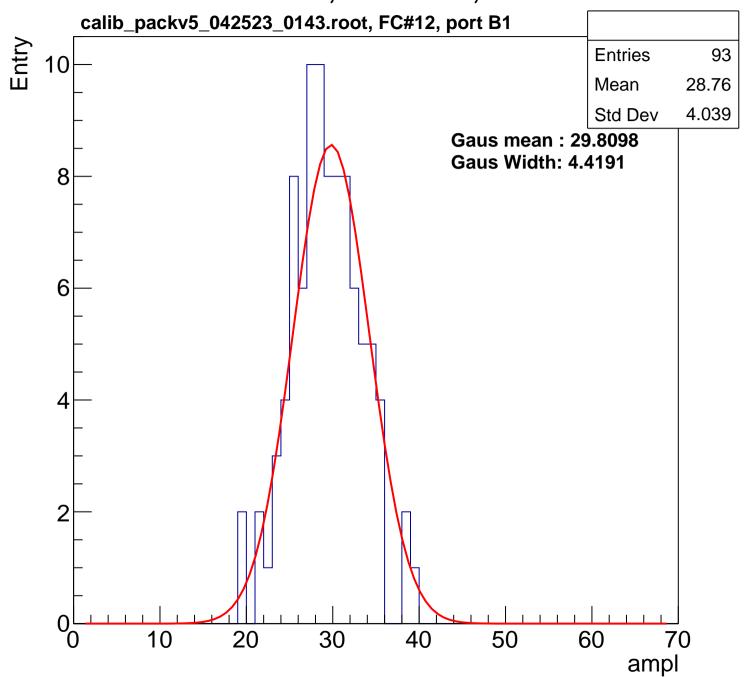


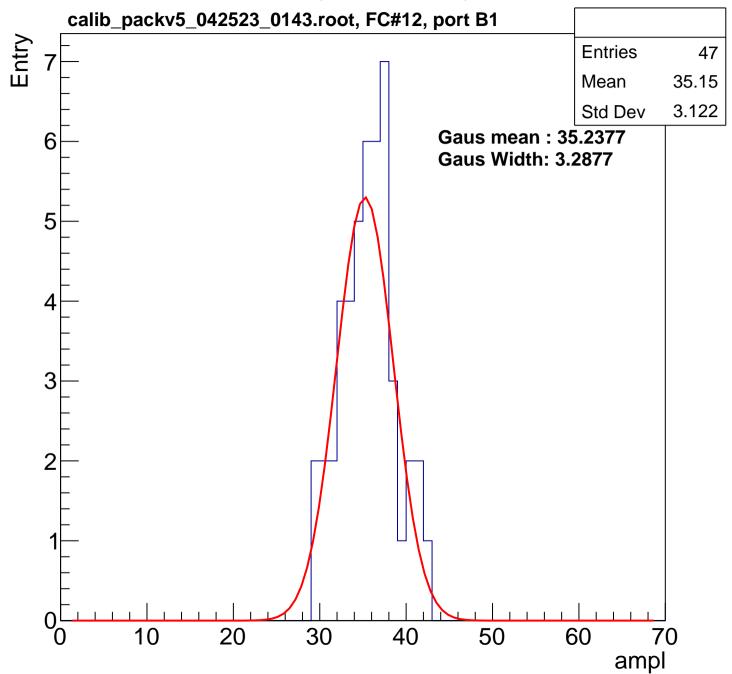


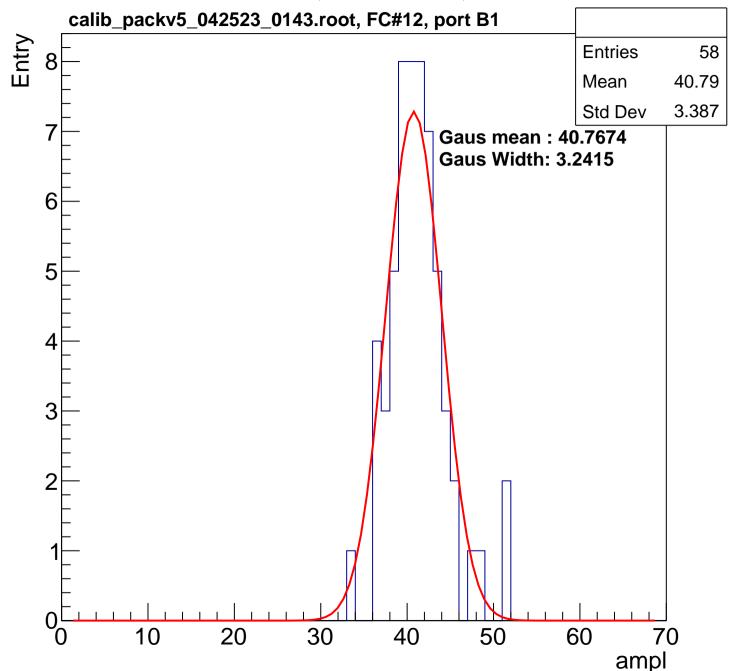


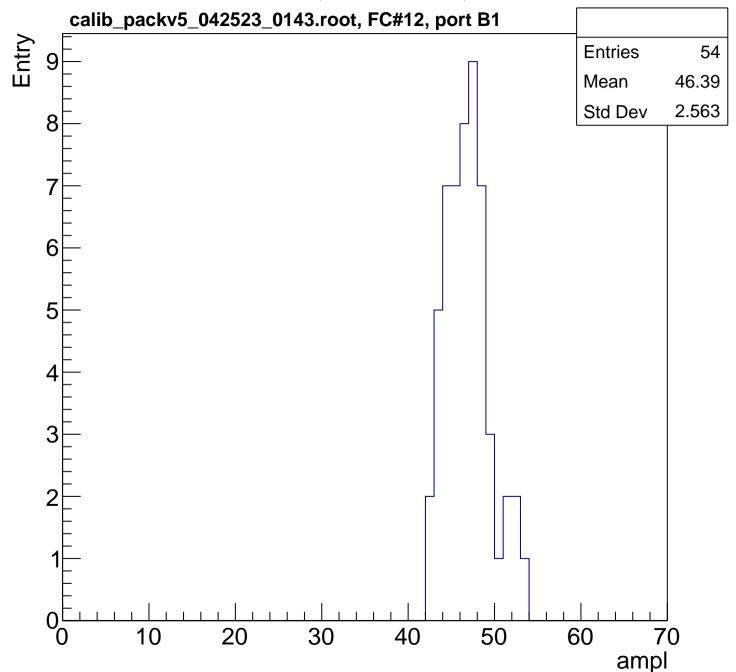
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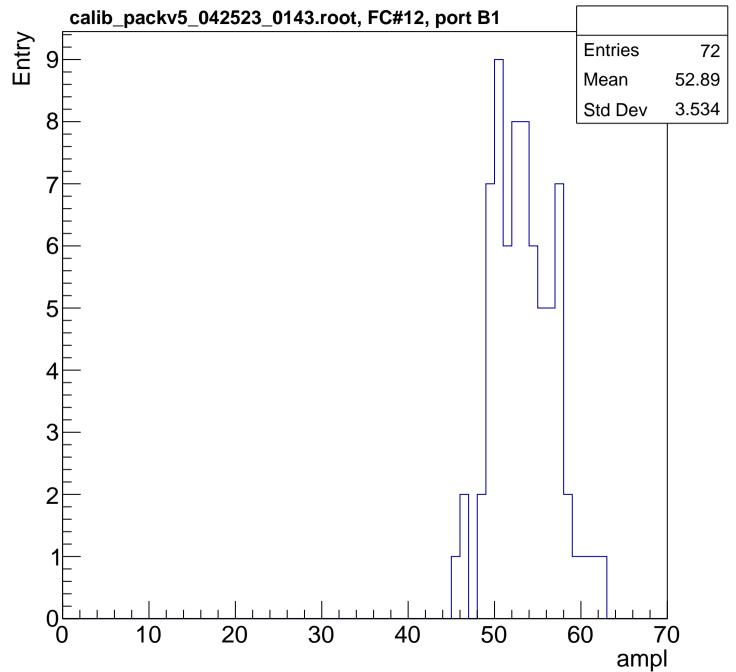


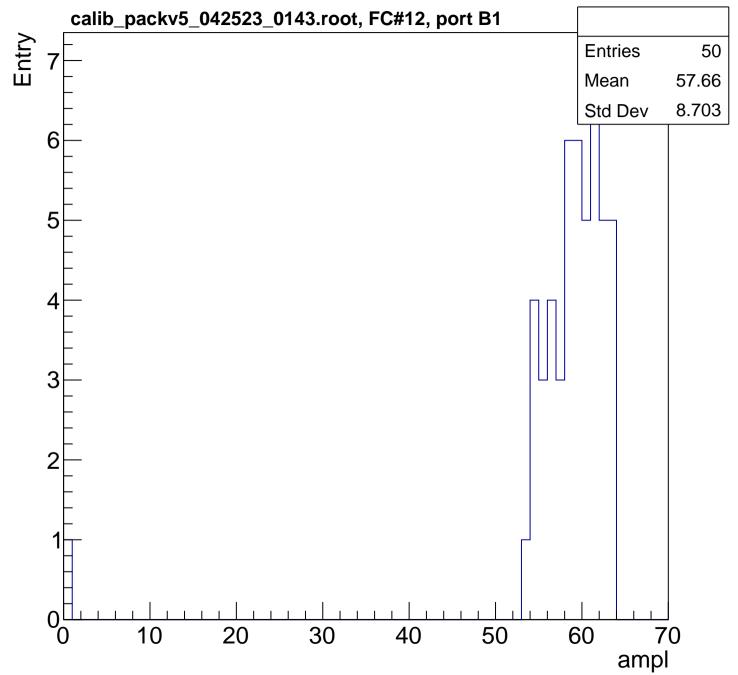


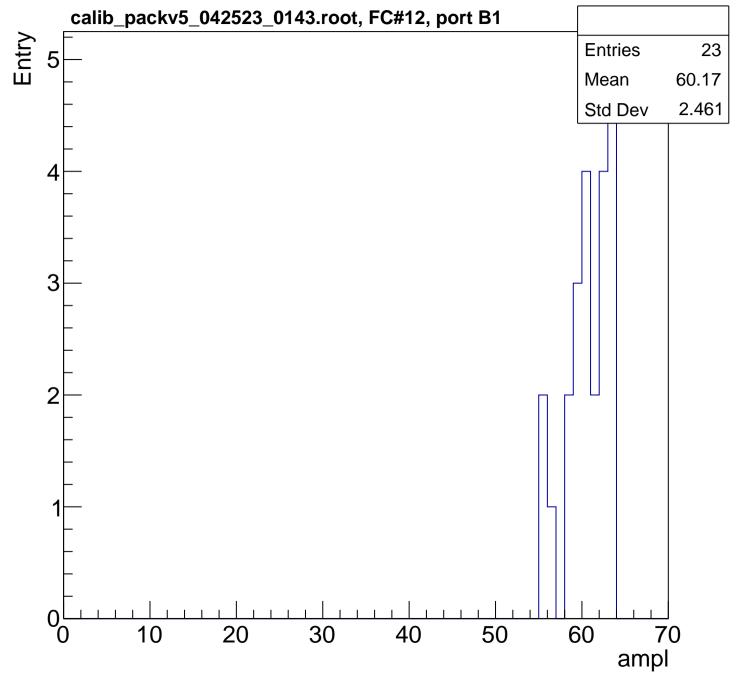


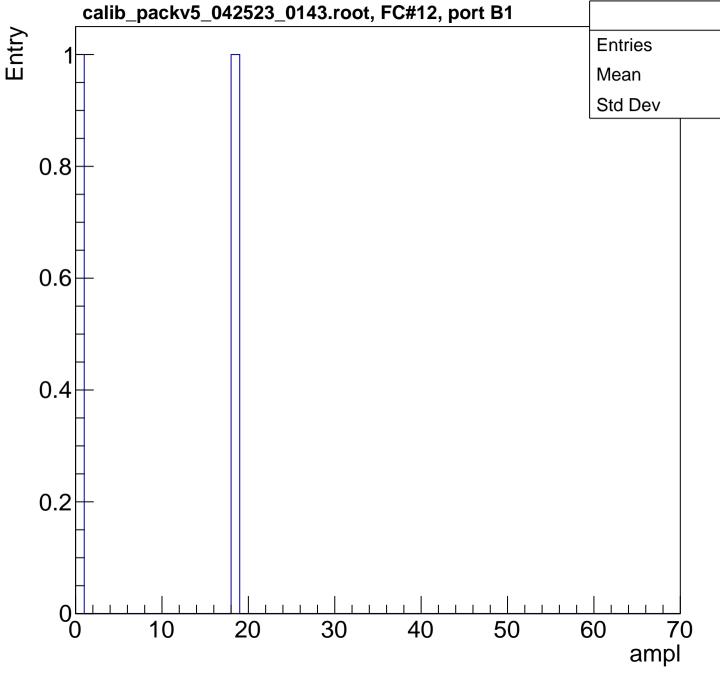


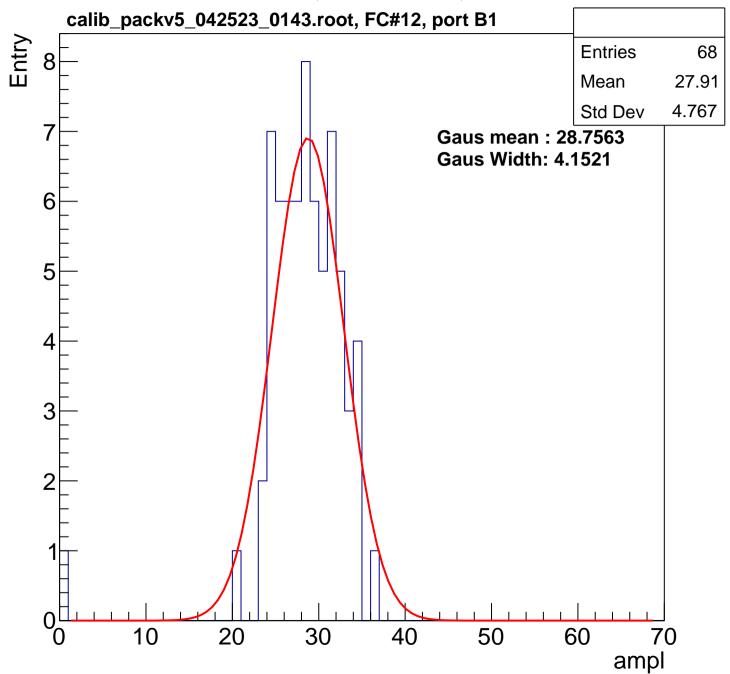


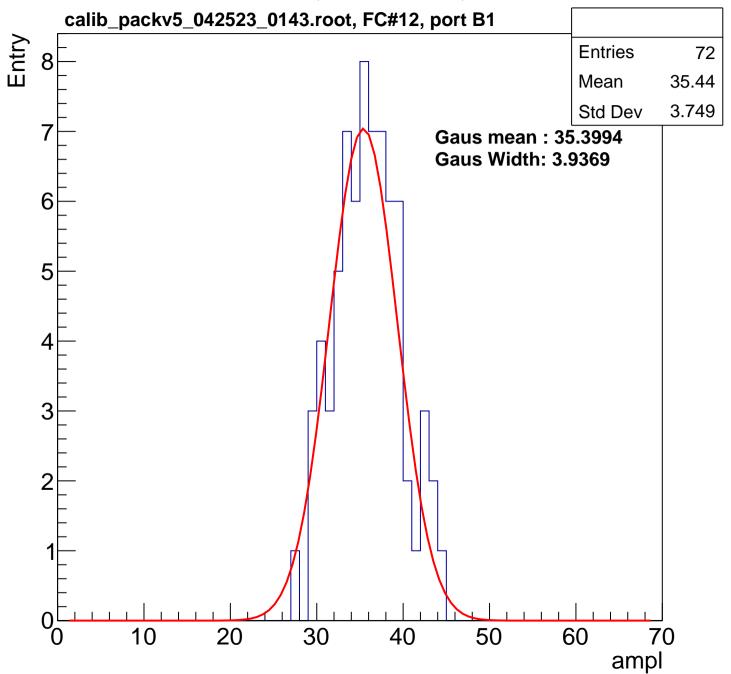


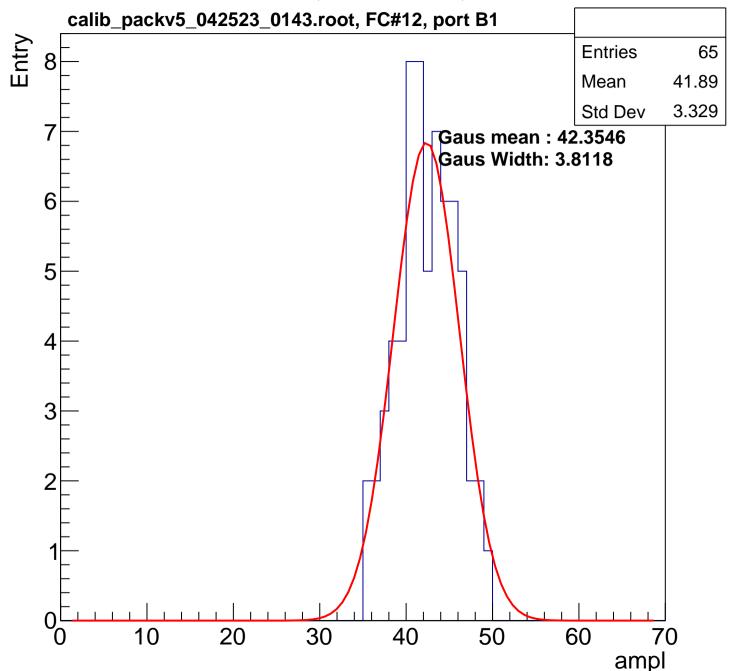


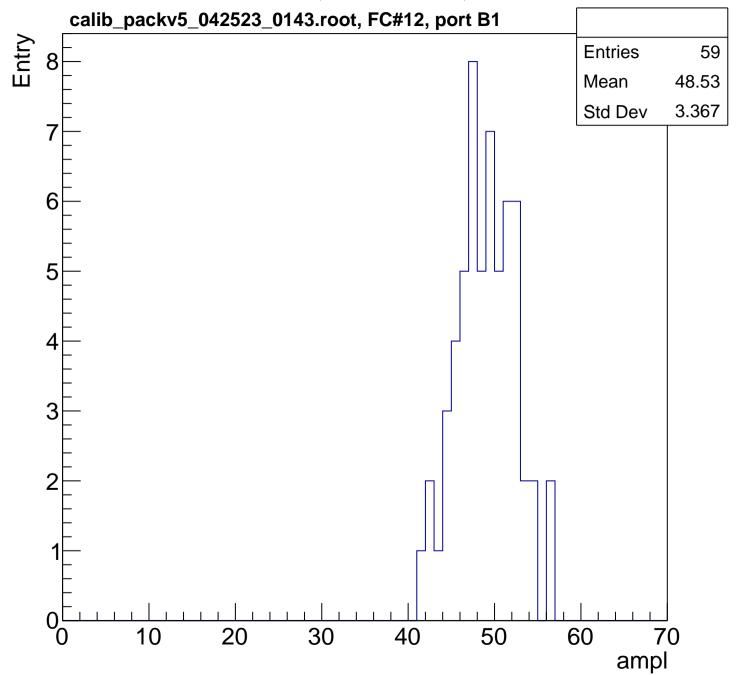


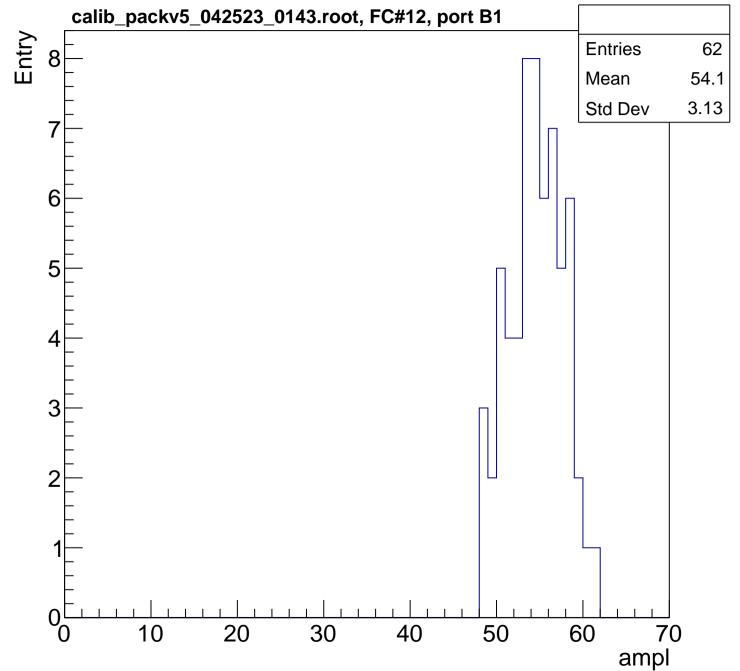


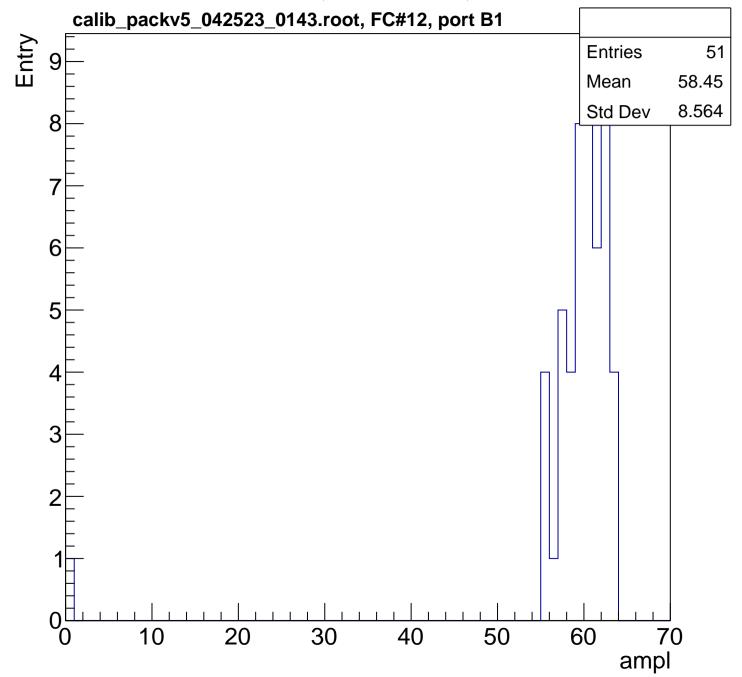


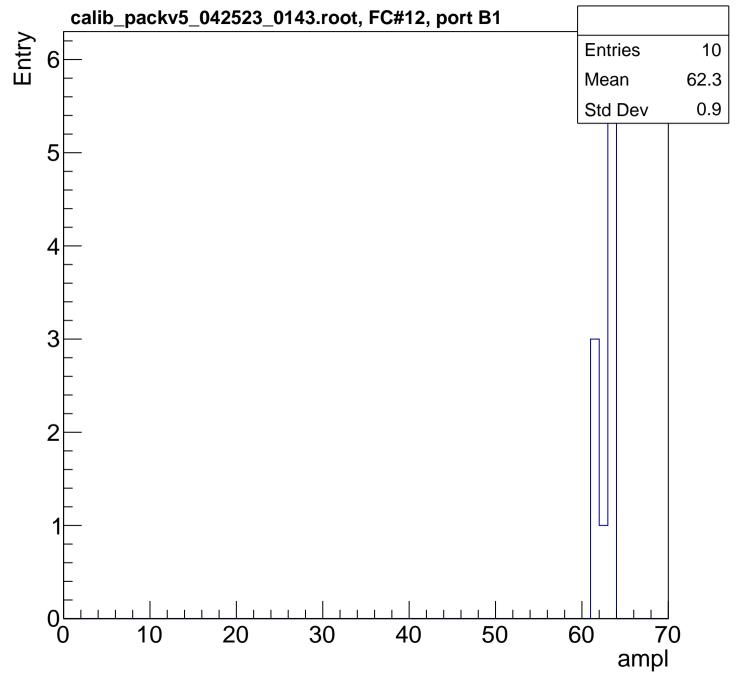


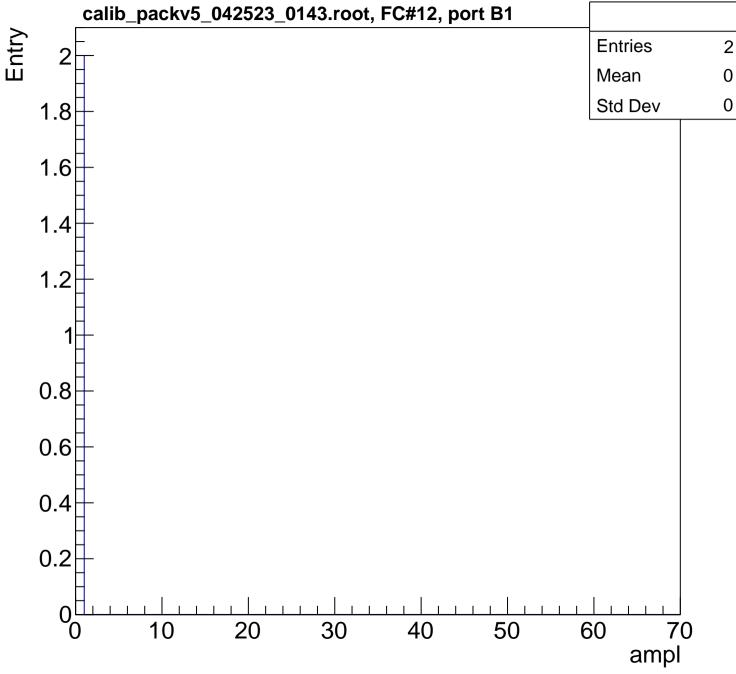


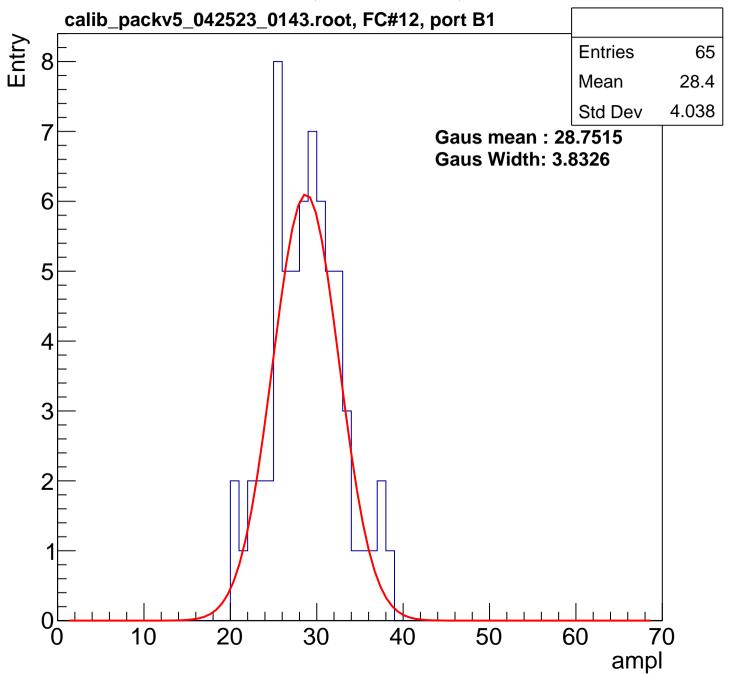


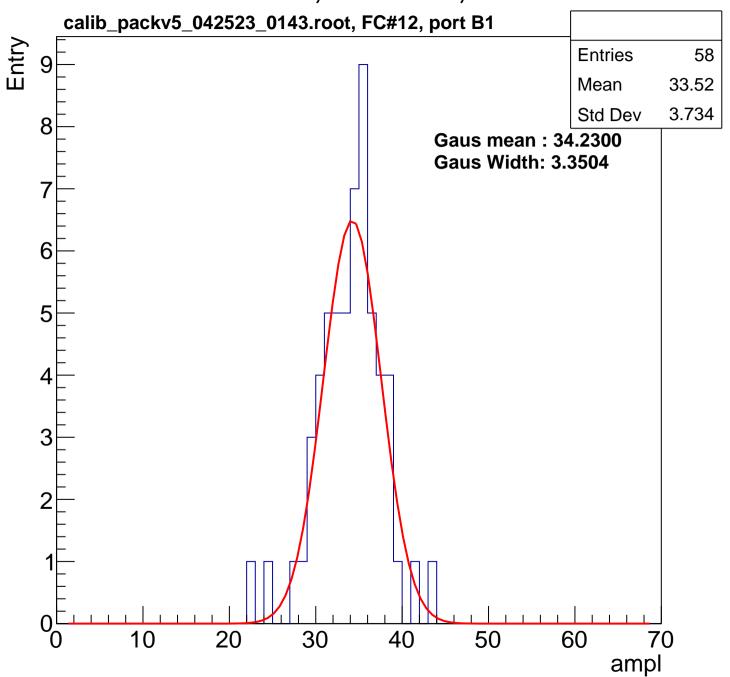


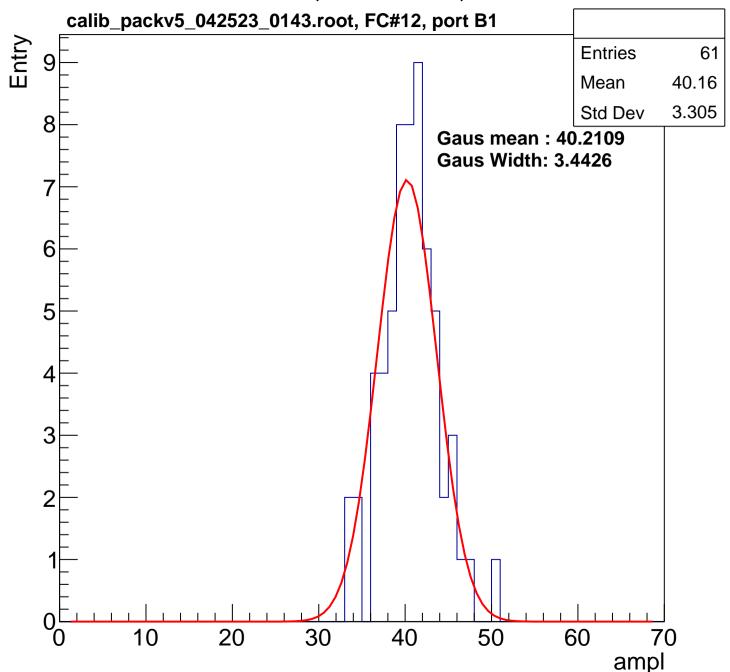


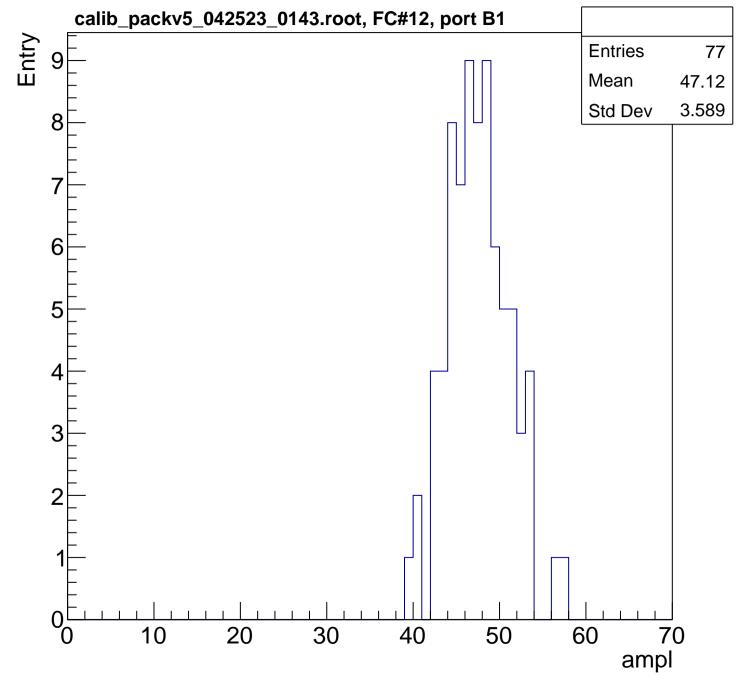


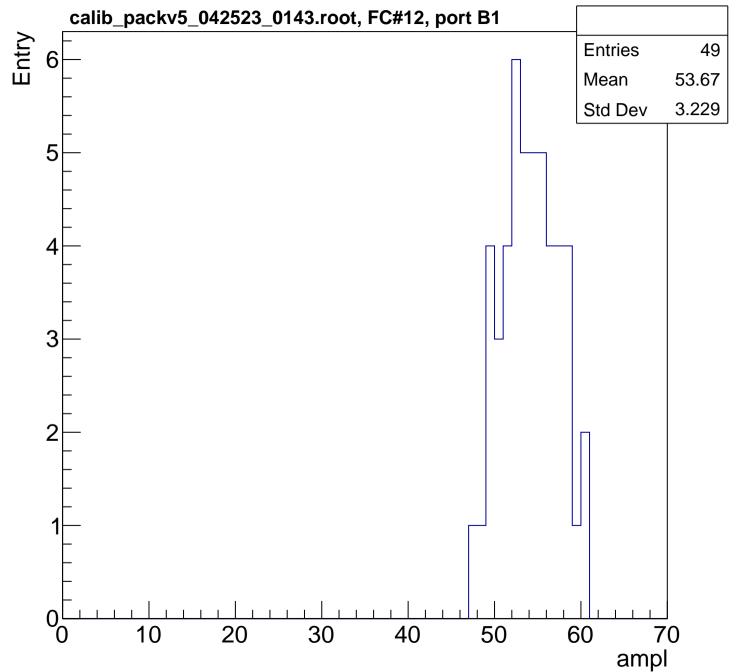


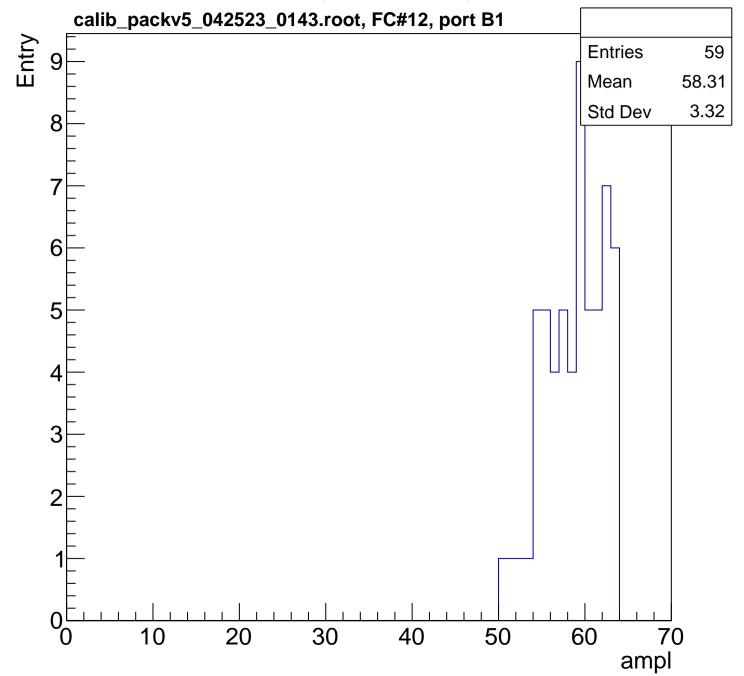


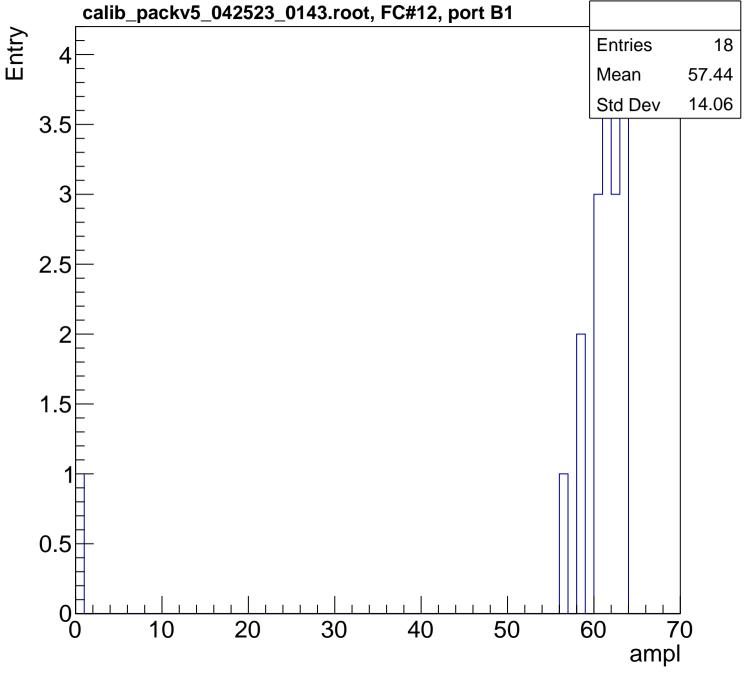


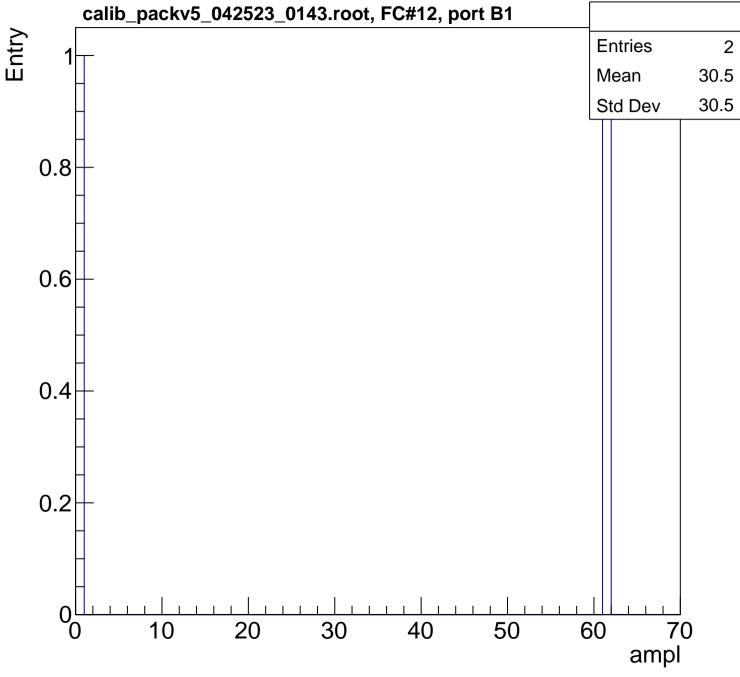


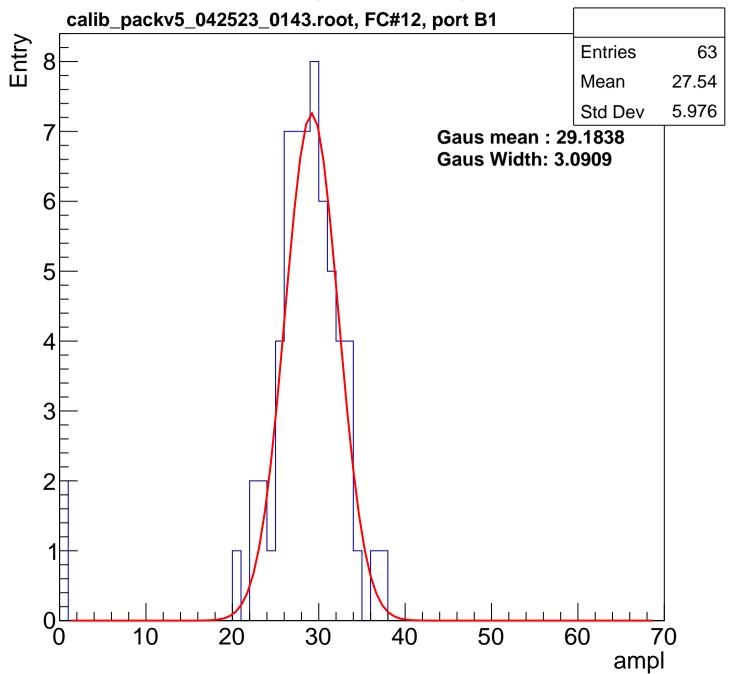


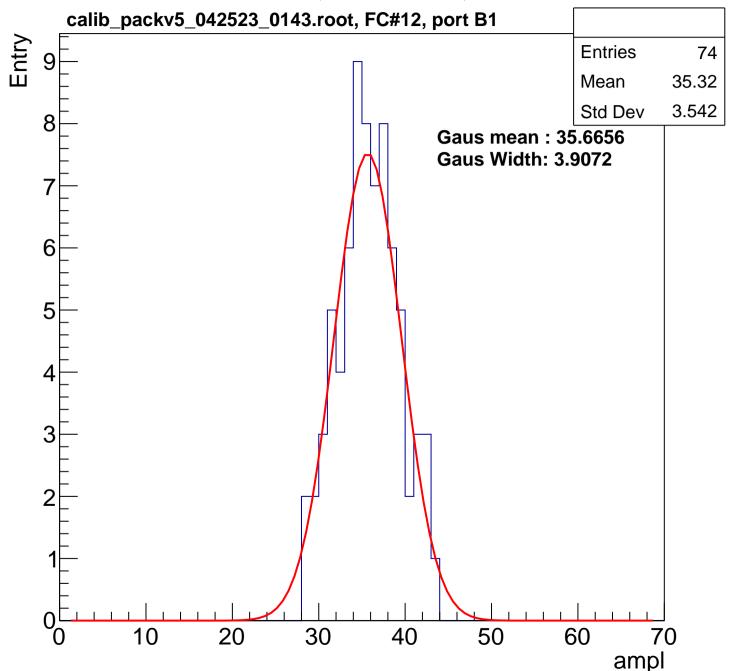


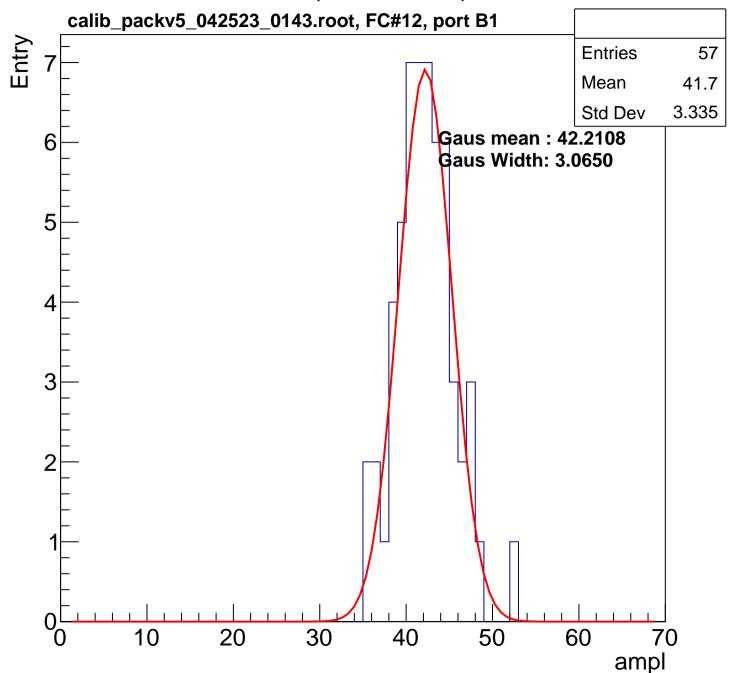


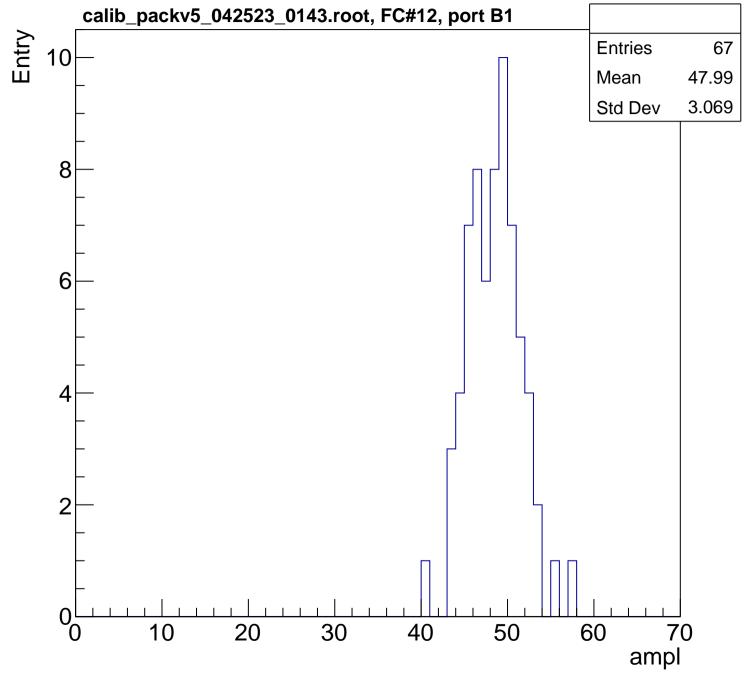


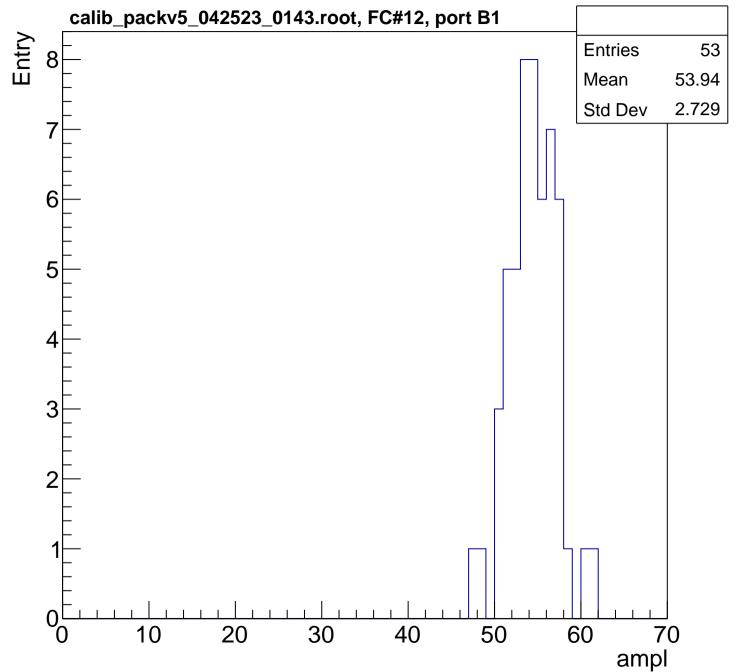


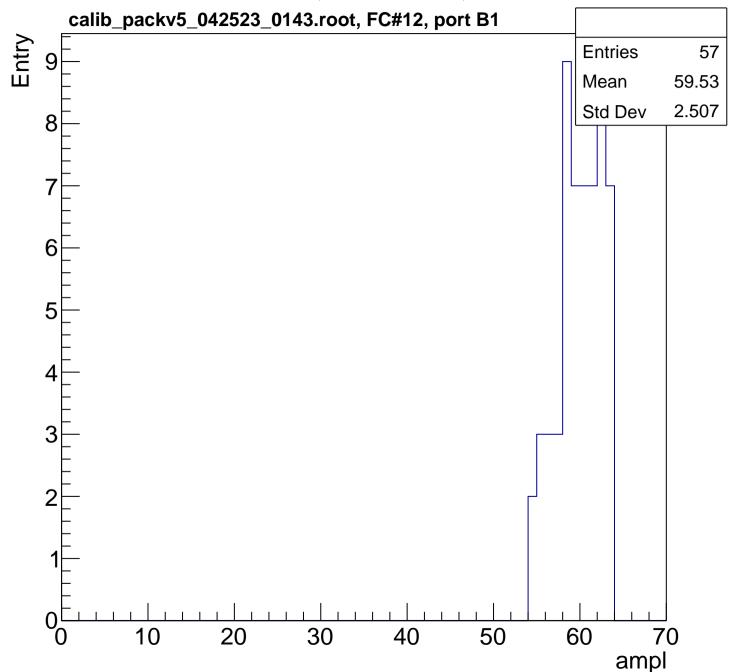


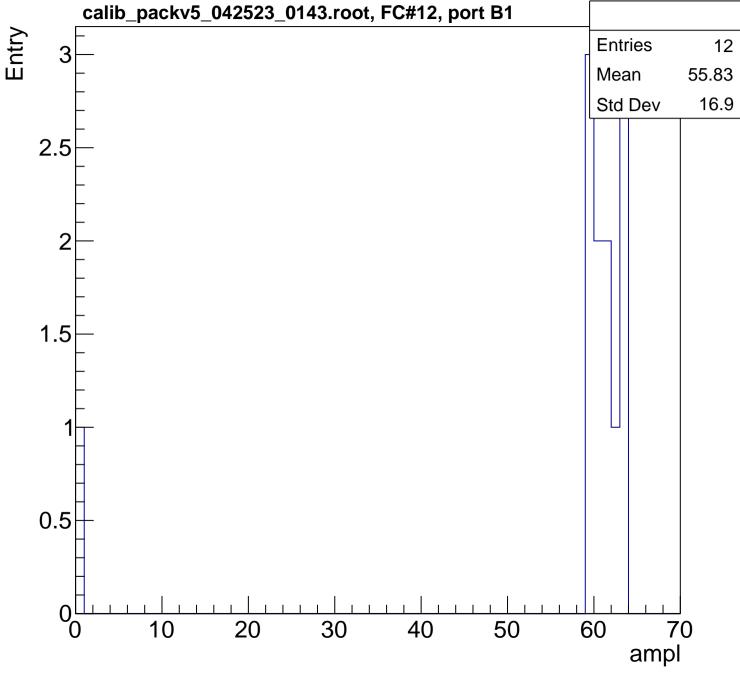




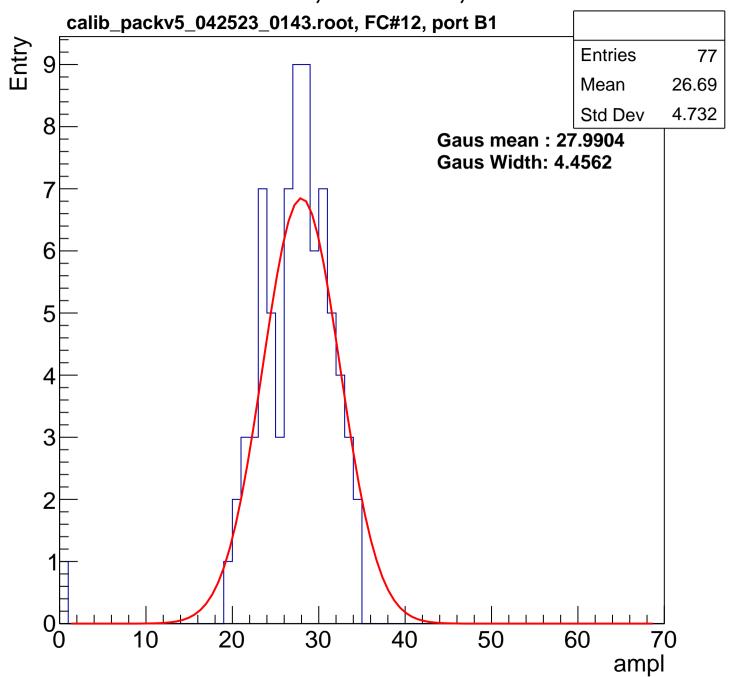


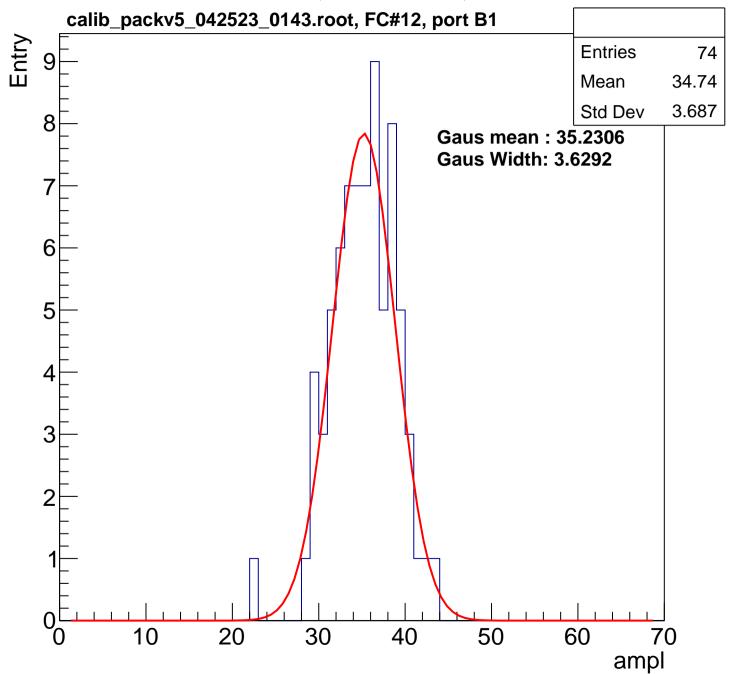


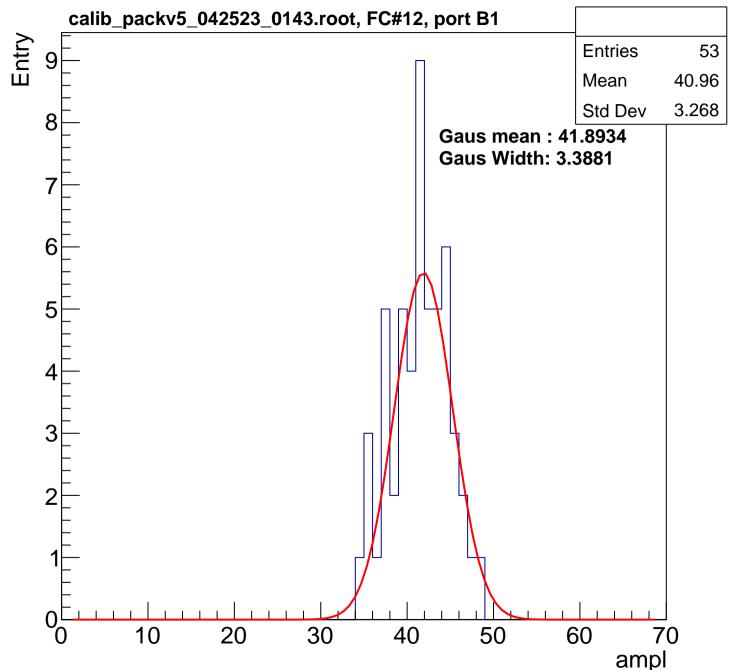


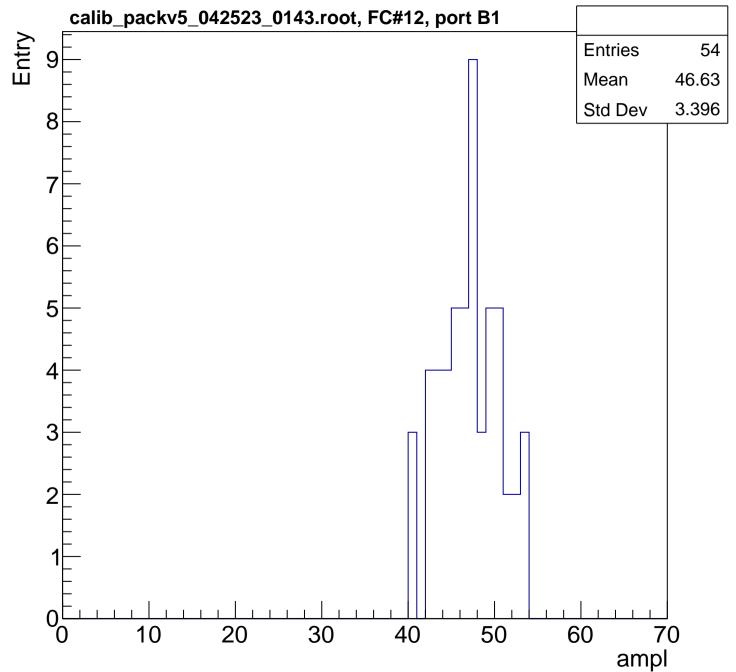


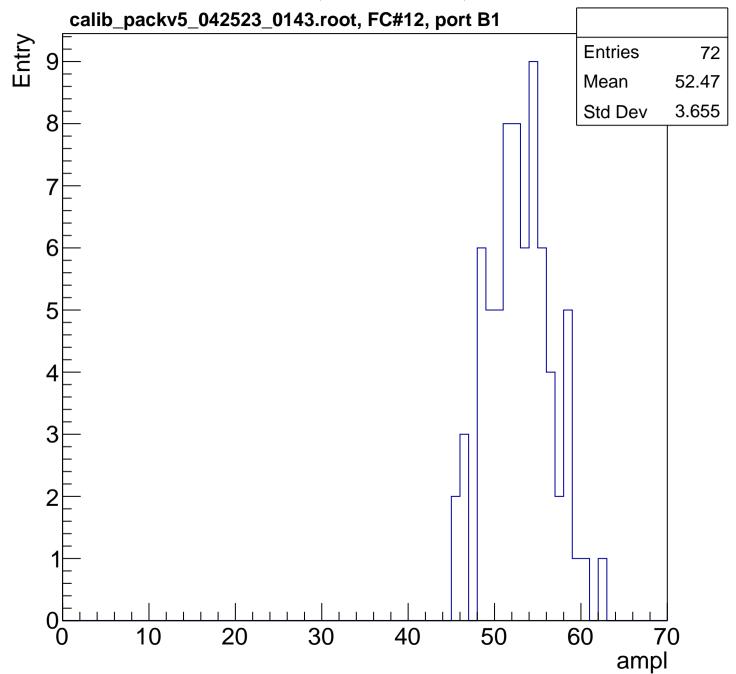
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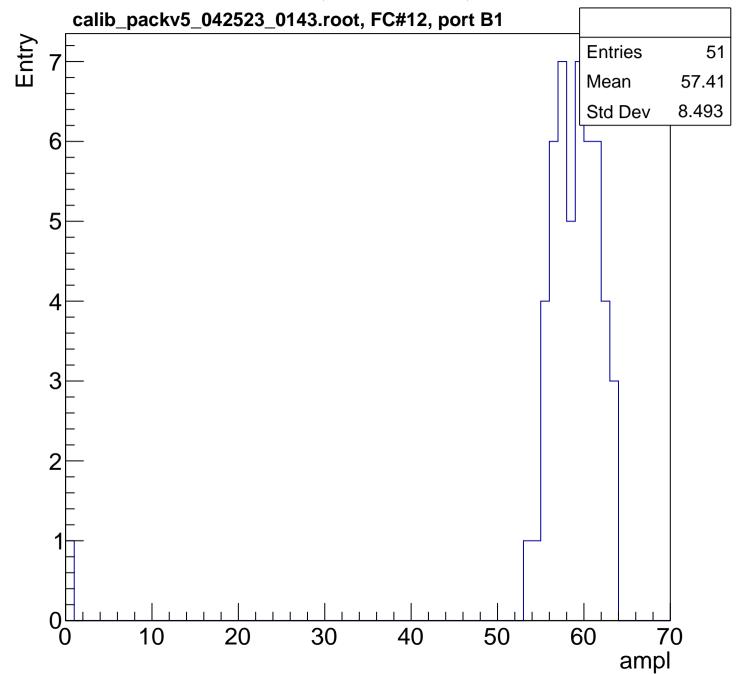


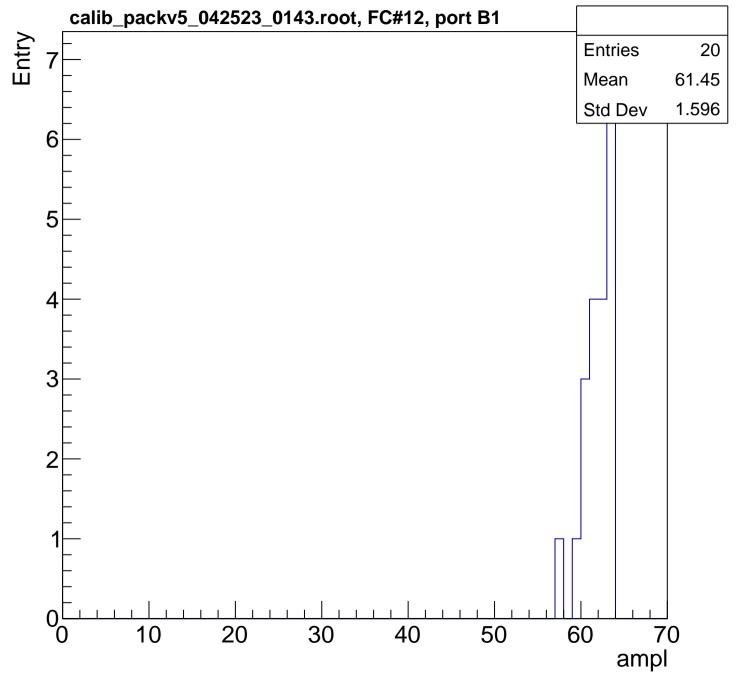


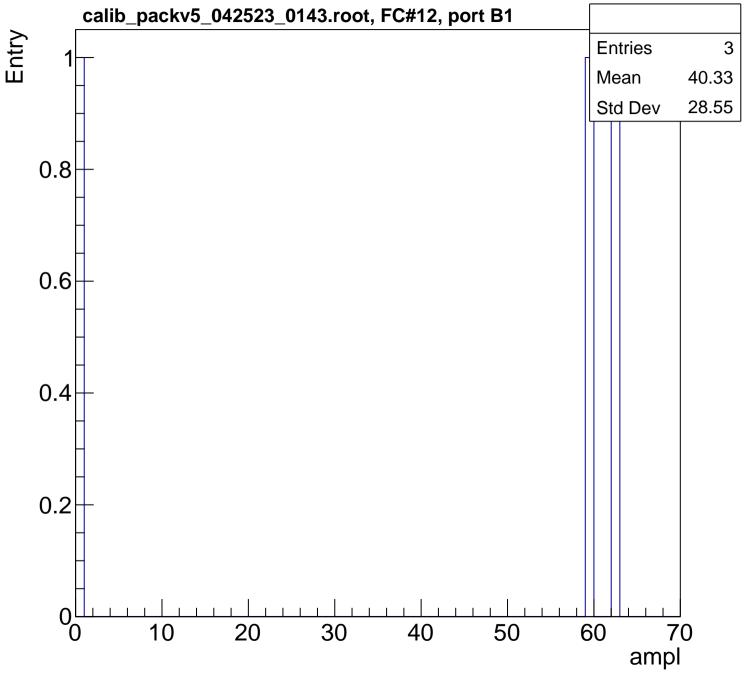


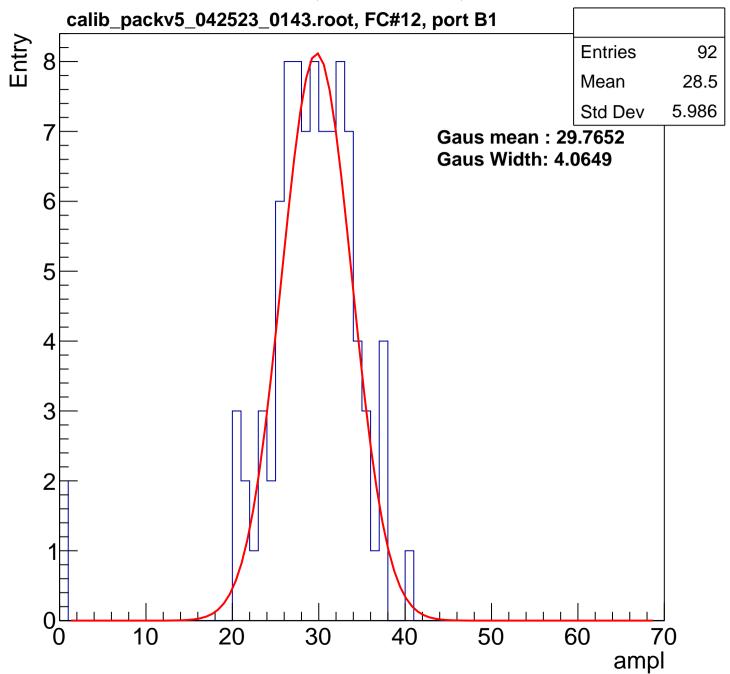


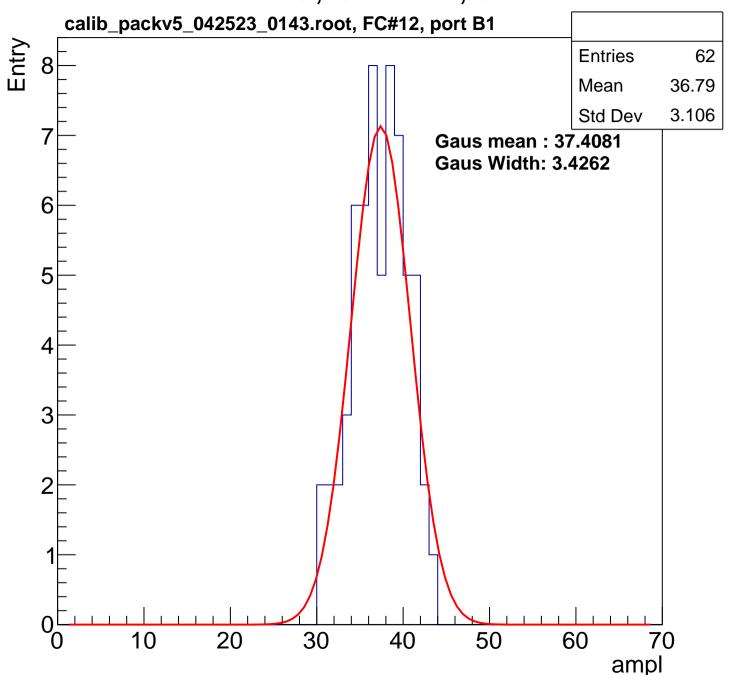


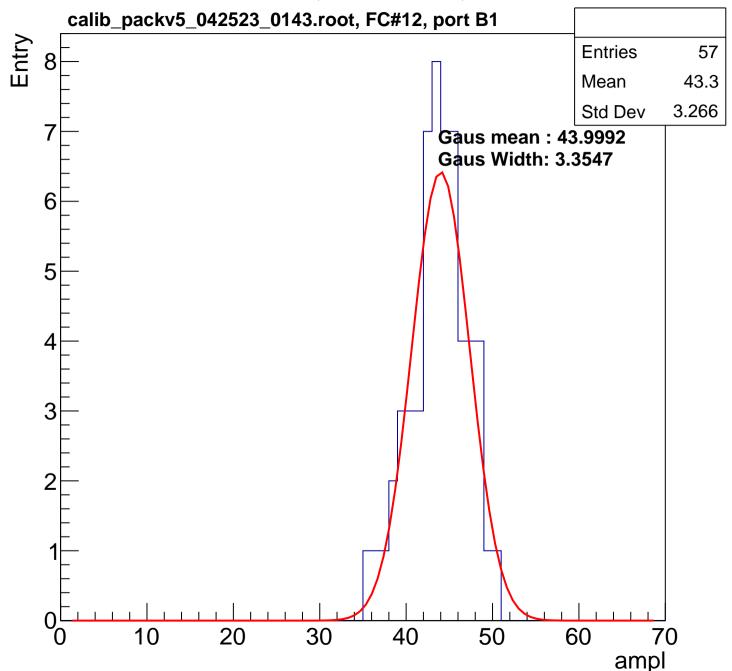


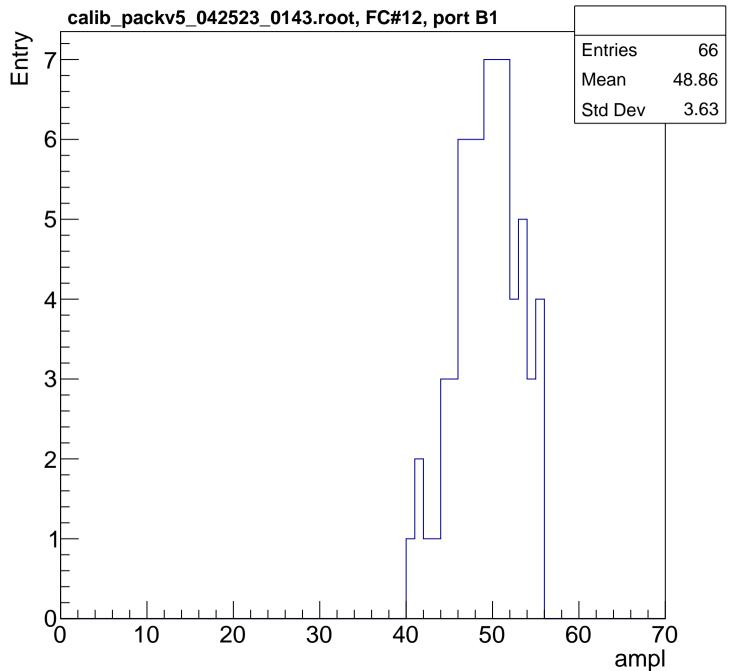


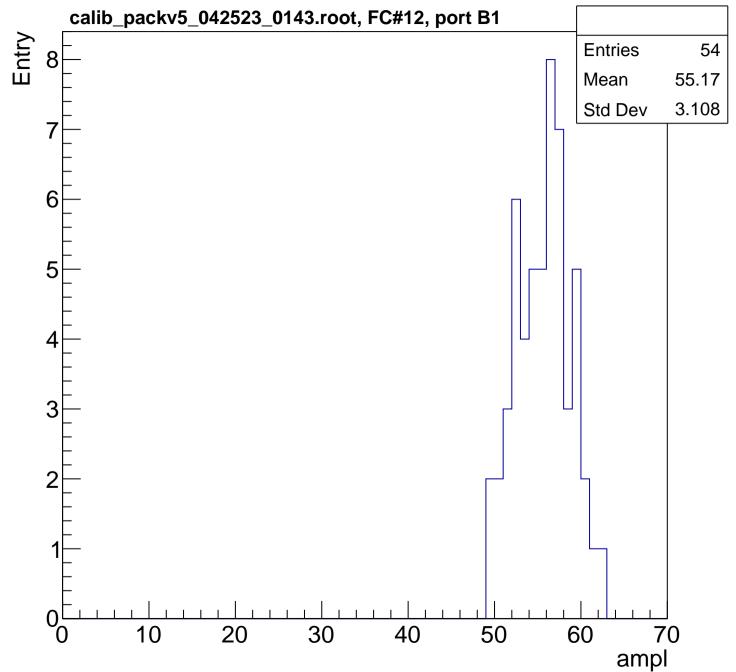


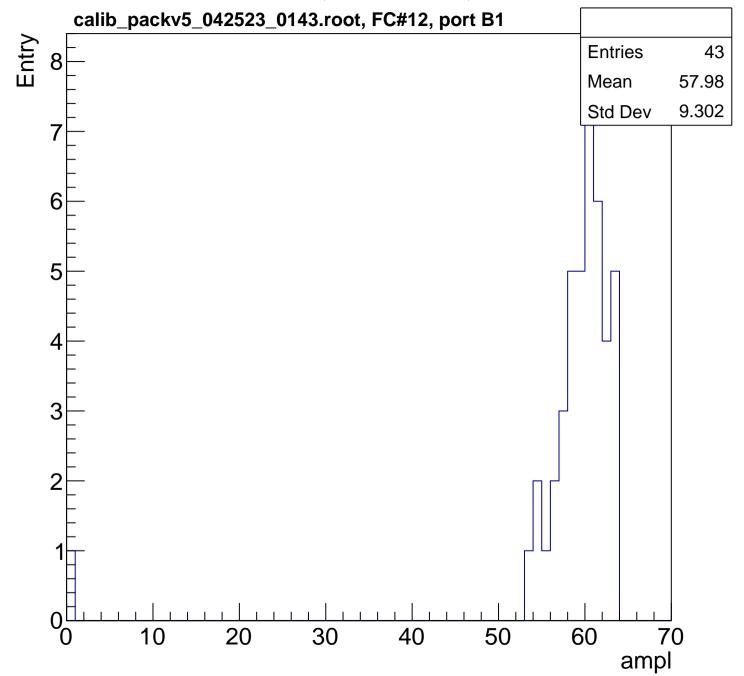


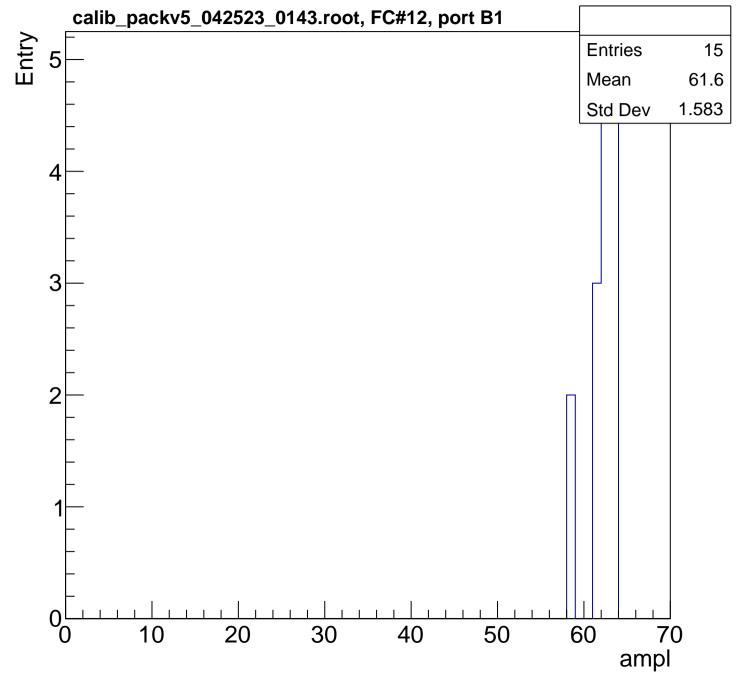




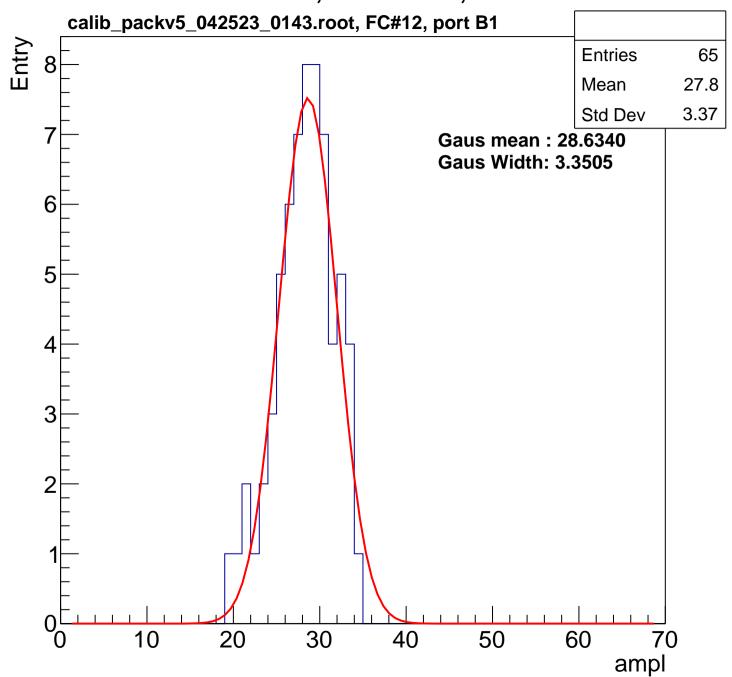


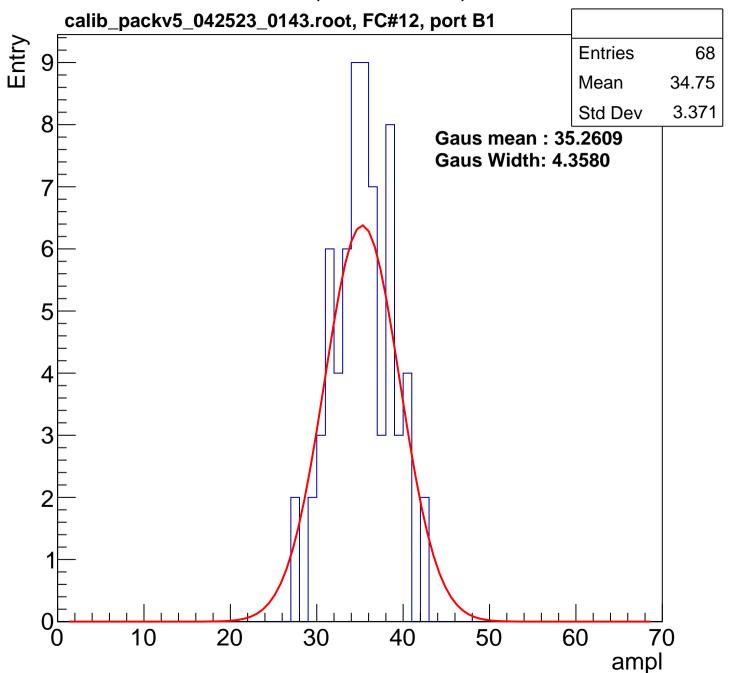


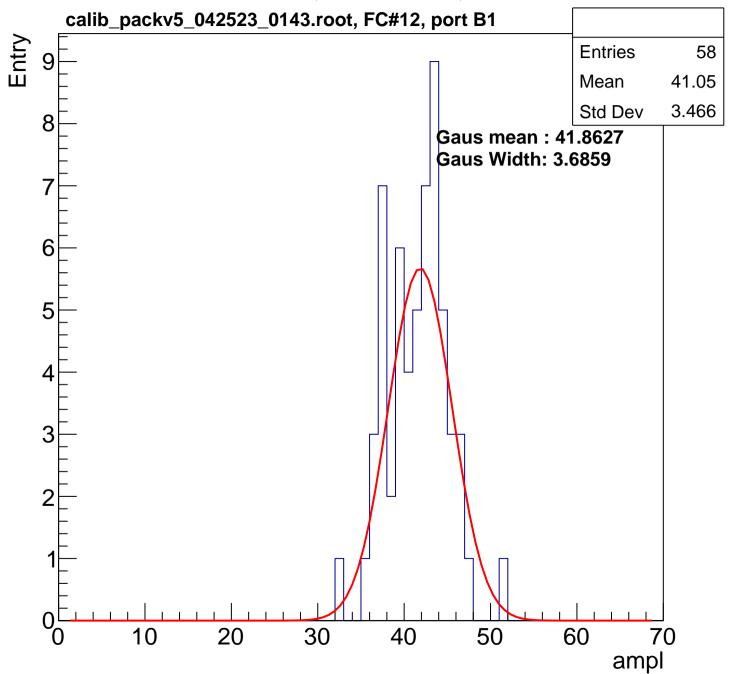


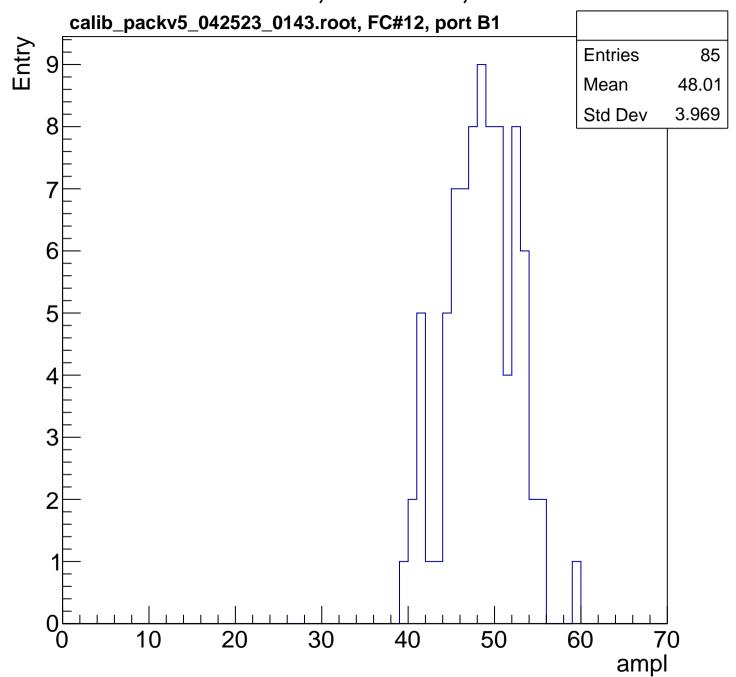


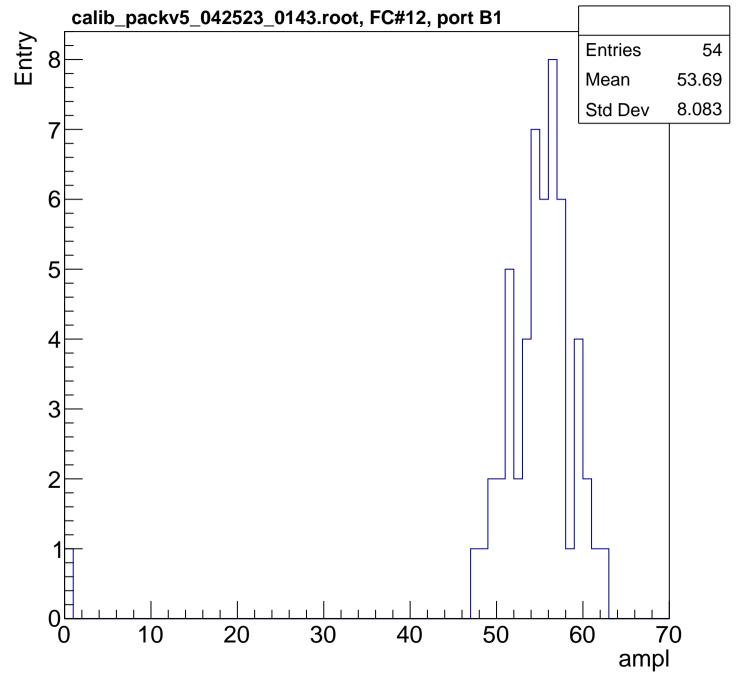
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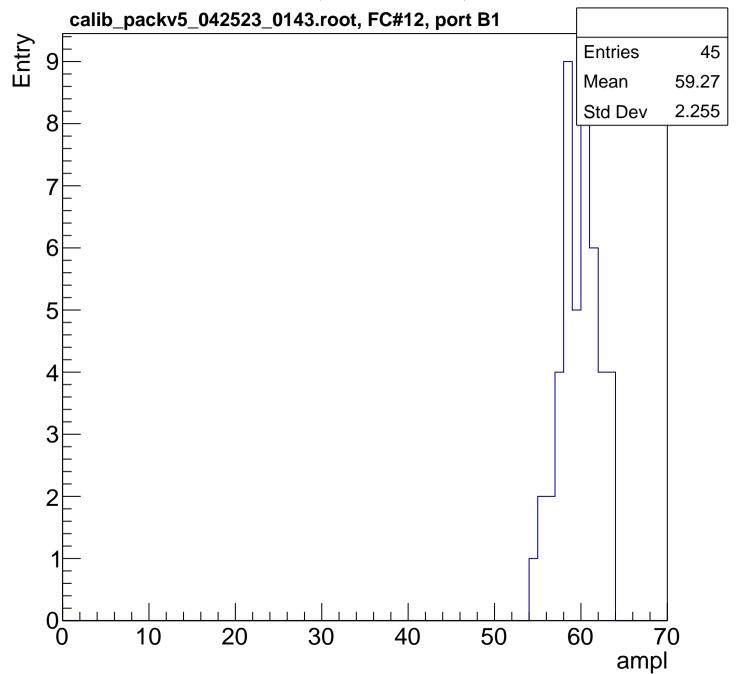


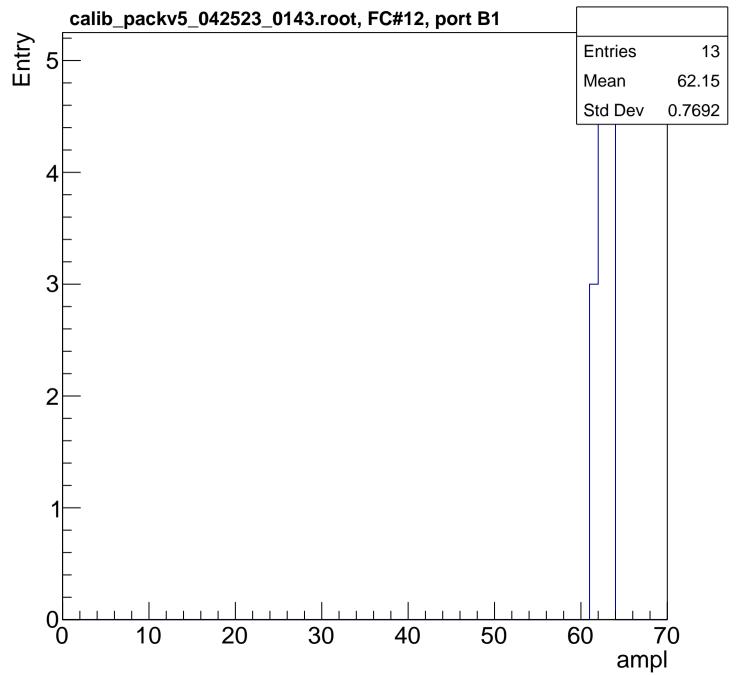


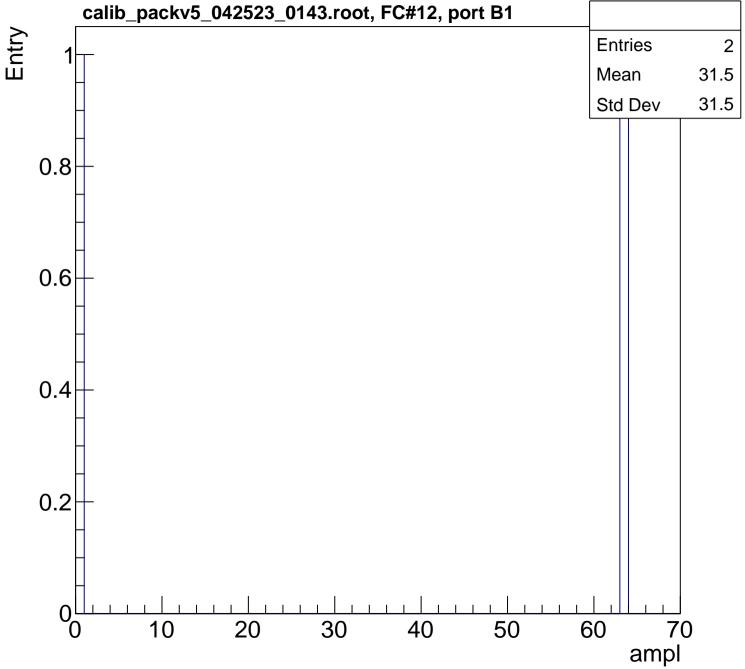


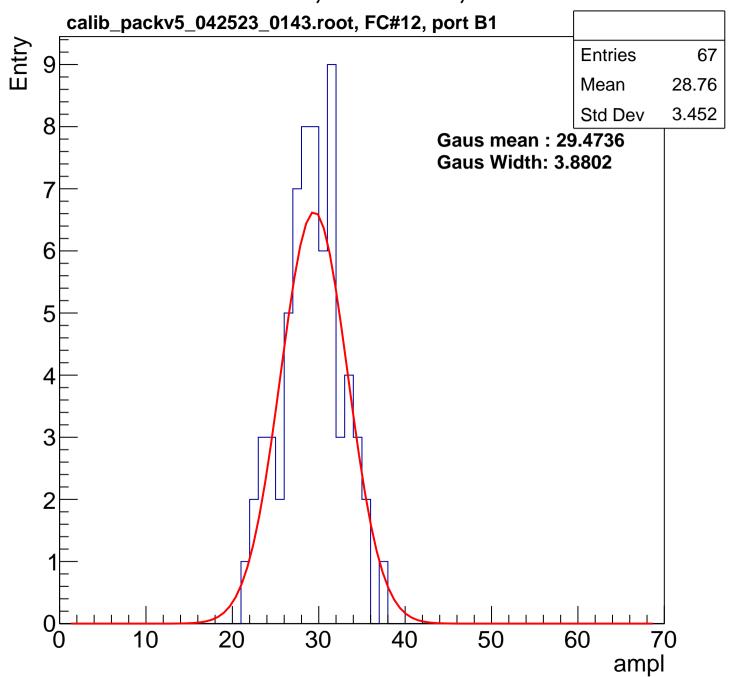


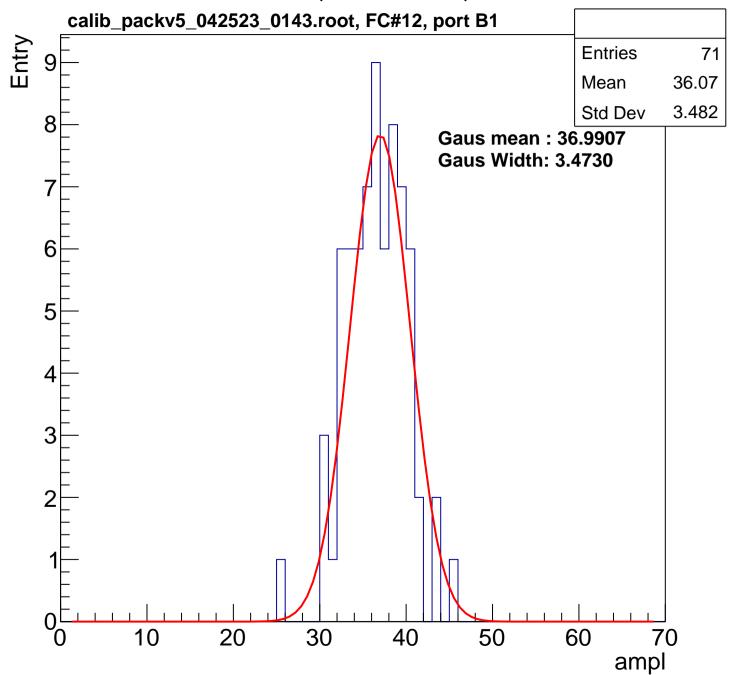


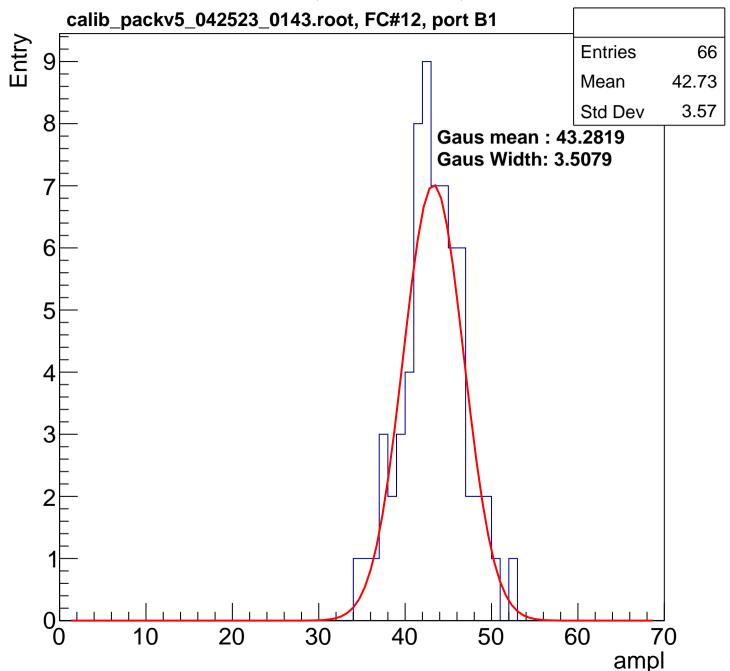


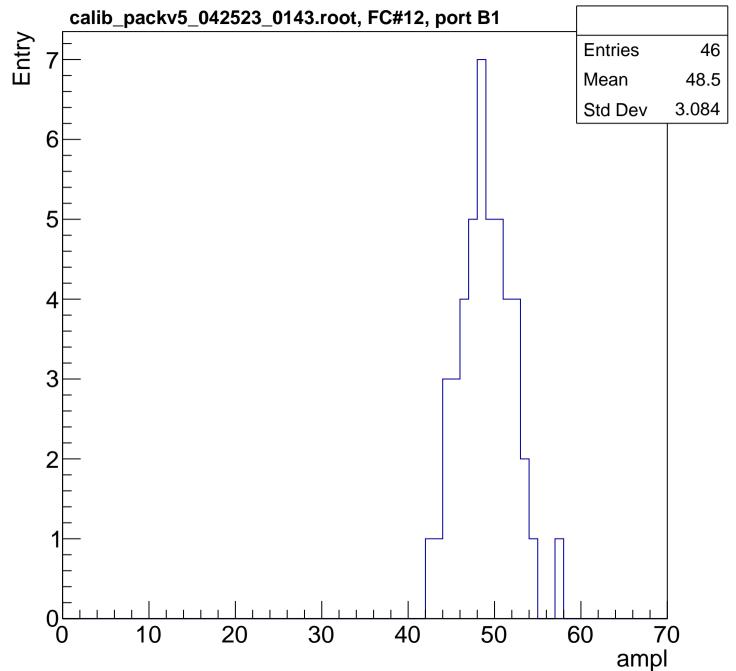


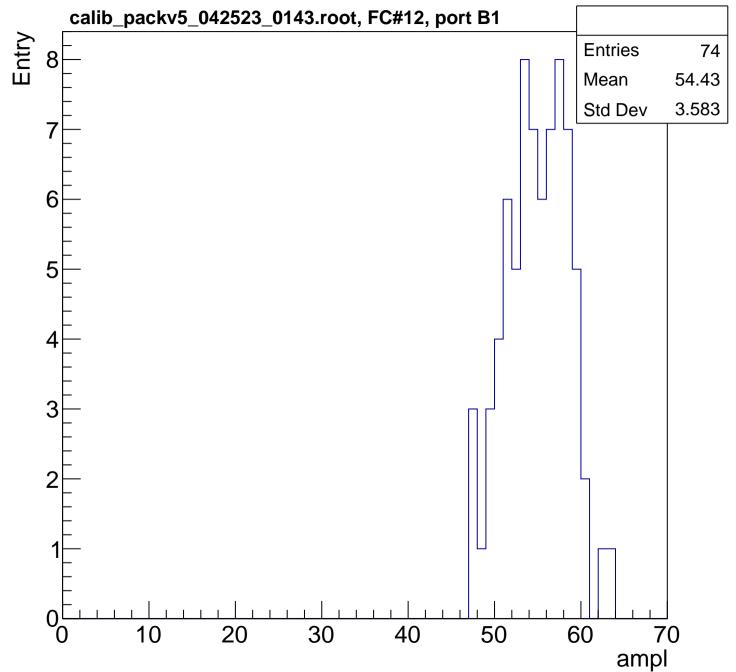


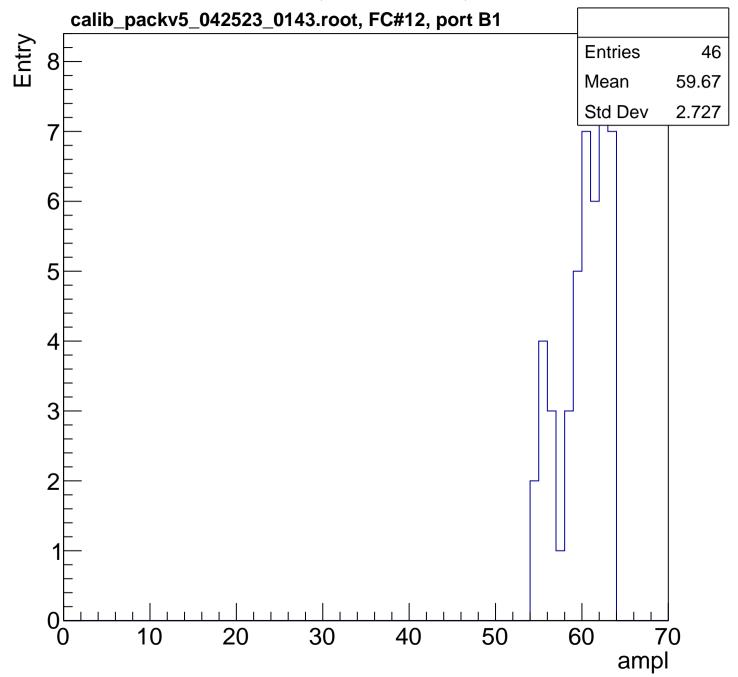


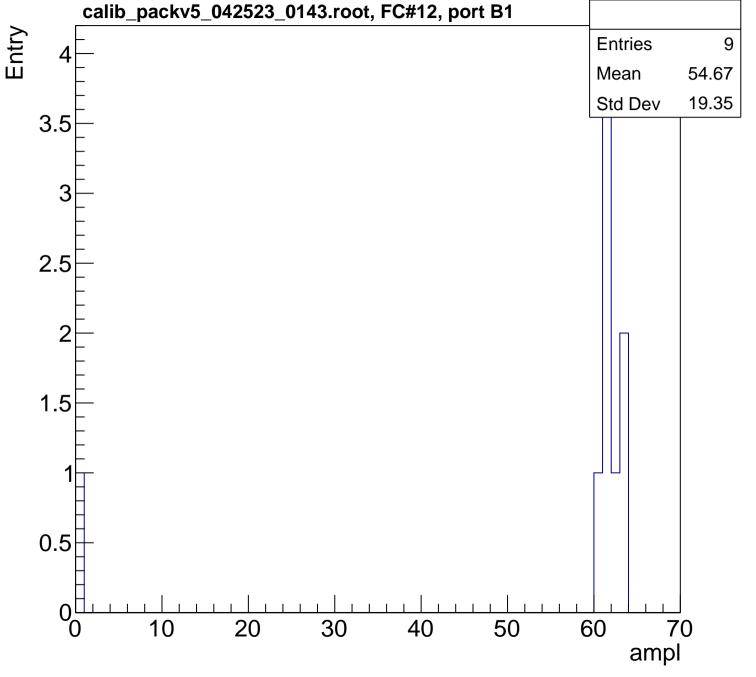




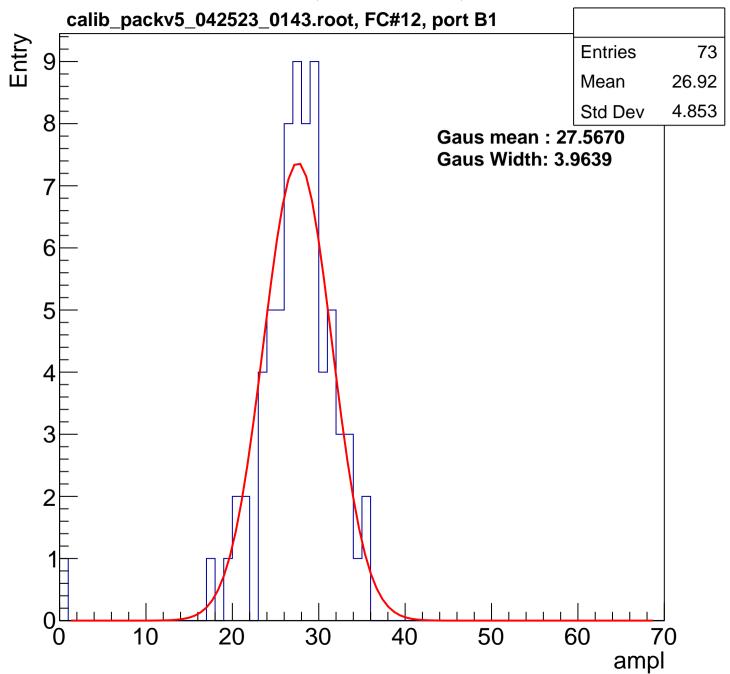


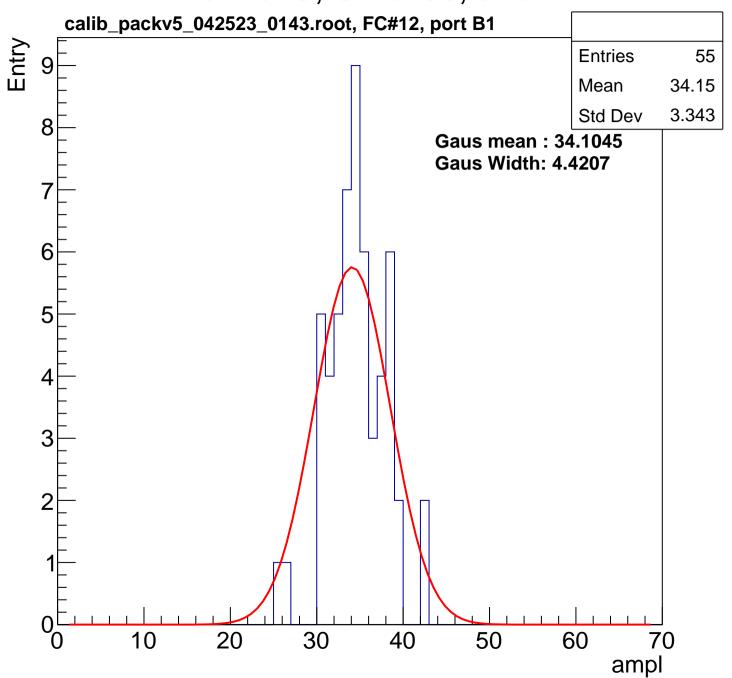


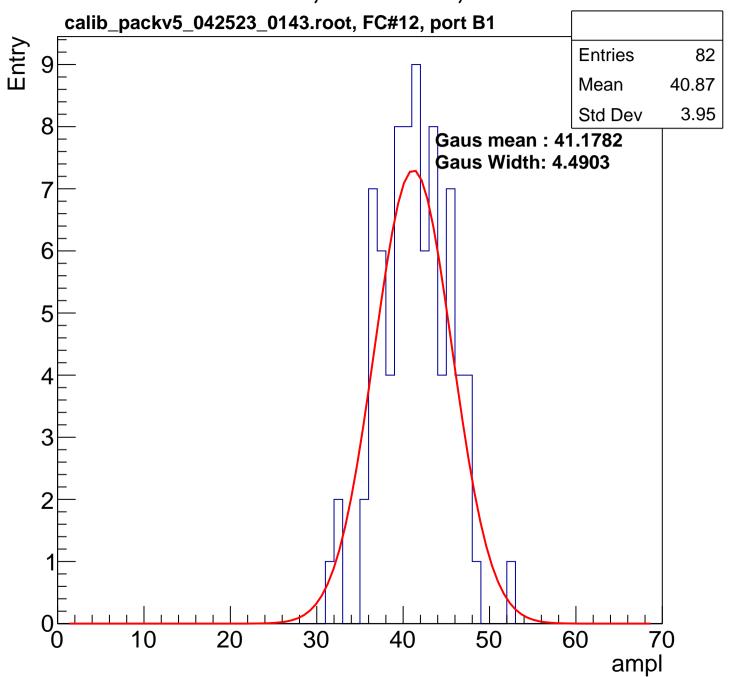


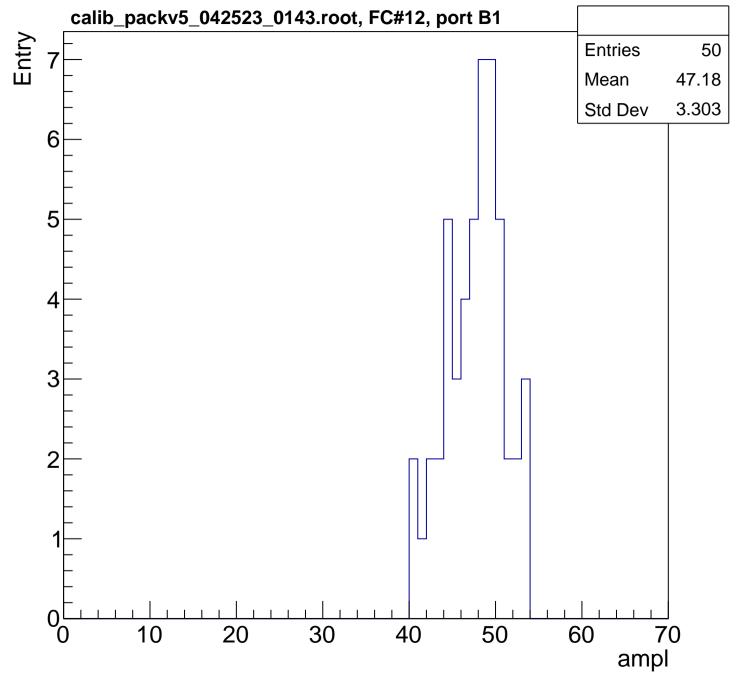


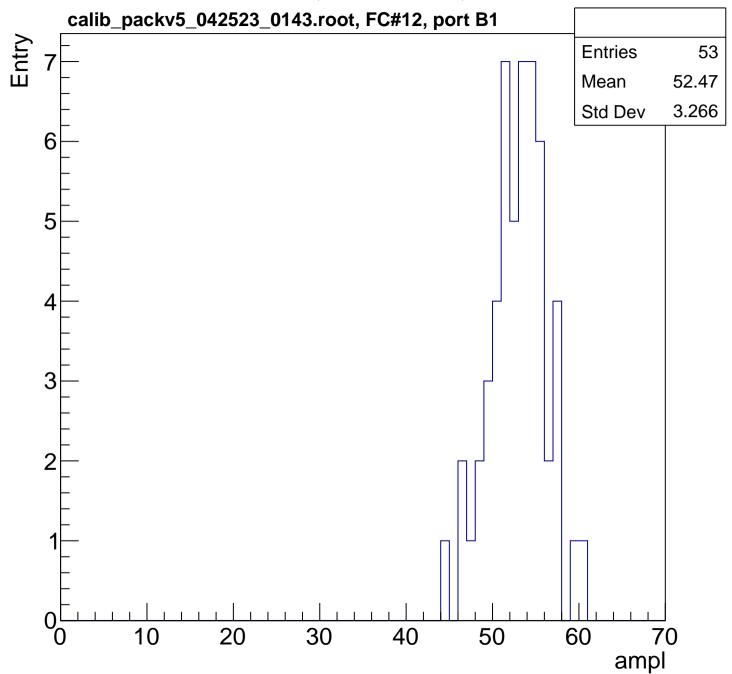
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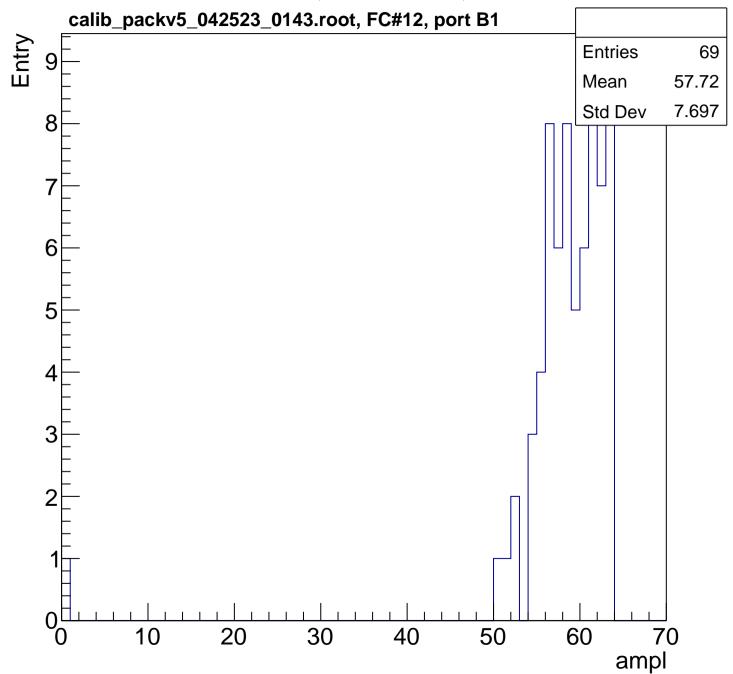


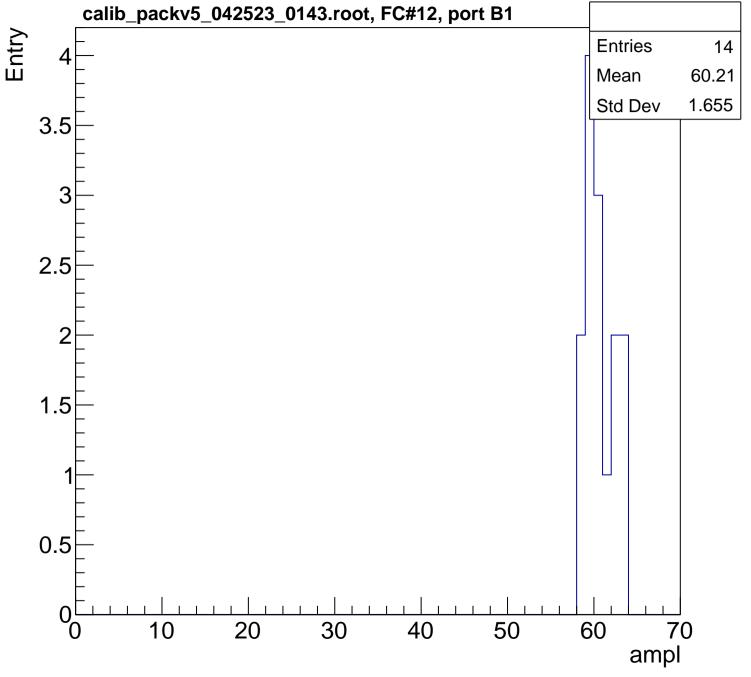




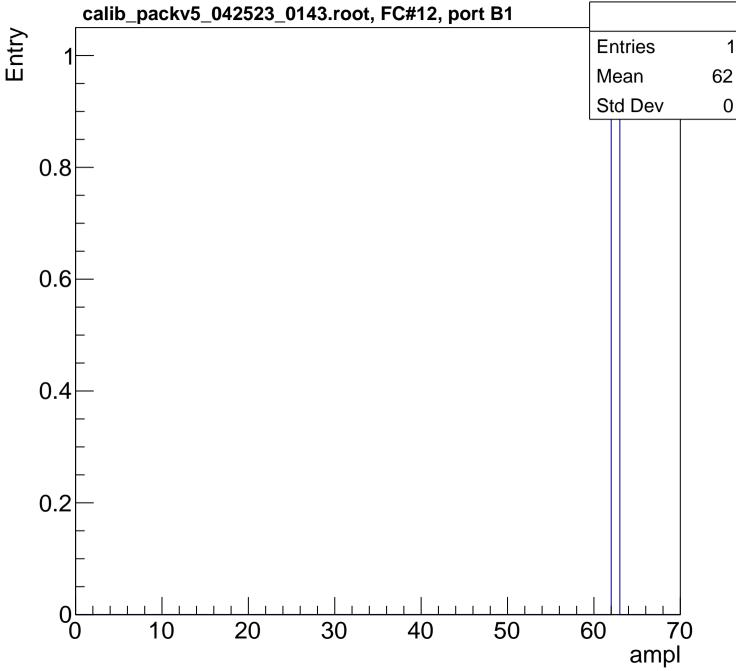


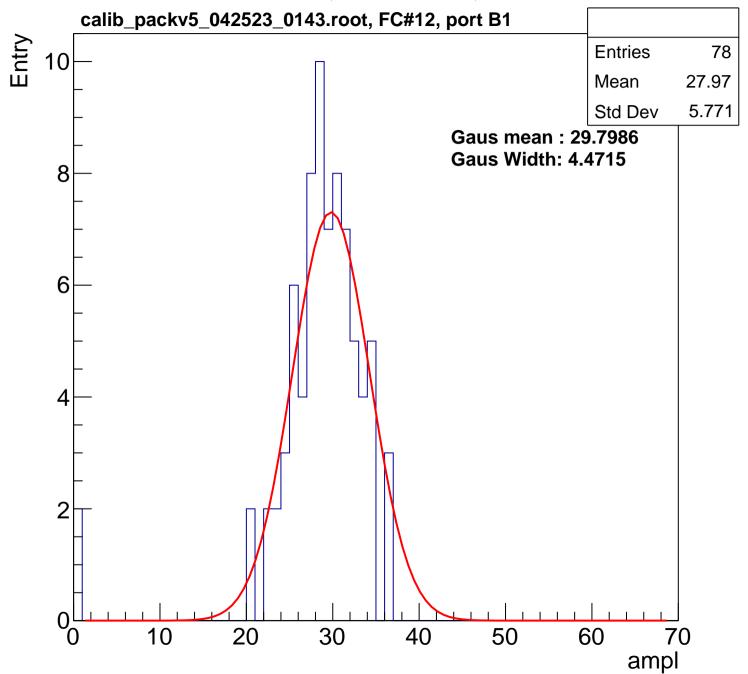


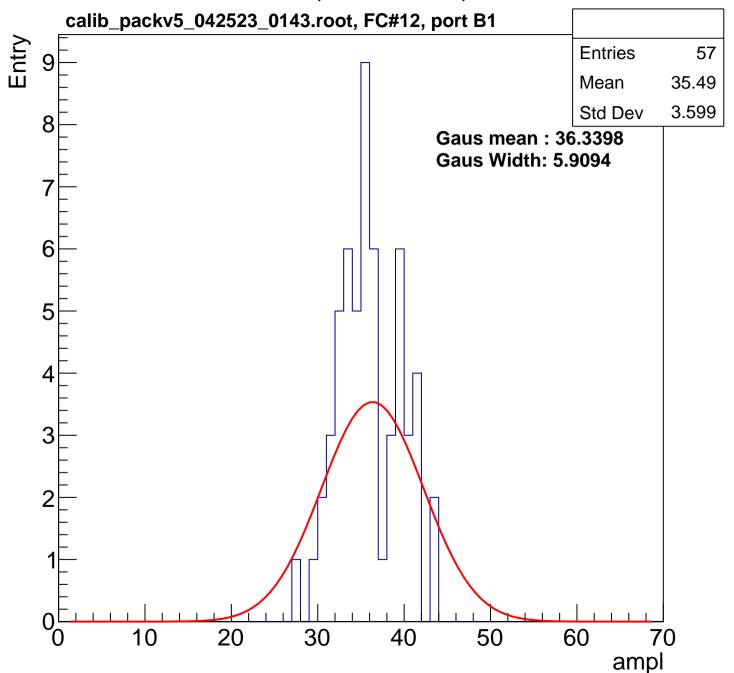


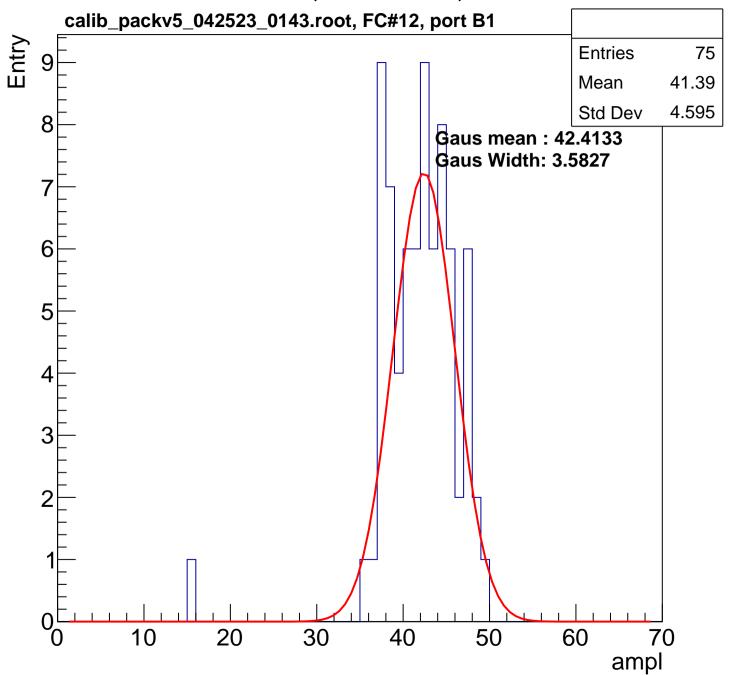


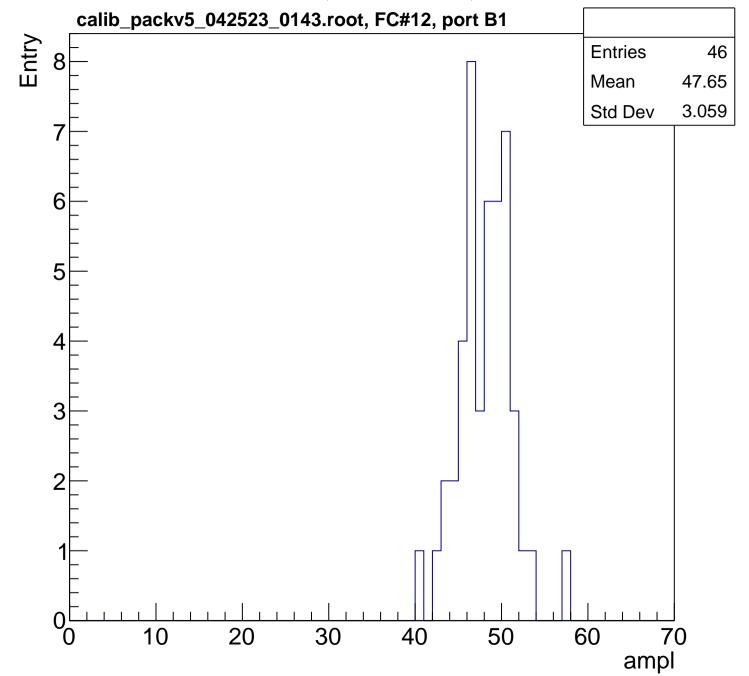
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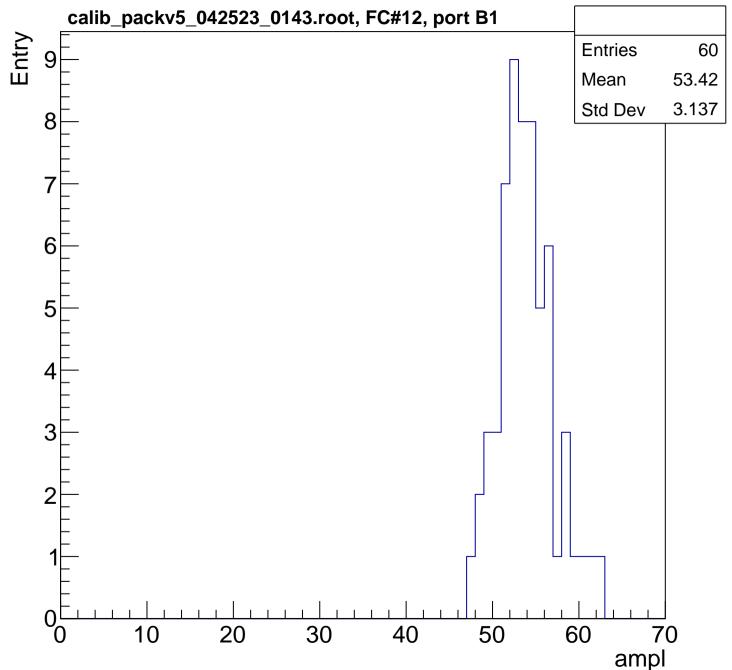


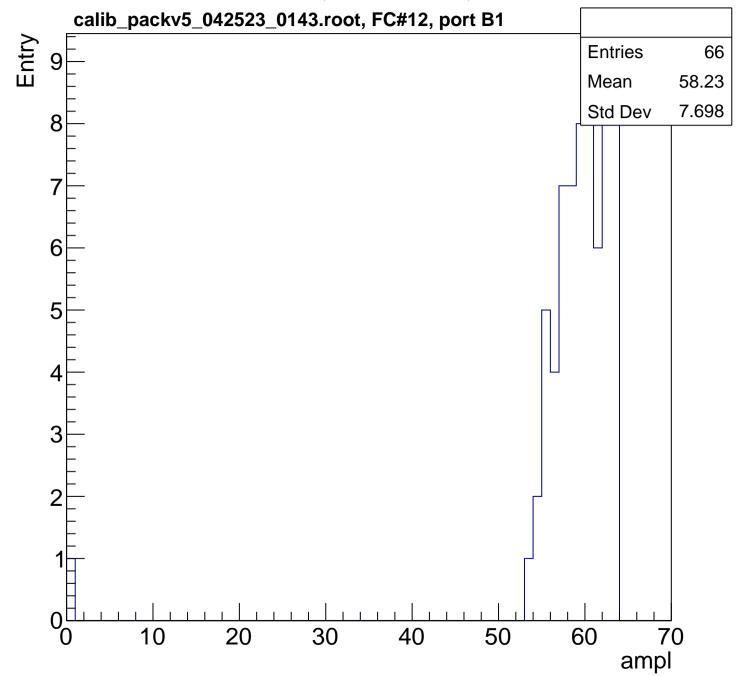


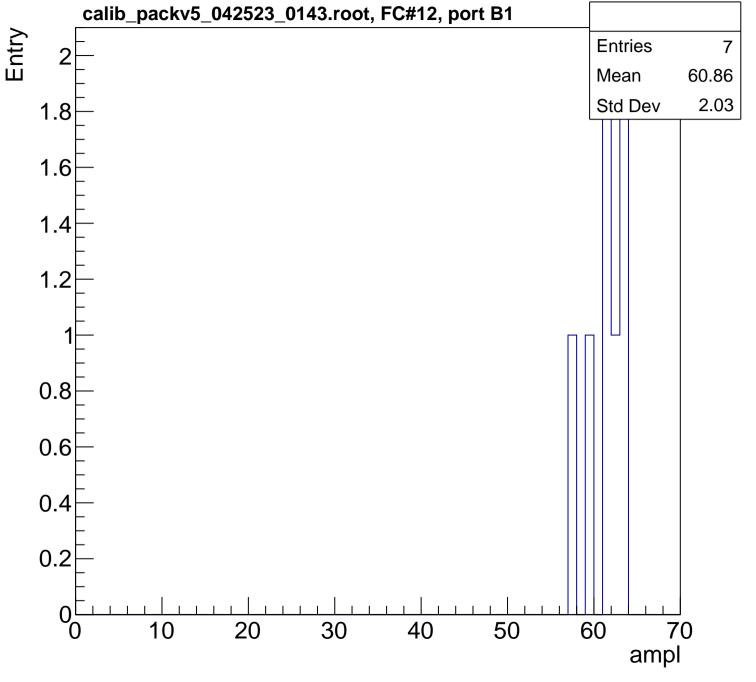


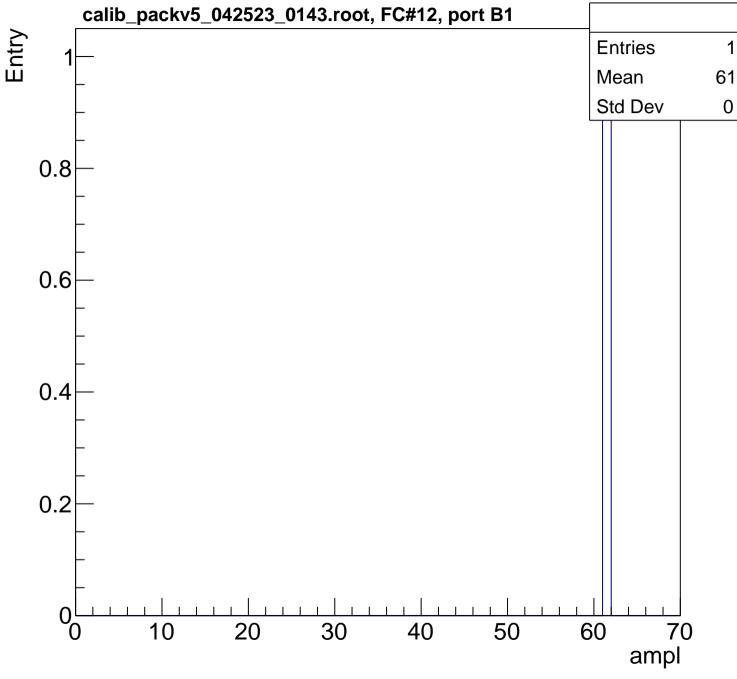


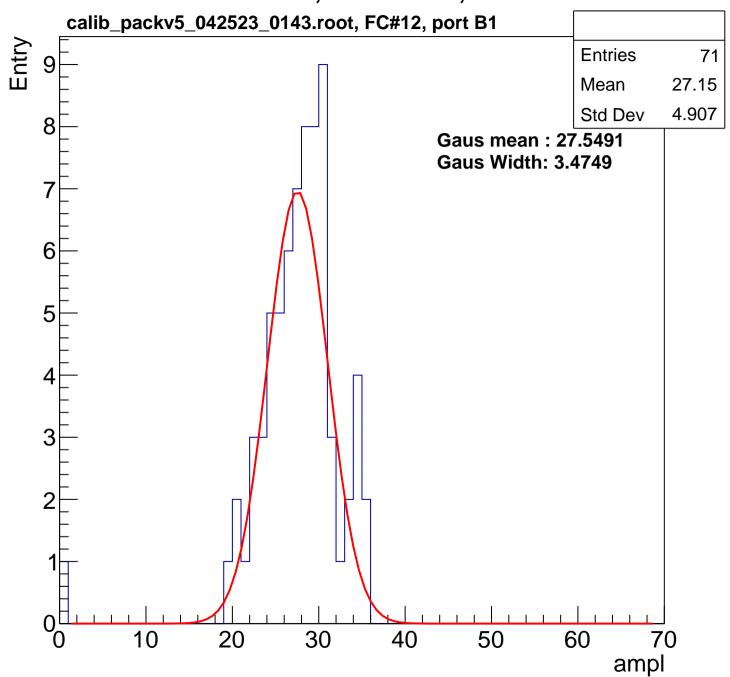


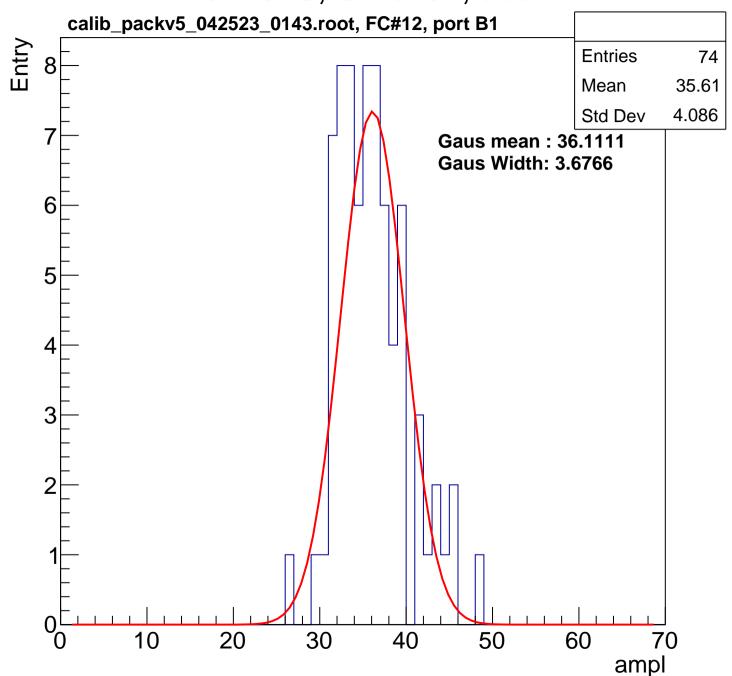


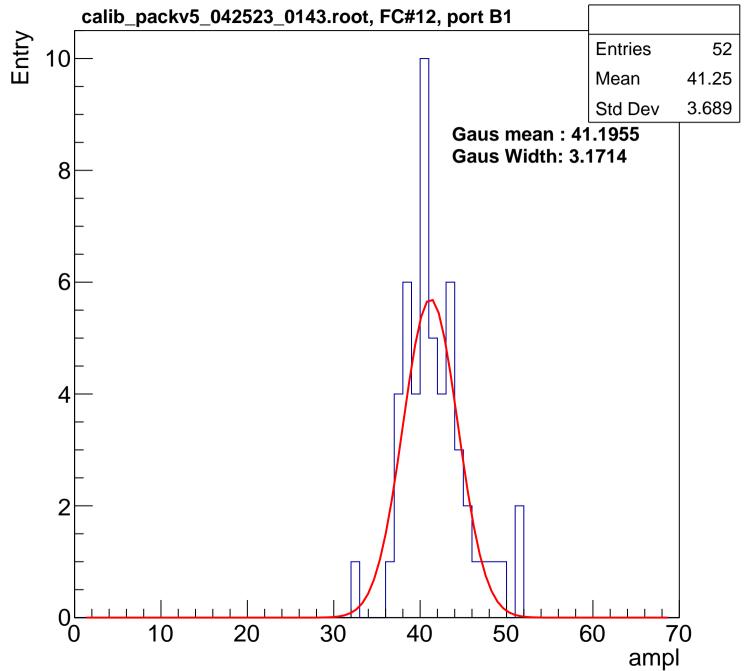


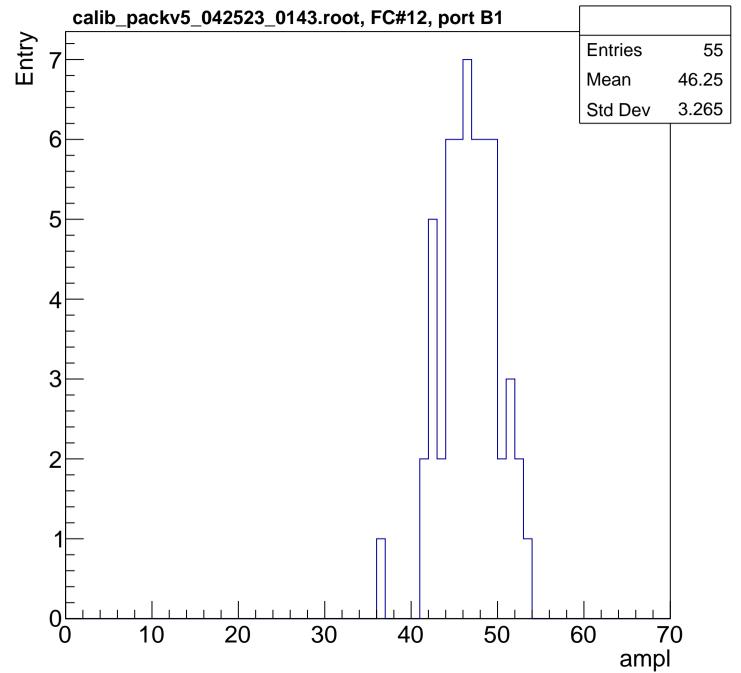


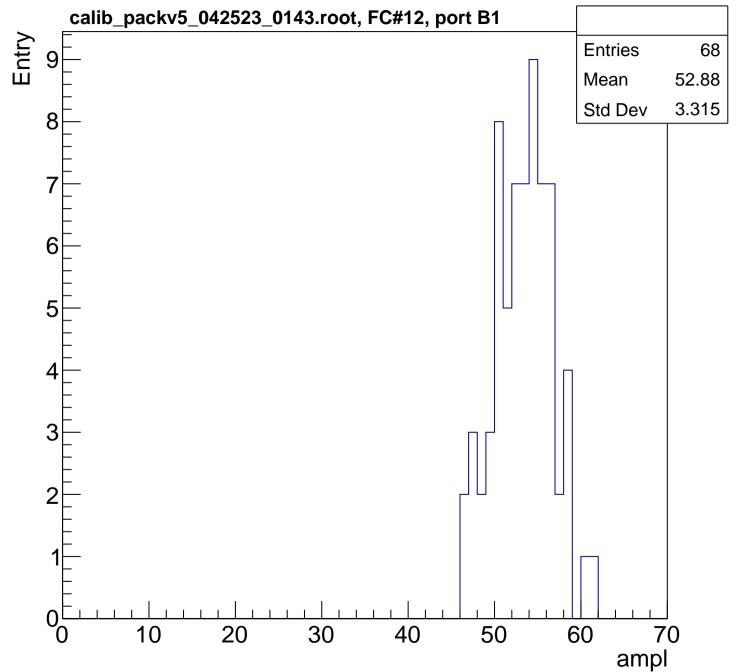


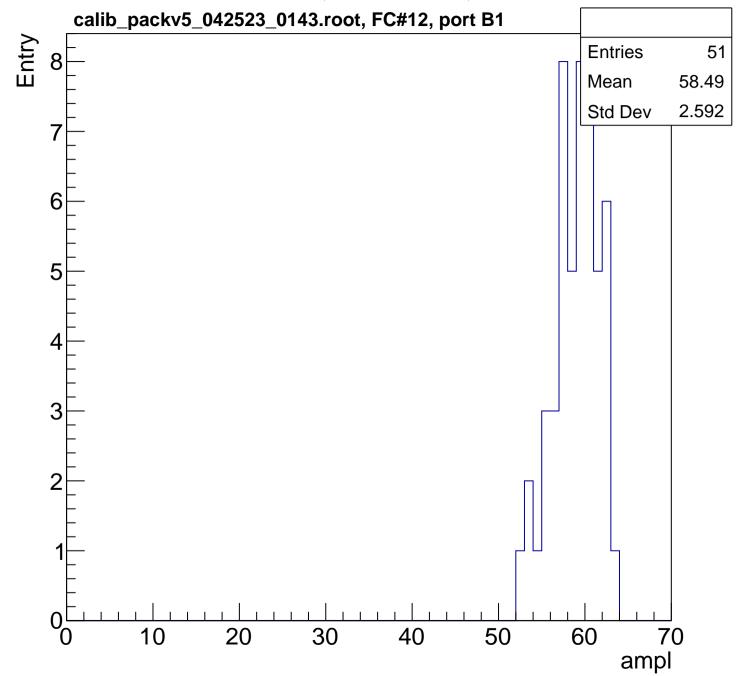


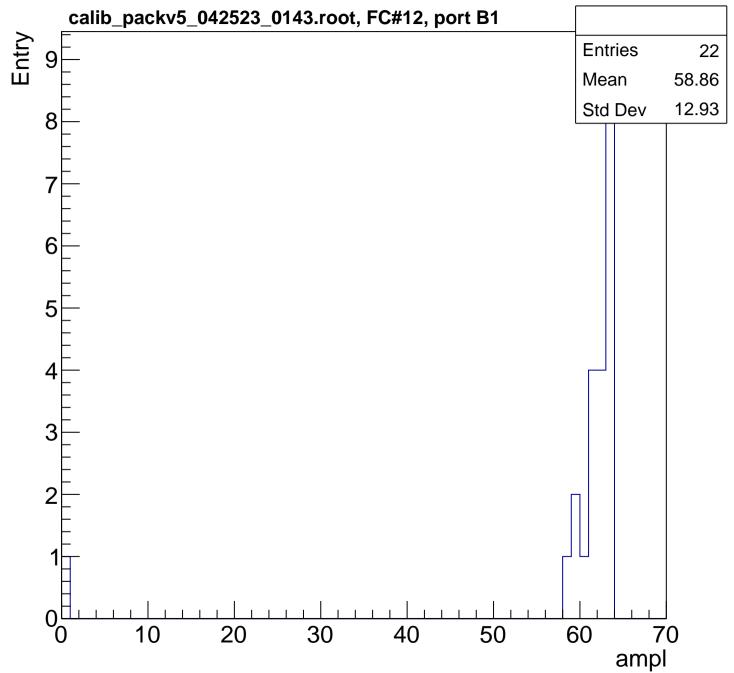




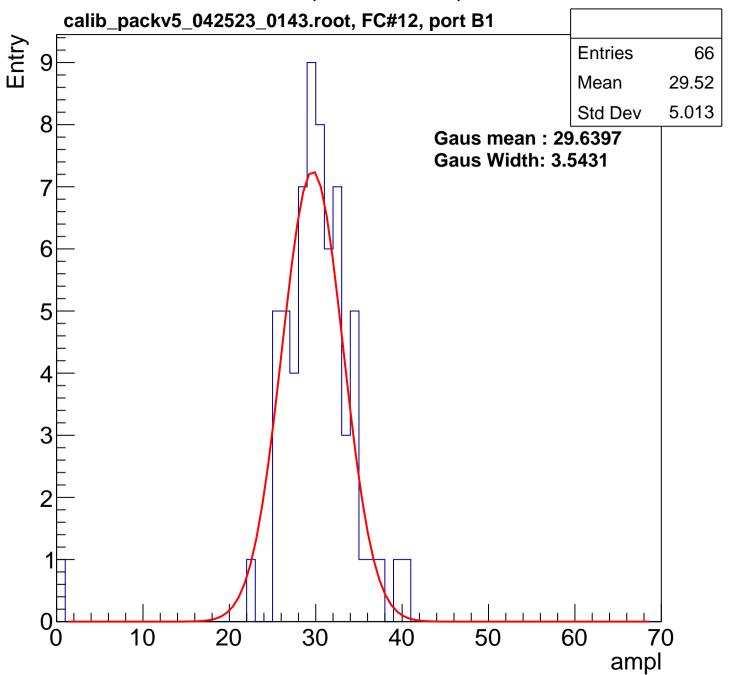


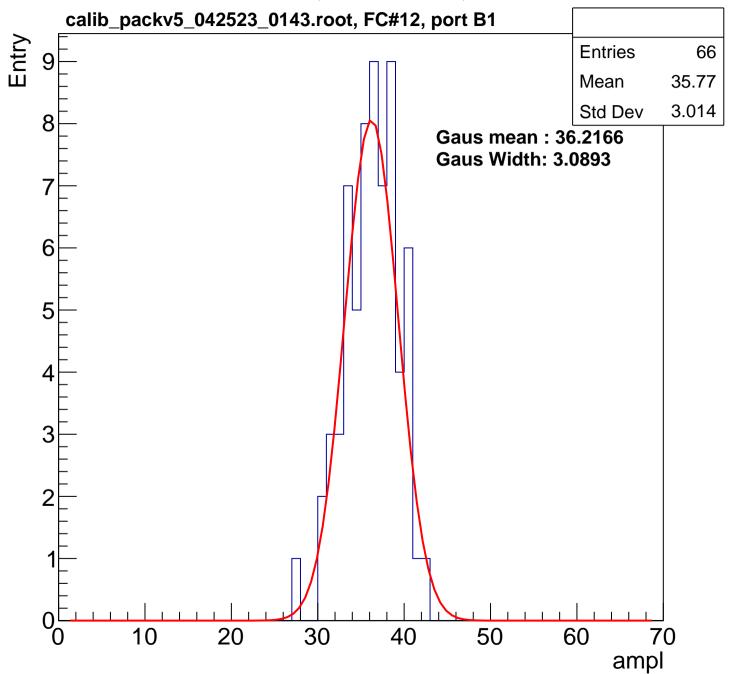


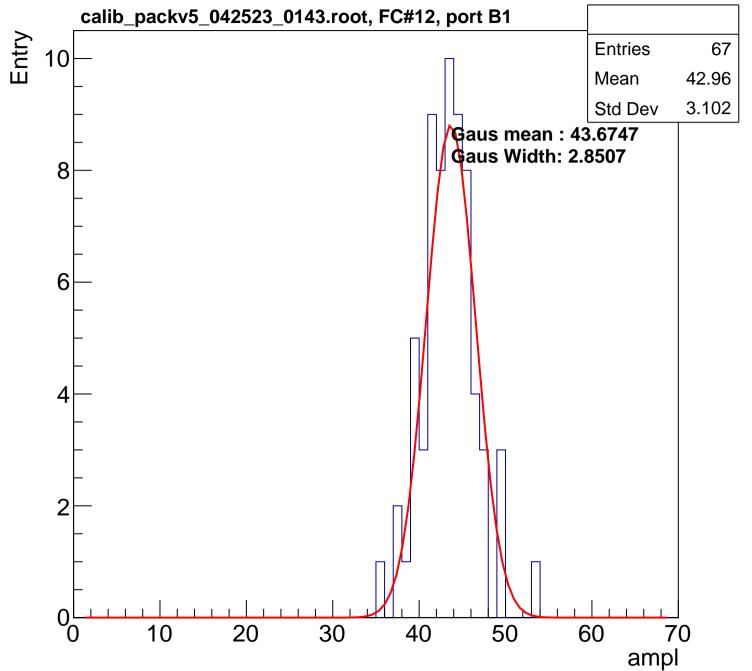


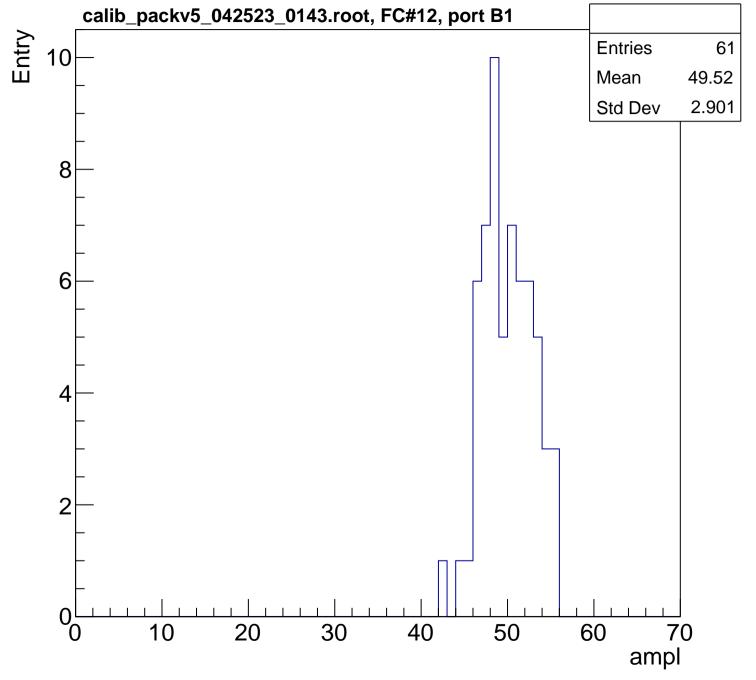


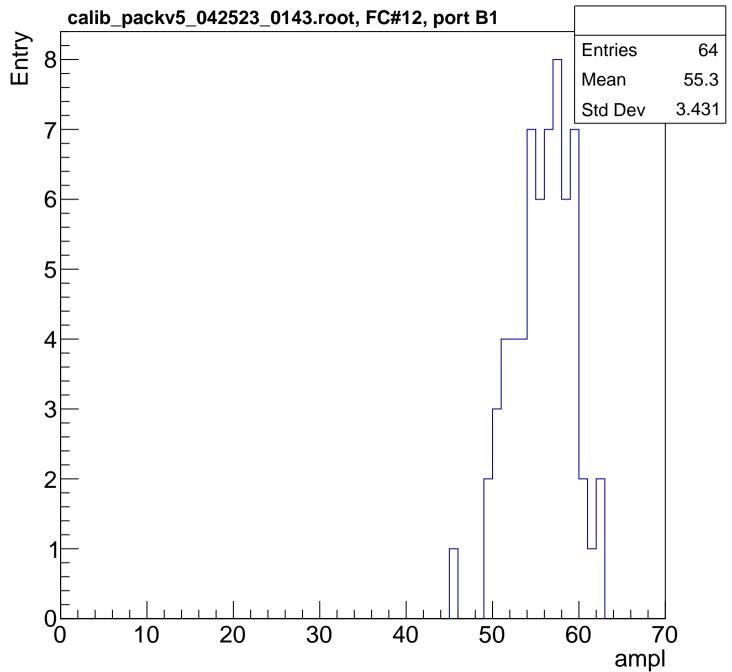


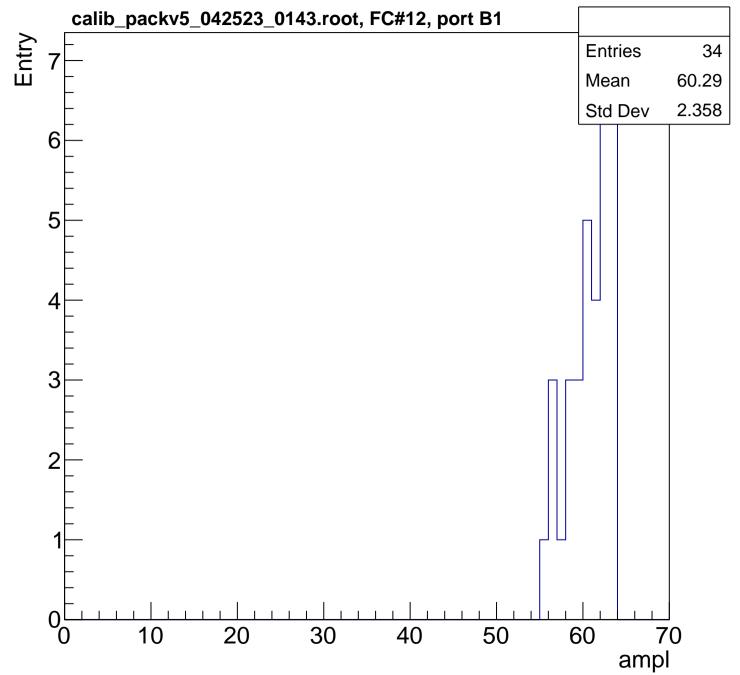


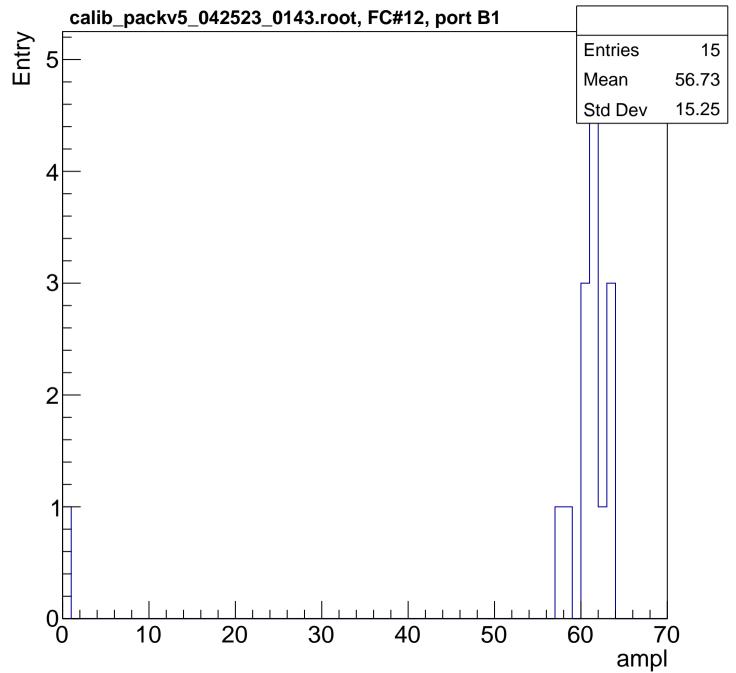




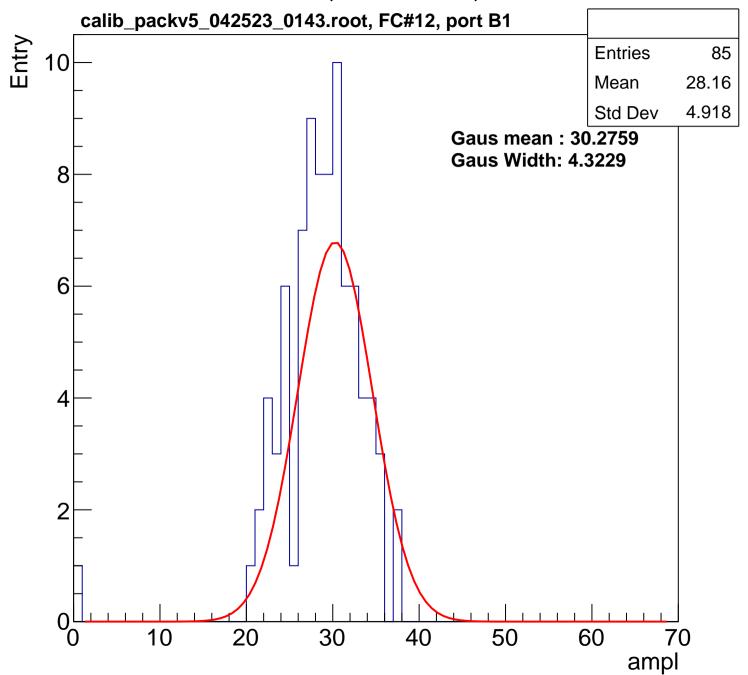


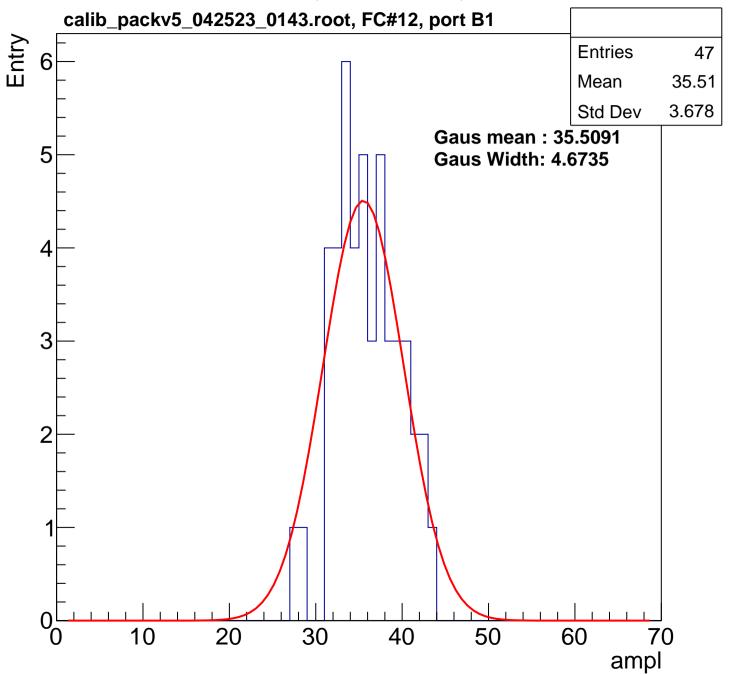


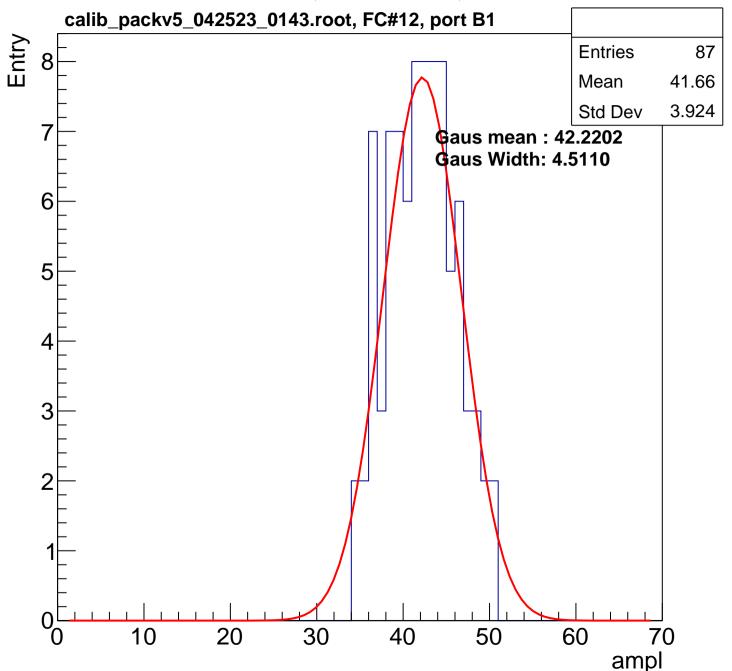


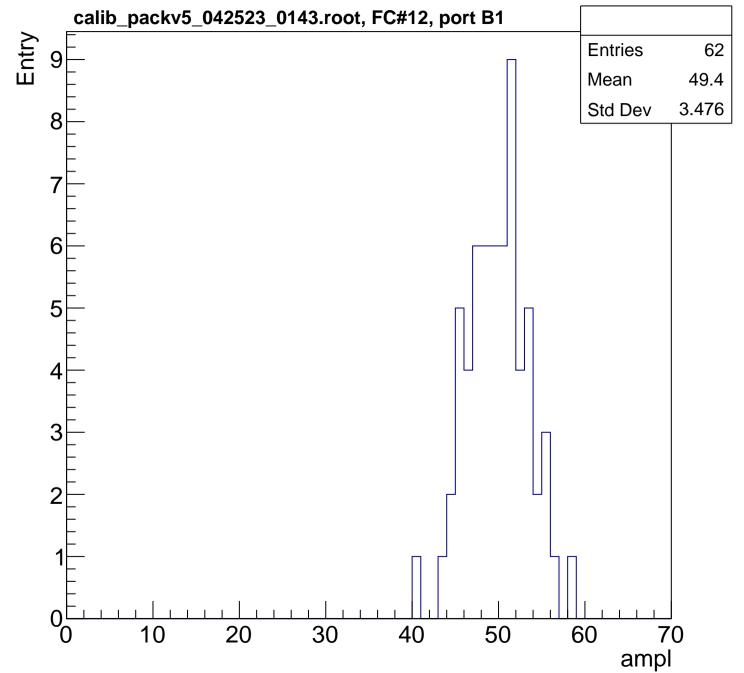


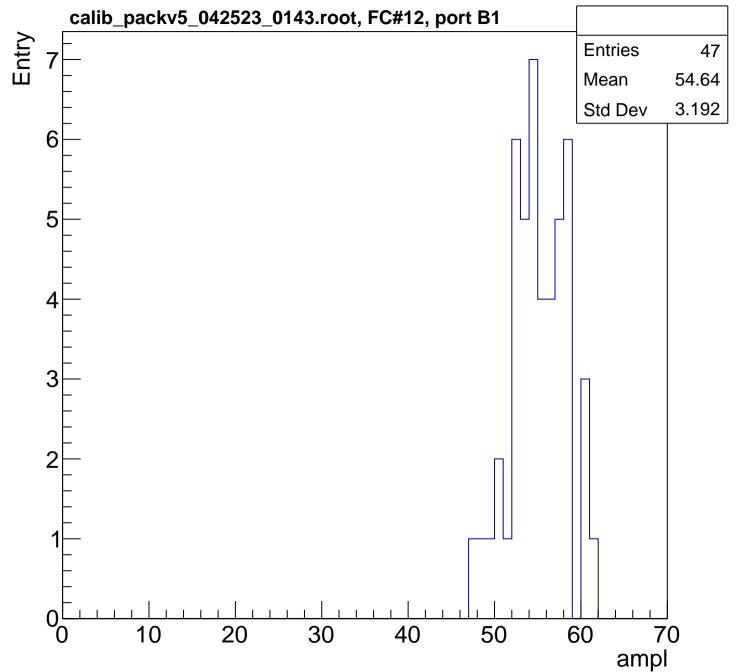


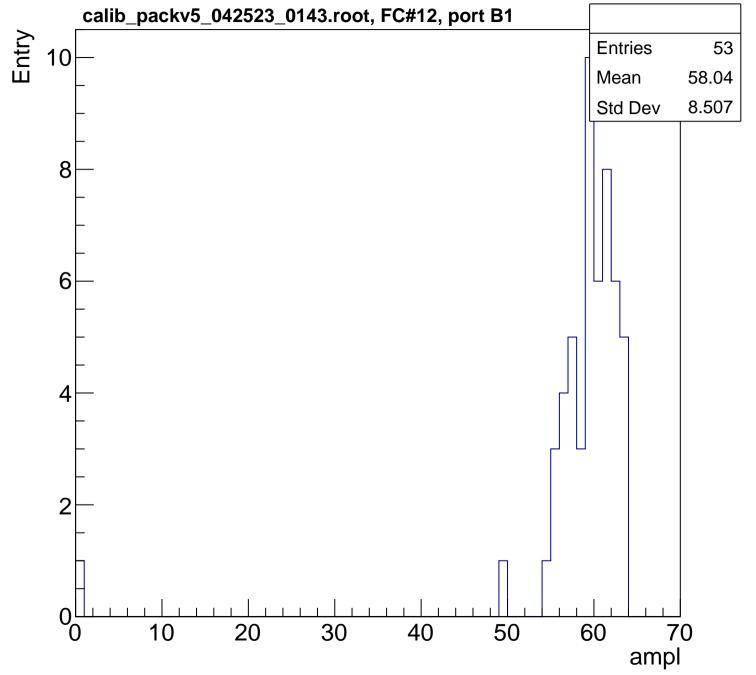


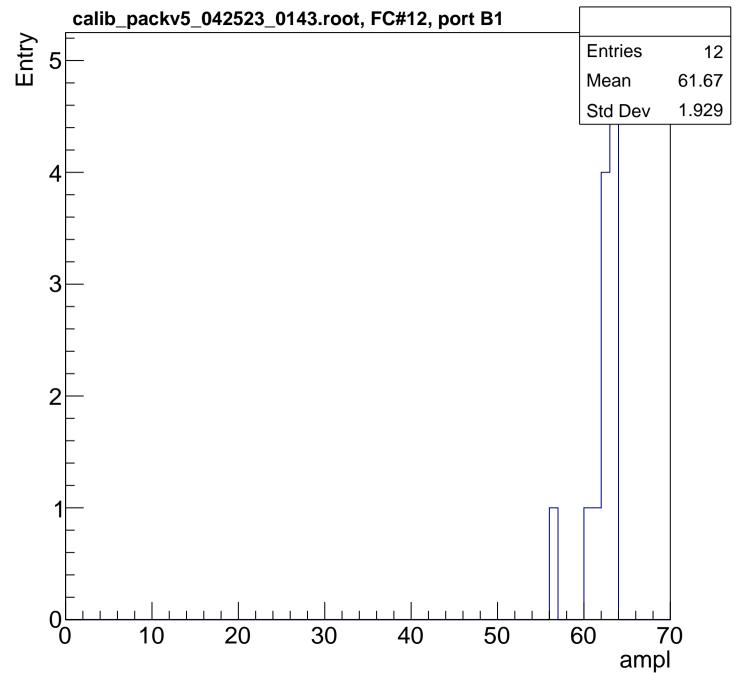




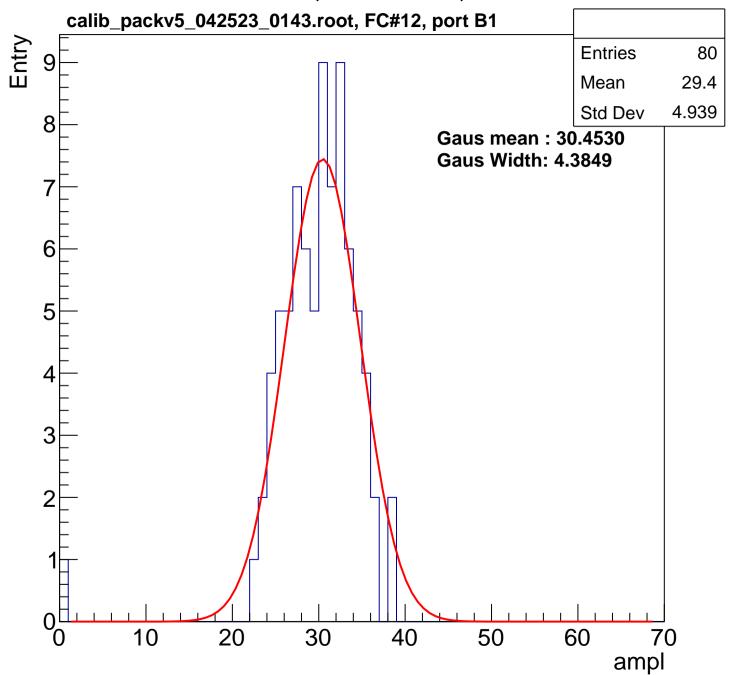


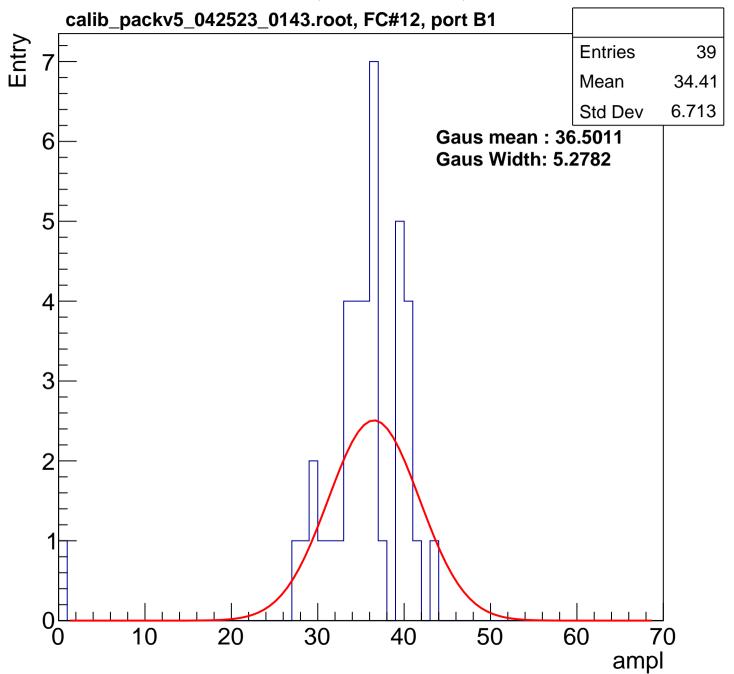


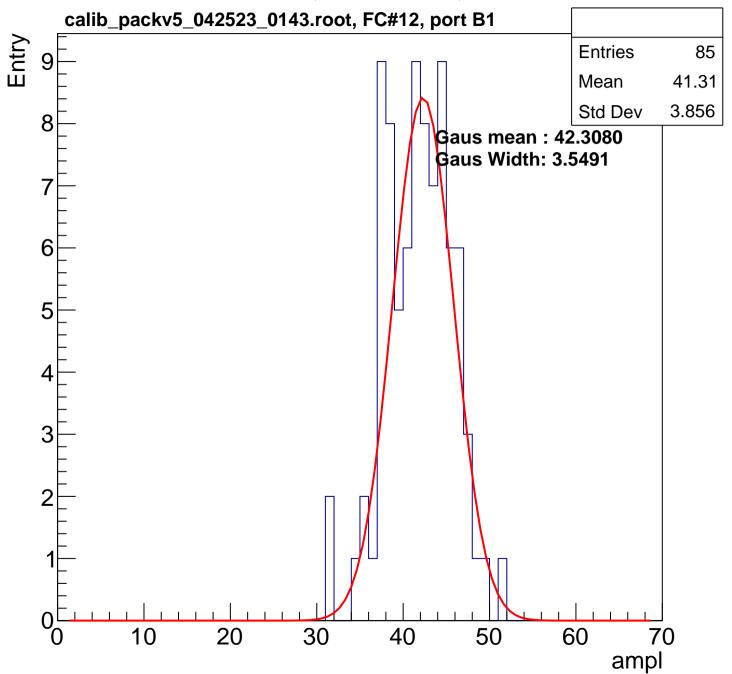


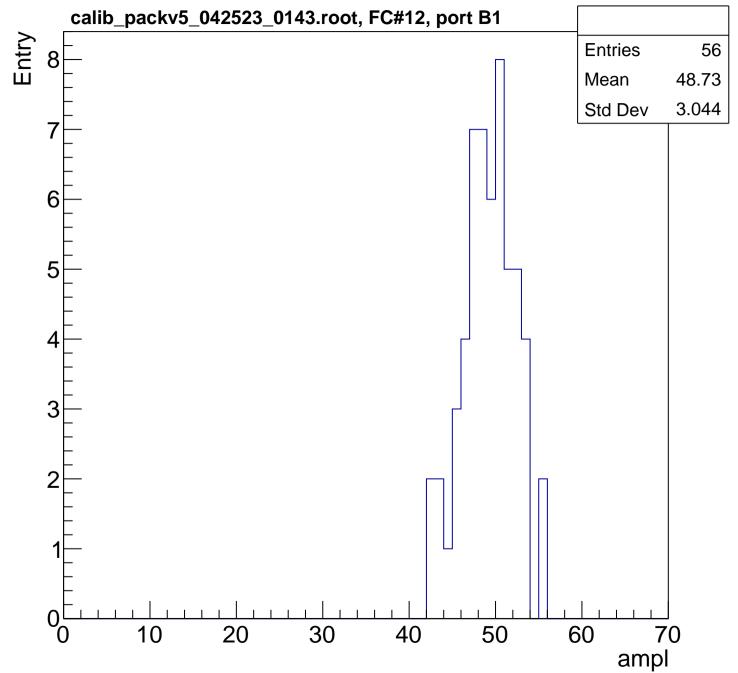


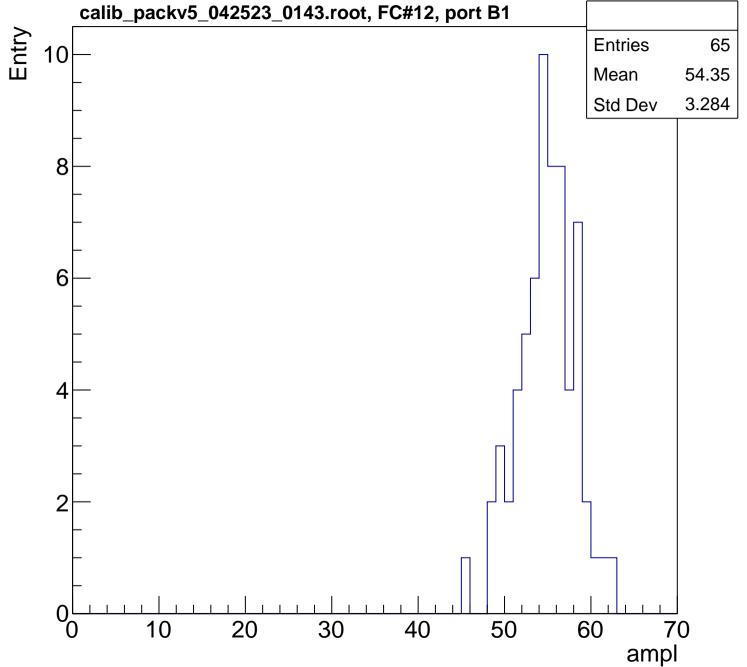


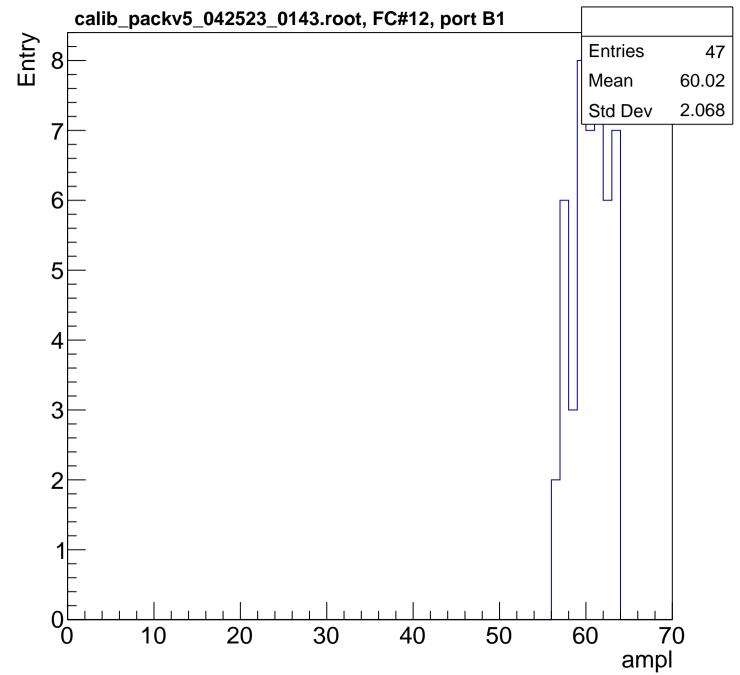


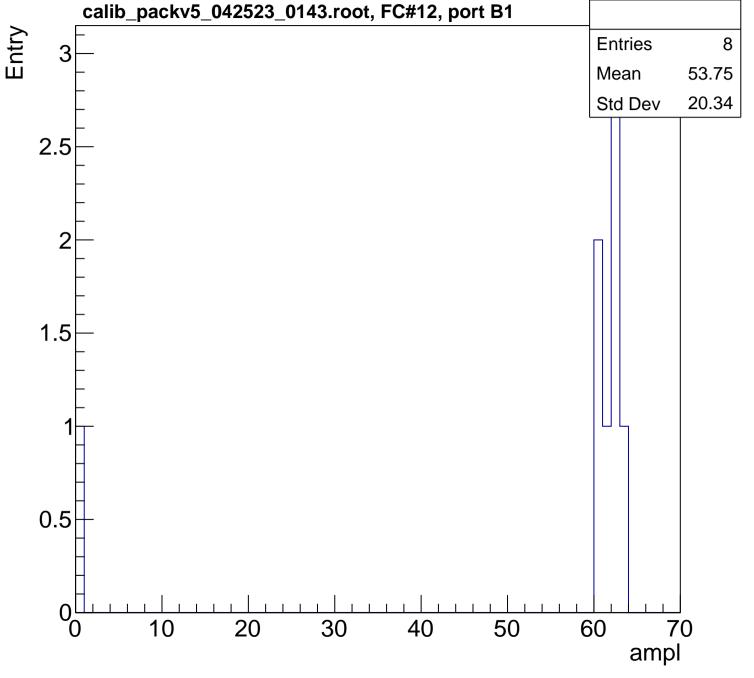


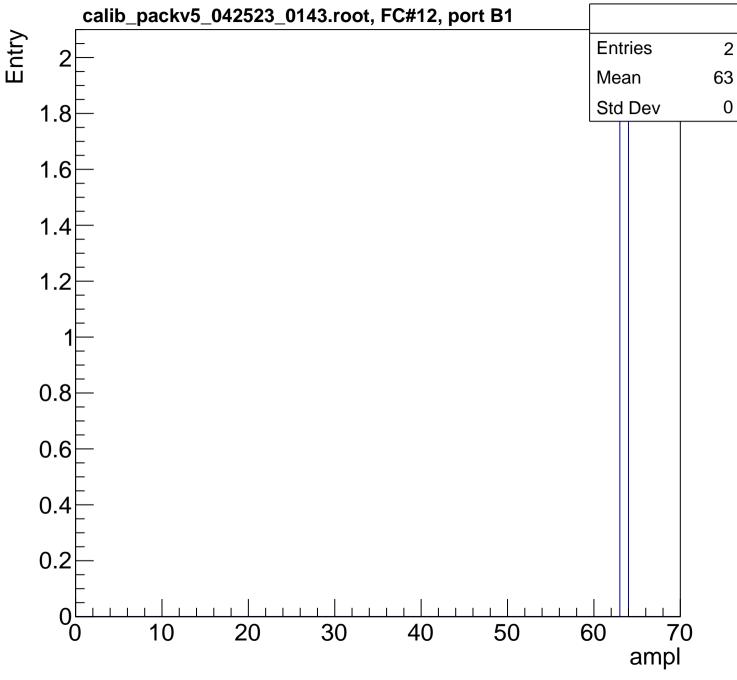


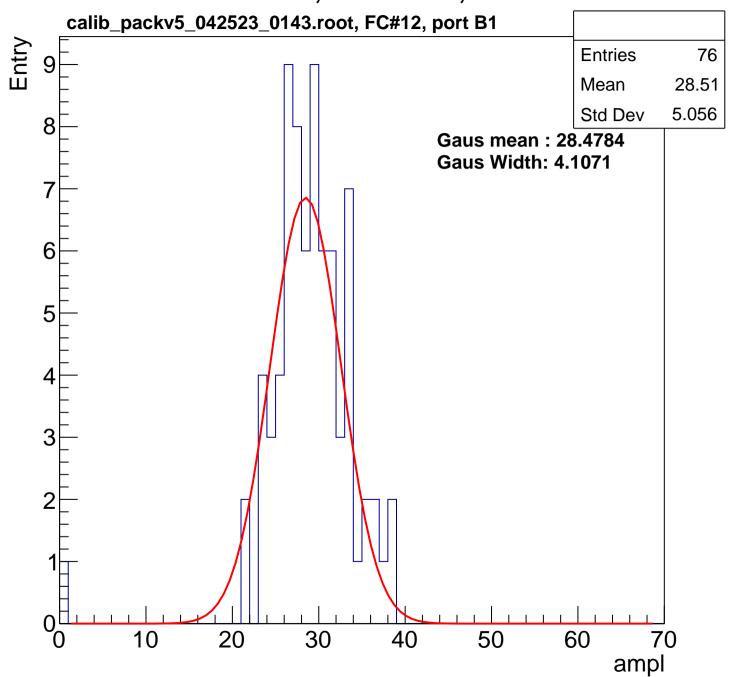


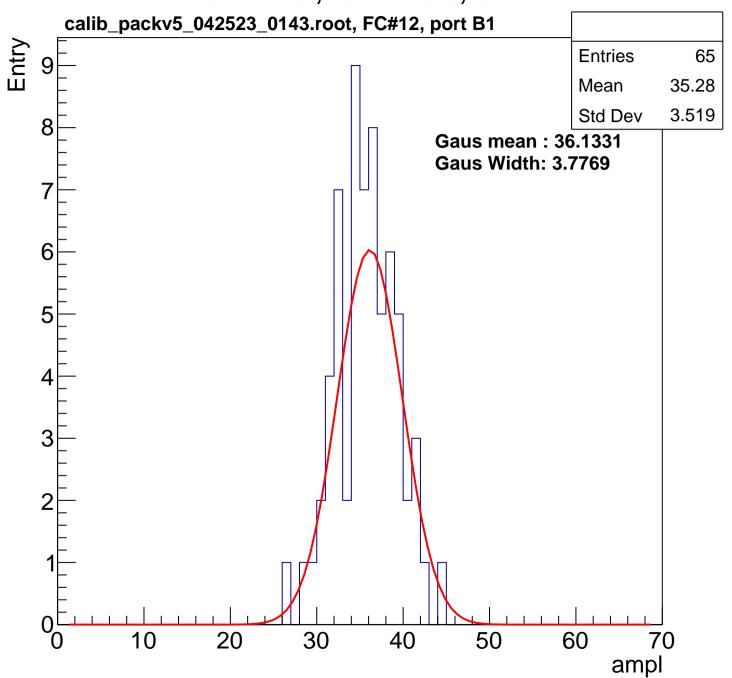


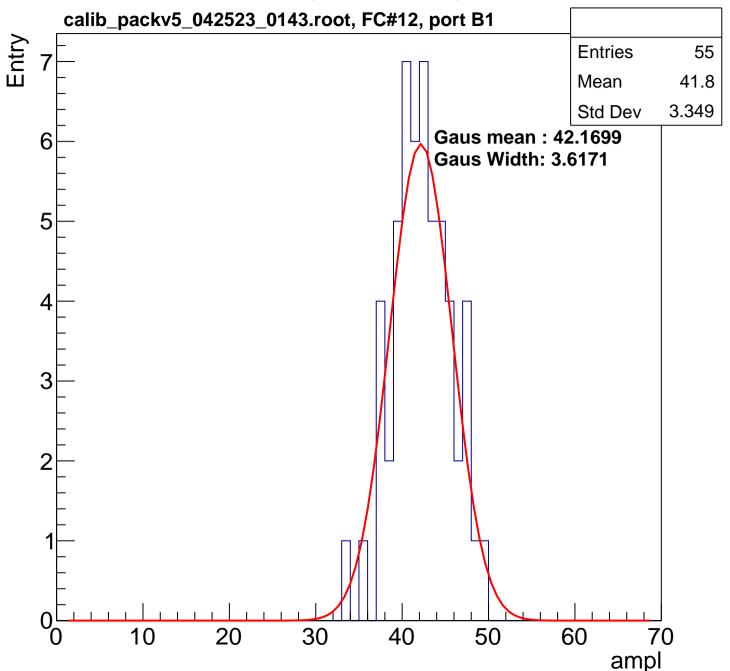


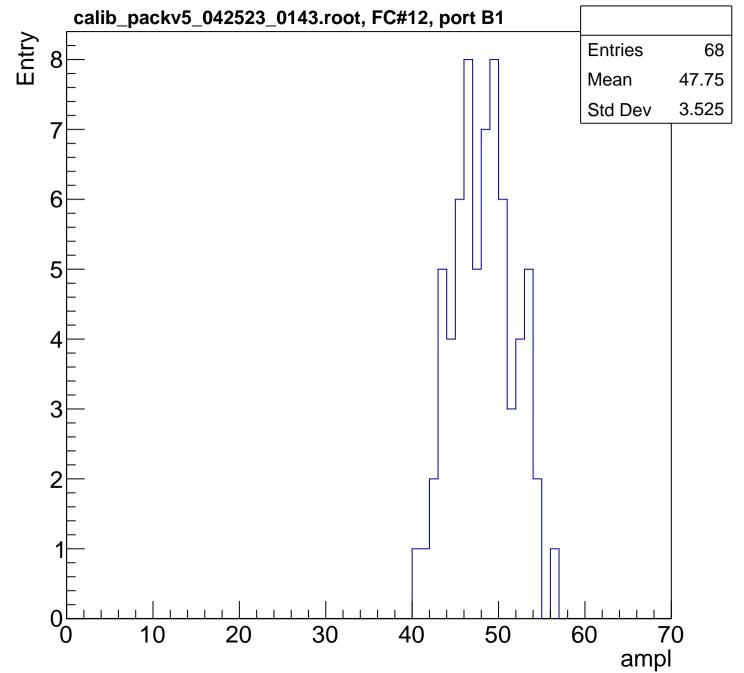


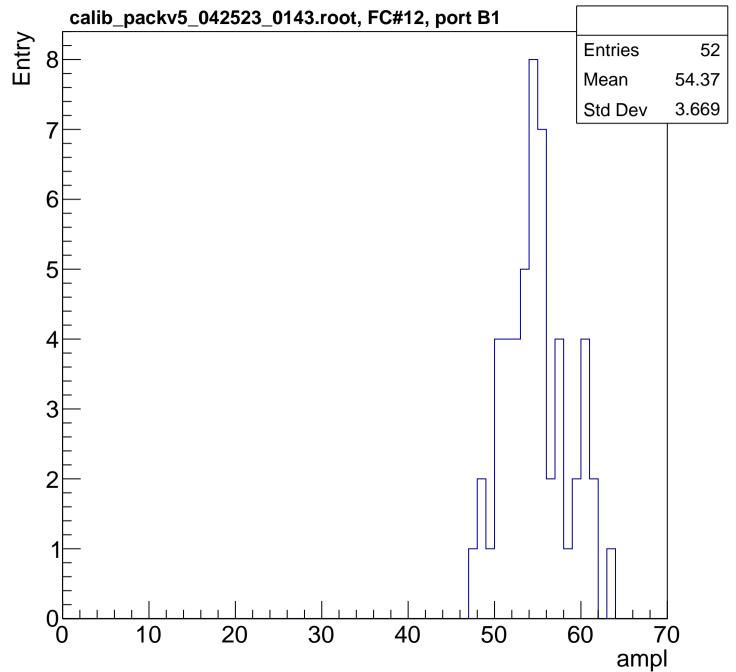


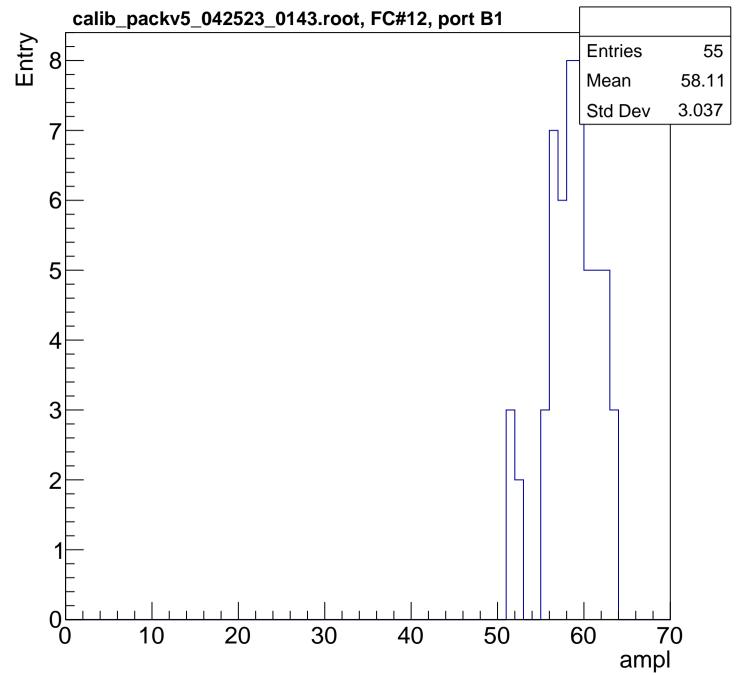


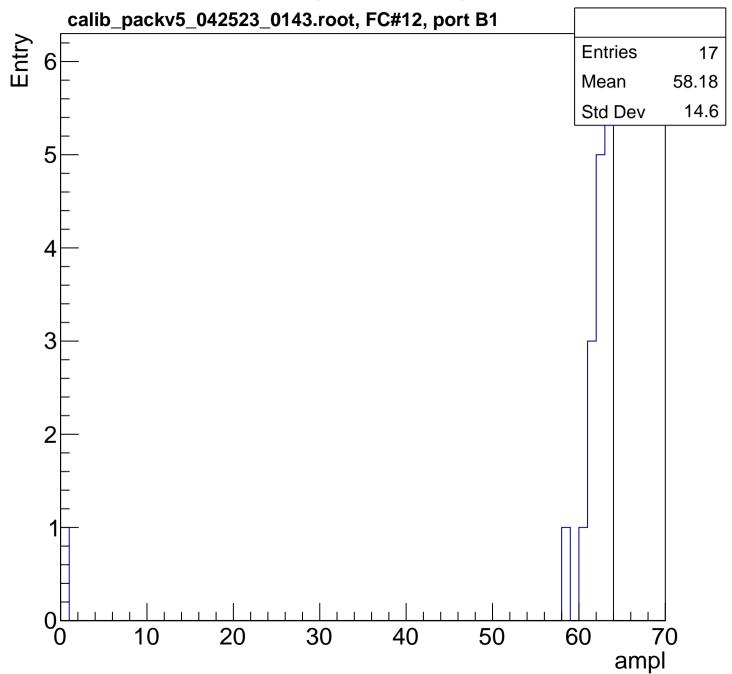






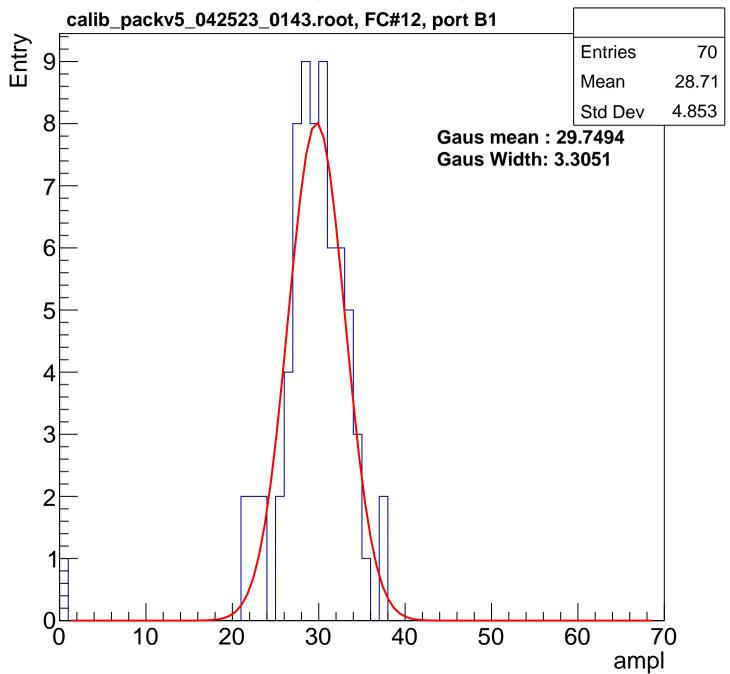


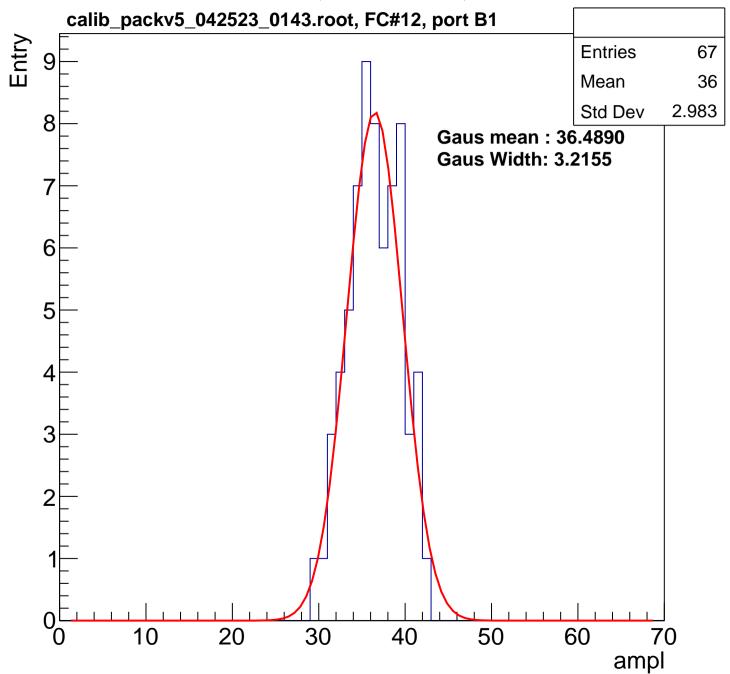


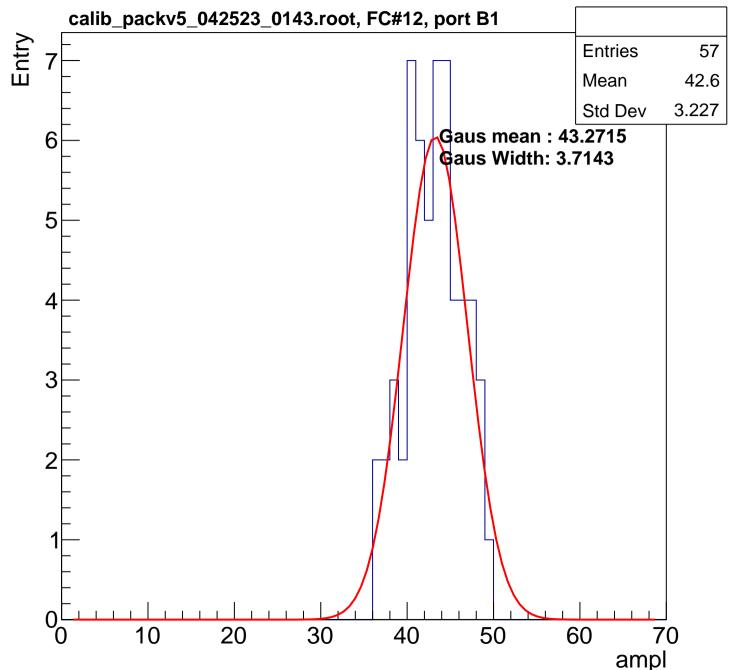


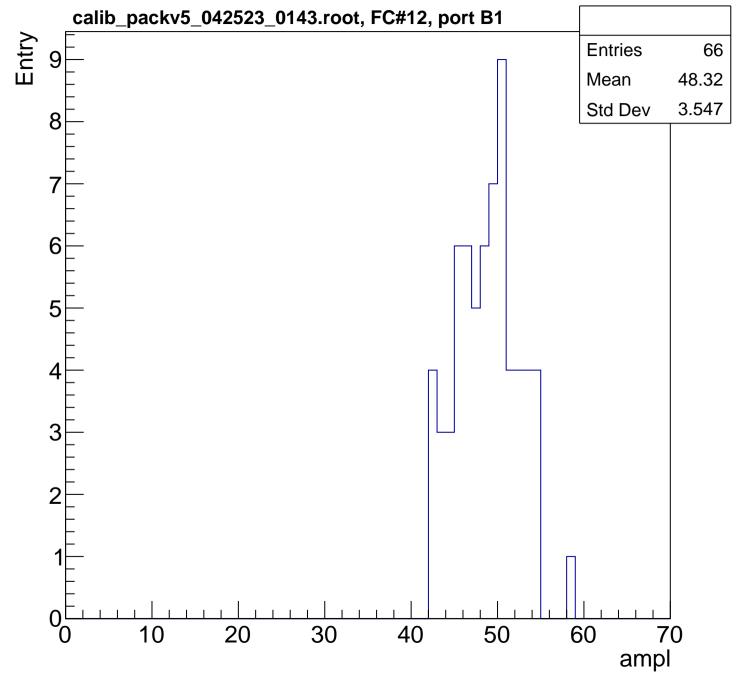
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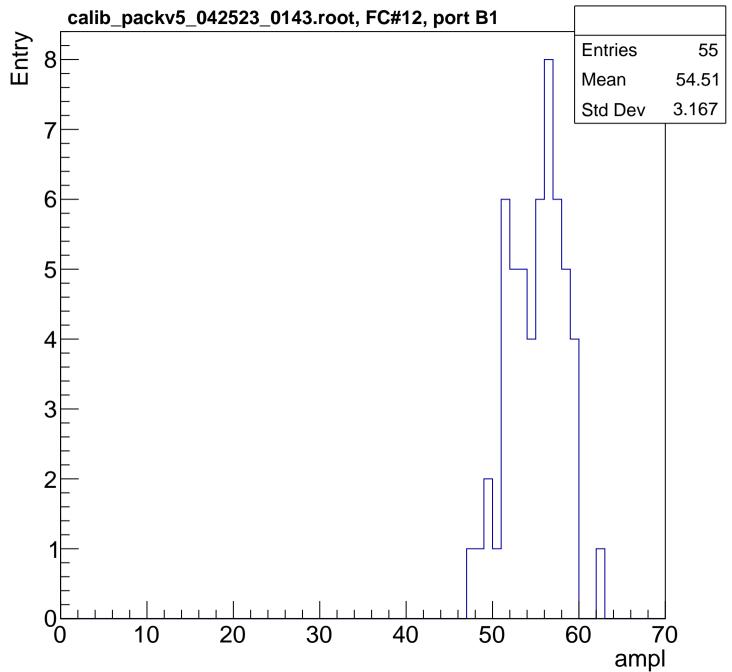
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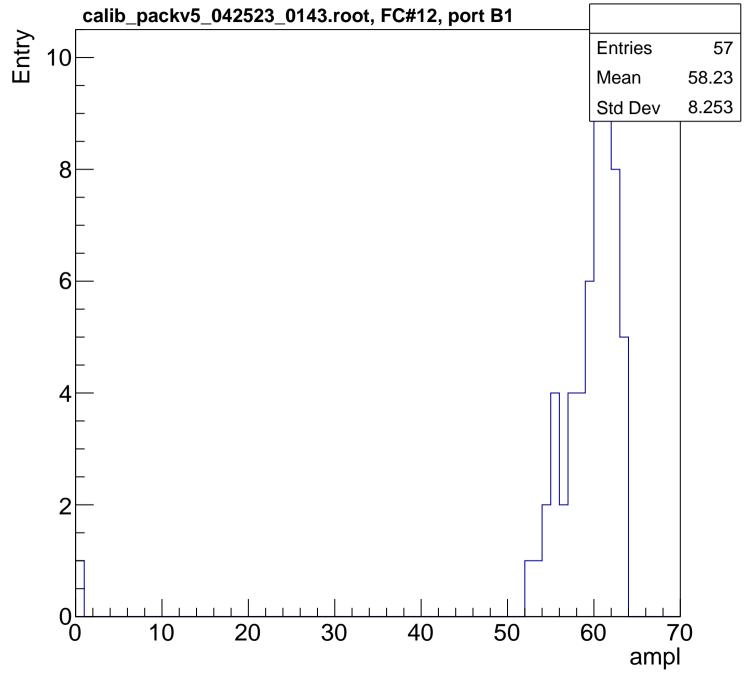


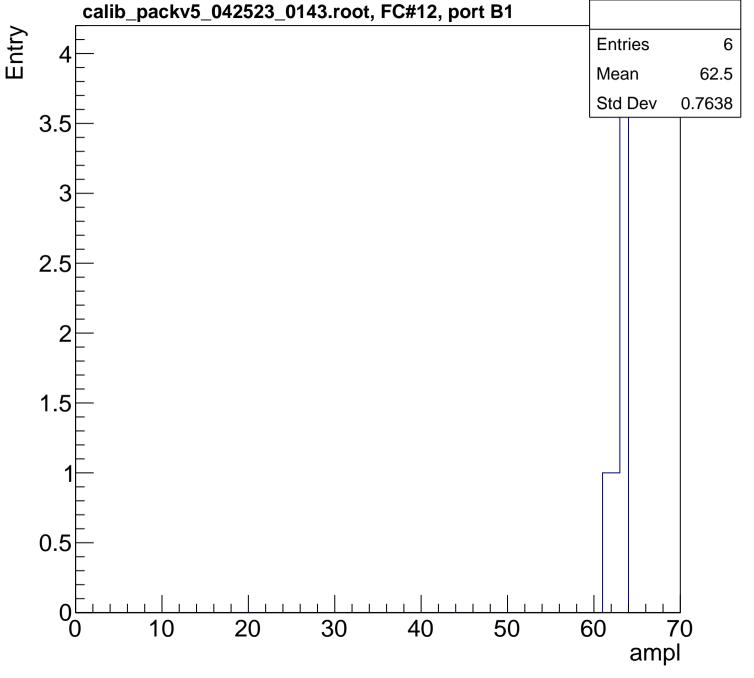


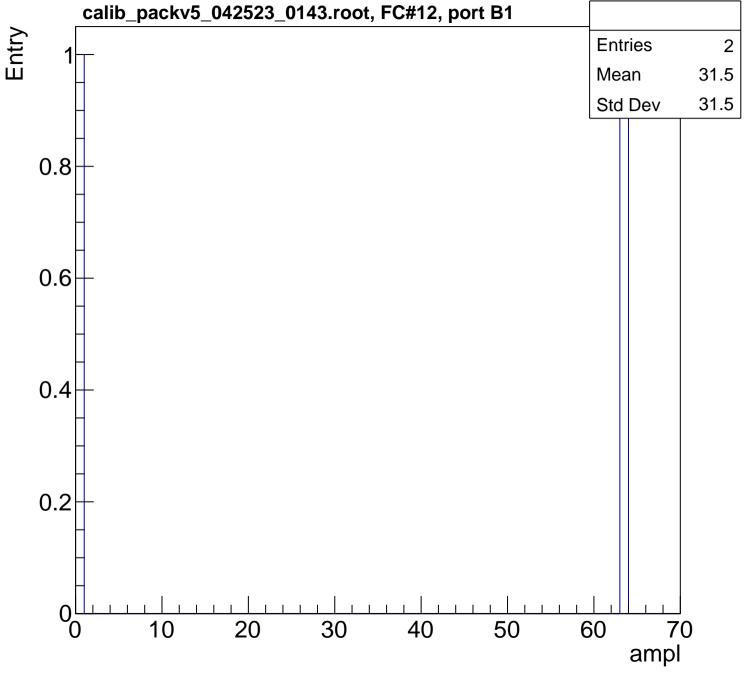


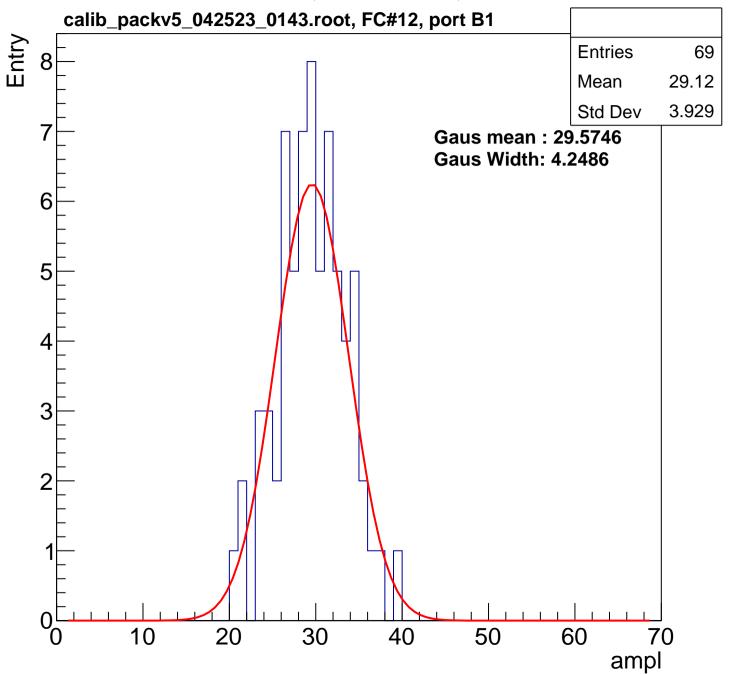


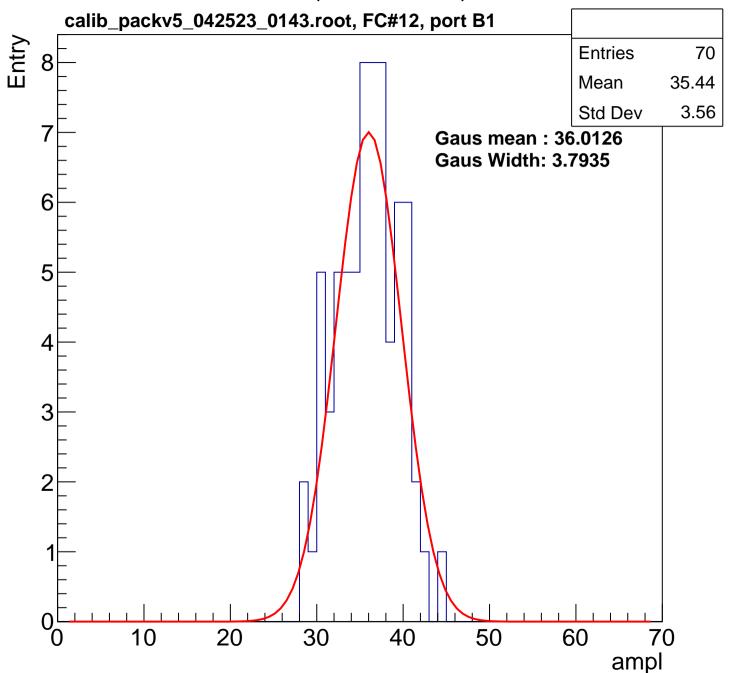


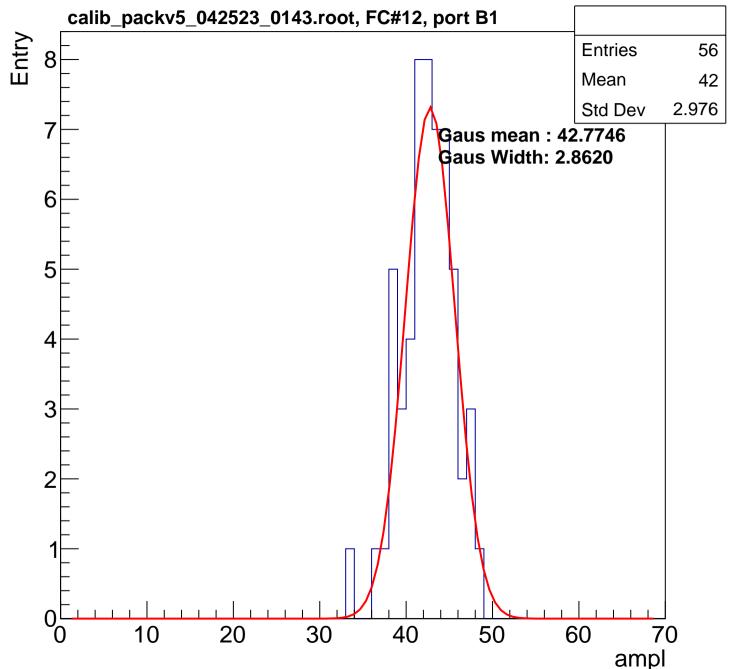


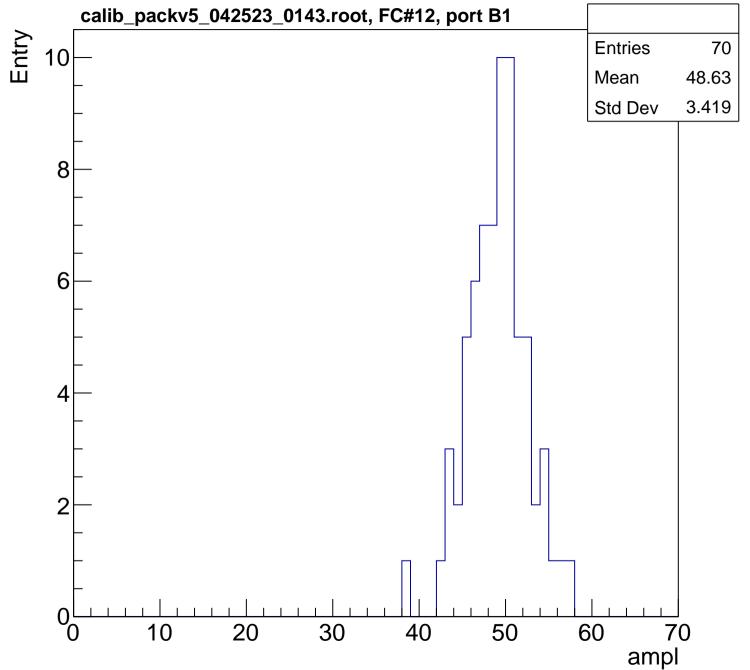


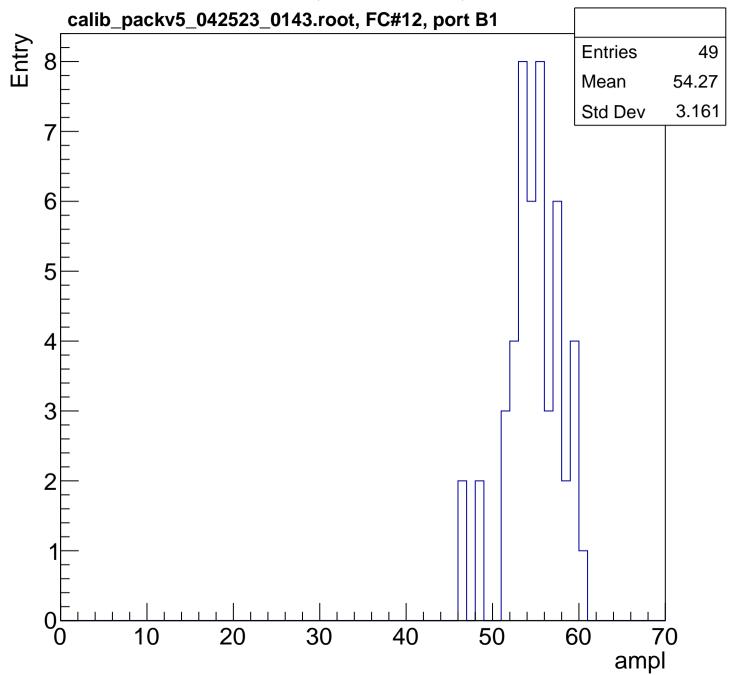


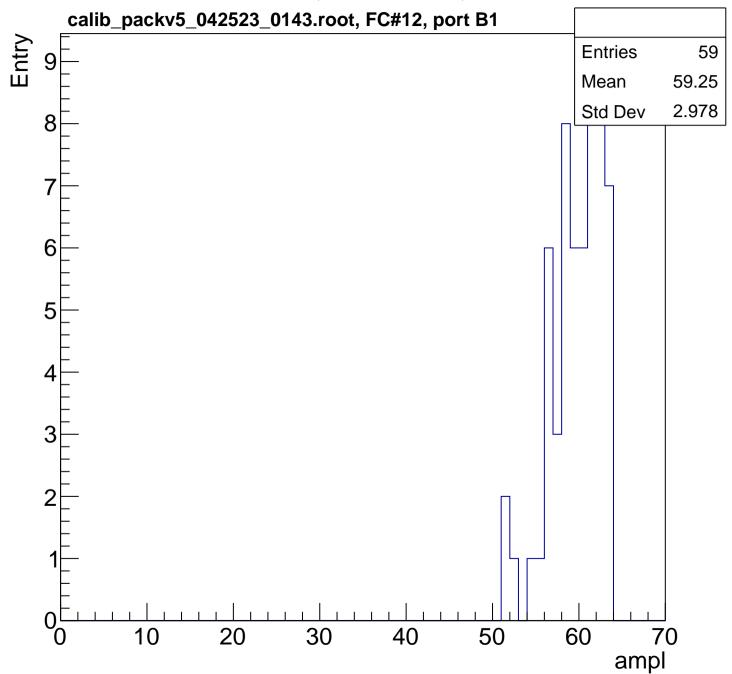


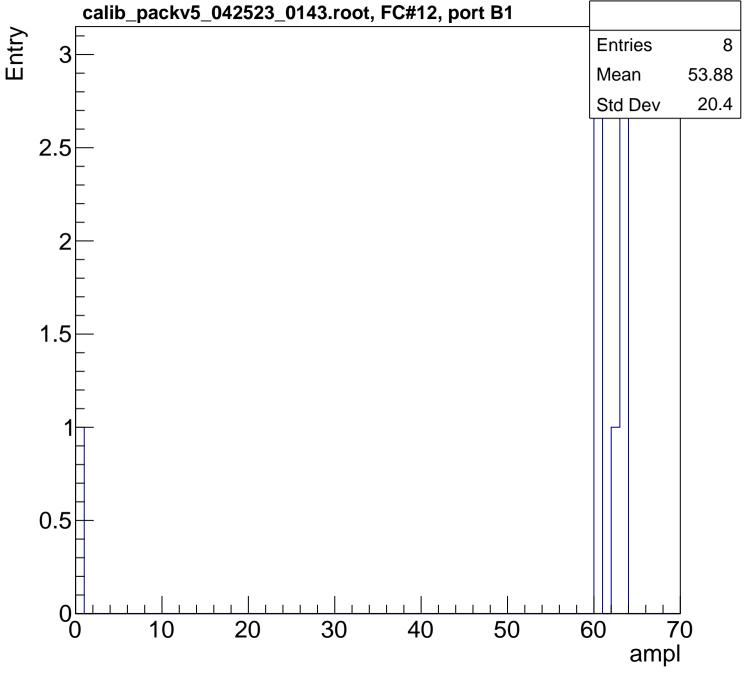


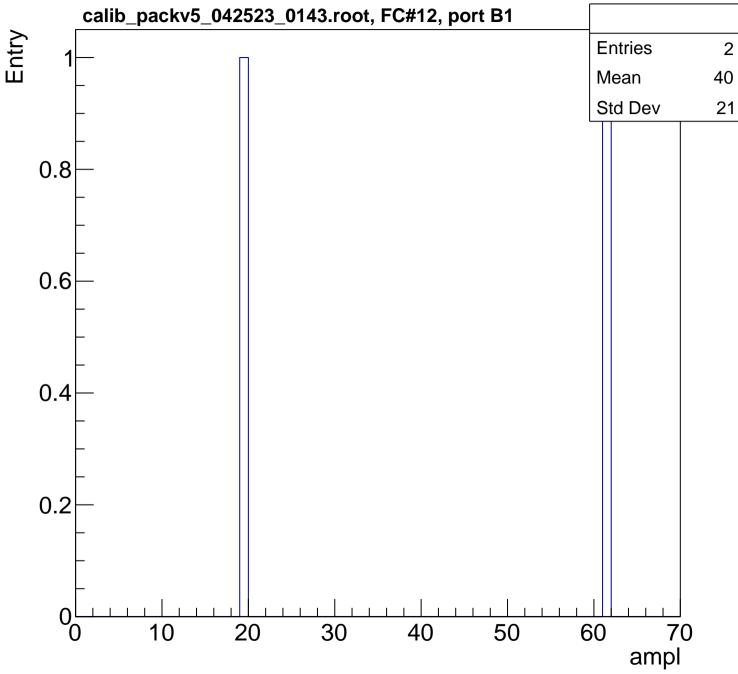


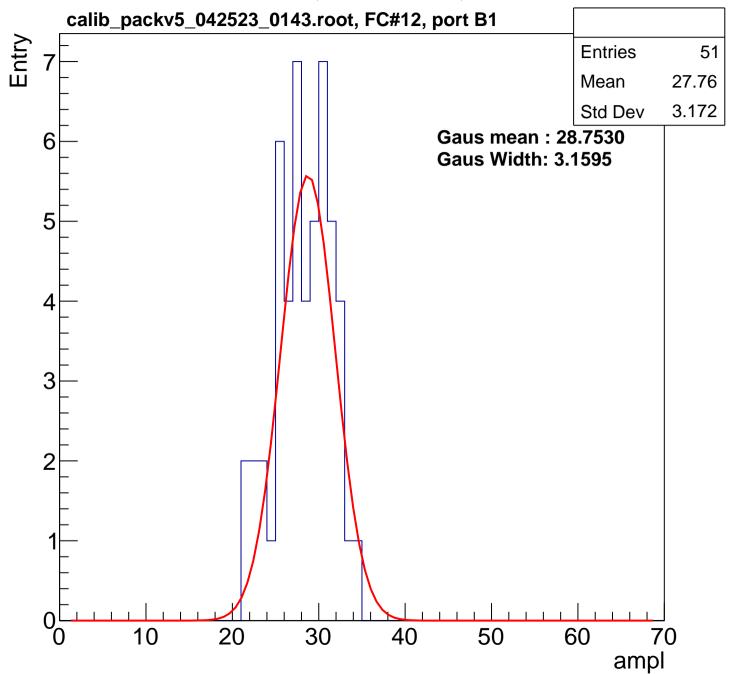


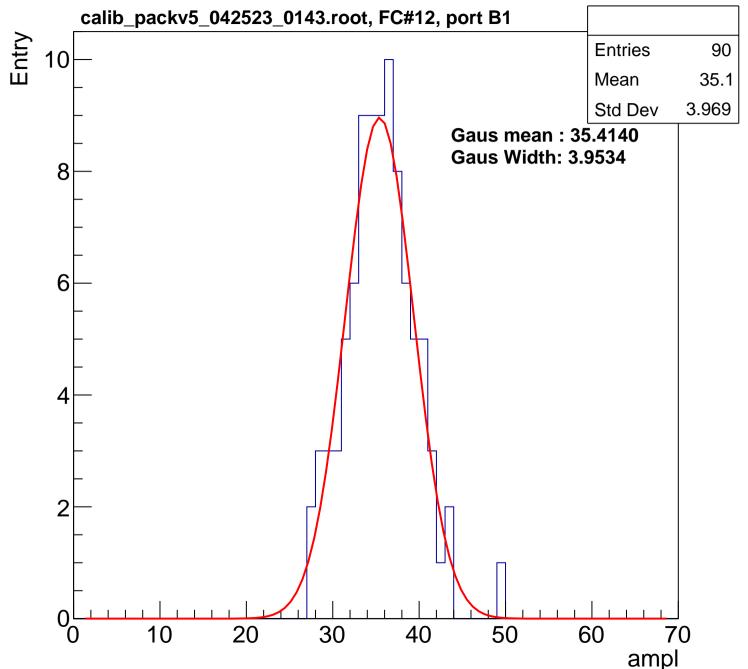


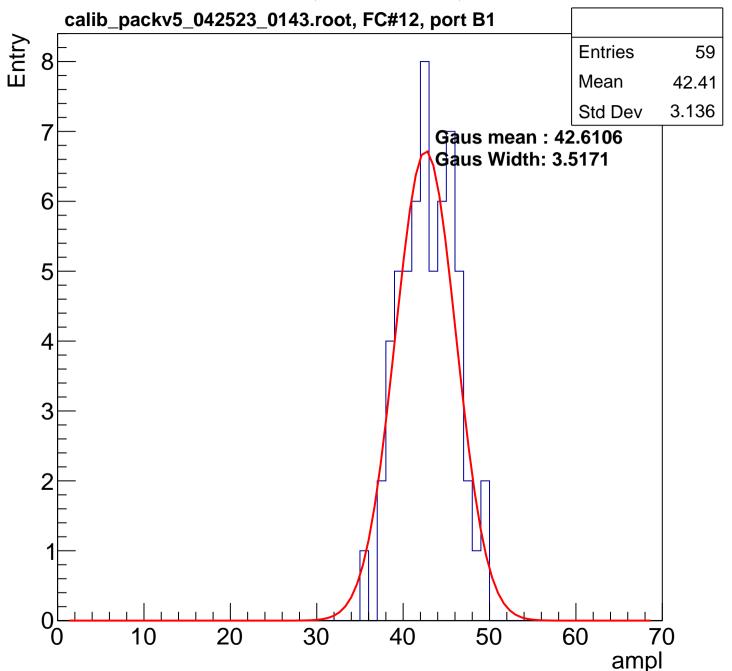


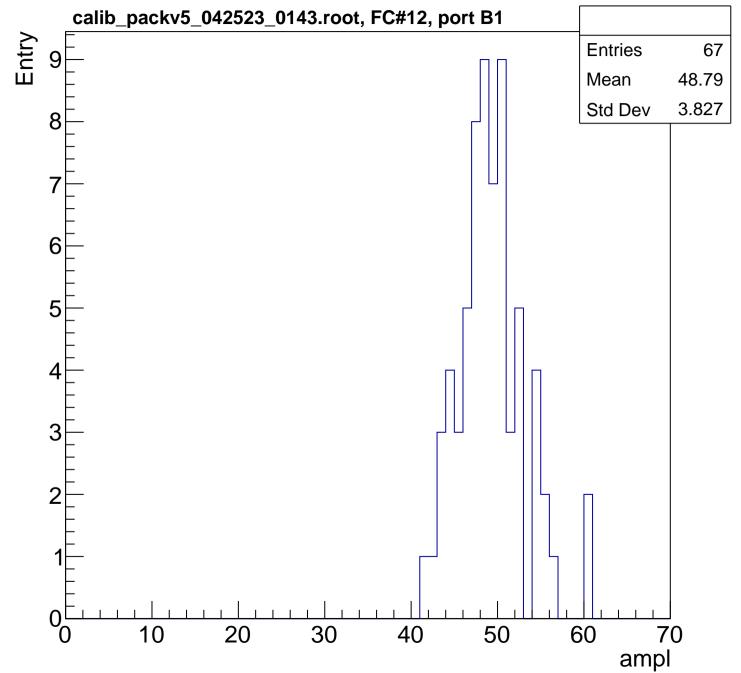


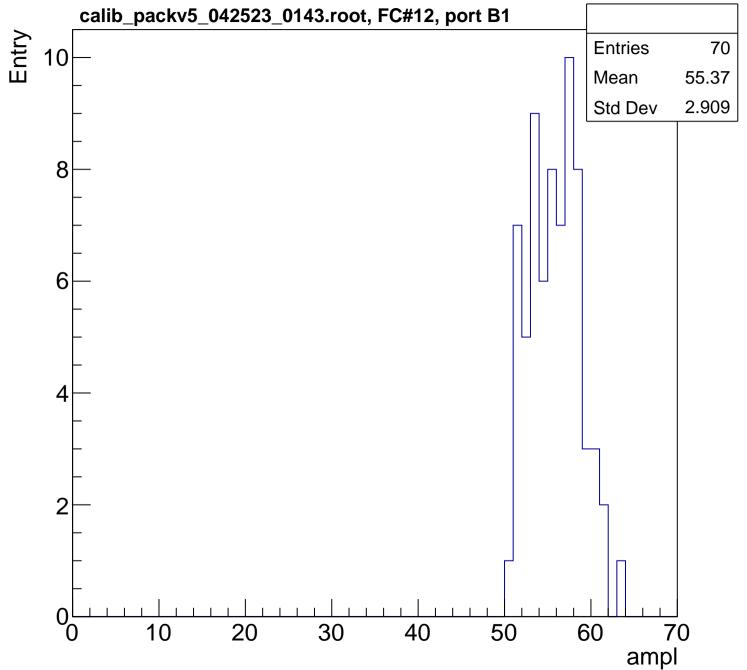


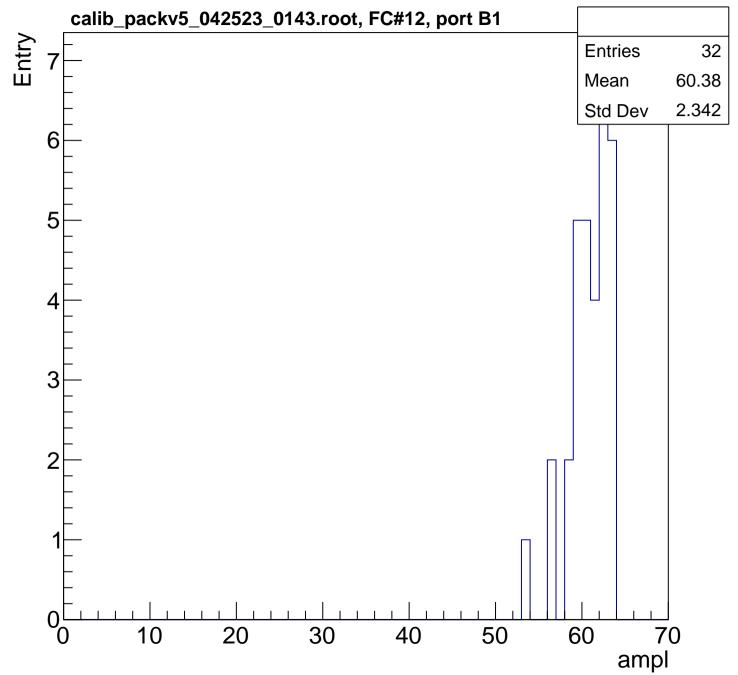


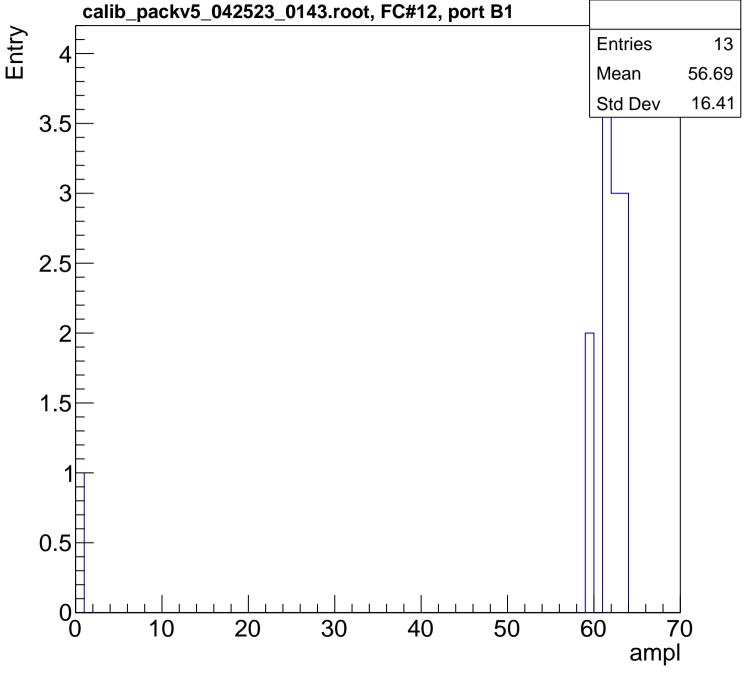


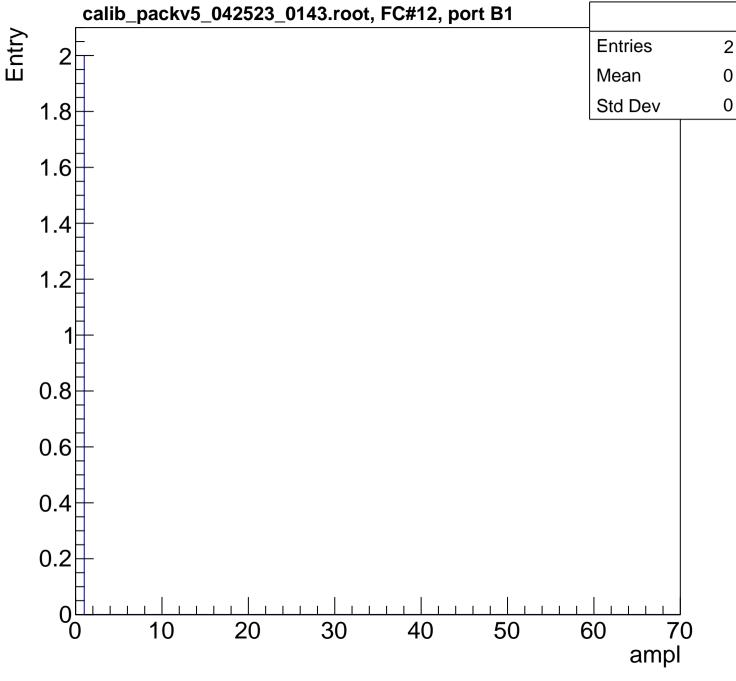


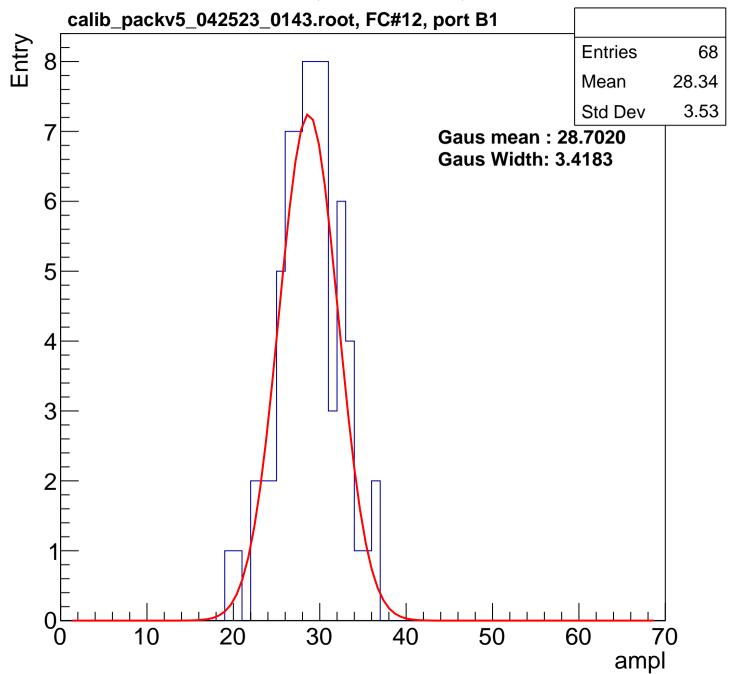


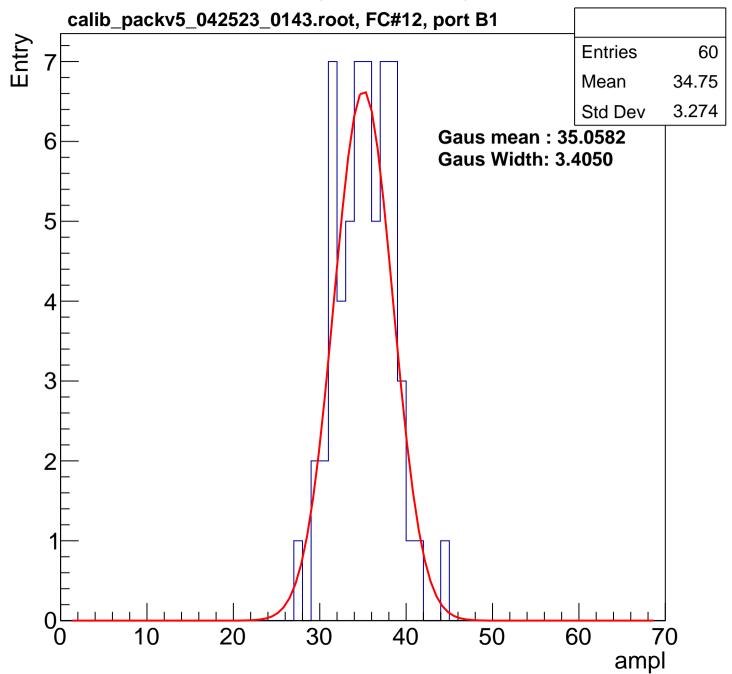


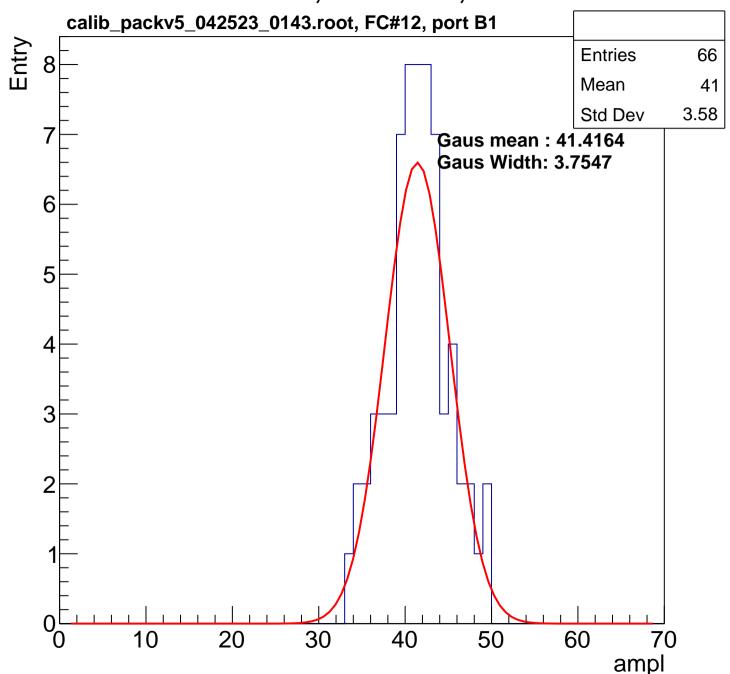


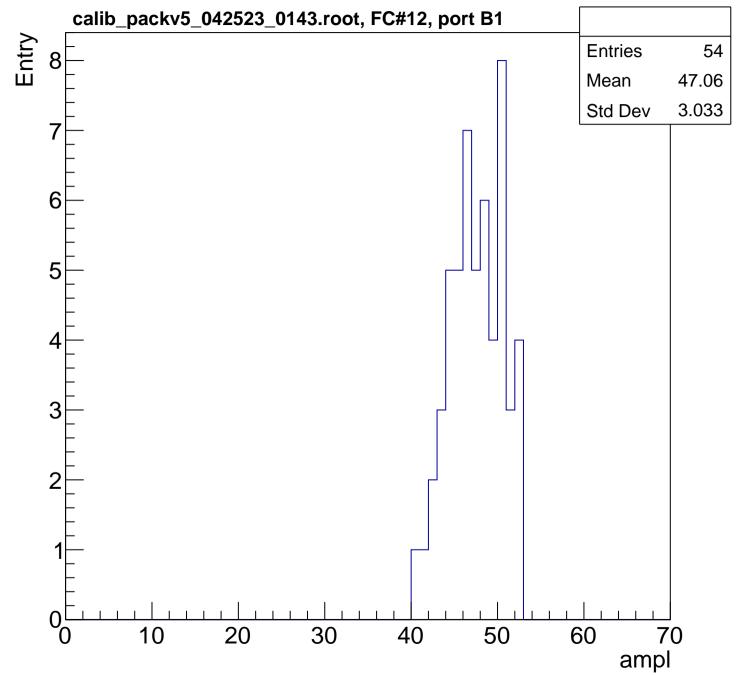


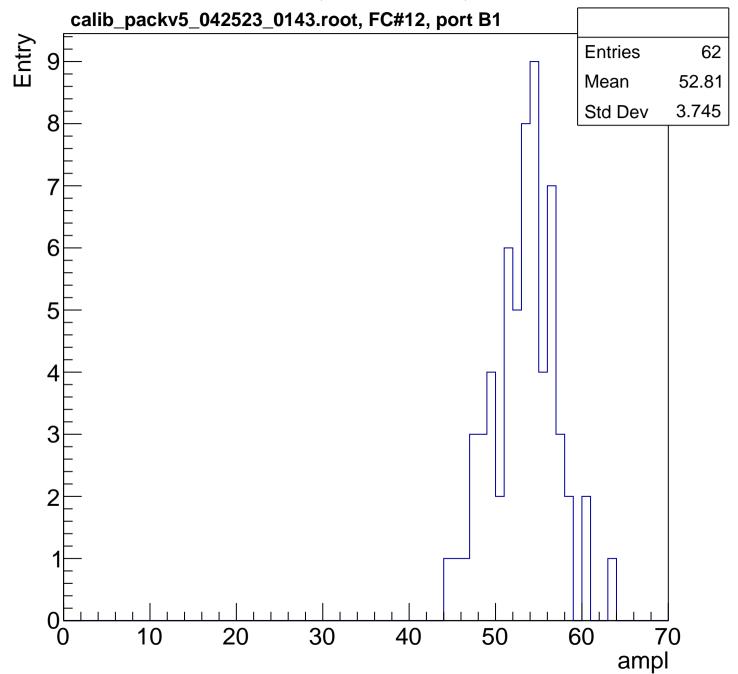


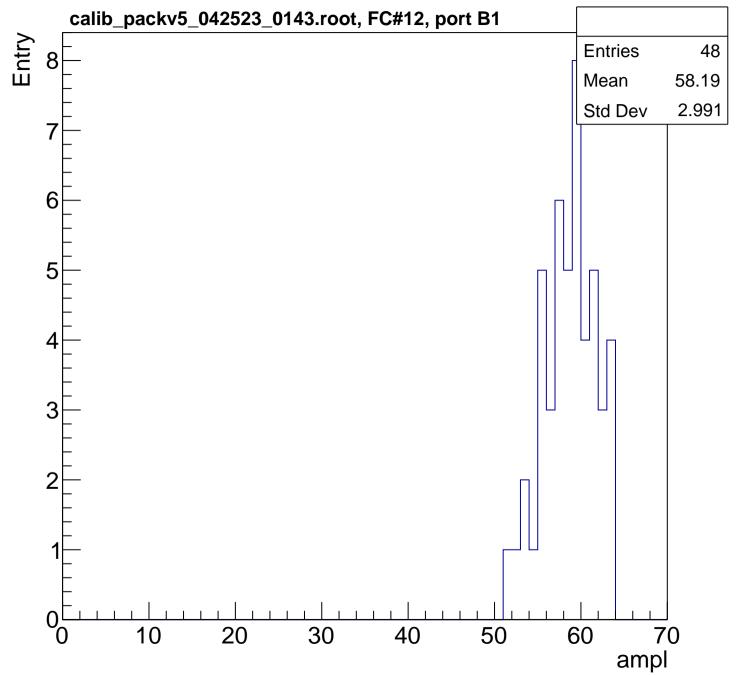


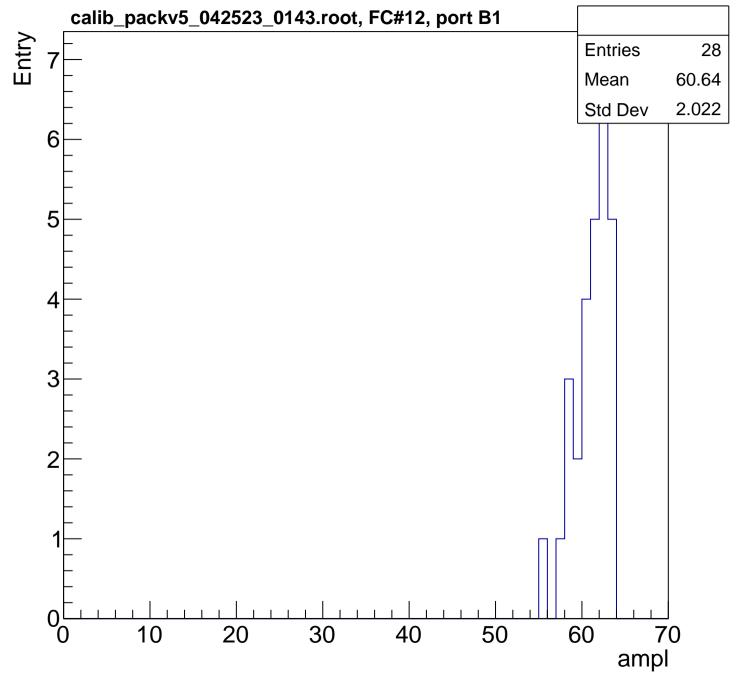


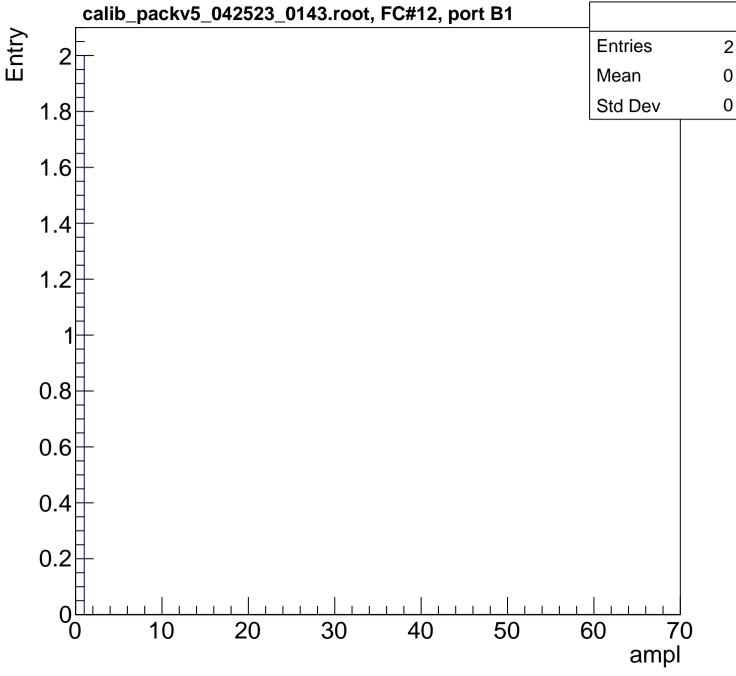


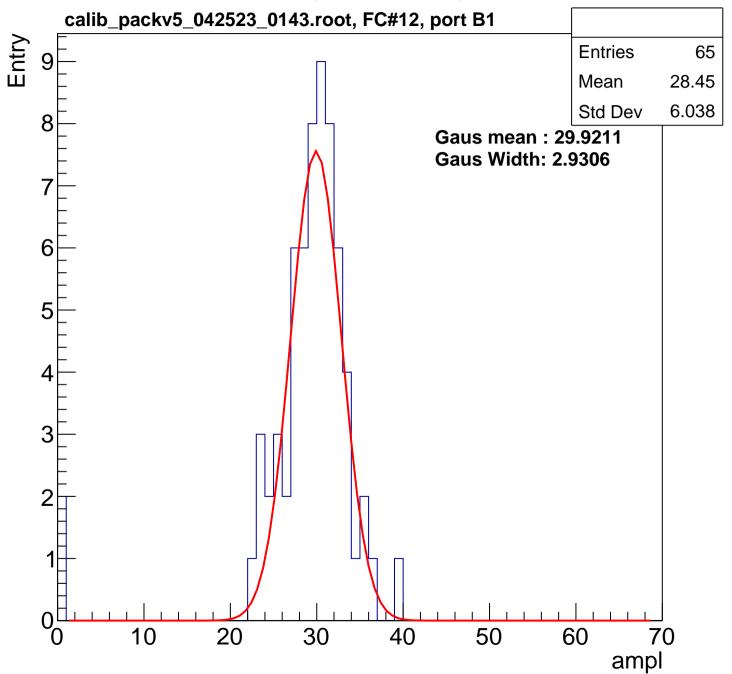


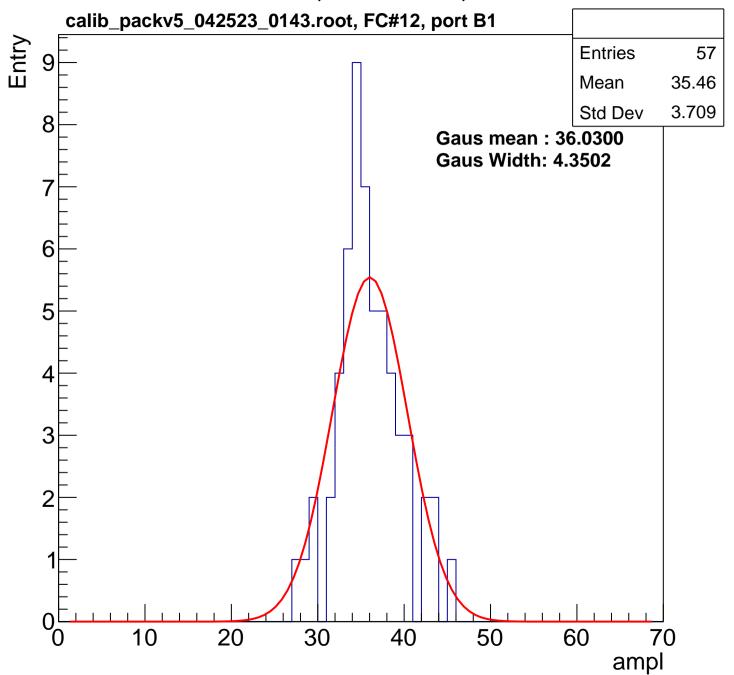


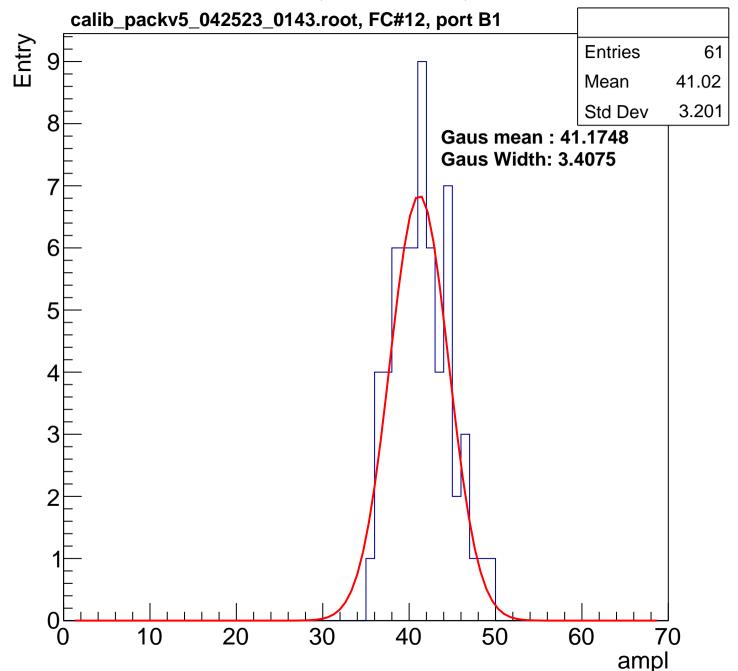


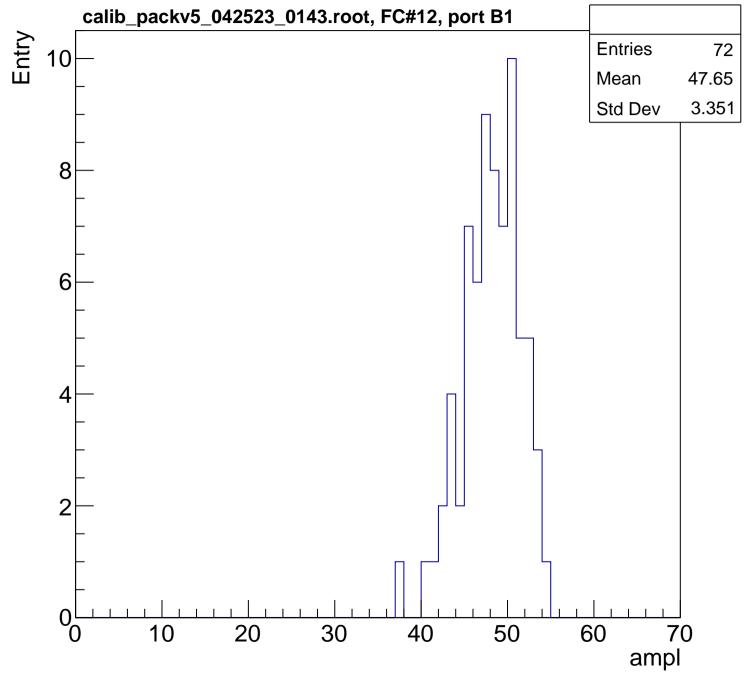


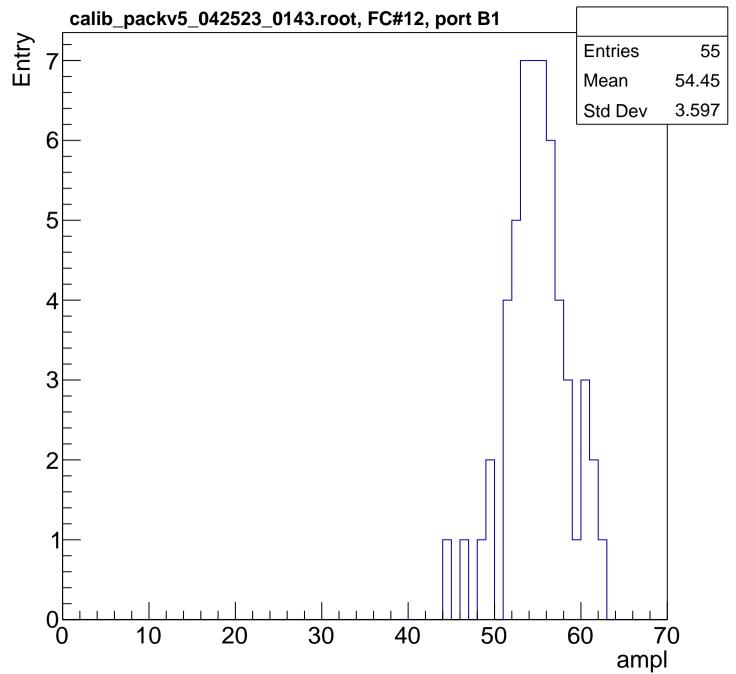


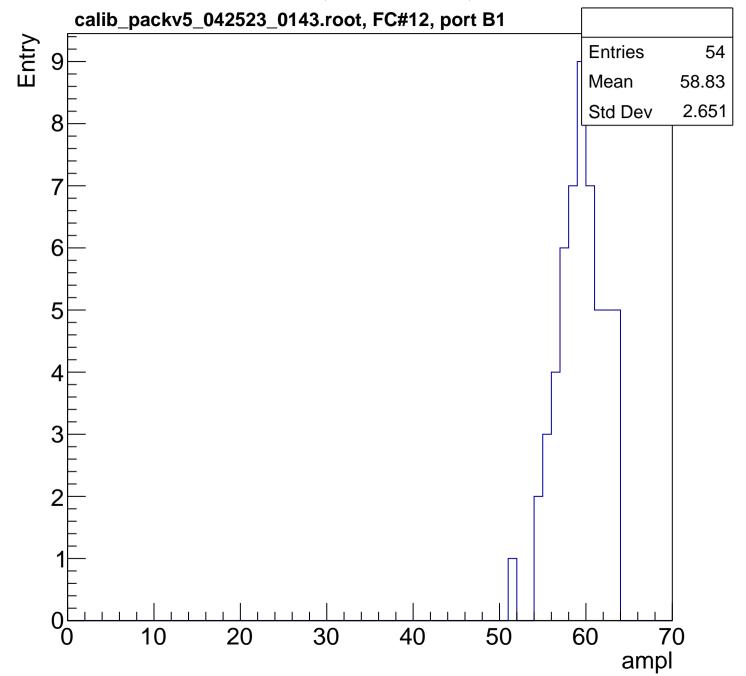


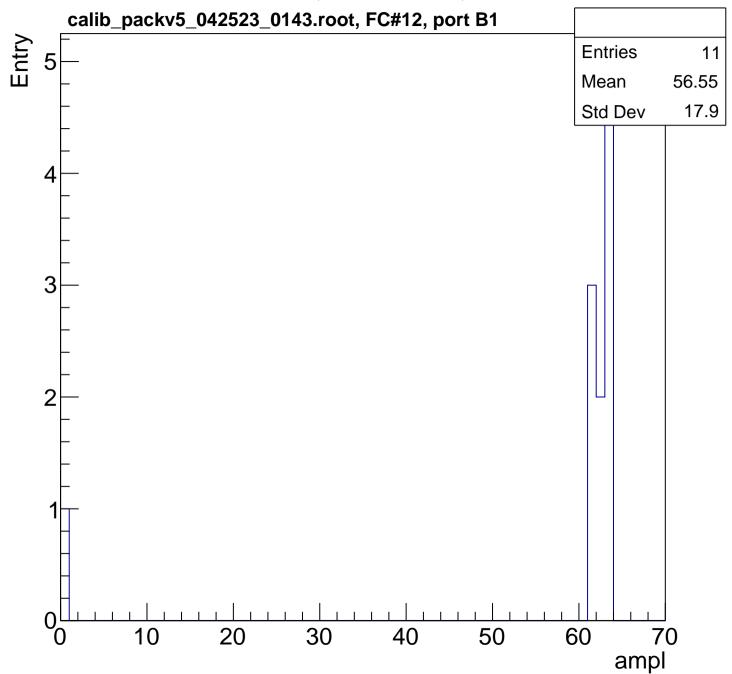


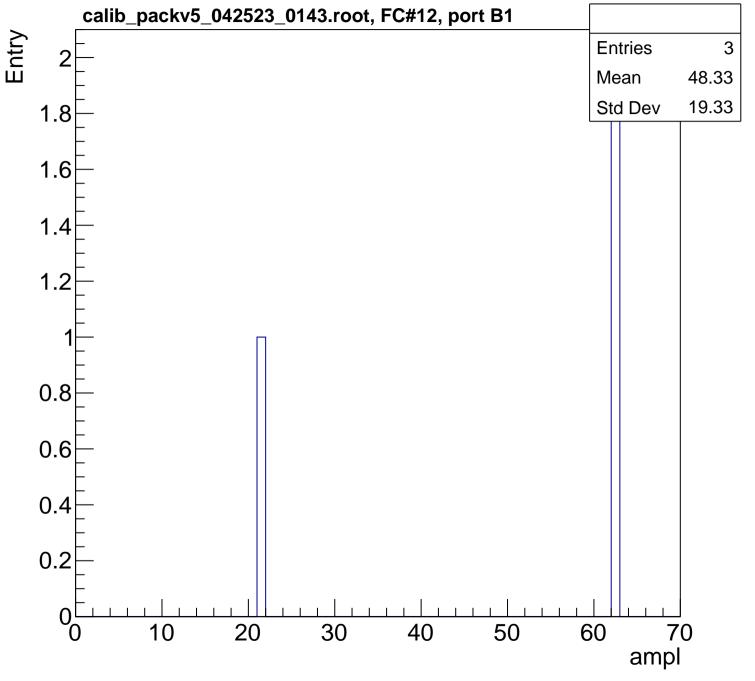


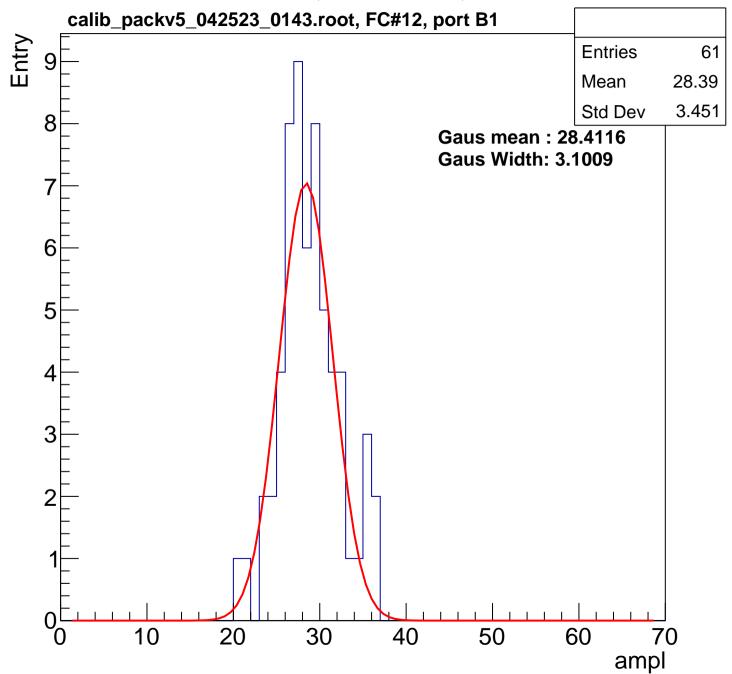


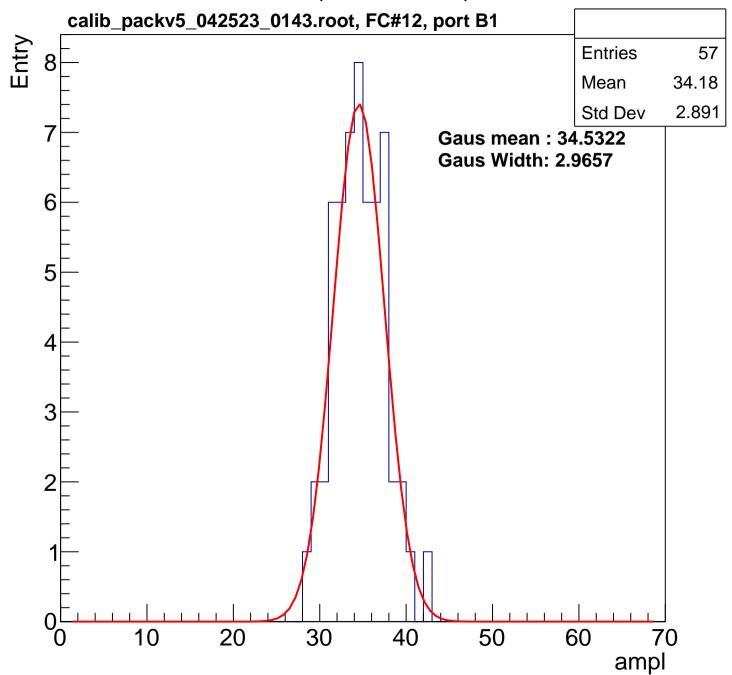


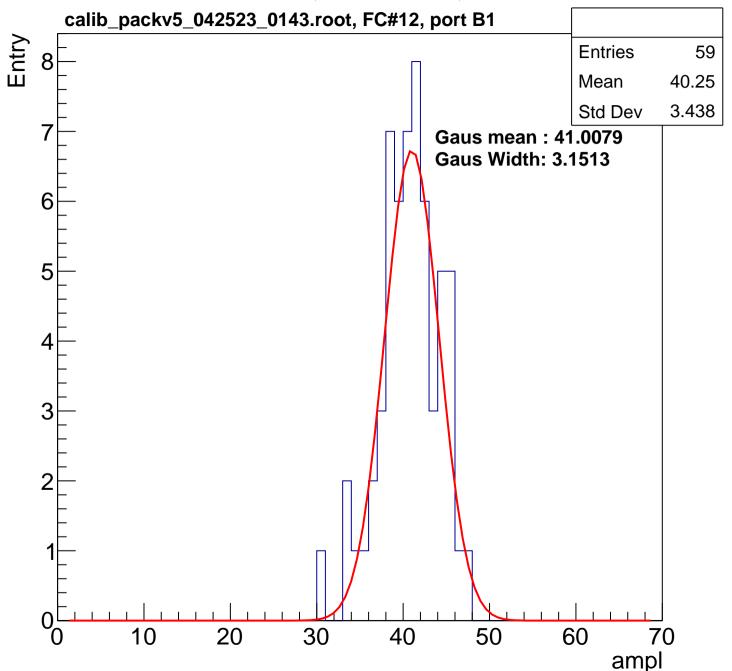


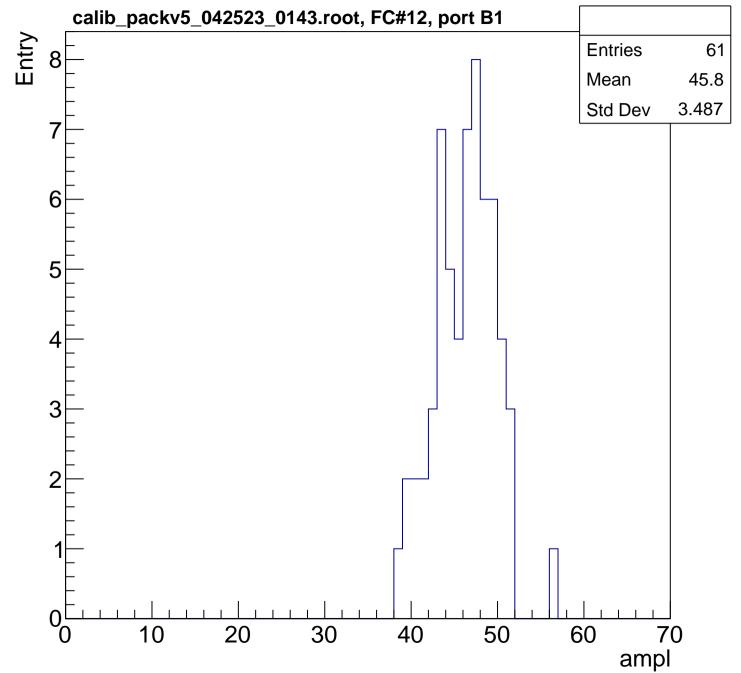


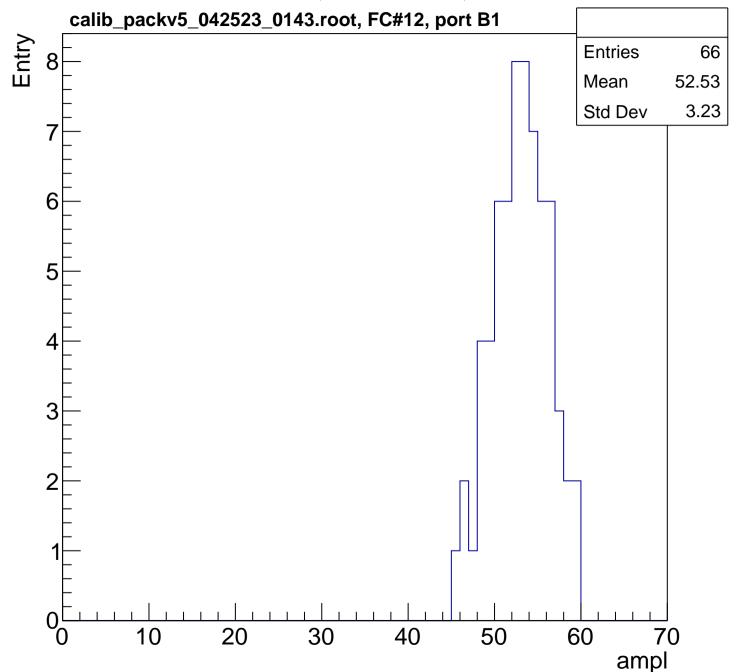


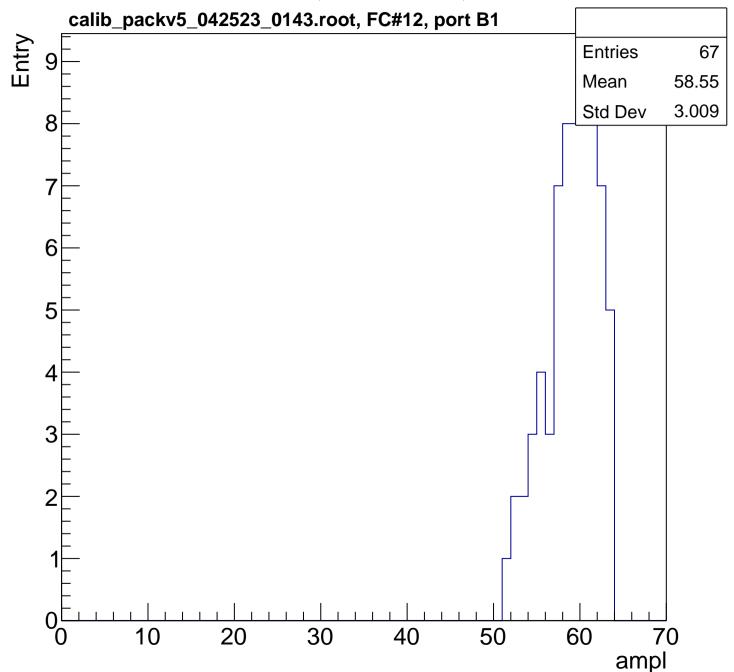


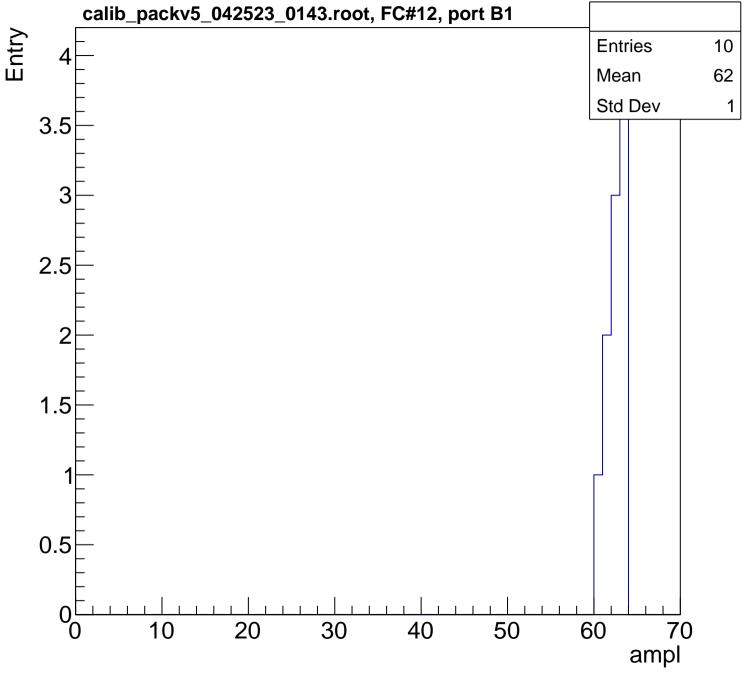


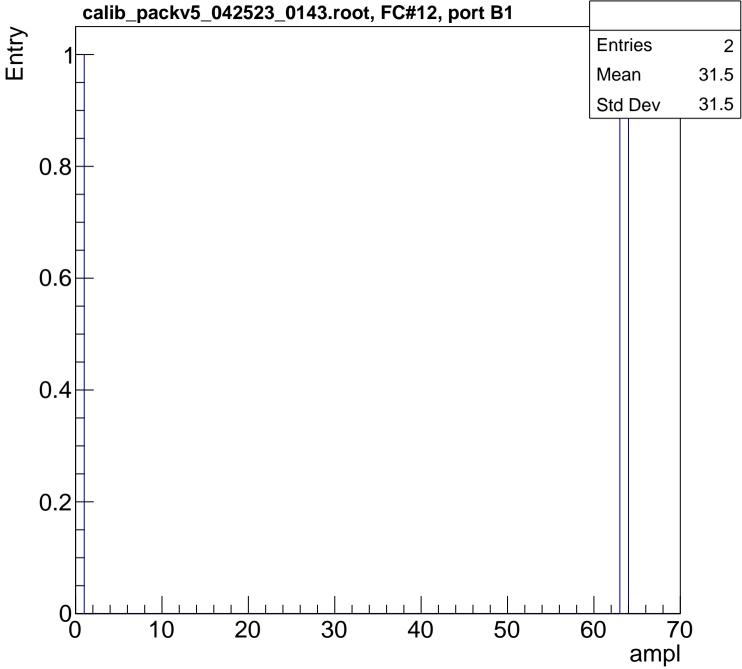


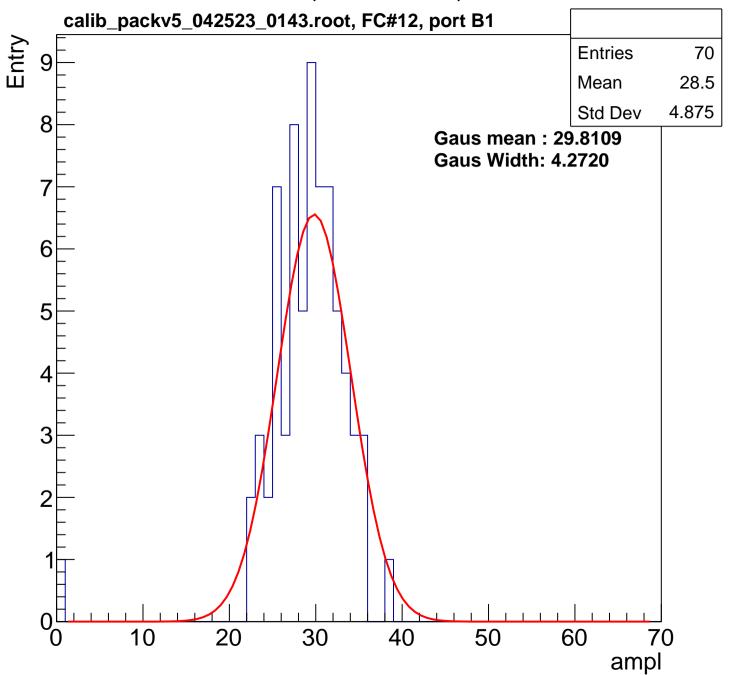


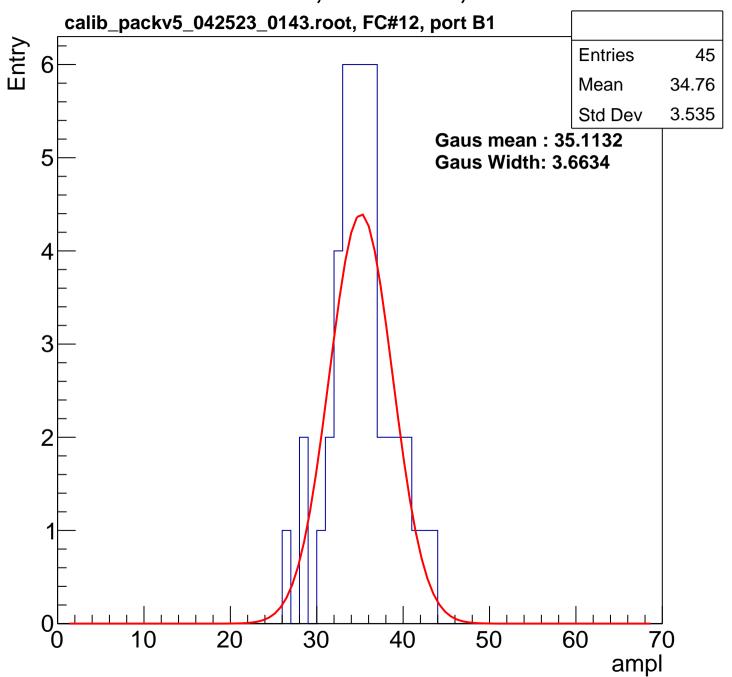


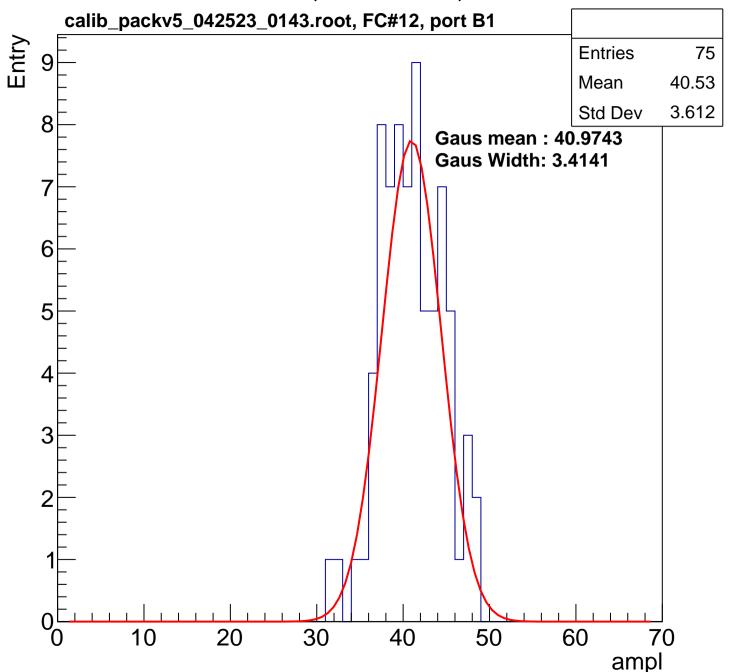


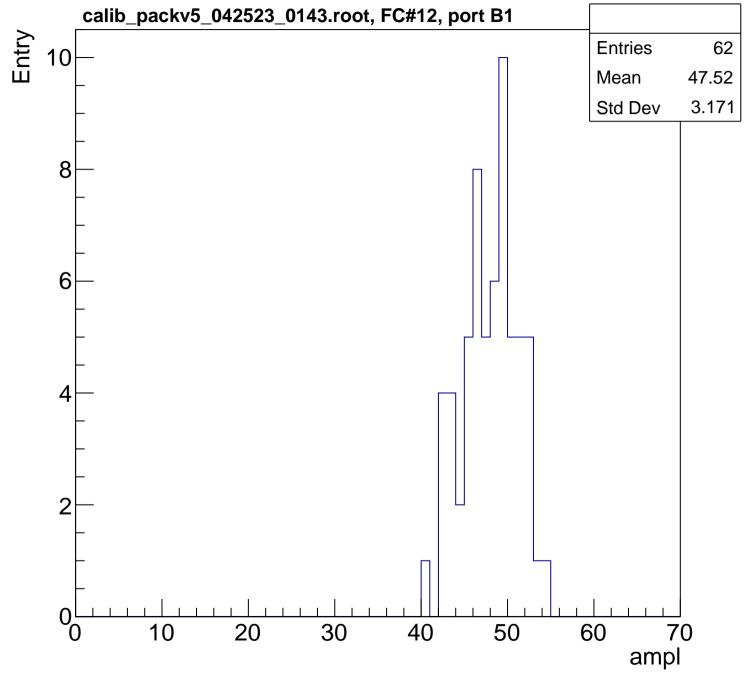


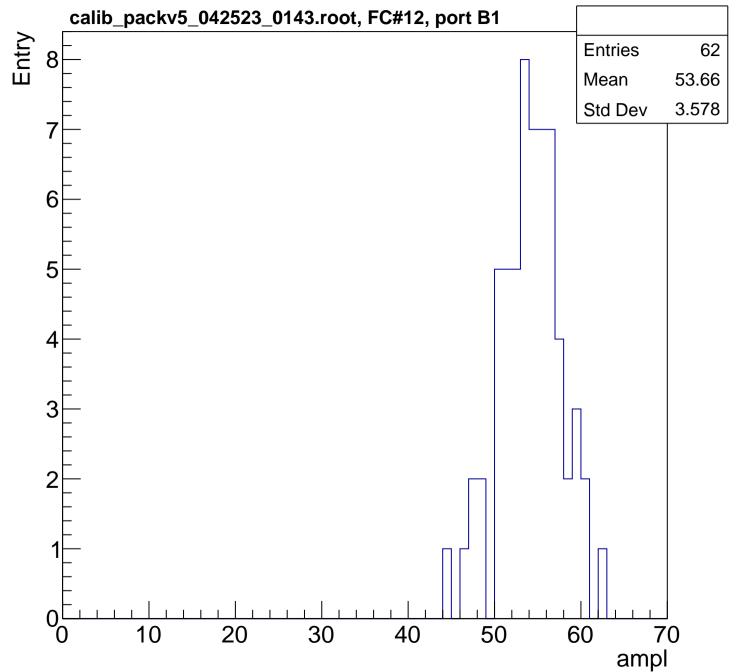


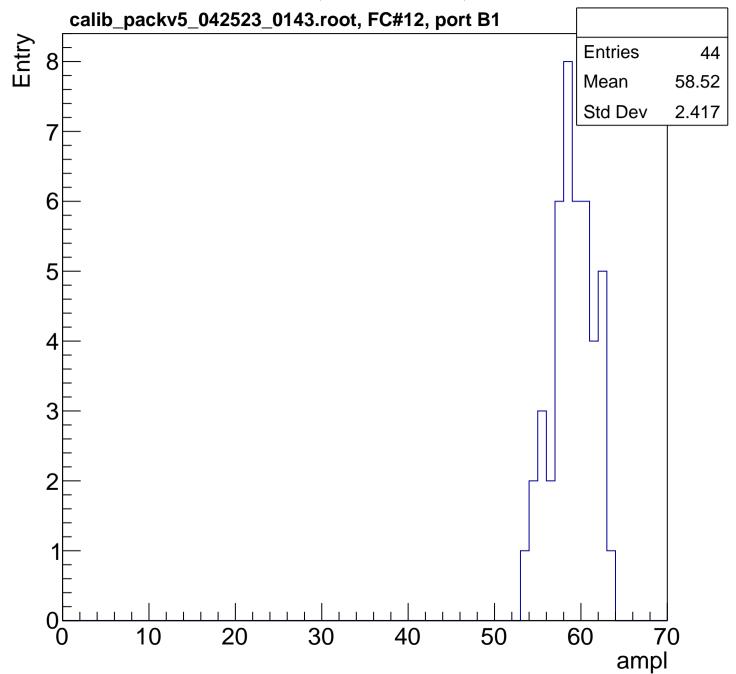


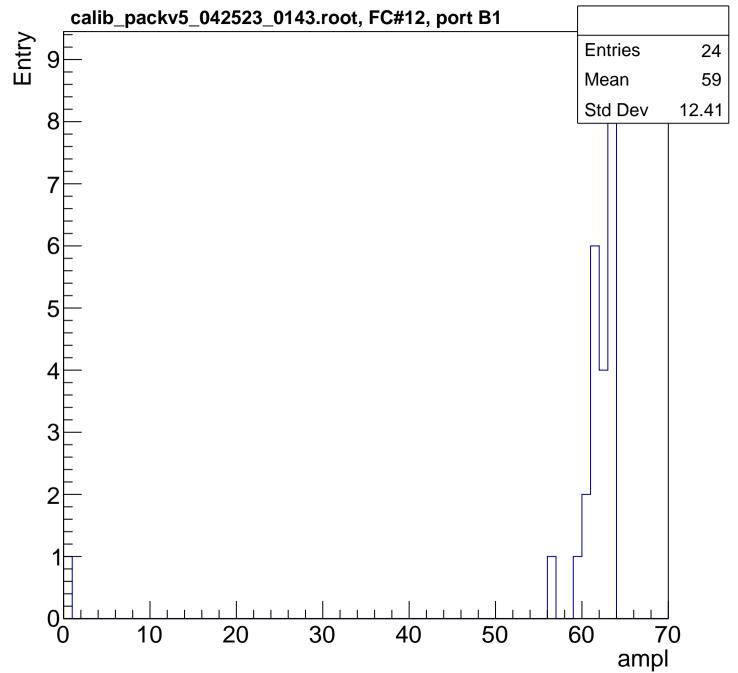




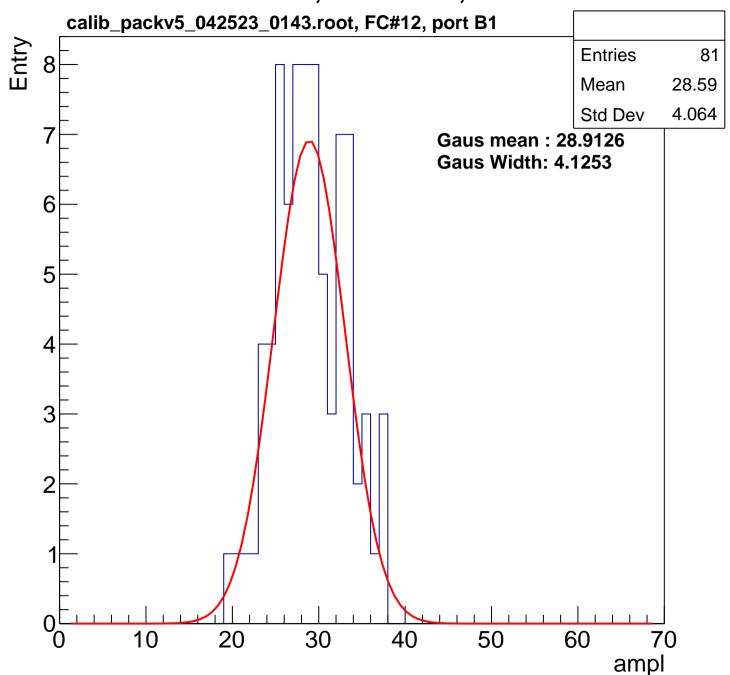


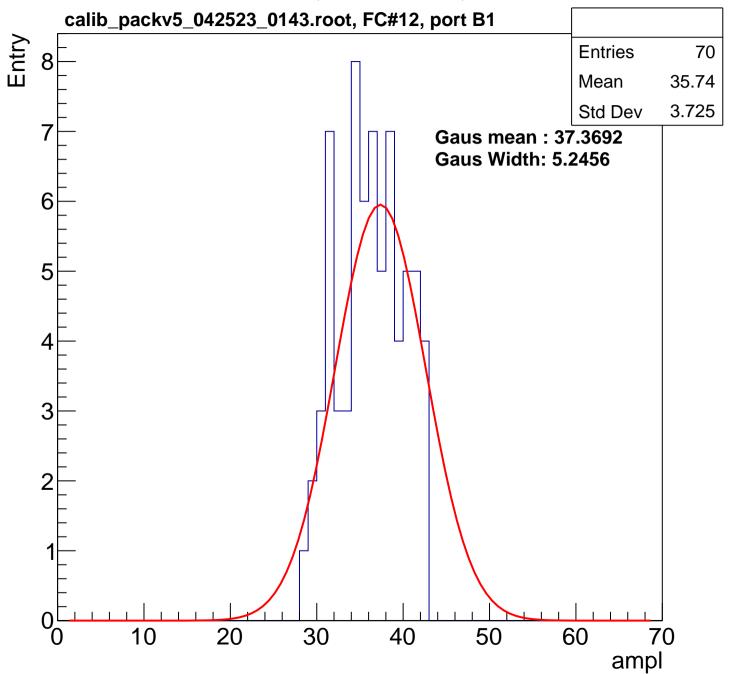


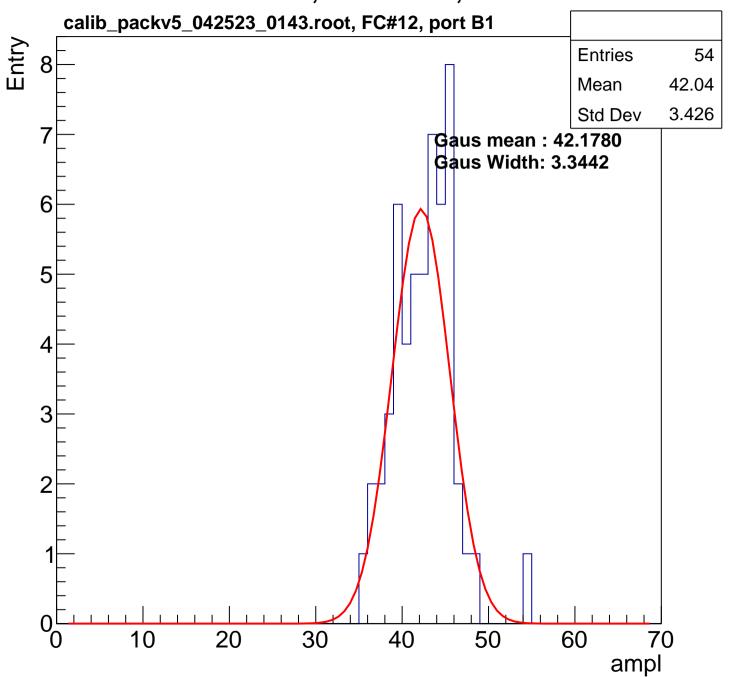


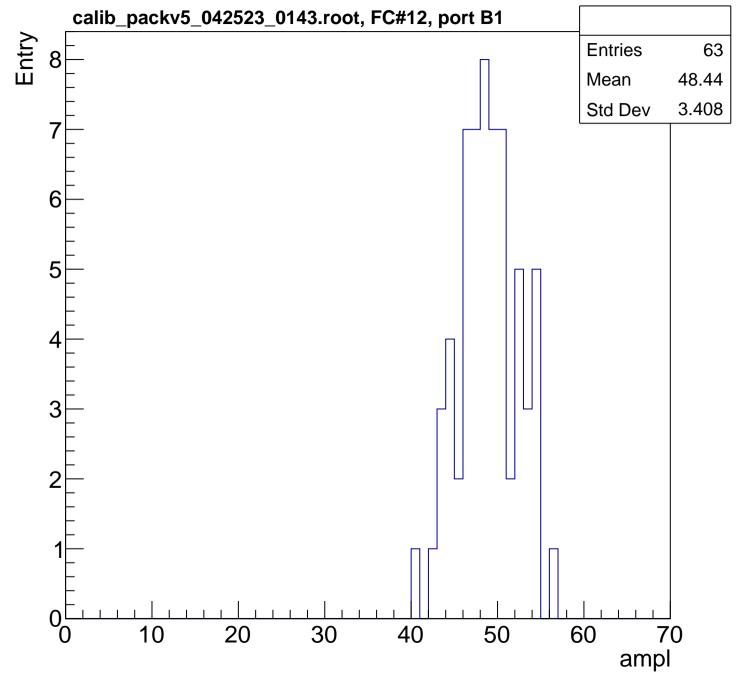


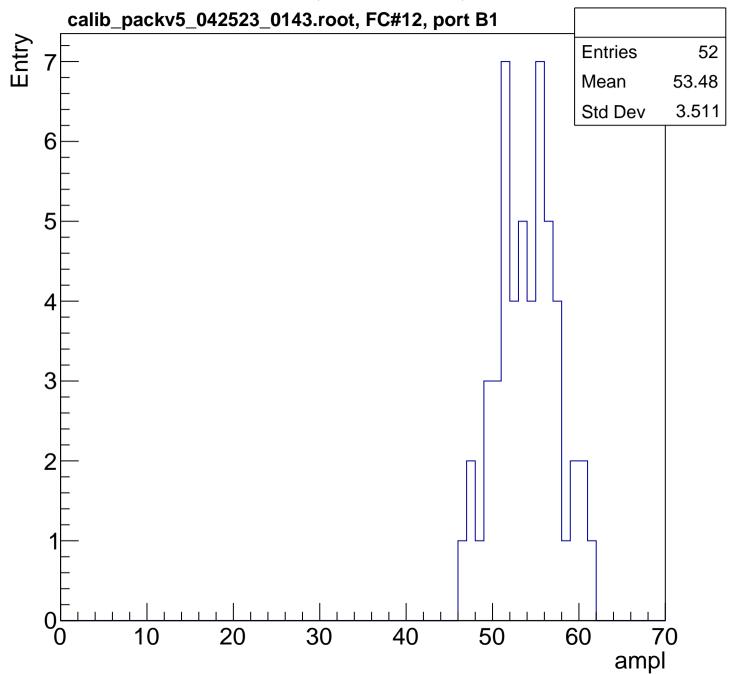
B0L102S, U2-ch63, adc7 calib_packv5_042523_0143.root, FC#12, port B1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

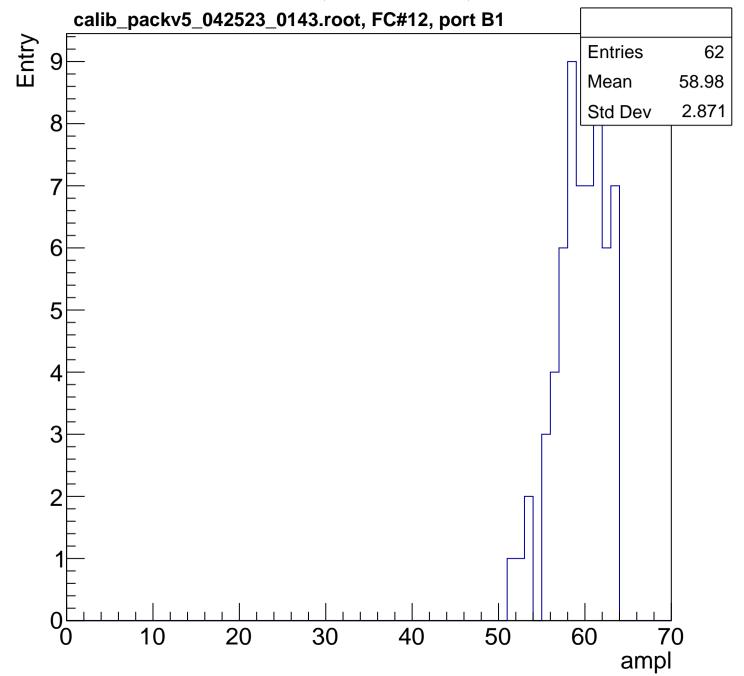


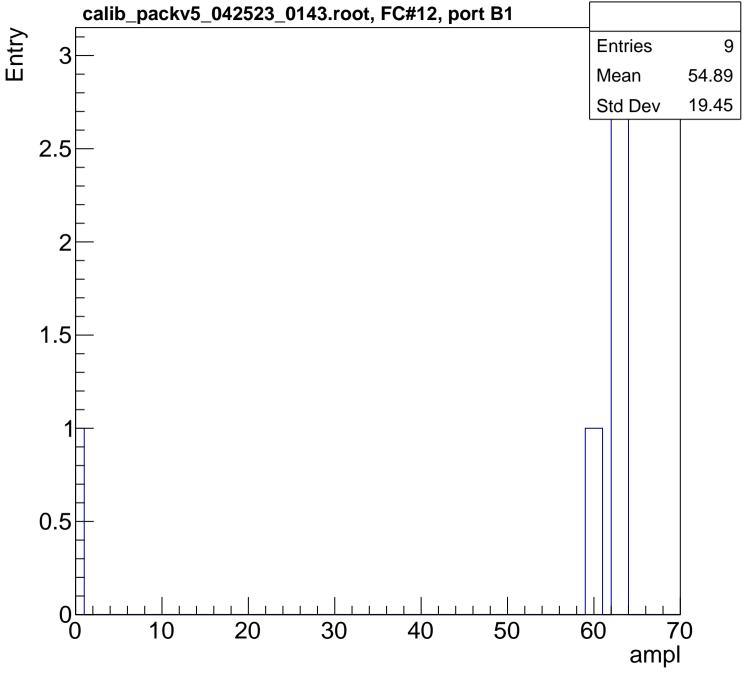




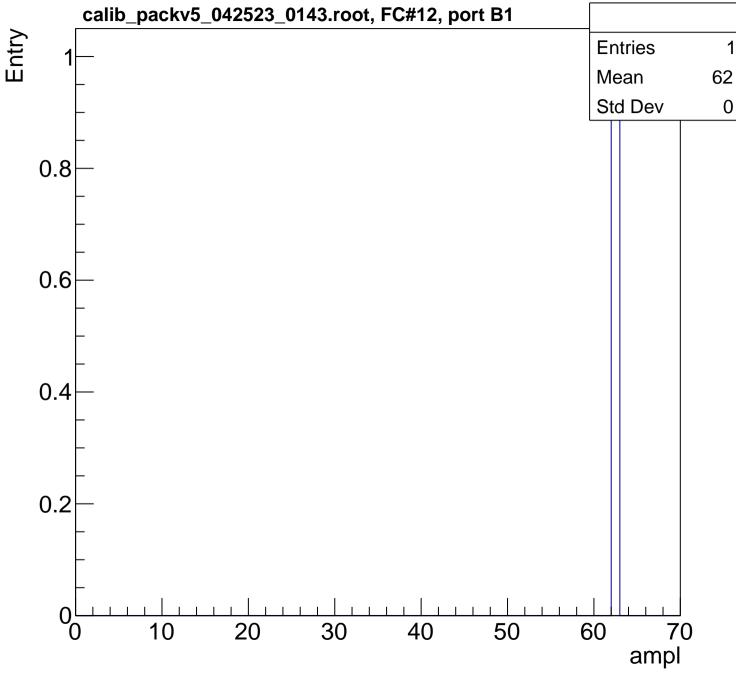


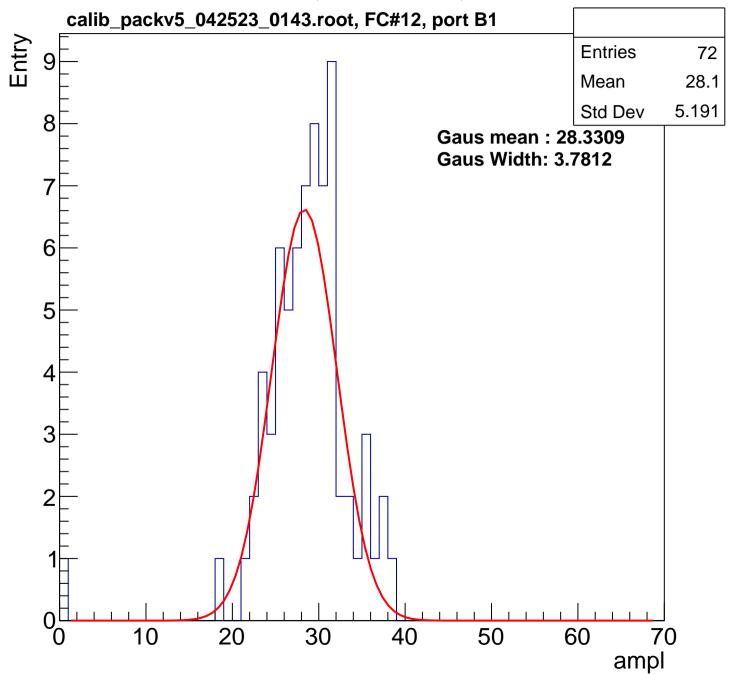


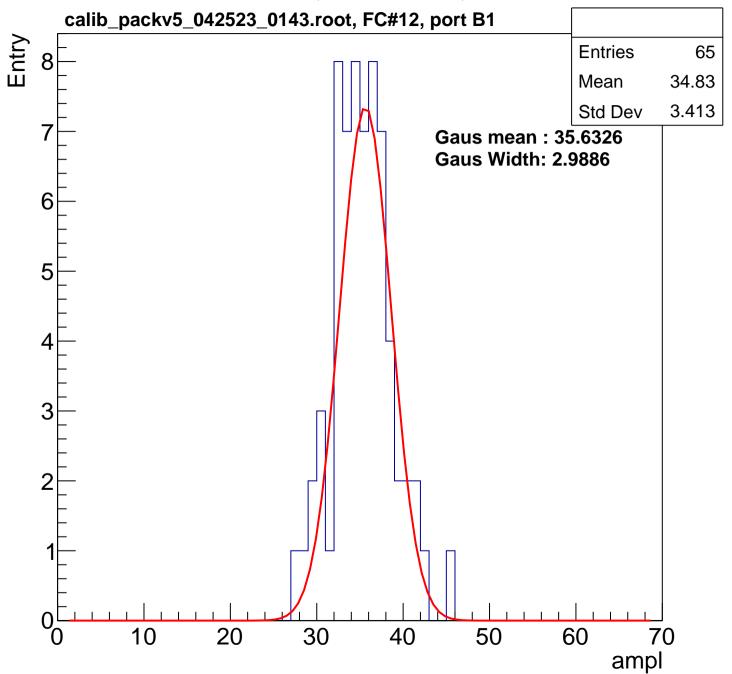


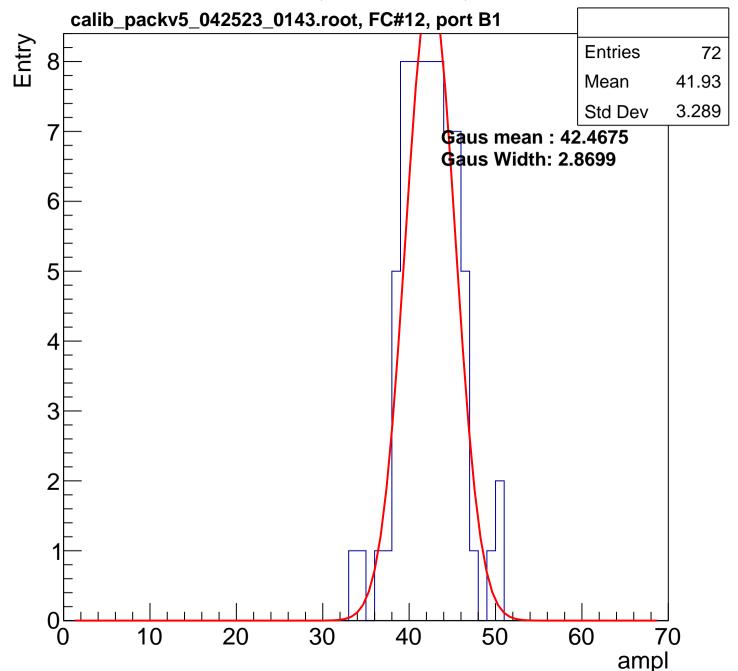


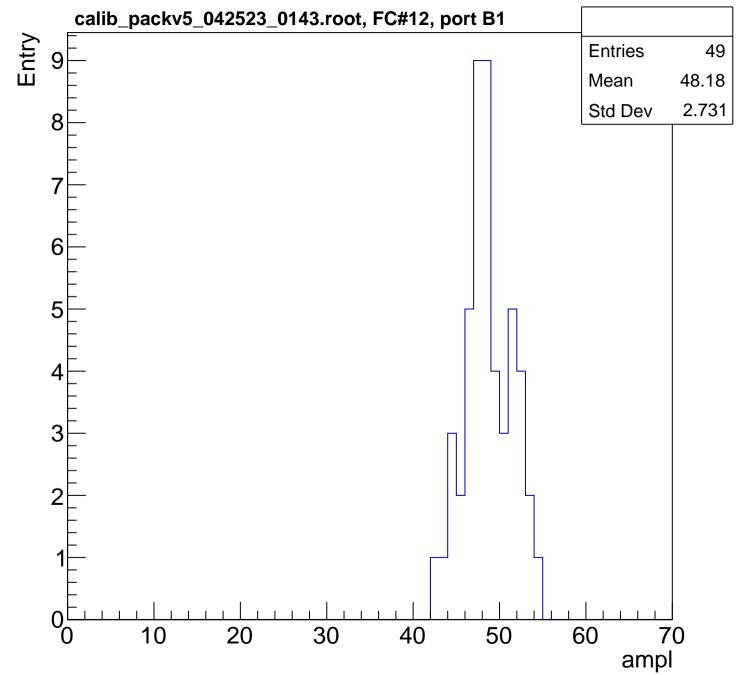
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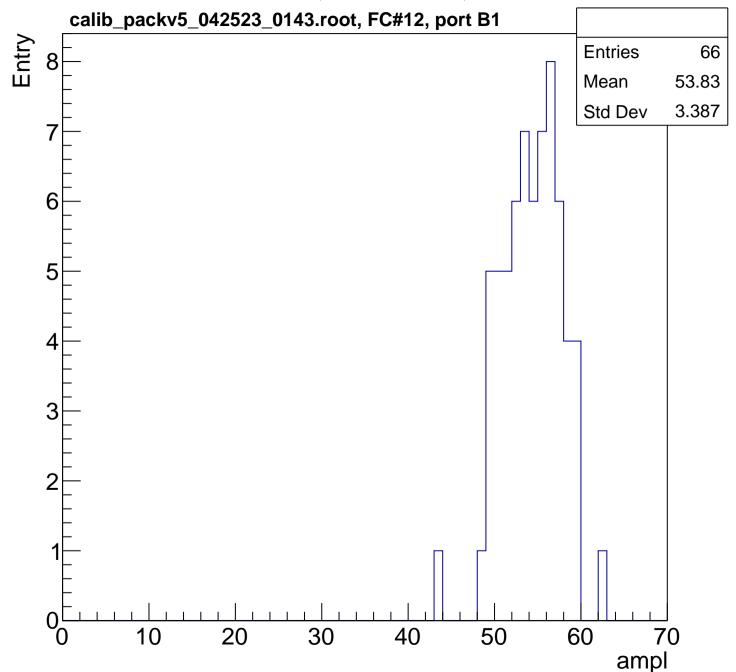


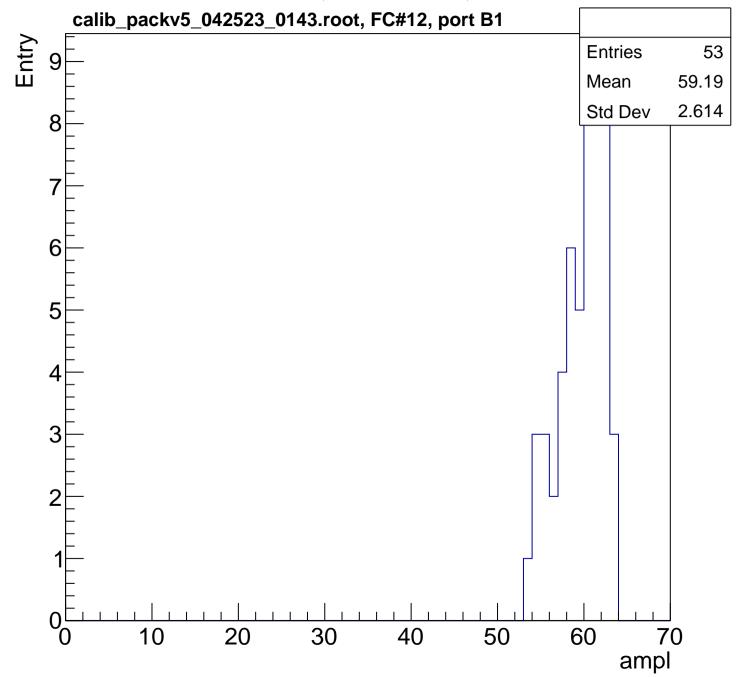


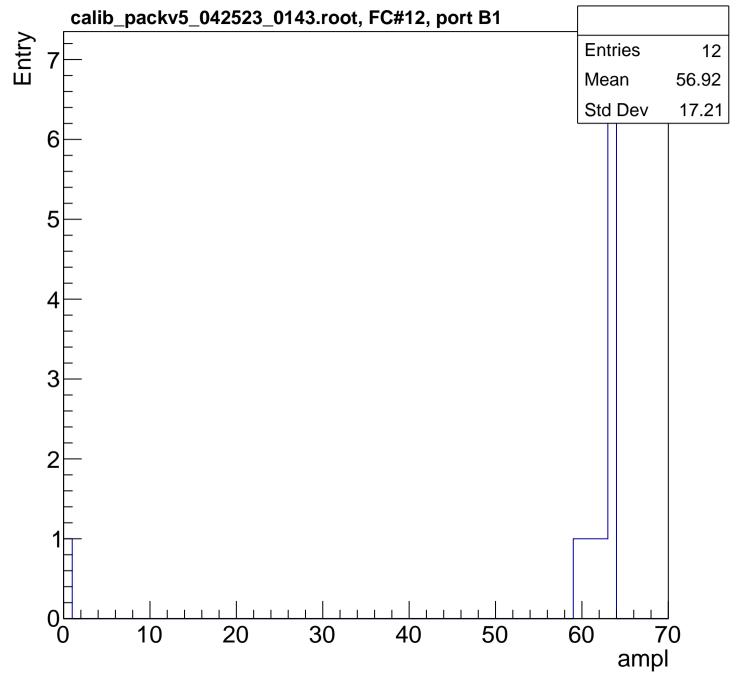




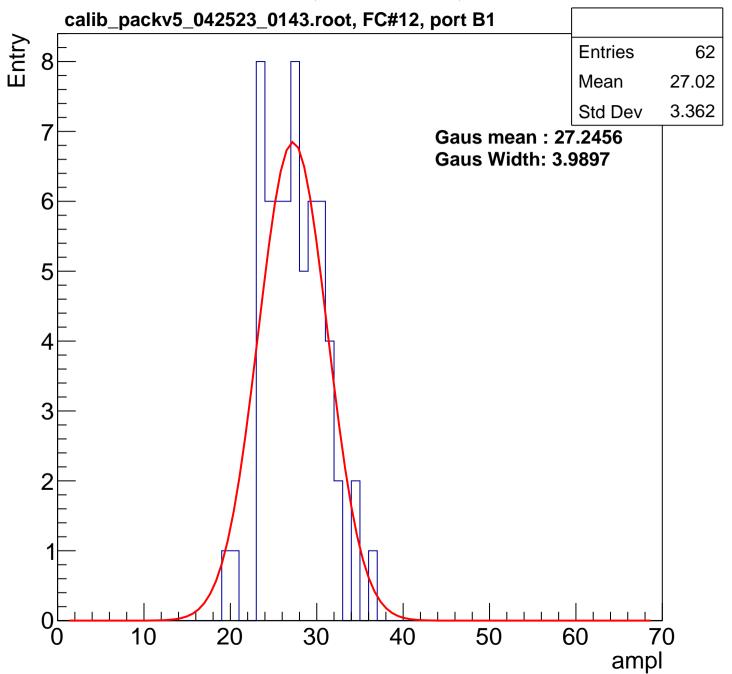


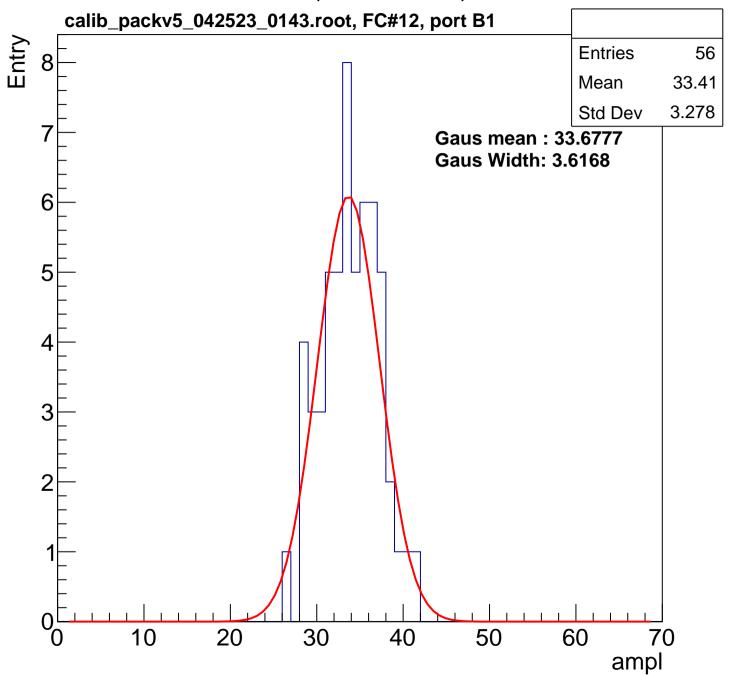


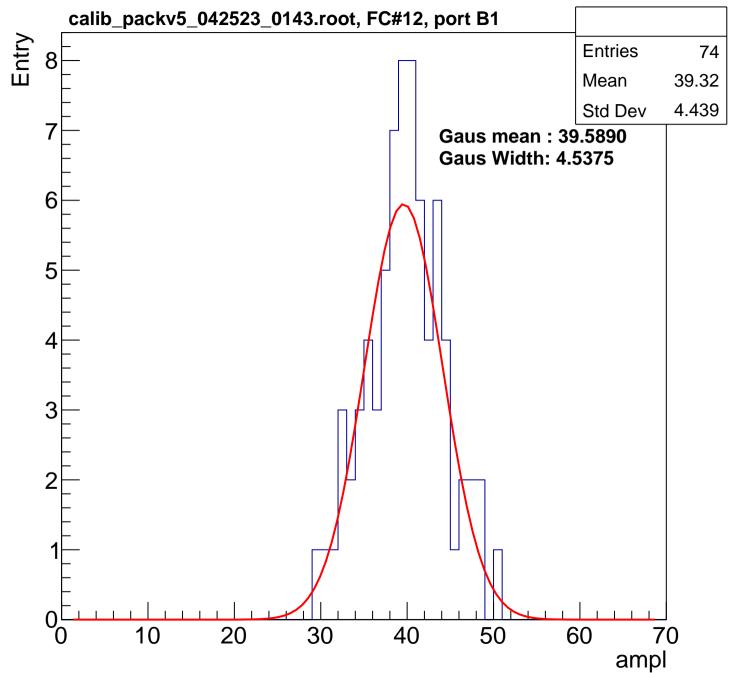


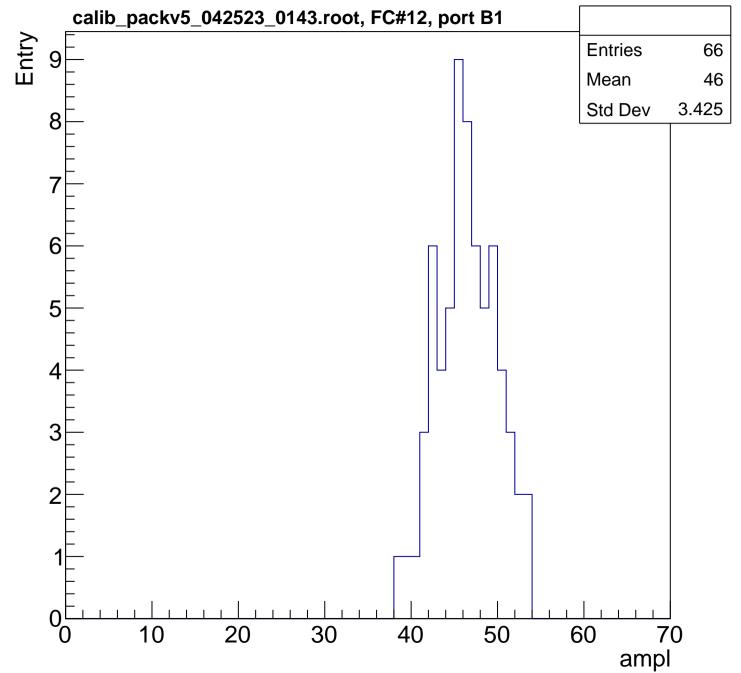


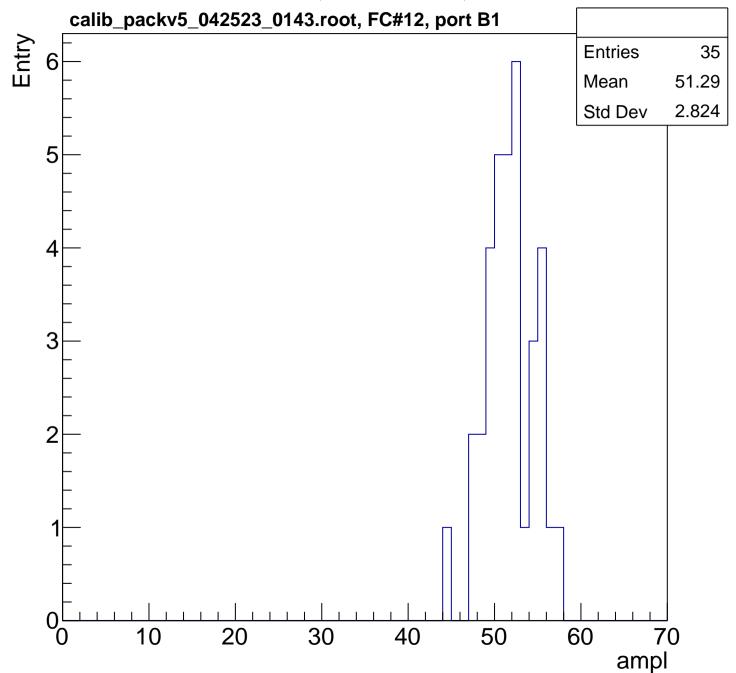
B0L102S, U2-ch65, adc7 calib_packv5_042523_0143.root, FC#12, port B1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

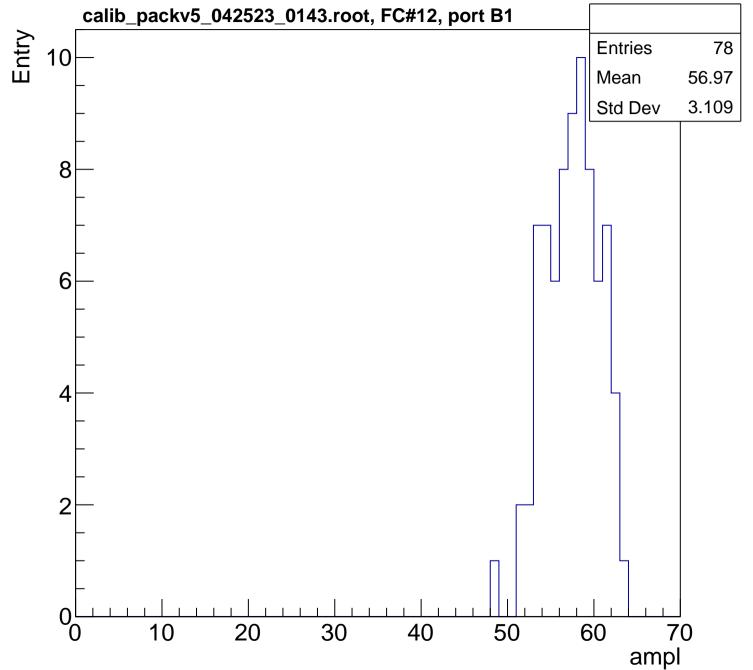


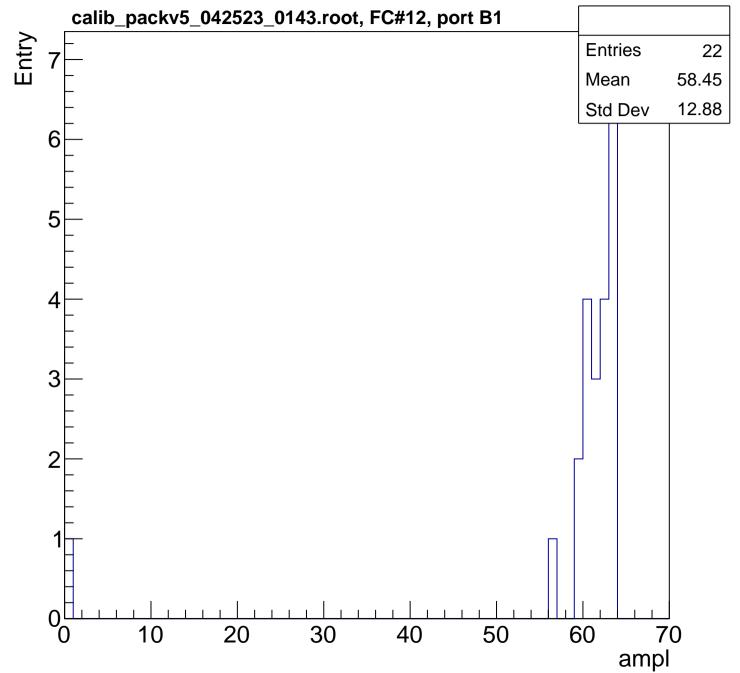


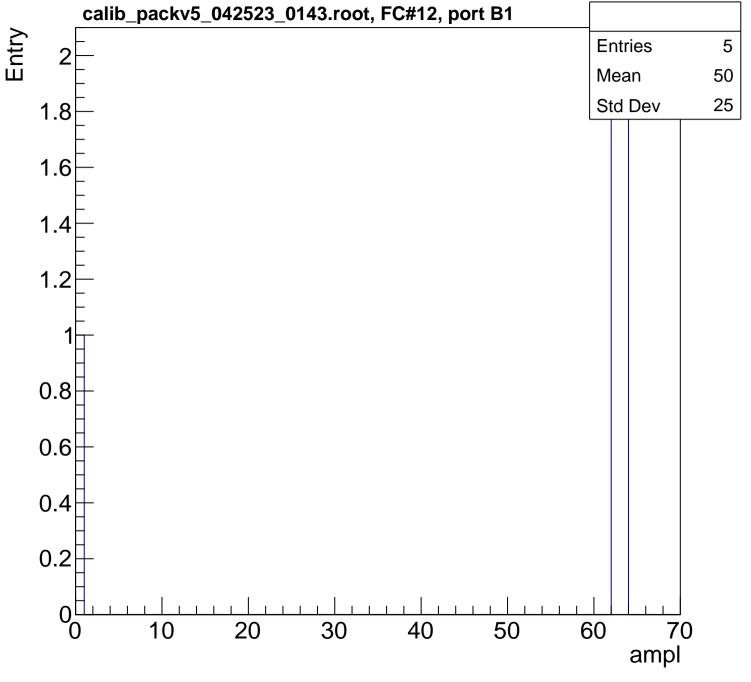


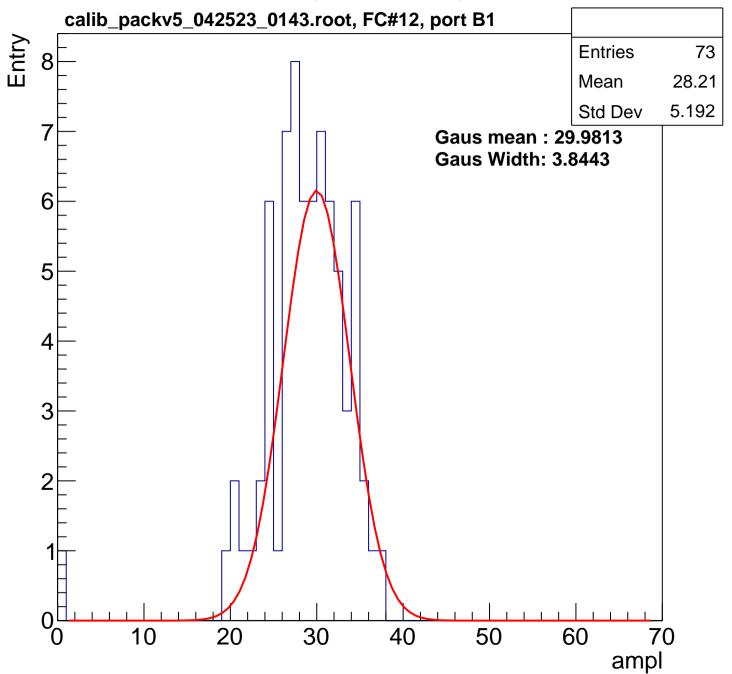


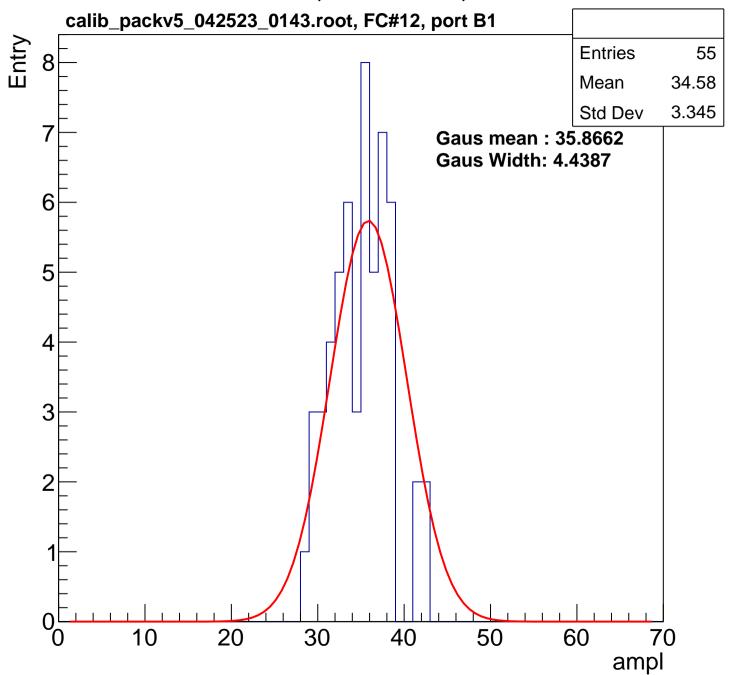


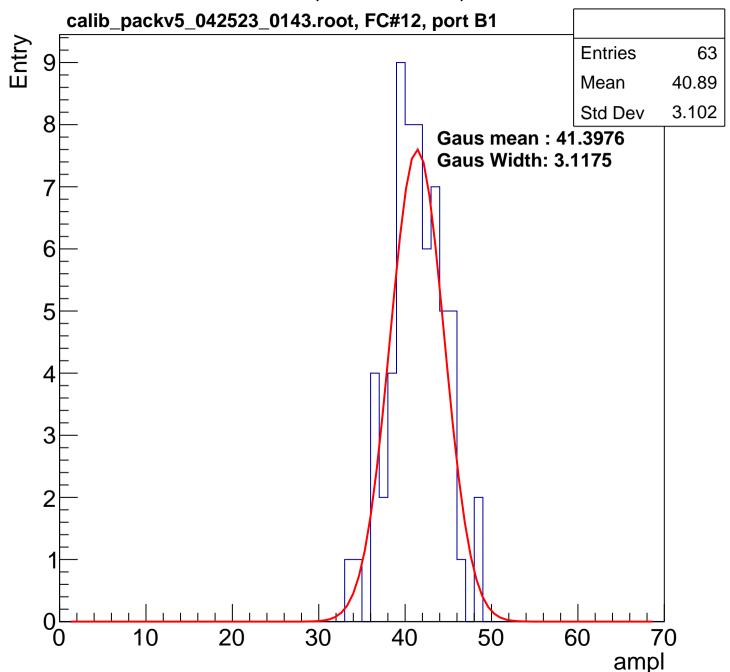


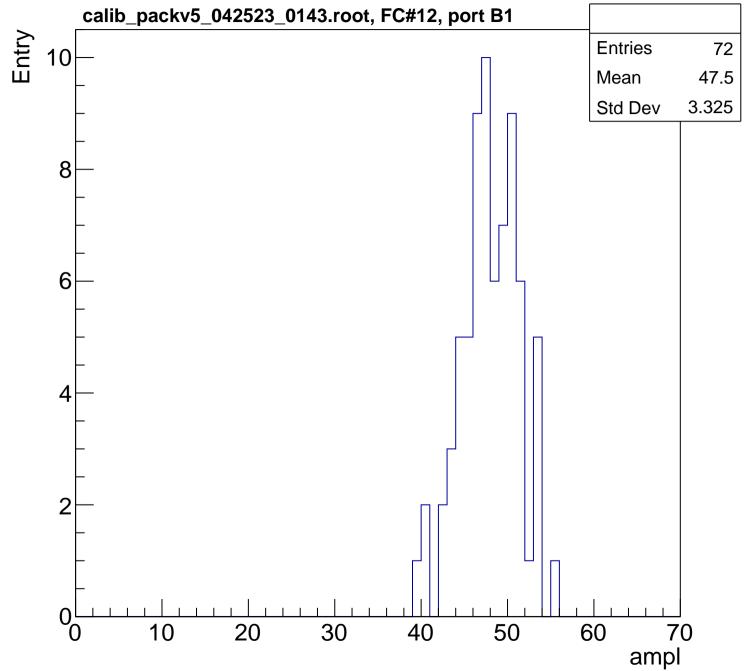


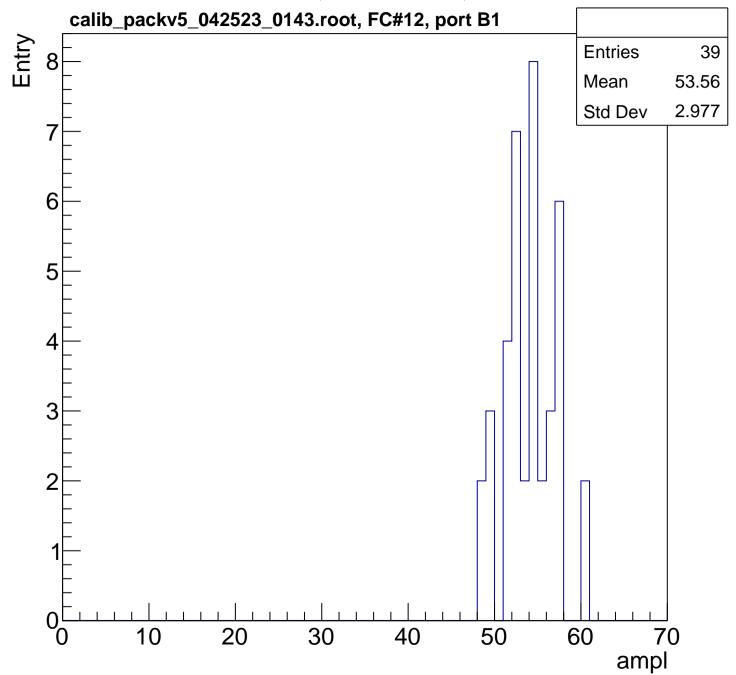


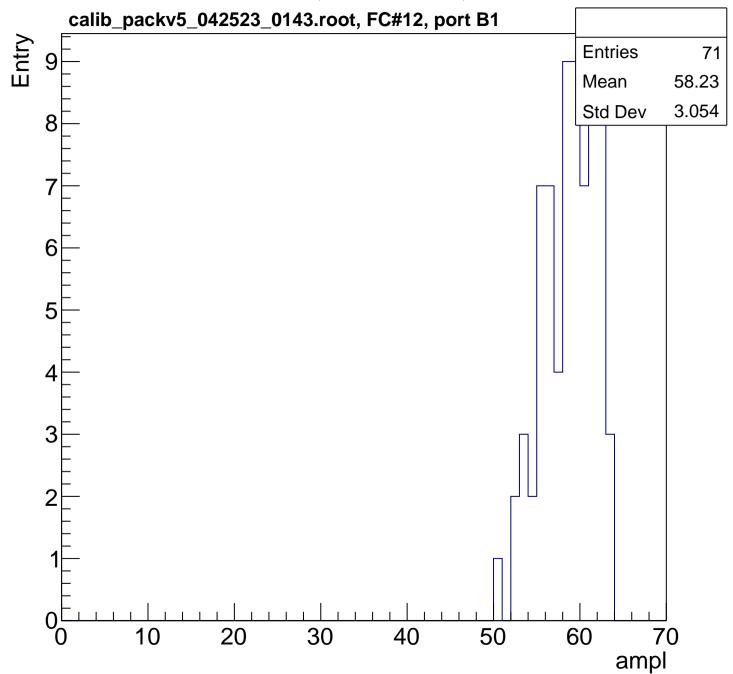


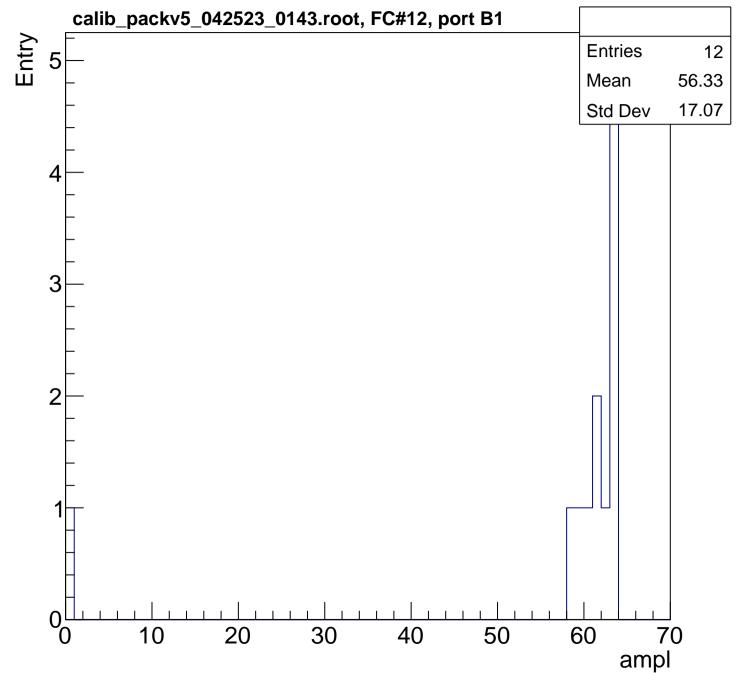


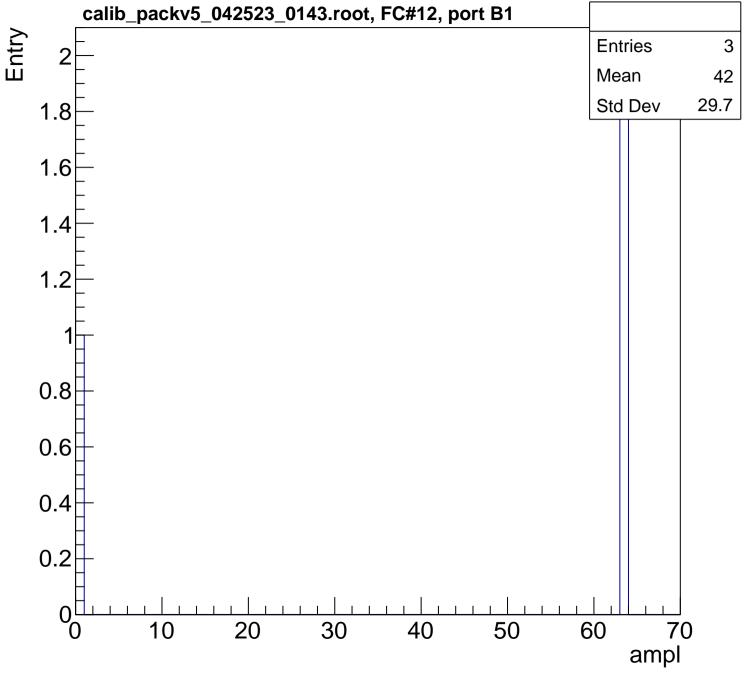


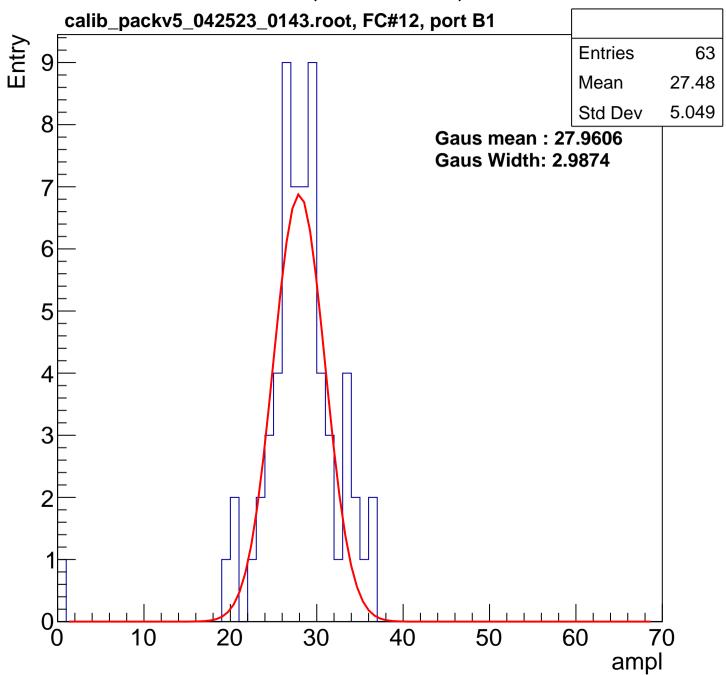


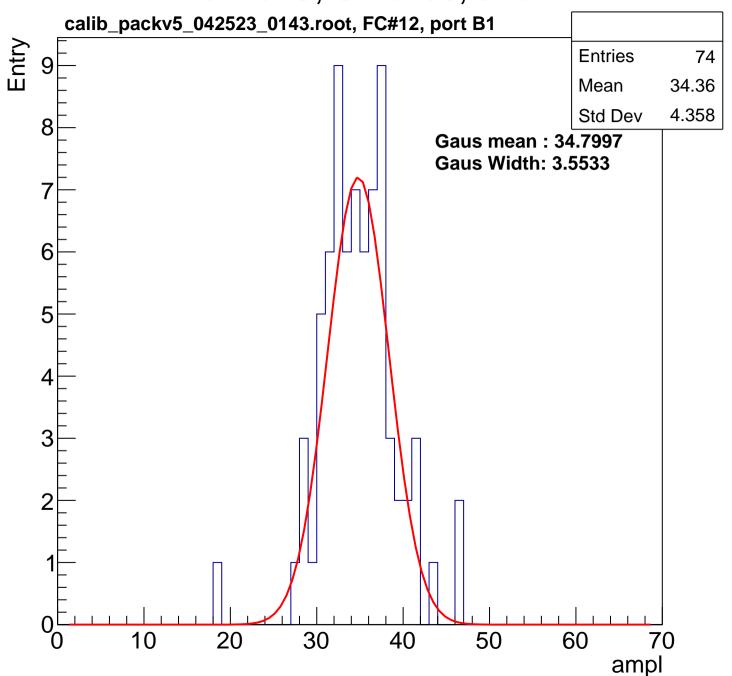


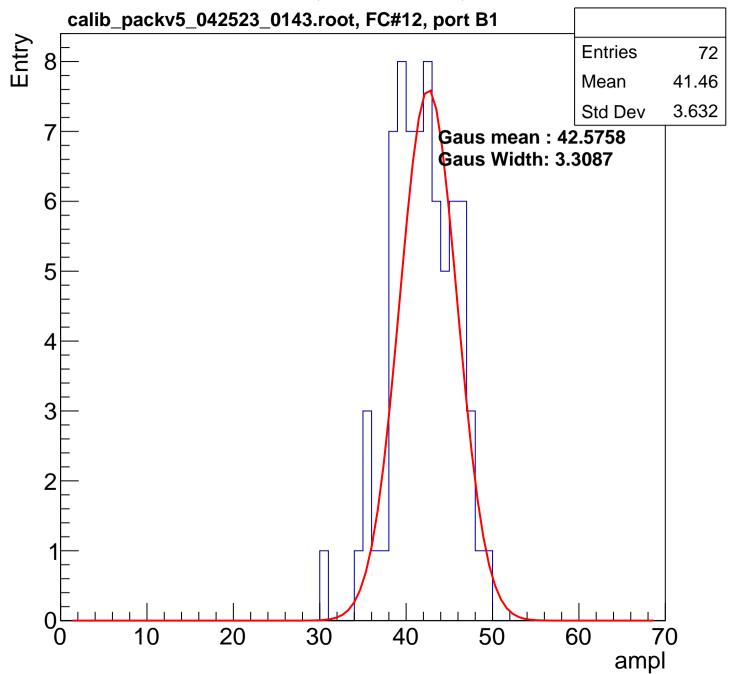


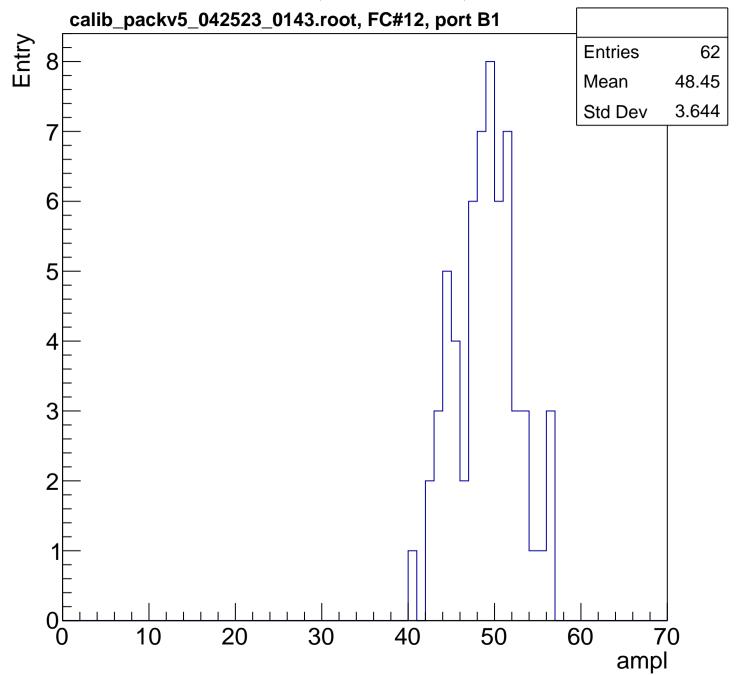


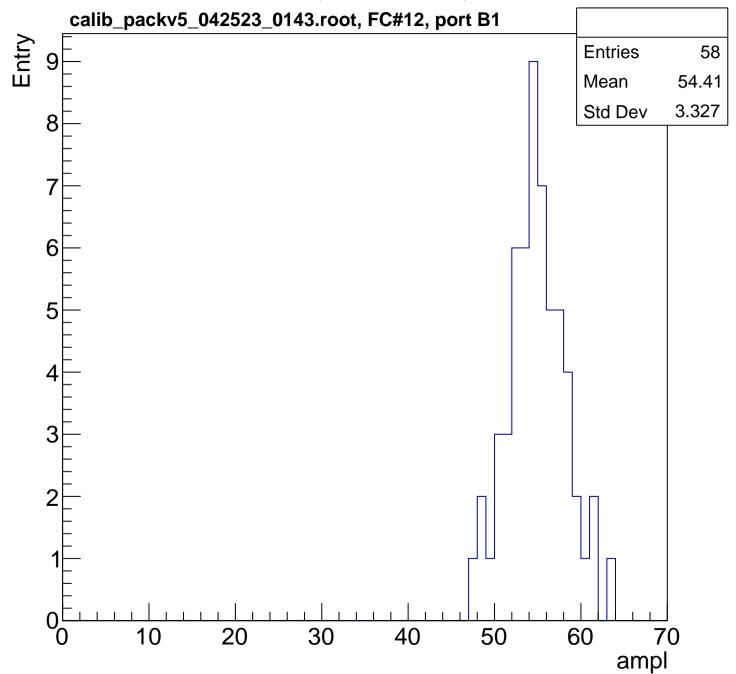


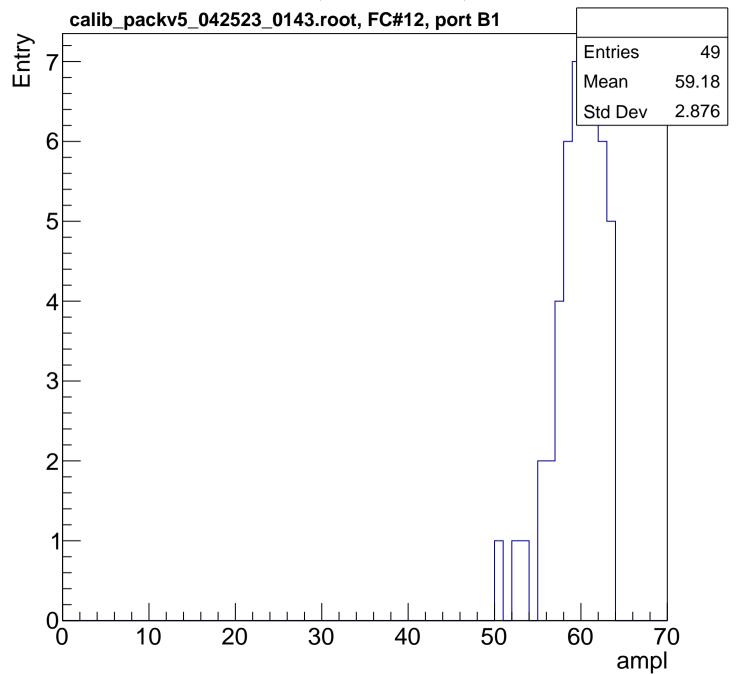


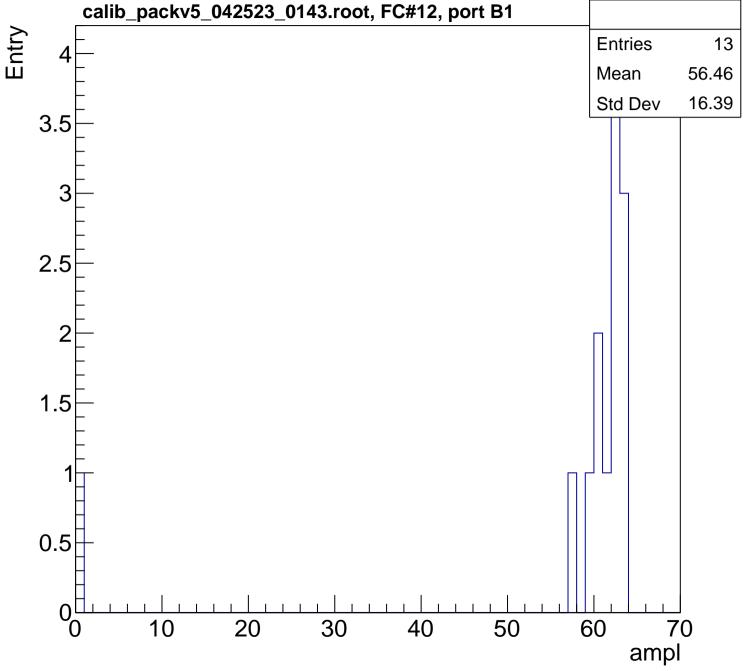


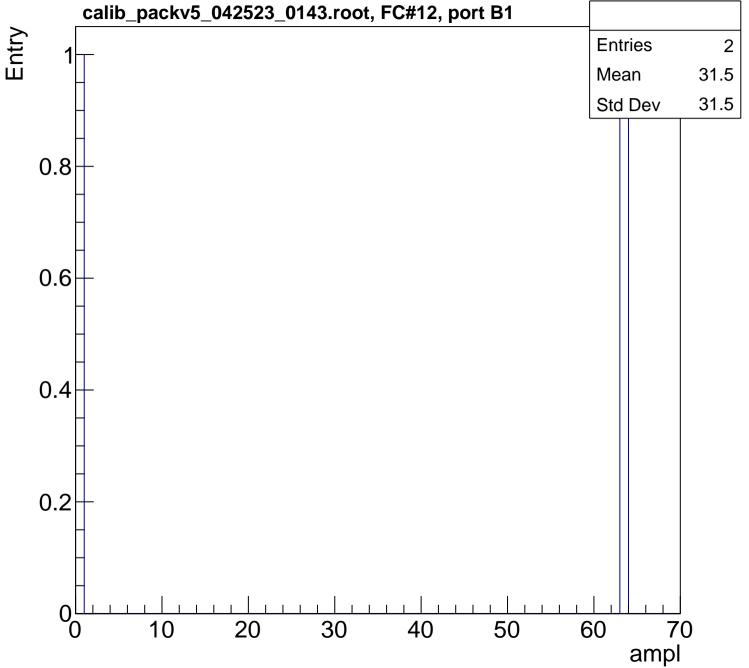


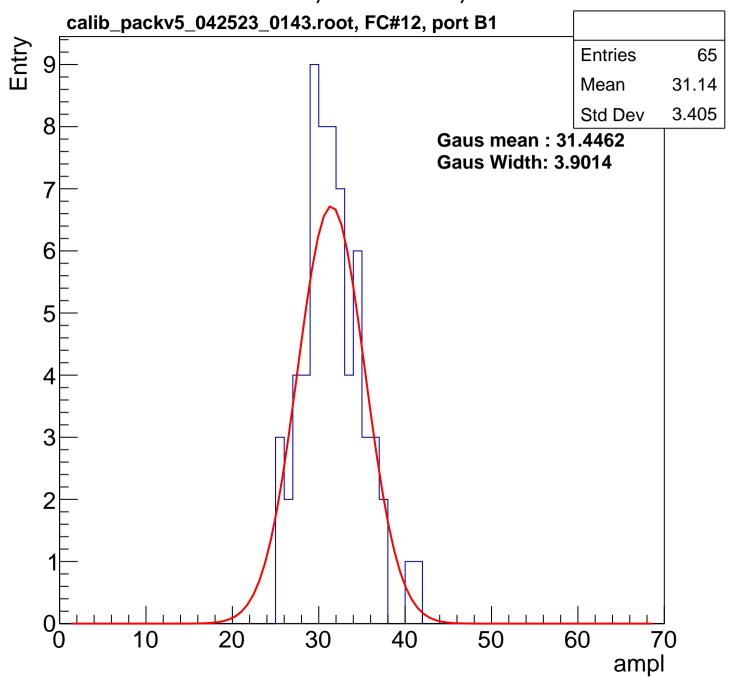


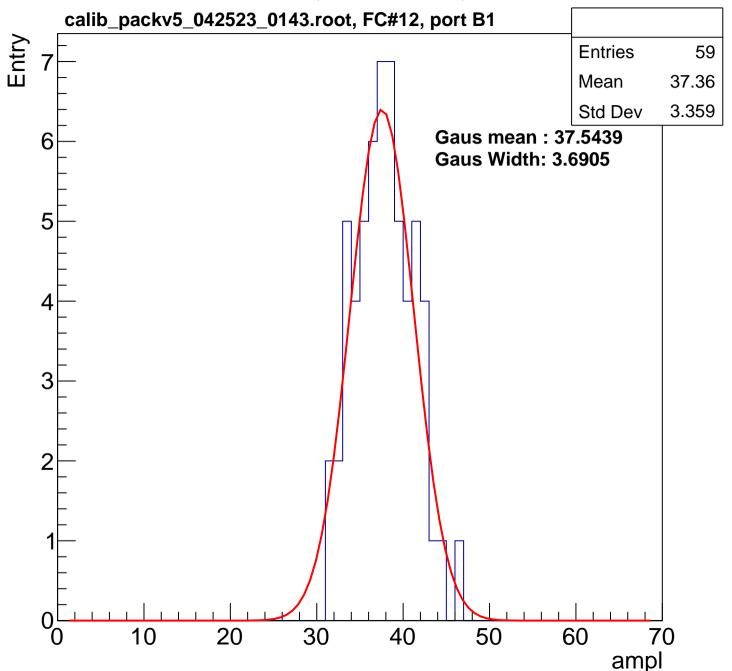


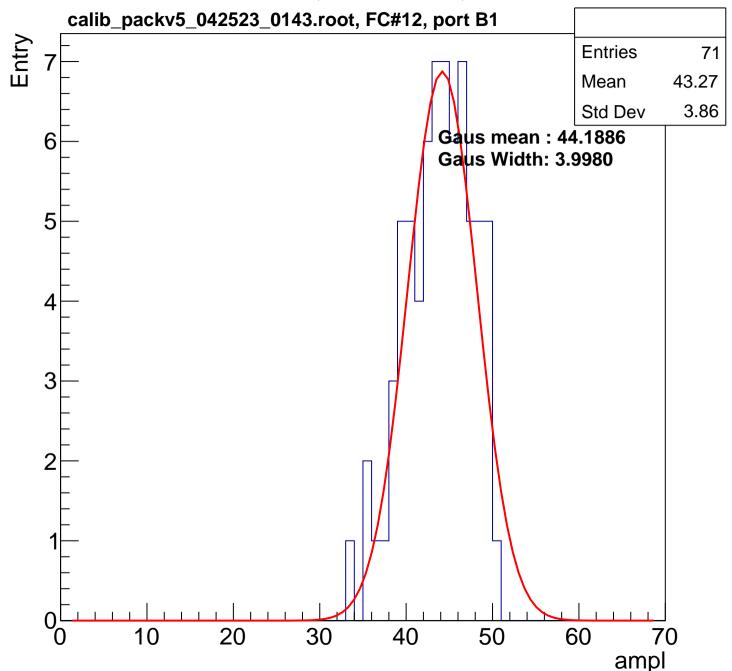


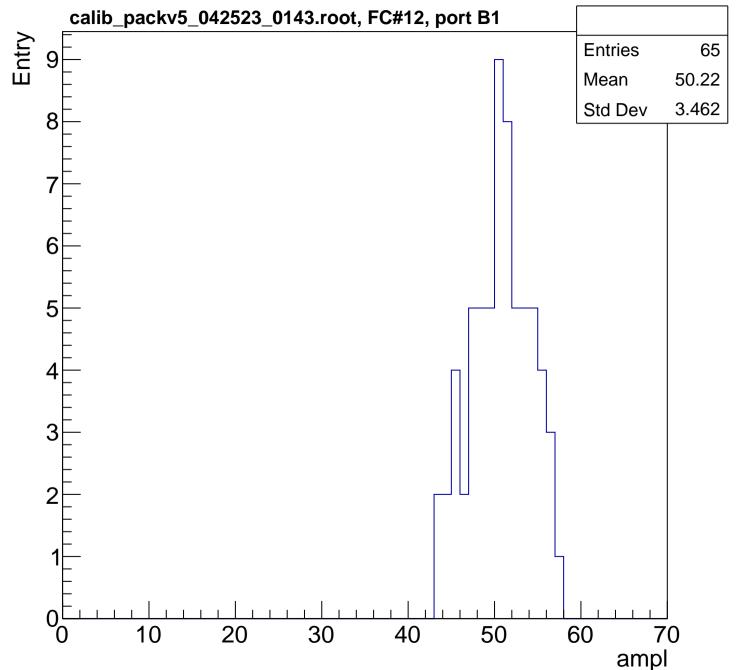


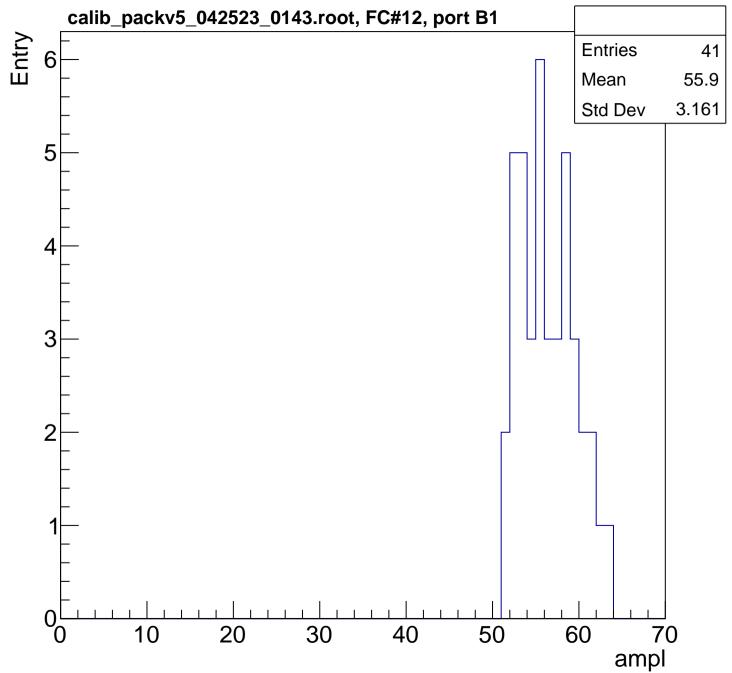


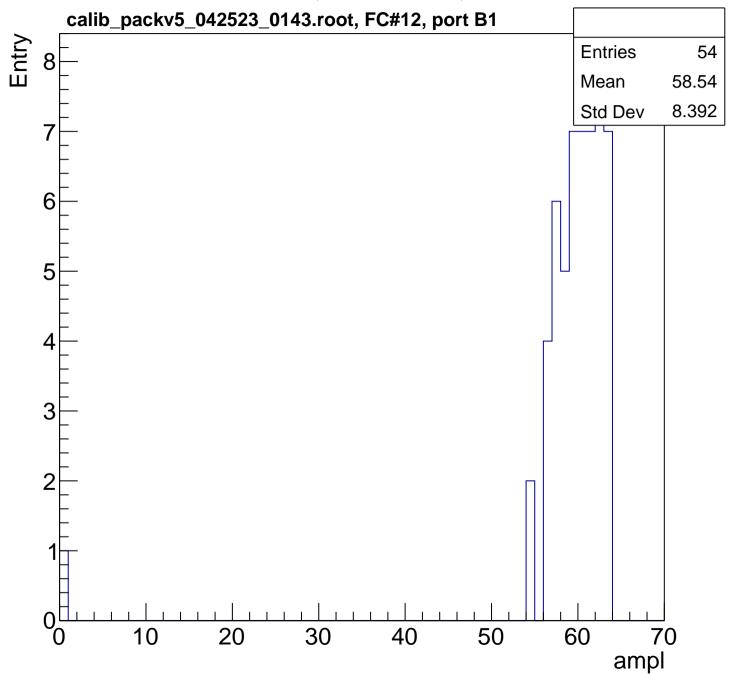


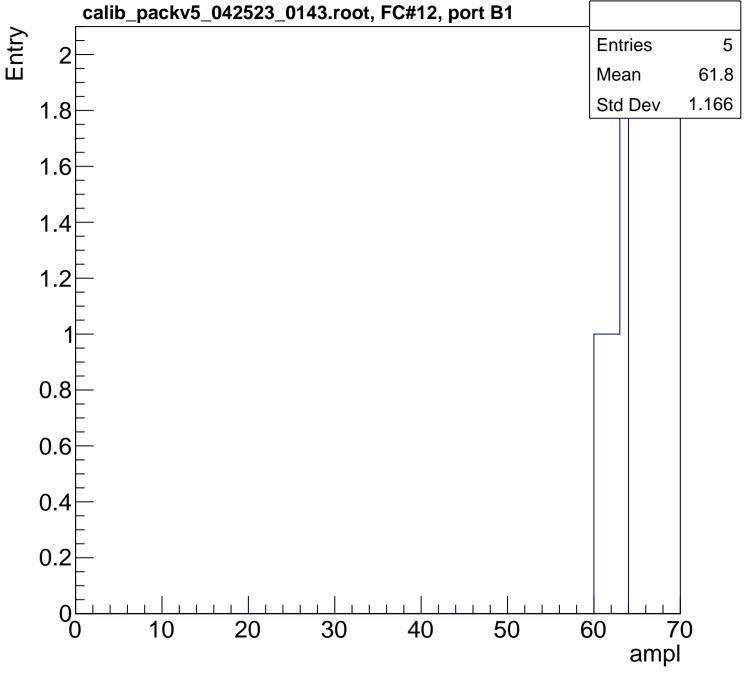


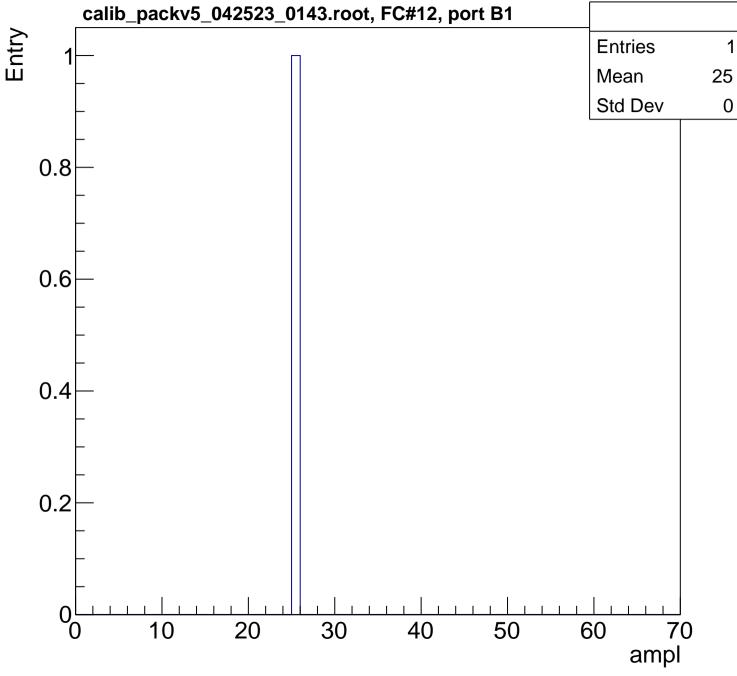


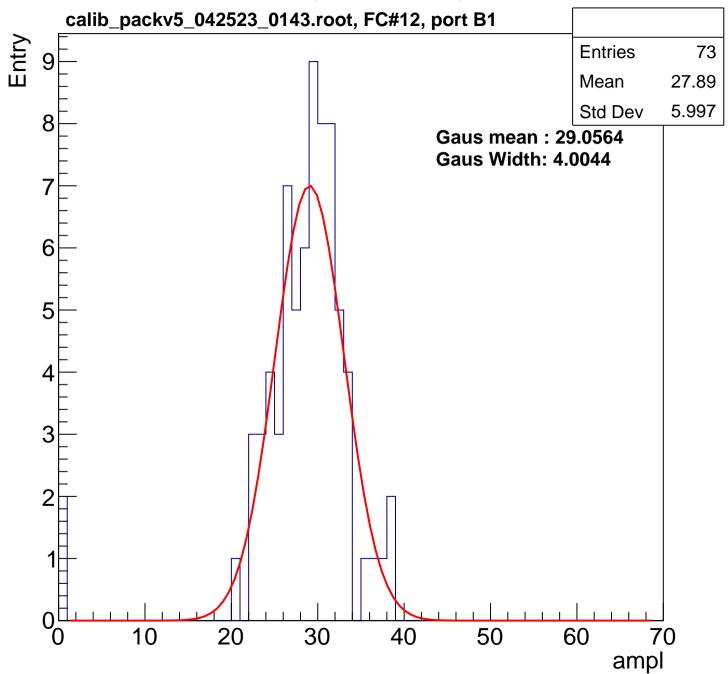


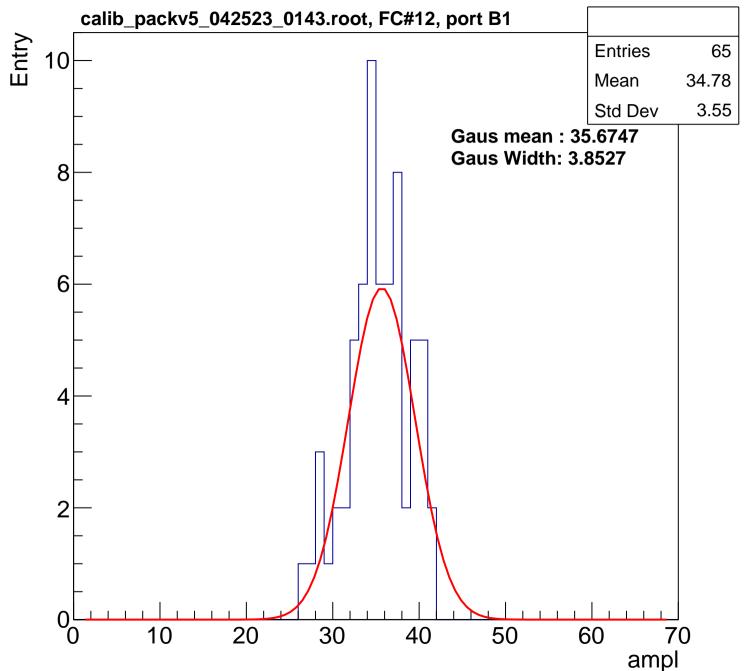


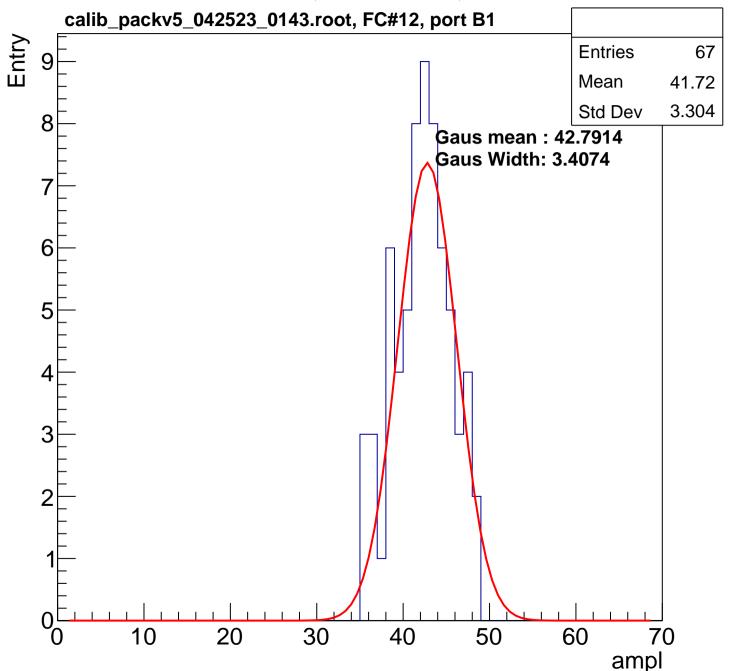


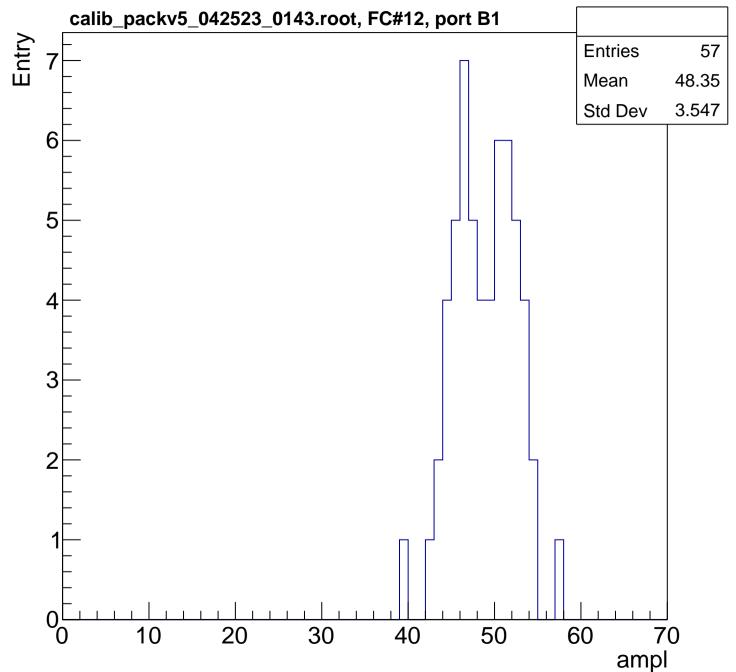


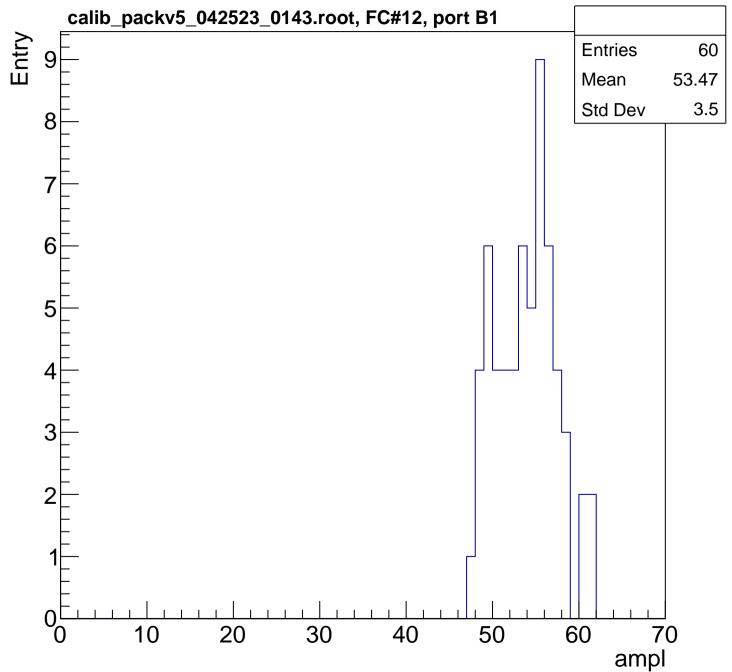


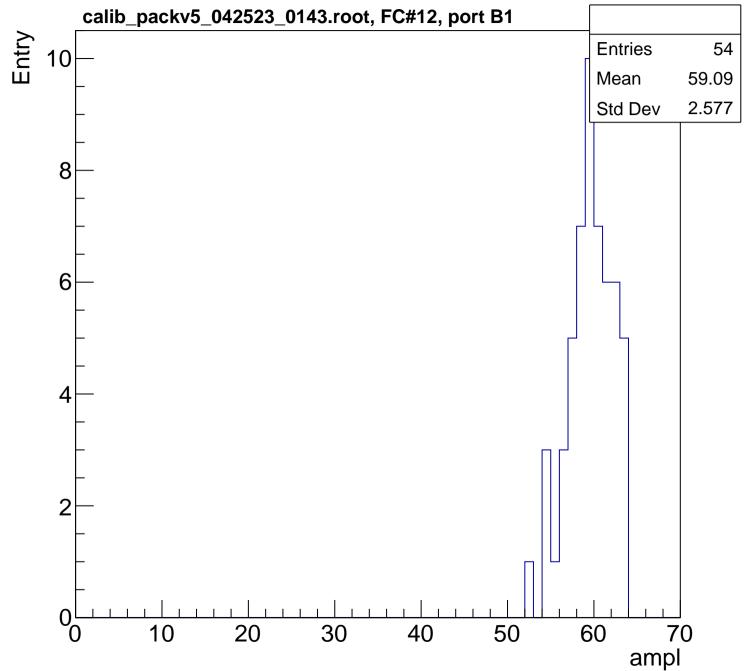


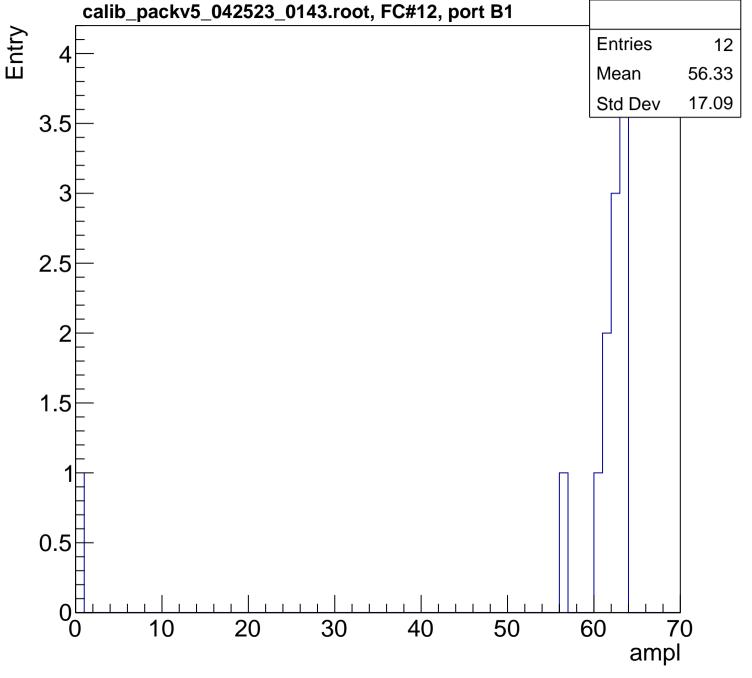


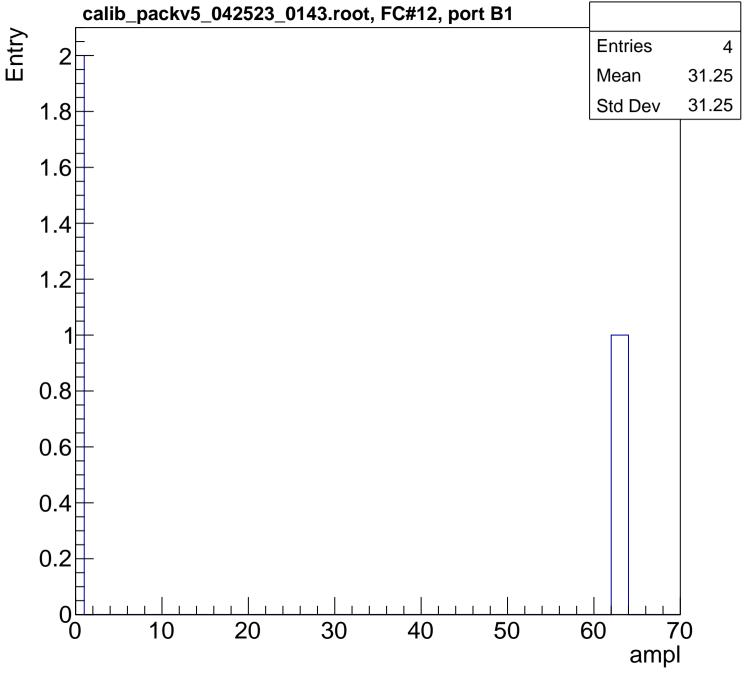


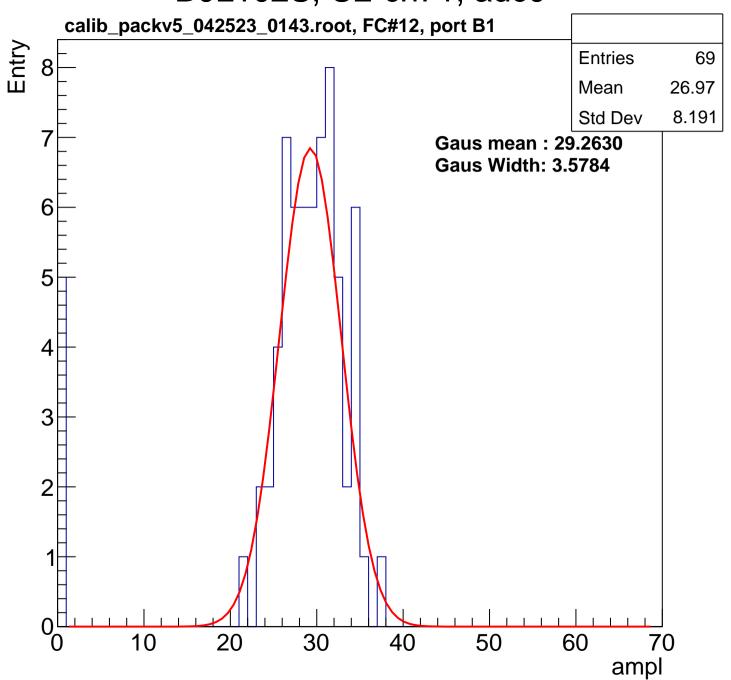


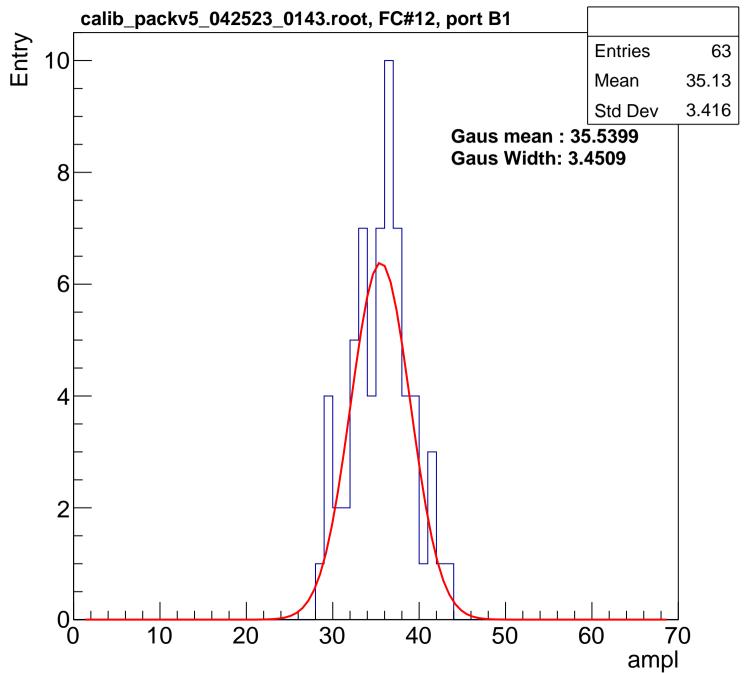


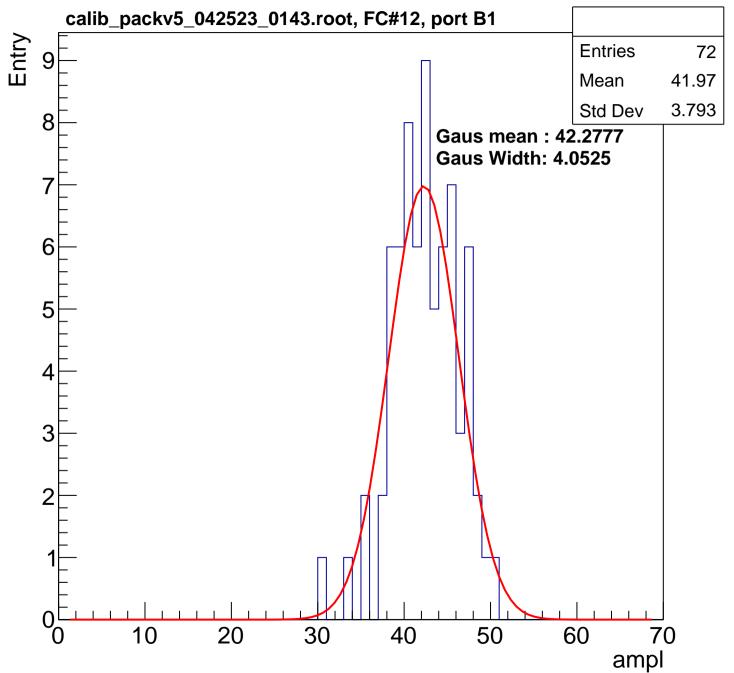


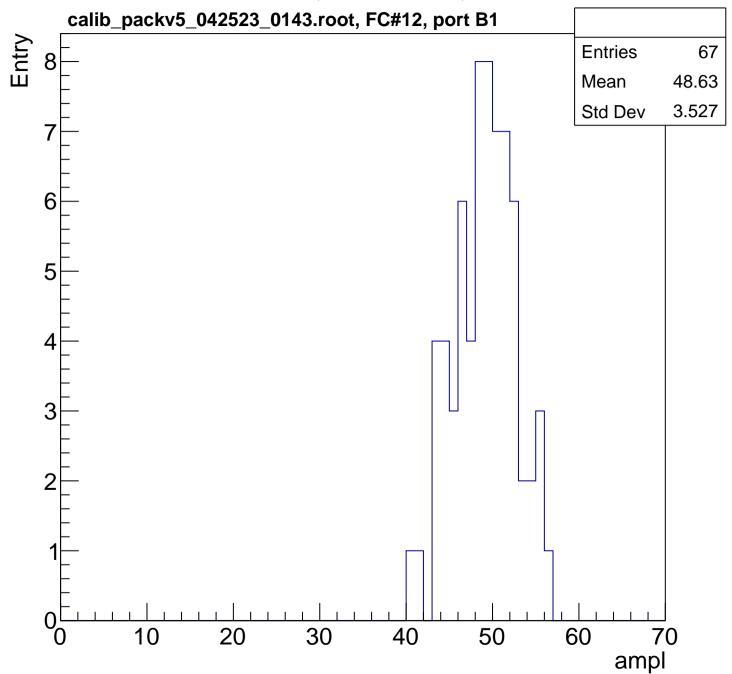


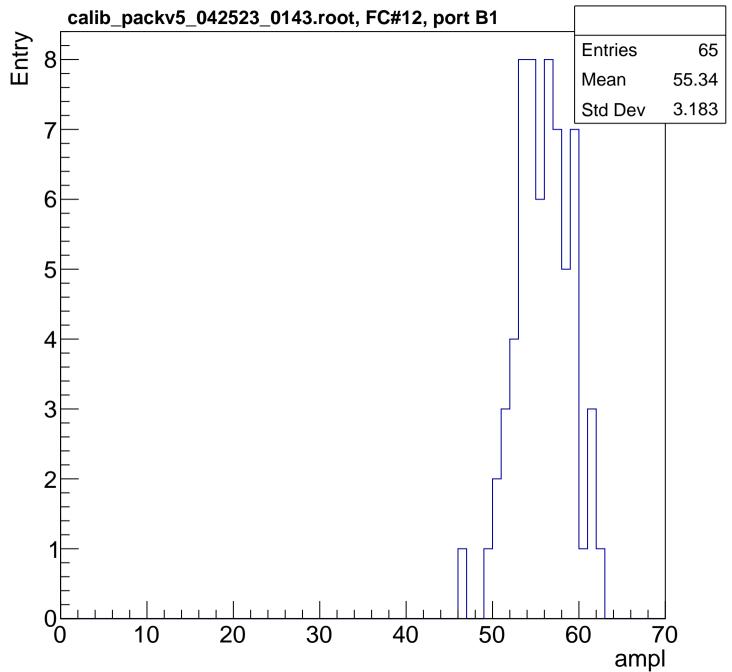


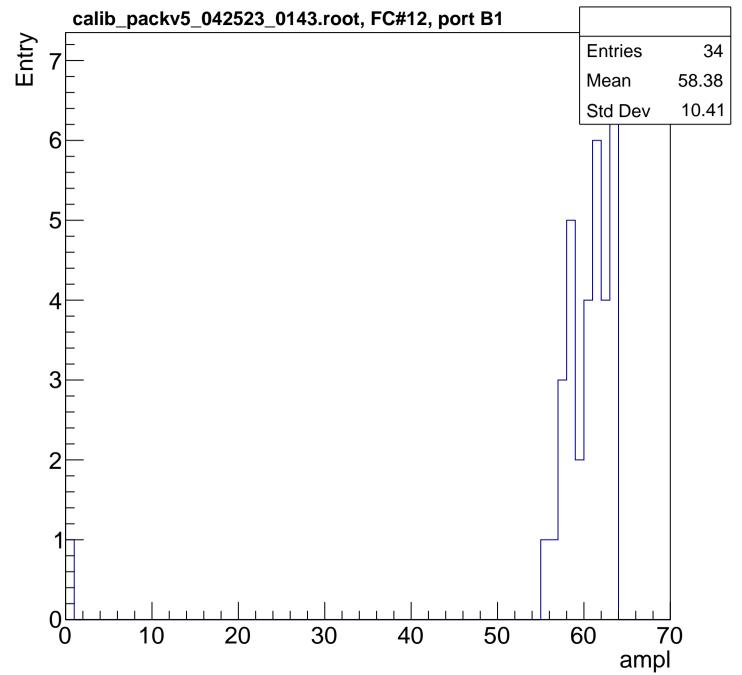


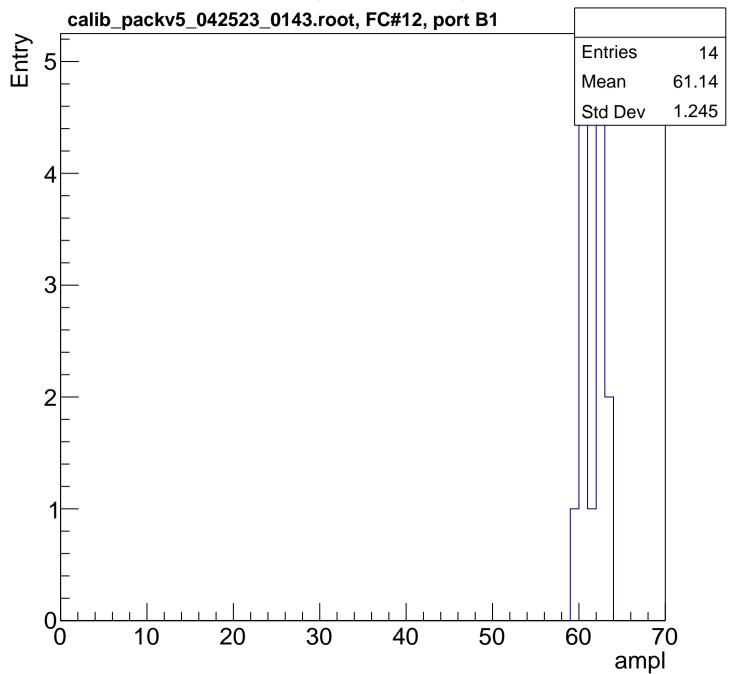


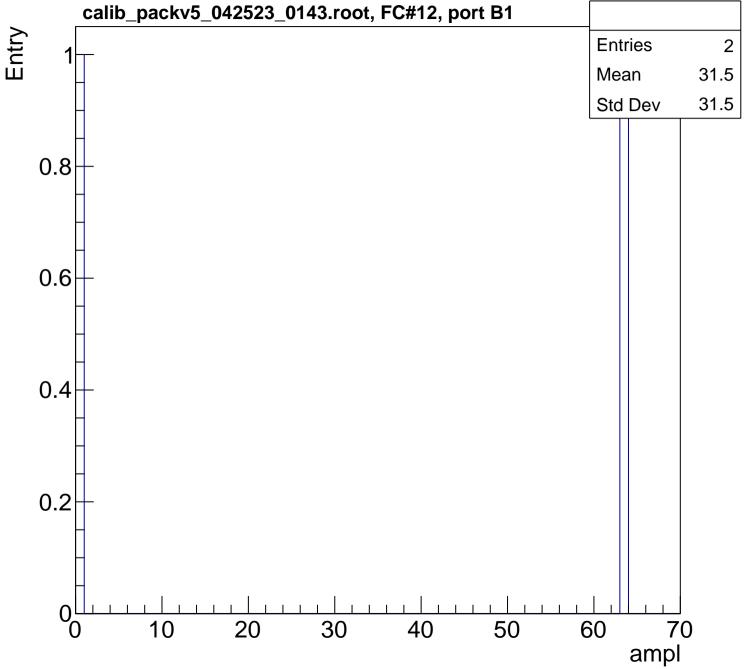


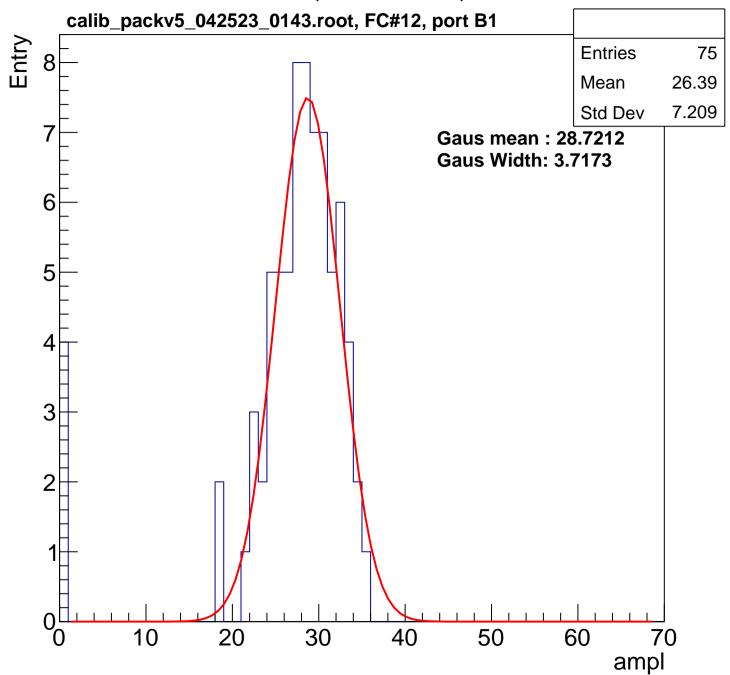


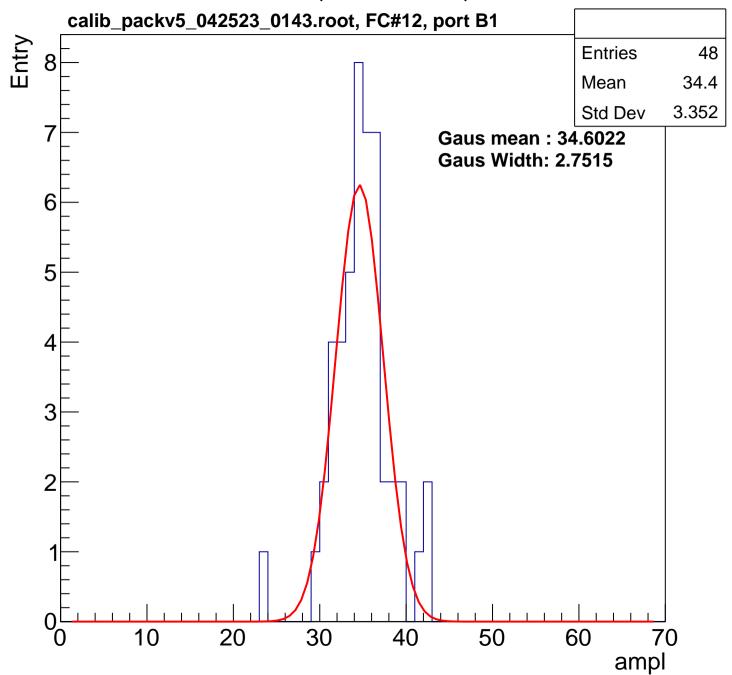


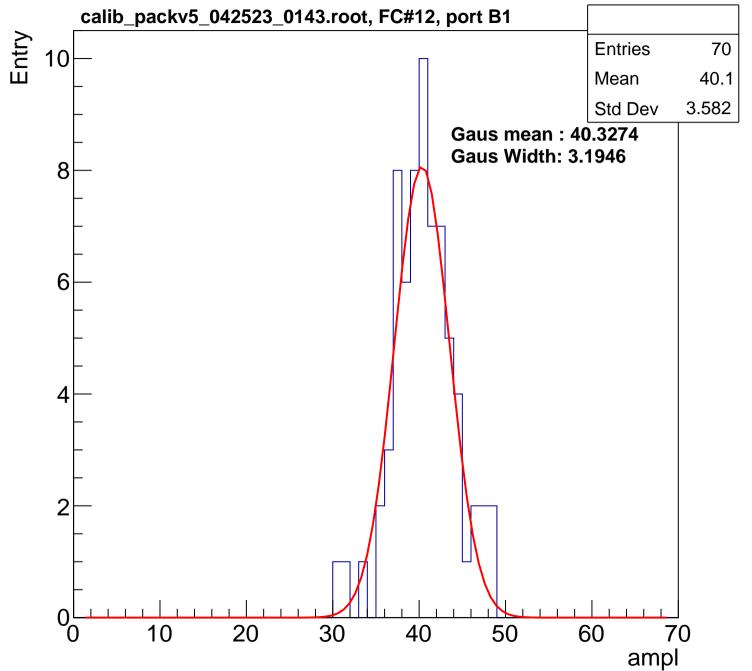


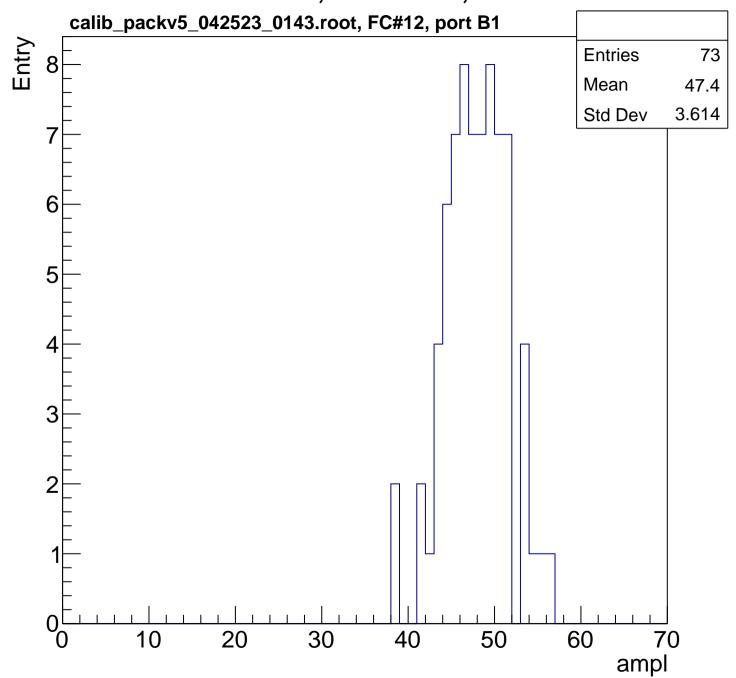


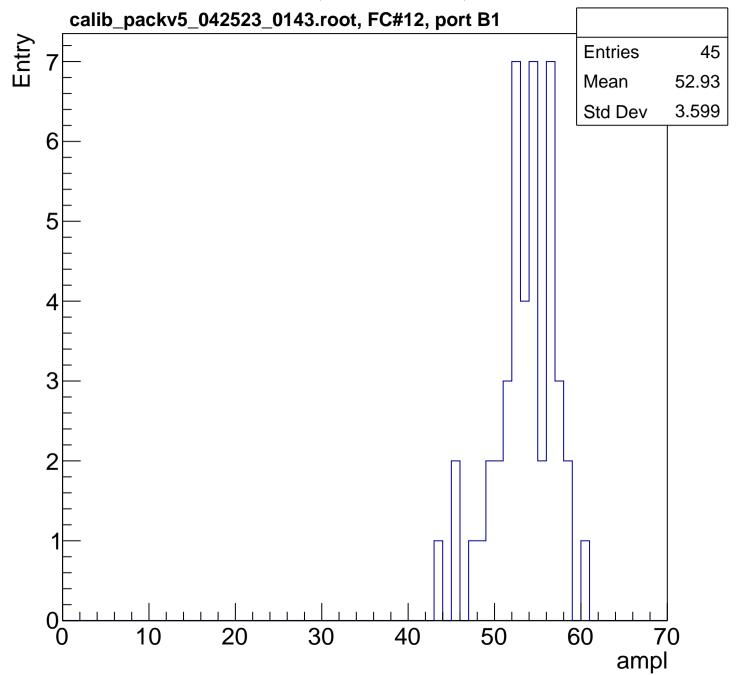


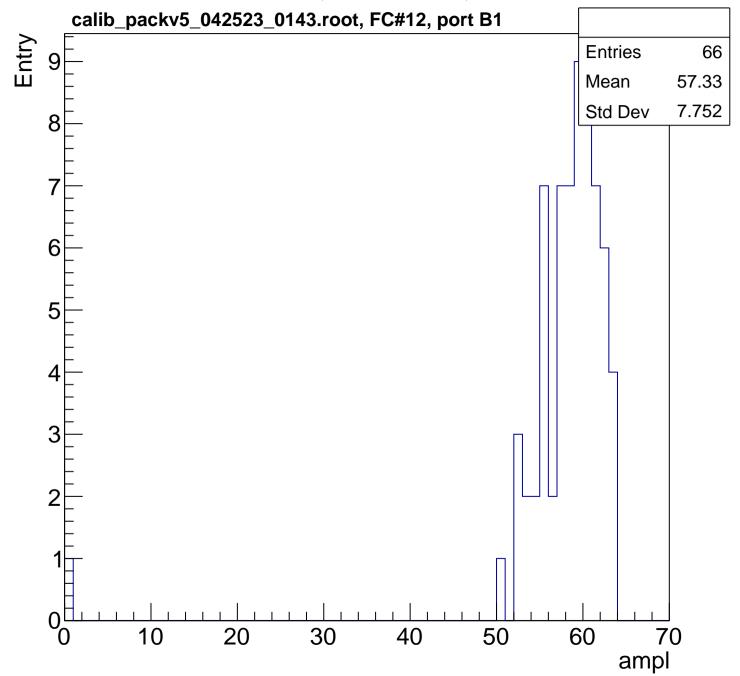


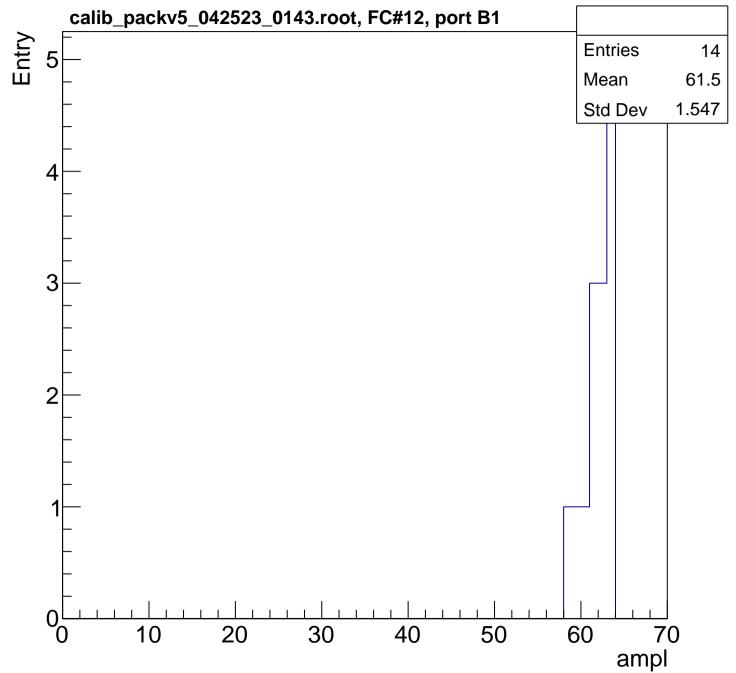


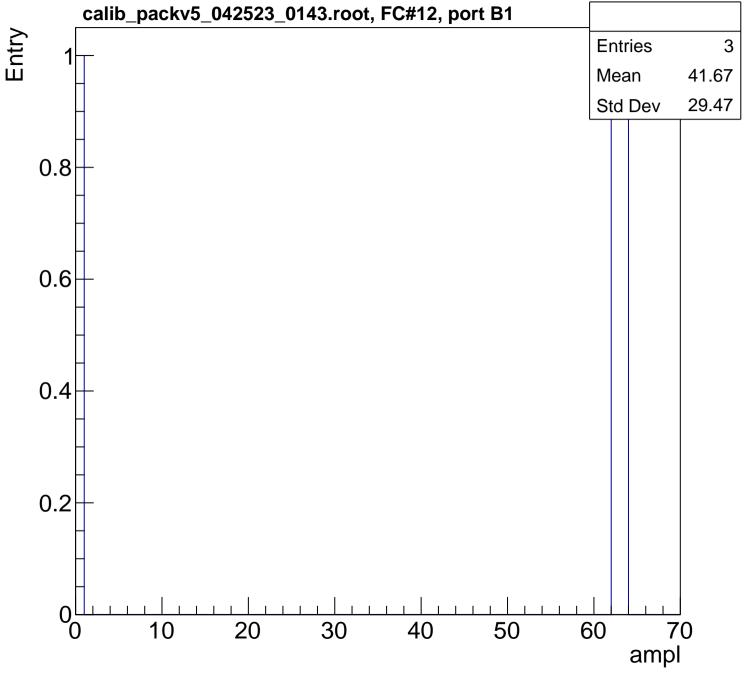


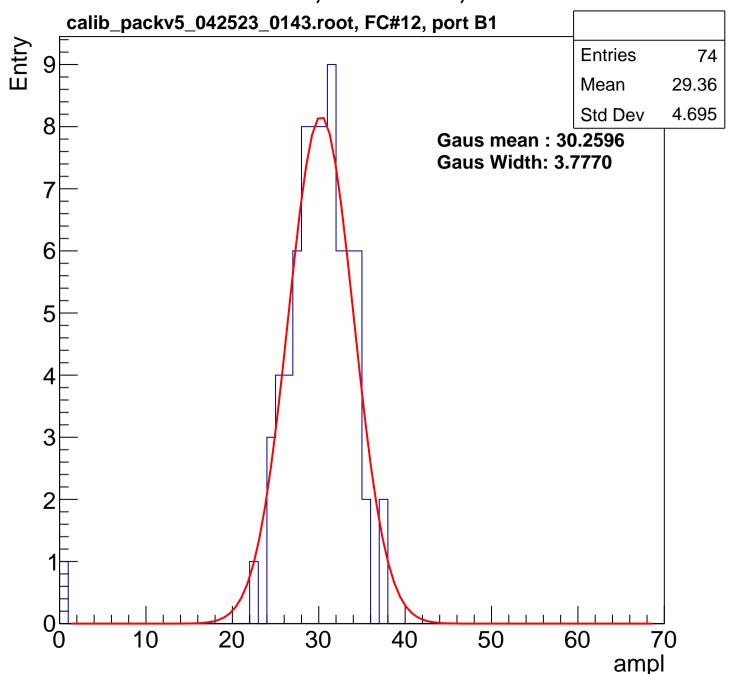


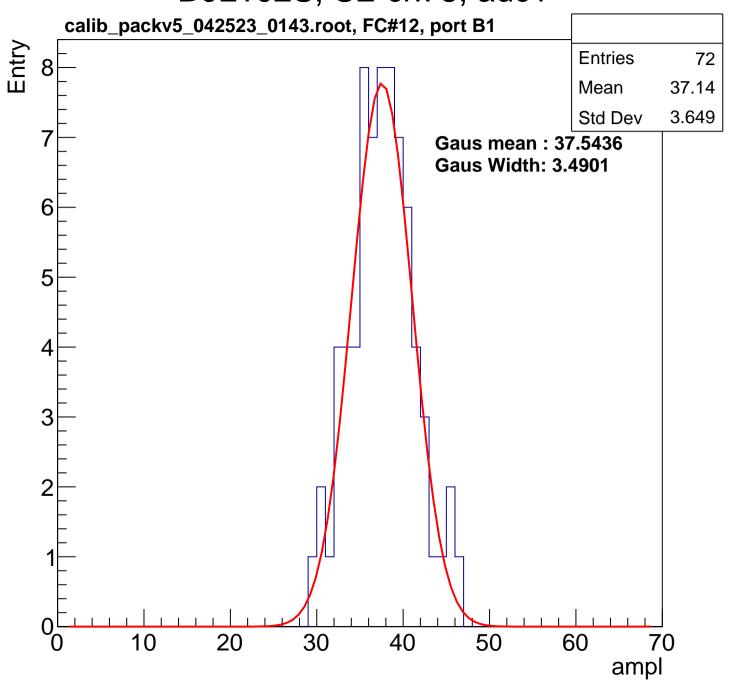


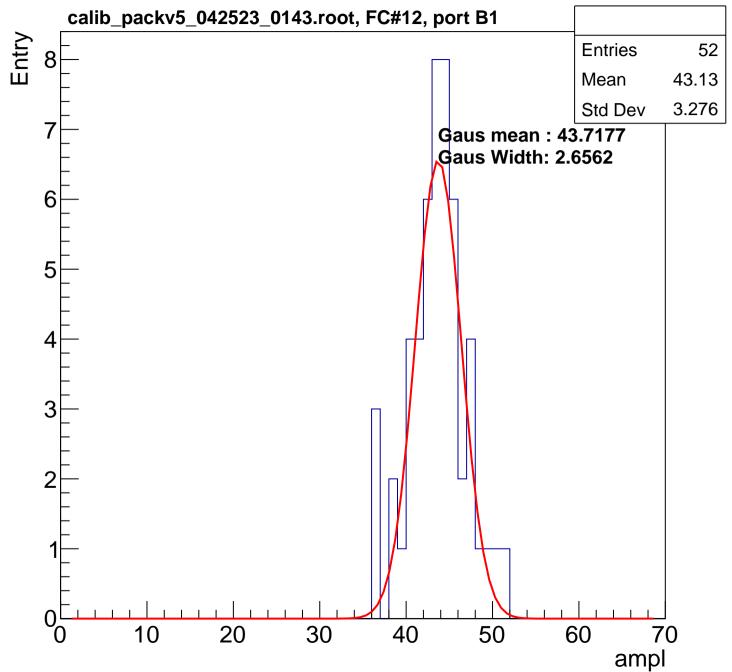


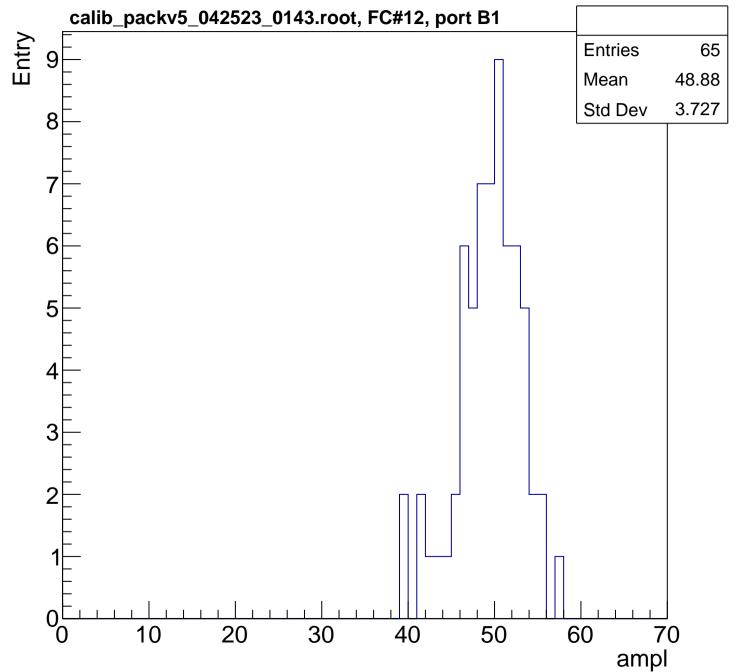


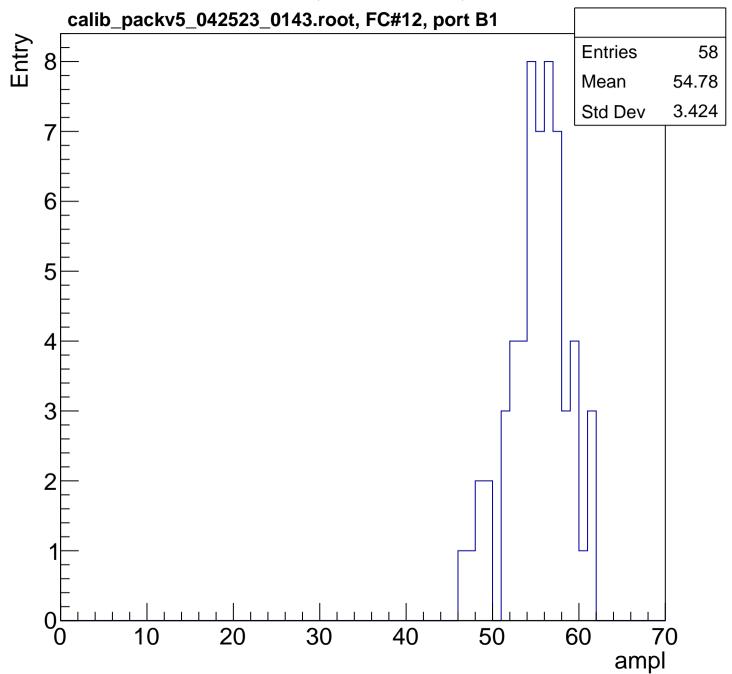


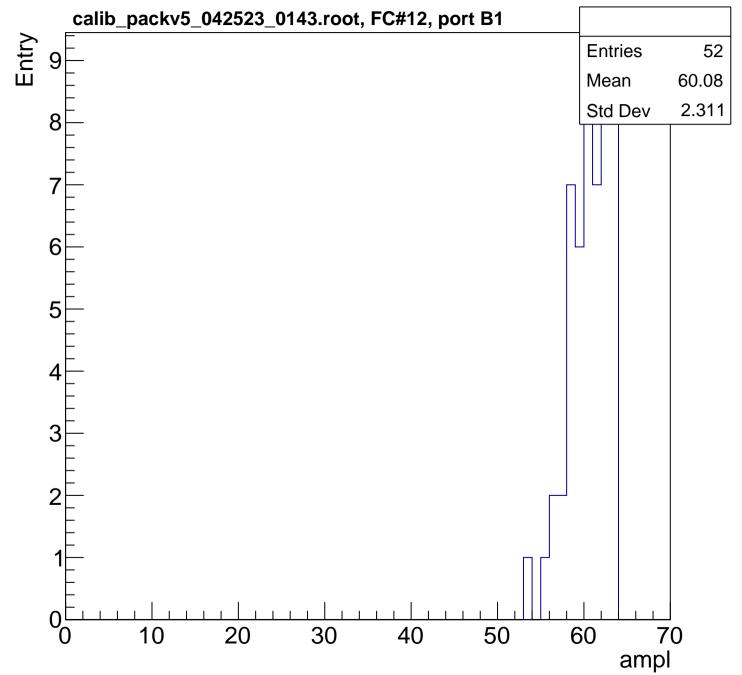


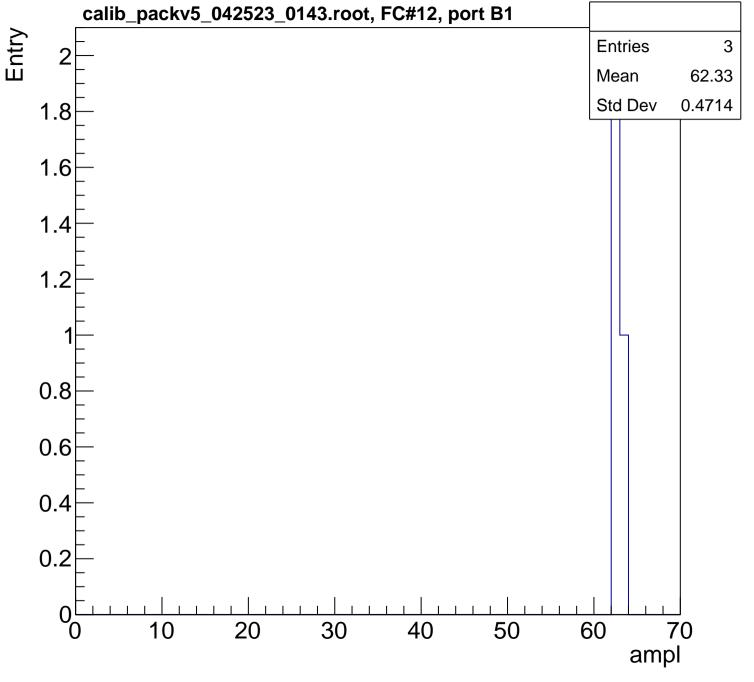




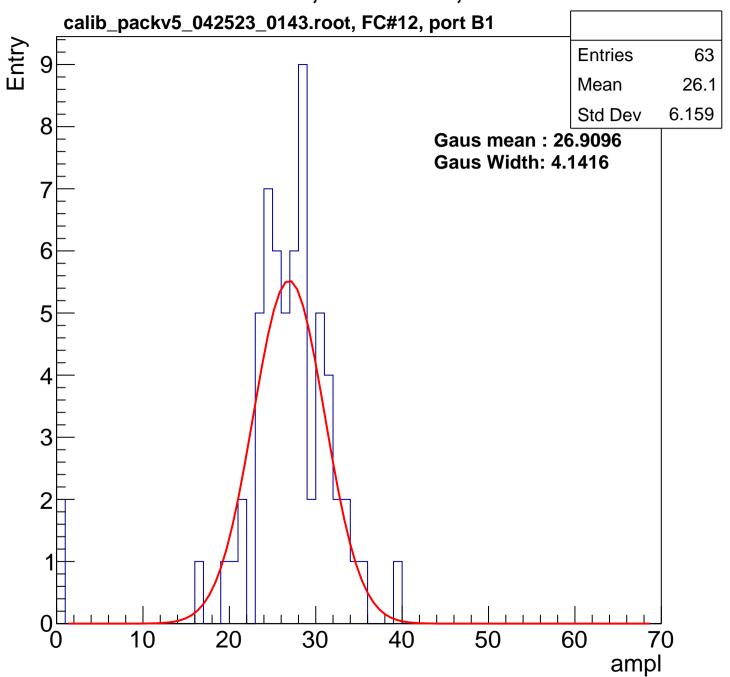


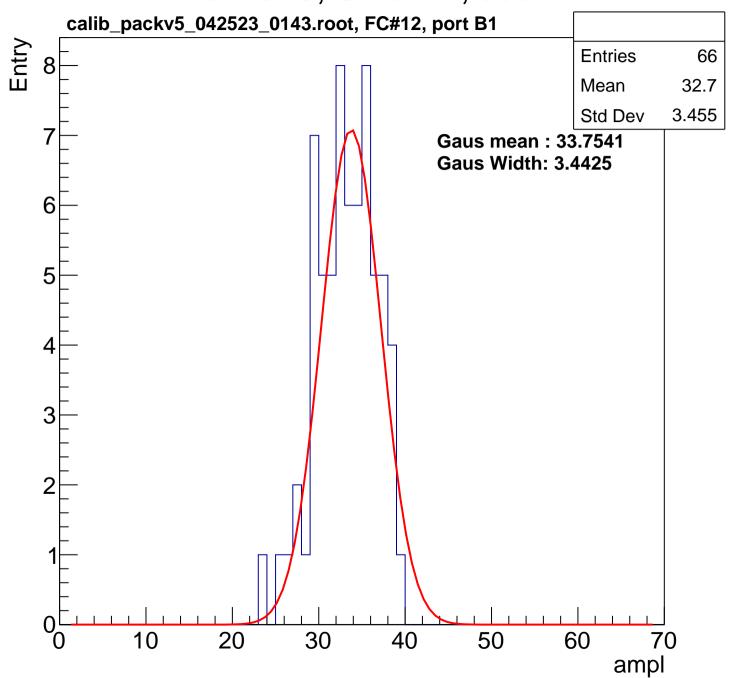


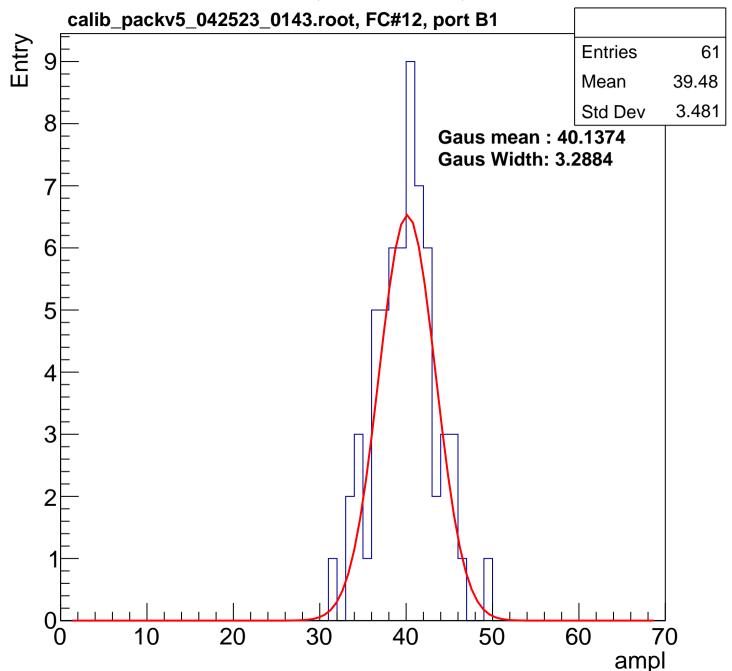


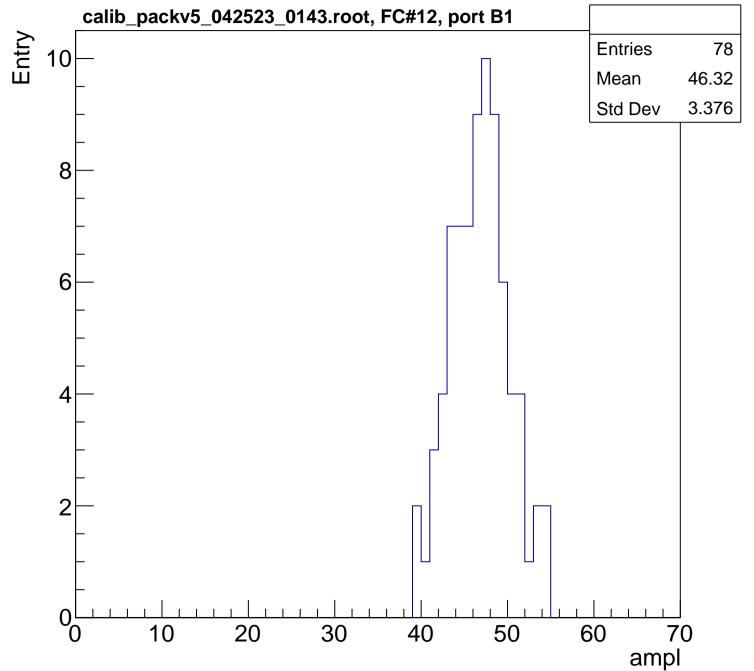


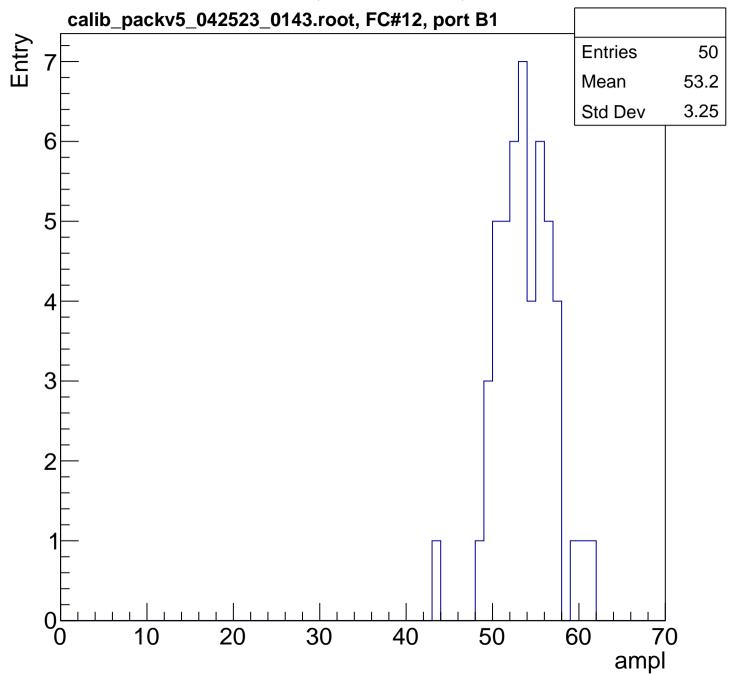
B0L102S, U2-ch73, adc7 calib_packv5_042523_0143.root, FC#12, port B1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

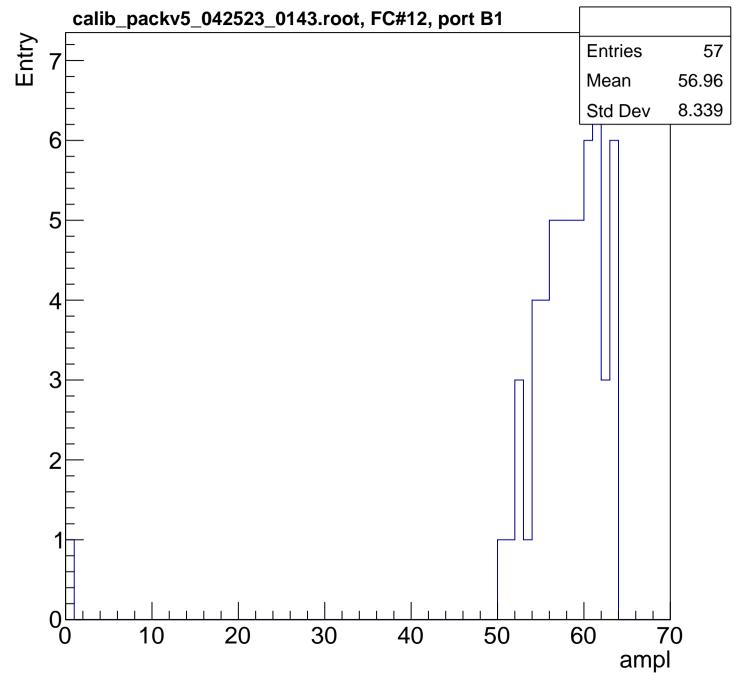


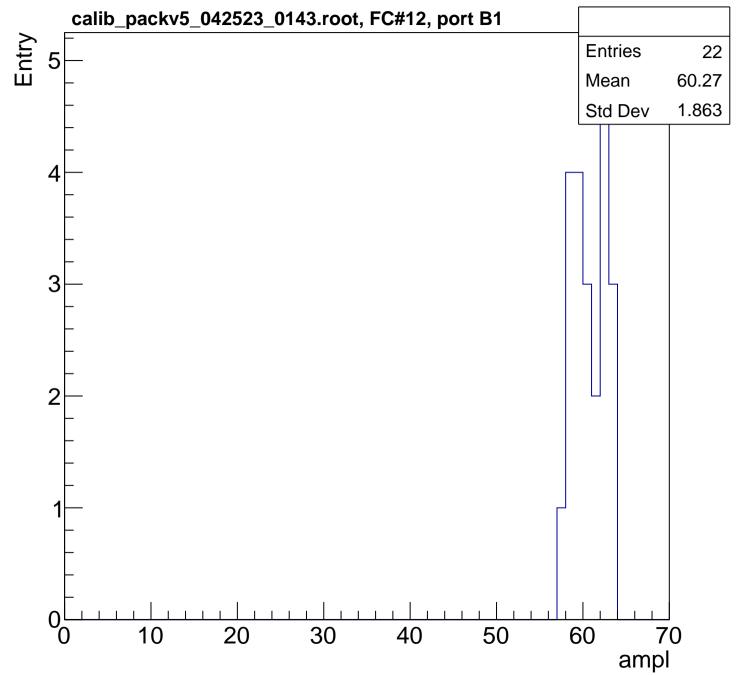


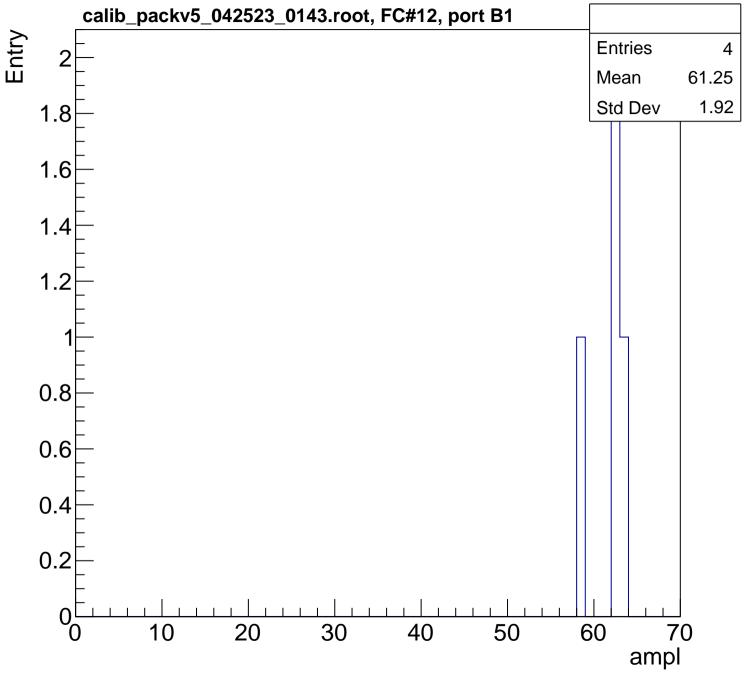


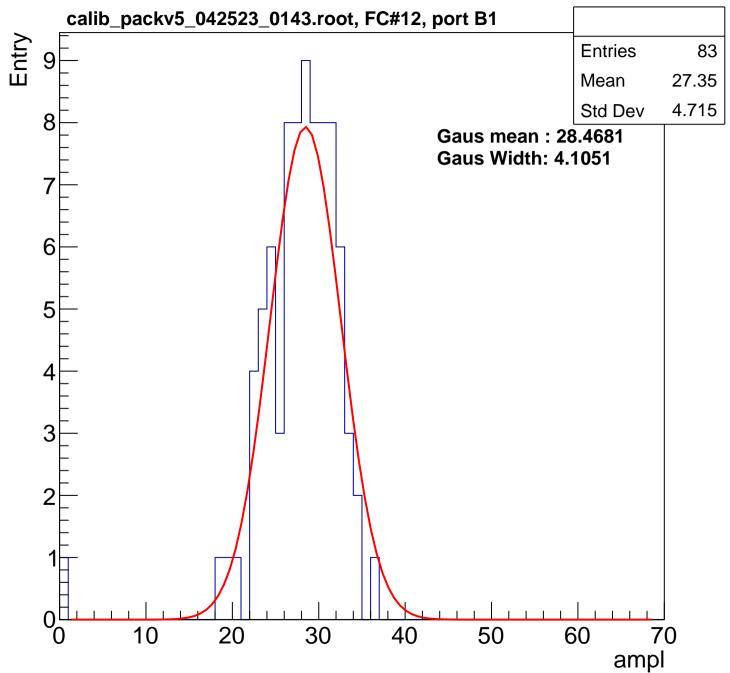


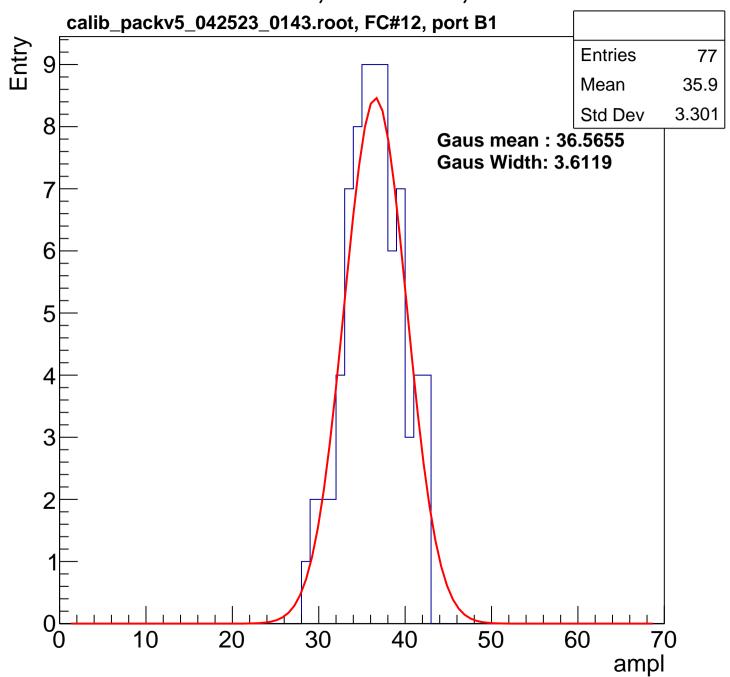


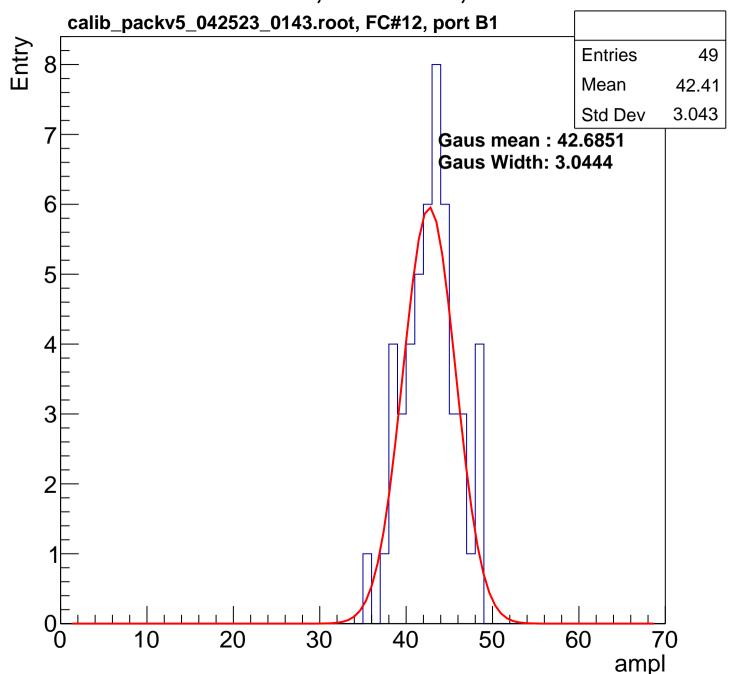


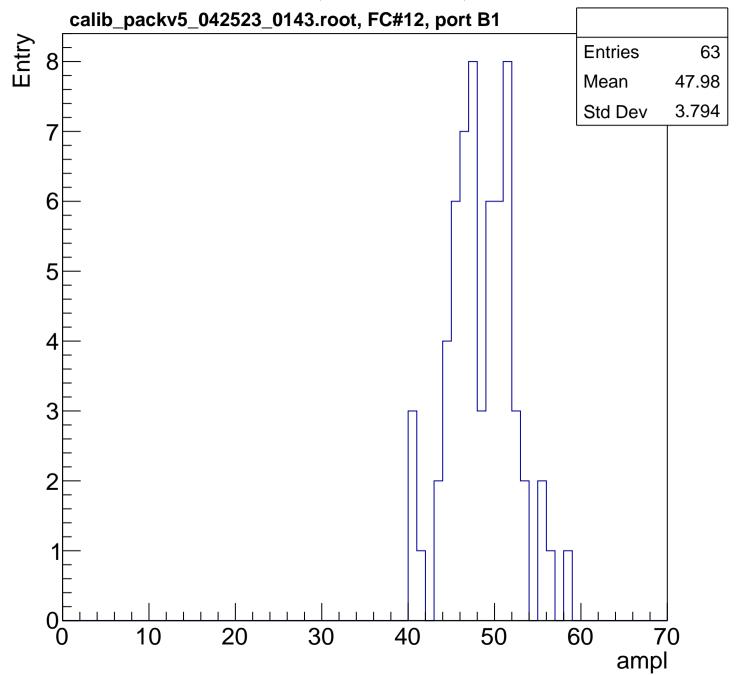


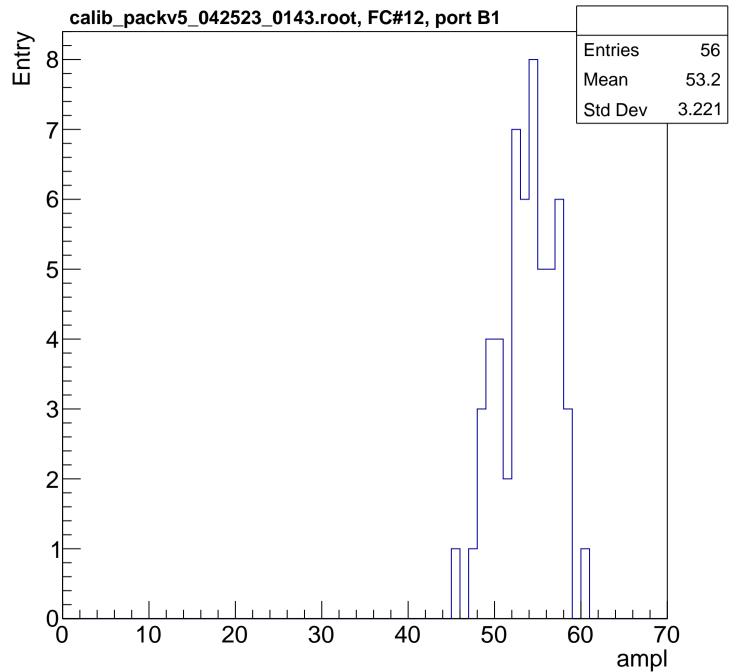


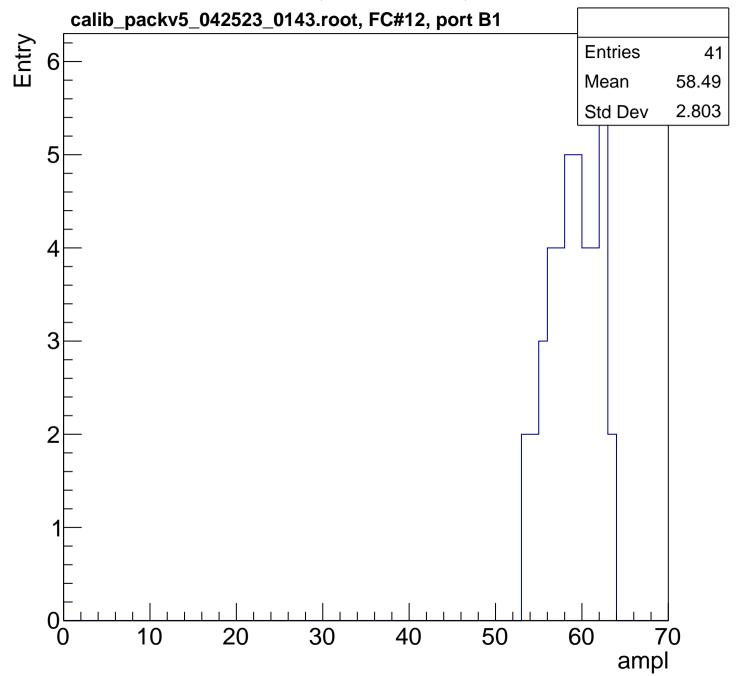


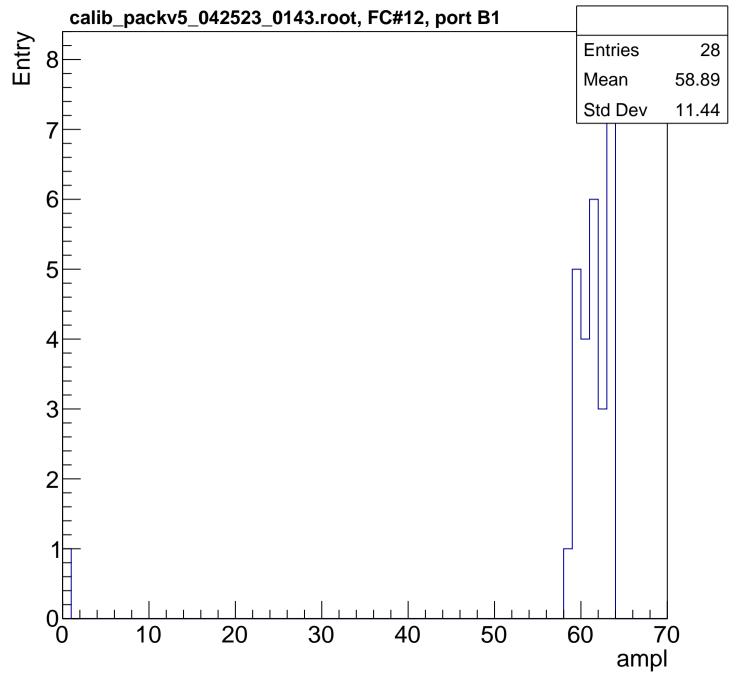


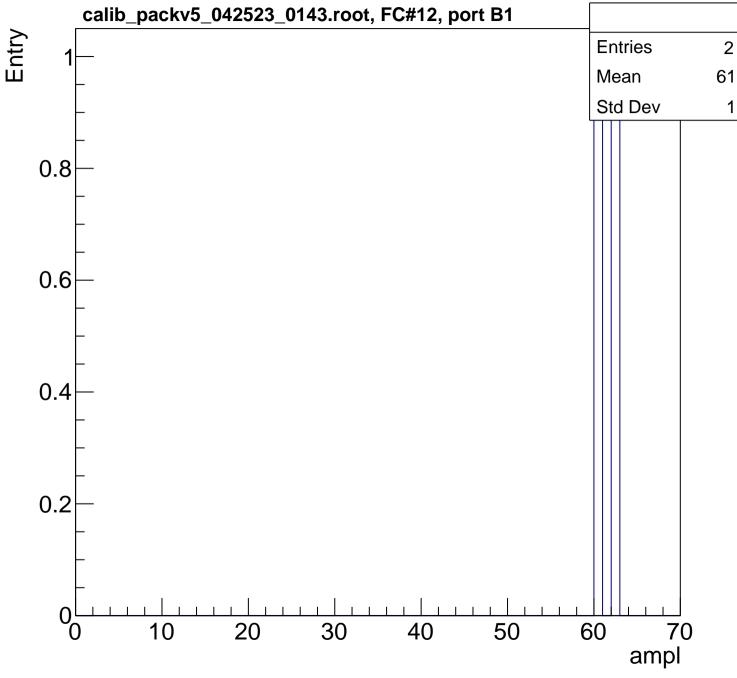


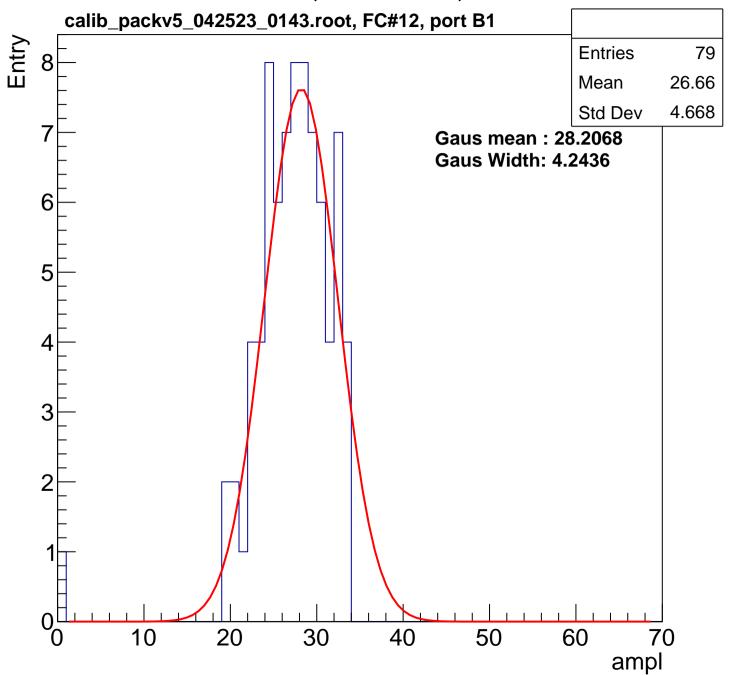


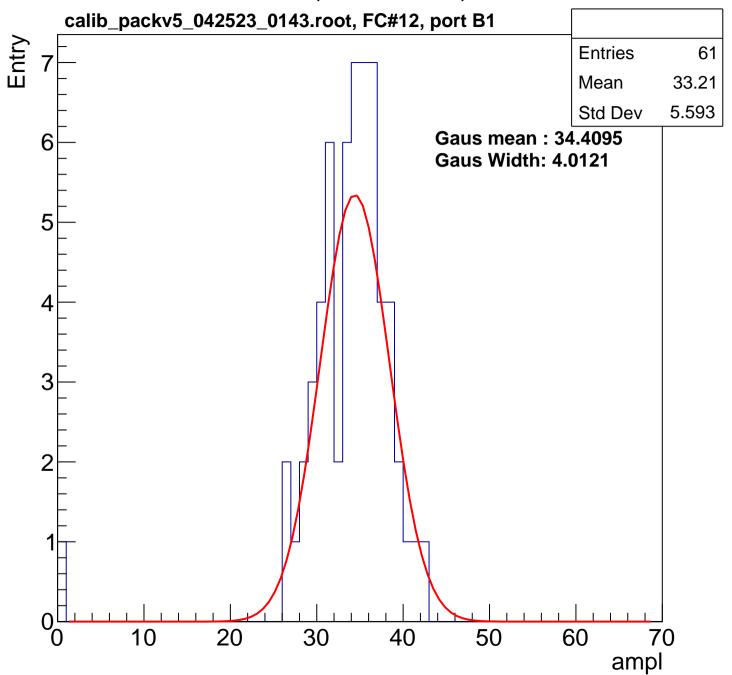


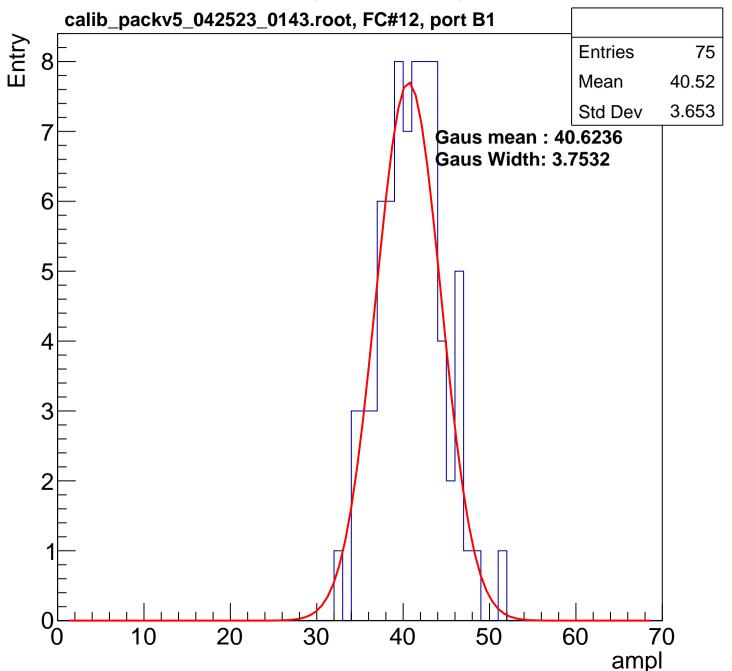


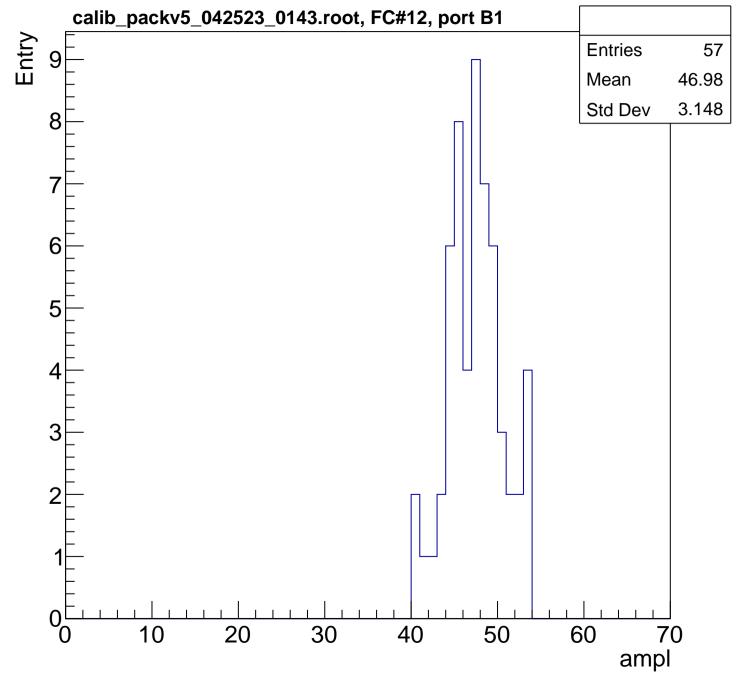


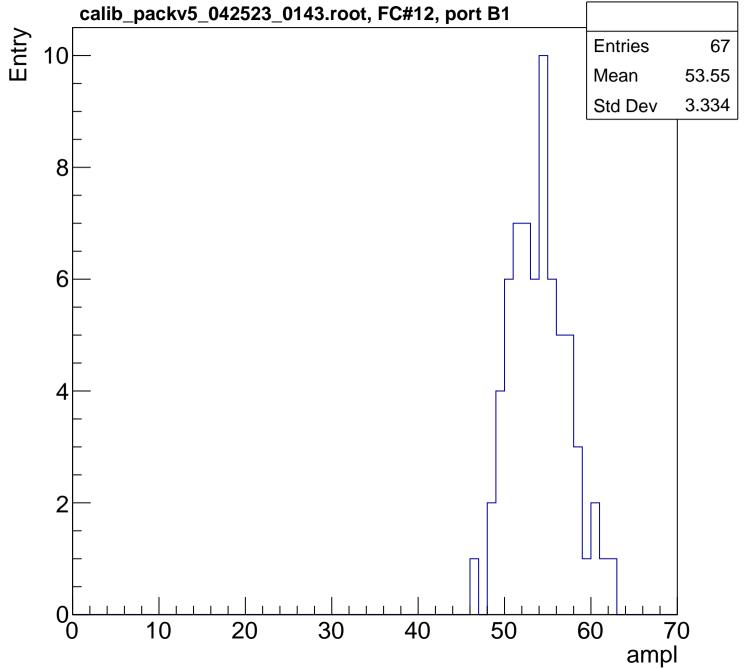


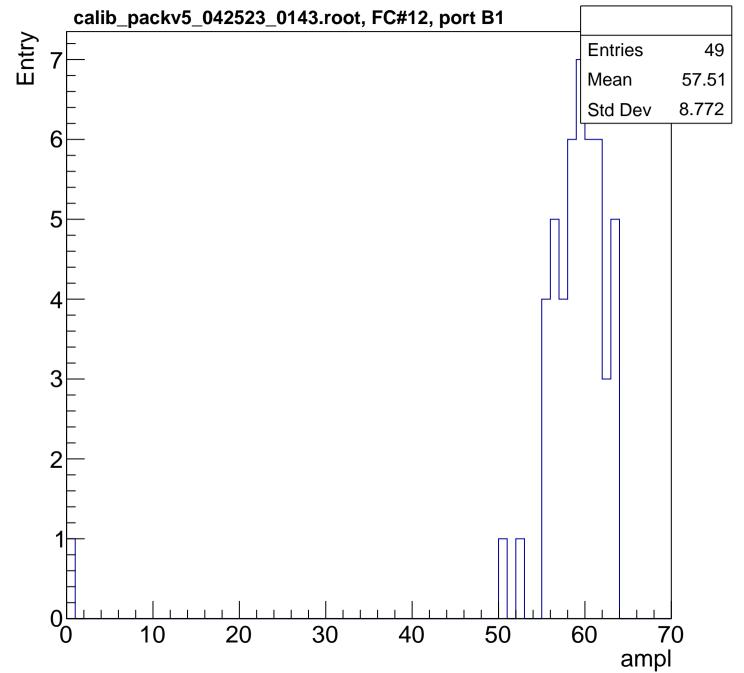


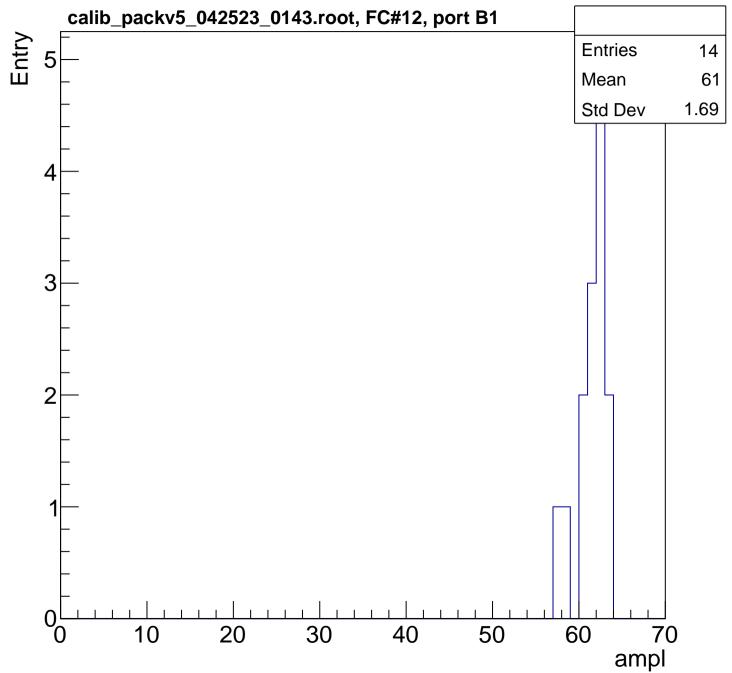


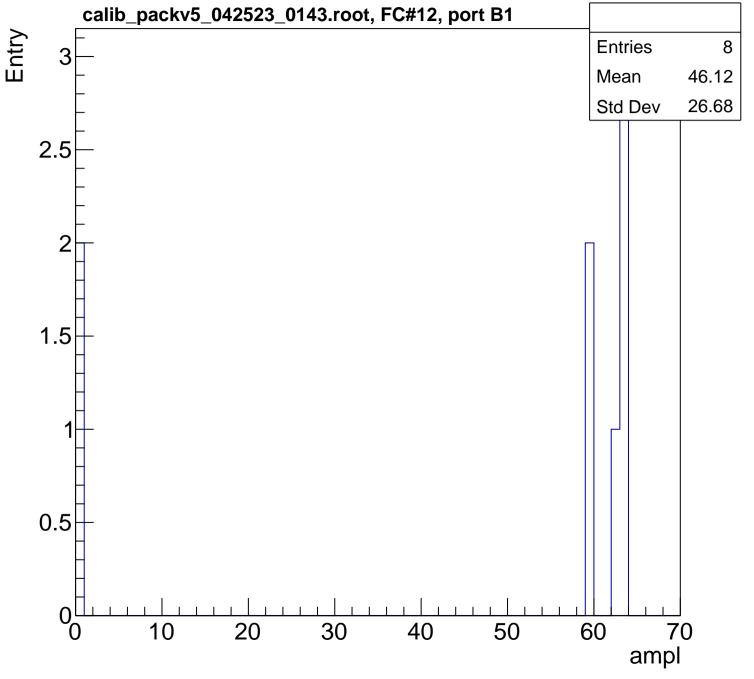


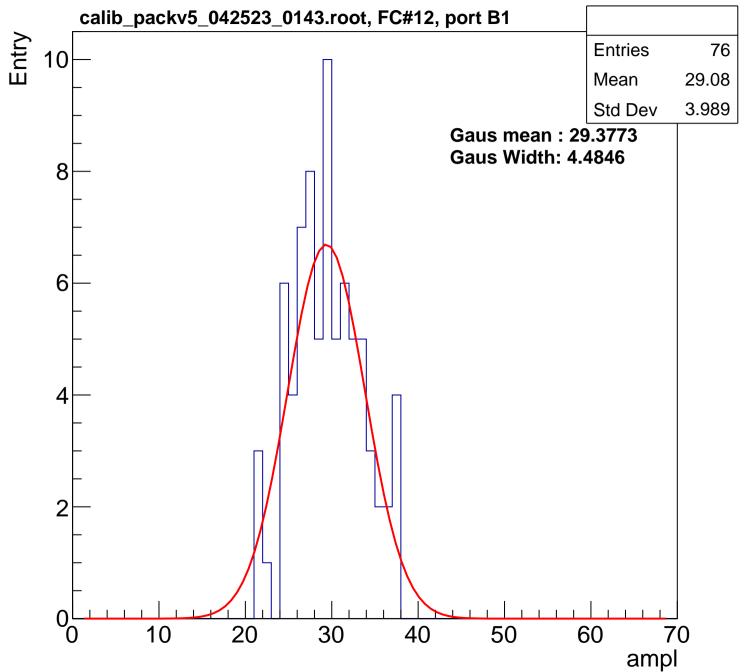


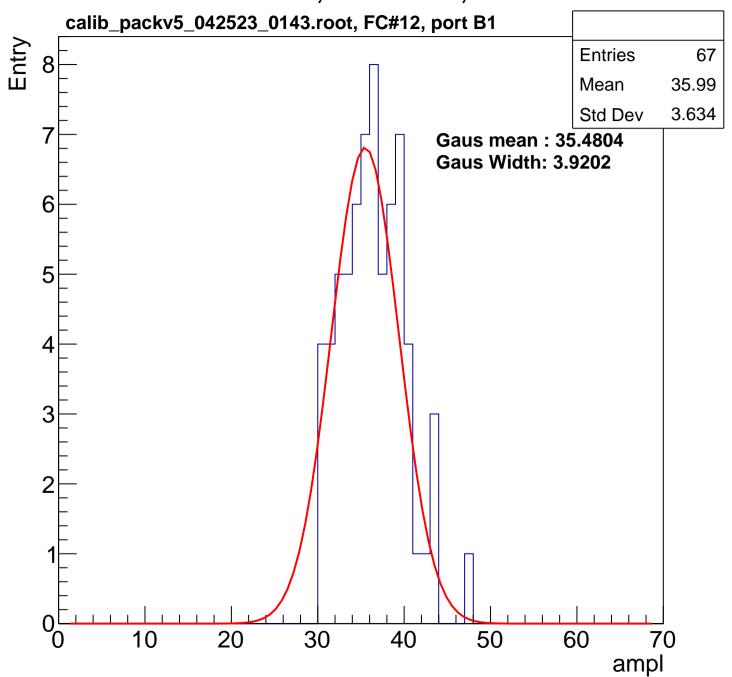


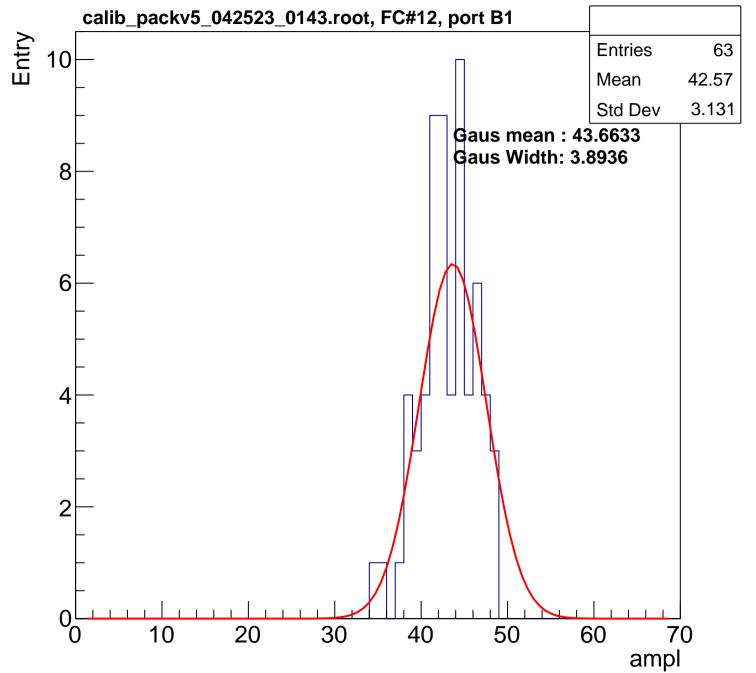


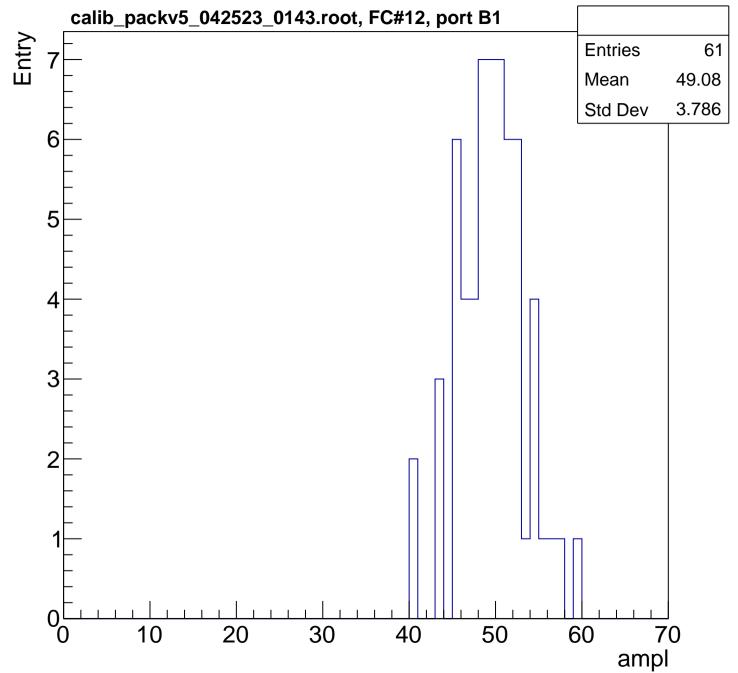


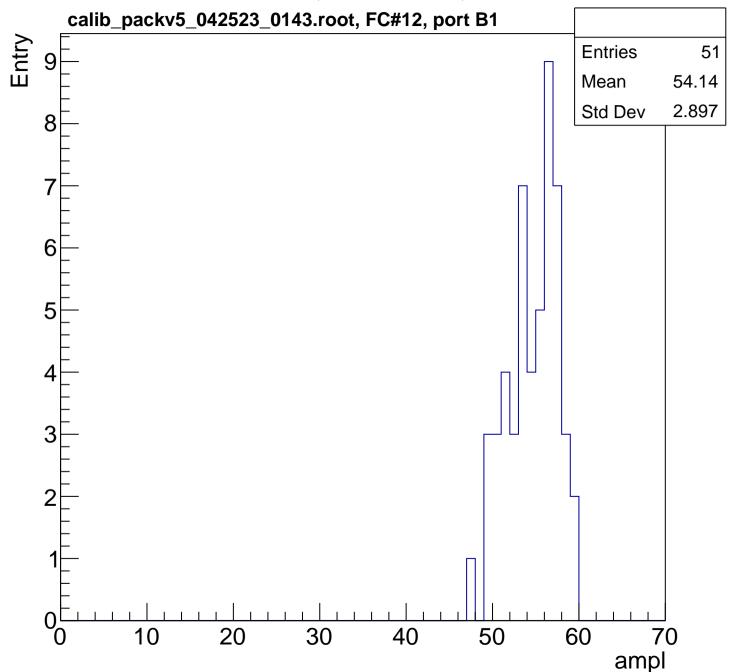


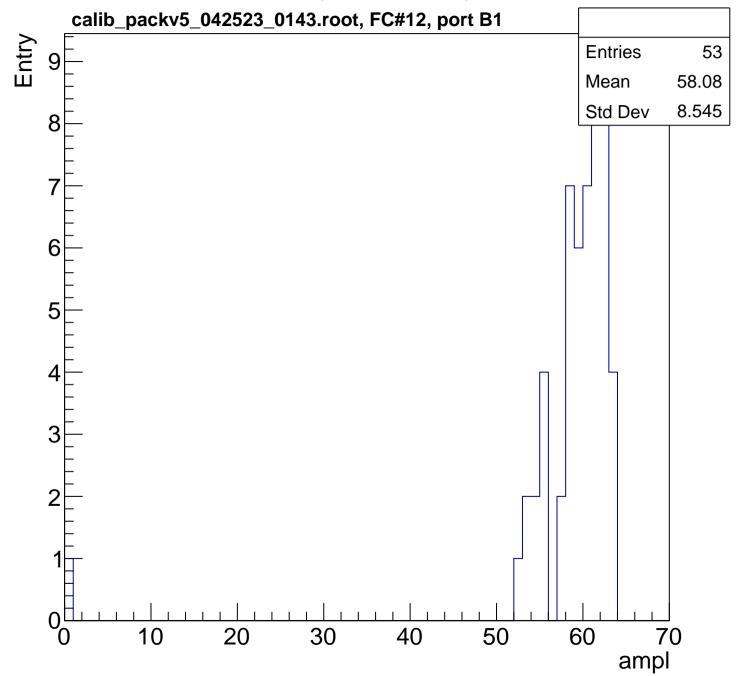


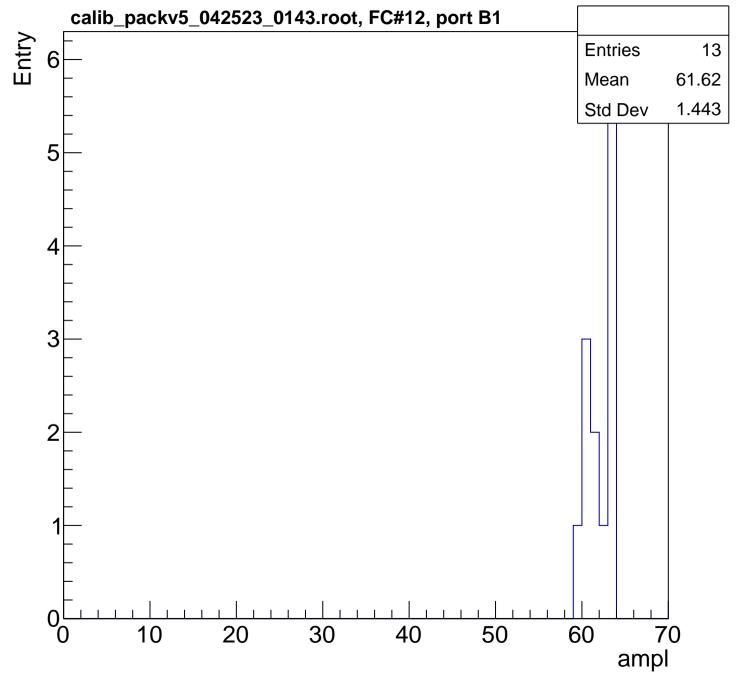


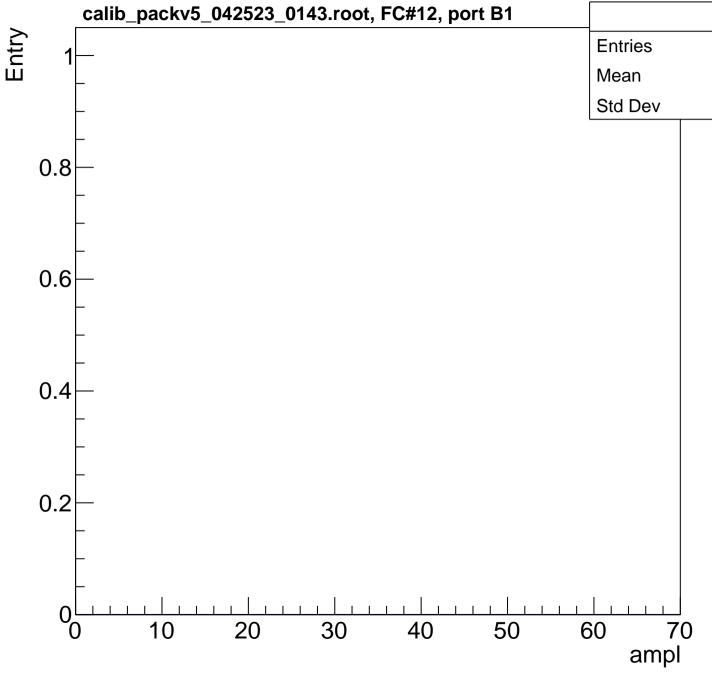


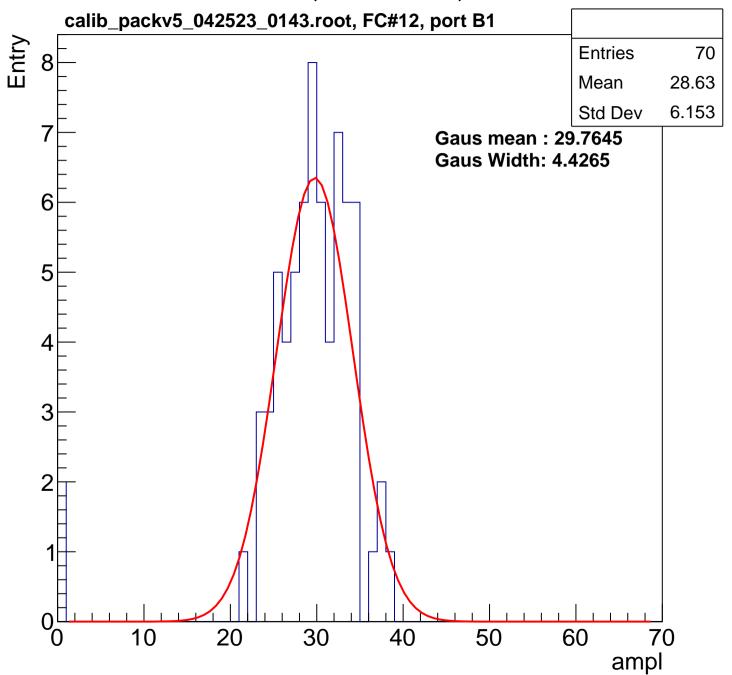


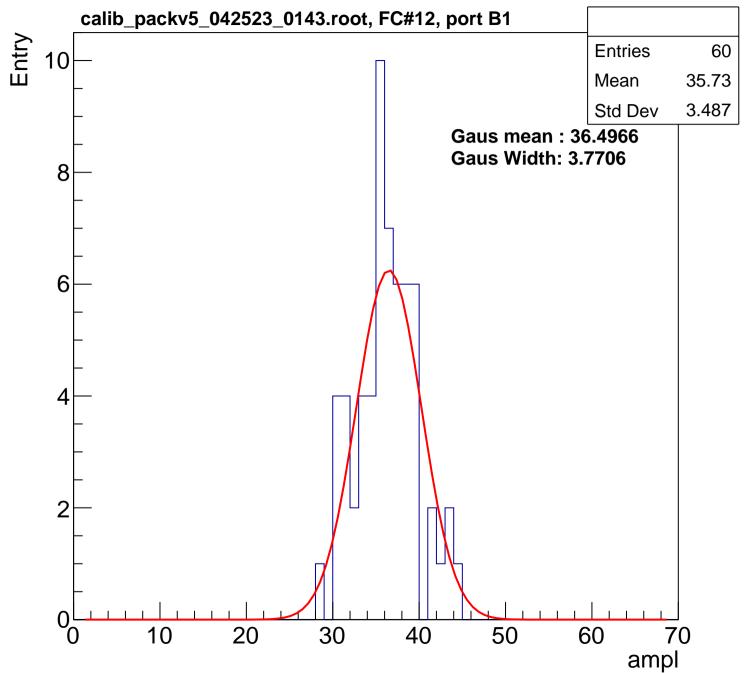


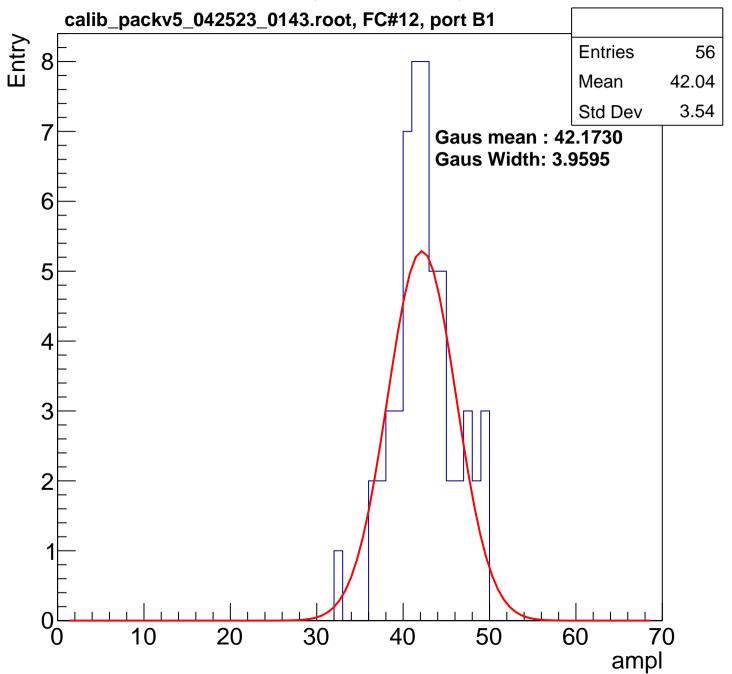


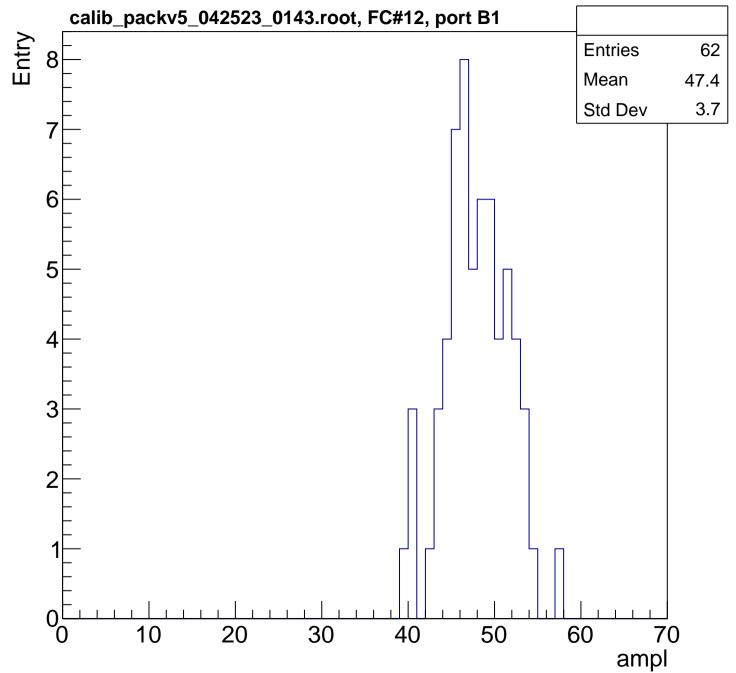


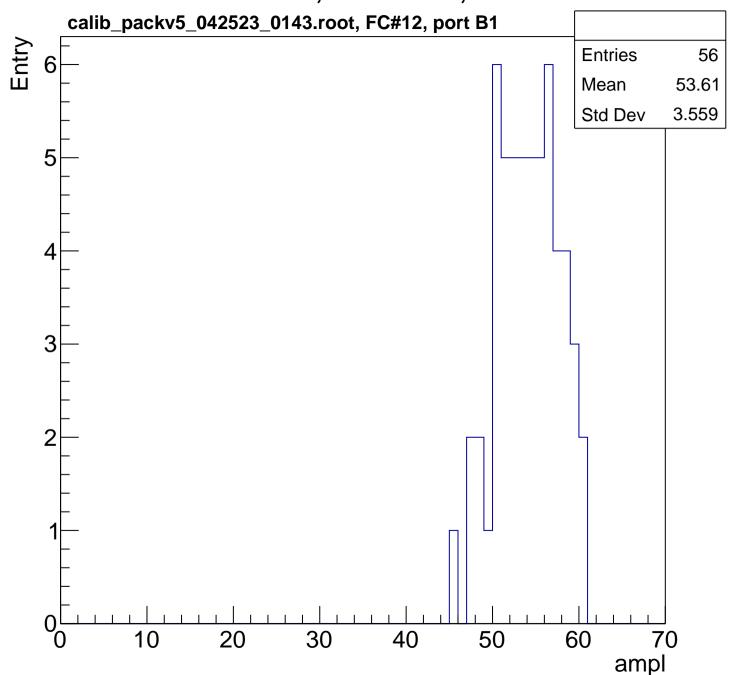


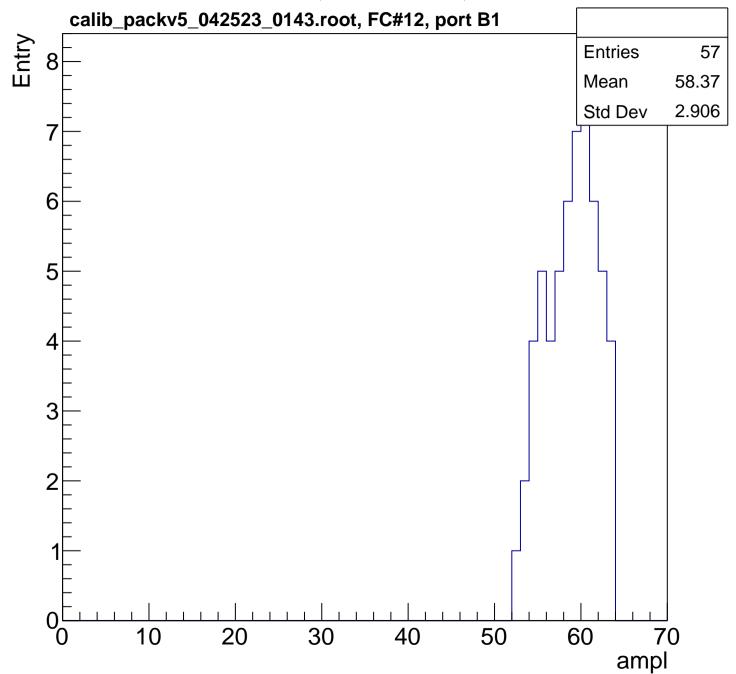


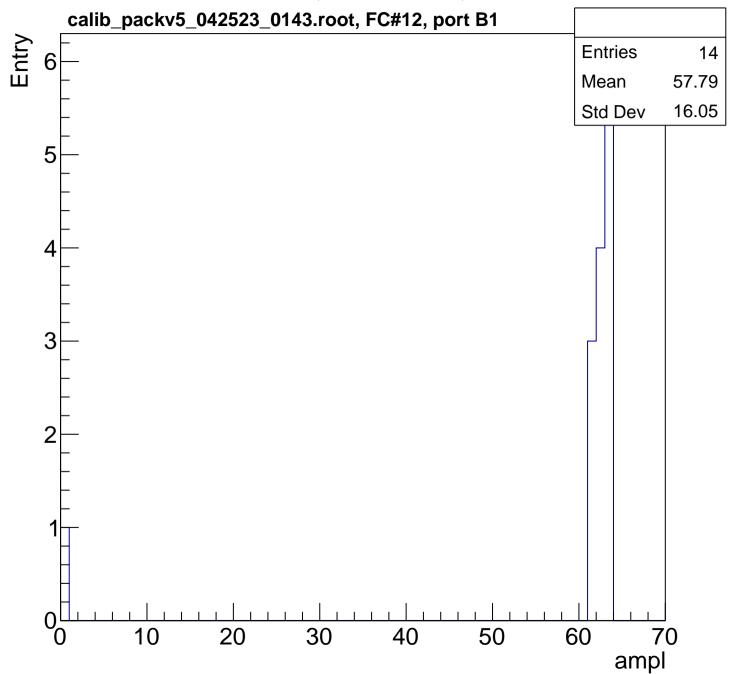




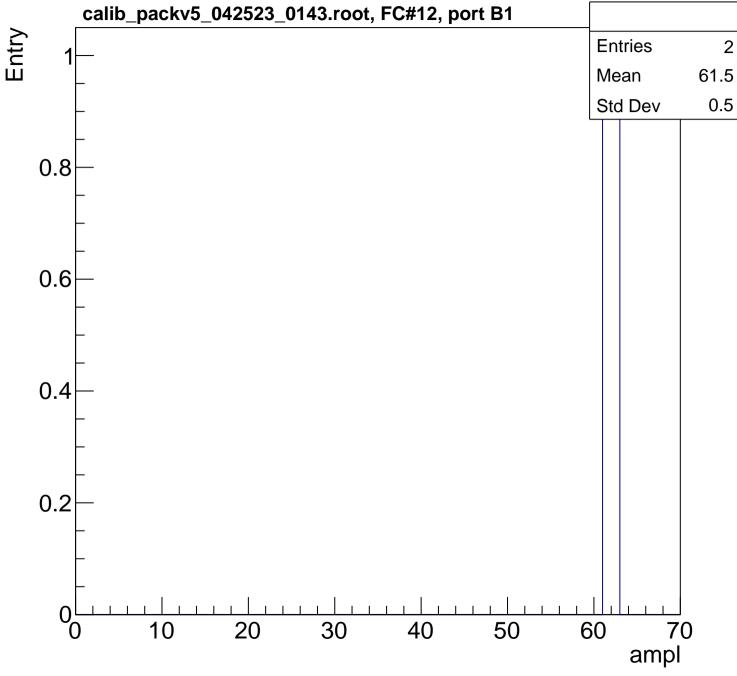


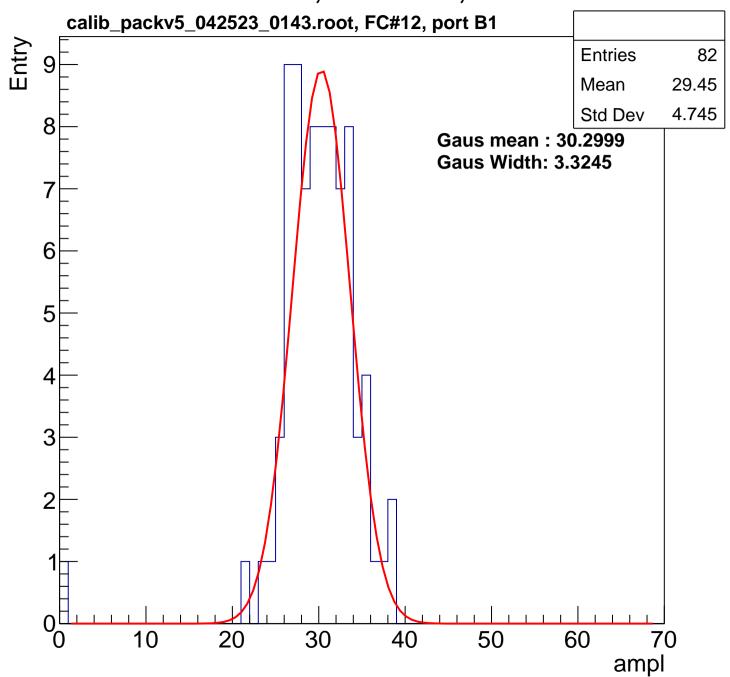


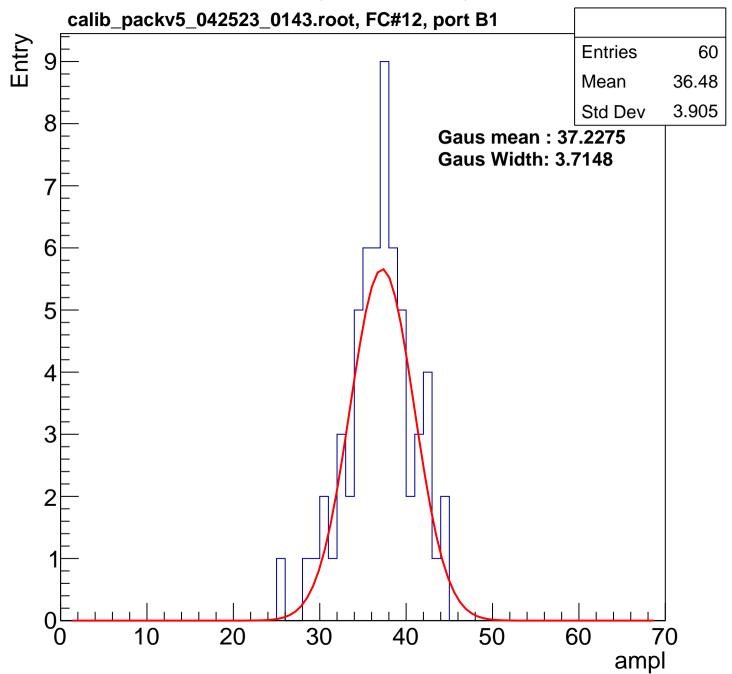


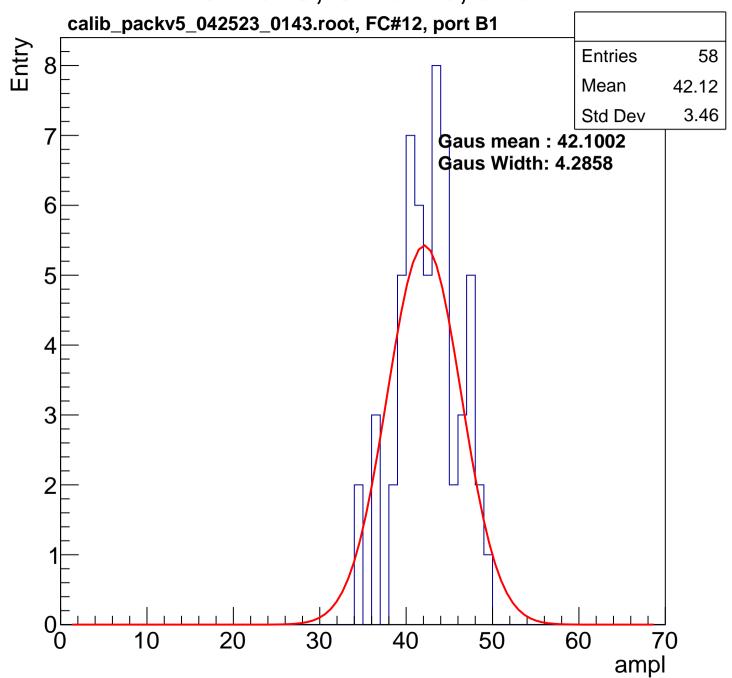


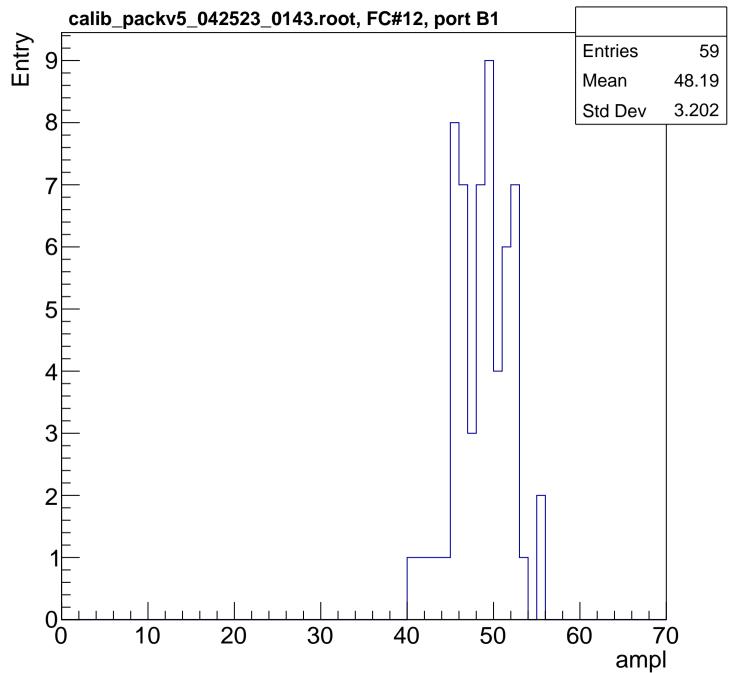
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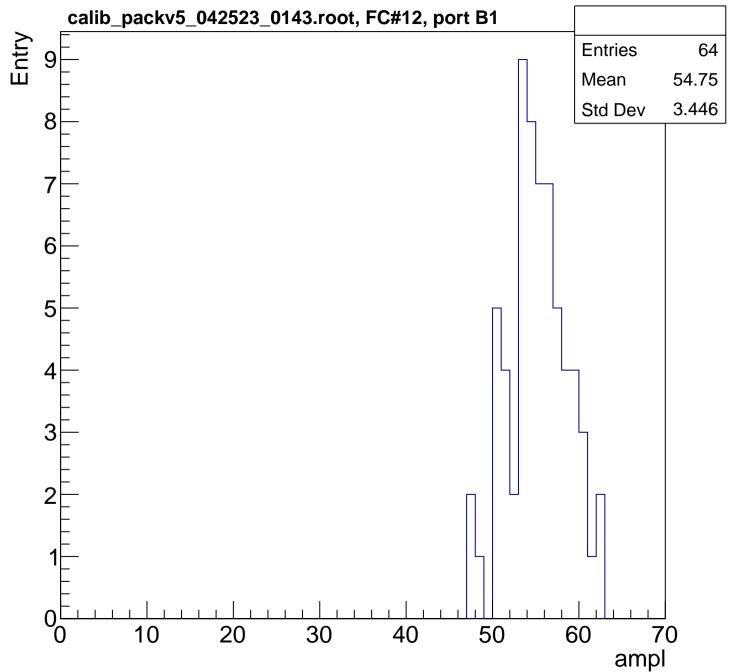


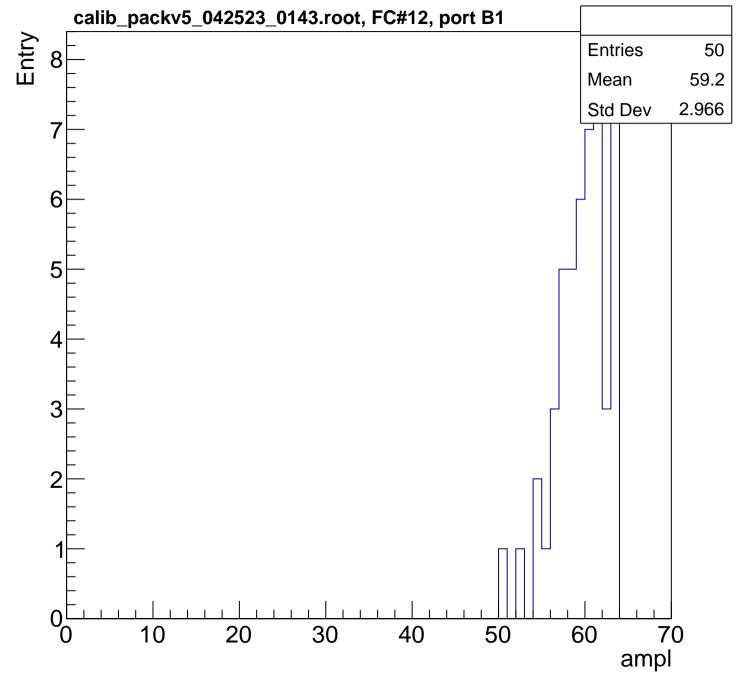


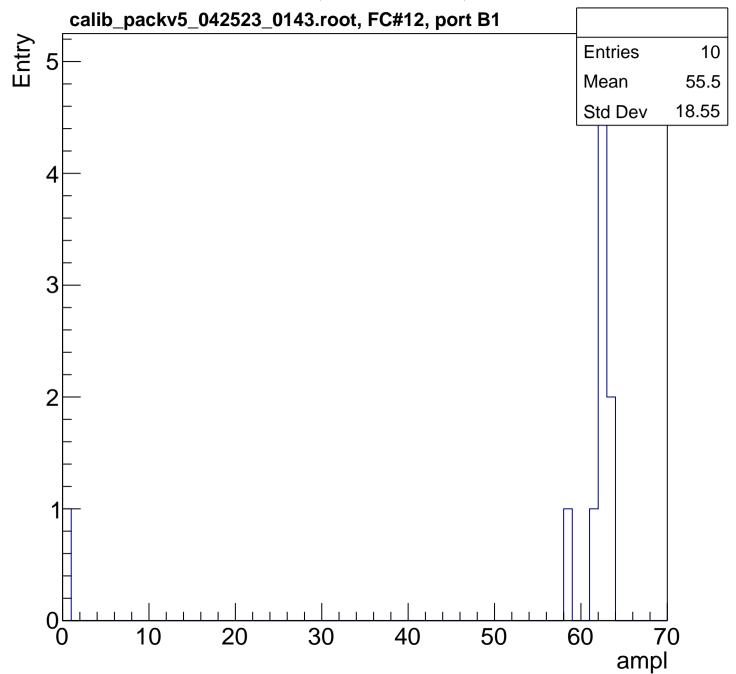




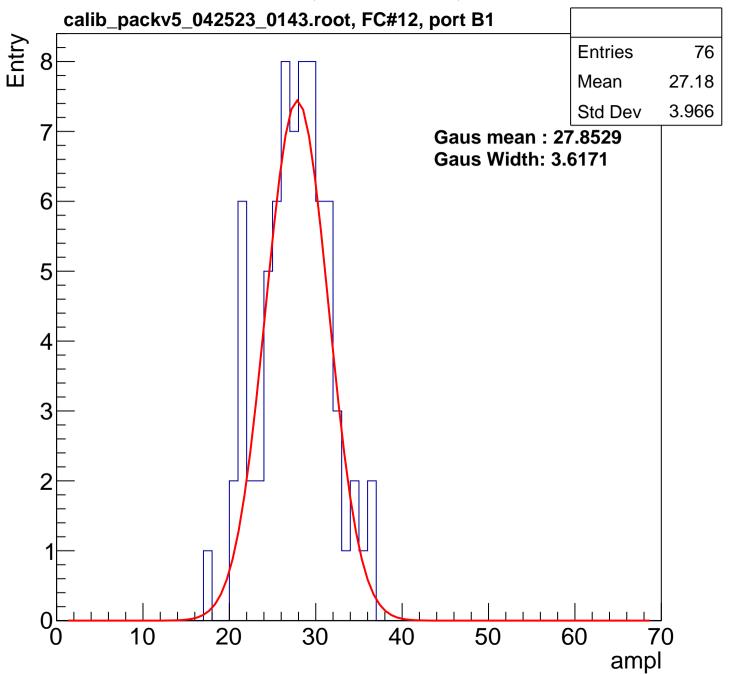


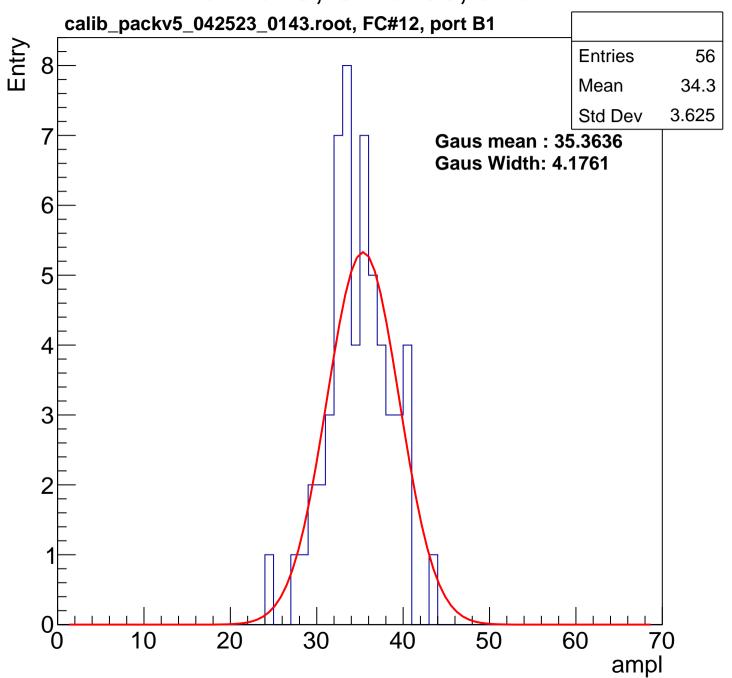


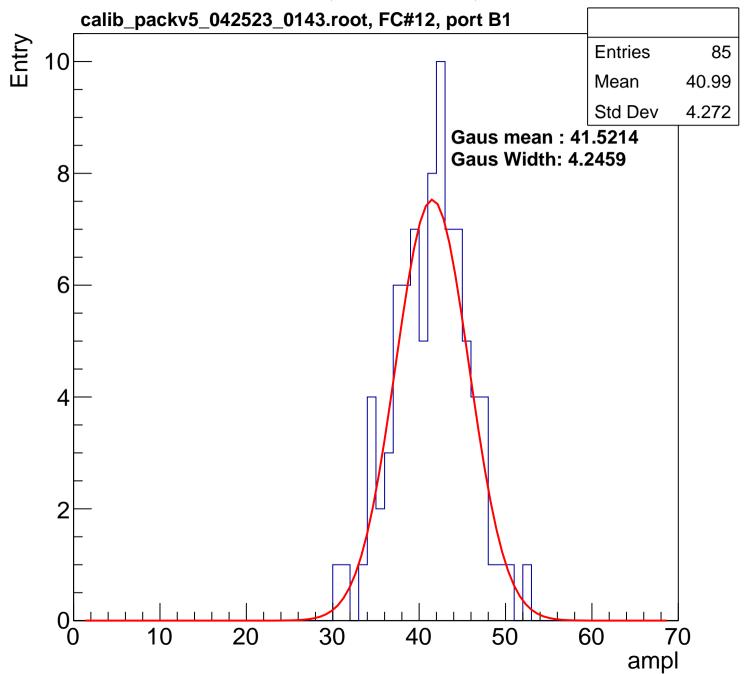


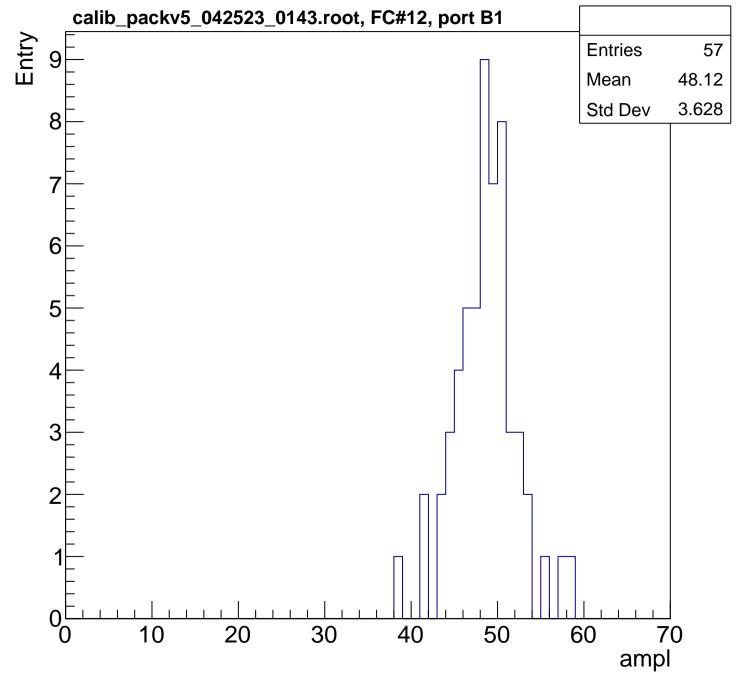


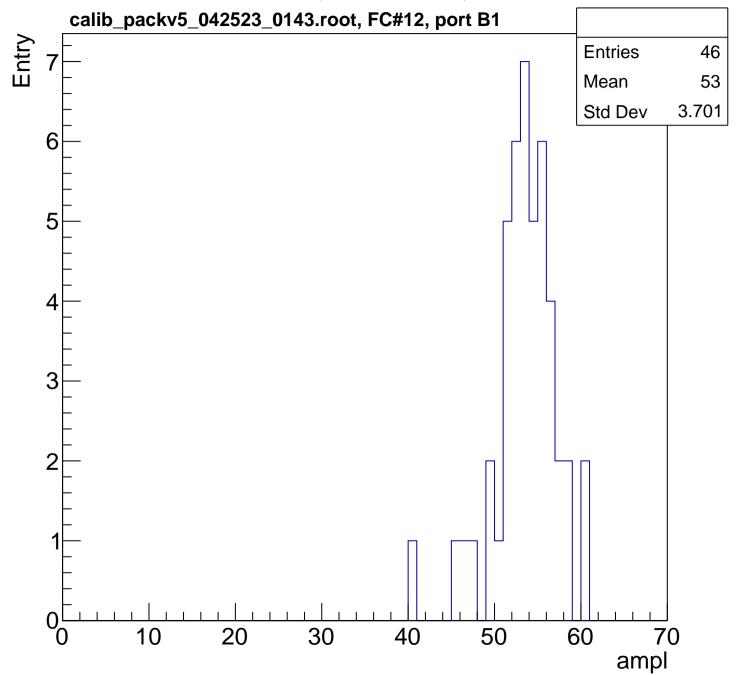


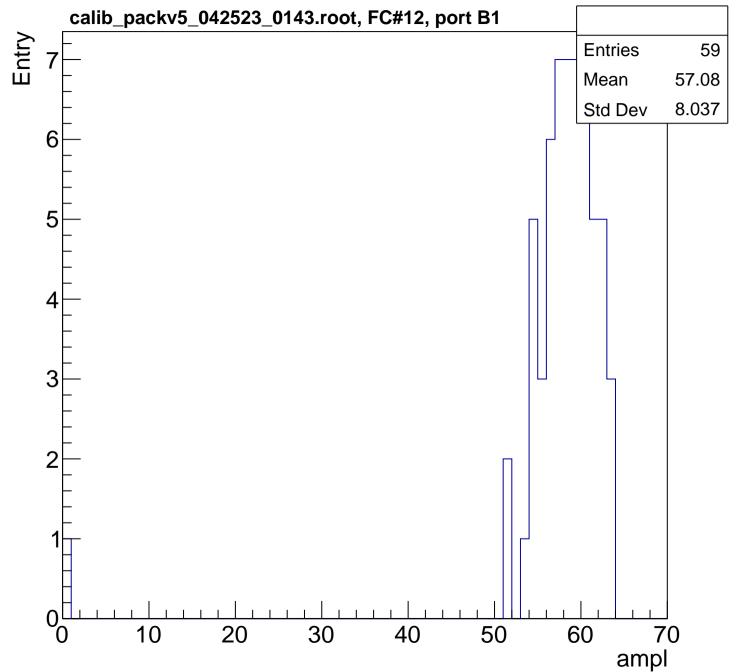


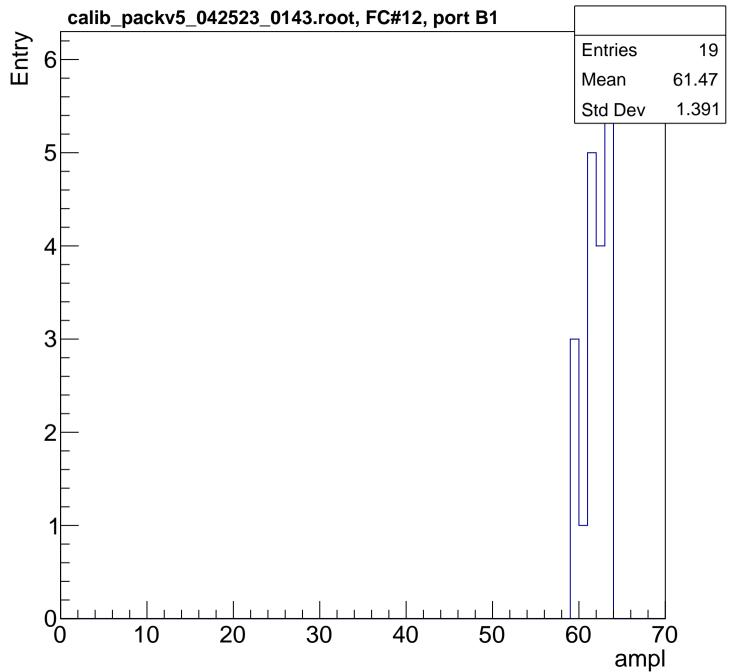




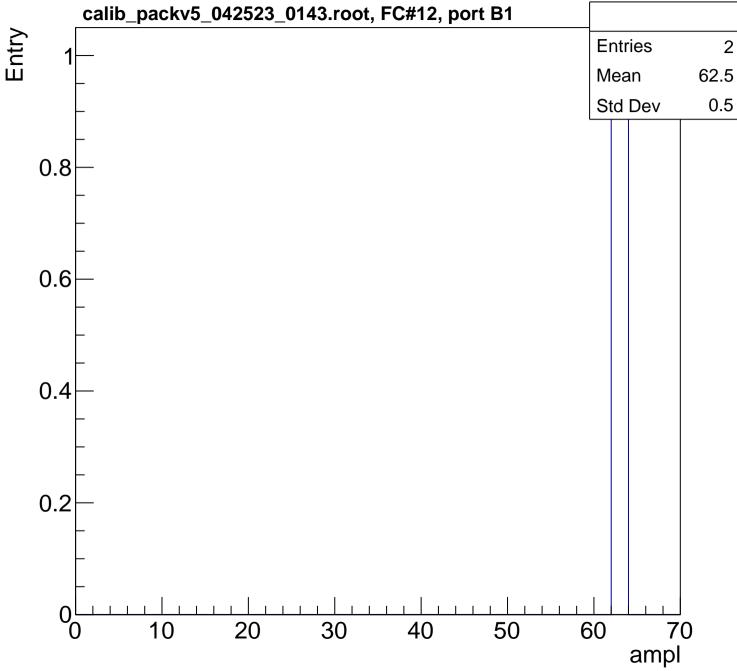


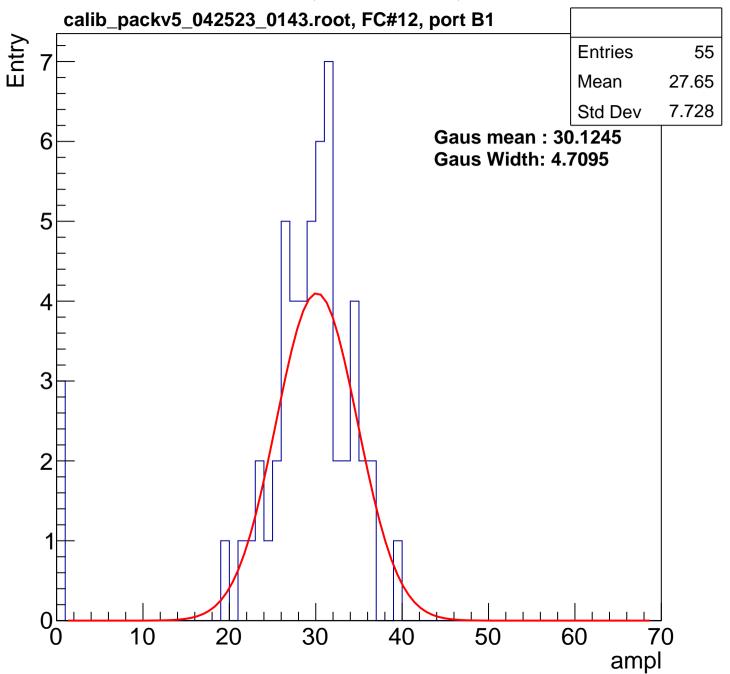


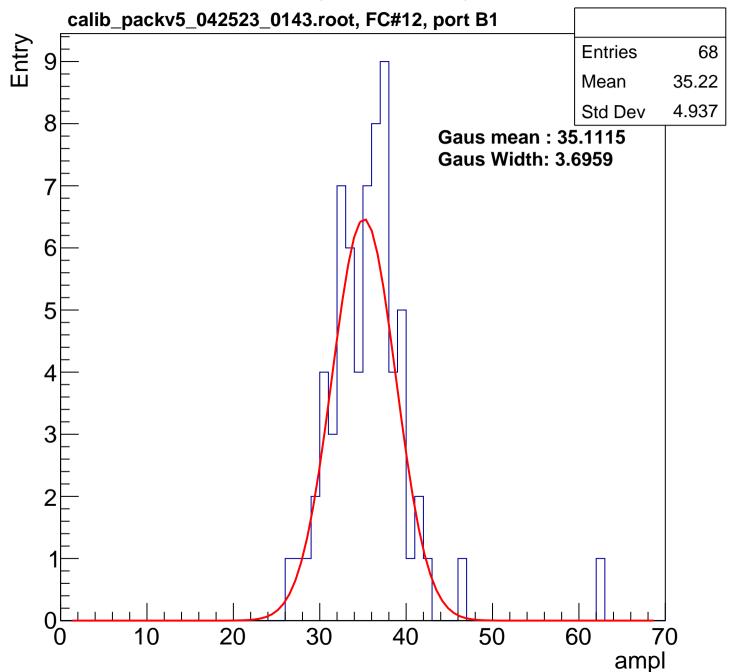


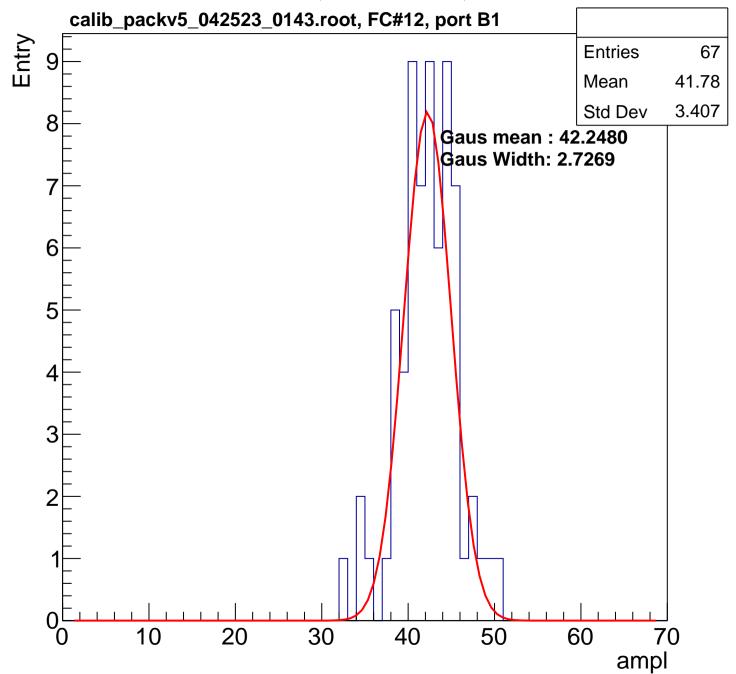


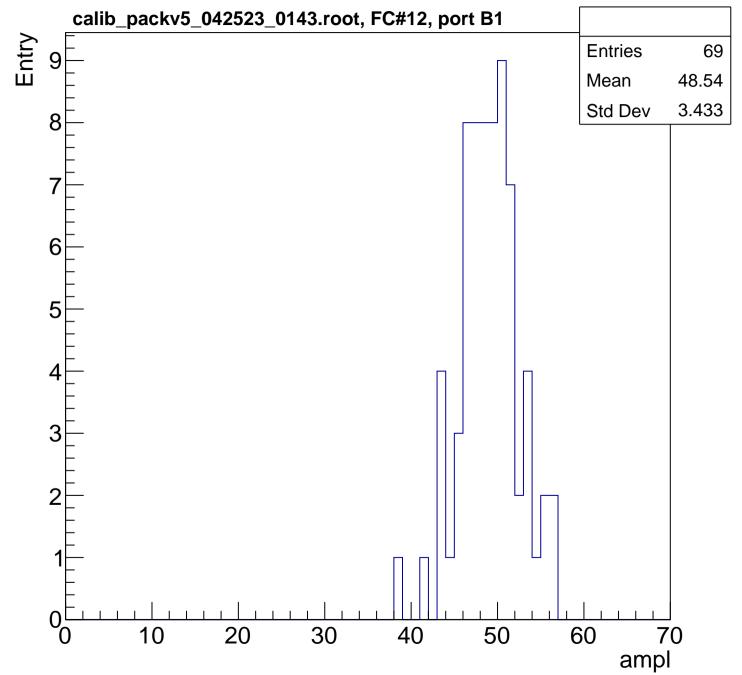
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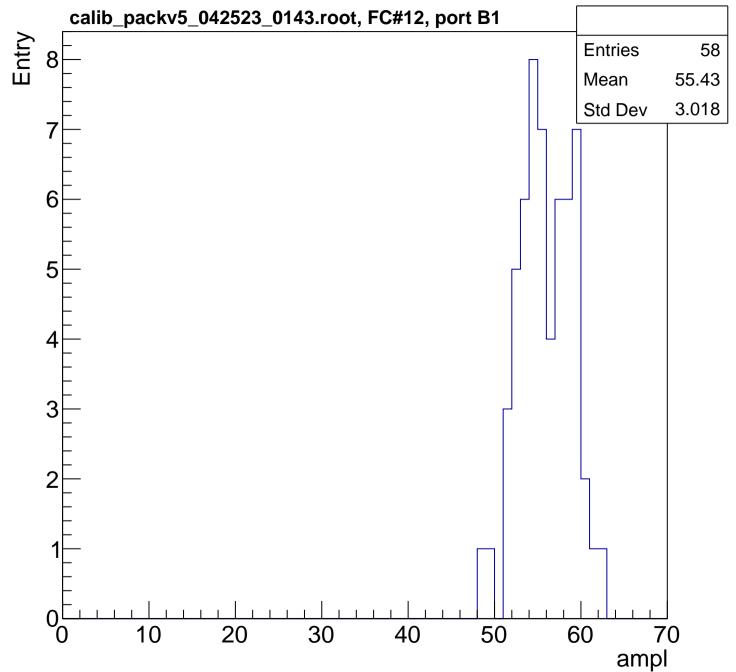


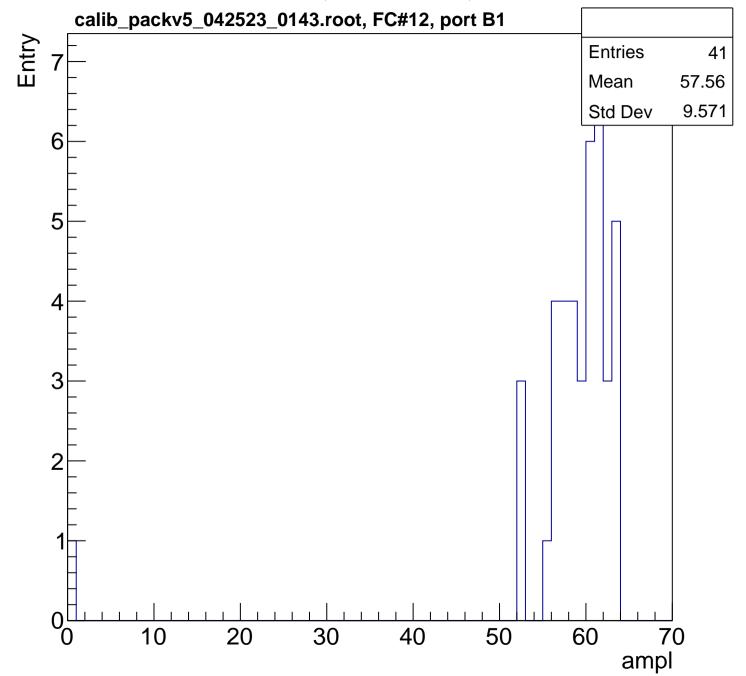


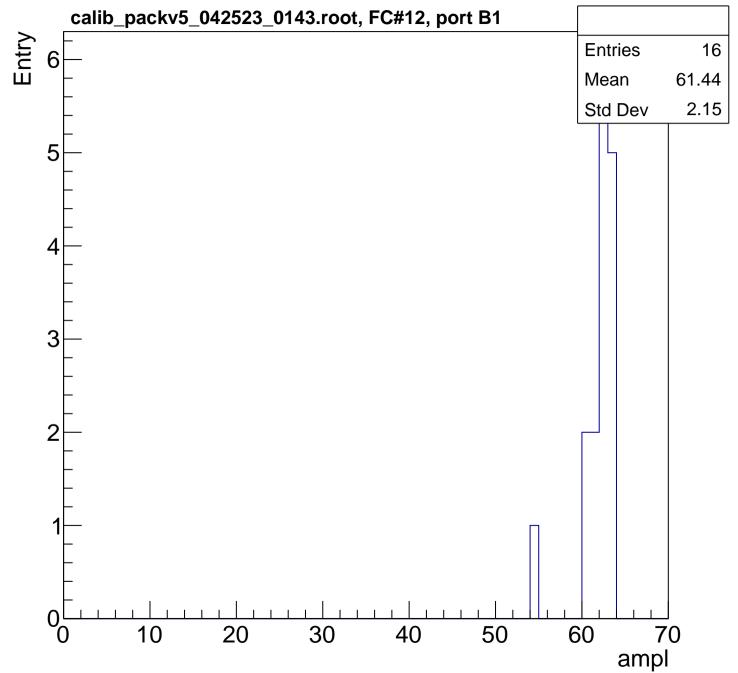


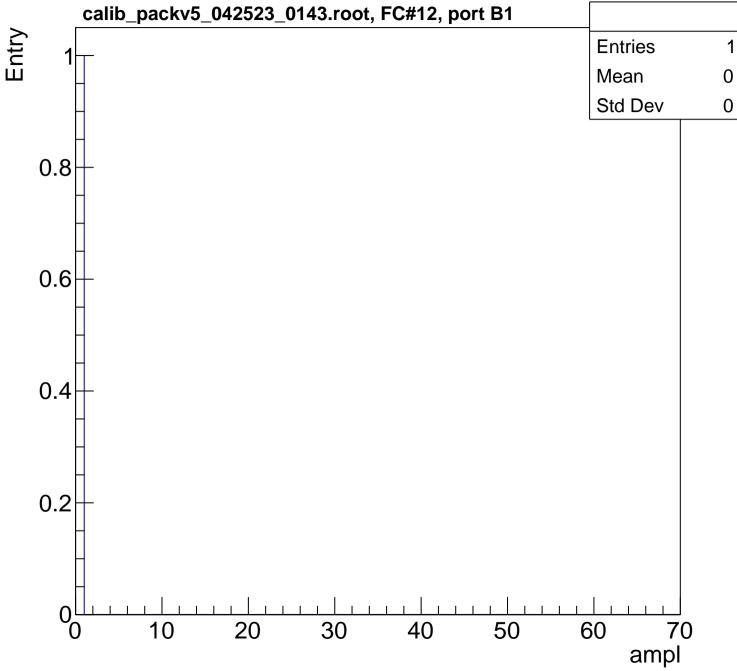


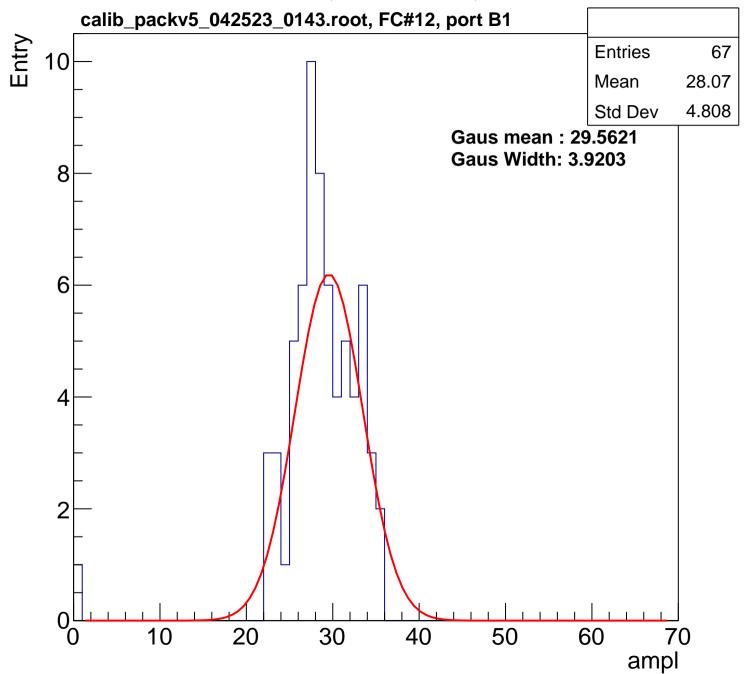


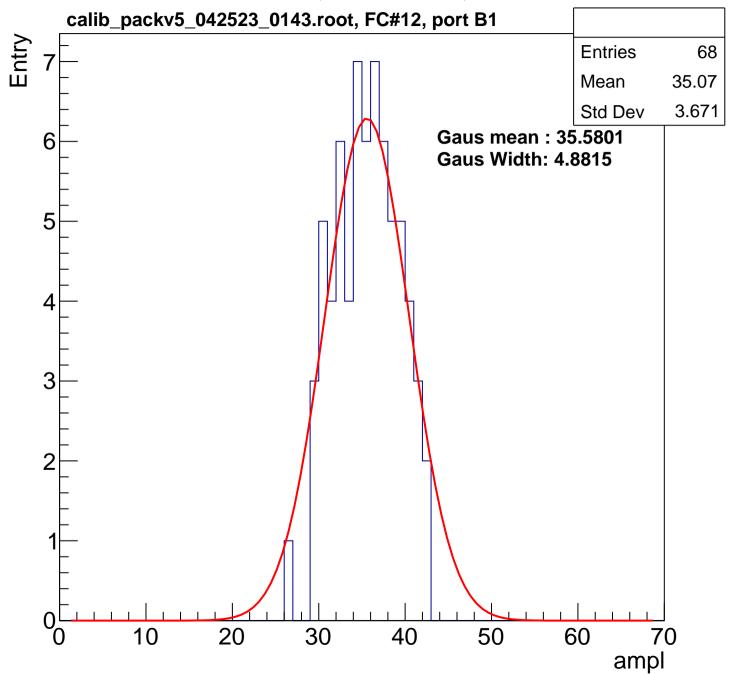


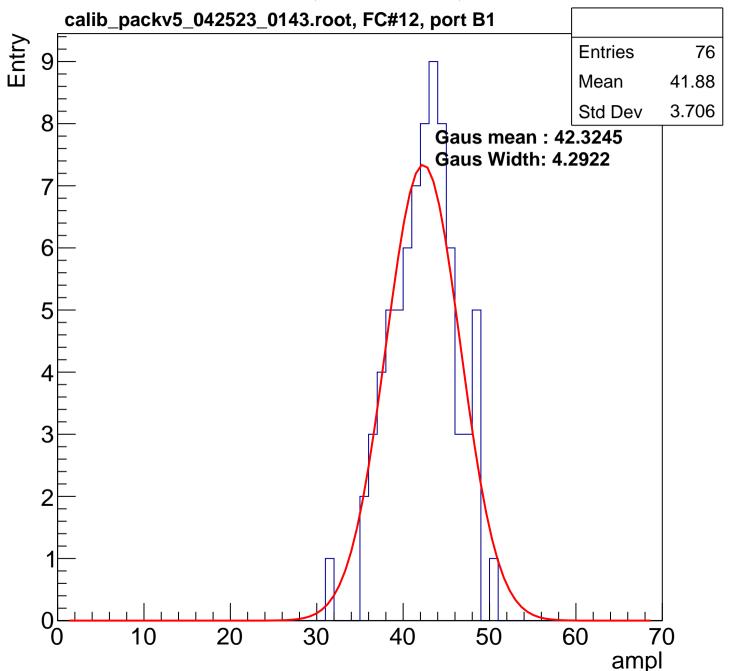


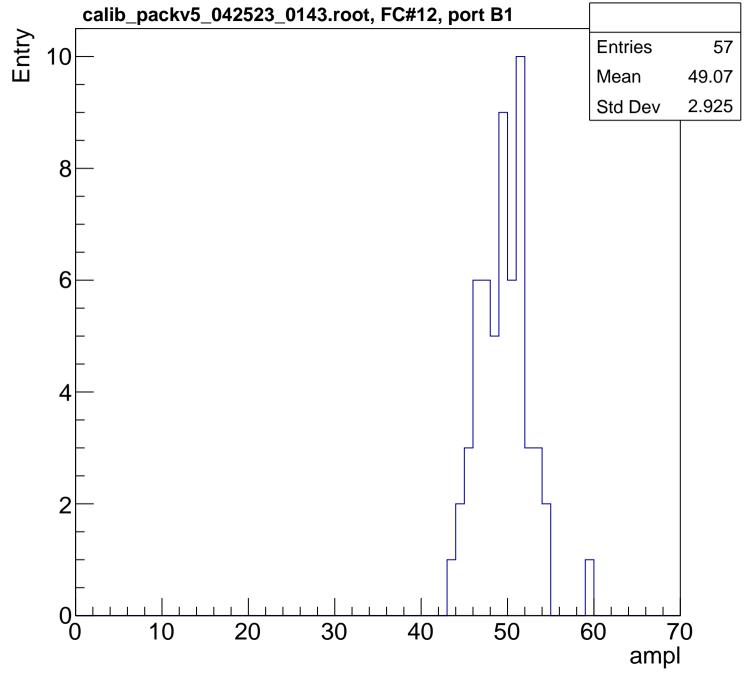


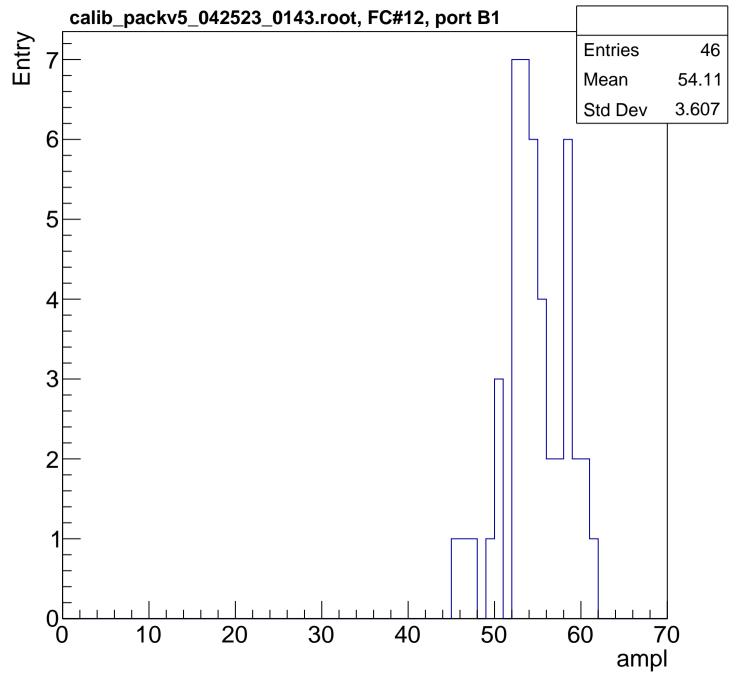


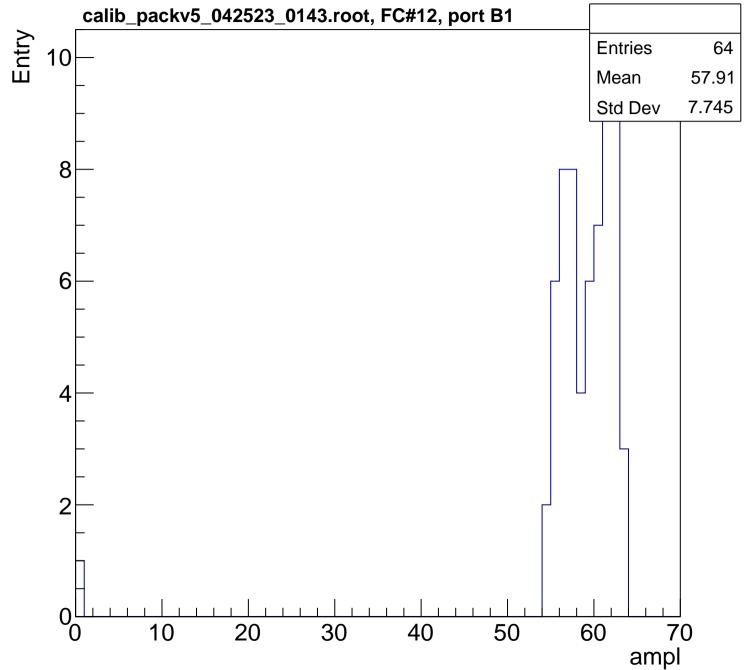


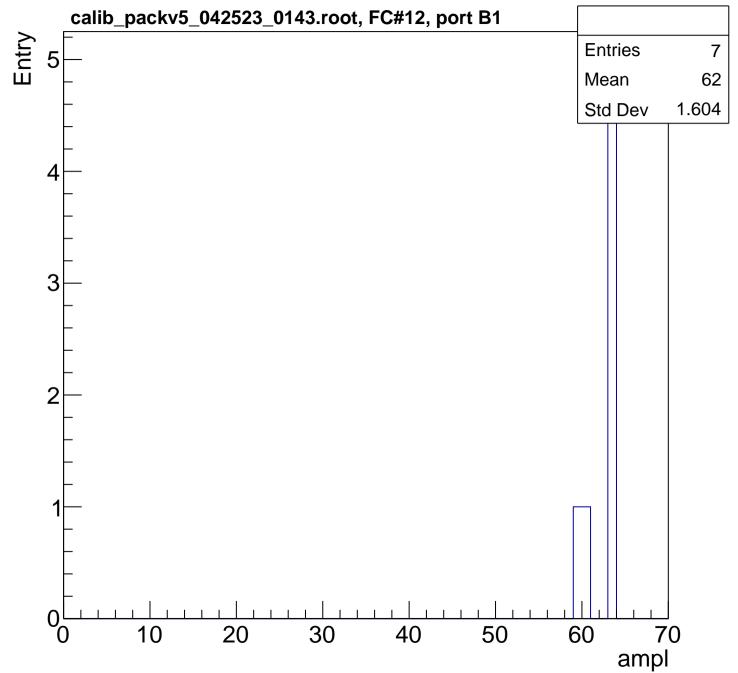


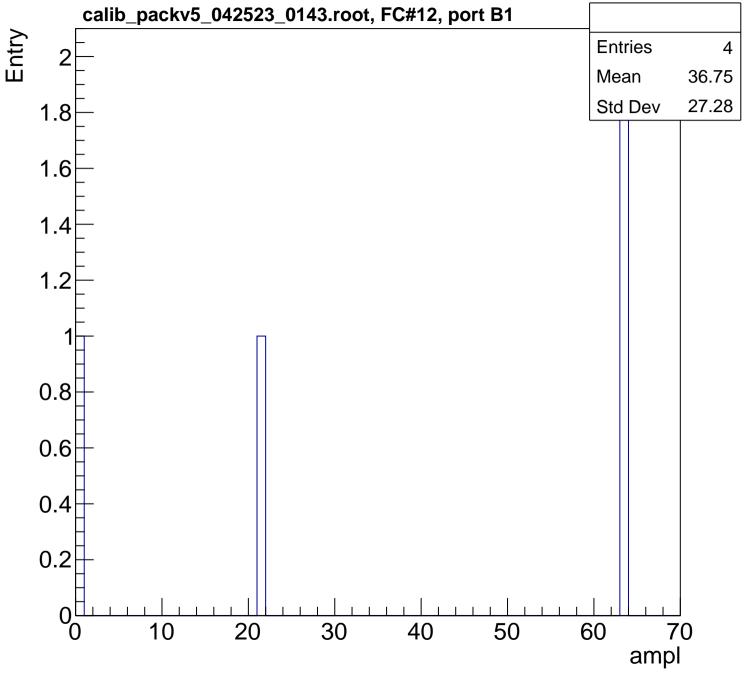


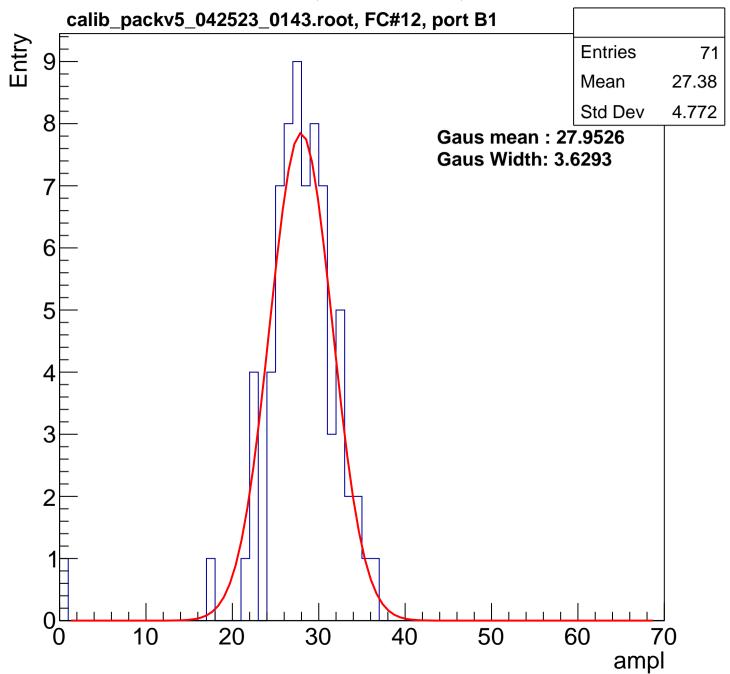


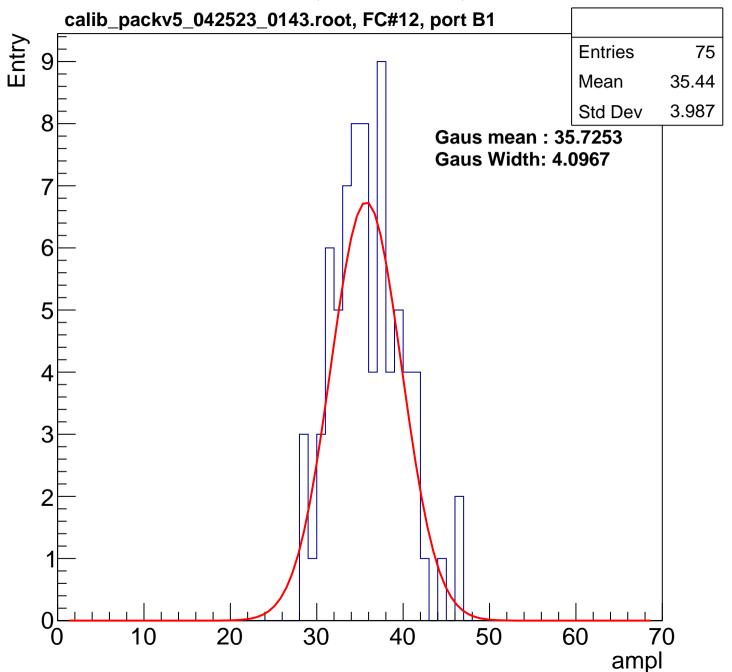


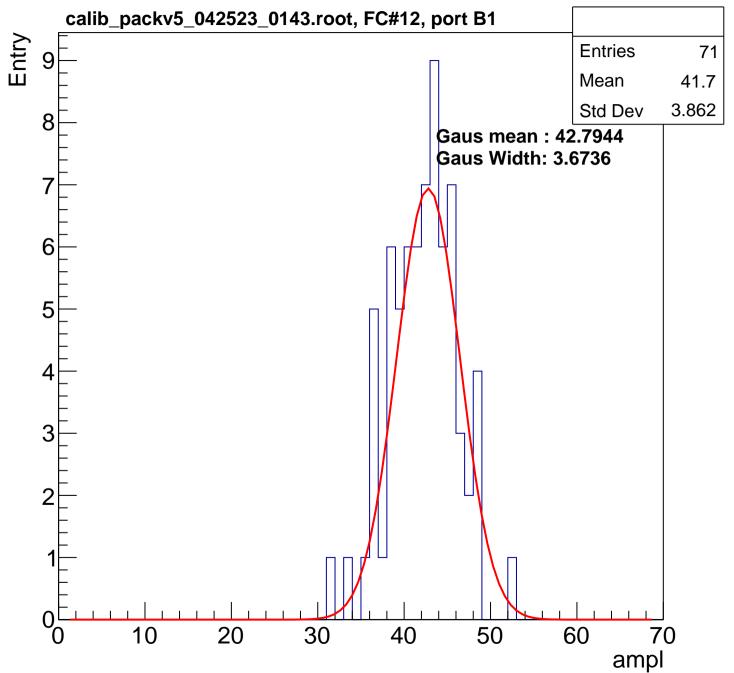


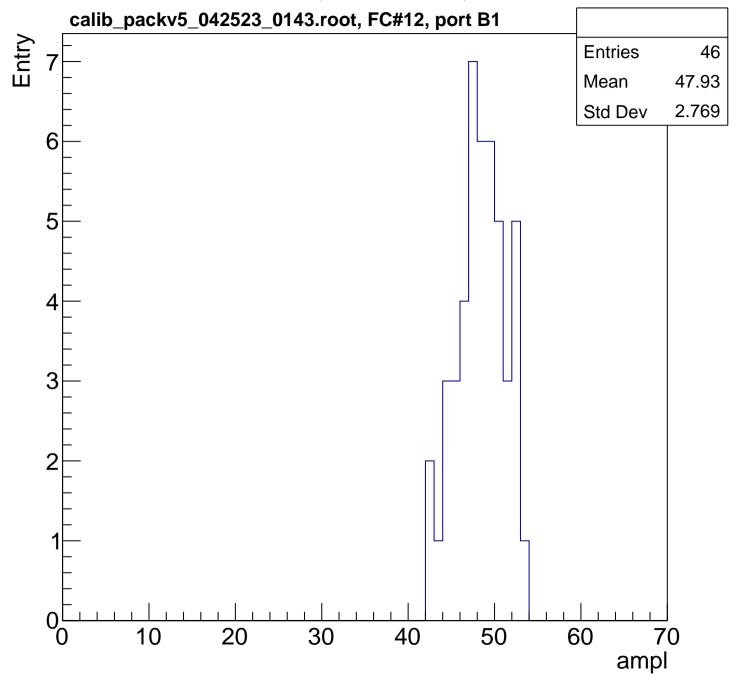


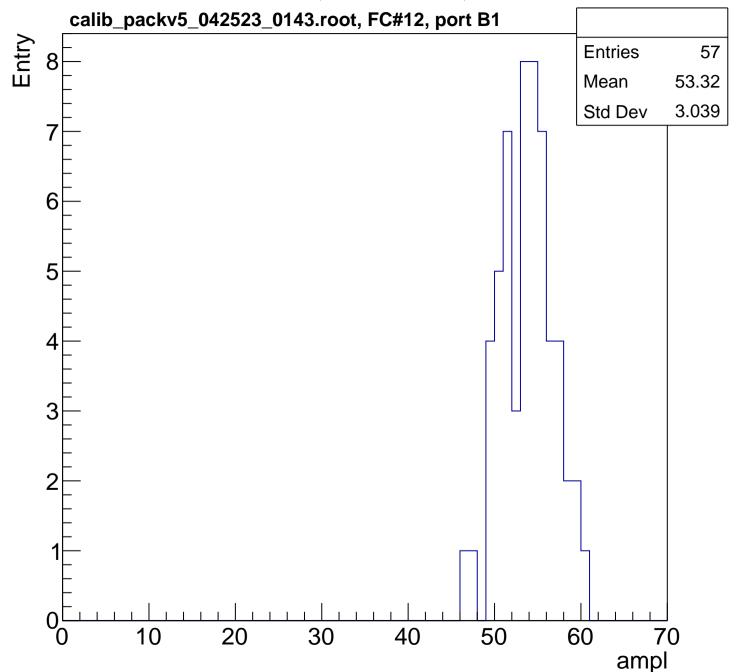


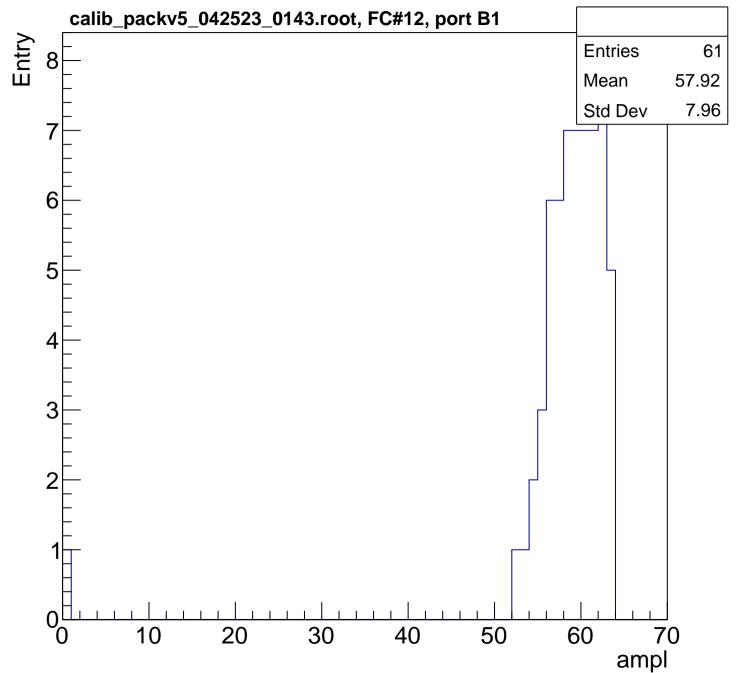


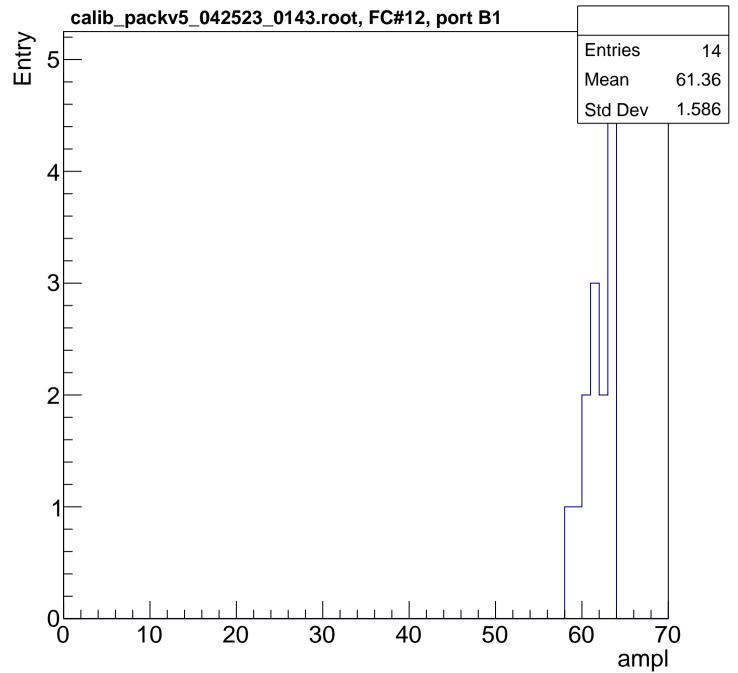


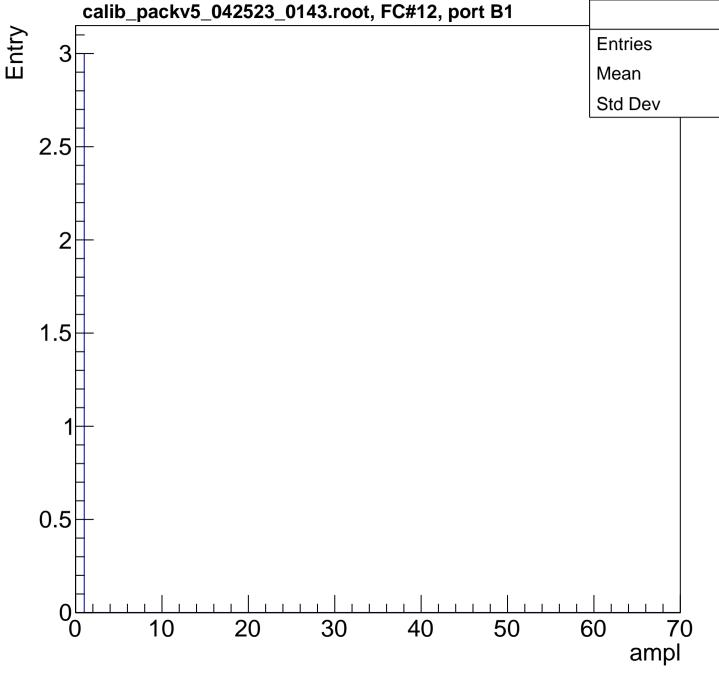


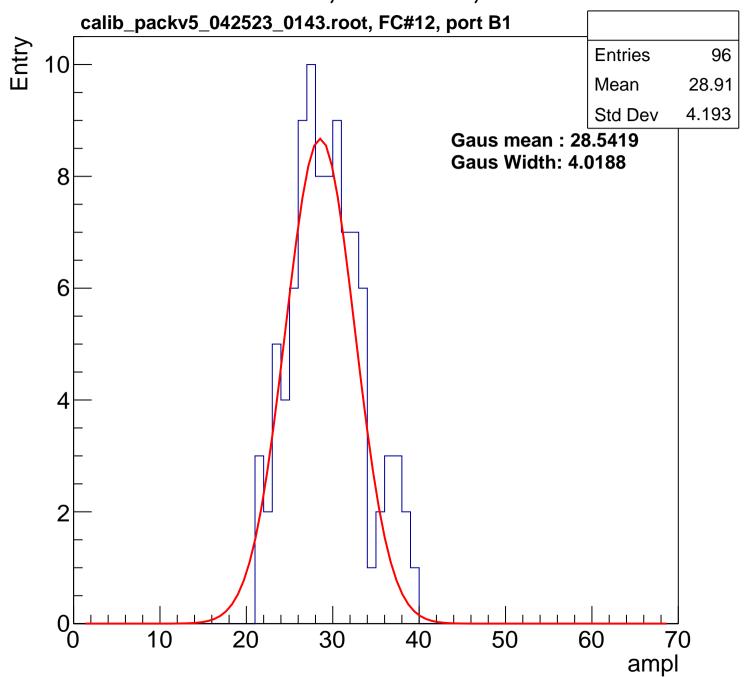


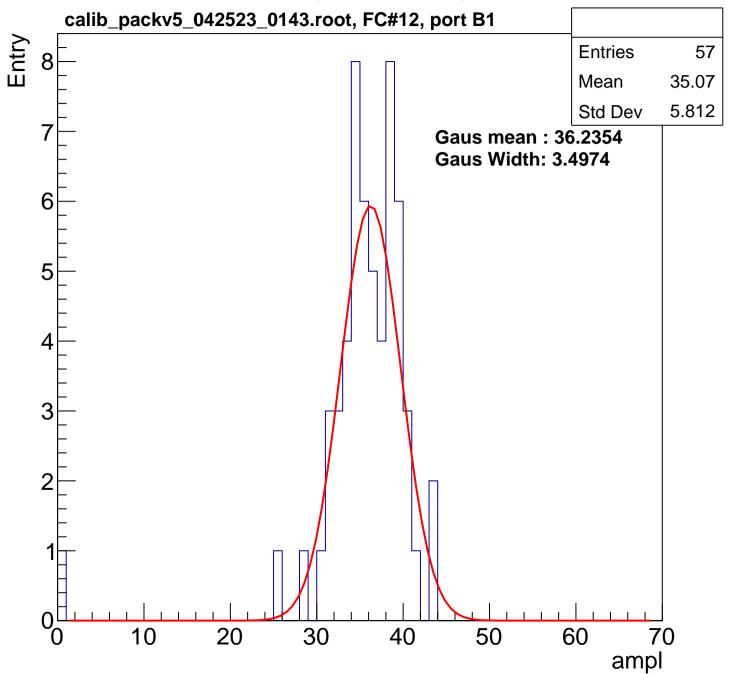


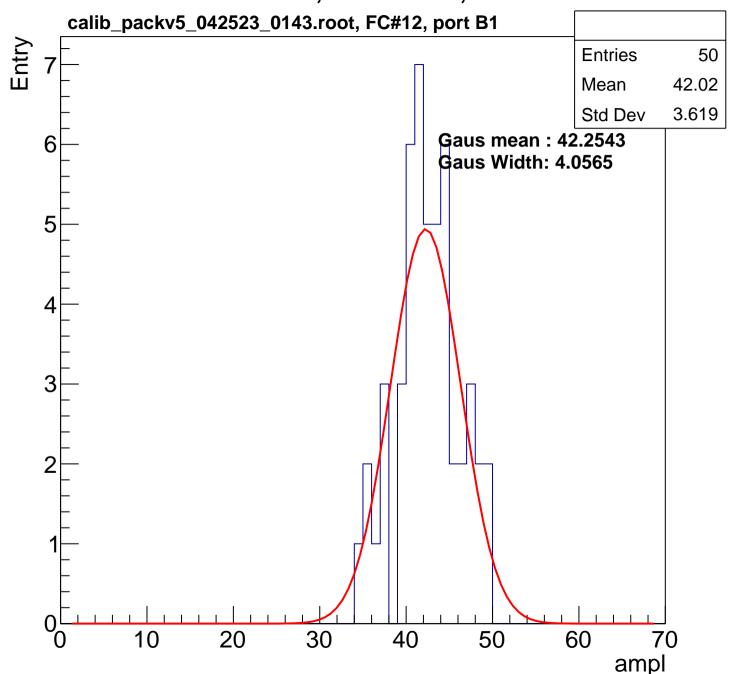


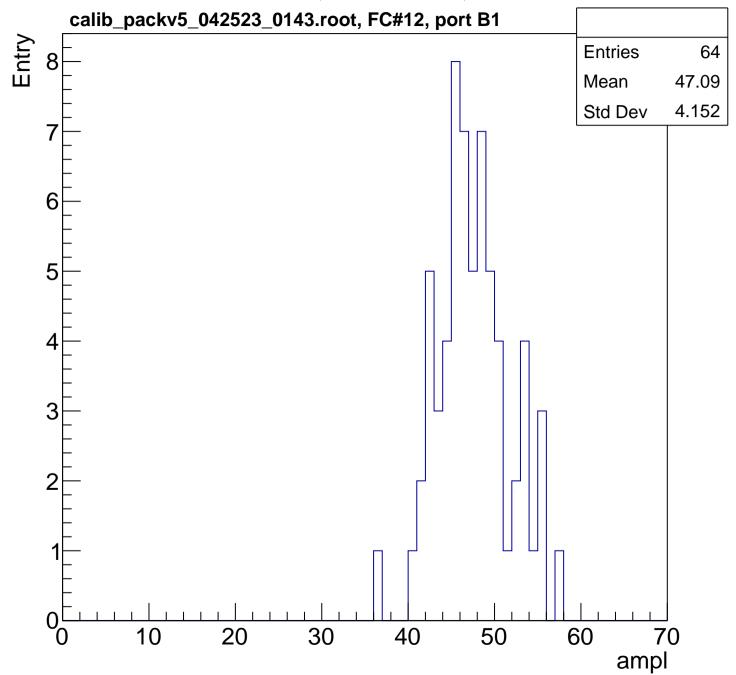


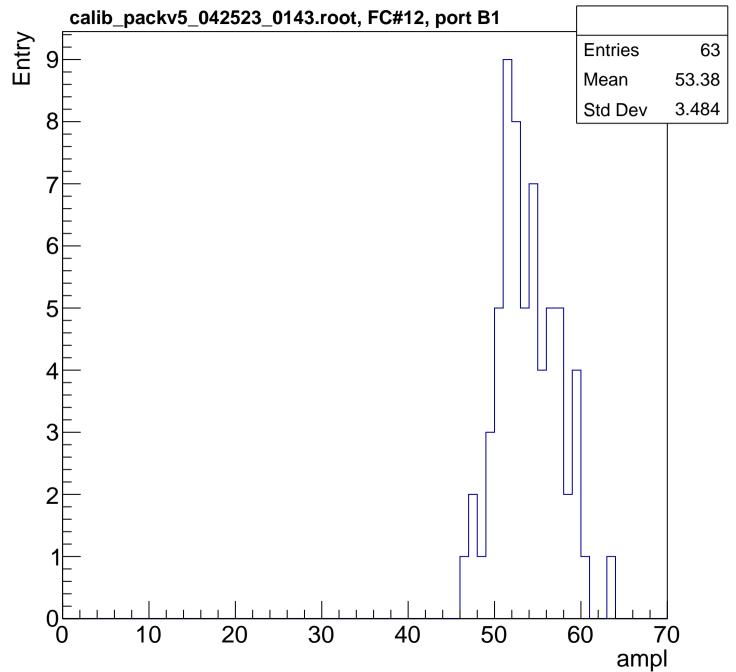


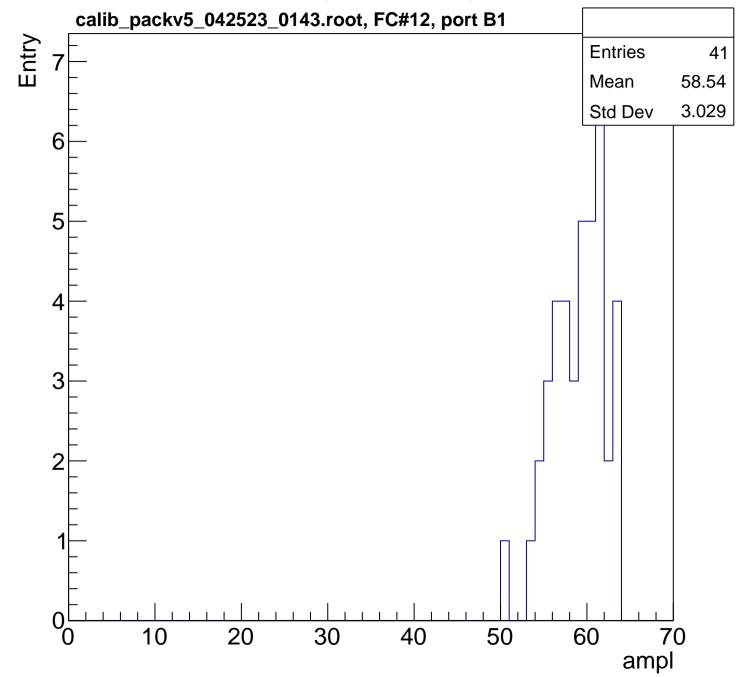


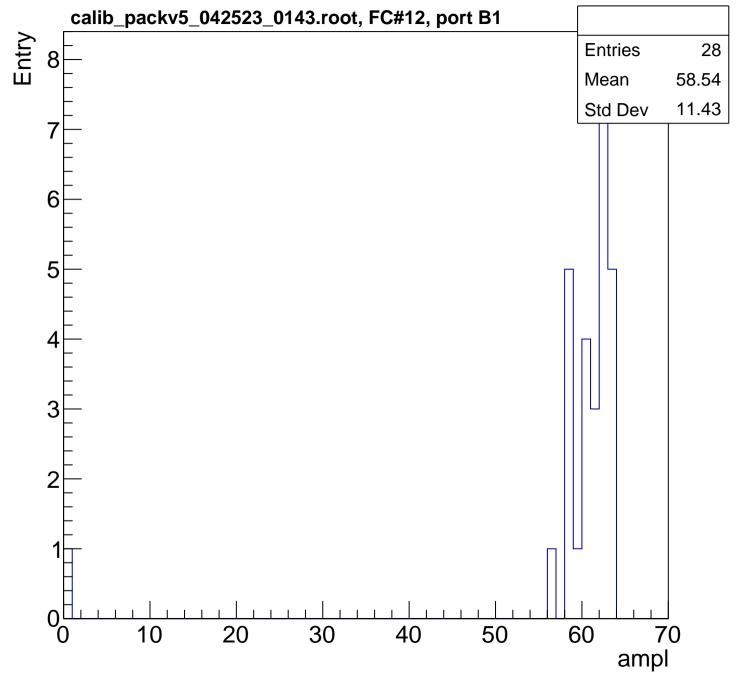




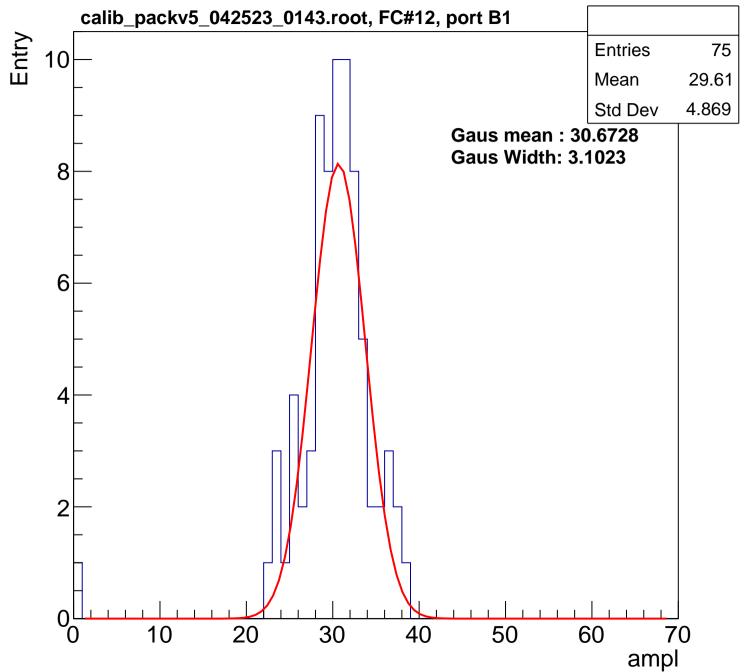


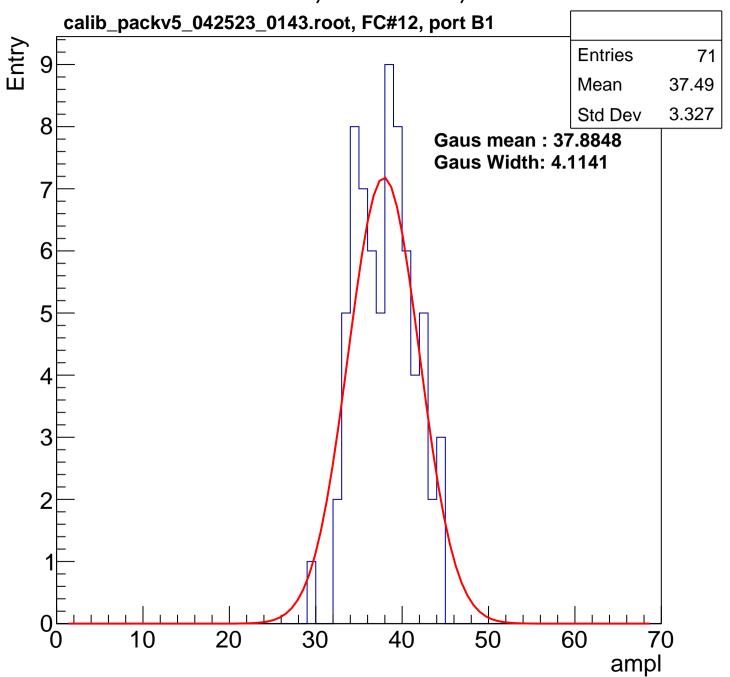


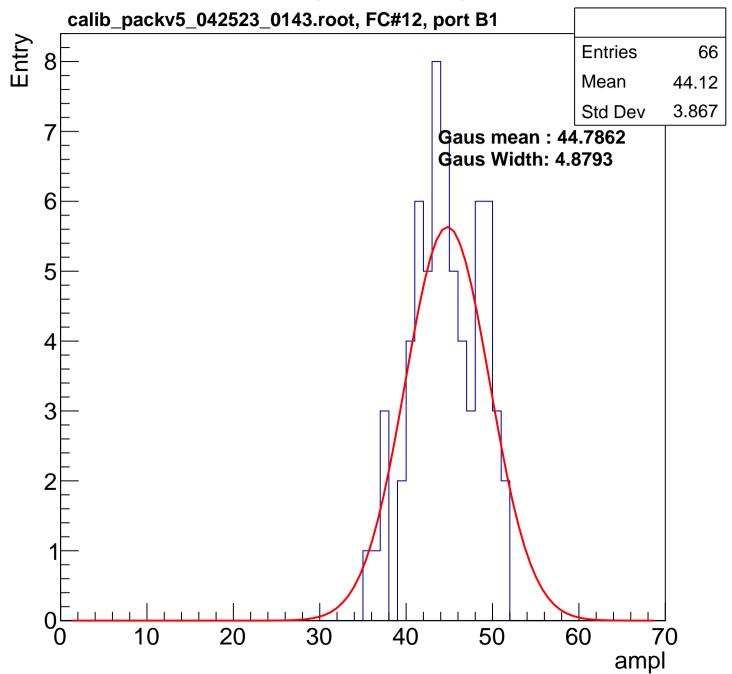


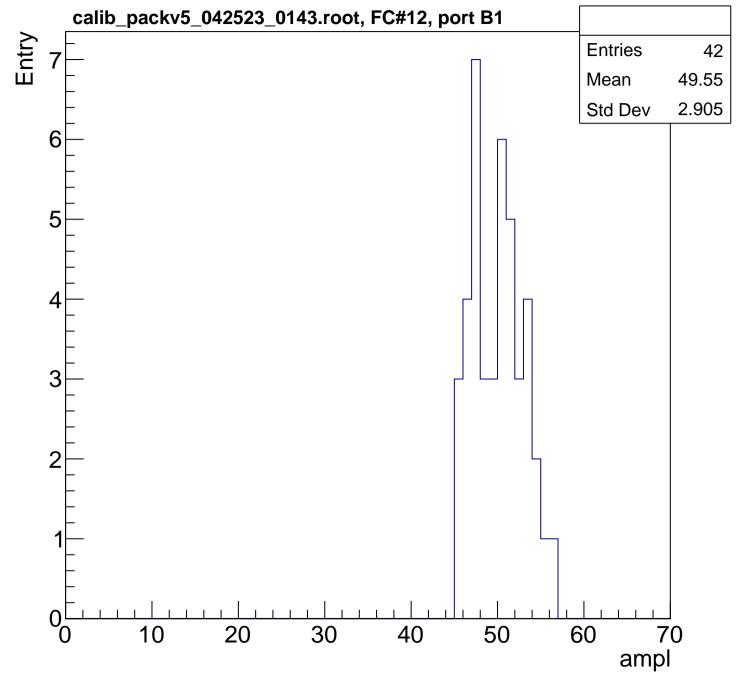


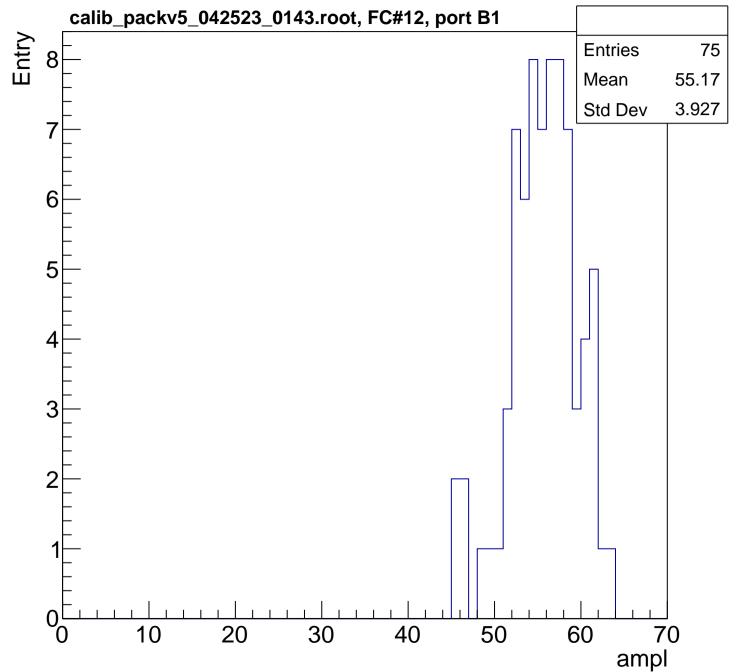
B0L102S, U2-ch84, adc7 calib_packv5_042523_0143.root, FC#12, port B1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

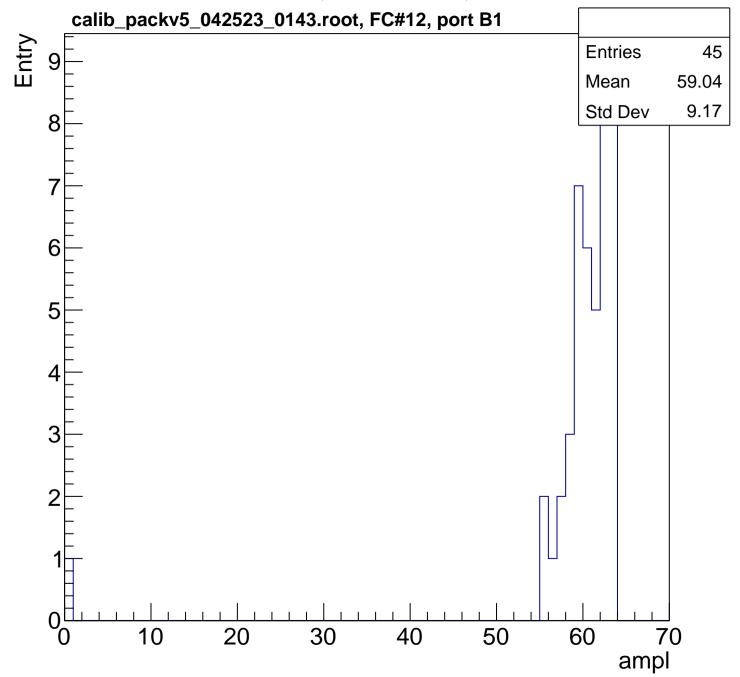


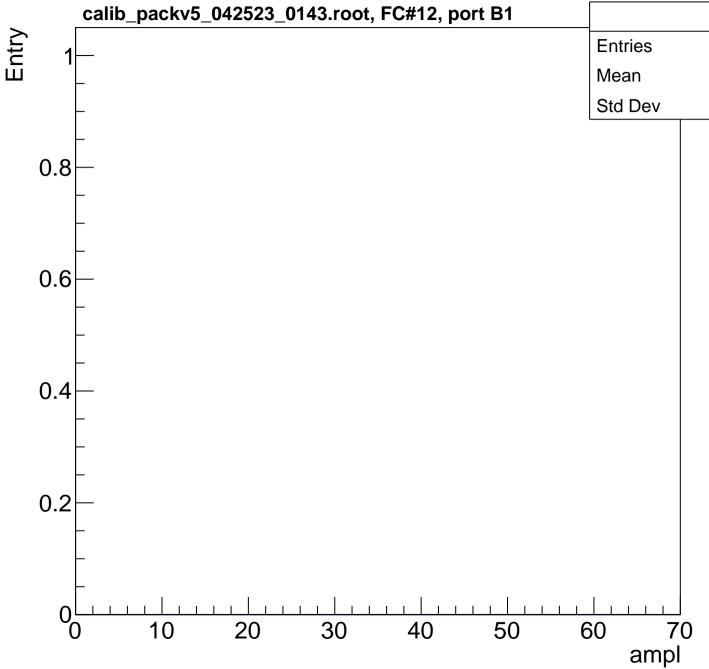


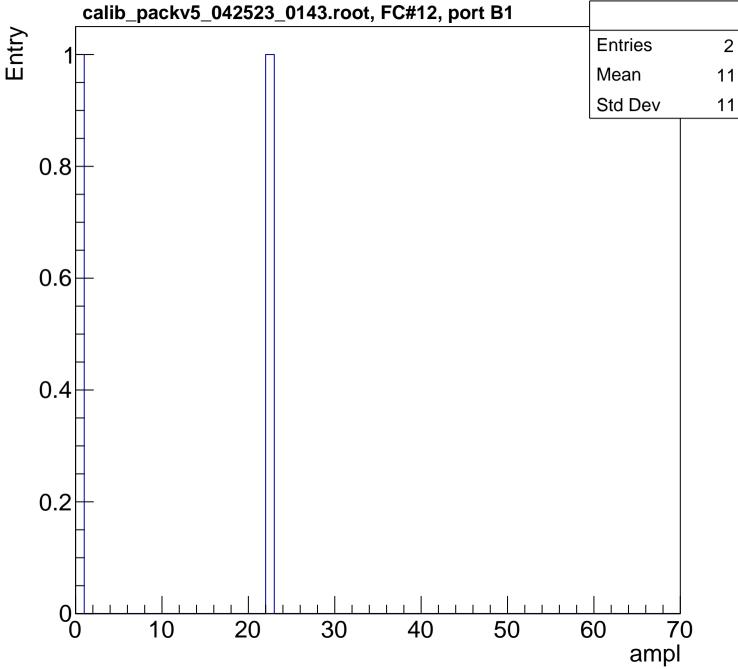


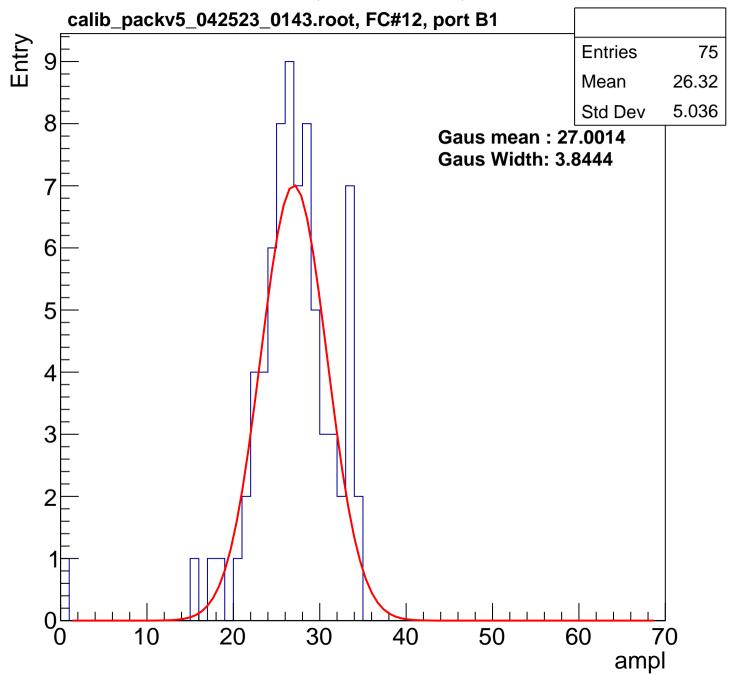


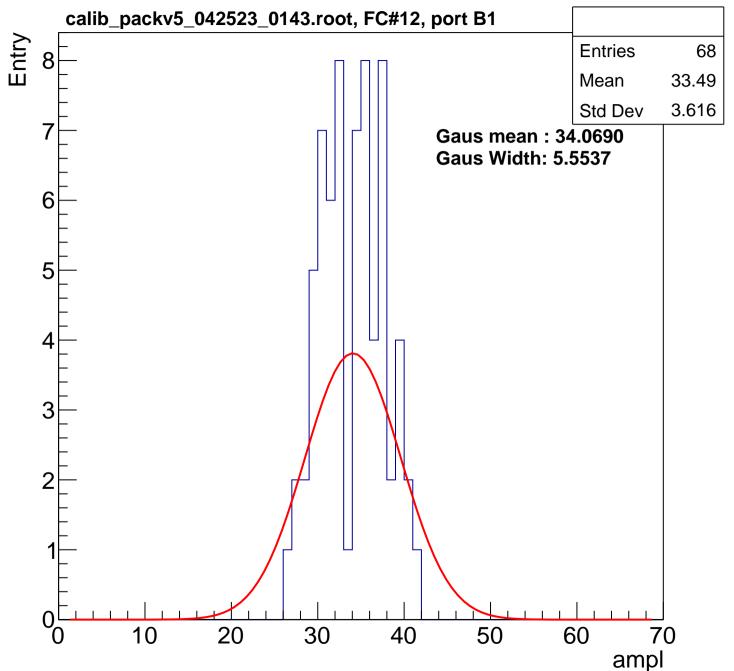


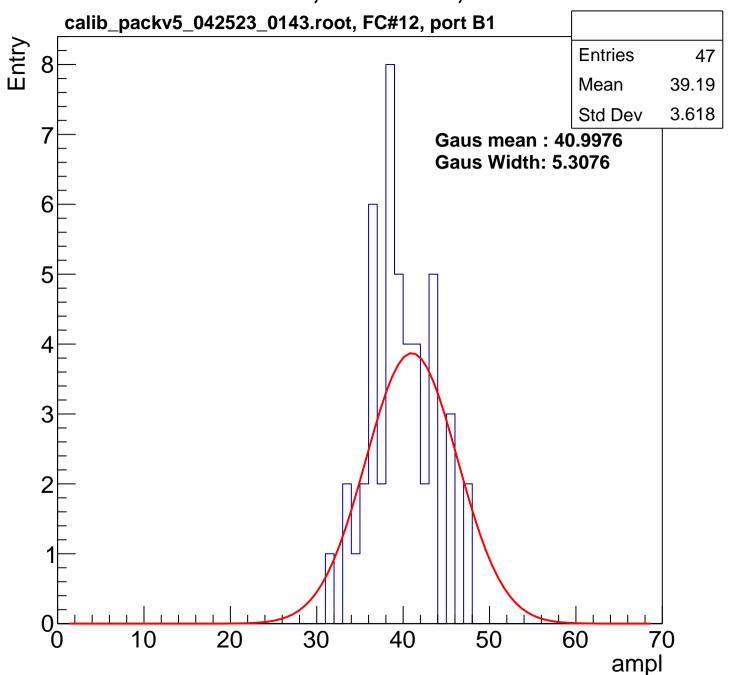


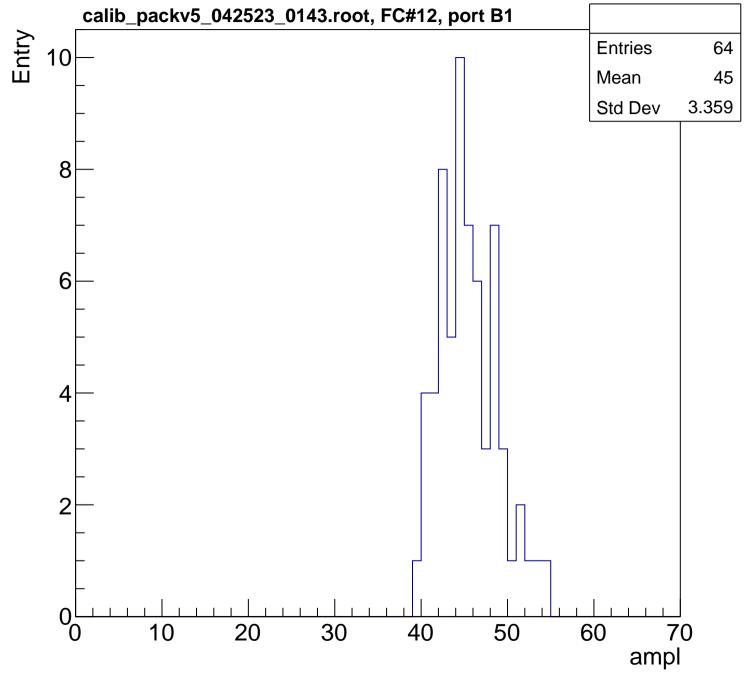


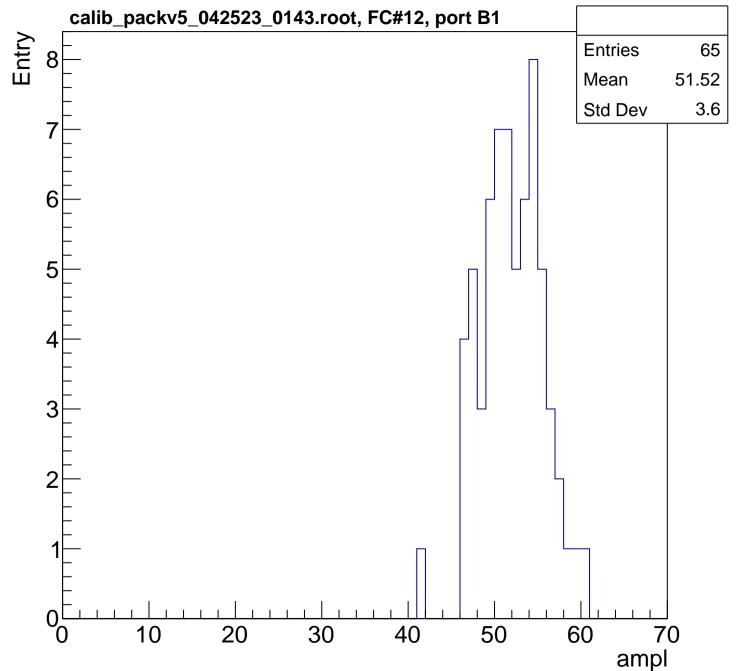


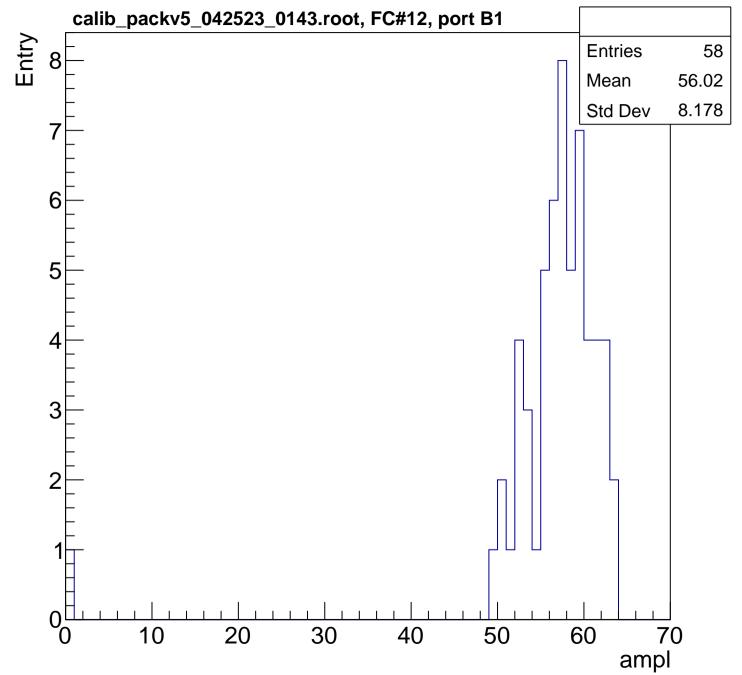


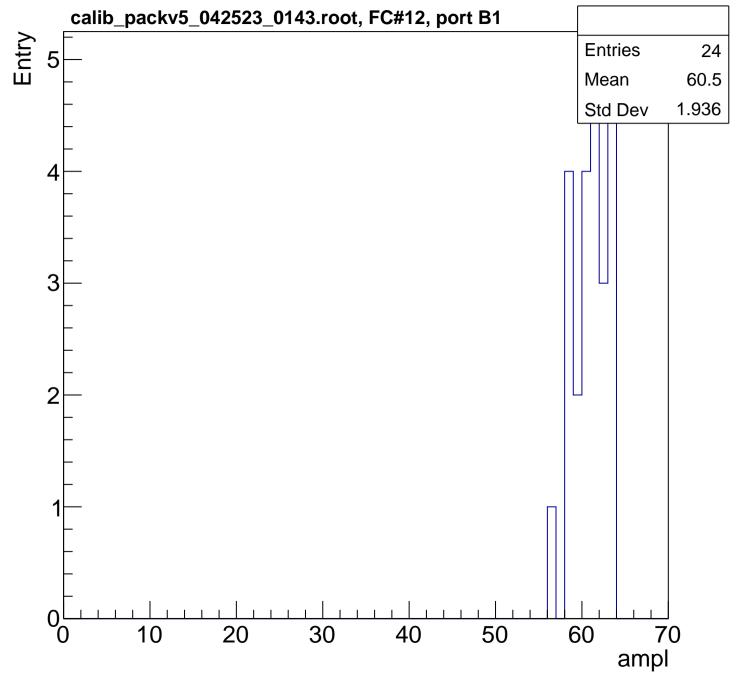


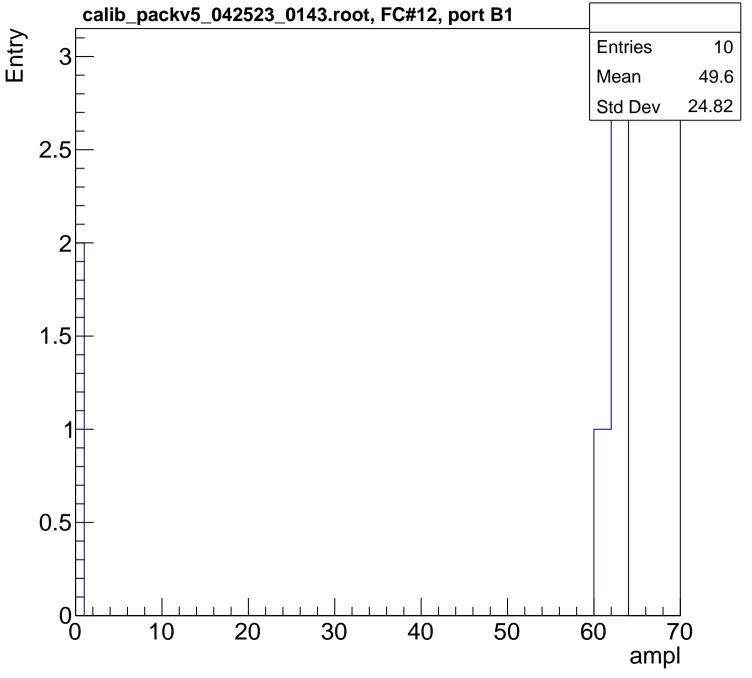


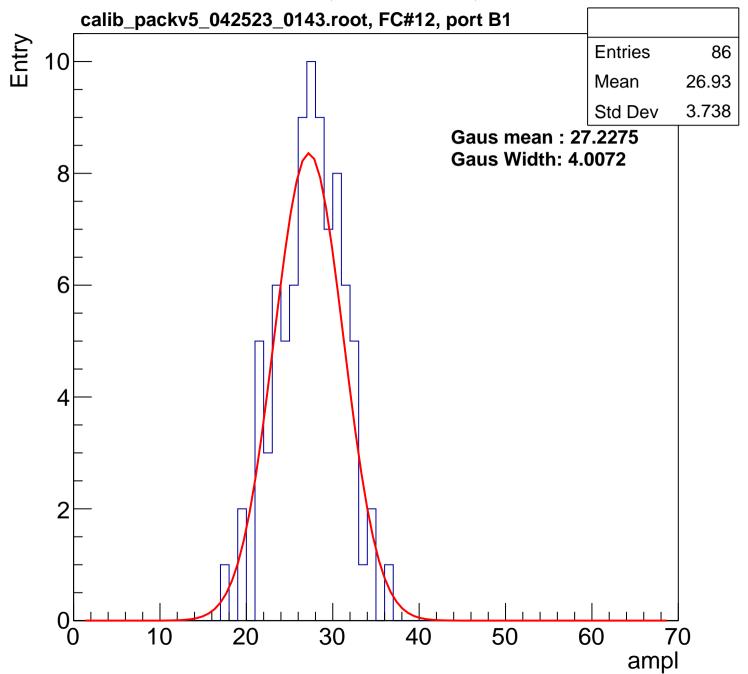


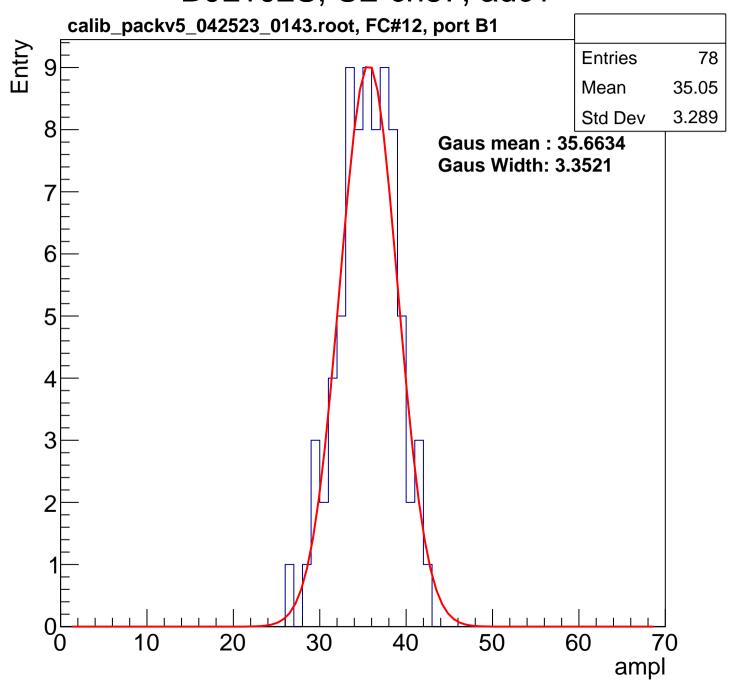


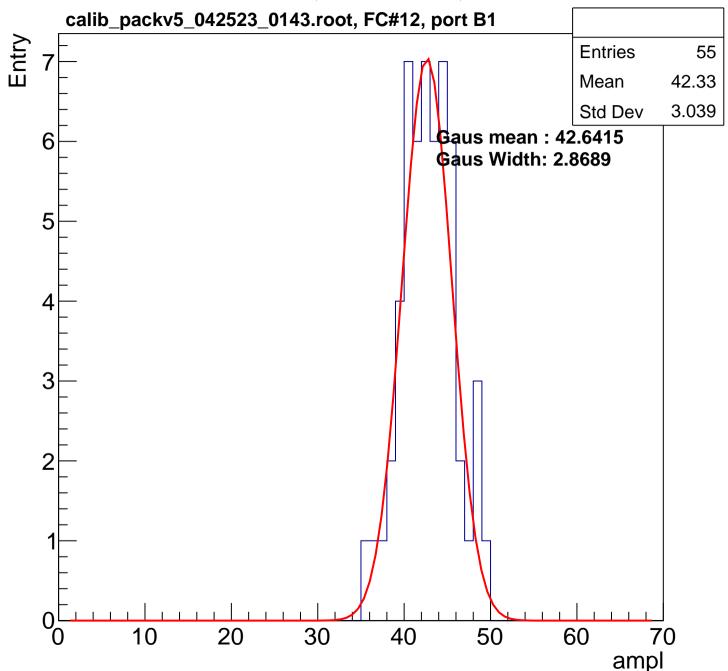


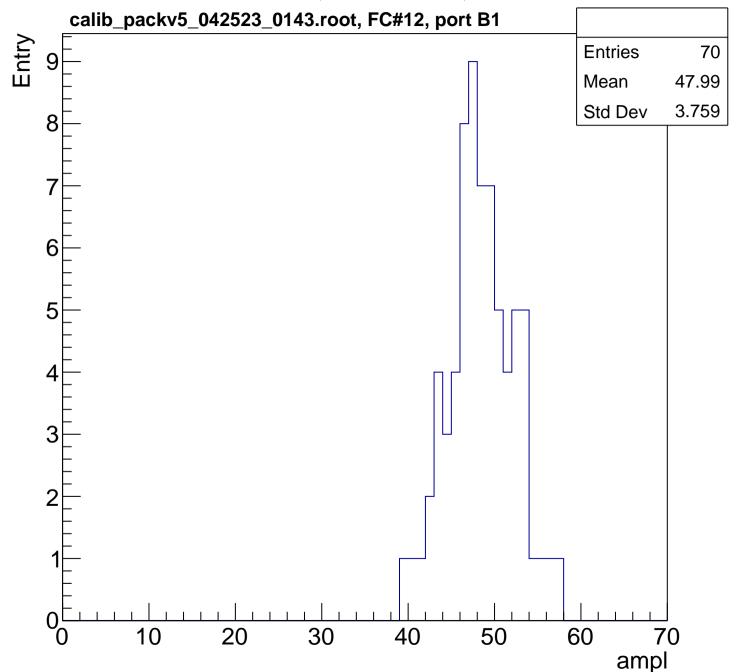


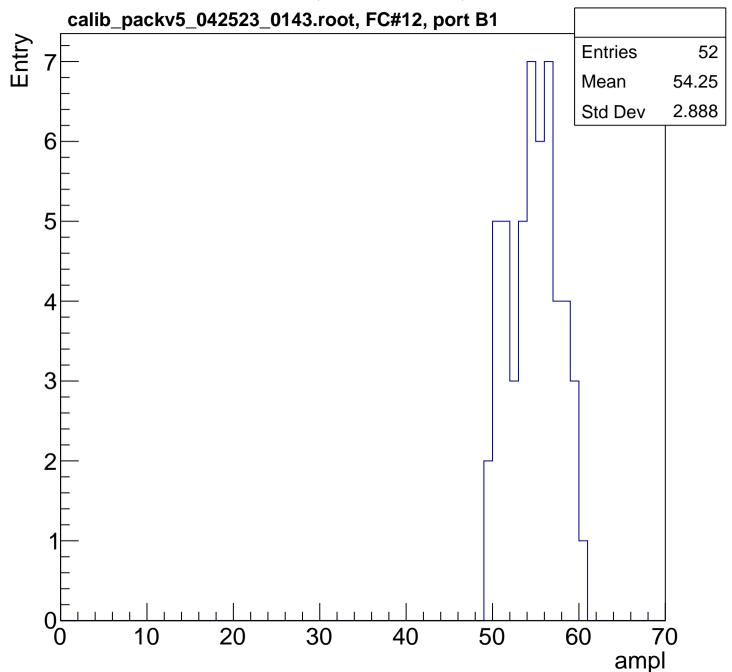


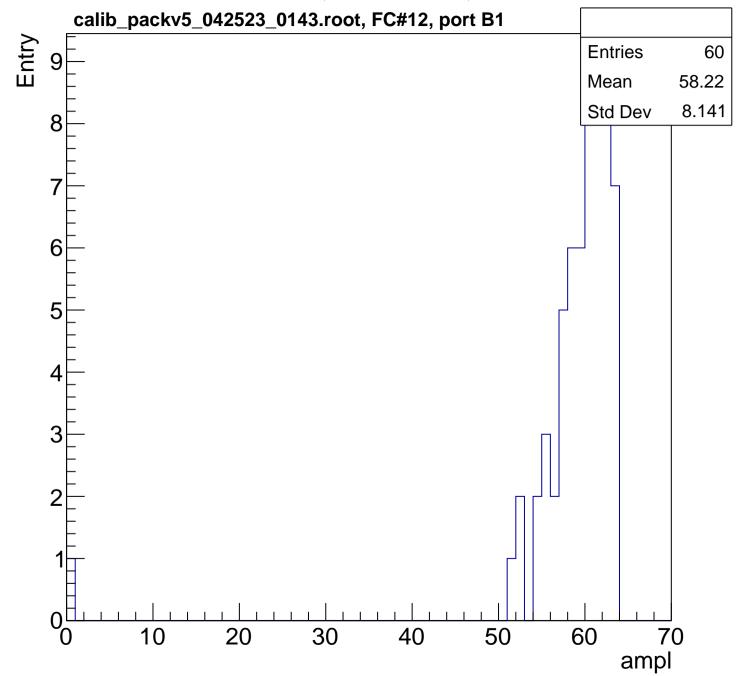


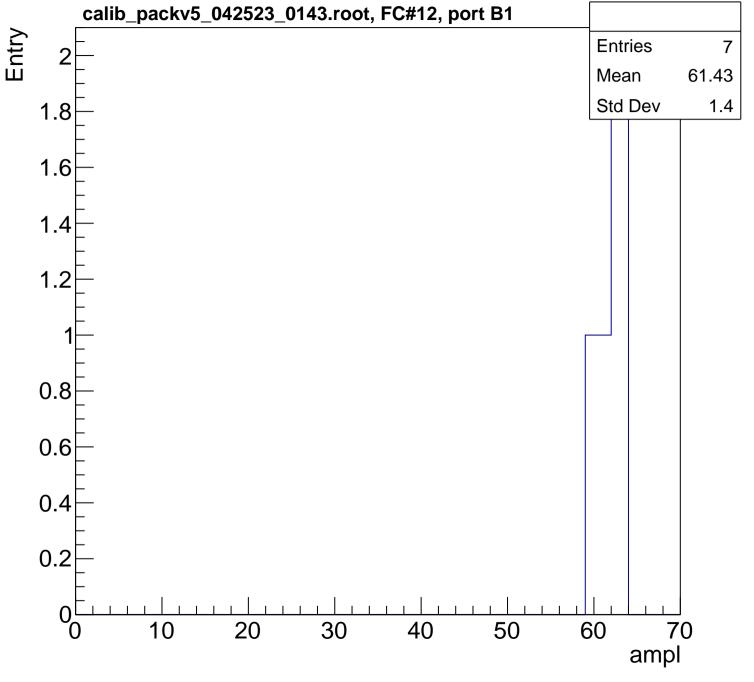


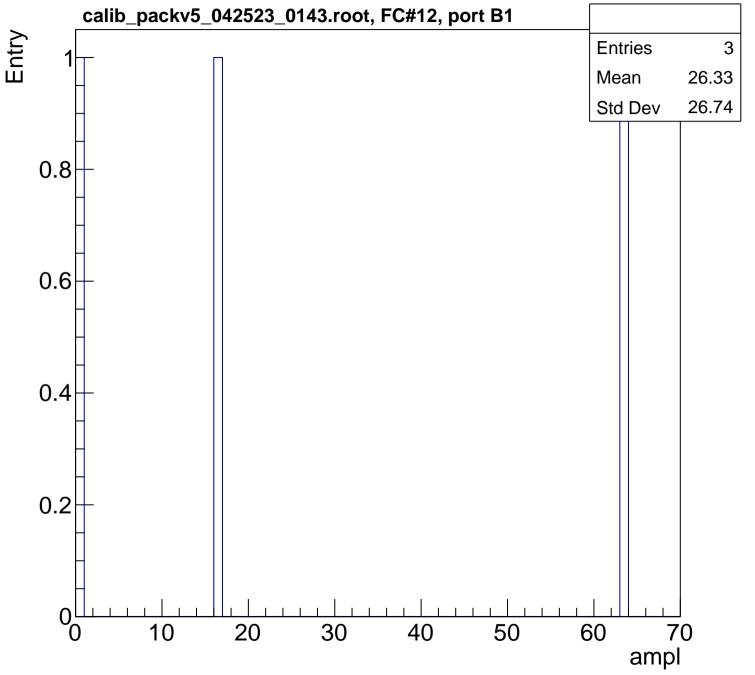


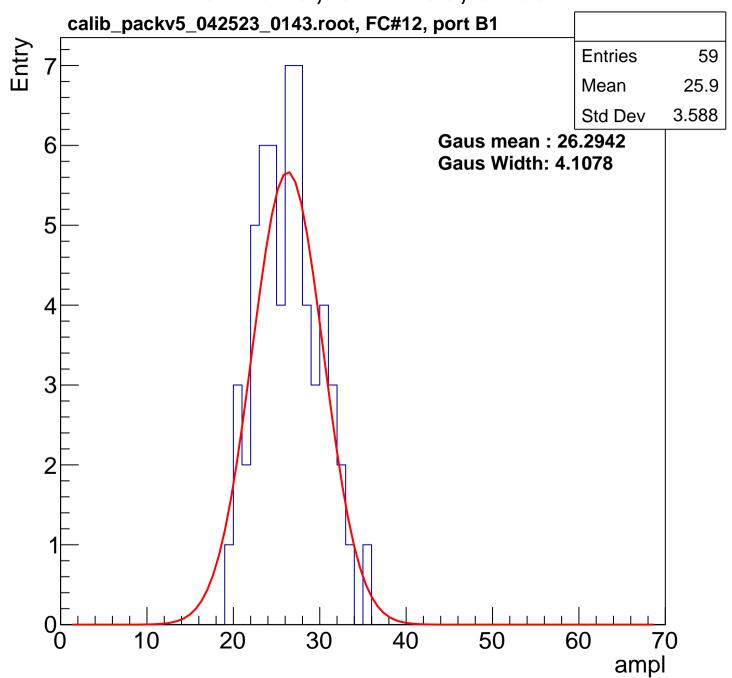


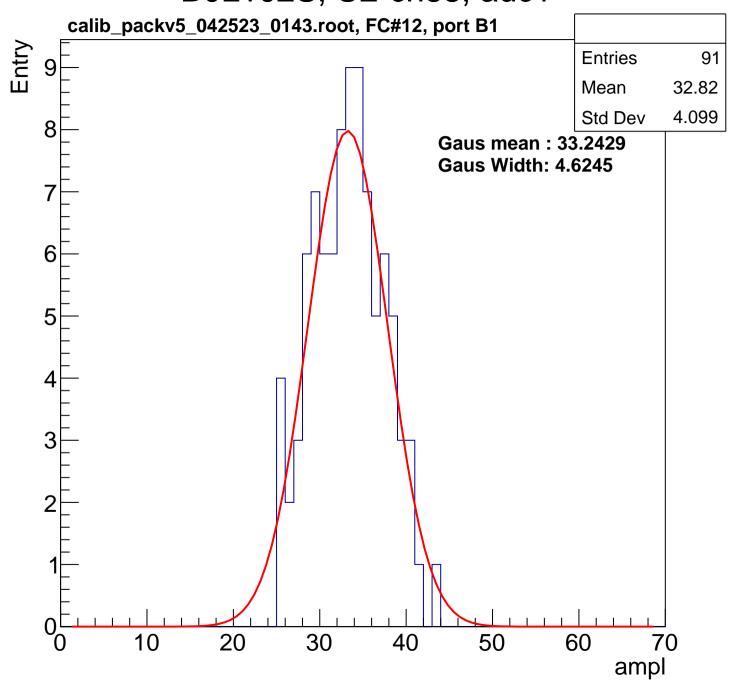


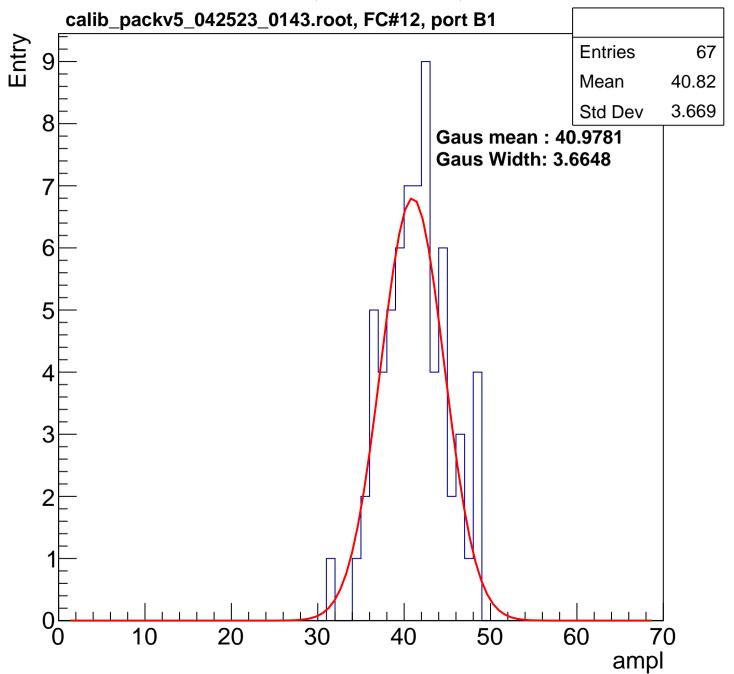


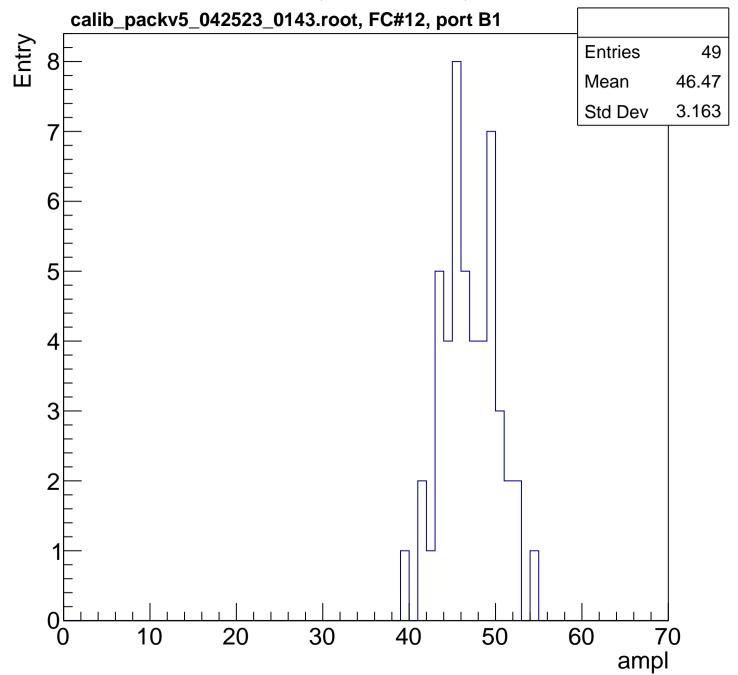


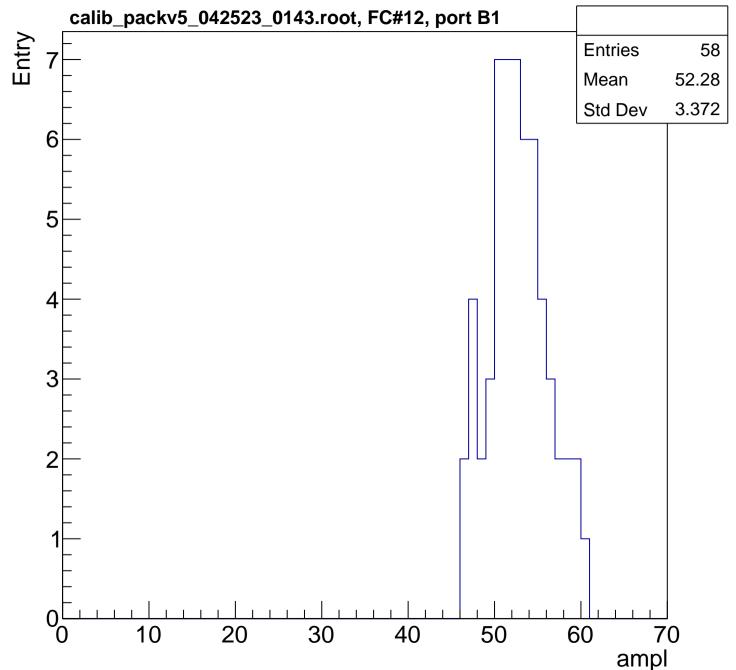


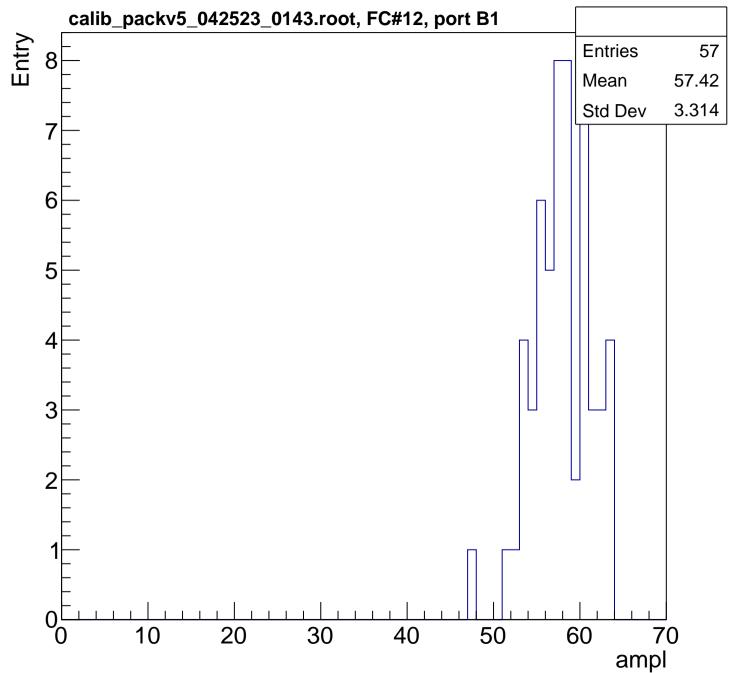


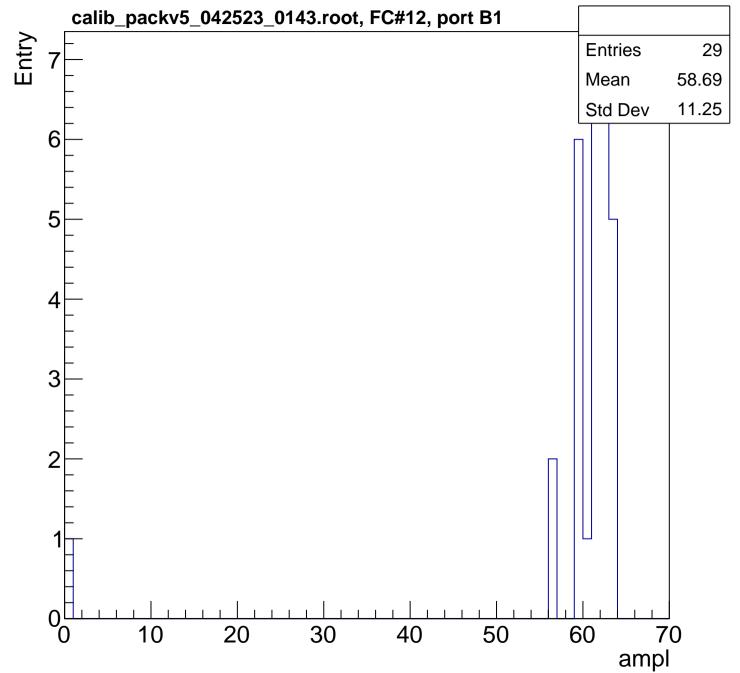


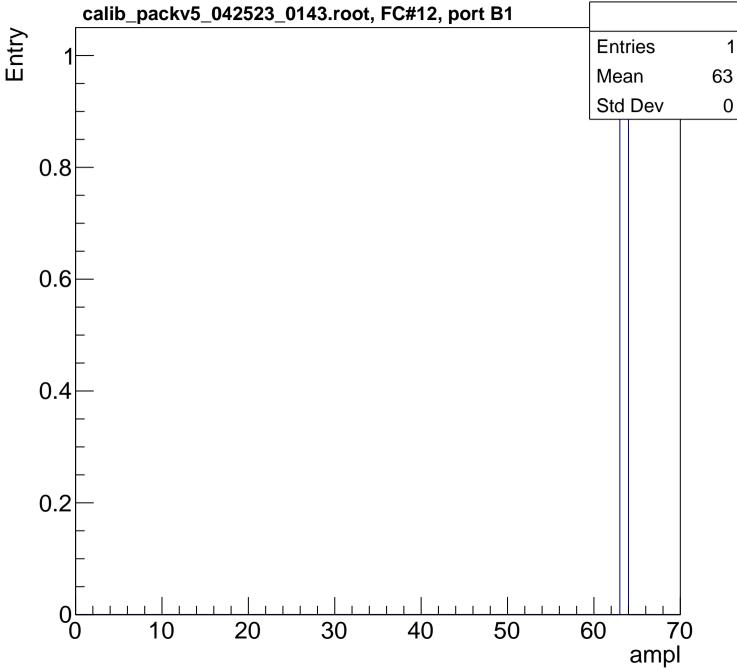


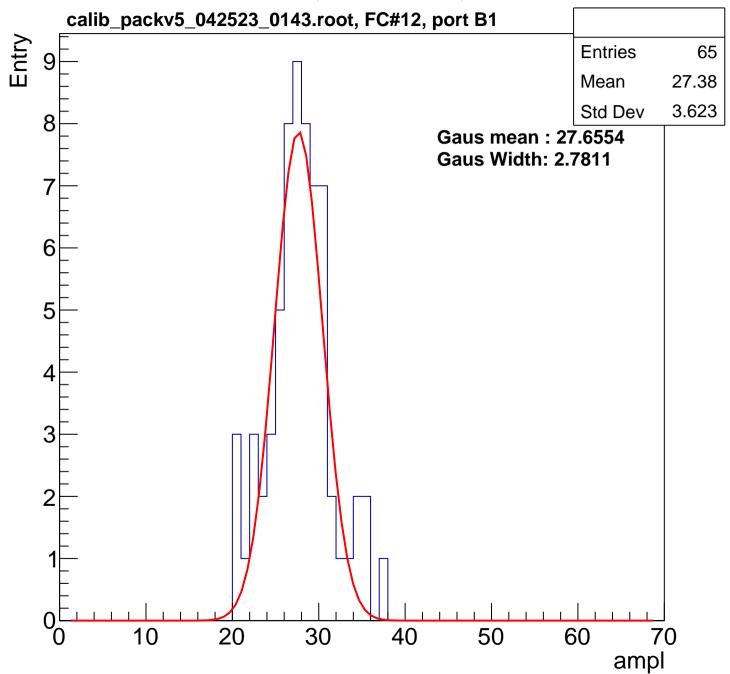


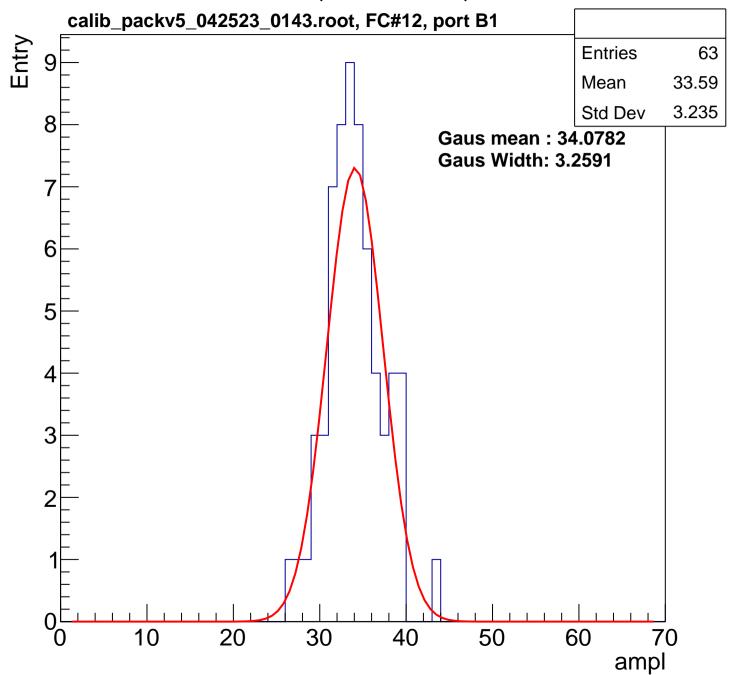


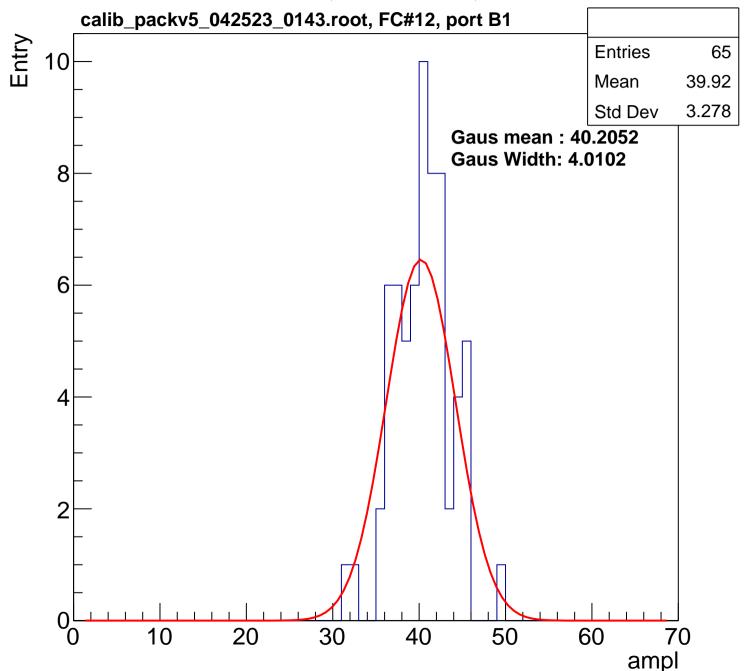


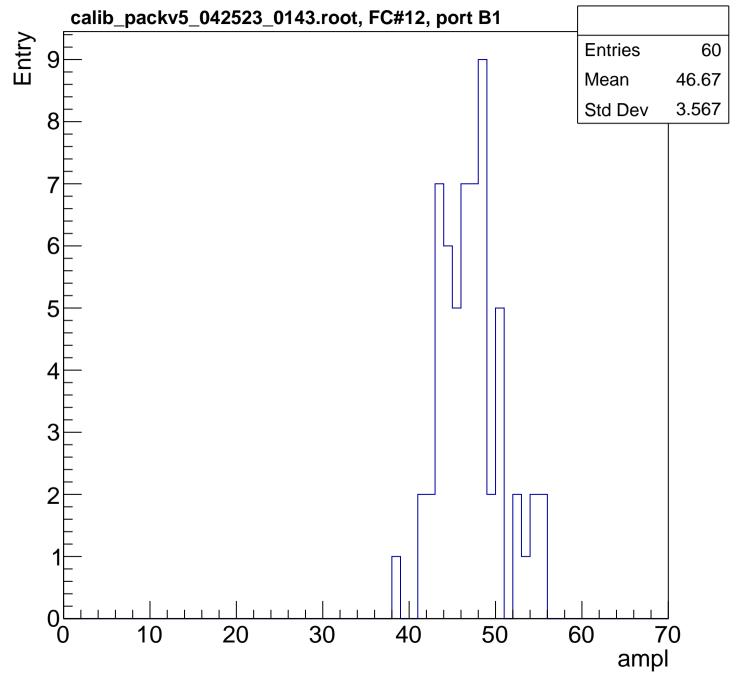


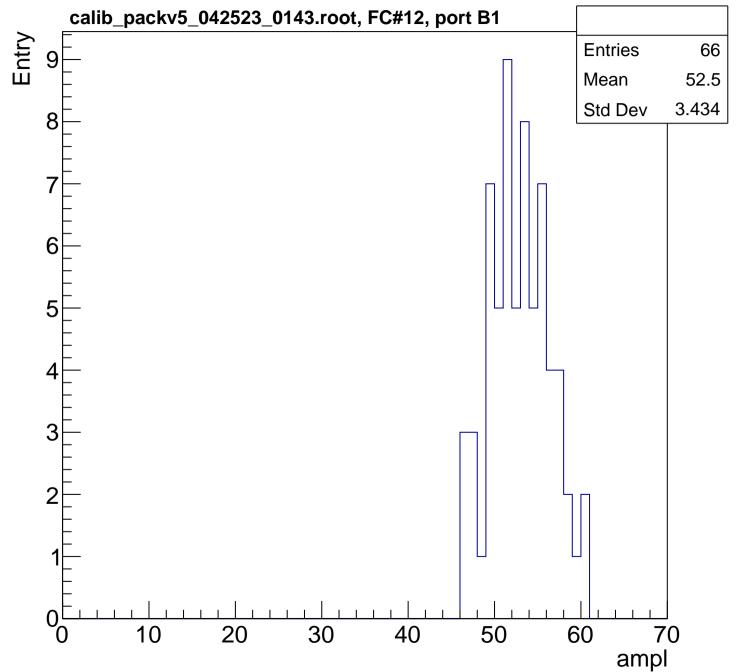


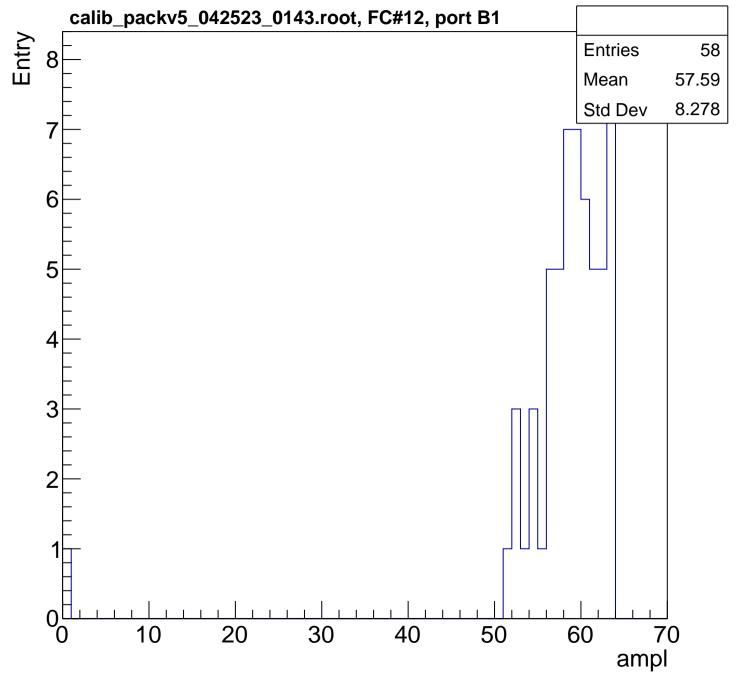


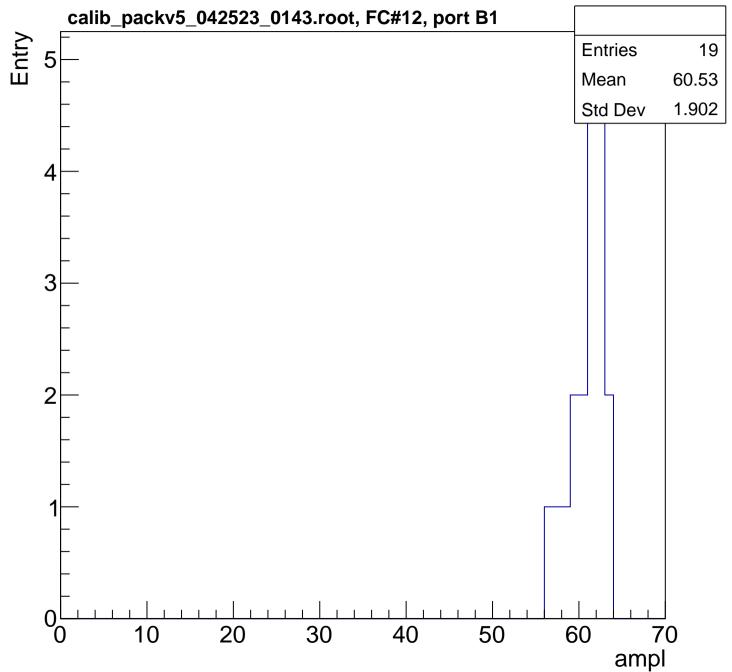


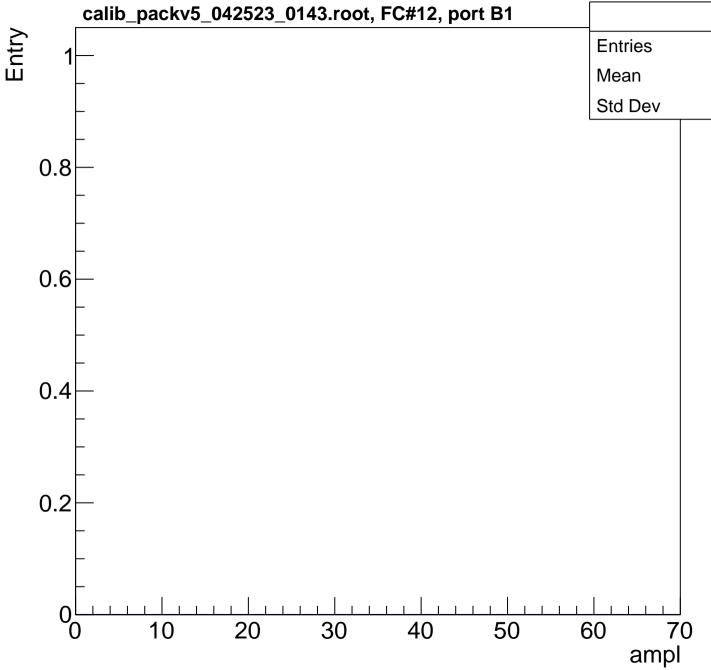


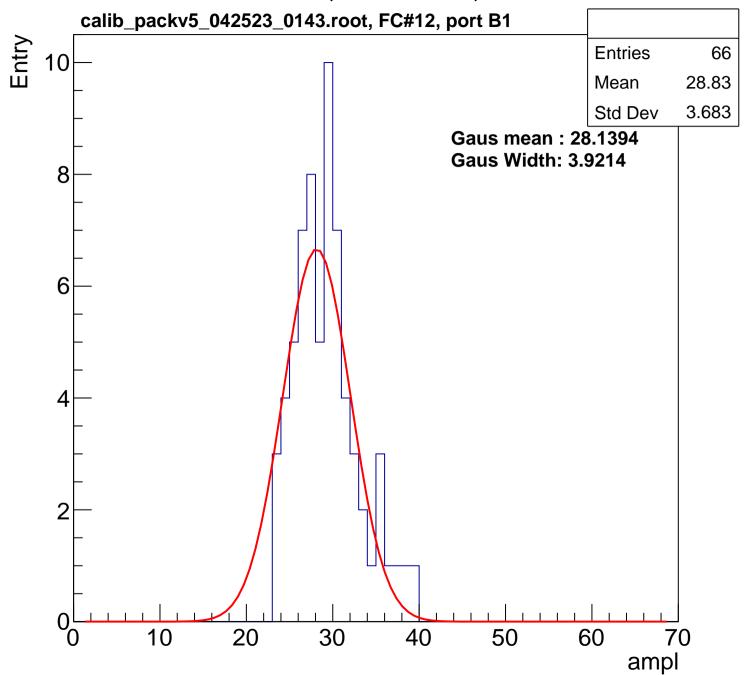


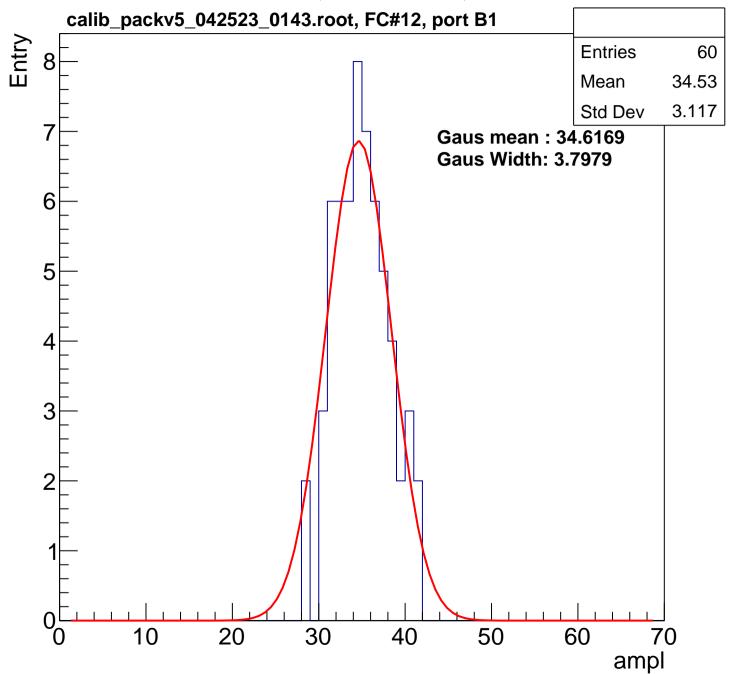


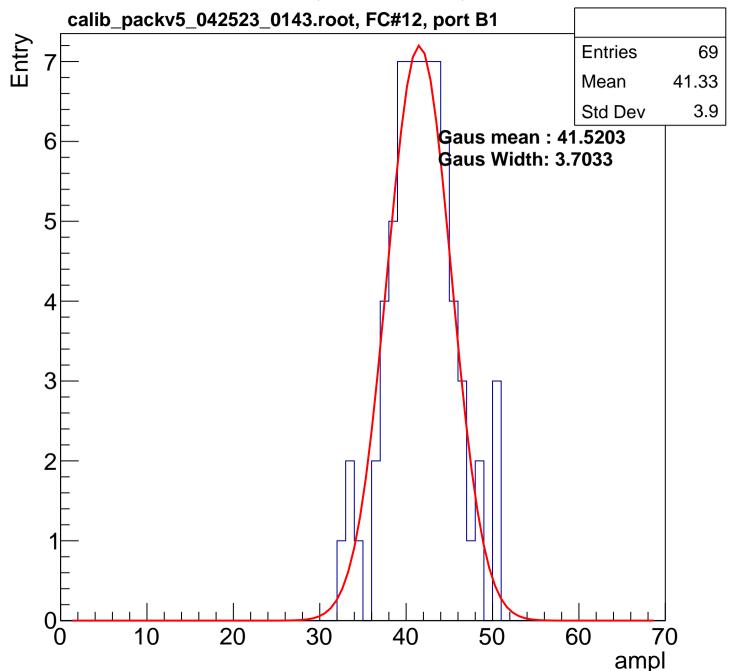


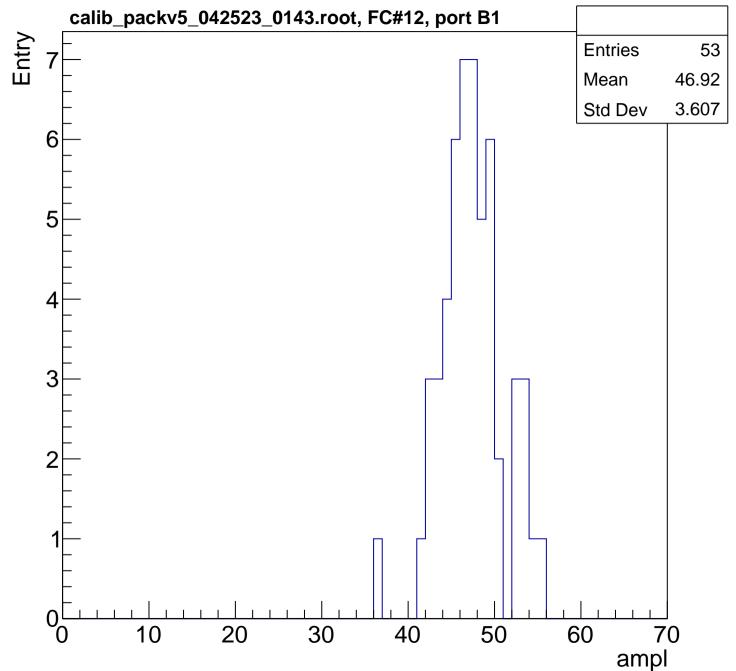


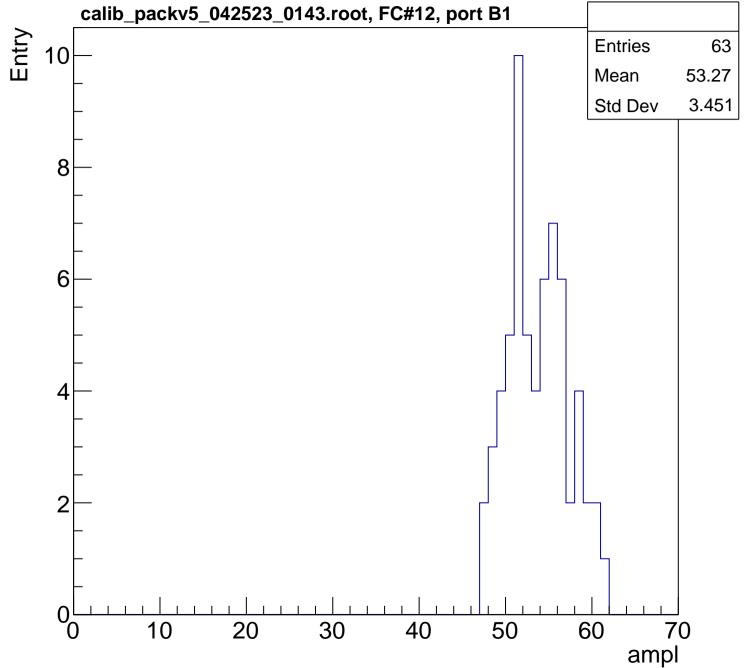


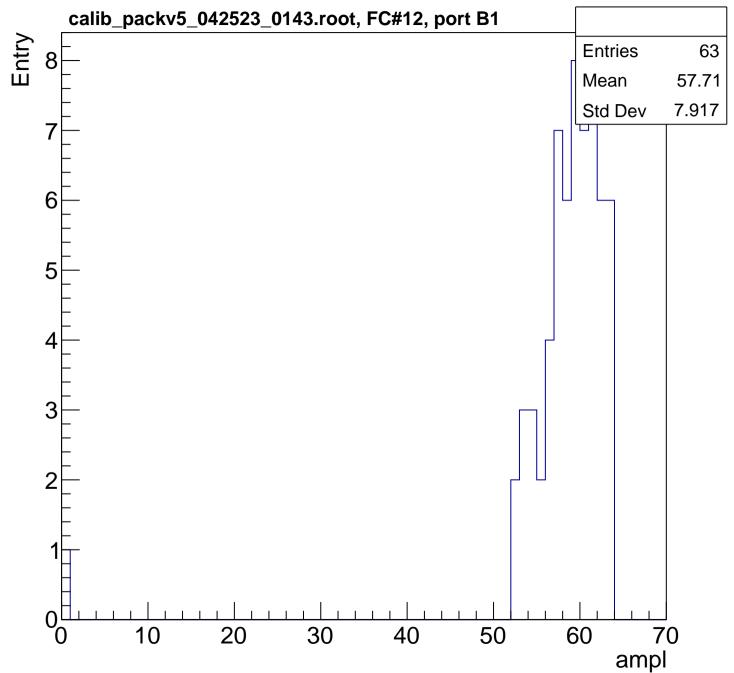


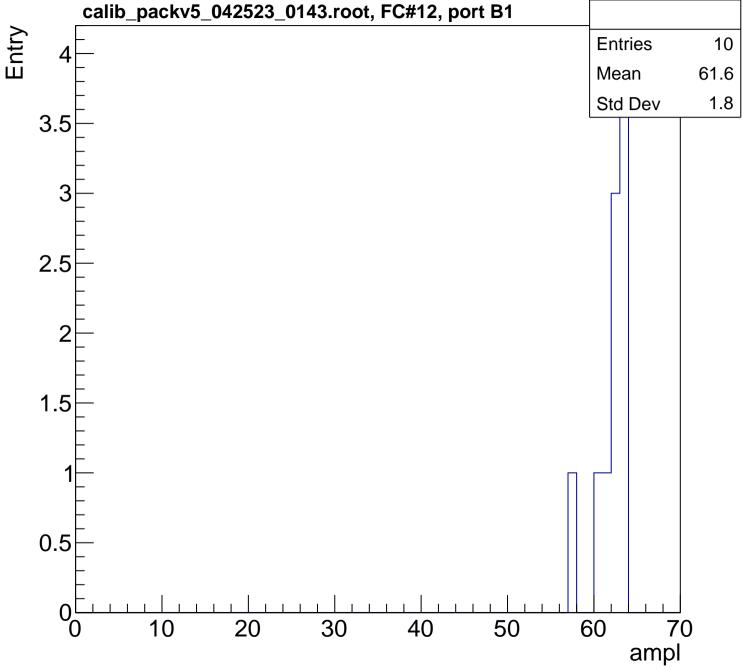




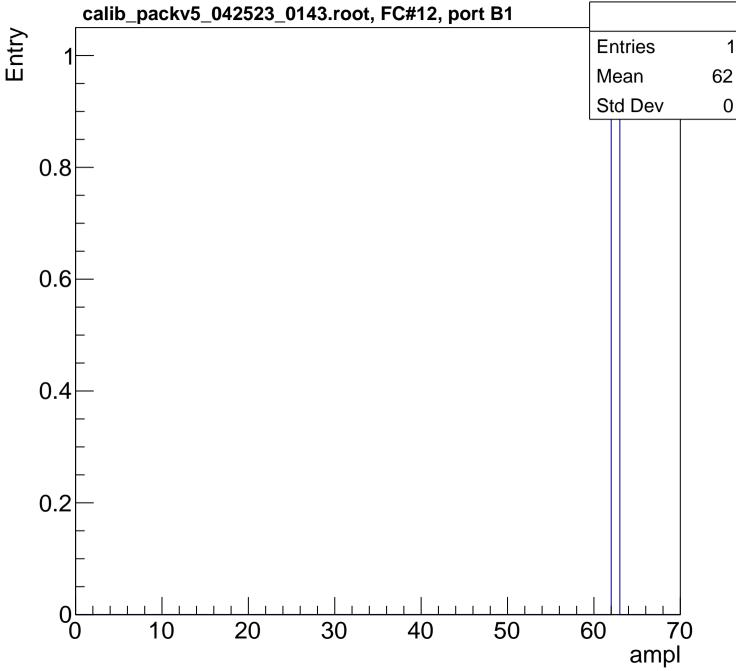


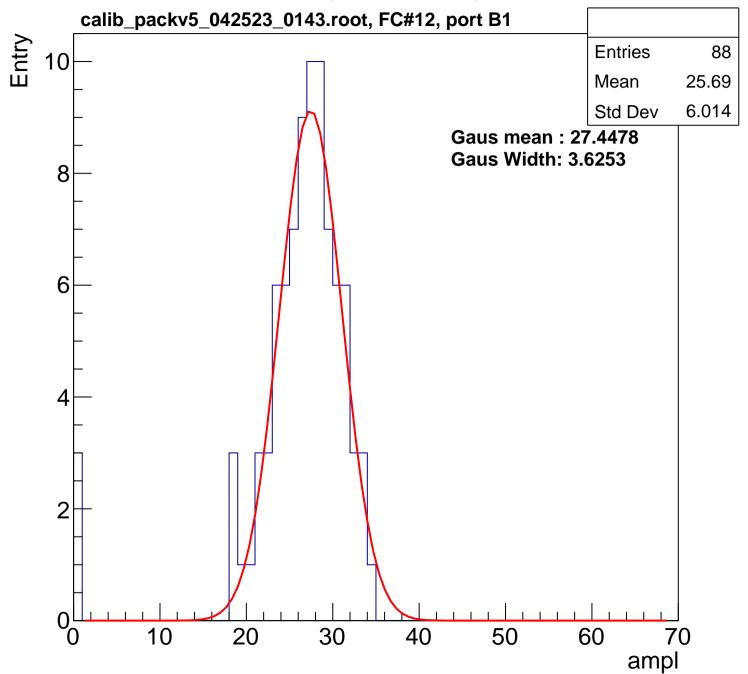


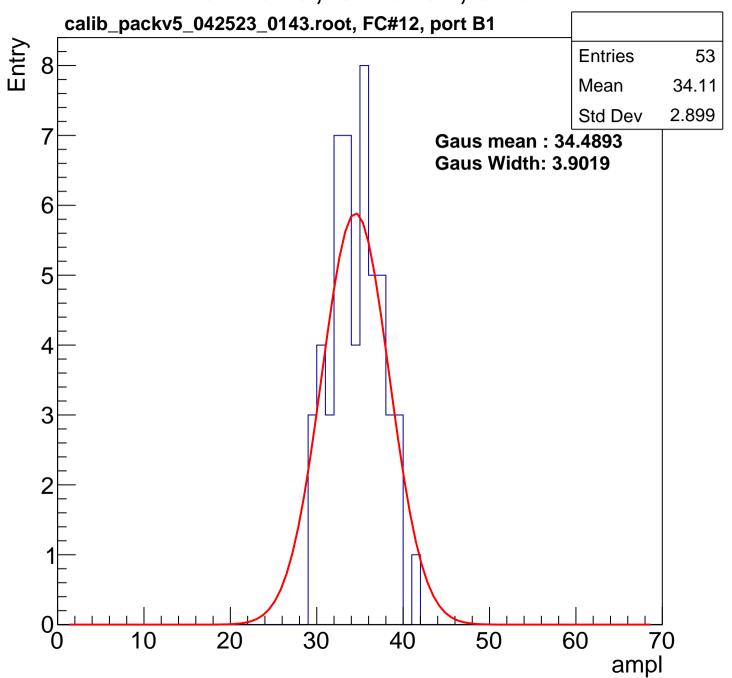


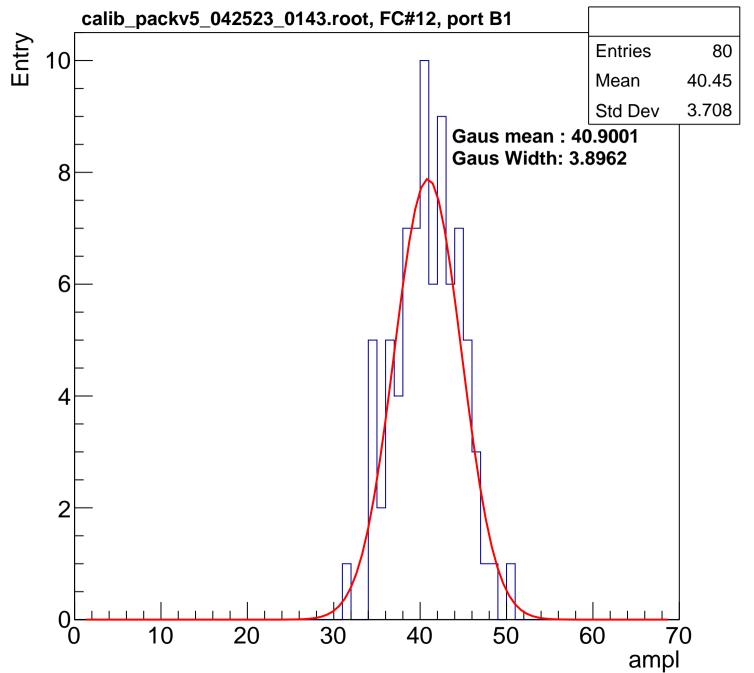


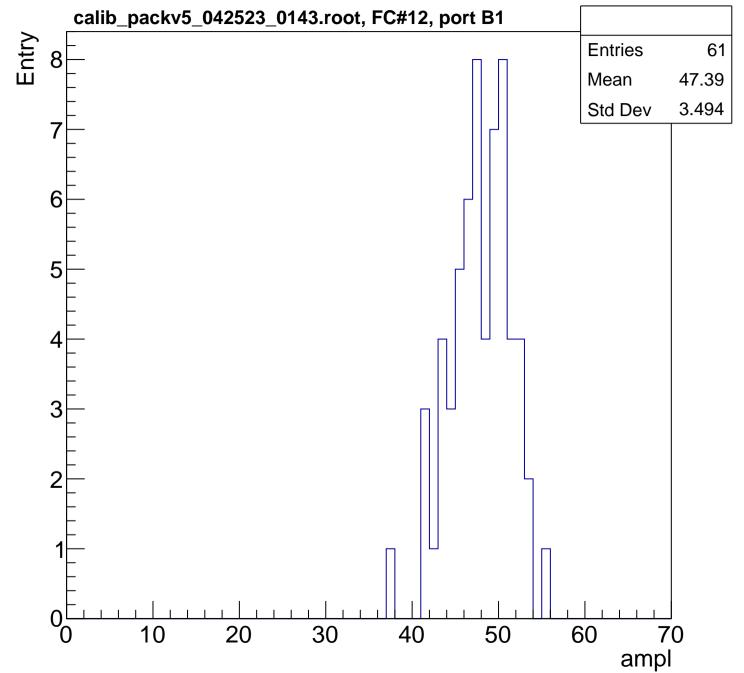
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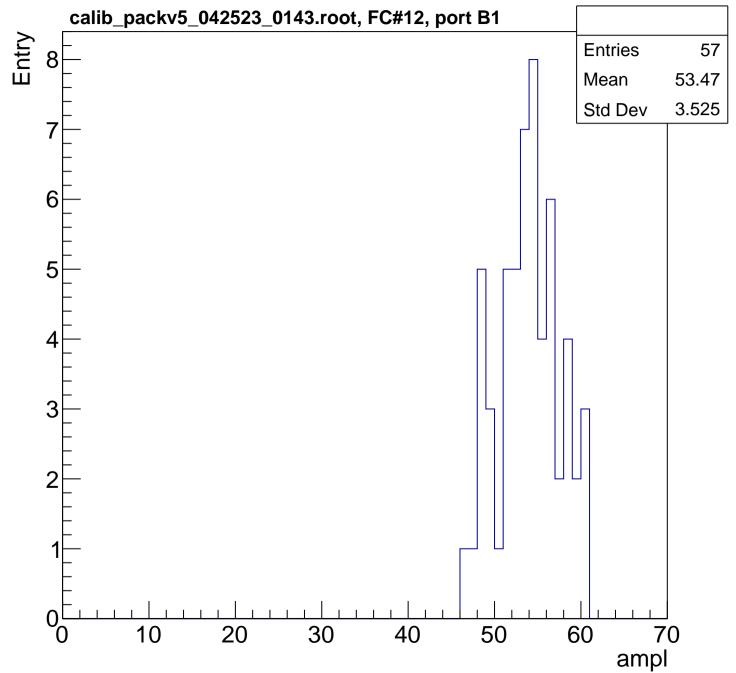


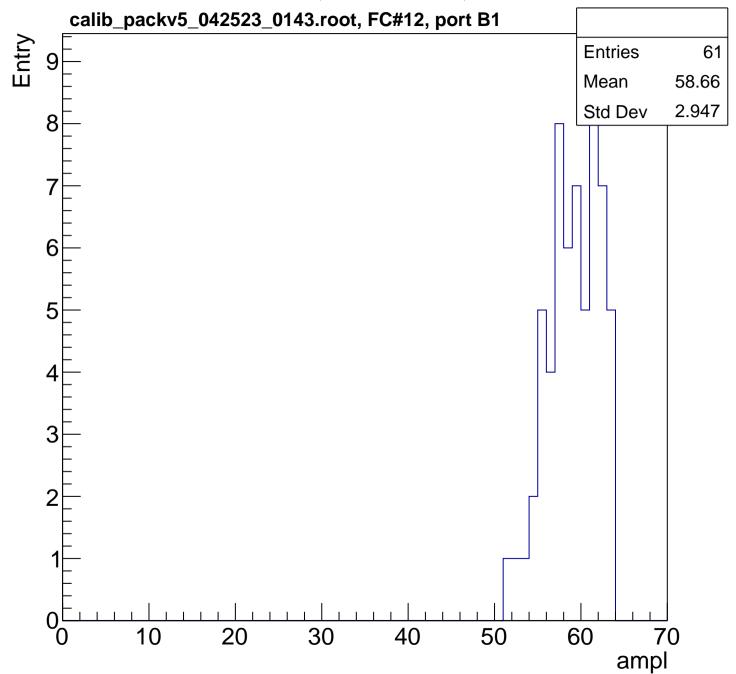


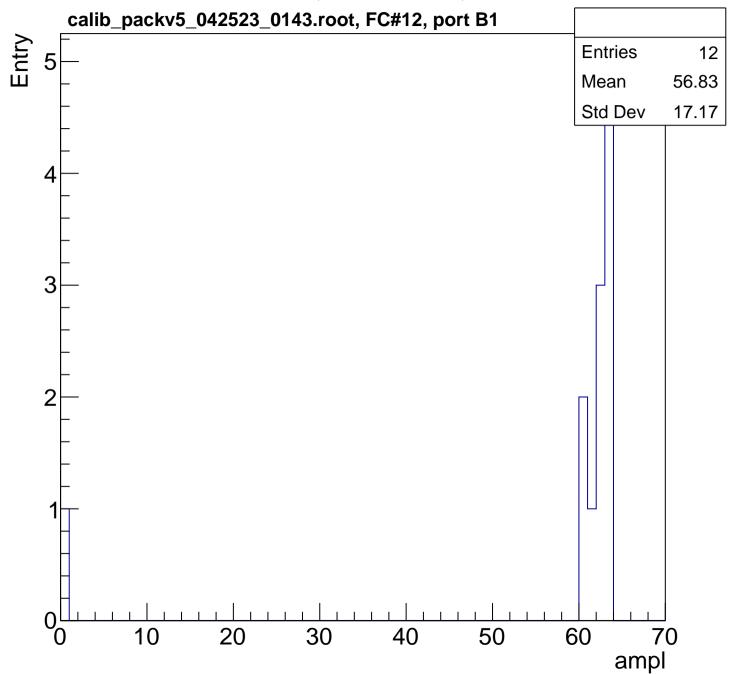


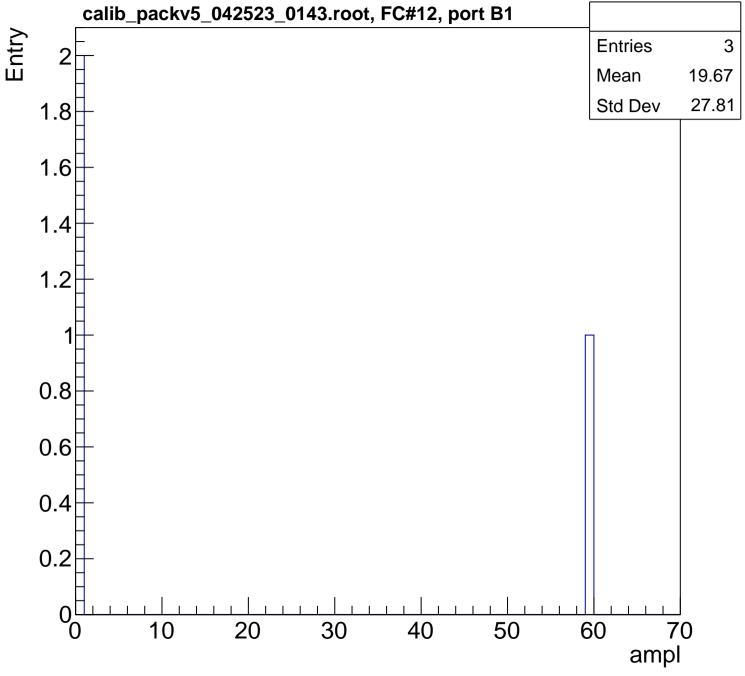


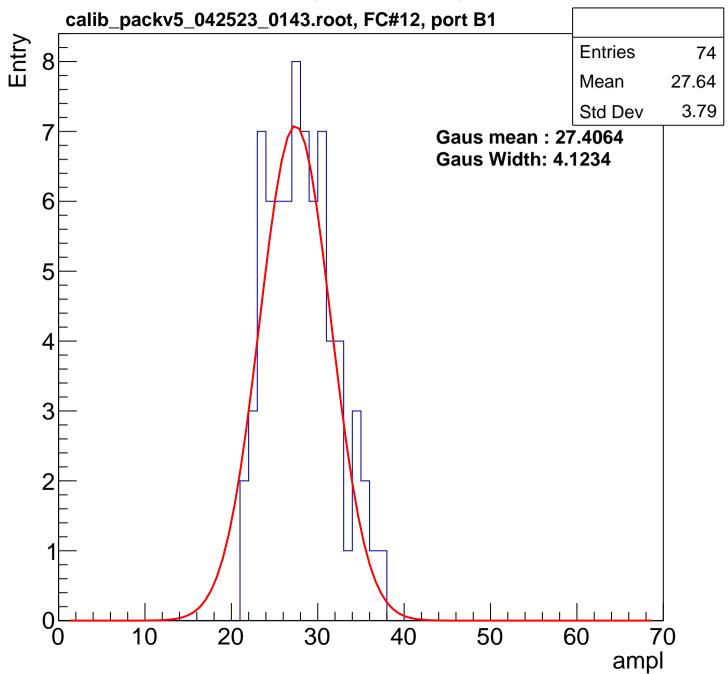


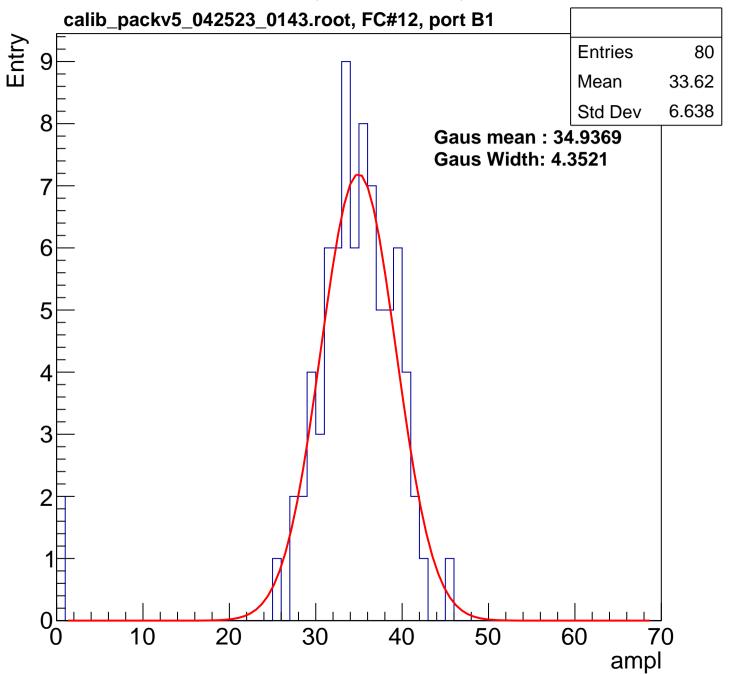


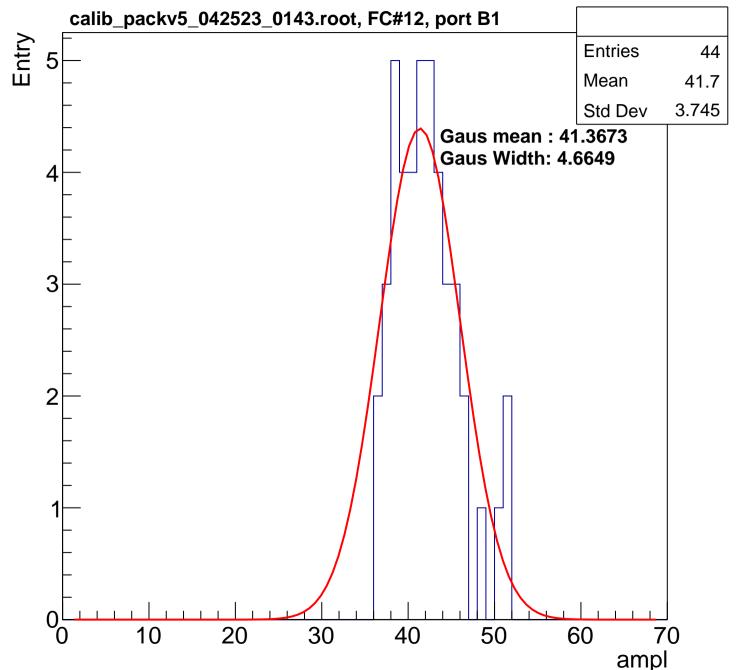


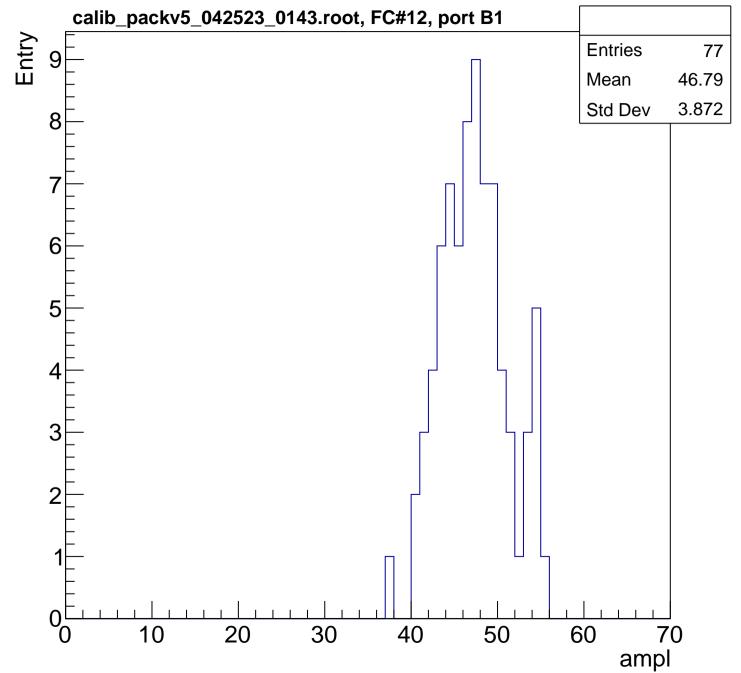


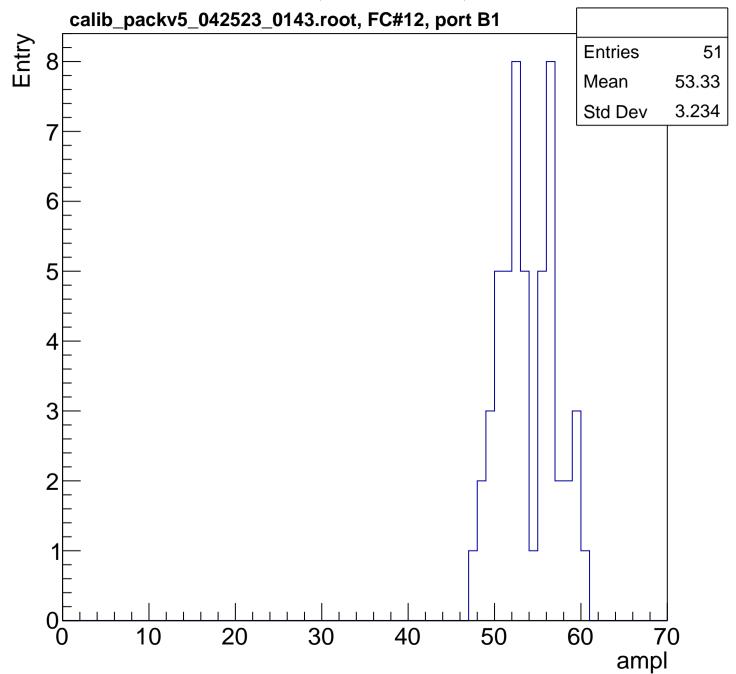


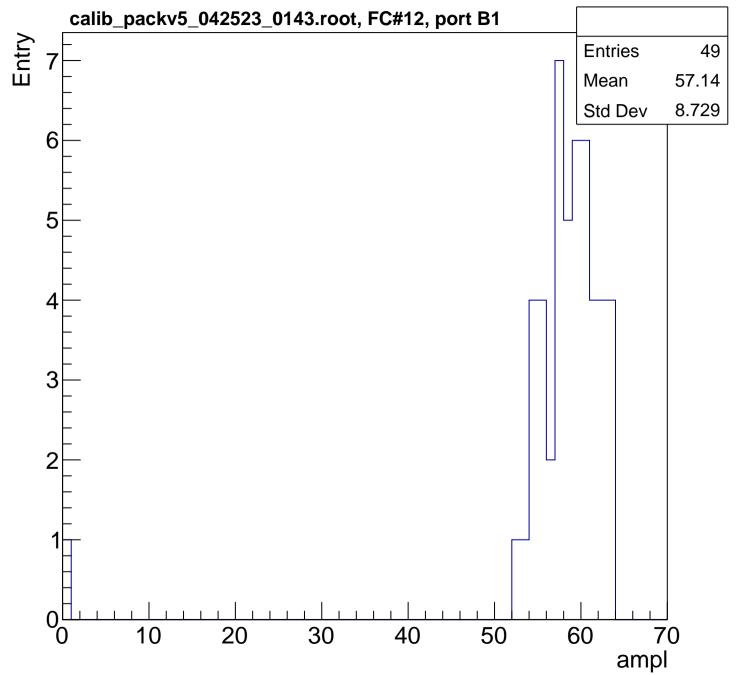


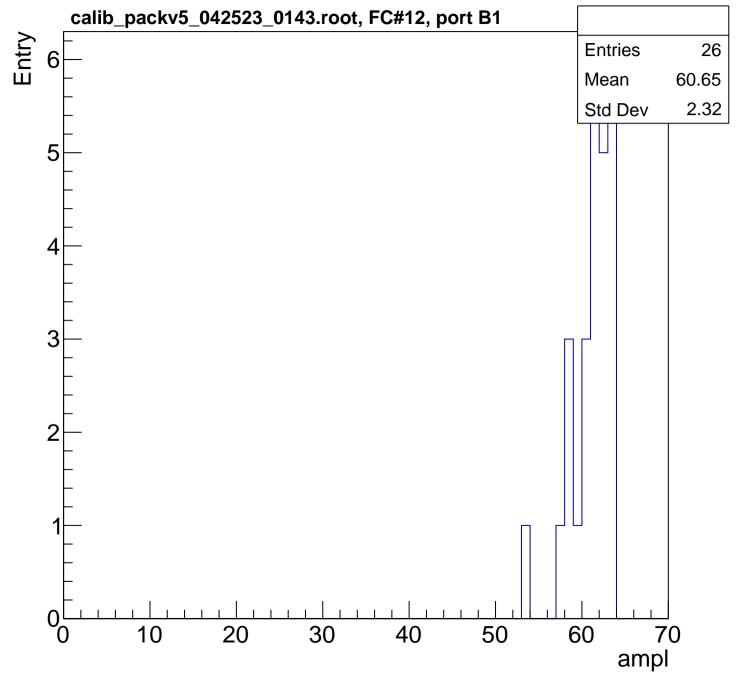


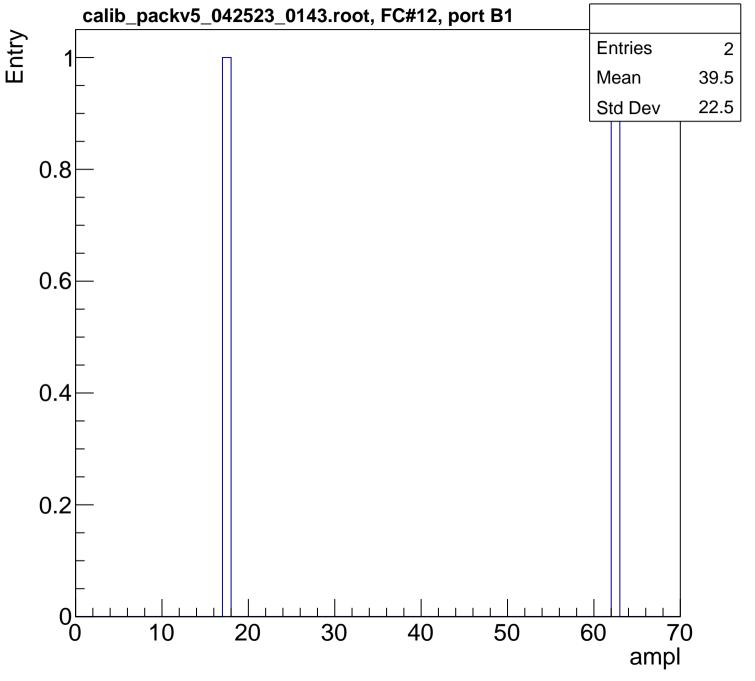


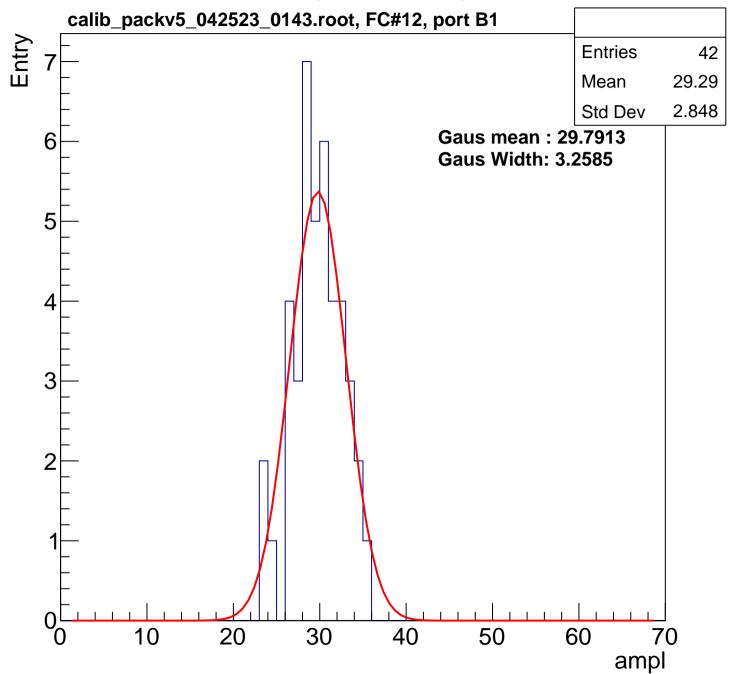


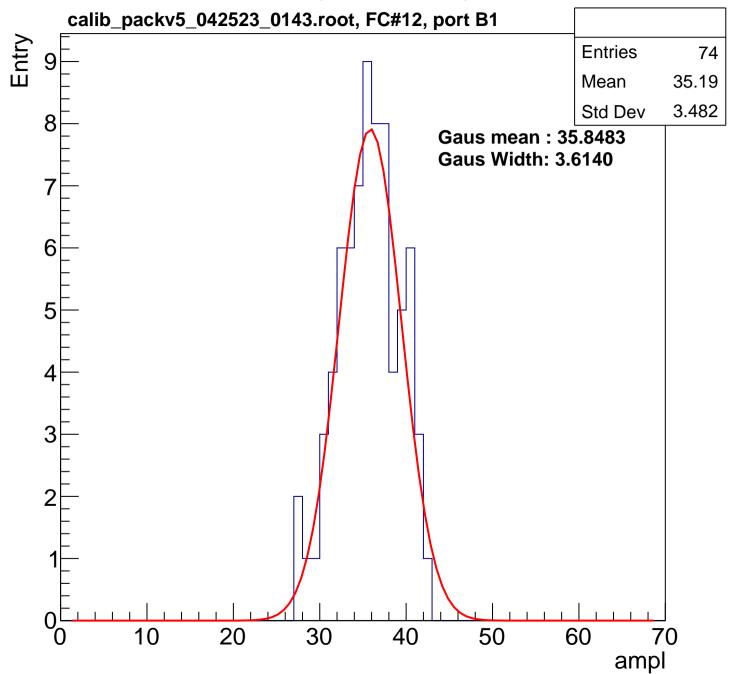


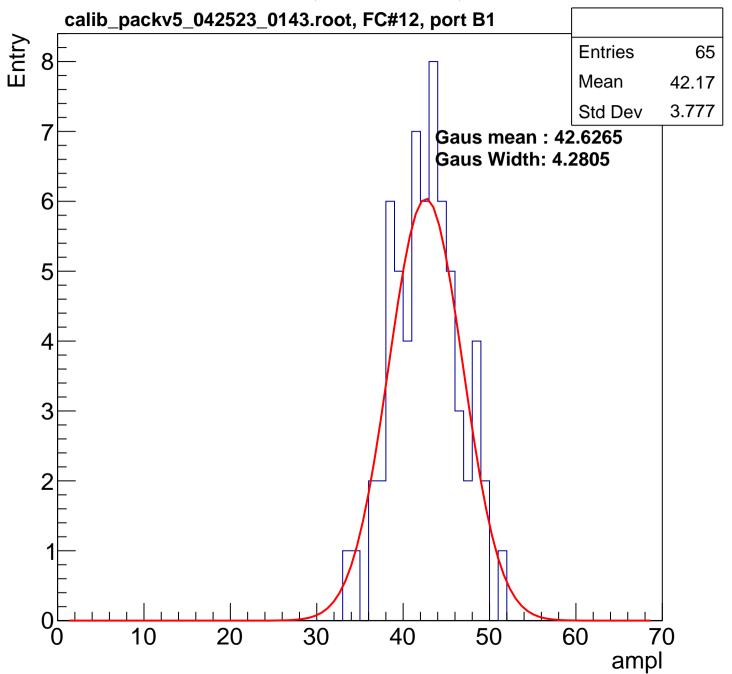


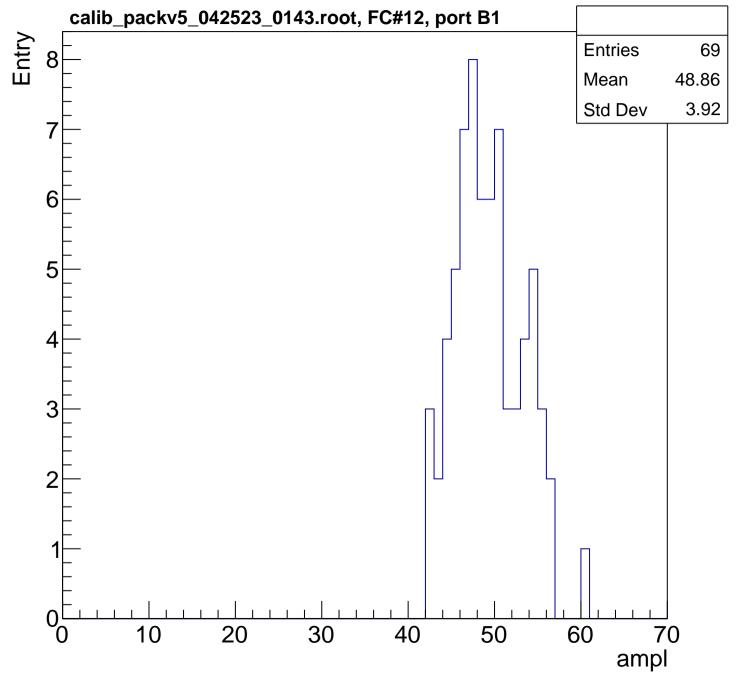


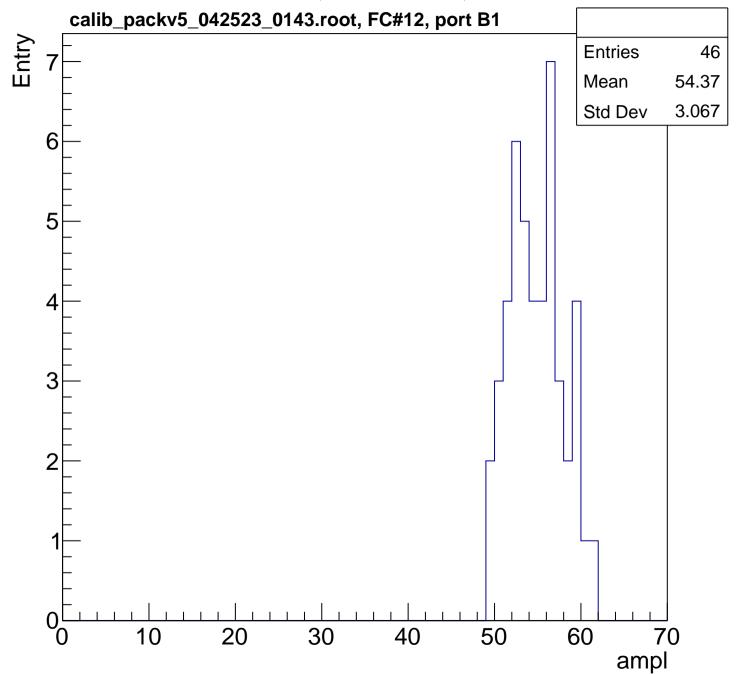


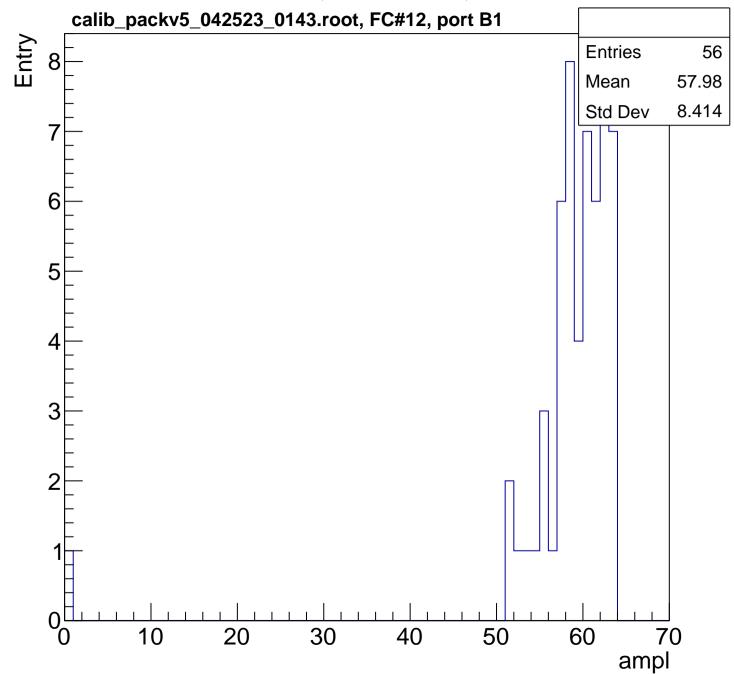


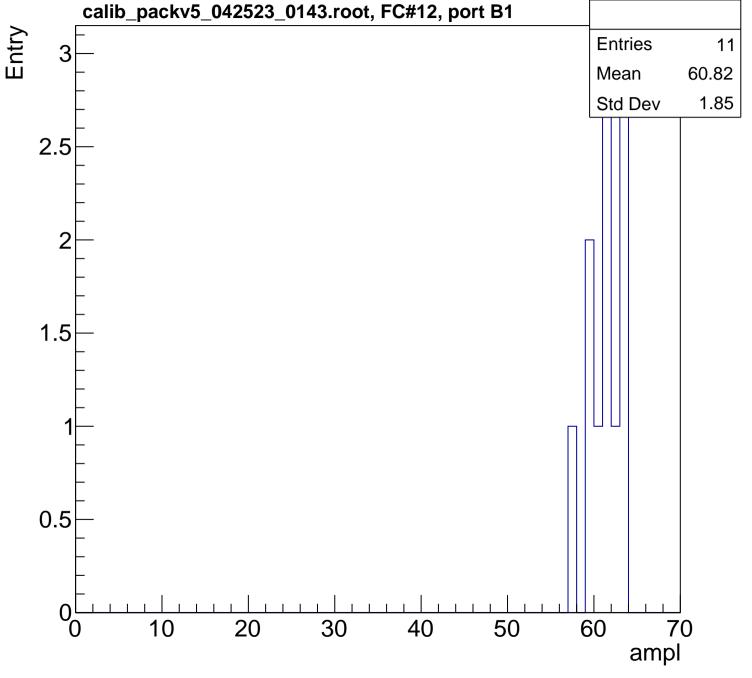












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