



# B1L003S, U11-ch0, adc0

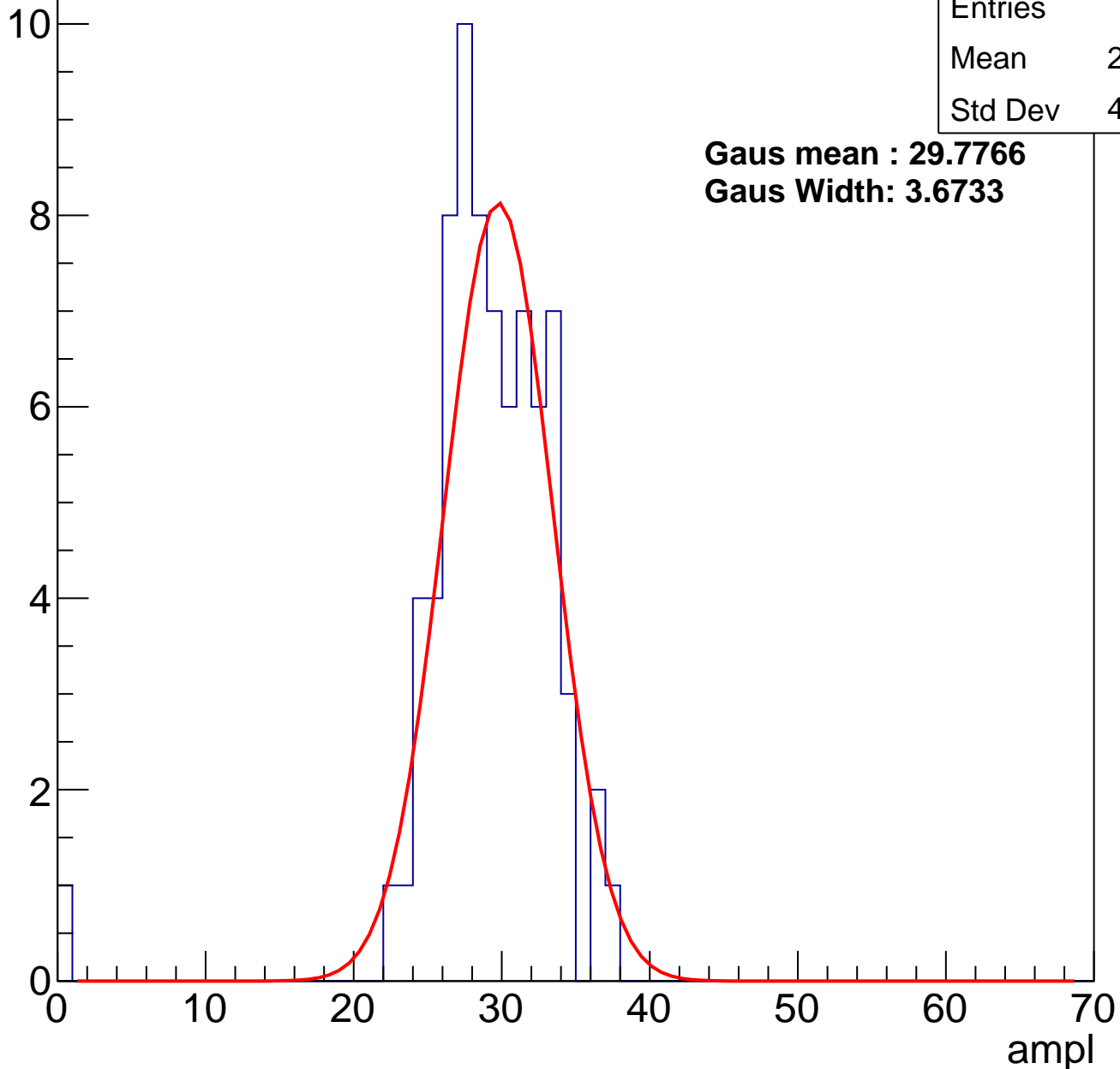
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	76
Mean	28.64
Std Dev	4.642

**Gaus mean : 29.7766**

**Gaus Width: 3.6733**

Entry



# B1L003S, U11-ch0, adc1

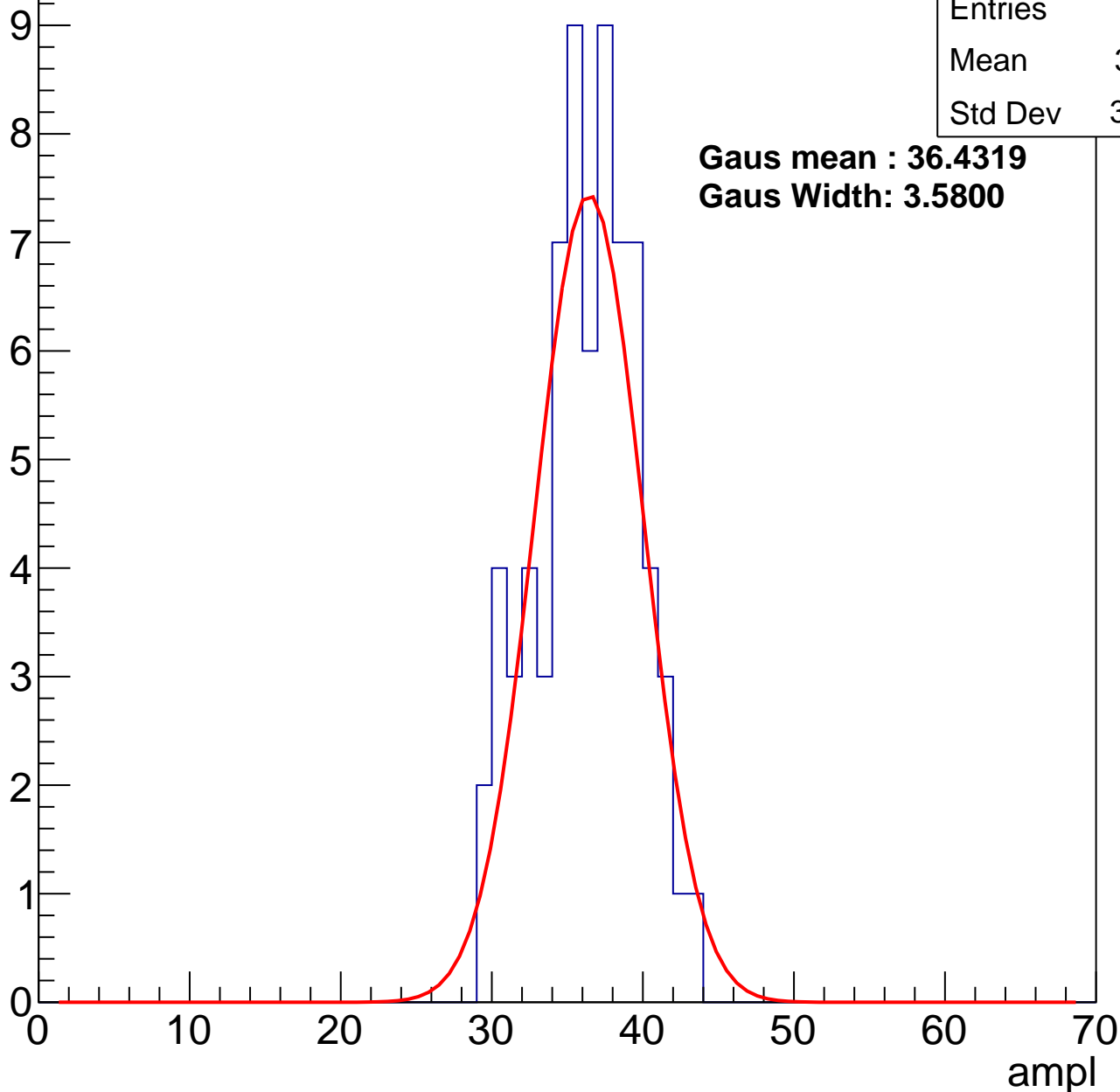
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	35.81
Std Dev	3.309

**Gaus mean : 36.4319**

**Gaus Width: 3.5800**



# B1L003S, U11-ch0, adc2

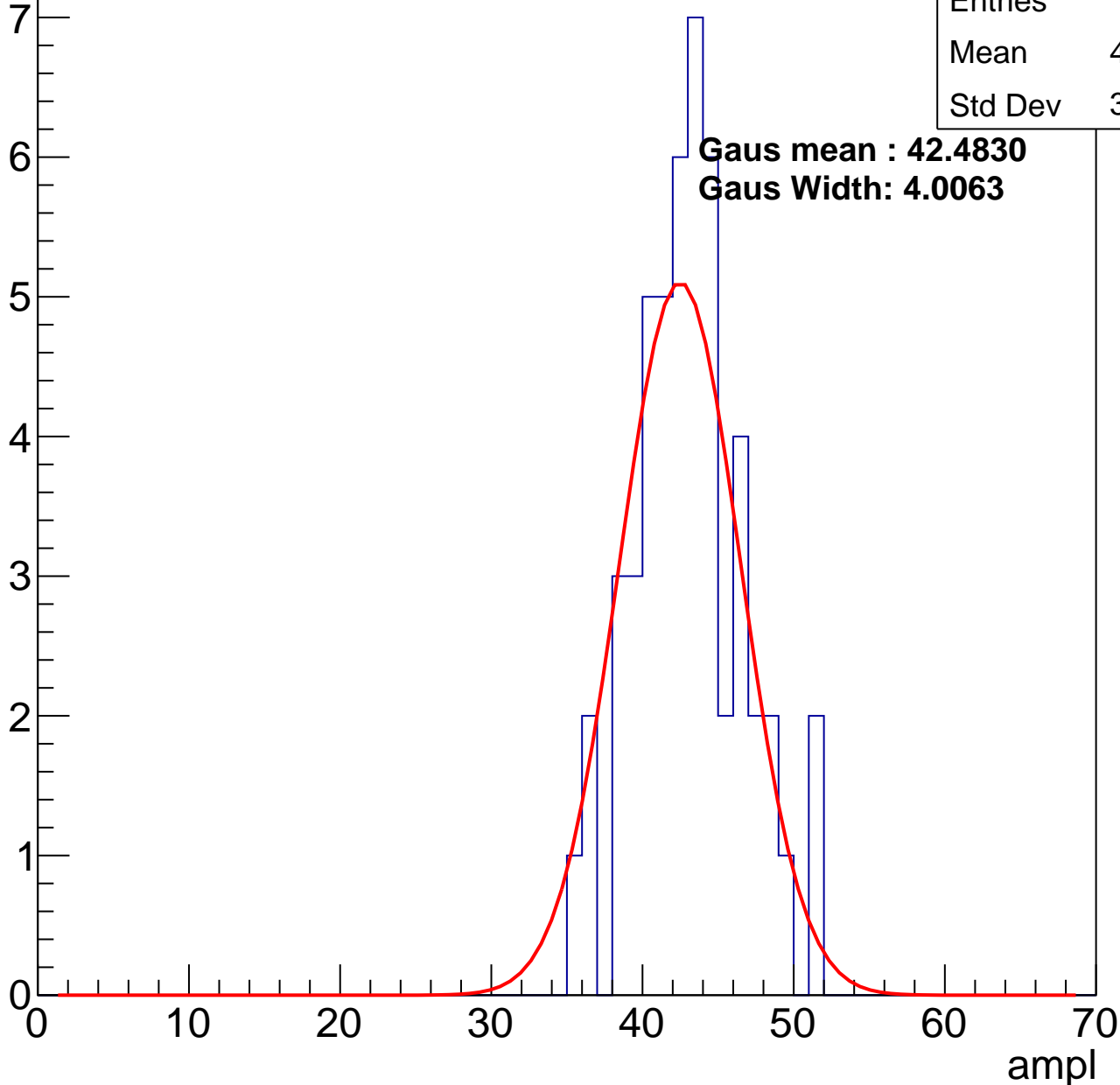
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	51
Mean	42.65
Std Dev	3.558

**Gaus mean : 42.4830**

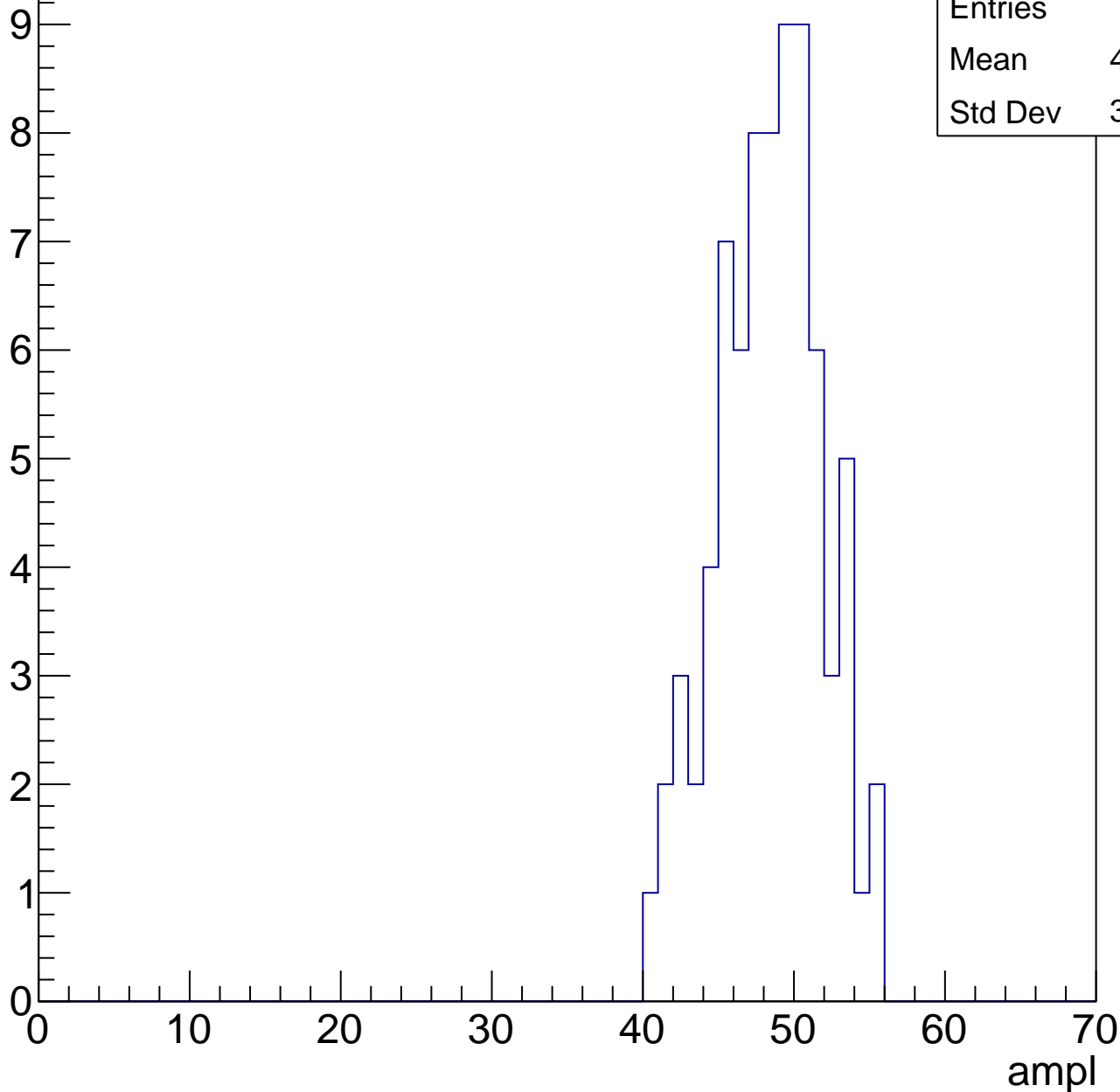
**Gaus Width: 4.0063**



# B1L003S, U11-ch0, adc3

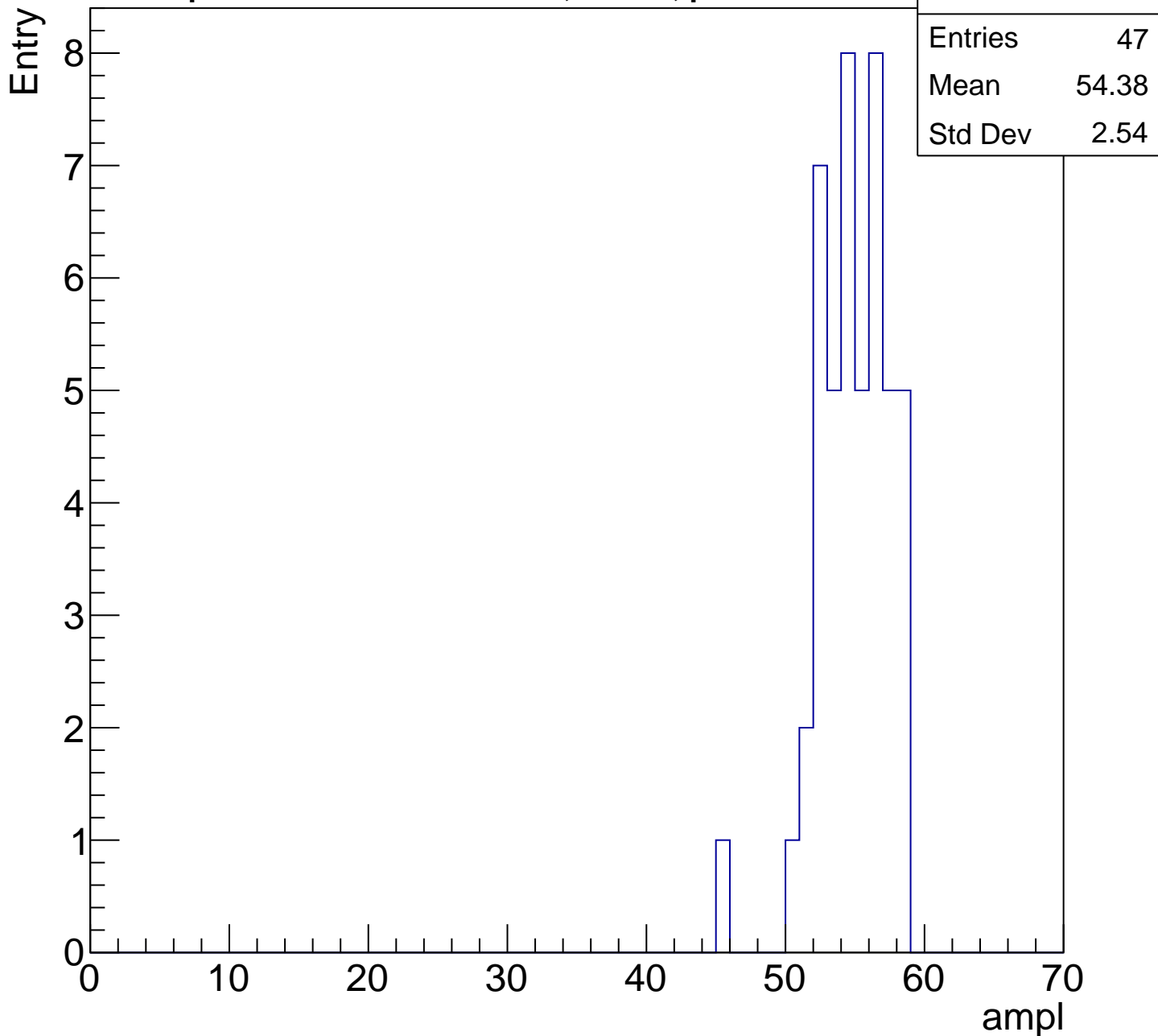
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U11-ch0, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2



# B1L003S, U11-ch0, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

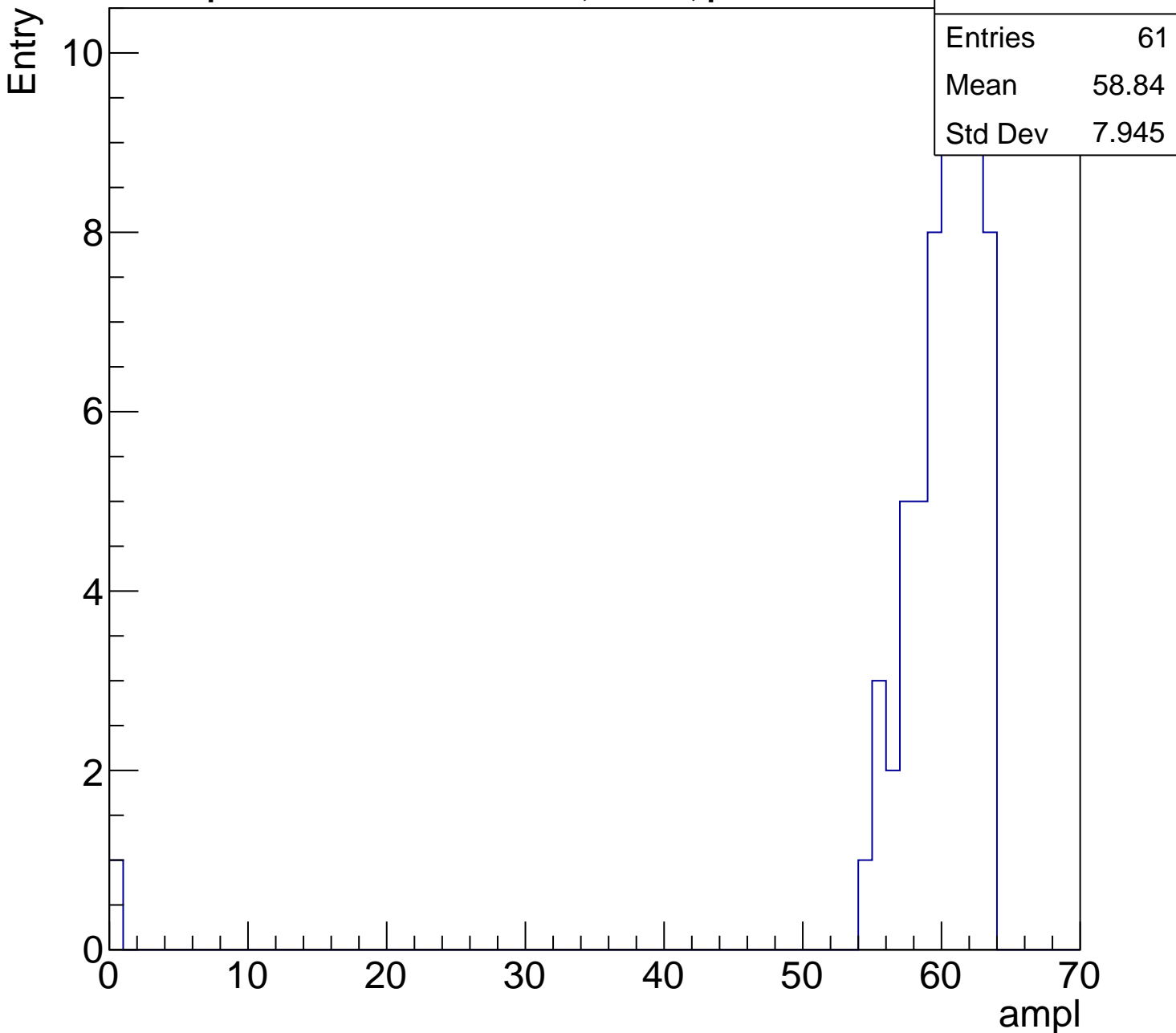
Entries	61
Mean	58.84
Std Dev	7.945

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L003S, U11-ch0, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

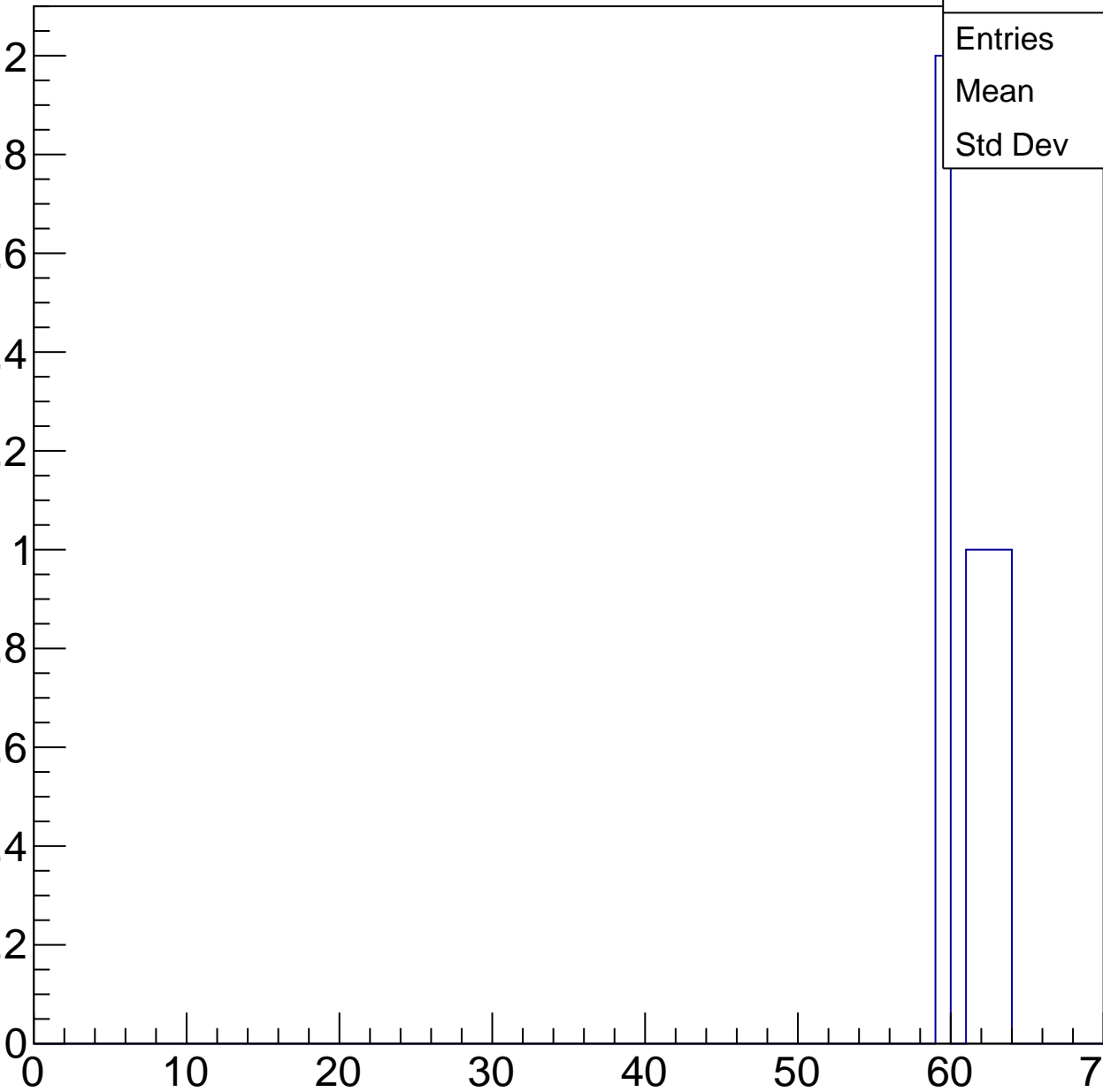
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	60.8
Std Dev	1.6

0 10 20 30 40 50 60 70

ampl

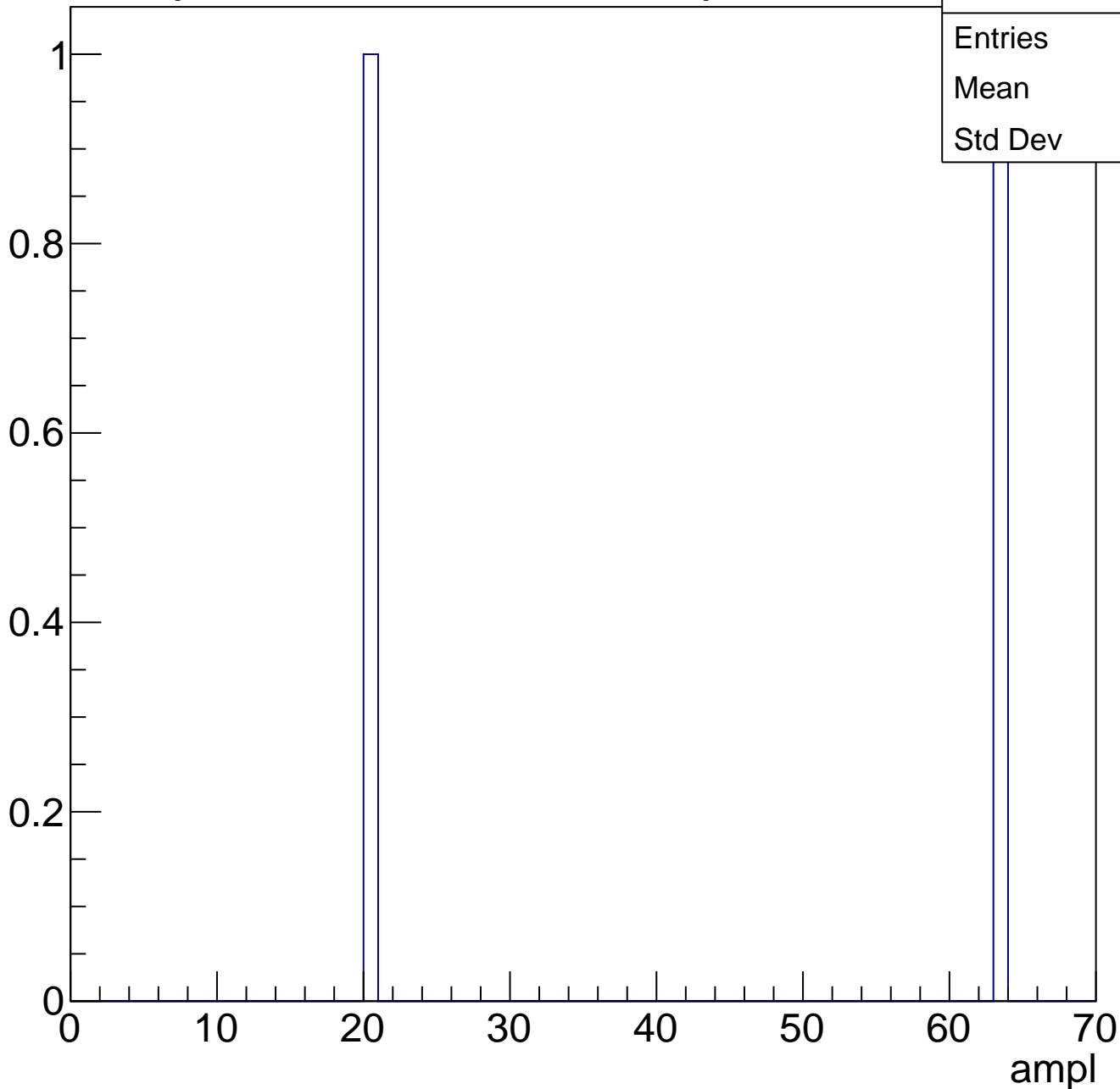




# B1L003S, U11-ch0, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U11-ch1, adc0

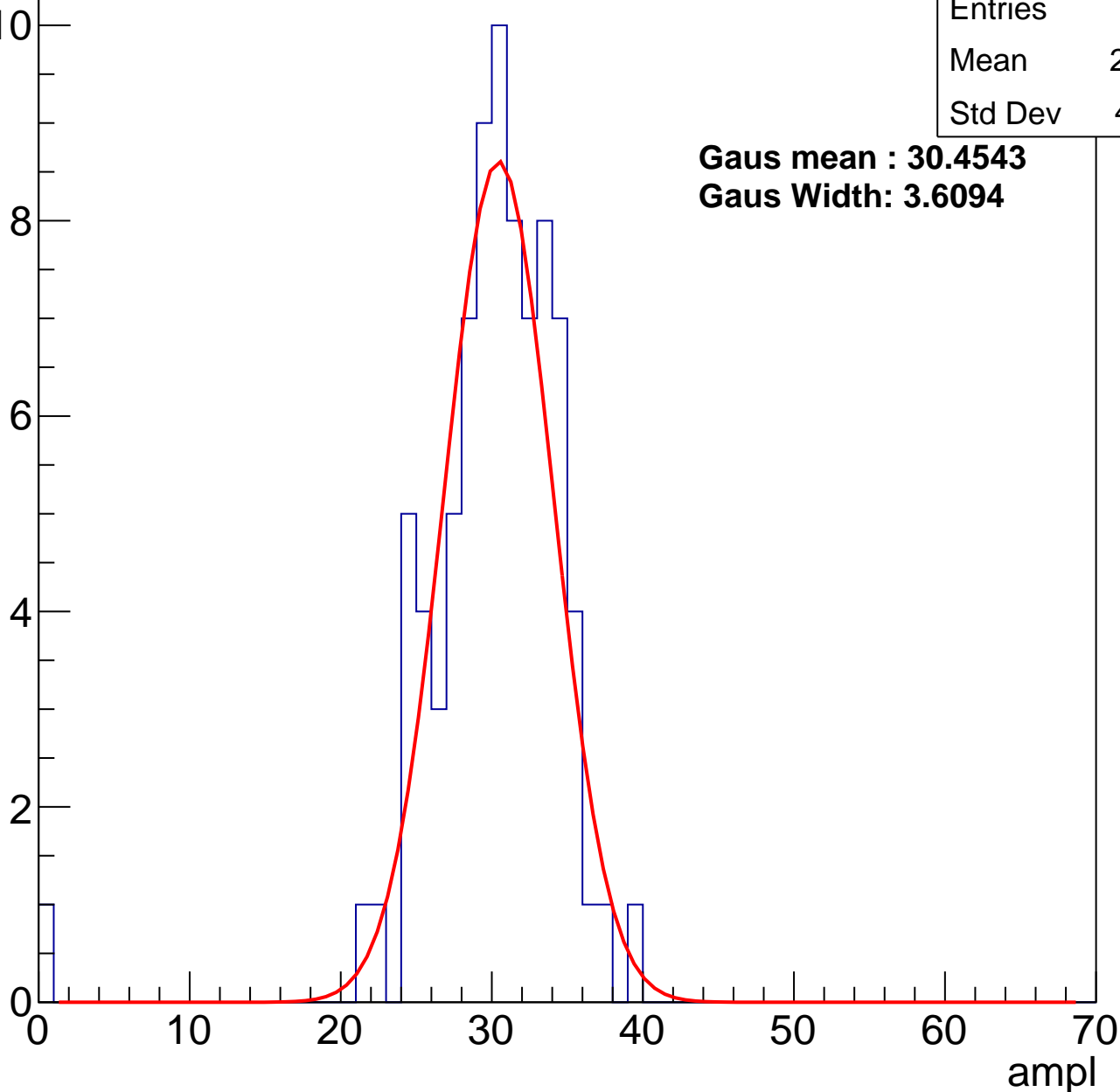
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	83
Mean	29.63
Std Dev	4.821

**Gaus mean : 30.4543**

**Gaus Width: 3.6094**



# B1L003S, U11-ch1, adc1

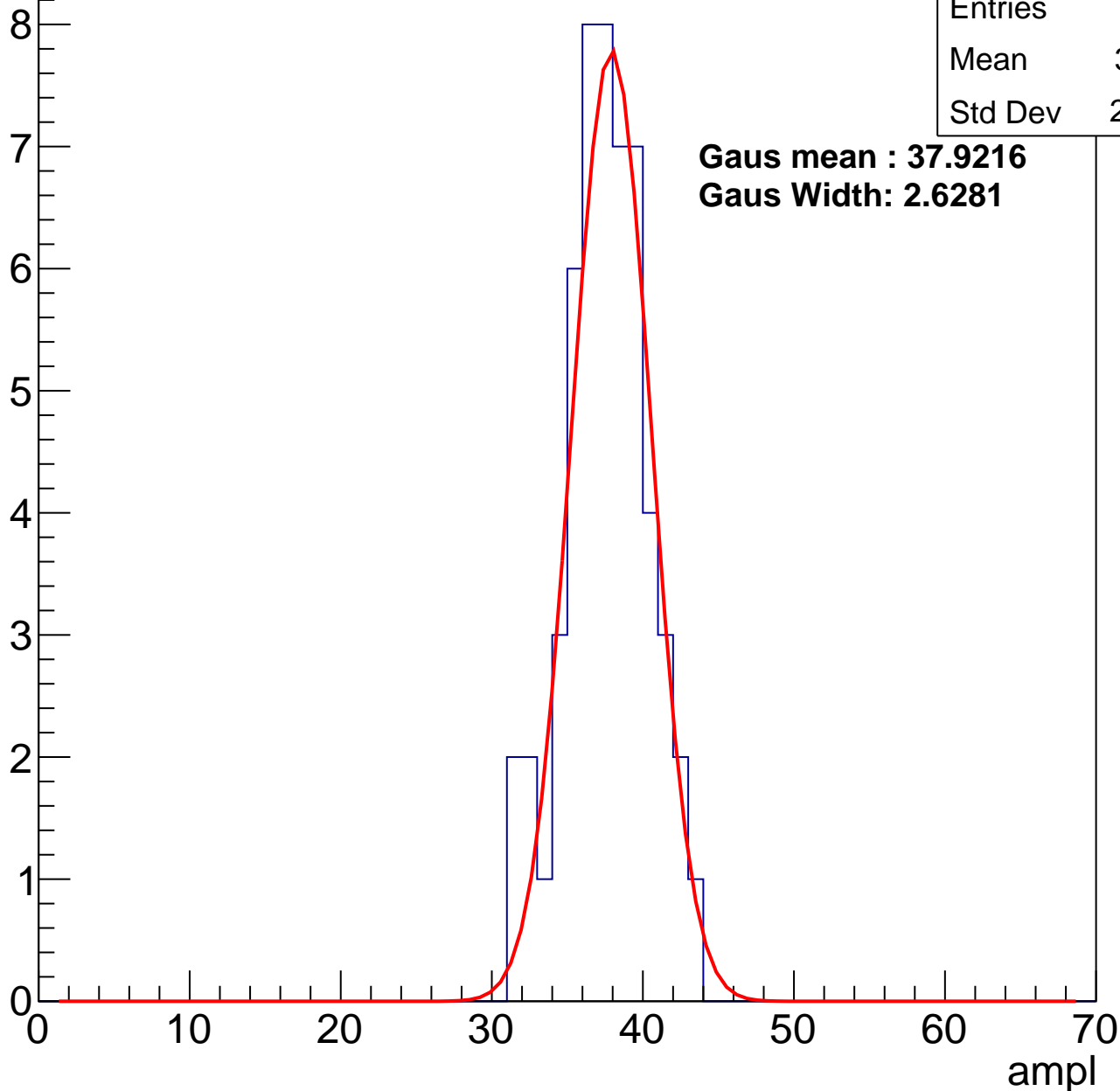
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	54
Mean	37.11
Std Dev	2.726

**Gaus mean : 37.9216**

**Gaus Width: 2.6281**



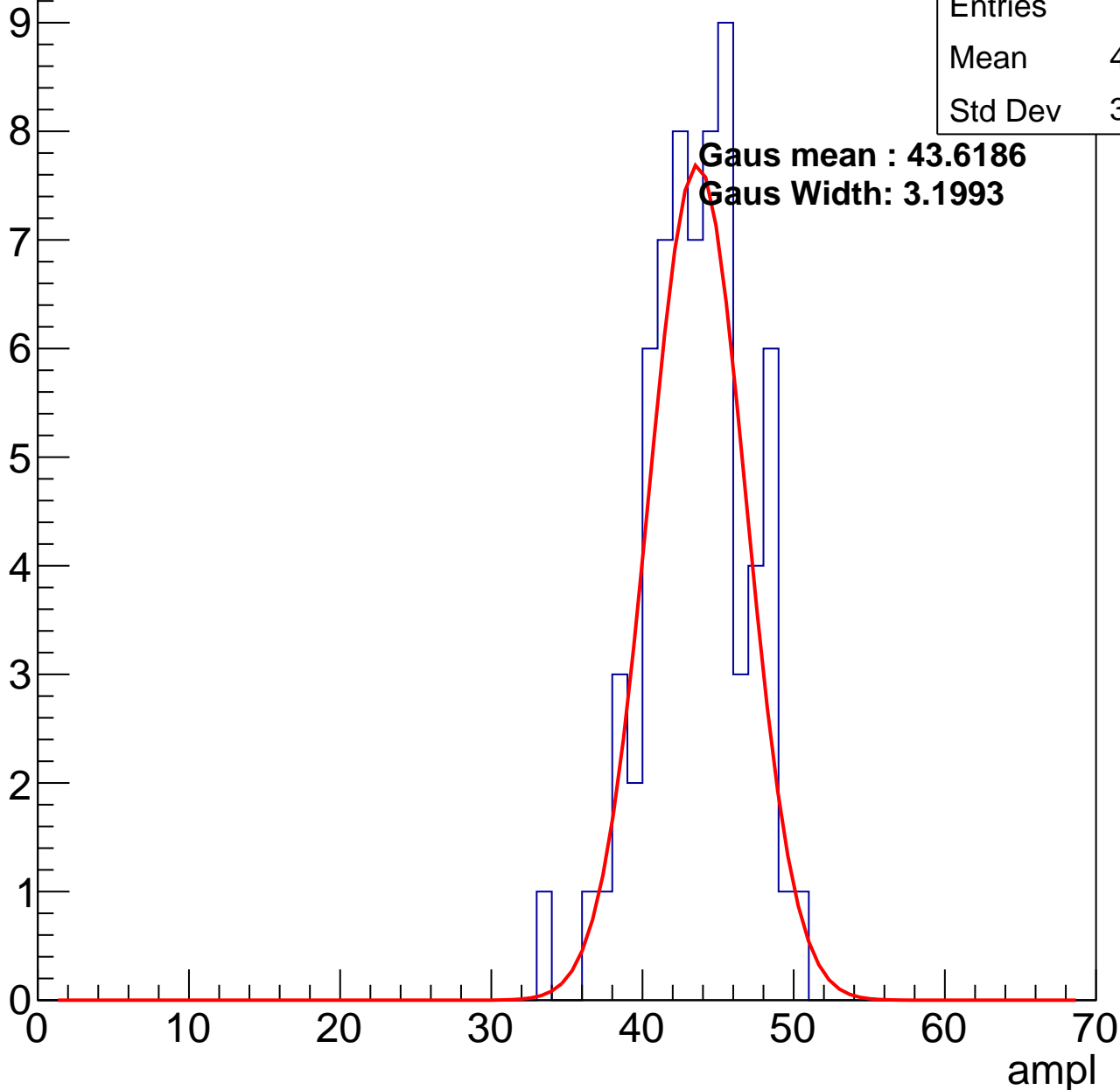
# B1L003S, U11-ch1, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	43.12
Std Dev	3.323

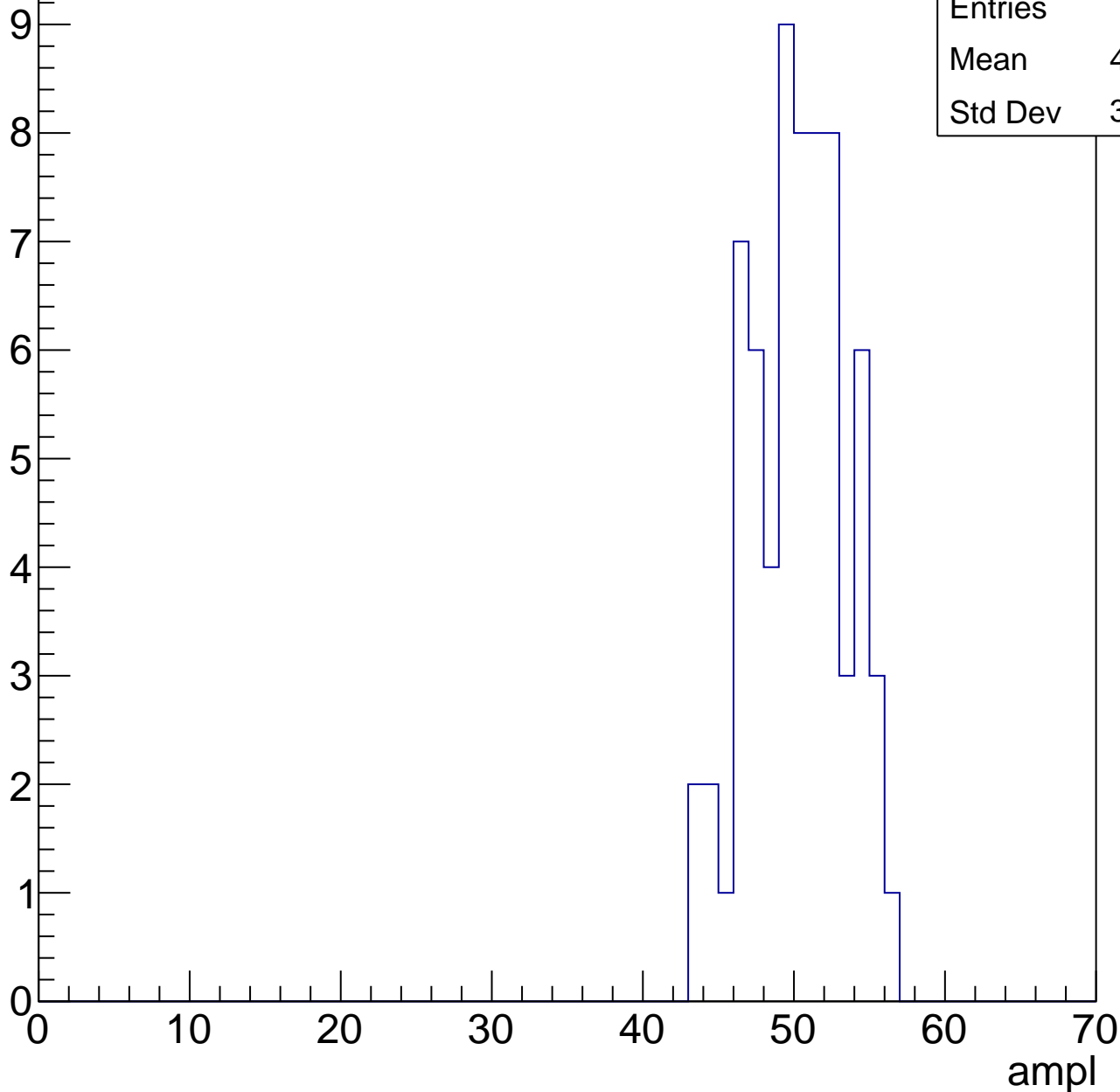
**Gaus mean : 43.6186**  
**Gaus Width: 3.1993**



# B1L003S, U11-ch1, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



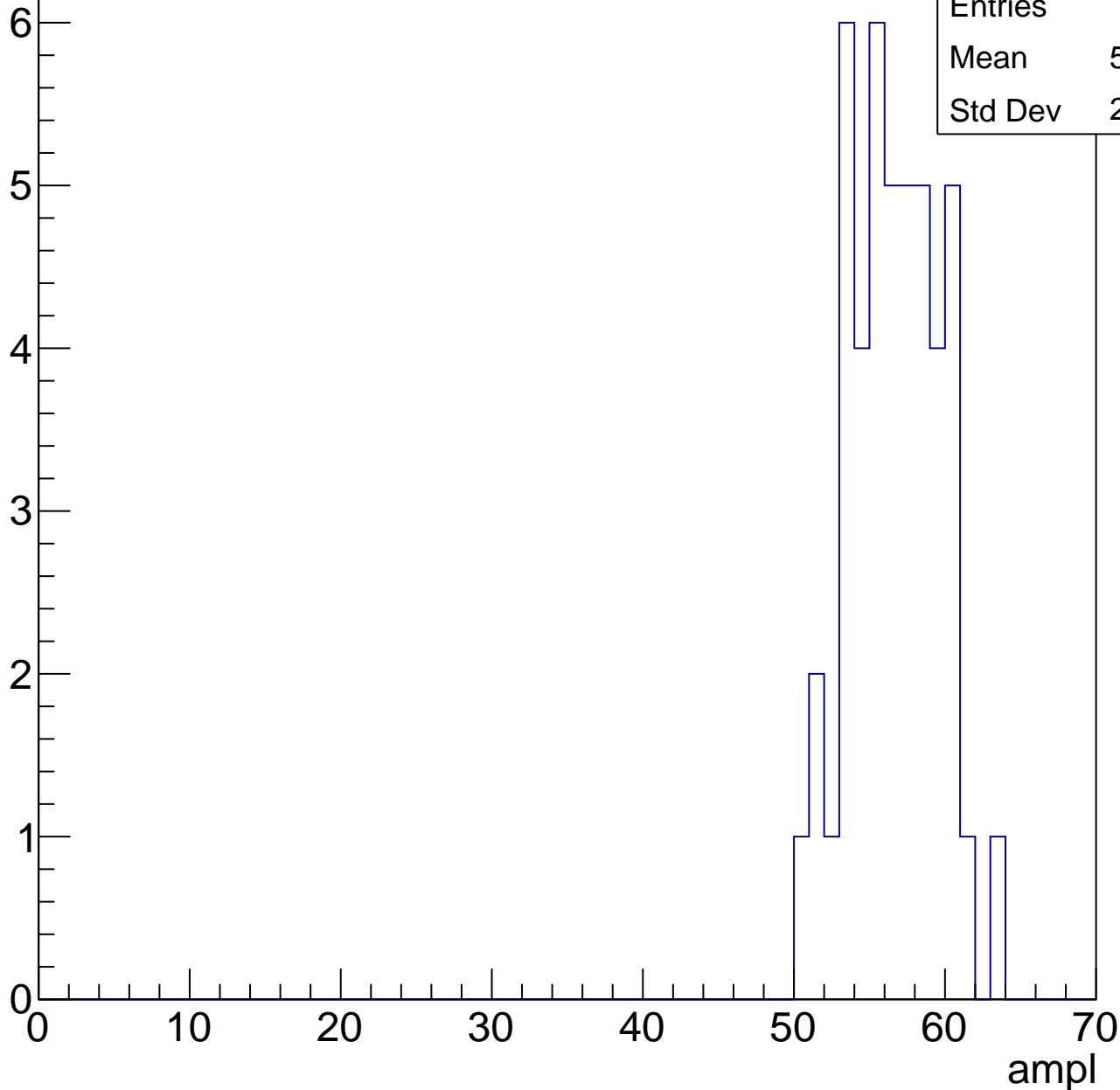
Entries	68
Mean	49.76
Std Dev	3.107

# B1L003S, U11-ch1, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	46
Mean	56.15
Std Dev	2.919

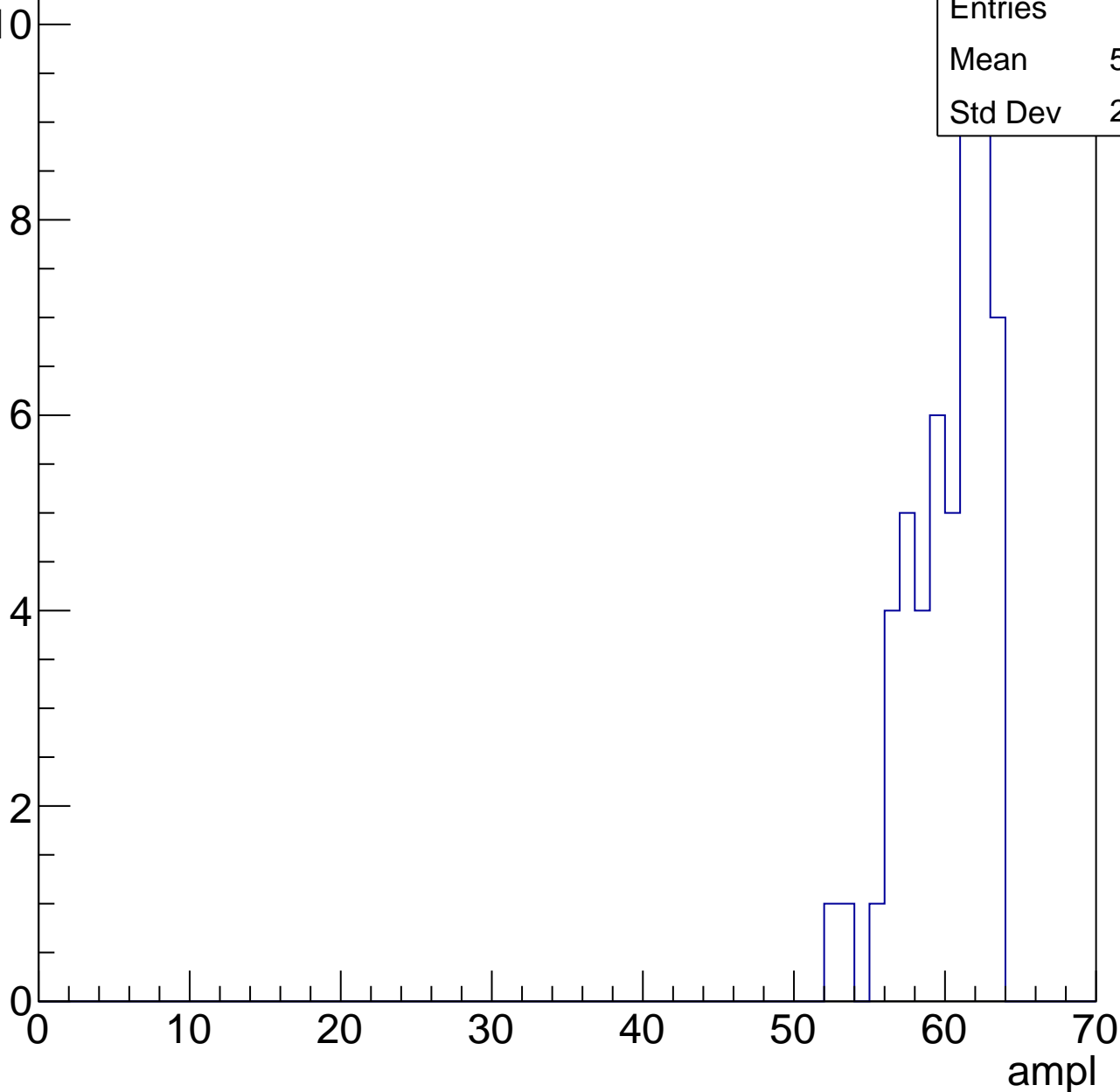


# B1L003S, U11-ch1, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

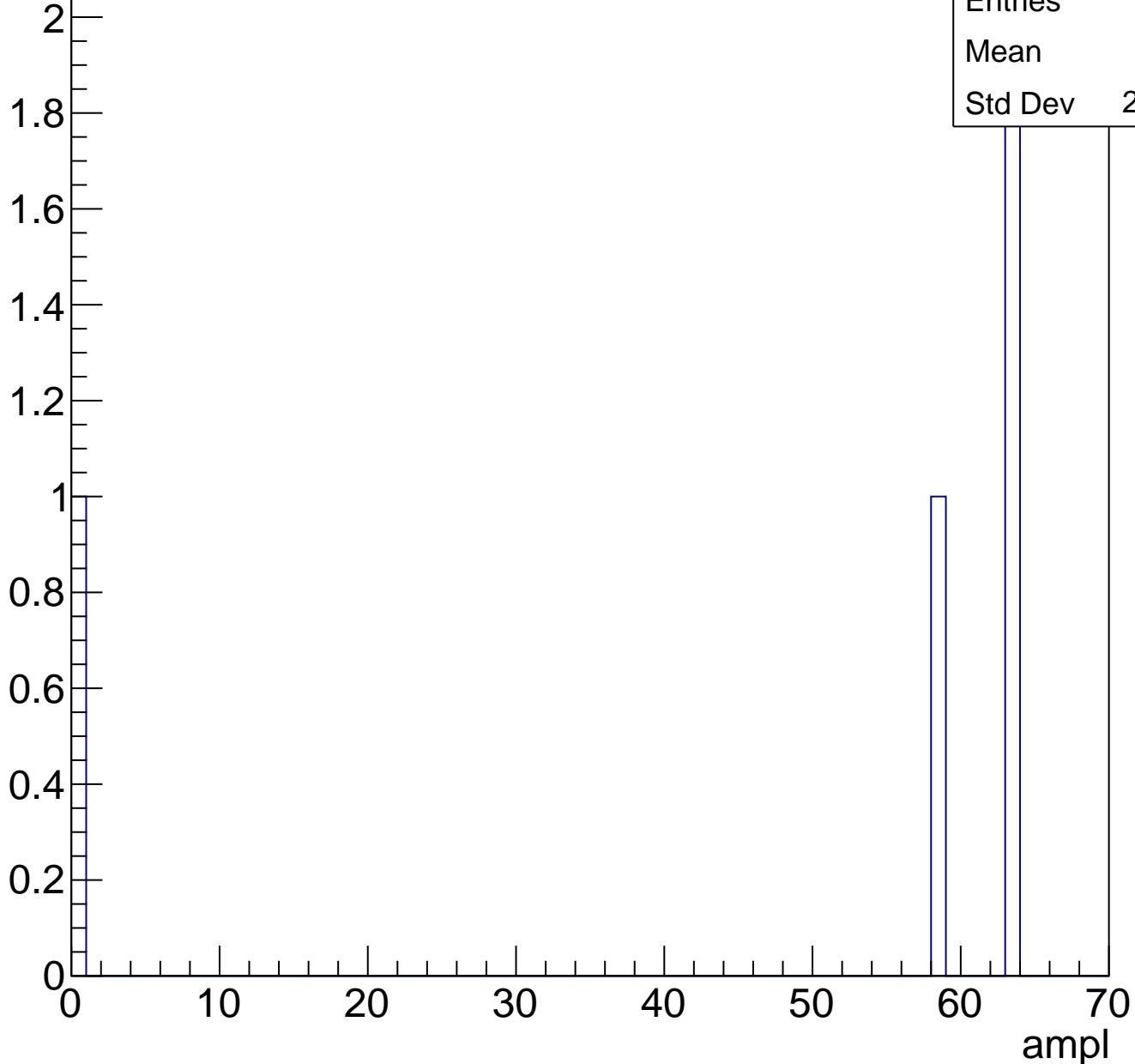
Entries	53
Mean	59.72
Std Dev	2.666



# B1L003S, U11-ch1, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	4
Mean	46
Std Dev	26.64



# B1L003S, U11-ch1, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U11-ch2, adc0

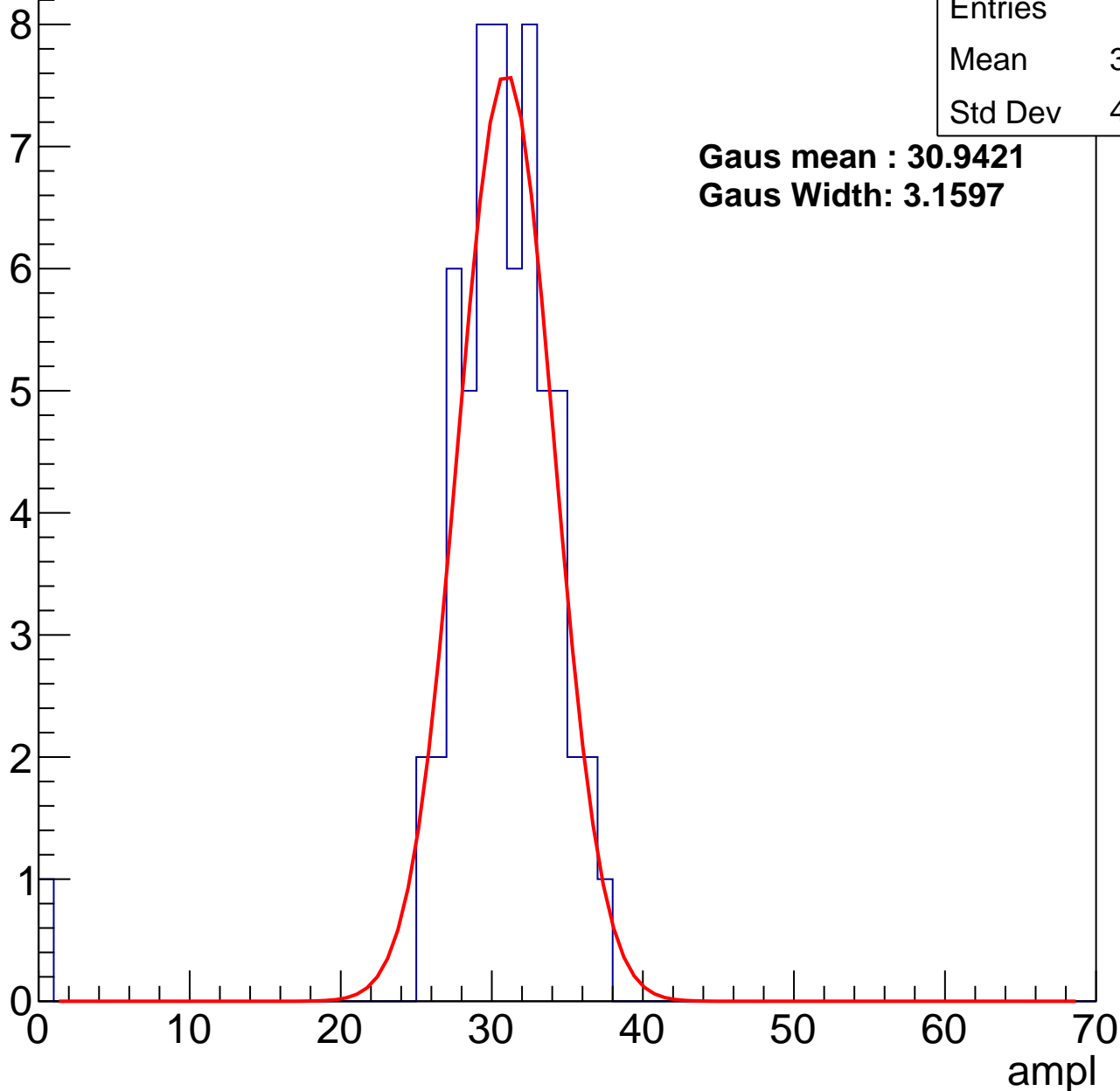
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	30.03
Std Dev	4.787

**Gaus mean : 30.9421**

**Gaus Width: 3.1597**



# B1L003S, U11-ch2, adc1

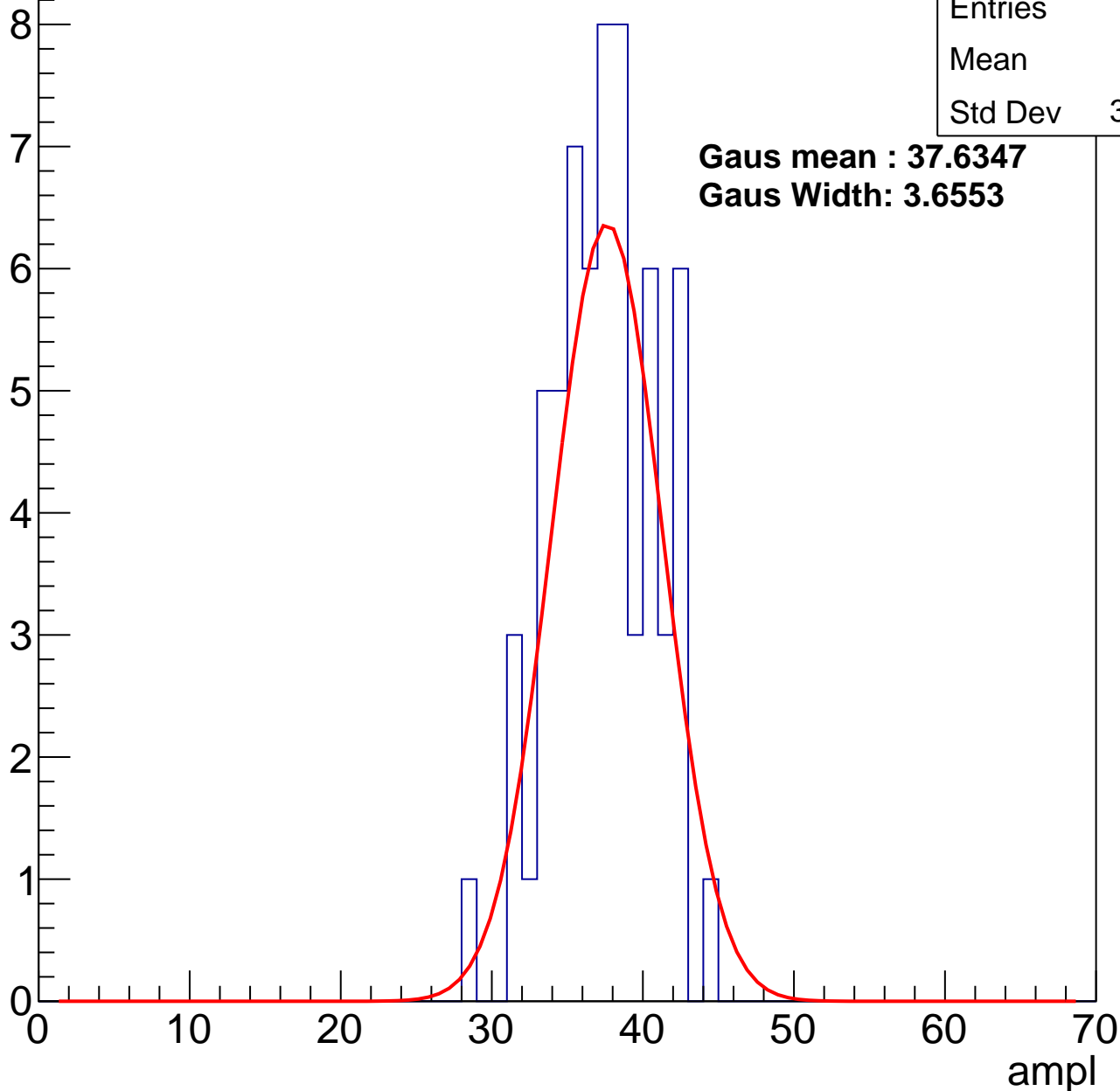
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	36.9
Std Dev	3.318

**Gaus mean : 37.6347**

**Gaus Width: 3.6553**



# B1L003S, U11-ch2, adc2

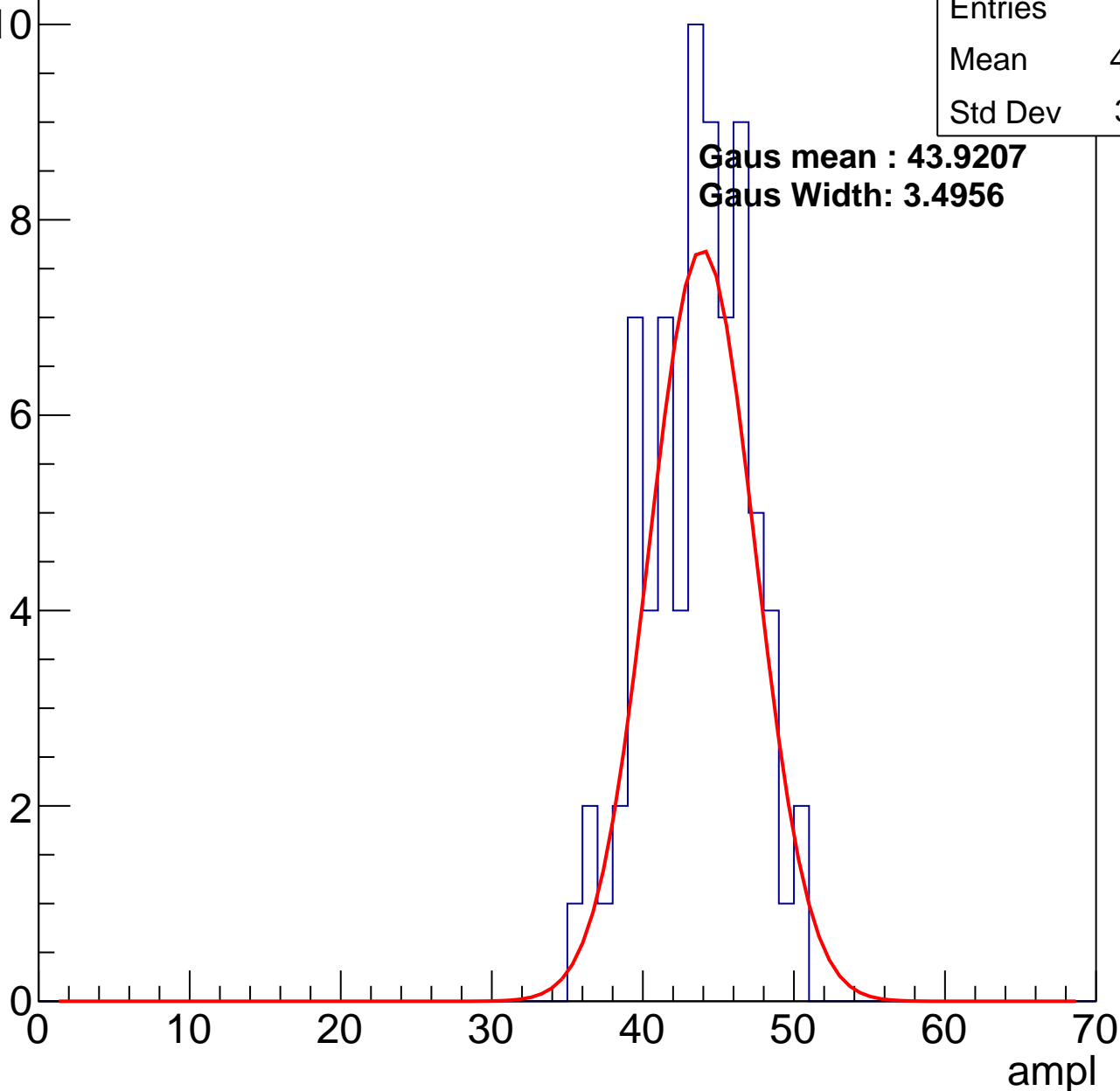
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	75
Mean	43.19
Std Dev	3.381

**Gaus mean : 43.9207**

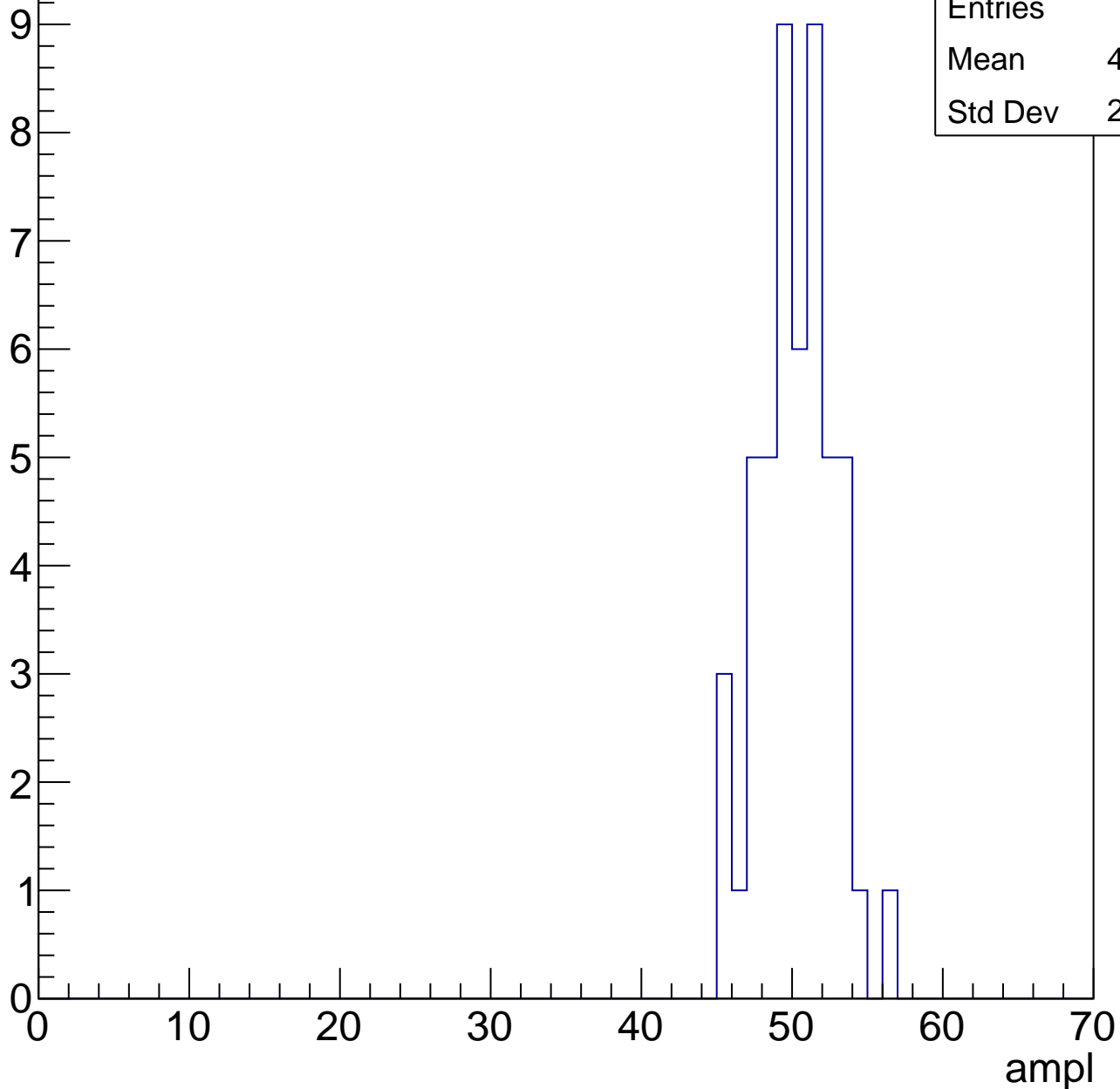
**Gaus Width: 3.4956**



# B1L003S, U11-ch2, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	50
Mean	49.82
Std Dev	2.406

# B1L003S, U11-ch2, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	66
Mean	54.97
Std Dev	7.439

Entry

10

8

6

4

2

0

0

10

20

30

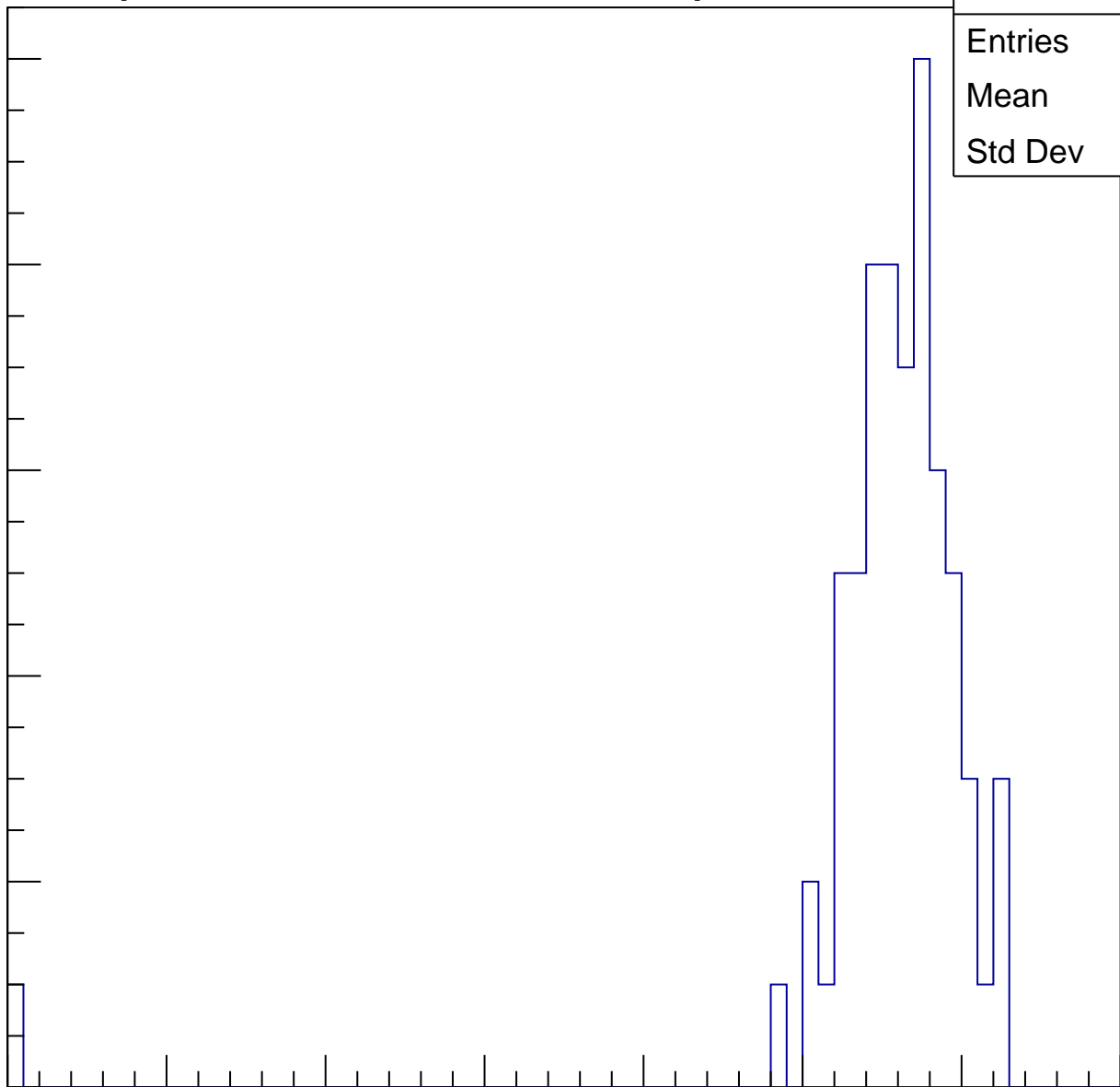
40

50

60

70

ampl

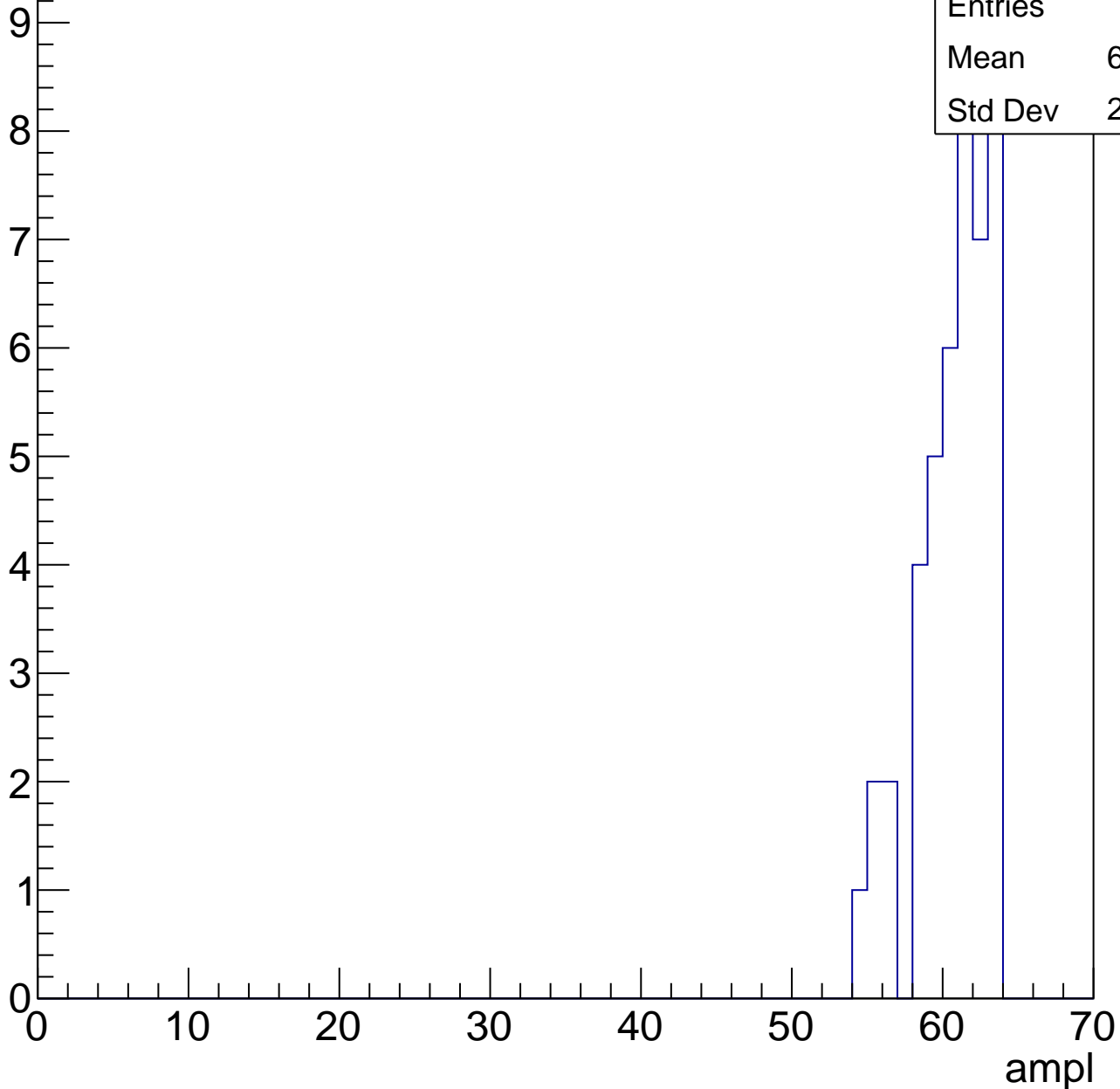


# B1L003S, U11-ch2, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	44
Mean	60.23
Std Dev	2.363



# B1L003S, U11-ch2, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



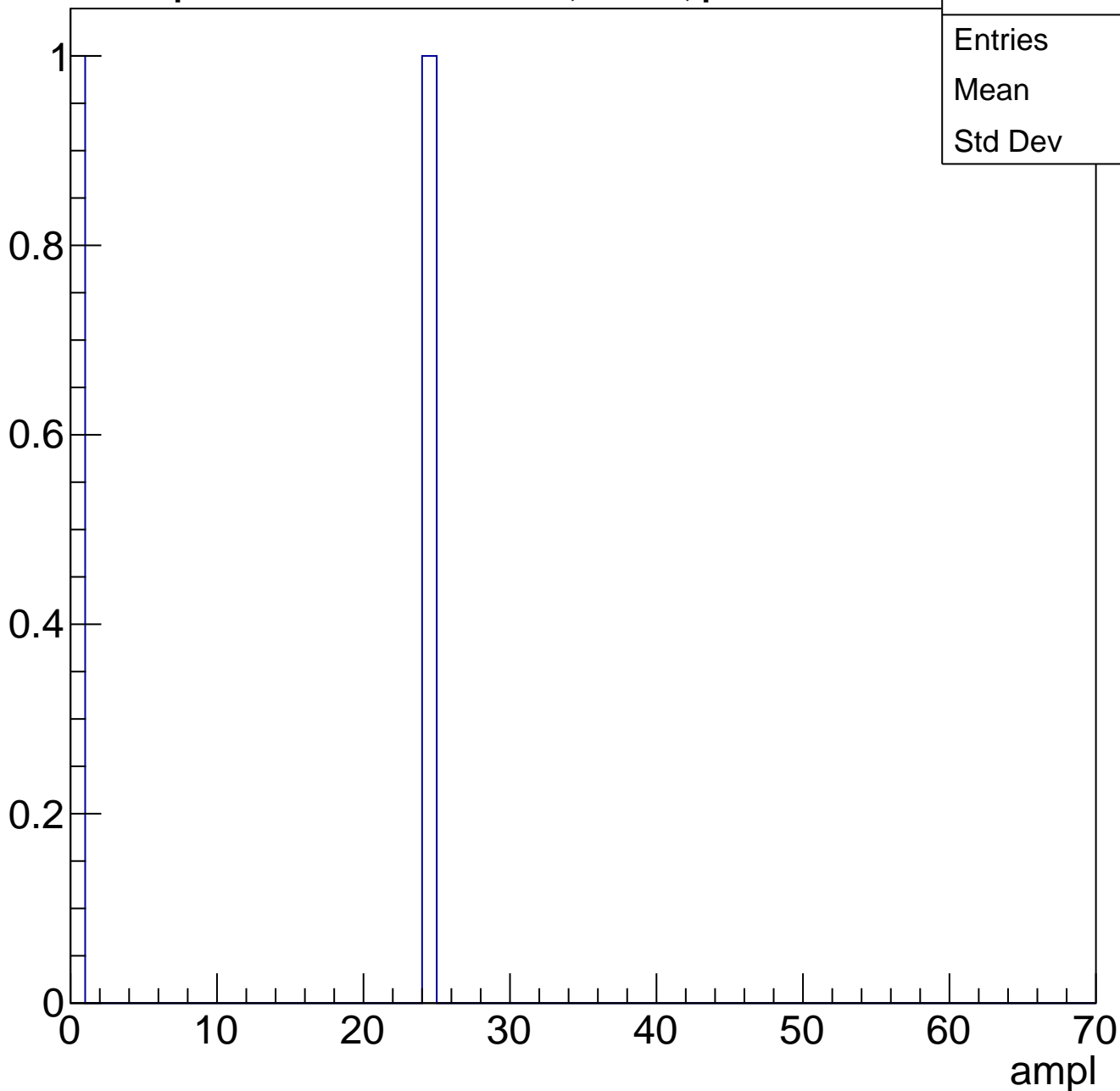
Entries	3
Mean	62
Std Dev	1.414



# B1L003S, U11-ch2, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U11-ch3, adc0

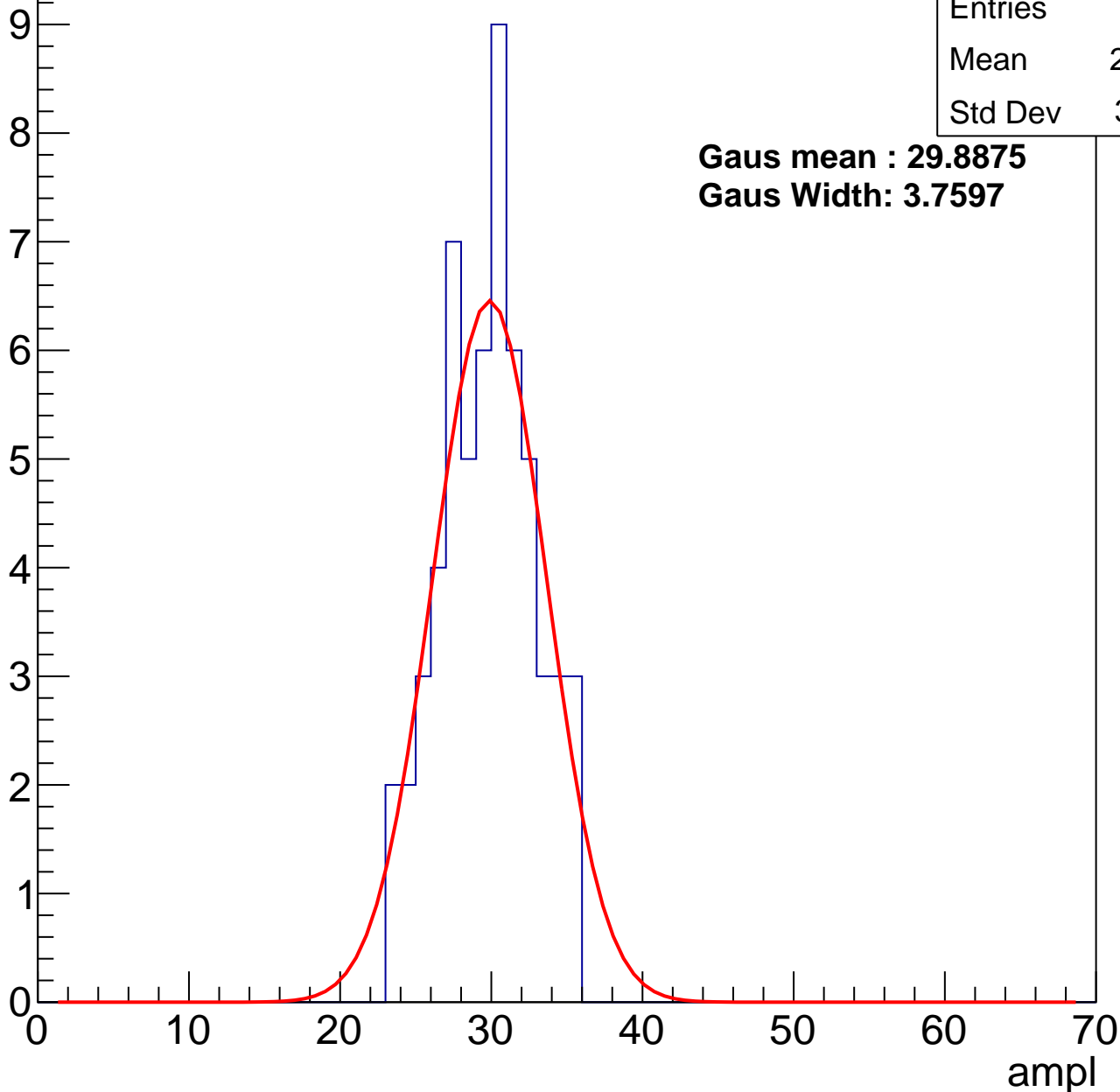
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	29.28
Std Dev	3.061

**Gaus mean : 29.8875**

**Gaus Width: 3.7597**



# B1L003S, U11-ch3, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	80
Mean	36.58
Std Dev	3.224

**Gaus mean : 37.1042**

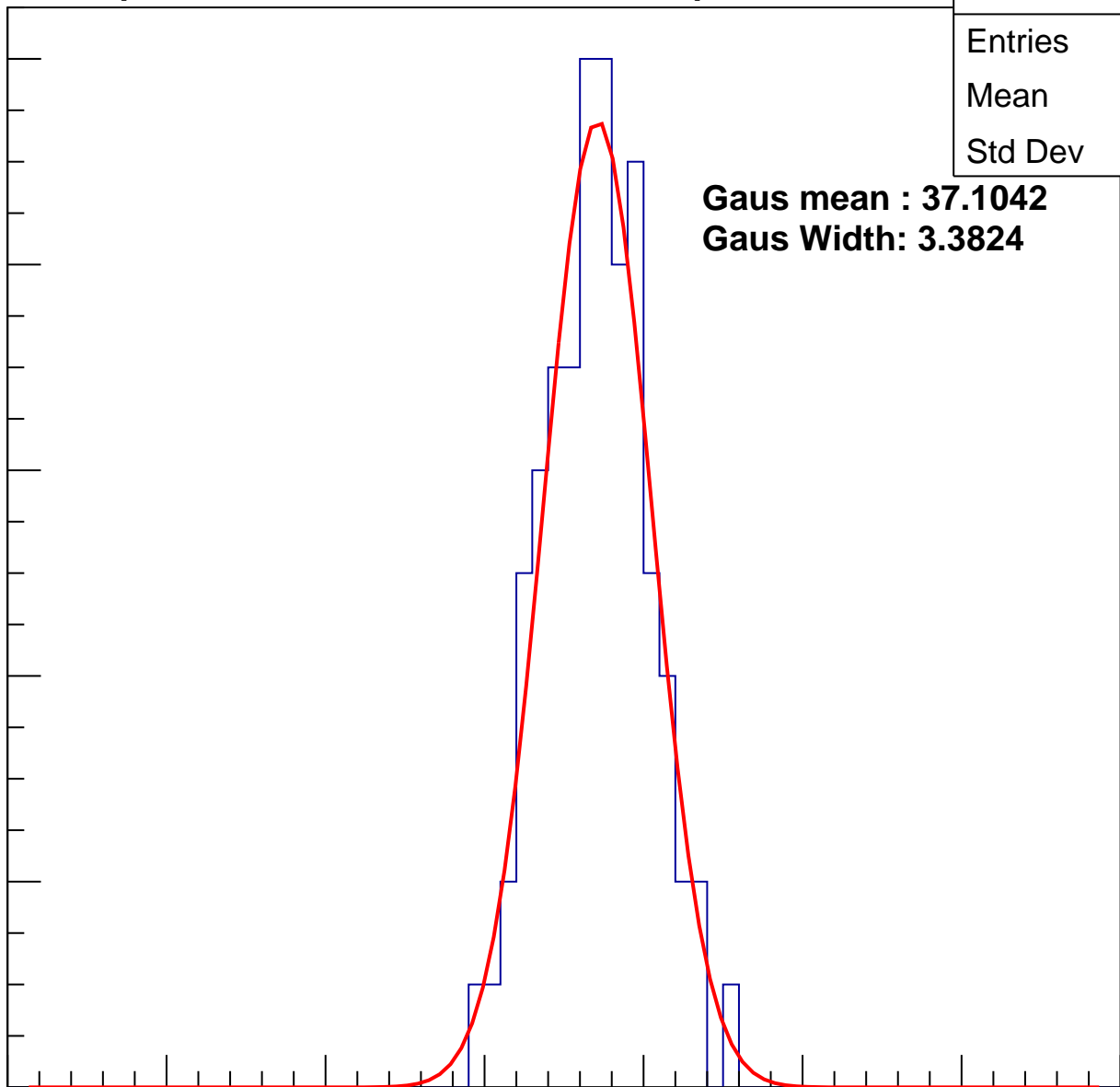
**Gaus Width: 3.3824**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U11-ch3, adc2

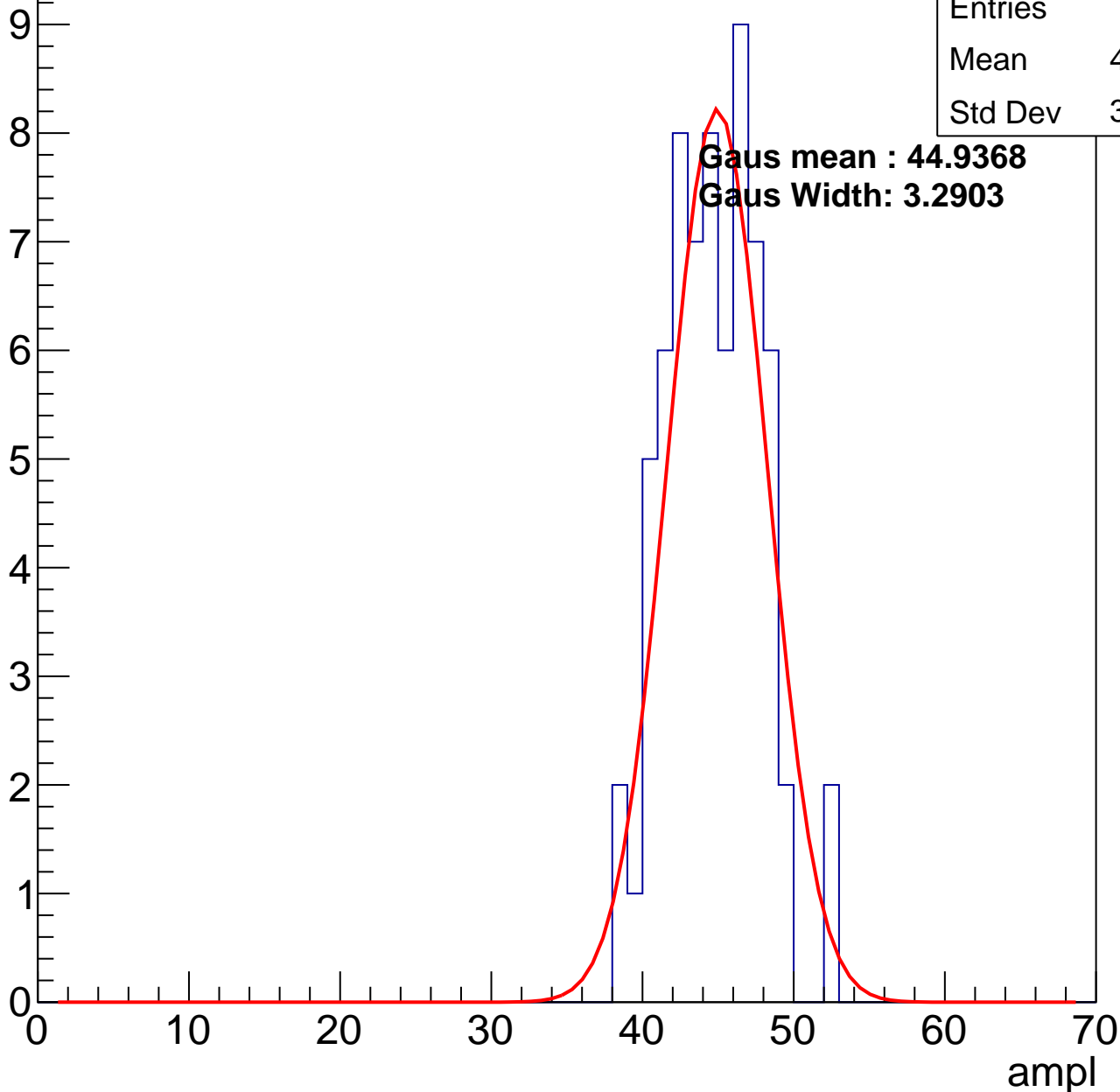
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	44.25
Std Dev	3.057

**Gaus mean : 44.9368**

**Gaus Width: 3.2903**



# B1L003S, U11-ch3, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

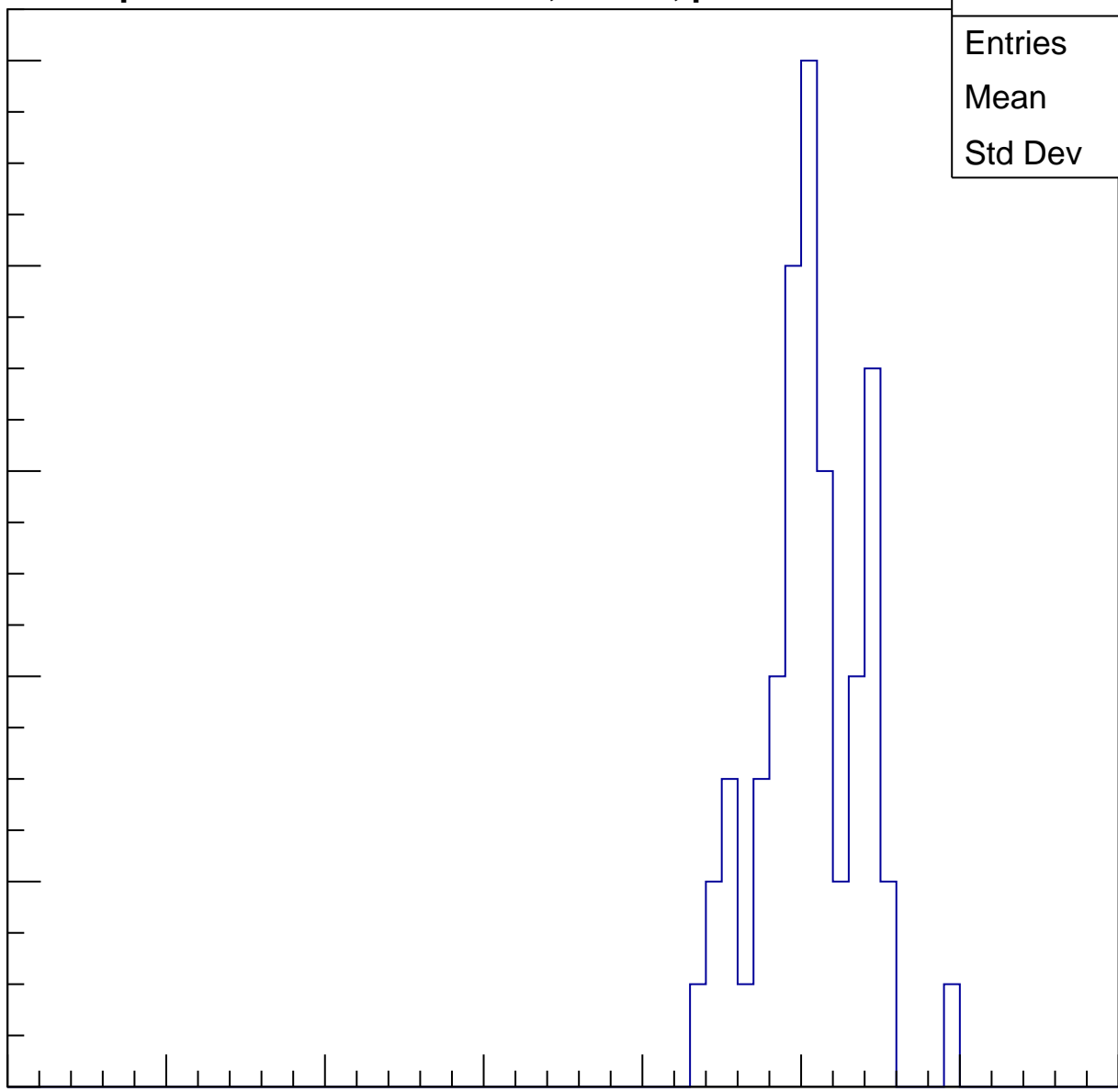
Entries	54
Mean	50.11
Std Dev	3.207

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

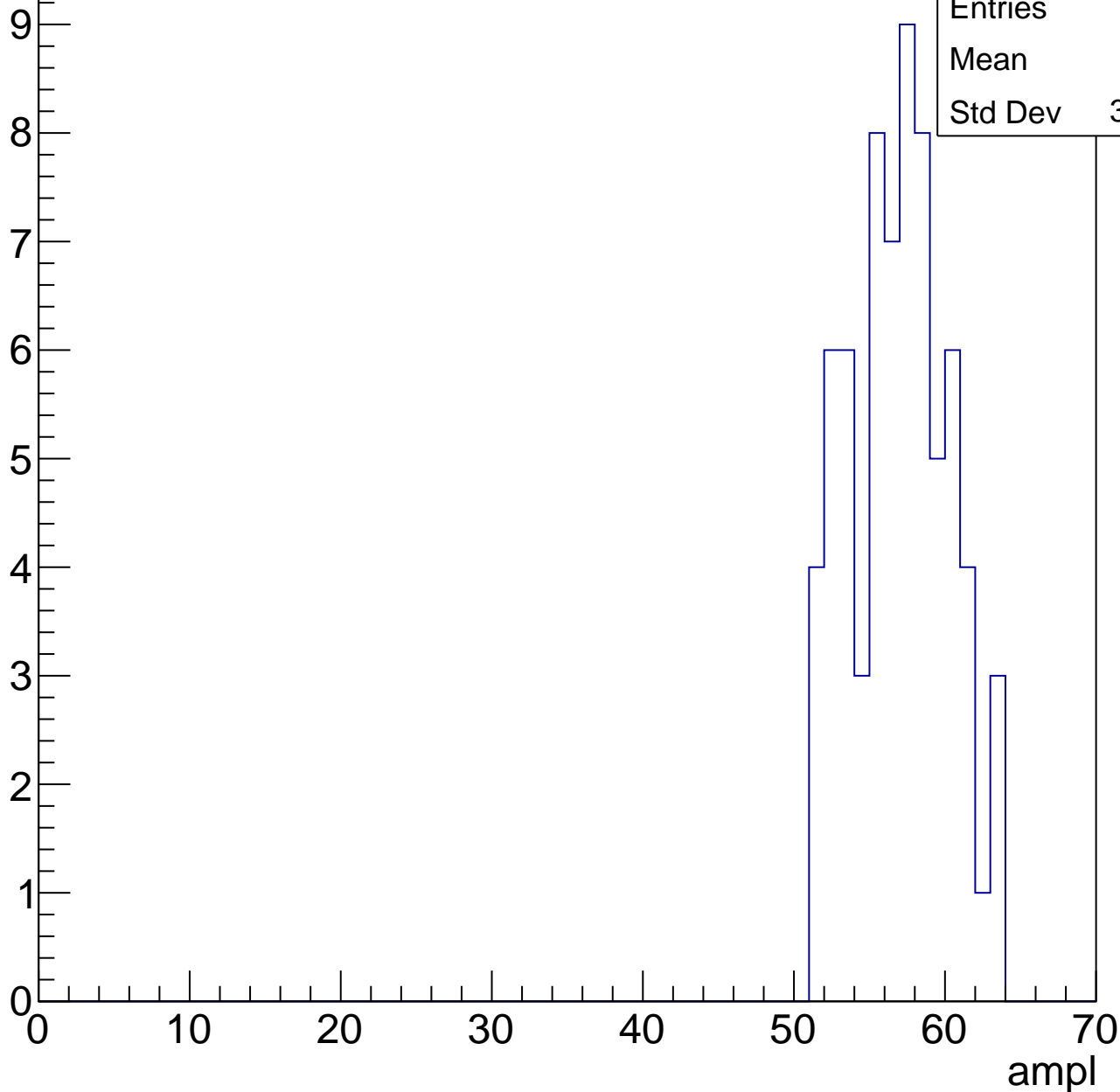
ampl



# B1L003S, U11-ch3, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

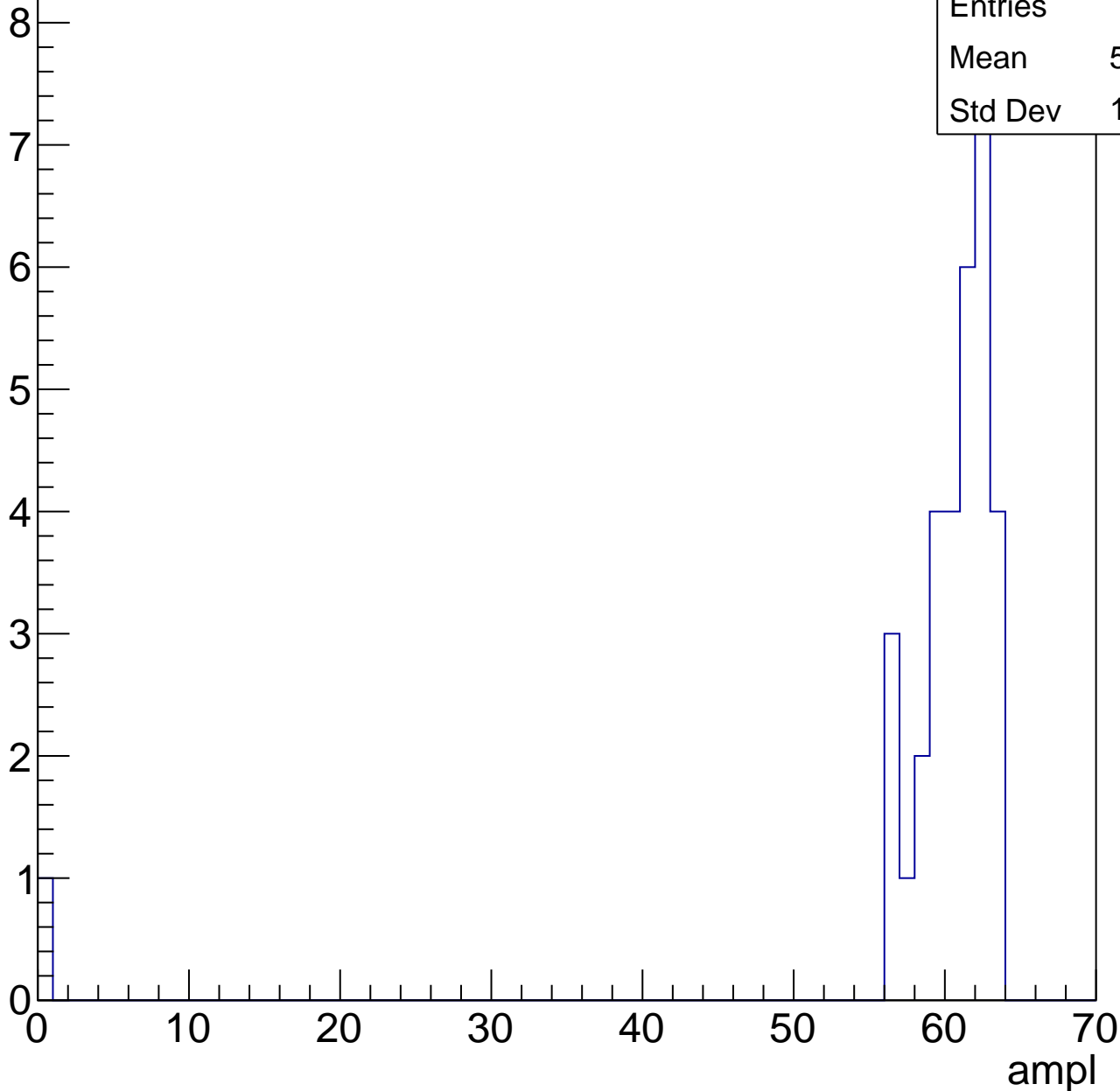


# B1L003S, U11-ch3, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

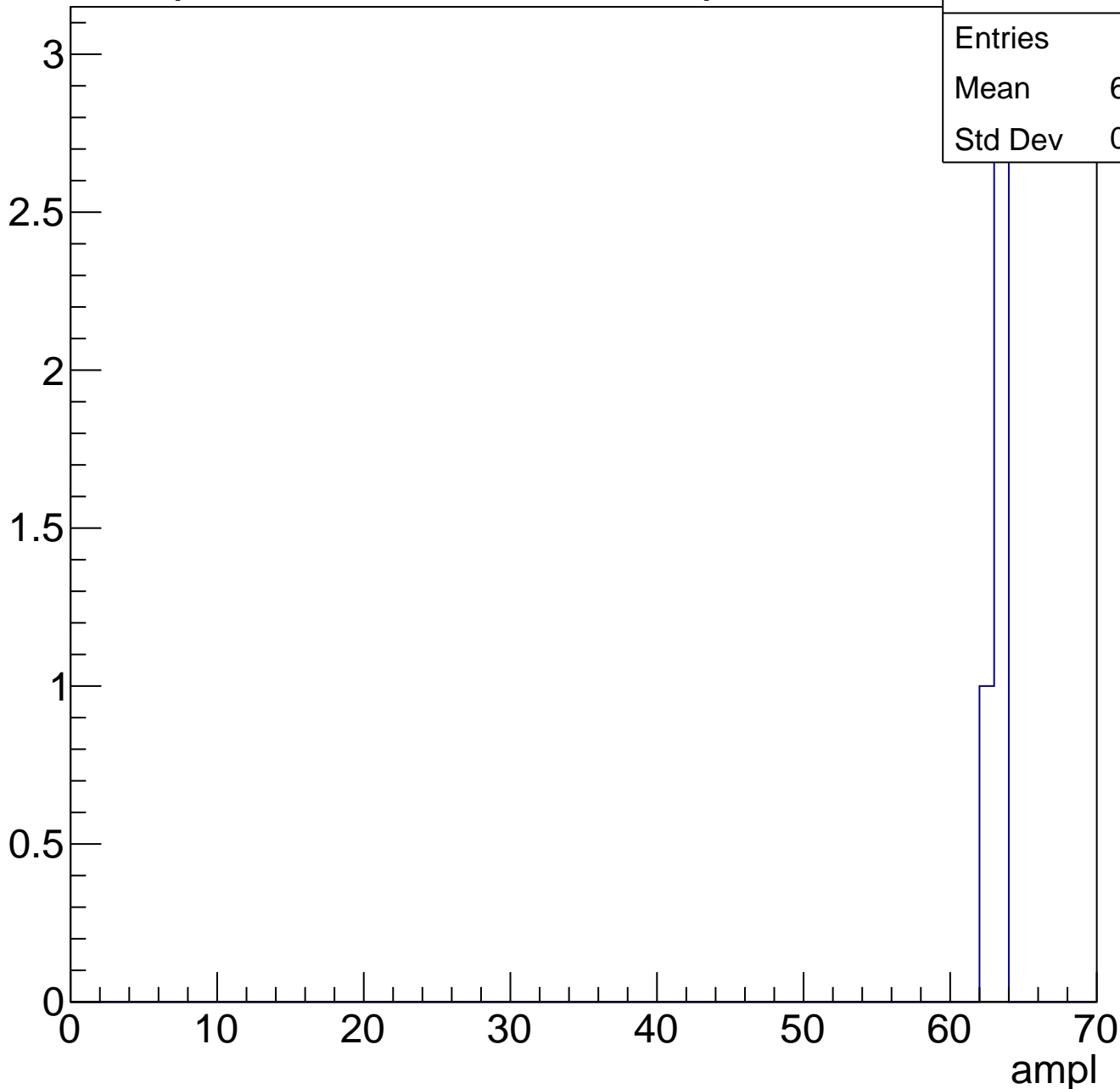
Entries	33
Mean	58.52
Std Dev	10.55



# B1L003S, U11-ch3, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch3, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U11-ch4, adc0

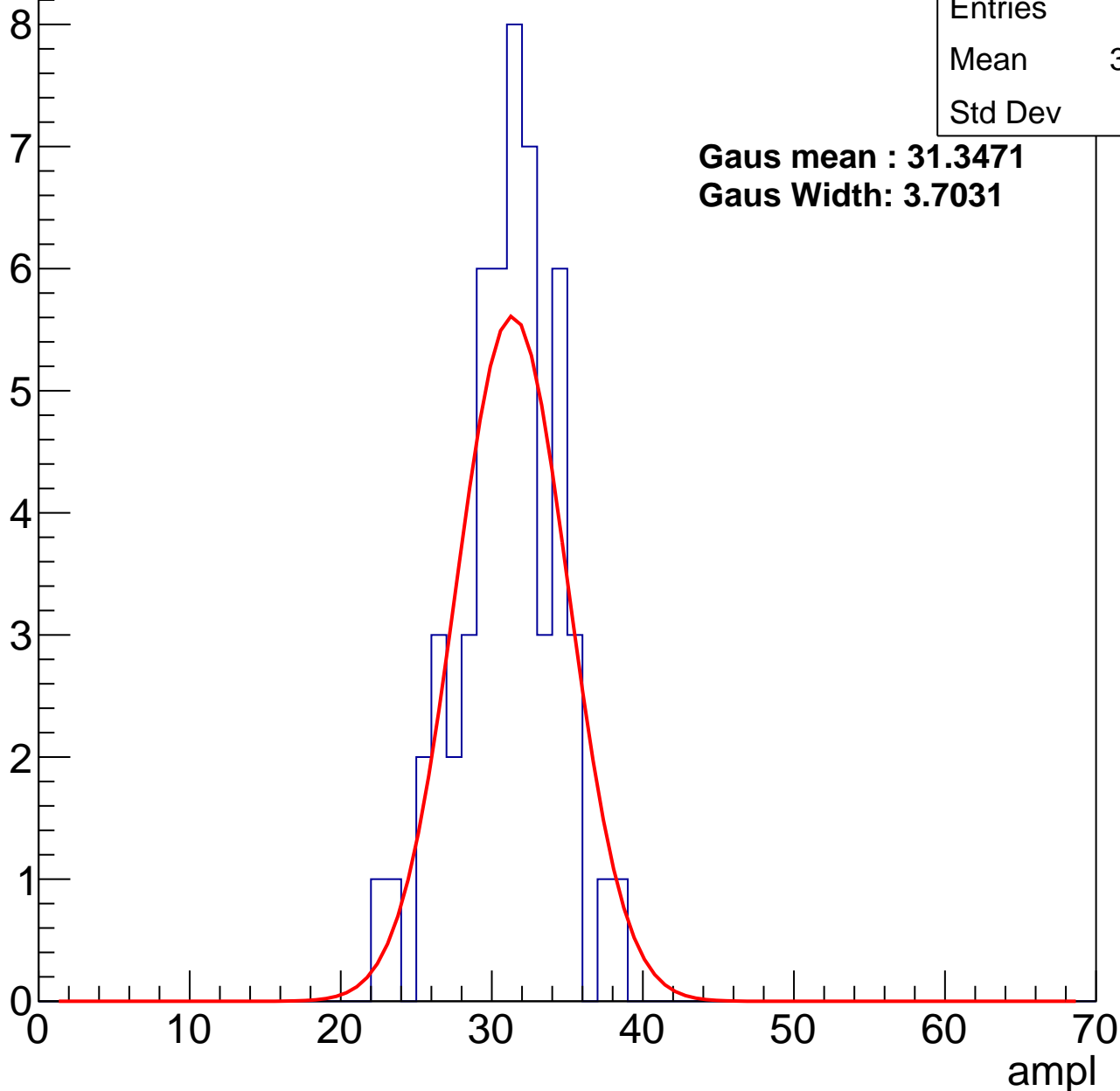
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	30.57
Std Dev	3.3

**Gaus mean : 31.3471**

**Gaus Width: 3.7031**



# B1L003S, U11-ch4, adc1

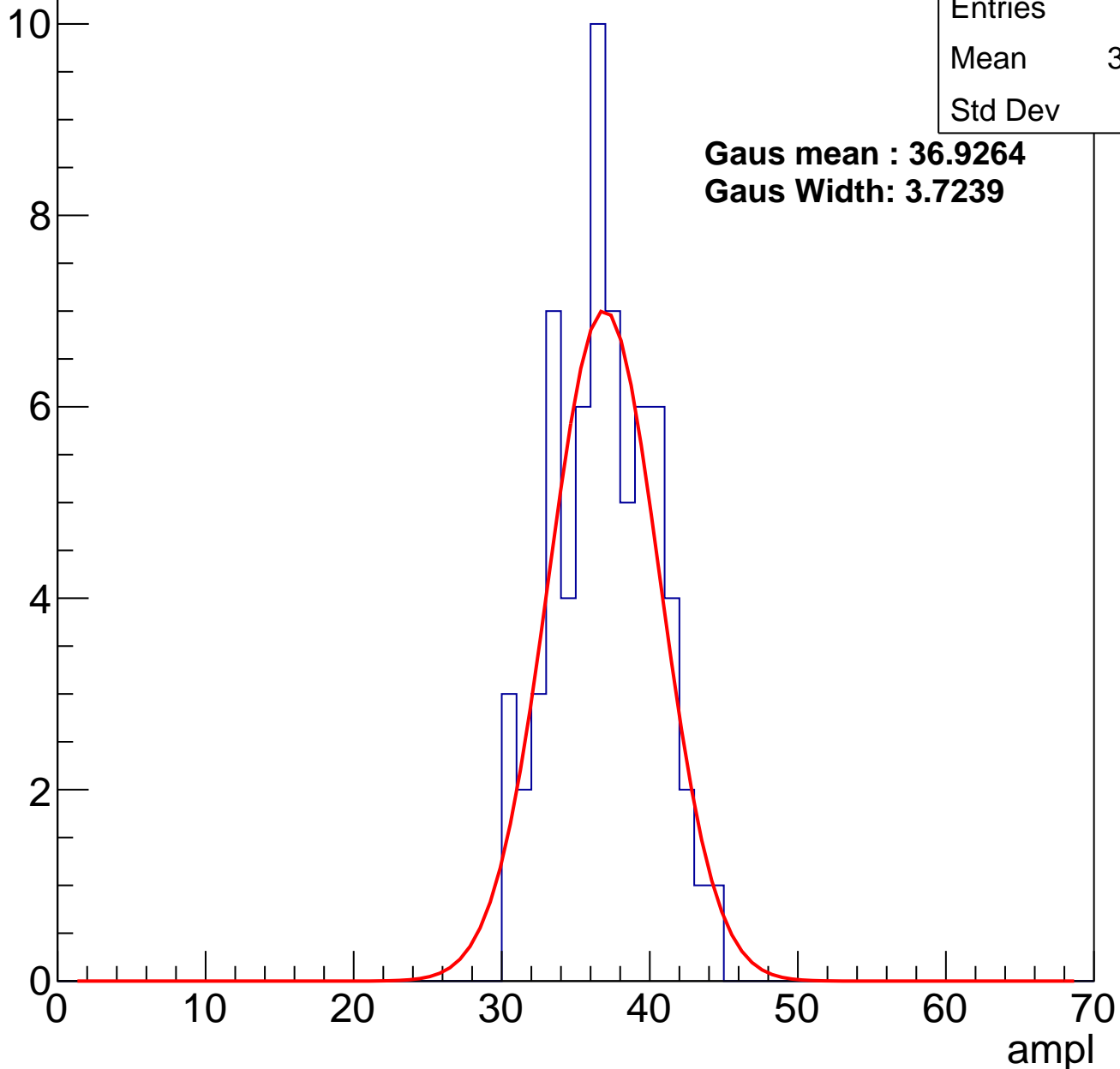
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	67
Mean	36.46
Std Dev	3.32

**Gaus mean : 36.9264**

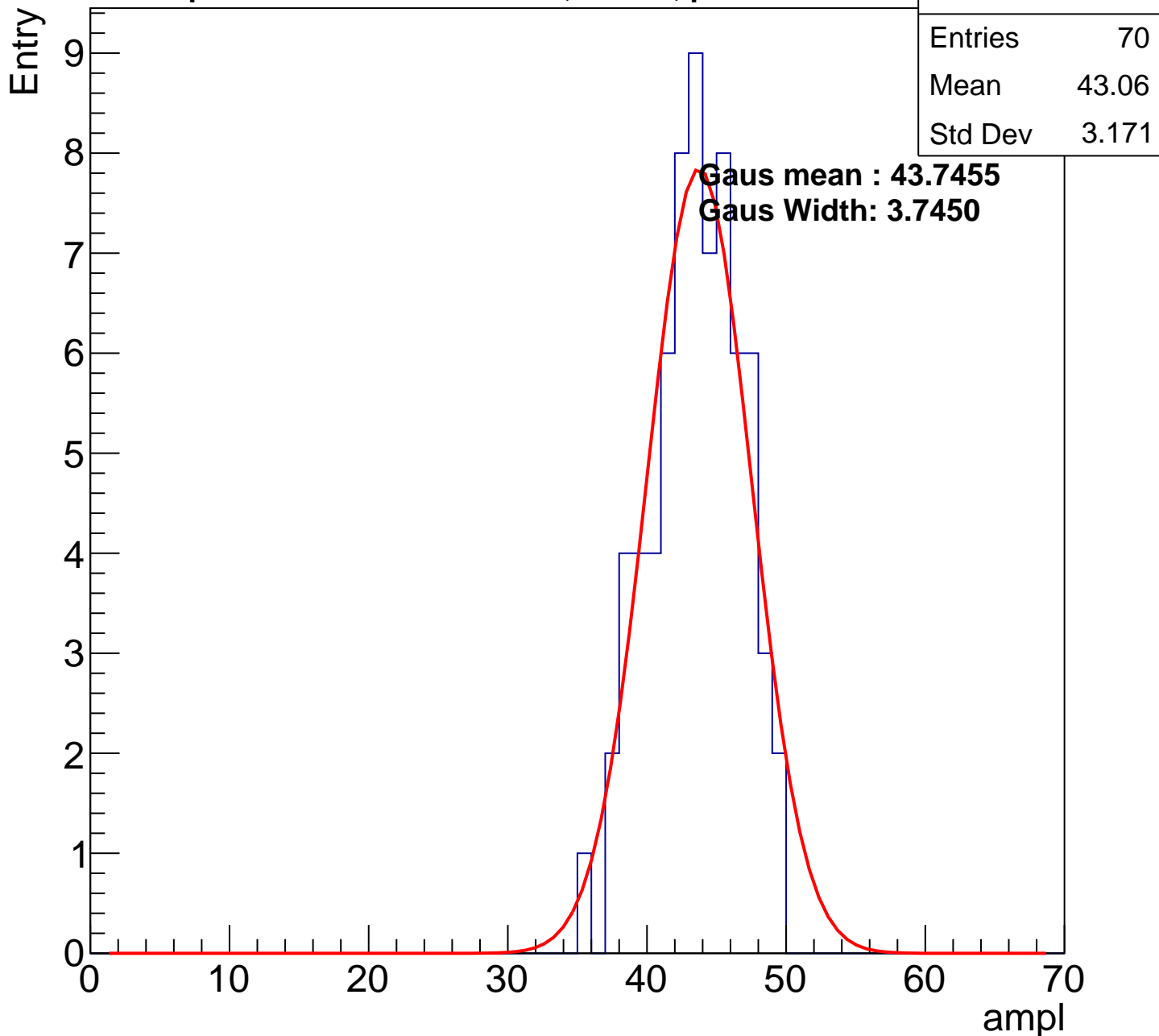
**Gaus Width: 3.7239**

Entry



# B1L003S, U11-ch4, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

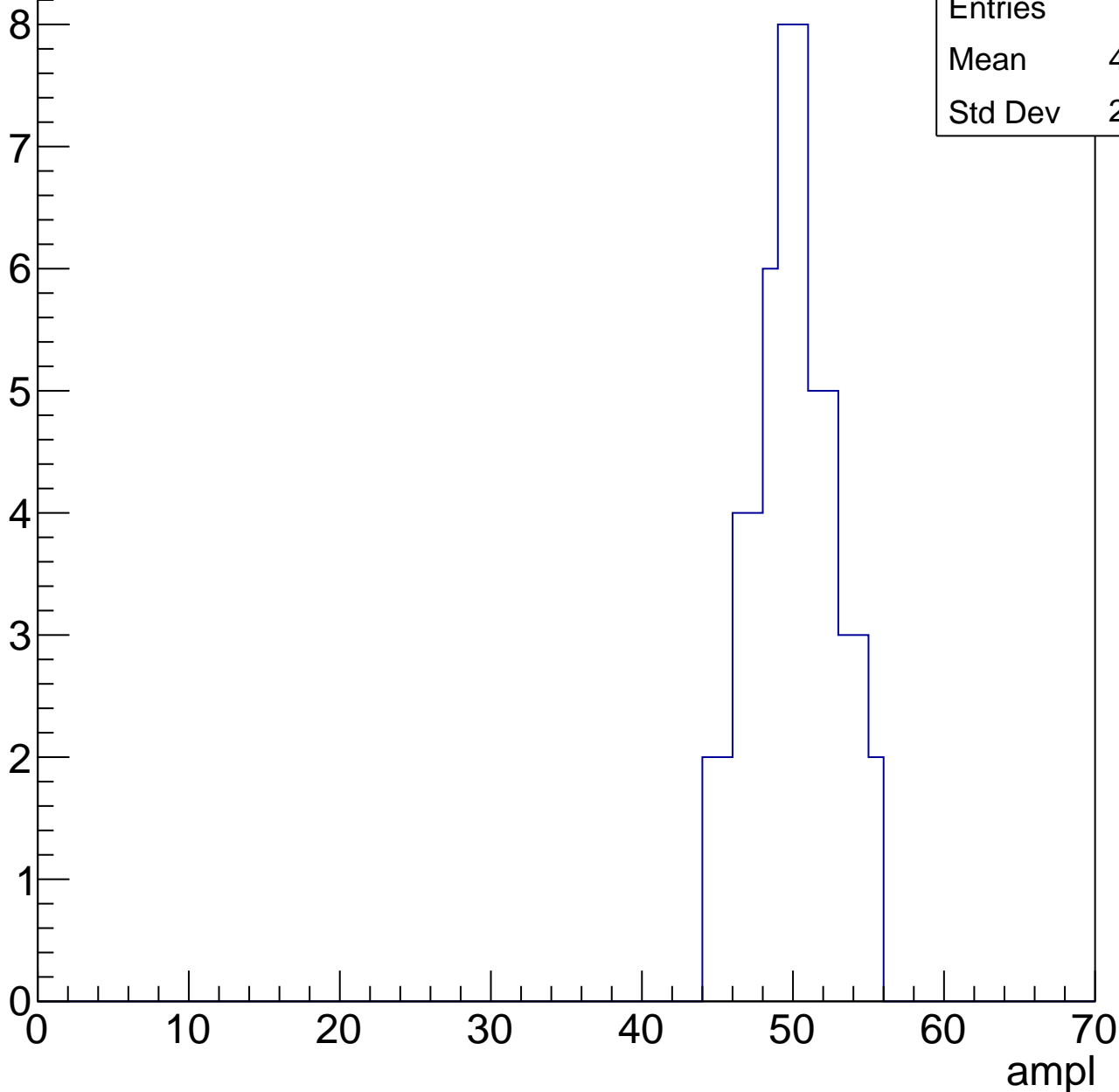


# B1L003S, U11-ch4, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	52
Mean	49.54
Std Dev	2.749

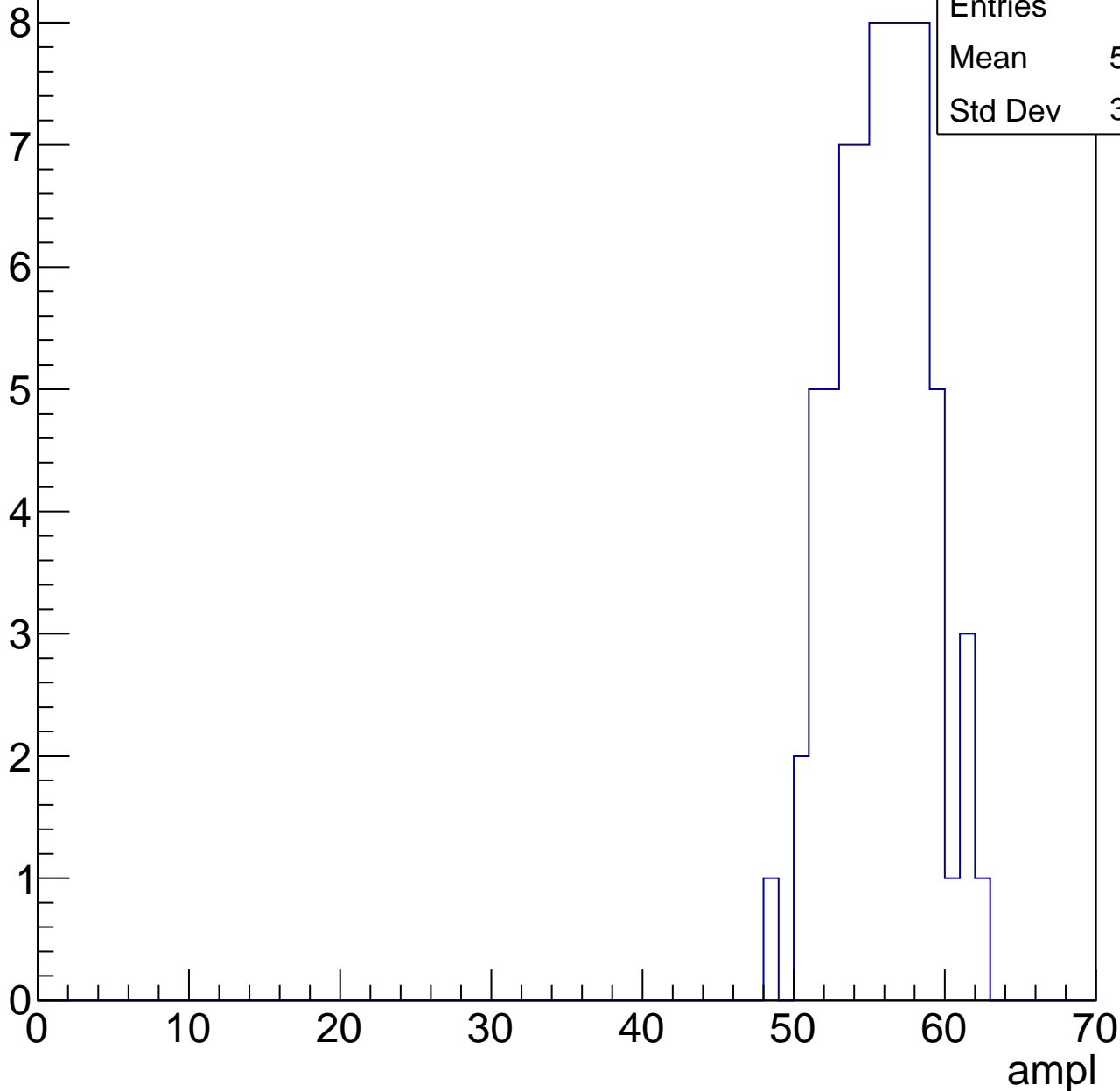


# B1L003S, U11-ch4, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	55.36
Std Dev	3.007



# B1L003S, U11-ch4, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	44
Mean	59.18
Std Dev	9.225

ampl

0 10 20 30 40 50 60 70

1

2

3

4

5

6

7

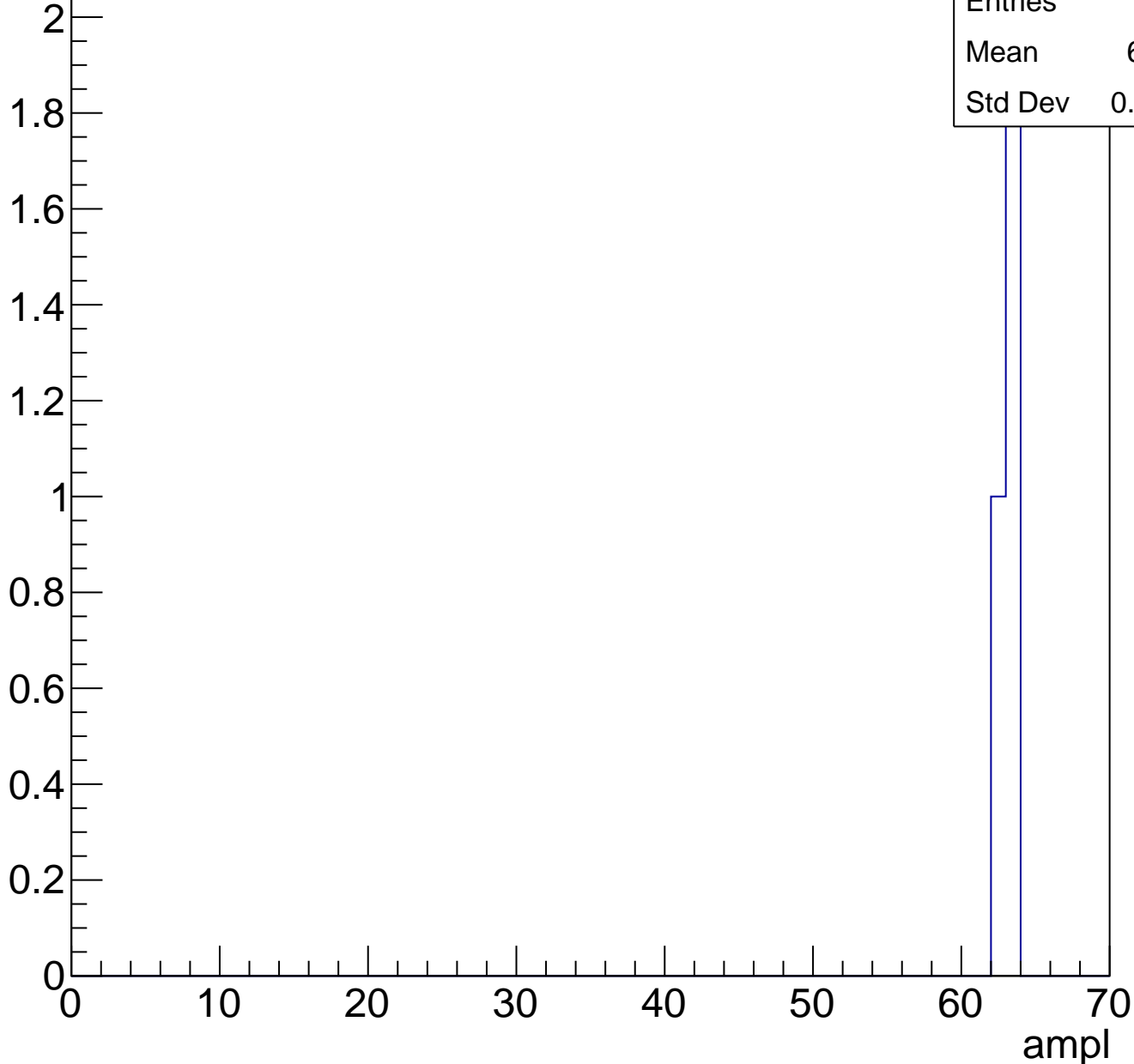
8

9

# B1L003S, U11-ch4, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch4, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U11-ch5, adc0

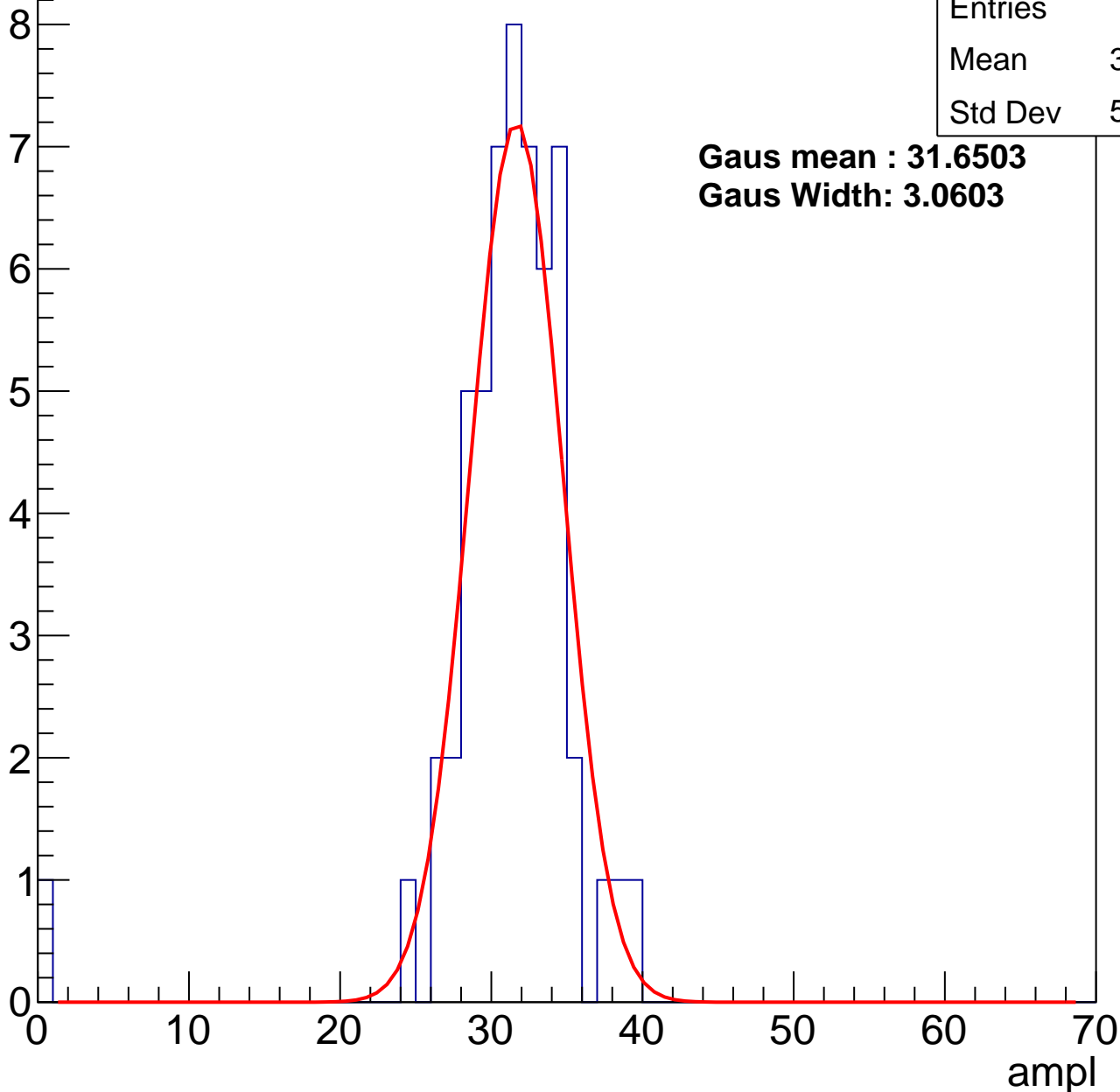
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	30.66
Std Dev	5.058

**Gaus mean : 31.6503**

**Gaus Width: 3.0603**



# B1L003S, U11-ch5, adc1

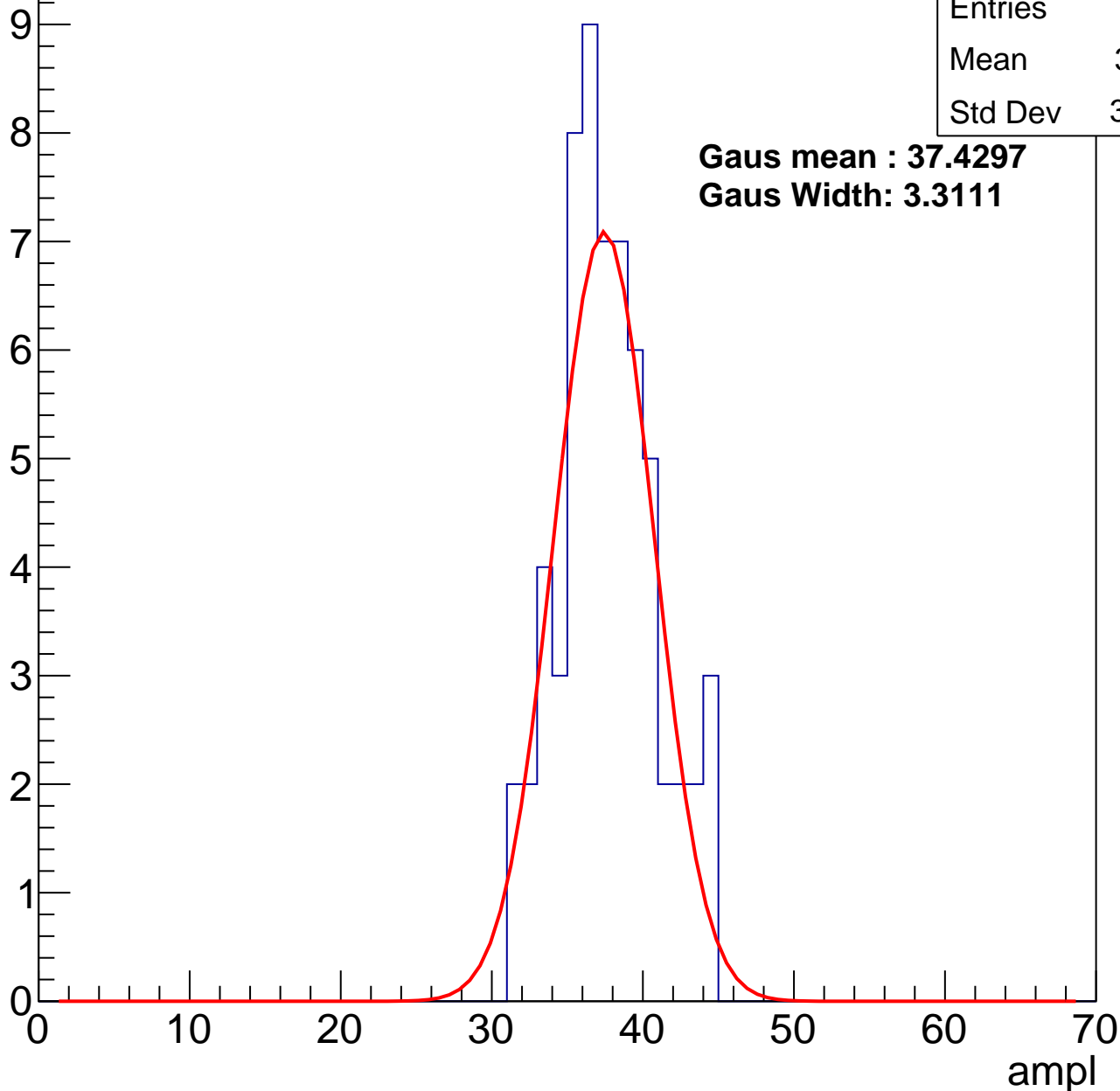
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	37.21
Std Dev	3.183

**Gaus mean : 37.4297**

**Gaus Width: 3.3111**



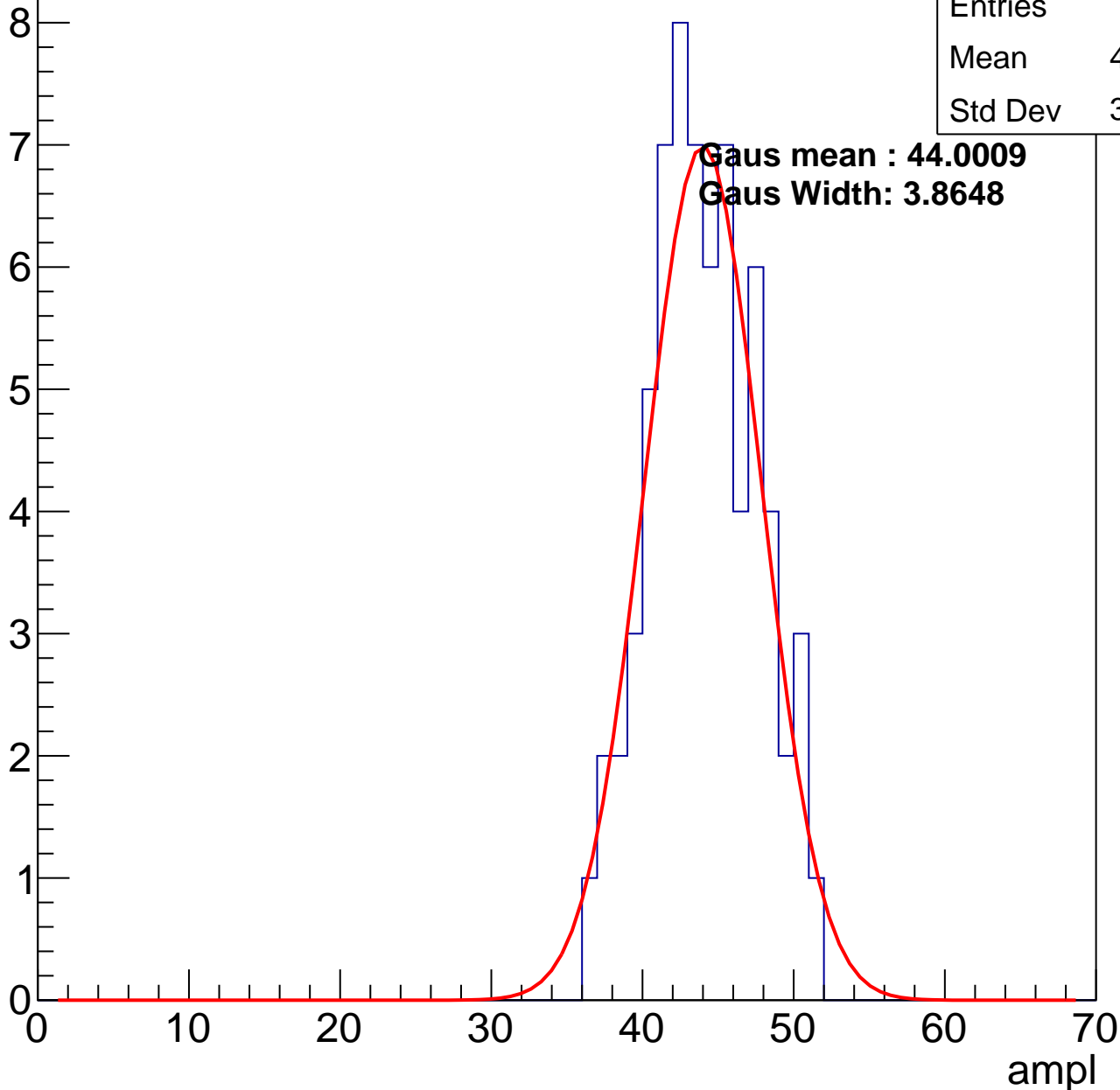
# B1L003S, U11-ch5, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	43.57
Std Dev	3.487

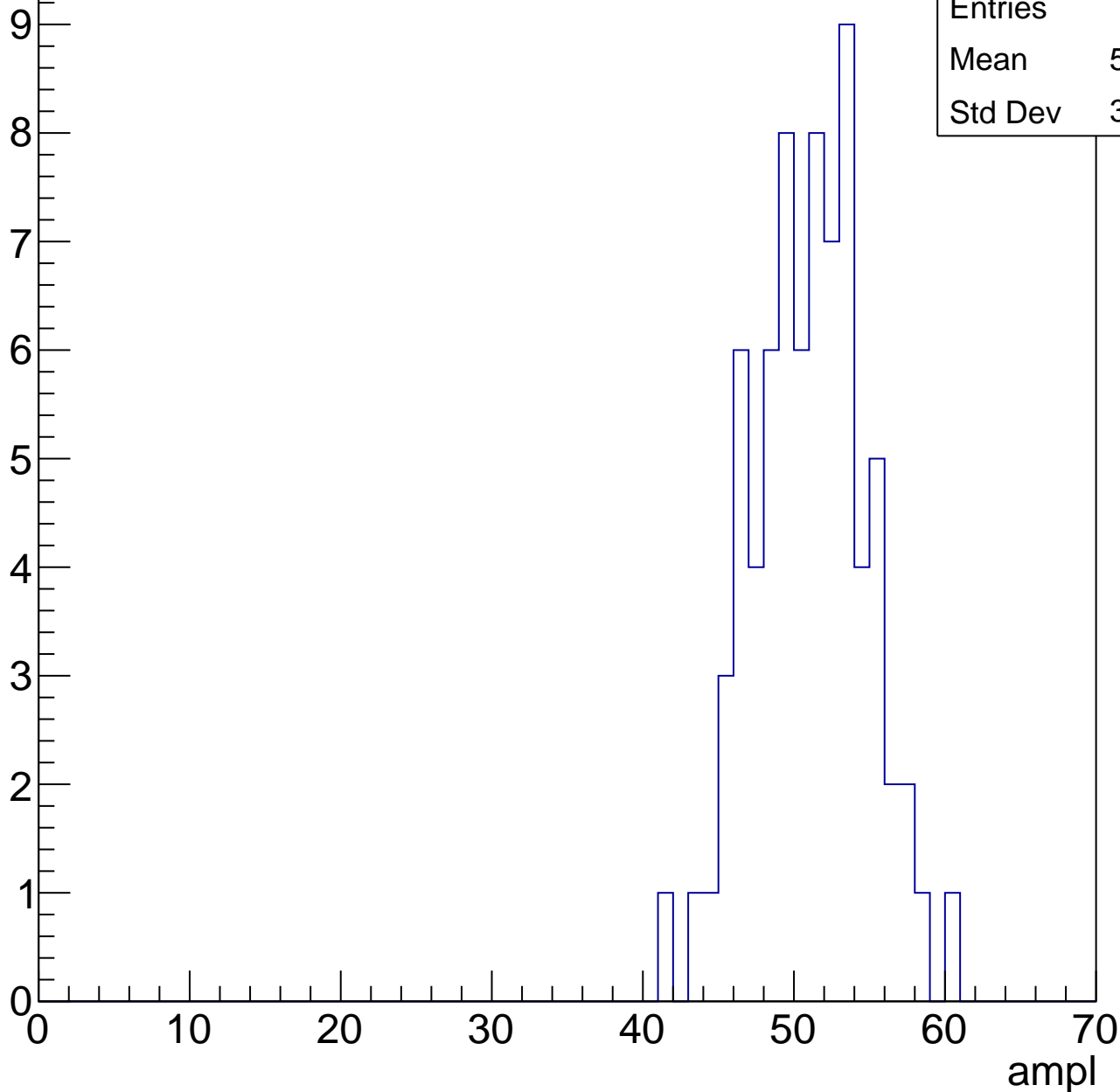
**Gaus mean : 44.0009**  
**Gaus Width: 3.8648**



# B1L003S, U11-ch5, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

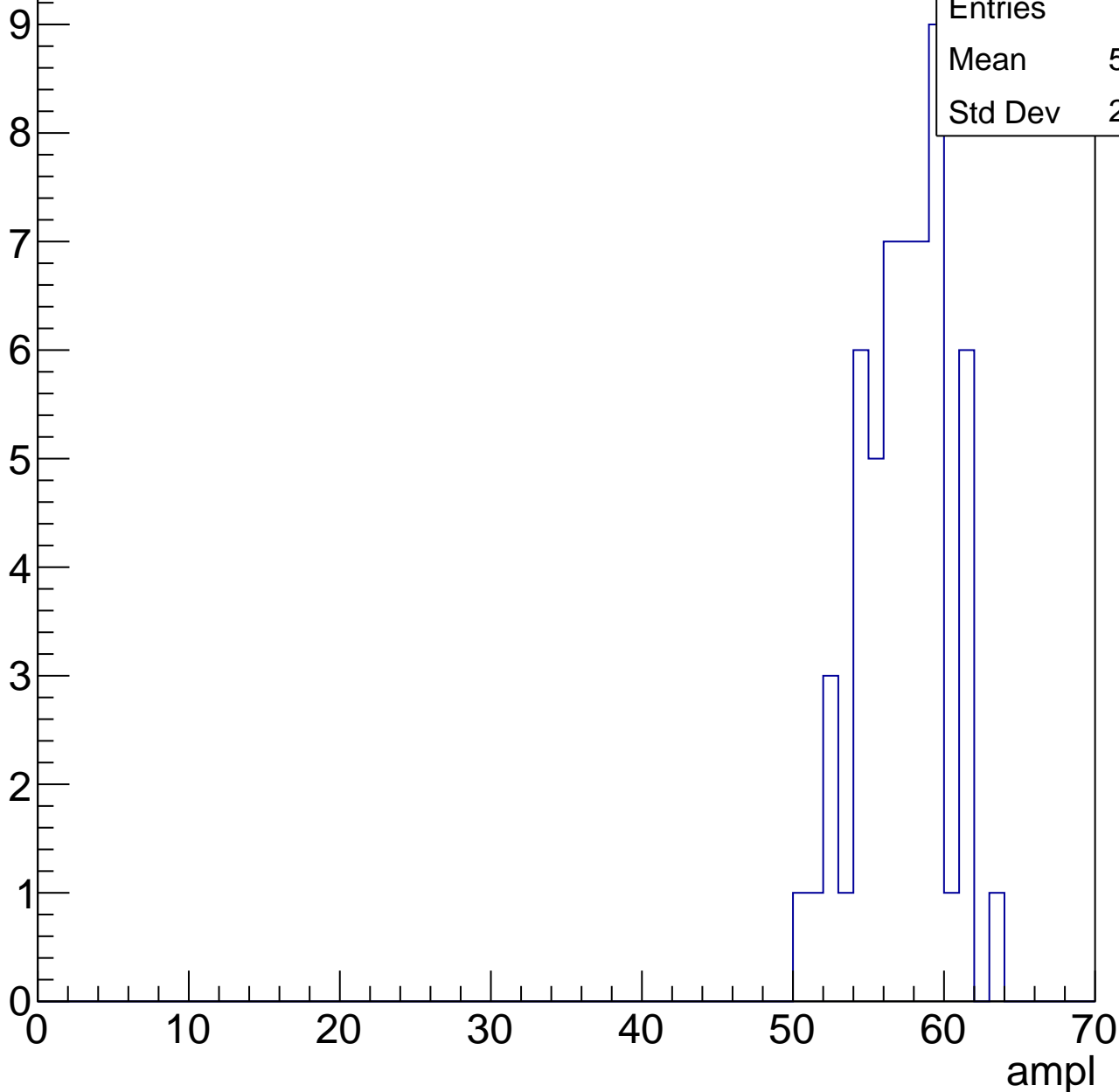


# B1L003S, U11-ch5, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

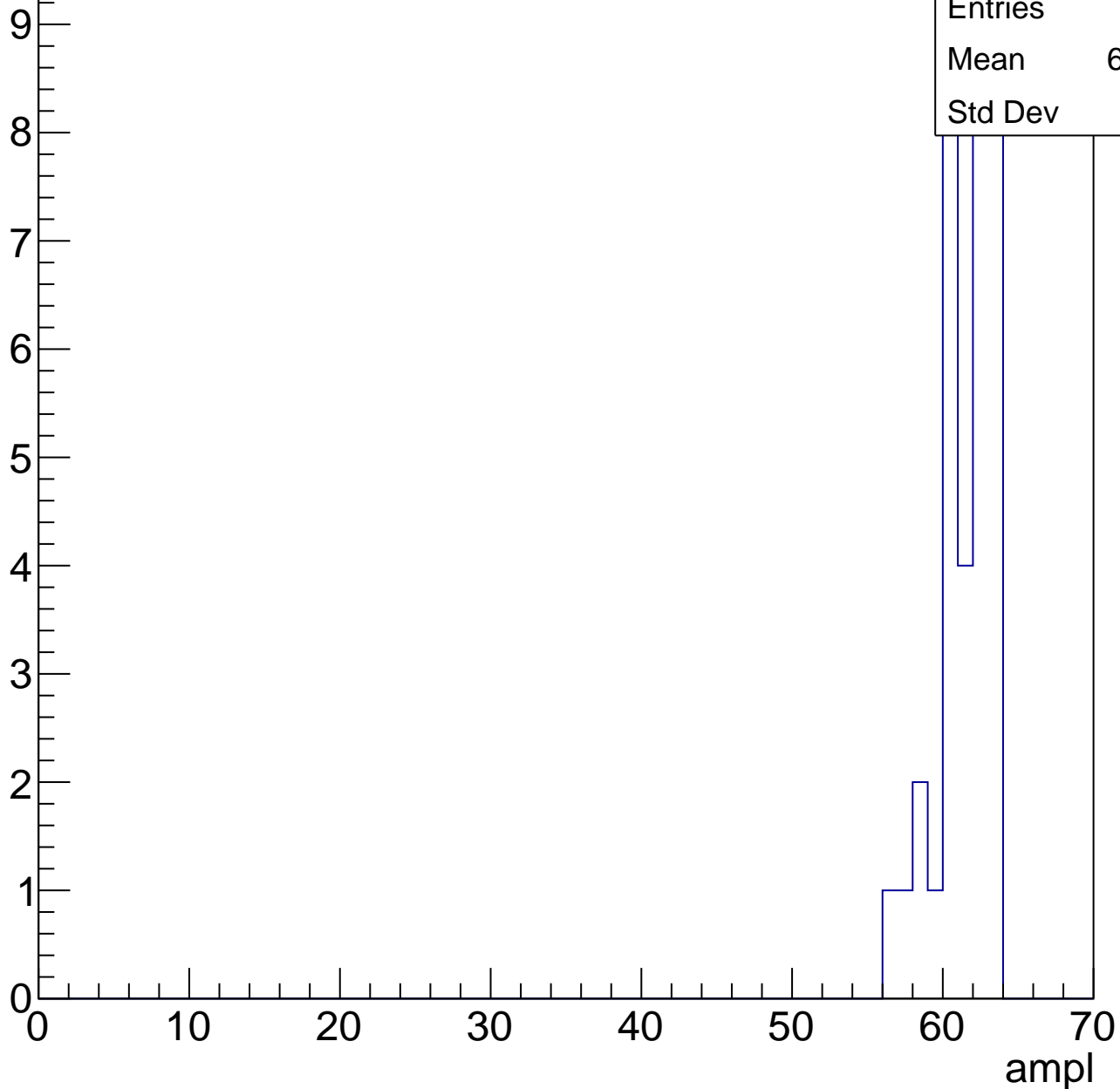
Entries	55
Mean	56.84
Std Dev	2.827



# B1L003S, U11-ch5, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

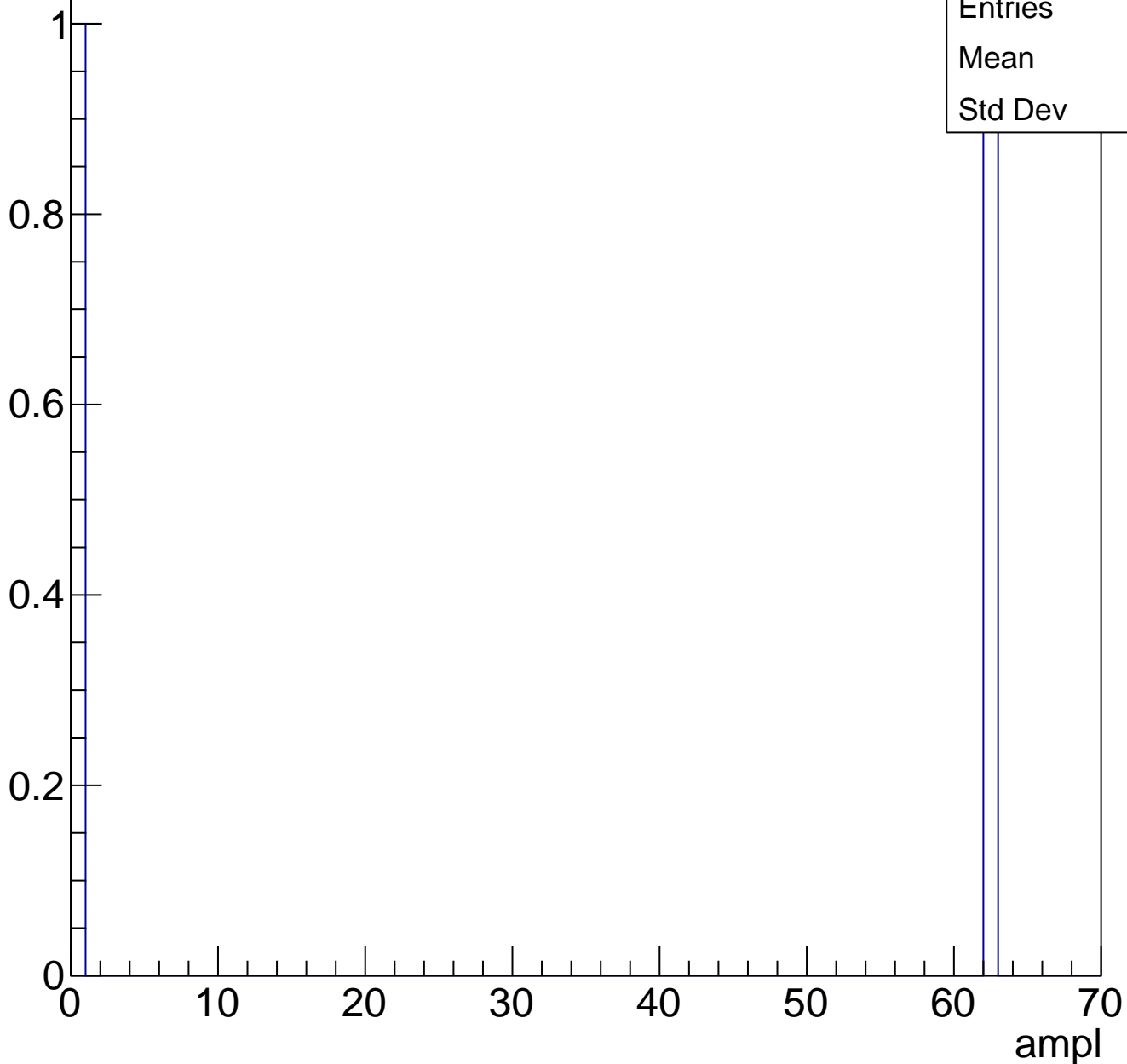
Entry



# B1L003S, U11-ch5, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch5, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U11-ch6, adc0

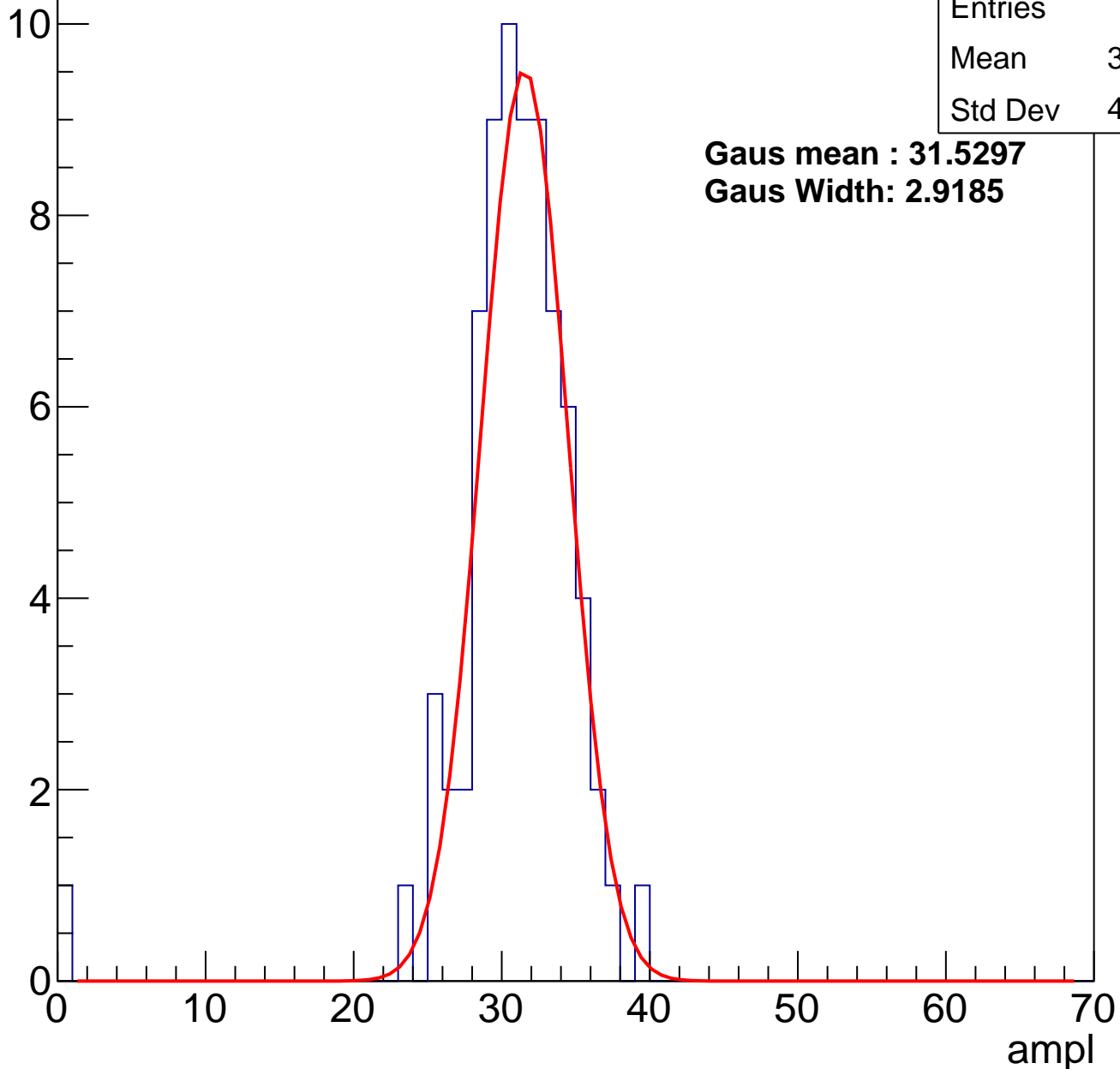
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	74
Mean	30.42
Std Dev	4.656

**Gaus mean : 31.5297**

**Gaus Width: 2.9185**

Entry

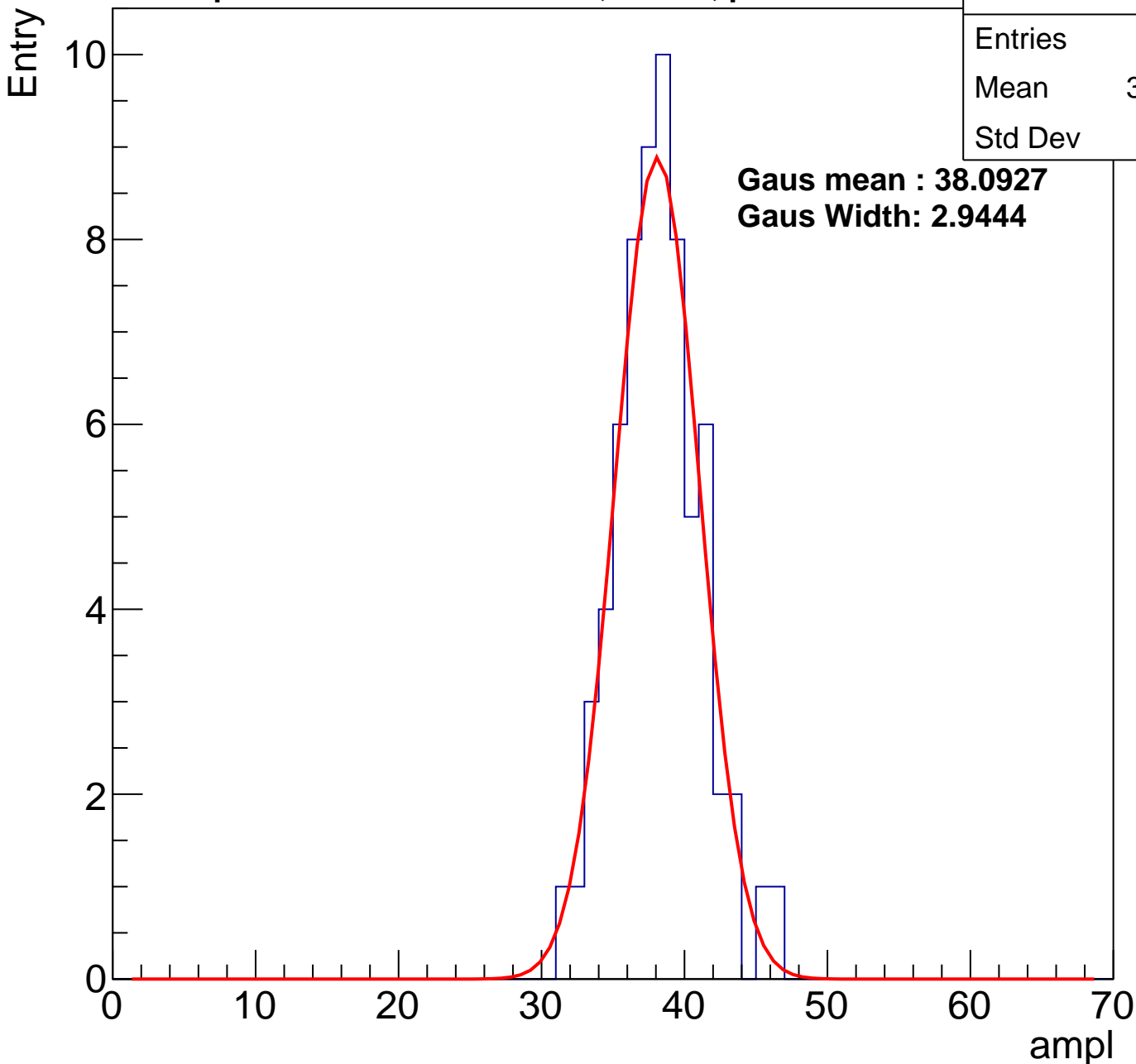


# B1L003S, U11-ch6, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	67
Mean	37.73
Std Dev	2.97

**Gaus mean : 38.0927**  
**Gaus Width: 2.9444**



# B1L003S, U11-ch6, adc2

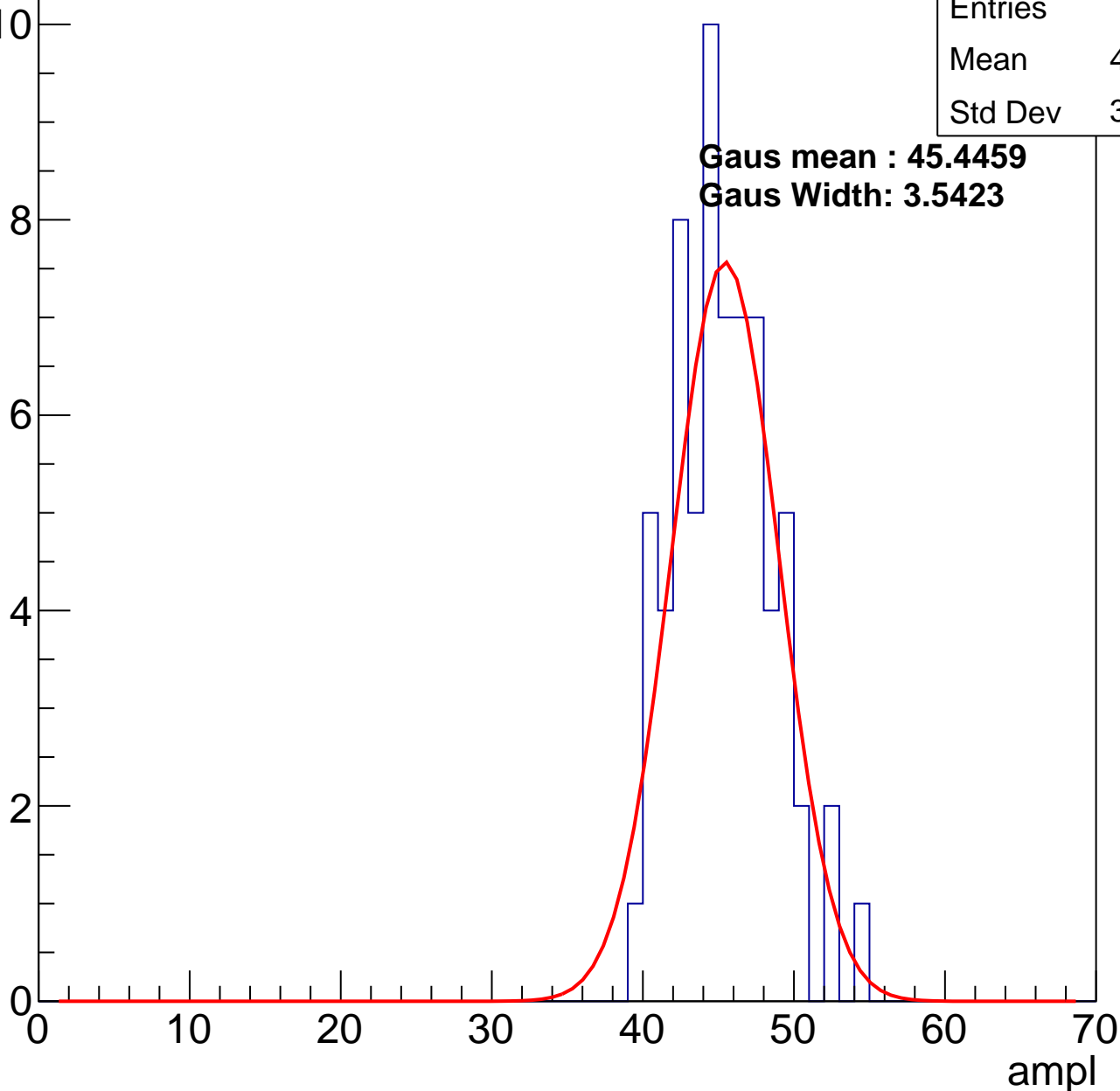
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	44.93
Std Dev	3.224

**Gaus mean : 45.4459**

**Gaus Width: 3.5423**

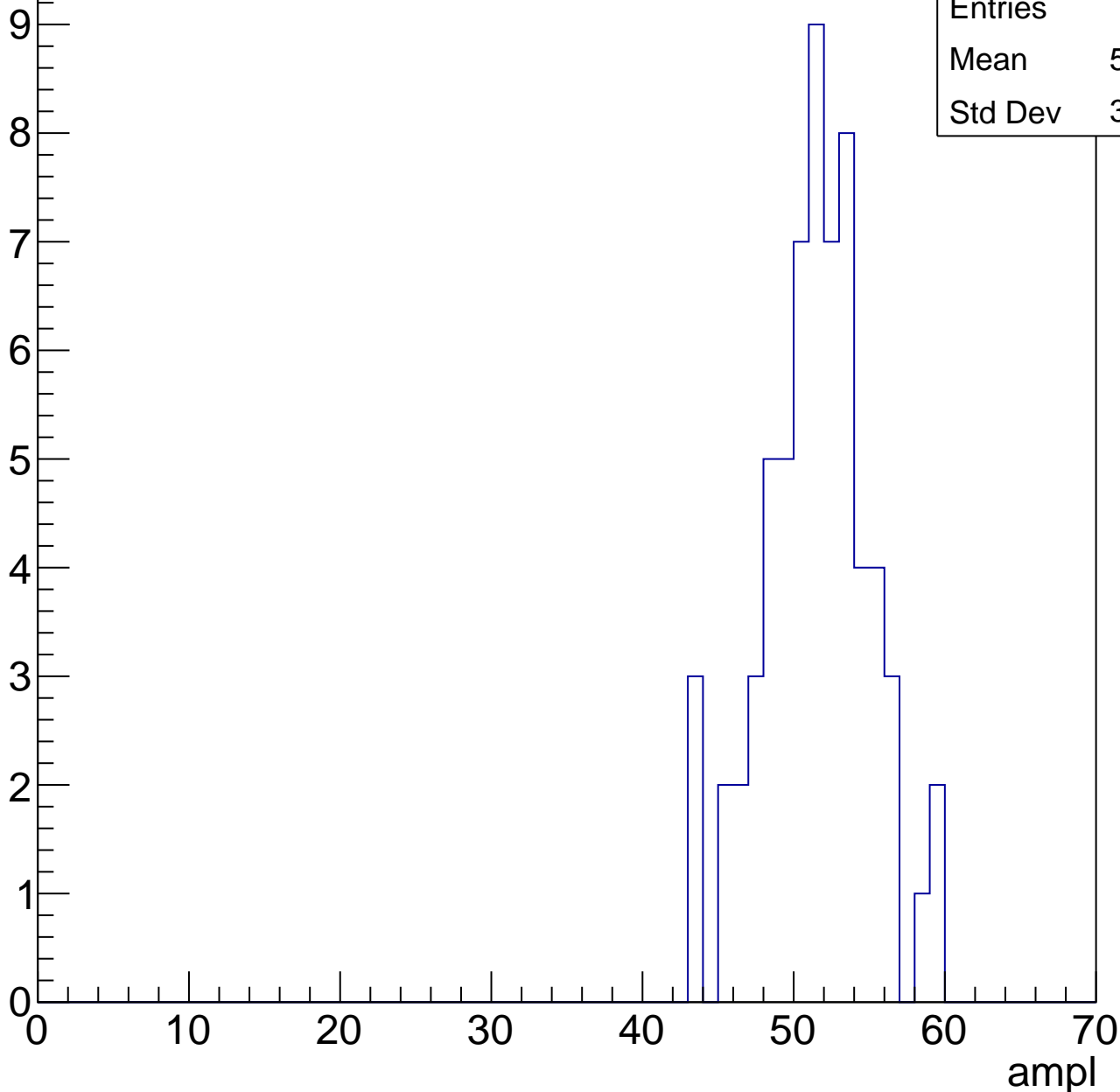


# B1L003S, U11-ch6, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	50.98
Std Dev	3.563

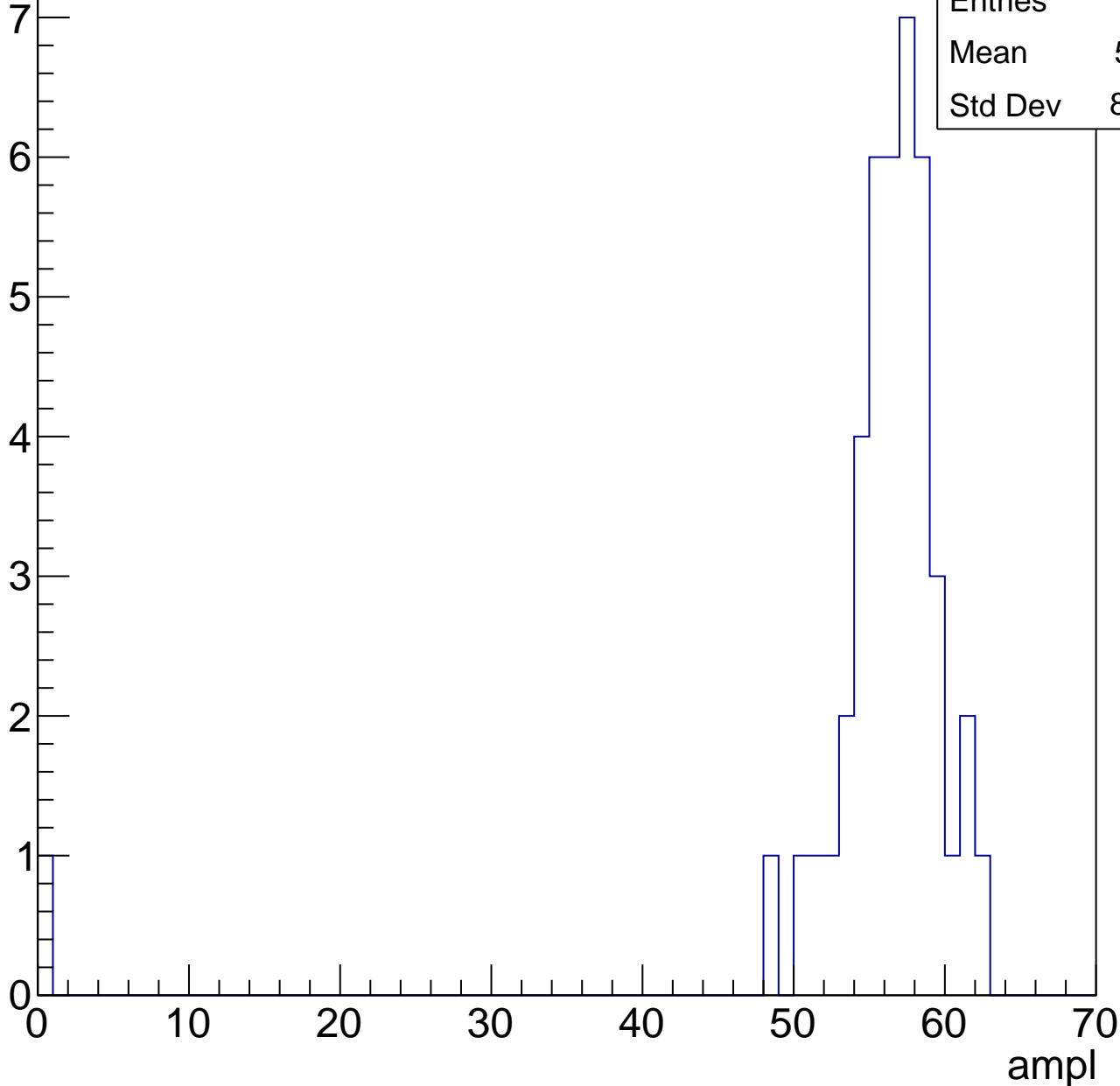


# B1L003S, U11-ch6, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	43
Mean	54.81
Std Dev	8.914



# B1L003S, U11-ch6, adc5

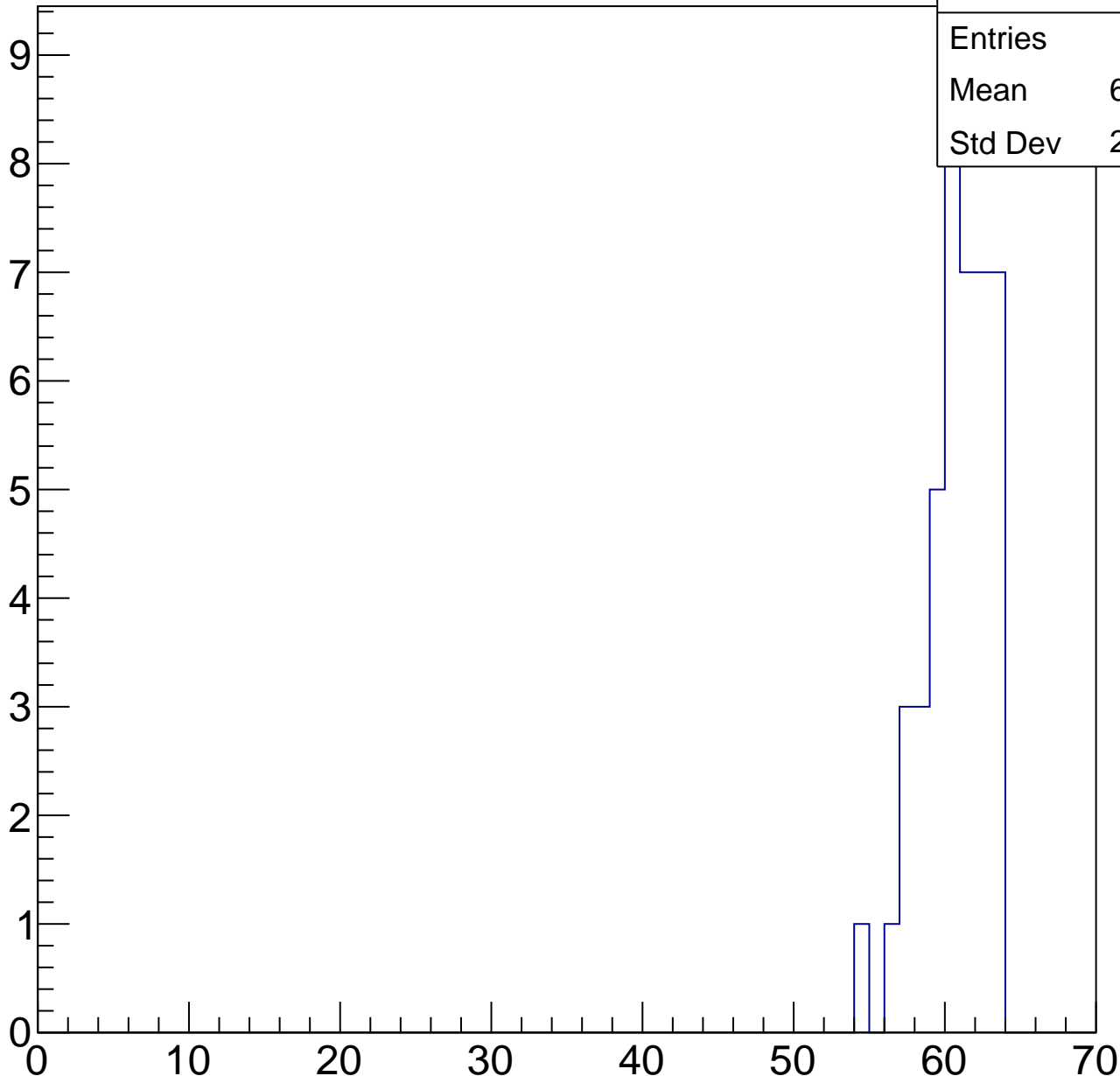
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	43
Mean	60.28
Std Dev	2.106

ampl



# B1L003S, U11-ch6, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch6, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U11-ch7, adc0

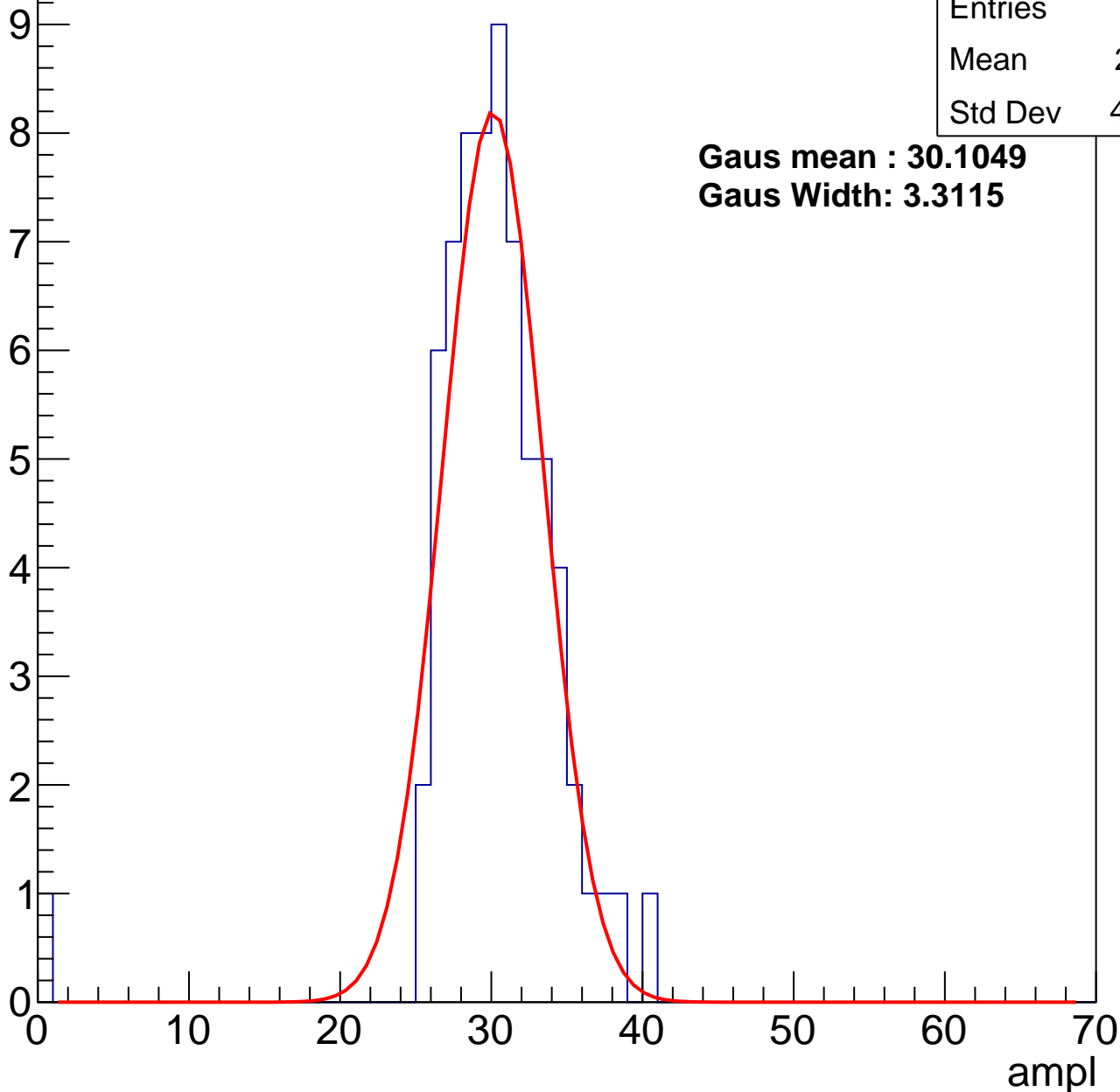
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	29.71
Std Dev	4.817

**Gaus mean : 30.1049**

**Gaus Width: 3.3115**



# B1L003S, U11-ch7, adc1

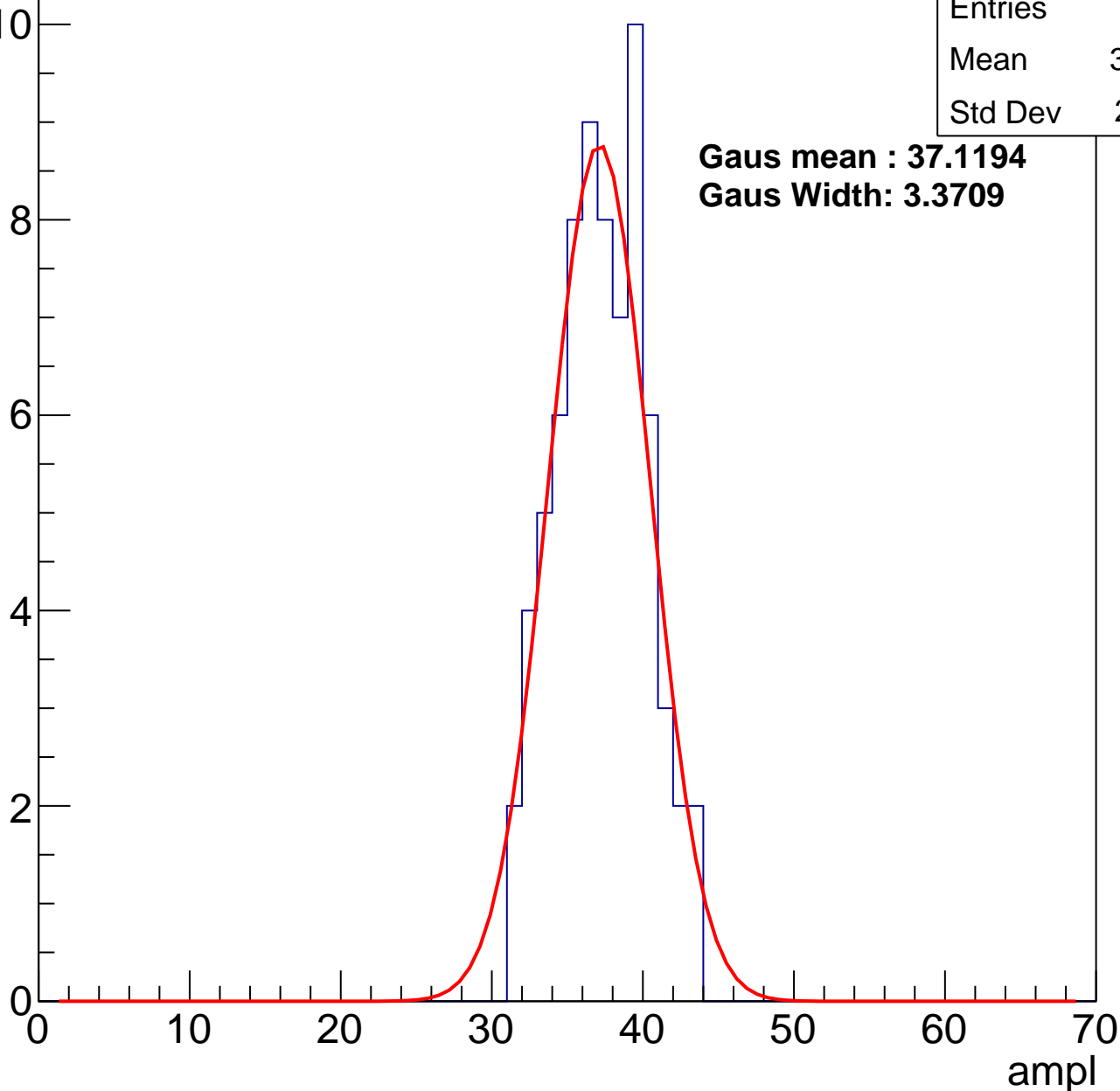
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	72
Mean	36.78
Std Dev	2.921

**Gaus mean : 37.1194**

**Gaus Width: 3.3709**



# B1L003S, U11-ch7, adc2

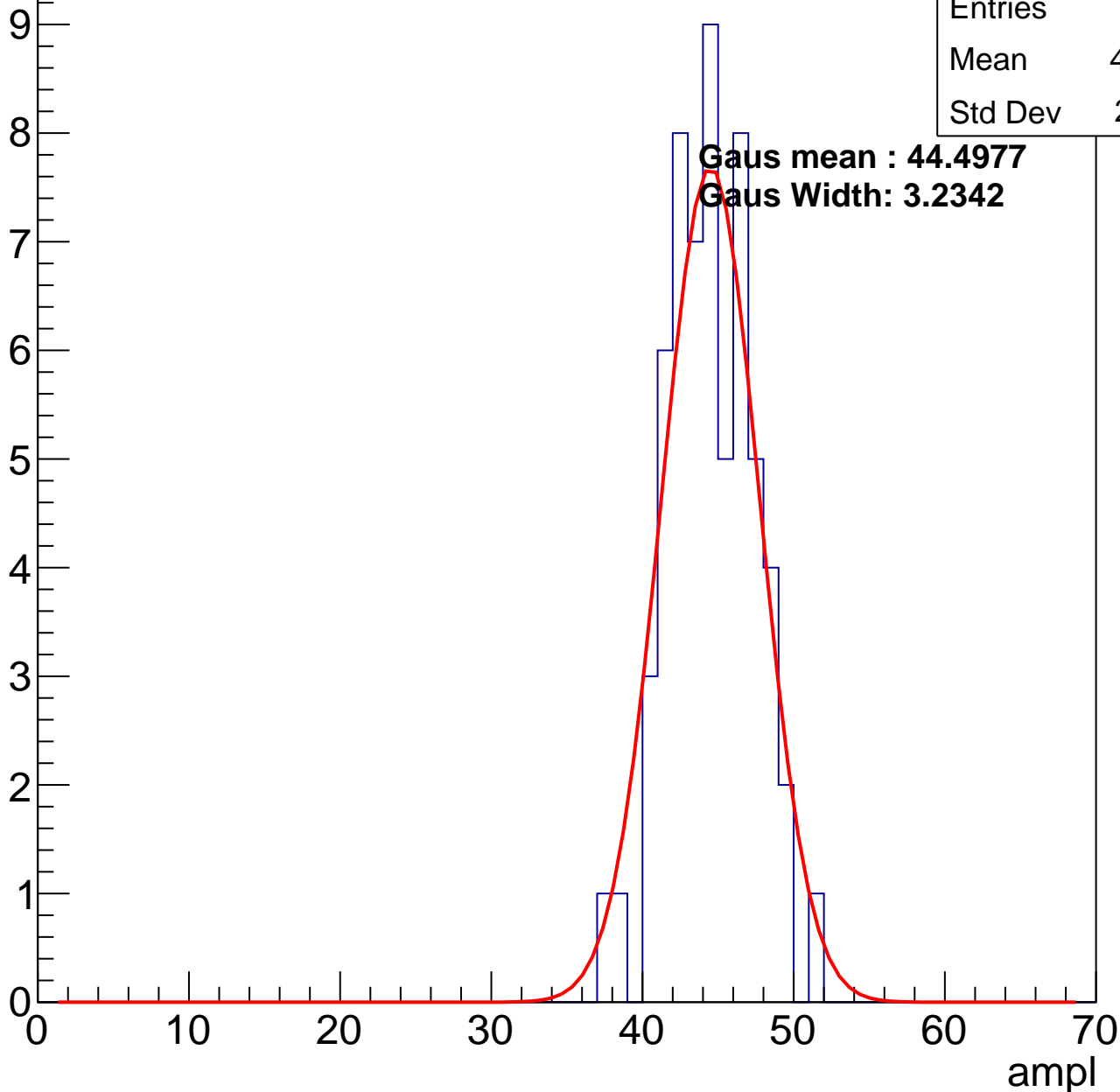
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	44.05
Std Dev	2.801

**Gaus mean : 44.4977**

**Gaus Width: 3.2342**

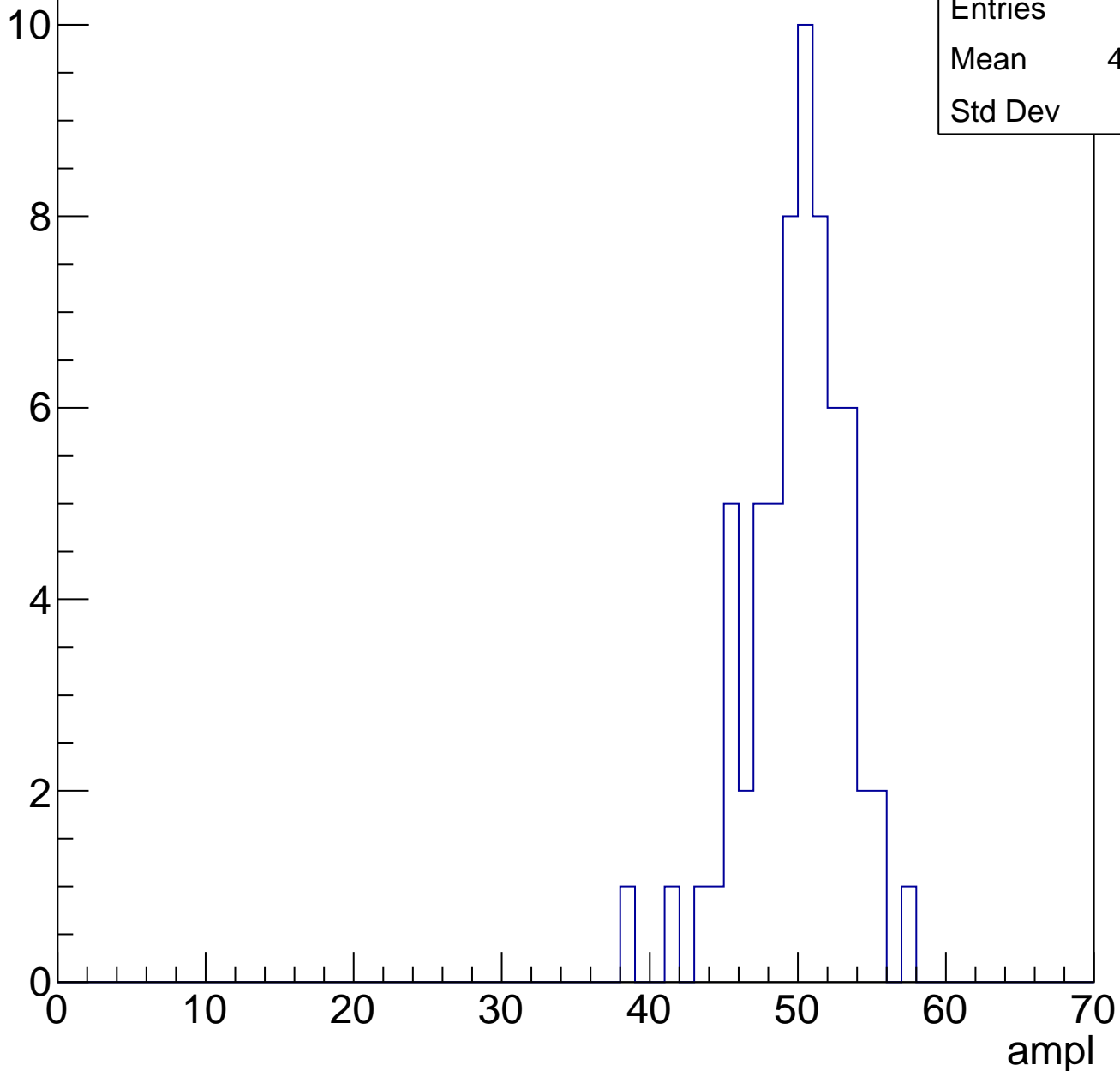


# B1L003S, U11-ch7, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	49.42
Std Dev	3.39

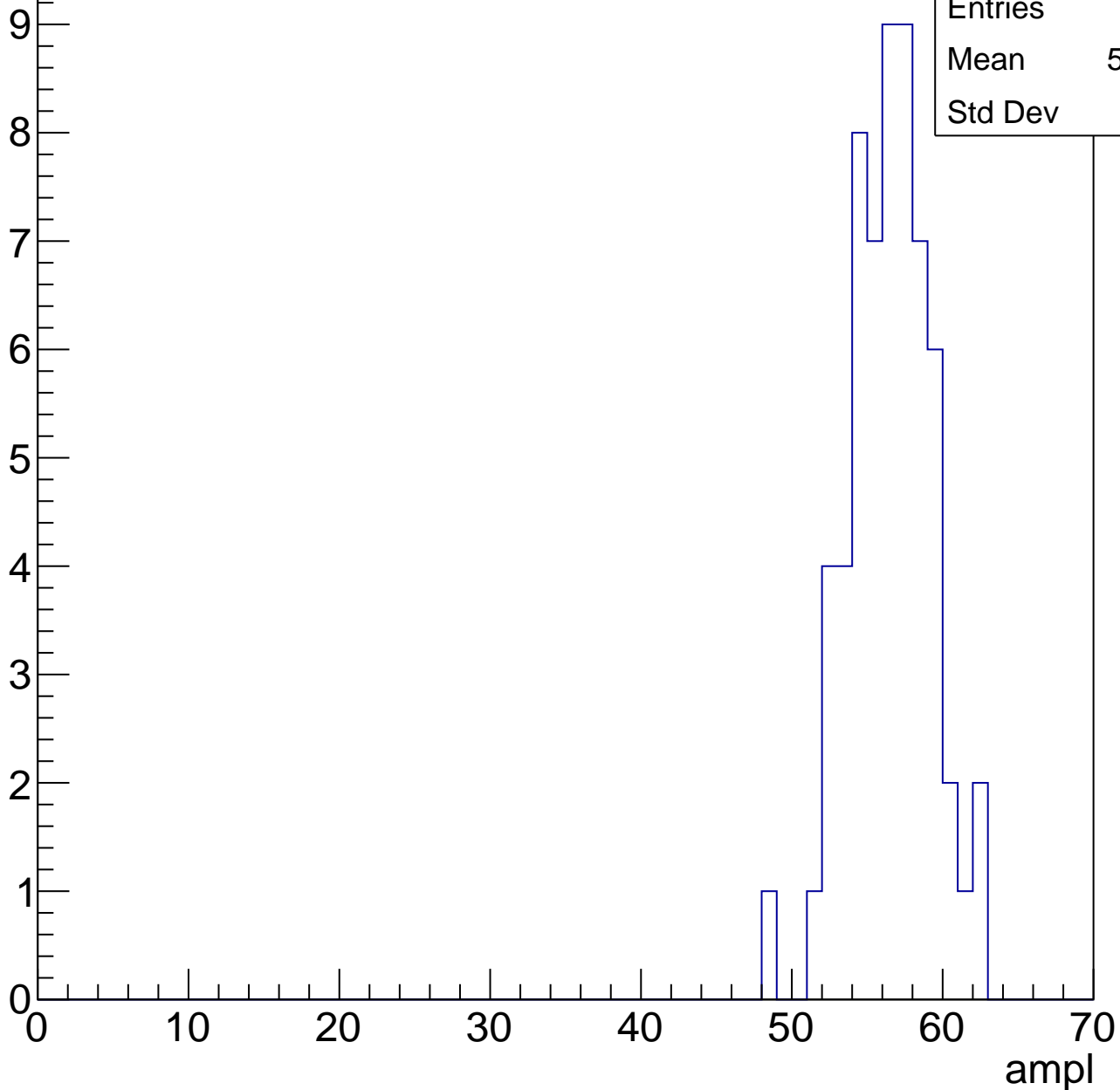


# B1L003S, U11-ch7, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	56.03
Std Dev	2.71

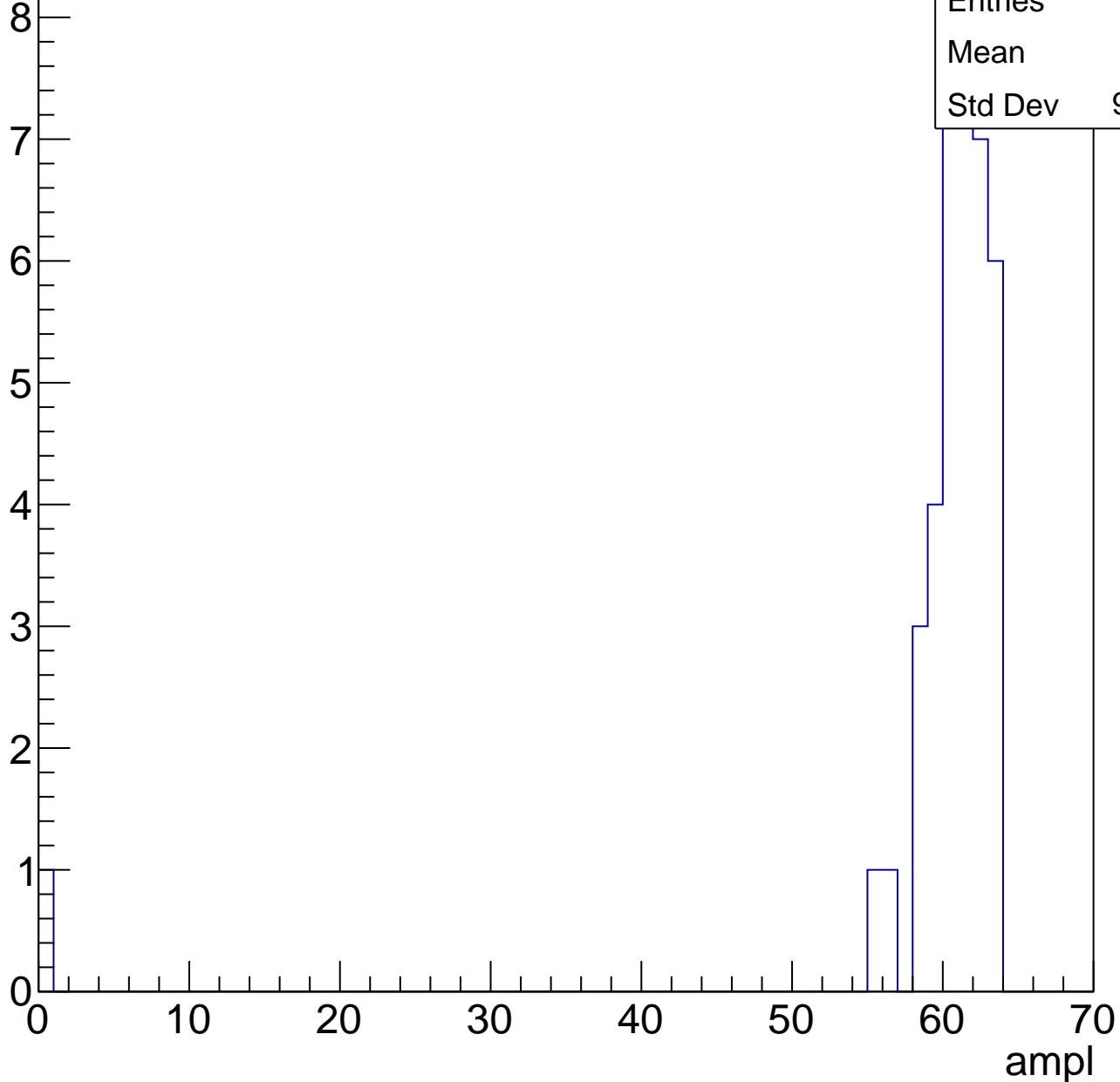


# B1L003S, U11-ch7, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

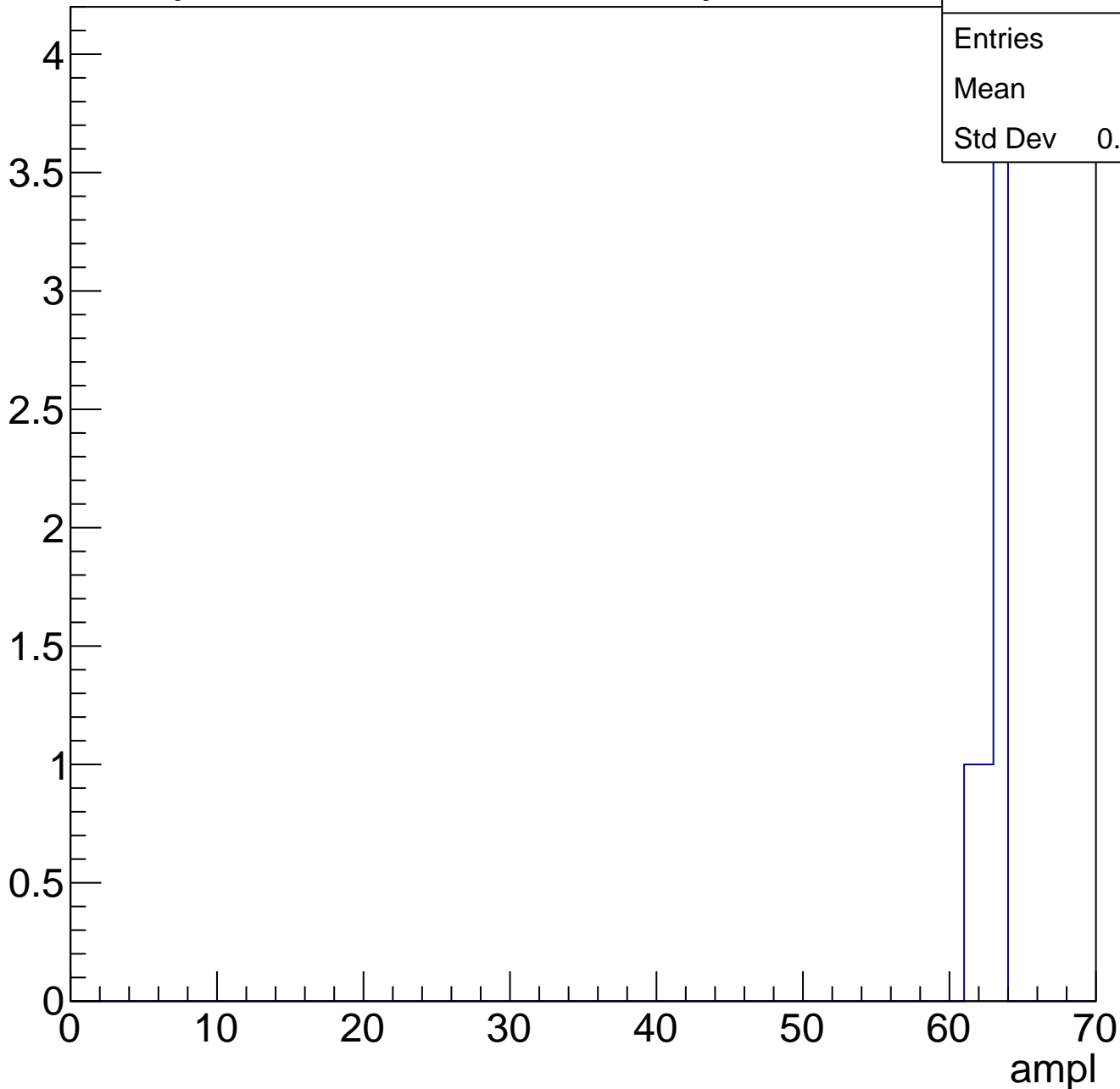
Entries	39
Mean	59
Std Dev	9.751



# B1L003S, U11-ch7, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch7, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U11-ch8, adc0

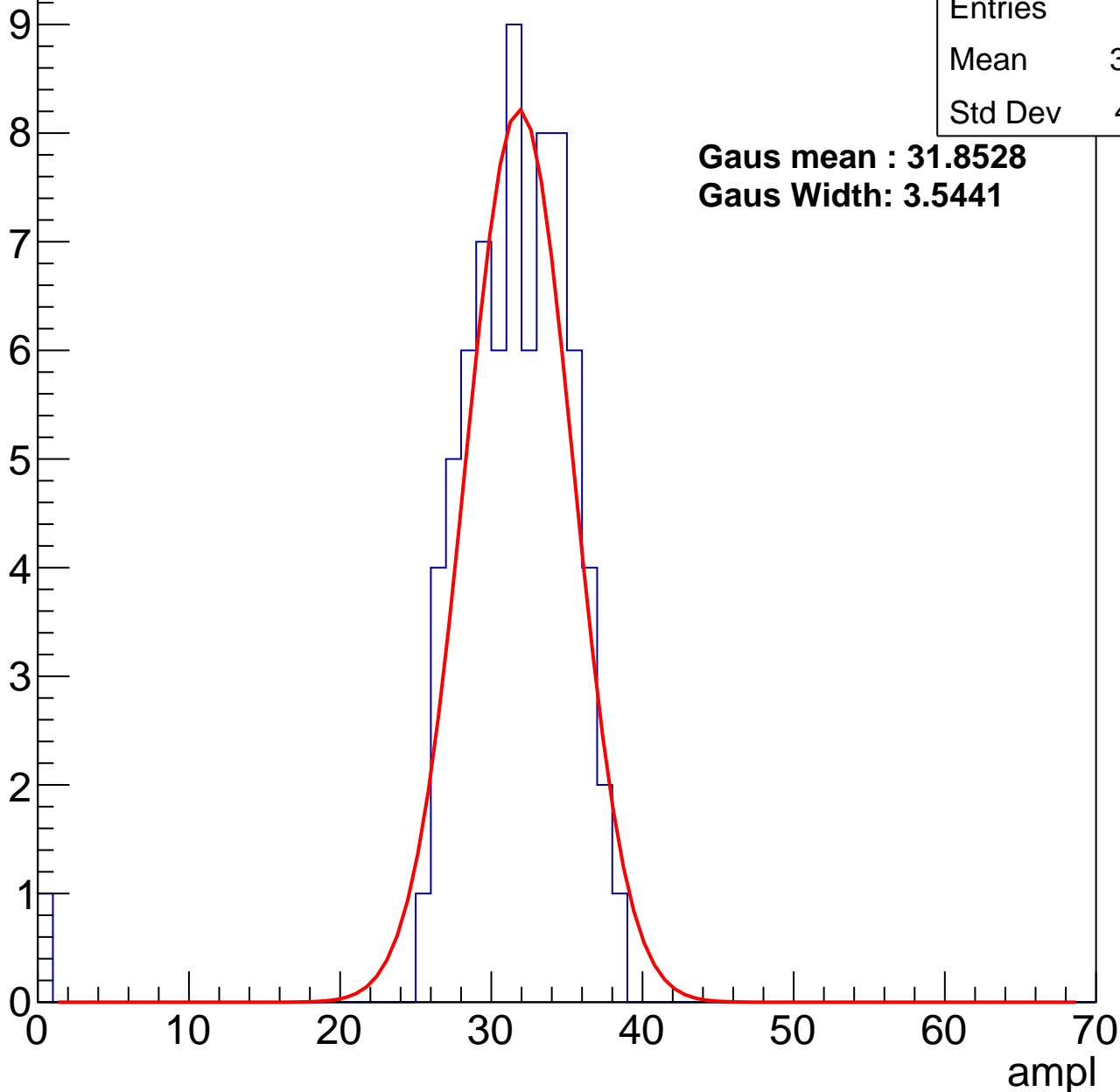
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	74
Mean	30.92
Std Dev	4.781

**Gaus mean : 31.8528**

**Gaus Width: 3.5441**



# B1L003S, U11-ch8, adc1

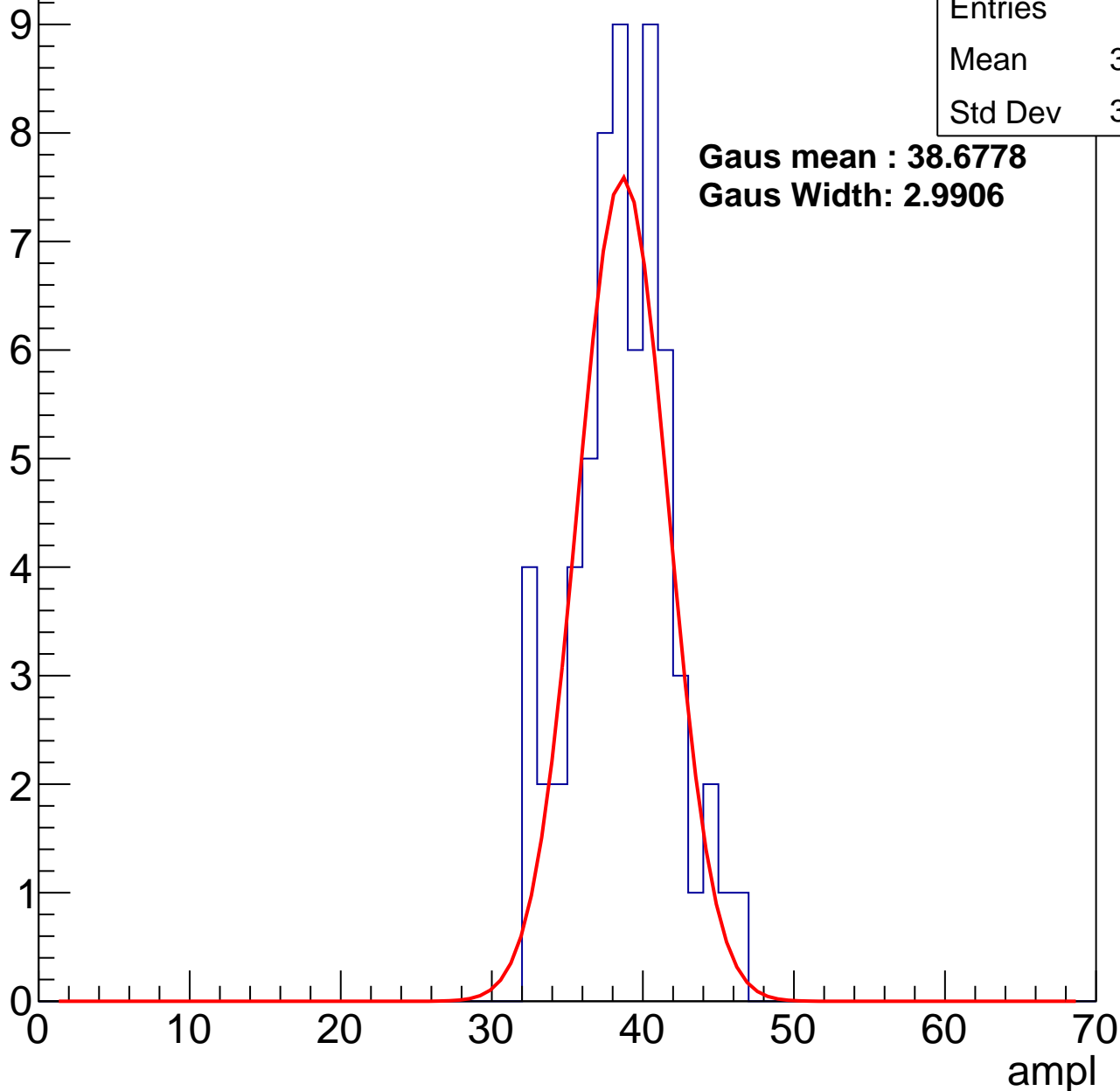
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	38.22
Std Dev	3.189

**Gaus mean : 38.6778**

**Gaus Width: 2.9906**



# B1L003S, U11-ch8, adc2

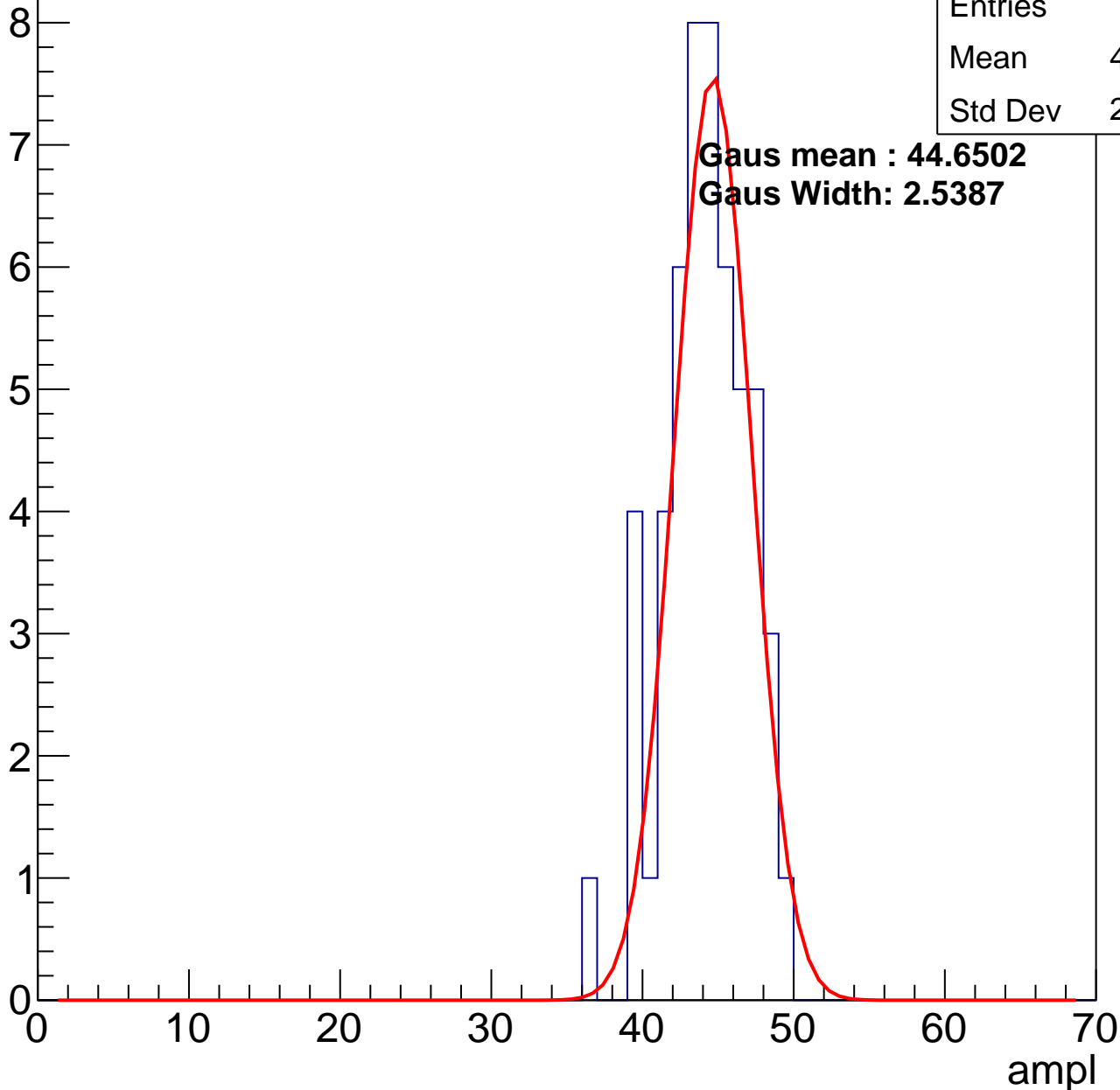
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	52
Mean	43.69
Std Dev	2.728

**Gaus mean : 44.6502**

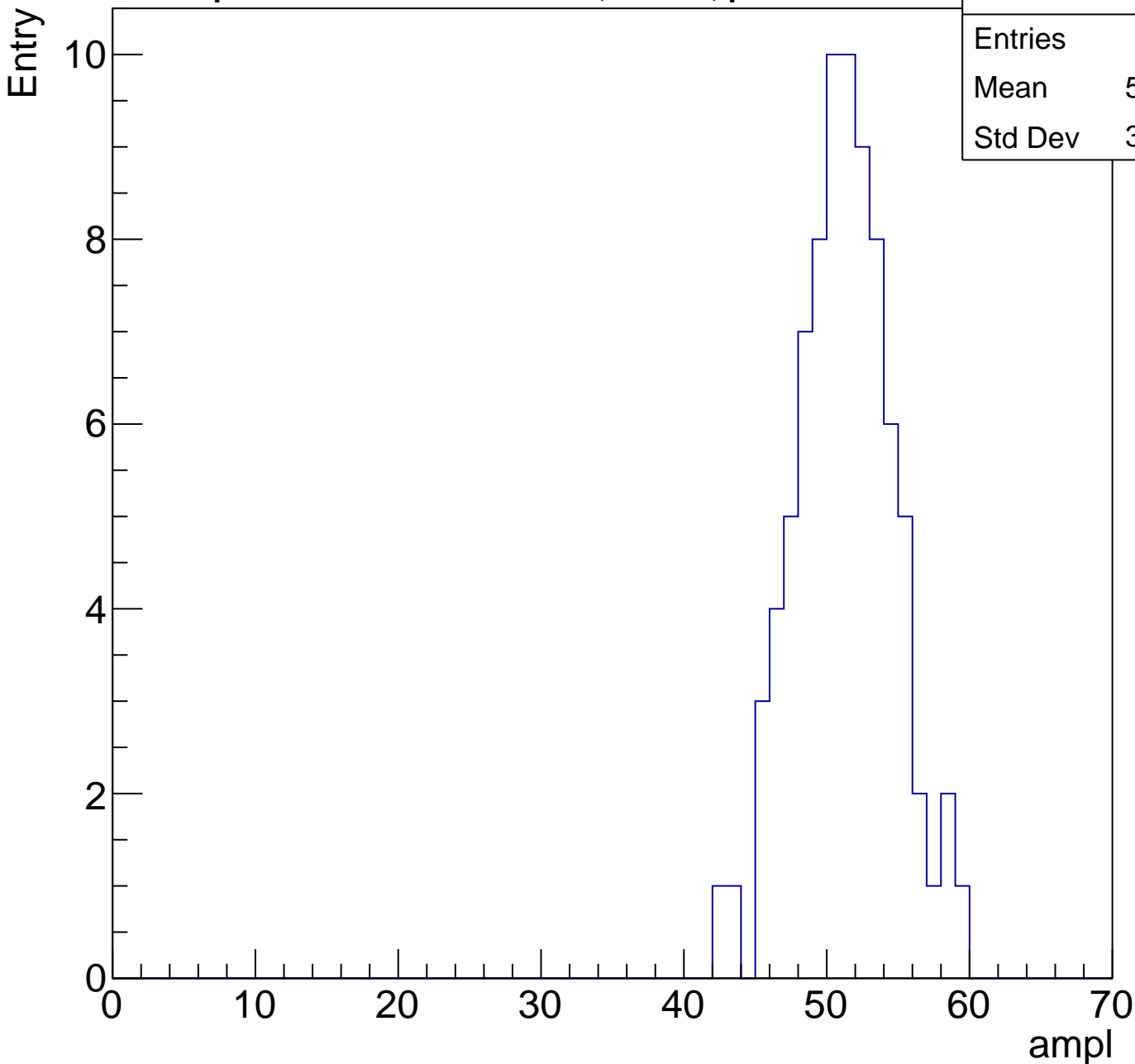
**Gaus Width: 2.5387**



# B1L003S, U11-ch8, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	83
Mean	50.75
Std Dev	3.393

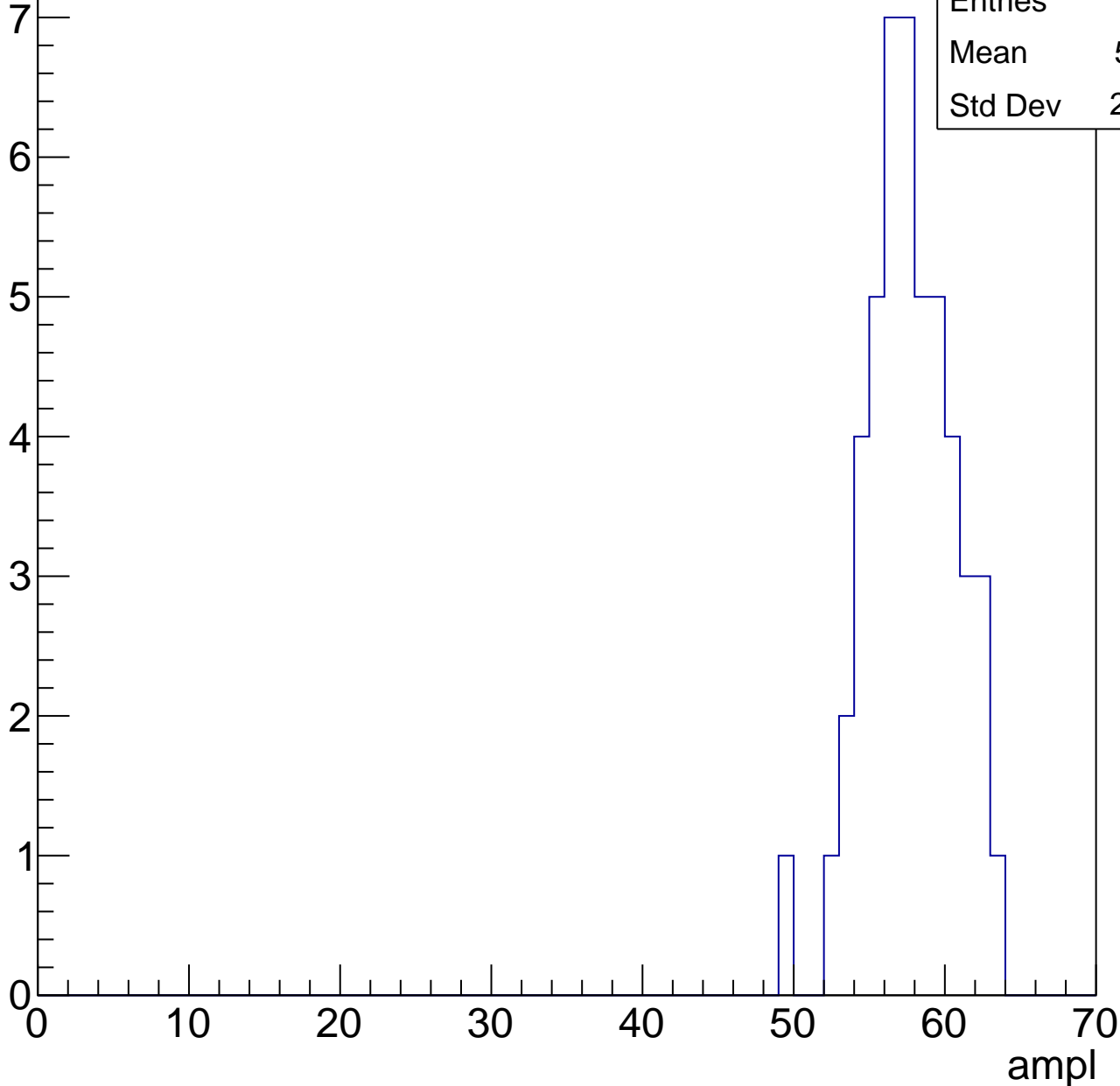


# B1L003S, U11-ch8, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	48
Mean	57.21
Std Dev	2.894

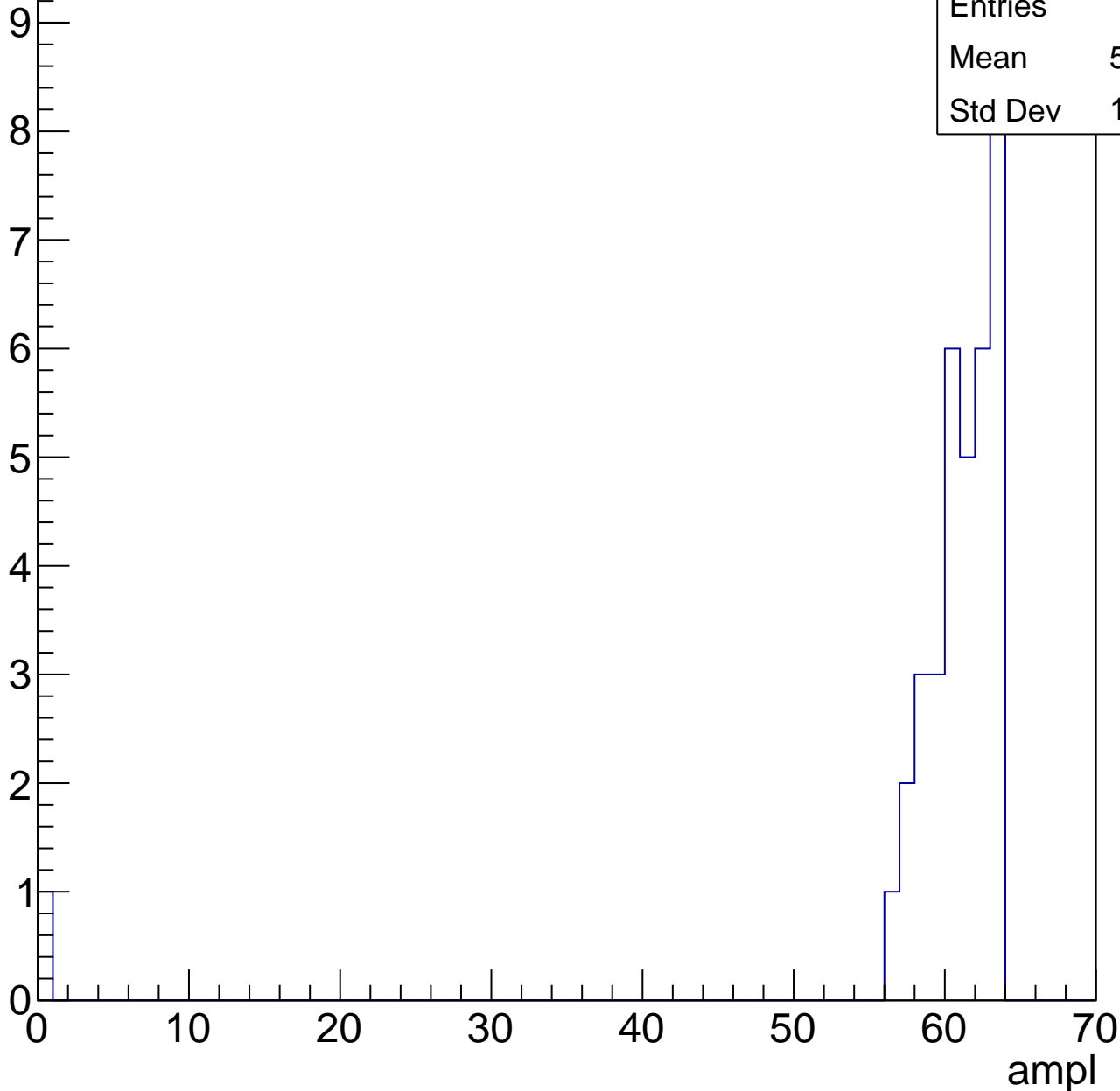


# B1L003S, U11-ch8, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

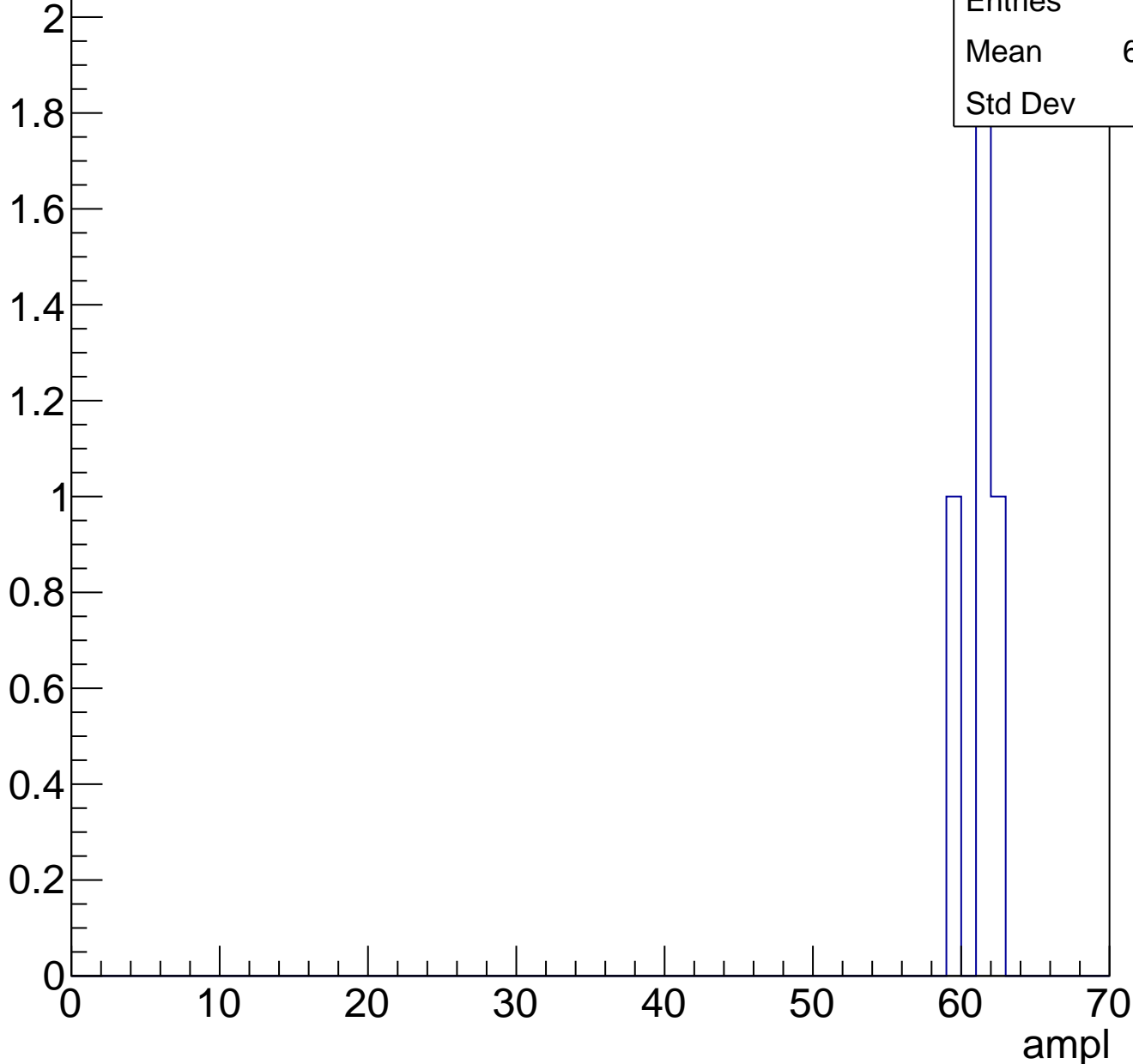
Entries	36
Mean	59.03
Std Dev	10.17



# B1L003S, U11-ch8, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

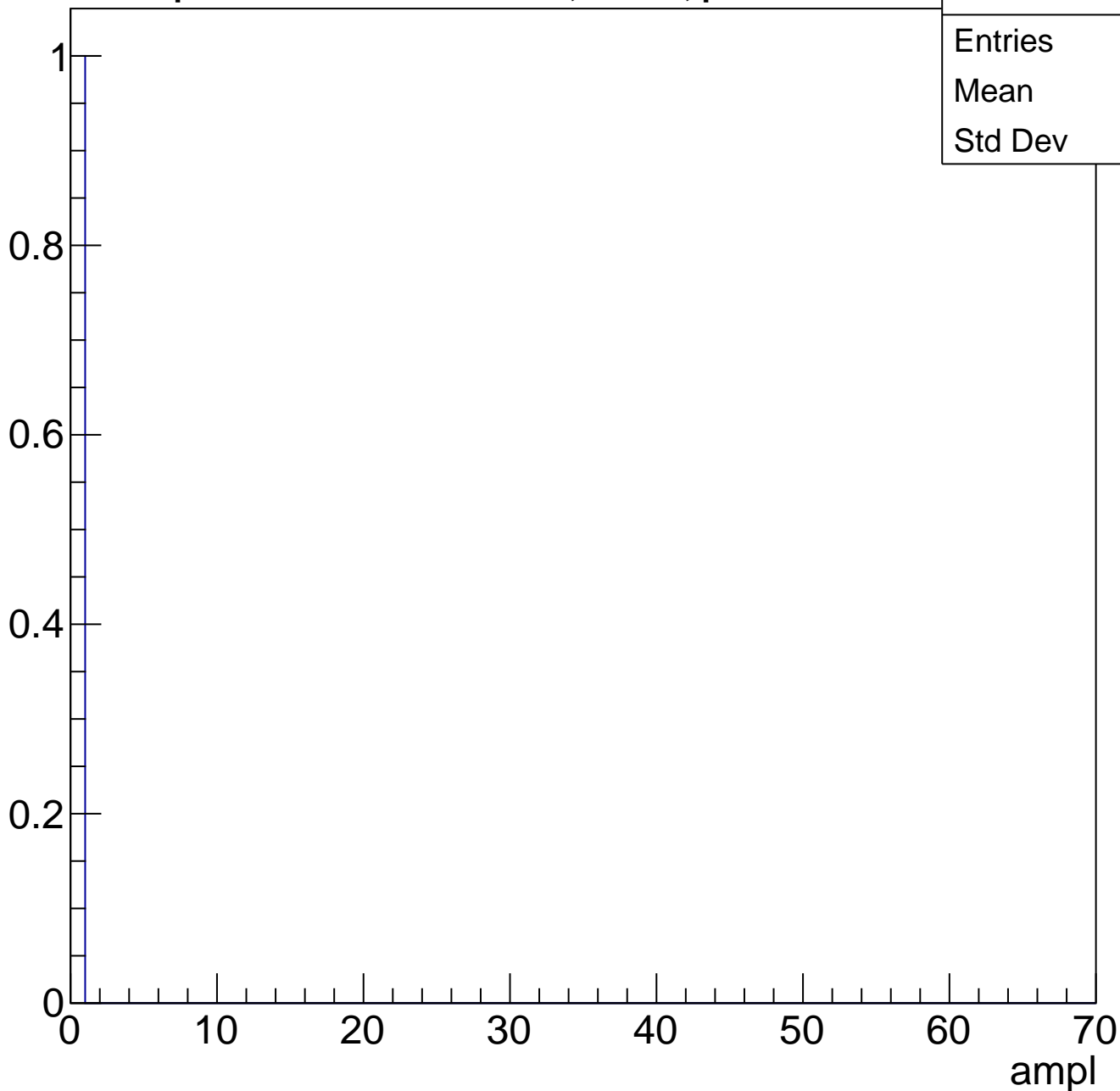




# B1L003S, U11-ch8, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U11-ch9, adc0

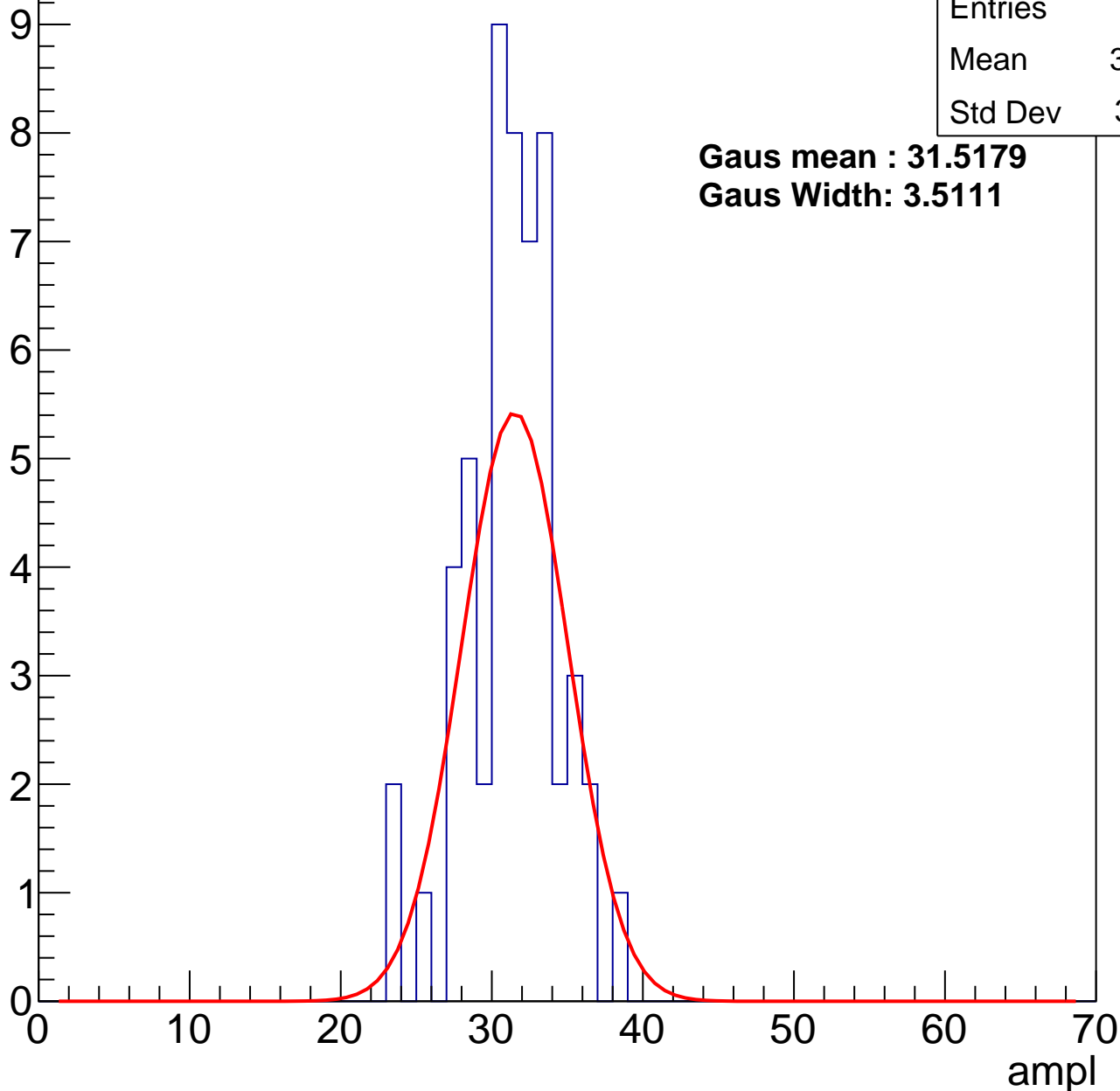
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	54
Mean	30.85
Std Dev	3.021

**Gaus mean : 31.5179**

**Gaus Width: 3.5111**



# B1L003S, U11-ch9, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	92
Mean	38.14
Std Dev	3.685

**Gaus mean : 38.7453**

**Gaus Width: 3.6777**

10

8

6

4

2

0

0

10

20

30

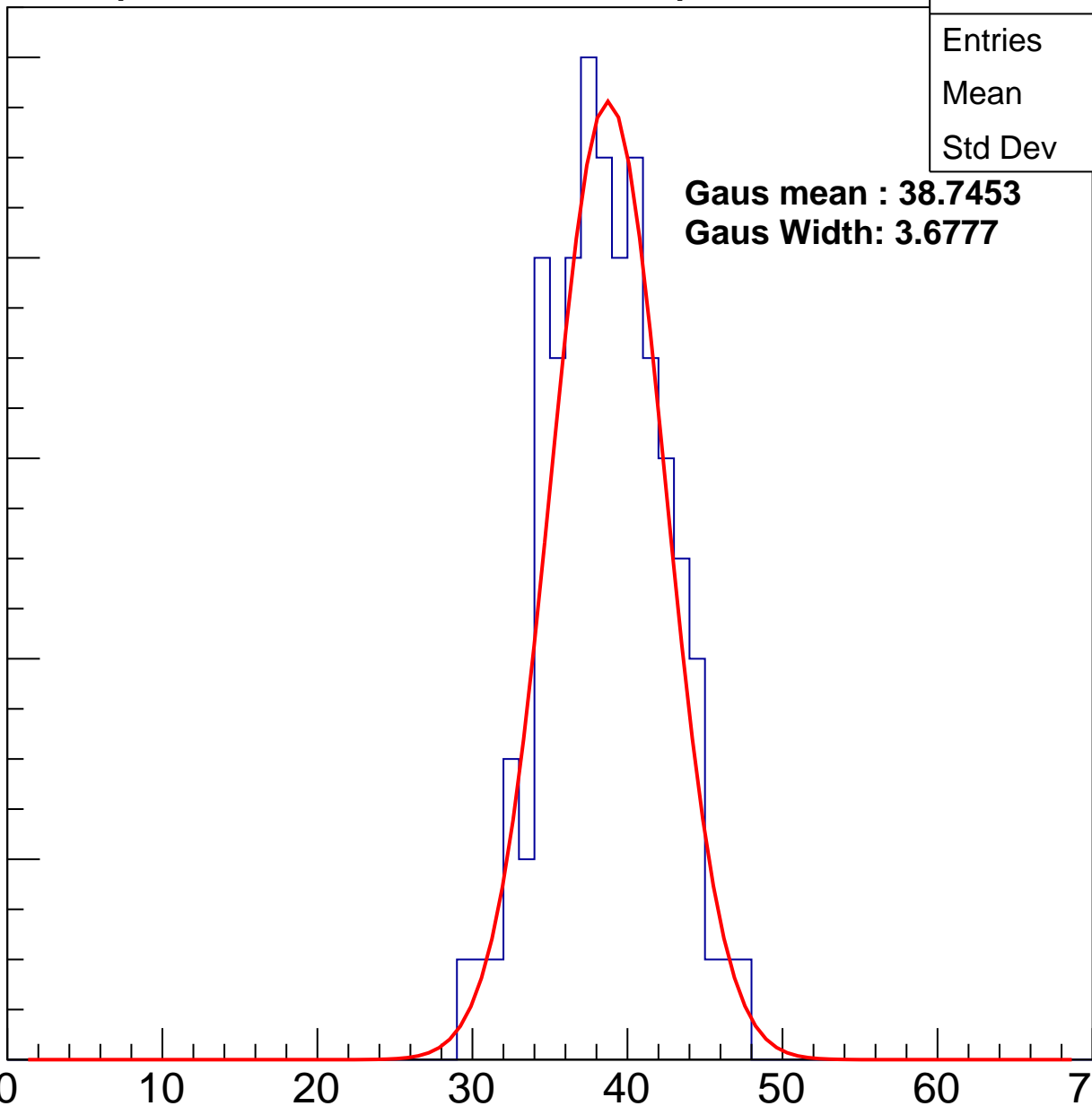
40

50

60

70

ampl



# B1L003S, U11-ch9, adc2

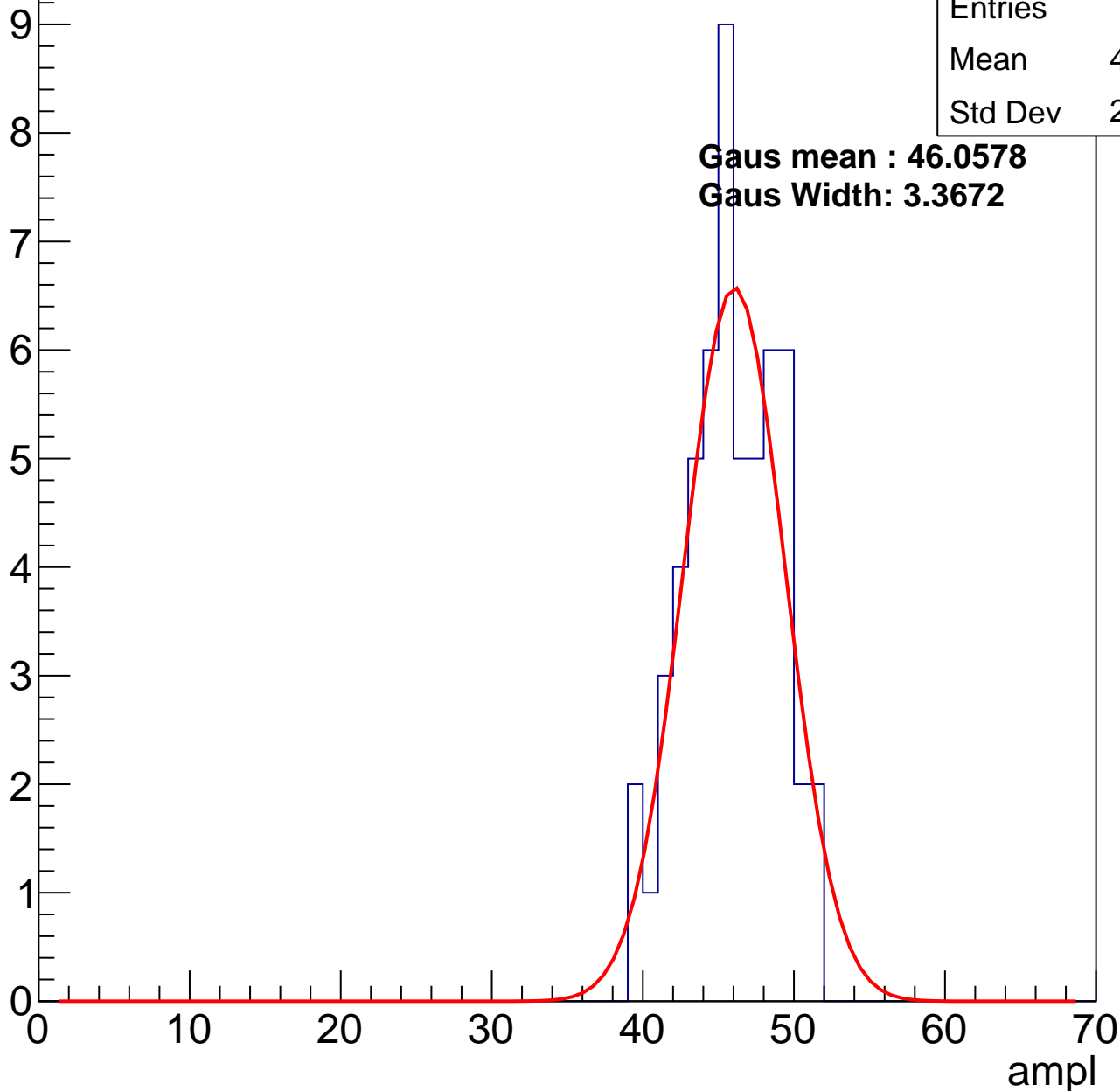
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	45.39
Std Dev	2.974

**Gaus mean : 46.0578**

**Gaus Width: 3.3672**



# B1L003S, U11-ch9, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	75
Mean	52.03
Std Dev	3.225

Entry

10

8

6

4

2

0

0

10

20

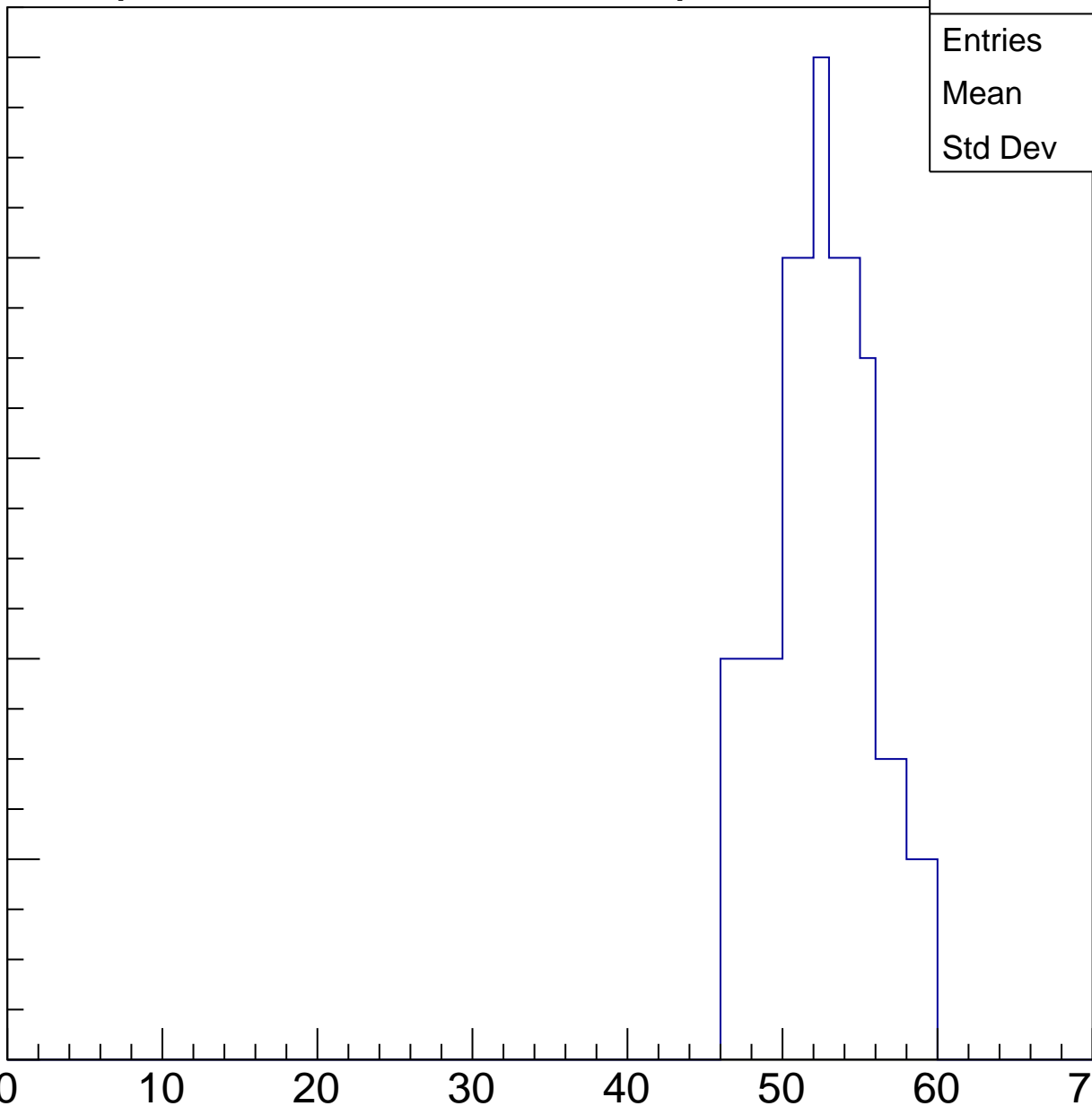
30

40

50

60

ampl

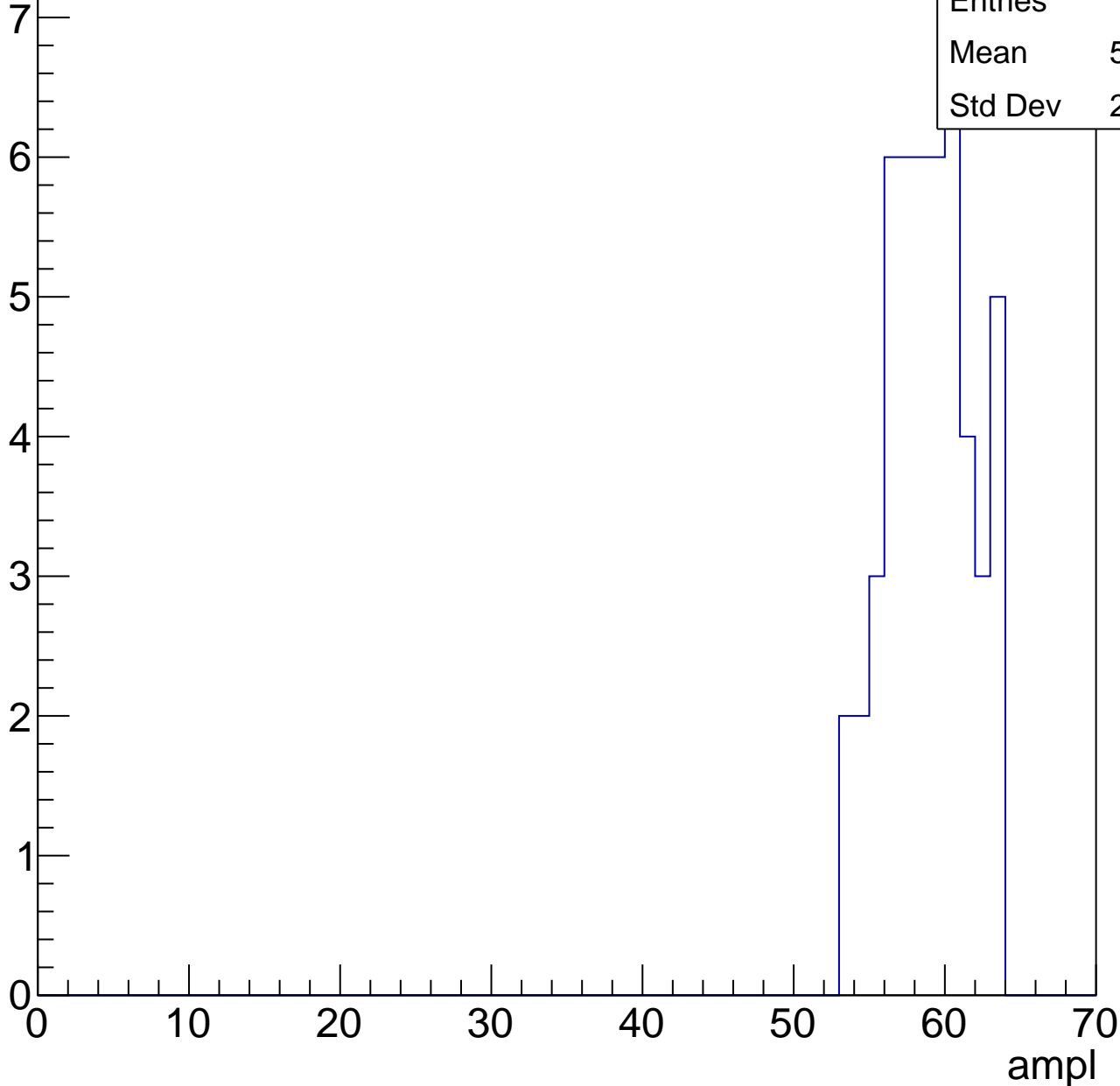


# B1L003S, U11-ch9, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	50
Mean	58.48
Std Dev	2.722

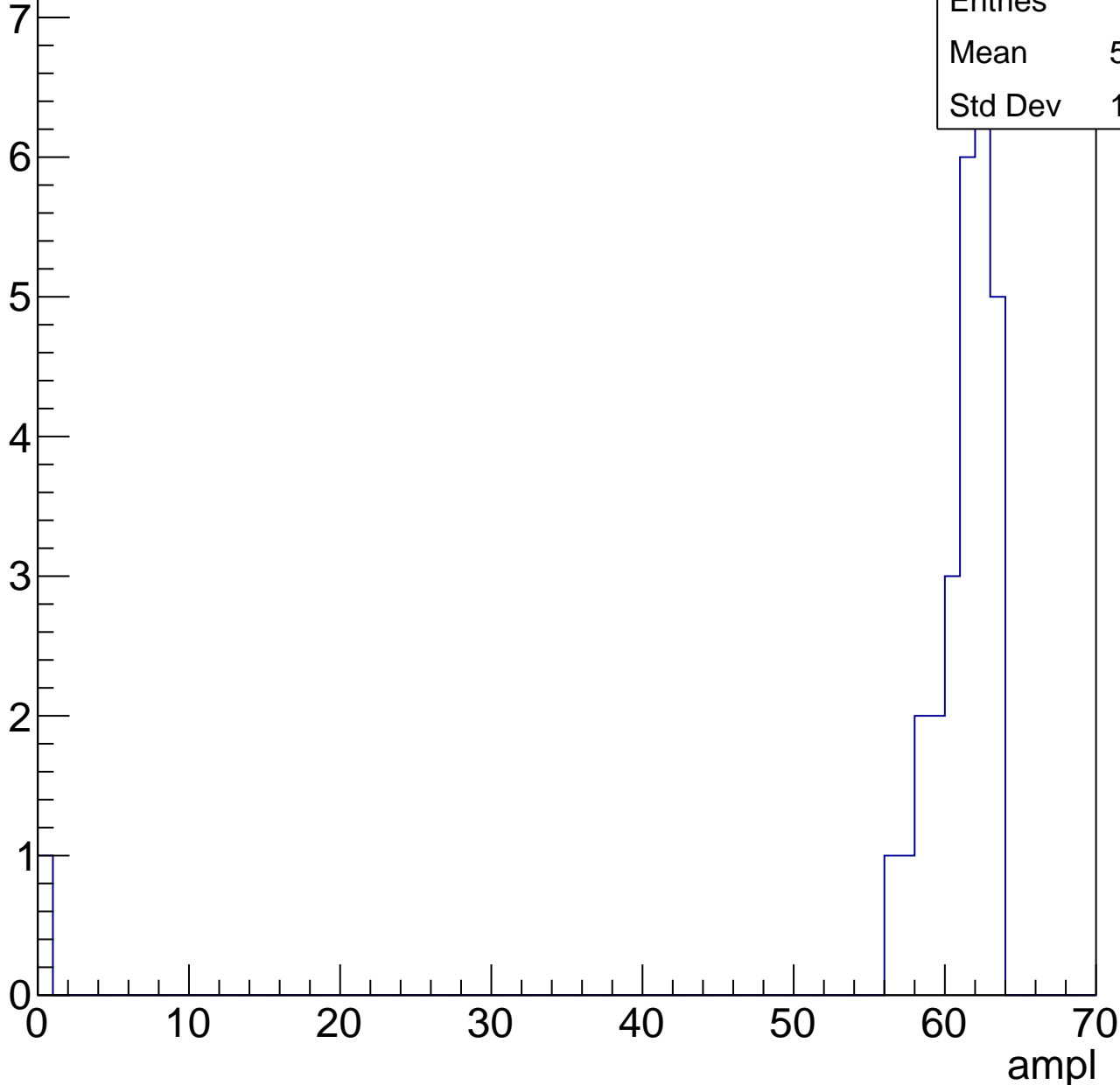


# B1L003S, U11-ch9, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	28
Mean	58.64
Std Dev	11.44



# B1L003S, U11-ch9, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L003S, U11-ch9, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U11-ch10, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	85
Mean	30.62
Std Dev	5.827

**Gaus mean : 31.8840**

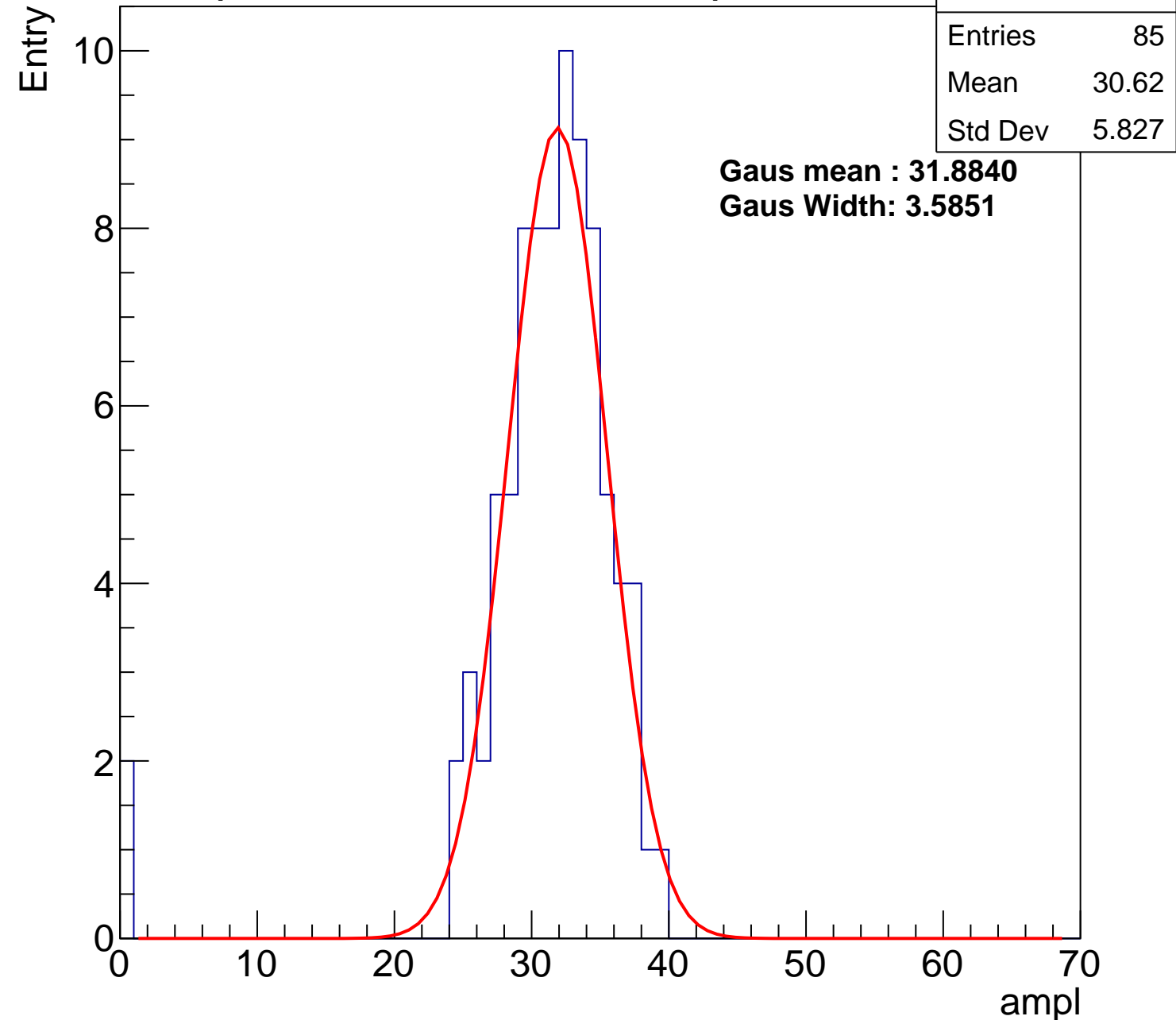
**Gaus Width: 3.5851**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U11-ch10, adc1

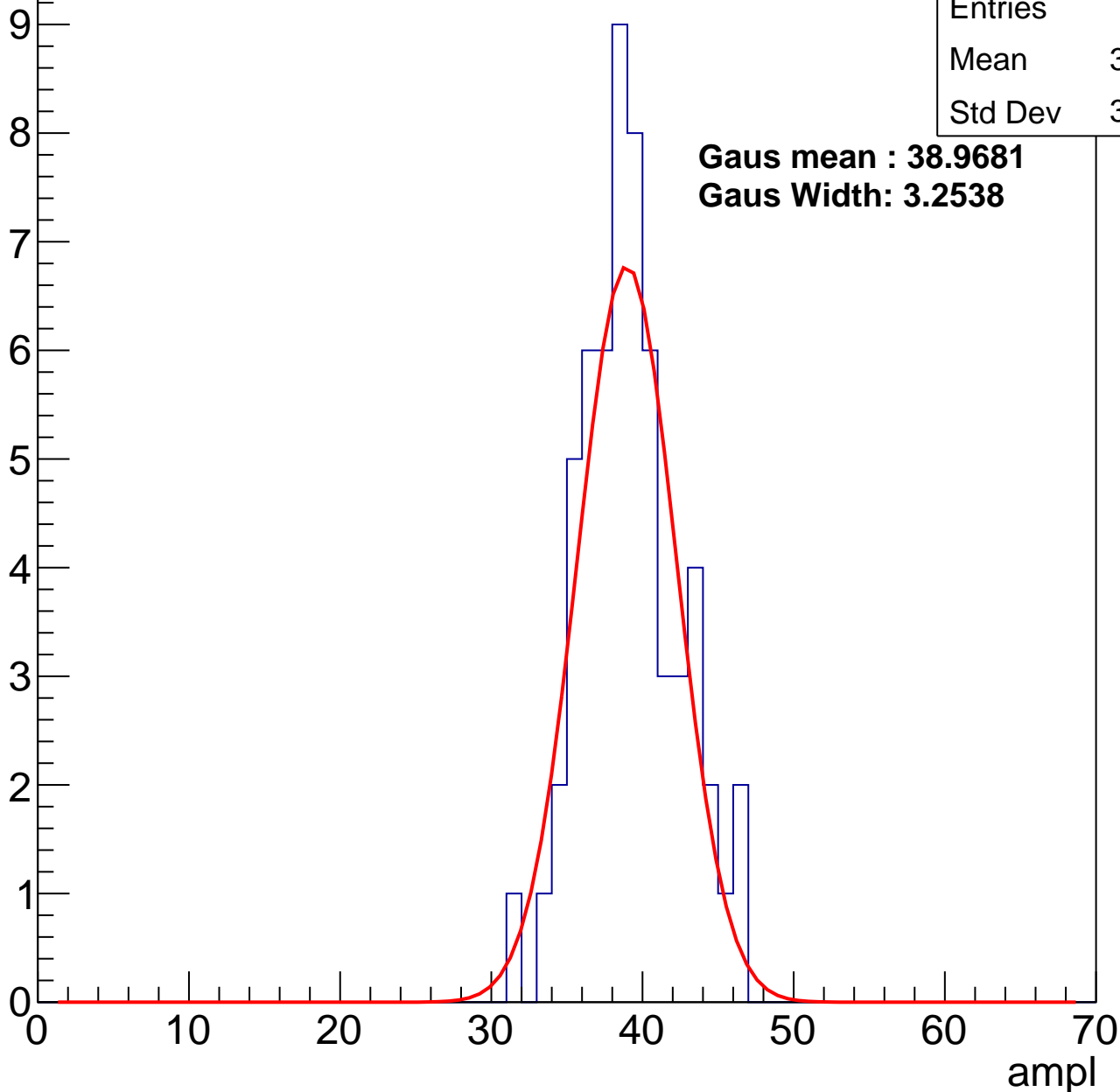
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	38.73
Std Dev	3.204

**Gaus mean : 38.9681**

**Gaus Width: 3.2538**



# B1L003S, U11-ch10, adc2

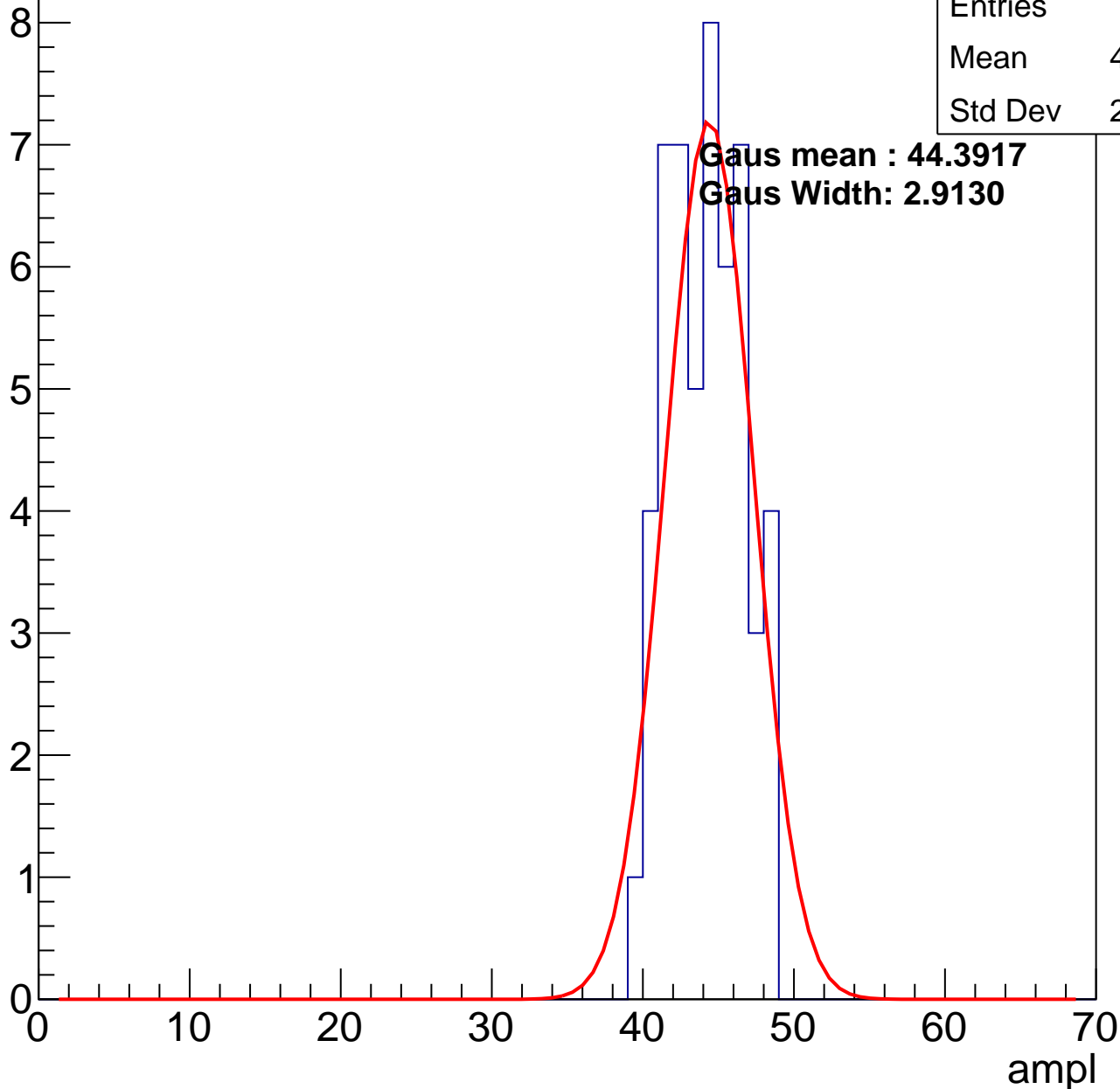
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	52
Mean	43.69
Std Dev	2.422

**Gaus mean : 44.3917**

**Gaus Width: 2.9130**

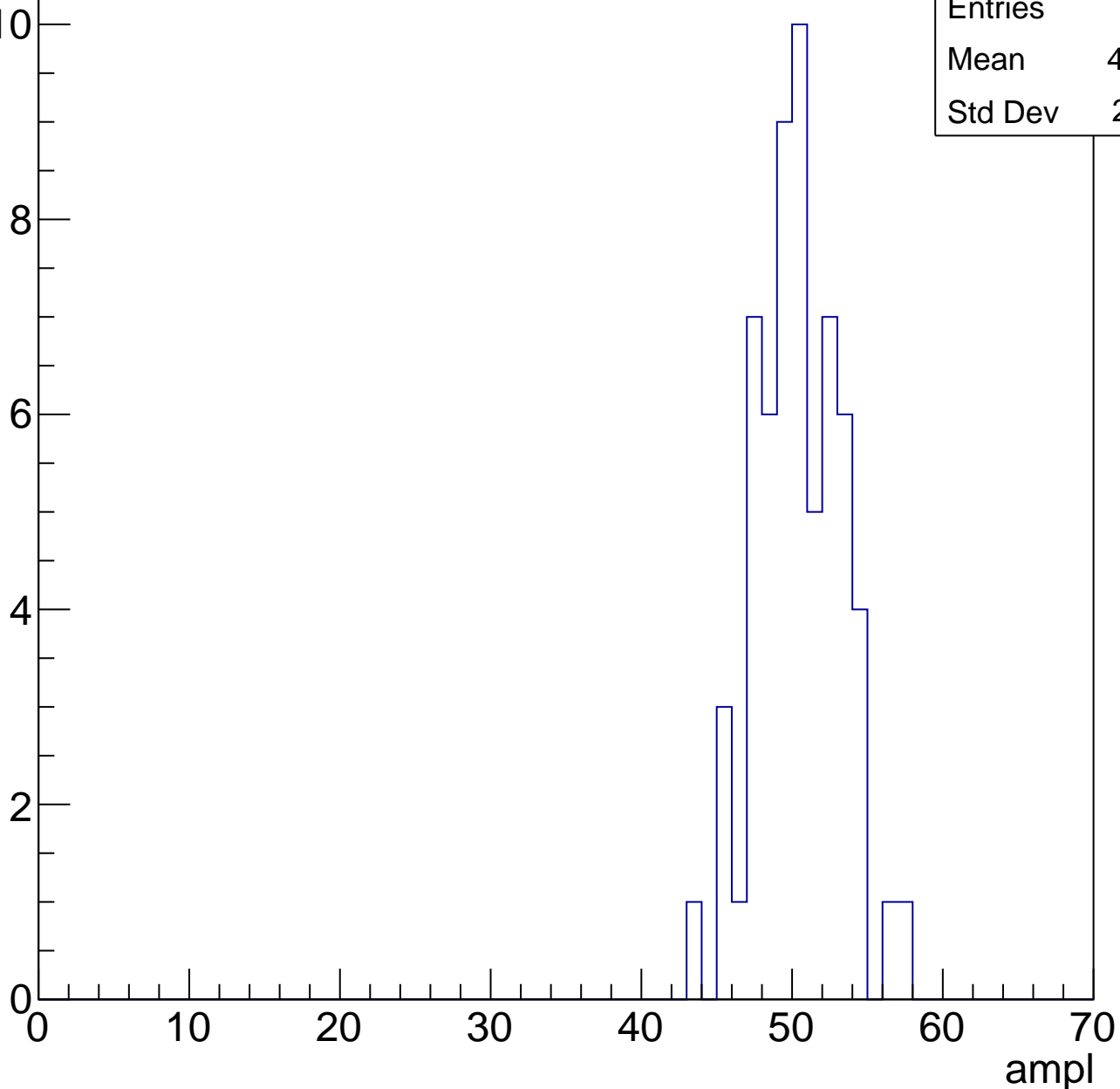


# B1L003S, U11-ch10, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	49.97
Std Dev	2.781

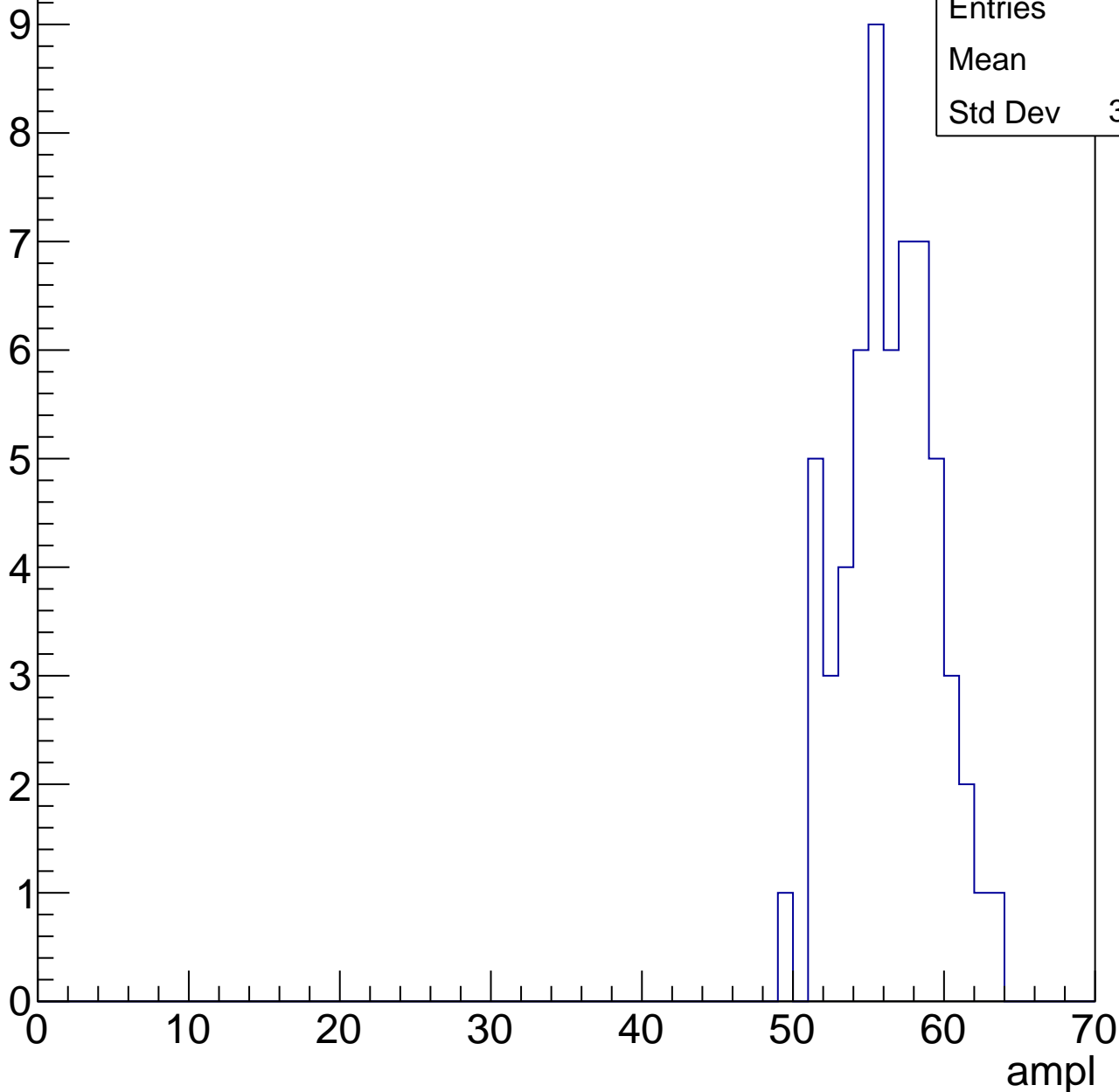


# B1L003S, U11-ch10, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	55.9
Std Dev	3.037

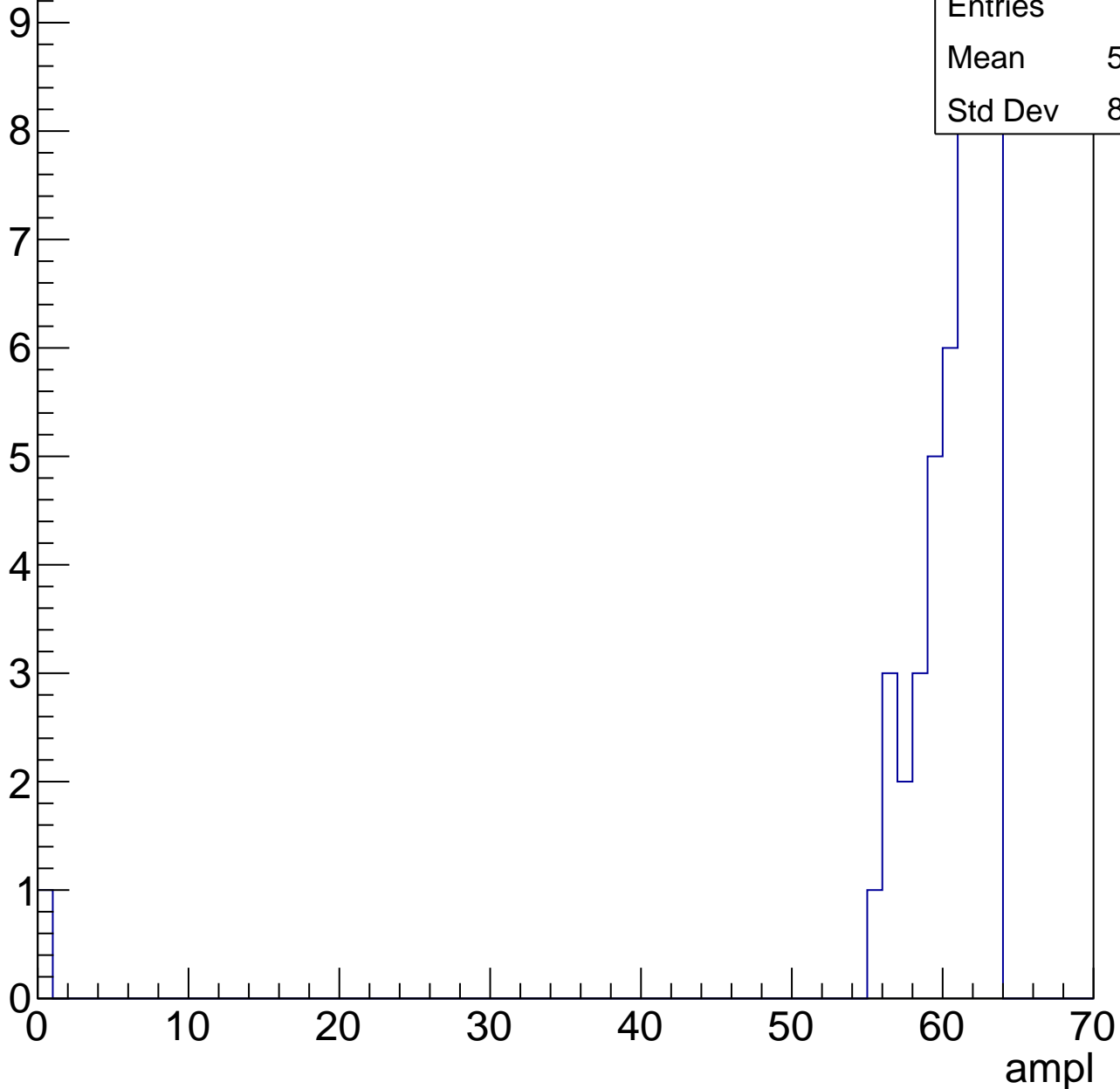


# B1L003S, U11-ch10, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	47
Mean	59.13
Std Dev	8.988



# B1L003S, U11-ch10, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	60
Std Dev	0



# B1L003S, U11-ch10, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U11-ch11, adc0

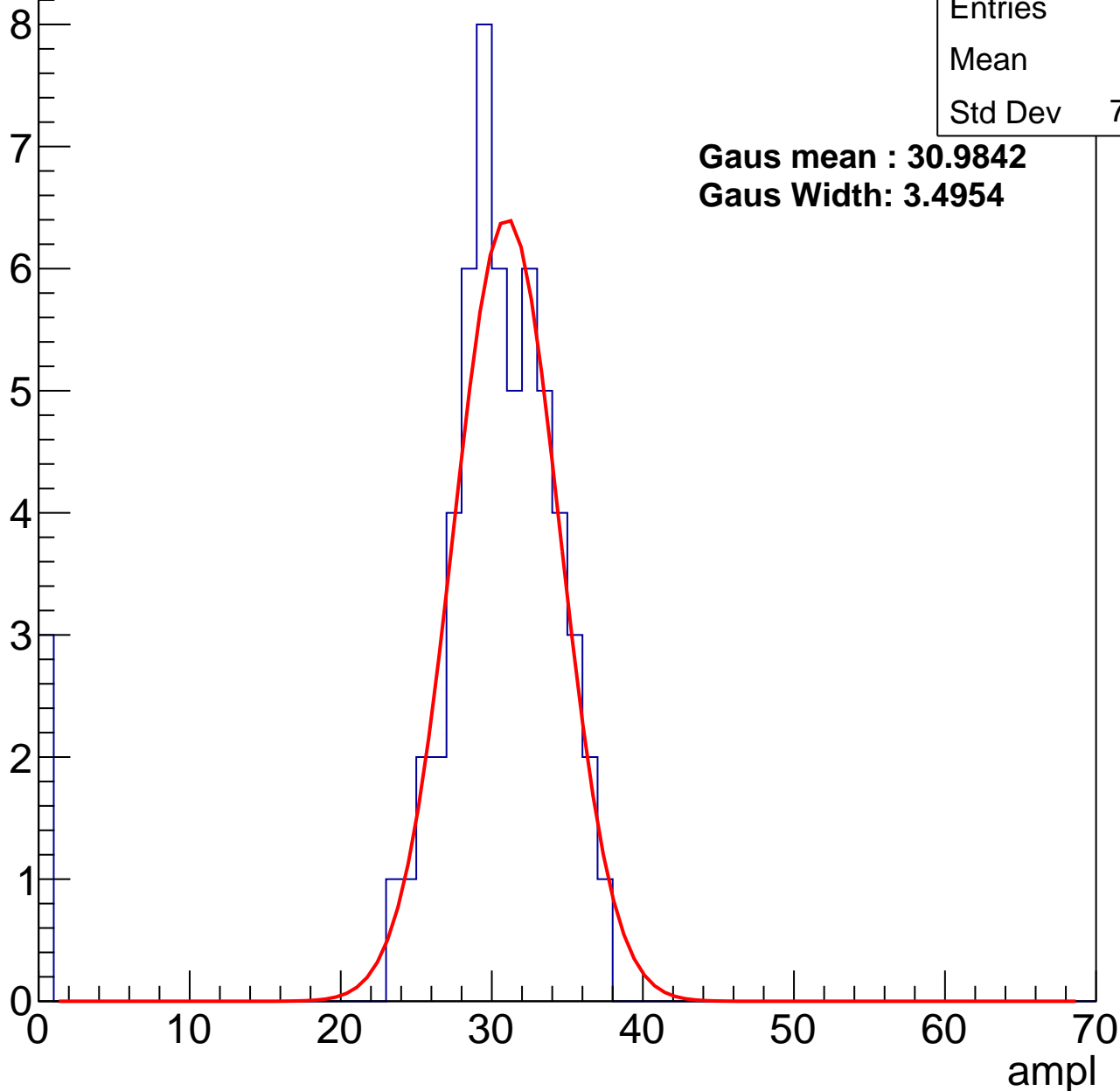
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	28.8
Std Dev	7.346

**Gaus mean : 30.9842**

**Gaus Width: 3.4954**



# B1L003S, U11-ch11, adc1

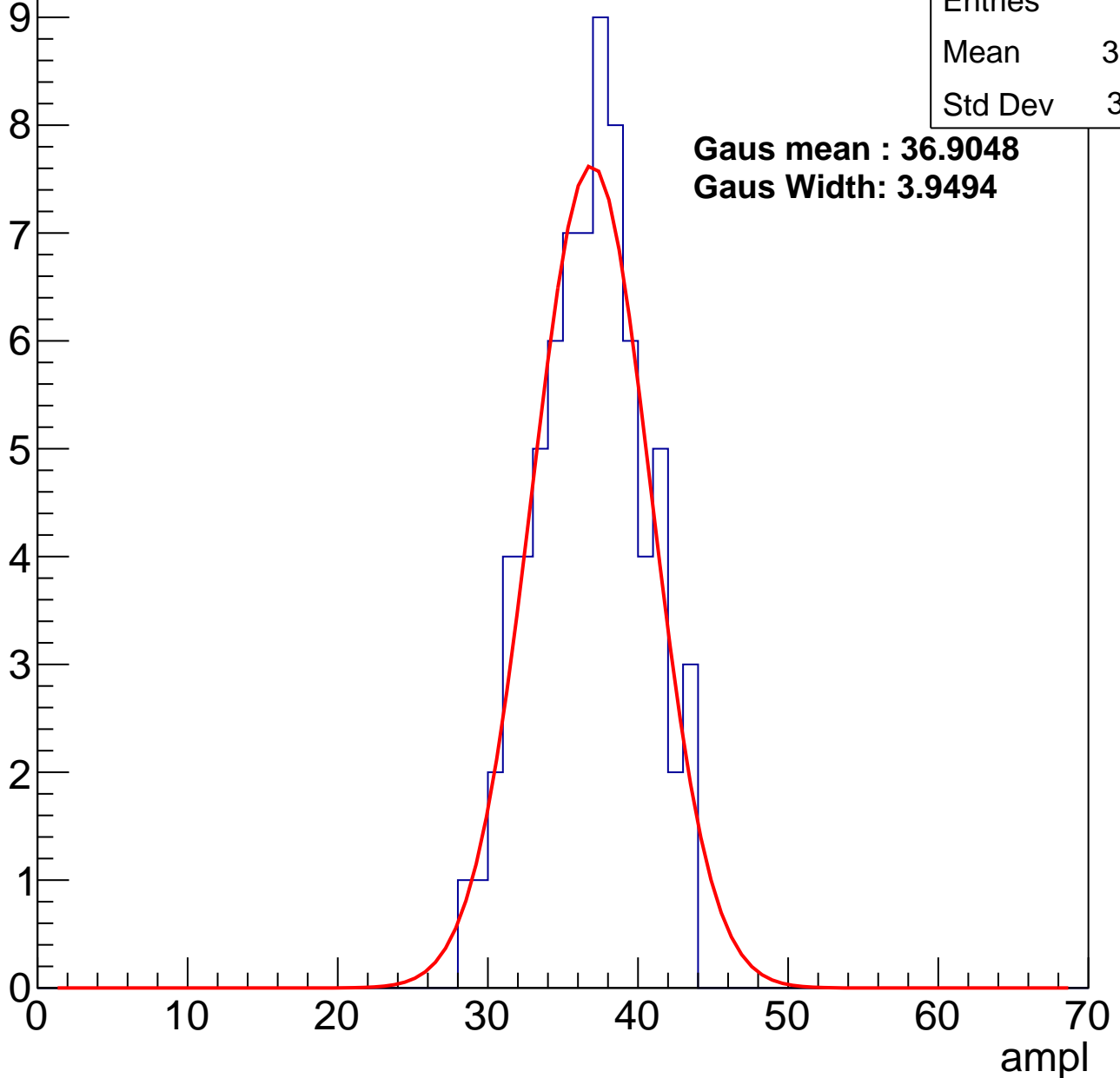
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	74
Mean	36.27
Std Dev	3.531

**Gaus mean : 36.9048**

**Gaus Width: 3.9494**



# B1L003S, U11-ch11, adc2

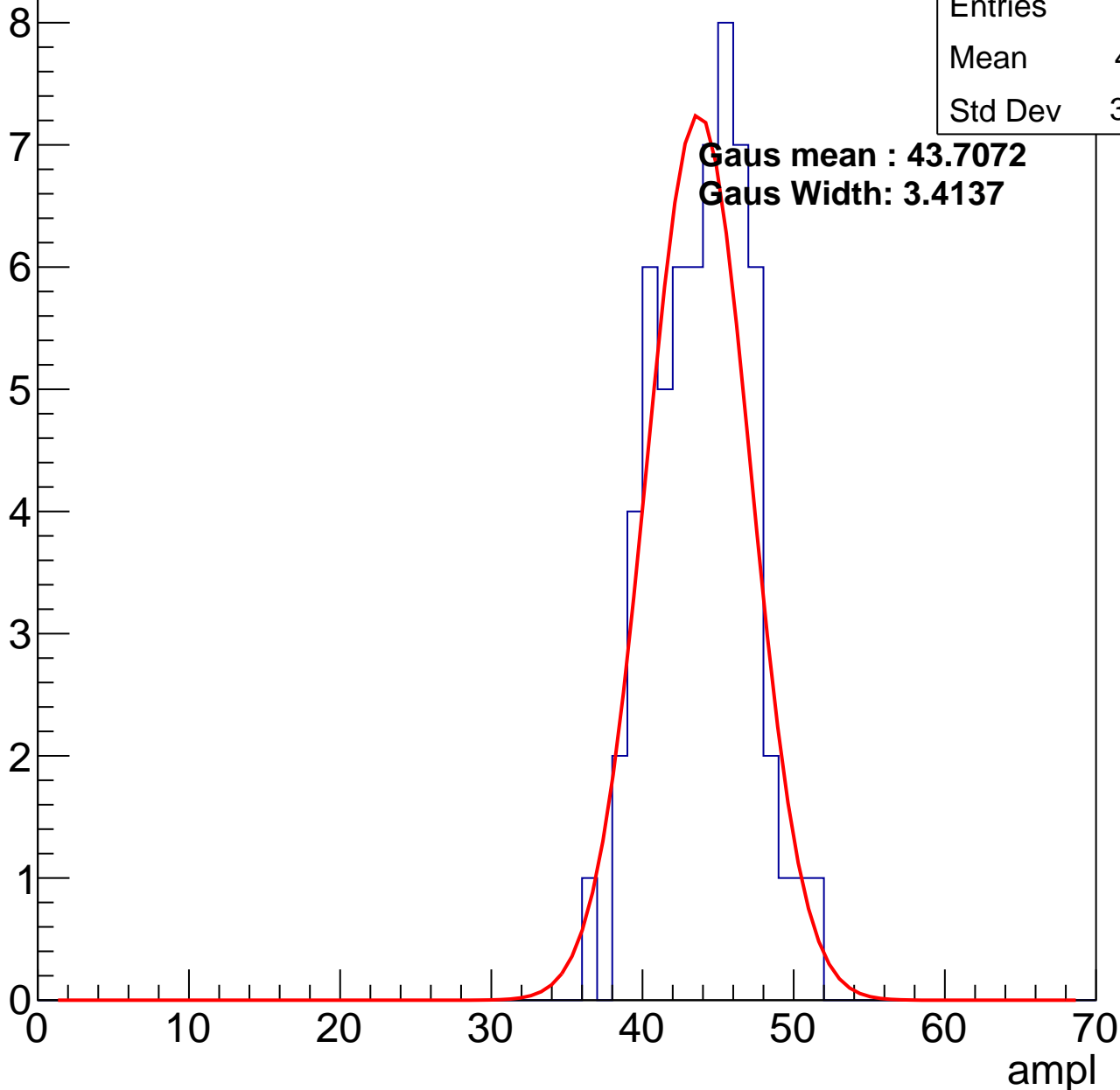
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	43.51
Std Dev	3.147

**Gaus mean : 43.7072**

**Gaus Width: 3.4137**

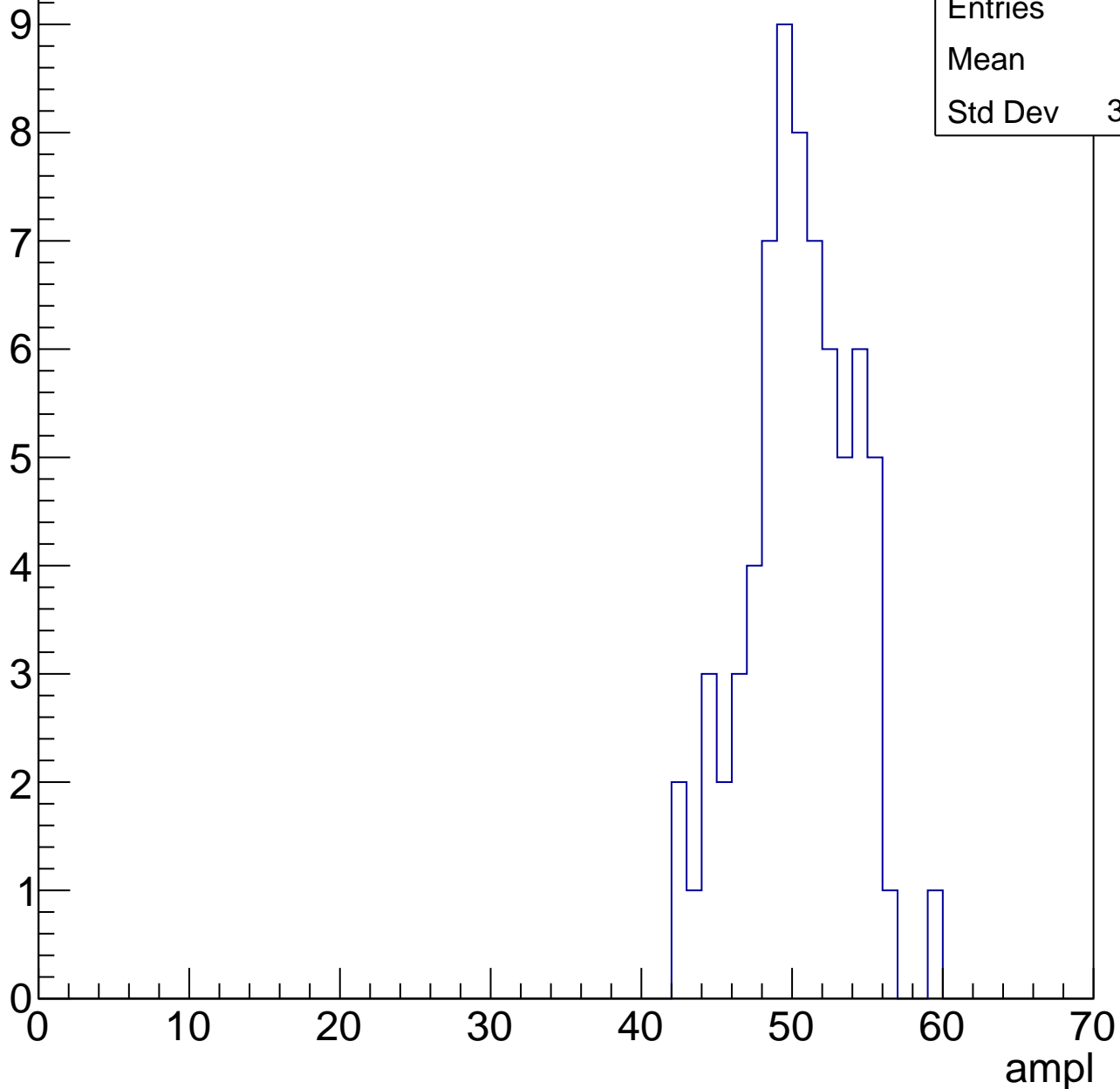


# B1L003S, U11-ch11, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	50
Std Dev	3.525

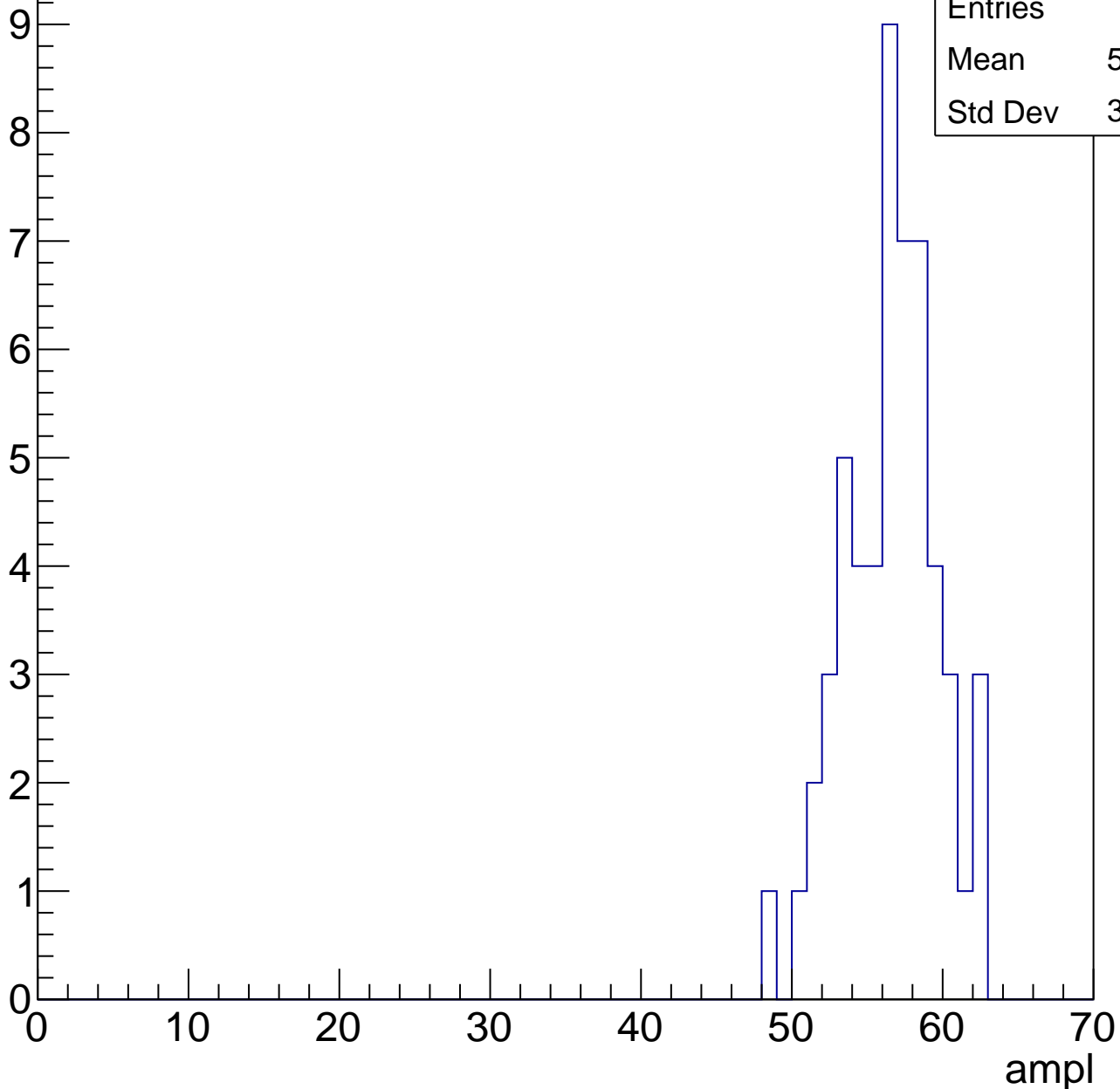


# B1L003S, U11-ch11, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	54
Mean	56.09
Std Dev	3.087

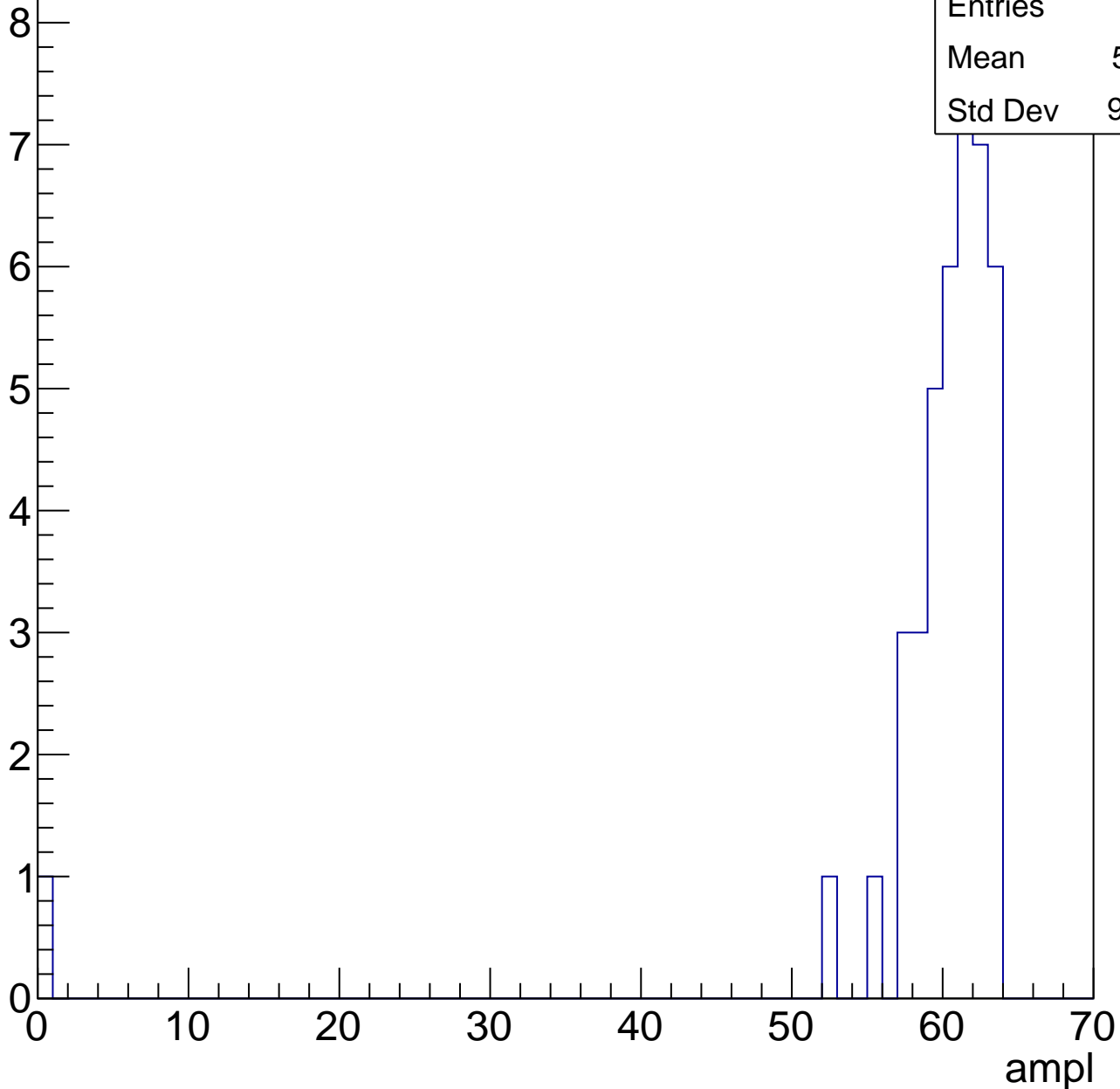


# B1L003S, U11-ch11, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

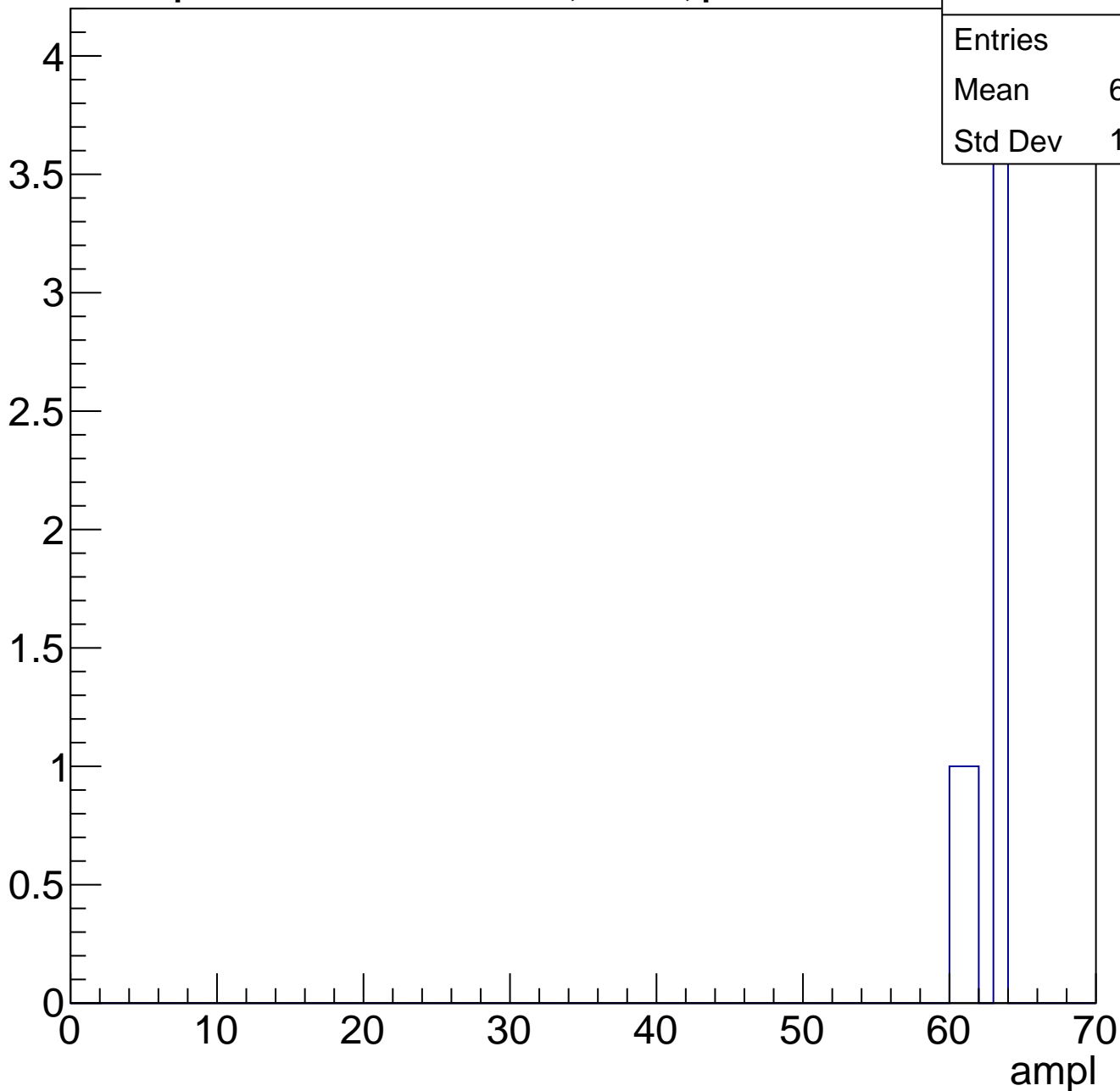
Entries	41
Mean	58.71
Std Dev	9.569



# B1L003S, U11-ch11, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch11, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U11-ch12, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	79
Mean	29.81
Std Dev	3.226

**Gaus mean : 30.5284**

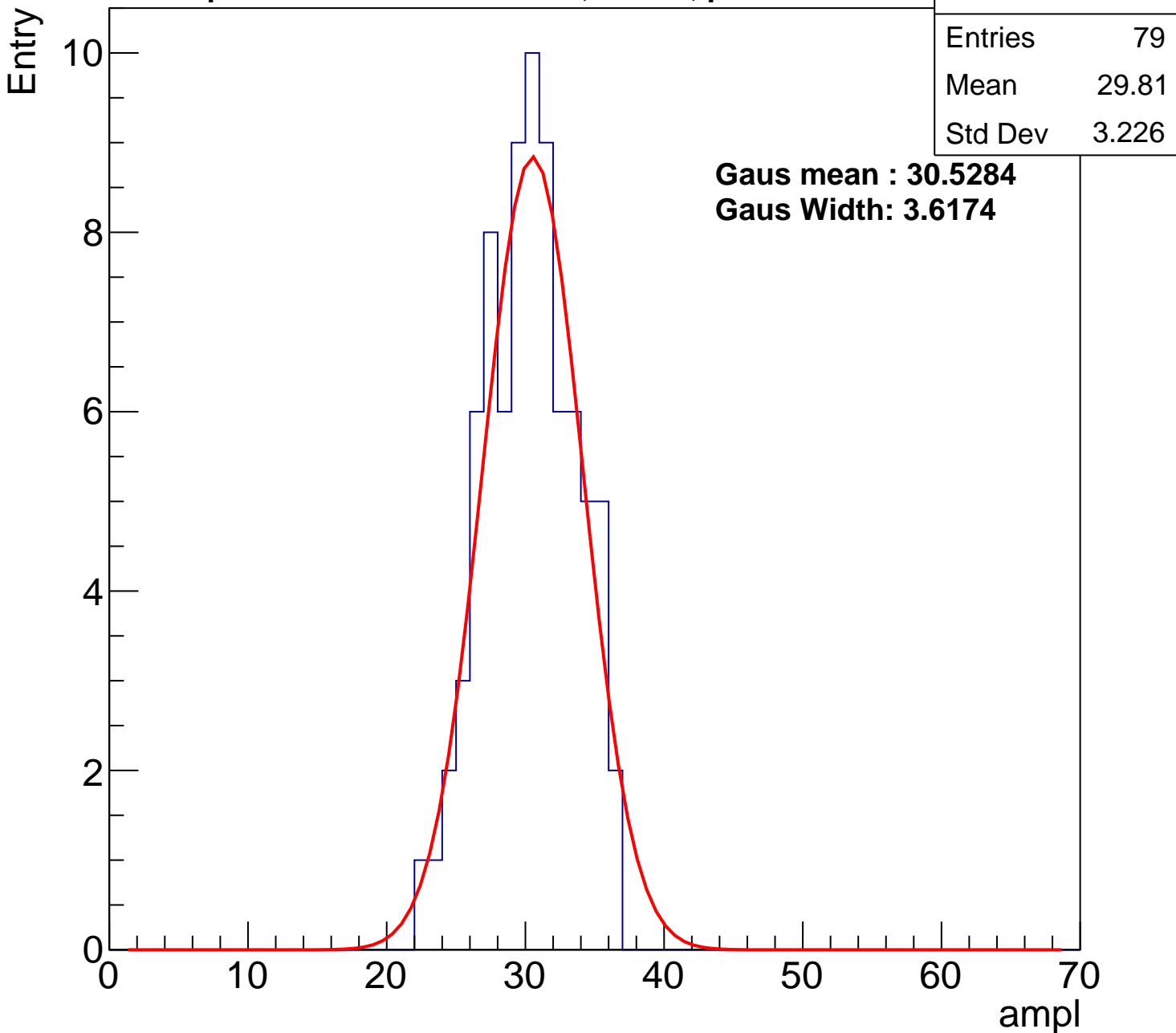
**Gaus Width: 3.6174**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U11-ch12, adc1

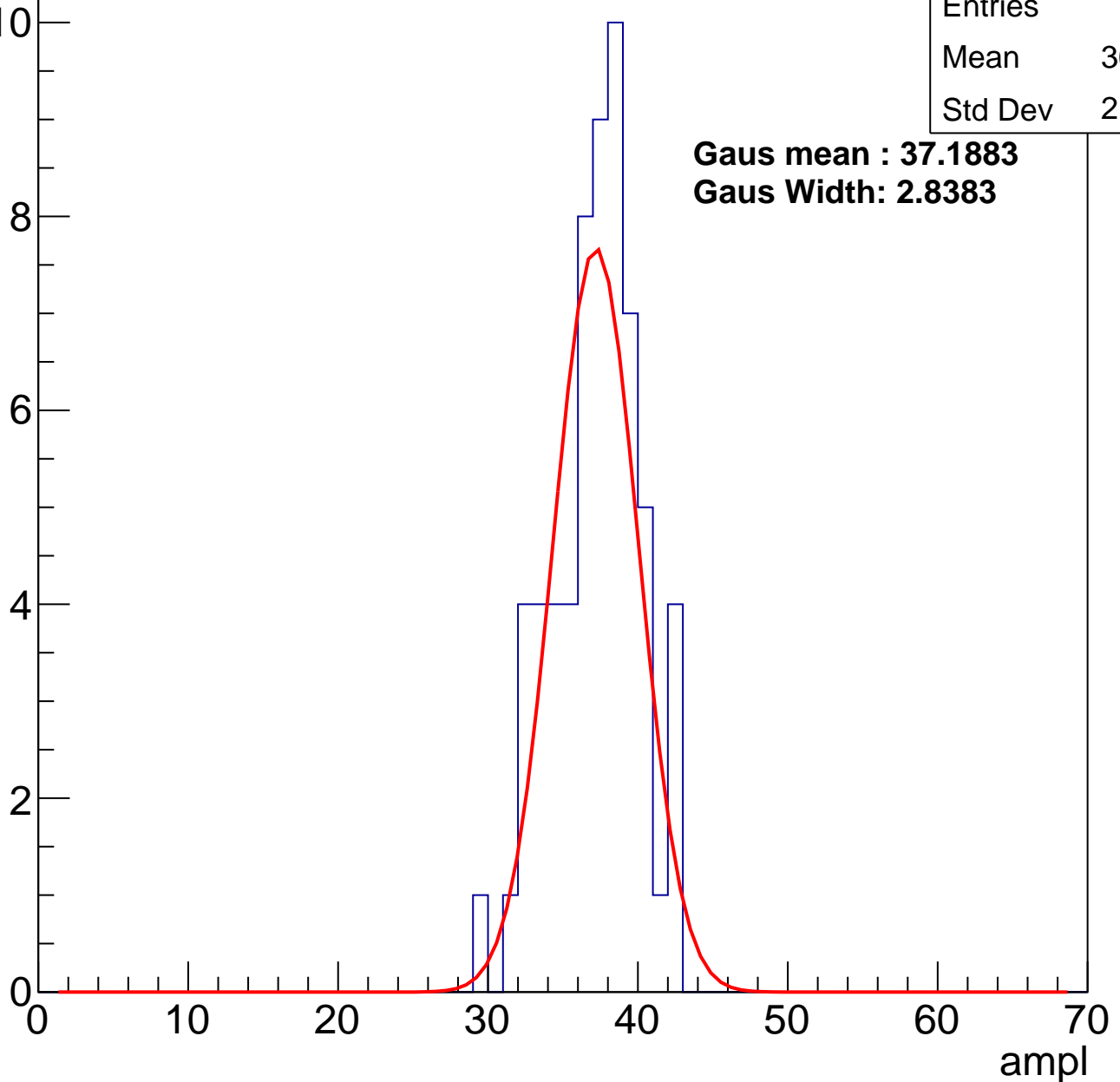
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	36.76
Std Dev	2.894

**Gaus mean : 37.1883**

**Gaus Width: 2.8383**



# B1L003S, U11-ch12, adc2

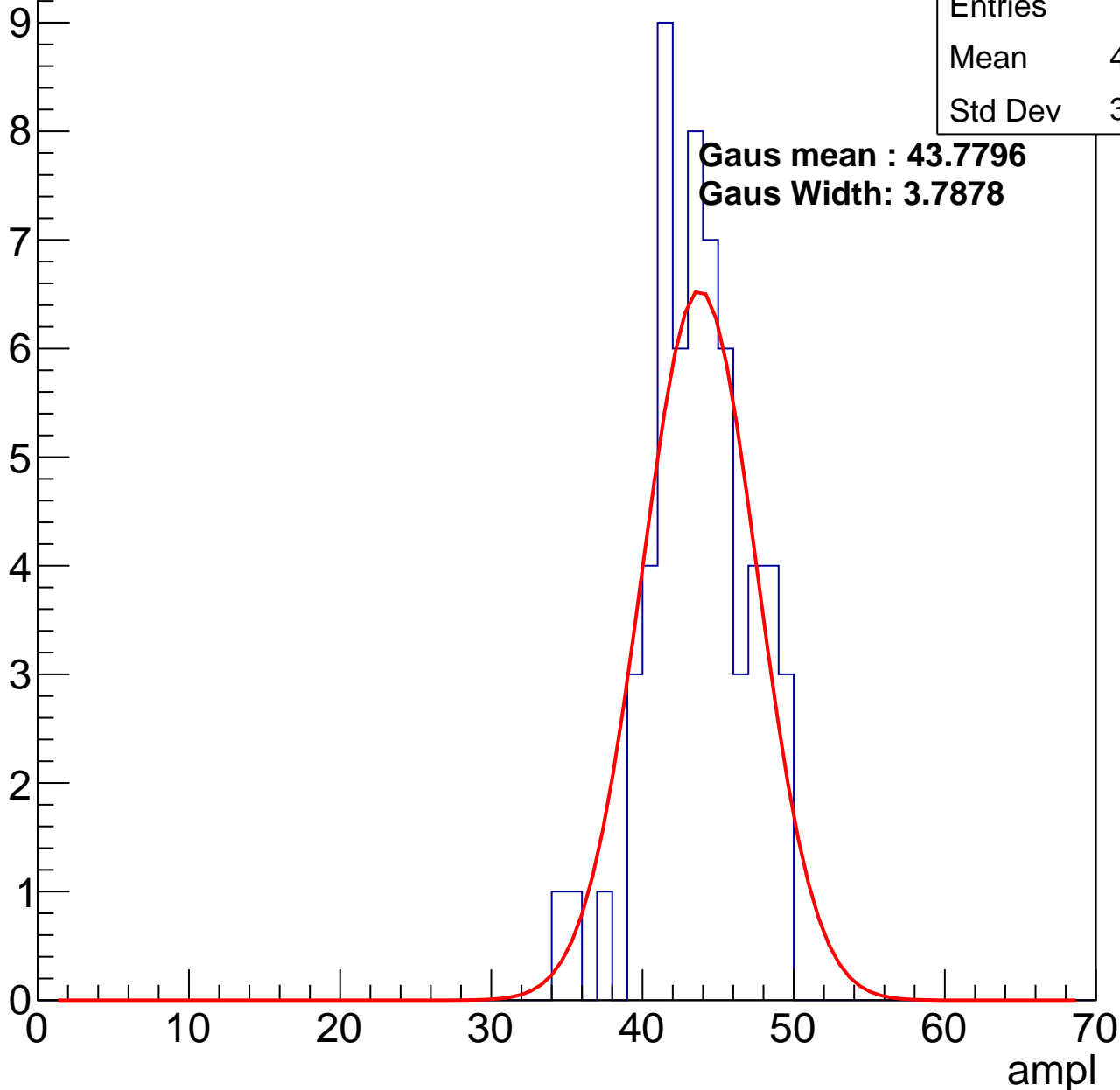
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	43.18
Std Dev	3.253

**Gaus mean : 43.7796**

**Gaus Width: 3.7878**

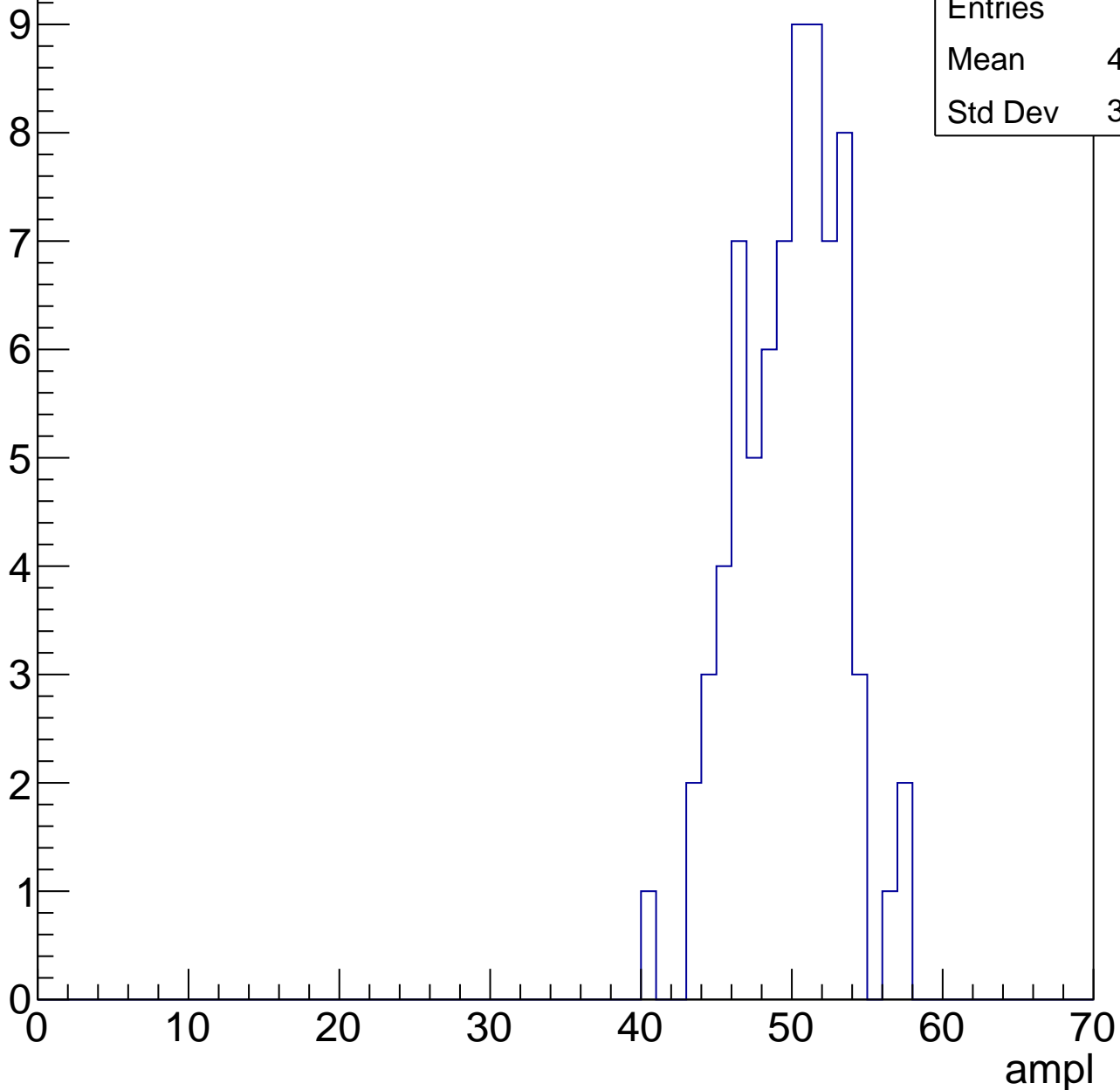


# B1L003S, U11-ch12, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

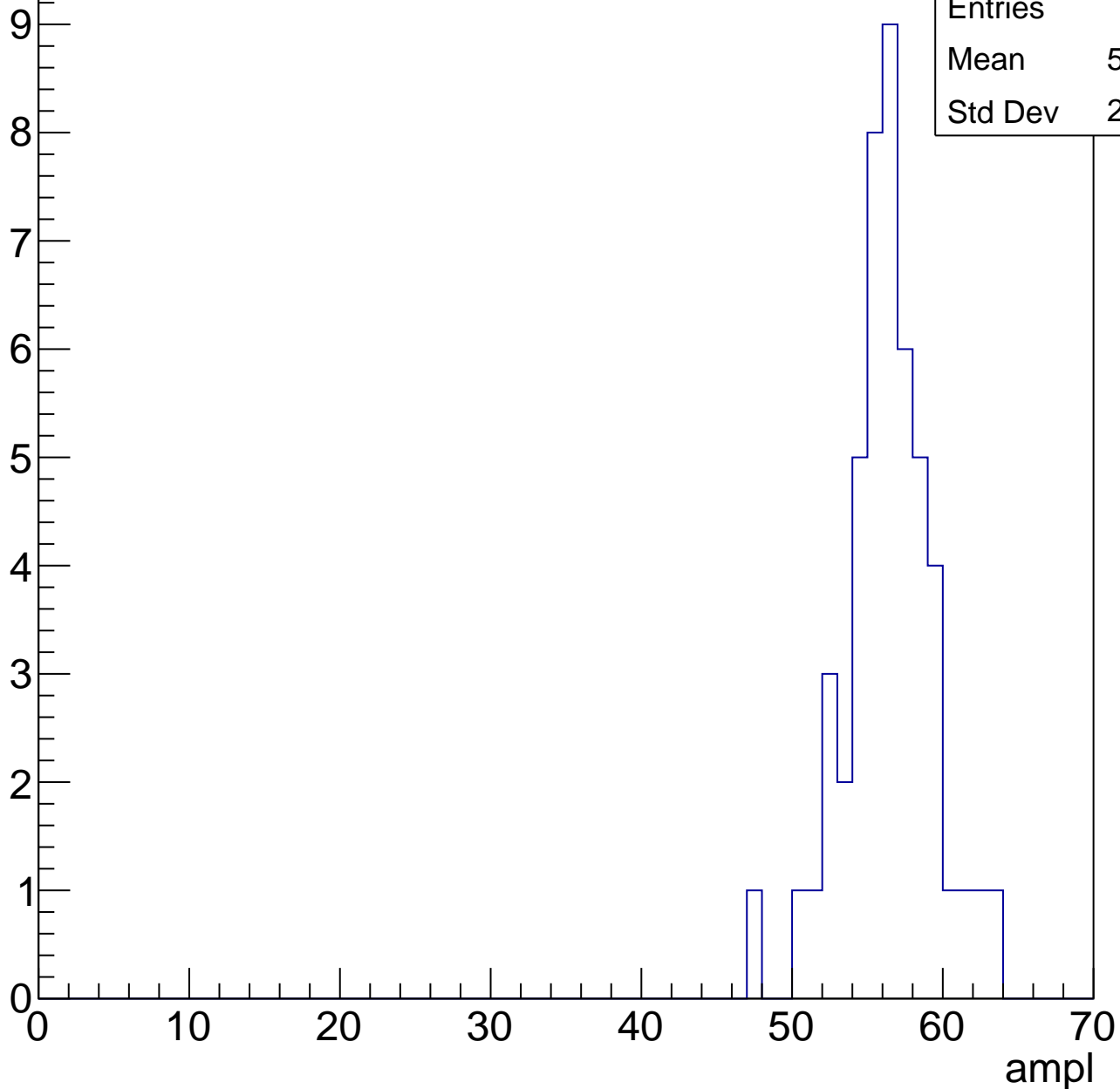
Entries	74
Mean	49.39
Std Dev	3.404



# B1L003S, U11-ch12, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

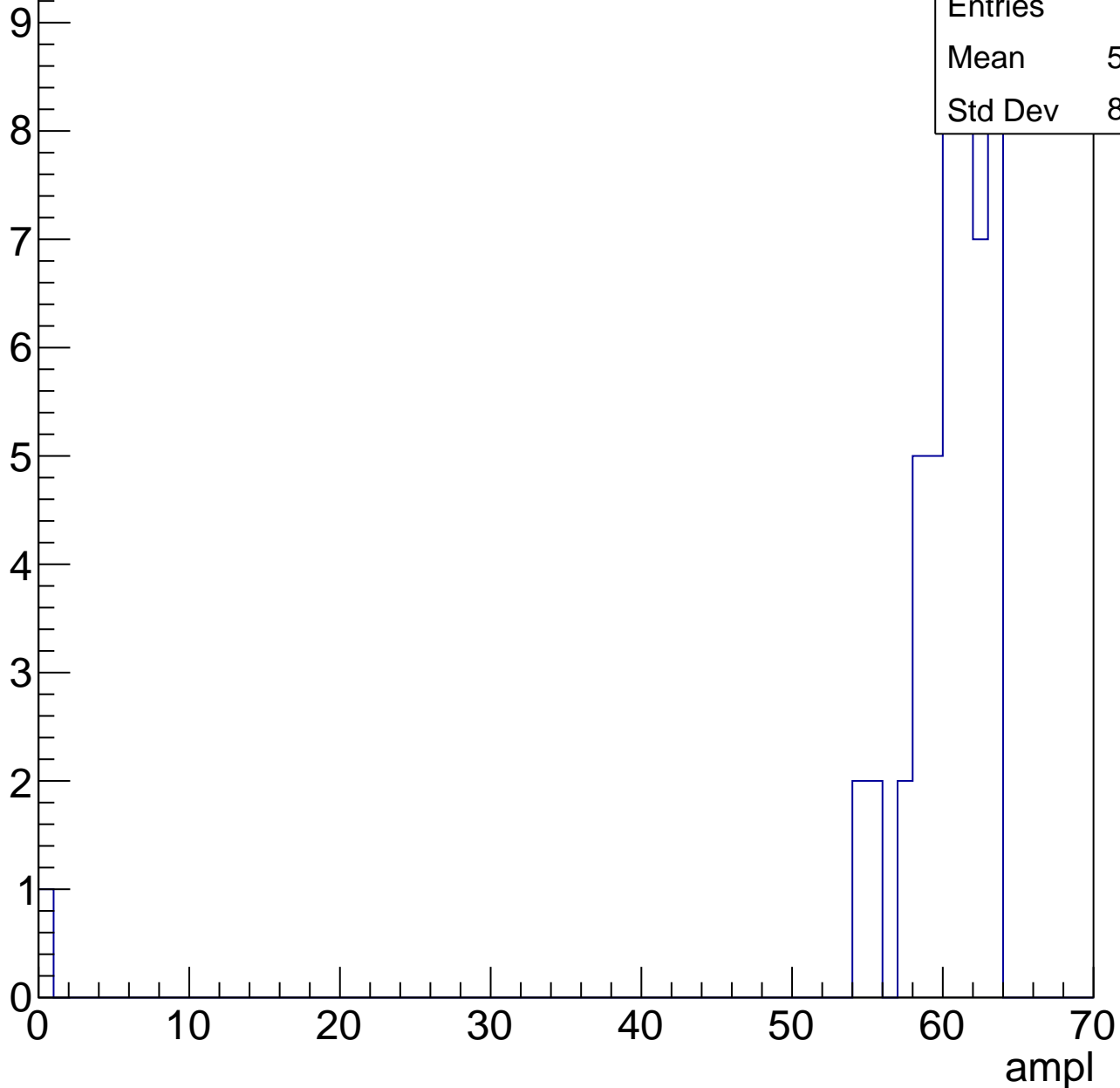
Entry



# B1L003S, U11-ch12, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	49
Mean	58.86
Std Dev	8.818

# B1L003S, U11-ch12, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

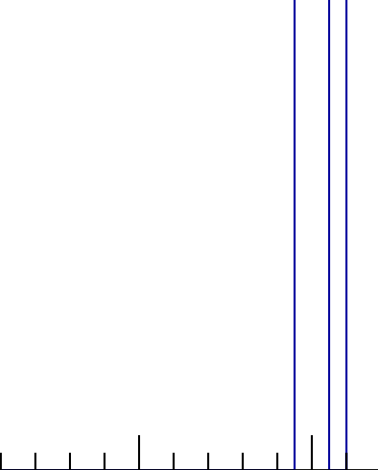
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	61.2
Std Dev	1.47

ampl

0 10 20 30 40 50 60 70





# B1L003S, U11-ch12, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U11-ch13, adc0

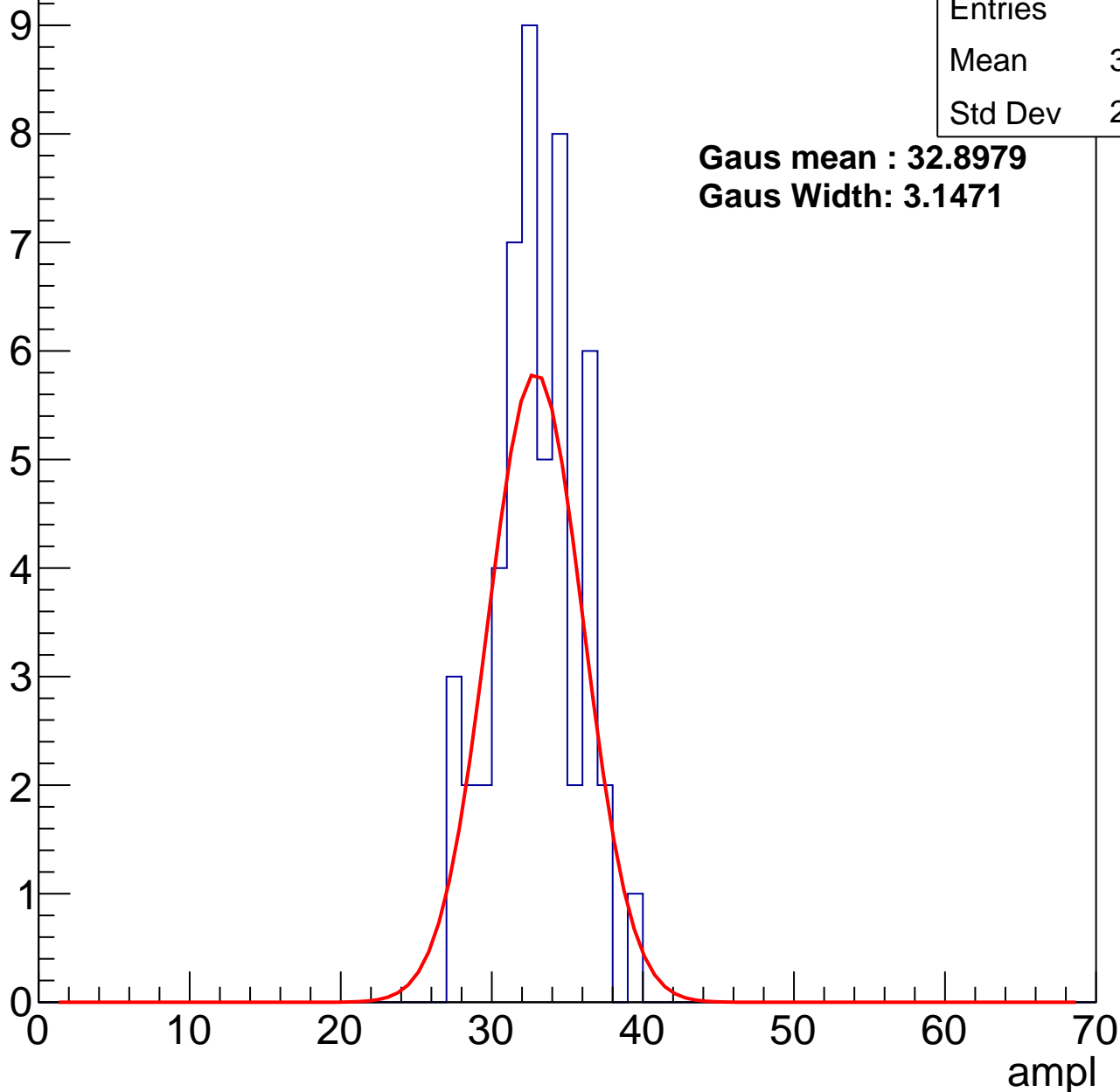
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	51
Mean	32.47
Std Dev	2.754

**Gaus mean : 32.8979**

**Gaus Width: 3.1471**



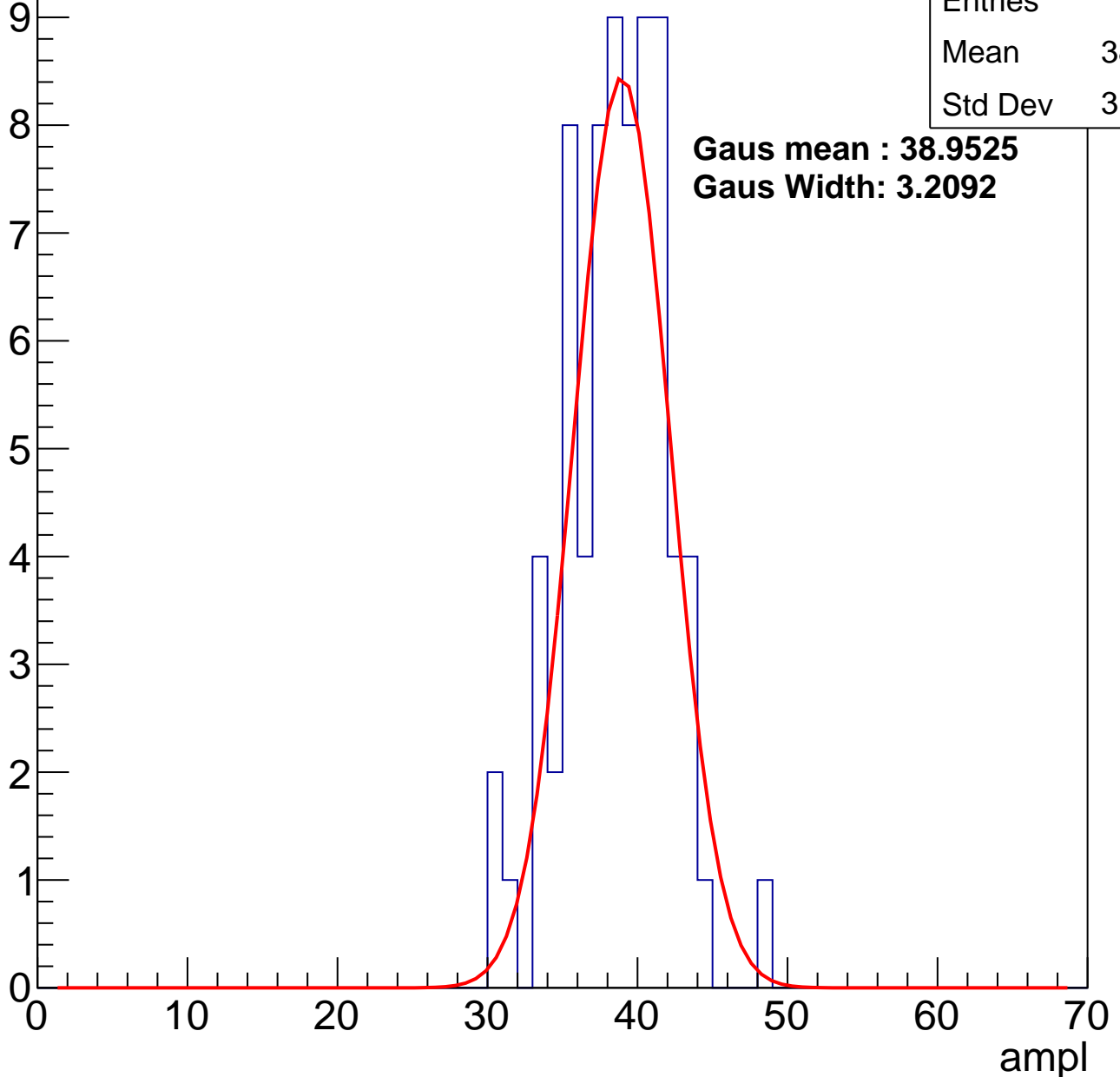
# B1L003S, U11-ch13, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	74
Mean	38.19
Std Dev	3.344

**Gaus mean : 38.9525**  
**Gaus Width: 3.2092**



# B1L003S, U11-ch13, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	72
Mean	45.92
Std Dev	3.144

**Gaus mean : 46.6104**

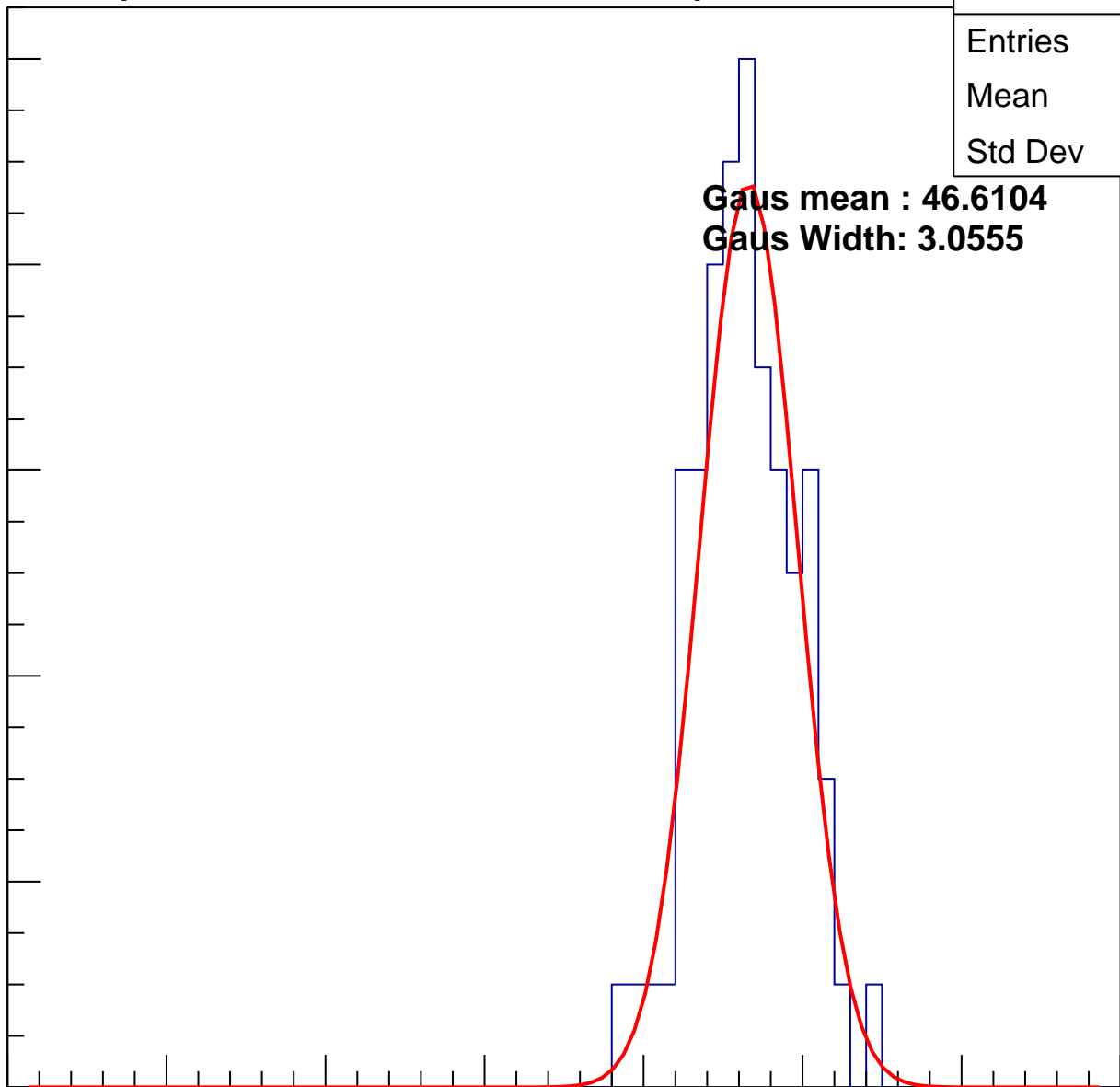
**Gaus Width: 3.0555**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U11-ch13, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

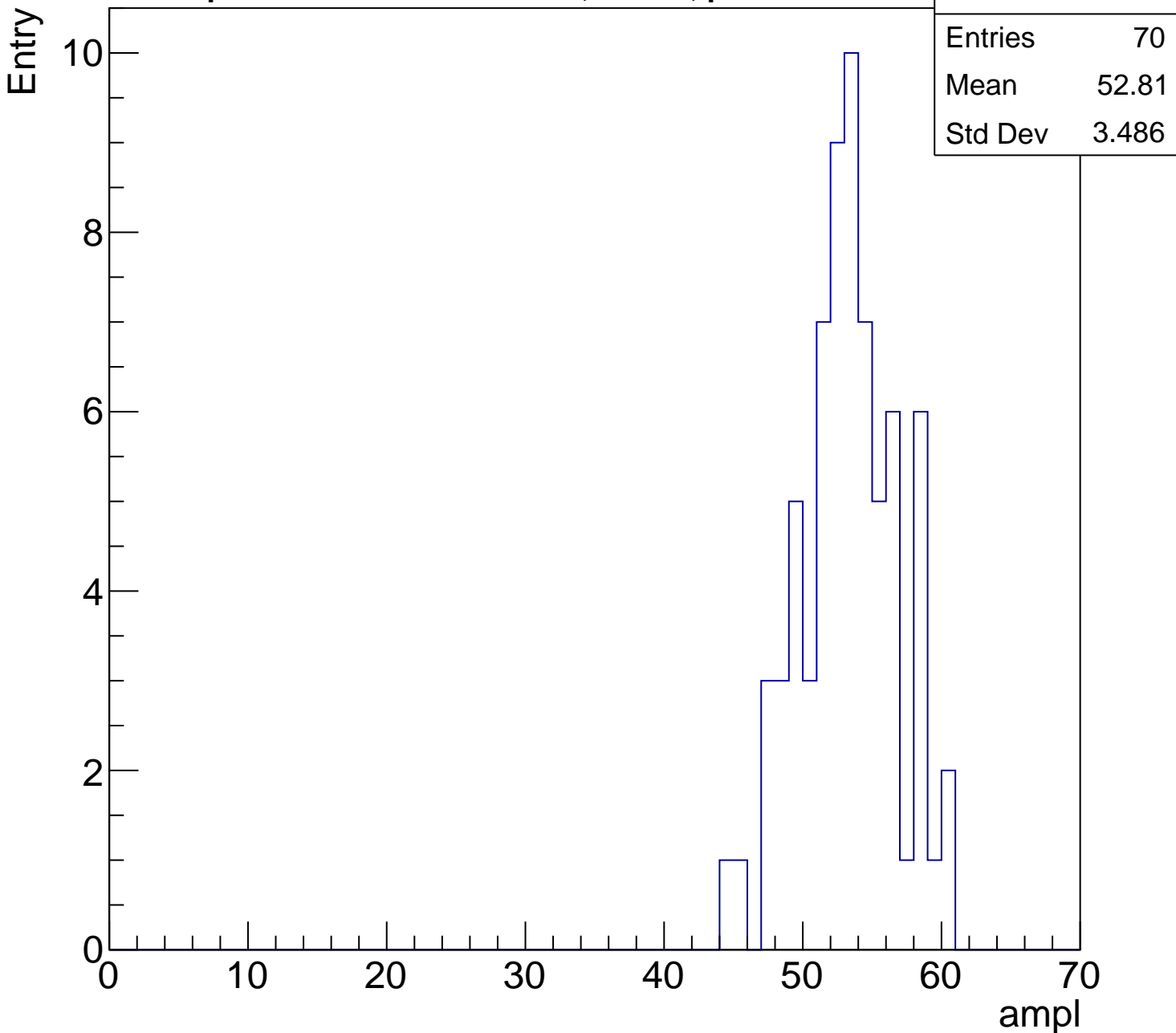
Entries	70
Mean	52.81
Std Dev	3.486

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

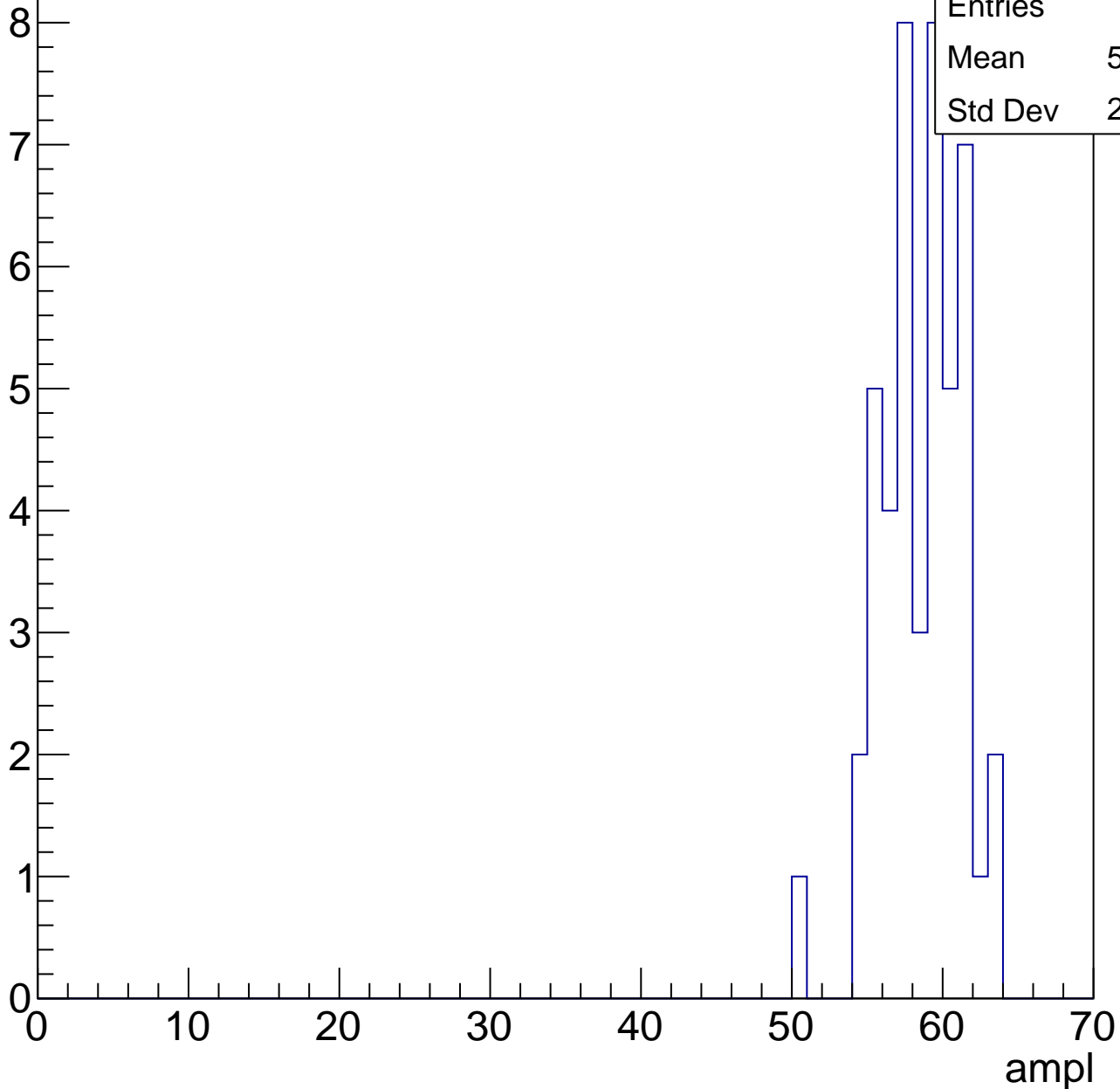


# B1L003S, U11-ch13, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	46
Mean	58.13
Std Dev	2.643

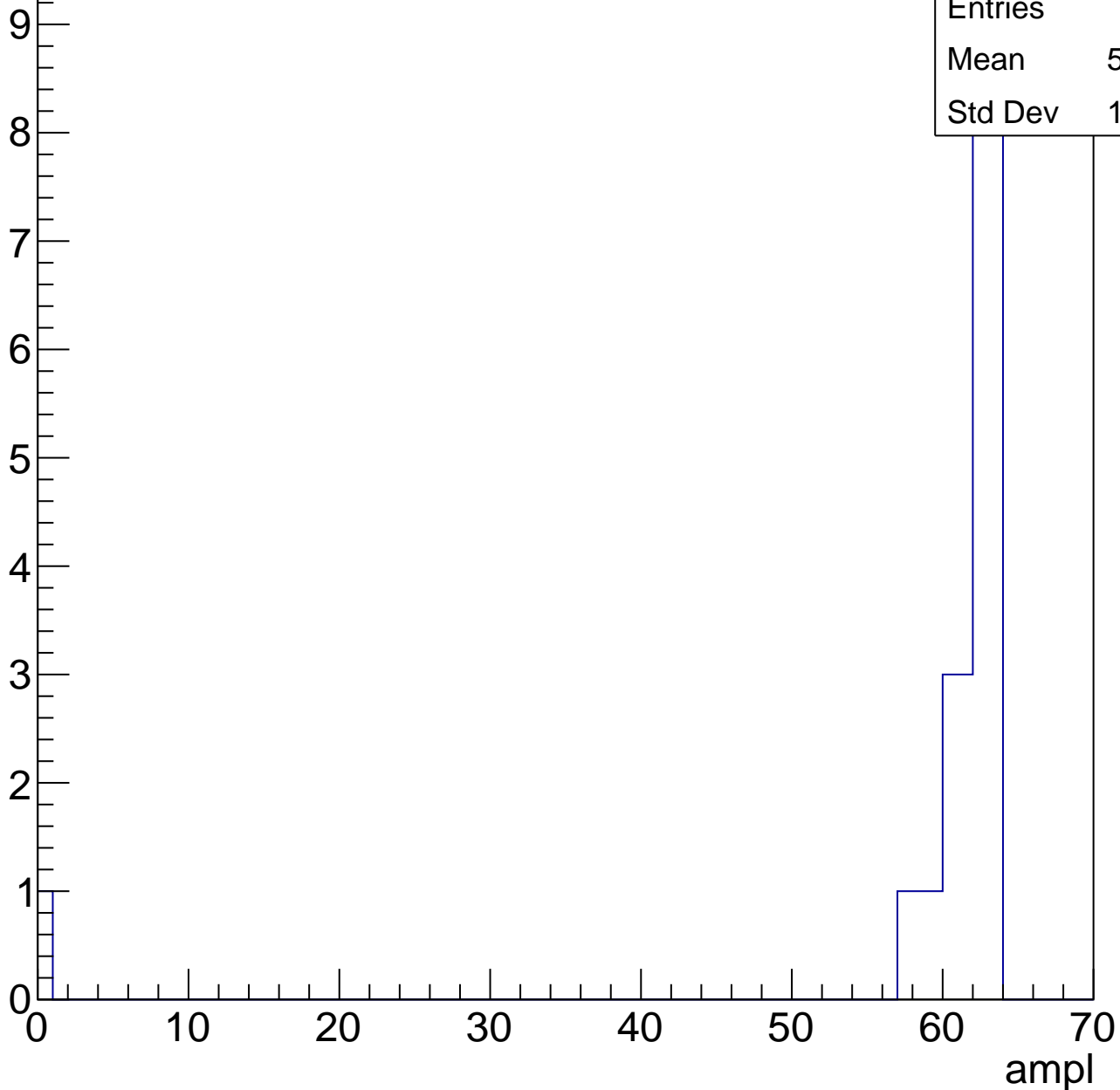


# B1L003S, U11-ch13, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	27
Mean	59.22
Std Dev	11.72



# B1L003S, U11-ch13, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L003S, U11-ch13, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U11-ch14, adc0

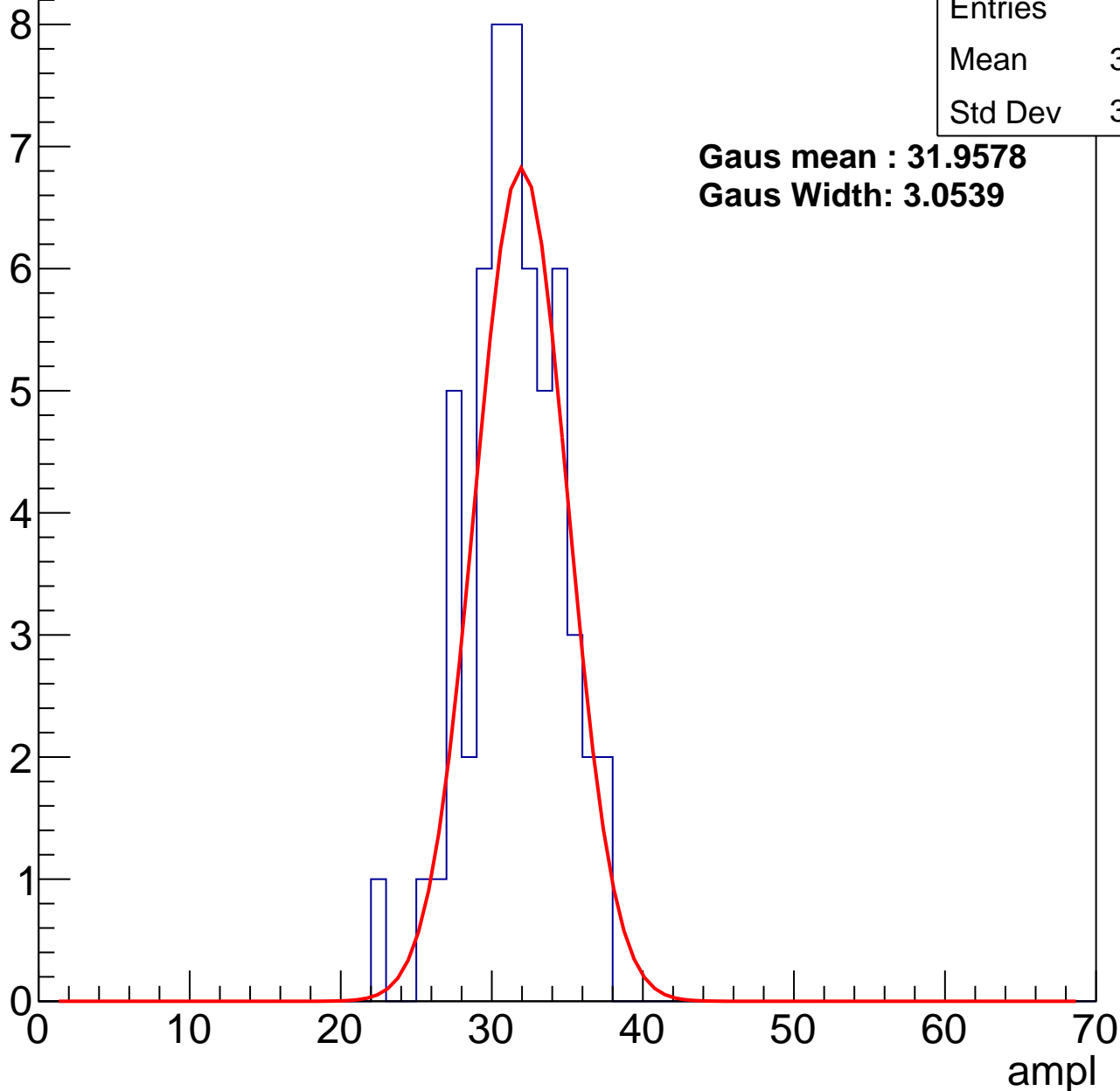
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	31.04
Std Dev	3.053

**Gaus mean : 31.9578**

**Gaus Width: 3.0539**



# B1L003S, U11-ch14, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	63
Mean	36.92
Std Dev	3.391

**Gaus mean : 37.2292**

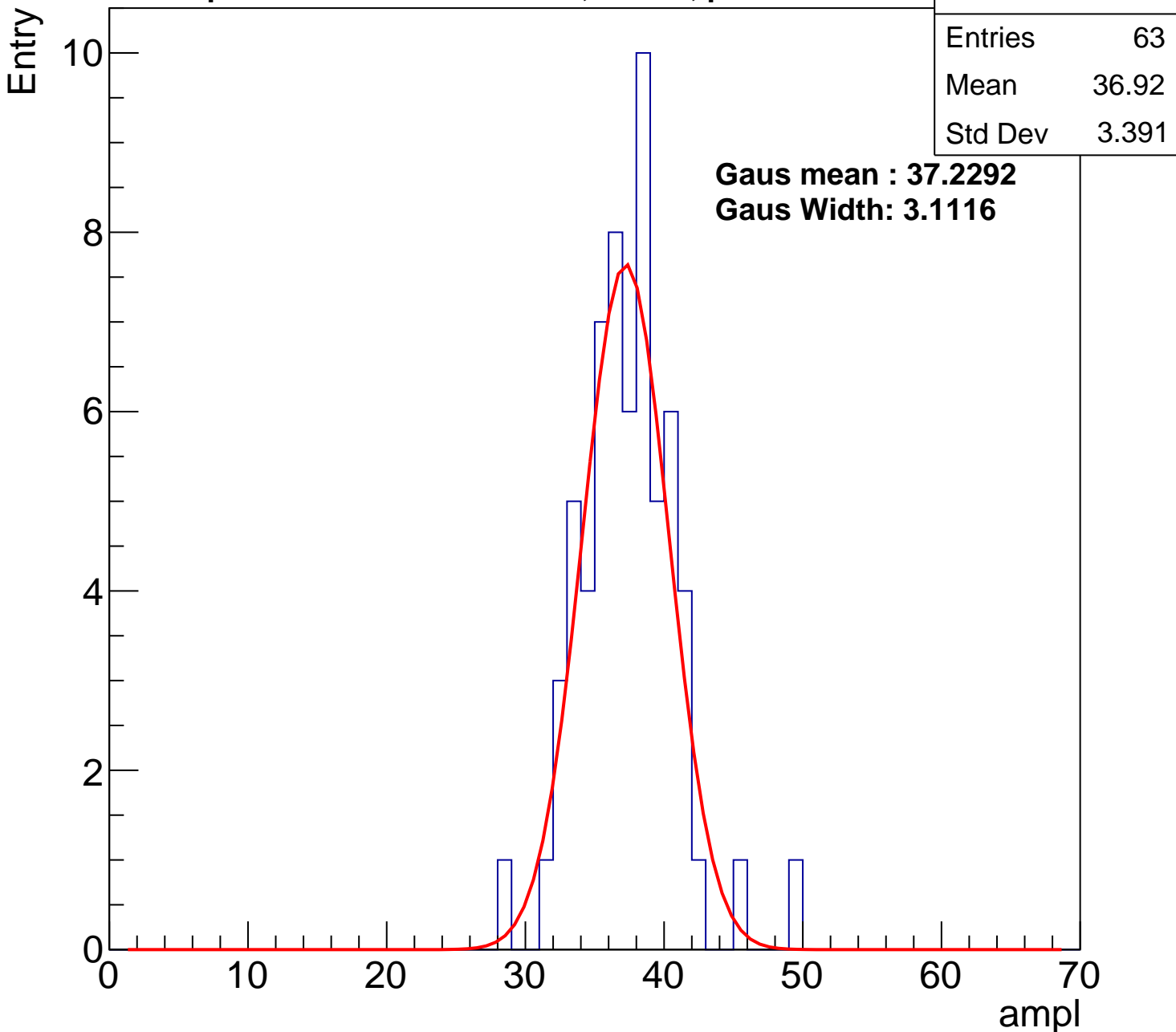
**Gaus Width: 3.1116**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L003S, U11-ch14, adc2

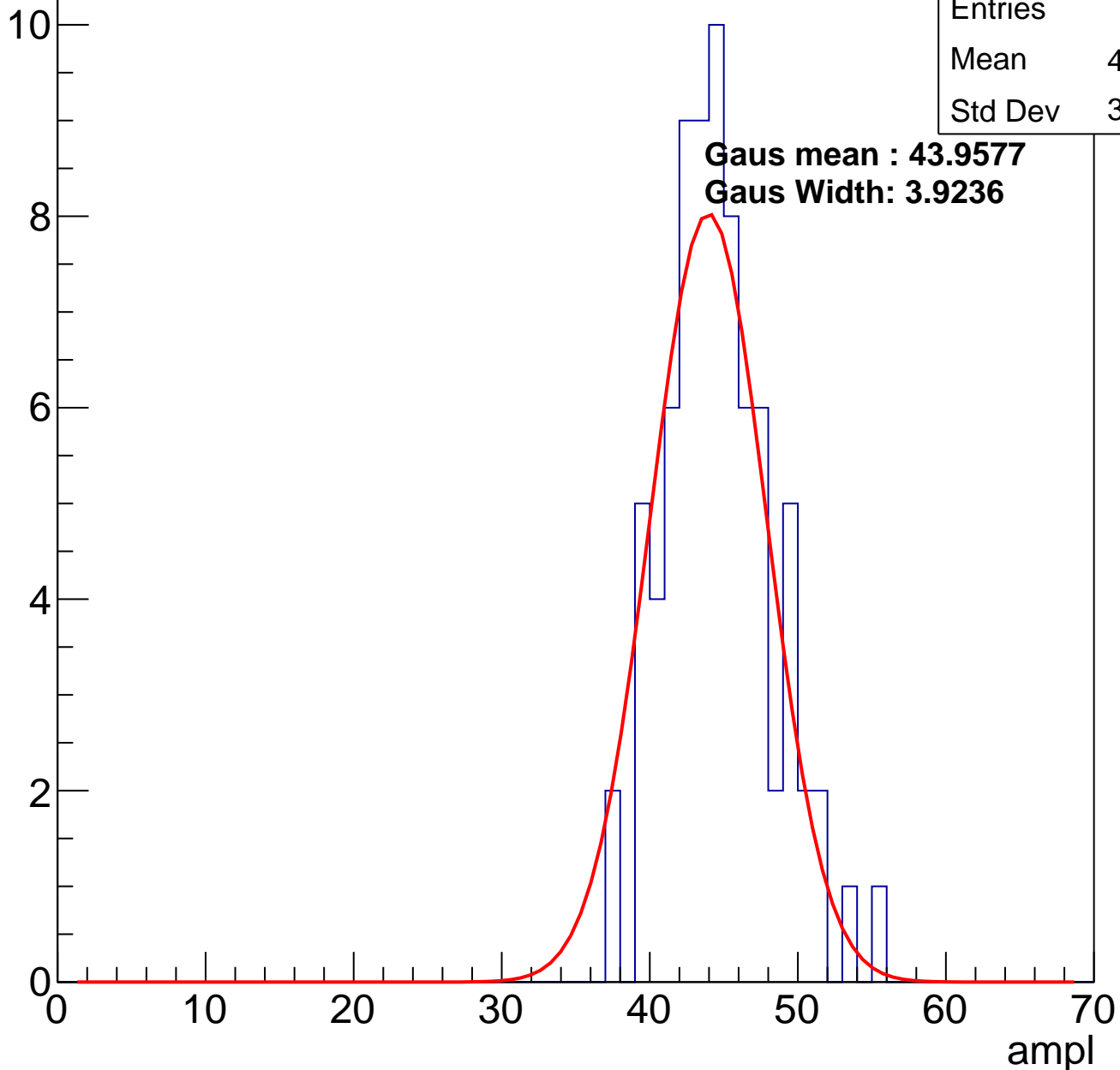
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	78
Mean	44.22
Std Dev	3.576

**Gaus mean : 43.9577**

**Gaus Width: 3.9236**

Entry

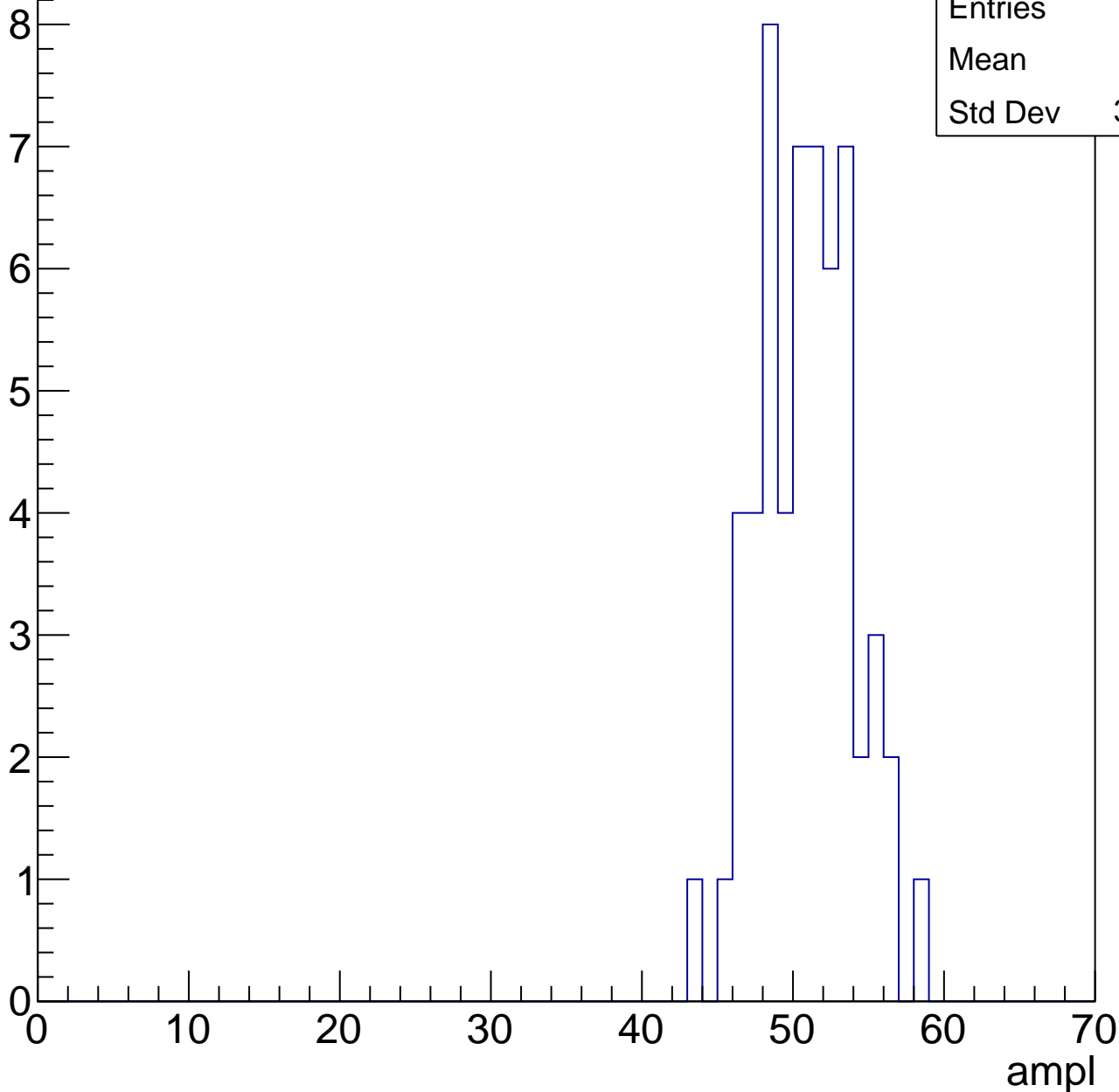


# B1L003S, U11-ch14, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	50.4
Std Dev	3.071

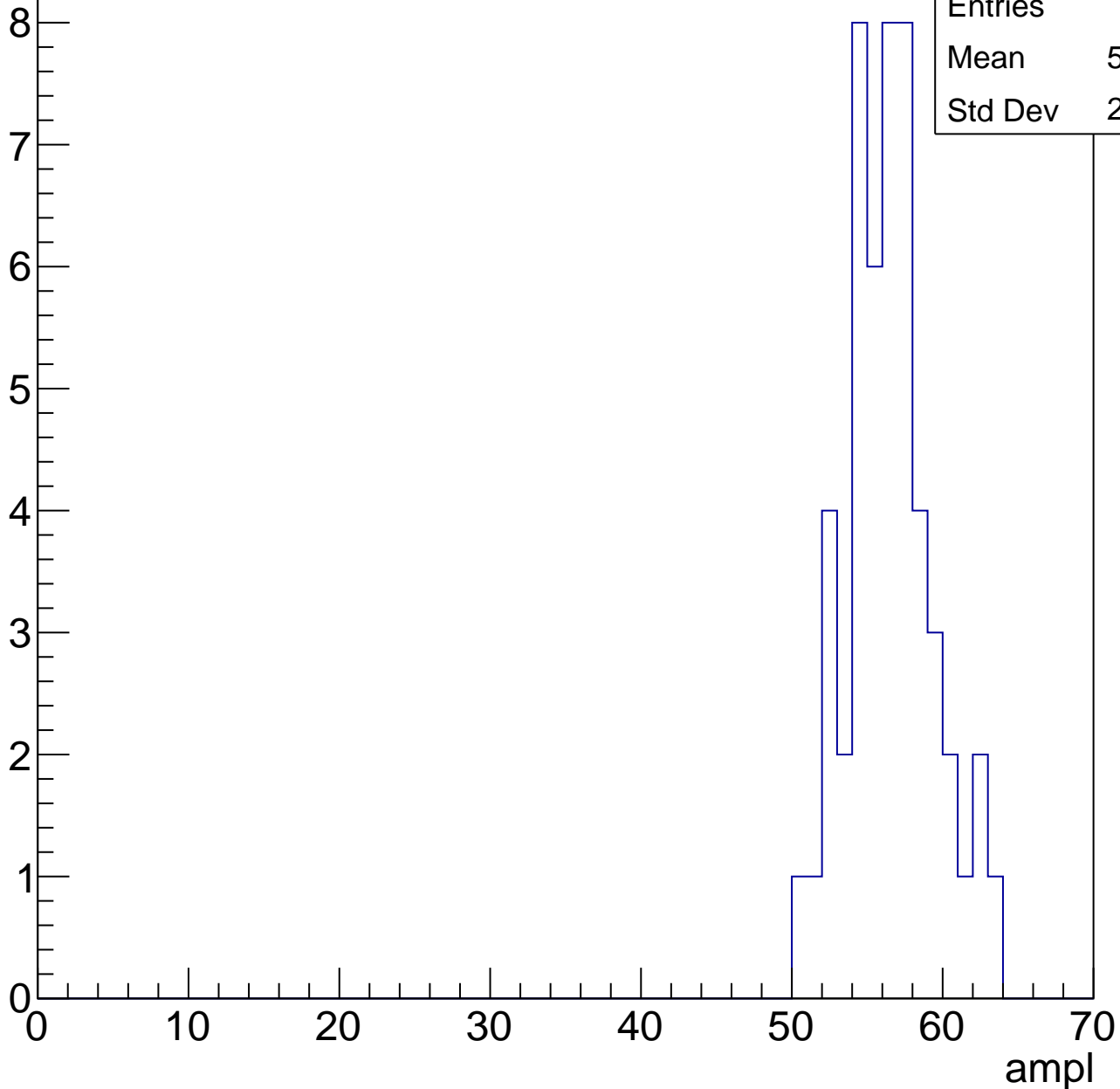


# B1L003S, U11-ch14, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	51
Mean	56.04
Std Dev	2.835

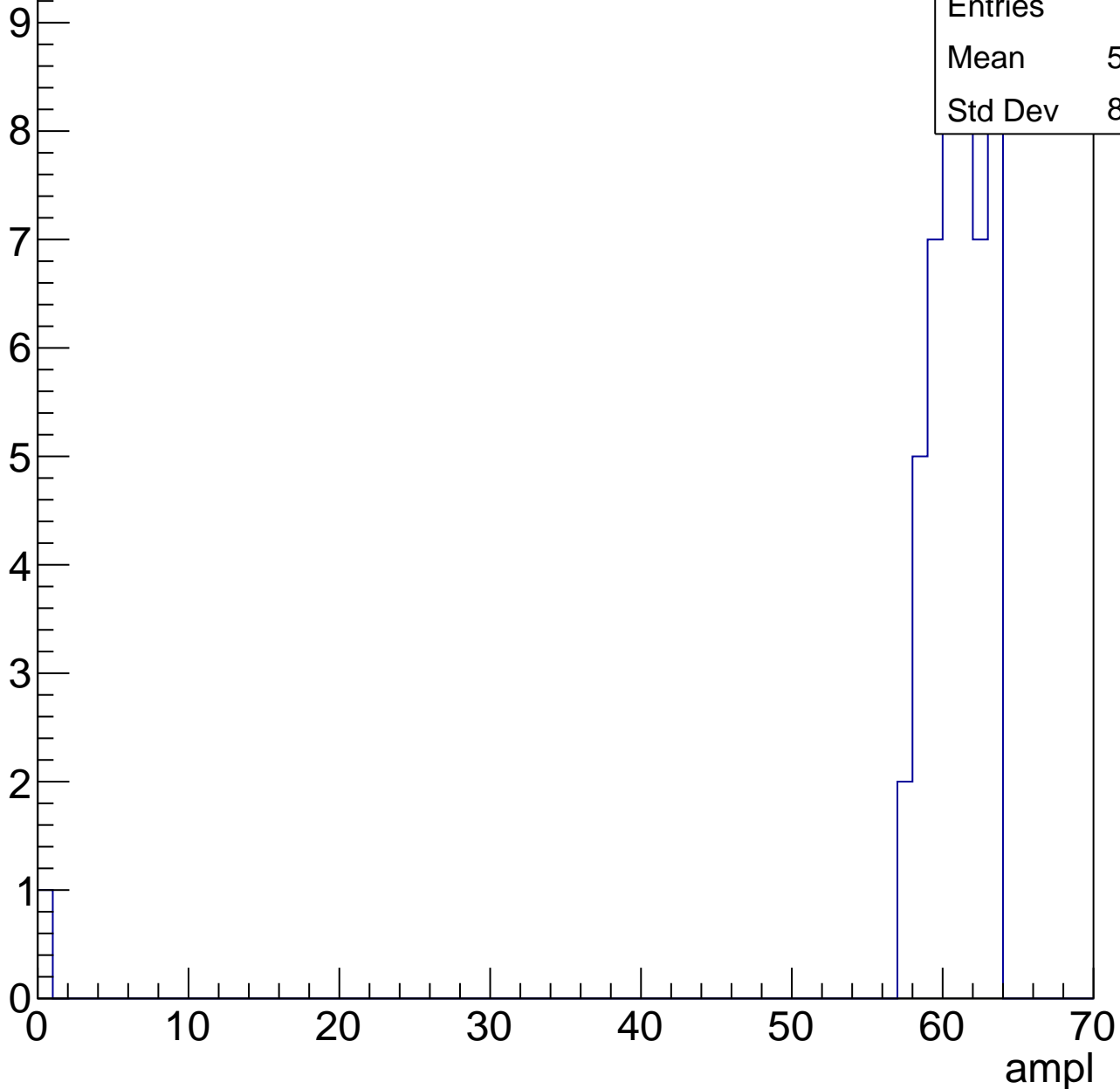


# B1L003S, U11-ch14, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	47
Mean	59.23
Std Dev	8.904



# B1L003S, U11-ch14, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch14, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U11-ch15, adc0

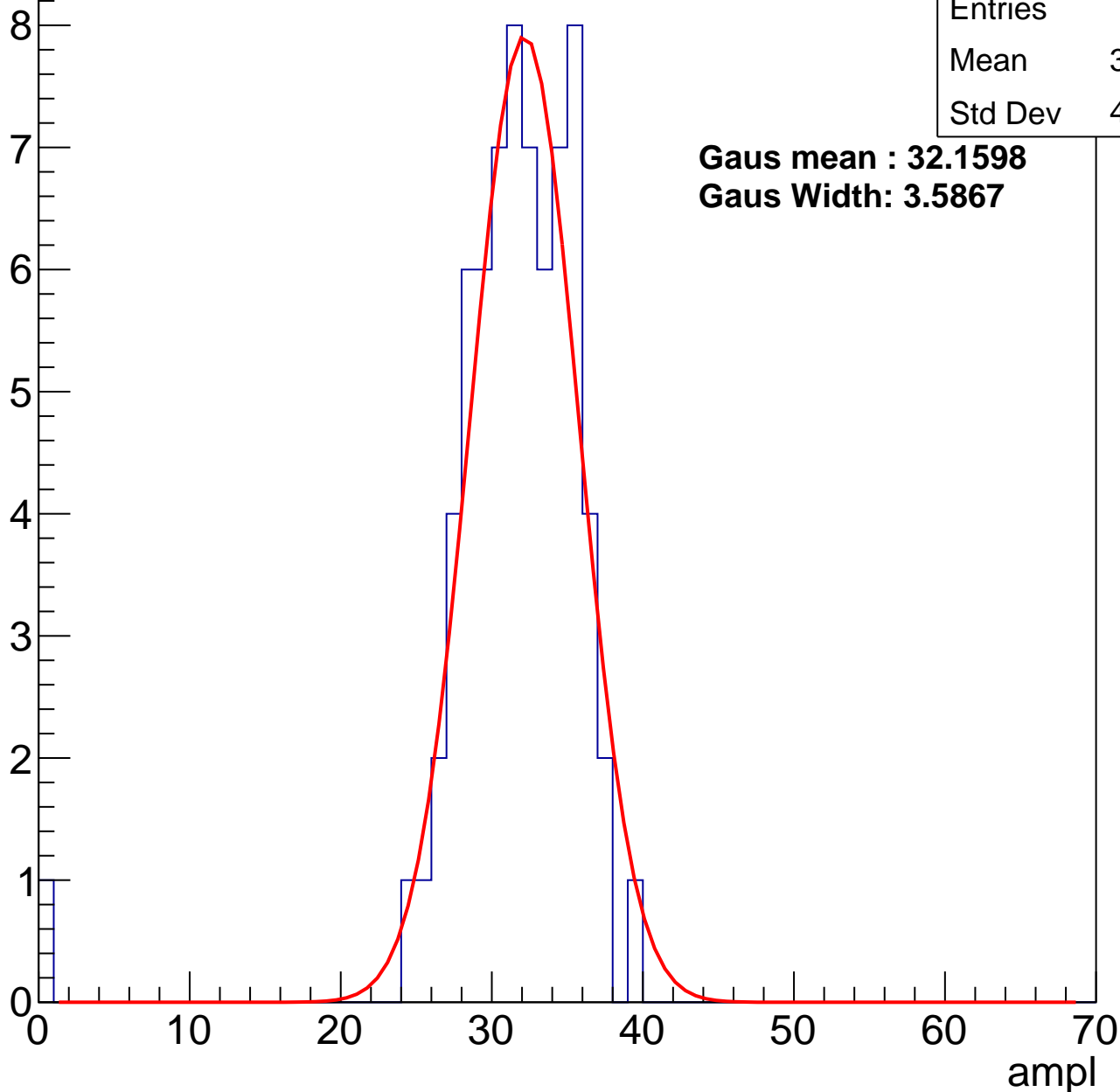
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	71
Mean	31.07
Std Dev	4.897

**Gaus mean : 32.1598**

**Gaus Width: 3.5867**



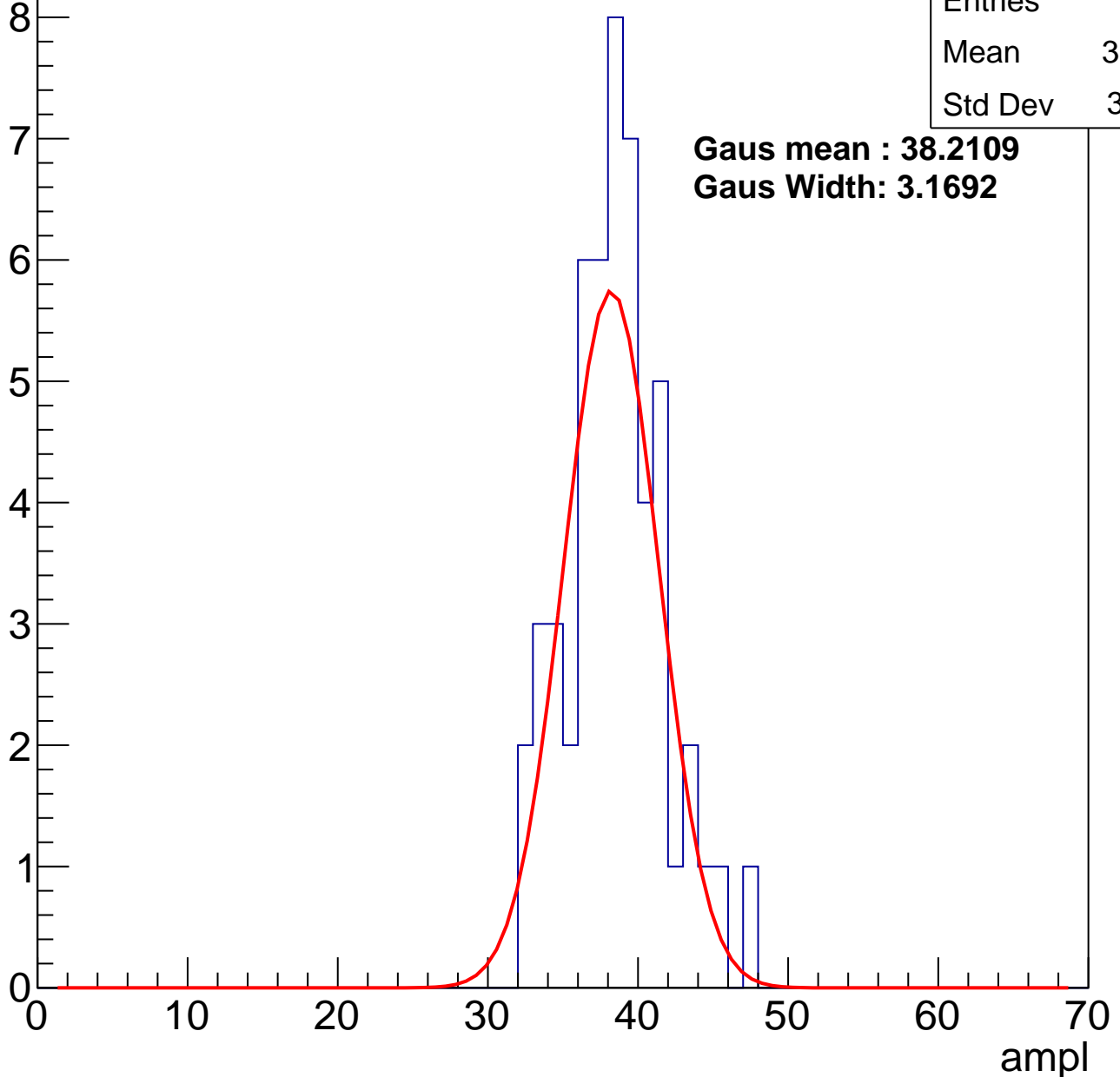
# B1L003S, U11-ch15, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	52
Mean	38.06
Std Dev	3.231

**Gaus mean : 38.2109**  
**Gaus Width: 3.1692**



# B1L003S, U11-ch15, adc2

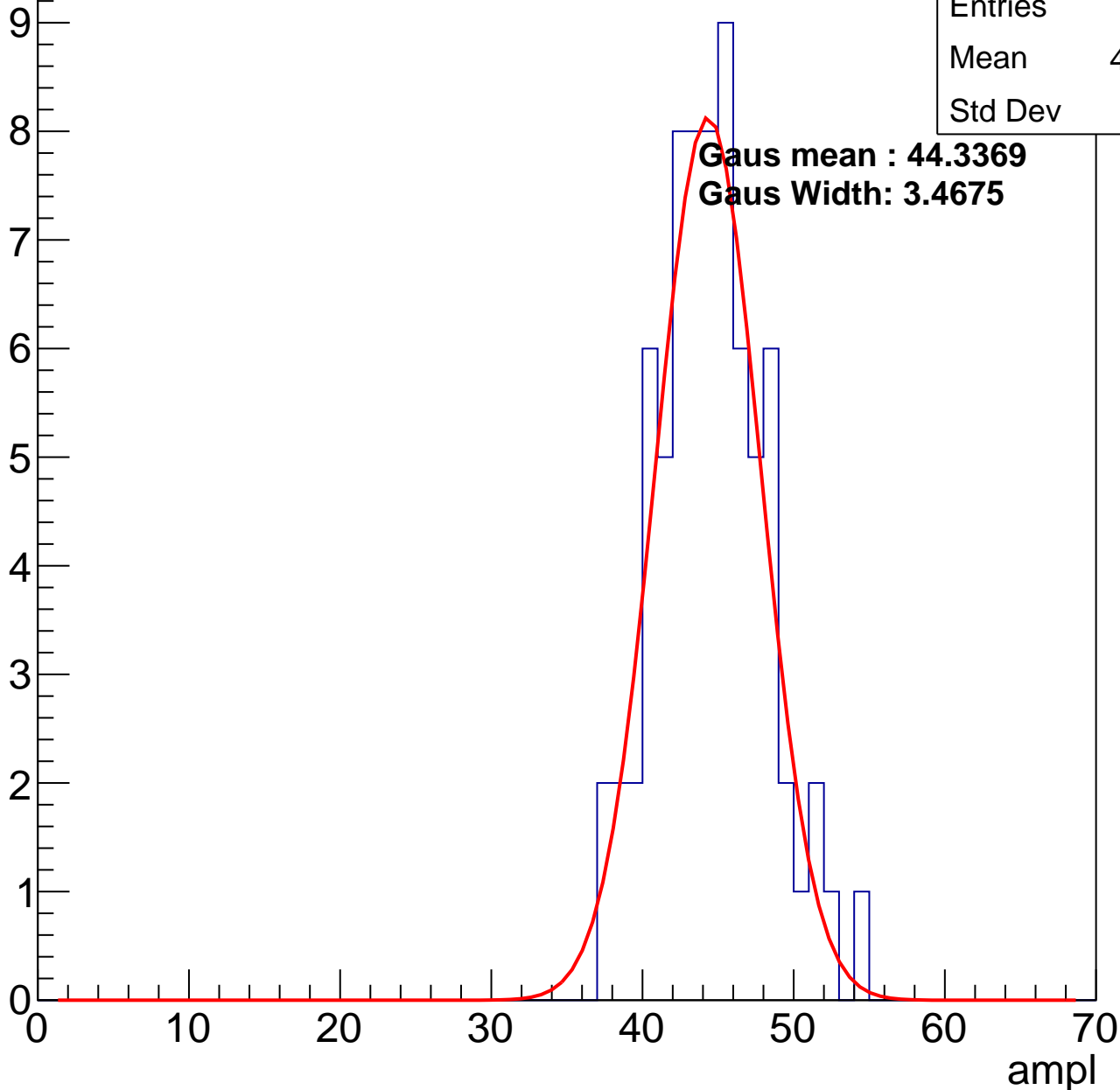
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	74
Mean	44.12
Std Dev	3.53

**Gaus mean : 44.3369**

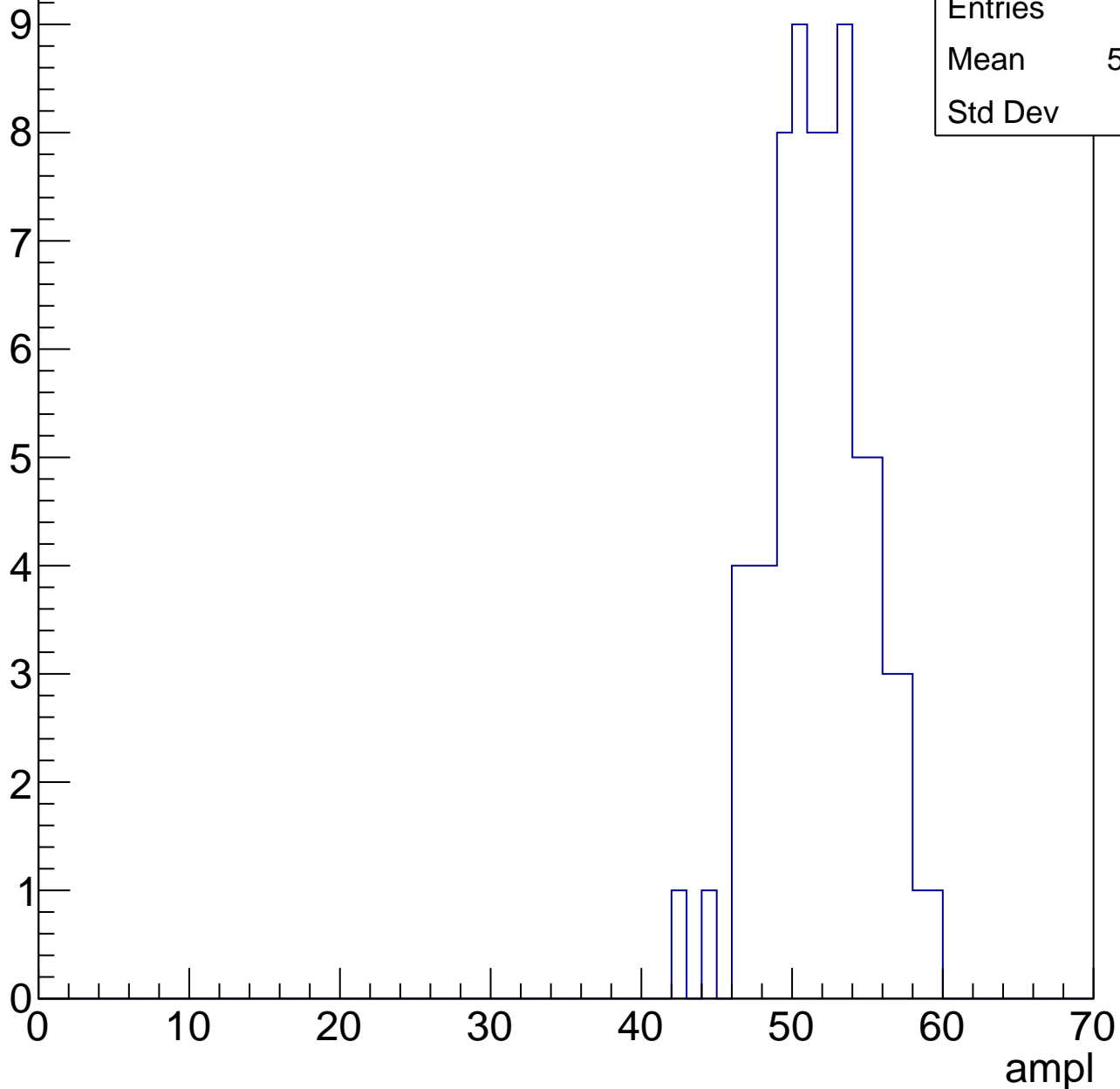
**Gaus Width: 3.4675**



# B1L003S, U11-ch15, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	74
Mean	51.27
Std Dev	3.35

# B1L003S, U11-ch15, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

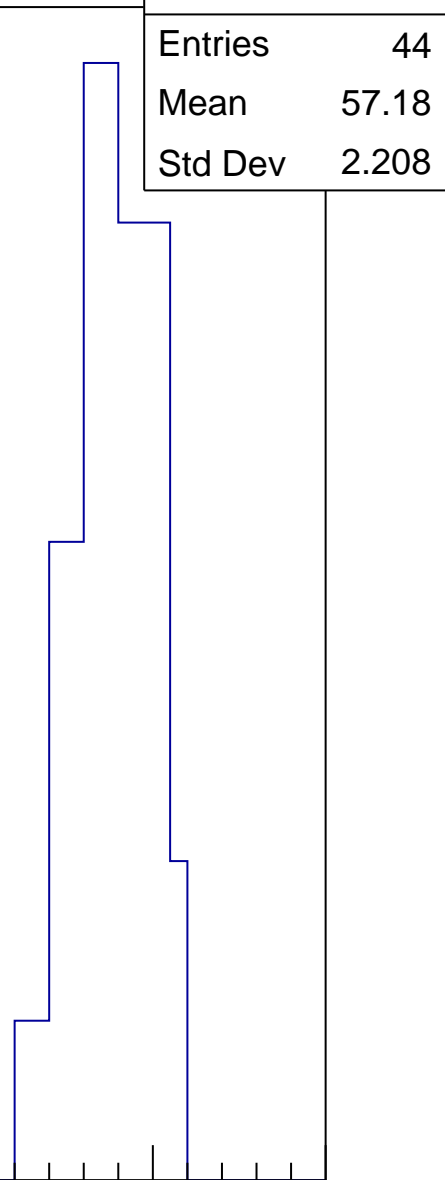
Entry

7  
6  
5  
4  
3  
2  
1  
0

Entries	44
Mean	57.18
Std Dev	2.208

ampl

0 10 20 30 40 50 60 70



# B1L003S, U11-ch15, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	39
Mean	59.54
Std Dev	9.826

Entry

10

8

6

4

2

0

0

10

20

30

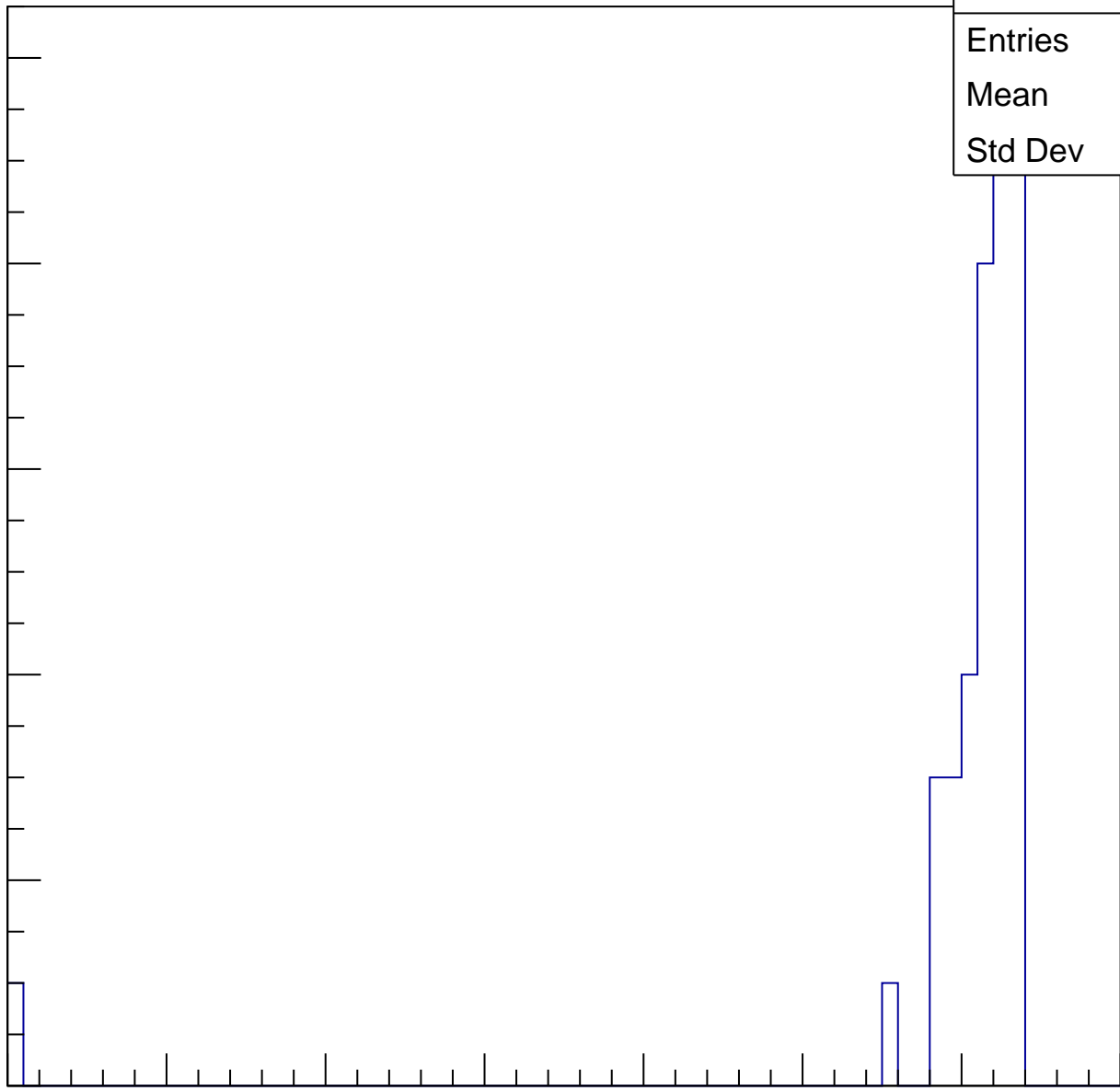
40

50

60

70

ampl



# B1L003S, U11-ch15, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	62
Std Dev	0



# B1L003S, U11-ch15, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U11-ch16, adc0

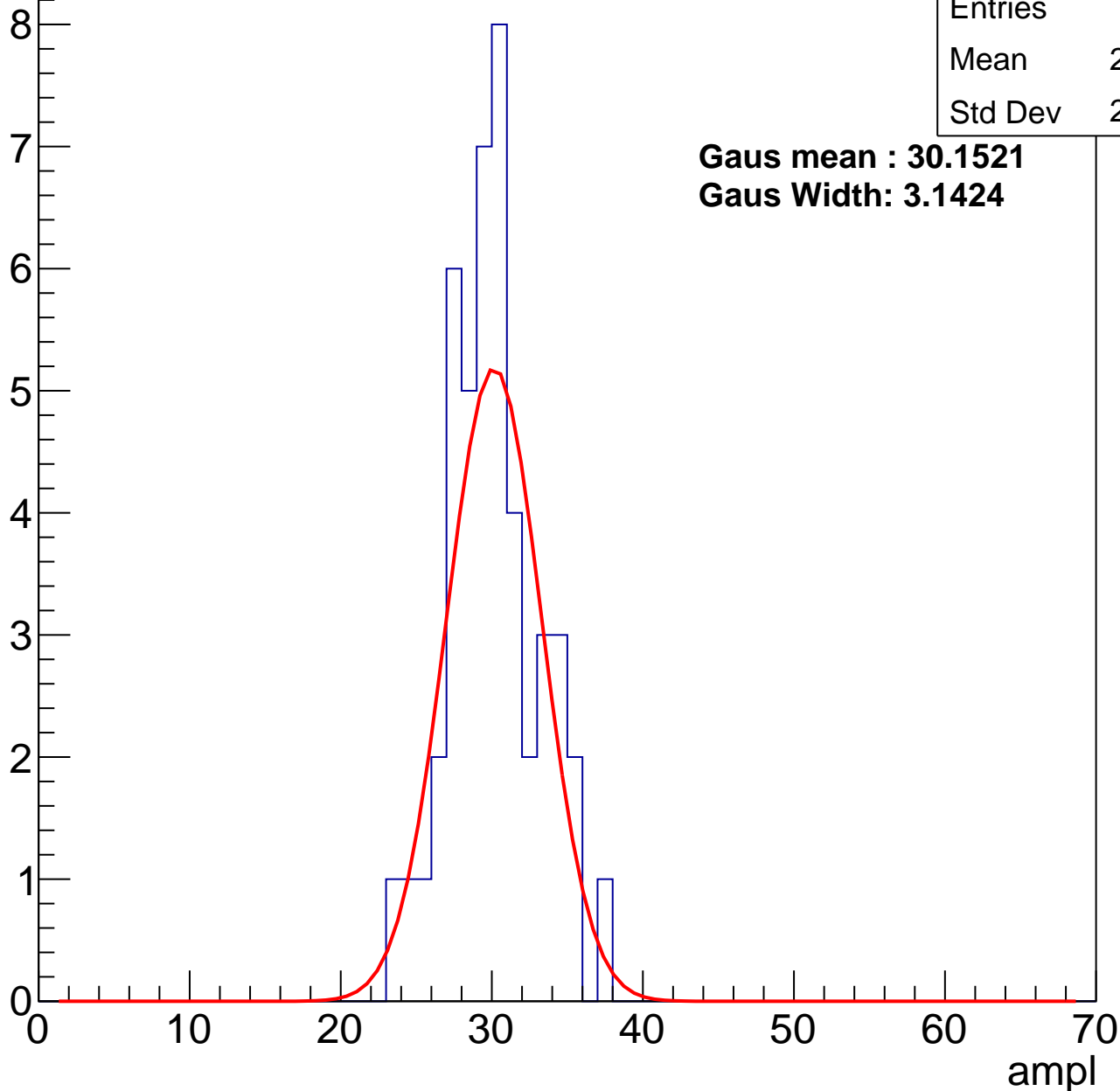
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	46
Mean	29.67
Std Dev	2.964

**Gaus mean : 30.1521**

**Gaus Width: 3.1424**



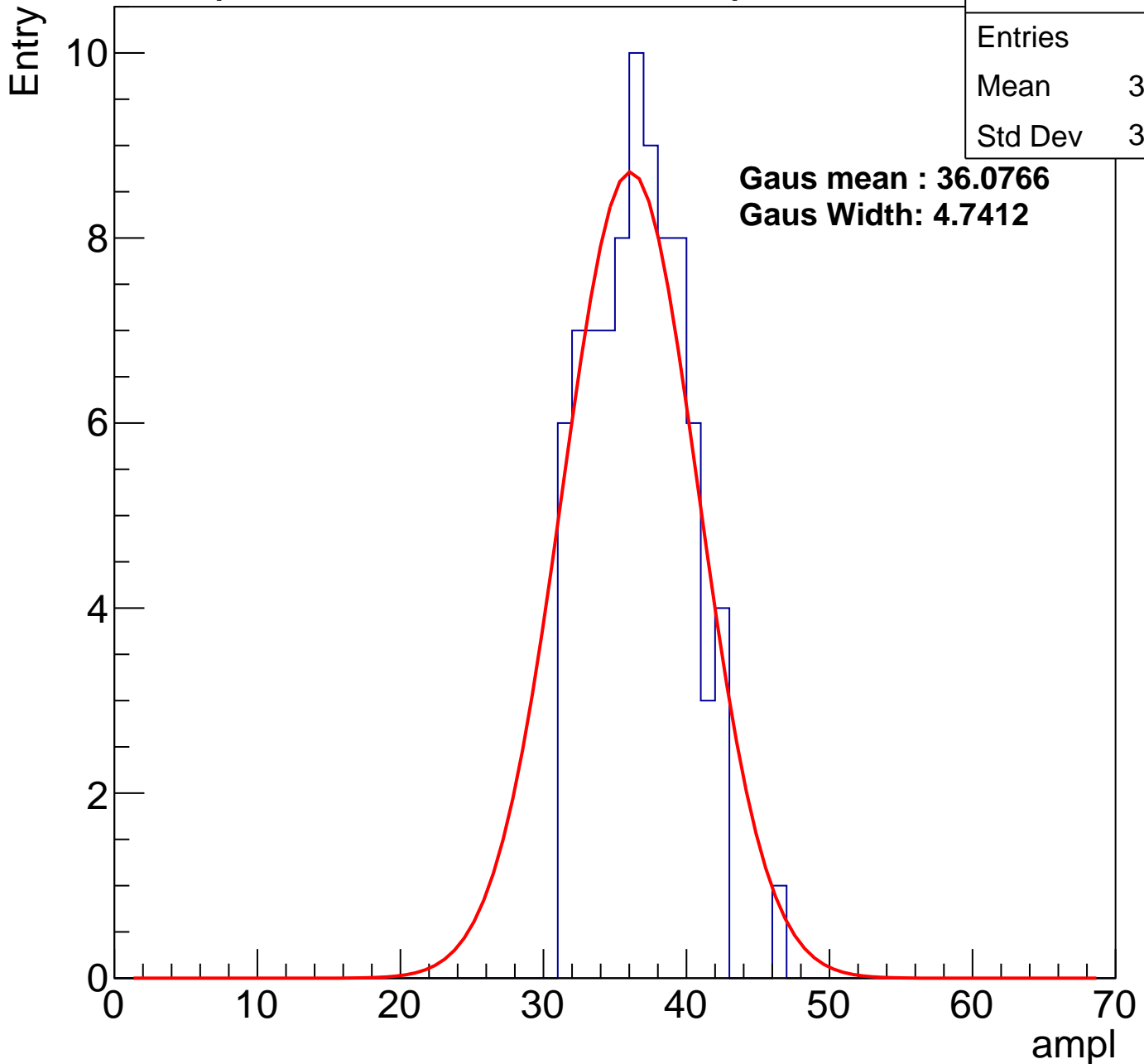
# B1L003S, U11-ch16, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	84
Mean	36.25
Std Dev	3.244

**Gaus mean : 36.0766**

**Gaus Width: 4.7412**



# B1L003S, U11-ch16, adc2

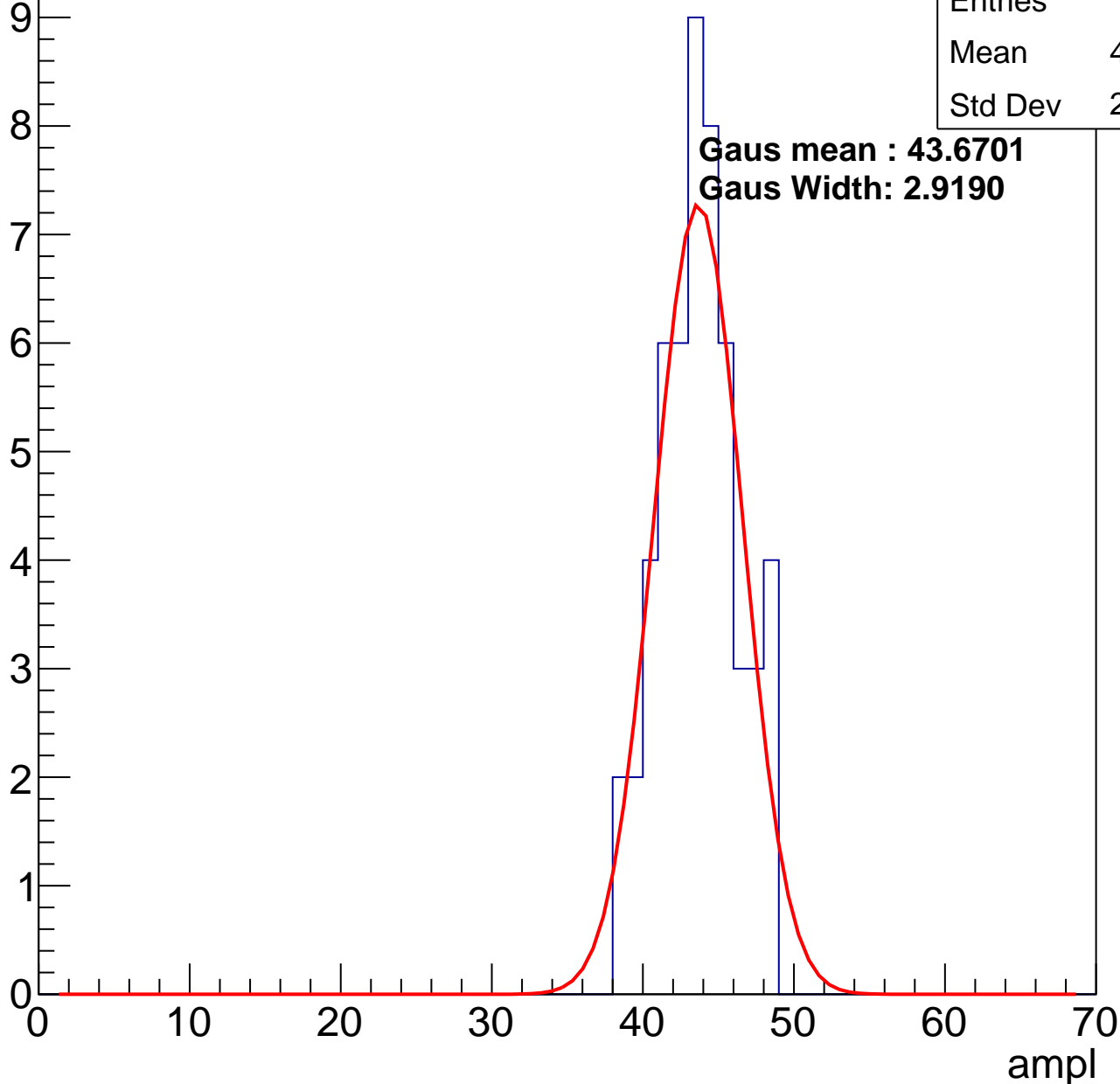
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	43.25
Std Dev	2.576

**Gaus mean : 43.6701**

**Gaus Width: 2.9190**



# B1L003S, U11-ch16, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	63
Mean	49.02
Std Dev	3.15

Entry

10

8

6

4

2

0

0

10

20

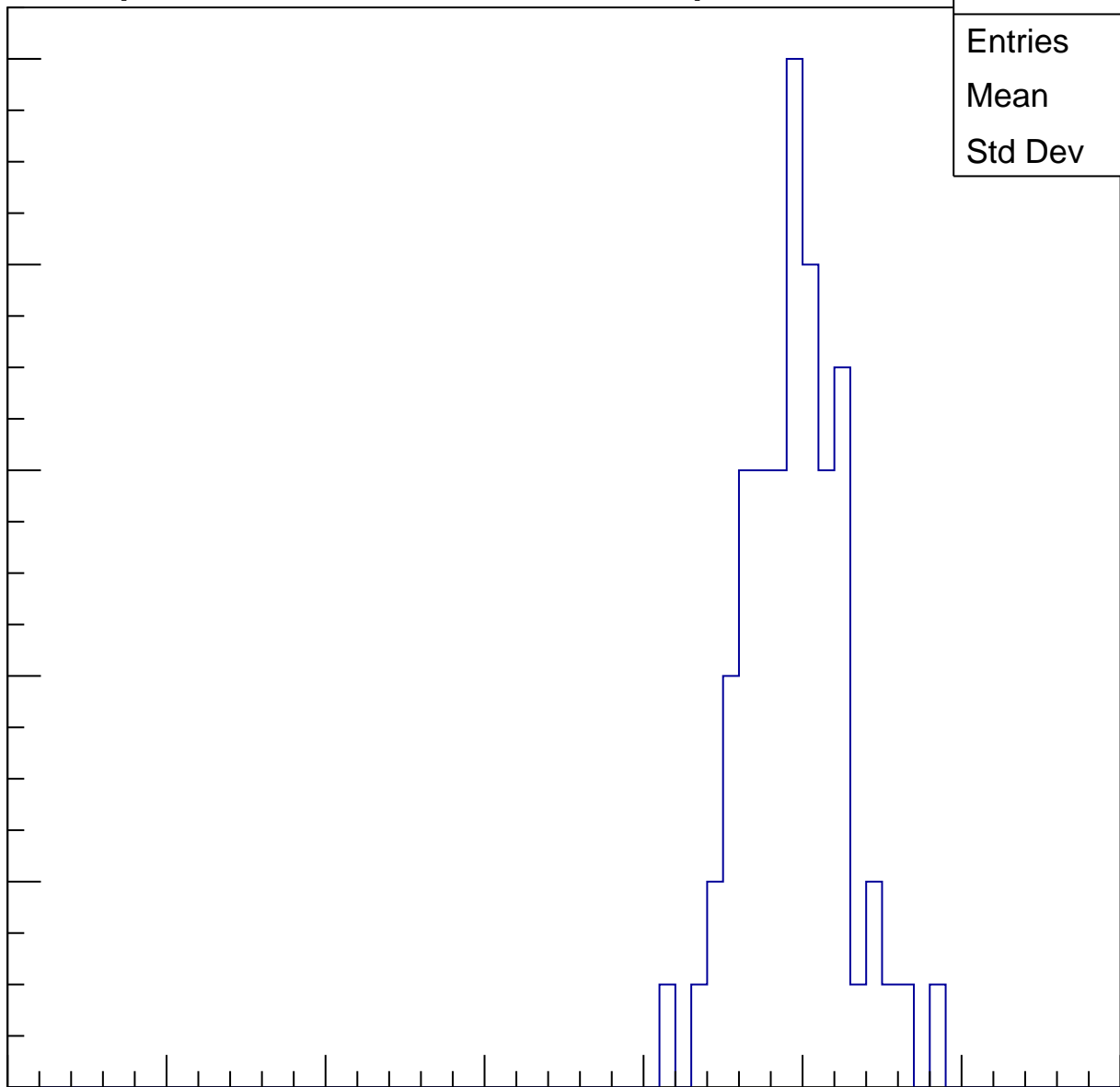
30

40

50

60

ampl

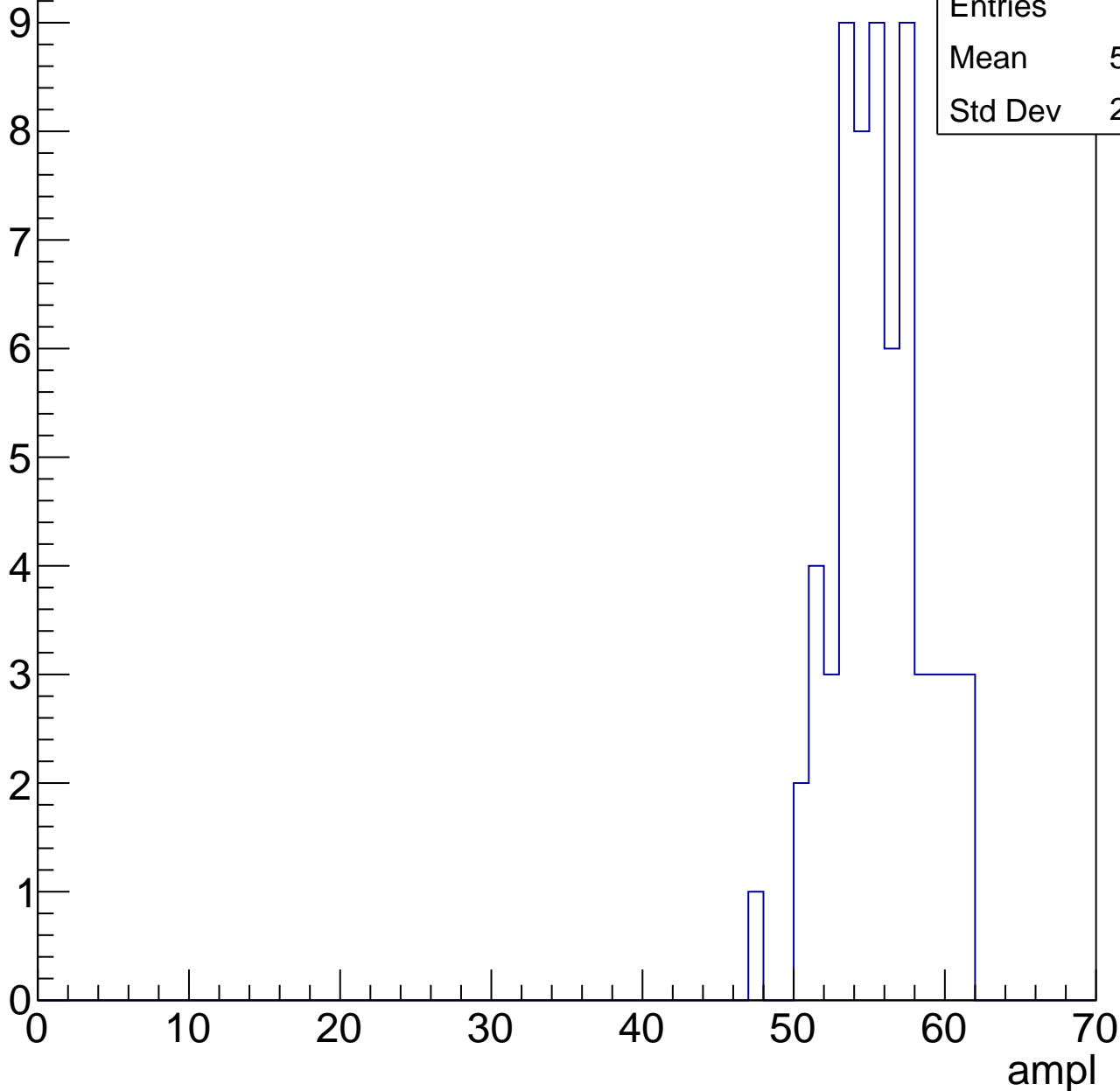


# B1L003S, U11-ch16, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	55.14
Std Dev	2.949

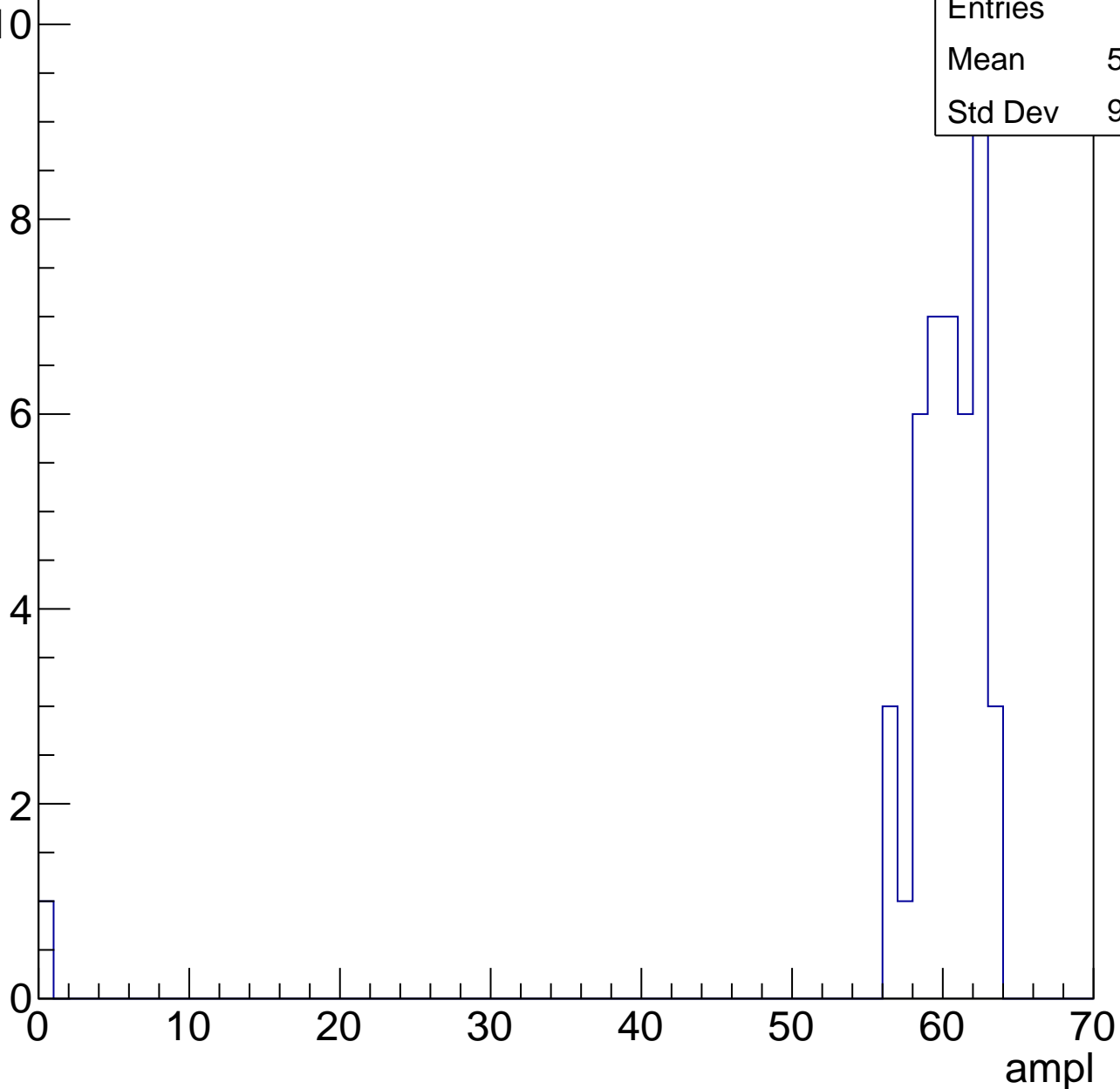


# B1L003S, U11-ch16, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	44
Mean	58.66
Std Dev	9.148

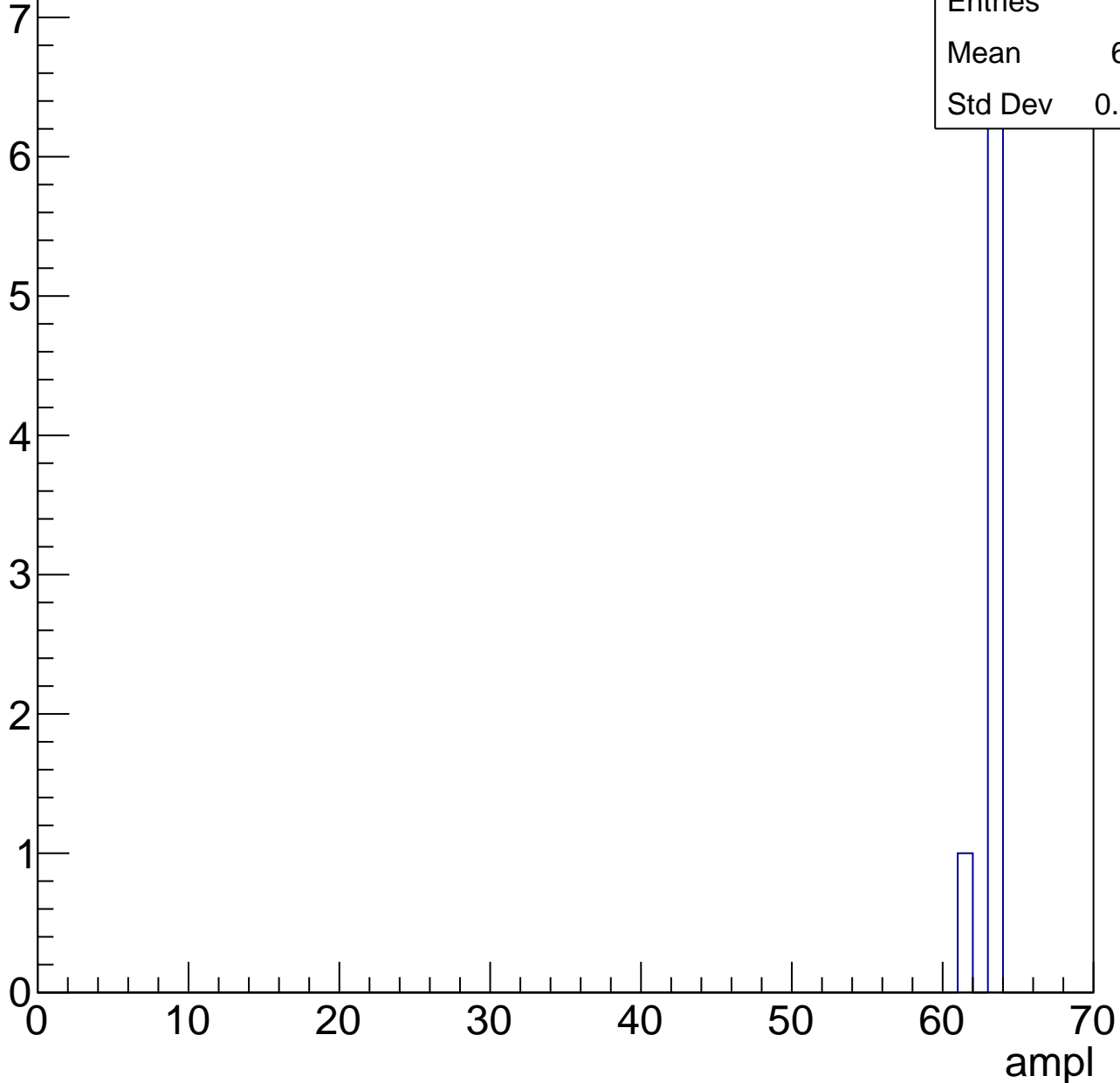


# B1L003S, U11-ch16, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	8
Mean	62.75
Std Dev	0.6614





# B1L003S, U11-ch16, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U11-ch17, adc0

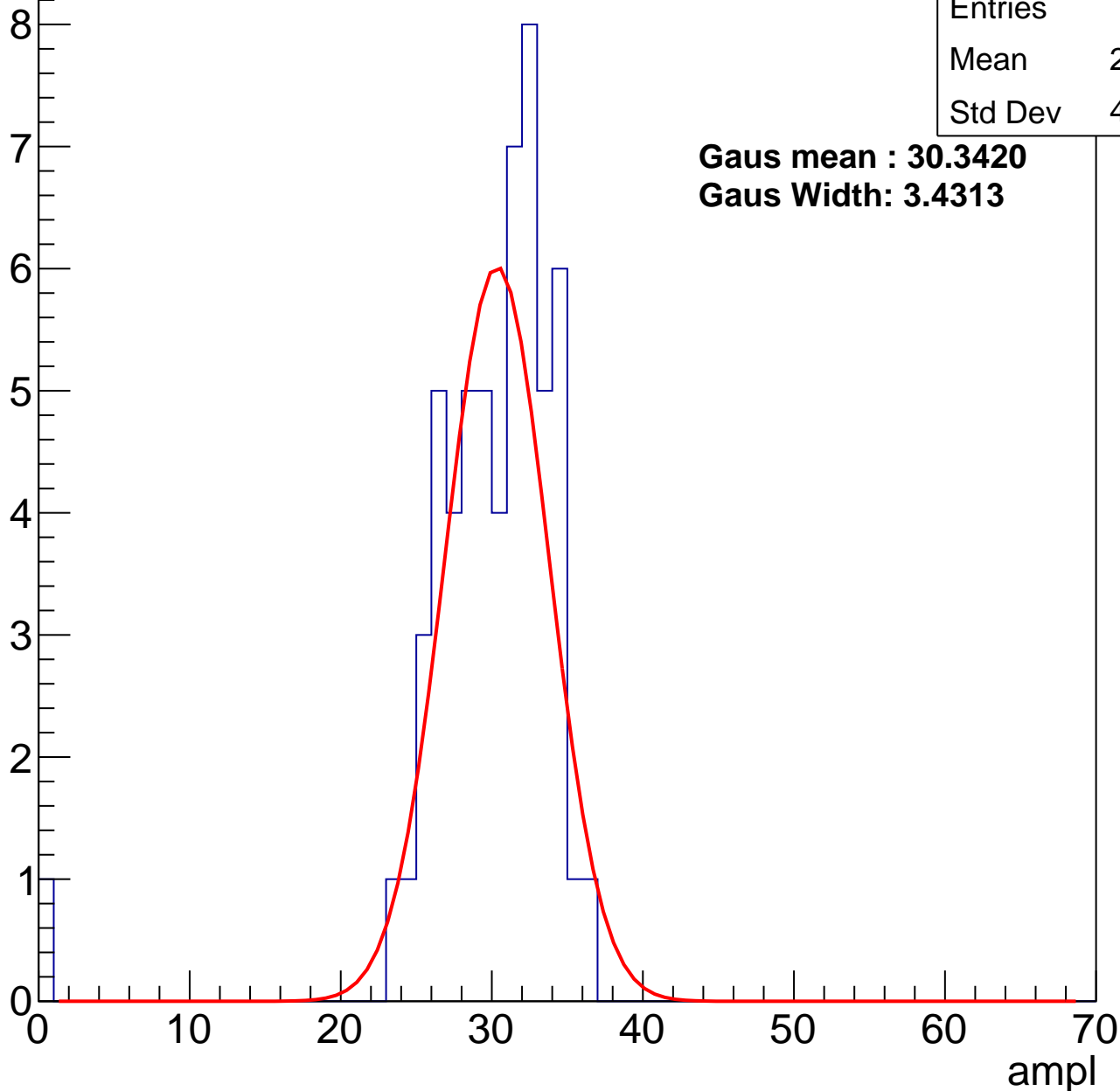
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	29.44
Std Dev	4.998

**Gaus mean : 30.3420**

**Gaus Width: 3.4313**



# B1L003S, U11-ch17, adc1

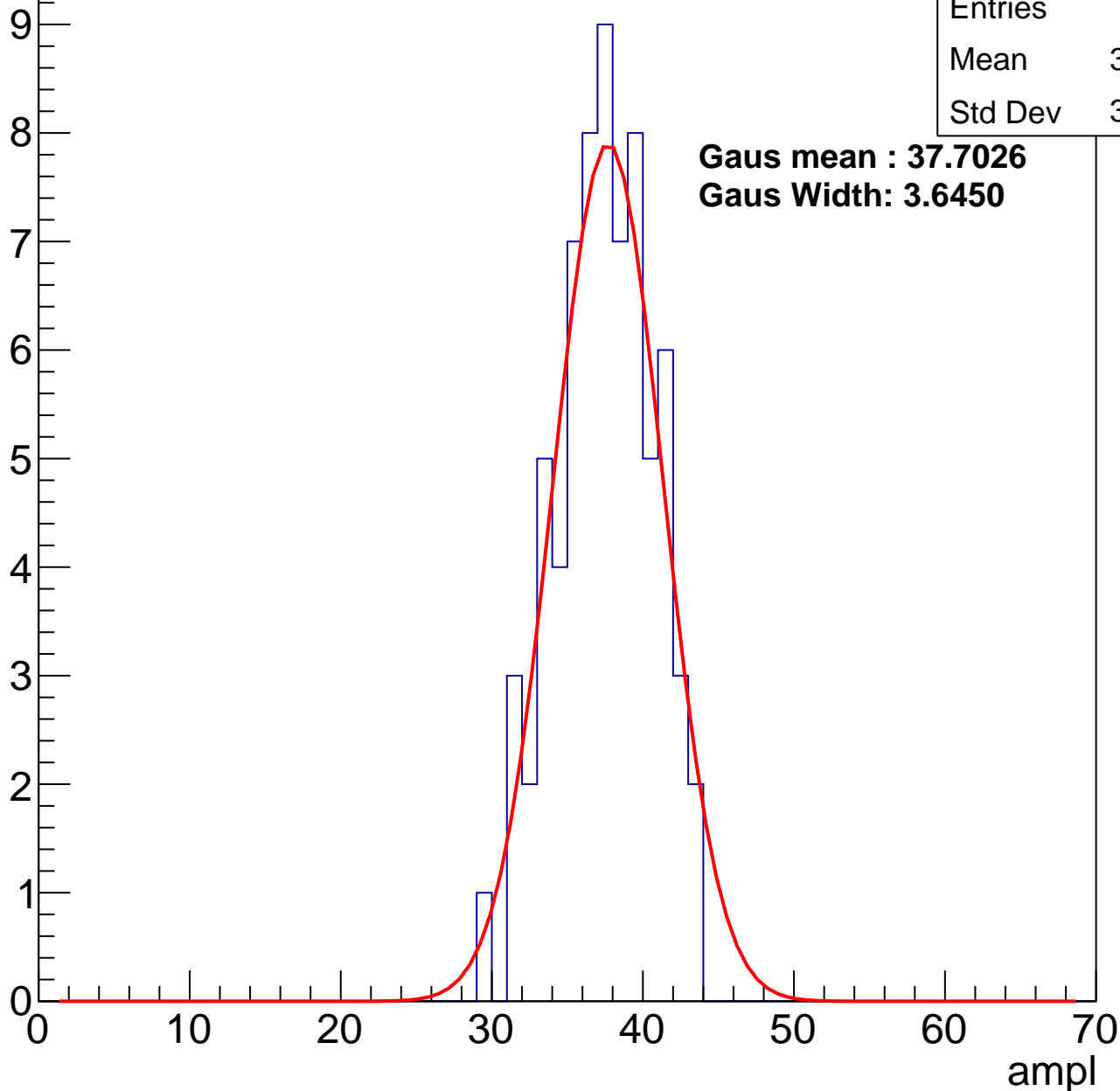
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	36.99
Std Dev	3.165

**Gaus mean : 37.7026**

**Gaus Width: 3.6450**



# B1L003S, U11-ch17, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	77
Mean	44.08
Std Dev	3.762

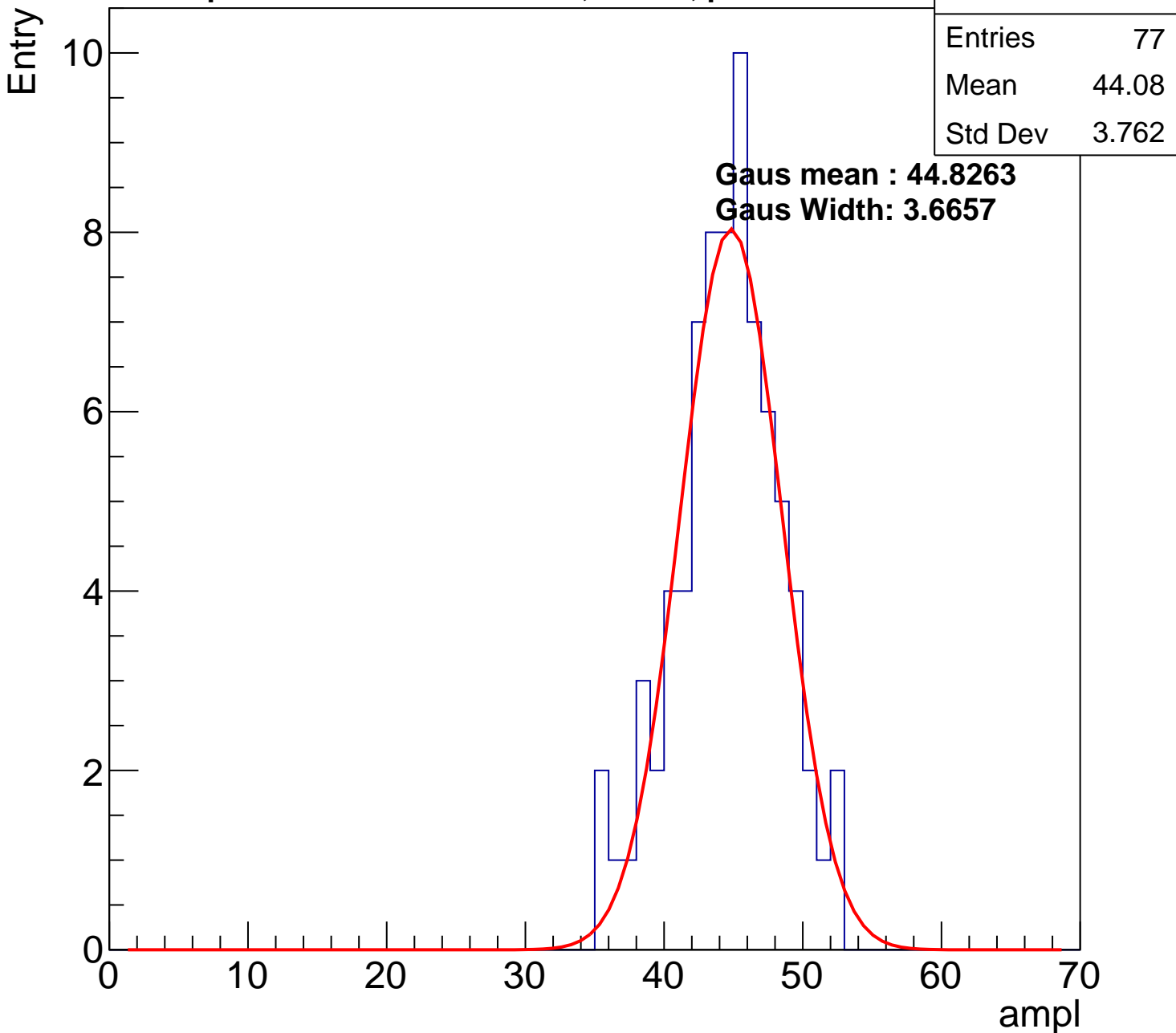
**Gaus mean : 44.8263**

**Gaus Width: 3.6657**

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

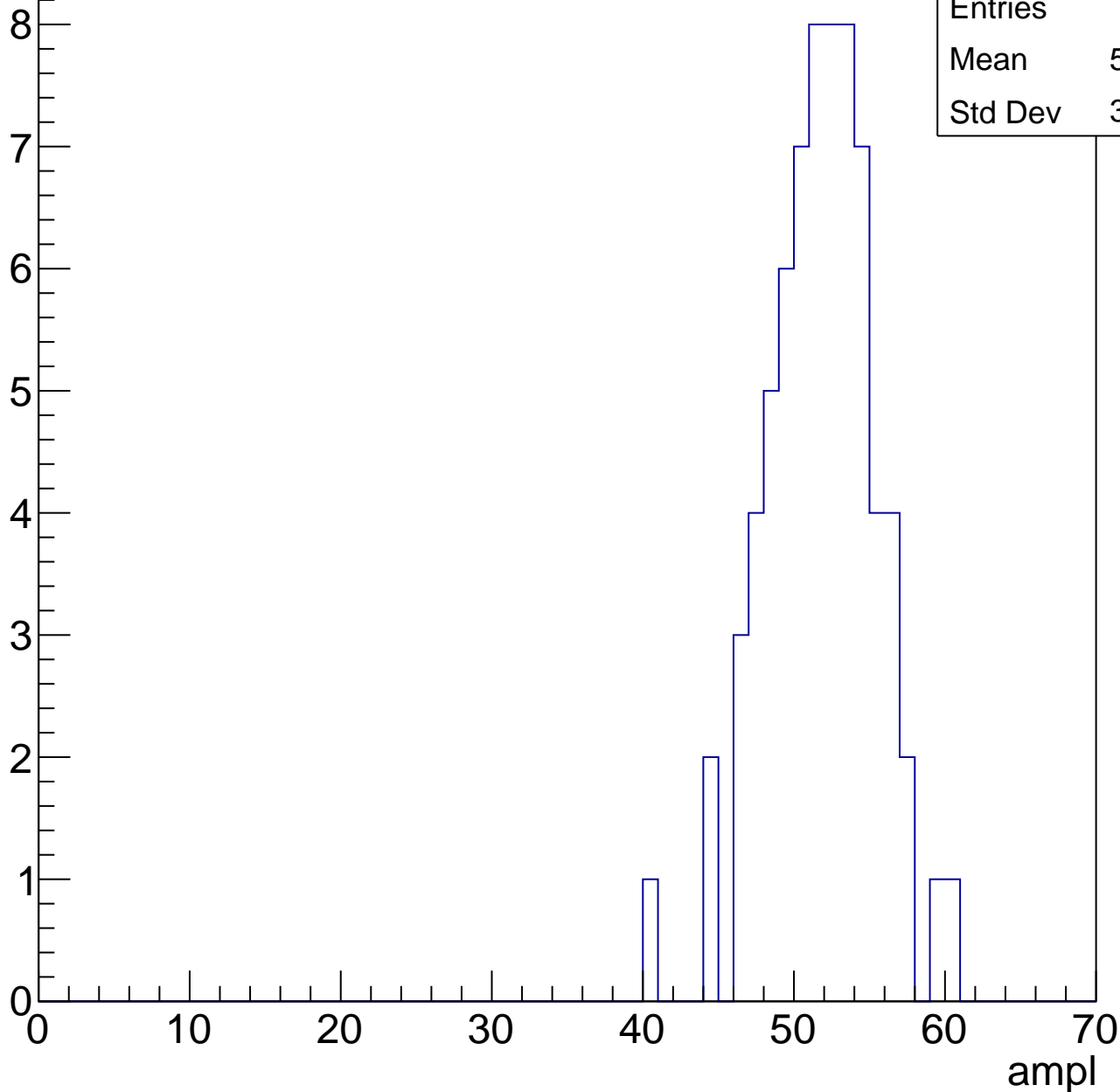


# B1L003S, U11-ch17, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	71
Mean	51.28
Std Dev	3.585

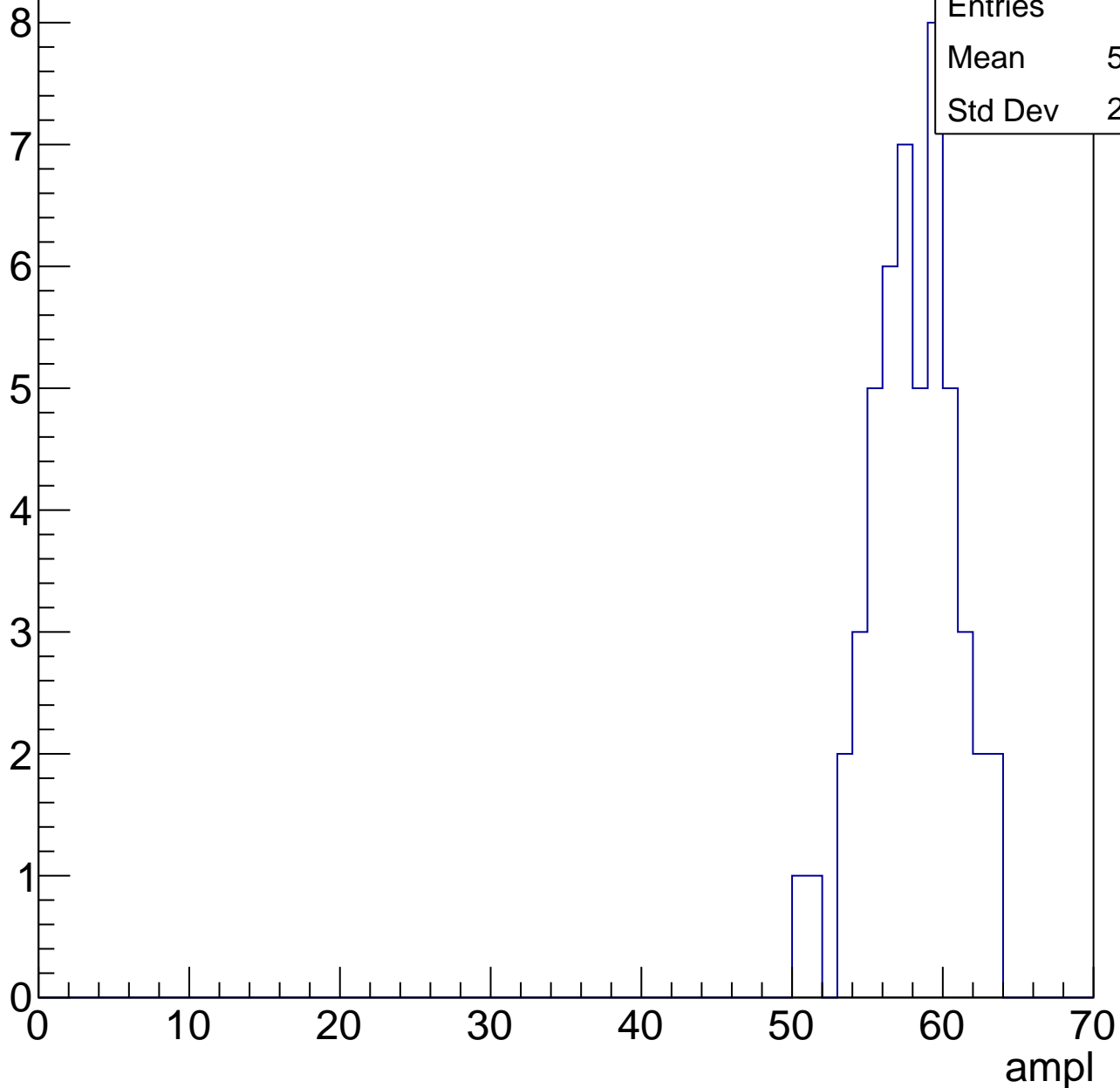


# B1L003S, U11-ch17, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	50
Mean	57.48
Std Dev	2.865

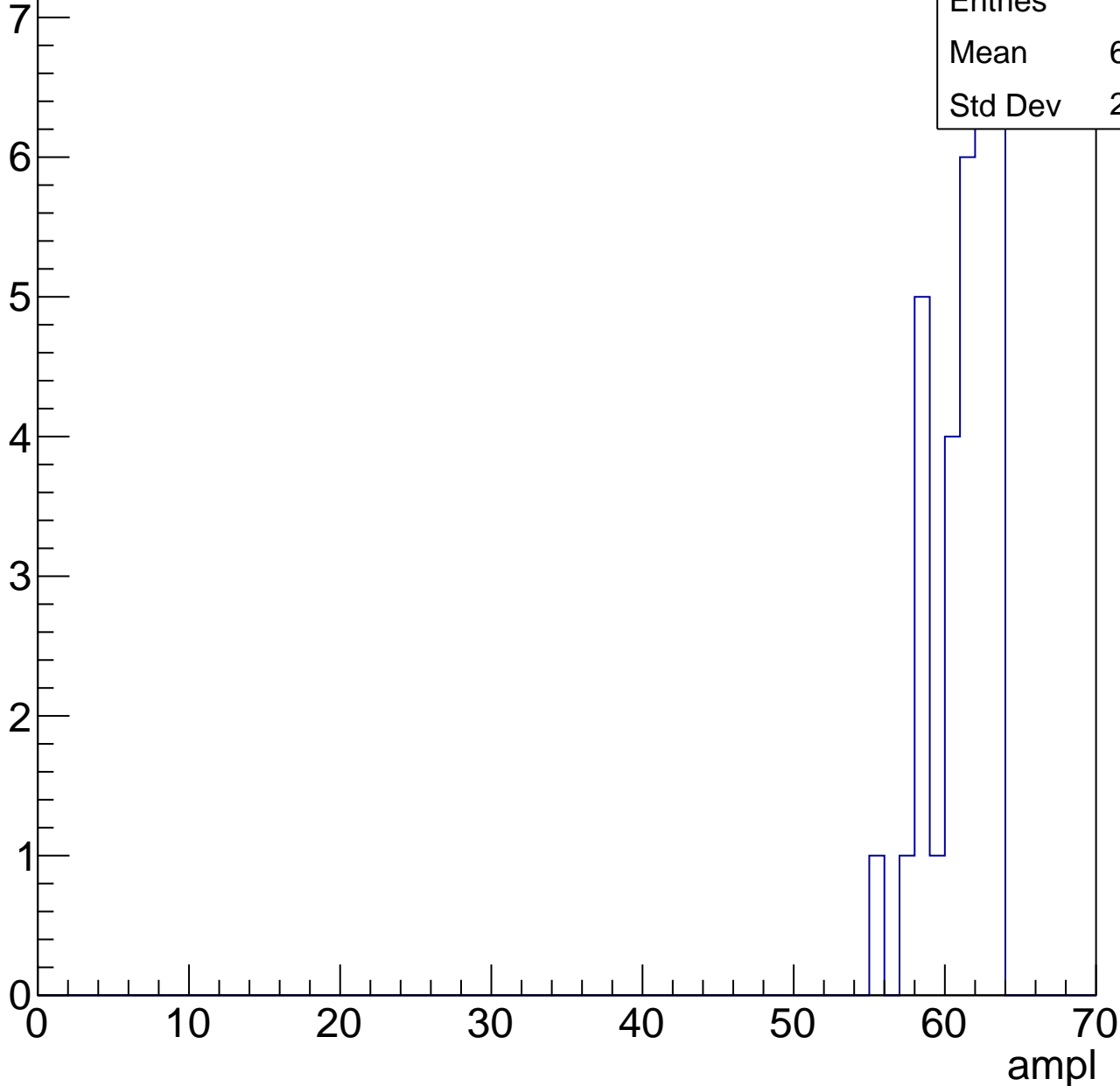


# B1L003S, U11-ch17, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

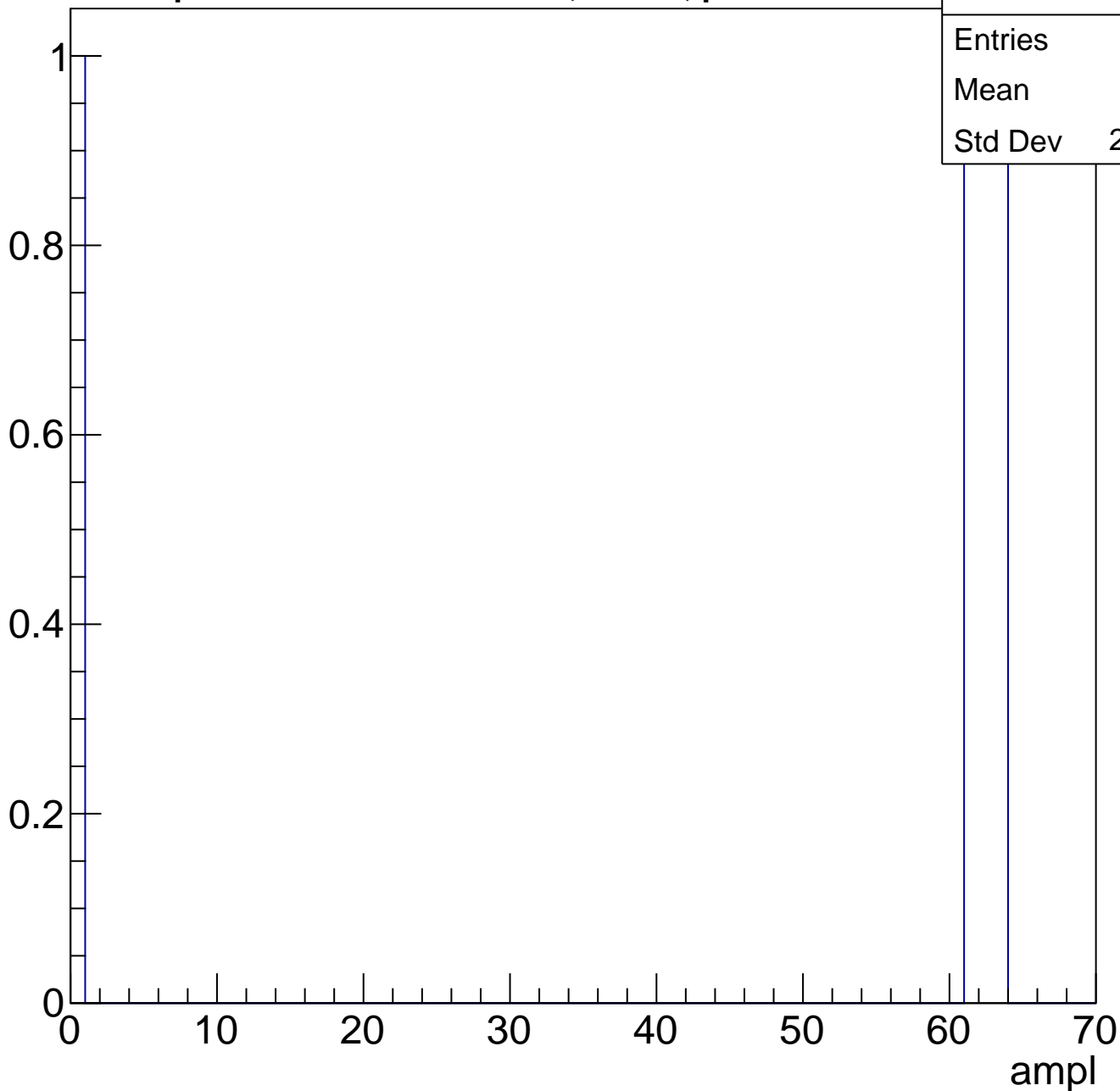
Entries	32
Mean	60.69
Std Dev	2.068



# B1L003S, U11-ch17, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch17, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U11-ch18, adc0

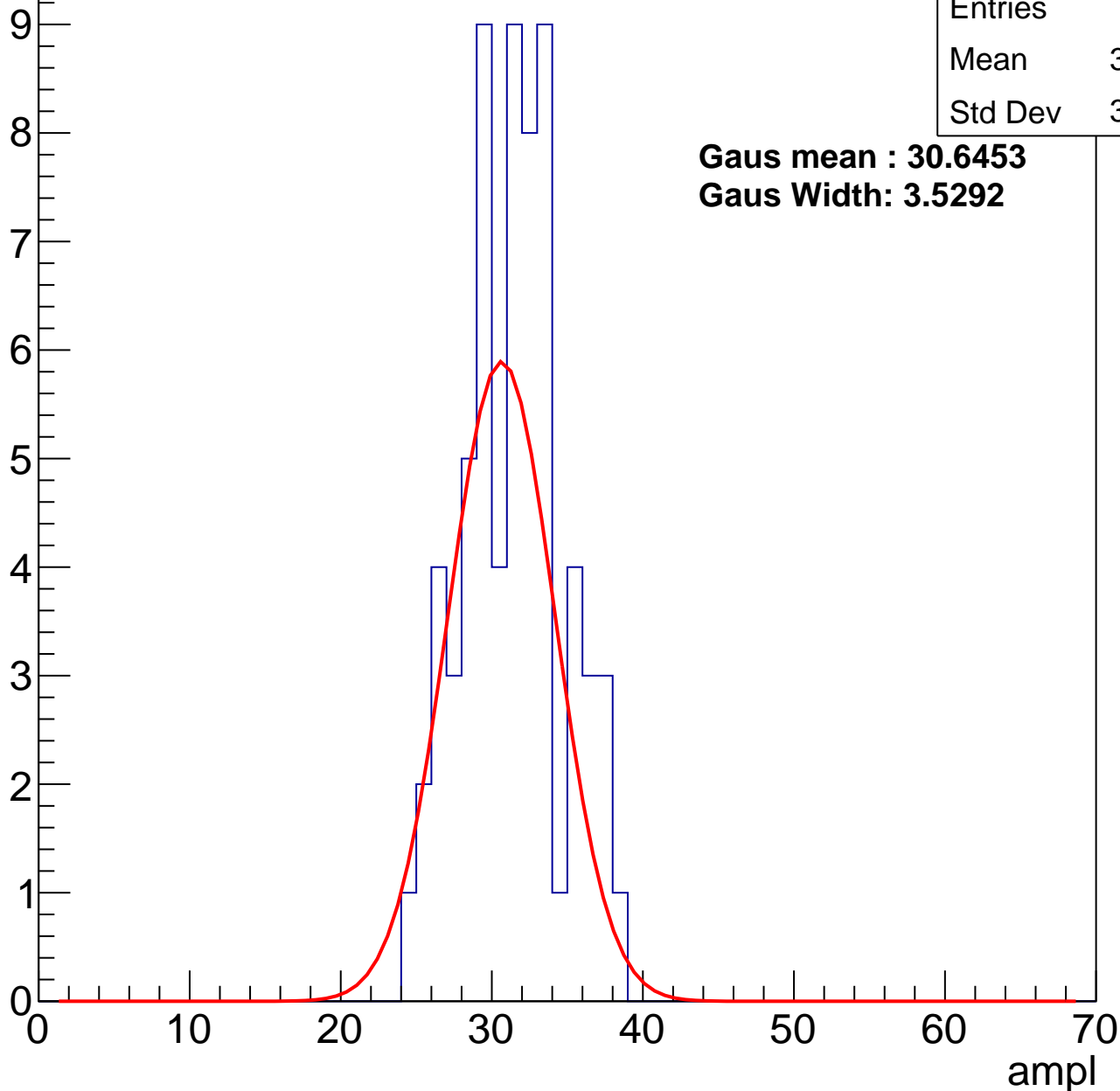
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	30.95
Std Dev	3.263

**Gaus mean : 30.6453**

**Gaus Width: 3.5292**



# B1L003S, U11-ch18, adc1

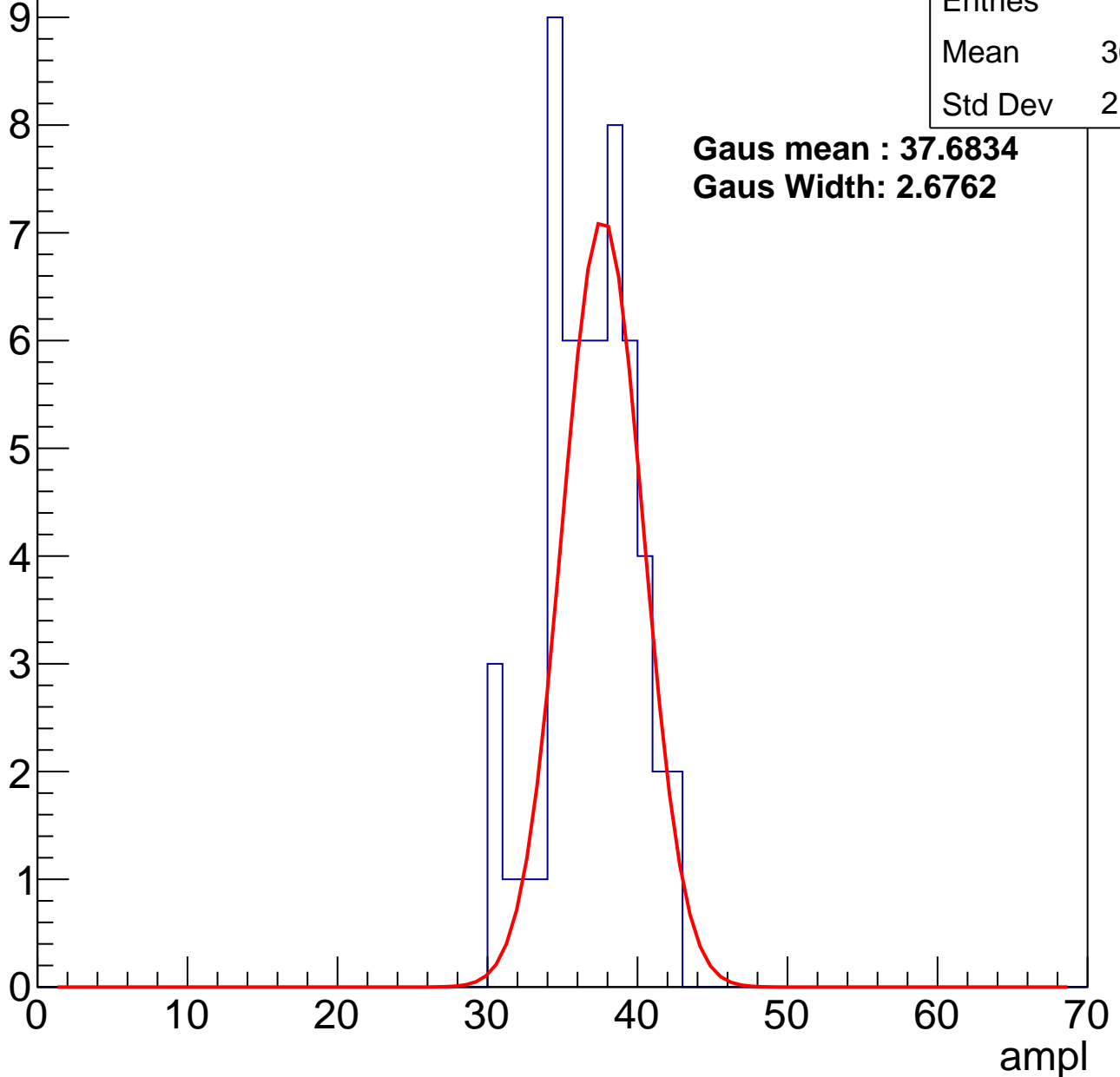
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	36.44
Std Dev	2.916

**Gaus mean : 37.6834**

**Gaus Width: 2.6762**



# B1L003S, U11-ch18, adc2

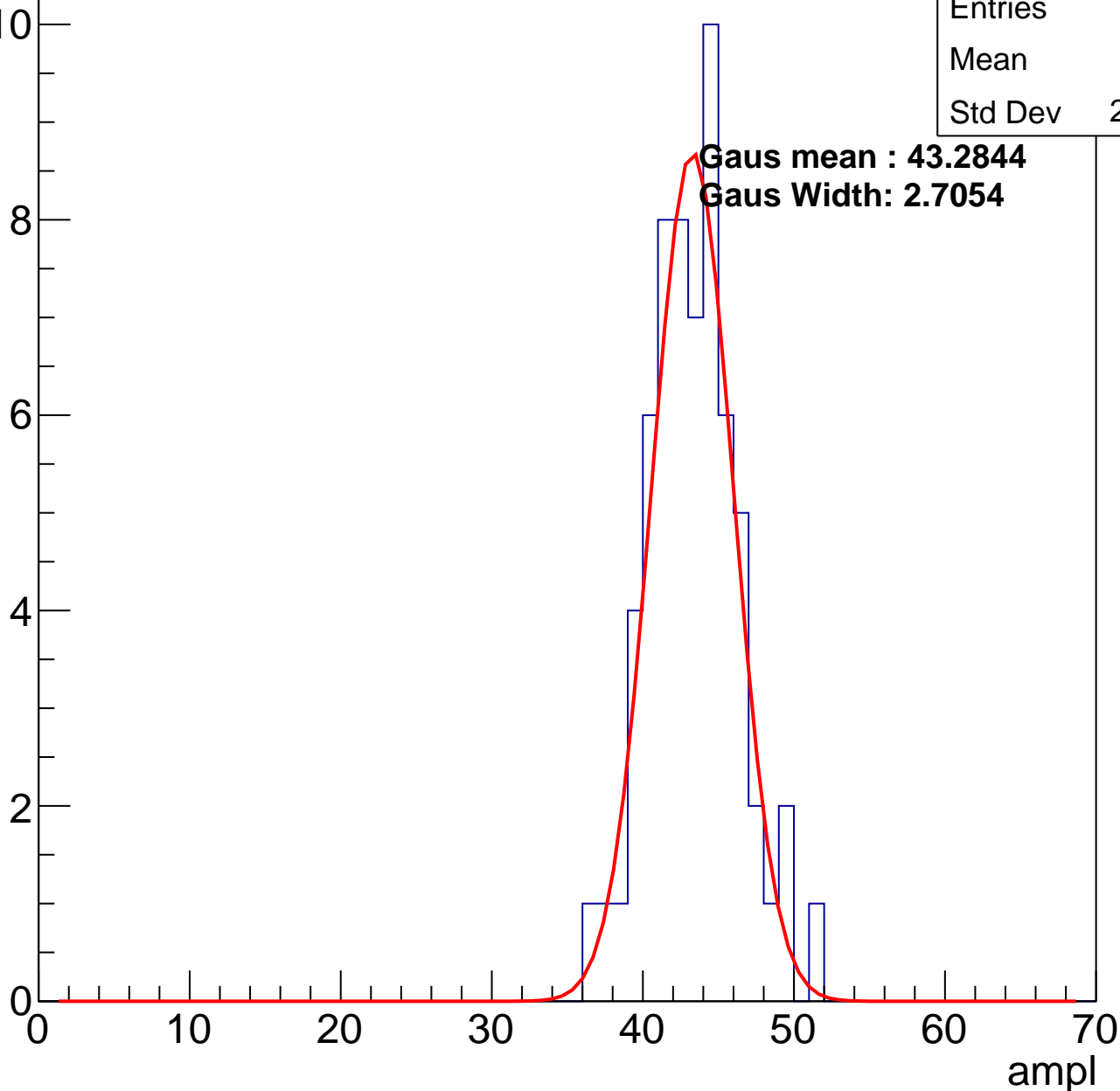
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	42.9
Std Dev	2.926

**Gaus mean : 43.2844**

**Gaus Width: 2.7054**



# B1L003S, U11-ch18, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	72
Mean	49.5
Std Dev	3.131

Entry

10

8

6

4

2

0

0

10

20

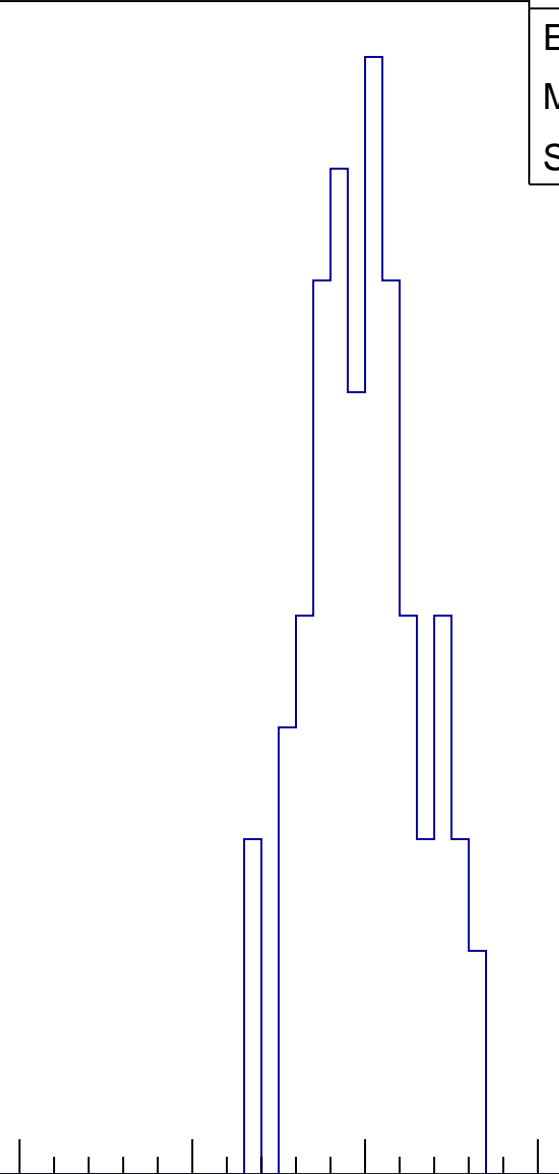
30

40

50

60

ampl



# B1L003S, U11-ch18, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	62
Mean	56.13
Std Dev	2.871

Entry

10

8

6

4

2

0

0

10

20

30

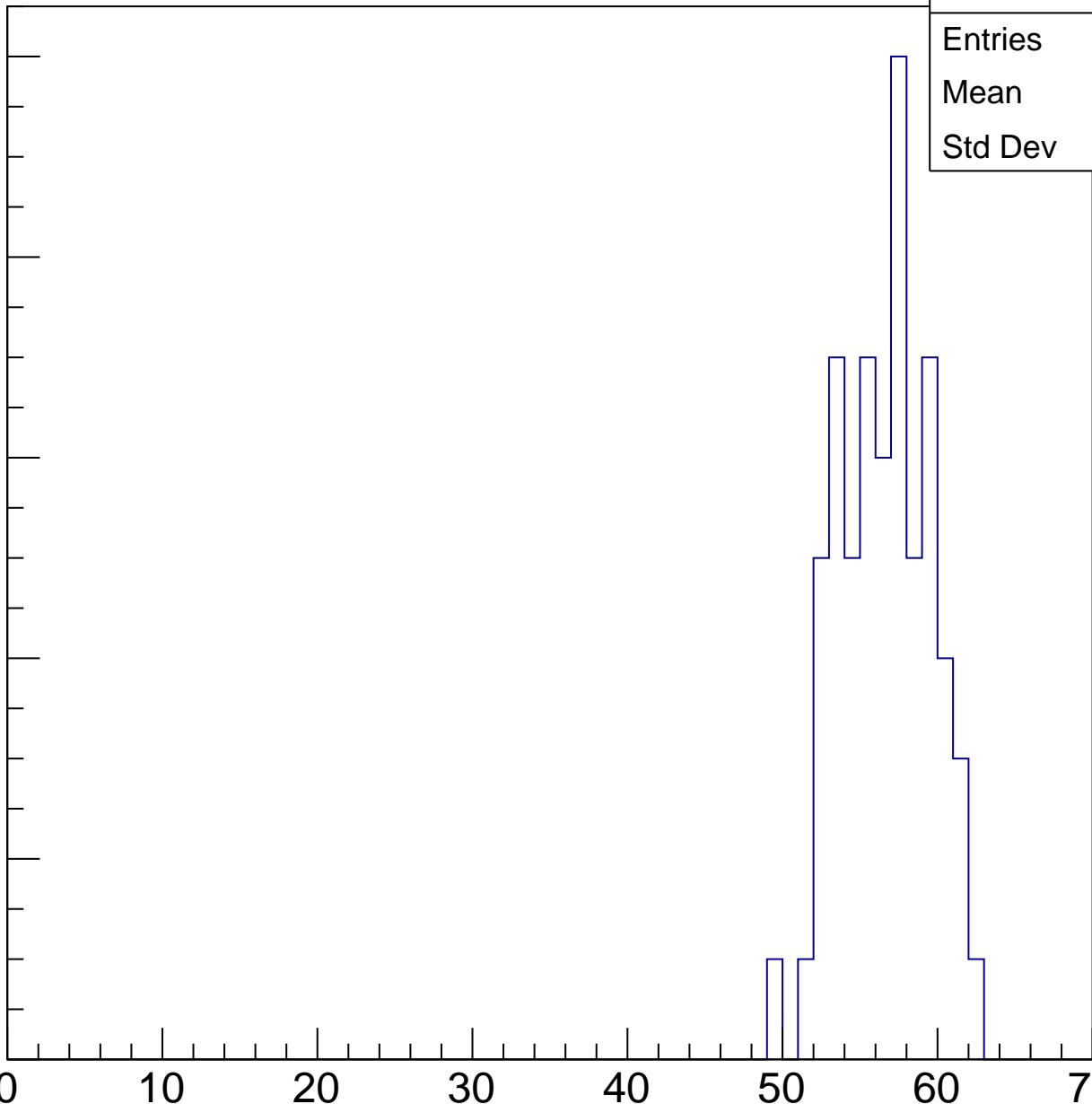
40

50

60

70

ampl



# B1L003S, U11-ch18, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	41
Mean	59.27
Std Dev	9.574

Entry

10

8

6

4

2

0

0

10

20

30

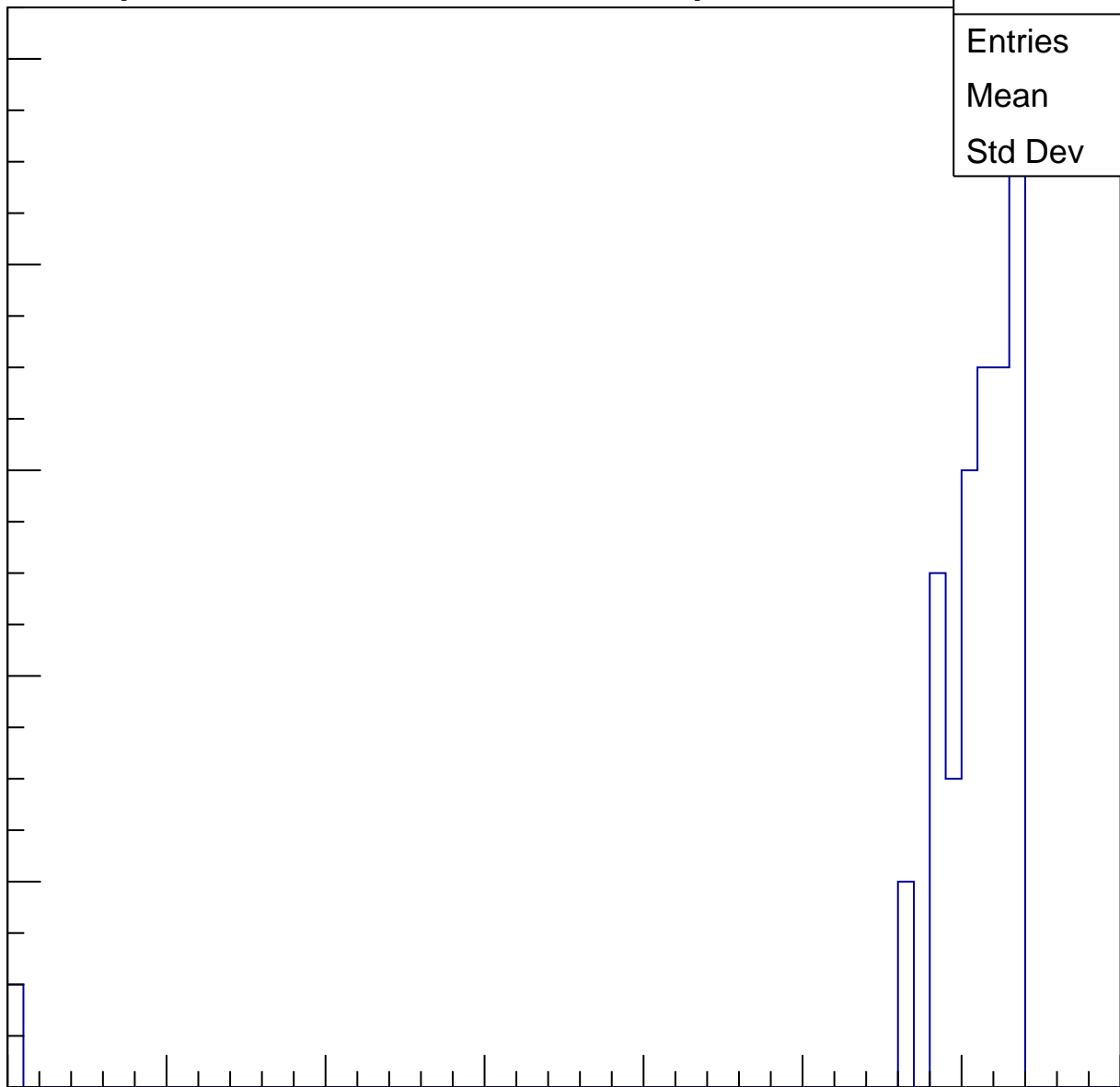
40

50

60

70

ampl



# B1L003S, U11-ch18, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	62
Std Dev	0

ampl



# B1L003S, U11-ch18, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U11-ch19, adc0

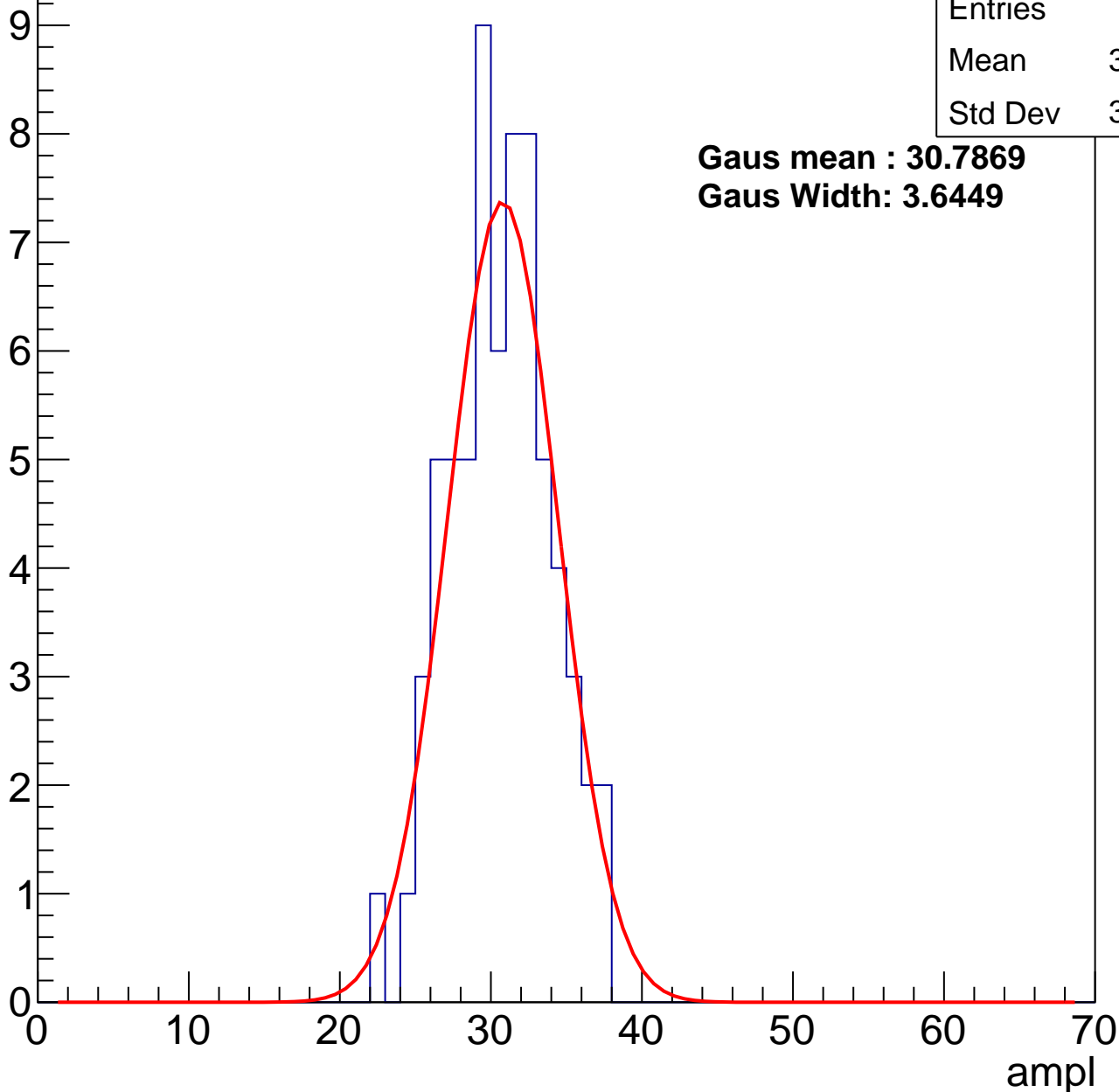
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	30.19
Std Dev	3.279

**Gaus mean : 30.7869**

**Gaus Width: 3.6449**



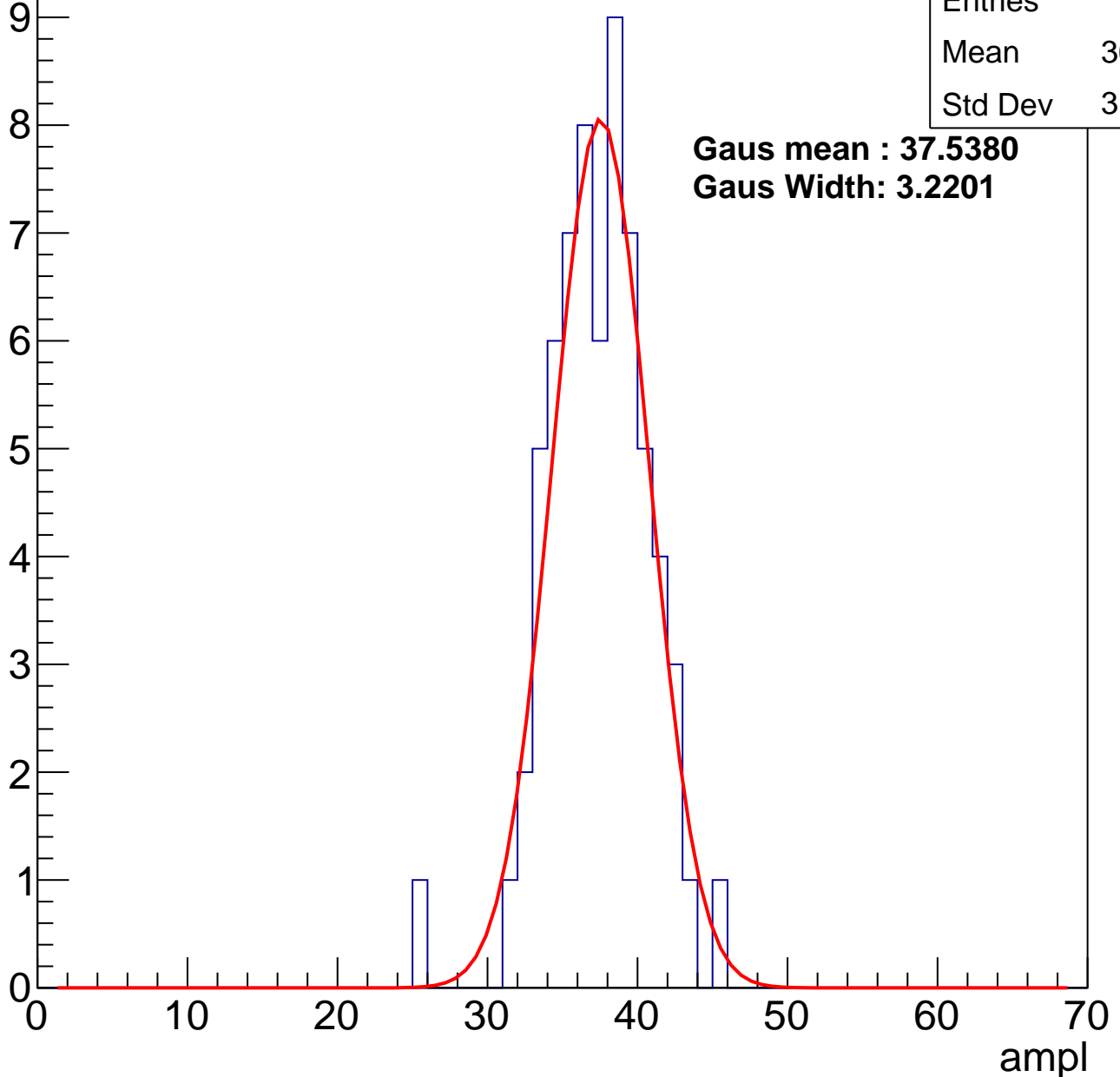
# B1L003S, U11-ch19, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	36.92
Std Dev	3.304

**Gaus mean : 37.5380**  
**Gaus Width: 3.2201**



# B1L003S, U11-ch19, adc2

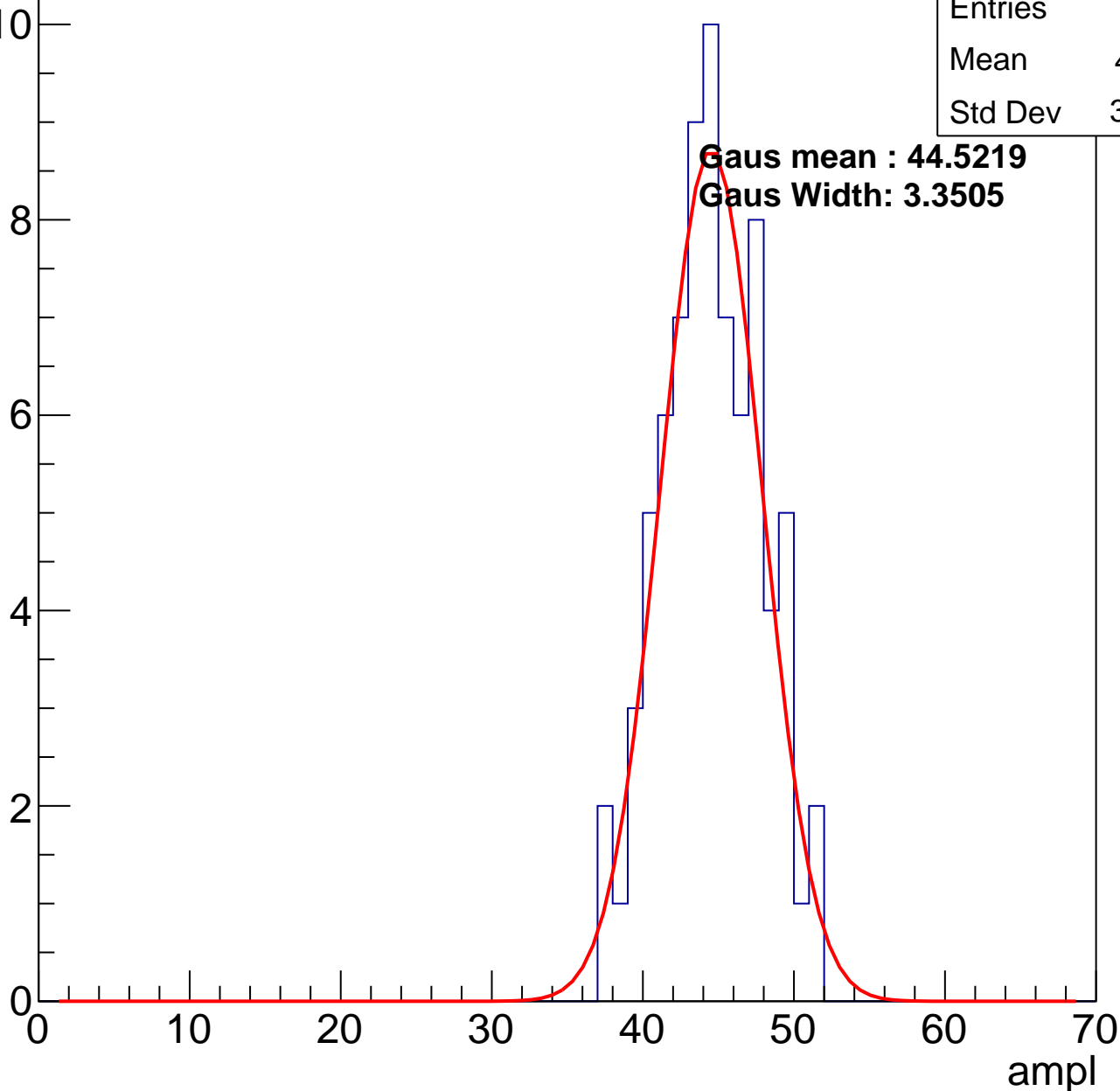
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	76
Mean	44.11
Std Dev	3.255

**Gaus mean : 44.5219**

**Gaus Width: 3.3505**

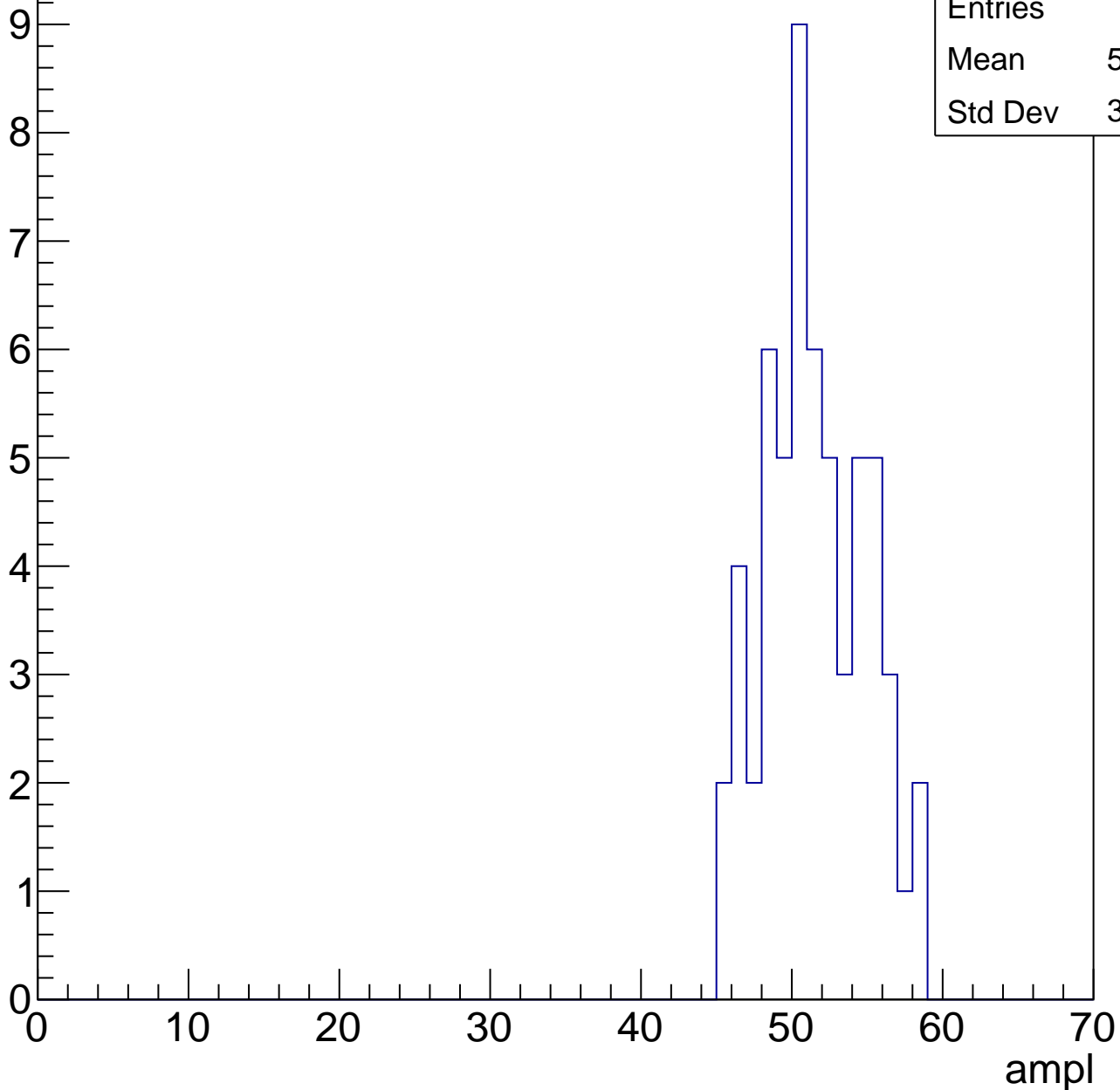


# B1L003S, U11-ch19, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	51.07
Std Dev	3.316

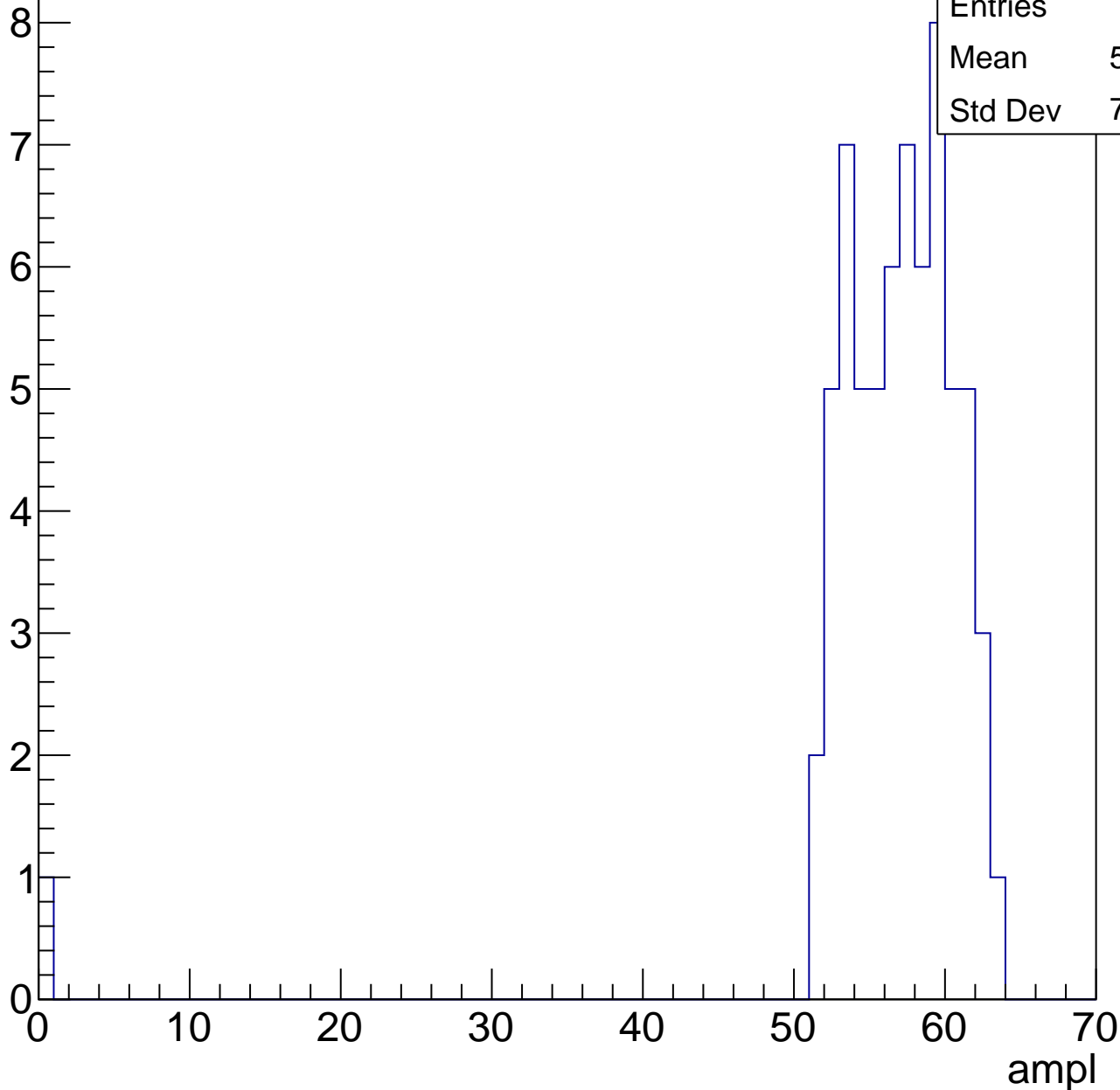


# B1L003S, U11-ch19, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	55.86
Std Dev	7.606



# B1L003S, U11-ch19, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

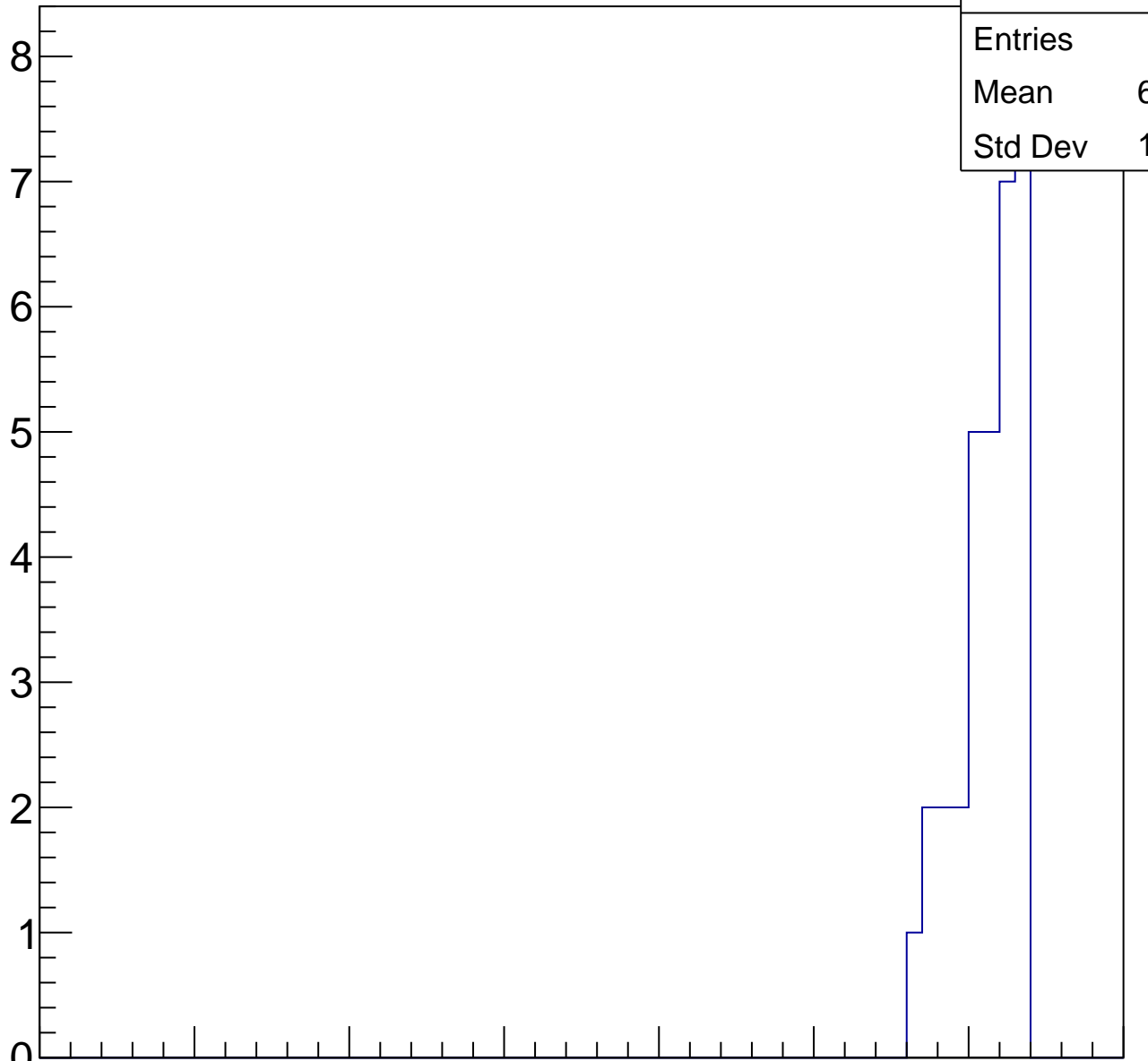
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	32
Mean	60.84
Std Dev	1.986

ampl

0 10 20 30 40 50 60 70



# B1L003S, U11-ch19, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

1

Mean

63

Std Dev

0



# B1L003S, U11-ch19, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

0

10

20

30

40

50

60

70

ampl

Entries	1
Mean	22
Std Dev	0

# B1L003S, U11-ch20, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	74
Mean	29.76
Std Dev	3.062

**Gaus mean : 29.7959**

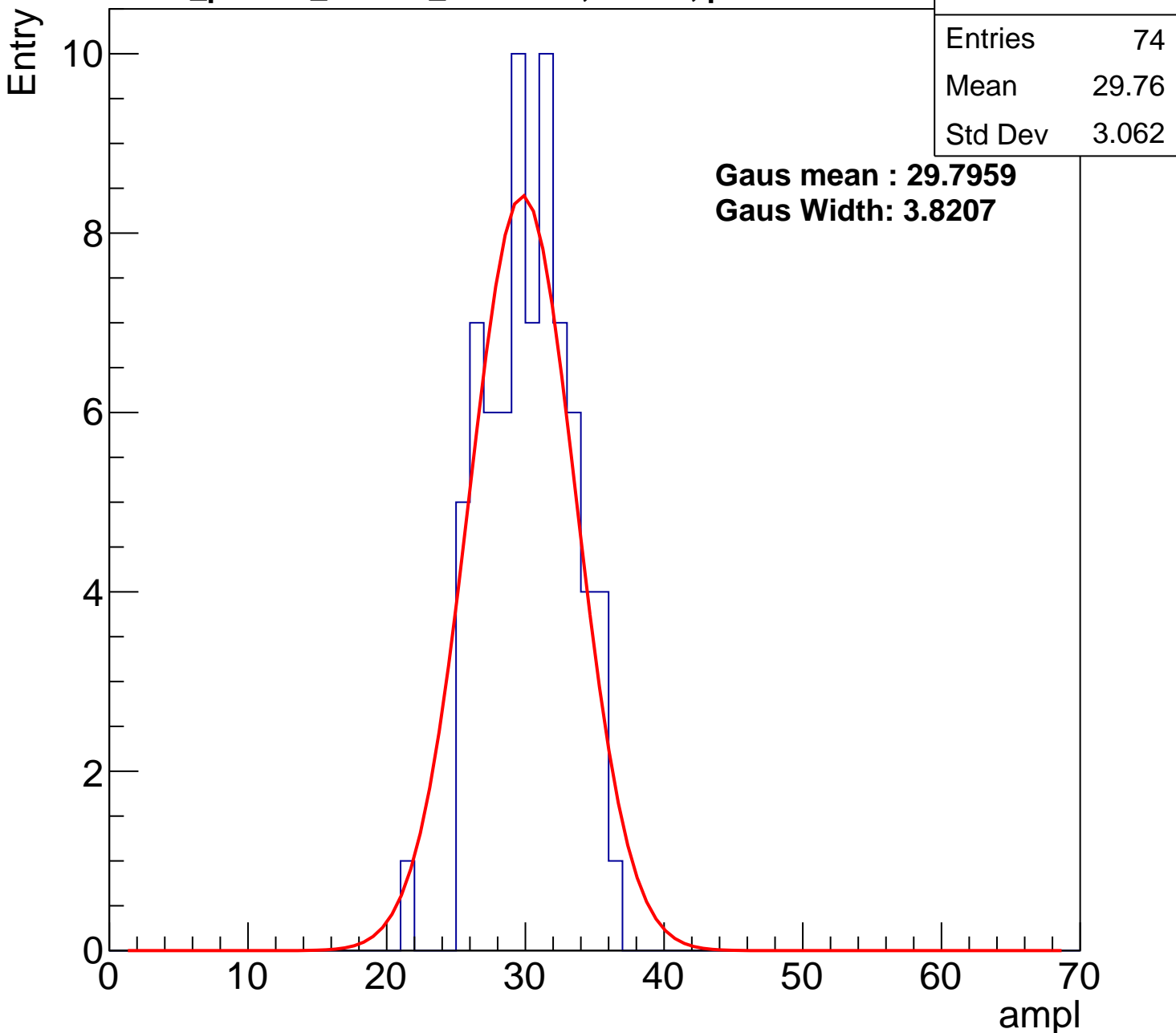
**Gaus Width: 3.8207**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U11-ch20, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	61
Mean	36.38
Std Dev	2.562

**Gaus mean : 36.8590**

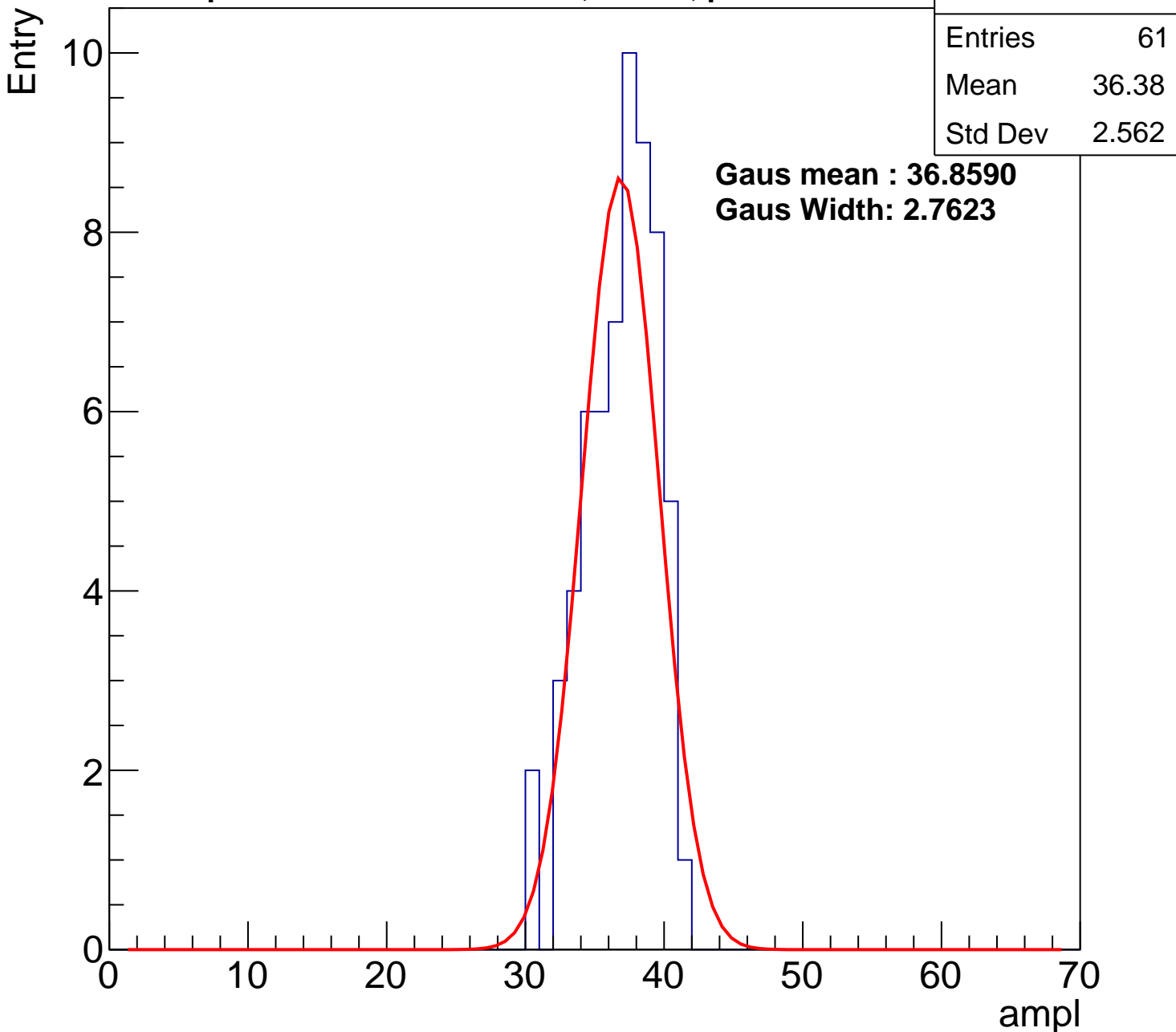
**Gaus Width: 2.7623**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L003S, U11-ch20, adc2

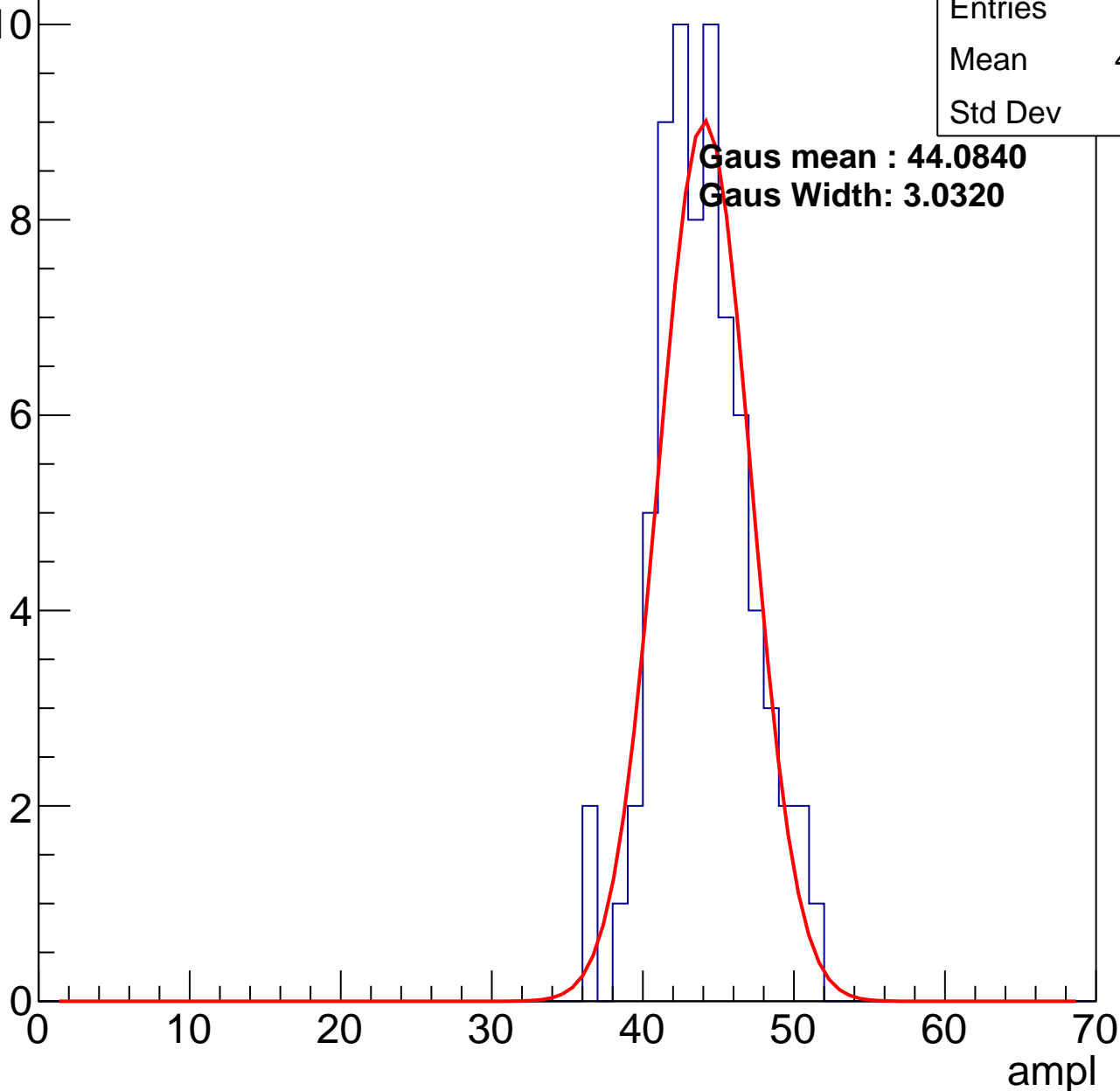
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	72
Mean	43.51
Std Dev	3.1

**Gaus mean : 44.0840**

**Gaus Width: 3.0320**

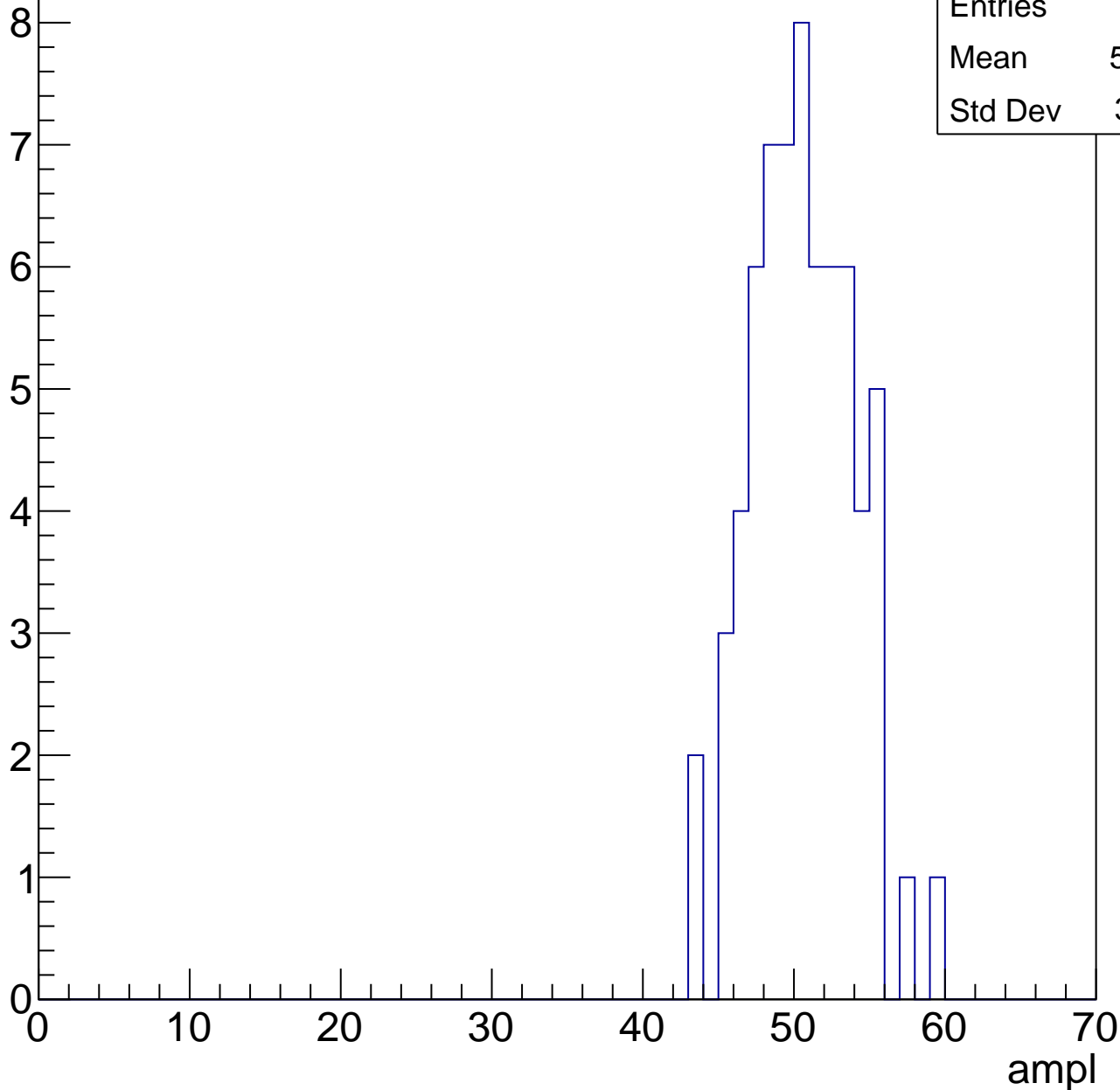


# B1L003S, U11-ch20, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

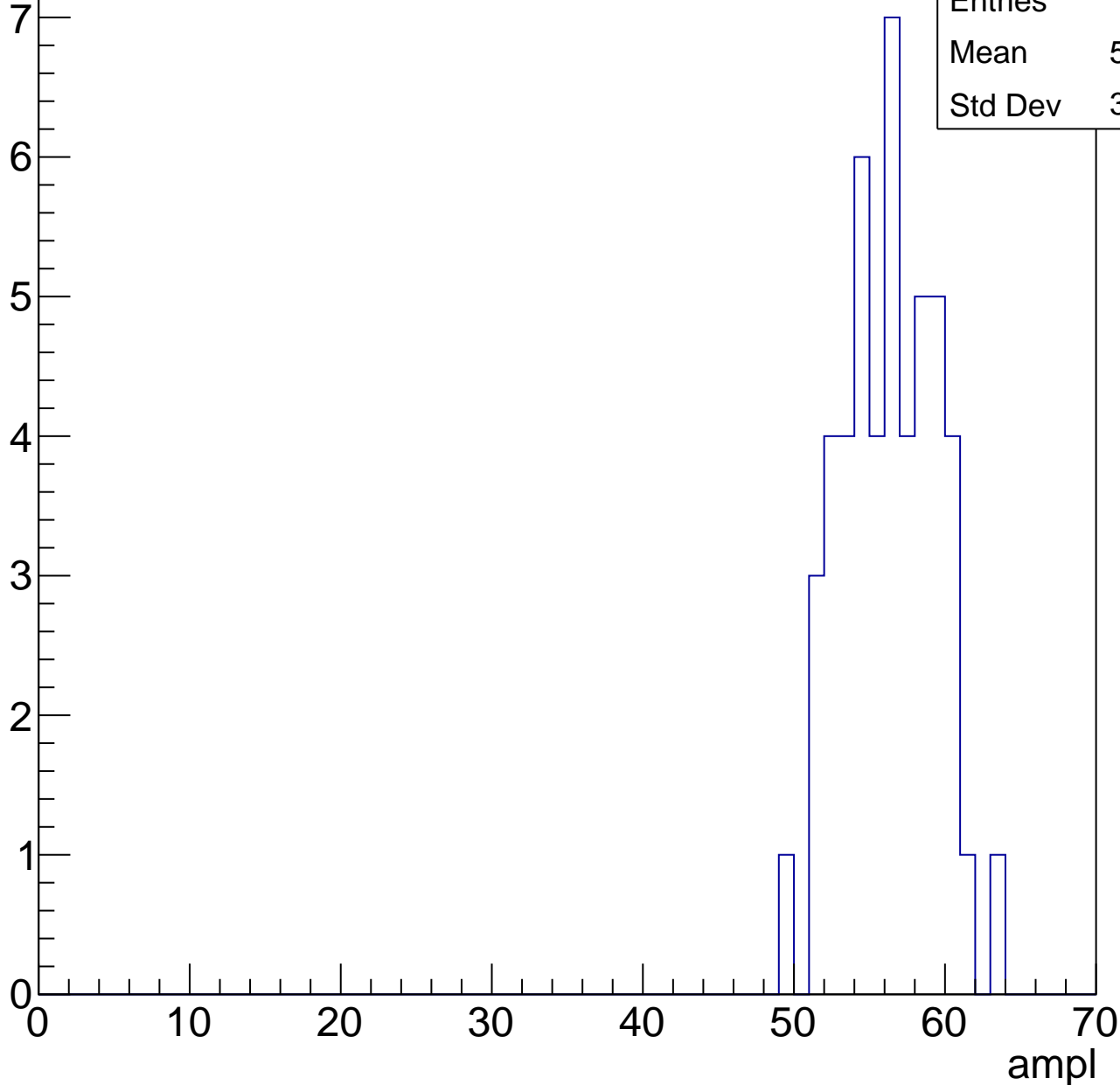
Entries	66
Mean	50.14
Std Dev	3.321



# B1L003S, U11-ch20, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

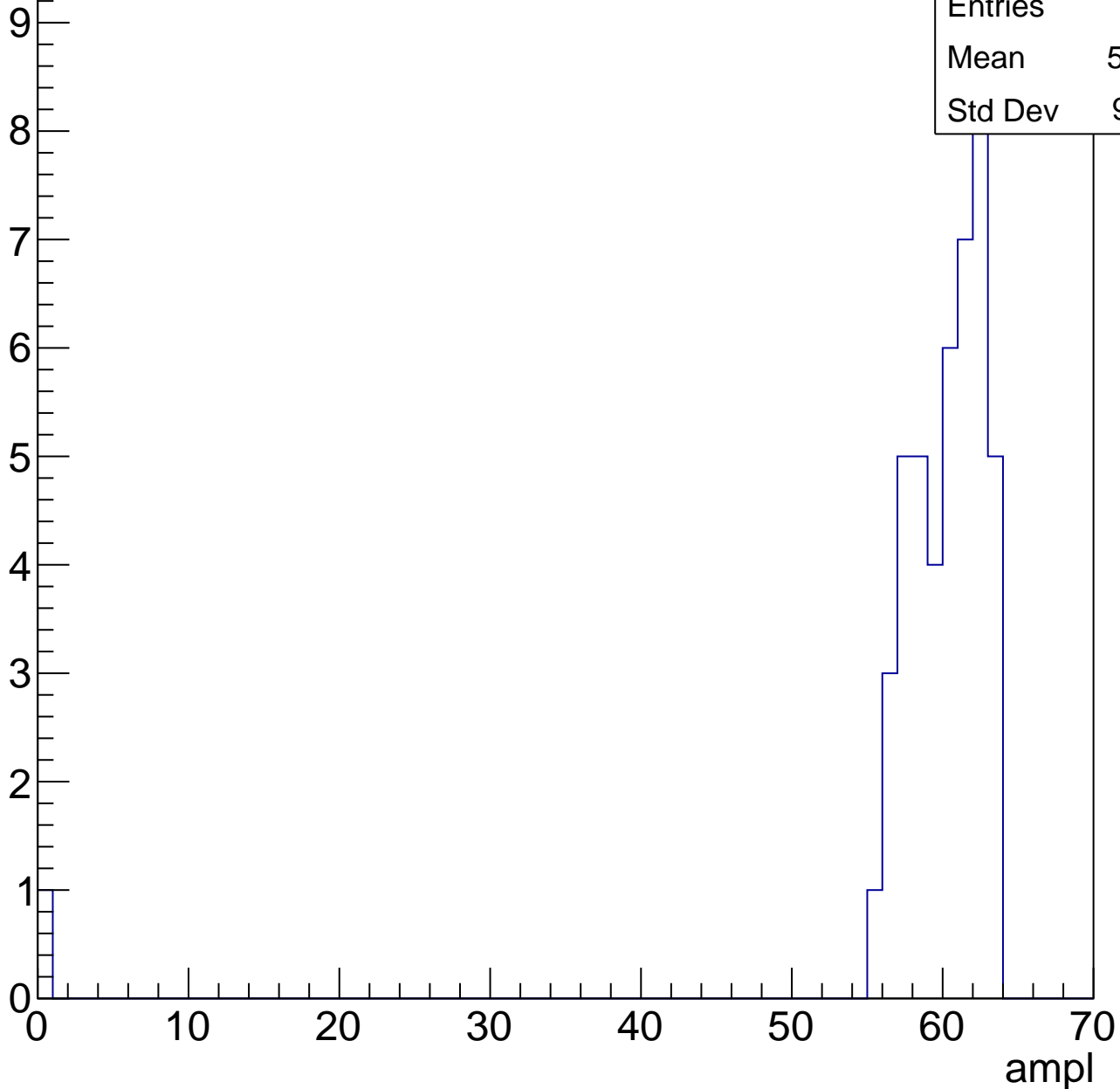


# B1L003S, U11-ch20, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

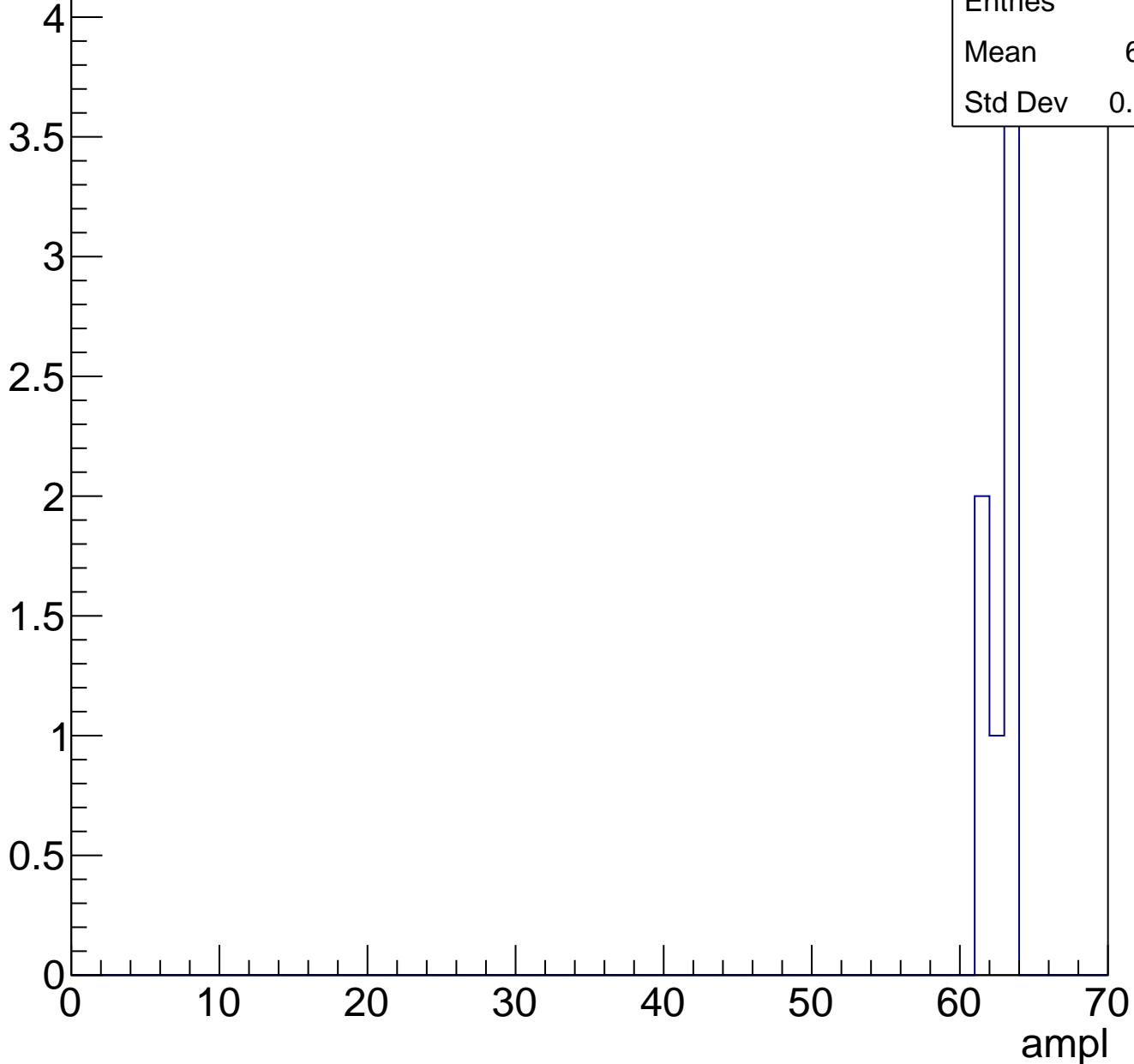
Entries	46
Mean	58.57
Std Dev	9.011



# B1L003S, U11-ch20, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch20, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

0

Mean

0

Std Dev

0

# B1L003S, U11-ch21, adc0

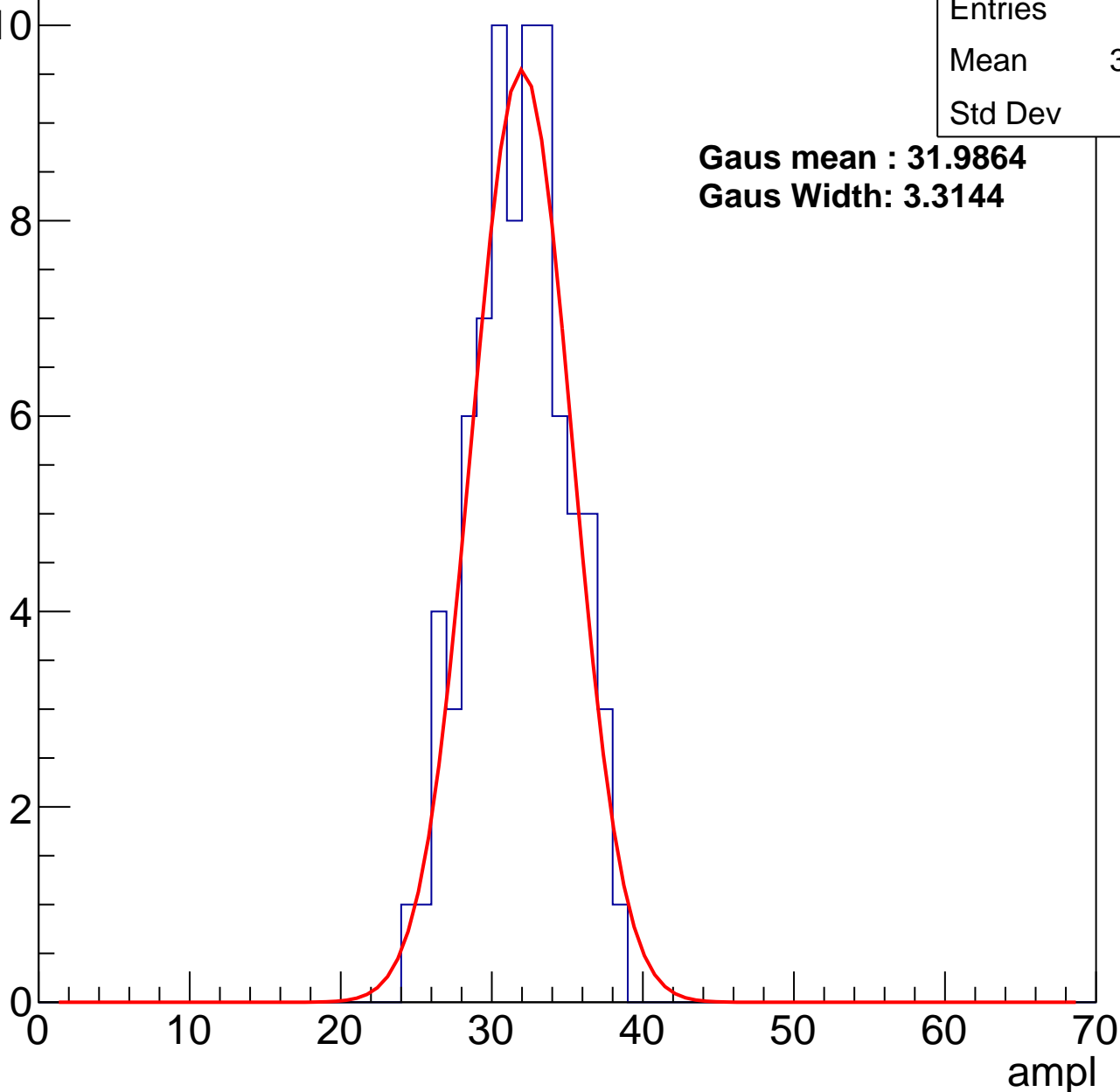
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	80
Mean	31.39
Std Dev	3.12

**Gaus mean : 31.9864**

**Gaus Width: 3.3144**



# B1L003S, U11-ch21, adc1

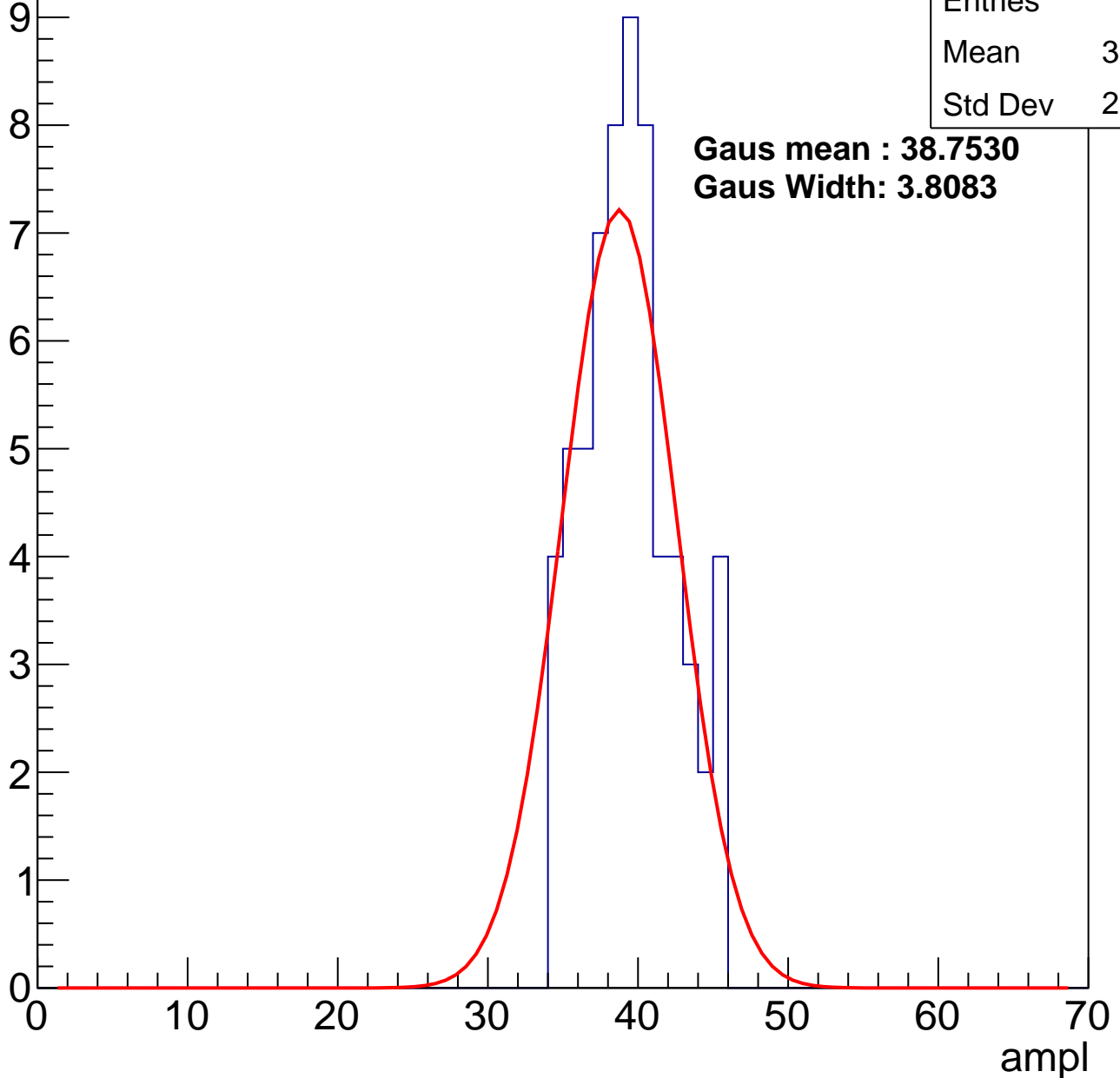
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	38.95
Std Dev	2.989

**Gaus mean : 38.7530**

**Gaus Width: 3.8083**



# B1L003S, U11-ch21, adc2

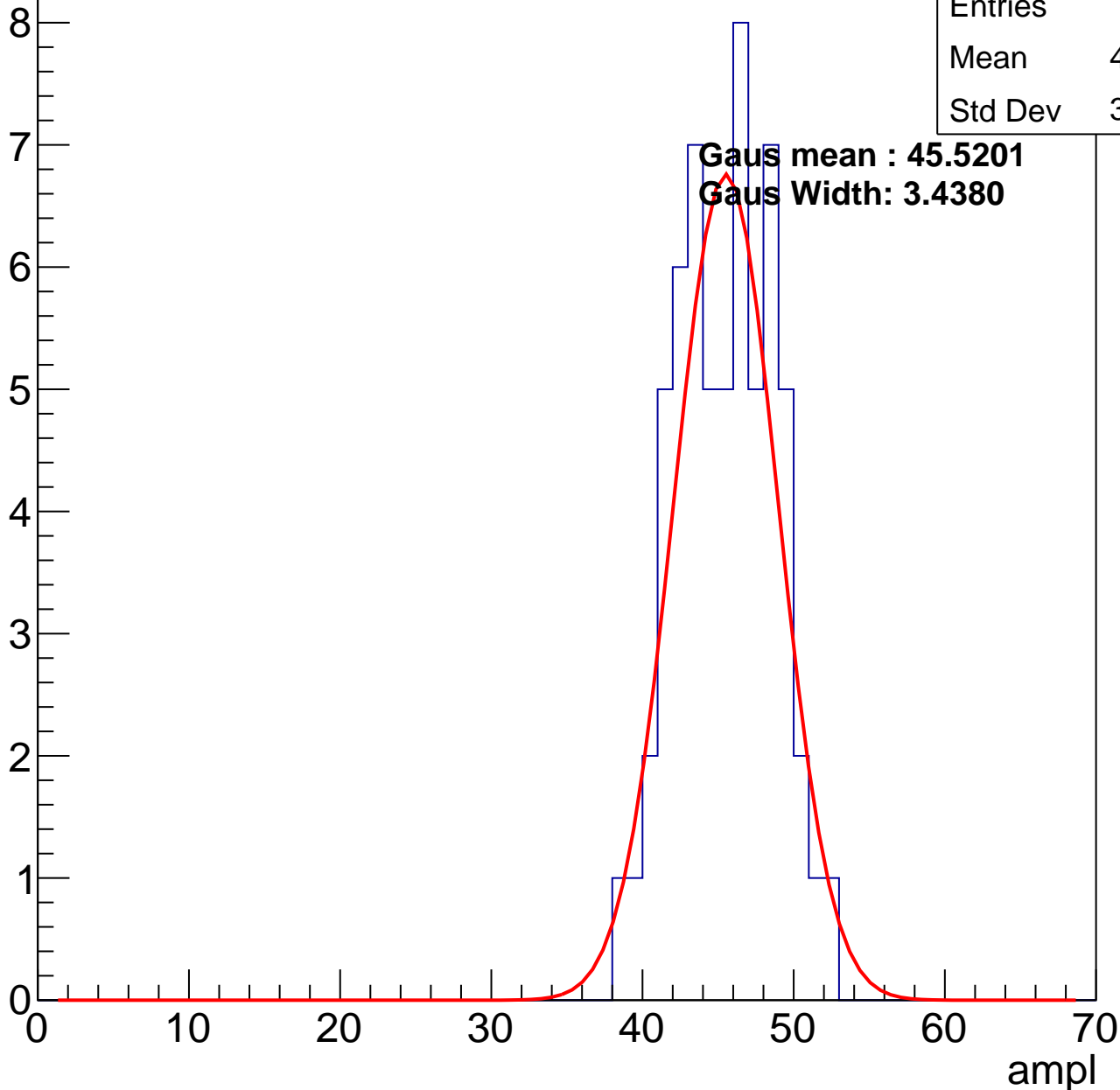
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	45.03
Std Dev	3.157

Gaus mean : 45.5201

Gaus Width: 3.4380

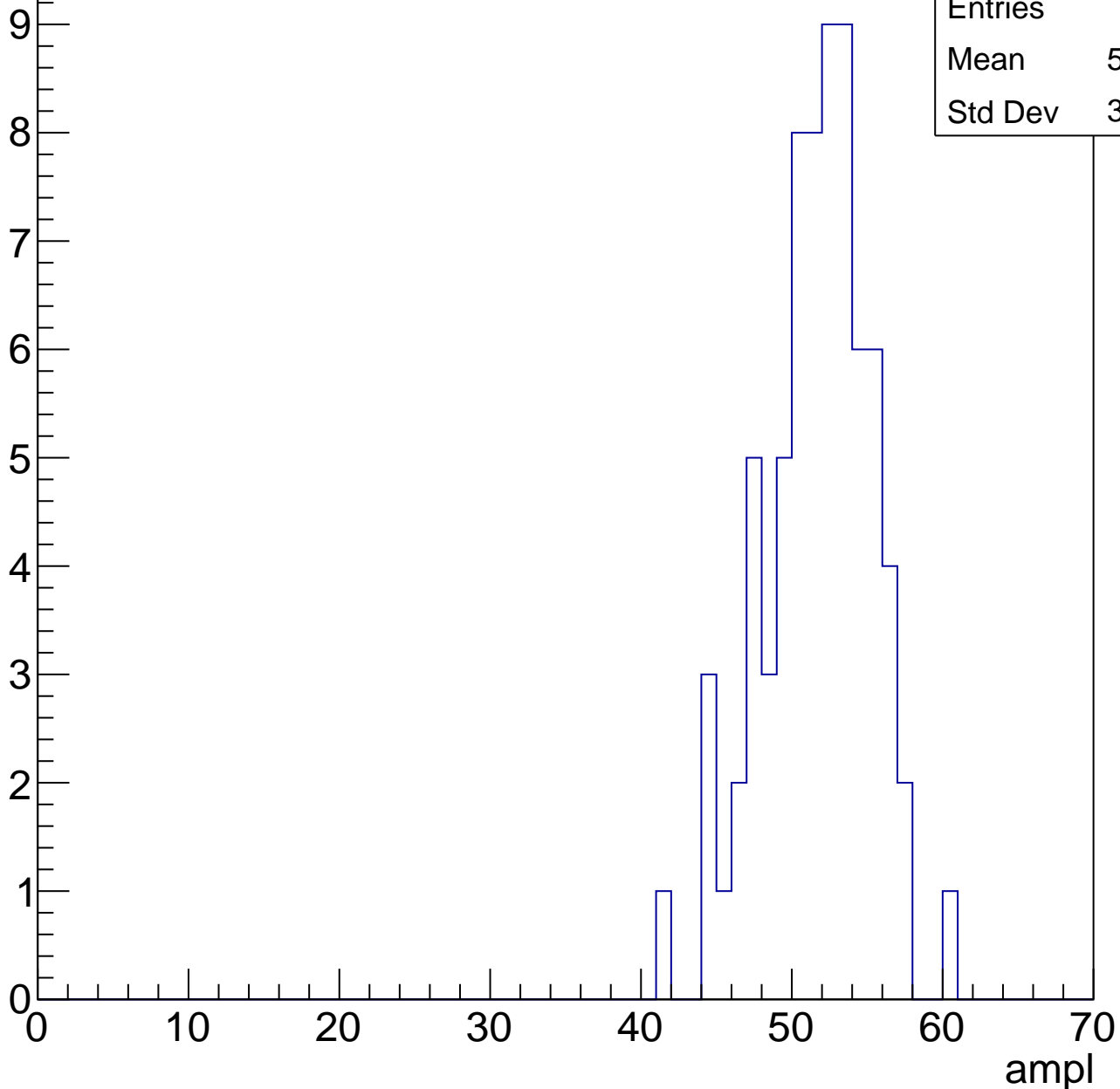


# B1L003S, U11-ch21, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	73
Mean	51.22
Std Dev	3.536

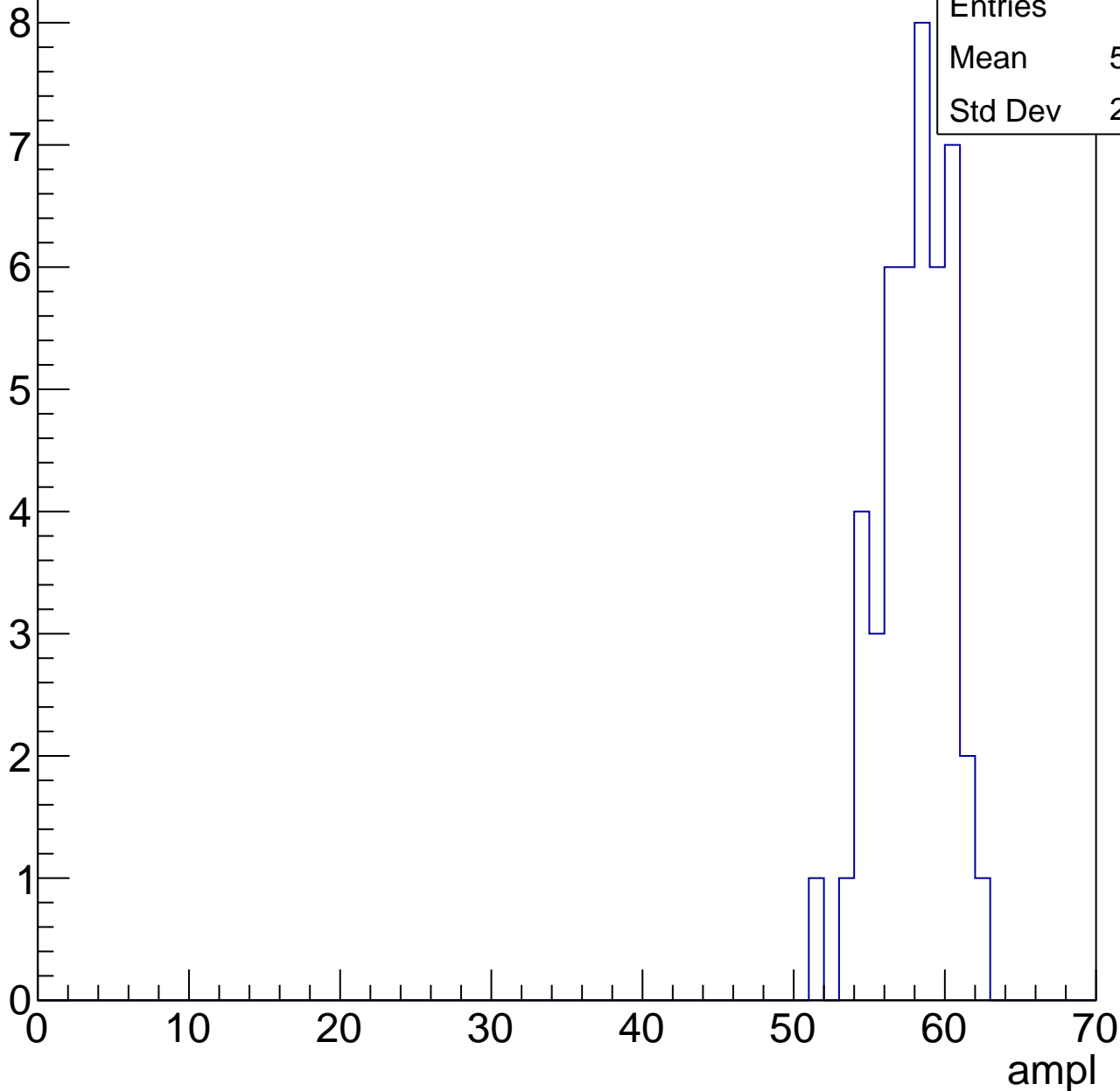


# B1L003S, U11-ch21, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	45
Mean	57.44
Std Dev	2.353

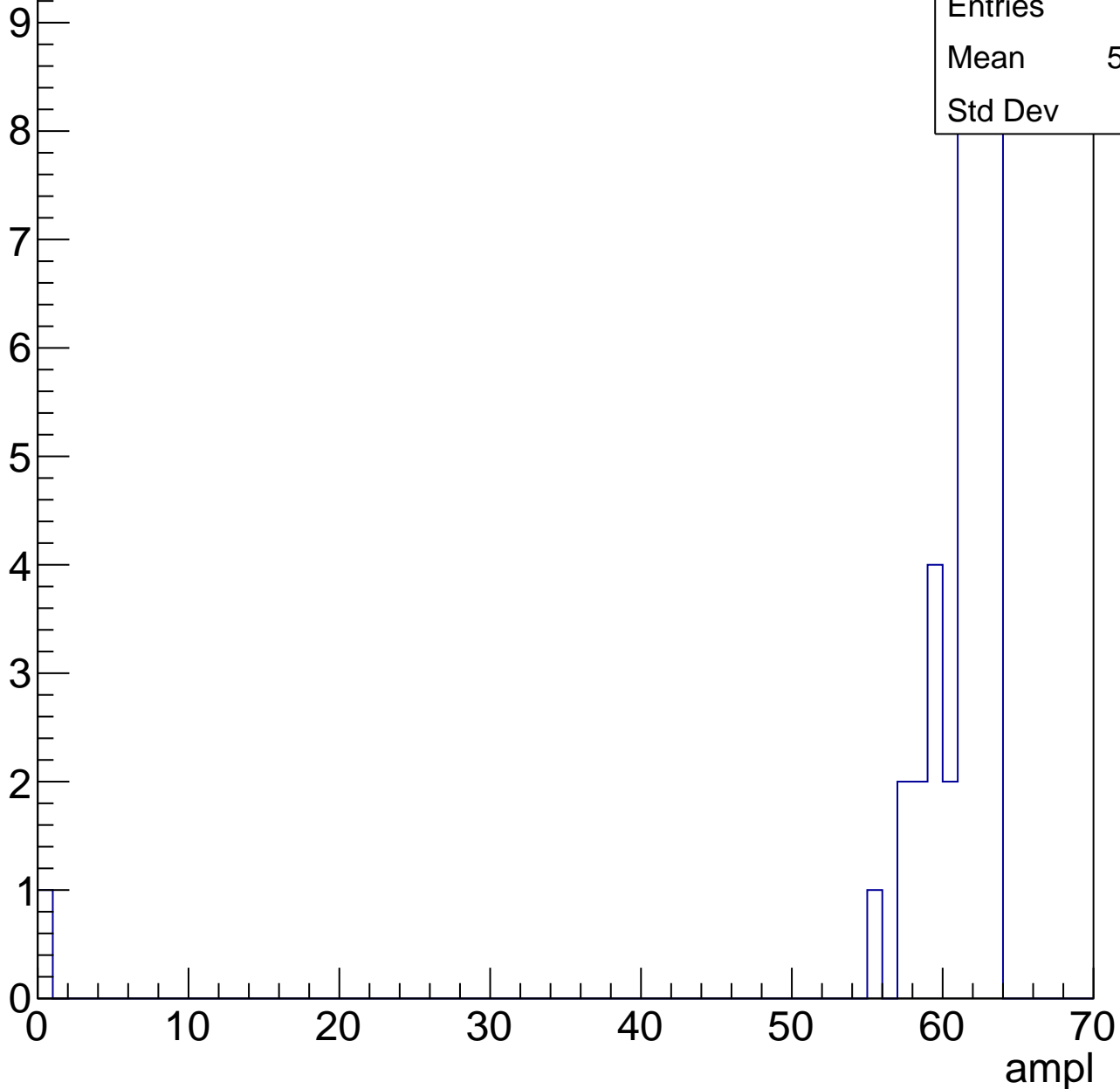


# B1L003S, U11-ch21, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	38
Mean	59.32
Std Dev	9.95



# B1L003S, U11-ch21, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch21, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U11-ch22, adc0

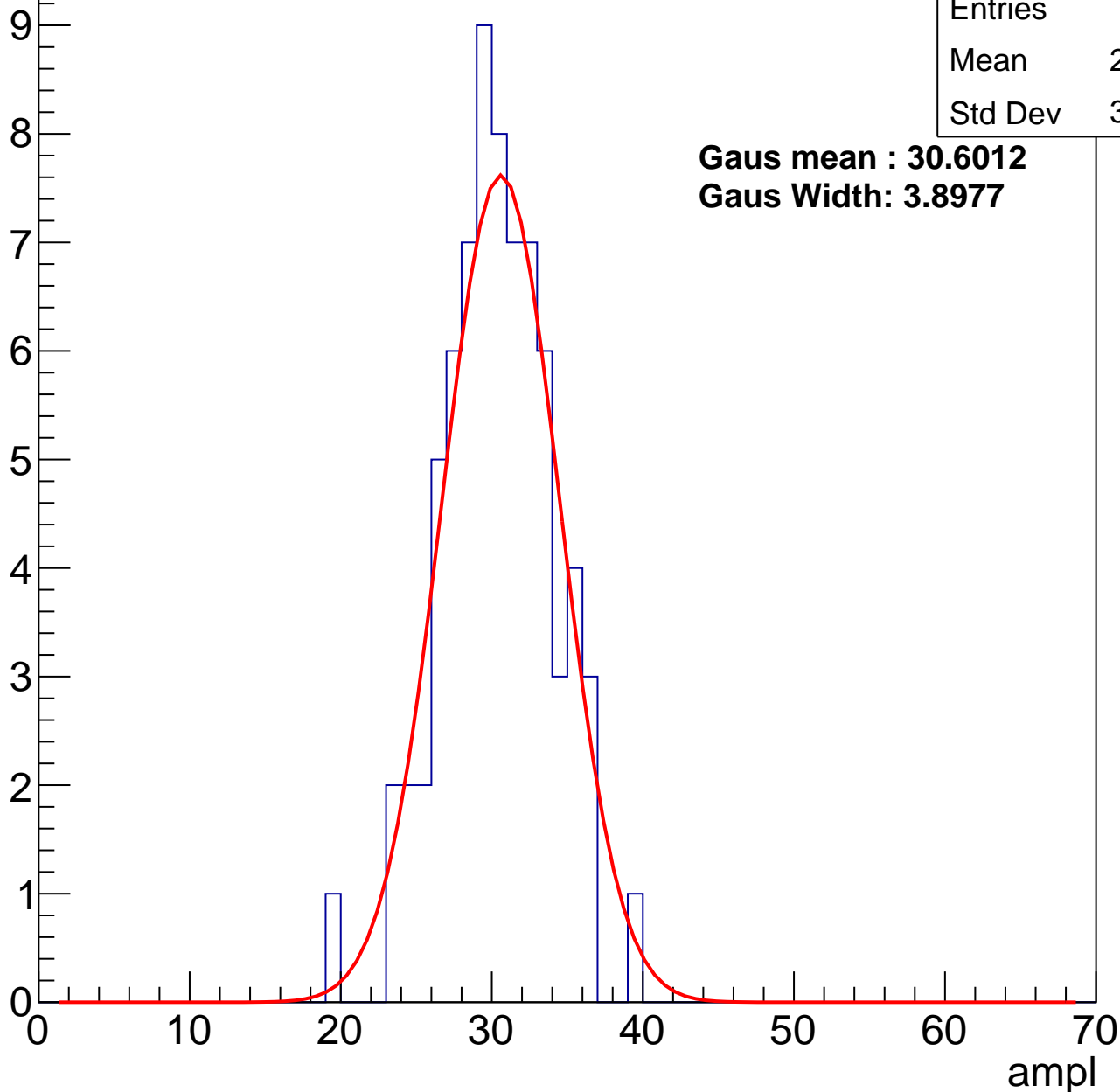
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	73
Mean	29.86
Std Dev	3.582

**Gaus mean : 30.6012**

**Gaus Width: 3.8977**



# B1L003S, U11-ch22, adc1

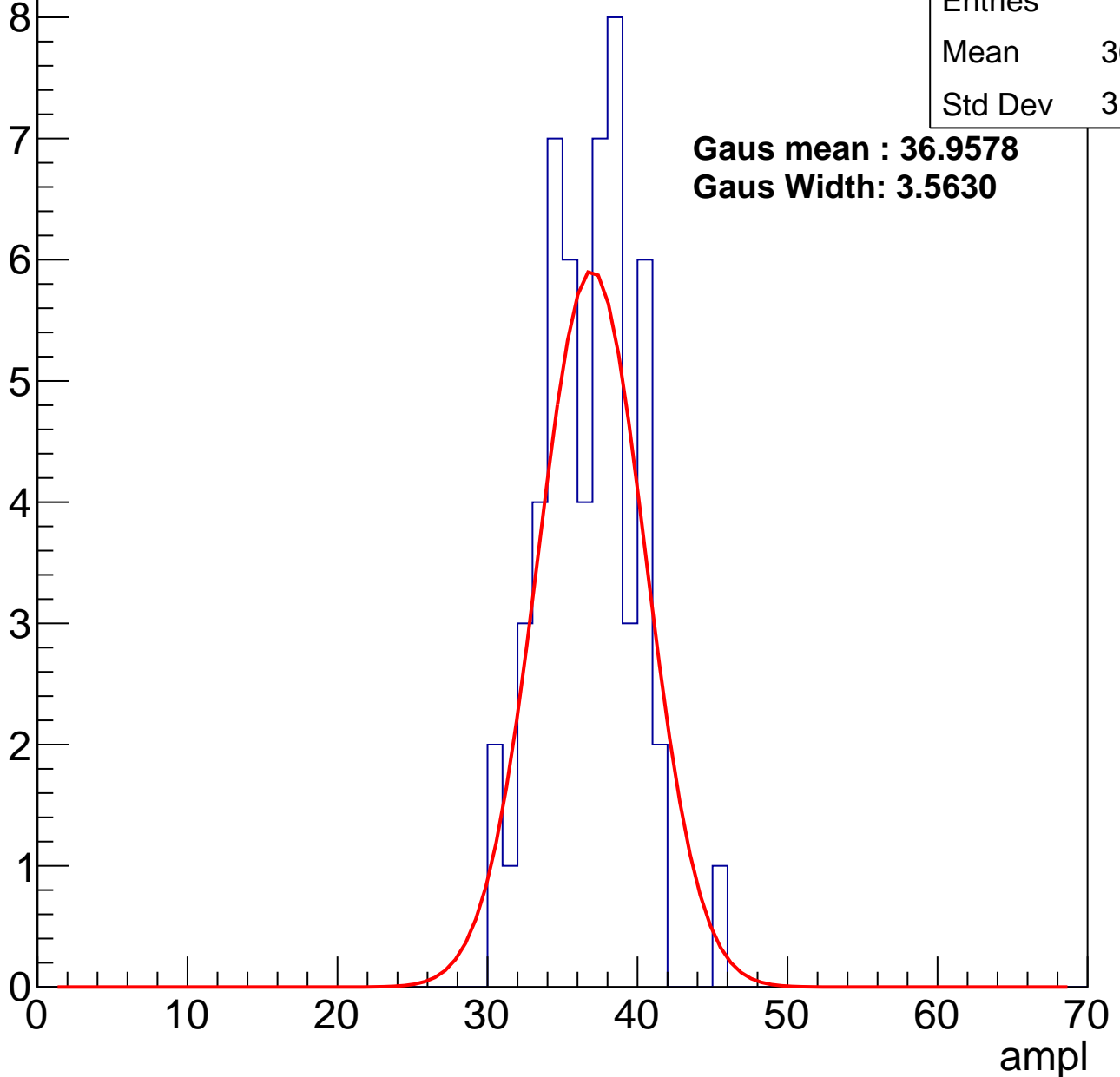
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	54
Mean	36.26
Std Dev	3.056

**Gaus mean : 36.9578**

**Gaus Width: 3.5630**



# B1L003S, U11-ch22, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	71
Mean	42.38
Std Dev	3.087

**Gaus mean : 43.1029**

**Gaus Width: 3.2882**

10

8

6

4

2

0

0

10

20

30

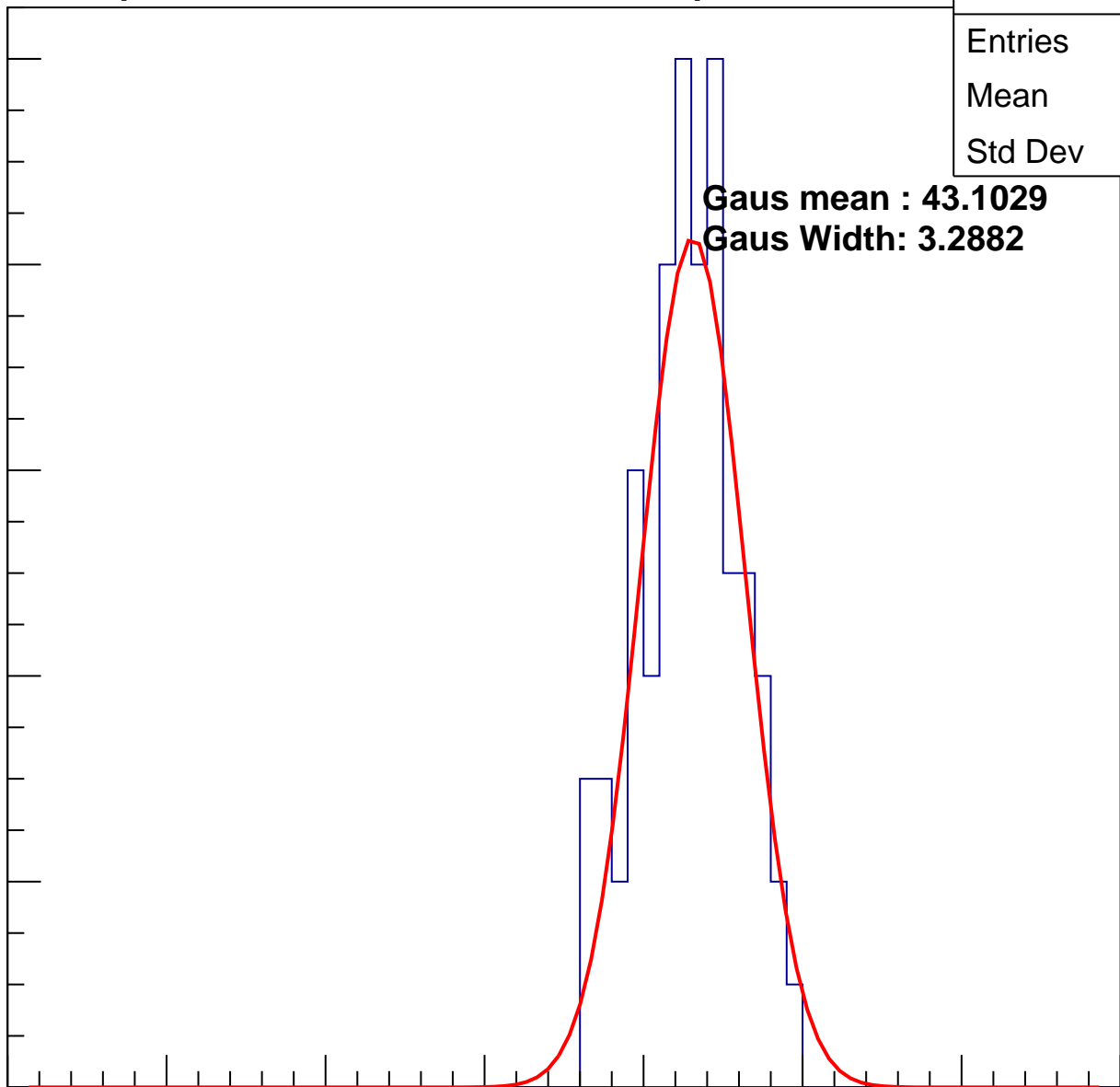
40

50

60

70

ampl

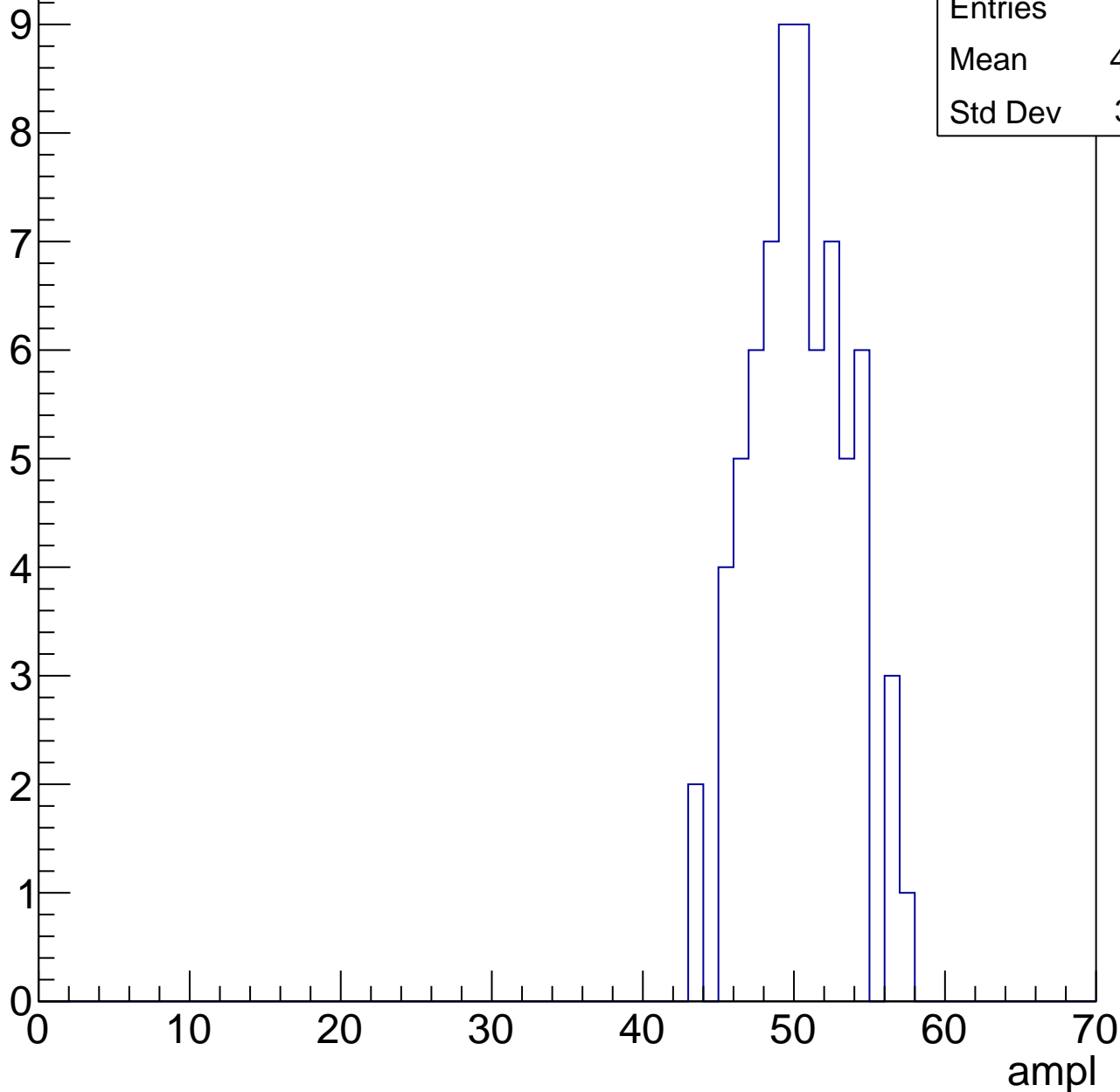


# B1L003S, U11-ch22, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

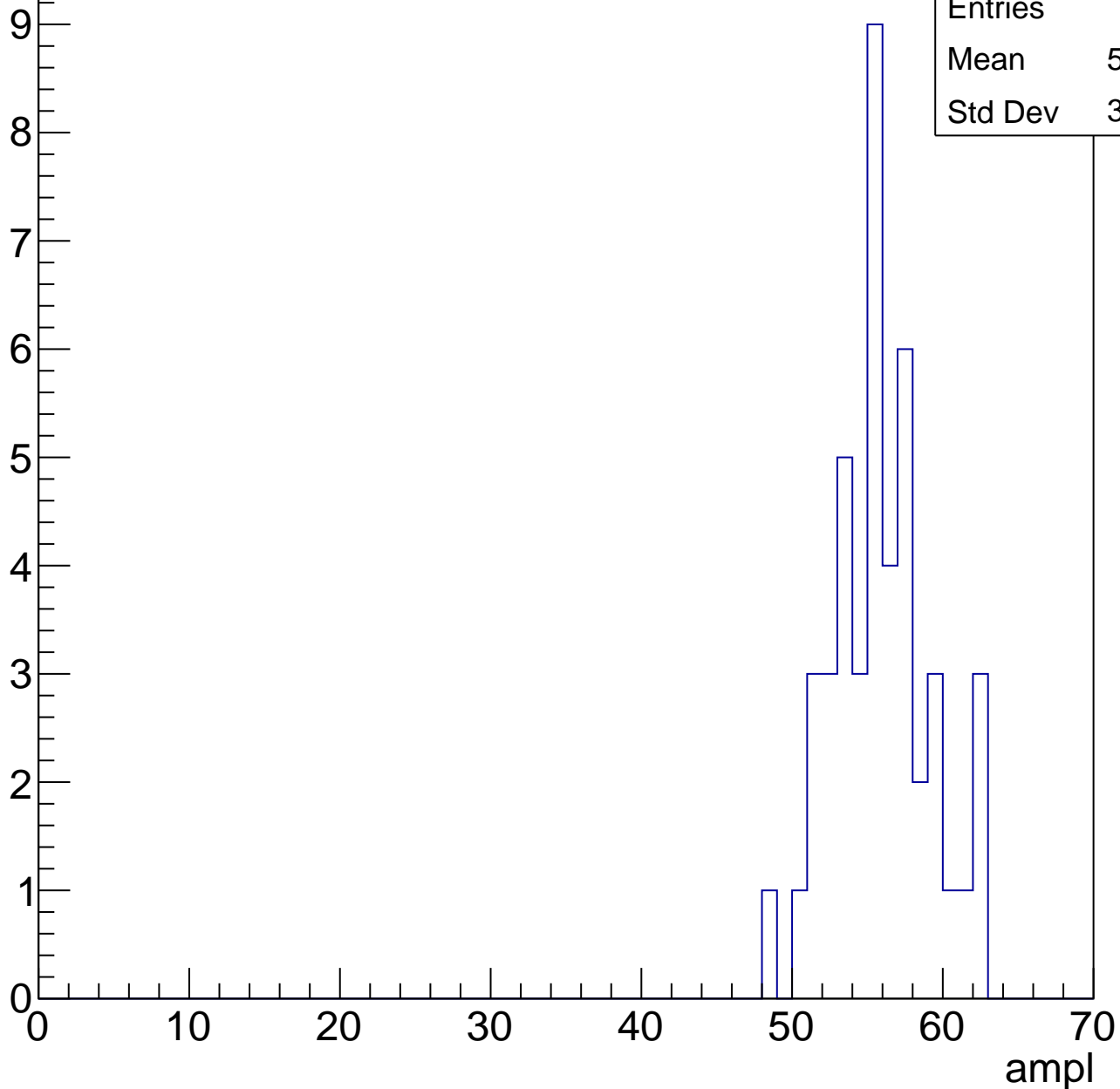
Entries	70
Mean	49.84
Std Dev	3.161



# B1L003S, U11-ch22, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

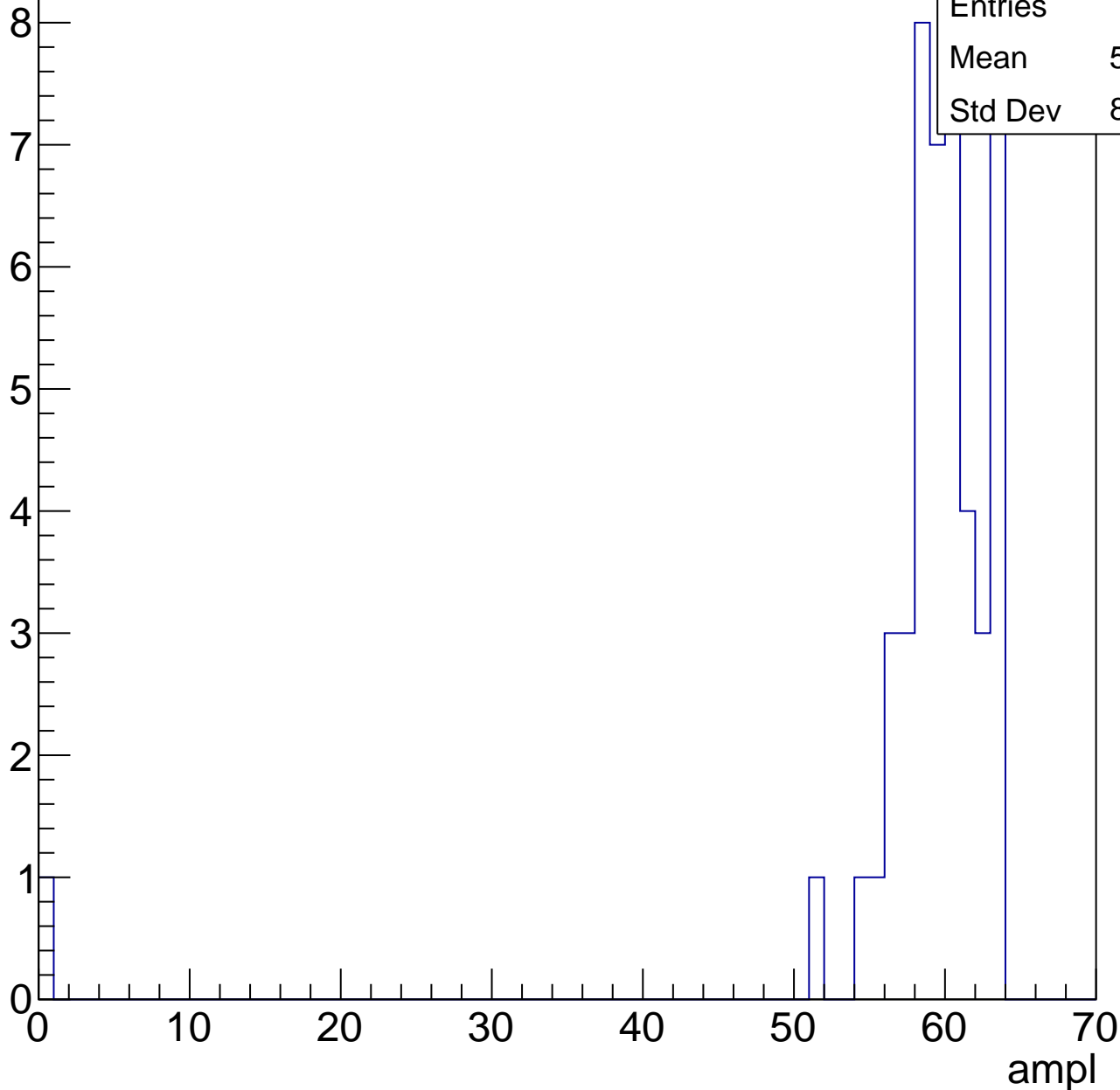


# B1L003S, U11-ch22, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

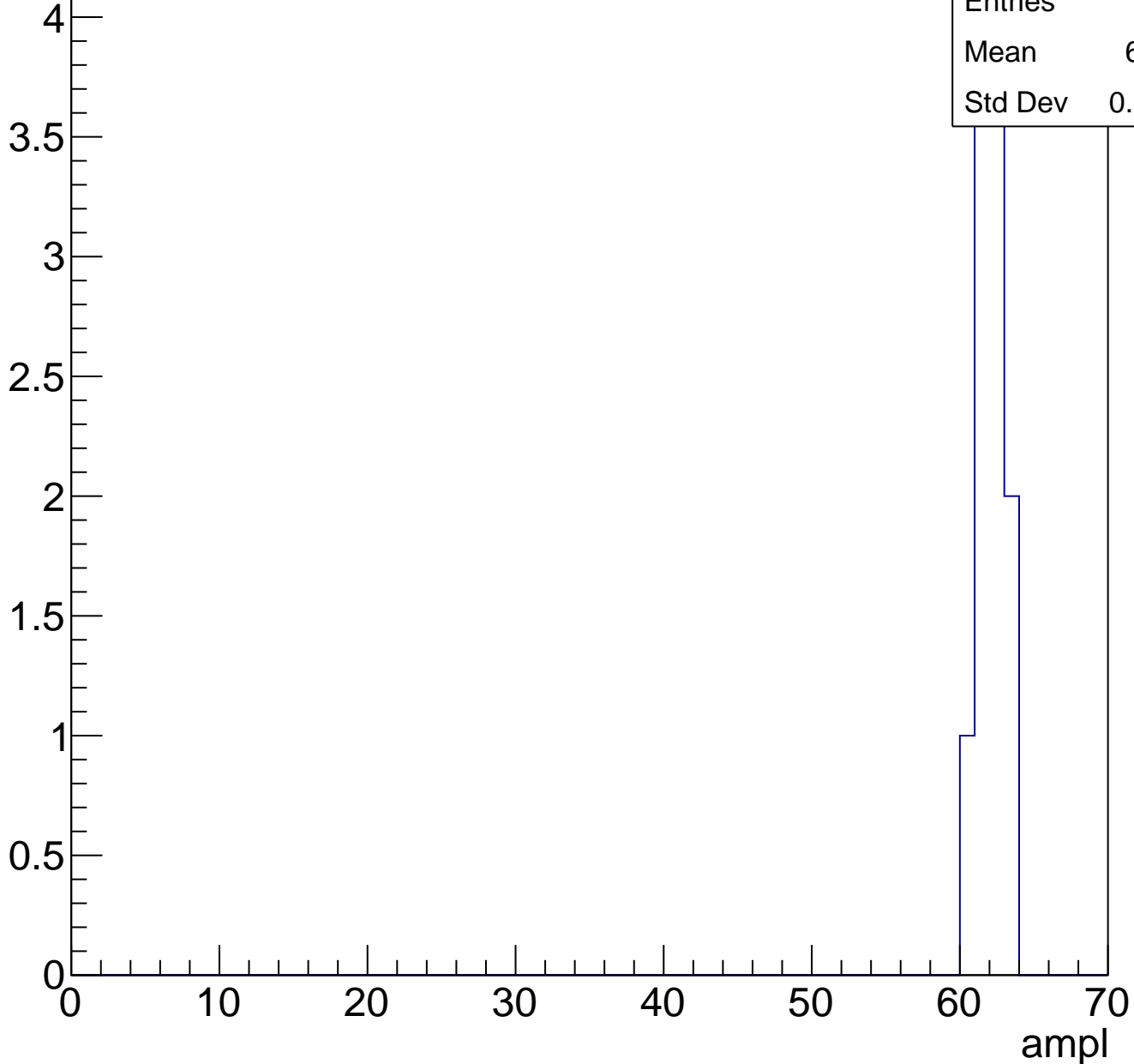
Entries	48
Mean	58.12
Std Dev	8.869



# B1L003S, U11-ch22, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



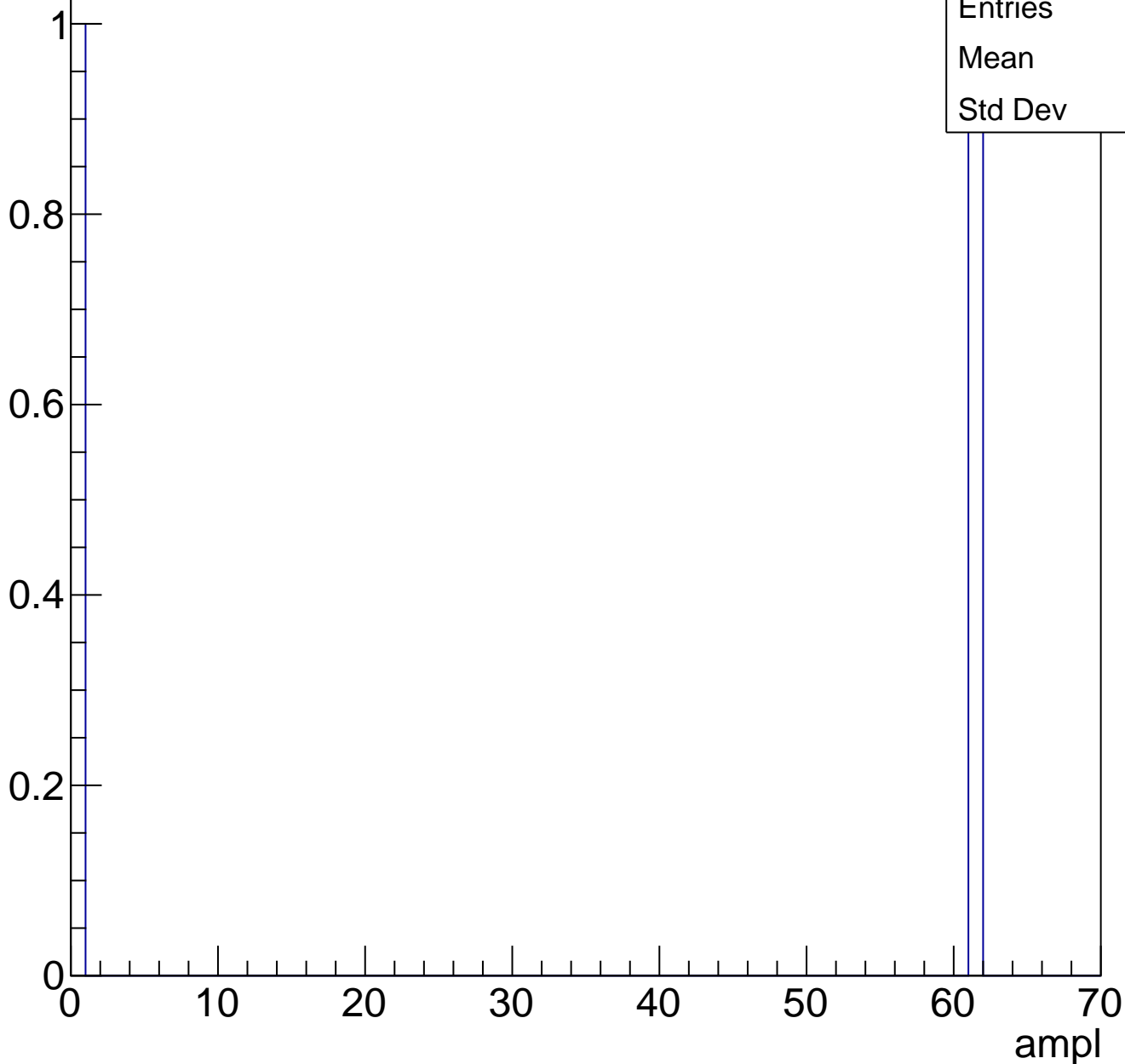
Entries	11
Mean	61.64
Std Dev	0.8814



# B1L003S, U11-ch22, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U11-ch23, adc0

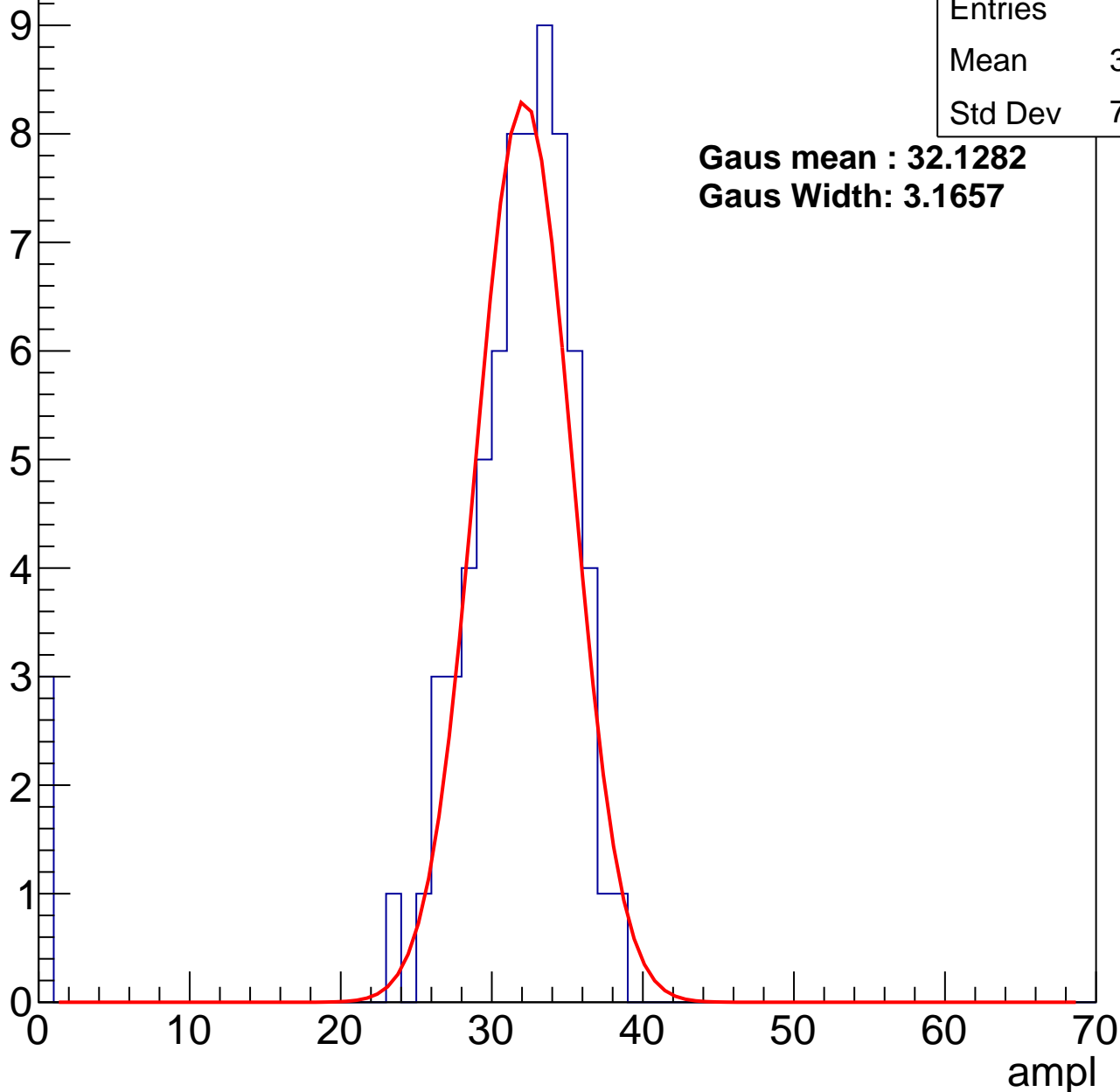
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	71
Mean	30.23
Std Dev	7.044

**Gaus mean : 32.1282**

**Gaus Width: 3.1657**



# B1L003S, U11-ch23, adc1

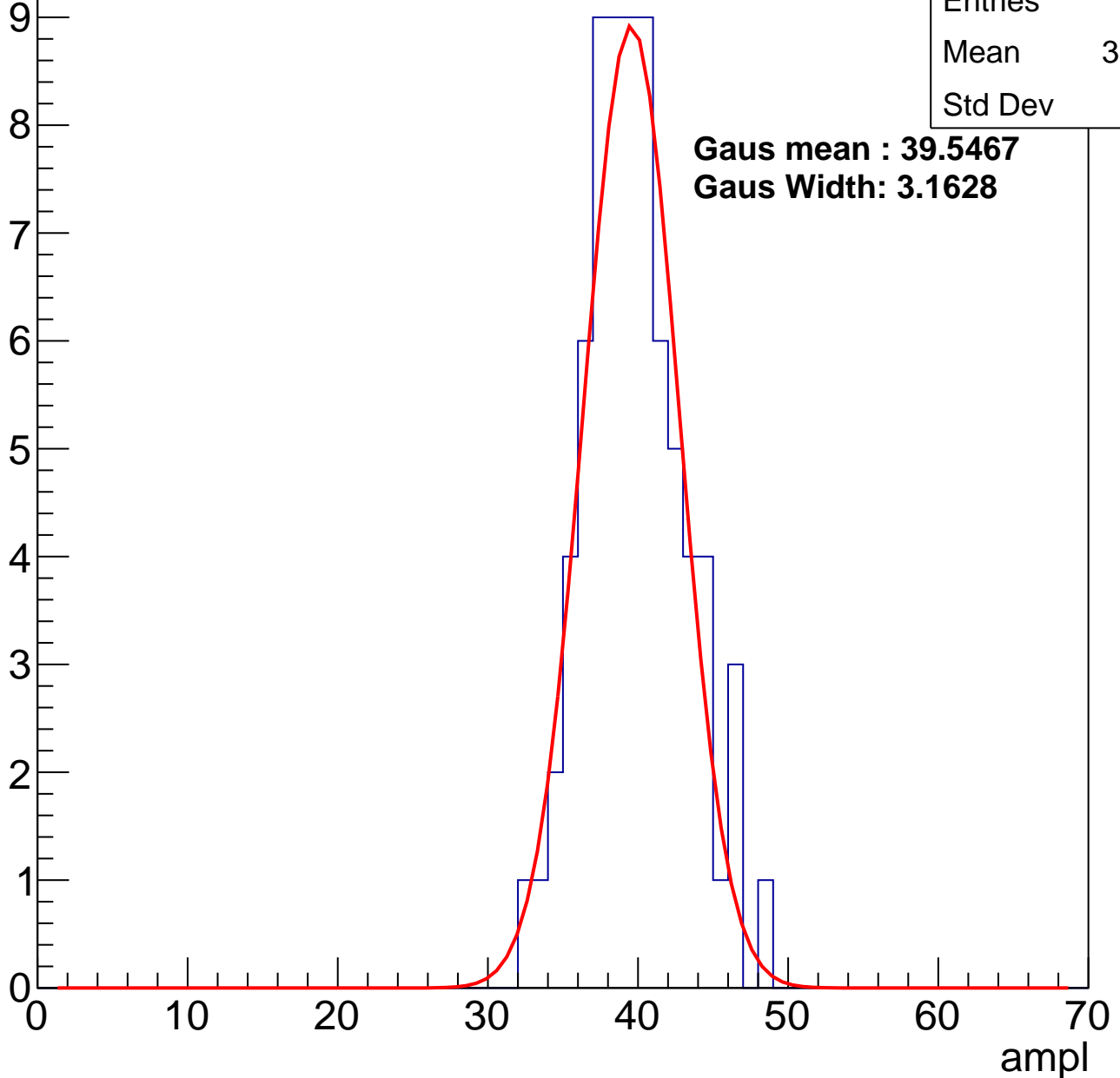
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	74
Mean	39.32
Std Dev	3.28

**Gaus mean : 39.5467**

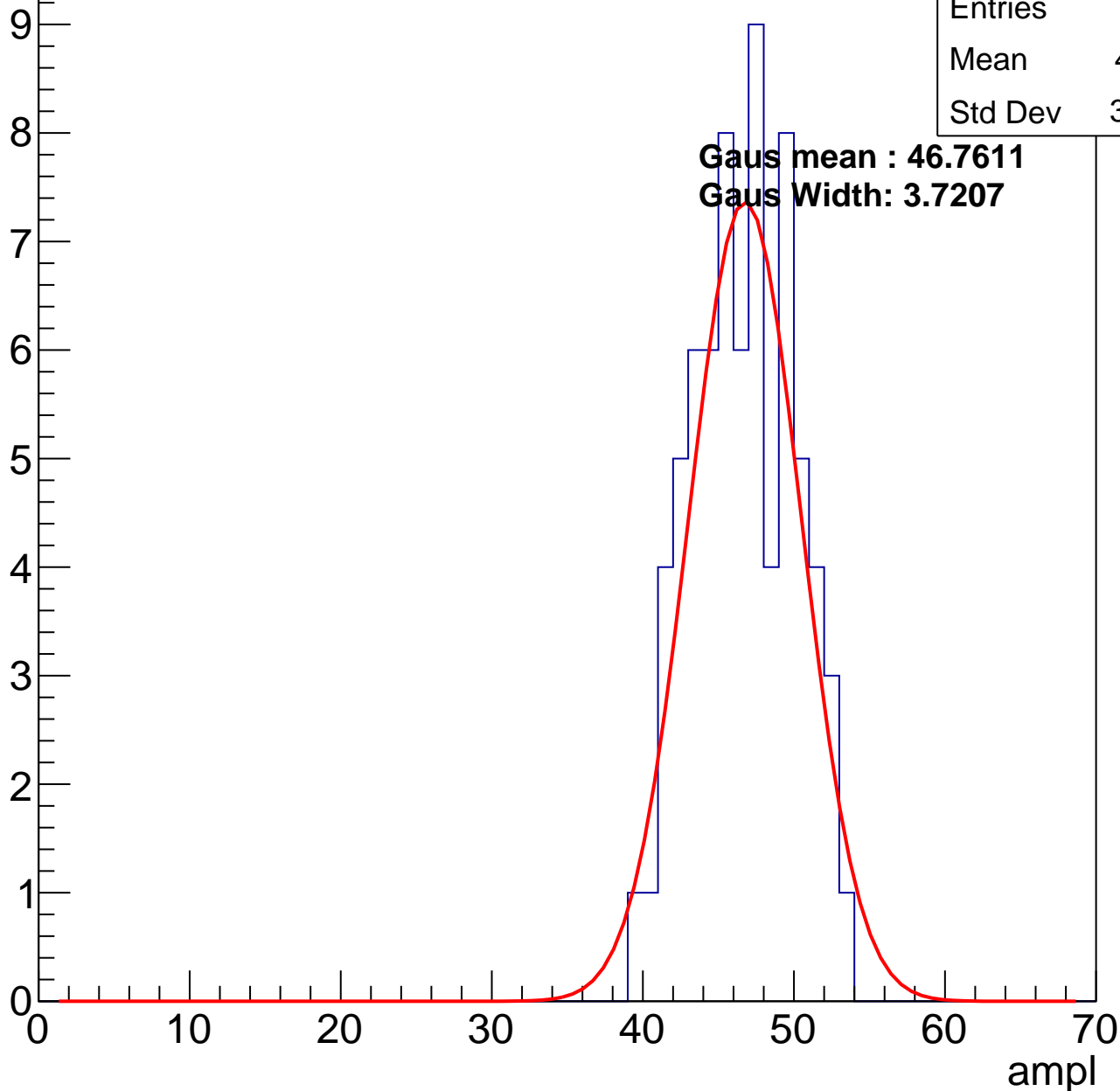
**Gaus Width: 3.1628**



# B1L003S, U11-ch23, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

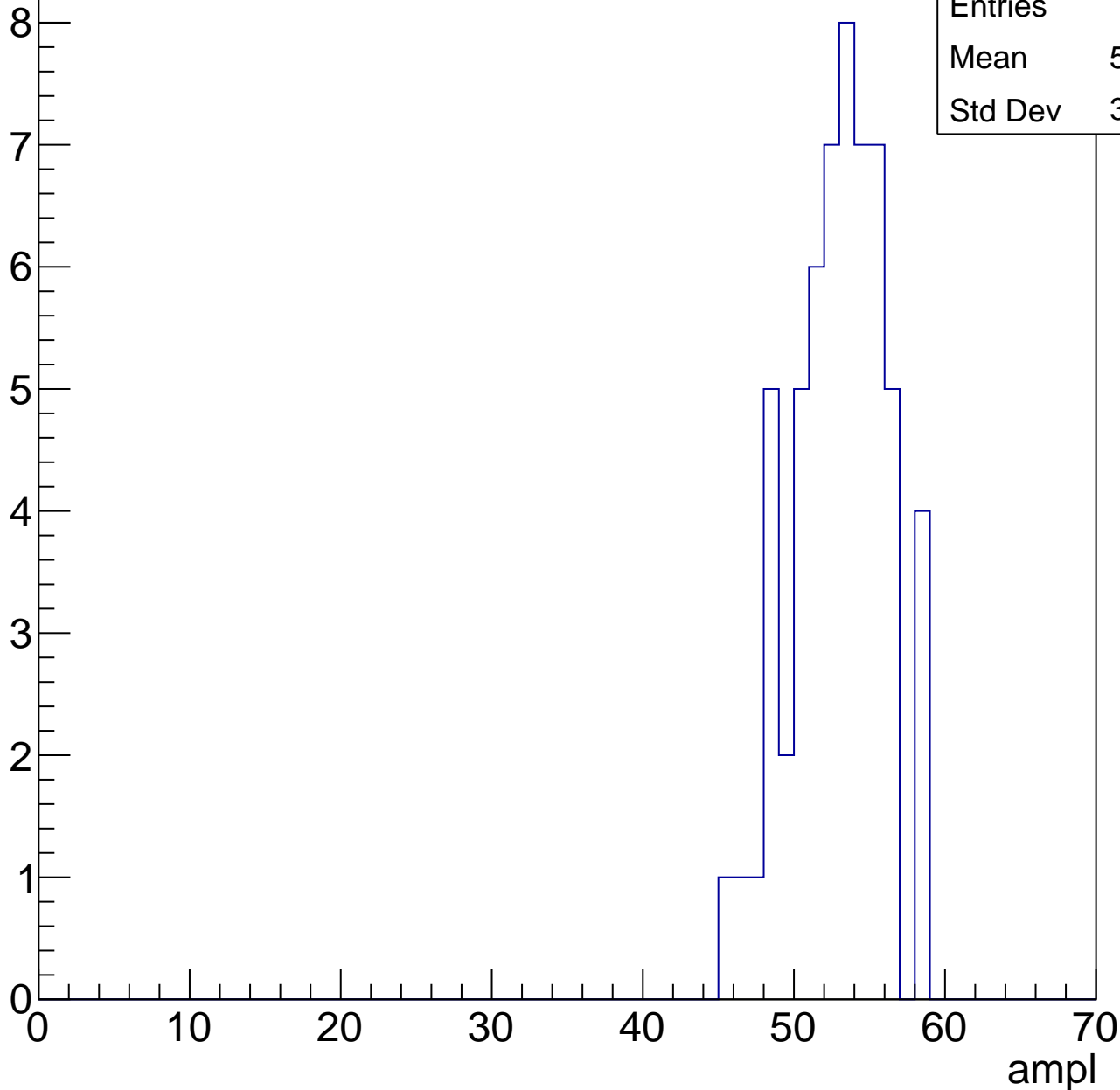


Entries	71
Mean	46.21
Std Dev	3.318

# B1L003S, U11-ch23, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U11-ch23, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

10

Entries 51

Mean 58.29

Std Dev 2.312

8

6

4

2

0

0

10

20

30

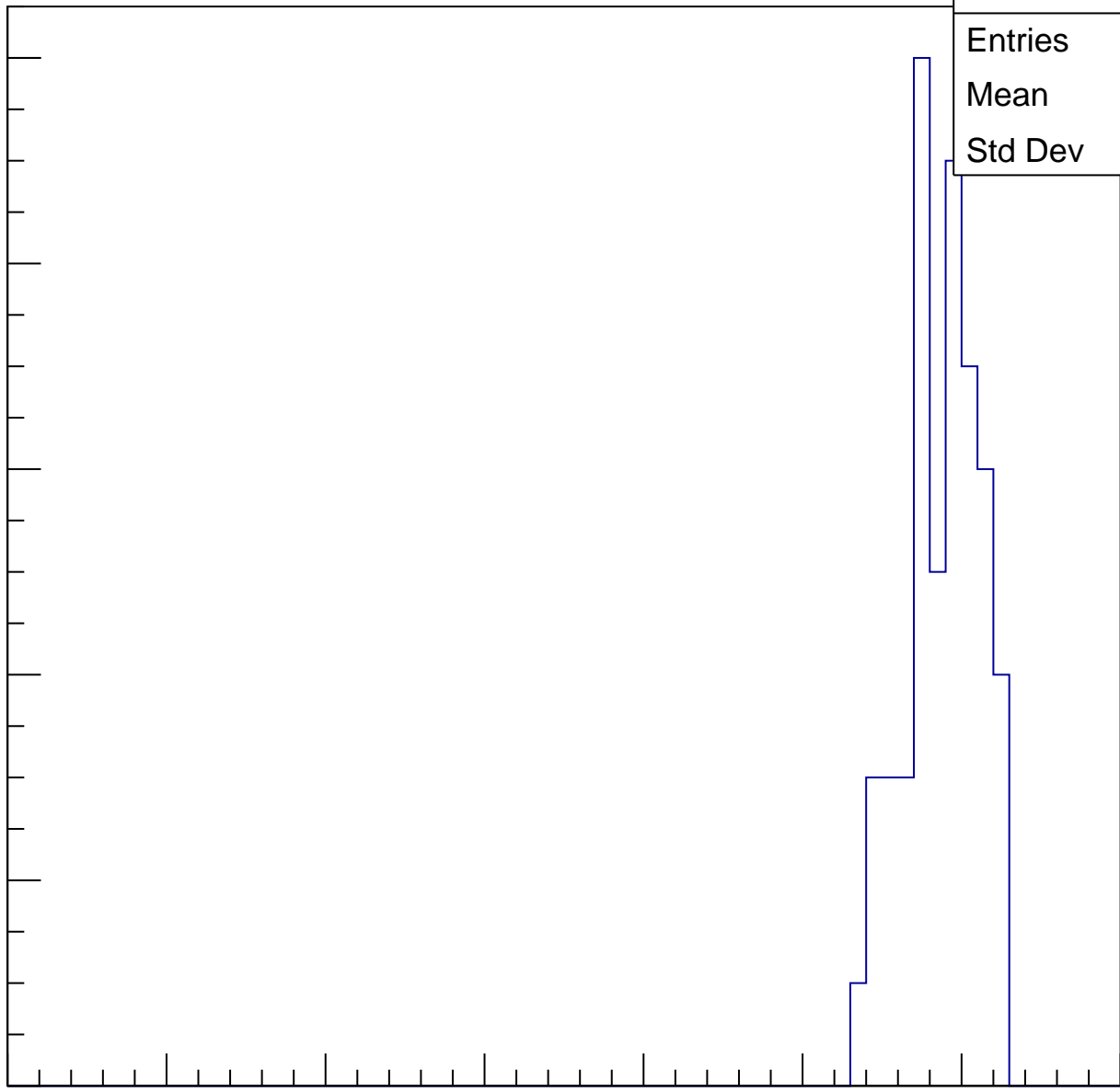
40

50

60

ampl

70

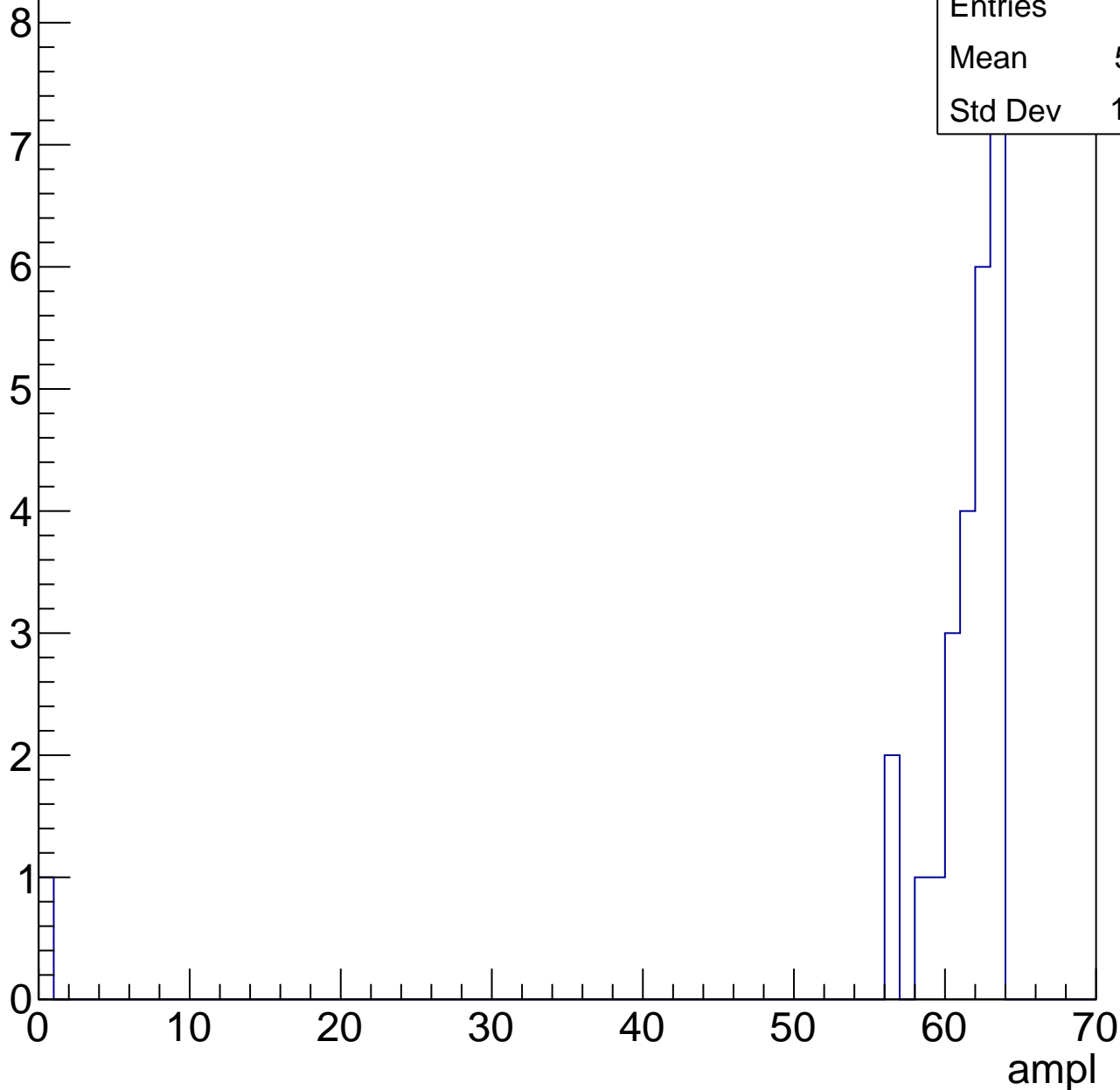


# B1L003S, U11-ch23, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	26
Mean	58.81
Std Dev	11.93



# B1L003S, U11-ch23, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch23, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U11-ch24, adc0

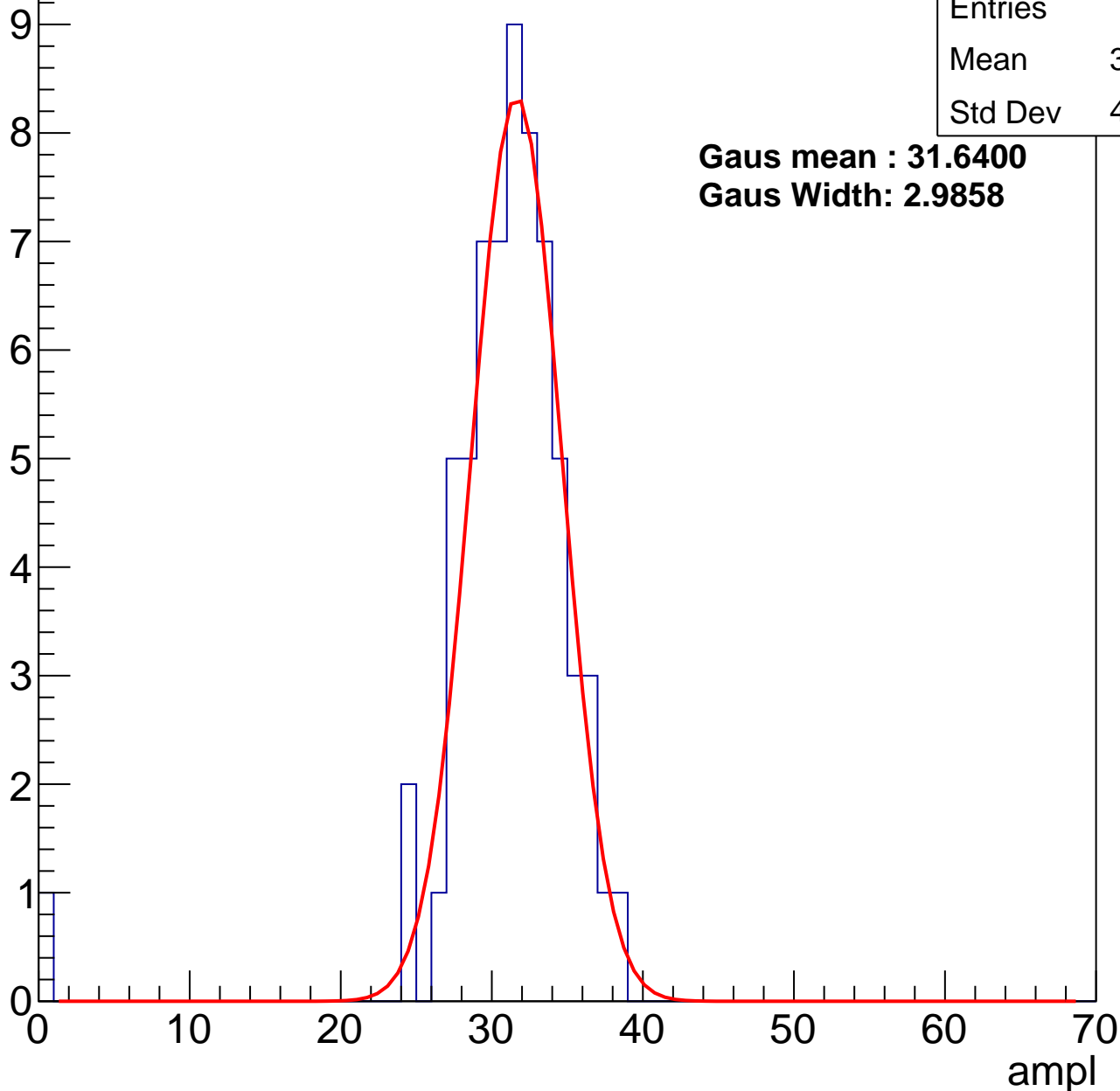
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	30.55
Std Dev	4.836

**Gaus mean : 31.6400**

**Gaus Width: 2.9858**



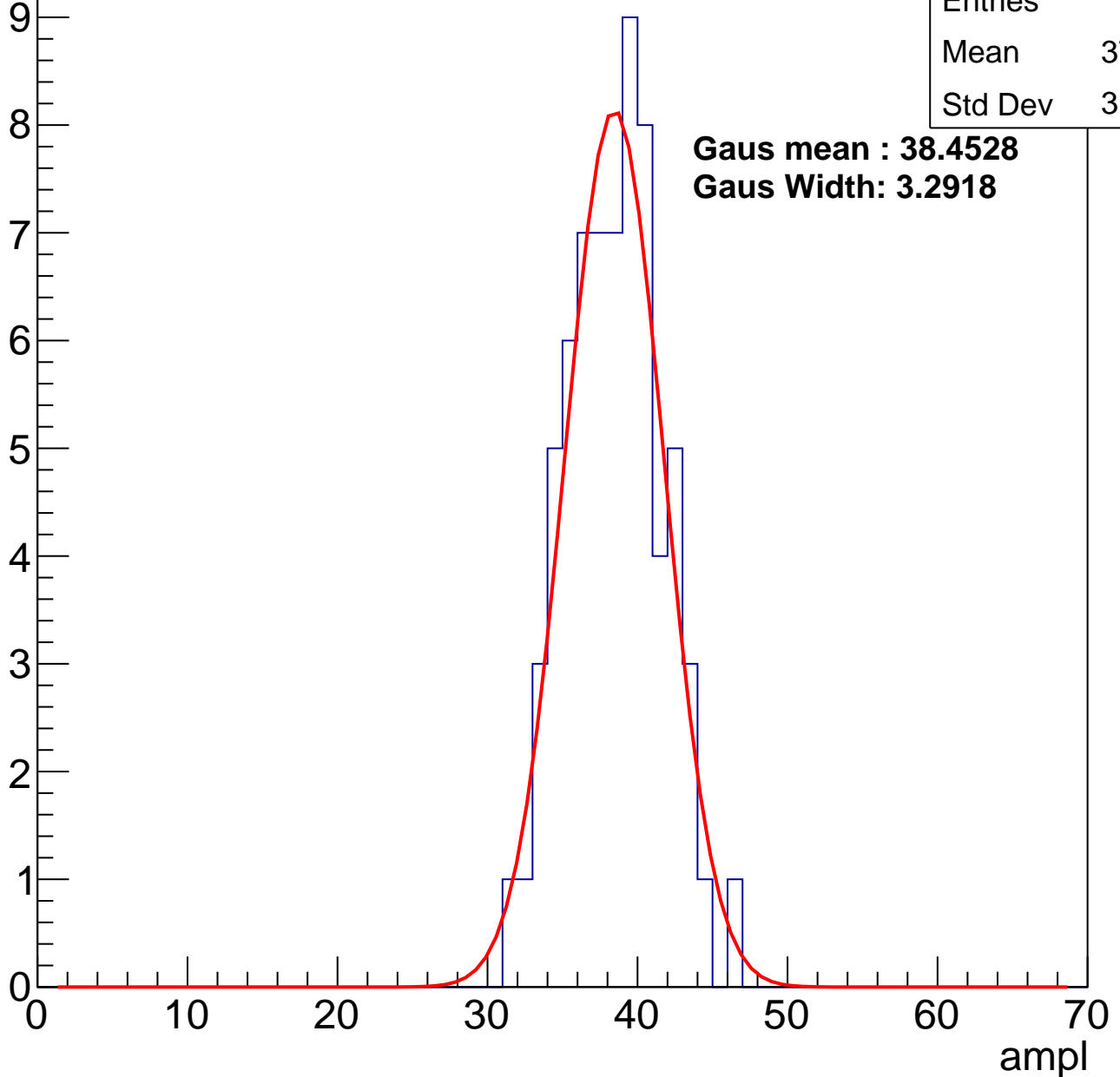
# B1L003S, U11-ch24, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	37.99
Std Dev	3.118

**Gaus mean : 38.4528**  
**Gaus Width: 3.2918**



# B1L003S, U11-ch24, adc2

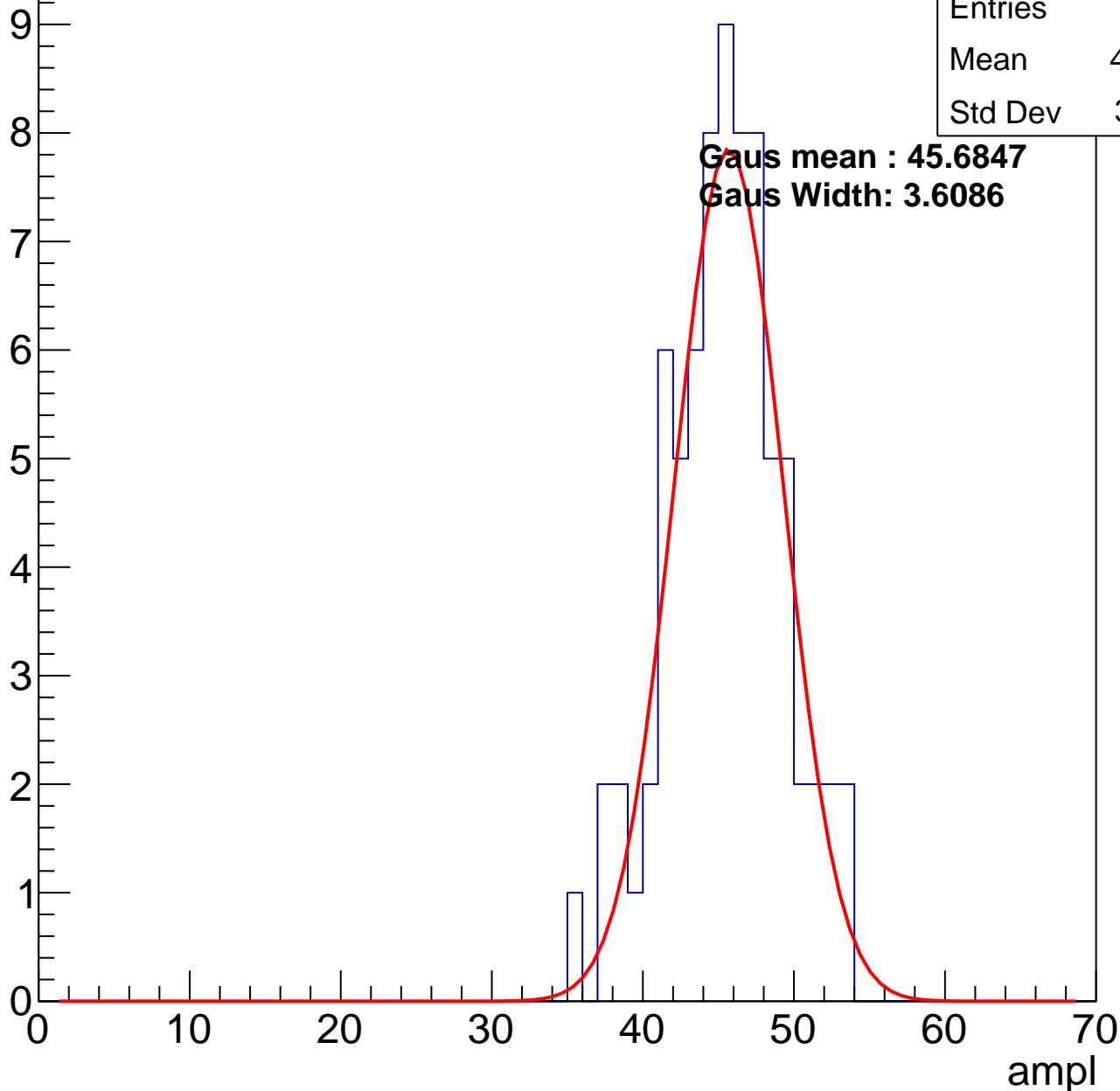
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	76
Mean	44.95
Std Dev	3.801

**Gaus mean : 45.6847**

**Gaus Width: 3.6086**

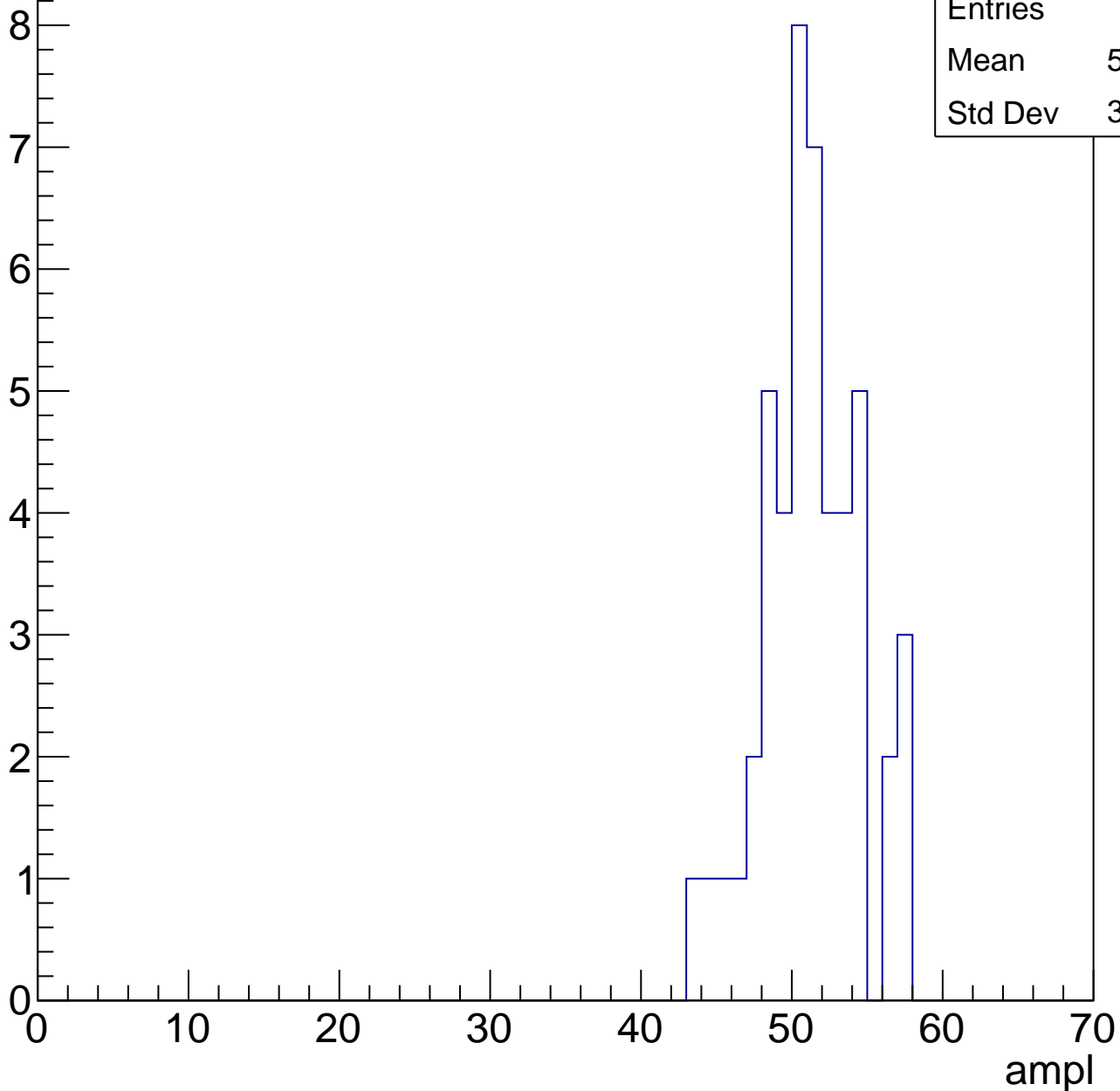


# B1L003S, U11-ch24, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

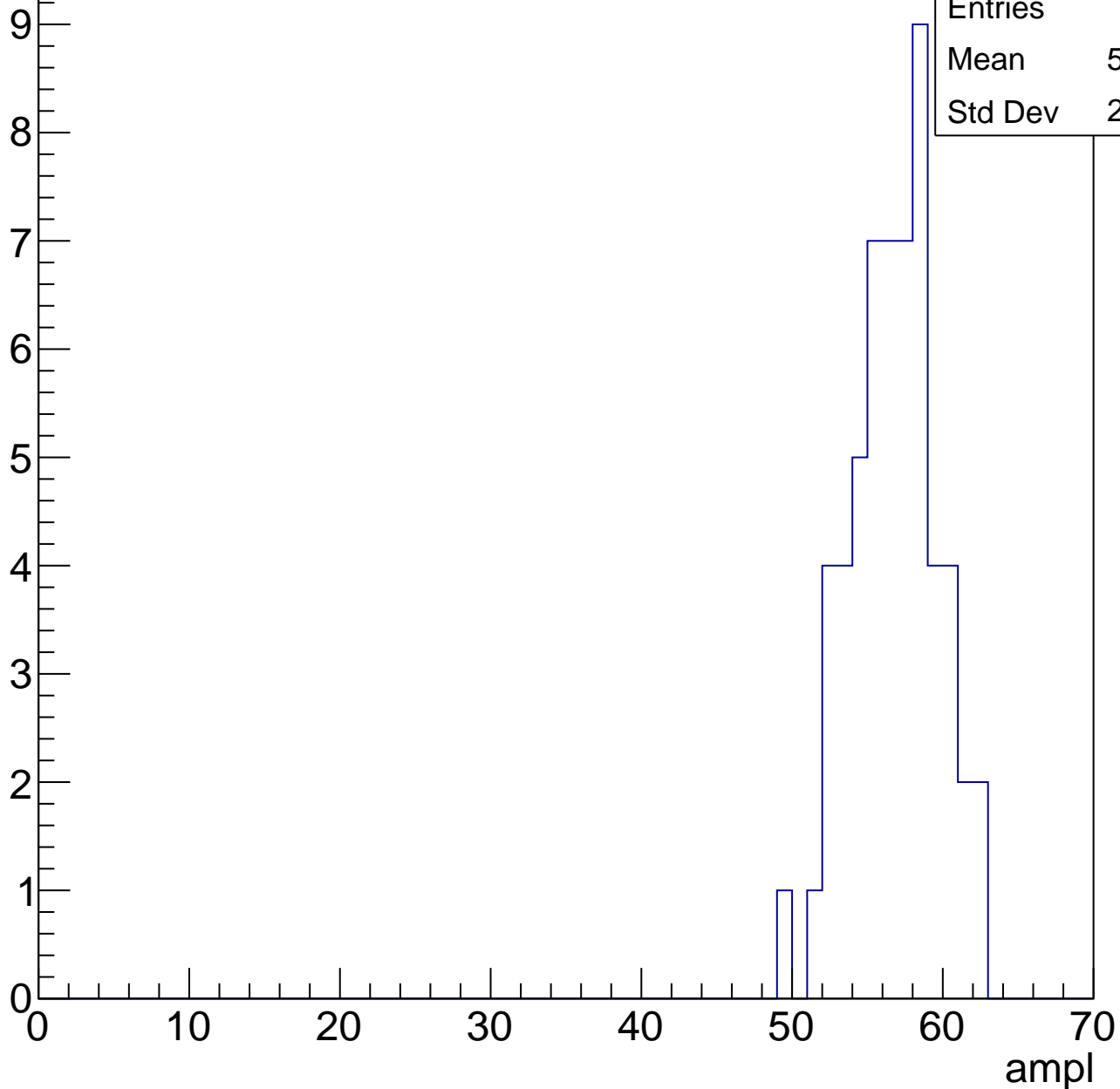
Entries	48
Mean	50.79
Std Dev	3.214



# B1L003S, U11-ch24, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

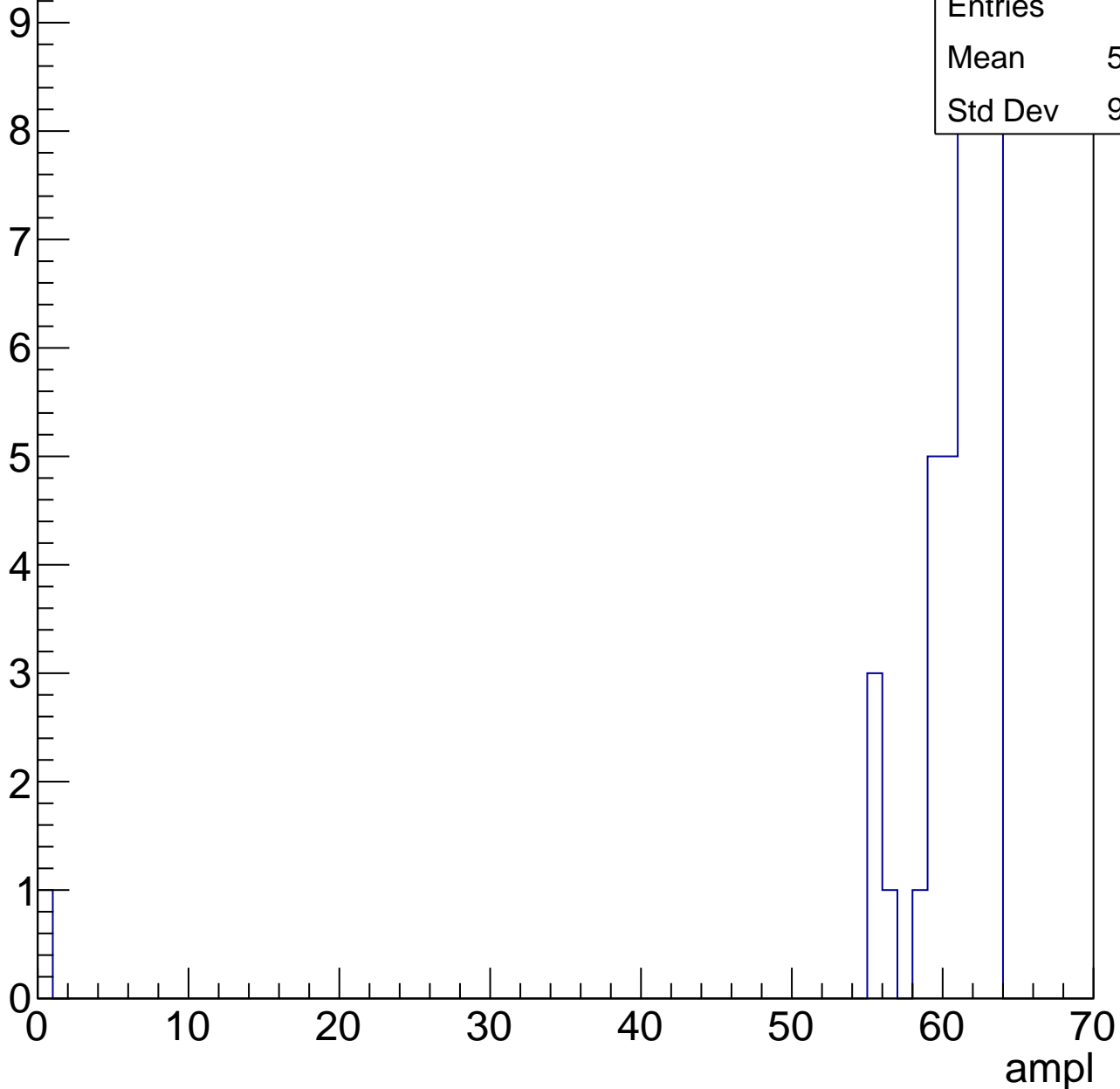


# B1L003S, U11-ch24, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	41
Mean	59.15
Std Dev	9.616



# B1L003S, U11-ch24, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

3

Mean

60.67

Std Dev

1.7



# B1L003S, U11-ch24, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U11-ch25, adc0

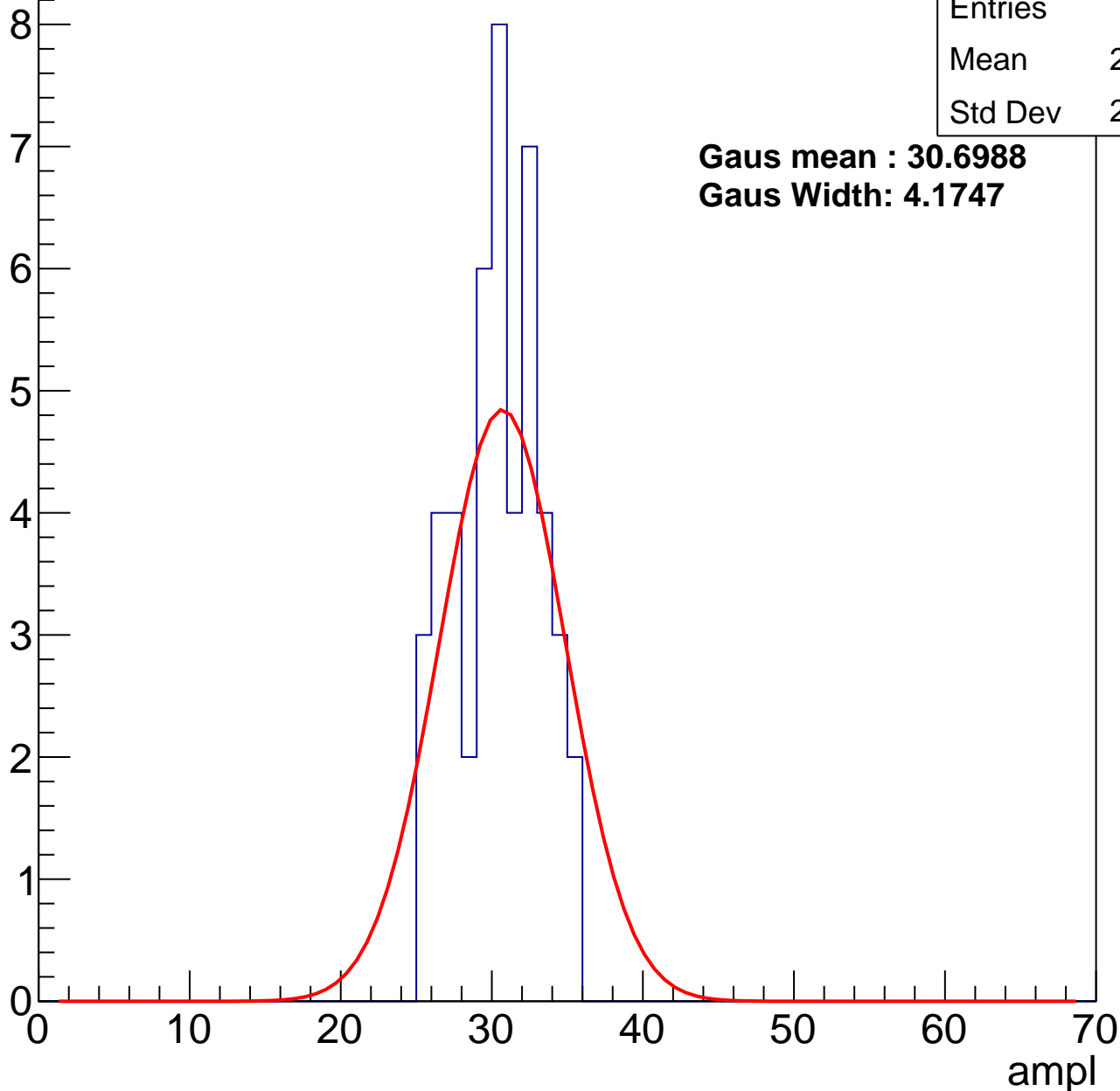
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	47
Mean	29.98
Std Dev	2.748

**Gaus mean : 30.6988**

**Gaus Width: 4.1747**



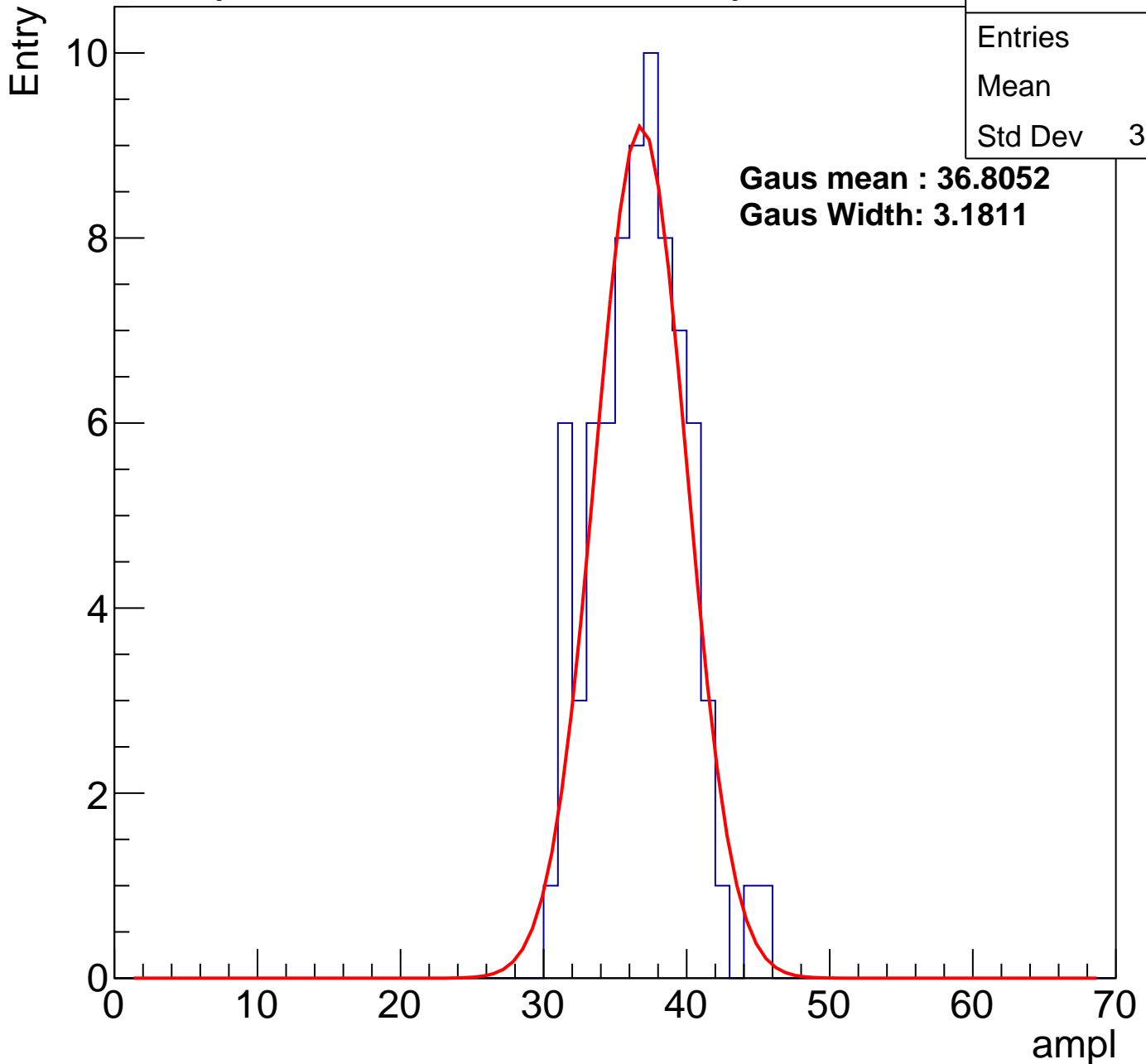
# B1L003S, U11-ch25, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	76
Mean	36.3
Std Dev	3.183

**Gaus mean : 36.8052**

**Gaus Width: 3.1811**



# B1L003S, U11-ch25, adc2

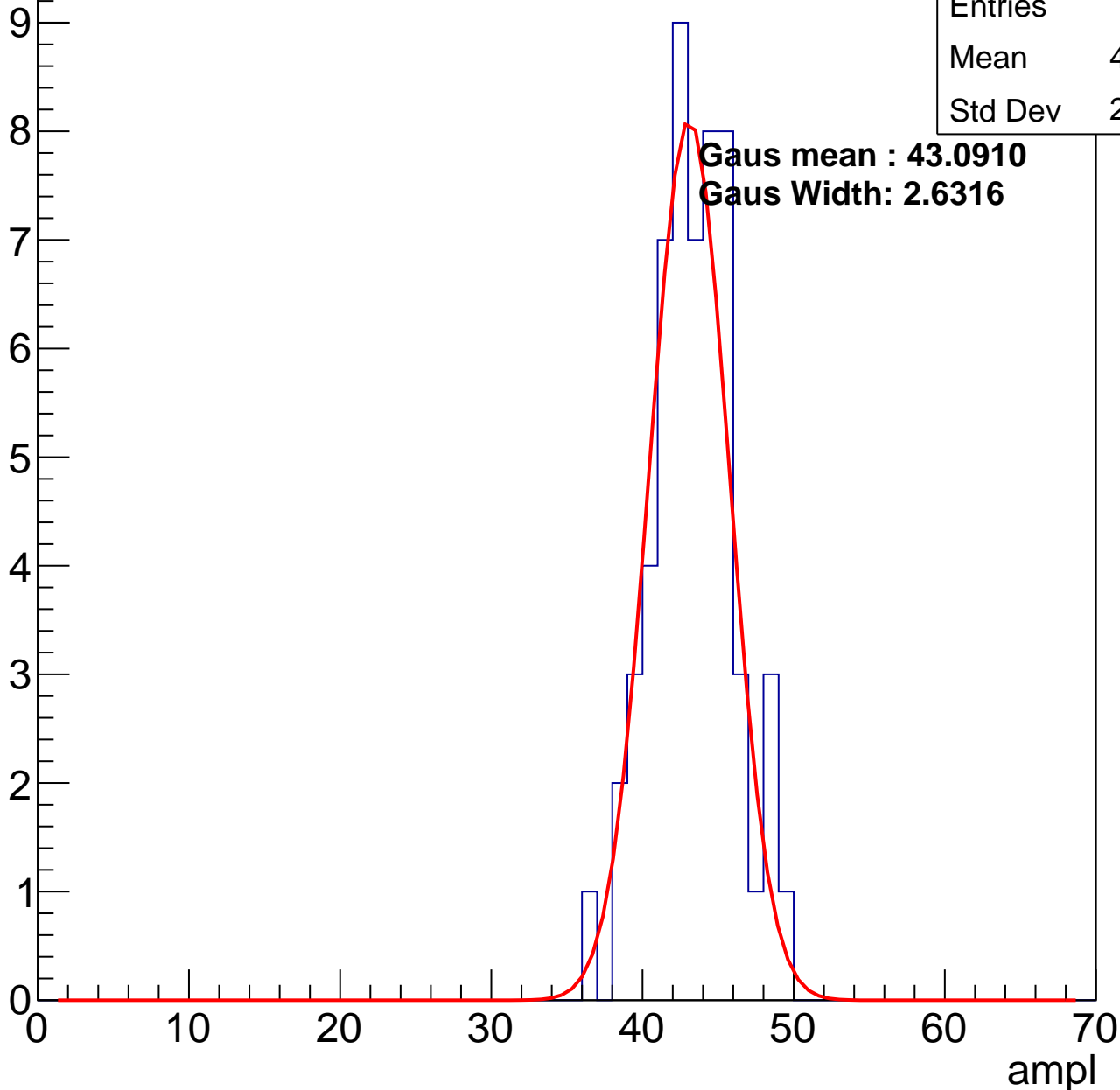
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	42.89
Std Dev	2.693

**Gaus mean : 43.0910**

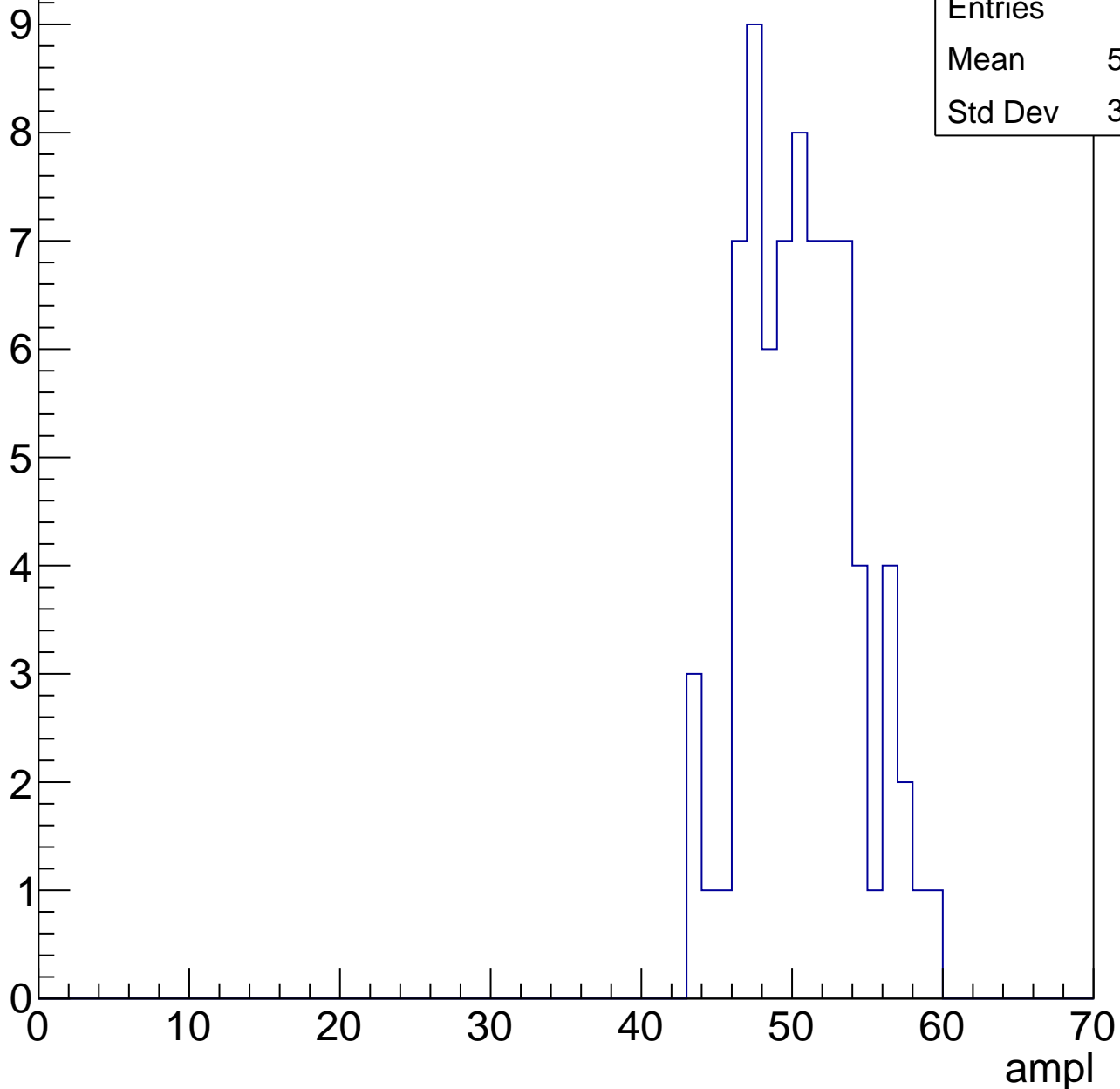
**Gaus Width: 2.6316**



# B1L003S, U11-ch25, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

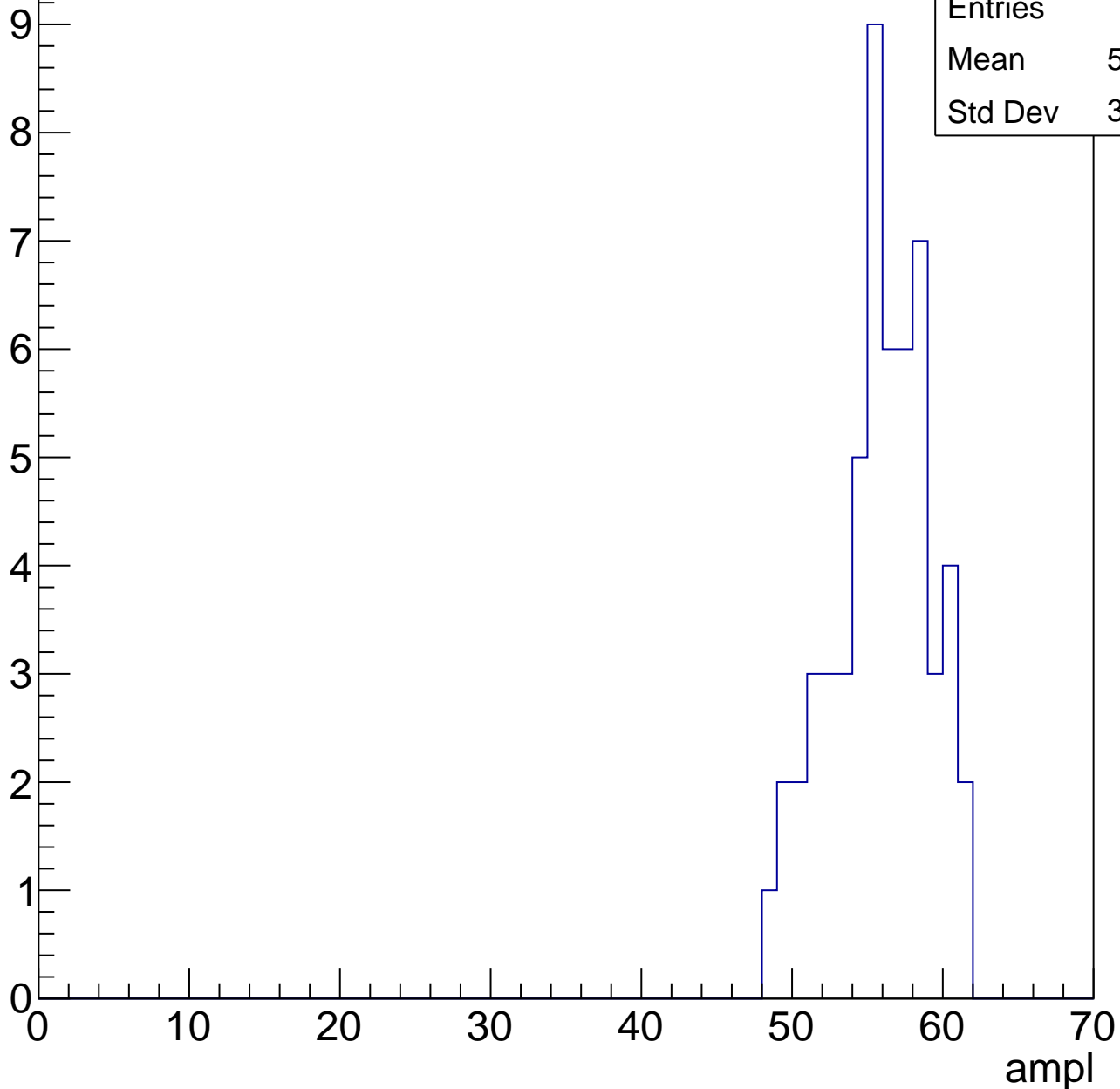


Entries	76
Mean	50.16
Std Dev	3.635

# B1L003S, U11-ch25, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

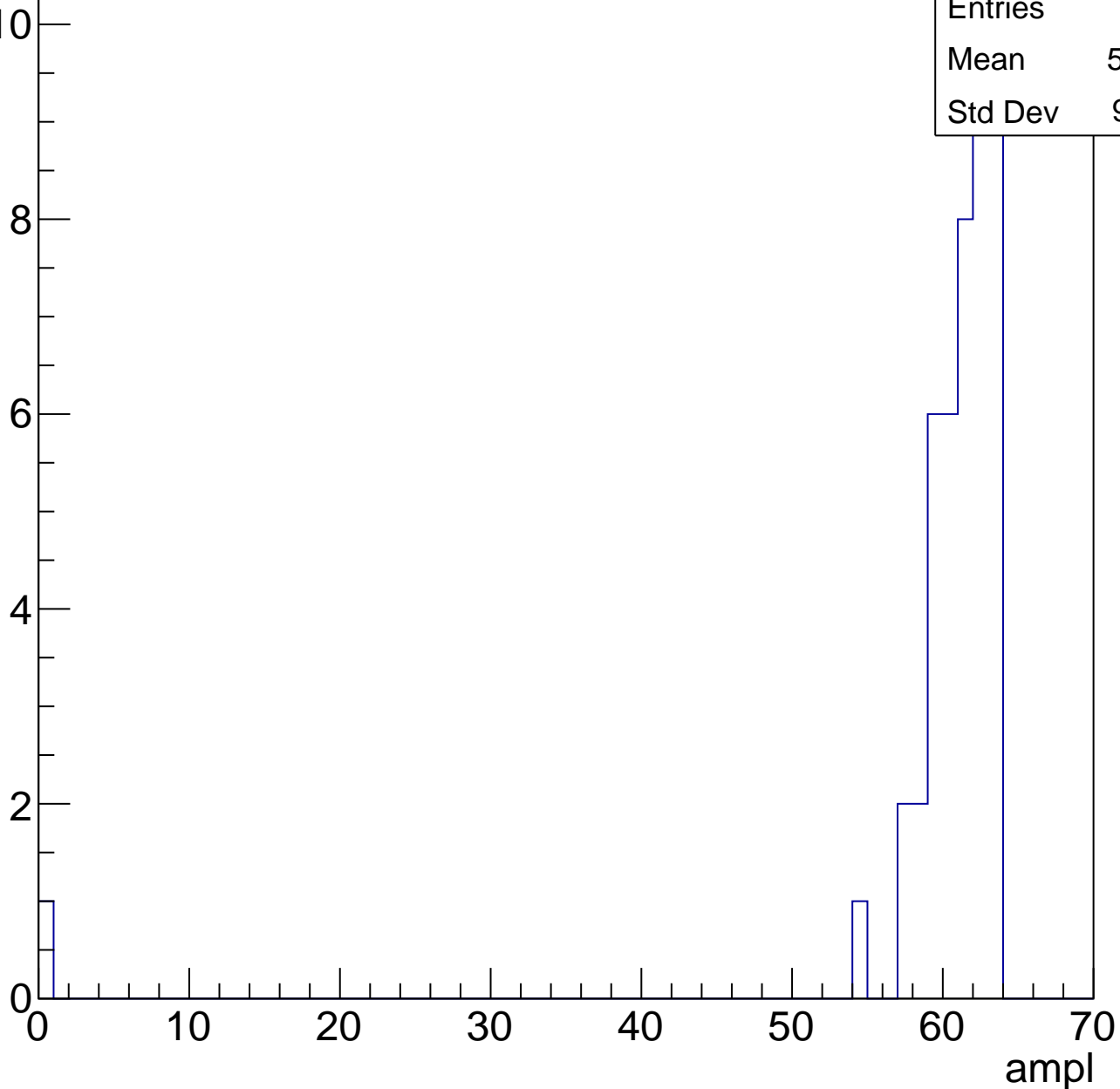


# B1L003S, U11-ch25, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	46
Mean	59.48
Std Dev	9.081



# B1L003S, U11-ch25, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L003S, U11-ch25, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U11-ch26, adc0

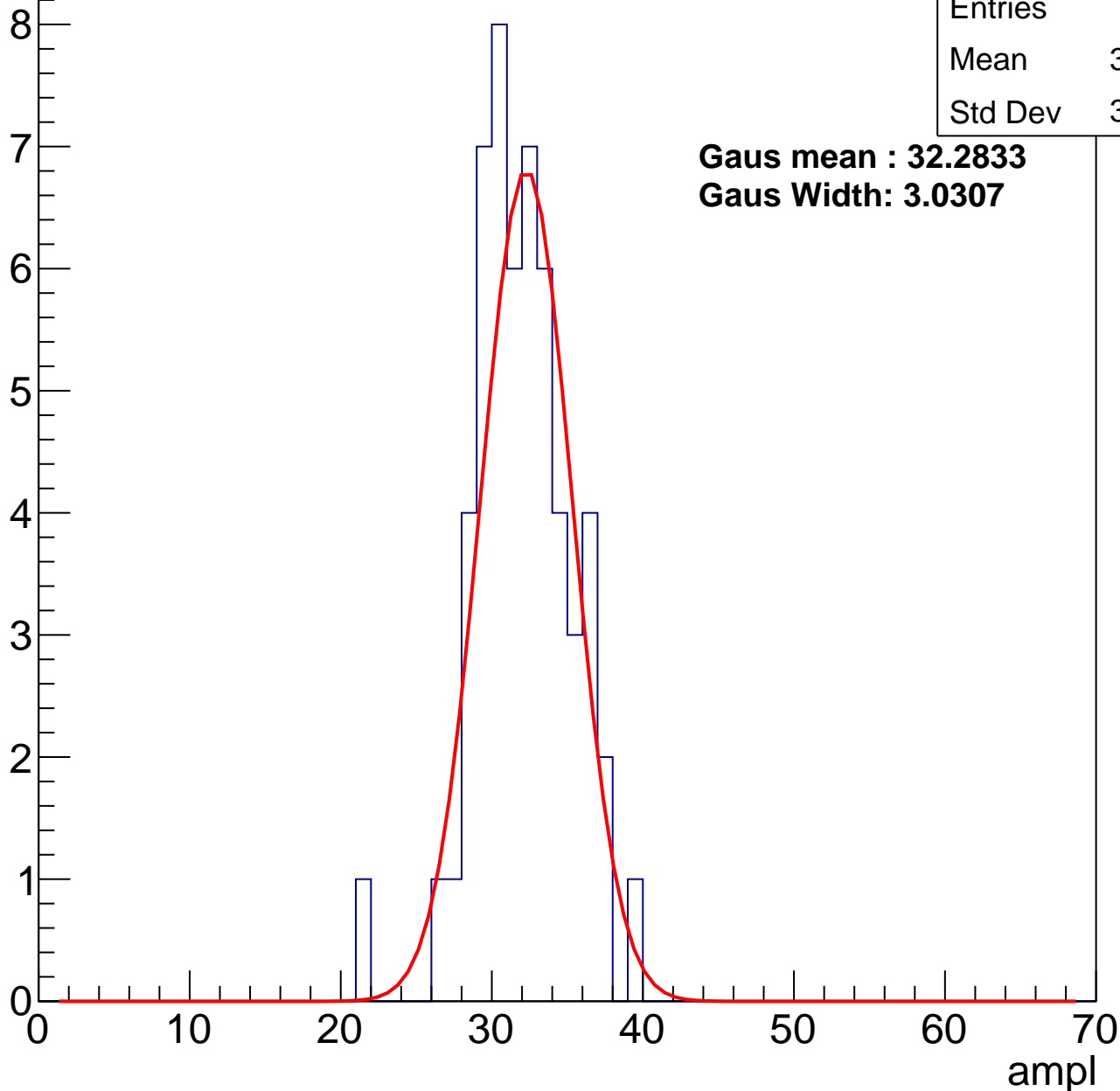
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	31.55
Std Dev	3.155

**Gaus mean : 32.2833**

**Gaus Width: 3.0307**



# B1L003S, U11-ch26, adc1

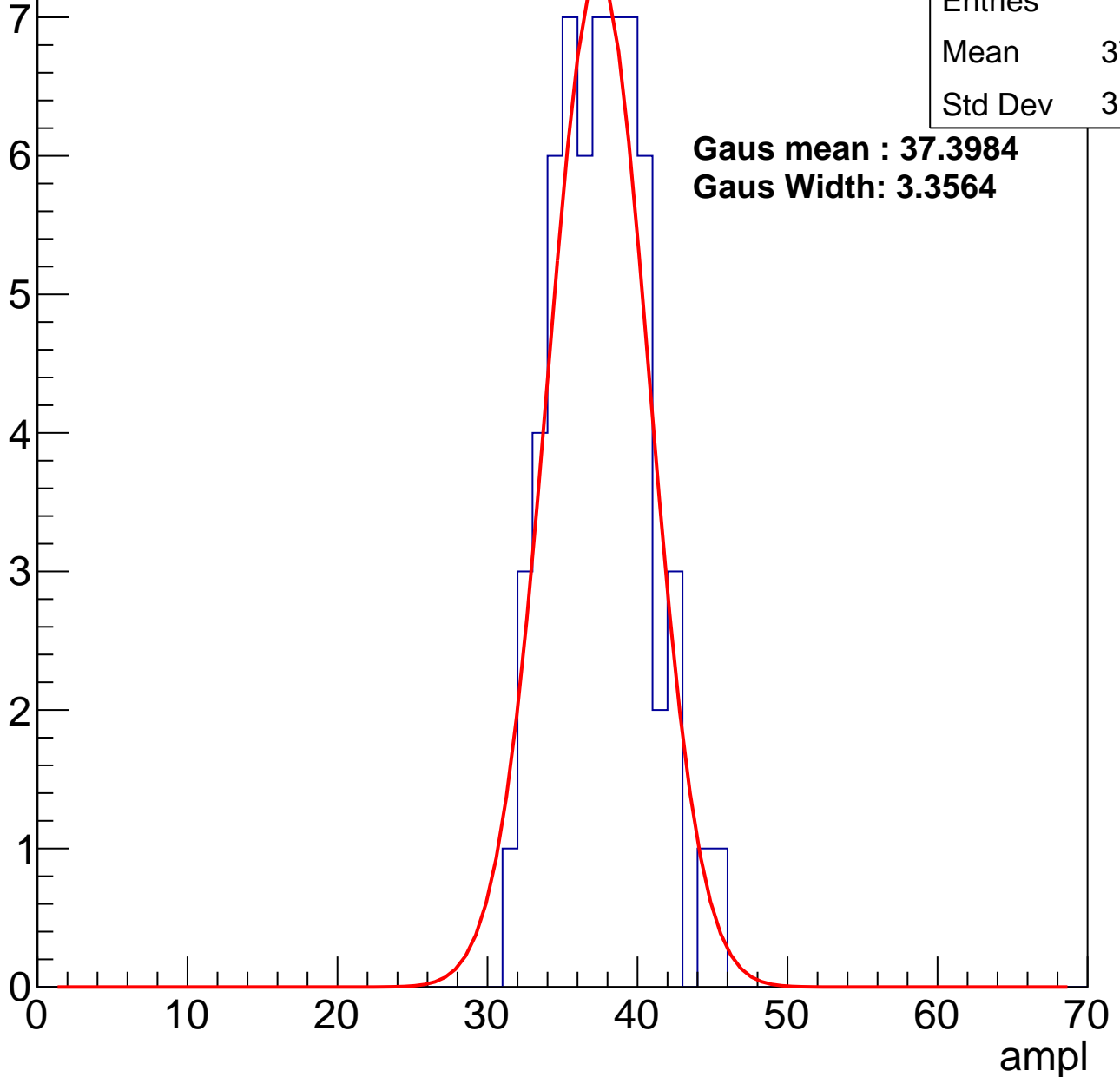
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	37.03
Std Dev	3.062

**Gaus mean : 37.3984**

**Gaus Width: 3.3564**



# B1L003S, U11-ch26, adc2

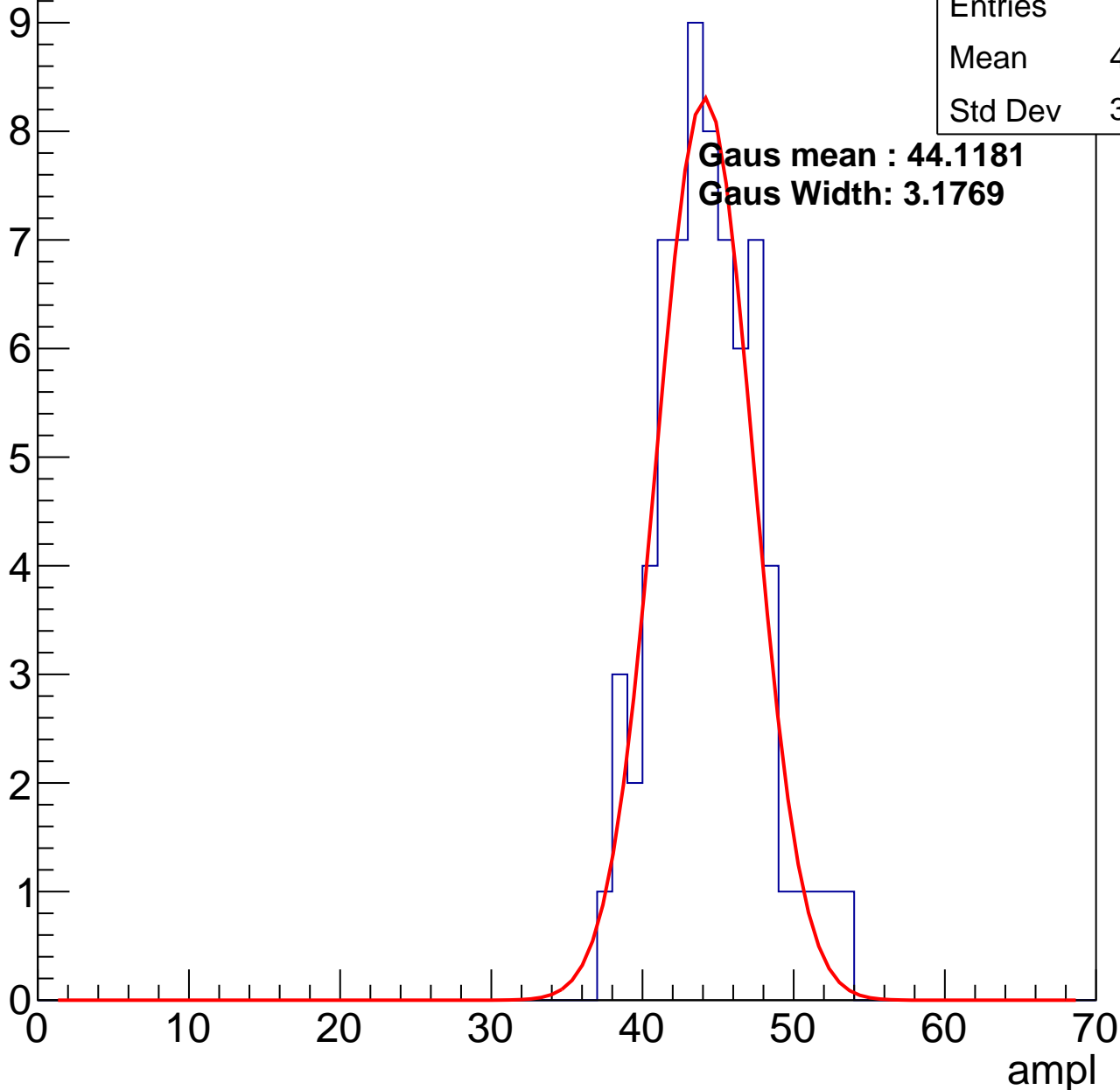
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	43.94
Std Dev	3.346

**Gaus mean : 44.1181**

**Gaus Width: 3.1769**

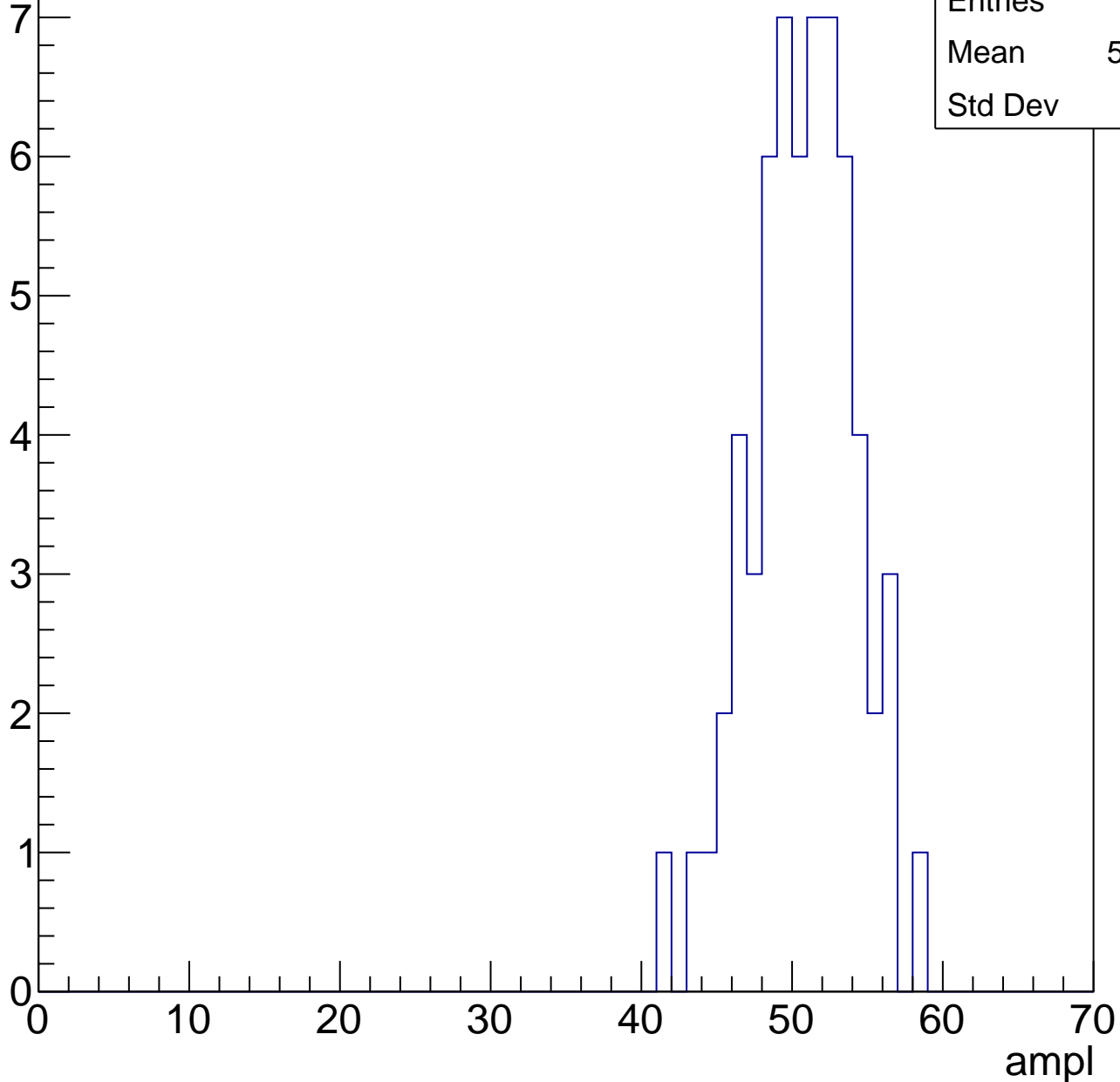


# B1L003S, U11-ch26, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	50.25
Std Dev	3.41



# B1L003S, U11-ch26, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	74
Mean	56.7
Std Dev	3.332

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

ampl

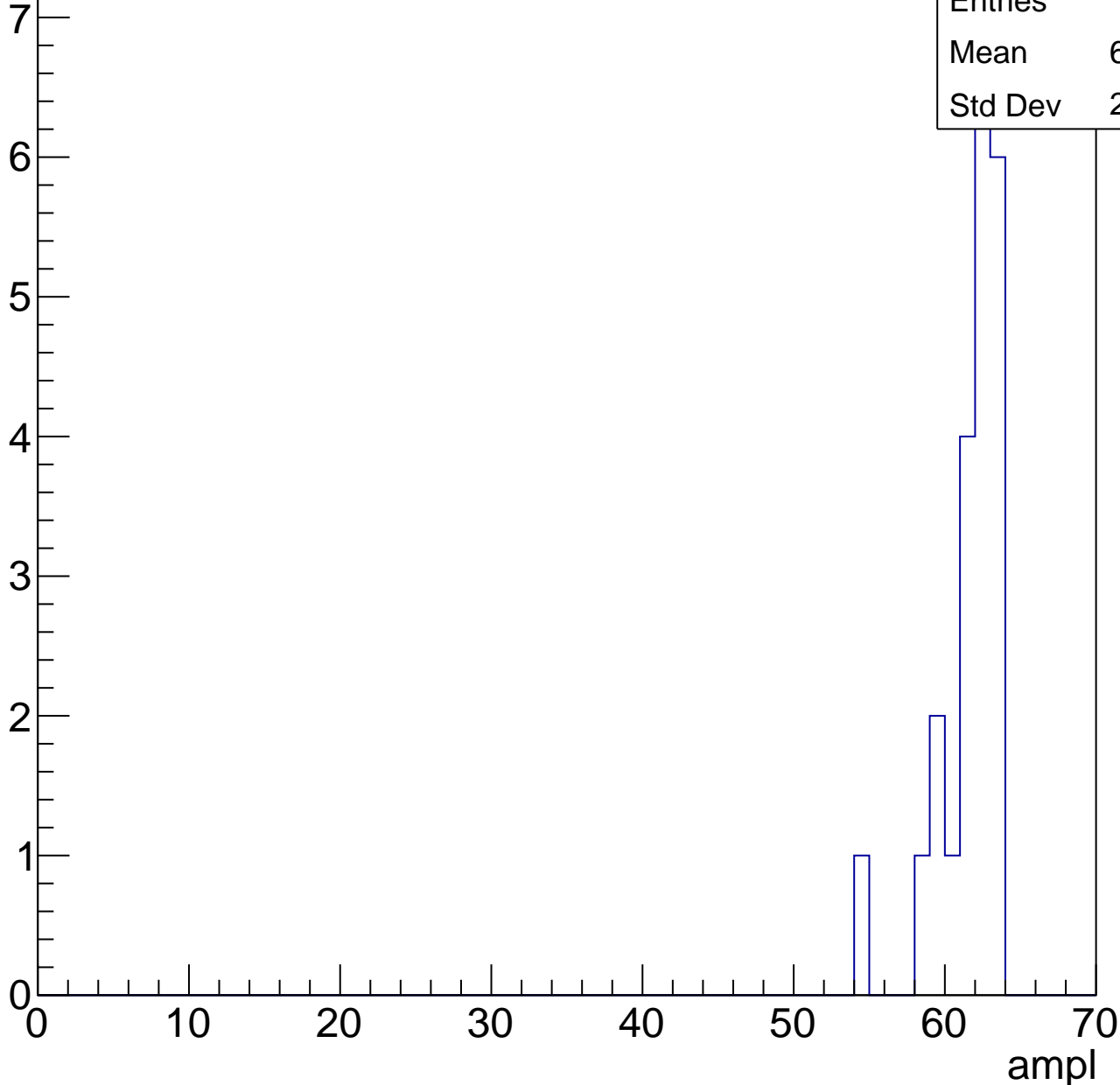
70

# B1L003S, U11-ch26, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

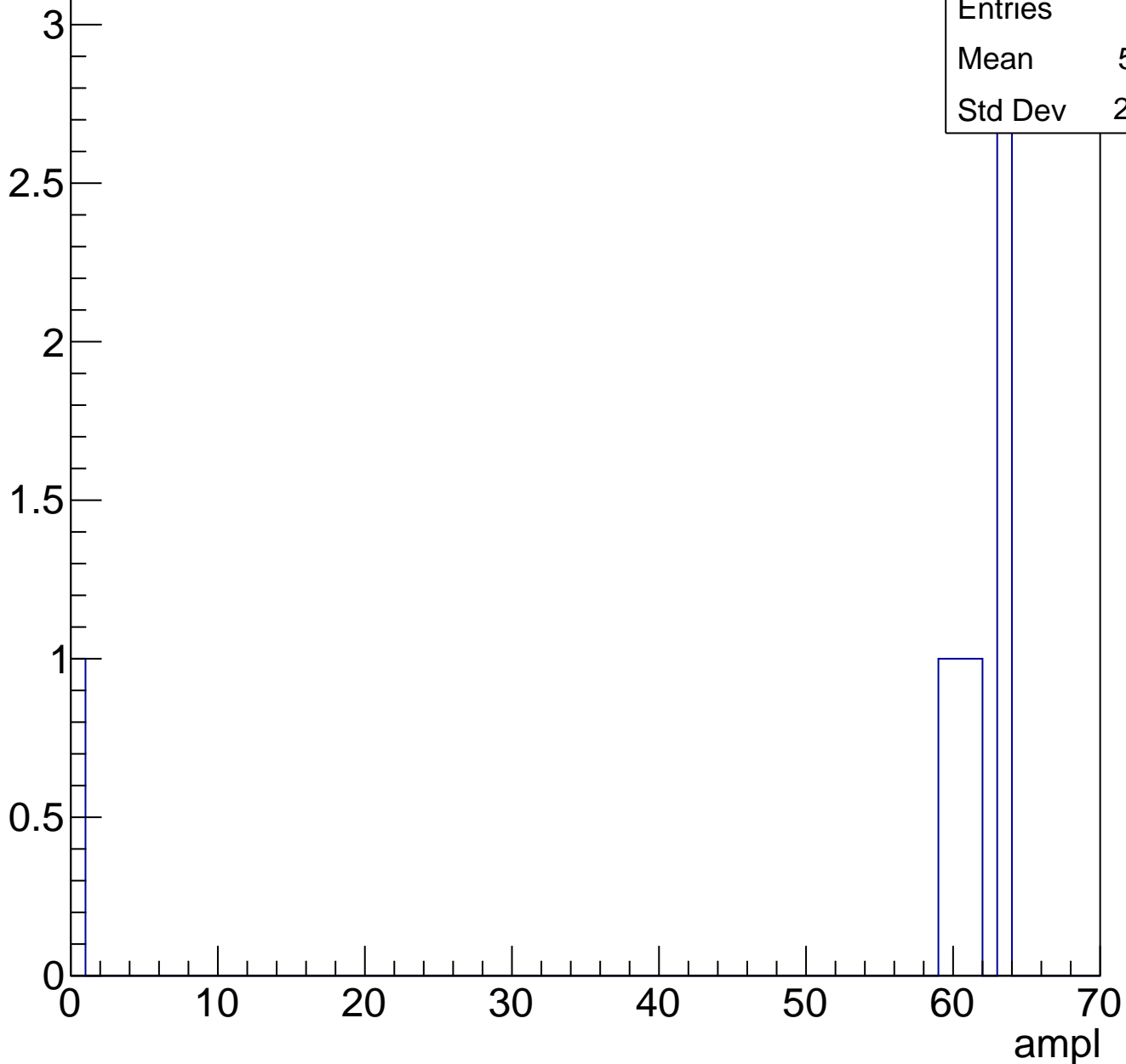
Entries	22
Mean	61.18
Std Dev	2.103



# B1L003S, U11-ch26, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch26, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U11-ch27, adc0

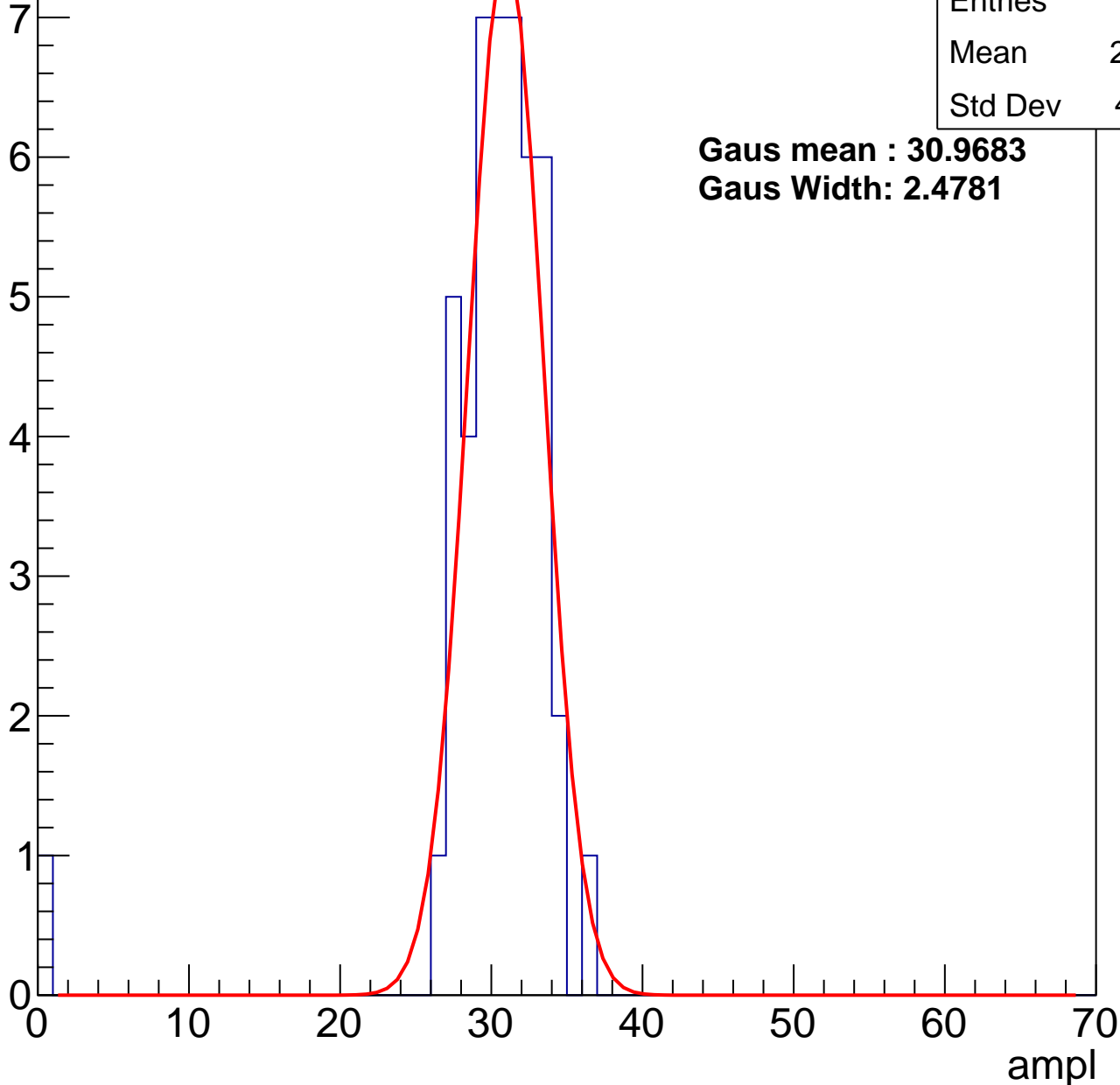
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	47
Mean	29.72
Std Dev	4.911

**Gaus mean : 30.9683**

**Gaus Width: 2.4781**

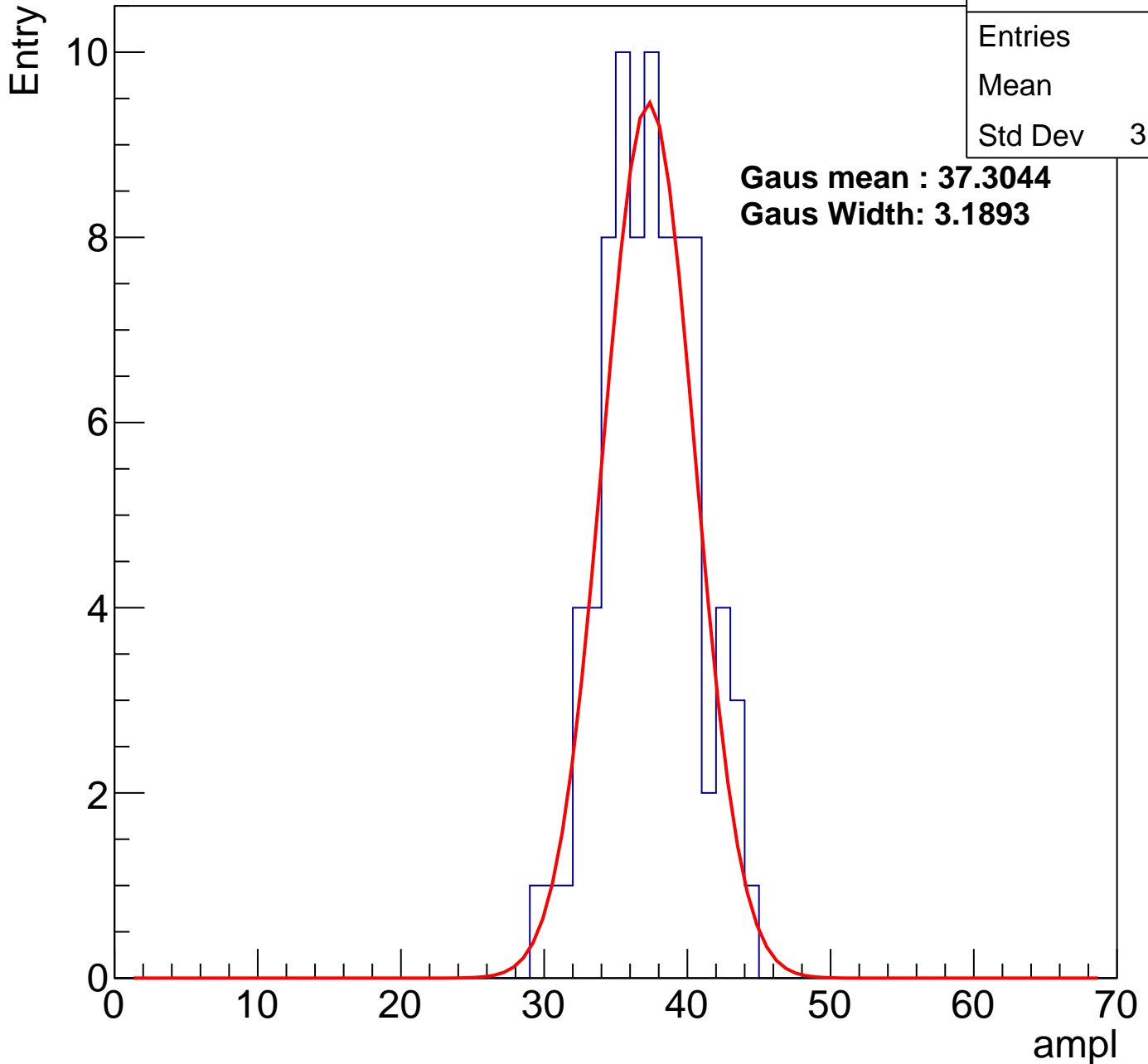


# B1L003S, U11-ch27, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	81
Mean	36.9
Std Dev	3.207

**Gaus mean : 37.3044**  
**Gaus Width: 3.1893**



# B1L003S, U11-ch27, adc2

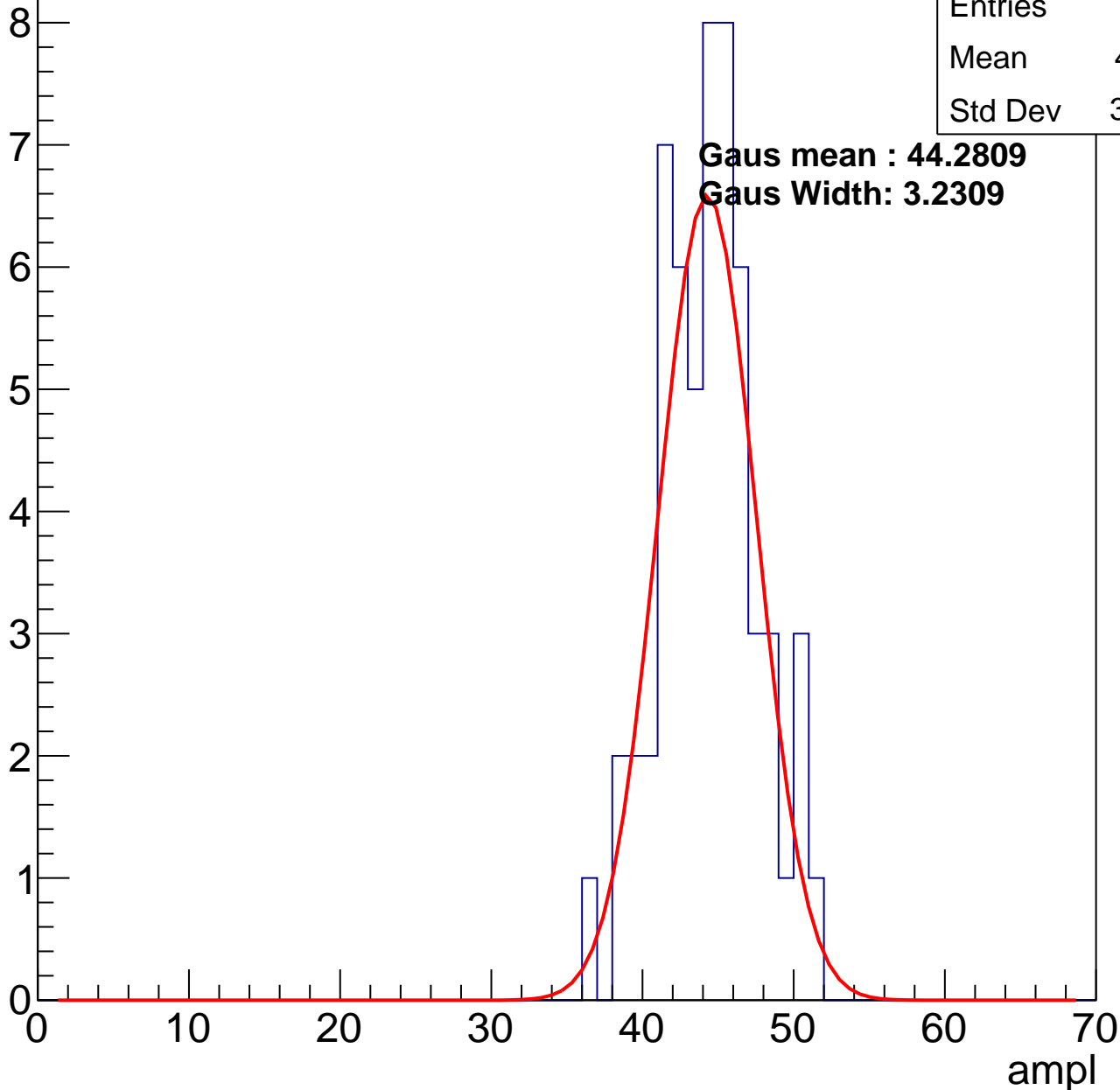
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	43.91
Std Dev	3.212

**Gaus mean : 44.2809**

**Gaus Width: 3.2309**

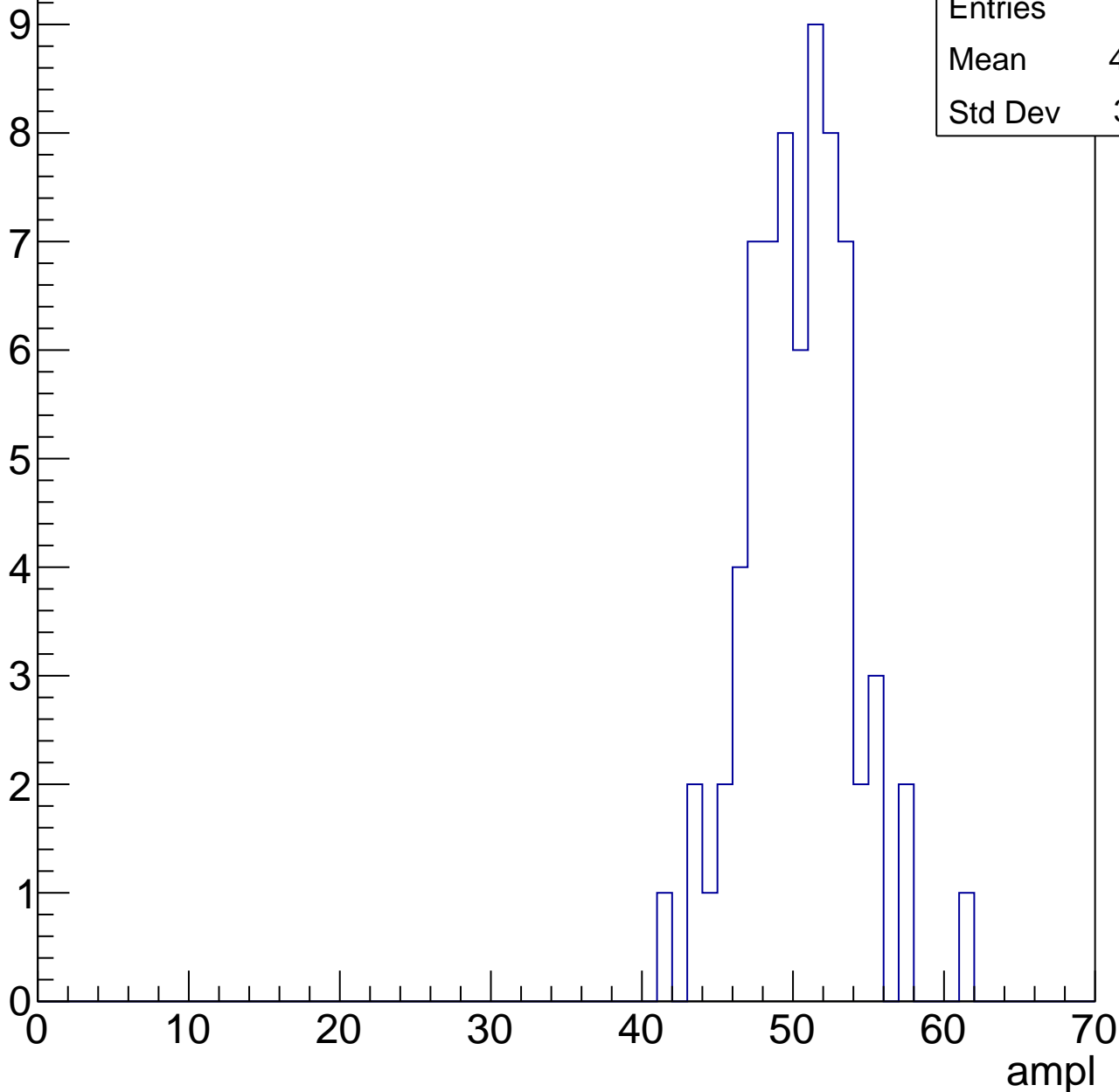


# B1L003S, U11-ch27, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

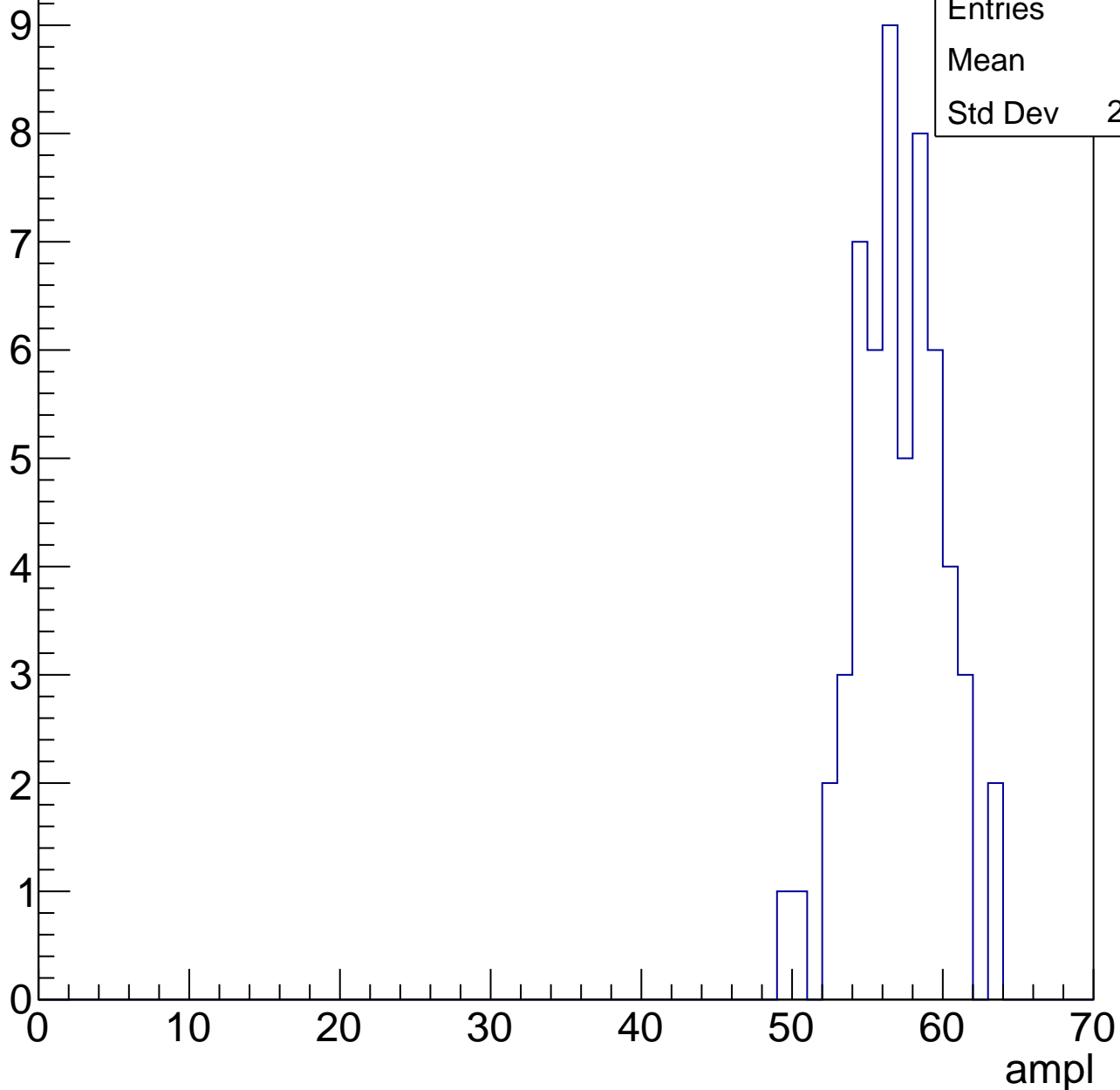
Entries	70
Mean	49.94
Std Dev	3.501



# B1L003S, U11-ch27, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

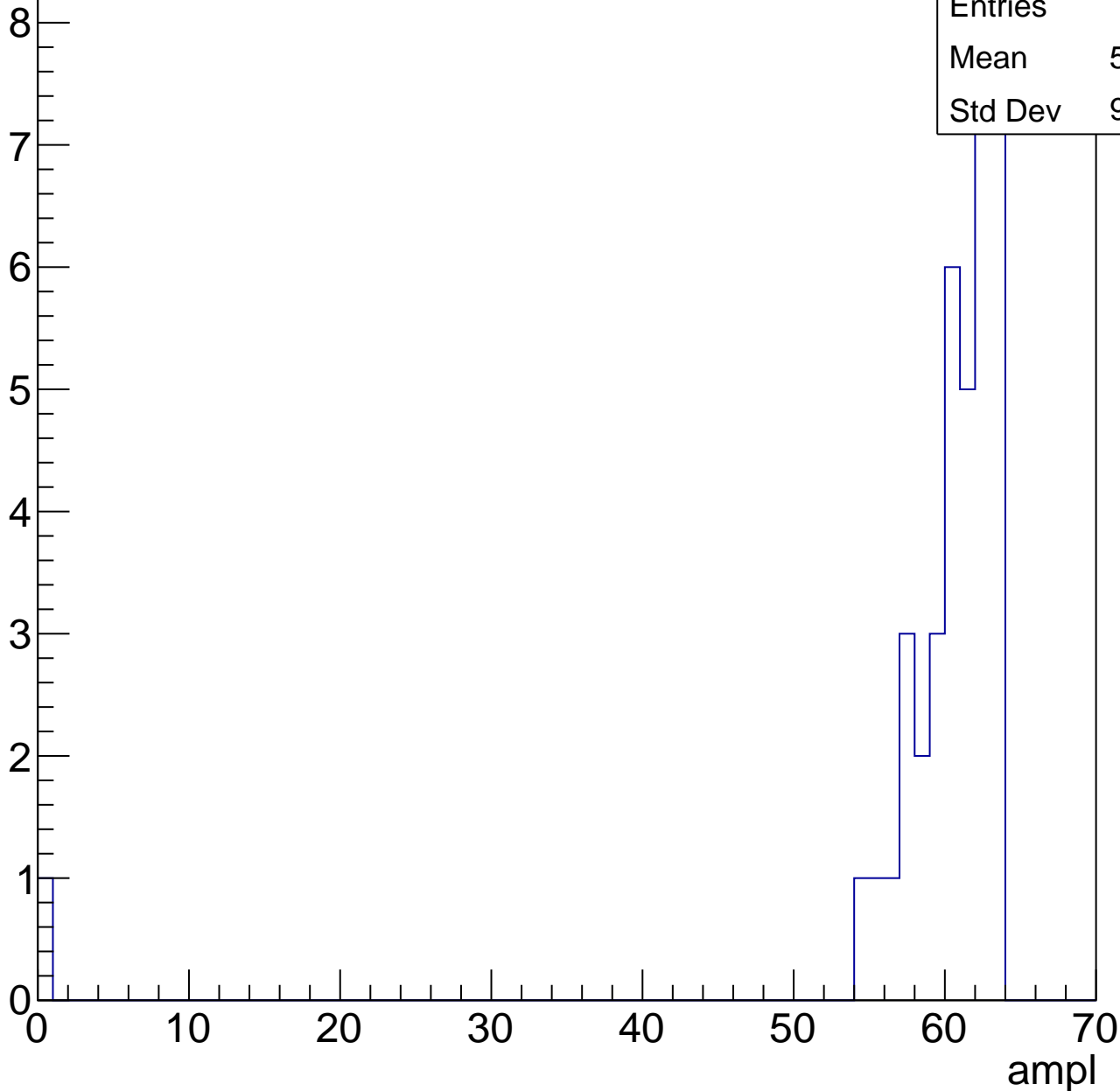


# B1L003S, U11-ch27, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

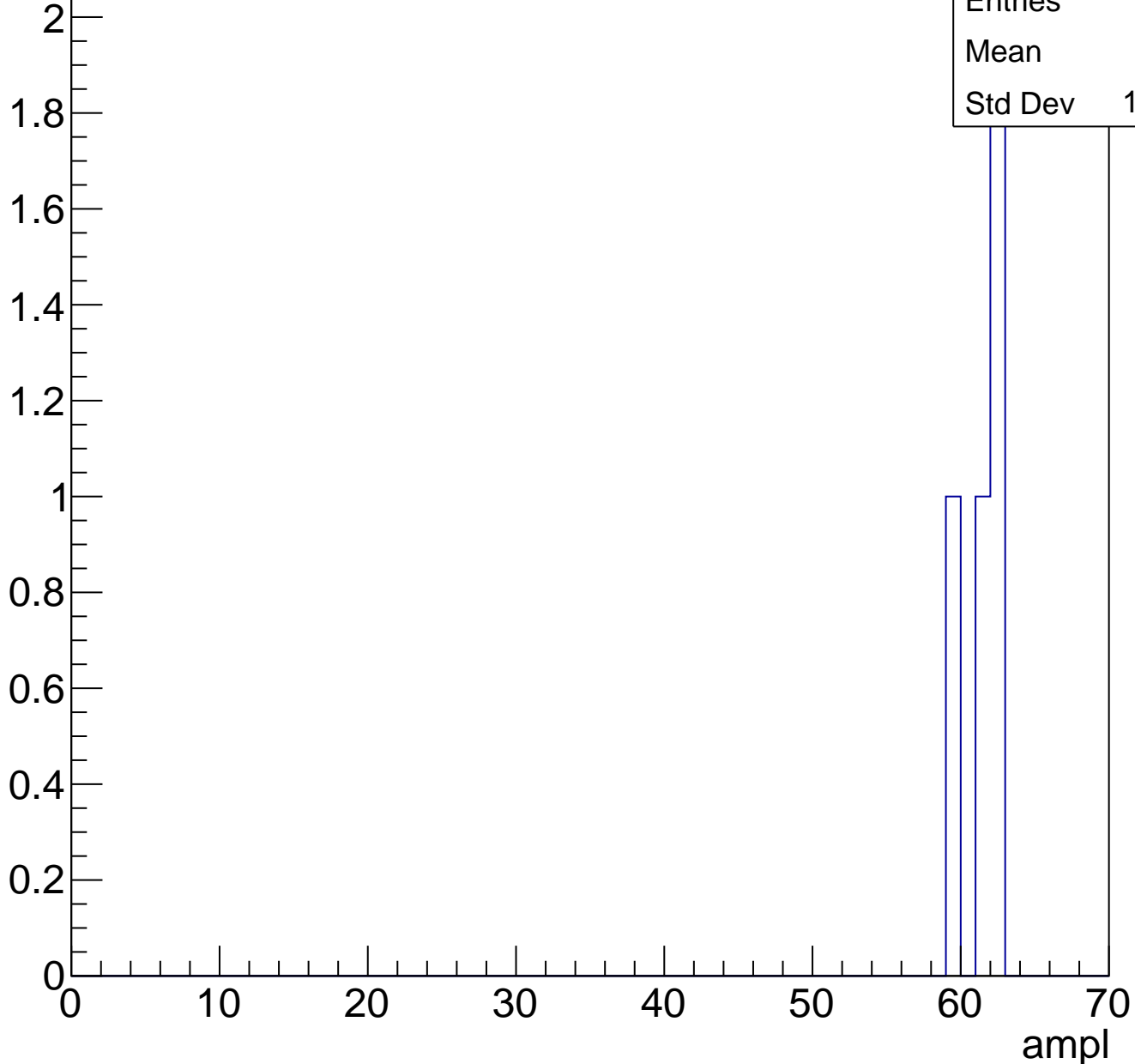
Entries	39
Mean	58.82
Std Dev	9.832



# B1L003S, U11-ch27, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch27, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U11-ch28, adc0

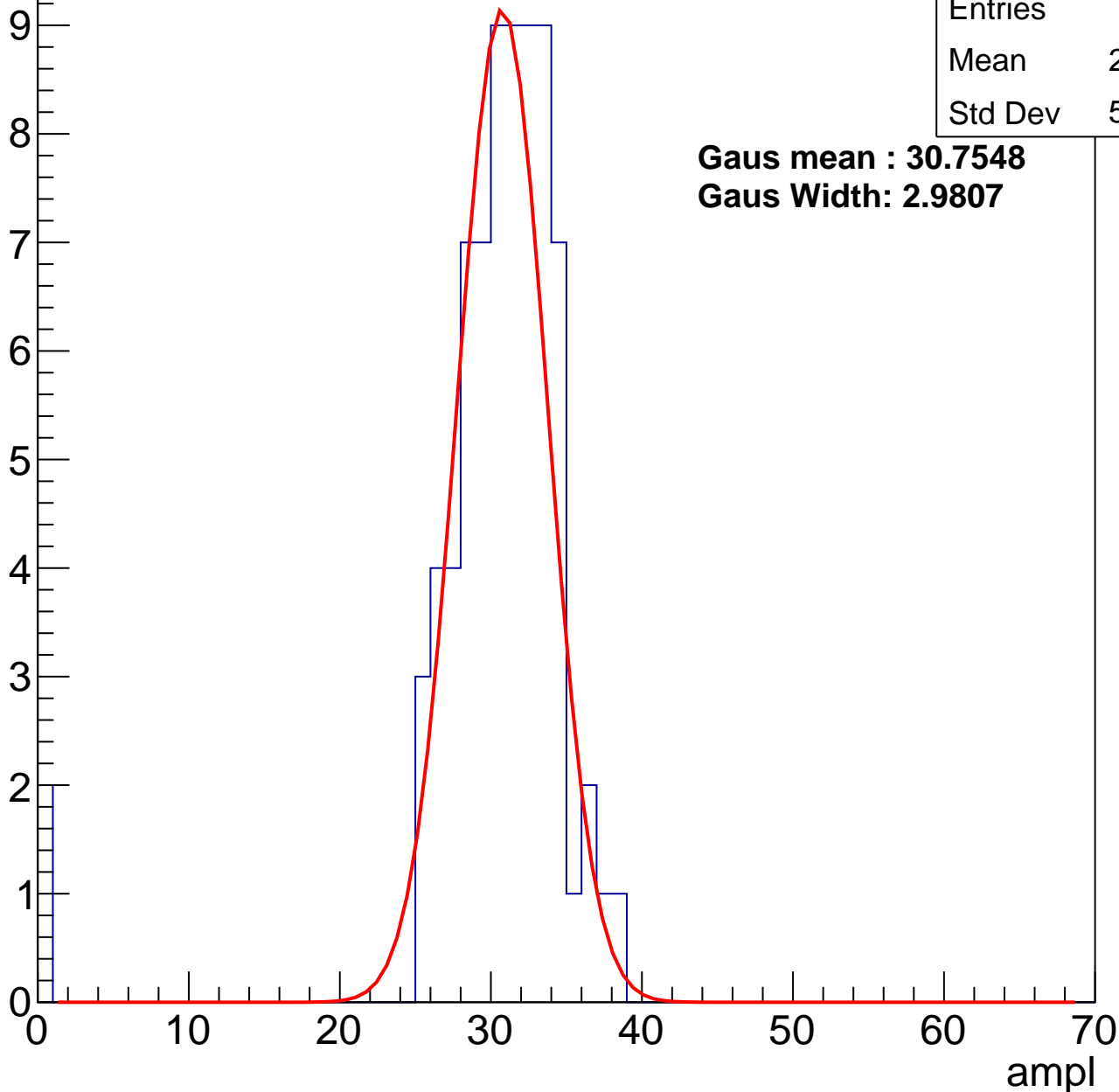
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	75
Mean	29.87
Std Dev	5.723

**Gaus mean : 30.7548**

**Gaus Width: 2.9807**



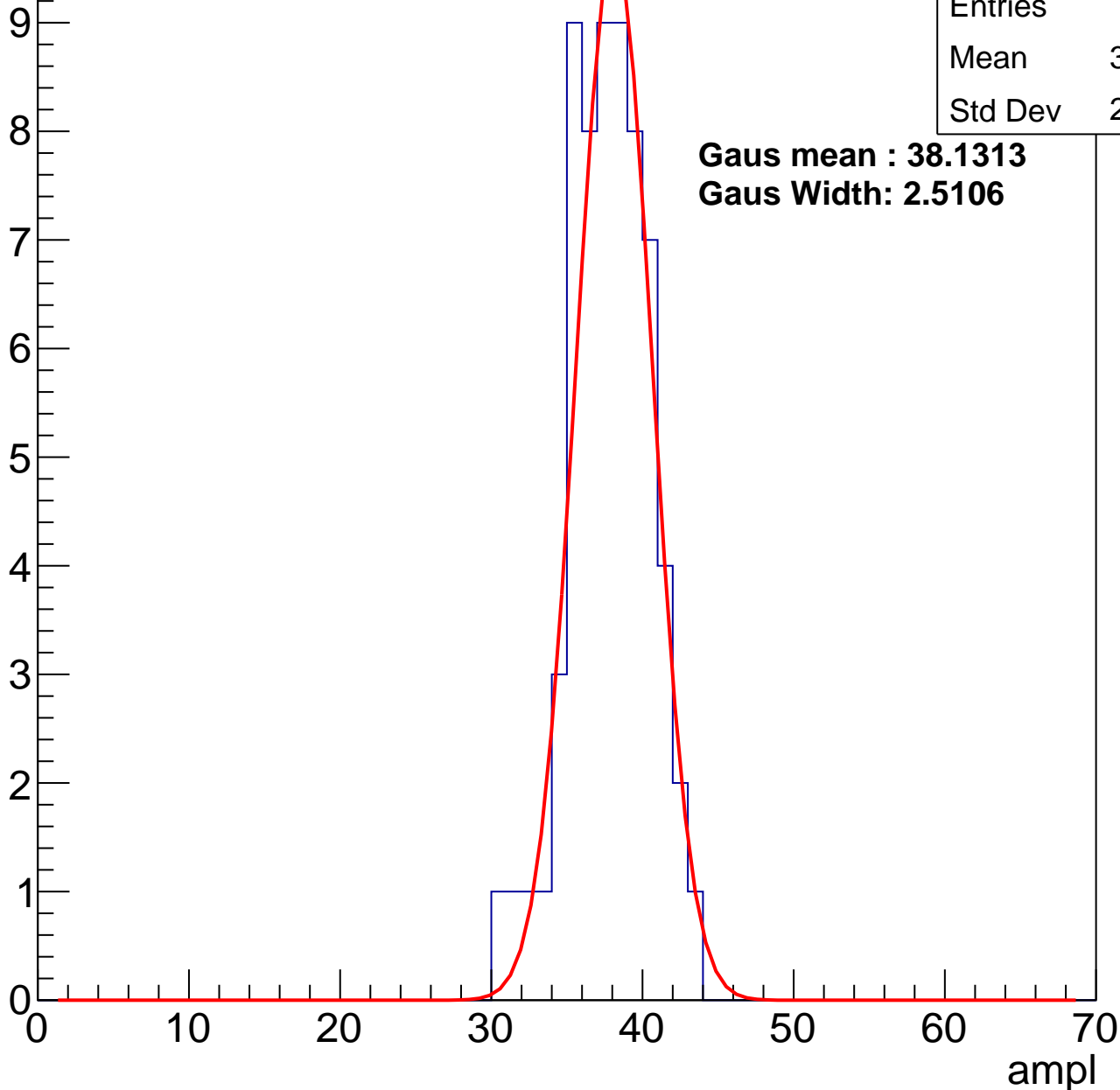
# B1L003S, U11-ch28, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	37.33
Std Dev	2.634

**Gaus mean : 38.1313**  
**Gaus Width: 2.5106**



# B1L003S, U11-ch28, adc2

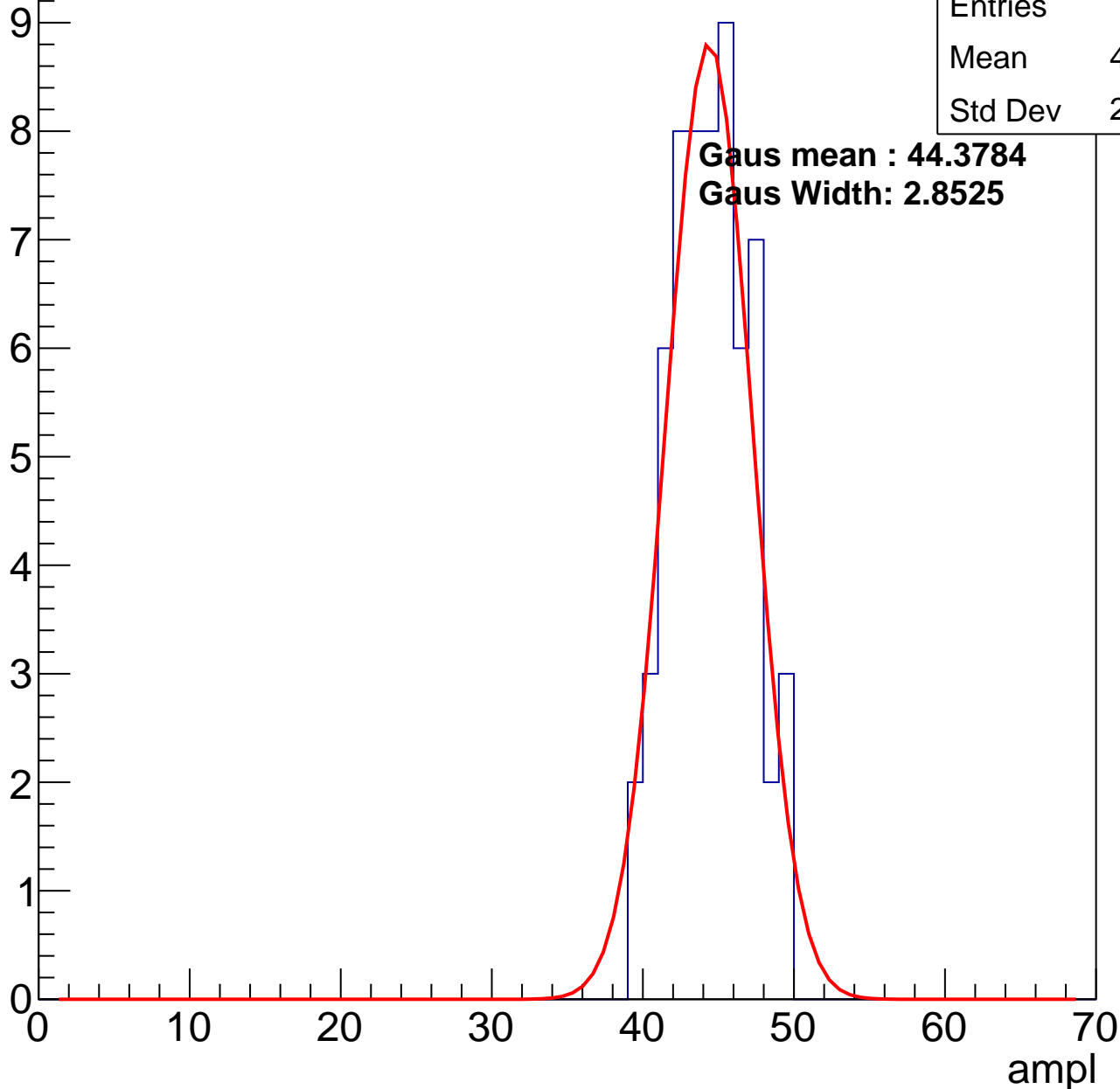
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	44.02
Std Dev	2.524

**Gaus mean : 44.3784**

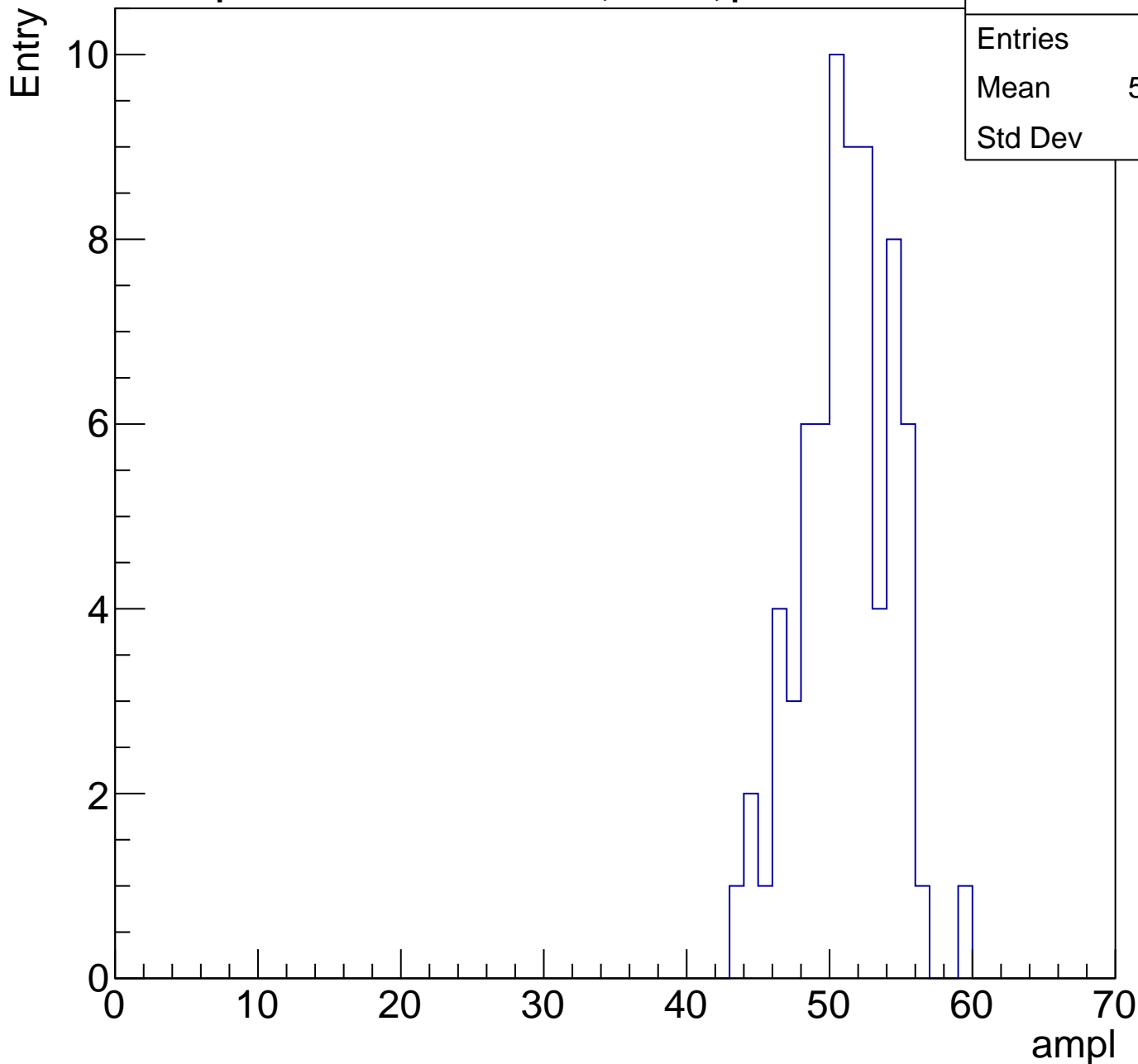
**Gaus Width: 2.8525**



# B1L003S, U11-ch28, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	71
Mean	50.69
Std Dev	3.16

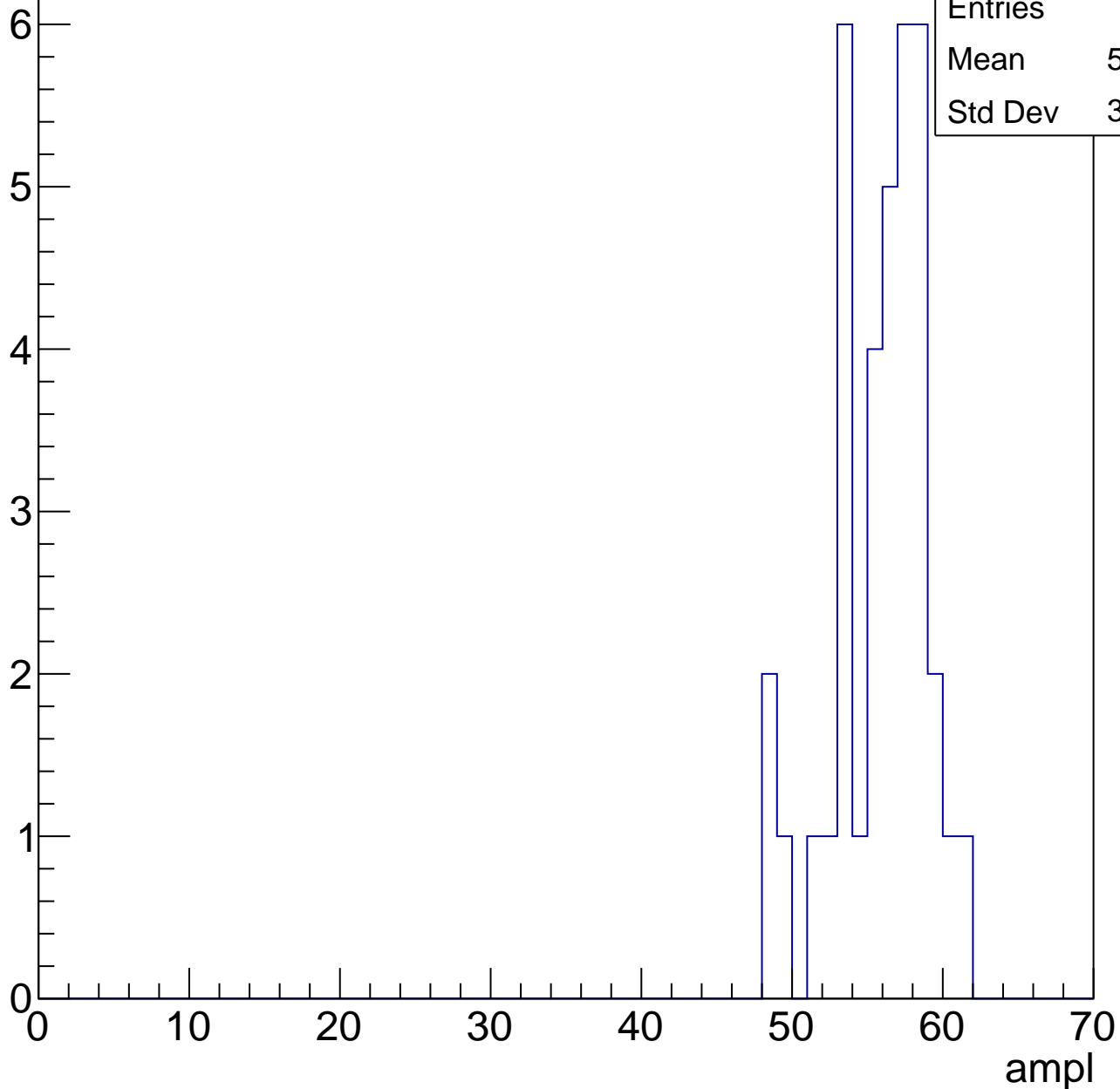


# B1L003S, U11-ch28, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	37
Mean	55.38
Std Dev	3.096

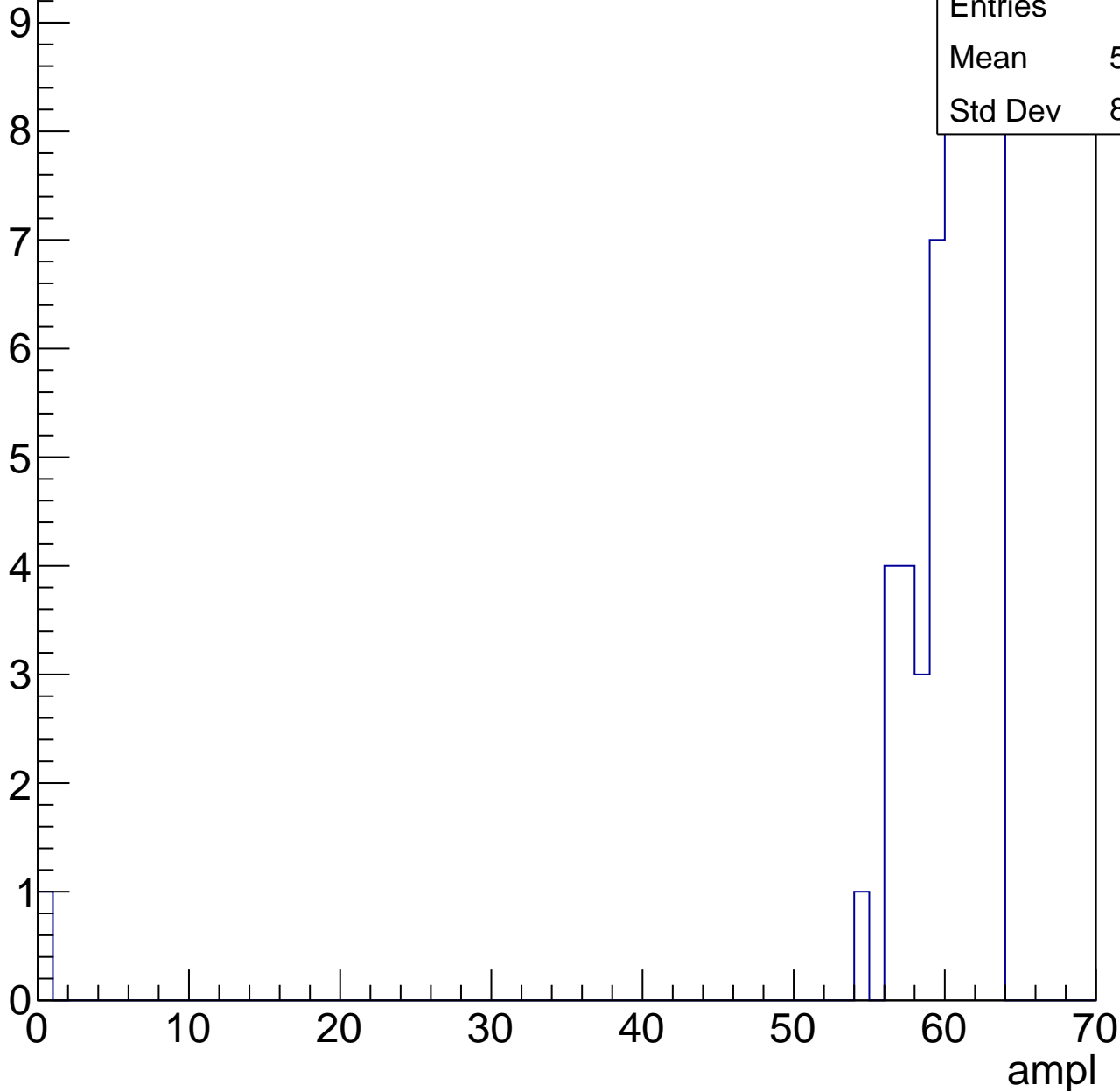


# B1L003S, U11-ch28, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

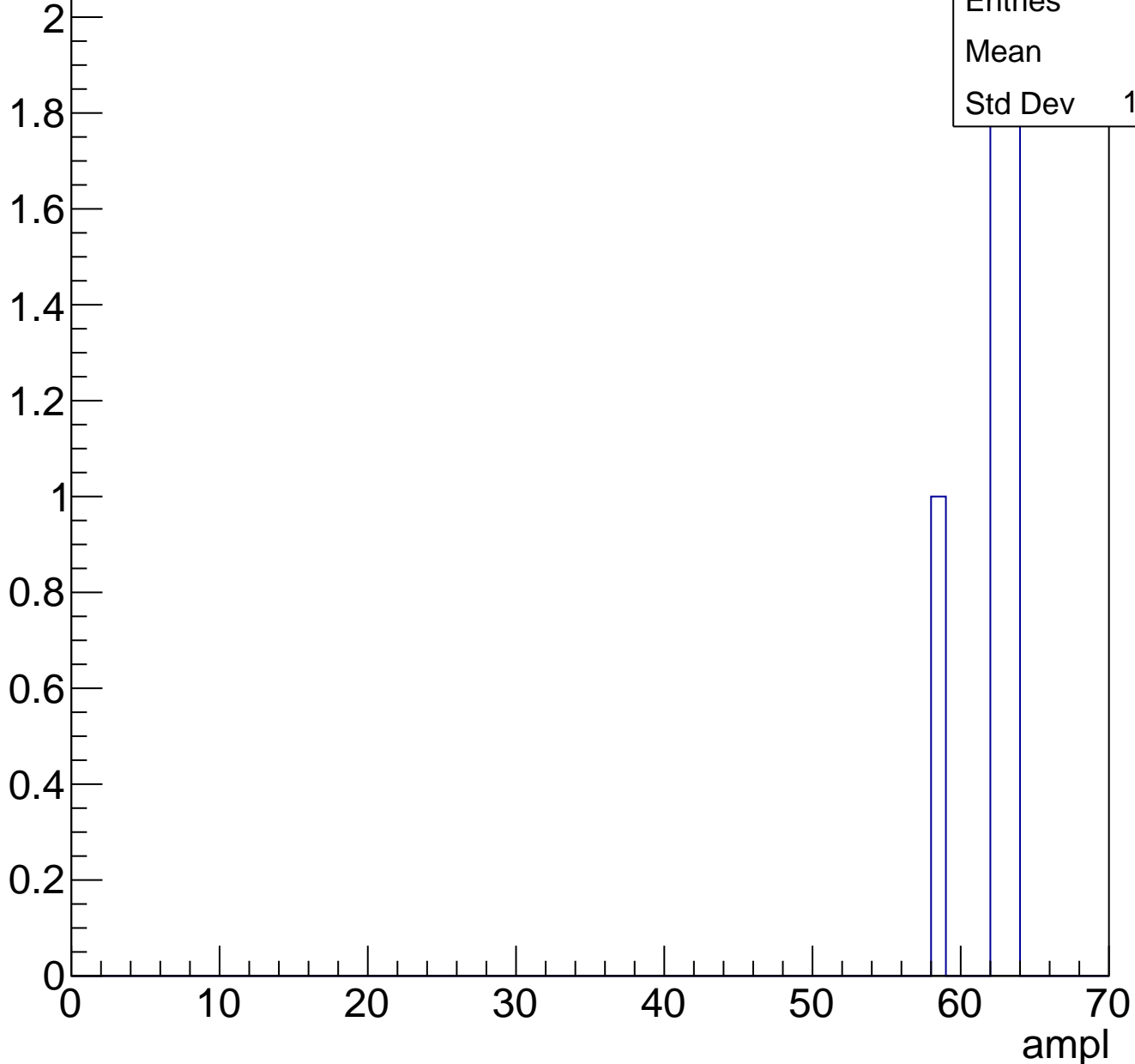
Entries	54
Mean	58.93
Std Dev	8.395



# B1L003S, U11-ch28, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch28, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U11-ch29, adc0

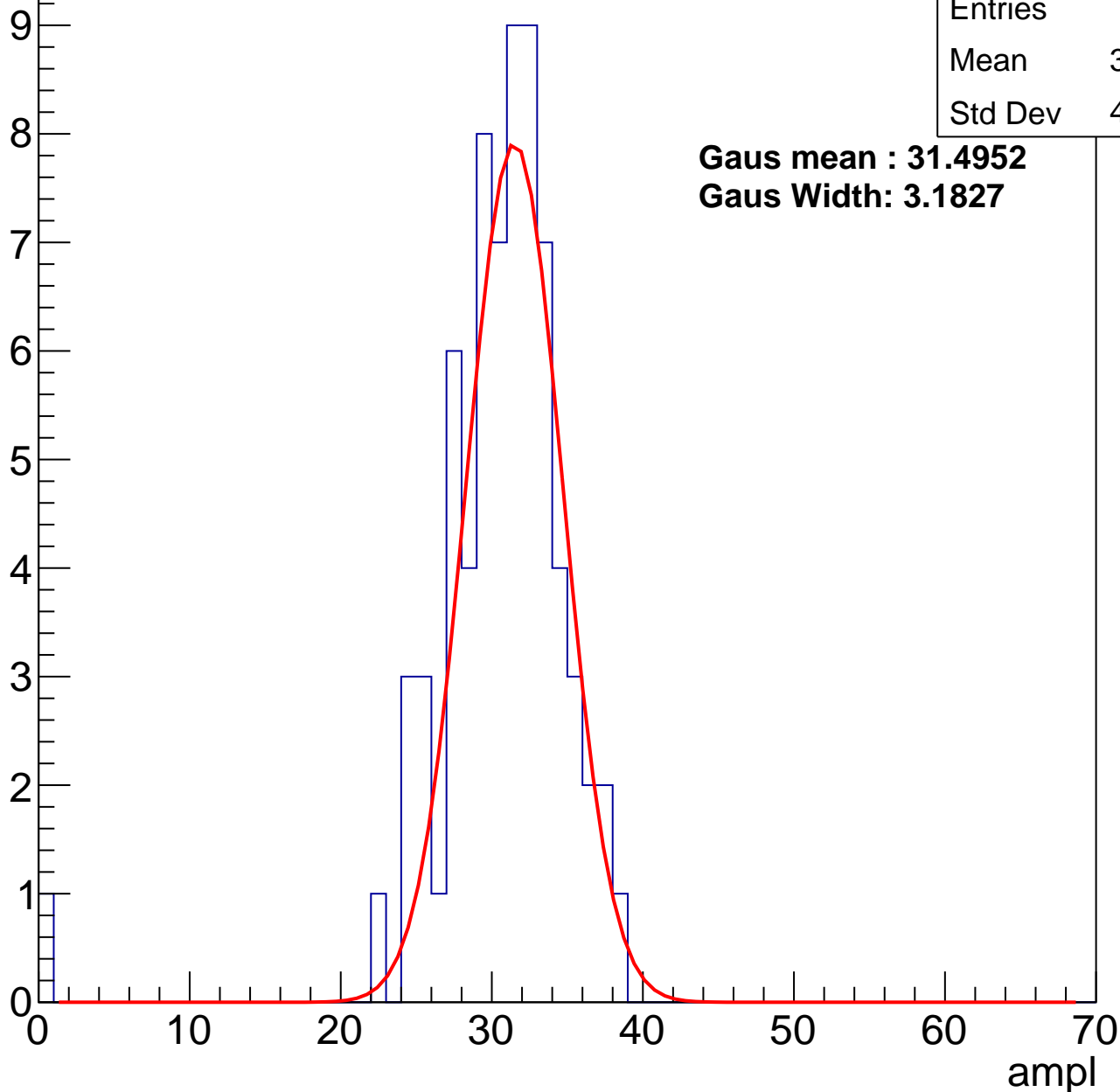
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	71
Mean	30.06
Std Dev	4.924

**Gaus mean : 31.4952**

**Gaus Width: 3.1827**



# B1L003S, U11-ch29, adc1

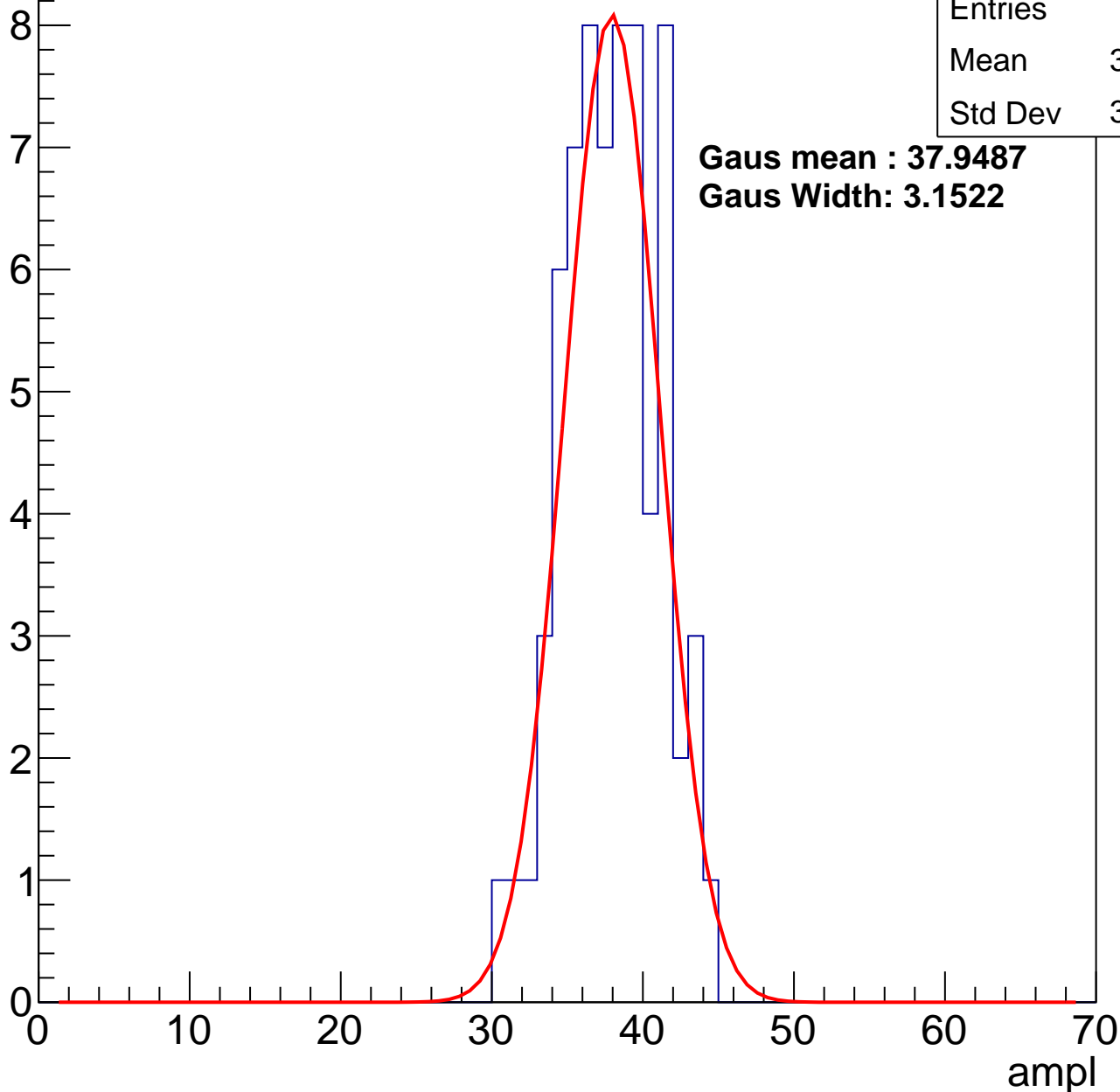
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	37.49
Std Dev	3.075

**Gaus mean : 37.9487**

**Gaus Width: 3.1522**



# B1L003S, U11-ch29, adc2

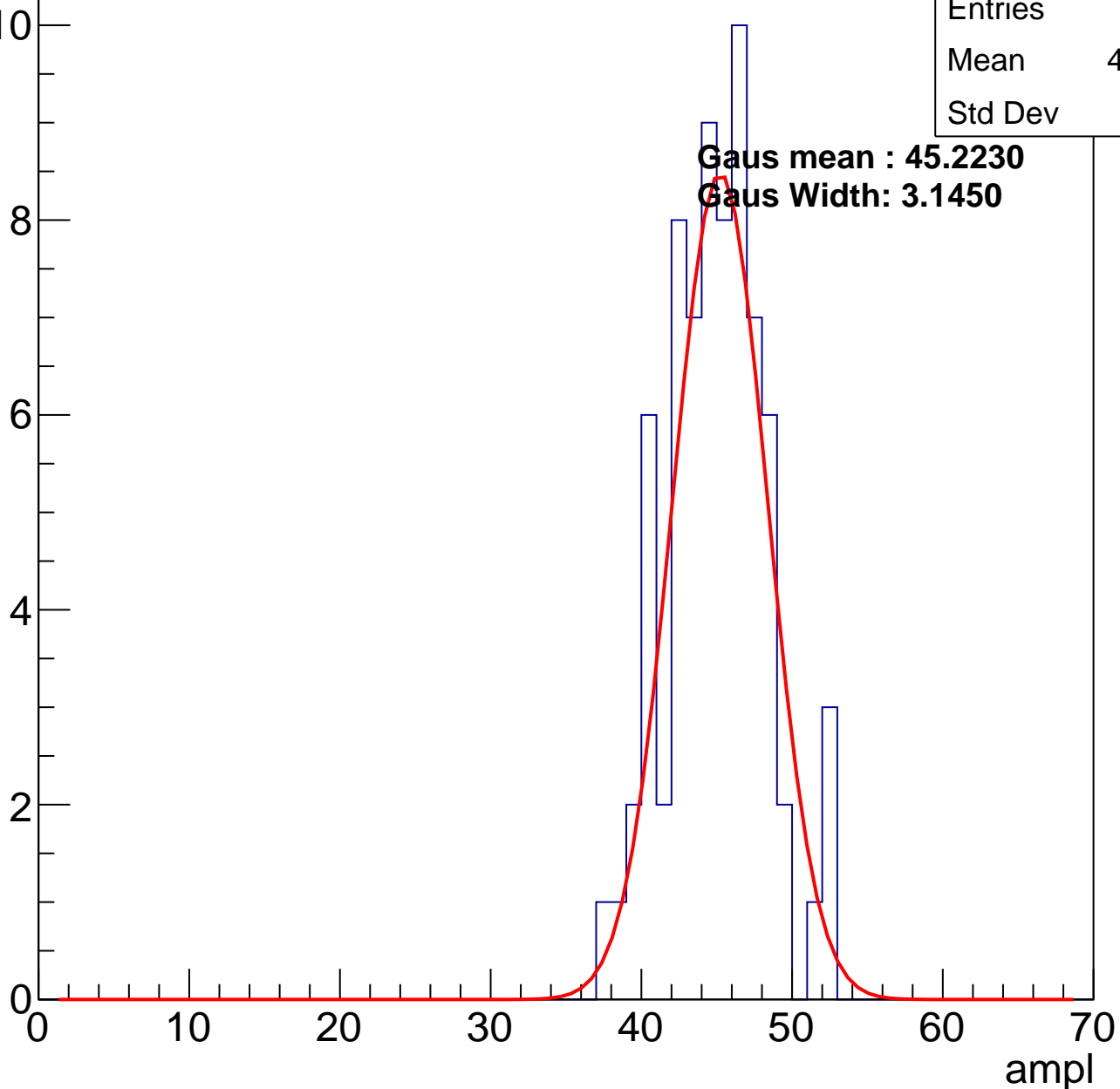
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	73
Mean	44.52
Std Dev	3.24

**Gaus mean : 45.2230**

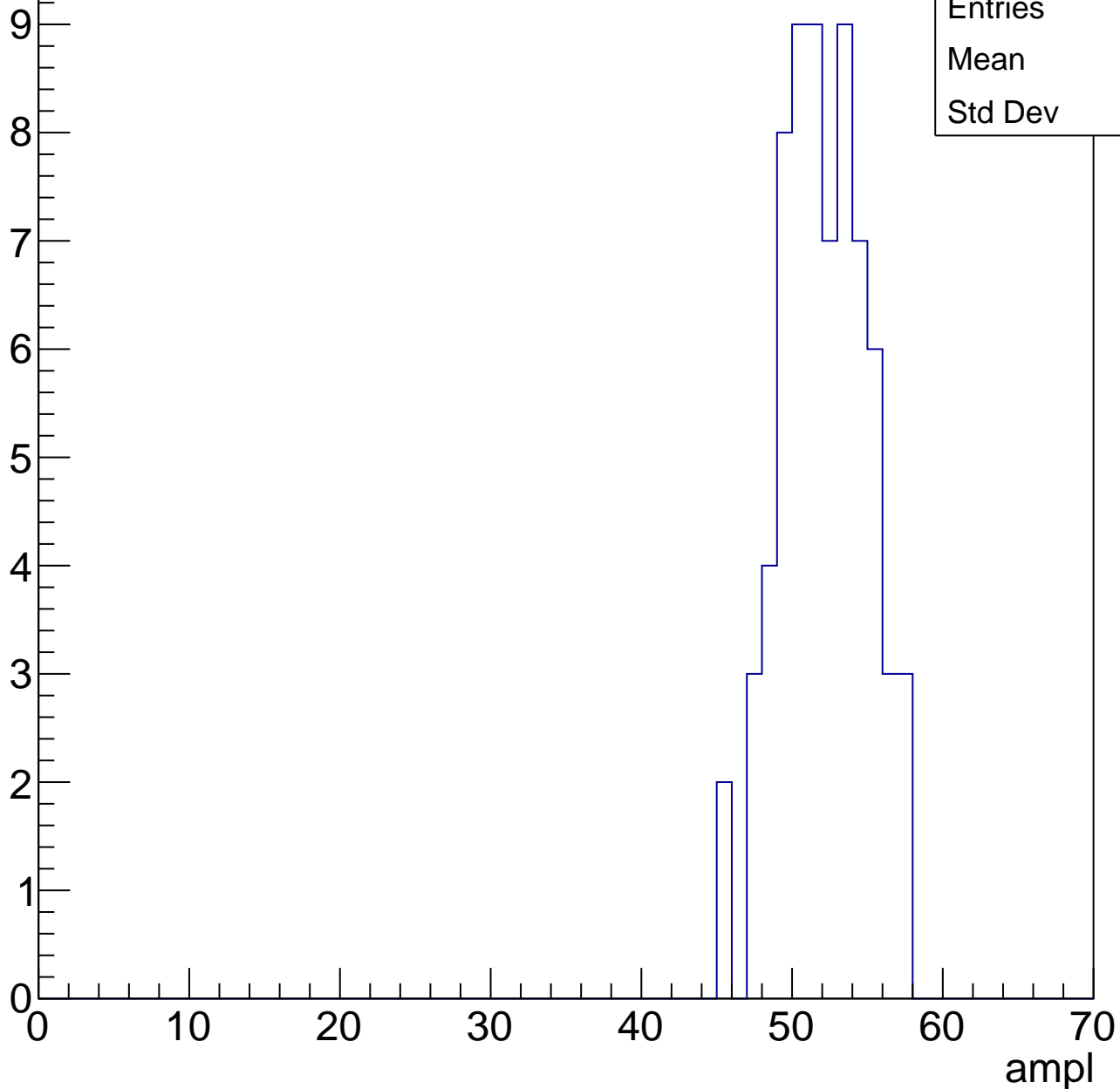
**Gaus Width: 3.1450**



# B1L003S, U11-ch29, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

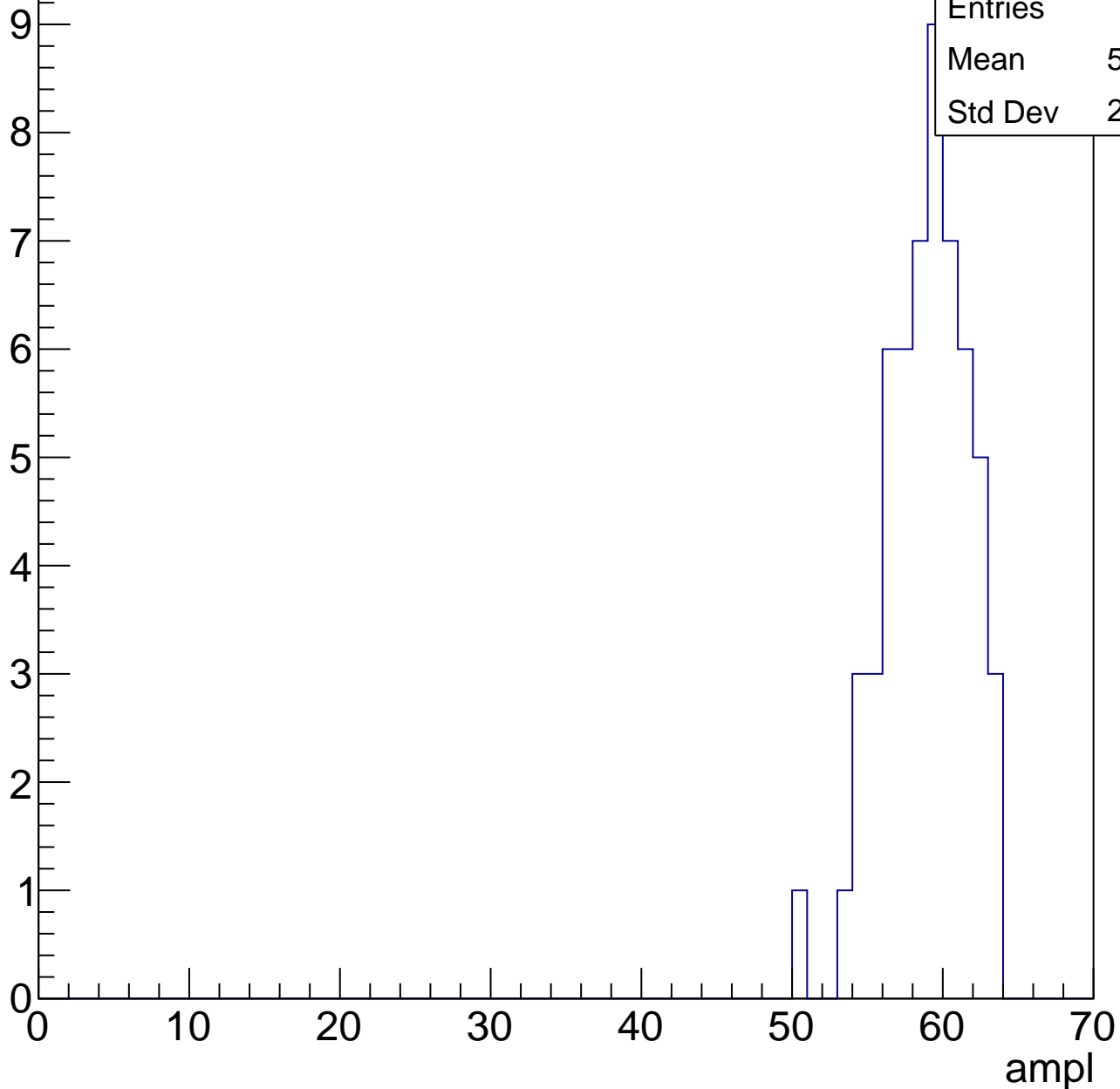


# B1L003S, U11-ch29, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	58.42
Std Dev	2.746

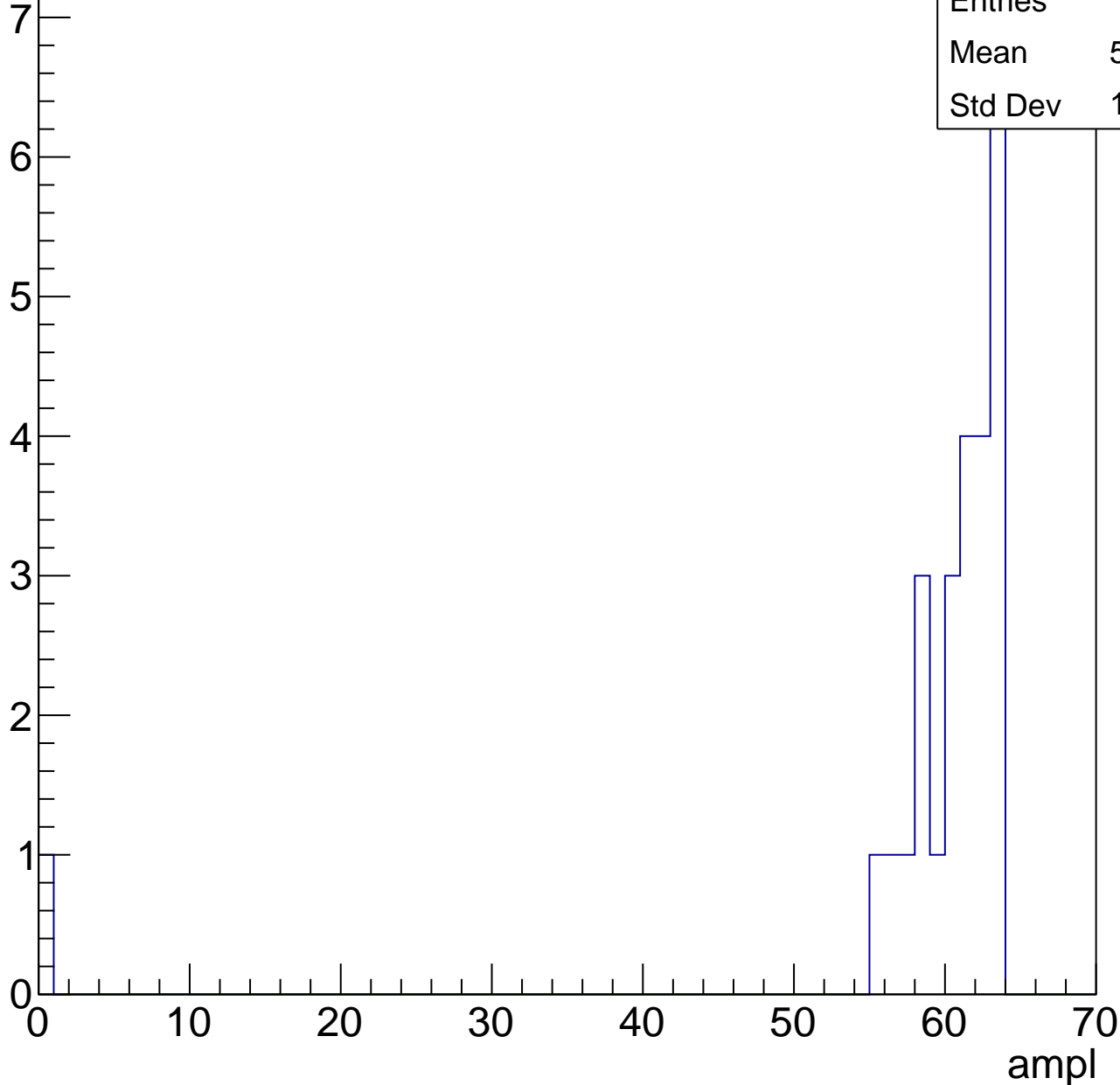


# B1L003S, U11-ch29, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	26
Mean	58.23
Std Dev	11.87



# B1L003S, U11-ch29, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch29, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L003S, U11-ch30, adc0

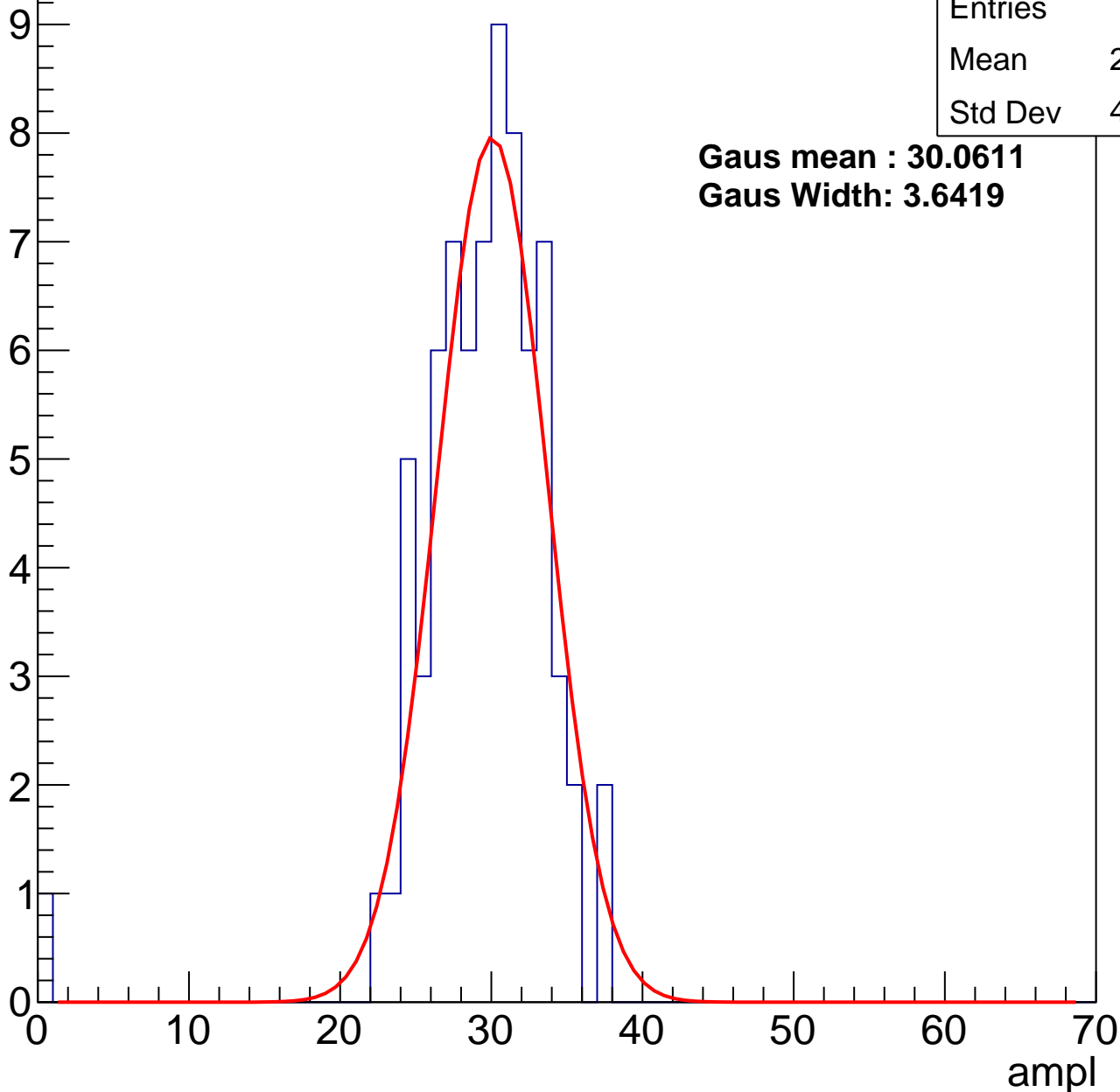
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	74
Mean	28.96
Std Dev	4.749

**Gaus mean : 30.0611**

**Gaus Width: 3.6419**

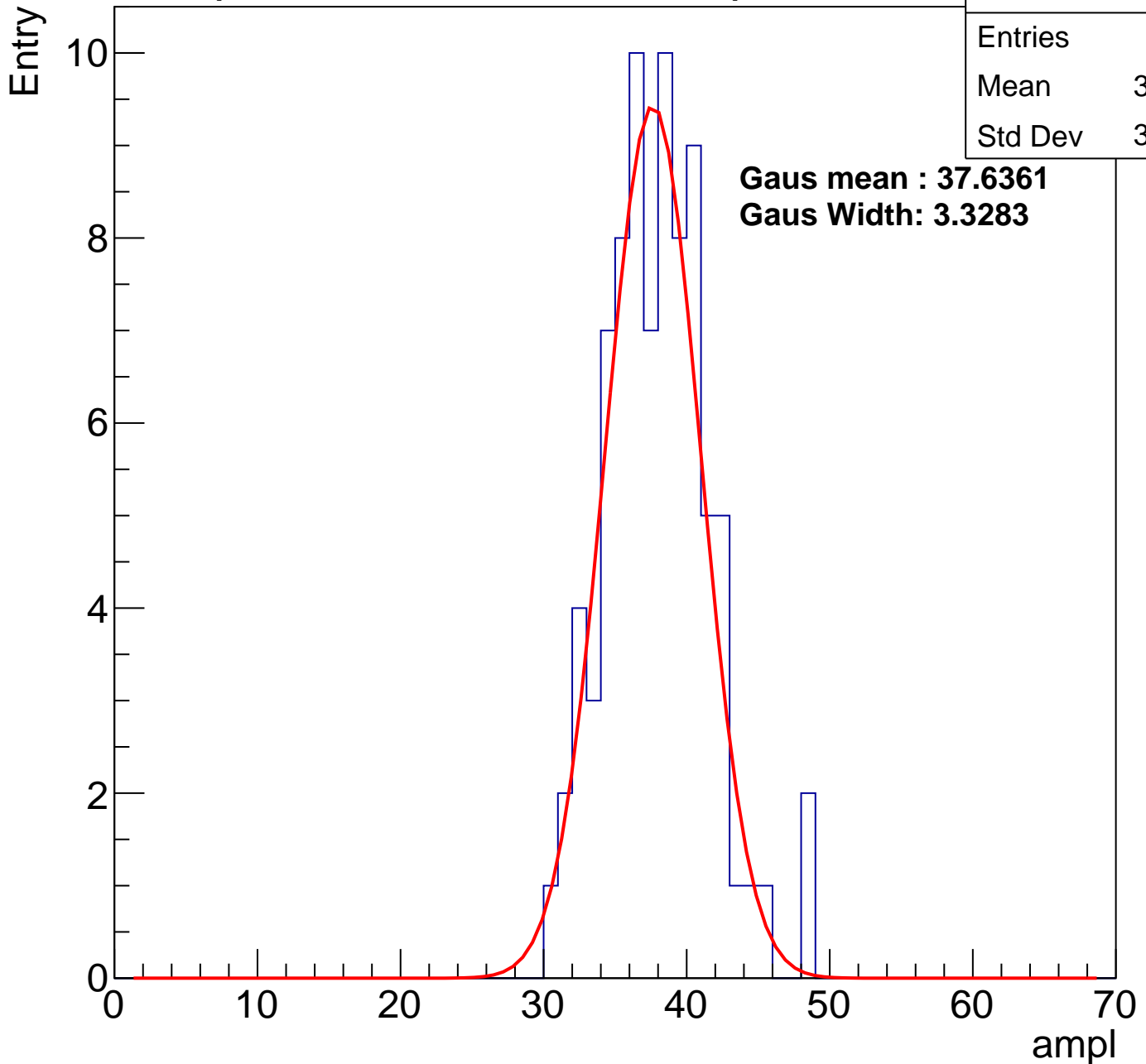


# B1L003S, U11-ch30, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	84
Mean	37.51
Std Dev	3.571

**Gaus mean : 37.6361**  
**Gaus Width: 3.3283**



# B1L003S, U11-ch30, adc2

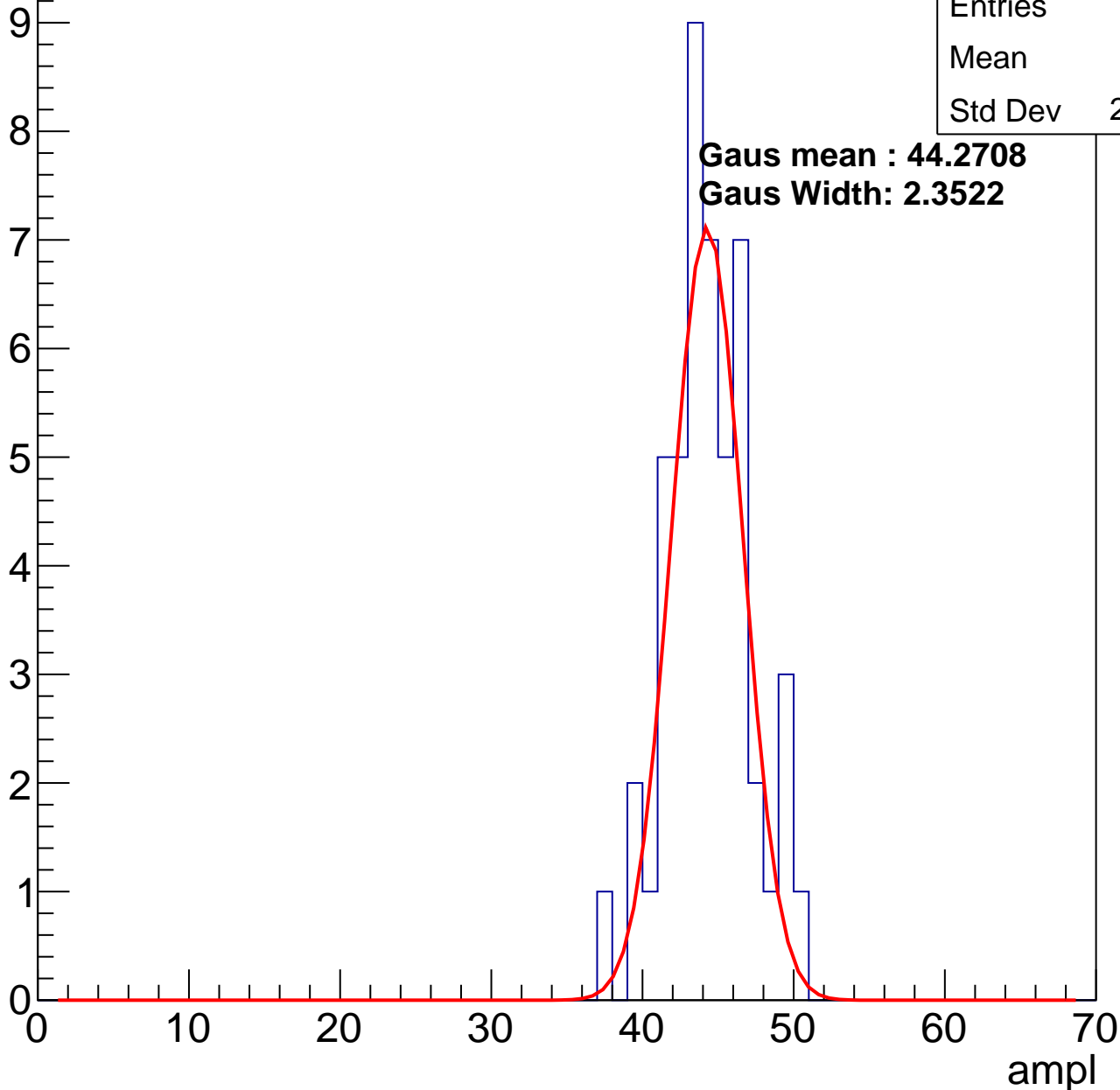
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	49
Mean	43.9
Std Dev	2.735

**Gaus mean : 44.2708**

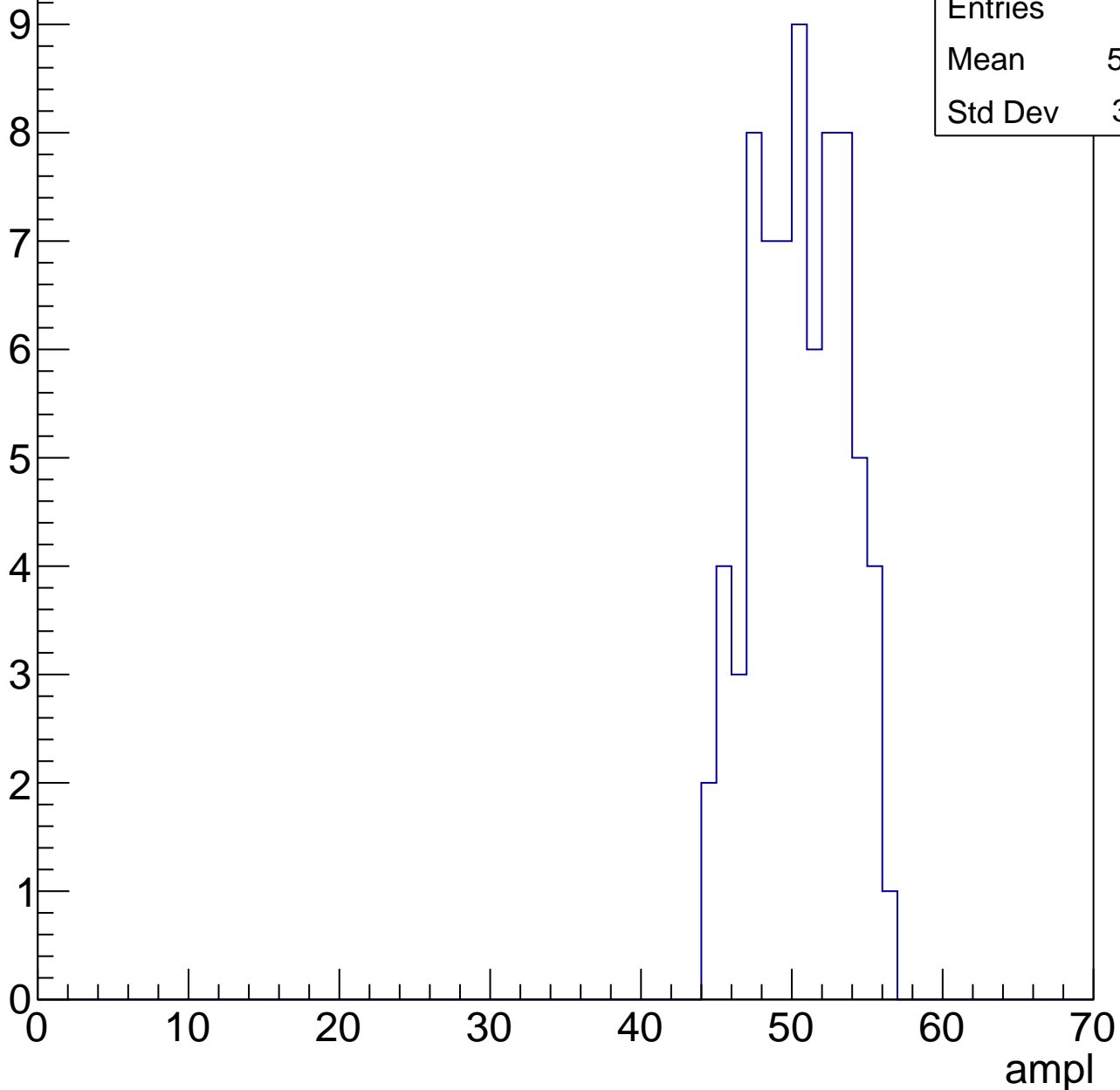
**Gaus Width: 2.3522**



# B1L003S, U11-ch30, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

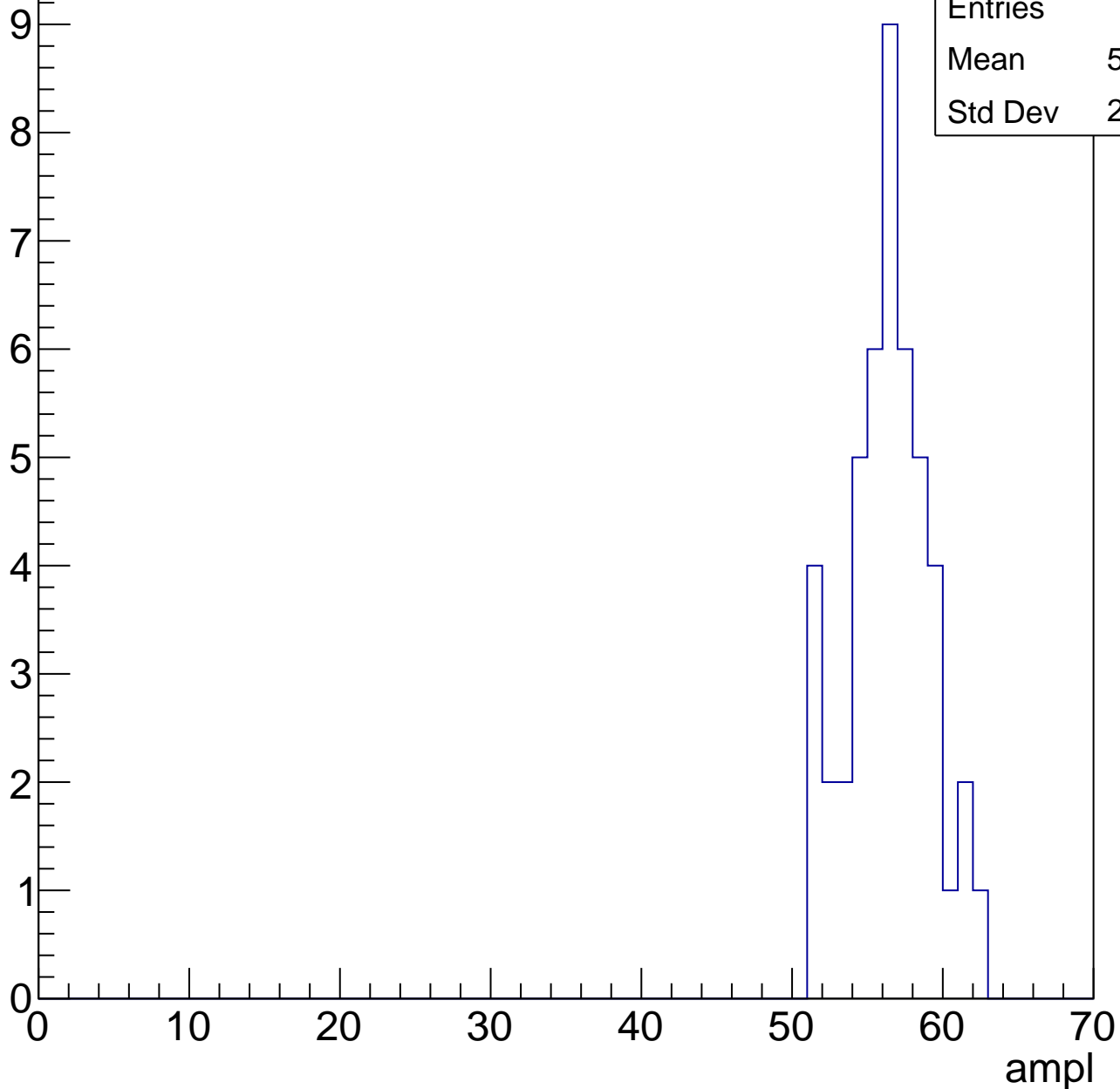


Entries	72
Mean	50.04
Std Dev	3.011

# B1L003S, U11-ch30, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

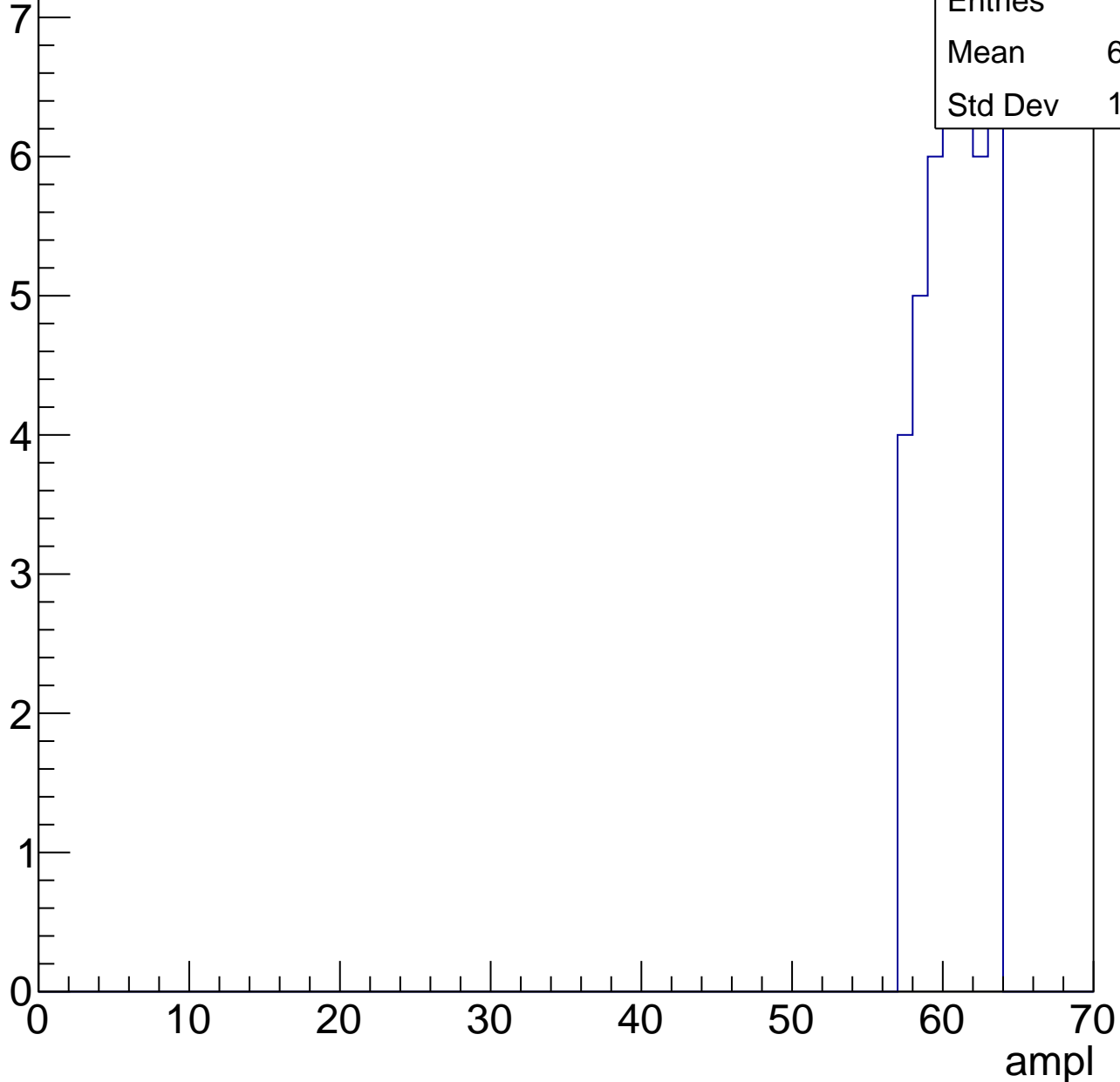
Entry



# B1L003S, U11-ch30, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

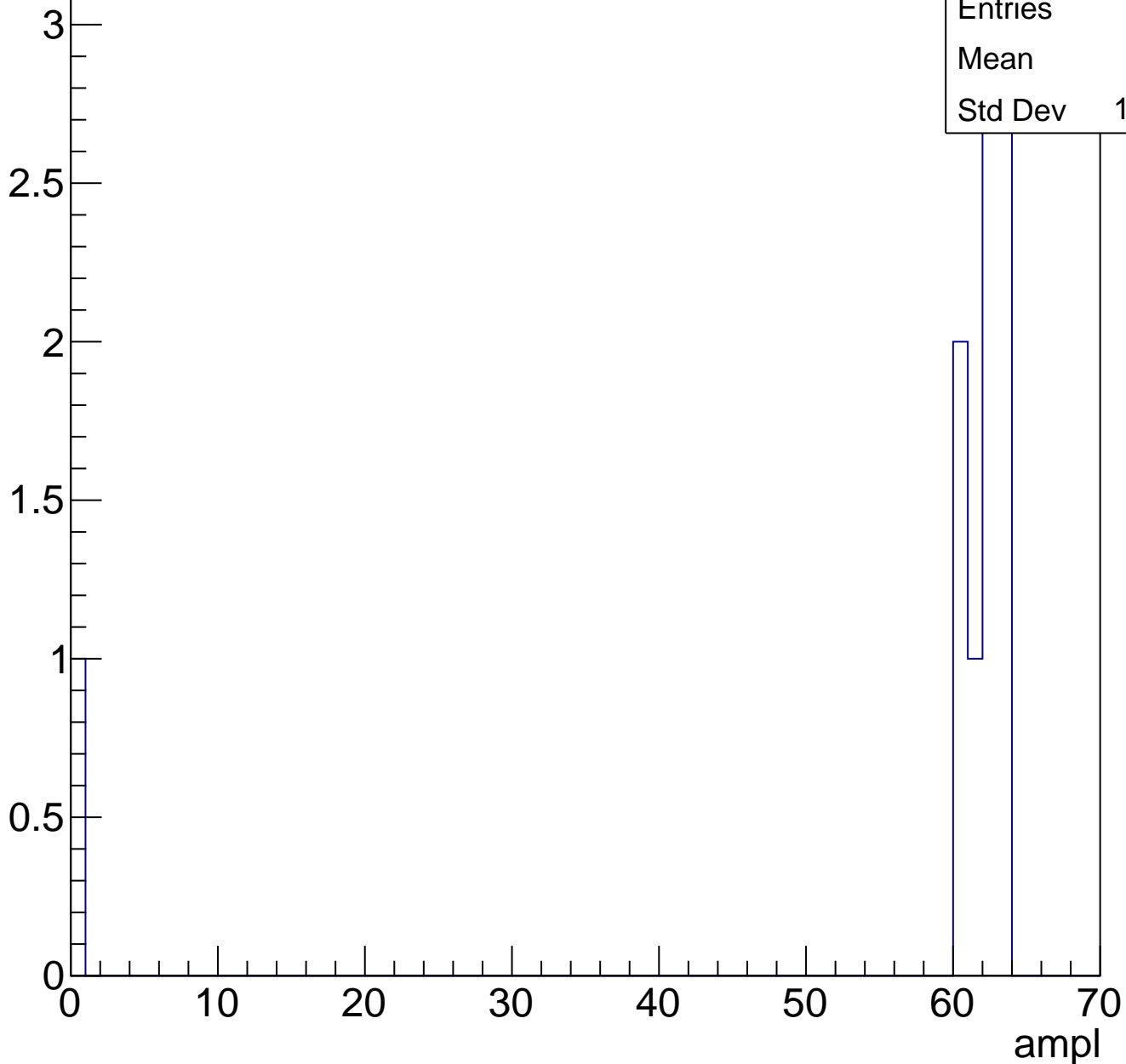
Entry



# B1L003S, U11-ch30, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch30, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	11
Std Dev	11

# B1L003S, U11-ch31, adc0

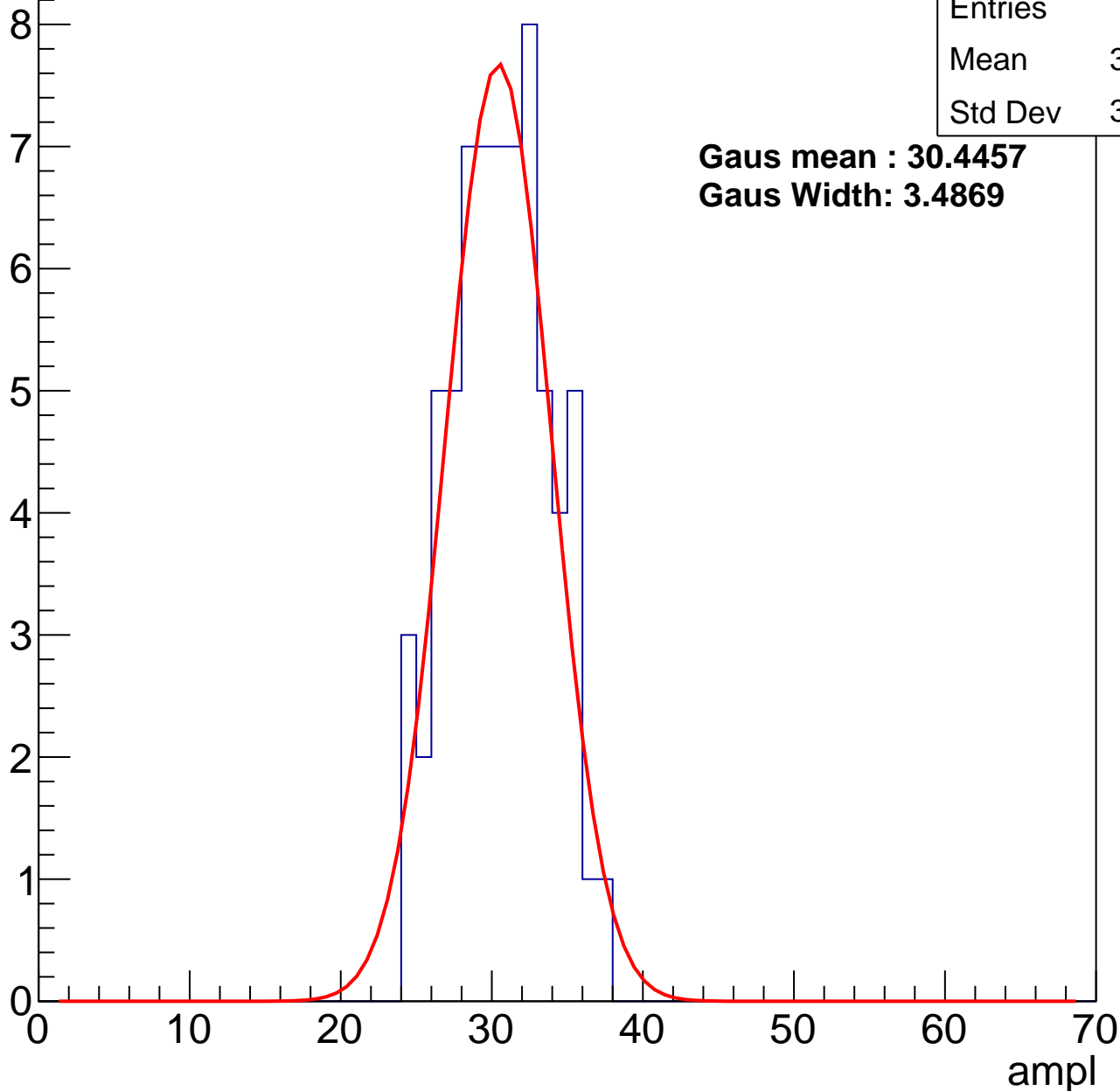
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	30.12
Std Dev	3.174

**Gaus mean : 30.4457**

**Gaus Width: 3.4869**



# B1L003S, U11-ch31, adc1

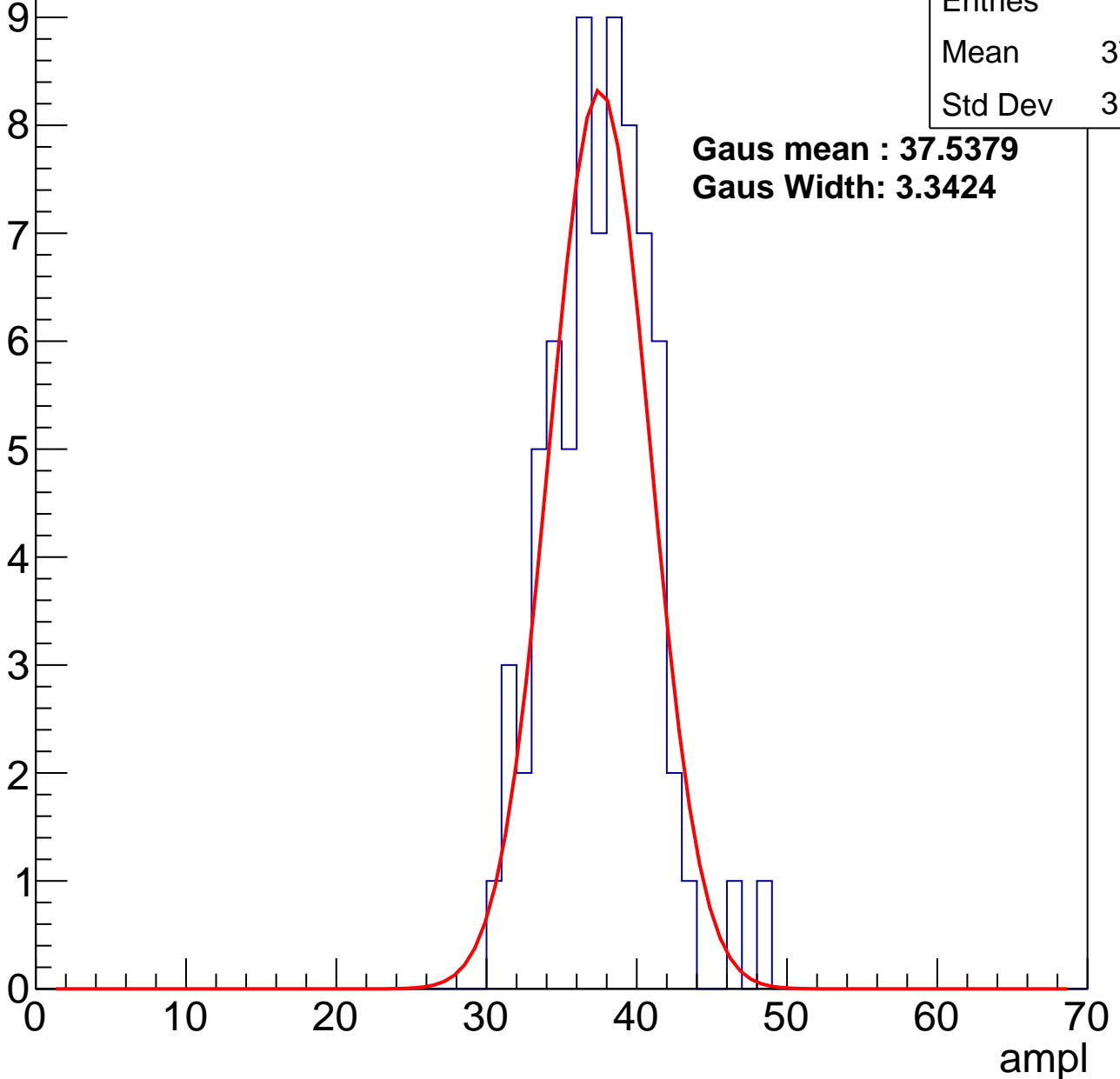
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	73
Mean	37.19
Std Dev	3.423

**Gaus mean : 37.5379**

**Gaus Width: 3.3424**



# B1L003S, U11-ch31, adc2

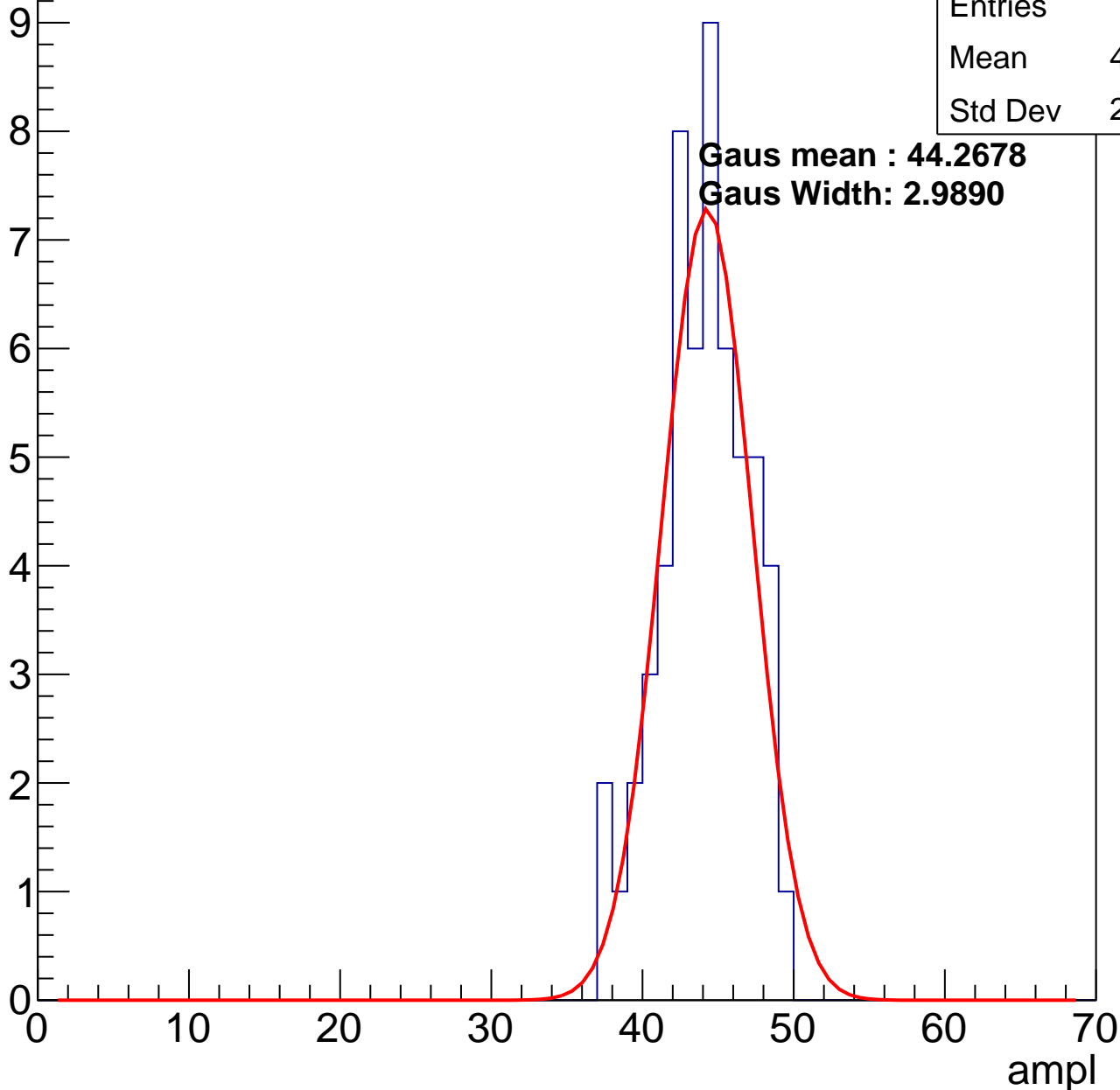
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	43.57
Std Dev	2.853

**Gaus mean : 44.2678**

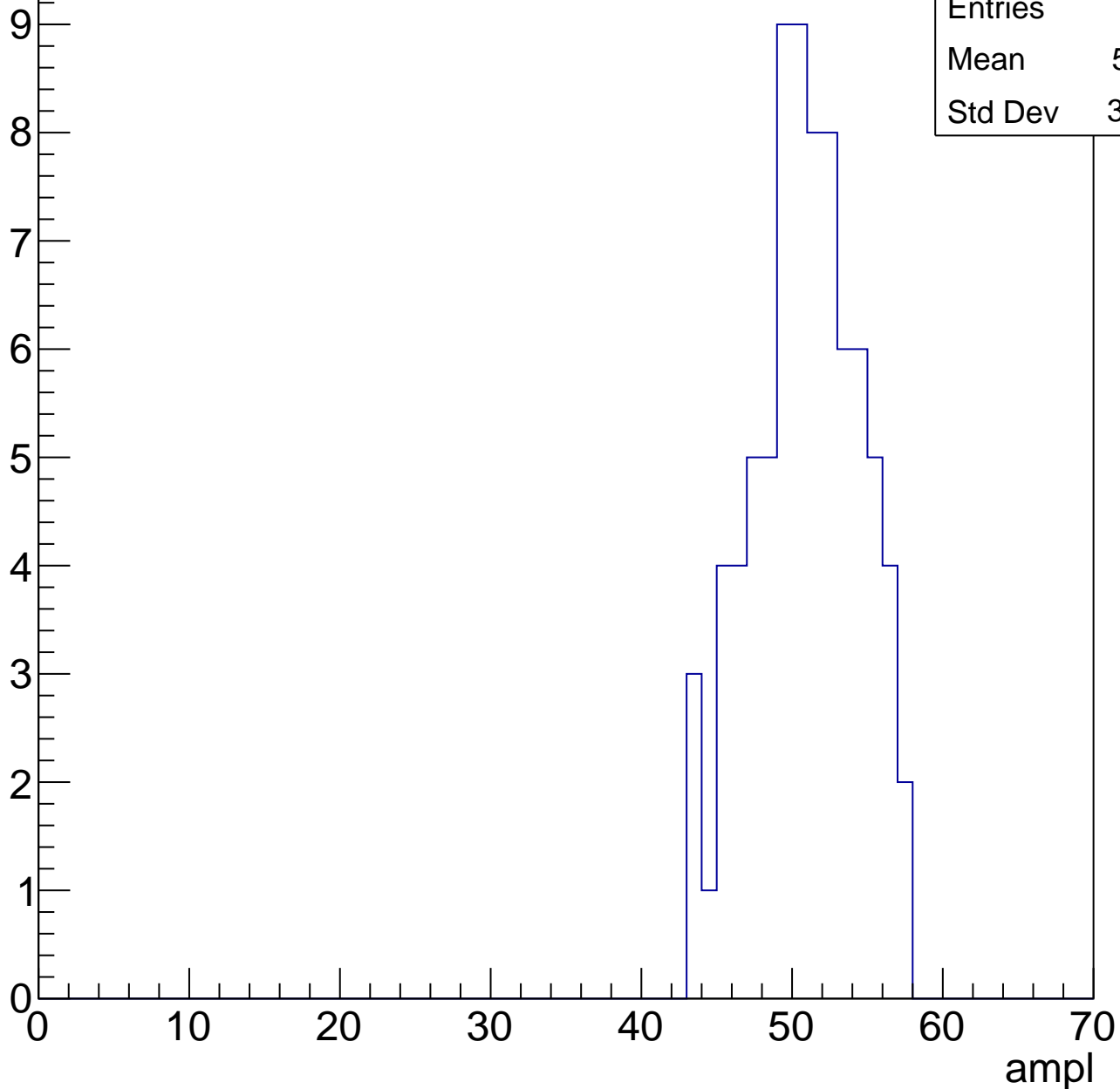
**Gaus Width: 2.9890**



# B1L003S, U11-ch31, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

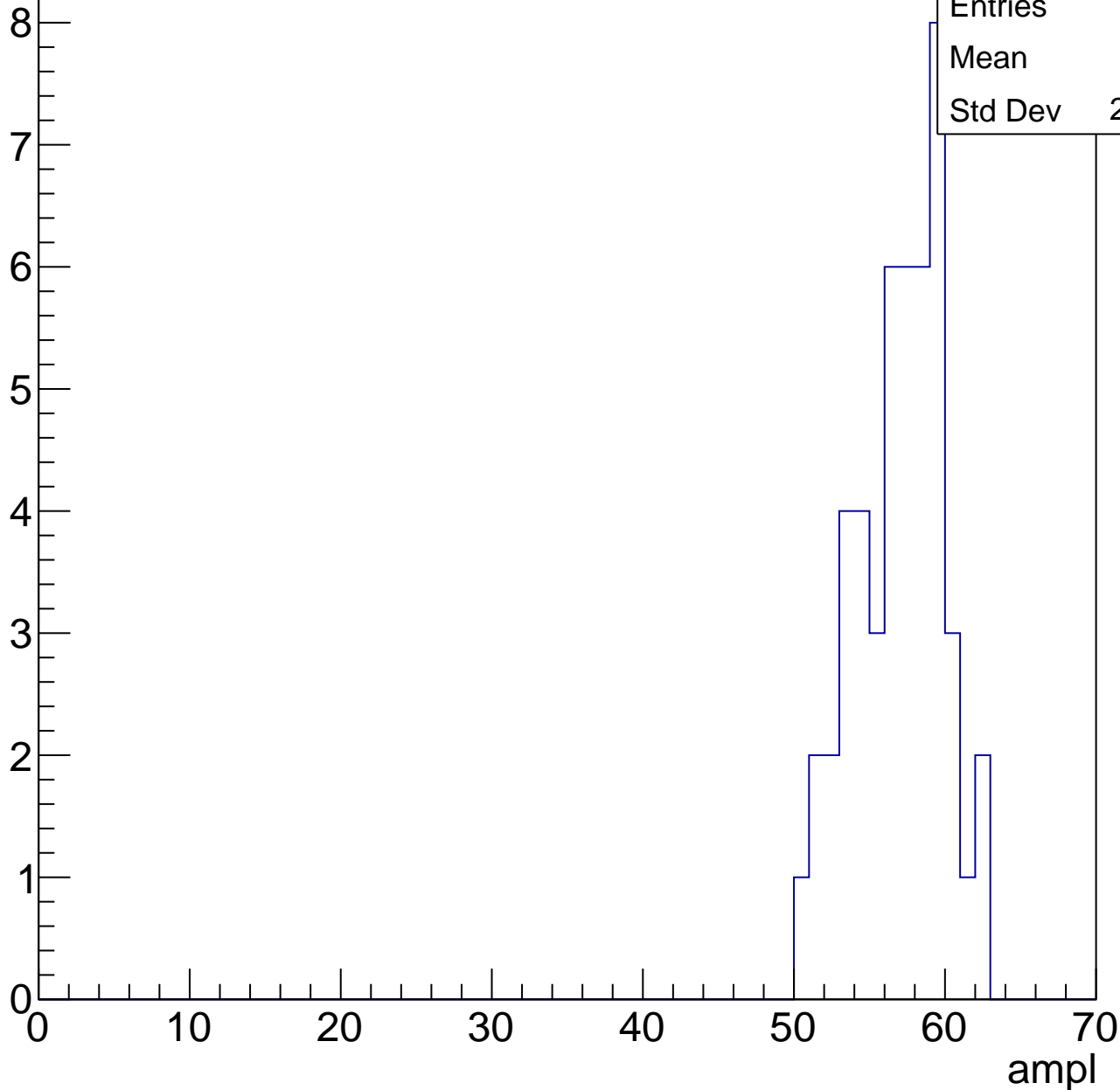


# B1L003S, U11-ch31, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	48
Mean	56.5
Std Dev	2.915

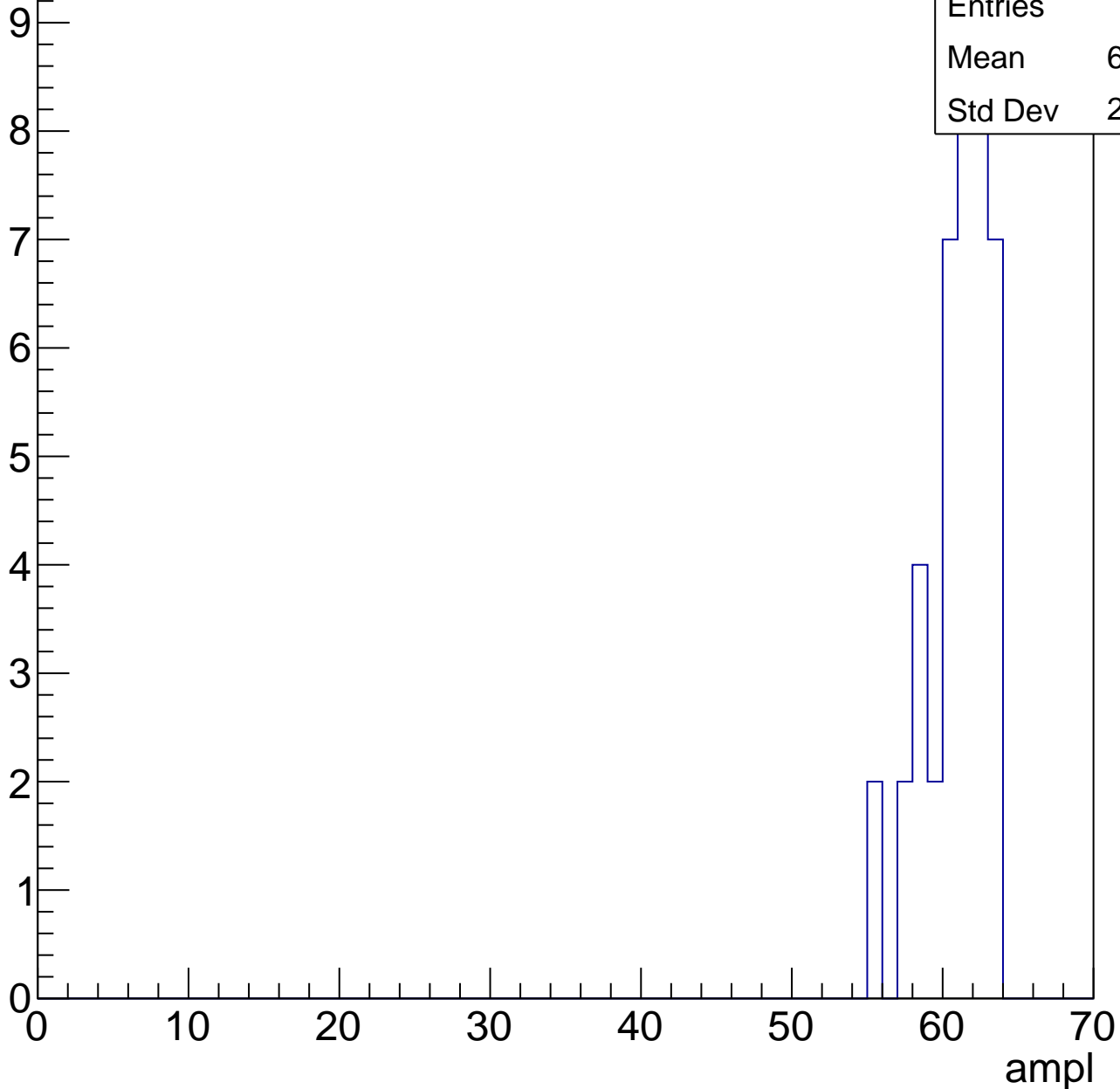


# B1L003S, U11-ch31, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

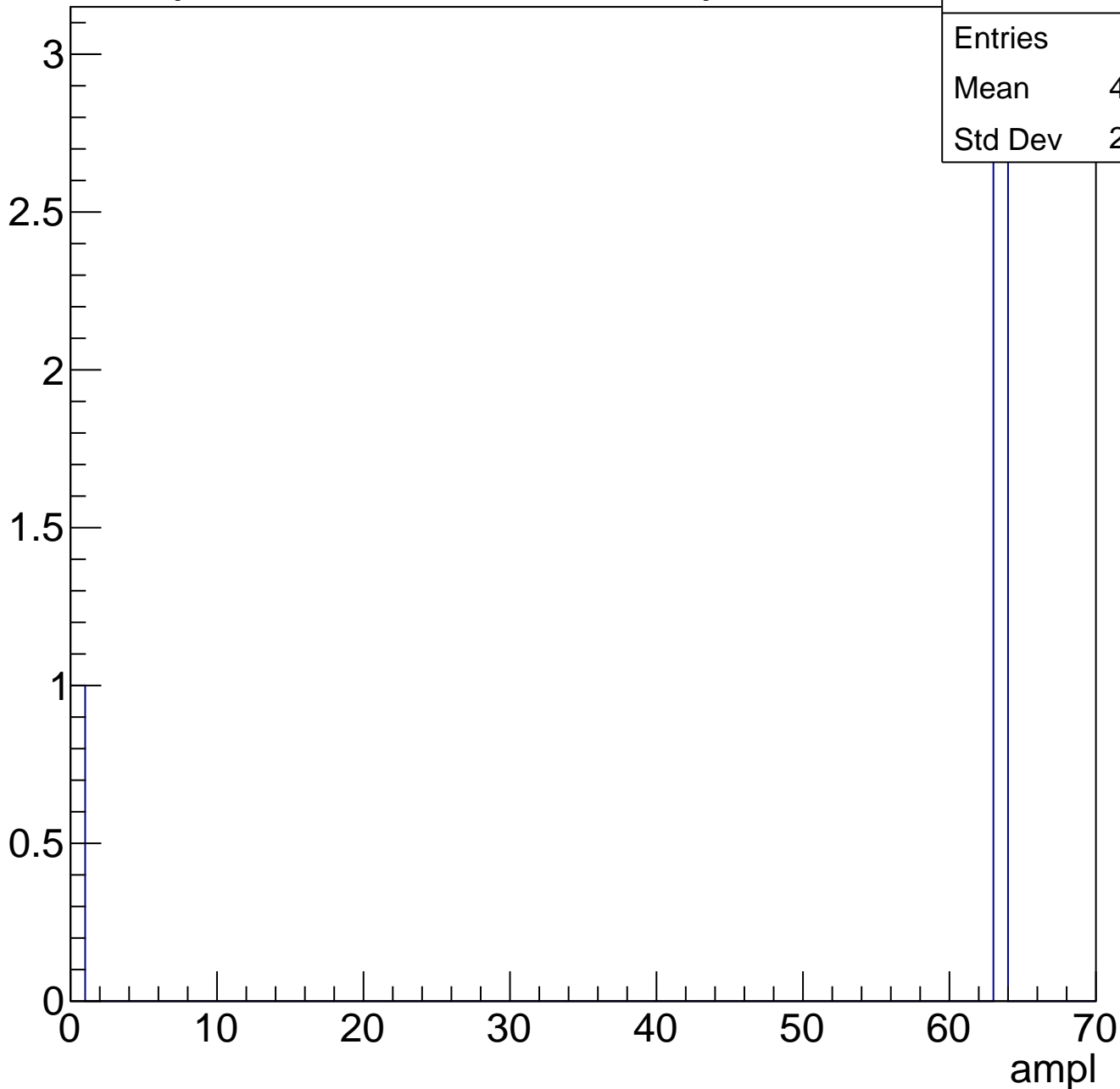
Entries	41
Mean	60.49
Std Dev	2.097



# B1L003S, U11-ch31, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

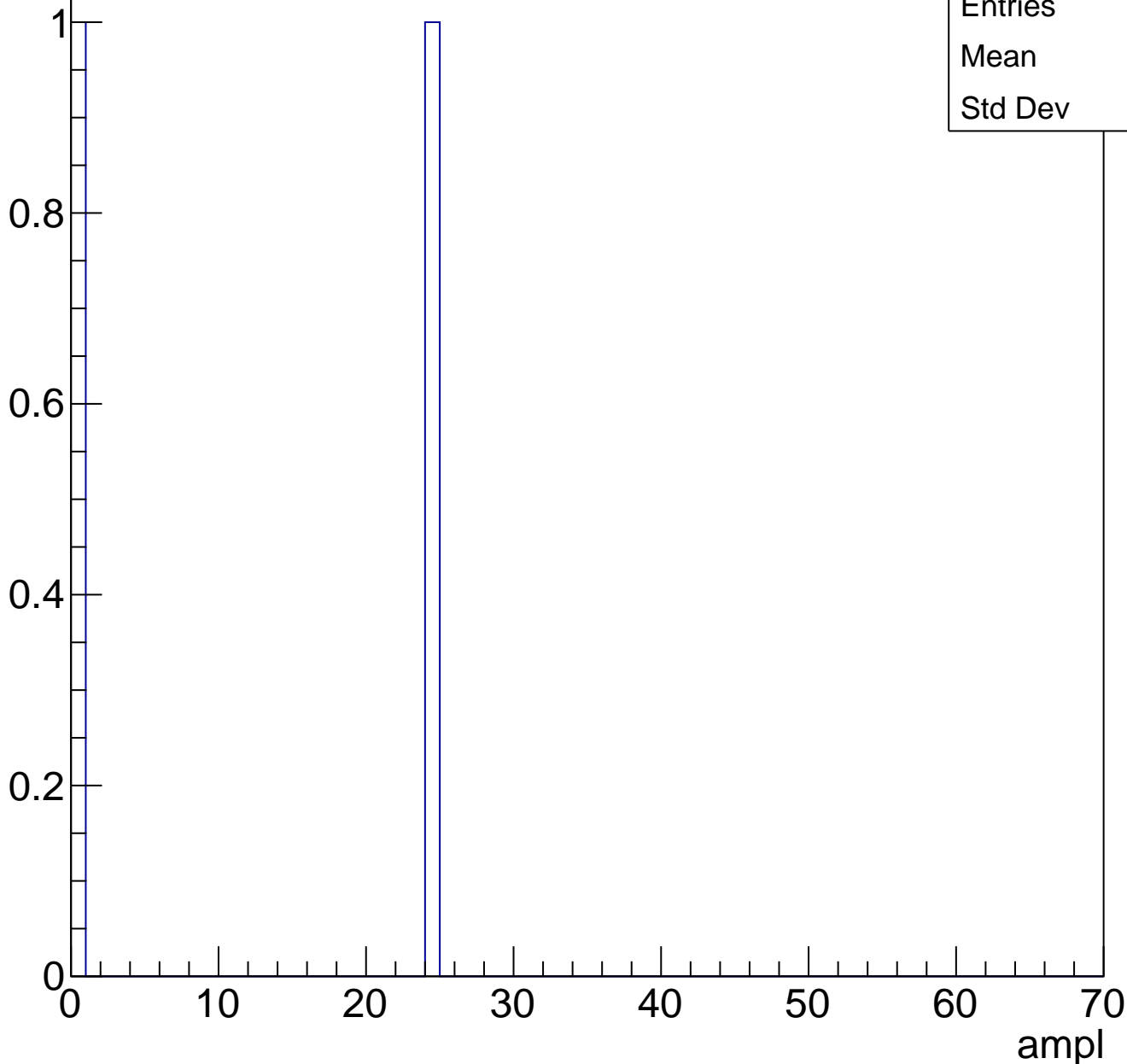




# B1L003S, U11-ch31, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U11-ch32, adc0

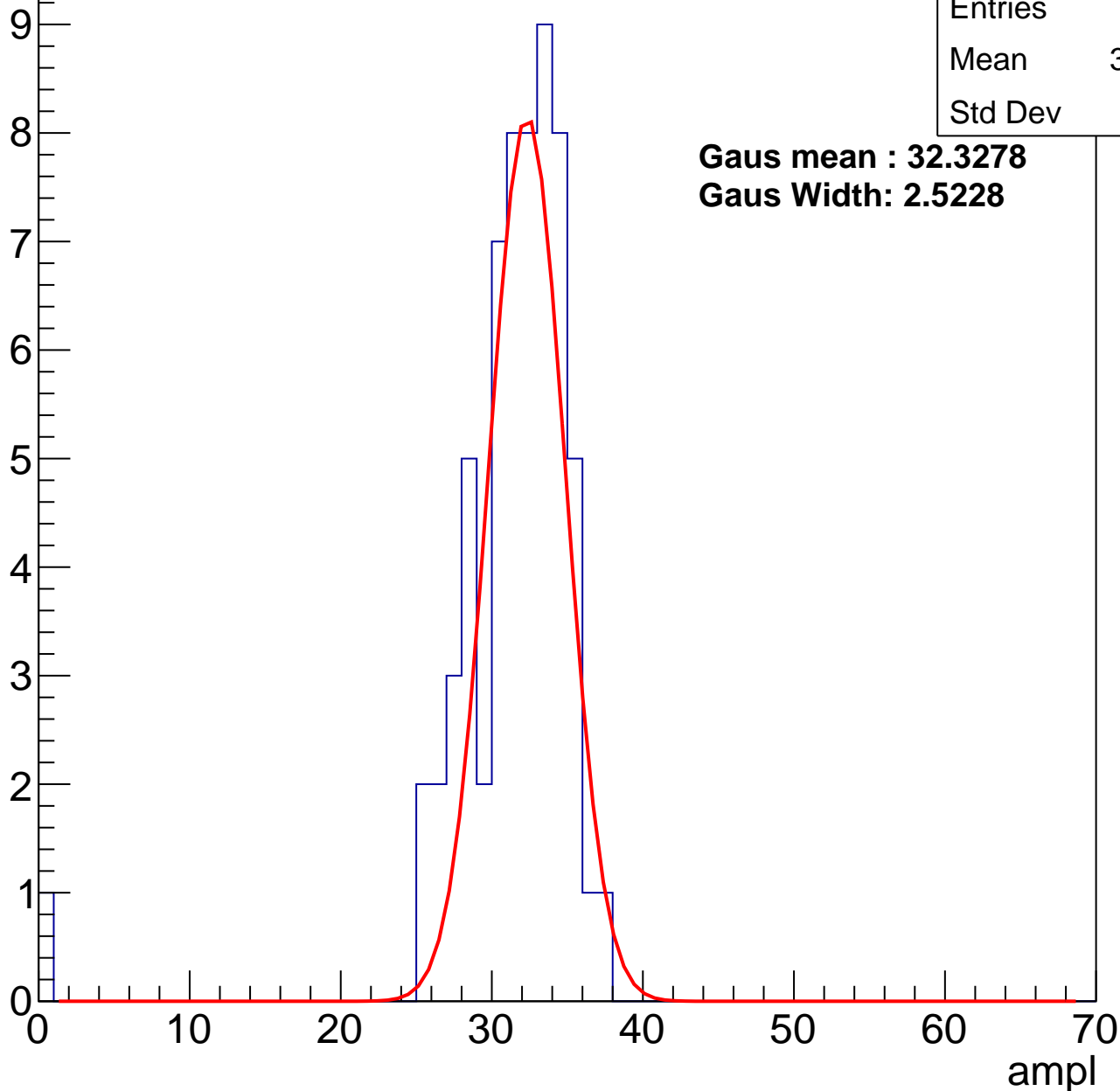
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	30.84
Std Dev	4.83

**Gaus mean : 32.3278**

**Gaus Width: 2.5228**



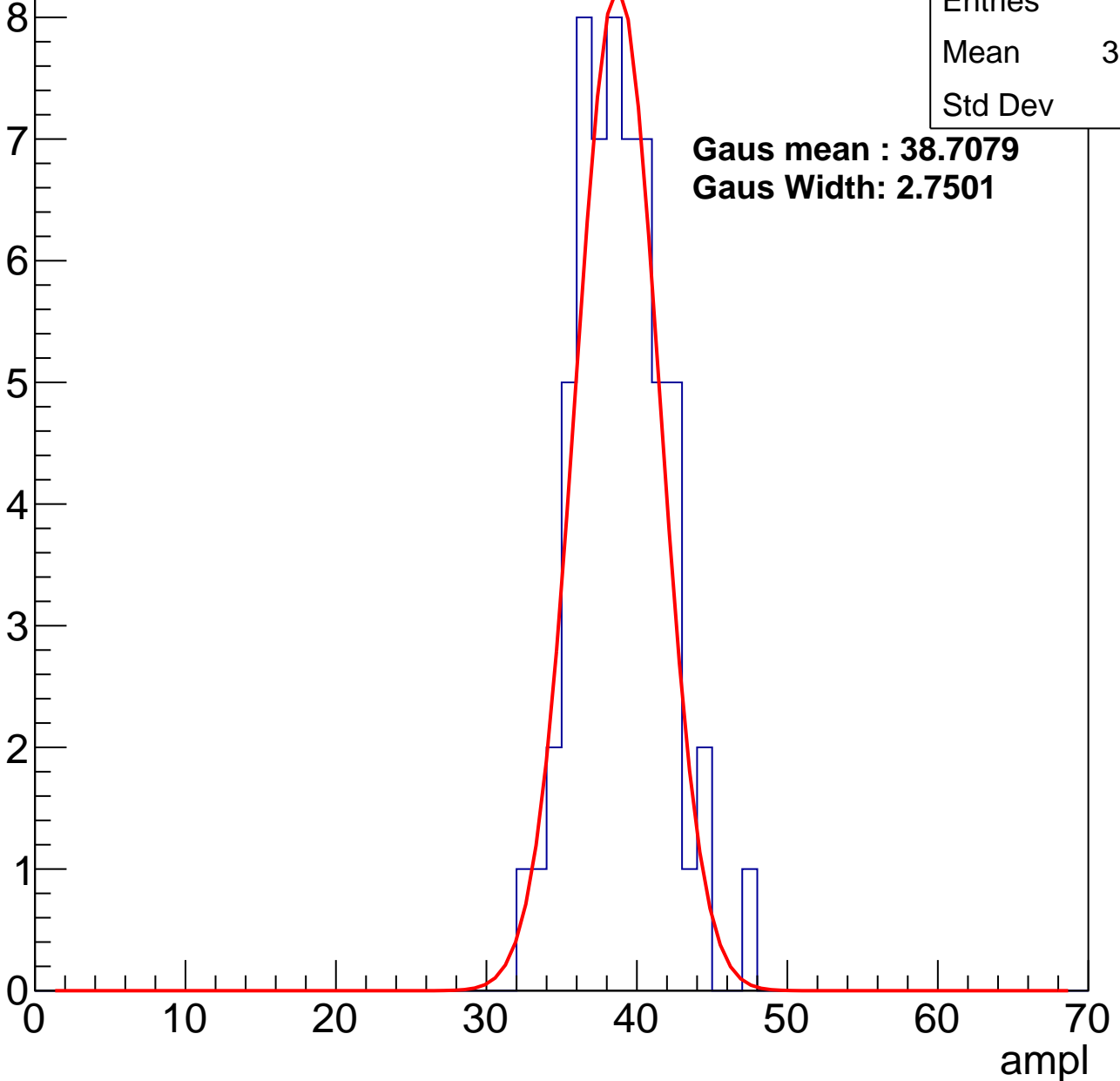
# B1L003S, U11-ch32, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	38.42
Std Dev	2.9

**Gaus mean : 38.7079**  
**Gaus Width: 2.7501**



# B1L003S, U11-ch32, adc2

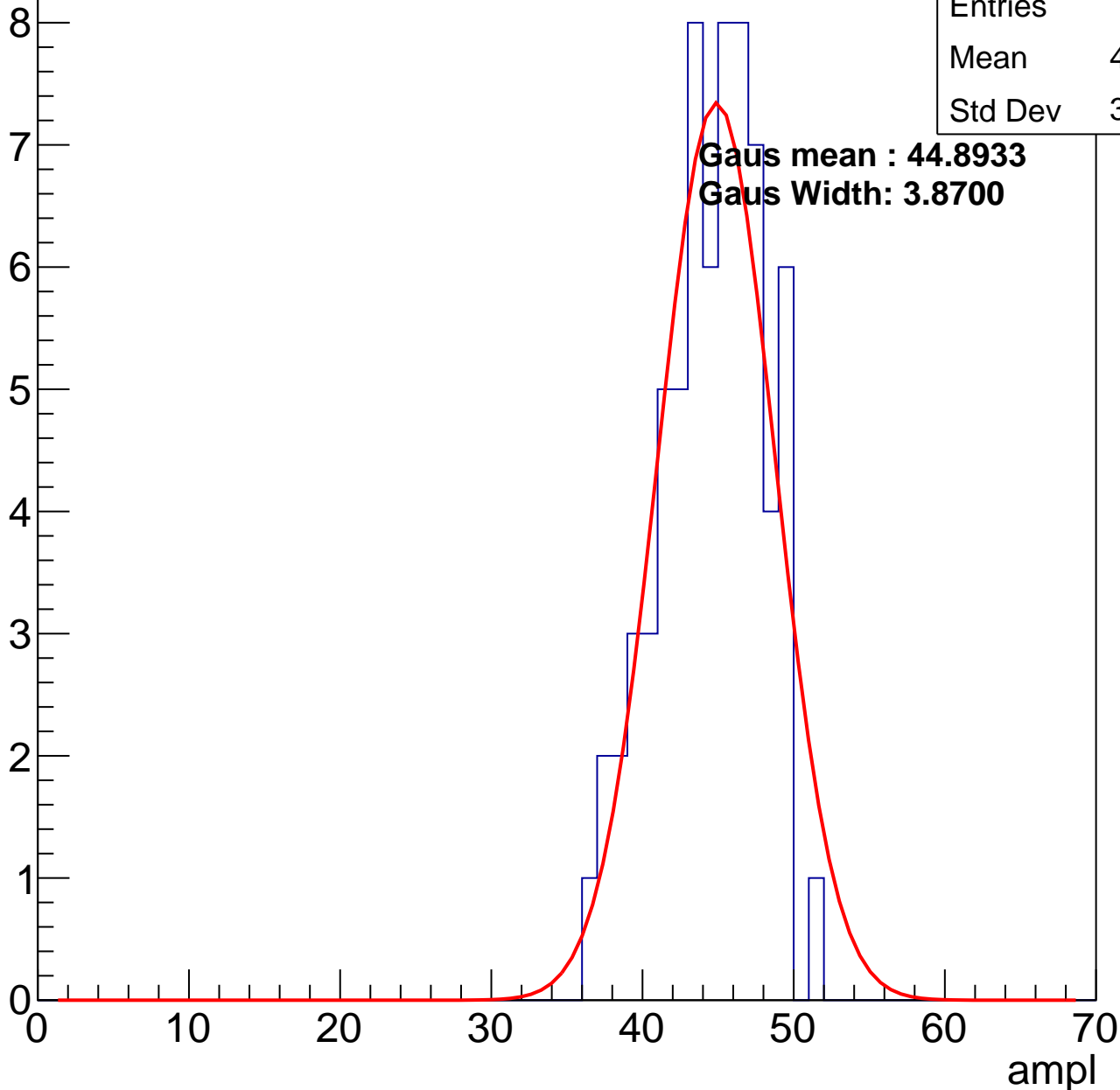
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	44.06
Std Dev	3.396

**Gaus mean : 44.8933**

**Gaus Width: 3.8700**

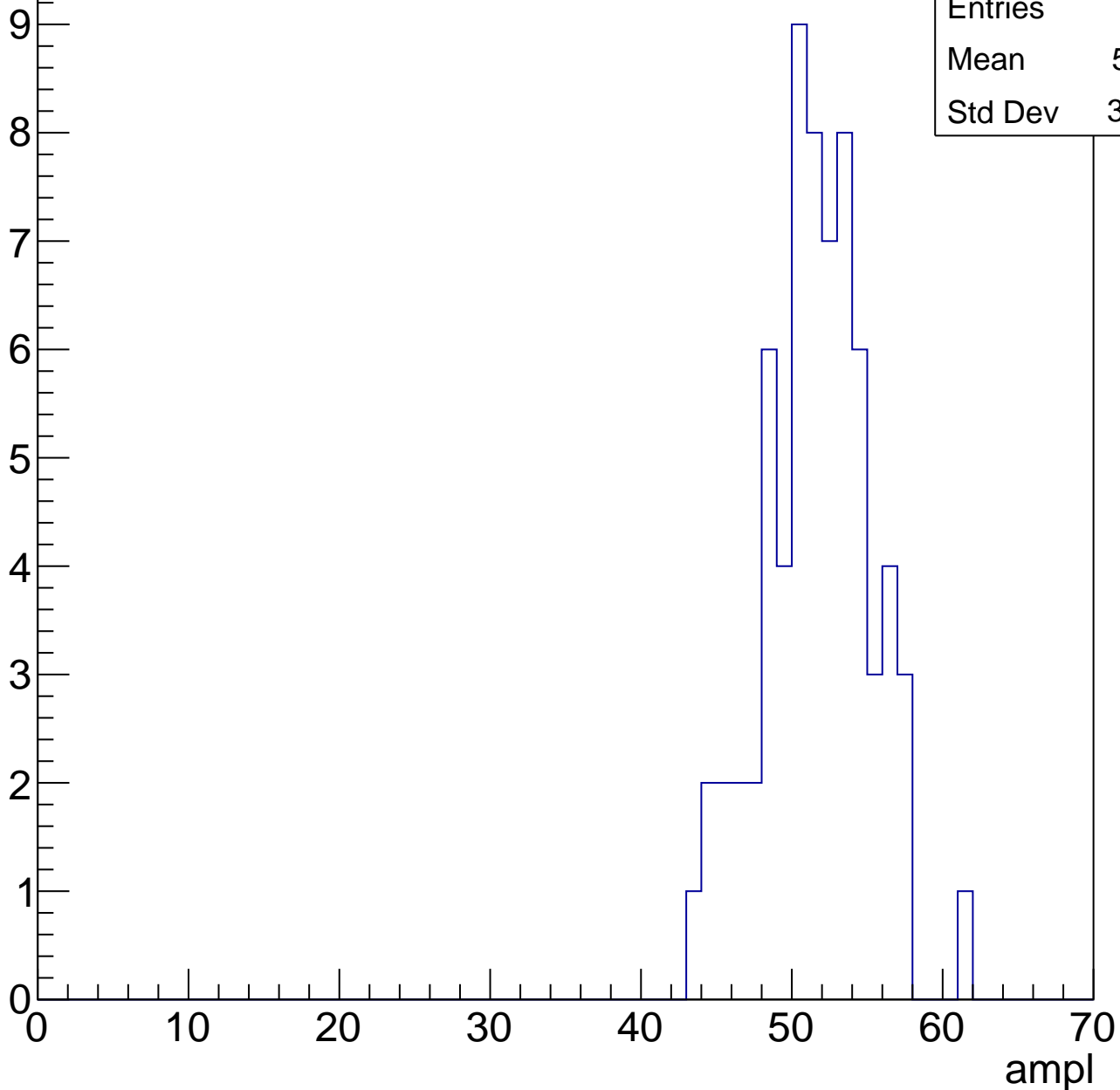


# B1L003S, U11-ch32, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	51.21
Std Dev	3.517

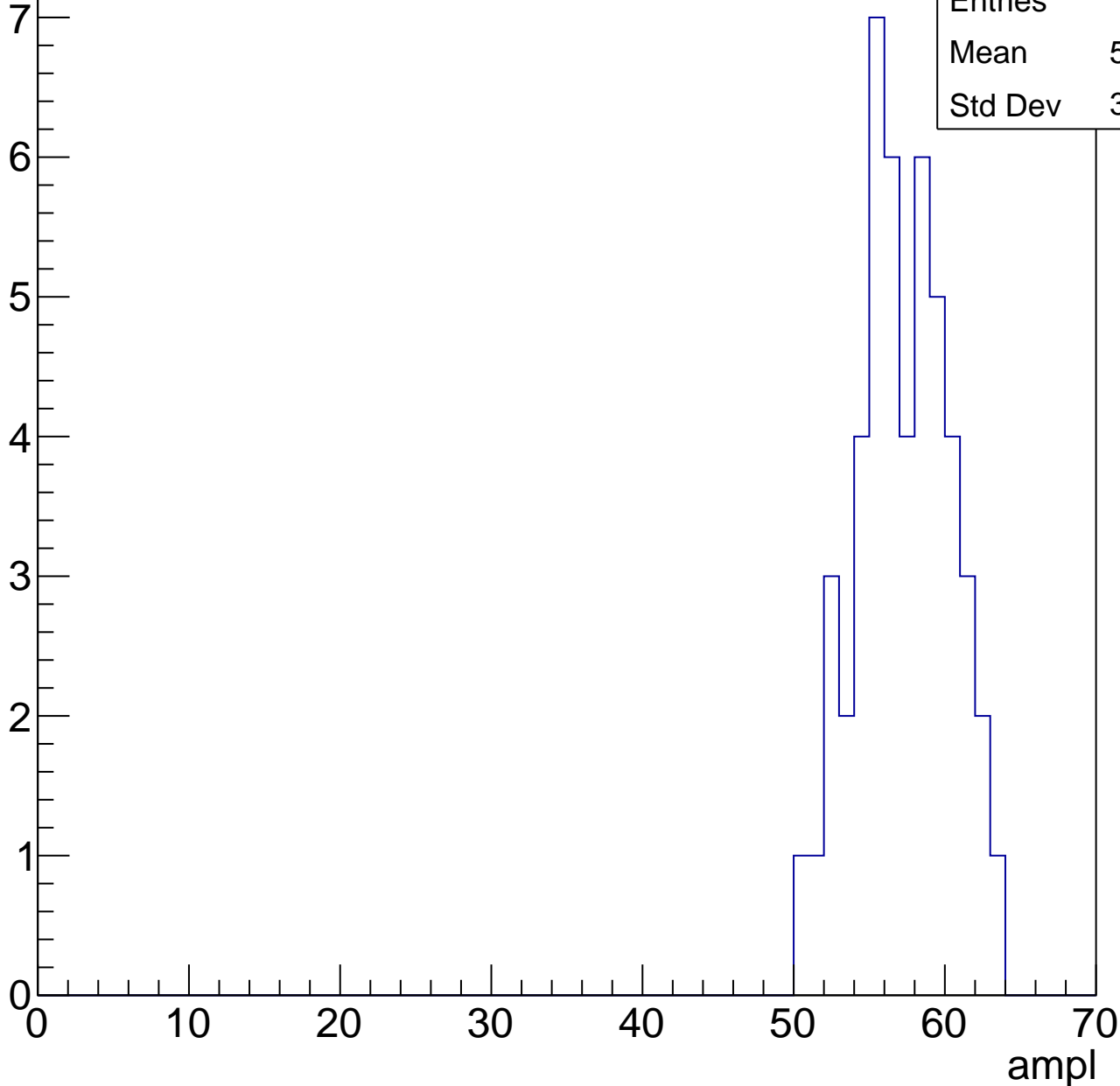


# B1L003S, U11-ch32, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	49
Mean	56.76
Std Dev	3.047

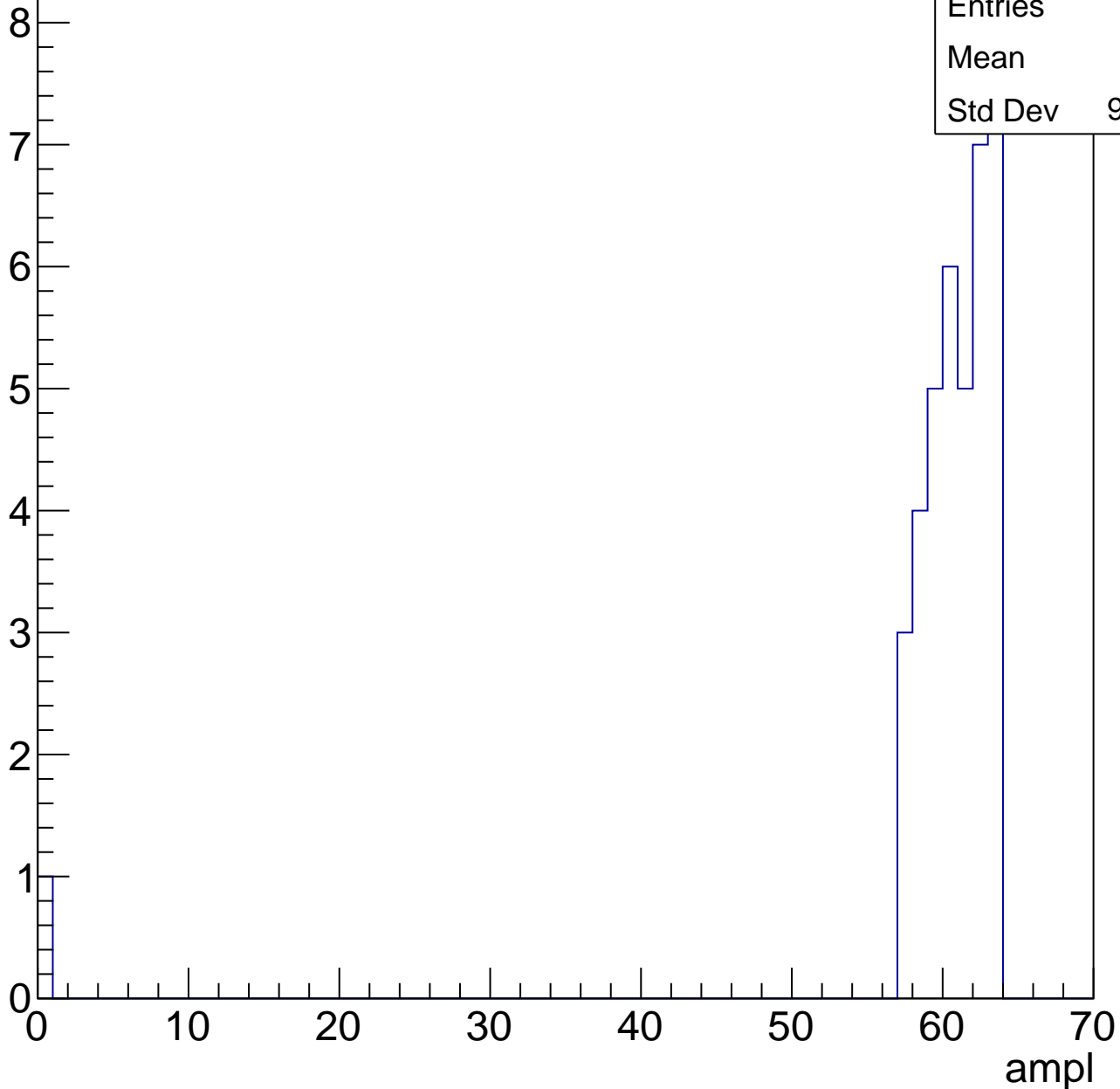


# B1L003S, U11-ch32, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	39
Mean	59
Std Dev	9.759



# B1L003S, U11-ch32, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

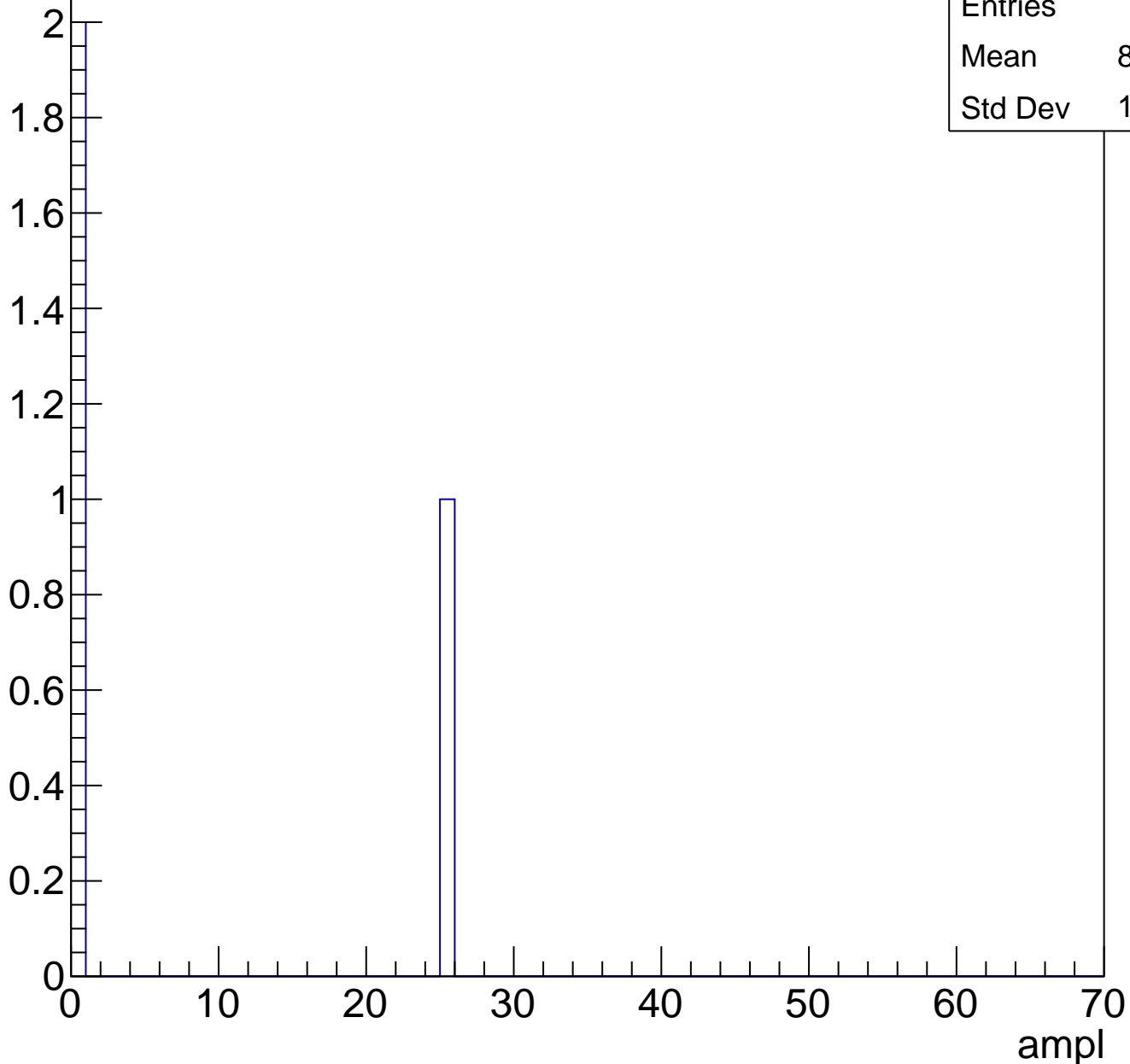




# B1L003S, U11-ch32, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	3
Mean	8.333
Std Dev	11.79

# B1L003S, U11-ch33, adc0

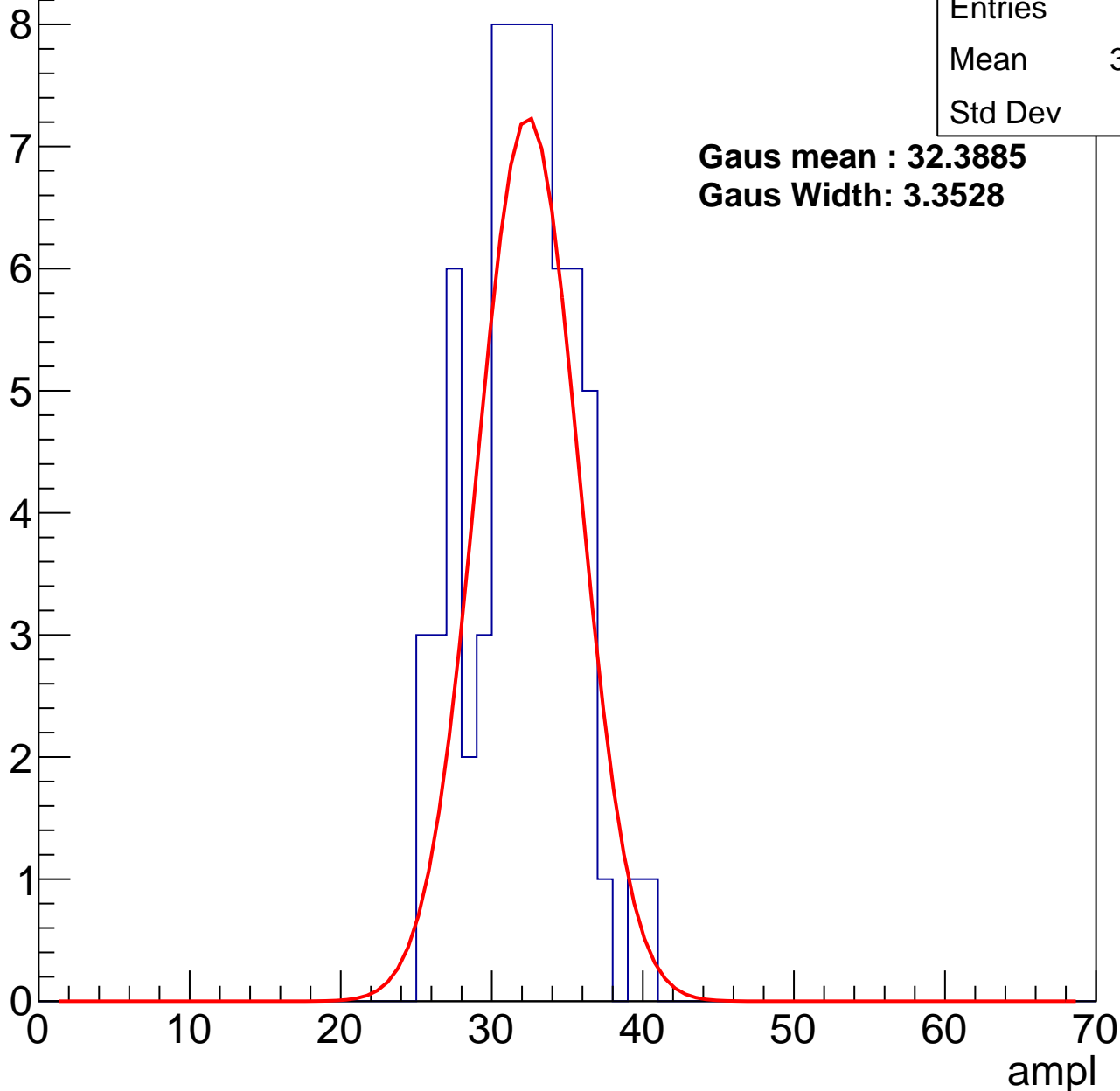
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	31.54
Std Dev	3.39

**Gaus mean : 32.3885**

**Gaus Width: 3.3528**



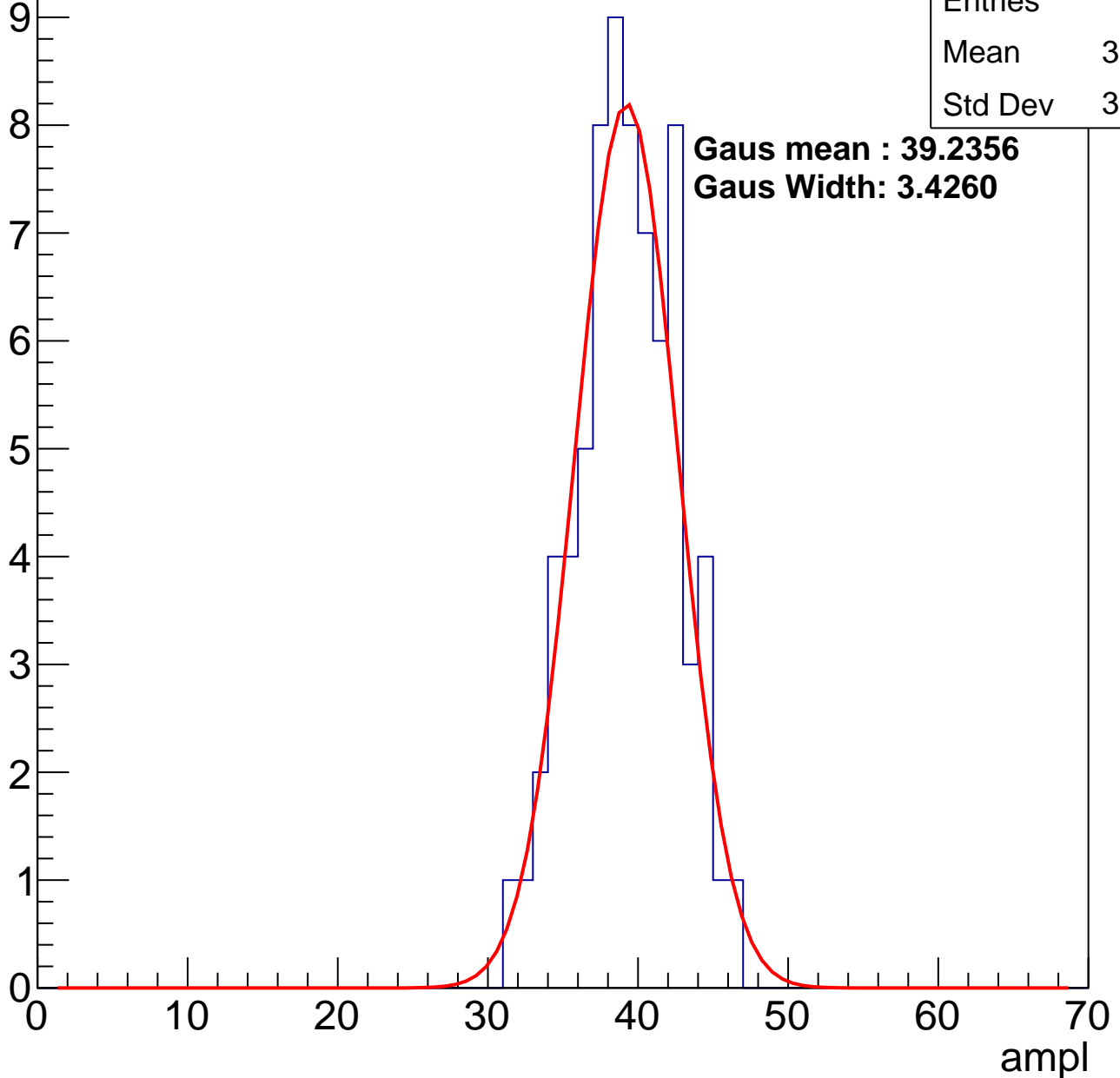
# B1L003S, U11-ch33, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	72
Mean	38.79
Std Dev	3.266

**Gaus mean : 39.2356**  
**Gaus Width: 3.4260**



# B1L003S, U11-ch33, adc2

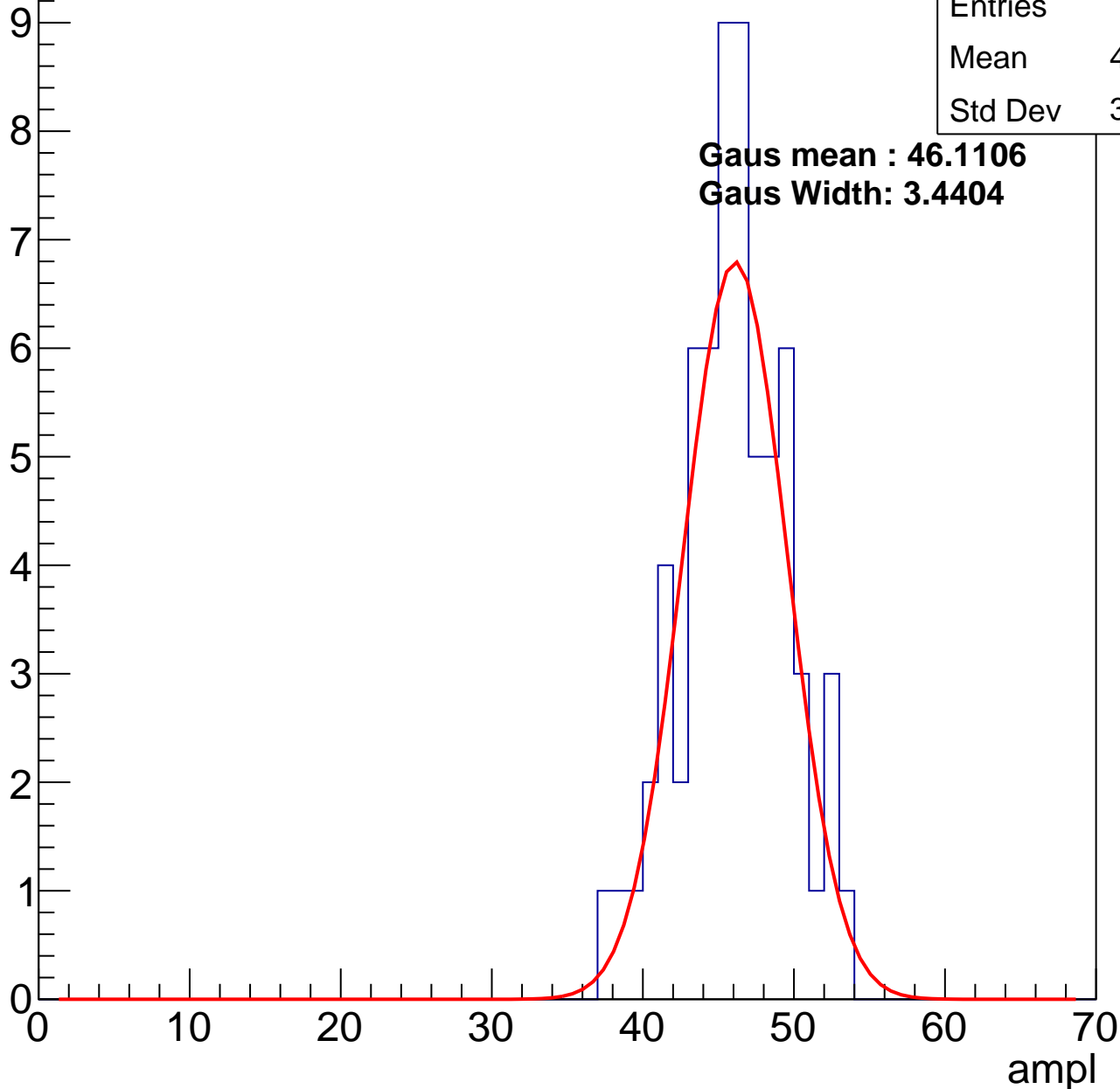
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	45.57
Std Dev	3.468

**Gaus mean : 46.1106**

**Gaus Width: 3.4404**

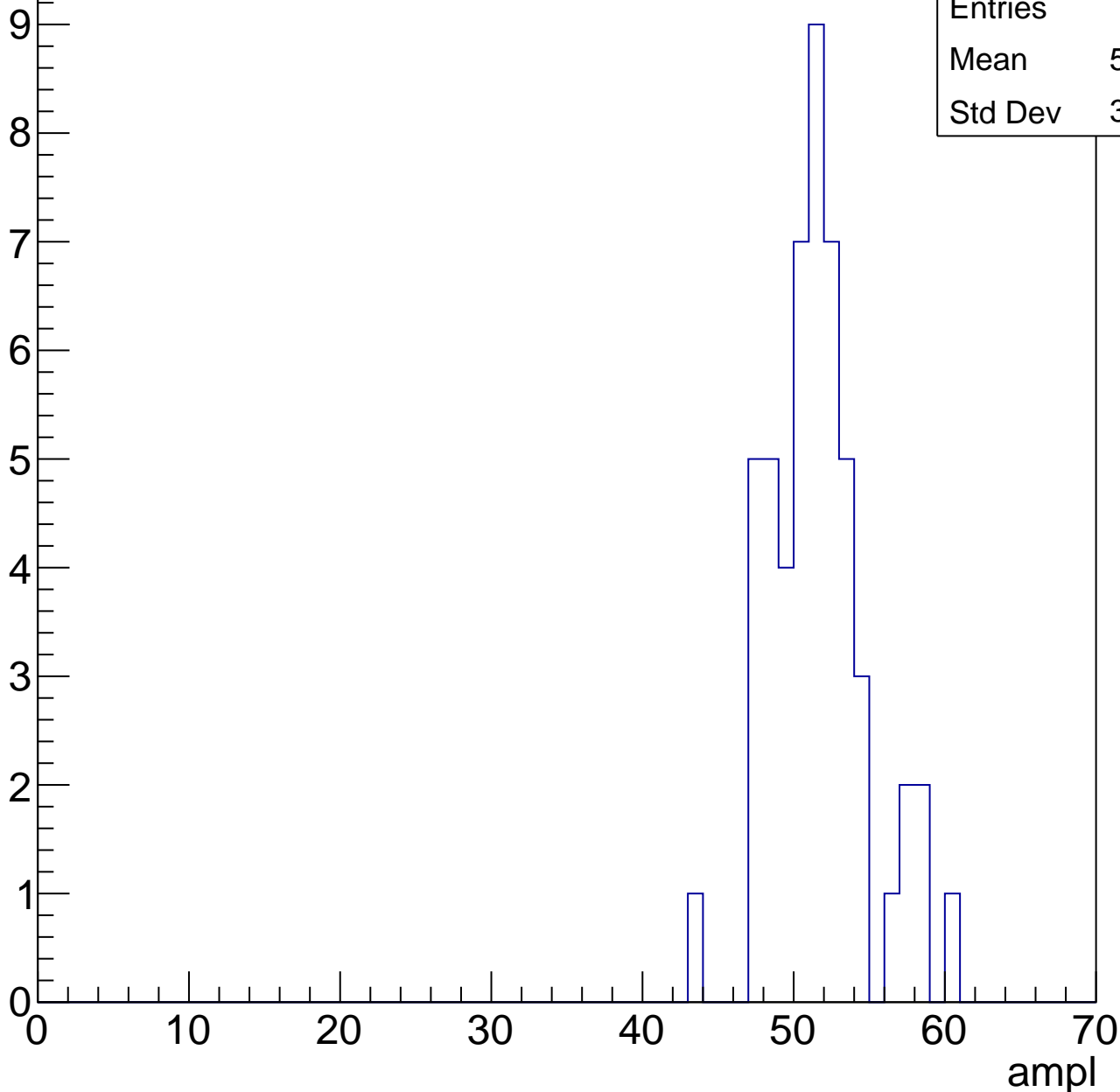


# B1L003S, U11-ch33, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	52
Mean	51.15
Std Dev	3.225



# B1L003S, U11-ch33, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

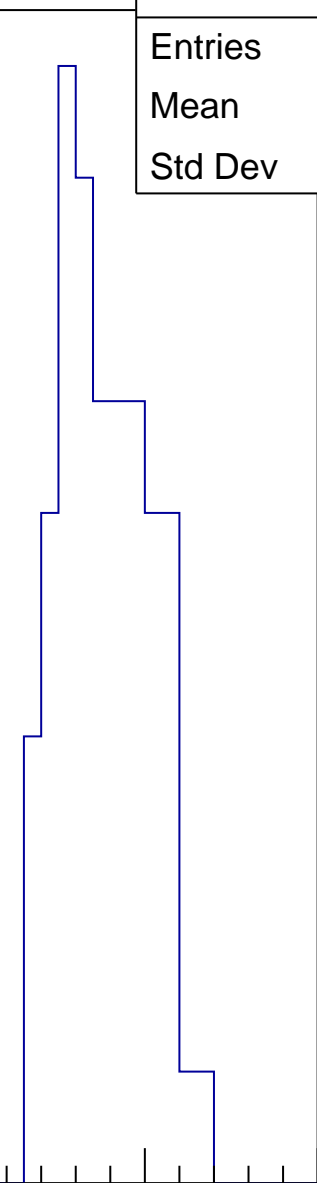
Entries	64
Mean	57.17
Std Dev	2.534

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

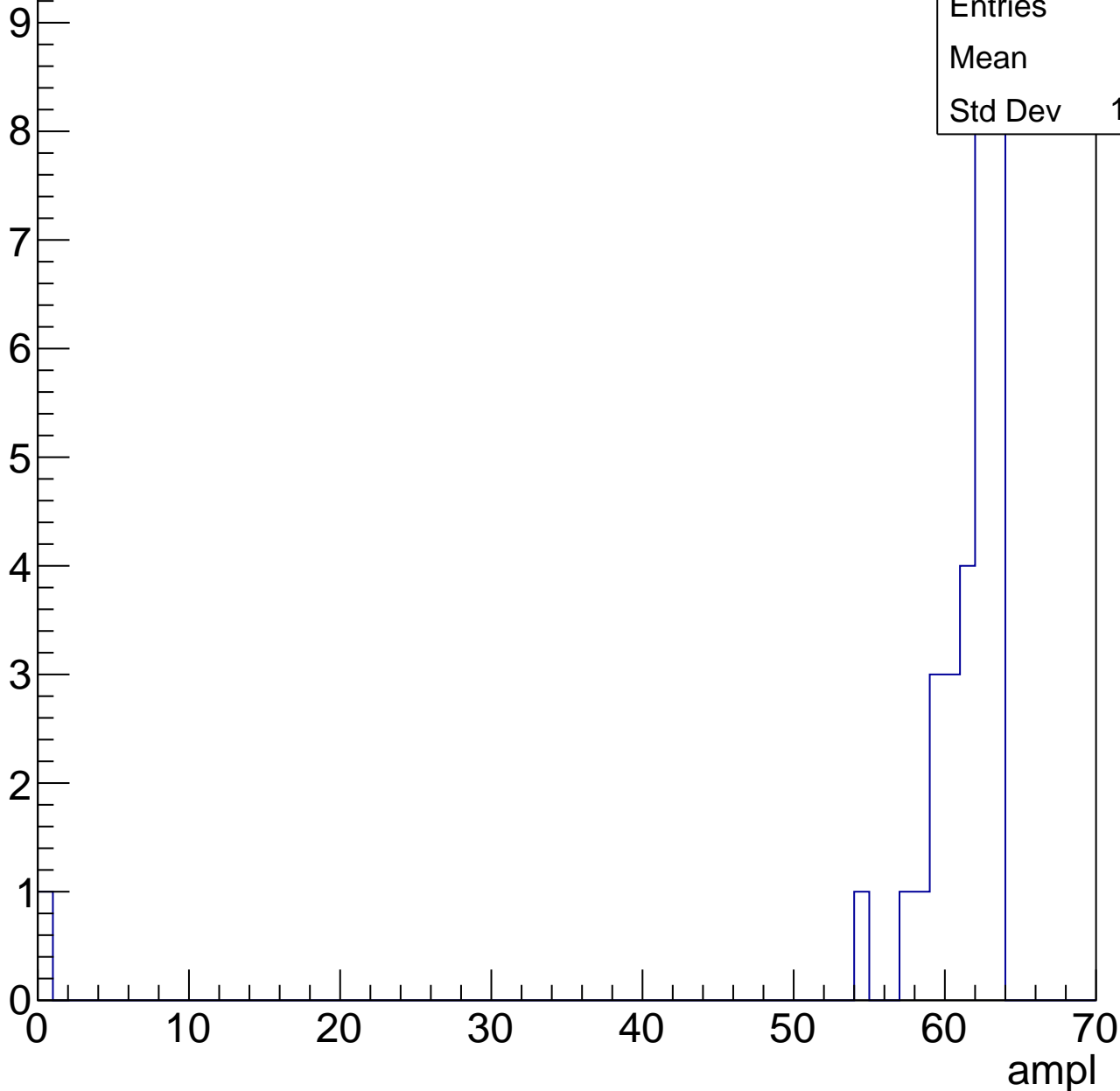


# B1L003S, U11-ch33, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	31
Mean	59.1
Std Dev	10.98



# B1L003S, U11-ch33, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch33, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U11-ch34, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	68
Mean	30.22
Std Dev	3.377

**Gaus mean : 31.0440**

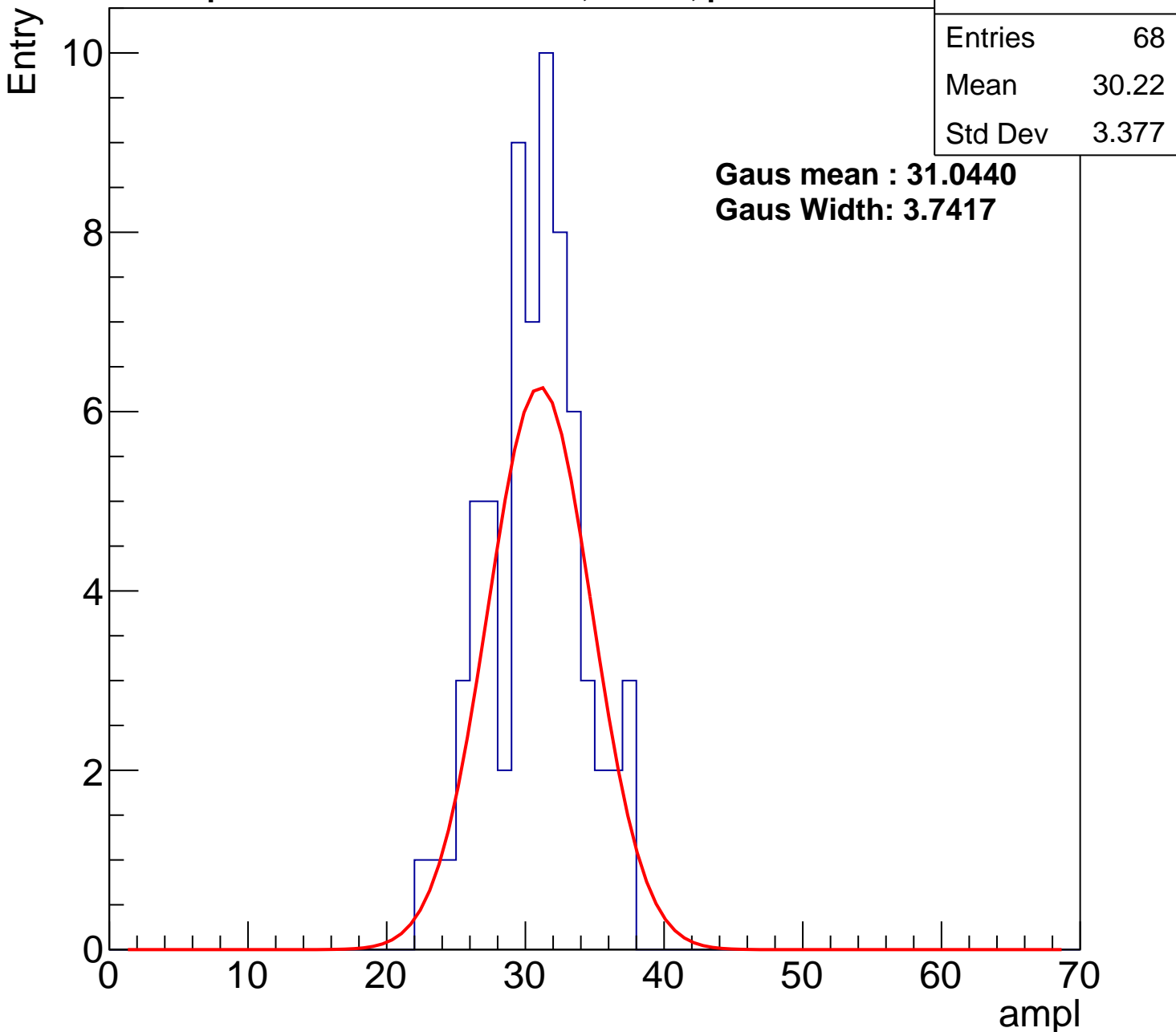
**Gaus Width: 3.7417**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L003S, U11-ch34, adc1

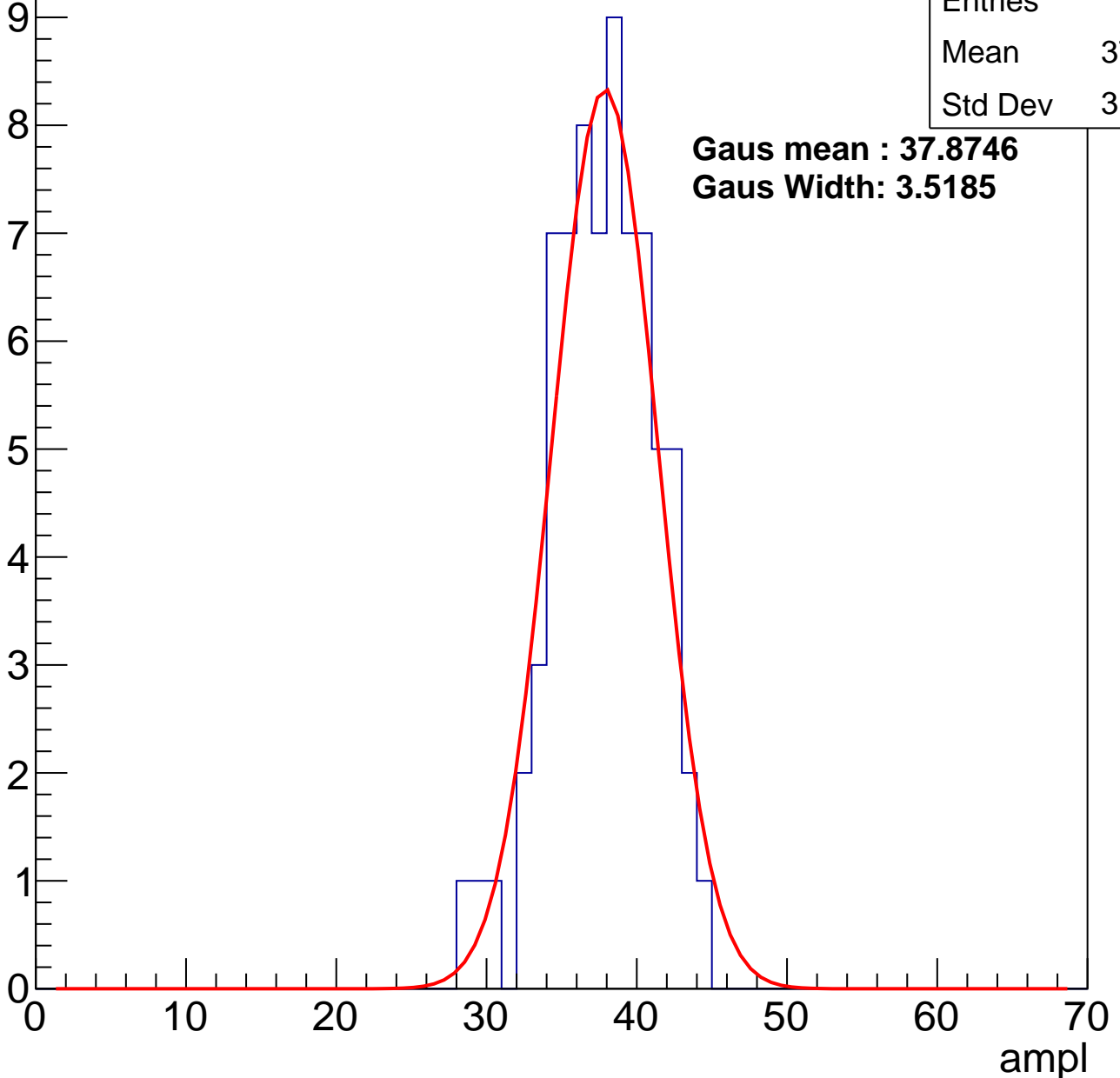
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	73
Mean	37.26
Std Dev	3.335

**Gaus mean : 37.8746**

**Gaus Width: 3.5185**



# B1L003S, U11-ch34, adc2

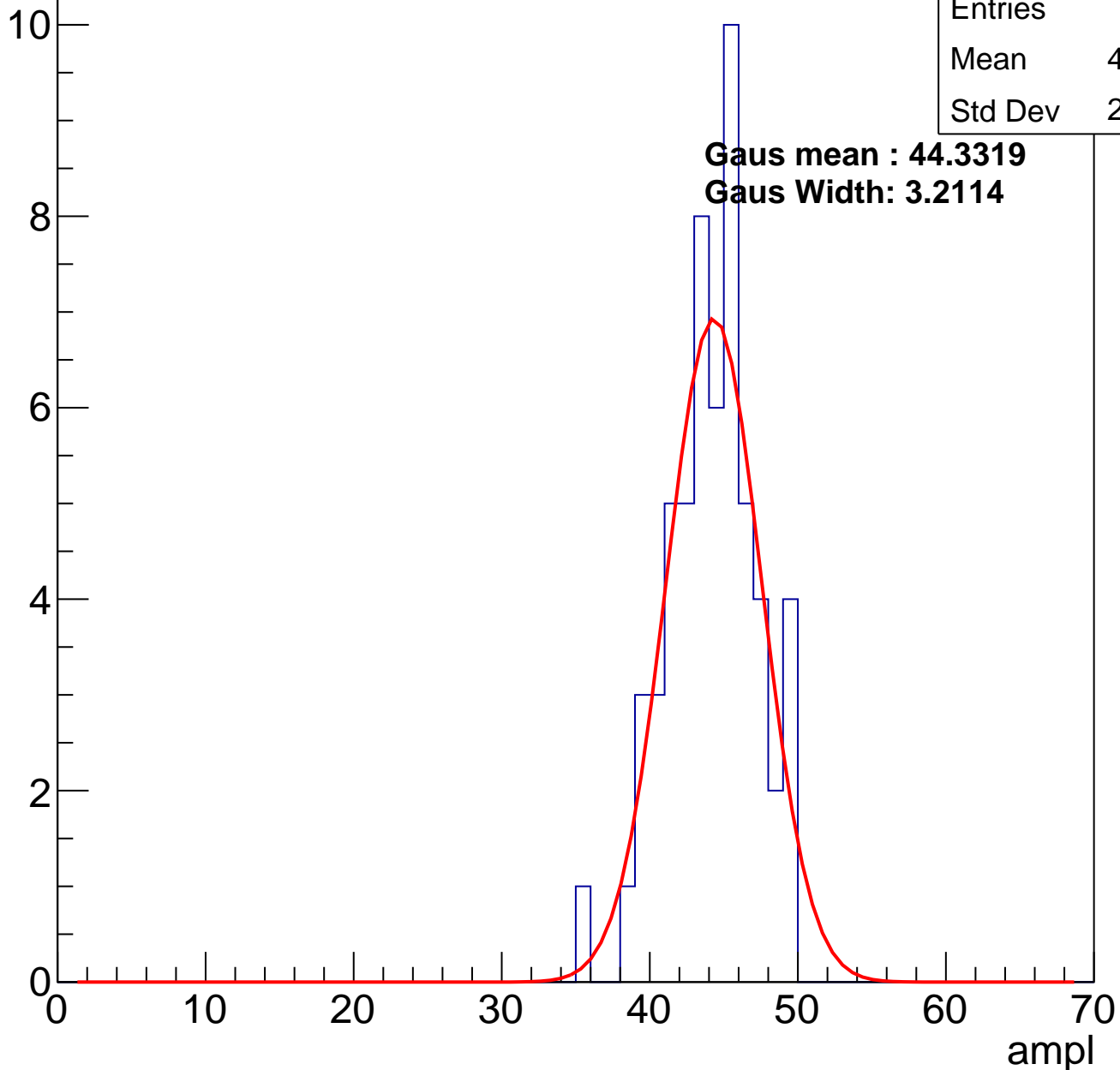
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	57
Mean	43.74
Std Dev	2.983

**Gaus mean : 44.3319**

**Gaus Width: 3.2114**

Entry

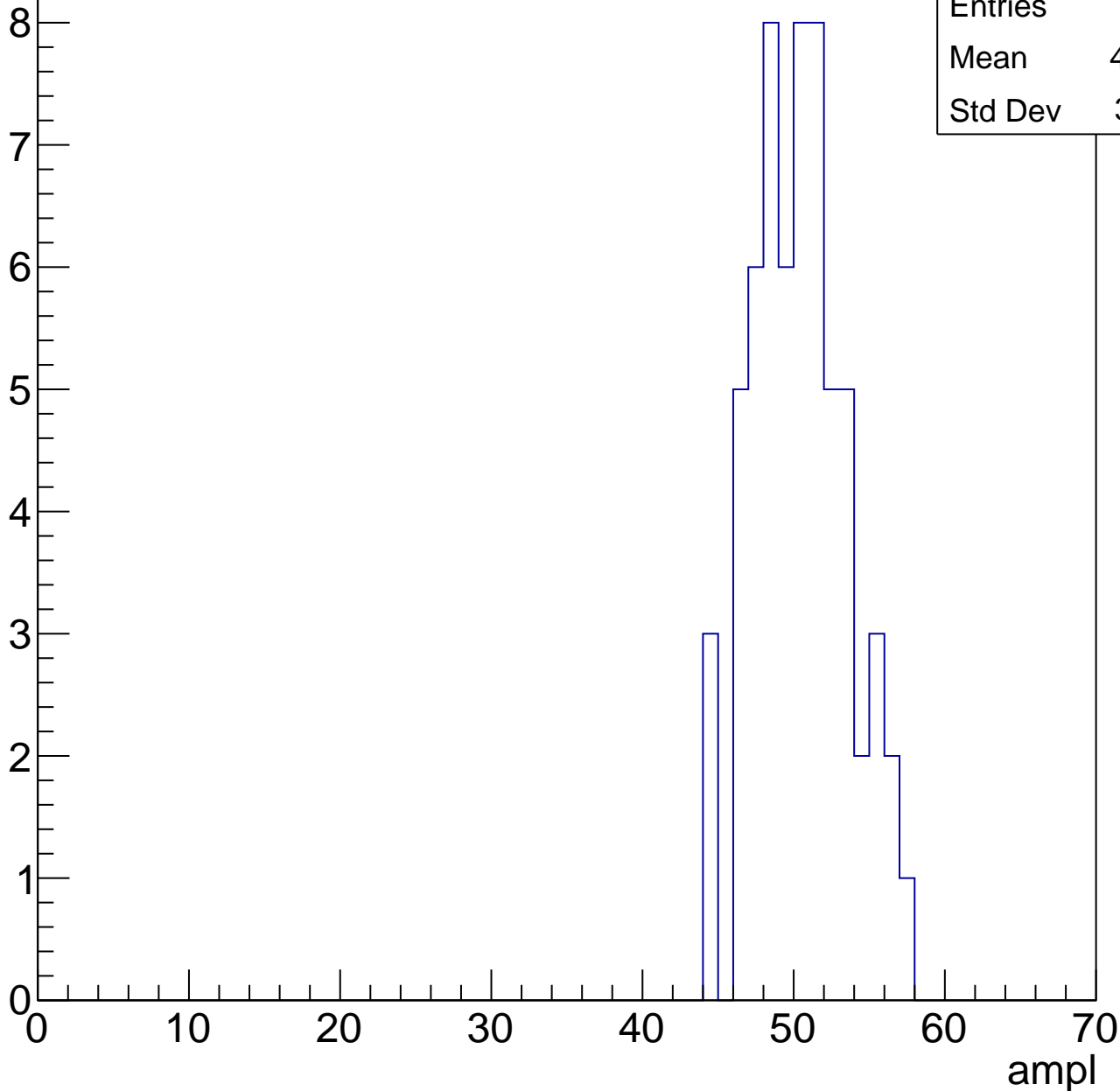


# B1L003S, U11-ch34, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

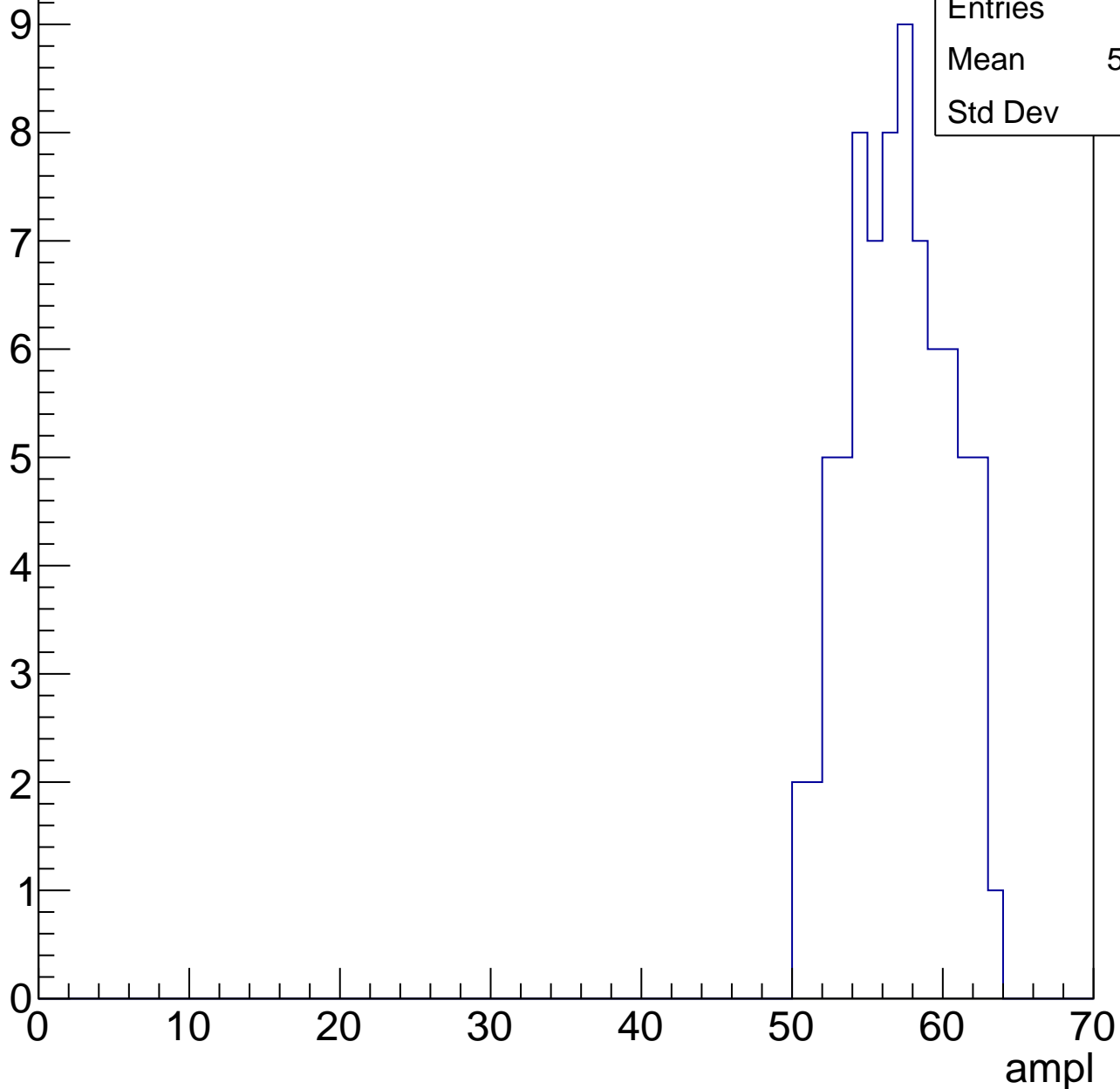
Entries	62
Mean	49.95
Std Dev	3.061



# B1L003S, U11-ch34, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



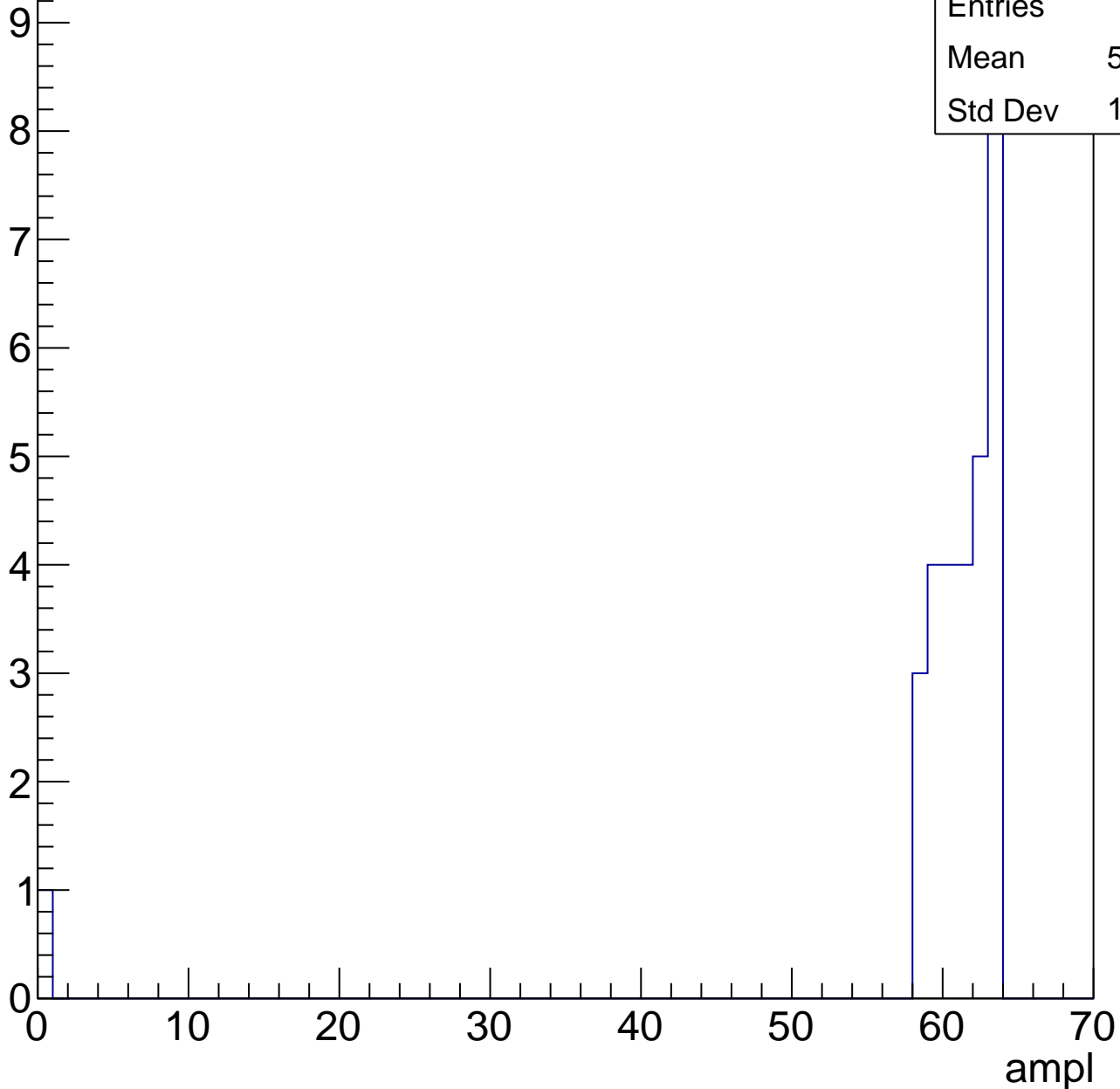
Entries	76
Mean	56.62
Std Dev	3.24

# B1L003S, U11-ch34, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	30
Mean	59.03
Std Dev	11.09



# B1L003S, U11-ch34, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch34, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U11-ch35, adc0

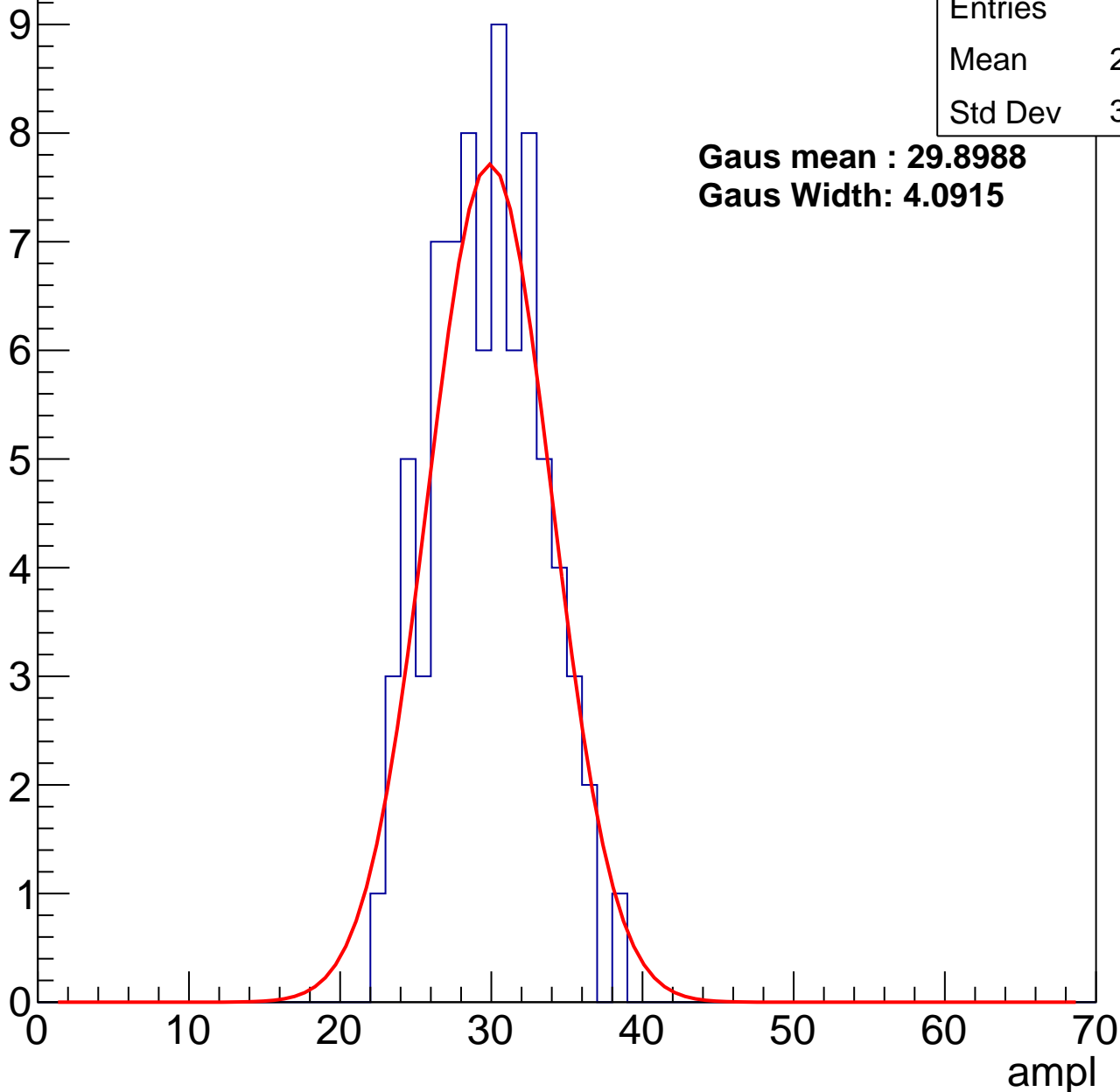
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	78
Mean	29.27
Std Dev	3.572

**Gaus mean : 29.8988**

**Gaus Width: 4.0915**



# B1L003S, U11-ch35, adc1

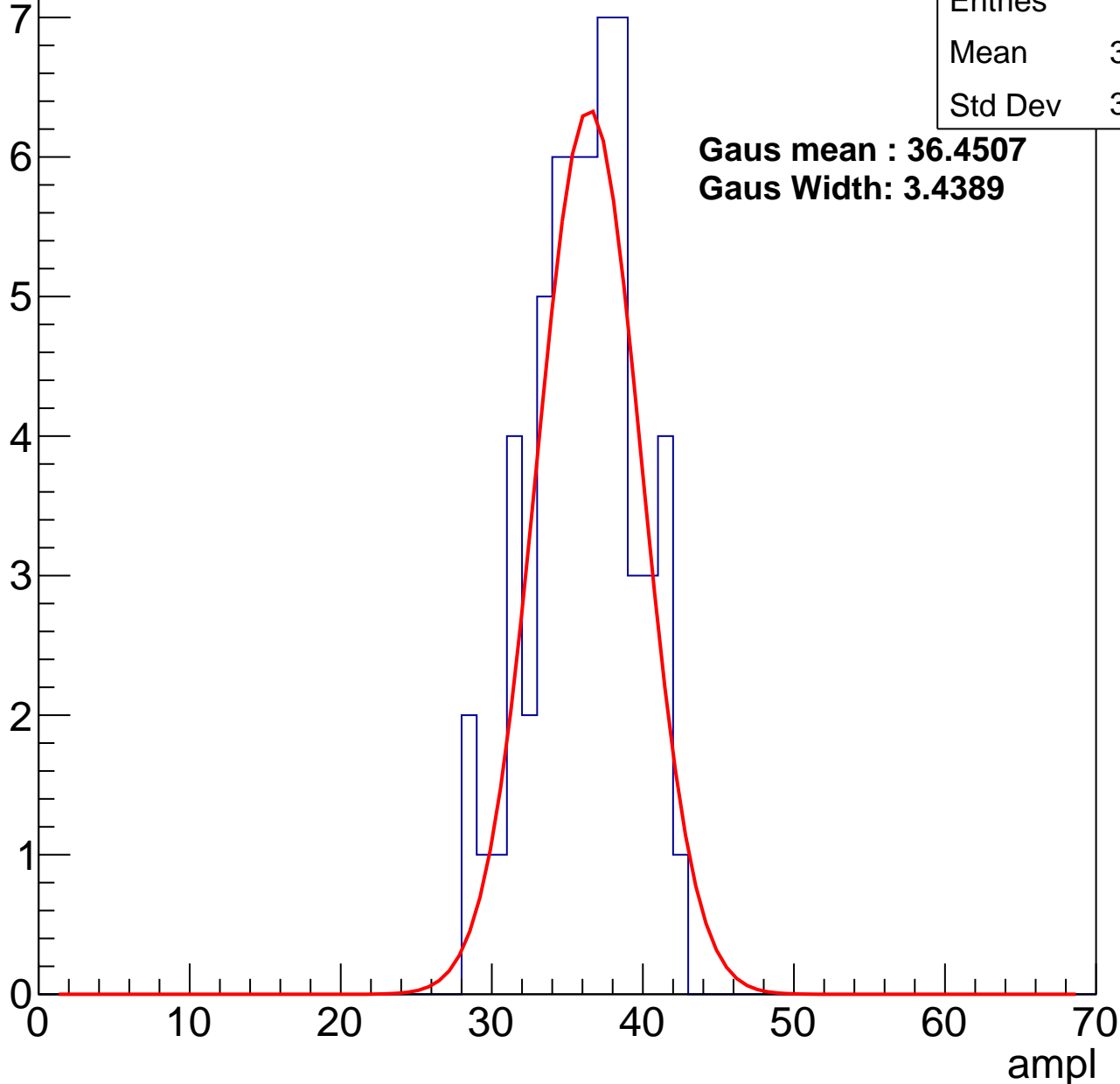
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	35.62
Std Dev	3.367

**Gaus mean : 36.4507**

**Gaus Width: 3.4389**



# B1L003S, U11-ch35, adc2

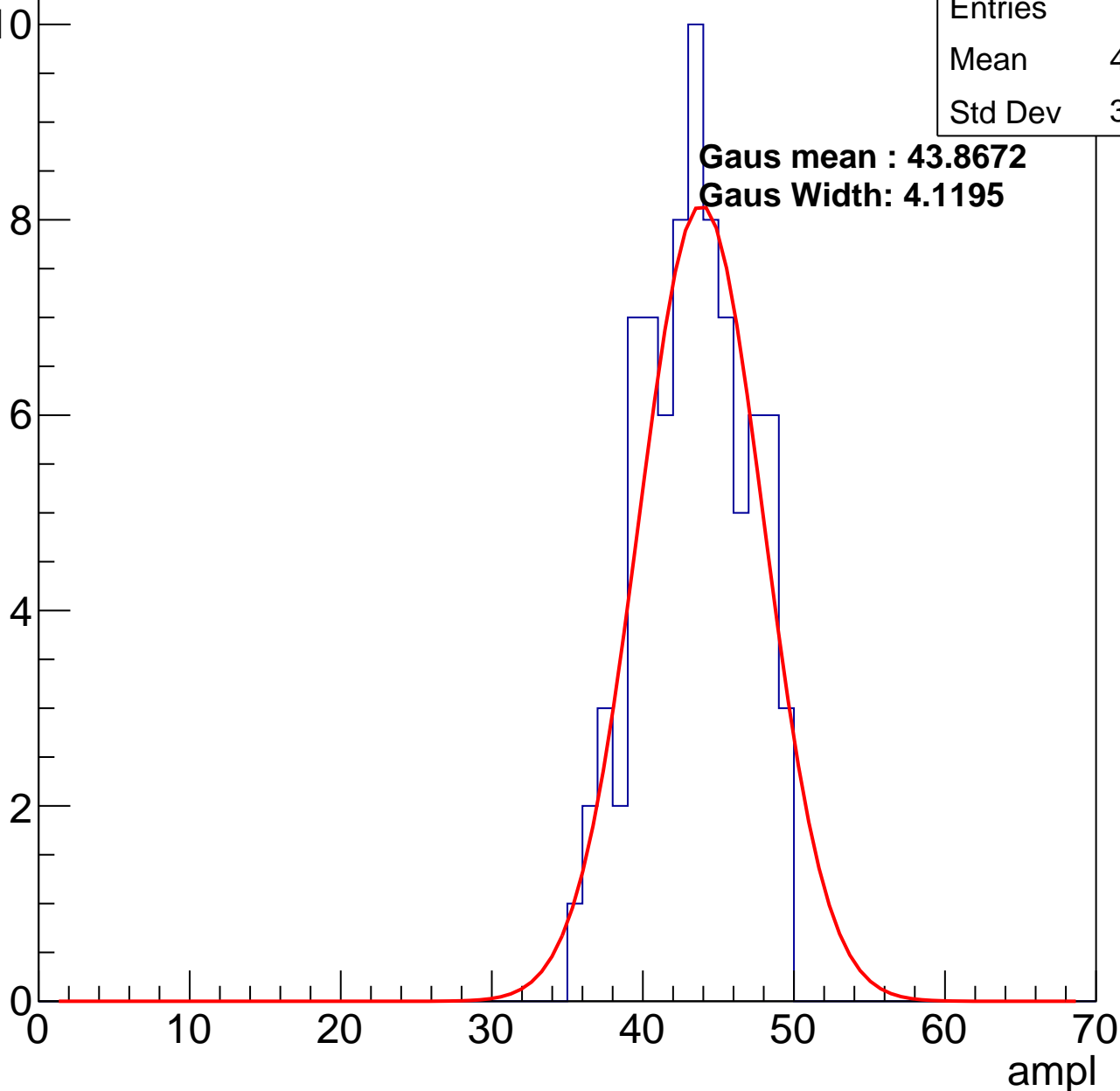
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	81
Mean	42.88
Std Dev	3.444

**Gaus mean : 43.8672**

**Gaus Width: 4.1195**

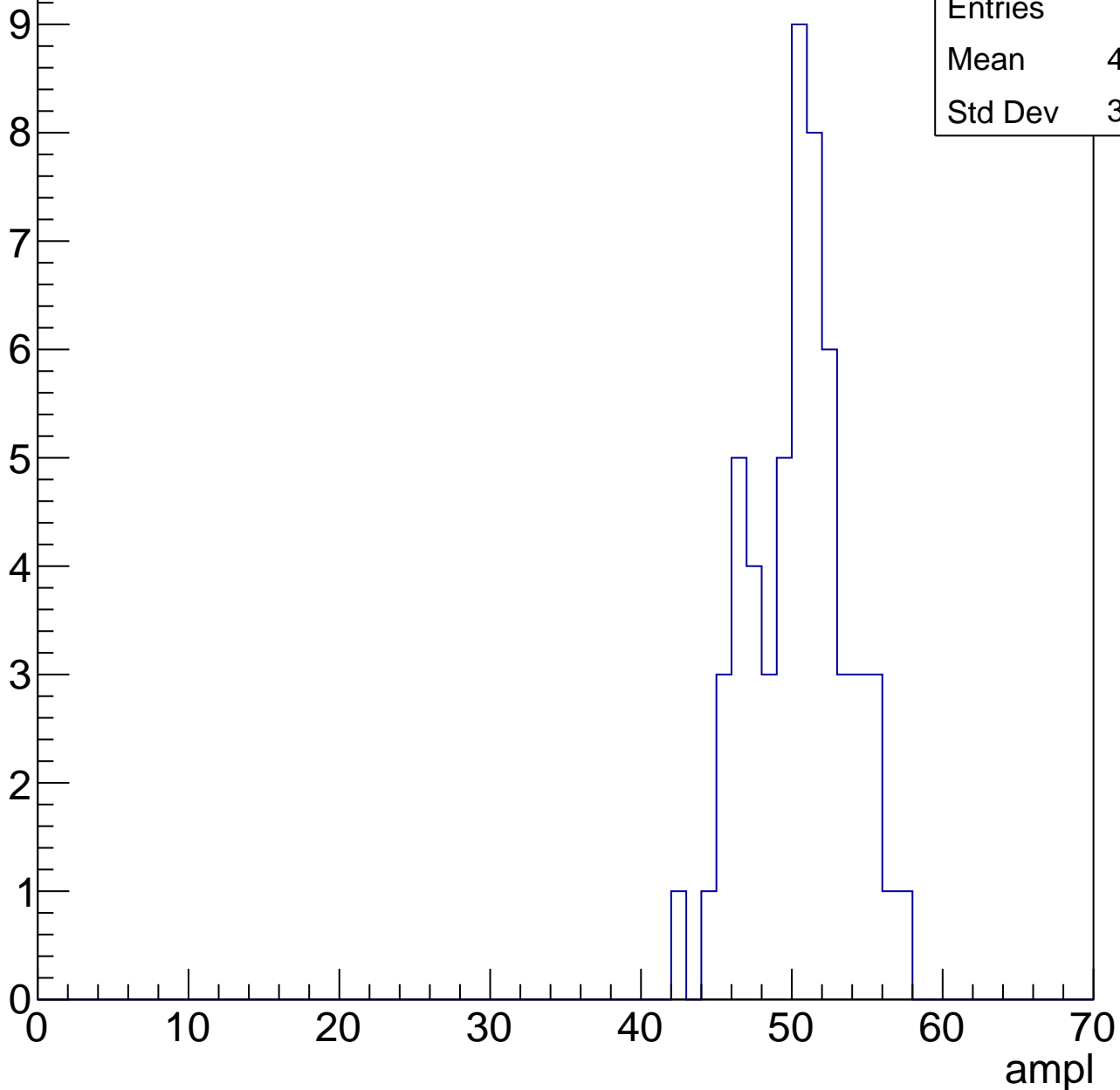


# B1L003S, U11-ch35, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	49.95
Std Dev	3.204

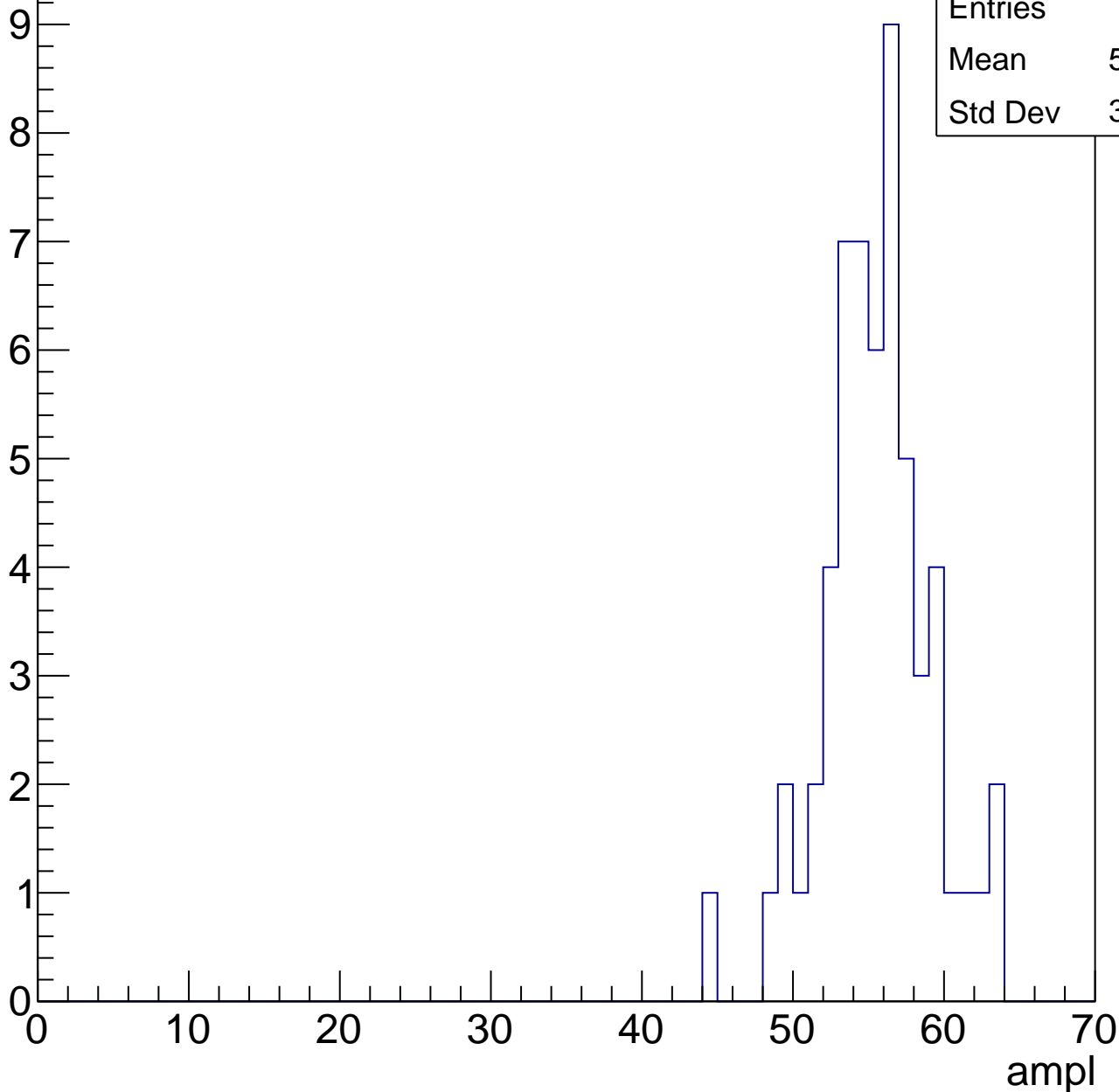


# B1L003S, U11-ch35, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	55.04
Std Dev	3.574

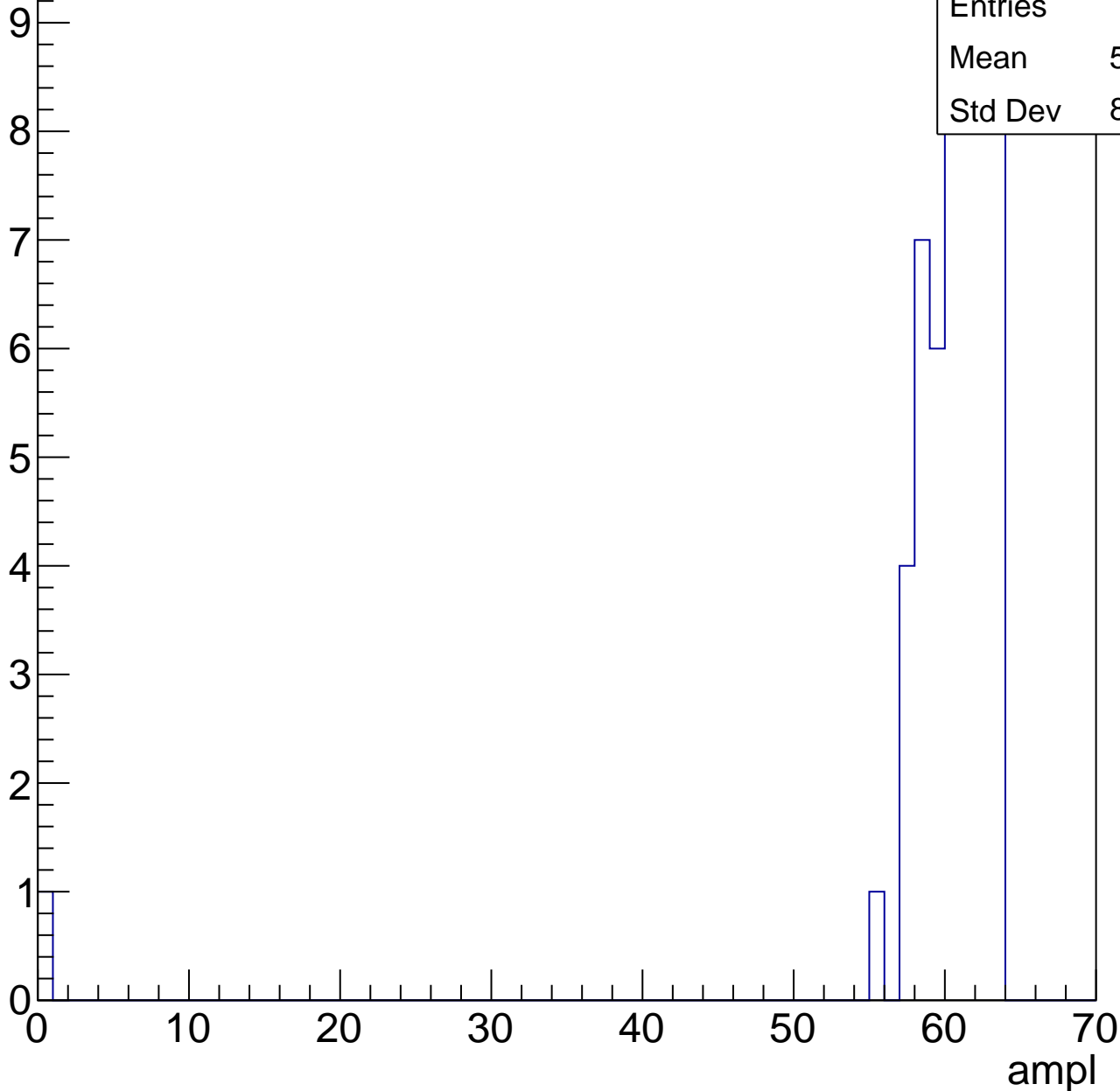


# B1L003S, U11-ch35, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	52
Mean	59.08
Std Dev	8.508



# B1L003S, U11-ch35, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch35, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U11-ch36, adc0

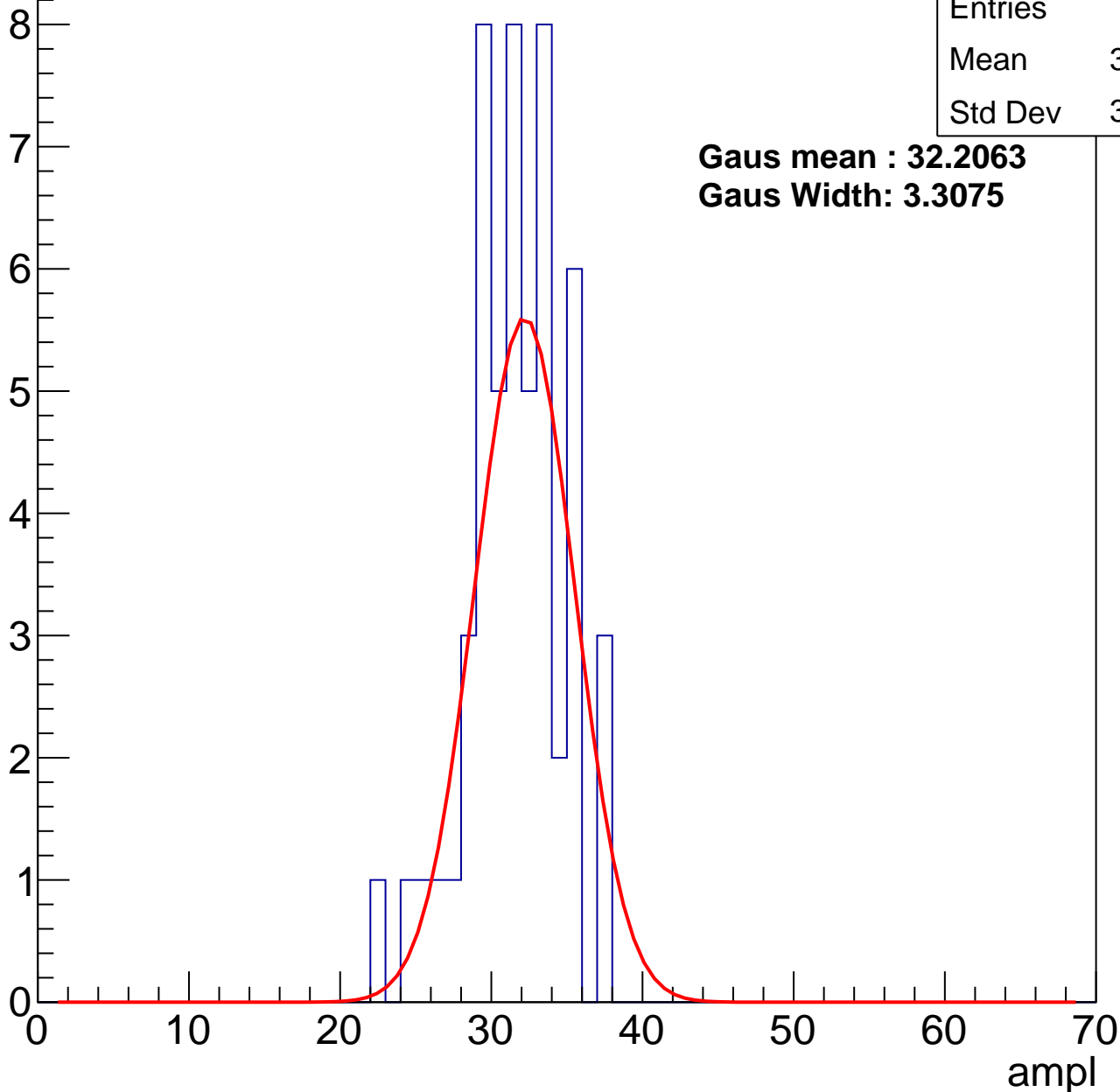
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	31.15
Std Dev	3.159

**Gaus mean : 32.2063**

**Gaus Width: 3.3075**

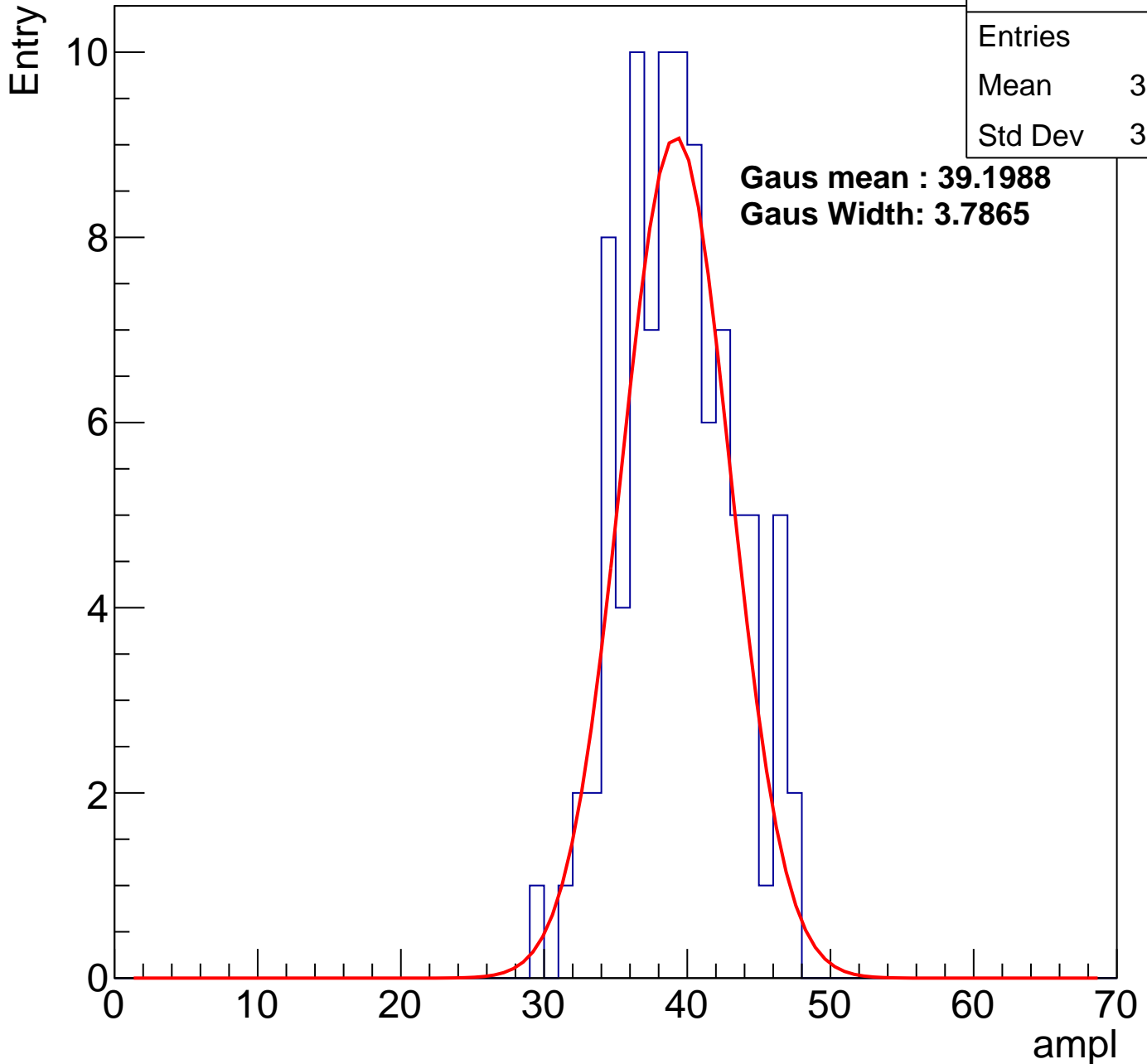


# B1L003S, U11-ch36, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	95
Mean	38.89
Std Dev	3.886

**Gaus mean : 39.1988**  
**Gaus Width: 3.7865**



# B1L003S, U11-ch36, adc2

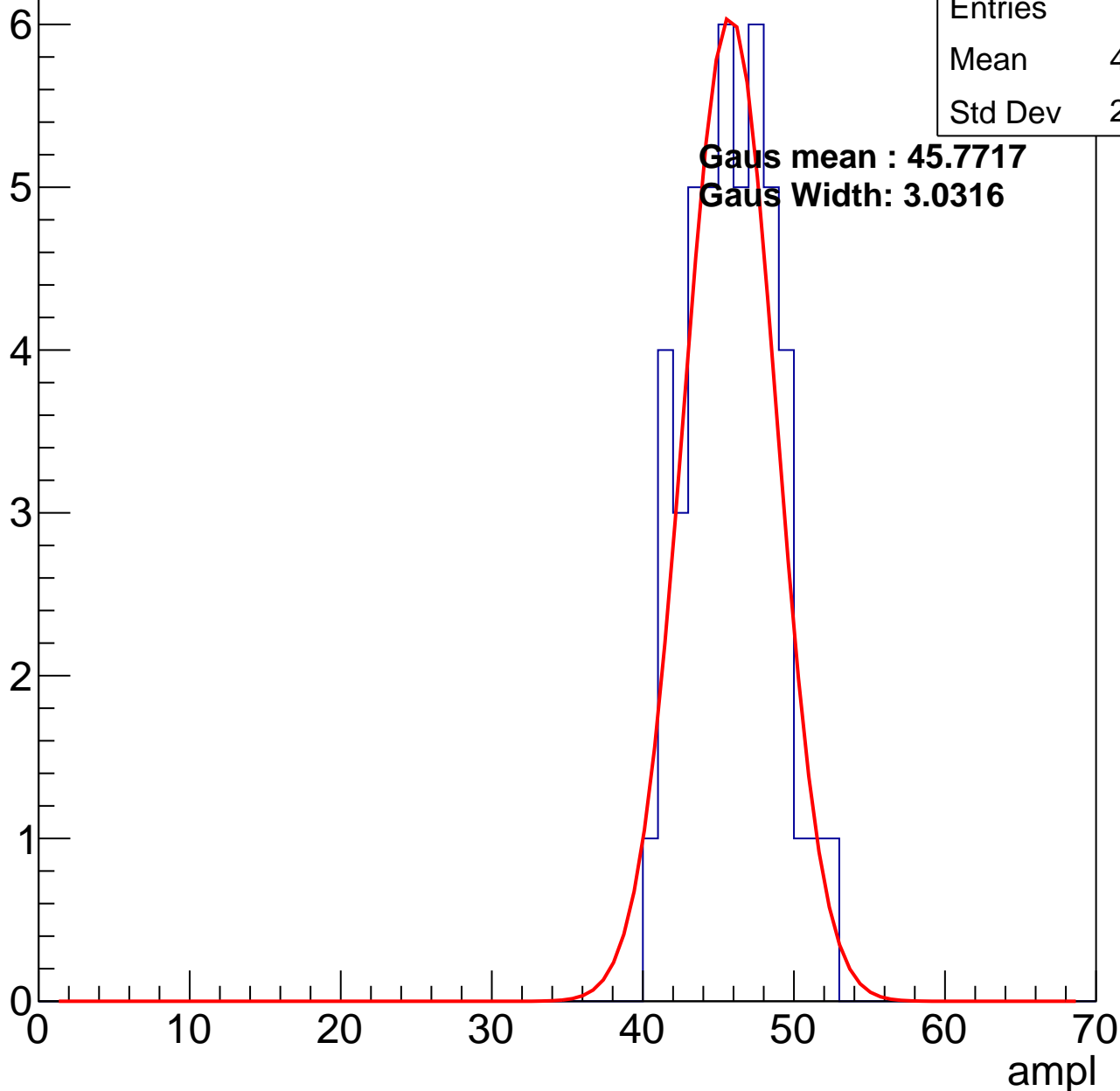
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	47
Mean	45.45
Std Dev	2.842

**Gaus mean : 45.7717**

**Gaus Width: 3.0316**

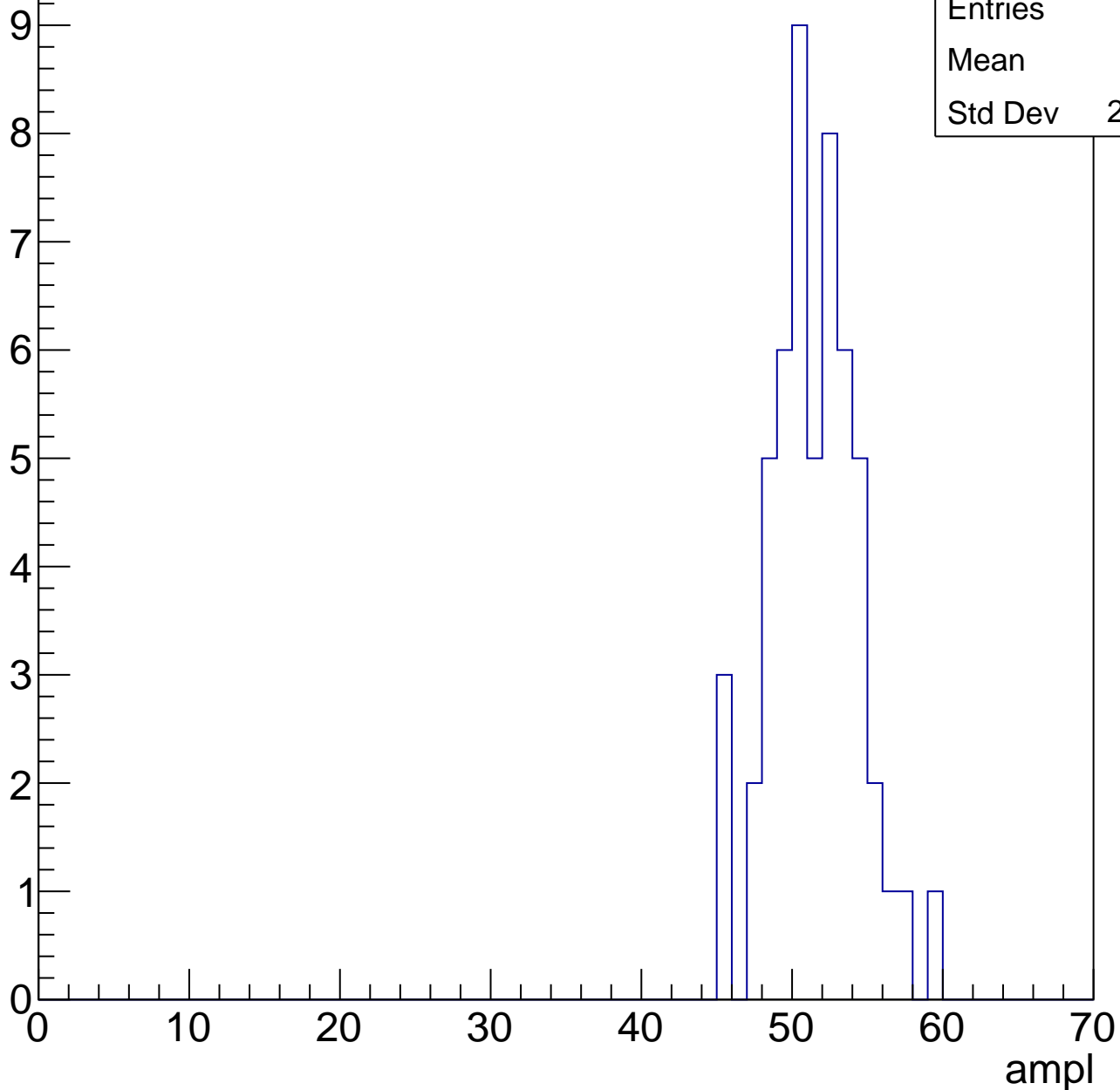


# B1L003S, U11-ch36, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	54
Mean	51
Std Dev	2.893

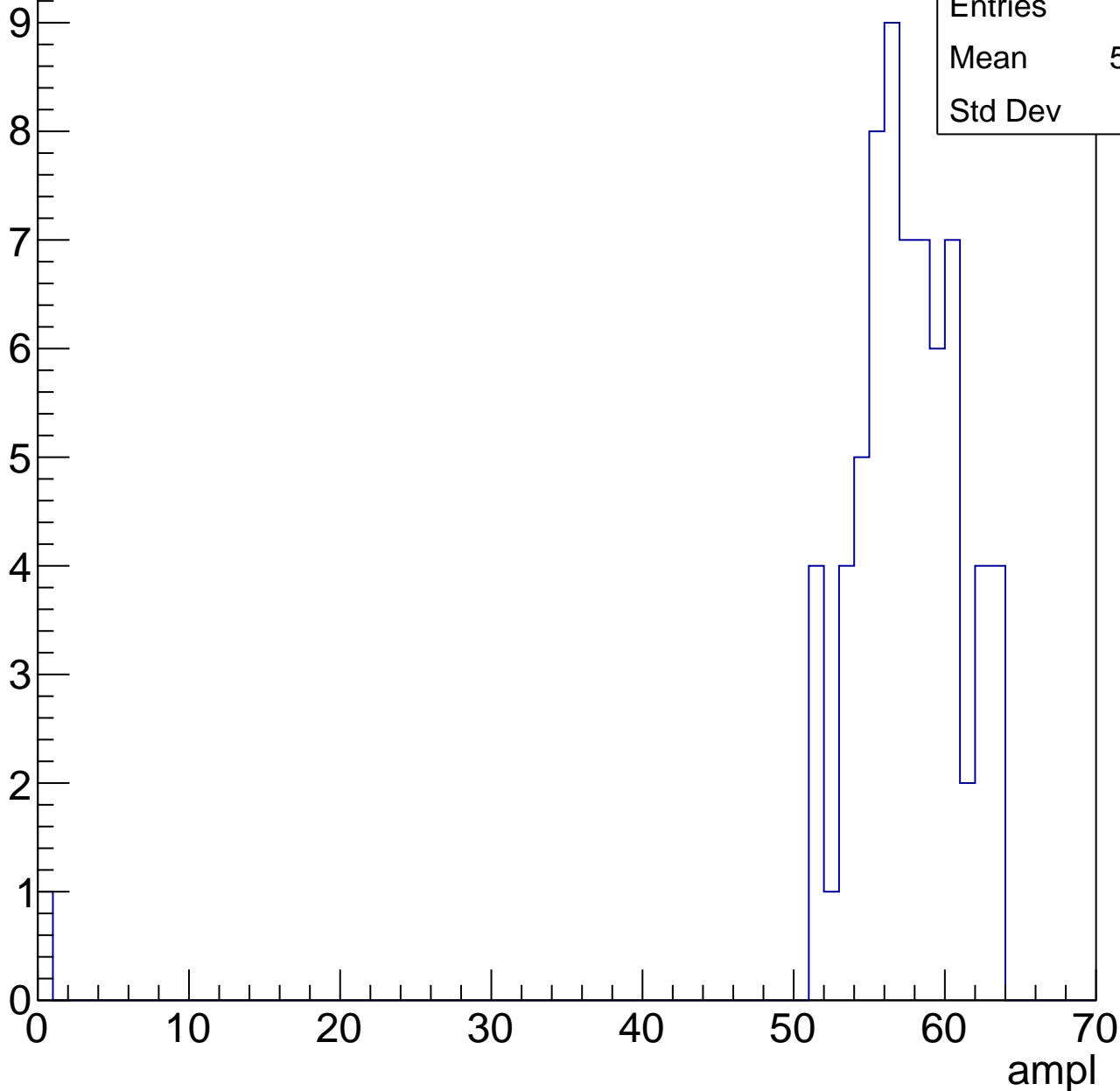


# B1L003S, U11-ch36, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	56.28
Std Dev	7.52



# B1L003S, U11-ch36, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

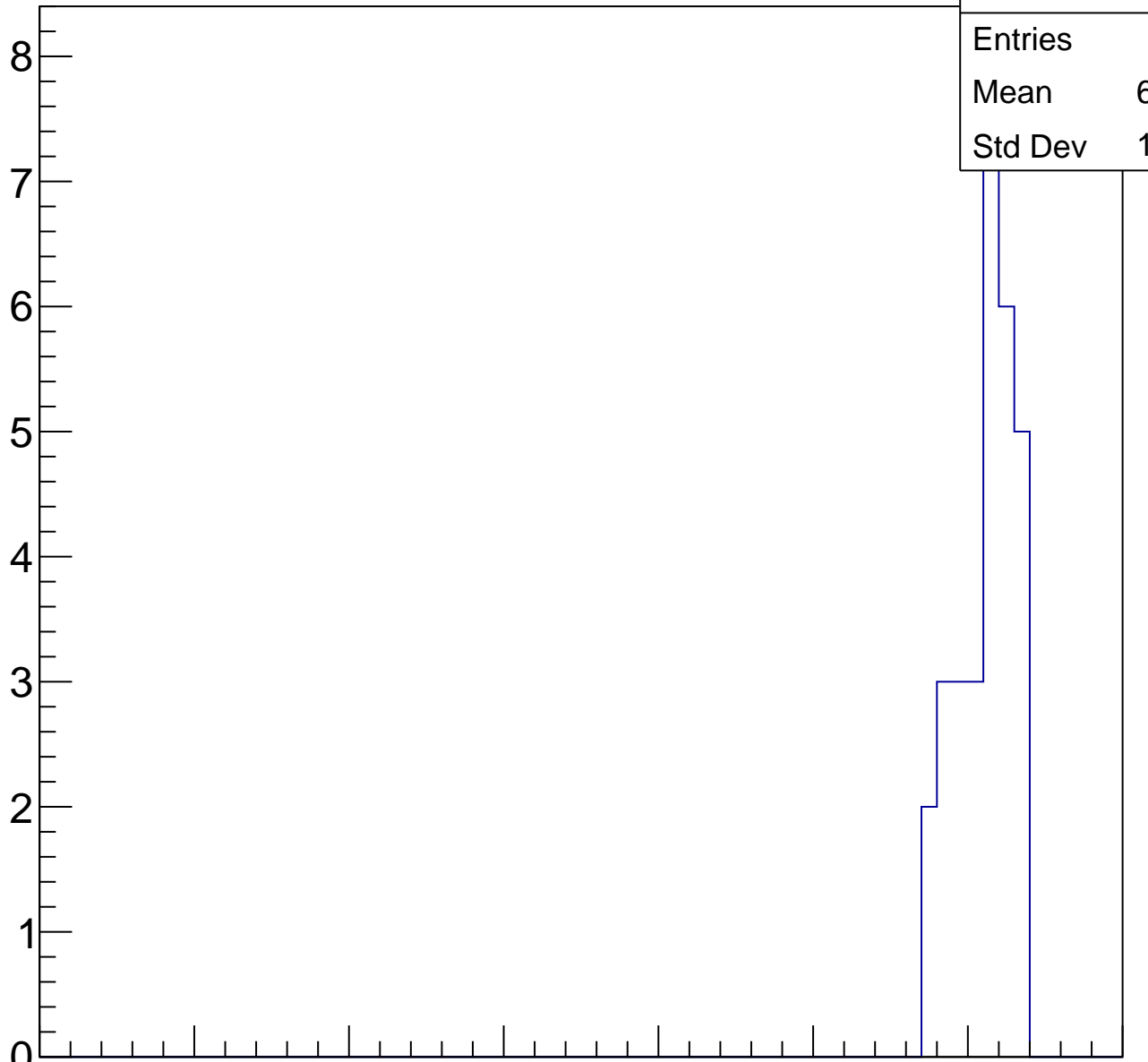
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	30
Mean	60.67
Std Dev	1.795

ampl

0 10 20 30 40 50 60 70



# B1L003S, U11-ch36, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch36, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U11-ch37, adc0

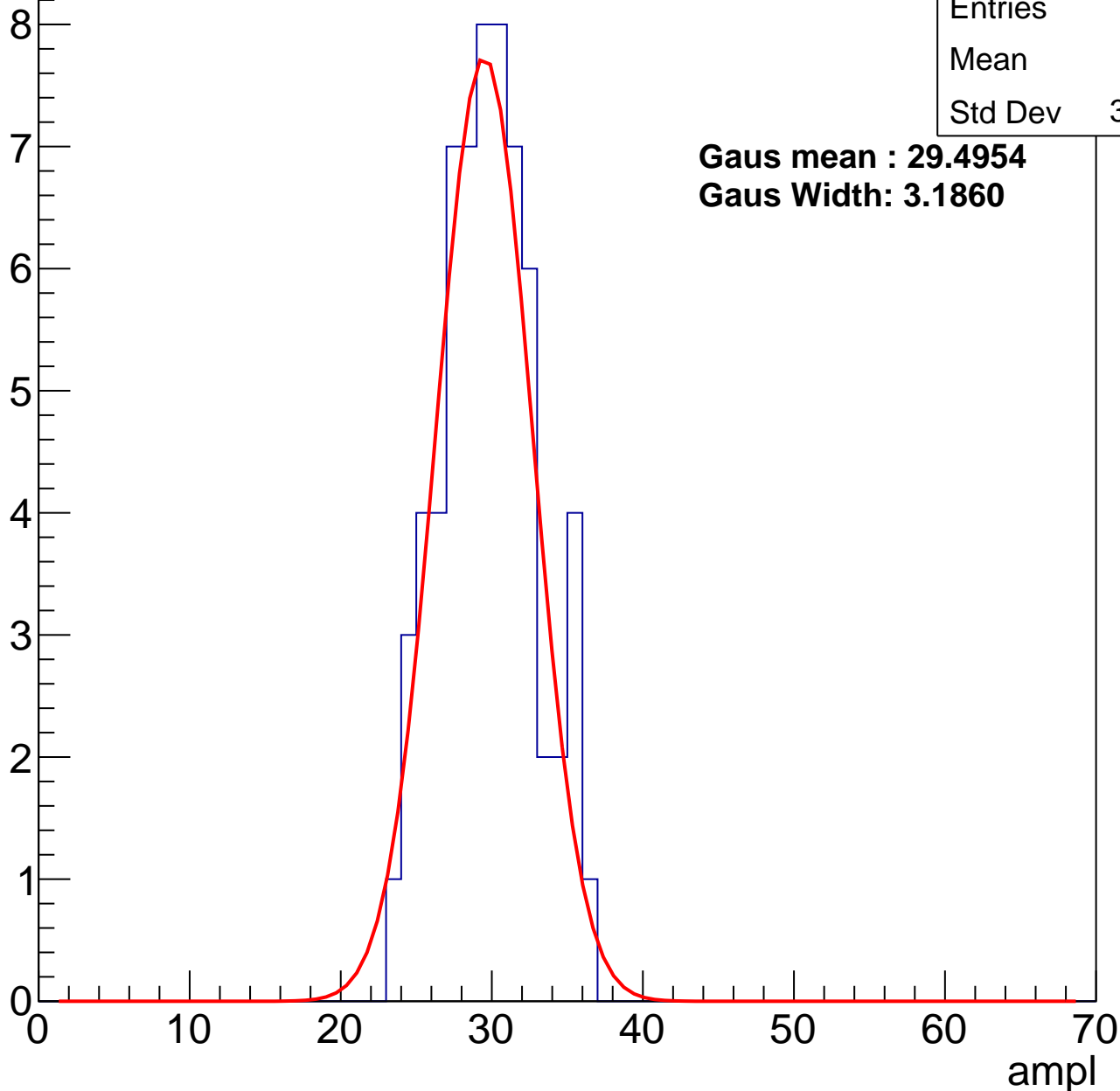
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	29.3
Std Dev	3.076

**Gaus mean : 29.4954**

**Gaus Width: 3.1860**



# B1L003S, U11-ch37, adc1

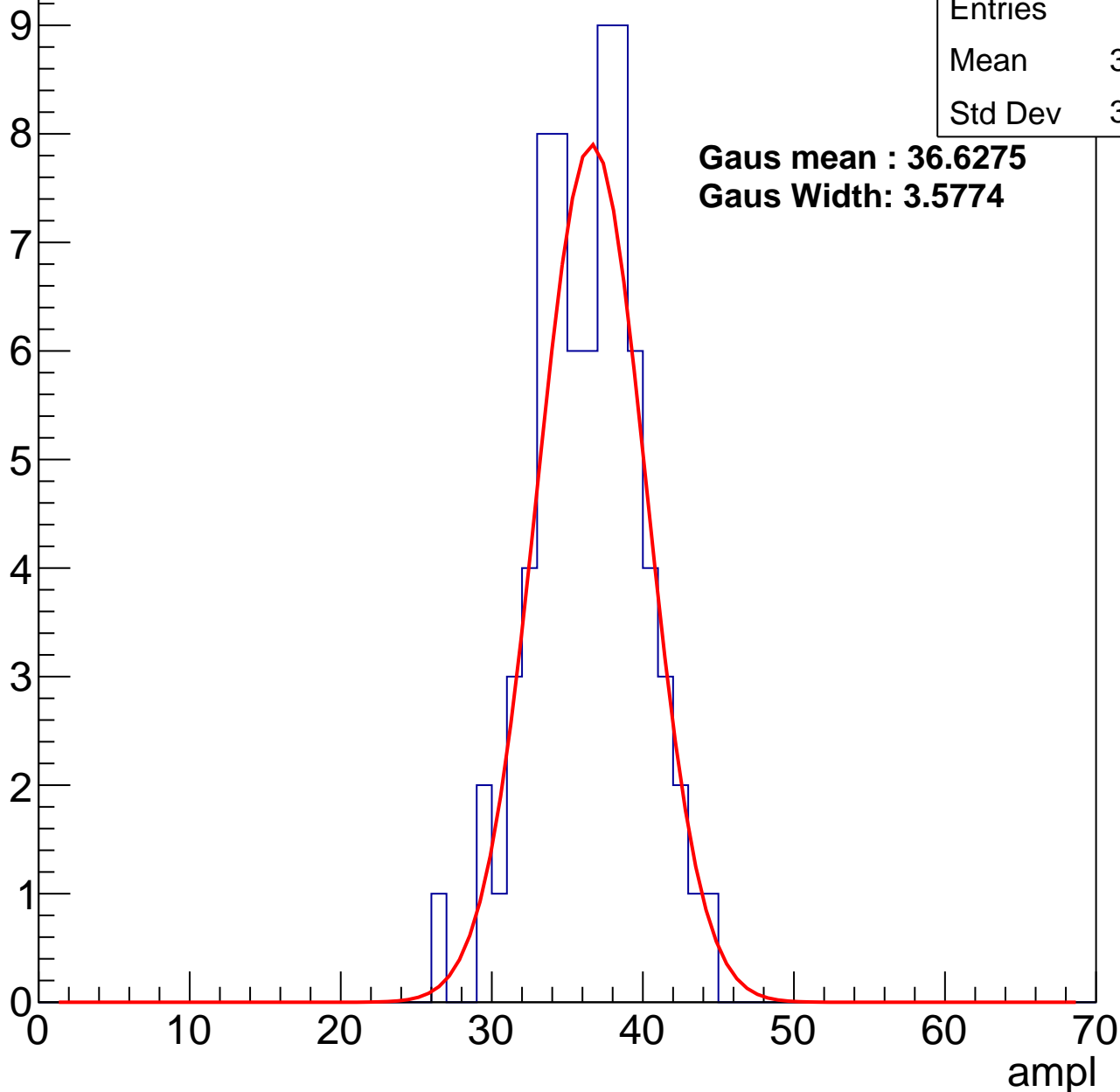
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	74
Mean	35.95
Std Dev	3.499

**Gaus mean : 36.6275**

**Gaus Width: 3.5774**



# B1L003S, U11-ch37, adc2

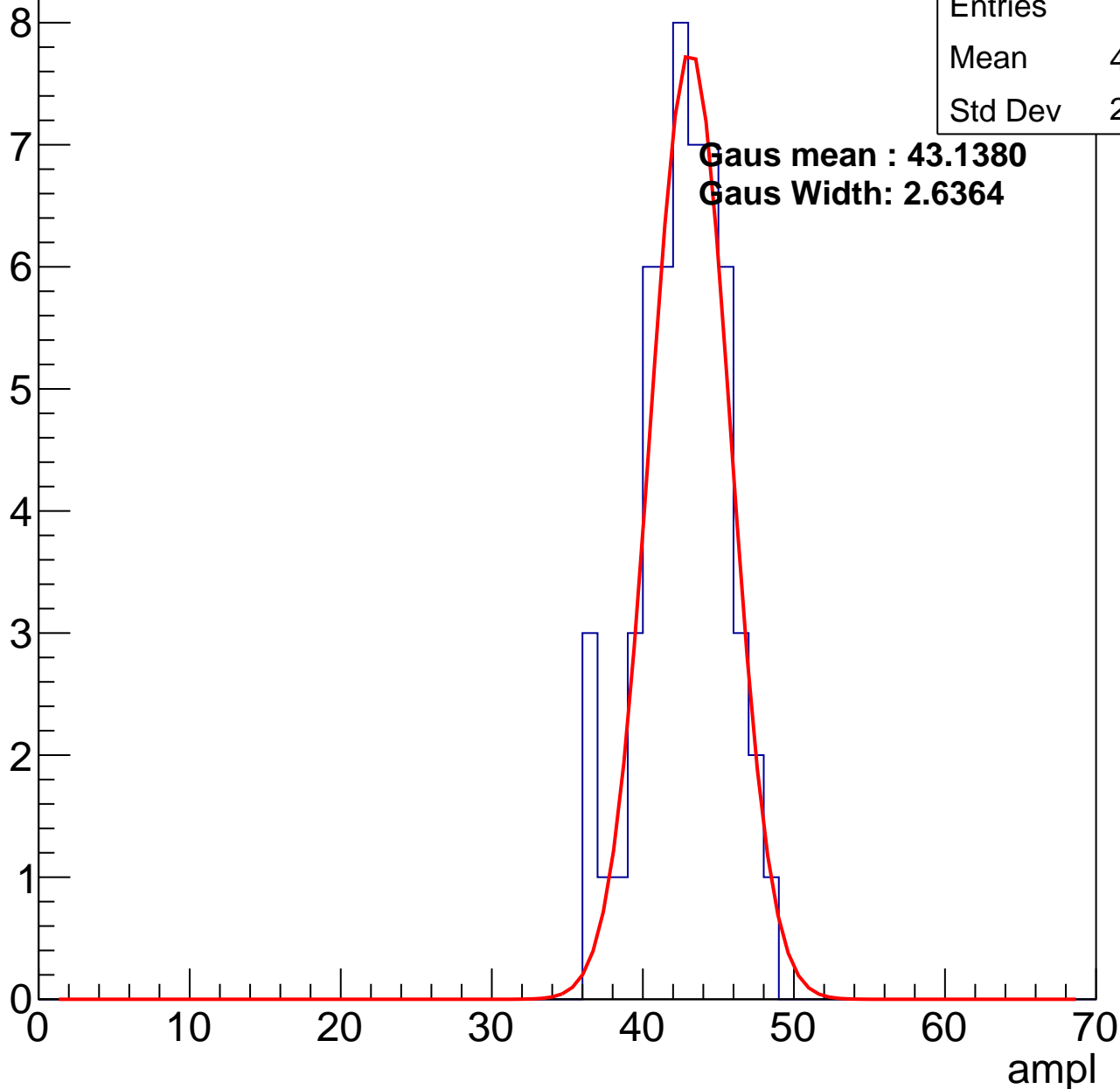
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	54
Mean	42.24
Std Dev	2.808

**Gaus mean : 43.1380**

**Gaus Width: 2.6364**



# B1L003S, U11-ch37, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

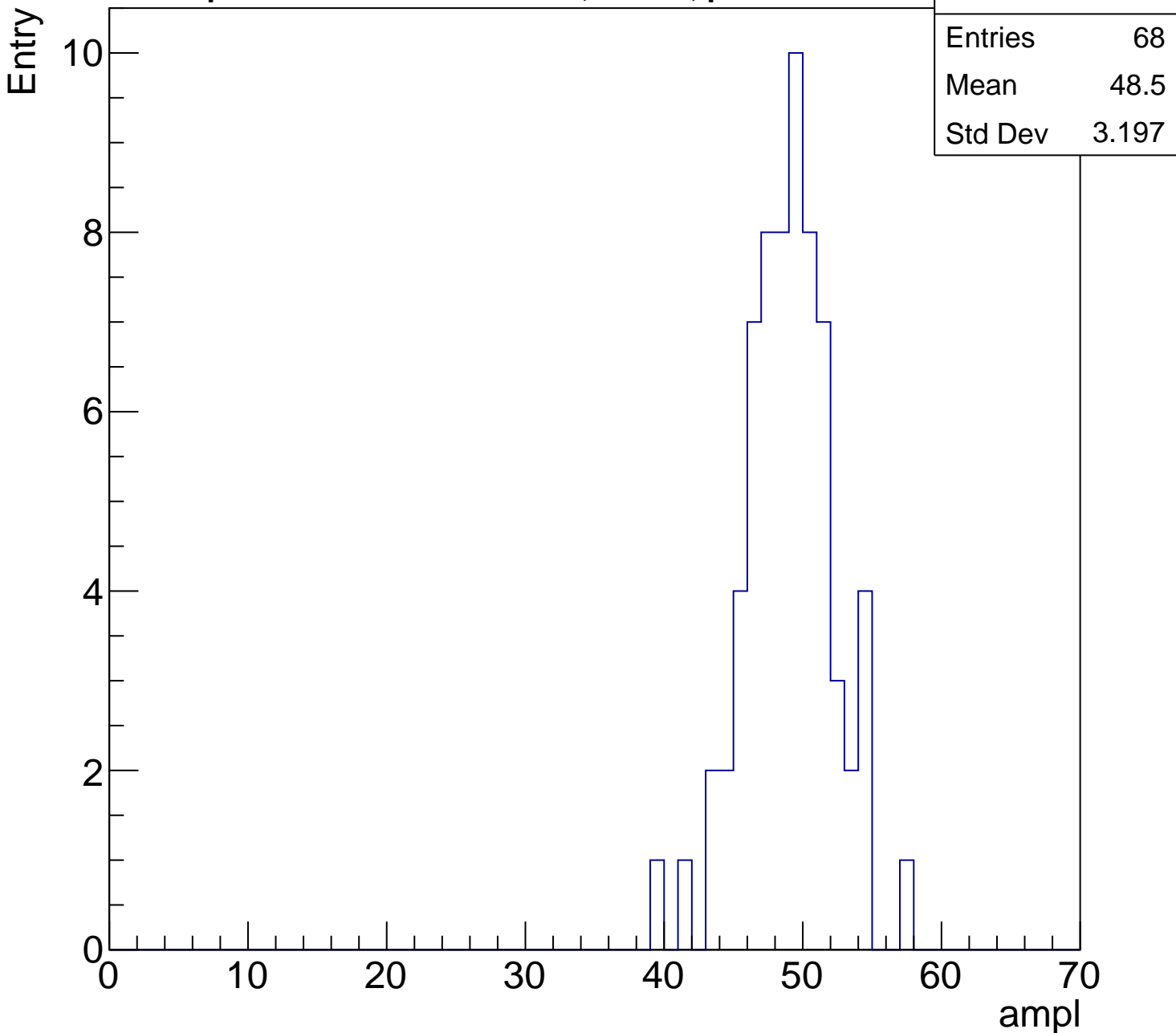
Entries	68
Mean	48.5
Std Dev	3.197

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L003S, U11-ch37, adc4

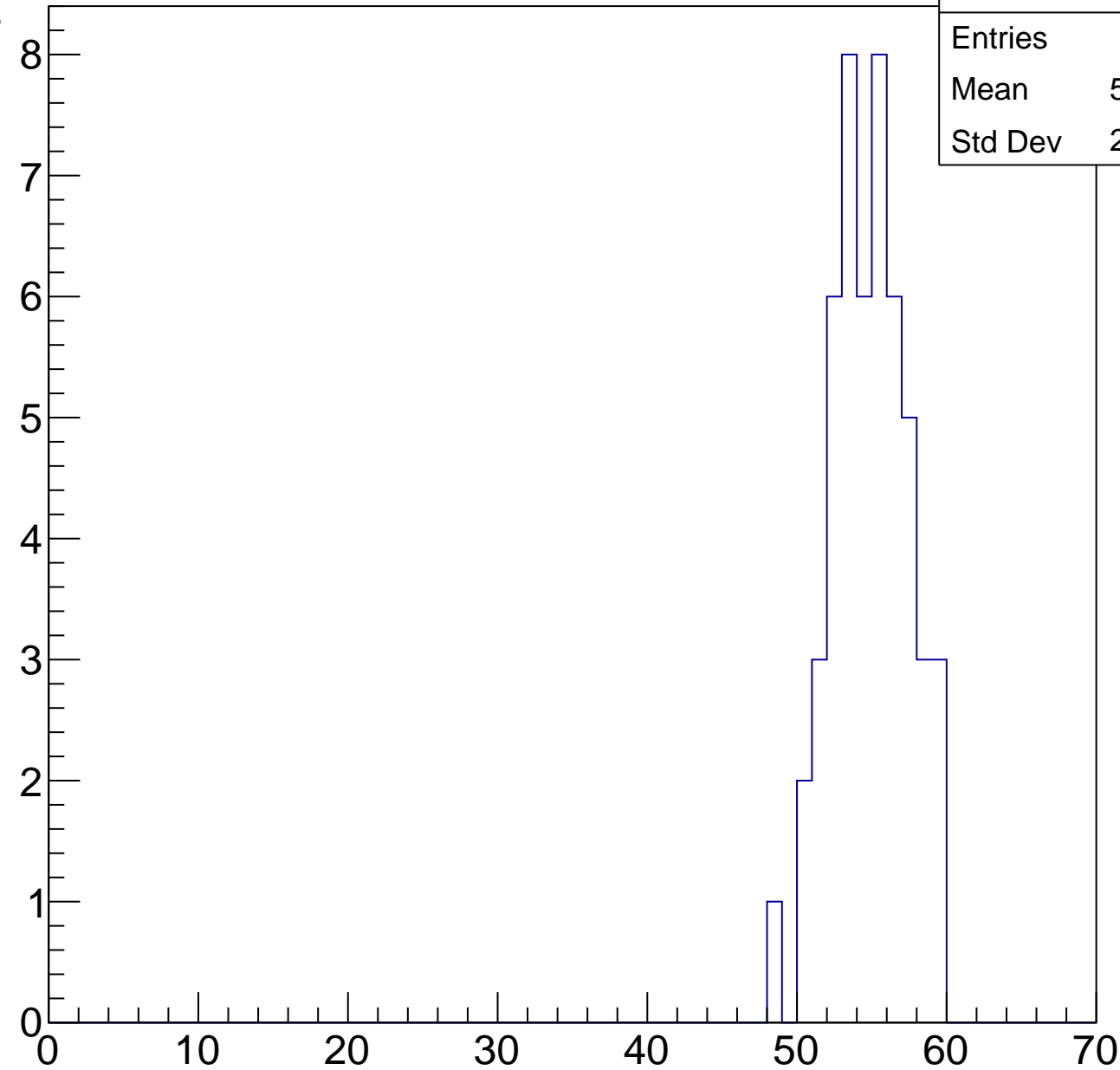
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	51
Mean	54.37
Std Dev	2.505

ampl

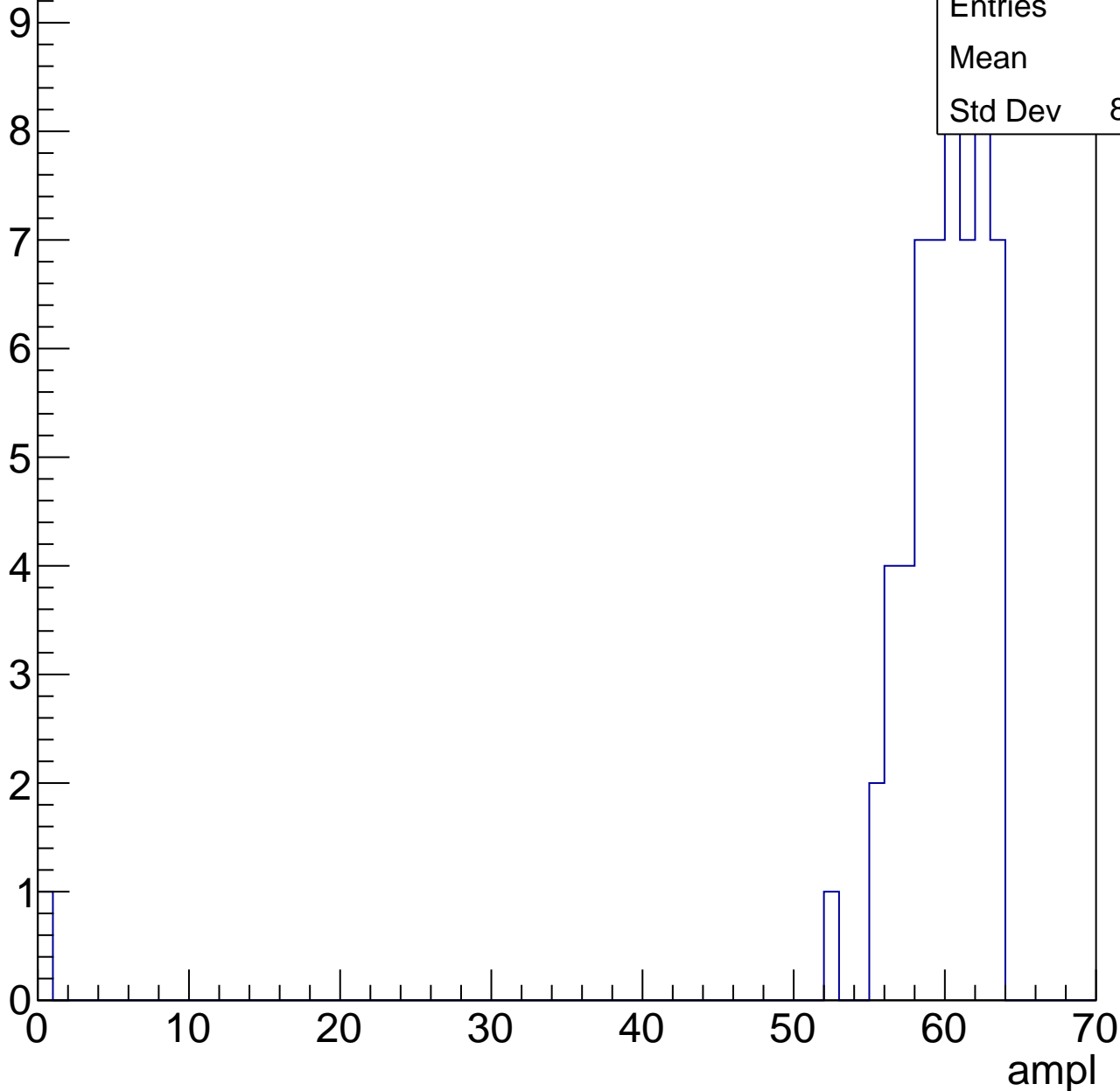


# B1L003S, U11-ch37, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

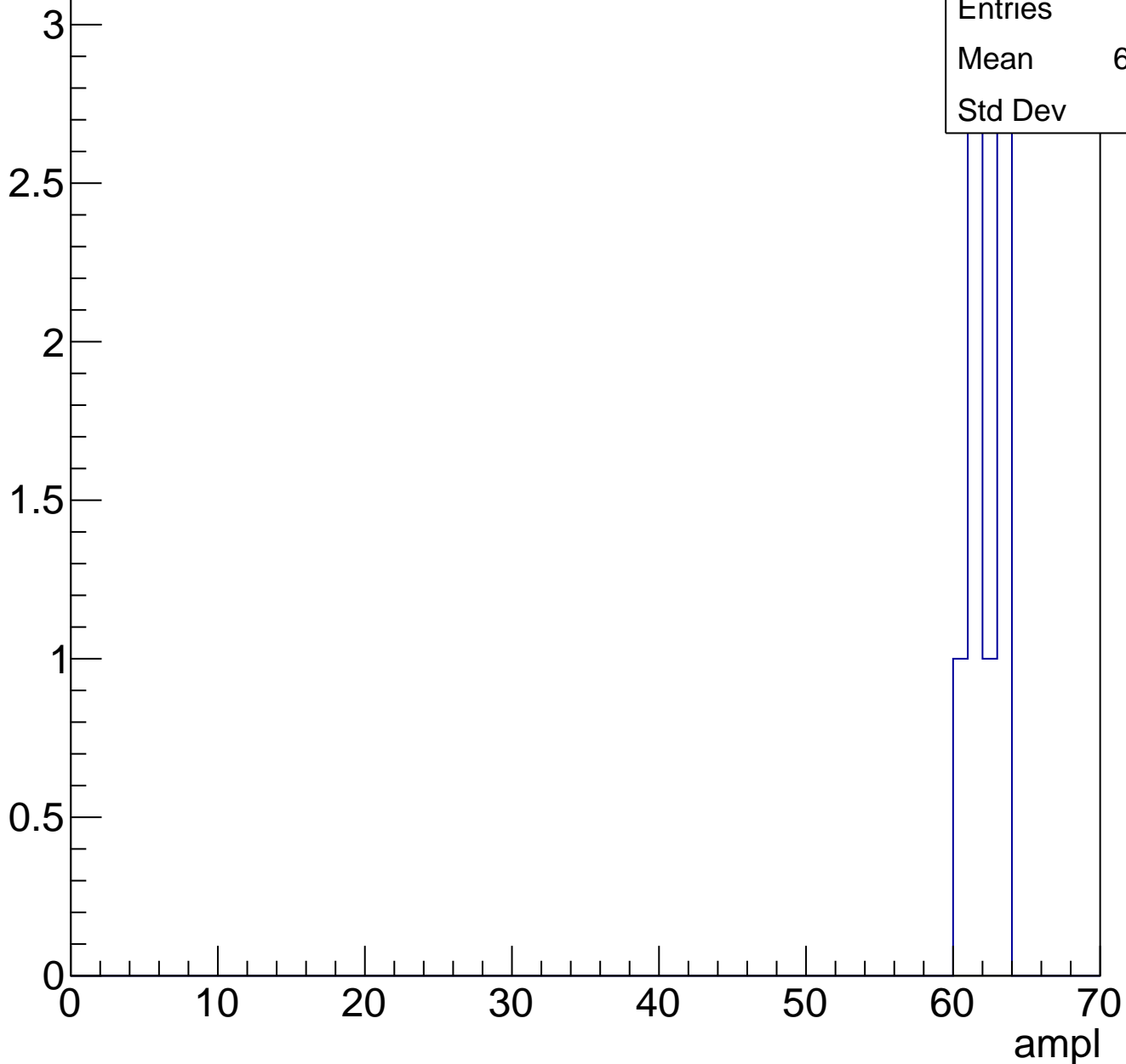
Entries	58
Mean	58.6
Std Dev	8.139



# B1L003S, U11-ch37, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

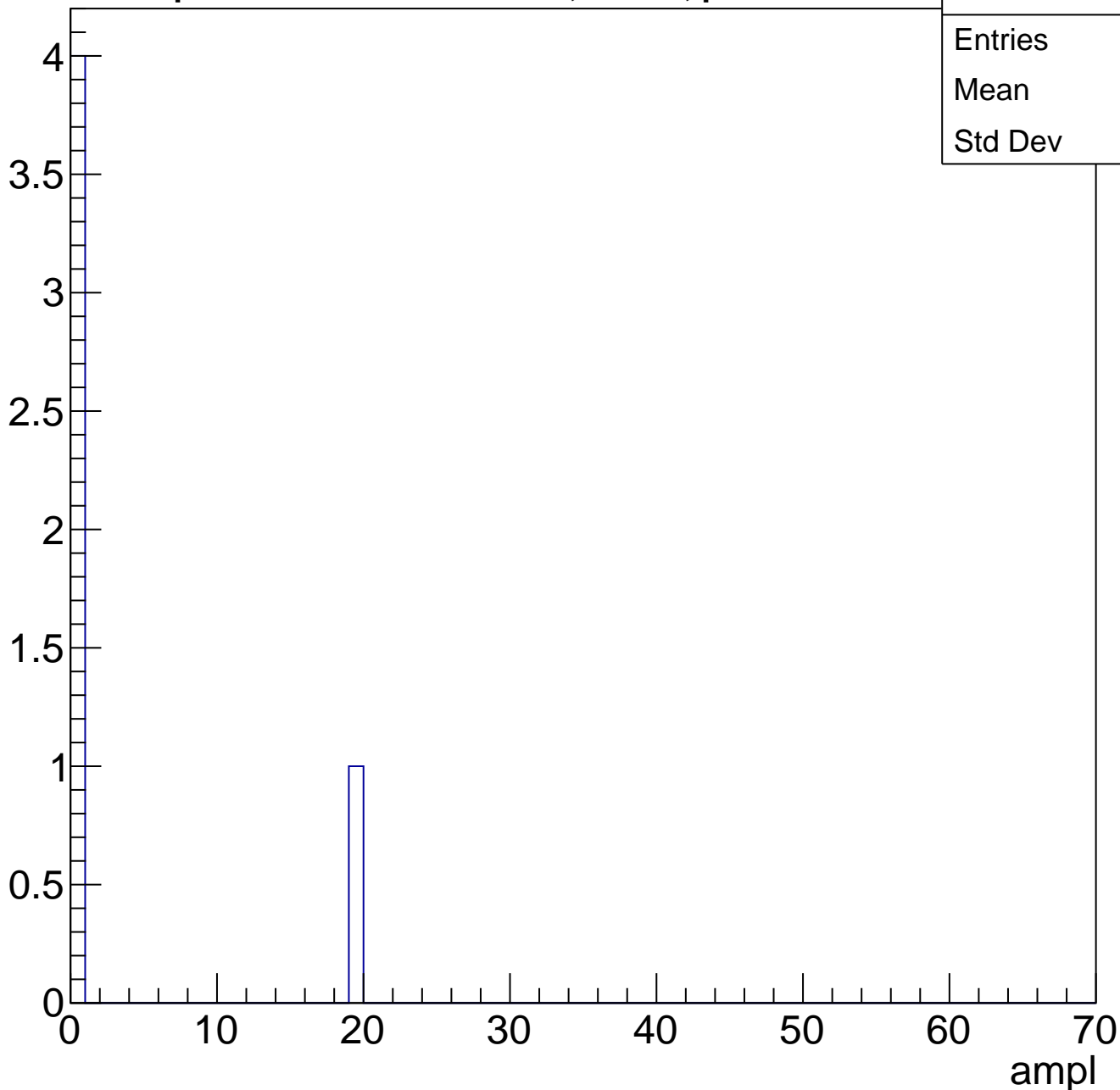




# B1L003S, U11-ch37, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	5
Mean	3.8
Std Dev	7.6

# B1L003S, U11-ch38, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	72
Mean	29.58
Std Dev	4.561

**Gaus mean : 30.3923**

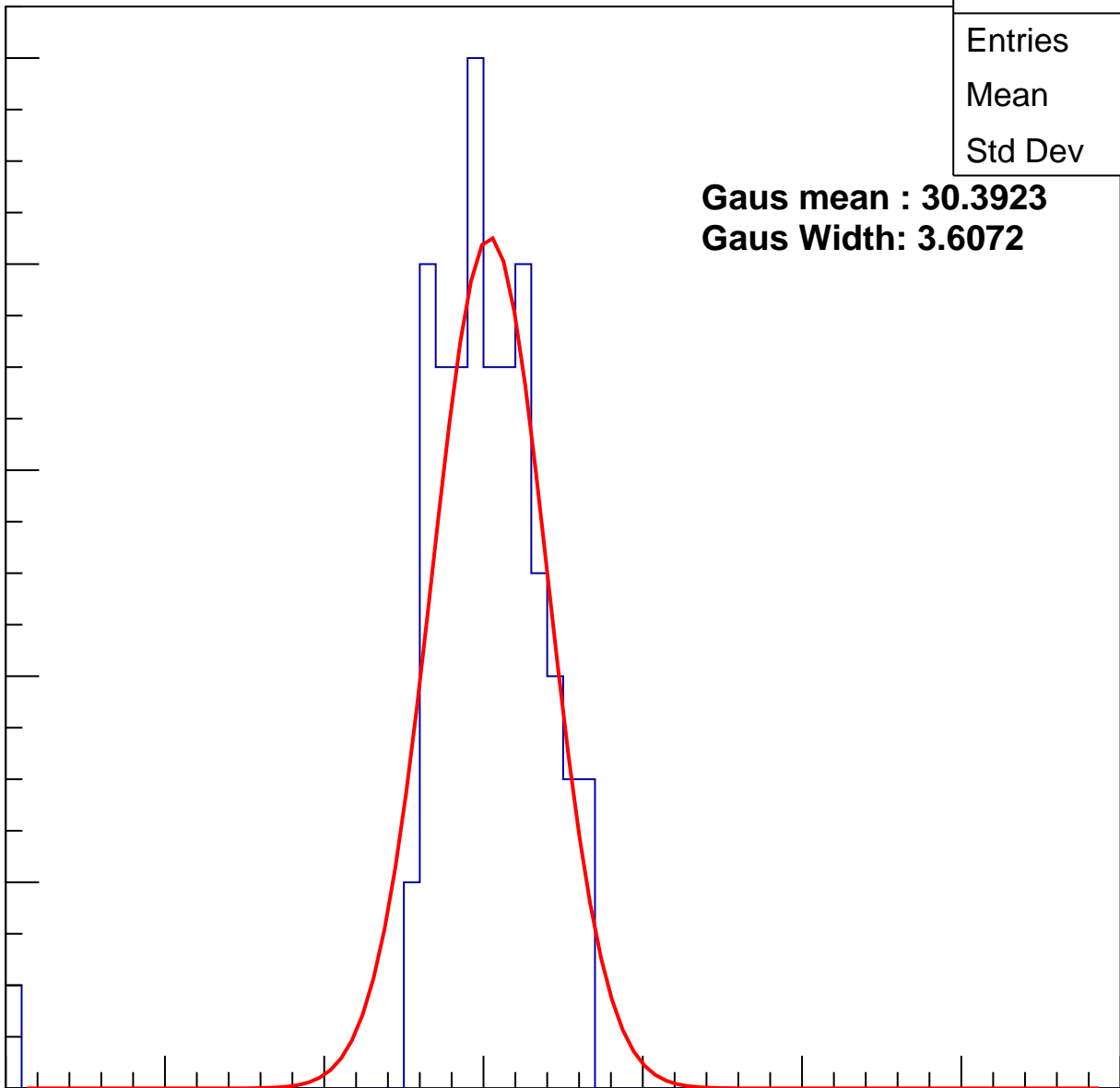
**Gaus Width: 3.6072**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

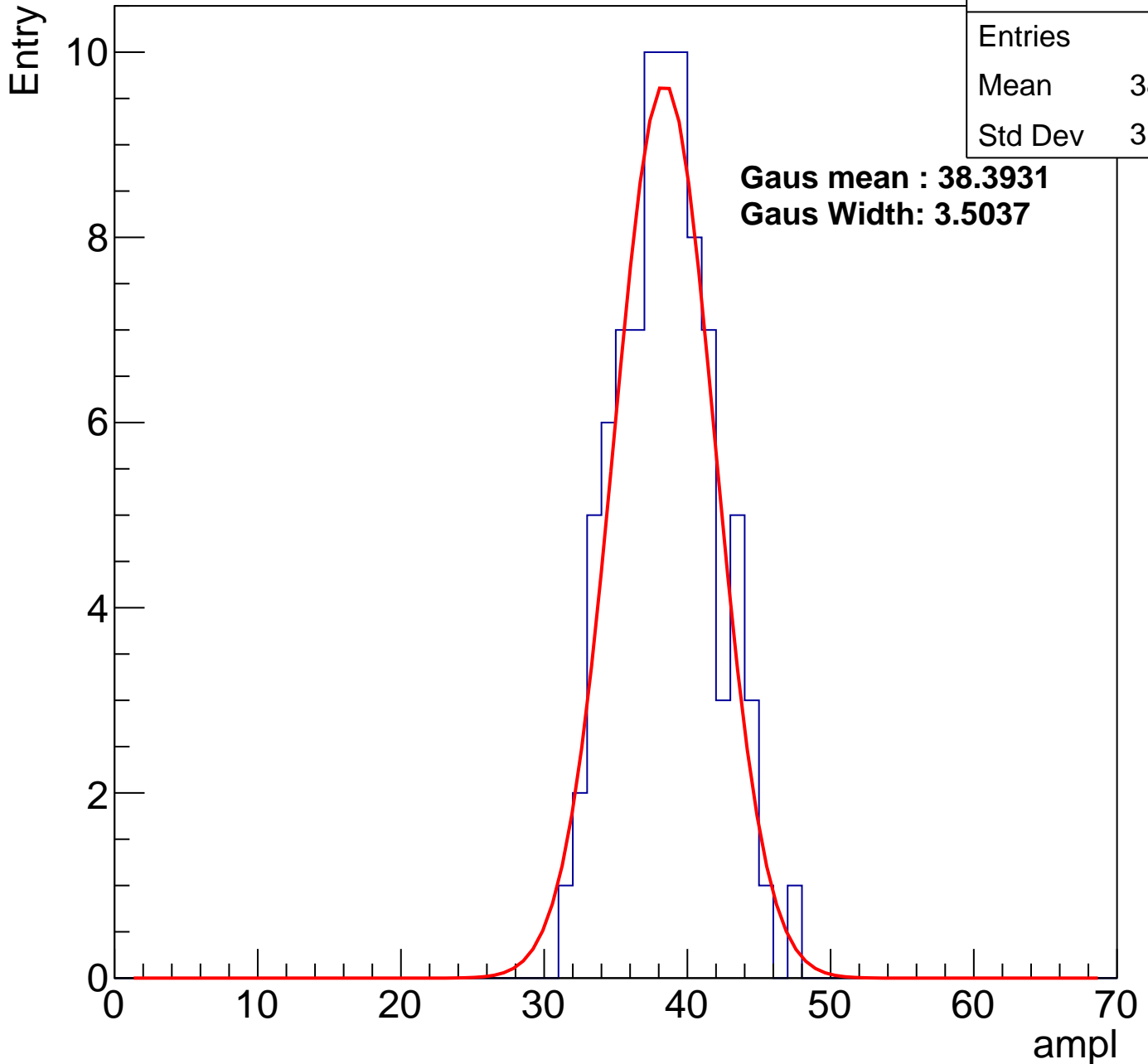


# B1L003S, U11-ch38, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	86
Mean	38.06
Std Dev	3.339

**Gaus mean : 38.3931**  
**Gaus Width: 3.5037**



# B1L003S, U11-ch38, adc2

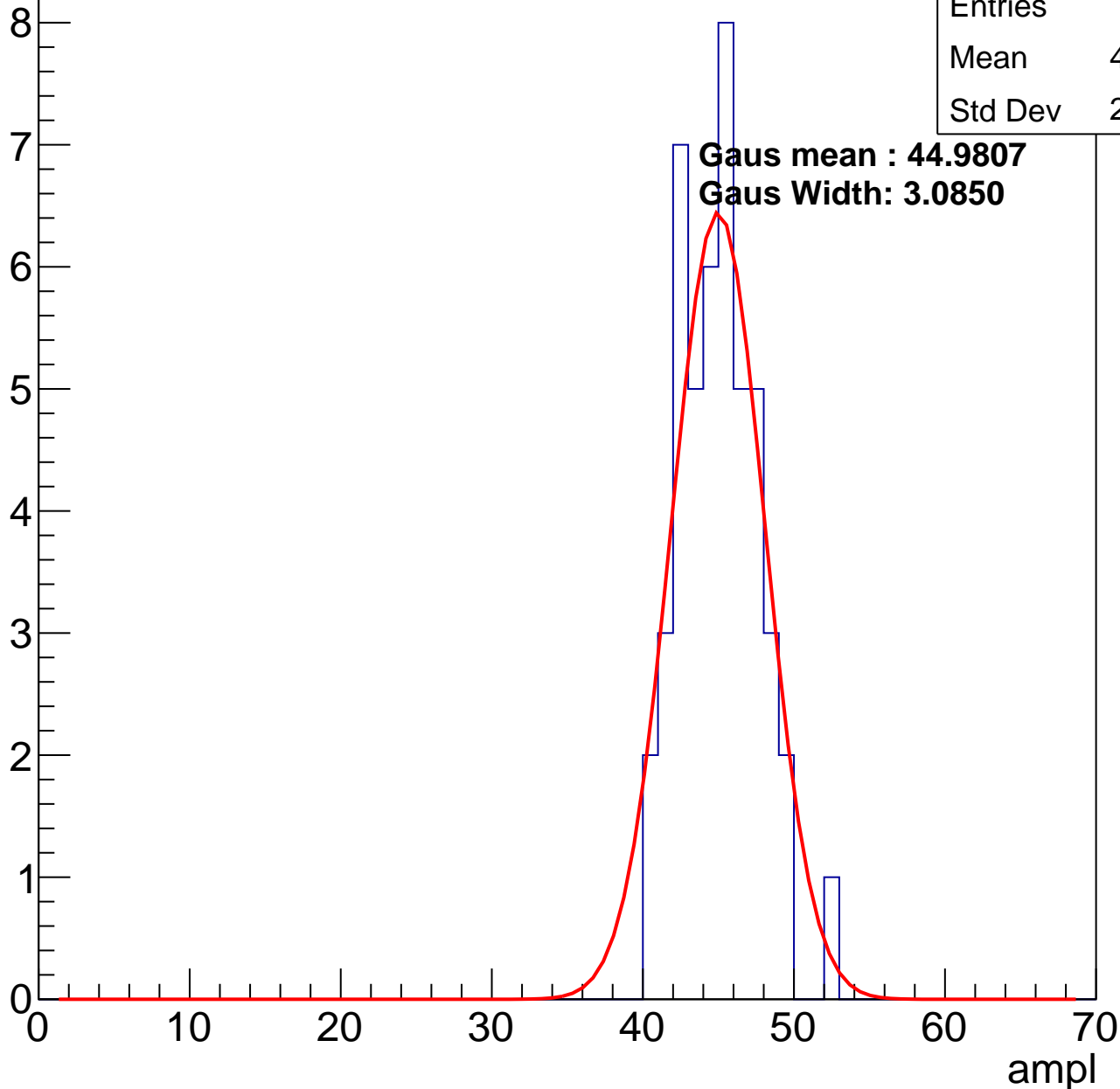
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	47
Mean	44.57
Std Dev	2.574

**Gaus mean : 44.9807**

**Gaus Width: 3.0850**

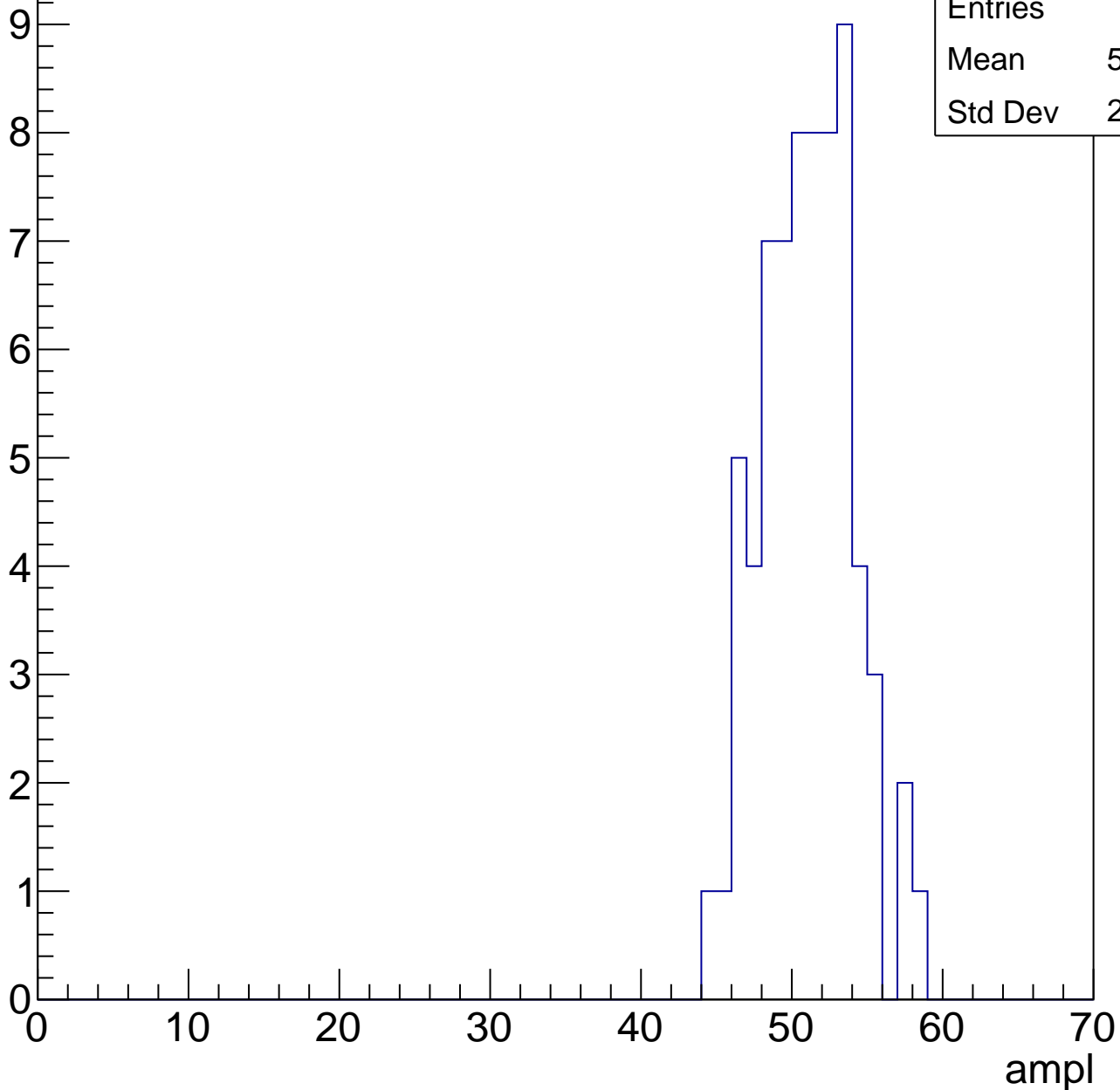


# B1L003S, U11-ch38, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	50.59
Std Dev	2.996



# B1L003S, U11-ch38, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

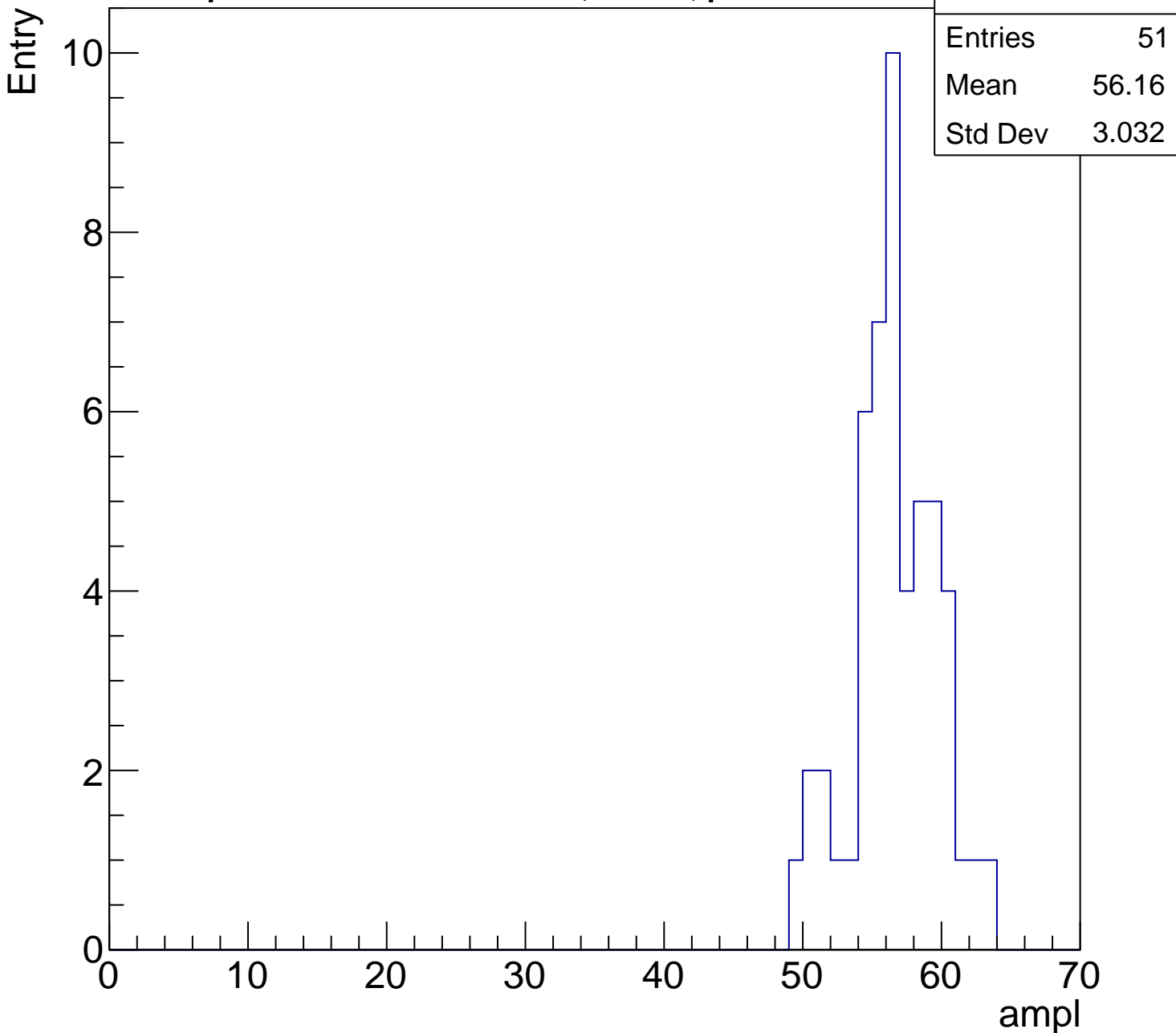
Entries	51
Mean	56.16
Std Dev	3.032

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

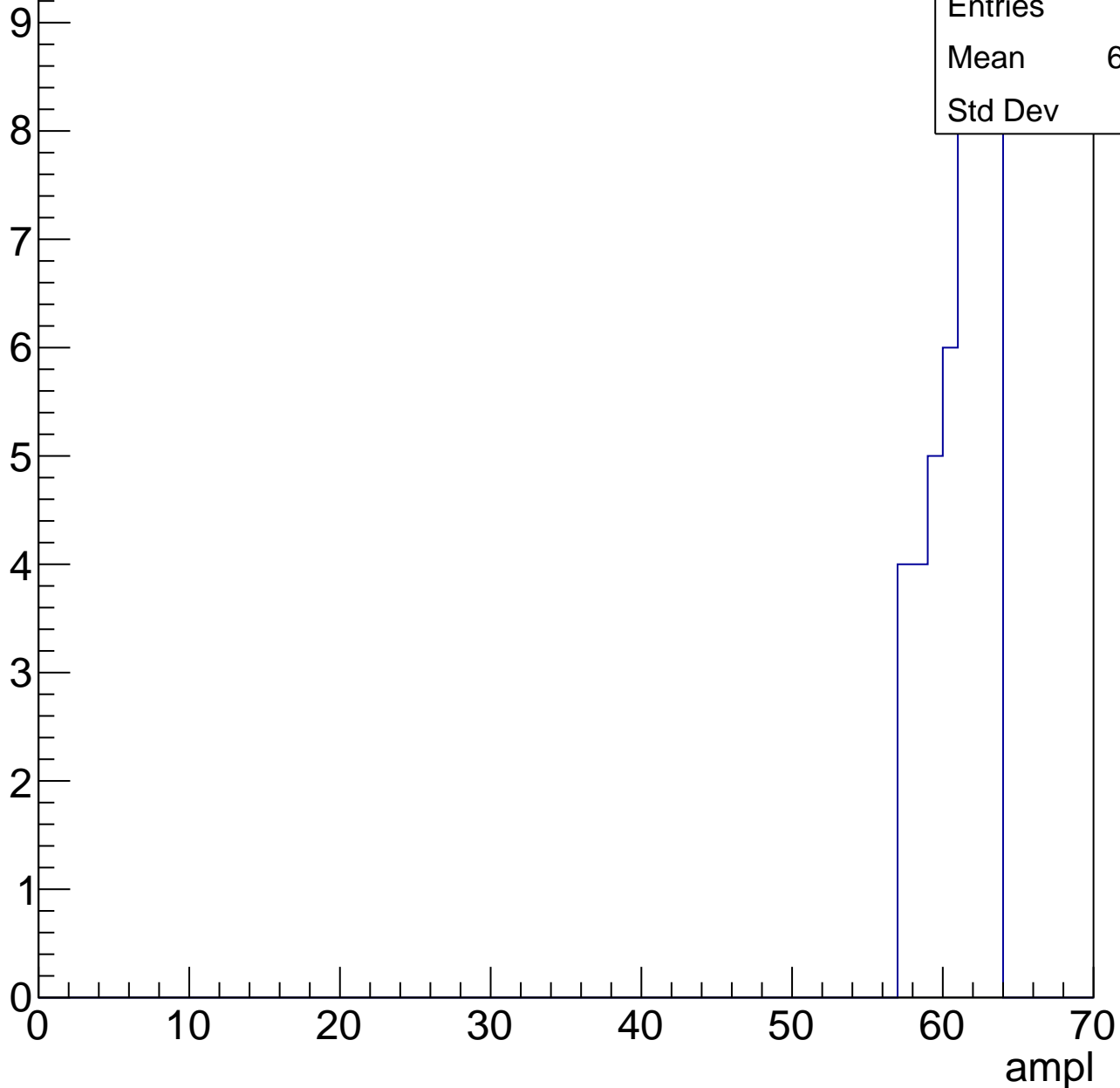
ampl



# B1L003S, U11-ch38, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

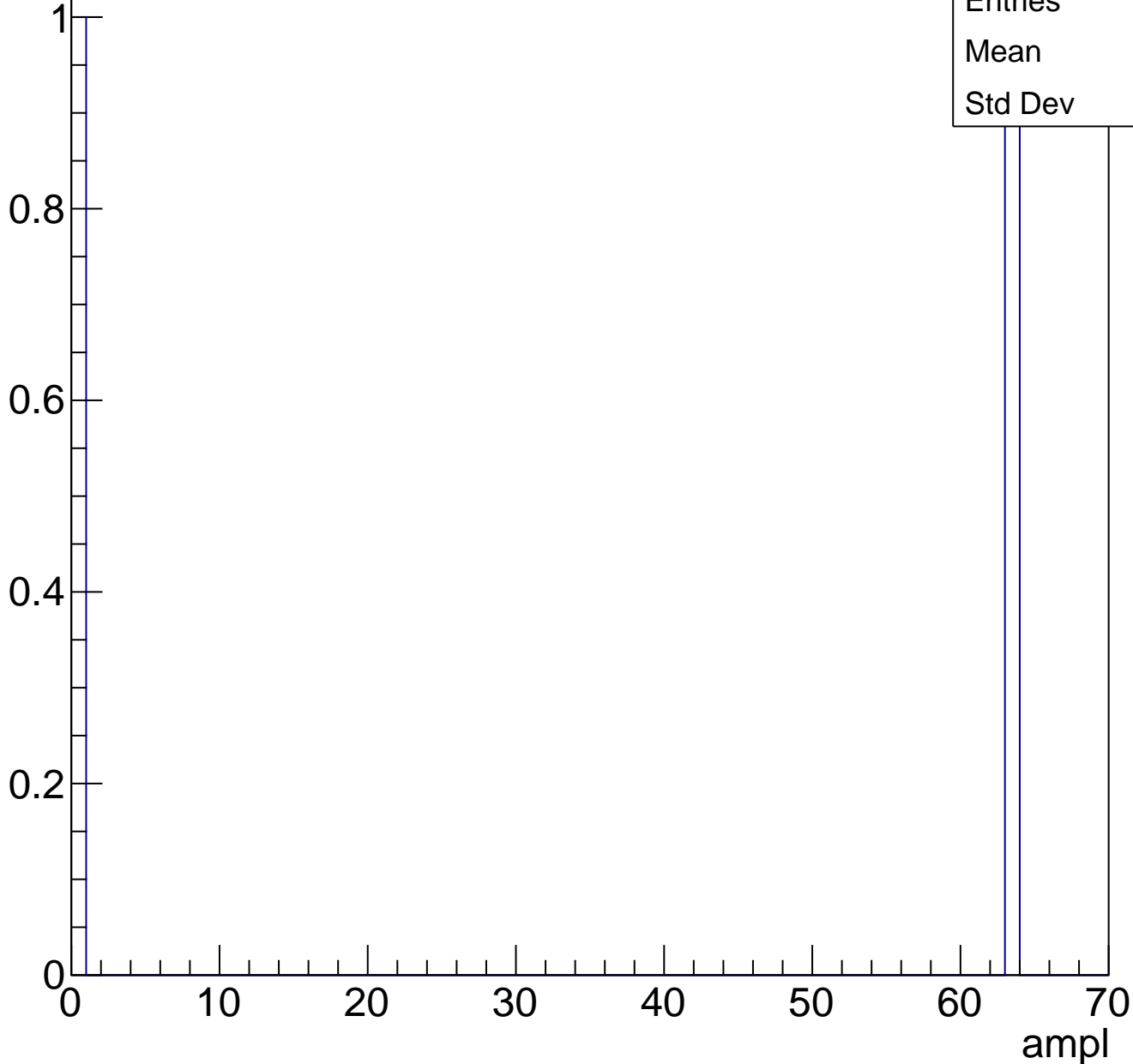


Entries	45
Mean	60.58
Std Dev	1.88

# B1L003S, U11-ch38, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch38, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U11-ch39, adc0

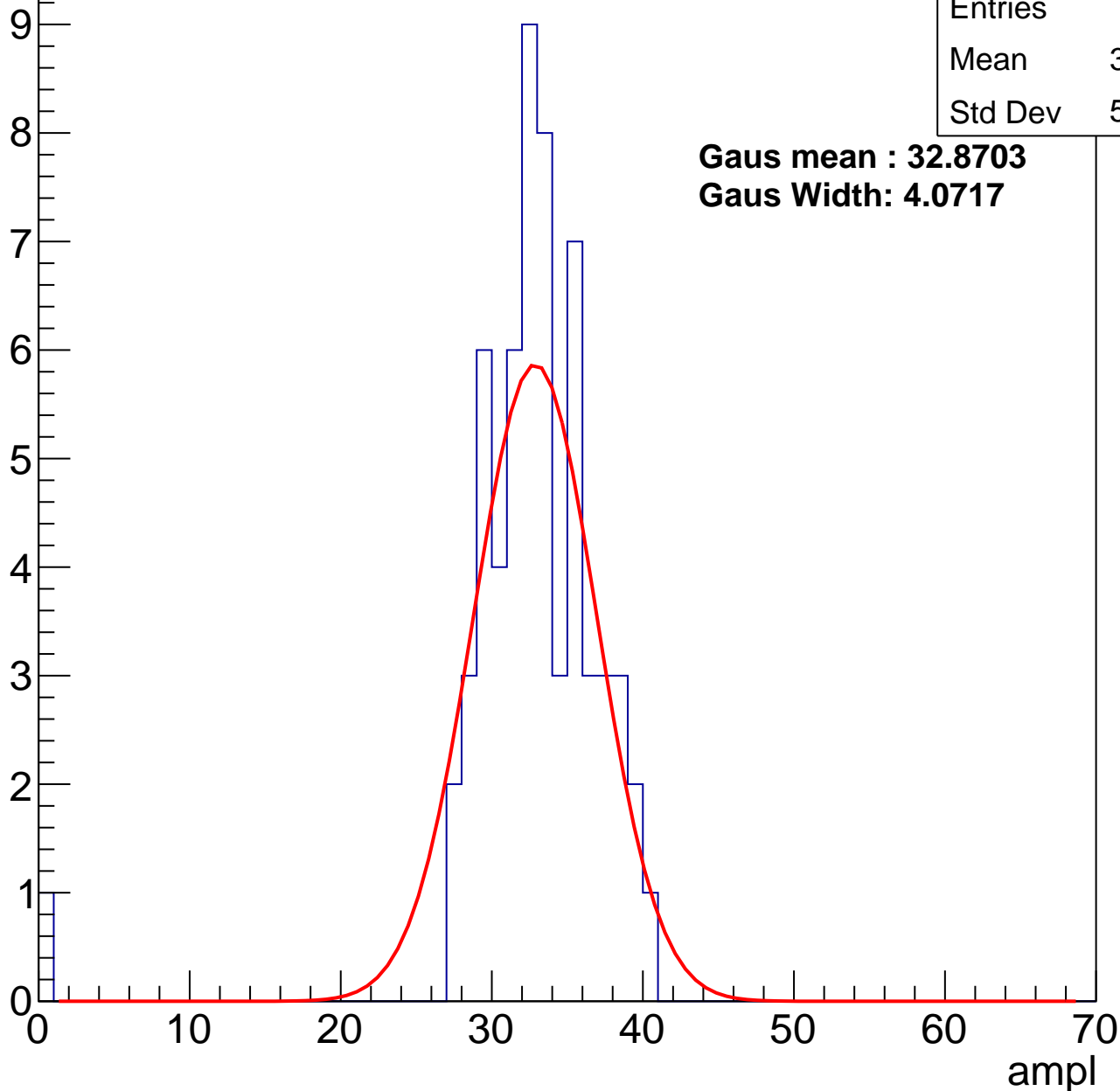
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	32.26
Std Dev	5.232

**Gaus mean : 32.8703**

**Gaus Width: 4.0717**



# B1L003S, U11-ch39, adc1

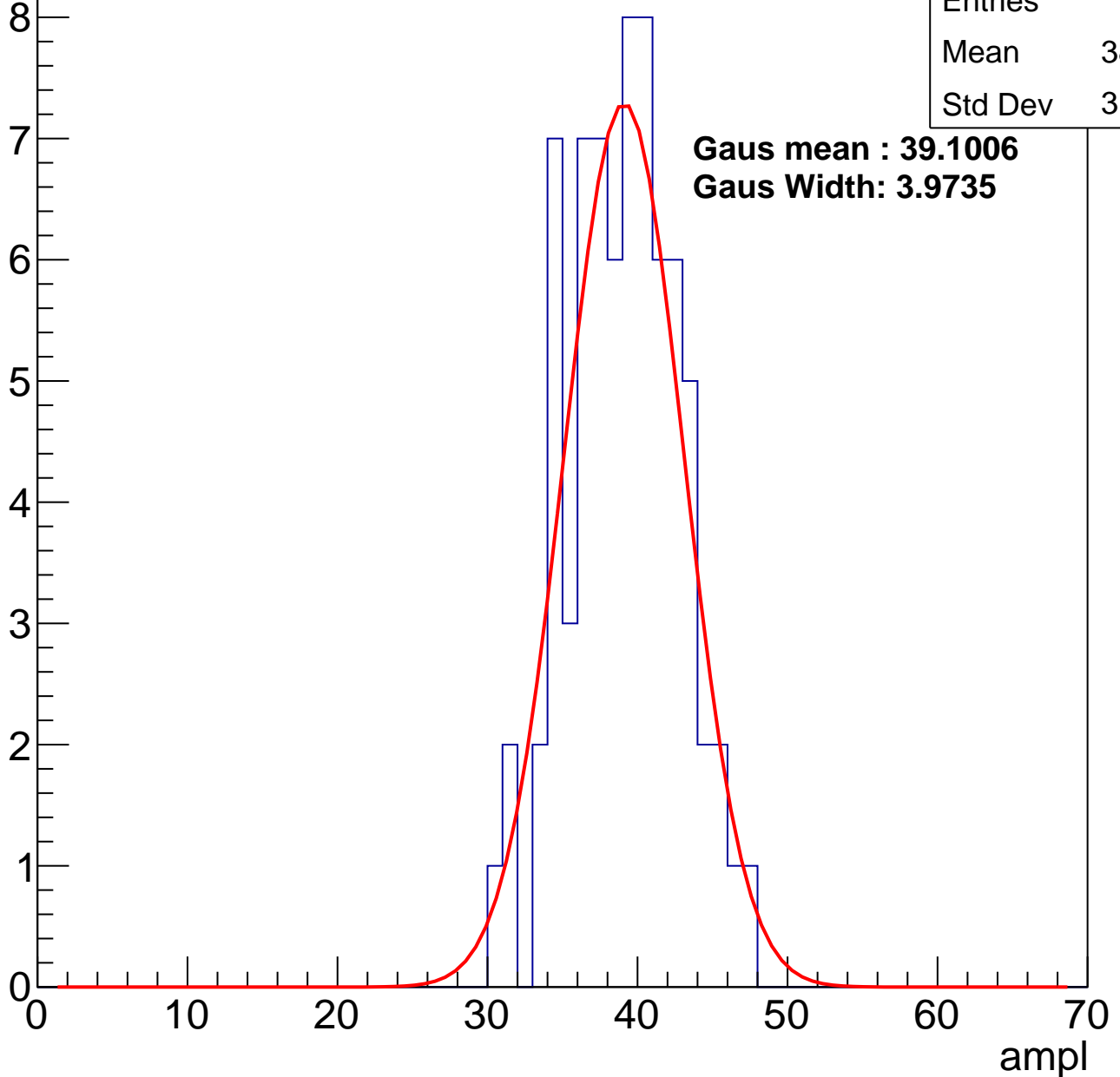
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	74
Mean	38.59
Std Dev	3.657

**Gaus mean : 39.1006**

**Gaus Width: 3.9735**



# B1L003S, U11-ch39, adc2

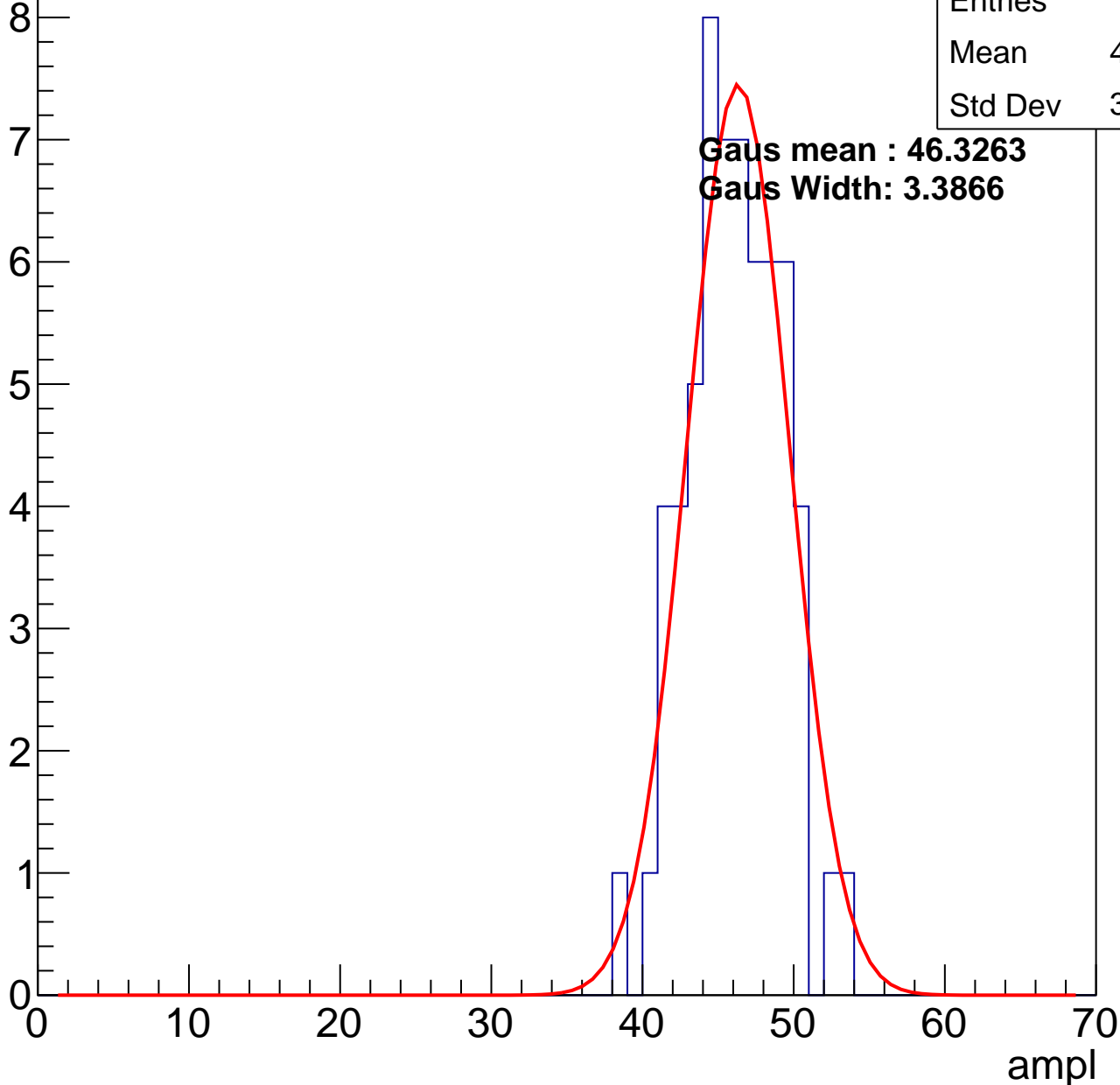
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	45.62
Std Dev	3.063

**Gaus mean : 46.3263**

**Gaus Width: 3.3866**

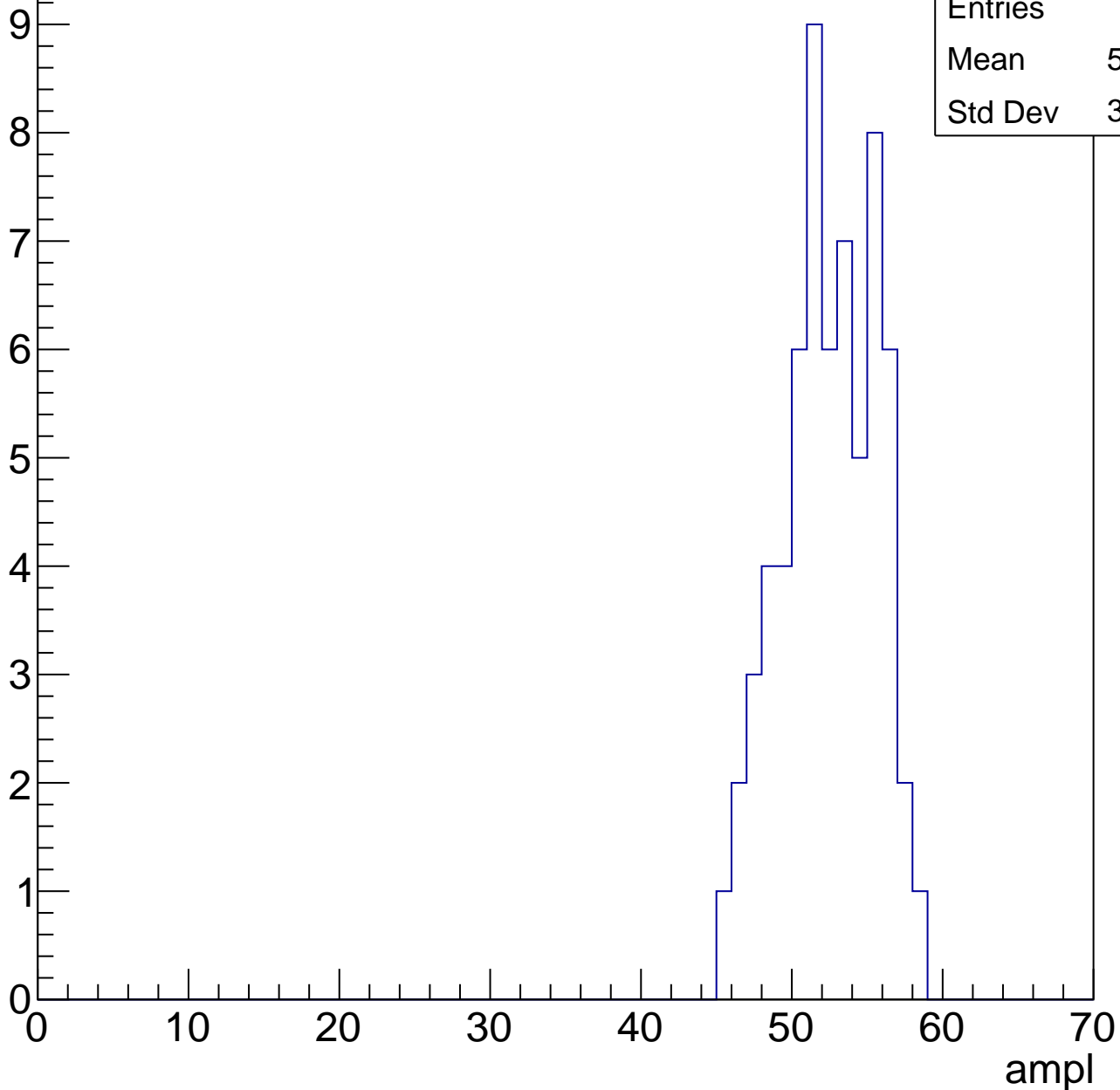


# B1L003S, U11-ch39, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	51.97
Std Dev	3.087

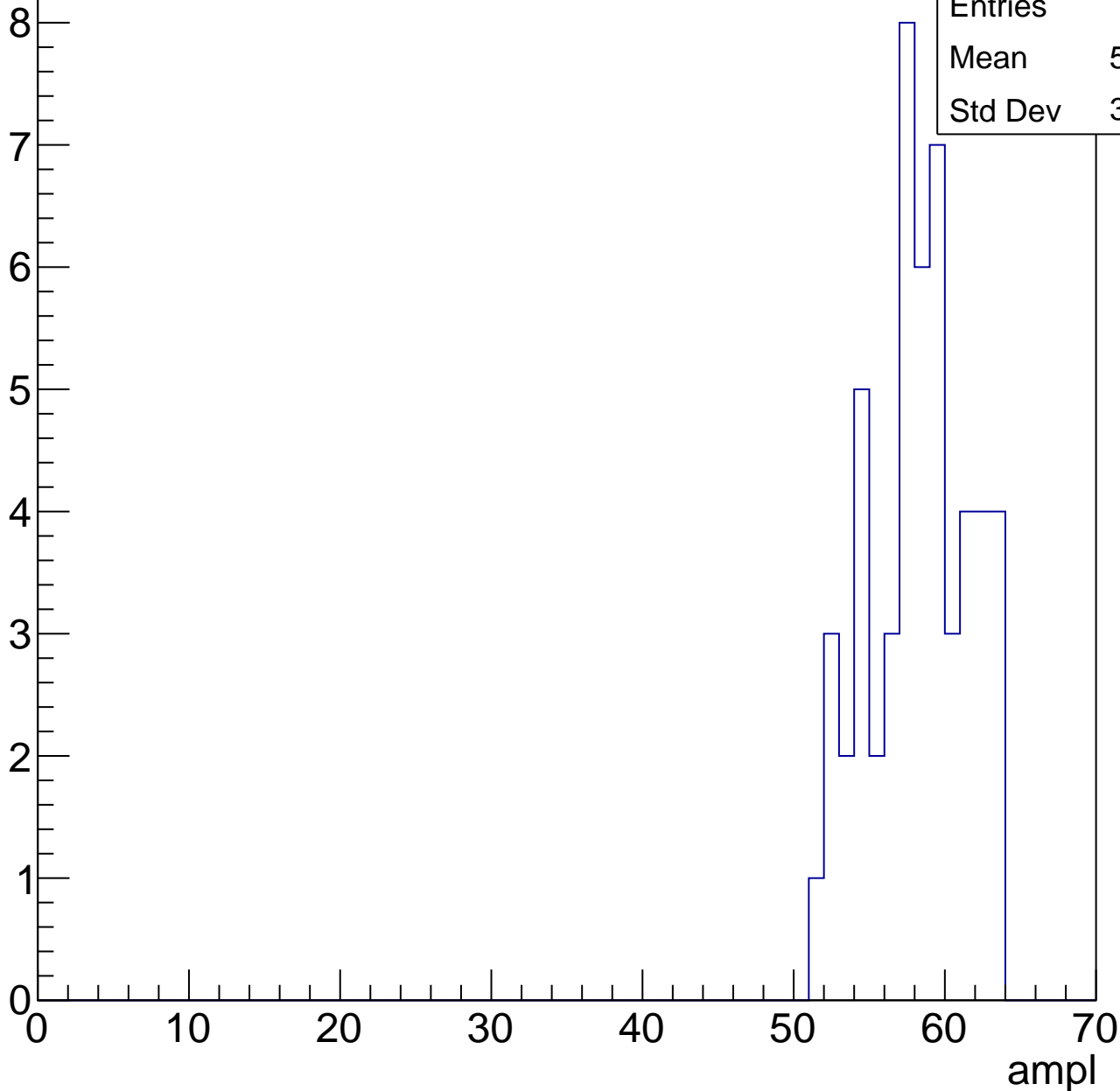


# B1L003S, U11-ch39, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	52
Mean	57.73
Std Dev	3.223



# B1L003S, U11-ch39, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

7

6

5

4

3

2

1

0

Entries	33
Mean	58.88
Std Dev	10.55

ampl

# B1L003S, U11-ch39, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch39, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L003S, U11-ch40, adc0

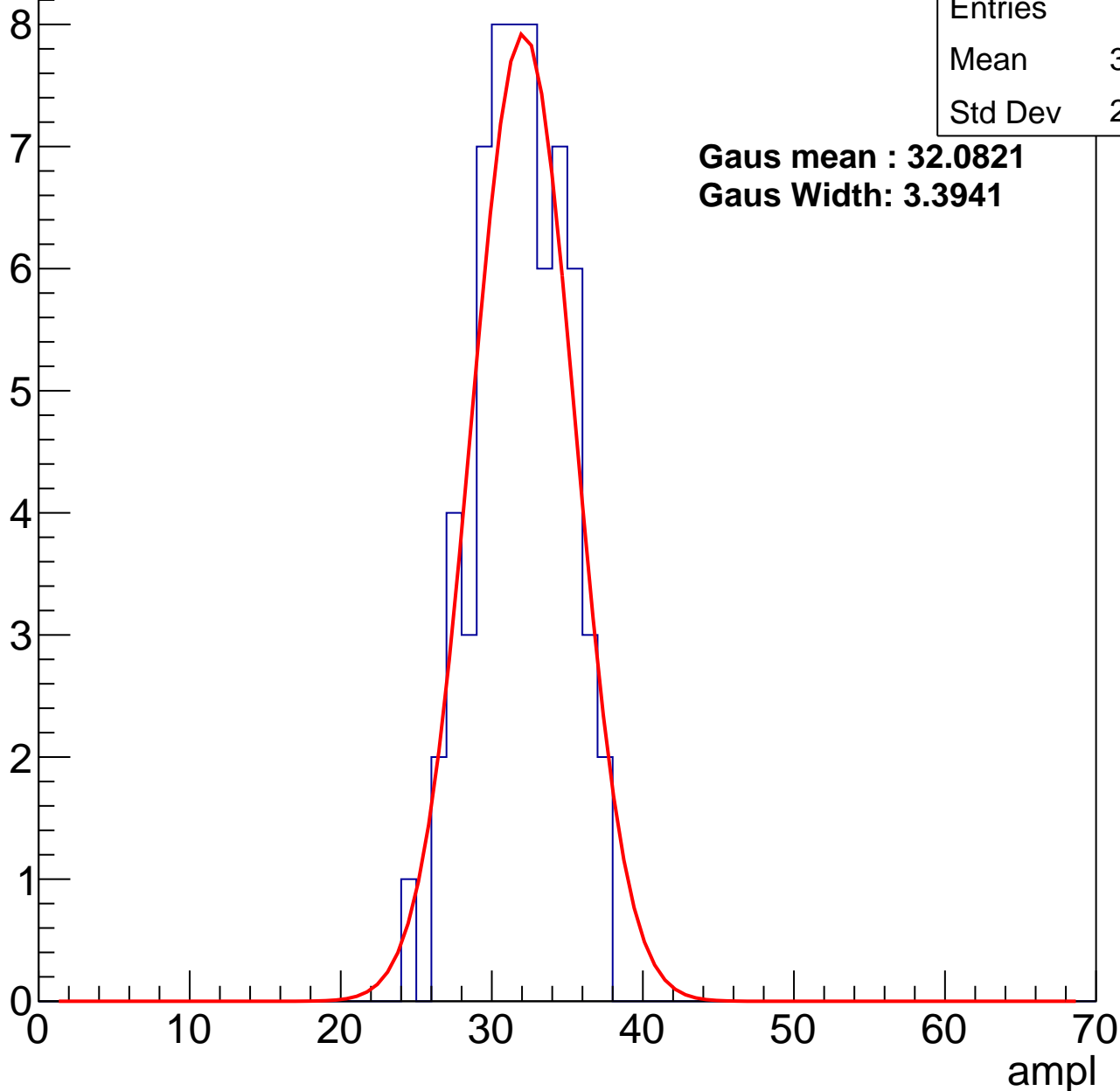
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	31.43
Std Dev	2.914

**Gaus mean : 32.0821**

**Gaus Width: 3.3941**

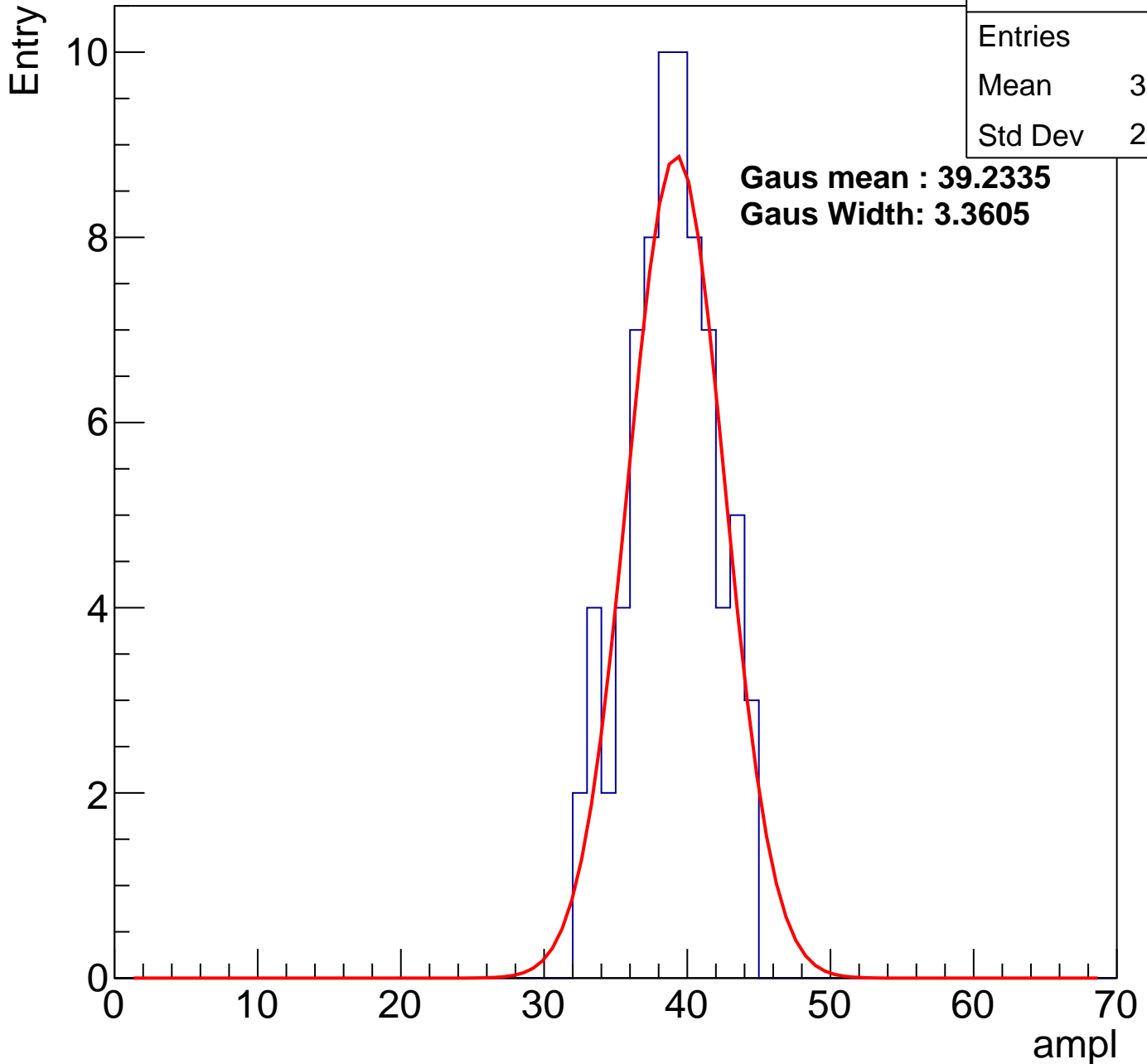


# B1L003S, U11-ch40, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	74
Mean	38.43
Std Dev	2.996

**Gaus mean : 39.2335**  
**Gaus Width: 3.3605**



# B1L003S, U11-ch40, adc2

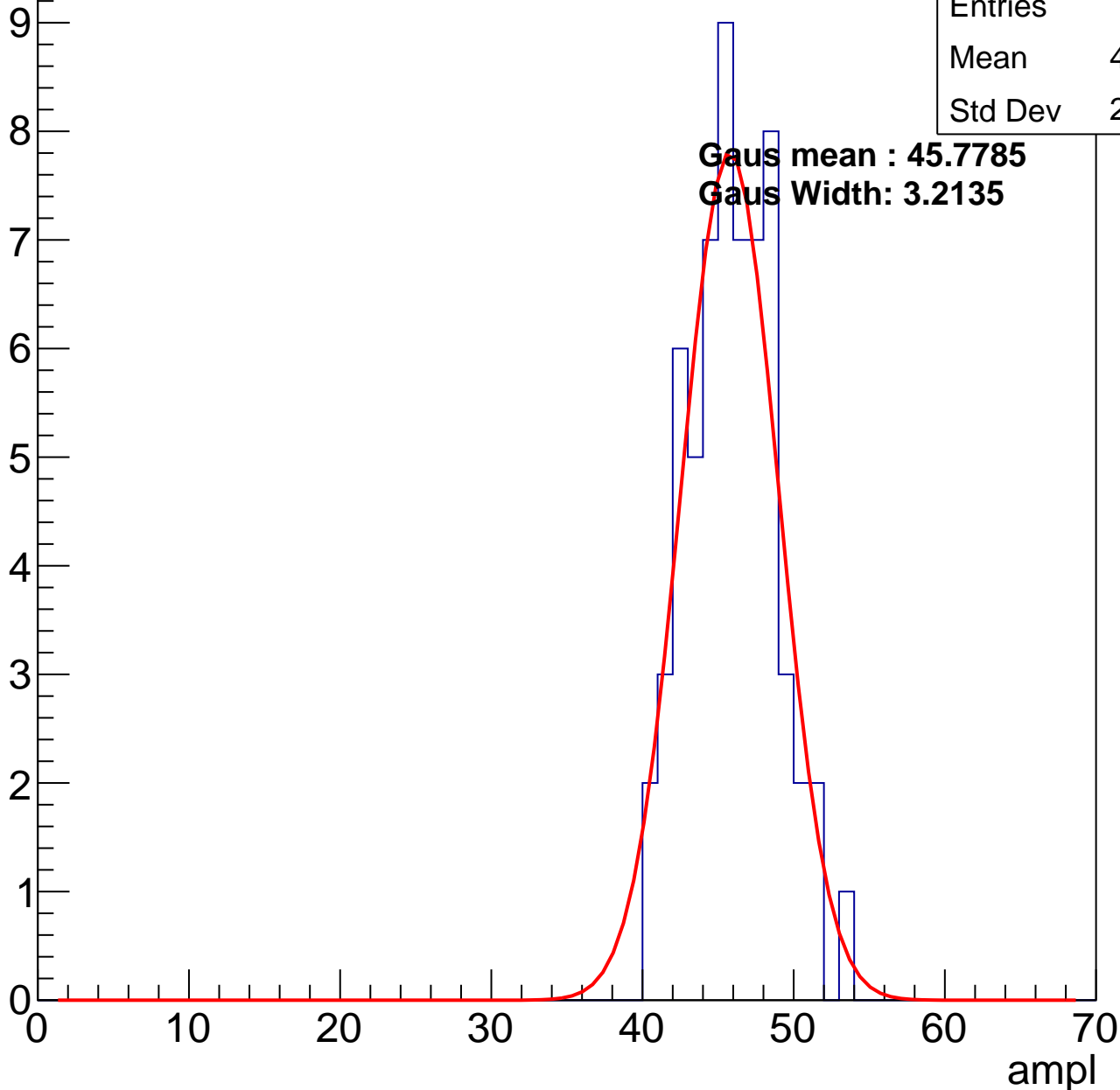
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	45.48
Std Dev	2.855

**Gaus mean : 45.7785**

**Gaus Width: 3.2135**

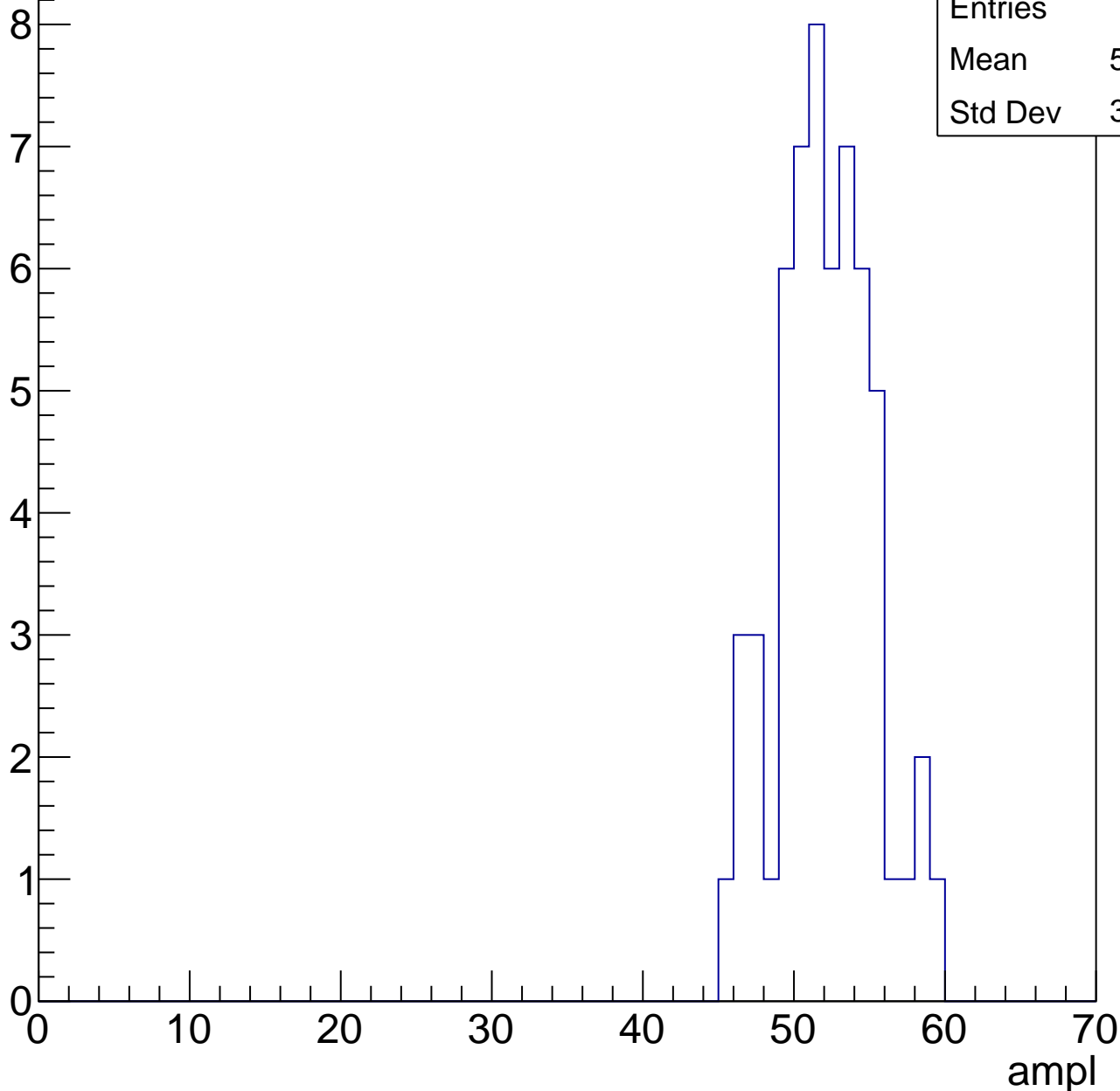


# B1L003S, U11-ch40, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	51.62
Std Dev	3.128

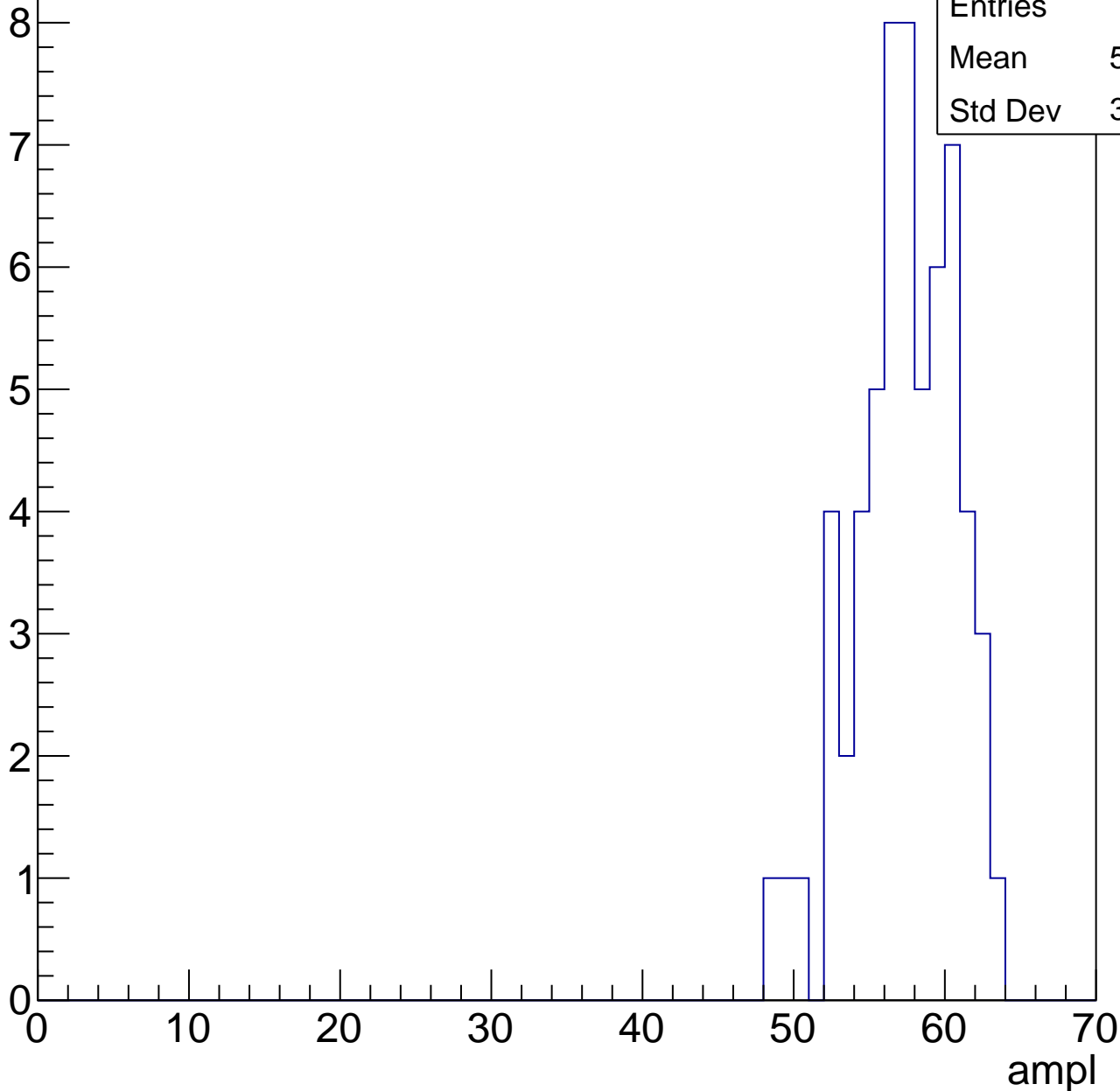


# B1L003S, U11-ch40, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	56.88
Std Dev	3.307

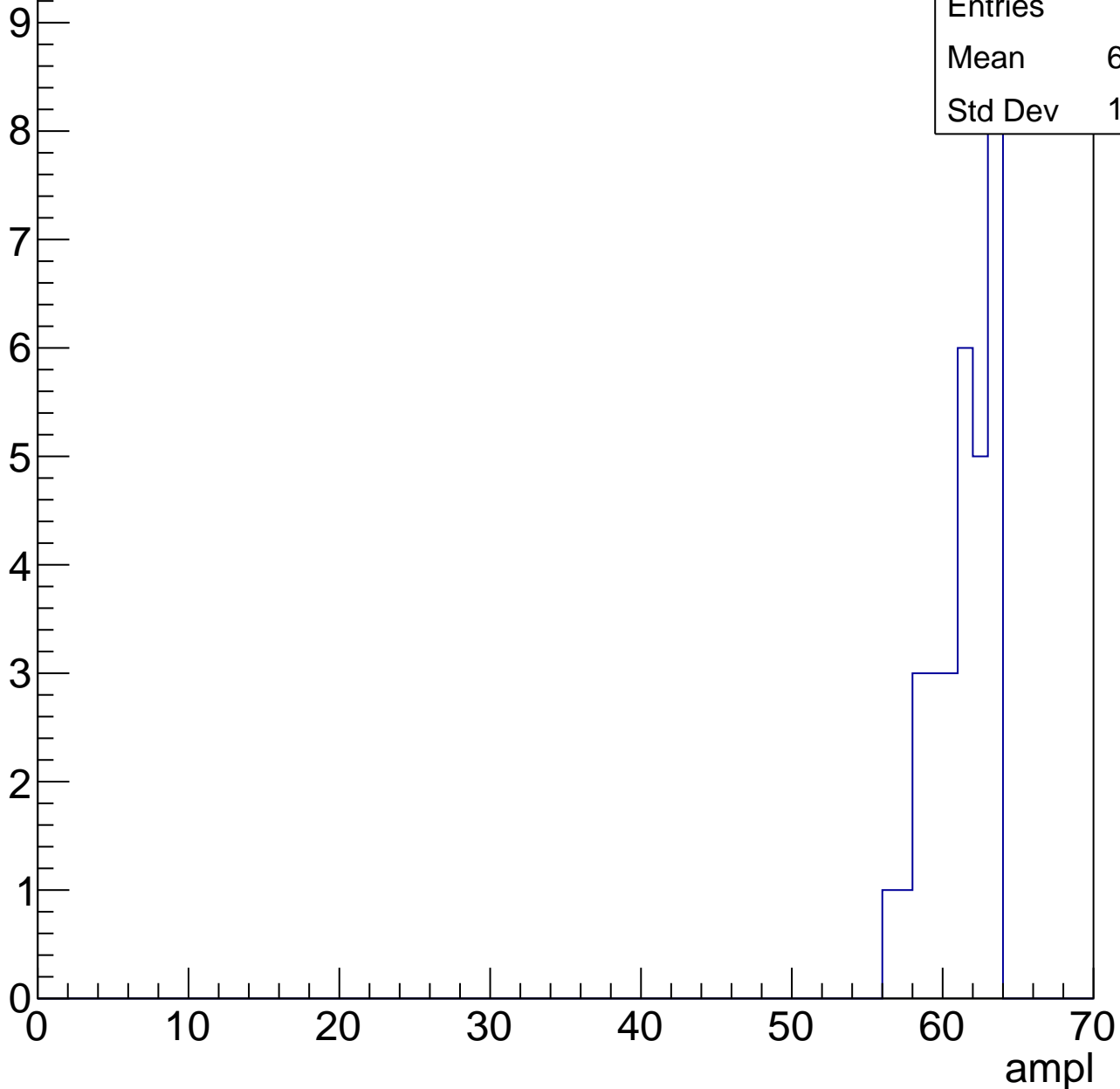


# B1L003S, U11-ch40, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

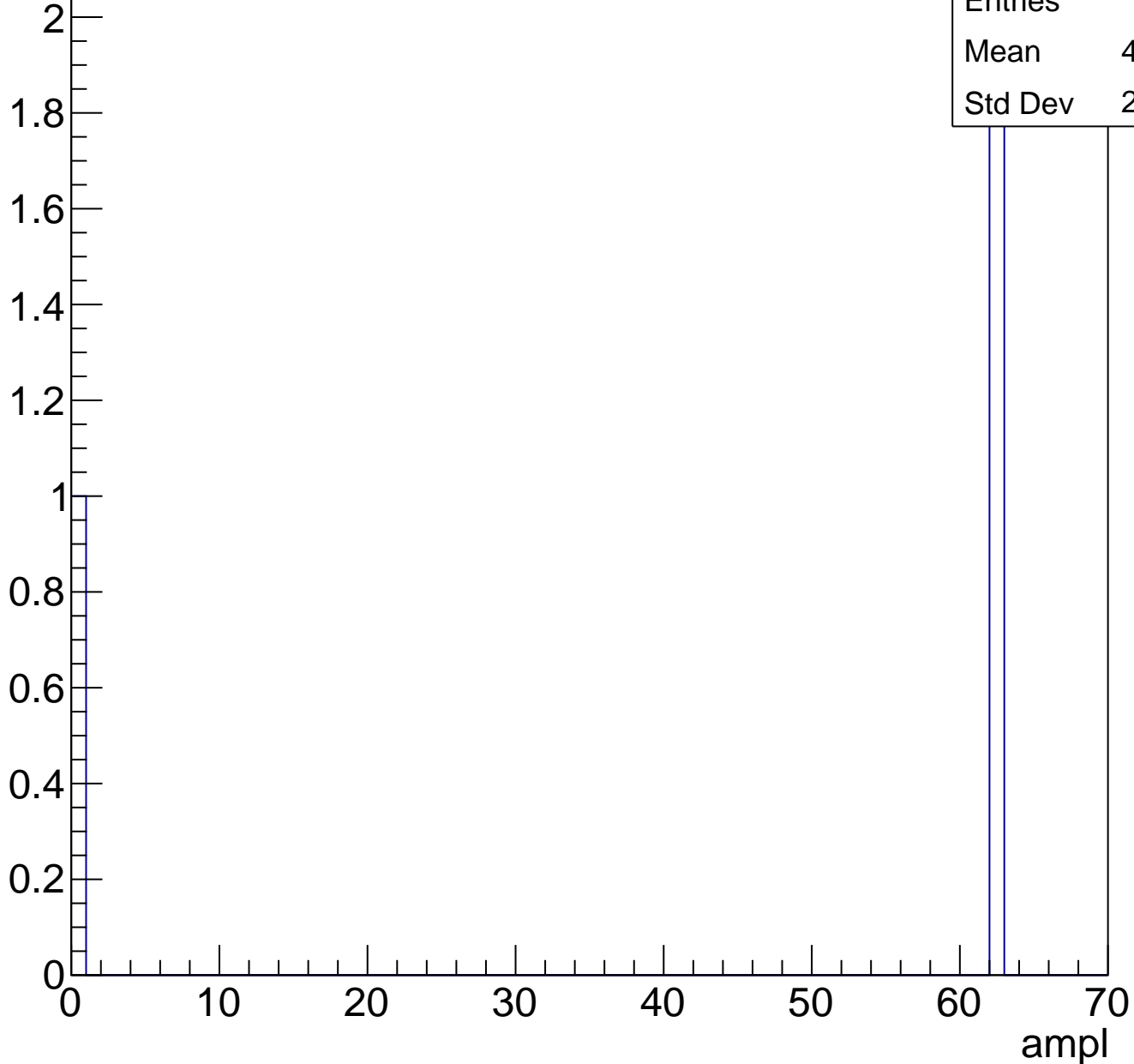
Entries	31
Mean	60.87
Std Dev	1.996



# B1L003S, U11-ch40, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch40, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U11-ch41, adc0

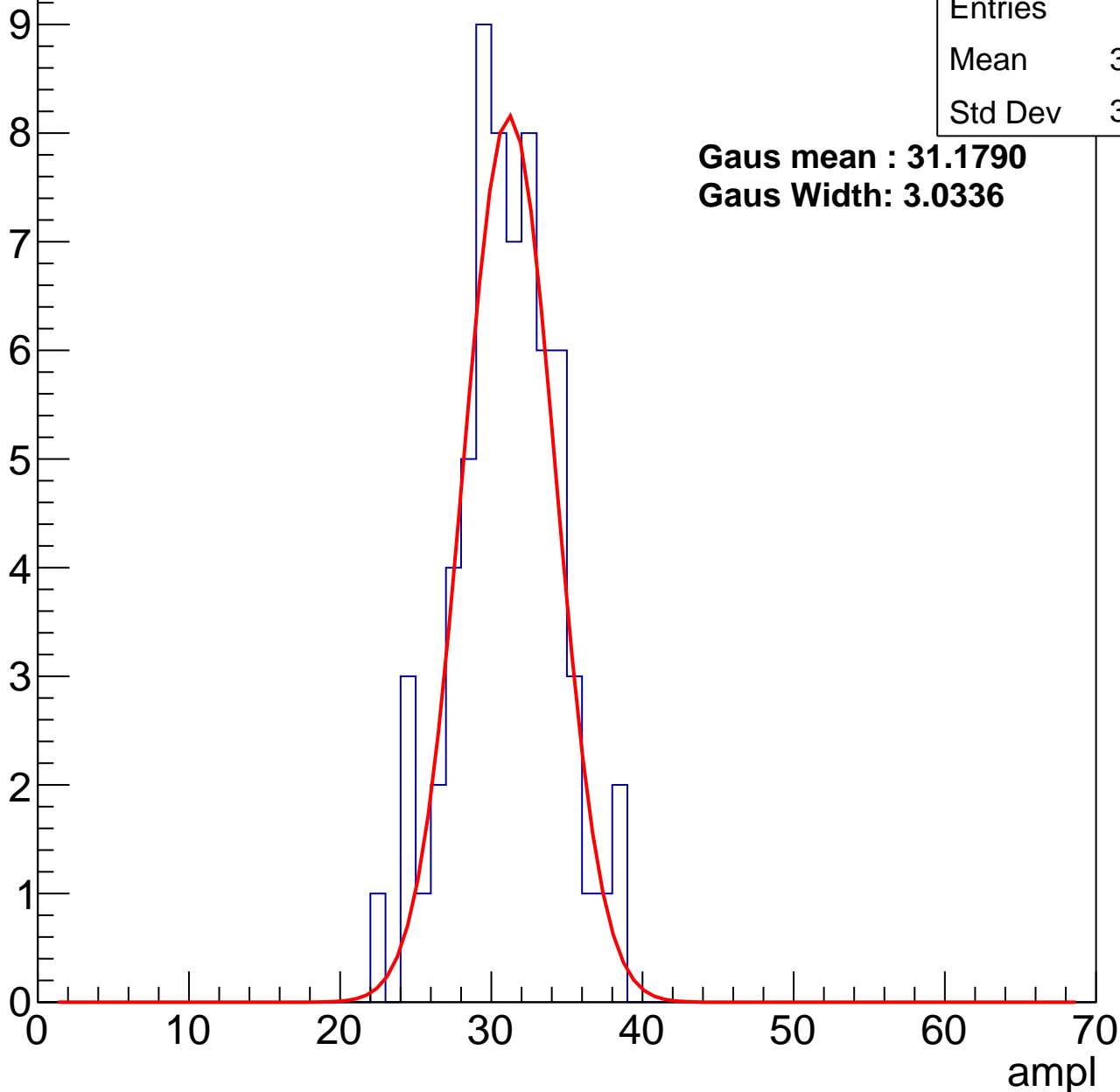
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	30.58
Std Dev	3.342

**Gaus mean : 31.1790**

**Gaus Width: 3.0336**



# B1L003S, U11-ch41, adc1

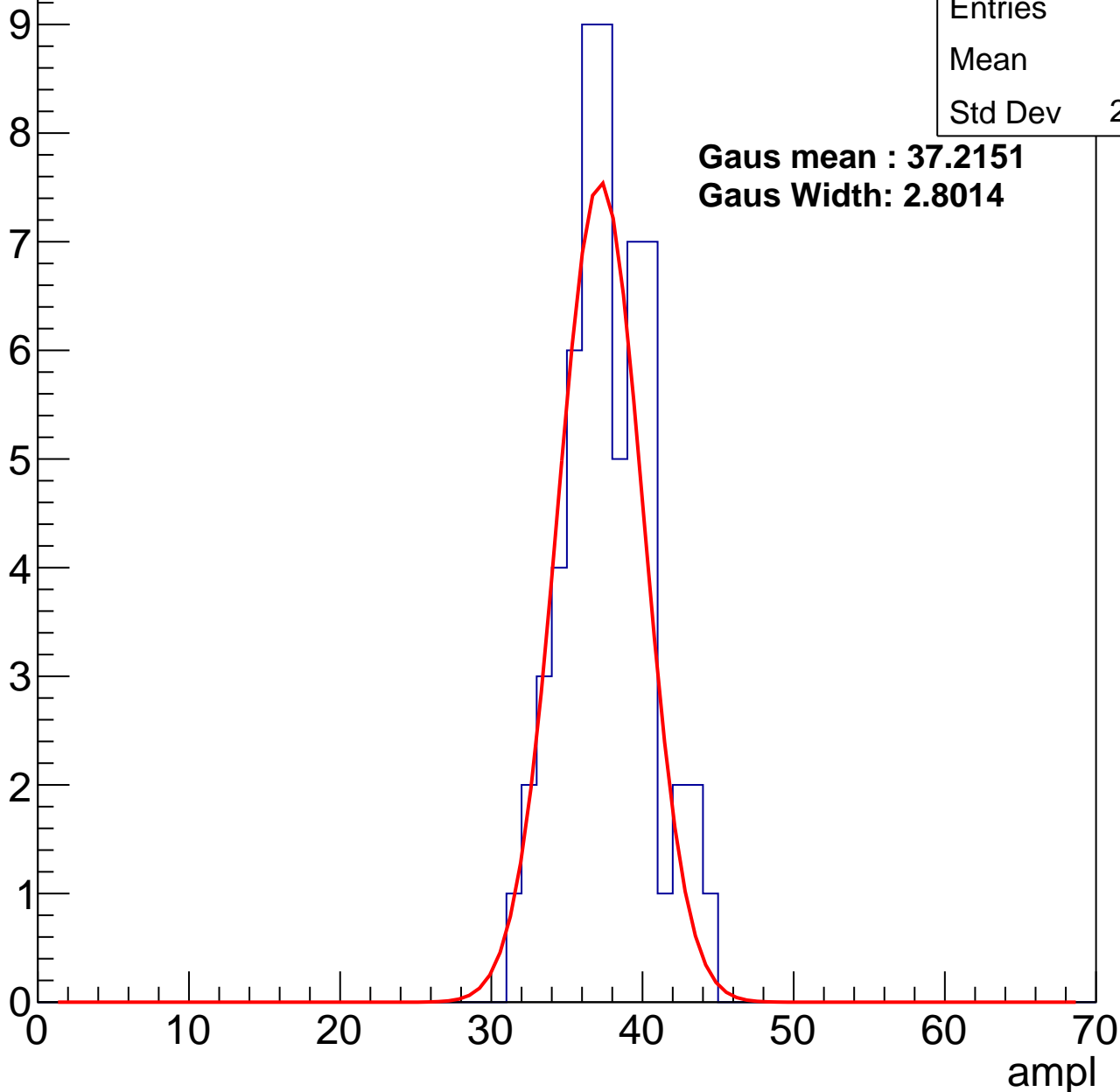
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	37.2
Std Dev	2.863

**Gaus mean : 37.2151**

**Gaus Width: 2.8014**



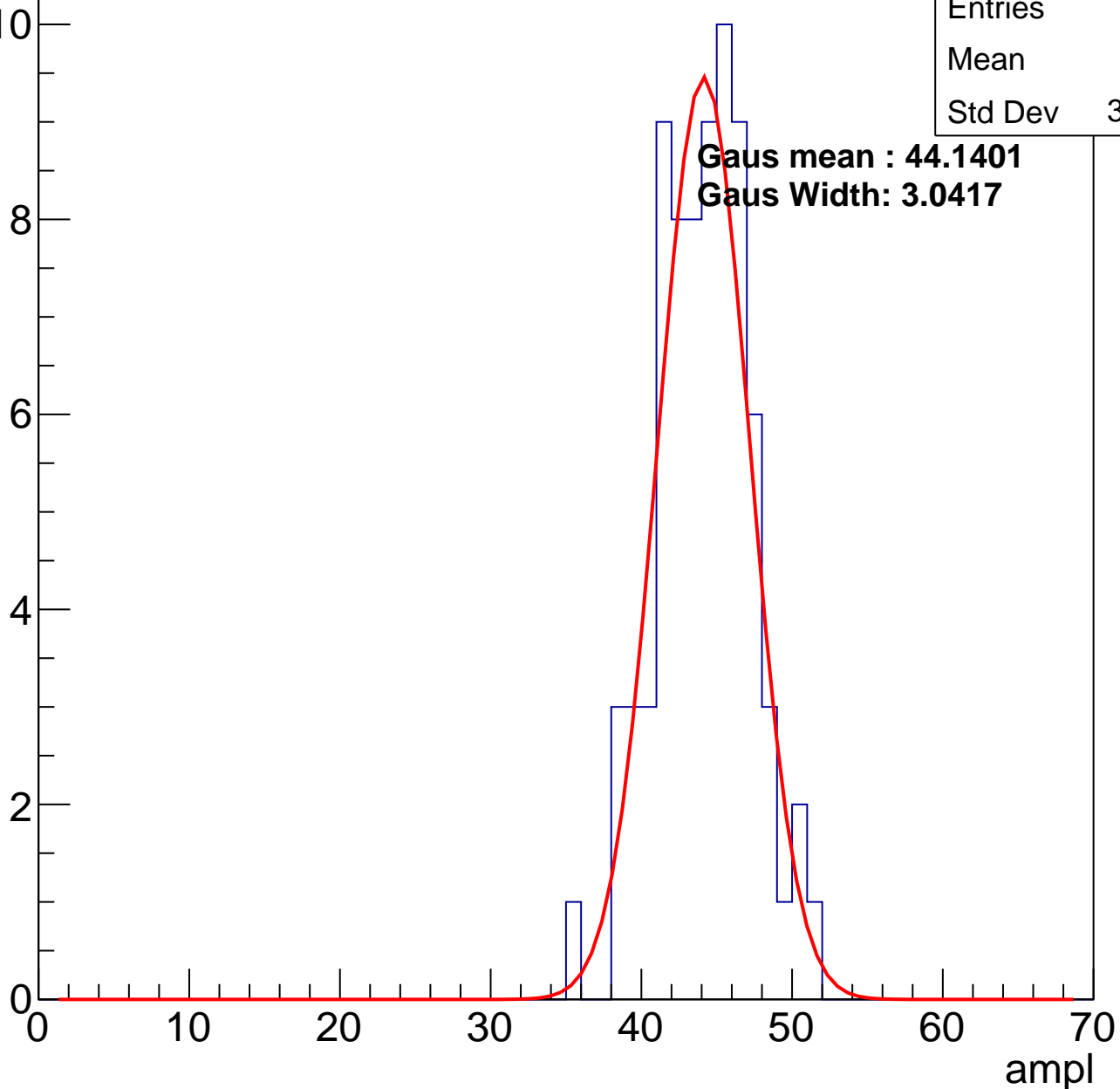
# B1L003S, U11-ch41, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	76
Mean	43.7
Std Dev	3.078

**Gaus mean : 44.1401**  
**Gaus Width: 3.0417**

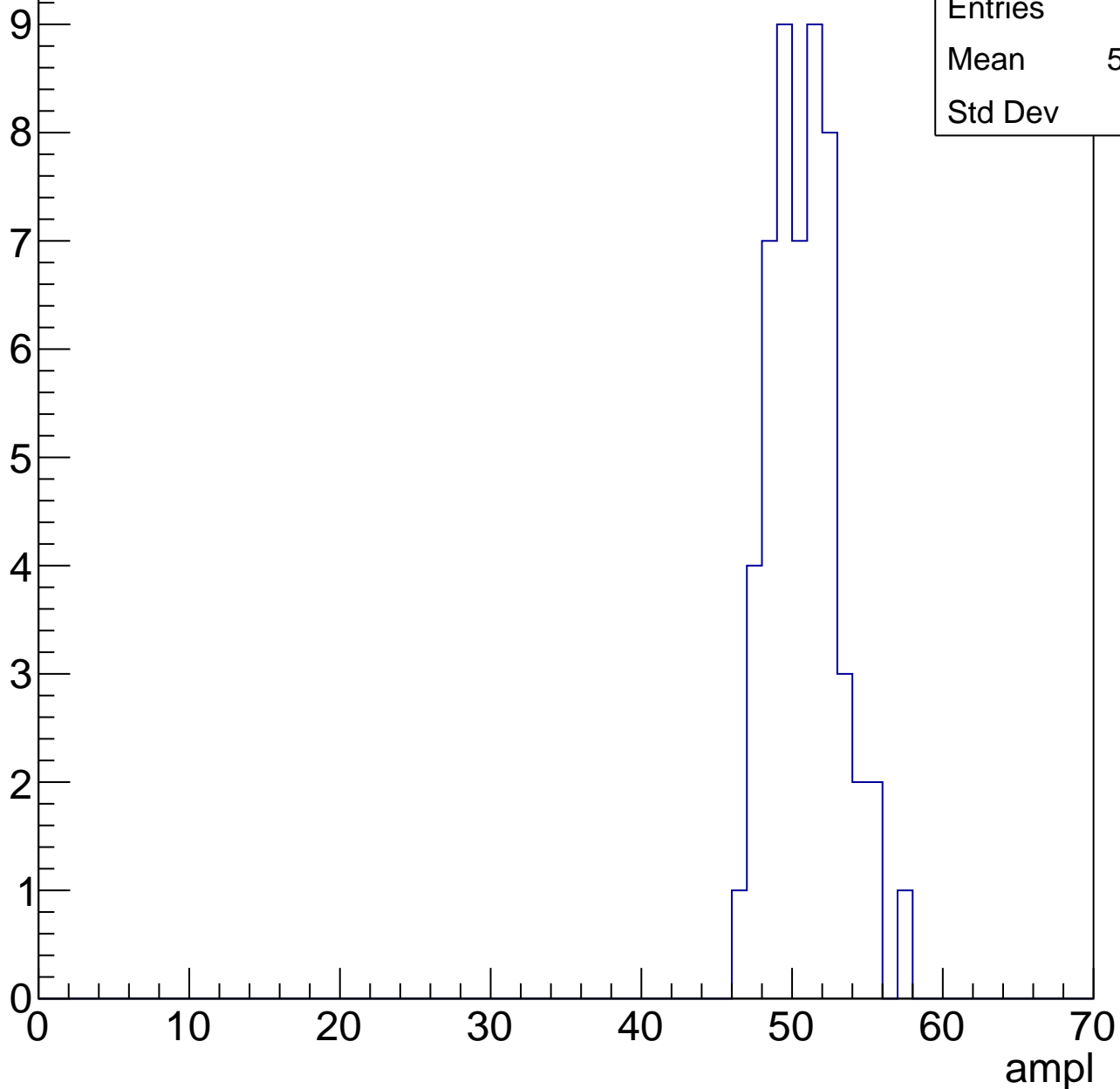
Entry



# B1L003S, U11-ch41, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



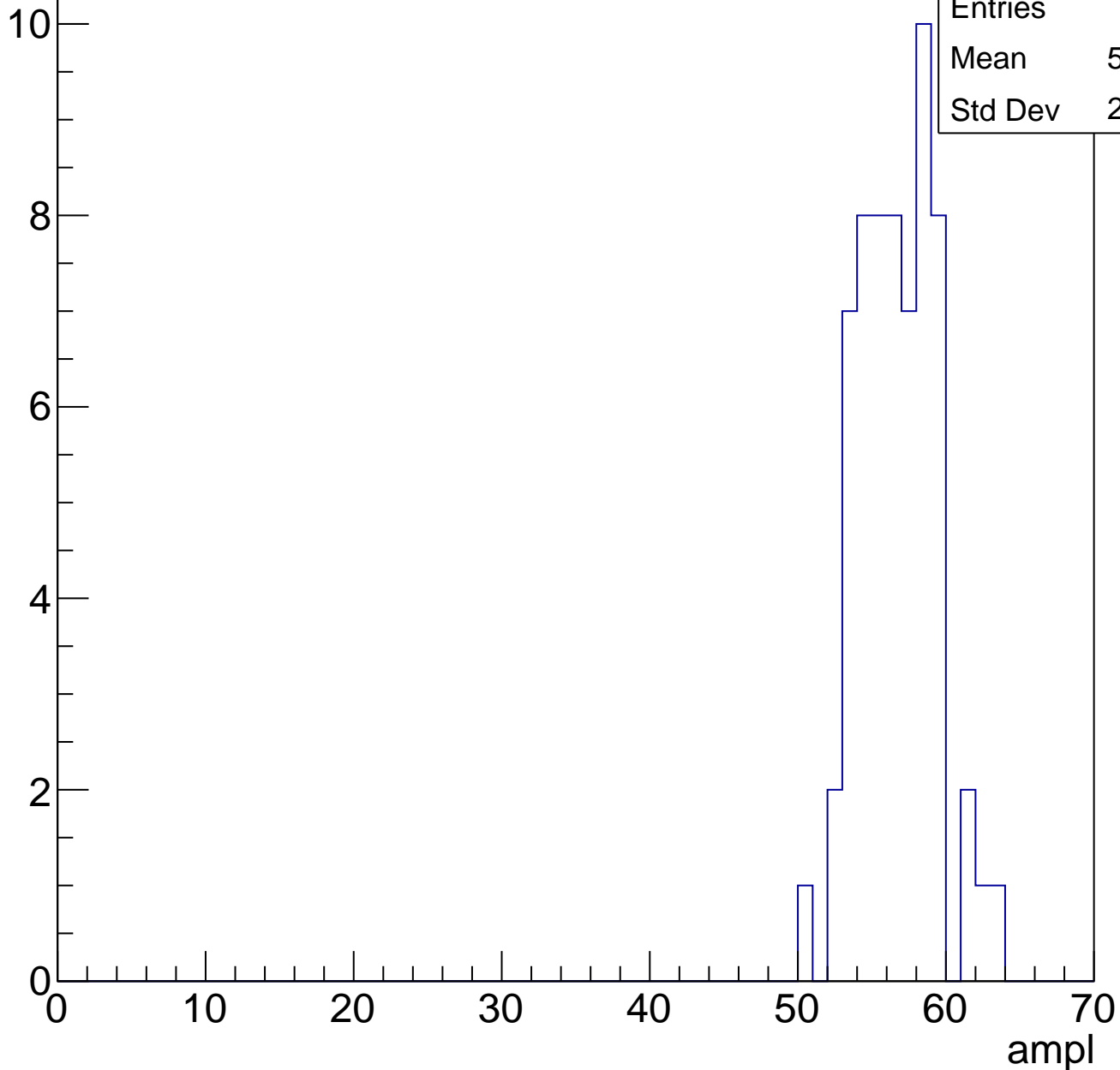
Entries	53
Mean	50.38
Std Dev	2.3

# B1L003S, U11-ch41, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	63
Mean	56.24
Std Dev	2.586

Entry

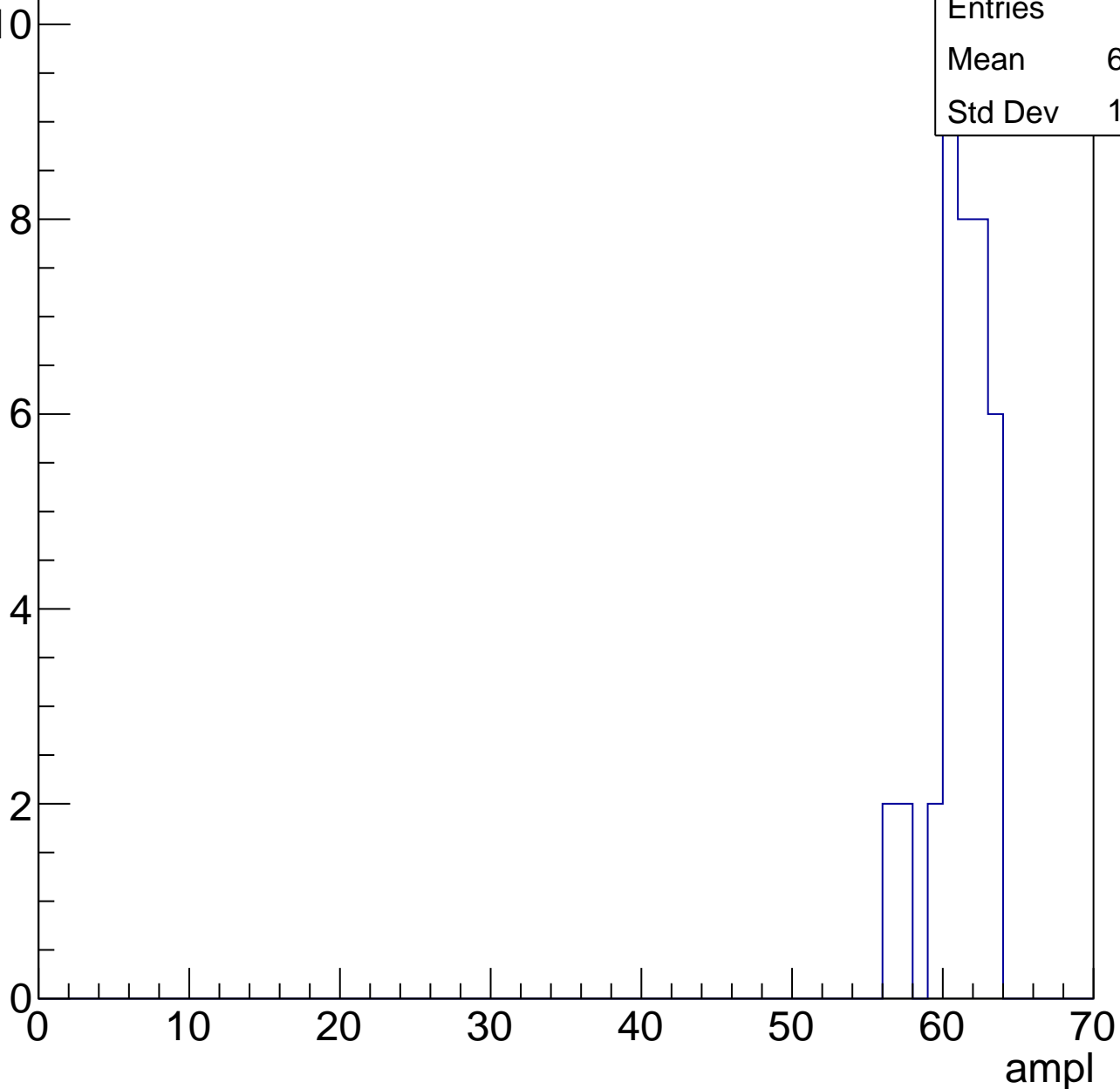


# B1L003S, U11-ch41, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	38
Mean	60.68
Std Dev	1.837



# B1L003S, U11-ch41, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch41, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	3
Mean	21
Std Dev	29.7

# B1L003S, U11-ch42, adc0

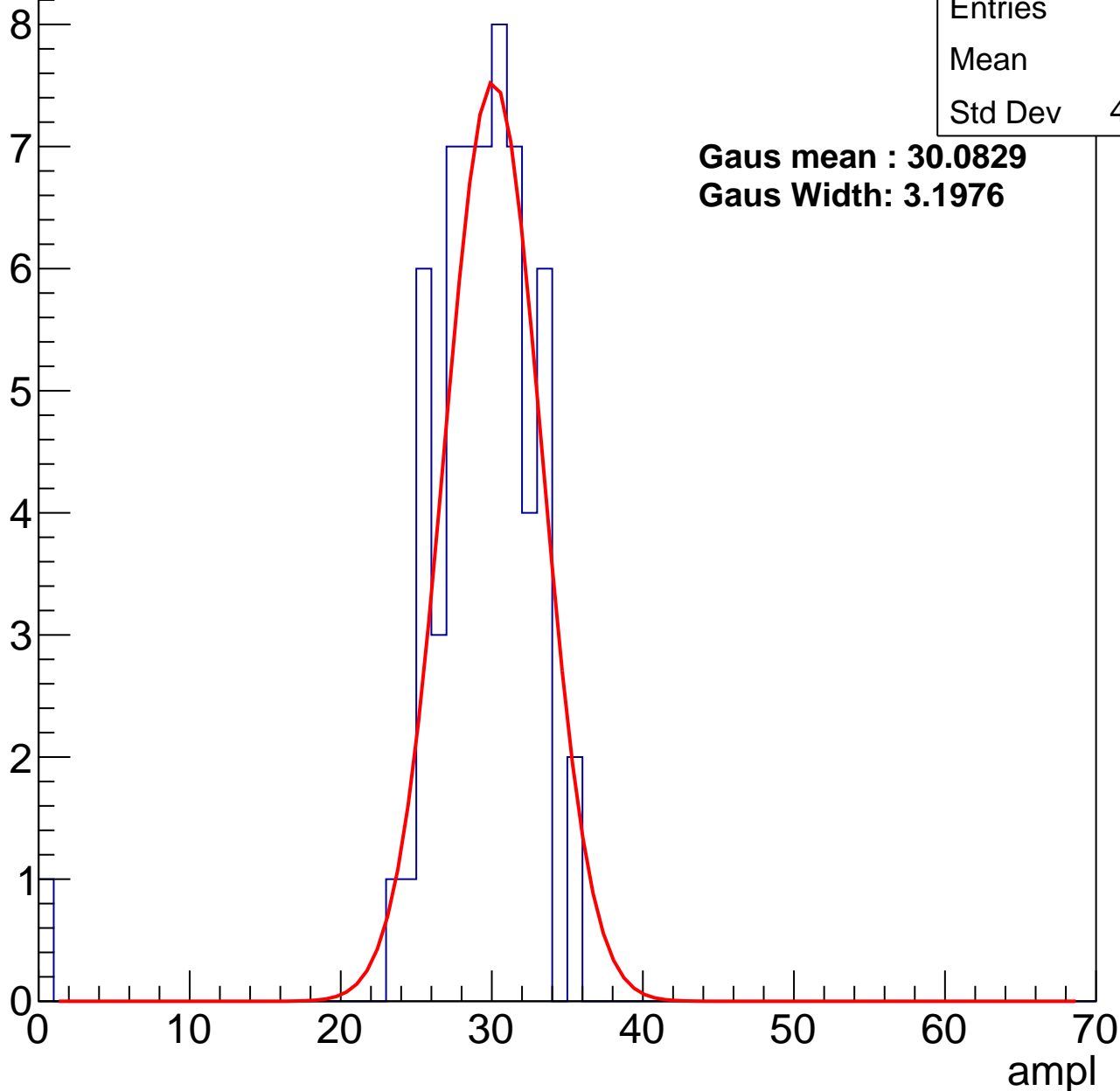
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	28.6
Std Dev	4.638

**Gaus mean : 30.0829**

**Gaus Width: 3.1976**



# B1L003S, U11-ch42, adc1

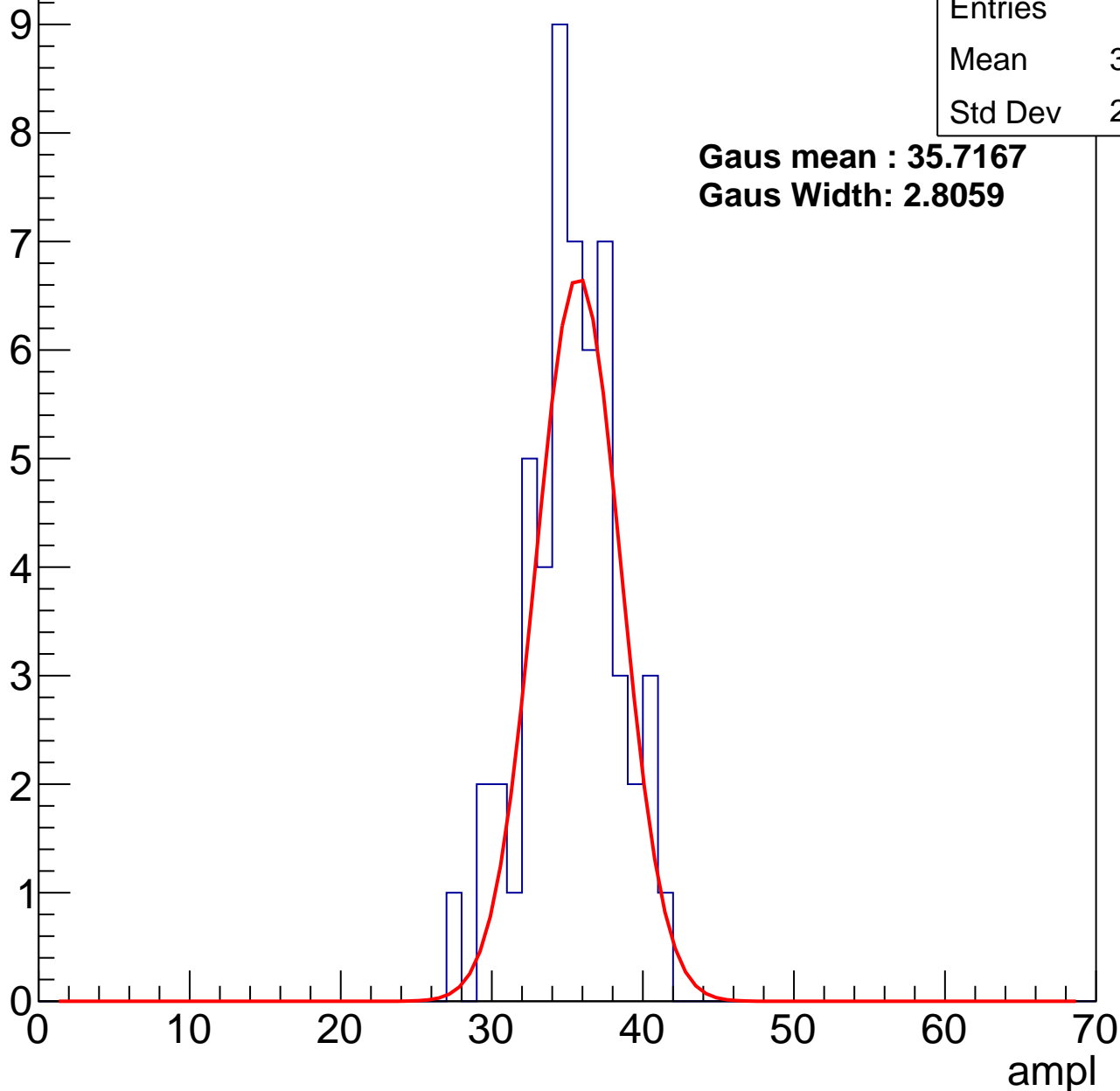
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	34.85
Std Dev	2.993

**Gaus mean : 35.7167**

**Gaus Width: 2.8059**



# B1L003S, U11-ch42, adc2

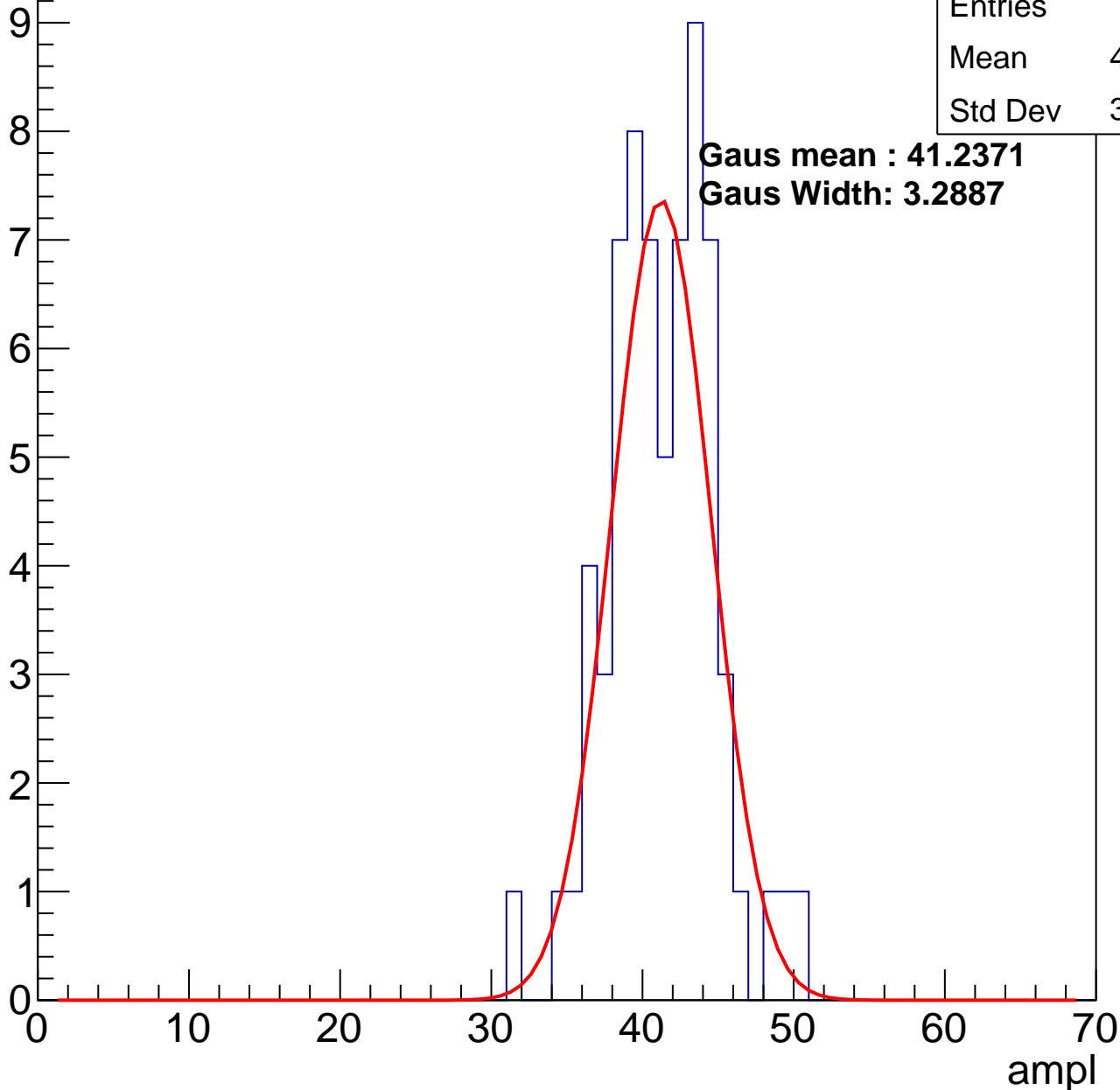
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	40.82
Std Dev	3.468

**Gaus mean : 41.2371**

**Gaus Width: 3.2887**



# B1L003S, U11-ch42, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

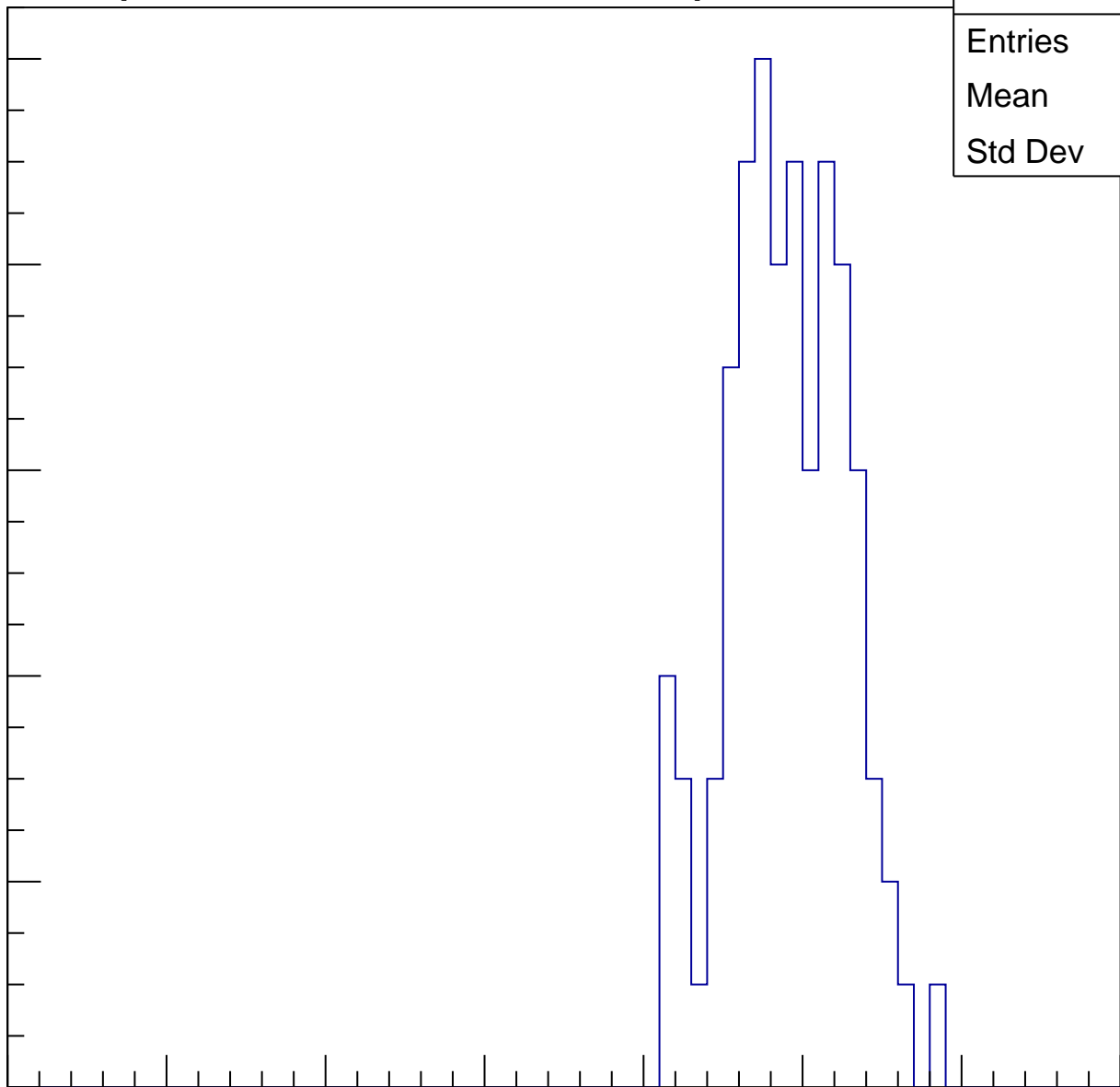
Entries	90
Mean	48.53
Std Dev	3.685

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

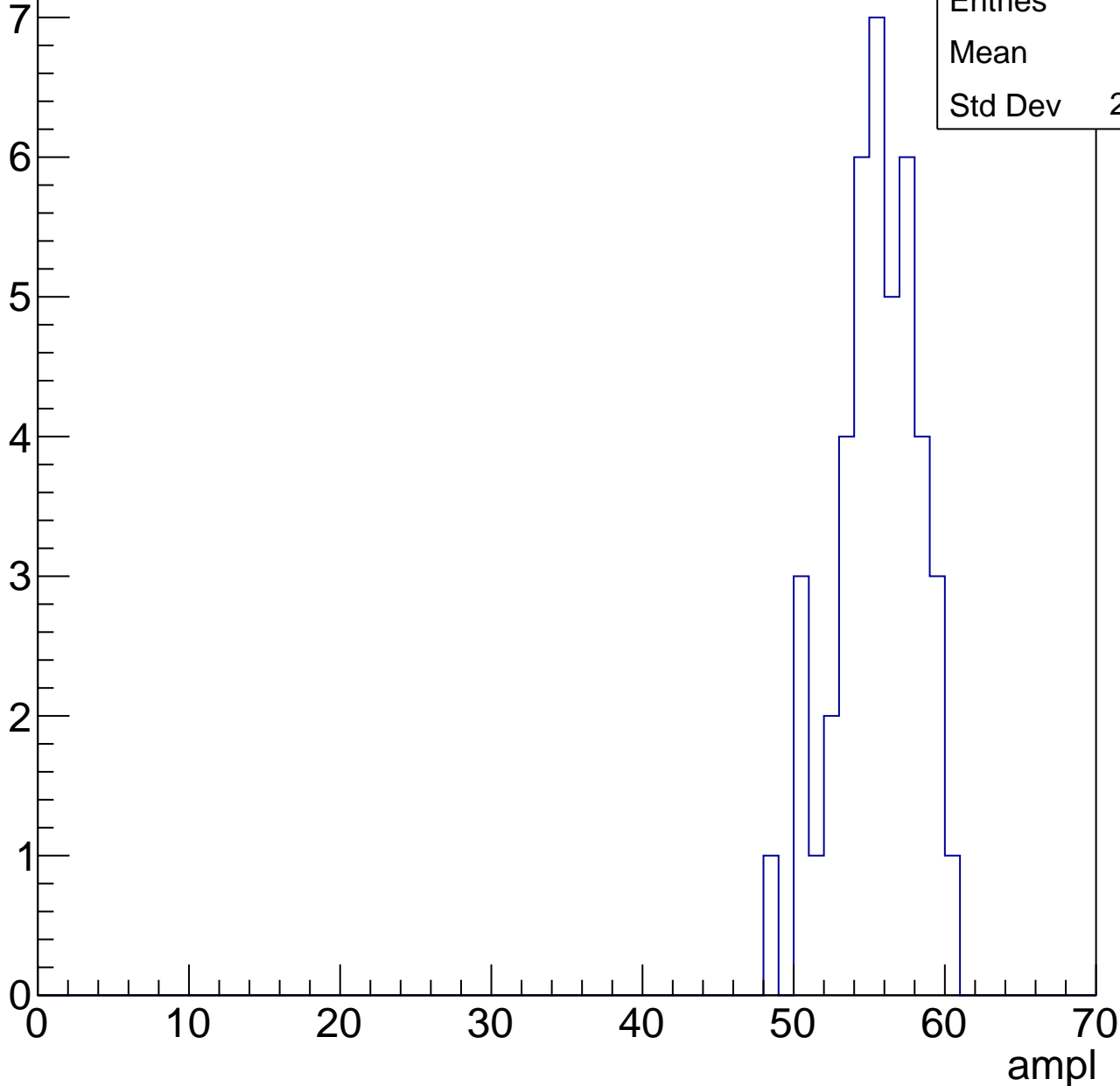


# B1L003S, U11-ch42, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	43
Mean	55
Std Dev	2.719



# B1L003S, U11-ch42, adc5

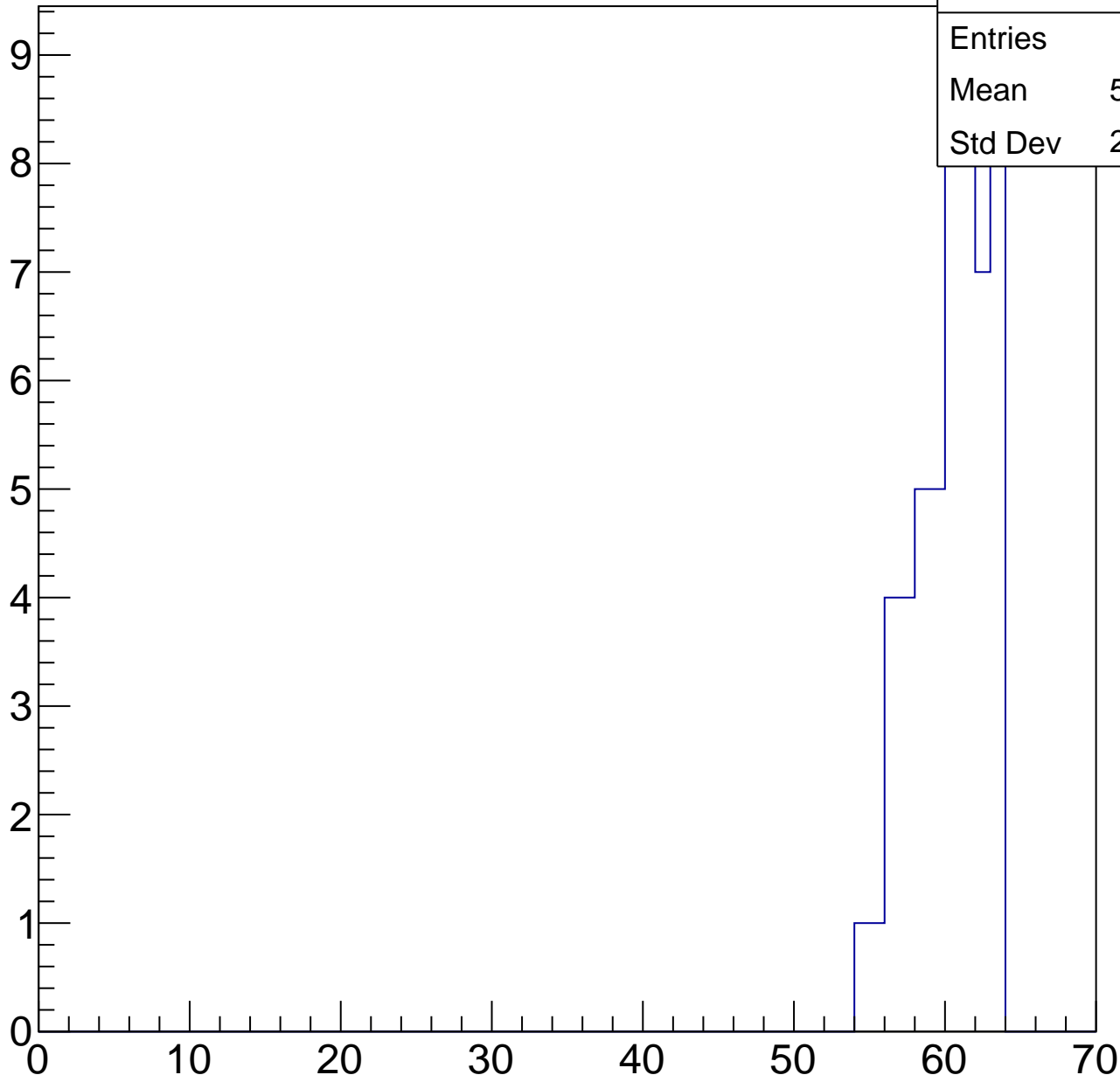
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	52
Mean	59.87
Std Dev	2.378

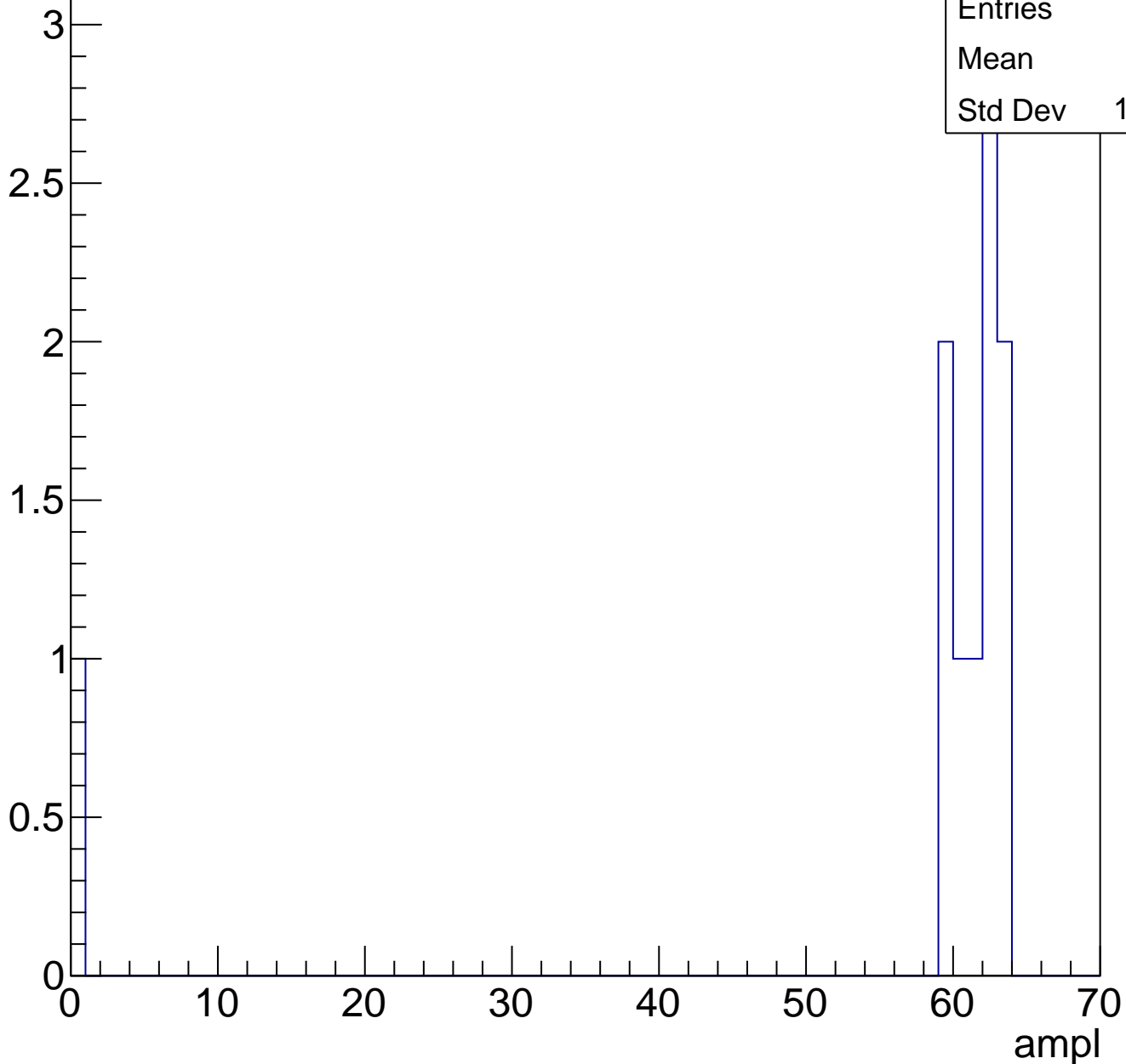
ampl



# B1L003S, U11-ch42, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch42, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U11-ch43, adc0

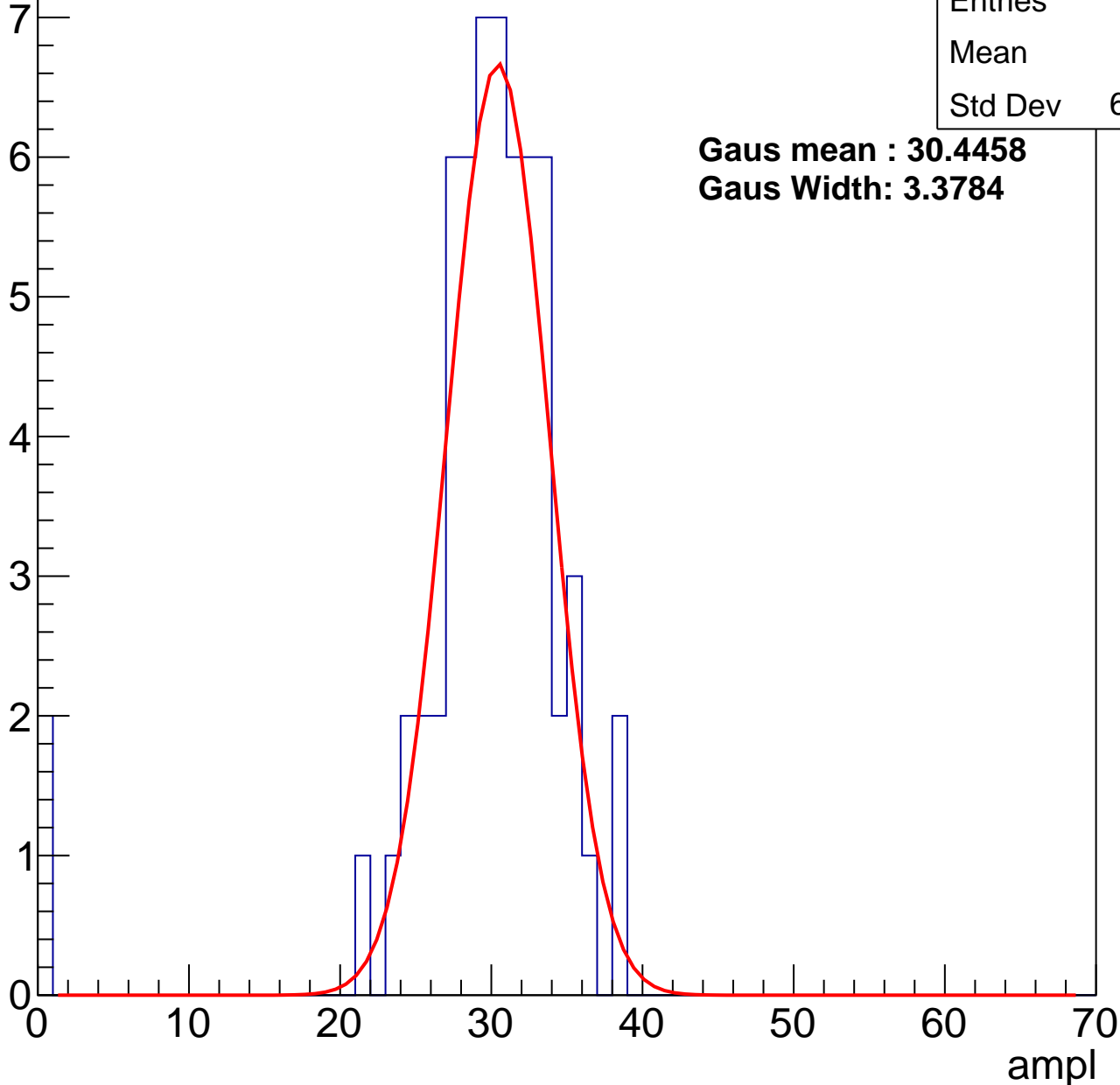
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	29
Std Dev	6.302

**Gaus mean : 30.4458**

**Gaus Width: 3.3784**



# B1L003S, U11-ch43, adc1

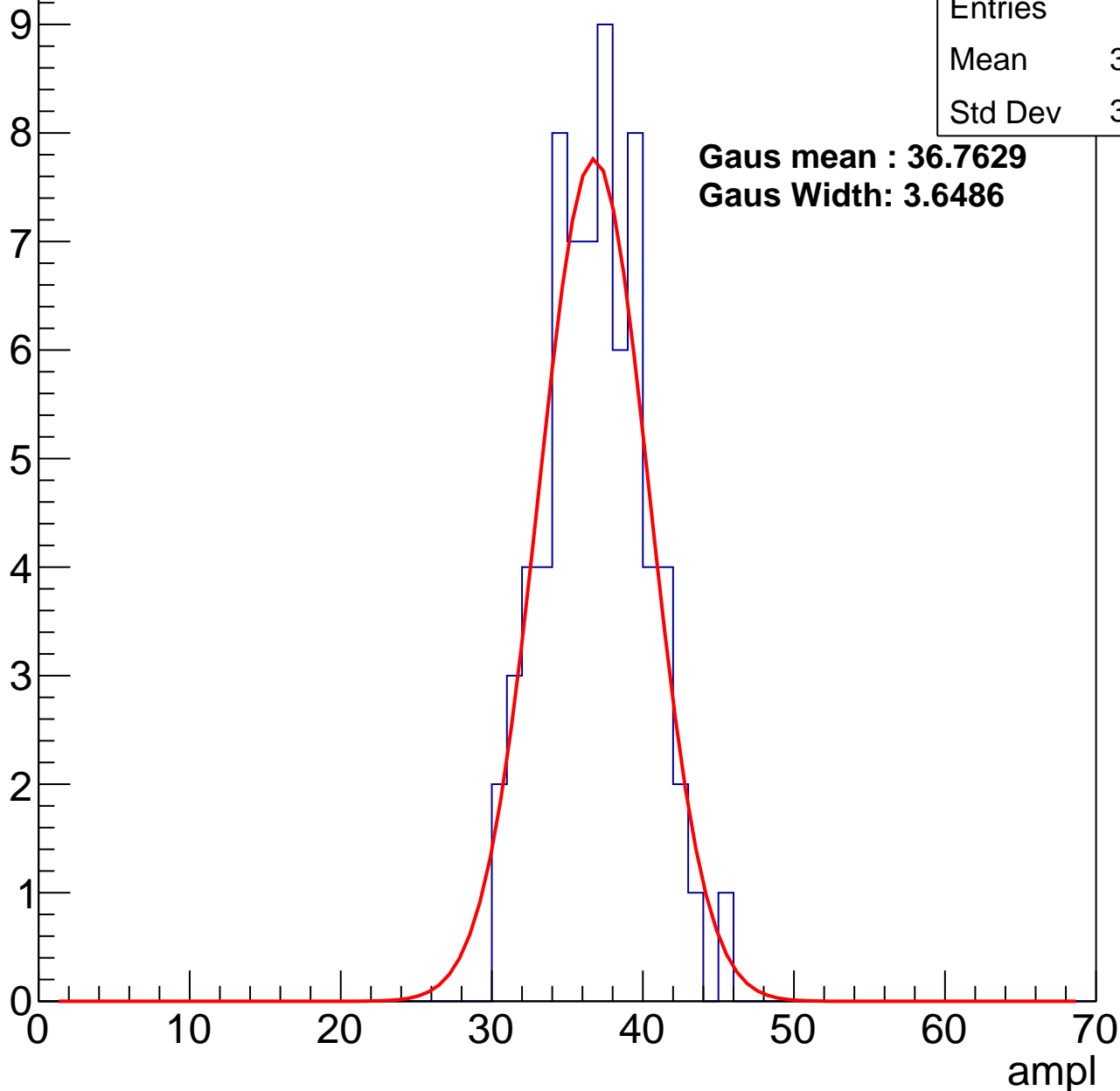
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	36.44
Std Dev	3.259

**Gaus mean : 36.7629**

**Gaus Width: 3.6486**



# B1L003S, U11-ch43, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	79
Mean	43.77
Std Dev	3.245

**Gaus mean : 44.6158**

**Gaus Width: 3.4688**

Entry

10

8

6

4

2

0

0

10

20

30

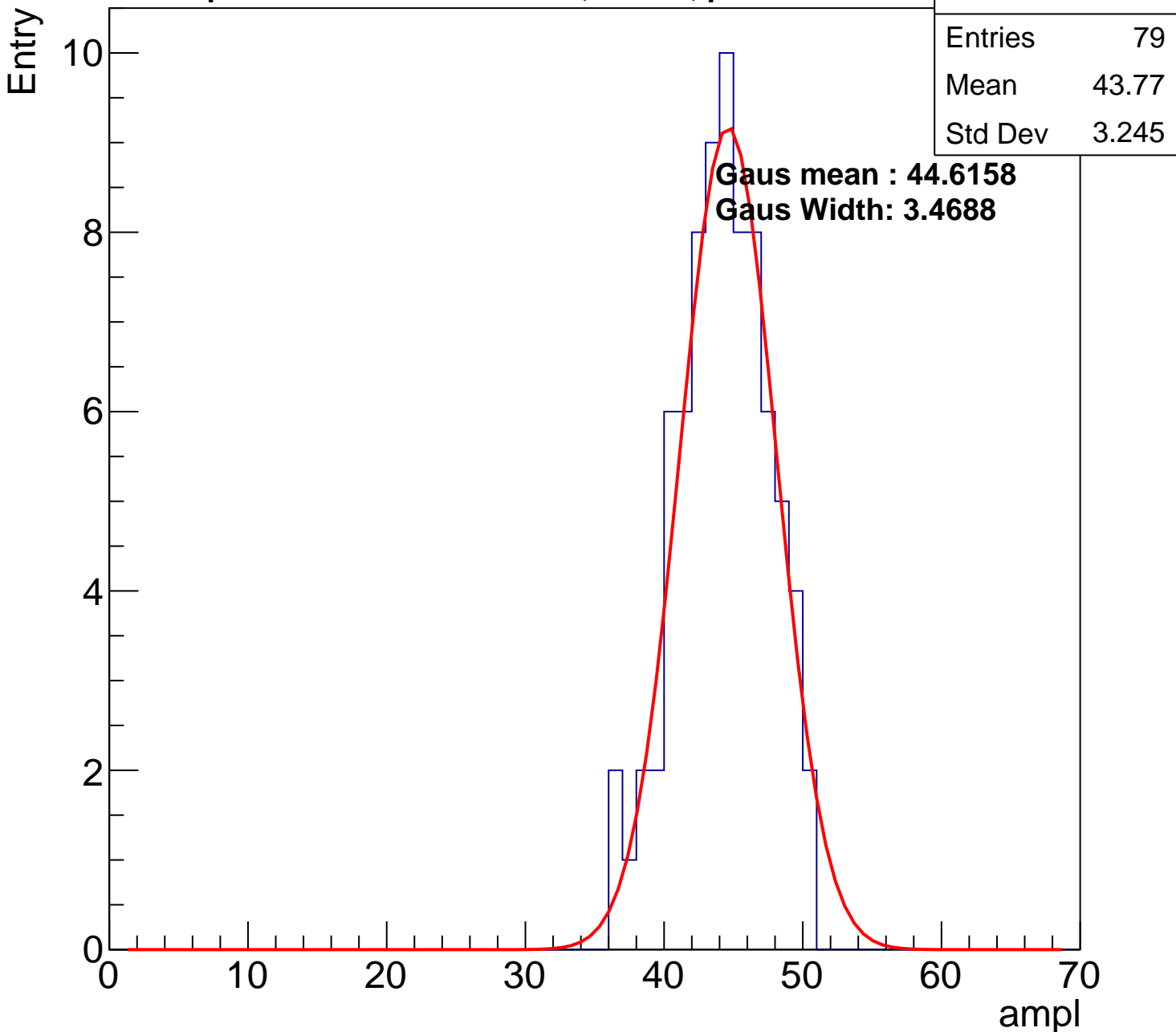
40

50

60

70

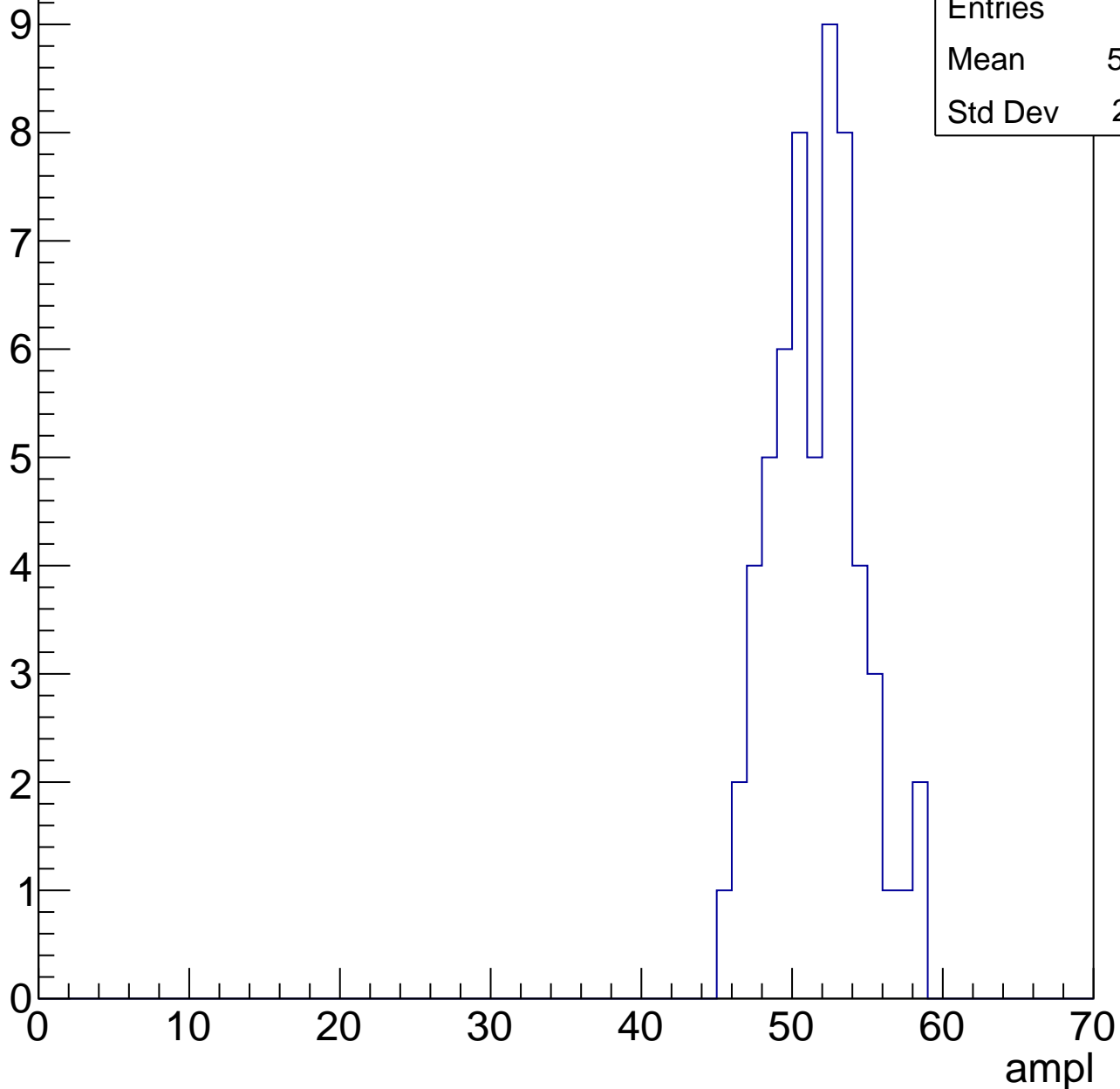
ampl



# B1L003S, U11-ch43, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

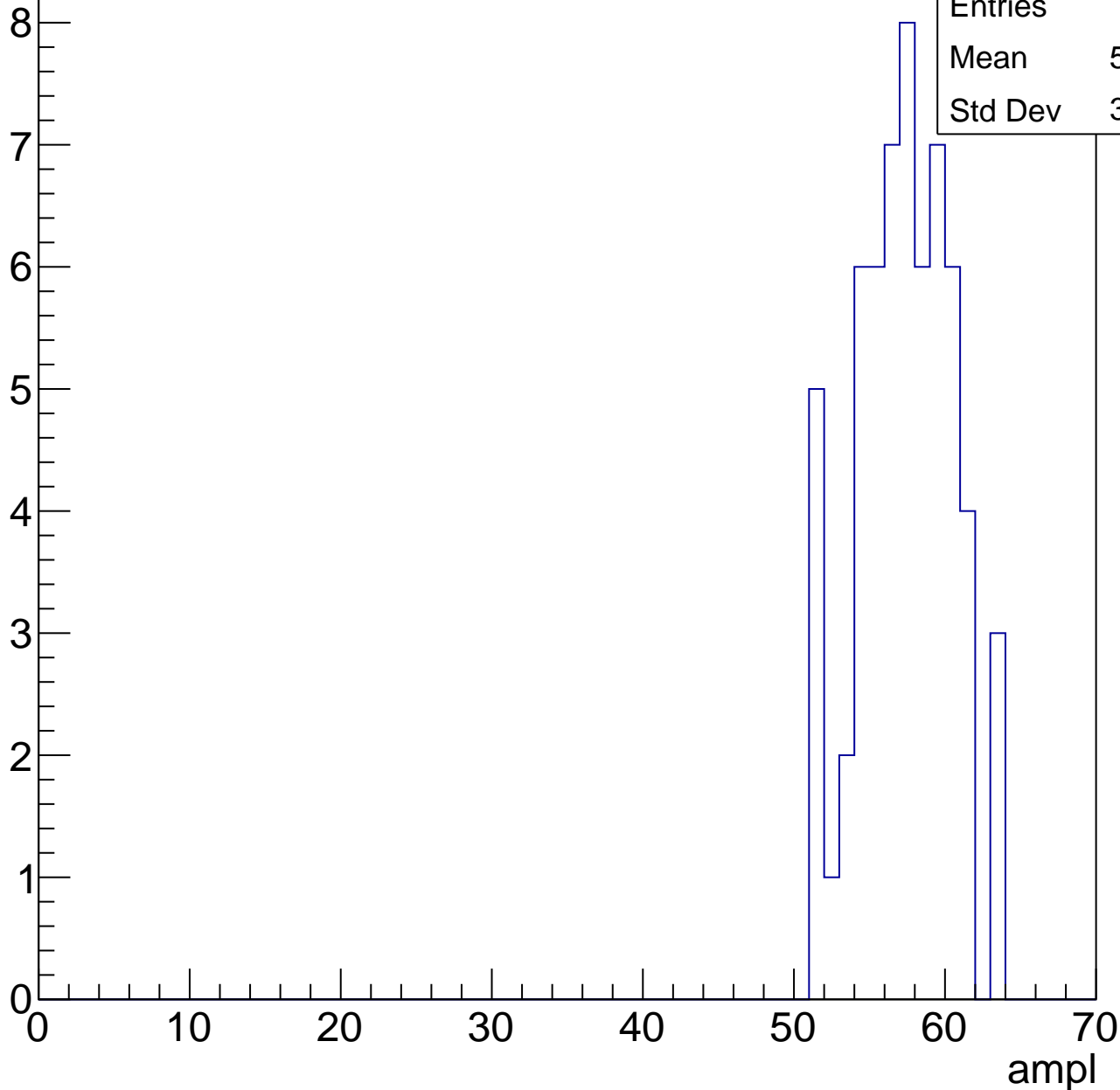


Entries	59
Mean	51.12
Std Dev	2.941

# B1L003S, U11-ch43, adc4

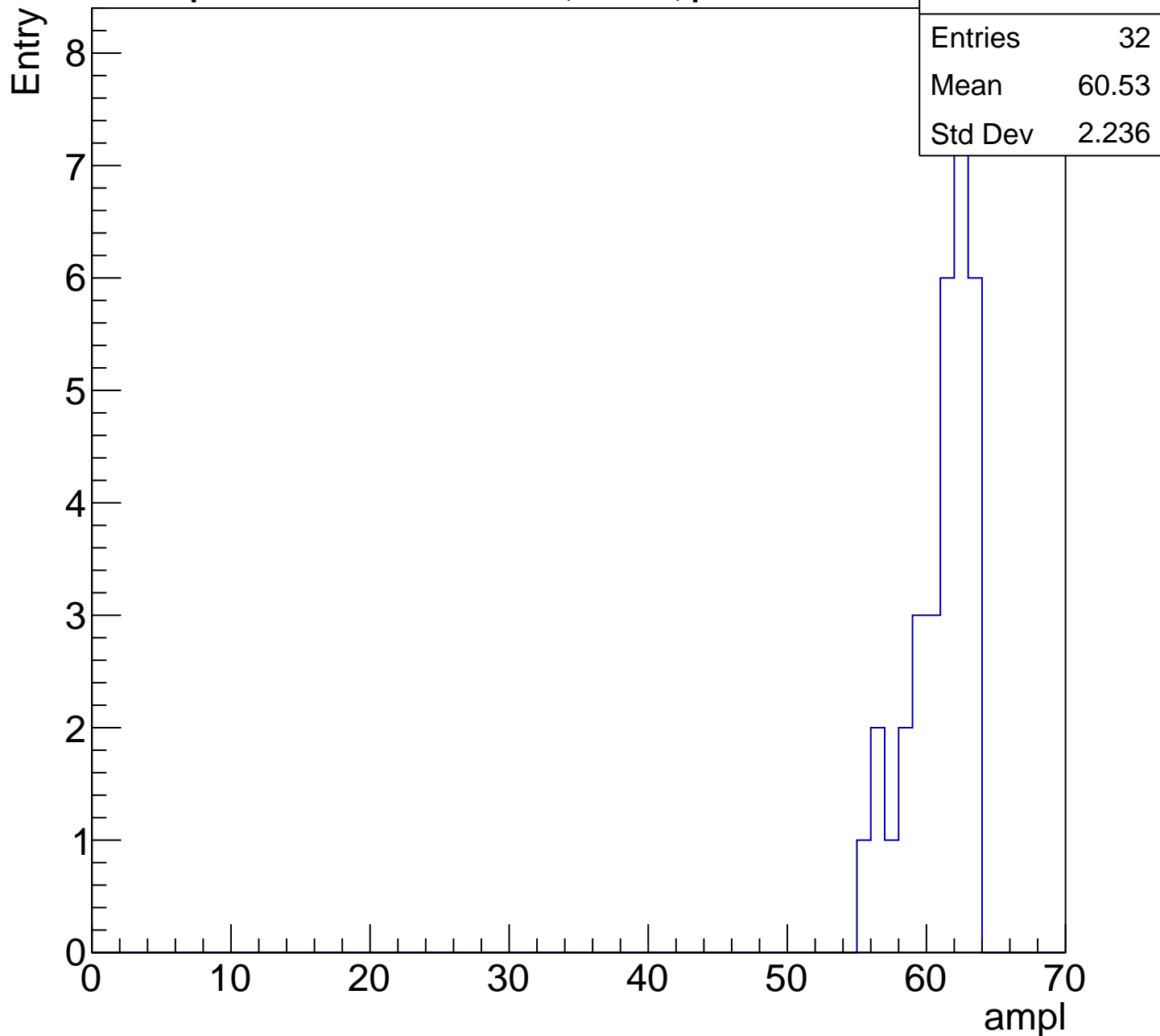
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U11-ch43, adc5

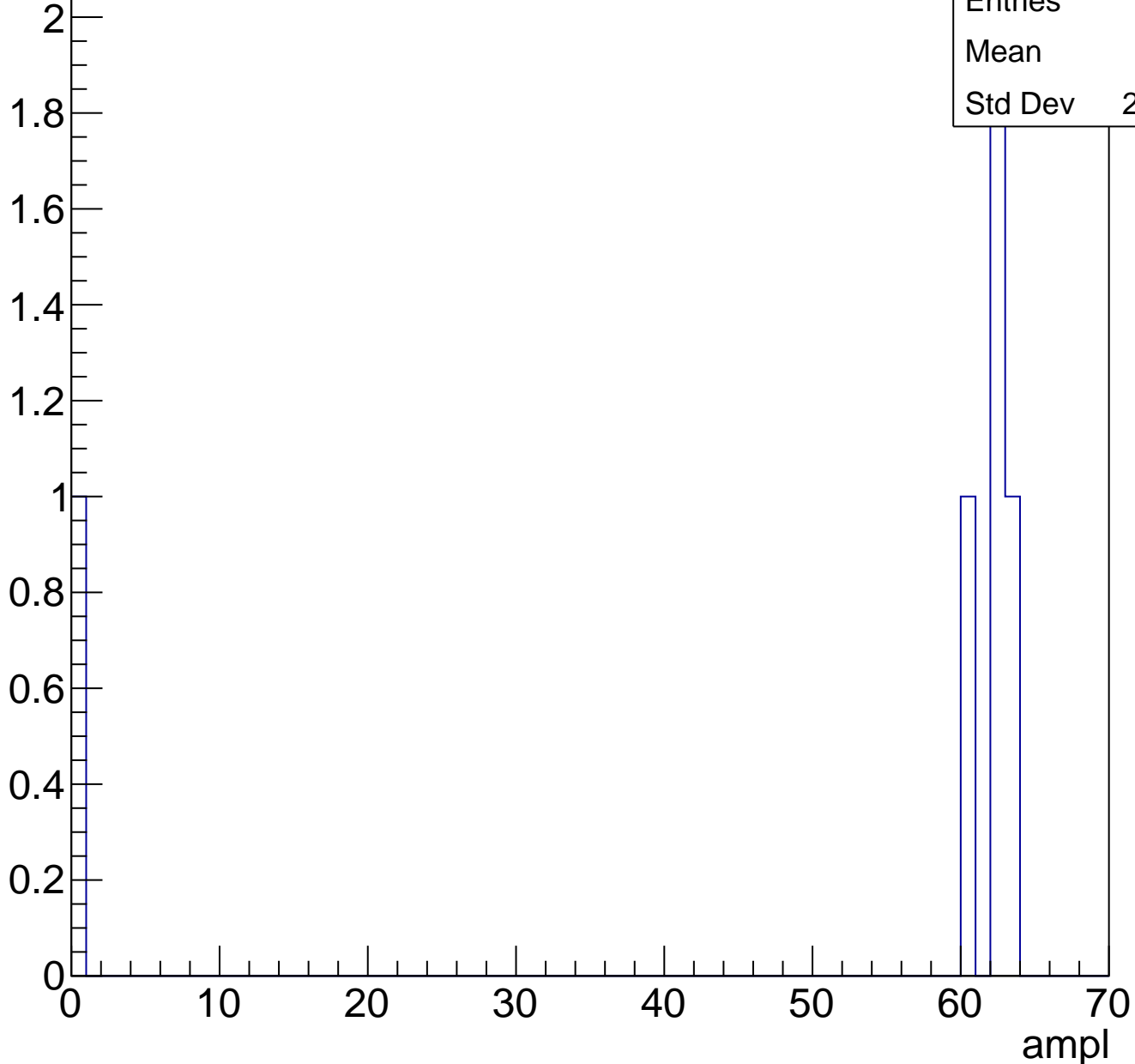
calib\_packv5\_042523\_0143.root, FC#13, port D2



# B1L003S, U11-ch43, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	5
Mean	49.4
Std Dev	24.72



# B1L003S, U11-ch43, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U11-ch44, adc0

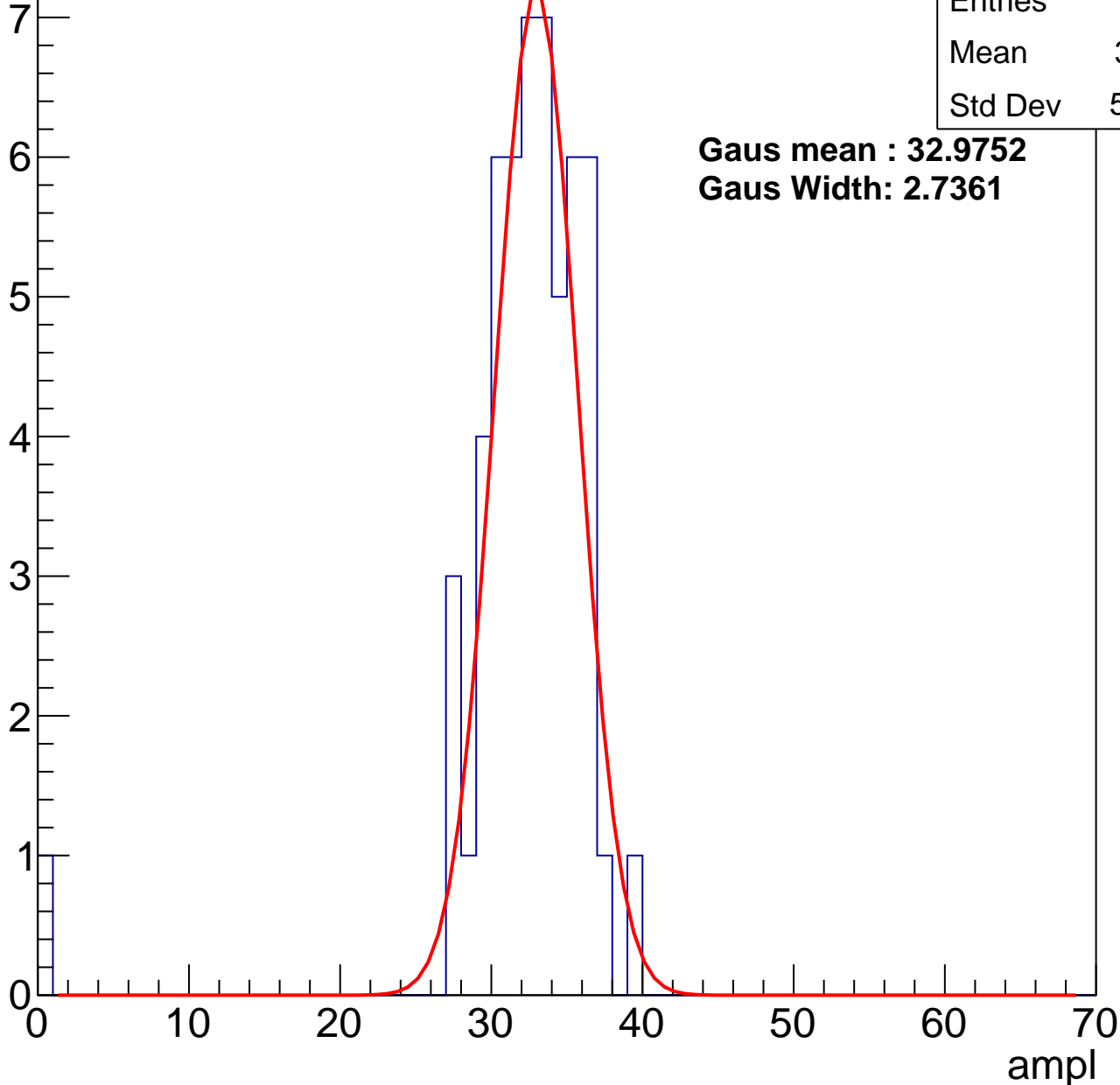
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	54
Mean	31.81
Std Dev	5.146

**Gaus mean : 32.9752**

**Gaus Width: 2.7361**



# B1L003S, U11-ch44, adc1

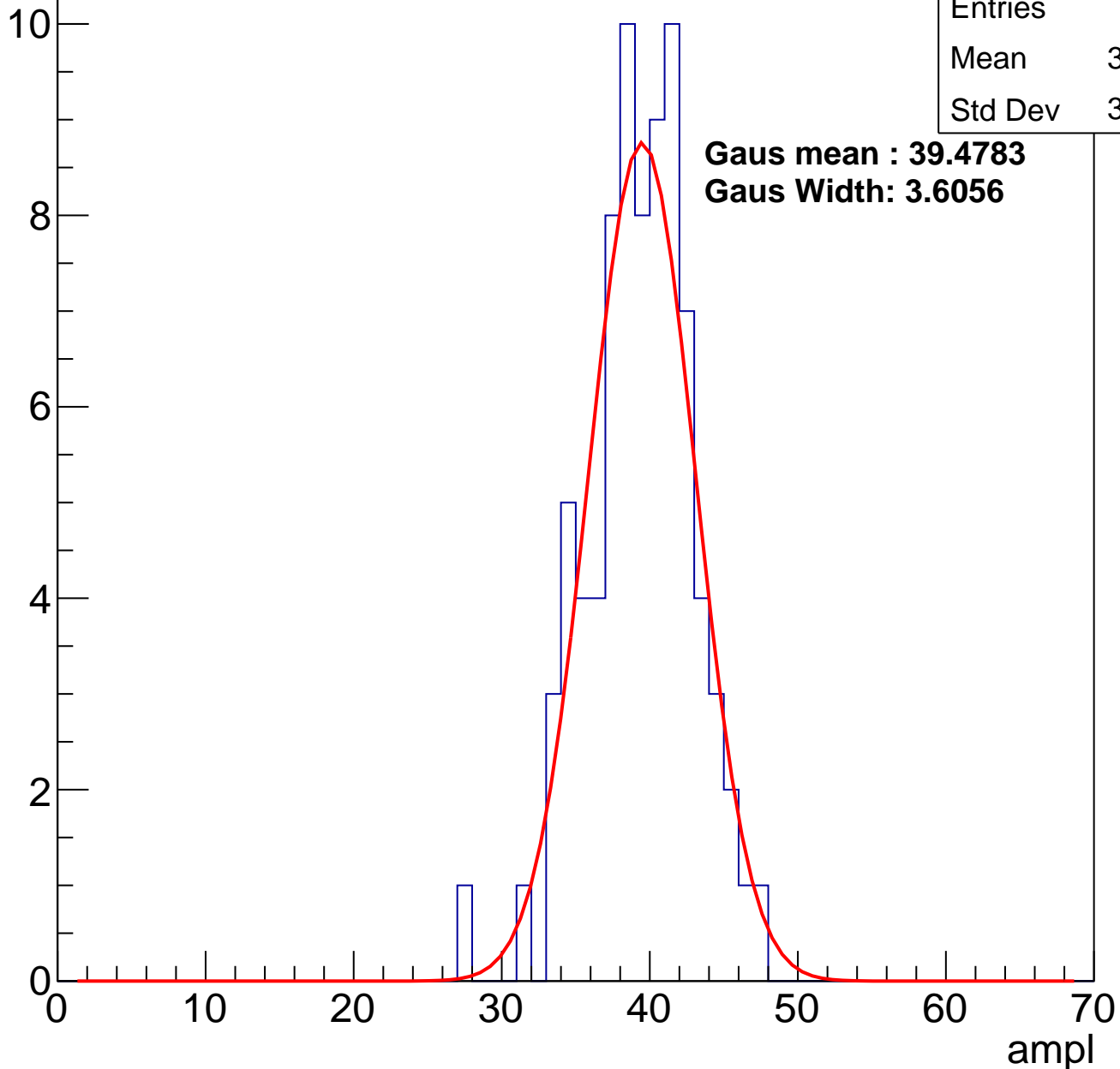
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	81
Mean	38.89
Std Dev	3.545

**Gaus mean : 39.4783**

**Gaus Width: 3.6056**

Entry



# B1L003S, U11-ch44, adc2

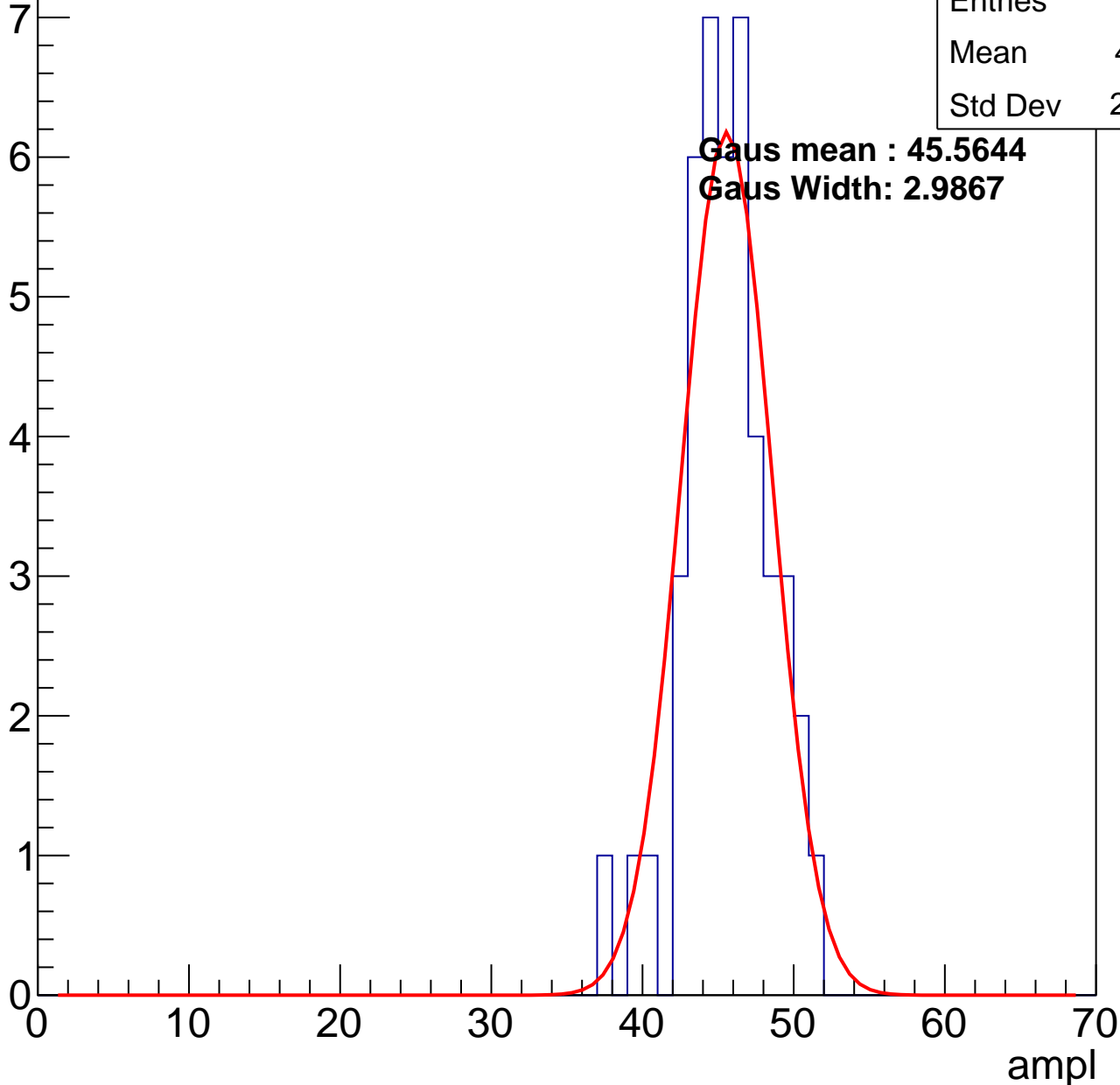
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	45
Mean	45.11
Std Dev	2.854

Gaus mean : 45.5644

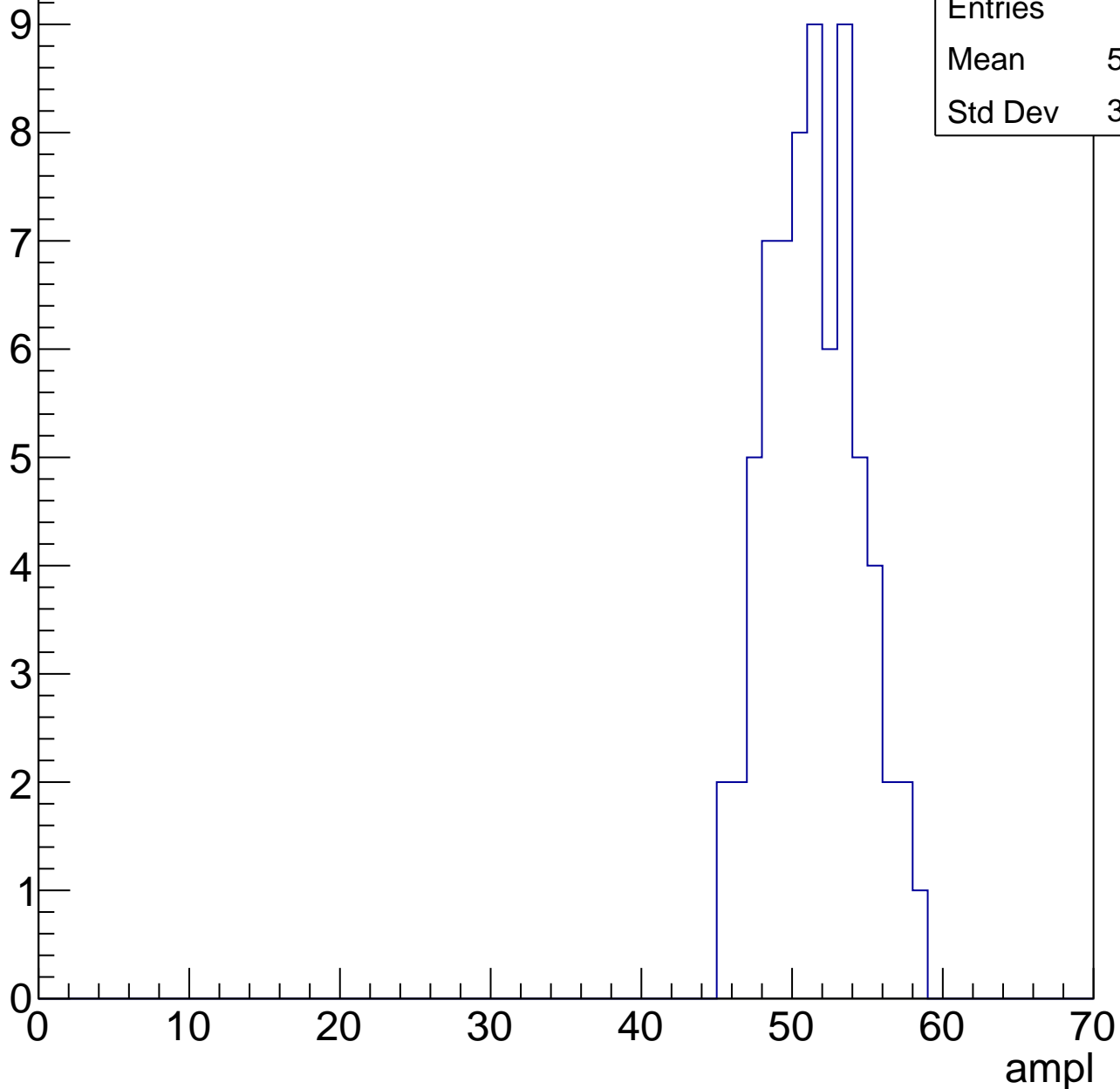
Gaus Width: 2.9867



# B1L003S, U11-ch44, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

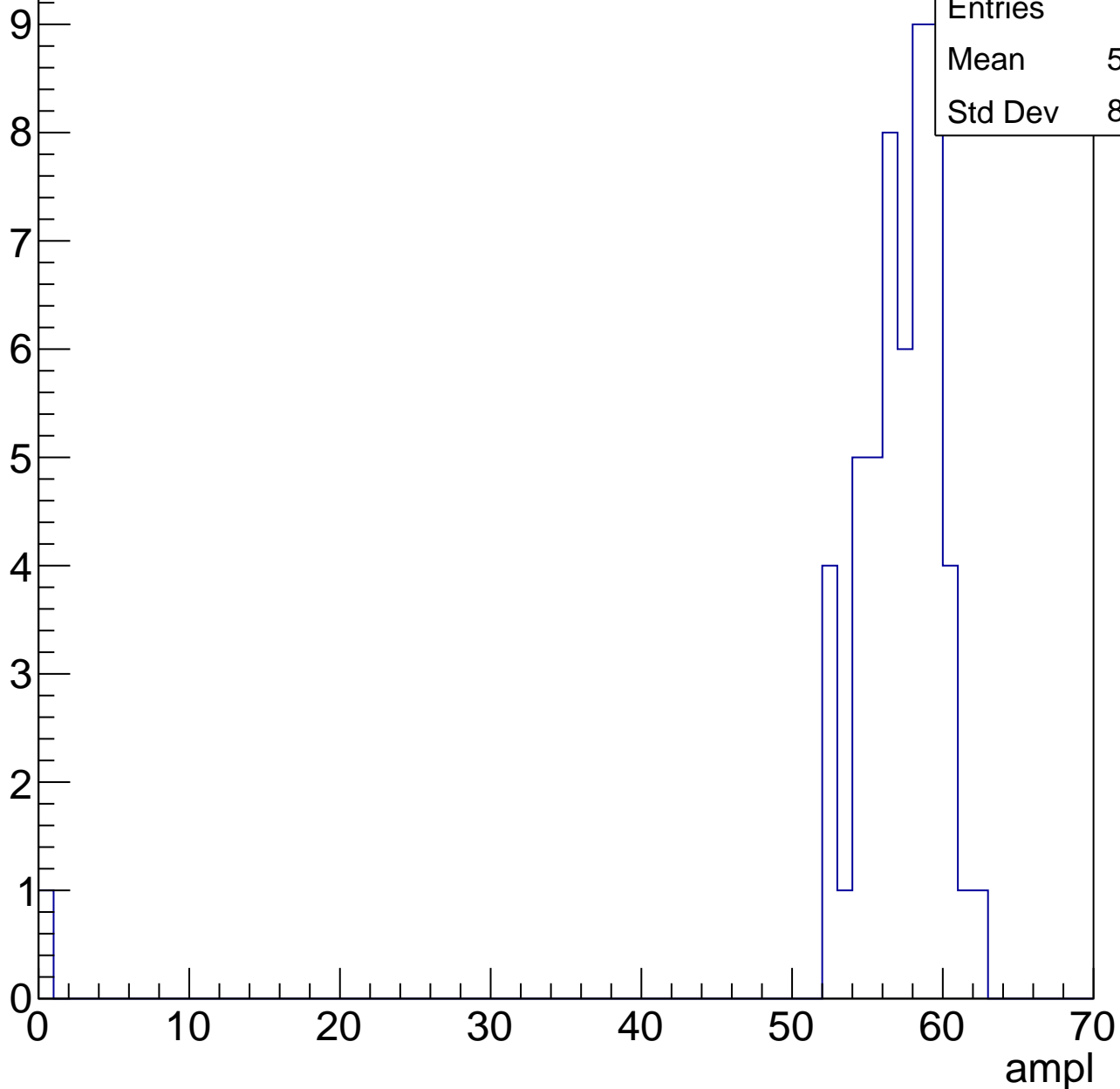
Entry



# B1L003S, U11-ch44, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

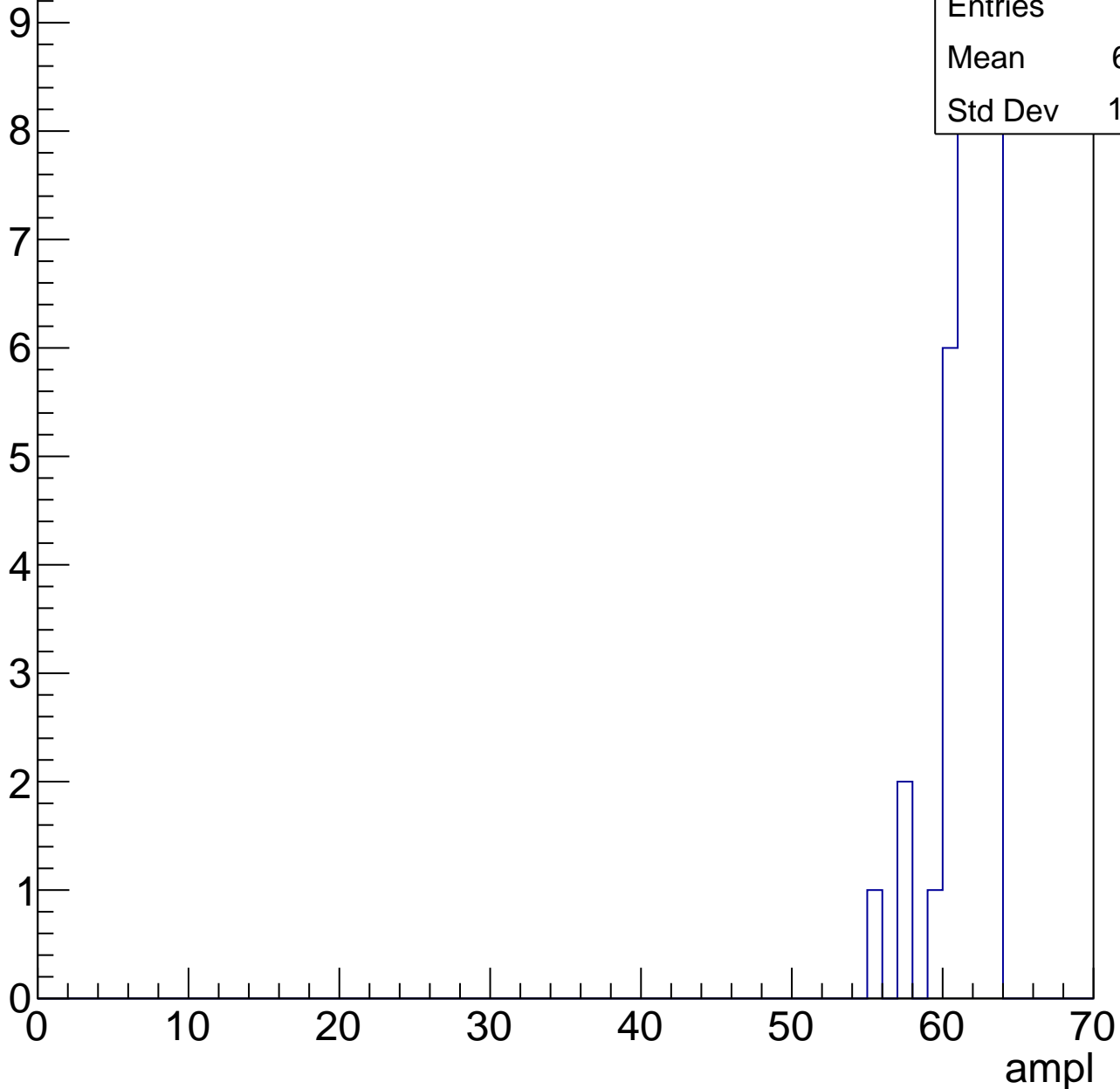


# B1L003S, U11-ch44, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	36
Mean	61.11
Std Dev	1.838



# B1L003S, U11-ch44, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch44, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	26
Std Dev	0

ampl

# B1L003S, U11-ch45, adc0

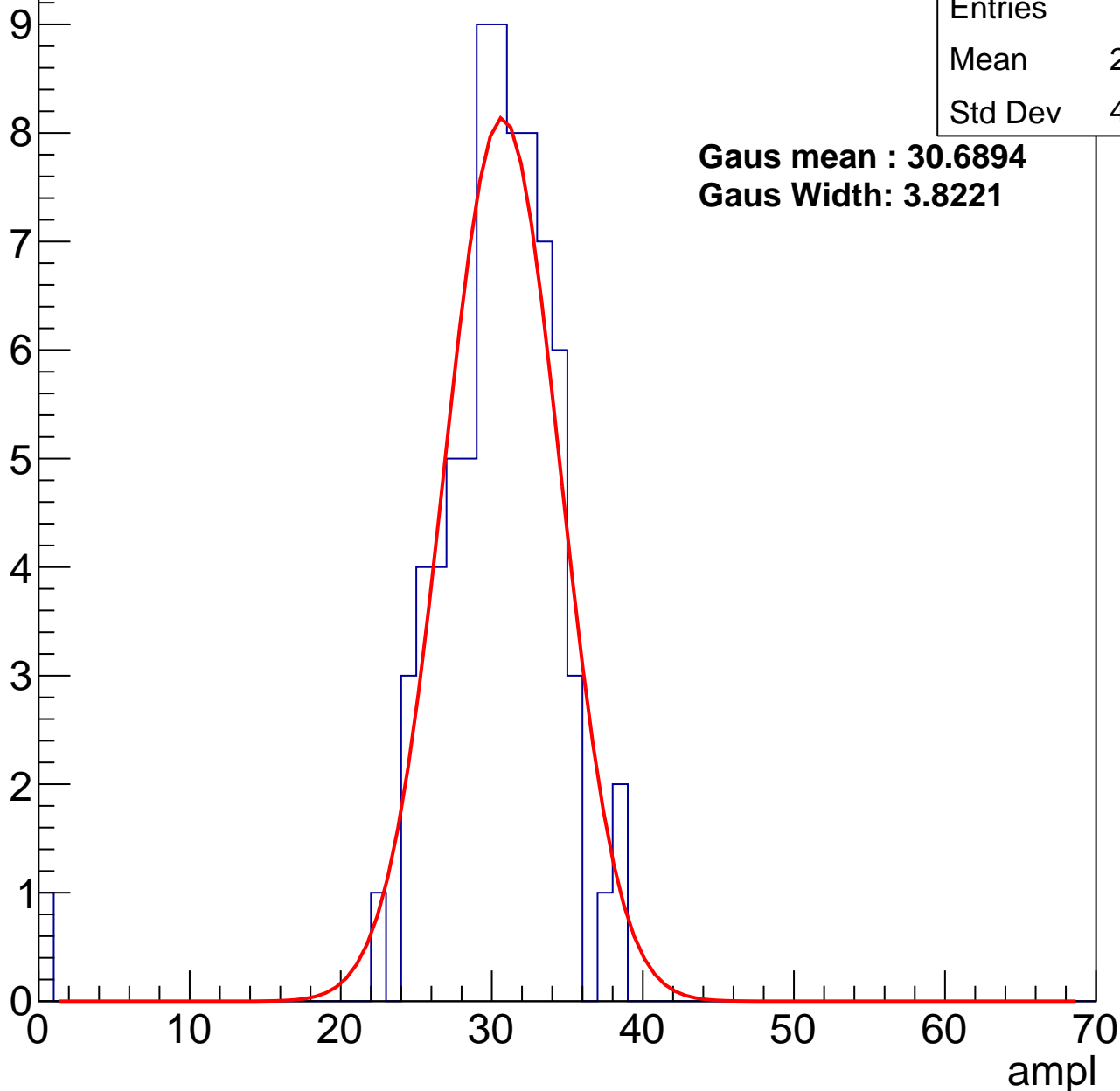
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	76
Mean	29.75
Std Dev	4.807

**Gaus mean : 30.6894**

**Gaus Width: 3.8221**



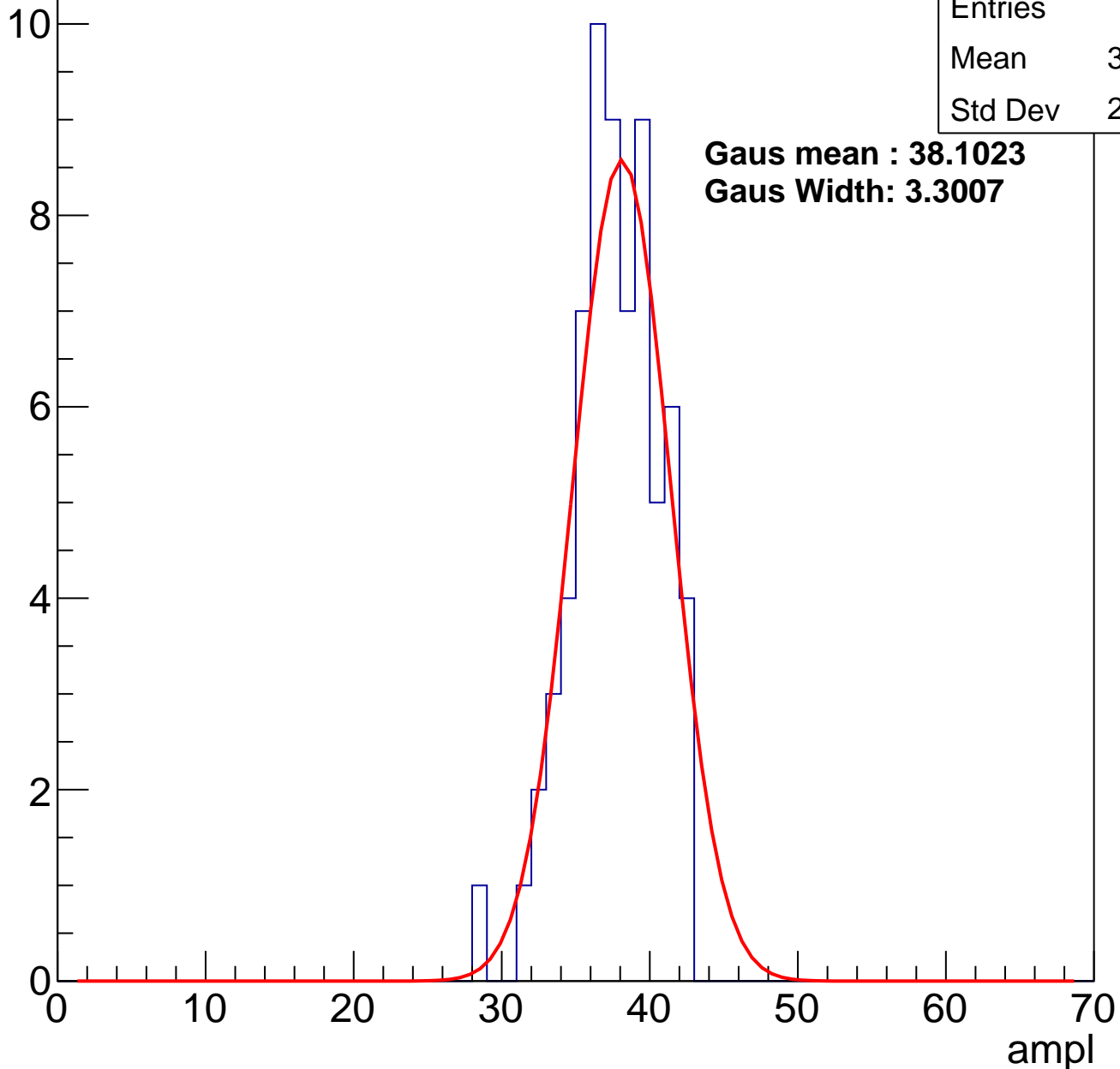
# B1L003S, U11-ch45, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	68
Mean	37.16
Std Dev	2.898

**Gaus mean : 38.1023**  
**Gaus Width: 3.3007**

Entry



# B1L003S, U11-ch45, adc2

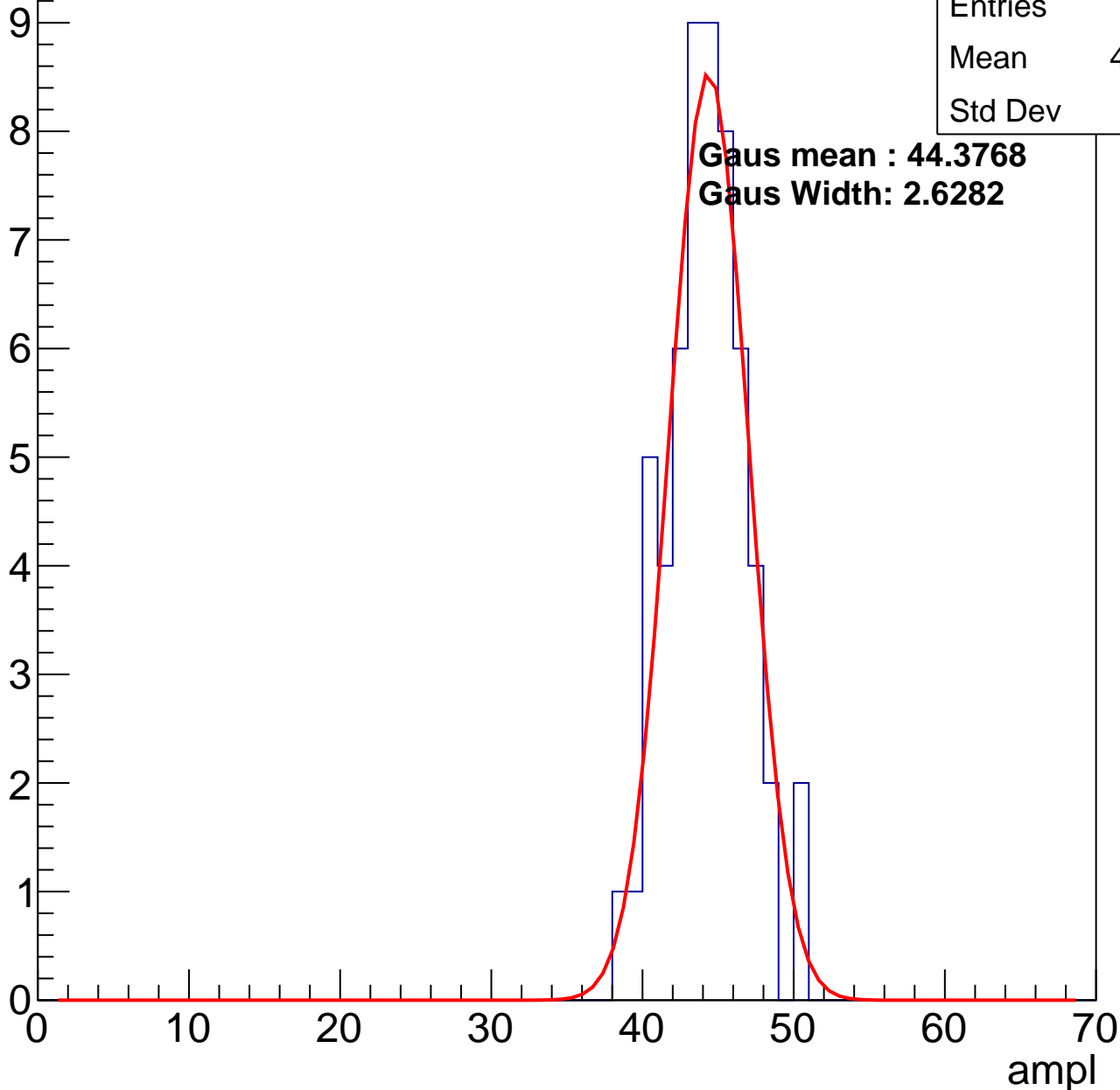
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	43.79
Std Dev	2.58

**Gaus mean : 44.3768**

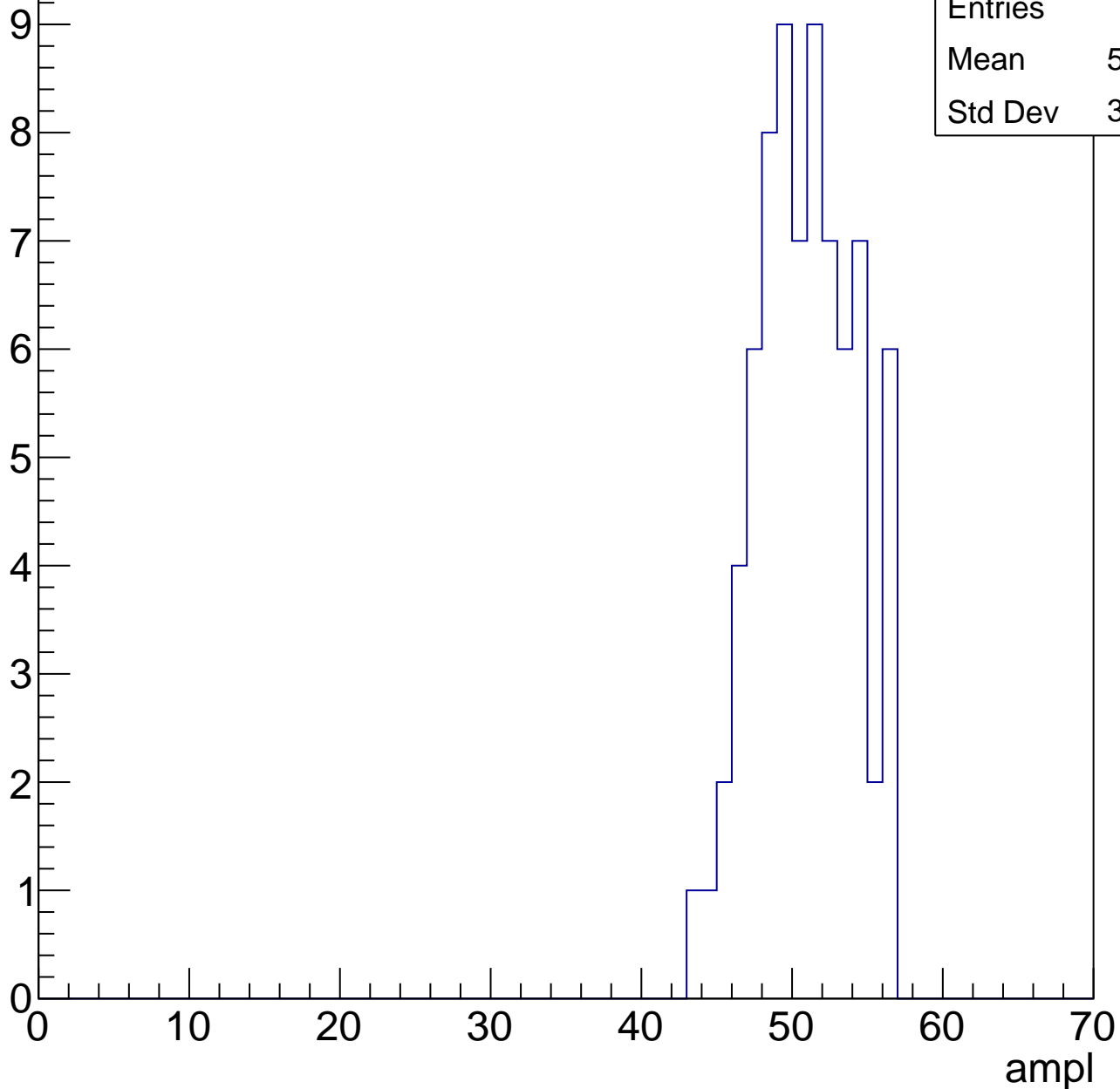
**Gaus Width: 2.6282**



# B1L003S, U11-ch45, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

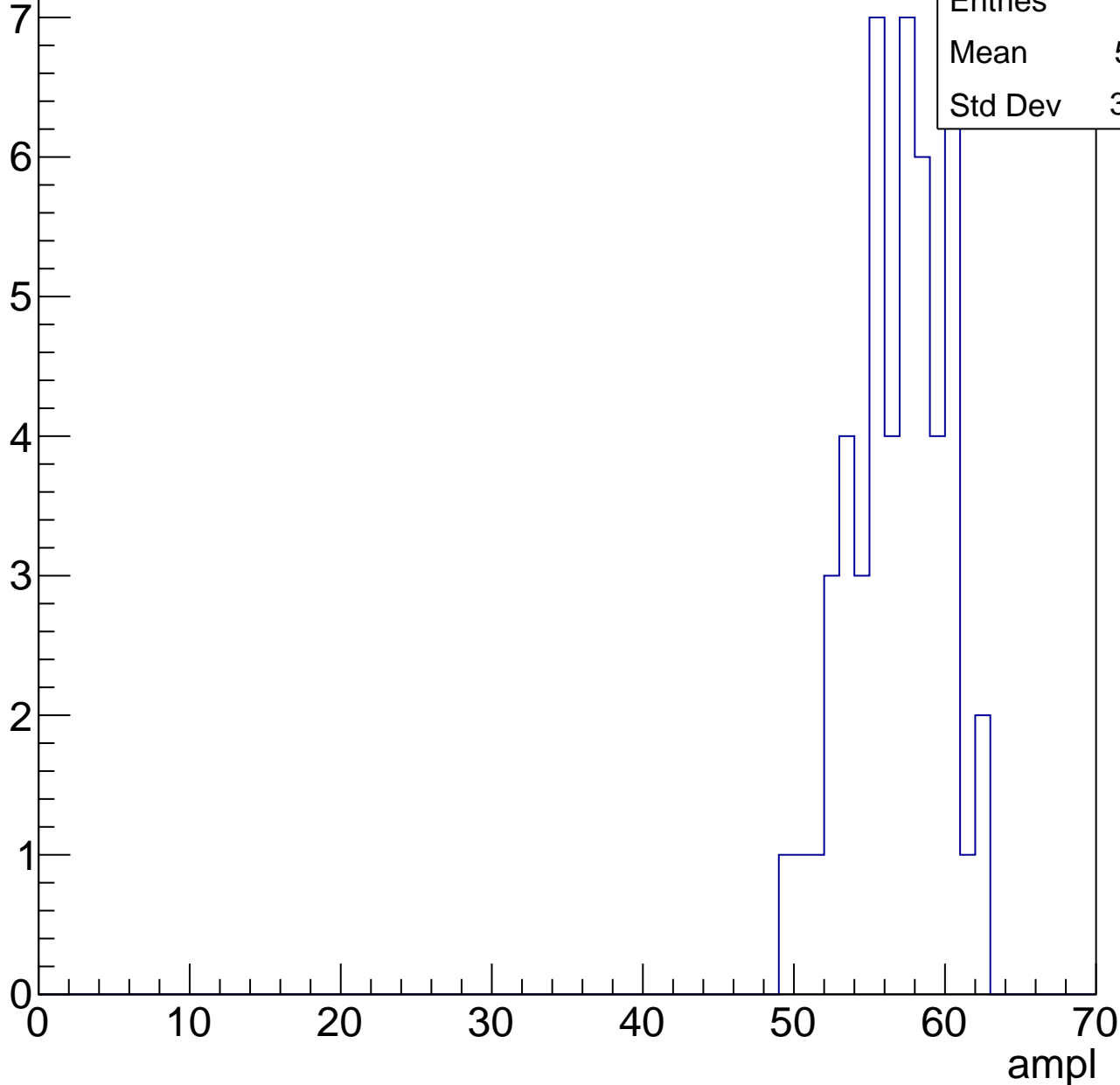


Entries	75
Mean	50.44
Std Dev	3.159

# B1L003S, U11-ch45, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

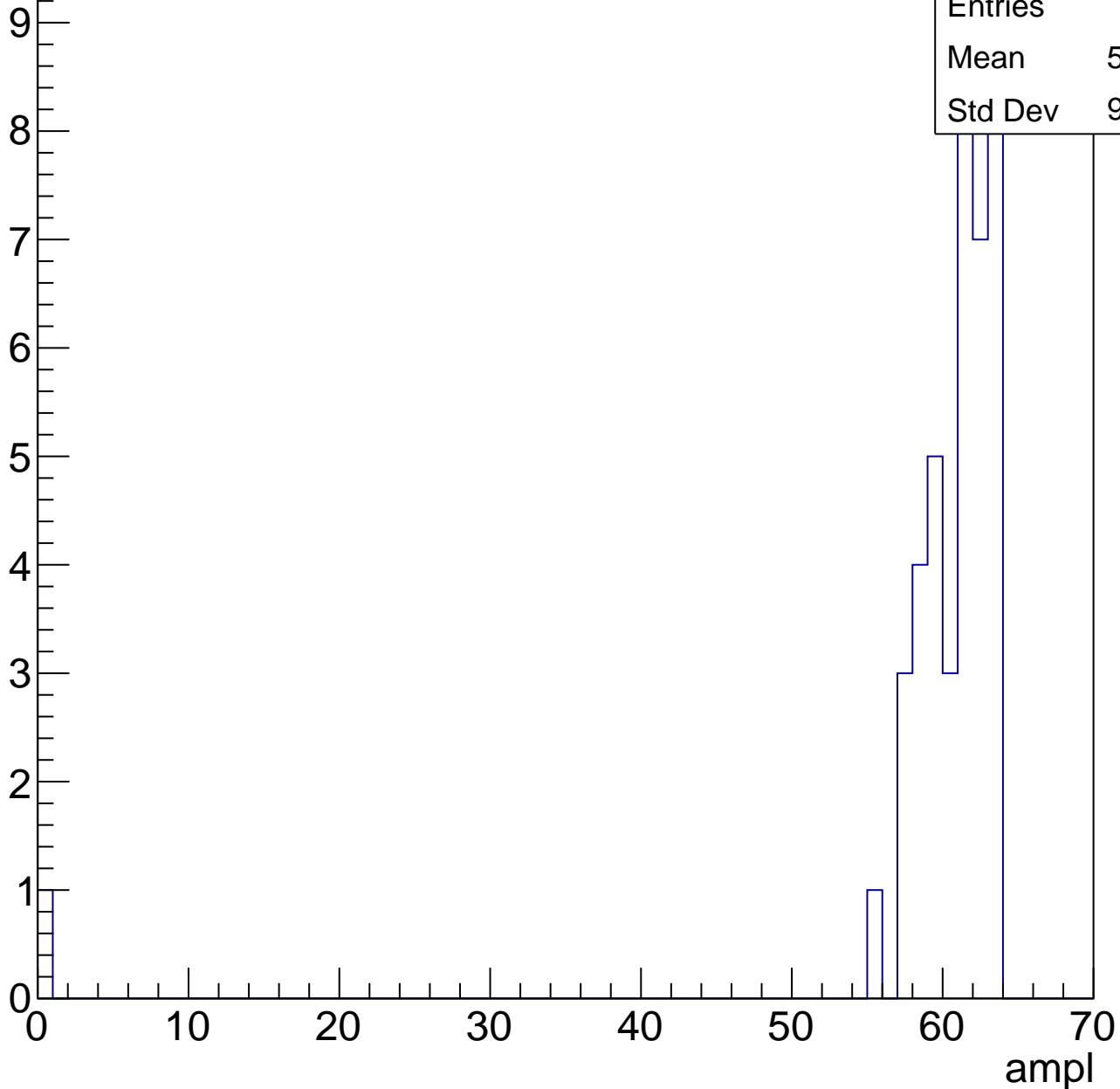


# B1L003S, U11-ch45, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

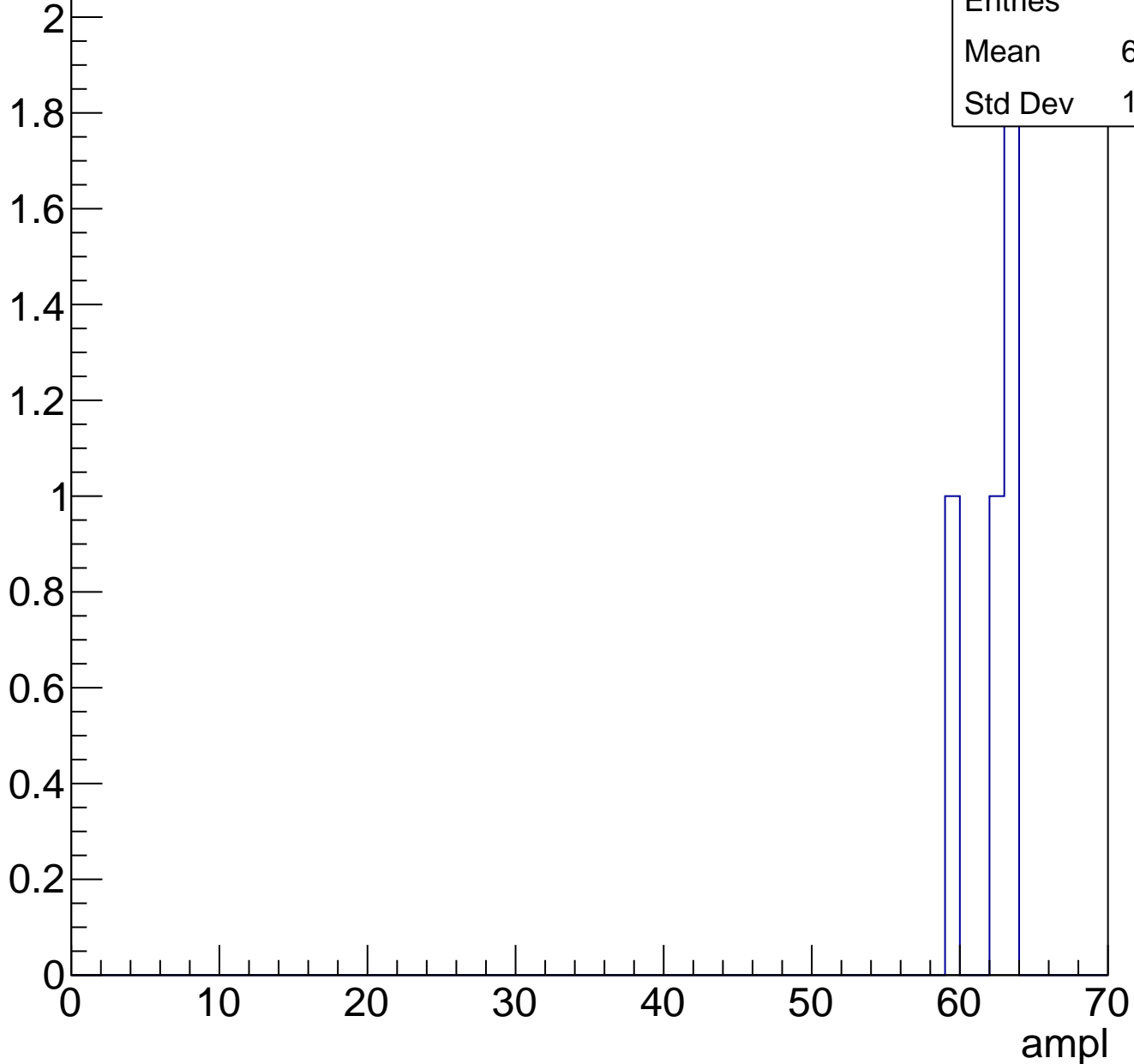
Entries	41
Mean	59.02
Std Dev	9.555



# B1L003S, U11-ch45, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch45, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U11-ch46, adc0

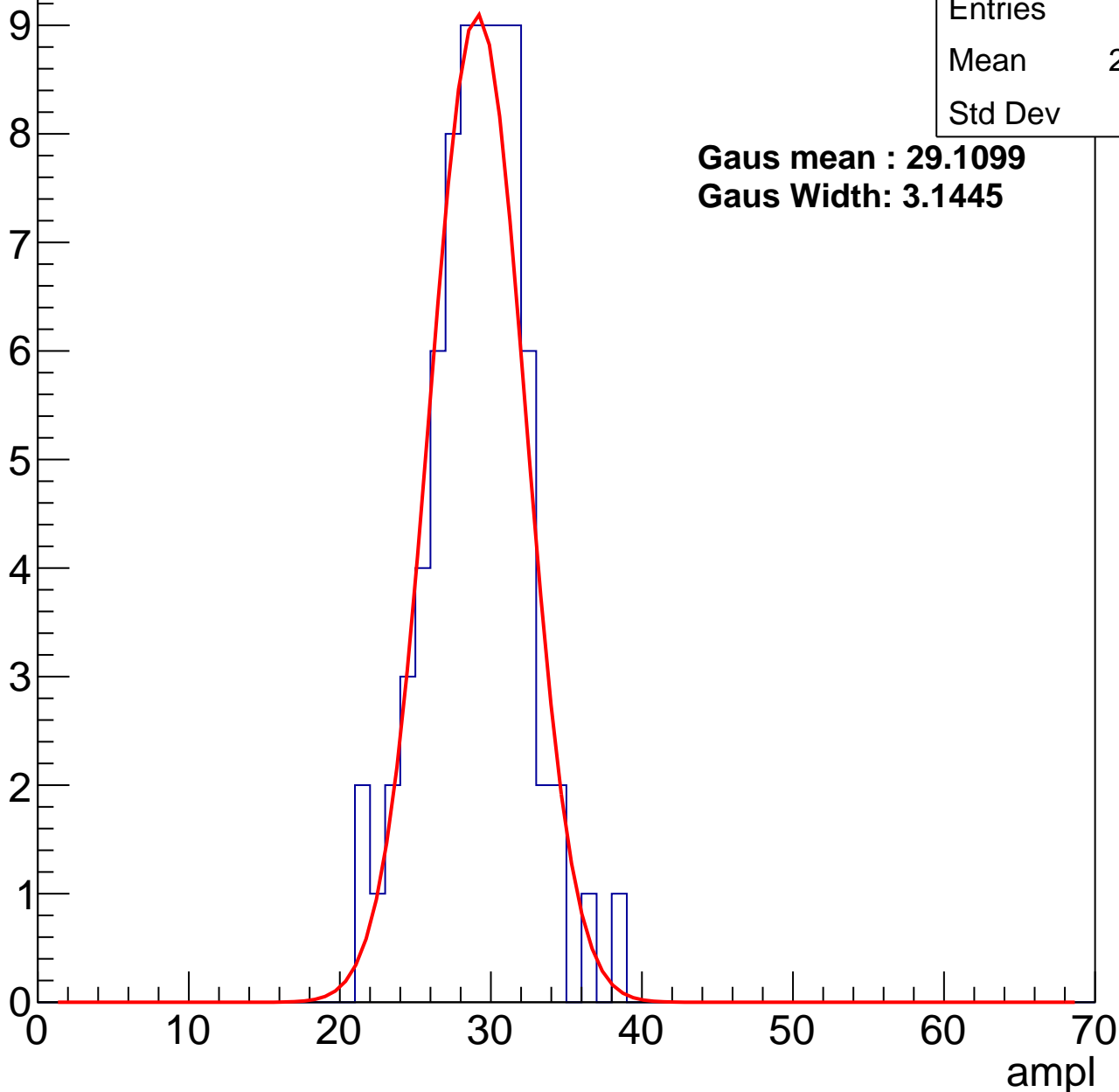
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	74
Mean	28.59
Std Dev	3.25

**Gaus mean : 29.1099**

**Gaus Width: 3.1445**



# B1L003S, U11-ch46, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	72
Mean	36.25
Std Dev	3.179

**Gaus mean : 36.7682**

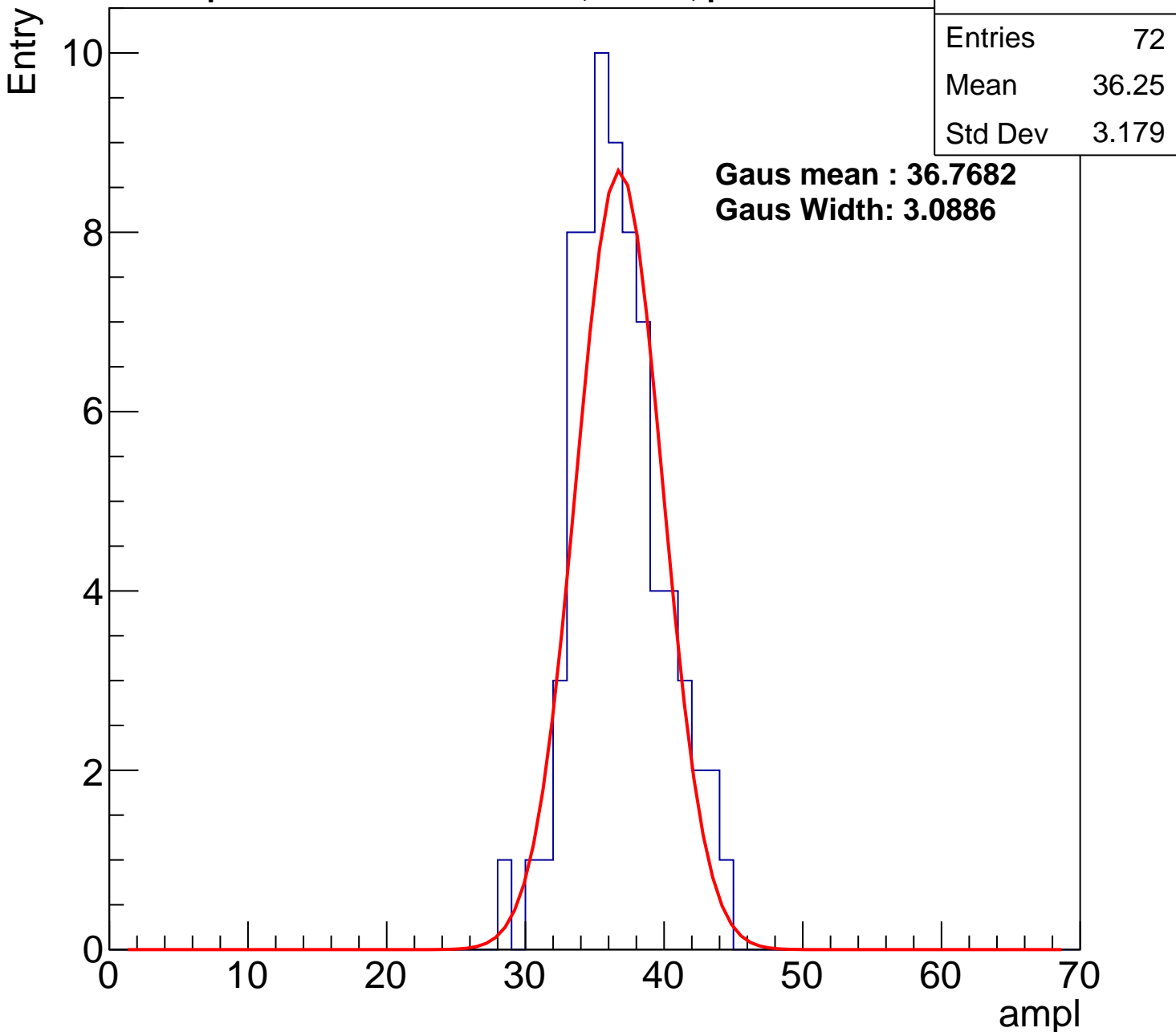
**Gaus Width: 3.0886**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U11-ch46, adc2

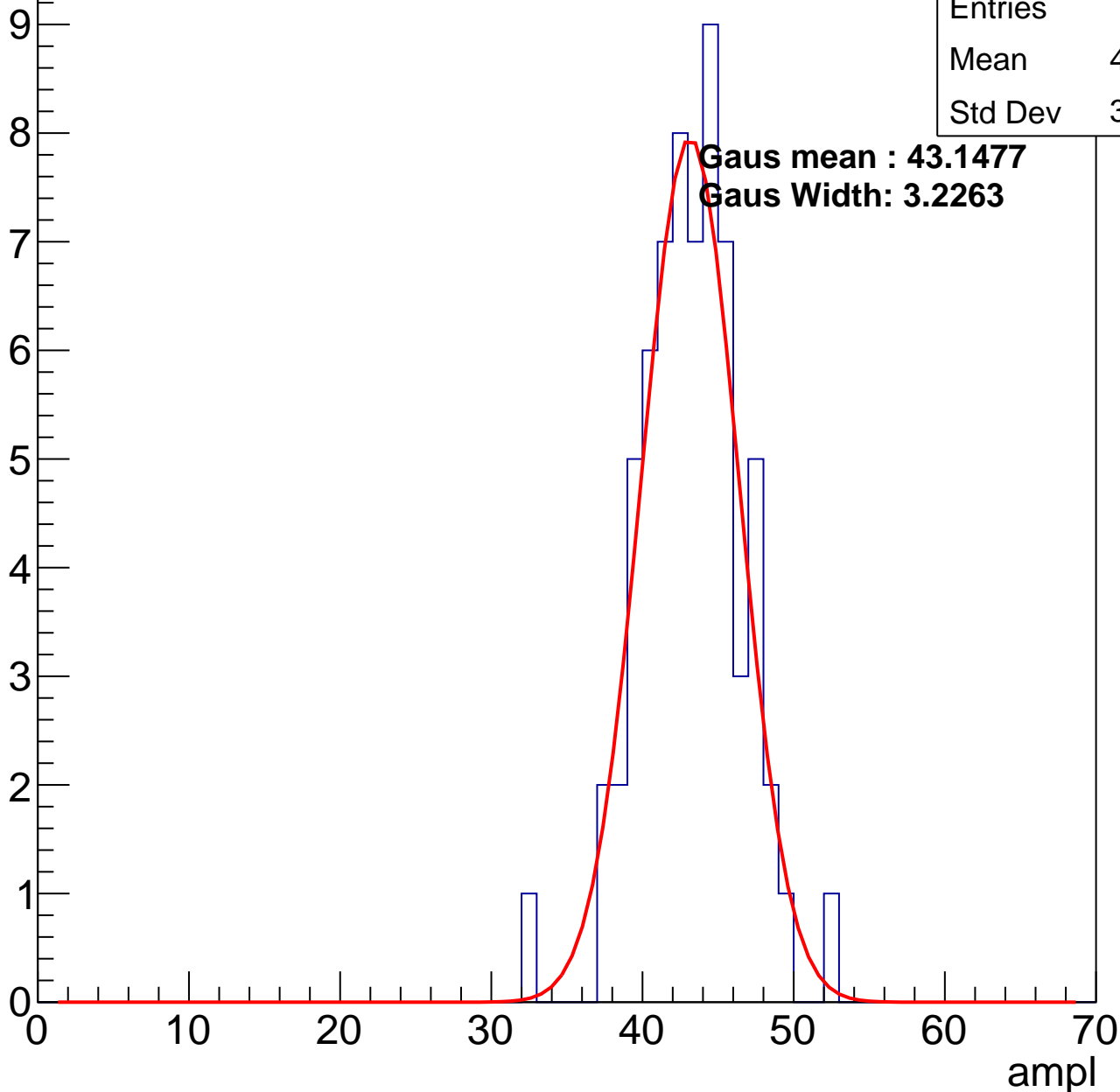
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	42.76
Std Dev	3.303

**Gaus mean : 43.1477**

**Gaus Width: 3.2263**



# B1L003S, U11-ch46, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	58
Mean	48.98
Std Dev	2.927

Entry

10

8

6

4

2

0

0

10

20

30

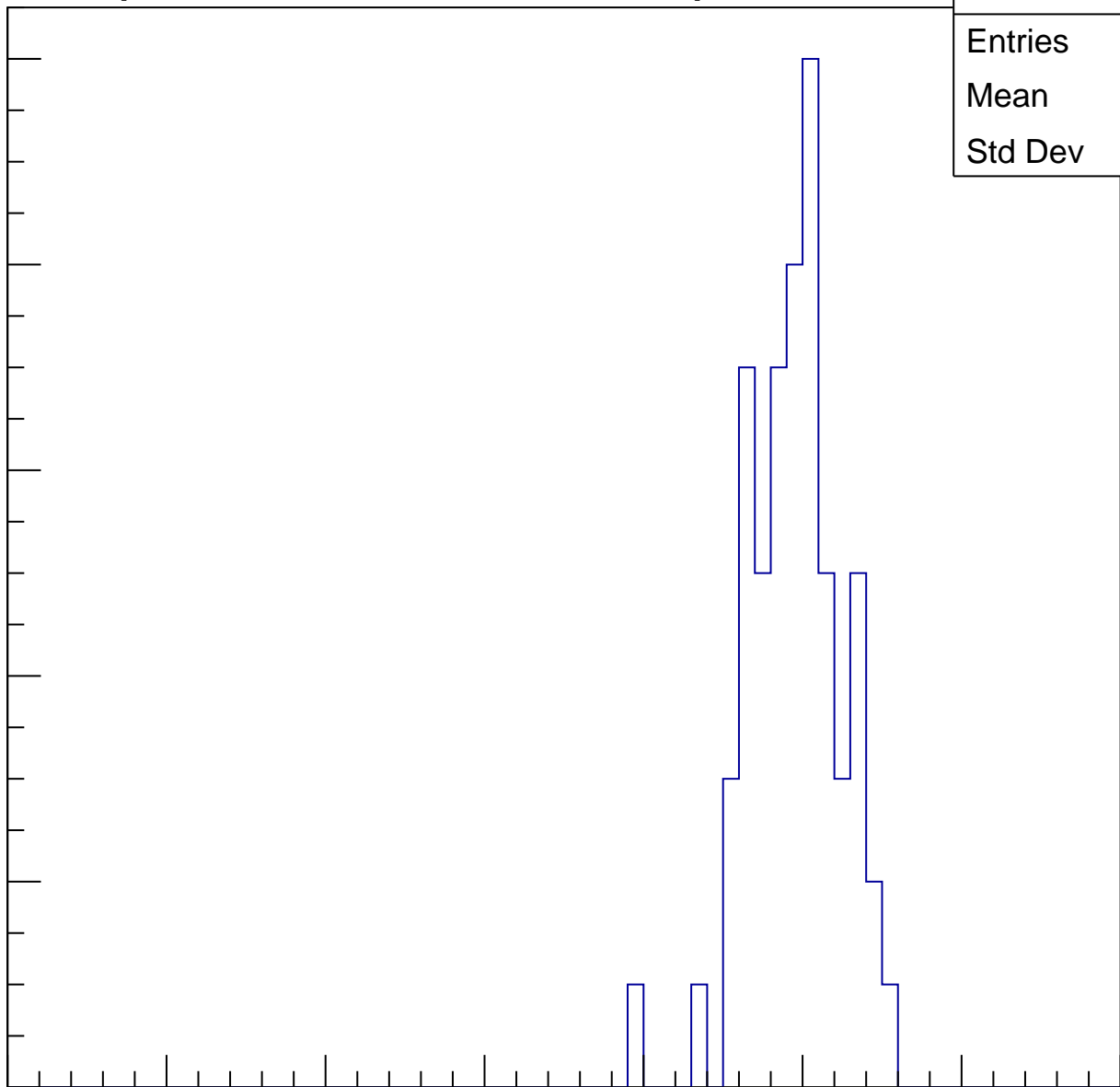
40

50

60

70

ampl

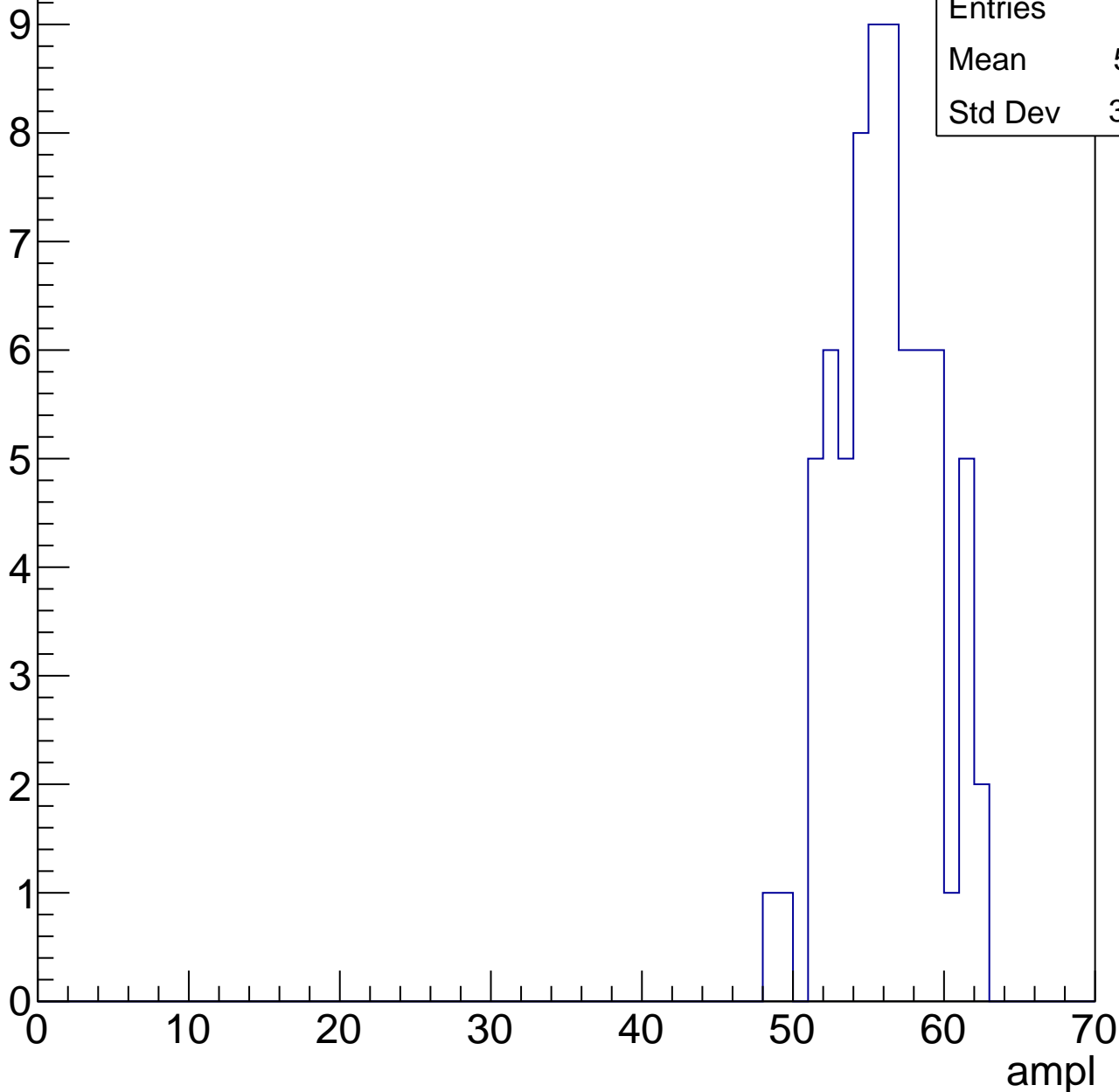


# B1L003S, U11-ch46, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	55.61
Std Dev	3.177

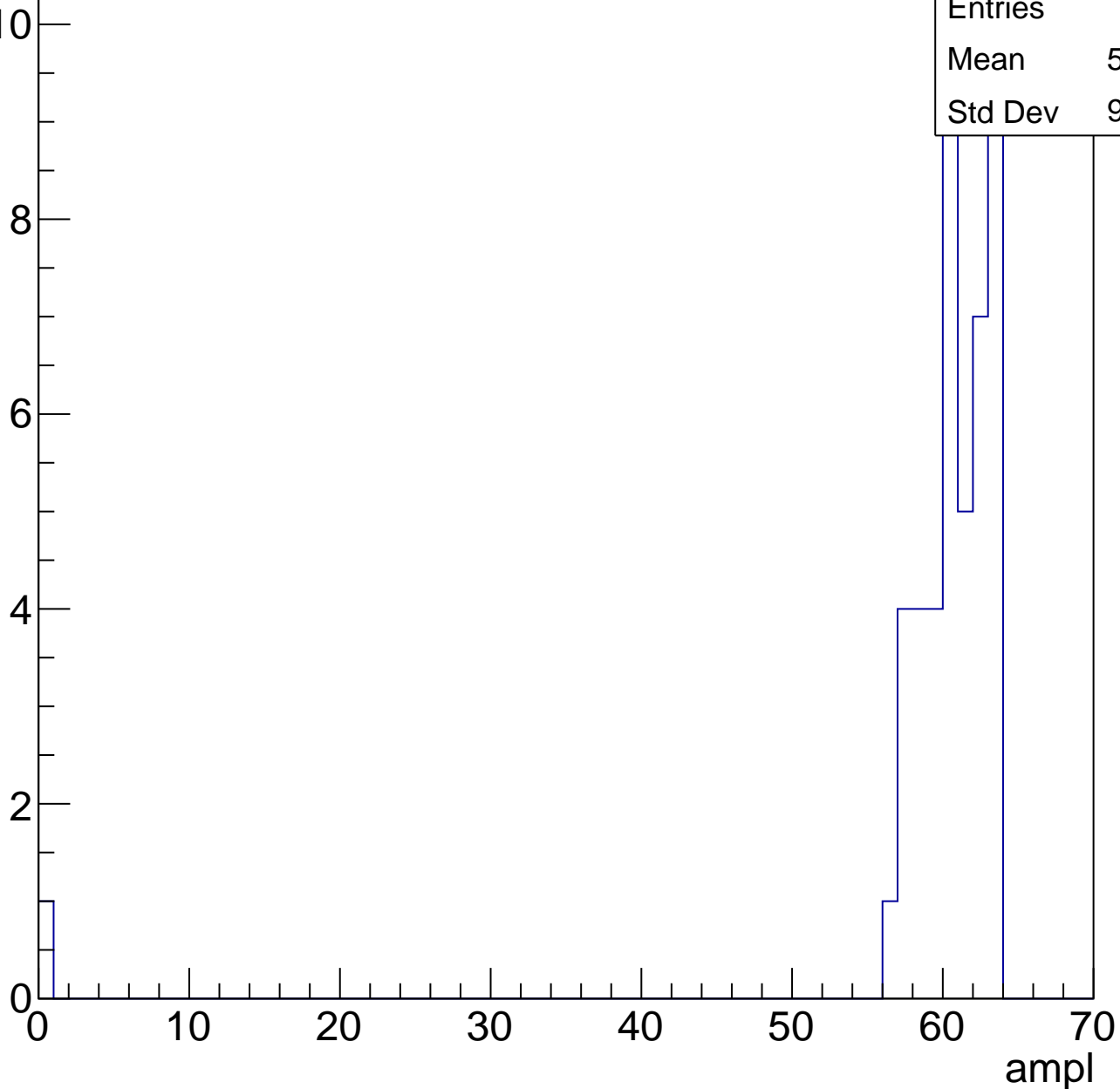


# B1L003S, U11-ch46, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	45
Mean	59.13
Std Dev	9.142



# B1L003S, U11-ch46, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch46, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L003S, U11-ch47, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	77
Mean	31.23
Std Dev	3.251

**Gaus mean : 31.4948**

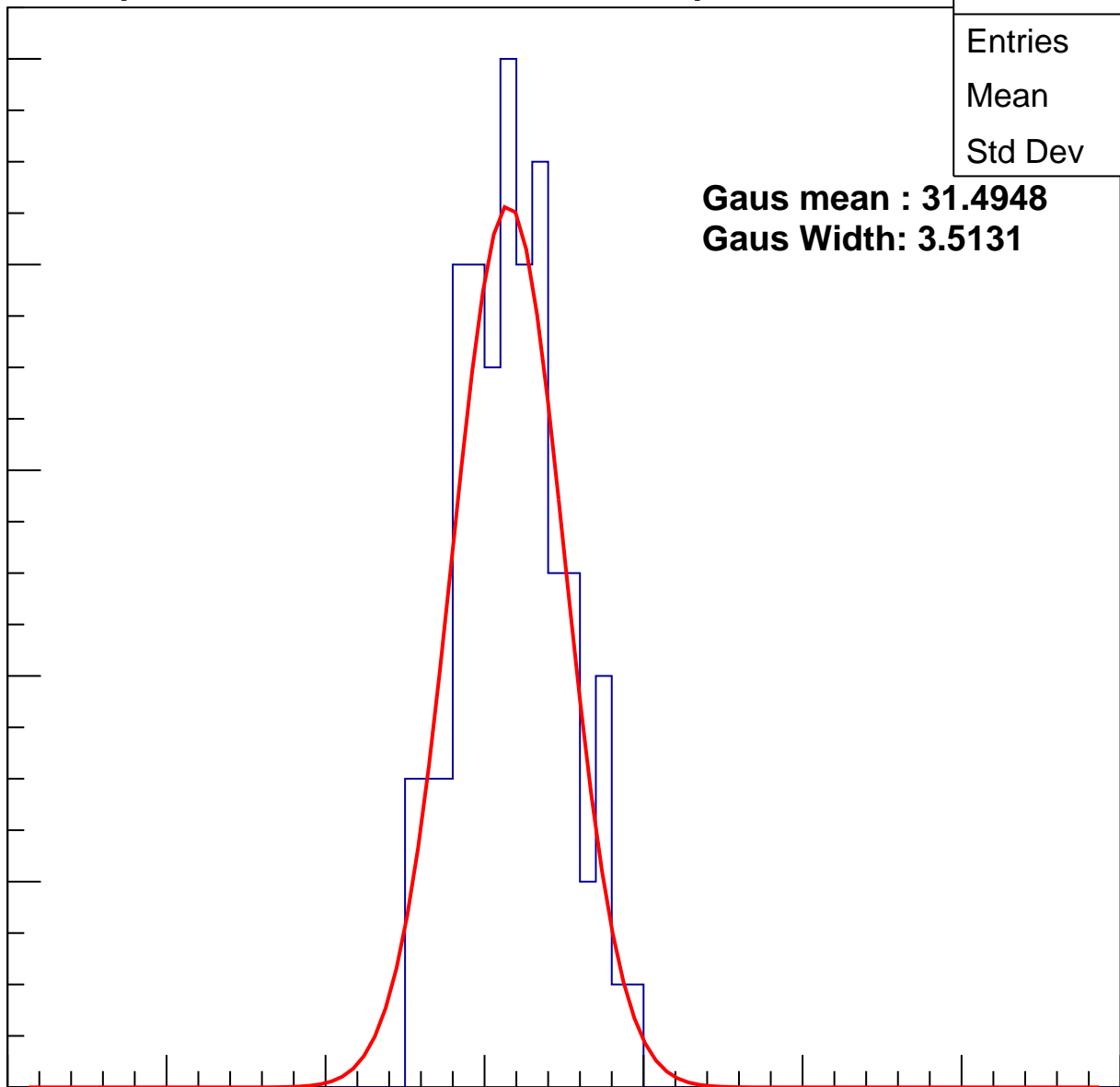
**Gaus Width: 3.5131**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U11-ch47, adc1

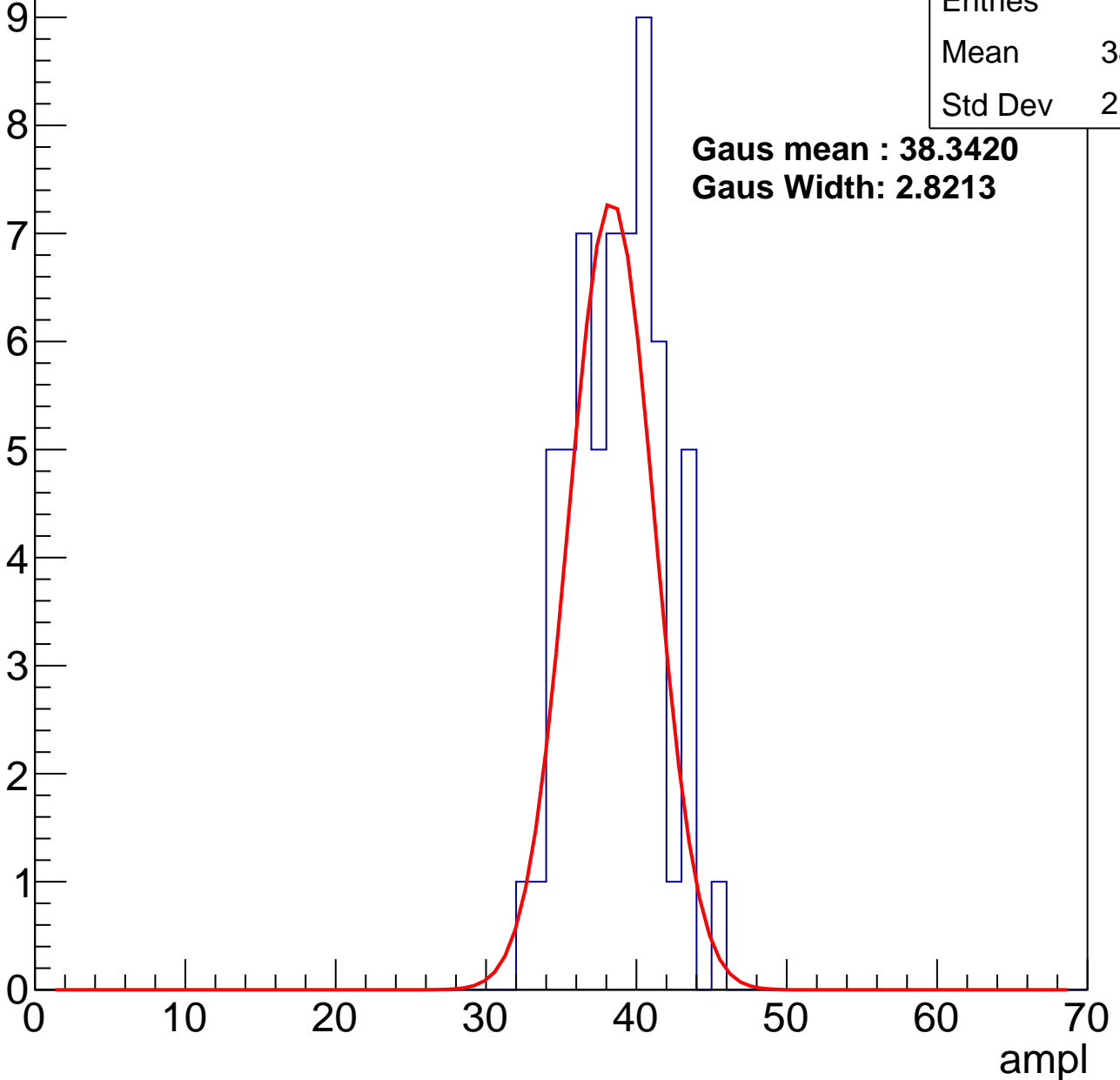
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	38.23
Std Dev	2.895

**Gaus mean : 38.3420**

**Gaus Width: 2.8213**



# B1L003S, U11-ch47, adc2

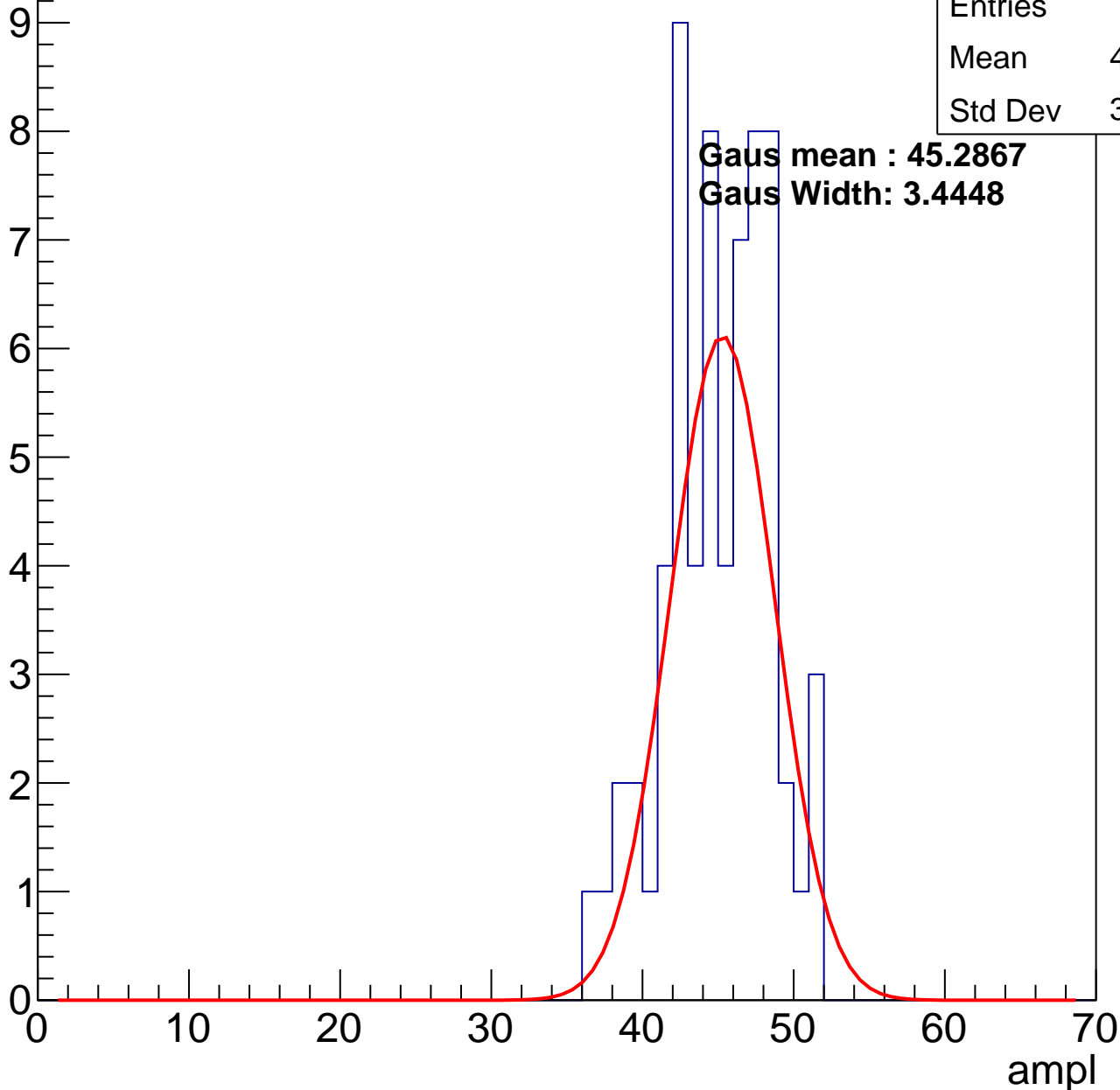
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	44.55
Std Dev	3.446

**Gaus mean : 45.2867**

**Gaus Width: 3.4448**



# B1L003S, U11-ch47, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	72
Mean	50.74
Std Dev	3.371

Entry

10

8

6

4

2

0

0

10

20

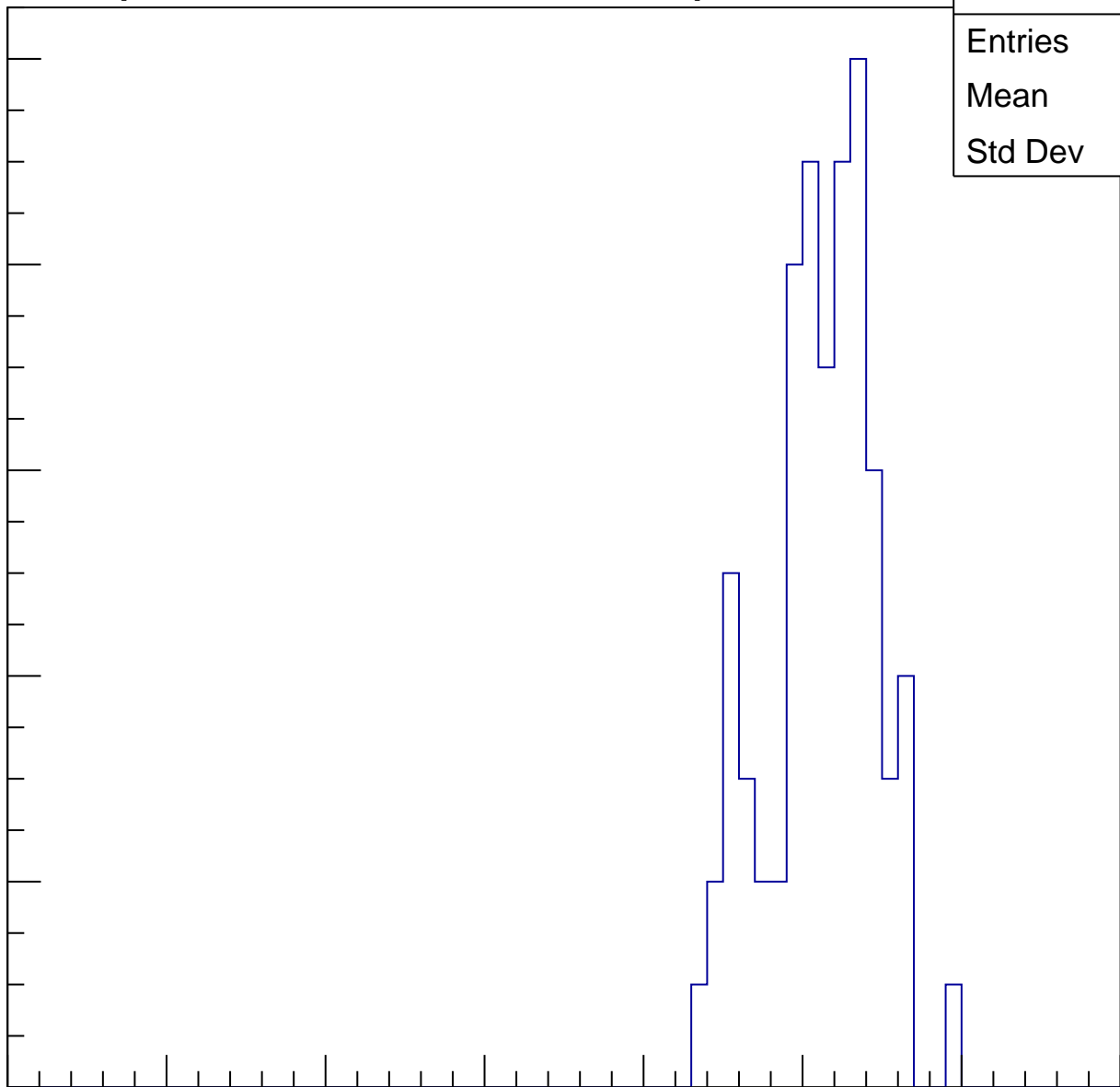
30

40

50

60

ampl

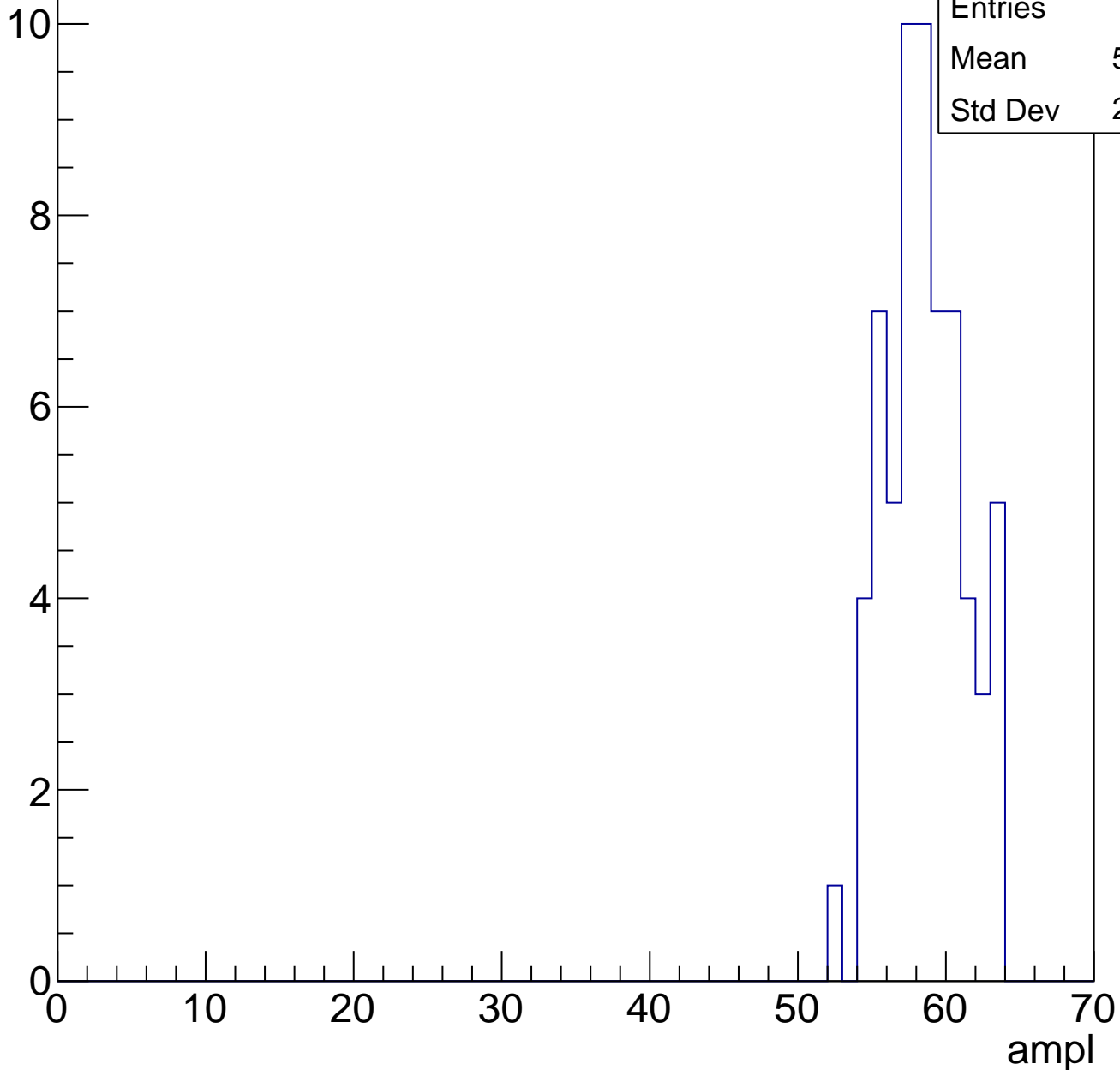


# B1L003S, U11-ch47, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	63
Mean	58.11
Std Dev	2.631

Entry

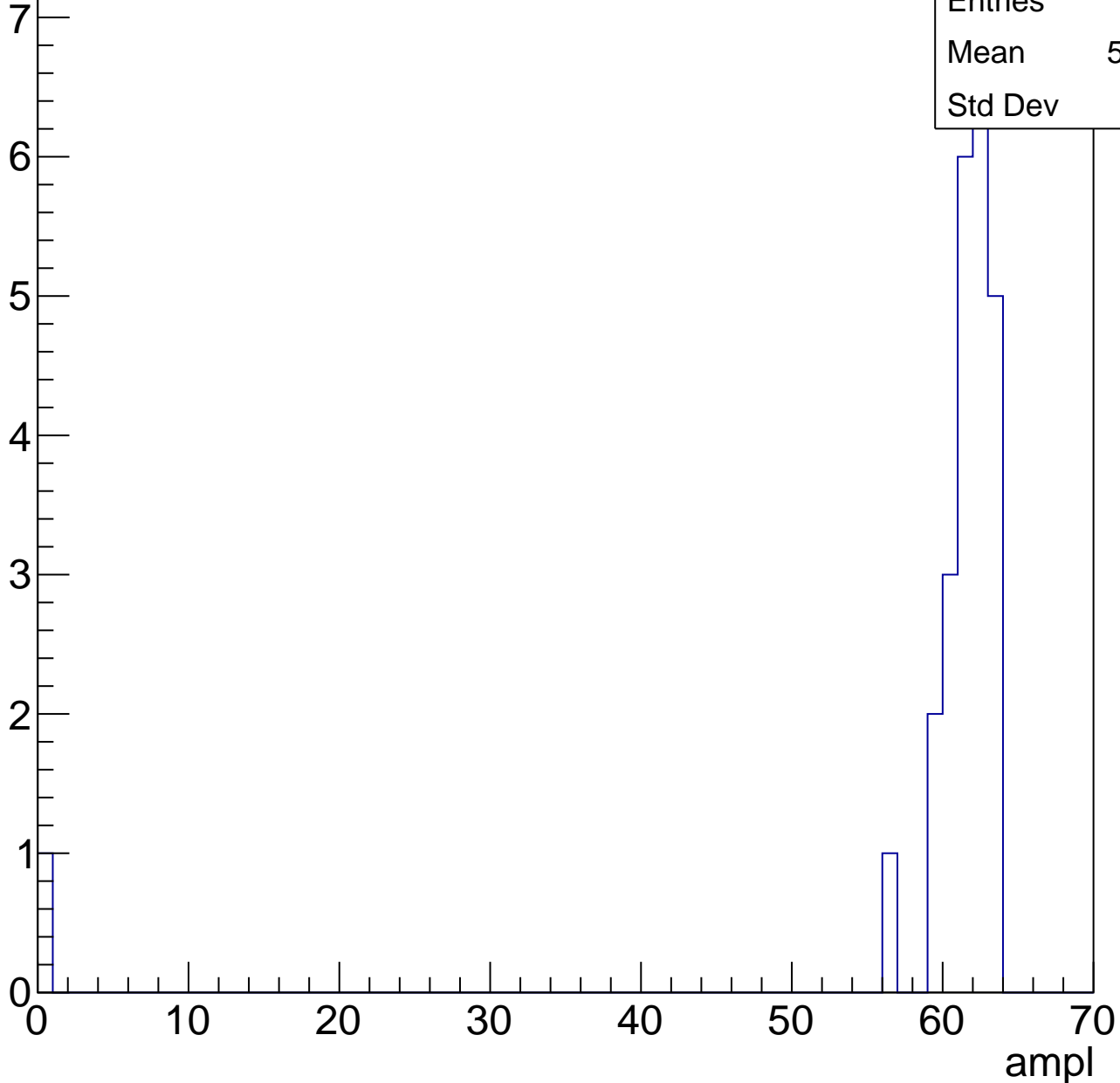


# B1L003S, U11-ch47, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	25
Mean	58.76
Std Dev	12.1



# B1L003S, U11-ch47, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L003S, U11-ch47, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	11.5
Std Dev	11.5

# B1L003S, U11-ch48, adc0

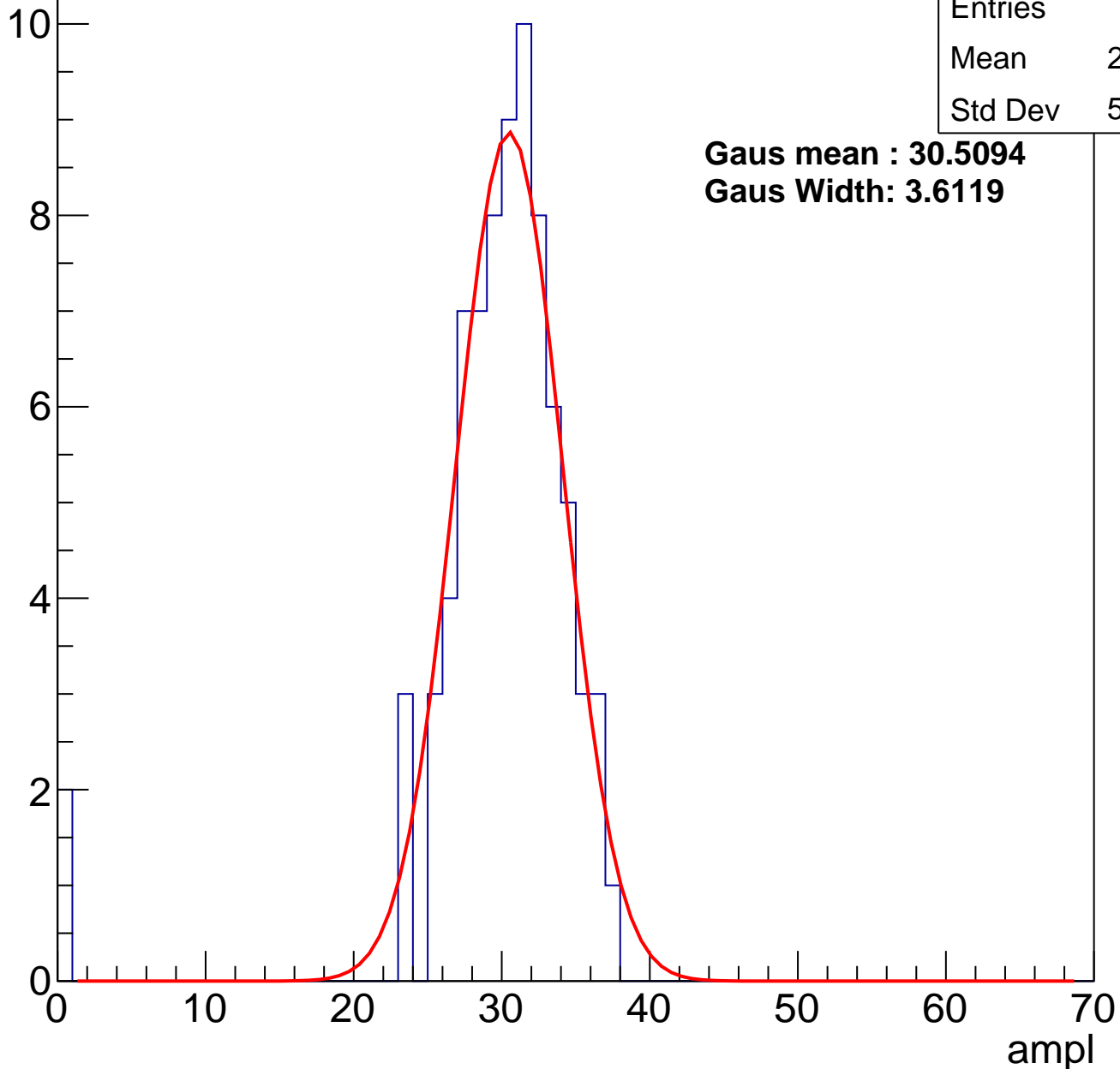
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	79
Mean	29.35
Std Dev	5.693

**Gaus mean : 30.5094**

**Gaus Width: 3.6119**

Entry



# B1L003S, U11-ch48, adc1

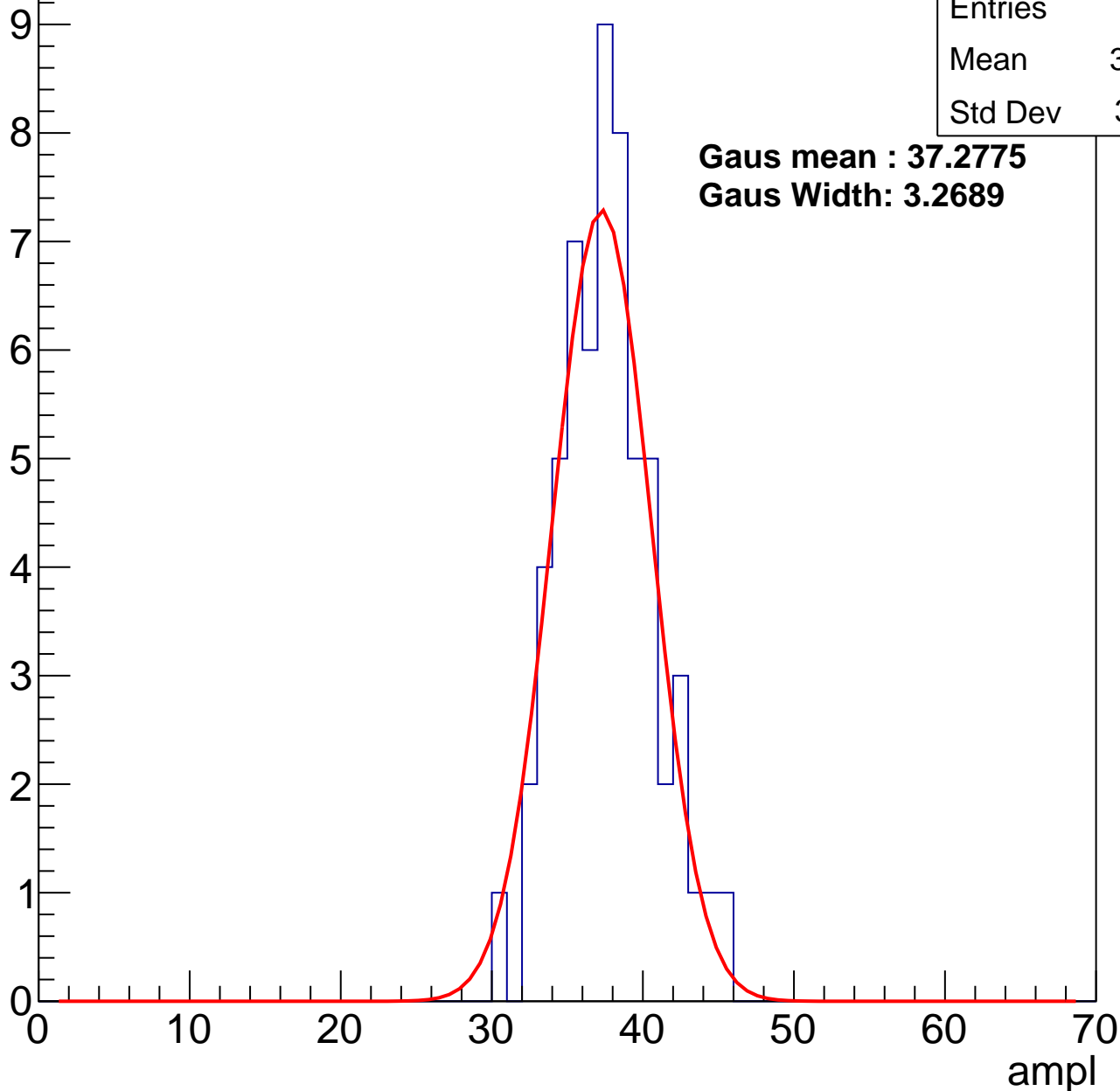
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	37.15
Std Dev	3.081

**Gaus mean : 37.2775**

**Gaus Width: 3.2689**



# B1L003S, U11-ch48, adc2

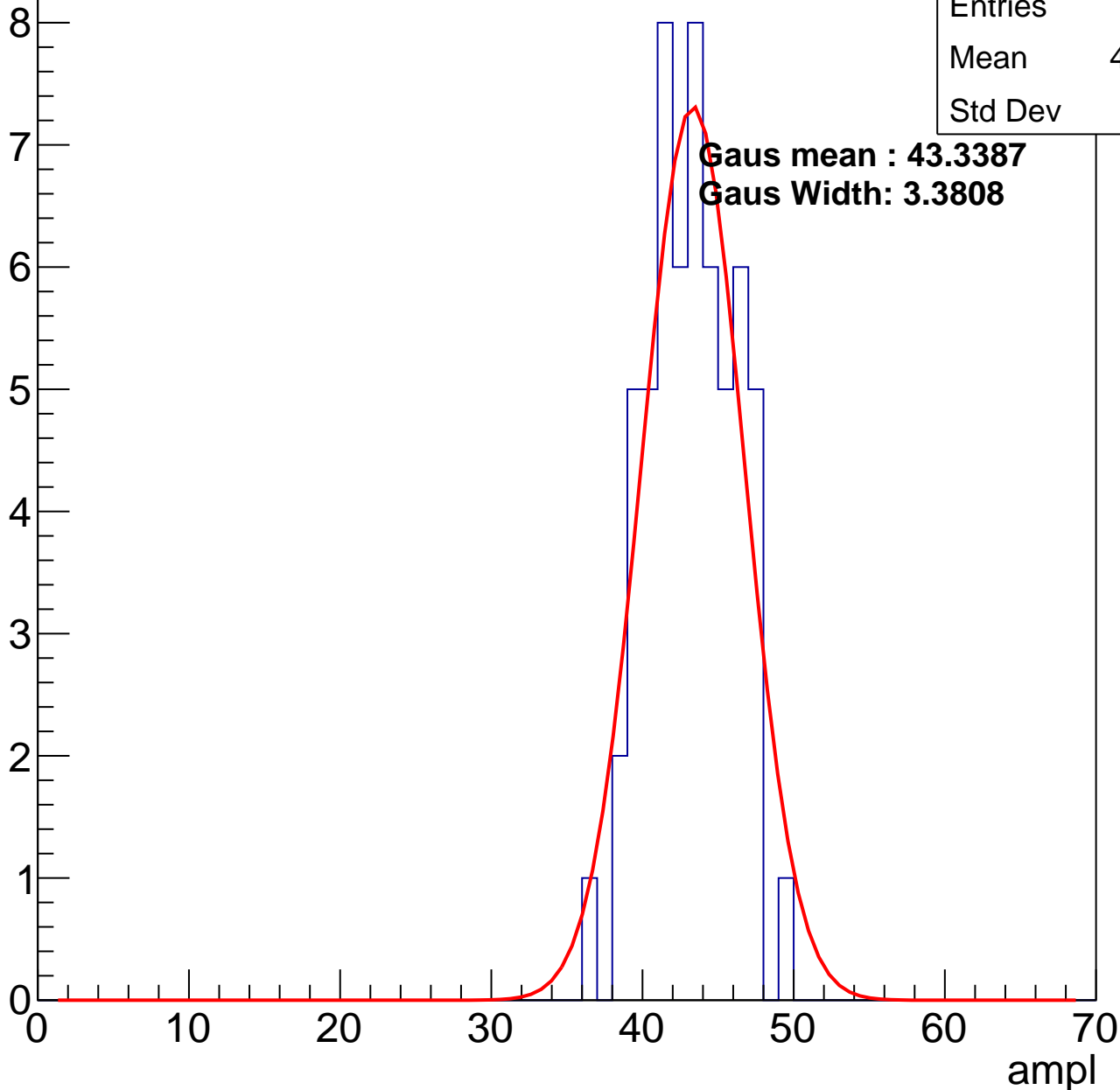
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	42.76
Std Dev	2.8

**Gaus mean : 43.3387**

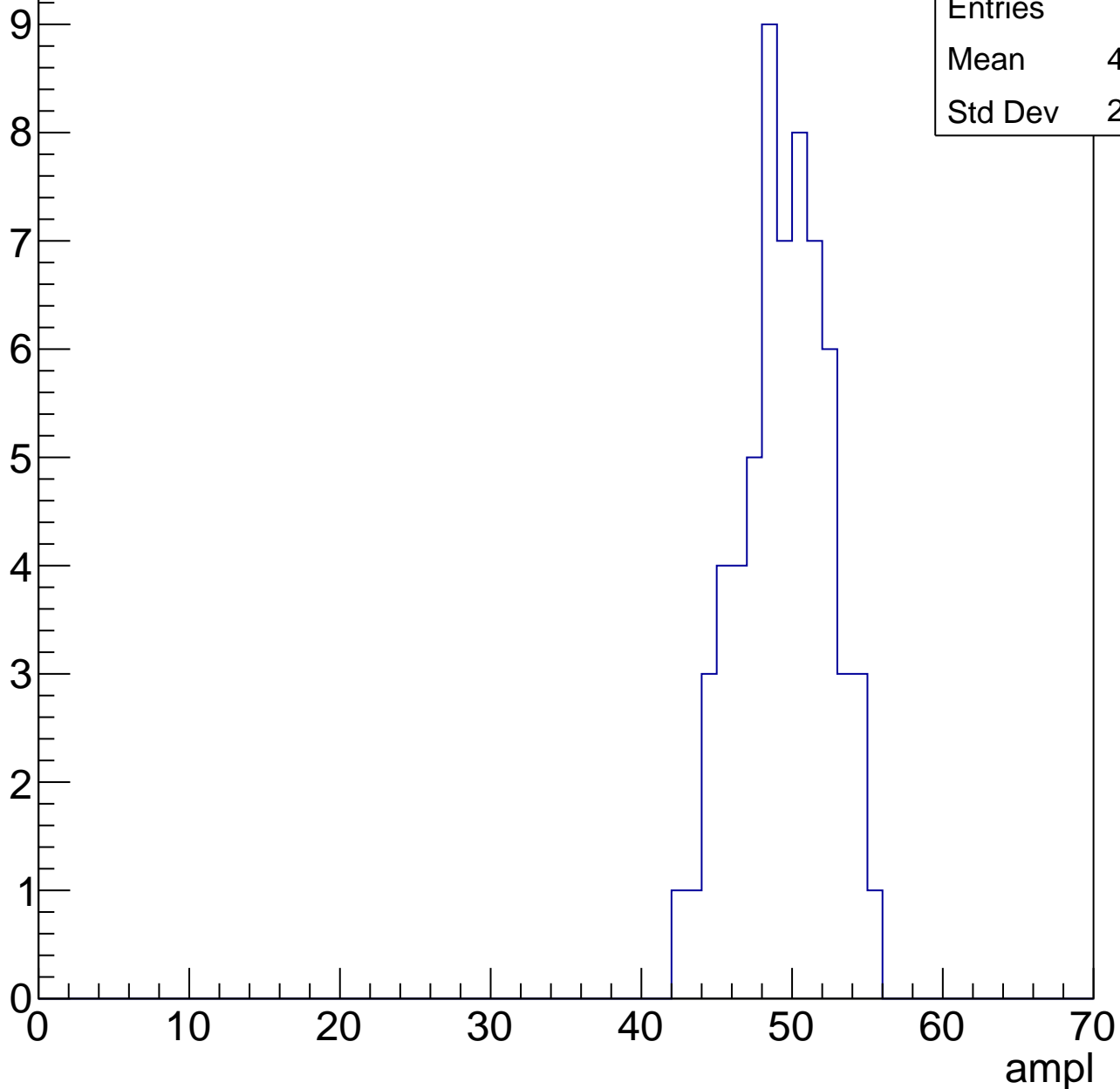
**Gaus Width: 3.3808**



# B1L003S, U11-ch48, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



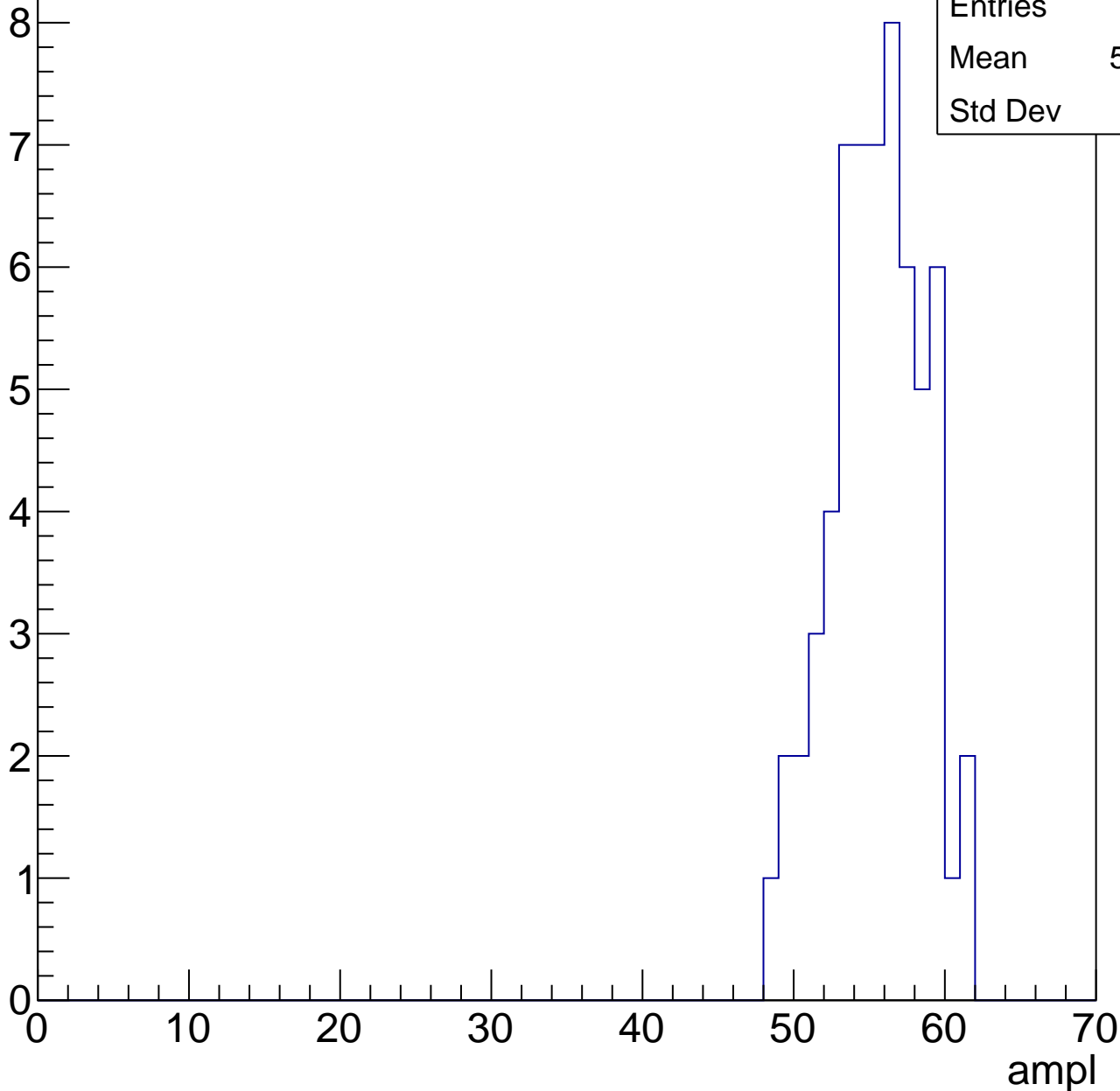
Entries	62
Mean	48.97
Std Dev	2.946

# B1L003S, U11-ch48, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	55.03
Std Dev	3.03



# B1L003S, U11-ch48, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

ampl

Entries

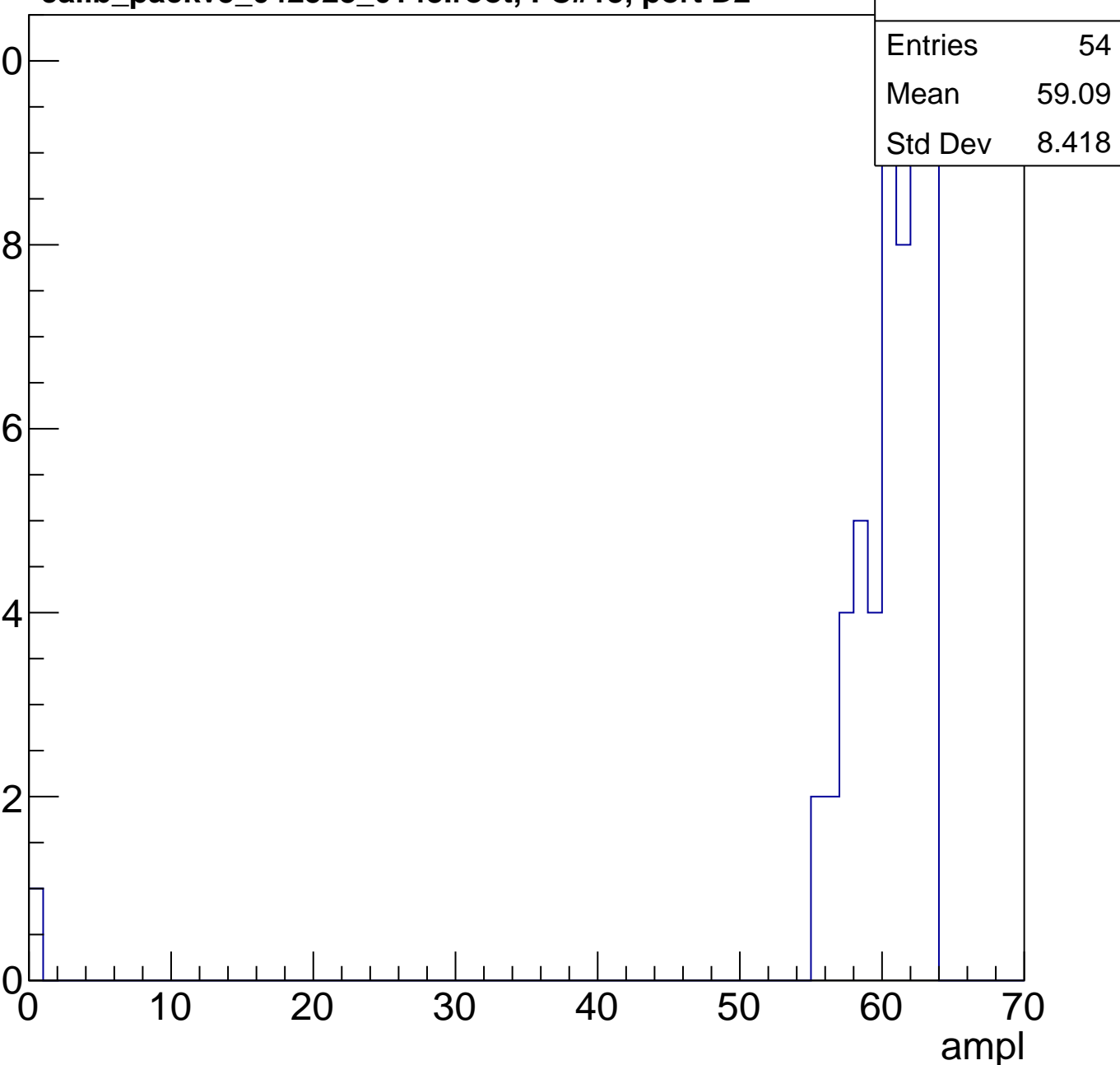
54

Mean

59.09

Std Dev

8.418



# B1L003S, U11-ch48, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch48, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U11-ch49, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	63
Mean	31.48
Std Dev	3.09

**Gaus mean : 31.4729**

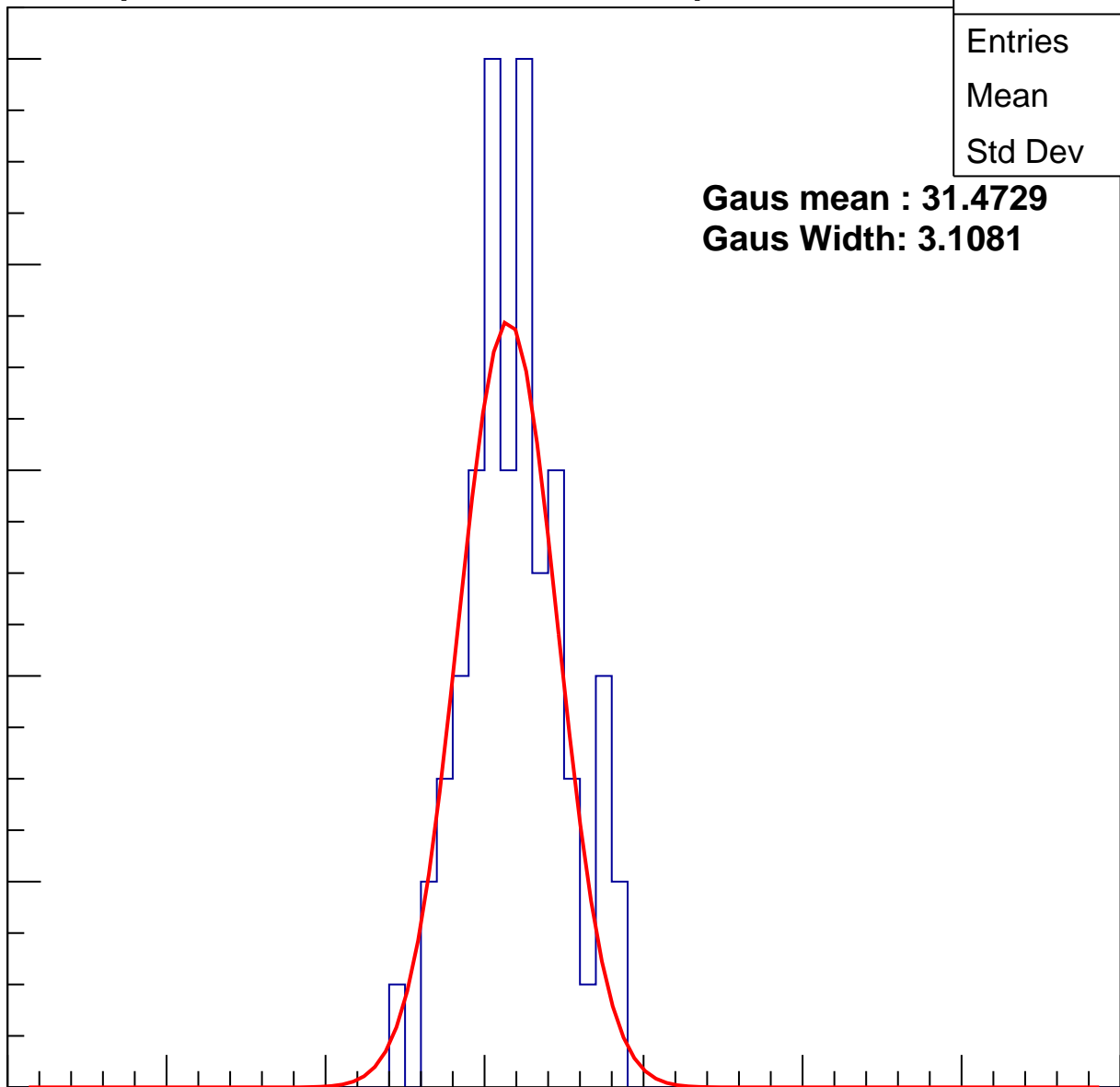
**Gaus Width: 3.1081**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U11-ch49, adc1

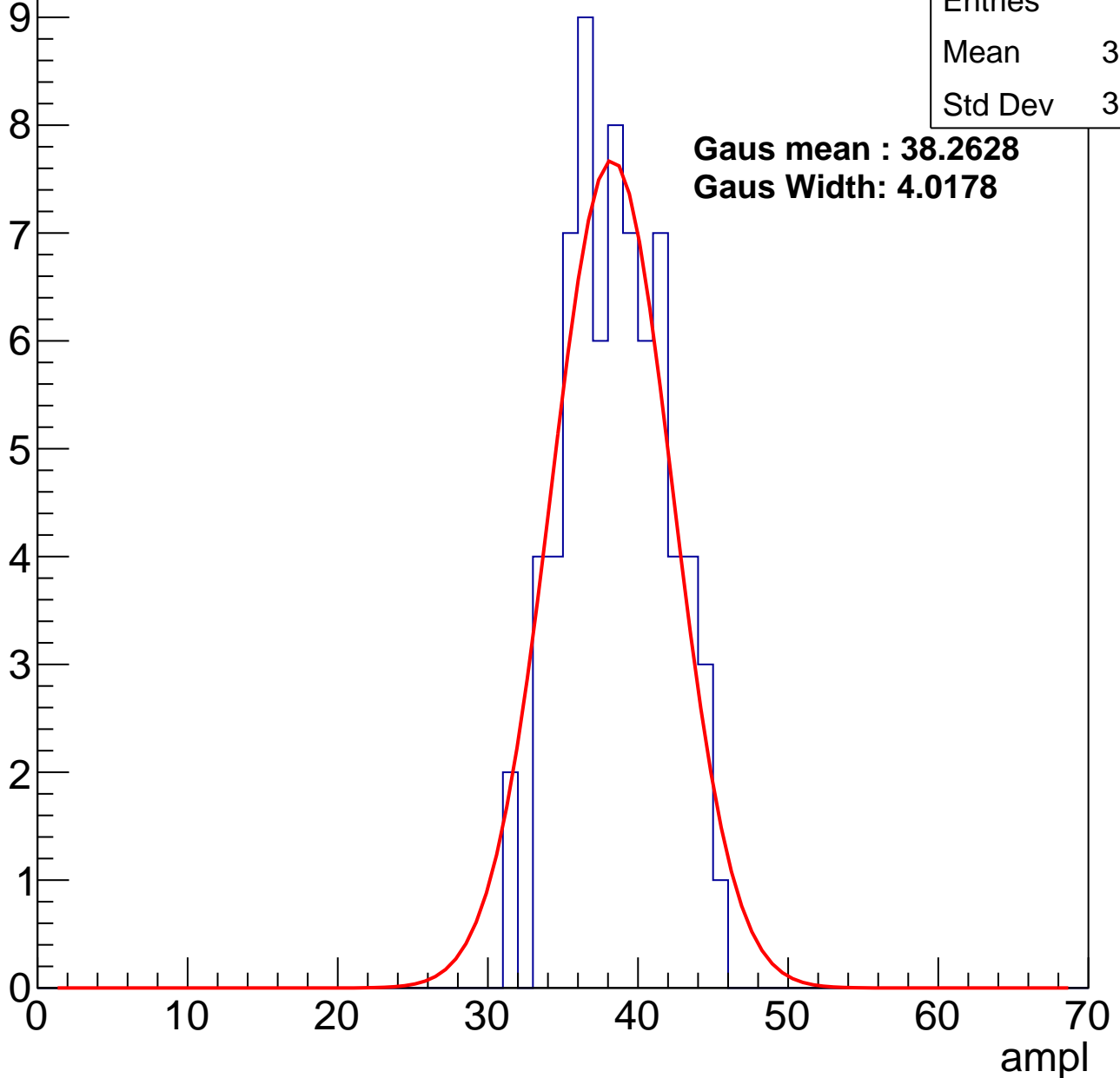
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	72
Mean	38.08
Std Dev	3.295

**Gaus mean : 38.2628**

**Gaus Width: 4.0178**



# B1L003S, U11-ch49, adc2

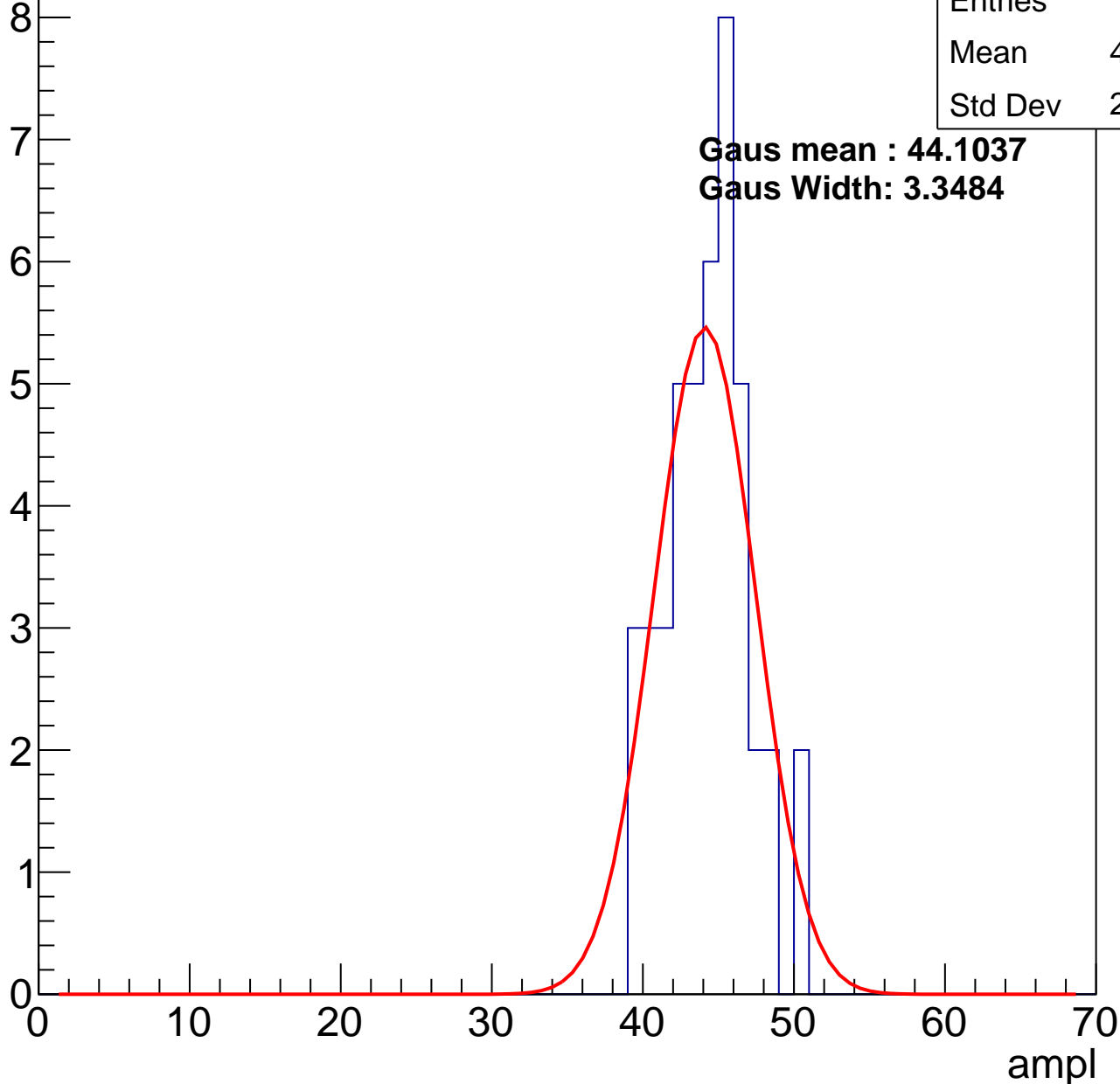
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	44
Mean	43.84
Std Dev	2.713

**Gaus mean : 44.1037**

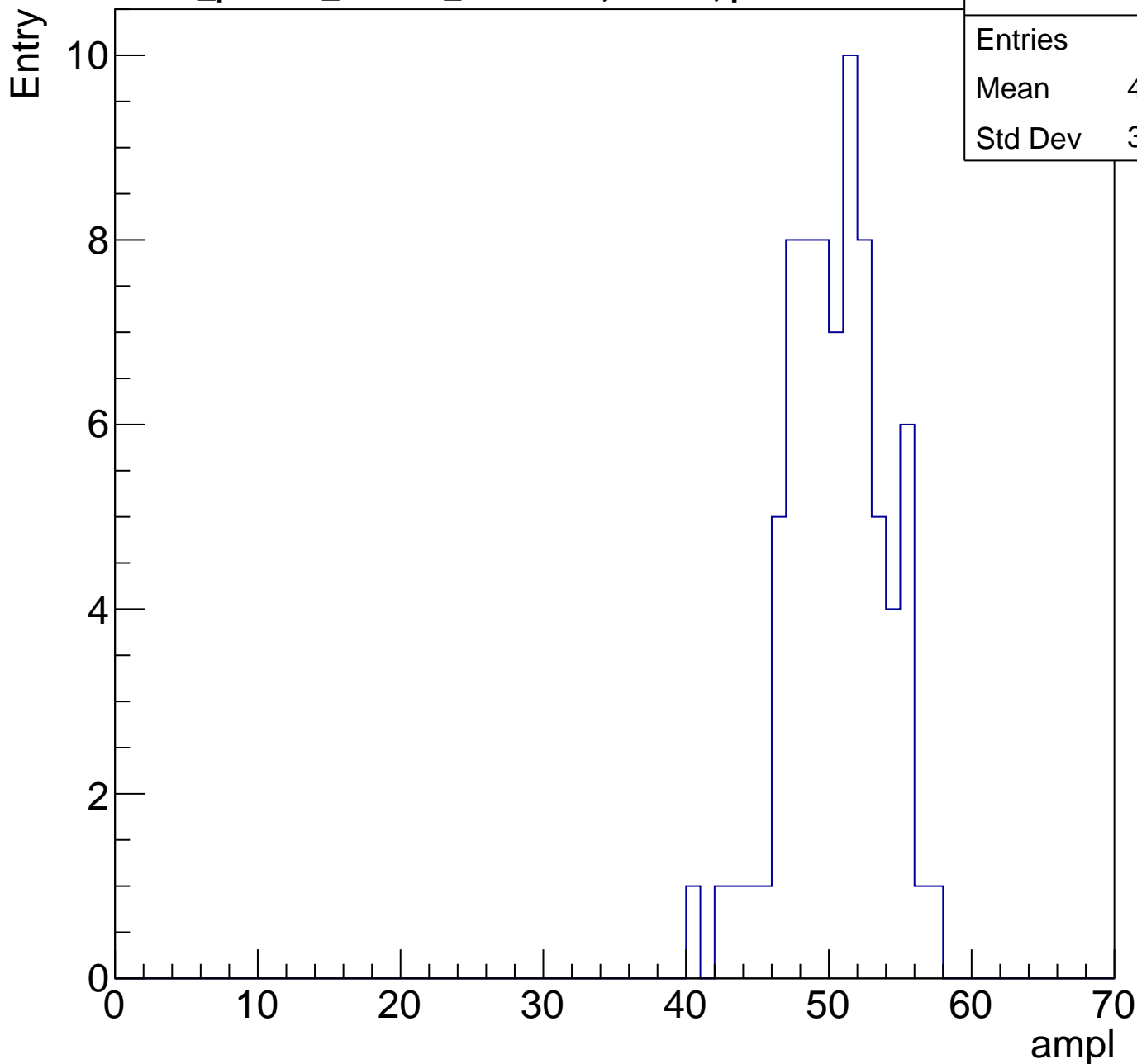
**Gaus Width: 3.3484**



# B1L003S, U11-ch49, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

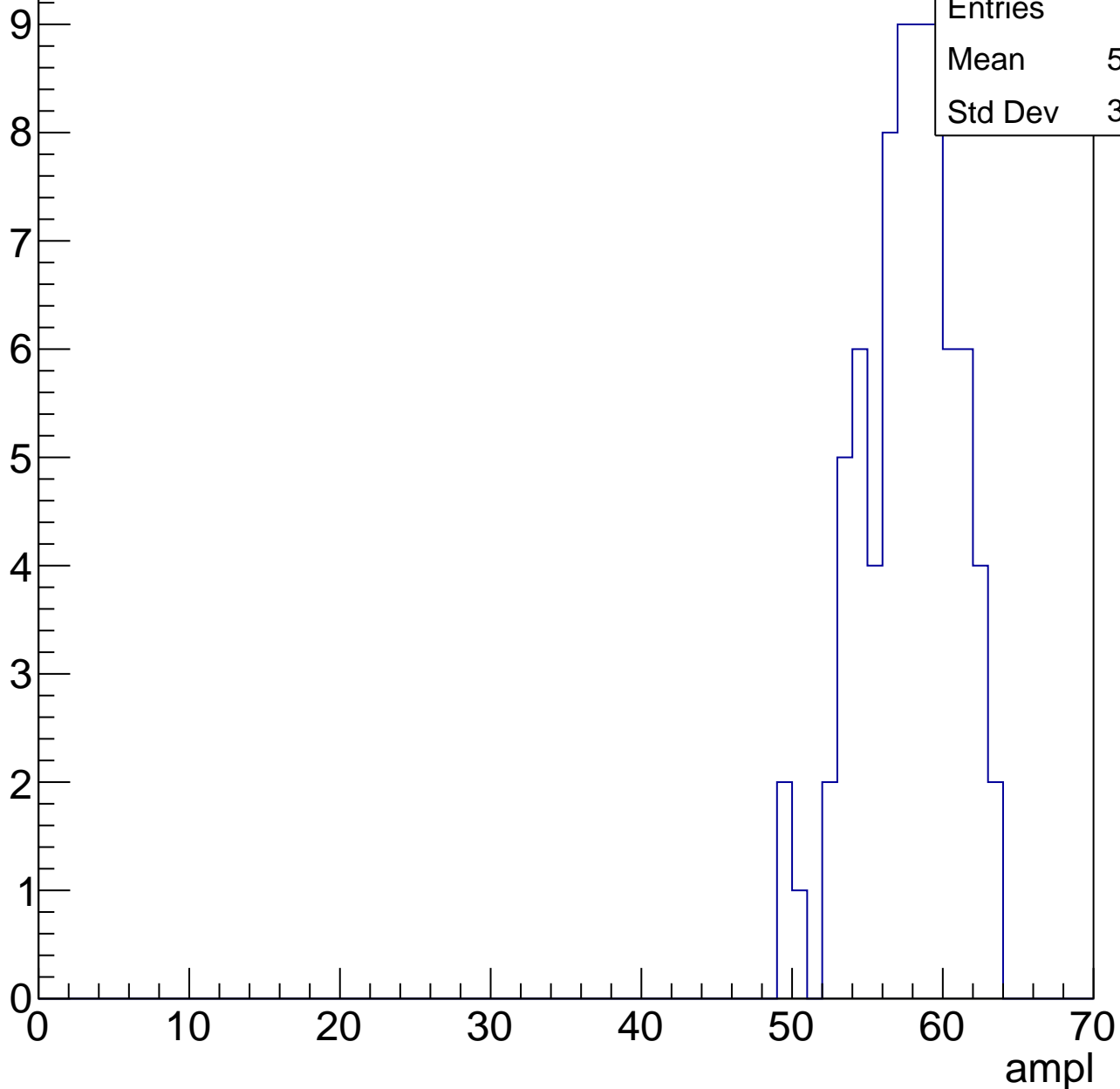
Entries	76
Mean	49.95
Std Dev	3.348



# B1L003S, U11-ch49, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

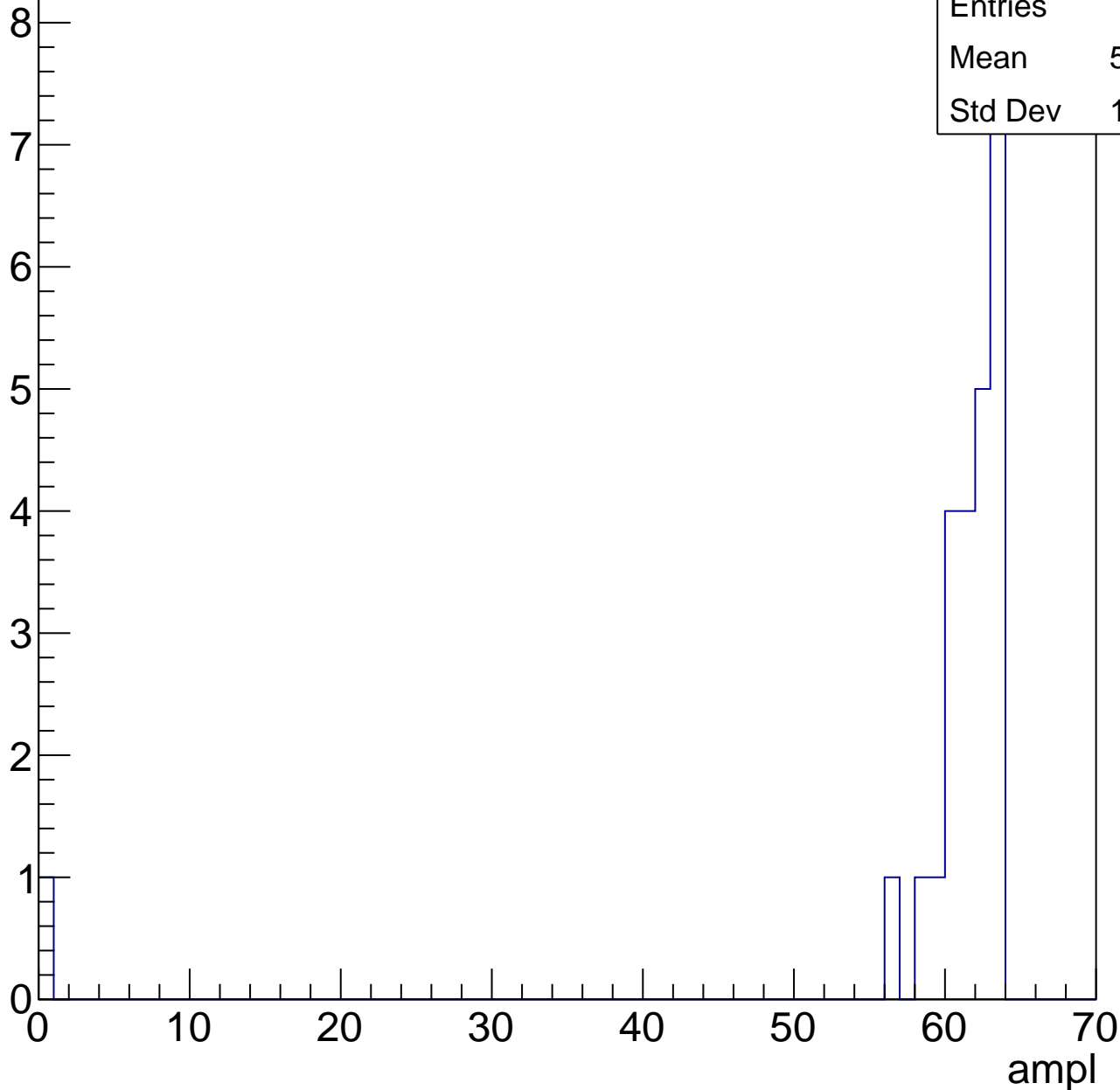


# B1L003S, U11-ch49, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

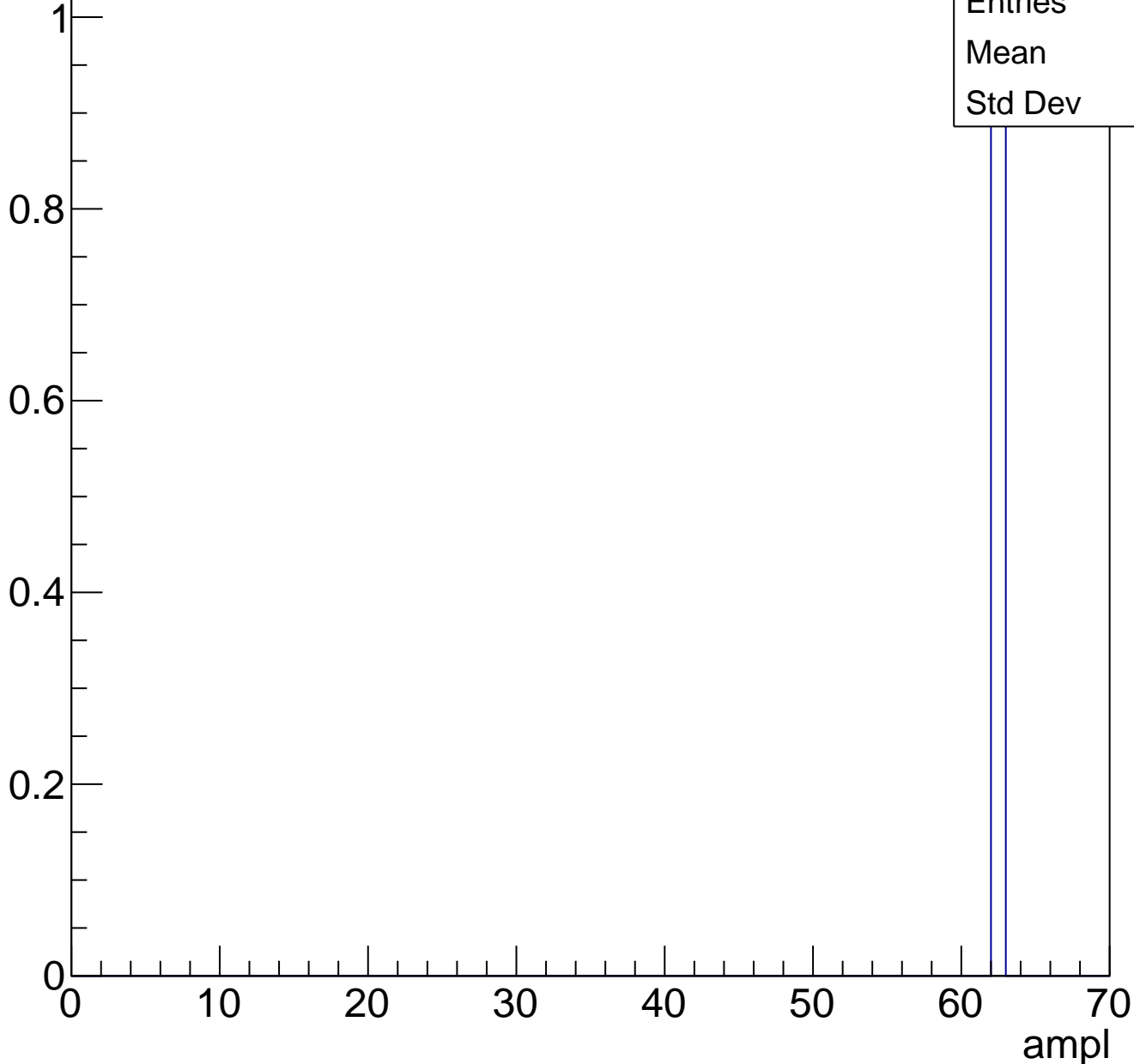
Entries	25
Mean	58.84
Std Dev	12.14



# B1L003S, U11-ch49, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch49, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L003S, U11-ch50, adc0

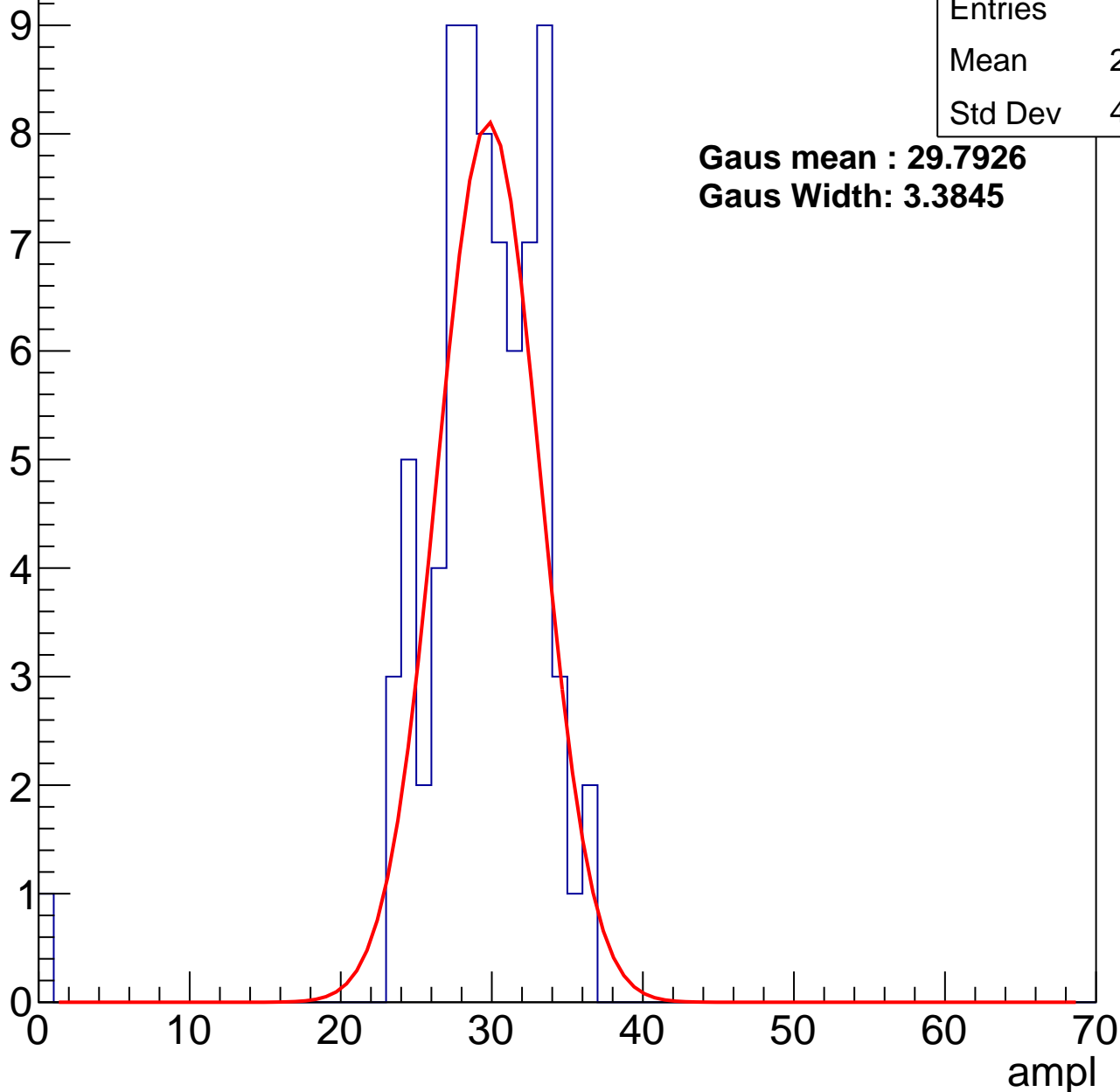
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	76
Mean	28.89
Std Dev	4.636

**Gaus mean : 29.7926**

**Gaus Width: 3.3845**



# B1L003S, U11-ch50, adc1

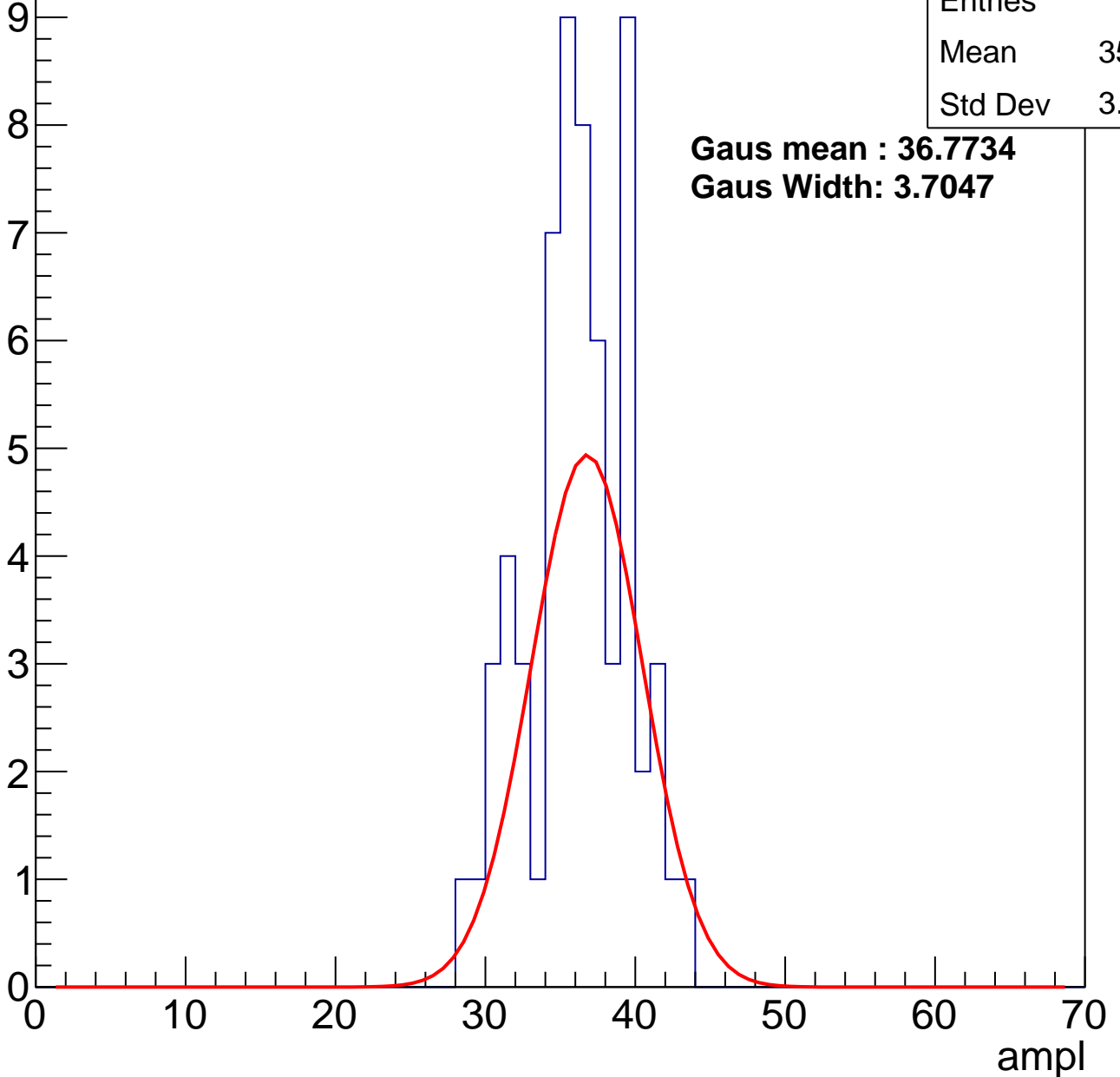
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	35.74
Std Dev	3.365

**Gaus mean : 36.7734**

**Gaus Width: 3.7047**



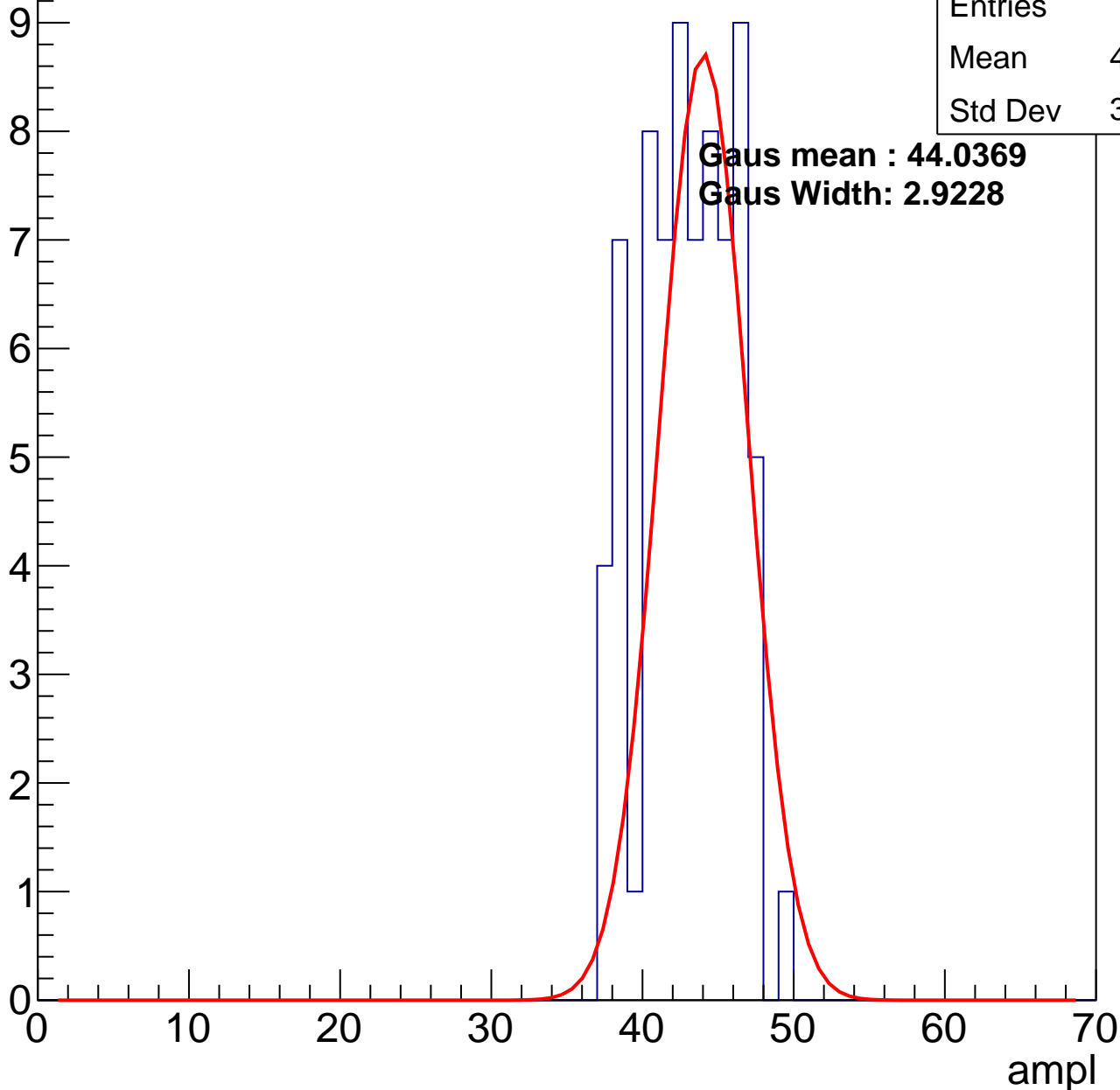
# B1L003S, U11-ch50, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	73
Mean	42.52
Std Dev	3.007

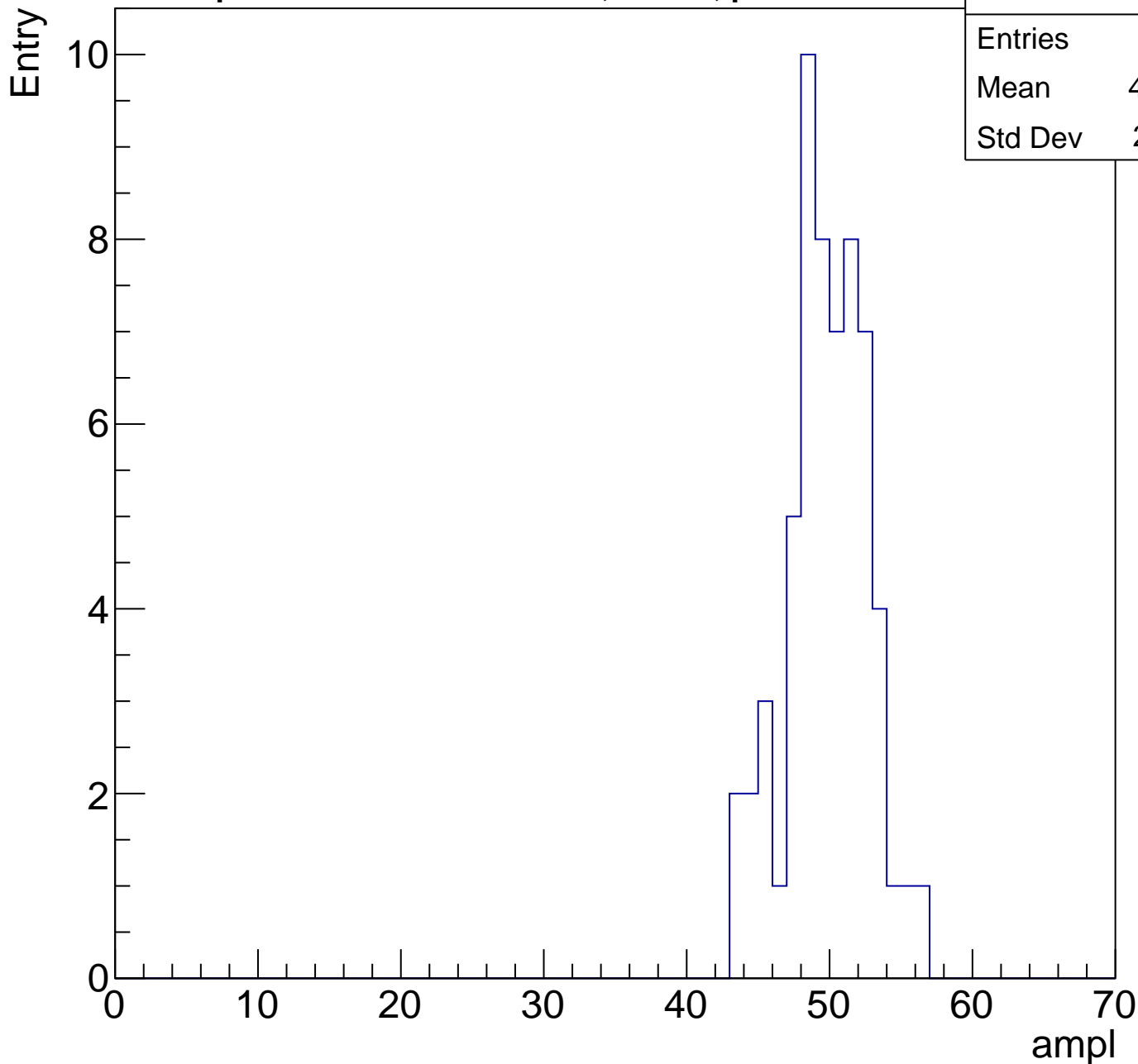
**Gaus mean : 44.0369**  
**Gaus Width: 2.9228**



# B1L003S, U11-ch50, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	60
Mean	49.35
Std Dev	2.821

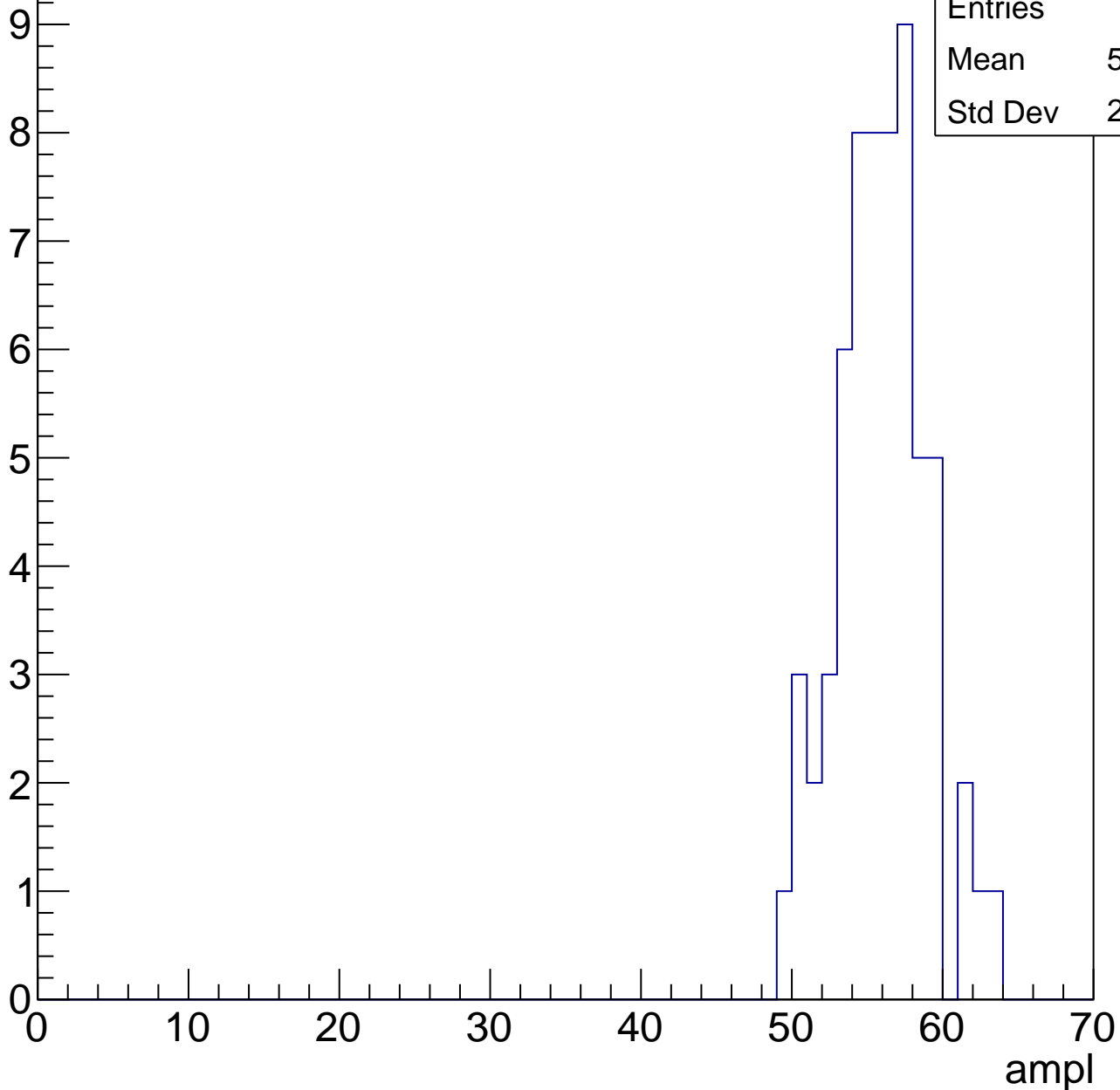


# B1L003S, U11-ch50, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	55.48
Std Dev	2.955

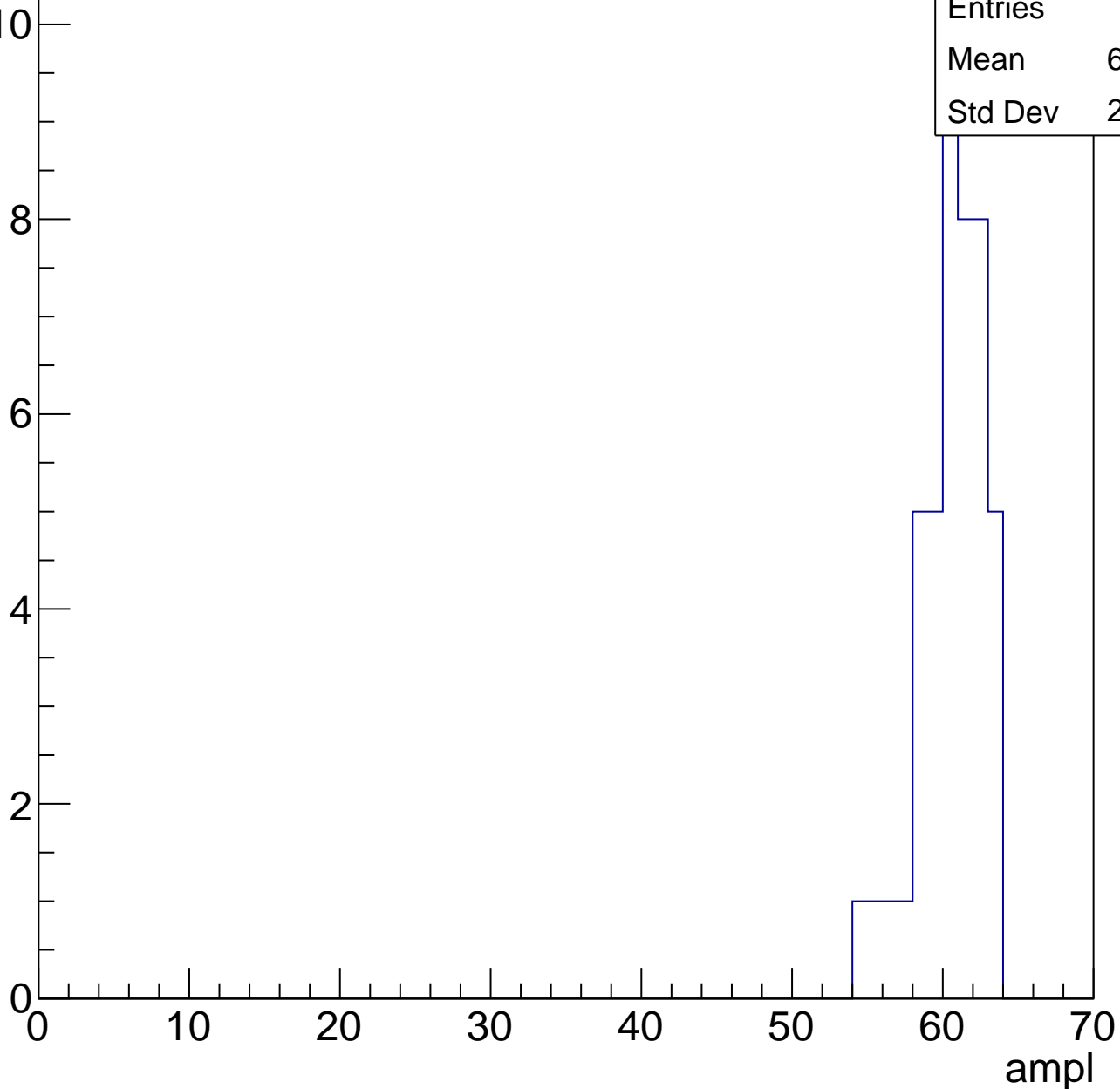


# B1L003S, U11-ch50, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

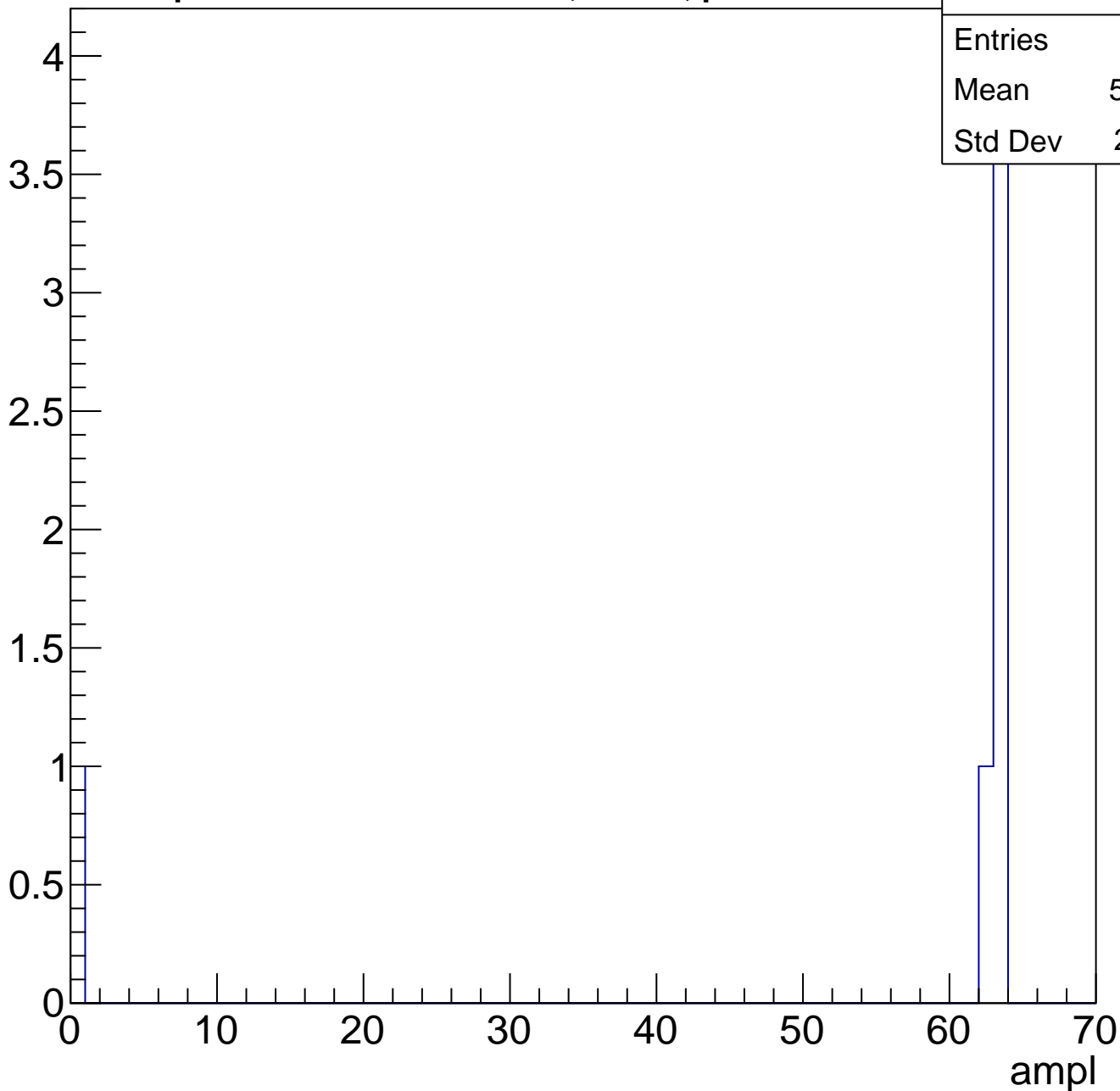
Entries	45
Mean	60.13
Std Dev	2.083



# B1L003S, U11-ch50, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch50, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U11-ch51, adc0

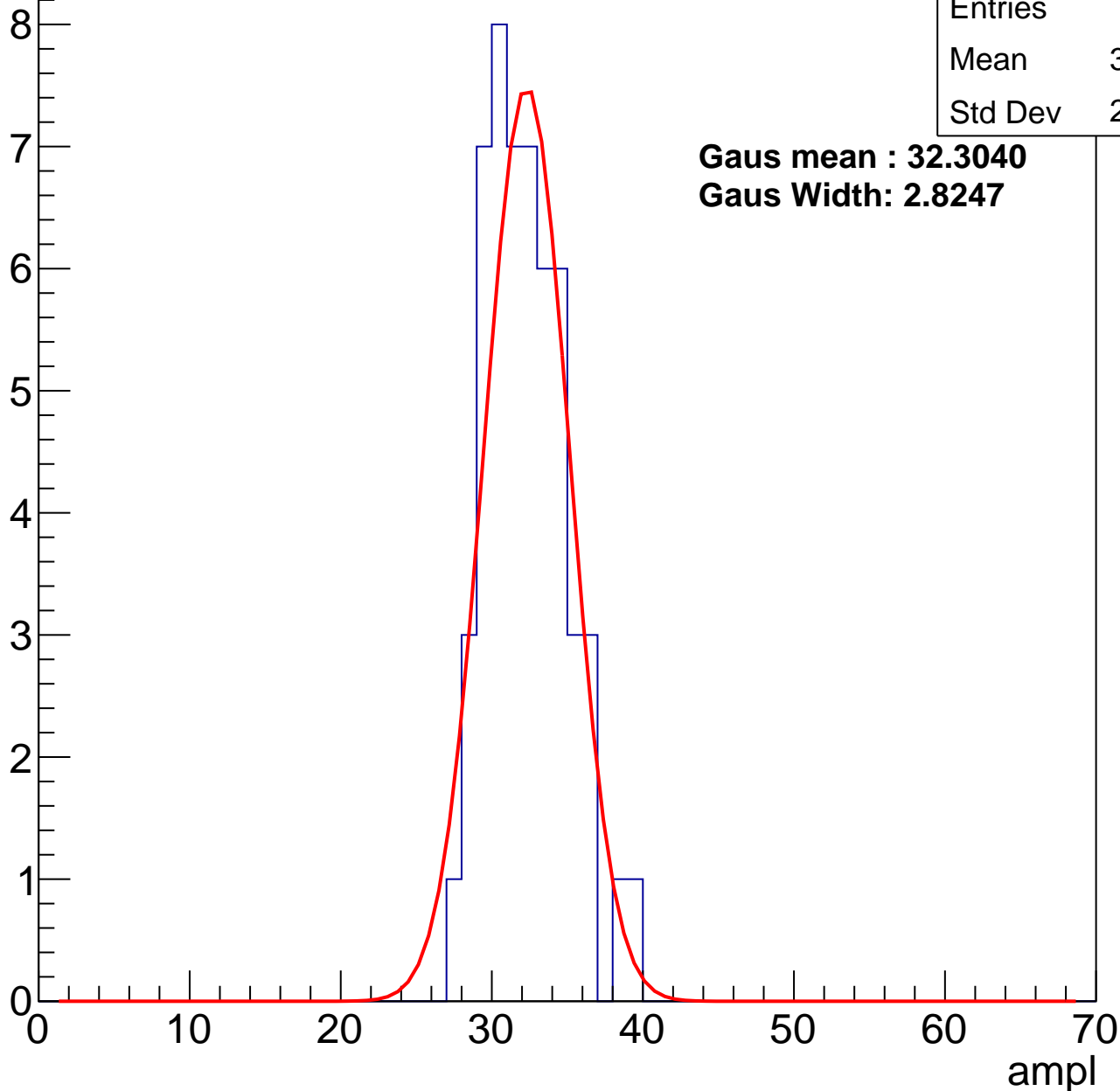
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	31.83
Std Dev	2.619

**Gaus mean : 32.3040**

**Gaus Width: 2.8247**



# B1L003S, U11-ch51, adc1

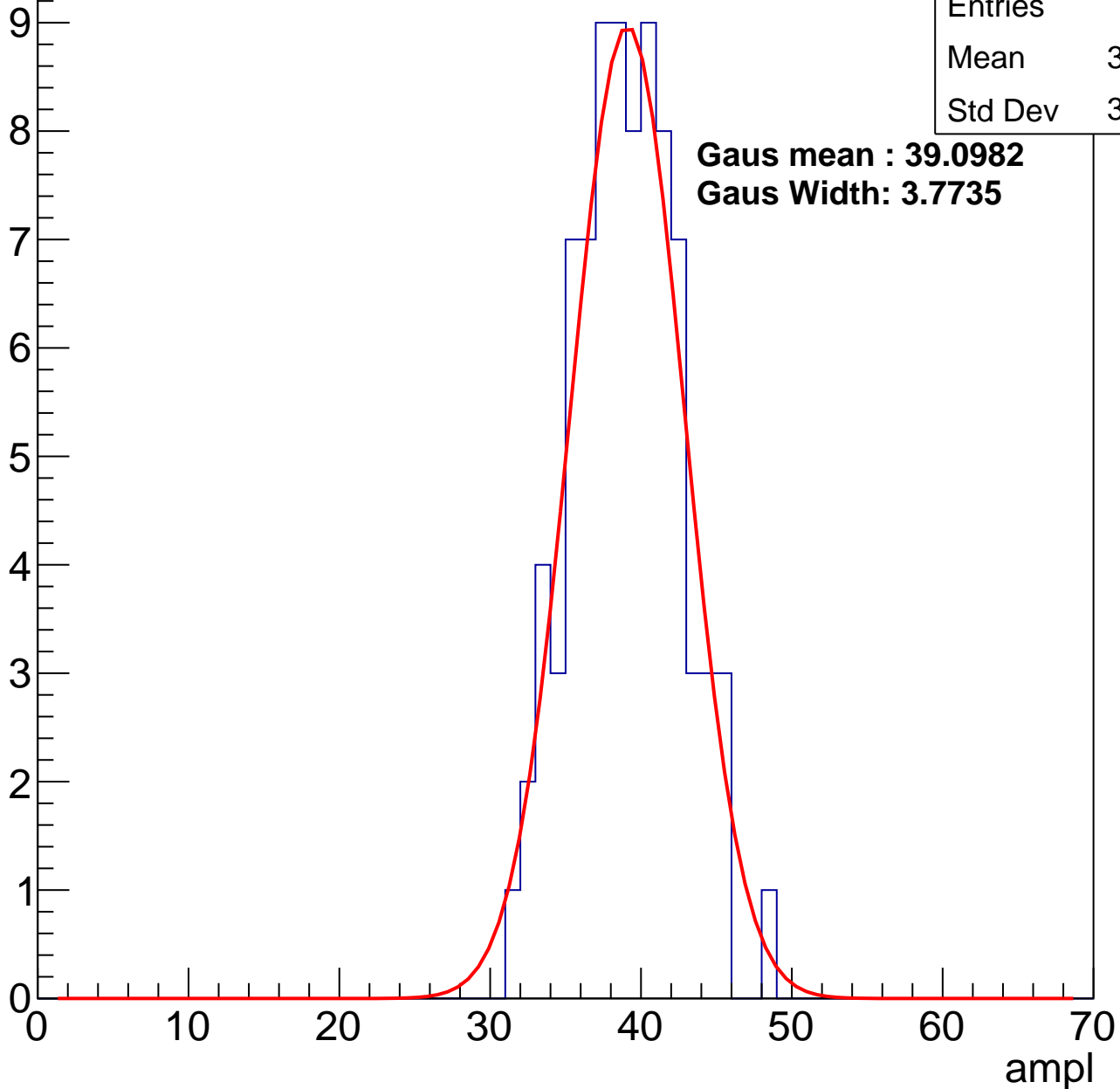
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	84
Mean	38.56
Std Dev	3.452

**Gaus mean : 39.0982**

**Gaus Width: 3.7735**



# B1L003S, U11-ch51, adc2

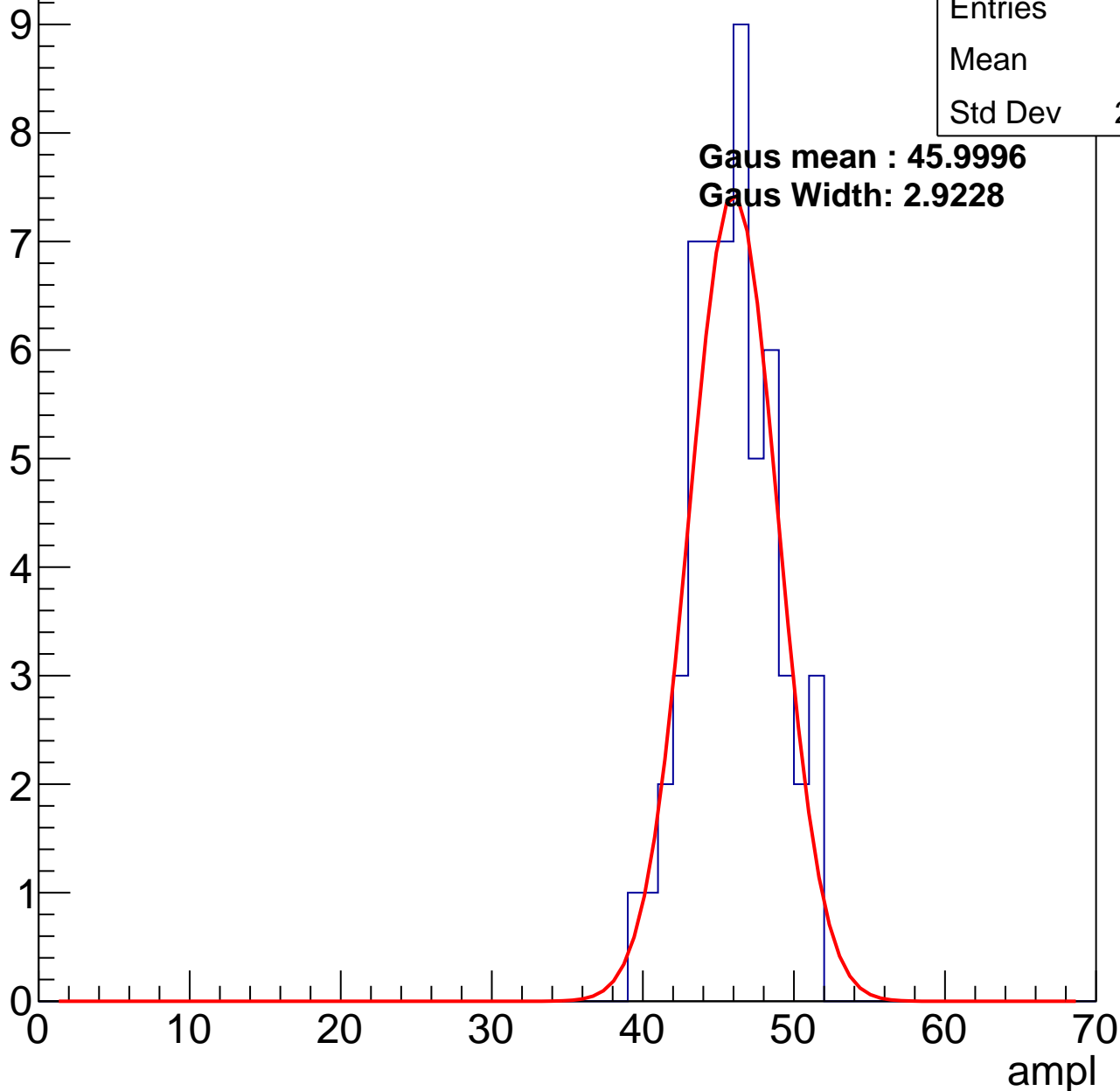
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	45.5
Std Dev	2.771

**Gaus mean : 45.9996**

**Gaus Width: 2.9228**

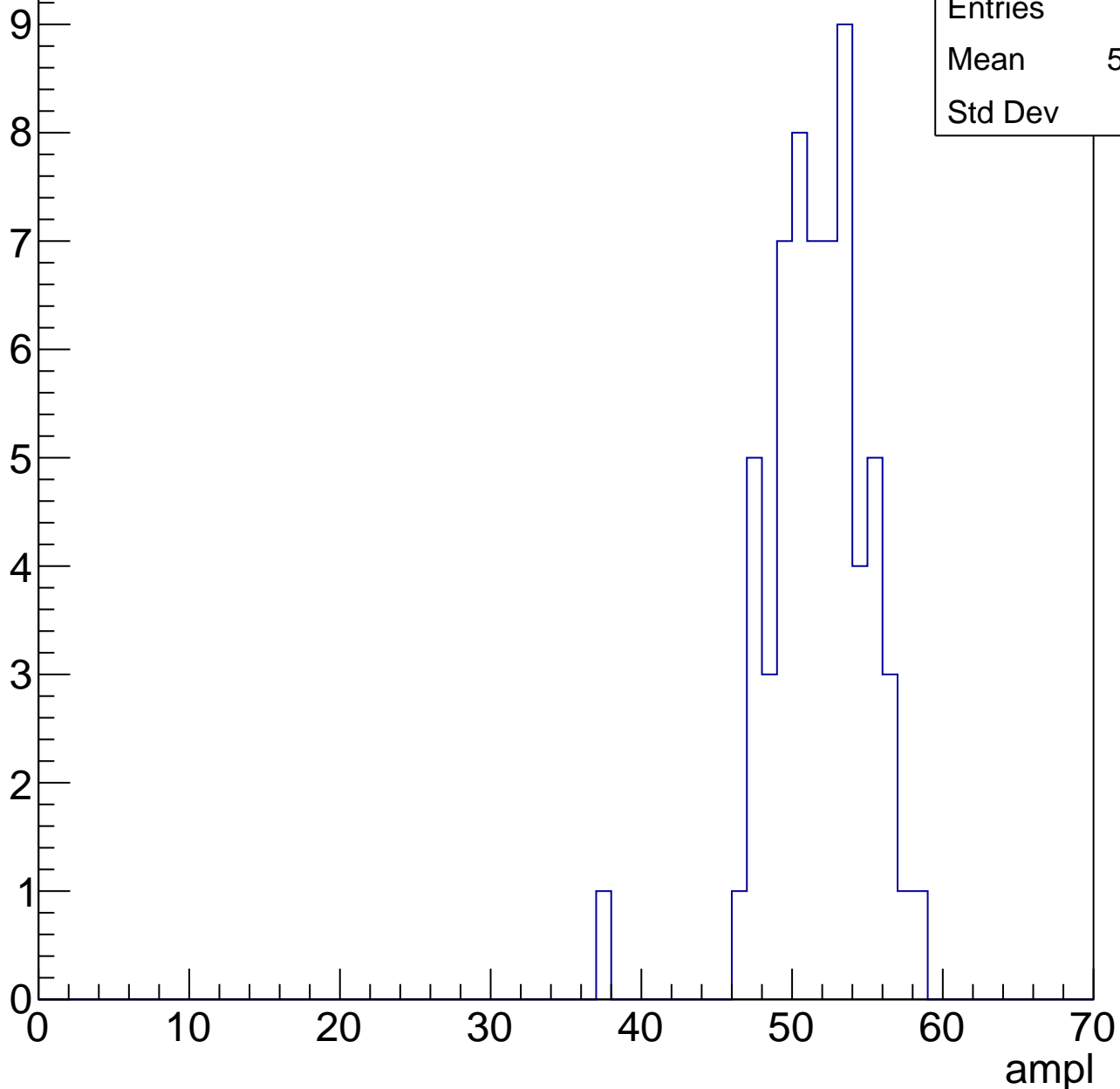


# B1L003S, U11-ch51, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	51.24
Std Dev	3.31

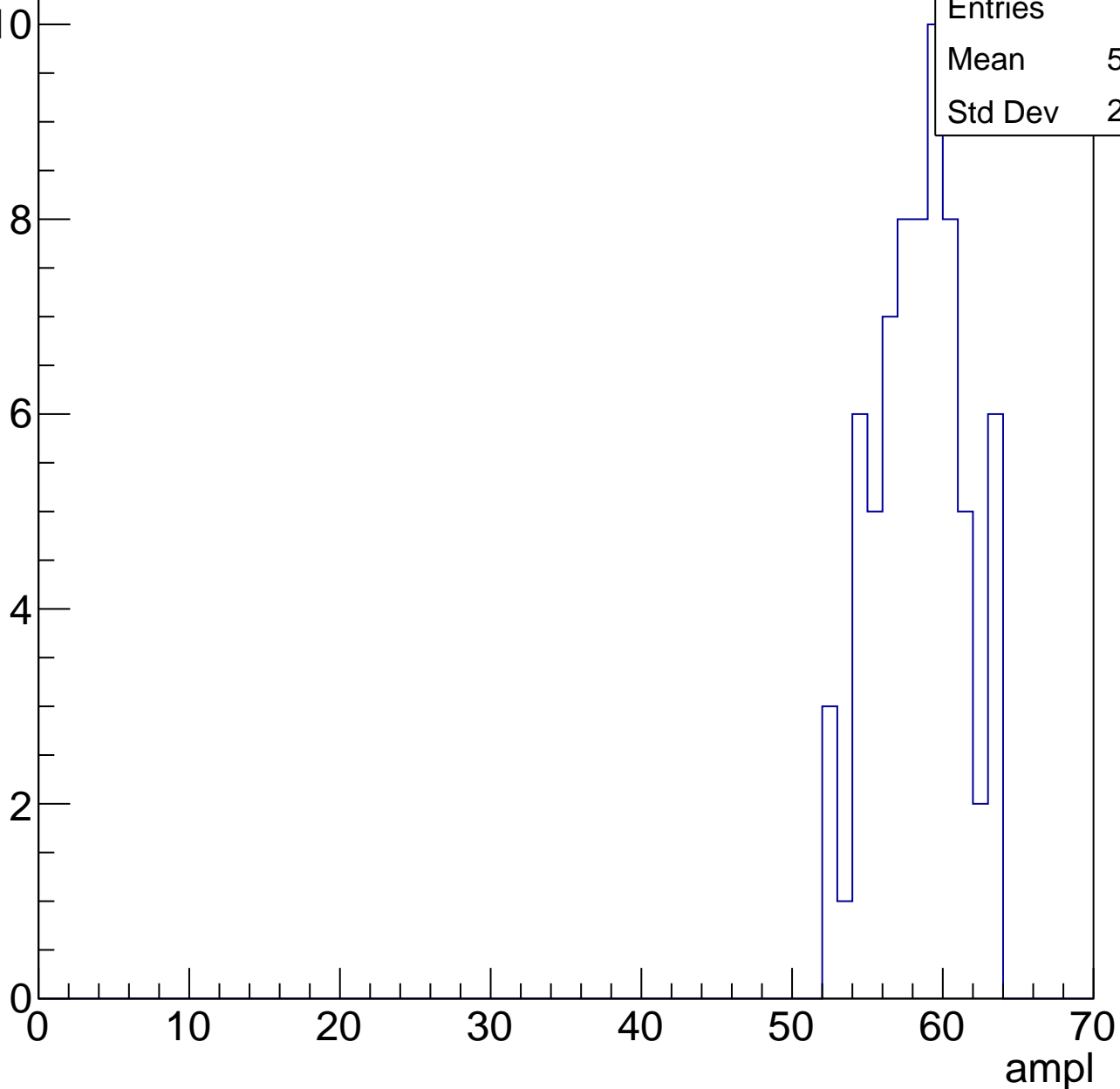


# B1L003S, U11-ch51, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	57.93
Std Dev	2.896

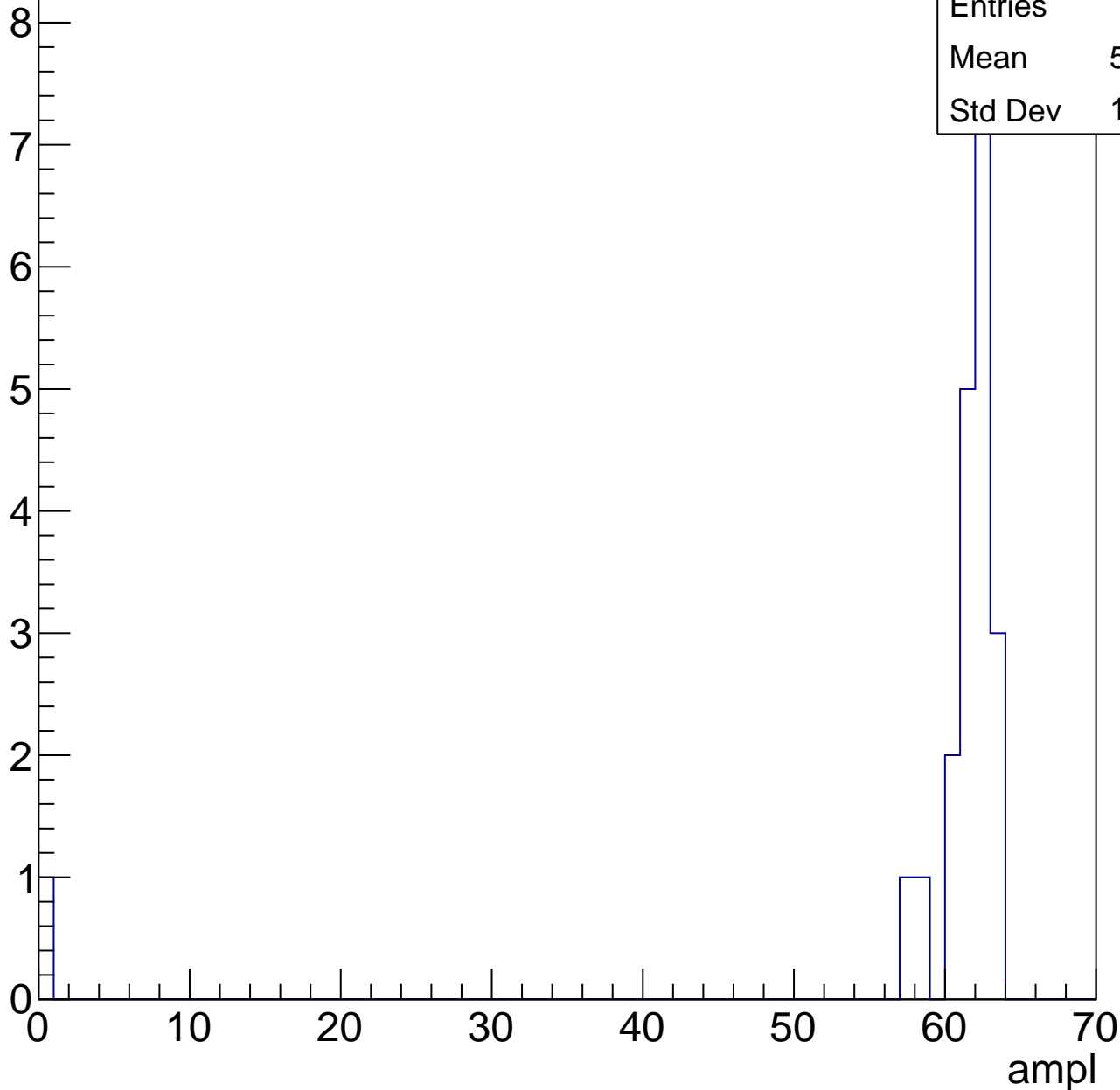


# B1L003S, U11-ch51, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	21
Mean	58.33
Std Dev	13.13



# B1L003S, U11-ch51, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



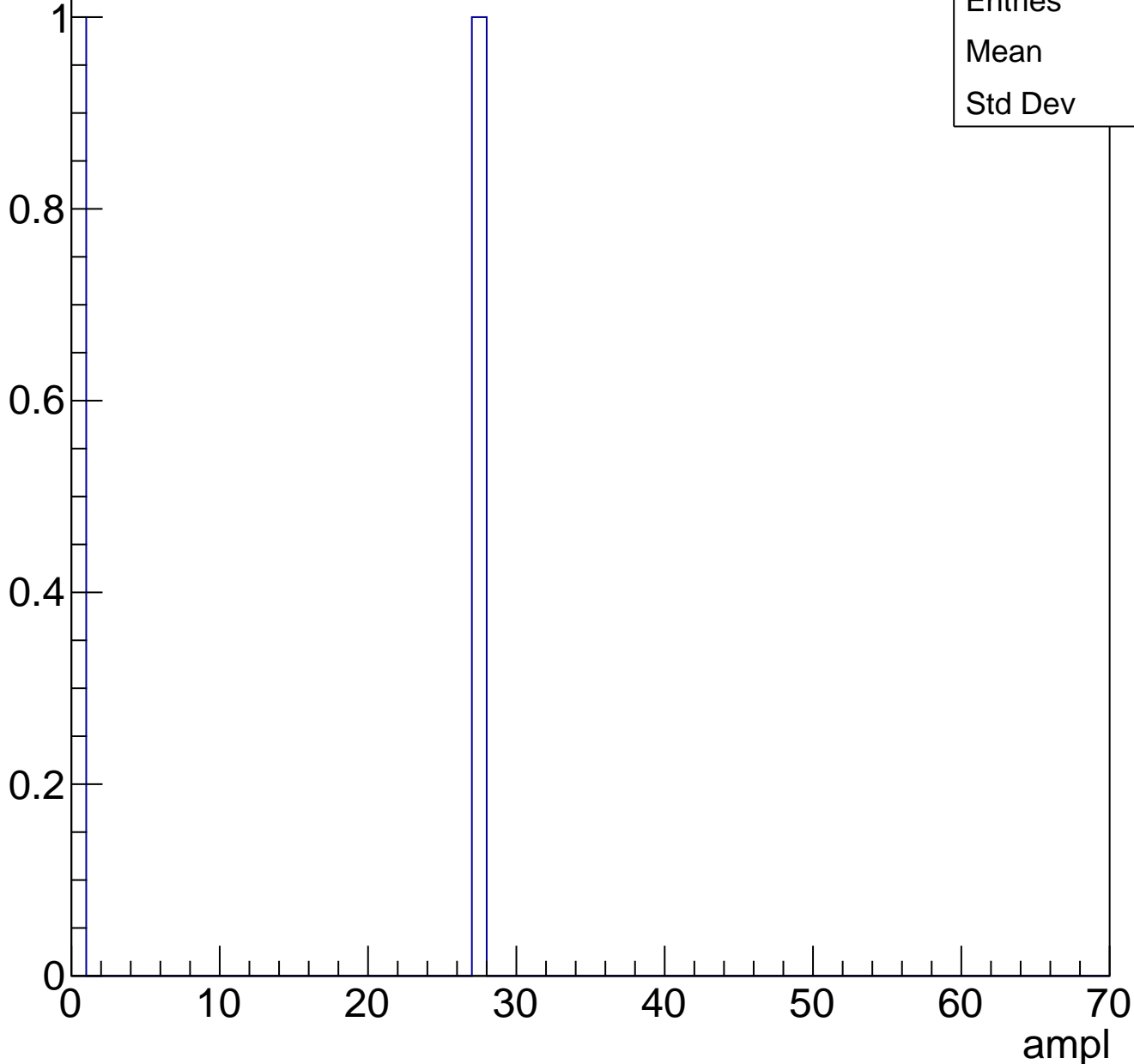
Entries	1
Mean	63
Std Dev	0



# B1L003S, U11-ch51, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	13.5
Std Dev	13.5

# B1L003S, U11-ch52, adc0

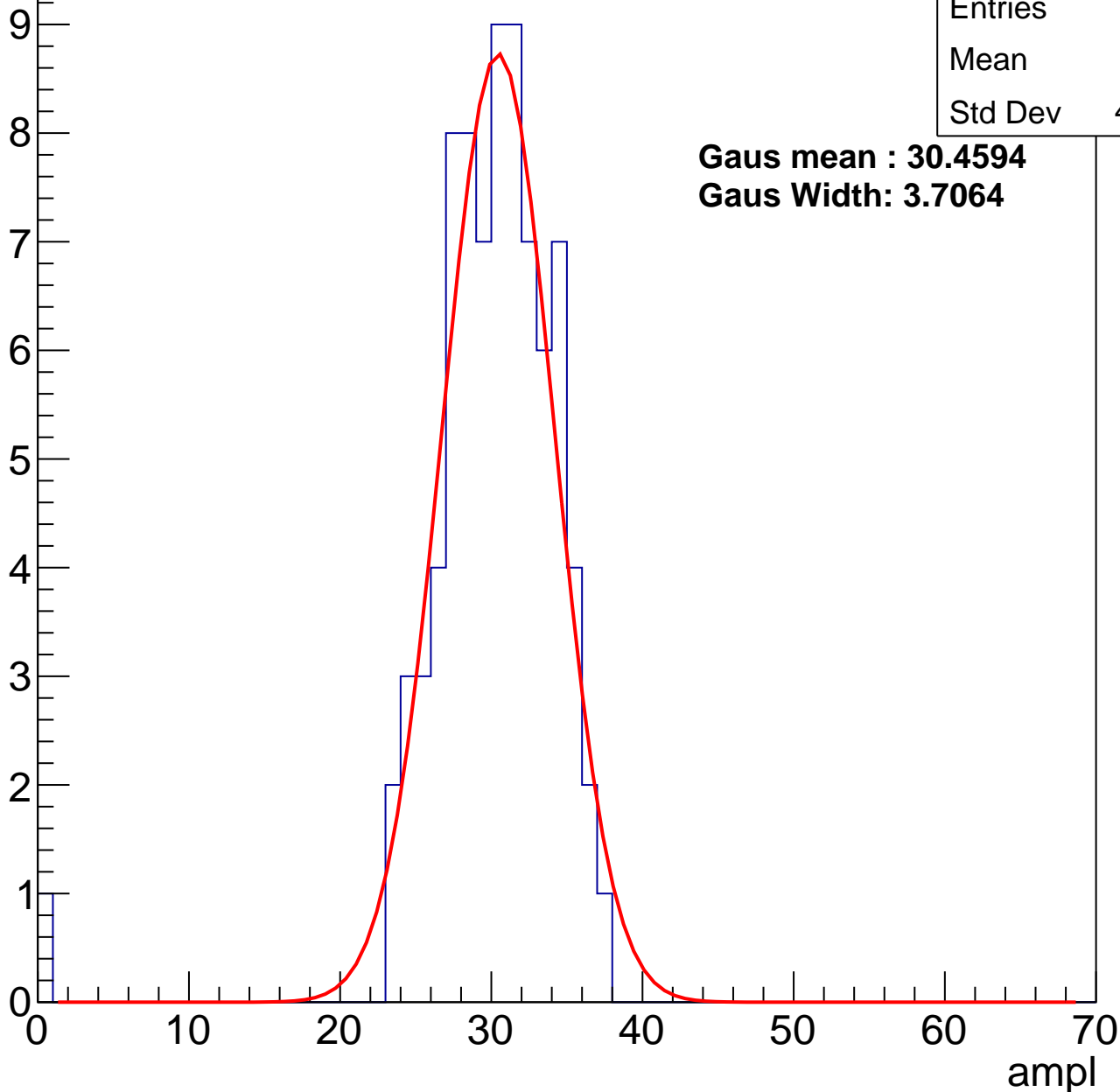
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	81
Mean	29.6
Std Dev	4.671

**Gaus mean : 30.4594**

**Gaus Width: 3.7064**



# B1L003S, U11-ch52, adc1

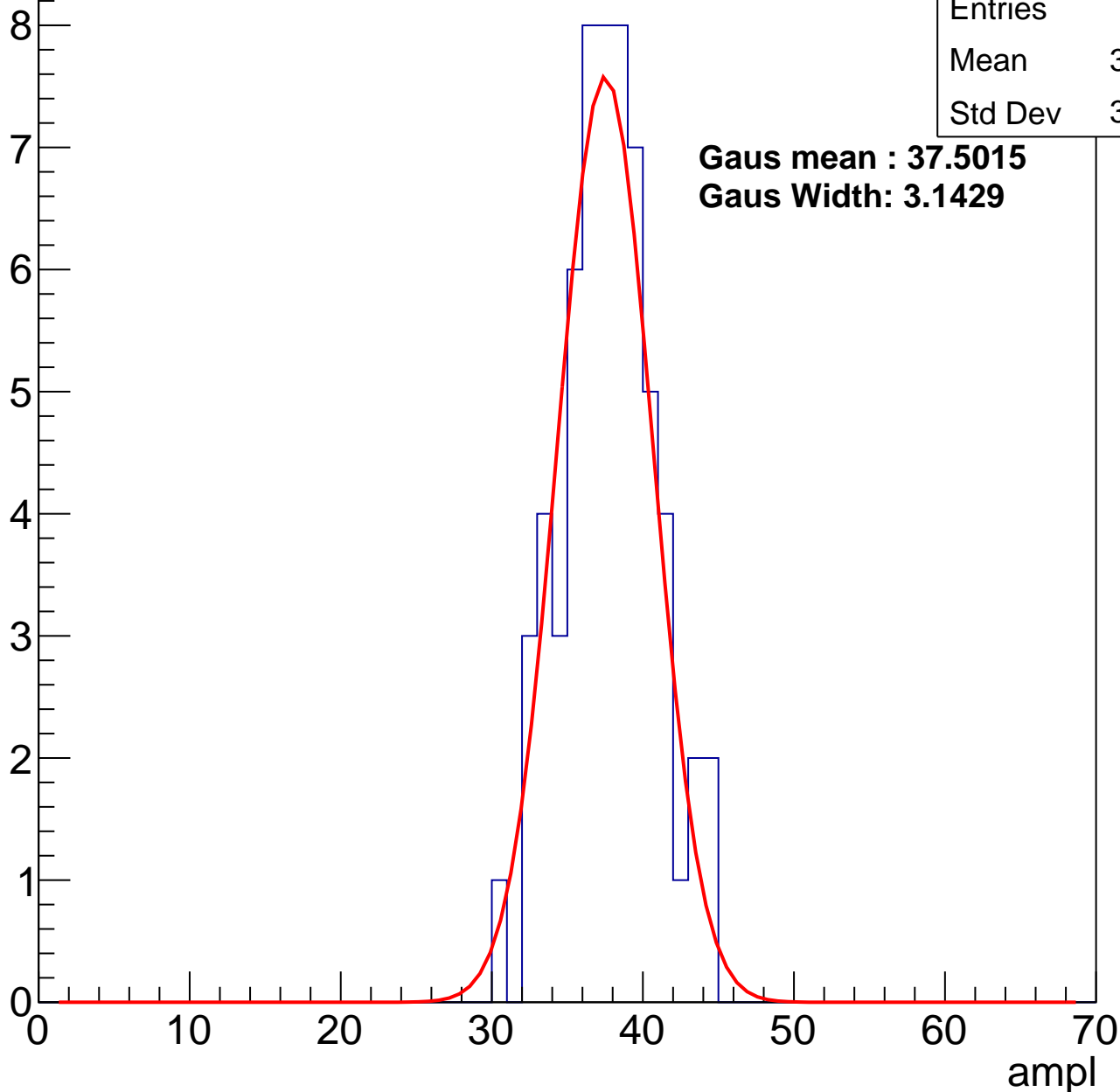
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	37.27
Std Dev	3.065

**Gaus mean : 37.5015**

**Gaus Width: 3.1429**



# B1L003S, U11-ch52, adc2

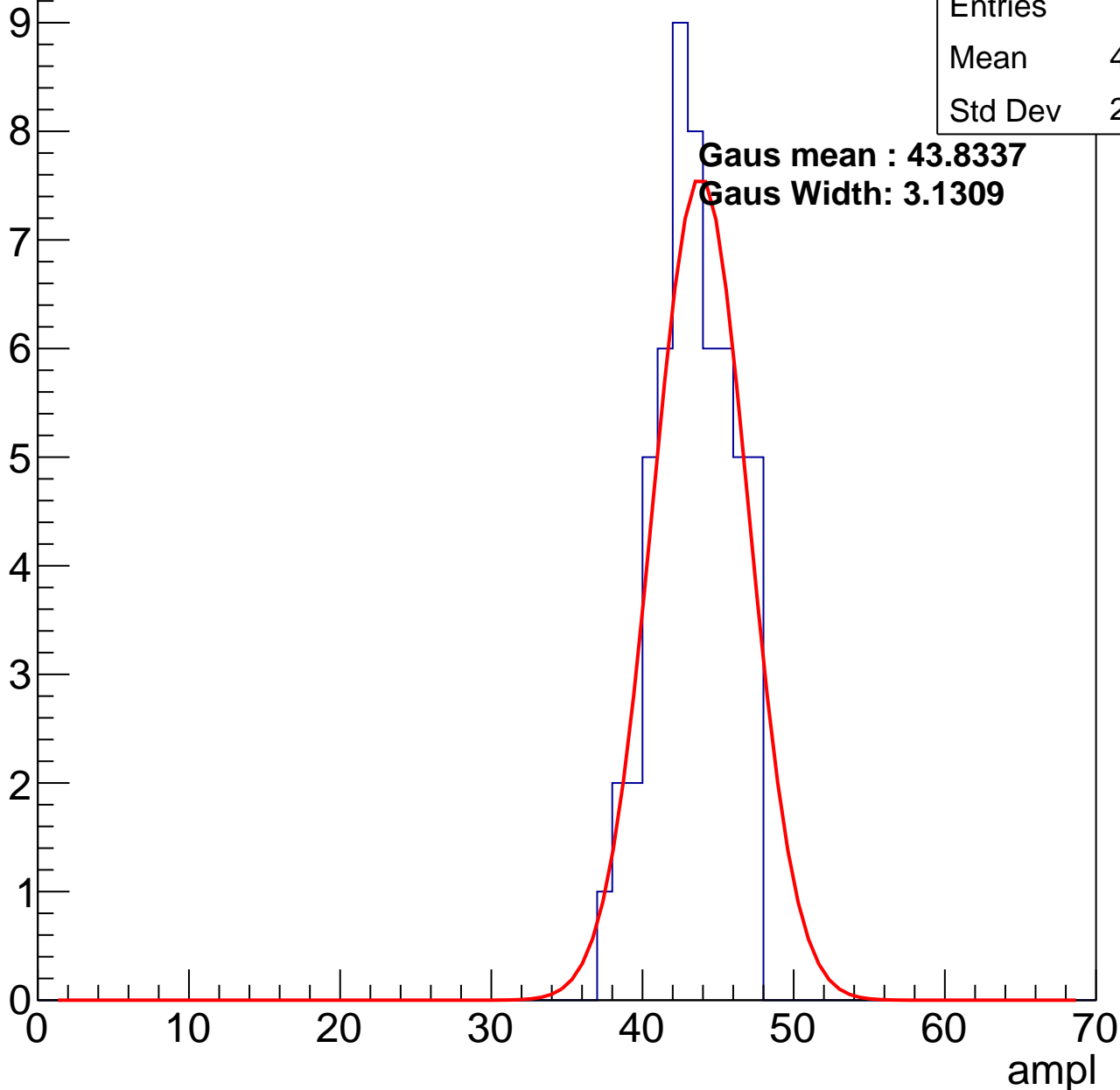
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	42.87
Std Dev	2.523

**Gaus mean : 43.8337**

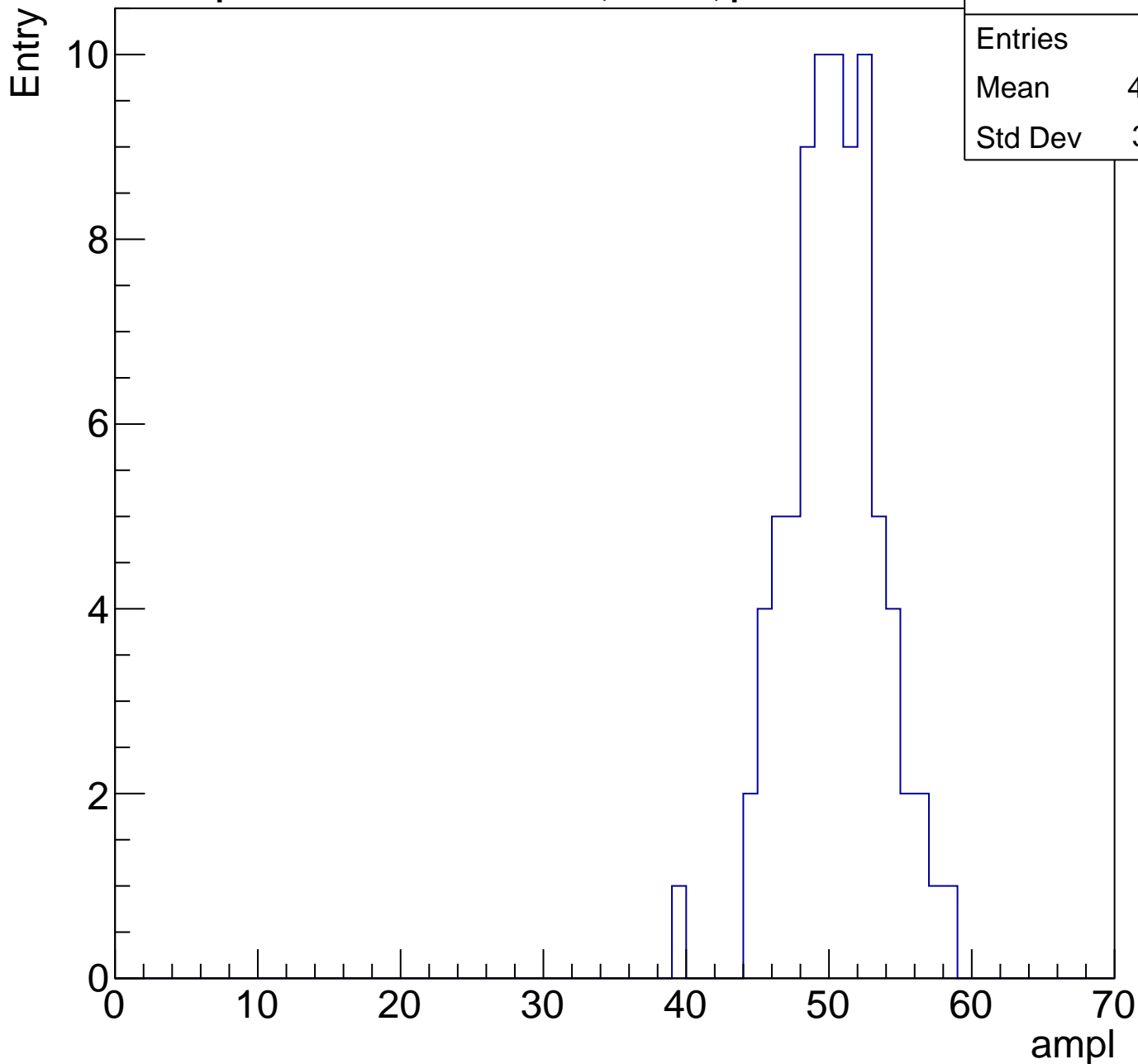
**Gaus Width: 3.1309**



# B1L003S, U11-ch52, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	80
Mean	49.89
Std Dev	3.271

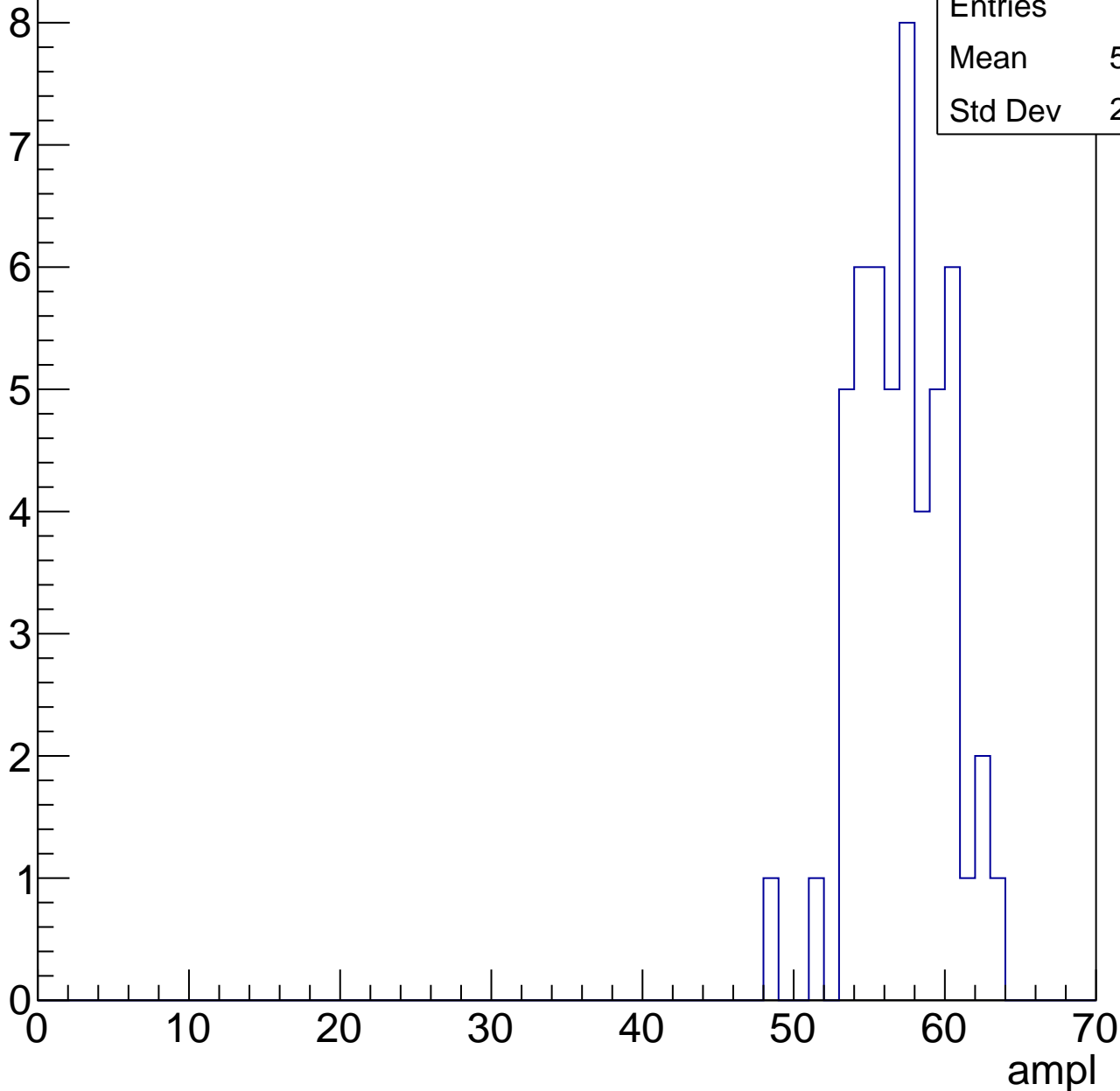


# B1L003S, U11-ch52, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

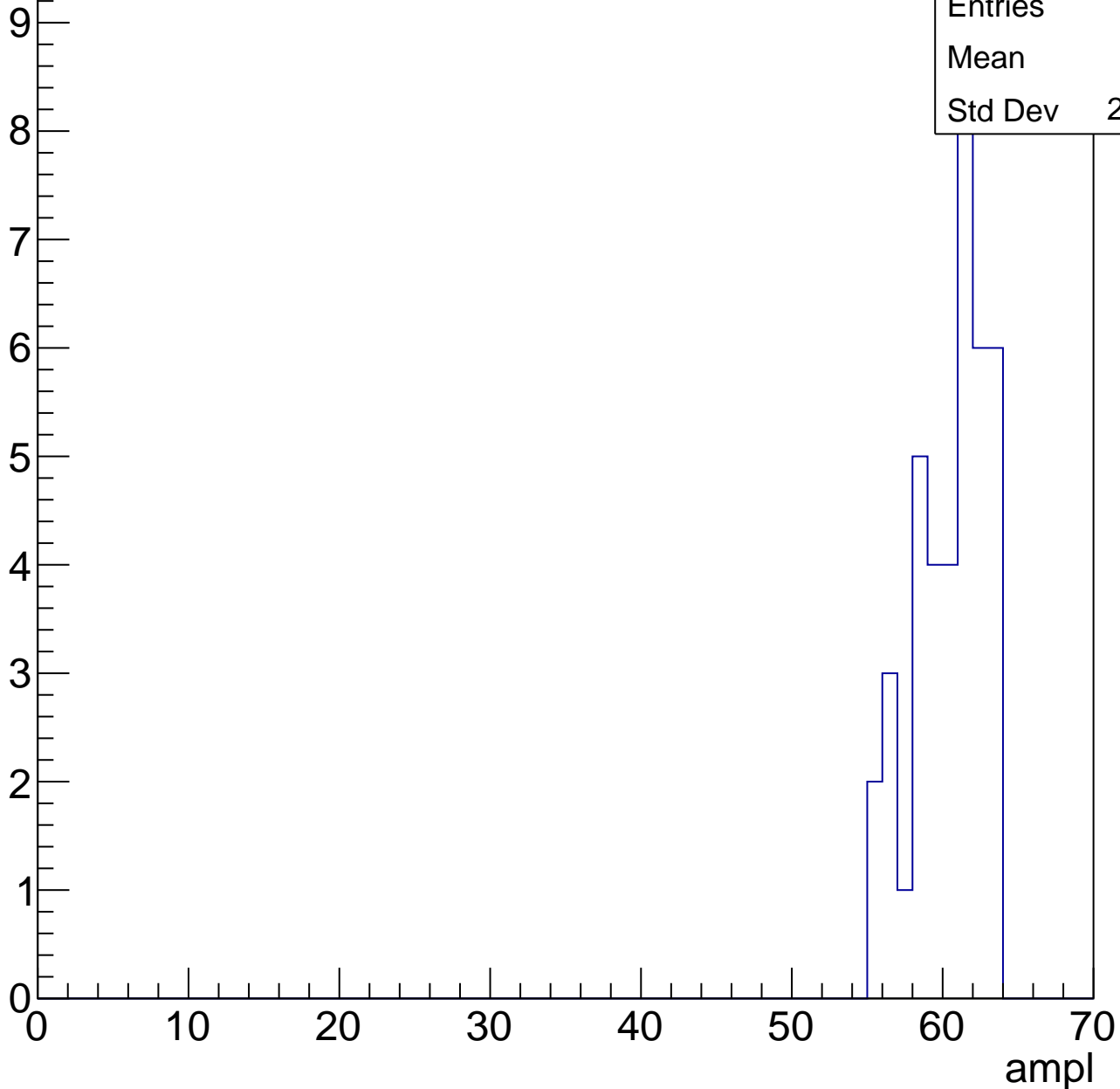
Entries	51
Mean	56.65
Std Dev	2.982



# B1L003S, U11-ch52, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

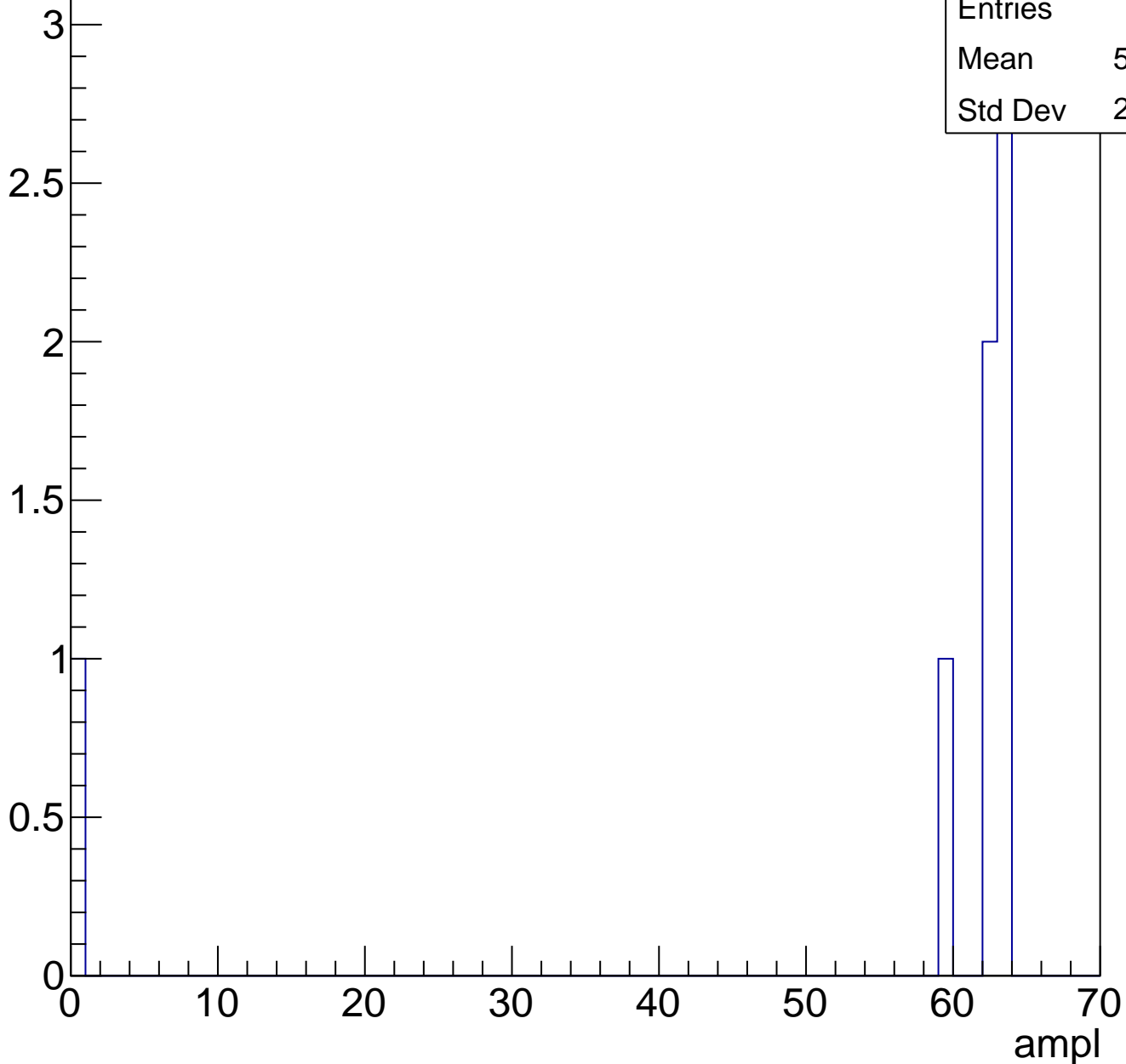
Entry



# B1L003S, U11-ch52, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch52, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L003S, U11-ch53, adc0

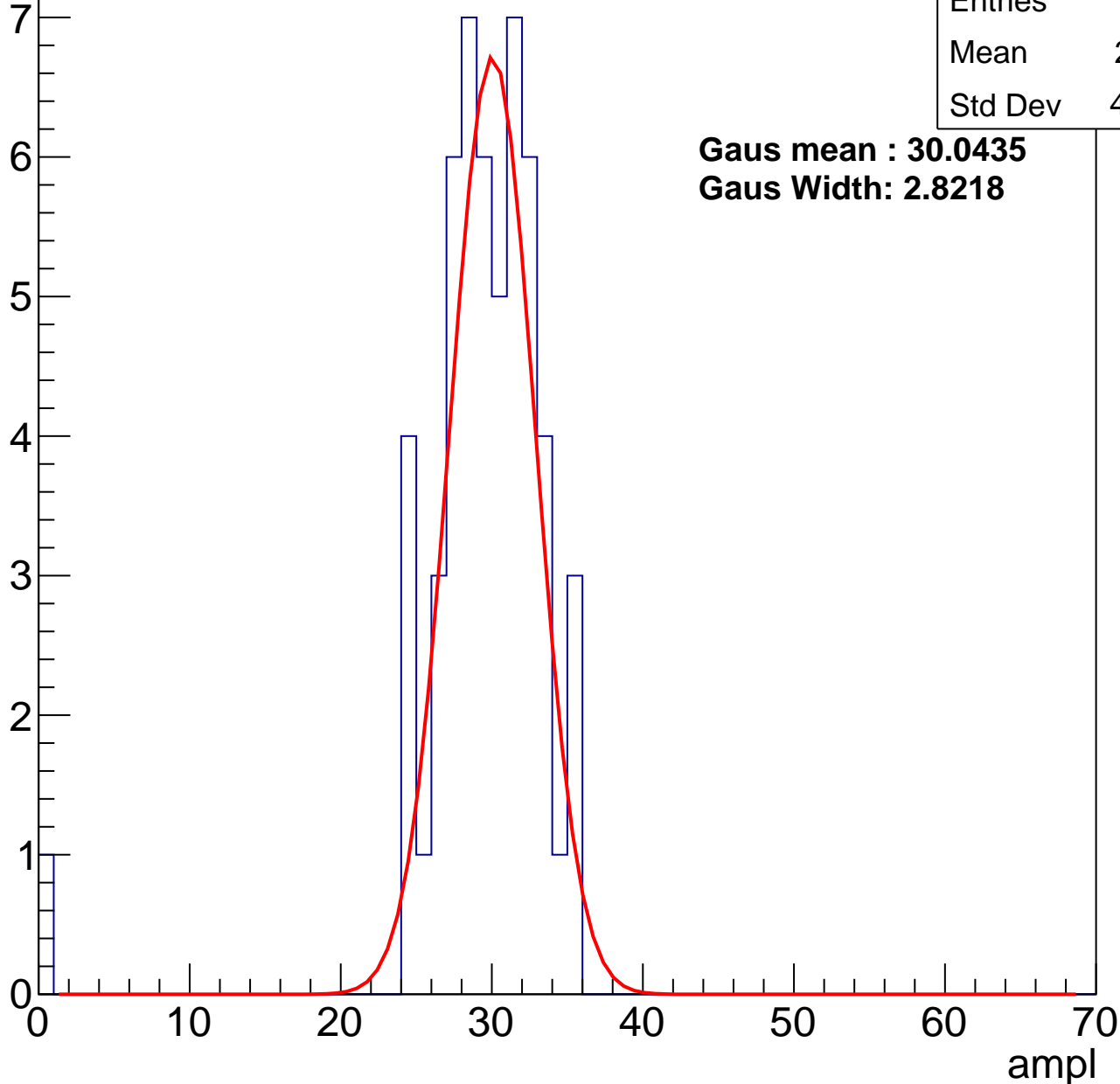
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	54
Mean	28.91
Std Dev	4.904

**Gaus mean : 30.0435**

**Gaus Width: 2.8218**



# B1L003S, U11-ch53, adc1

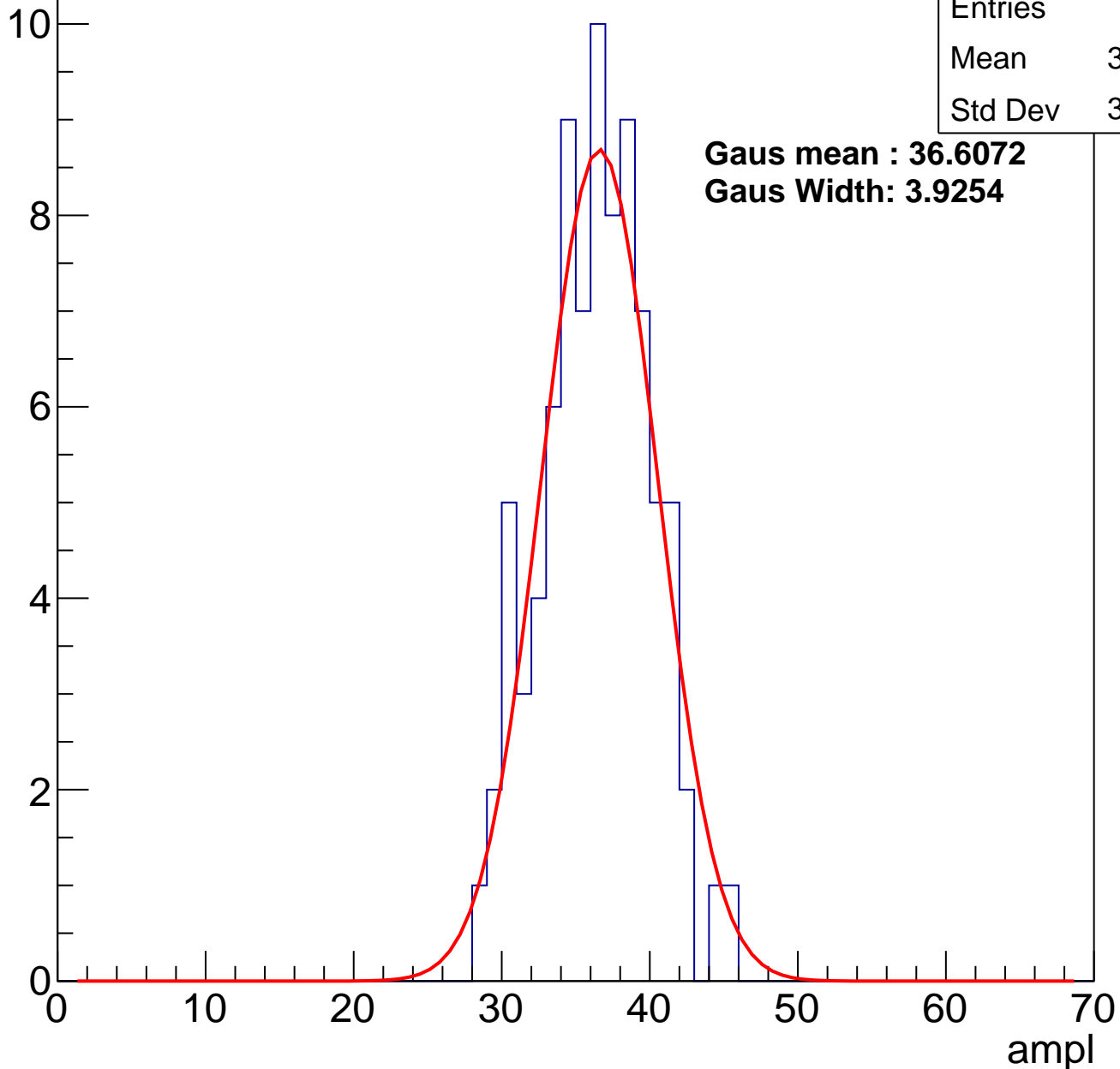
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	85
Mean	35.94
Std Dev	3.608

**Gaus mean : 36.6072**

**Gaus Width: 3.9254**

Entry



# B1L003S, U11-ch53, adc2

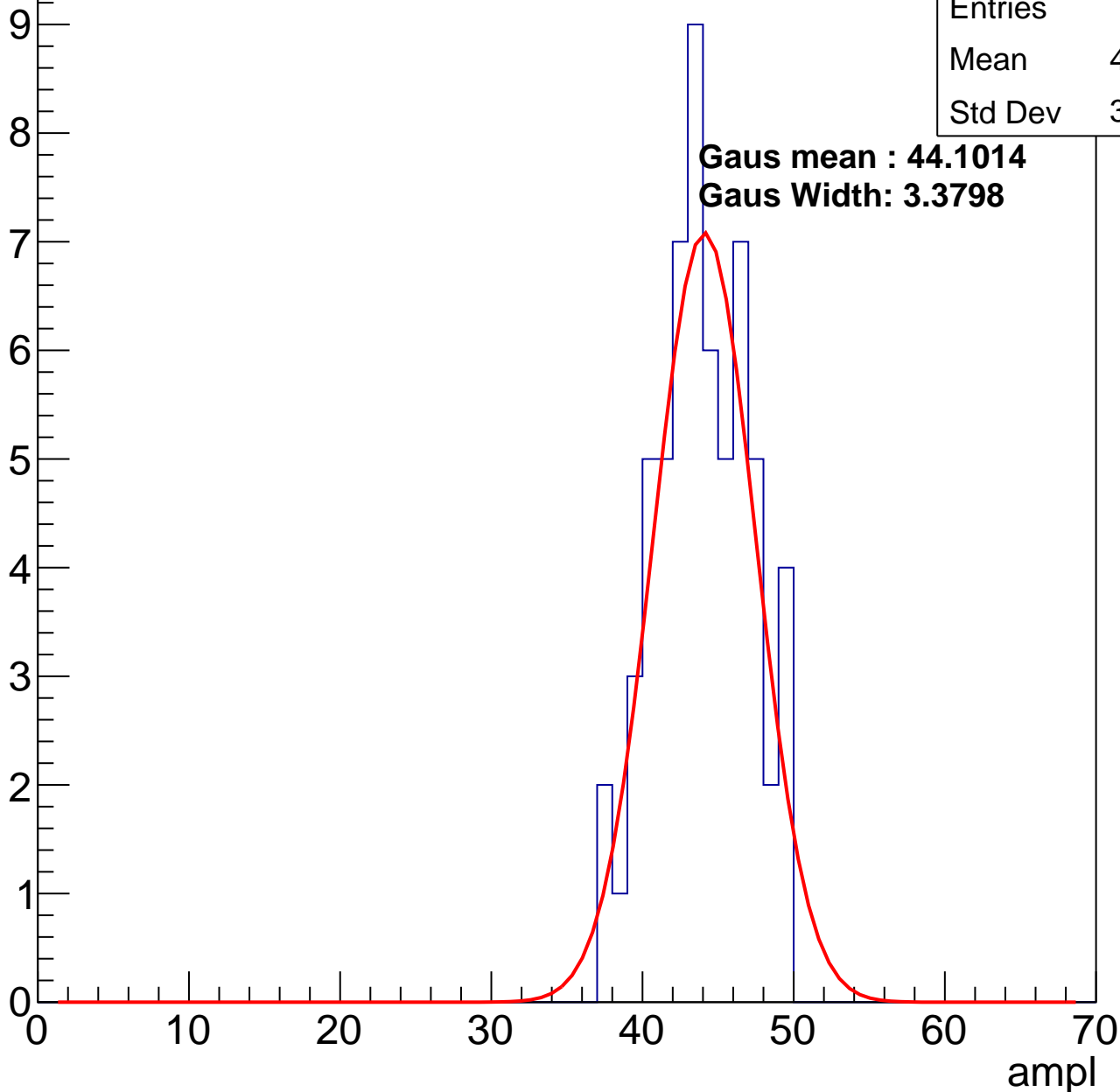
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	43.49
Std Dev	3.044

**Gaus mean : 44.1014**

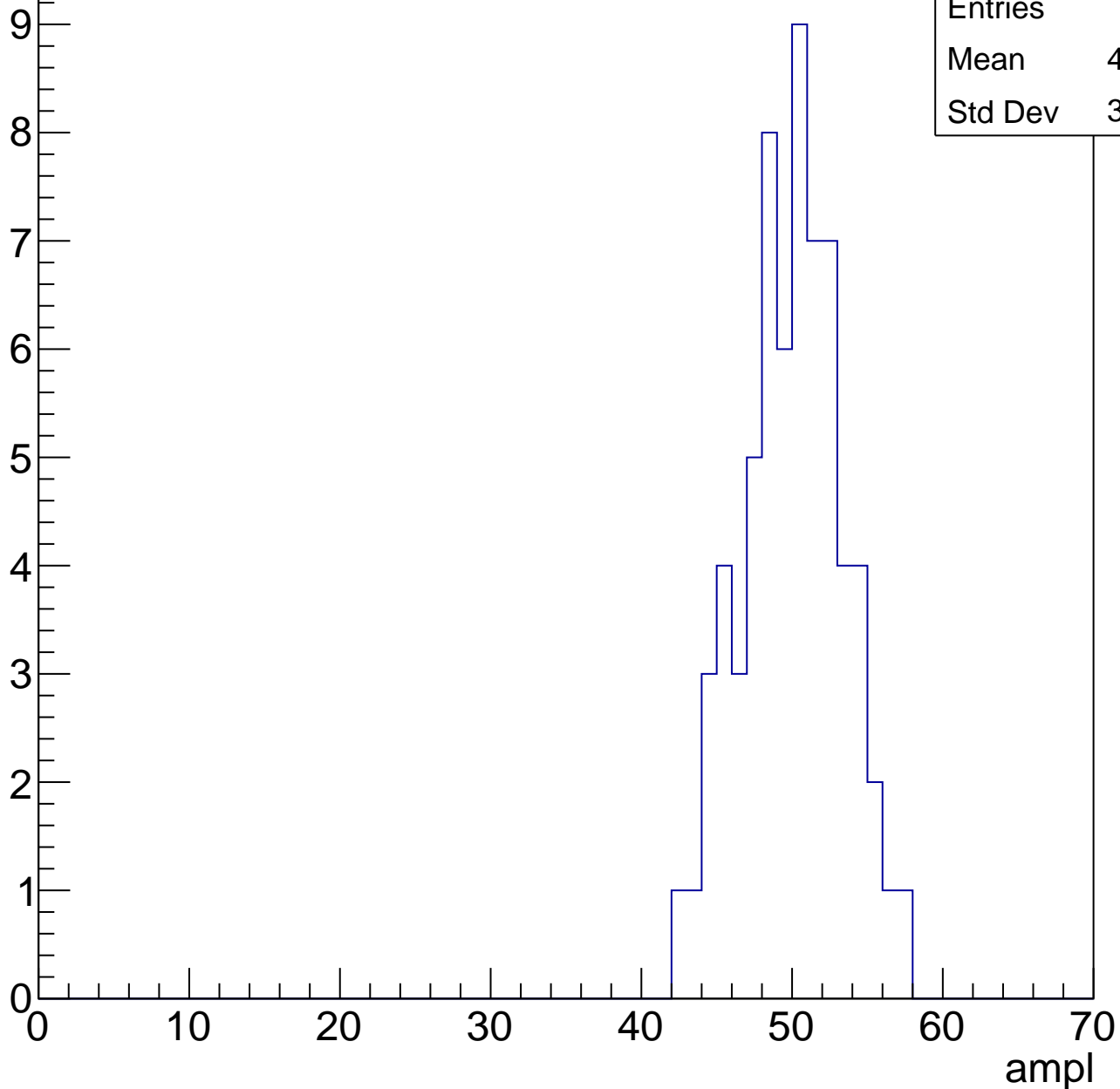
**Gaus Width: 3.3798**



# B1L003S, U11-ch53, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

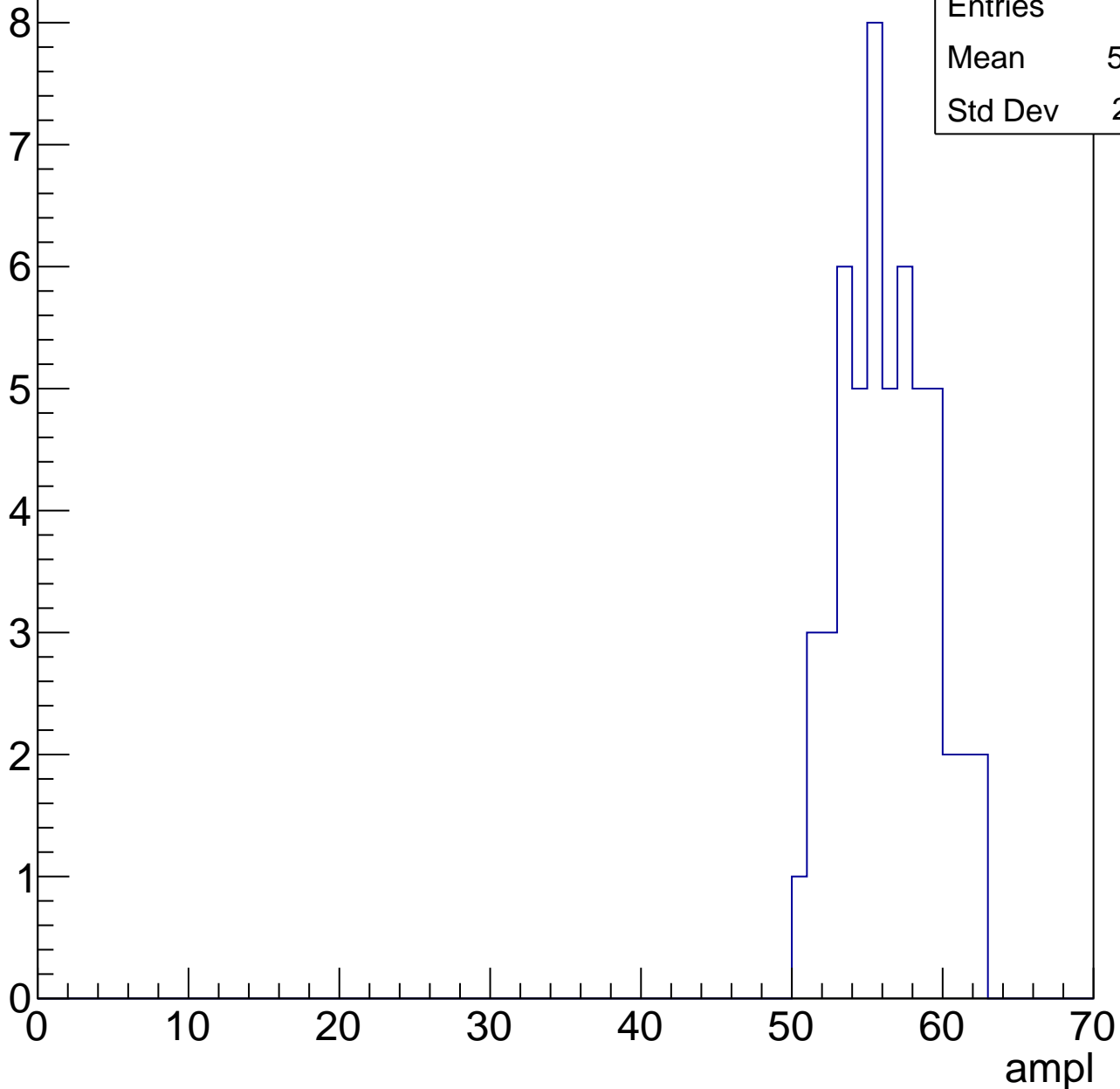


# B1L003S, U11-ch53, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	55.85
Std Dev	2.961



# B1L003S, U11-ch53, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

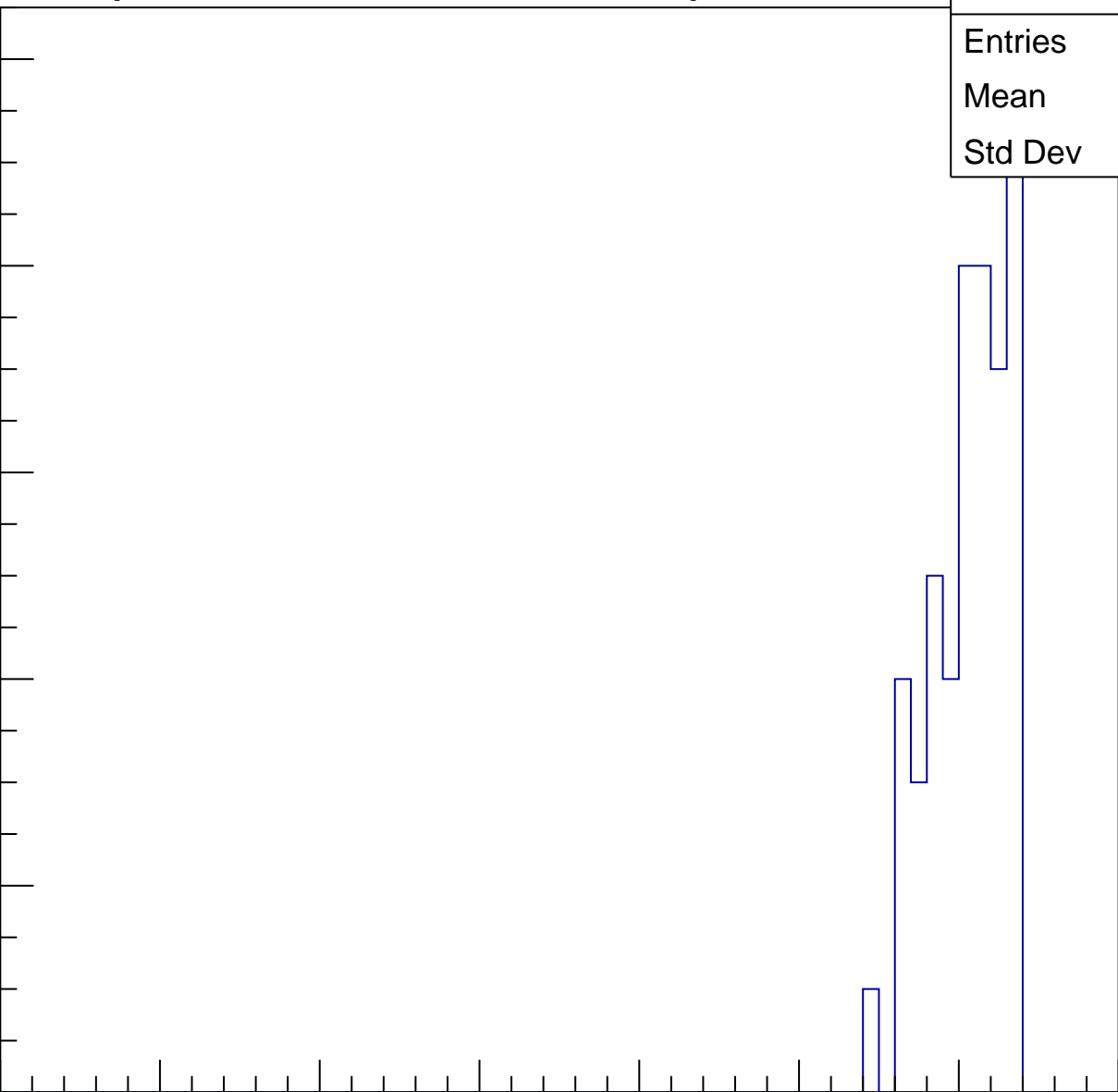
Entries	50
Mean	60.14
Std Dev	2.35

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

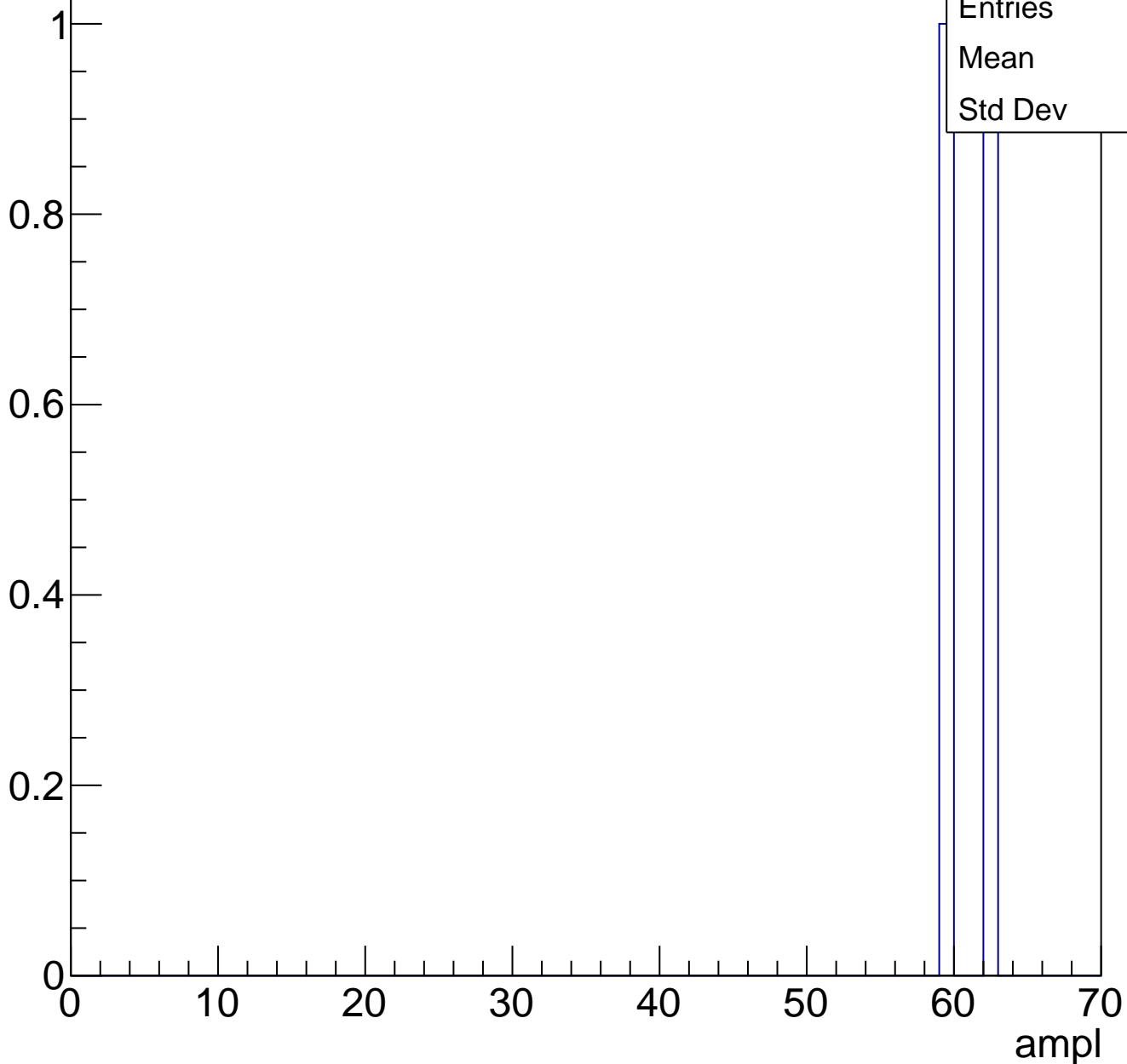
ampl



# B1L003S, U11-ch53, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch53, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L003S, U11-ch54, adc0

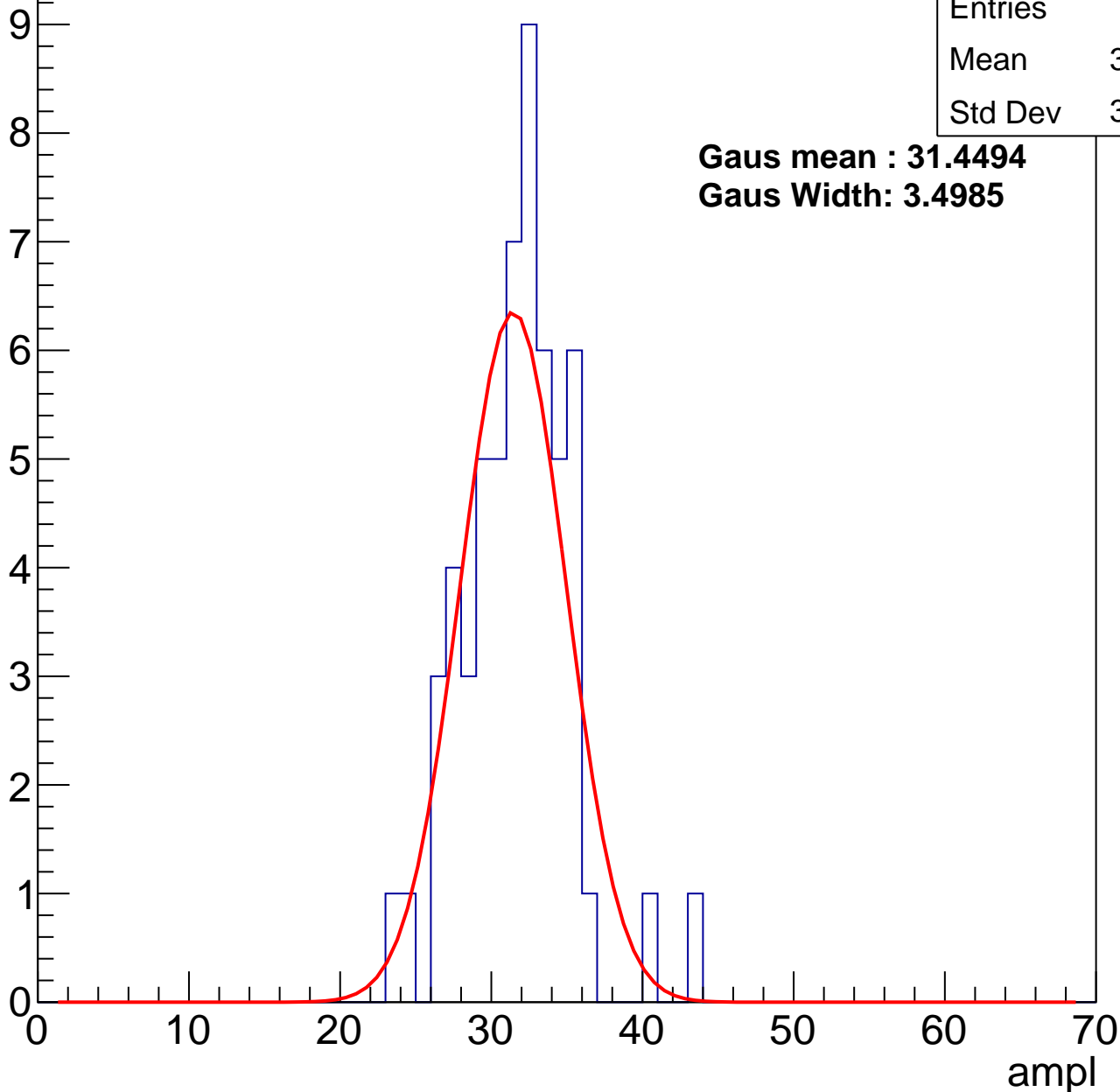
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	31.28
Std Dev	3.532

**Gaus mean : 31.4494**

**Gaus Width: 3.4985**



# B1L003S, U11-ch54, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	70
Mean	37.3
Std Dev	3.502

**Gaus mean : 37.7862**

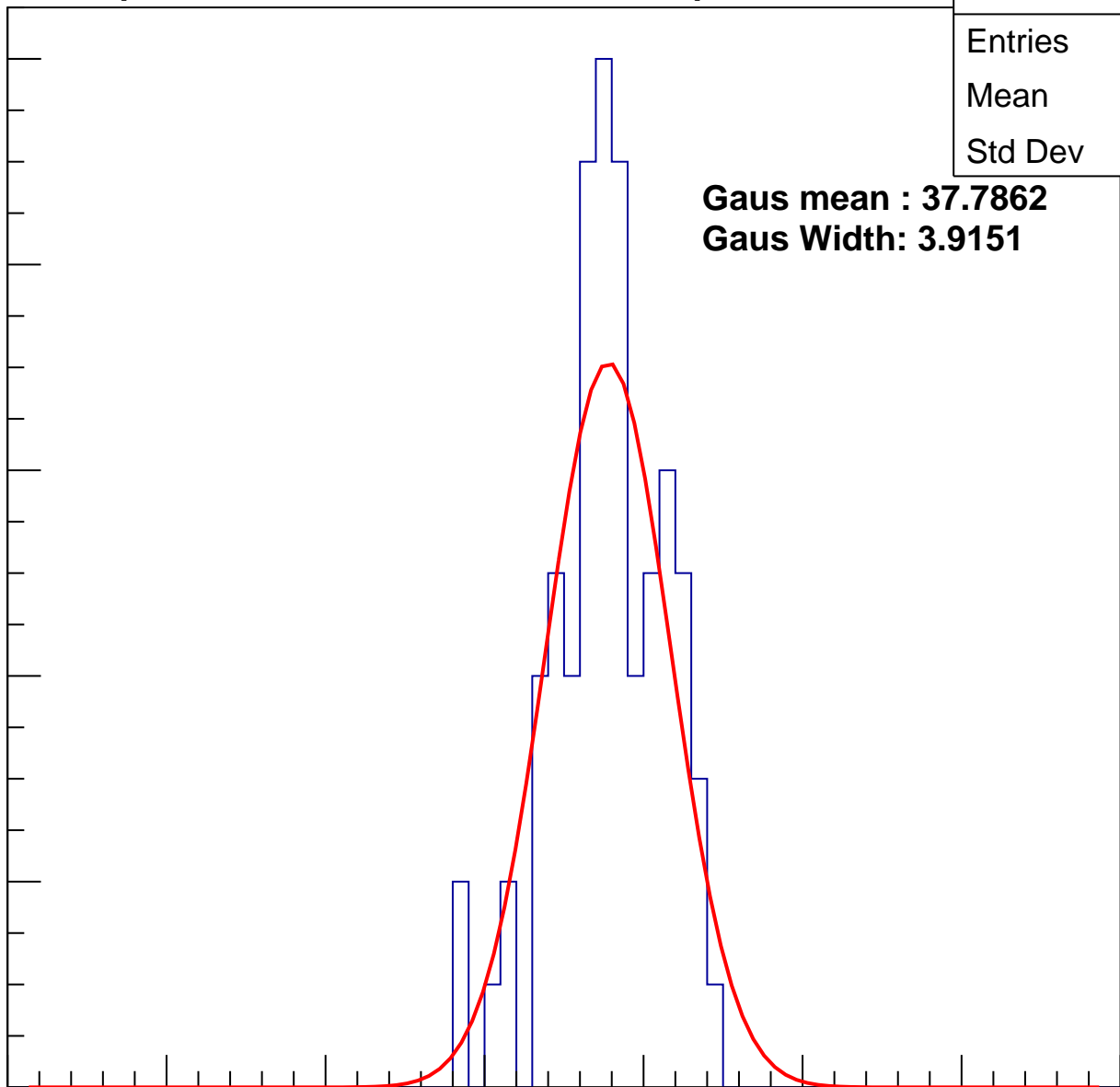
**Gaus Width: 3.9151**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U11-ch54, adc2

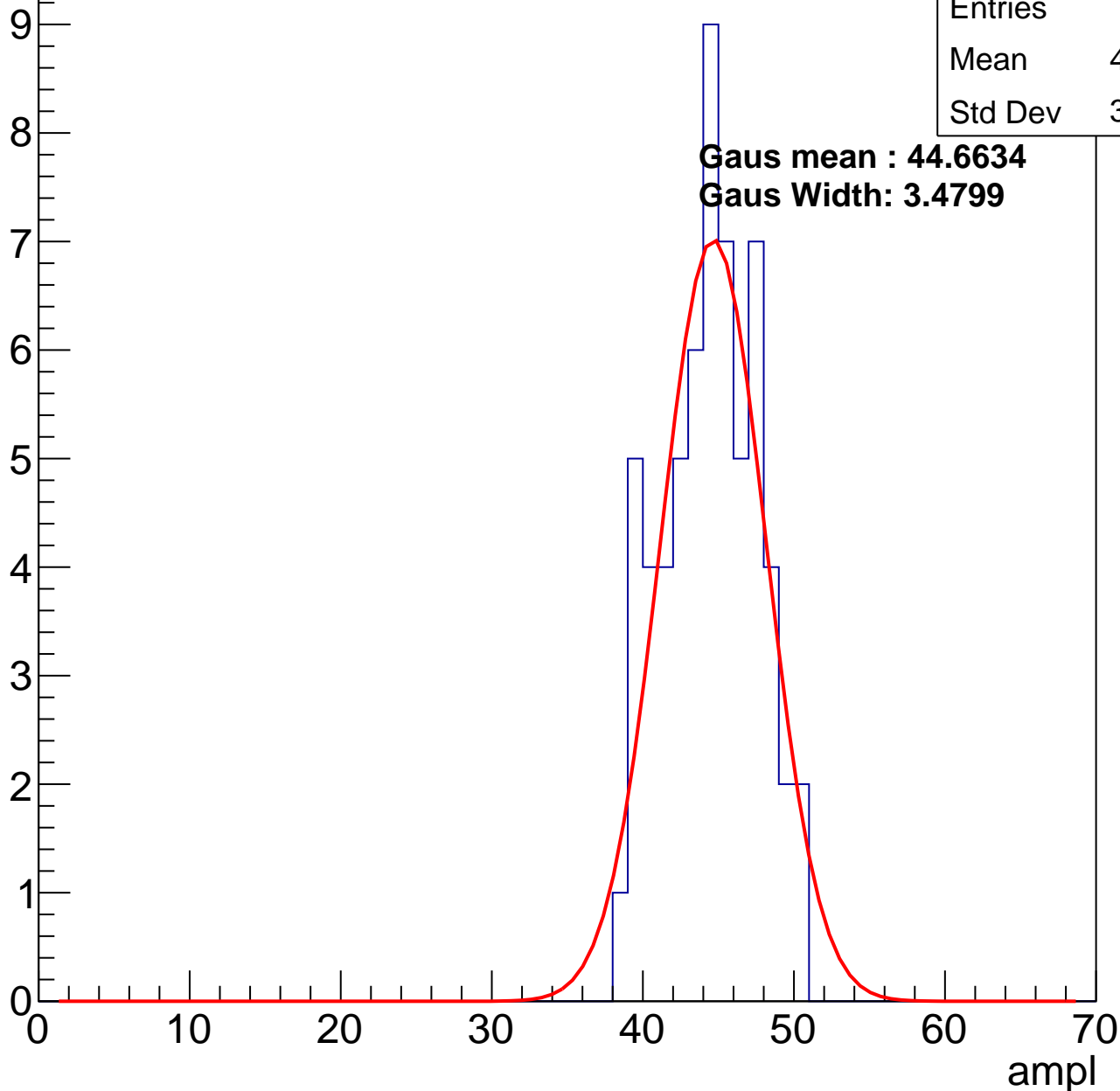
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	44.02
Std Dev	3.038

**Gaus mean : 44.6634**

**Gaus Width: 3.4799**

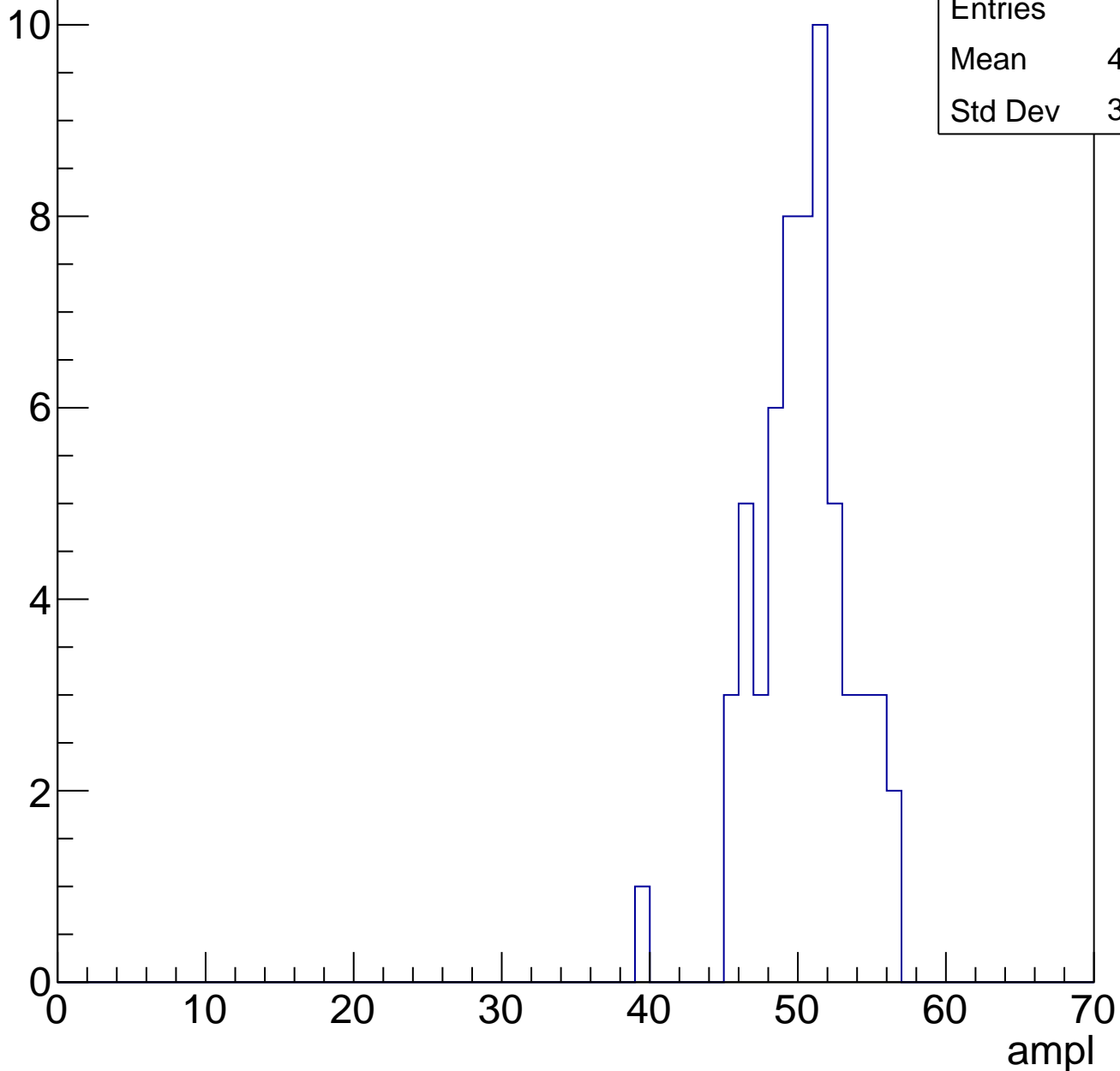


# B1L003S, U11-ch54, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	60
Mean	49.88
Std Dev	3.126

Entry

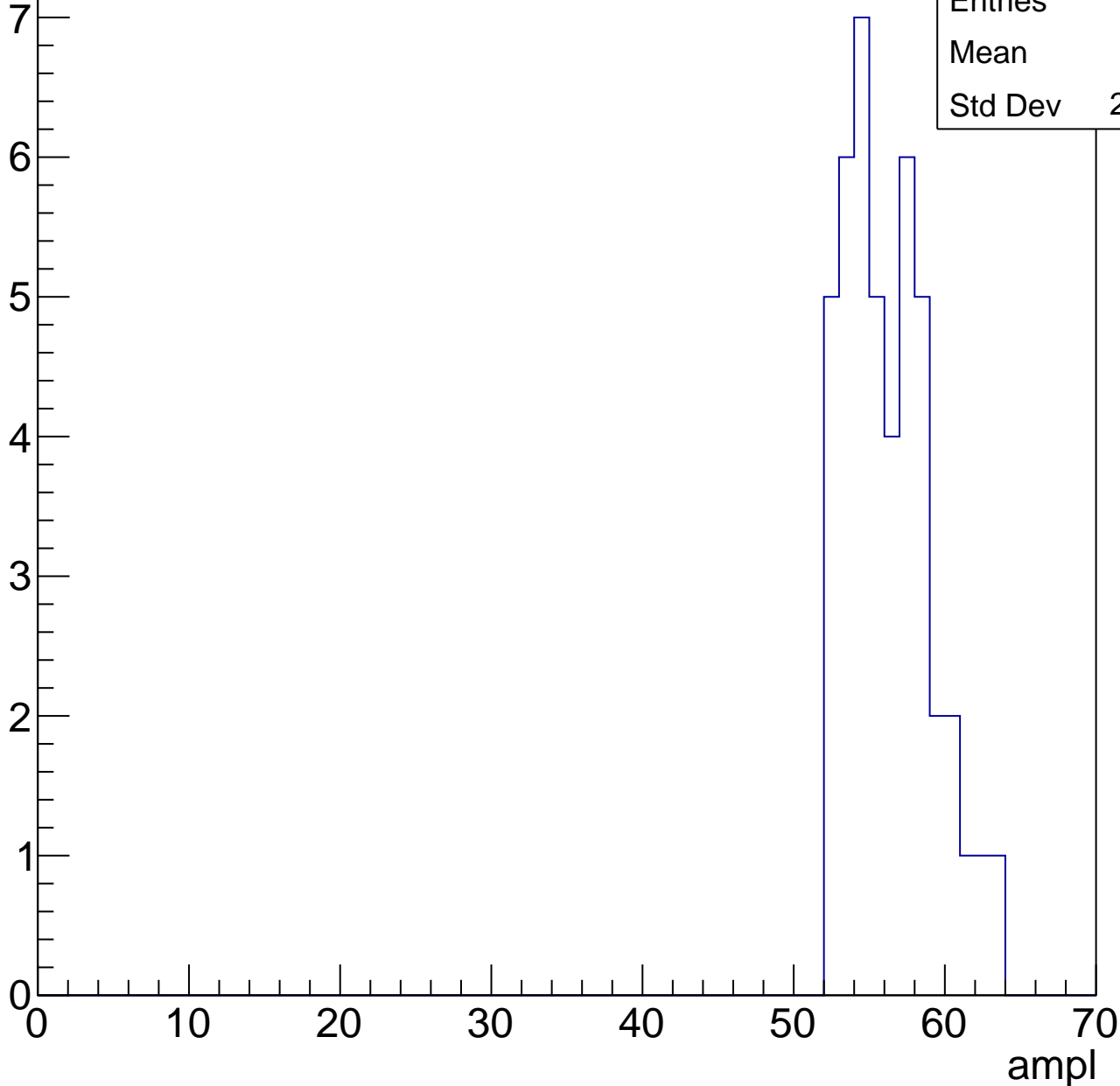


# B1L003S, U11-ch54, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	45
Mean	55.8
Std Dev	2.794

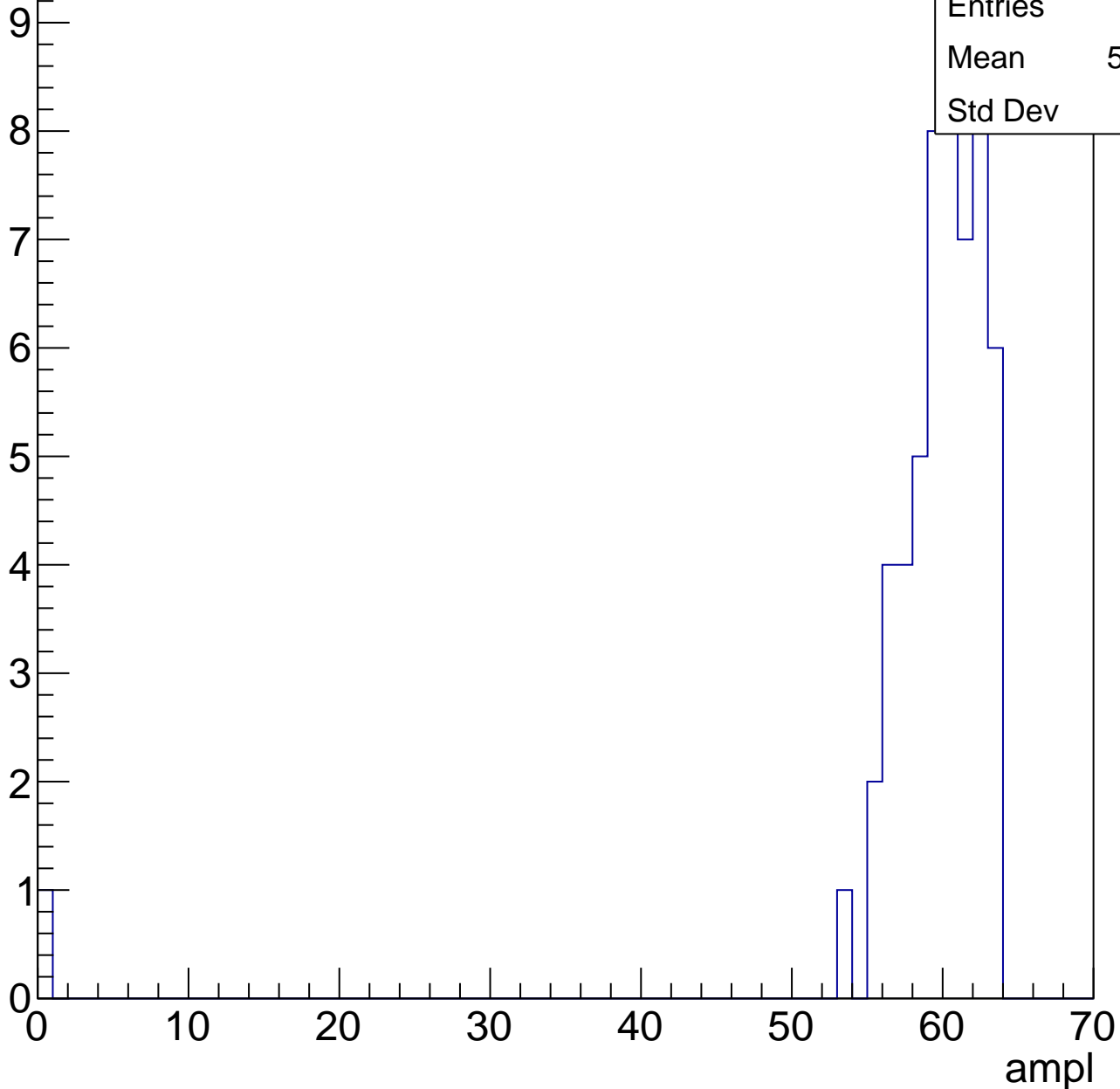


# B1L003S, U11-ch54, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	58.55
Std Dev	8.32



# B1L003S, U11-ch54, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch54, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U11-ch55, adc0

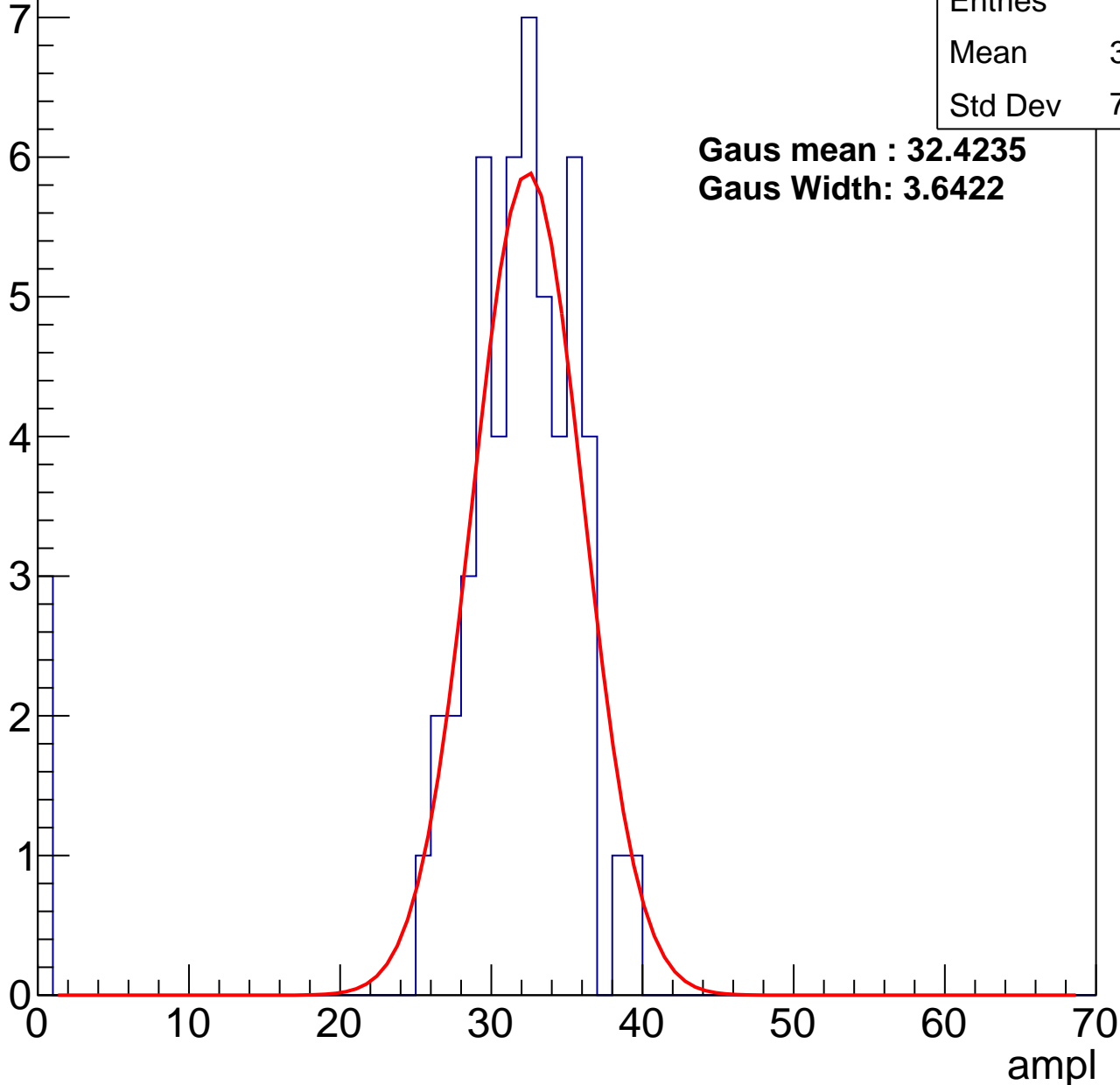
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	30.02
Std Dev	7.833

**Gaus mean : 32.4235**

**Gaus Width: 3.6422**



# B1L003S, U11-ch55, adc1

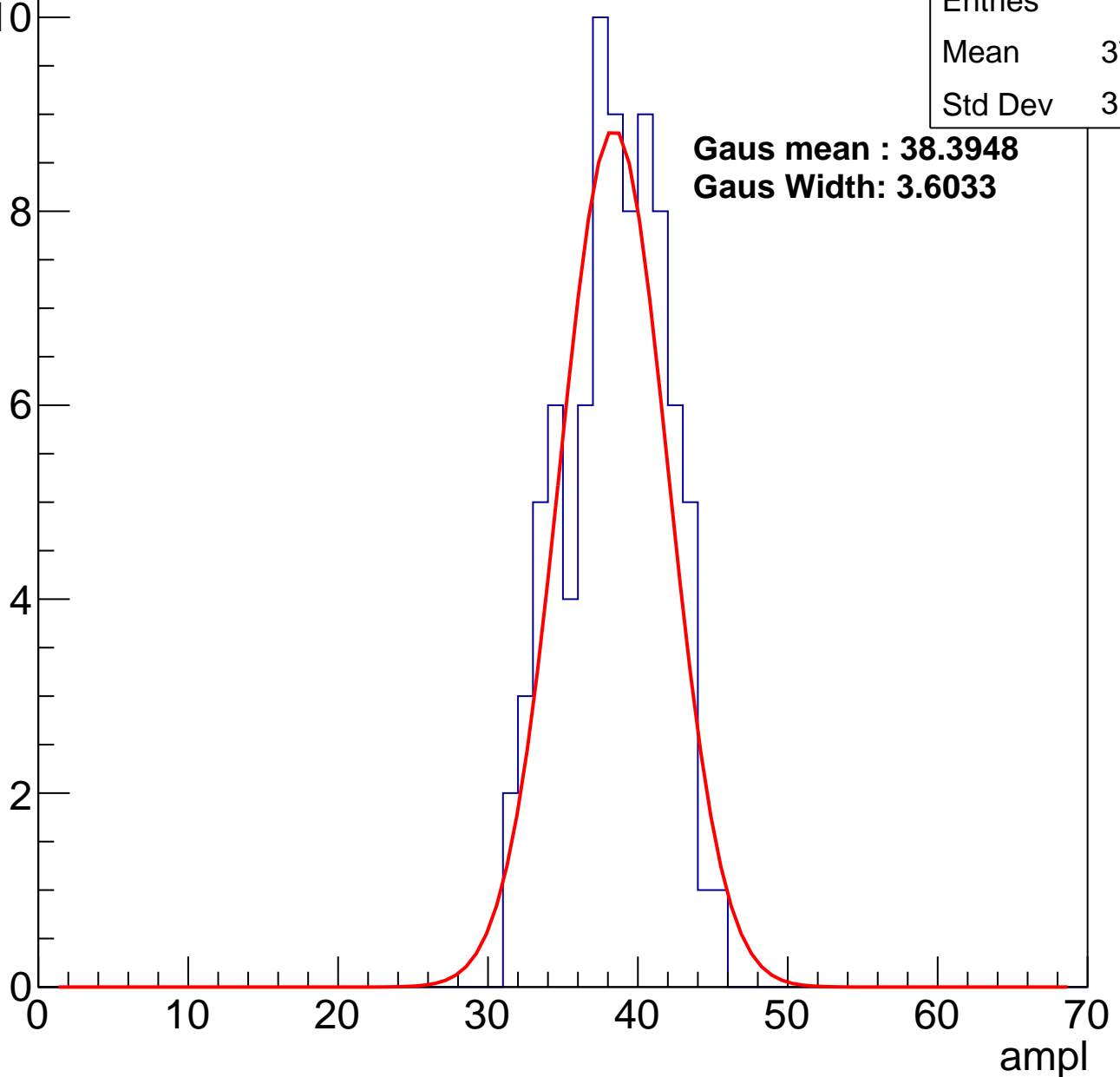
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	83
Mean	37.96
Std Dev	3.327

**Gaus mean : 38.3948**

**Gaus Width: 3.6033**



# B1L003S, U11-ch55, adc2

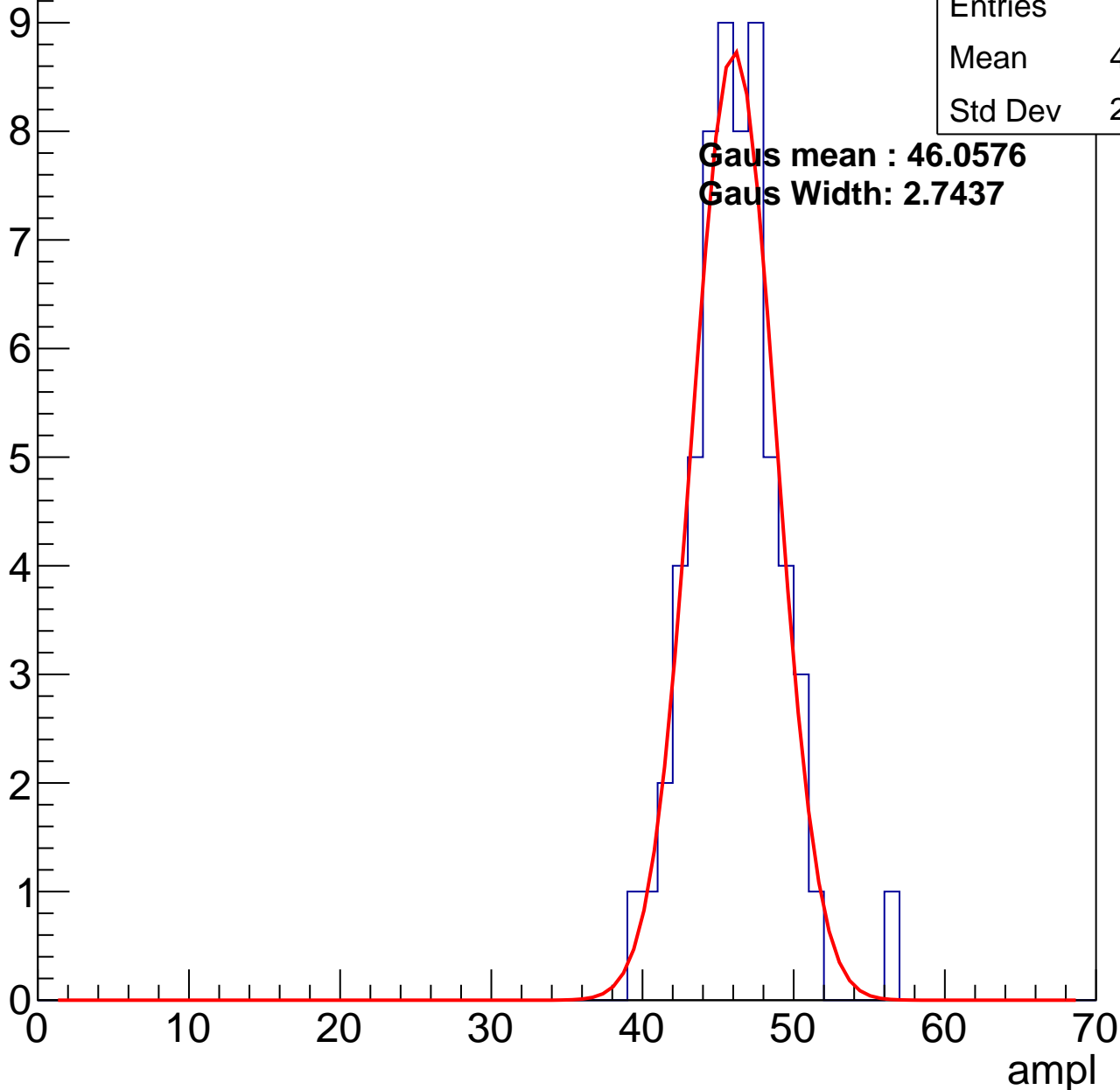
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	45.66
Std Dev	2.908

**Gaus mean : 46.0576**

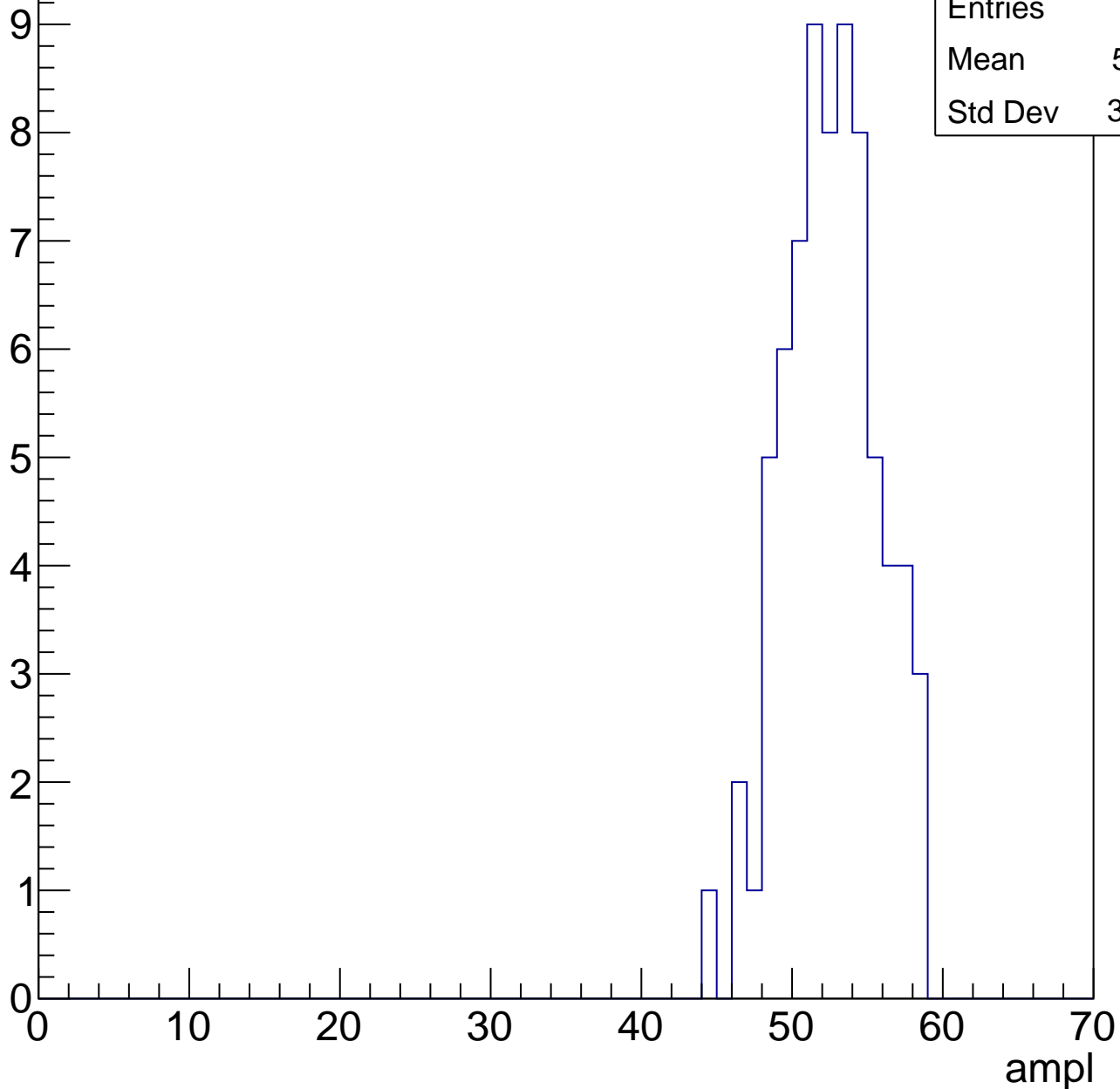
**Gaus Width: 2.7437**



# B1L003S, U11-ch55, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



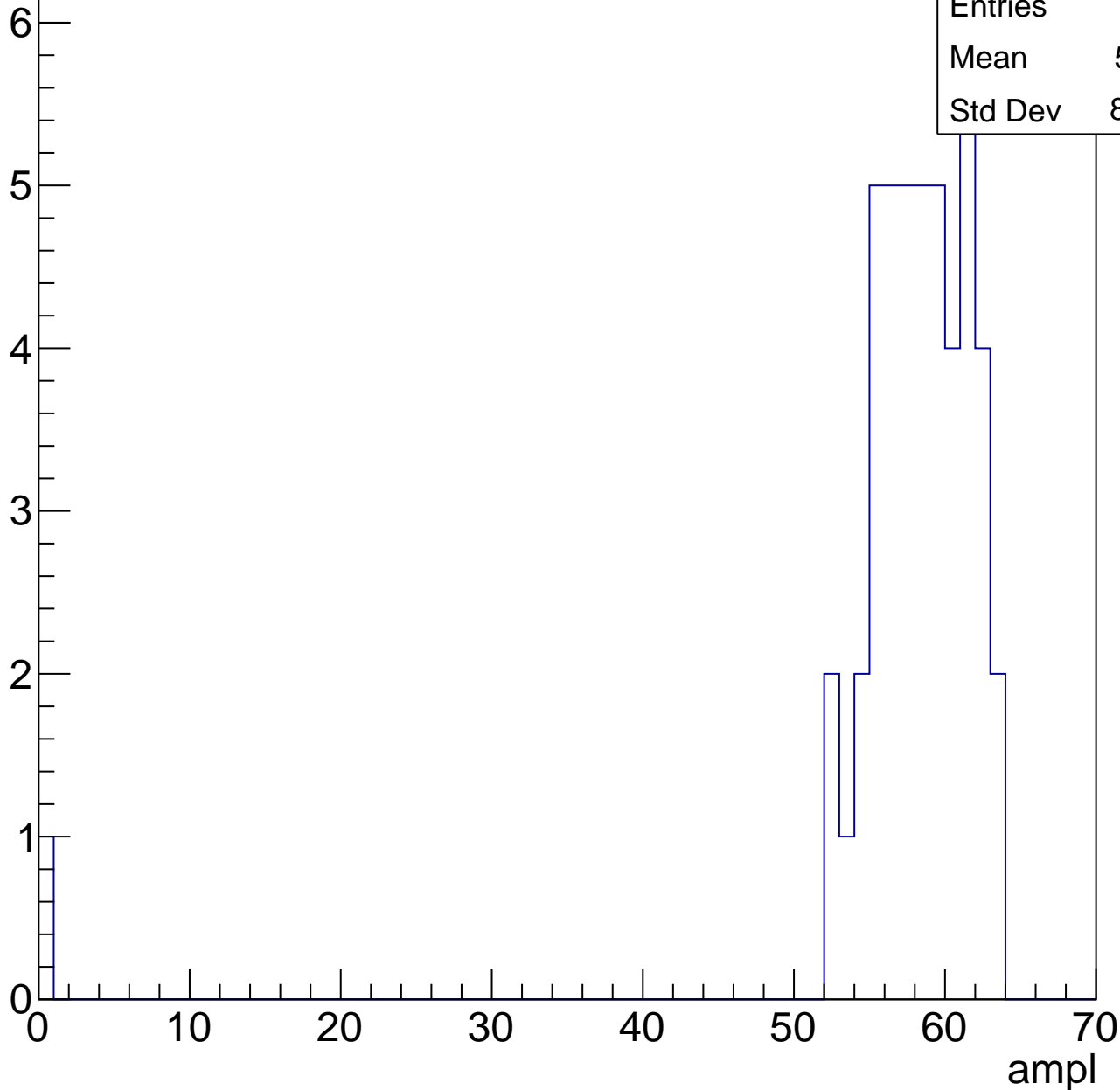
Entries	72
Mean	52.11
Std Dev	3.094

# B1L003S, U11-ch55, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	47
Mean	56.81
Std Dev	8.855

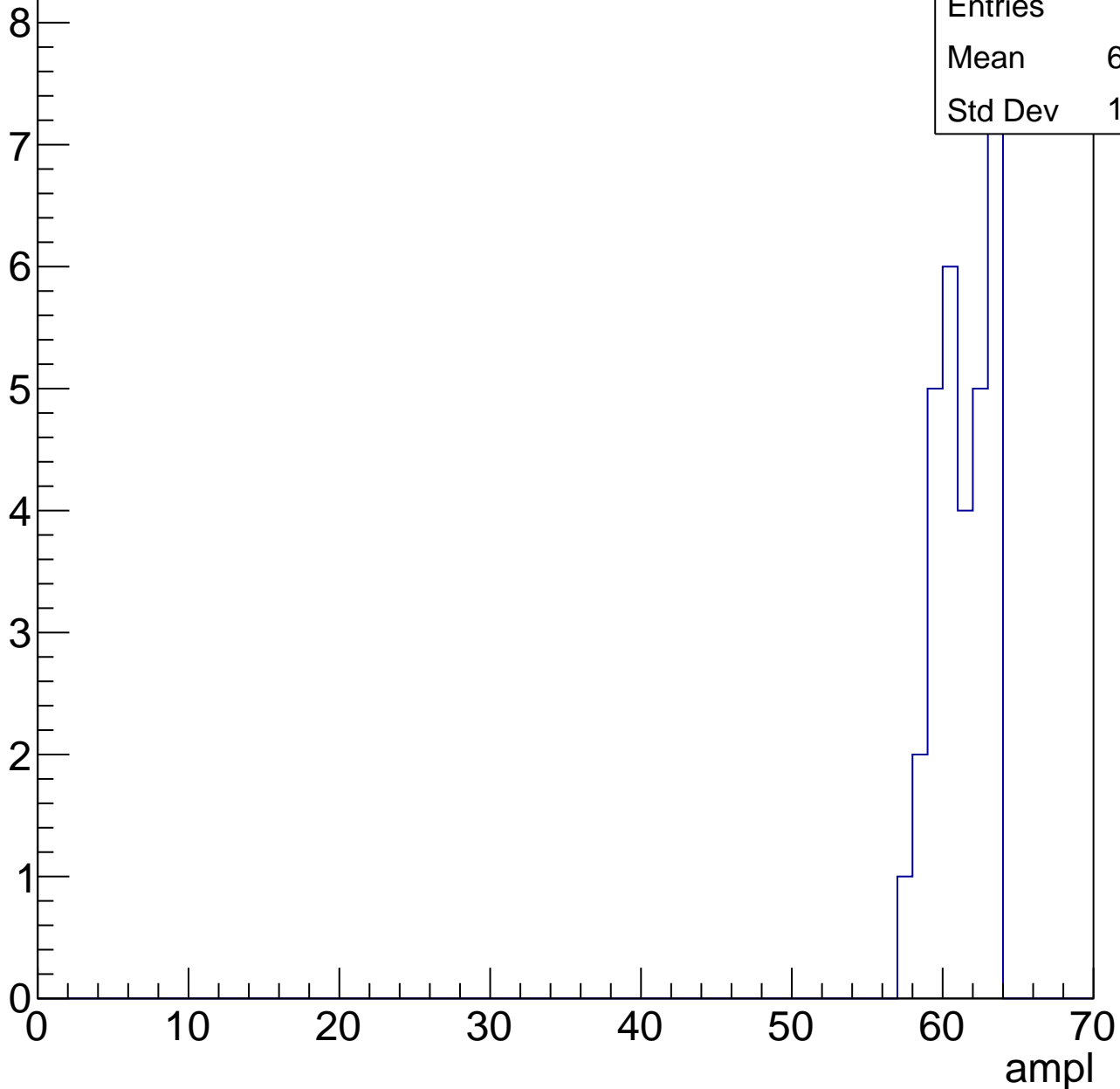


# B1L003S, U11-ch55, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	31
Mean	60.84
Std Dev	1.762



# B1L003S, U11-ch55, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



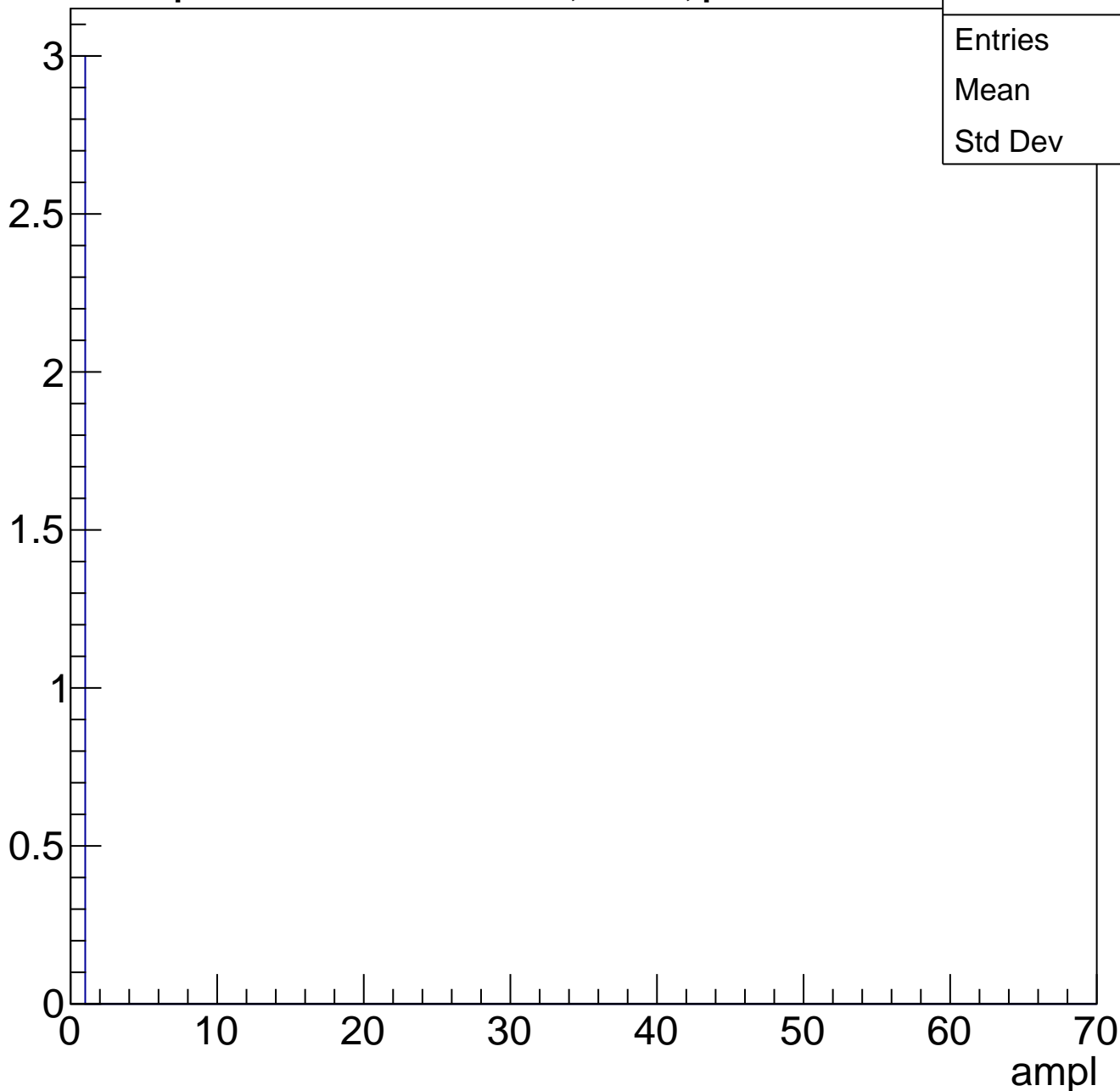
Entries	1
Mean	62
Std Dev	0



# B1L003S, U11-ch55, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L003S, U11-ch56, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	65
Mean	30.58
Std Dev	2.789

**Gaus mean : 31.5096**

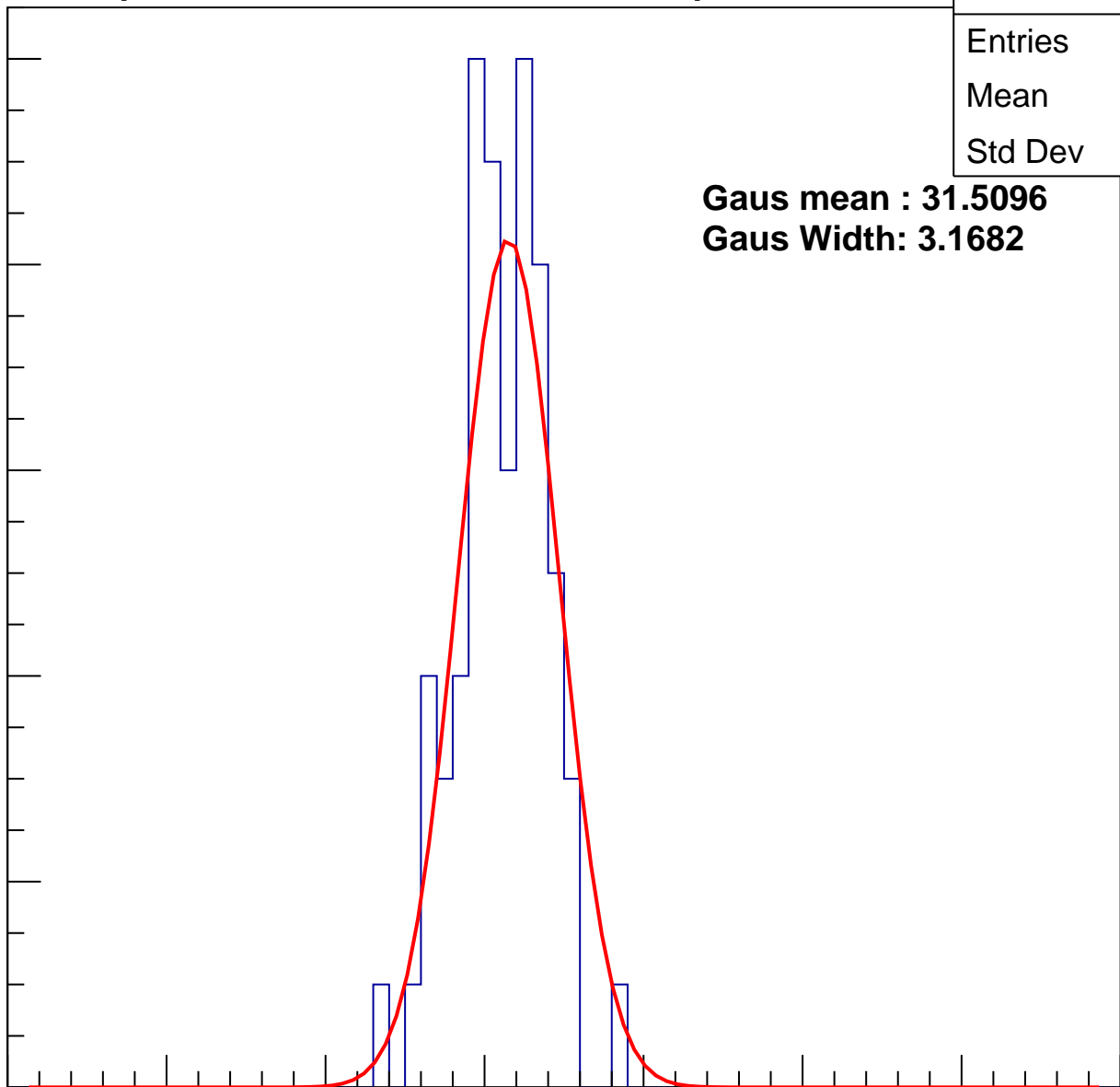
**Gaus Width: 3.1682**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L003S, U11-ch56, adc1

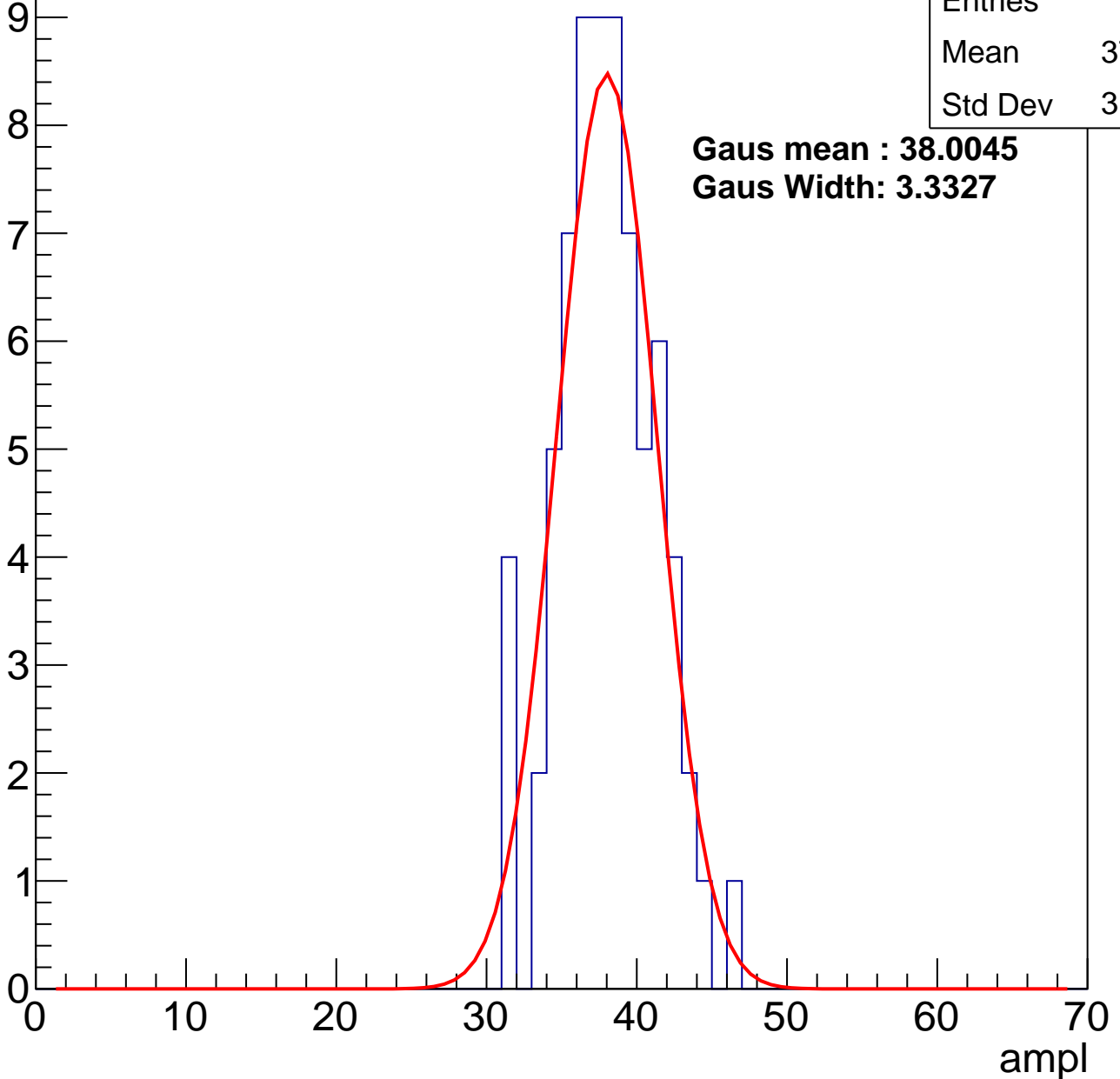
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	71
Mean	37.56
Std Dev	3.174

**Gaus mean : 38.0045**

**Gaus Width: 3.3327**



# B1L003S, U11-ch56, adc2

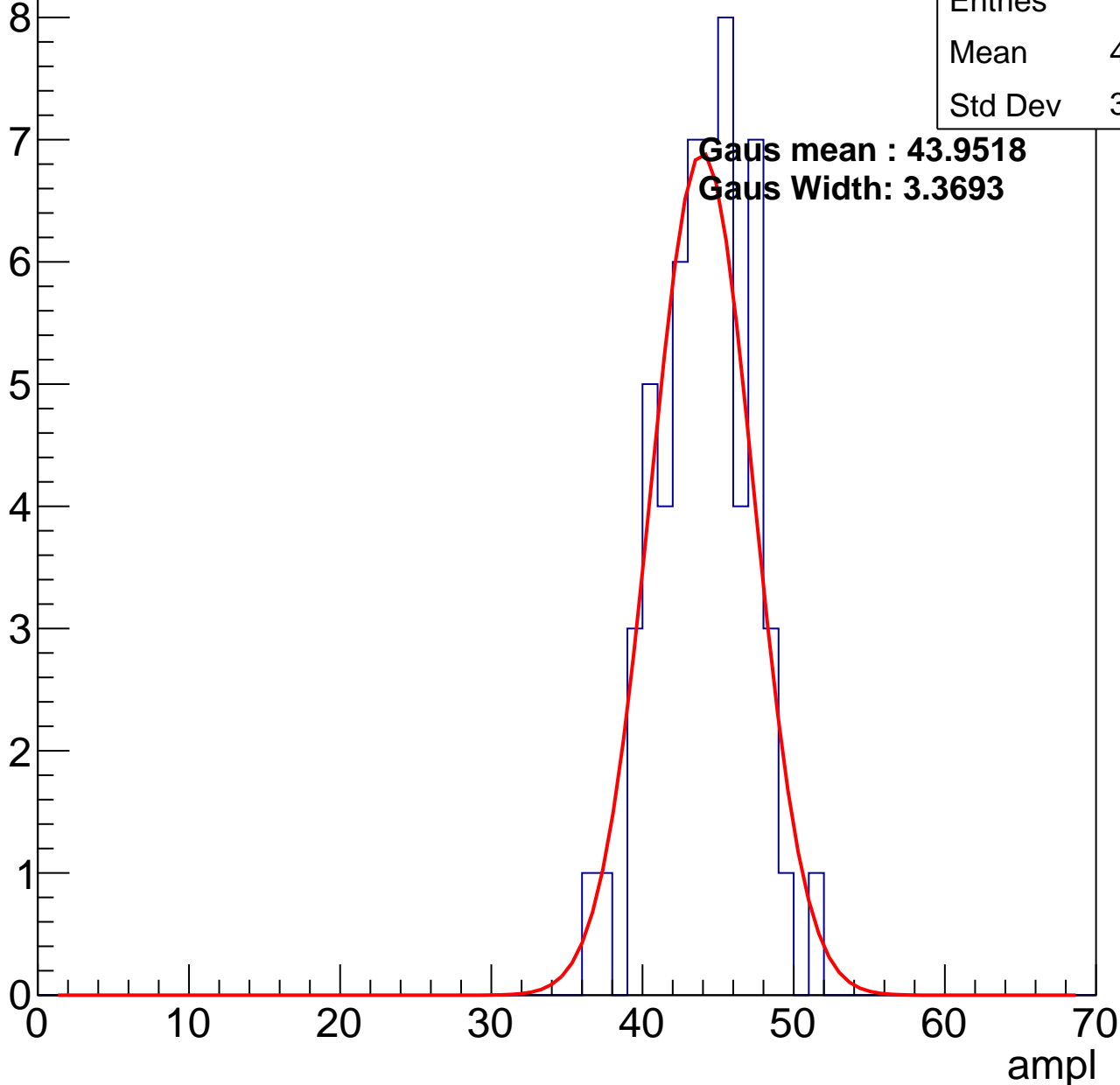
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	43.66
Std Dev	3.043

Gaus mean : 43.9518

Gaus Width: 3.3693

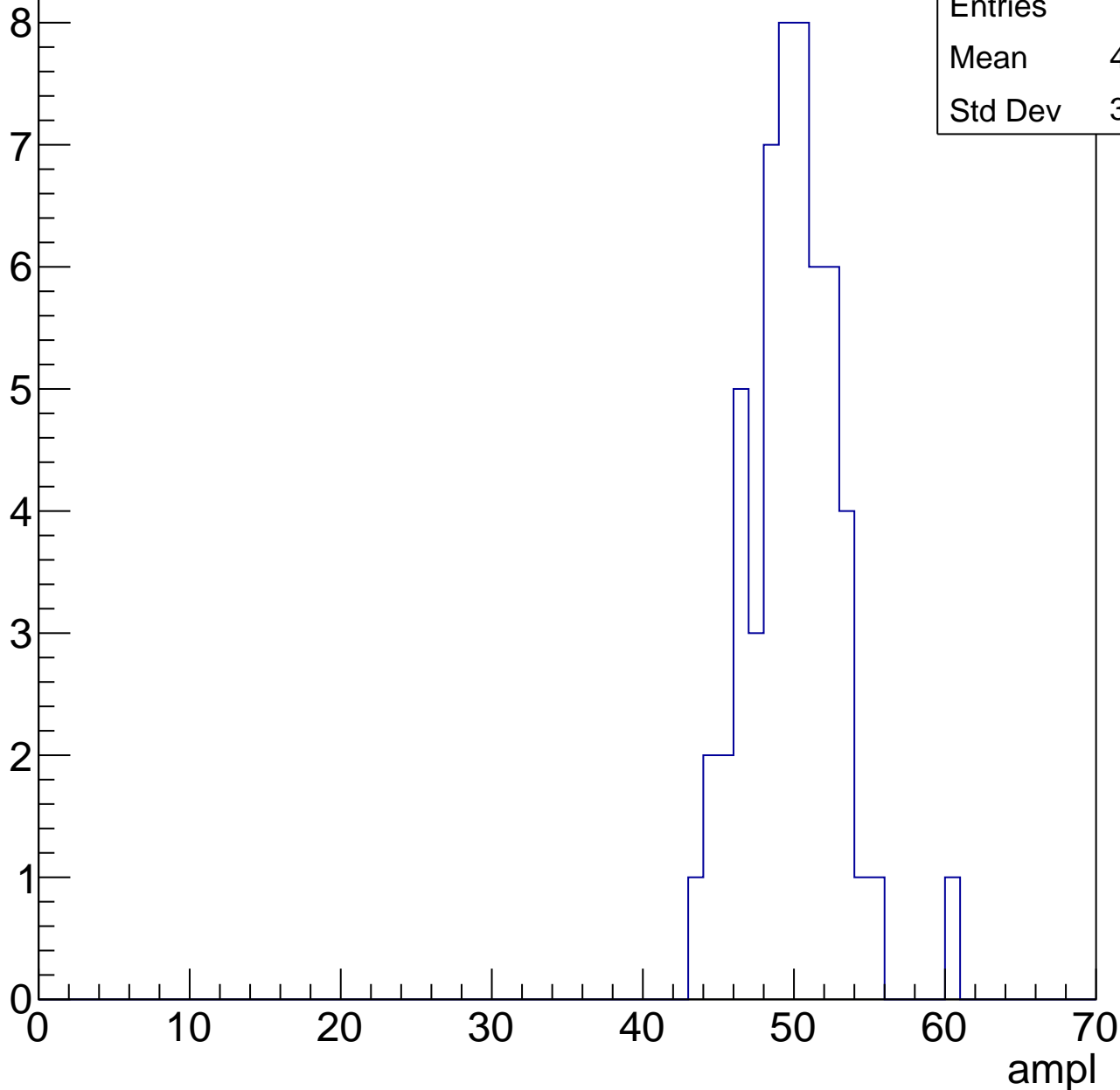


# B1L003S, U11-ch56, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

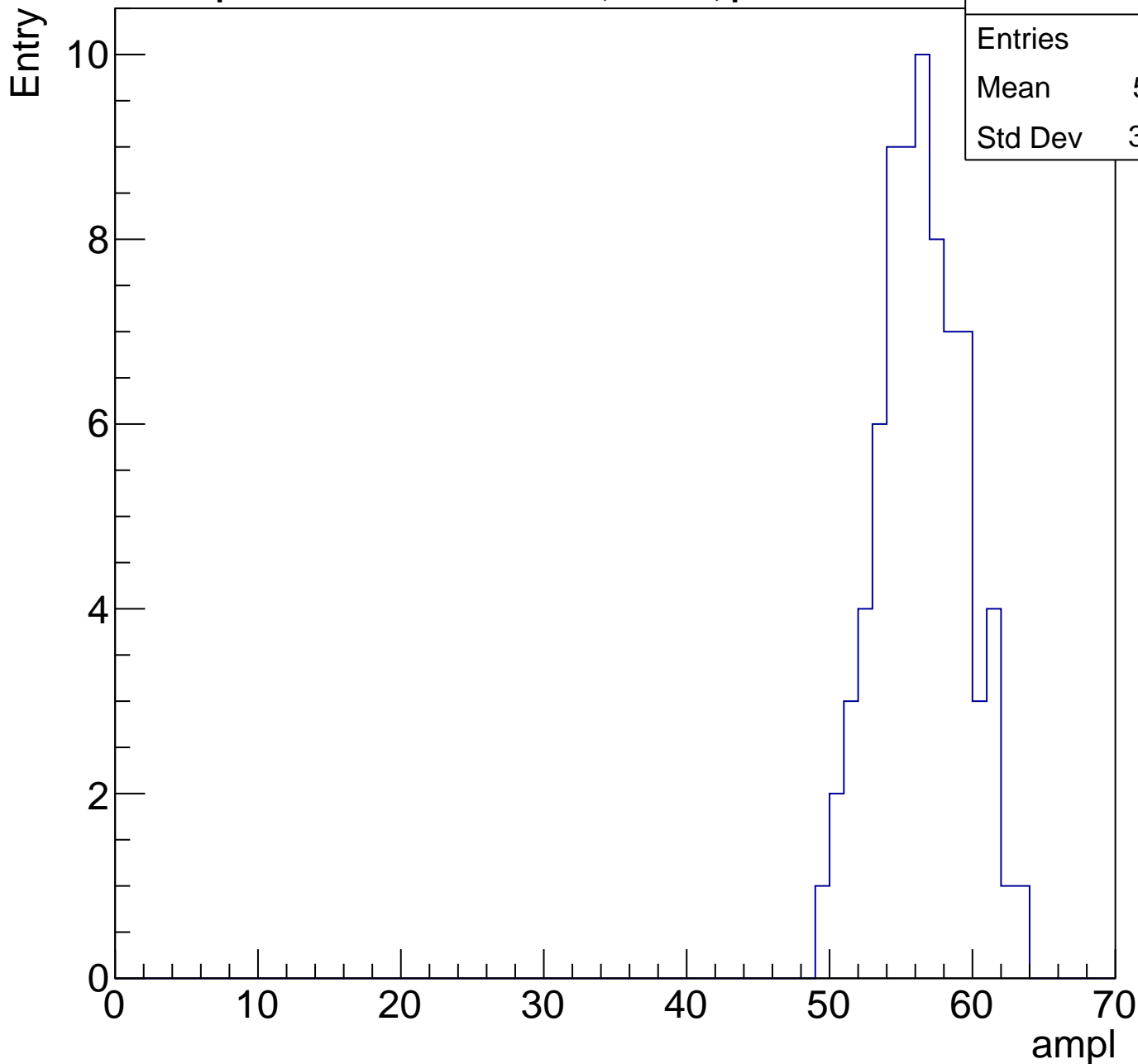
Entries	55
Mean	49.44
Std Dev	3.026



# B1L003S, U11-ch56, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	75
Mean	55.91
Std Dev	3.034

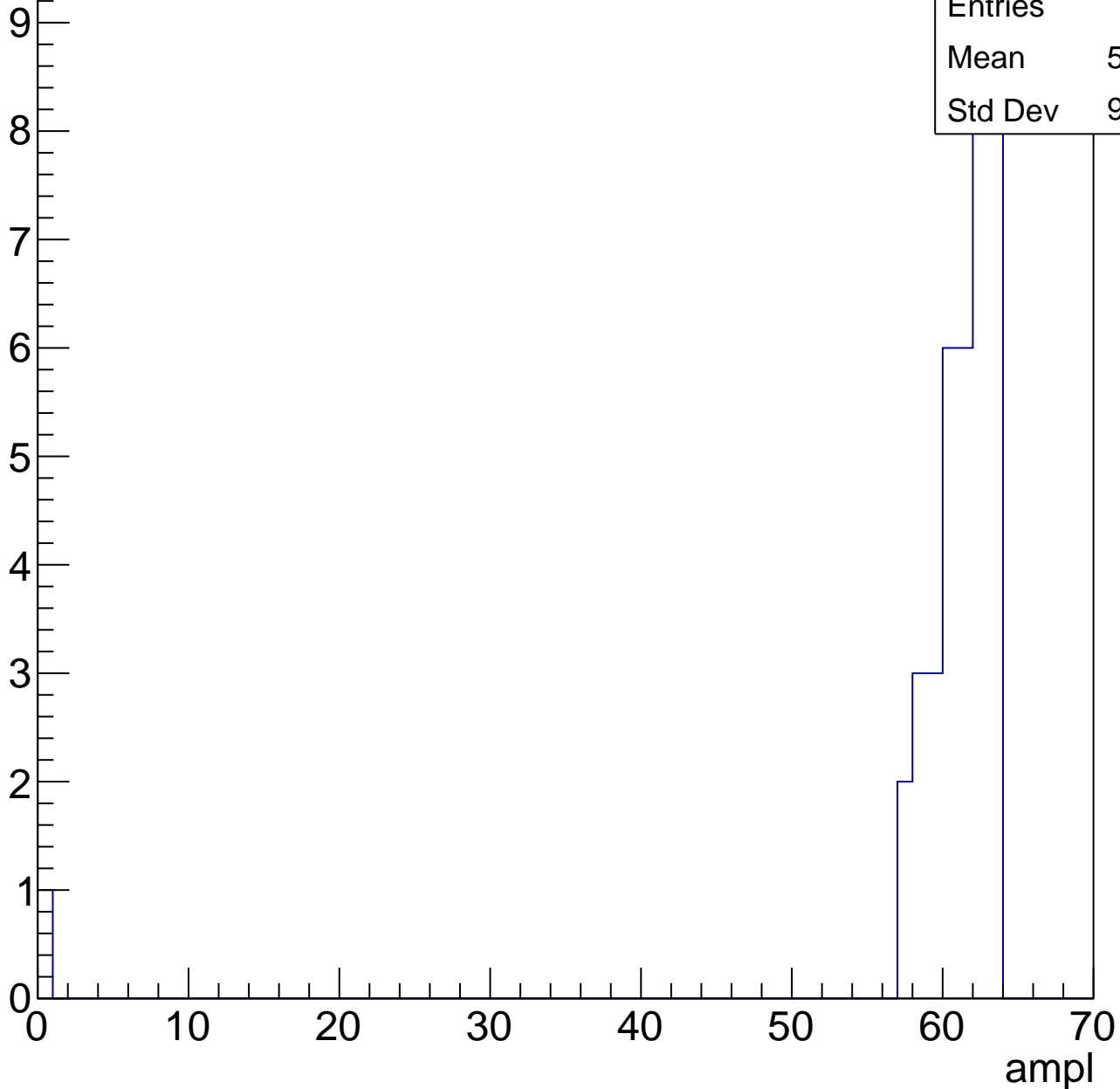


# B1L003S, U11-ch56, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	38
Mean	59.29
Std Dev	9.905



# B1L003S, U11-ch56, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	63
Std Dev	0



# B1L003S, U11-ch56, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U11-ch57, adc0

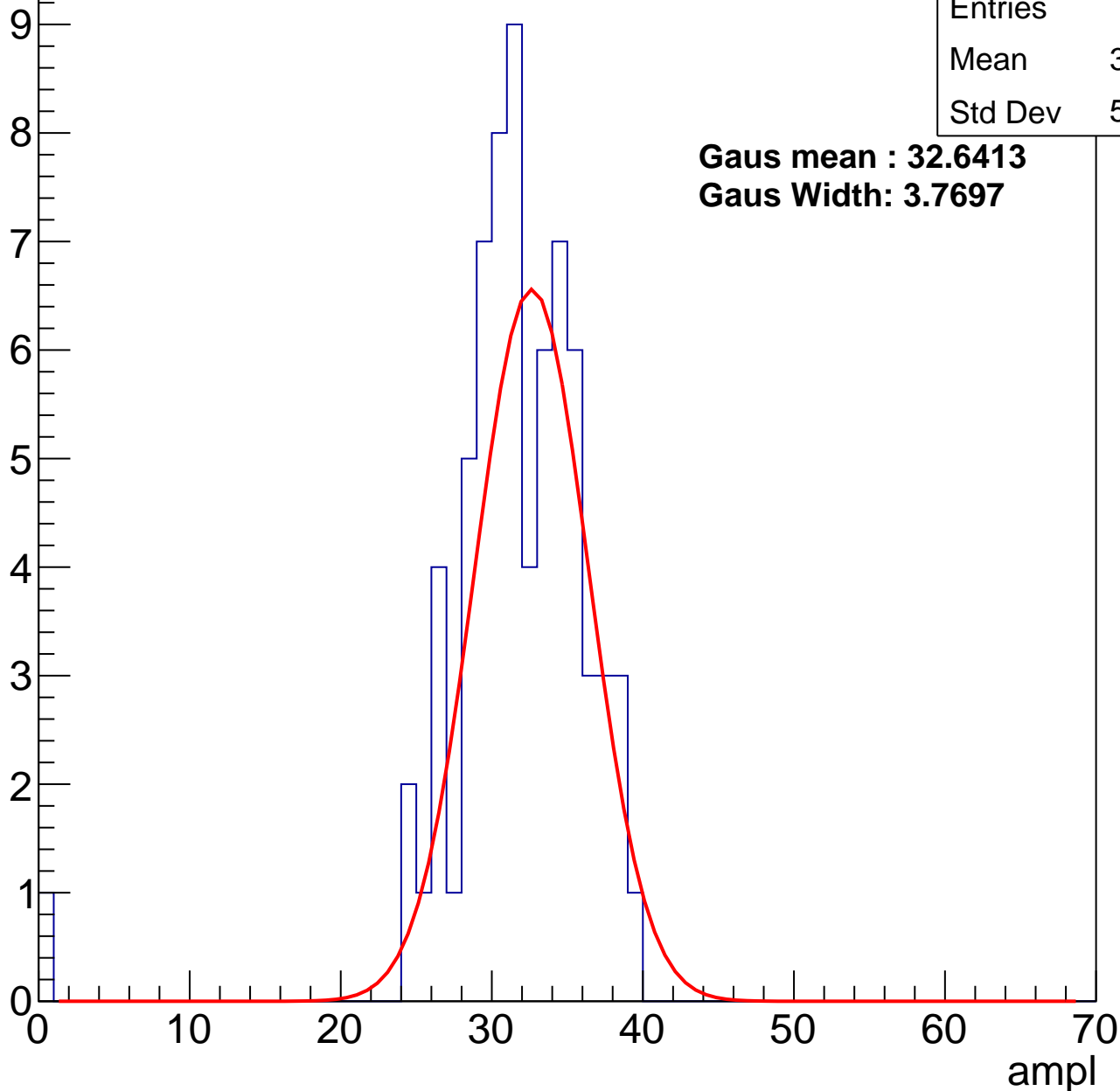
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	71
Mean	31.15
Std Dev	5.134

**Gaus mean : 32.6413**

**Gaus Width: 3.7697**



# B1L003S, U11-ch57, adc1

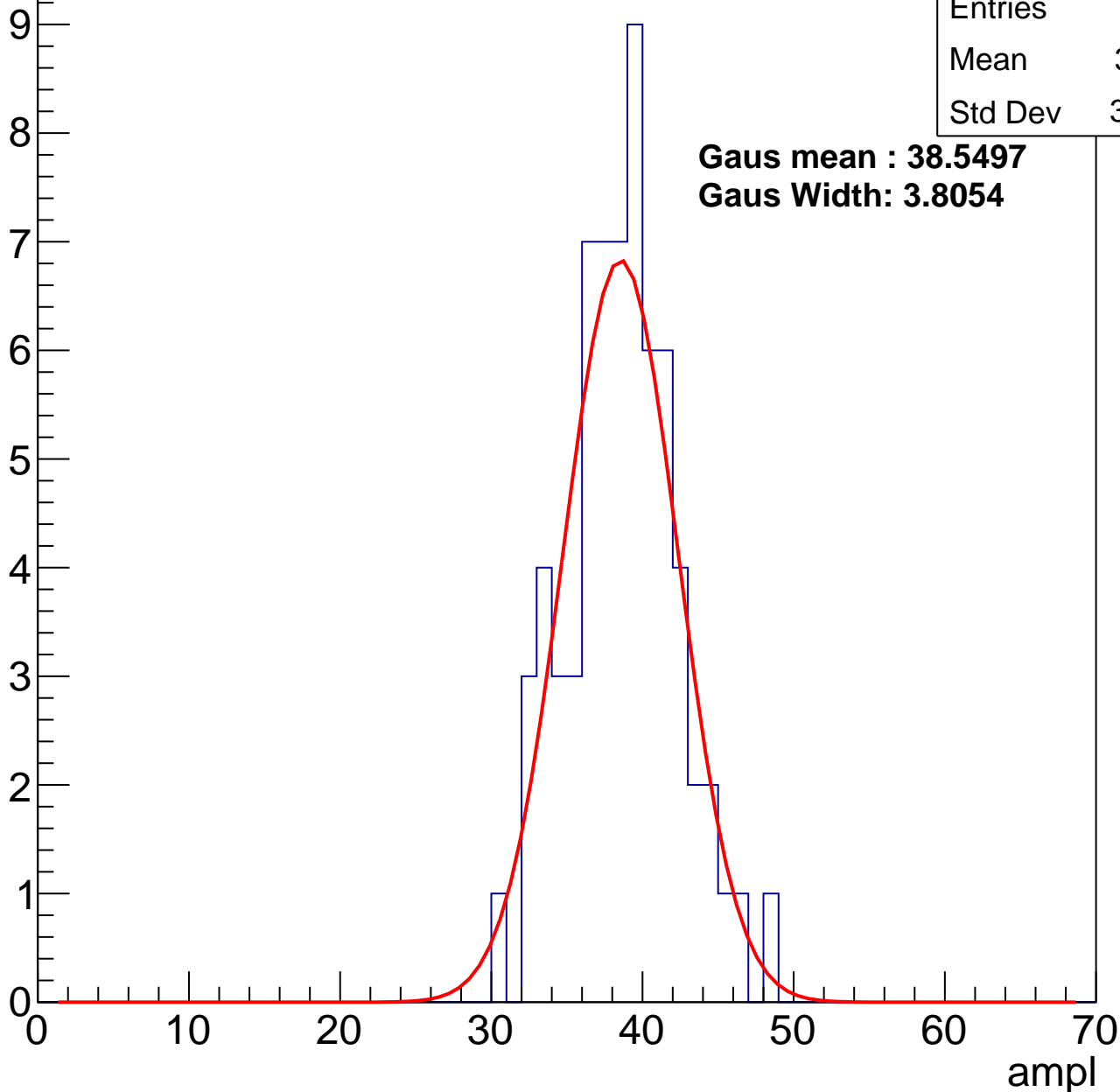
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	38.21
Std Dev	3.593

**Gaus mean : 38.5497**

**Gaus Width: 3.8054**



# B1L003S, U11-ch57, adc2

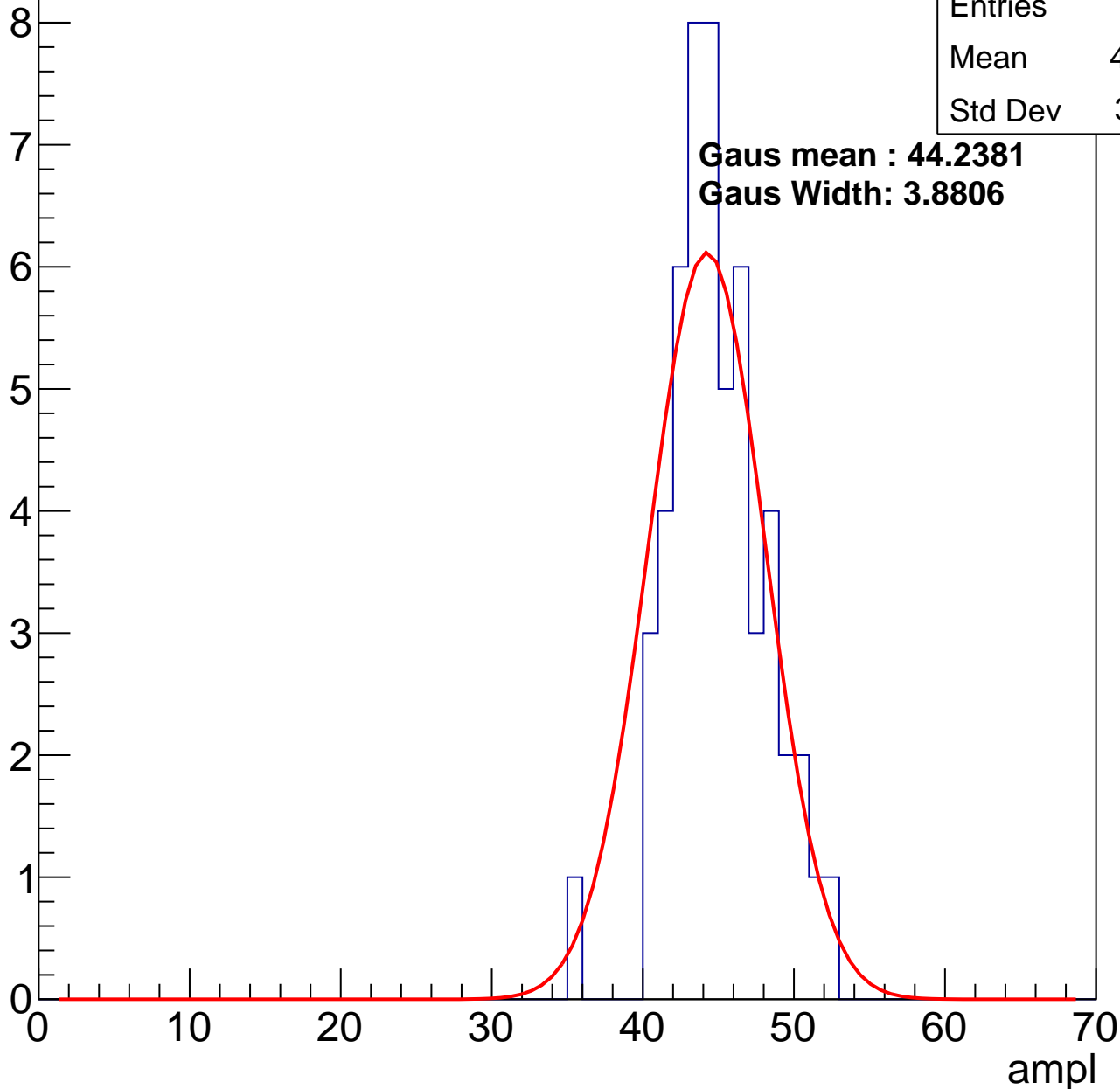
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	54
Mean	44.48
Std Dev	3.161

**Gaus mean : 44.2381**

**Gaus Width: 3.8806**

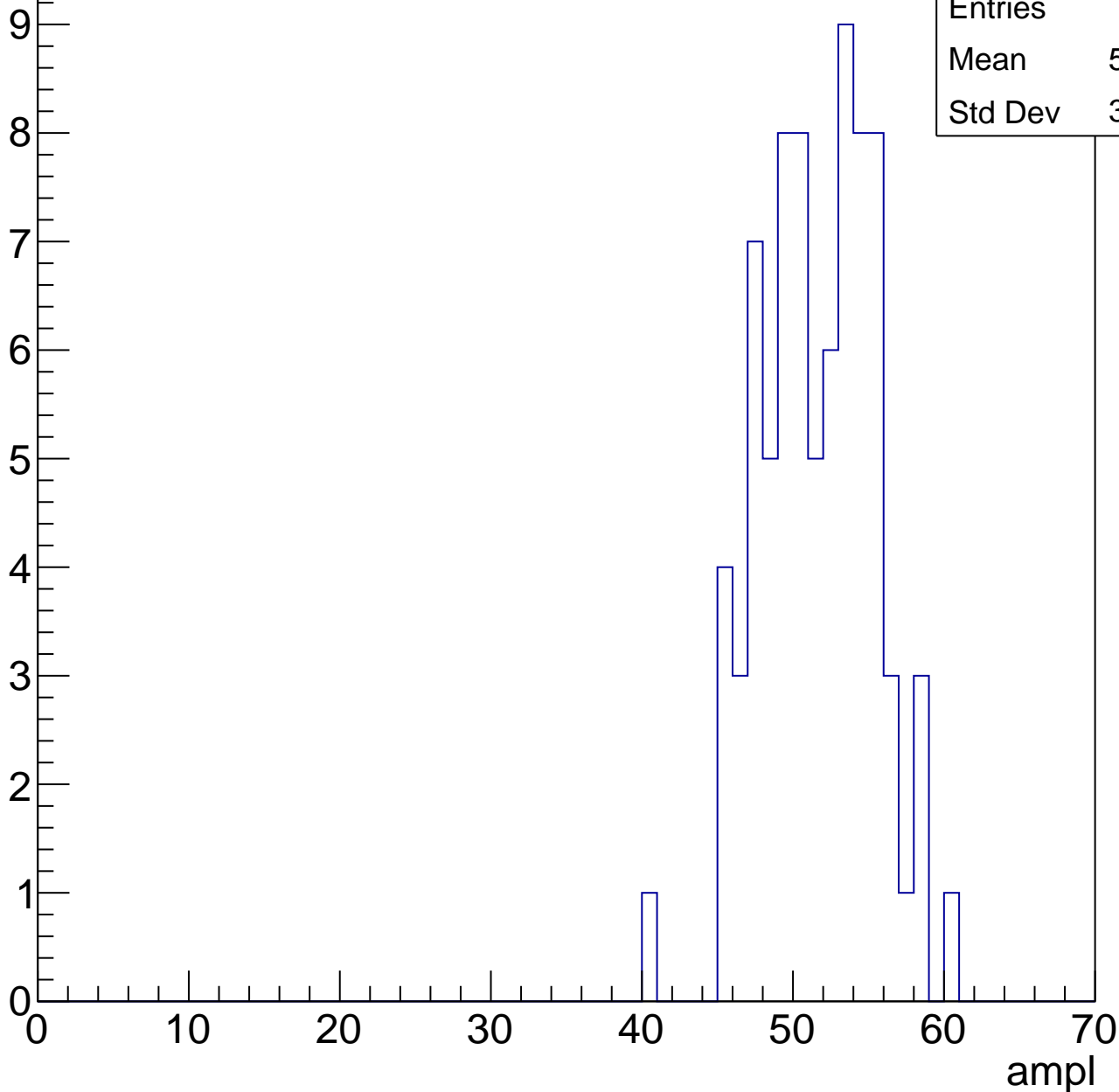


# B1L003S, U11-ch57, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

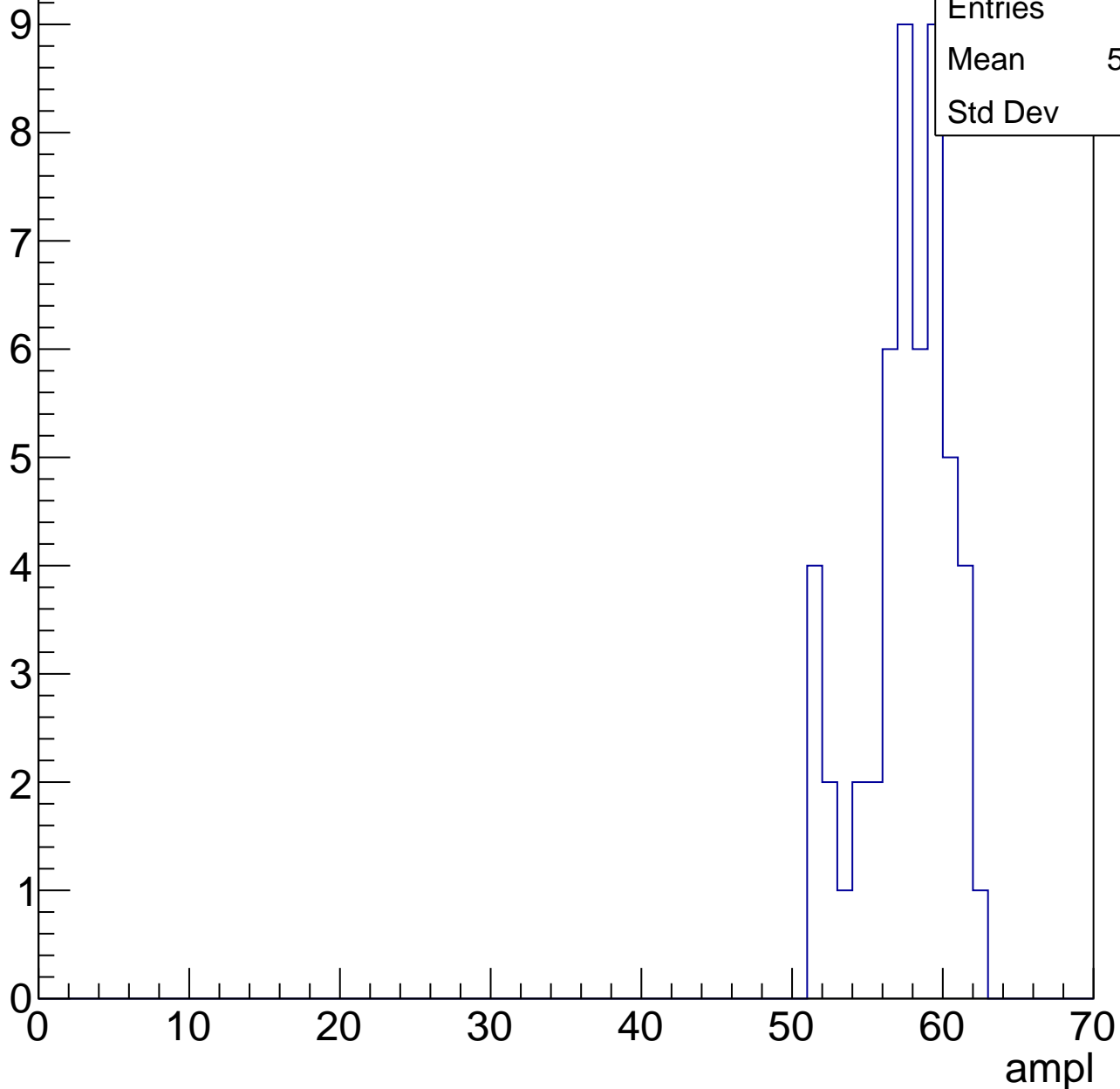
Entries	80
Mean	51.17
Std Dev	3.734



# B1L003S, U11-ch57, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U11-ch57, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	33
Mean	61.18
Std Dev	2.276

Entry

10

8

6

4

2

0

0

10

20

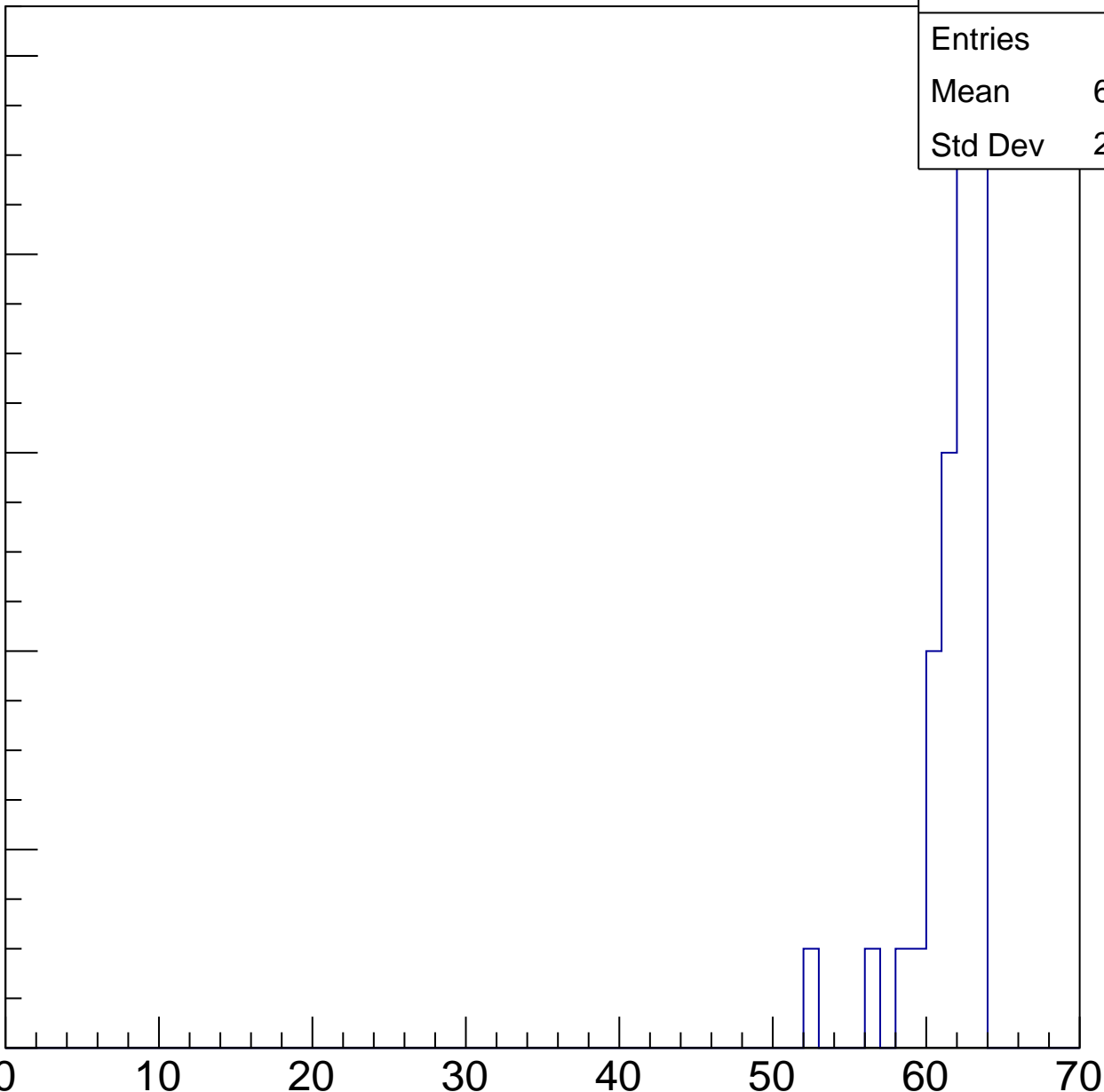
30

40

50

60

ampl



# B1L003S, U11-ch57, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch57, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U11-ch58, adc0

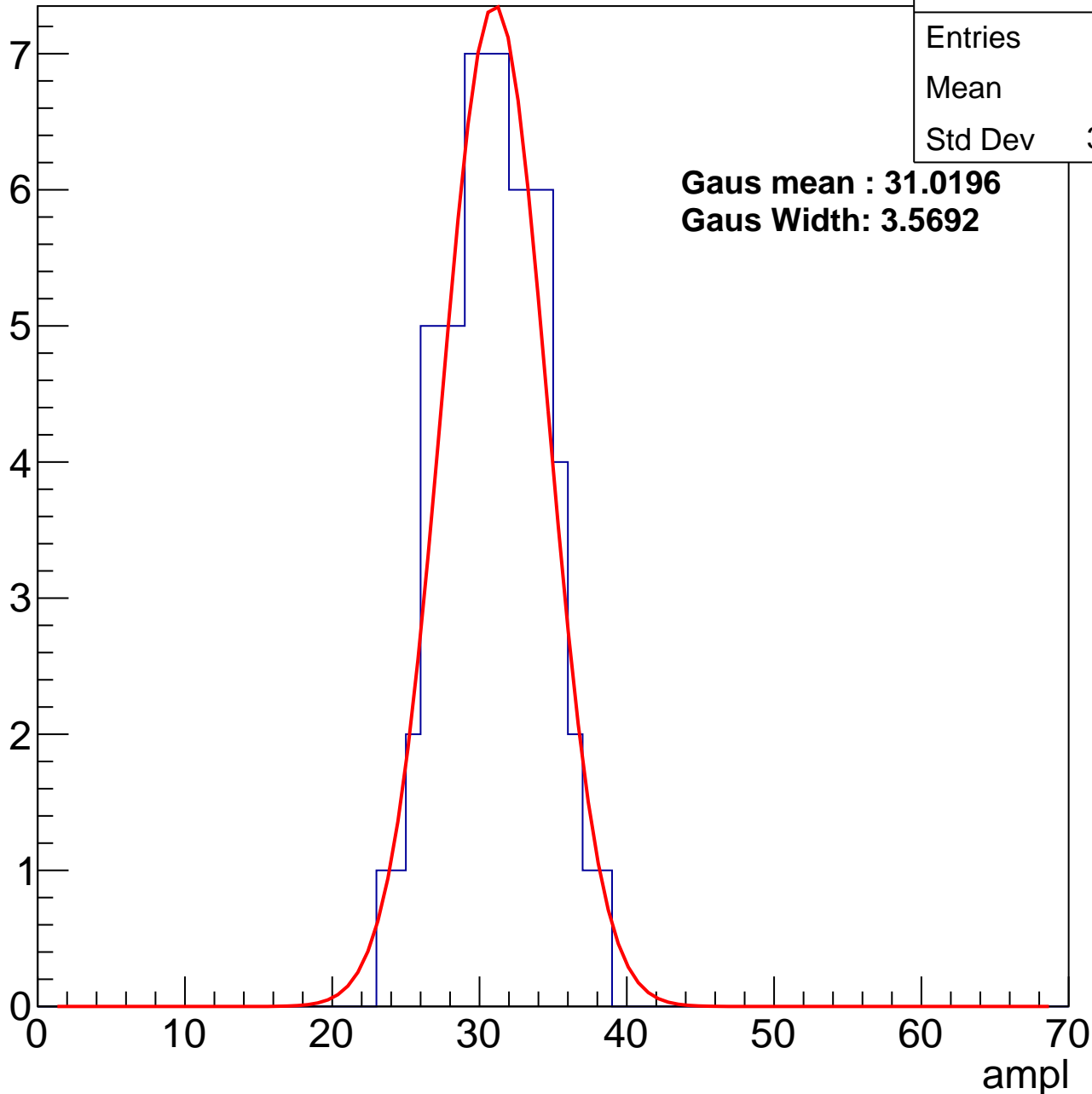
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	30.5
Std Dev	3.341

**Gaus mean : 31.0196**

**Gaus Width: 3.5692**



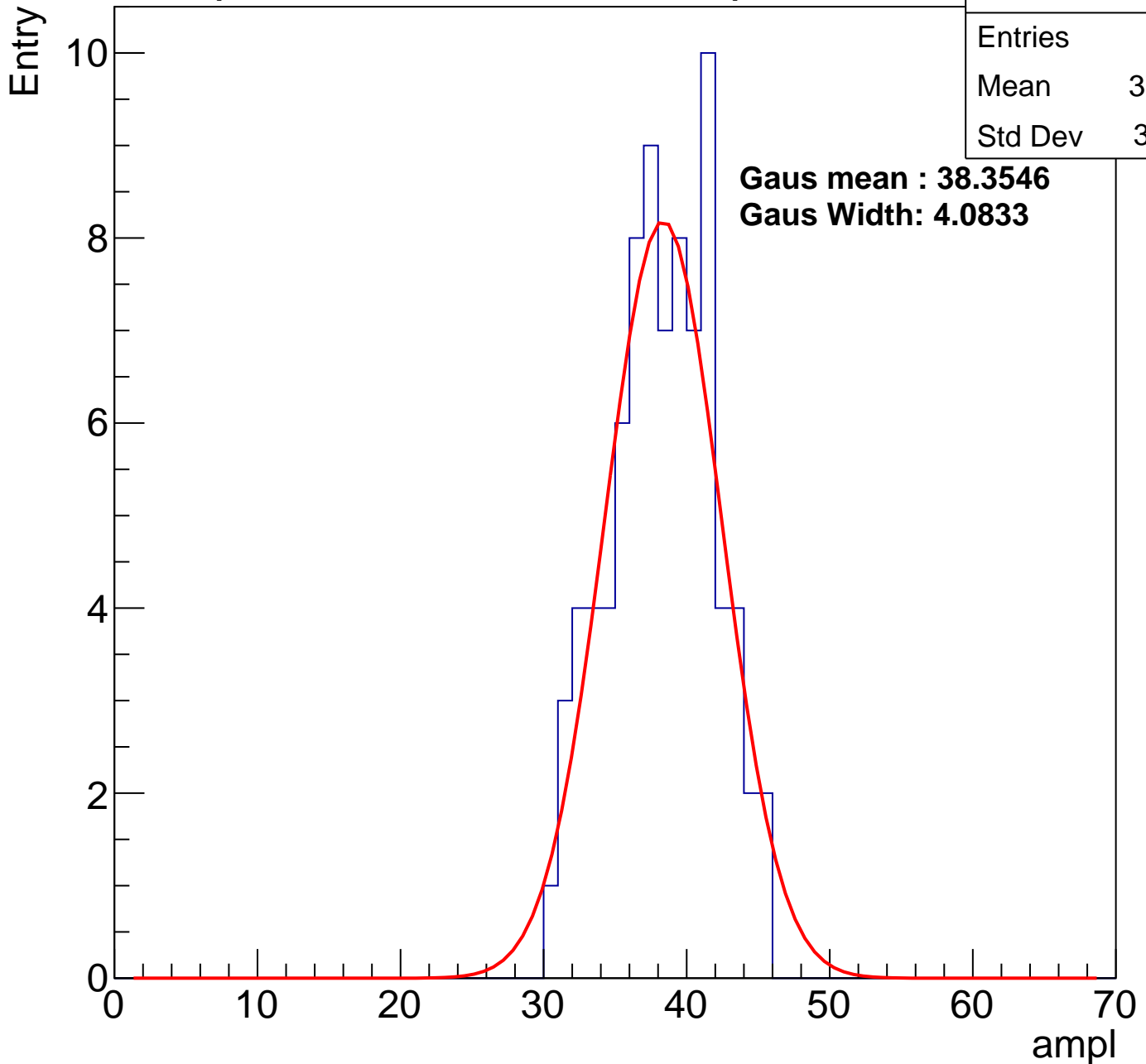
# B1L003S, U11-ch58, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	83
Mean	37.78
Std Dev	3.591

**Gaus mean : 38.3546**

**Gaus Width: 4.0833**



# B1L003S, U11-ch58, adc2

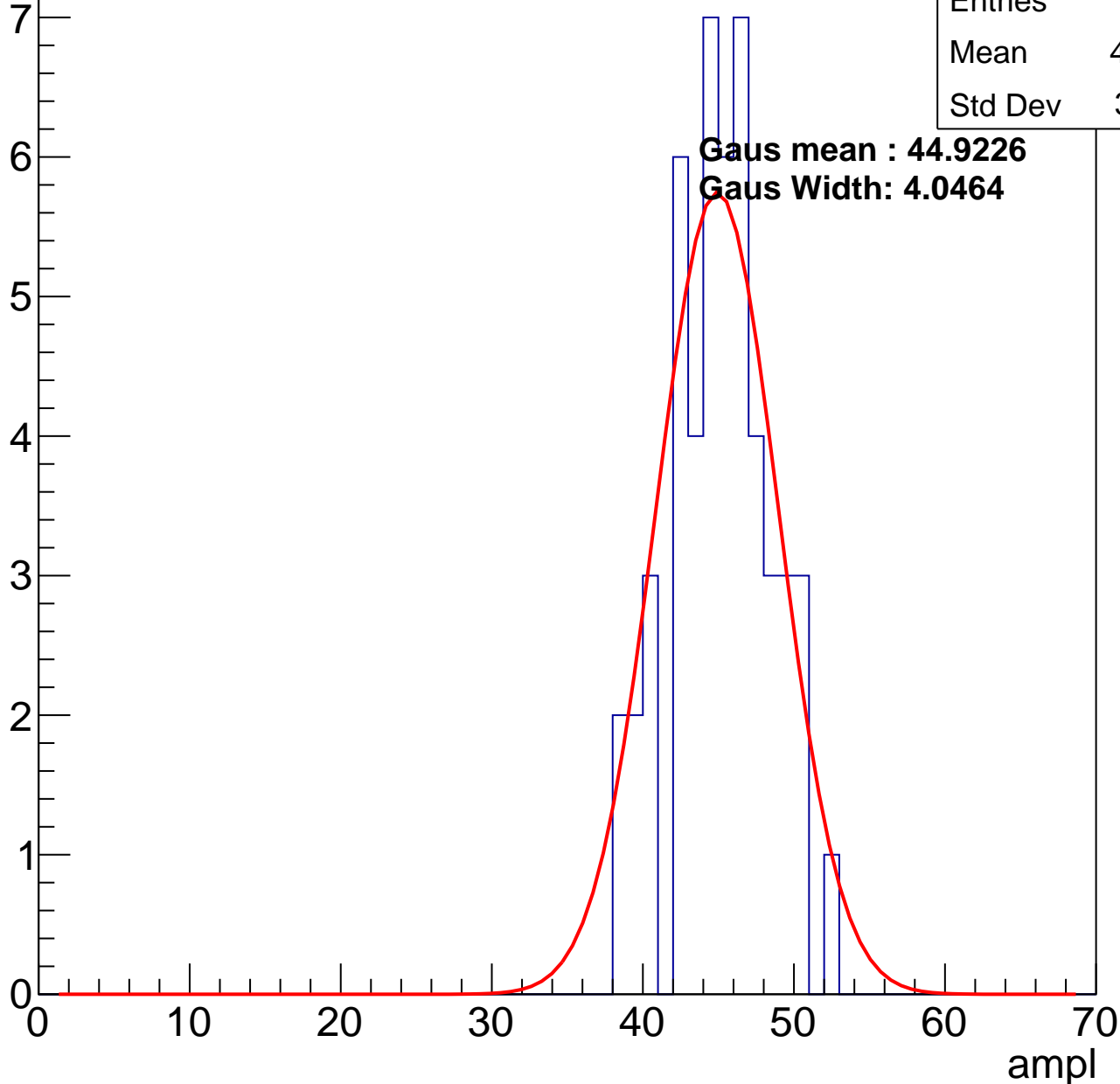
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	51
Mean	44.69
Std Dev	3.251

**Gaus mean : 44.9226**

**Gaus Width: 4.0464**

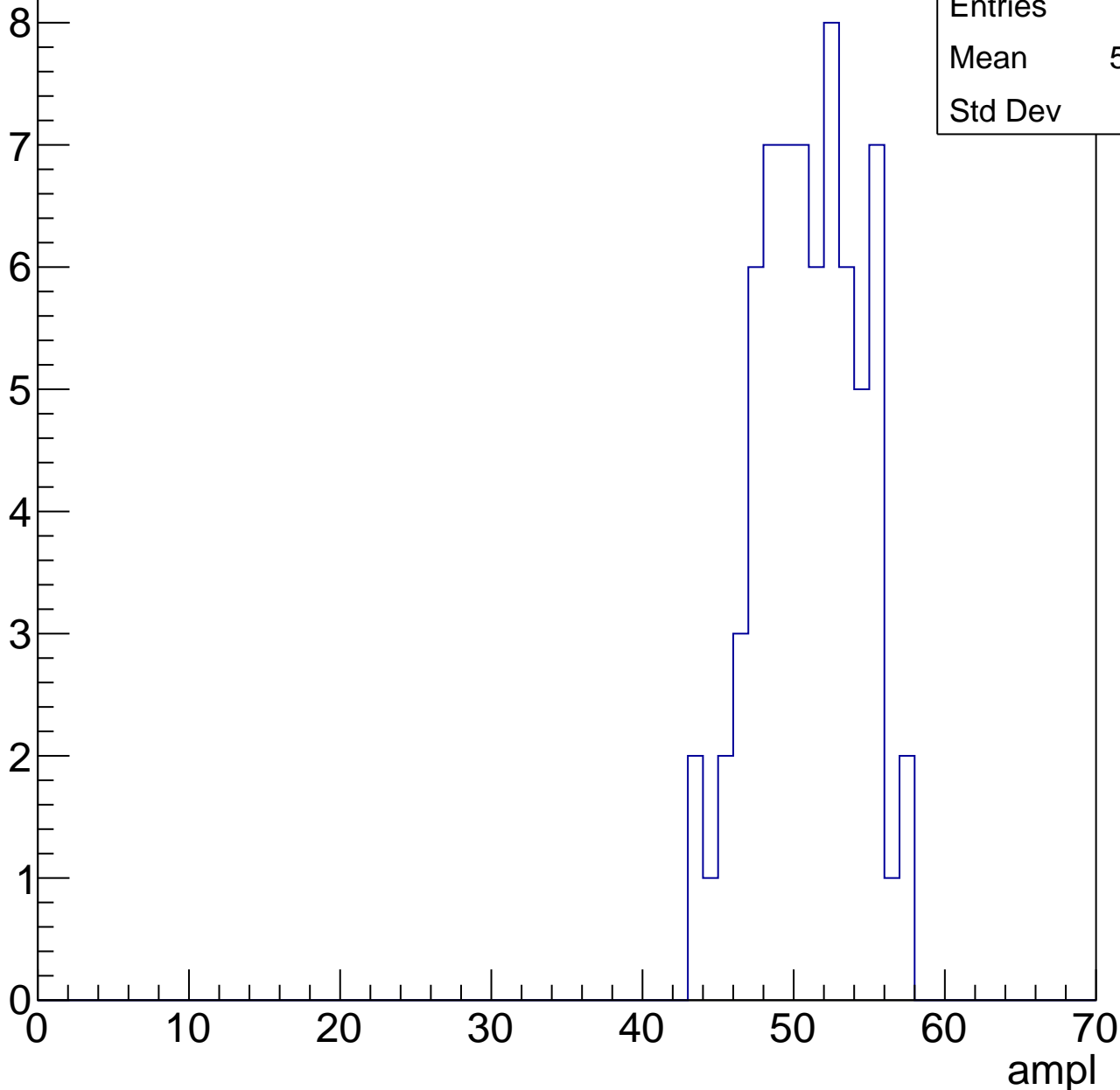


# B1L003S, U11-ch58, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

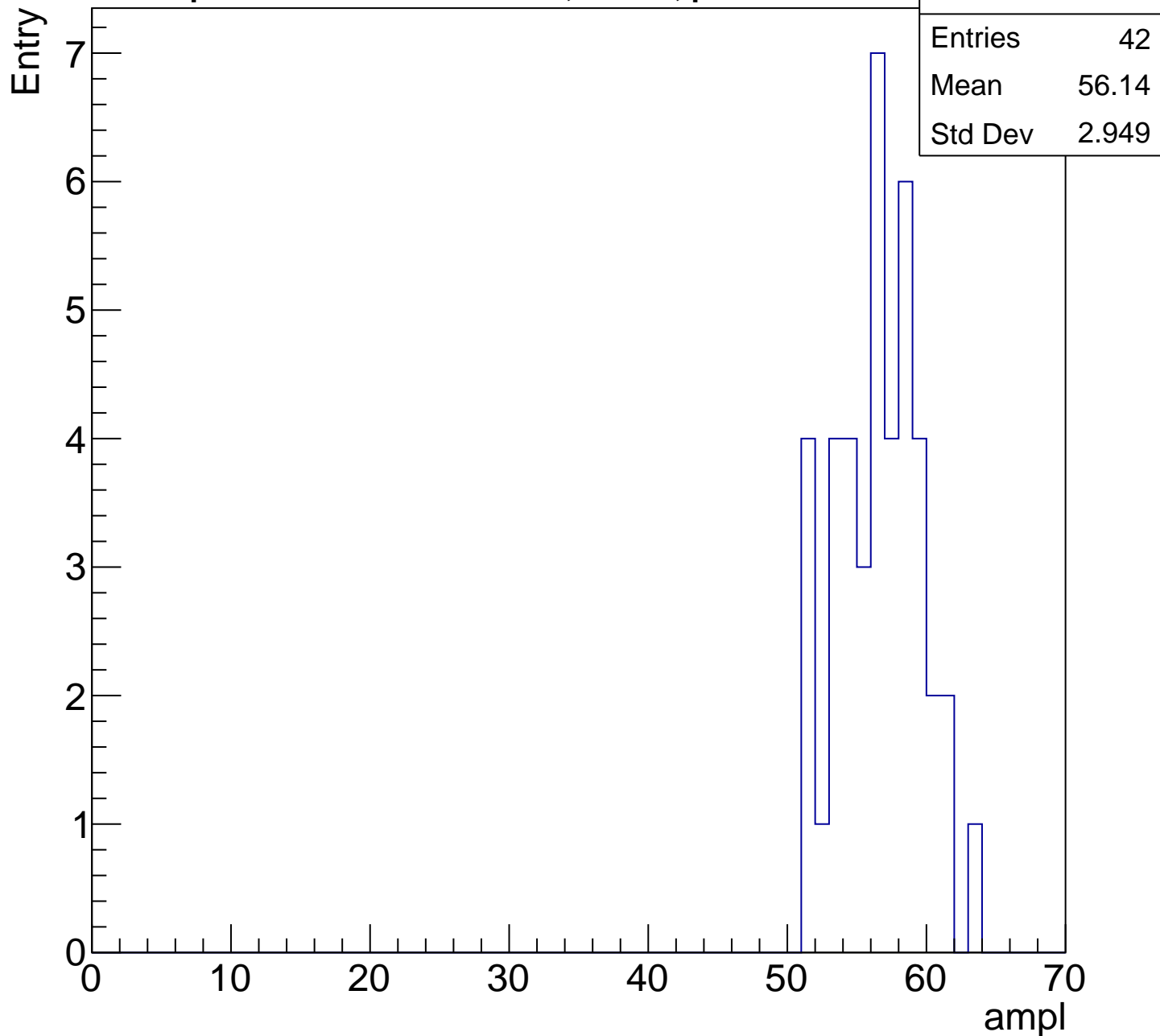
Entry

Entries	70
Mean	50.49
Std Dev	3.35



# B1L003S, U11-ch58, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

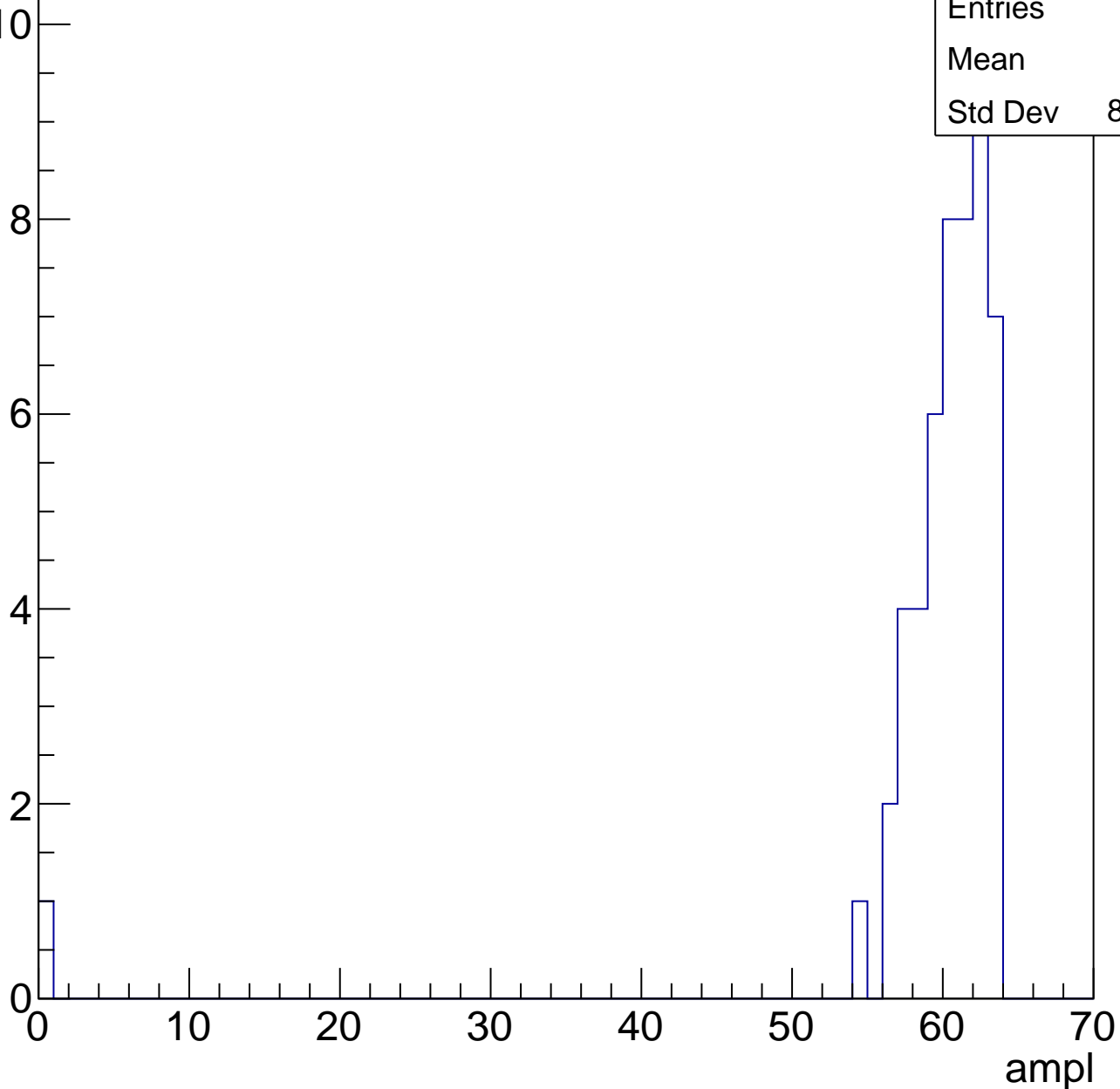


# B1L003S, U11-ch58, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	51
Mean	59
Std Dev	8.616



# B1L003S, U11-ch58, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch58, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U11-ch59, adc0

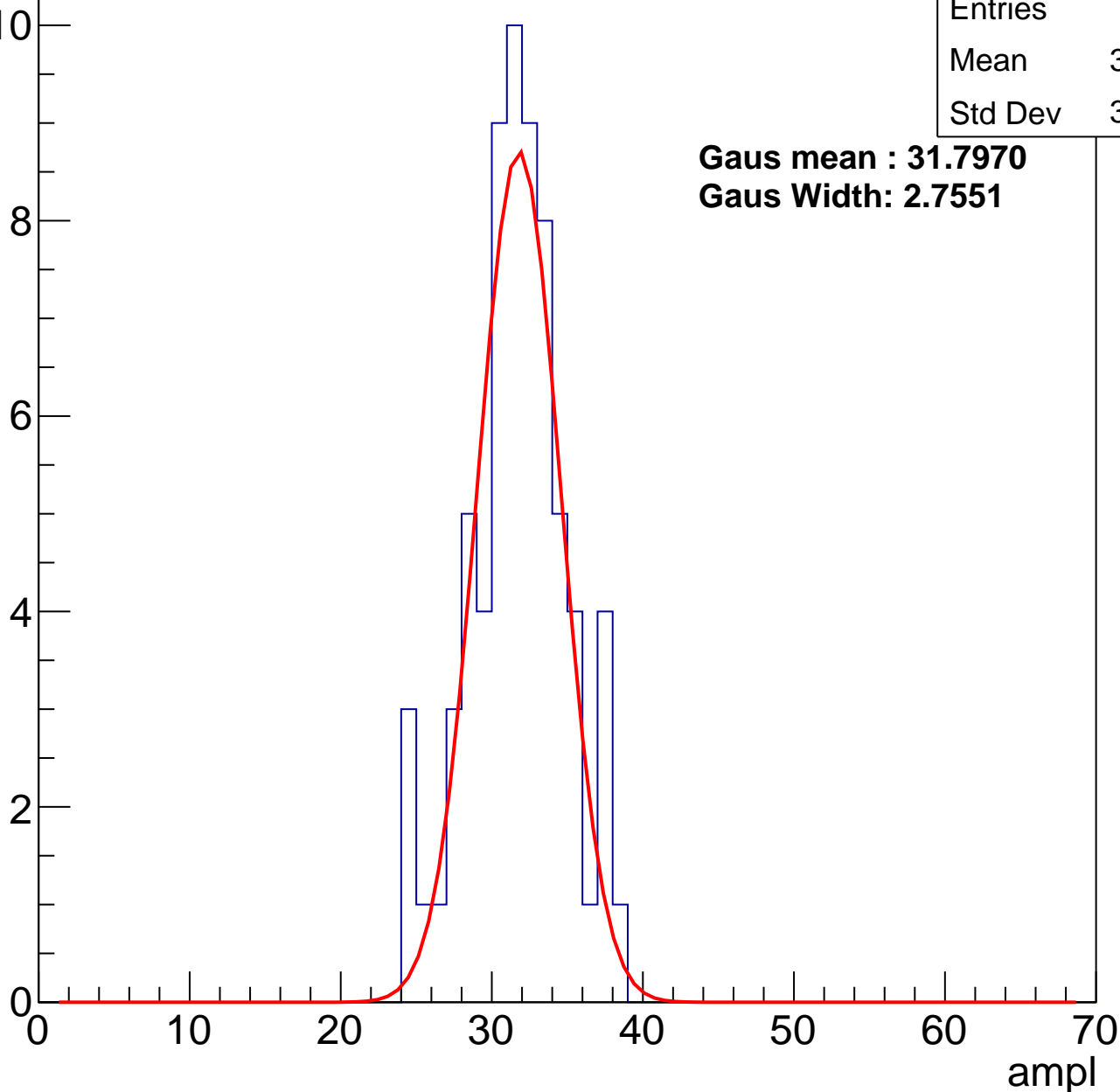
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	31.24
Std Dev	3.186

**Gaus mean : 31.7970**

**Gaus Width: 2.7551**



# B1L003S, U11-ch59, adc1

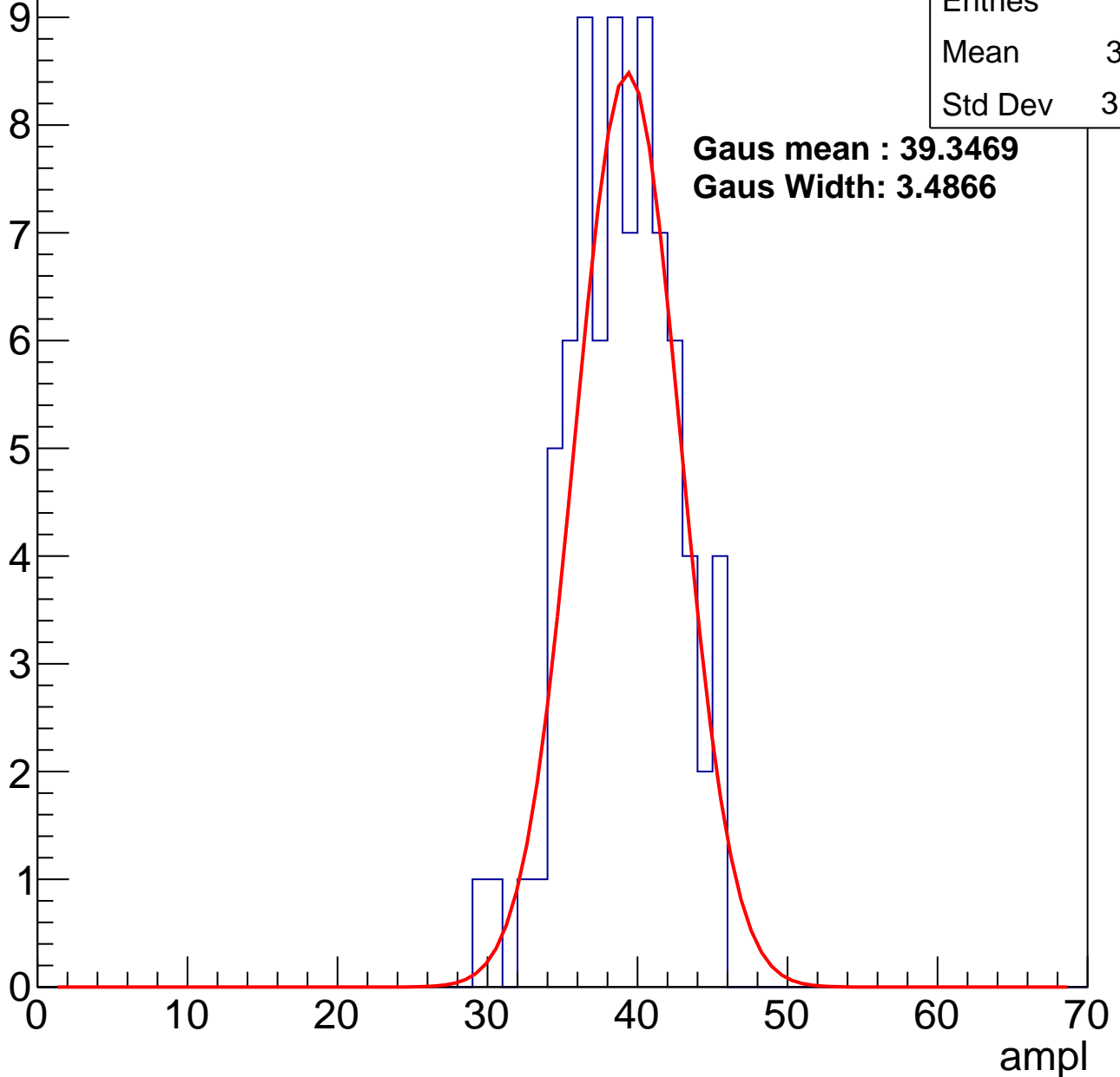
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	78
Mean	38.51
Std Dev	3.456

**Gaus mean : 39.3469**

**Gaus Width: 3.4866**



# B1L003S, U11-ch59, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	61
Mean	45.49
Std Dev	3.312

**Gaus mean : 45.7740**

**Gaus Width: 3.2977**

Entry

10

8

6

4

2

0

0

10

20

30

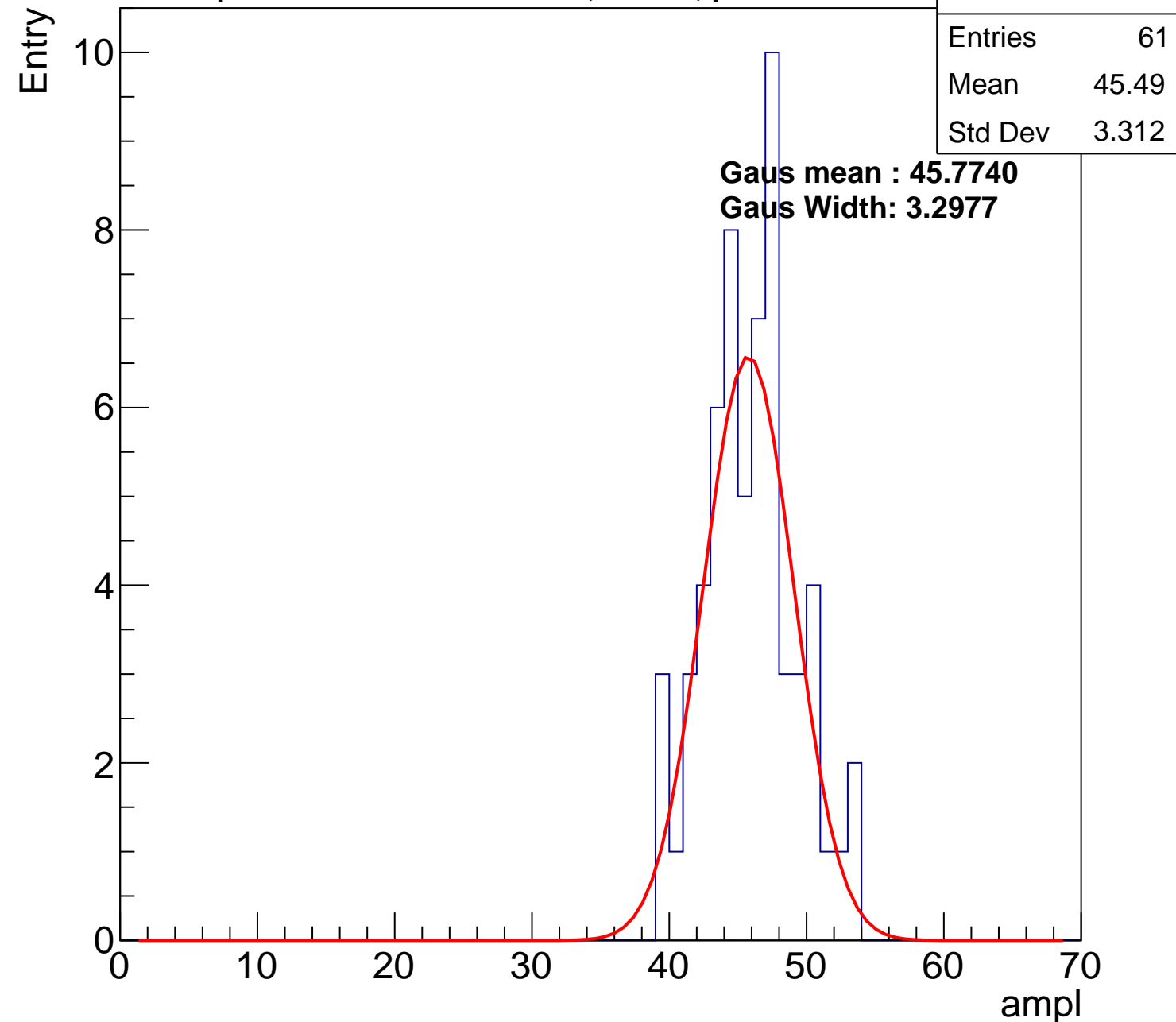
40

50

60

70

ampl

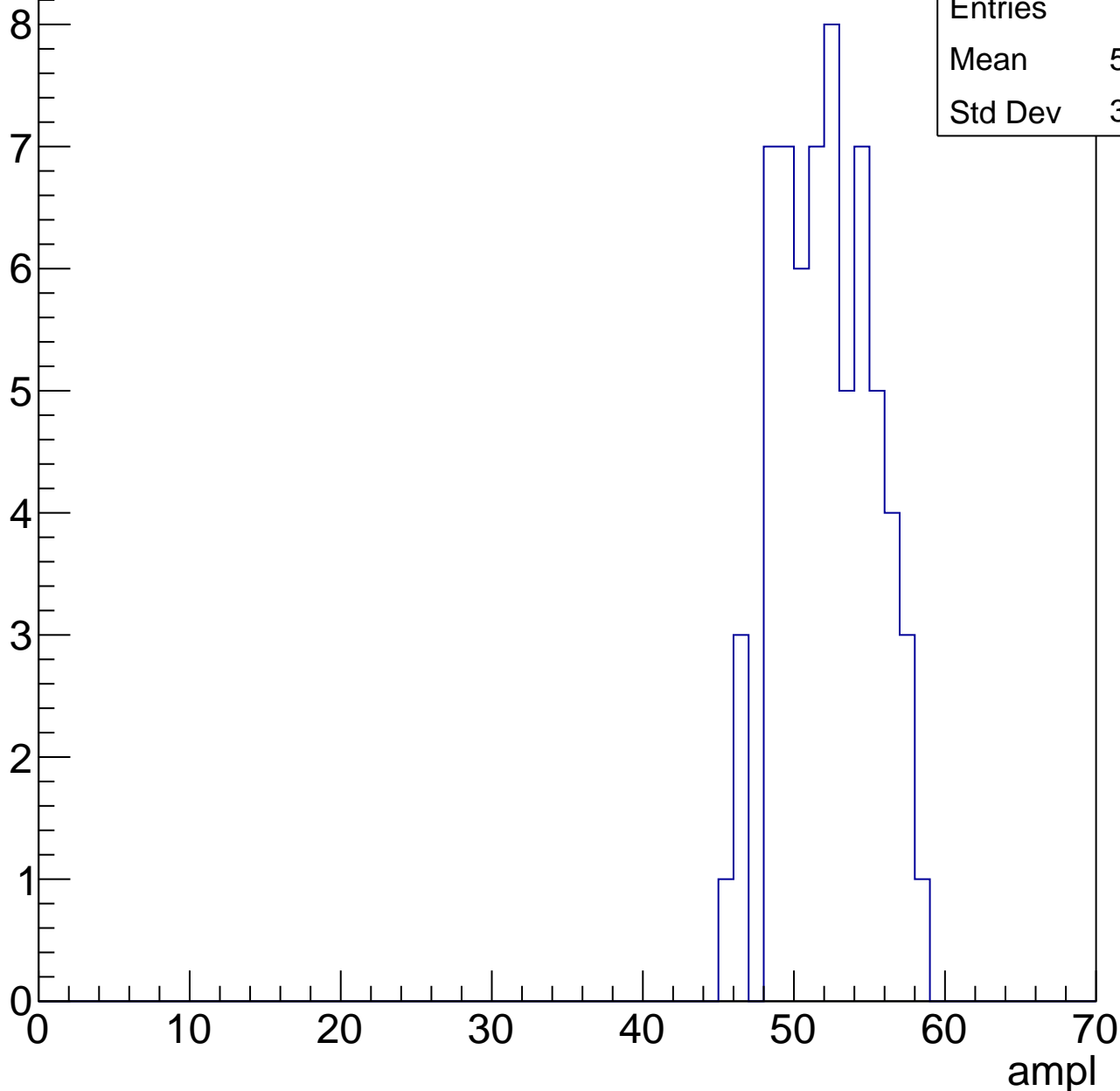


# B1L003S, U11-ch59, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	51.66
Std Dev	3.083



# B1L003S, U11-ch59, adc4

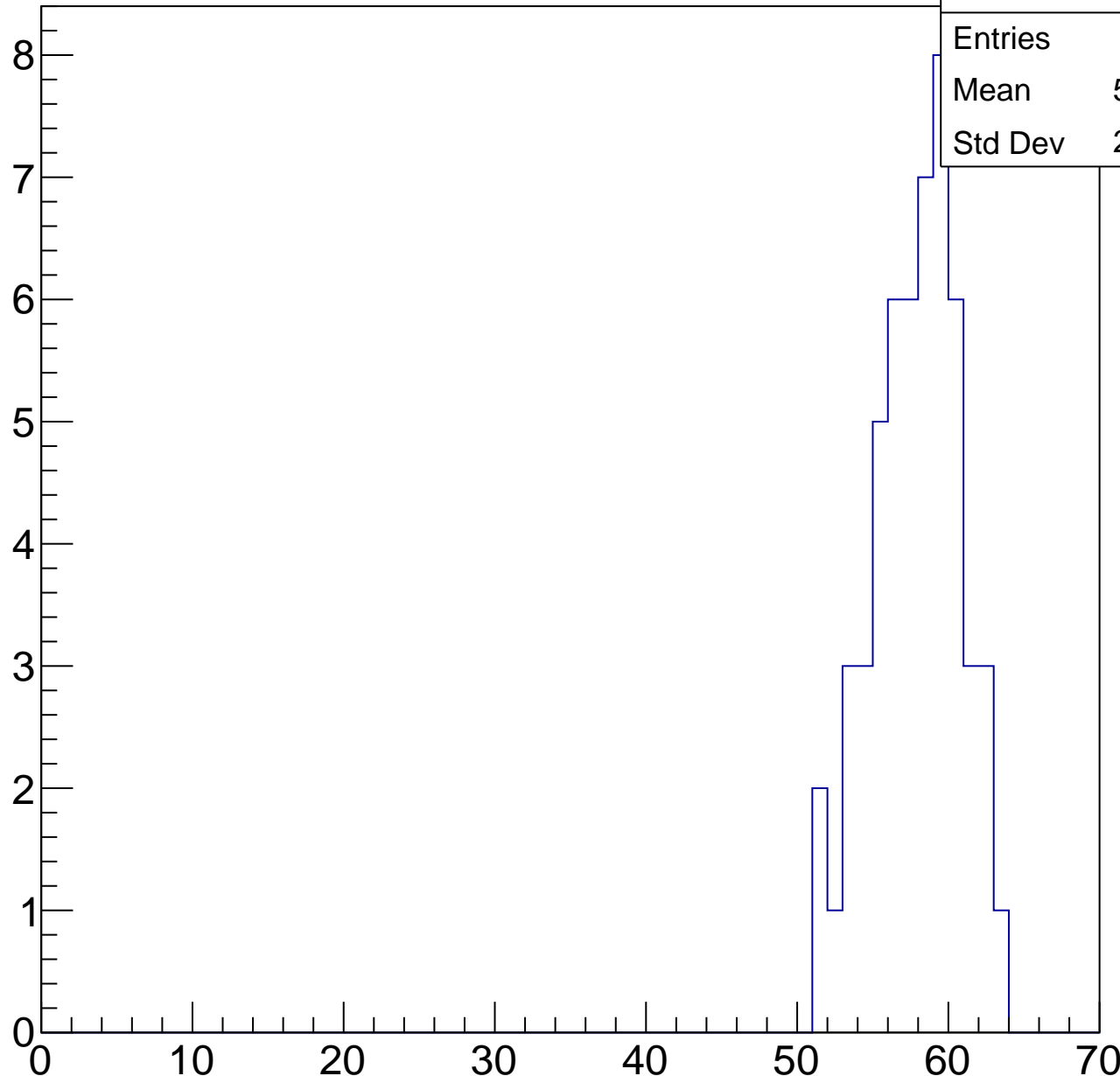
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	54
Mean	57.37
Std Dev	2.863

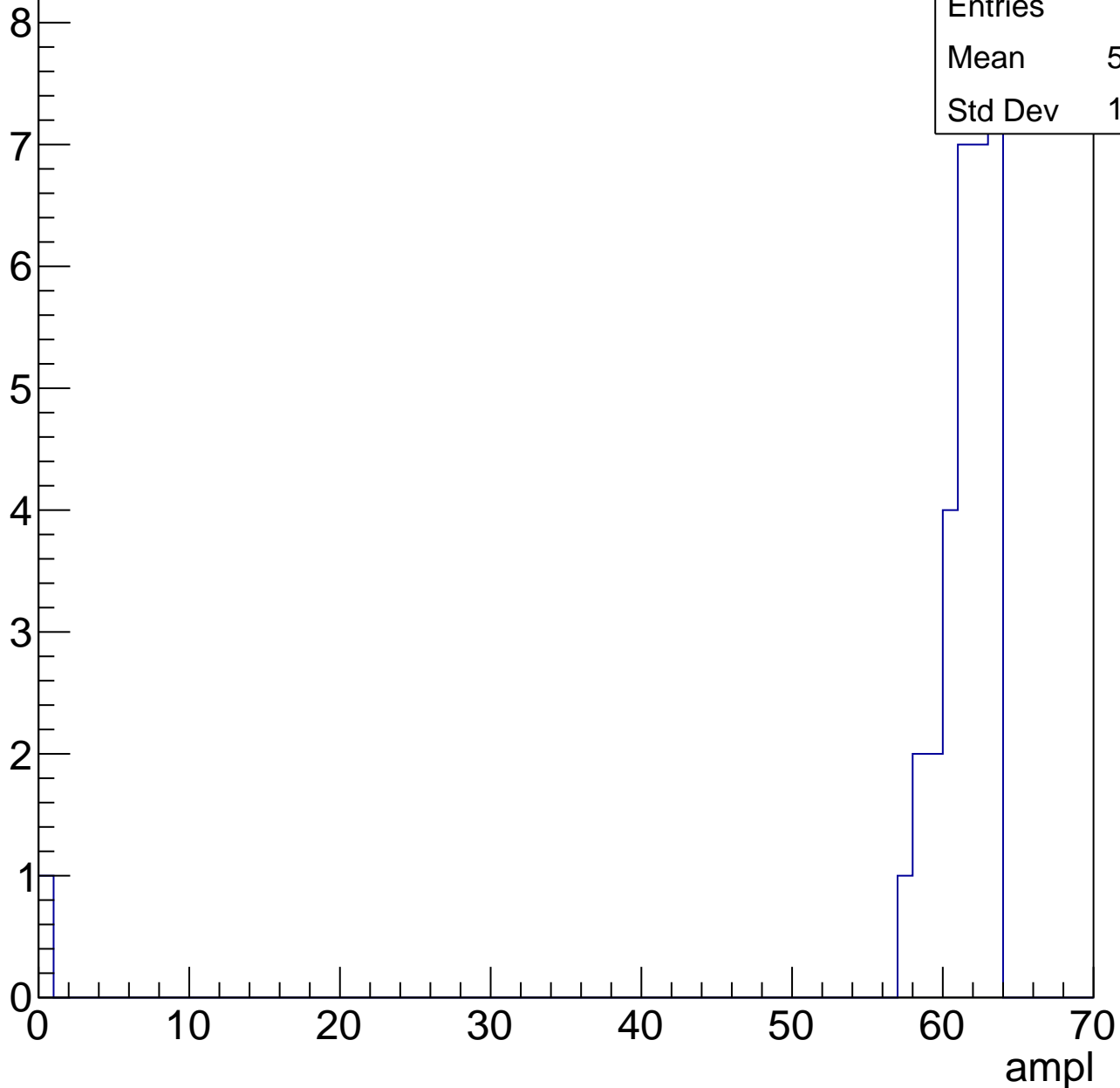
ampl



# B1L003S, U11-ch59, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U11-ch59, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch59, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U11-ch60, adc0

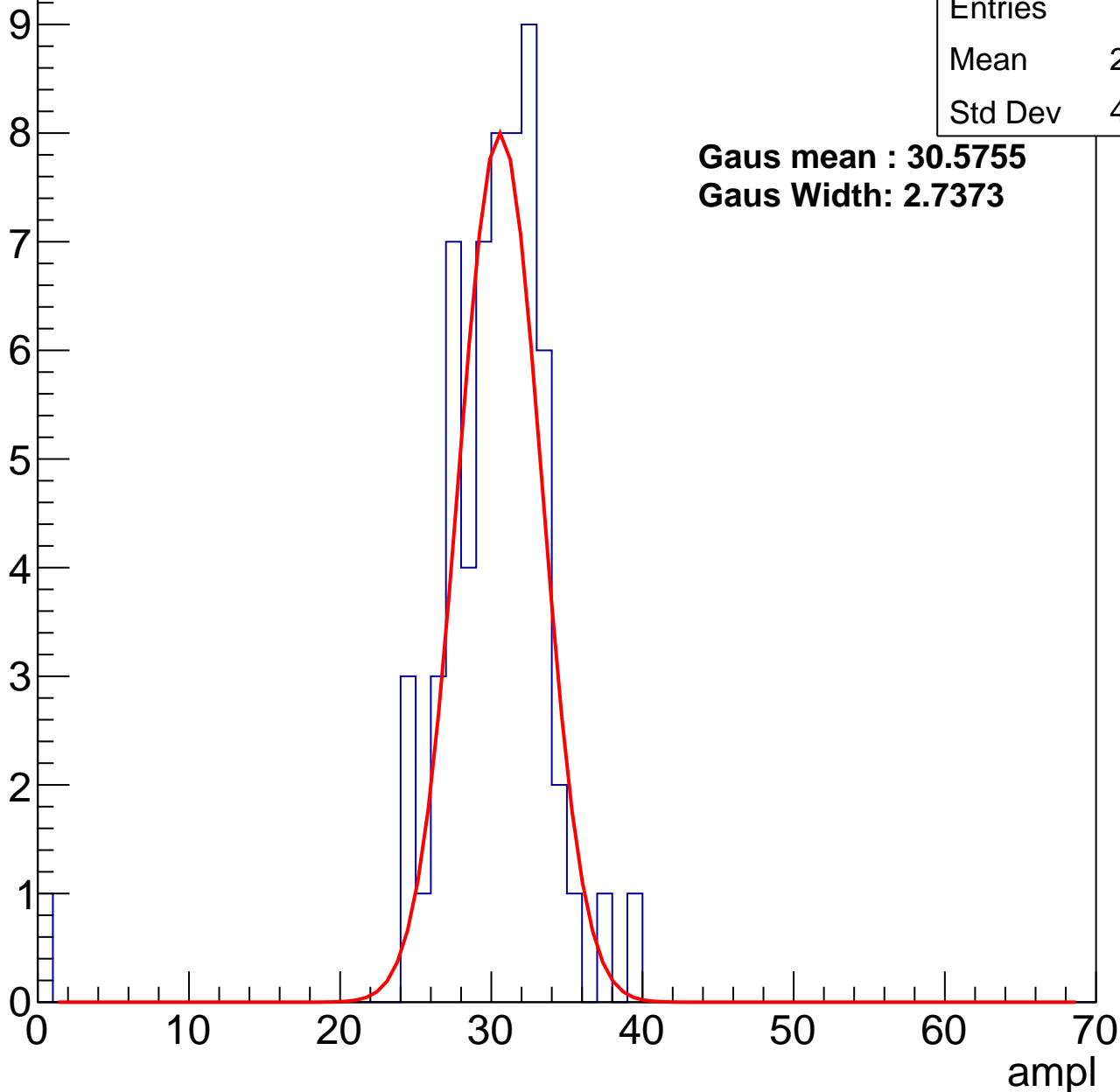
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	29.55
Std Dev	4.818

**Gaus mean : 30.5755**

**Gaus Width: 2.7373**

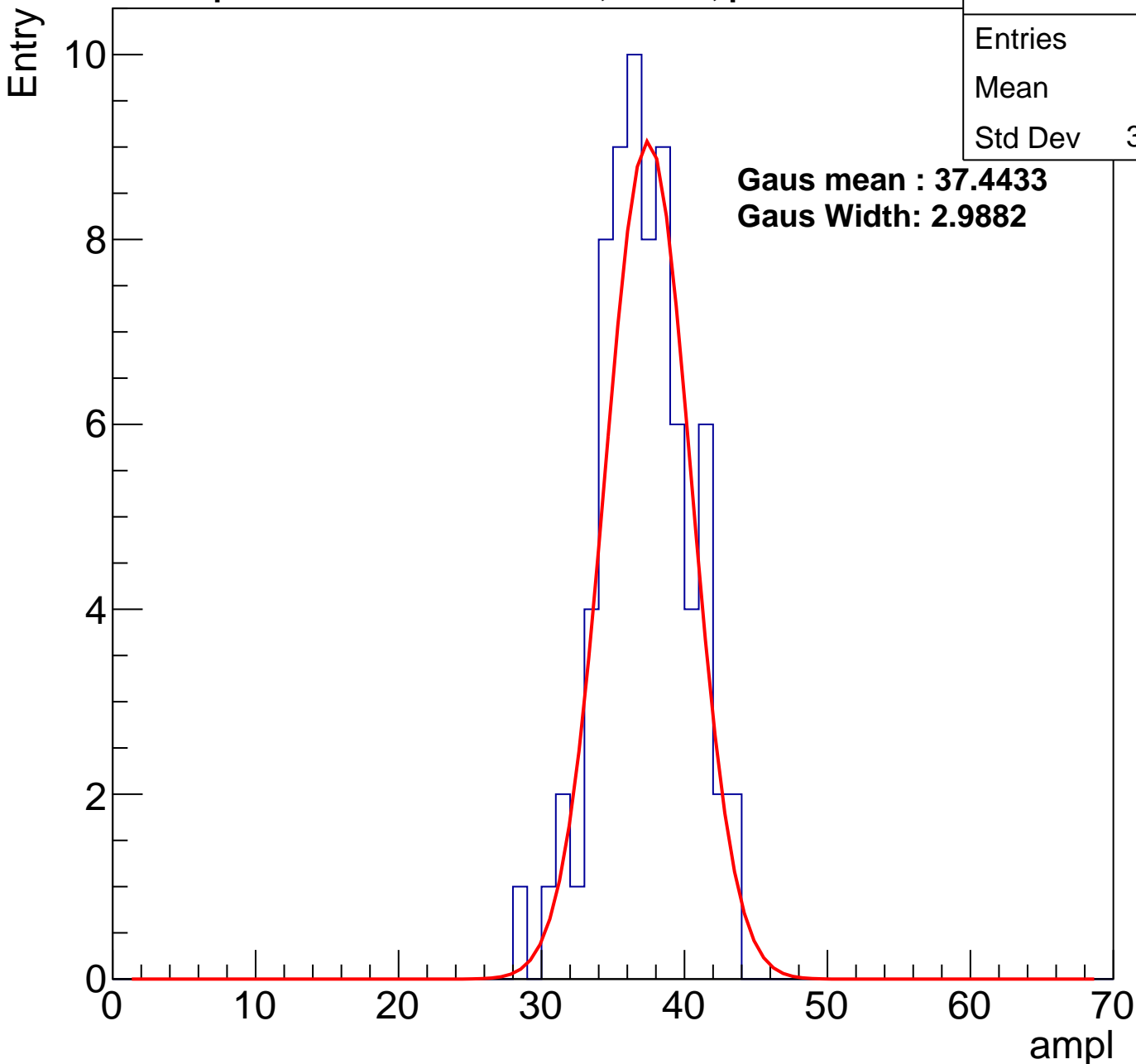


# B1L003S, U11-ch60, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	73
Mean	36.7
Std Dev	3.073

**Gaus mean : 37.4433**  
**Gaus Width: 2.9882**



# B1L003S, U11-ch60, adc2

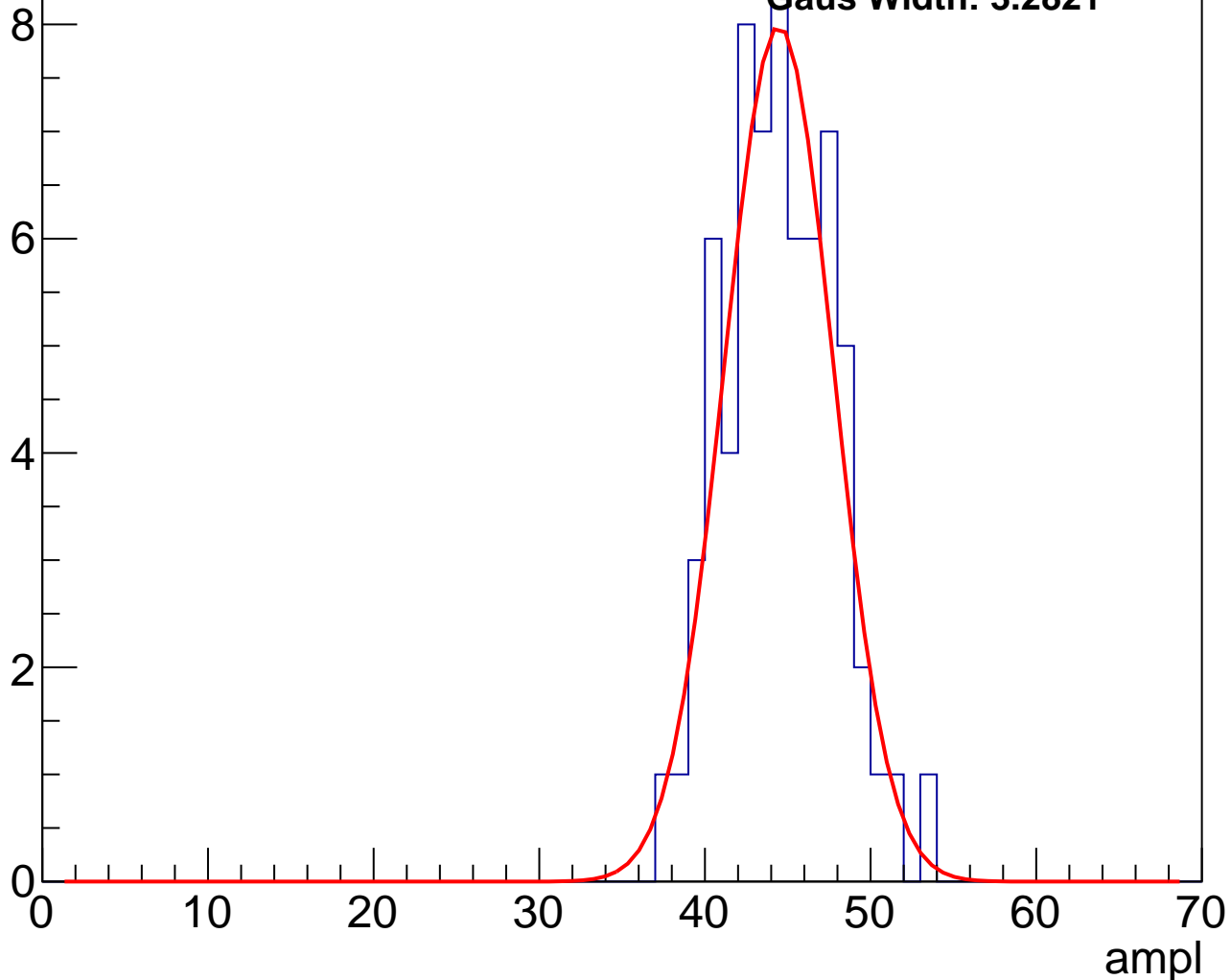
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	44.06
Std Dev	3.23

**Gaus mean : 44.4659**

**Gaus Width: 3.2821**

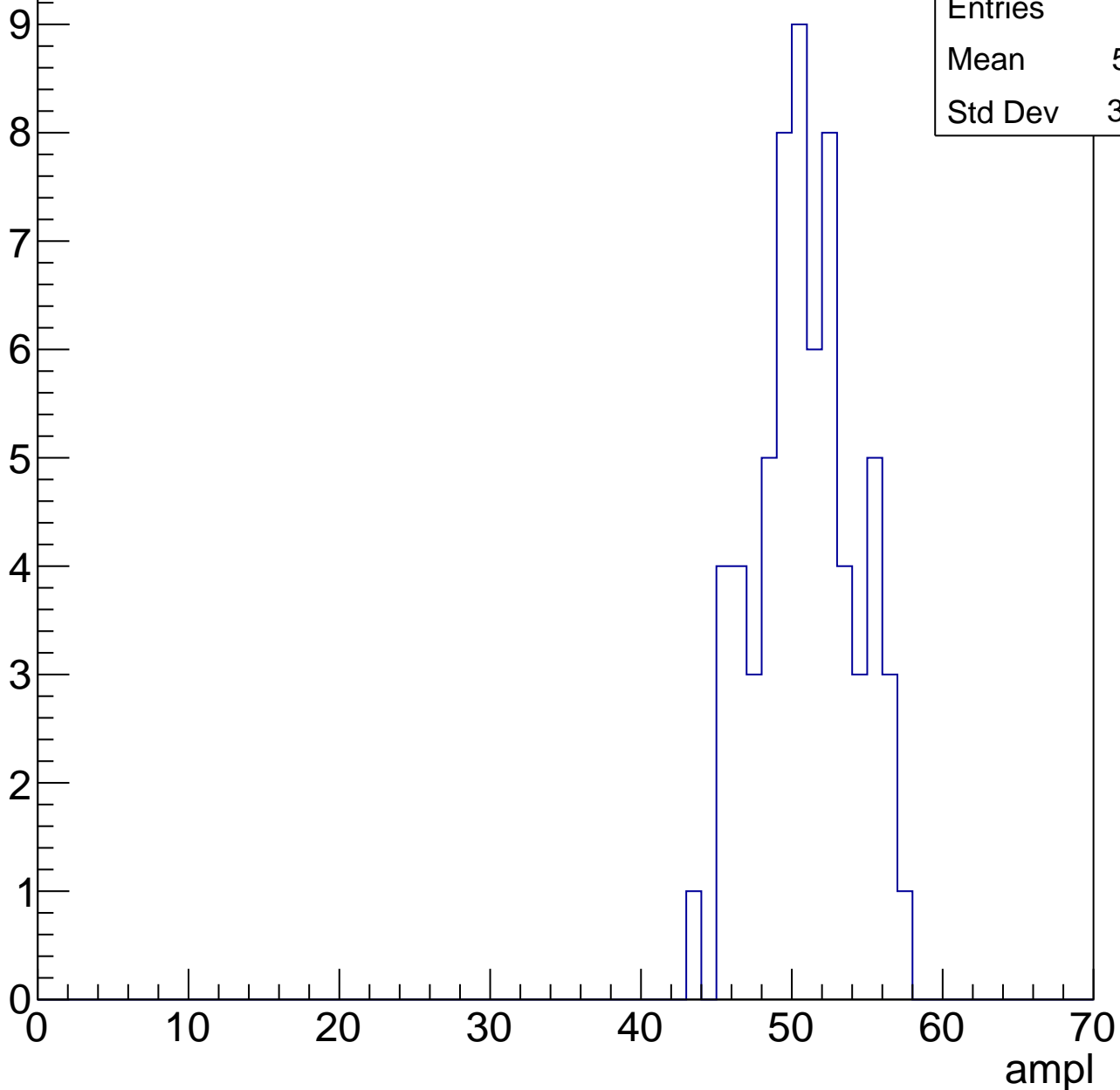


# B1L003S, U11-ch60, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

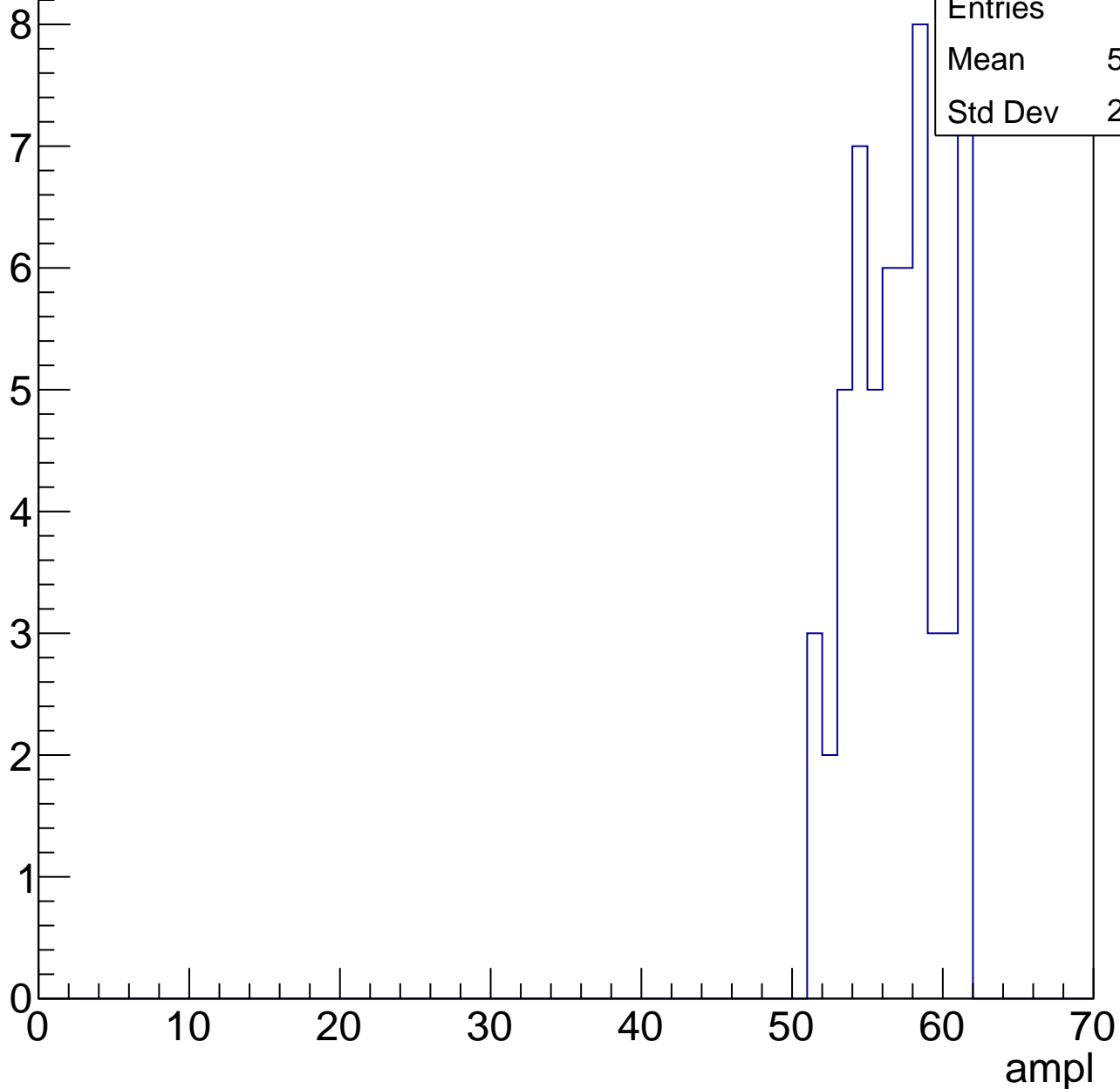
Entries	64
Mean	50.41
Std Dev	3.215



# B1L003S, U11-ch60, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



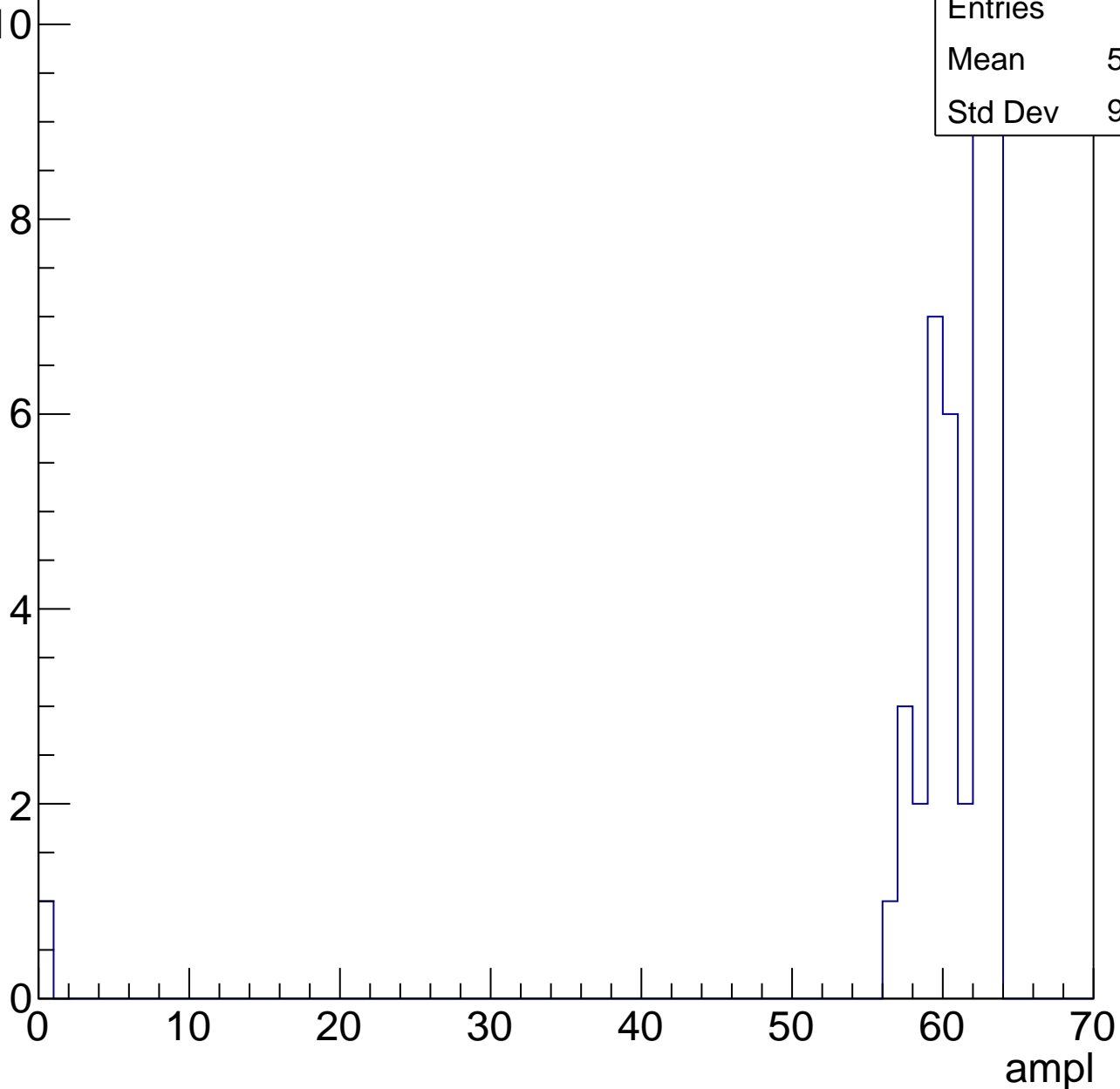
Entries	56
Mean	56.46
Std Dev	2.946

# B1L003S, U11-ch60, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	42
Mean	59.24
Std Dev	9.469



# B1L003S, U11-ch60, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	60
Std Dev	0



# B1L003S, U11-ch60, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U11-ch61, adc0

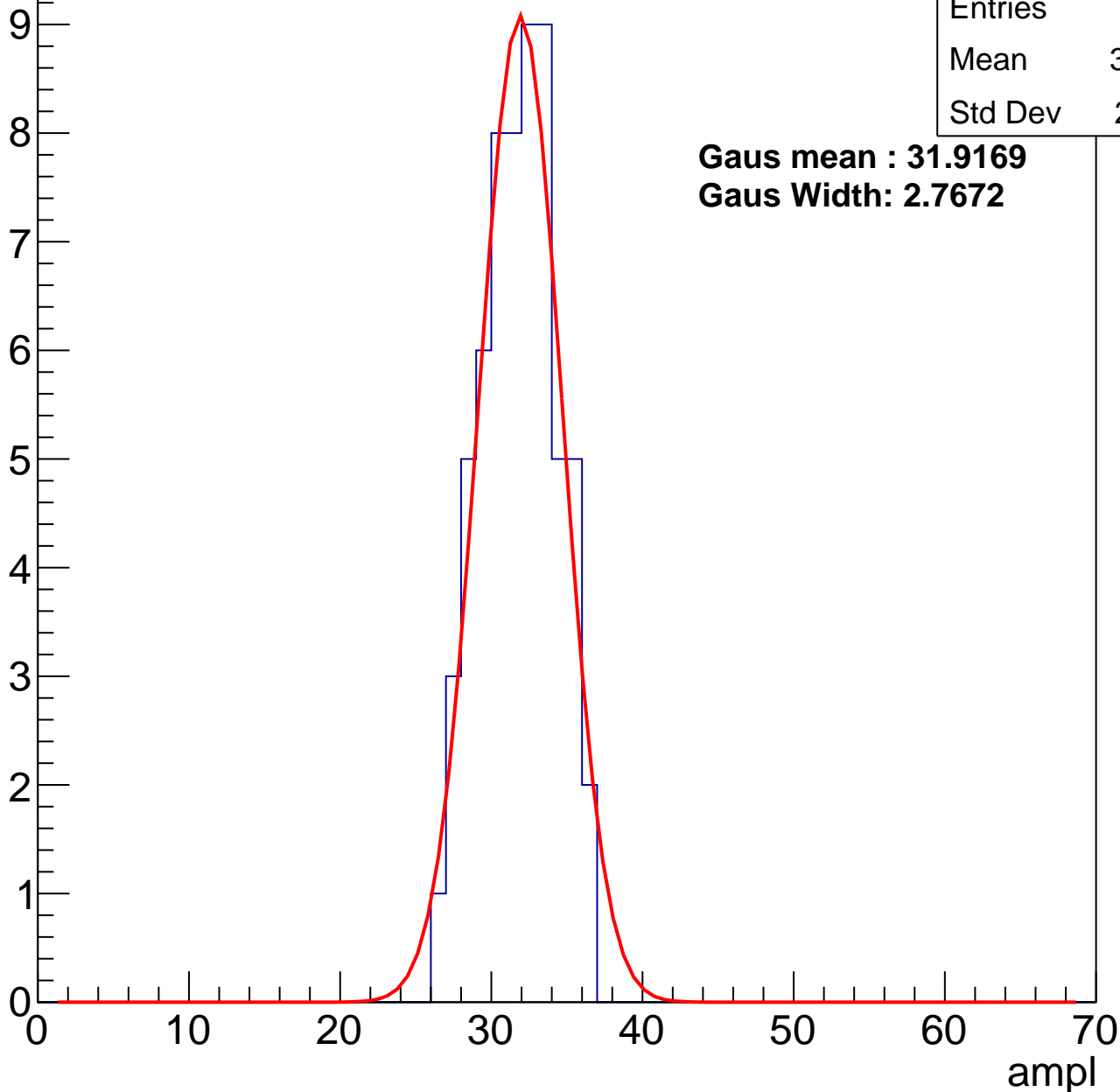
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	31.33
Std Dev	2.441

**Gaus mean : 31.9169**

**Gaus Width: 2.7672**



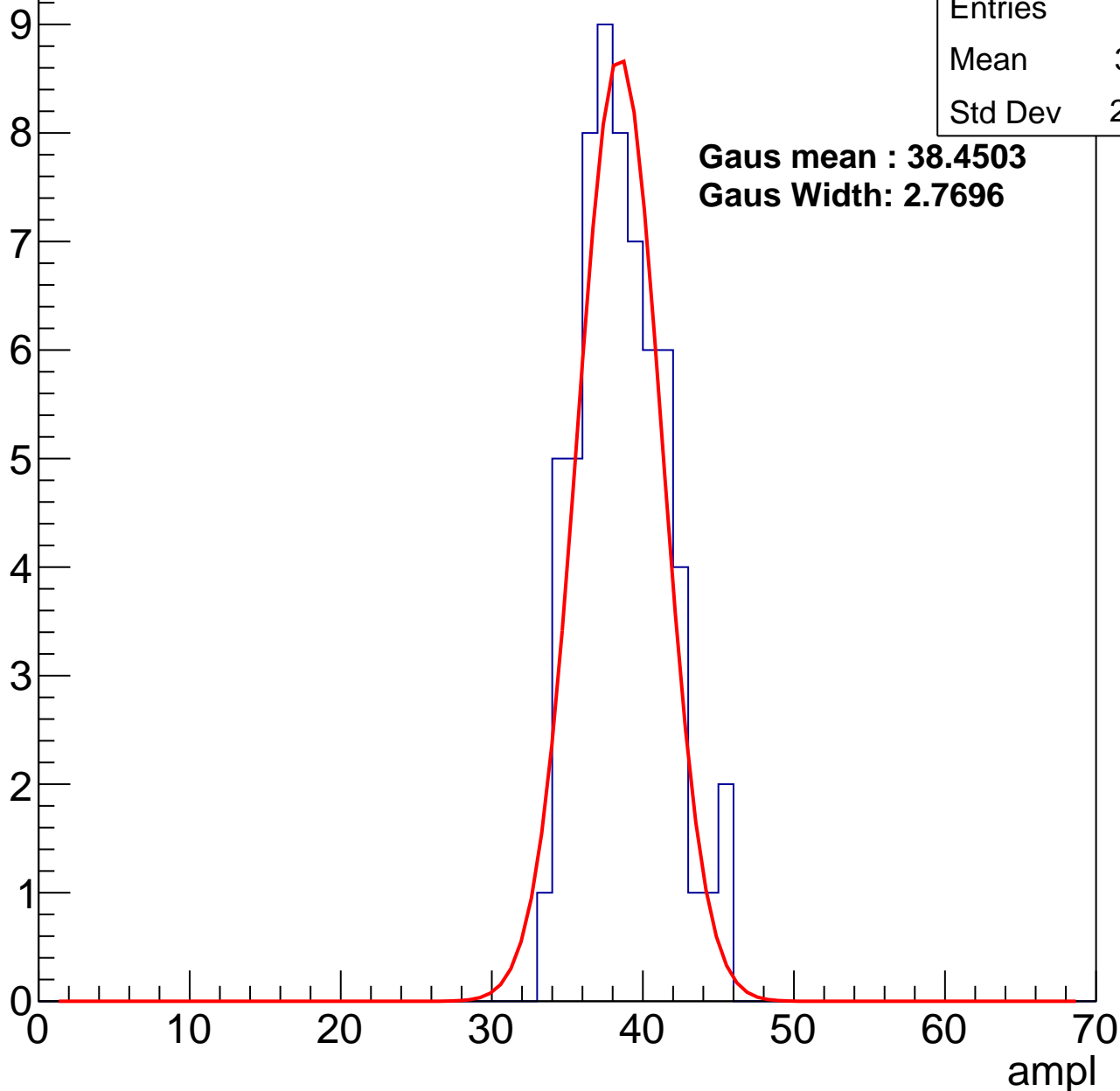
# B1L003S, U11-ch61, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	38.21
Std Dev	2.807

**Gaus mean : 38.4503**  
**Gaus Width: 2.7696**



# B1L003S, U11-ch61, adc2

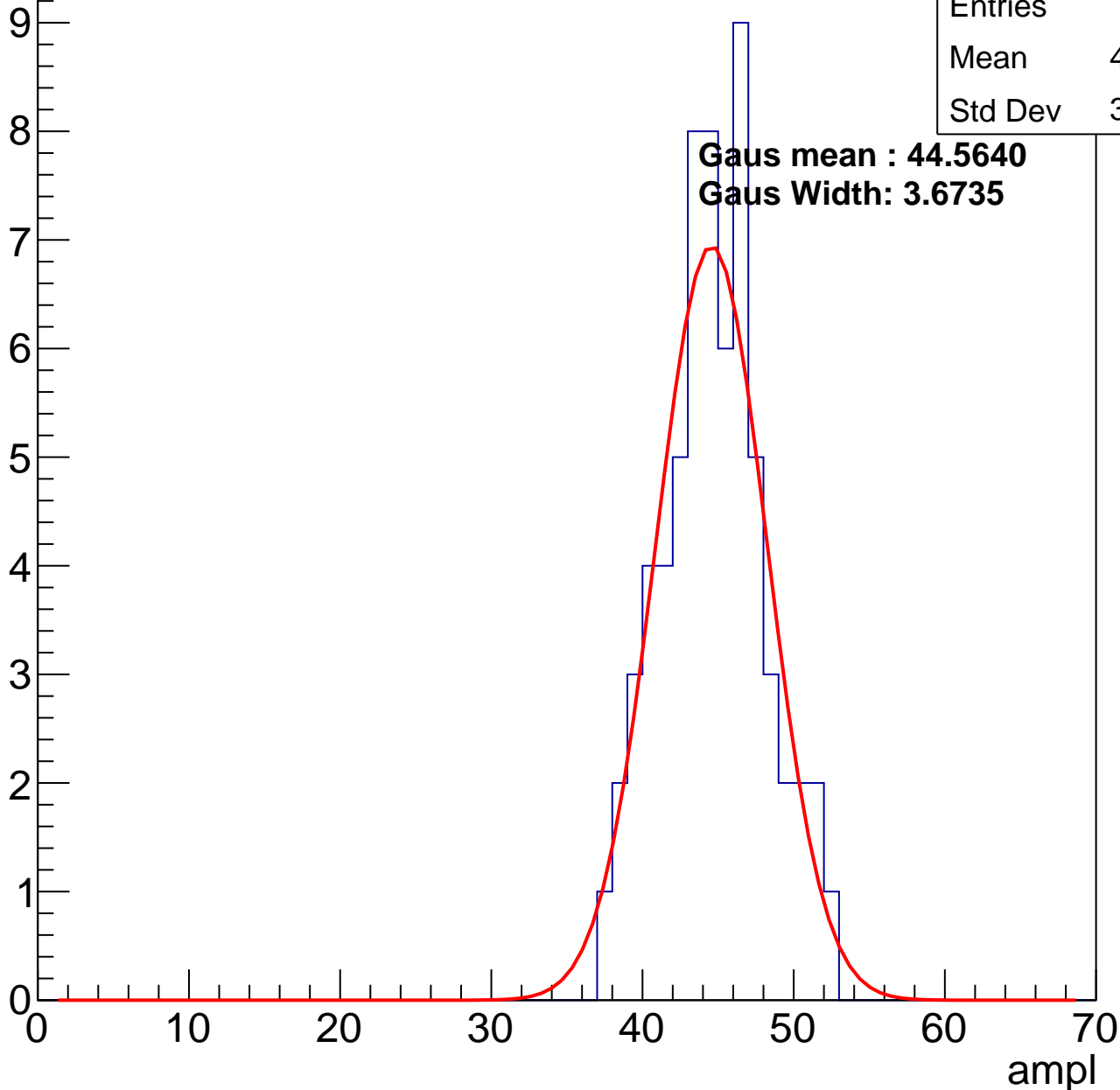
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	44.23
Std Dev	3.373

**Gaus mean : 44.5640**

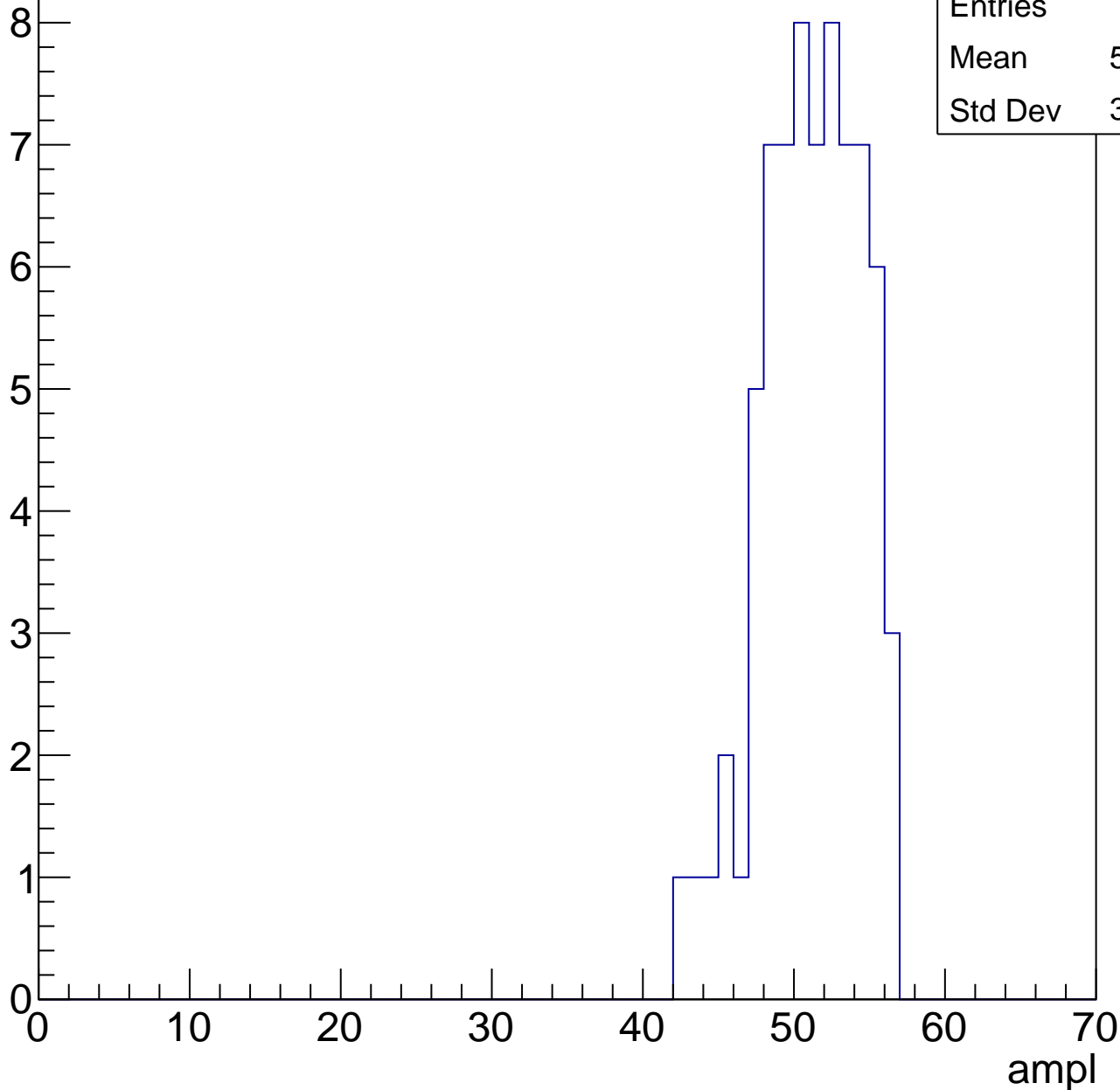
**Gaus Width: 3.6735**



# B1L003S, U11-ch61, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



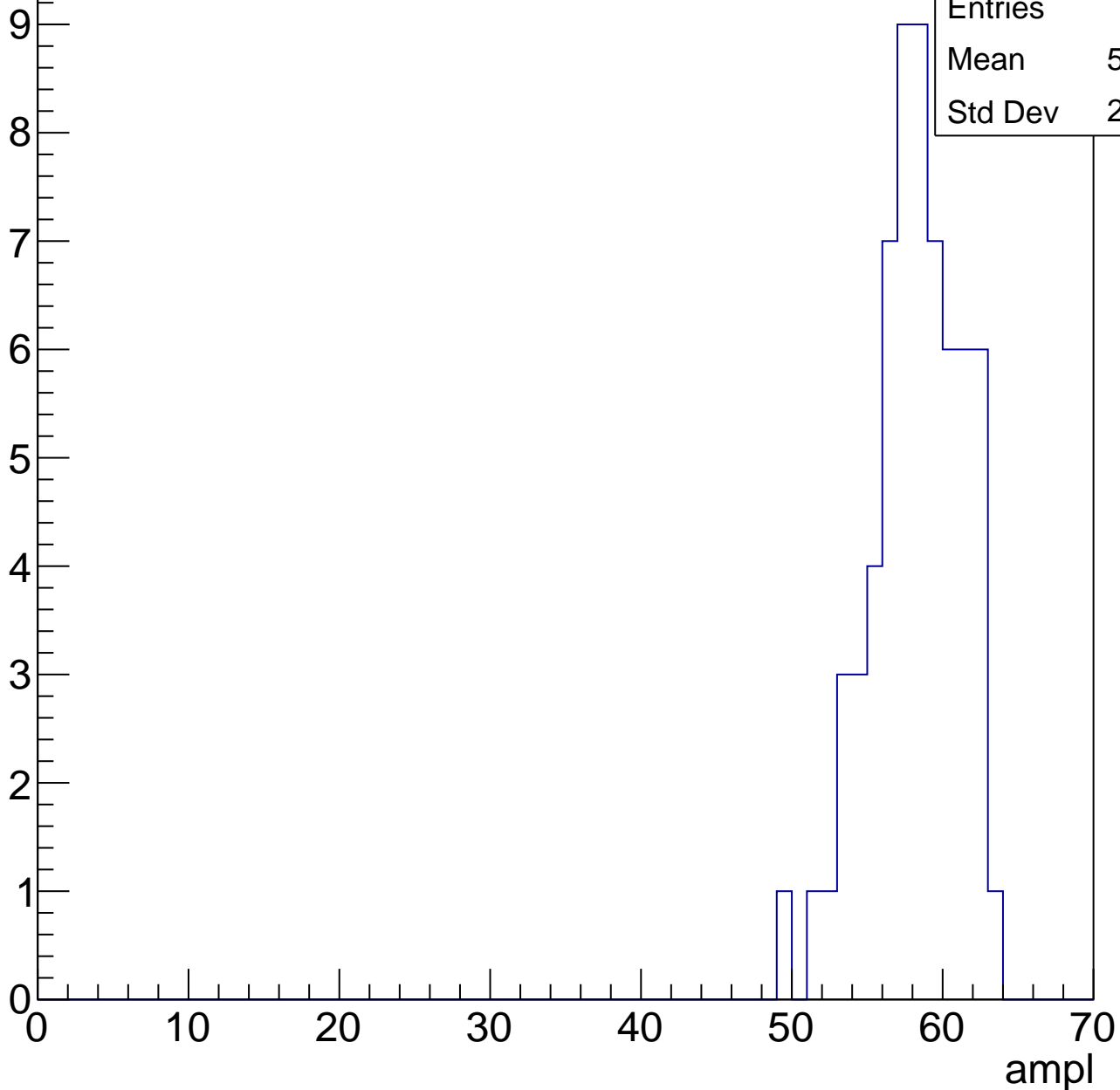
Entries	71
Mean	50.69
Std Dev	3.213

# B1L003S, U11-ch61, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	57.72
Std Dev	2.966

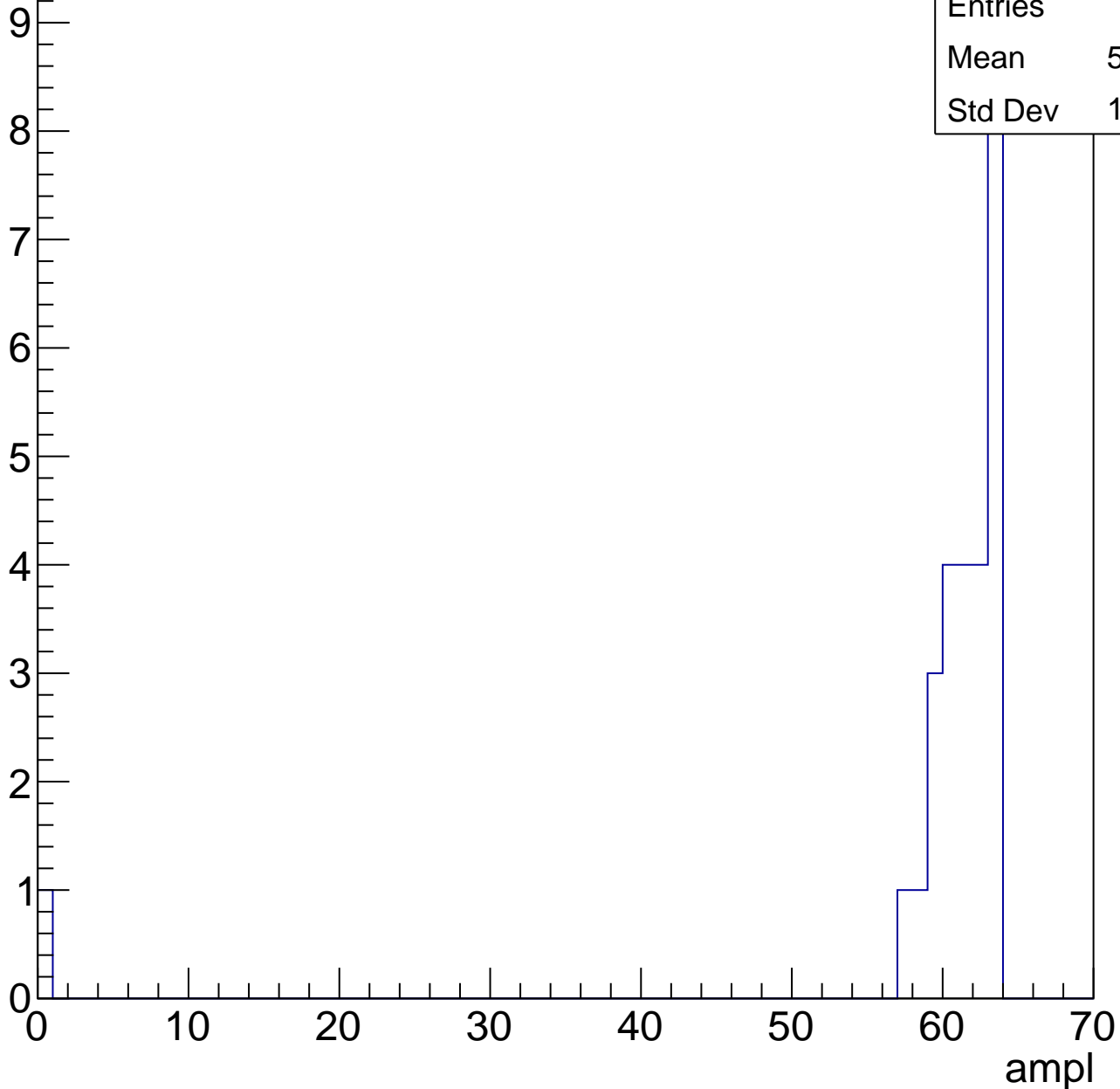


# B1L003S, U11-ch61, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	27
Mean	58.93
Std Dev	11.68



# B1L003S, U11-ch61, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L003S, U11-ch61, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U11-ch62, adc0

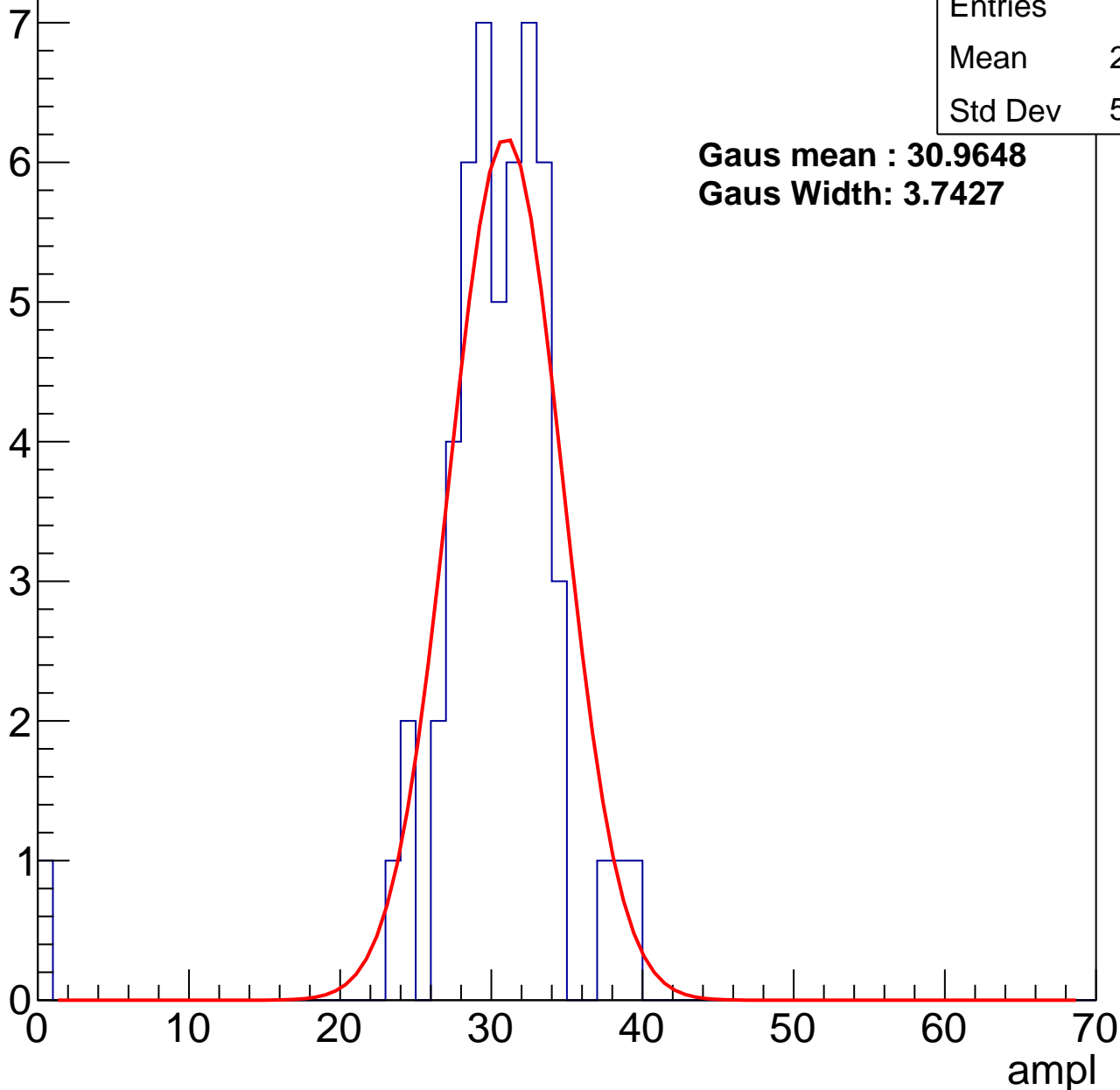
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	29.74
Std Dev	5.224

**Gaus mean : 30.9648**

**Gaus Width: 3.7427**

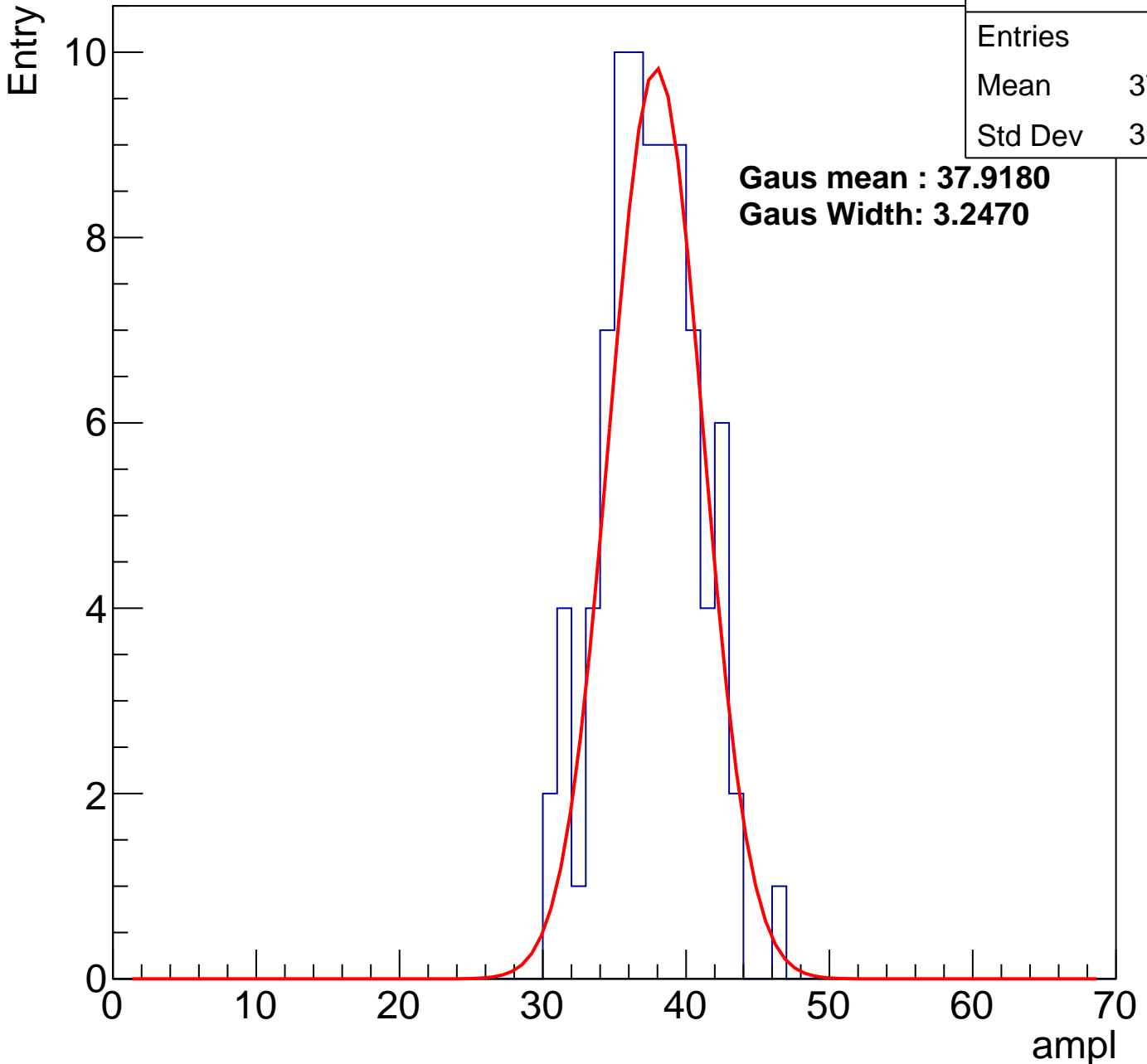


# B1L003S, U11-ch62, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	85
Mean	37.06
Std Dev	3.288

**Gaus mean : 37.9180**  
**Gaus Width: 3.2470**



# B1L003S, U11-ch62, adc2

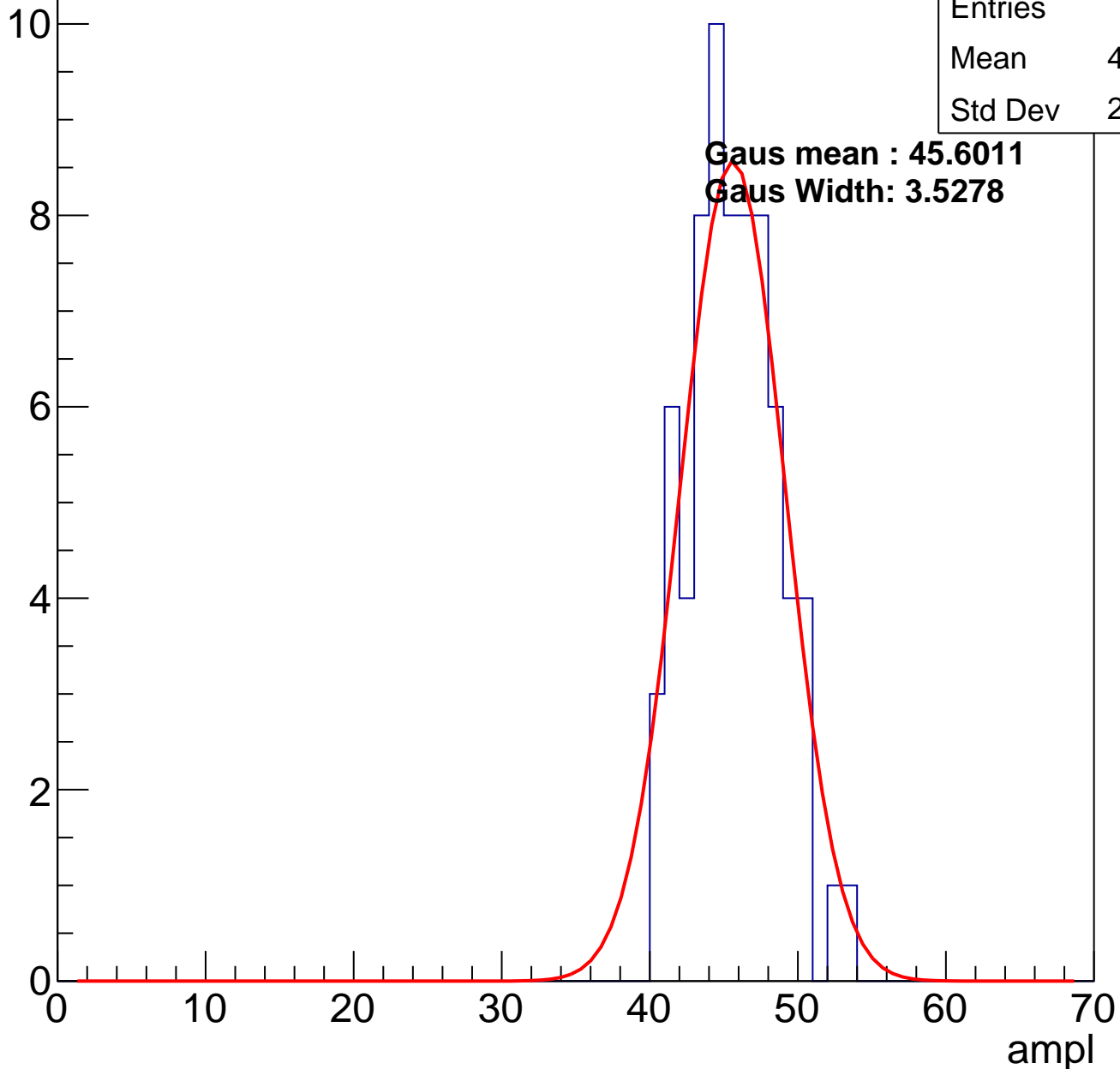
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	71
Mean	45.23
Std Dev	2.946

**Gaus mean : 45.6011**

**Gaus Width: 3.5278**

Entry

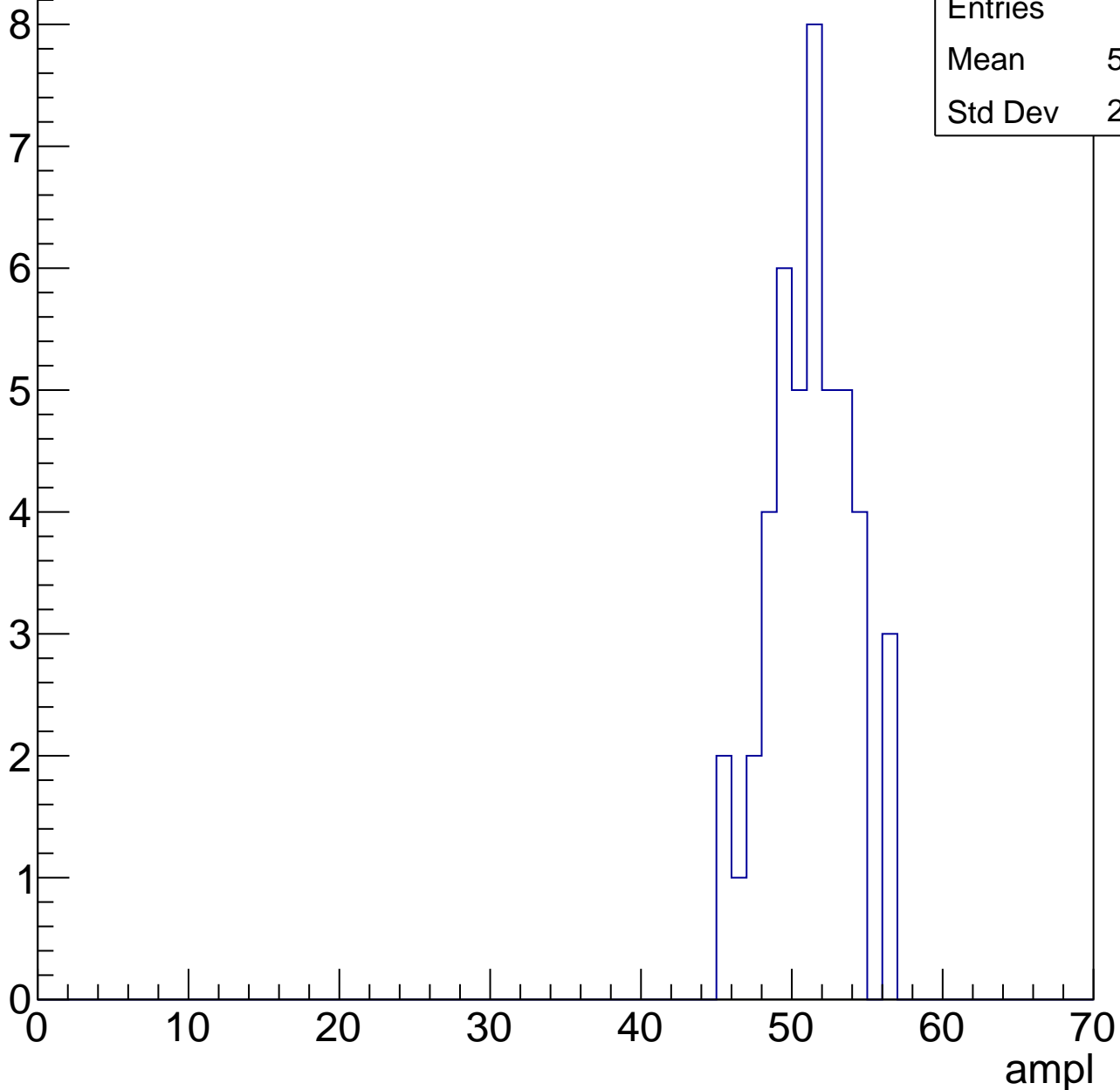


# B1L003S, U11-ch62, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	45
Mean	50.73
Std Dev	2.695

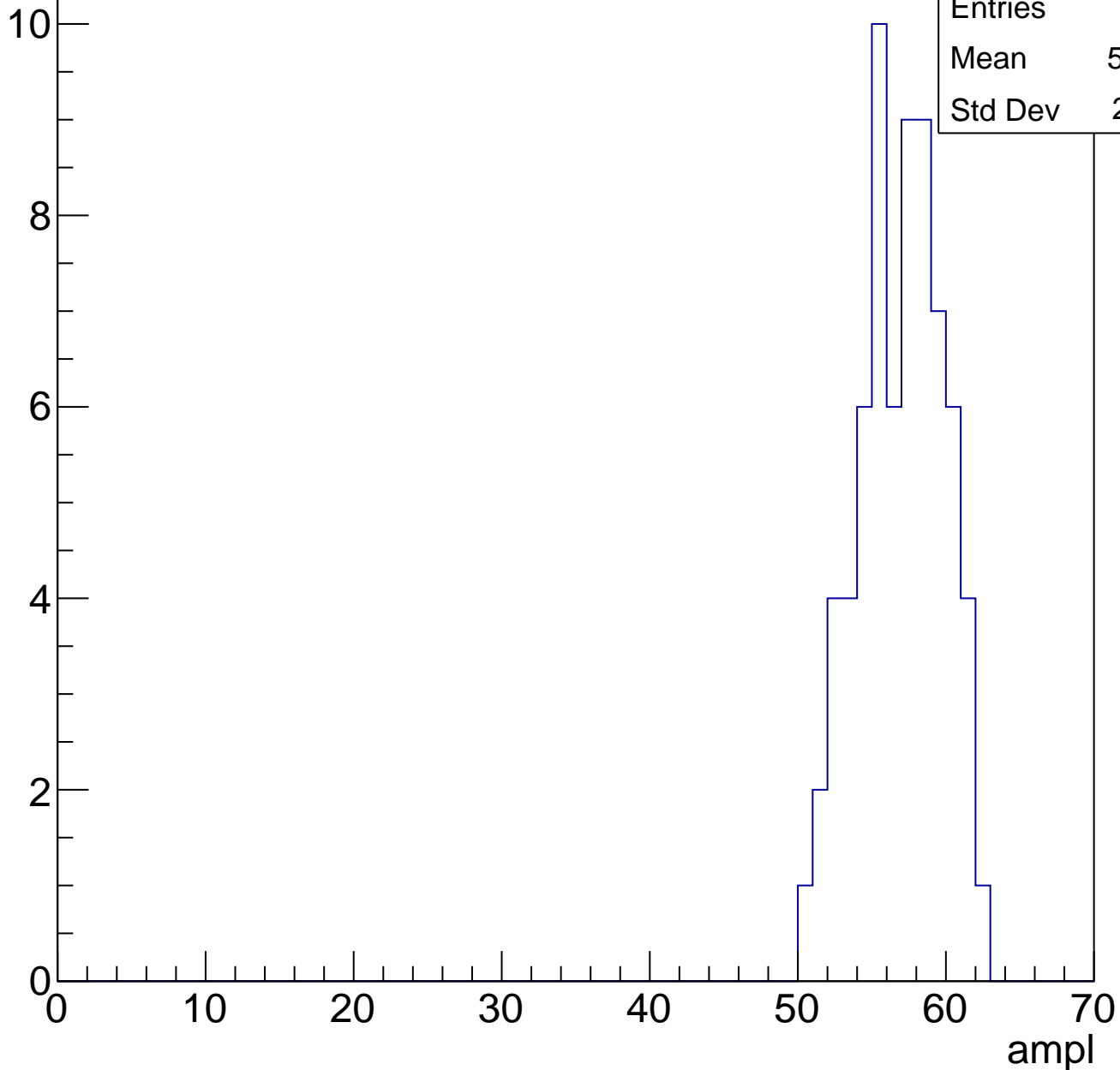


# B1L003S, U11-ch62, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	69
Mean	56.46
Std Dev	2.811

Entry

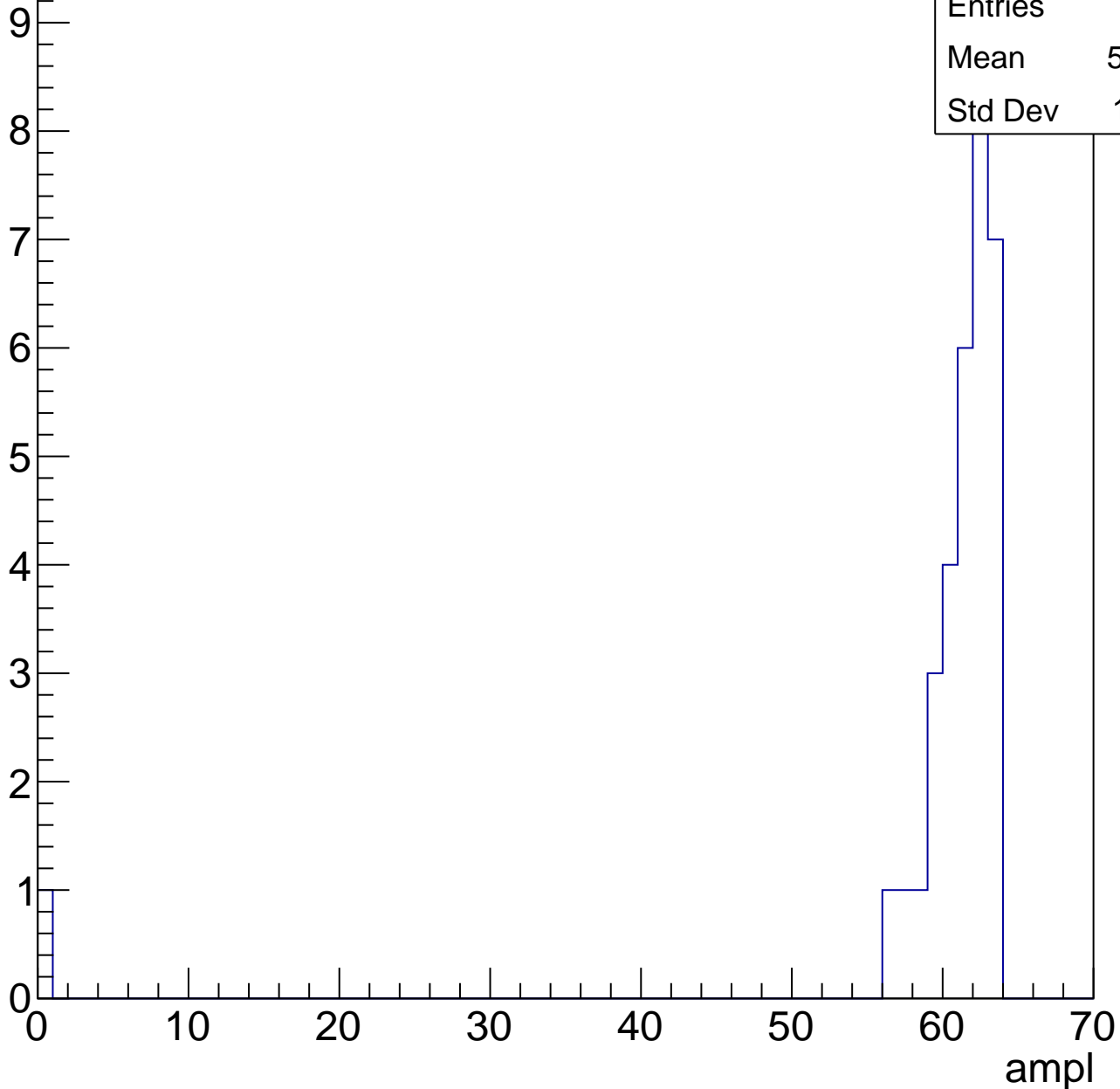


# B1L003S, U11-ch62, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	33
Mean	59.18
Std Dev	10.61



# B1L003S, U11-ch62, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

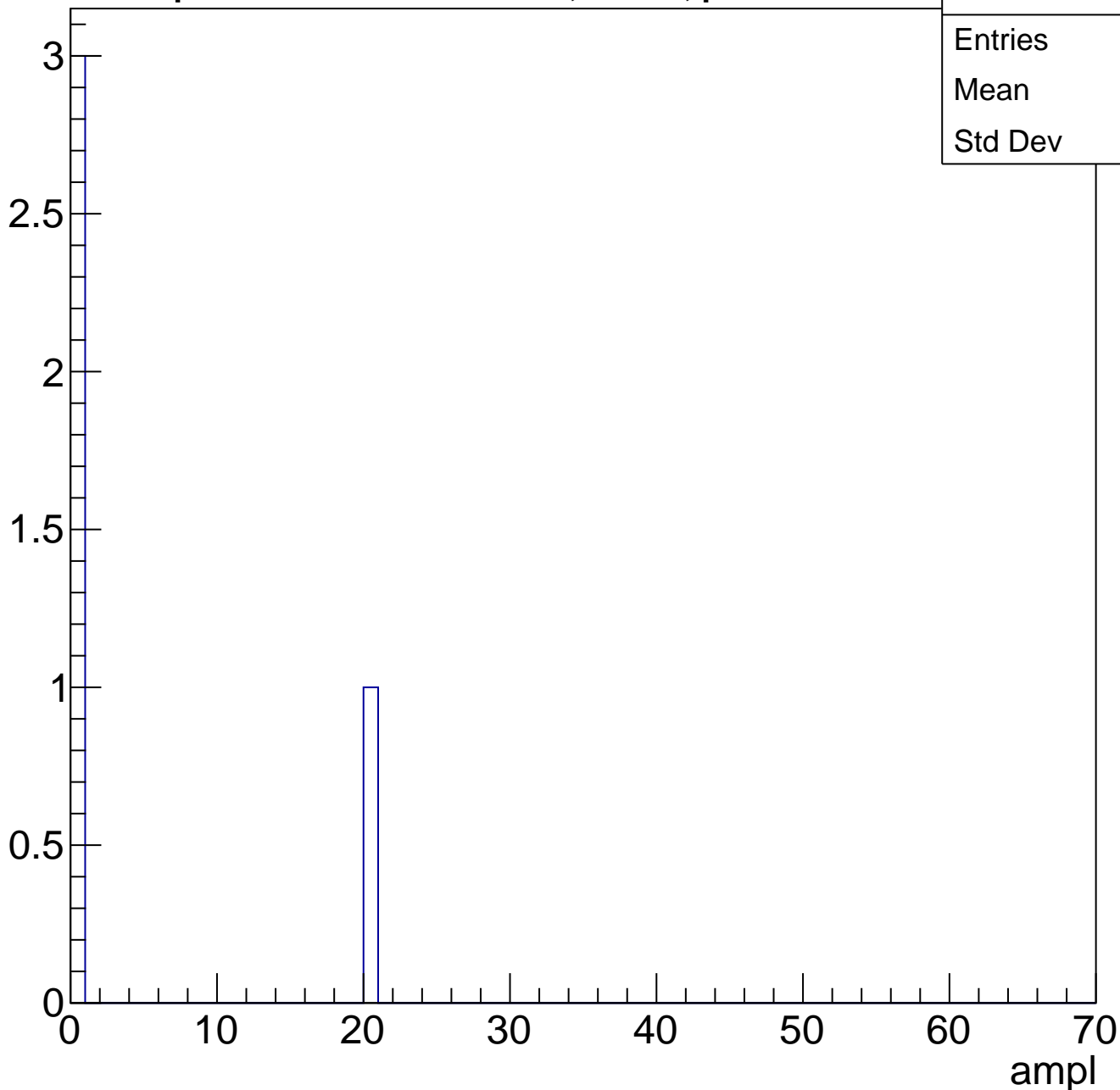




# B1L003S, U11-ch62, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	4
Mean	5
Std Dev	8.66

# B1L003S, U11-ch63, adc0

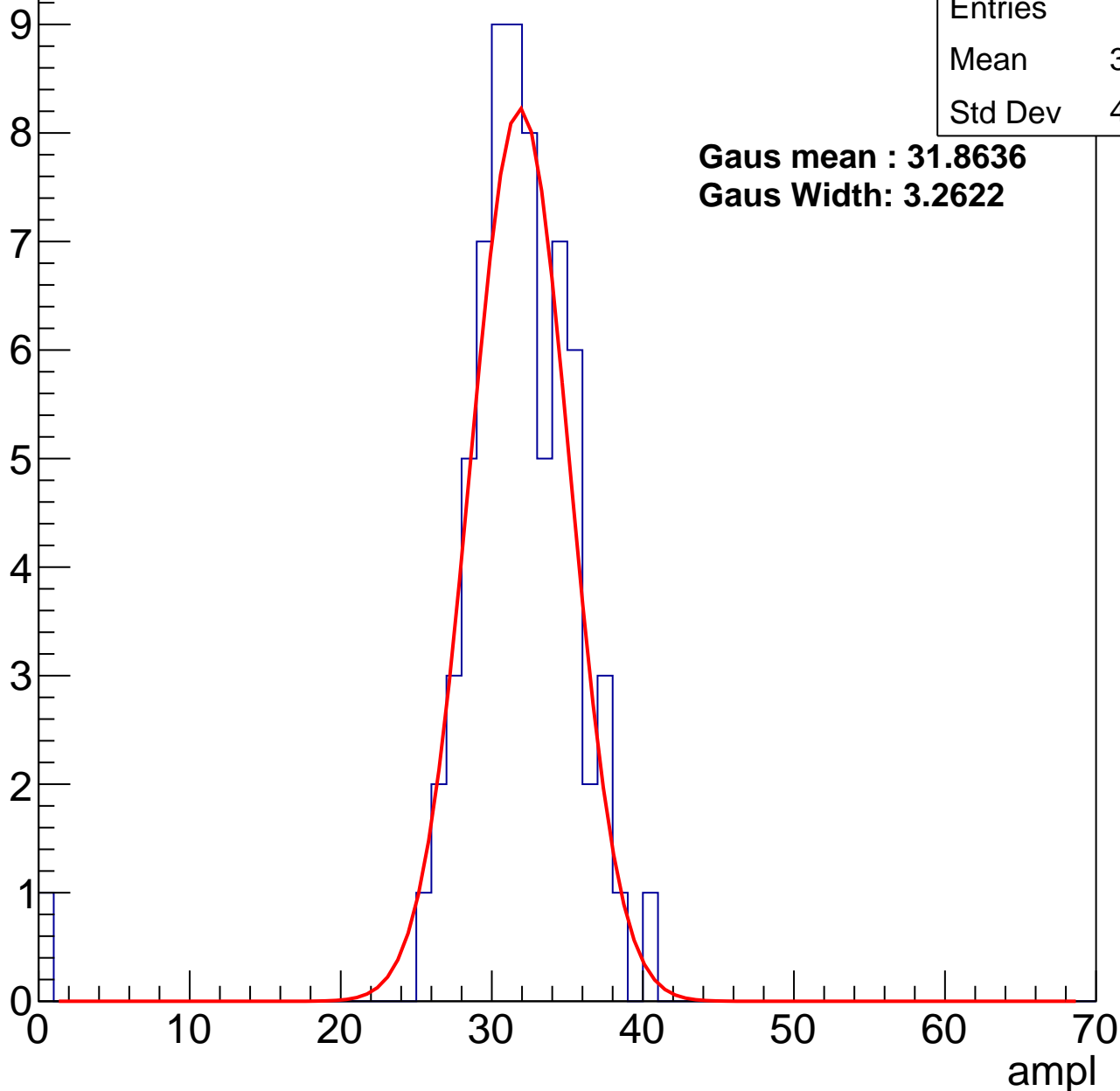
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	31.14
Std Dev	4.856

**Gaus mean : 31.8636**

**Gaus Width: 3.2622**



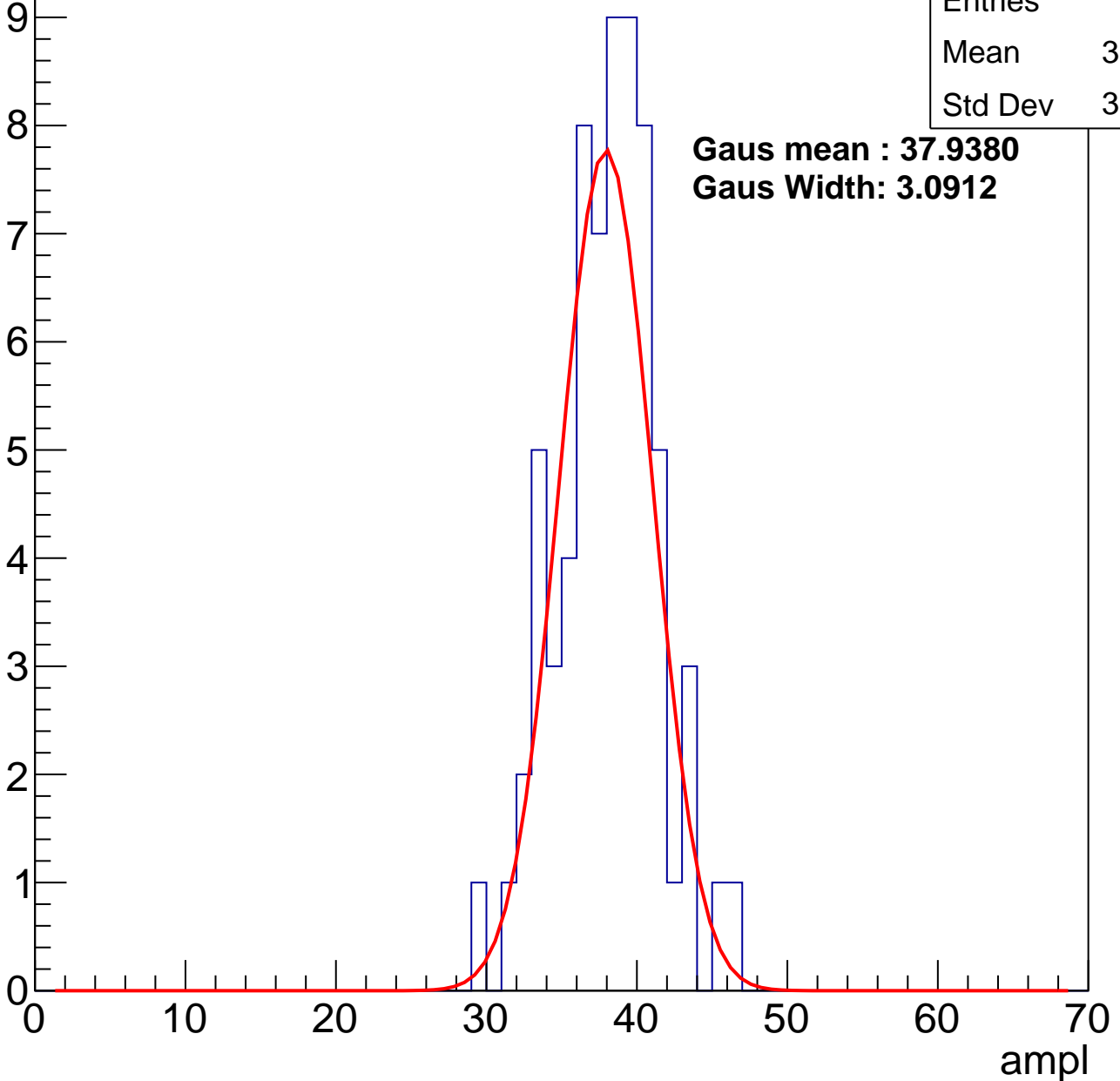
# B1L003S, U11-ch63, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	37.62
Std Dev	3.277

**Gaus mean : 37.9380**  
**Gaus Width: 3.0912**



# B1L003S, U11-ch63, adc2

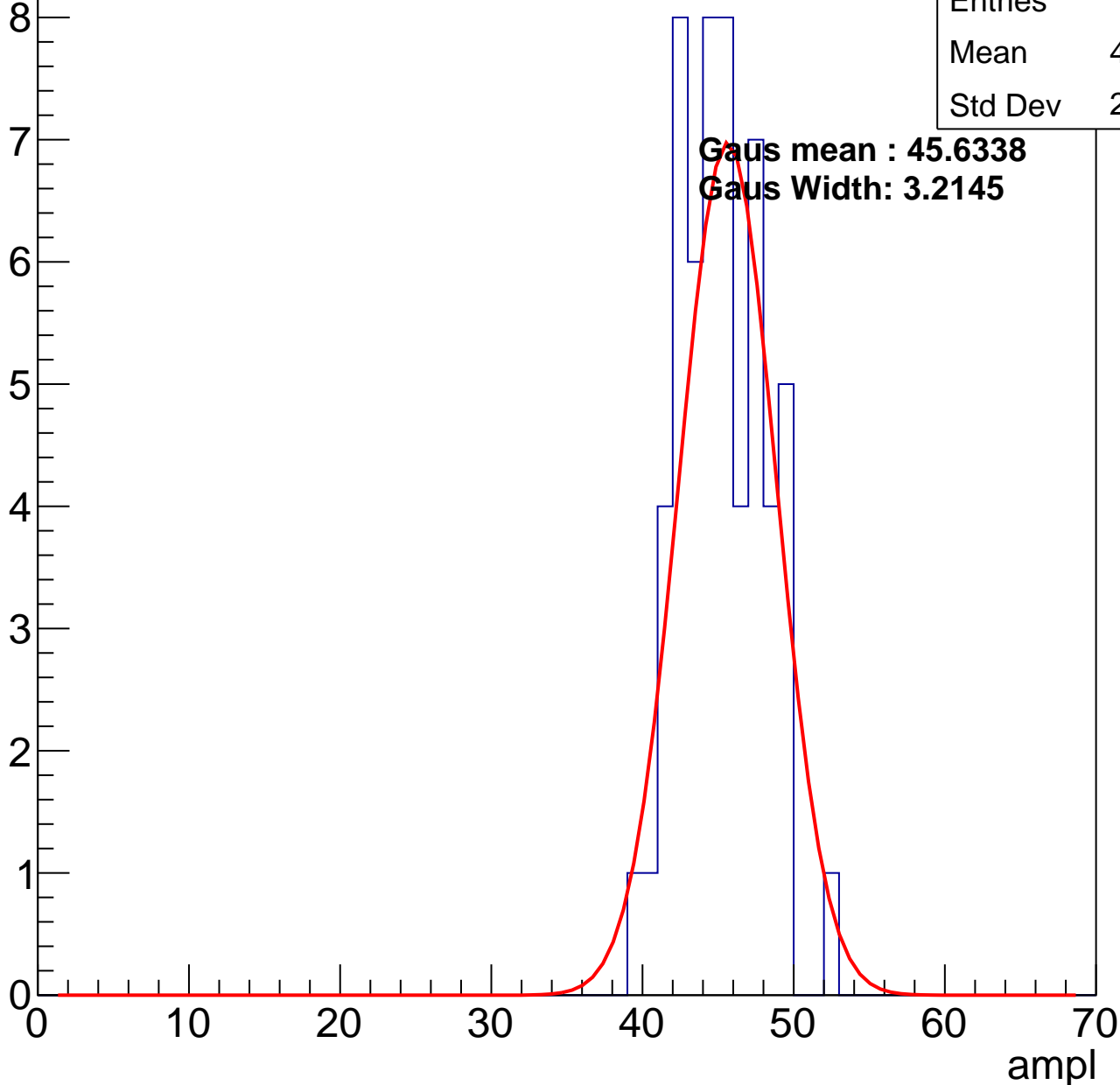
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	44.75
Std Dev	2.723

**Gaus mean : 45.6338**

**Gaus Width: 3.2145**

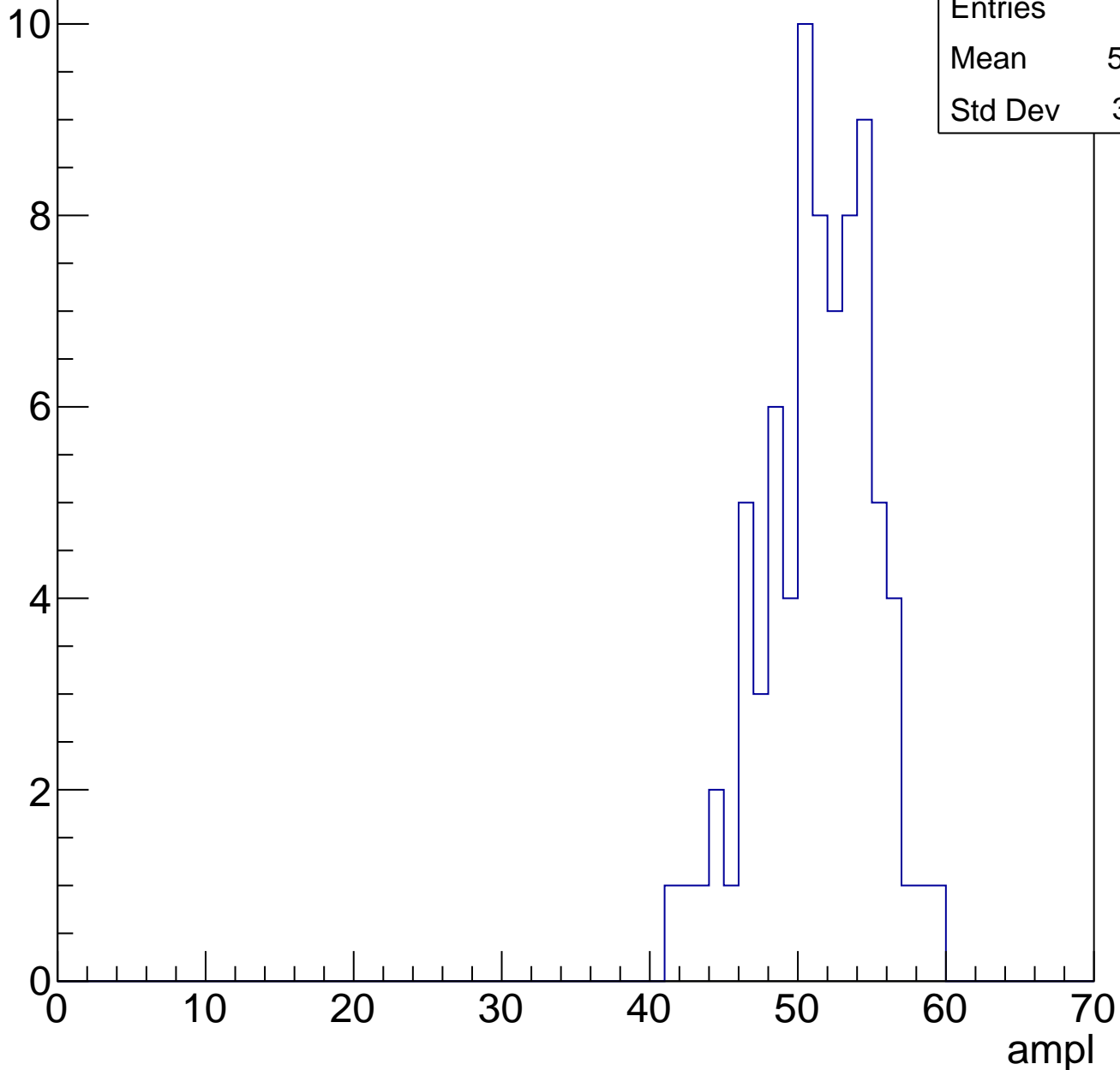


# B1L003S, U11-ch63, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	78
Mean	50.88
Std Dev	3.721

Entry

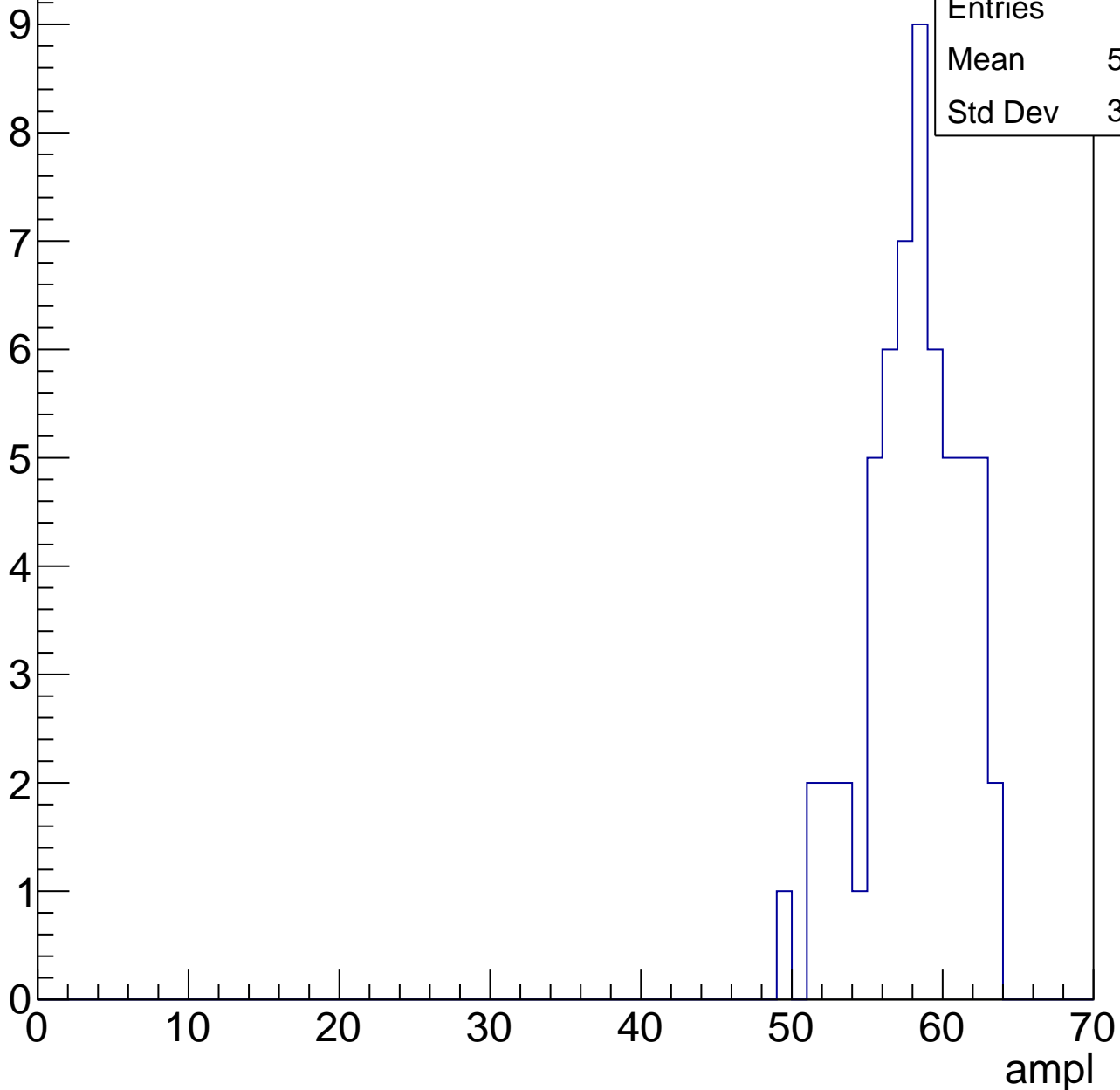


# B1L003S, U11-ch63, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	57.62
Std Dev	3.178

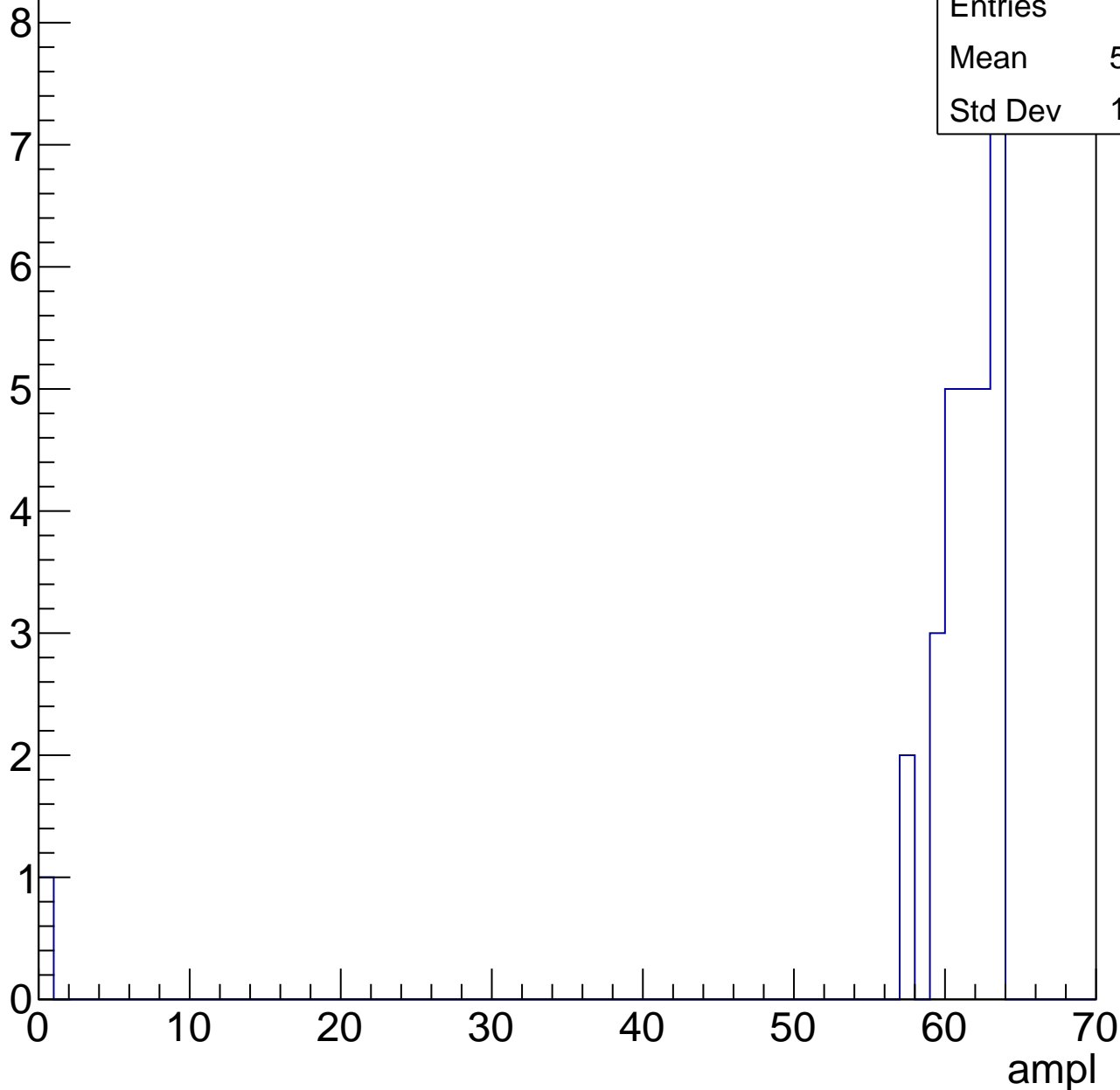


# B1L003S, U11-ch63, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	29
Mean	58.97
Std Dev	11.28



# B1L003S, U11-ch63, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L003S, U11-ch63, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L003S, U11-ch64, adc0

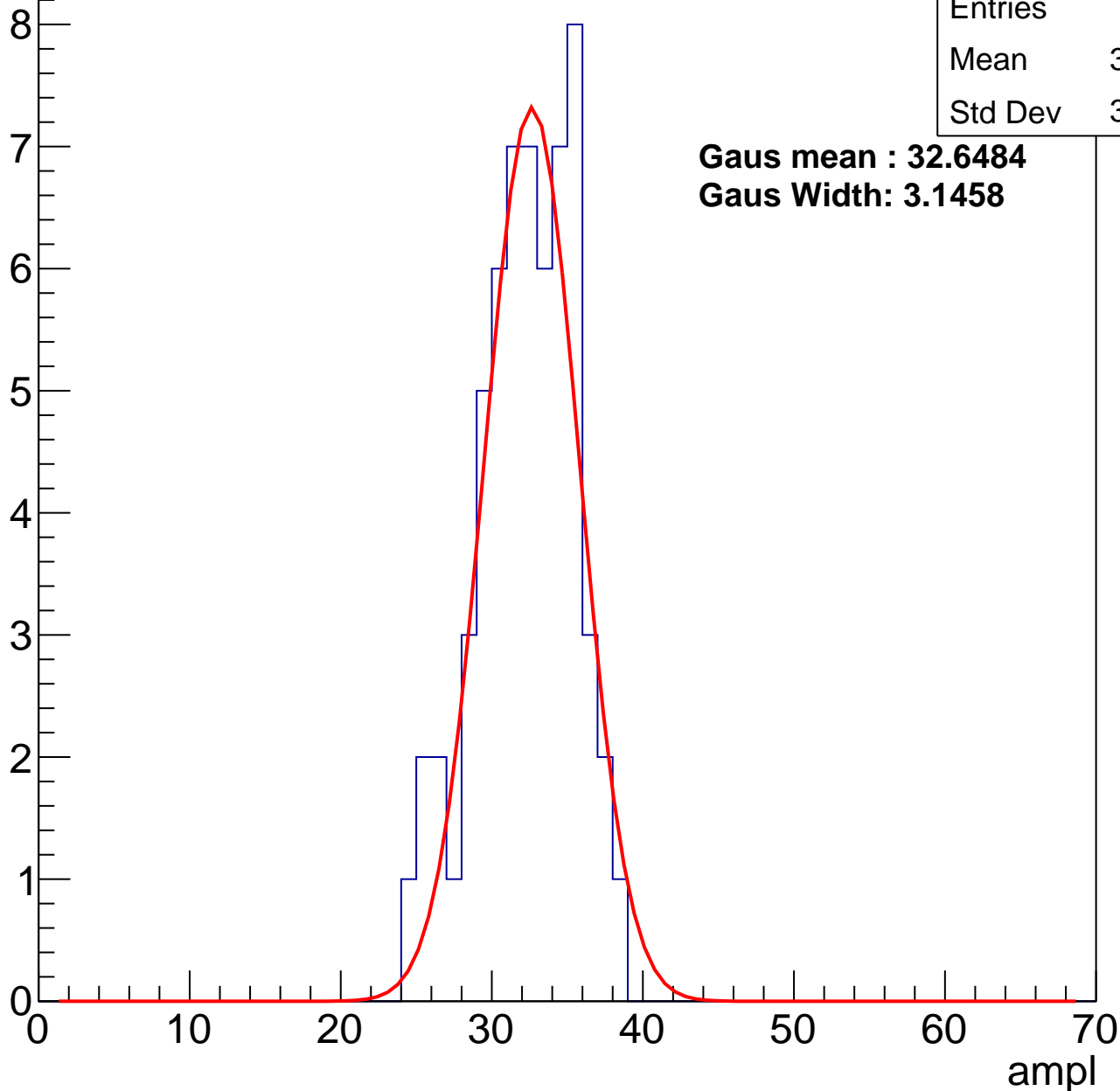
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	31.79
Std Dev	3.189

**Gaus mean : 32.6484**

**Gaus Width: 3.1458**



# B1L003S, U11-ch64, adc1

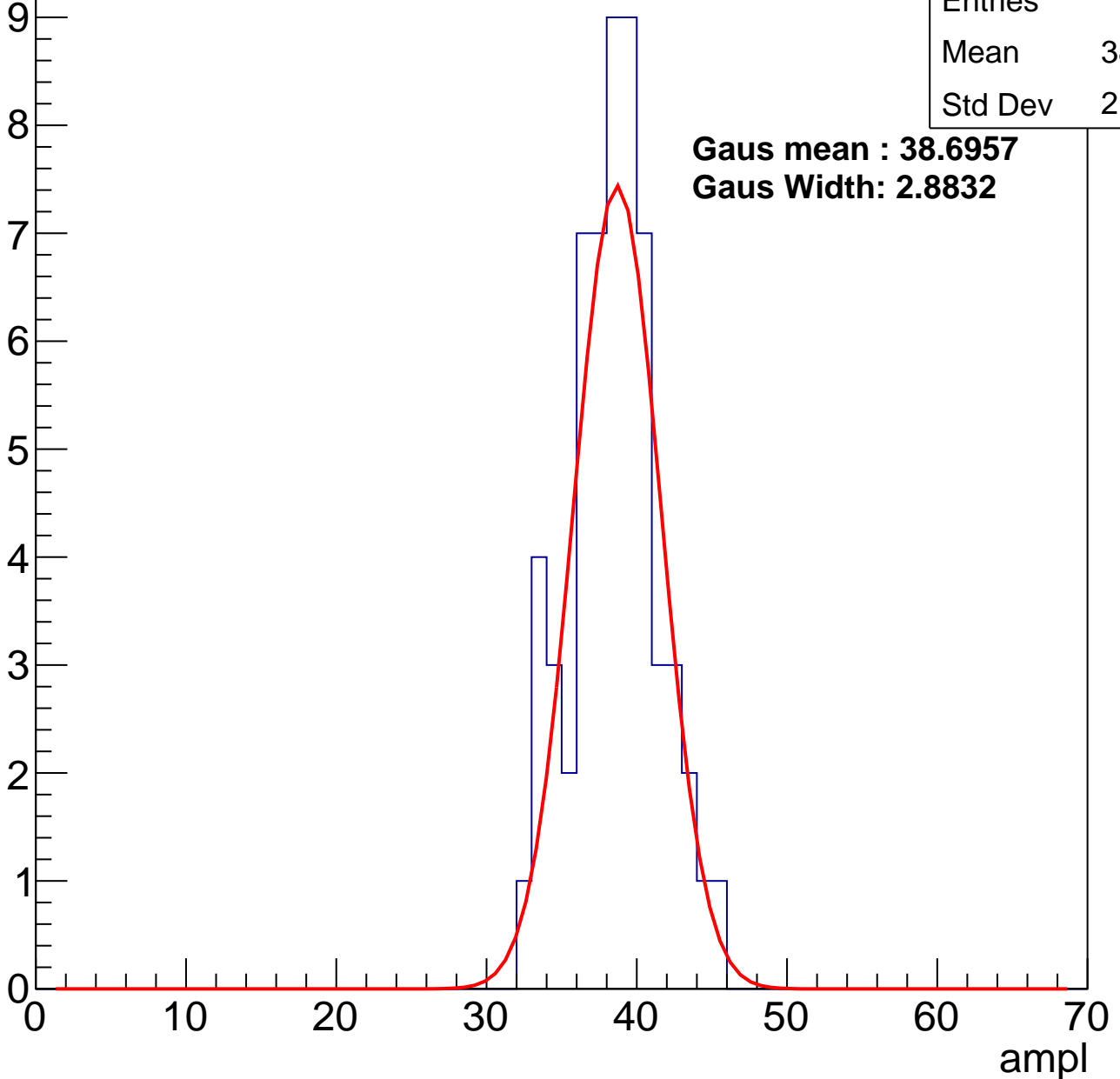
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	38.03
Std Dev	2.864

**Gaus mean : 38.6957**

**Gaus Width: 2.8832**



# B1L003S, U11-ch64, adc2

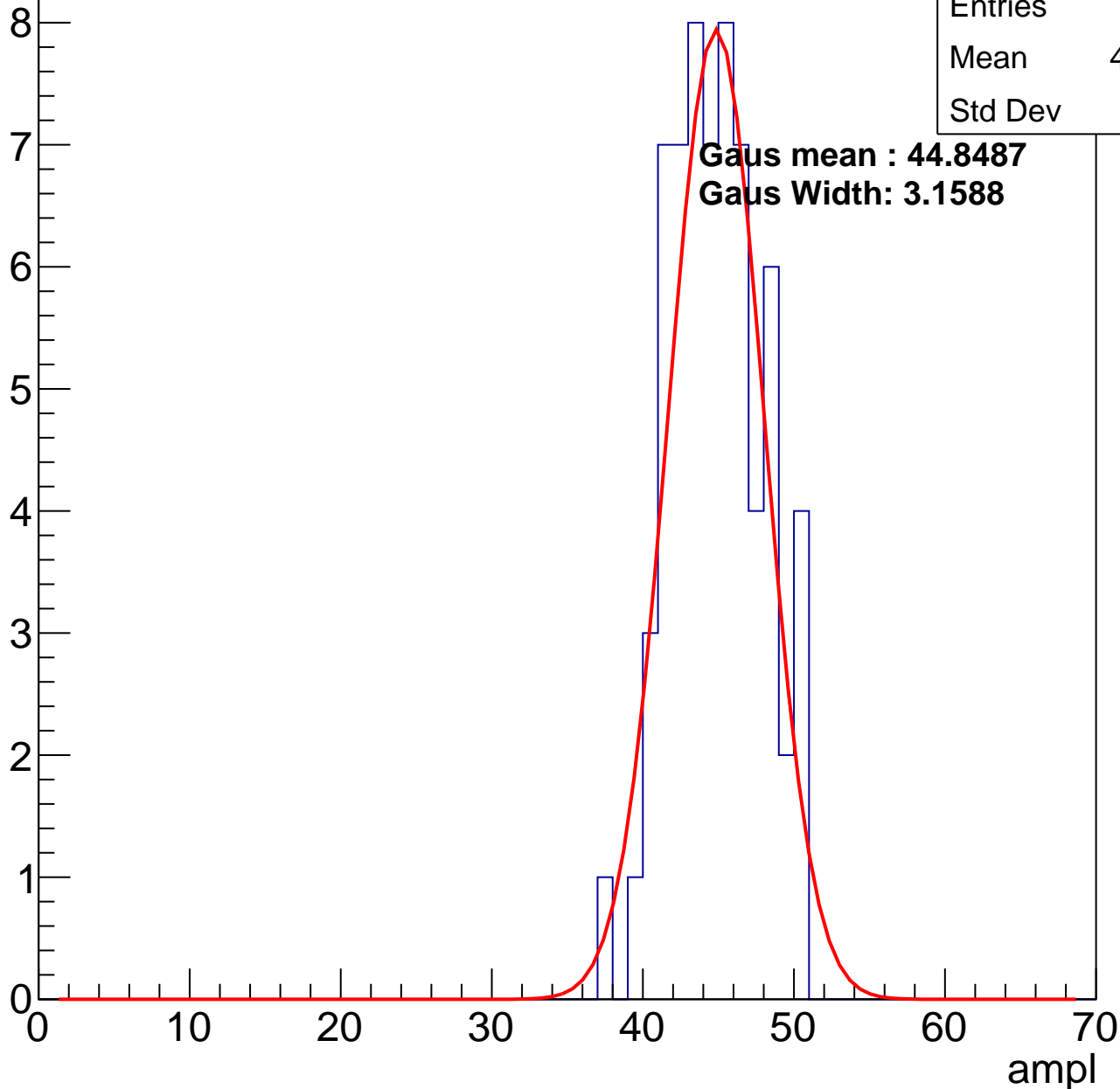
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	44.38
Std Dev	2.97

**Gaus mean : 44.8487**

**Gaus Width: 3.1588**

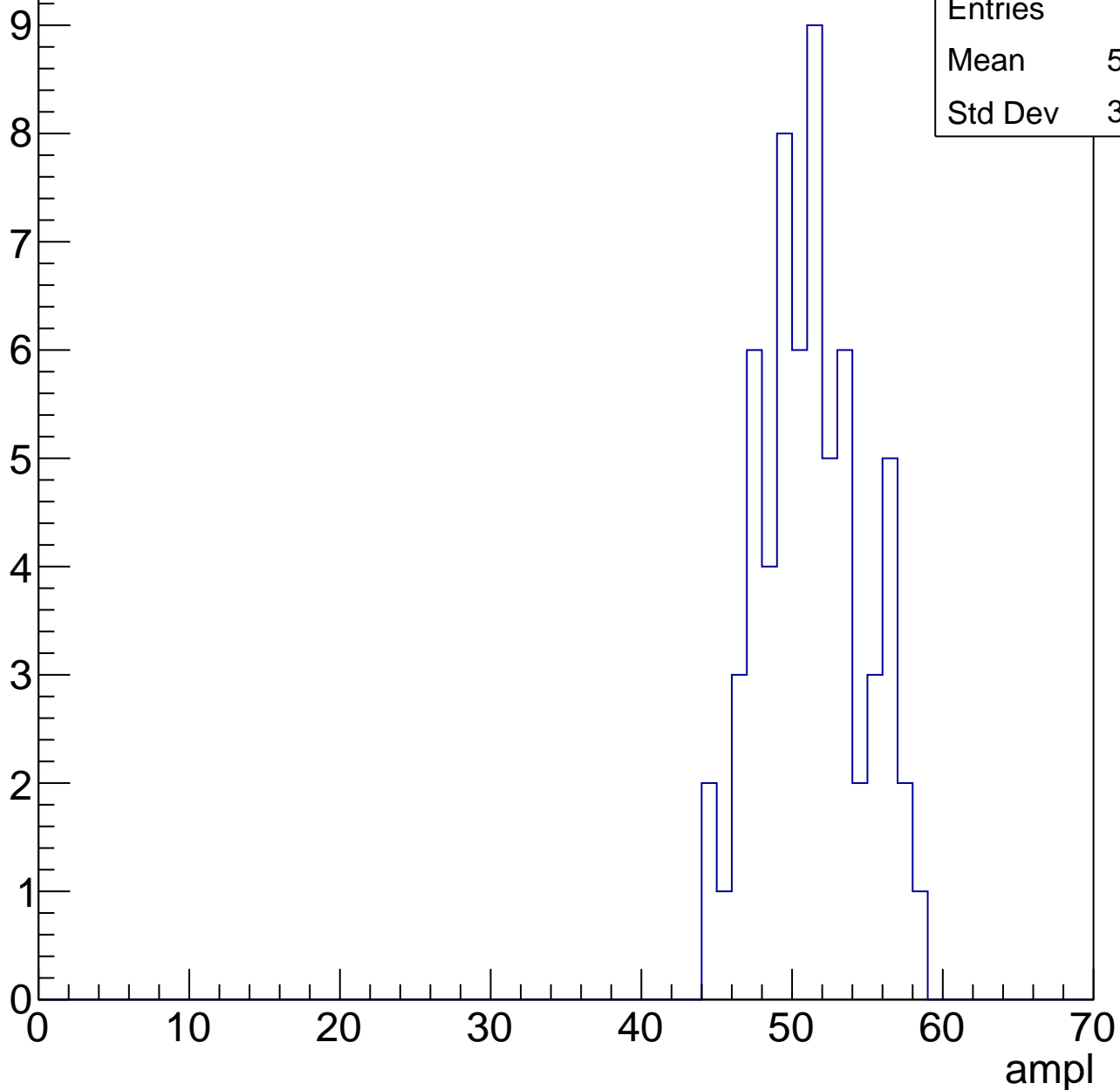


# B1L003S, U11-ch64, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

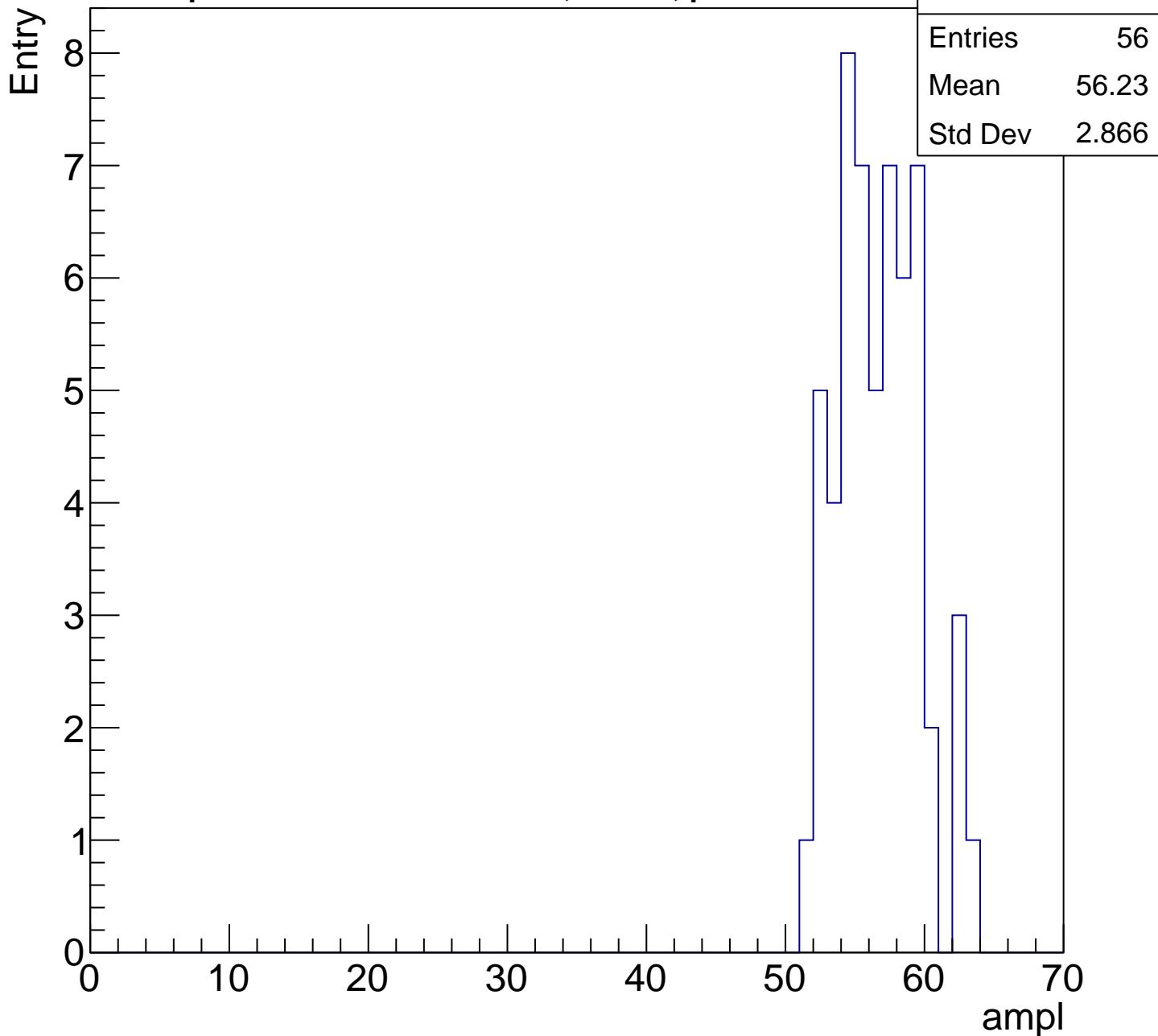
Entry

Entries	63
Mean	50.78
Std Dev	3.373



# B1L003S, U11-ch64, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

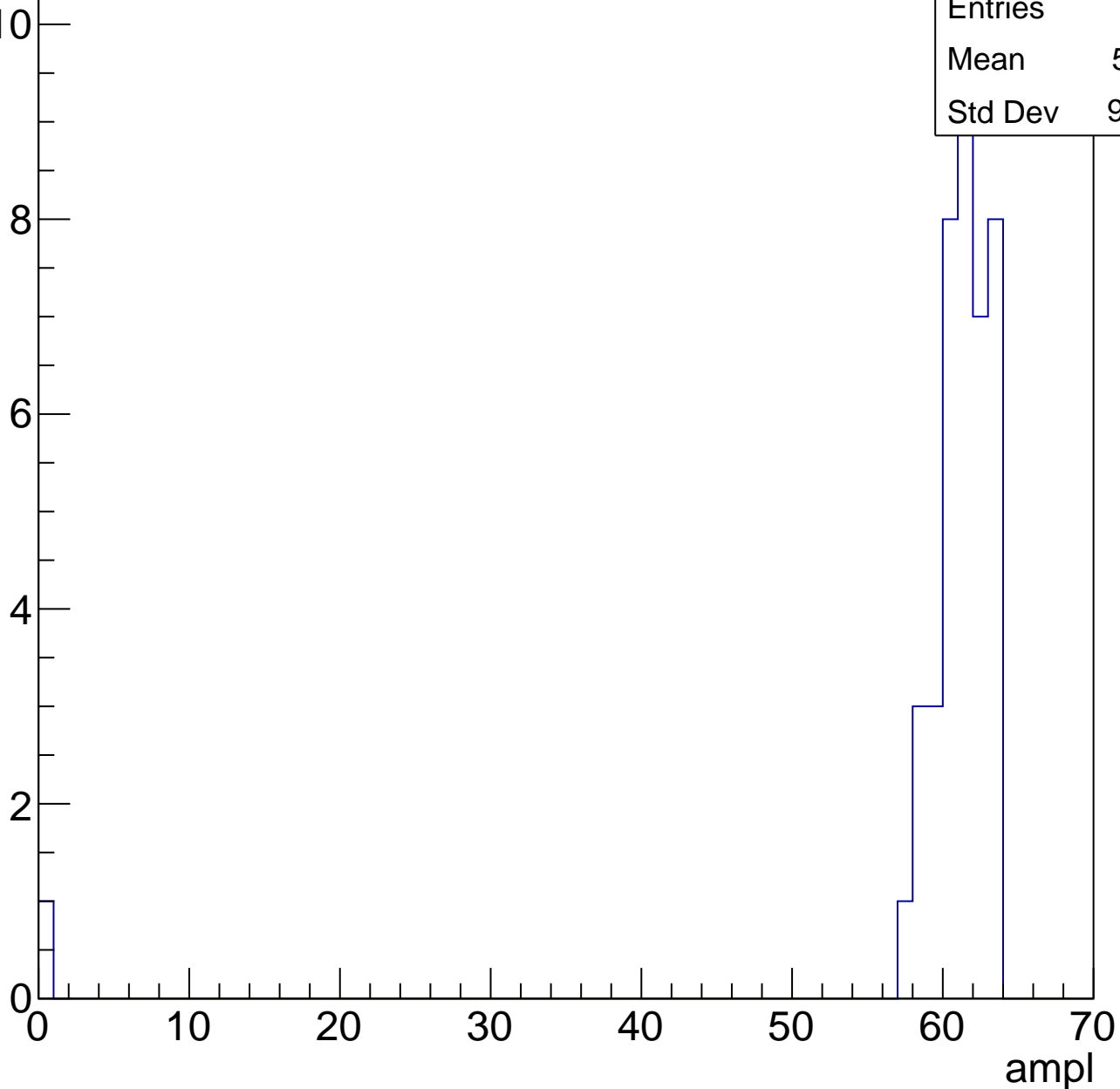


# B1L003S, U11-ch64, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	41
Mean	59.41
Std Dev	9.525



# B1L003S, U11-ch64, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

1

Mean

63

Std Dev

0



# B1L003S, U11-ch64, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U11-ch65, adc0

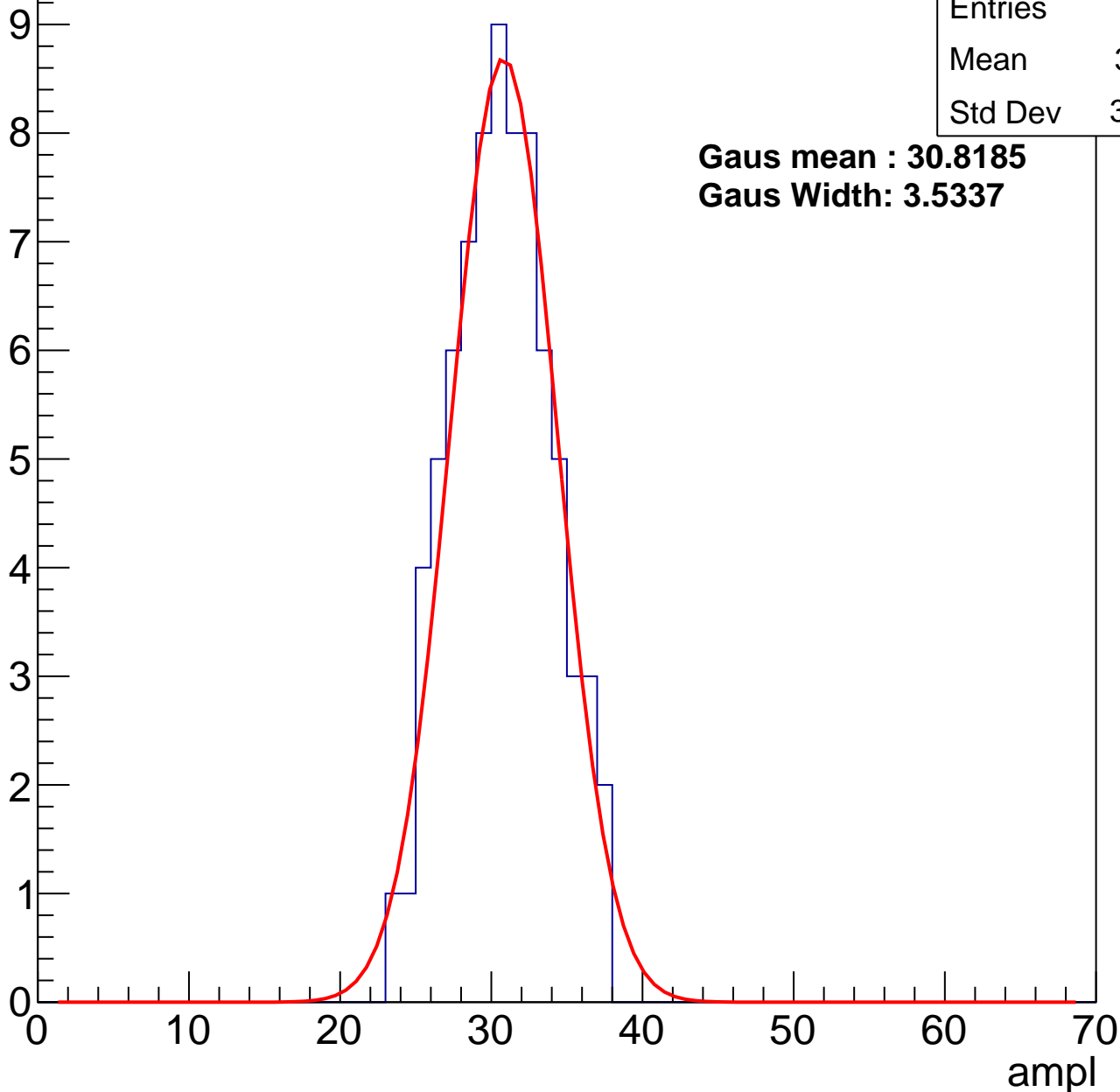
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	76
Mean	30.21
Std Dev	3.258

**Gaus mean : 30.8185**

**Gaus Width: 3.5337**



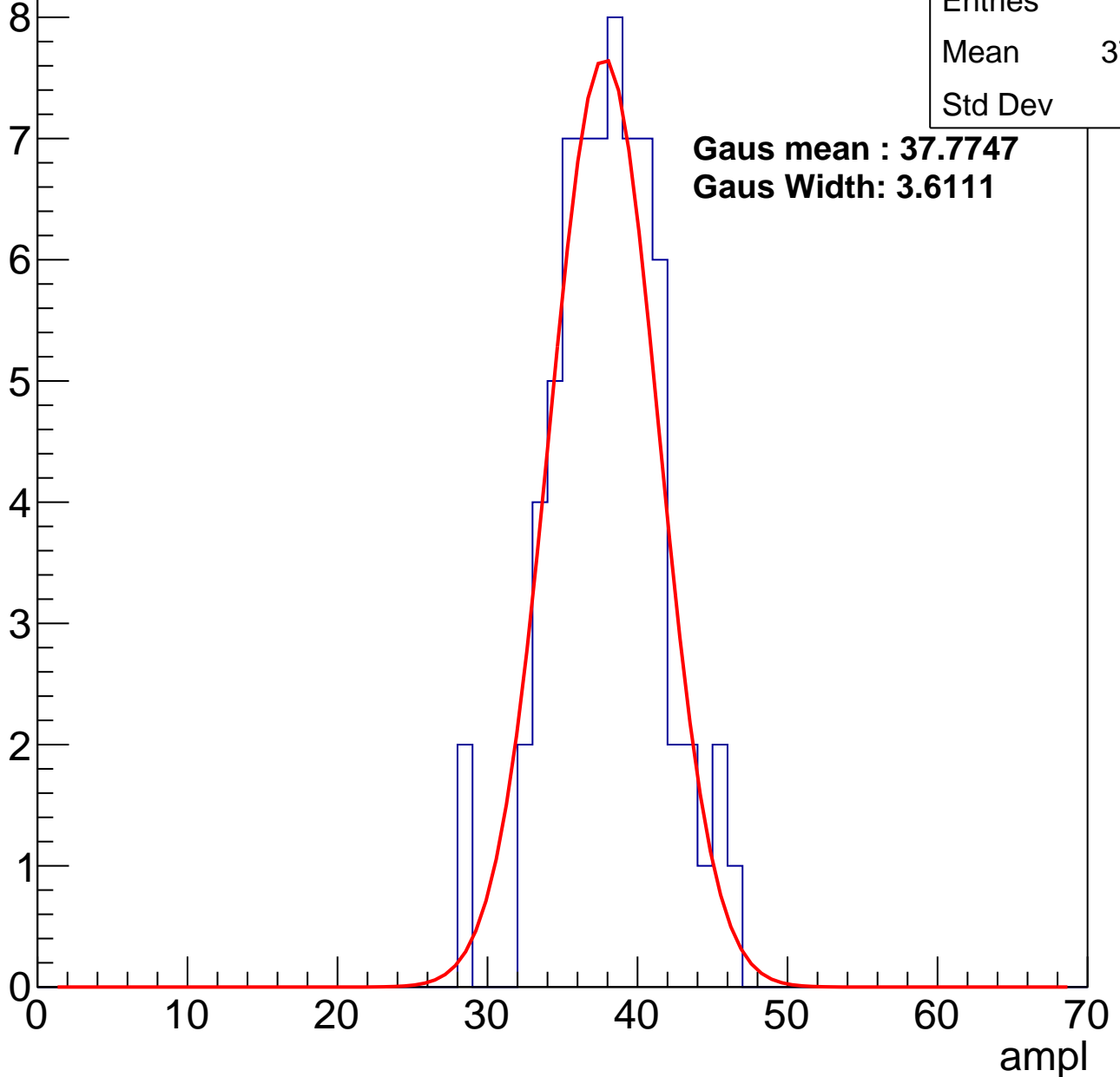
# B1L003S, U11-ch65, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	37.59
Std Dev	3.6

**Gaus mean : 37.7747**  
**Gaus Width: 3.6111**



# B1L003S, U11-ch65, adc2

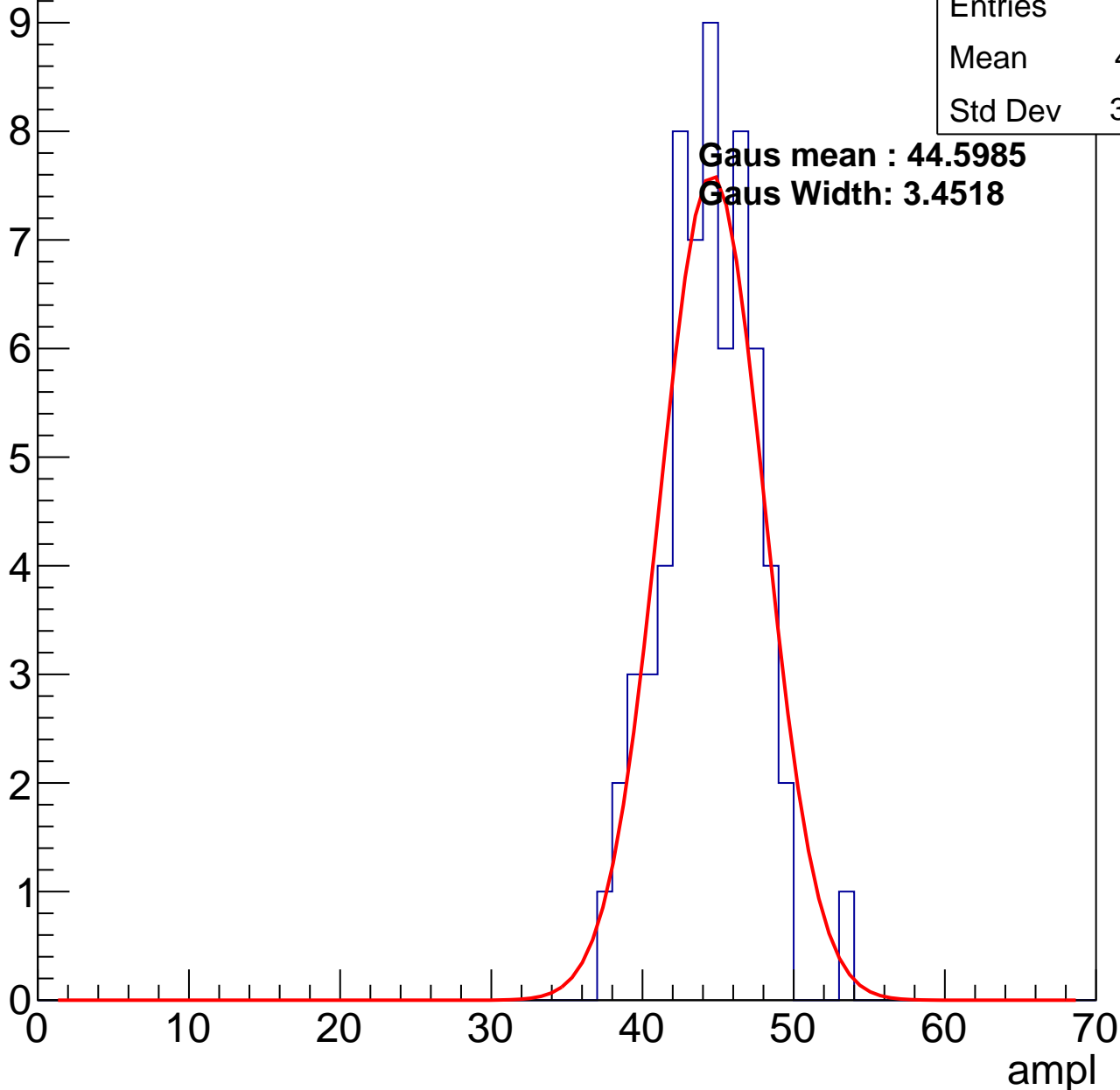
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	43.91
Std Dev	3.076

**Gaus mean : 44.5985**

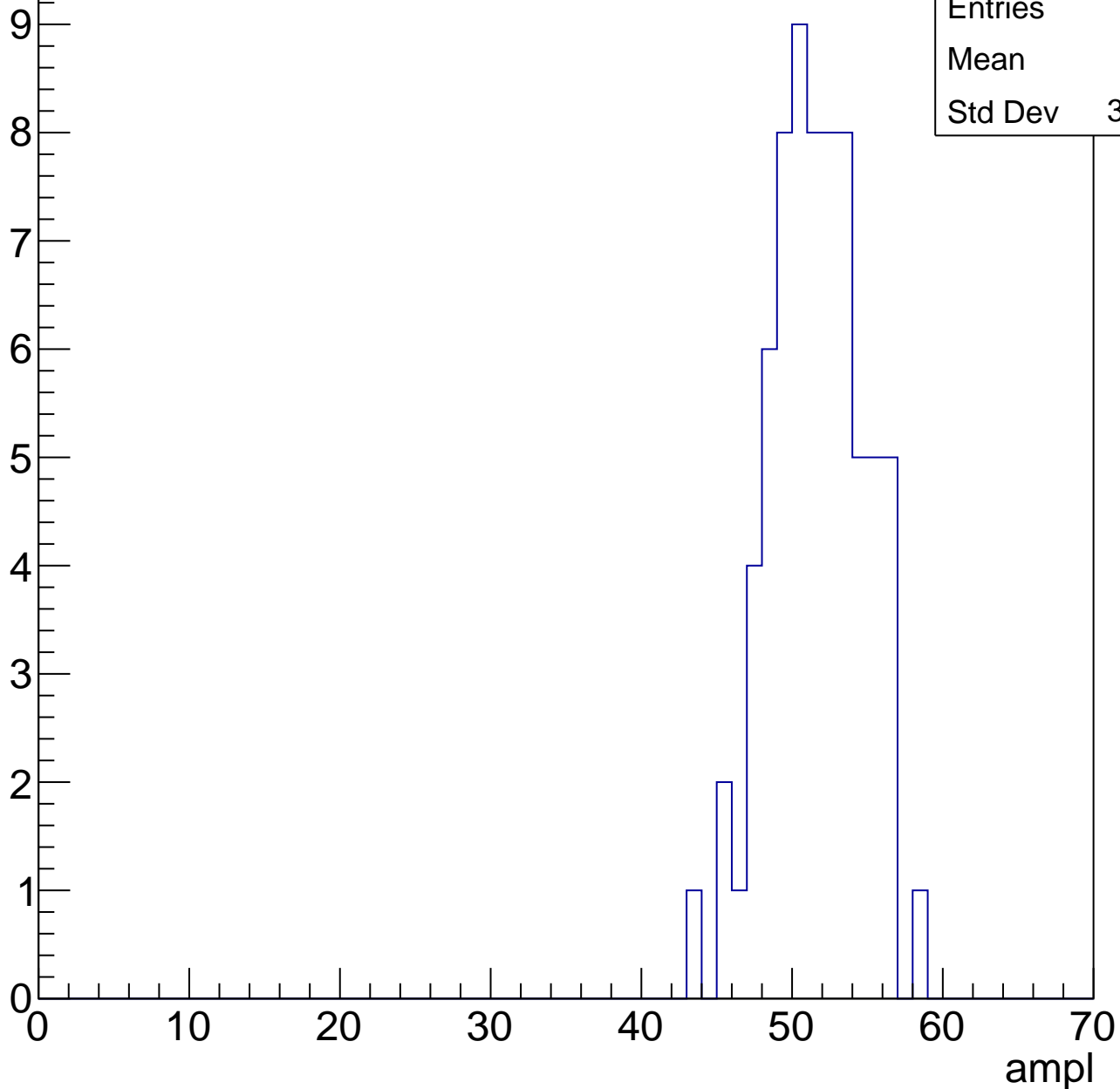
**Gaus Width: 3.4518**



# B1L003S, U11-ch65, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U11-ch65, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

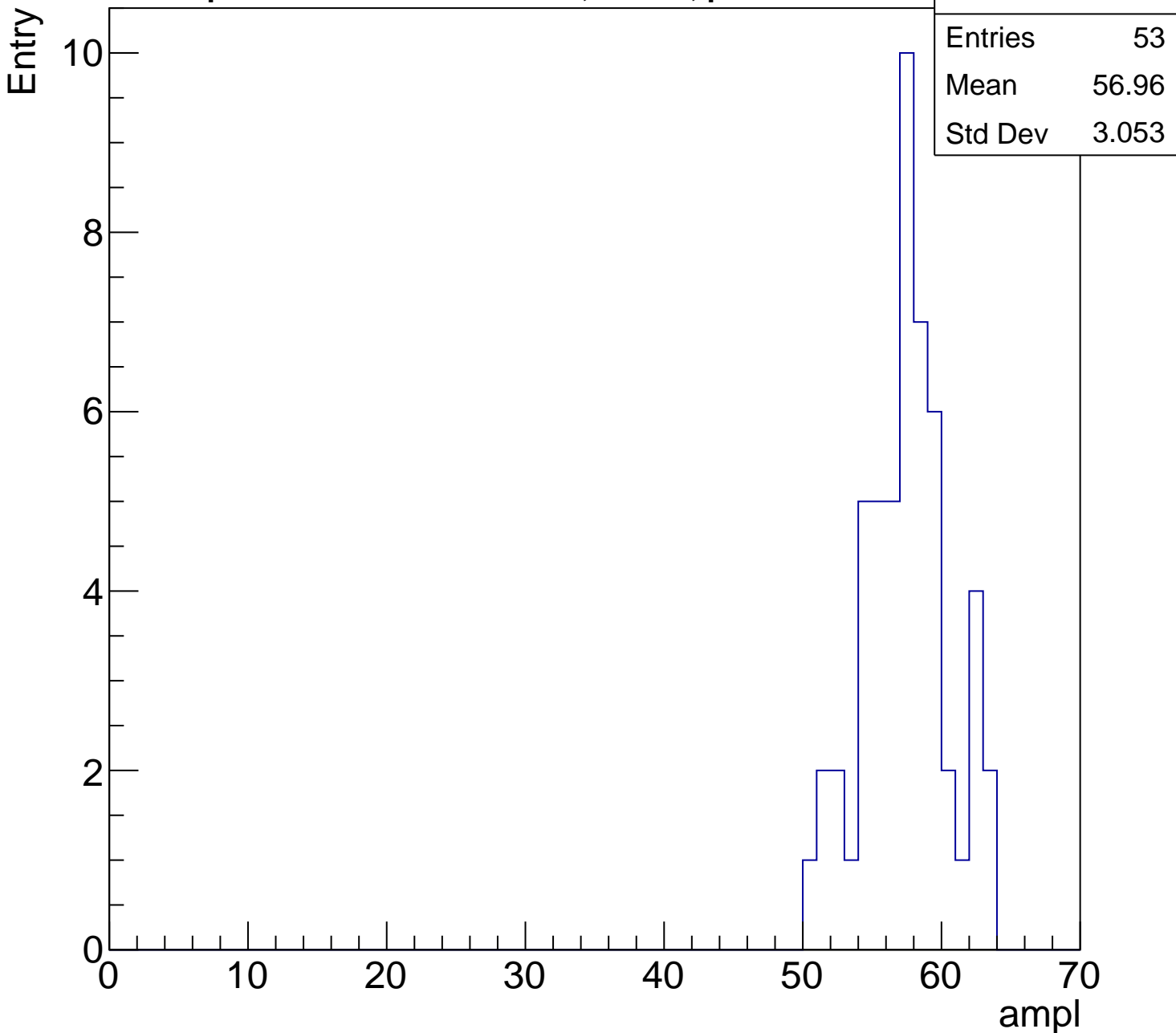
Entries	53
Mean	56.96
Std Dev	3.053

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

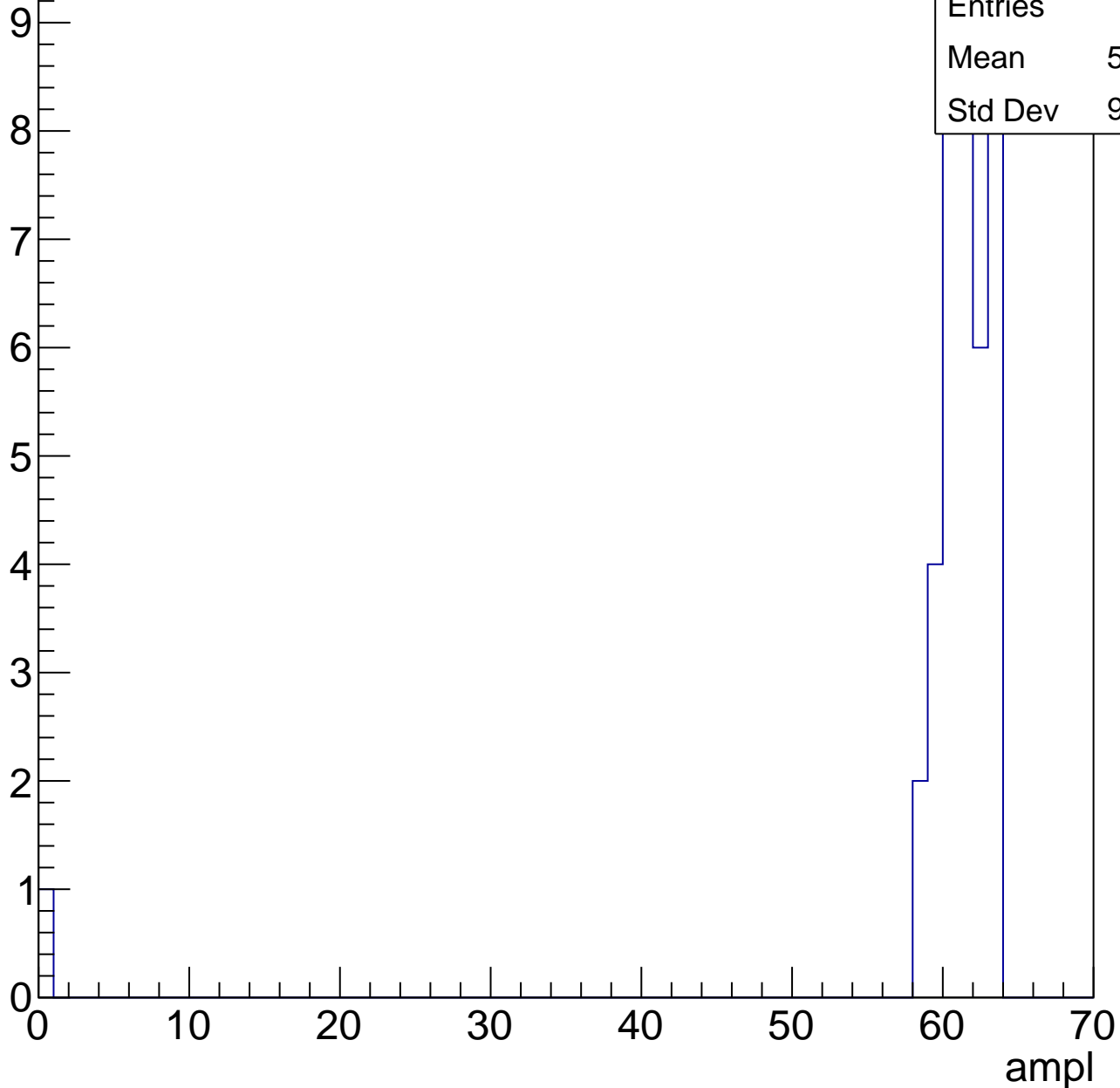
ampl



# B1L003S, U11-ch65, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U11-ch65, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L003S, U11-ch65, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U11-ch66, adc0

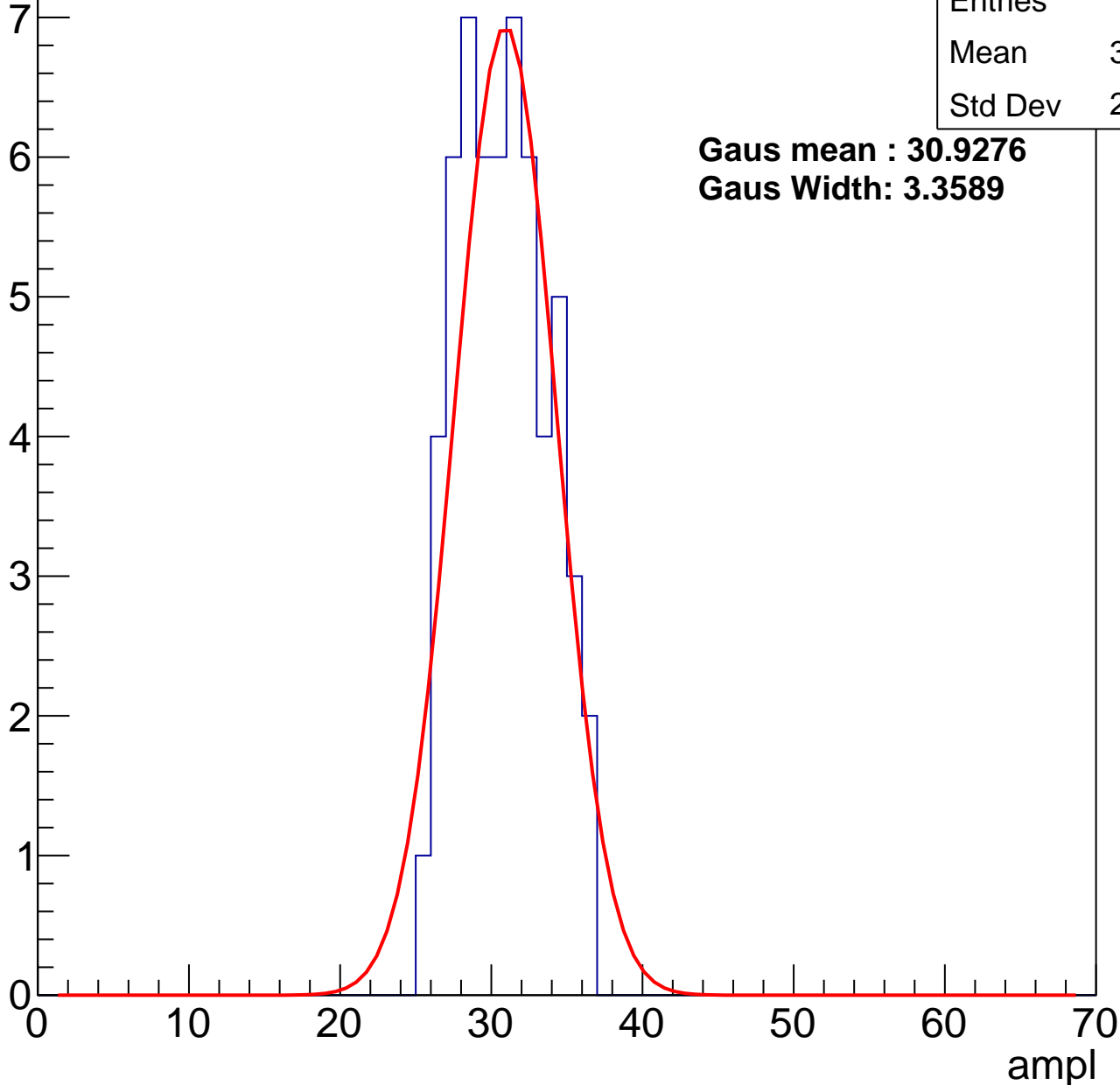
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	30.33
Std Dev	2.855

**Gaus mean : 30.9276**

**Gaus Width: 3.3589**



# B1L003S, U11-ch66, adc1

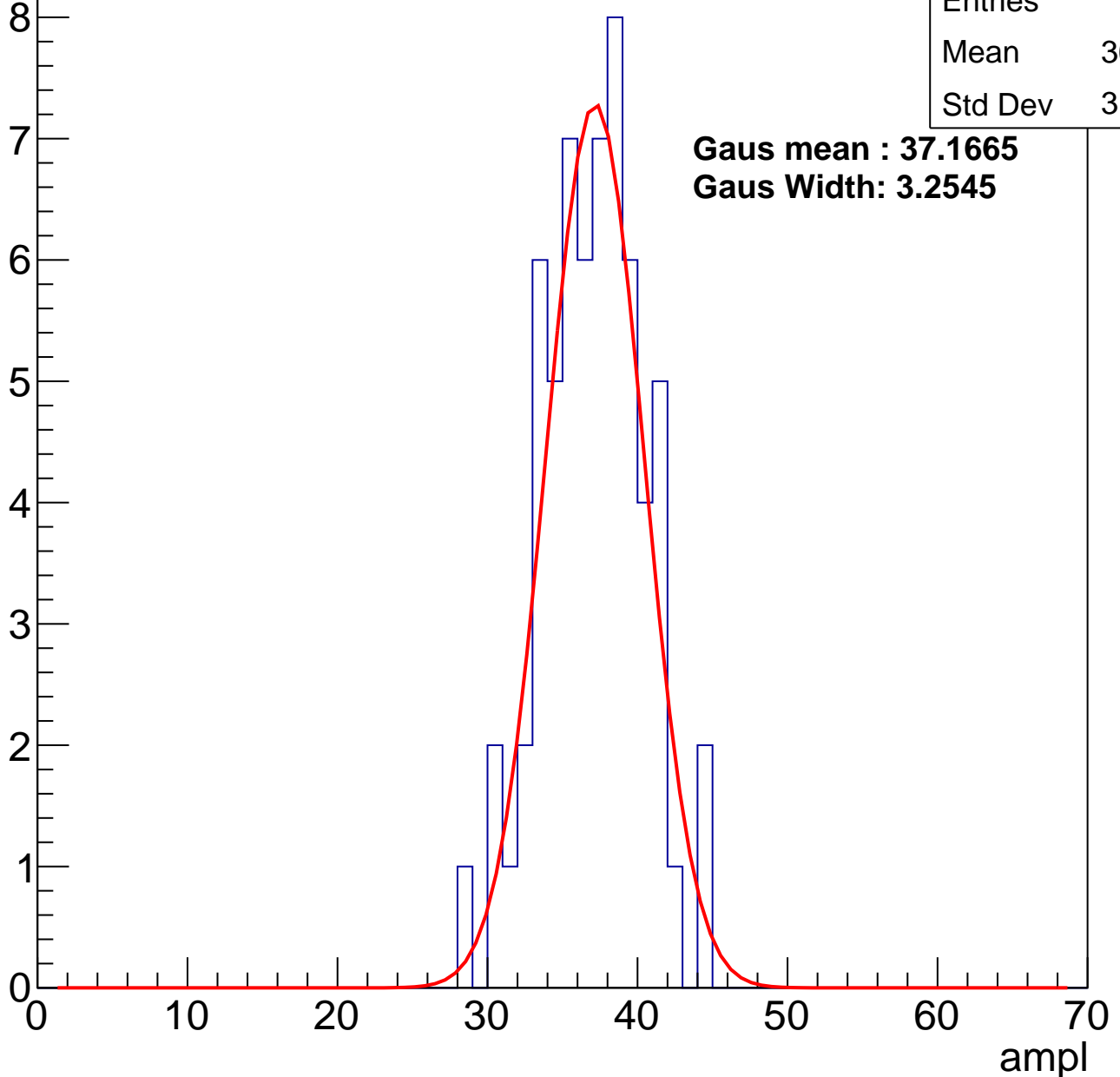
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	36.57
Std Dev	3.332

**Gaus mean : 37.1665**

**Gaus Width: 3.2545**



# B1L003S, U11-ch66, adc2

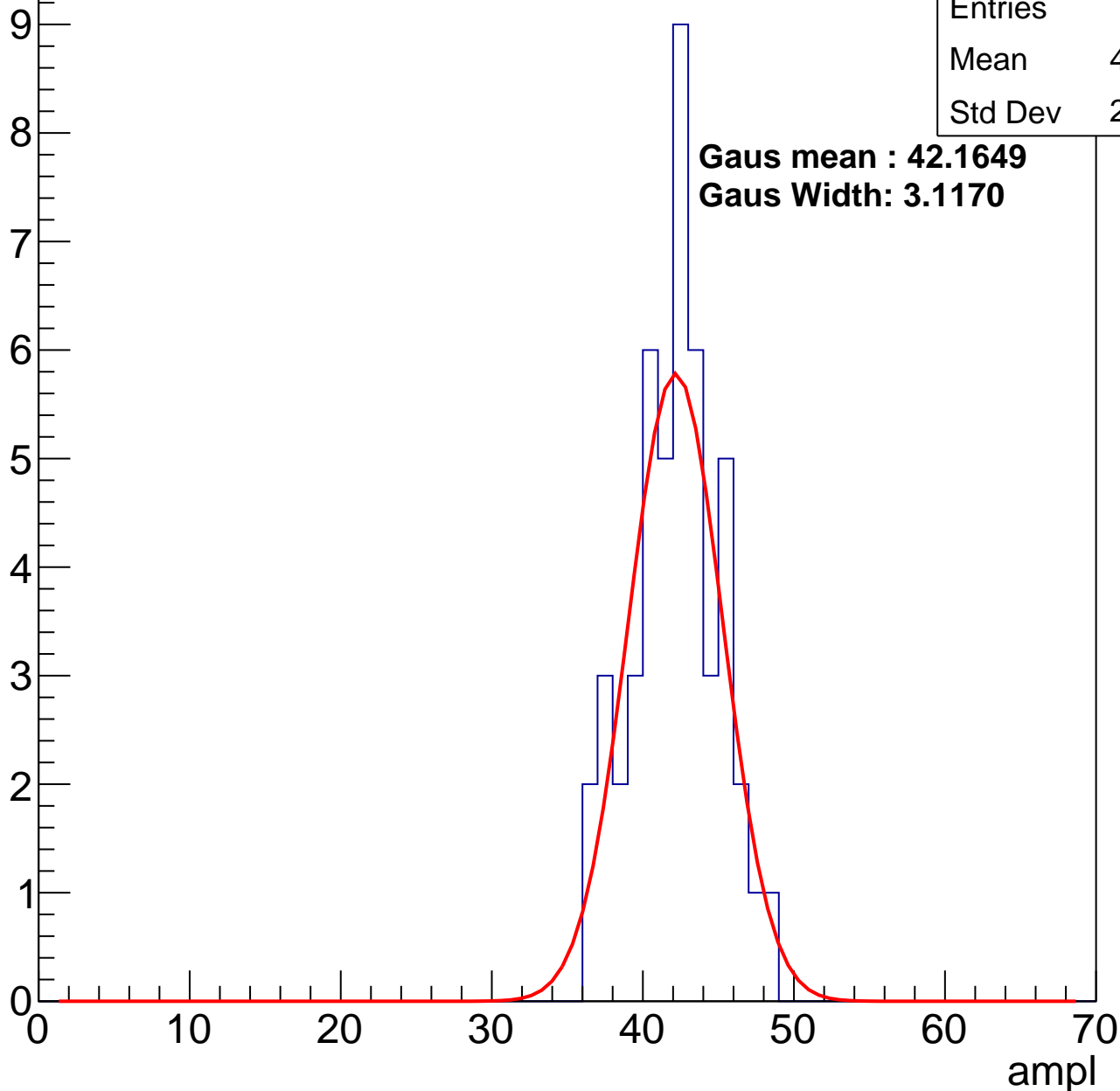
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	48
Mean	41.69
Std Dev	2.837

**Gaus mean : 42.1649**

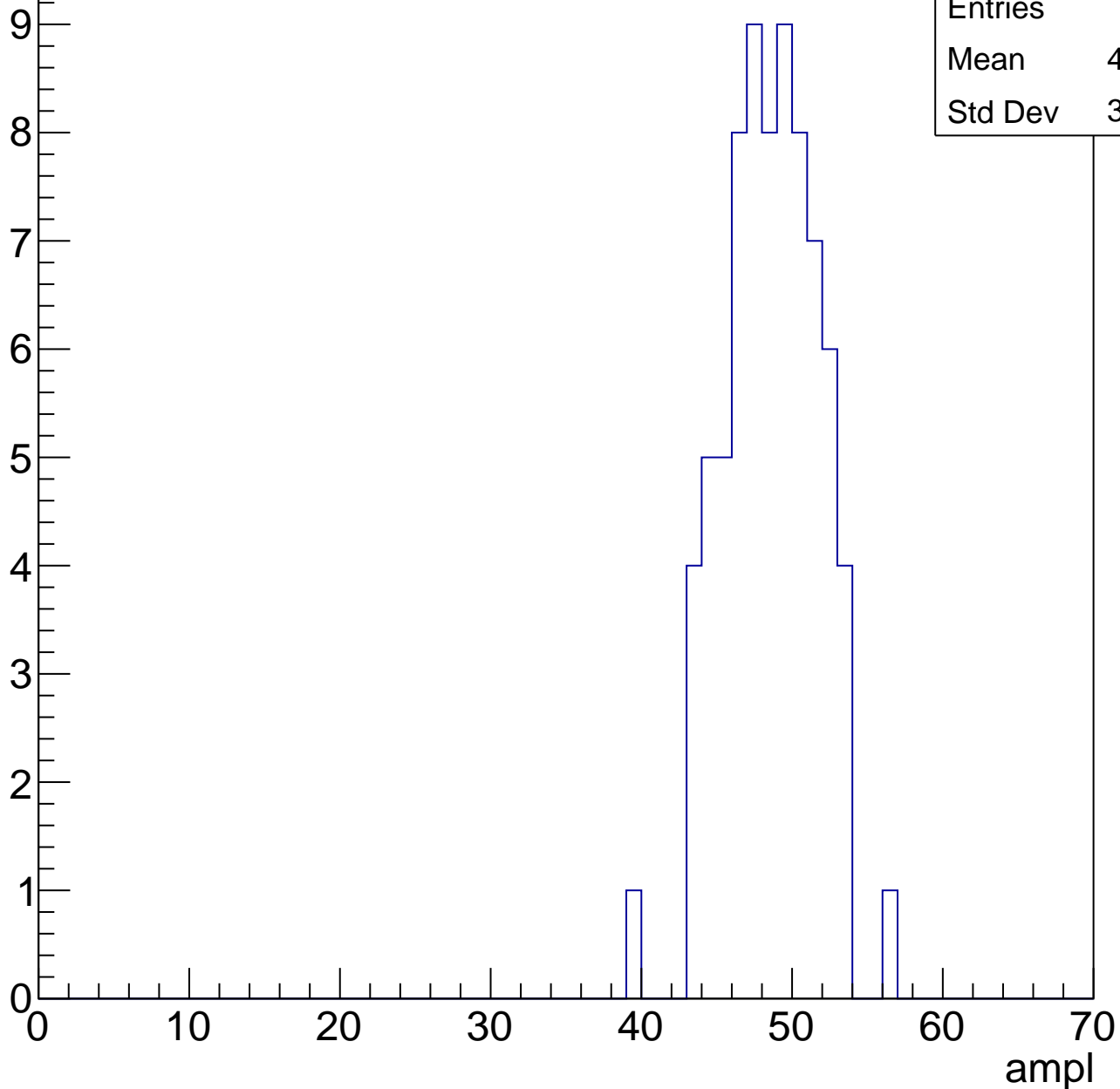
**Gaus Width: 3.1170**



# B1L003S, U11-ch66, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

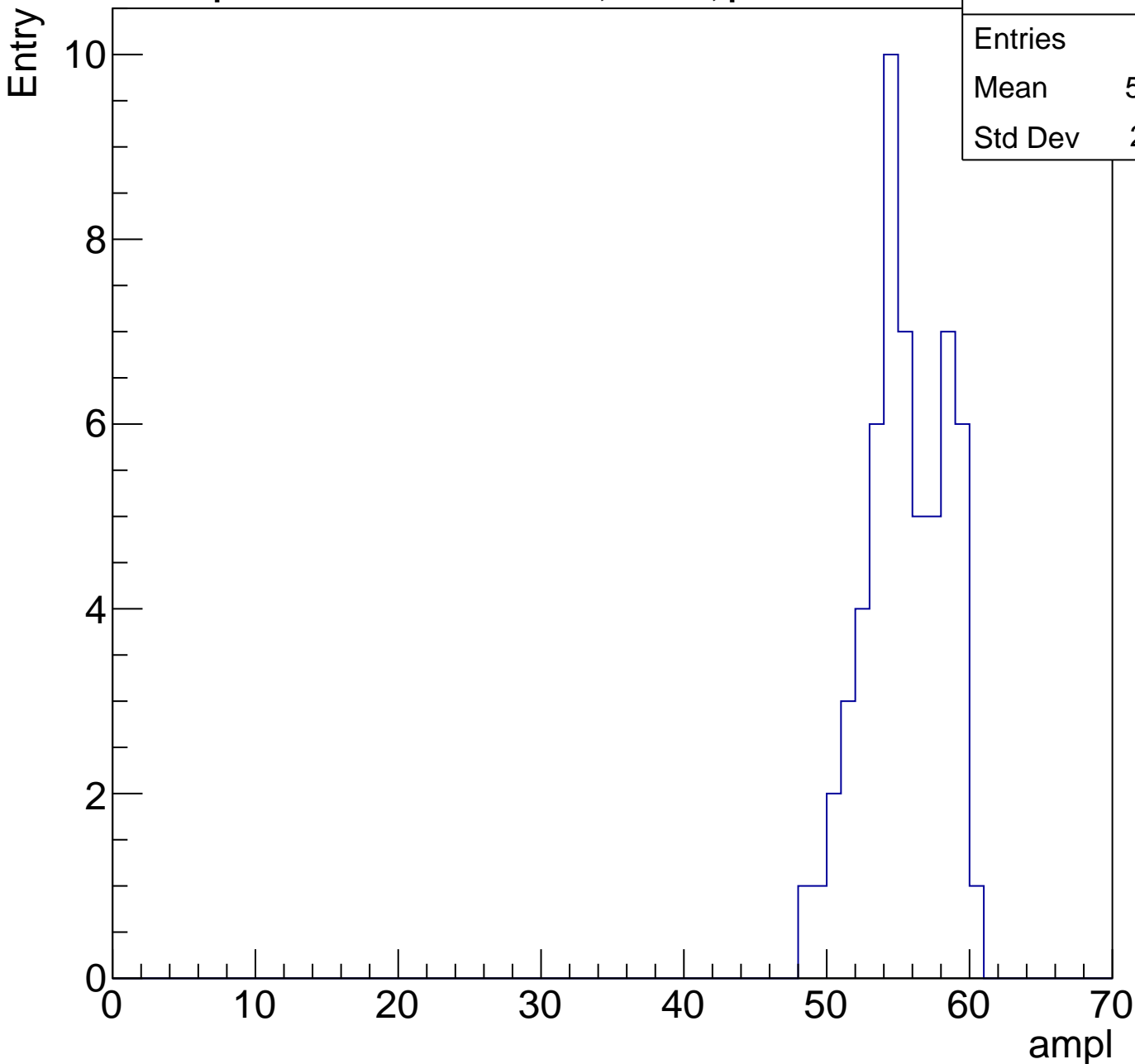
Entry



# B1L003S, U11-ch66, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	58
Mean	54.93
Std Dev	2.821

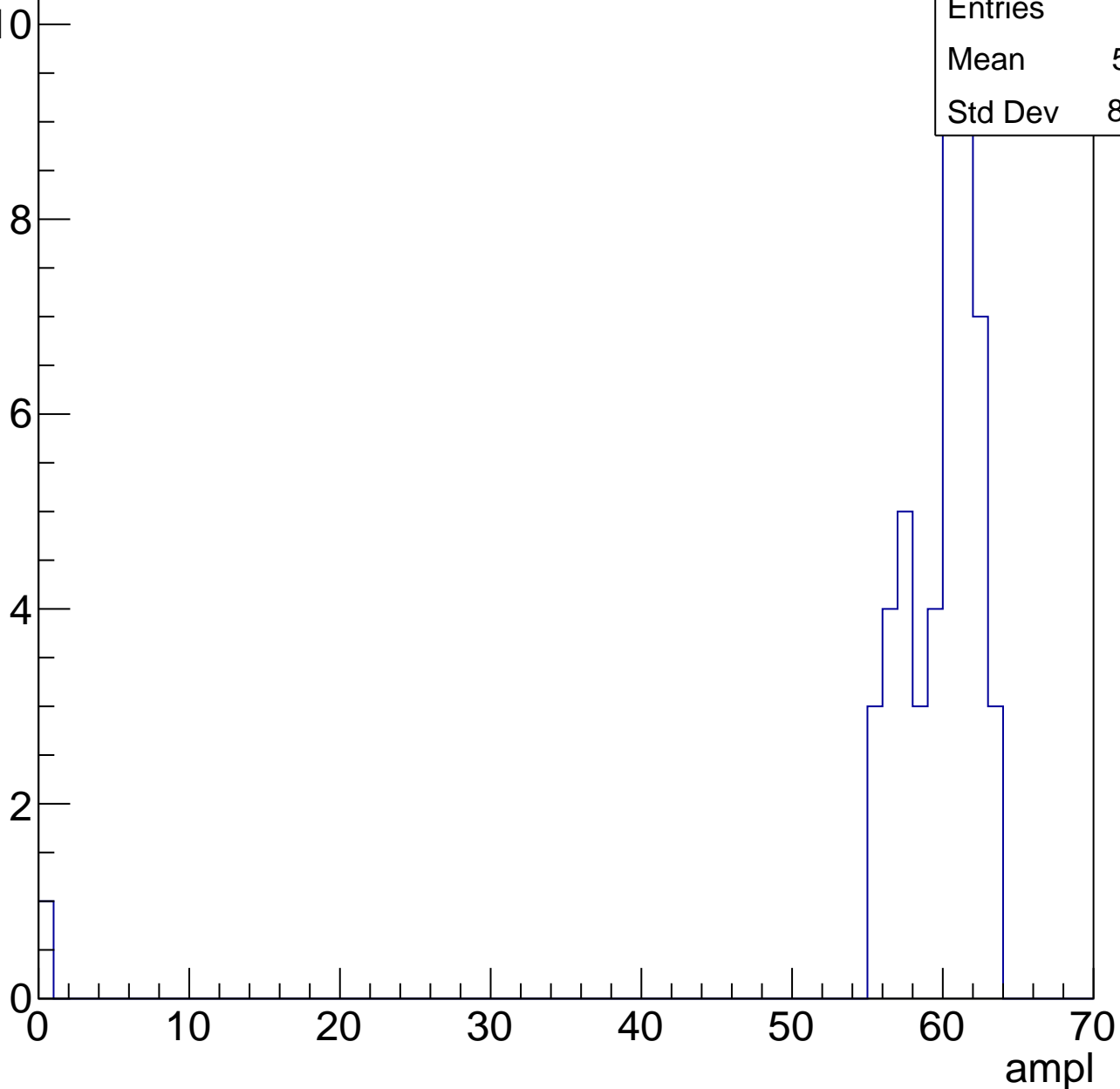


# B1L003S, U11-ch66, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	49
Mean	58.31
Std Dev	8.718

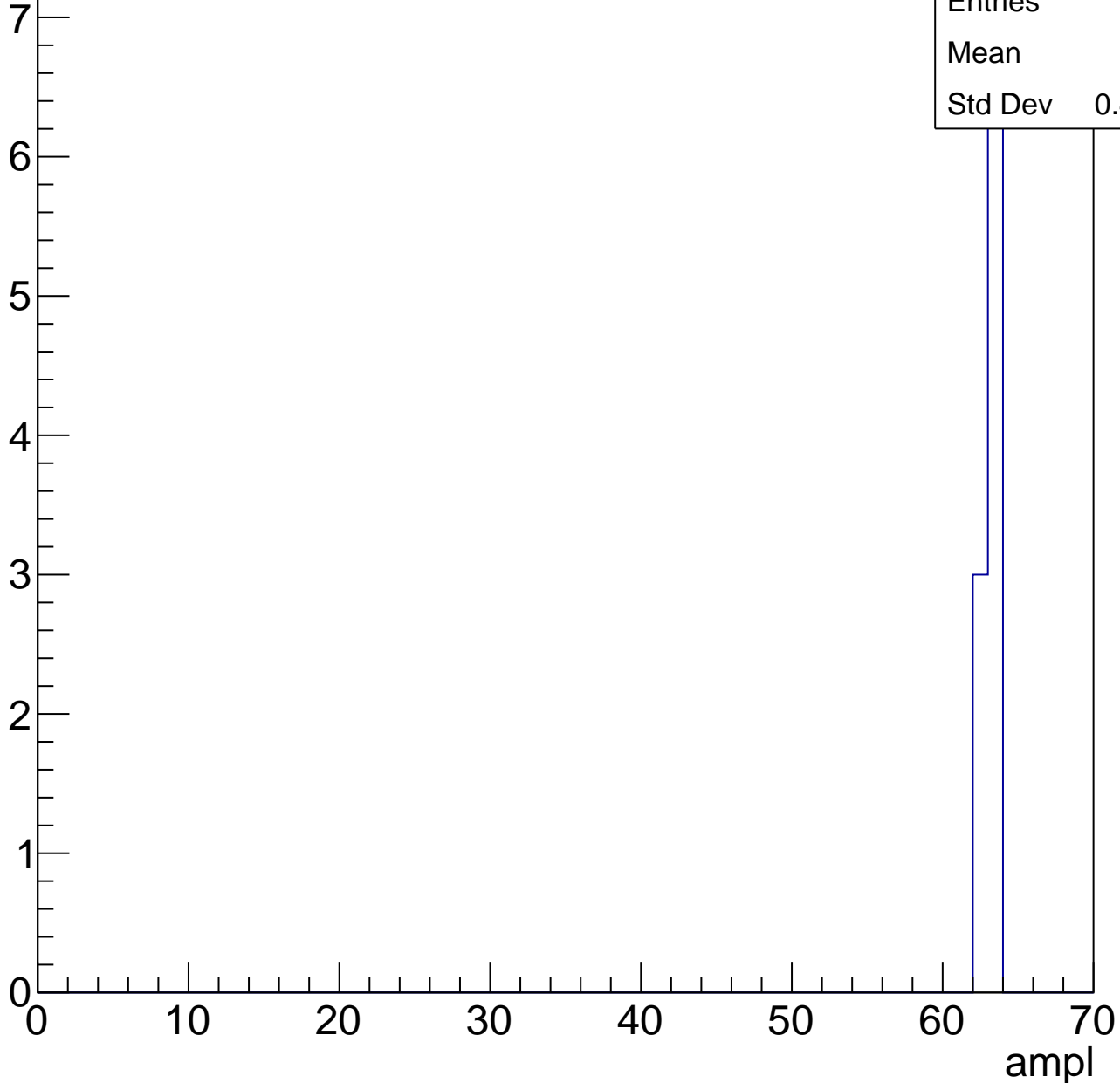


# B1L003S, U11-ch66, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	10
Mean	62.7
Std Dev	0.4583





# B1L003S, U11-ch66, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

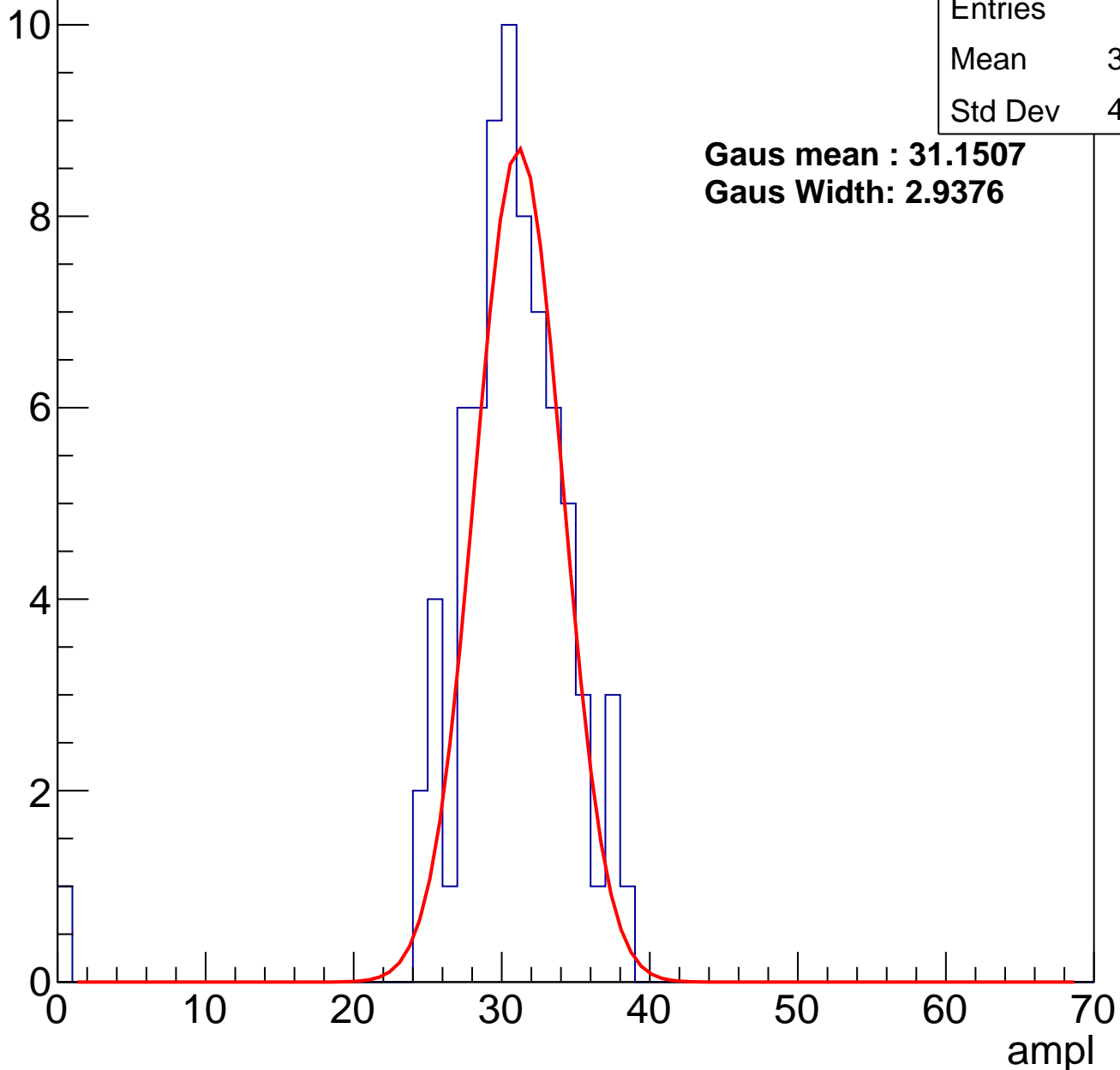
# B1L003S, U11-ch67, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	73
Mean	30.07
Std Dev	4.778

**Gaus mean : 31.1507**  
**Gaus Width: 2.9376**

Entry



# B1L003S, U11-ch67, adc1

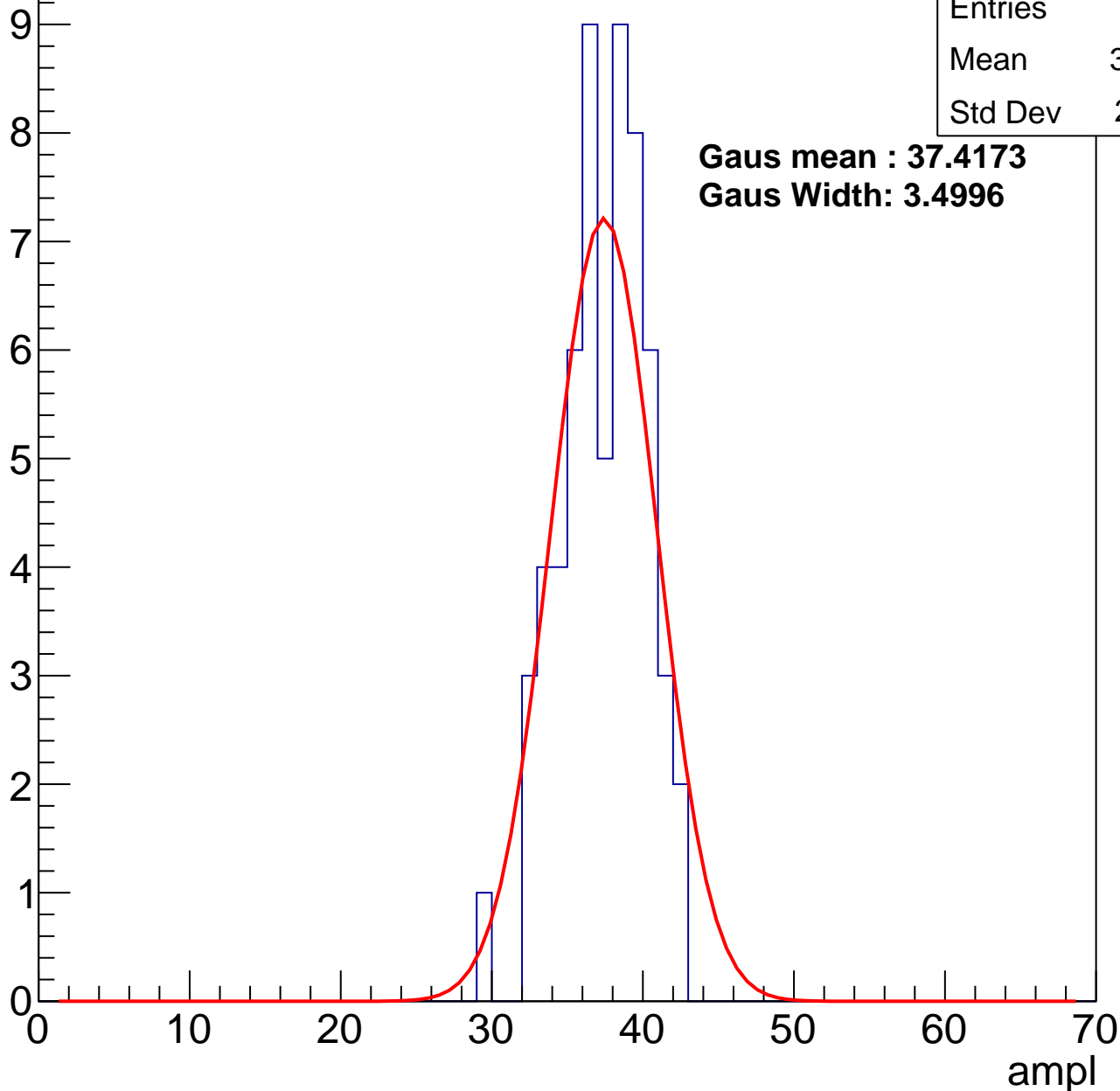
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	36.88
Std Dev	2.781

**Gaus mean : 37.4173**

**Gaus Width: 3.4996**



# B1L003S, U11-ch67, adc2

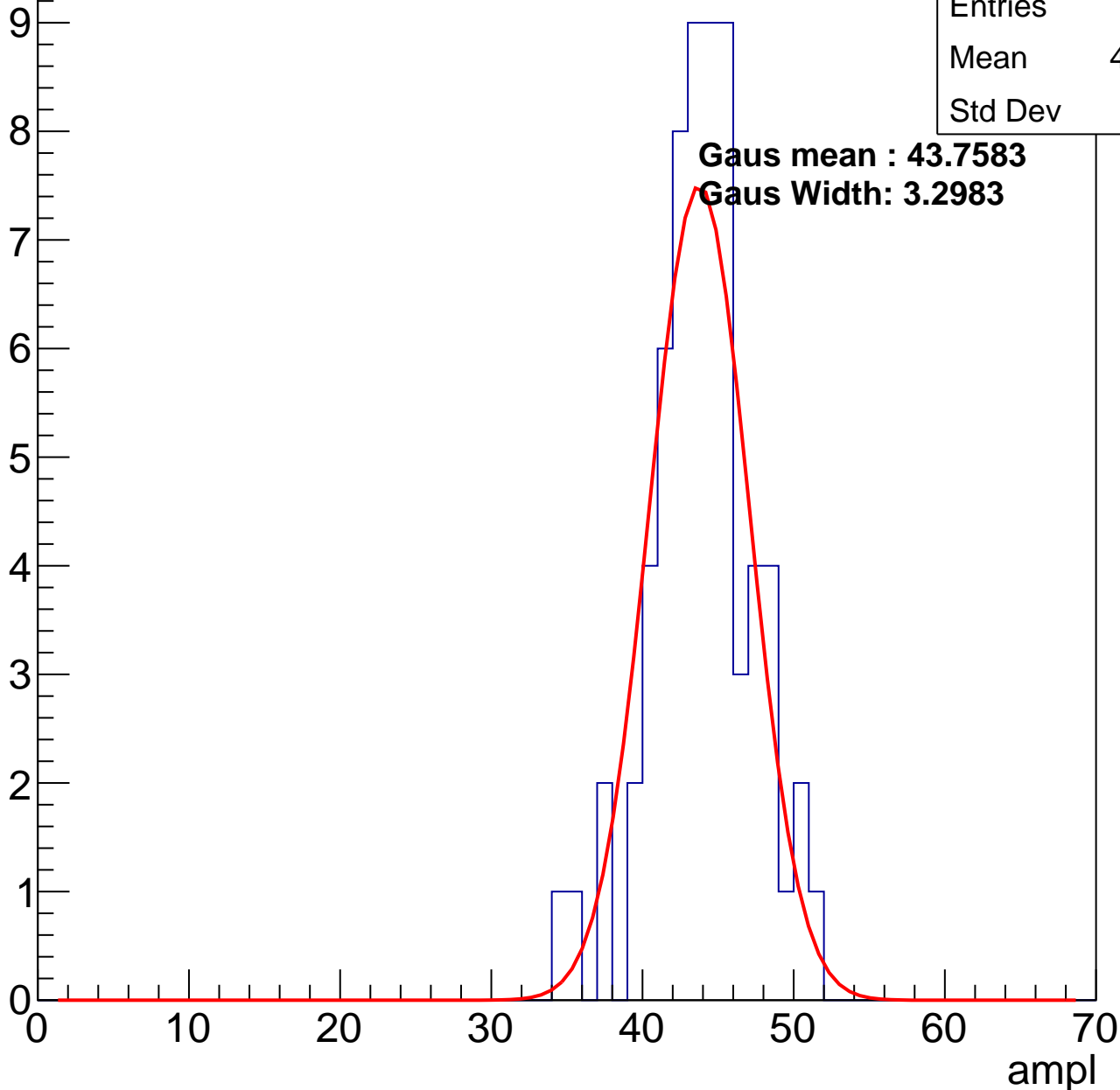
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	43.47
Std Dev	3.34

**Gaus mean : 43.7583**

**Gaus Width: 3.2983**

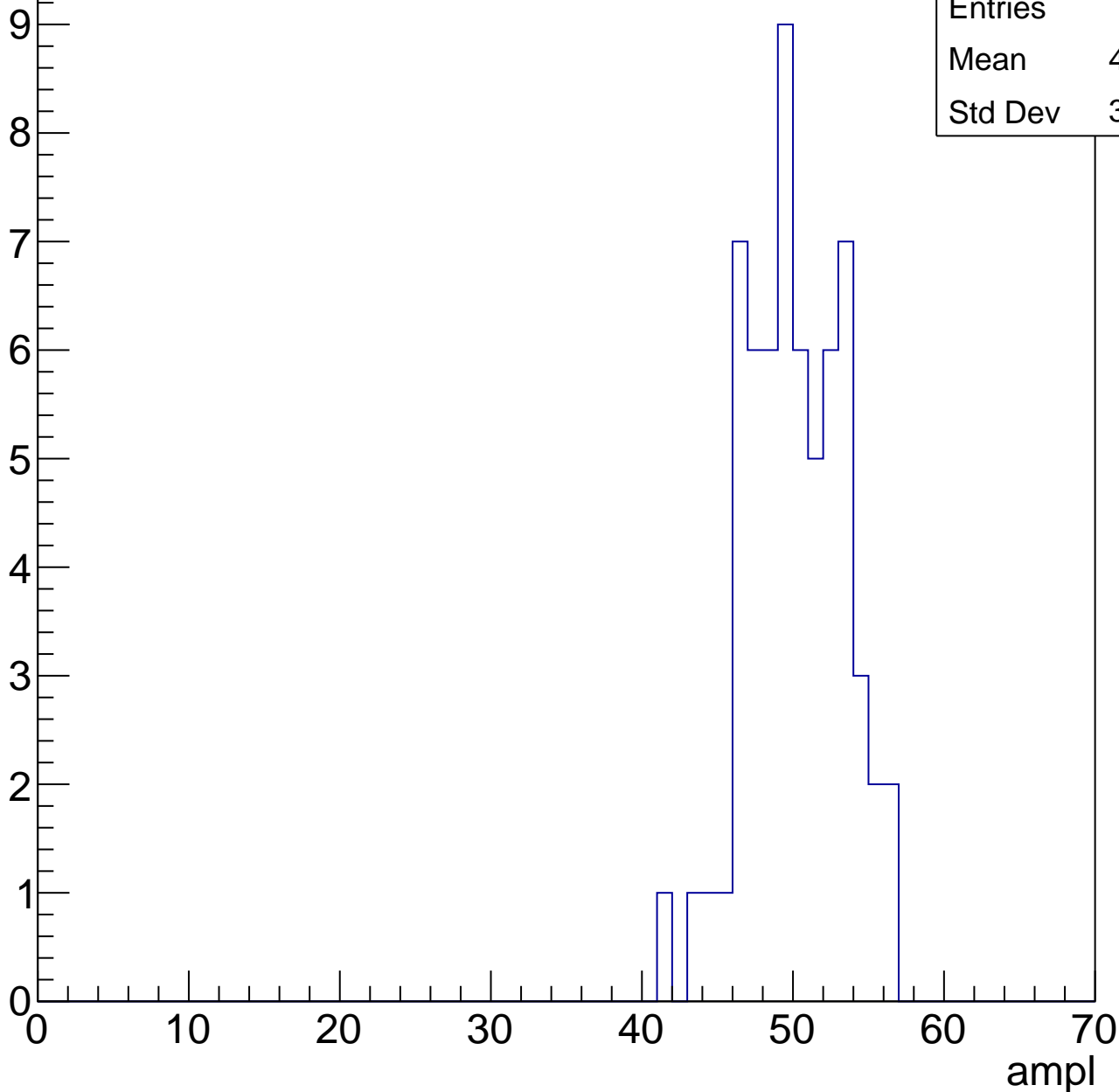


# B1L003S, U11-ch67, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

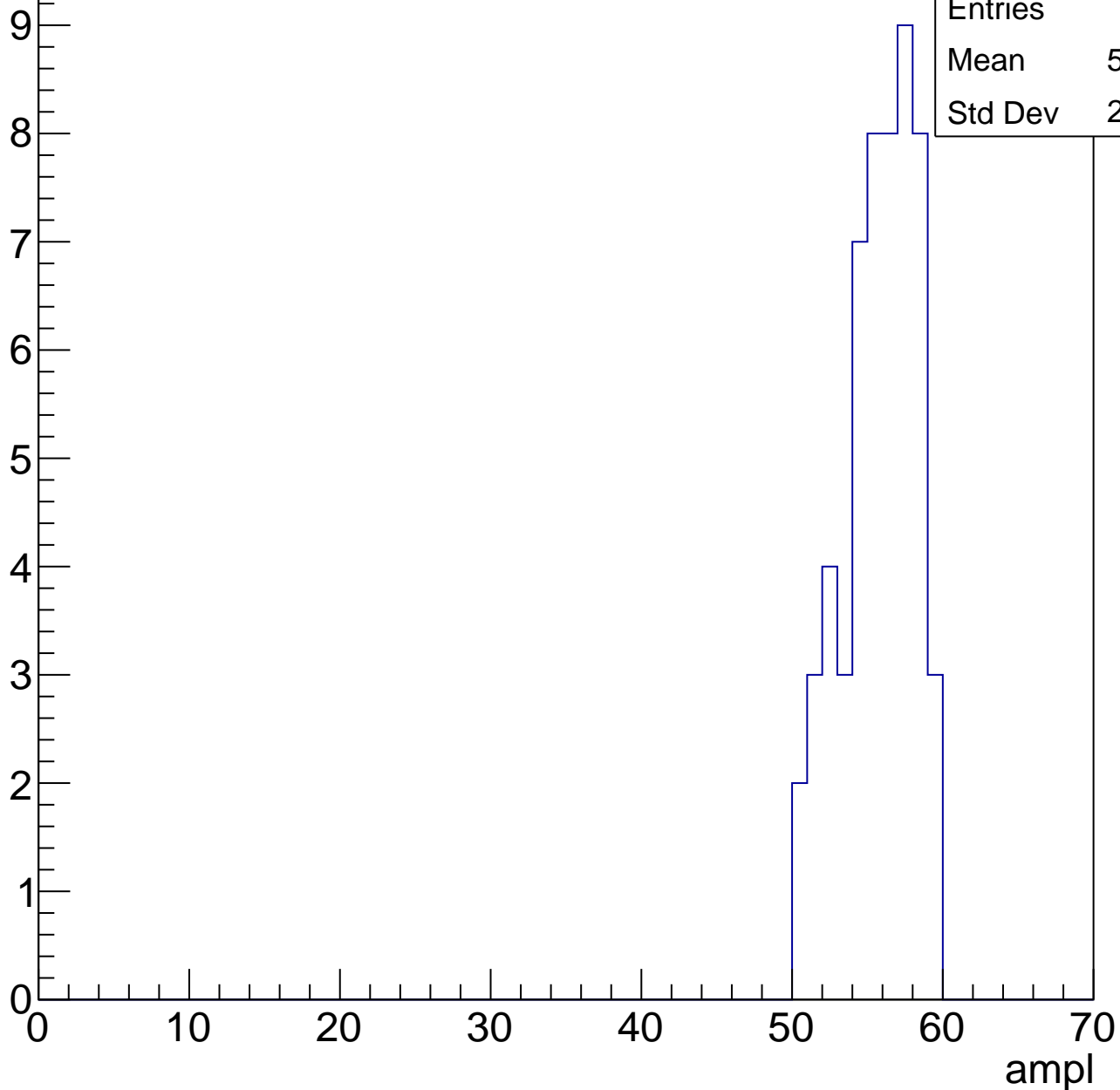
Entries	63
Mean	49.65
Std Dev	3.198



# B1L003S, U11-ch67, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

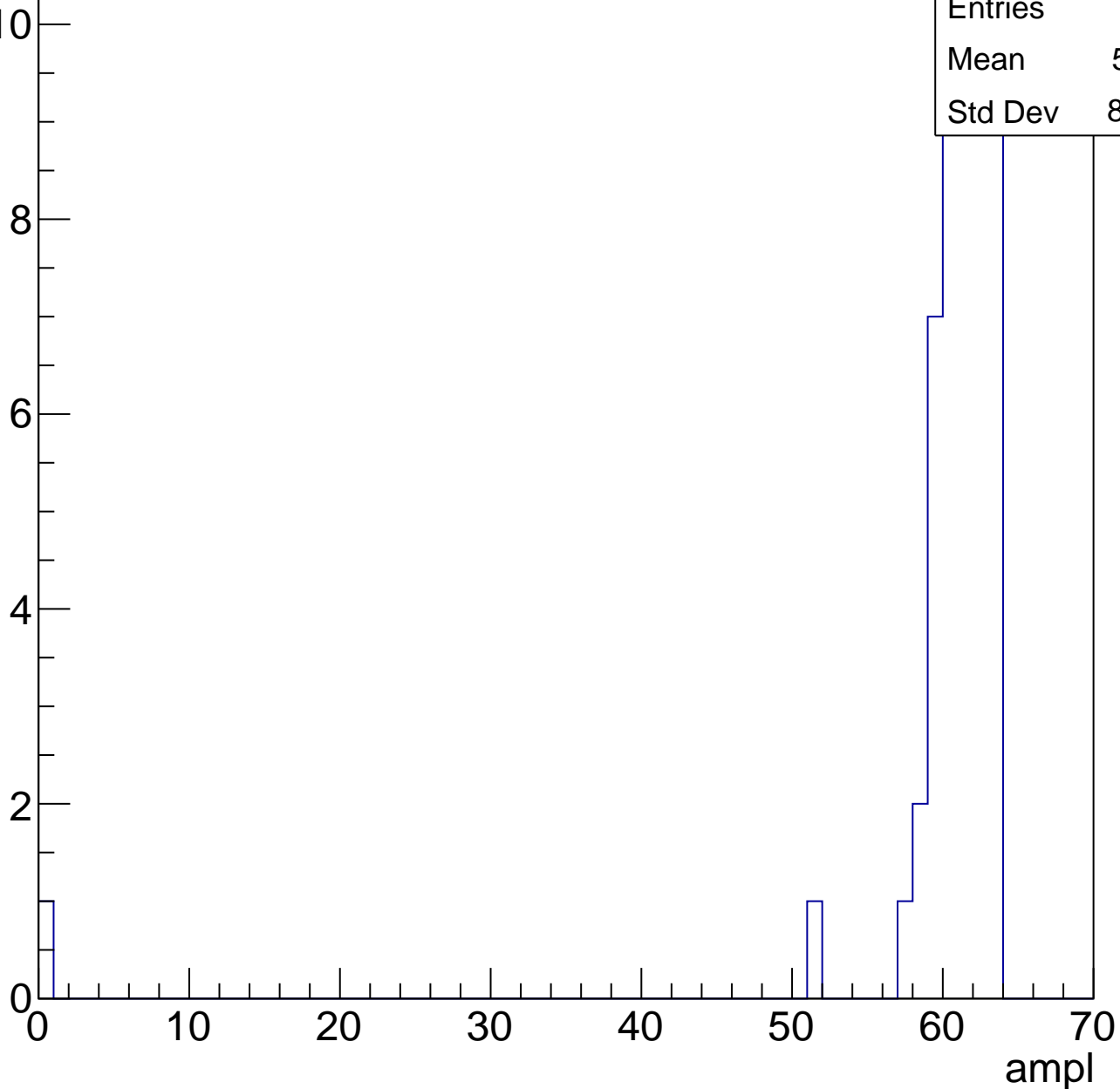


# B1L003S, U11-ch67, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	49
Mean	59.41
Std Dev	8.822



# B1L003S, U11-ch67, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch67, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L003S, U11-ch68, adc0

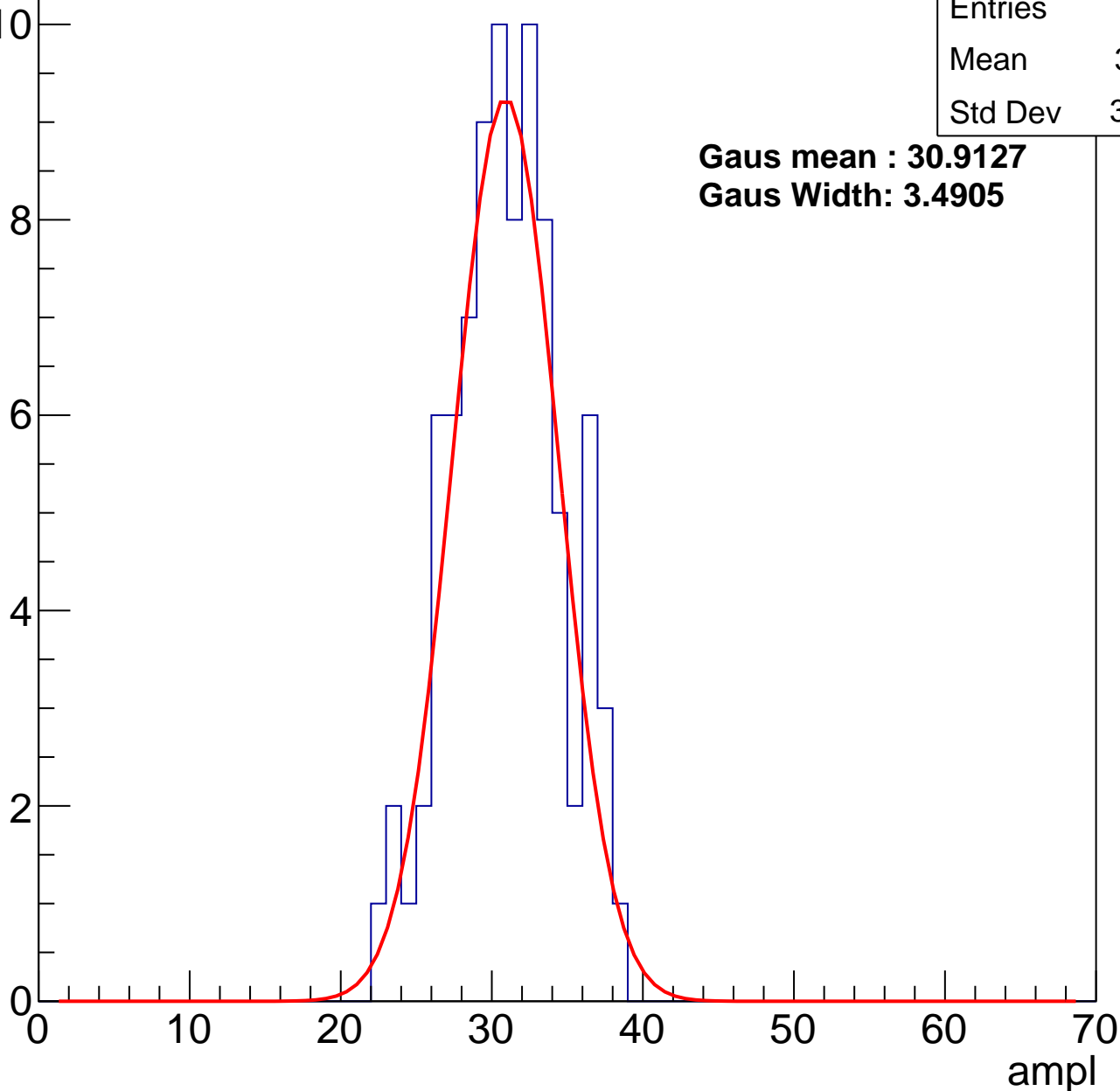
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	87
Mean	30.51
Std Dev	3.539

**Gaus mean : 30.9127**

**Gaus Width: 3.4905**



# B1L003S, U11-ch68, adc1

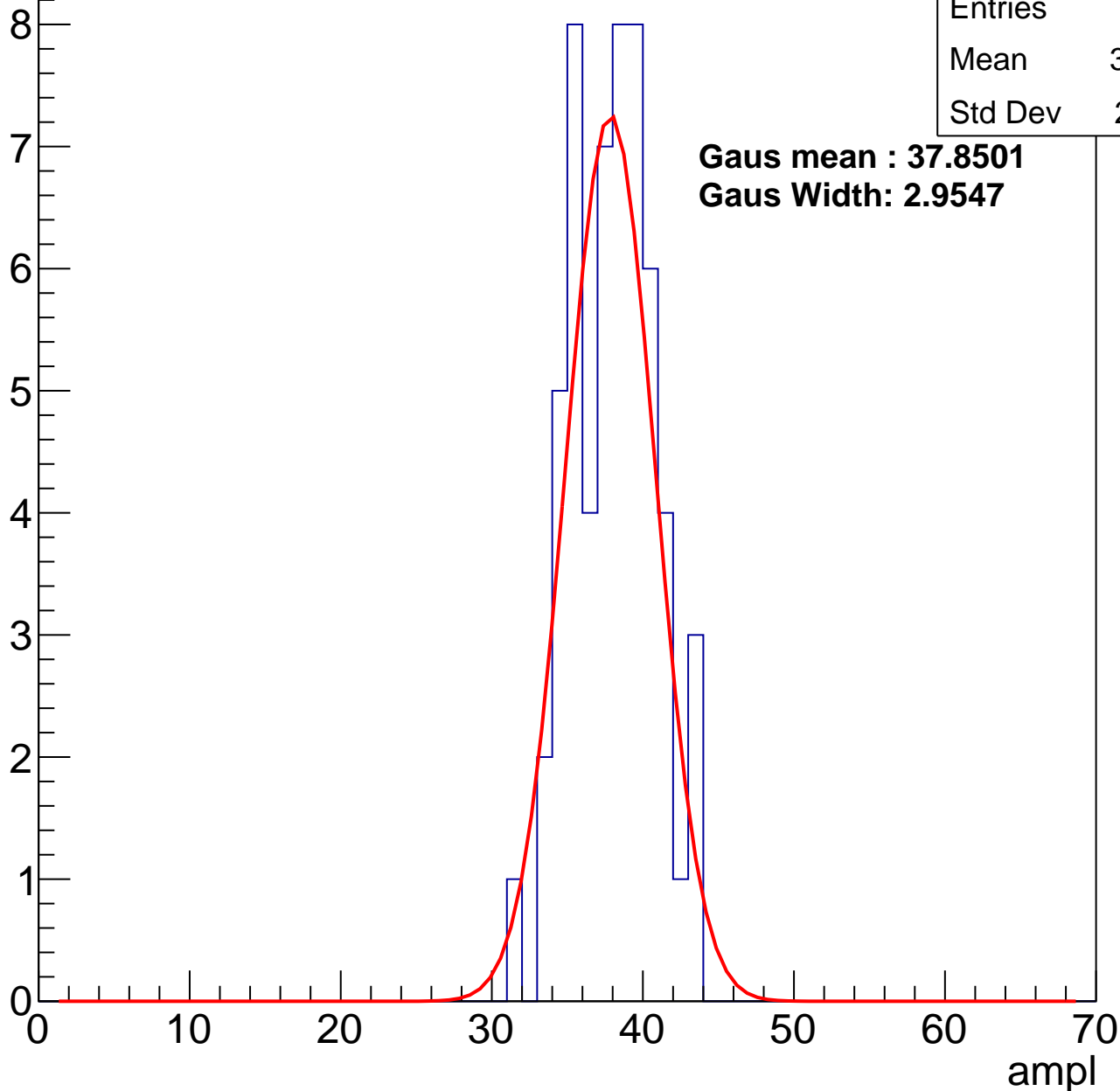
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	37.56
Std Dev	2.721

**Gaus mean : 37.8501**

**Gaus Width: 2.9547**



# B1L003S, U11-ch68, adc2

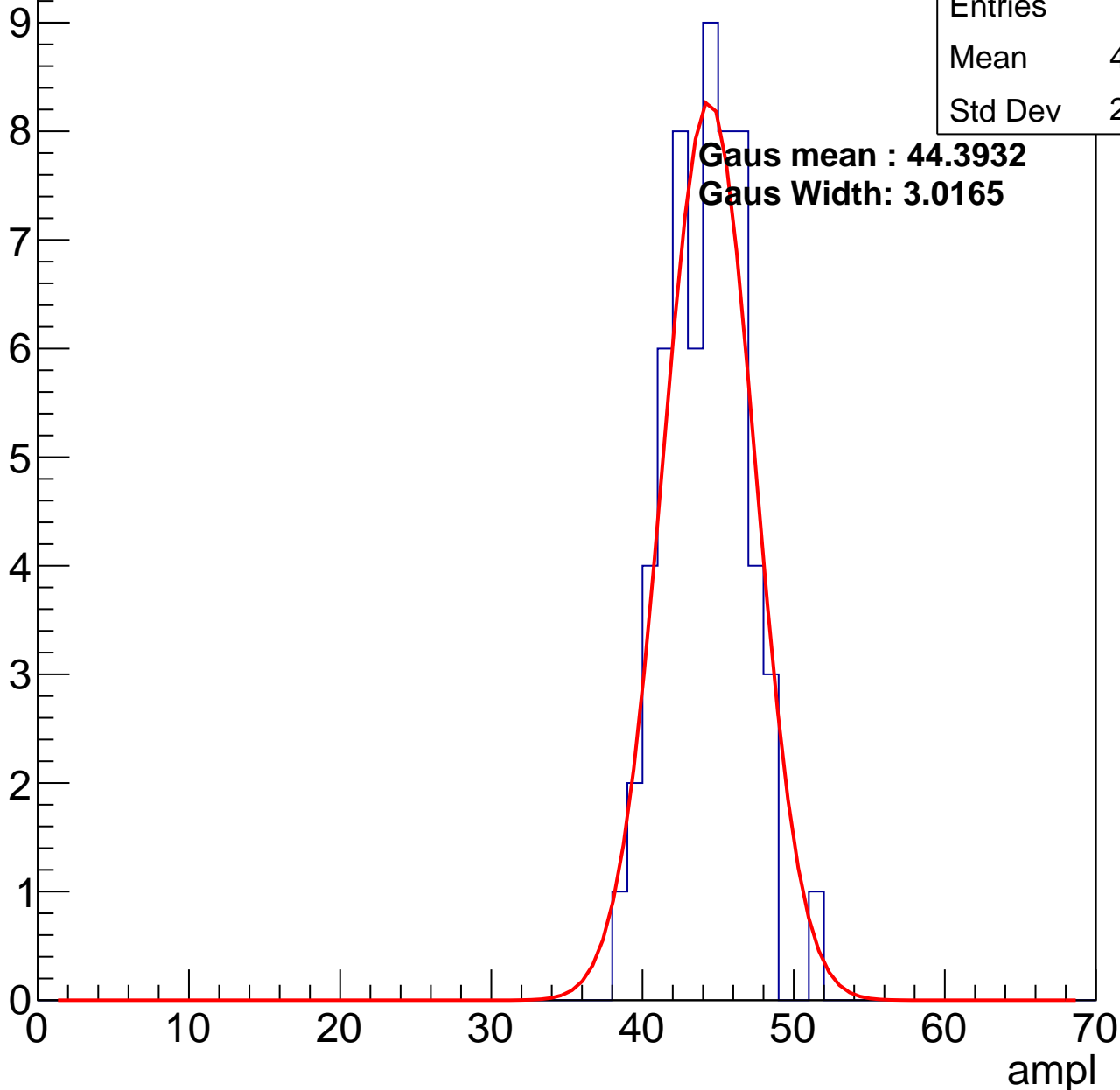
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	43.72
Std Dev	2.615

**Gaus mean : 44.3932**

**Gaus Width: 3.0165**



# B1L003S, U11-ch68, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	66
Mean	50.08
Std Dev	3.12

Entry

10

8

6

4

2

0

0

10

20

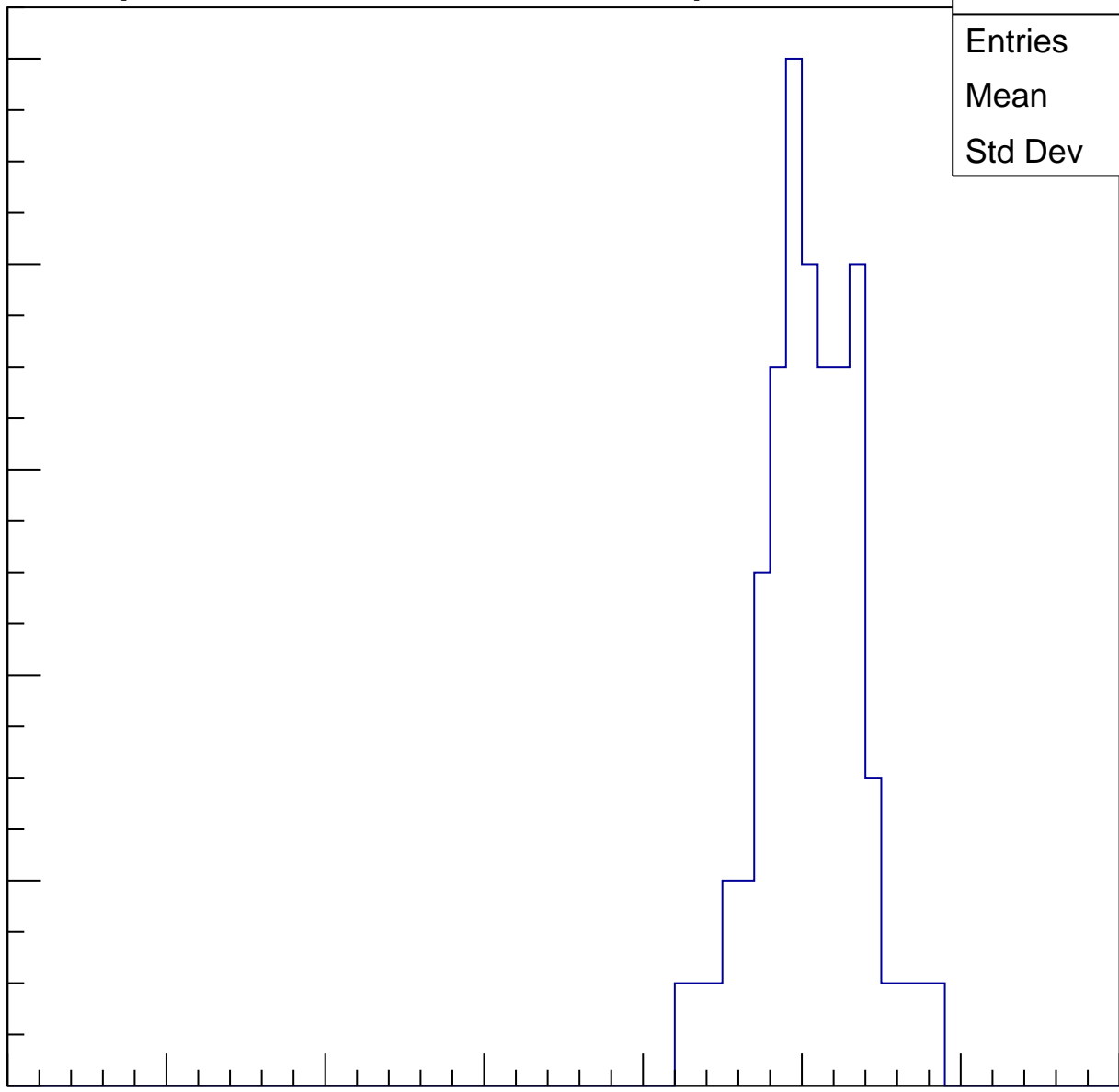
30

40

50

60

ampl

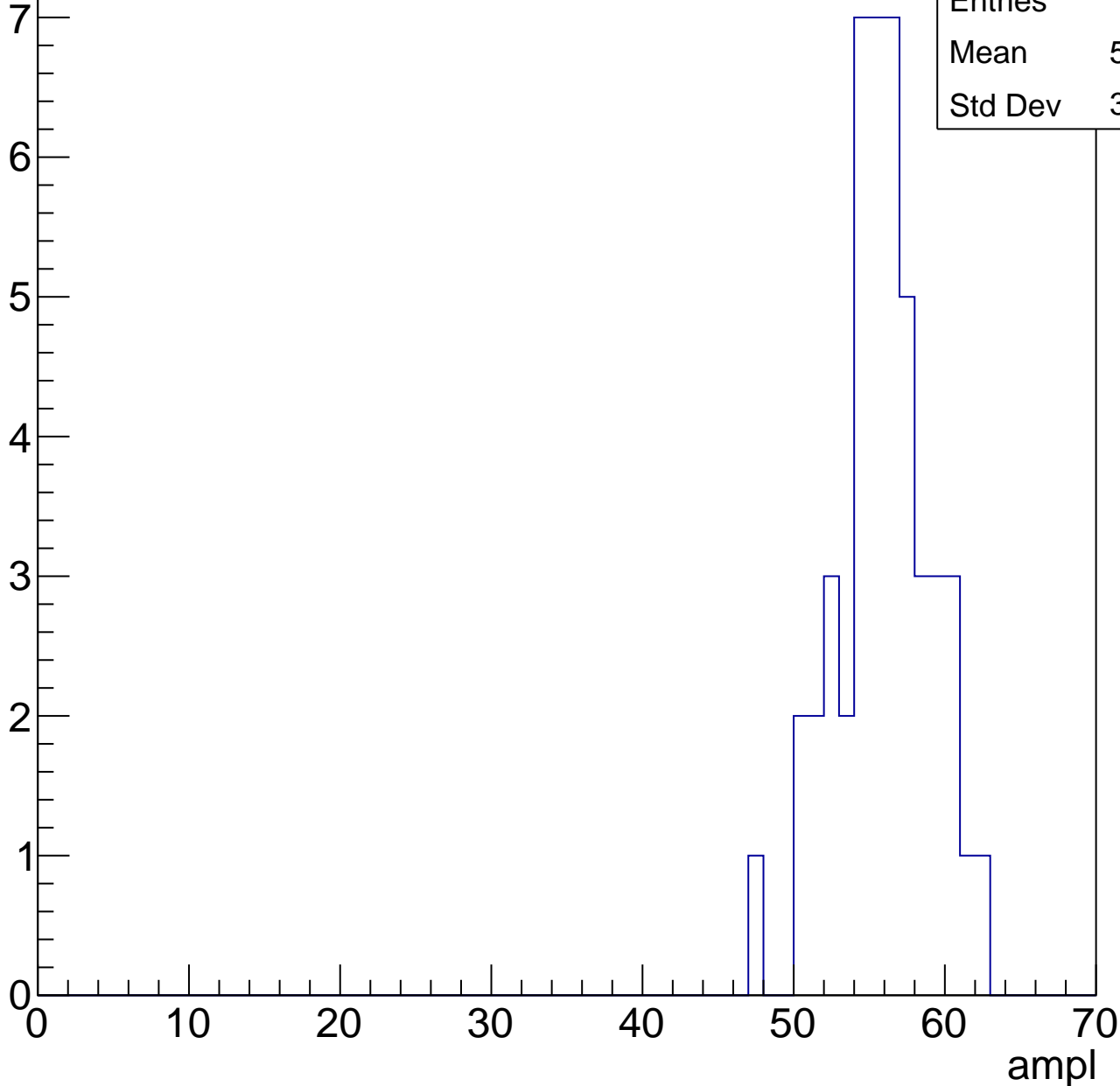


# B1L003S, U11-ch68, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

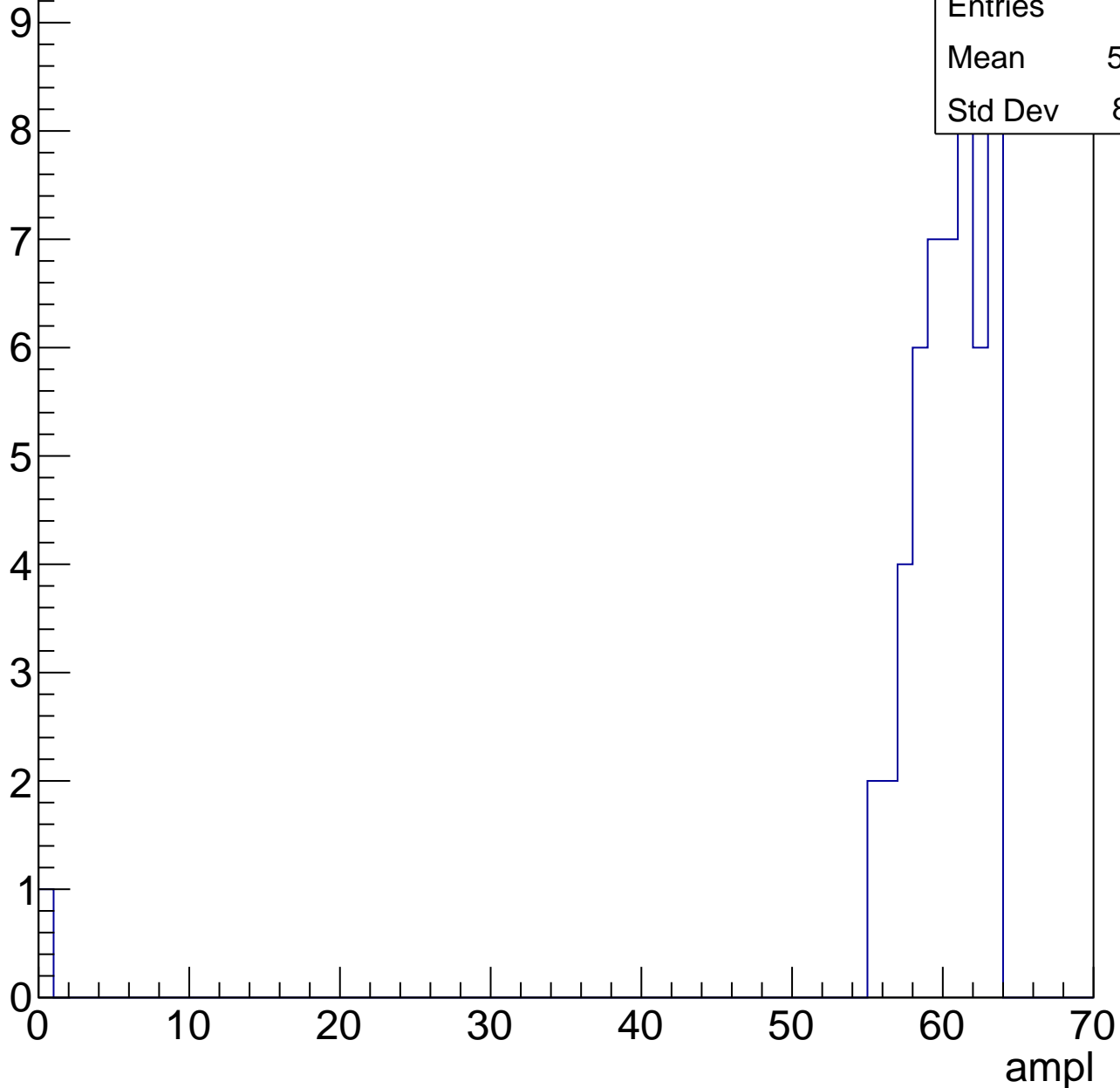
Entries	47
Mean	55.43
Std Dev	3.065



# B1L003S, U11-ch68, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U11-ch68, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch68, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U11-ch69, adc0

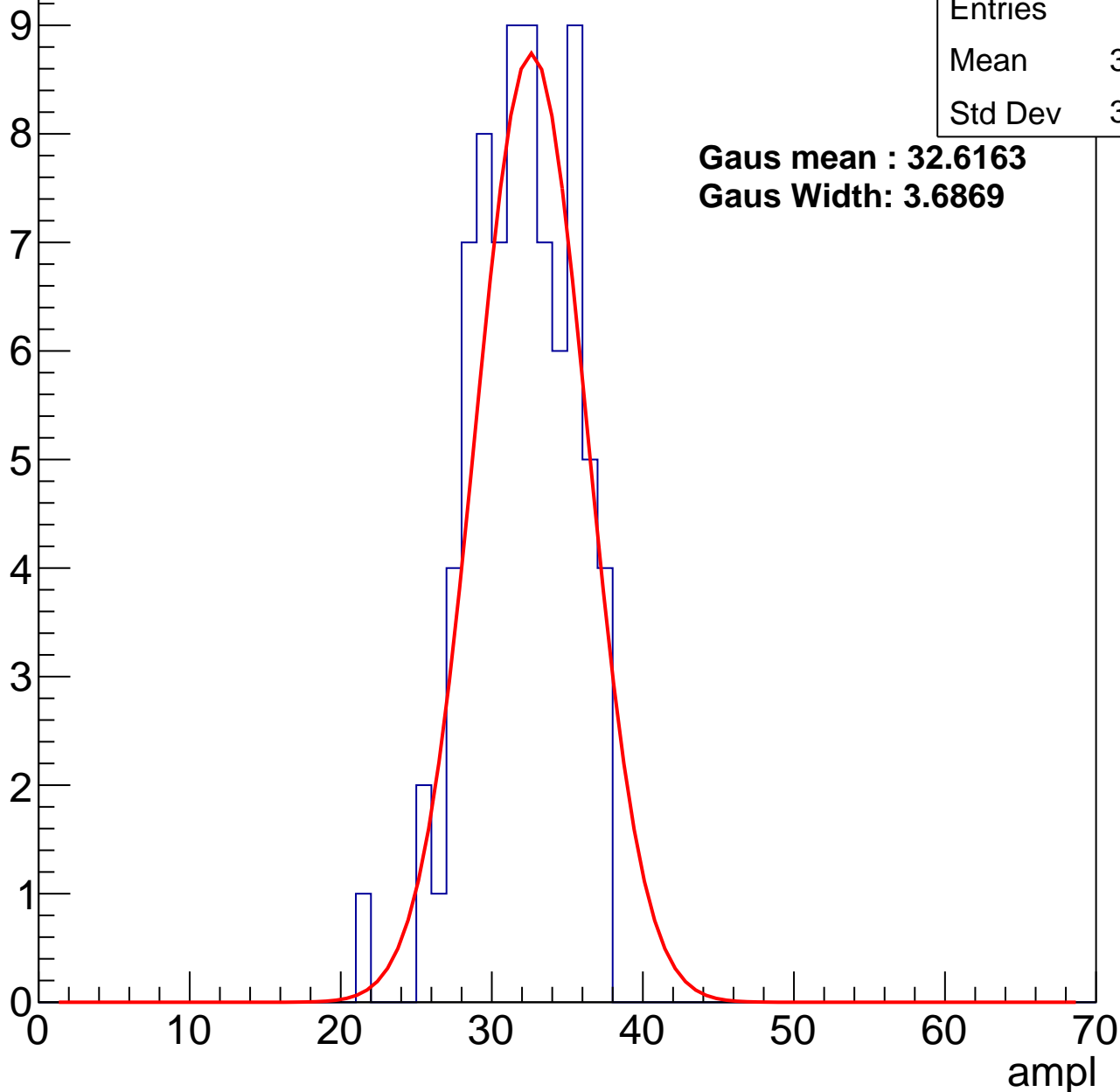
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	79
Mean	31.49
Std Dev	3.276

**Gaus mean : 32.6163**

**Gaus Width: 3.6869**



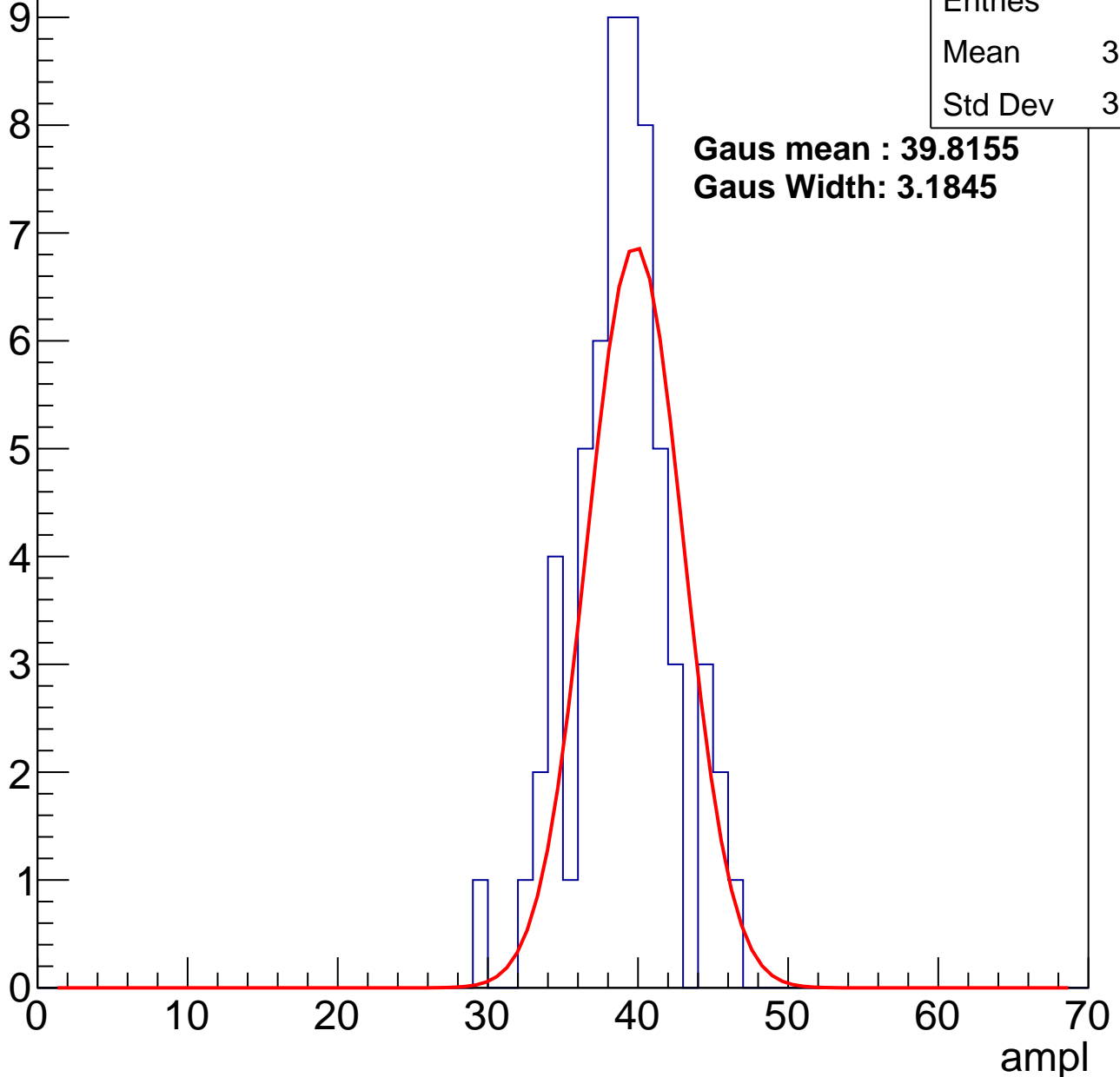
# B1L003S, U11-ch69, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	38.53
Std Dev	3.299

**Gaus mean : 39.8155**  
**Gaus Width: 3.1845**



# B1L003S, U11-ch69, adc2

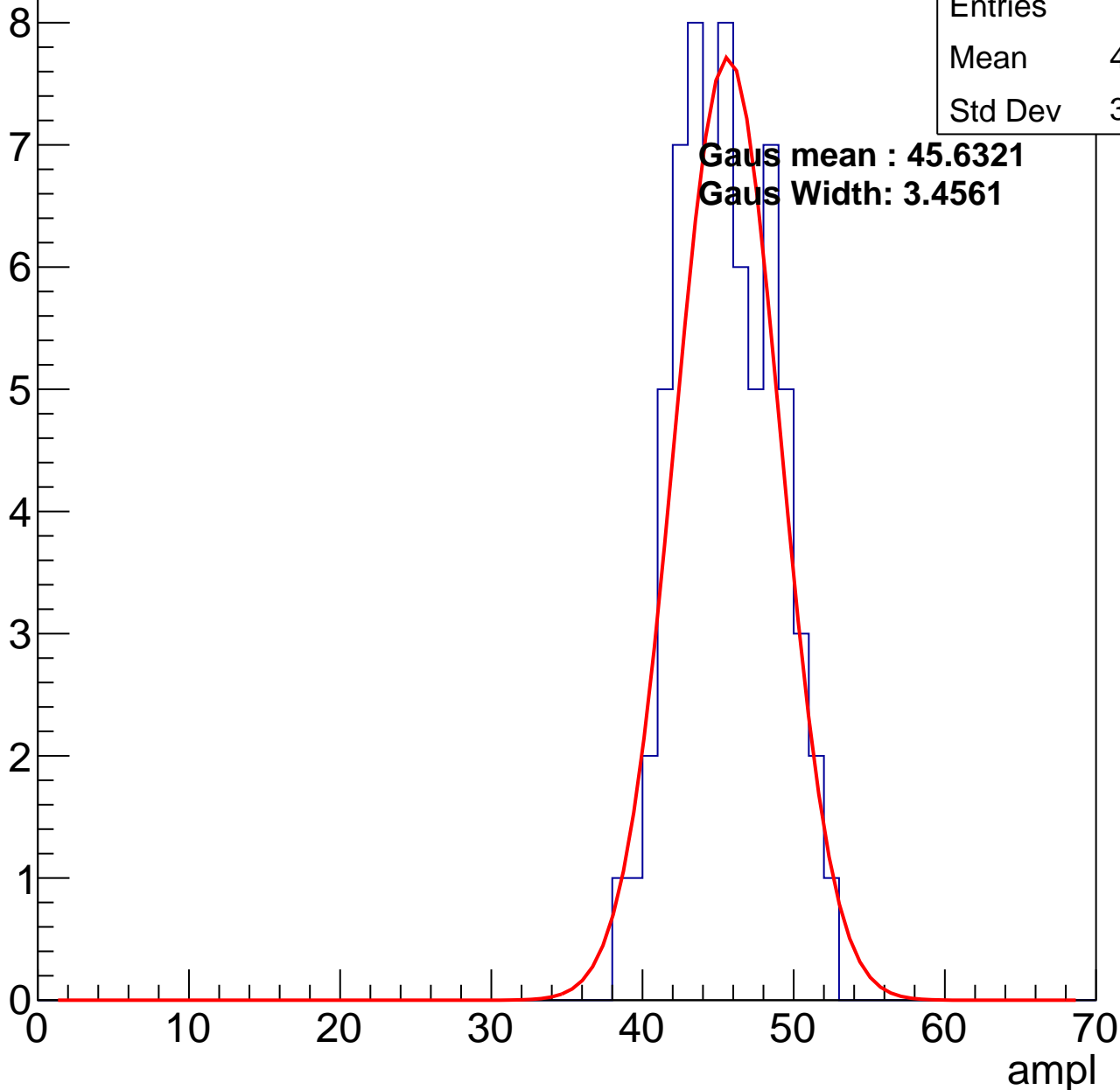
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	45.06
Std Dev	3.166

**Gaus mean : 45.6321**

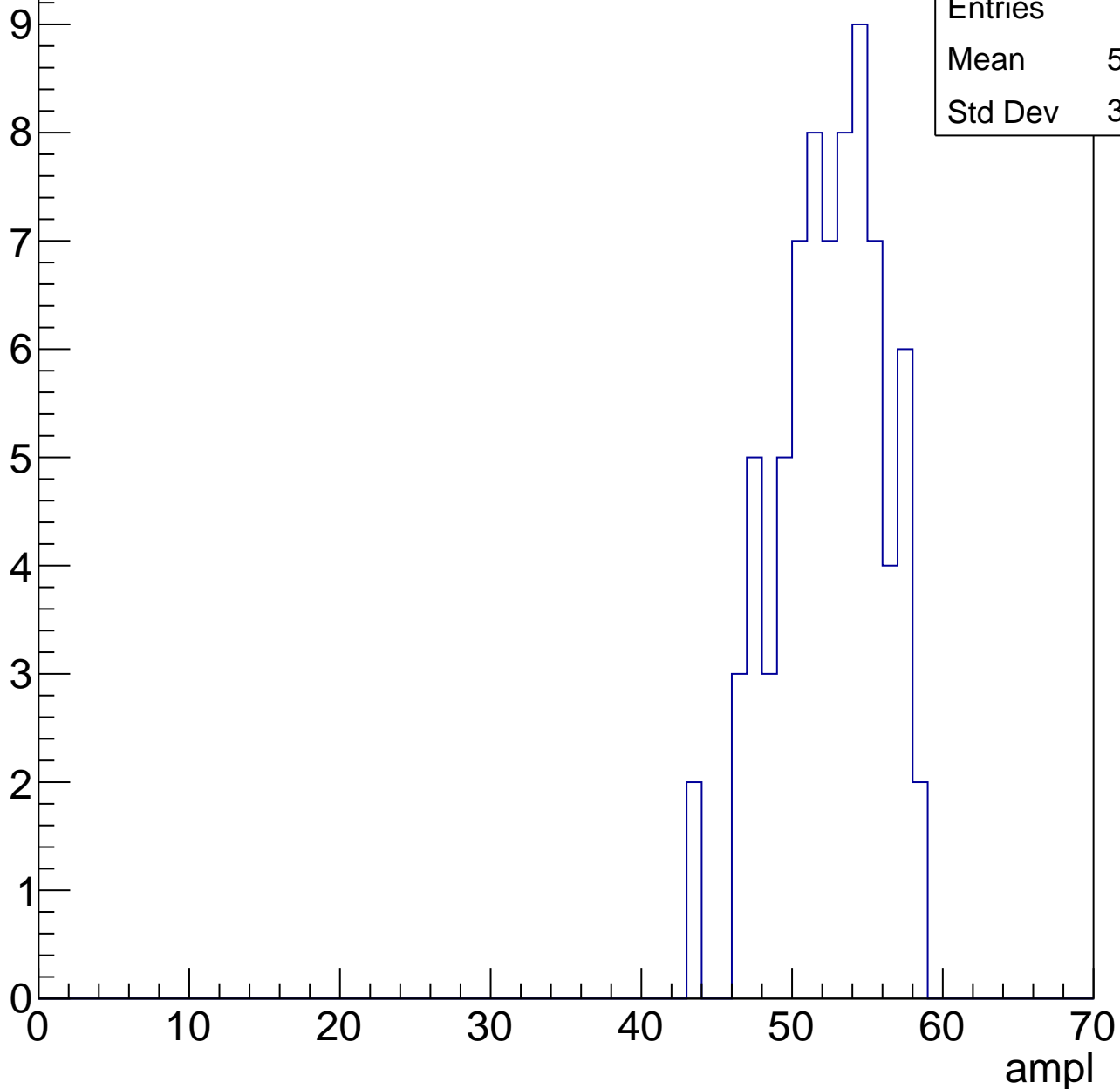
**Gaus Width: 3.4561**



# B1L003S, U11-ch69, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

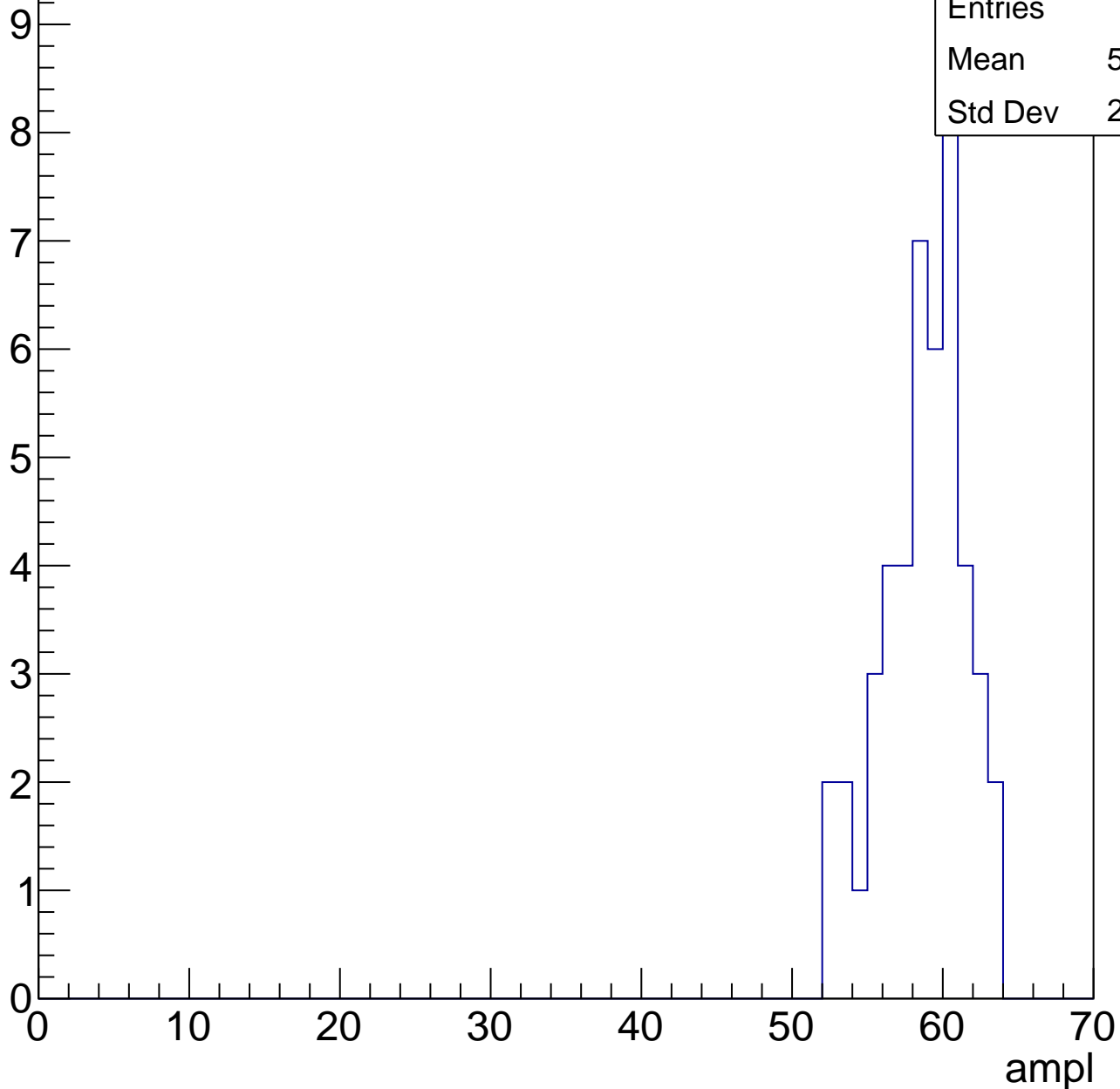
Entry



# B1L003S, U11-ch69, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

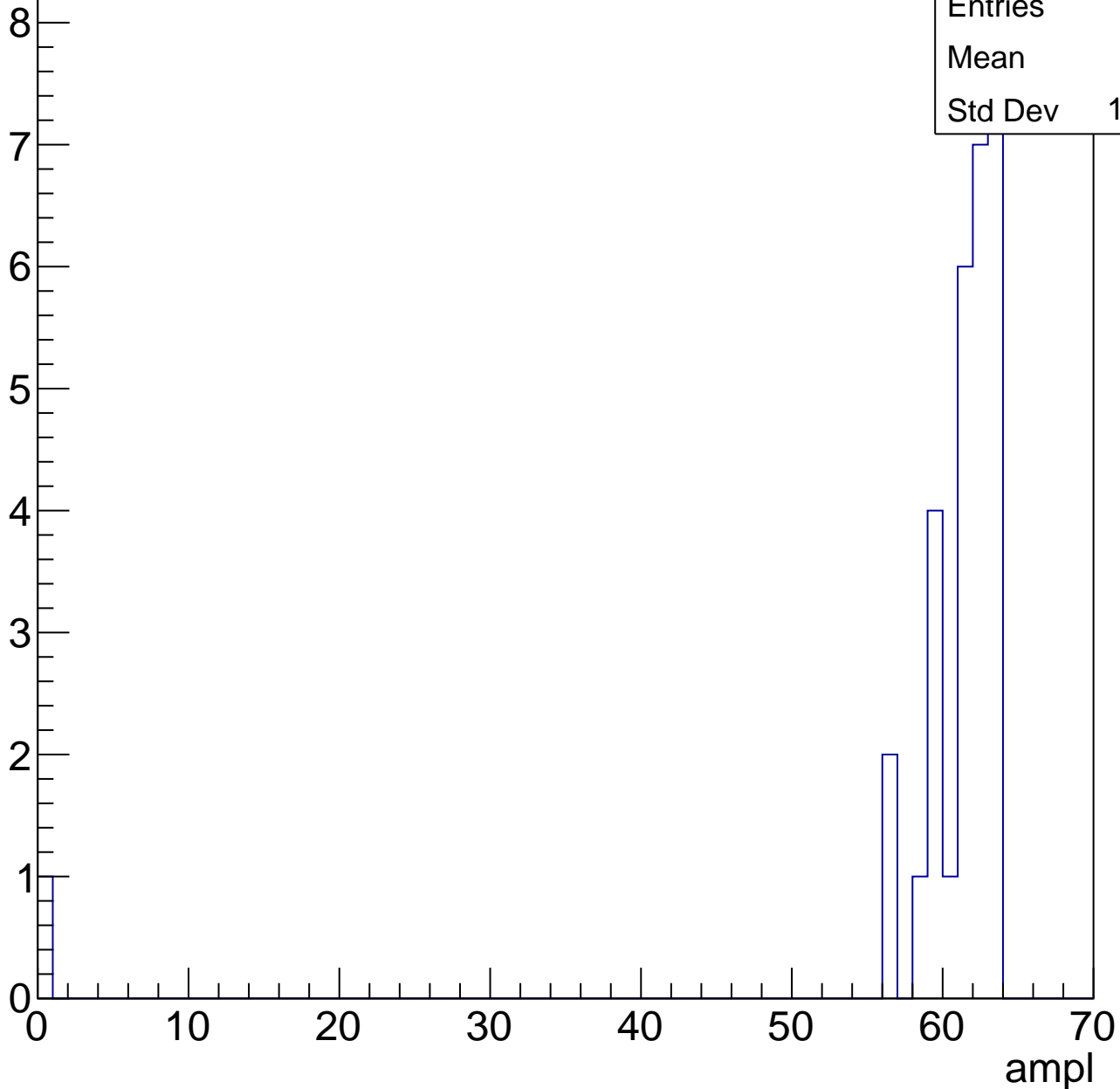


# B1L003S, U11-ch69, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	30
Mean	59
Std Dev	11.13



# B1L003S, U11-ch69, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L003S, U11-ch69, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L003S, U11-ch70, adc0

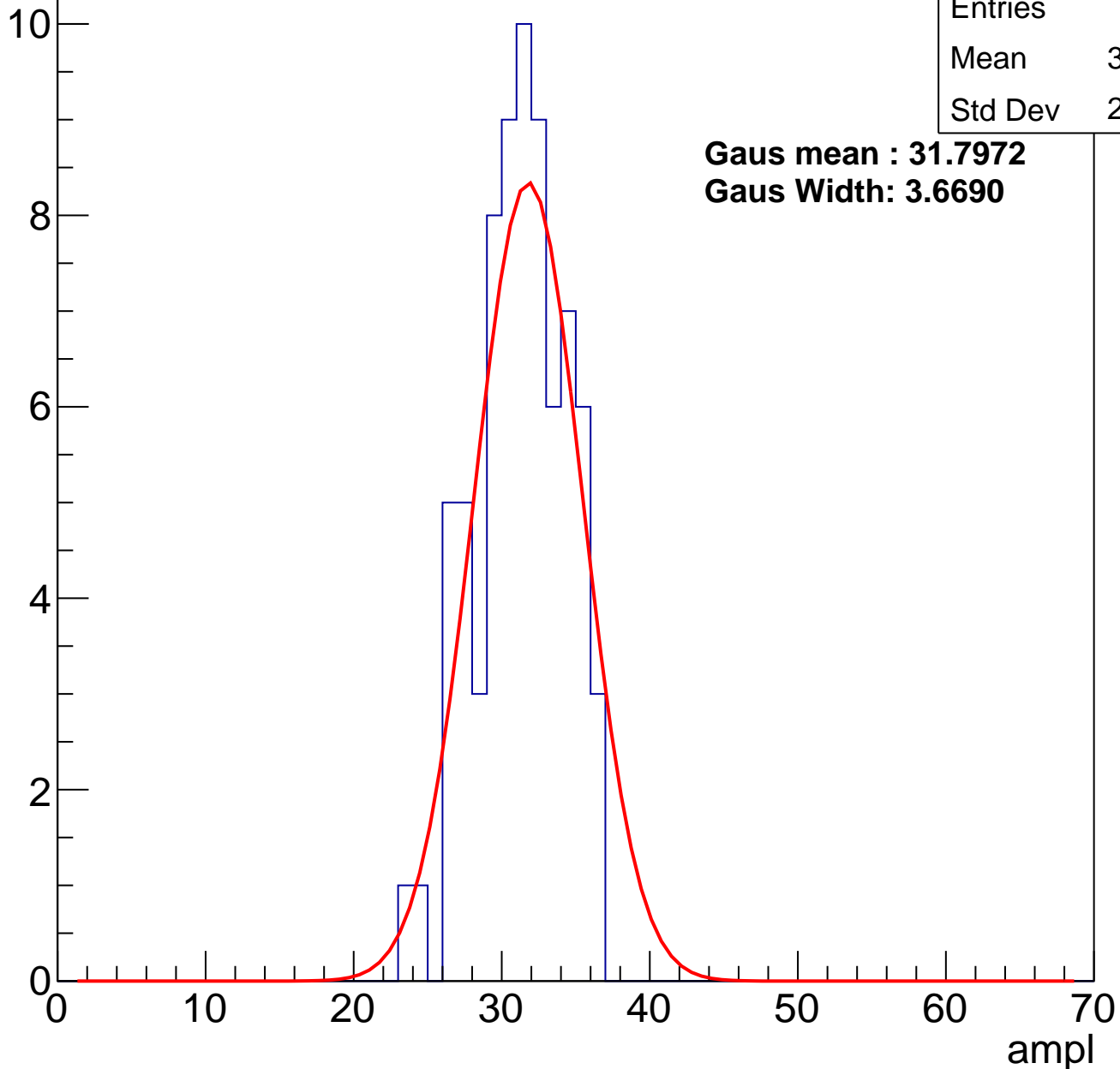
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	73
Mean	30.82
Std Dev	2.986

**Gaus mean : 31.7972**

**Gaus Width: 3.6690**

Entry

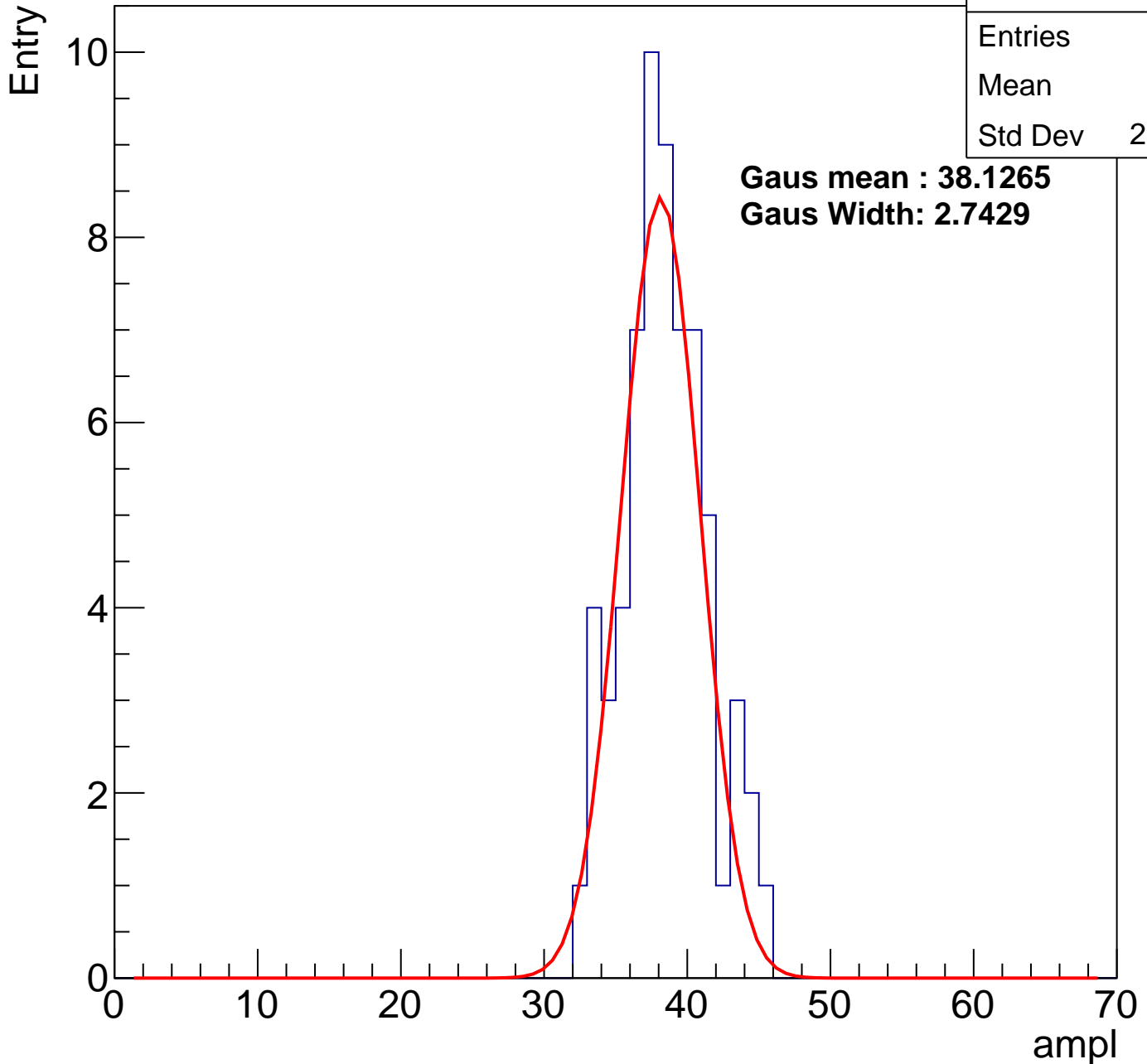


# B1L003S, U11-ch70, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	64
Mean	38
Std Dev	2.932

**Gaus mean : 38.1265**  
**Gaus Width: 2.7429**



# B1L003S, U11-ch70, adc2

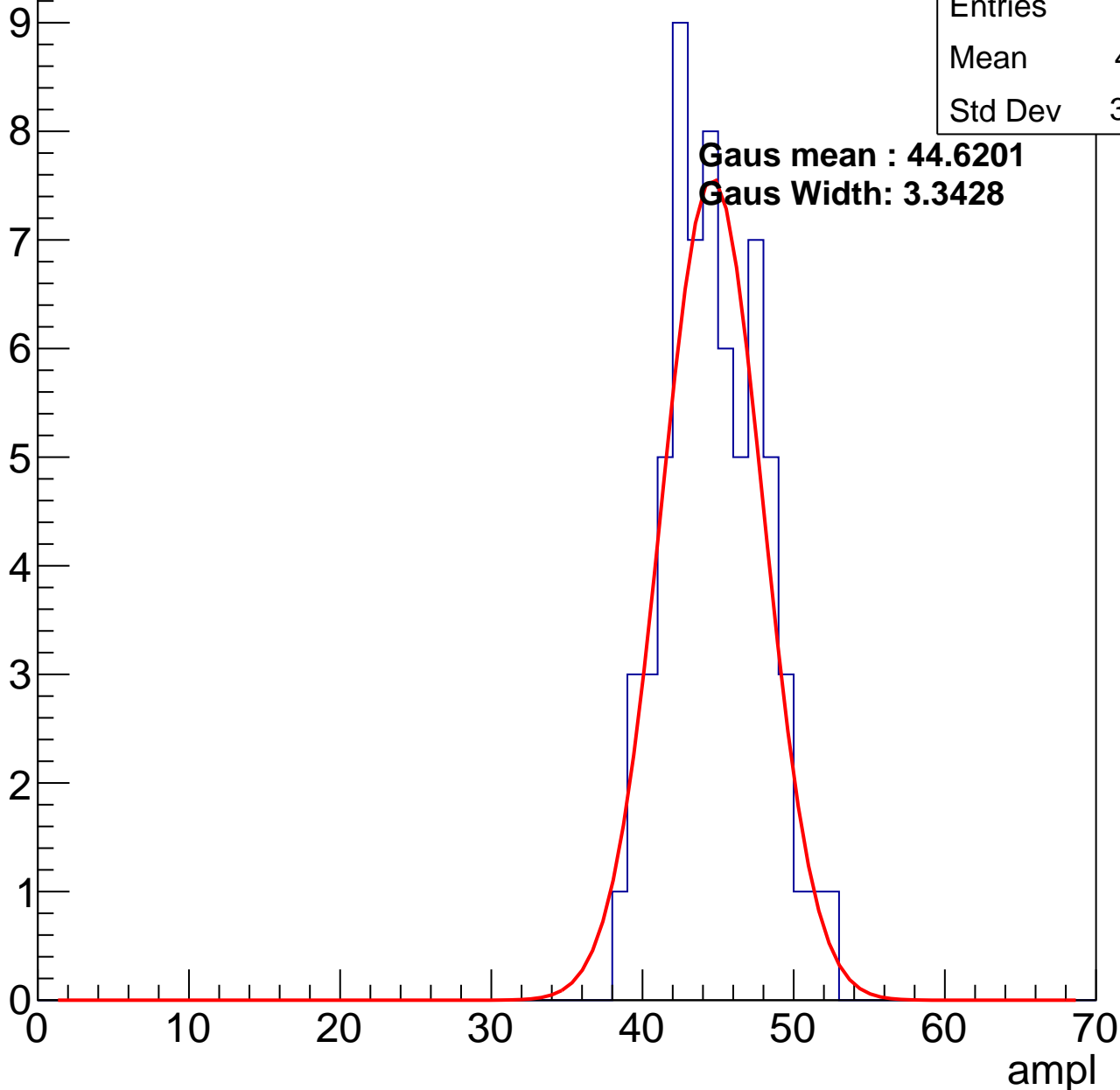
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	44.31
Std Dev	3.123

**Gaus mean : 44.6201**

**Gaus Width: 3.3428**

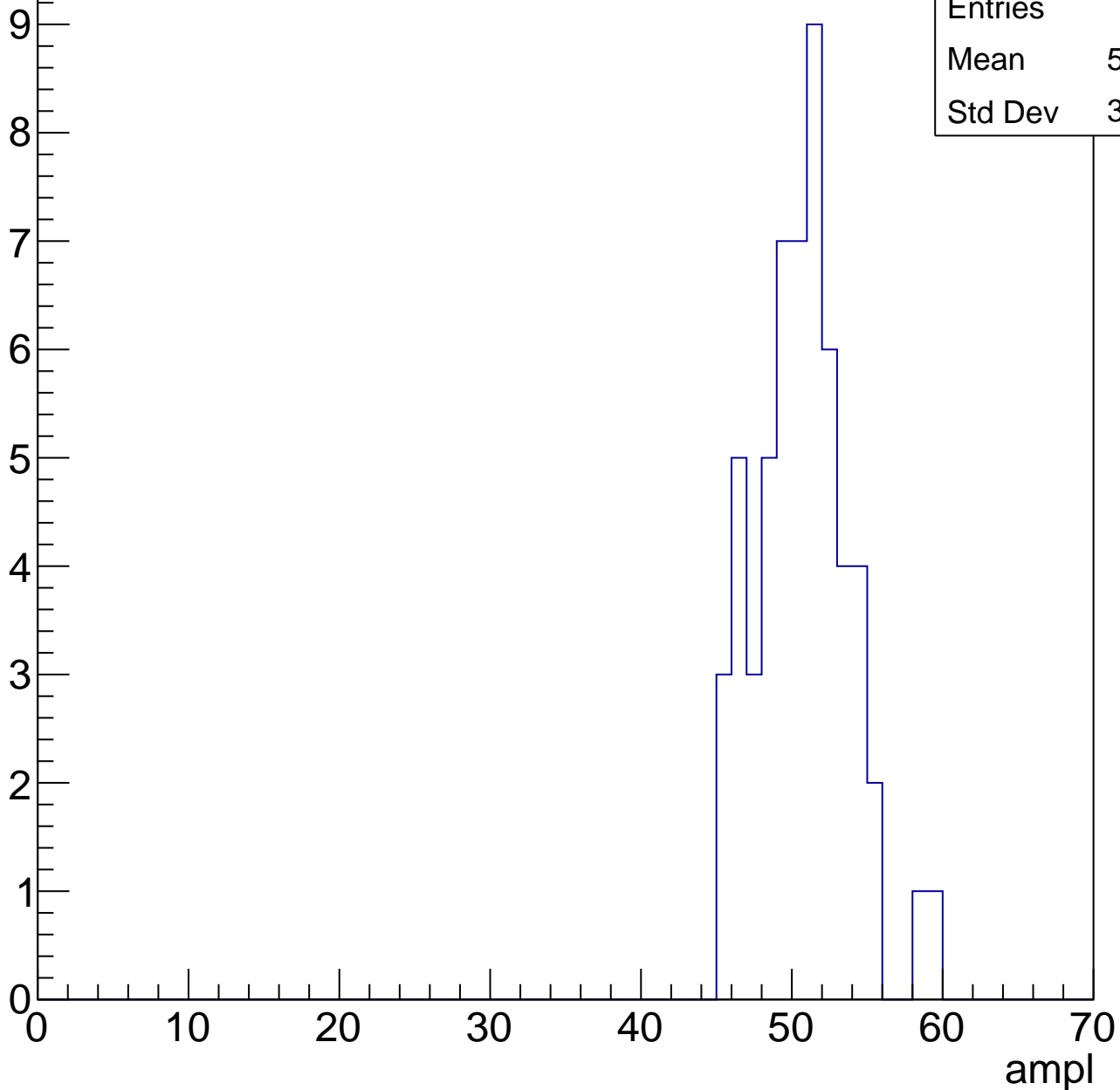


# B1L003S, U11-ch70, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	50.26
Std Dev	3.058



# B1L003S, U11-ch70, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

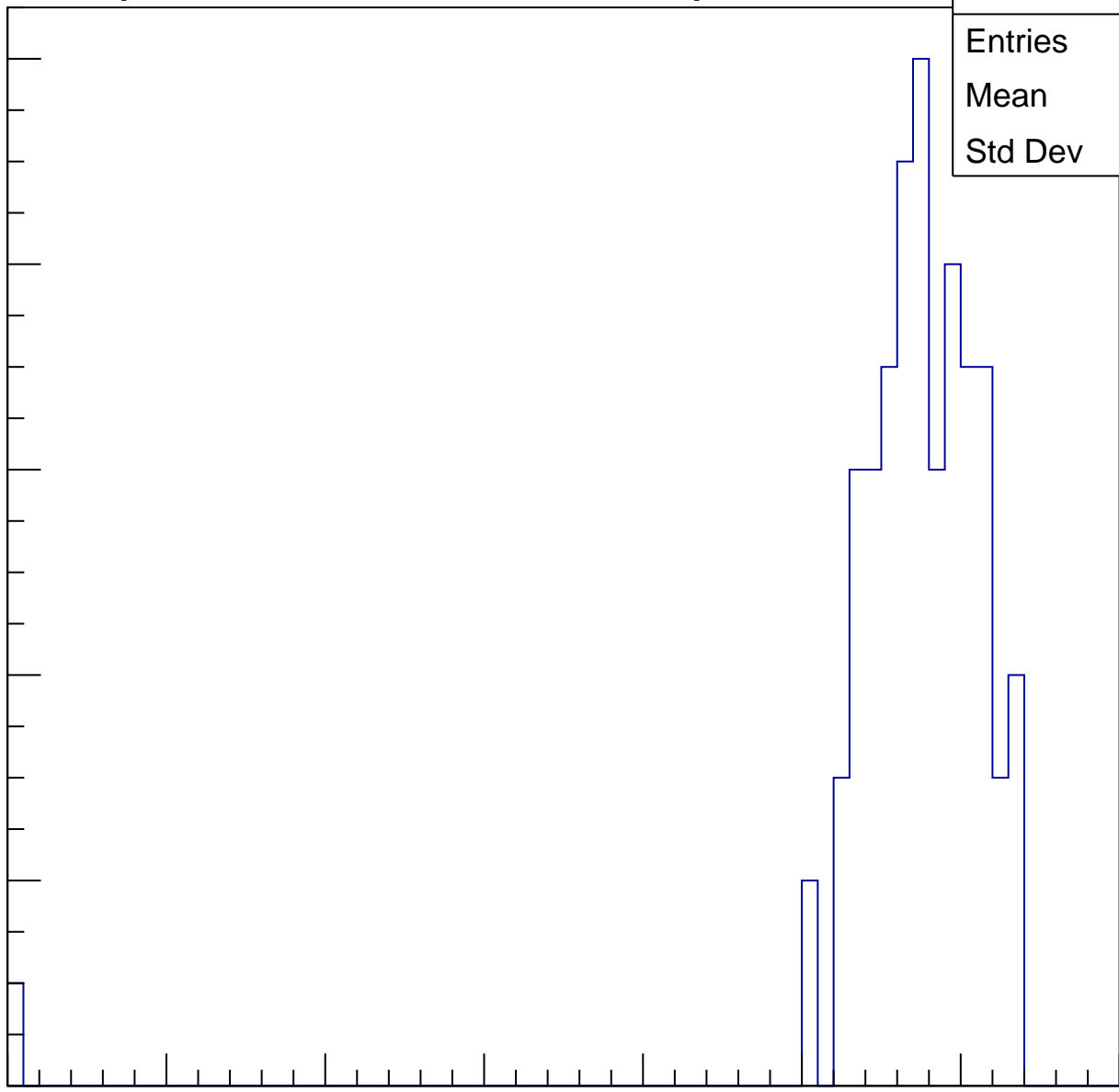
Entries	79
Mean	56.48
Std Dev	7.133

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

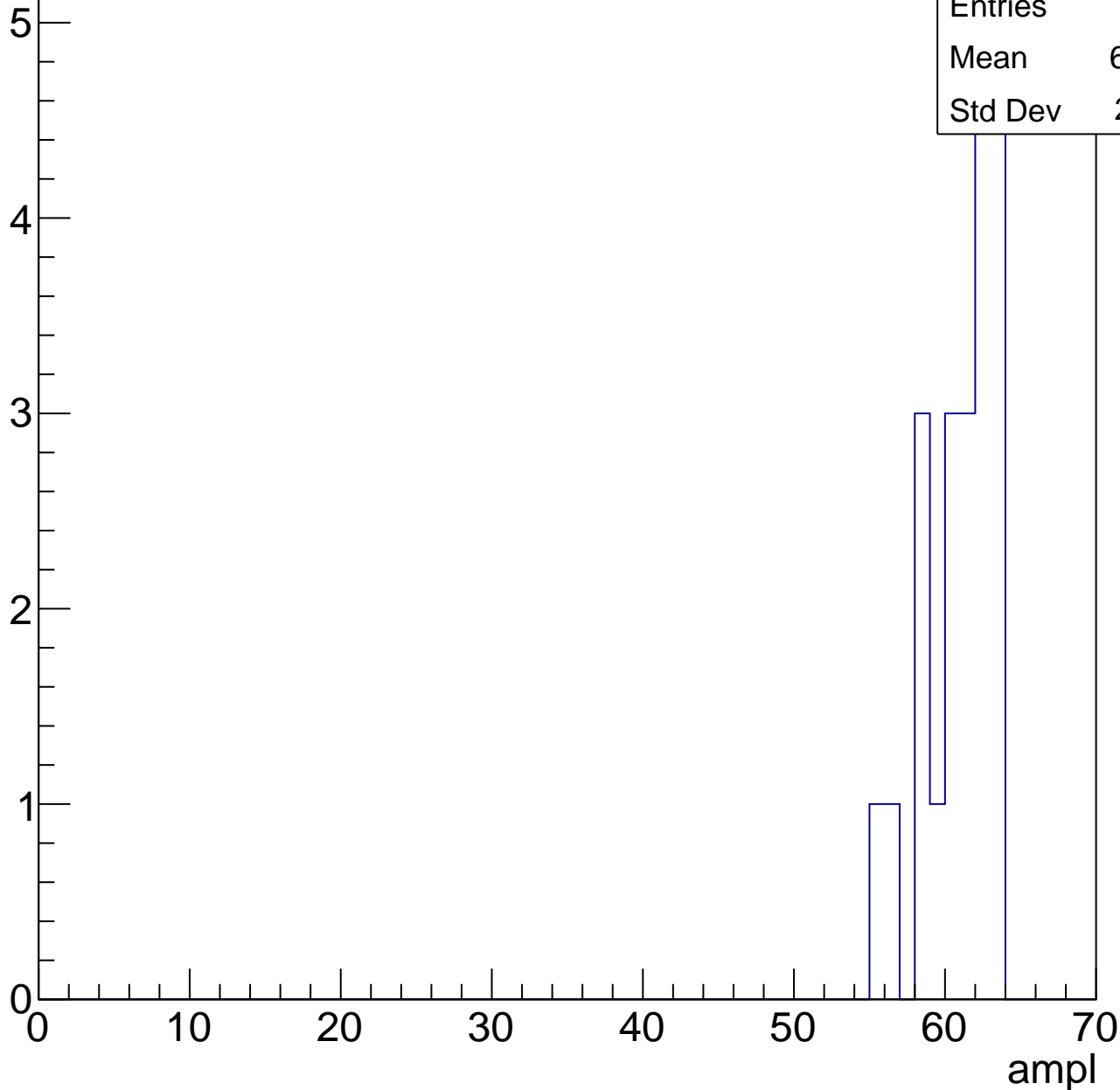


# B1L003S, U11-ch70, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	22
Mean	60.55
Std Dev	2.291



# B1L003S, U11-ch70, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch70, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L003S, U11-ch71, adc0

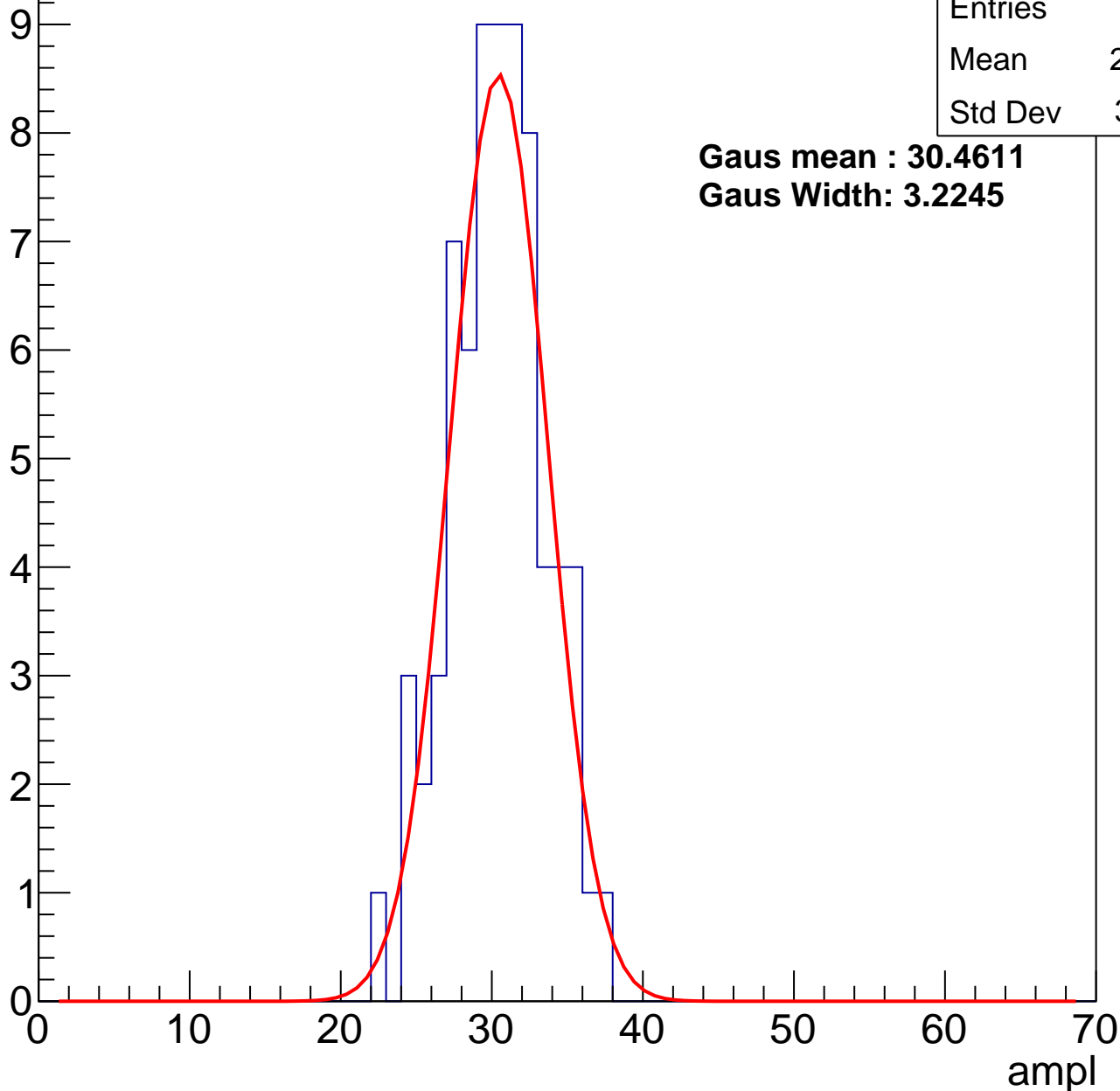
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	71
Mean	29.94
Std Dev	3.121

**Gaus mean : 30.4611**

**Gaus Width: 3.2245**



# B1L003S, U11-ch71, adc1

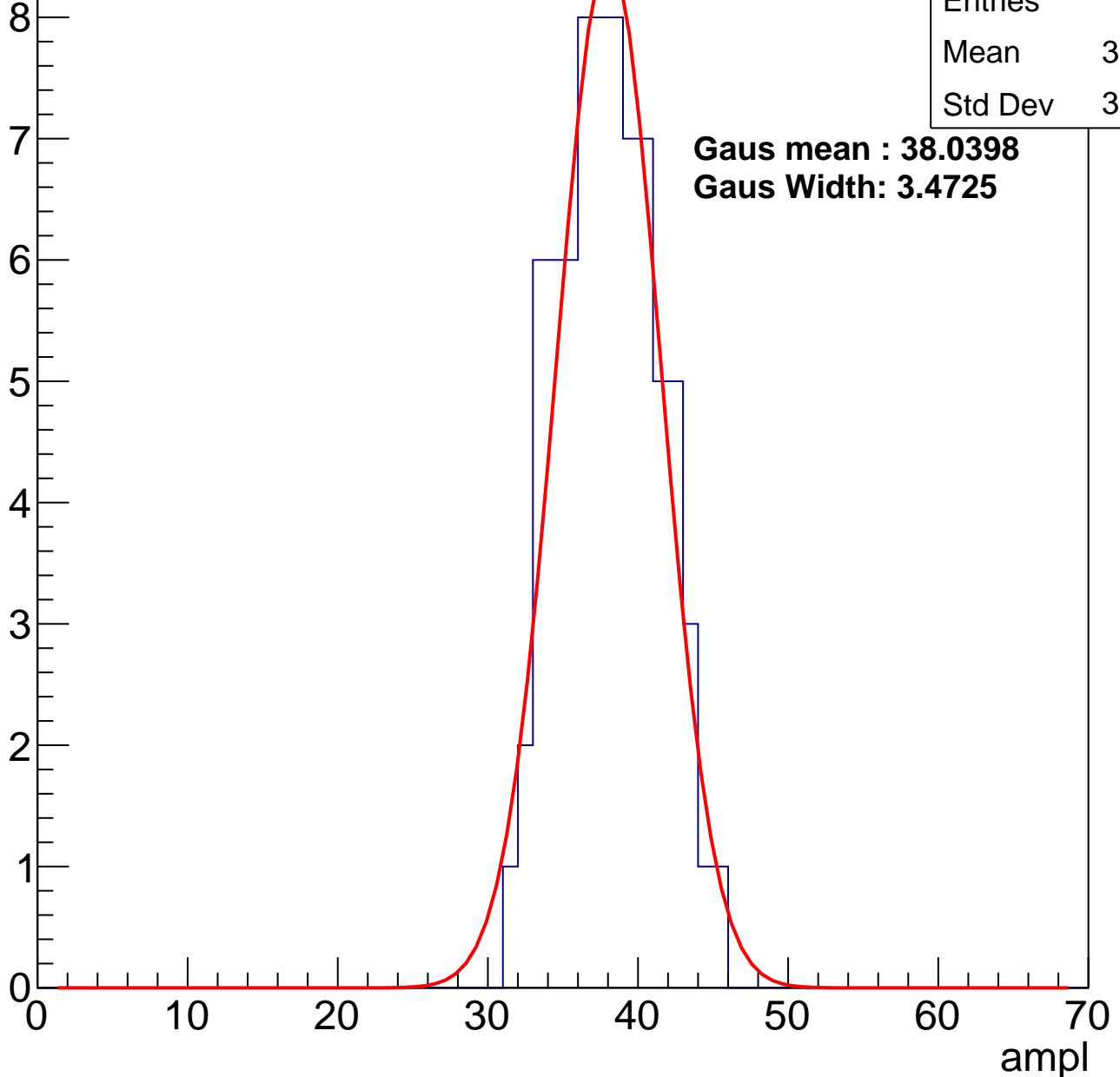
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	74
Mean	37.58
Std Dev	3.222

**Gaus mean : 38.0398**

**Gaus Width: 3.4725**



# B1L003S, U11-ch71, adc2

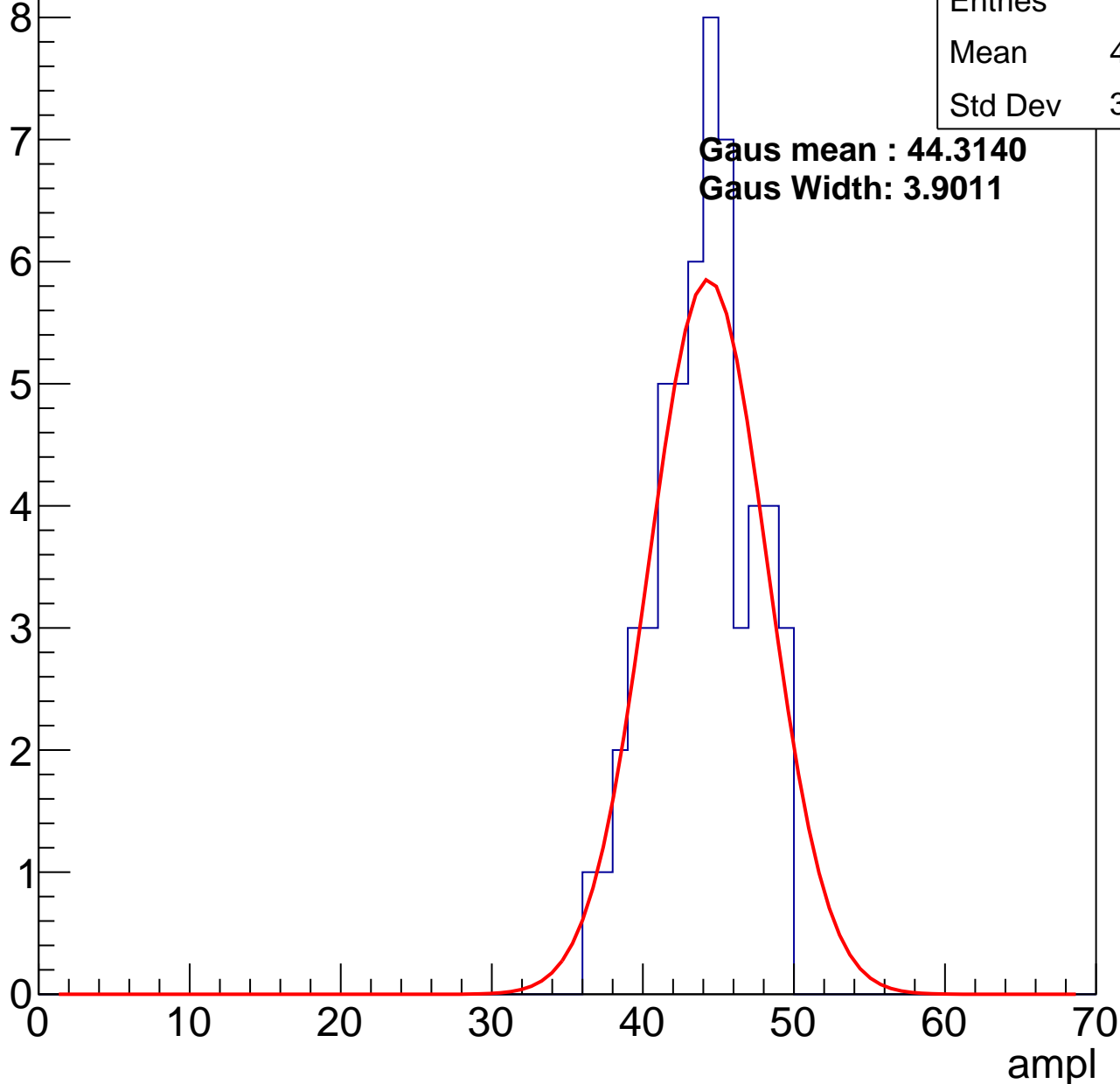
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	43.47
Std Dev	3.184

**Gaus mean : 44.3140**

**Gaus Width: 3.9011**

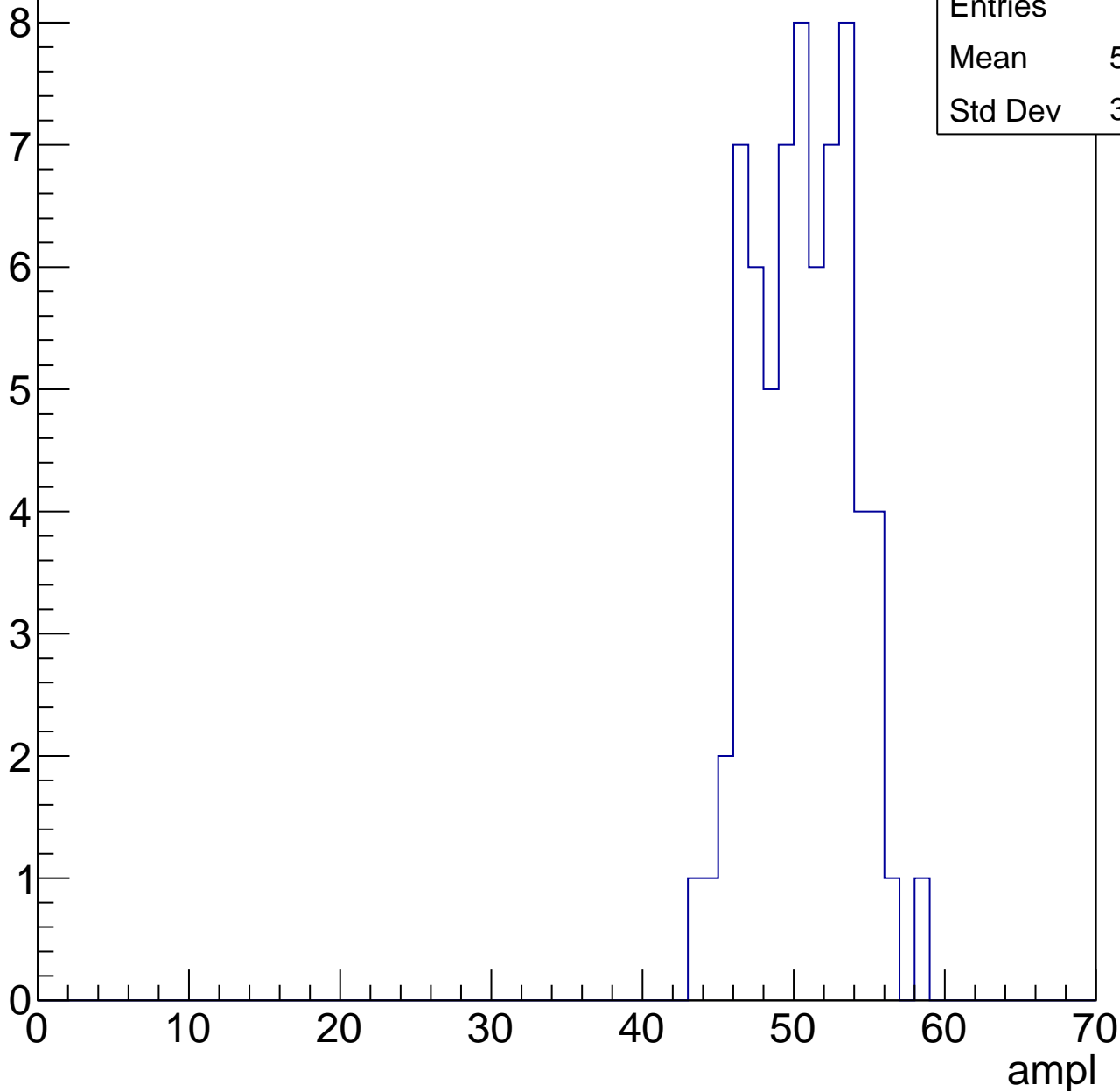


# B1L003S, U11-ch71, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	50.12
Std Dev	3.202

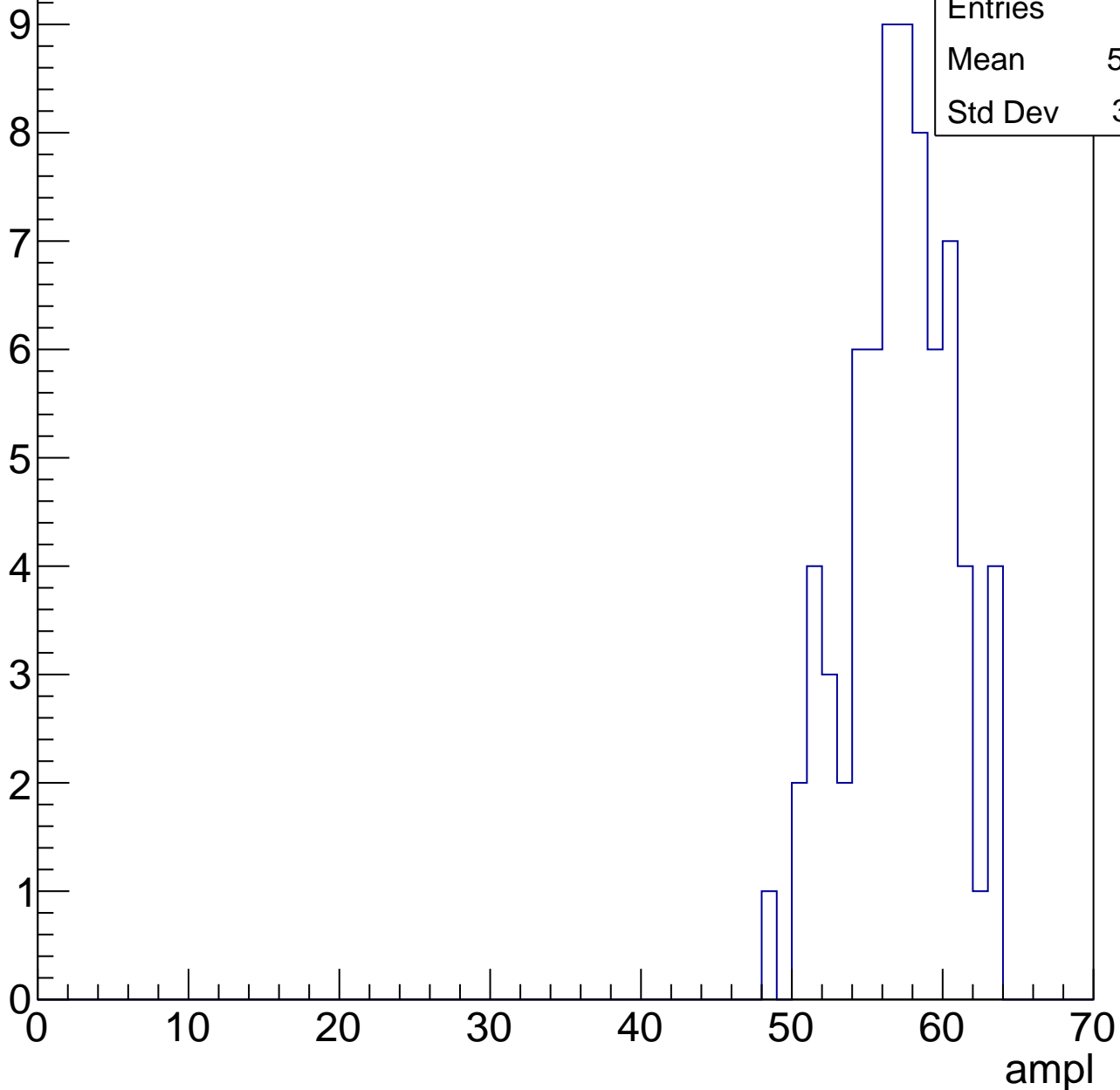


# B1L003S, U11-ch71, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

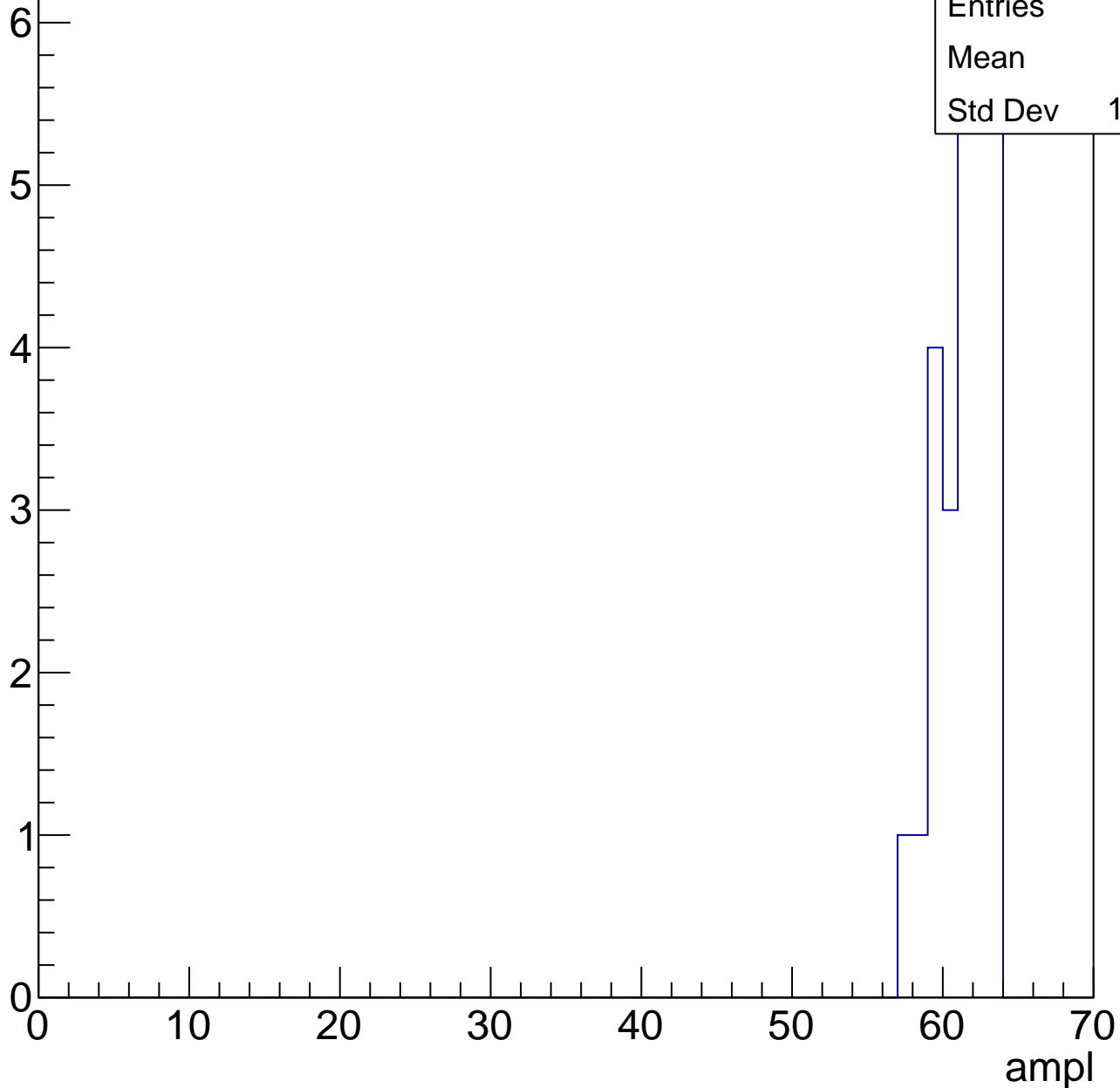
Entries	72
Mean	56.68
Std Dev	3.411



# B1L003S, U11-ch71, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

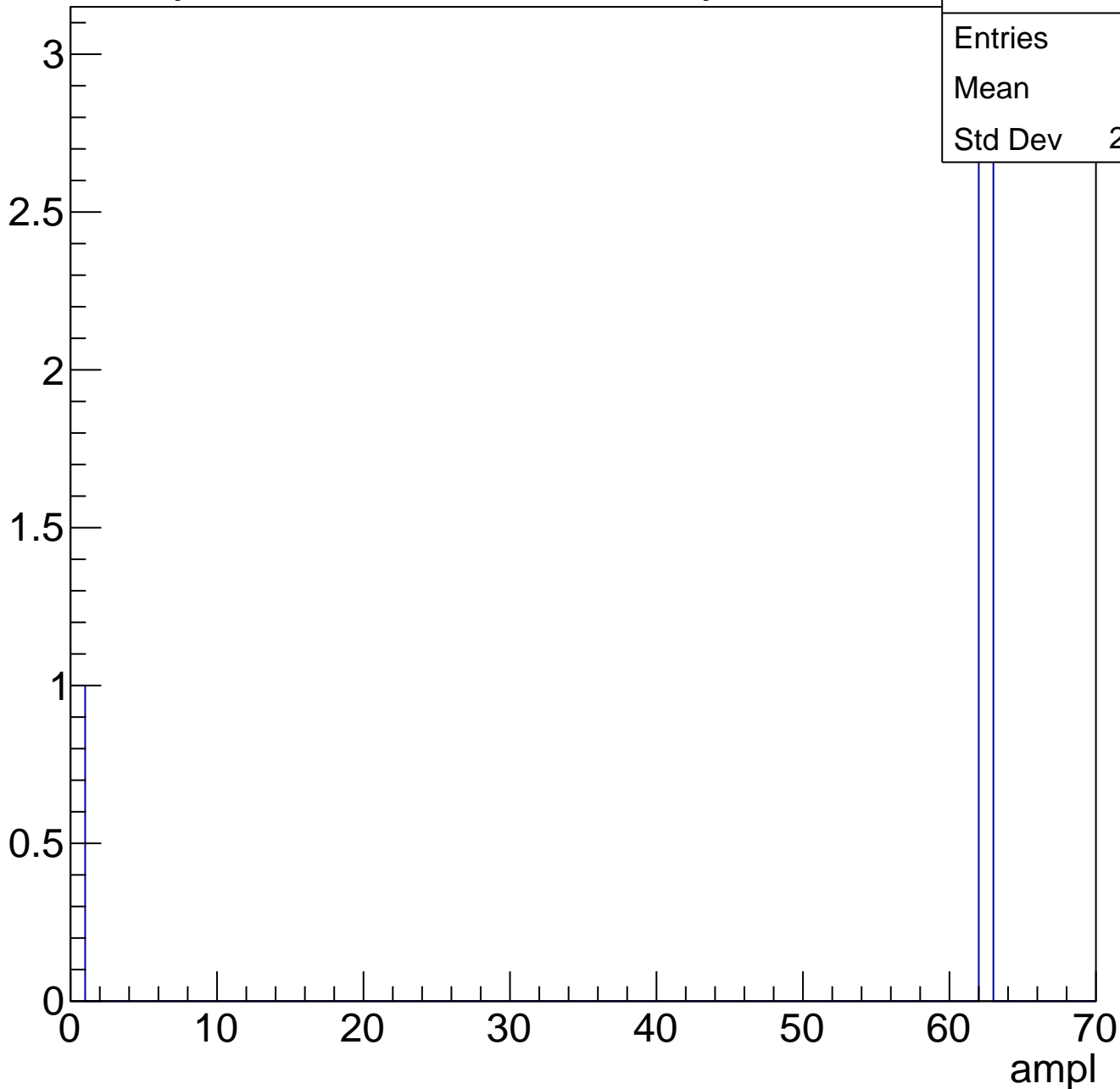
Entry



# B1L003S, U11-ch71, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch71, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U11-ch72, adc0

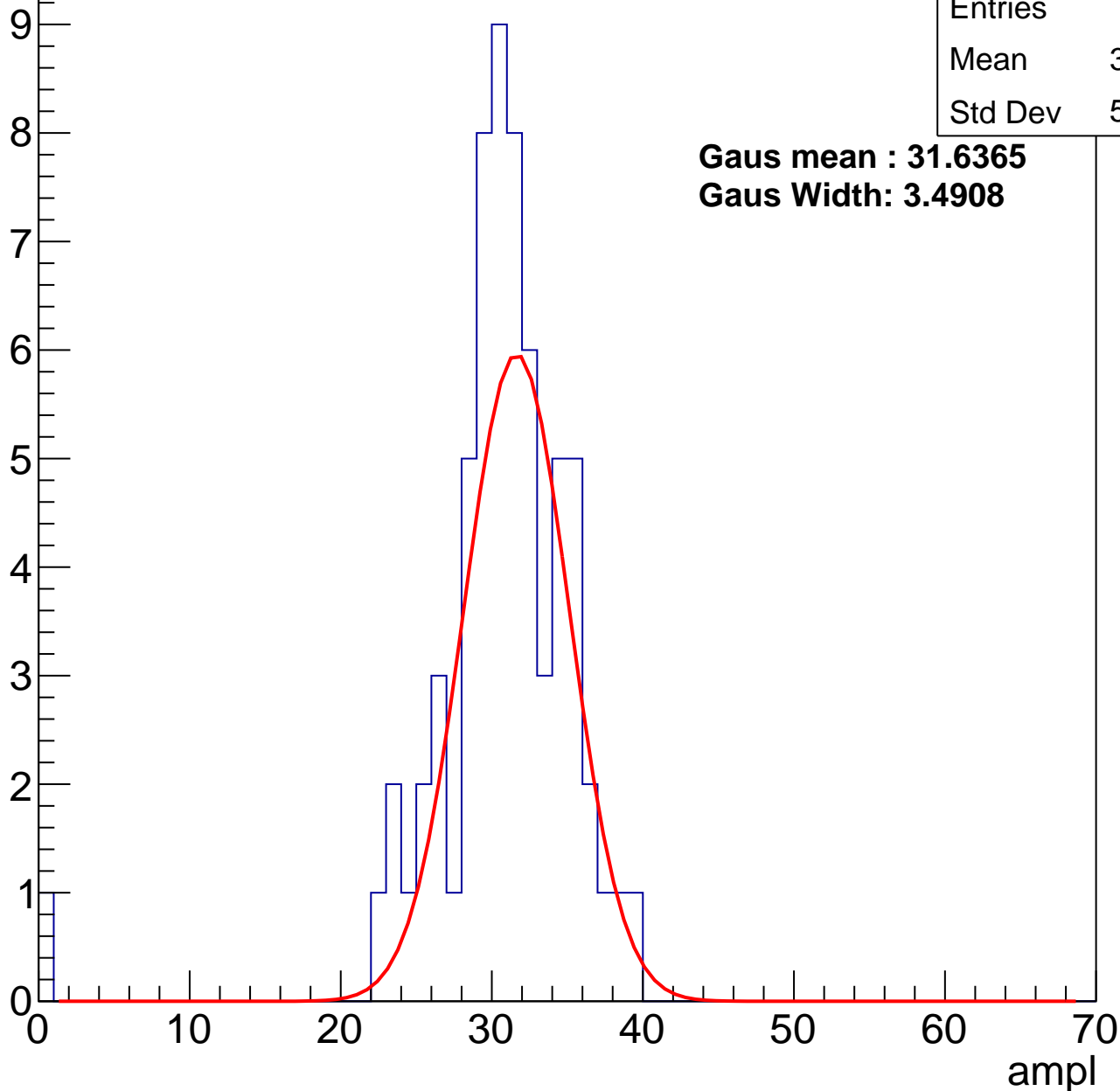
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	30.14
Std Dev	5.206

**Gaus mean : 31.6365**

**Gaus Width: 3.4908**



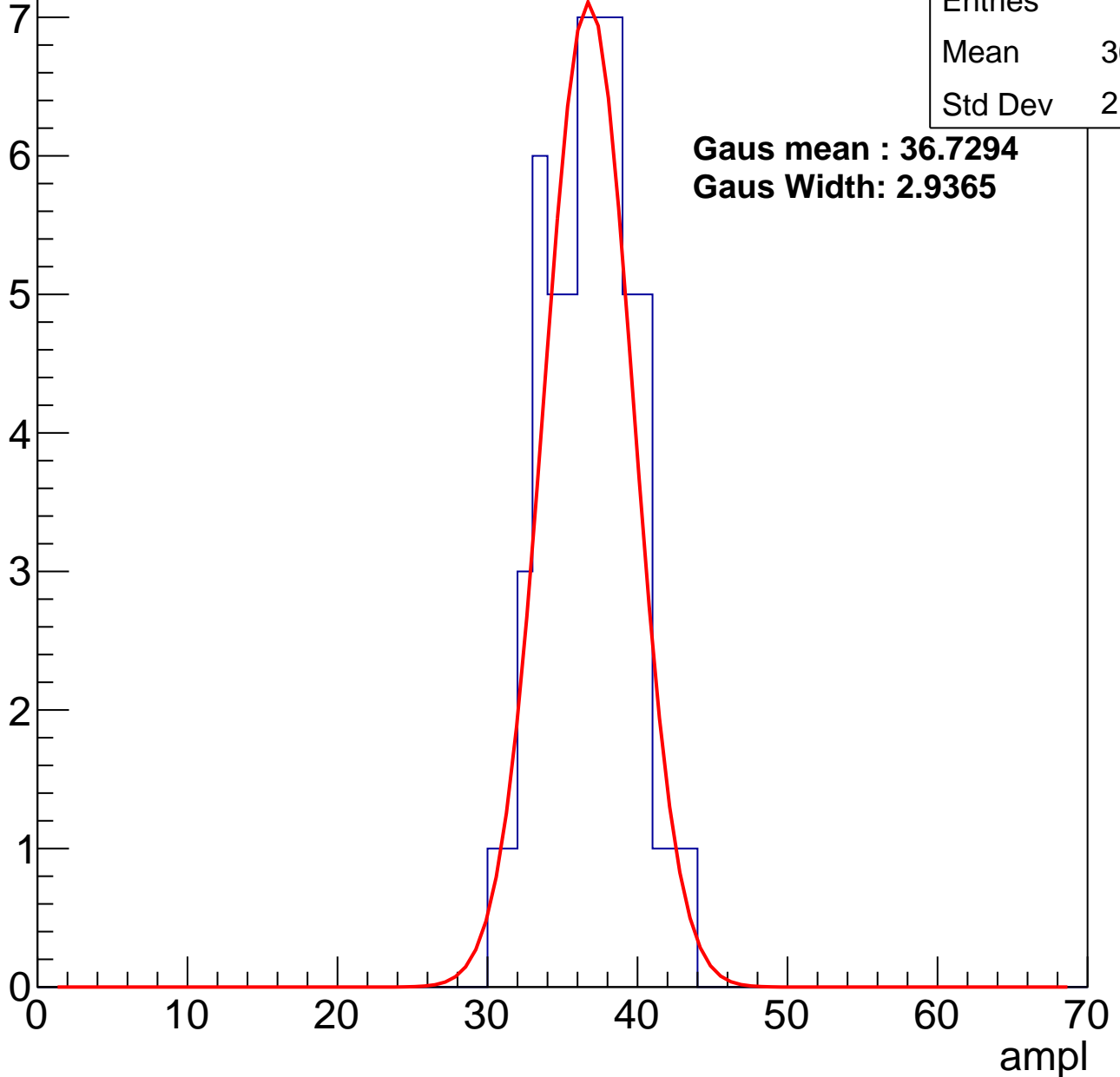
# B1L003S, U11-ch72, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	36.33
Std Dev	2.867

**Gaus mean : 36.7294**  
**Gaus Width: 2.9365**



# B1L003S, U11-ch72, adc2

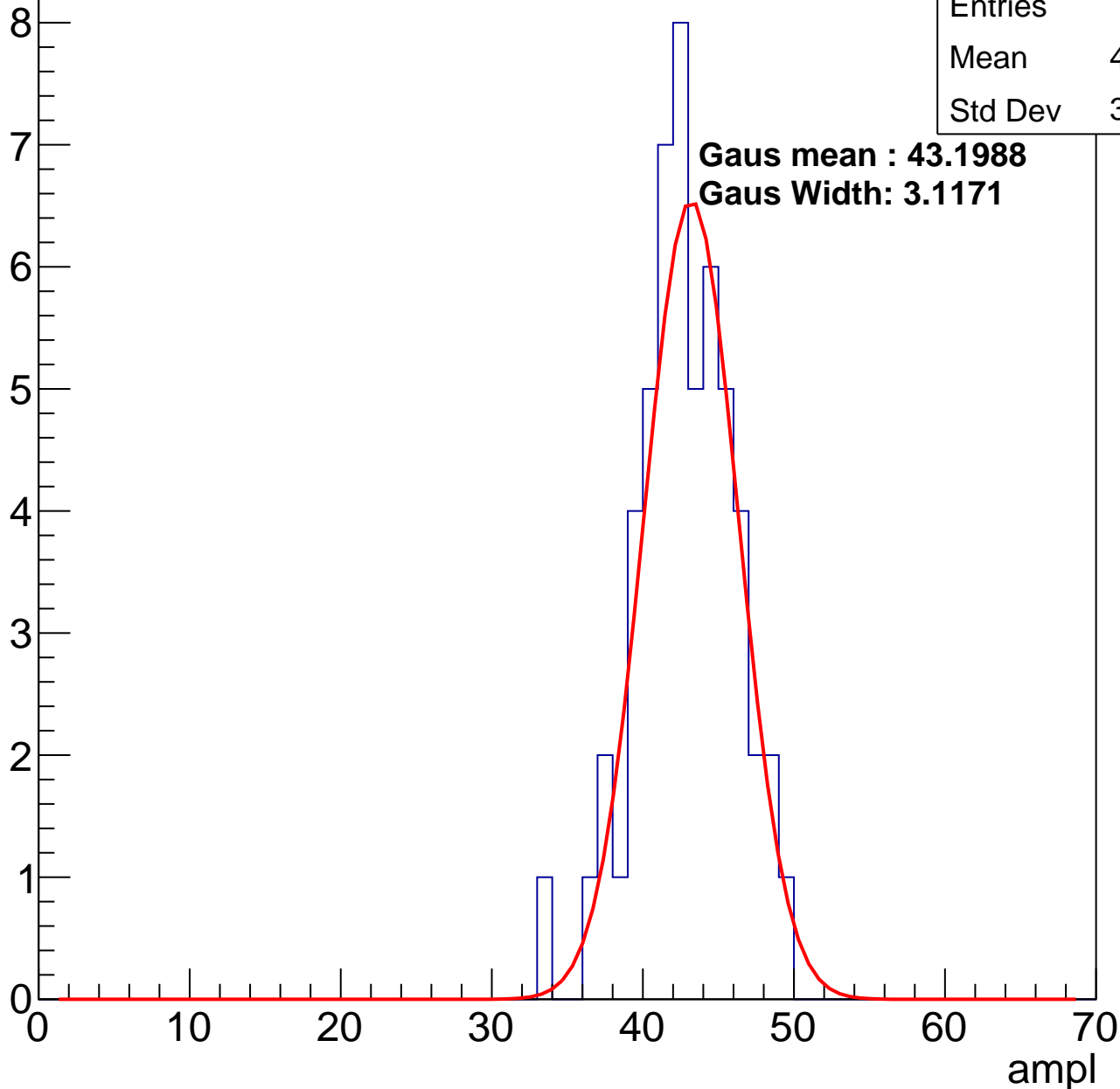
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	54
Mean	42.35
Std Dev	3.187

**Gaus mean : 43.1988**

**Gaus Width: 3.1171**

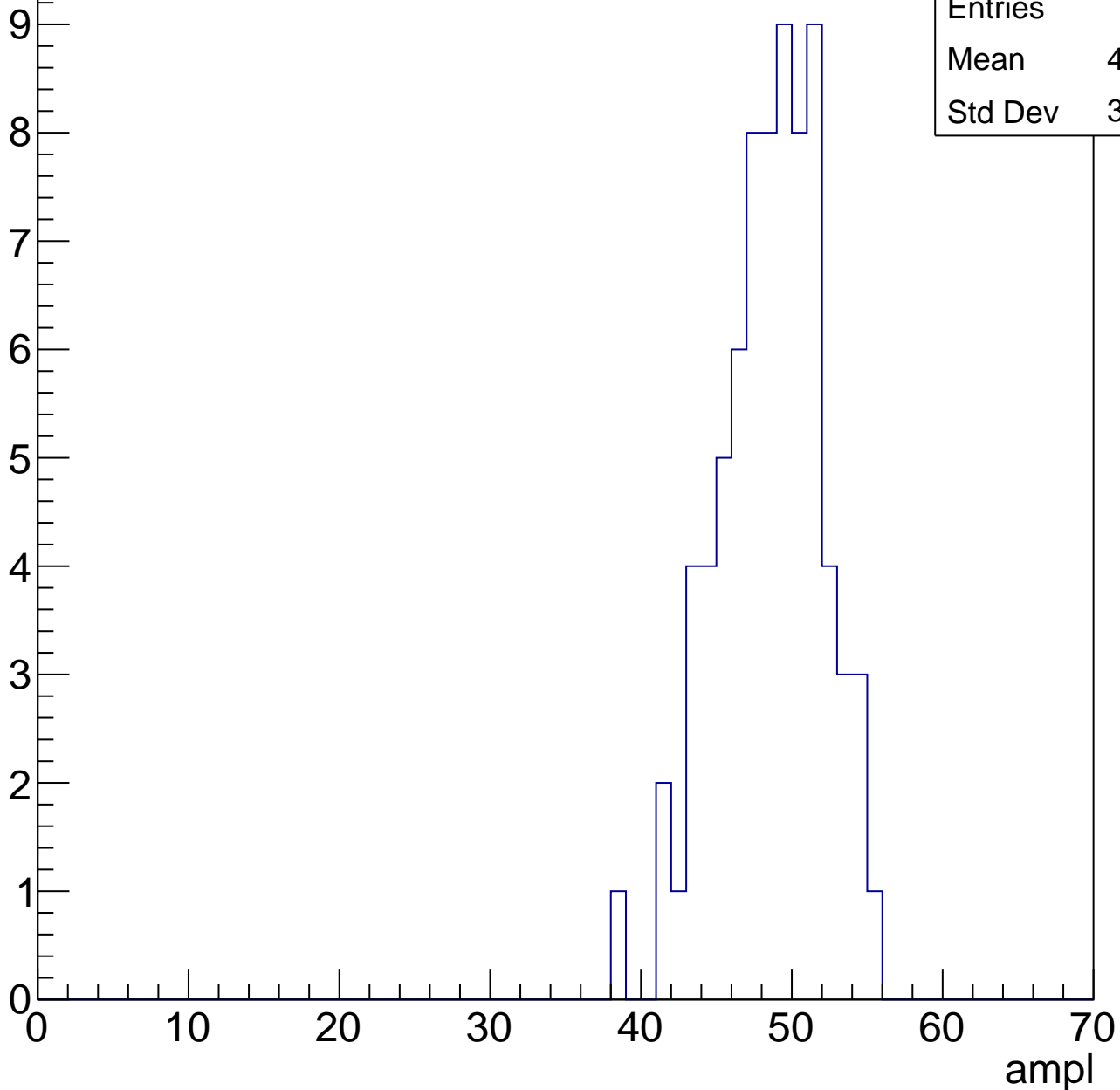


# B1L003S, U11-ch72, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

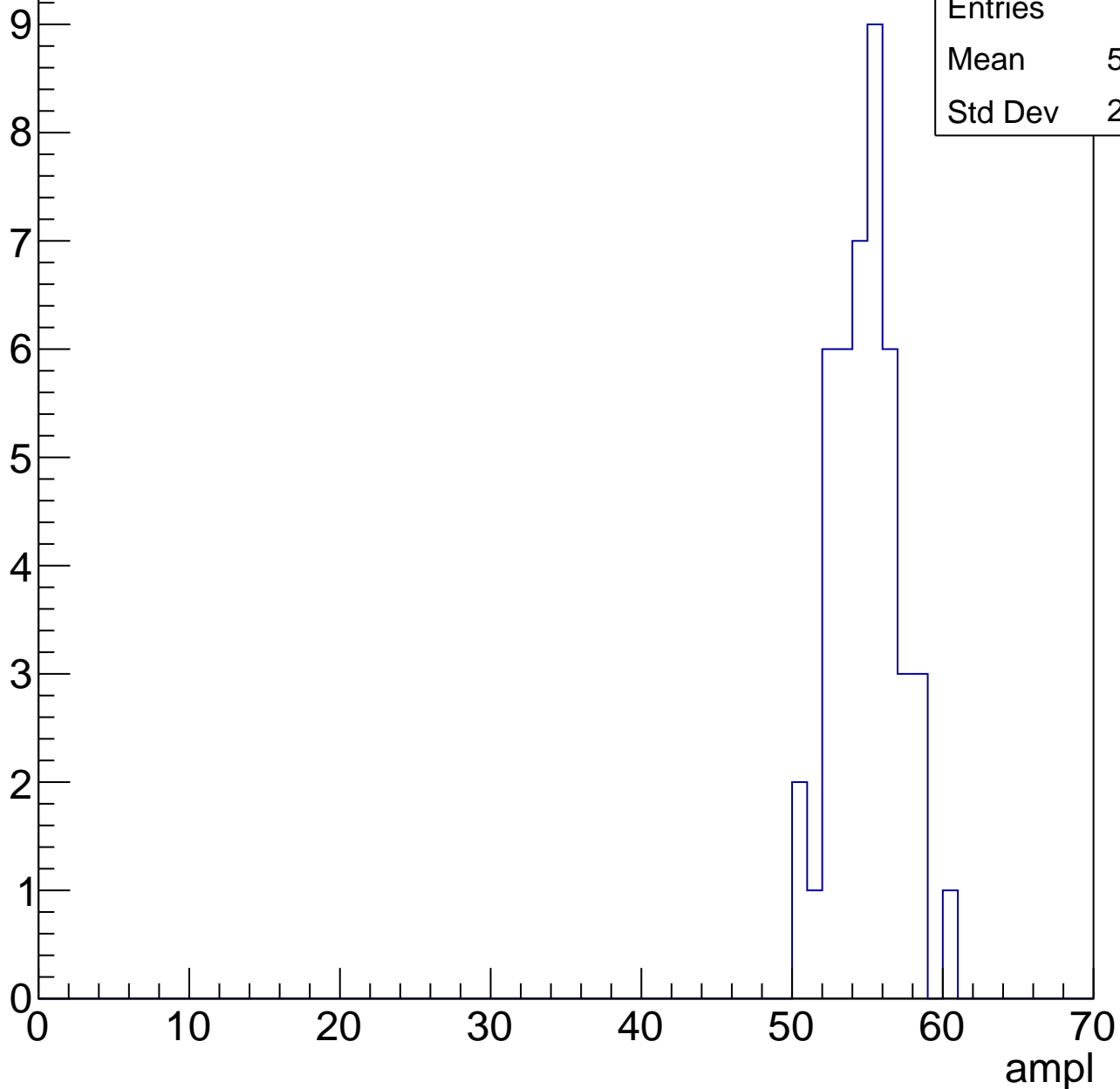
Entries	76
Mean	48.09
Std Dev	3.427



# B1L003S, U11-ch72, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

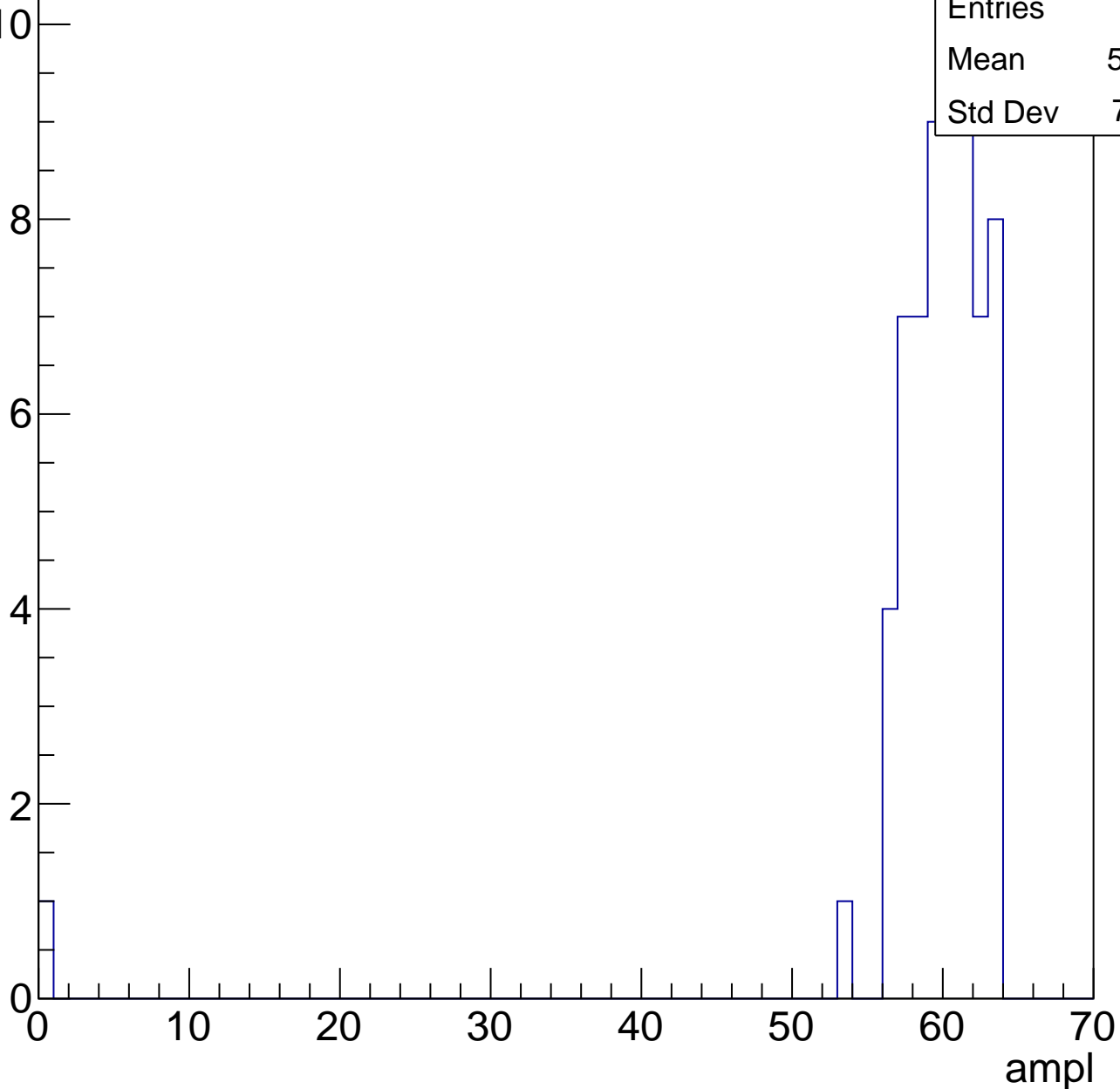


# B1L003S, U11-ch72, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

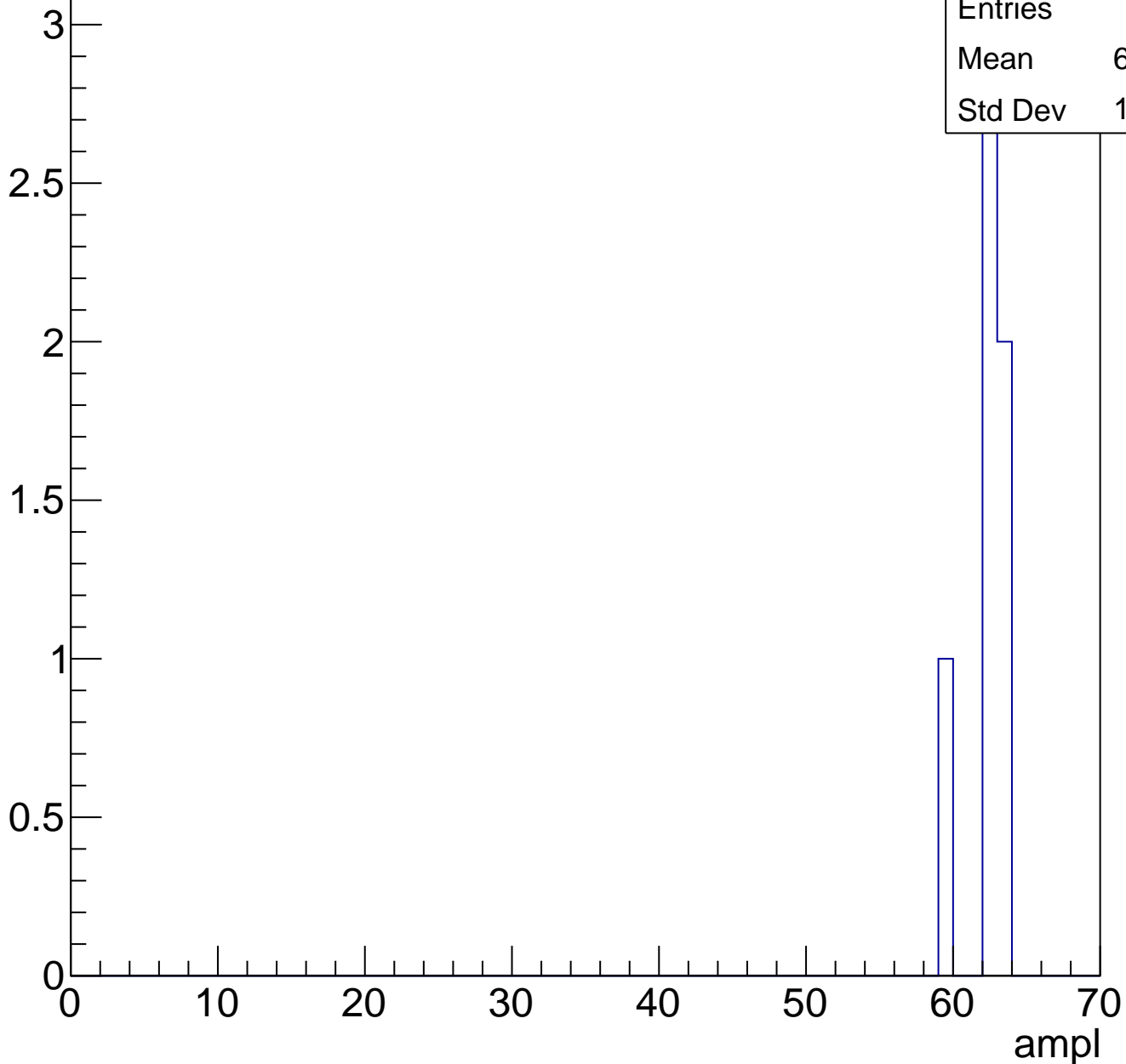
Entries	63
Mean	58.75
Std Dev	7.791



# B1L003S, U11-ch72, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch72, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U11-ch73, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	82
Mean	31.32
Std Dev	3.642

**Gaus mean : 31.9815**

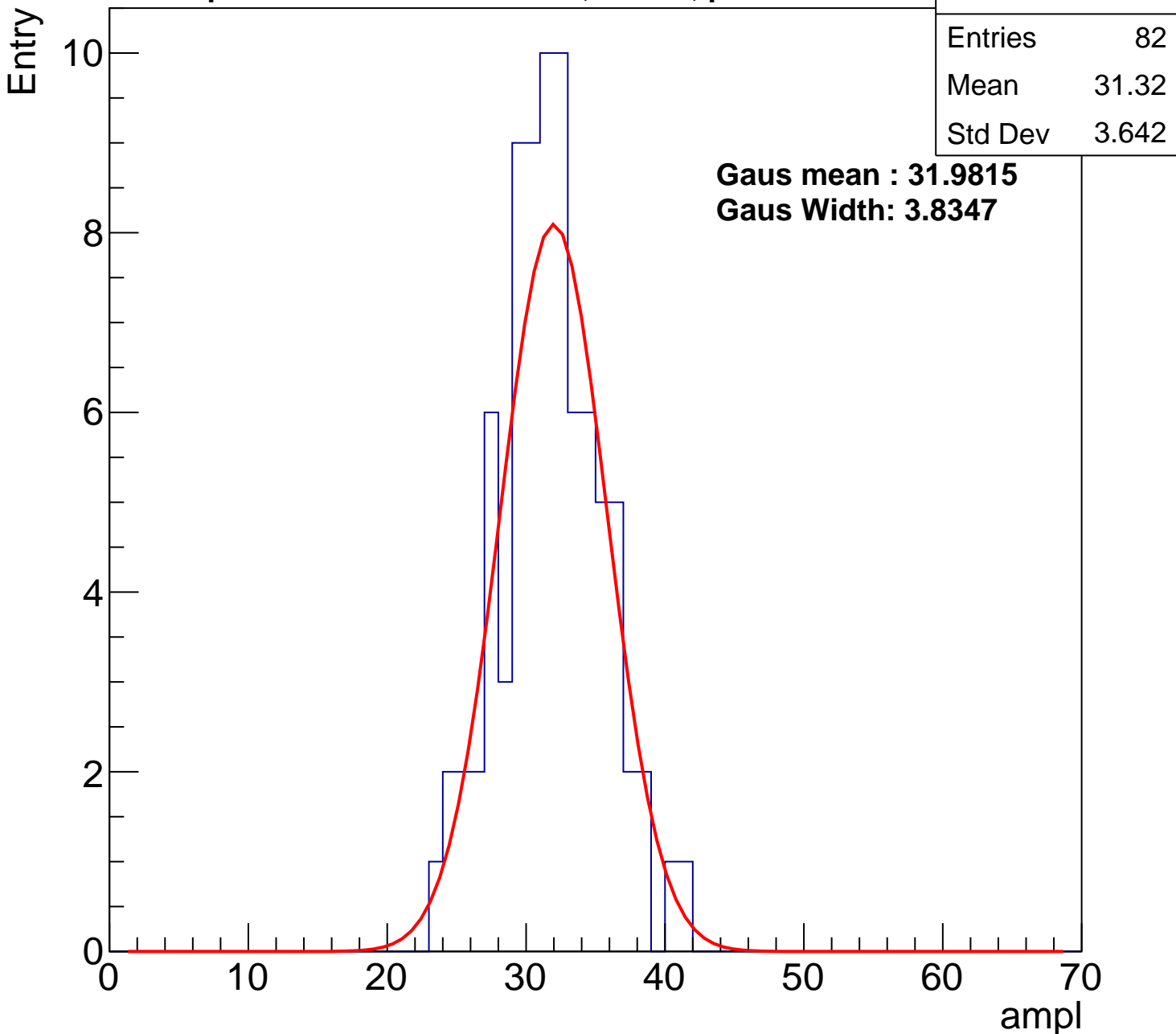
**Gaus Width: 3.8347**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L003S, U11-ch73, adc1

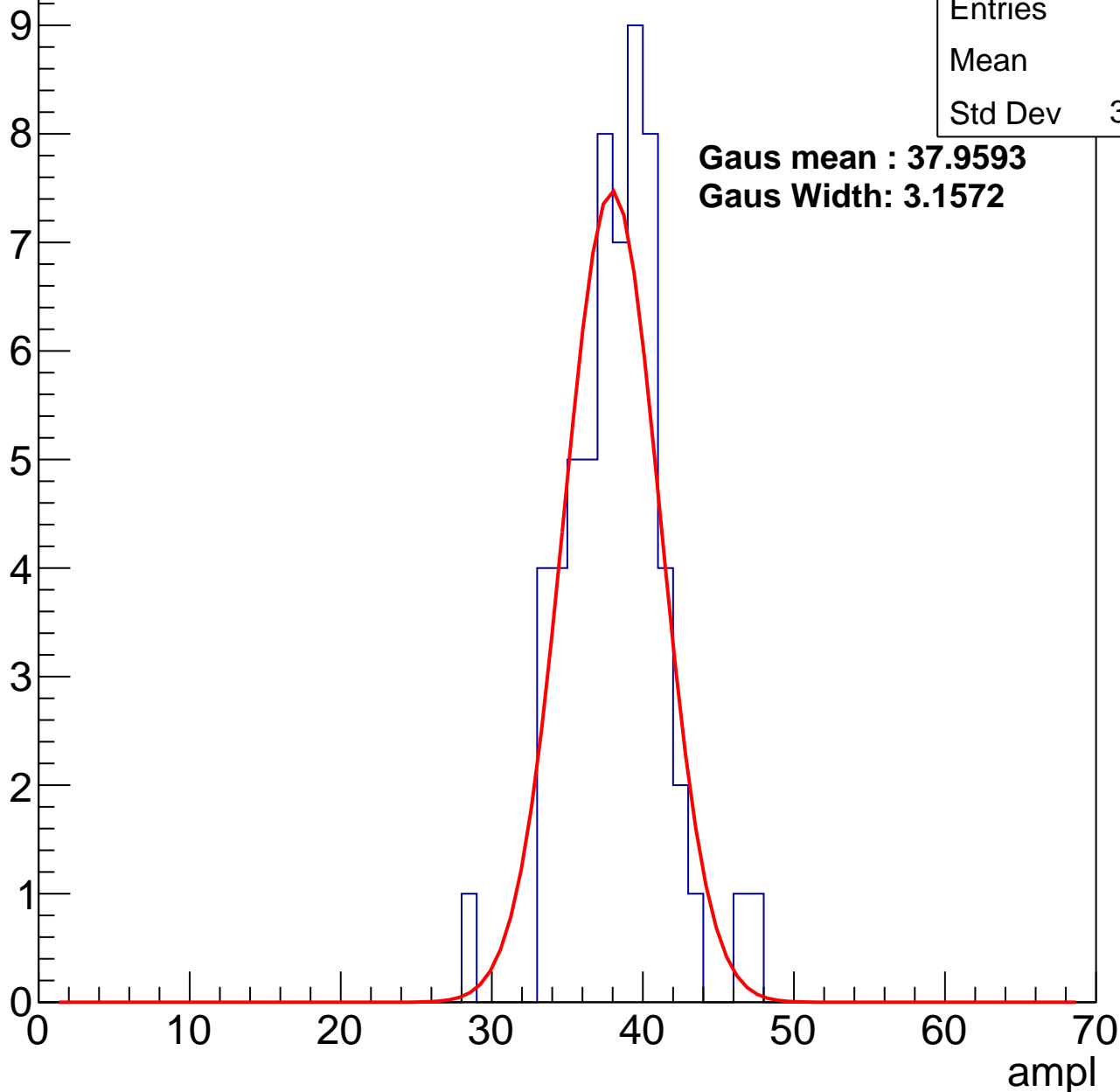
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	37.8
Std Dev	3.198

**Gaus mean : 37.9593**

**Gaus Width: 3.1572**



# B1L003S, U11-ch73, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	44.73
Std Dev	2.895

**Gaus mean : 44.9599**

**Gaus Width: 2.6534**

10

8

6

4

2

0

ampl

0

10

20

30

40

50

60

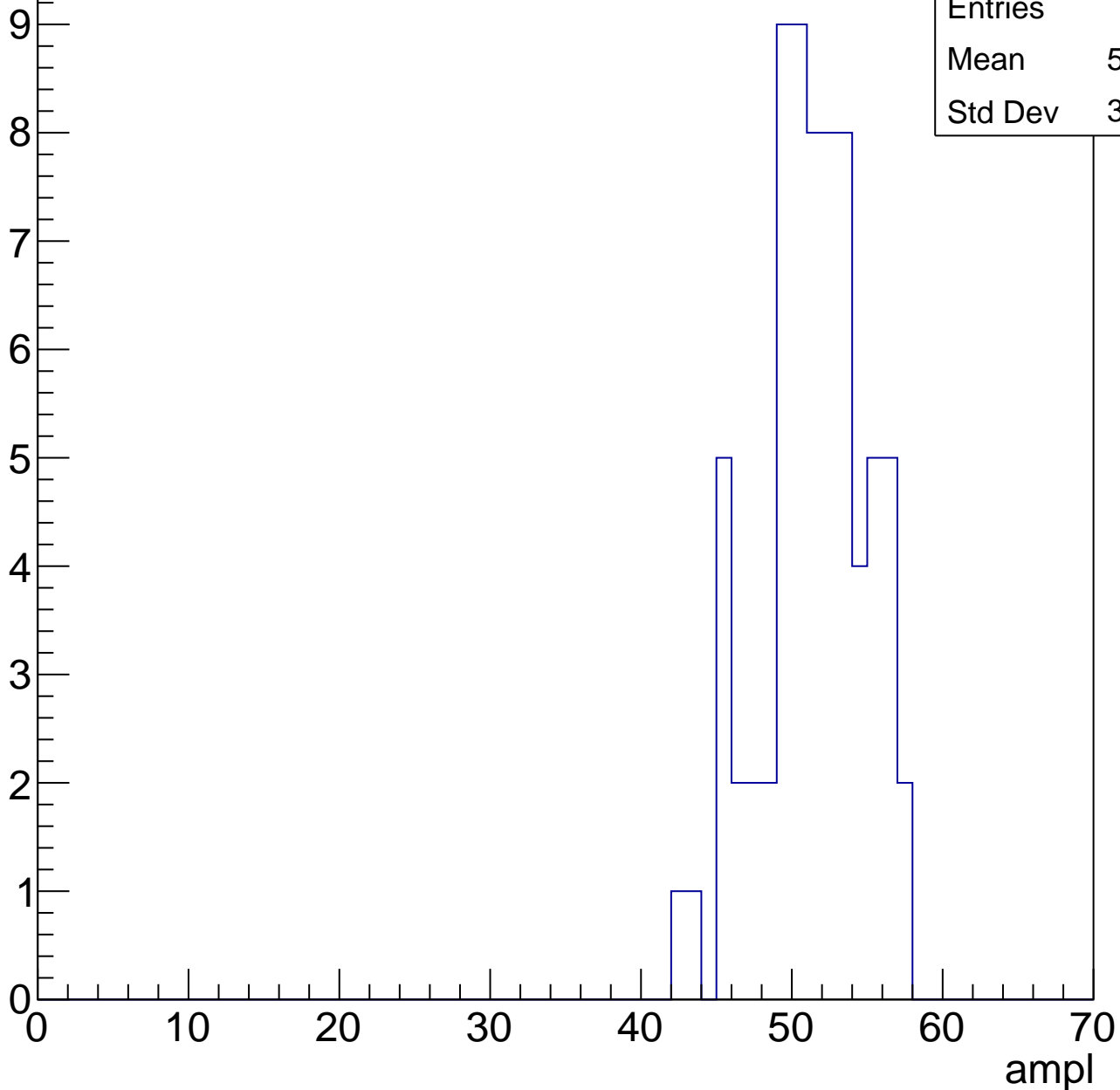
70

# B1L003S, U11-ch73, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	71
Mean	50.93
Std Dev	3.404

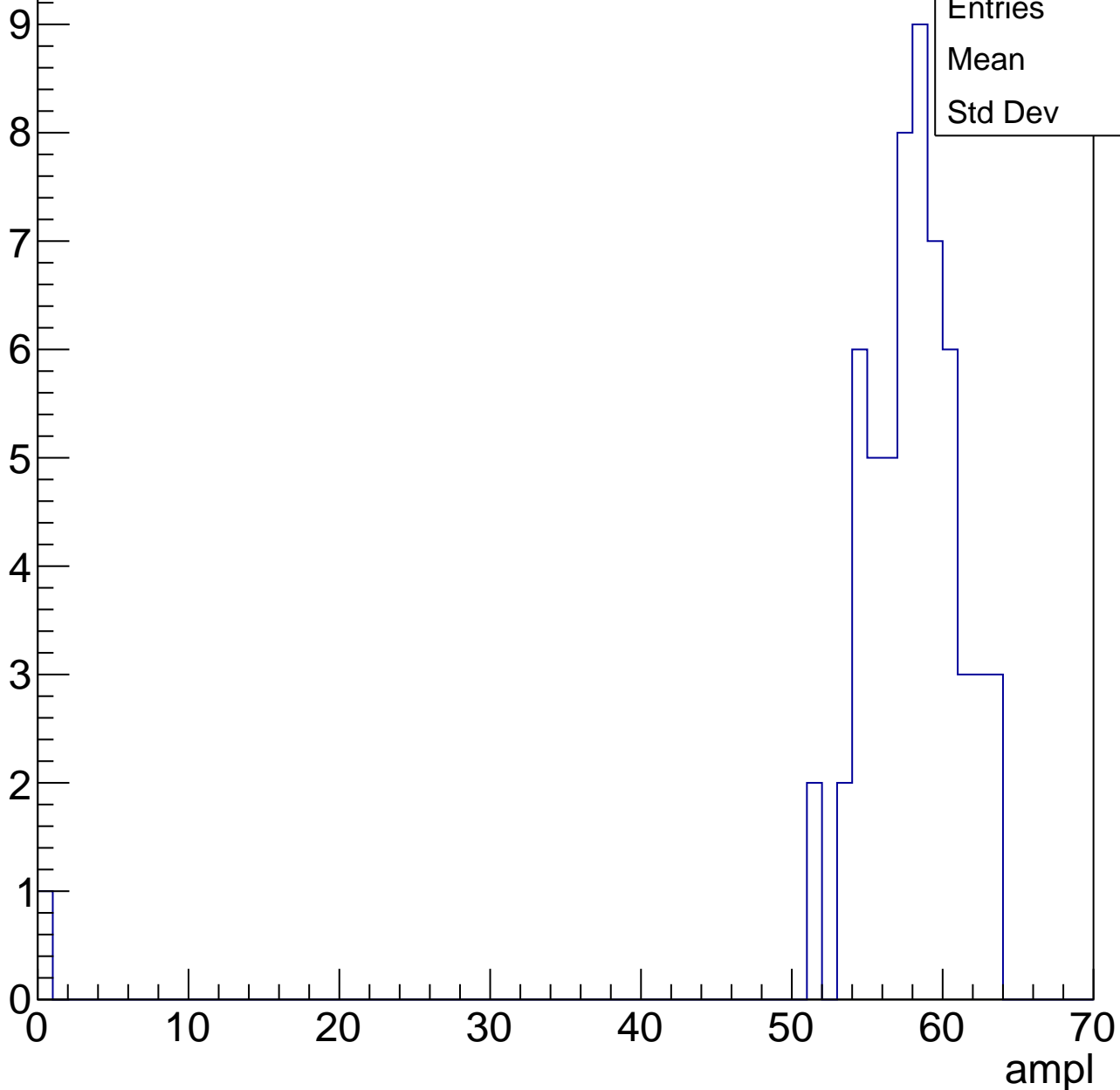


# B1L003S, U11-ch73, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

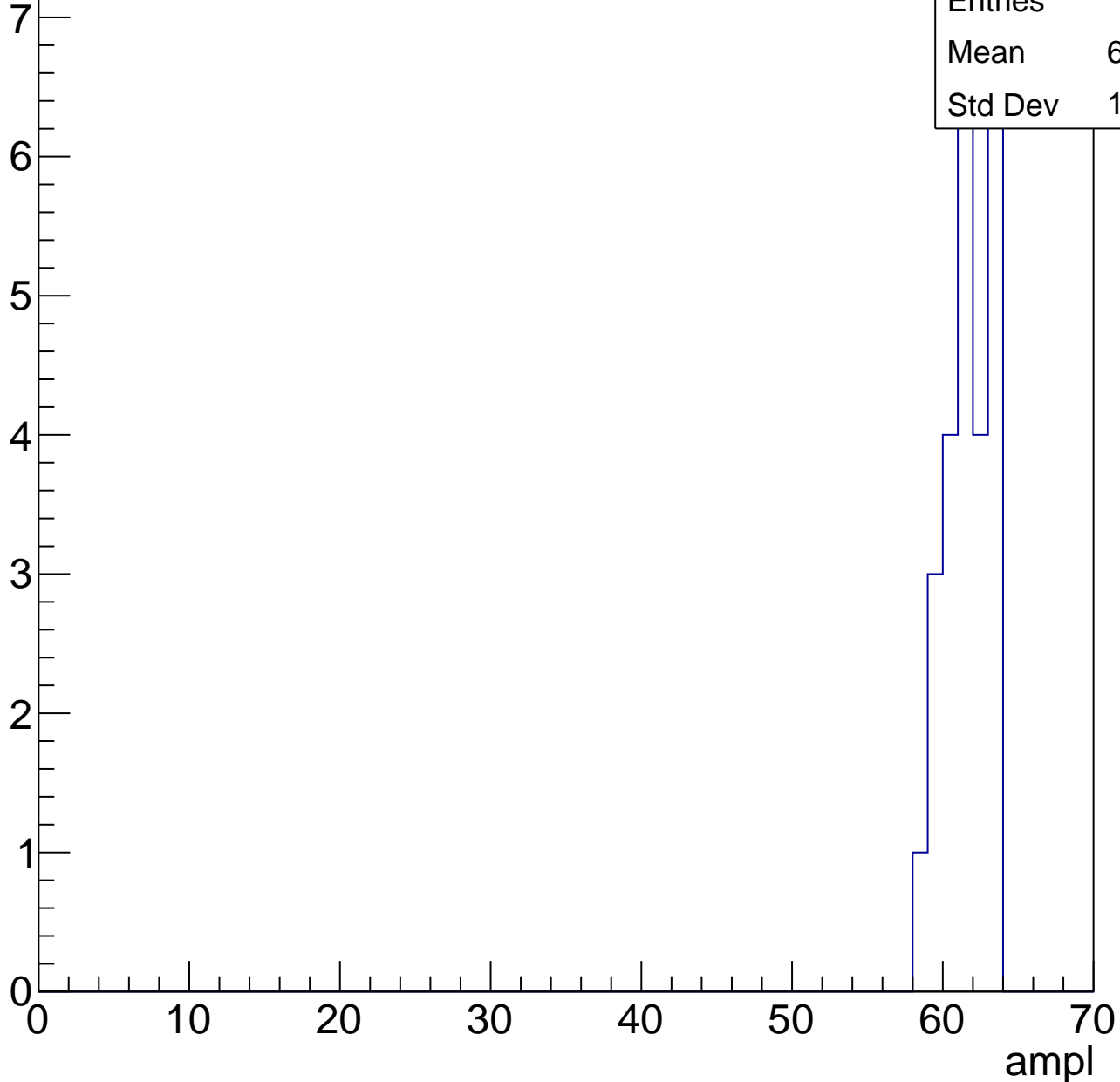
Entries	60
Mean	56.6
Std Dev	7.9



# B1L003S, U11-ch73, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	26
Mean	61.19
Std Dev	1.468

# B1L003S, U11-ch73, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch73, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U11-ch74, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	80
Mean	28.51
Std Dev	3.795

**Gaus mean : 28.9073**

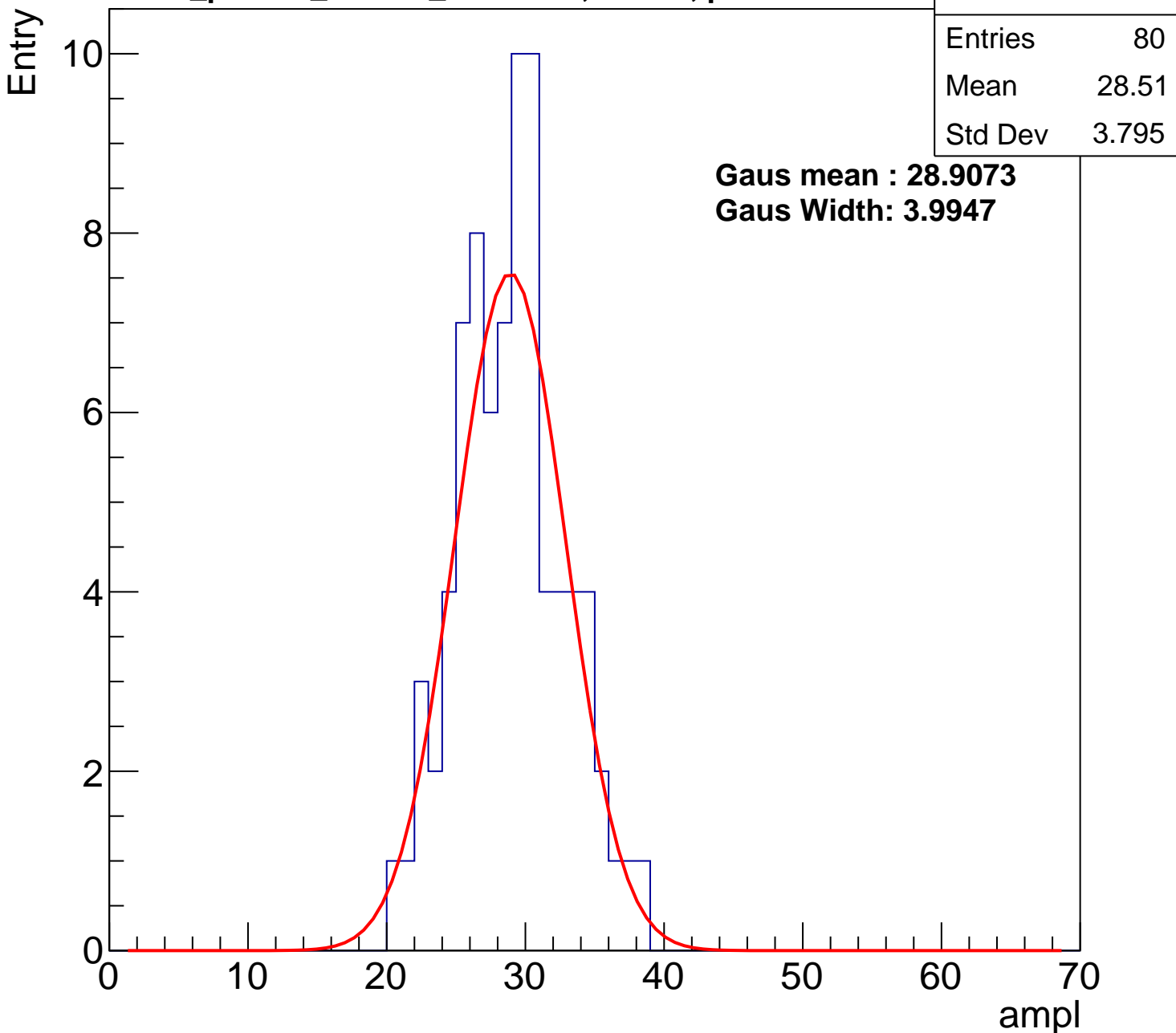
**Gaus Width: 3.9947**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U11-ch74, adc1

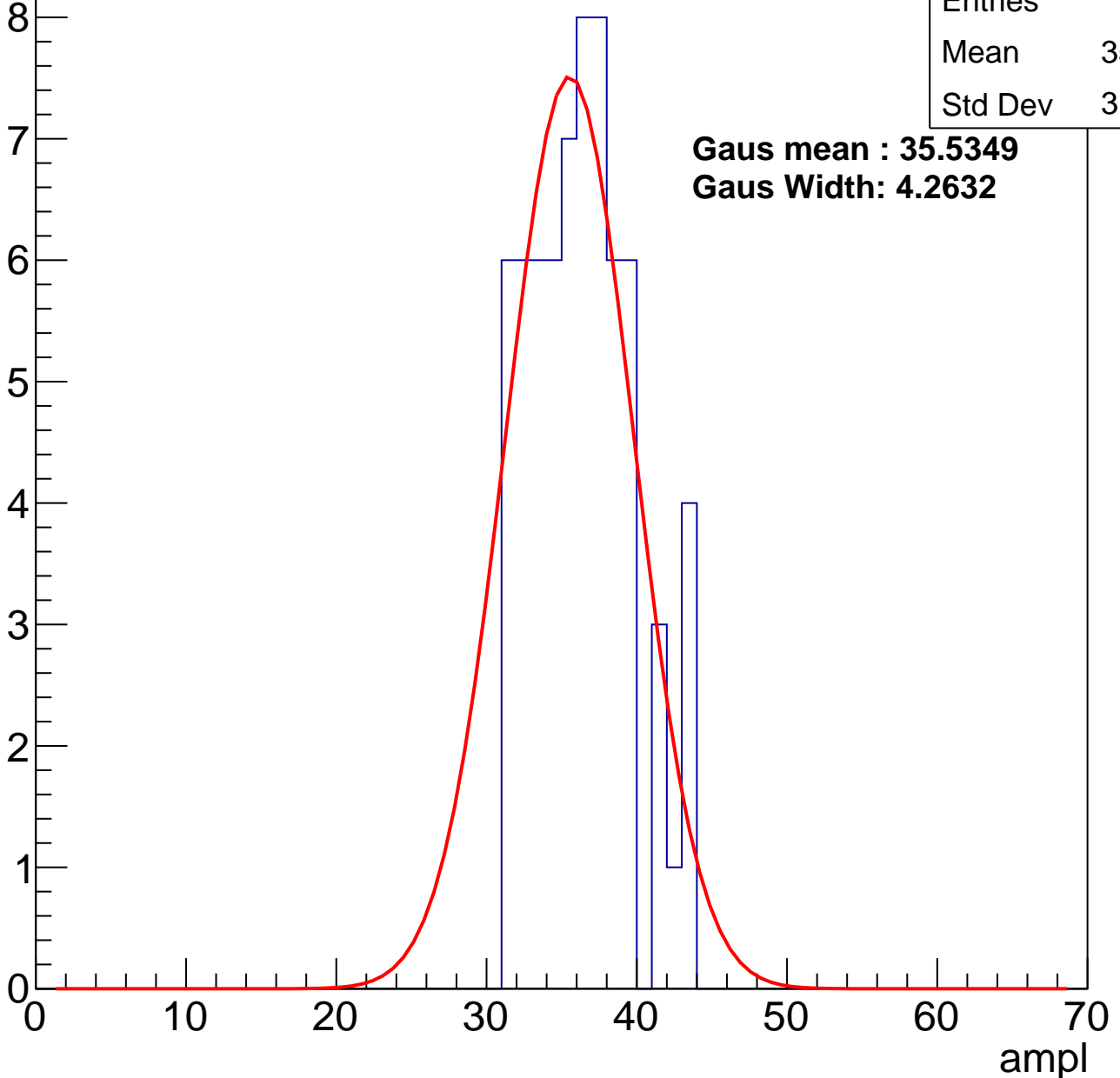
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	35.94
Std Dev	3.287

**Gaus mean : 35.5349**

**Gaus Width: 4.2632**



# B1L003S, U11-ch74, adc2

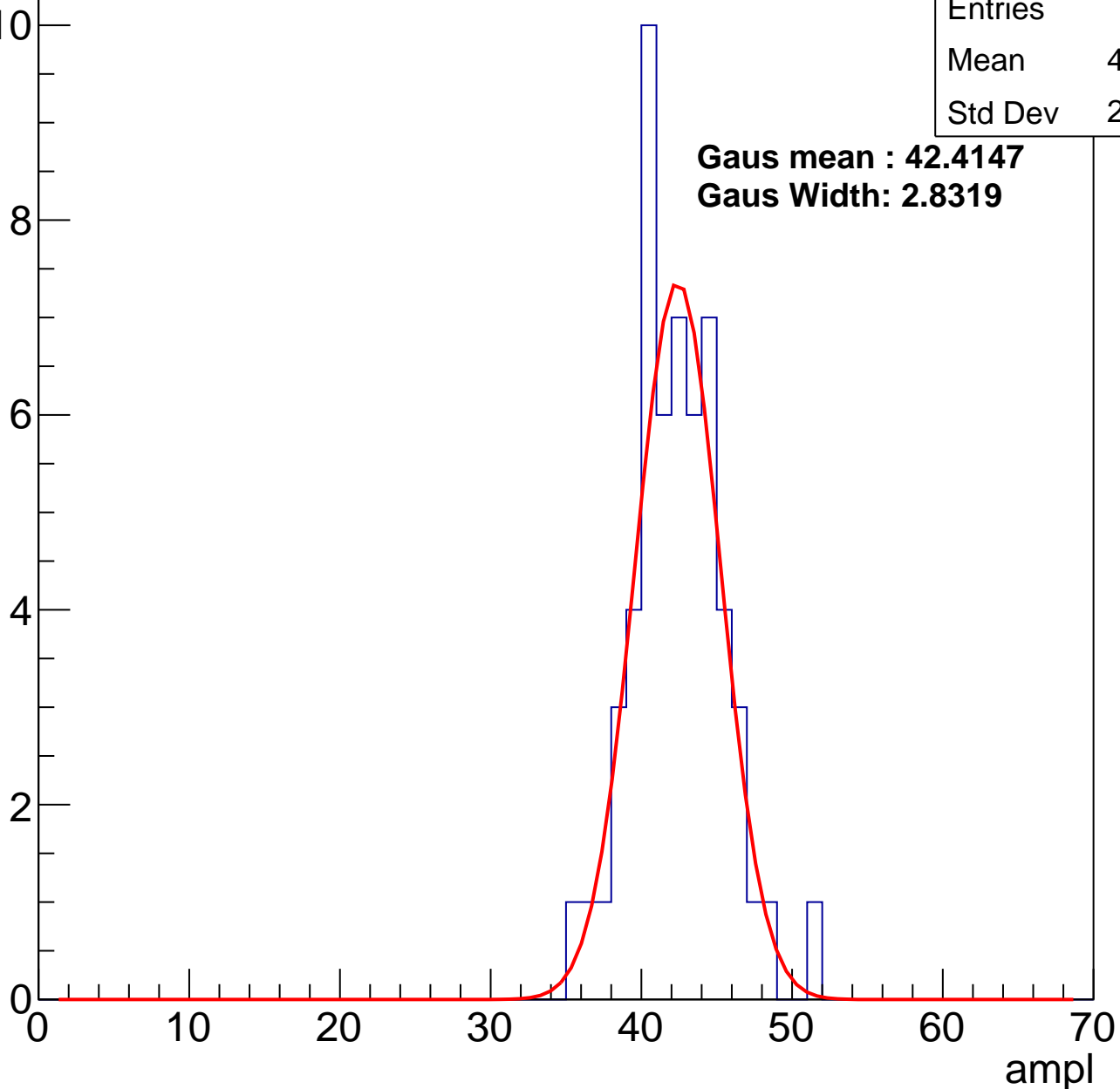
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	41.93
Std Dev	2.987

**Gaus mean : 42.4147**

**Gaus Width: 2.8319**

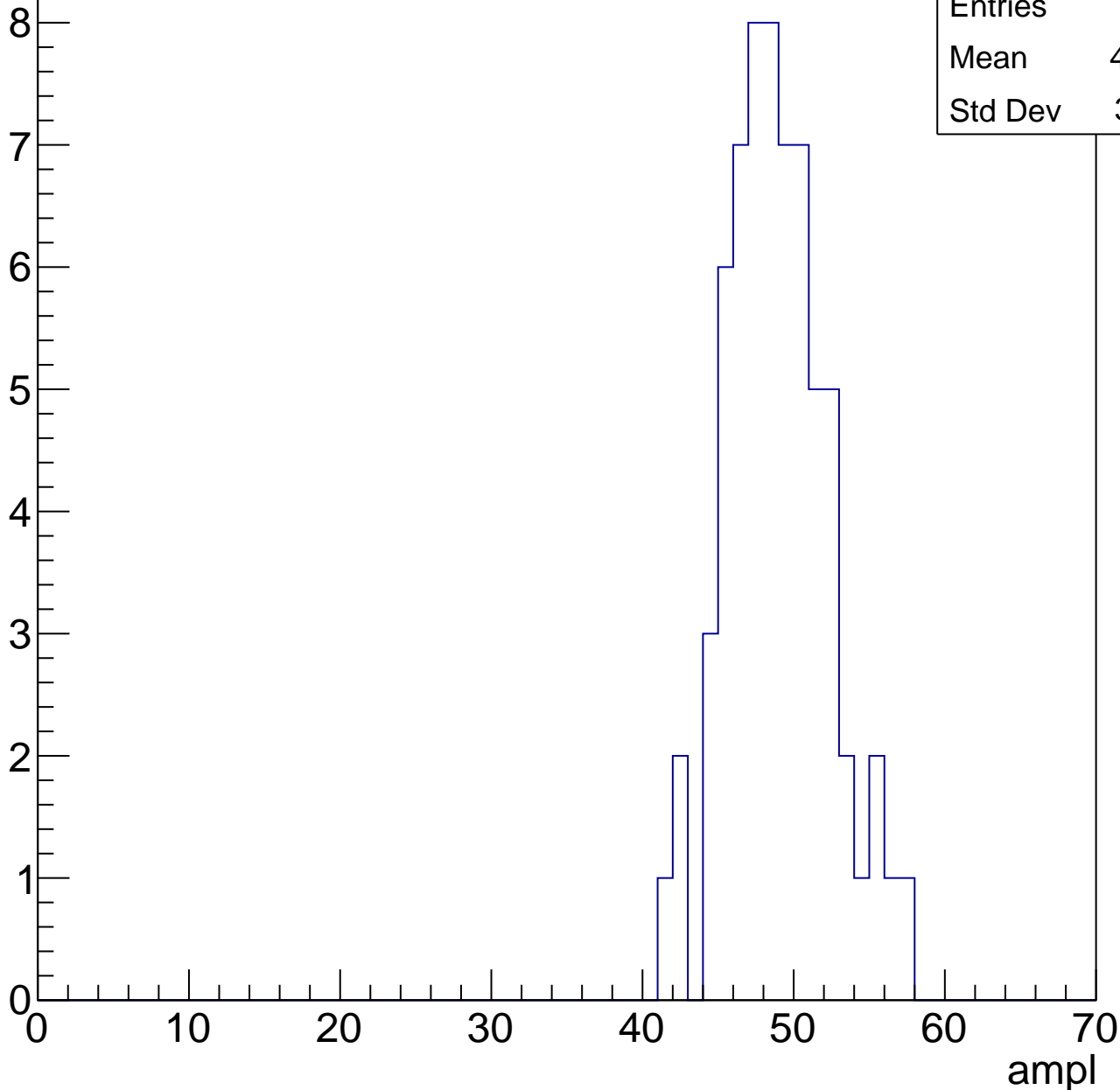


# B1L003S, U11-ch74, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	48.48
Std Dev	3.331

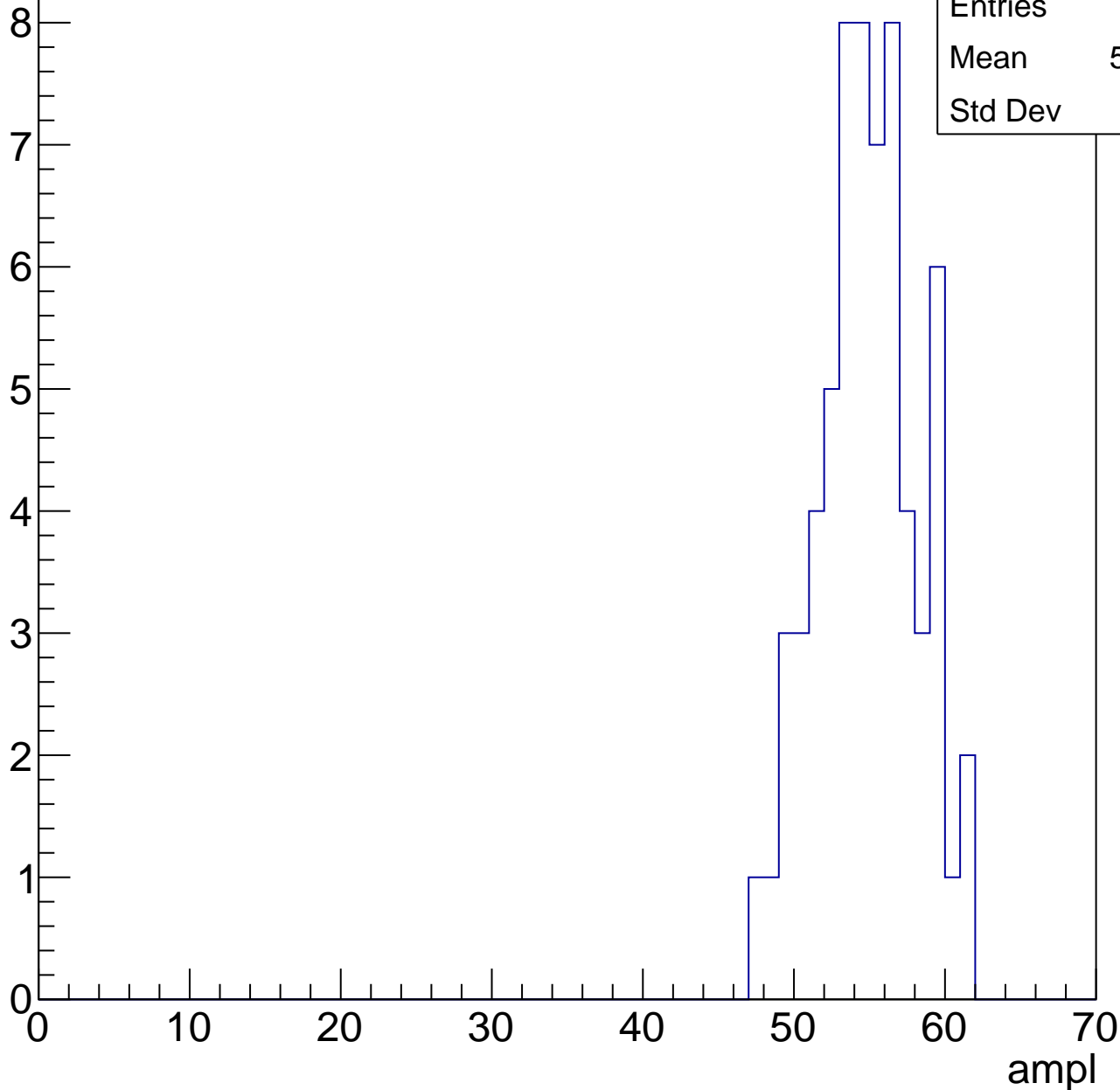


# B1L003S, U11-ch74, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

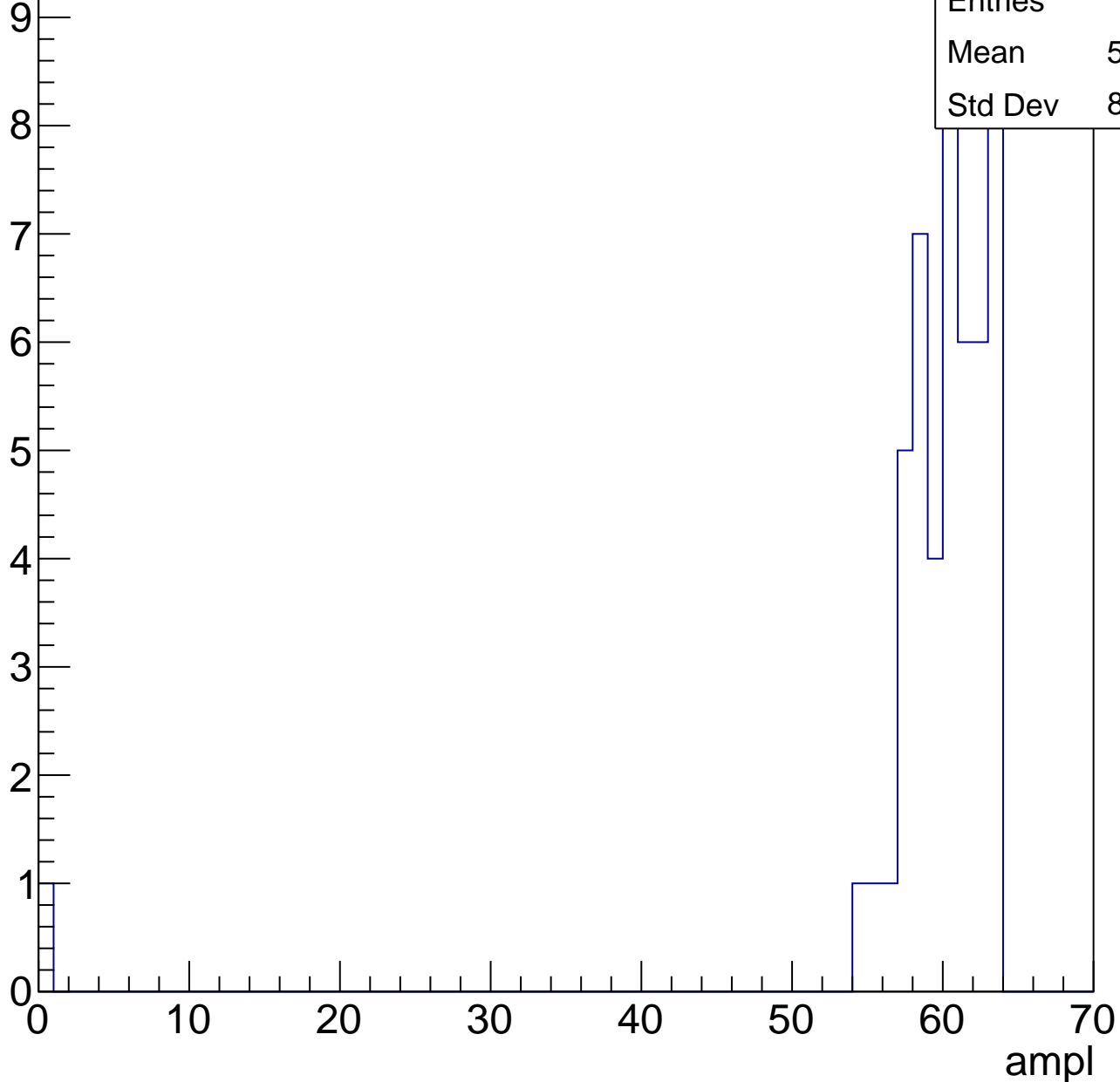
Entries	64
Mean	54.42
Std Dev	3.23



# B1L003S, U11-ch74, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

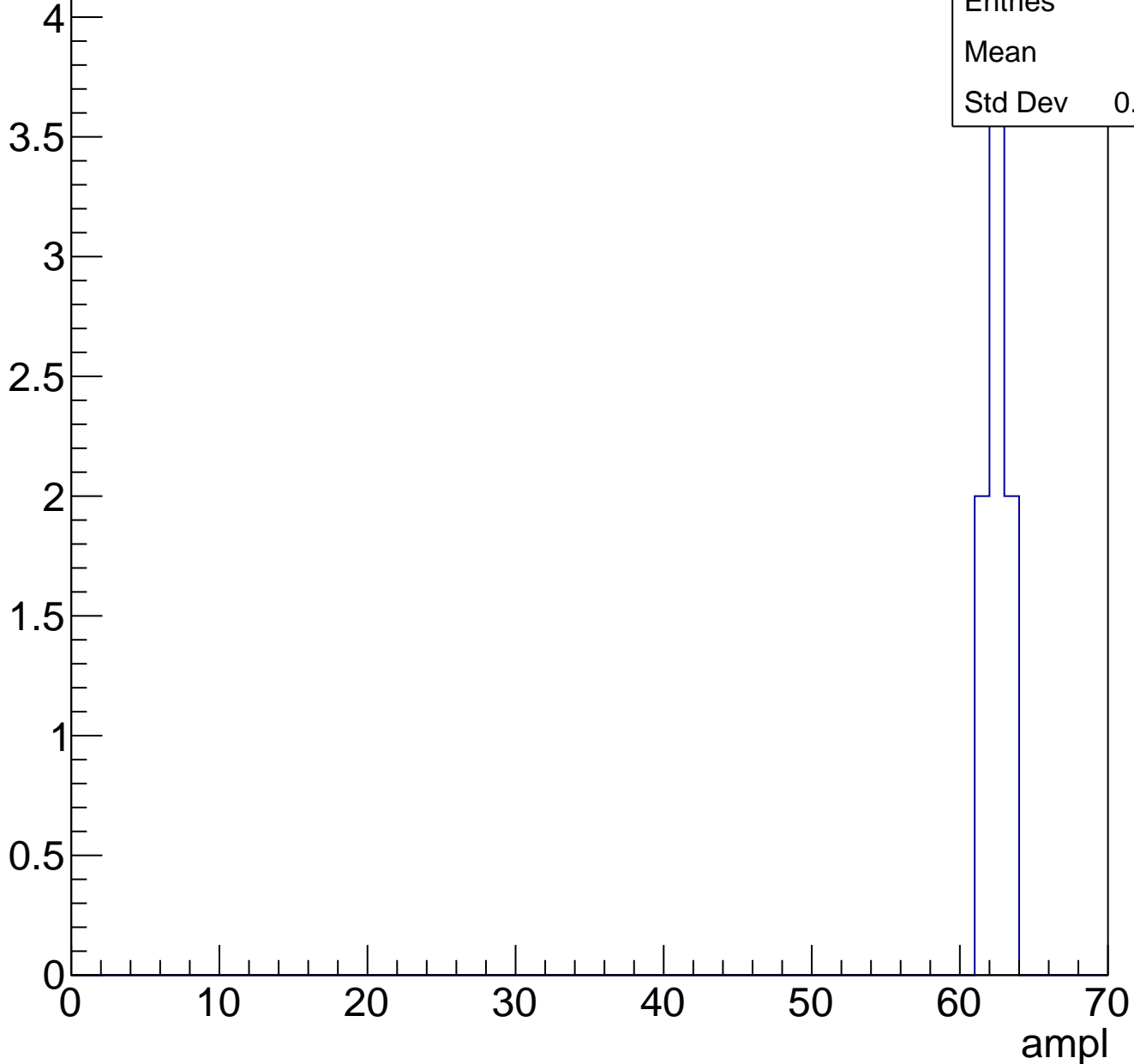
Entry



# B1L003S, U11-ch74, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

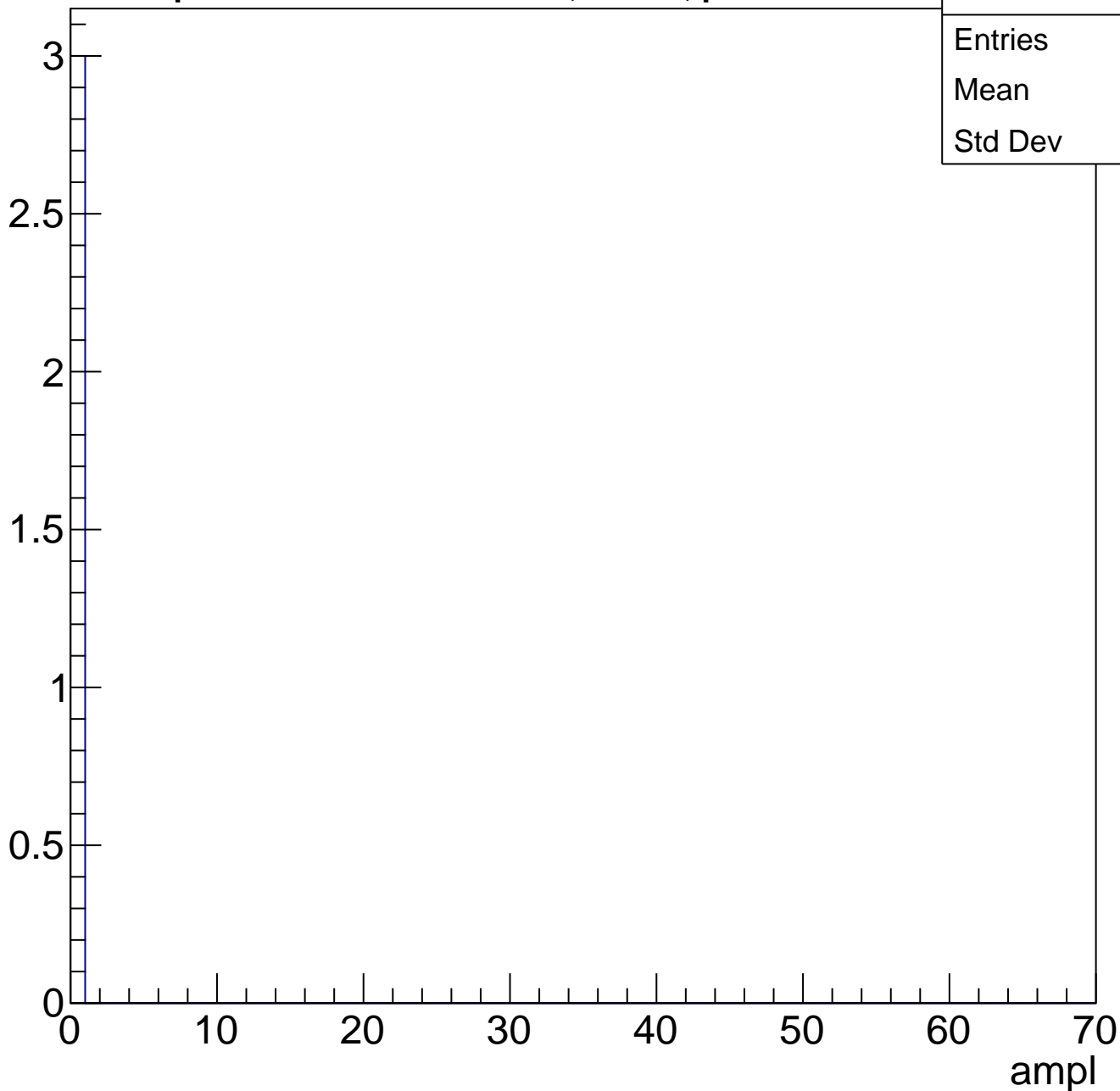




# B1L003S, U11-ch74, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L003S, U11-ch75, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	69
Mean	28.83
Std Dev	3.283

**Gaus mean : 29.4300**

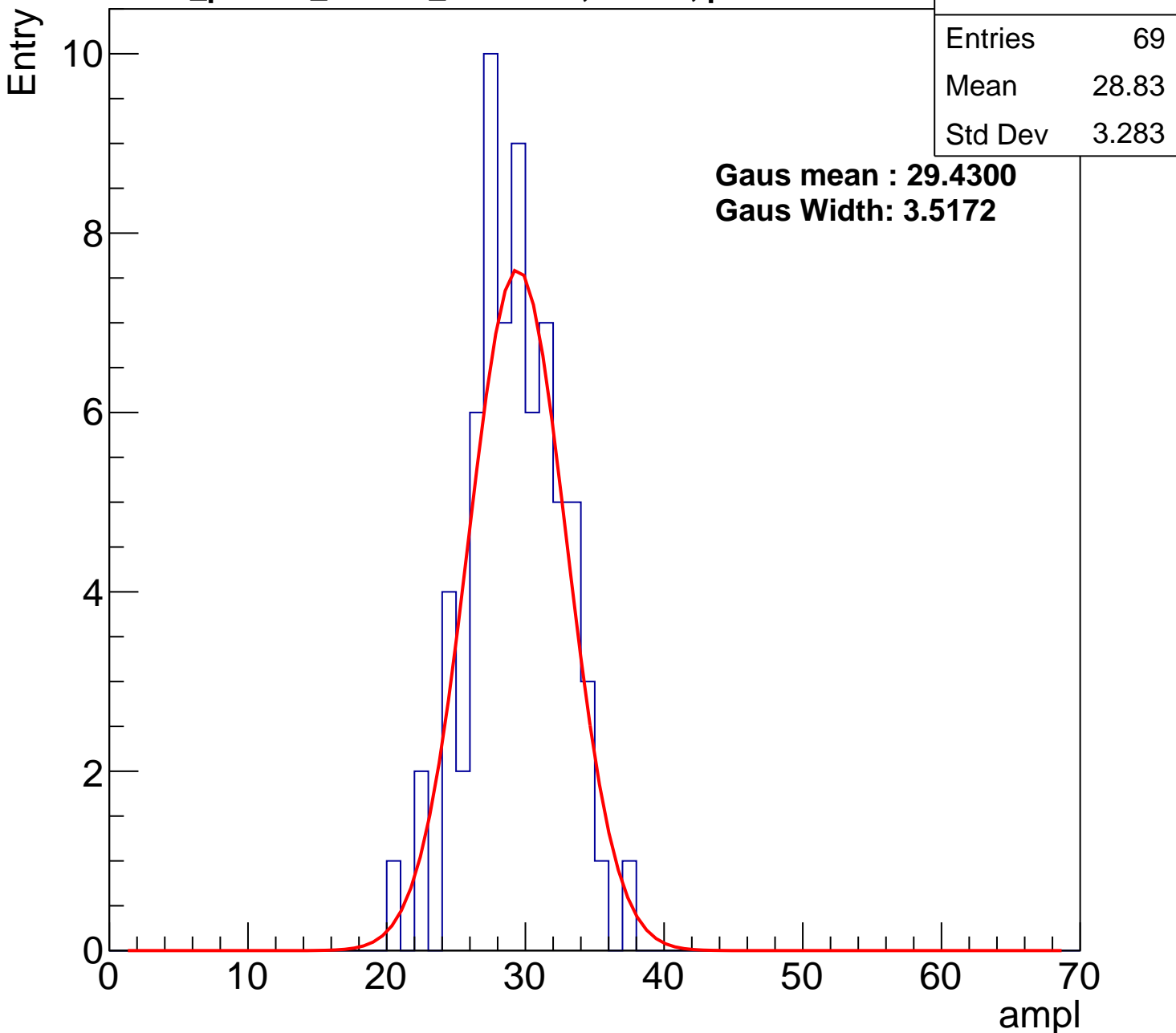
**Gaus Width: 3.5172**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U11-ch75, adc1

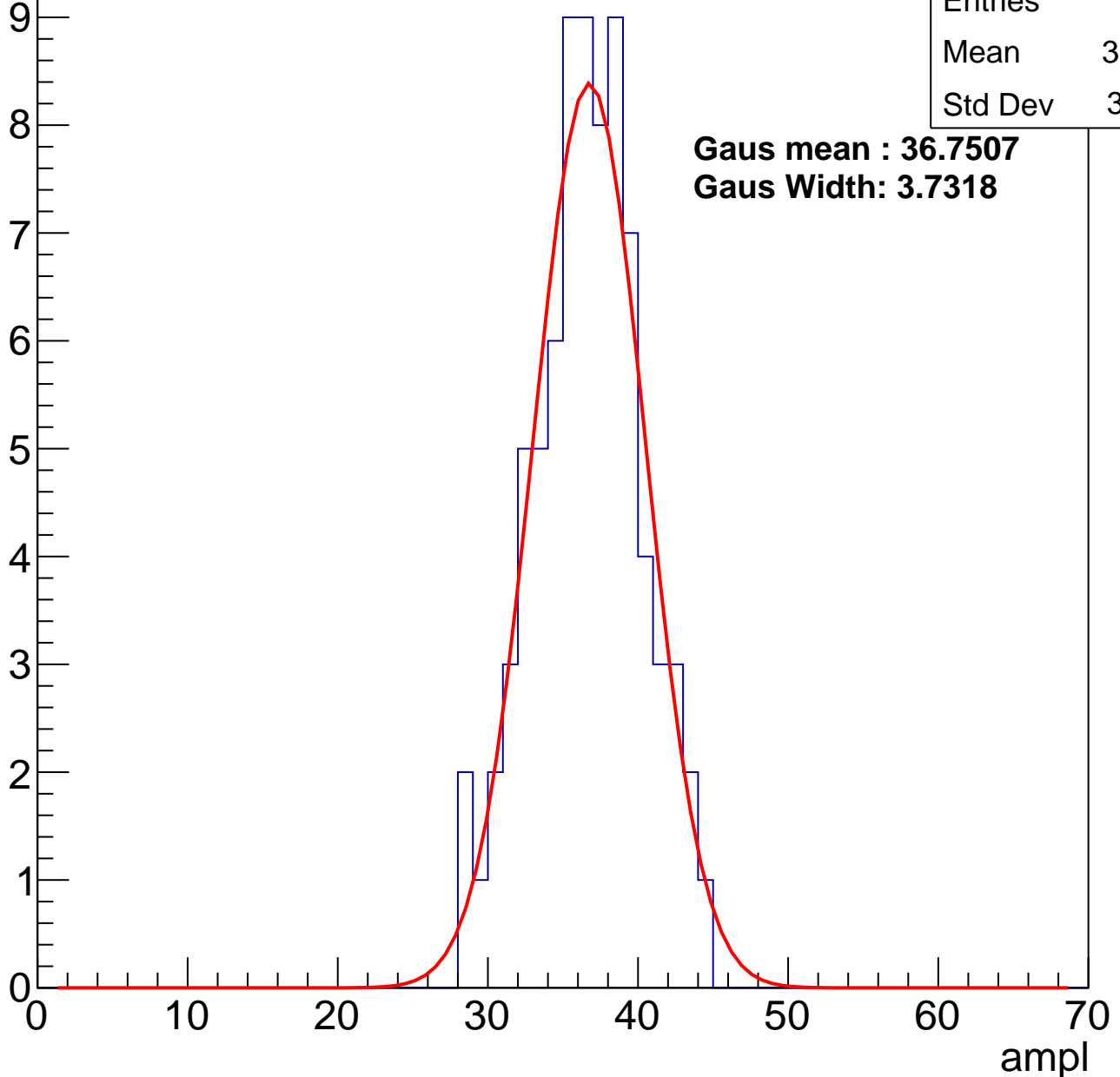
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	79
Mean	36.15
Std Dev	3.551

**Gaus mean : 36.7507**

**Gaus Width: 3.7318**



# B1L003S, U11-ch75, adc2

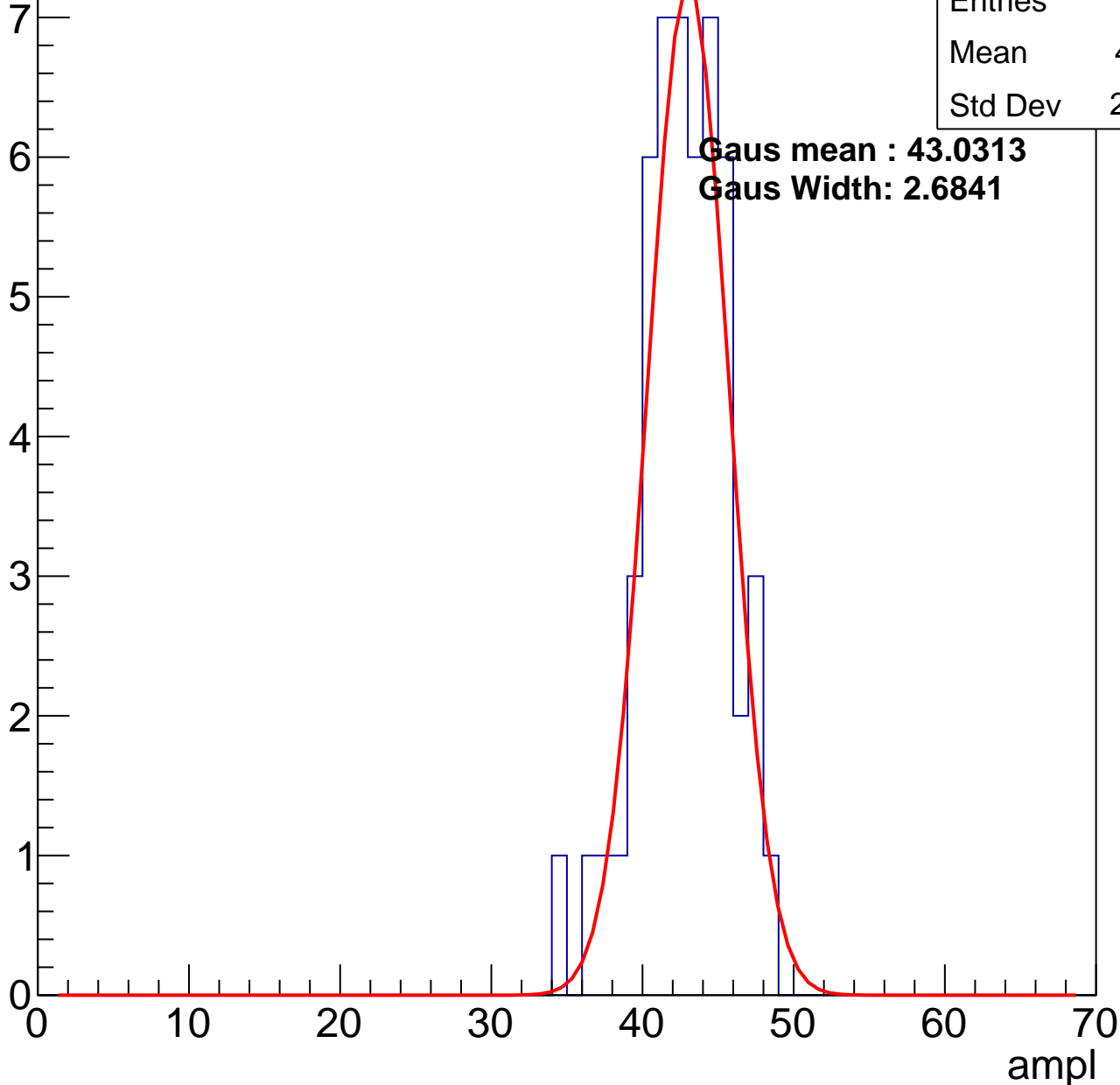
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	52
Mean	42.31
Std Dev	2.859

**Gaus mean : 43.0313**

**Gaus Width: 2.6841**

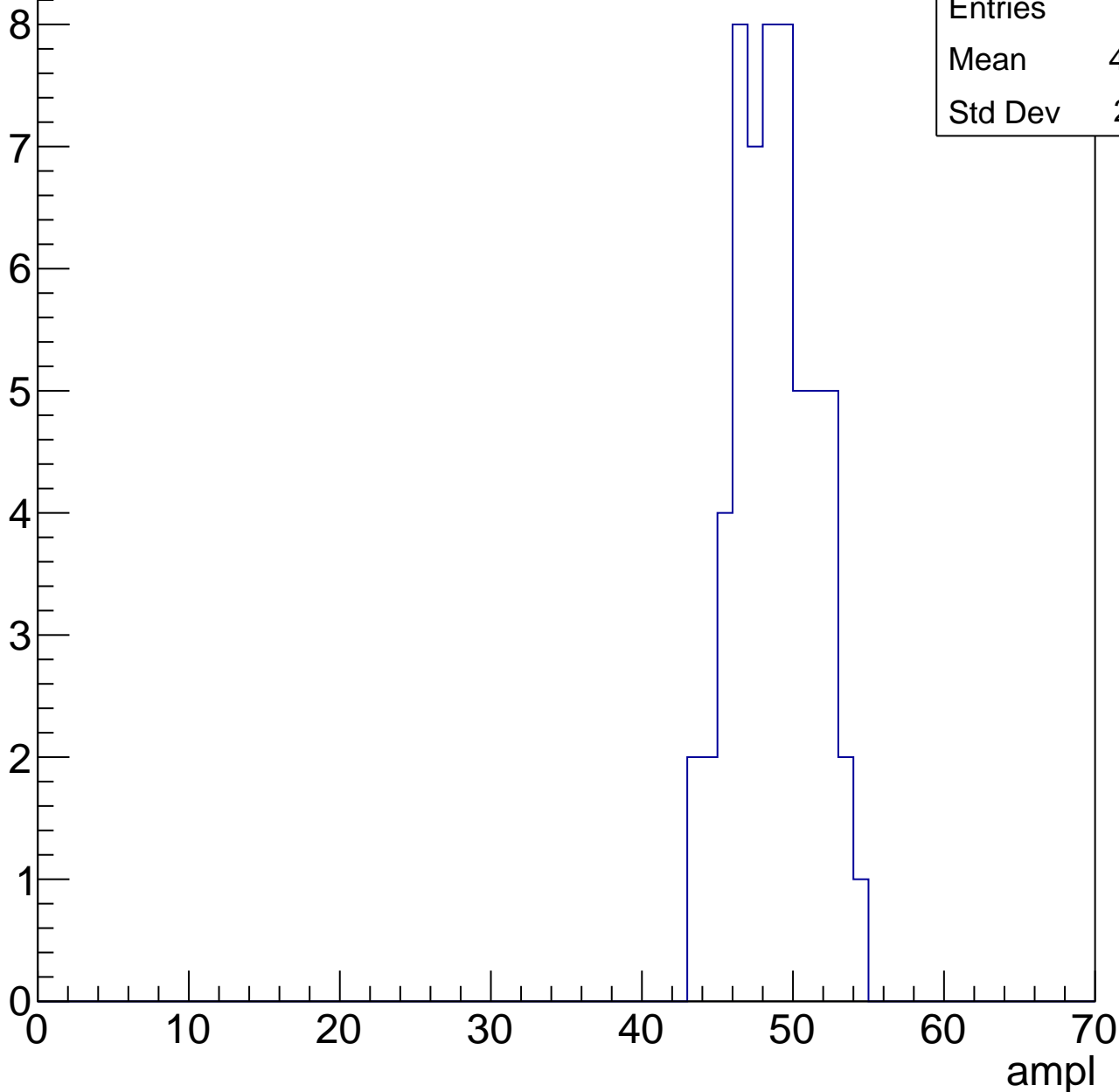


# B1L003S, U11-ch75, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

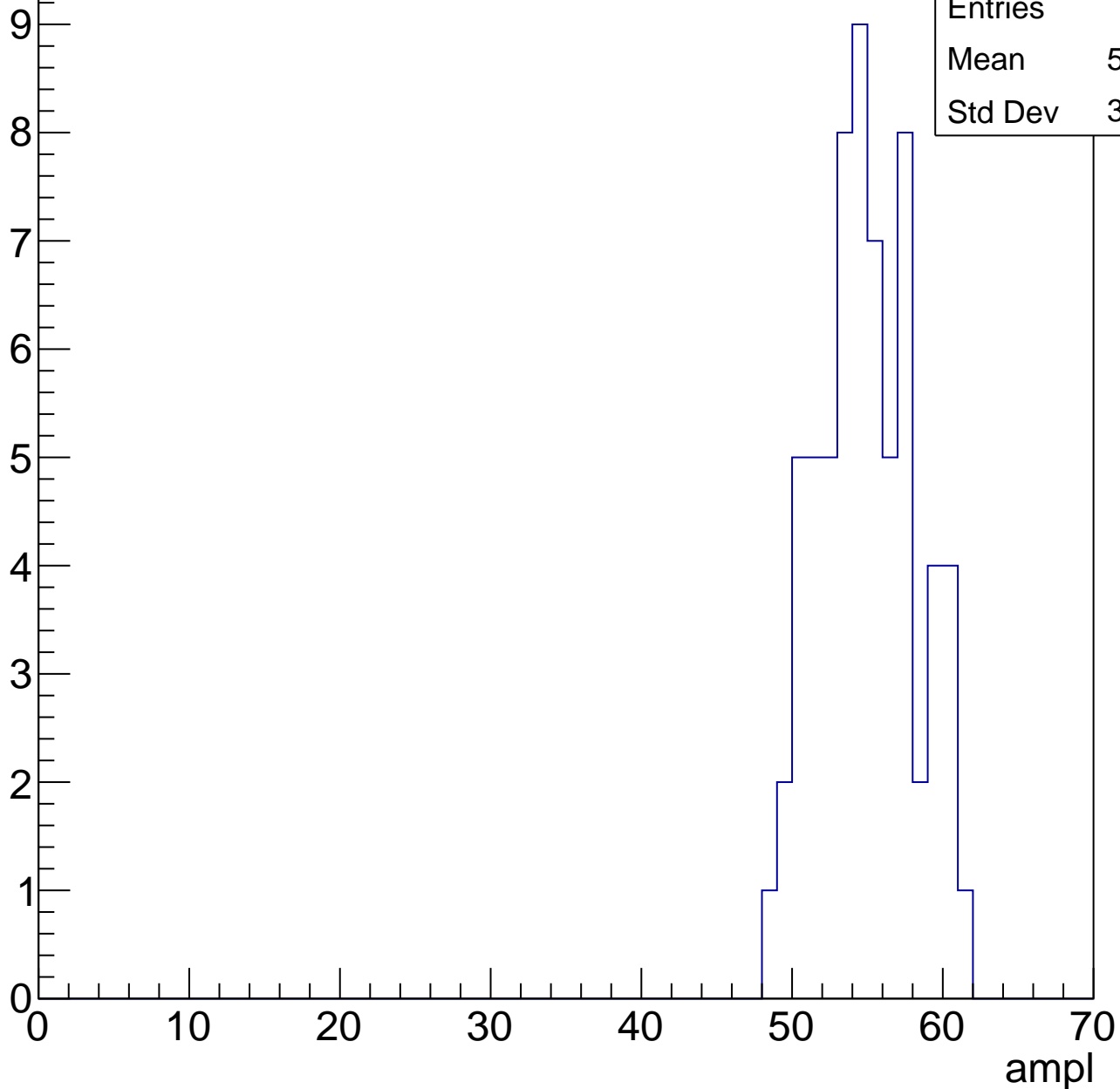
Entries	57
Mean	48.28
Std Dev	2.621



# B1L003S, U11-ch75, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	66
Mean	54.47
Std Dev	3.134

# B1L003S, U11-ch75, adc5

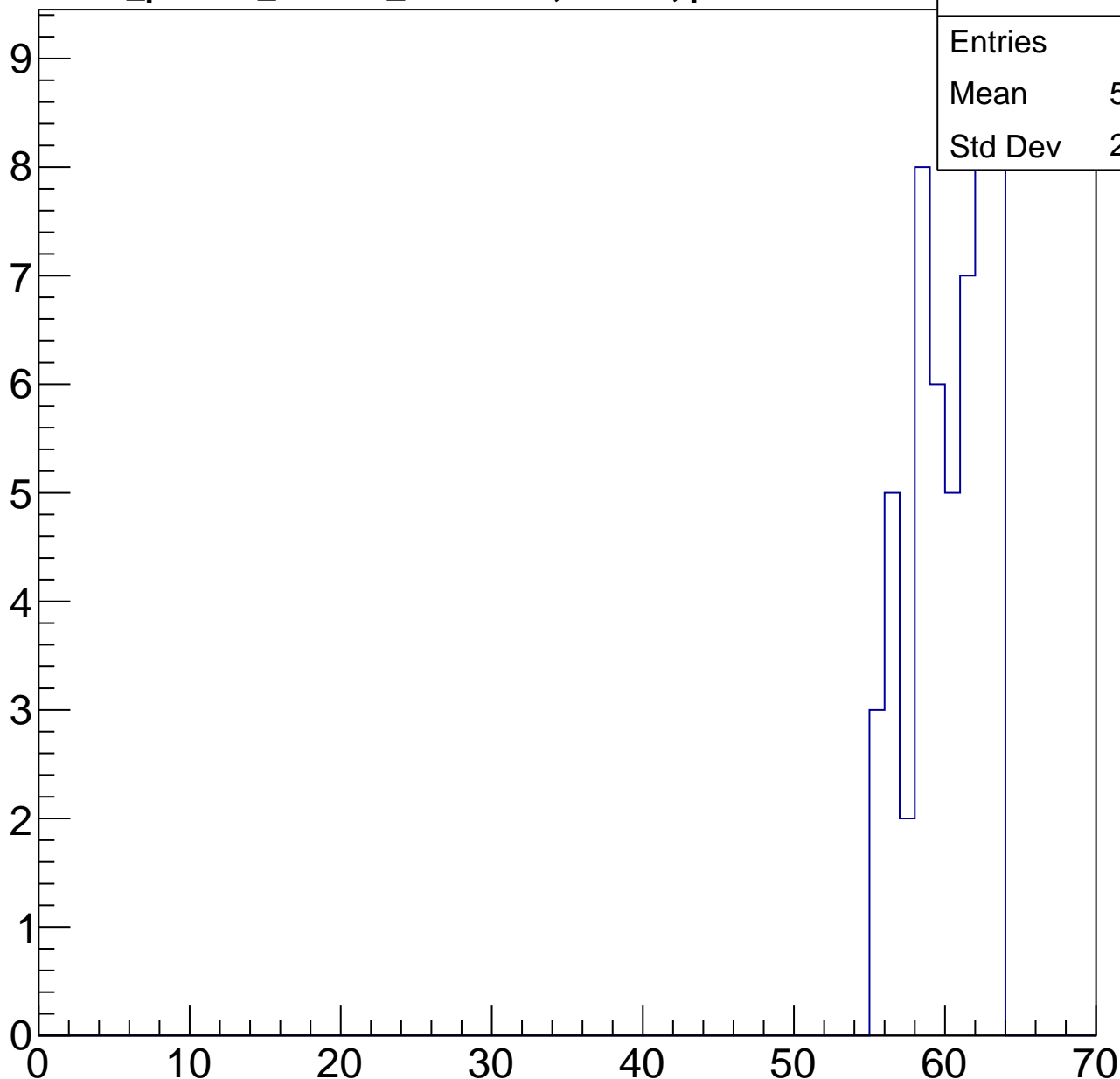
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	53
Mean	59.74
Std Dev	2.466

ampl



# B1L003S, U11-ch75, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

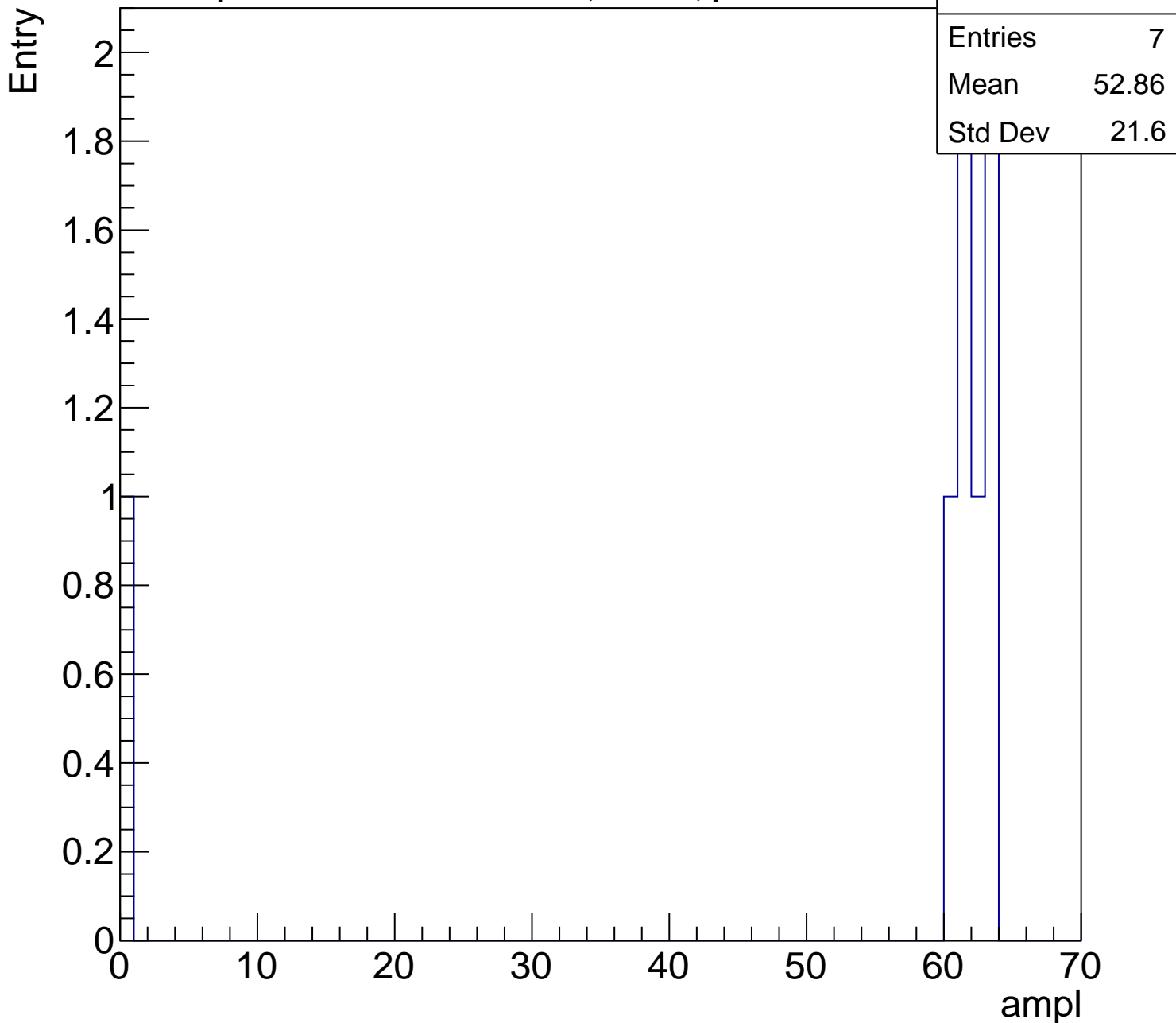
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	7
Mean	52.86
Std Dev	21.6

0 10 20 30 40 50 60 70

ampl





# B1L003S, U11-ch75, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L003S, U11-ch76, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	73
Mean	29.38
Std Dev	5.956

**Gaus mean : 30.8375**

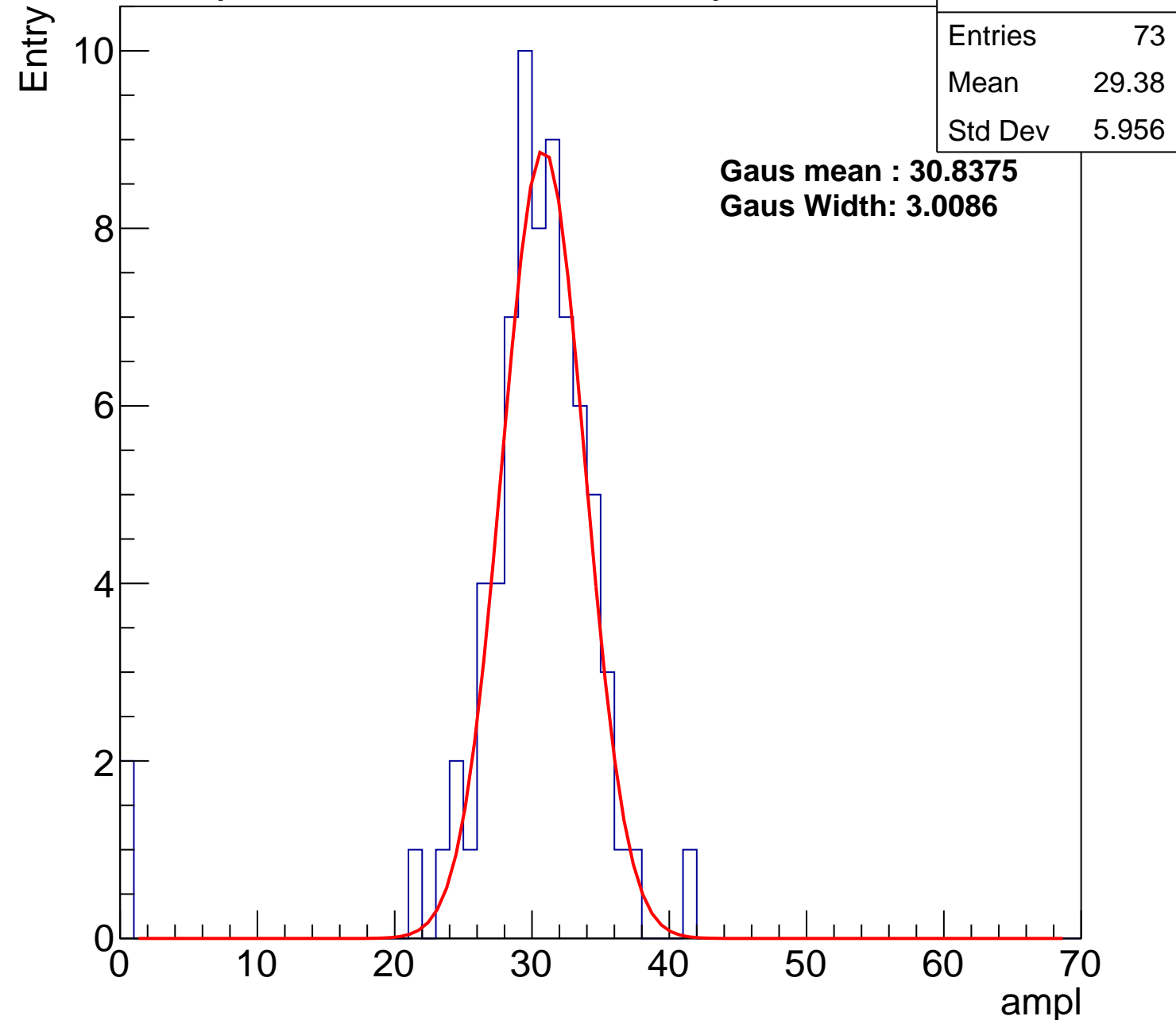
**Gaus Width: 3.0086**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U11-ch76, adc1

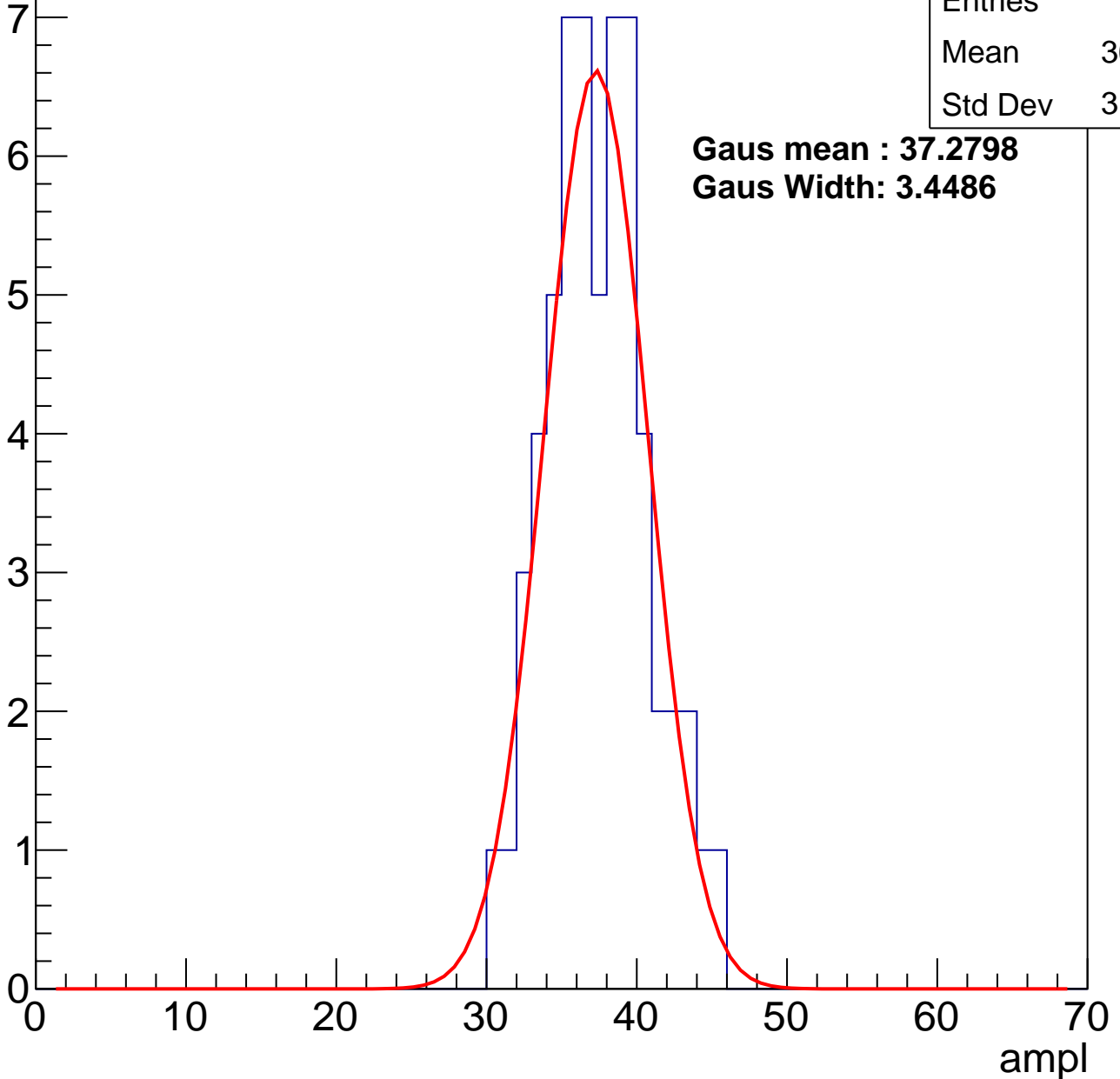
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	36.97
Std Dev	3.299

**Gaus mean : 37.2798**

**Gaus Width: 3.4486**



# B1L003S, U11-ch76, adc2

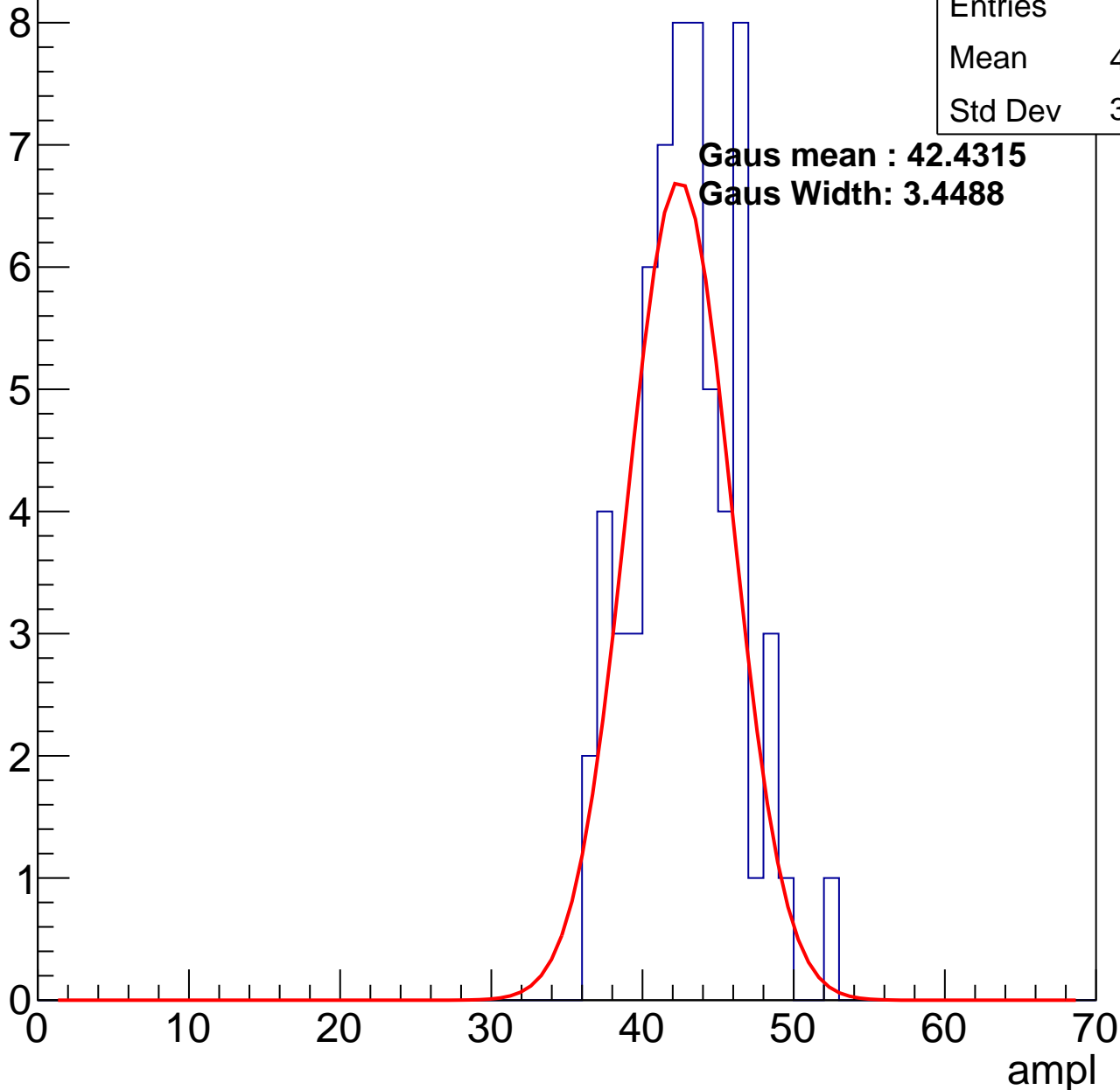
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	42.47
Std Dev	3.396

**Gaus mean : 42.4315**

**Gaus Width: 3.4488**



# B1L003S, U11-ch76, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

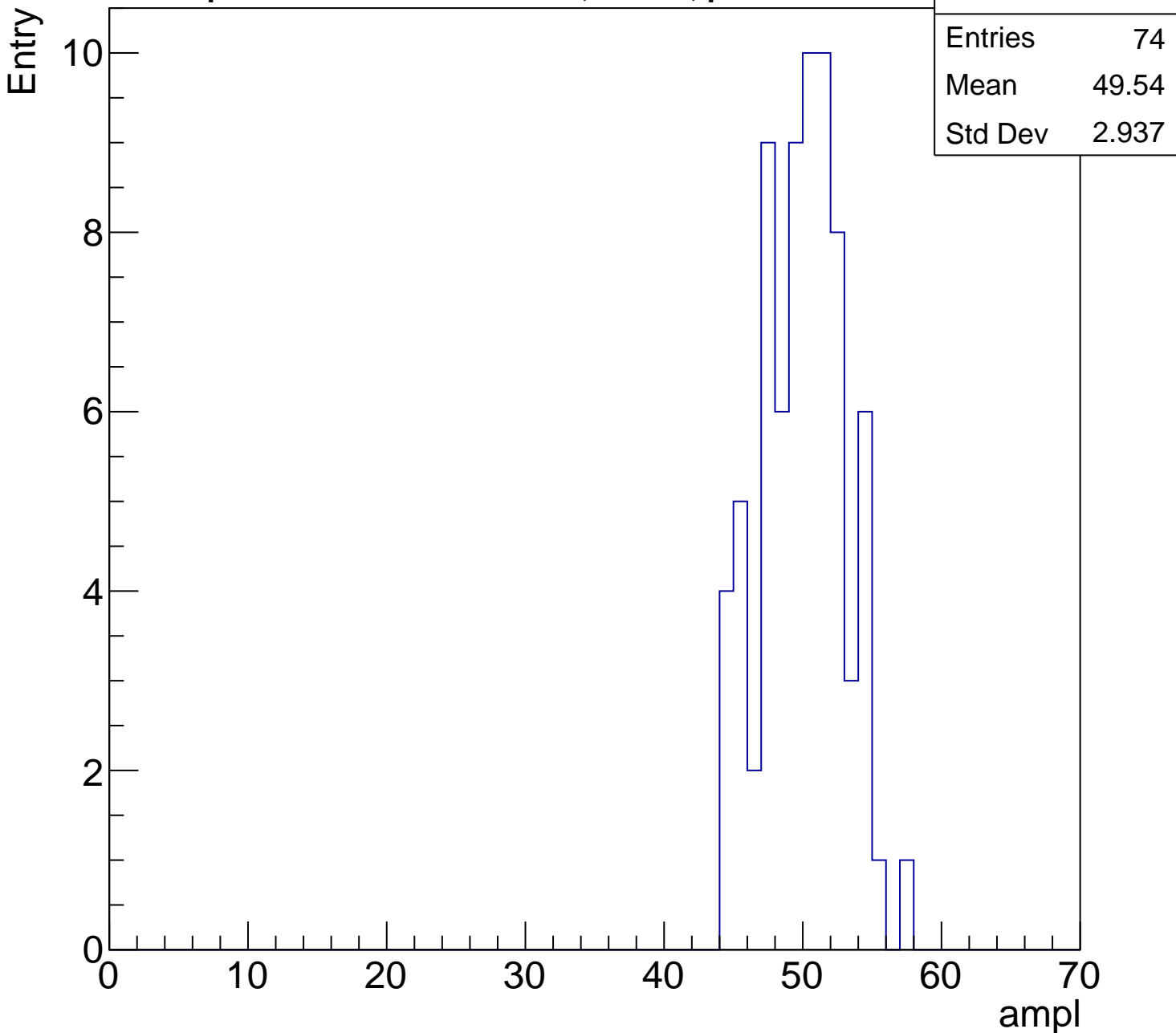
Entries	74
Mean	49.54
Std Dev	2.937

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

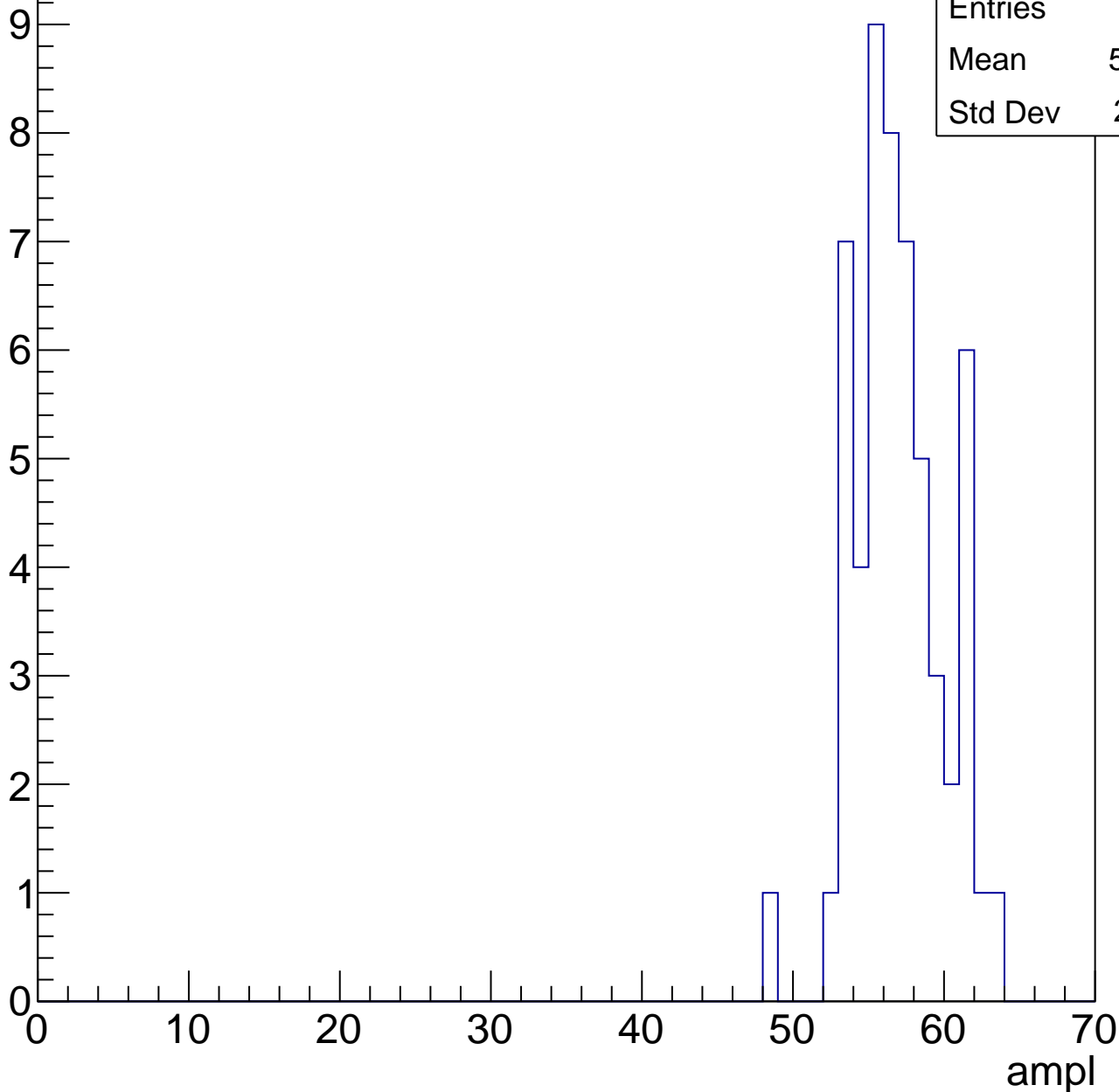


# B1L003S, U11-ch76, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	56.49
Std Dev	2.941

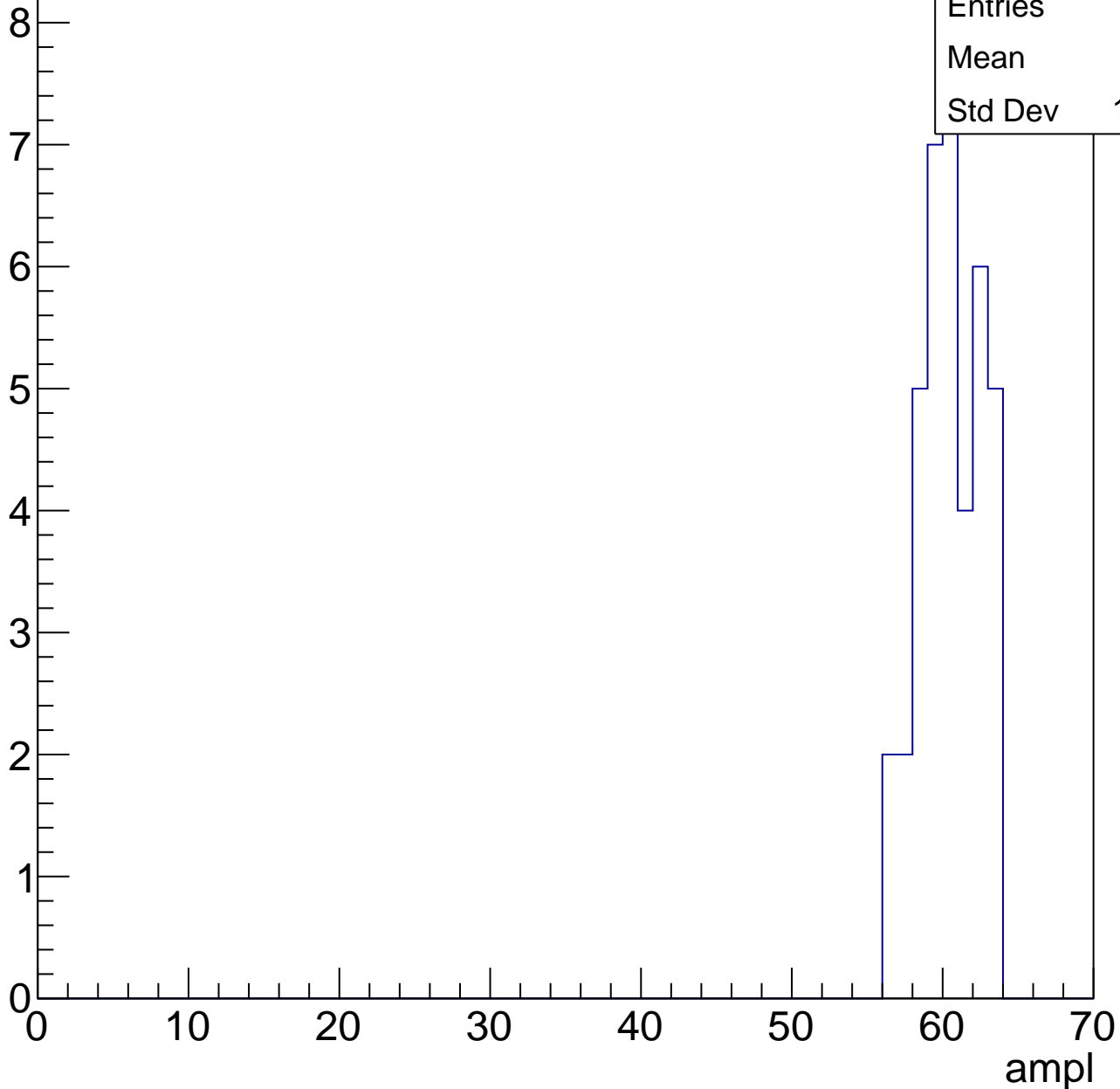


# B1L003S, U11-ch76, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

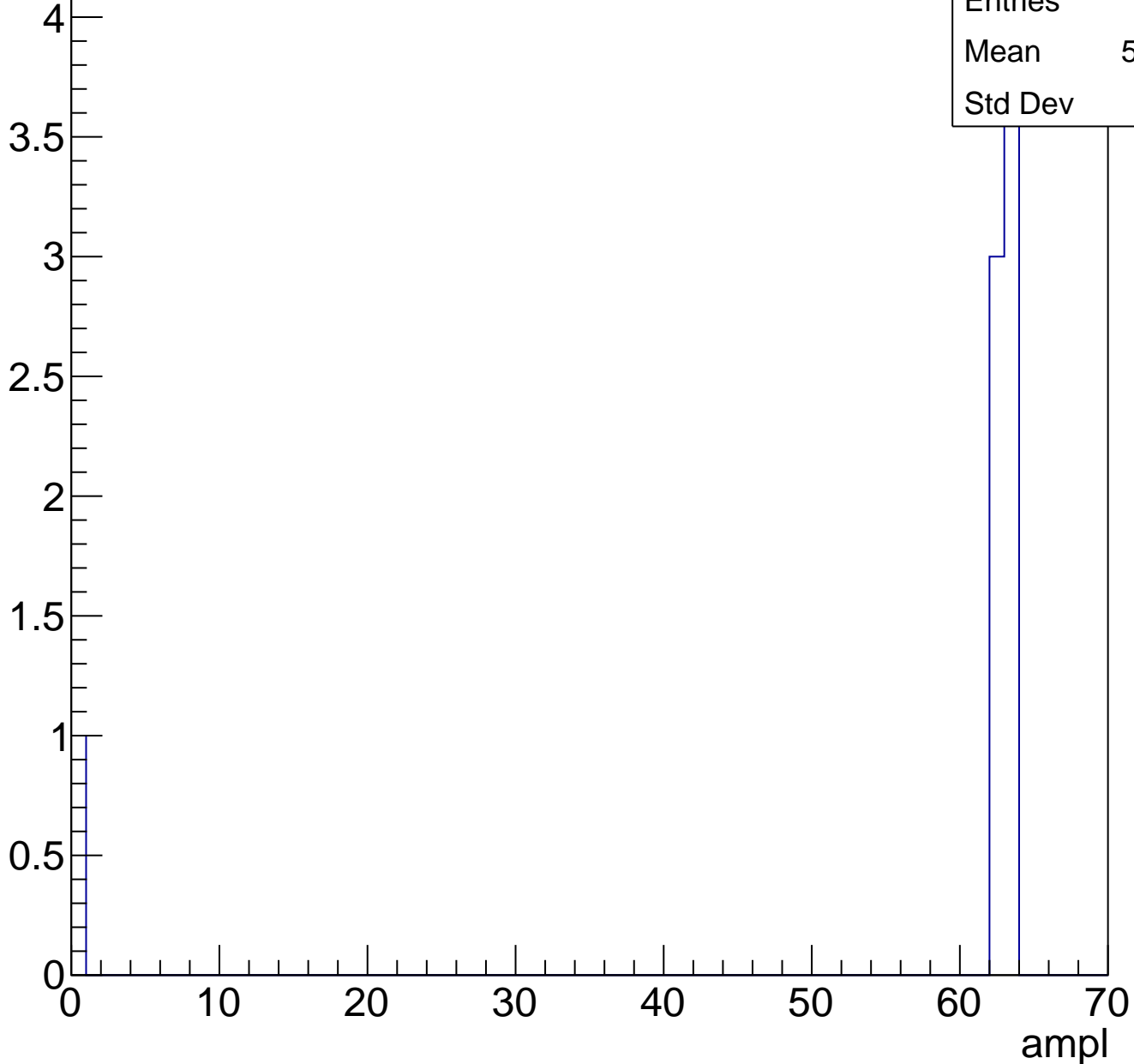
Entries	39
Mean	60
Std Dev	1.961



# B1L003S, U11-ch76, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch76, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U11-ch77, adc0

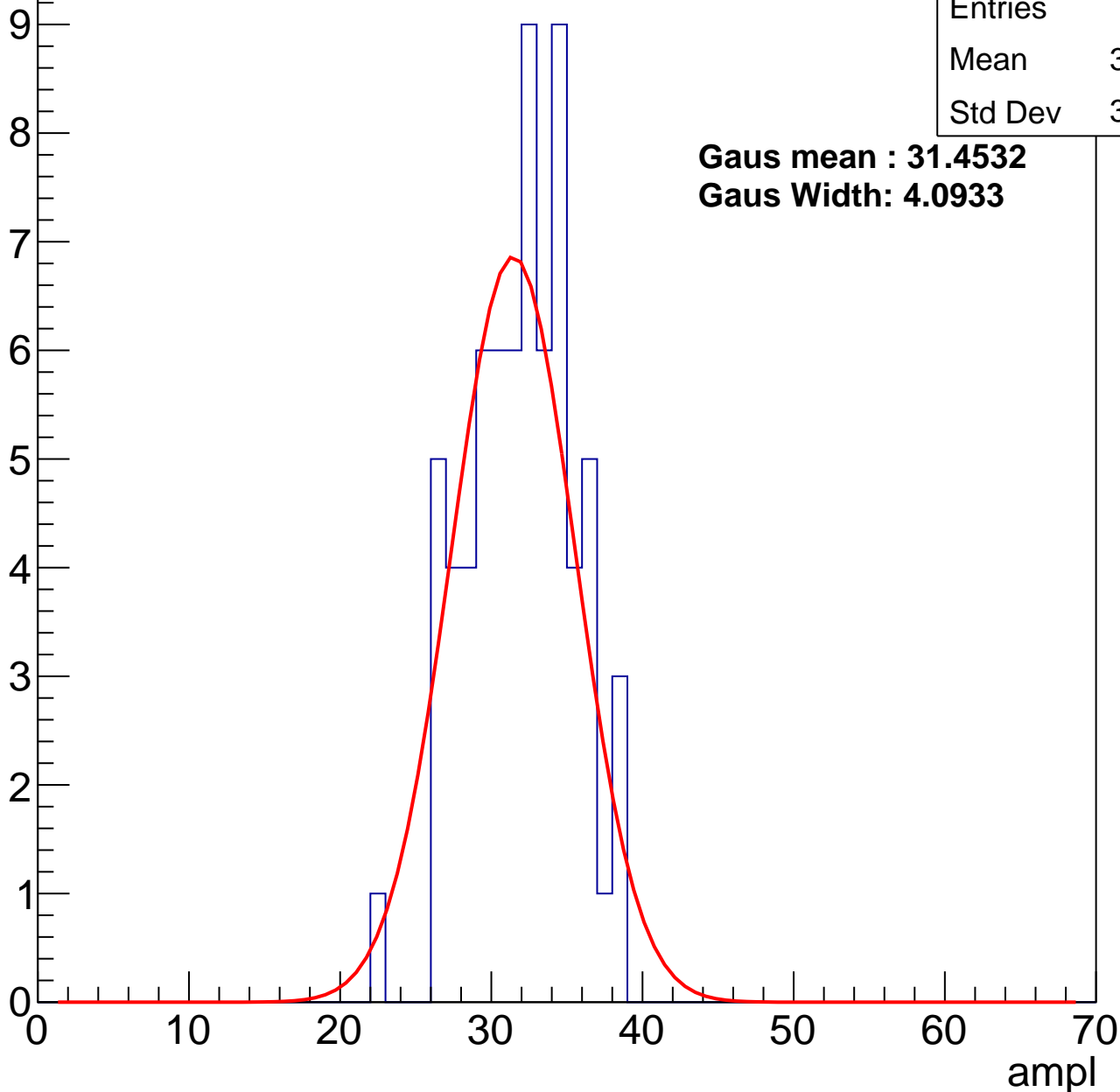
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	31.52
Std Dev	3.412

**Gaus mean : 31.4532**

**Gaus Width: 4.0933**



# B1L003S, U11-ch77, adc1

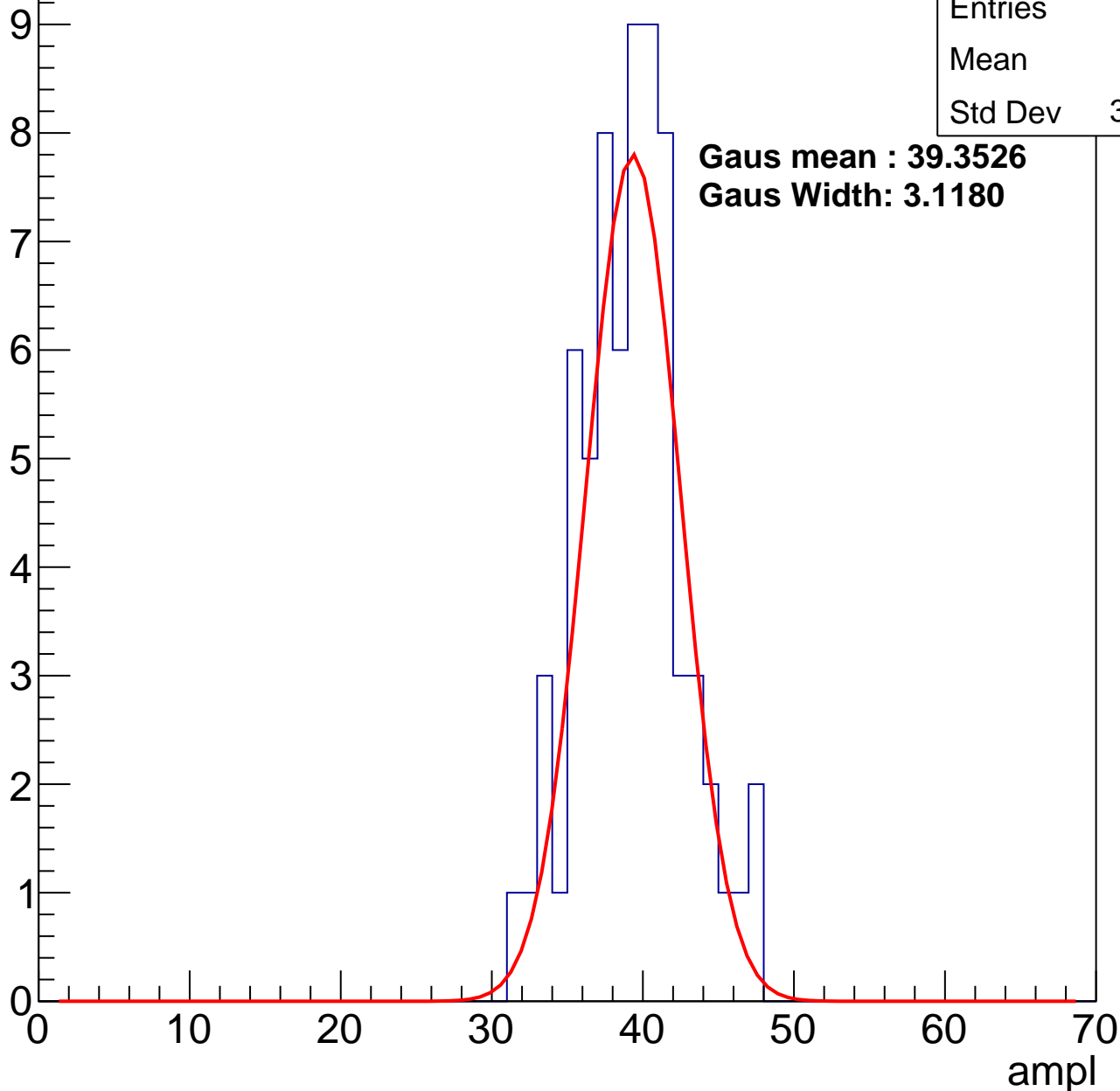
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	38.8
Std Dev	3.407

**Gaus mean : 39.3526**

**Gaus Width: 3.1180**



# B1L003S, U11-ch77, adc2

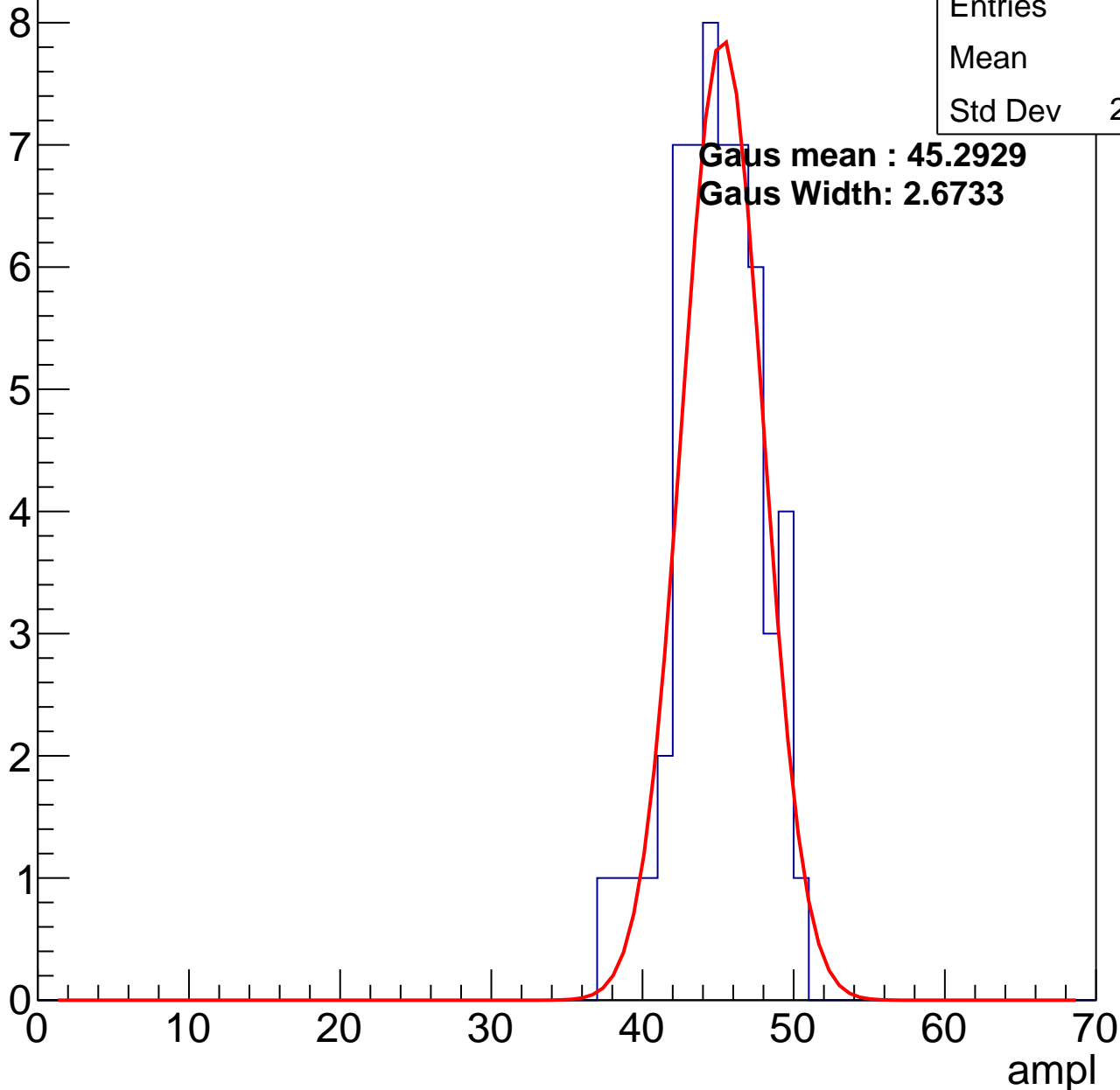
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	44.5
Std Dev	2.797

**Gaus mean : 45.2929**

**Gaus Width: 2.6733**

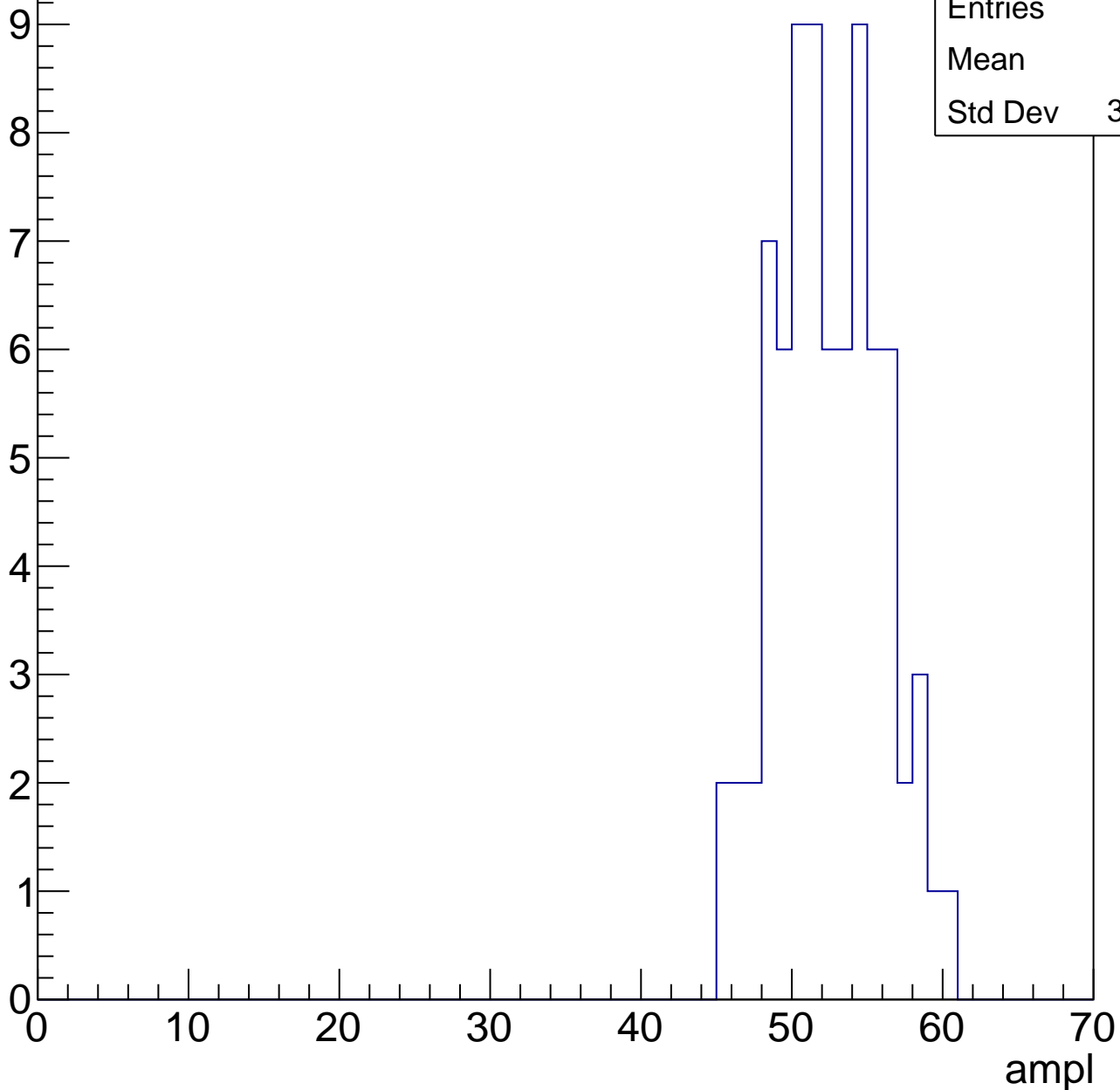


# B1L003S, U11-ch77, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

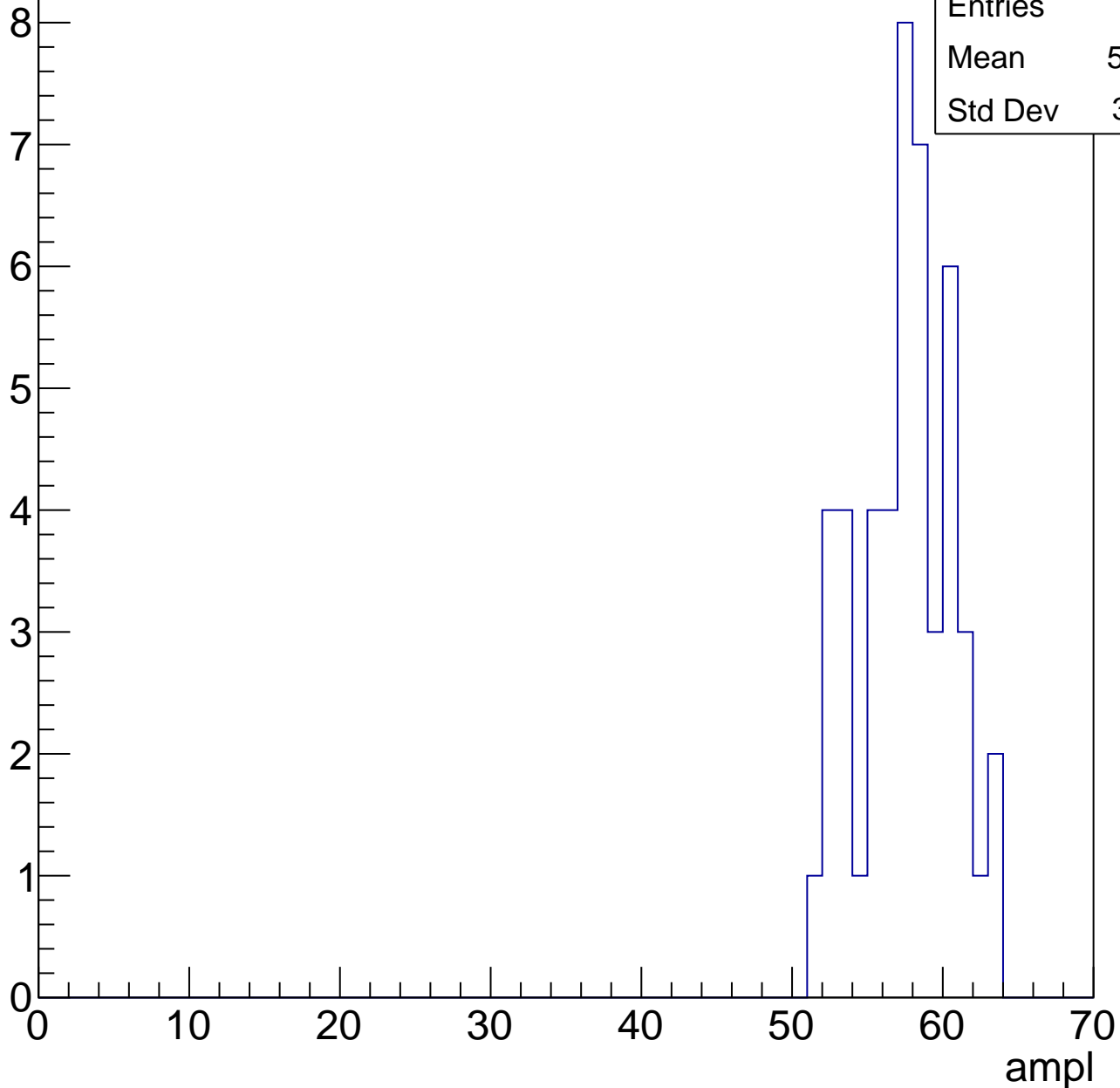
Entries	77
Mean	52
Std Dev	3.407



# B1L003S, U11-ch77, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

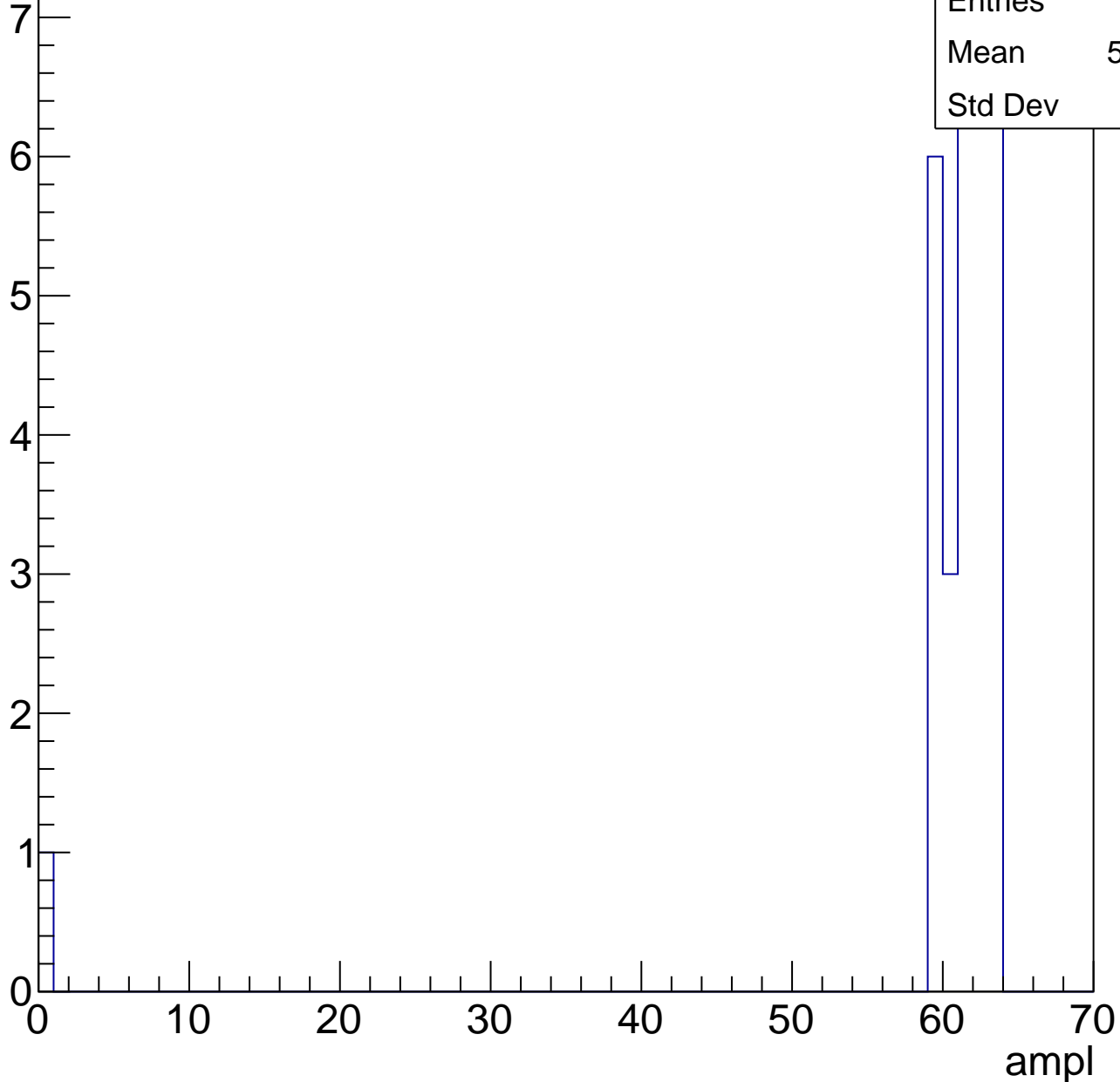


Entries	48
Mean	57.06
Std Dev	3.051

# B1L003S, U11-ch77, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U11-ch77, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.33
Std Dev	0.4714

ampl



# B1L003S, U11-ch77, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	4
Mean	0
Std Dev	0

# B1L003S, U11-ch78, adc0

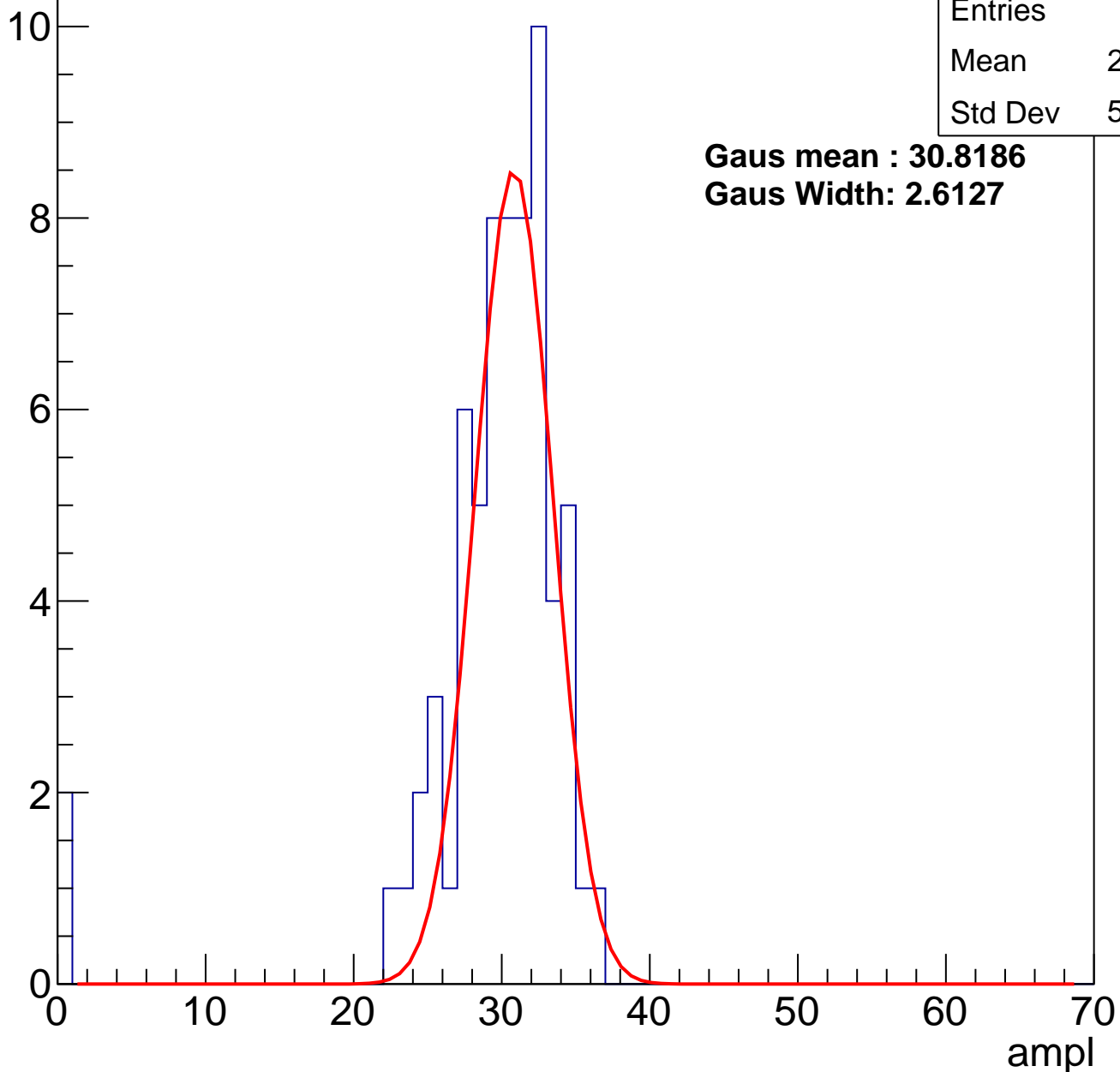
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	66
Mean	28.92
Std Dev	5.912

**Gaus mean : 30.8186**

**Gaus Width: 2.6127**

Entry



# B1L003S, U11-ch78, adc1

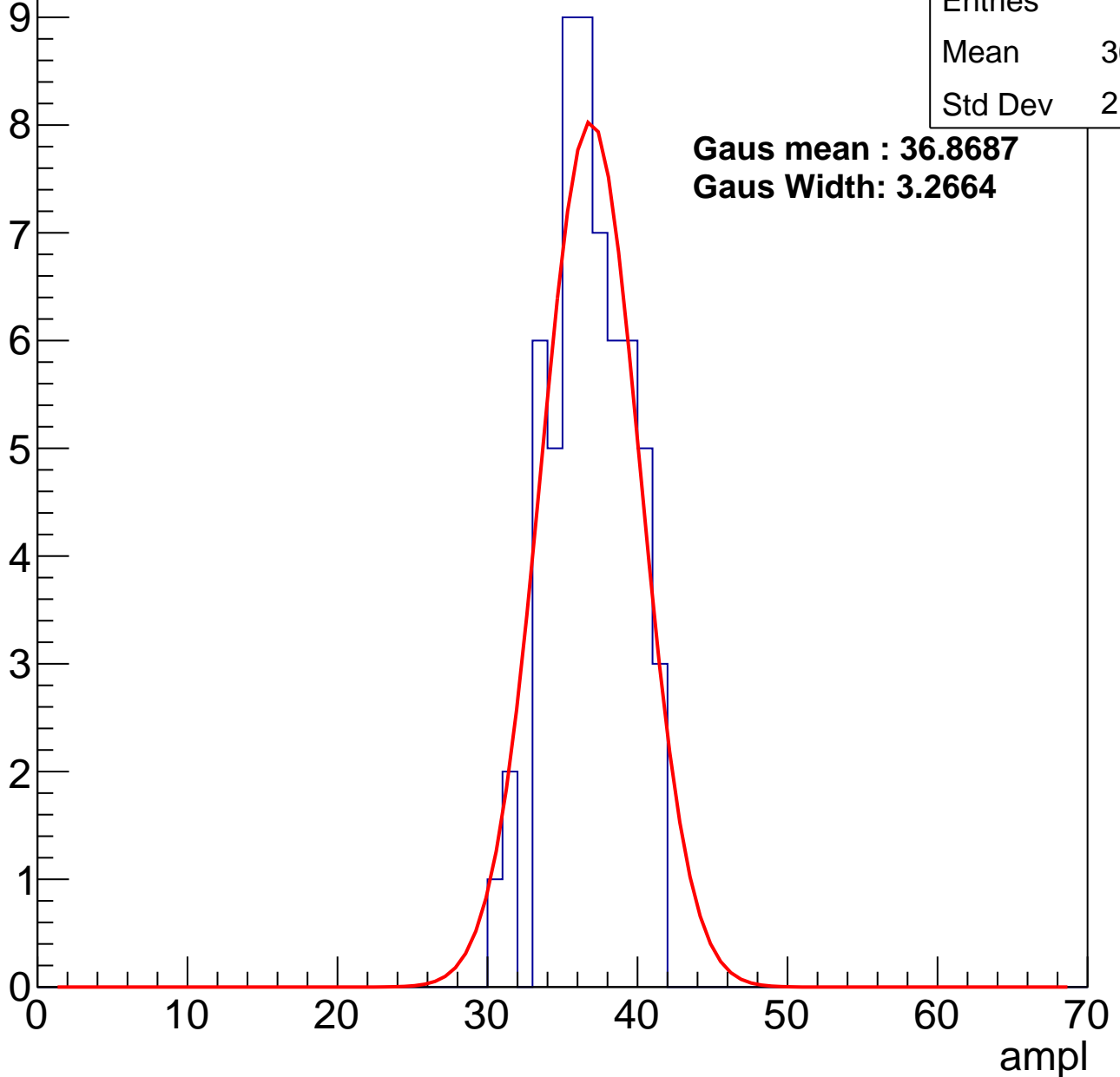
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	36.32
Std Dev	2.613

**Gaus mean : 36.8687**

**Gaus Width: 3.2664**



# B1L003S, U11-ch78, adc2

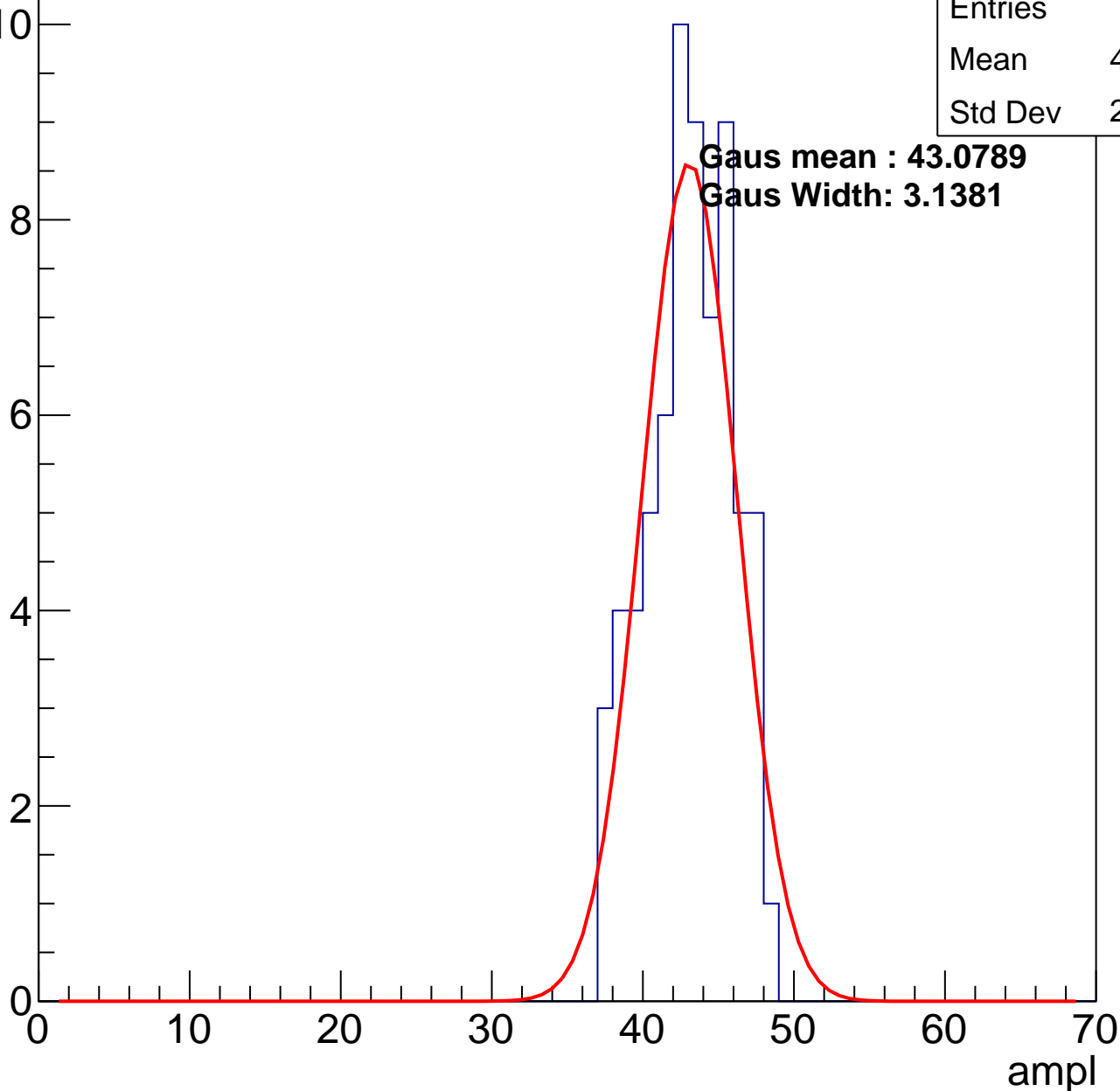
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	42.62
Std Dev	2.802

**Gaus mean : 43.0789**

**Gaus Width: 3.1381**

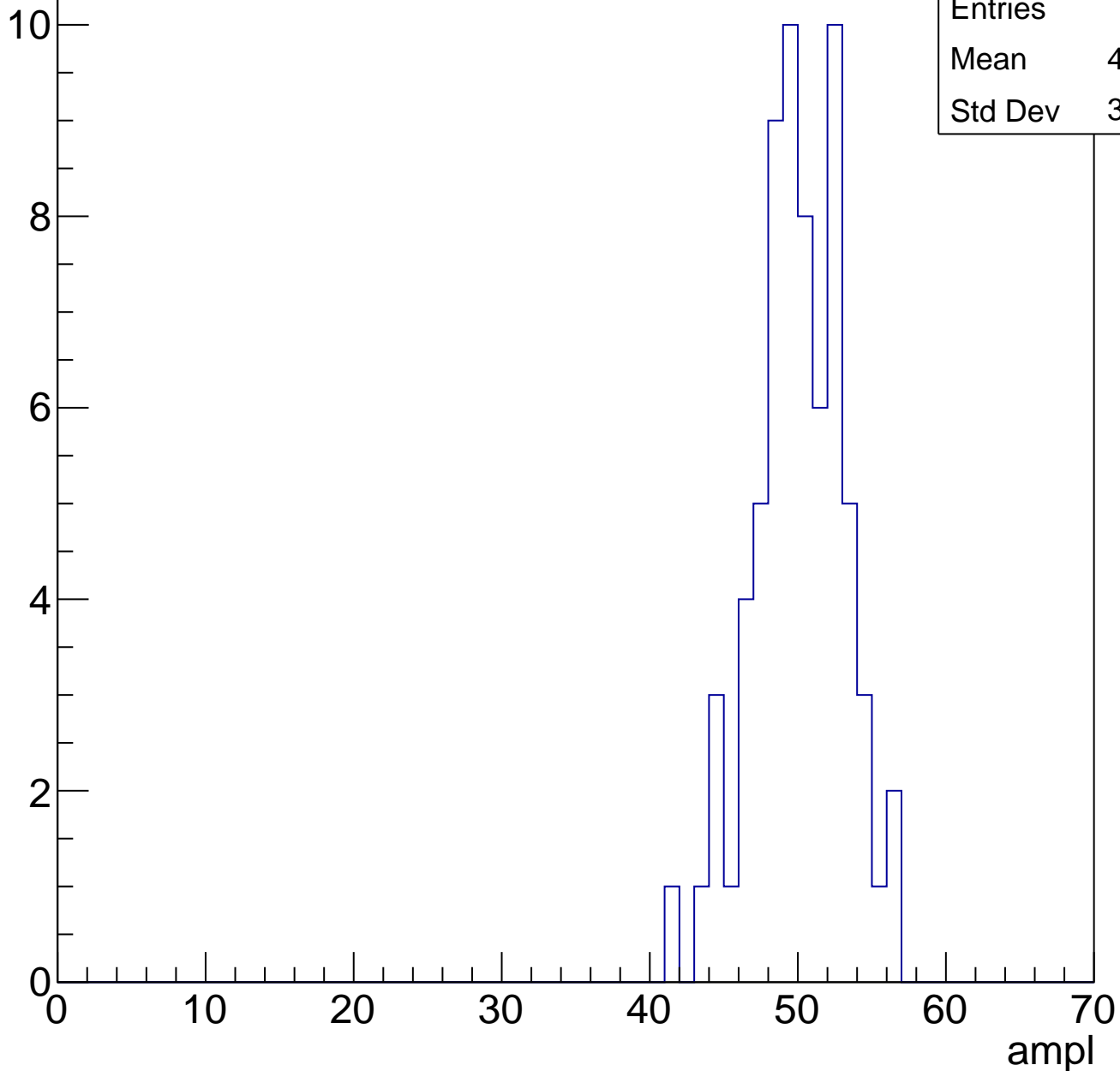


# B1L003S, U11-ch78, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	69
Mean	49.59
Std Dev	3.052

Entry

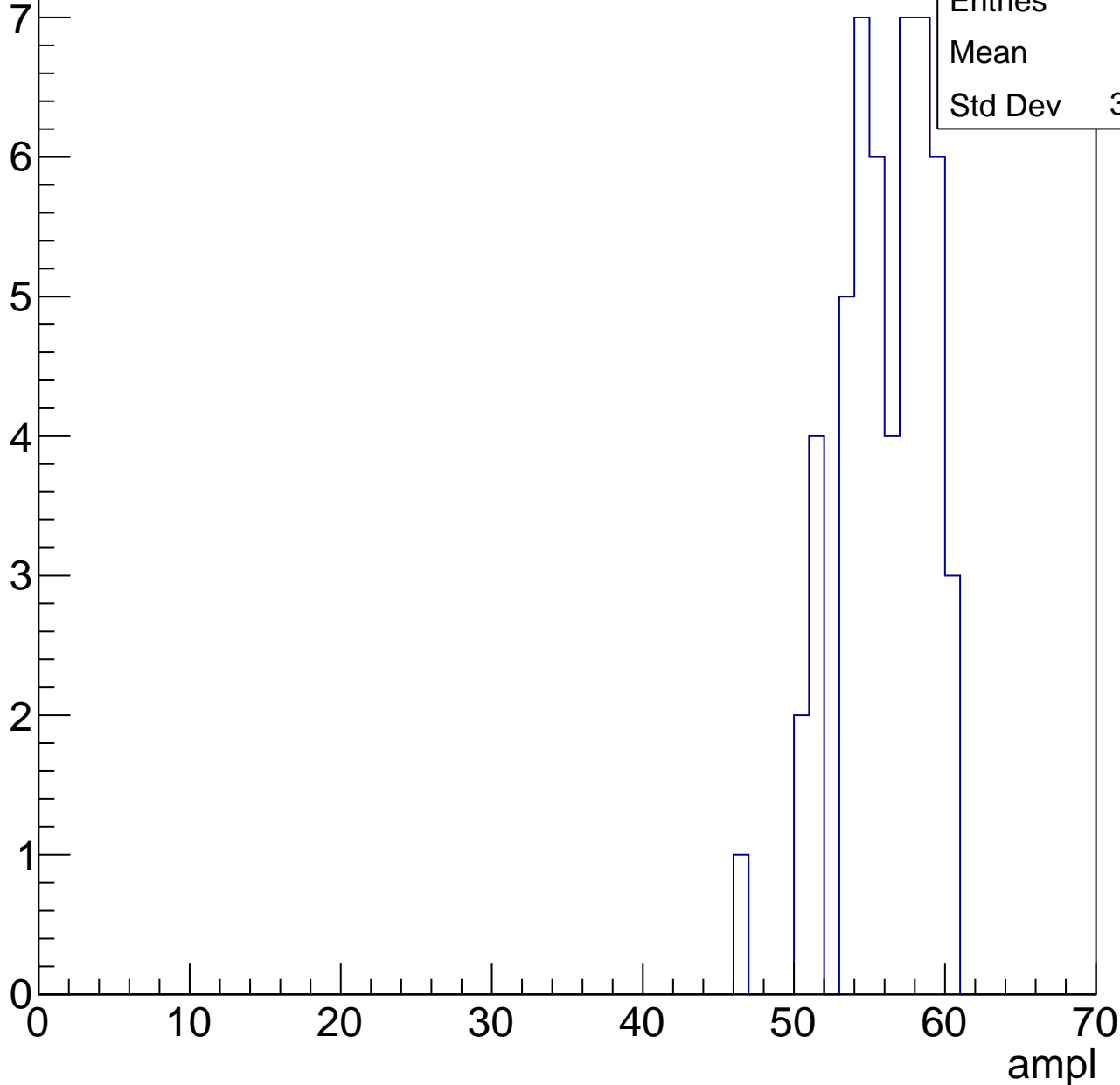


# B1L003S, U11-ch78, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	52
Mean	55.5
Std Dev	3.022

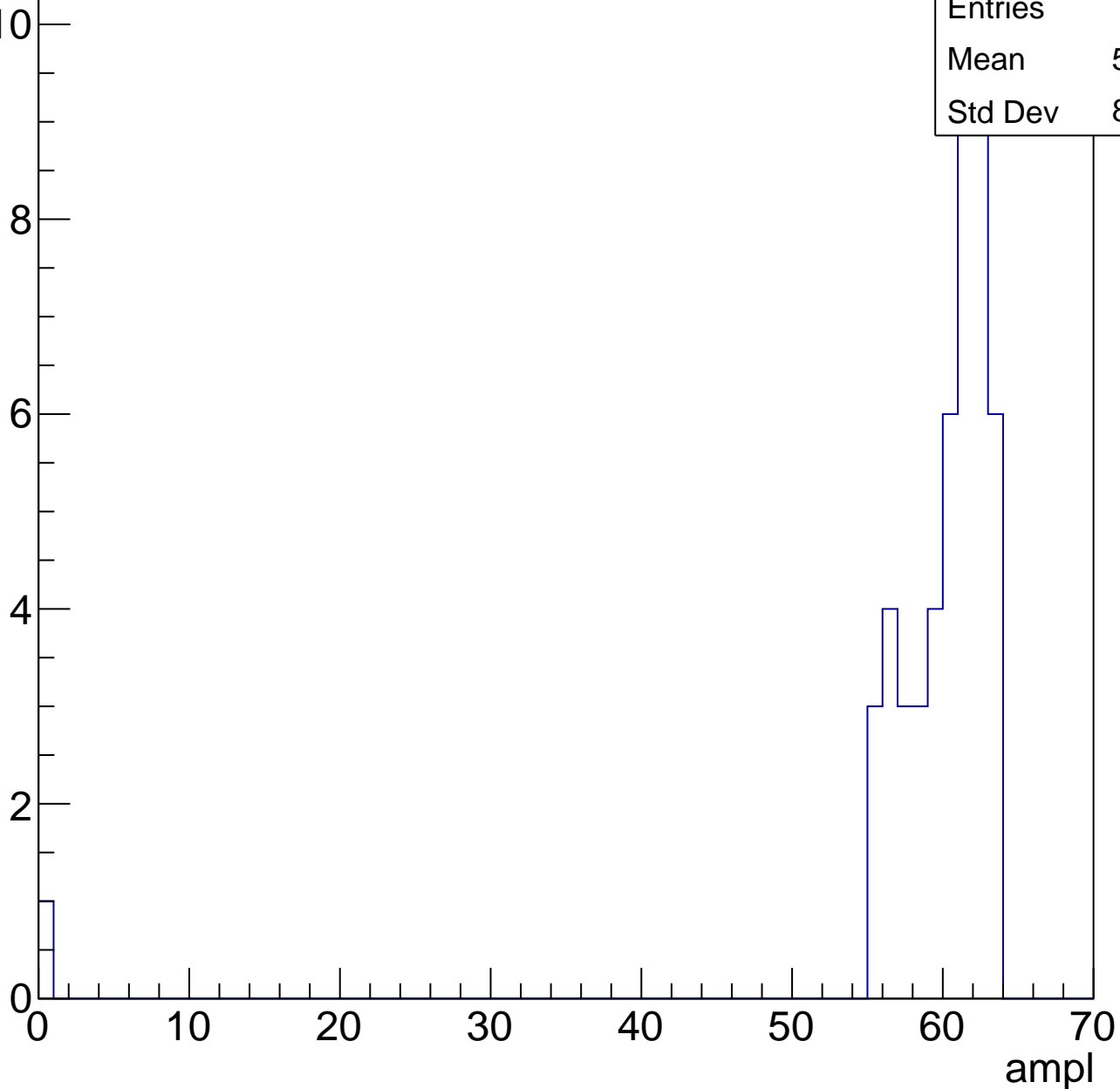


# B1L003S, U11-ch78, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

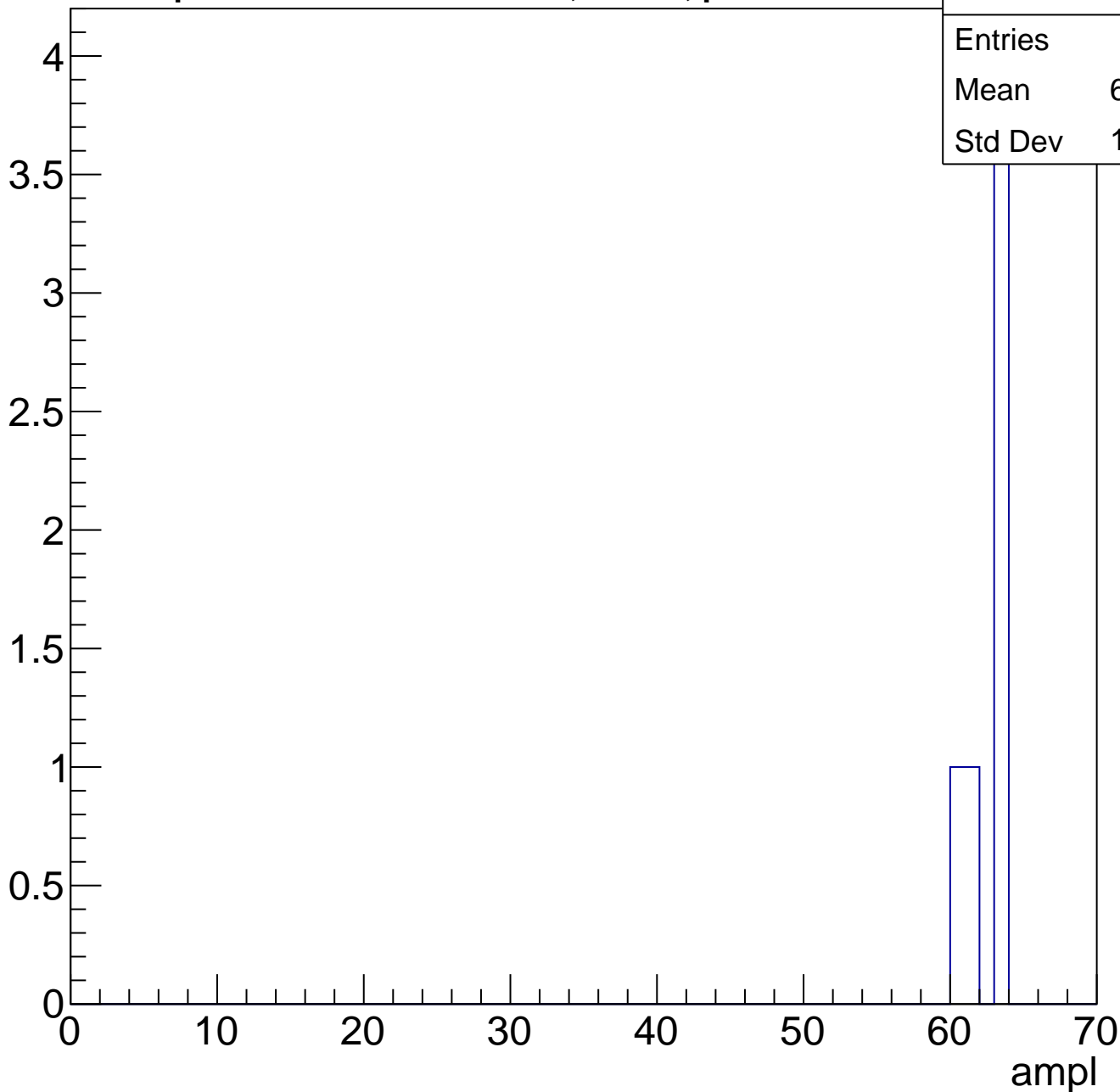
Entries	49
Mean	58.71
Std Dev	8.811



# B1L003S, U11-ch78, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch78, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U11-ch79, adc0

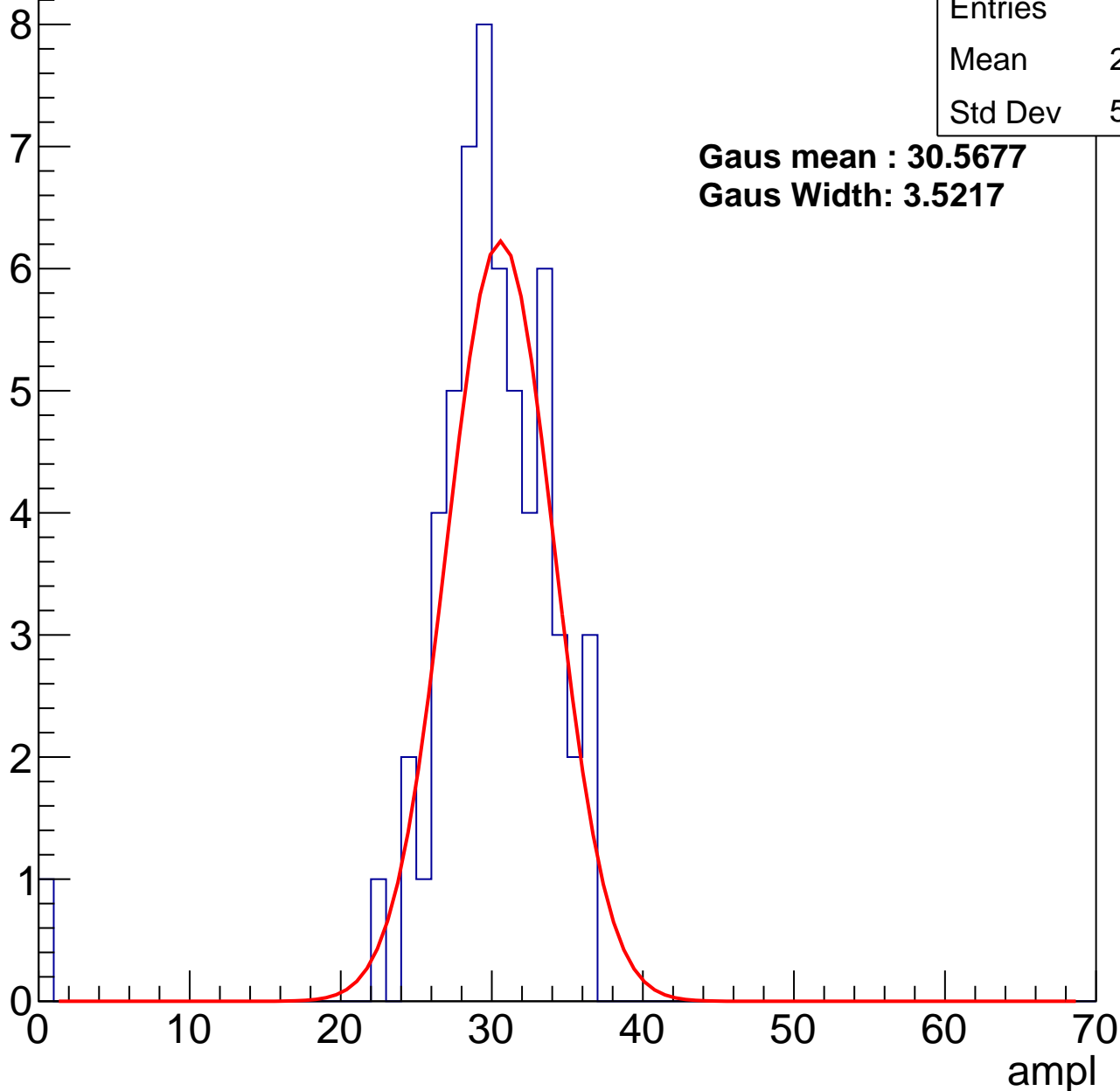
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	29.36
Std Dev	5.023

**Gaus mean : 30.5677**

**Gaus Width: 3.5217**



# B1L003S, U11-ch79, adc1

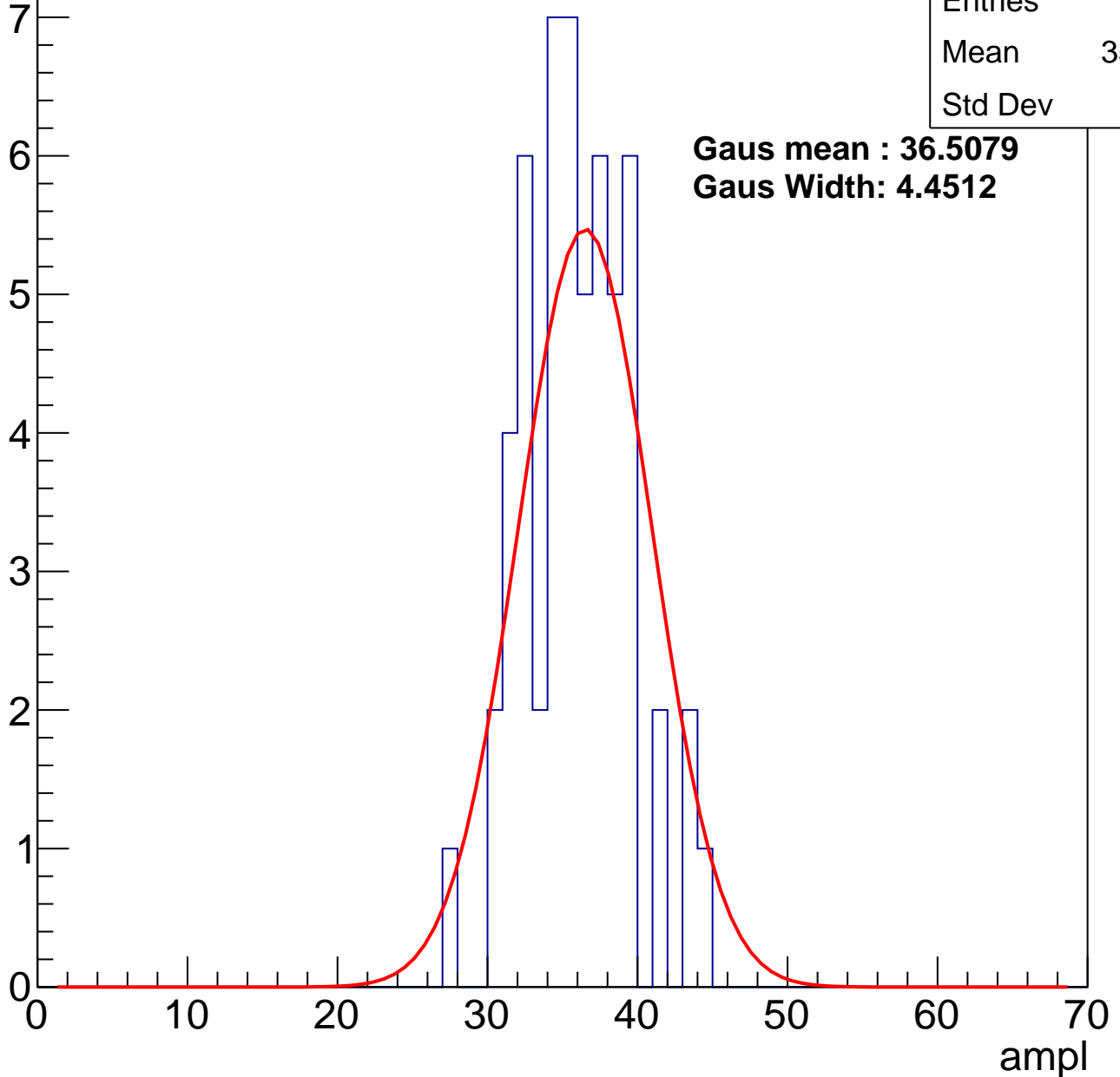
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	35.54
Std Dev	3.49

**Gaus mean : 36.5079**

**Gaus Width: 4.4512**



# B1L003S, U11-ch79, adc2

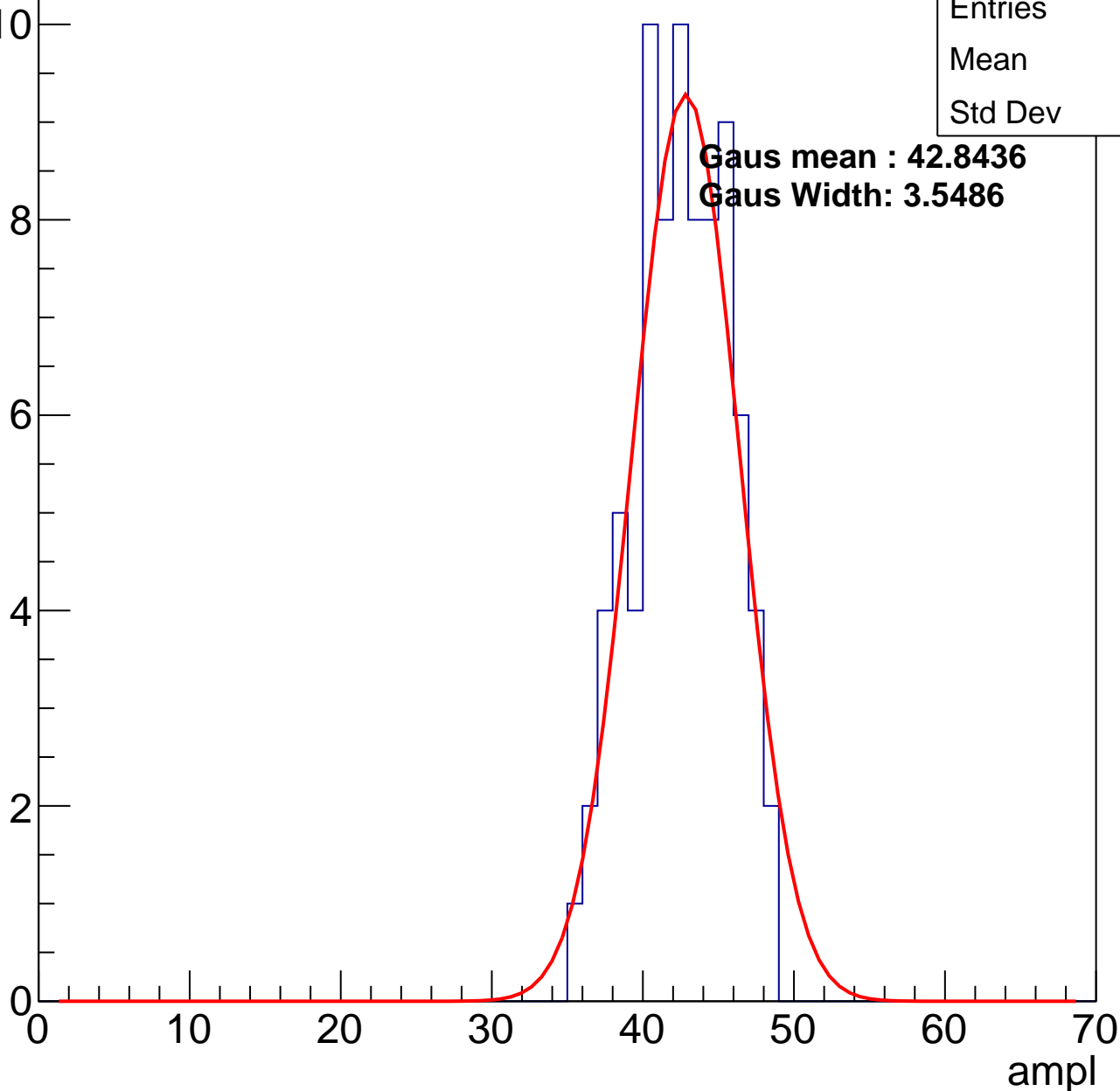
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	81
Mean	42.1
Std Dev	3.09

**Gaus mean : 42.8436**

**Gaus Width: 3.5486**



# B1L003S, U11-ch79, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	70
Mean	50.4
Std Dev	2.949

Entry

10

8

6

4

2

0

0

10

20

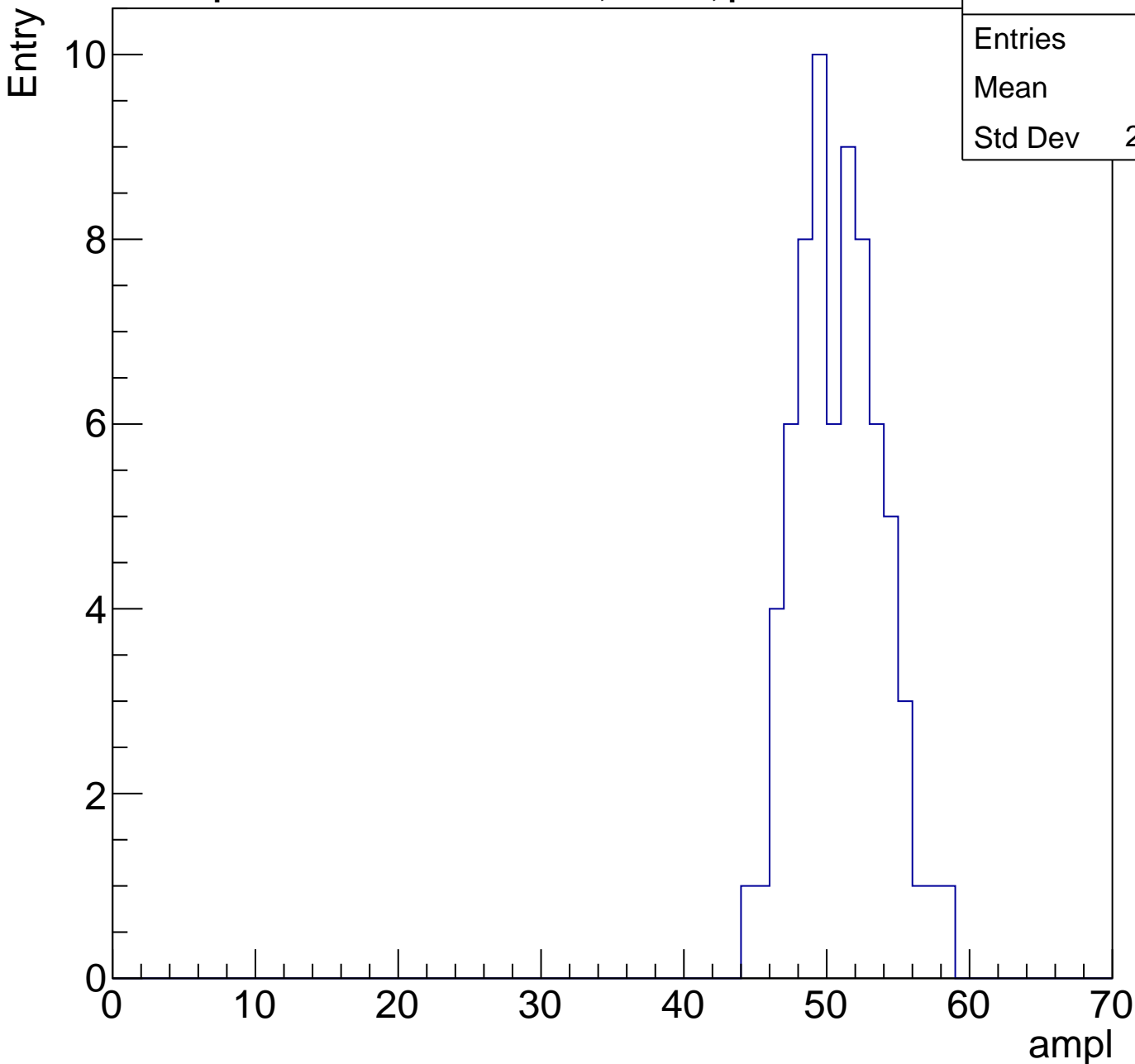
30

40

50

60

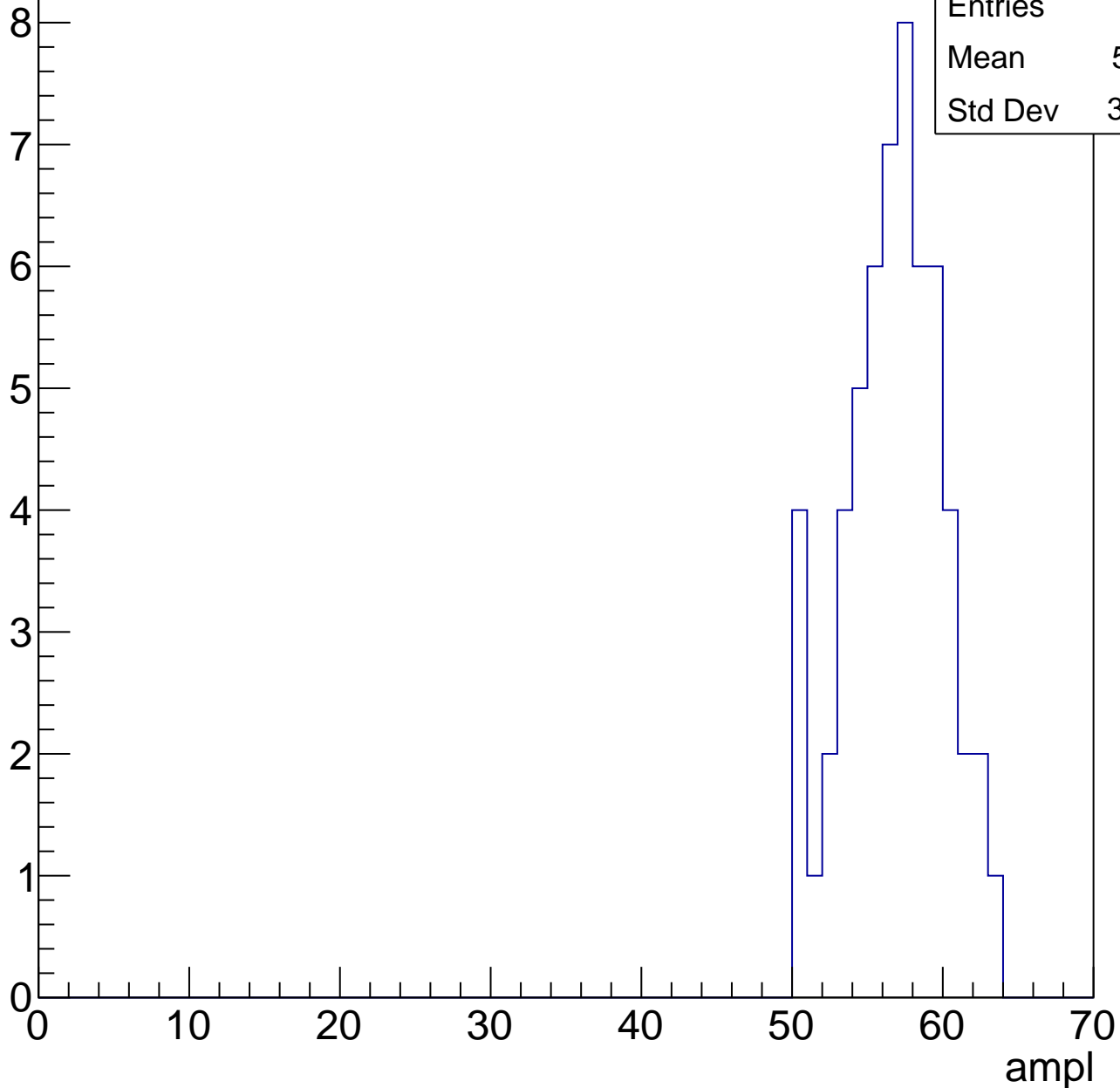
ampl



# B1L003S, U11-ch79, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

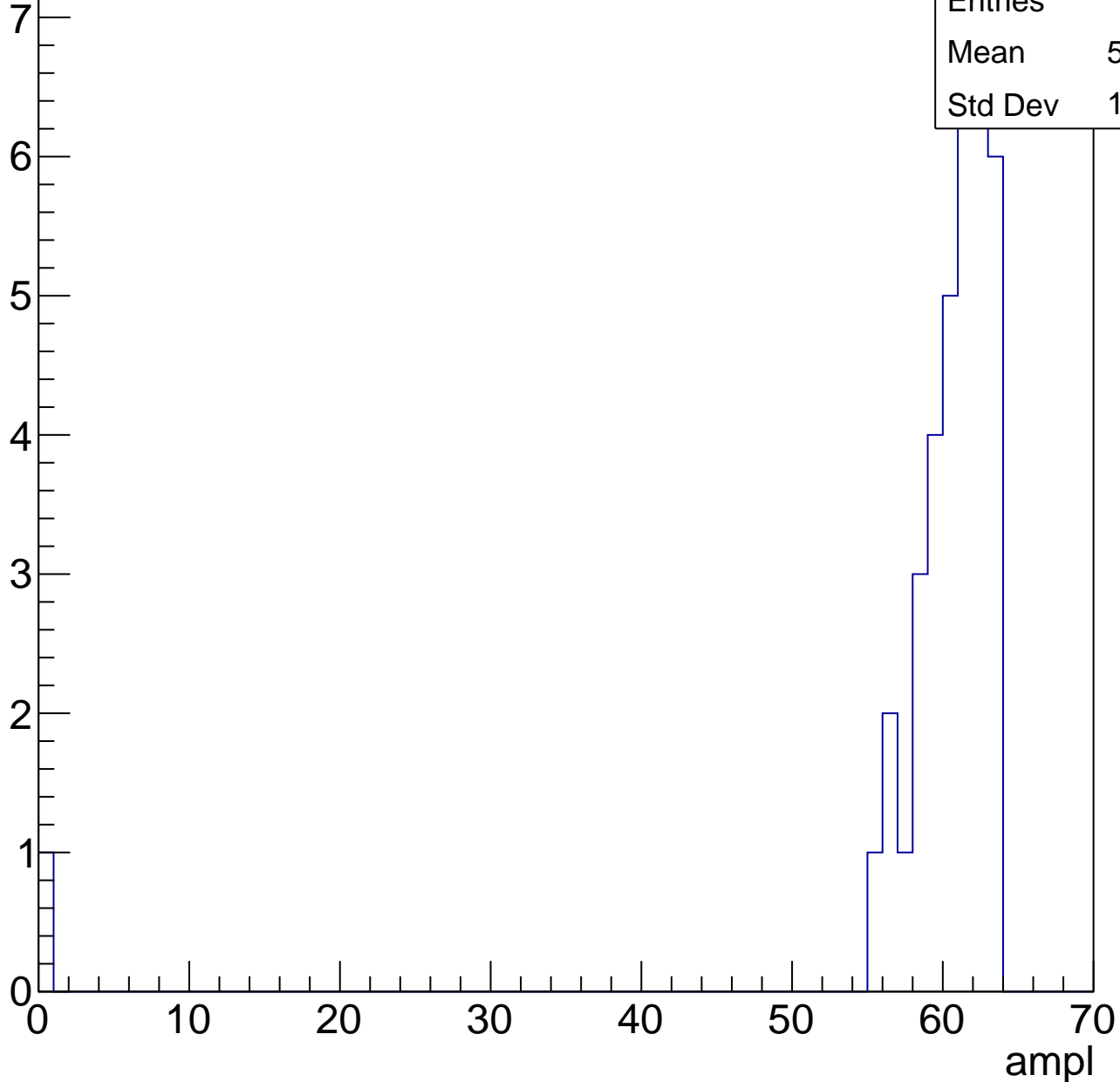
Entry



# B1L003S, U11-ch79, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

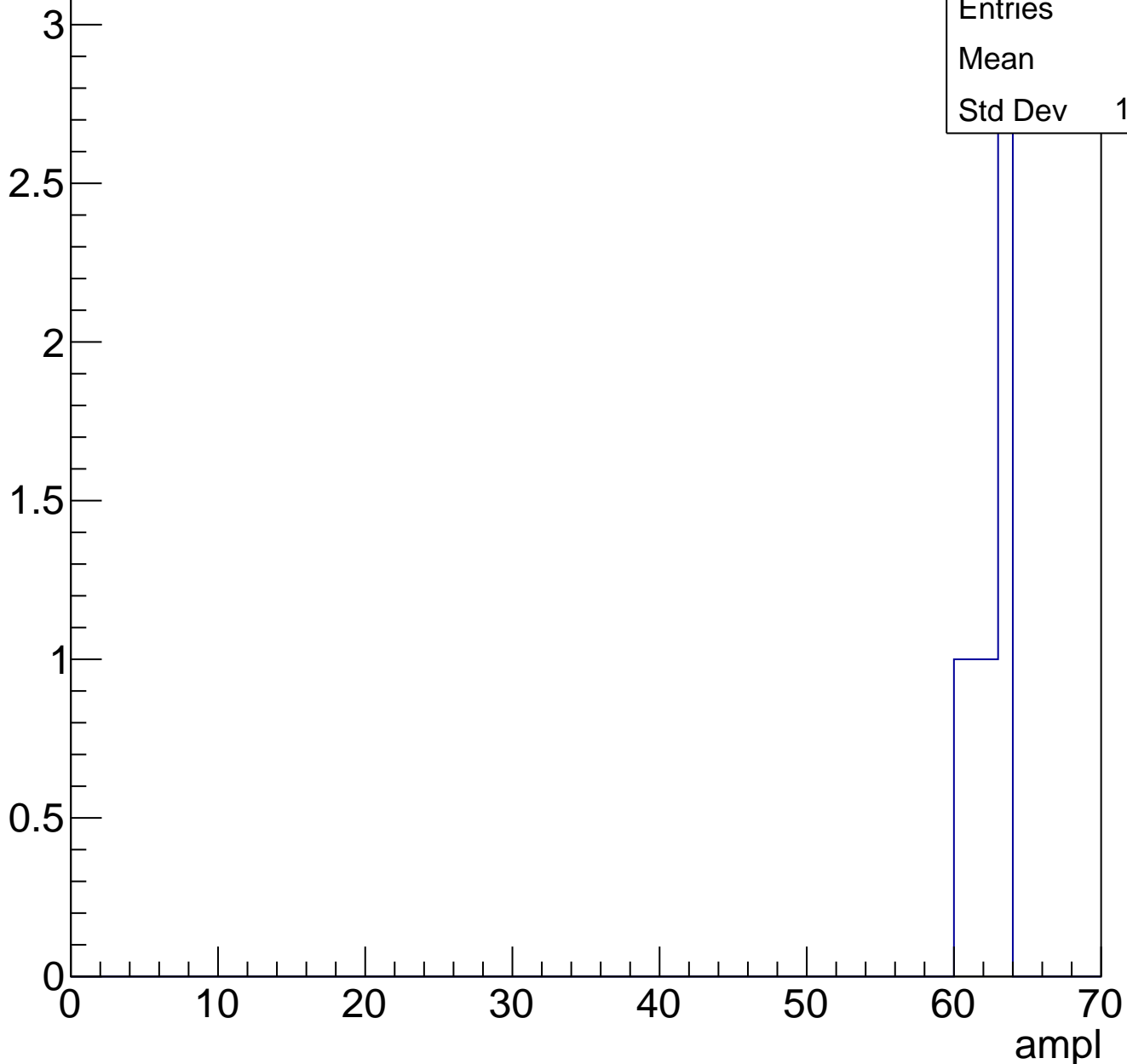
Entry



# B1L003S, U11-ch79, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch79, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U11-ch80, adc0

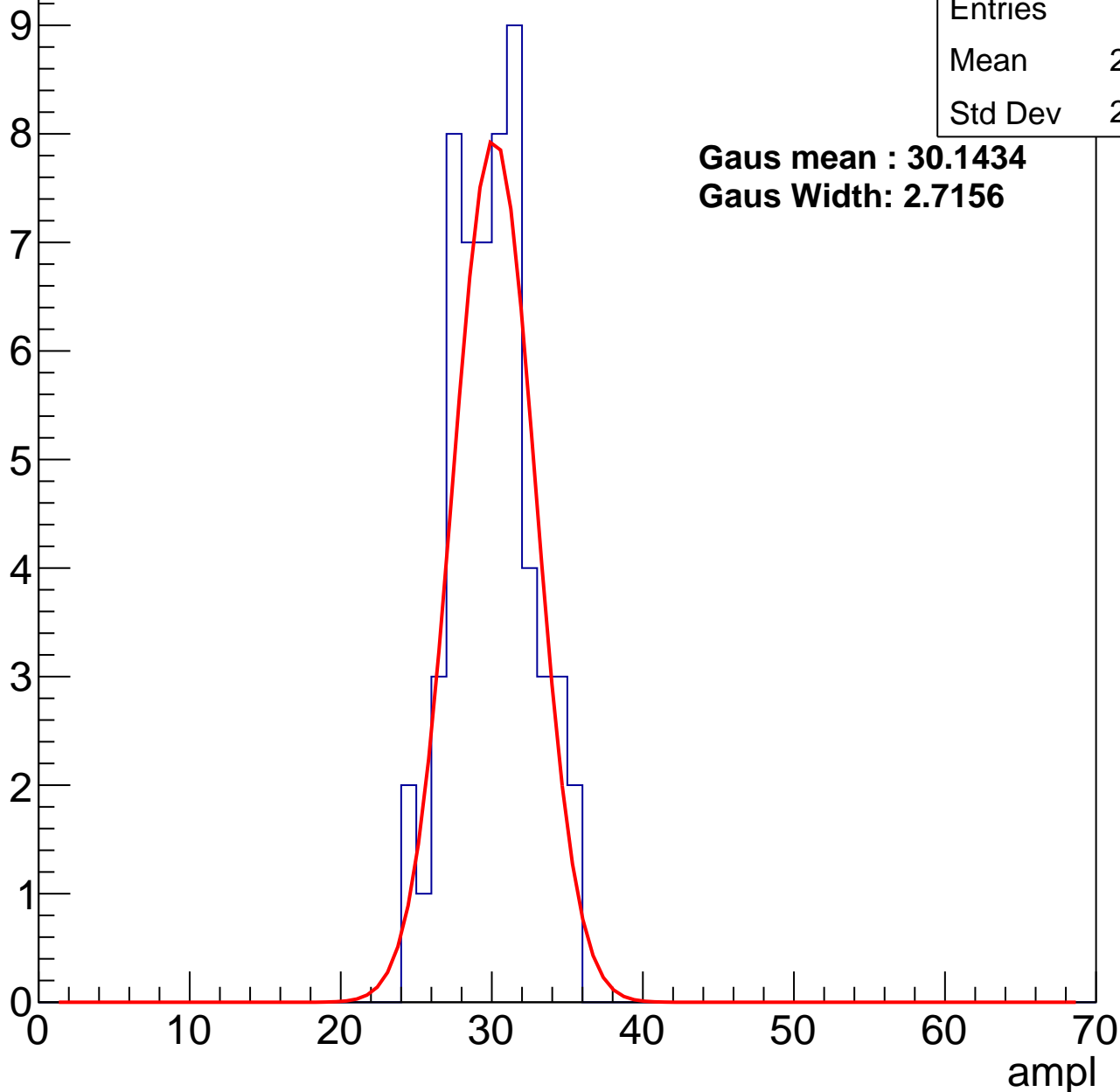
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	29.54
Std Dev	2.616

**Gaus mean : 30.1434**

**Gaus Width: 2.7156**



# B1L003S, U11-ch80, adc1

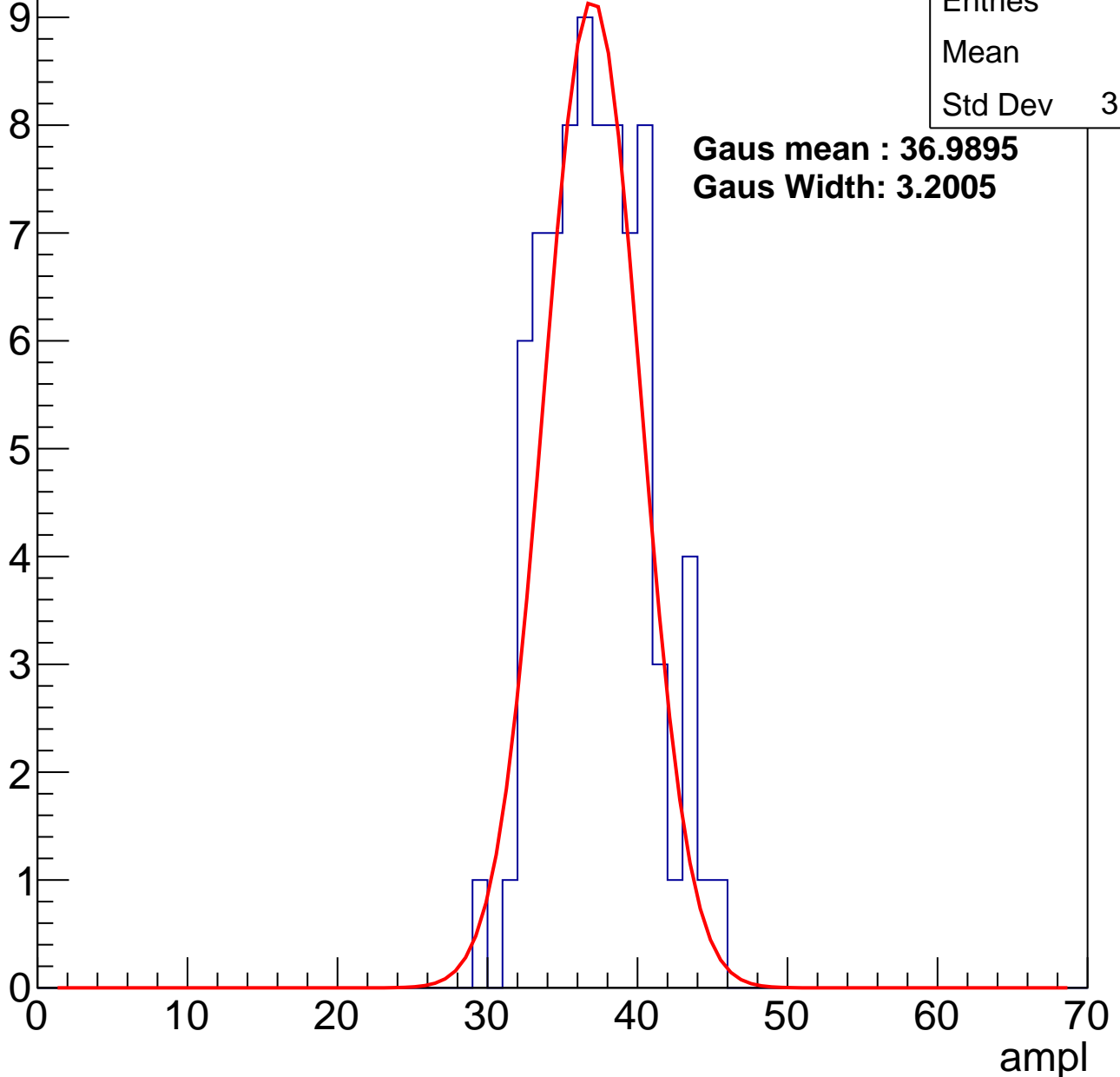
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	80
Mean	36.8
Std Dev	3.356

**Gaus mean : 36.9895**

**Gaus Width: 3.2005**



# B1L003S, U11-ch80, adc2

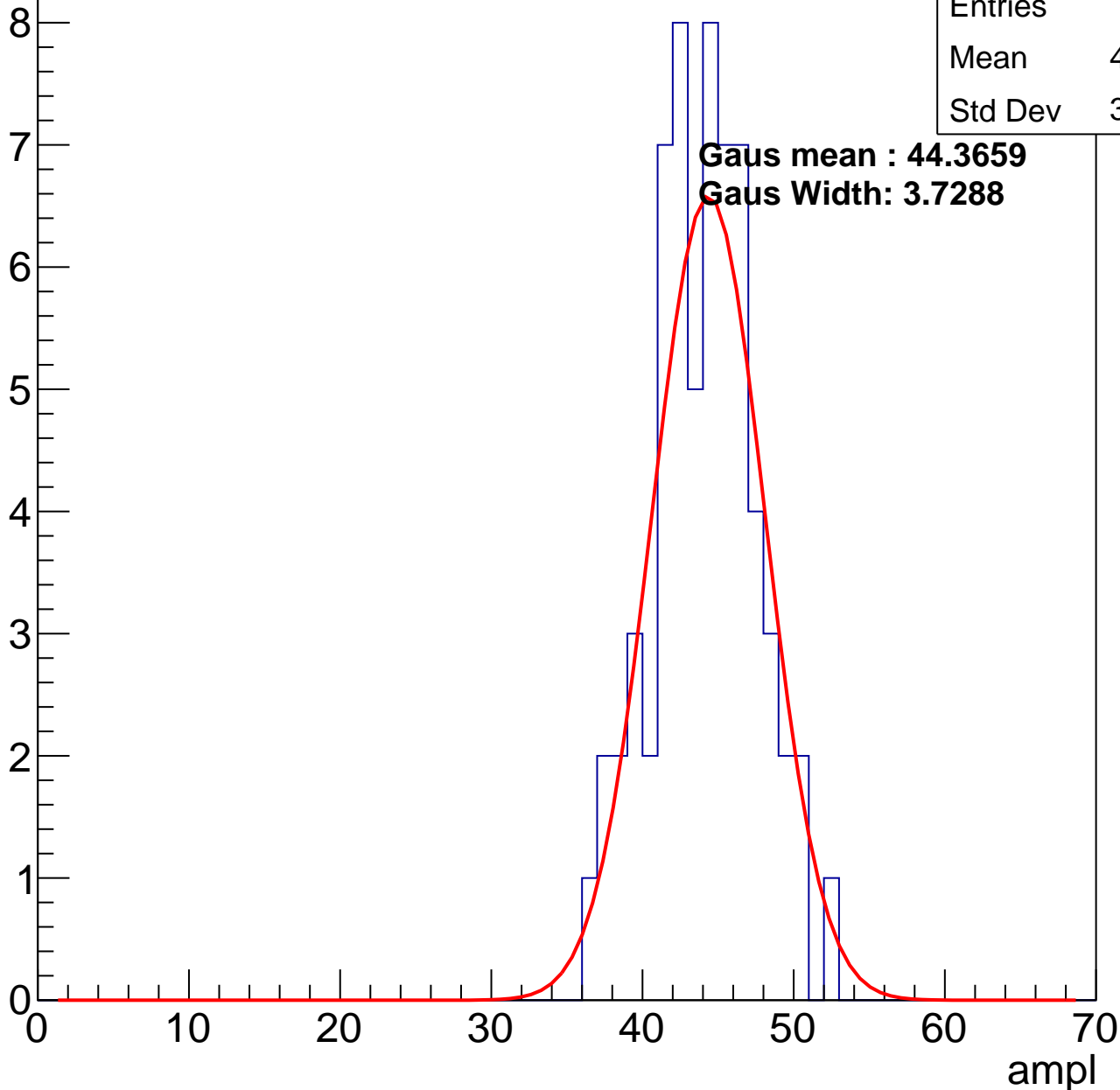
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	43.62
Std Dev	3.393

**Gaus mean : 44.3659**

**Gaus Width: 3.7288**

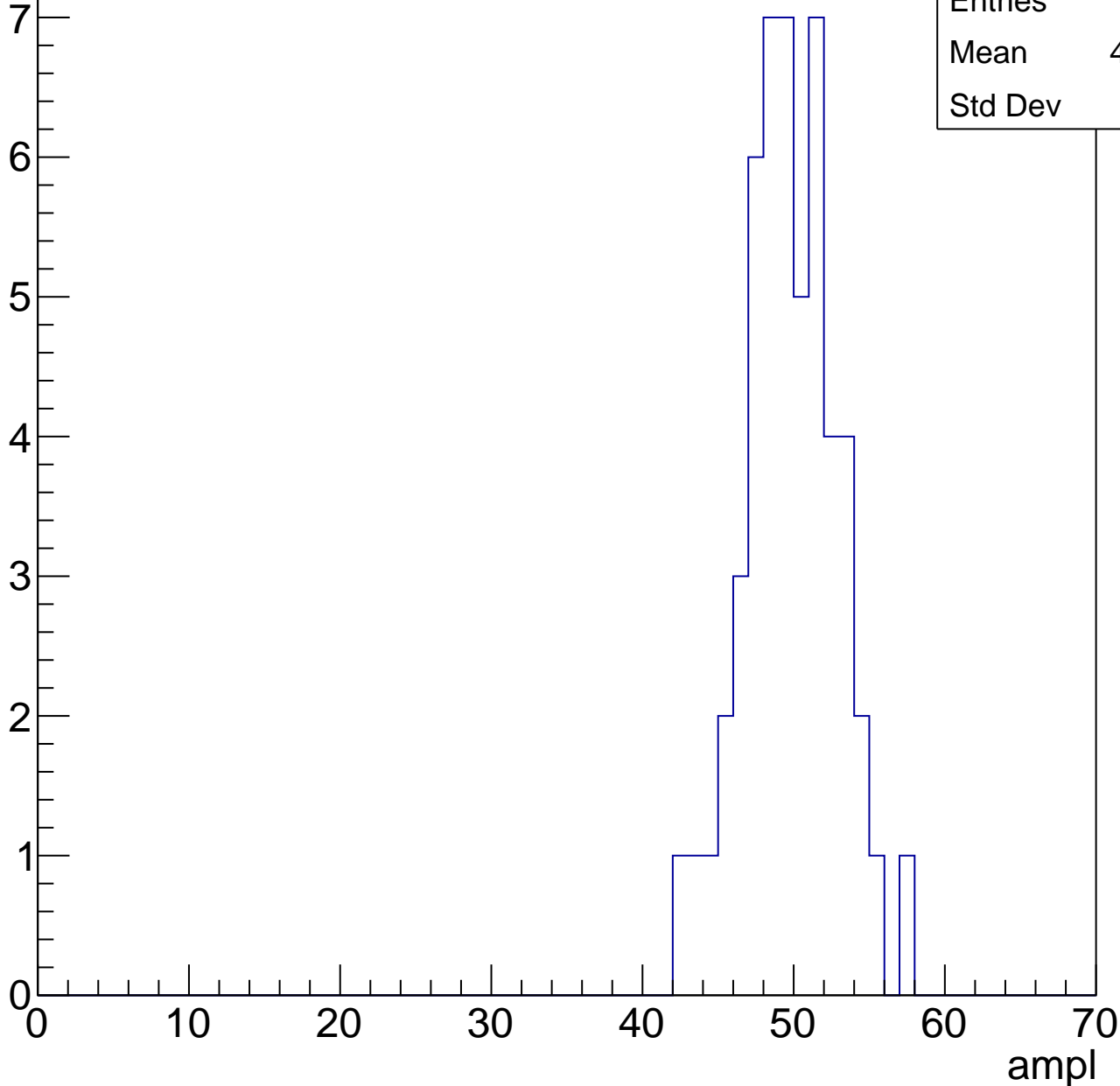


# B1L003S, U11-ch80, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	52
Mean	49.33
Std Dev	3.03

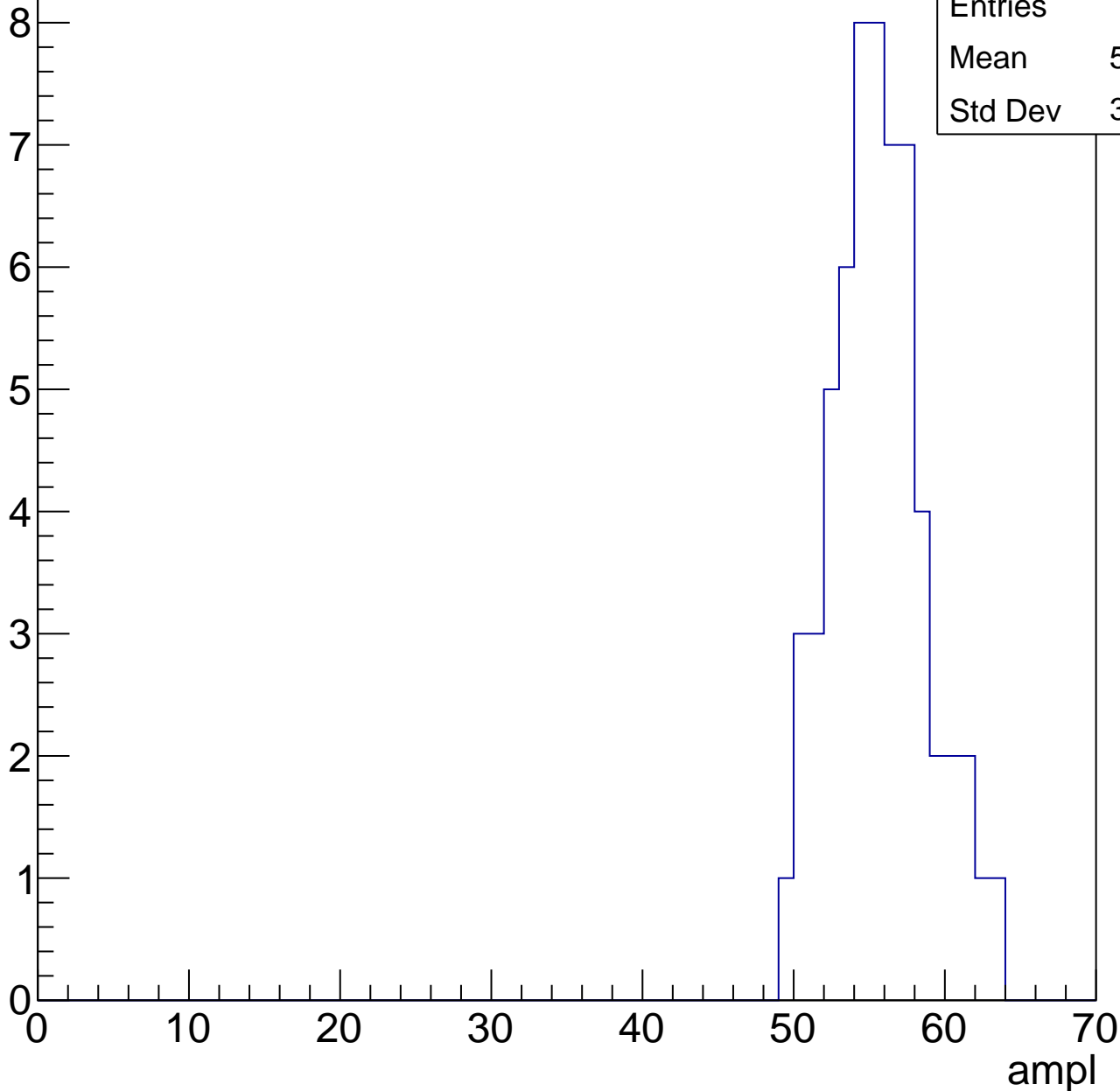


# B1L003S, U11-ch80, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

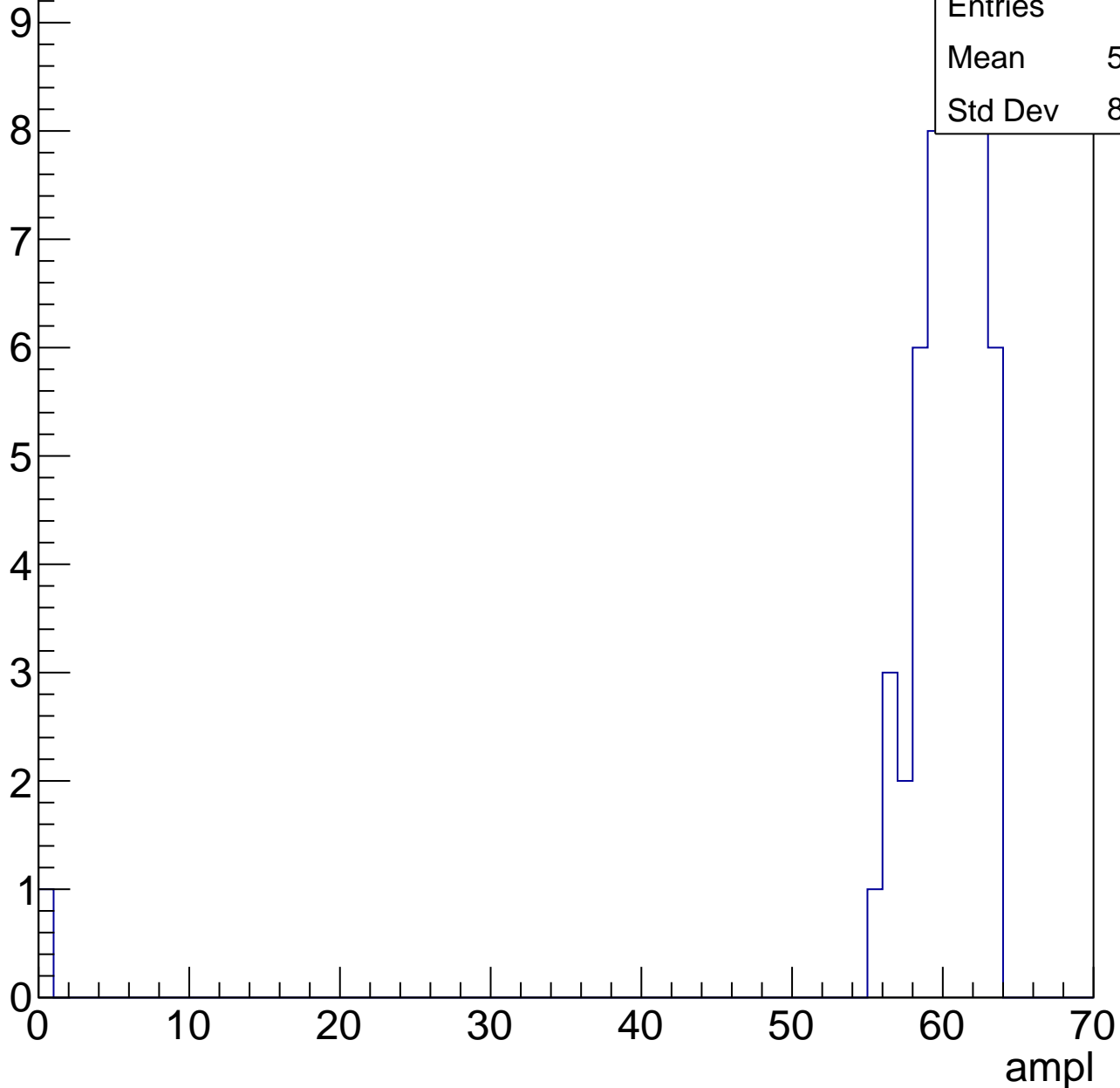
Entries	60
Mean	55.17
Std Dev	3.089



# B1L003S, U11-ch80, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U11-ch80, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

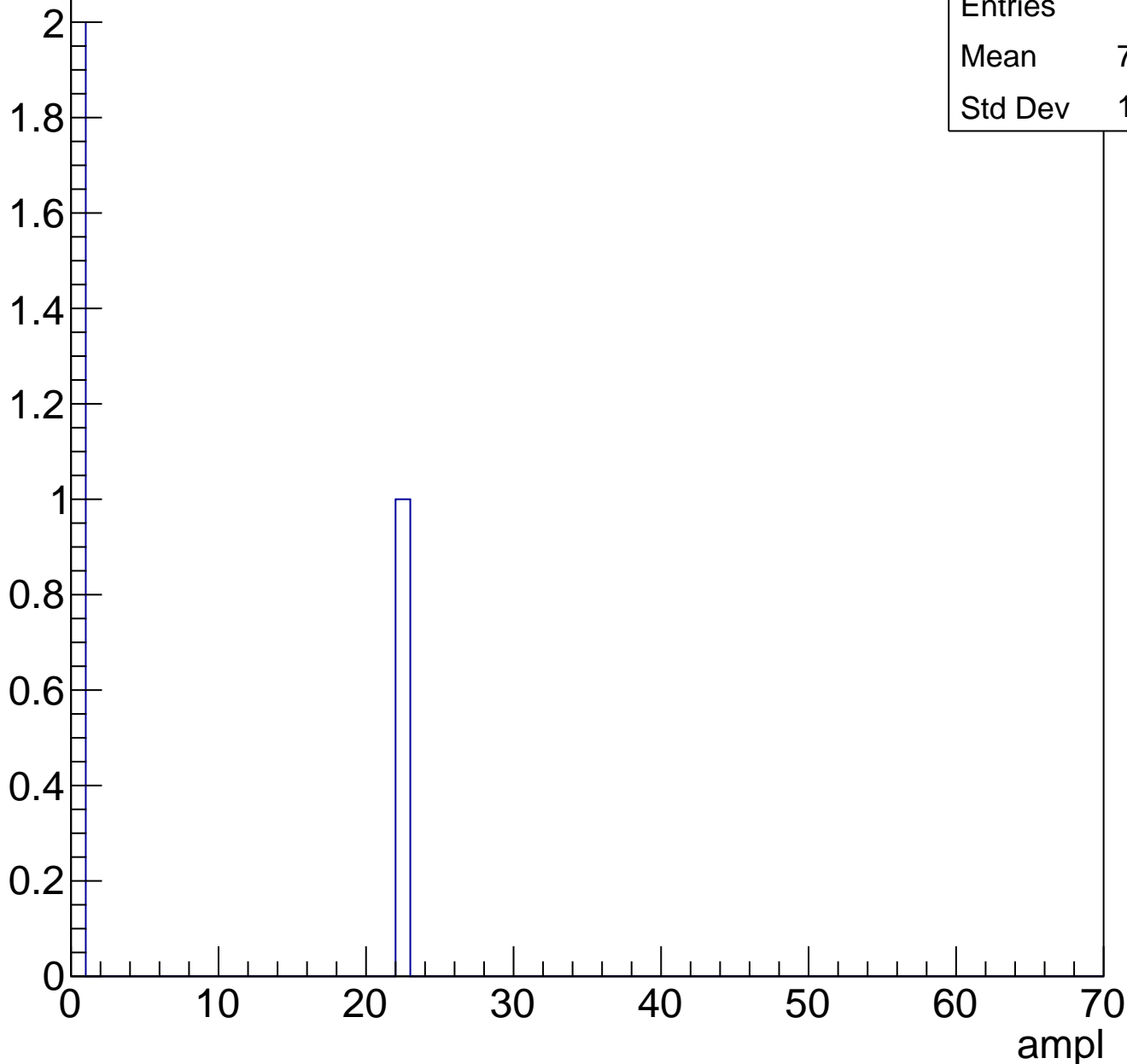




# B1L003S, U11-ch80, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U11-ch81, adc0

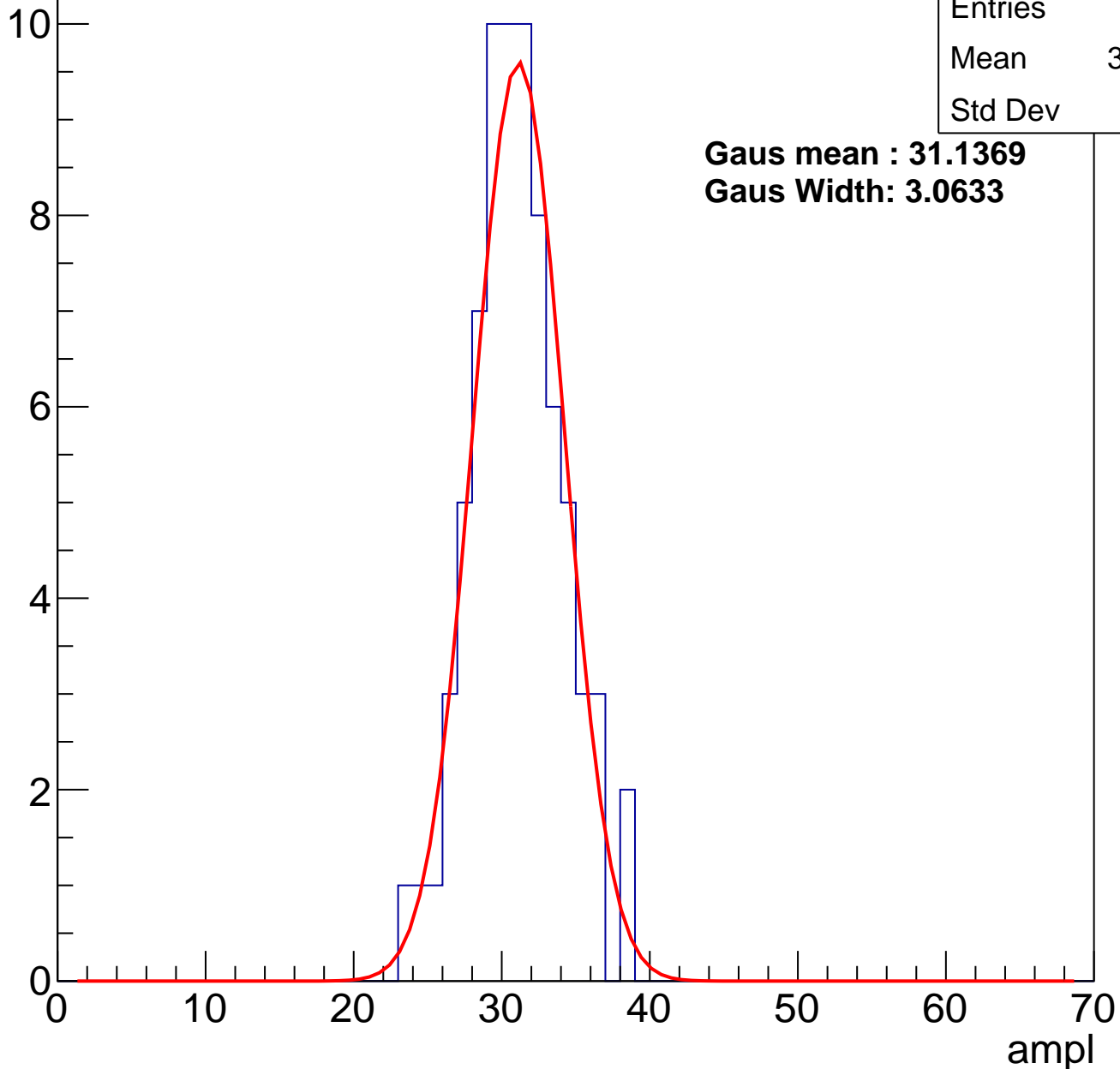
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	75
Mean	30.59
Std Dev	3.06

**Gaus mean : 31.1369**

**Gaus Width: 3.0633**

Entry



# B1L003S, U11-ch81, adc1

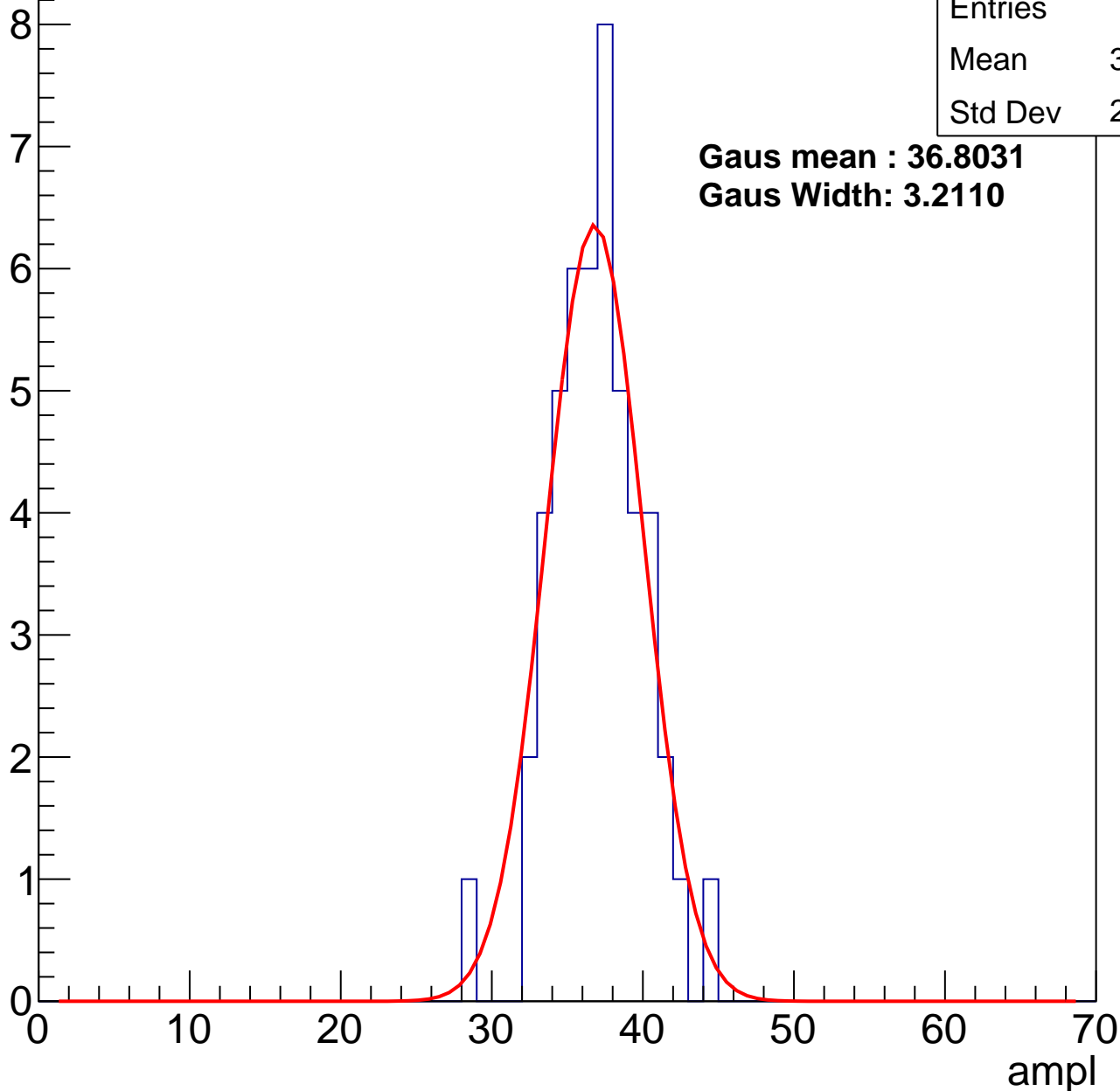
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	49
Mean	36.53
Std Dev	2.935

**Gaus mean : 36.8031**

**Gaus Width: 3.2110**



# B1L003S, U11-ch81, adc2

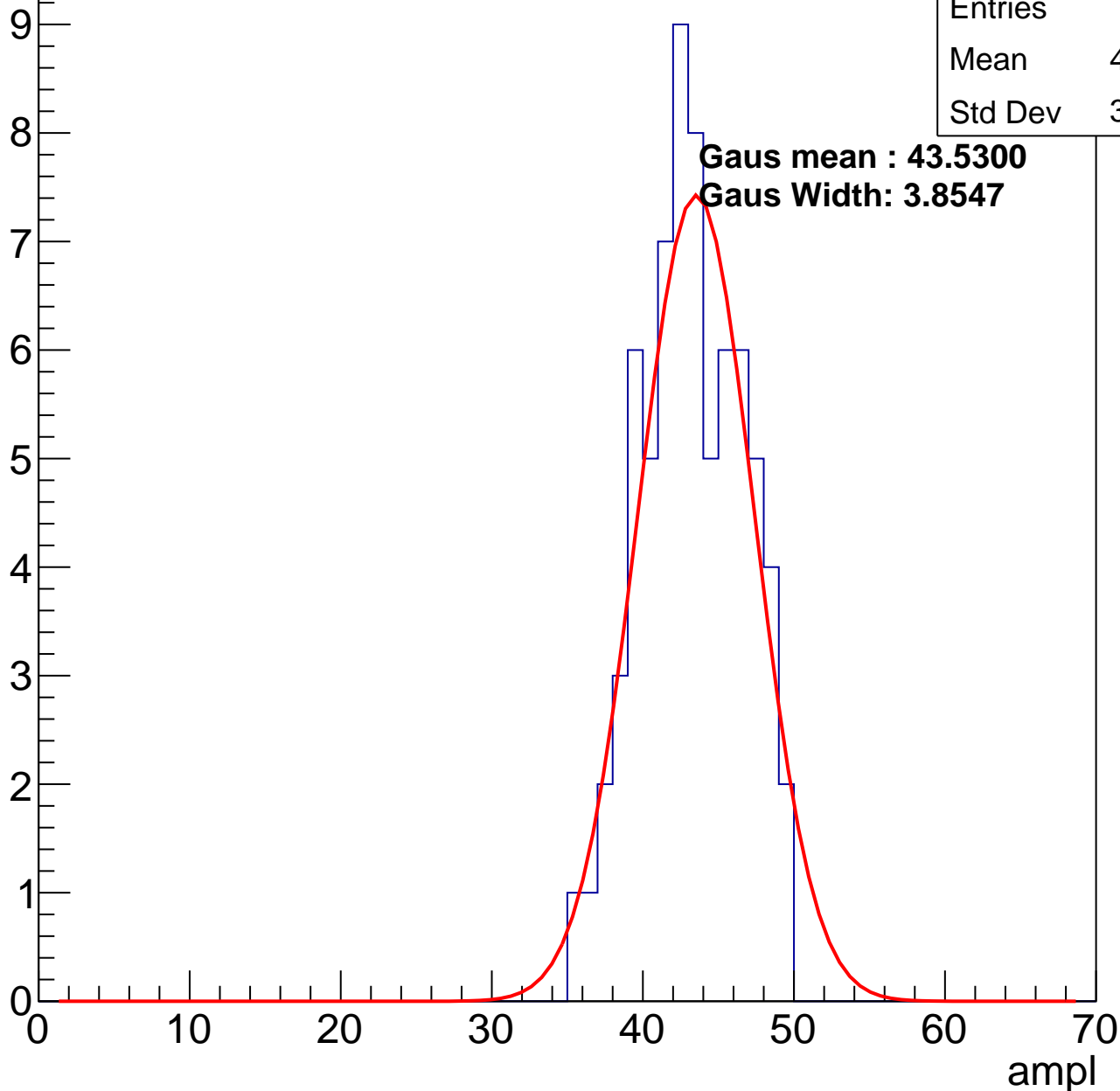
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	42.76
Std Dev	3.314

**Gaus mean : 43.5300**

**Gaus Width: 3.8547**

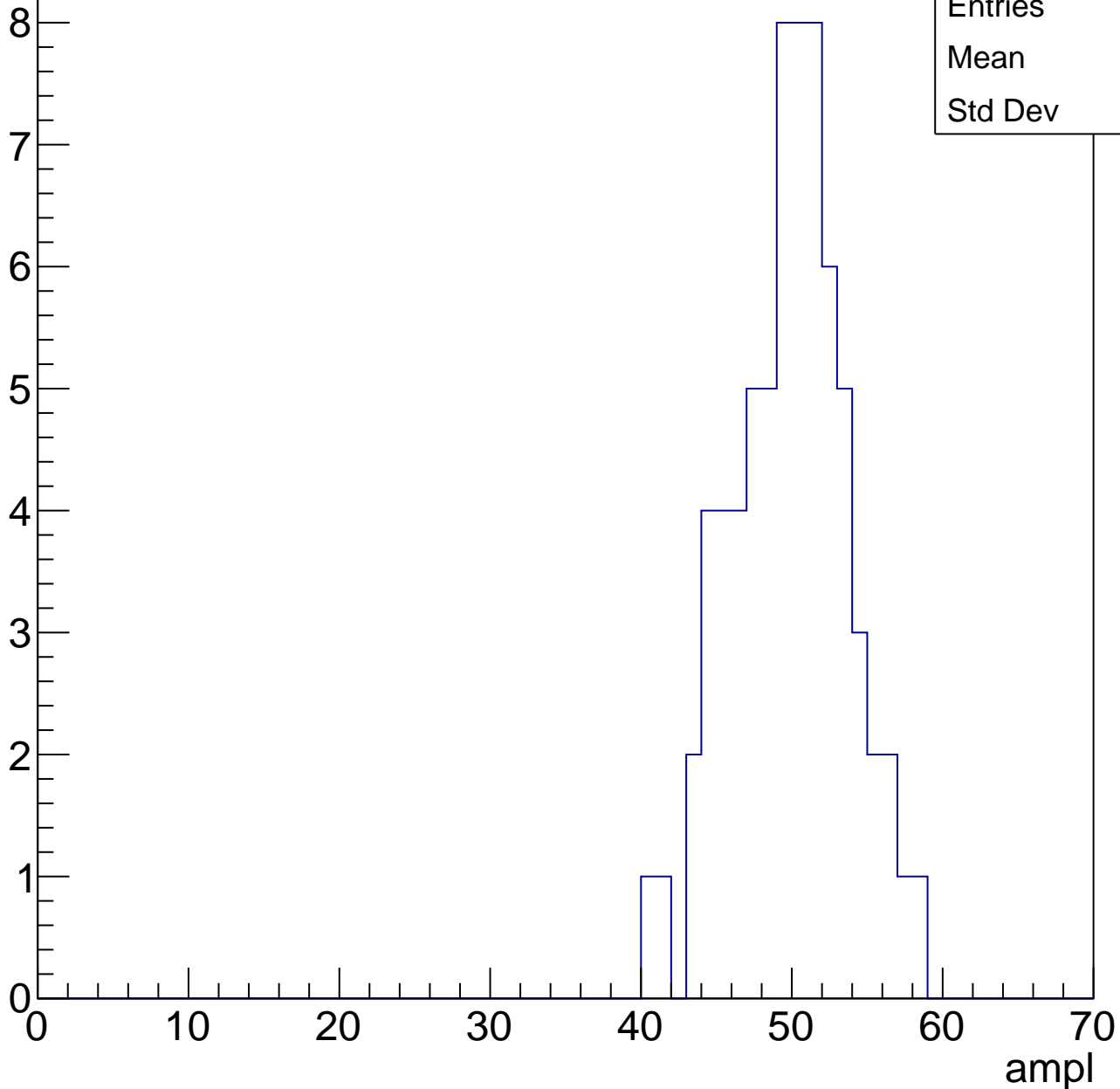


# B1L003S, U11-ch81, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	49.4
Std Dev	3.77

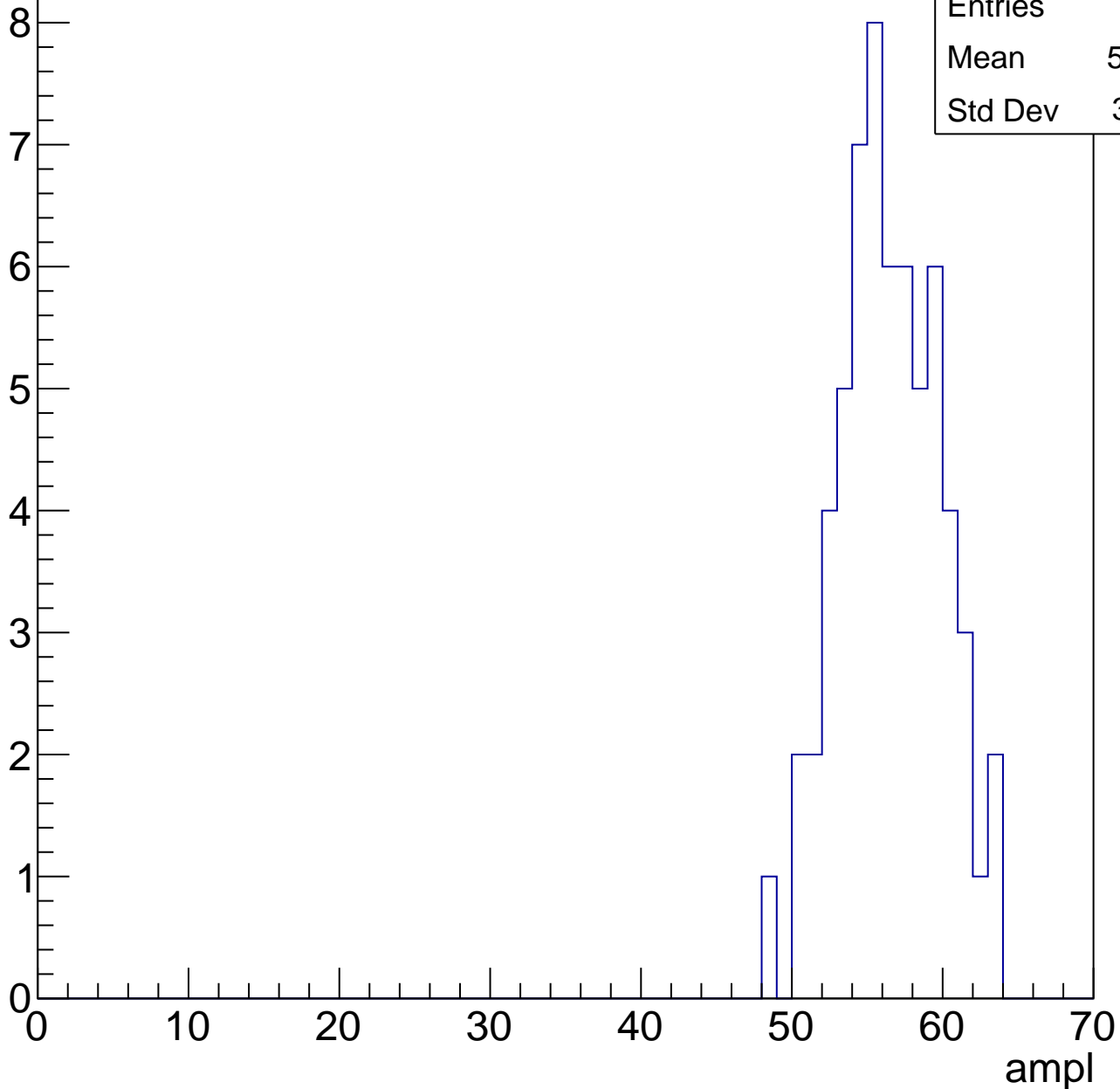


# B1L003S, U11-ch81, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	56.03
Std Dev	3.321

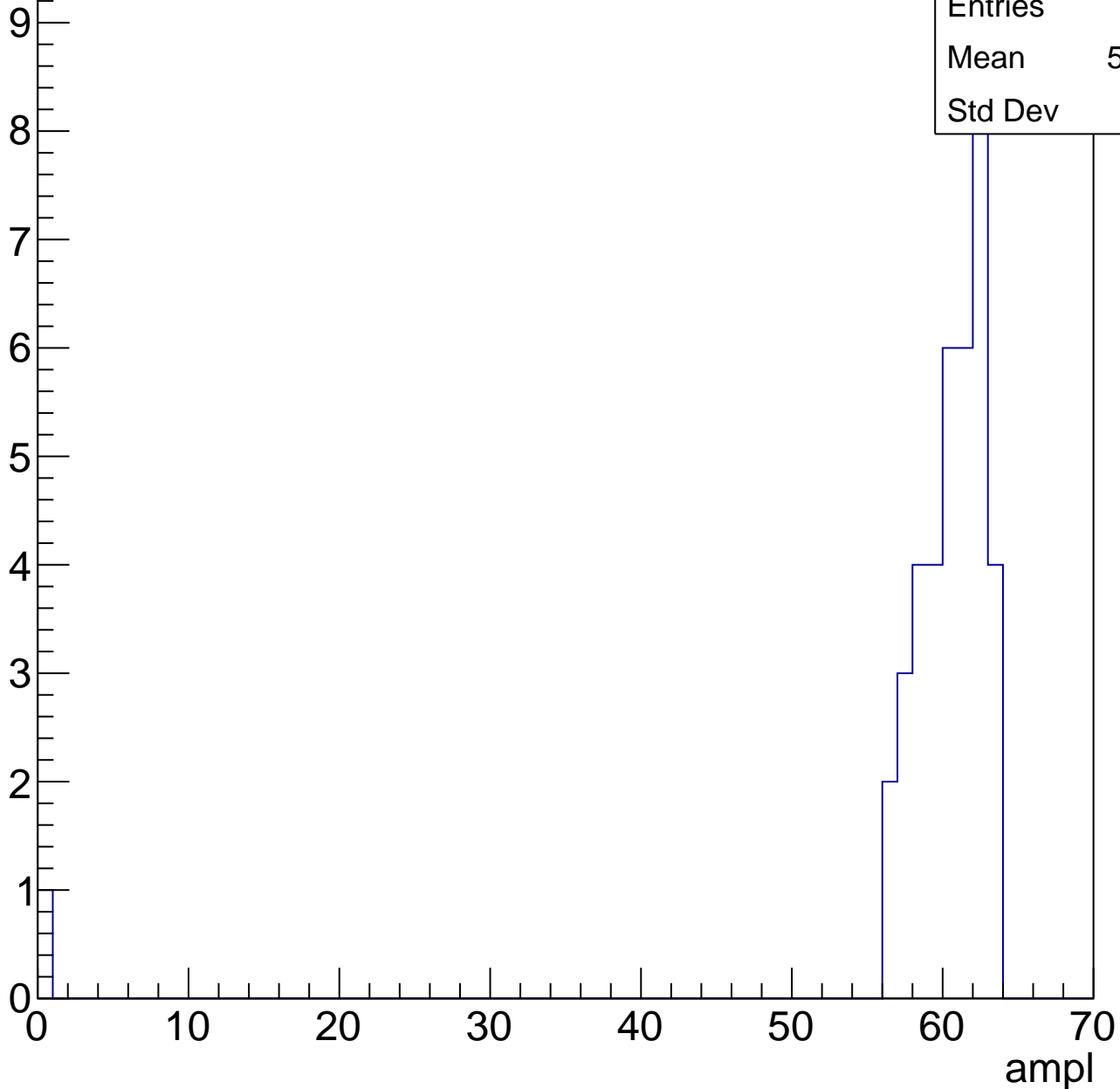


# B1L003S, U11-ch81, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

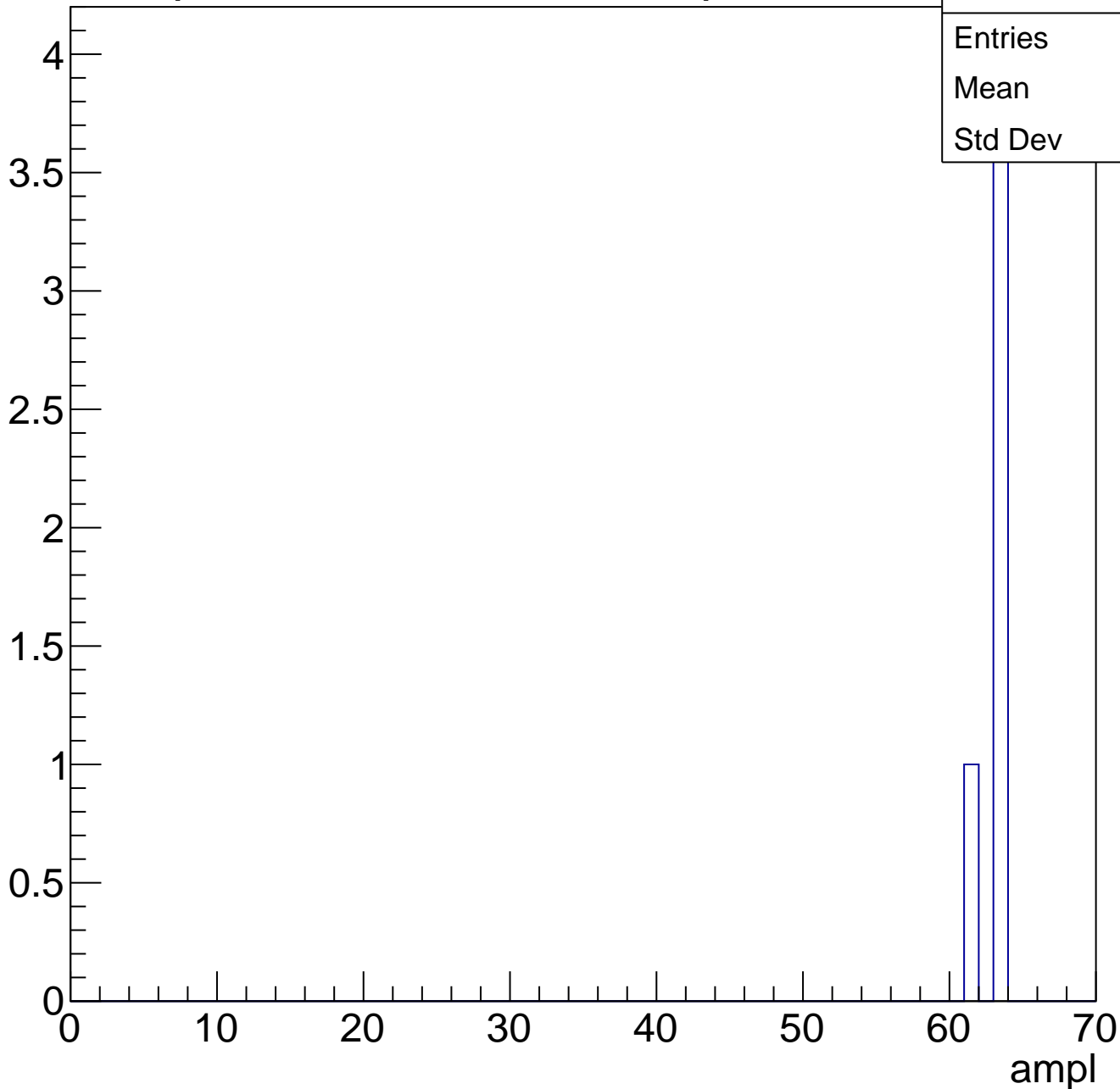
Entries	39
Mean	58.64
Std Dev	9.72



# B1L003S, U11-ch81, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch81, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U11-ch82, adc0

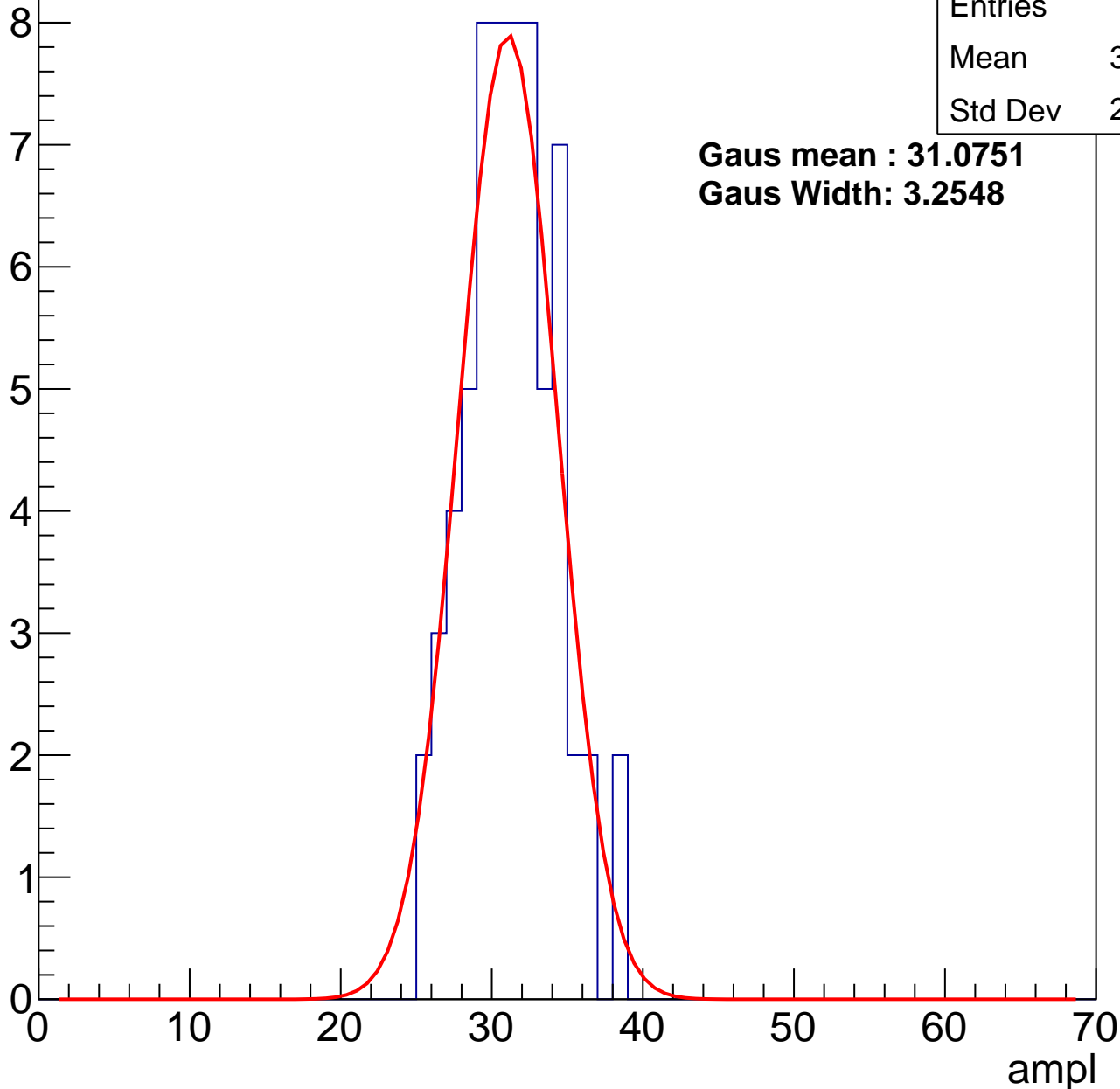
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	30.83
Std Dev	2.972

**Gaus mean : 31.0751**

**Gaus Width: 3.2548**



# B1L003S, U11-ch82, adc1

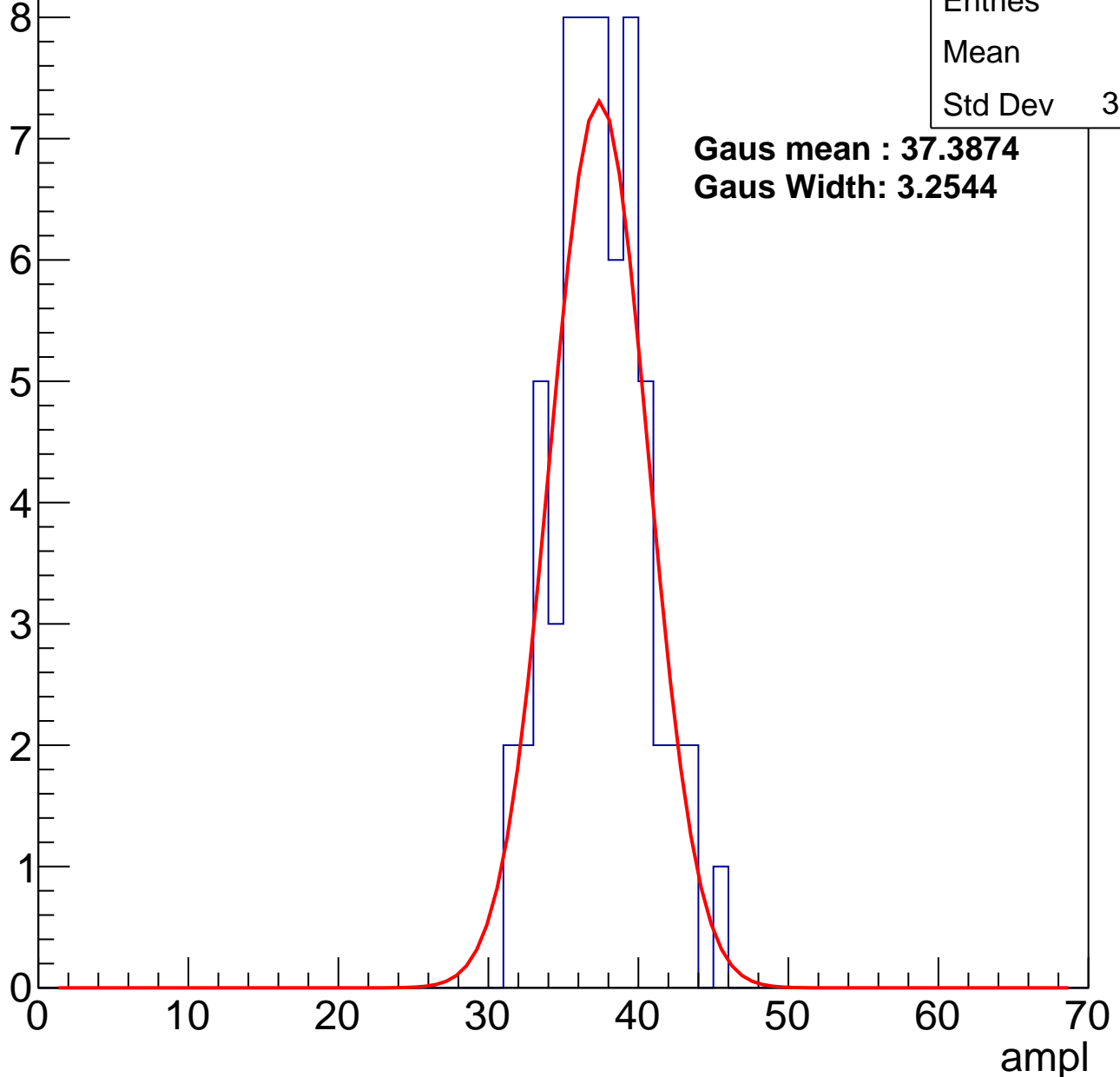
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	37
Std Dev	3.032

**Gaus mean : 37.3874**

**Gaus Width: 3.2544**



# B1L003S, U11-ch82, adc2

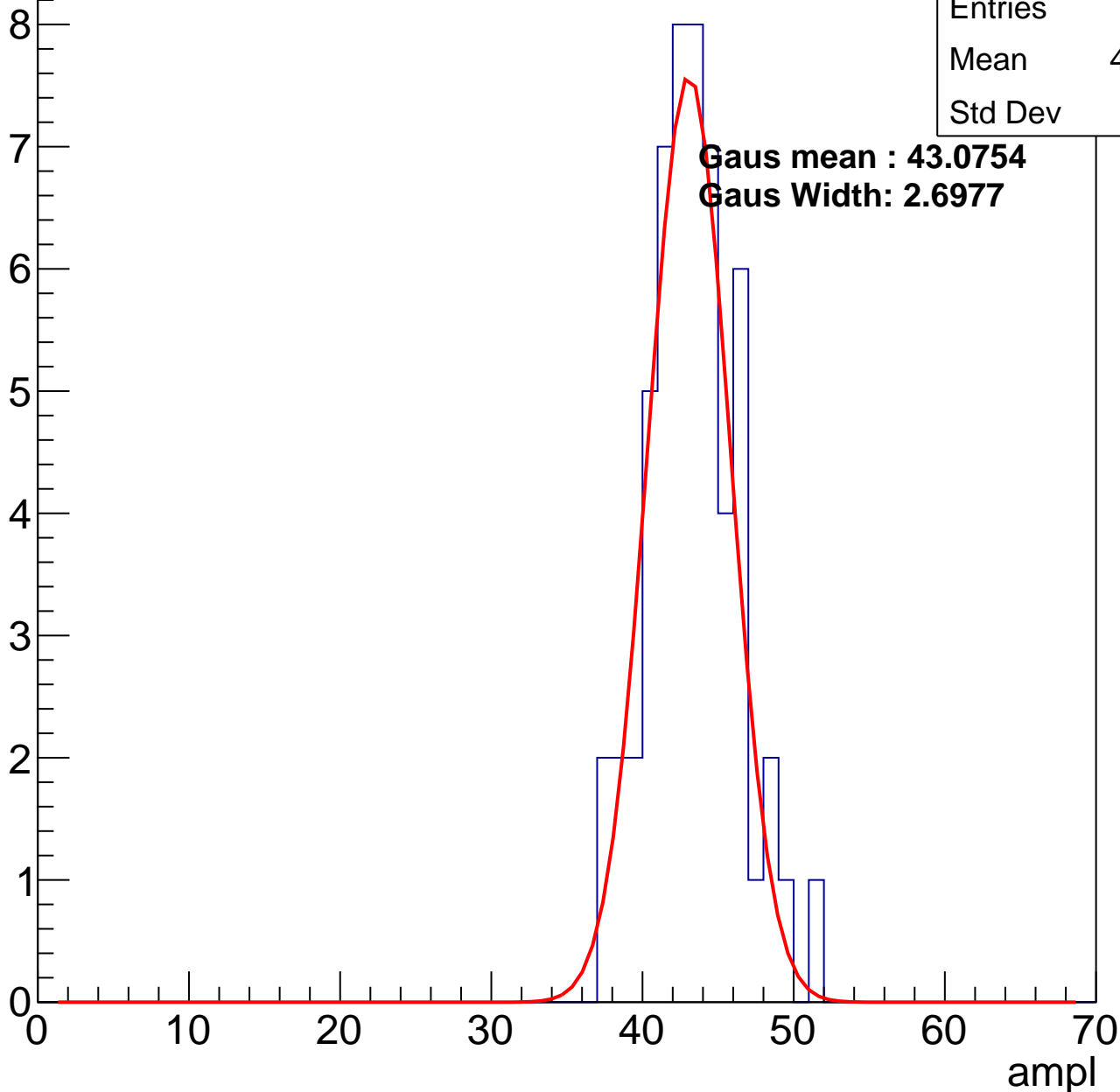
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	42.89
Std Dev	2.92

**Gaus mean : 43.0754**

**Gaus Width: 2.6977**

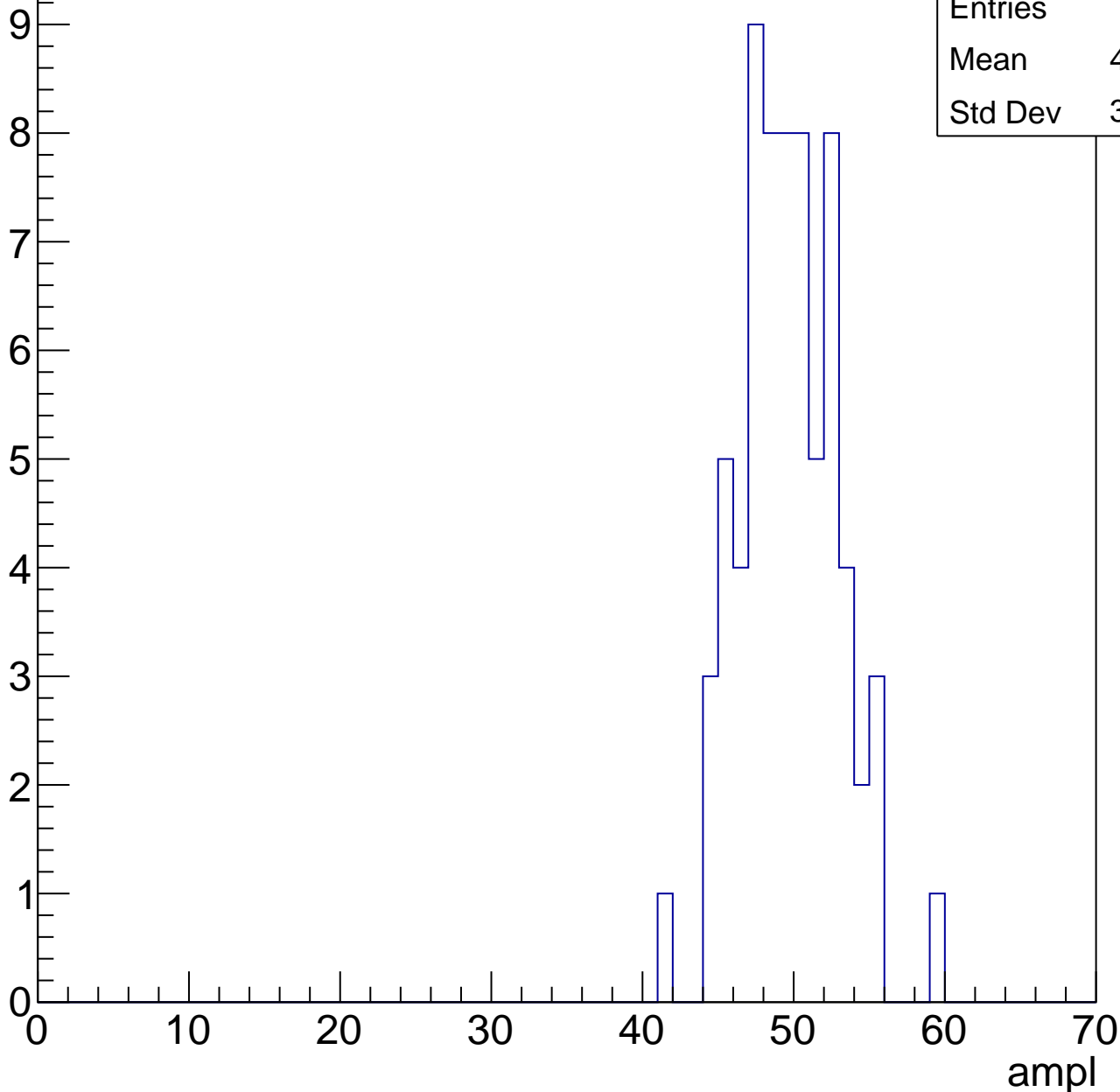


# B1L003S, U11-ch82, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	49.22
Std Dev	3.225

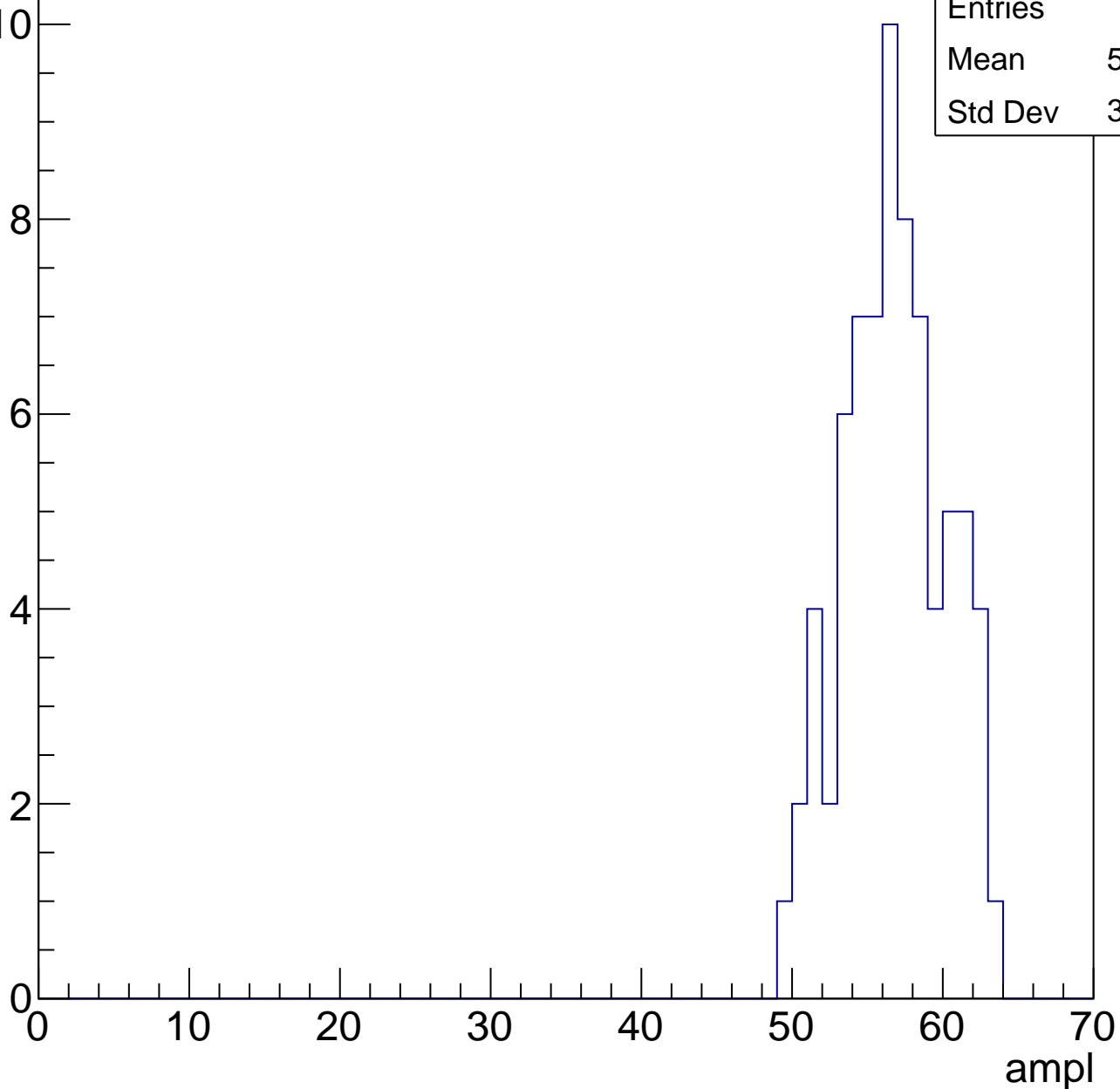


# B1L003S, U11-ch82, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	73
Mean	56.33
Std Dev	3.319

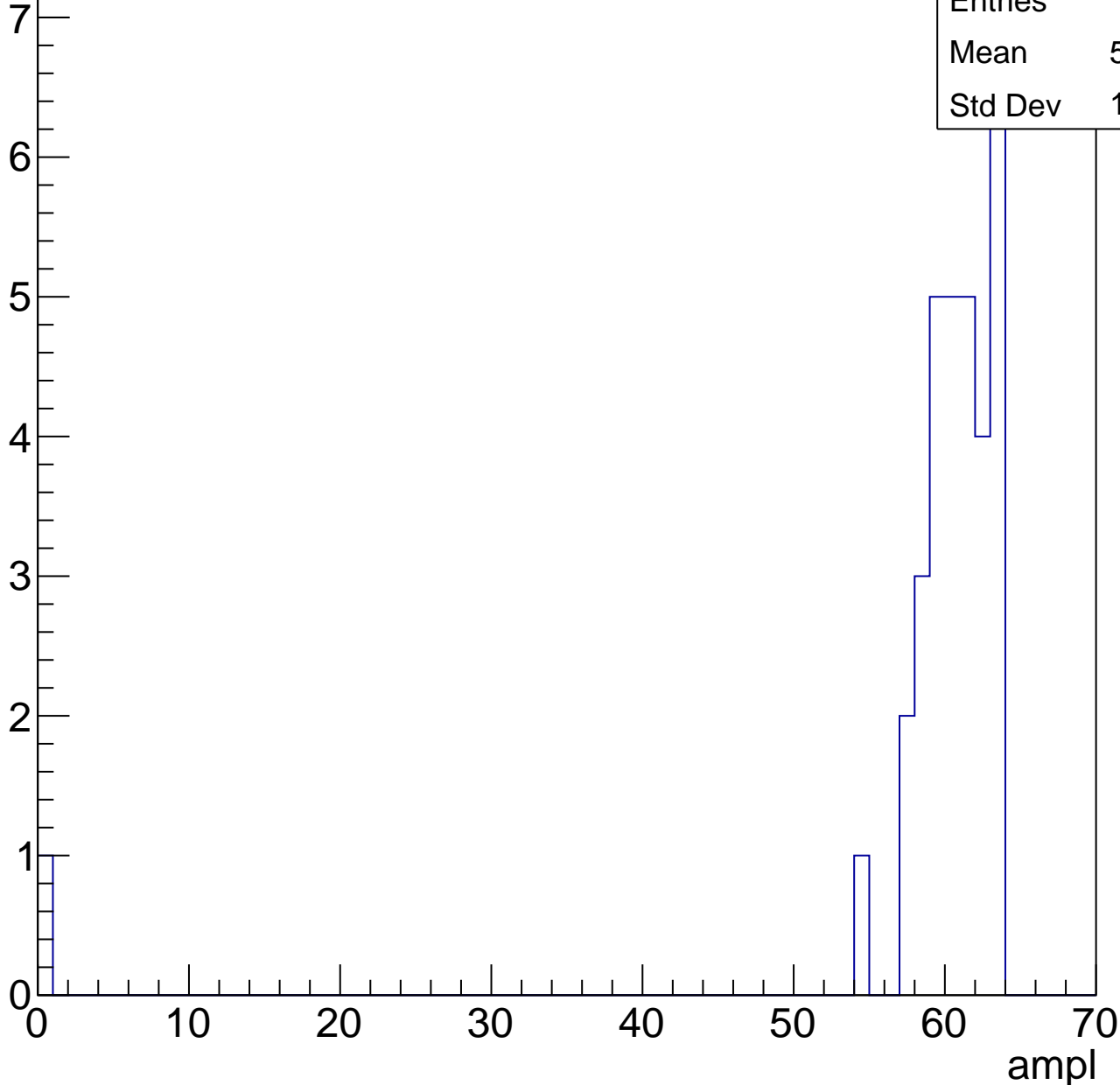


# B1L003S, U11-ch82, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	33
Mean	58.52
Std Dev	10.56



# B1L003S, U11-ch82, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch82, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U11-ch83, adc0

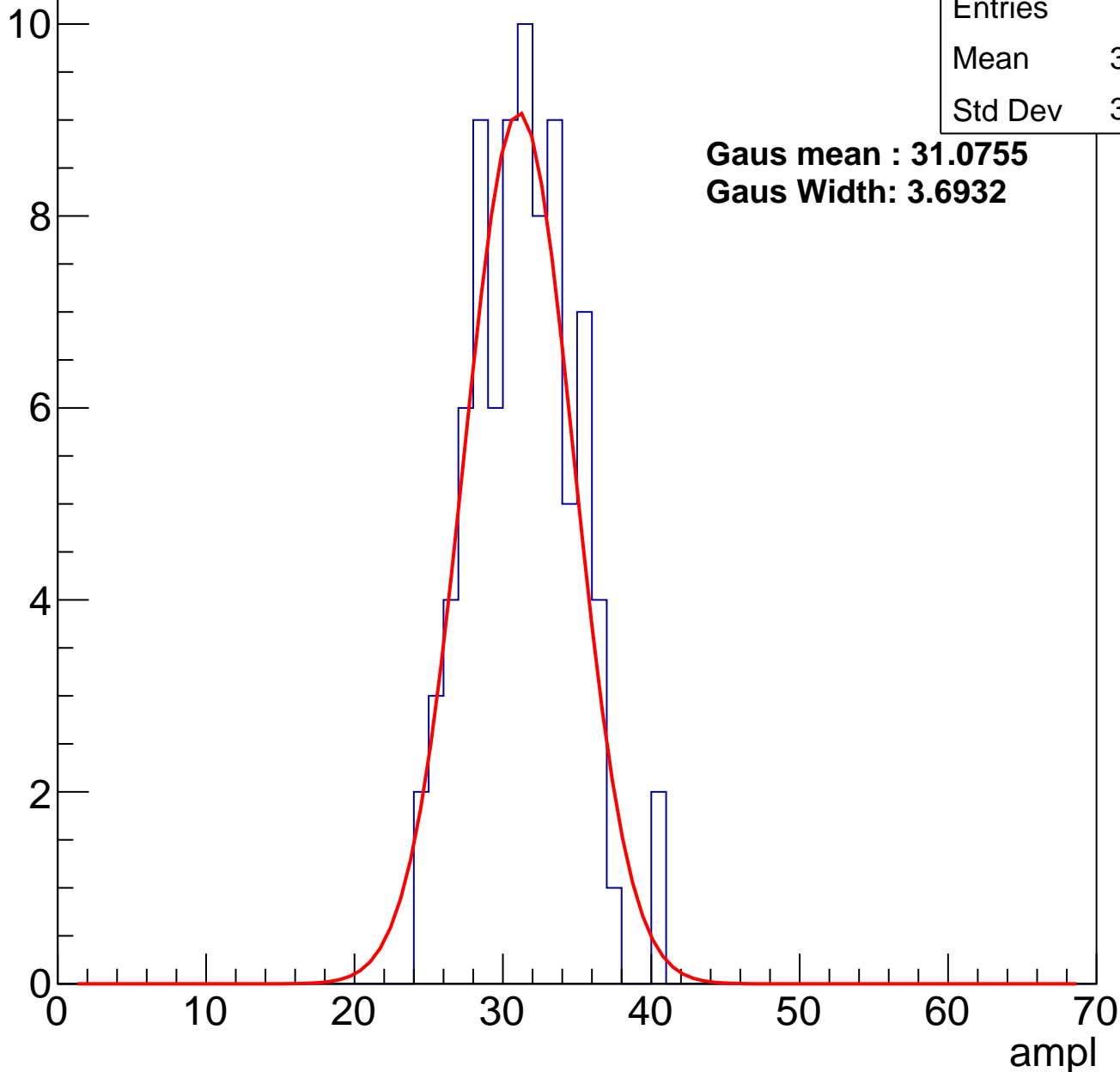
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	85
Mean	30.87
Std Dev	3.453

**Gaus mean : 31.0755**

**Gaus Width: 3.6932**

Entry



# B1L003S, U11-ch83, adc1

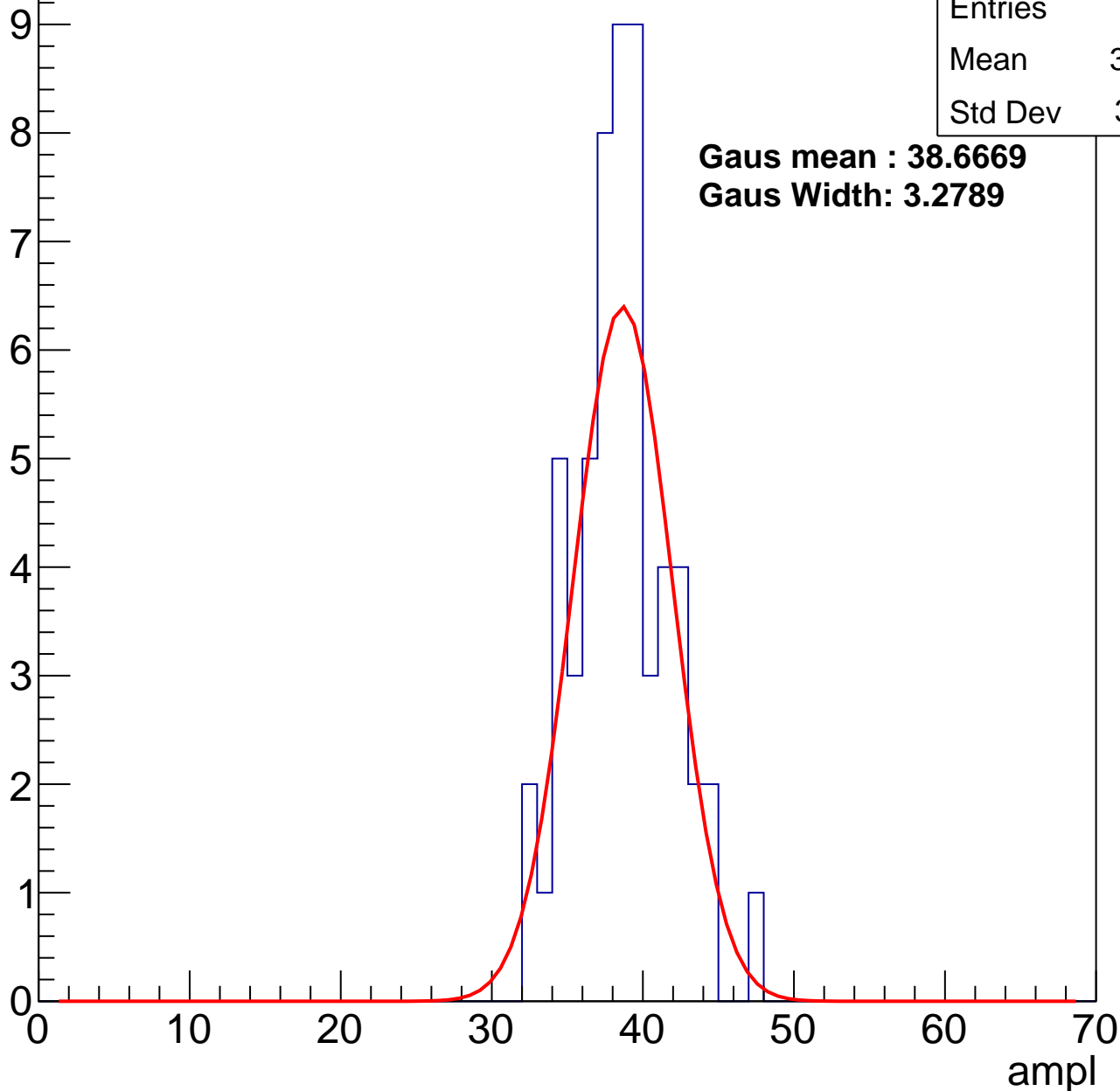
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	38.17
Std Dev	3.091

**Gaus mean : 38.6669**

**Gaus Width: 3.2789**



# B1L003S, U11-ch83, adc2

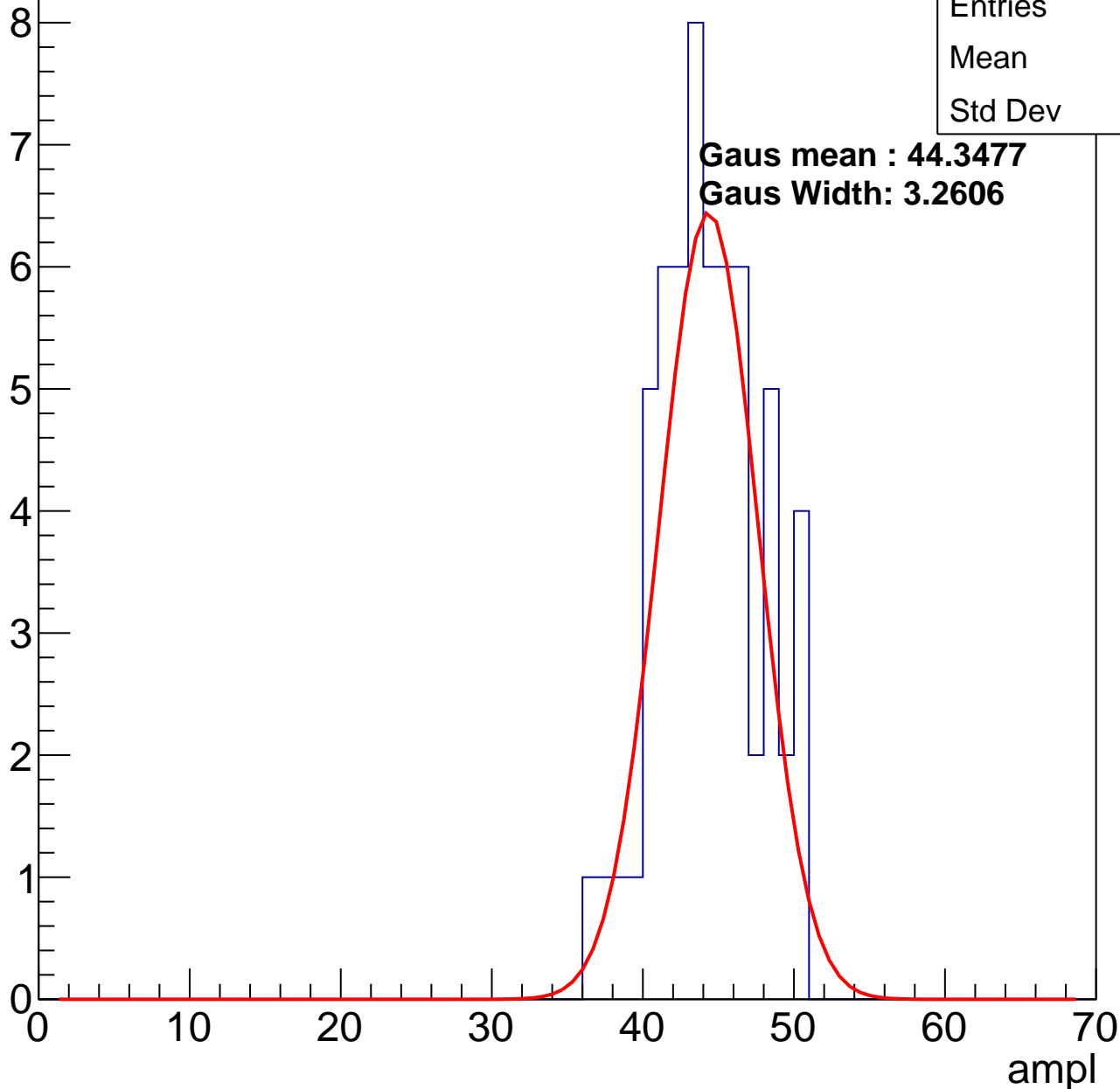
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	43.9
Std Dev	3.32

**Gaus mean : 44.3477**

**Gaus Width: 3.2606**

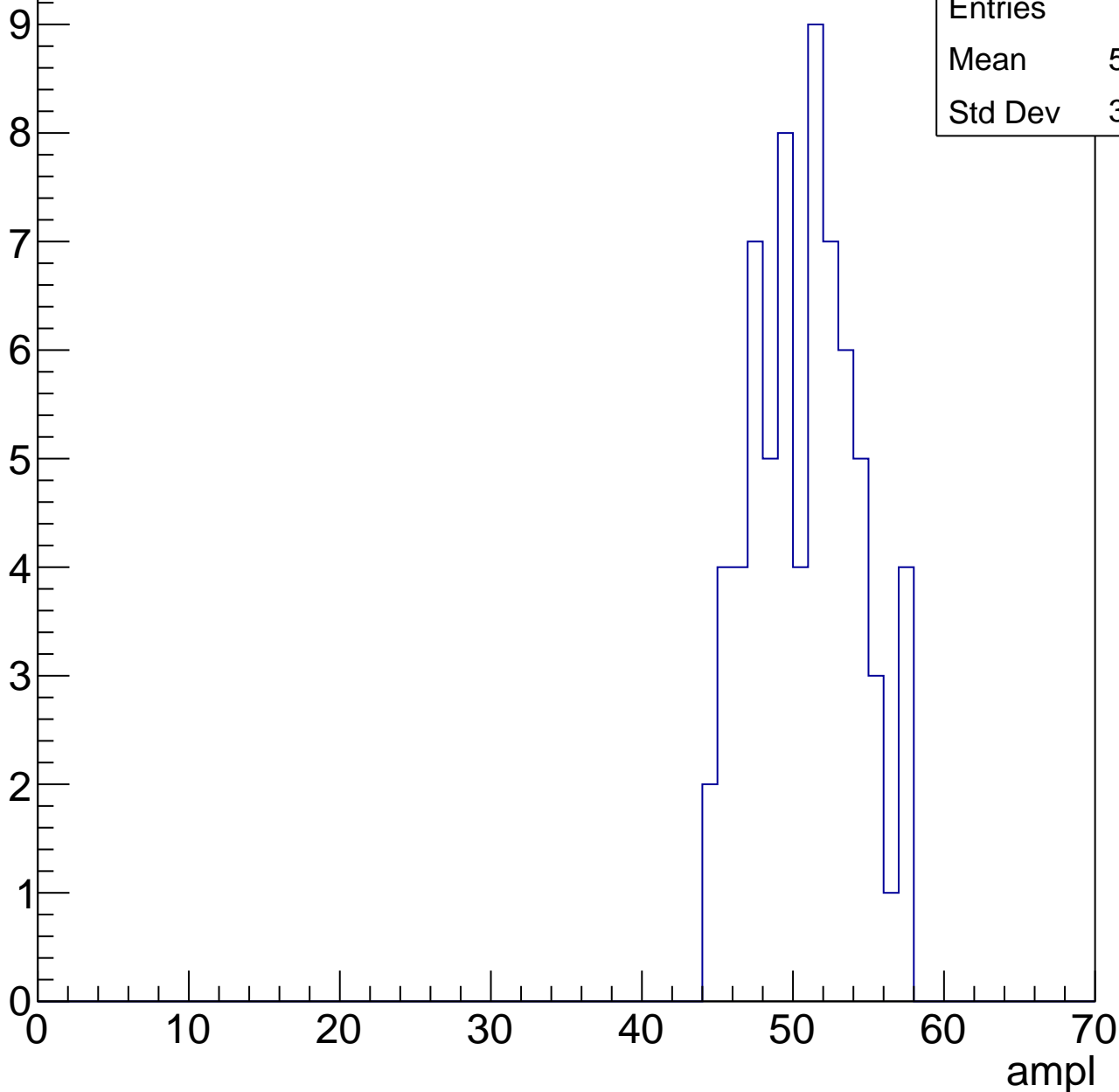


# B1L003S, U11-ch83, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	50.33
Std Dev	3.399

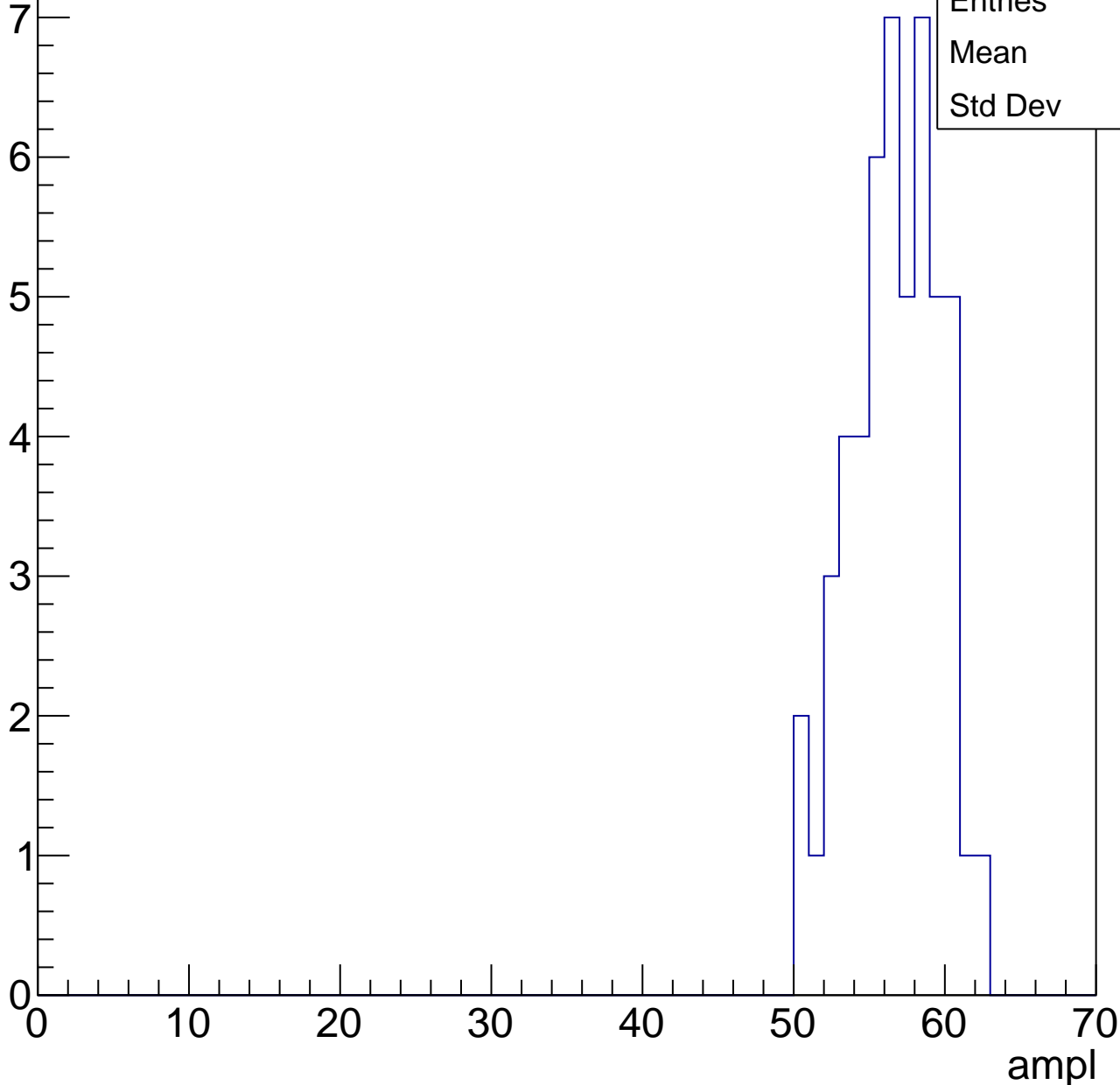


# B1L003S, U11-ch83, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	51
Mean	56.2
Std Dev	2.87

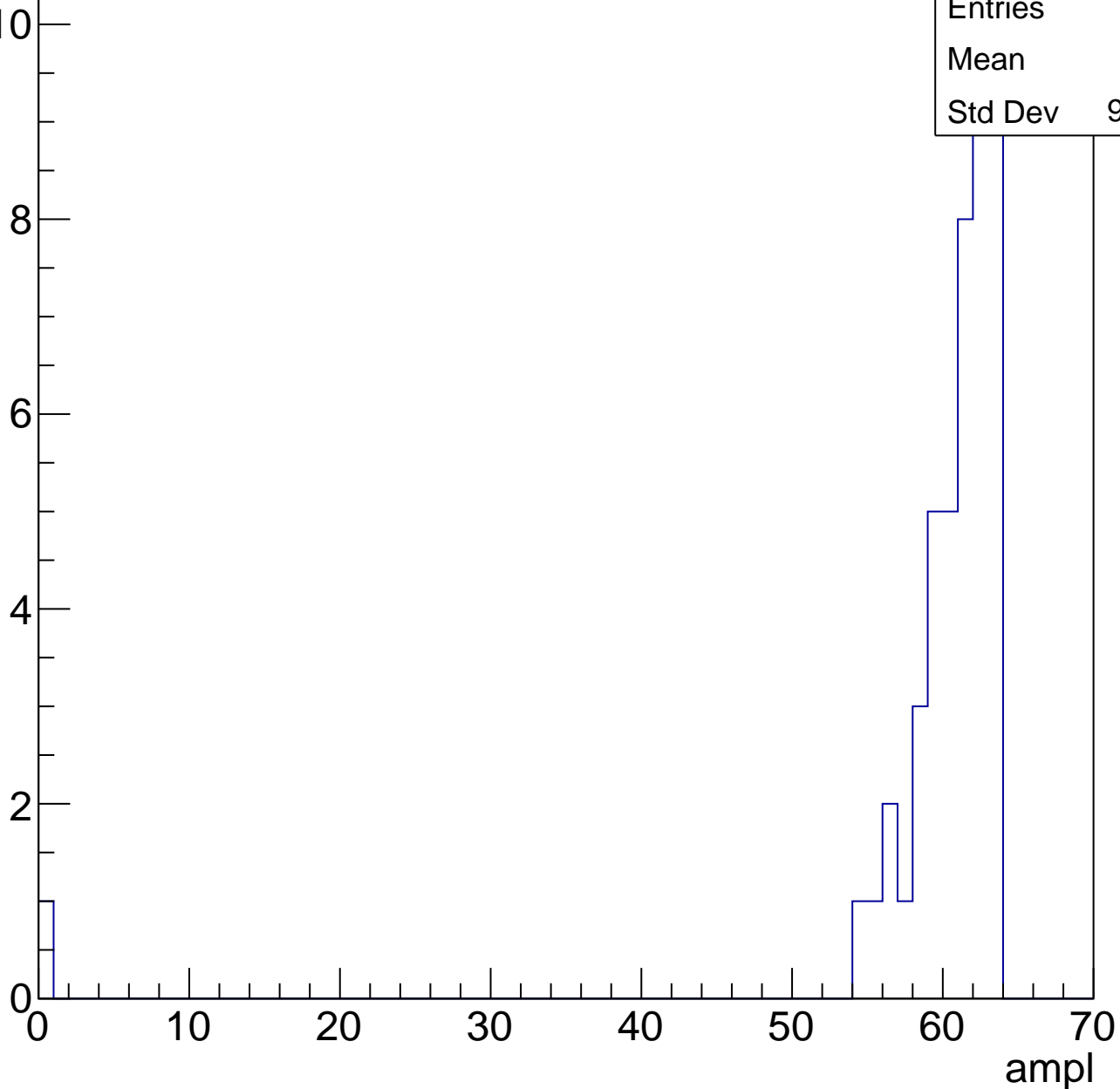


# B1L003S, U11-ch83, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	46
Mean	59.2
Std Dev	9.117



# B1L003S, U11-ch83, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	61
Std Dev	0



# B1L003S, U11-ch83, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U11-ch84, adc0

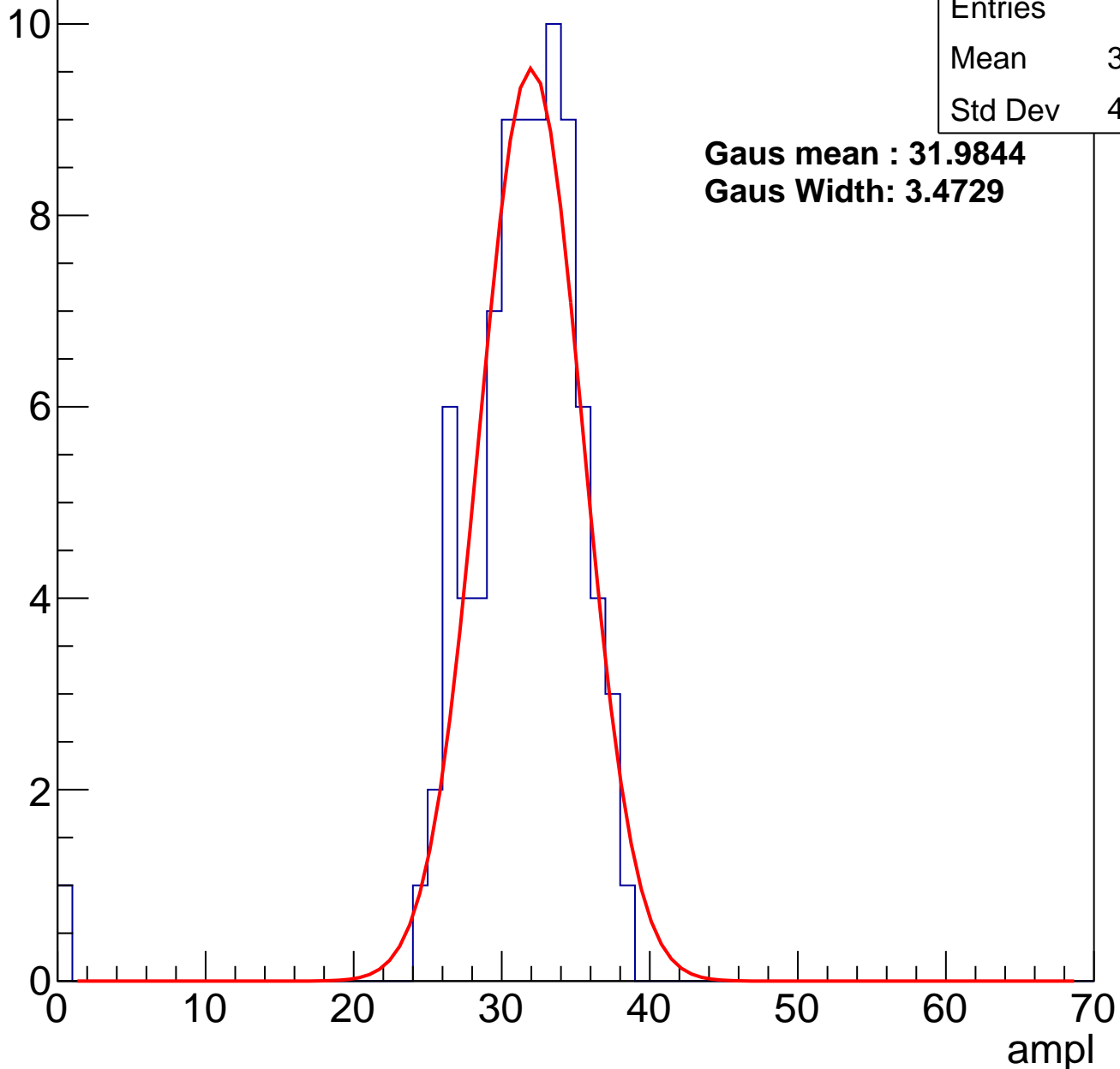
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	85
Mean	30.93
Std Dev	4.667

**Gaus mean : 31.9844**

**Gaus Width: 3.4729**

Entry



# B1L003S, U11-ch84, adc1

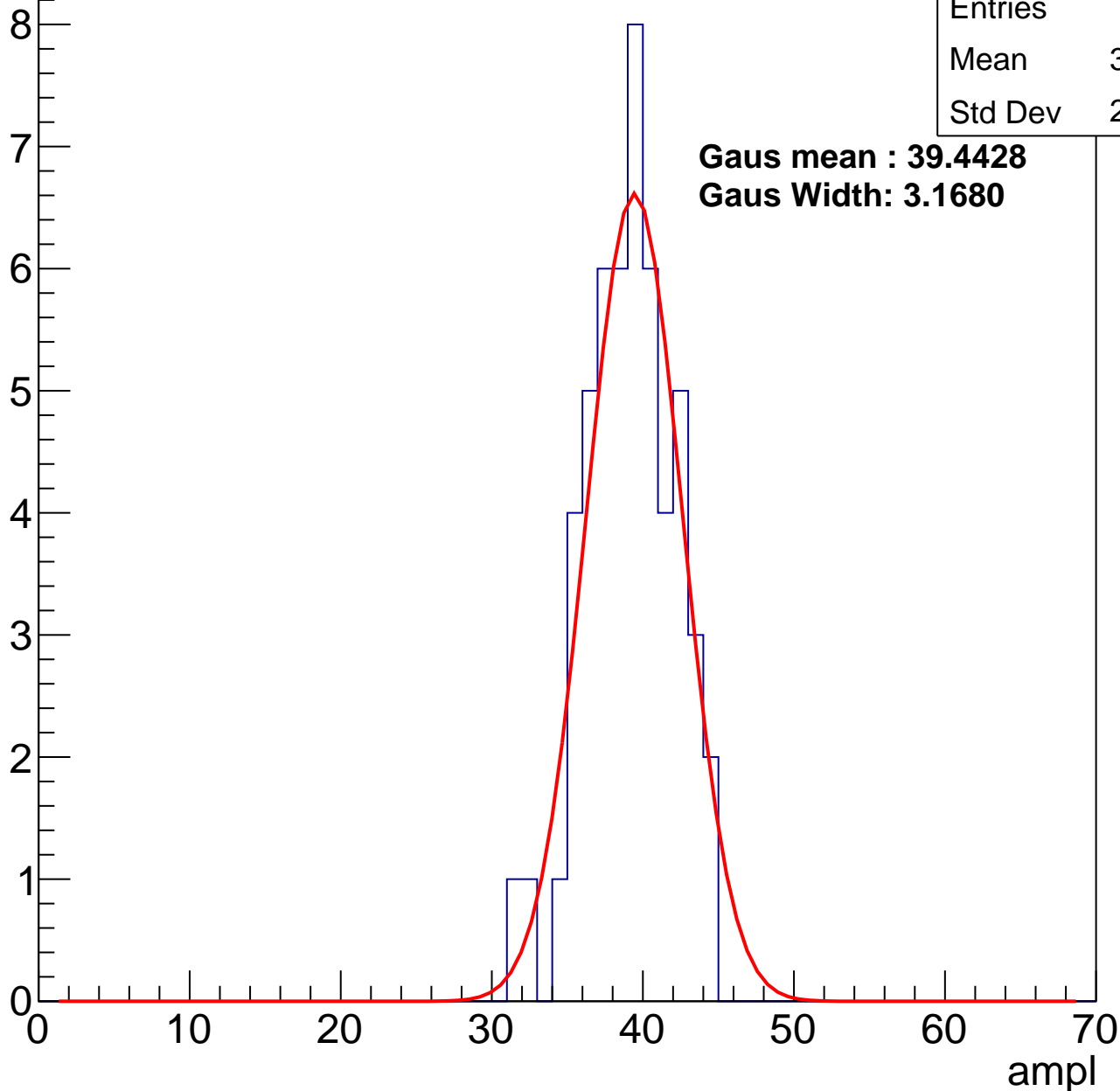
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	52
Mean	38.65
Std Dev	2.895

**Gaus mean : 39.4428**

**Gaus Width: 3.1680**



# B1L003S, U11-ch84, adc2

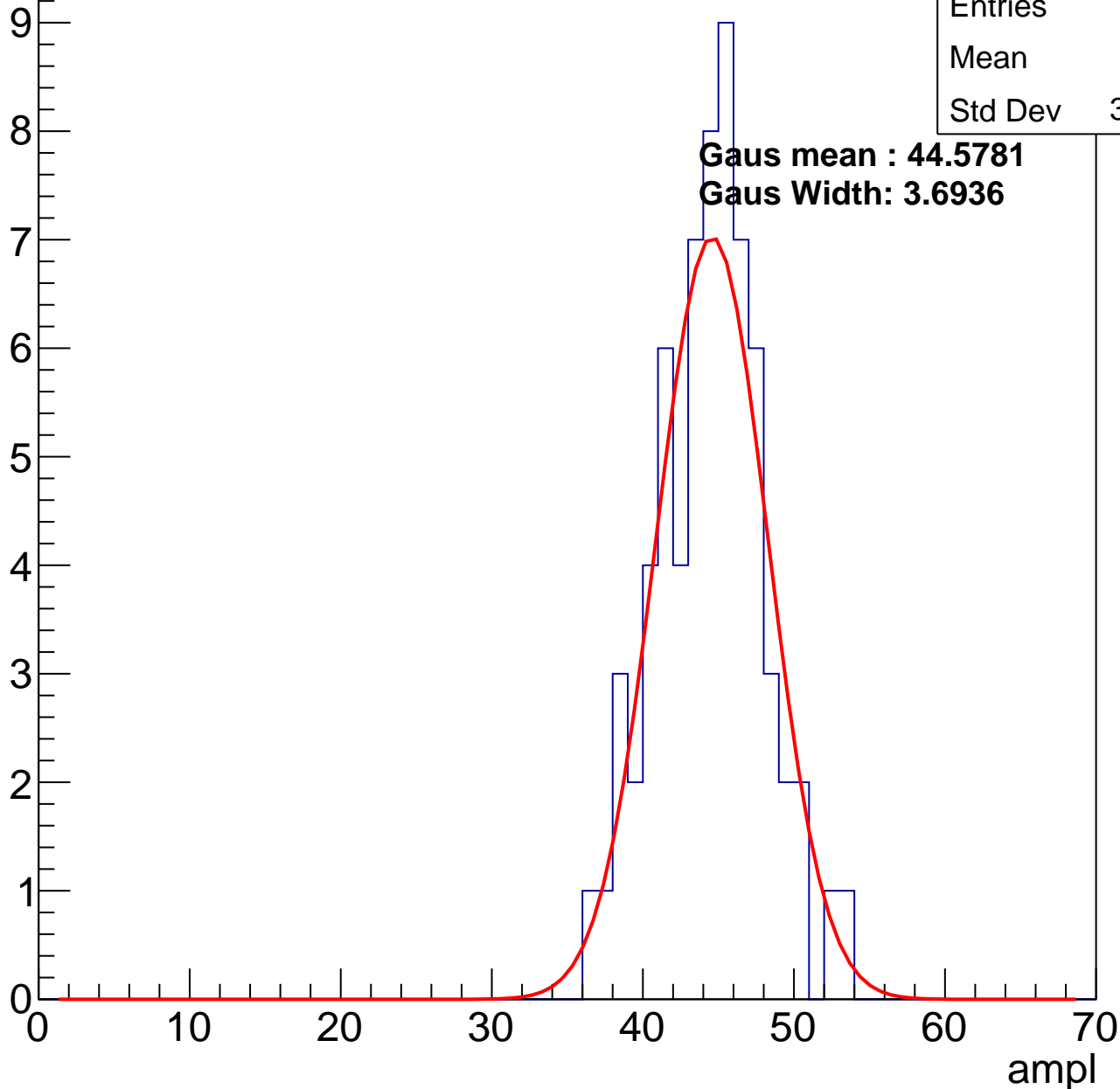
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	44
Std Dev	3.494

**Gaus mean : 44.5781**

**Gaus Width: 3.6936**

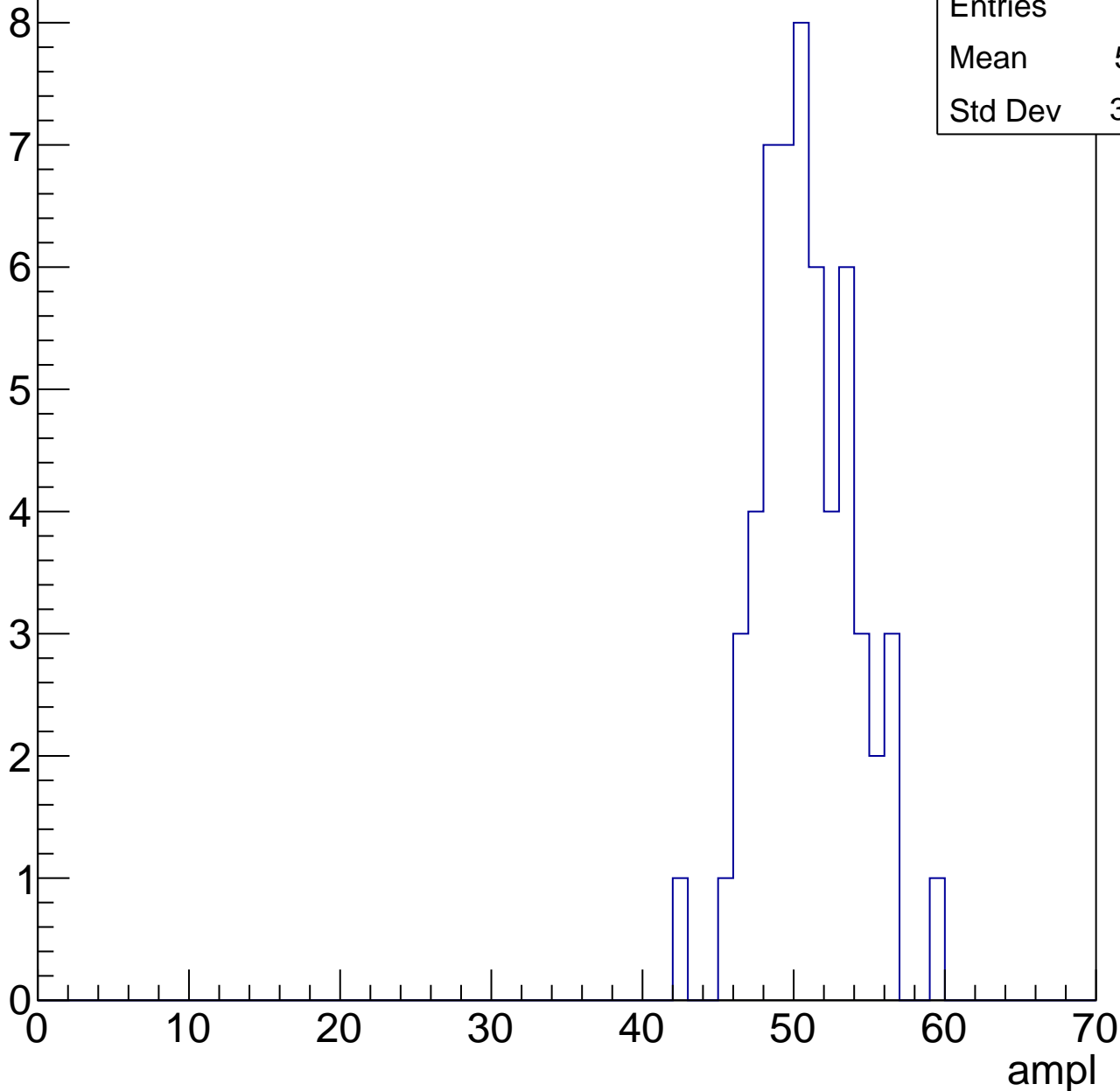


# B1L003S, U11-ch84, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	50.41
Std Dev	3.167

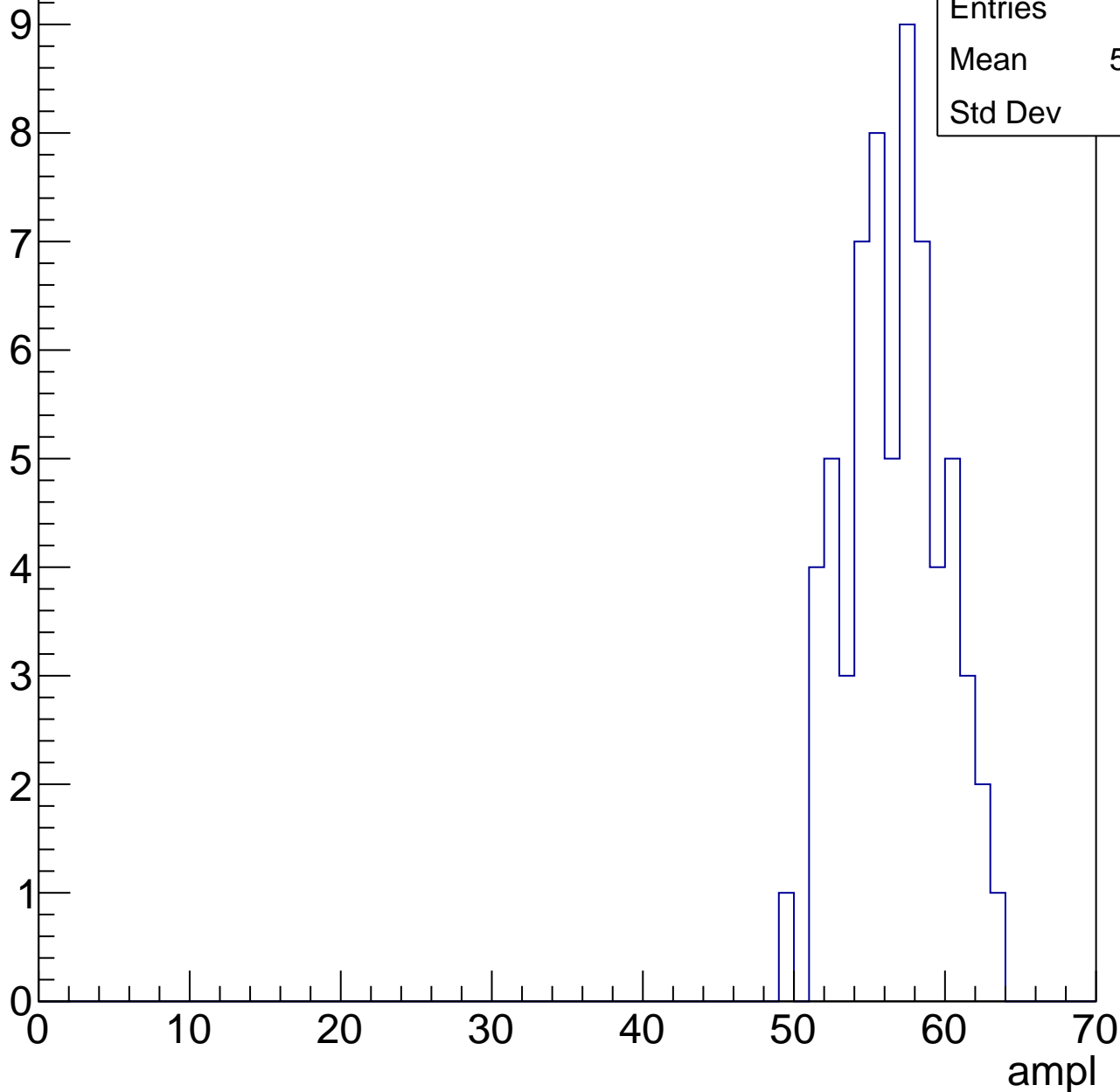


# B1L003S, U11-ch84, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	56.17
Std Dev	3.16

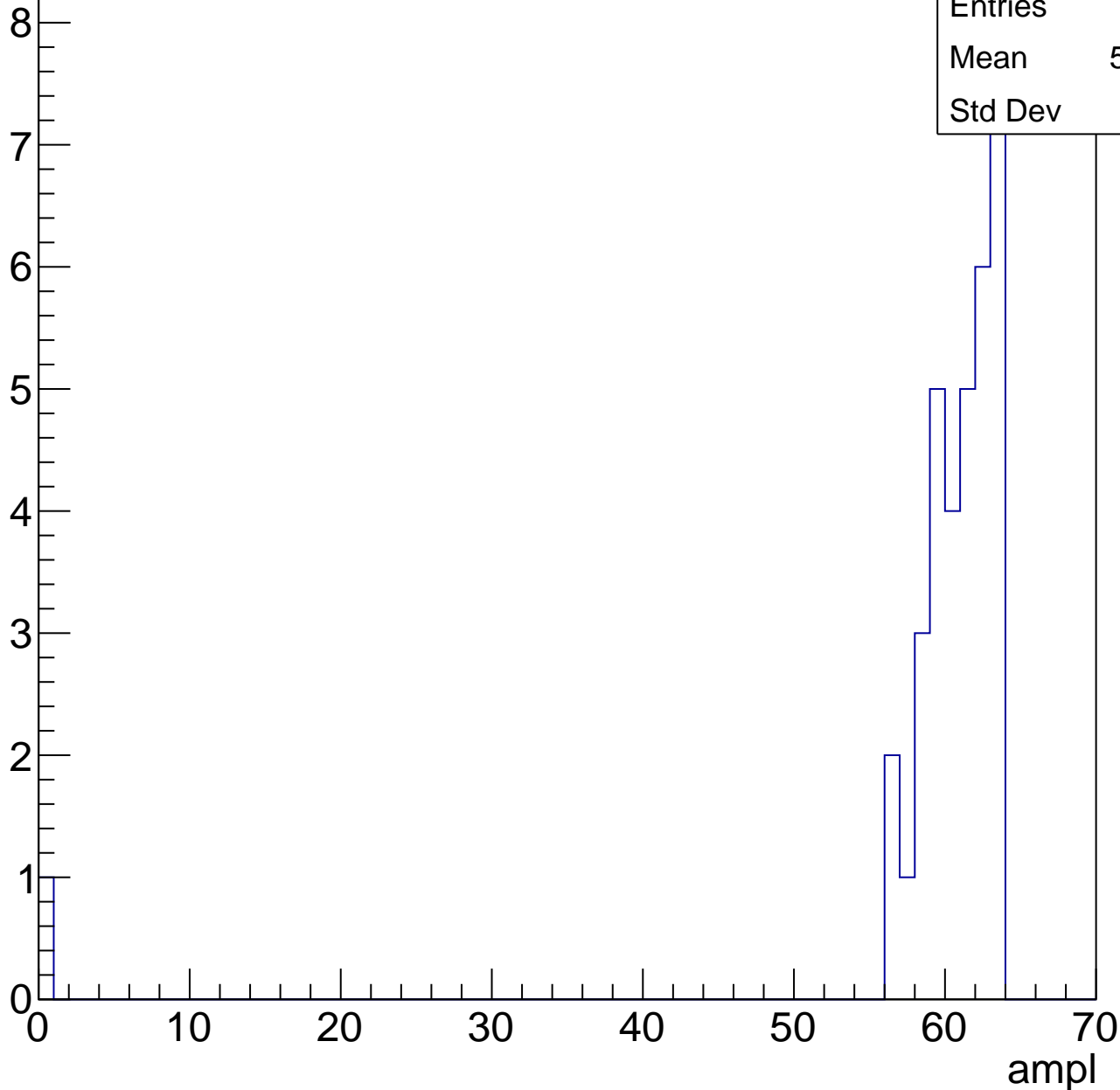


# B1L003S, U11-ch84, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	35
Mean	58.83
Std Dev	10.3



# B1L003S, U11-ch84, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	61.5
Std Dev	0.9574

ampl

0 10 20 30 40 50 60 70



# B1L003S, U11-ch84, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	23
Std Dev	0

ampl

# B1L003S, U11-ch85, adc0

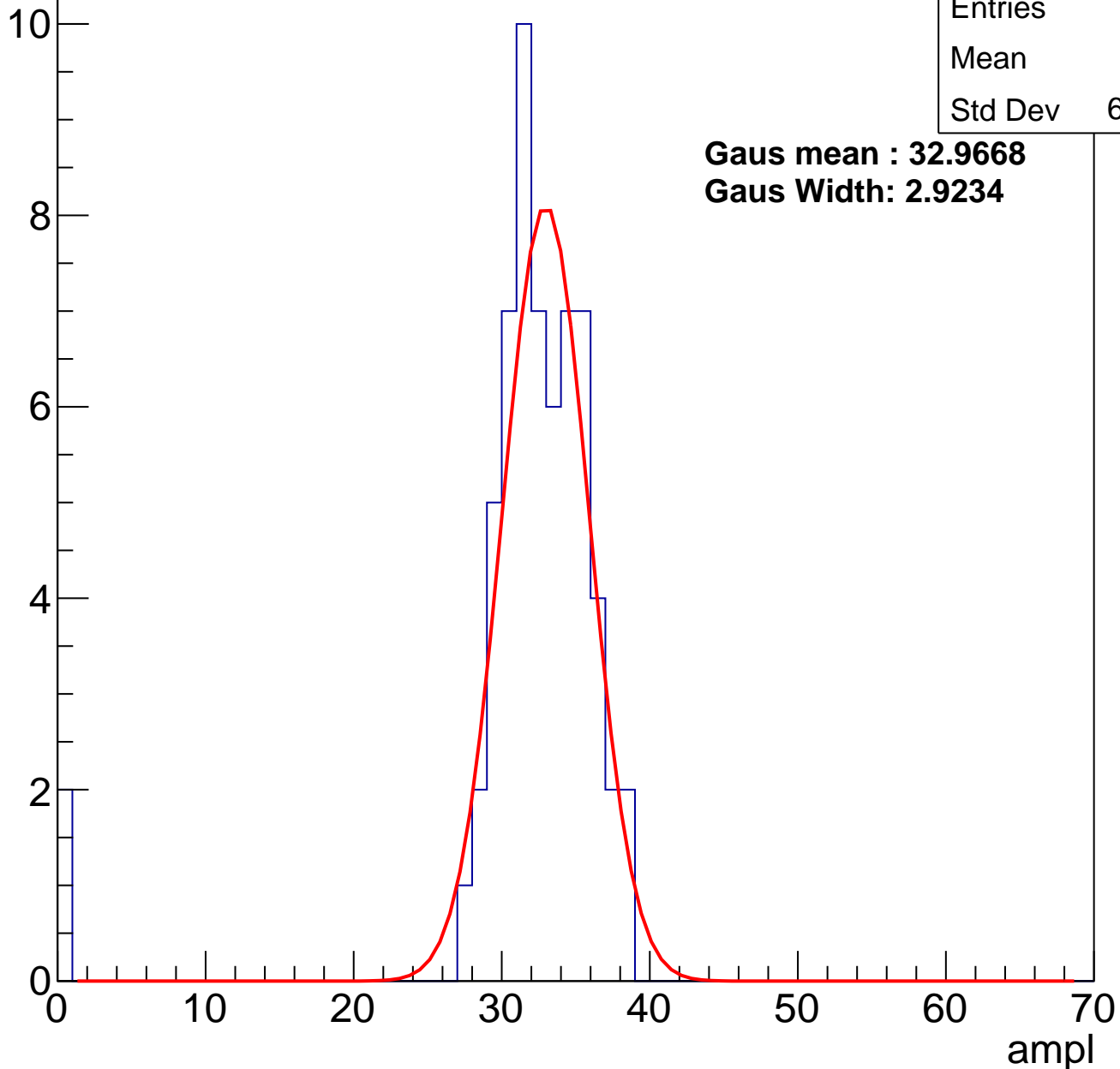
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	62
Mean	31.4
Std Dev	6.285

**Gaus mean : 32.9668**

**Gaus Width: 2.9234**

Entry



# B1L003S, U11-ch85, adc1

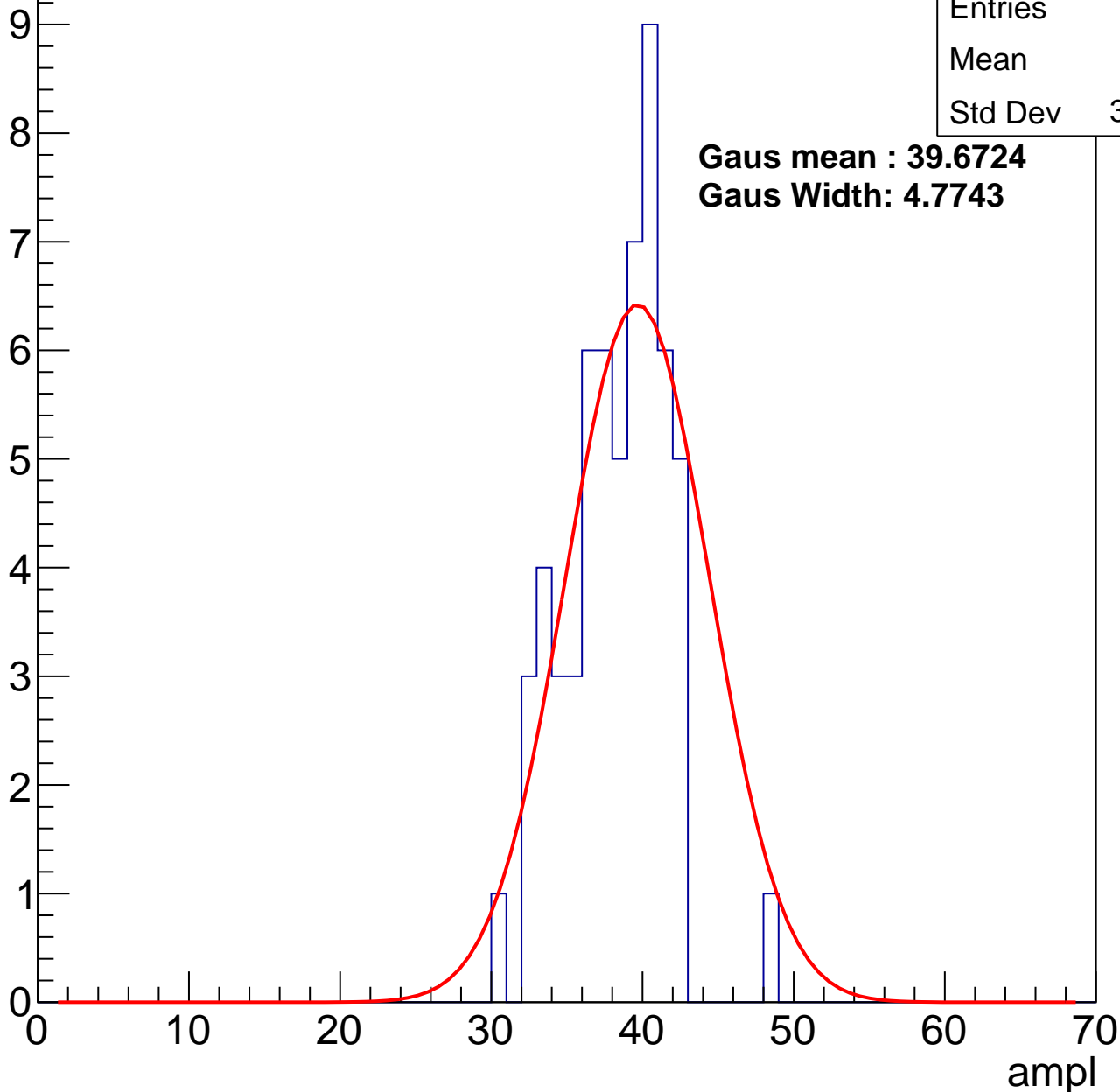
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	37.8
Std Dev	3.323

**Gaus mean : 39.6724**

**Gaus Width: 4.7743**



# B1L003S, U11-ch85, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	69
Mean	44.36
Std Dev	3.443

**Gaus mean : 45.1774**

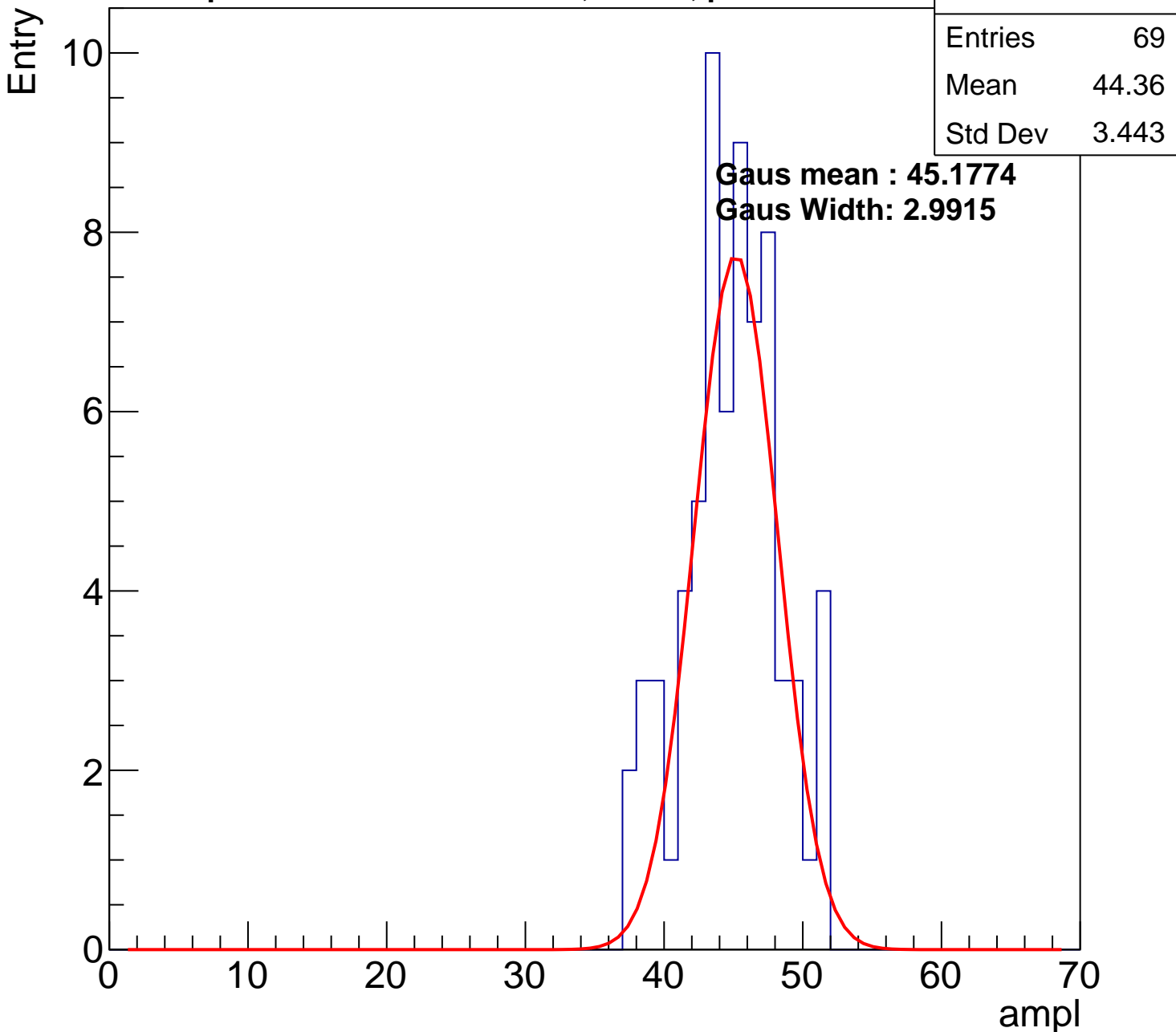
**Gaus Width: 2.9915**

Entry

10  
8  
6  
4  
2  
0

ampl

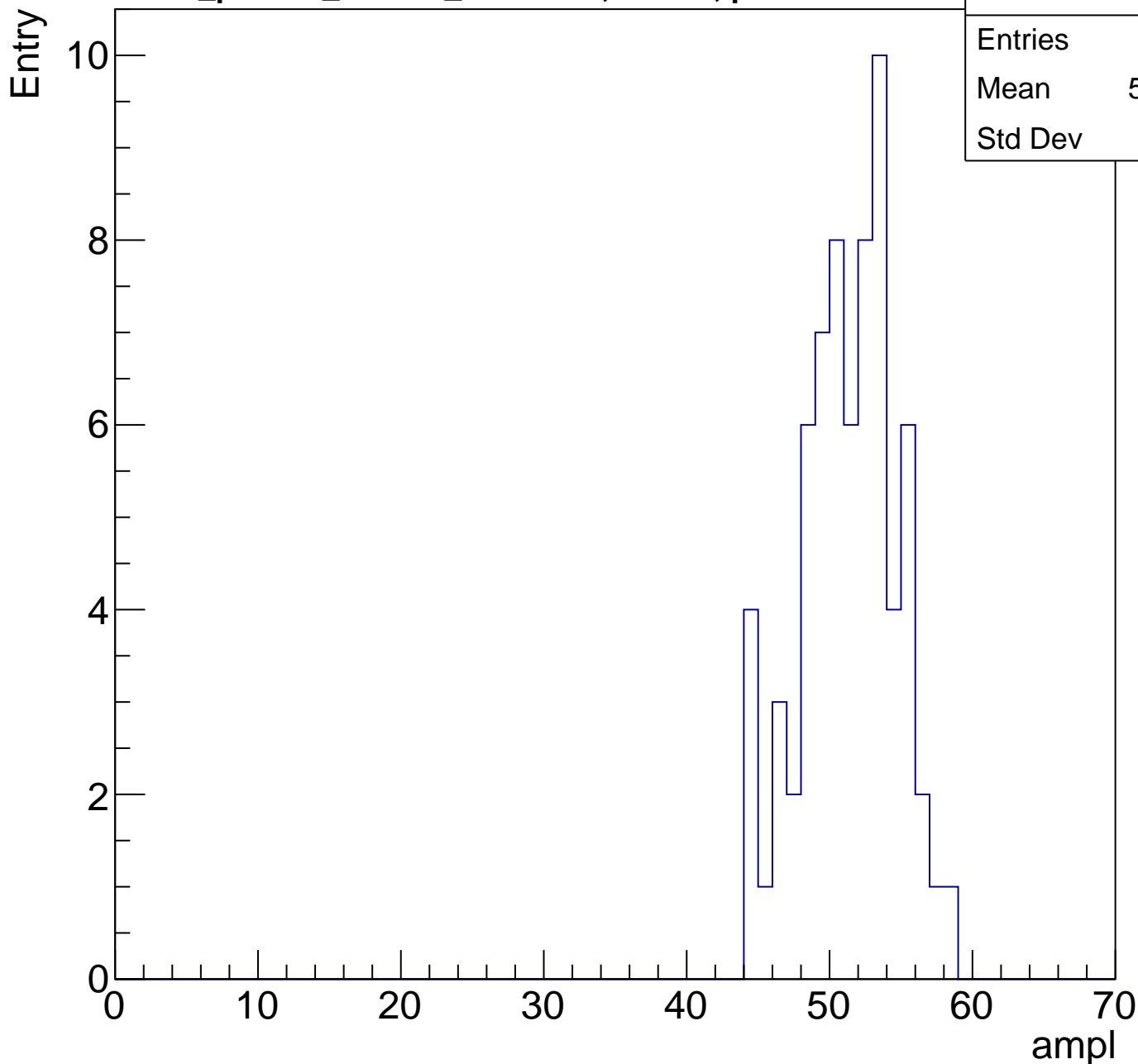
0 10 20 30 40 50 60 70



# B1L003S, U11-ch85, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	69
Mean	50.86
Std Dev	3.28

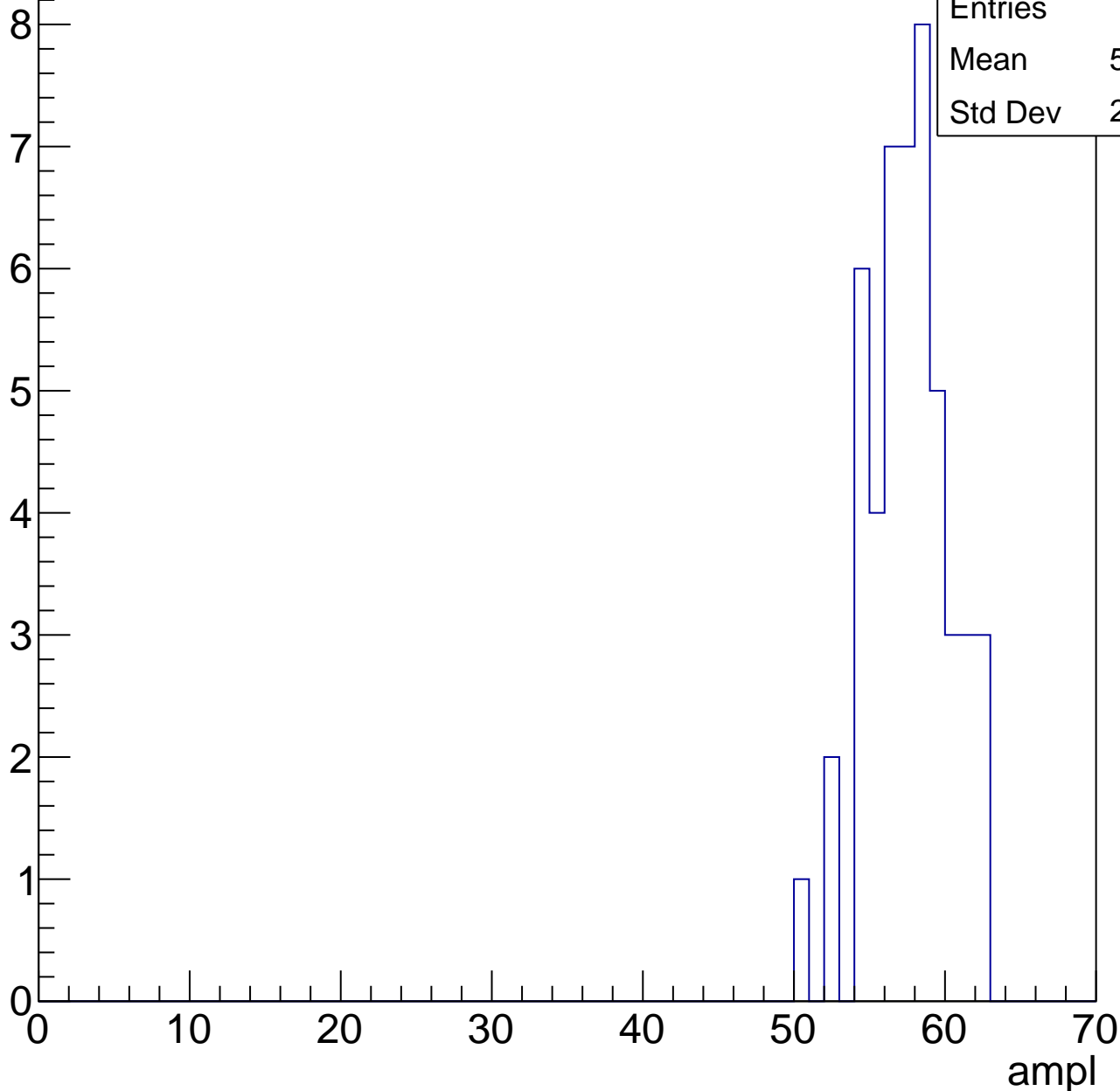


# B1L003S, U11-ch85, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	49
Mean	57.08
Std Dev	2.687



# B1L003S, U11-ch85, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	39
Mean	59.33
Std Dev	9.807

Entry

10

8

6

4

2

0

0

10

20

30

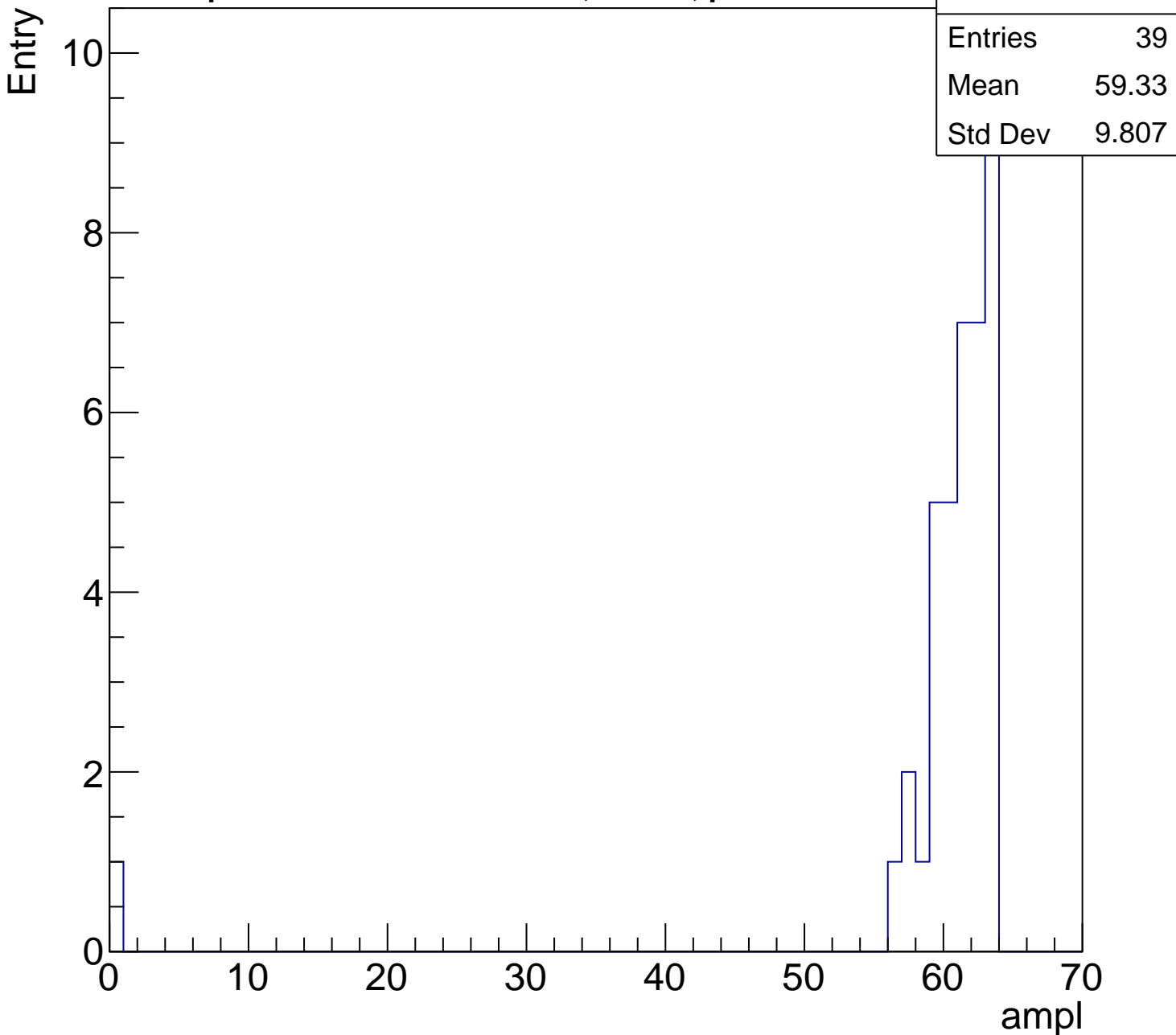
40

50

60

70

ampl



# B1L003S, U11-ch85, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

0 10 20 30 40 50 60 70

ampl

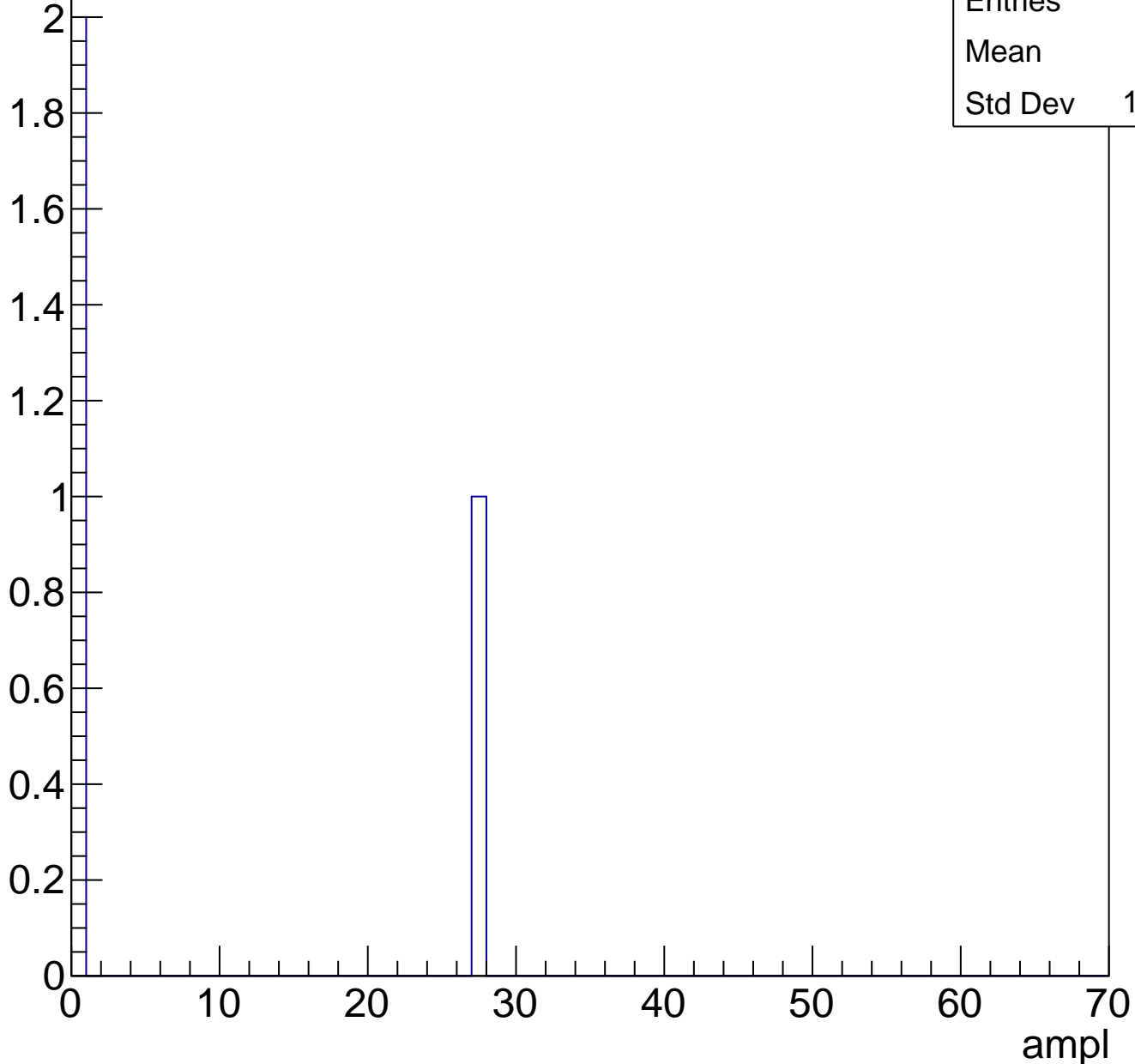
Entries	2
Mean	60
Std Dev	0



# B1L003S, U11-ch85, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	3
Mean	9
Std Dev	12.73

# B1L003S, U11-ch86, adc0

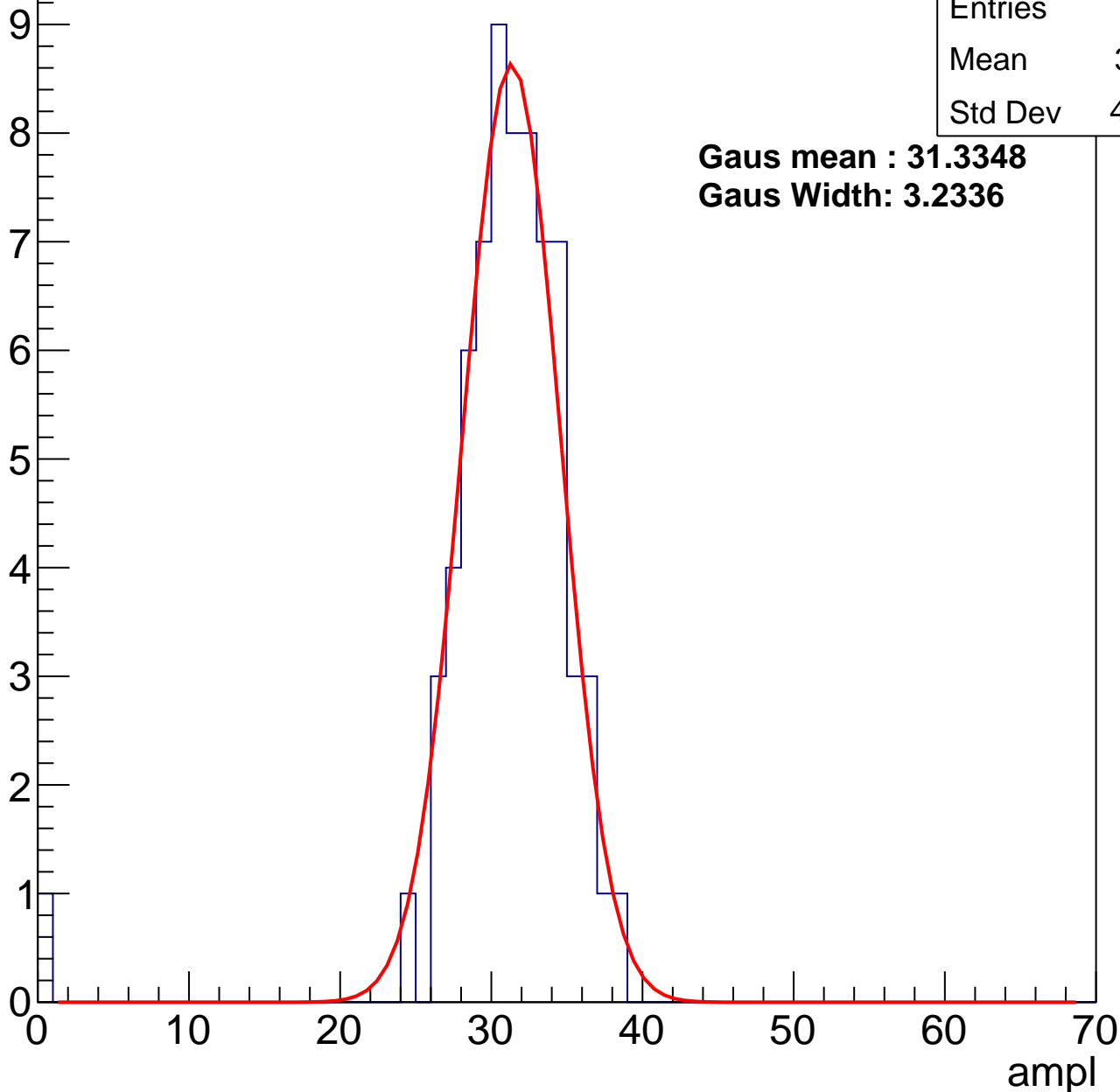
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	30.61
Std Dev	4.719

**Gaus mean : 31.3348**

**Gaus Width: 3.2336**



# B1L003S, U11-ch86, adc1

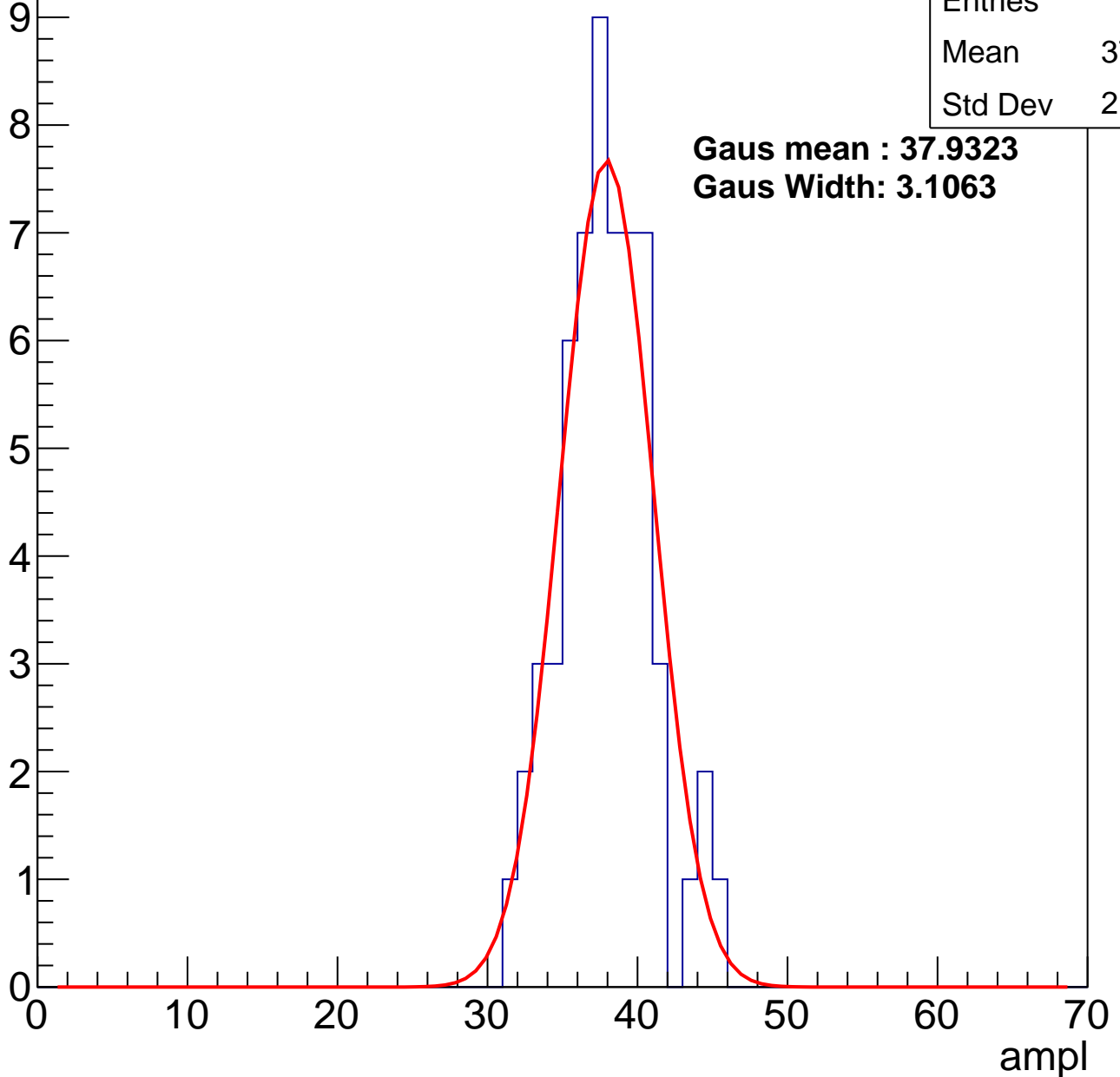
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	37.44
Std Dev	2.982

**Gaus mean : 37.9323**

**Gaus Width: 3.1063**



# B1L003S, U11-ch86, adc2

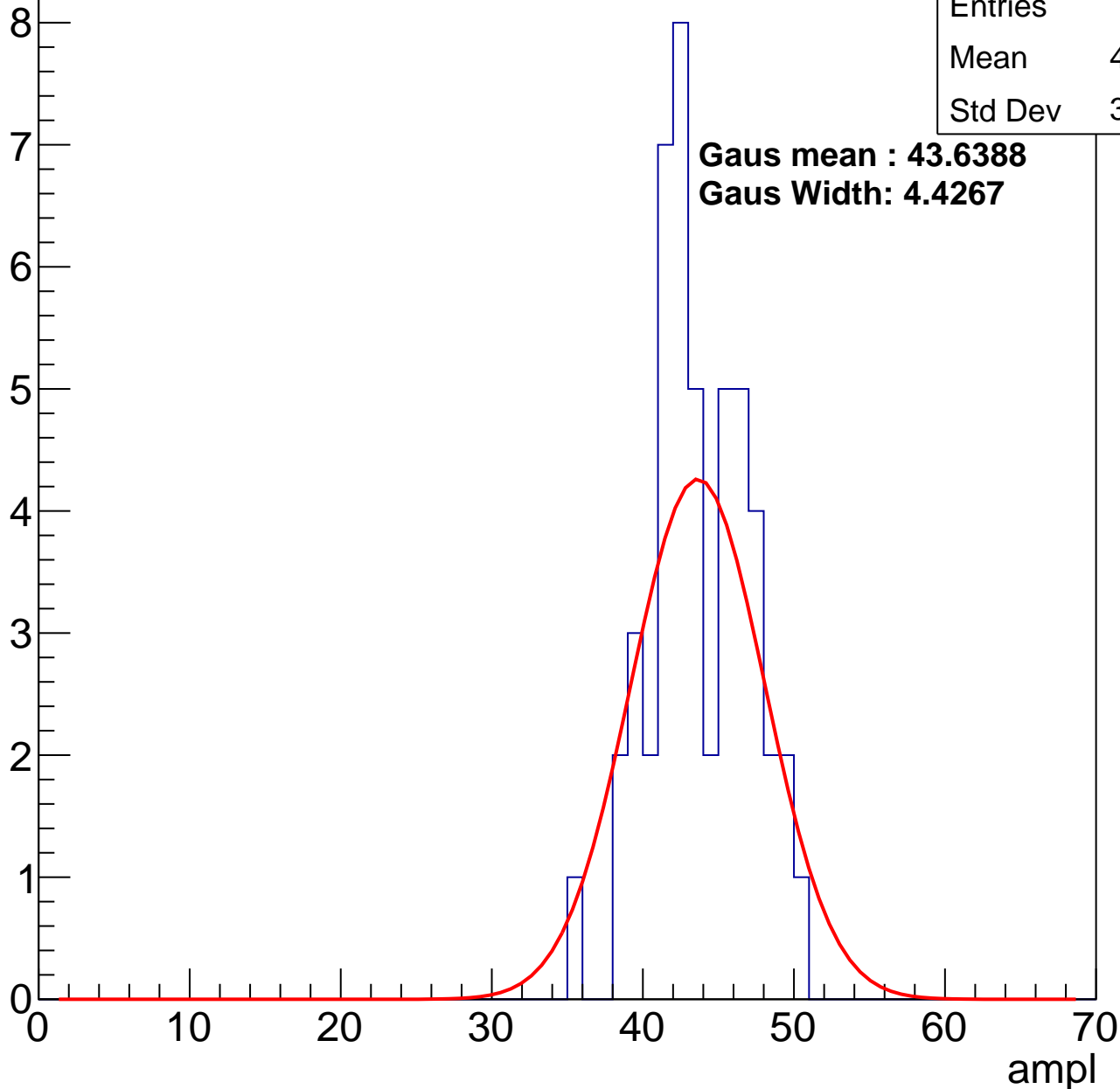
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	49
Mean	43.29
Std Dev	3.239

**Gaus mean : 43.6388**

**Gaus Width: 4.4267**

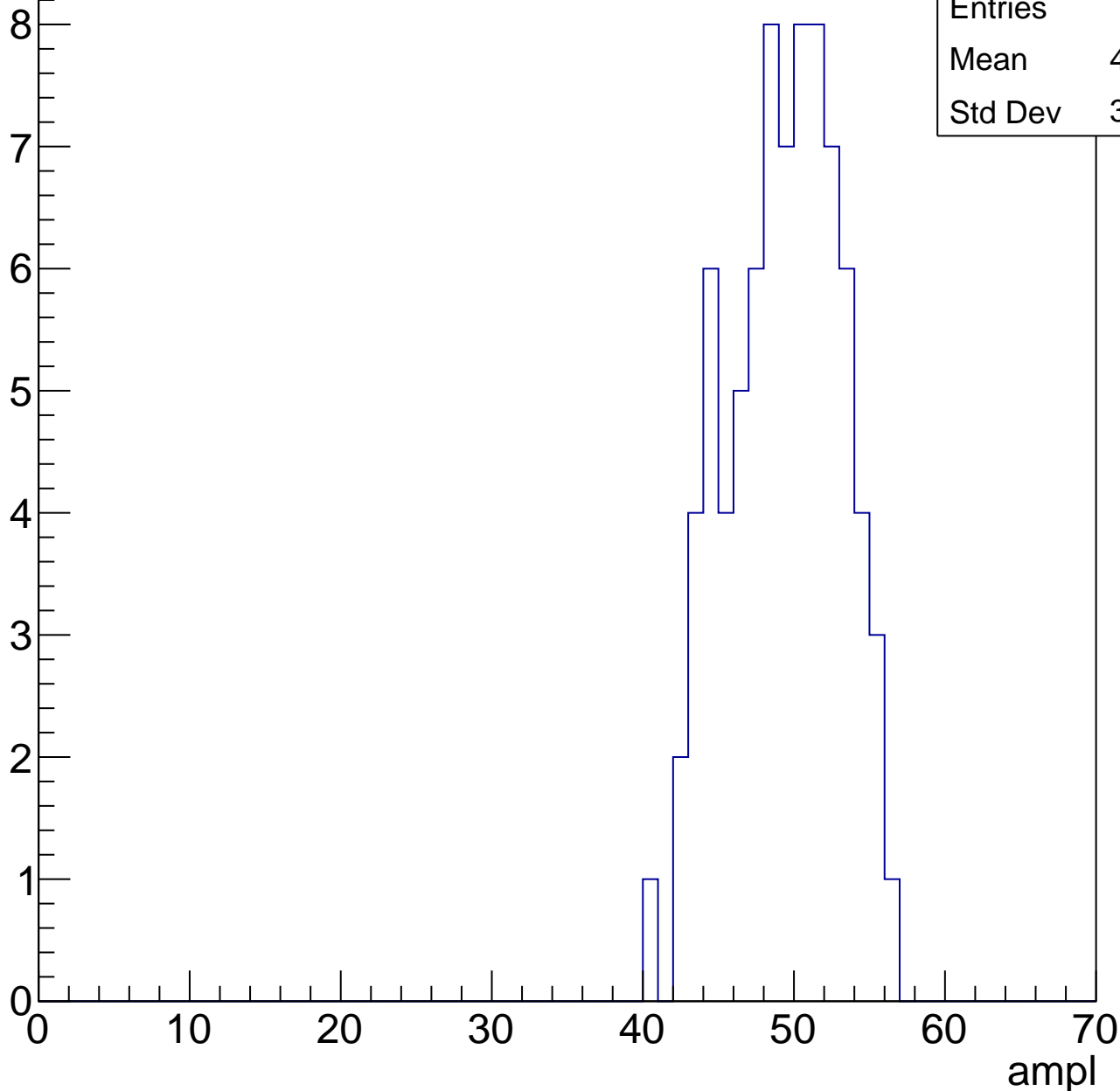


# B1L003S, U11-ch86, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

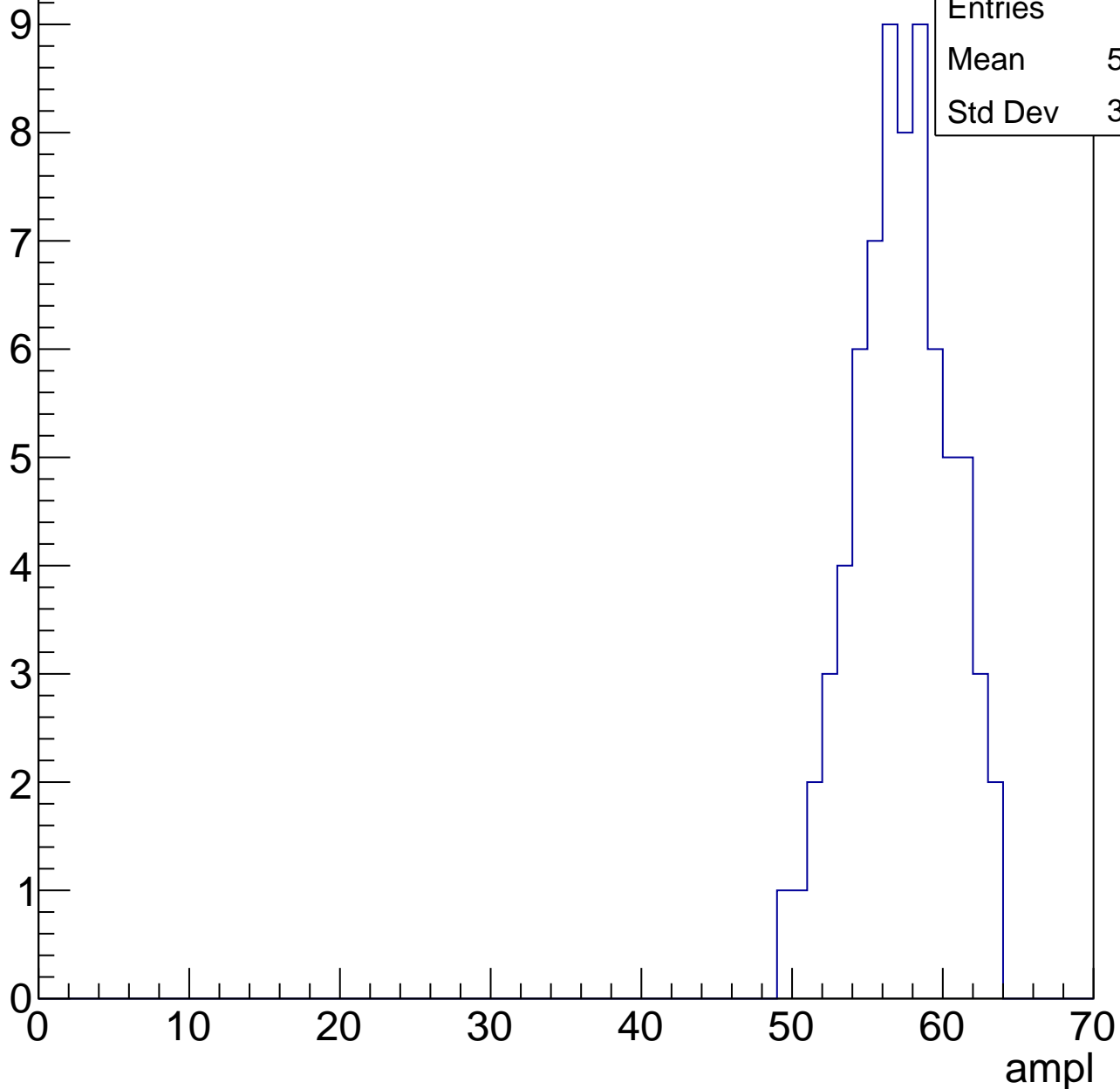
Entries	80
Mean	48.83
Std Dev	3.653



# B1L003S, U11-ch86, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



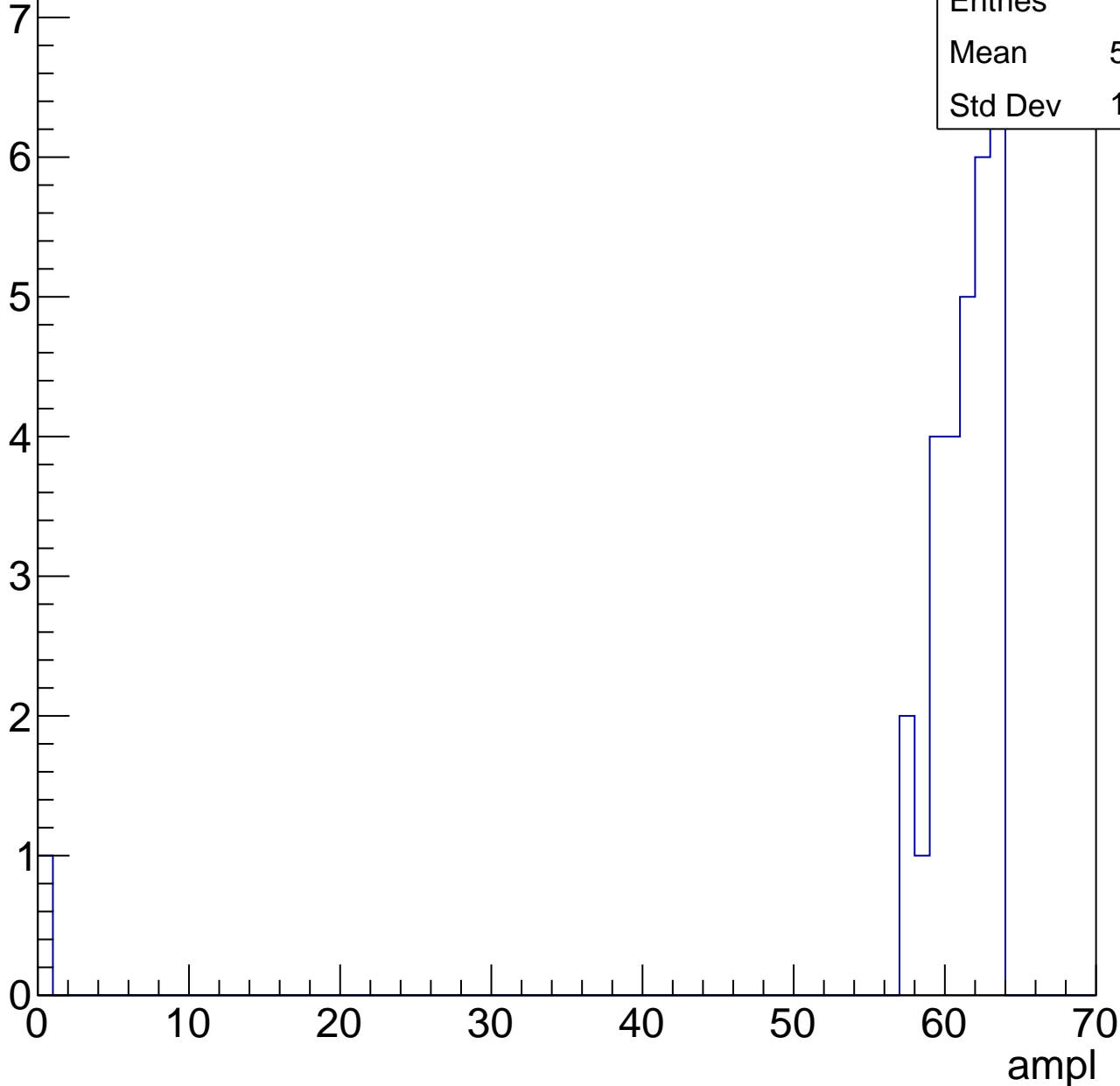
Entries	71
Mean	56.77
Std Dev	3.176

# B1L003S, U11-ch86, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	30
Mean	58.87
Std Dev	11.07



# B1L003S, U11-ch86, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch86, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U11-ch87, adc0

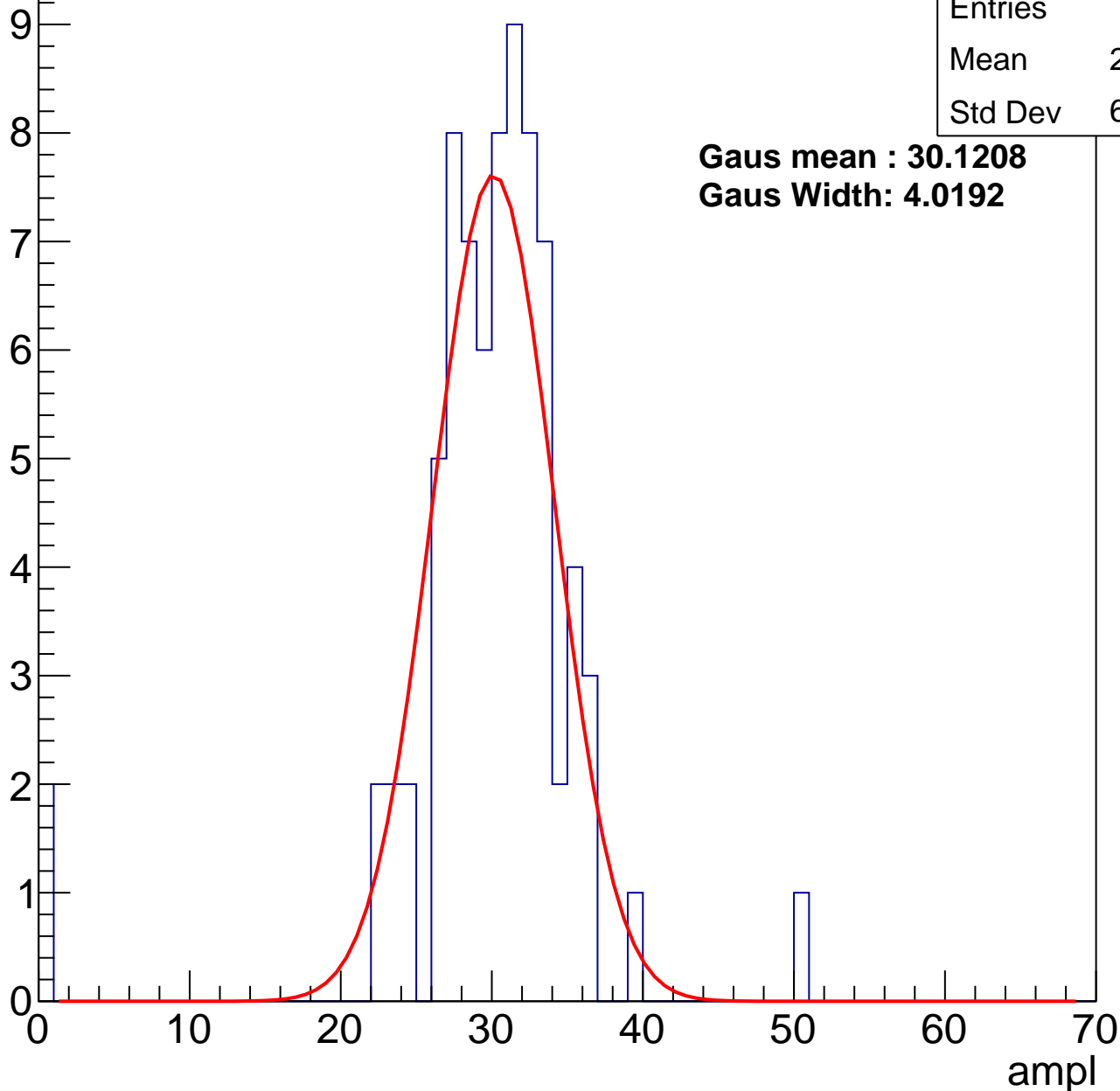
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	77
Mean	29.42
Std Dev	6.327

**Gaus mean : 30.1208**

**Gaus Width: 4.0192**



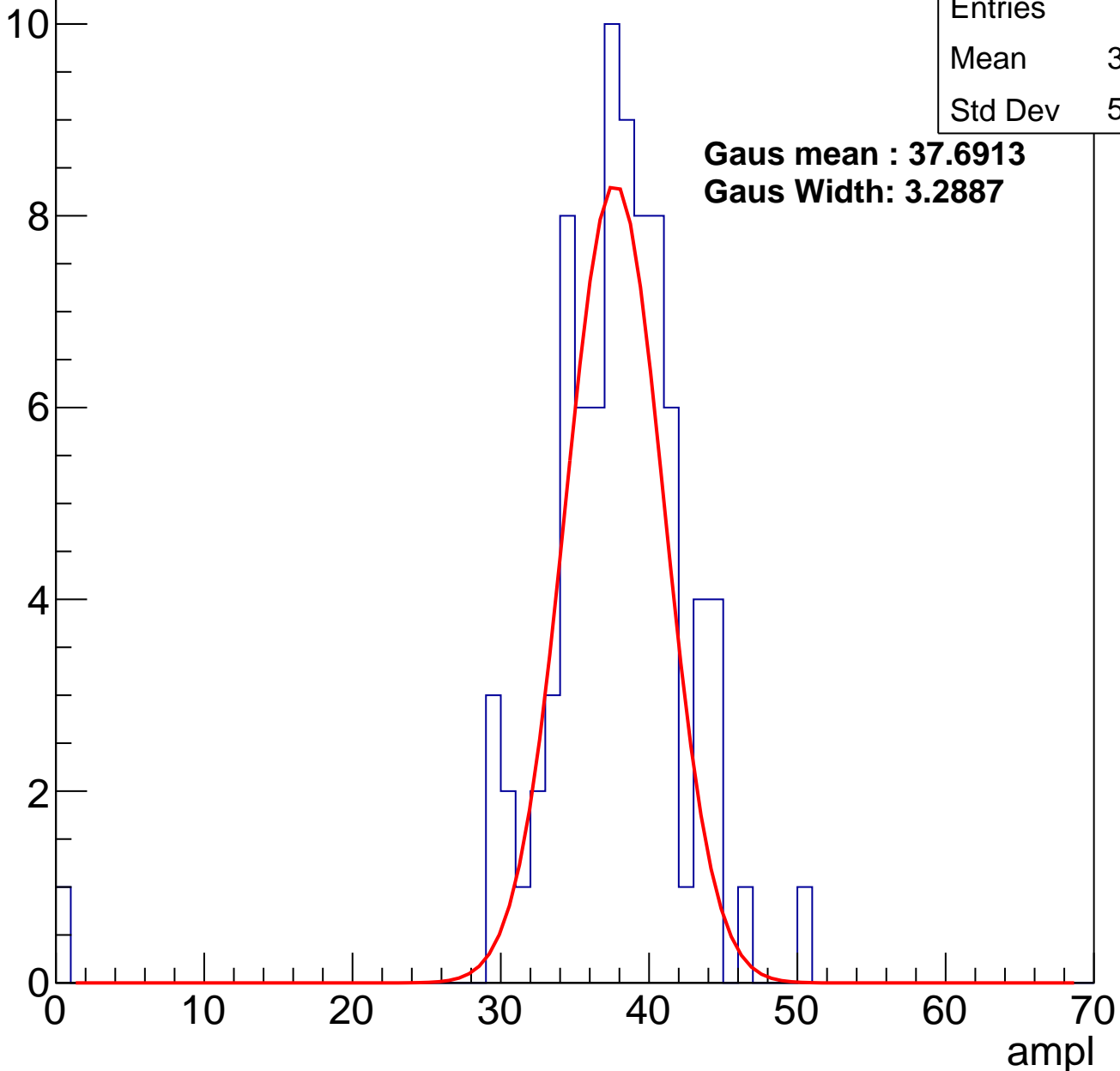
# B1L003S, U11-ch87, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	84
Mean	37.08
Std Dev	5.689

**Gaus mean : 37.6913**  
**Gaus Width: 3.2887**

Entry



# B1L003S, U11-ch87, adc2

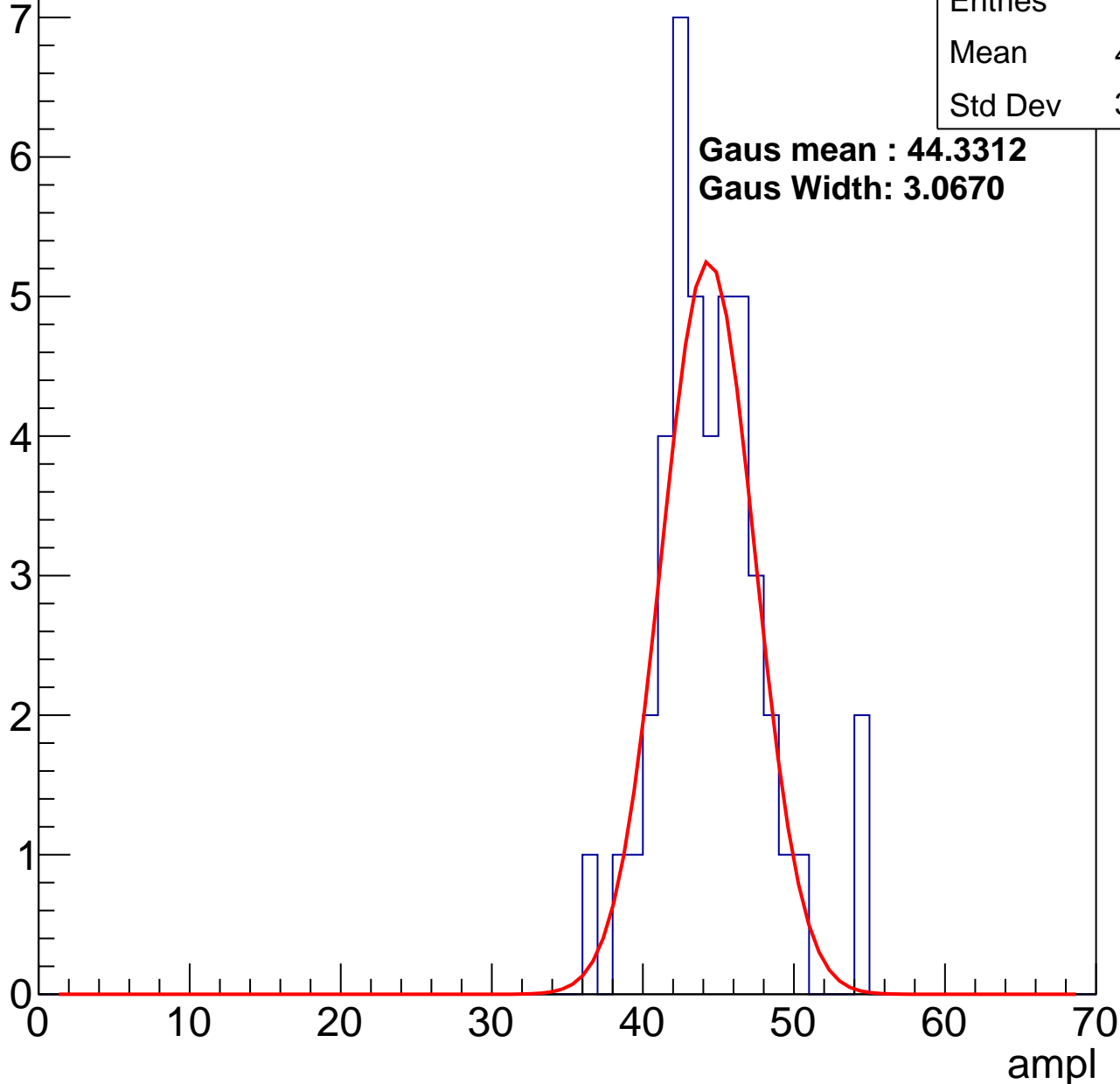
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	44
Mean	44.11
Std Dev	3.601

**Gaus mean : 44.3312**

**Gaus Width: 3.0670**

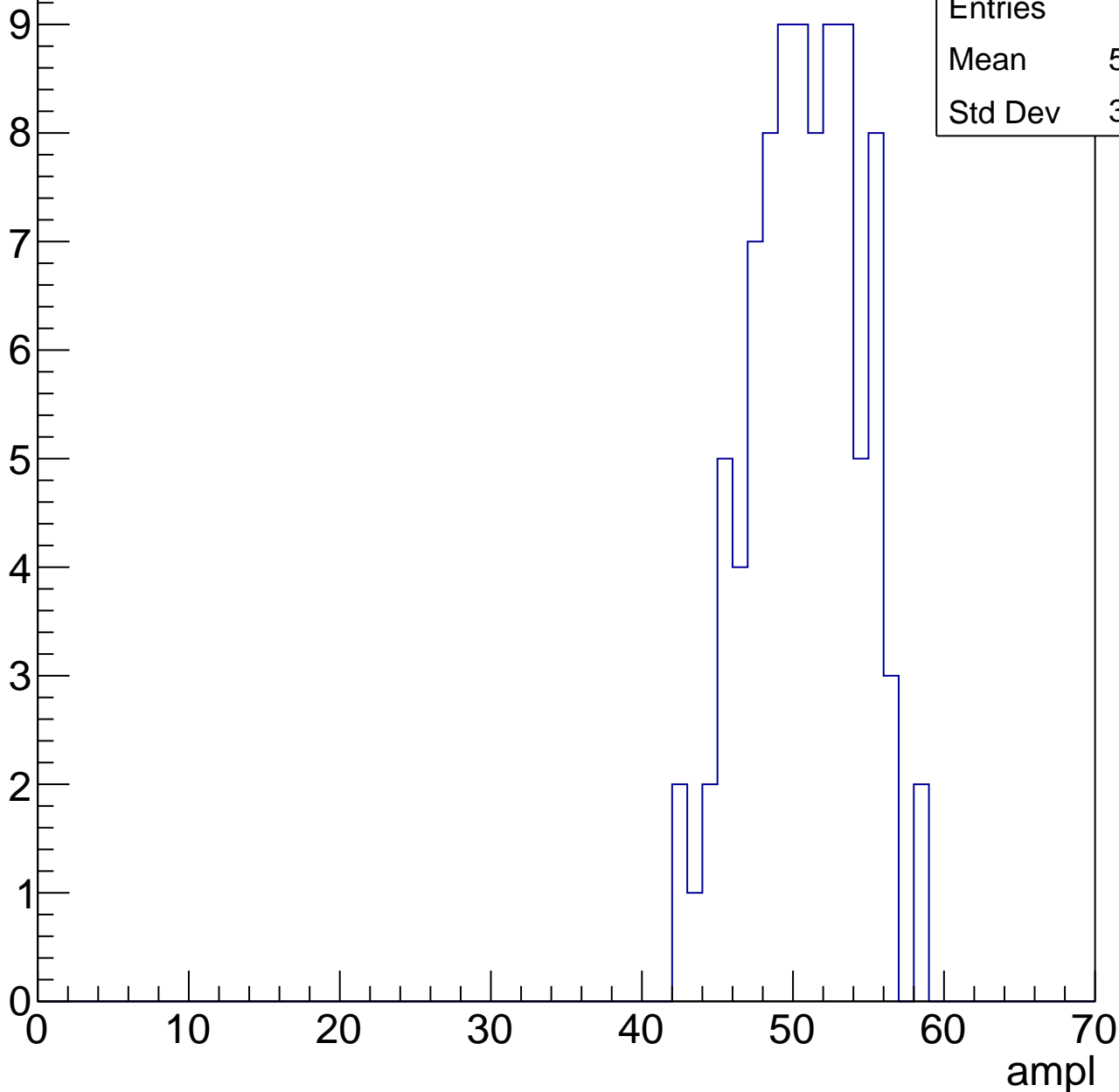


# B1L003S, U11-ch87, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	91
Mean	50.27
Std Dev	3.595

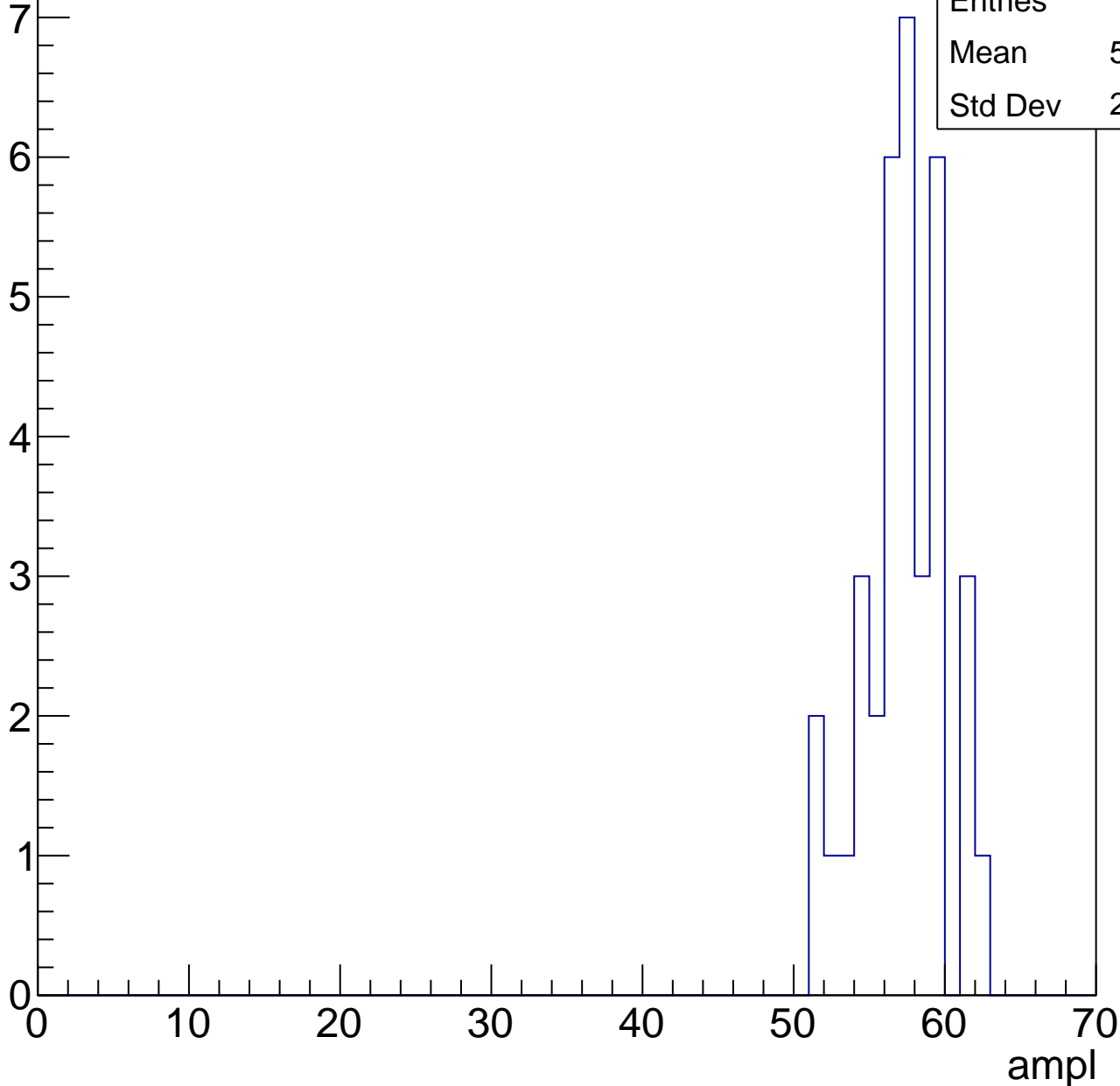


# B1L003S, U11-ch87, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	35
Mean	56.77
Std Dev	2.684



# B1L003S, U11-ch87, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

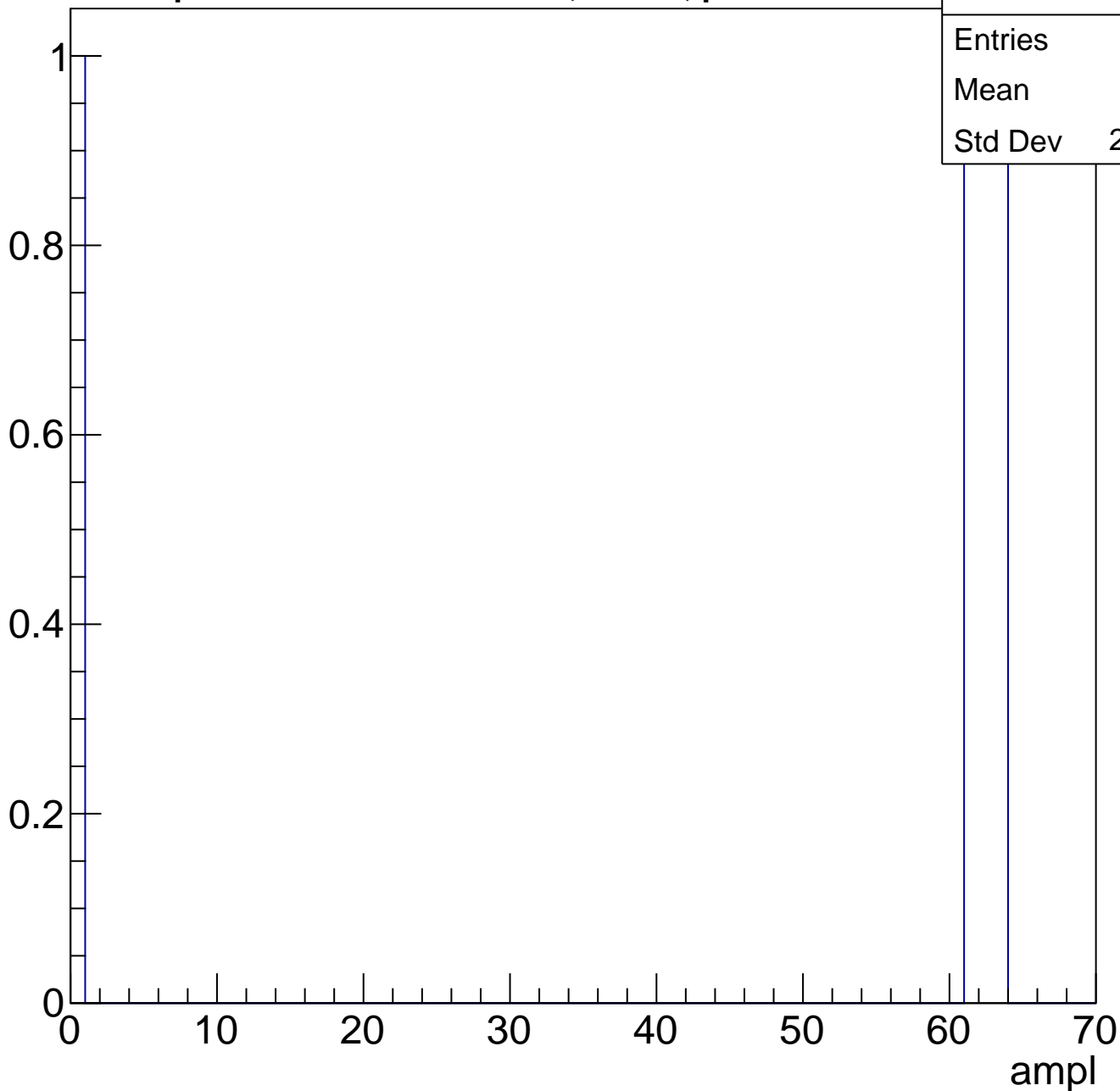
ampl

Entries	46
Mean	60.48
Std Dev	1.953

# B1L003S, U11-ch87, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

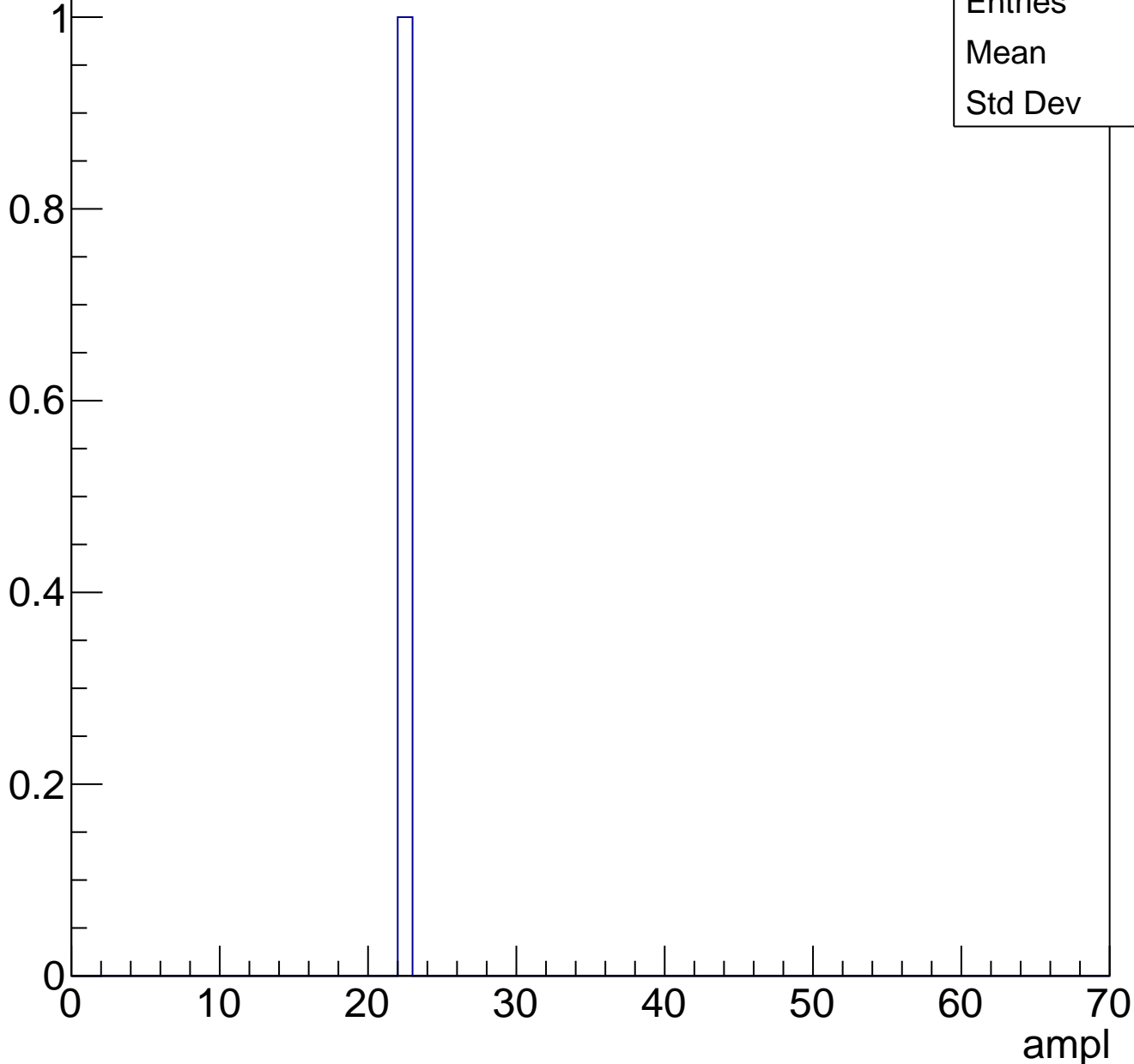




# B1L003S, U11-ch87, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

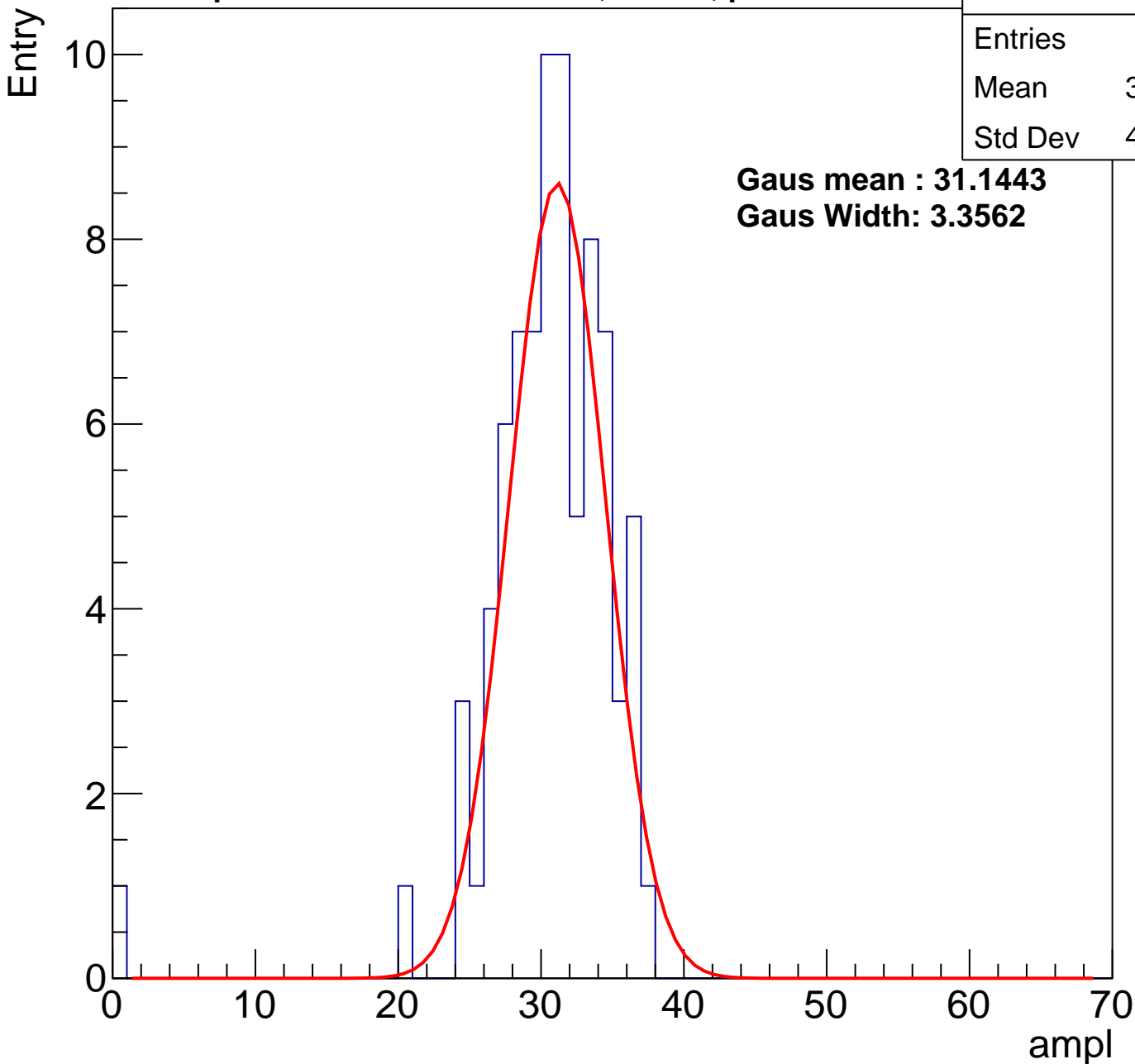


# B1L003S, U11-ch88, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	79
Mean	30.08
Std Dev	4.778

**Gaus mean : 31.1443**  
**Gaus Width: 3.3562**



# B1L003S, U11-ch88, adc1

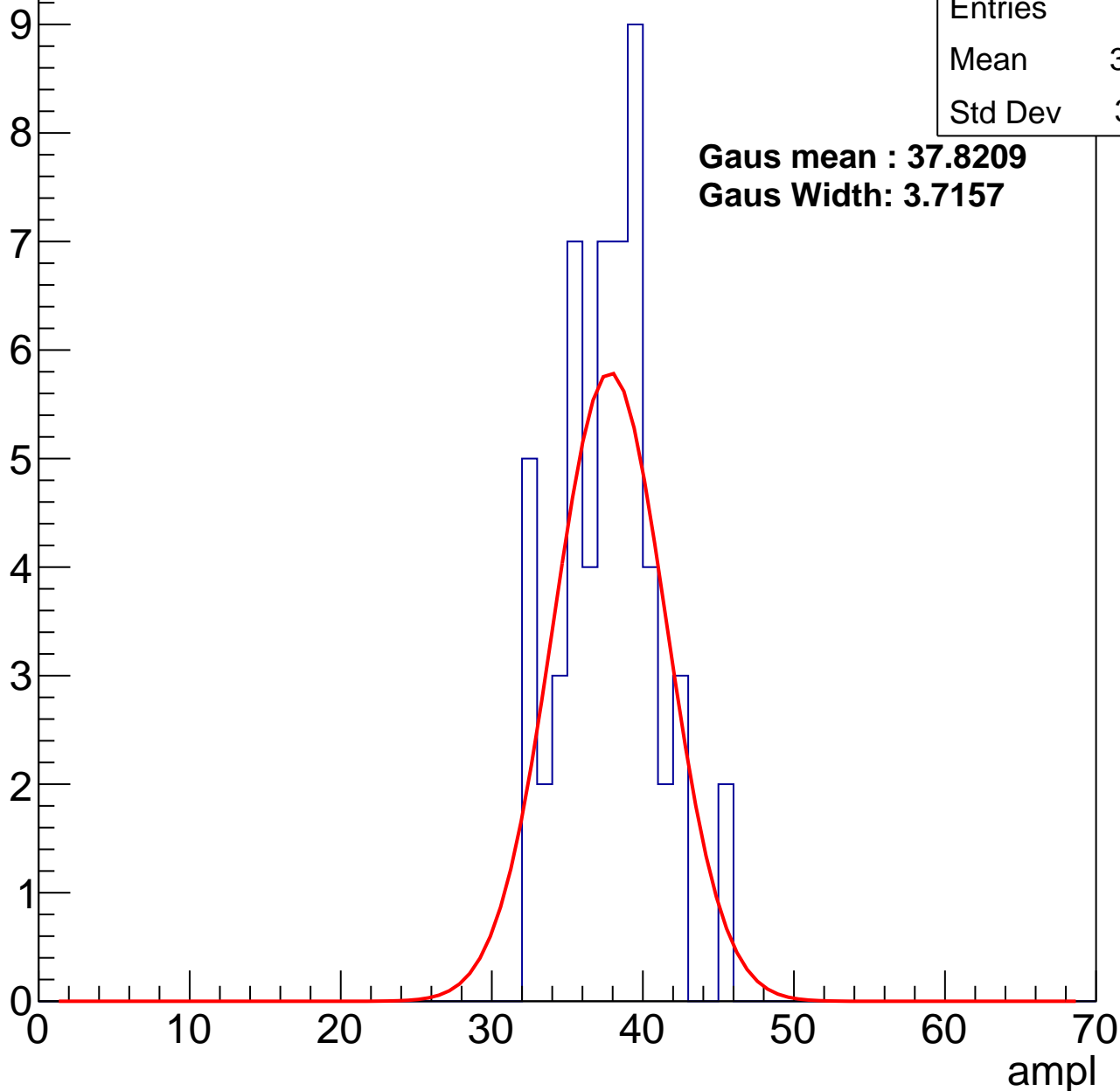
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	37.29
Std Dev	3.091

**Gaus mean : 37.8209**

**Gaus Width: 3.7157**



# B1L003S, U11-ch88, adc2

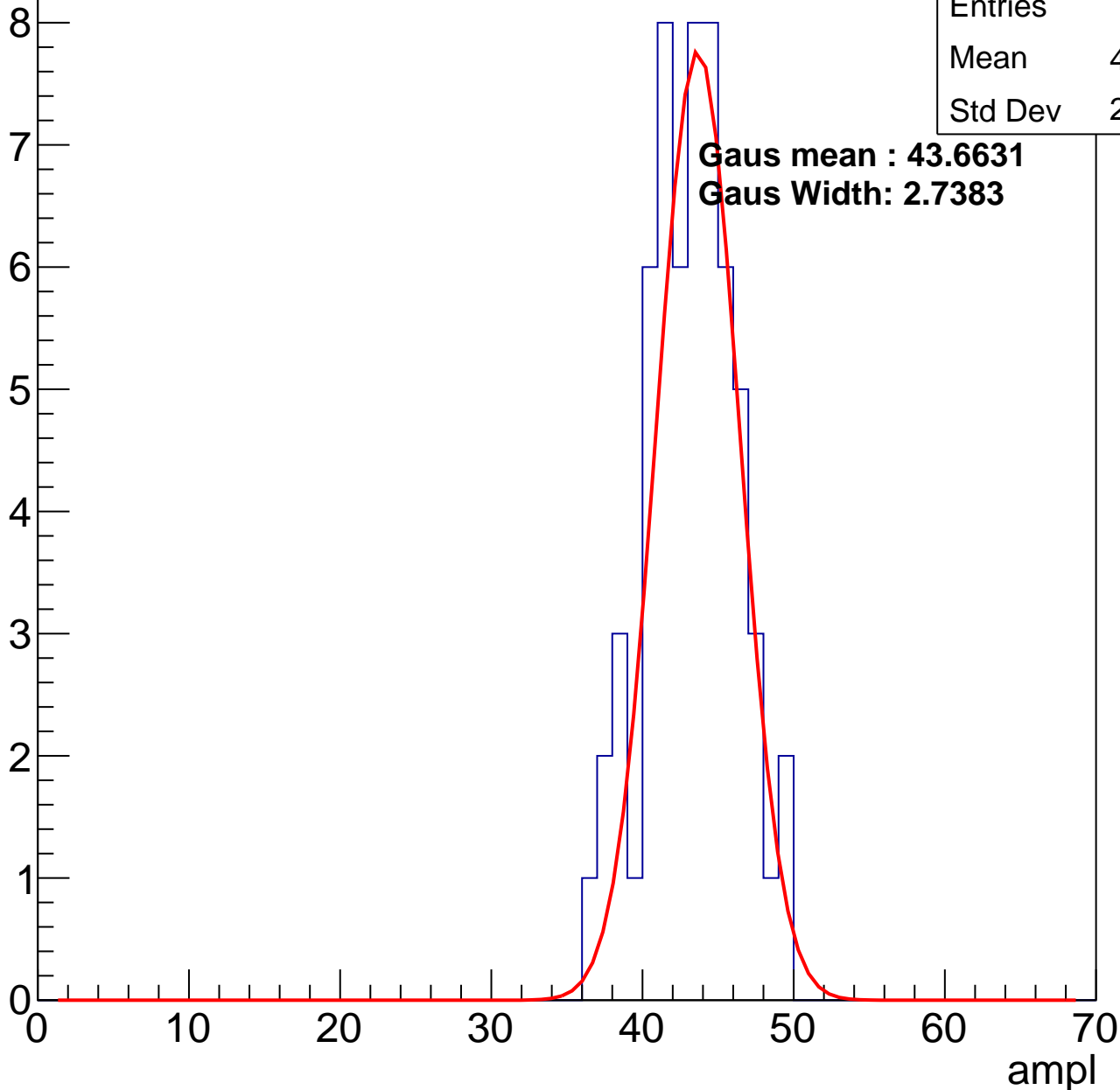
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	42.77
Std Dev	2.952

**Gaus mean : 43.6631**

**Gaus Width: 2.7383**



# B1L003S, U11-ch88, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	87
Mean	50.28
Std Dev	3.493

Entry

10

8

6

4

2

0

0

10

20

30

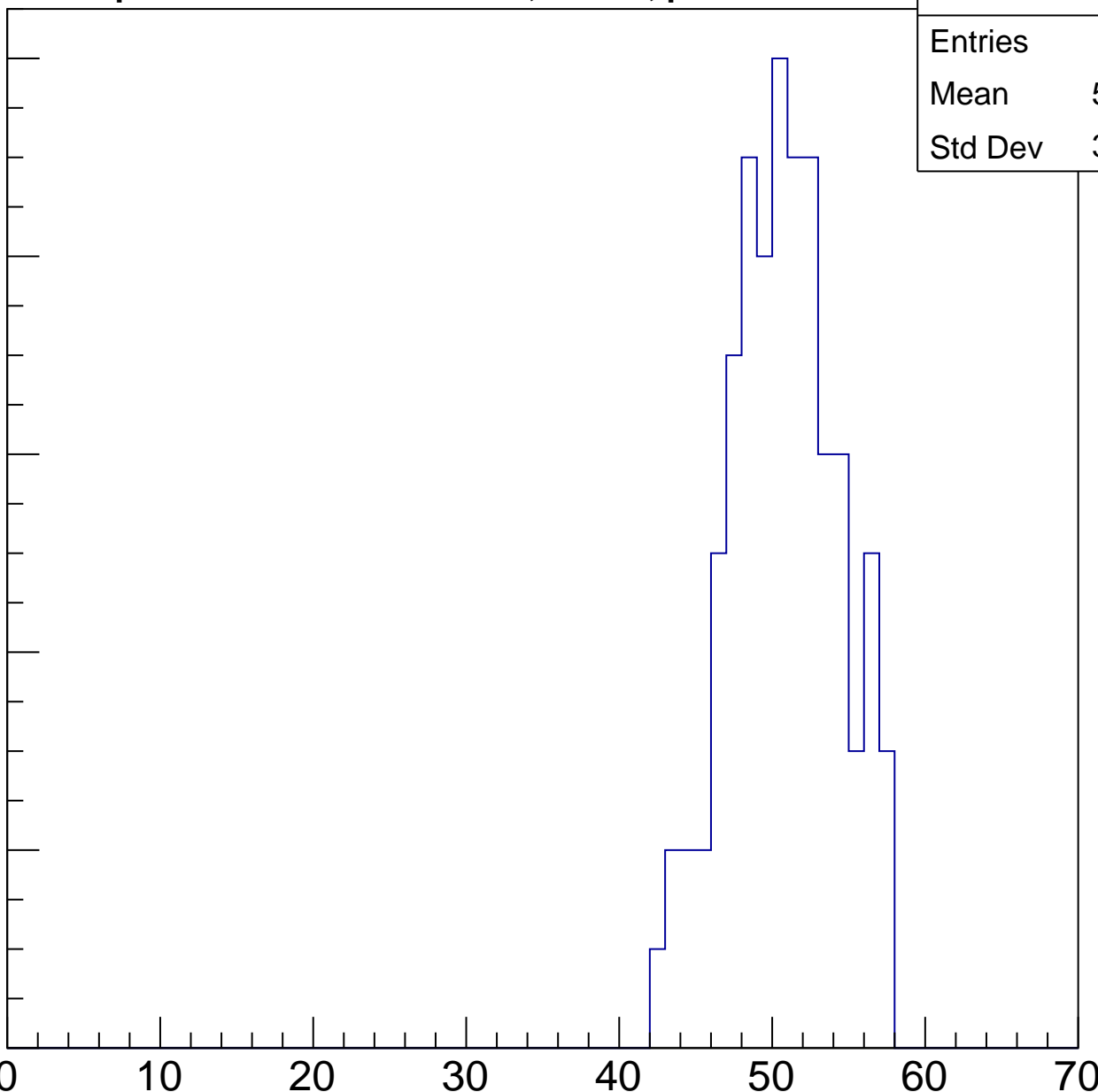
40

50

60

70

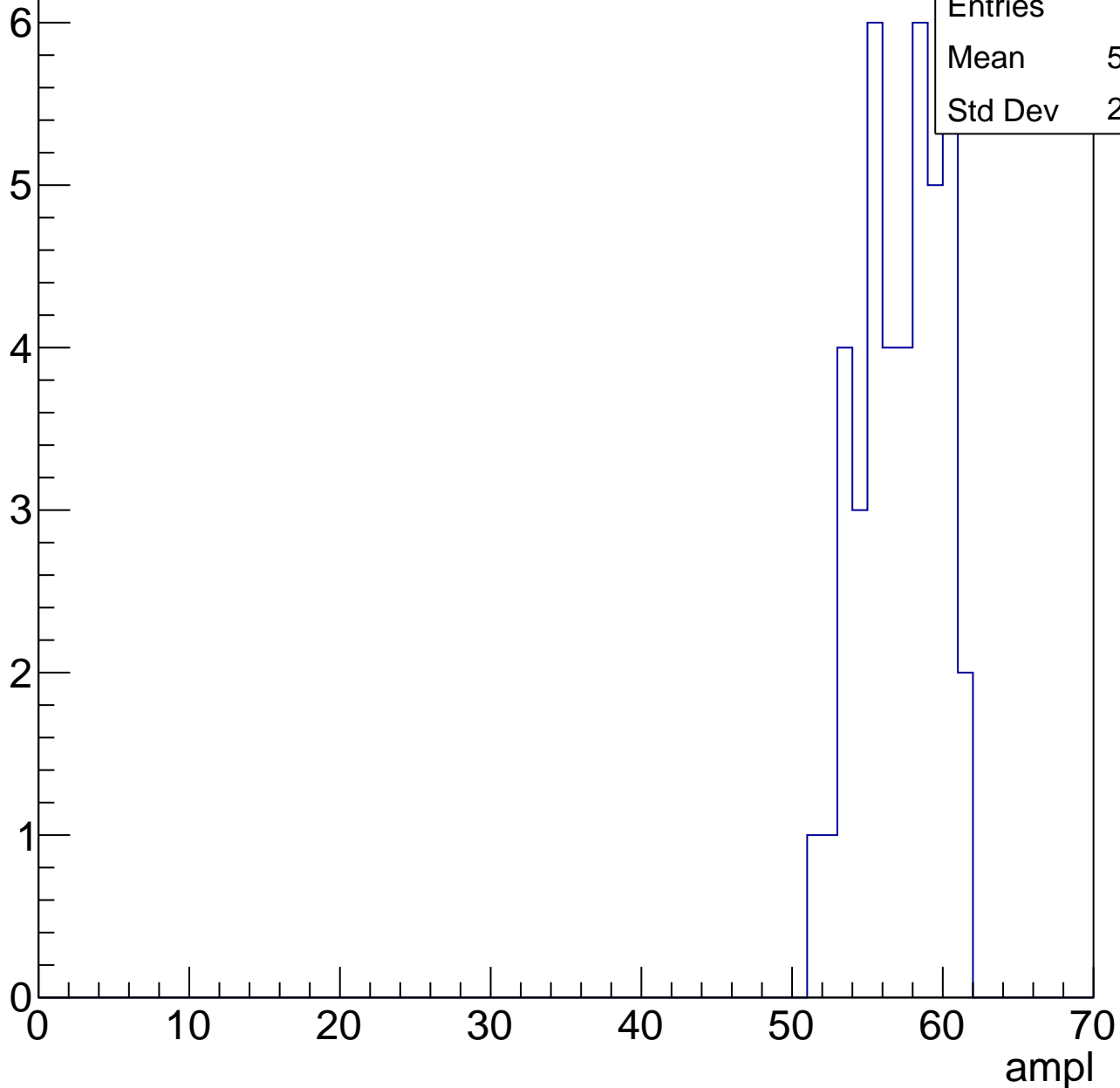
ampl



# B1L003S, U11-ch88, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

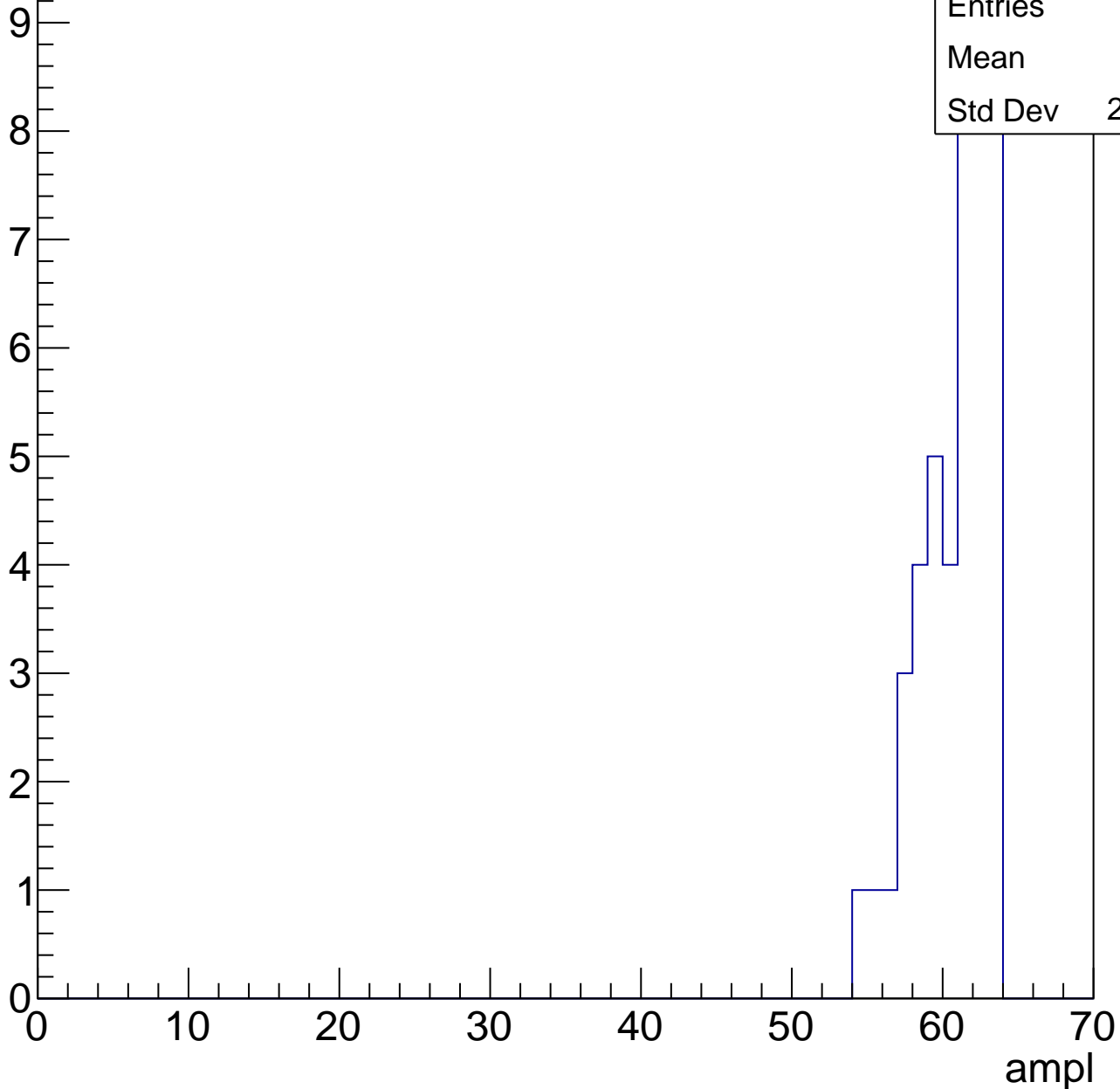
Entry



# B1L003S, U11-ch88, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U11-ch88, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch88, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U11-ch89, adc0

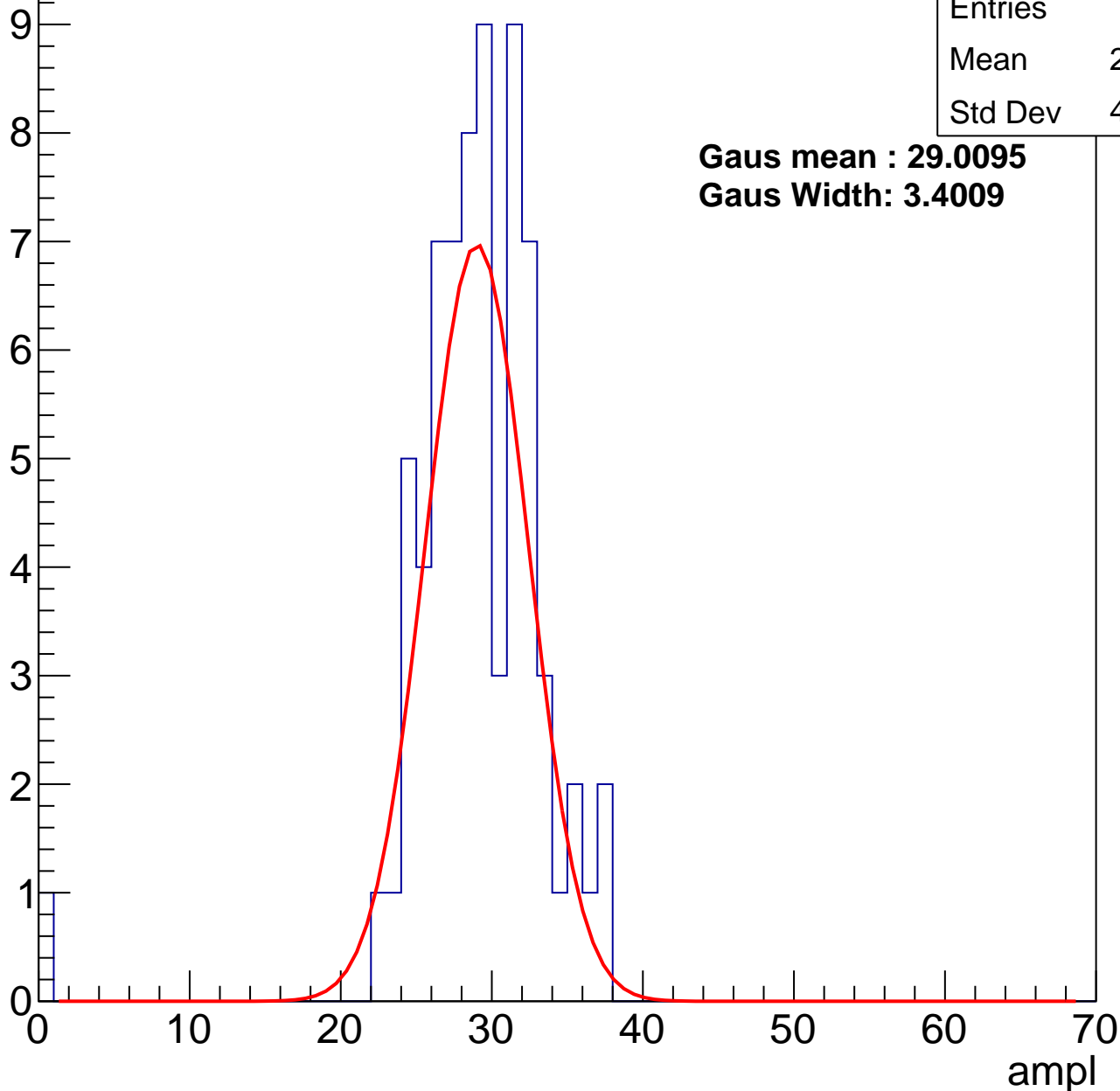
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	71
Mean	28.55
Std Dev	4.782

**Gaus mean : 29.0095**

**Gaus Width: 3.4009**



# B1L003S, U11-ch89, adc1

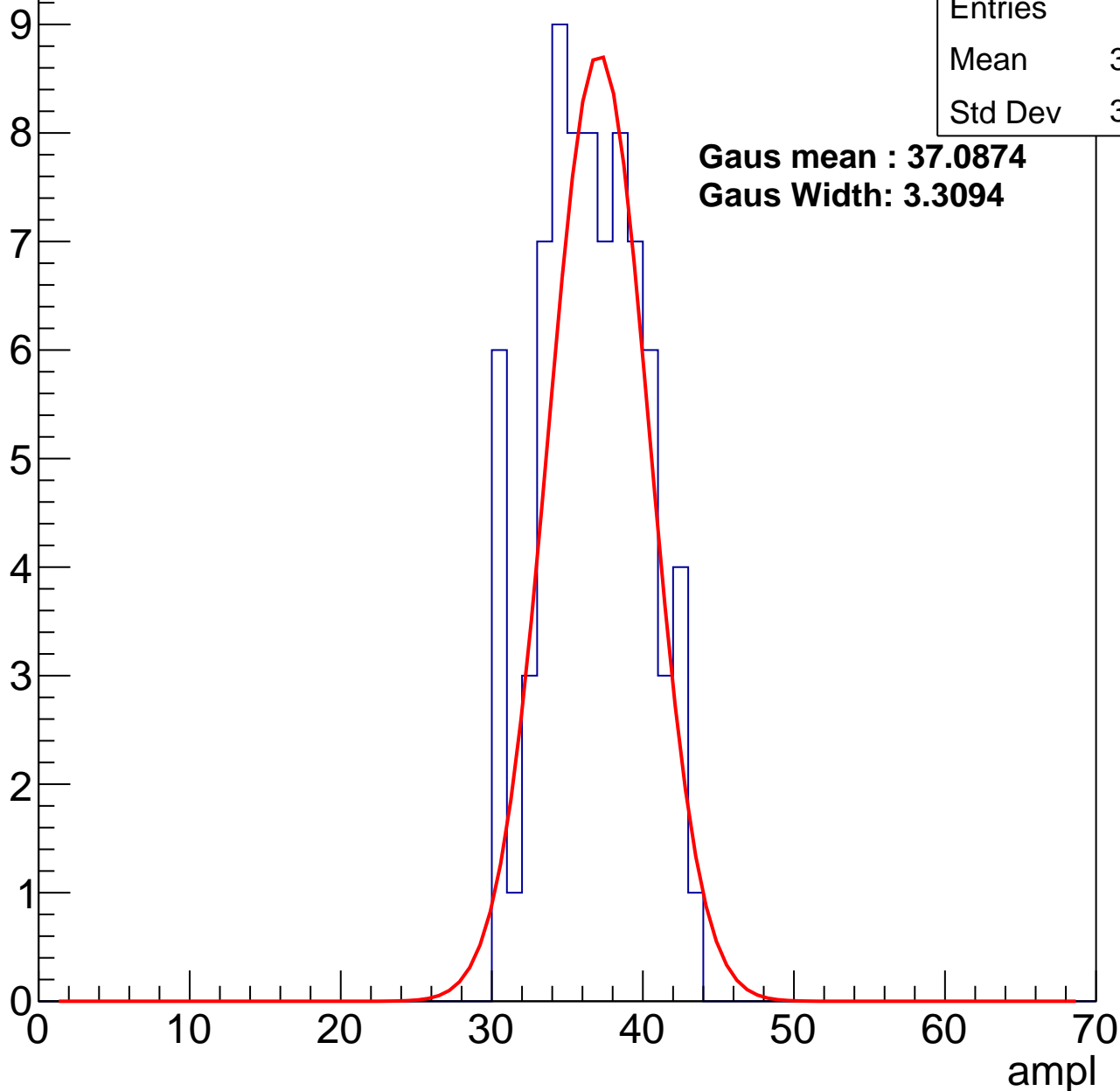
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	78
Mean	36.18
Std Dev	3.319

**Gaus mean : 37.0874**

**Gaus Width: 3.3094**



# B1L003S, U11-ch89, adc2

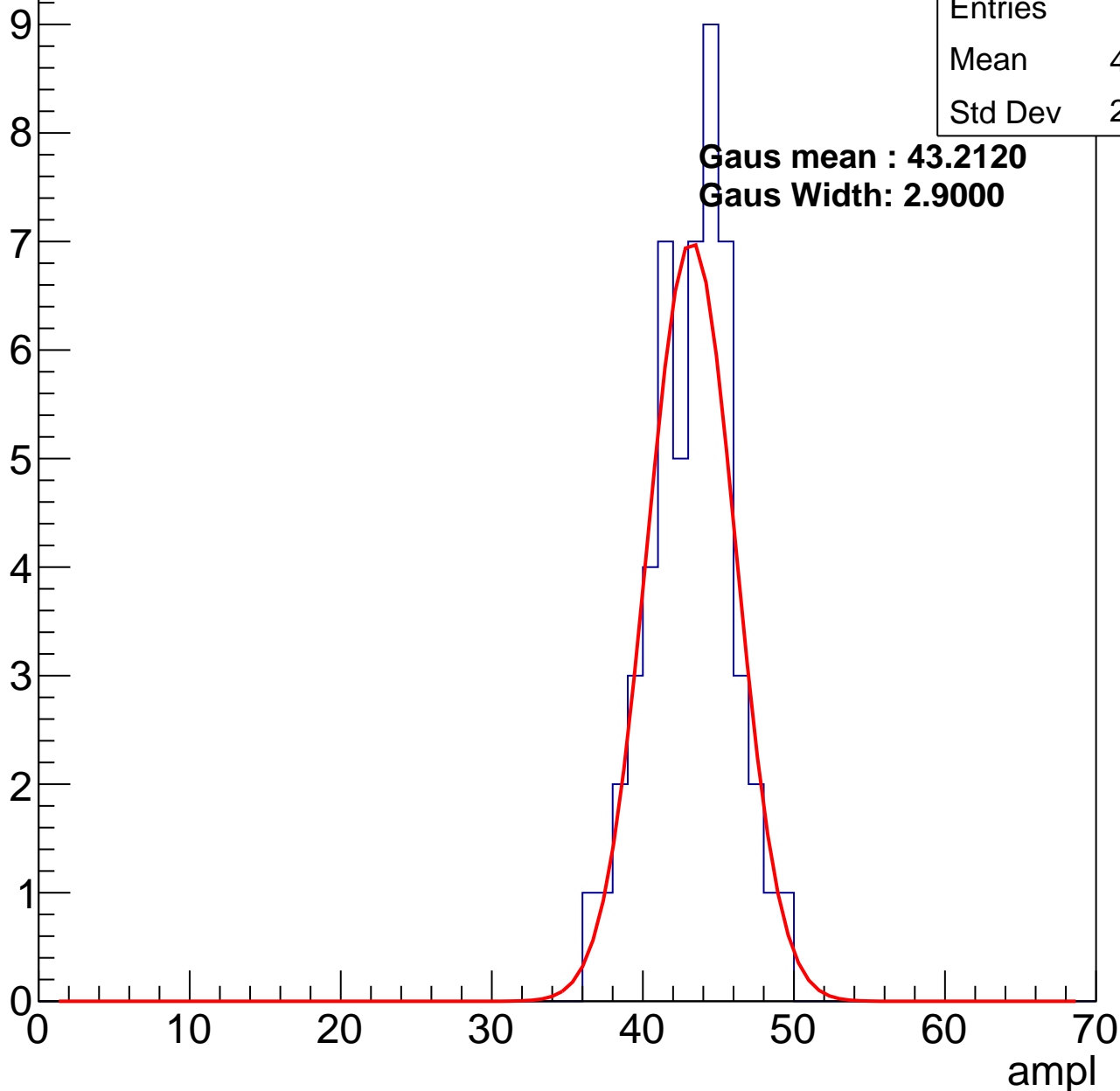
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	42.72
Std Dev	2.763

**Gaus mean : 43.2120**

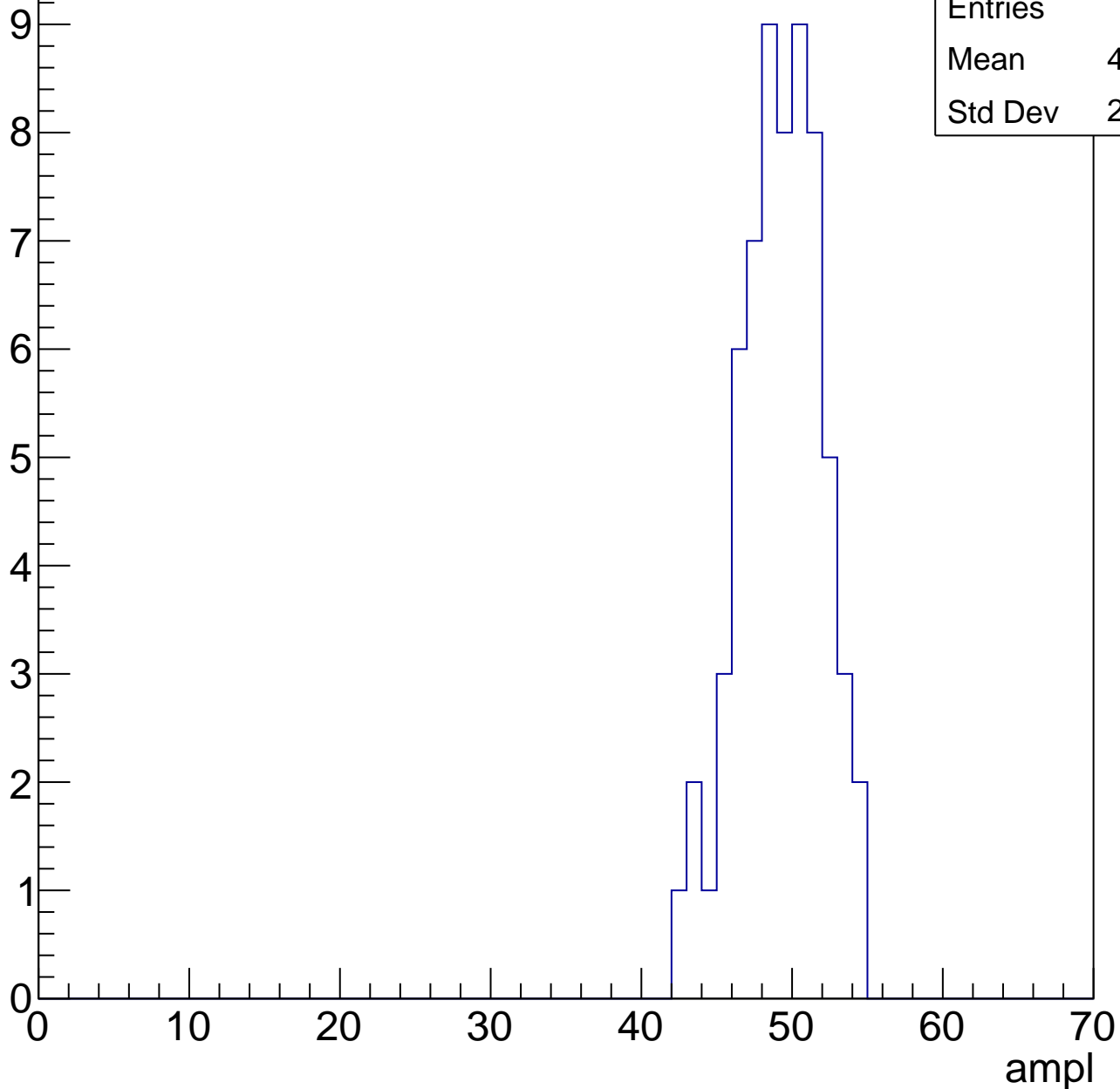
**Gaus Width: 2.9000**



# B1L003S, U11-ch89, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U11-ch89, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	64
Mean	54.98
Std Dev	2.955

Entry

10

8

6

4

2

0

0

10

20

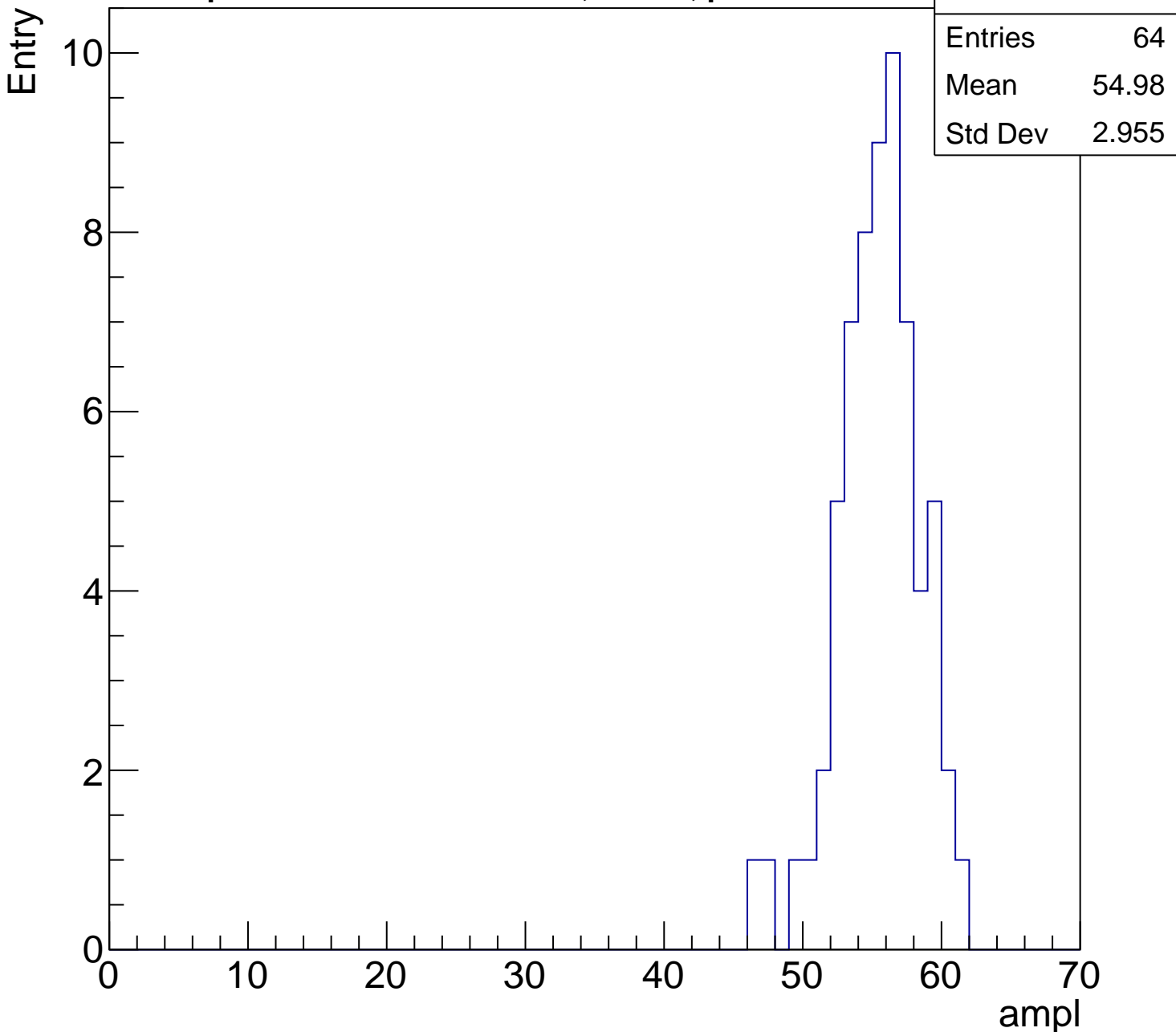
30

40

50

60

ampl

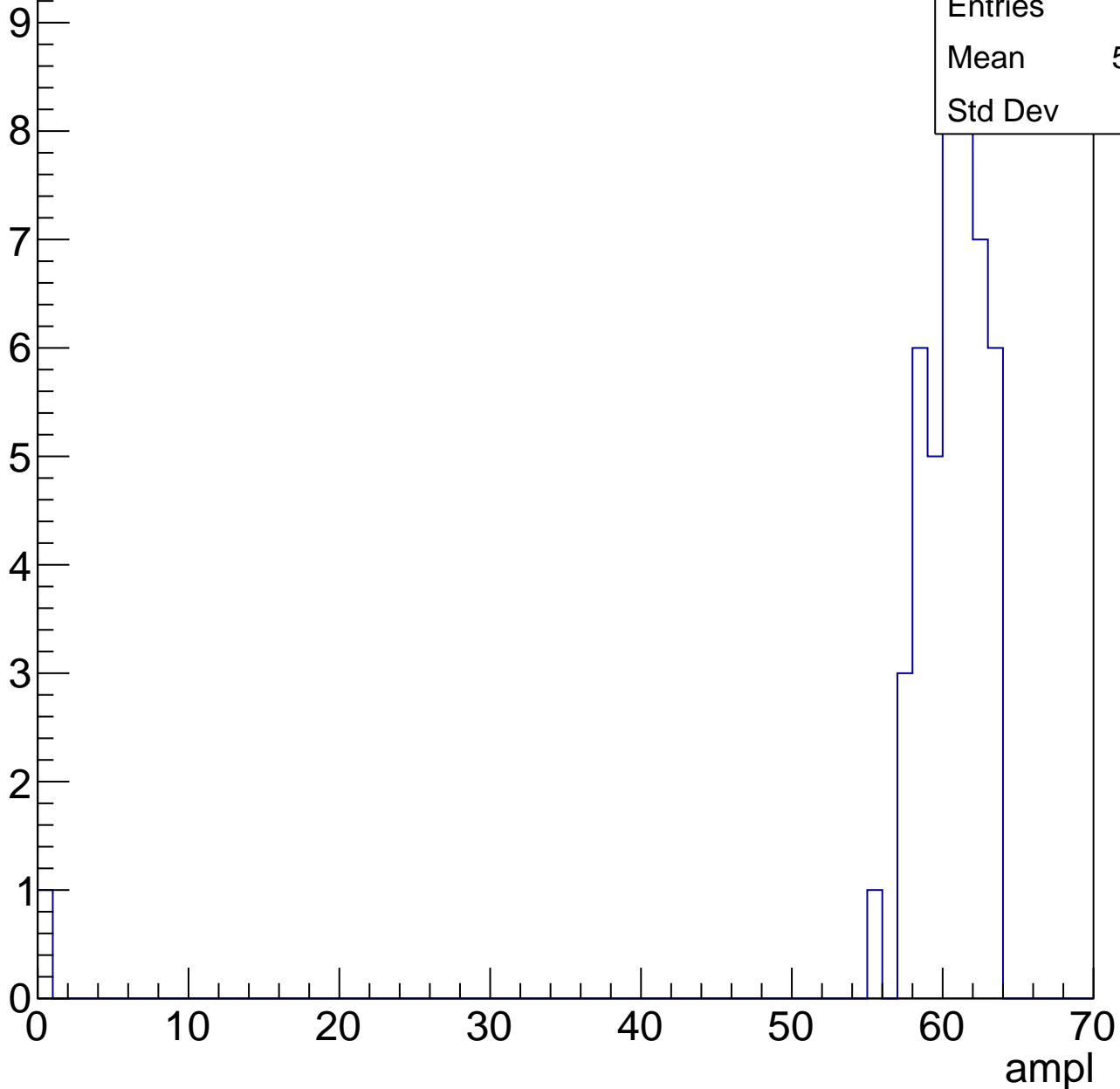


# B1L003S, U11-ch89, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	46
Mean	58.91
Std Dev	8.99



# B1L003S, U11-ch89, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	7
Mean	62.57
Std Dev	0.4949



# B1L003S, U11-ch89, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L003S, U11-ch90, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	76
Mean	30.71
Std Dev	3.576

**Gaus mean : 30.9543**

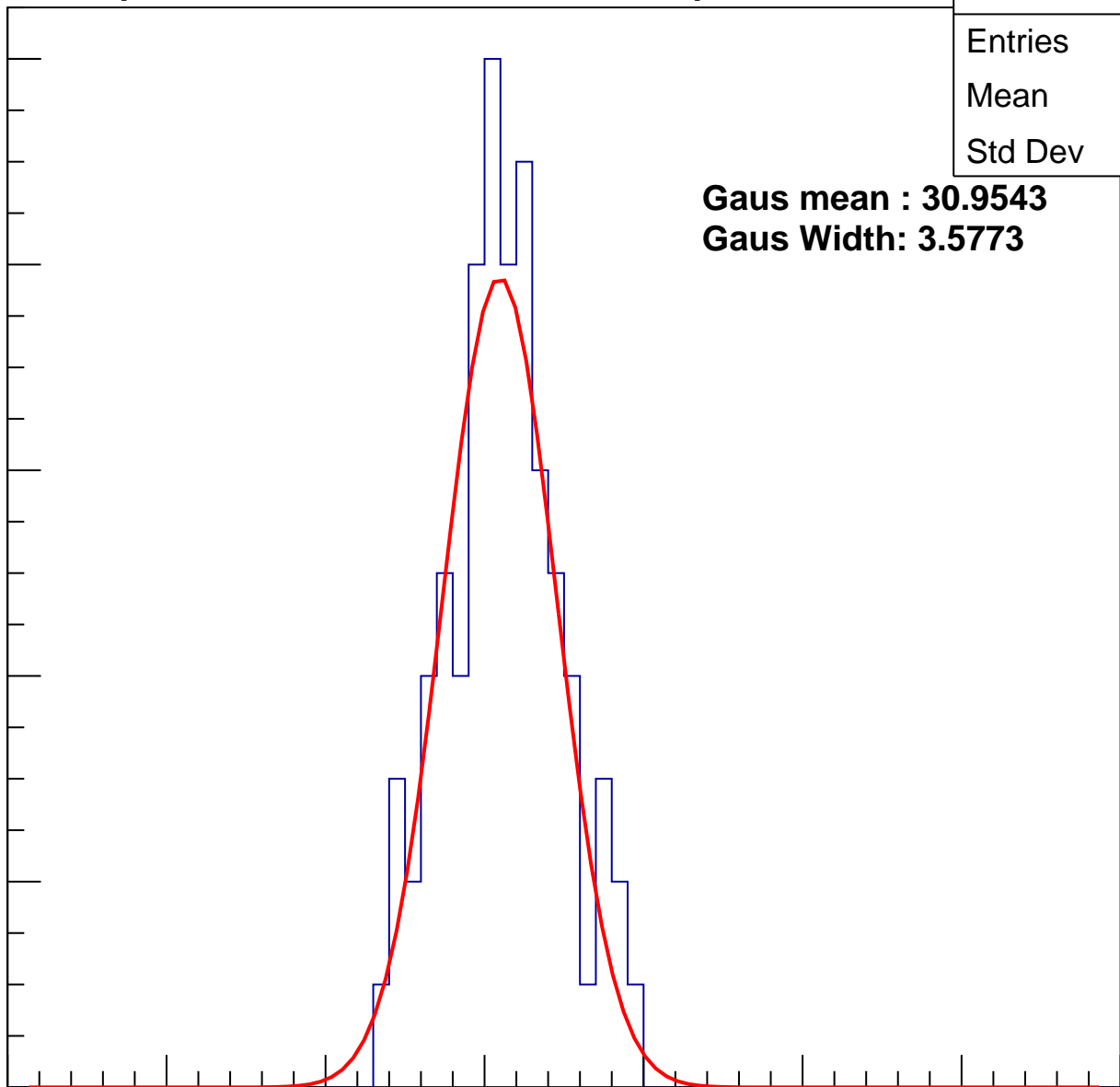
**Gaus Width: 3.5773**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U11-ch90, adc1

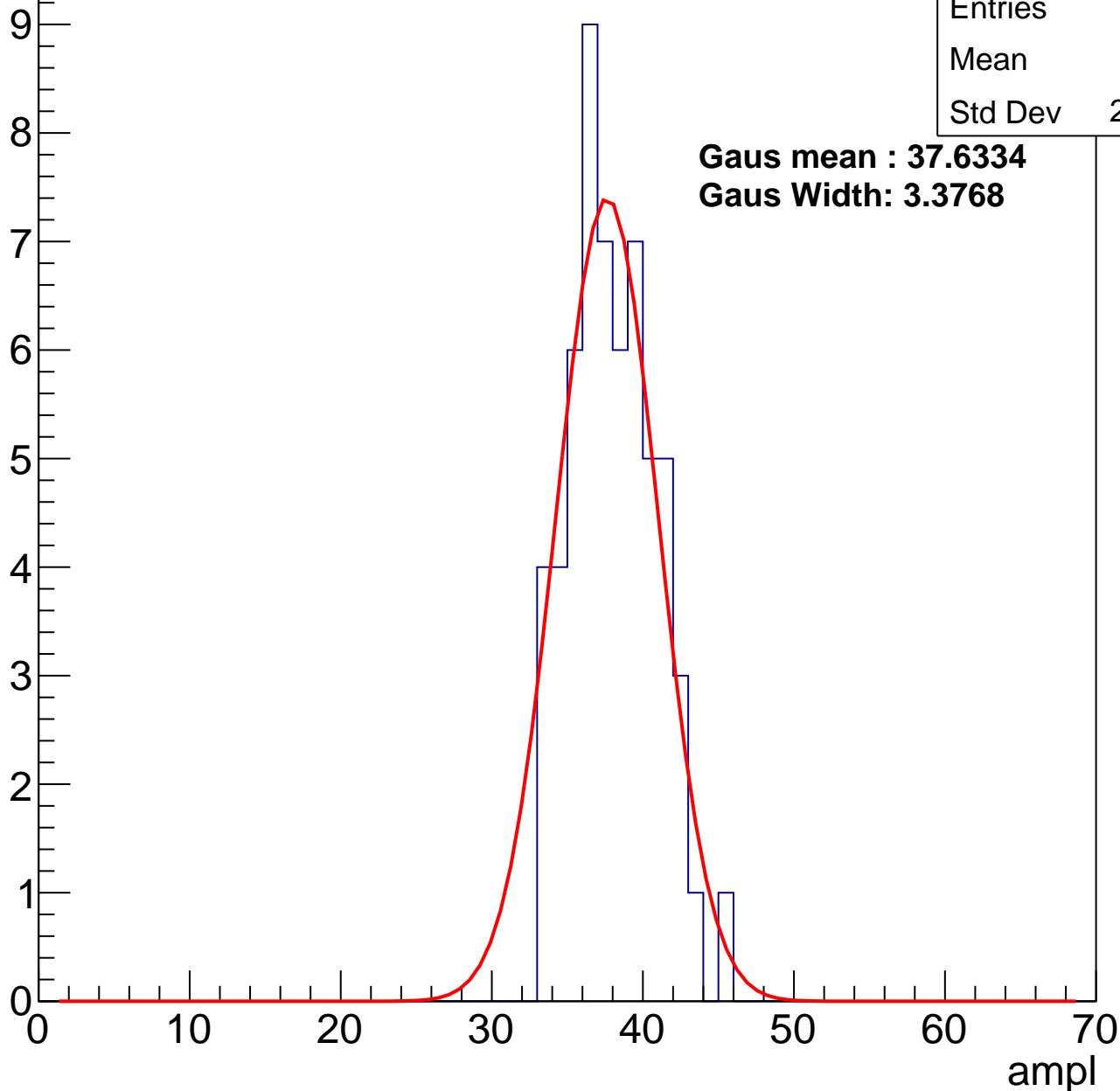
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	37.6
Std Dev	2.773

**Gaus mean : 37.6334**

**Gaus Width: 3.3768**



# B1L003S, U11-ch90, adc2

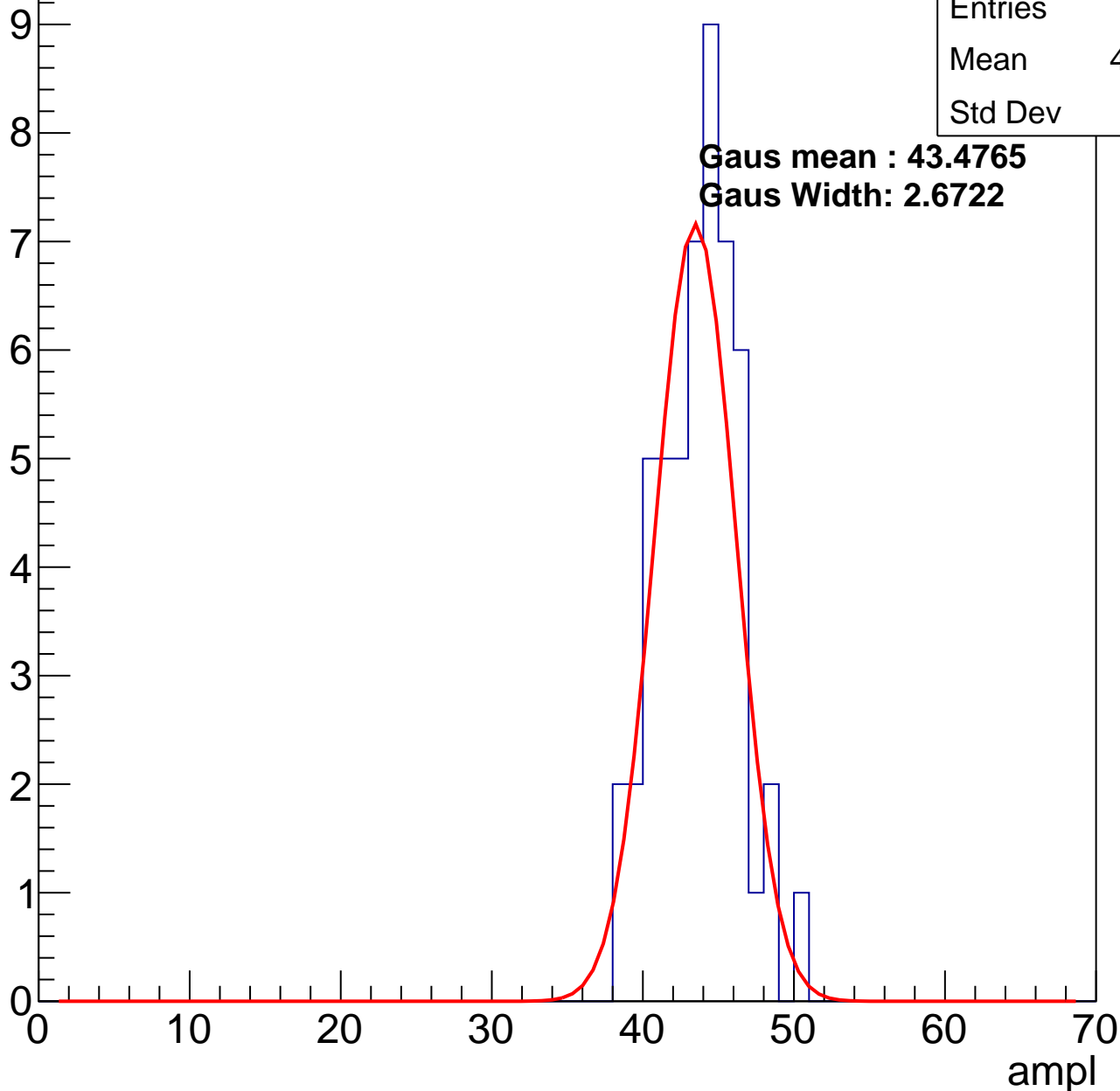
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	52
Mean	43.27
Std Dev	2.61

**Gaus mean : 43.4765**

**Gaus Width: 2.6722**



# B1L003S, U11-ch90, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

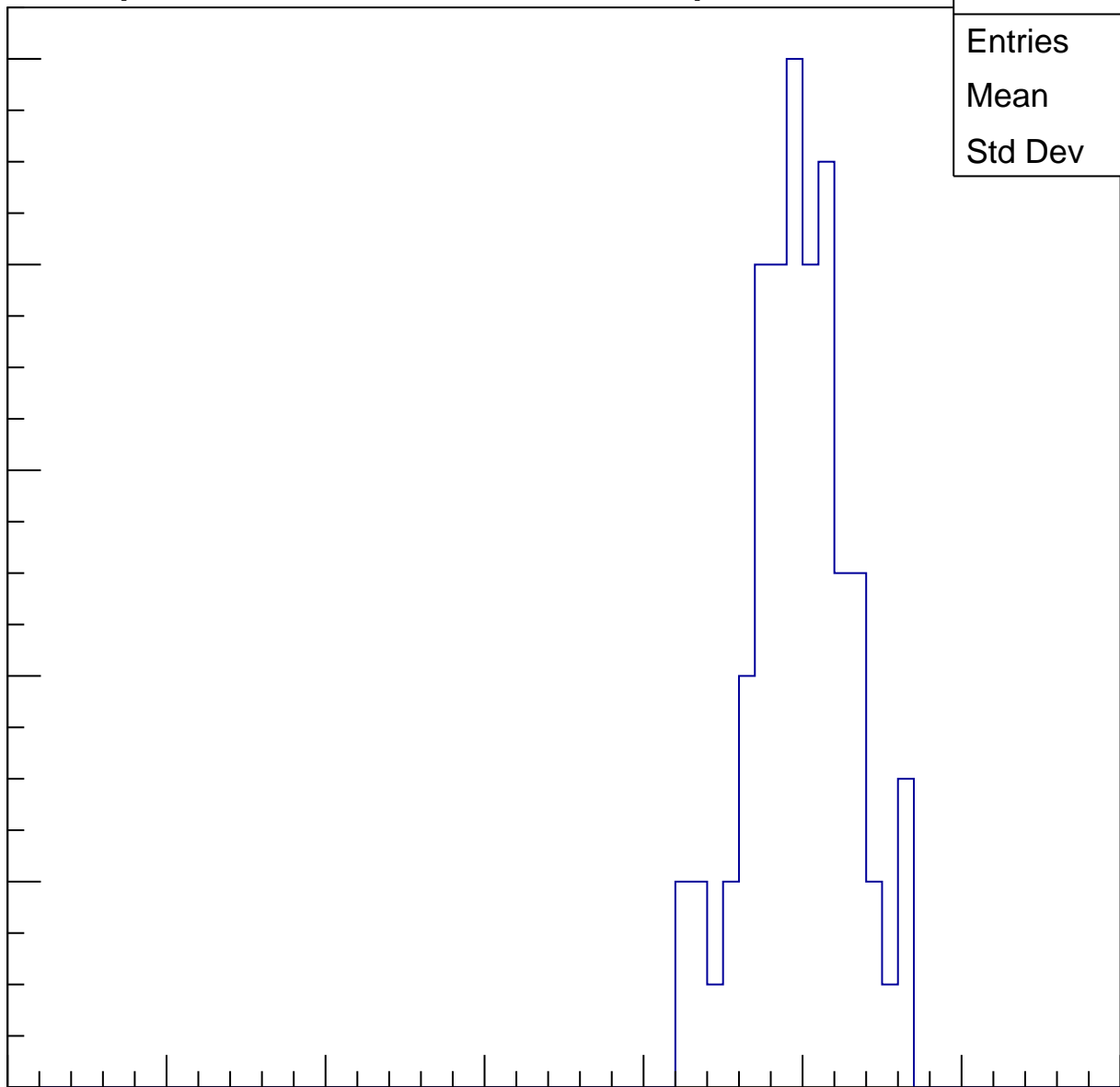
Entries	70
Mean	49.33
Std Dev	3.156

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

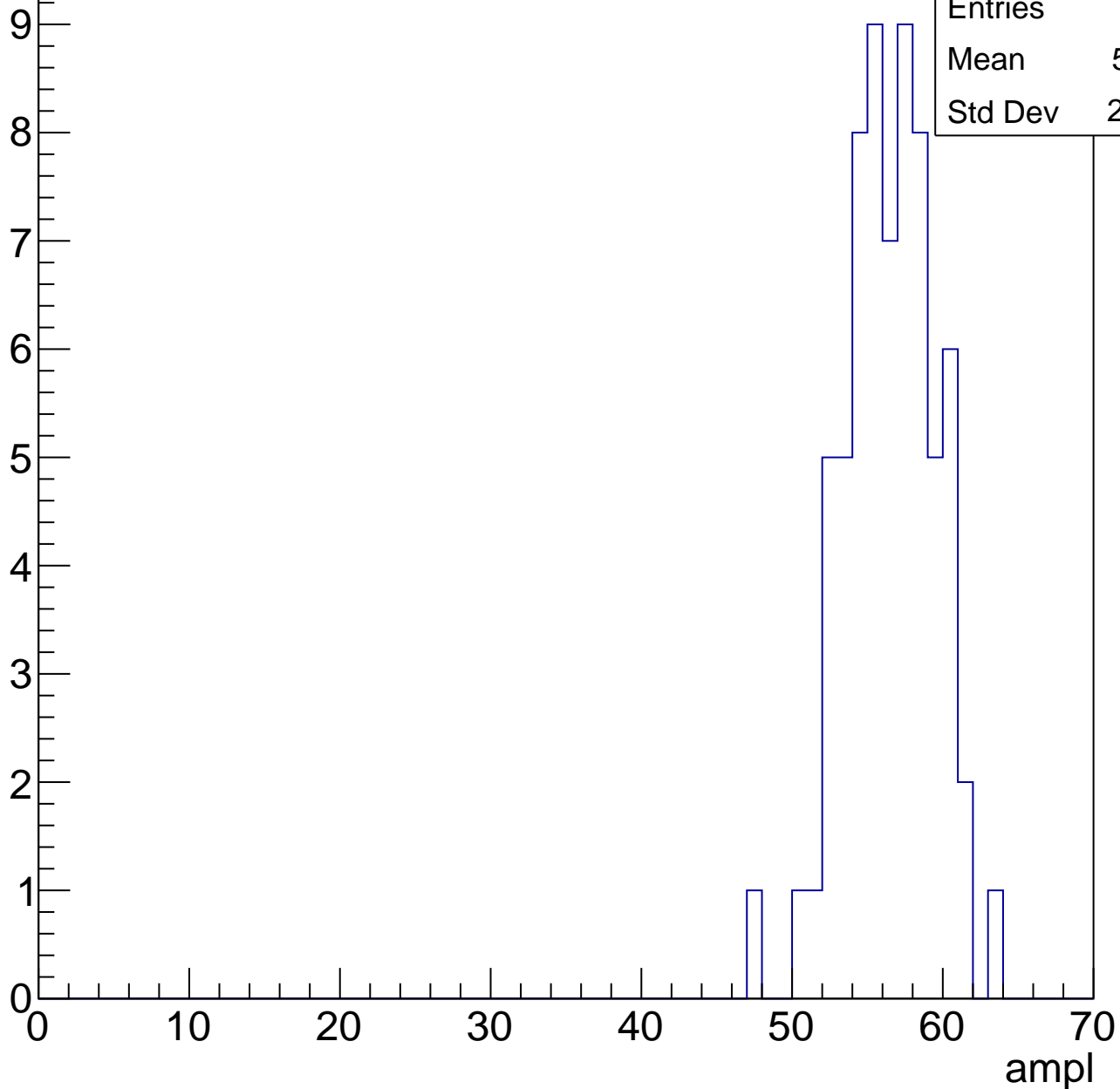
ampl



# B1L003S, U11-ch90, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

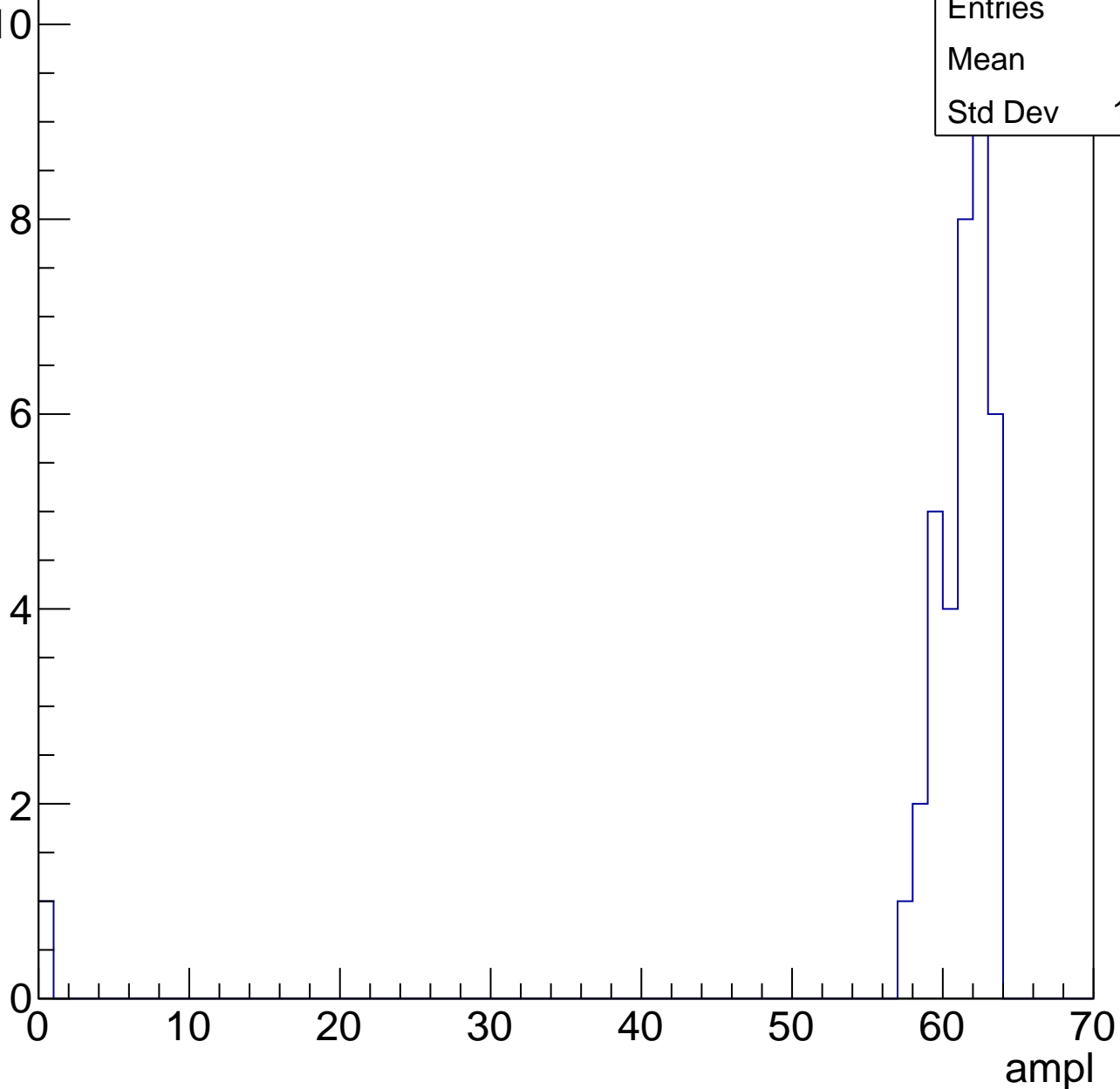


# B1L003S, U11-ch90, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	37
Mean	59.3
Std Dev	10.01



# B1L003S, U11-ch90, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch90, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U11-ch91, adc0

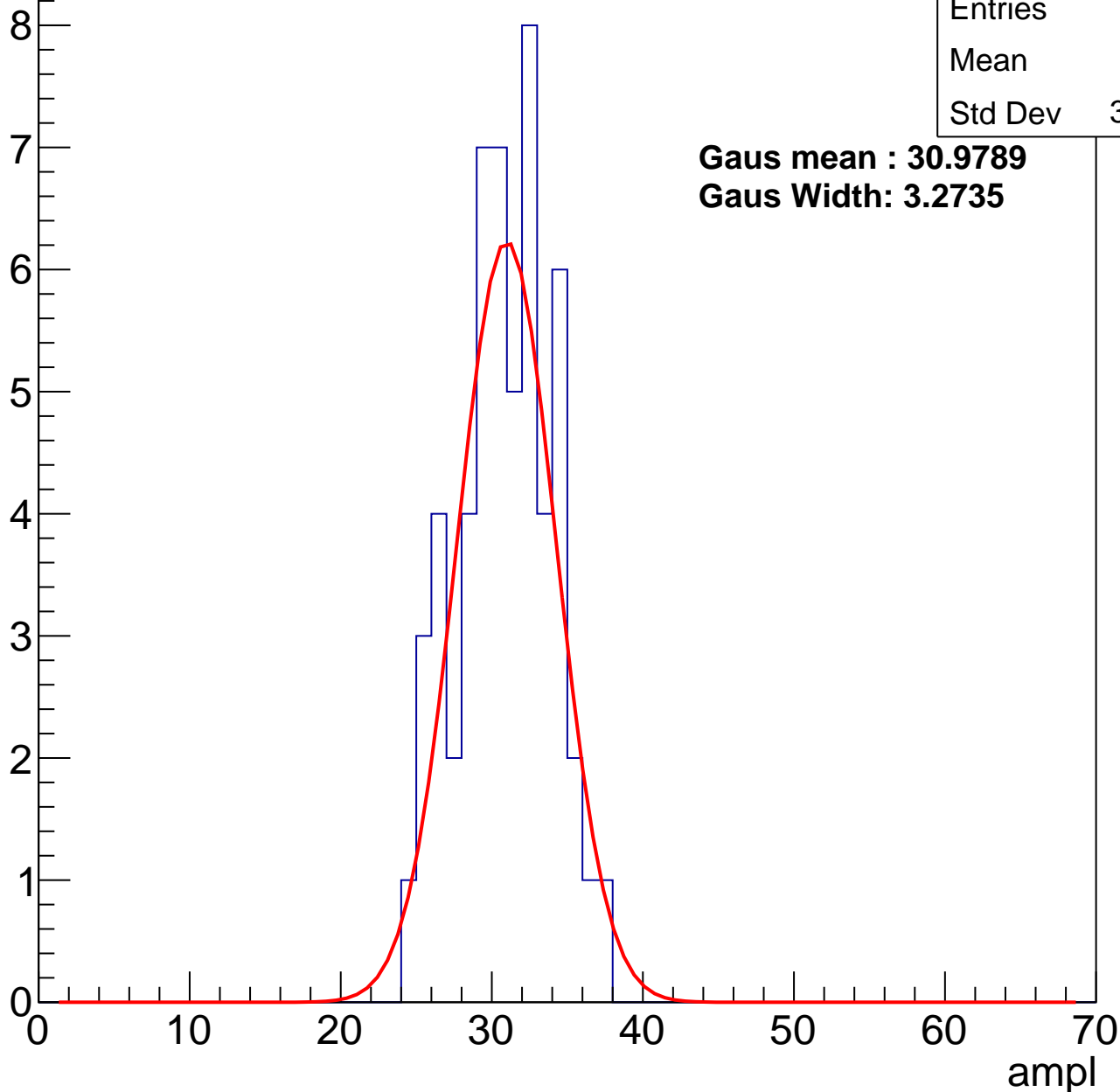
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	30.4
Std Dev	3.049

**Gaus mean : 30.9789**

**Gaus Width: 3.2735**



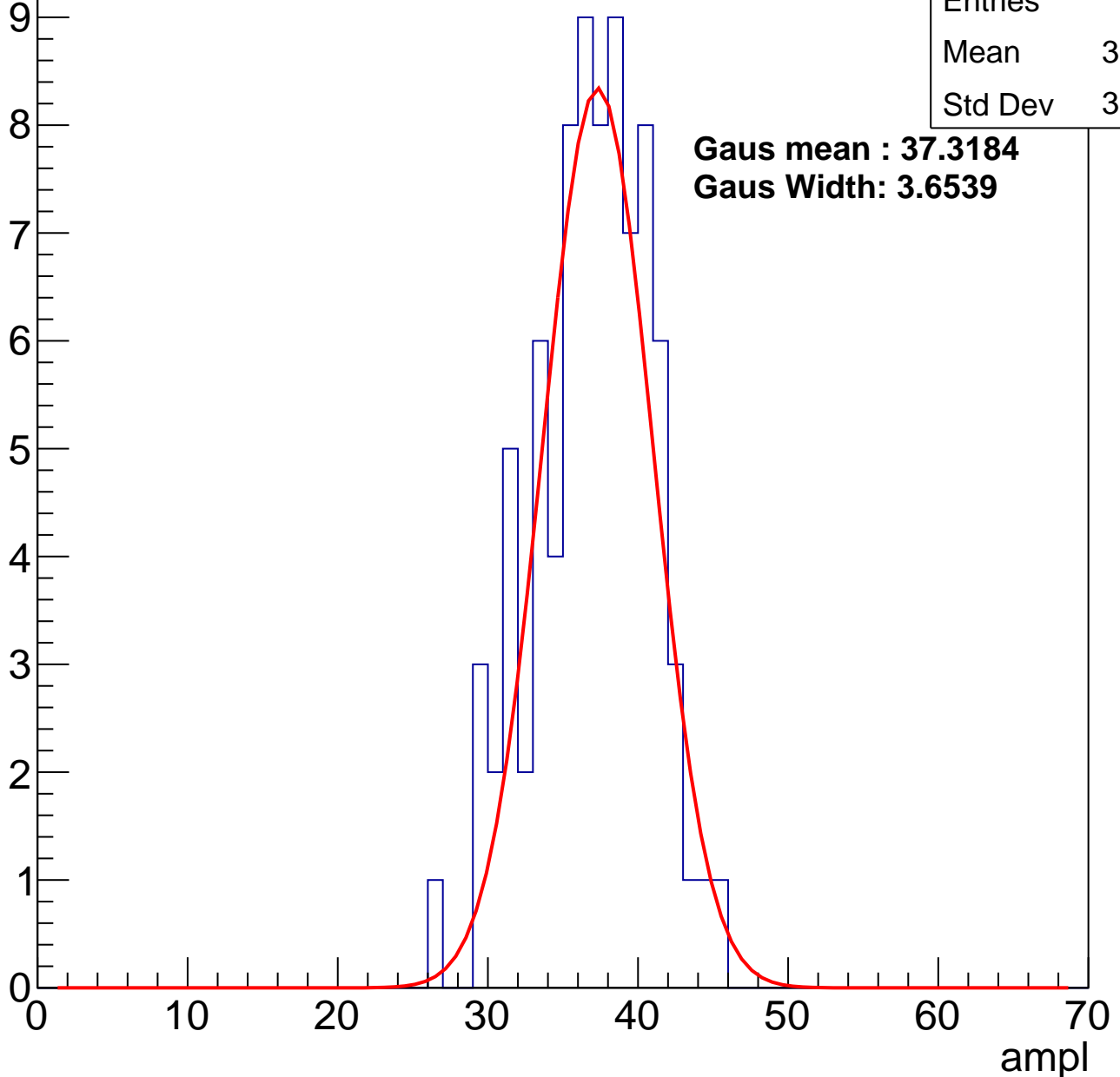
# B1L003S, U11-ch91, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	84
Mean	36.49
Std Dev	3.813

**Gaus mean : 37.3184**  
**Gaus Width: 3.6539**



# B1L003S, U11-ch91, adc2

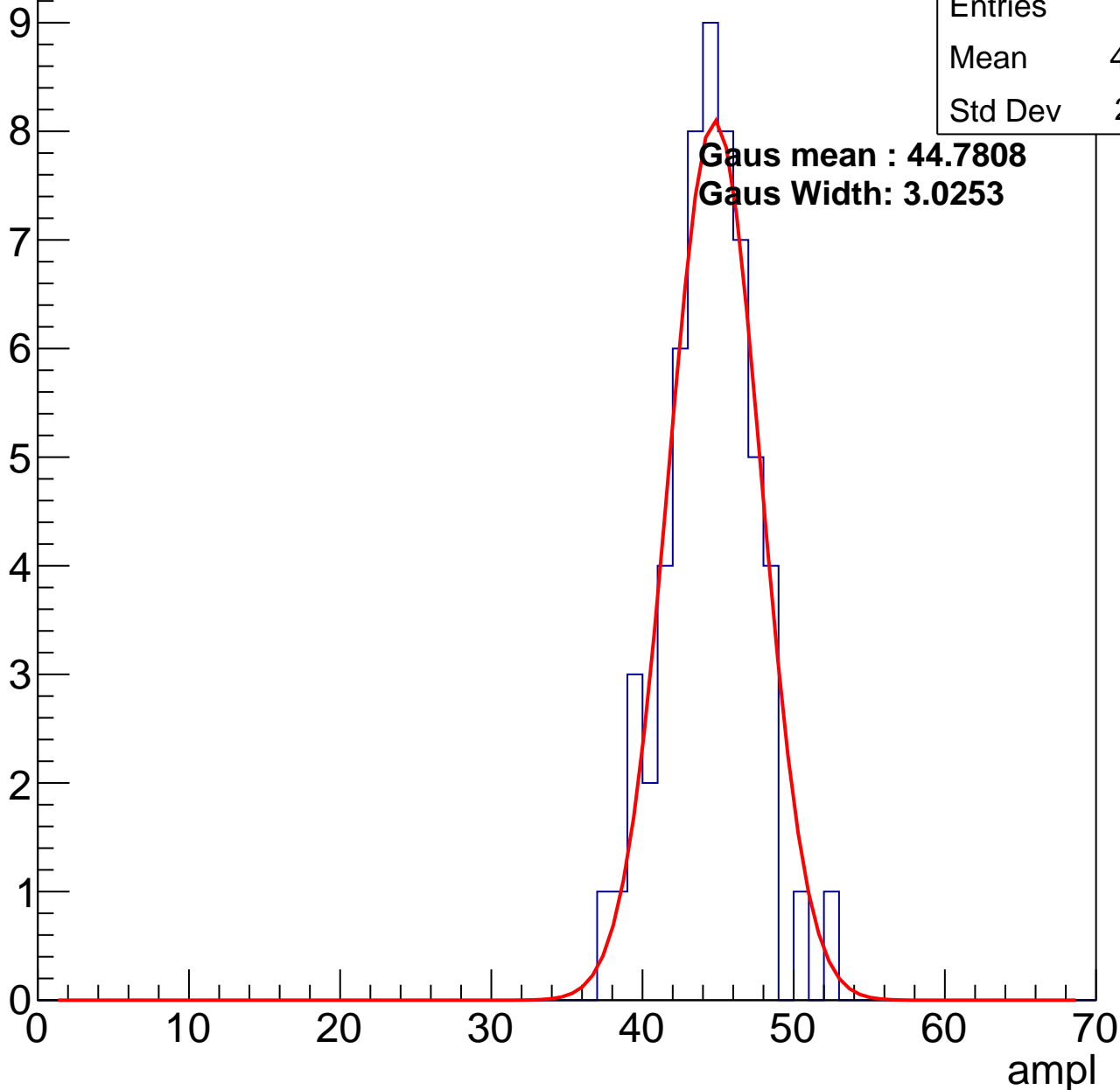
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	43.98
Std Dev	2.901

**Gaus mean : 44.7808**

**Gaus Width: 3.0253**

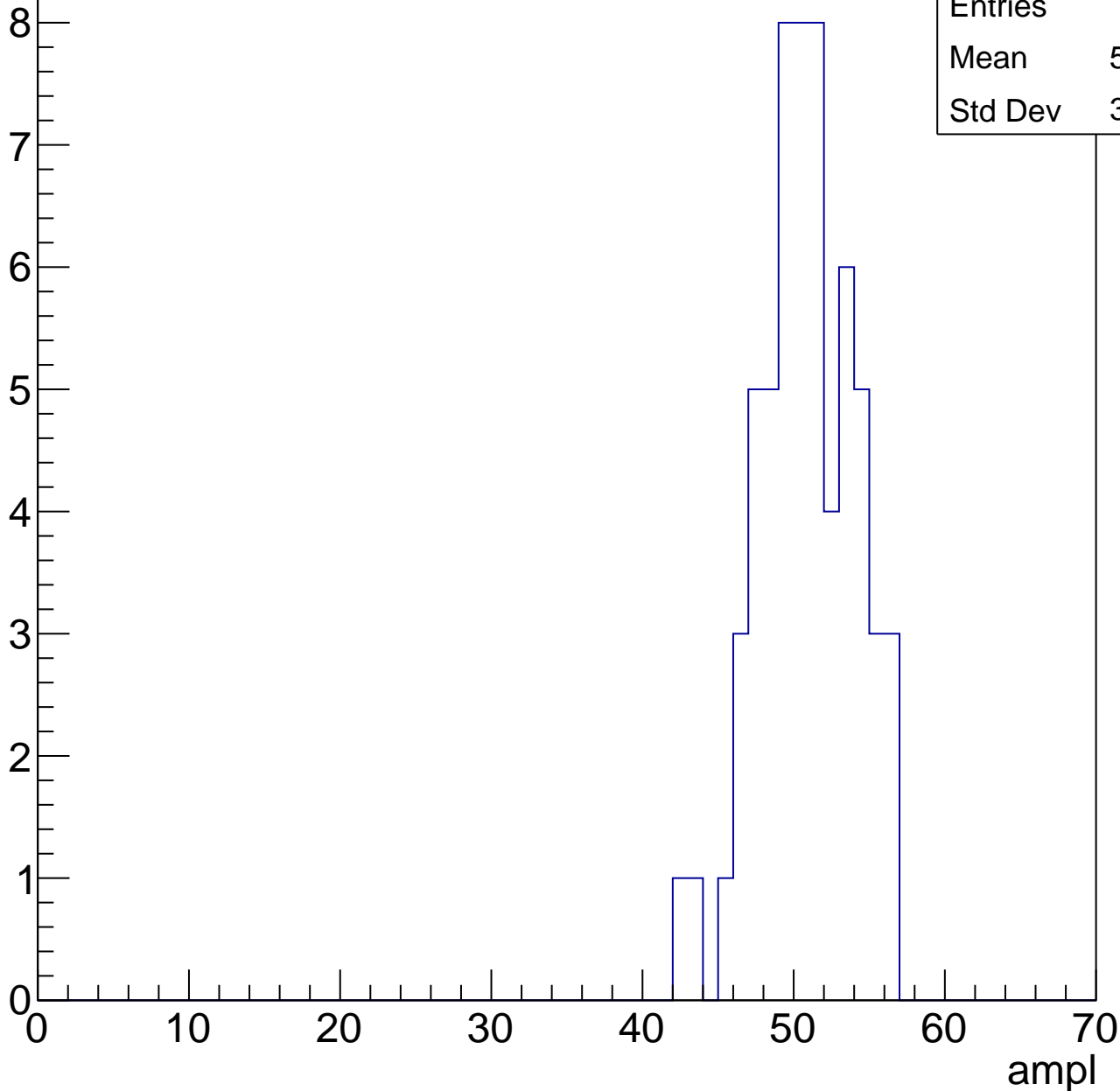


# B1L003S, U11-ch91, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

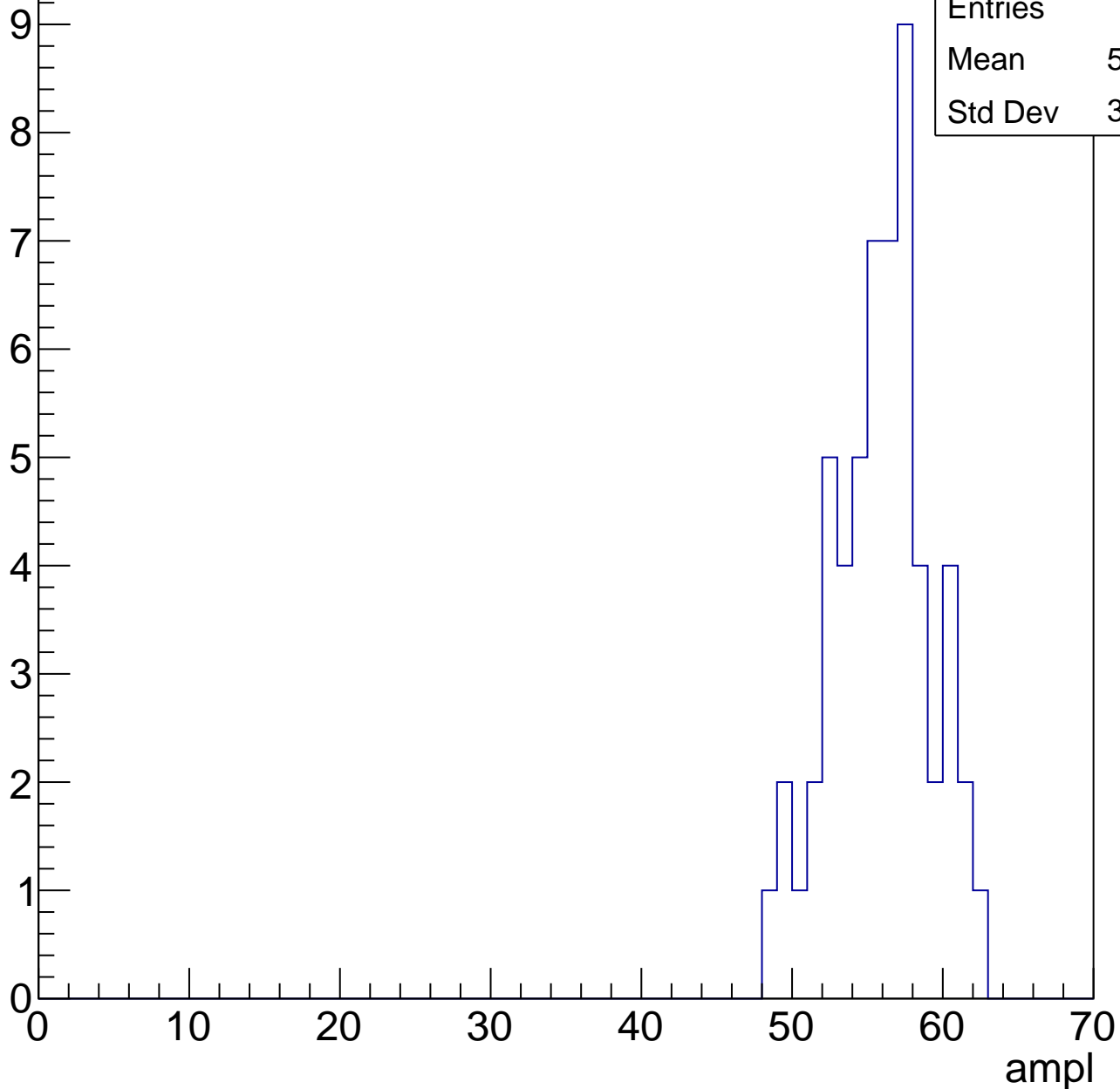
Entries	61
Mean	50.36
Std Dev	3.115



# B1L003S, U11-ch91, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



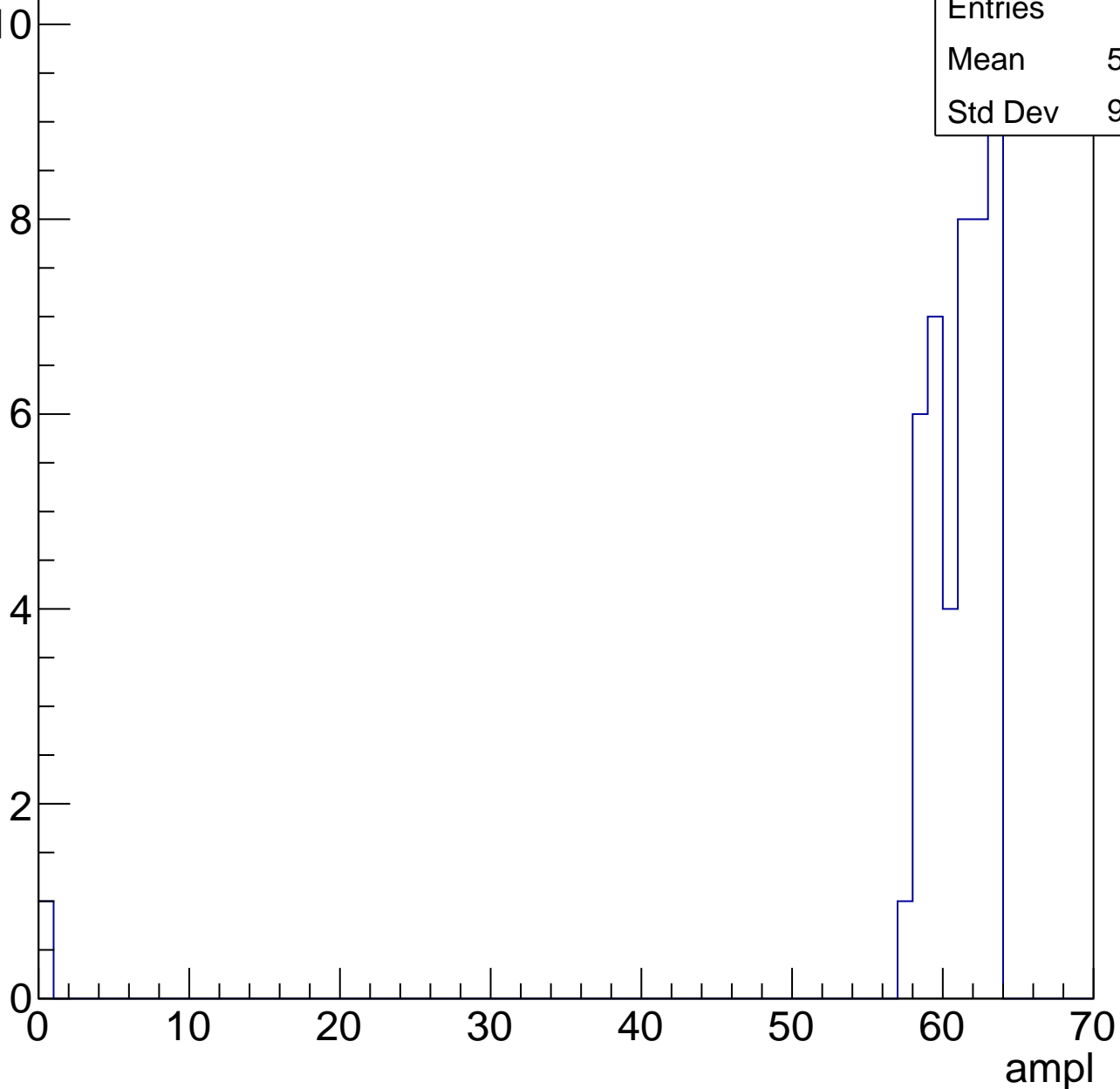
Entries	56
Mean	55.43
Std Dev	3.178

# B1L003S, U11-ch91, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	45
Mean	59.38
Std Dev	9.132



# B1L003S, U11-ch91, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	60.25
Std Dev	1.09

ampl

0 10 20 30 40 50 60 70



# B1L003S, U11-ch91, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

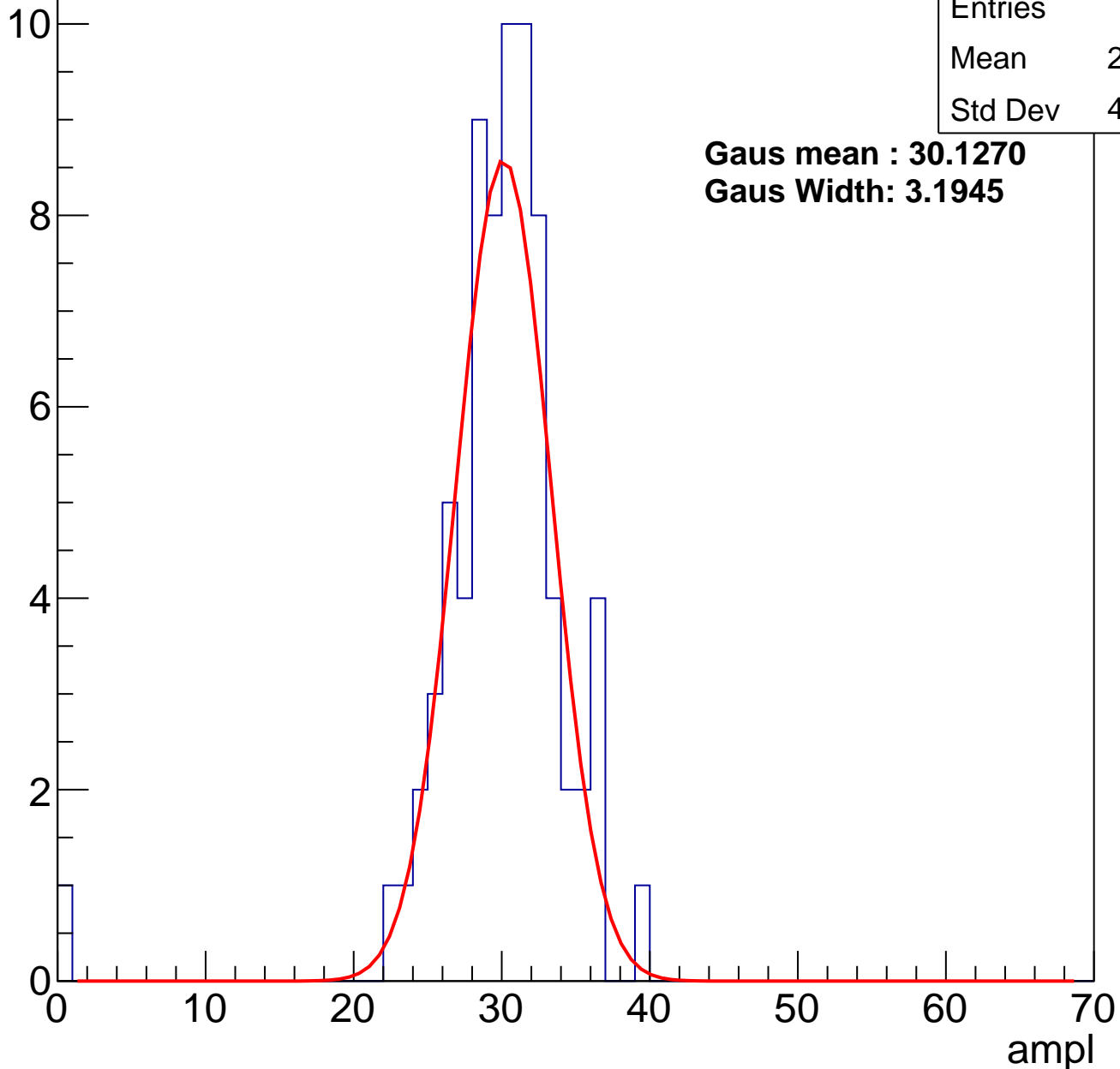
# B1L003S, U11-ch92, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	75
Mean	29.45
Std Dev	4.737

**Gaus mean : 30.1270**  
**Gaus Width: 3.1945**

Entry



# B1L003S, U11-ch92, adc1

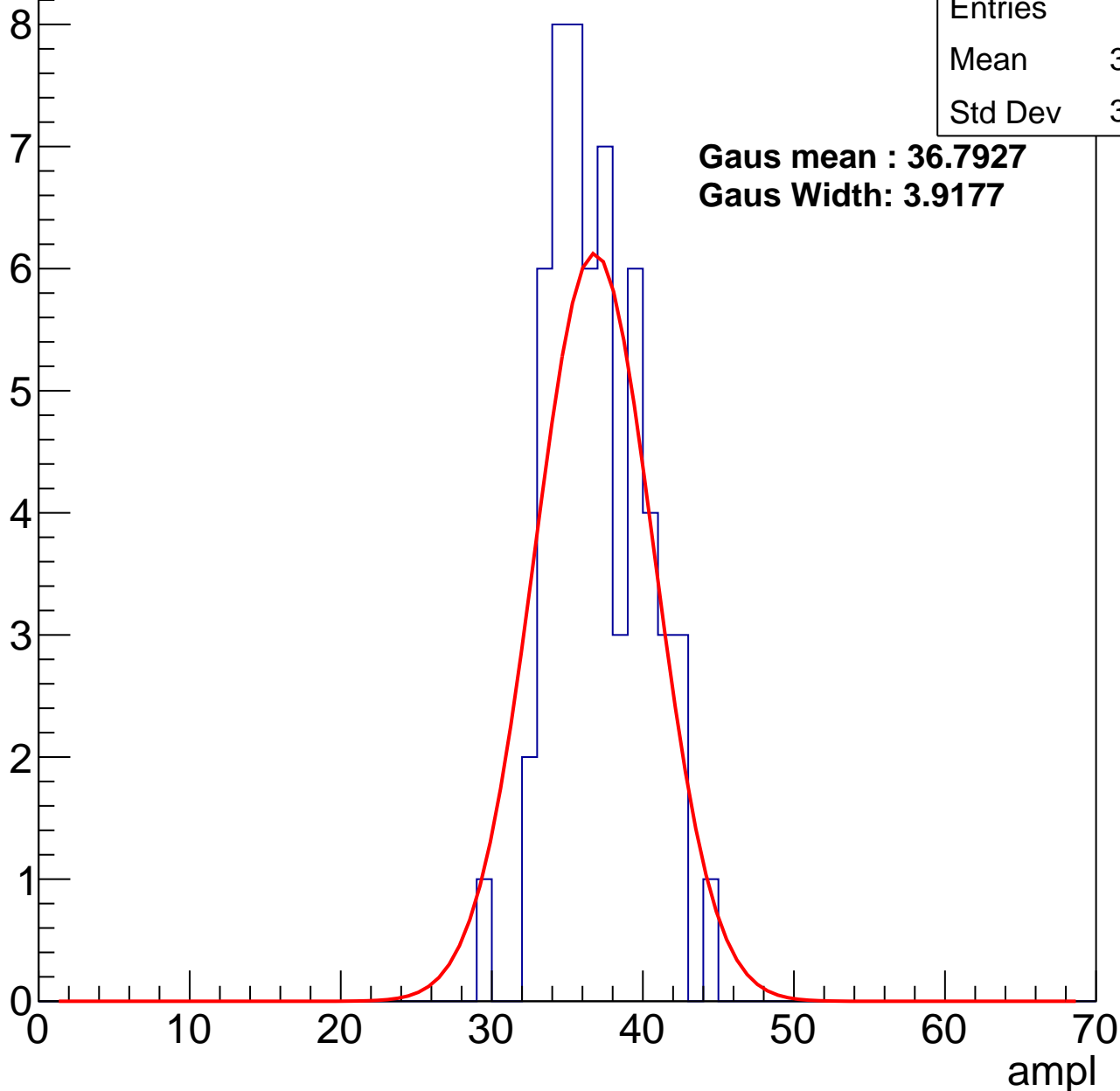
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	36.53
Std Dev	3.058

**Gaus mean : 36.7927**

**Gaus Width: 3.9177**



# B1L003S, U11-ch92, adc2

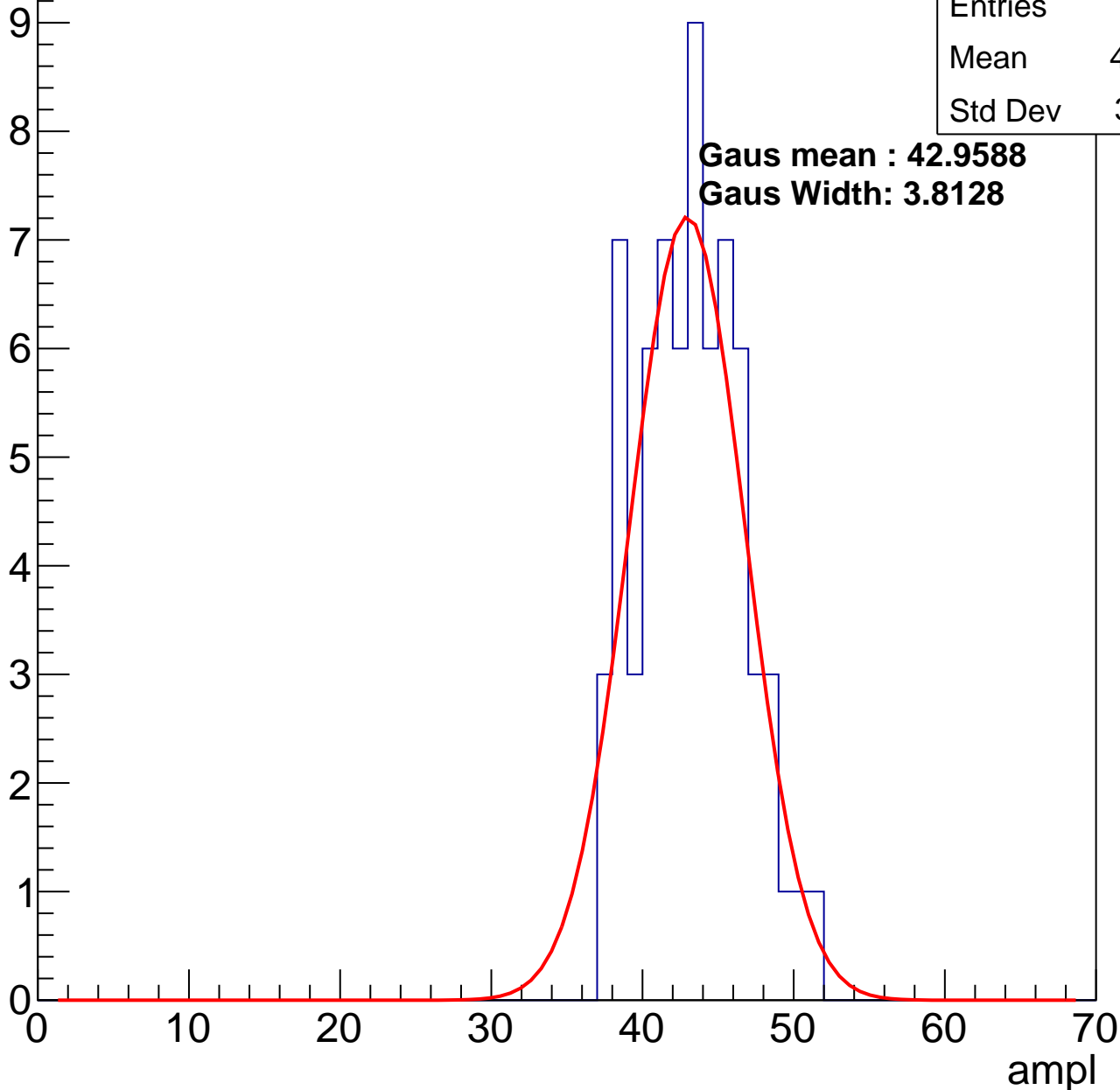
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	42.75
Std Dev	3.351

**Gaus mean : 42.9588**

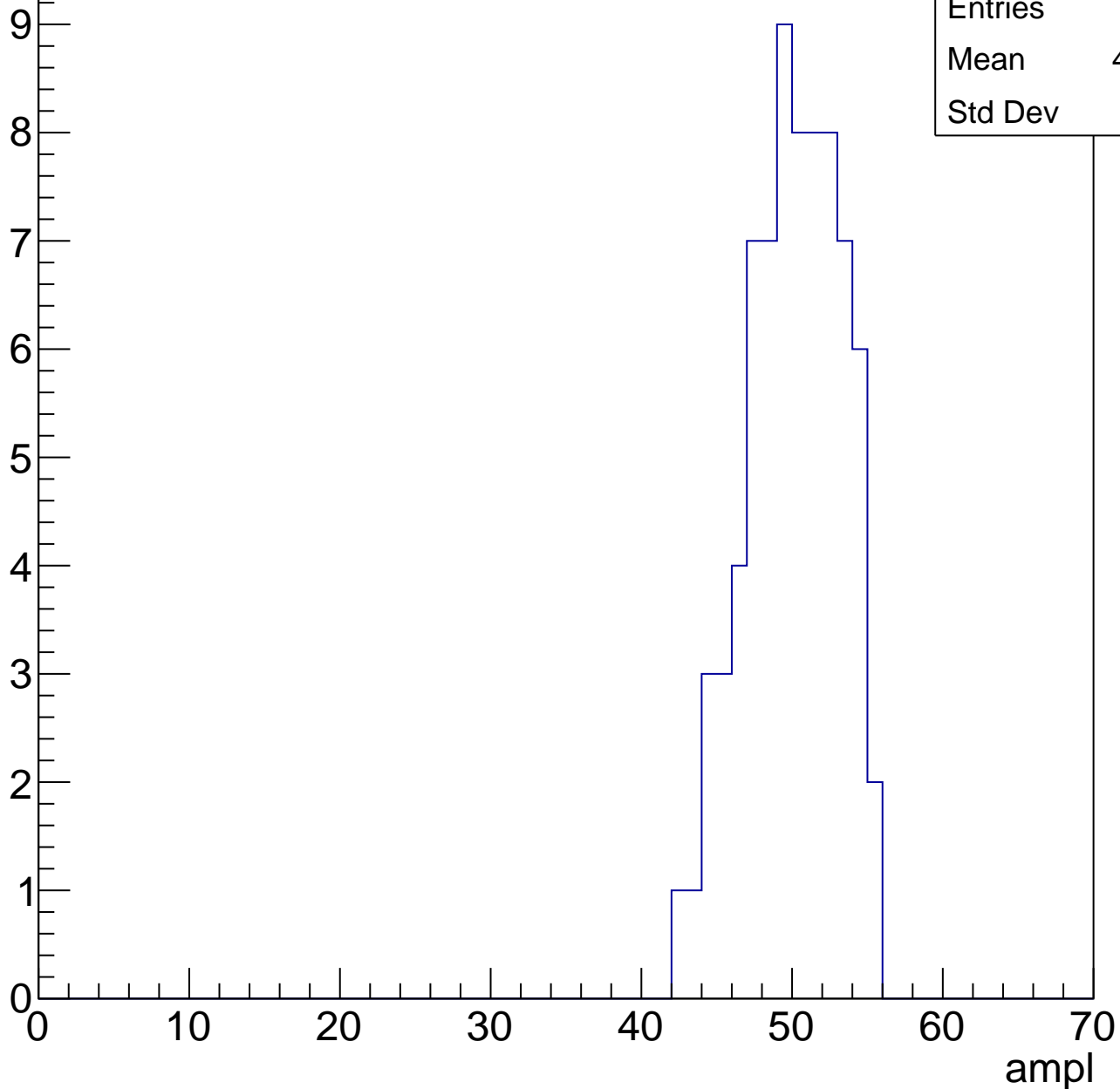
**Gaus Width: 3.8128**



# B1L003S, U11-ch92, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U11-ch92, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	52
Mean	56.29
Std Dev	2.397

Entry

10

8

6

4

2

0

0

10

20

30

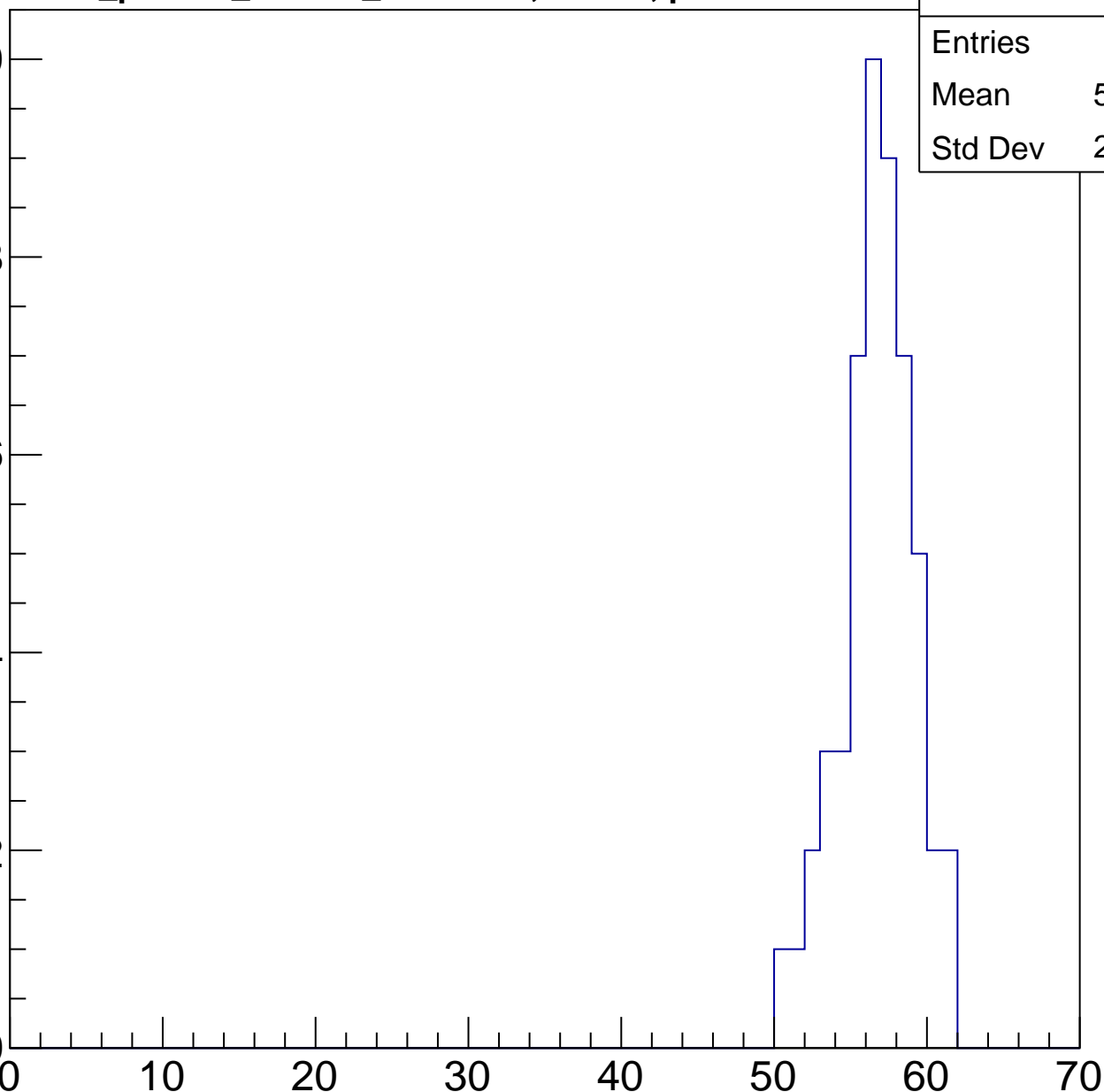
40

50

ampl

60

70

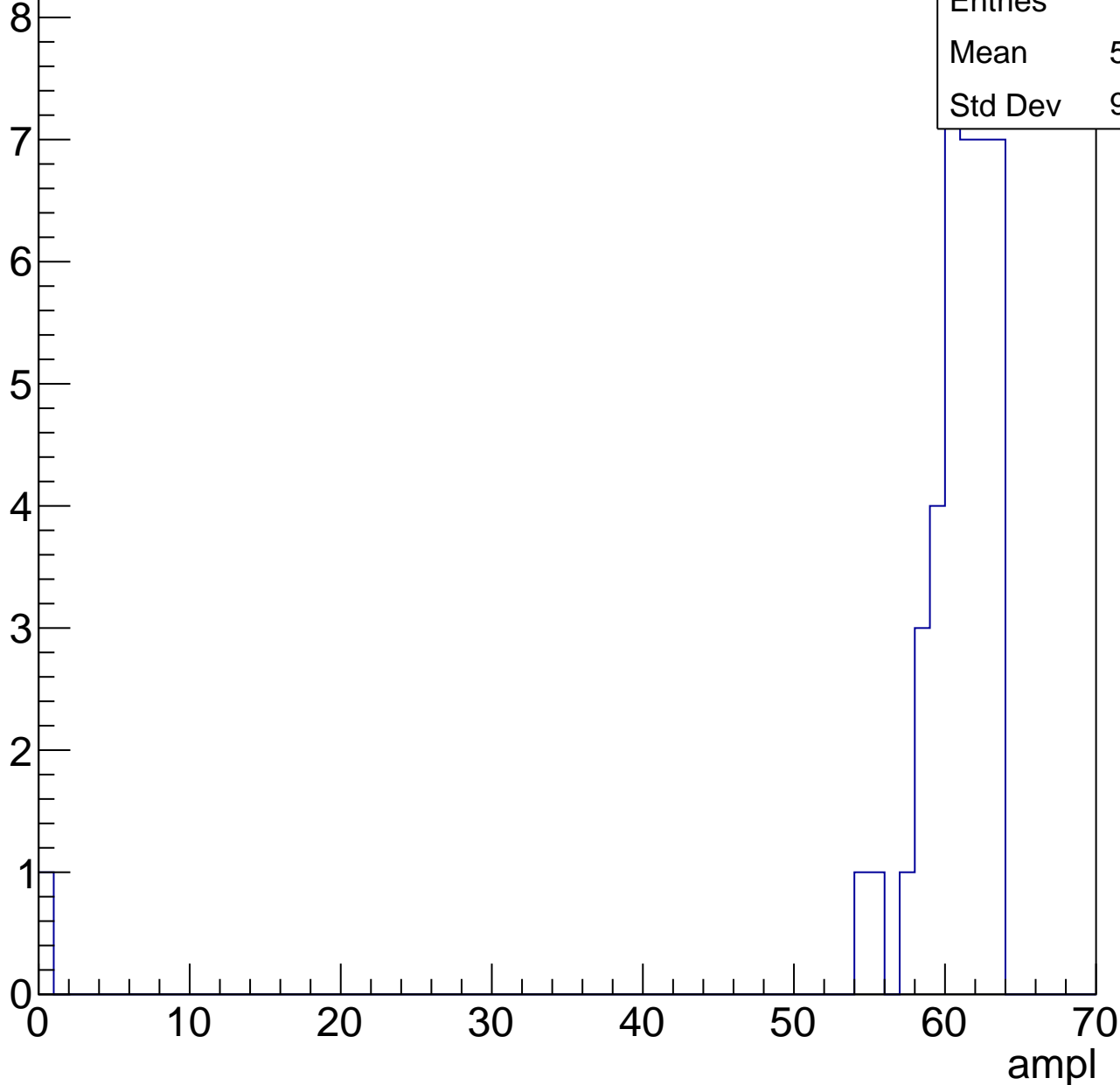


# B1L003S, U11-ch92, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

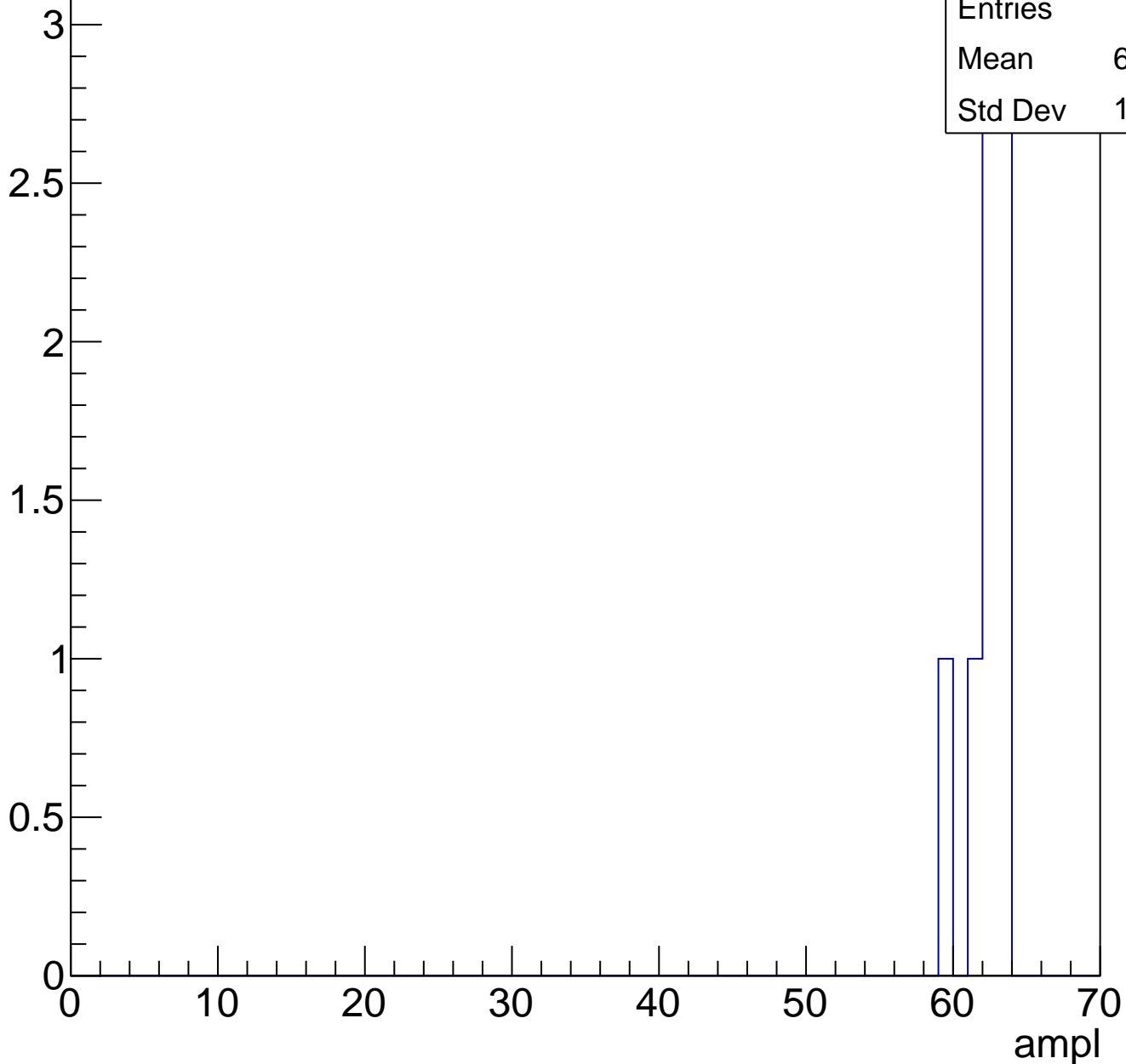
Entries	40
Mean	58.95
Std Dev	9.669



# B1L003S, U11-ch92, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch92, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U11-ch93, adc0

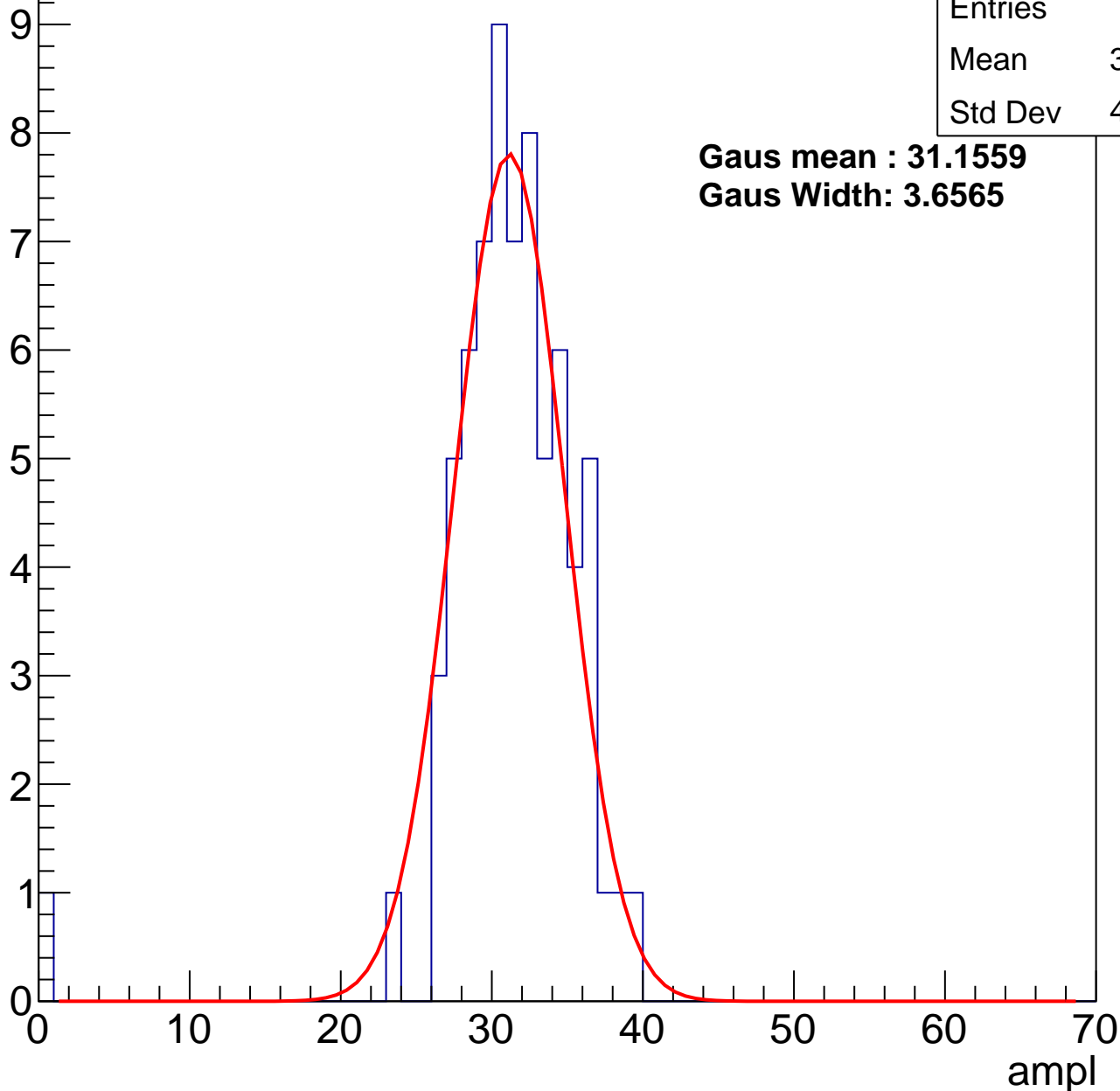
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	30.76
Std Dev	4.909

**Gaus mean : 31.1559**

**Gaus Width: 3.6565**



# B1L003S, U11-ch93, adc1

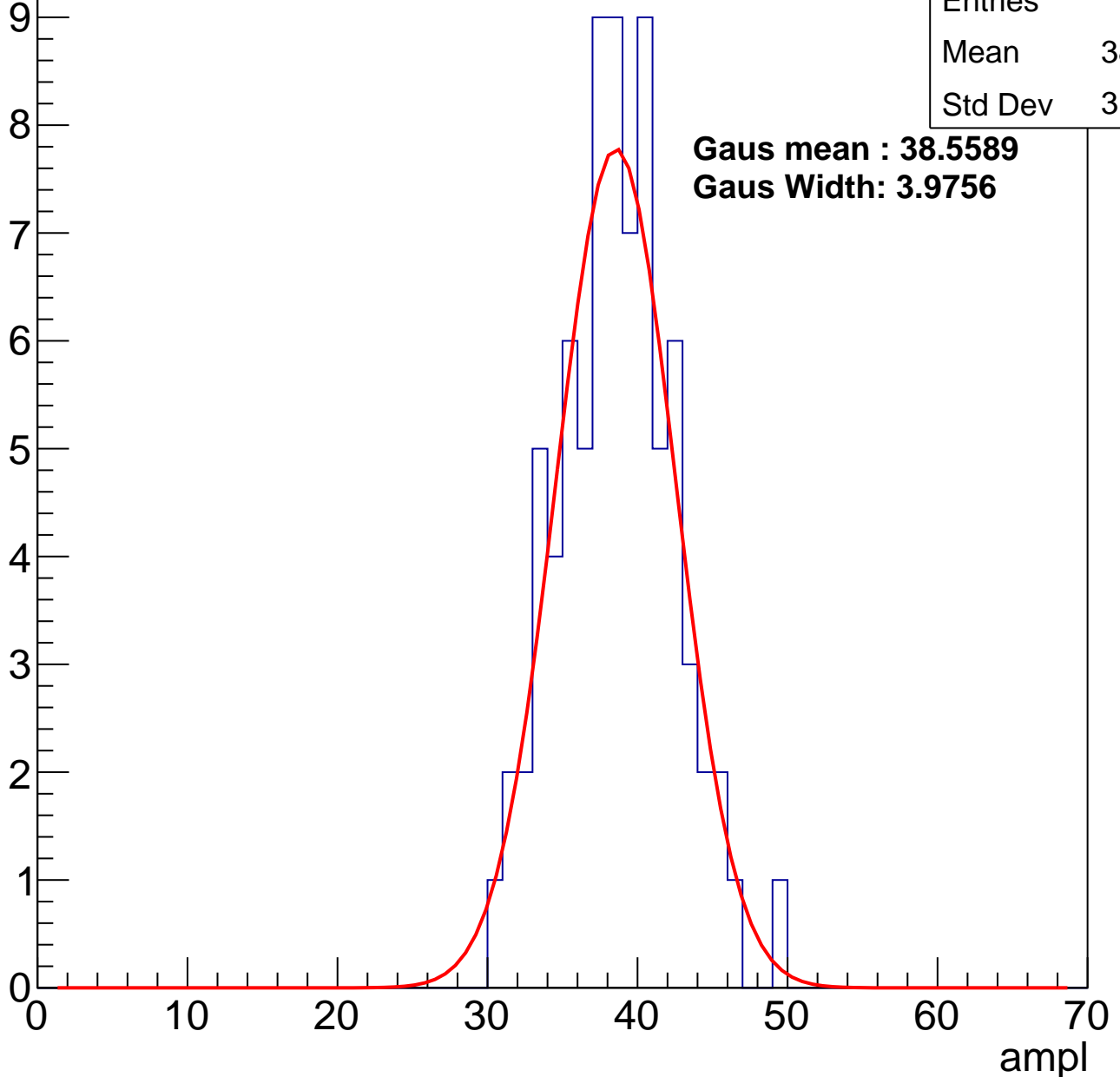
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	79
Mean	38.15
Std Dev	3.762

**Gaus mean : 38.5589**

**Gaus Width: 3.9756**



# B1L003S, U11-ch93, adc2

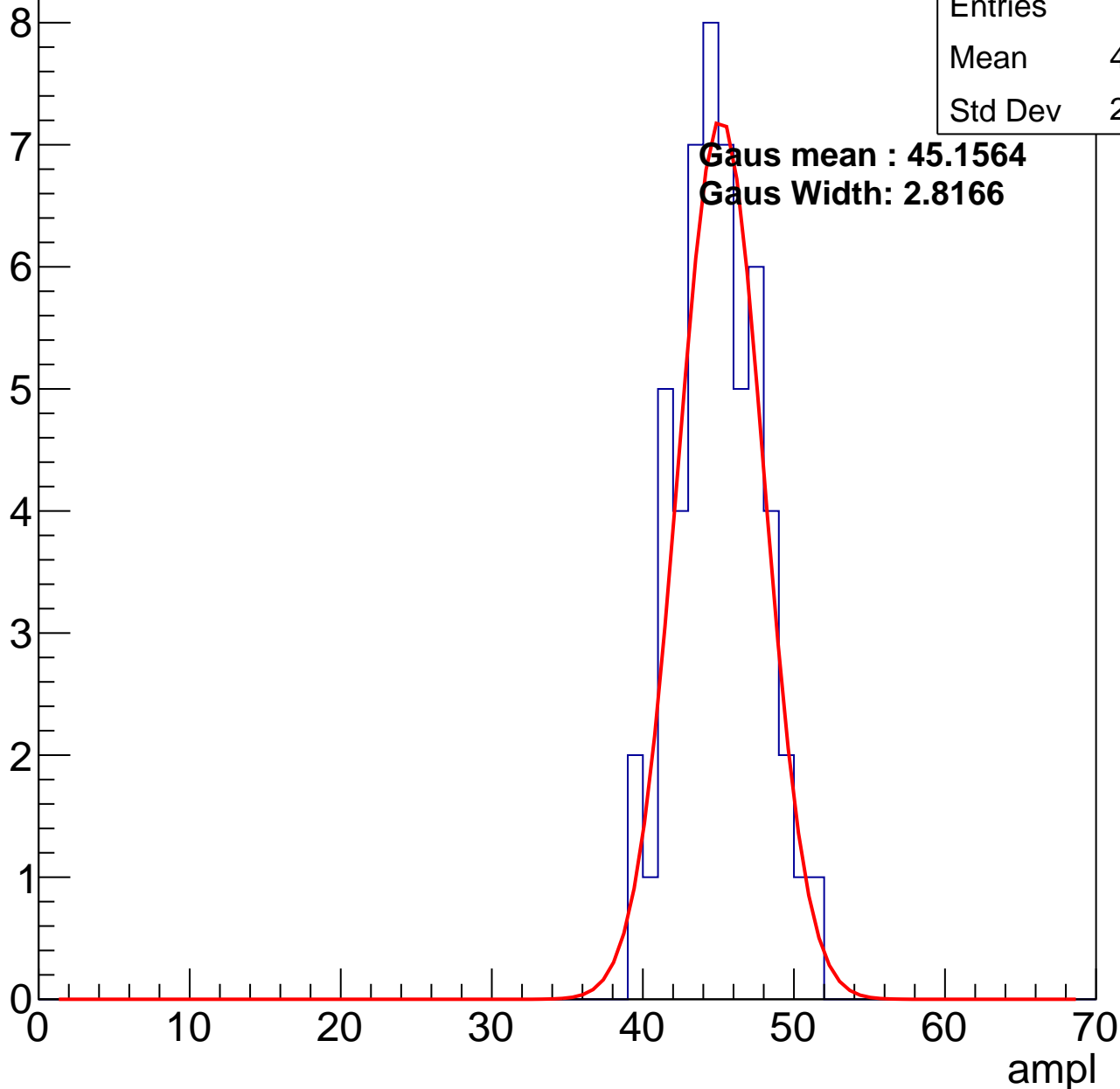
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	44.57
Std Dev	2.737

**Gaus mean : 45.1564**

**Gaus Width: 2.8166**

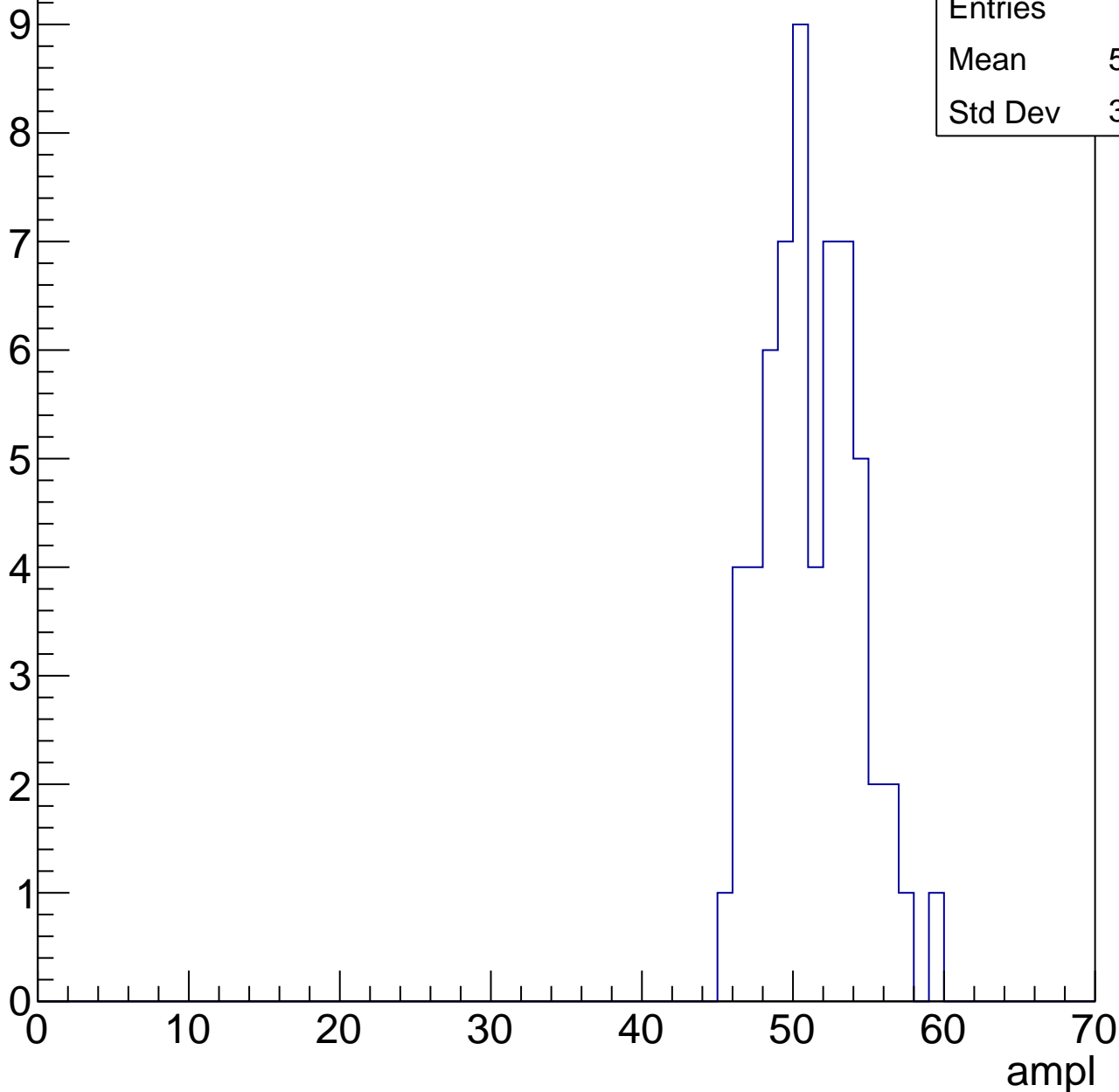


# B1L003S, U11-ch93, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	50.75
Std Dev	3.026

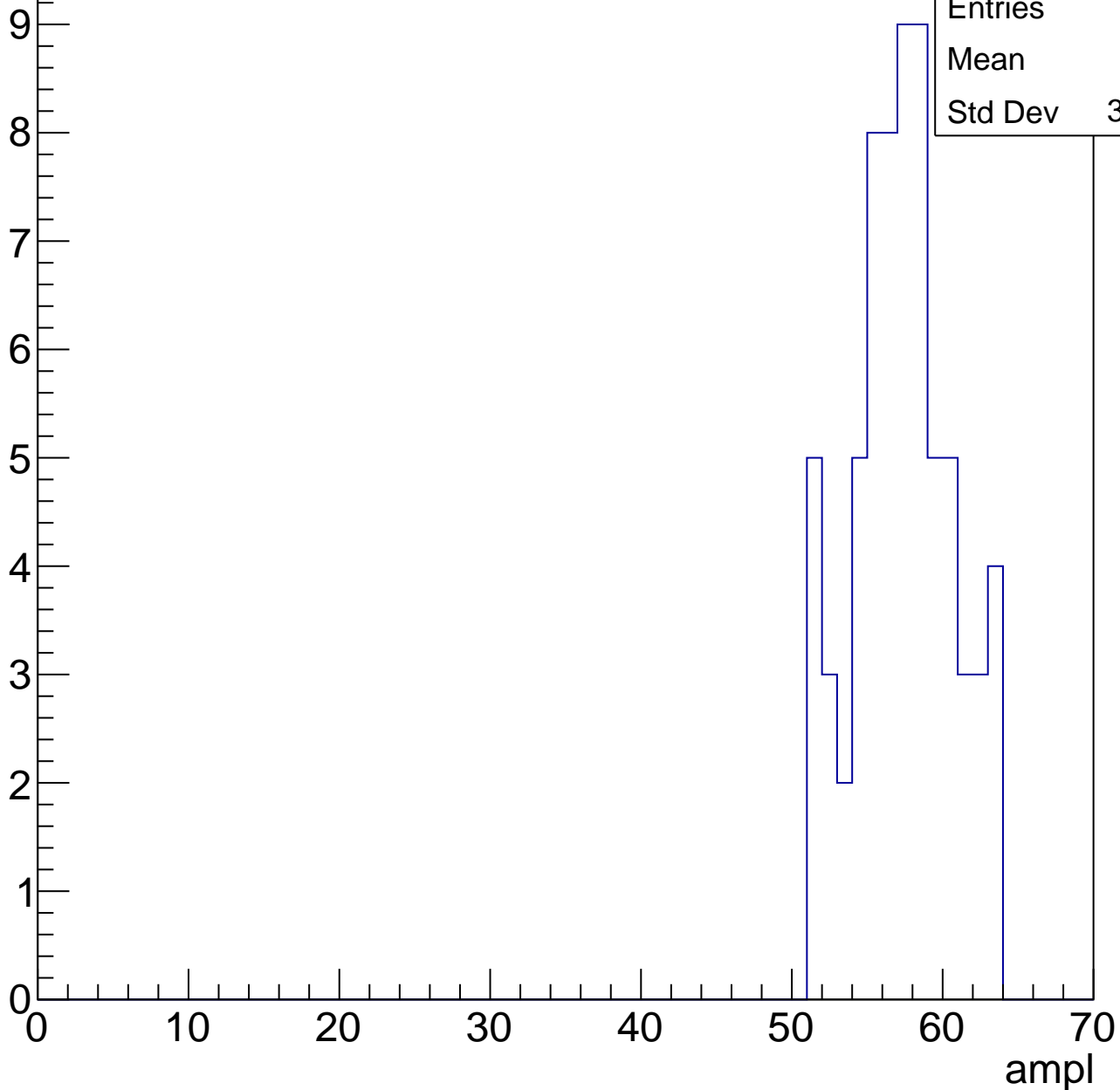


# B1L003S, U11-ch93, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	56.9
Std Dev	3.213

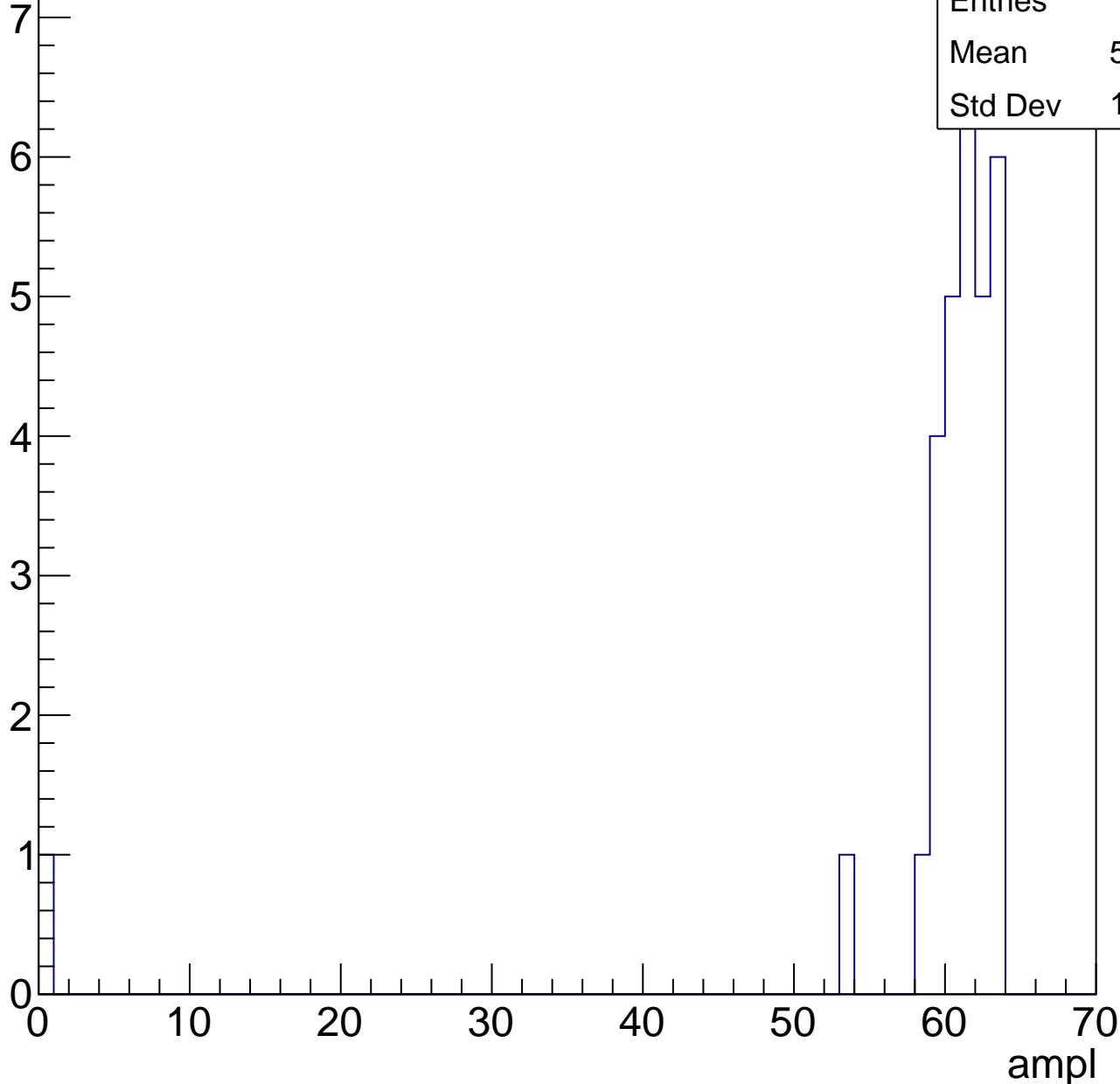


# B1L003S, U11-ch93, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	30
Mean	58.73
Std Dev	11.09



# B1L003S, U11-ch93, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch93, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U11-ch94, adc0

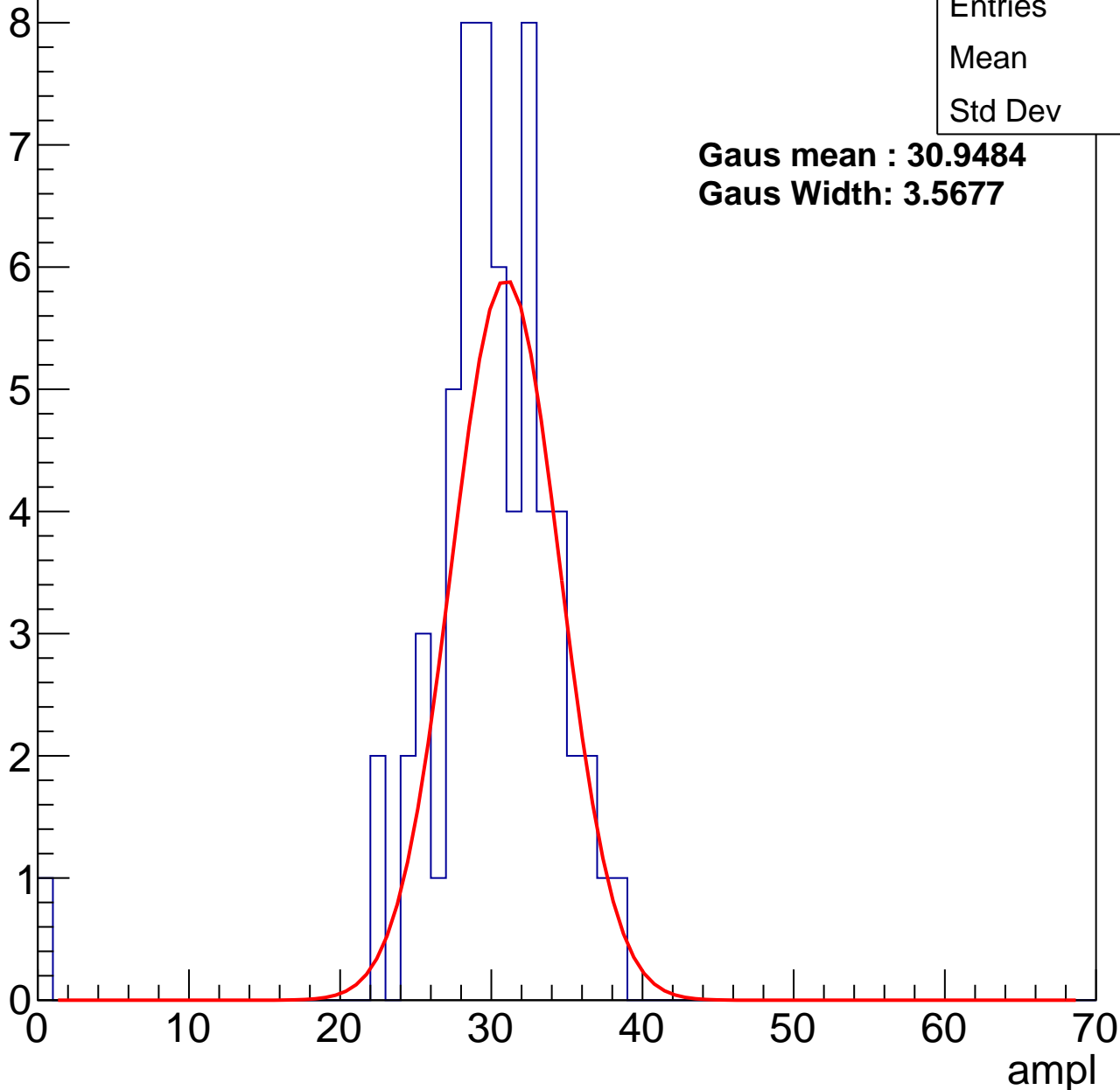
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	29.5
Std Dev	5.13

**Gaus mean : 30.9484**

**Gaus Width: 3.5677**



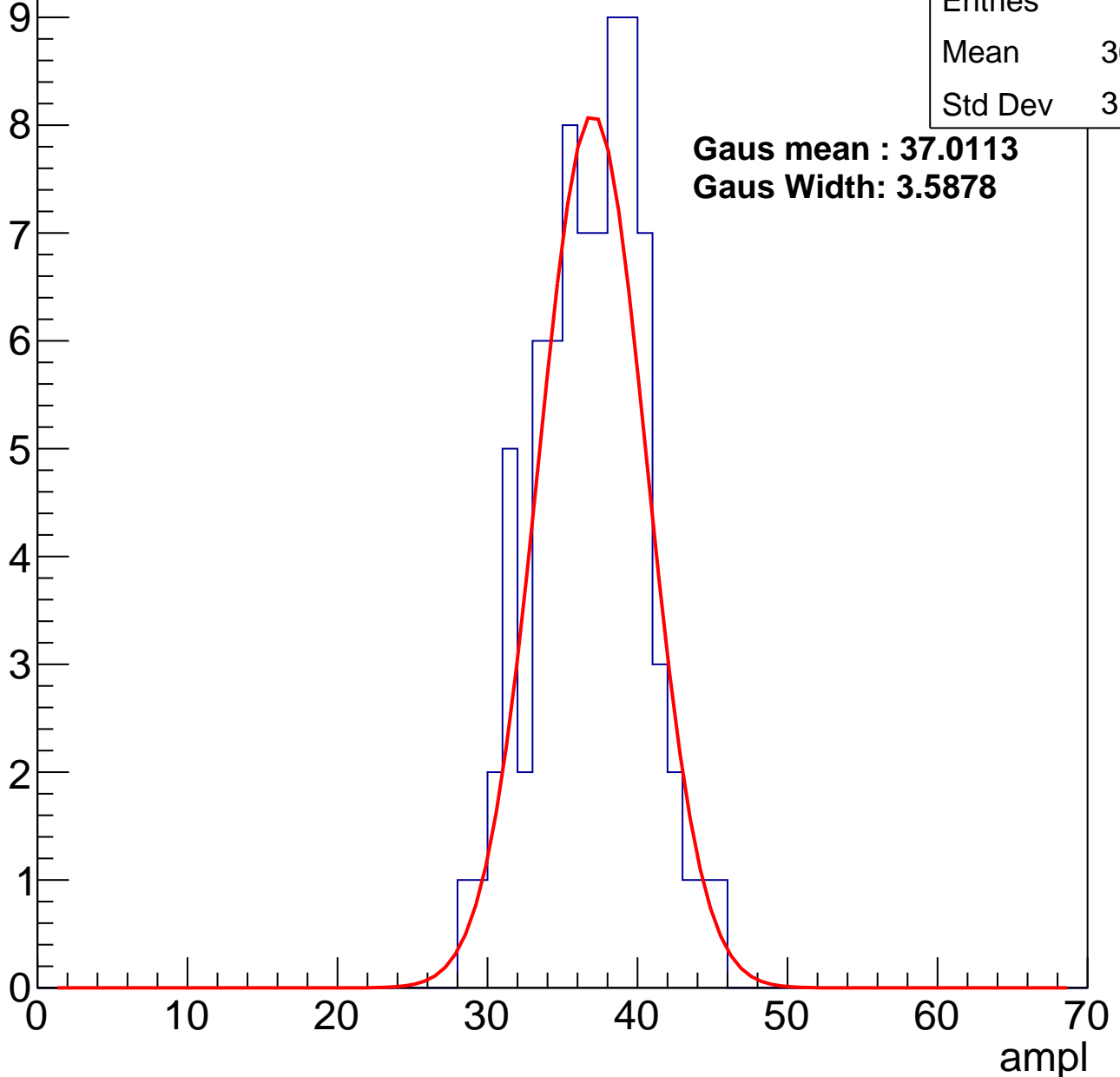
# B1L003S, U11-ch94, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	78
Mean	36.42
Std Dev	3.564

**Gaus mean : 37.0113**  
**Gaus Width: 3.5878**



# B1L003S, U11-ch94, adc2

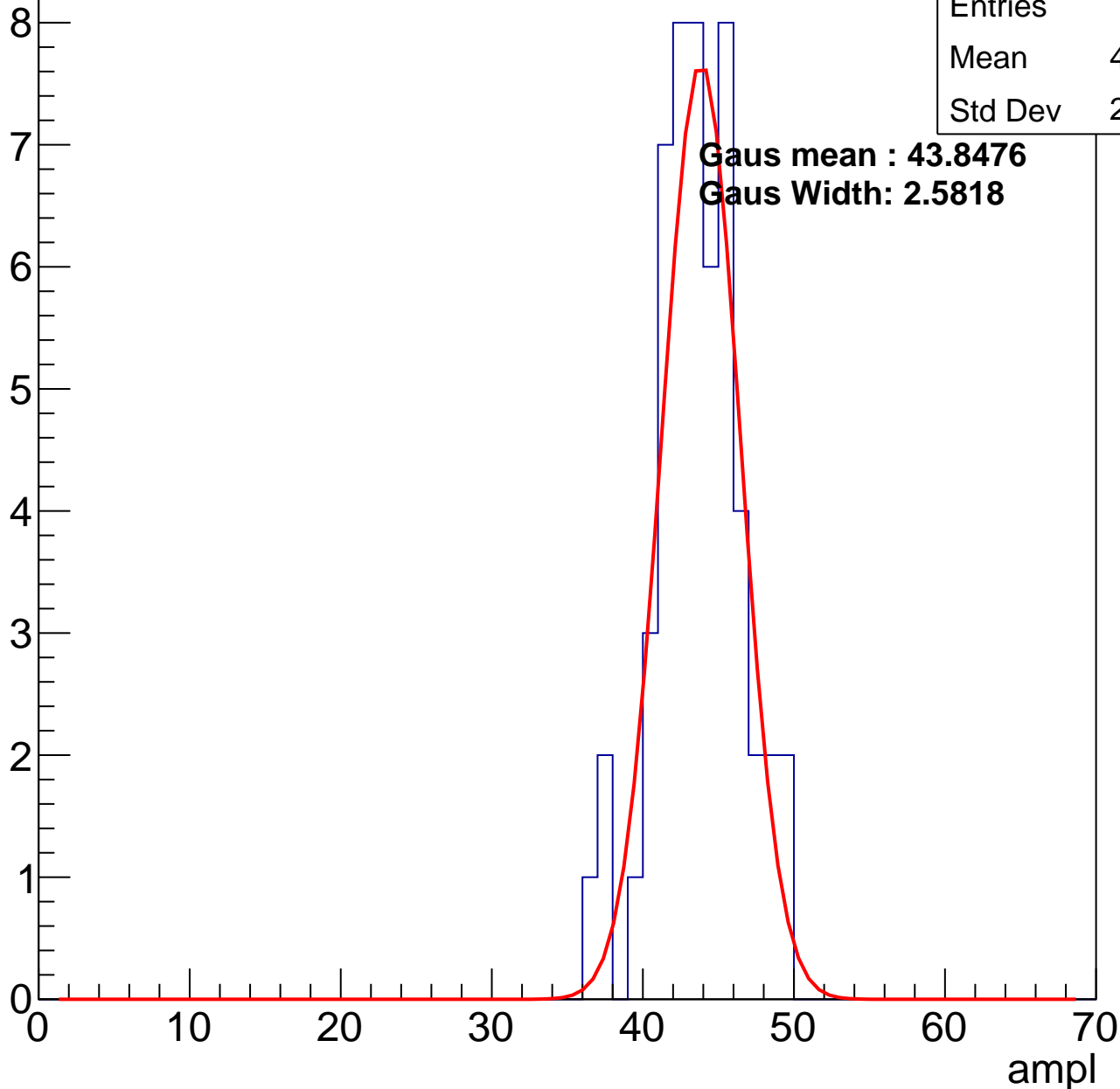
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	54
Mean	43.19
Std Dev	2.809

**Gaus mean : 43.8476**

**Gaus Width: 2.5818**

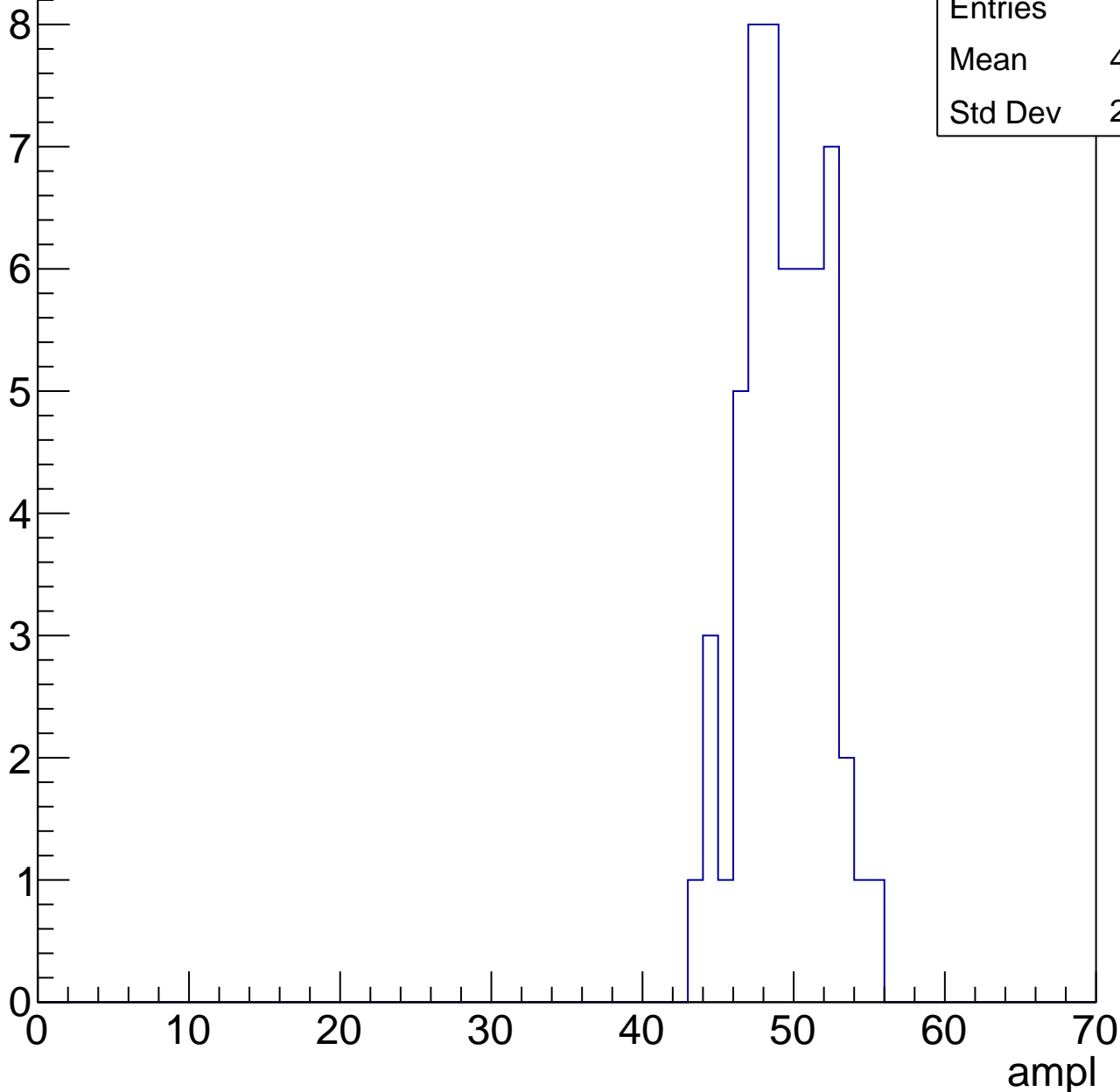


# B1L003S, U11-ch94, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	48.89
Std Dev	2.688

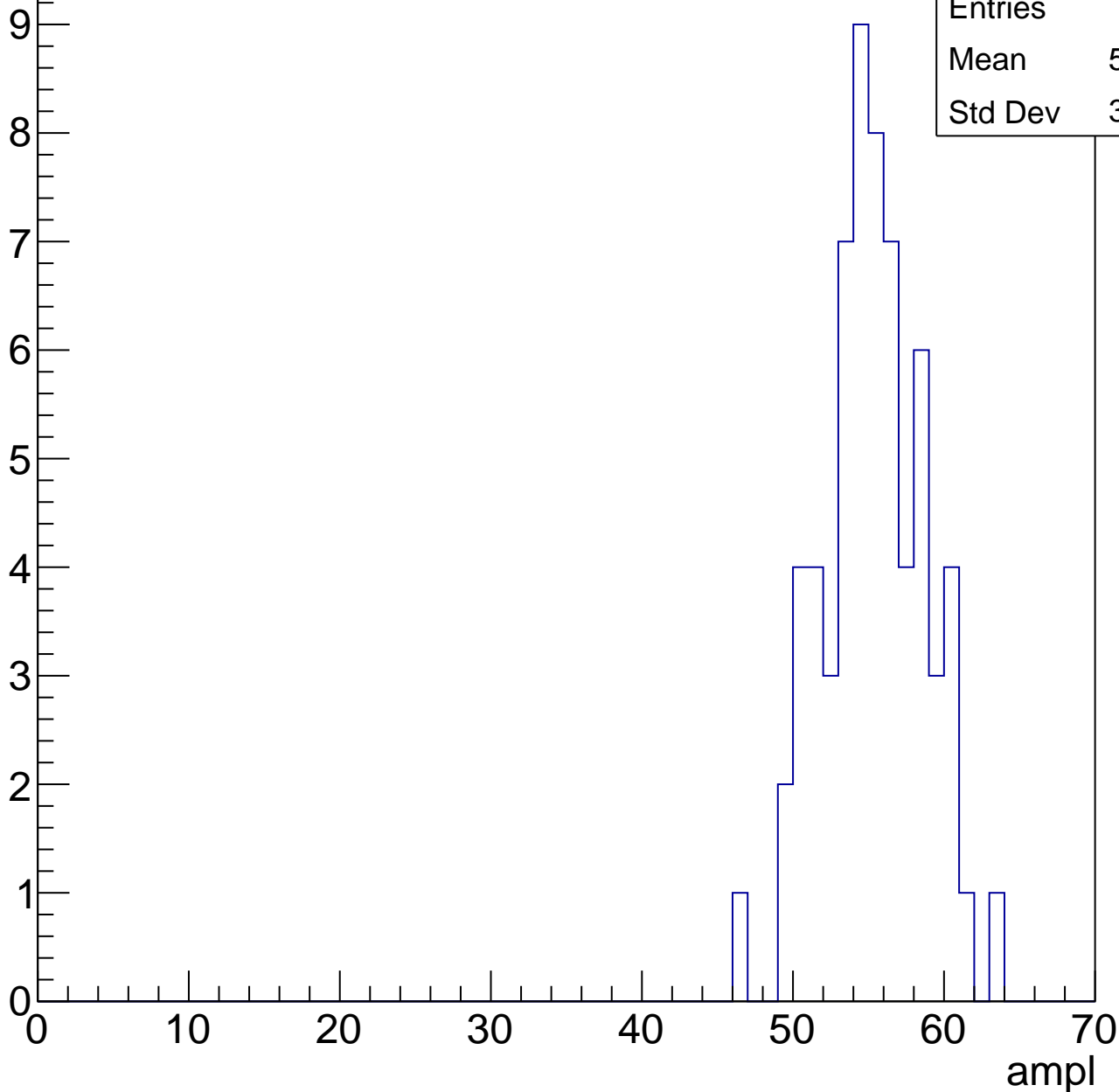


# B1L003S, U11-ch94, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	54.84
Std Dev	3.318

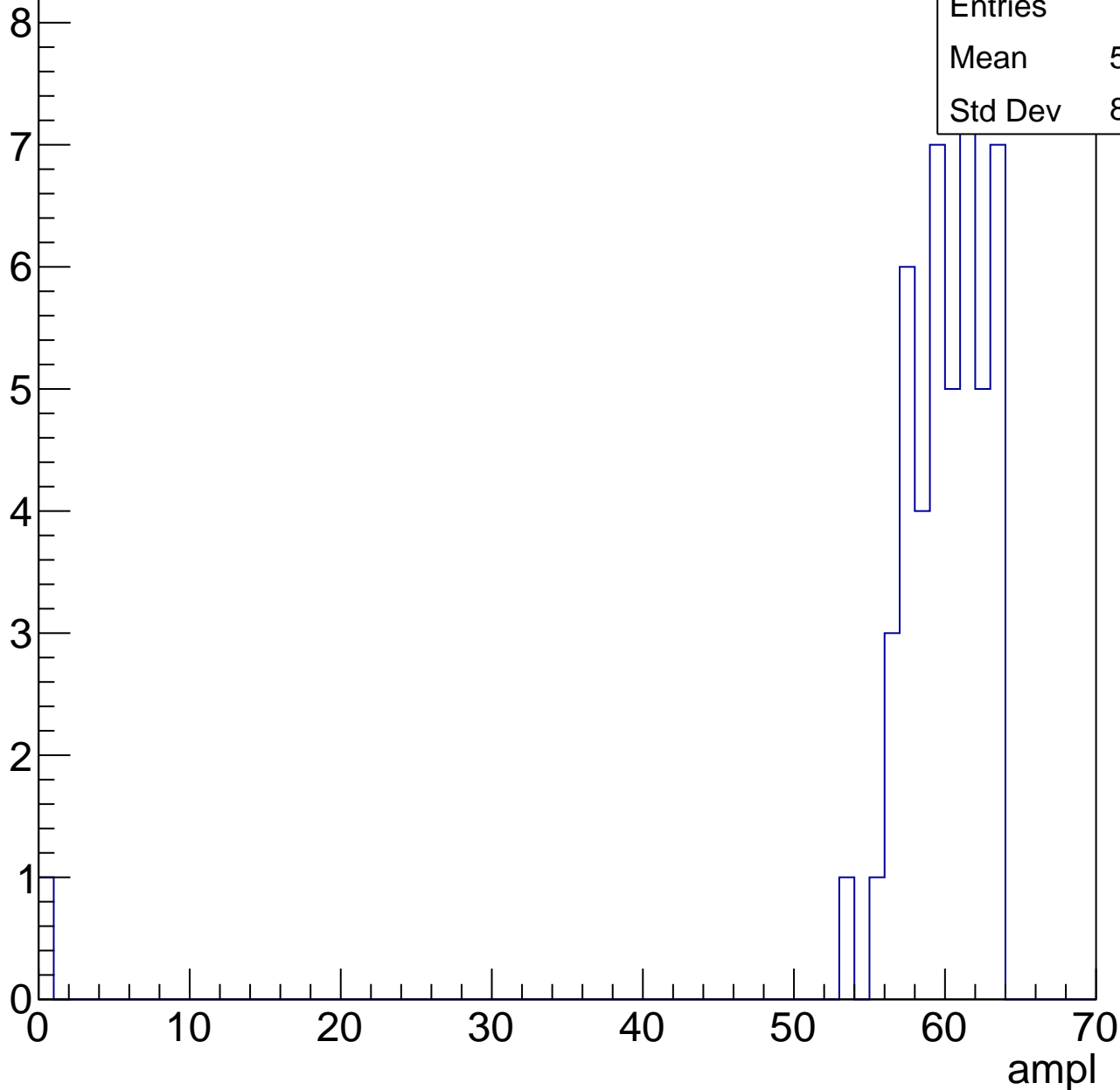


# B1L003S, U11-ch94, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	48
Mean	58.38
Std Dev	8.854

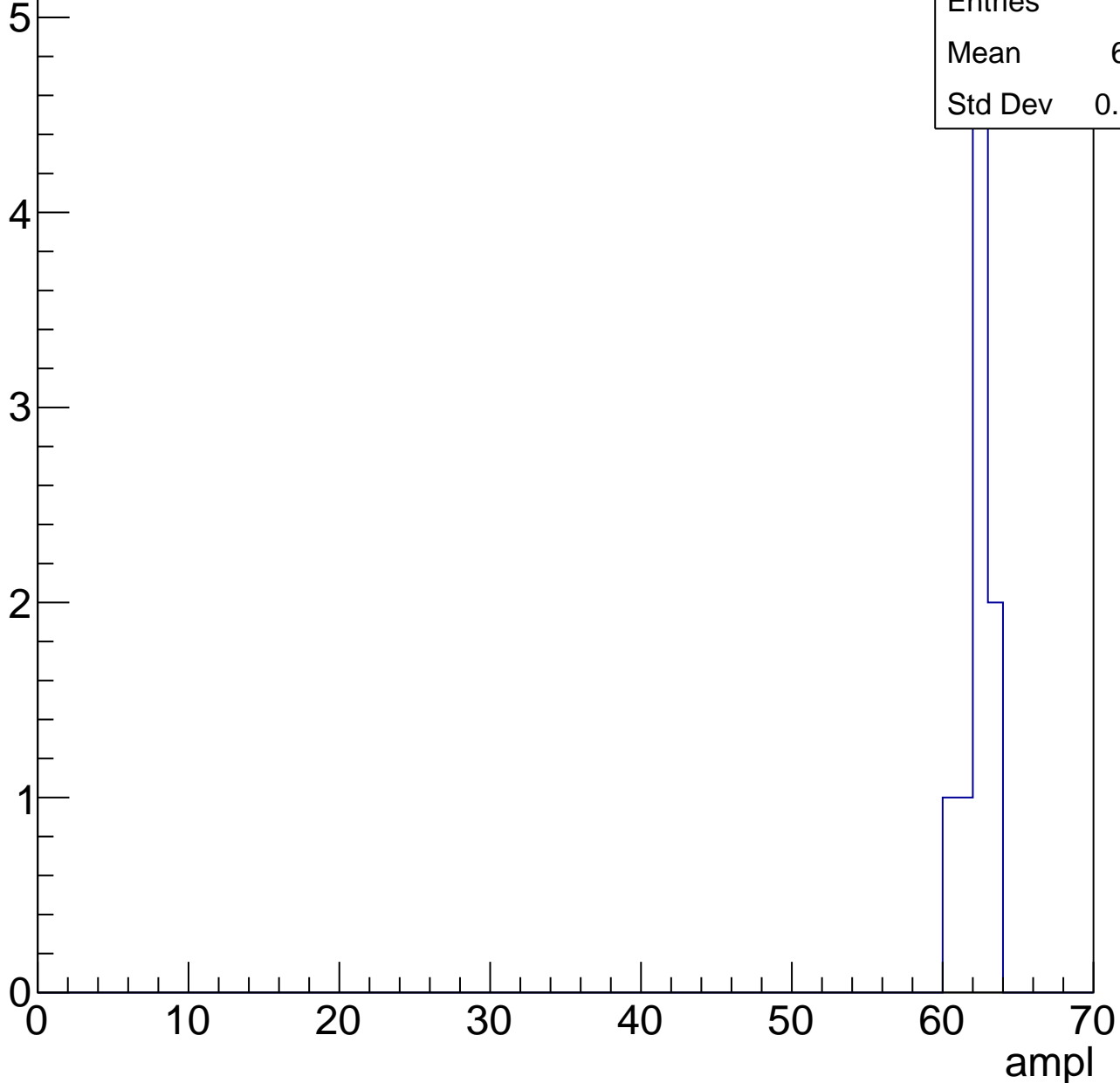


# B1L003S, U11-ch94, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	9
Mean	61.89
Std Dev	0.8749





# B1L003S, U11-ch94, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U11-ch95, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	87
Mean	29.13
Std Dev	5.984

**Gaus mean : 30.0157**

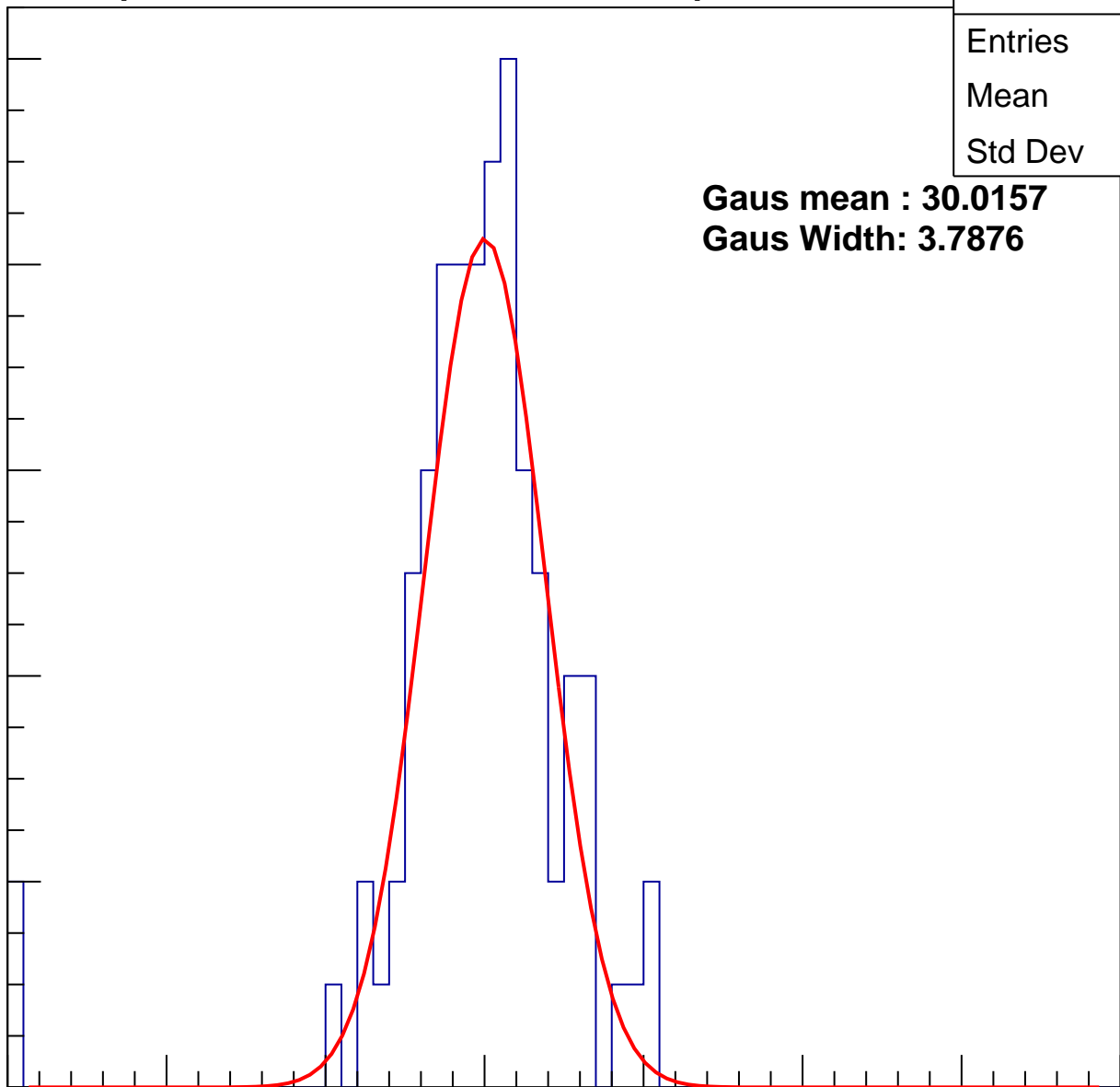
**Gaus Width: 3.7876**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U11-ch95, adc1

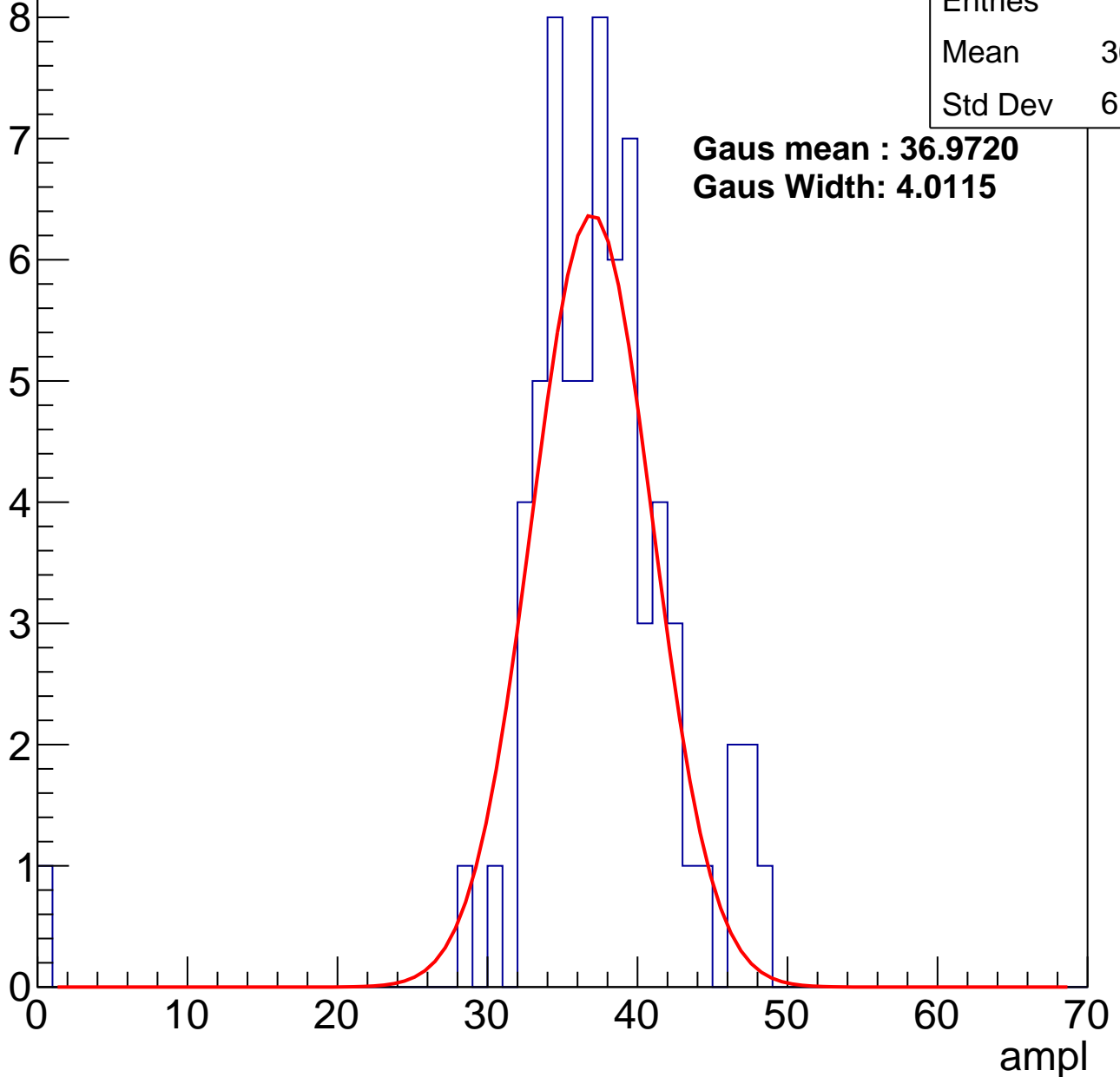
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	36.85
Std Dev	6.115

**Gaus mean : 36.9720**

**Gaus Width: 4.0115**



# B1L003S, U11-ch95, adc2

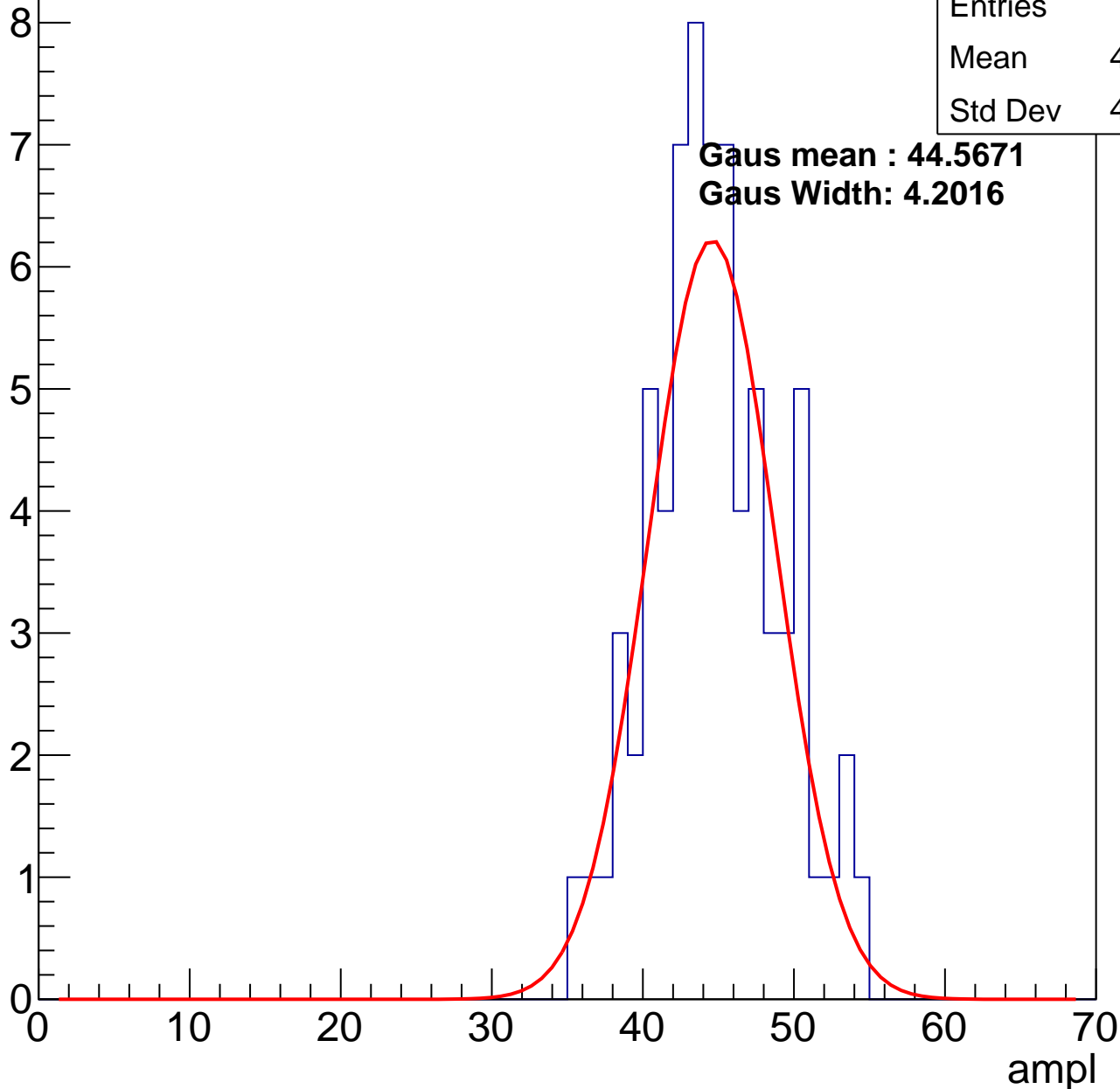
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	71
Mean	44.34
Std Dev	4.182

**Gaus mean : 44.5671**

**Gaus Width: 4.2016**

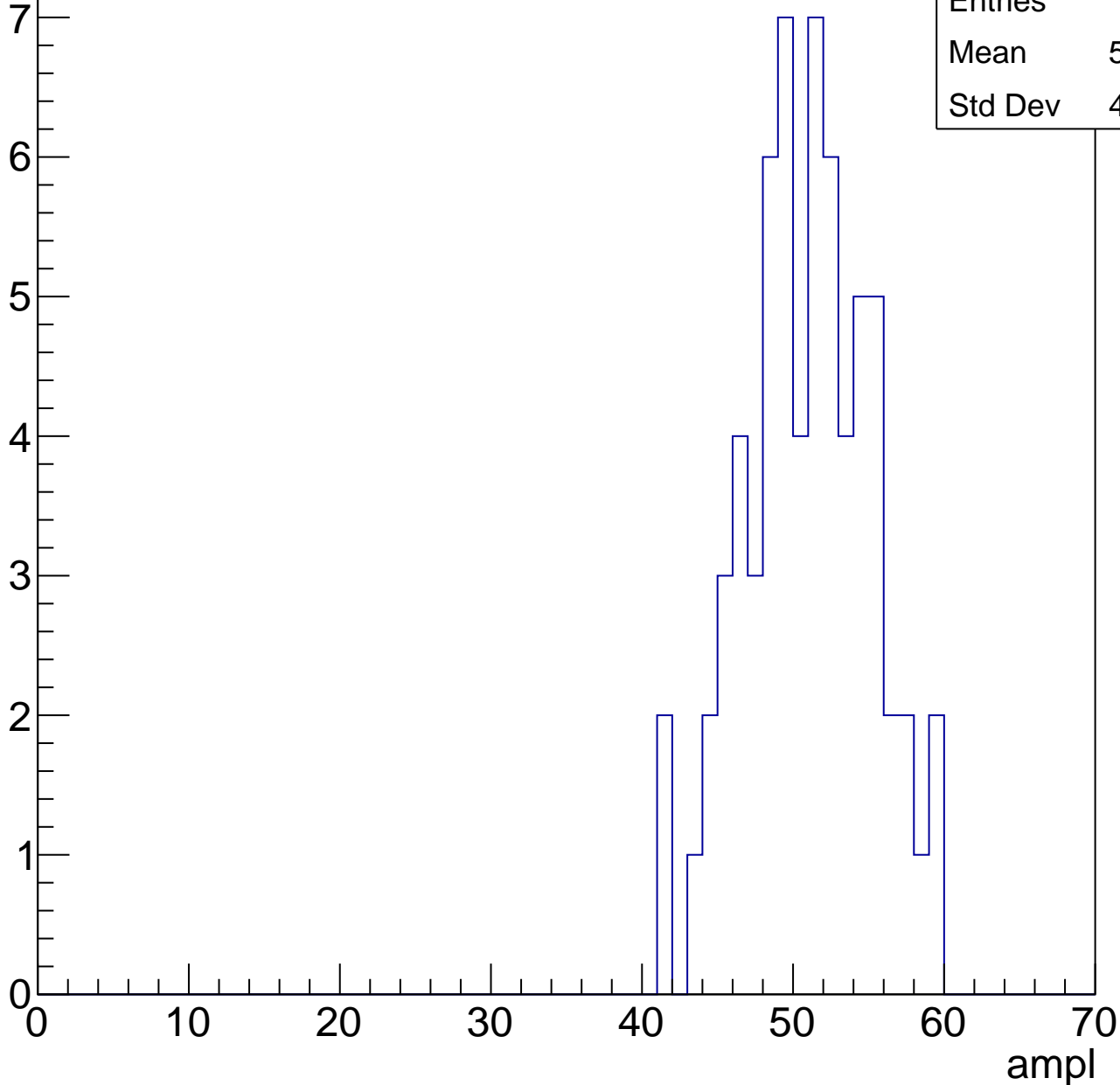


# B1L003S, U11-ch95, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	50.48
Std Dev	4.142

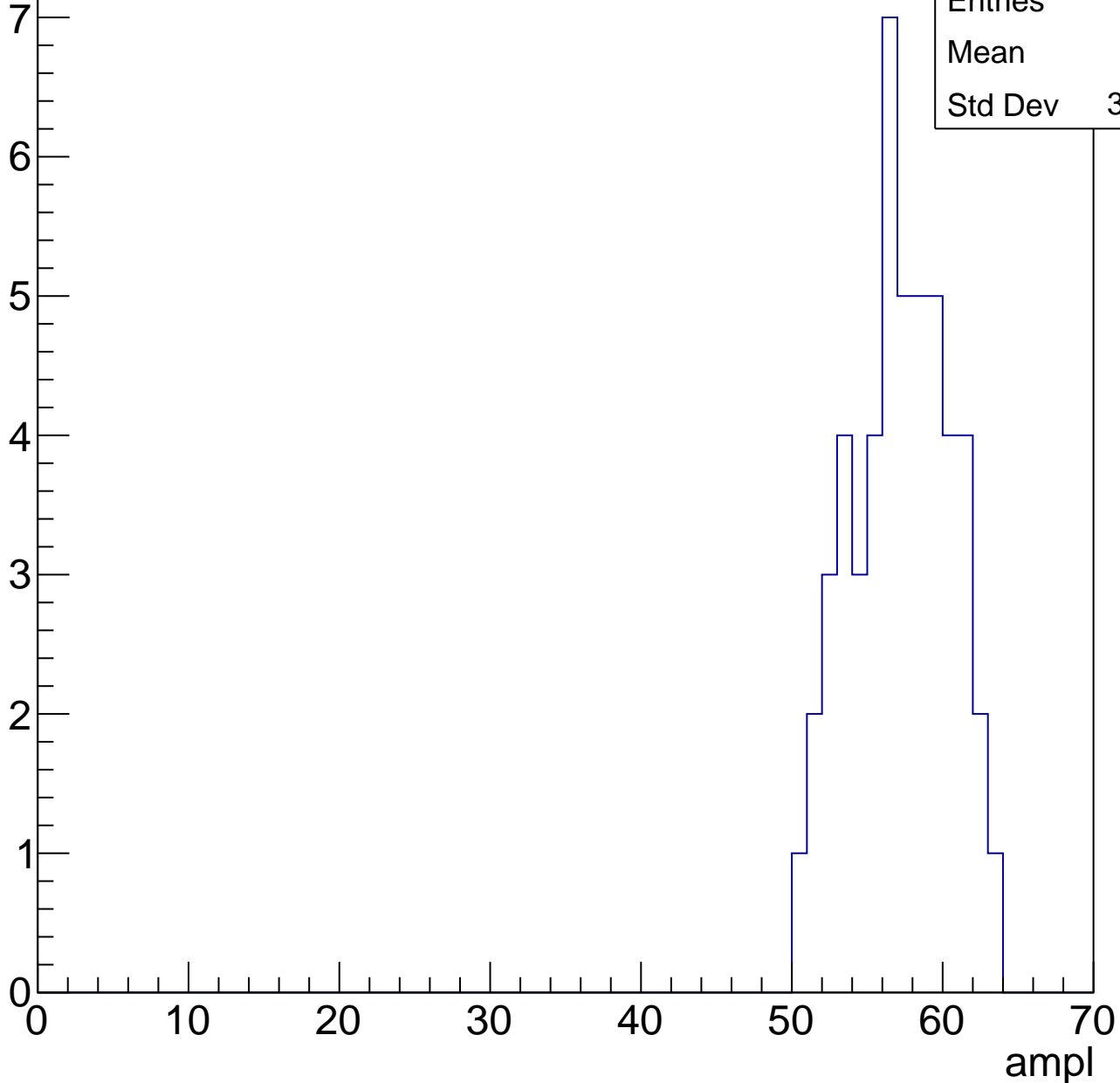


# B1L003S, U11-ch95, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	50
Mean	56.7
Std Dev	3.214

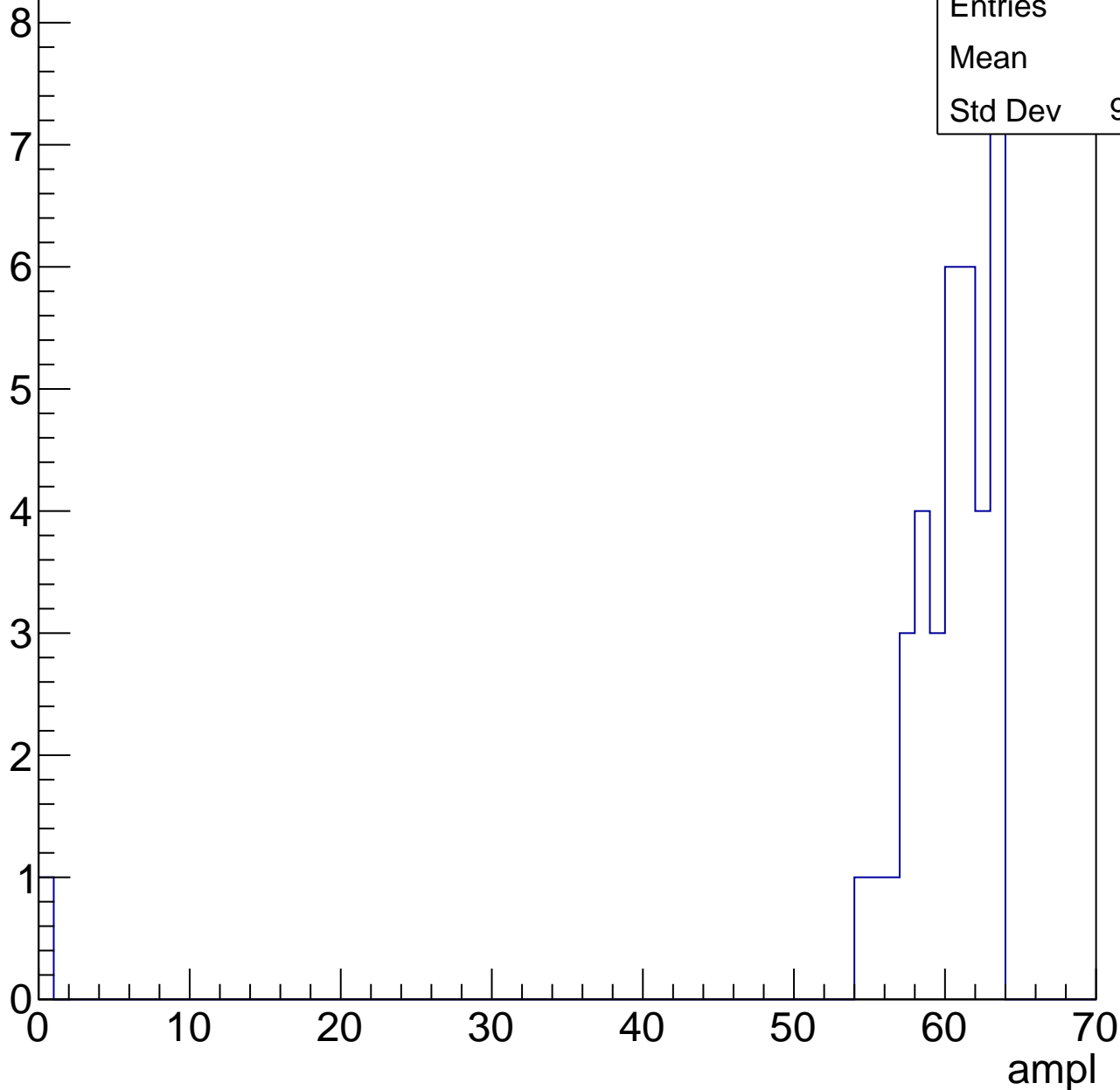


# B1L003S, U11-ch95, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

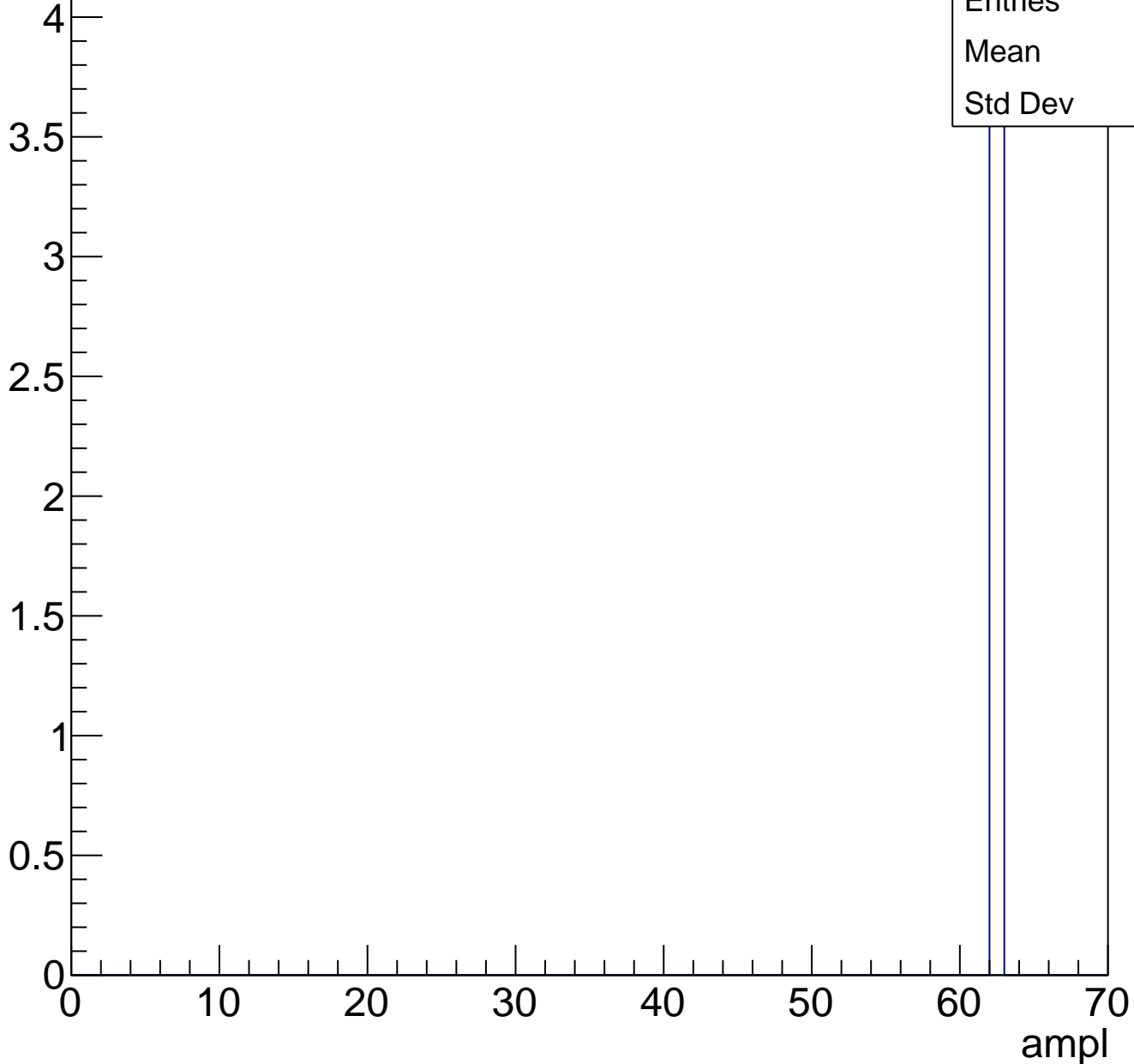
Entries	38
Mean	58.5
Std Dev	9.909



# B1L003S, U11-ch95, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch95, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U11-ch96, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

120

100

80

60

40

20

0

0

10

20

30

40

50

60

70

ampl

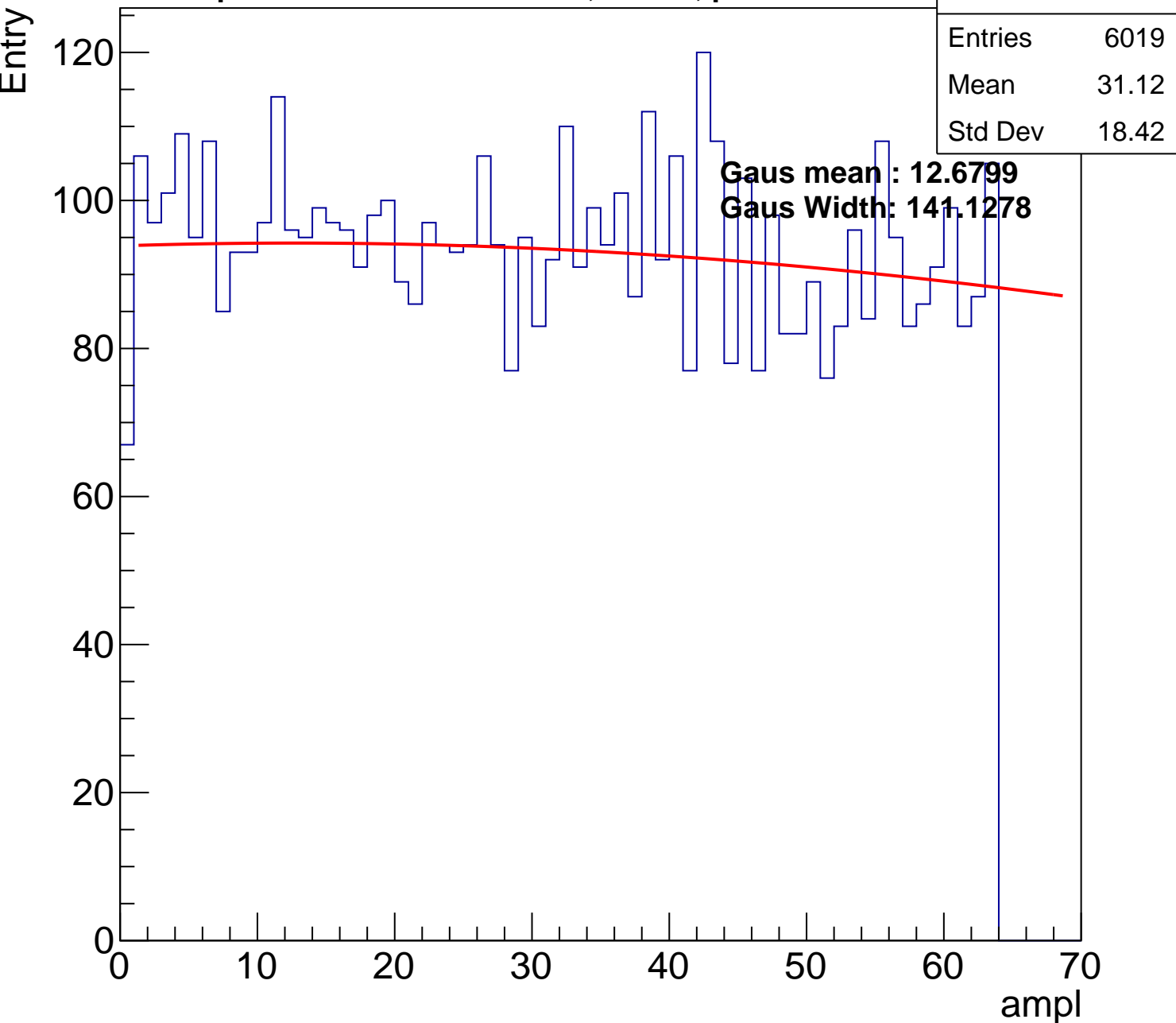
Entries 6019

Mean 31.12

Std Dev 18.42

**Gaus mean : 12.6799**

**Gaus Width: 141.1278**

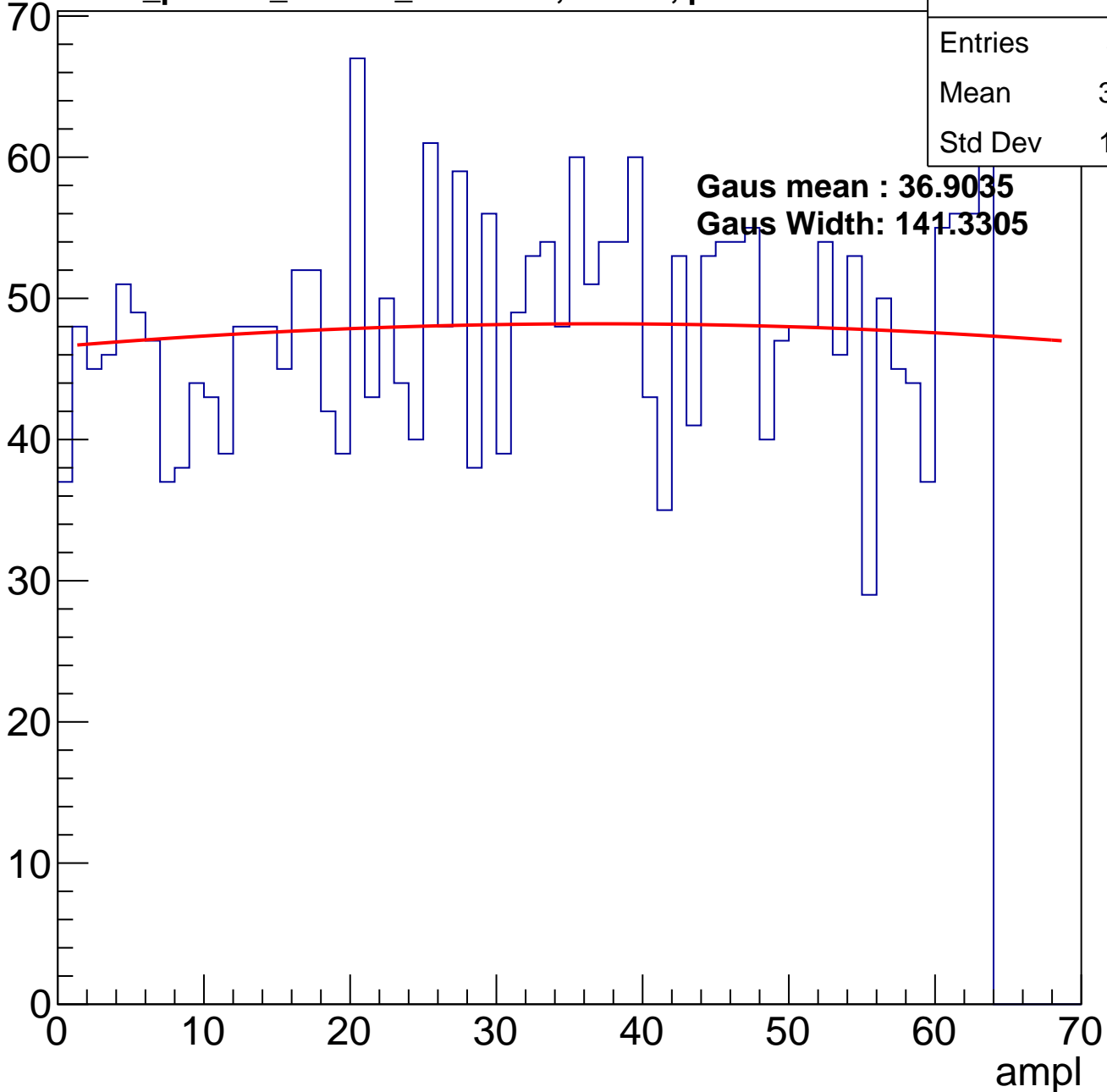


# B1L003S, U11-ch96, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	3082
Mean	32.09
Std Dev	18.28

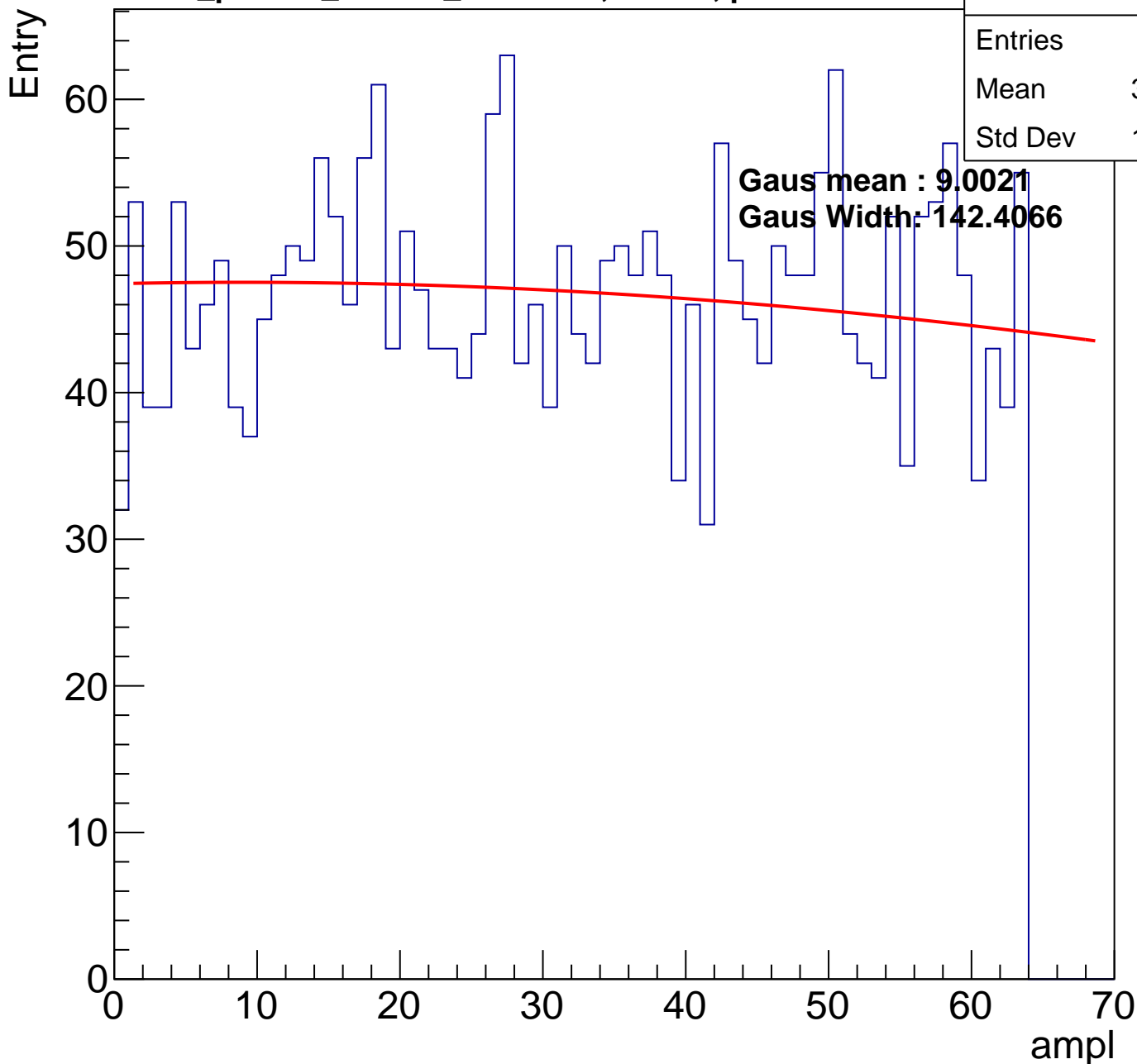
Entry



# B1L003S, U11-ch96, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

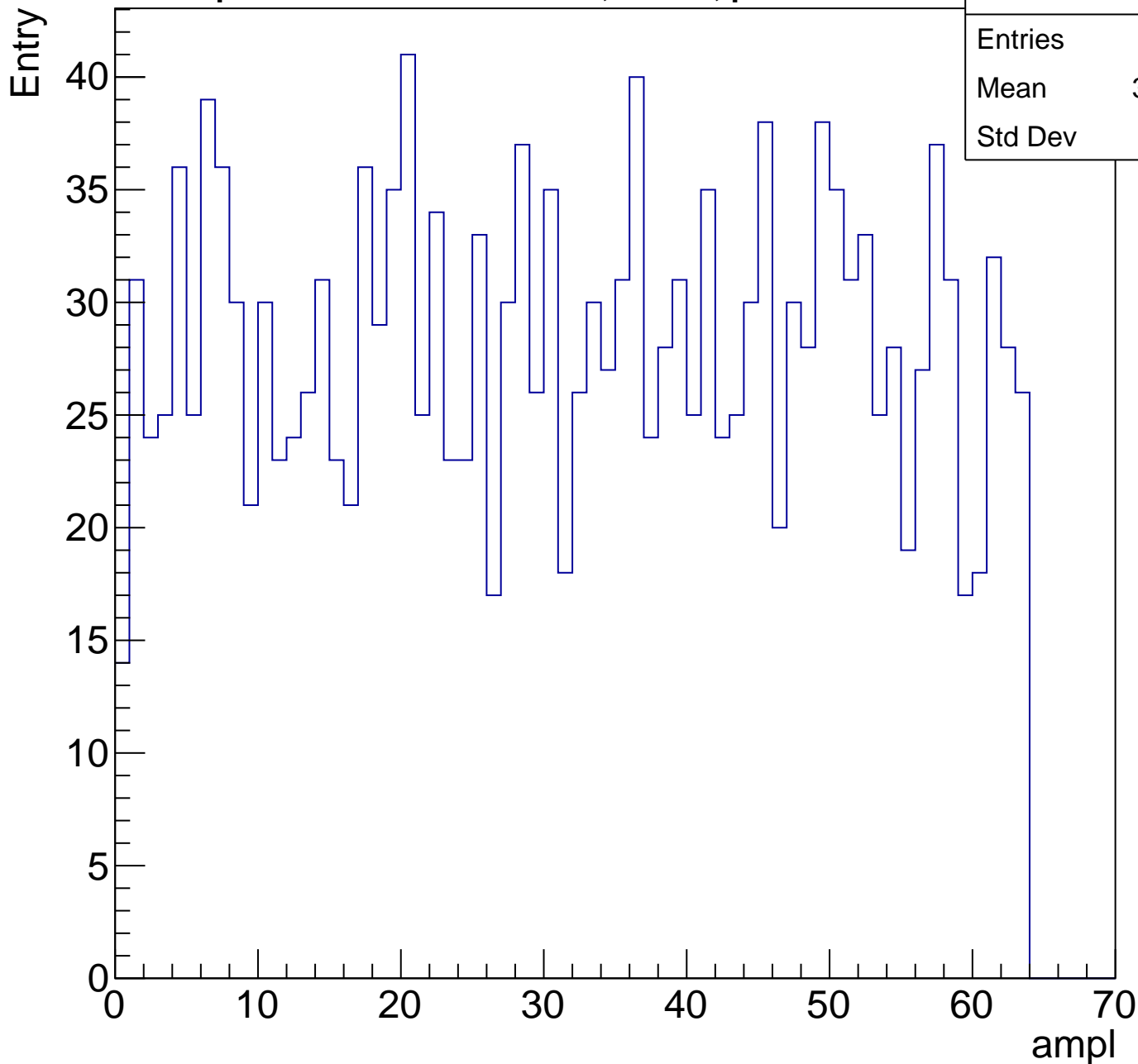
Entries	2998
Mean	31.65
Std Dev	18.29



# B1L003S, U11-ch96, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

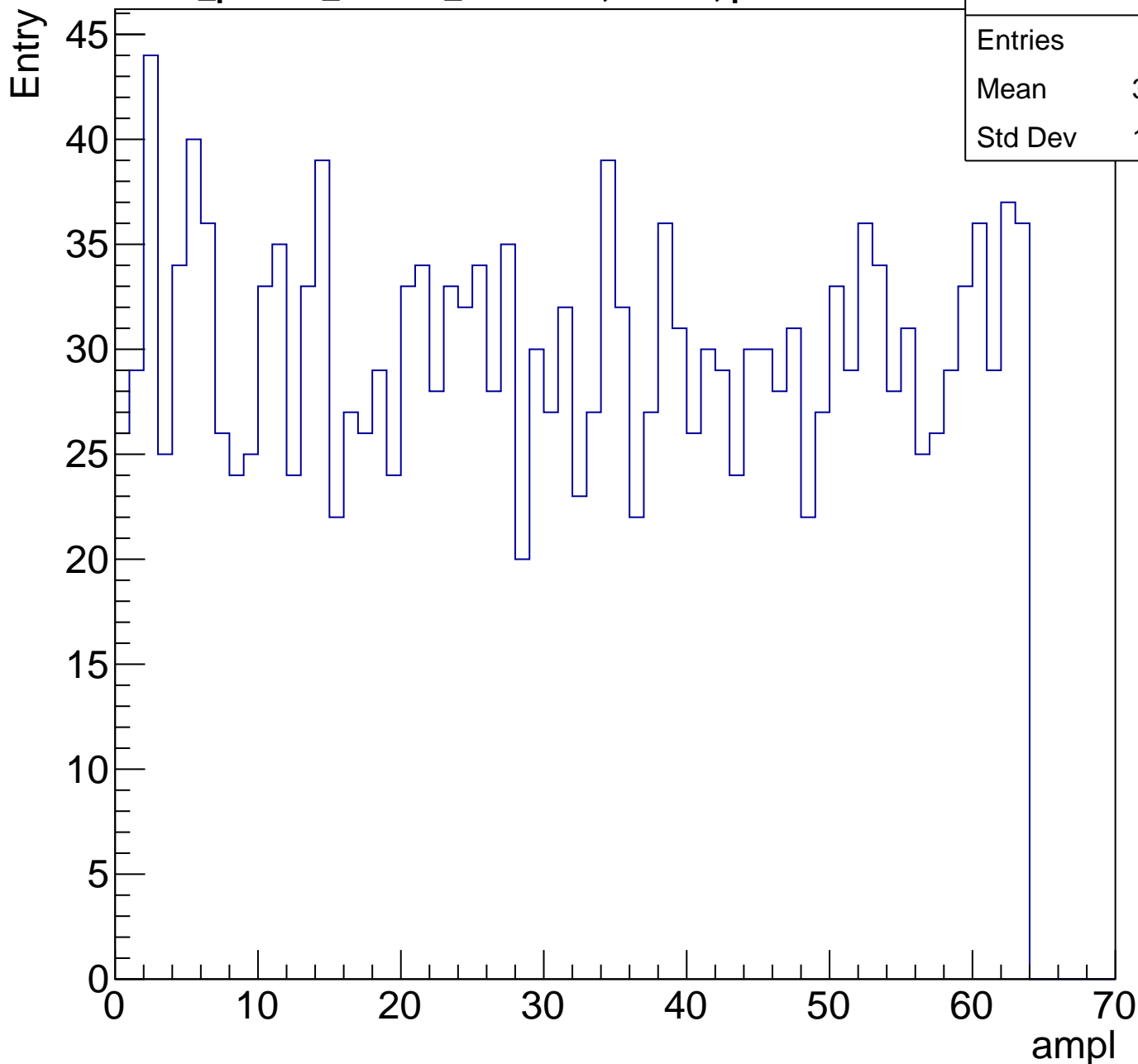
Entries	1818
Mean	31.54
Std Dev	18.2



# B1L003S, U11-ch96, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

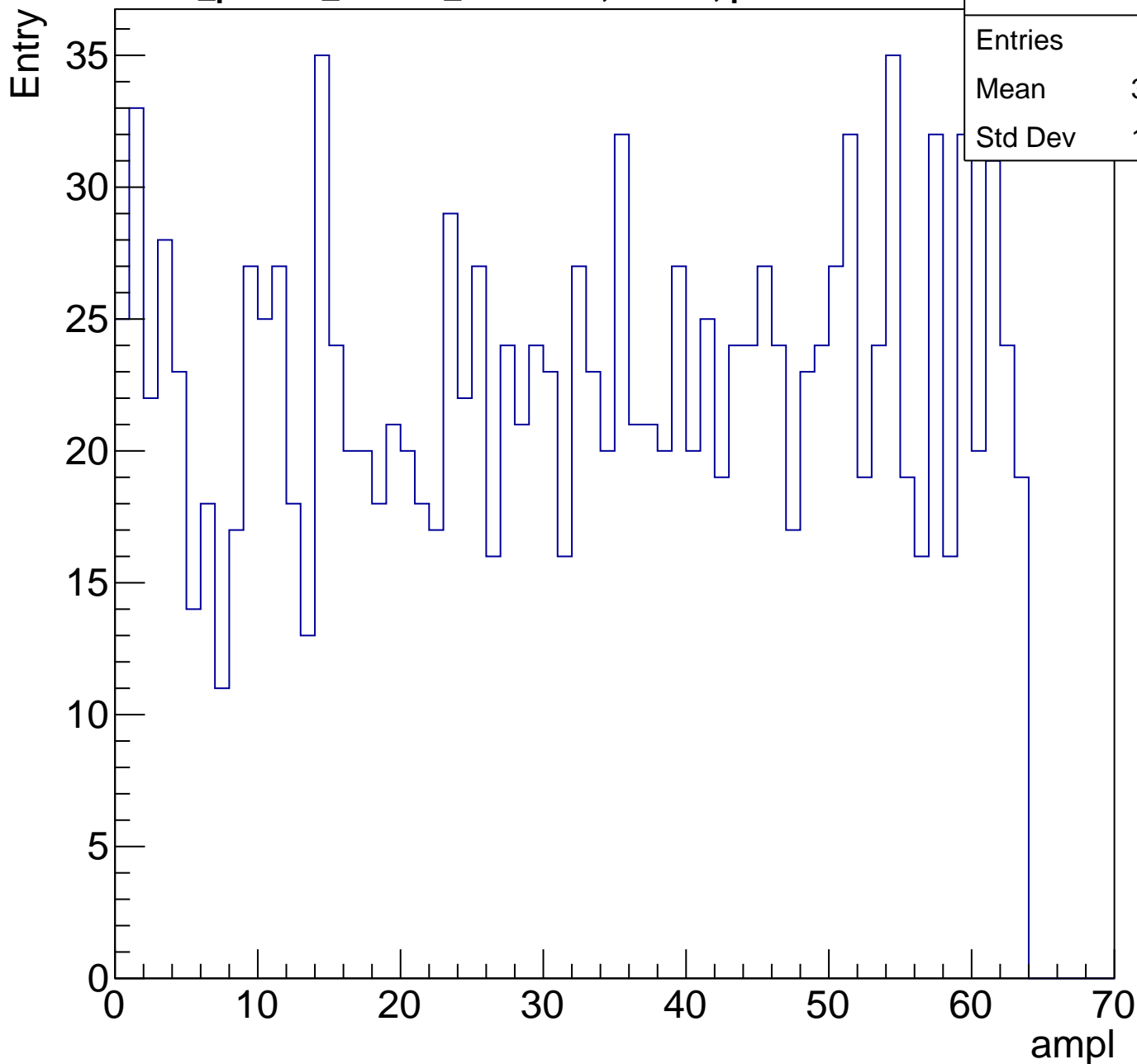
Entries	1923
Mean	31.49
Std Dev	18.78



# B1L003S, U11-ch96, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

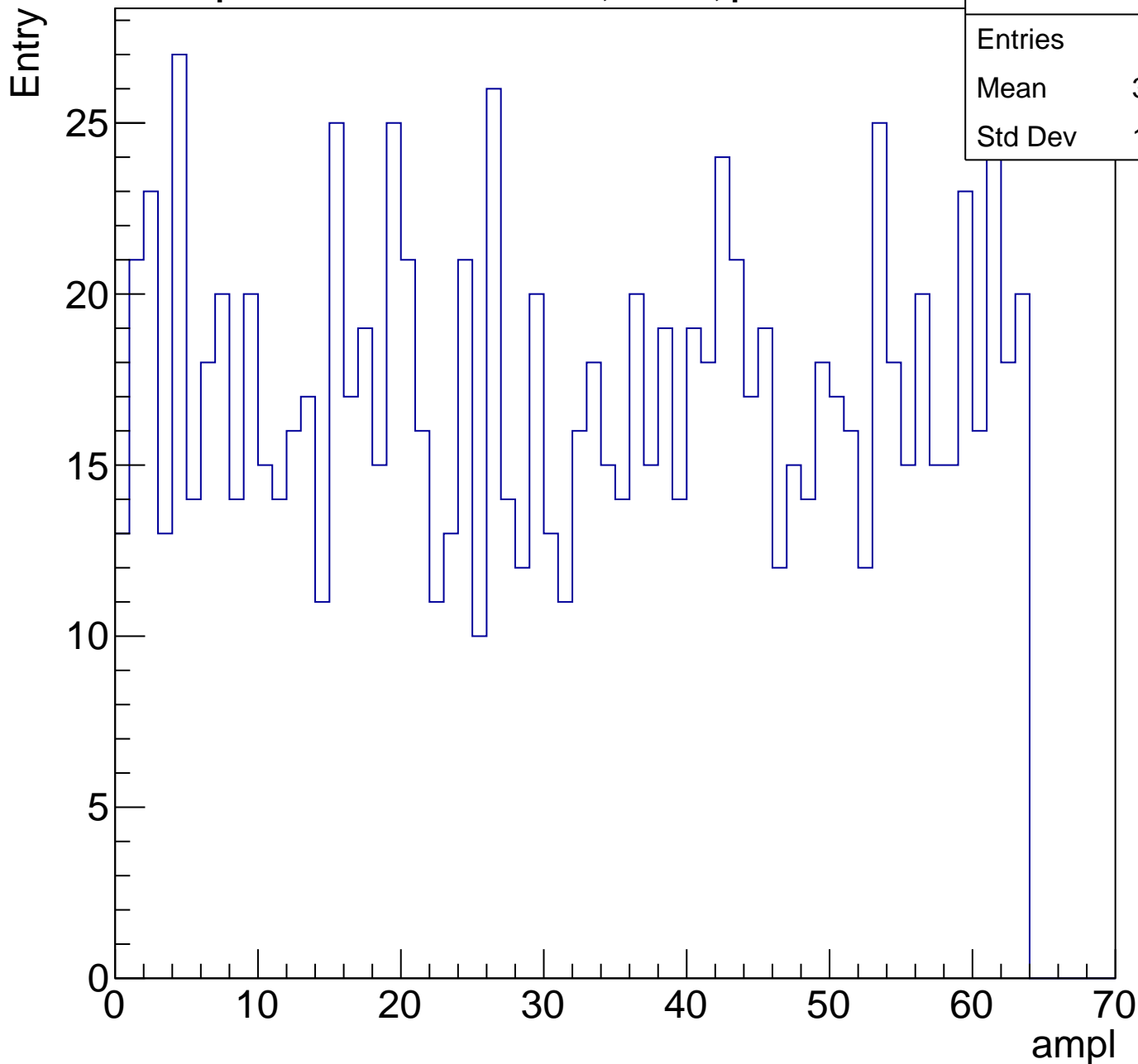
Entries	1460
Mean	32.17
Std Dev	18.65



# B1L003S, U11-ch96, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	1110
Mean	31.74
Std Dev	18.87

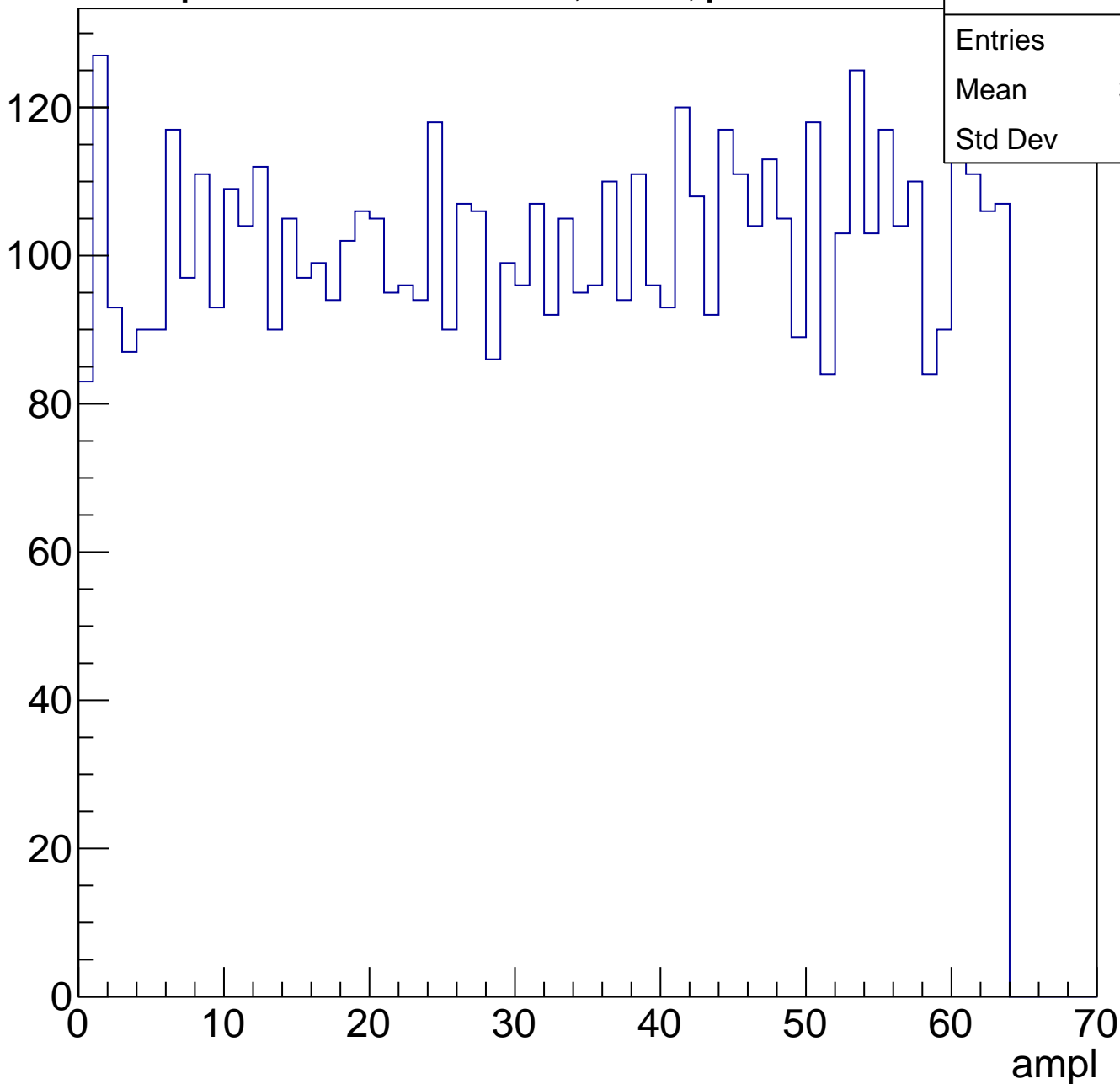




# B1L003S, U11-ch96, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U11-ch97, adc0

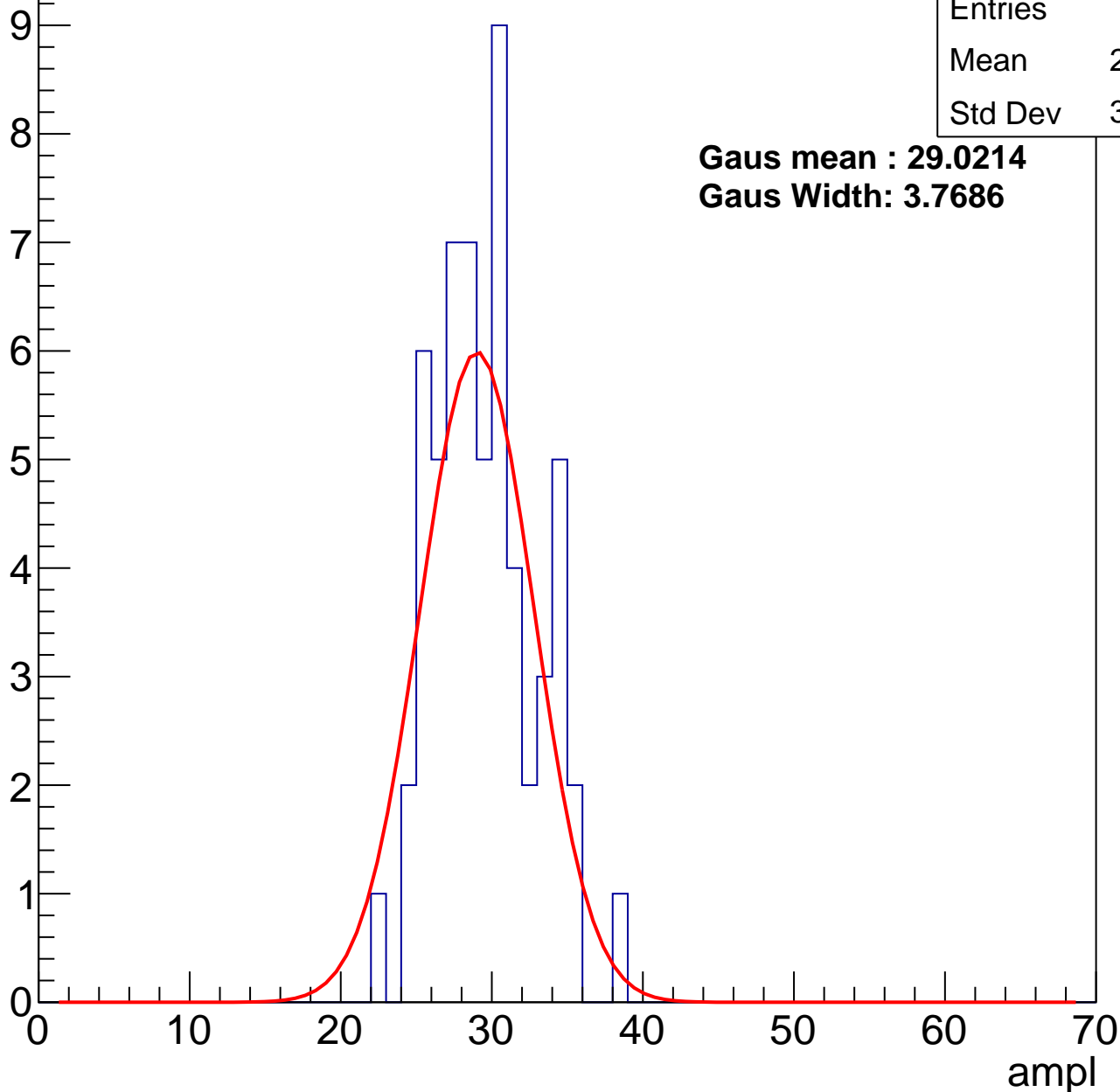
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	29.07
Std Dev	3.303

**Gaus mean : 29.0214**

**Gaus Width: 3.7686**



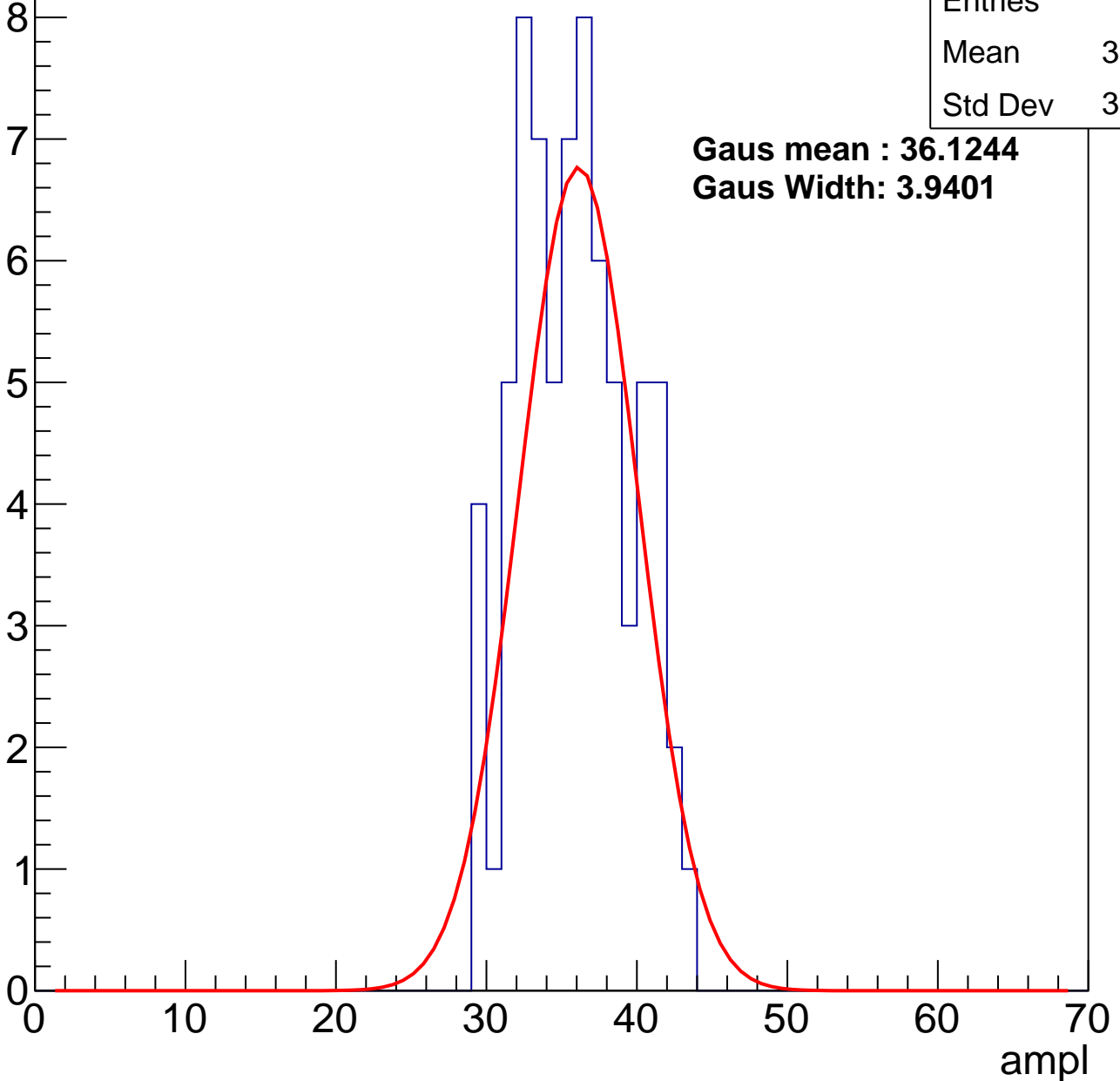
# B1L003S, U11-ch97, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	72
Mean	35.44
Std Dev	3.597

**Gaus mean : 36.1244**  
**Gaus Width: 3.9401**



# B1L003S, U11-ch97, adc2

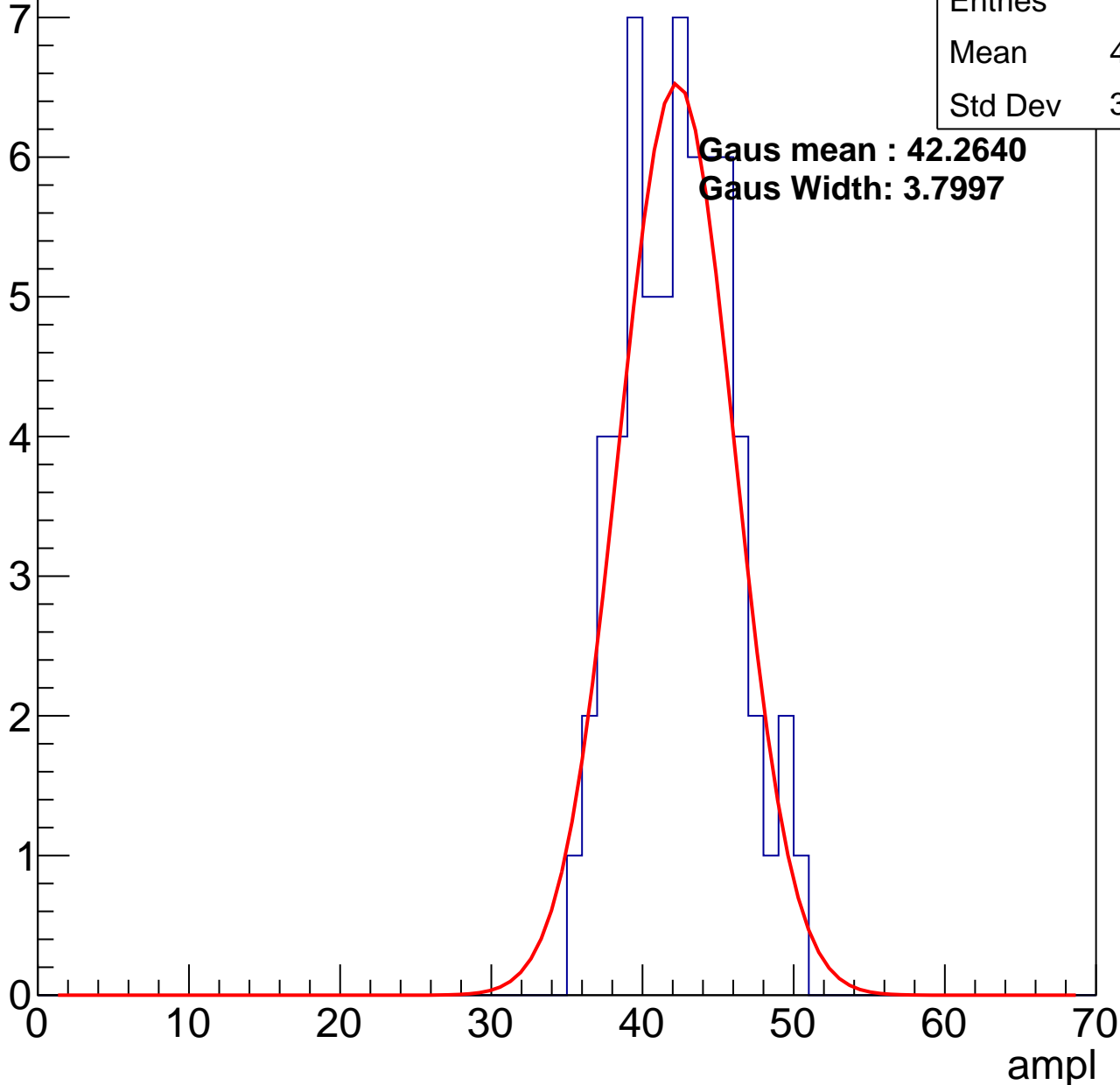
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	41.98
Std Dev	3.494

**Gaus mean : 42.2640**

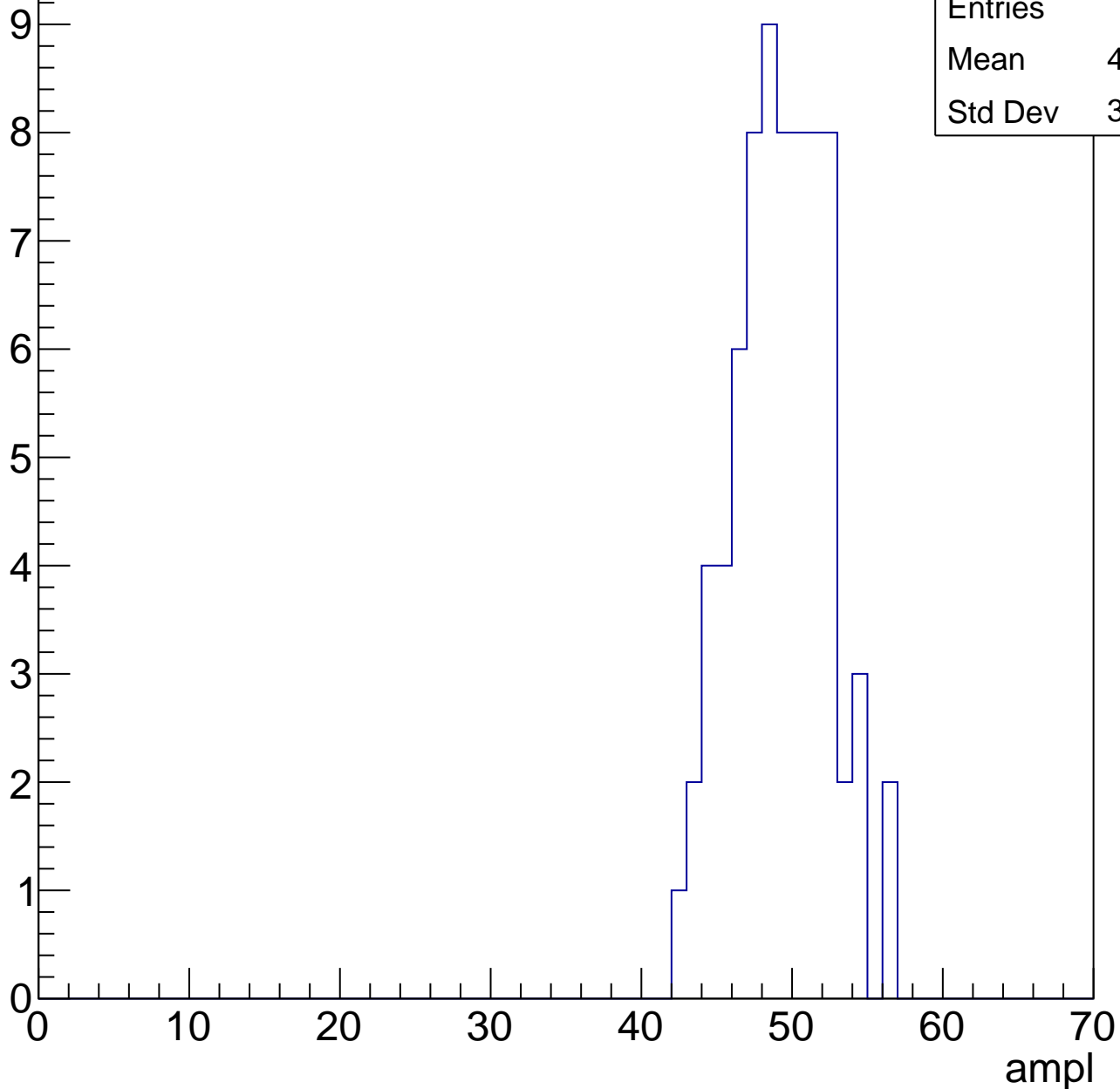
**Gaus Width: 3.7997**



# B1L003S, U11-ch97, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



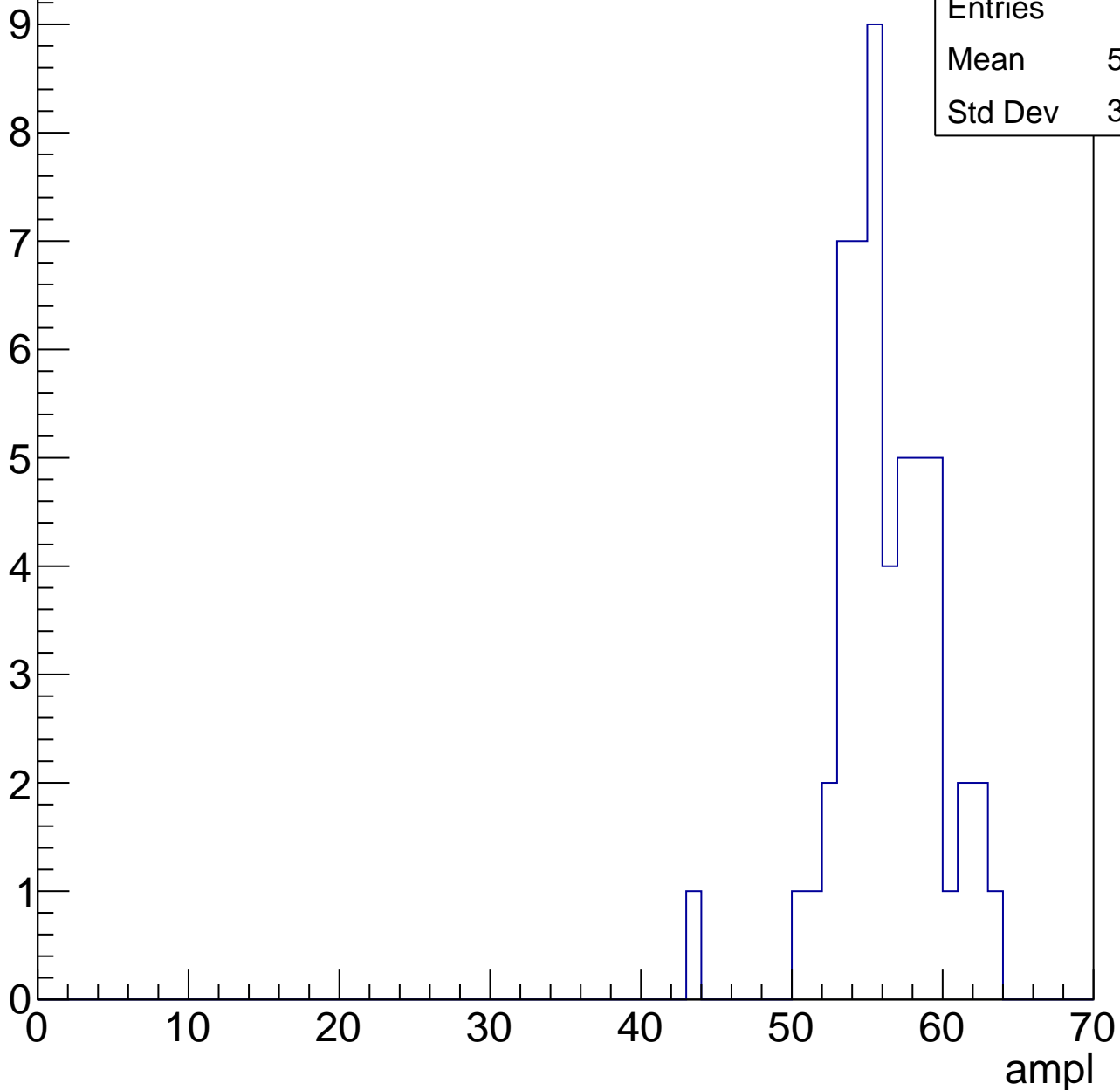
Entries	73
Mean	48.82
Std Dev	3.085

# B1L003S, U11-ch97, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

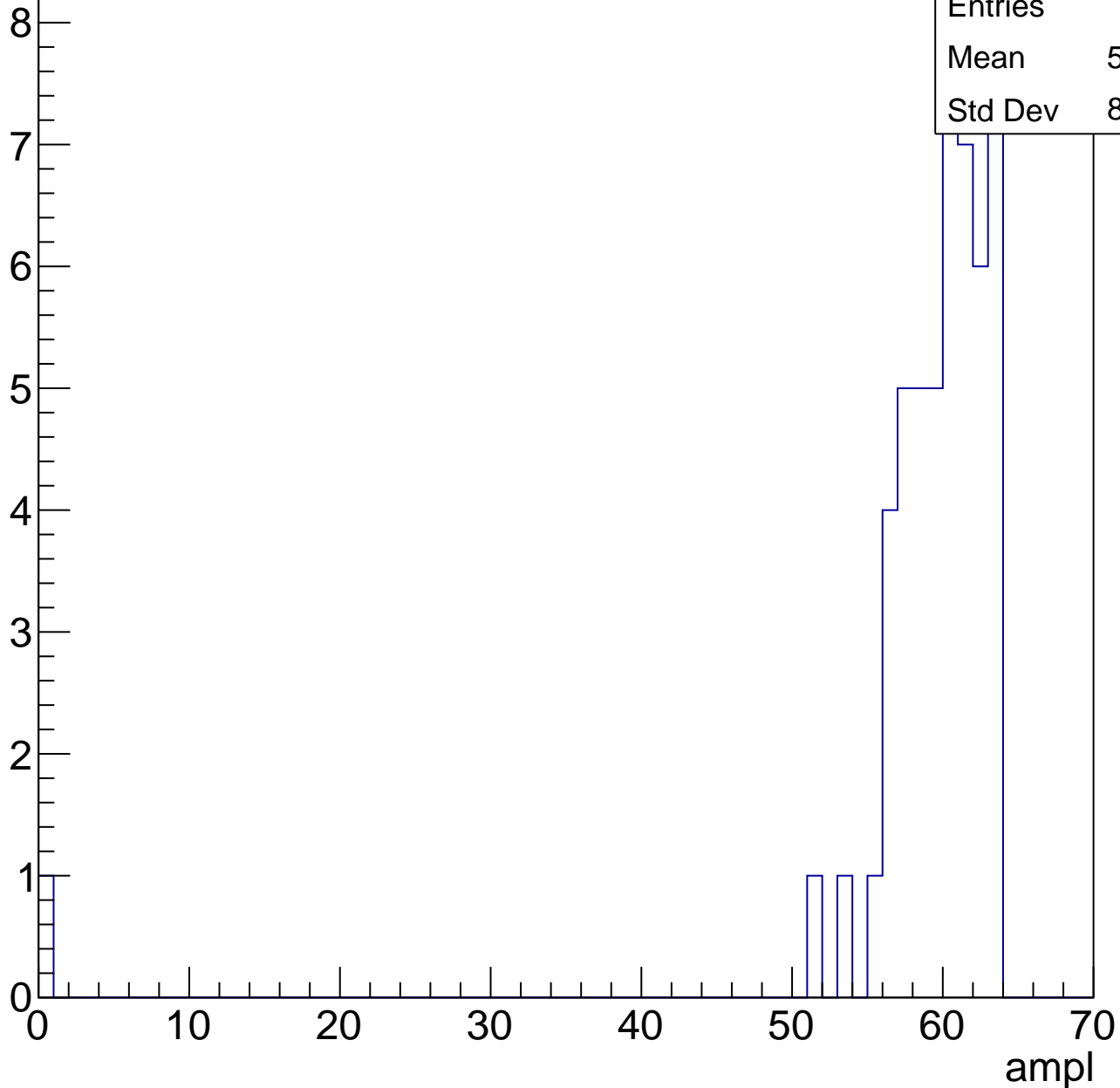
Entries	53
Mean	55.75
Std Dev	3.409



# B1L003S, U11-ch97, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U11-ch97, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

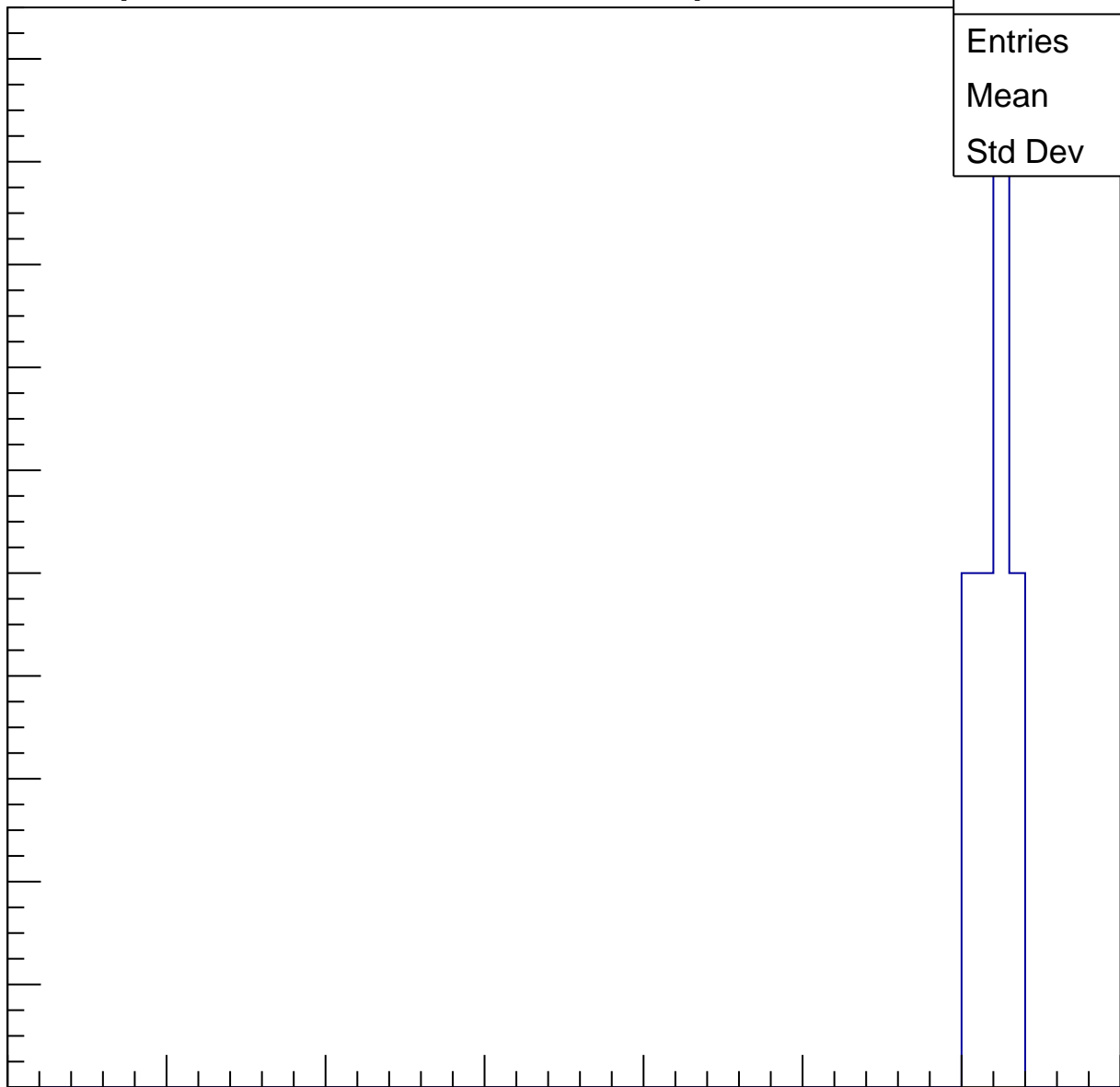
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	61.6
Std Dev	1.02

0 10 20 30 40 50 60 70

ampl





# B1L003S, U11-ch97, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U11-ch98, adc0

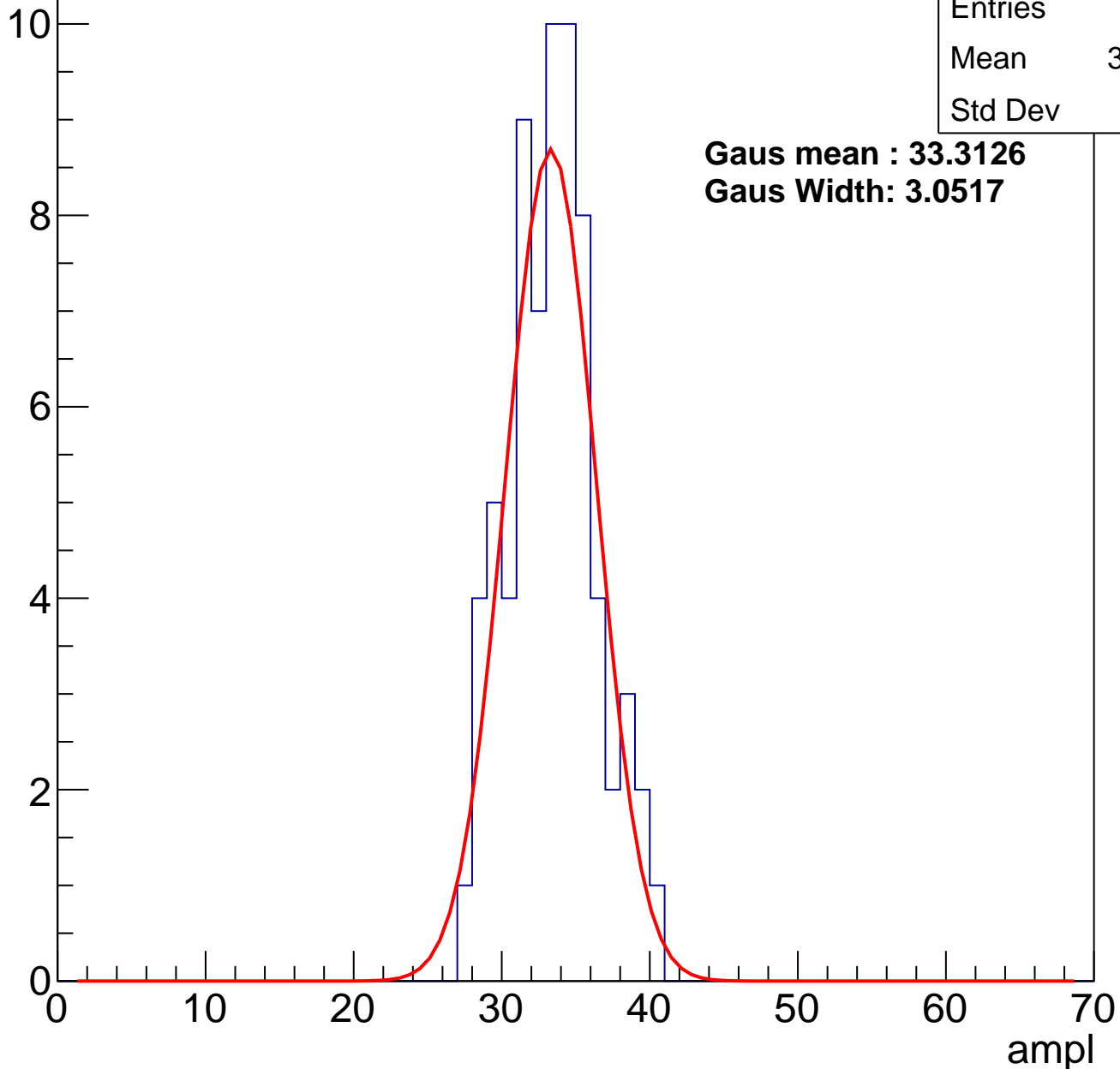
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	70
Mean	32.96
Std Dev	2.93

**Gaus mean : 33.3126**

**Gaus Width: 3.0517**

Entry



# B1L003S, U11-ch98, adc1

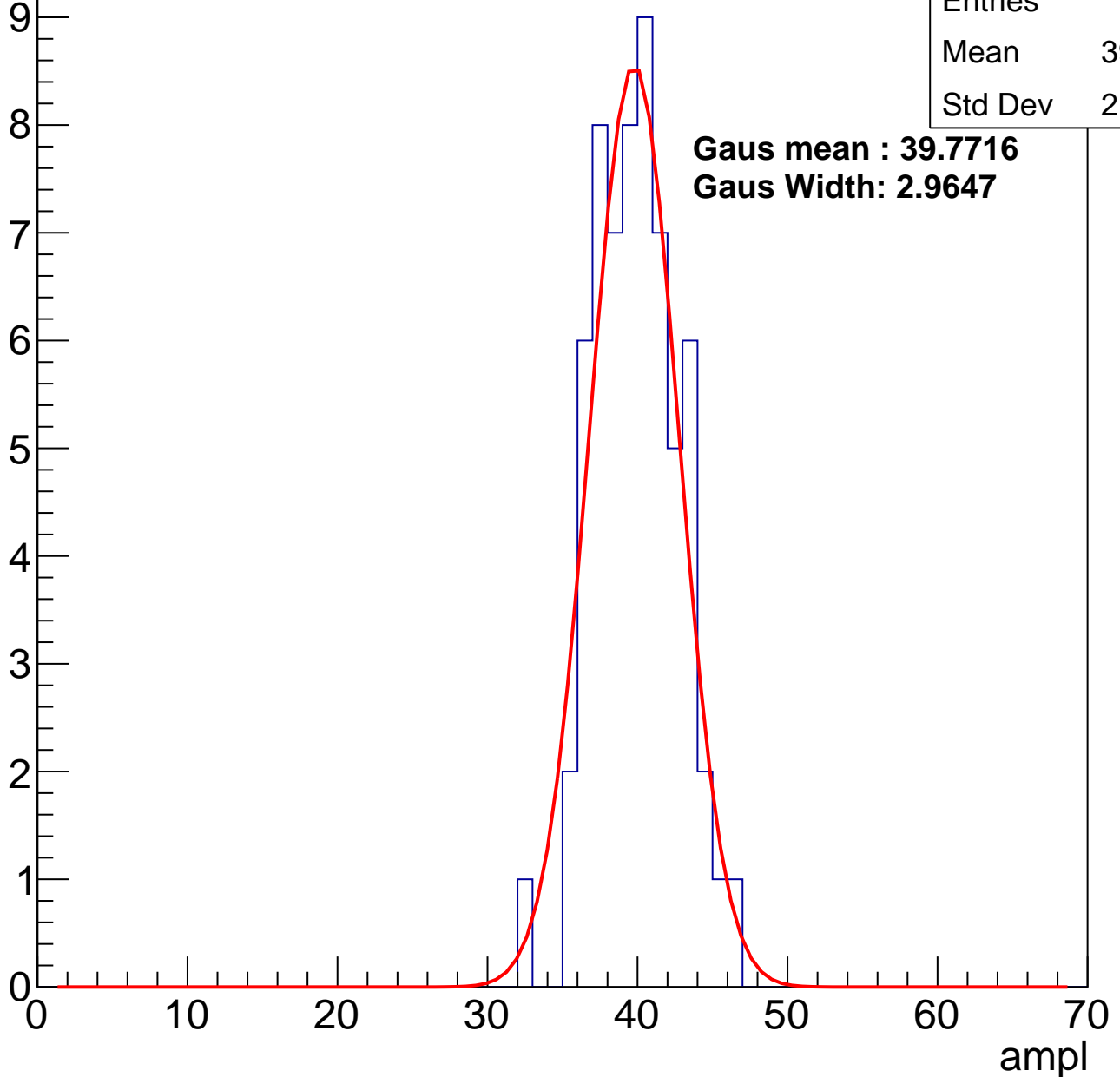
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	39.46
Std Dev	2.742

**Gaus mean : 39.7716**

**Gaus Width: 2.9647**



# B1L003S, U11-ch98, adc2

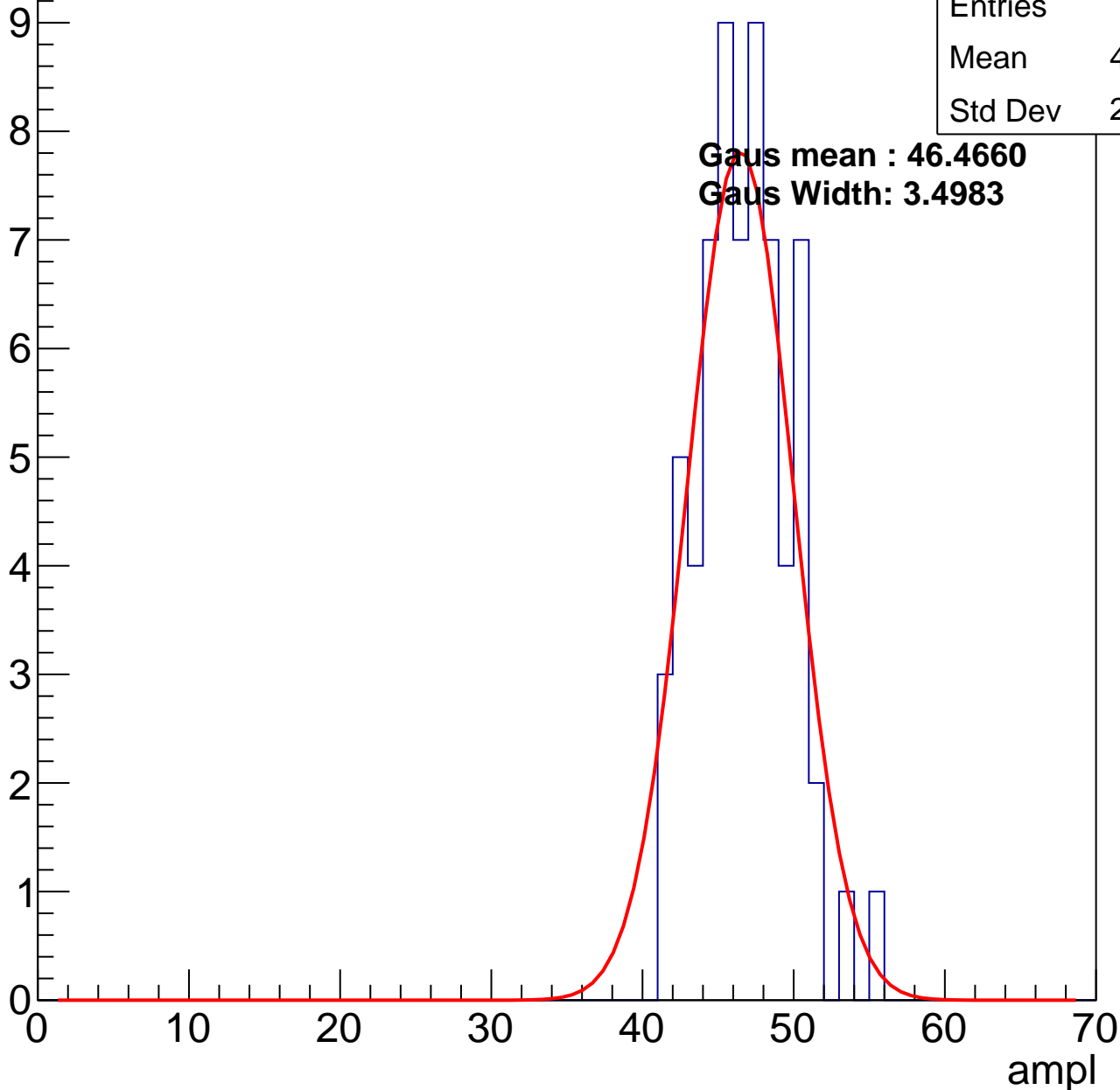
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	46.29
Std Dev	2.984

**Gaus mean : 46.4660**

**Gaus Width: 3.4983**



# B1L003S, U11-ch98, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

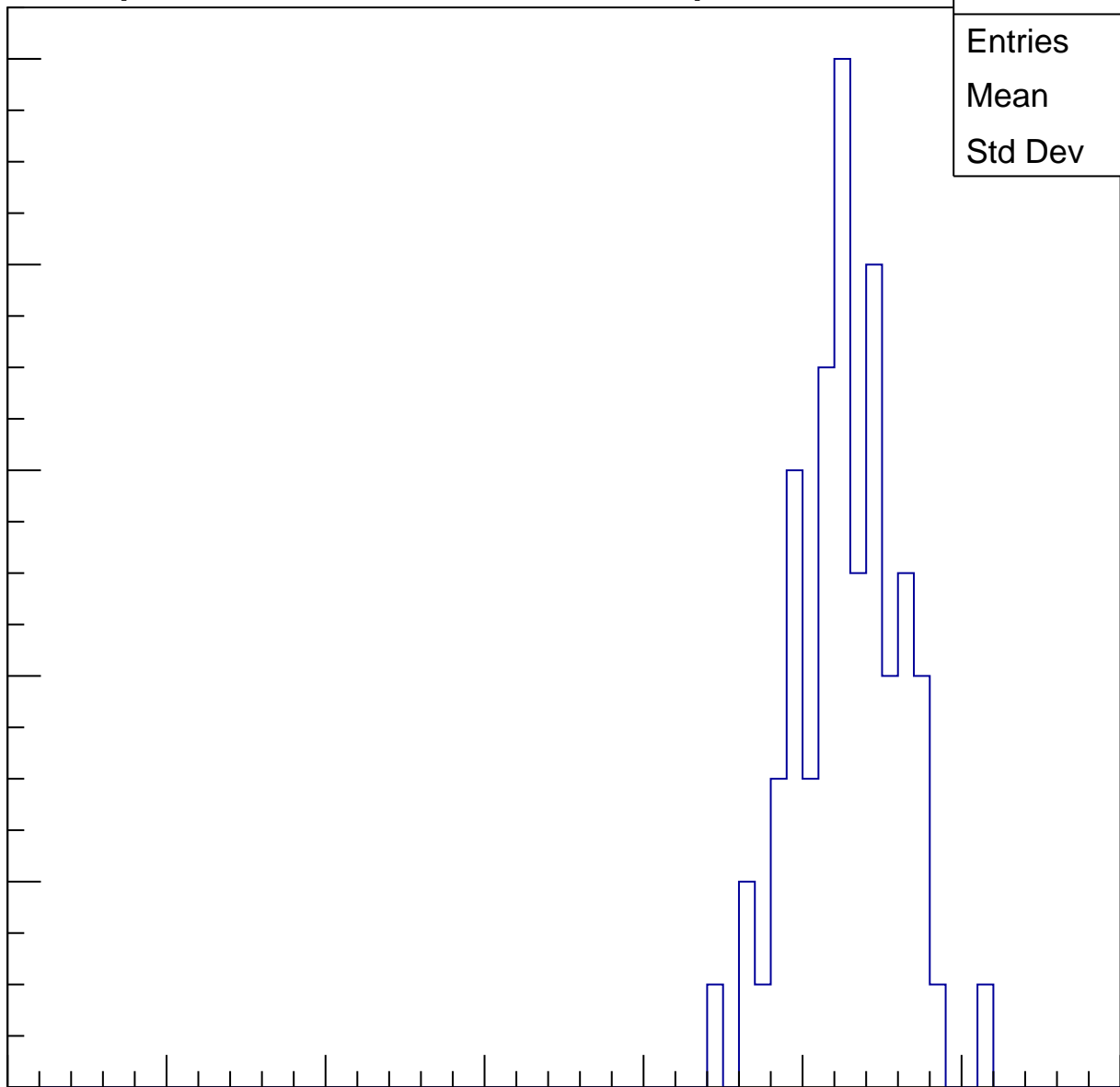
Entries	61
Mean	52.33
Std Dev	3.253

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

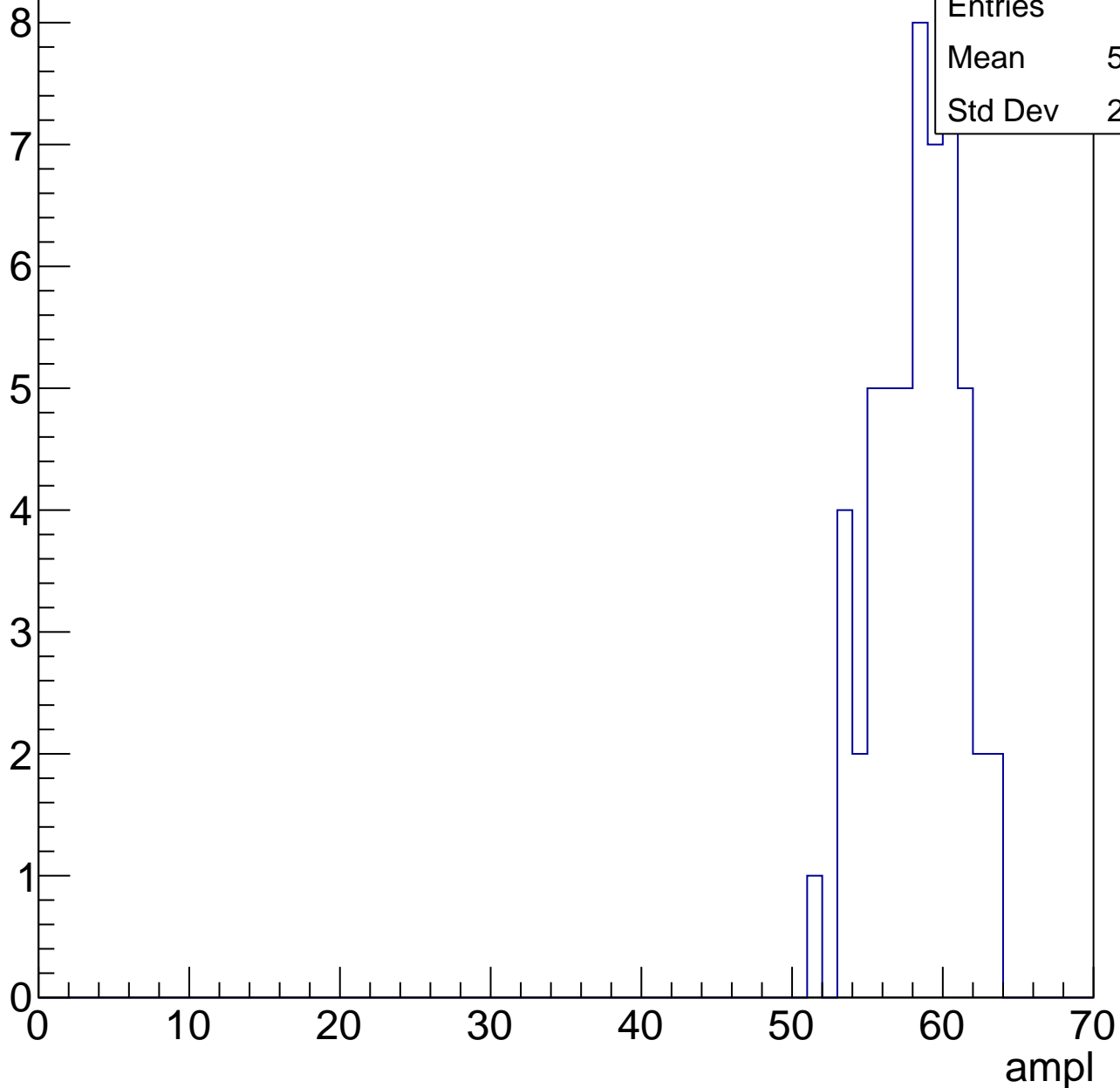
ampl



# B1L003S, U11-ch98, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

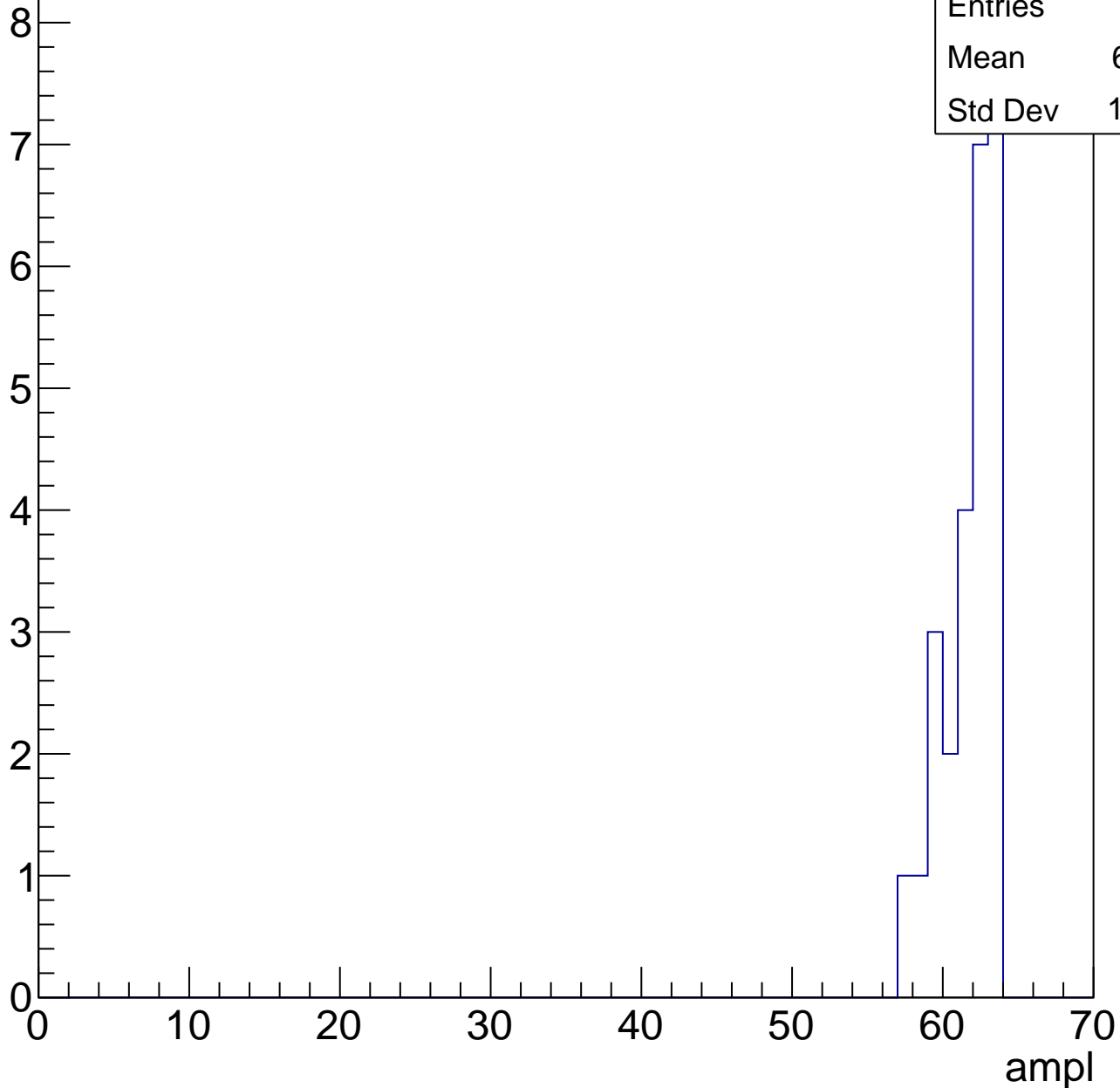
Entry



# B1L003S, U11-ch98, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

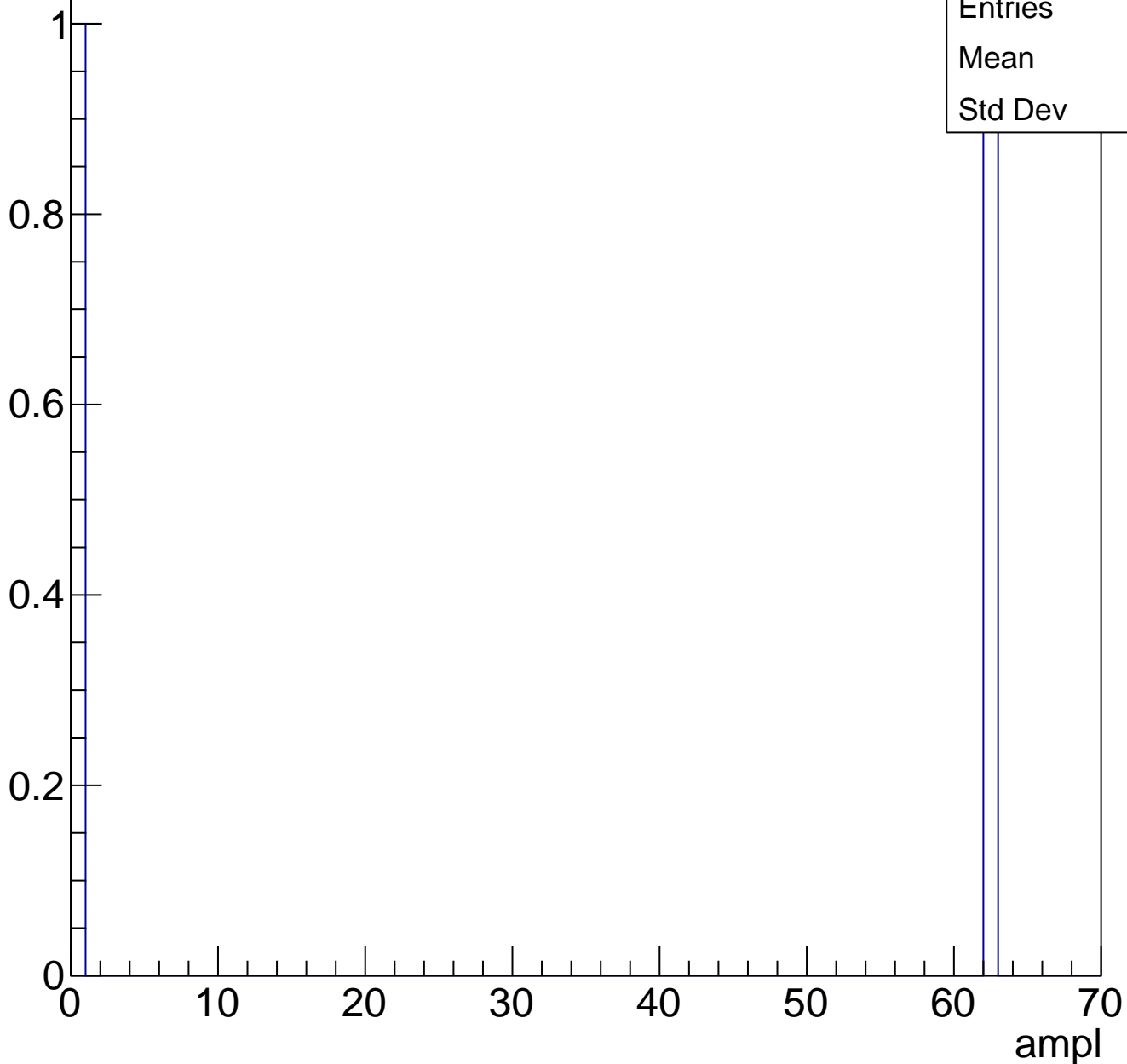
Entry



# B1L003S, U11-ch98, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

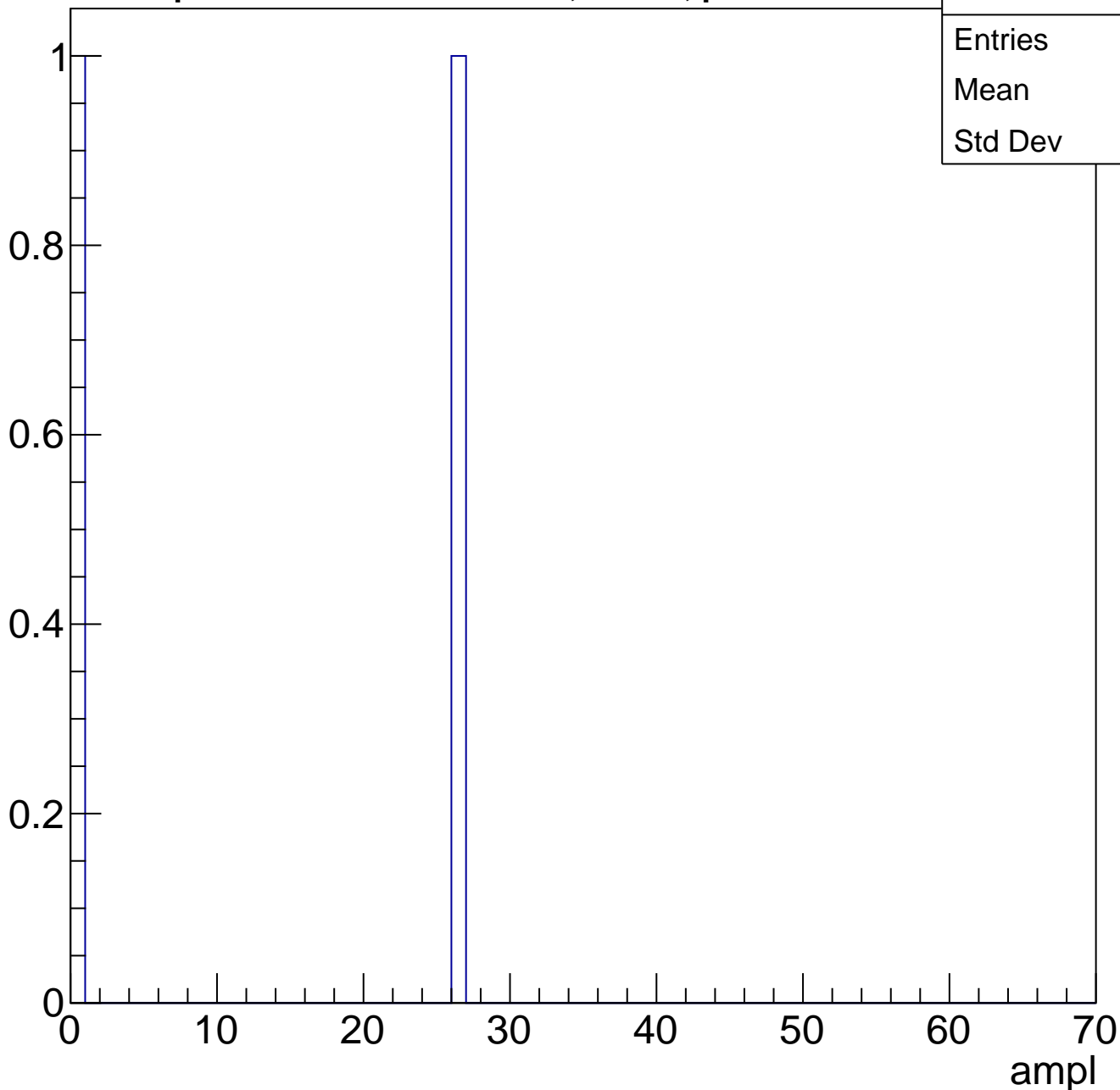




# B1L003S, U11-ch98, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	13
Std Dev	13

# B1L003S, U11-ch99, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	73
Mean	30.99
Std Dev	3.09

**Gaus mean : 31.4798**

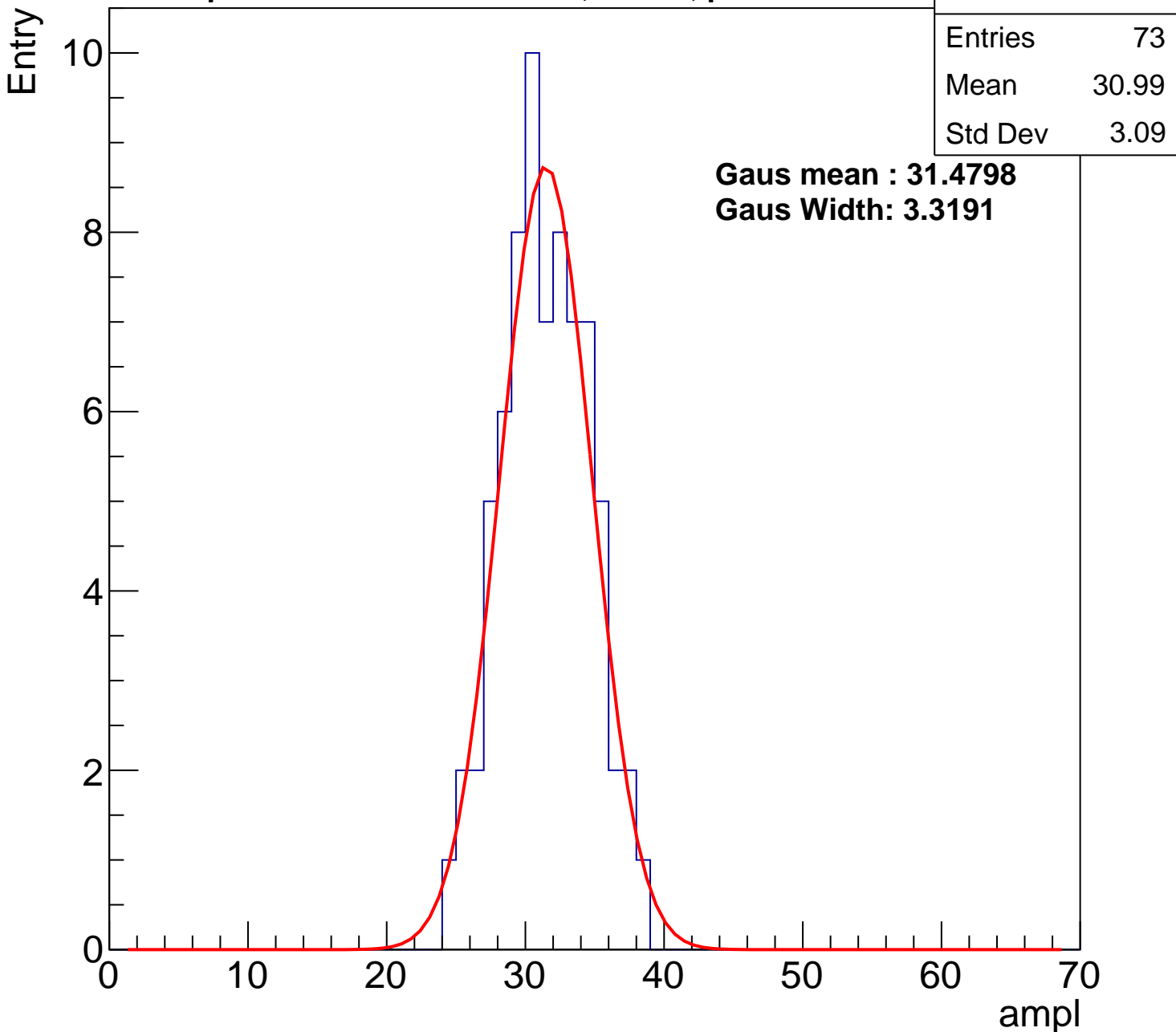
**Gaus Width: 3.3191**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L003S, U11-ch99, adc1

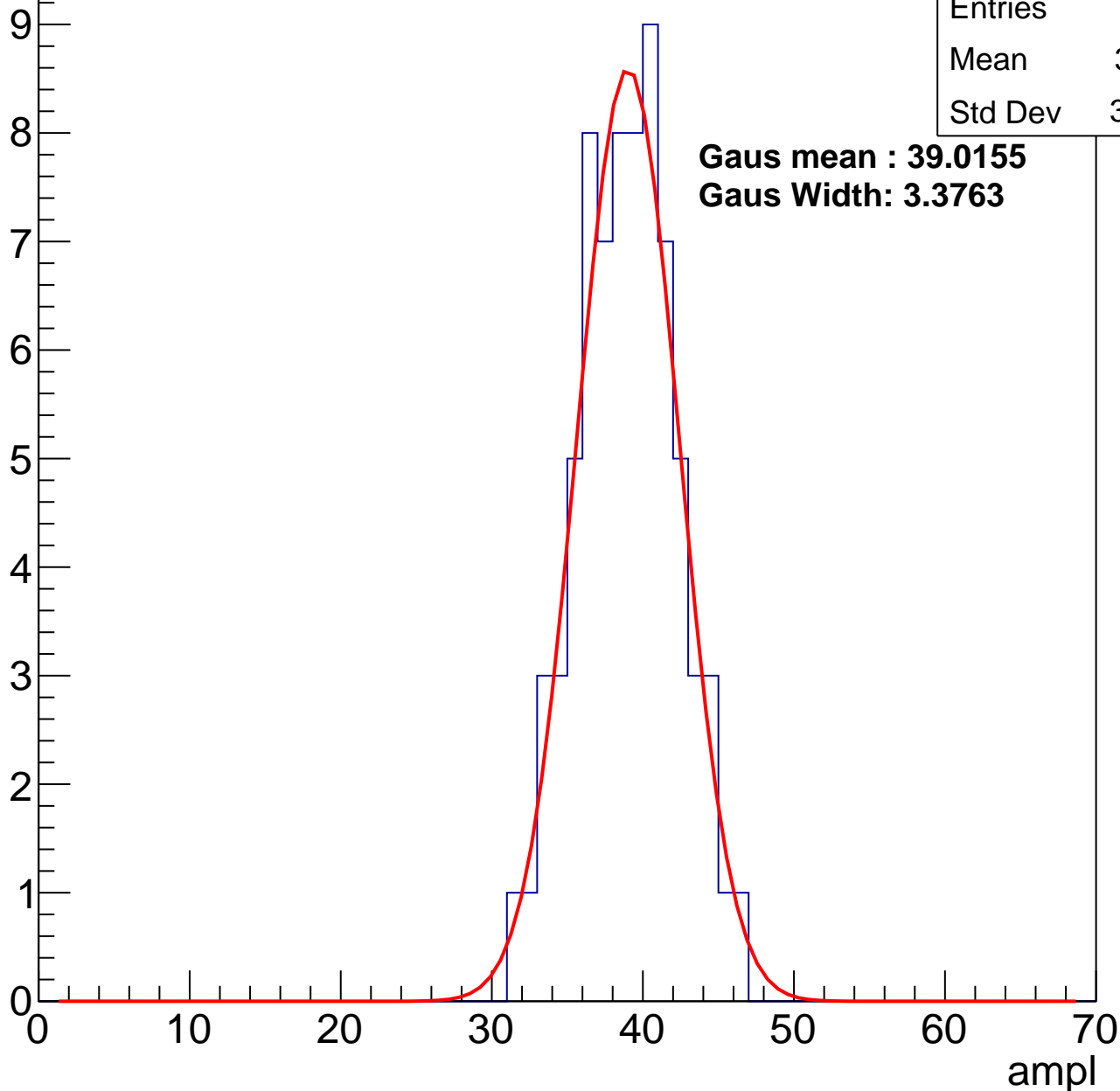
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	73
Mean	38.51
Std Dev	3.219

**Gaus mean : 39.0155**

**Gaus Width: 3.3763**



# B1L003S, U11-ch99, adc2

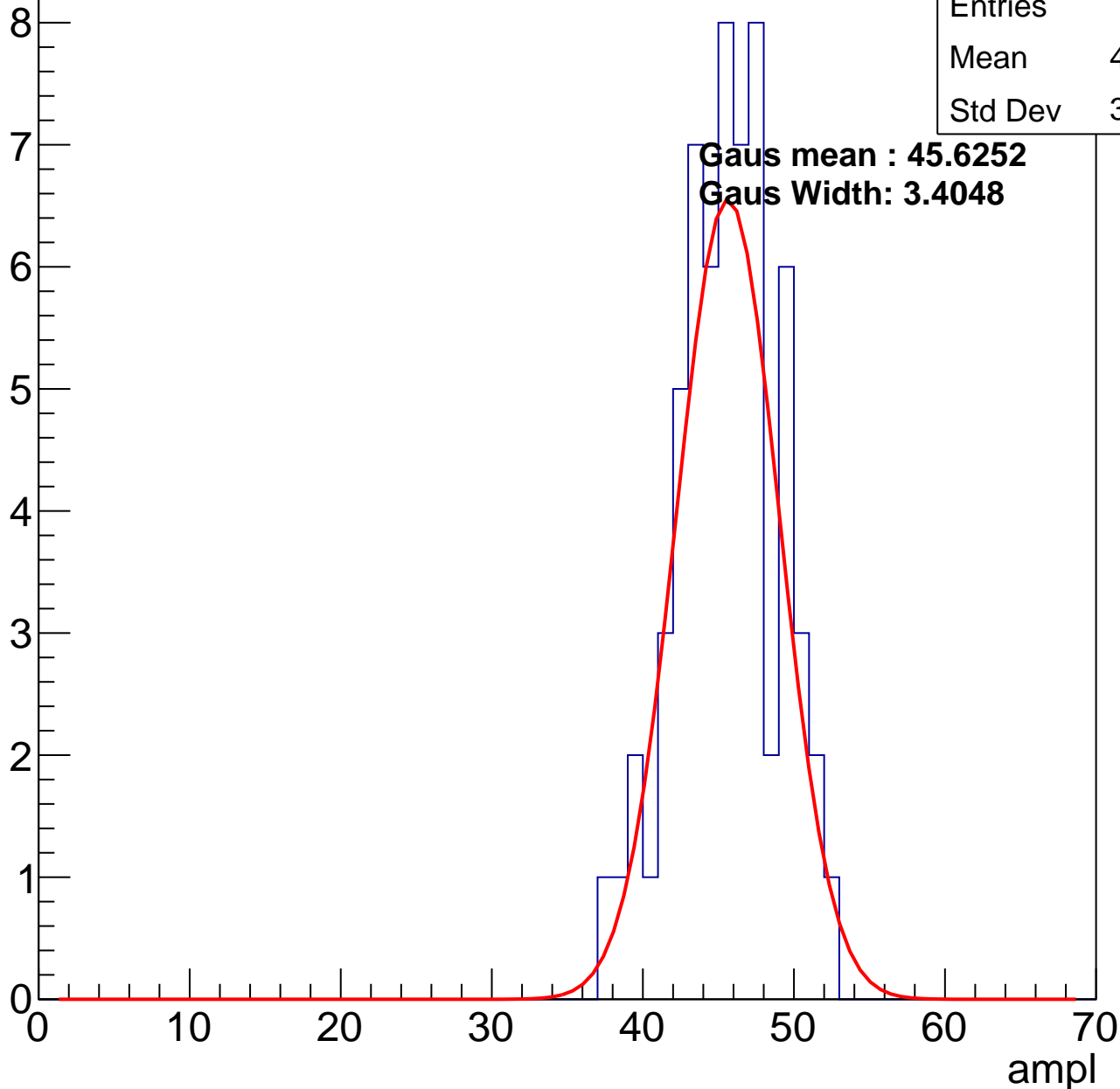
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	45.13
Std Dev	3.297

**Gaus mean : 45.6252**

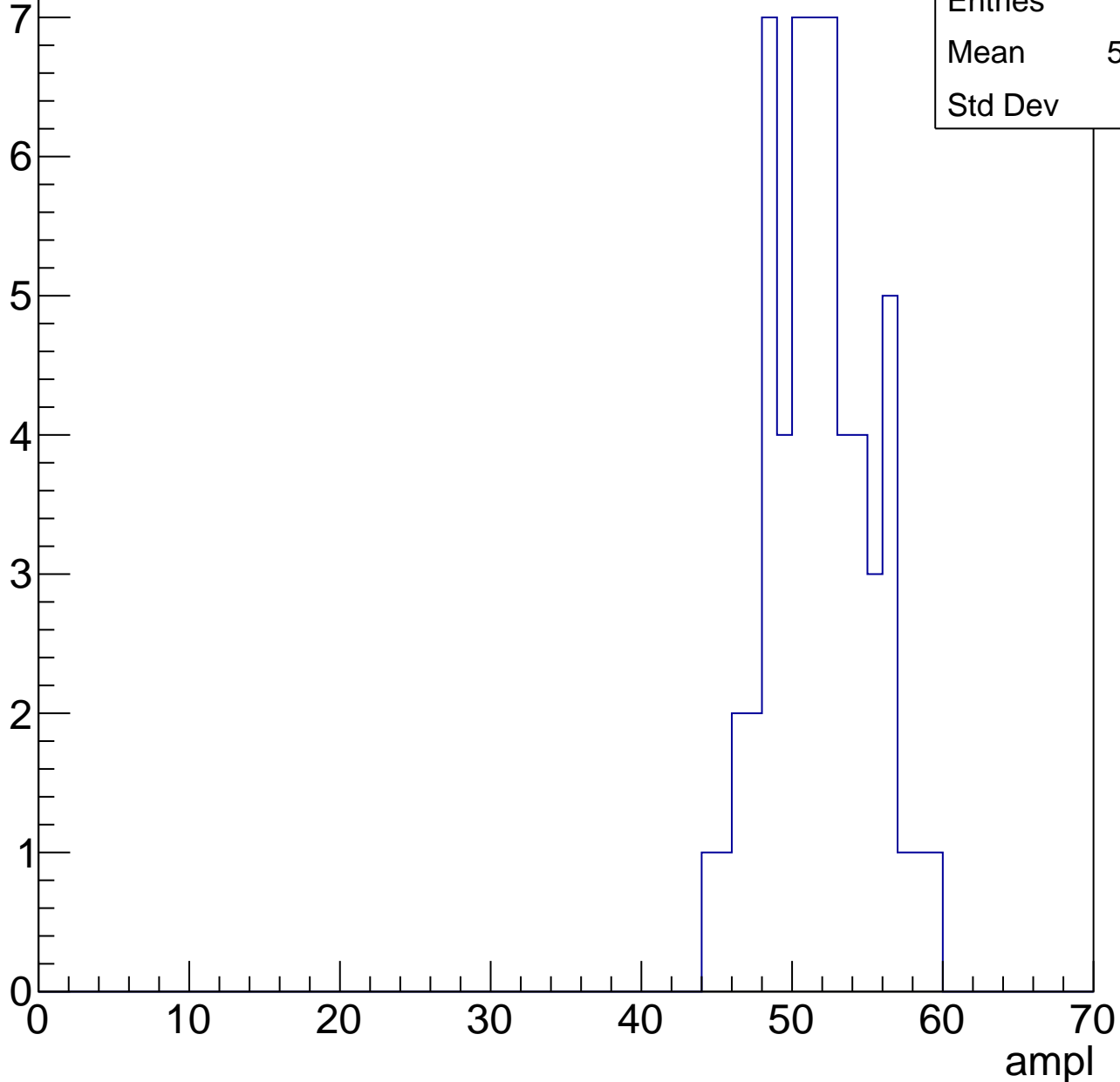
**Gaus Width: 3.4048**



# B1L003S, U11-ch99, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

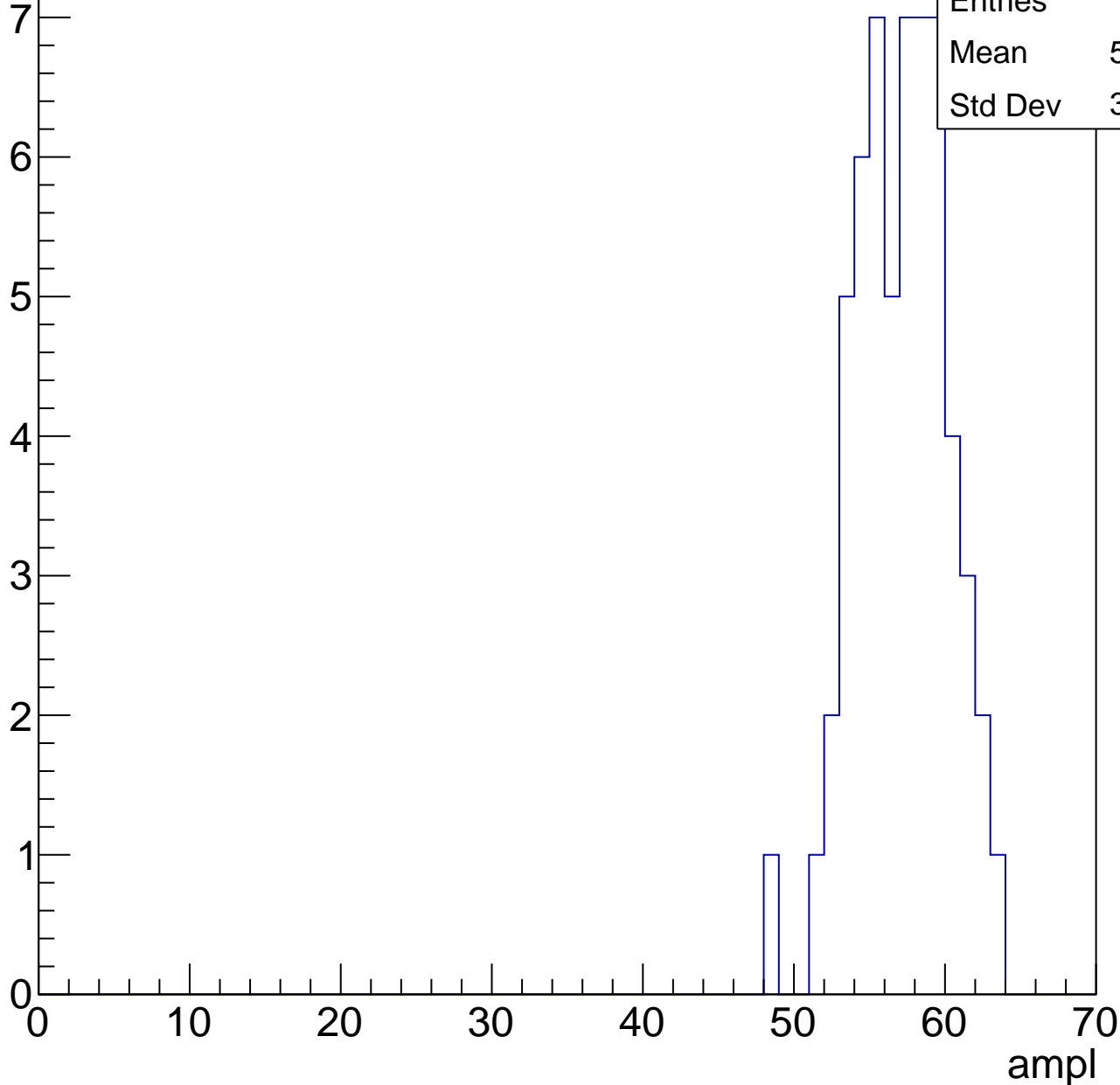


Entries	57
Mean	51.32
Std Dev	3.32

# B1L003S, U11-ch99, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

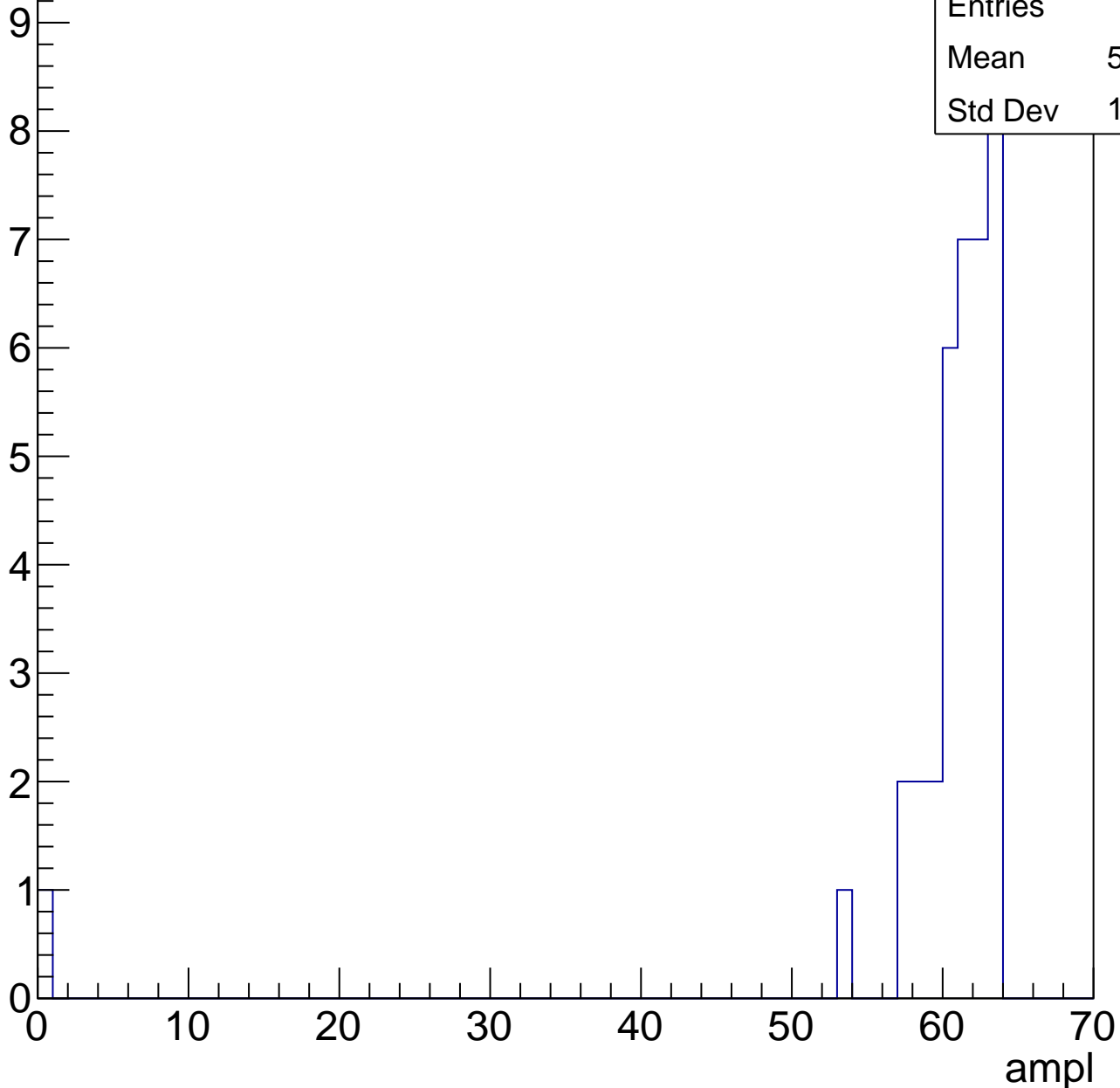


# B1L003S, U11-ch99, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	37
Mean	59.16
Std Dev	10.09



# B1L003S, U11-ch99, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch99, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U11-ch100, adc0

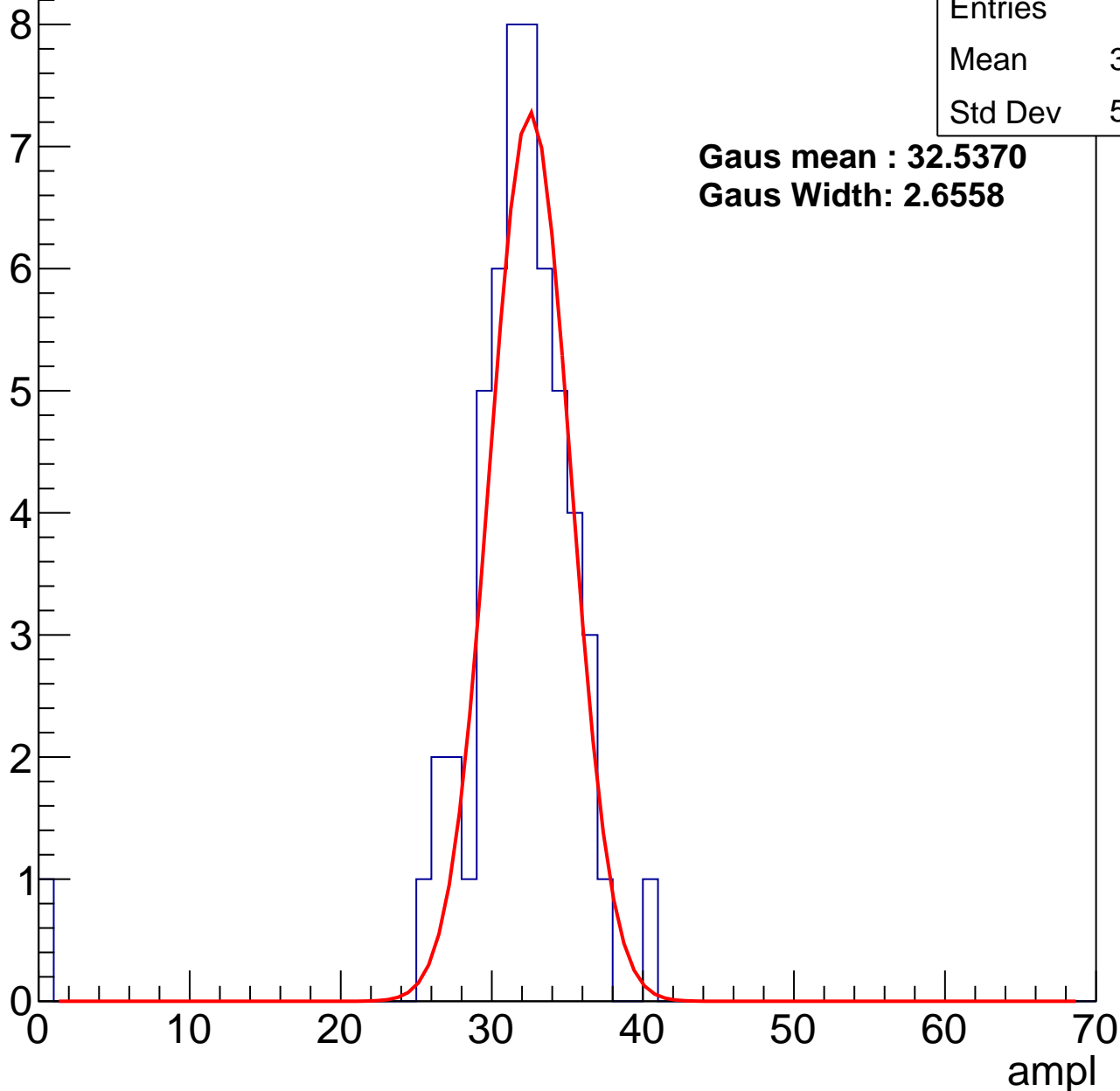
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	54
Mean	31.13
Std Dev	5.175

**Gaus mean : 32.5370**

**Gaus Width: 2.6558**



# B1L003S, U11-ch100, adc1

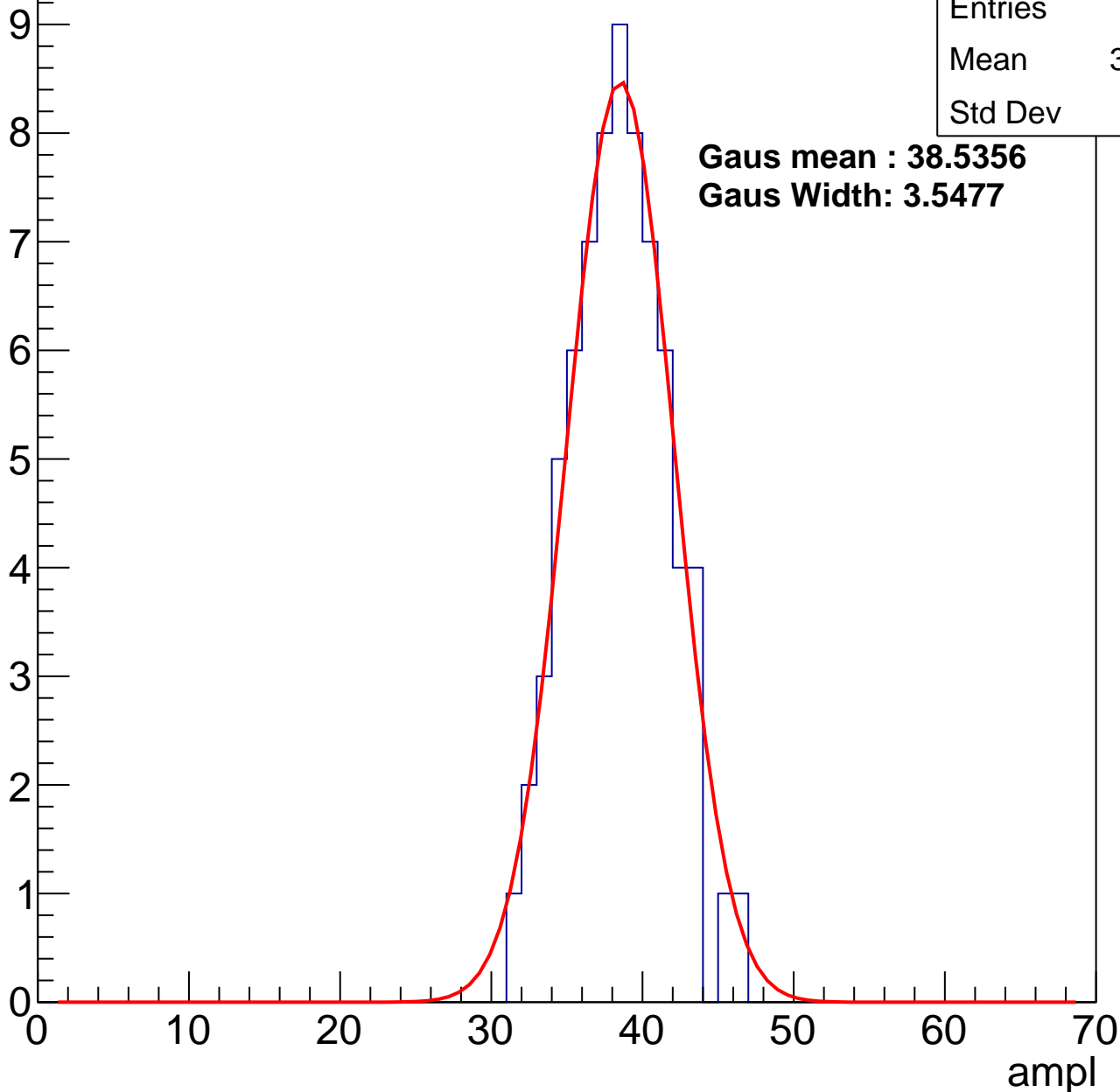
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	72
Mean	37.96
Std Dev	3.19

**Gaus mean : 38.5356**

**Gaus Width: 3.5477**



# B1L003S, U11-ch100, adc2

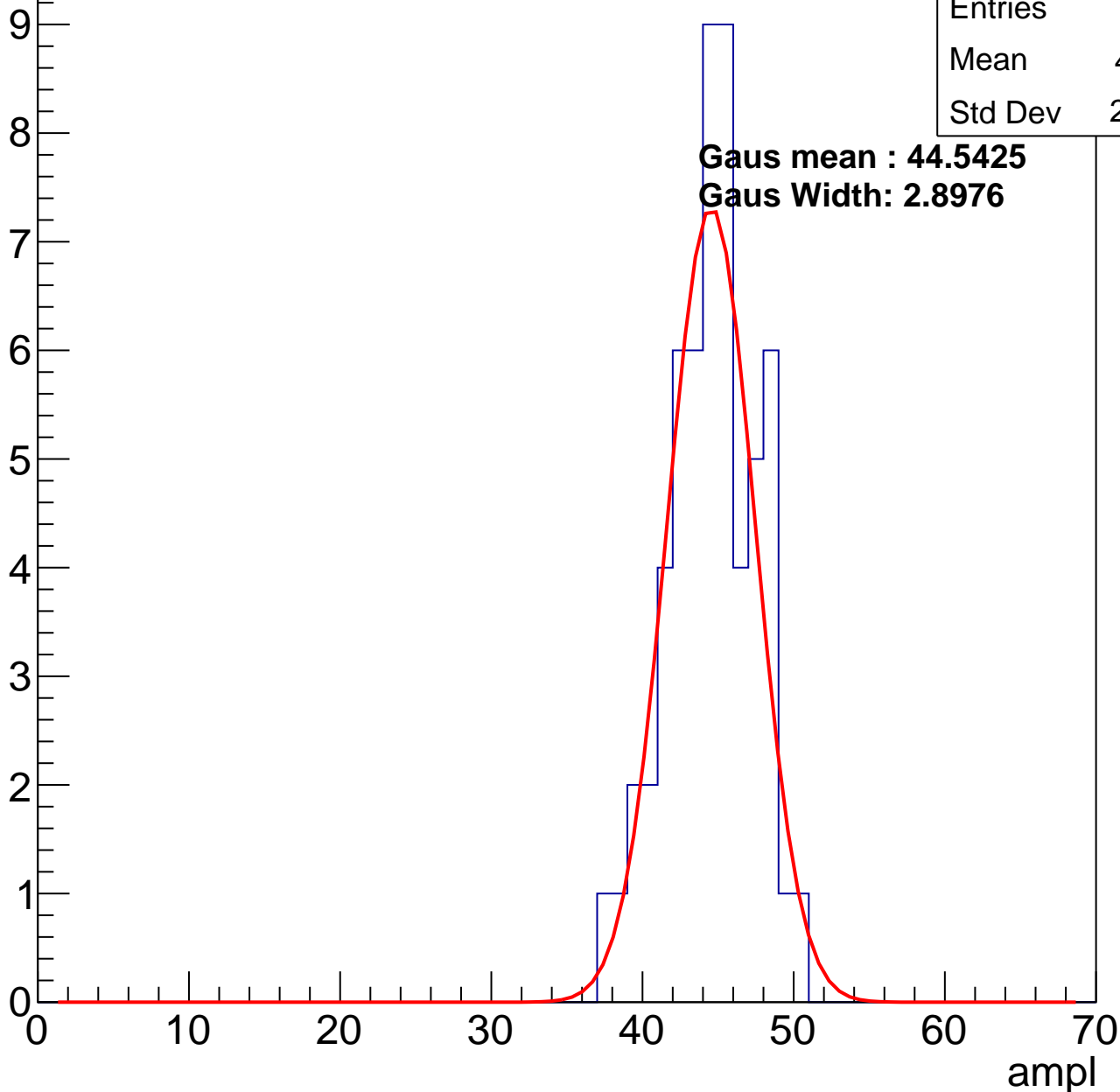
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	44.11
Std Dev	2.839

**Gaus mean : 44.5425**

**Gaus Width: 2.8976**

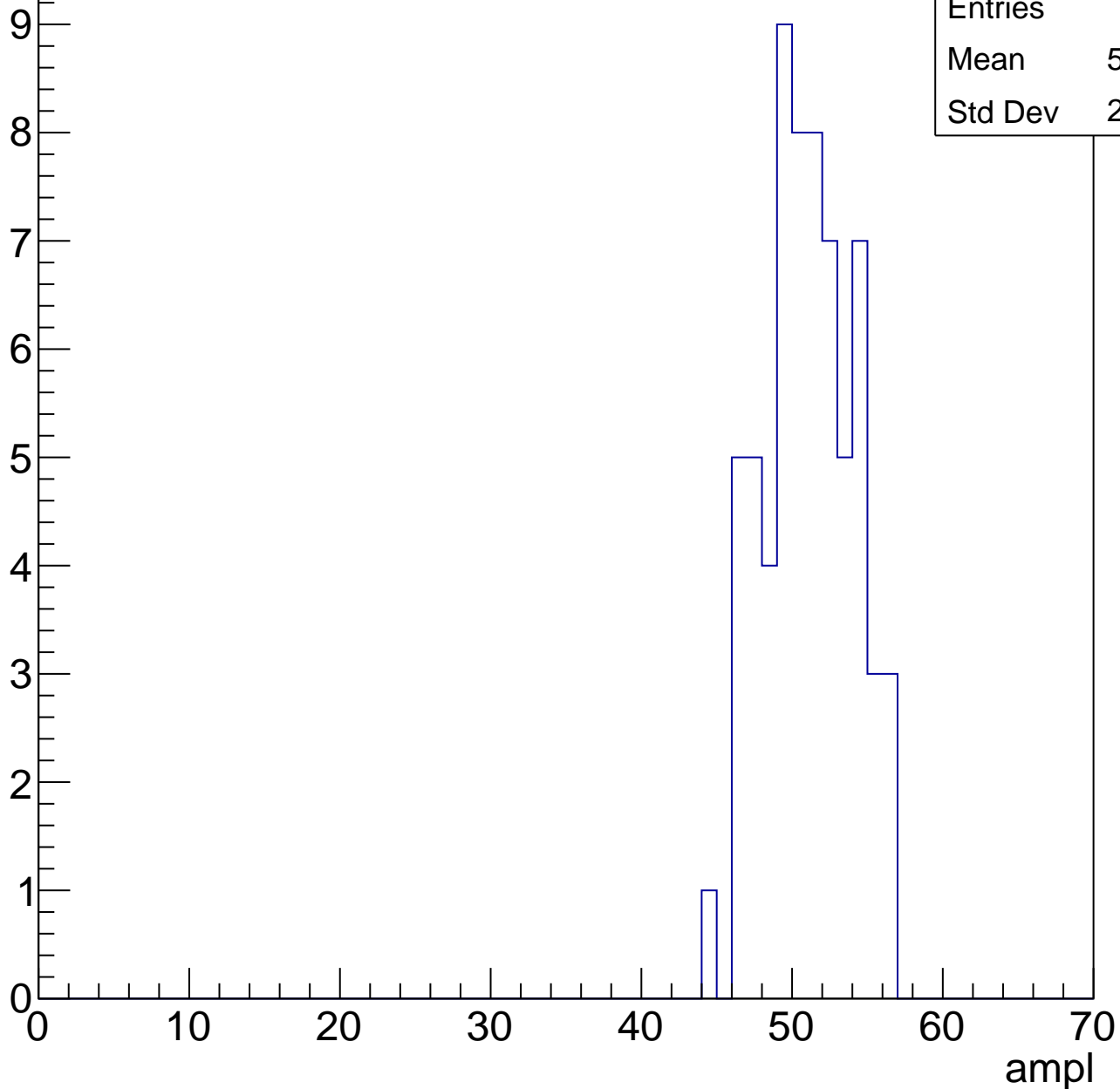


# B1L003S, U11-ch100, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	50.62
Std Dev	2.875

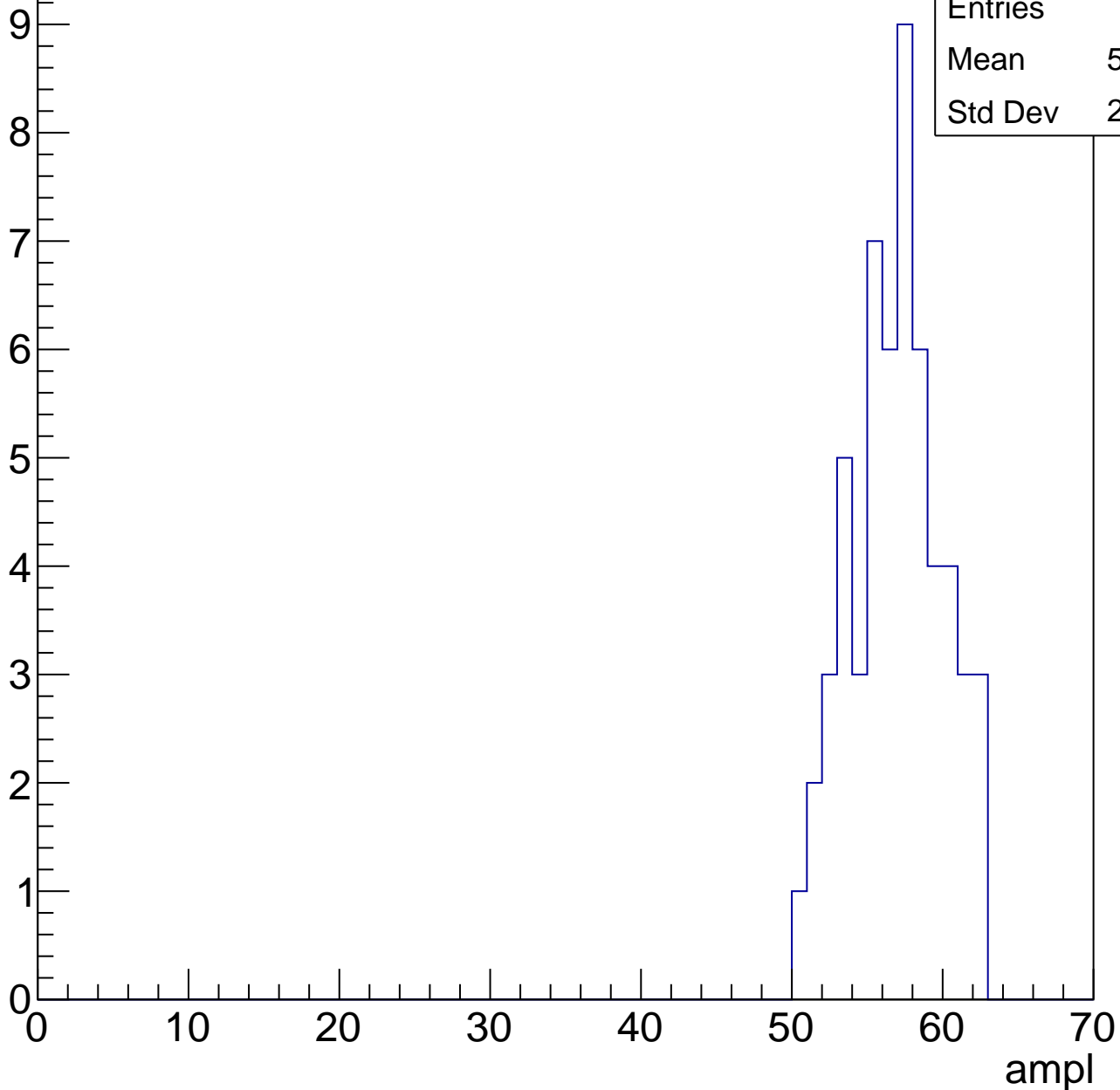


# B1L003S, U11-ch100, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	56.46
Std Dev	2.994



# B1L003S, U11-ch100, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	42
Mean	59.24
Std Dev	9.441

Entry

10

8

6

4

2

0

0

10

20

30

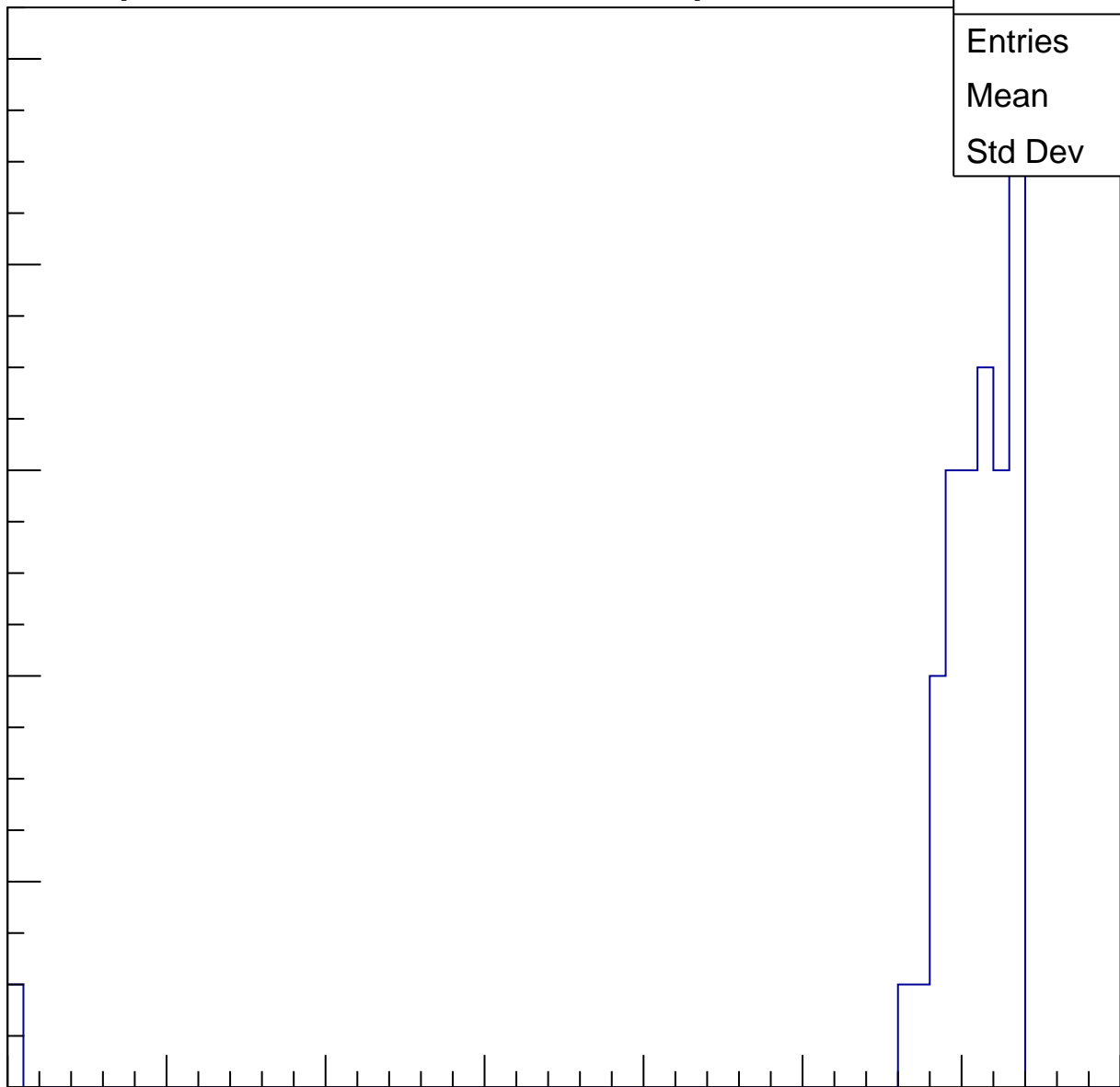
40

50

60

70

ampl



# B1L003S, U11-ch100, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

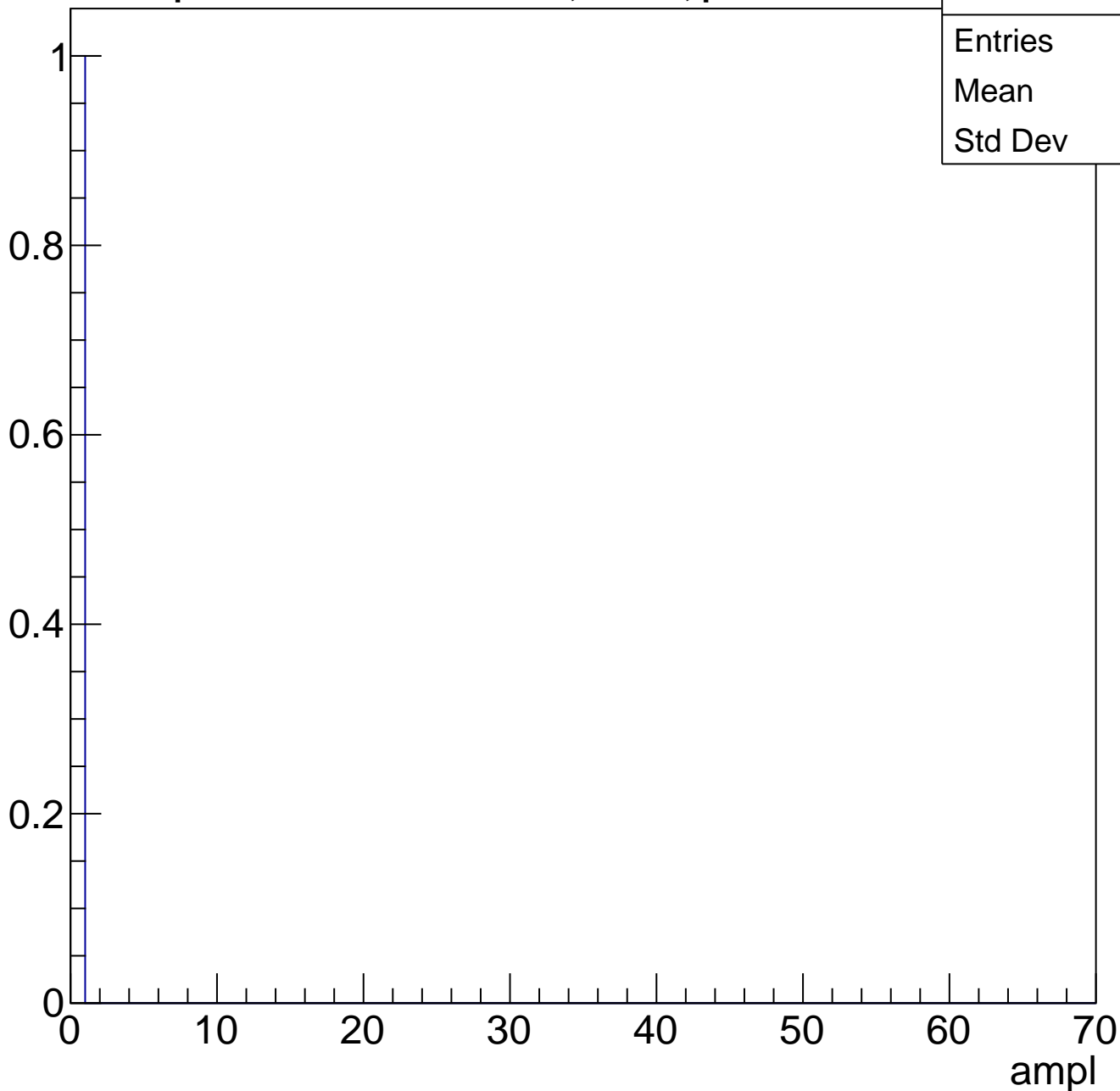




# B1L003S, U11-ch100, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U11-ch101, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	80
Mean	31.32
Std Dev	3.517

**Gaus mean : 32.0491**

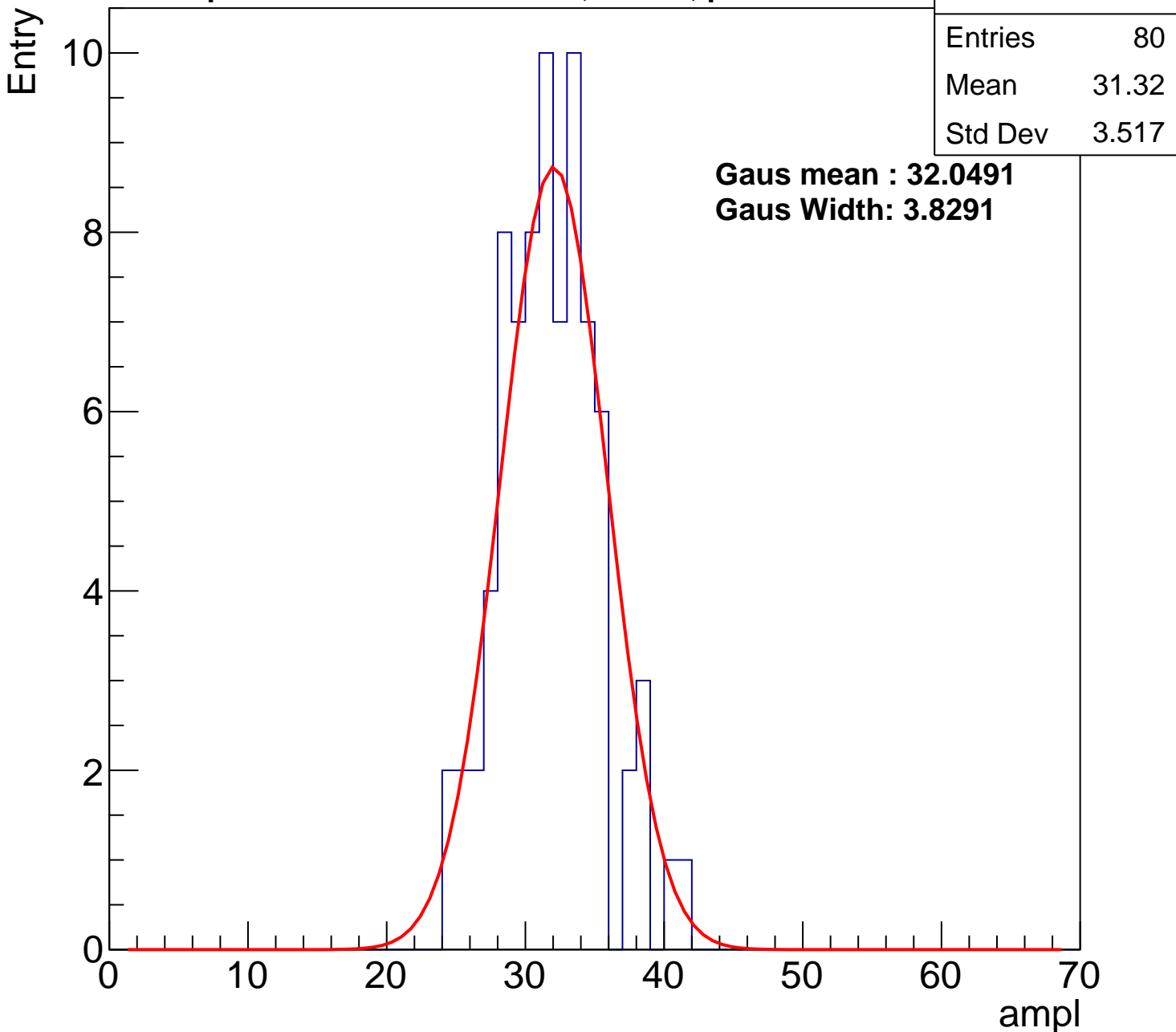
**Gaus Width: 3.8291**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U11-ch101, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	65
Mean	38.8
Std Dev	3.114

**Gaus mean : 39.1117**

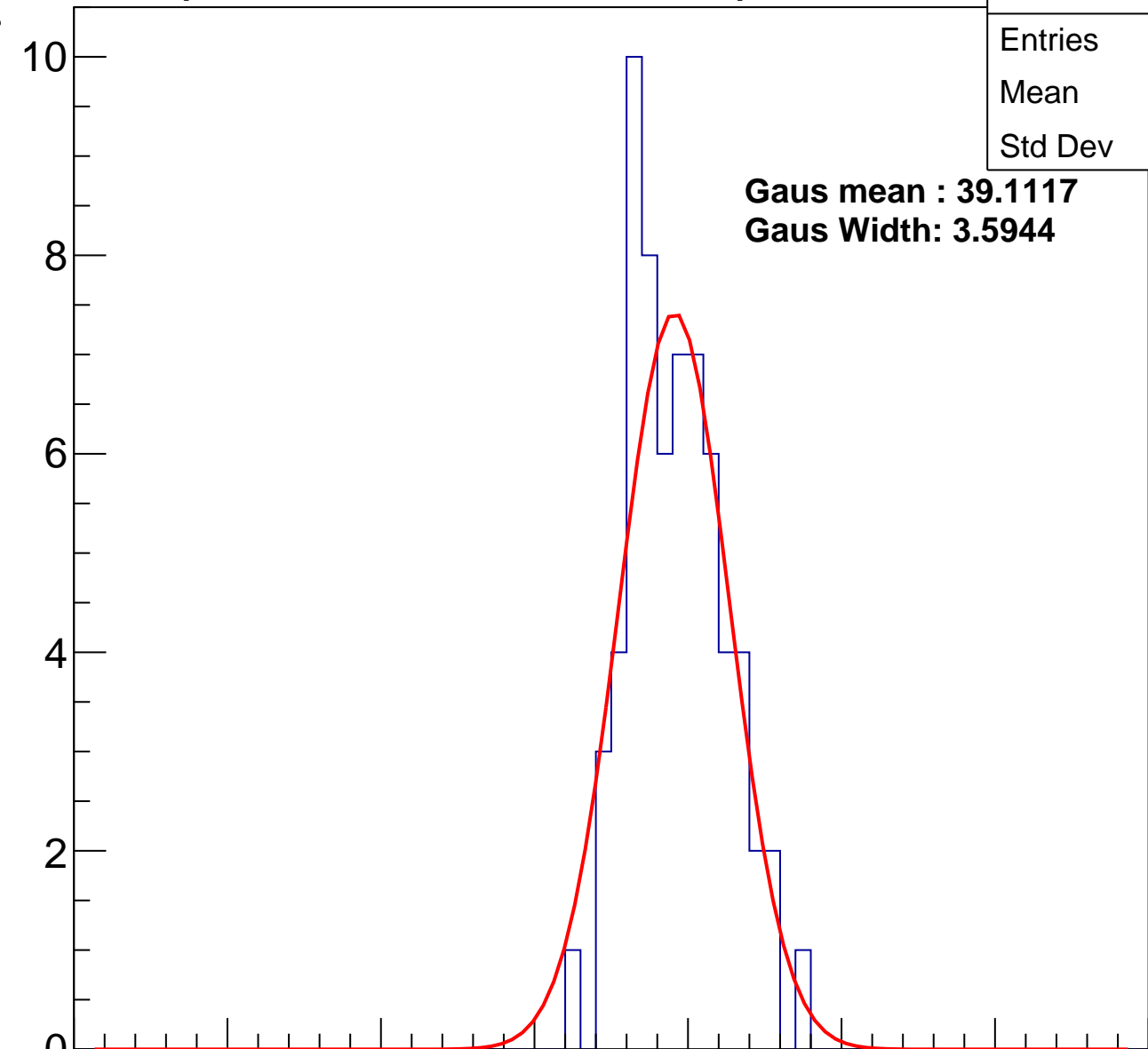
**Gaus Width: 3.5944**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L003S, U11-ch101, adc2

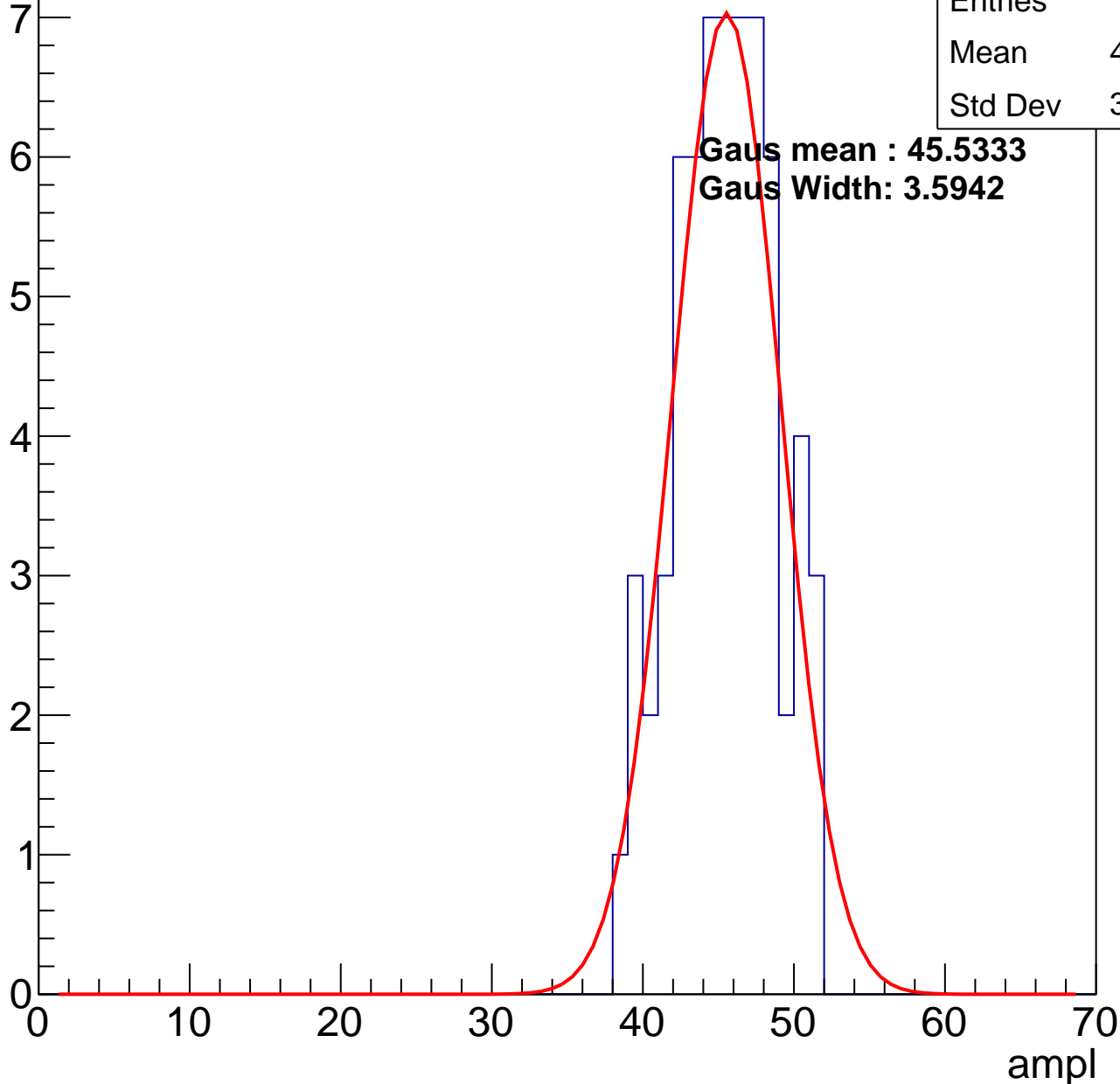
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	45.02
Std Dev	3.233

**Gaus mean : 45.5333**

**Gaus Width: 3.5942**

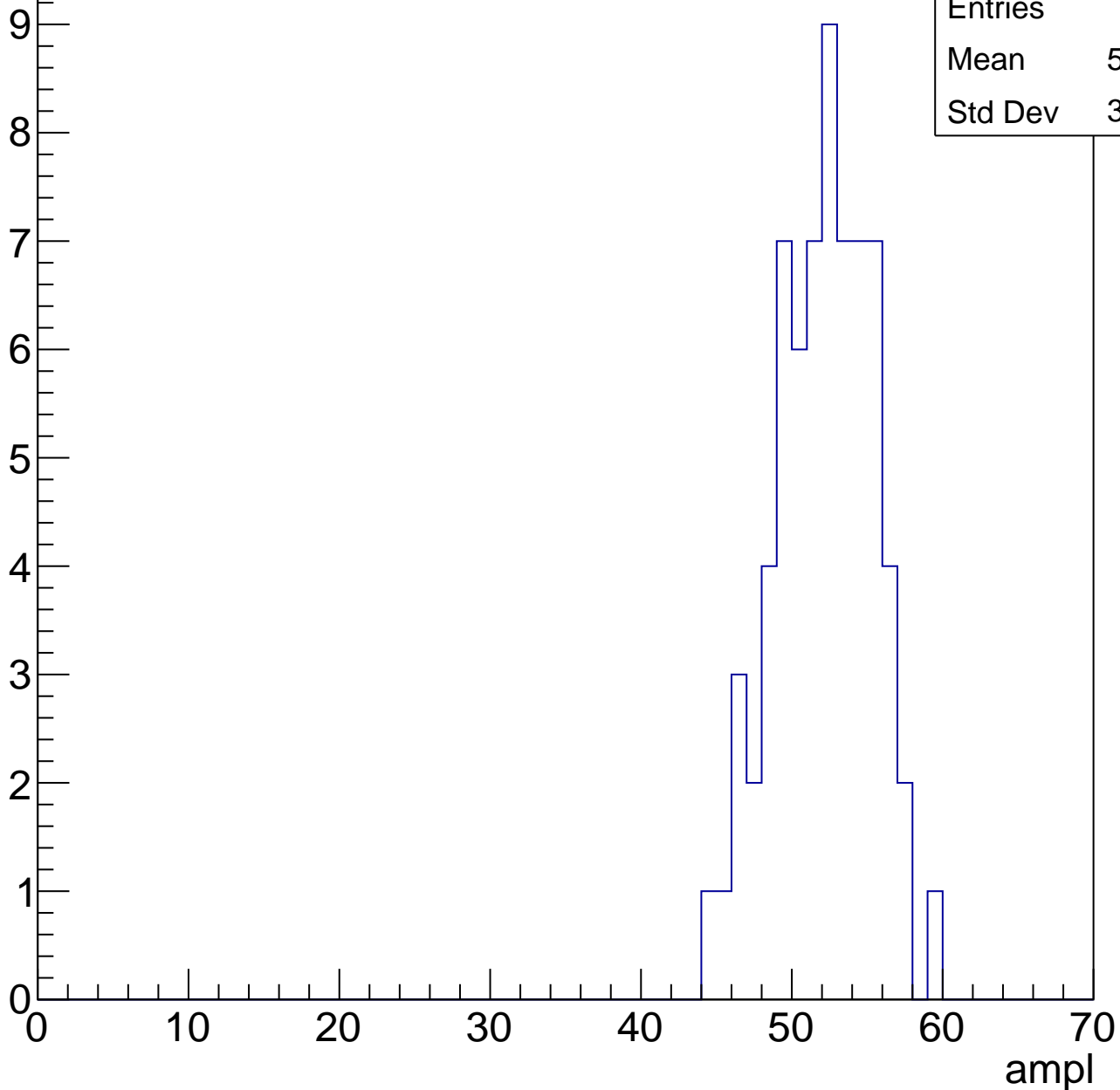


# B1L003S, U11-ch101, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	51.65
Std Dev	3.166



# B1L003S, U11-ch101, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

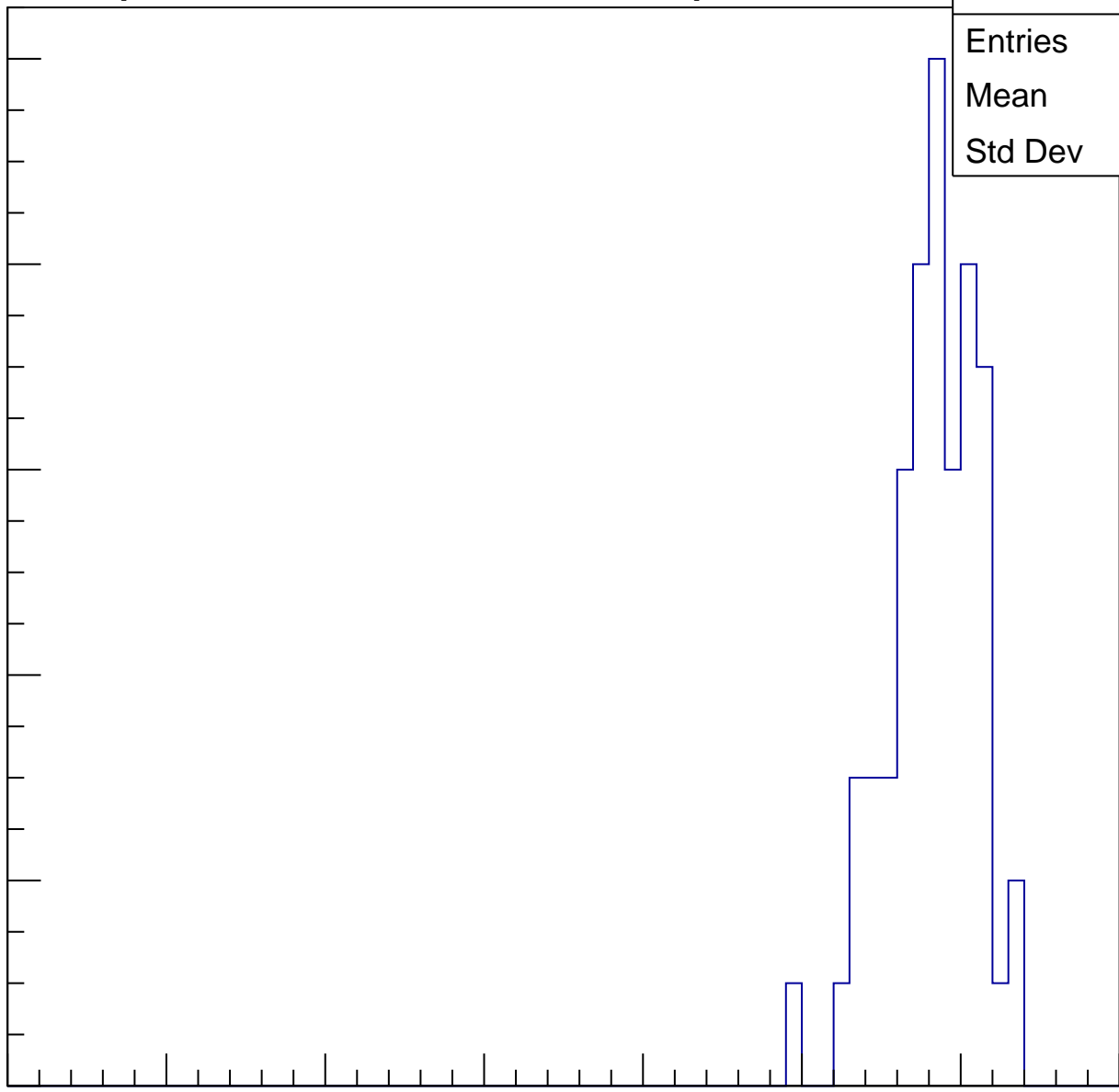
Entries	59
Mean	57.76
Std Dev	2.8

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

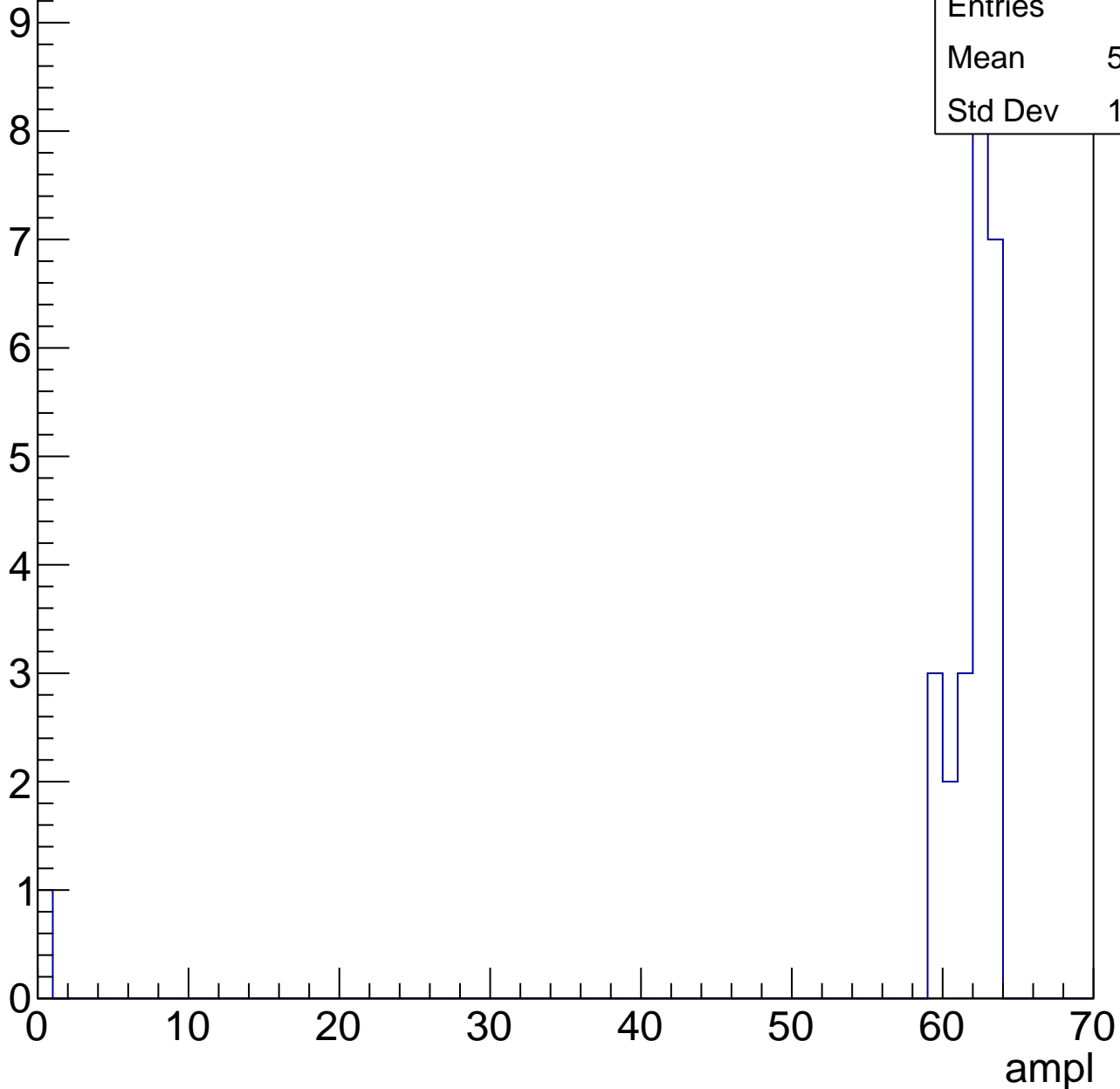


# B1L003S, U11-ch101, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	25
Mean	59.16
Std Dev	12.14



# B1L003S, U11-ch101, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	63
Std Dev	0



# B1L003S, U11-ch101, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U11-ch102, adc0

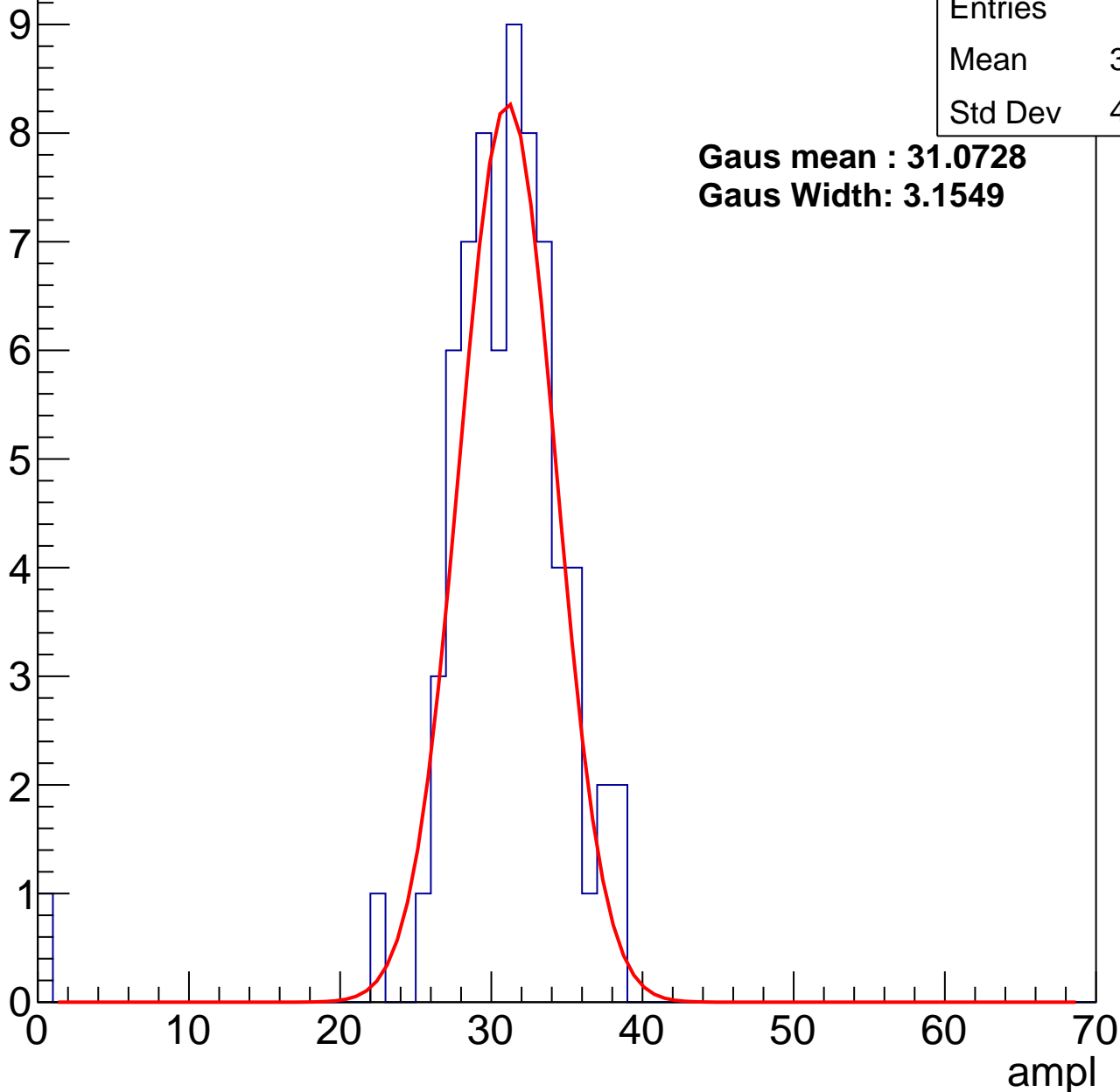
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	30.33
Std Dev	4.854

**Gaus mean : 31.0728**

**Gaus Width: 3.1549**



# B1L003S, U11-ch102, adc1

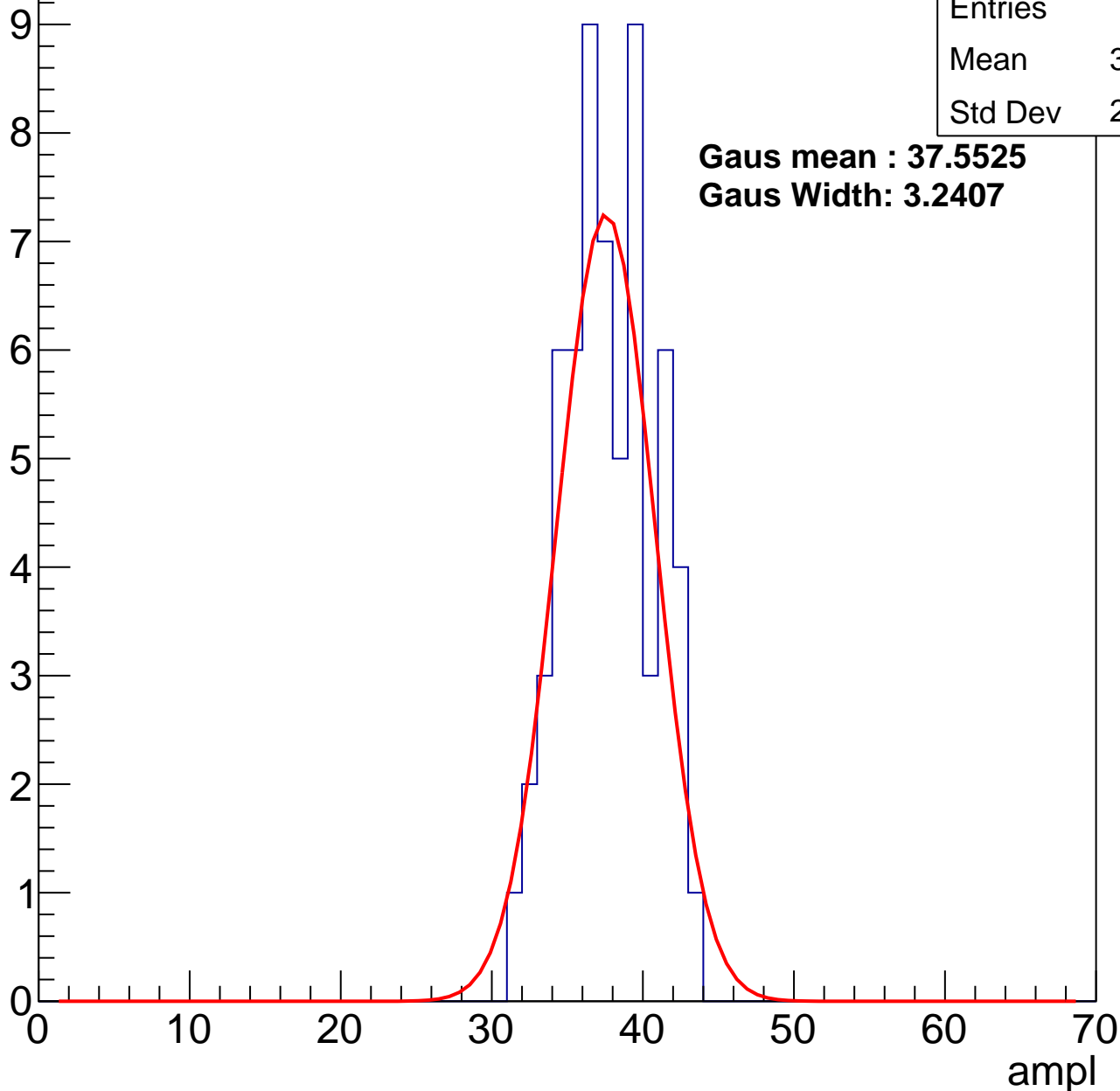
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	37.24
Std Dev	2.889

**Gaus mean : 37.5525**

**Gaus Width: 3.2407**



# B1L003S, U11-ch102, adc2

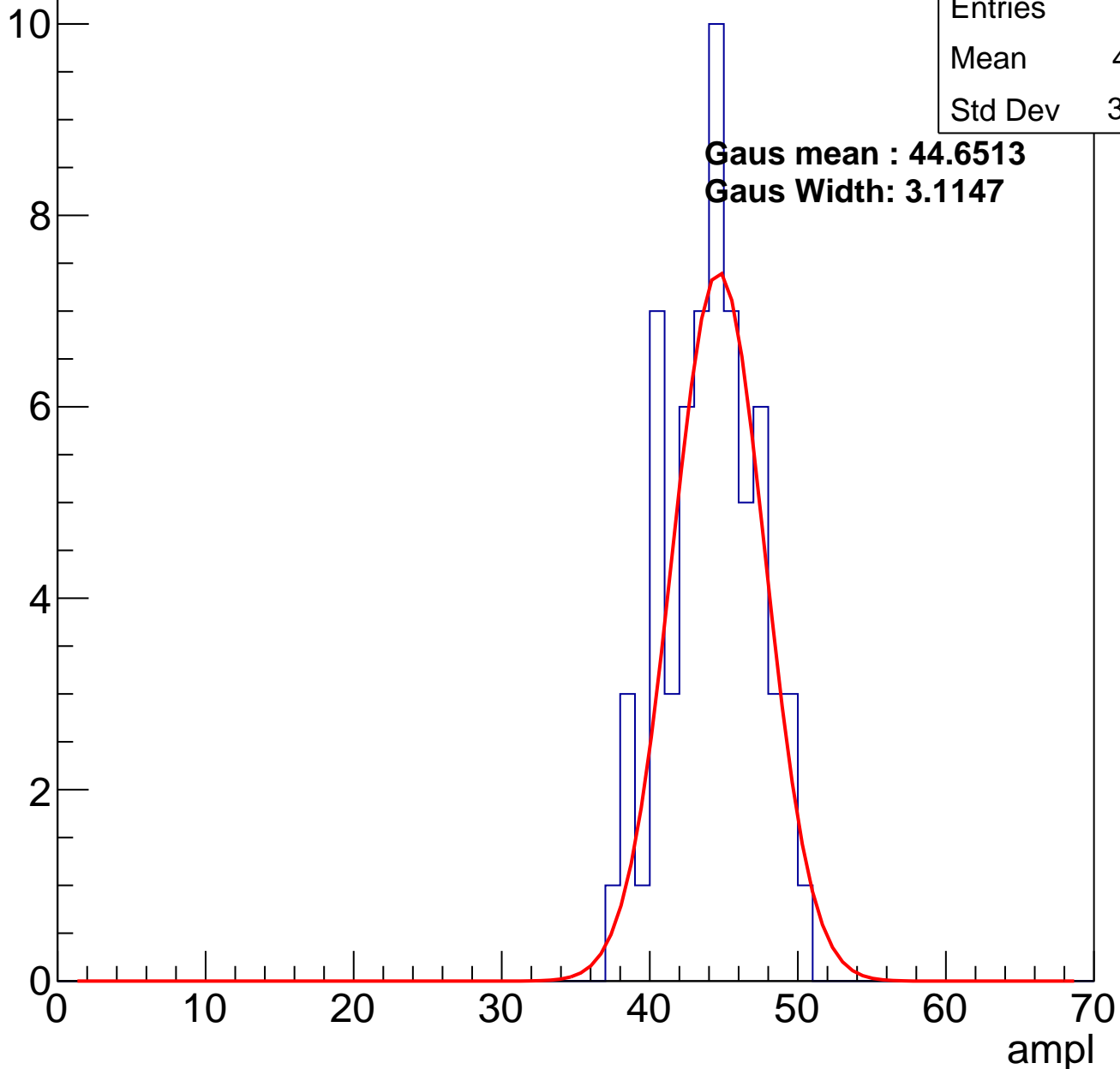
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	63
Mean	43.71
Std Dev	3.052

**Gaus mean : 44.6513**

**Gaus Width: 3.1147**

Entry

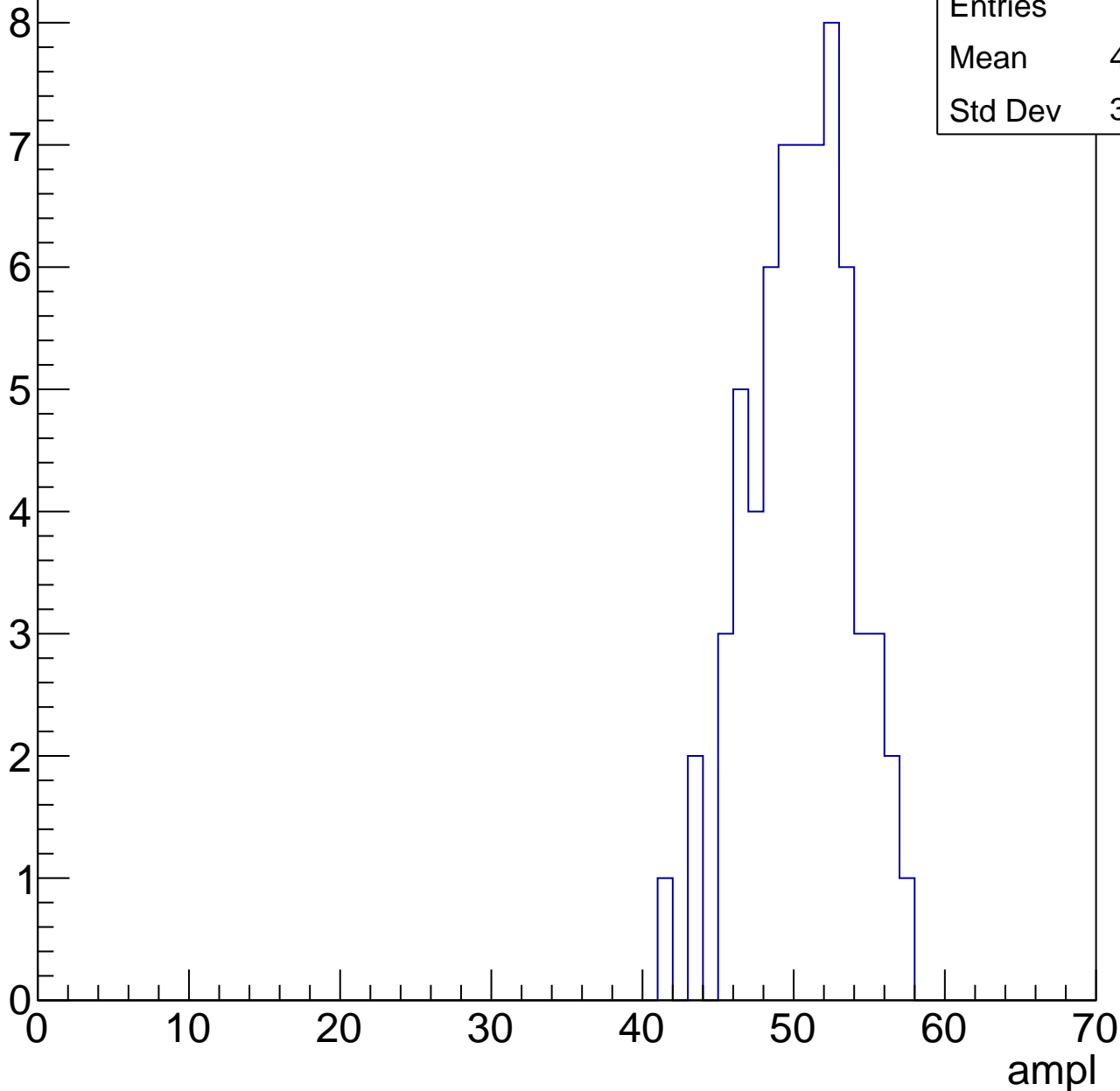


# B1L003S, U11-ch102, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	49.97
Std Dev	3.369

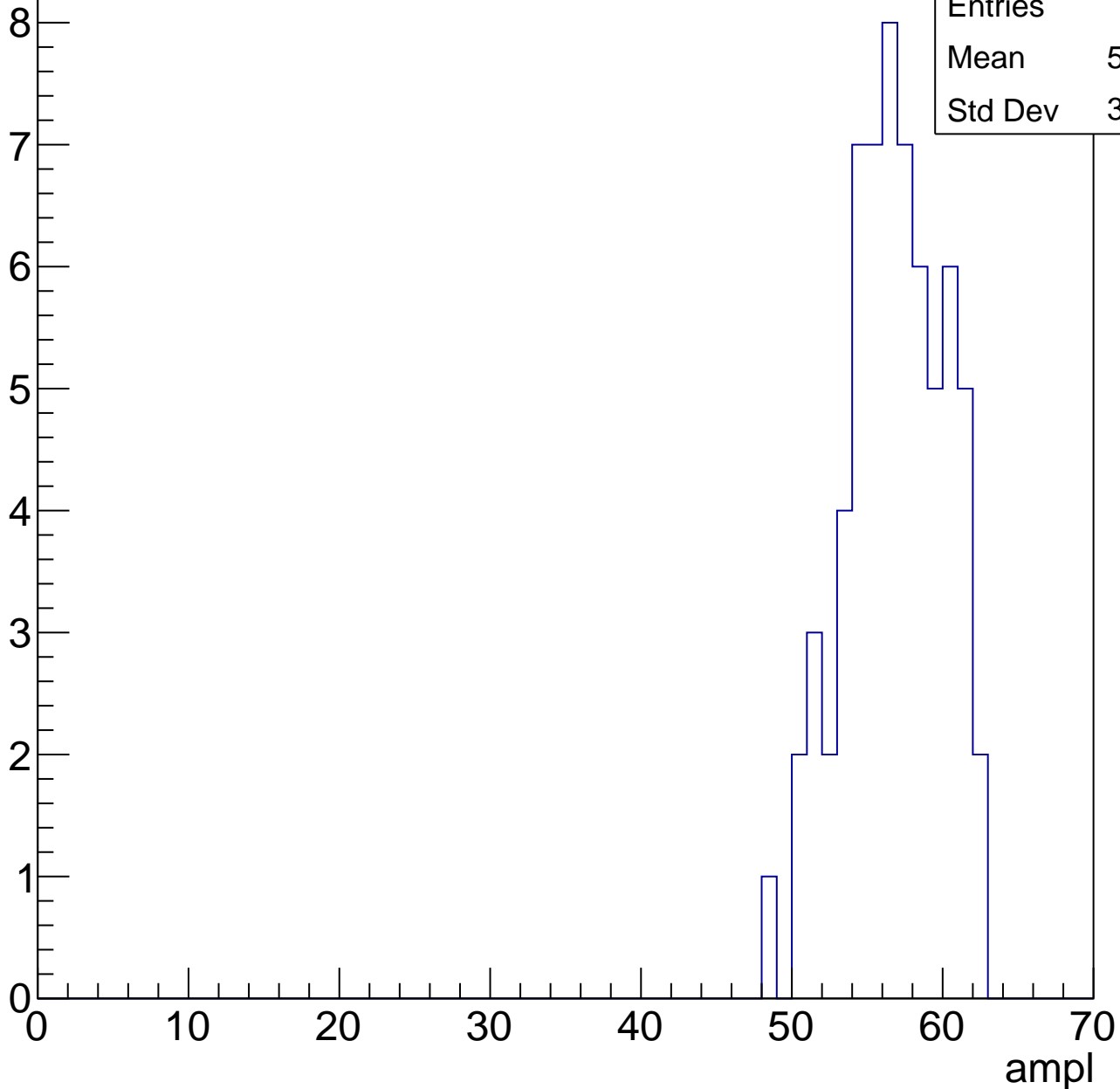


# B1L003S, U11-ch102, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	56.29
Std Dev	3.228

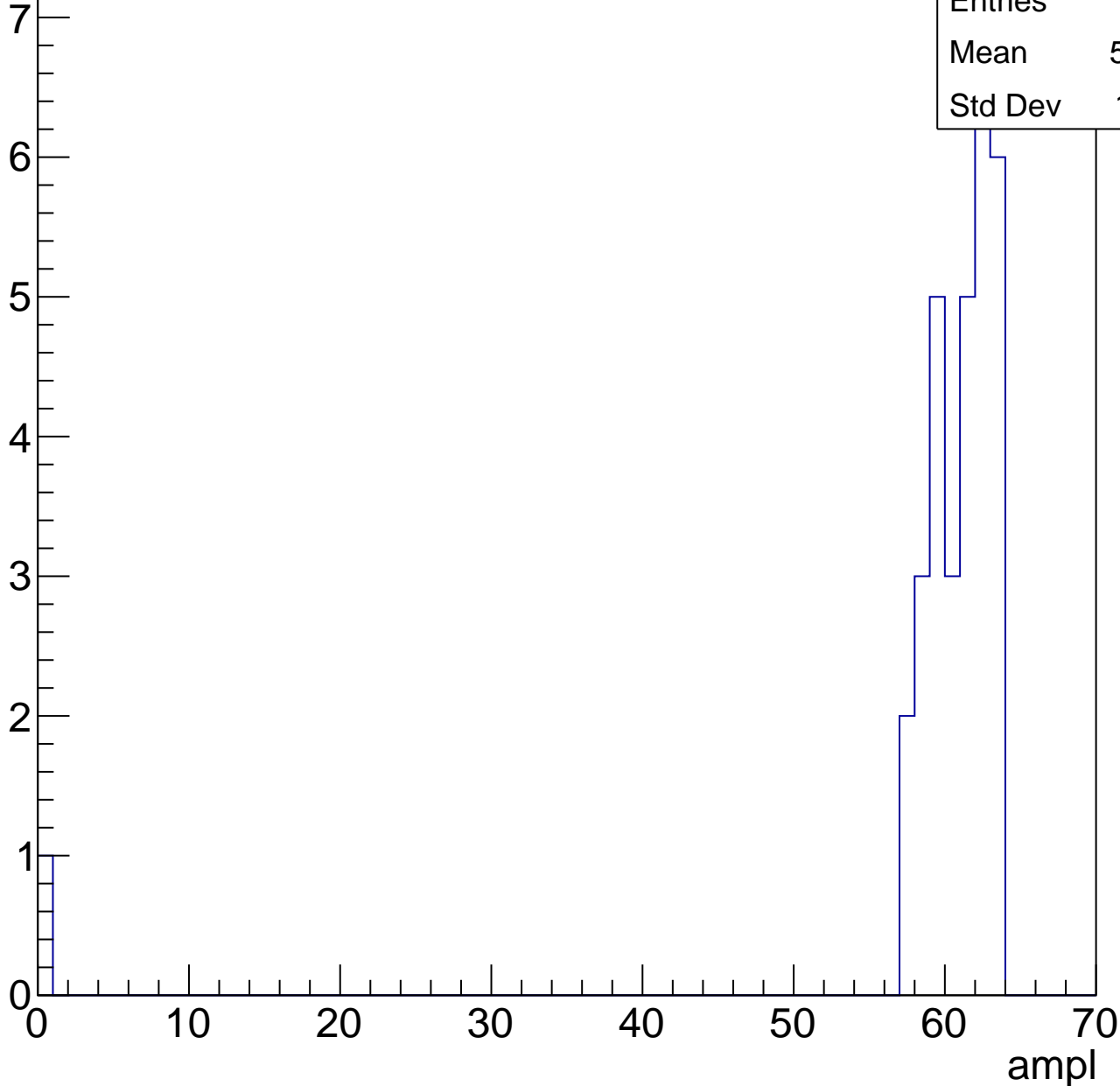


# B1L003S, U11-ch102, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

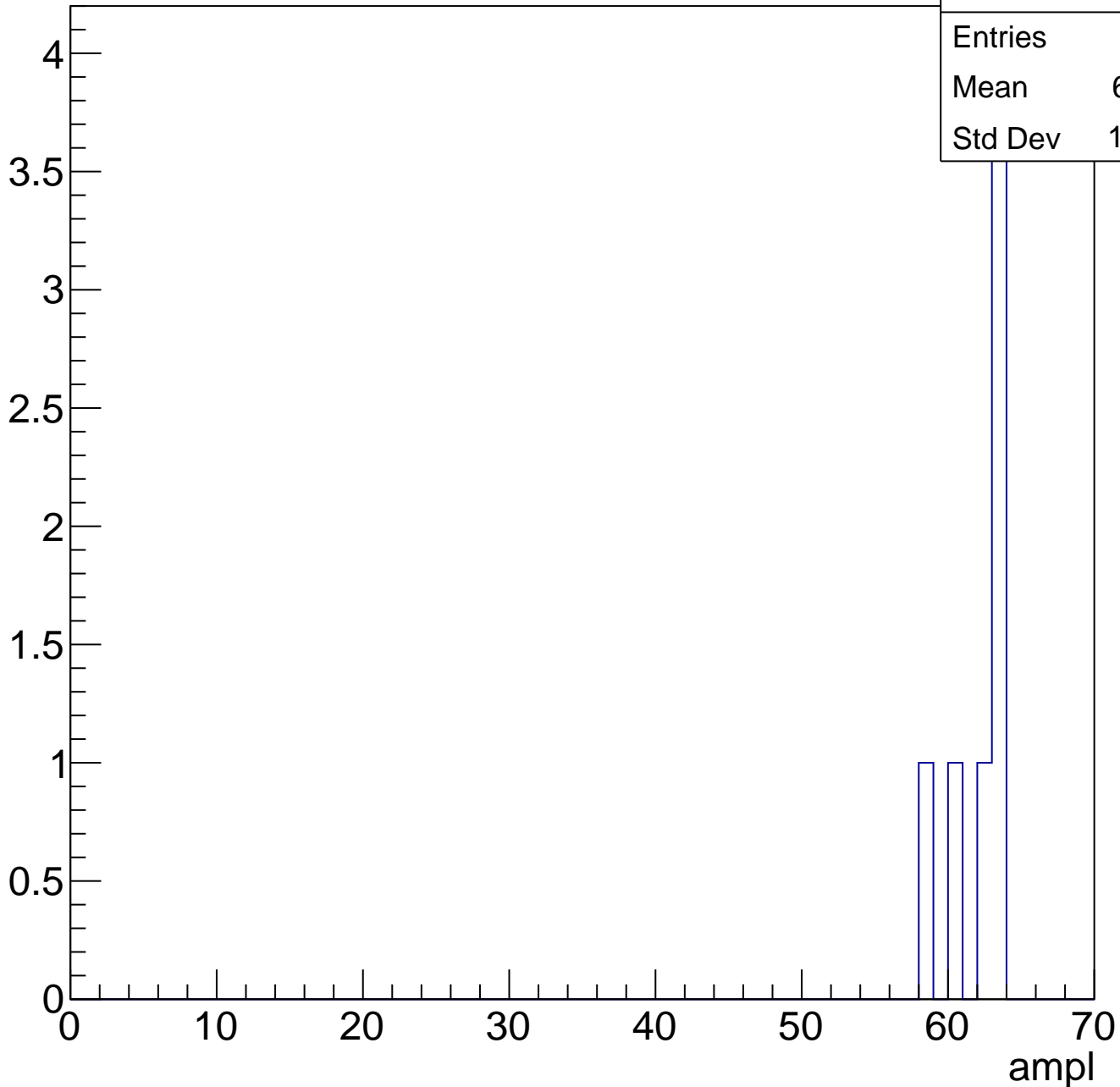
Entries	32
Mean	58.75
Std Dev	10.71



# B1L003S, U11-ch102, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



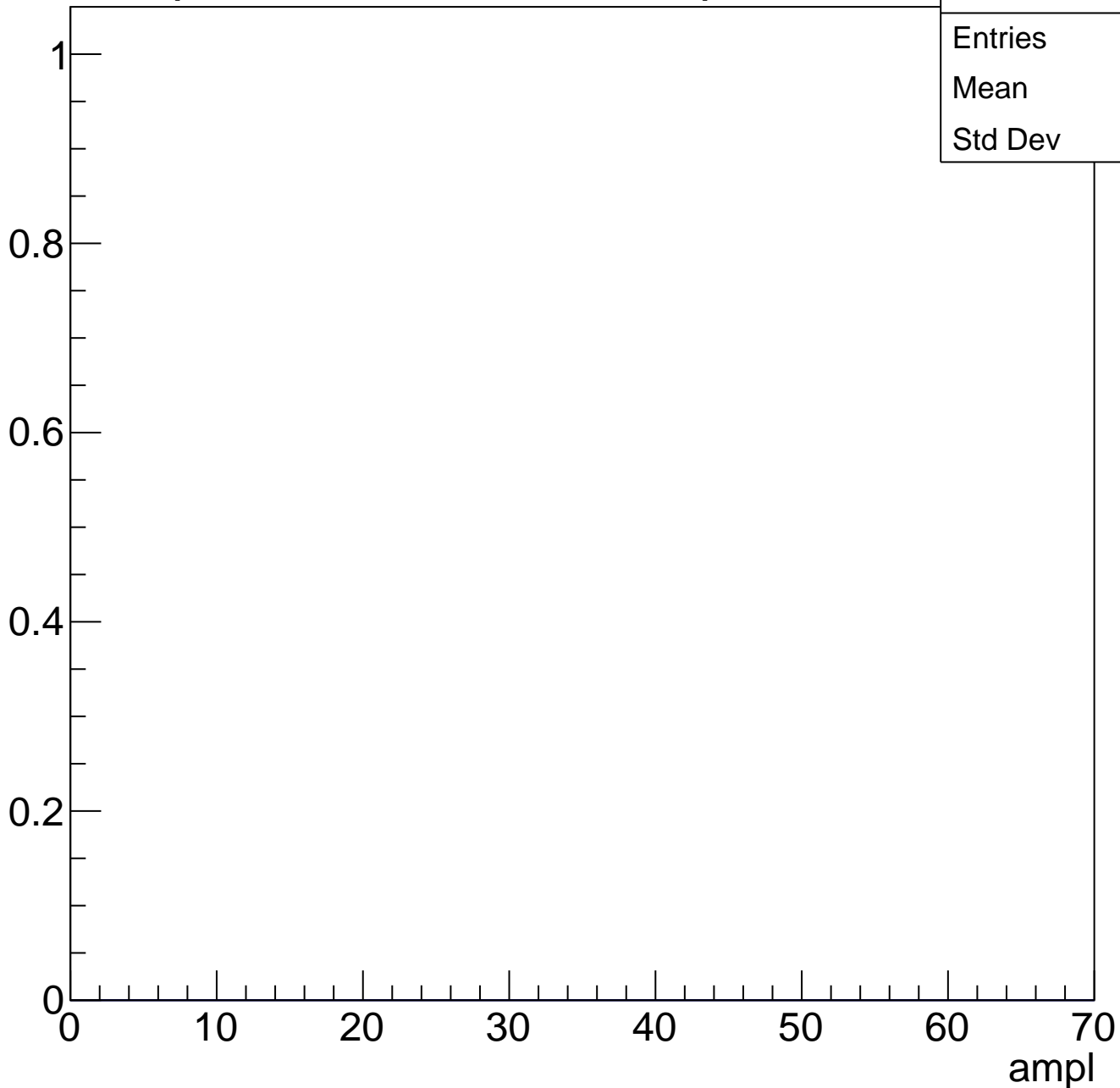
Entries	7
Mean	61.71
Std Dev	1.829



# B1L003S, U11-ch102, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U11-ch103, adc0

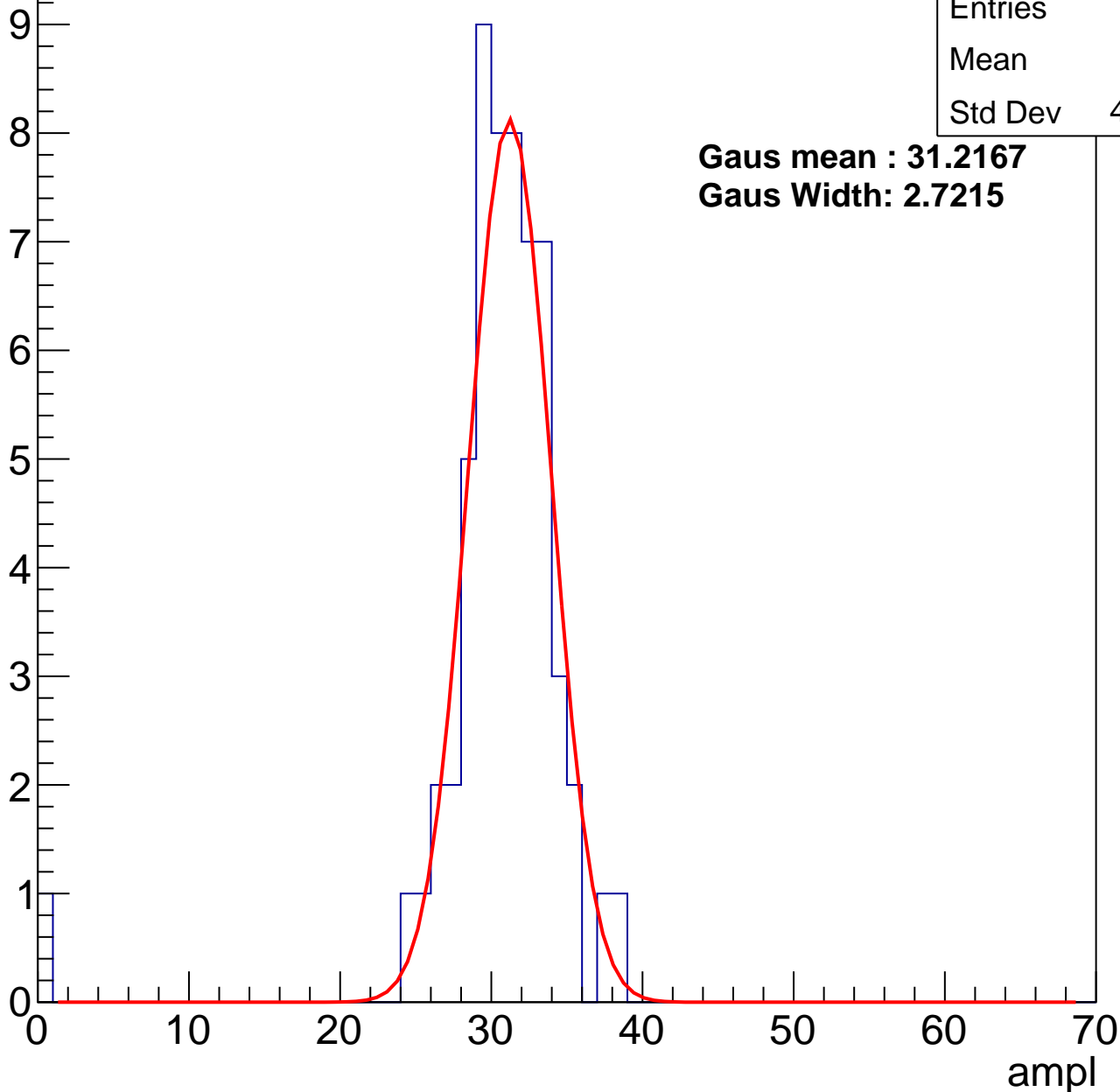
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	30.1
Std Dev	4.823

**Gaus mean : 31.2167**

**Gaus Width: 2.7215**



# B1L003S, U11-ch103, adc1

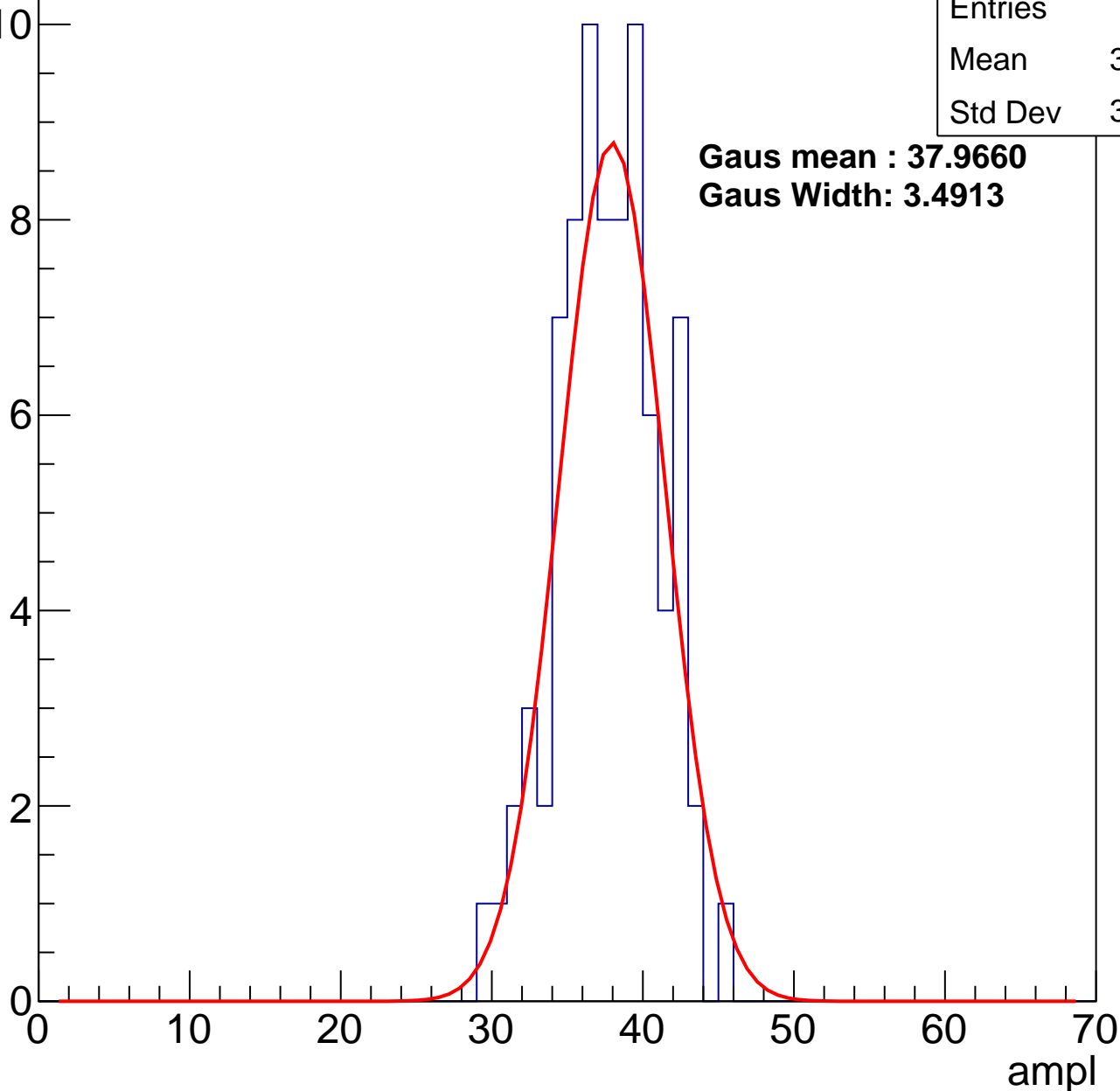
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	80
Mean	37.25
Std Dev	3.296

**Gaus mean : 37.9660**

**Gaus Width: 3.4913**



# B1L003S, U11-ch103, adc2

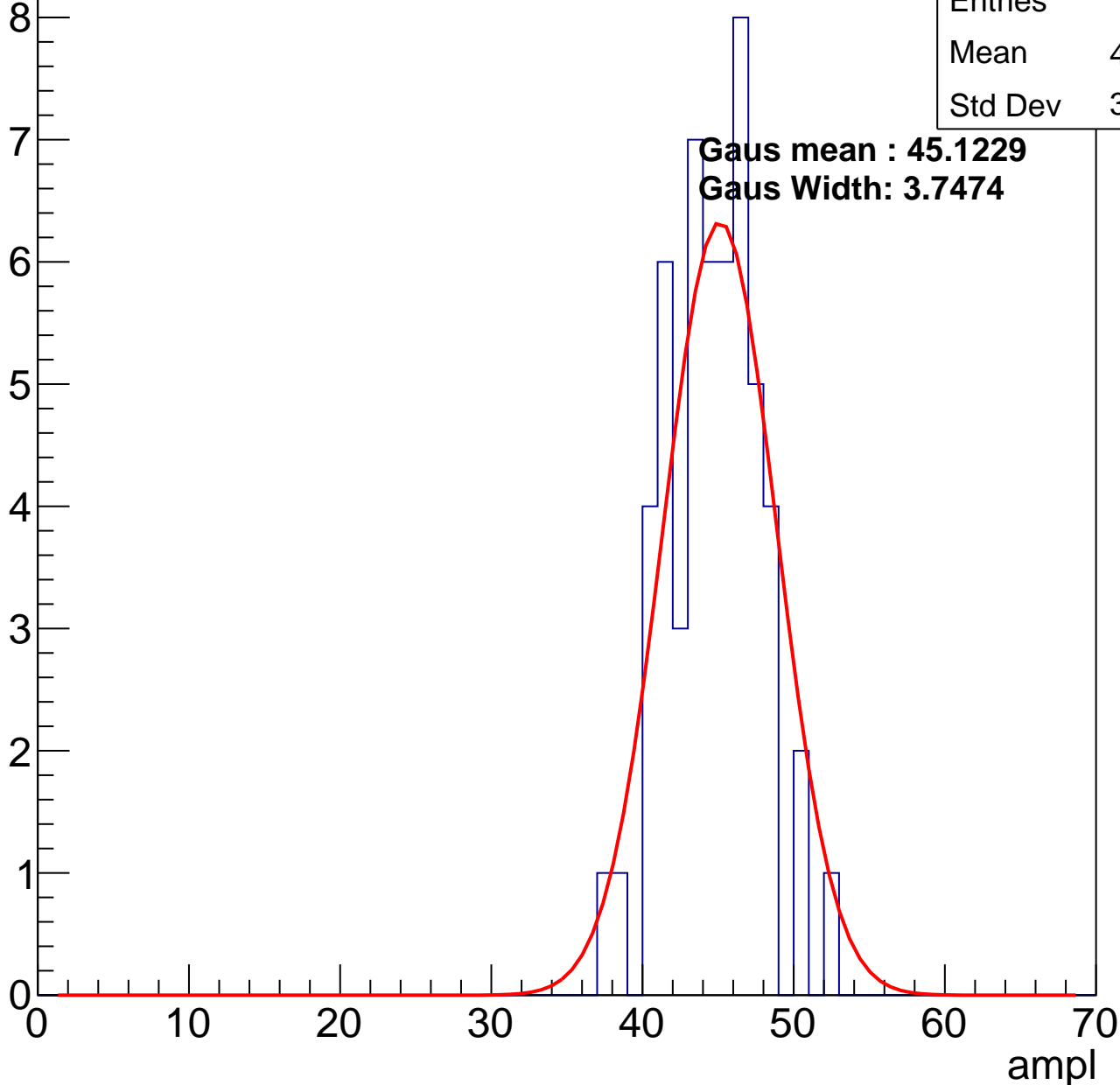
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	54
Mean	44.24
Std Dev	3.049

**Gaus mean : 45.1229**

**Gaus Width: 3.7474**

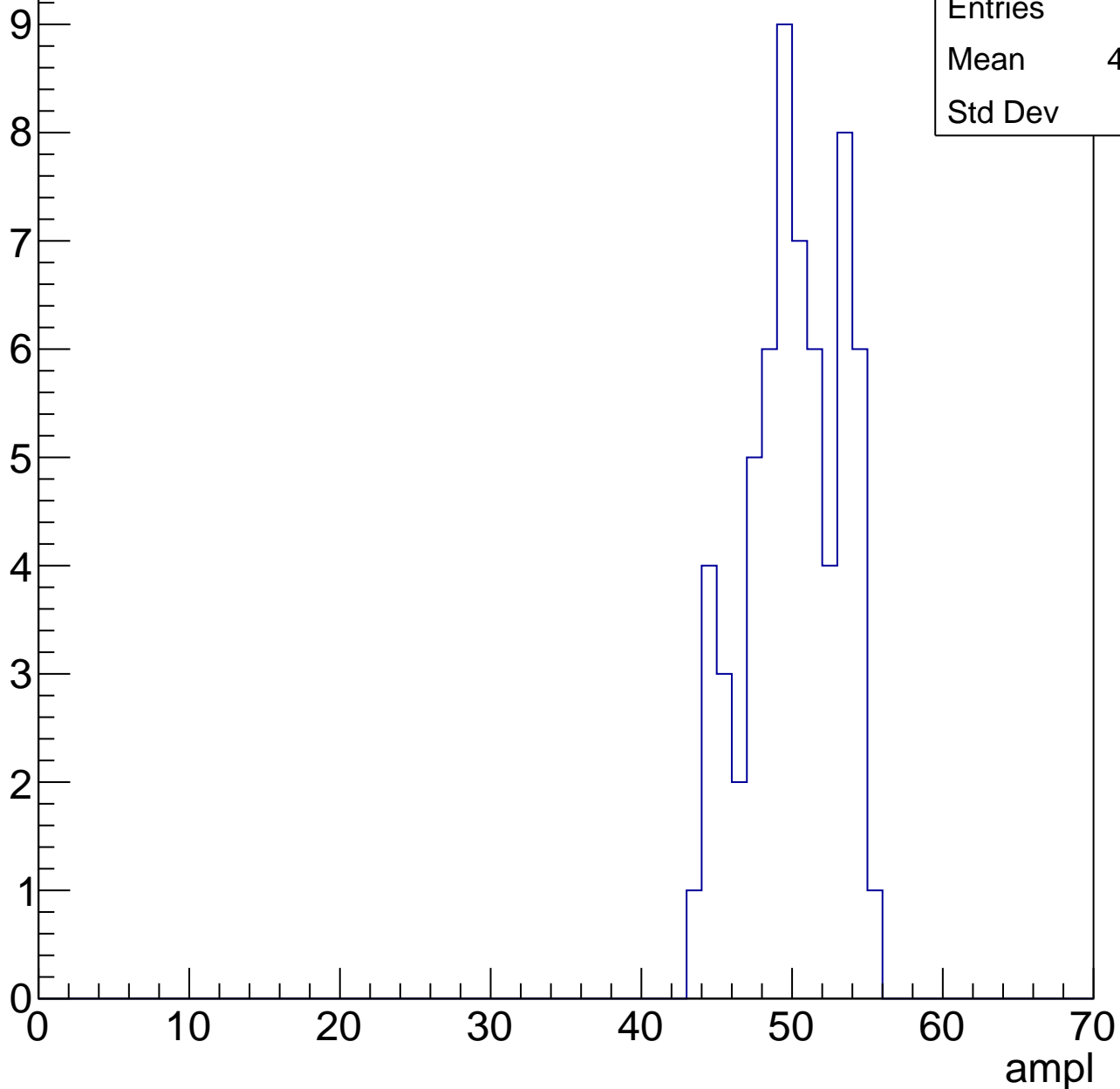


# B1L003S, U11-ch103, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	49.63
Std Dev	3.07

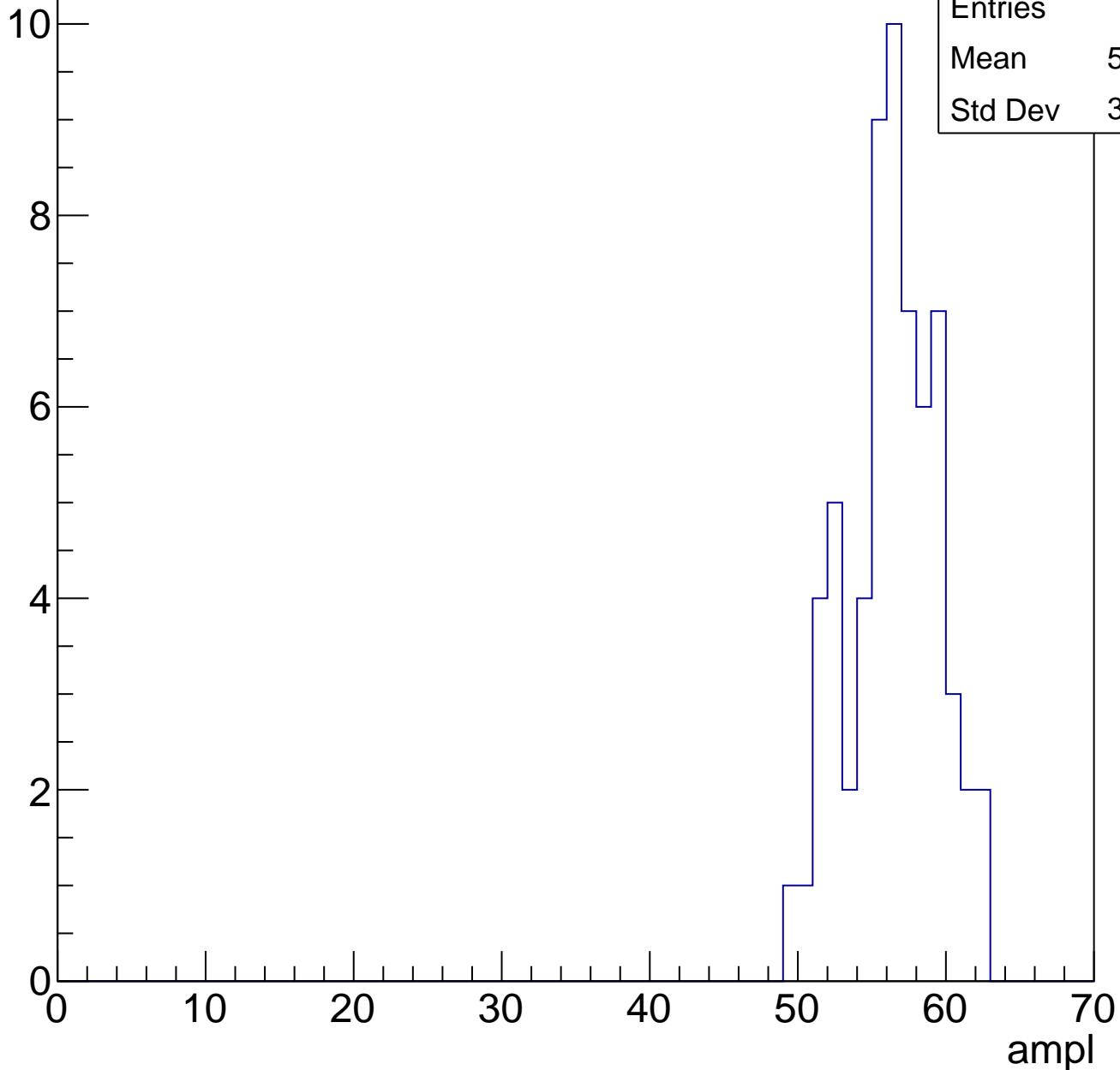


# B1L003S, U11-ch103, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	63
Mean	55.97
Std Dev	3.013

Entry

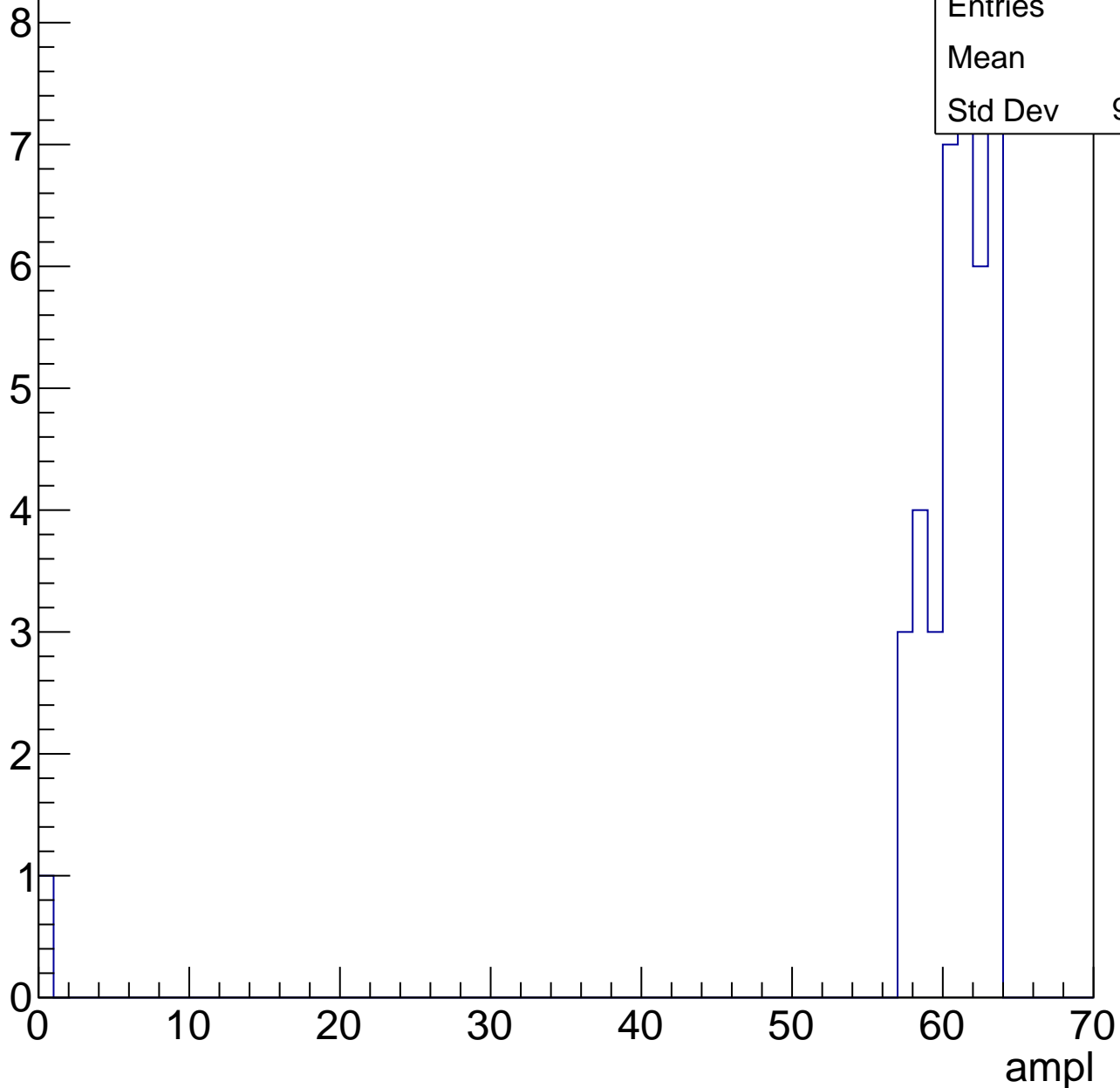


# B1L003S, U11-ch103, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	40
Mean	59.1
Std Dev	9.641



# B1L003S, U11-ch103, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch103, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	23
Std Dev	0

# B1L003S, U11-ch104, adc0

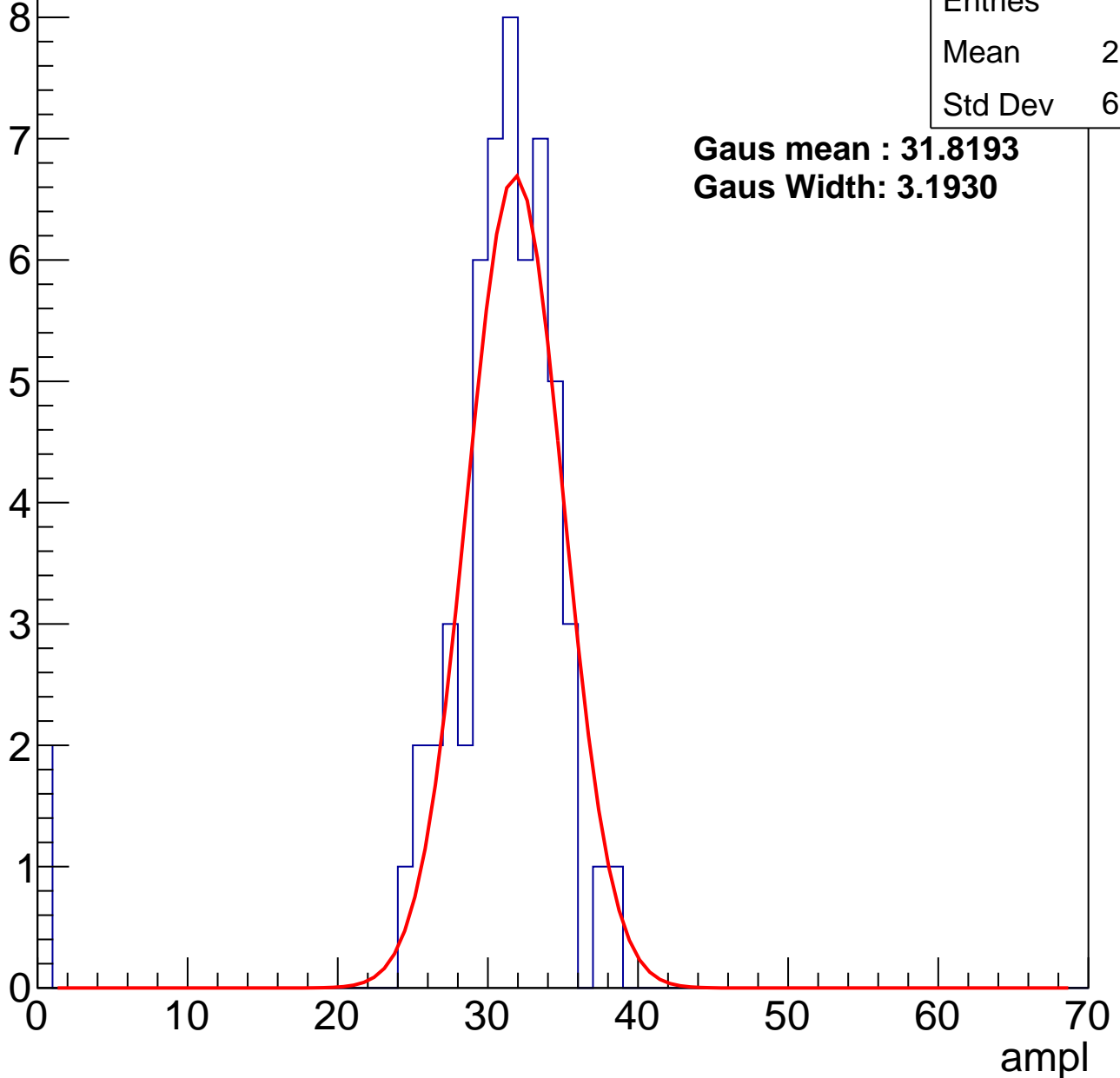
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	29.79
Std Dev	6.436

**Gaus mean : 31.8193**

**Gaus Width: 3.1930**



# B1L003S, U11-ch104, adc1

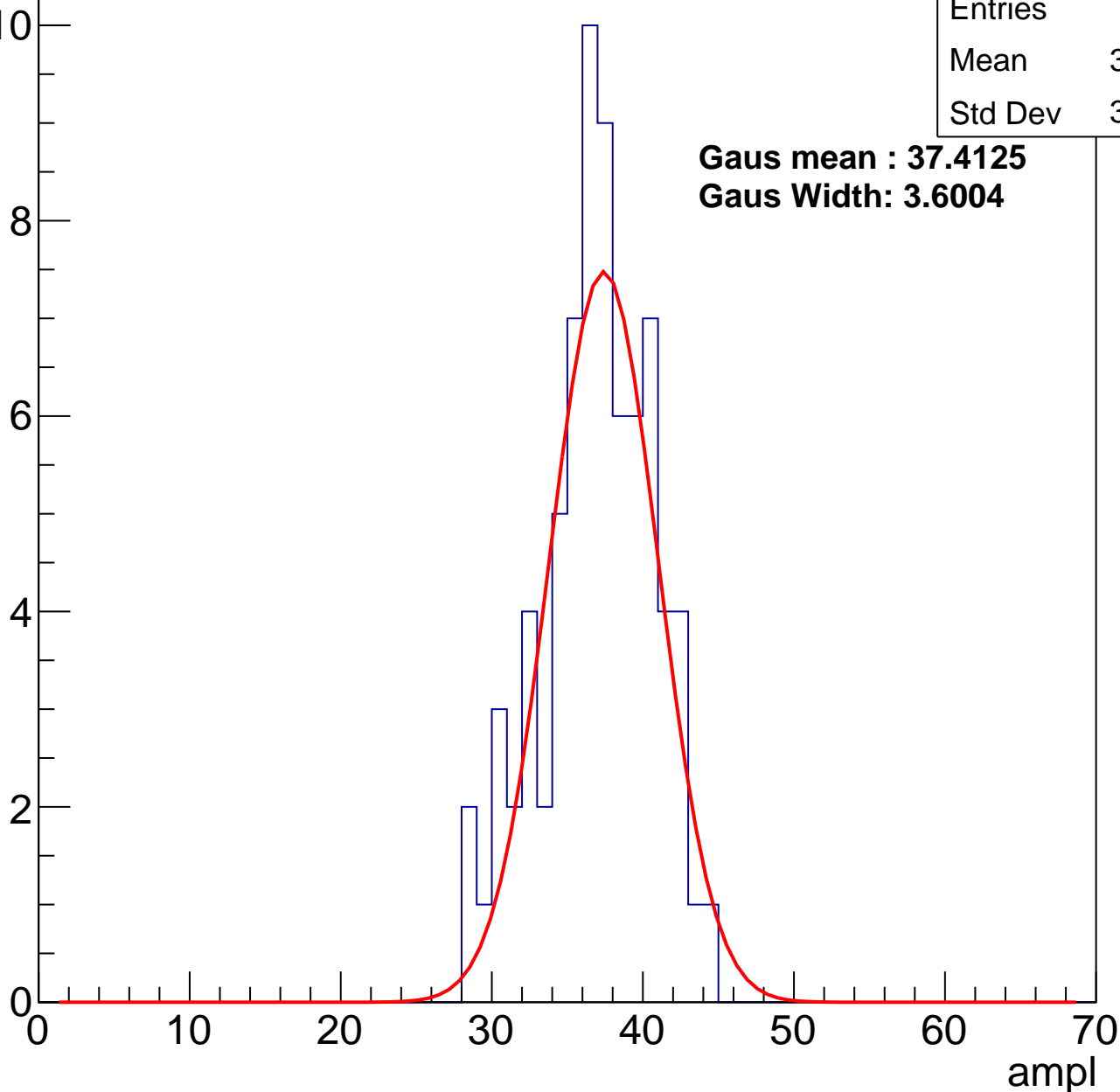
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	74
Mean	36.49
Std Dev	3.644

**Gaus mean : 37.4125**

**Gaus Width: 3.6004**



# B1L003S, U11-ch104, adc2

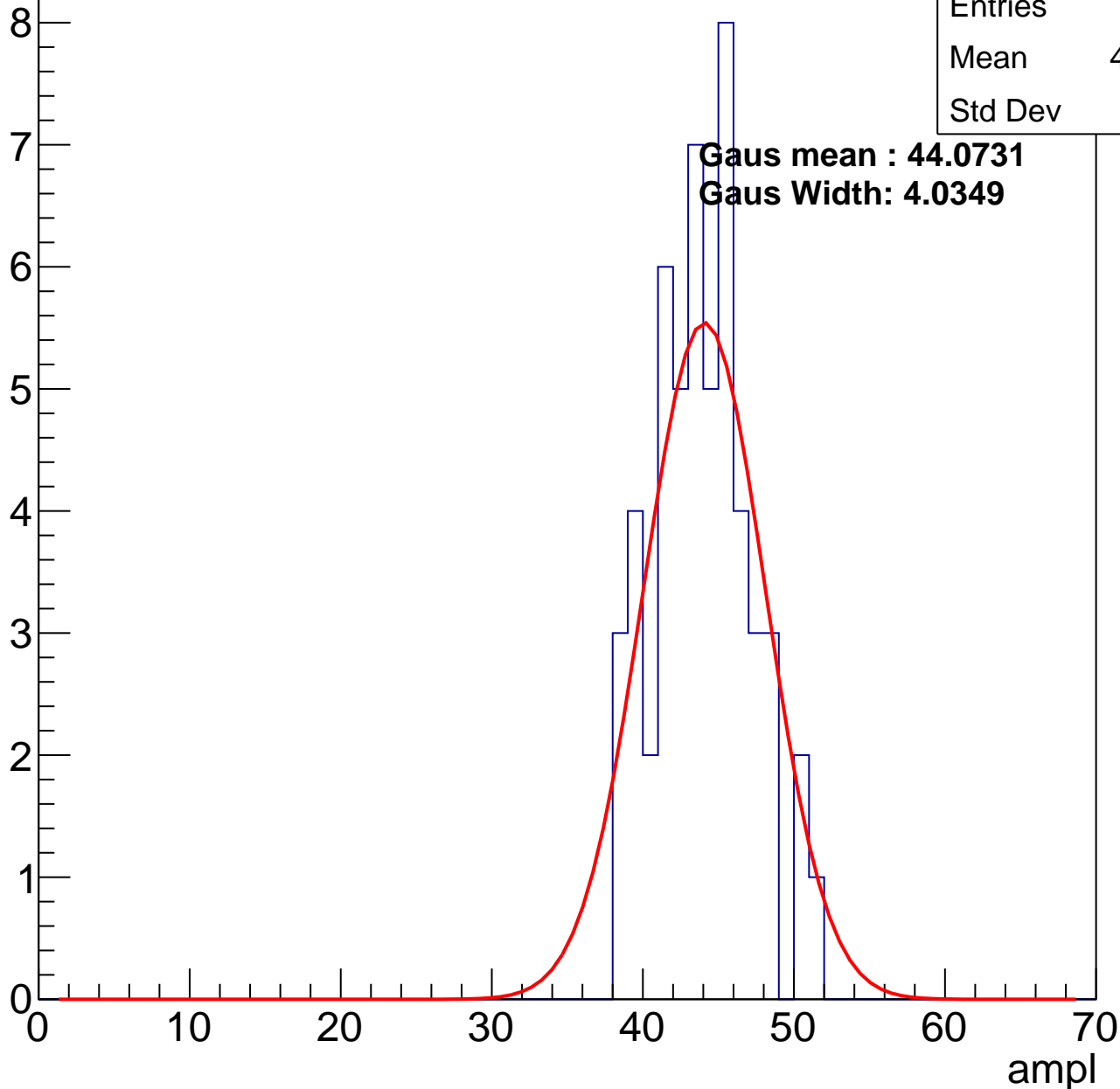
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	43.53
Std Dev	3.16

**Gaus mean : 44.0731**

**Gaus Width: 4.0349**

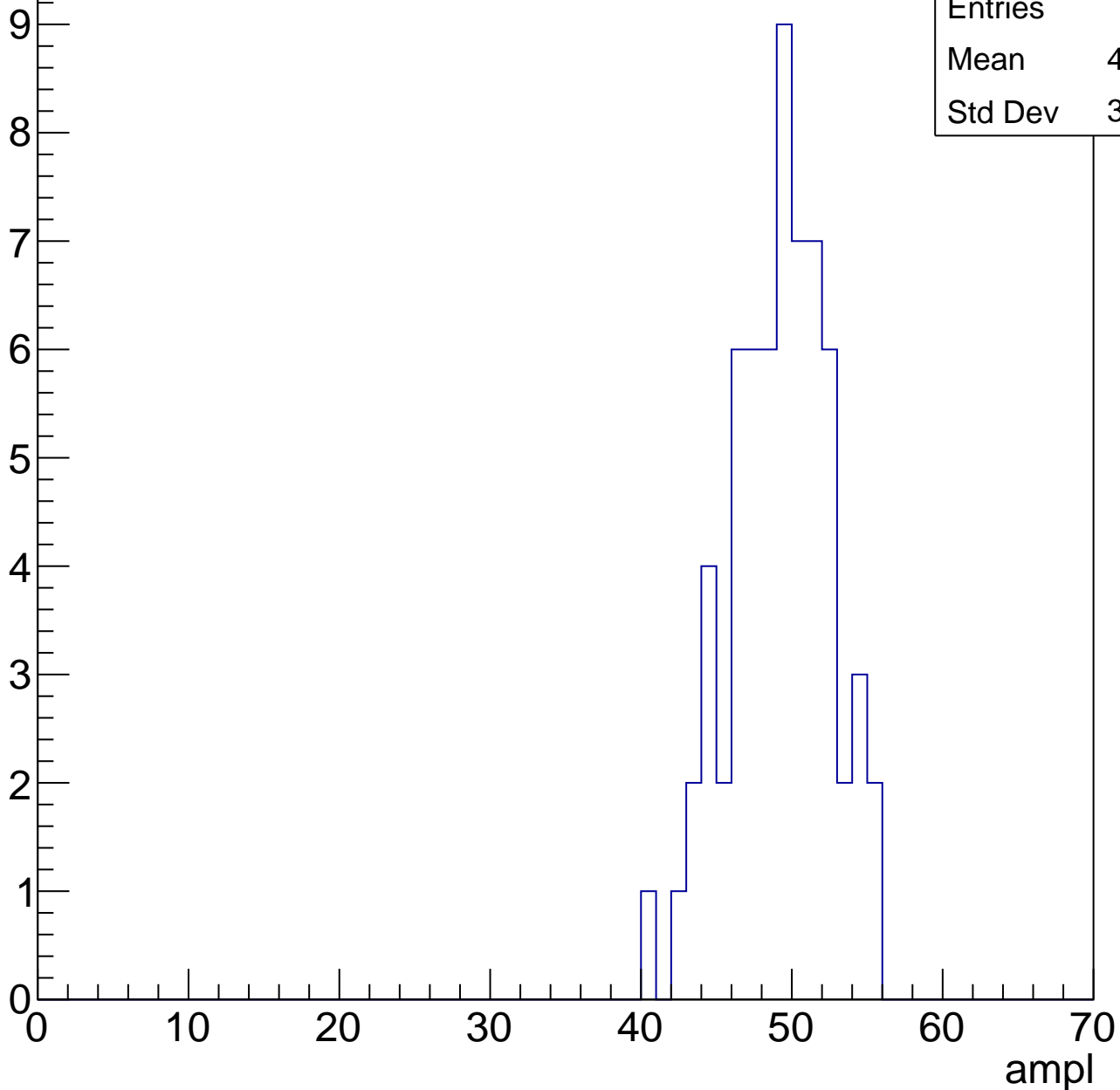


# B1L003S, U11-ch104, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	48.72
Std Dev	3.262

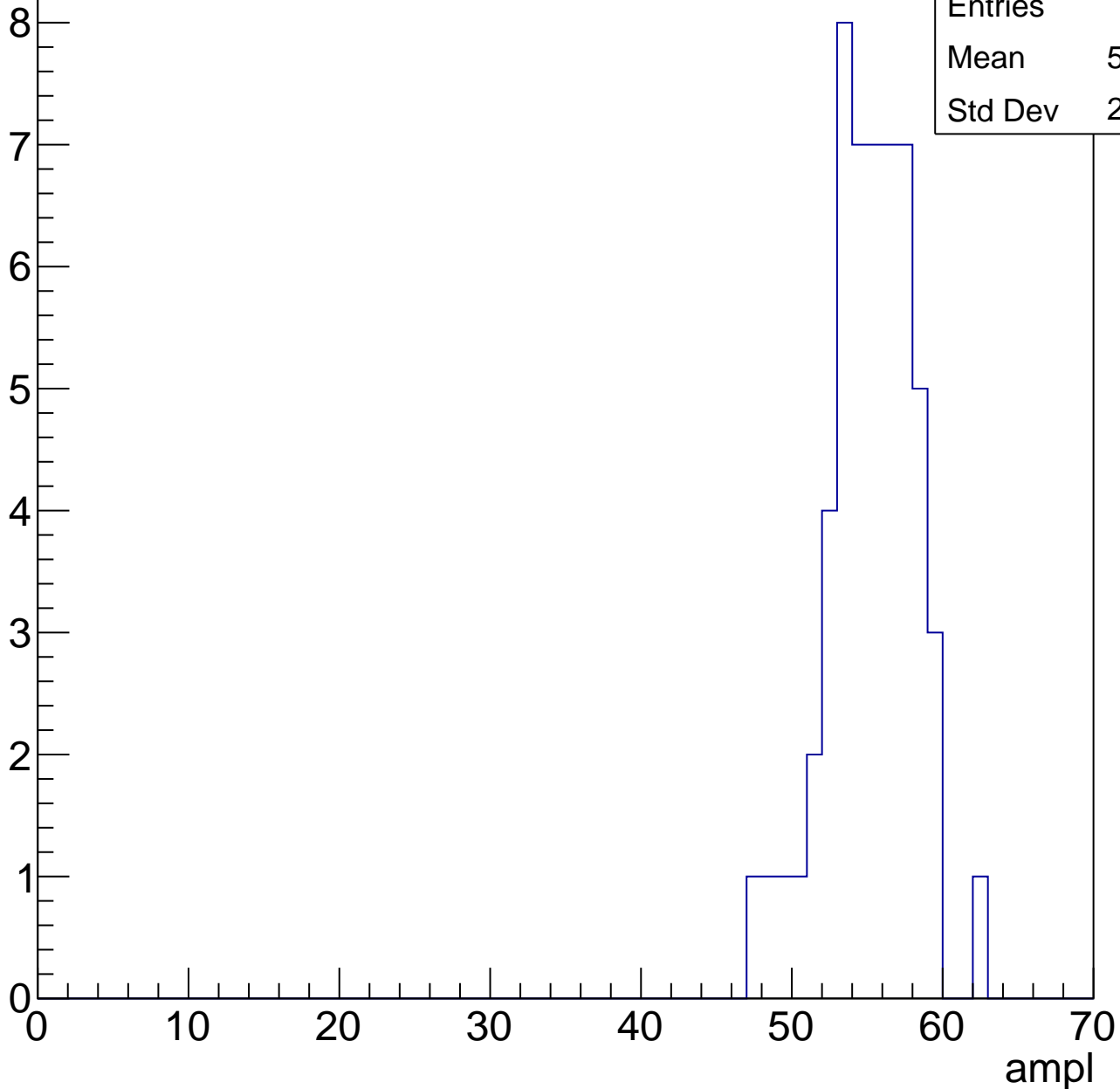


# B1L003S, U11-ch104, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	54.75
Std Dev	2.874

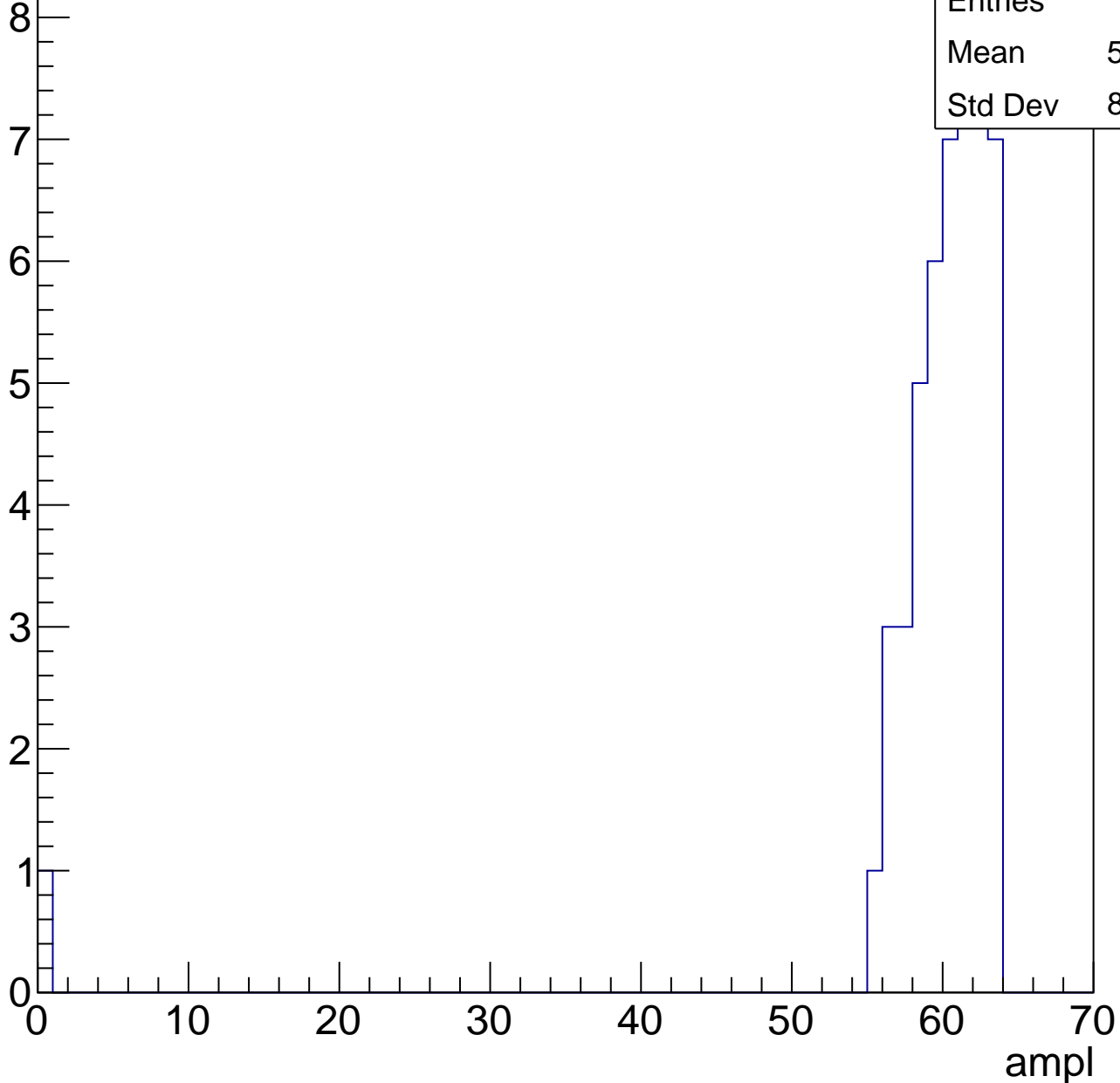


# B1L003S, U11-ch104, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	49
Mean	58.84
Std Dev	8.763



# B1L003S, U11-ch104, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries

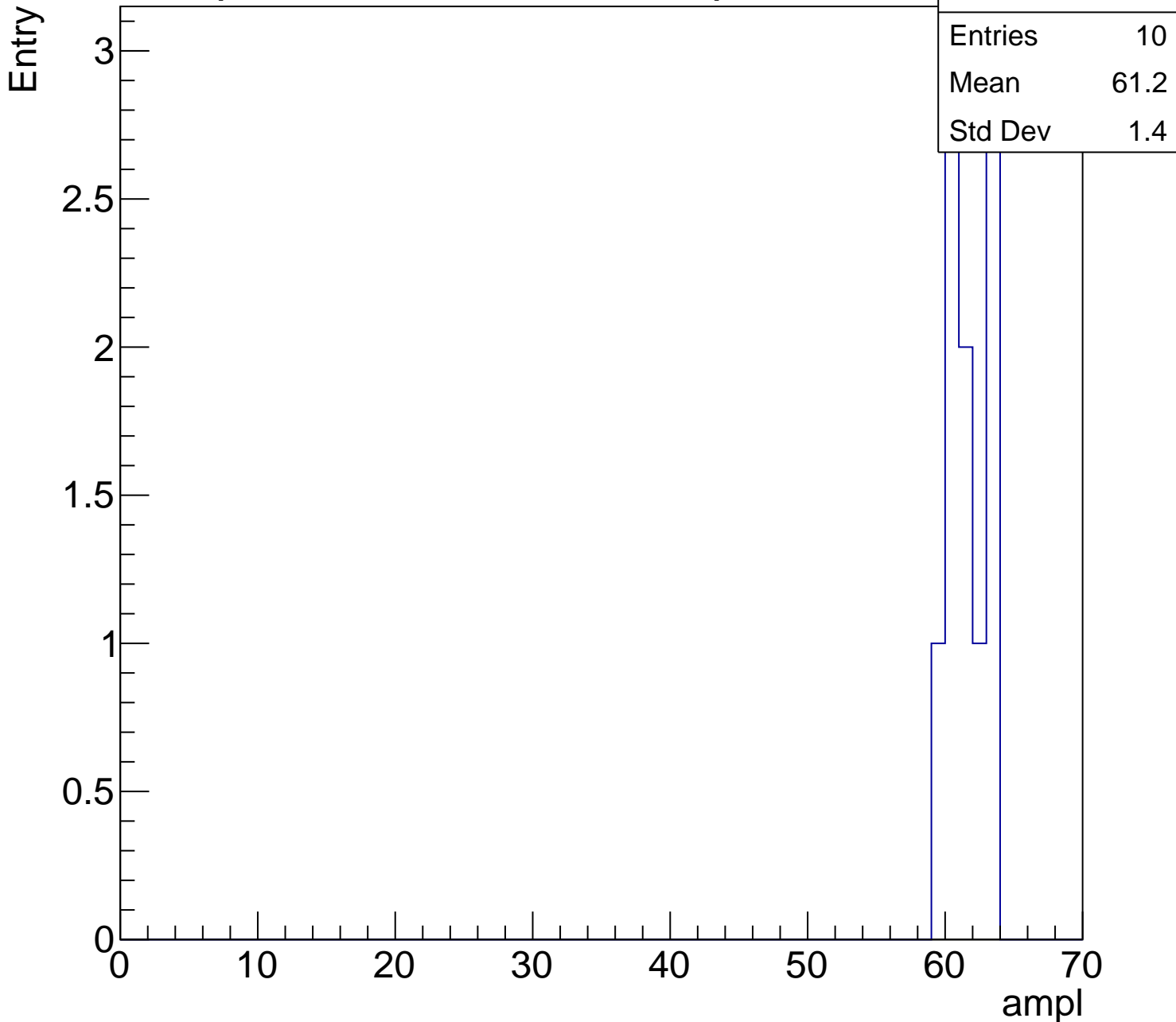
10

Mean

61.2

Std Dev

1.4





# B1L003S, U11-ch104, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	23
Std Dev	0

ampl

# B1L003S, U11-ch105, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	78
Mean	31.77
Std Dev	3.351

**Gaus mean : 32.0553**

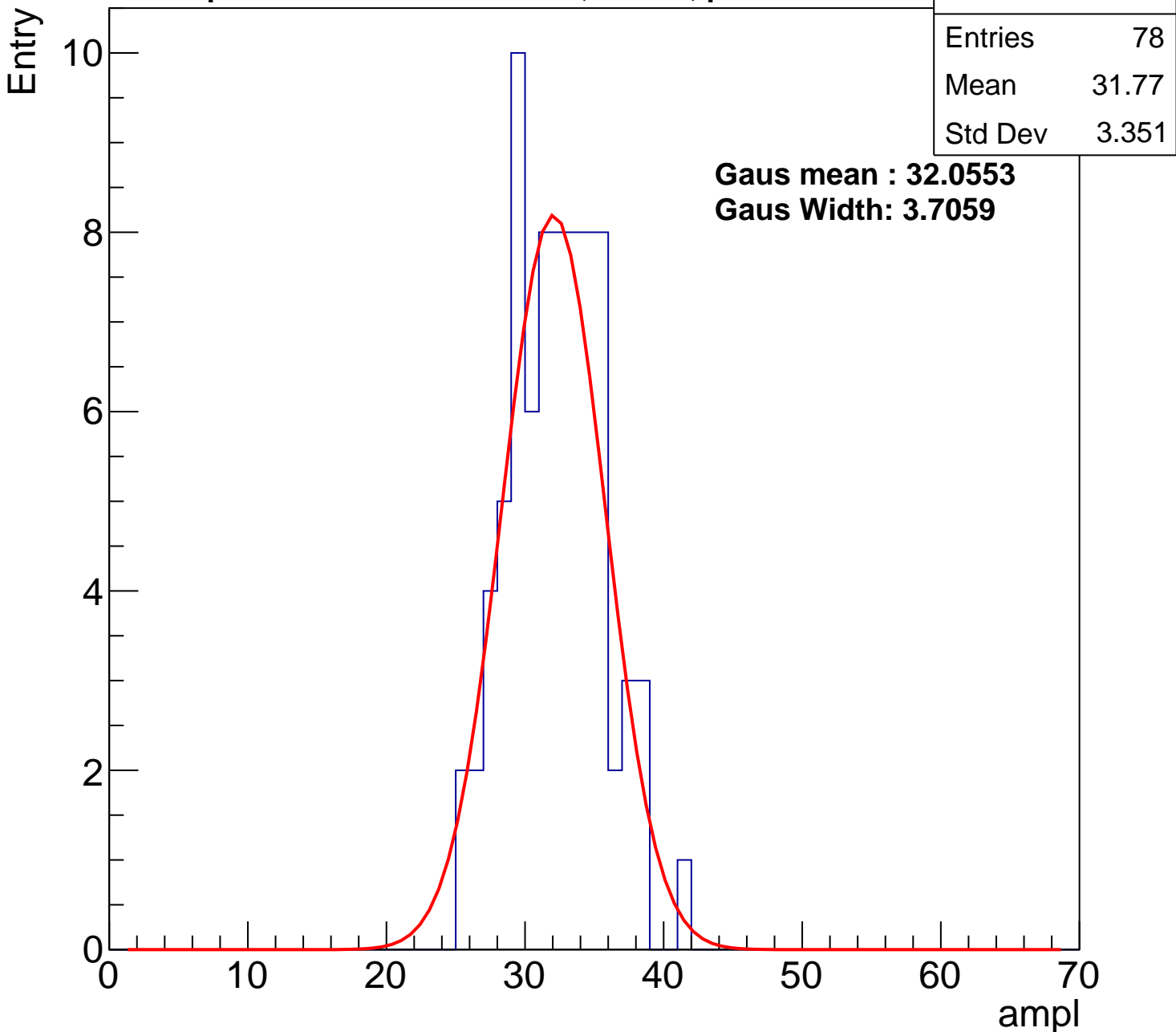
**Gaus Width: 3.7059**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U11-ch105, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	70
Mean	38.64
Std Dev	3.439

**Gaus mean : 39.3258**

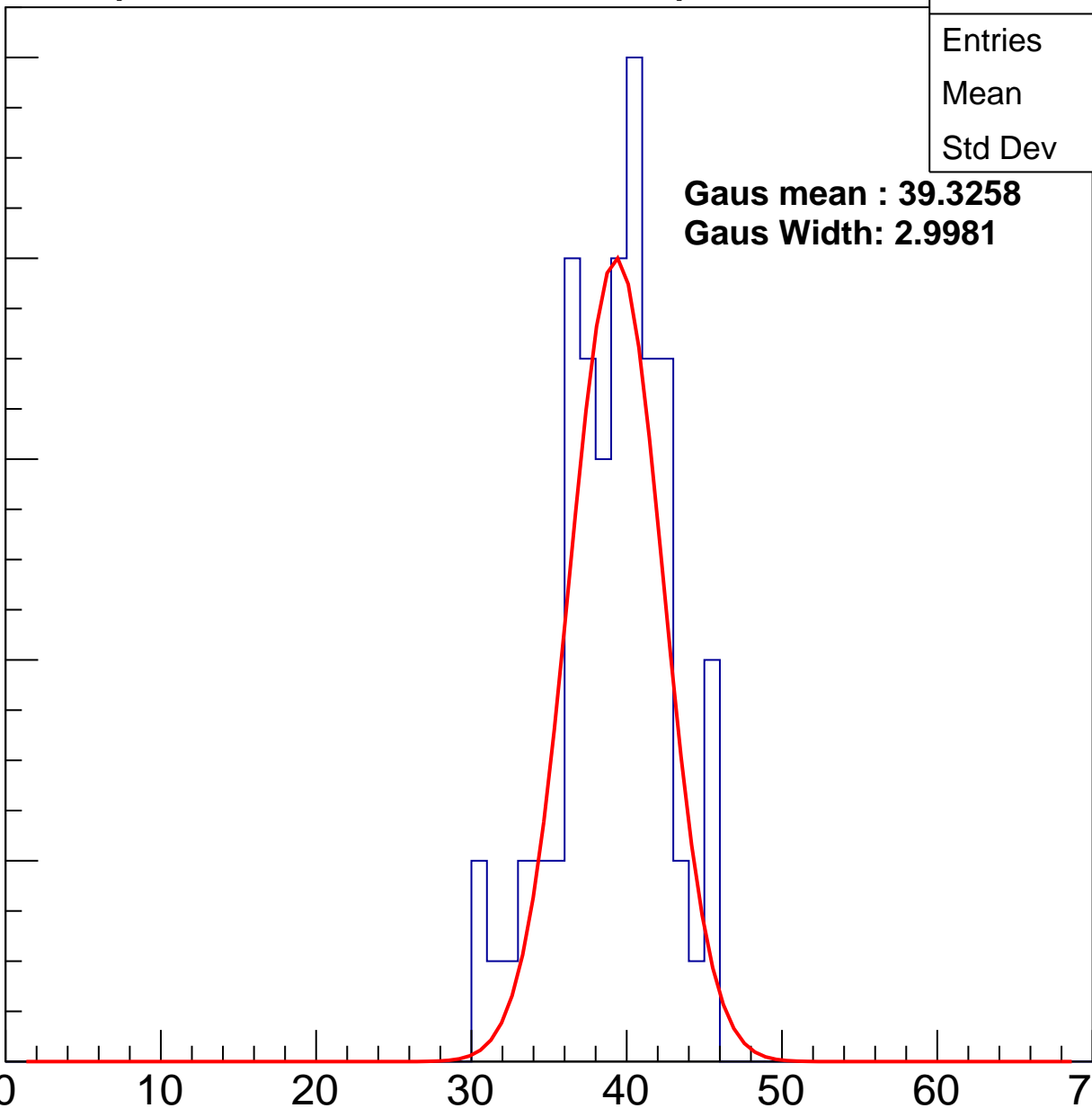
**Gaus Width: 2.9981**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L003S, U11-ch105, adc2

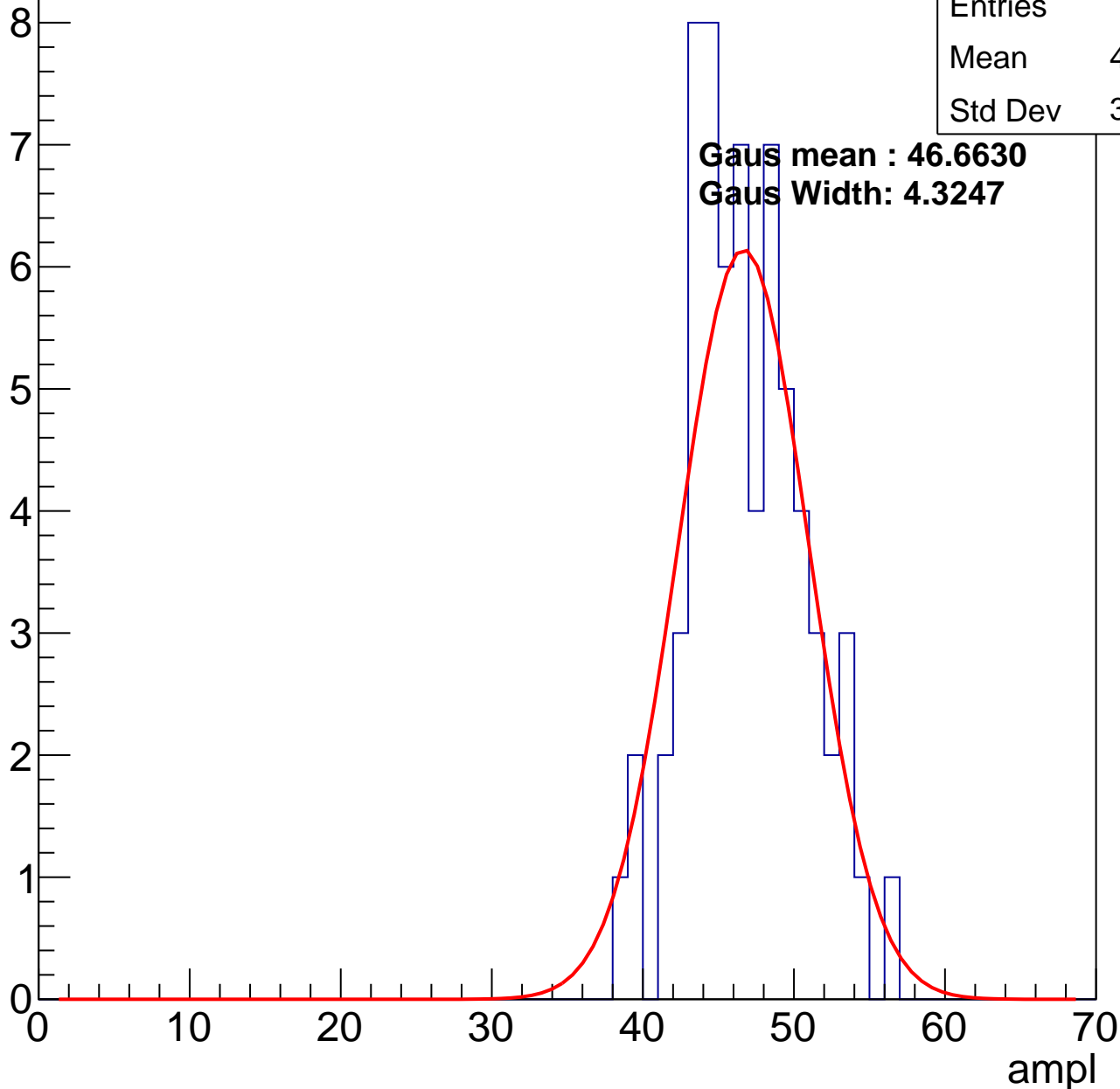
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	46.37
Std Dev	3.785

**Gaus mean : 46.6630**

**Gaus Width: 4.3247**

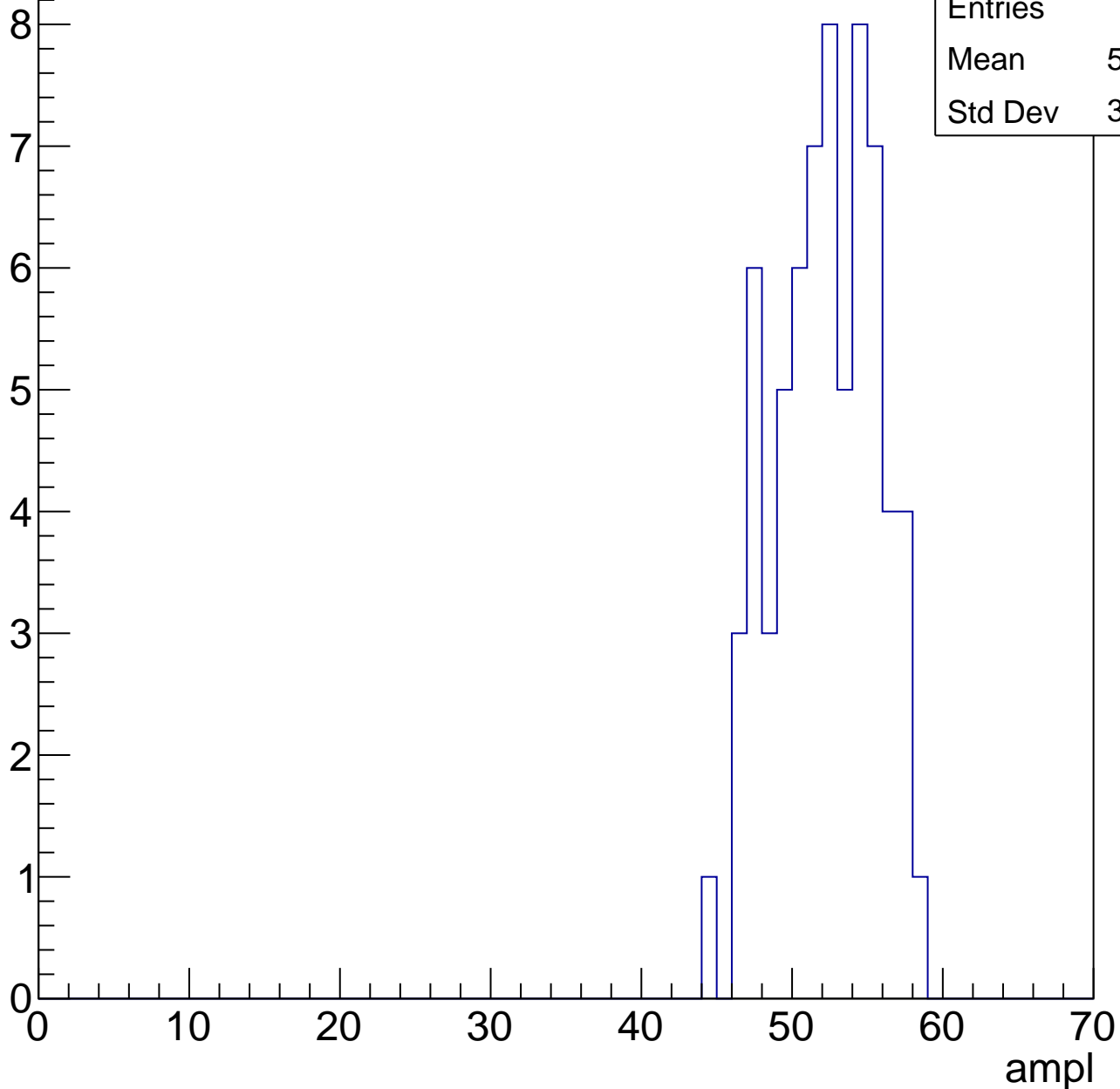


# B1L003S, U11-ch105, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	51.74
Std Dev	3.302

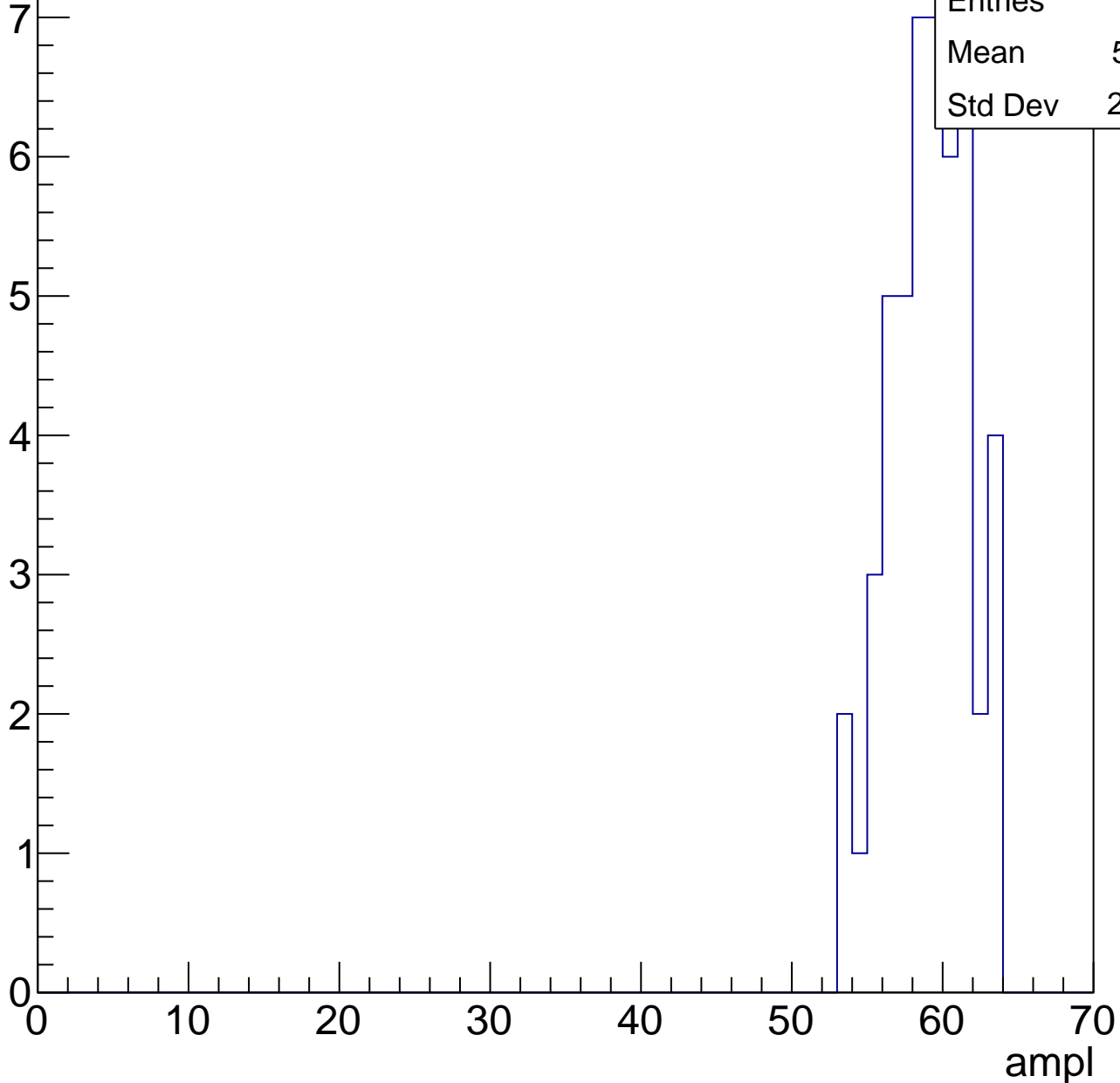


# B1L003S, U11-ch105, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	49
Mean	58.61
Std Dev	2.578

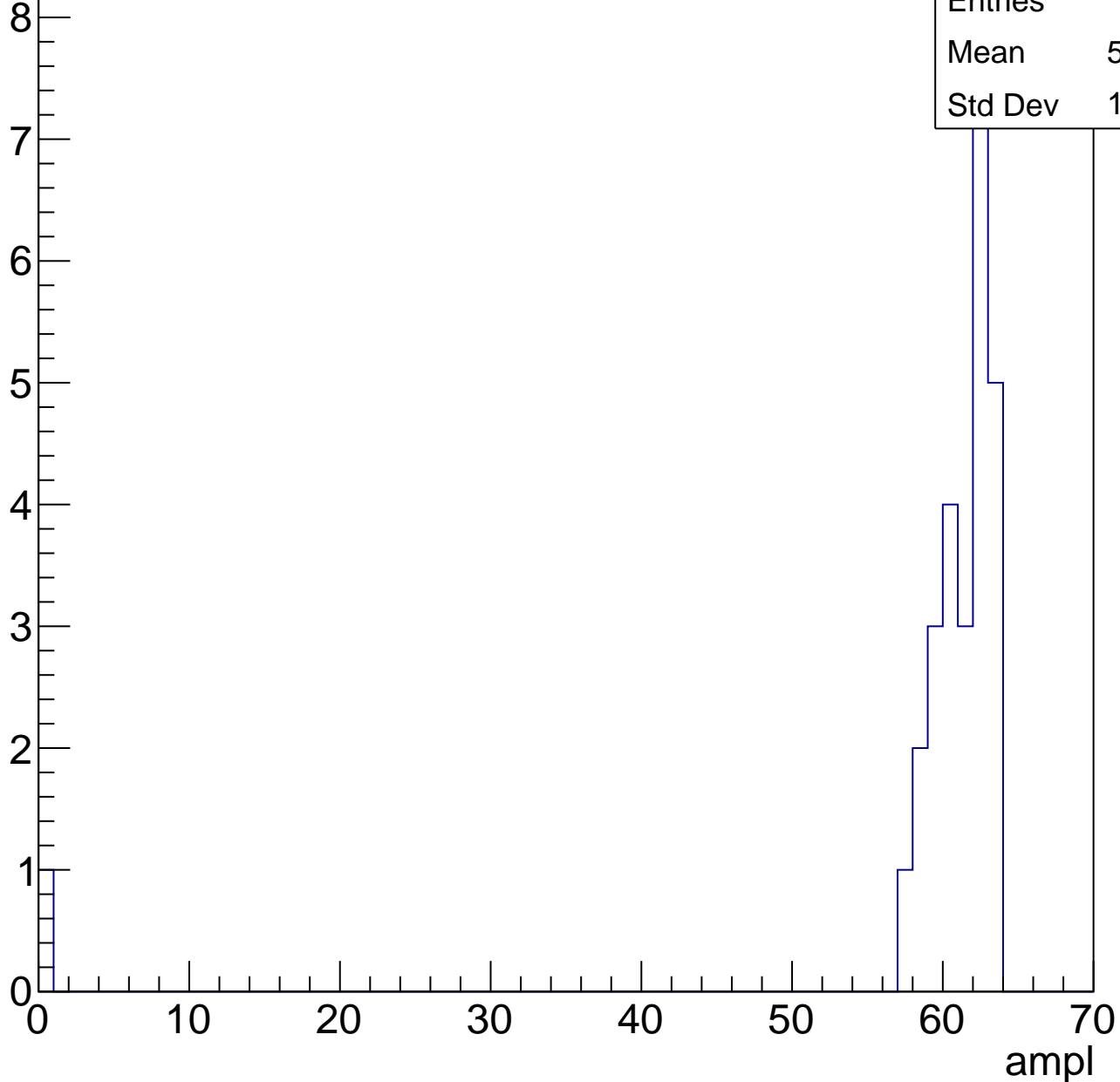


# B1L003S, U11-ch105, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	27
Mean	58.67
Std Dev	11.63



# B1L003S, U11-ch105, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	63
Std Dev	0



# B1L003S, U11-ch105, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U11-ch106, adc0

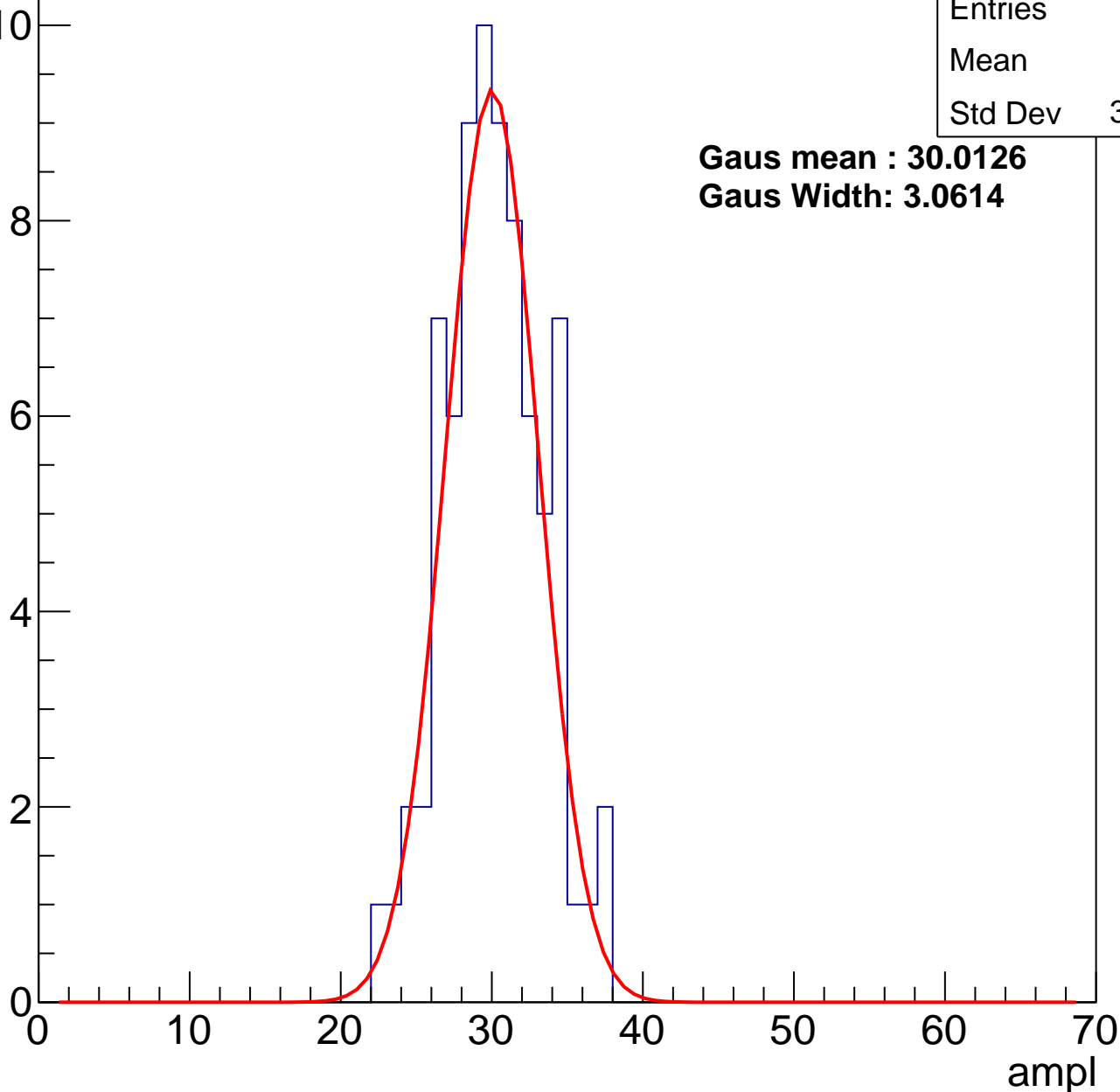
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	77
Mean	29.7
Std Dev	3.199

**Gaus mean : 30.0126**

**Gaus Width: 3.0614**



# B1L003S, U11-ch106, adc1

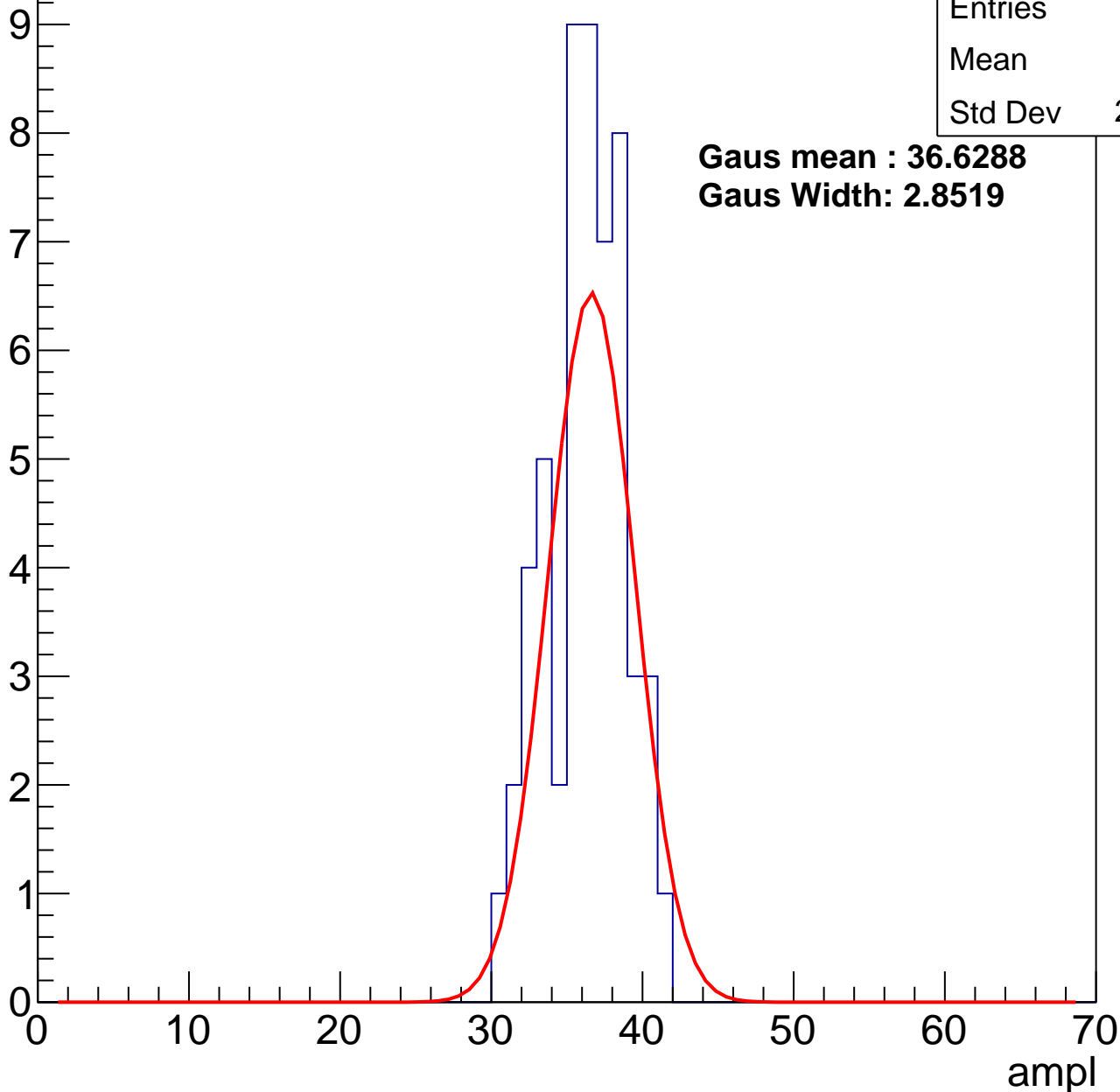
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	54
Mean	35.8
Std Dev	2.541

**Gaus mean : 36.6288**

**Gaus Width: 2.8519**



# B1L003S, U11-ch106, adc2

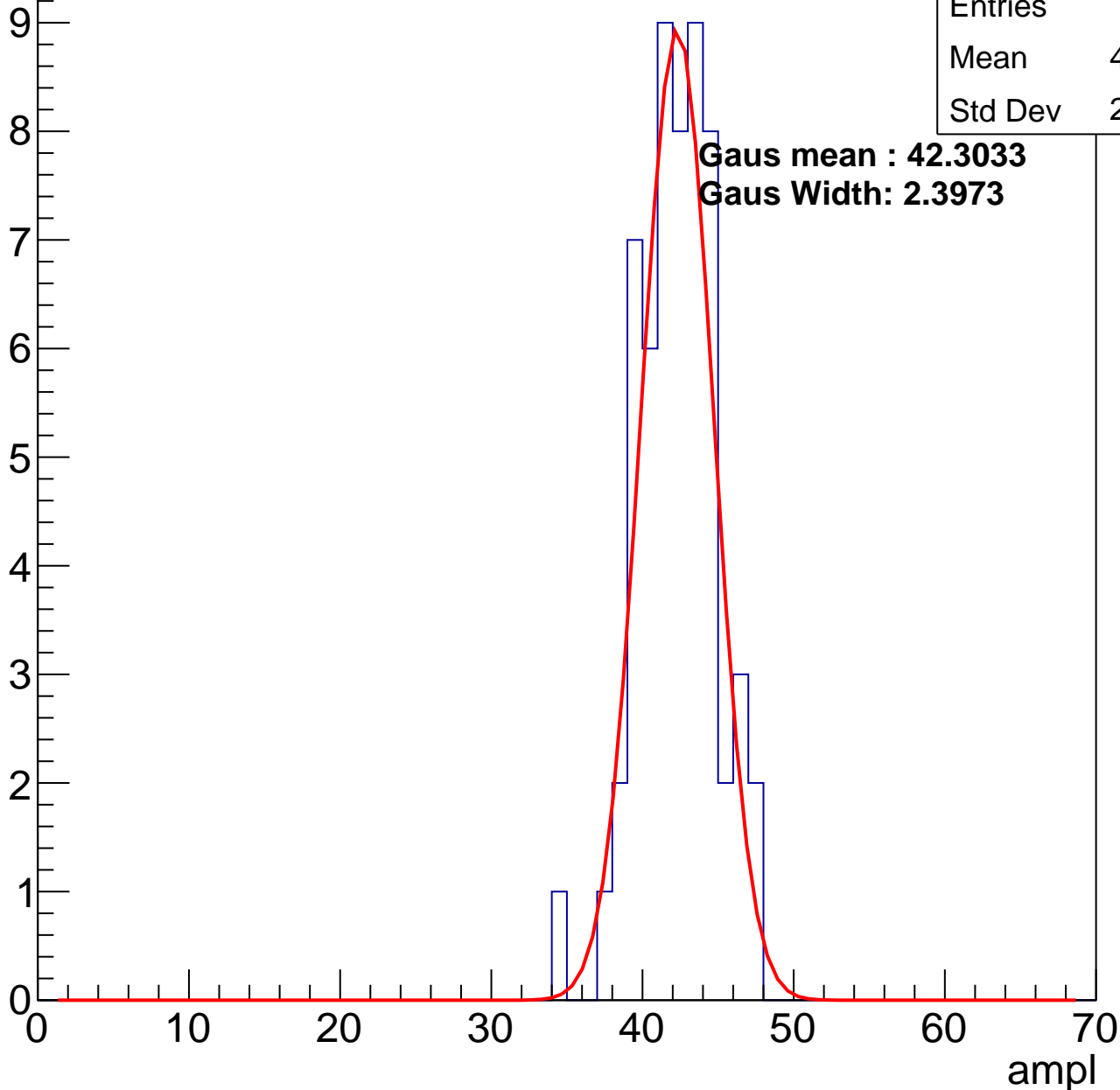
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	41.83
Std Dev	2.533

**Gaus mean : 42.3033**

**Gaus Width: 2.3973**



# B1L003S, U11-ch106, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	79
Mean	48.61
Std Dev	3.136

Entry

10

8

6

4

2

0

0

10

20

30

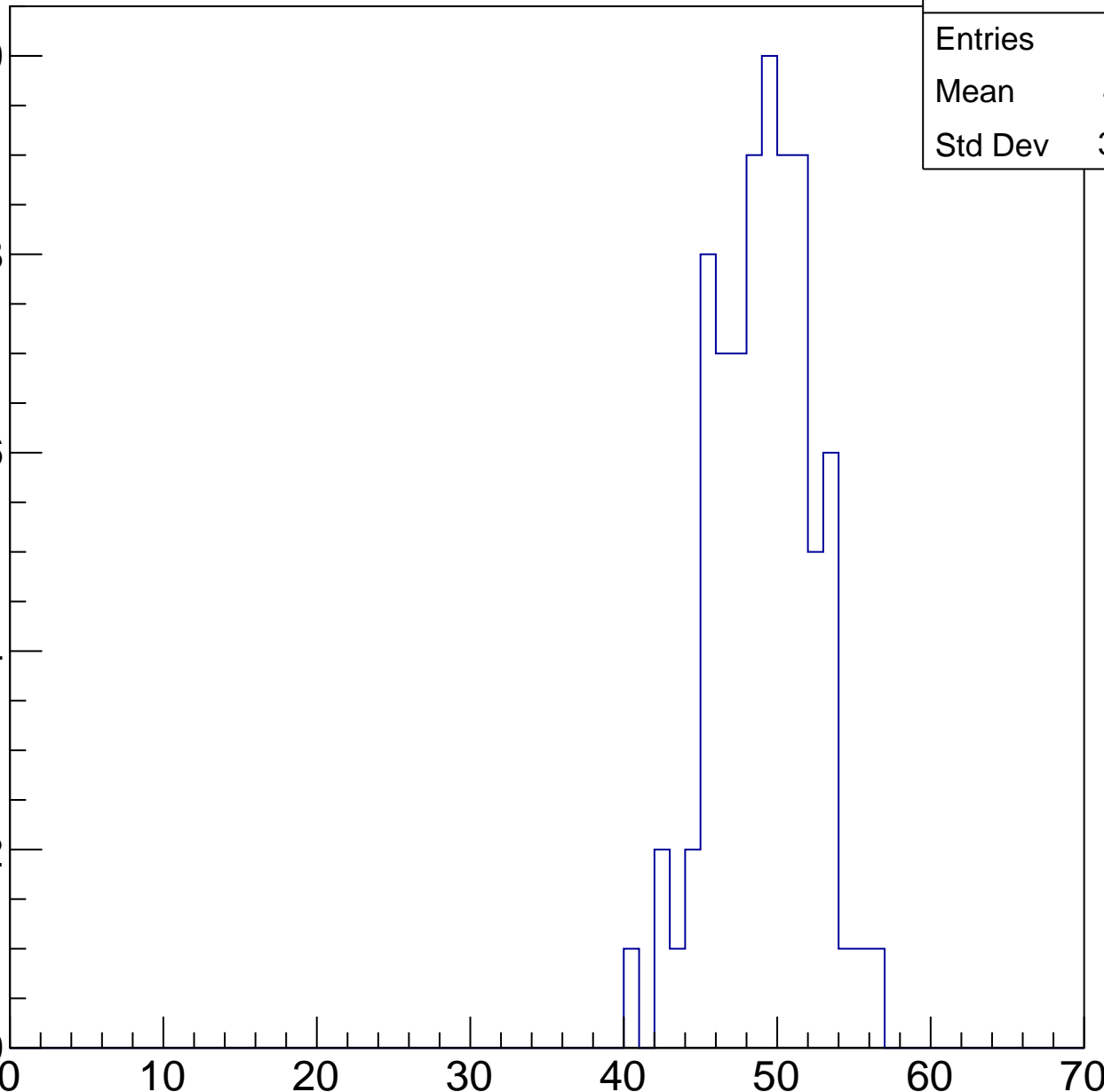
40

50

60

70

ampl

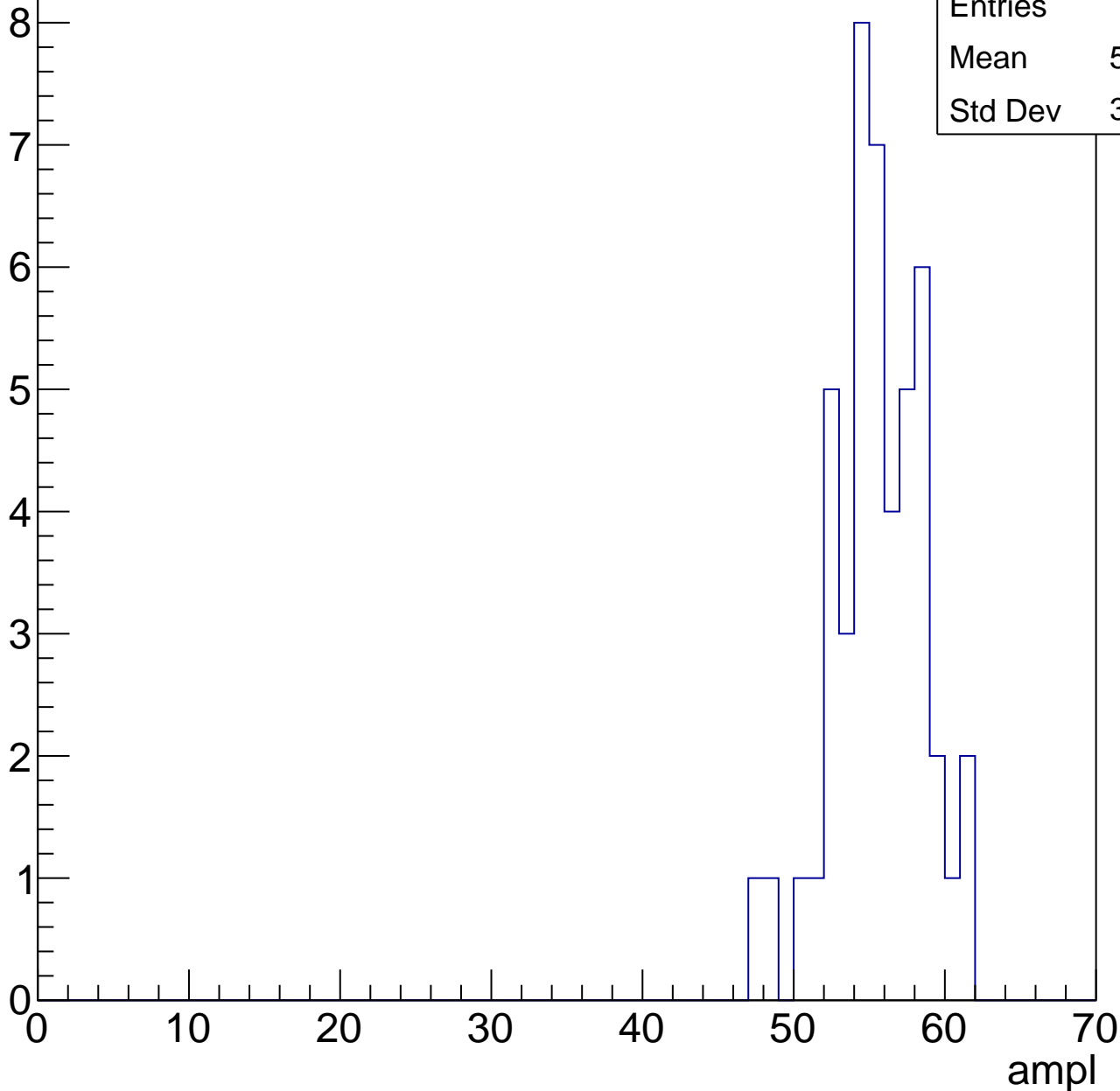


# B1L003S, U11-ch106, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	47
Mean	55.09
Std Dev	3.009



# B1L003S, U11-ch106, adc5

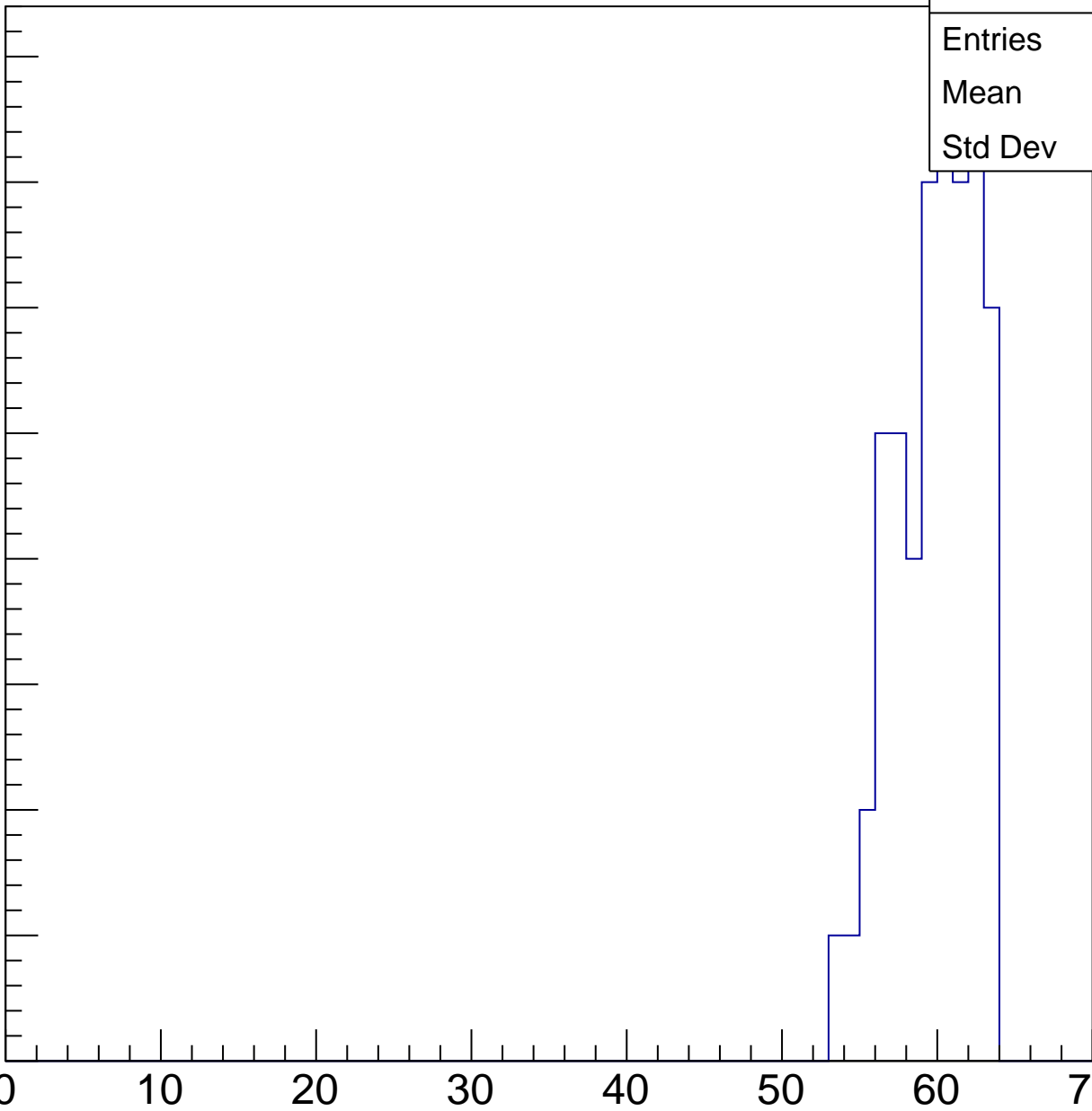
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	54
Mean	59.41
Std Dev	2.571

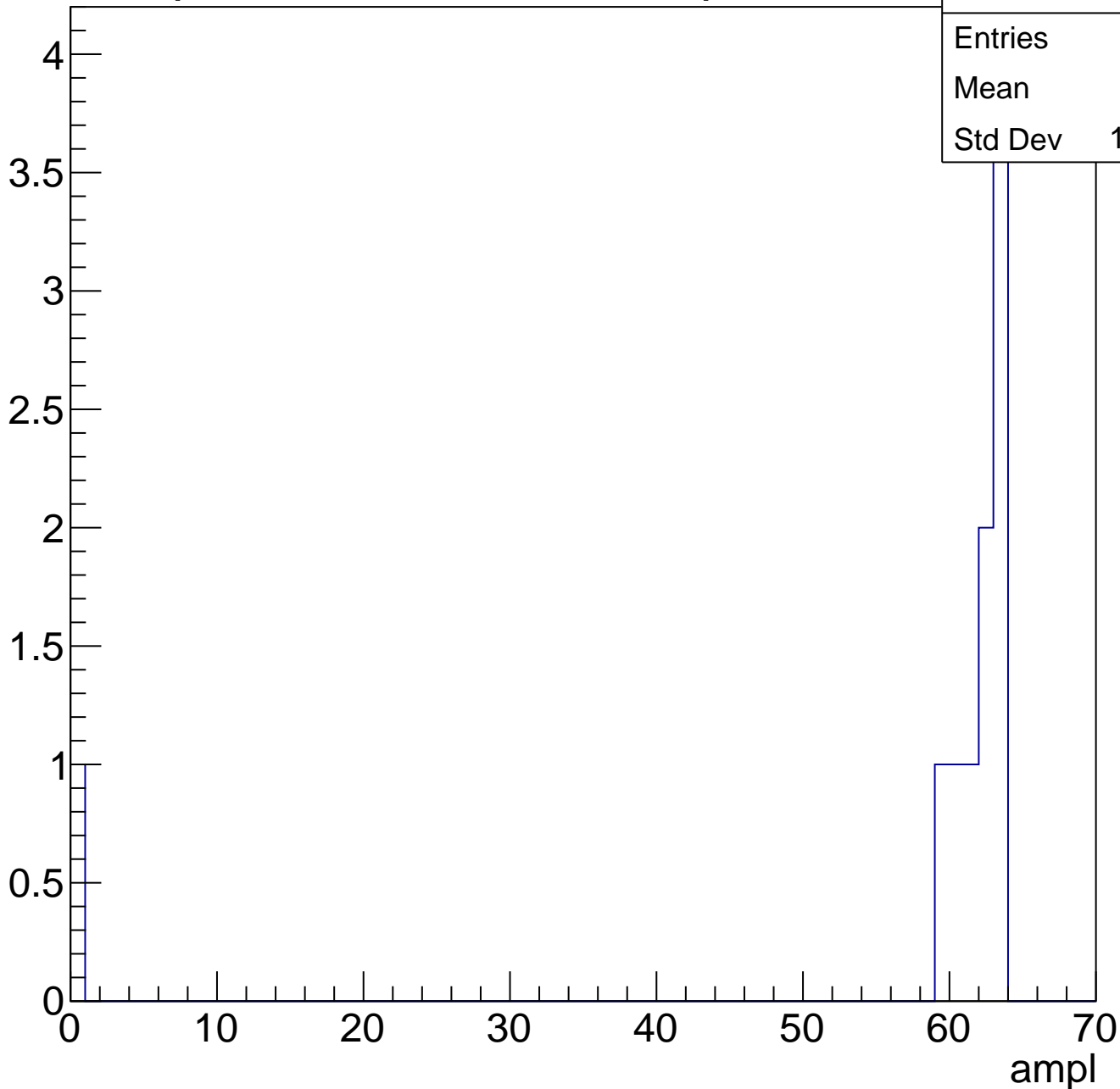
ampl



# B1L003S, U11-ch106, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

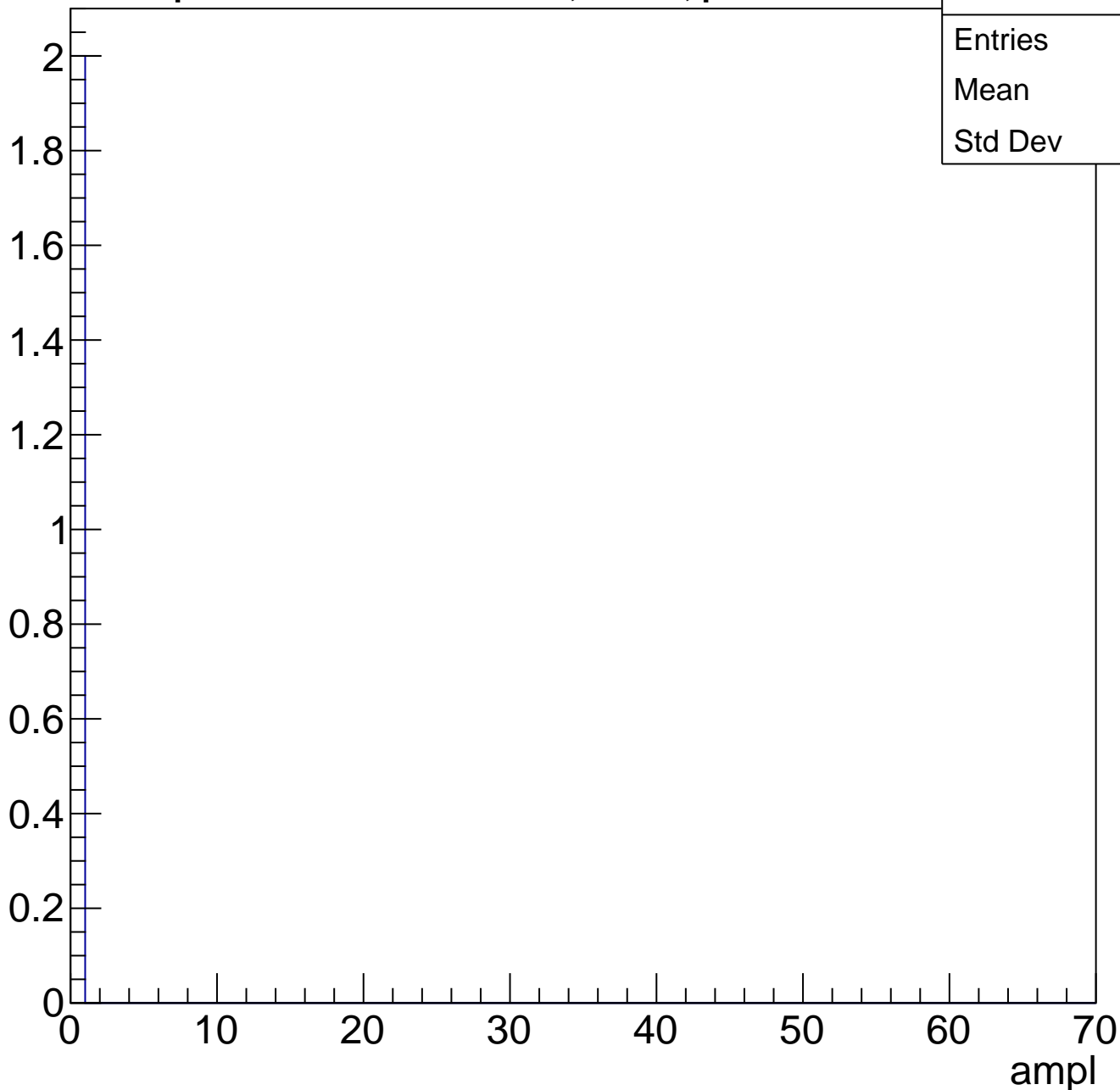




# B1L003S, U11-ch106, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U11-ch107, adc0

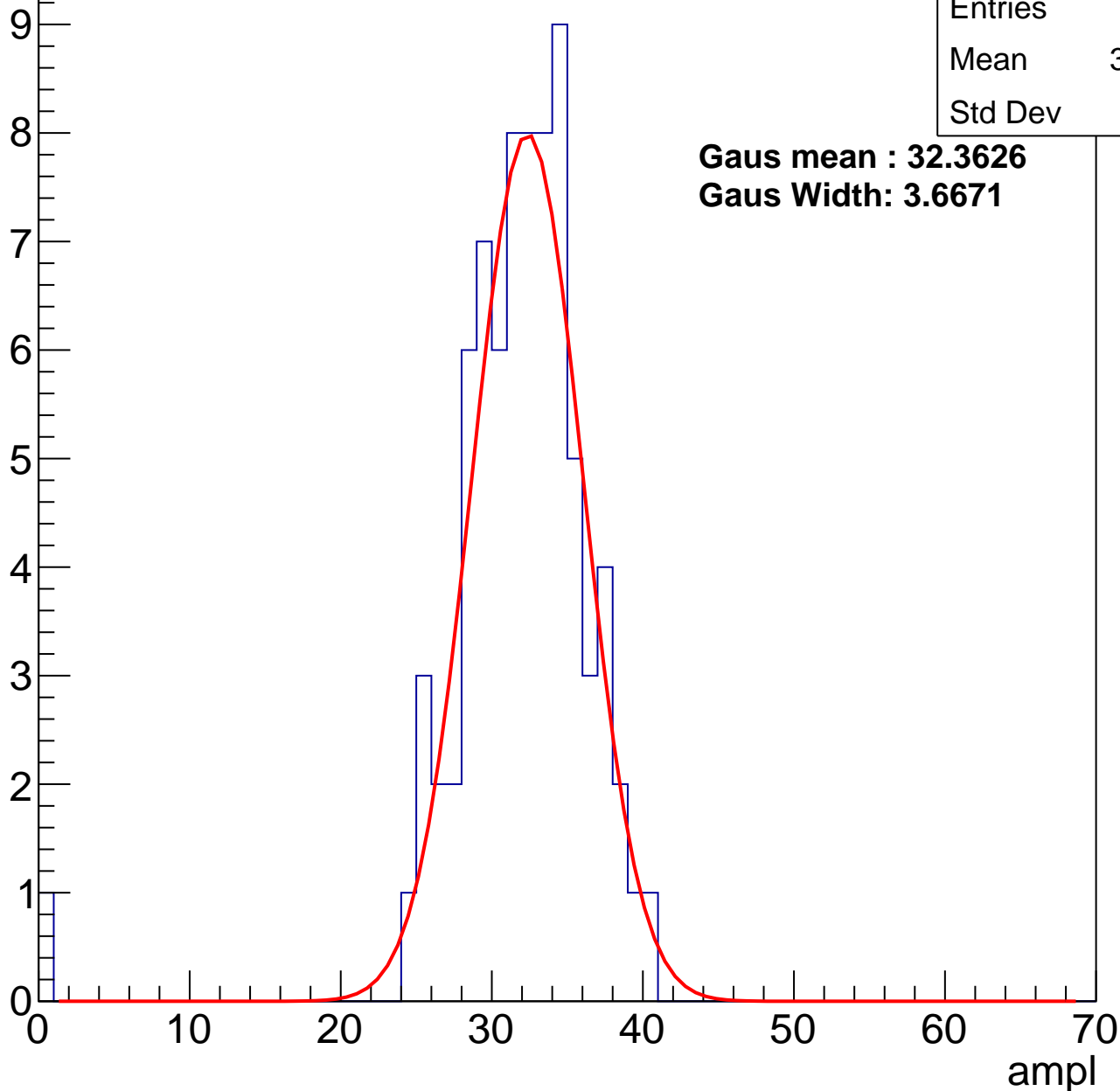
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	77
Mean	31.38
Std Dev	5.02

**Gaus mean : 32.3626**

**Gaus Width: 3.6671**



# B1L003S, U11-ch107, adc1

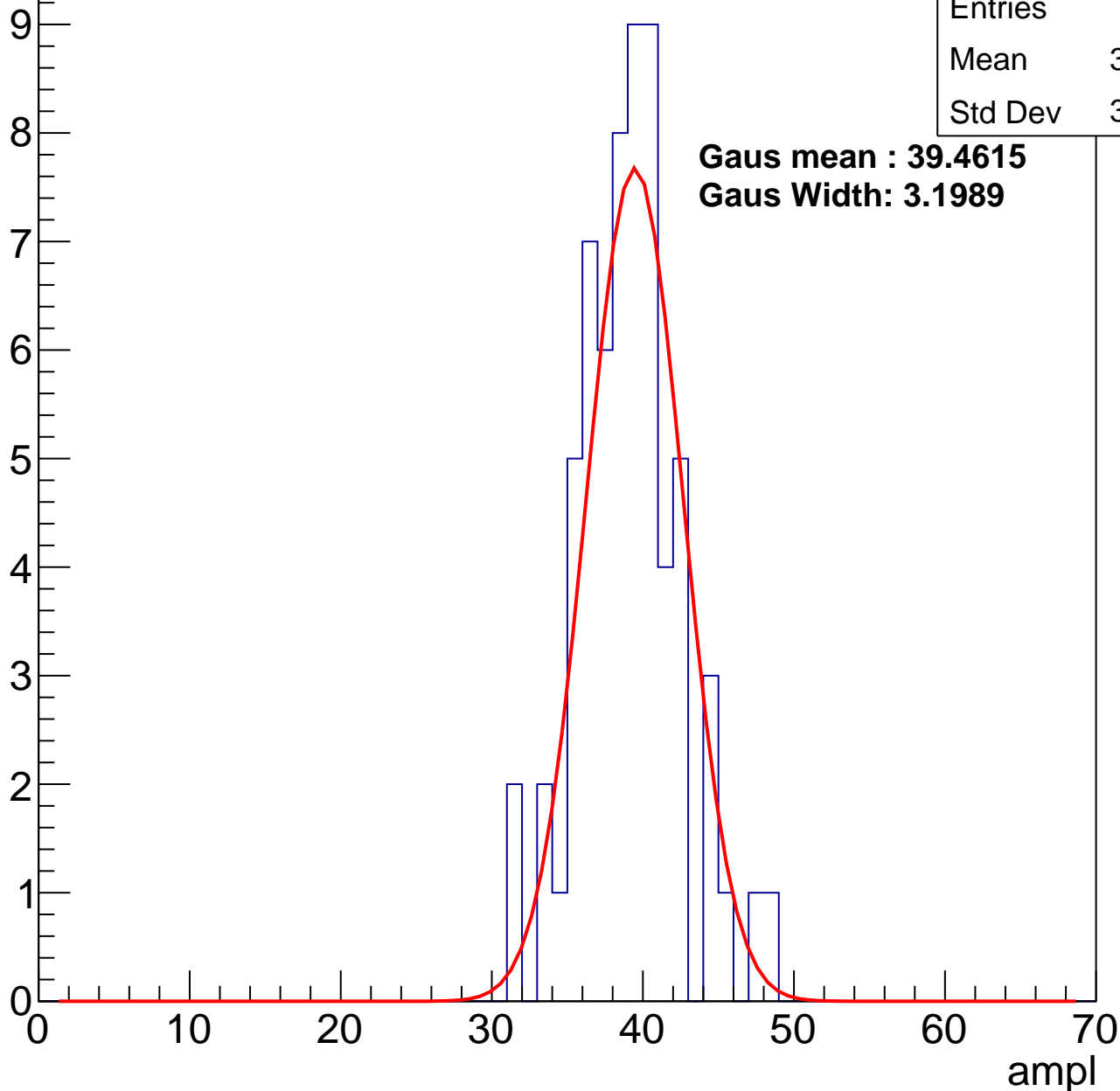
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	38.62
Std Dev	3.347

**Gaus mean : 39.4615**

**Gaus Width: 3.1989**



# B1L003S, U11-ch107, adc2

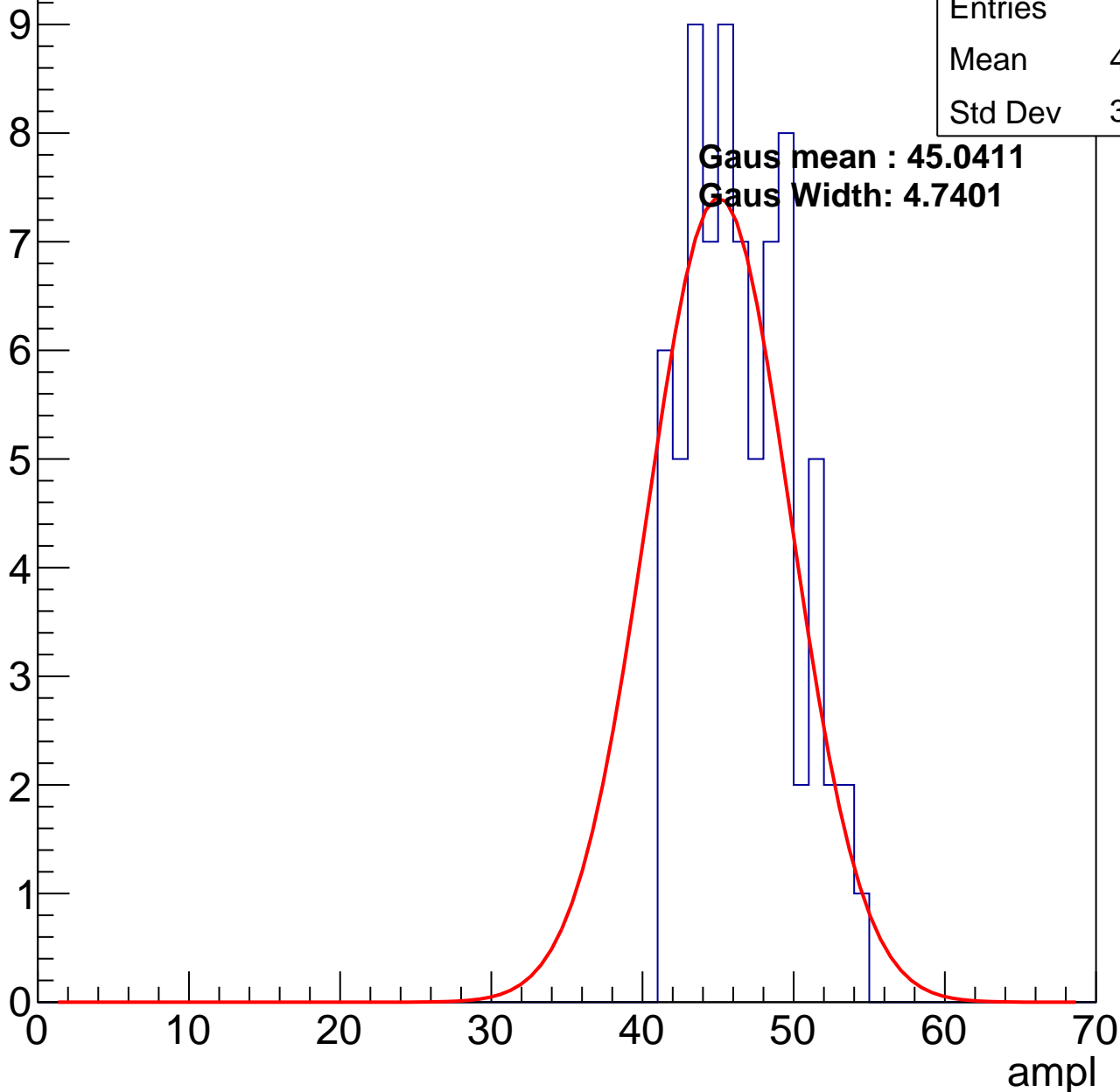
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	75
Mean	46.13
Std Dev	3.352

Gaus mean : 45.0411

Gaus Width: 4.7401

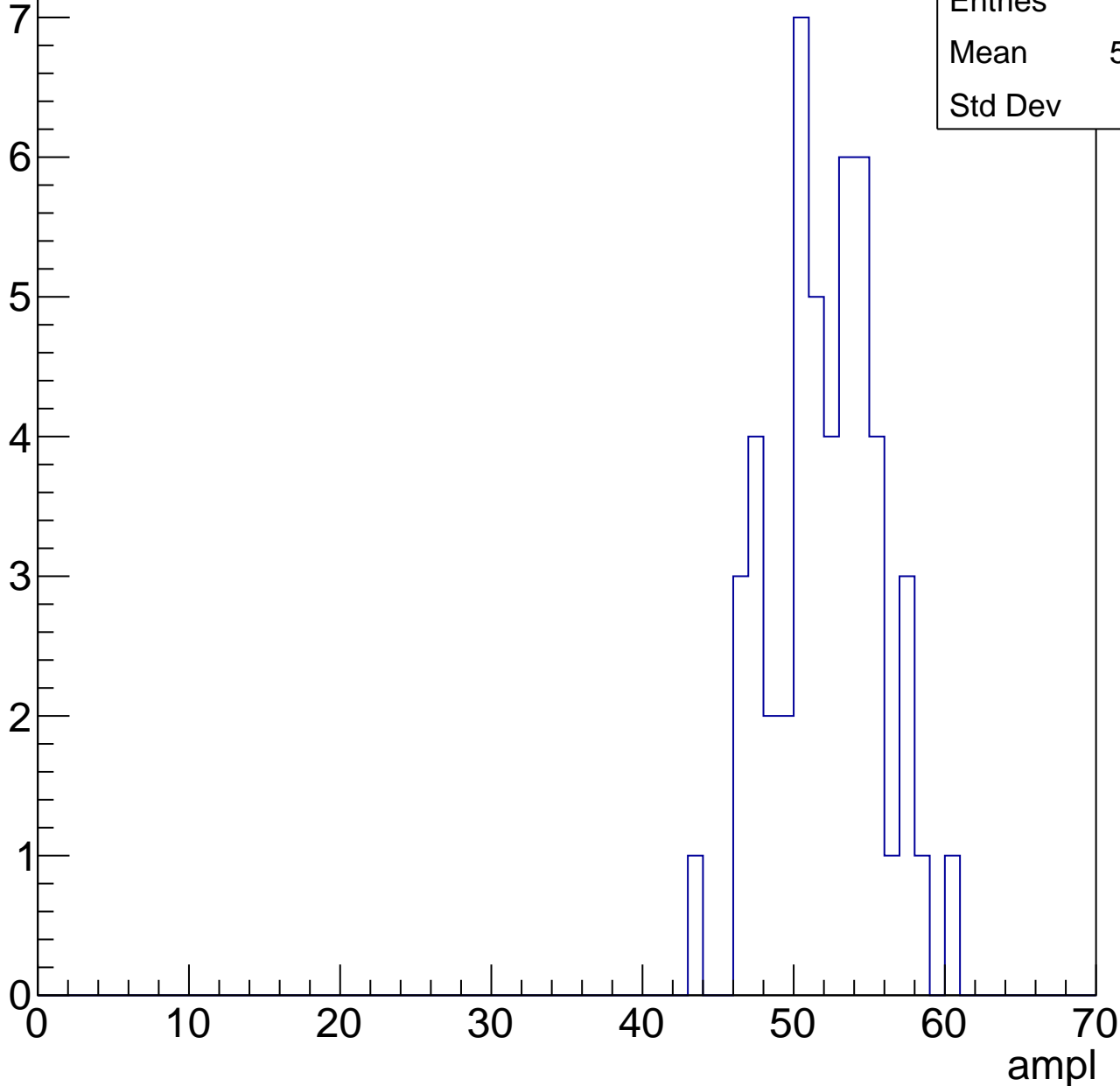


# B1L003S, U11-ch107, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	50
Mean	51.66
Std Dev	3.53

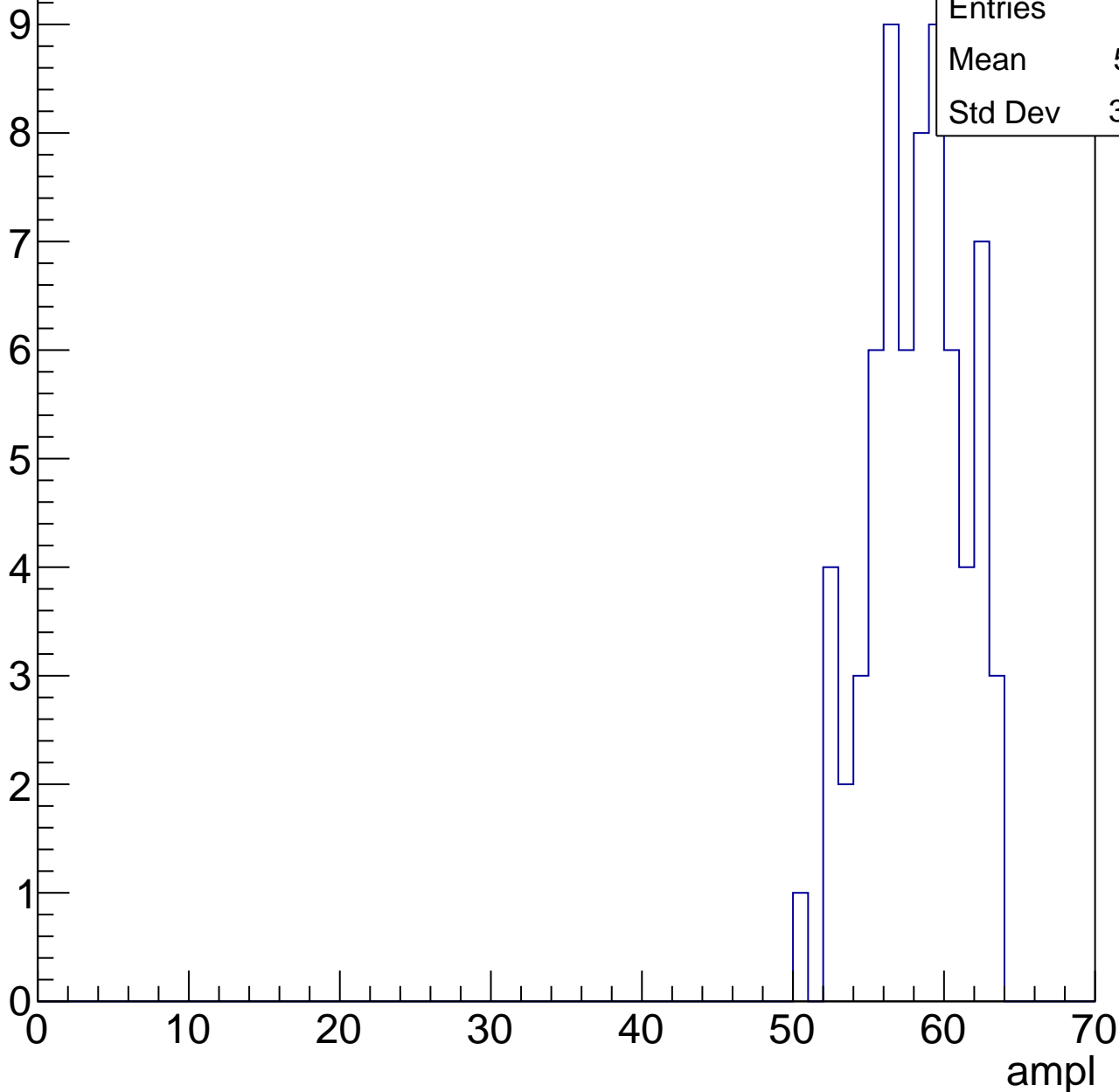


# B1L003S, U11-ch107, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	57.71
Std Dev	3.097

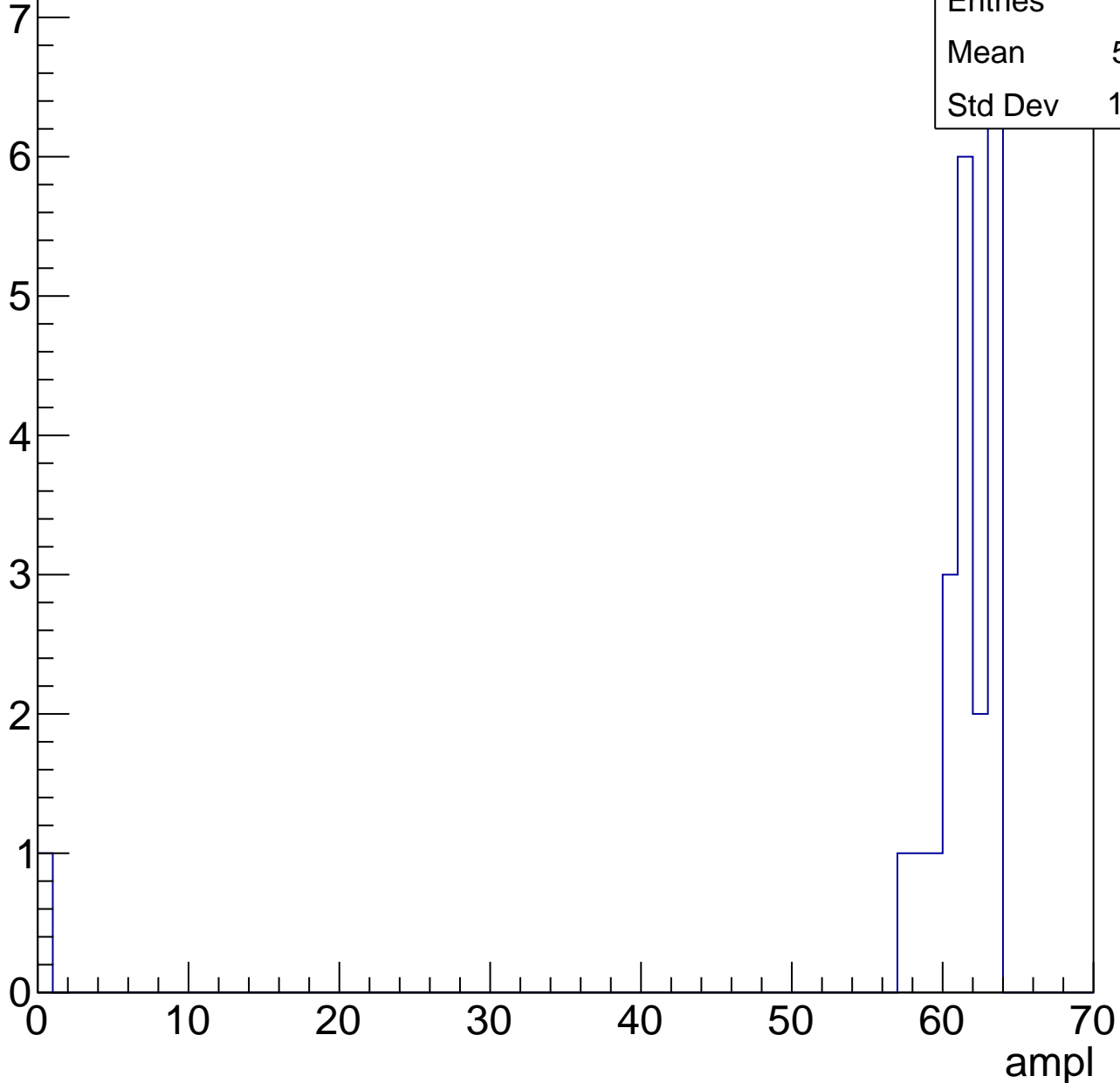


# B1L003S, U11-ch107, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	22
Mean	58.41
Std Dev	12.85



# B1L003S, U11-ch107, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch107, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U11-ch108, adc0

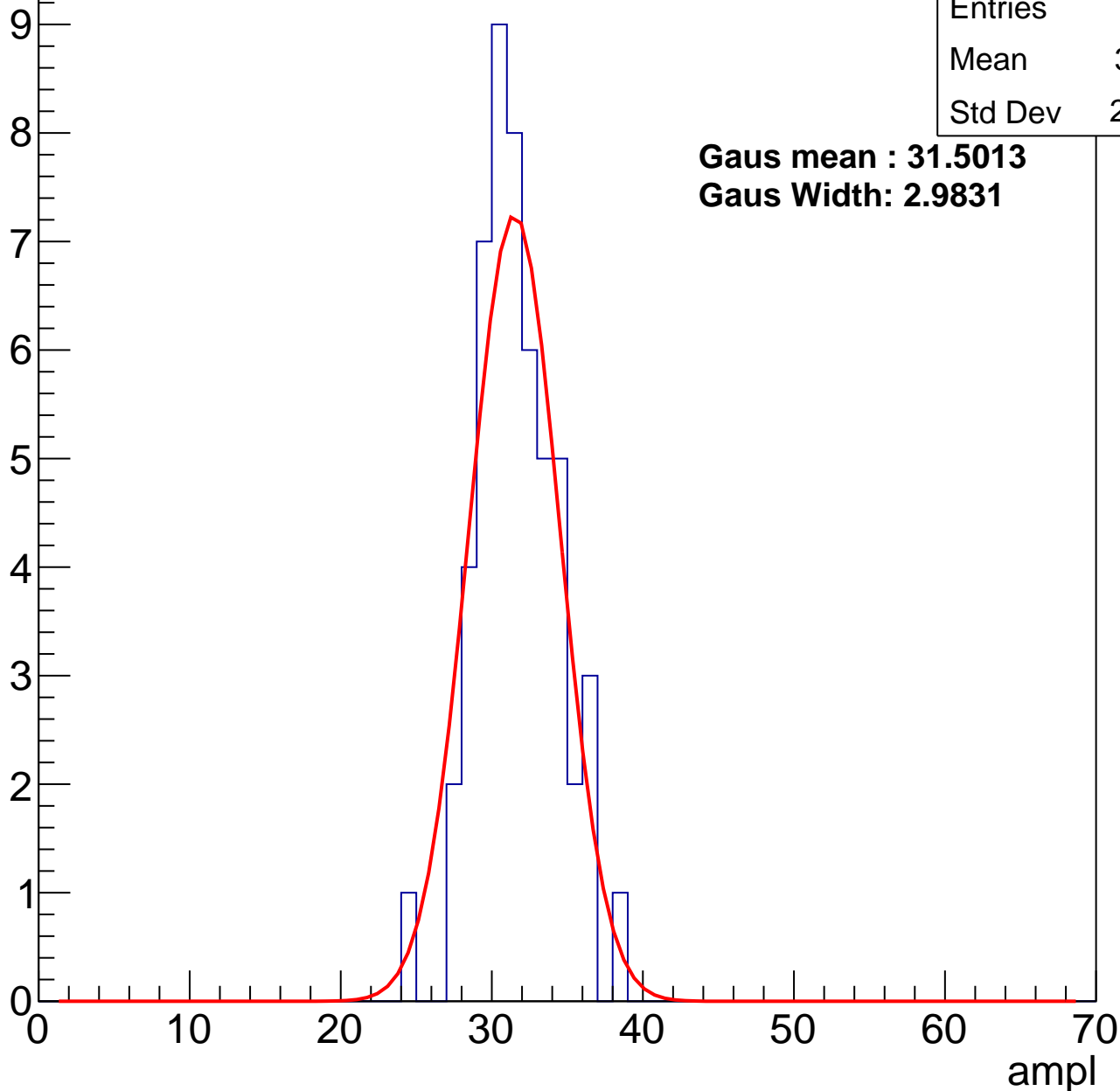
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	31.21
Std Dev	2.673

**Gaus mean : 31.5013**

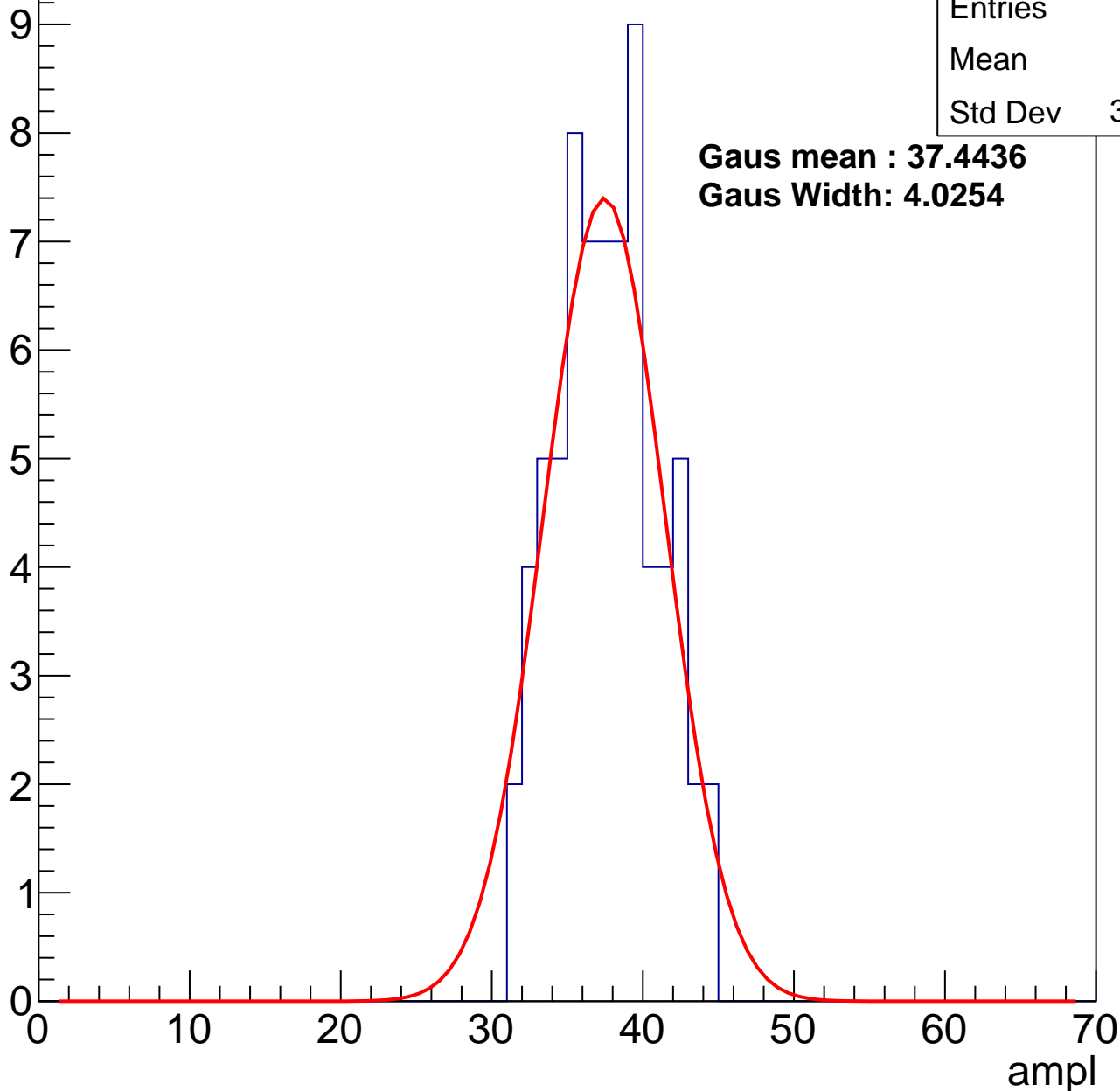
**Gaus Width: 2.9831**



# B1L003S, U11-ch108, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U11-ch108, adc2

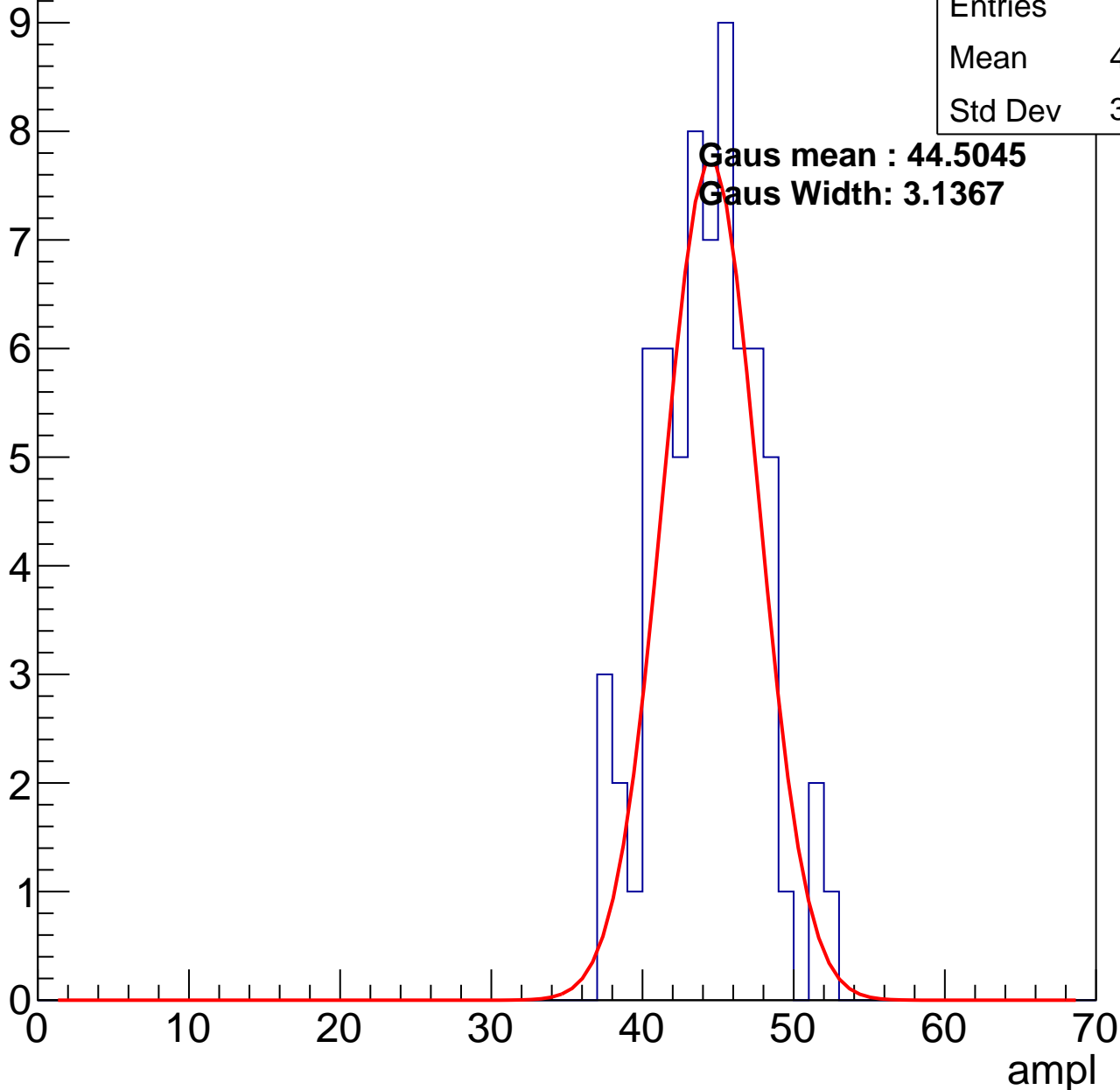
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	43.82
Std Dev	3.374

**Gaus mean : 44.5045**

**Gaus Width: 3.1367**

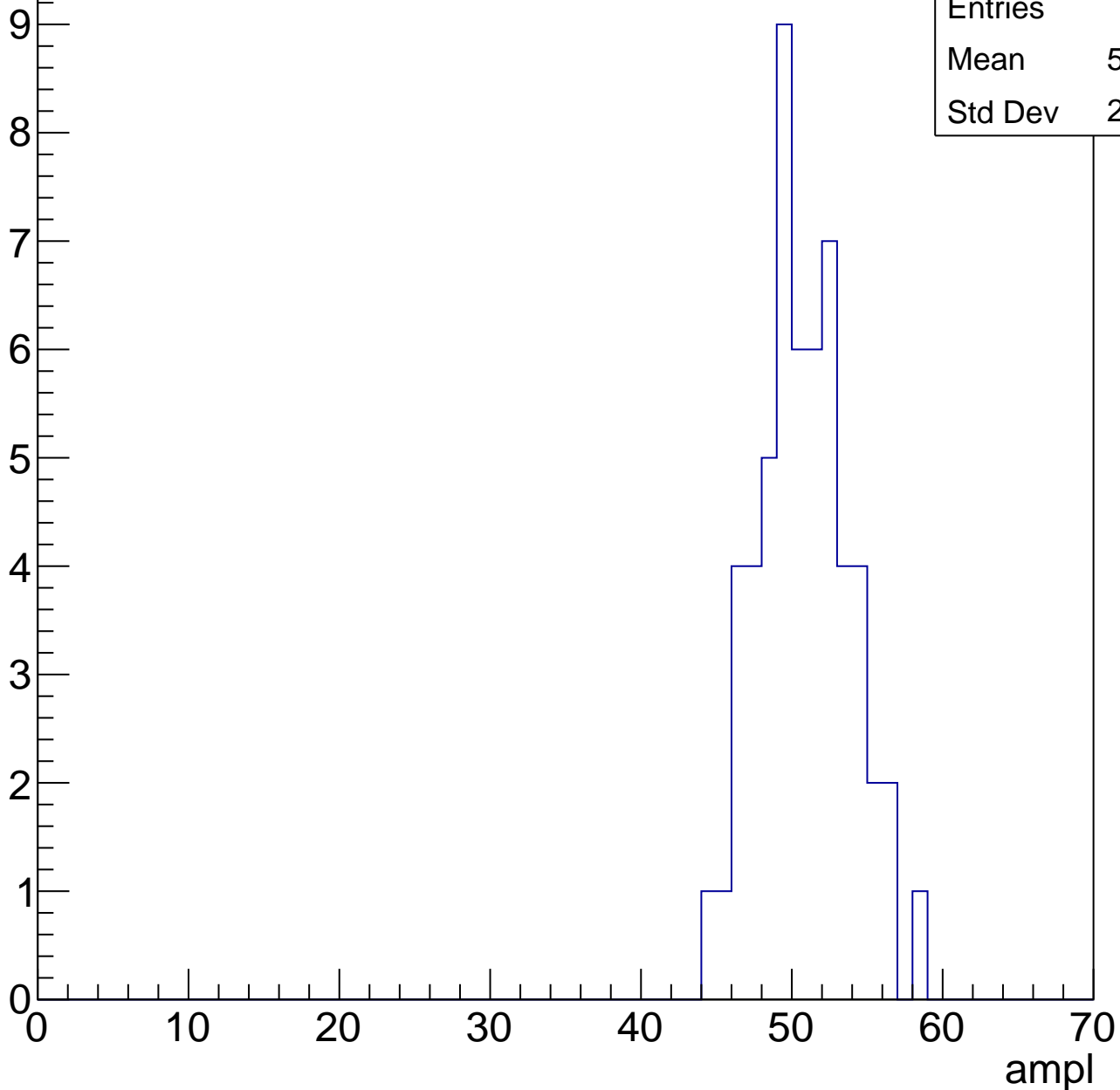


# B1L003S, U11-ch108, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	50.36
Std Dev	2.997

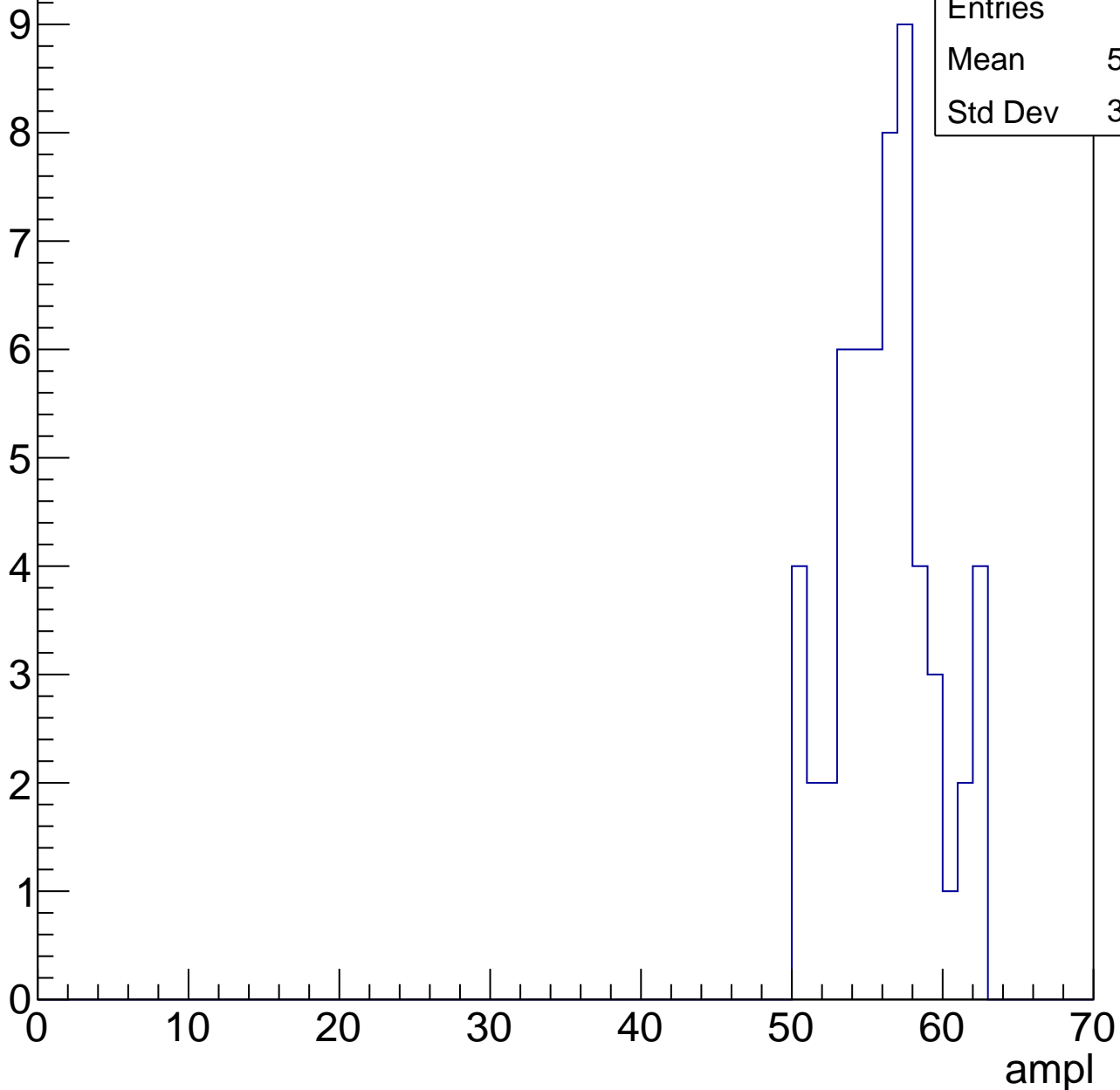


# B1L003S, U11-ch108, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	55.75
Std Dev	3.158

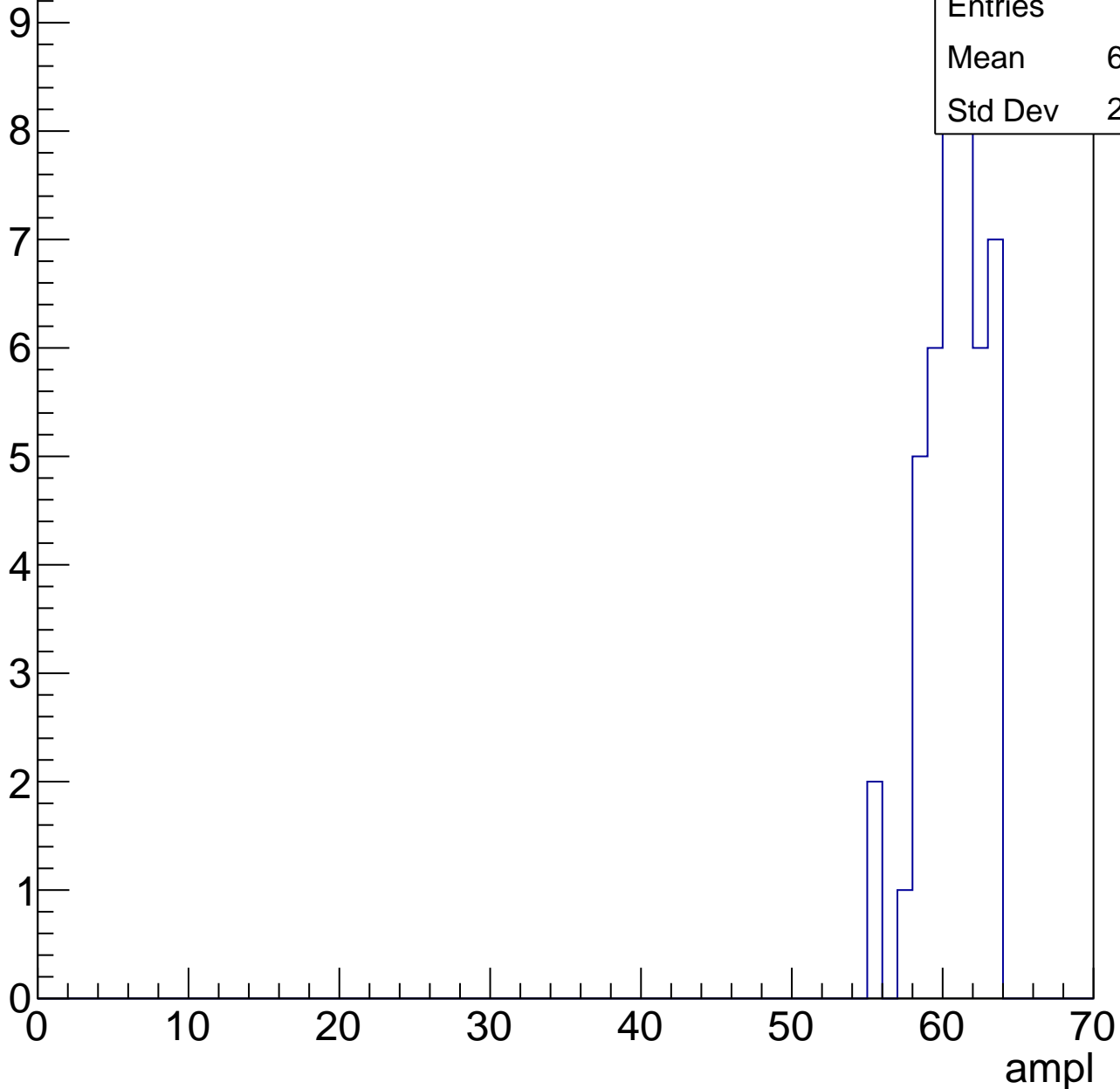


# B1L003S, U11-ch108, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

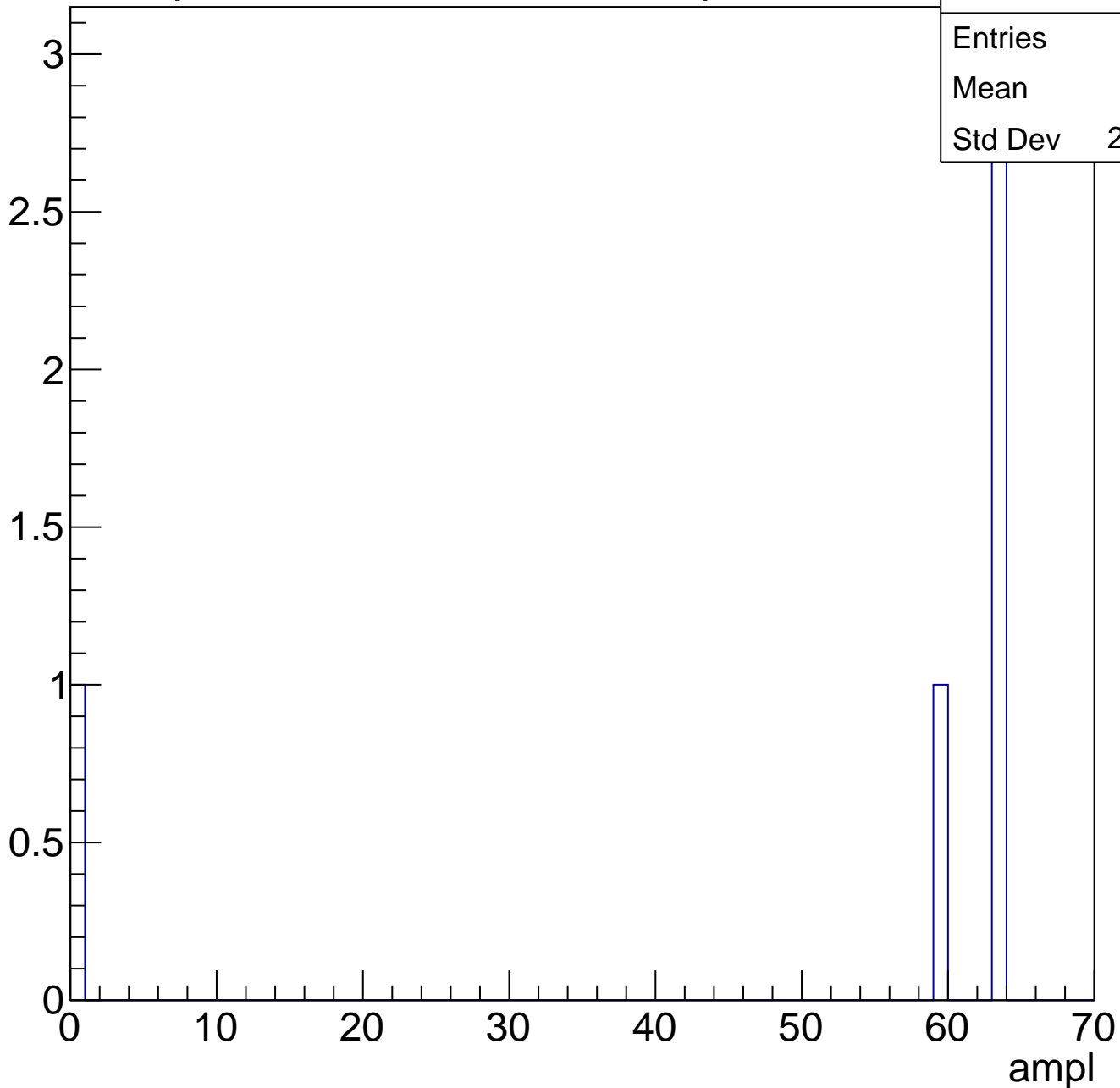
Entries	44
Mean	60.27
Std Dev	2.004



# B1L003S, U11-ch108, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch108, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U11-ch109, adc0

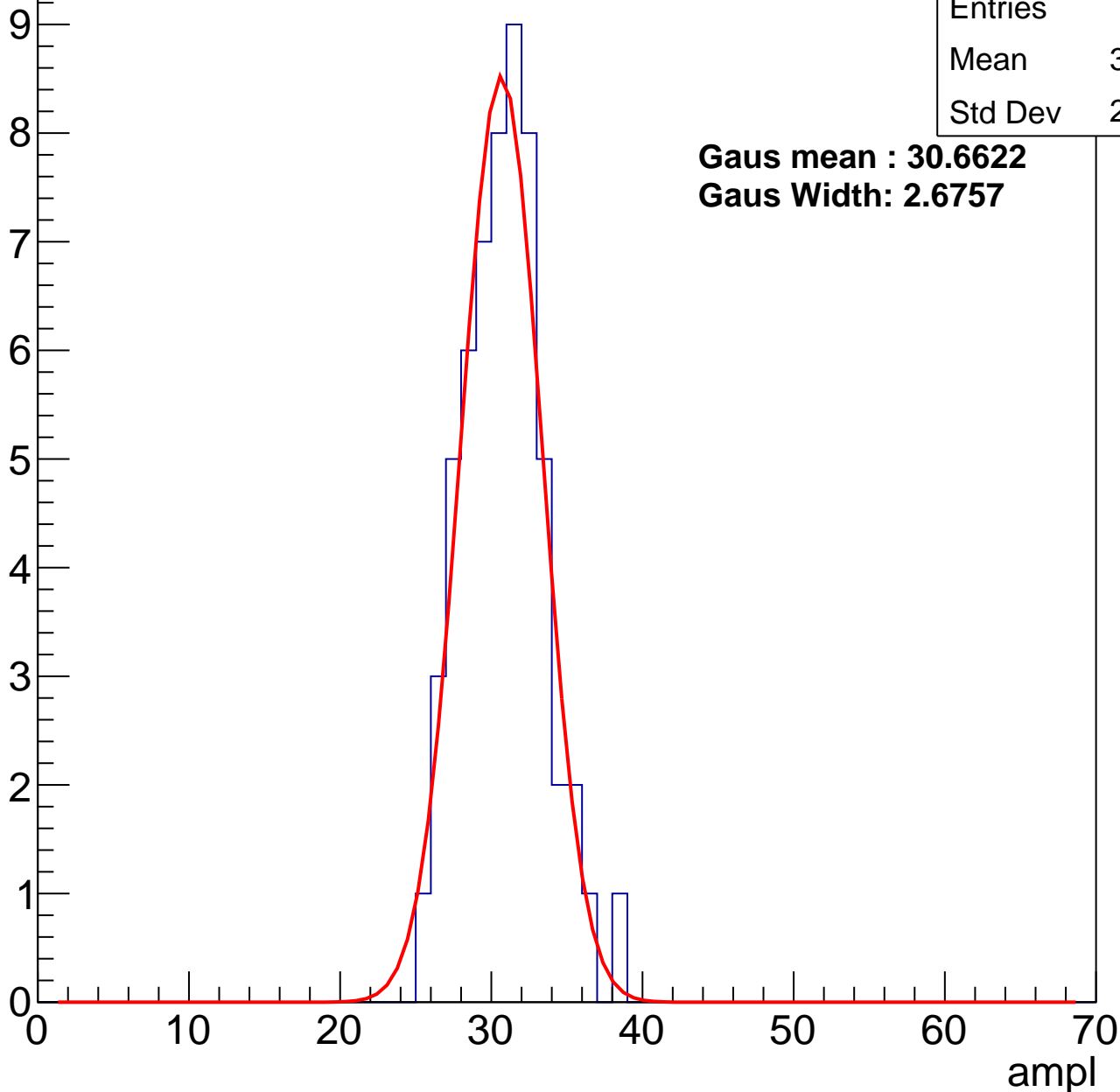
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	30.36
Std Dev	2.657

**Gaus mean : 30.6622**

**Gaus Width: 2.6757**



# B1L003S, U11-ch109, adc1

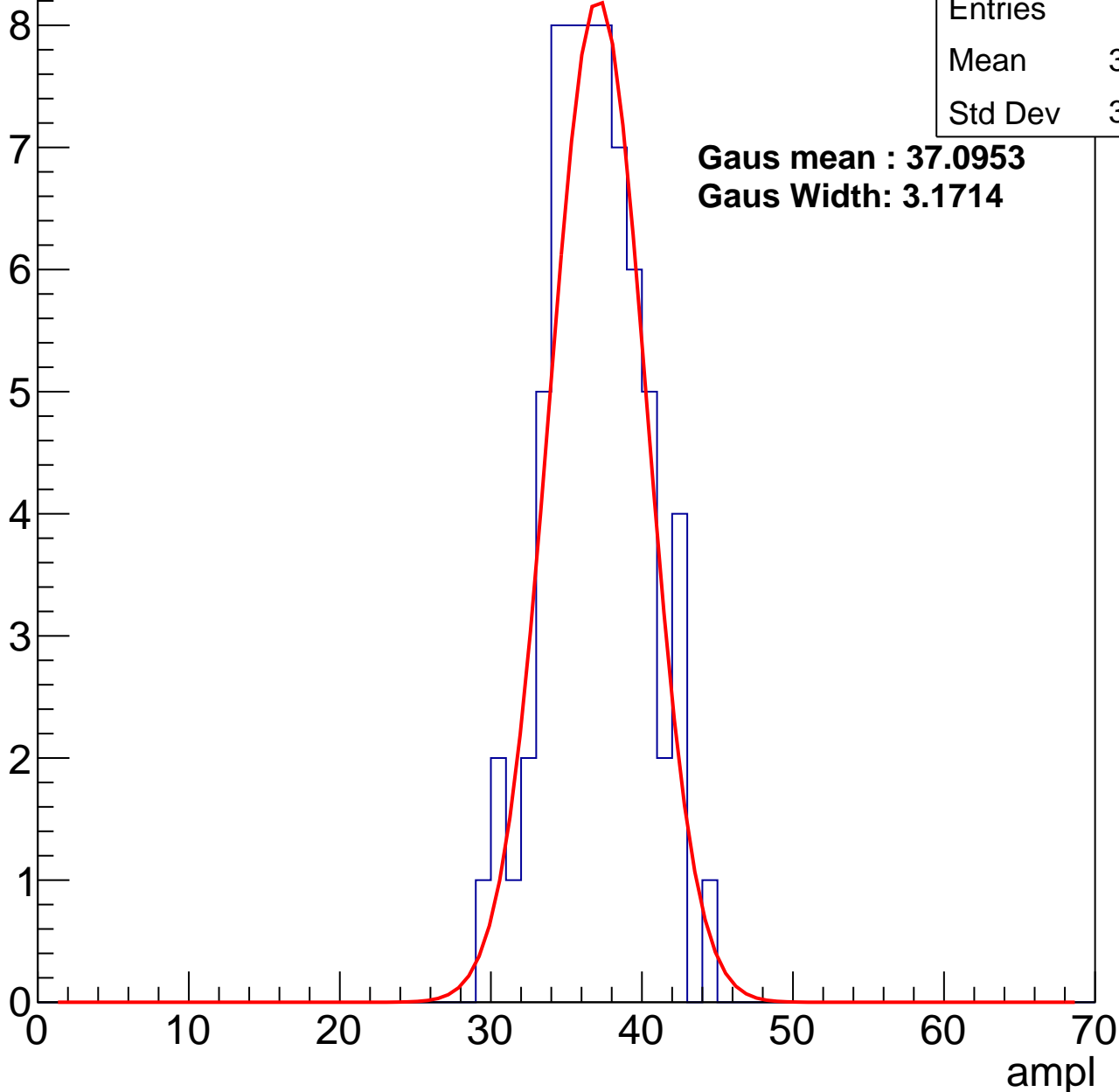
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	36.46
Std Dev	3.155

**Gaus mean : 37.0953**

**Gaus Width: 3.1714**



# B1L003S, U11-ch109, adc2

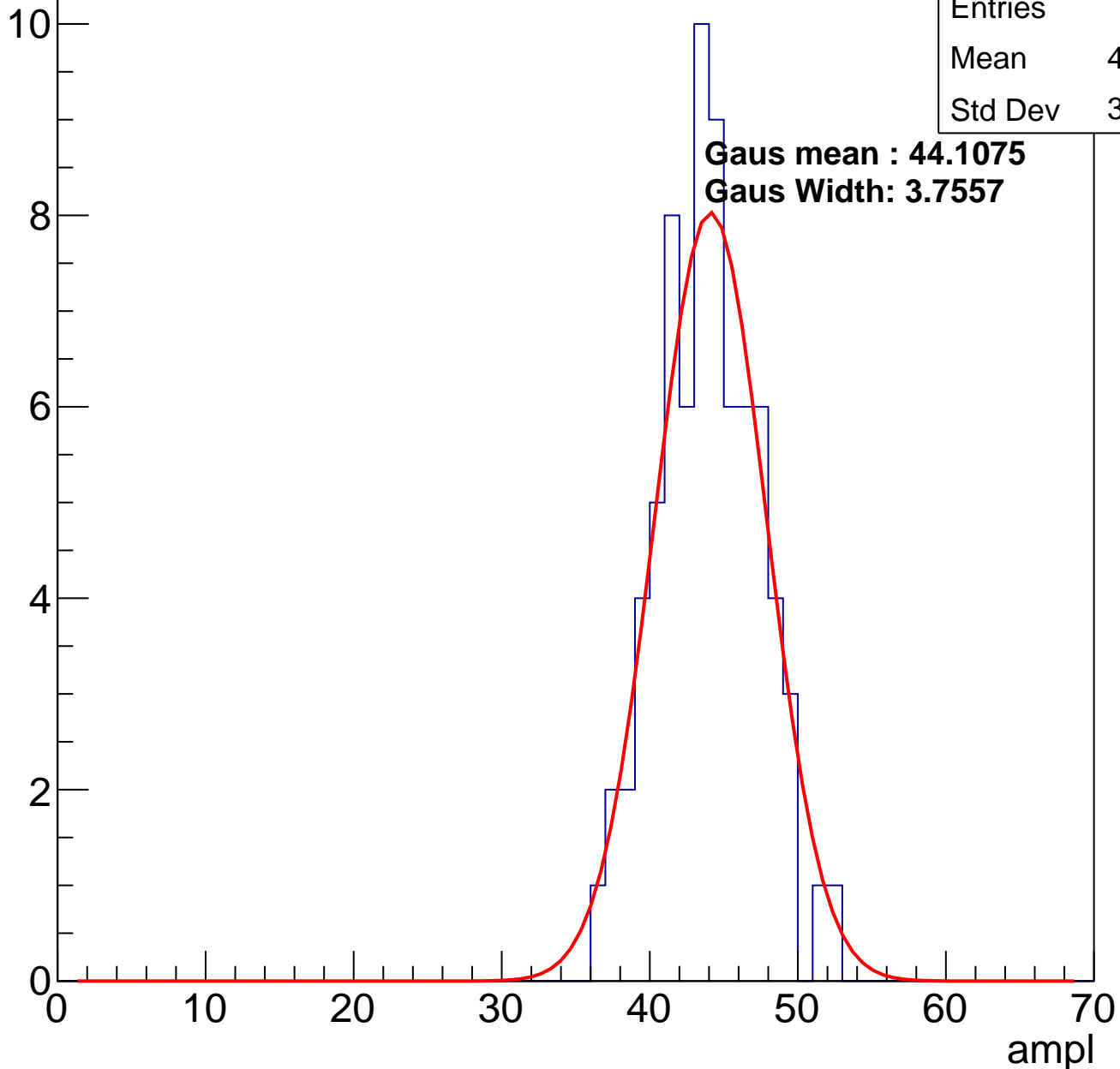
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	74
Mean	43.49
Std Dev	3.362

**Gaus mean : 44.1075**

**Gaus Width: 3.7557**

Entry

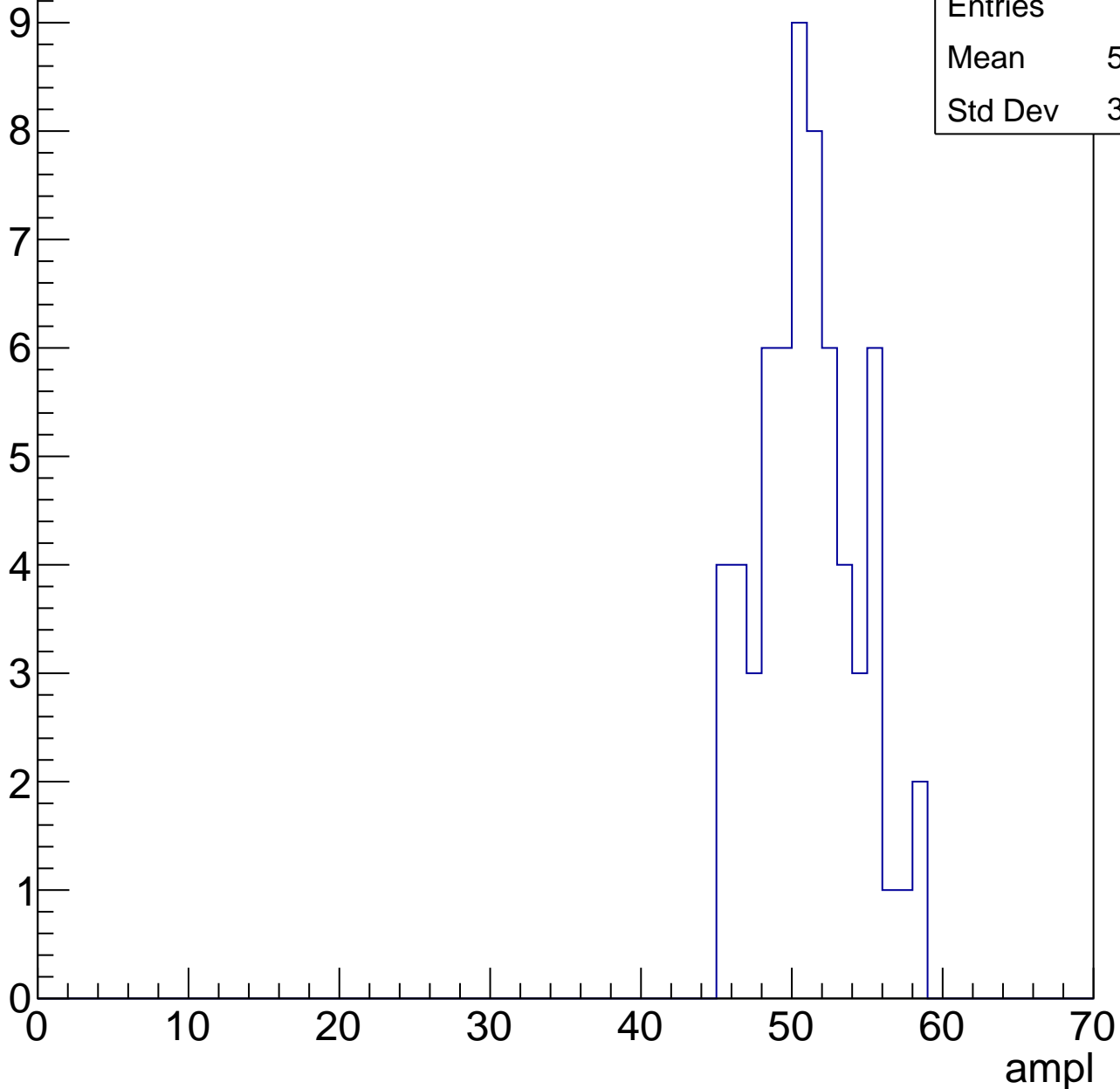


# B1L003S, U11-ch109, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	50.63
Std Dev	3.272



# B1L003S, U11-ch109, adc4

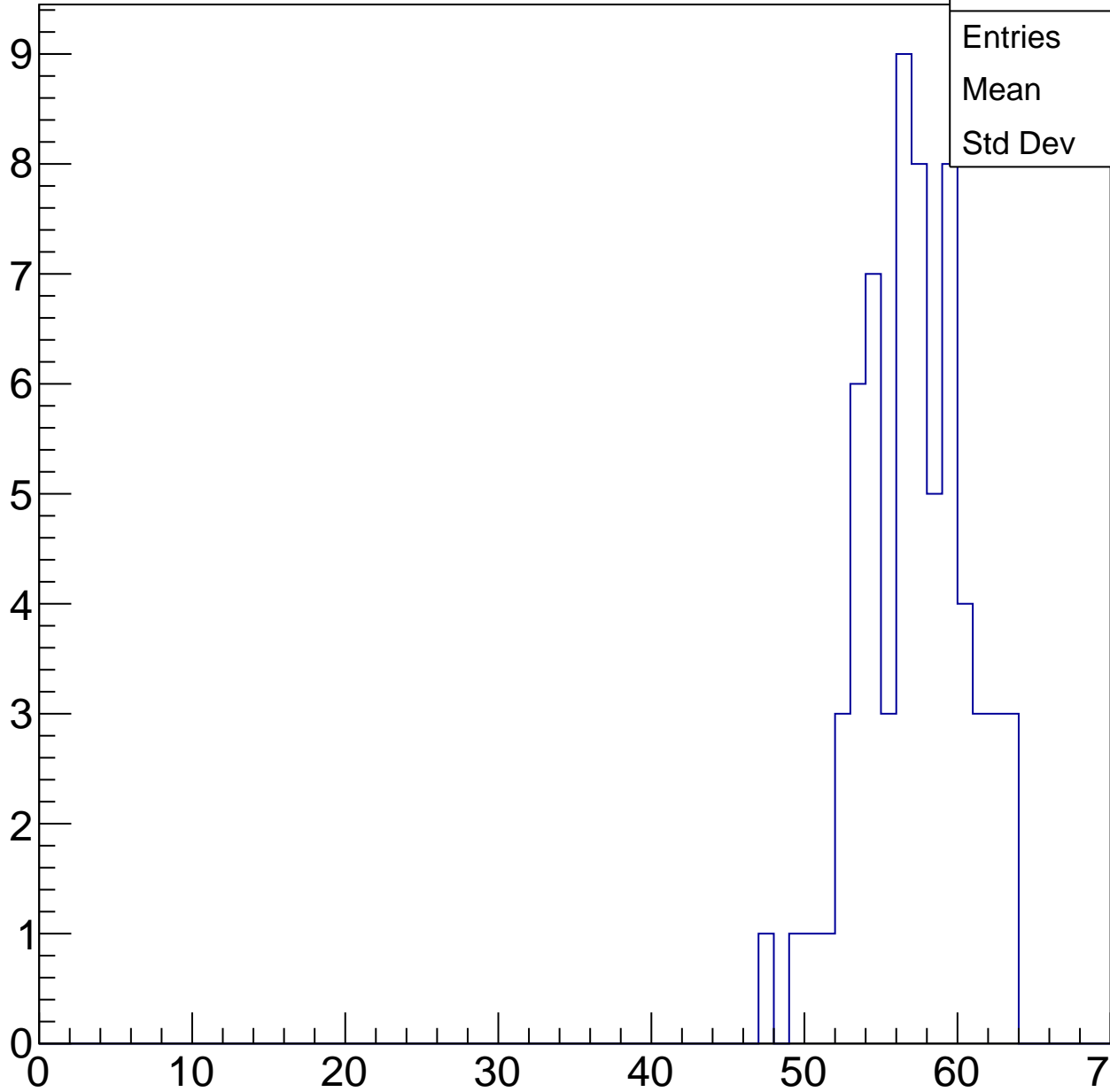
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	66
Mean	56.58
Std Dev	3.473

ampl

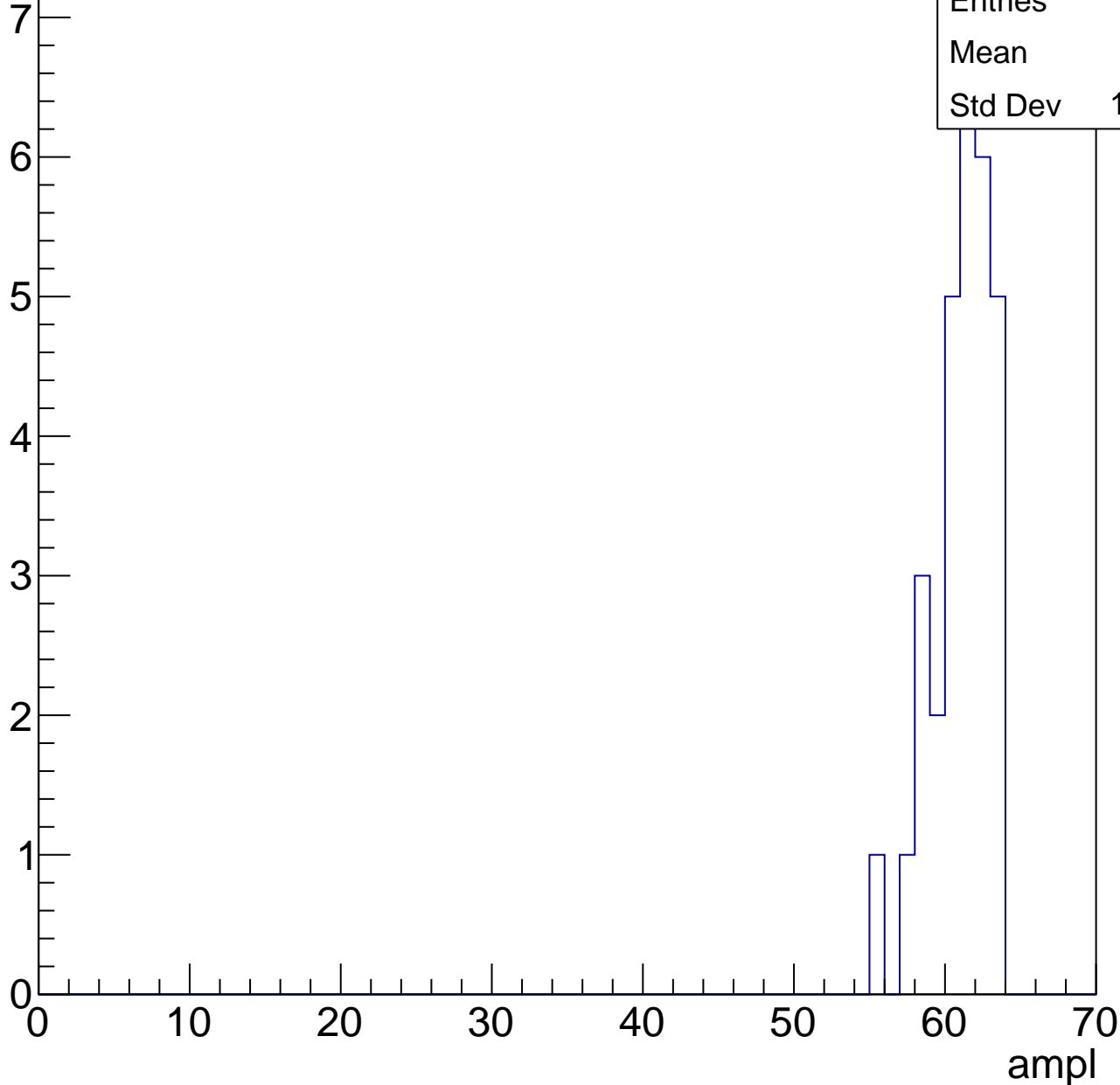


# B1L003S, U11-ch109, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

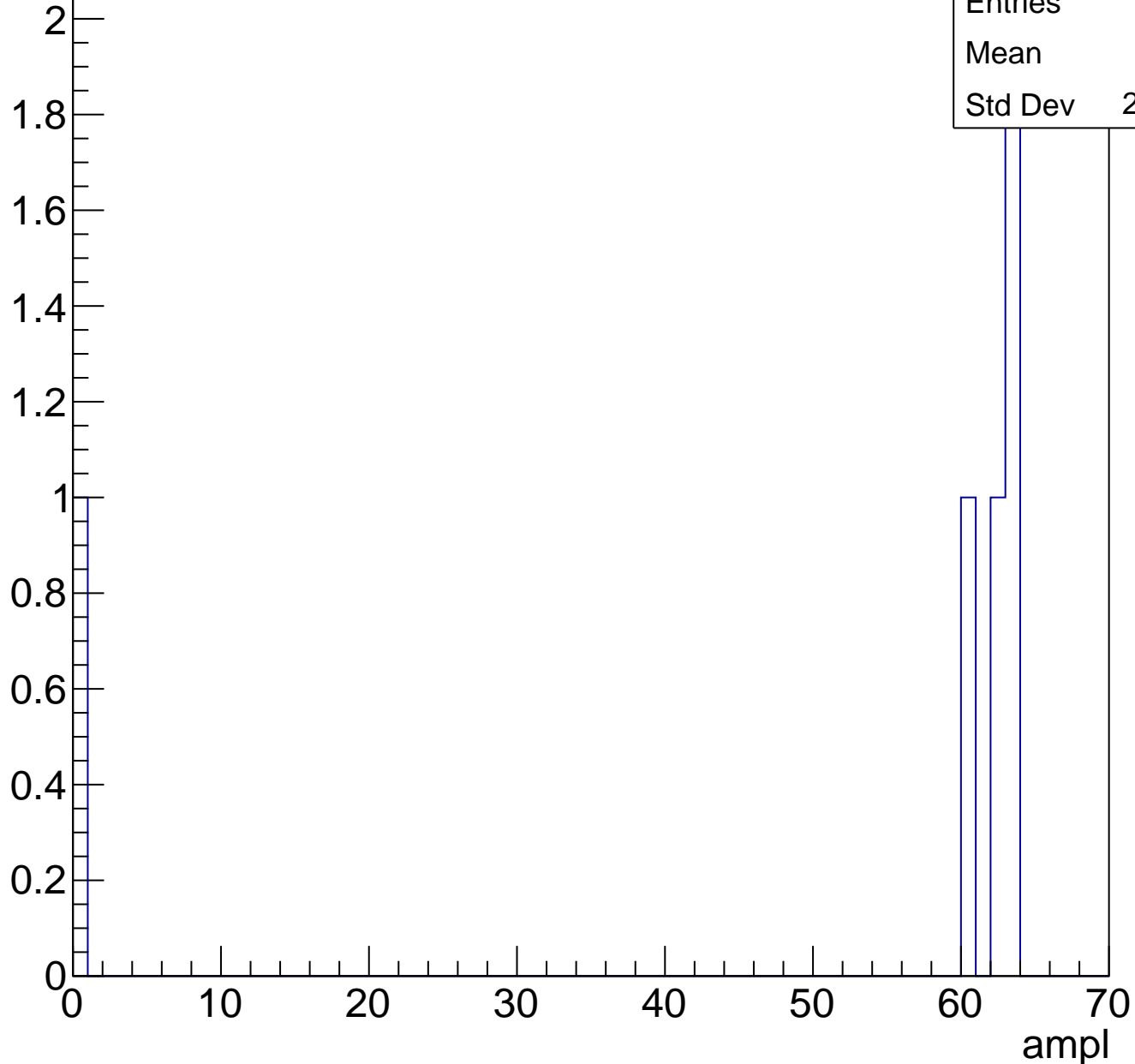
Entries	30
Mean	60.6
Std Dev	1.943



# B1L003S, U11-ch109, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	5
Mean	49.6
Std Dev	24.82



# B1L003S, U11-ch109, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	22
Std Dev	0

# B1L003S, U11-ch110, adc0

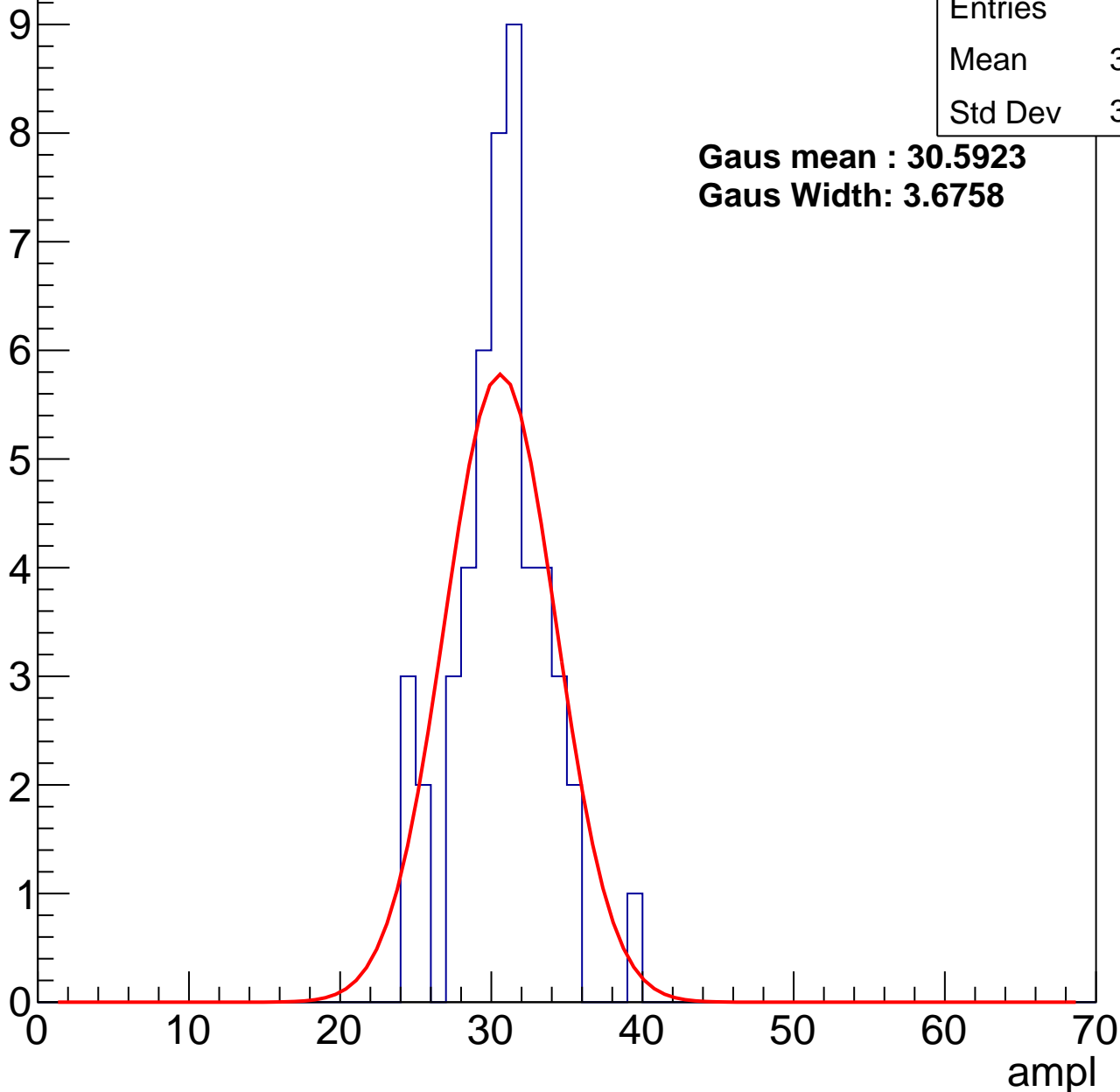
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	49
Mean	30.18
Std Dev	3.015

**Gaus mean : 30.5923**

**Gaus Width: 3.6758**



# B1L003S, U11-ch110, adc1

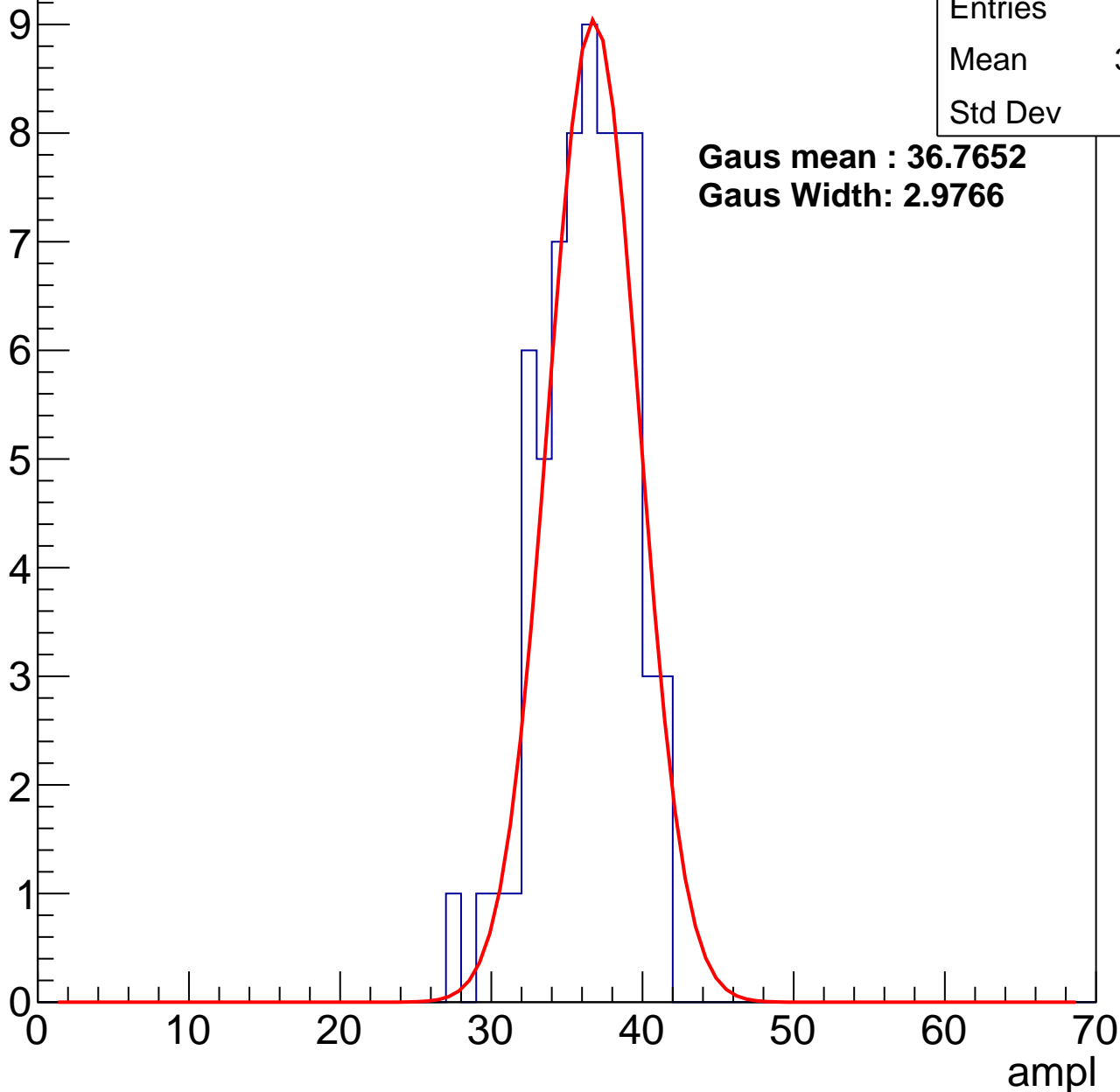
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	35.81
Std Dev	2.95

**Gaus mean : 36.7652**

**Gaus Width: 2.9766**



# B1L003S, U11-ch110, adc2

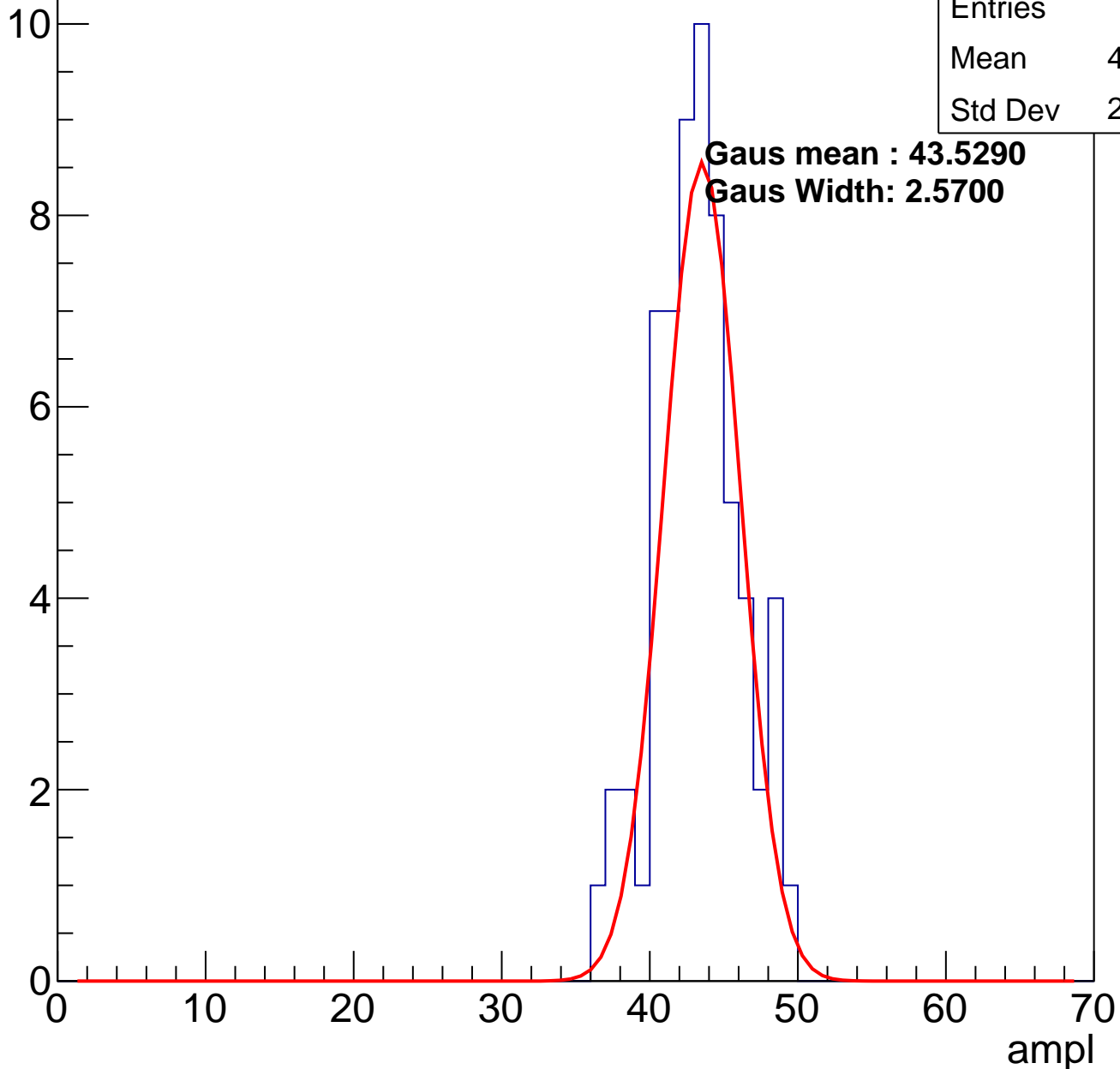
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	63
Mean	42.79
Std Dev	2.863

**Gaus mean : 43.5290**

**Gaus Width: 2.5700**

Entry

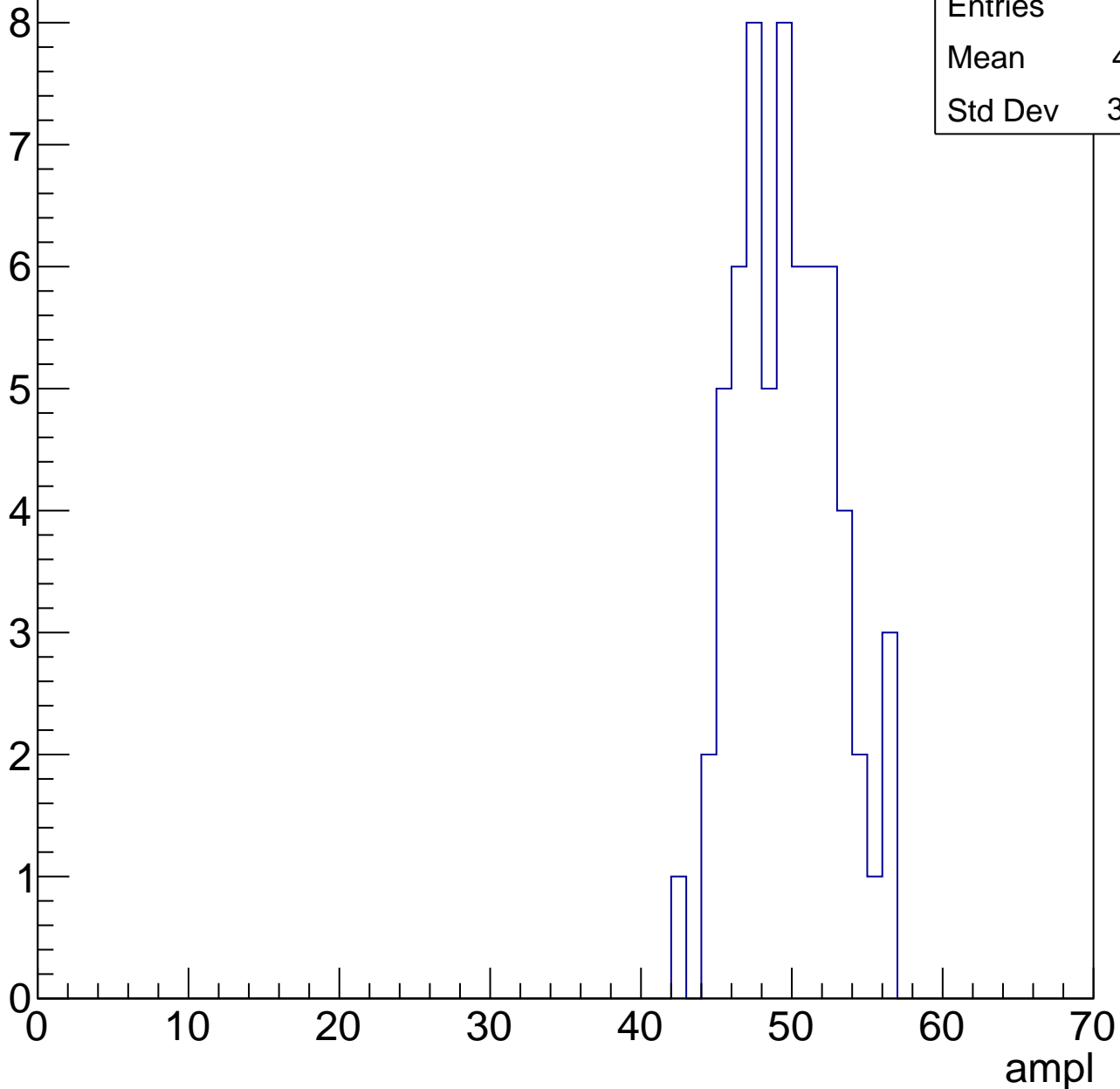


# B1L003S, U11-ch110, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

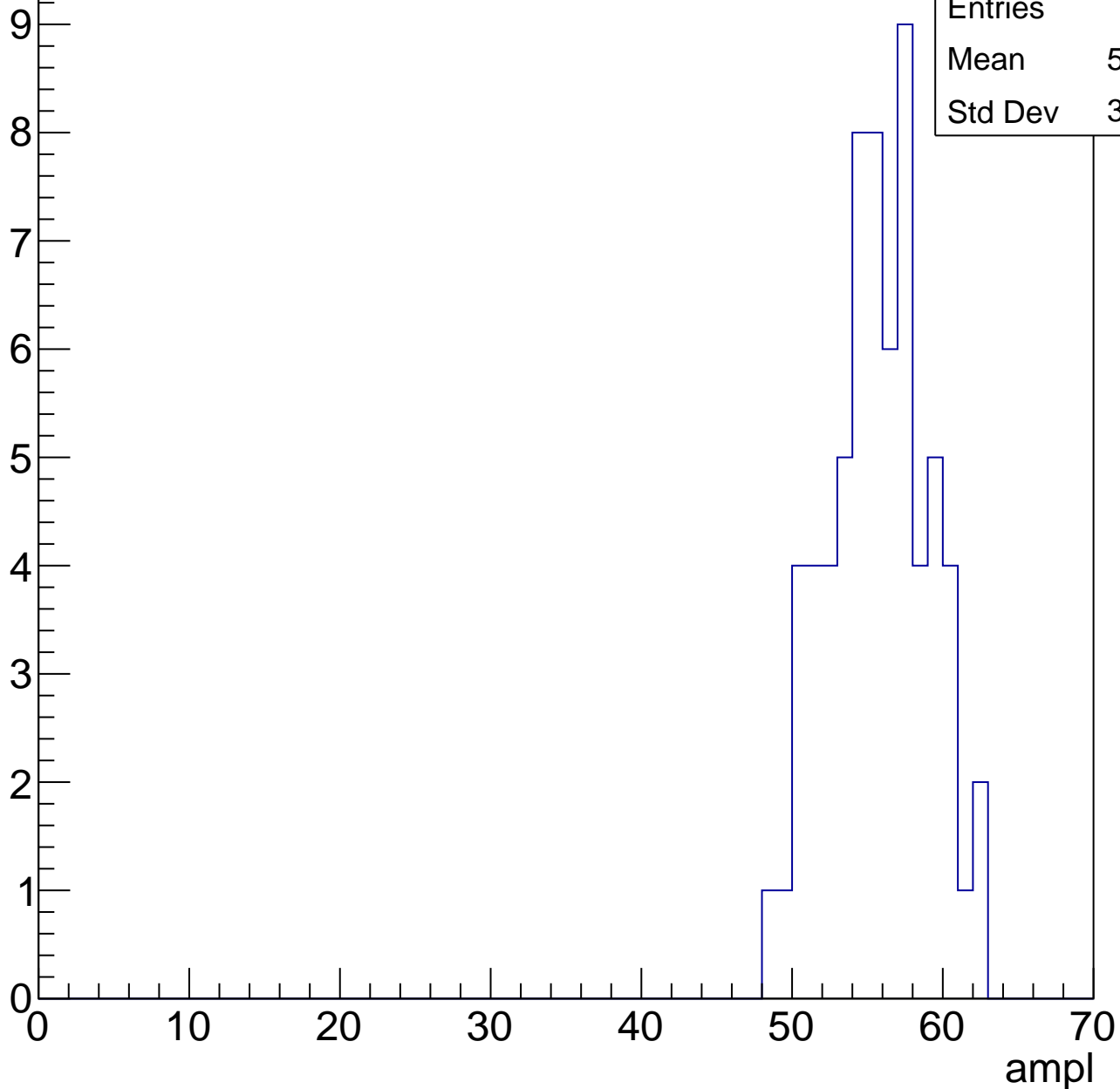
Entries	63
Mean	49.21
Std Dev	3.208



# B1L003S, U11-ch110, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

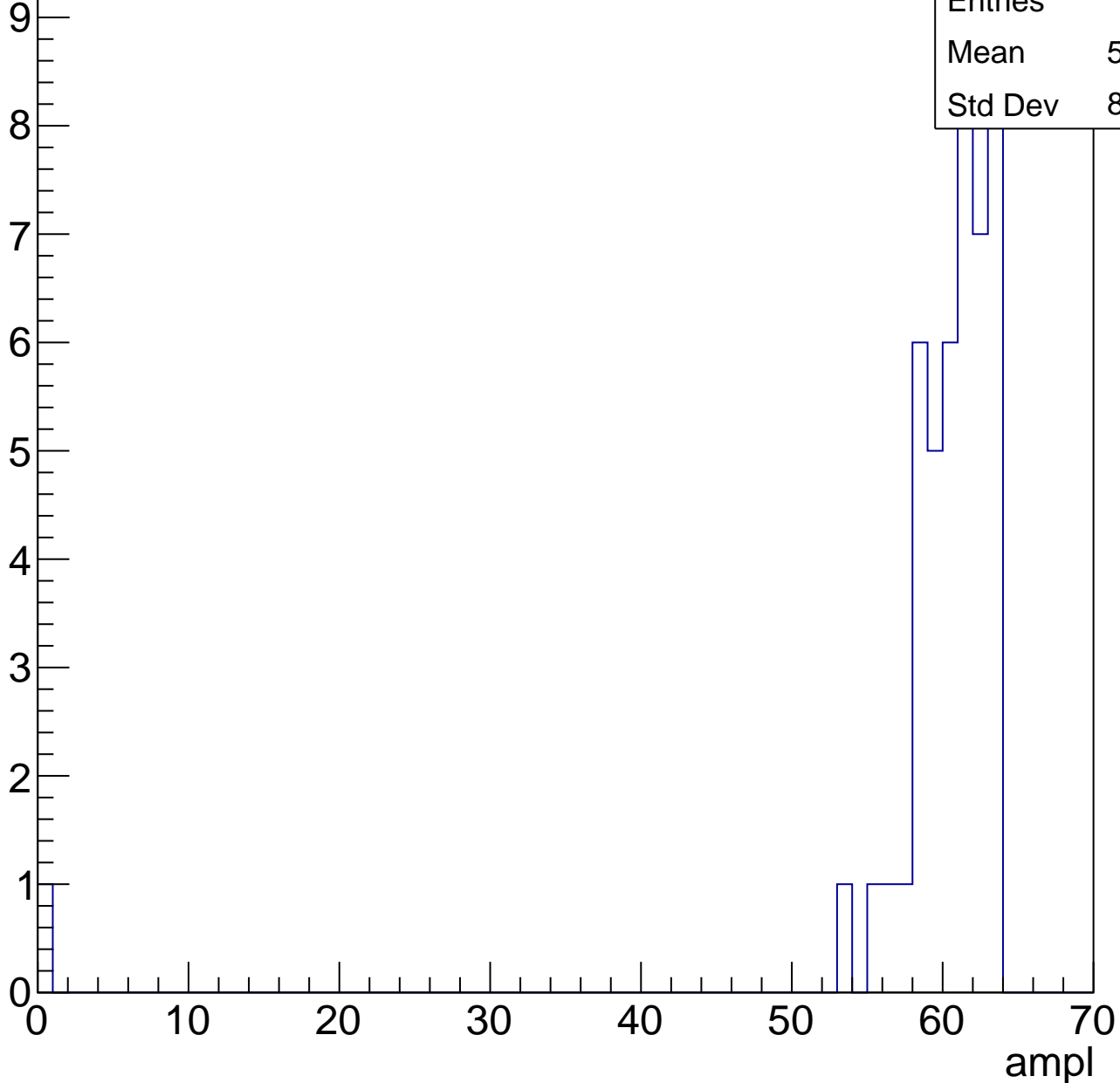


# B1L003S, U11-ch110, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

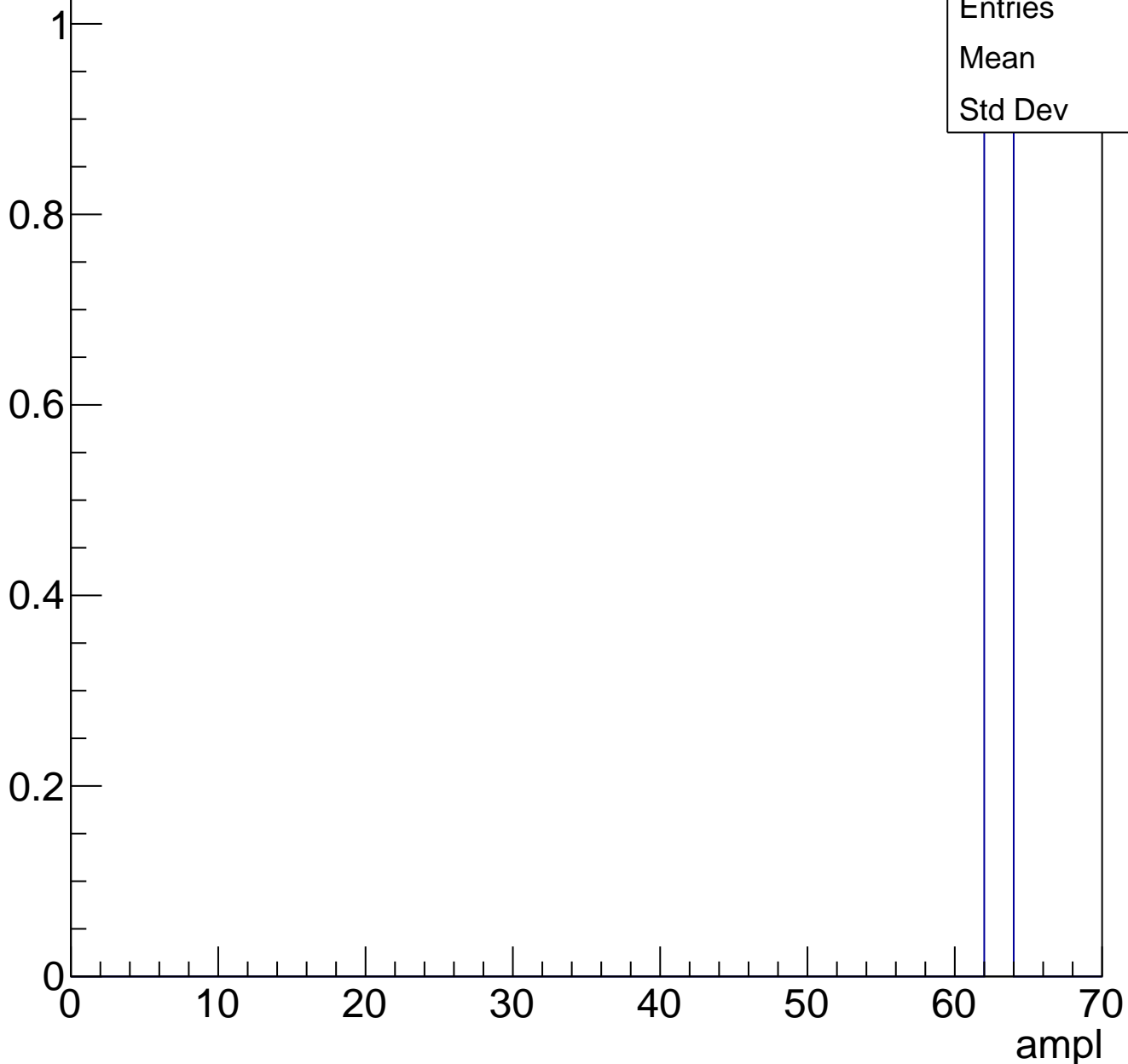
Entries	47
Mean	59.02
Std Dev	8.993



# B1L003S, U11-ch110, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

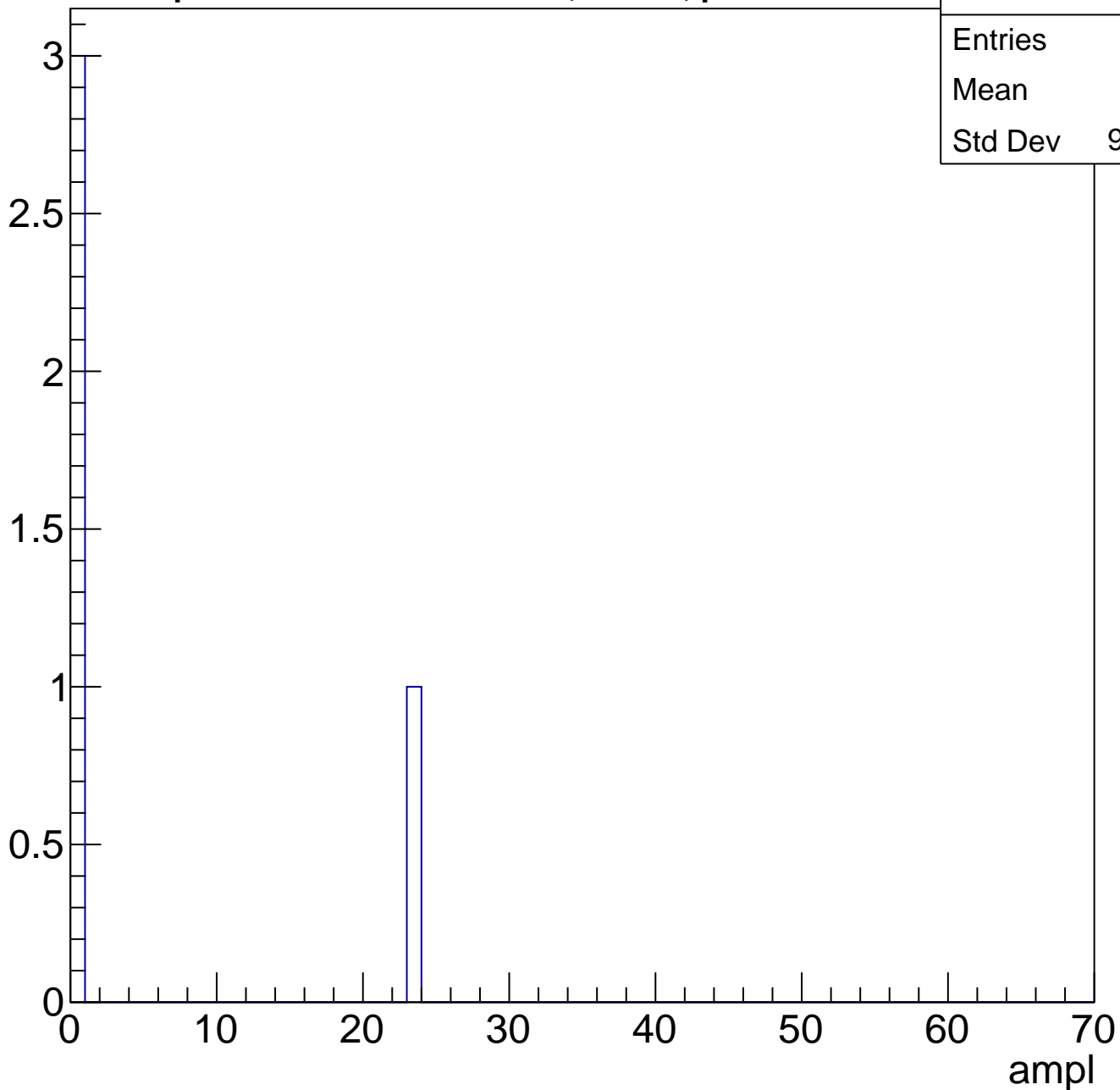




# B1L003S, U11-ch110, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U11-ch111, adc0

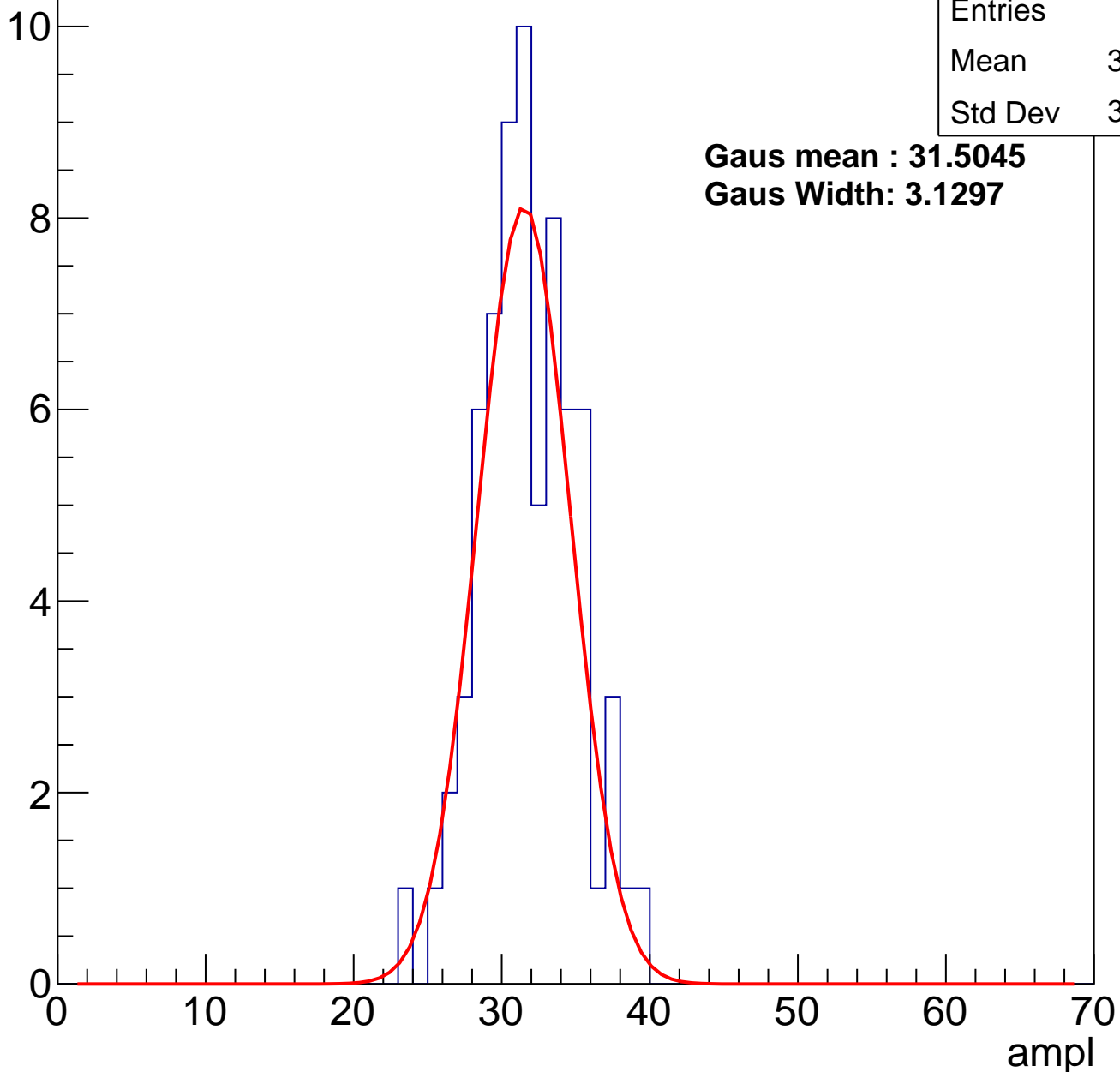
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	70
Mean	31.34
Std Dev	3.193

**Gaus mean : 31.5045**

**Gaus Width: 3.1297**

Entry



# B1L003S, U11-ch111, adc1

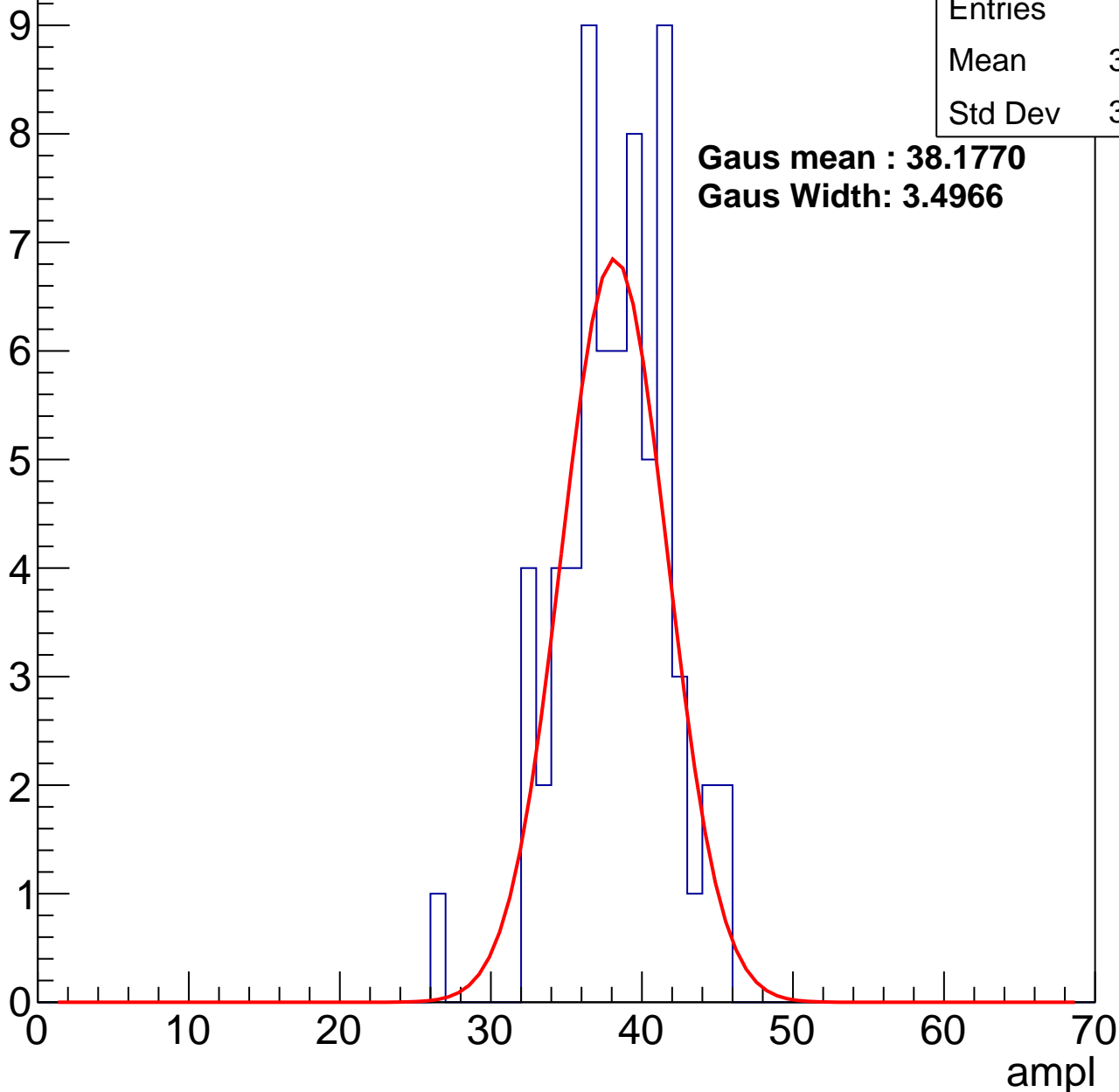
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	37.85
Std Dev	3.547

**Gaus mean : 38.1770**

**Gaus Width: 3.4966**



# B1L003S, U11-ch111, adc2

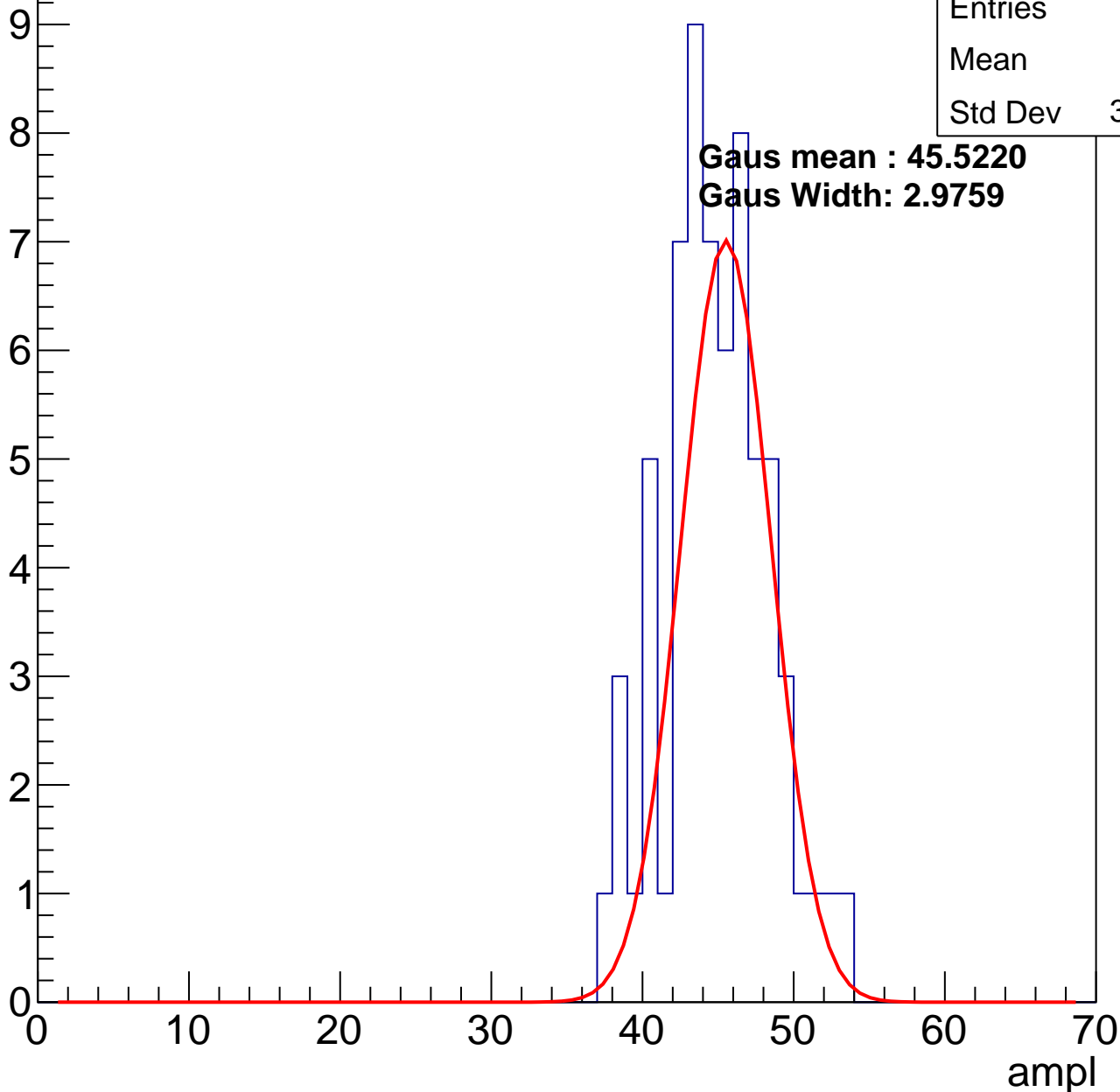
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	44.4
Std Dev	3.432

**Gaus mean : 45.5220**

**Gaus Width: 2.9759**

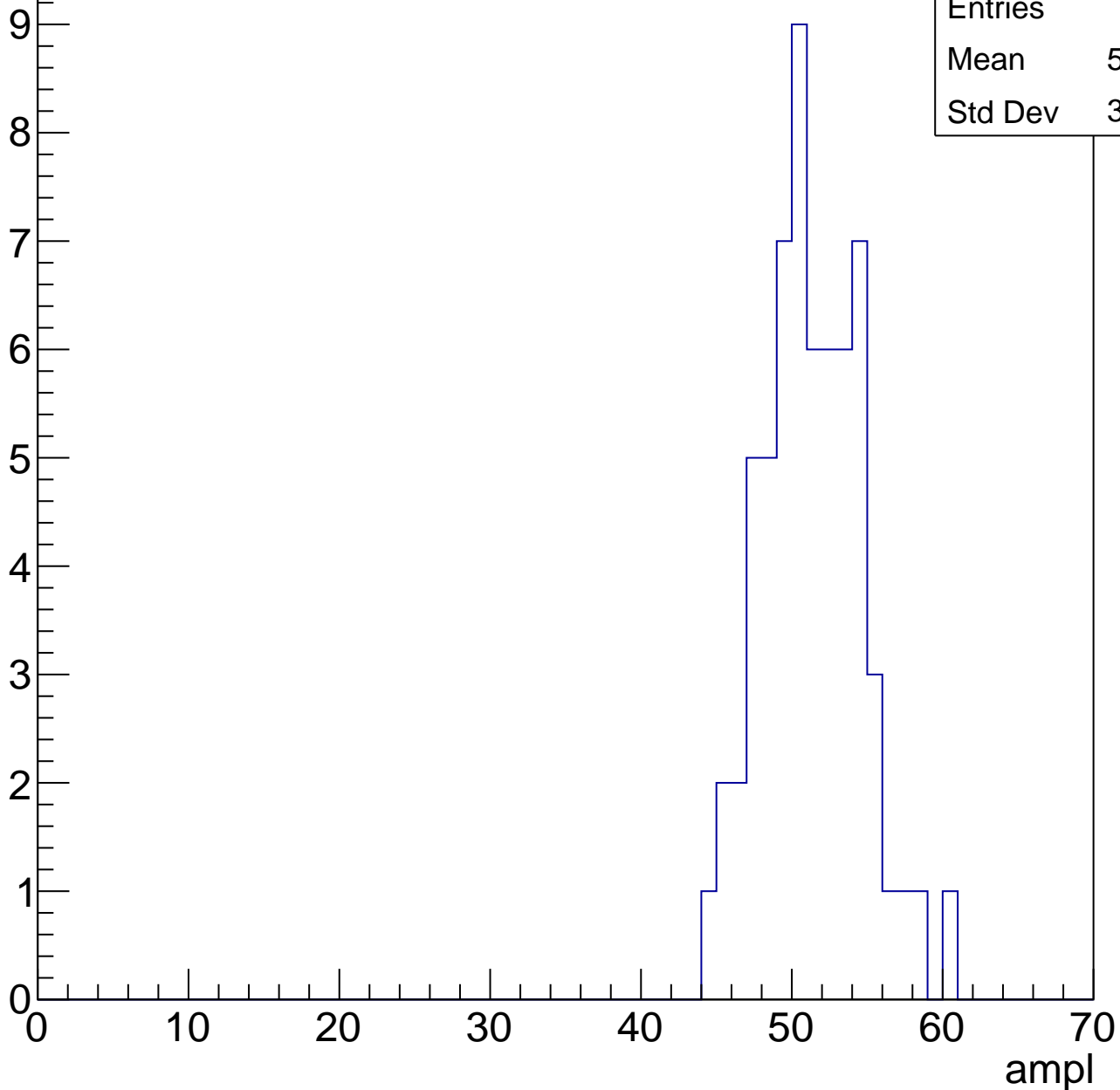


# B1L003S, U11-ch111, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

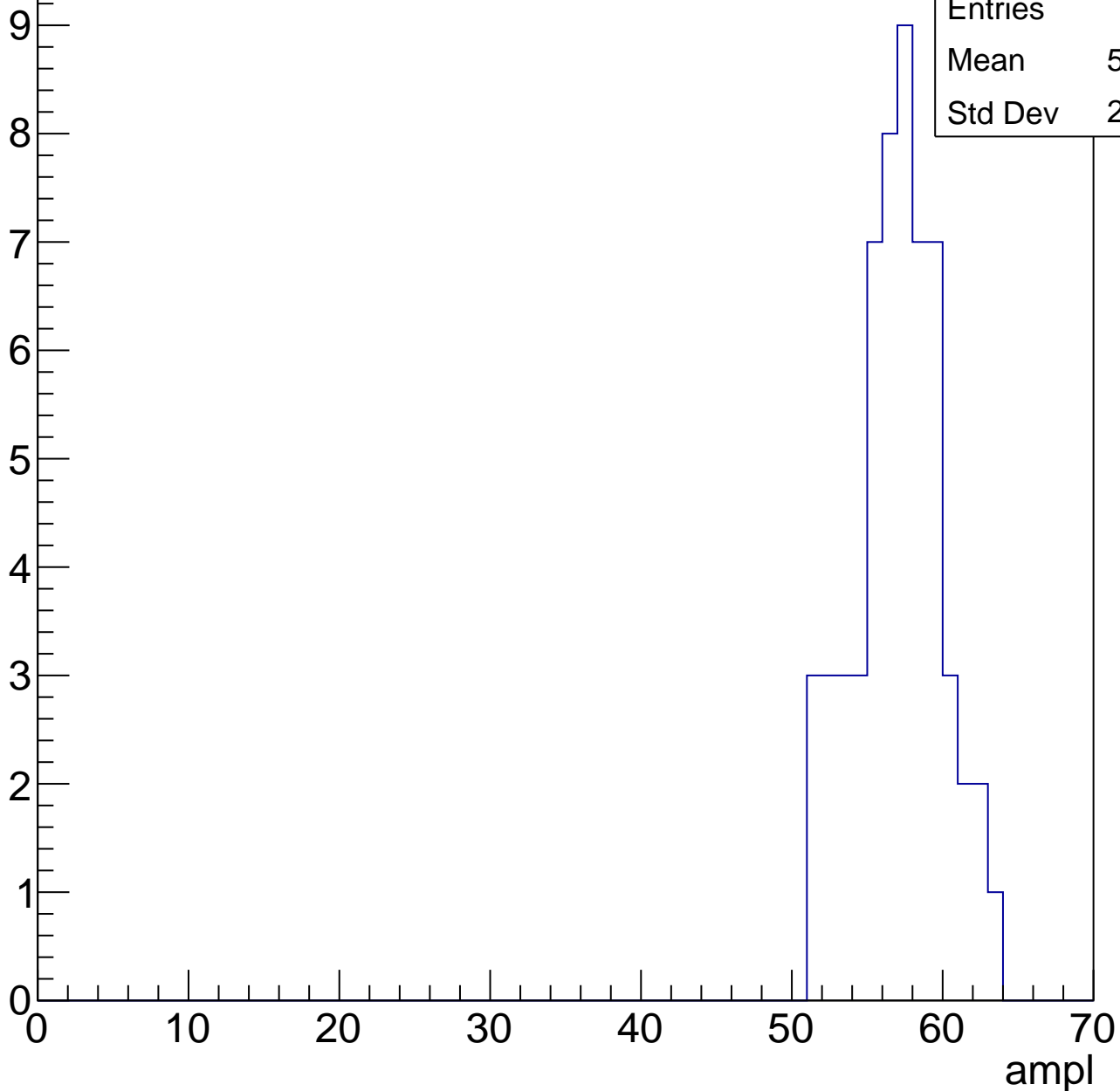
Entries	63
Mean	50.86
Std Dev	3.246



# B1L003S, U11-ch111, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



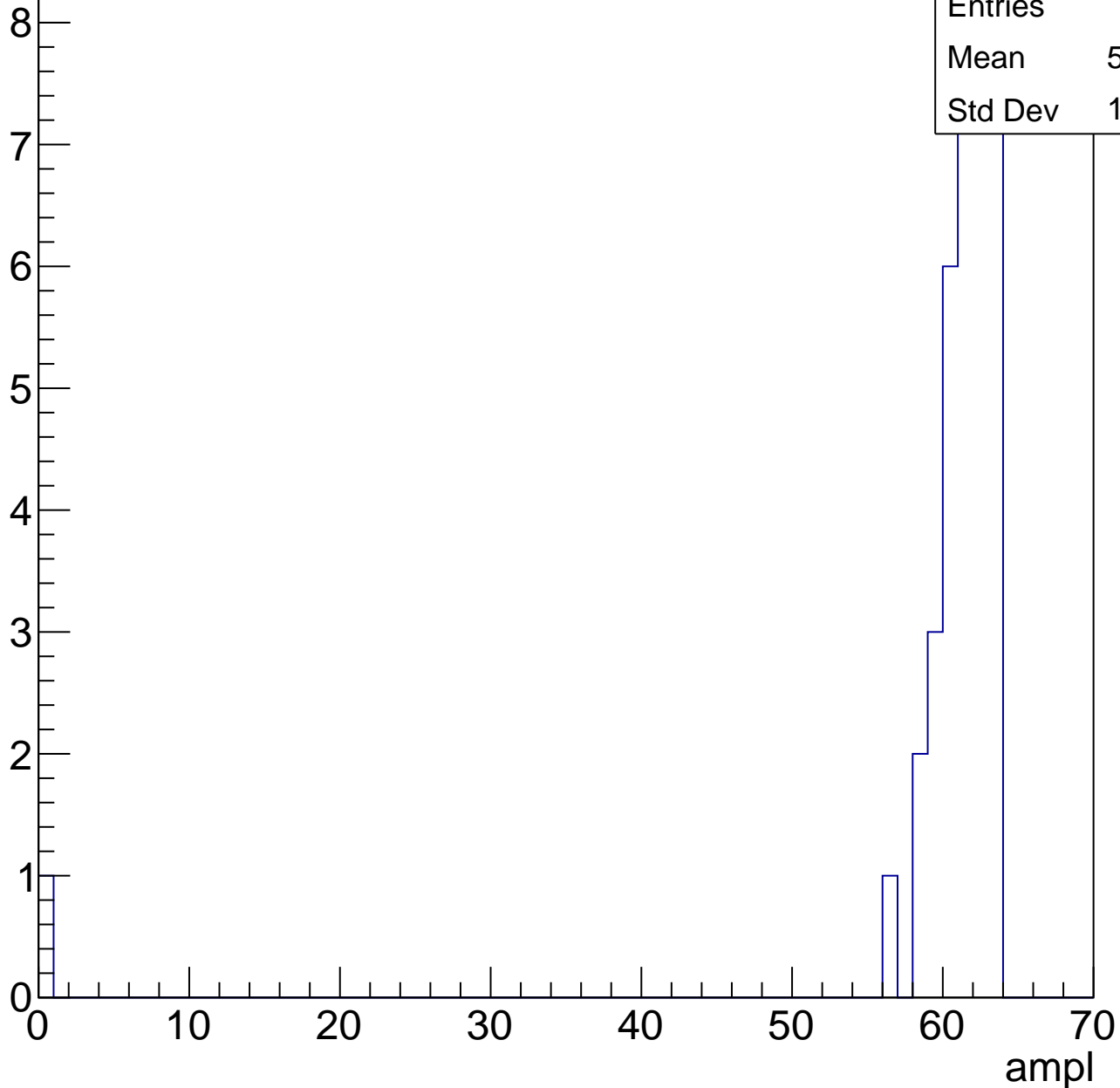
Entries	58
Mean	56.62
Std Dev	2.833

# B1L003S, U11-ch111, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	37
Mean	59.38
Std Dev	10.03



# B1L003S, U11-ch111, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	63
Std Dev	0



# B1L003S, U11-ch111, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U11-ch112, adc0

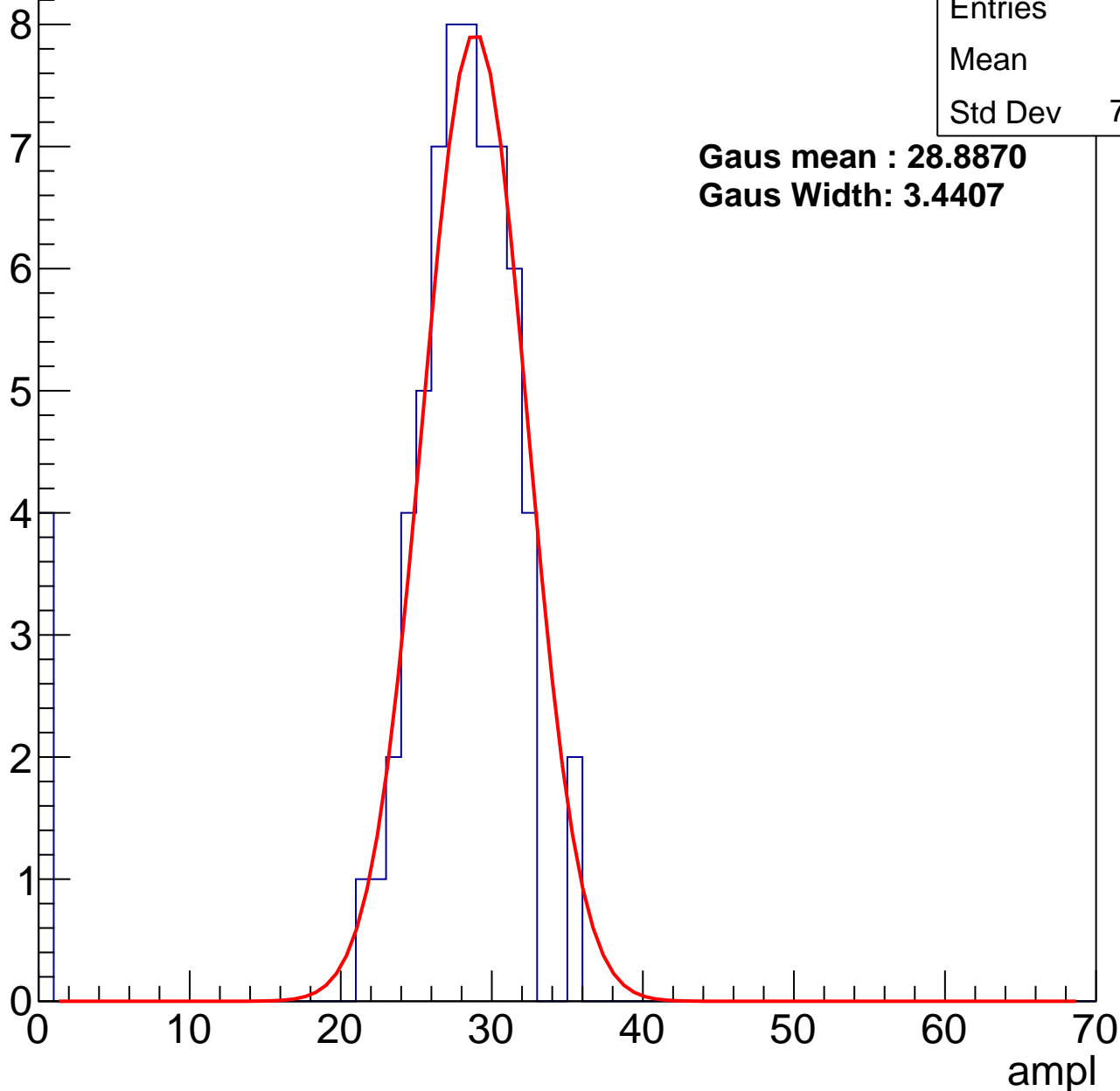
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	26.2
Std Dev	7.233

**Gaus mean : 28.8870**

**Gaus Width: 3.4407**



# B1L003S, U11-ch112, adc1

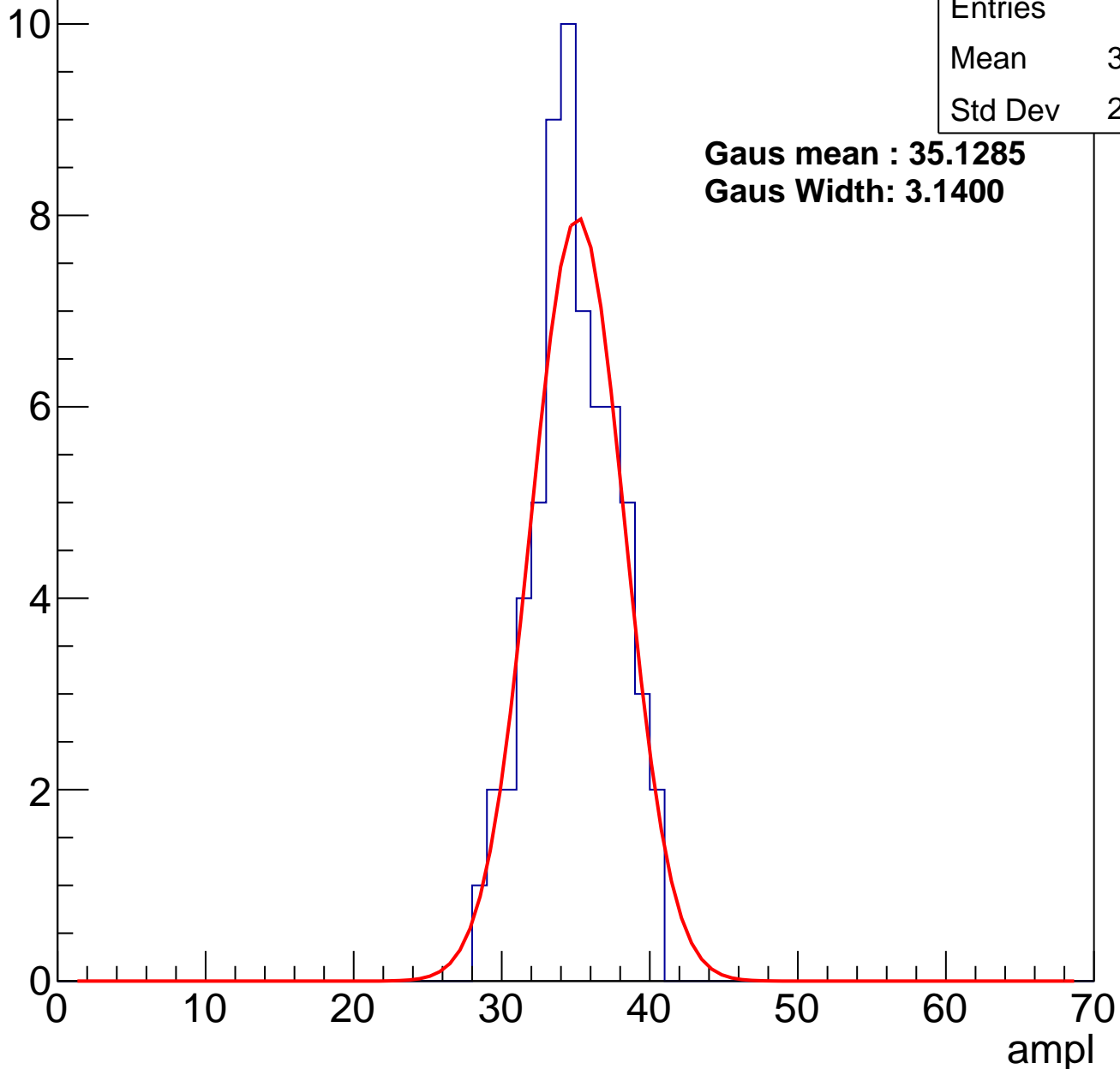
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	62
Mean	34.47
Std Dev	2.787

**Gaus mean : 35.1285**

**Gaus Width: 3.1400**

Entry



# B1L003S, U11-ch112, adc2

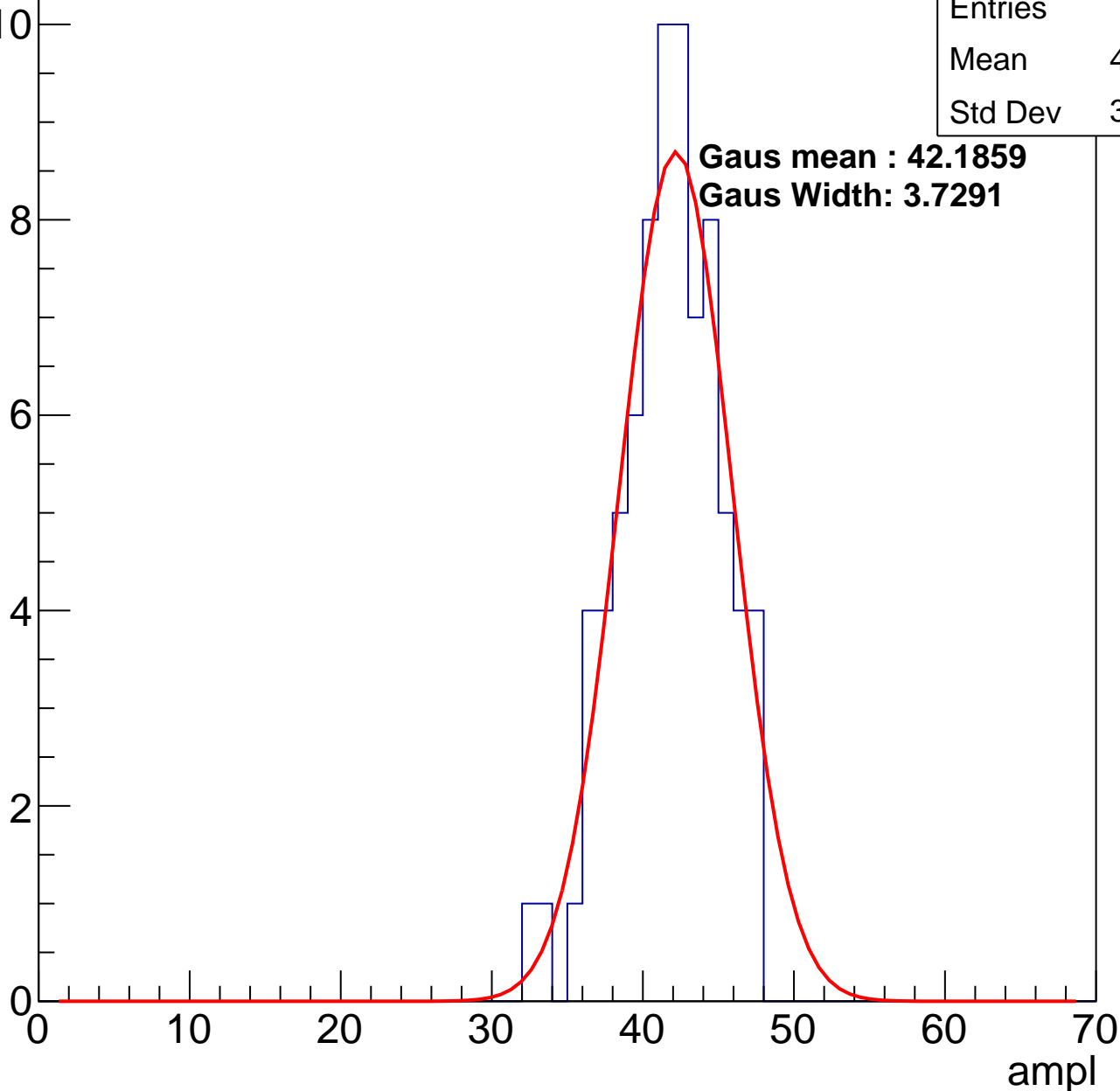
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	78
Mean	41.23
Std Dev	3.305

**Gaus mean : 42.1859**

**Gaus Width: 3.7291**

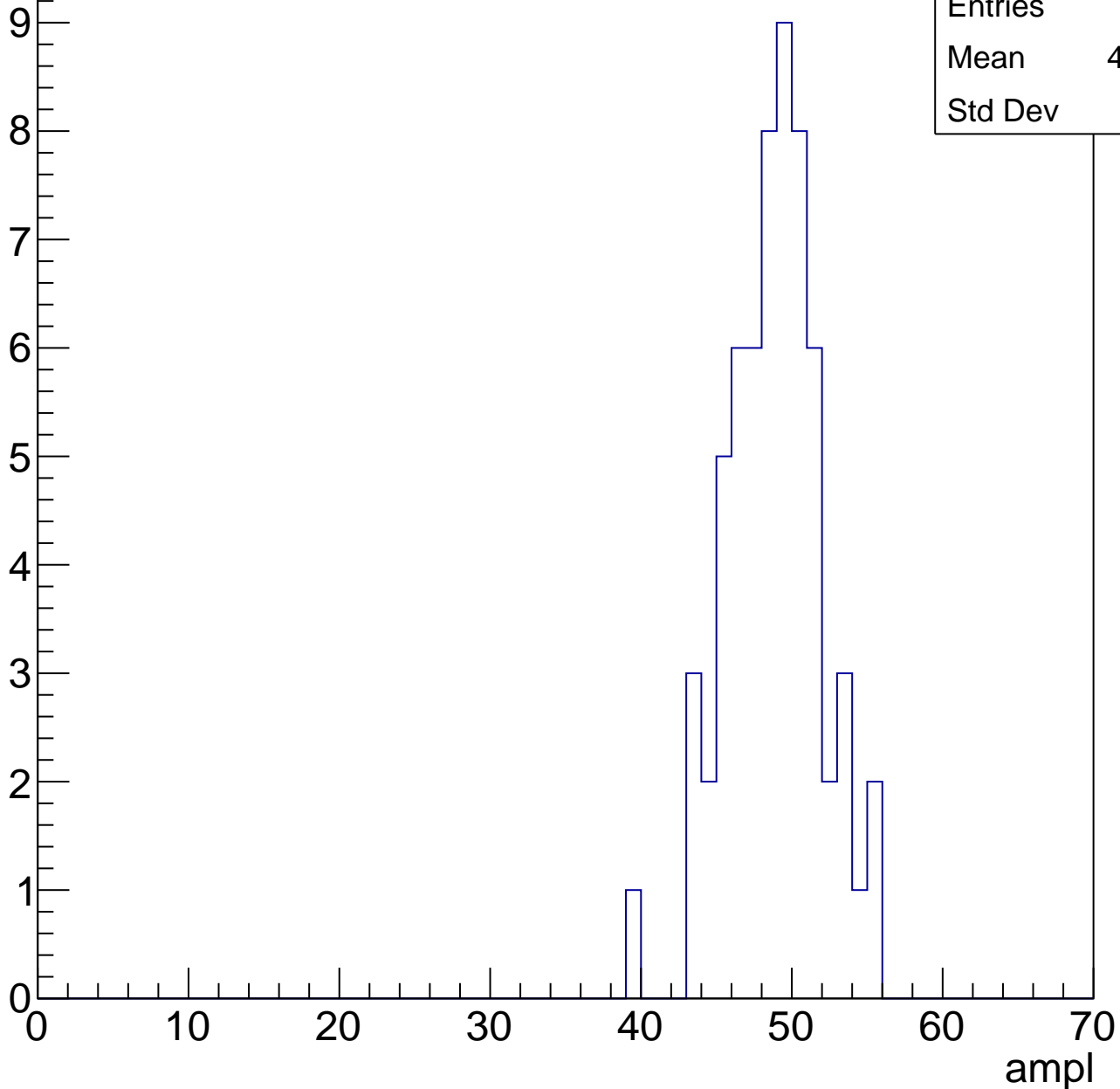


# B1L003S, U11-ch112, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	48.34
Std Dev	3.09

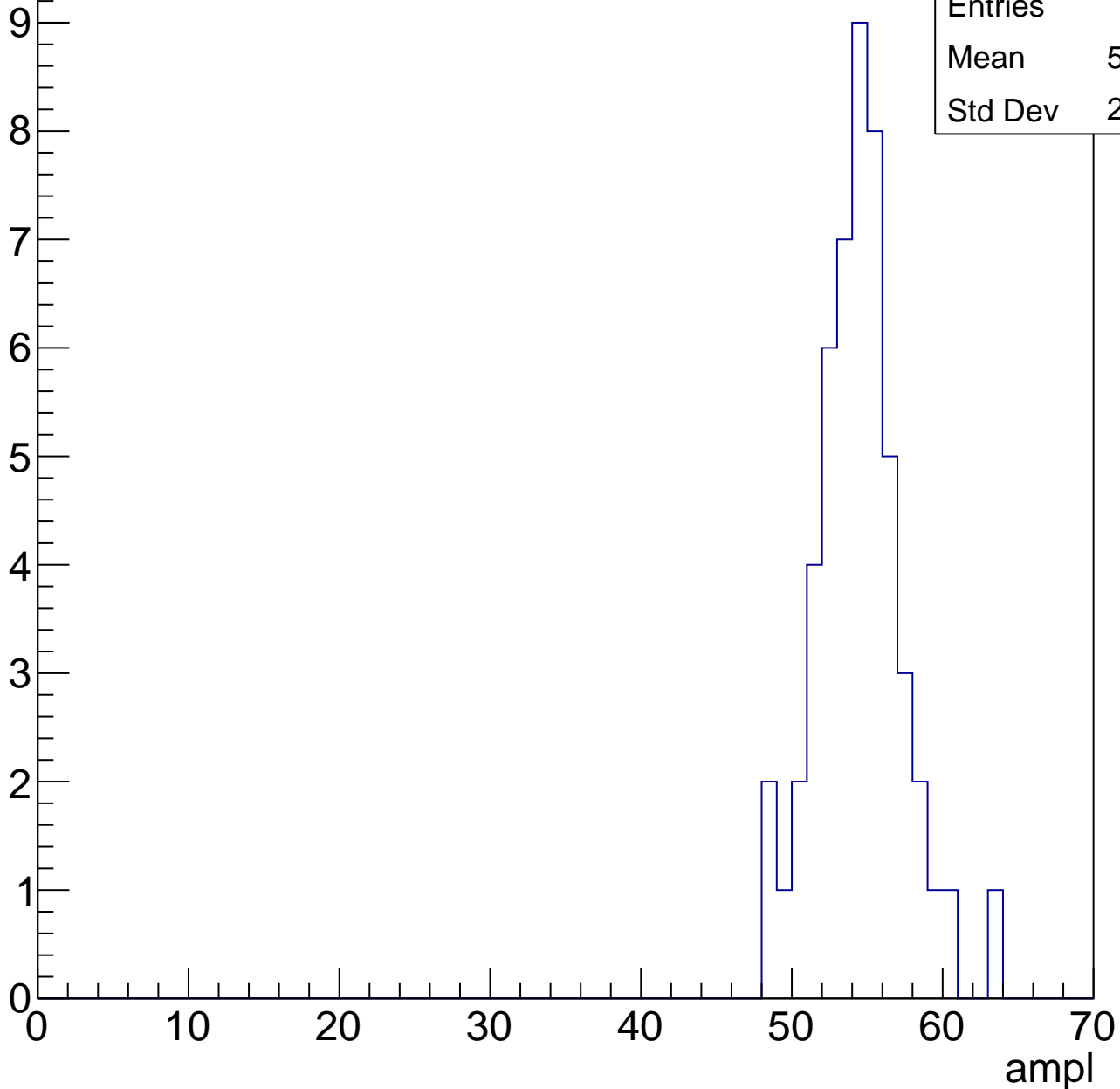


# B1L003S, U11-ch112, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	52
Mean	53.98
Std Dev	2.859

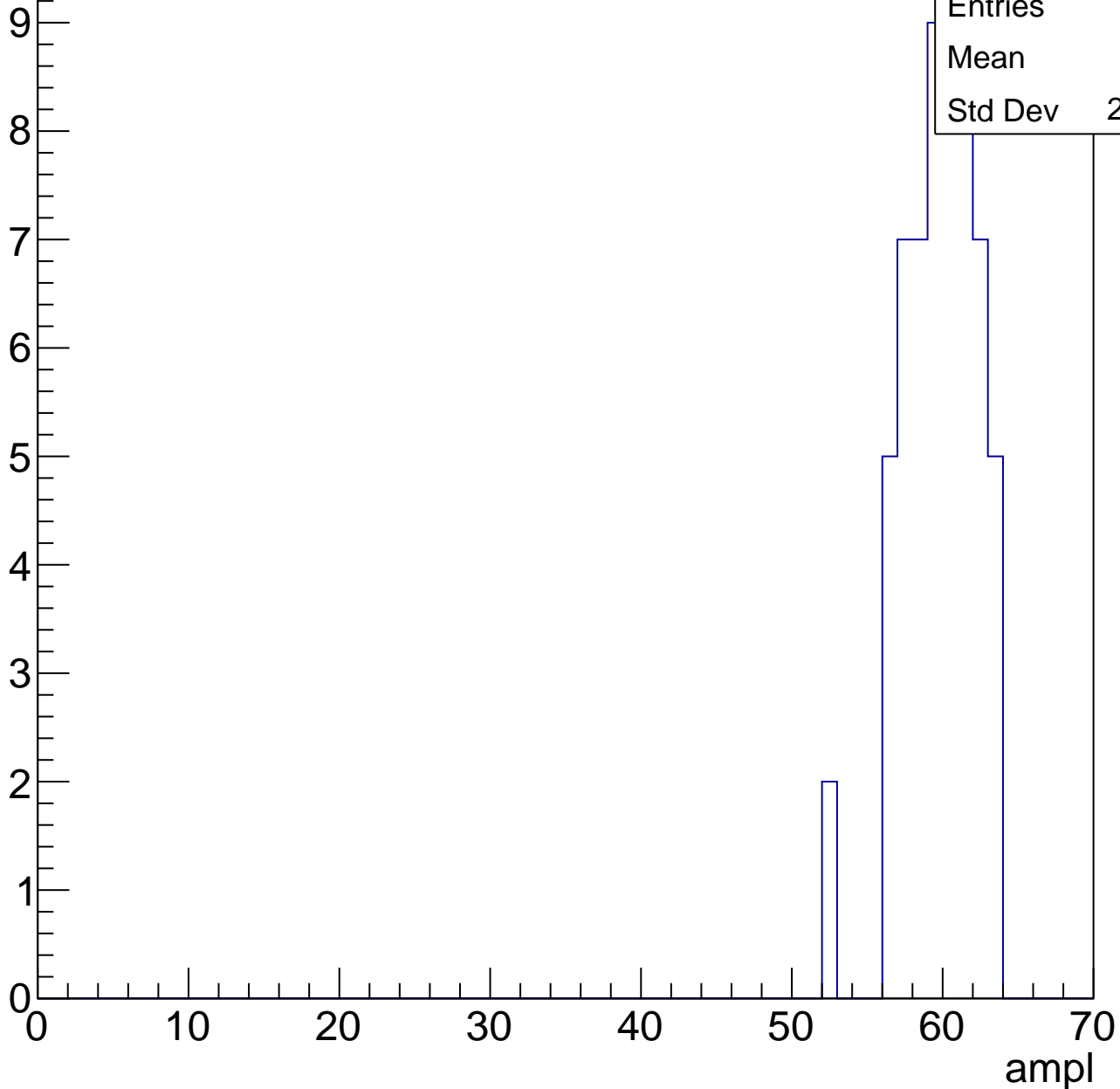


# B1L003S, U11-ch112, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

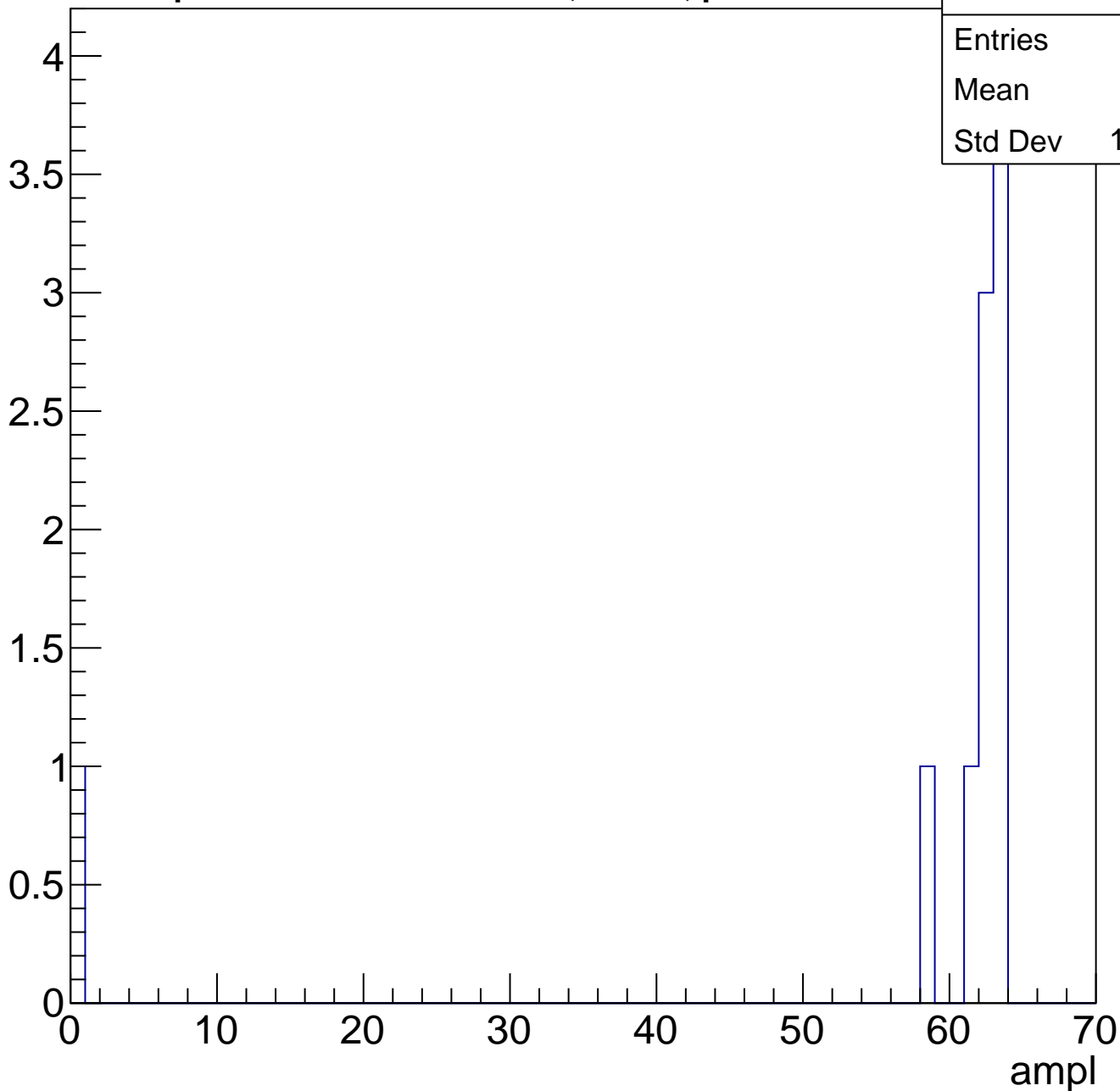
Entries	60
Mean	59.3
Std Dev	2.452



# B1L003S, U11-ch112, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

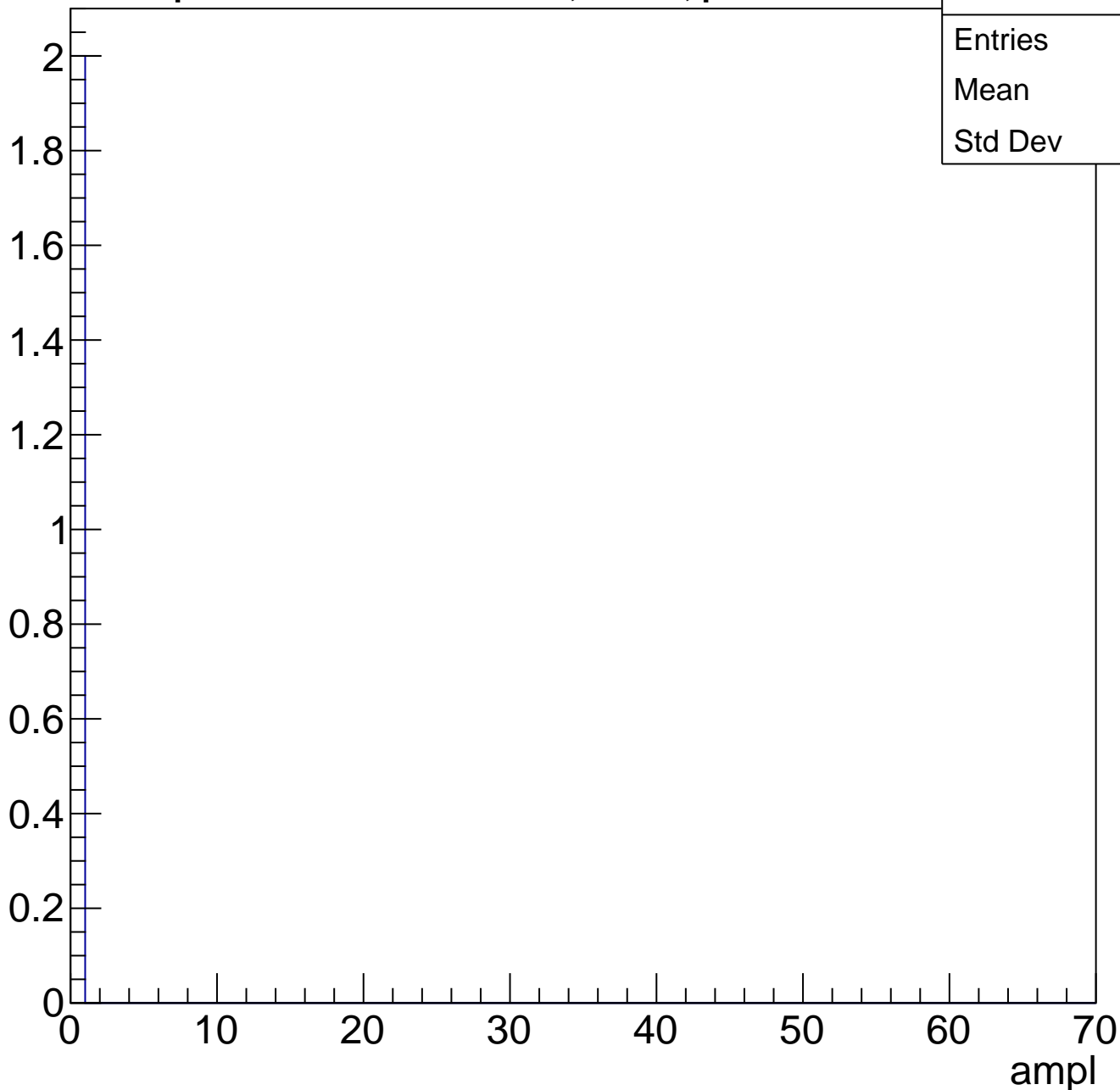




# B1L003S, U11-ch112, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U11-ch113, adc0

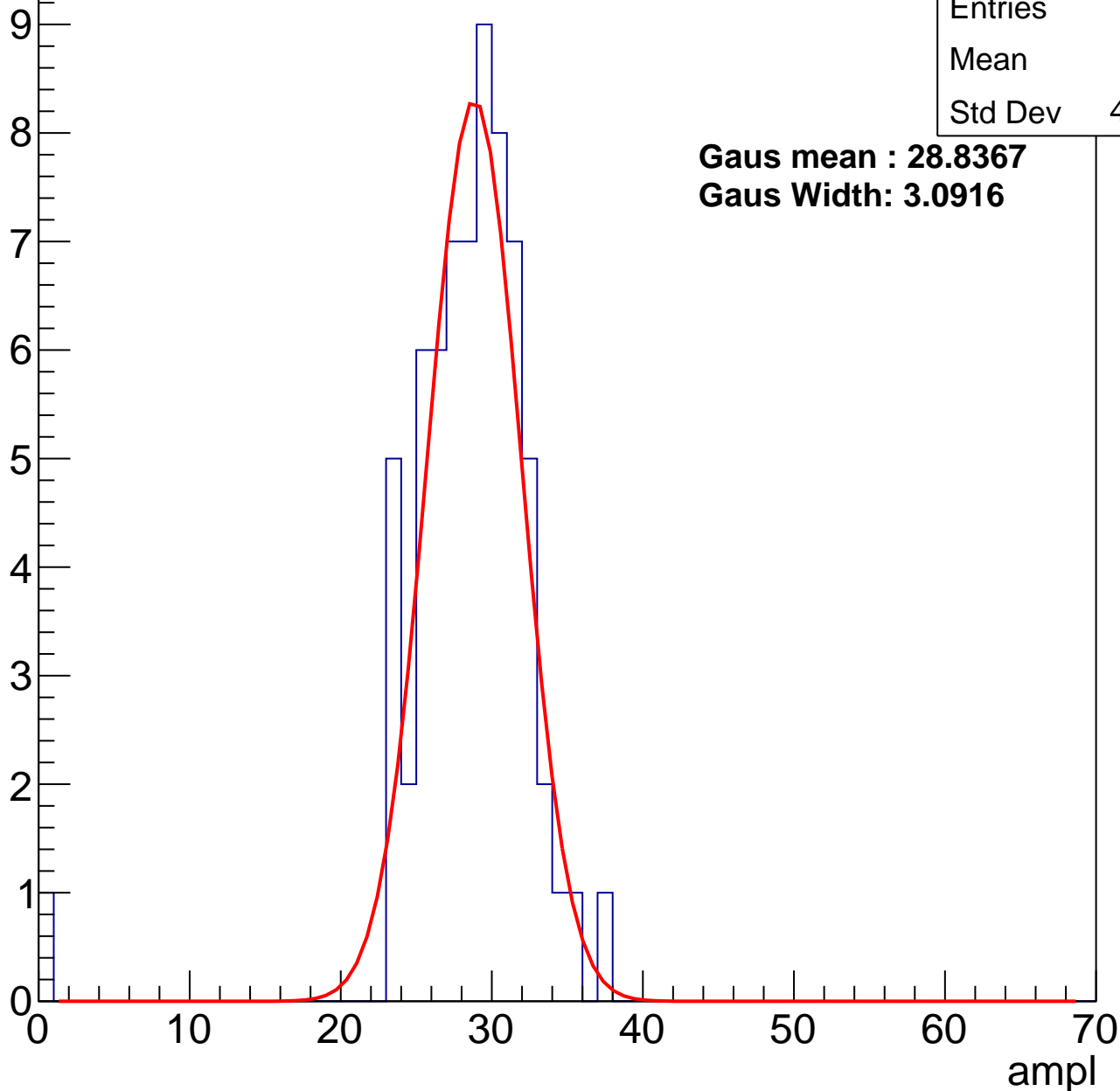
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	28
Std Dev	4.579

**Gaus mean : 28.8367**

**Gaus Width: 3.0916**



# B1L003S, U11-ch113, adc1

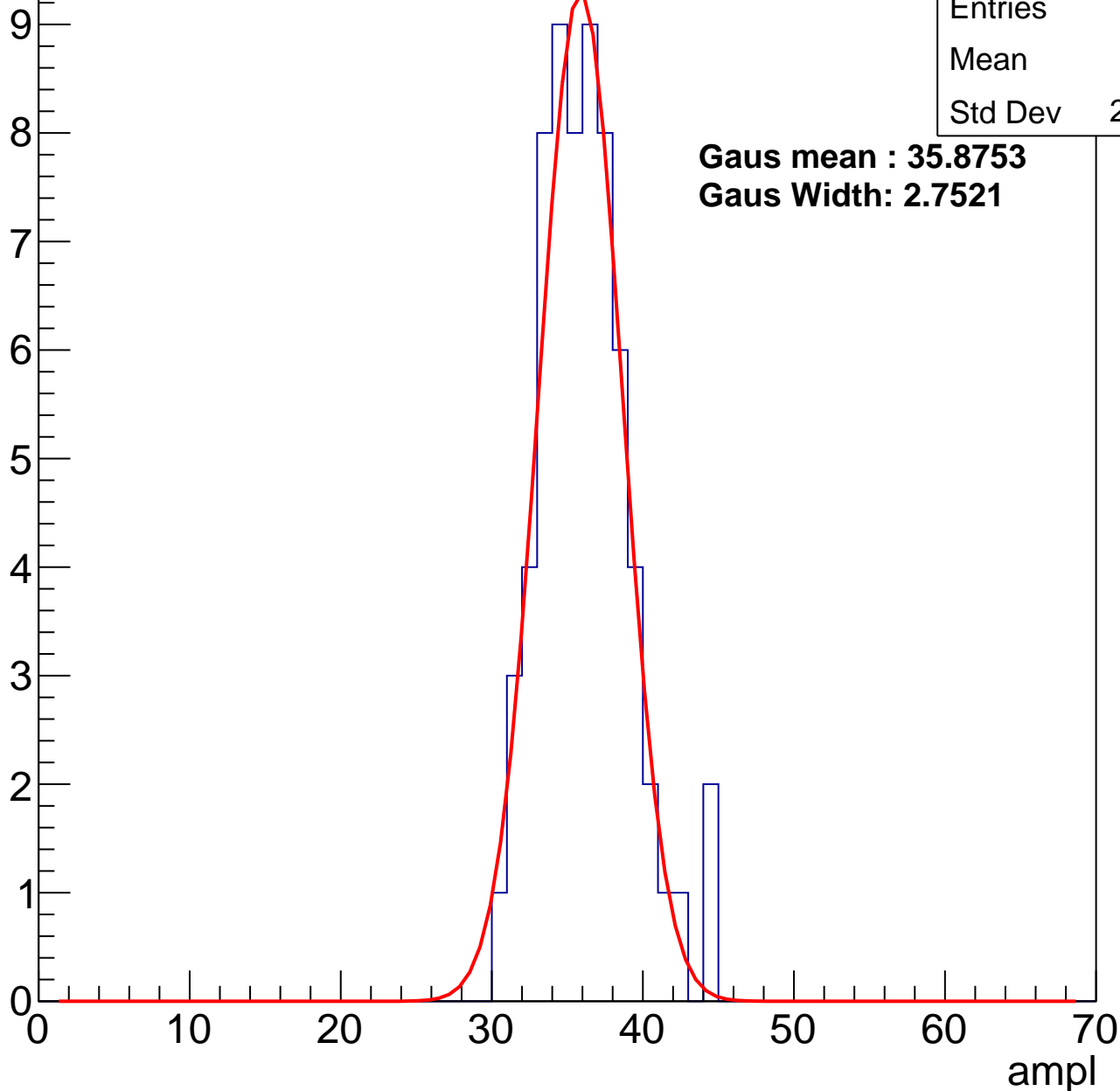
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	35.7
Std Dev	2.949

**Gaus mean : 35.8753**

**Gaus Width: 2.7521**



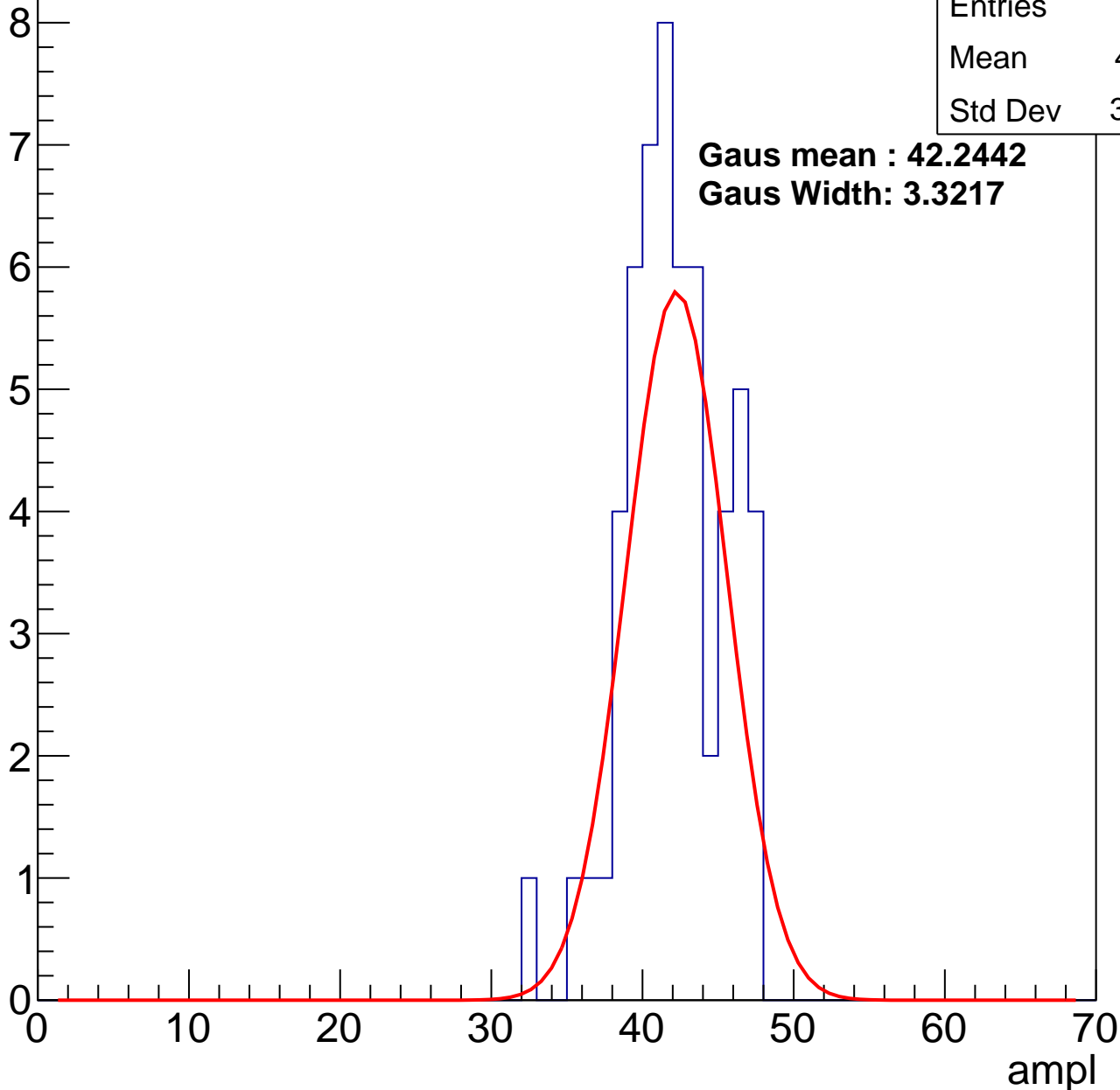
# B1L003S, U11-ch113, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	41.61
Std Dev	3.233

**Gaus mean : 42.2442**  
**Gaus Width: 3.3217**



# B1L003S, U11-ch113, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	84
Mean	48.23
Std Dev	3.476

Entry

10

8

6

4

2

0

0

10

20

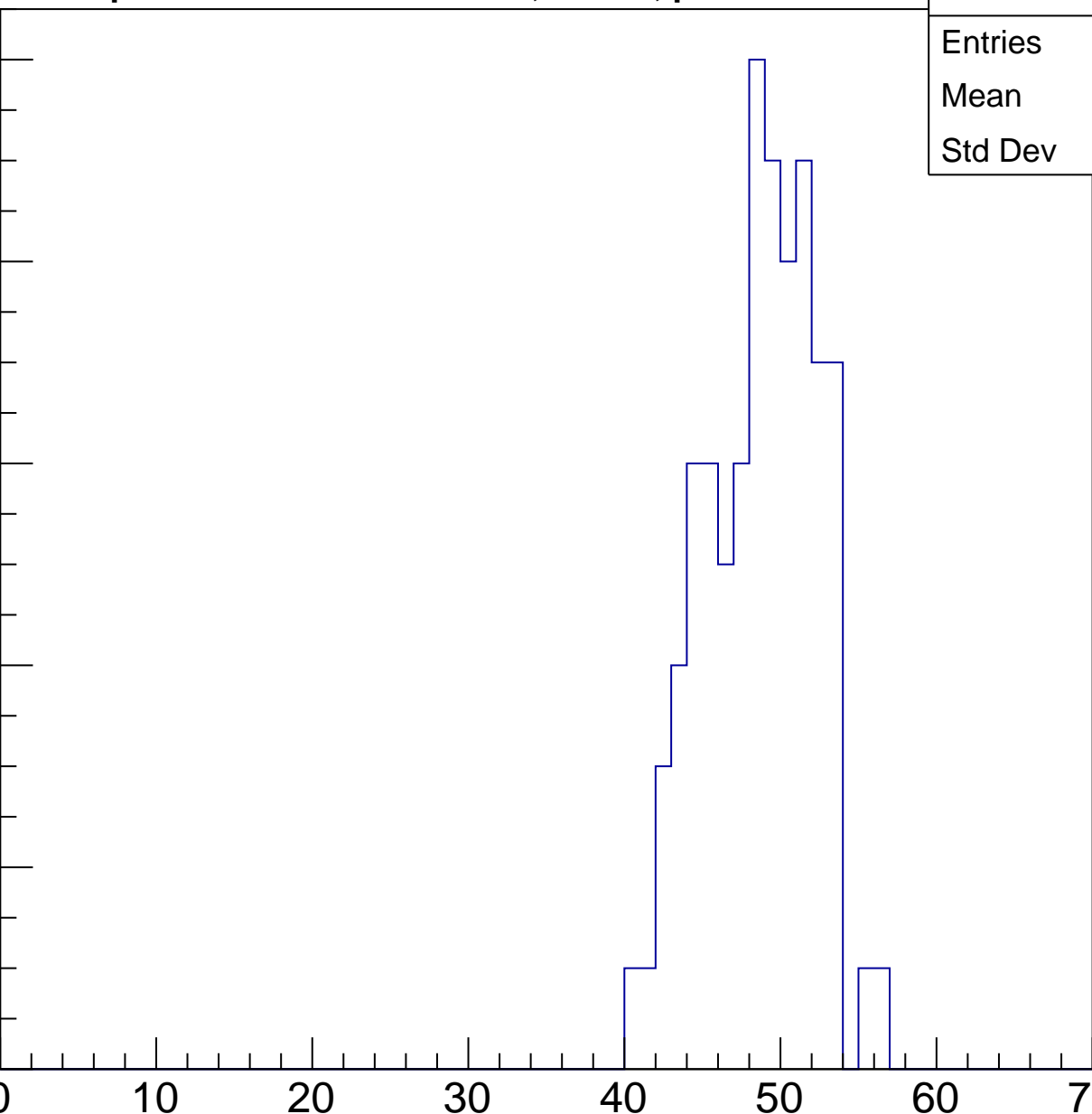
30

40

50

60

ampl

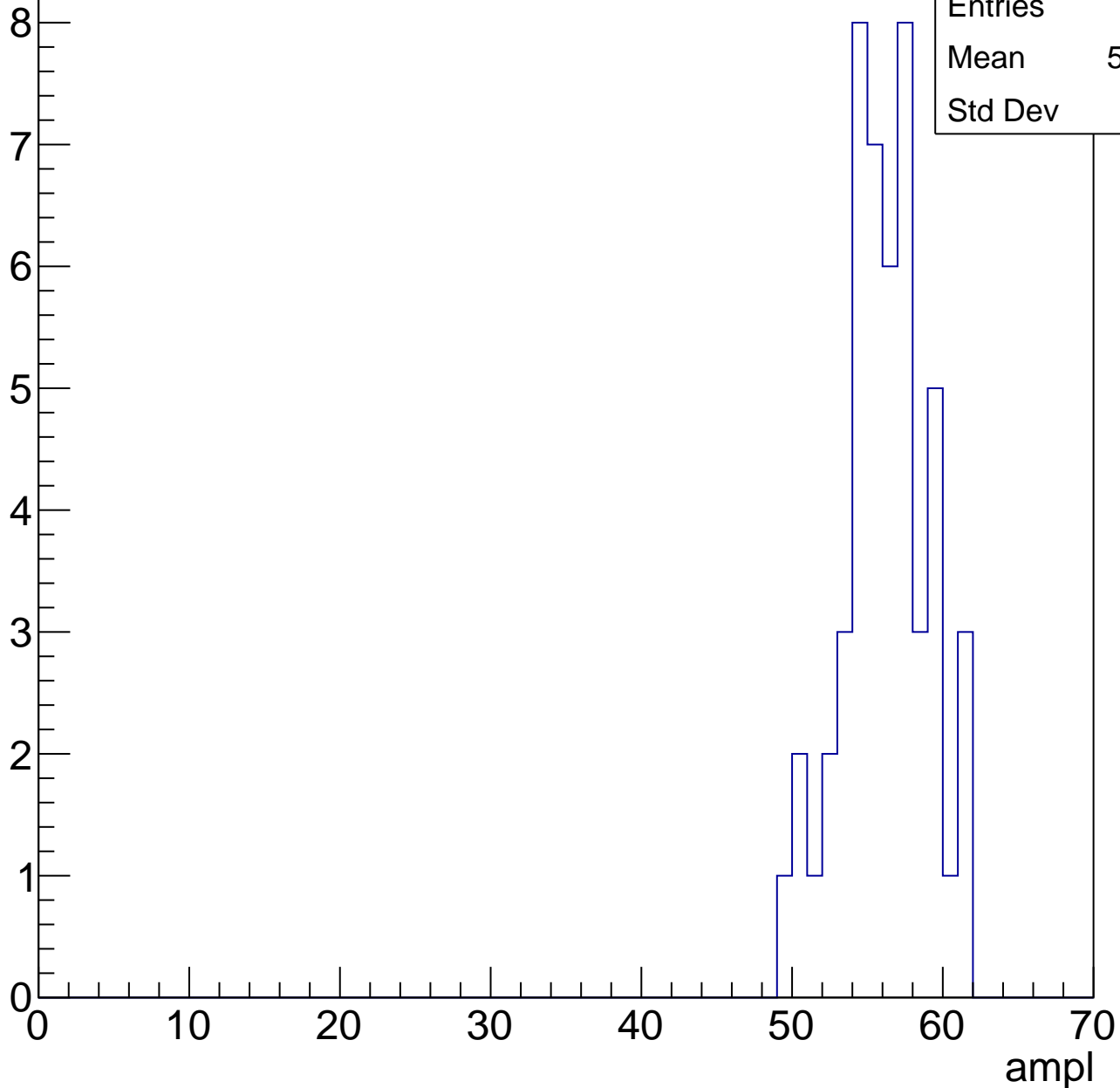


# B1L003S, U11-ch113, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

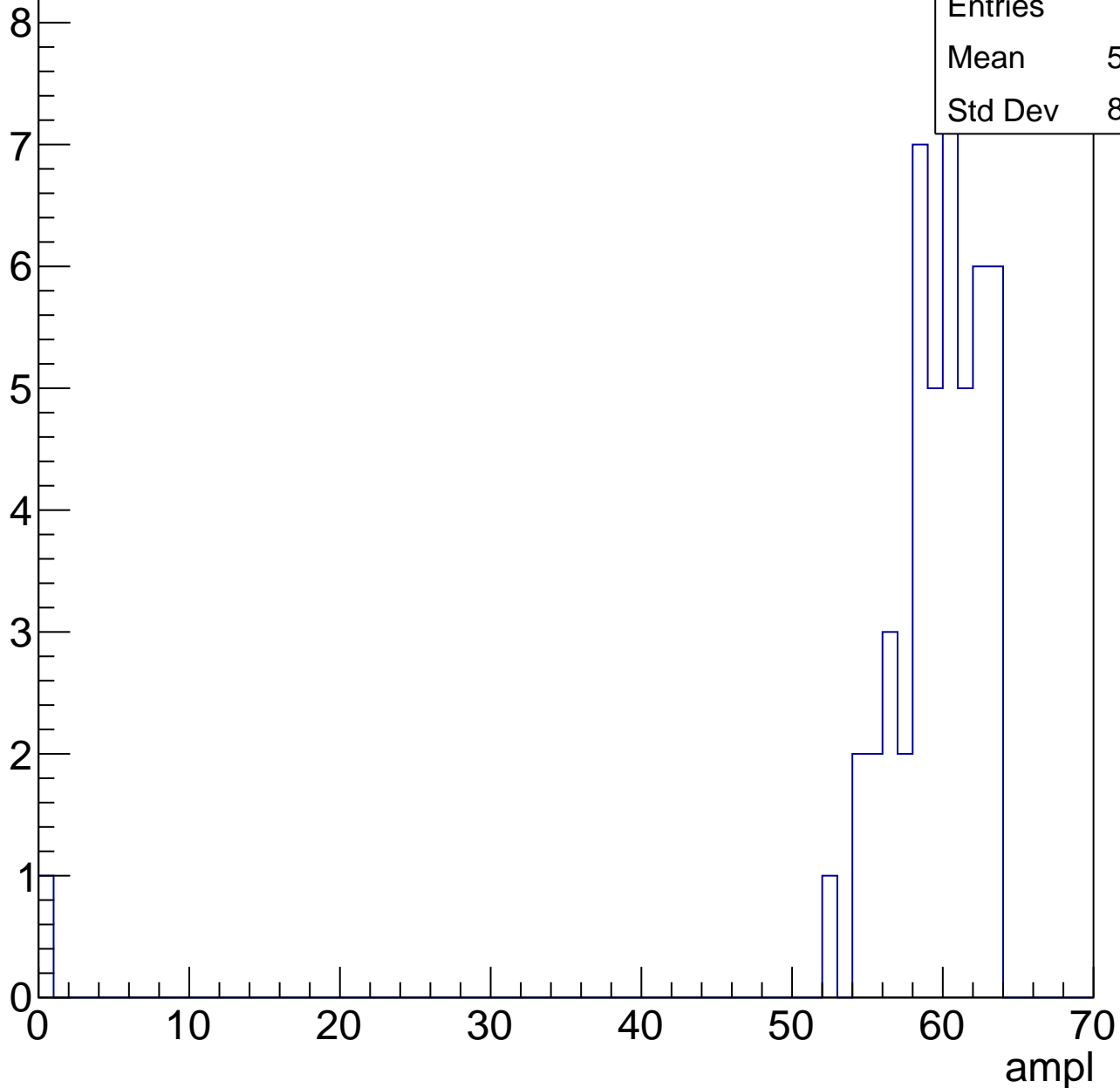
Entries	50
Mean	55.68
Std Dev	2.81



# B1L003S, U11-ch113, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

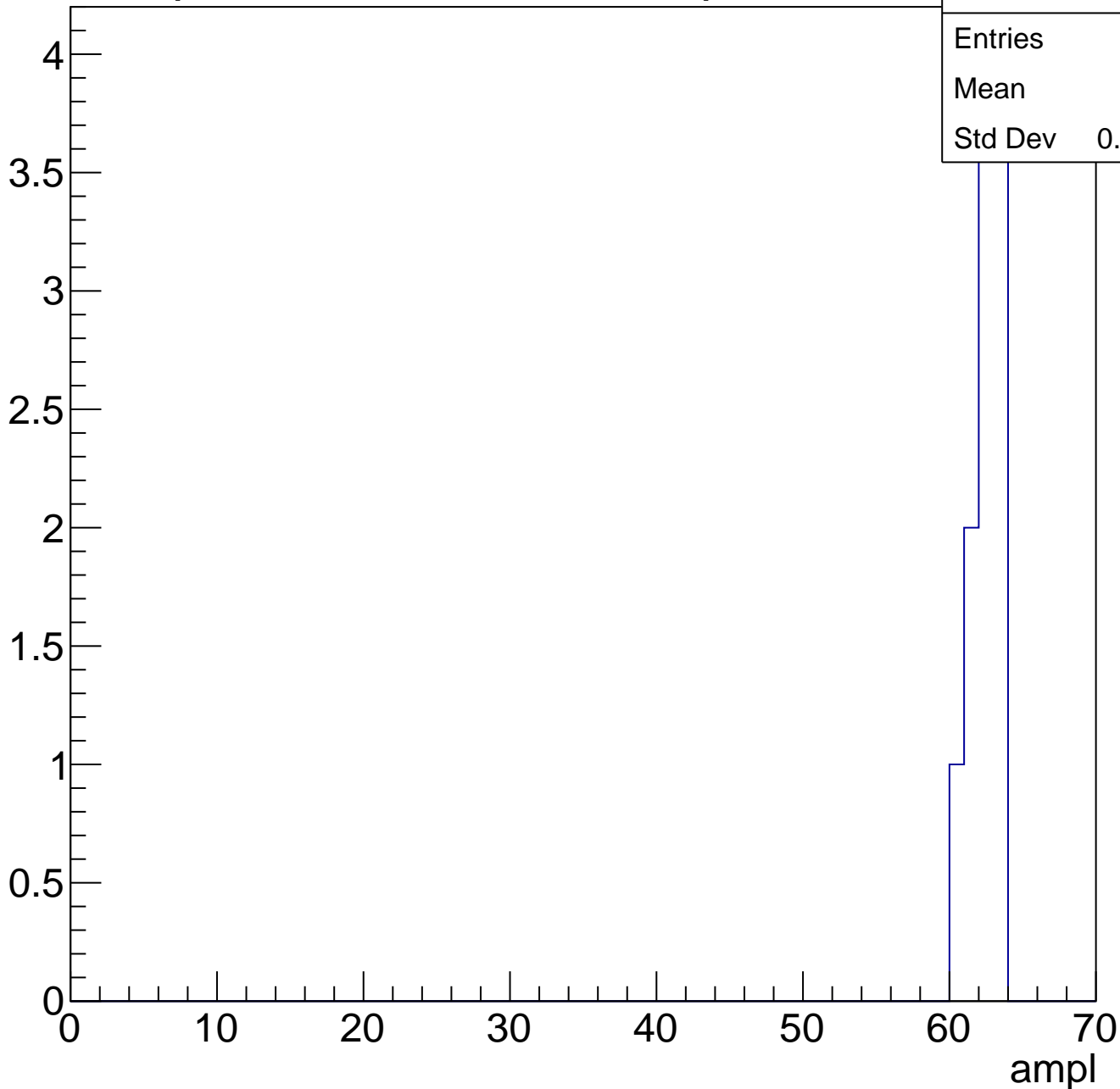
Entry



# B1L003S, U11-ch113, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



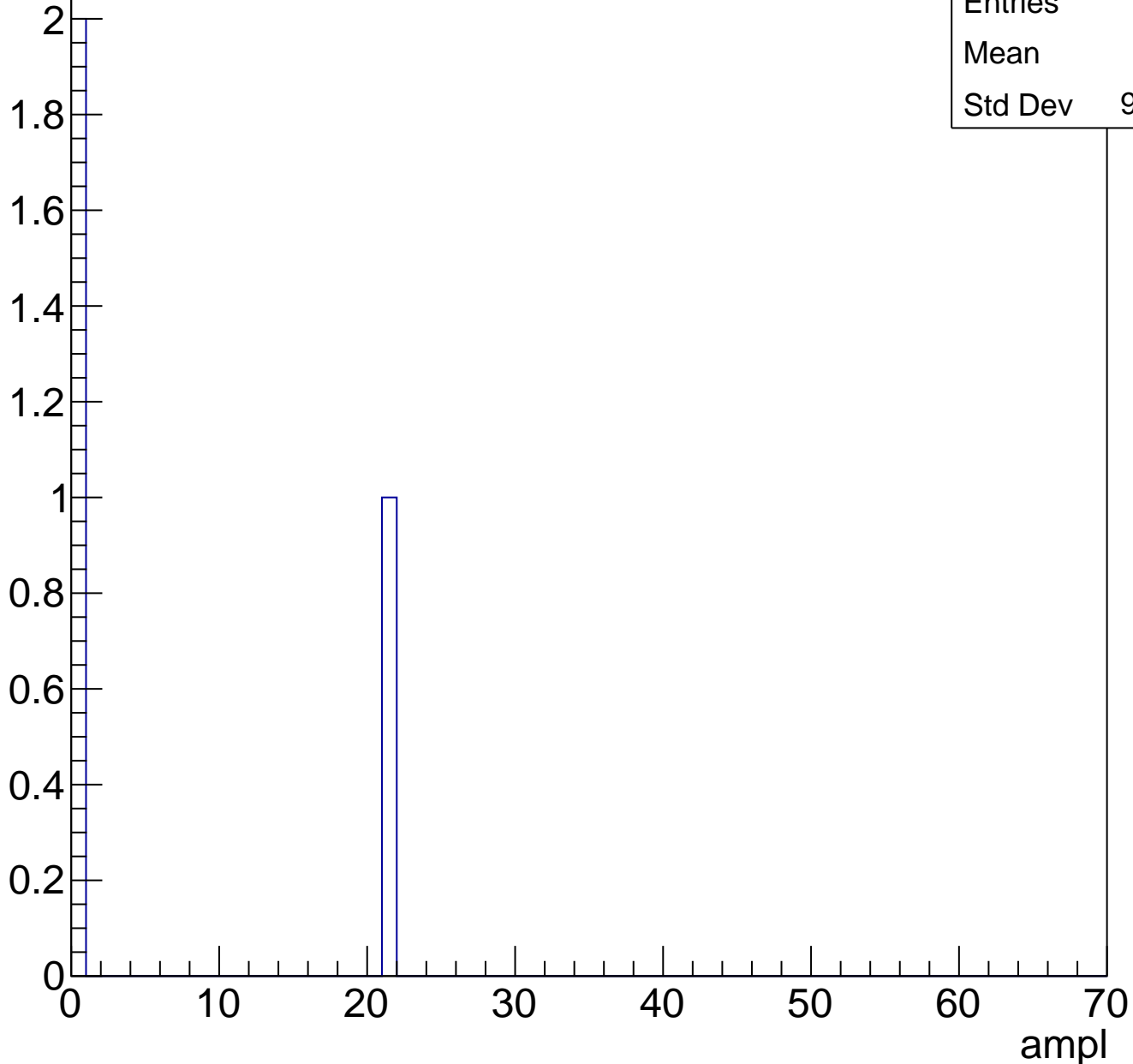
Entries	11
Mean	62
Std Dev	0.9535



# B1L003S, U11-ch113, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U11-ch114, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	56
Mean	29.2
Std Dev	2.58

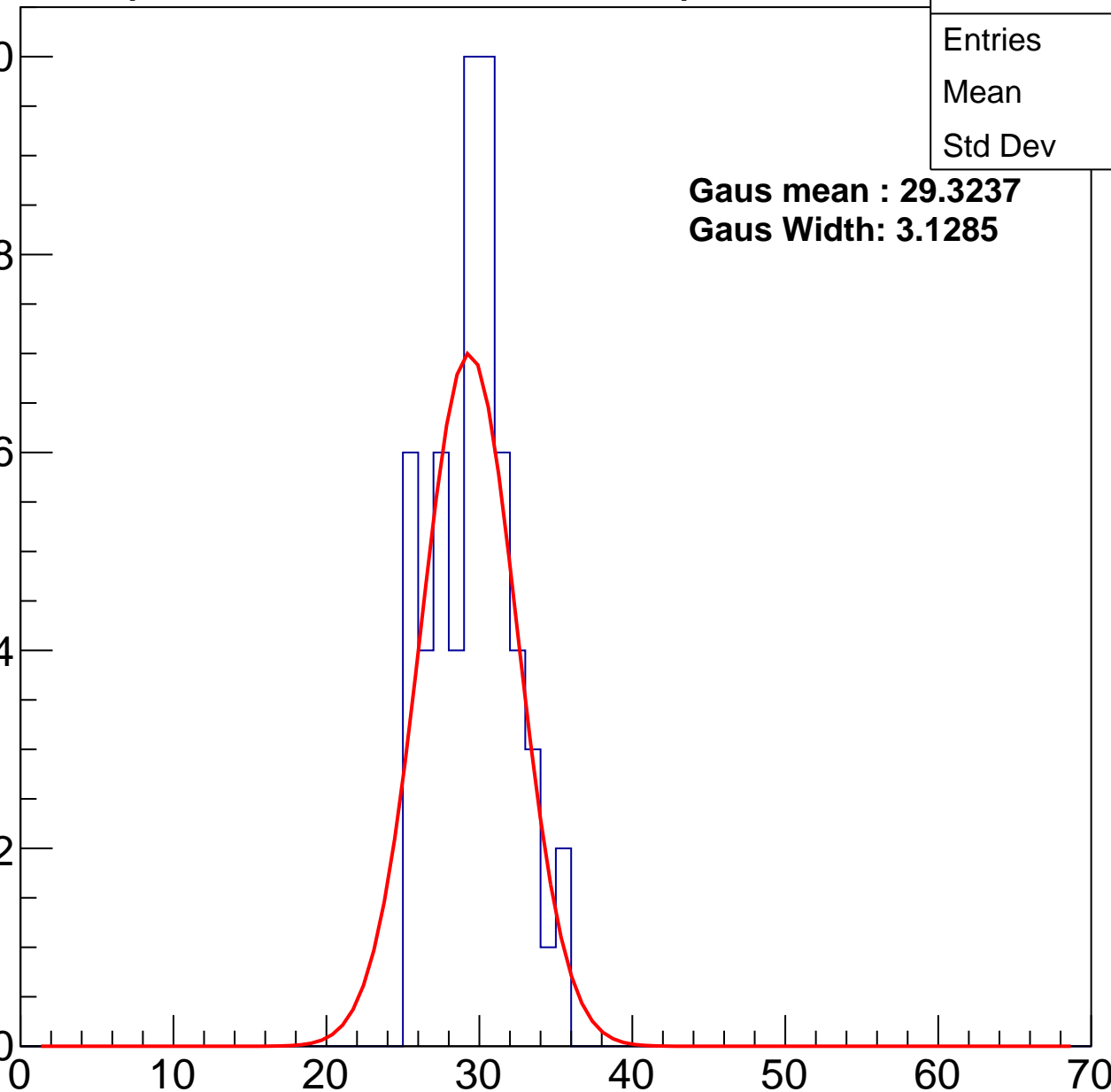
**Gaus mean : 29.3237**

**Gaus Width: 3.1285**

Entry

10  
8  
6  
4  
2  
0

ampl



# B1L003S, U11-ch114, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	66
Mean	35.73
Std Dev	3.25

**Gaus mean : 35.7021**

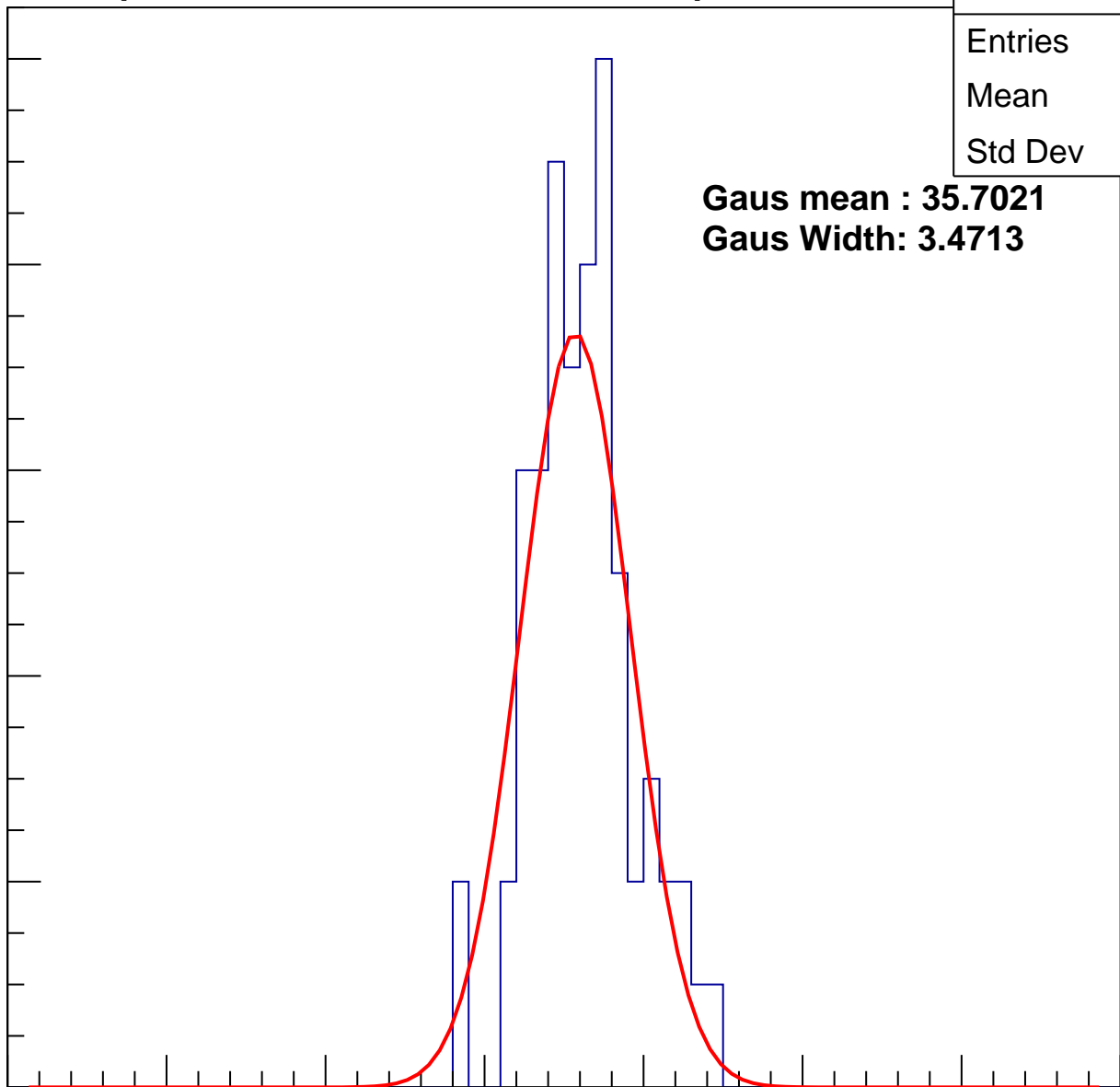
**Gaus Width: 3.4713**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U11-ch114, adc2

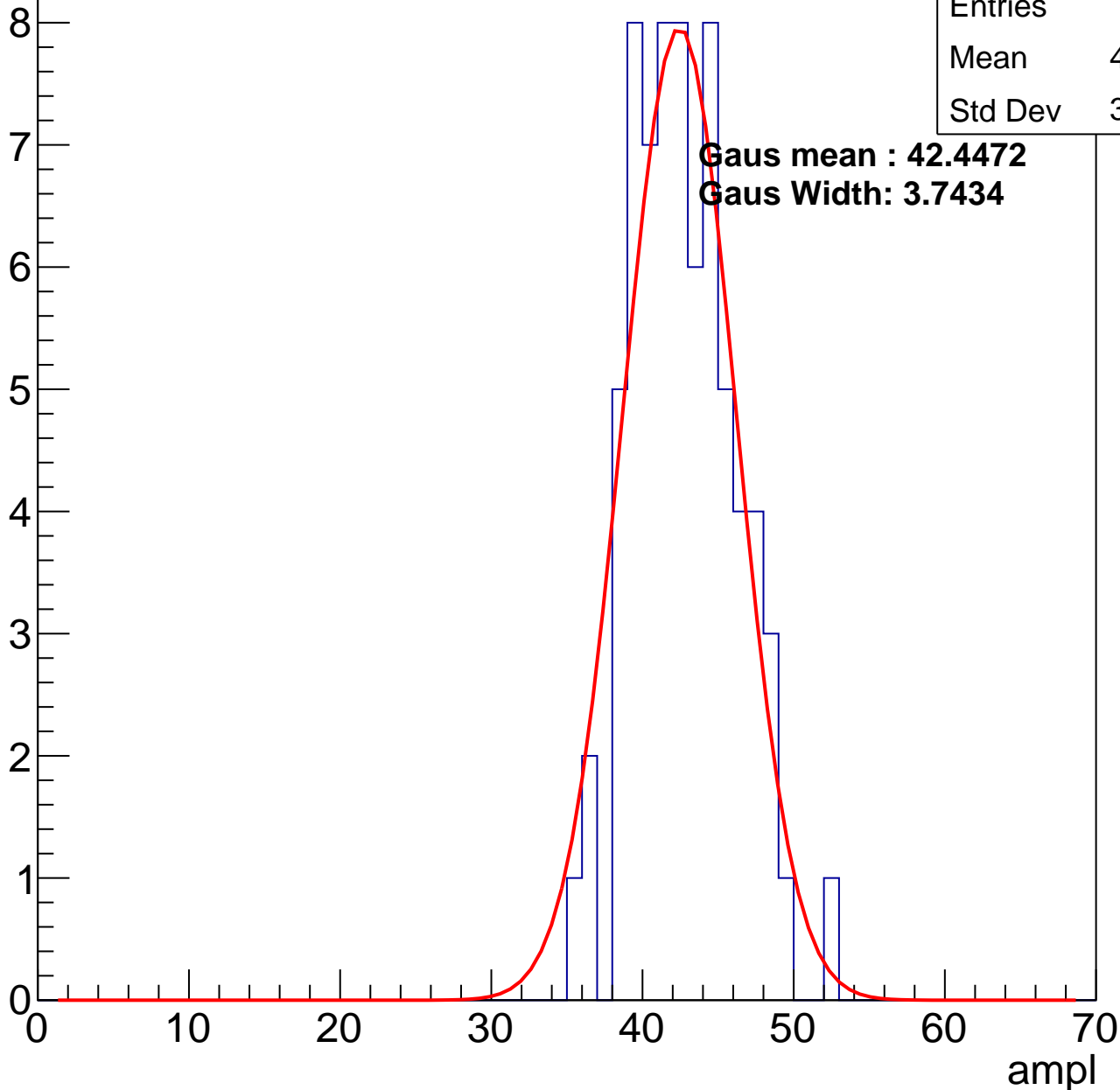
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	71
Mean	42.32
Std Dev	3.368

**Gaus mean : 42.4472**

**Gaus Width: 3.7434**

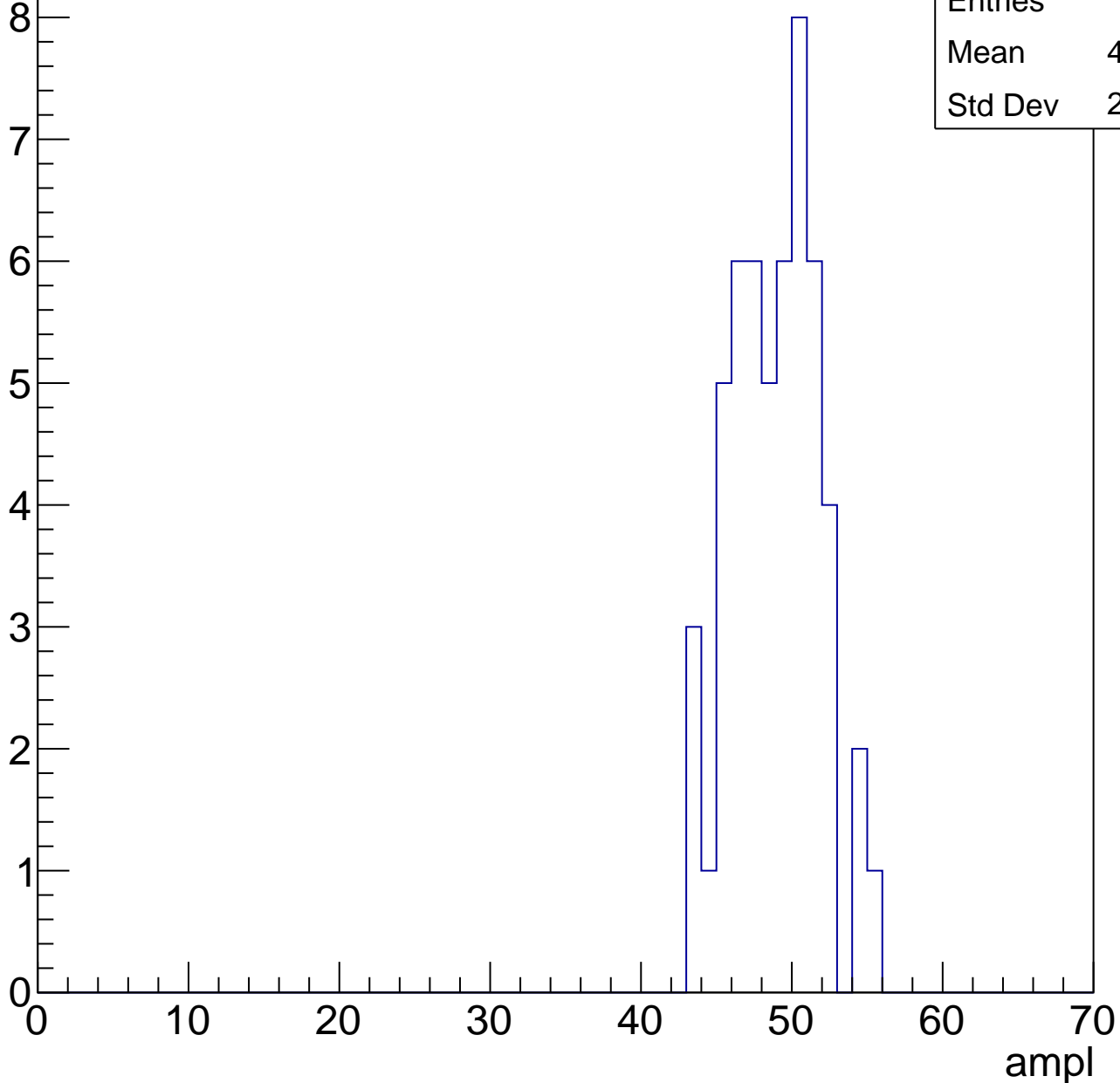


# B1L003S, U11-ch114, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	48.43
Std Dev	2.858

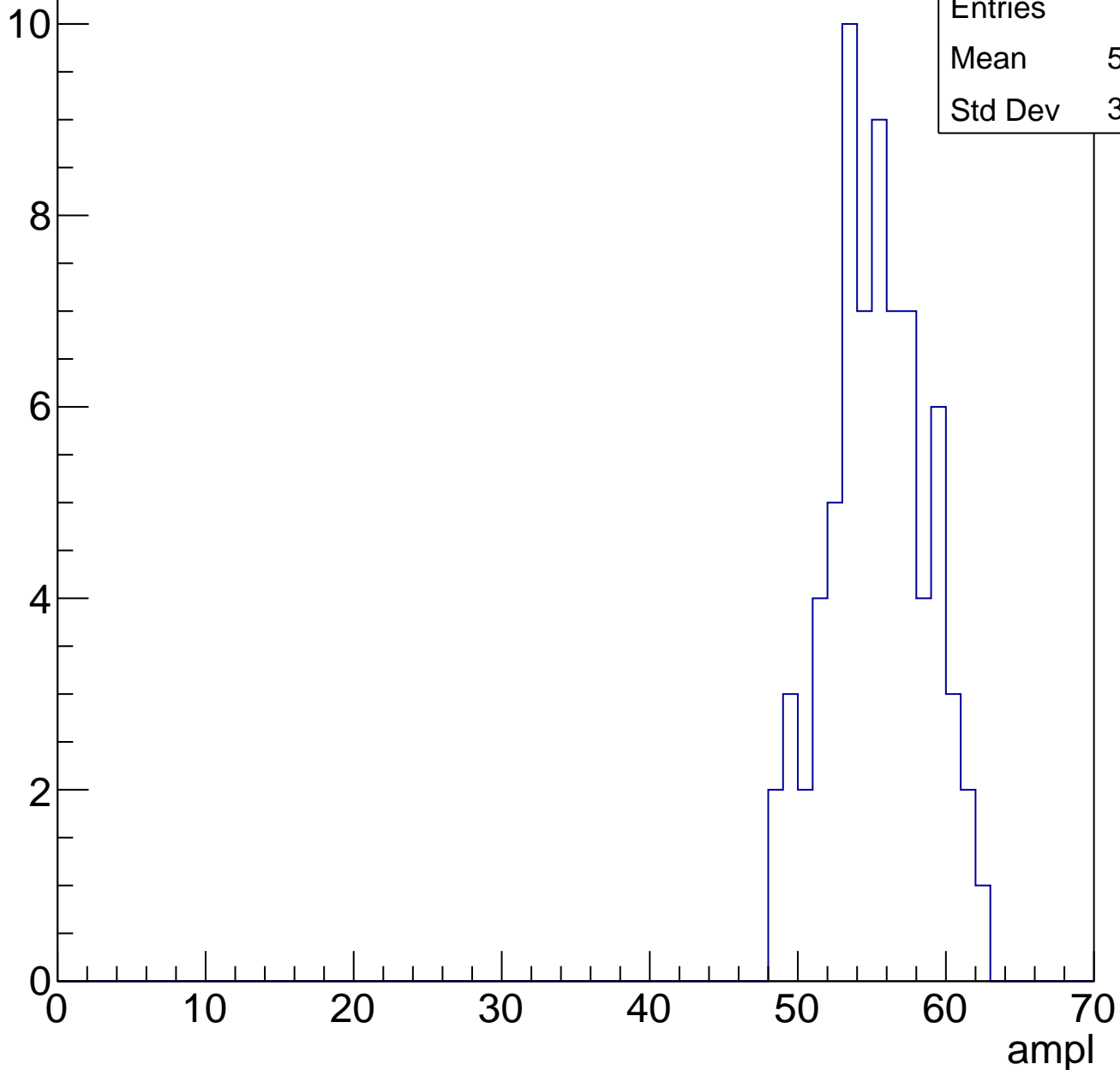


# B1L003S, U11-ch114, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	72
Mean	54.88
Std Dev	3.278

Entry

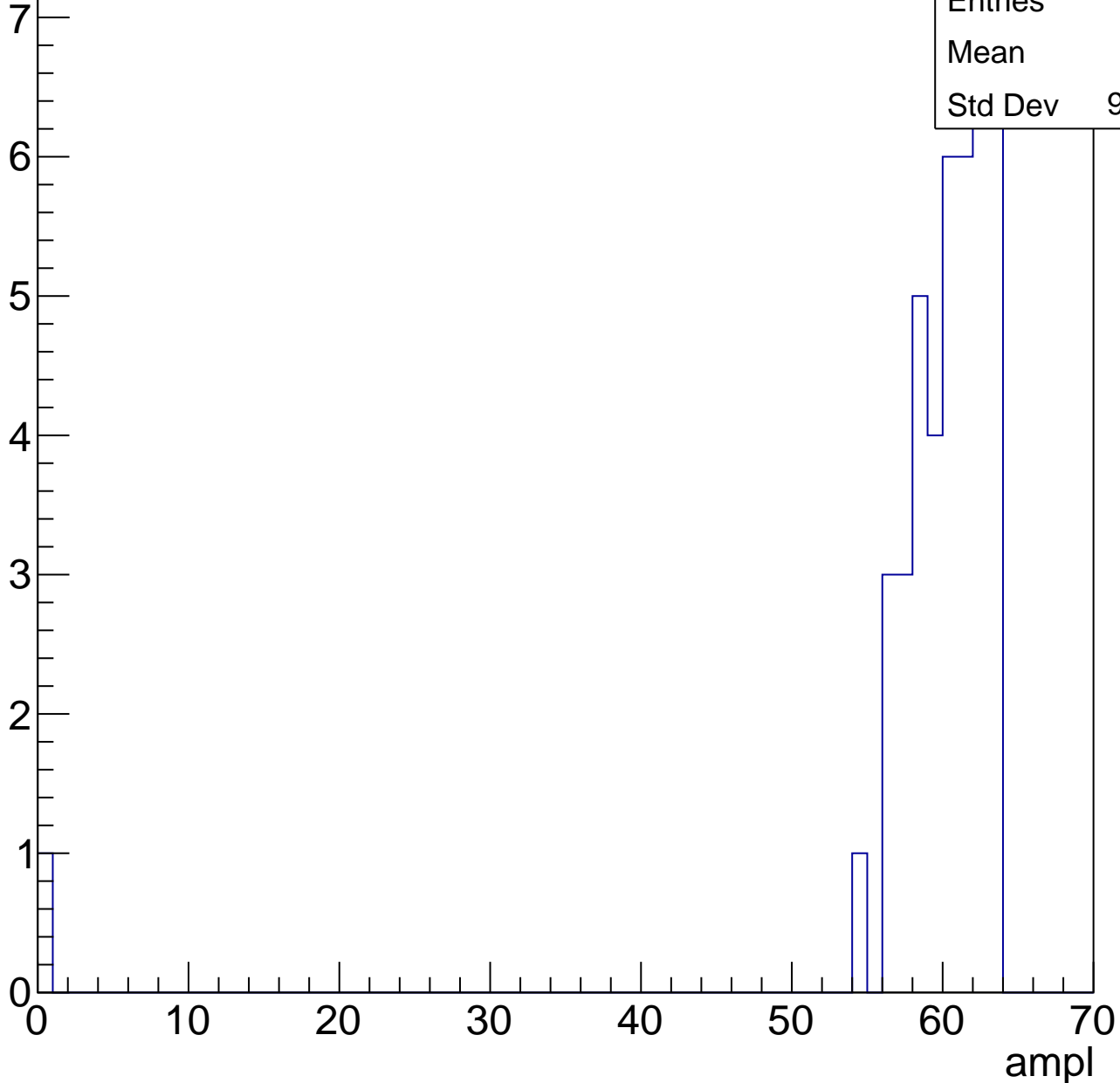


# B1L003S, U11-ch114, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

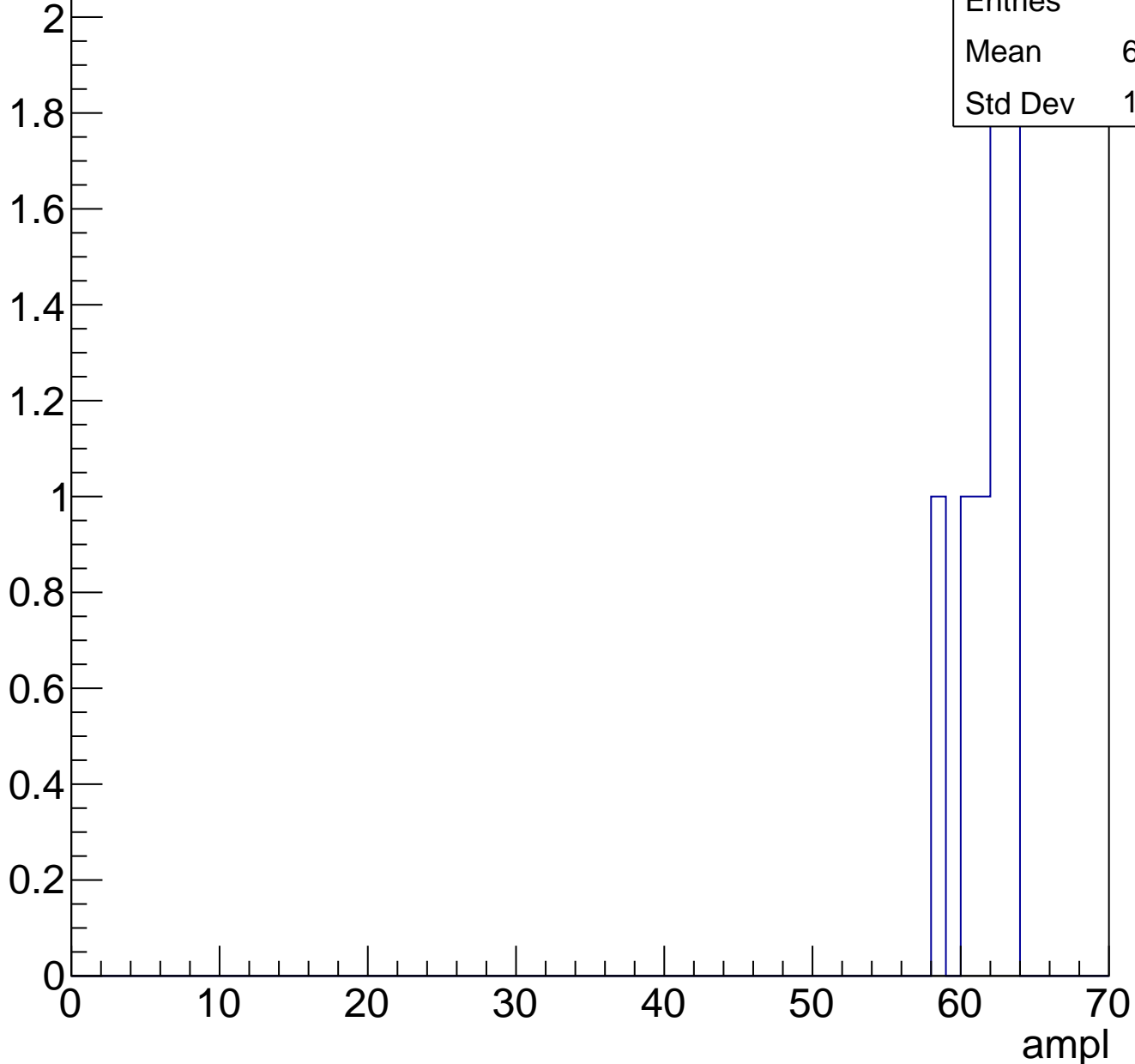
Entries	43
Mean	58.6
Std Dev	9.336



# B1L003S, U11-ch114, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch114, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U11-ch115, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	91
Mean	29.15
Std Dev	5.561

**Gaus mean : 30.3765**

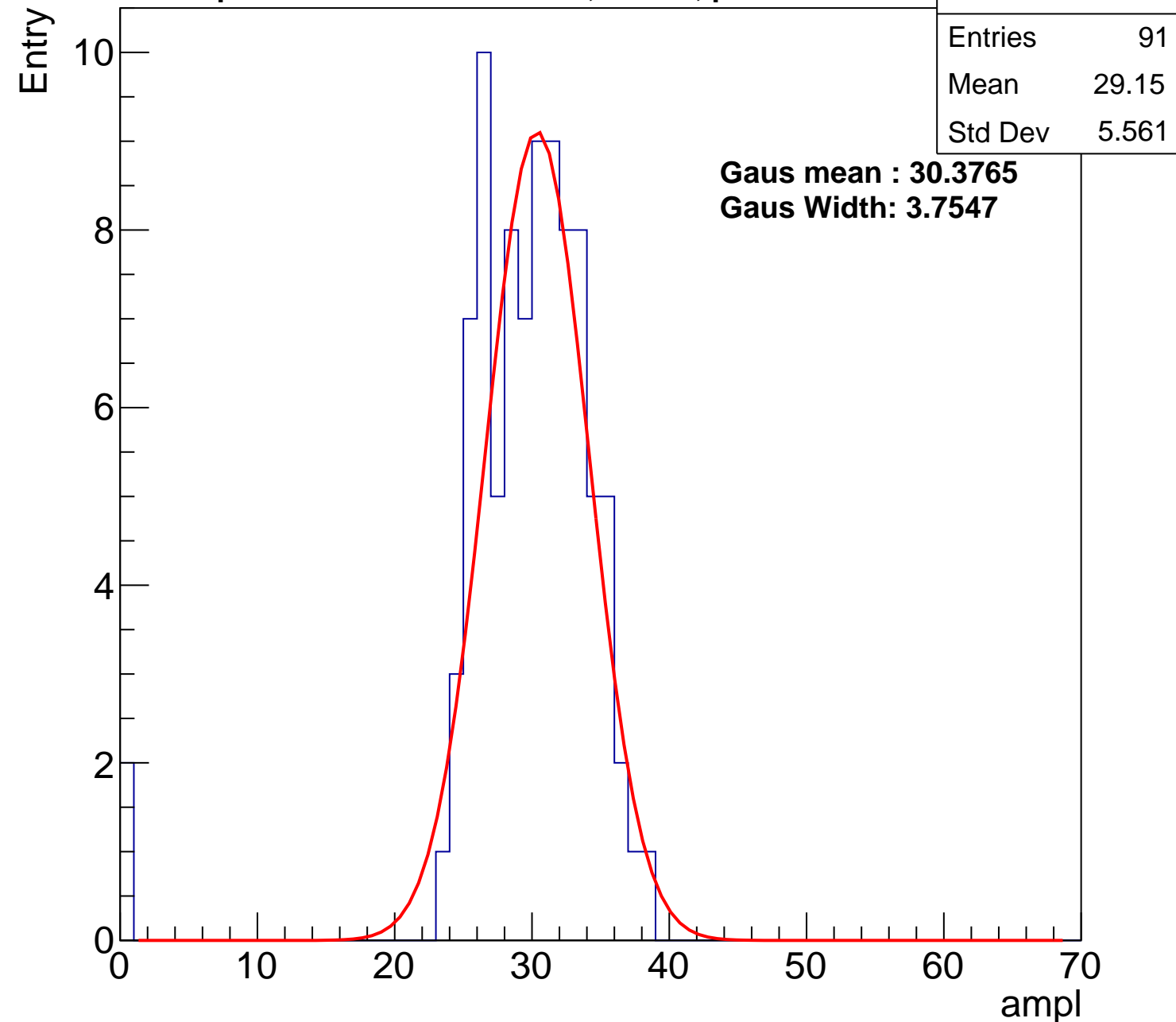
**Gaus Width: 3.7547**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U11-ch115, adc1

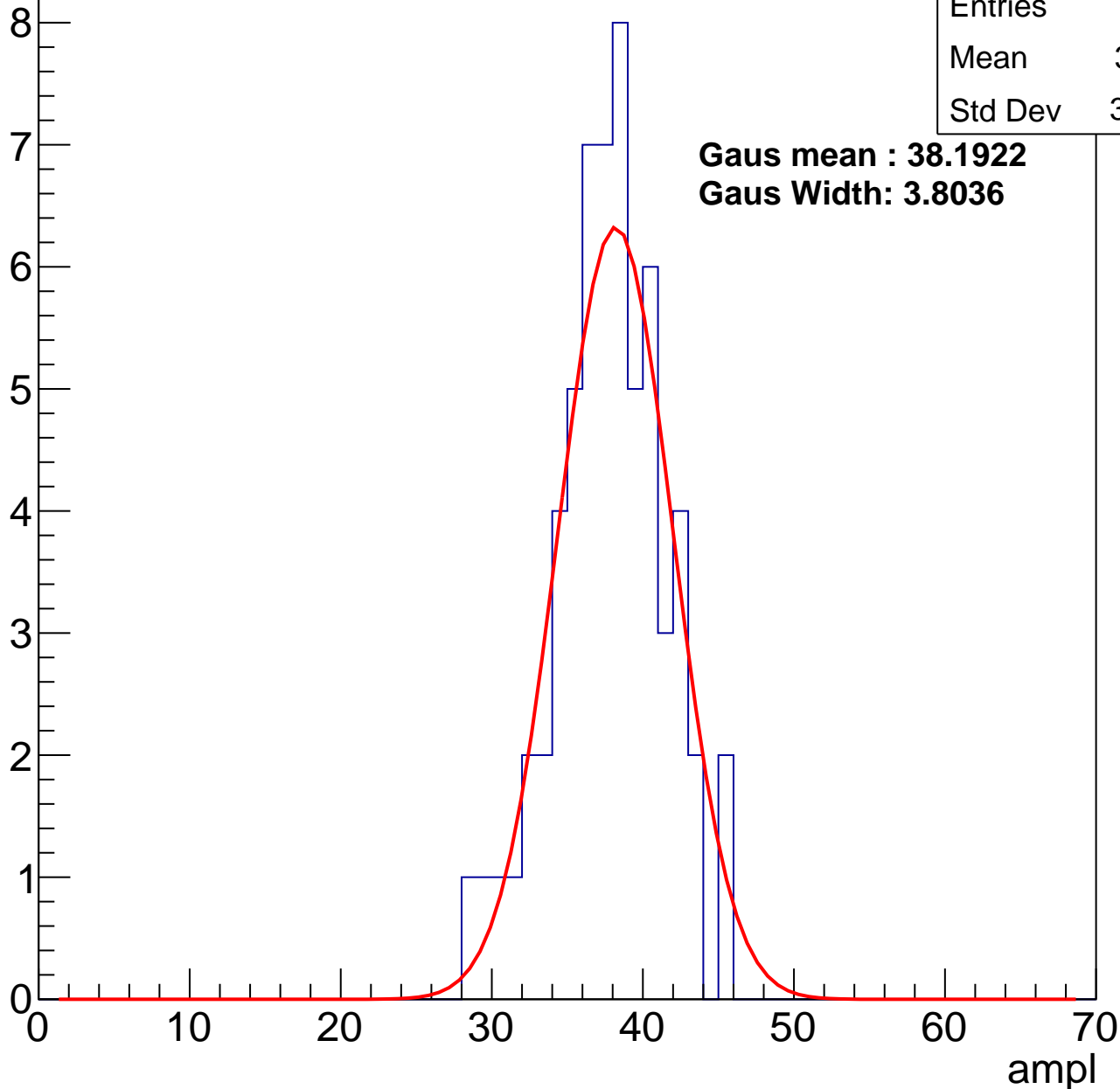
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	37.31
Std Dev	3.619

**Gaus mean : 38.1922**

**Gaus Width: 3.8036**



# B1L003S, U11-ch115, adc2

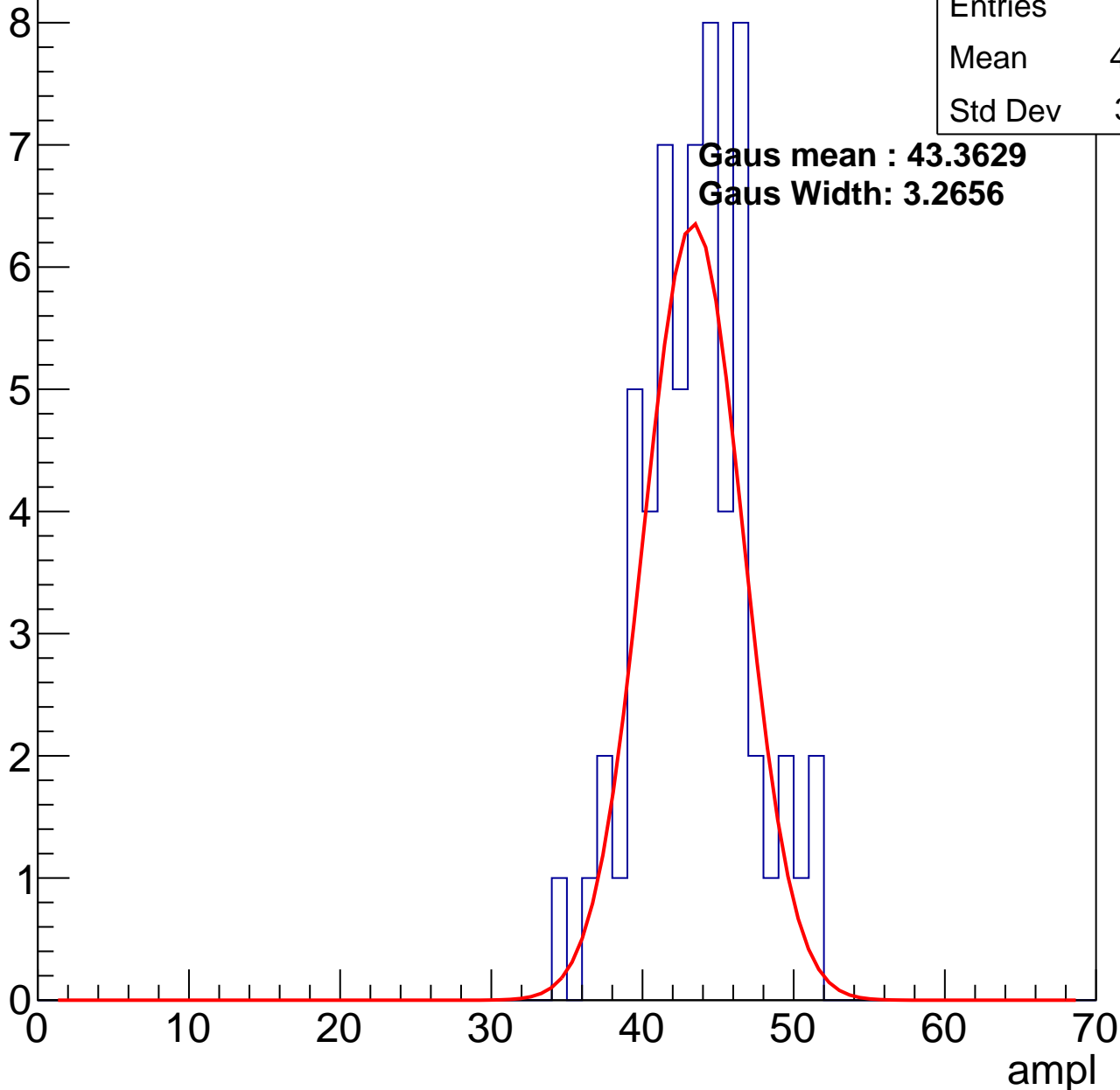
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	43.07
Std Dev	3.571

**Gaus mean : 43.3629**

**Gaus Width: 3.2656**

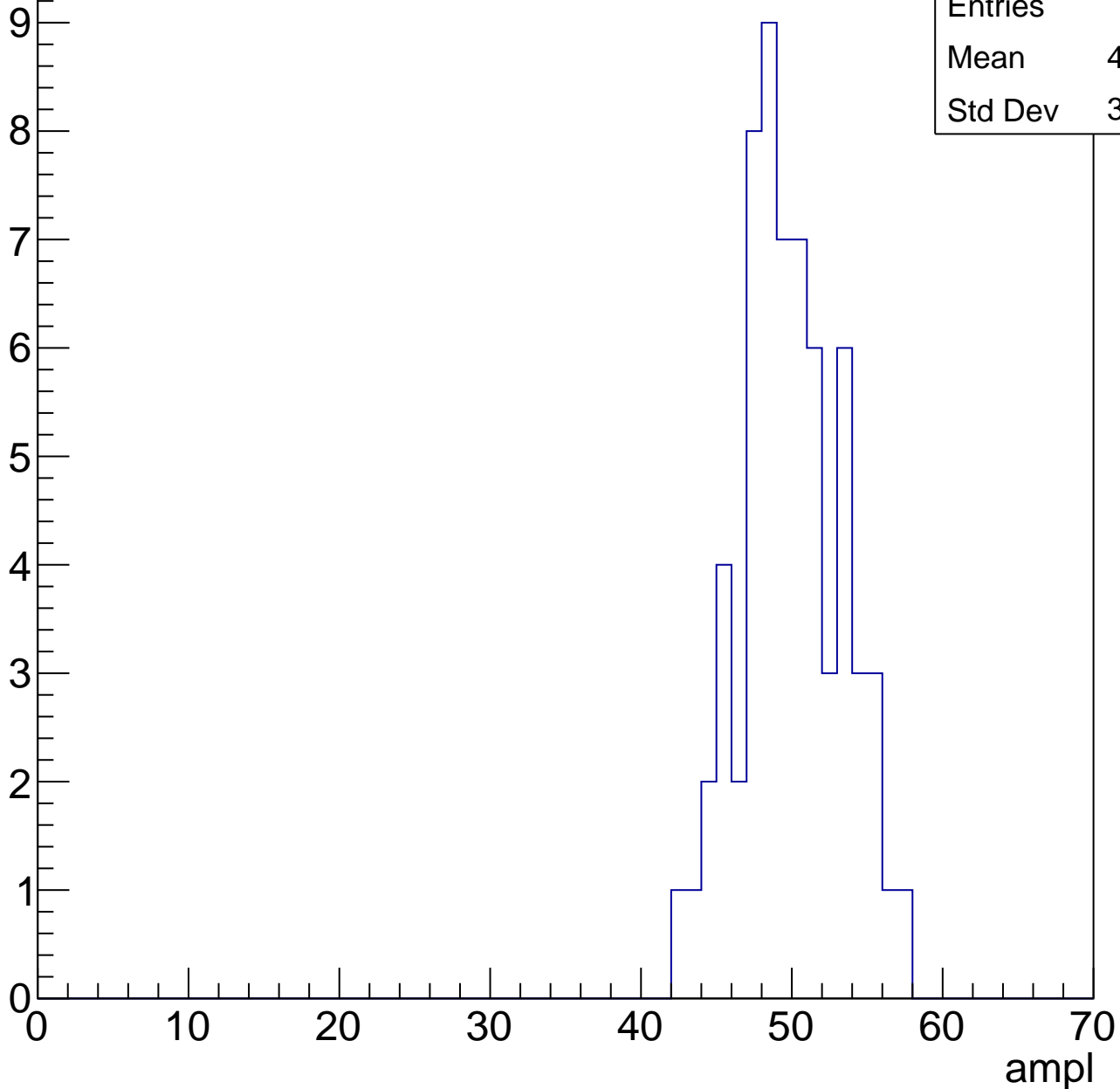


# B1L003S, U11-ch115, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	49.47
Std Dev	3.293

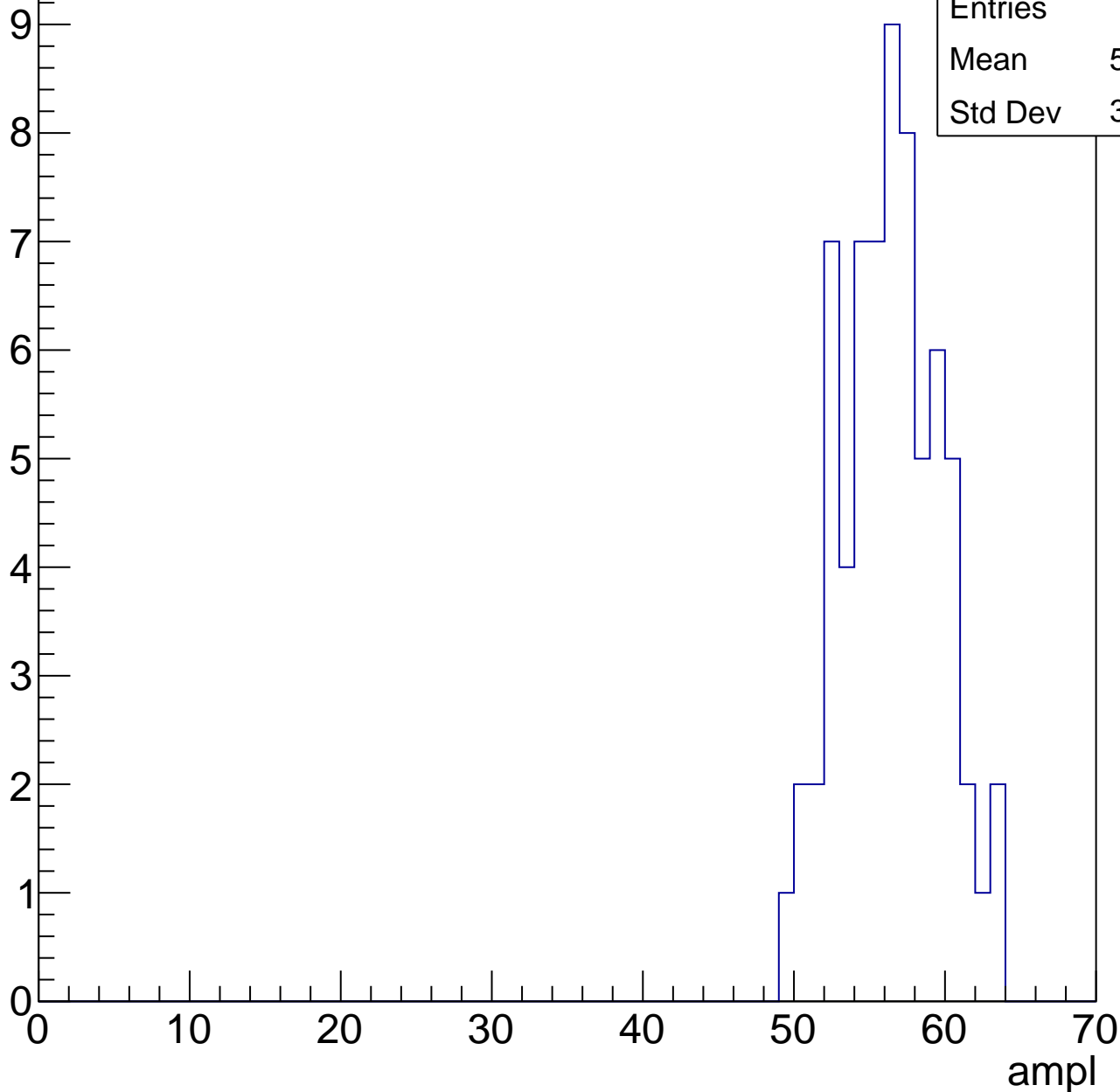


# B1L003S, U11-ch115, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	55.94
Std Dev	3.208

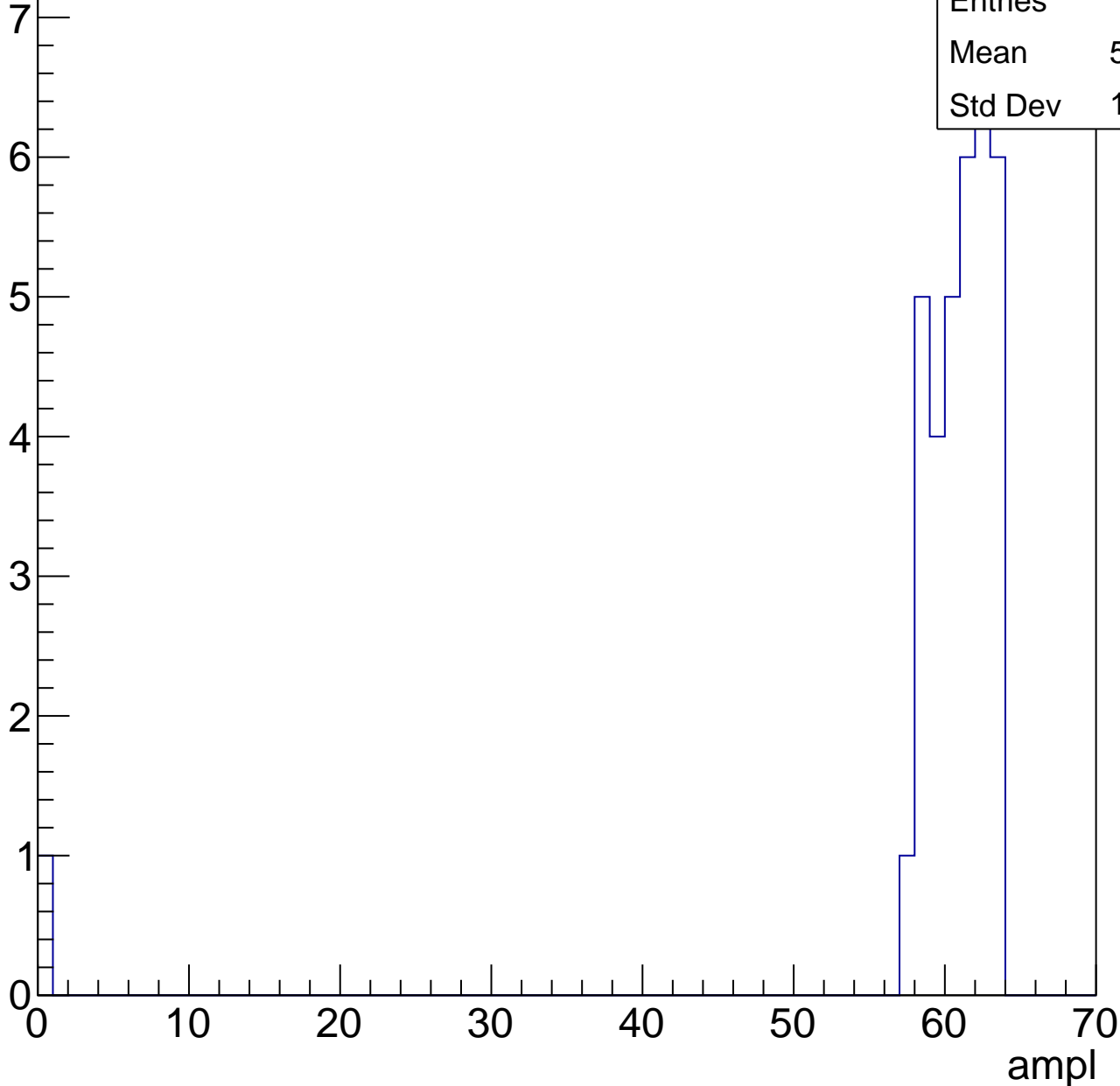


# B1L003S, U11-ch115, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	35
Mean	58.89
Std Dev	10.25



# B1L003S, U11-ch115, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

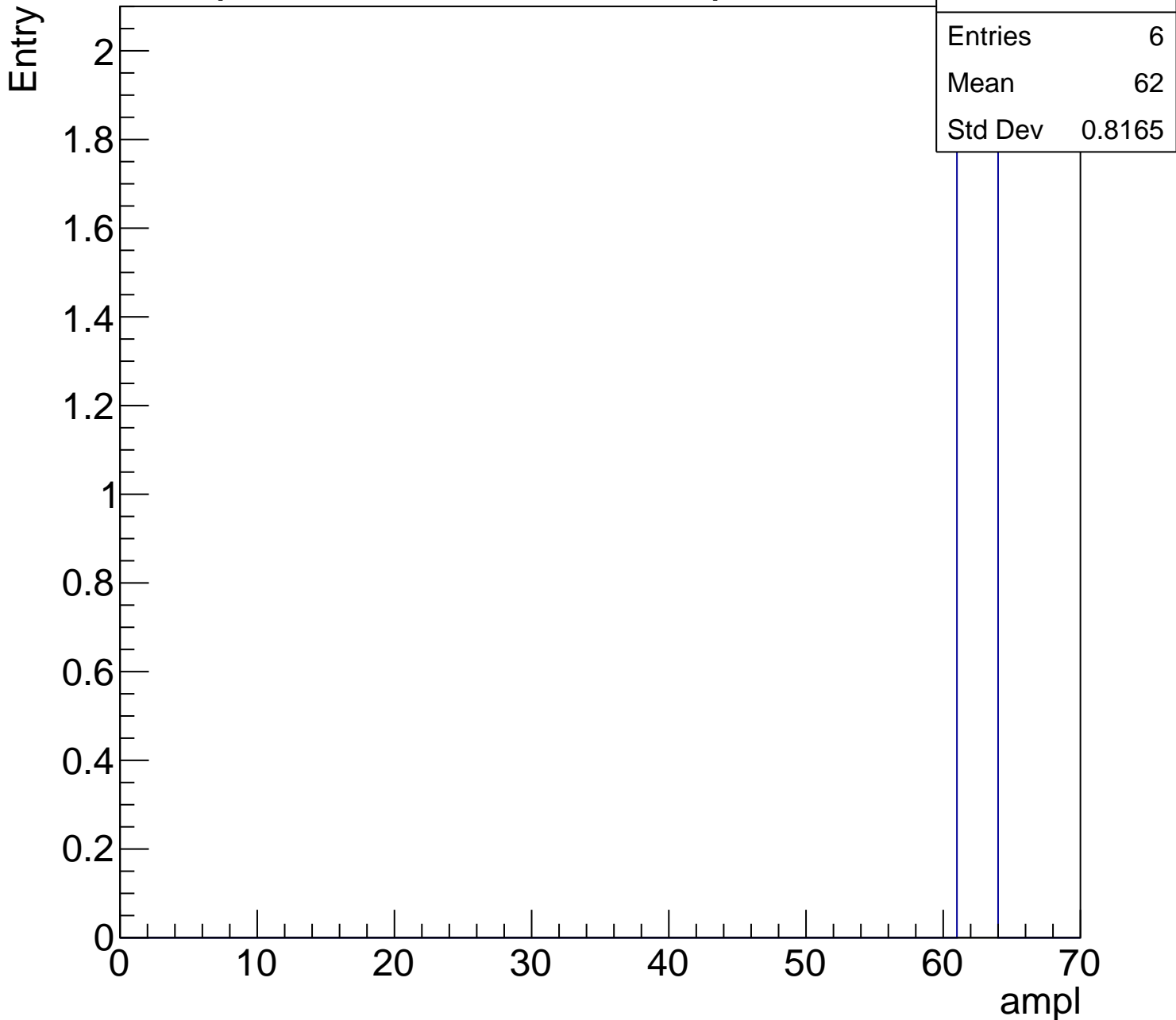
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	62
Std Dev	0.8165

0 10 20 30 40 50 60 70

ampl





# B1L003S, U11-ch115, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U11-ch116, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	64
Mean	29.33
Std Dev	2.716

**Gaus mean : 29.7099**

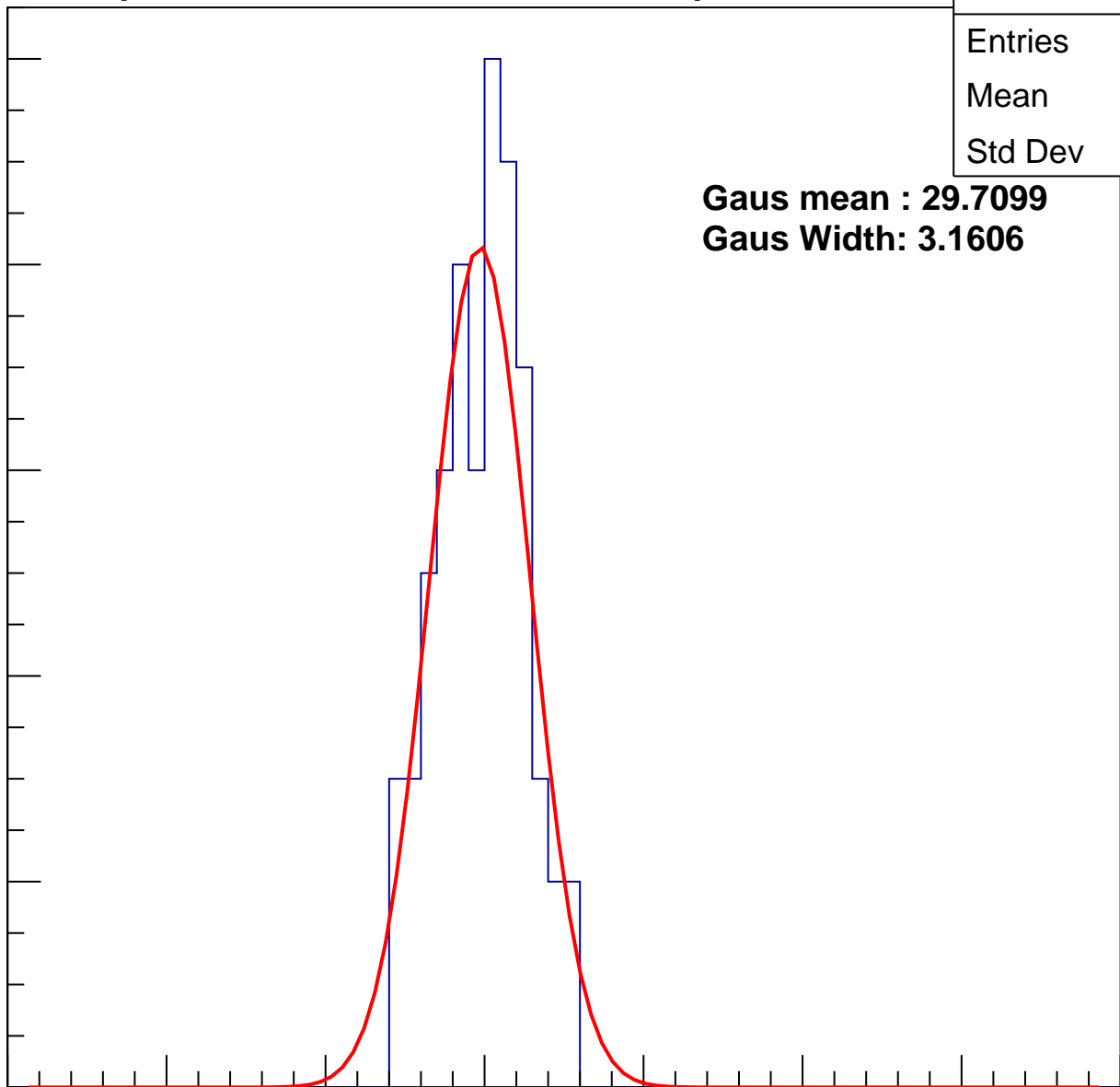
**Gaus Width: 3.1606**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U11-ch116, adc1

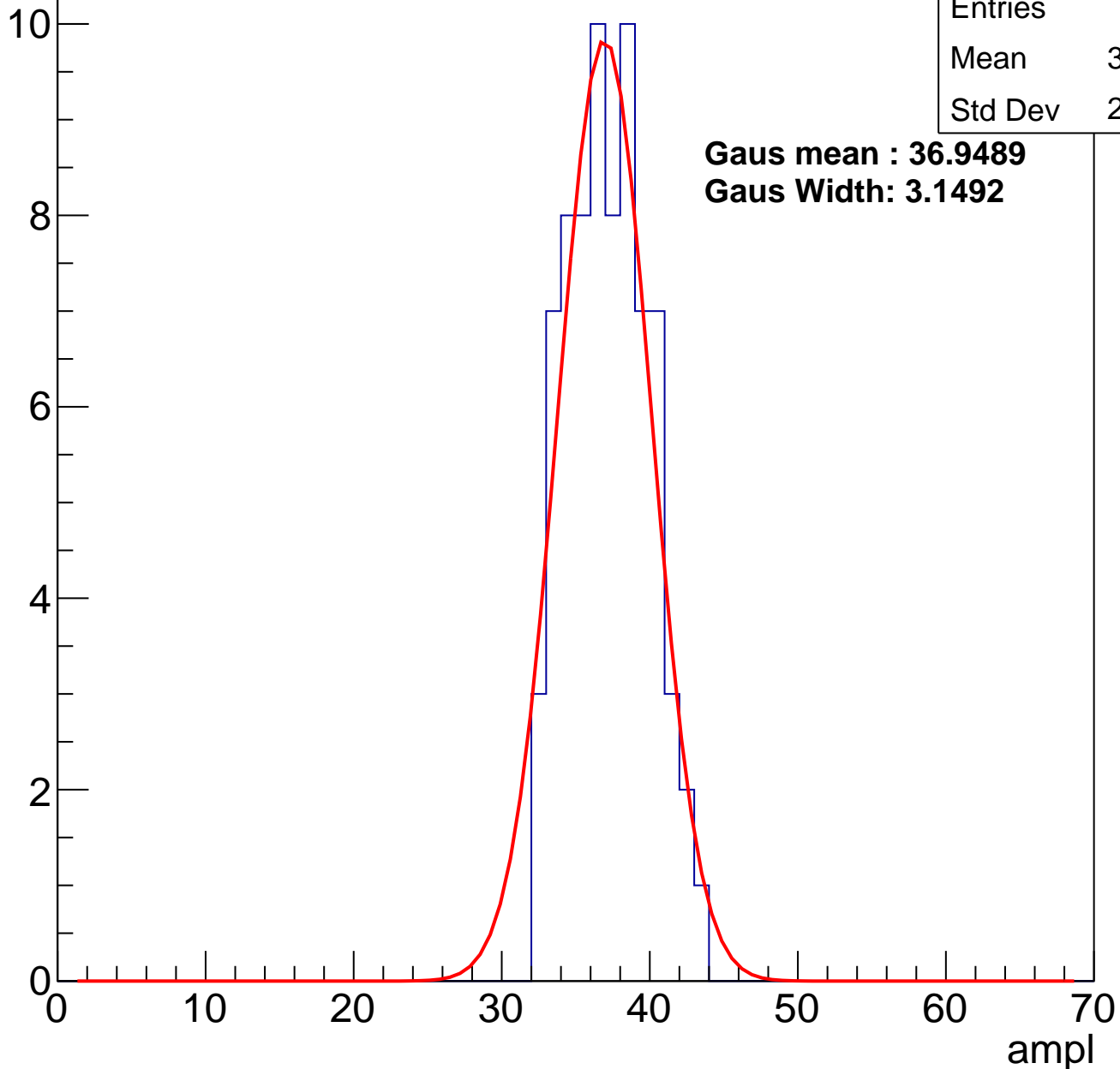
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	74
Mean	36.73
Std Dev	2.678

**Gaus mean : 36.9489**

**Gaus Width: 3.1492**

Entry



# B1L003S, U11-ch116, adc2

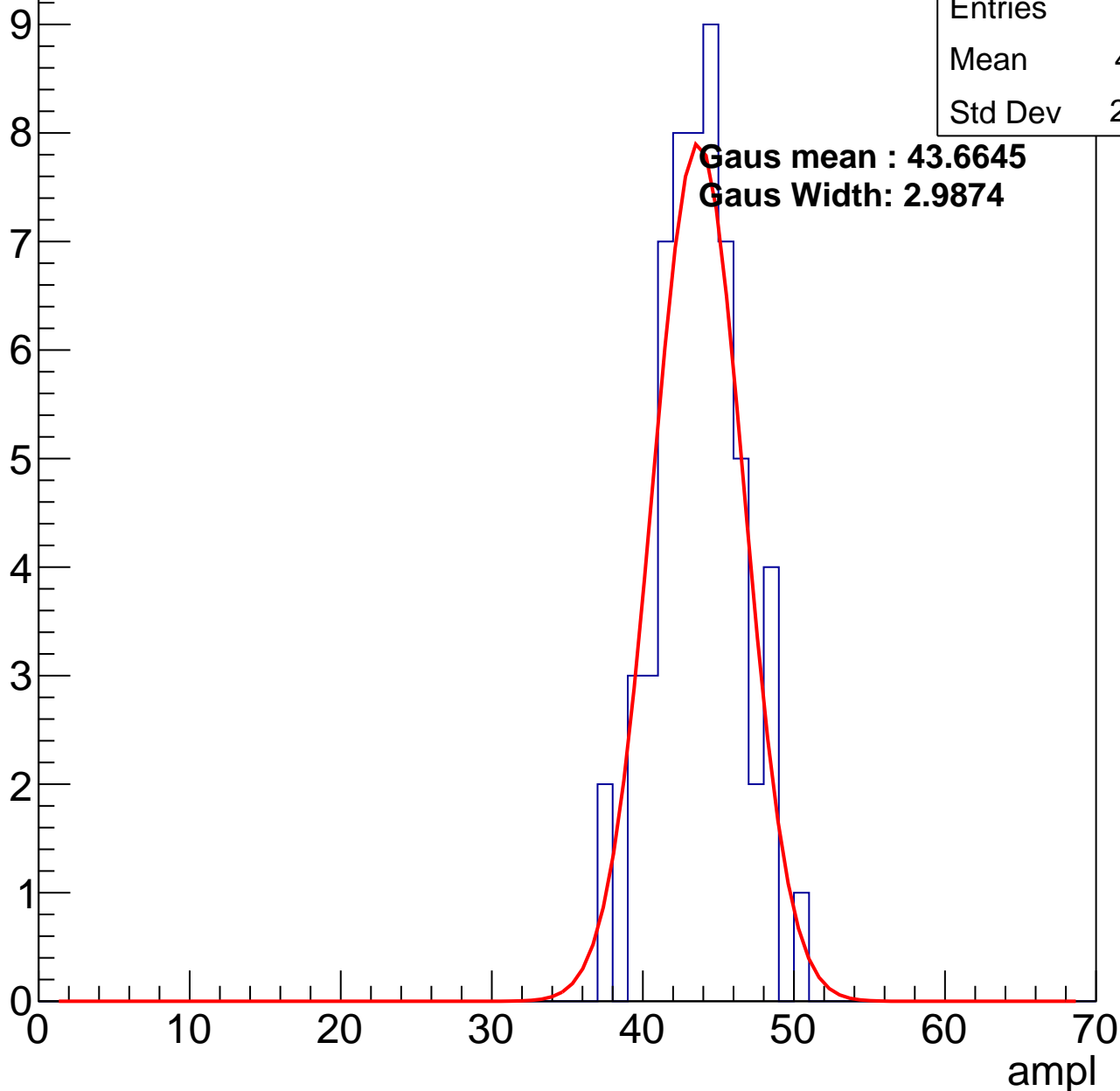
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	43.31
Std Dev	2.732

**Gaus mean : 43.6645**

**Gaus Width: 2.9874**

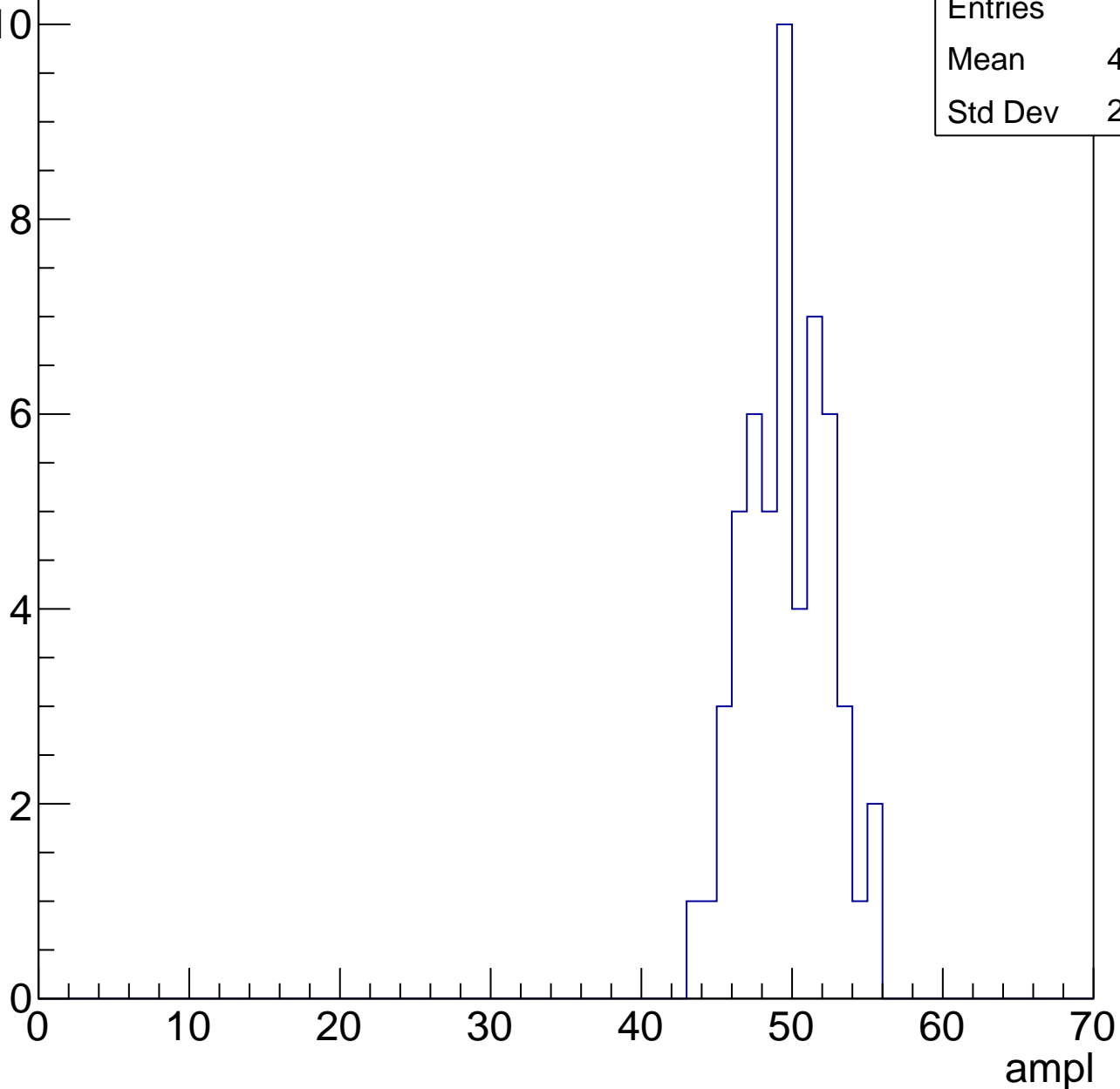


# B1L003S, U11-ch116, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	54
Mean	49.19
Std Dev	2.763

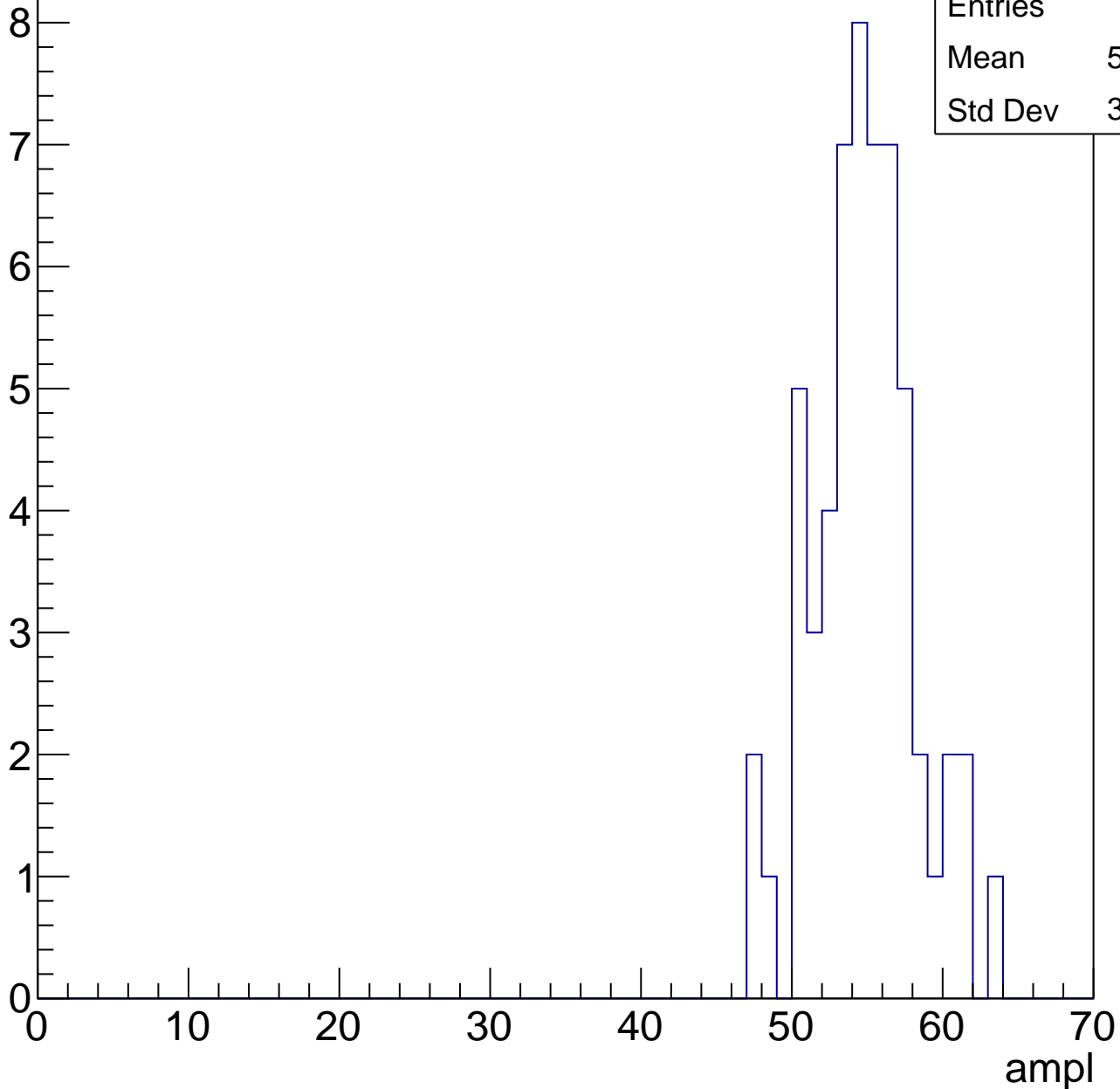


# B1L003S, U11-ch116, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	54.35
Std Dev	3.364



# B1L003S, U11-ch116, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

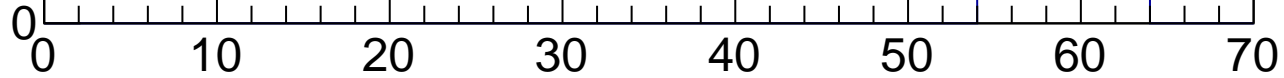
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	50
Mean	59.84
Std Dev	2.335

ampl

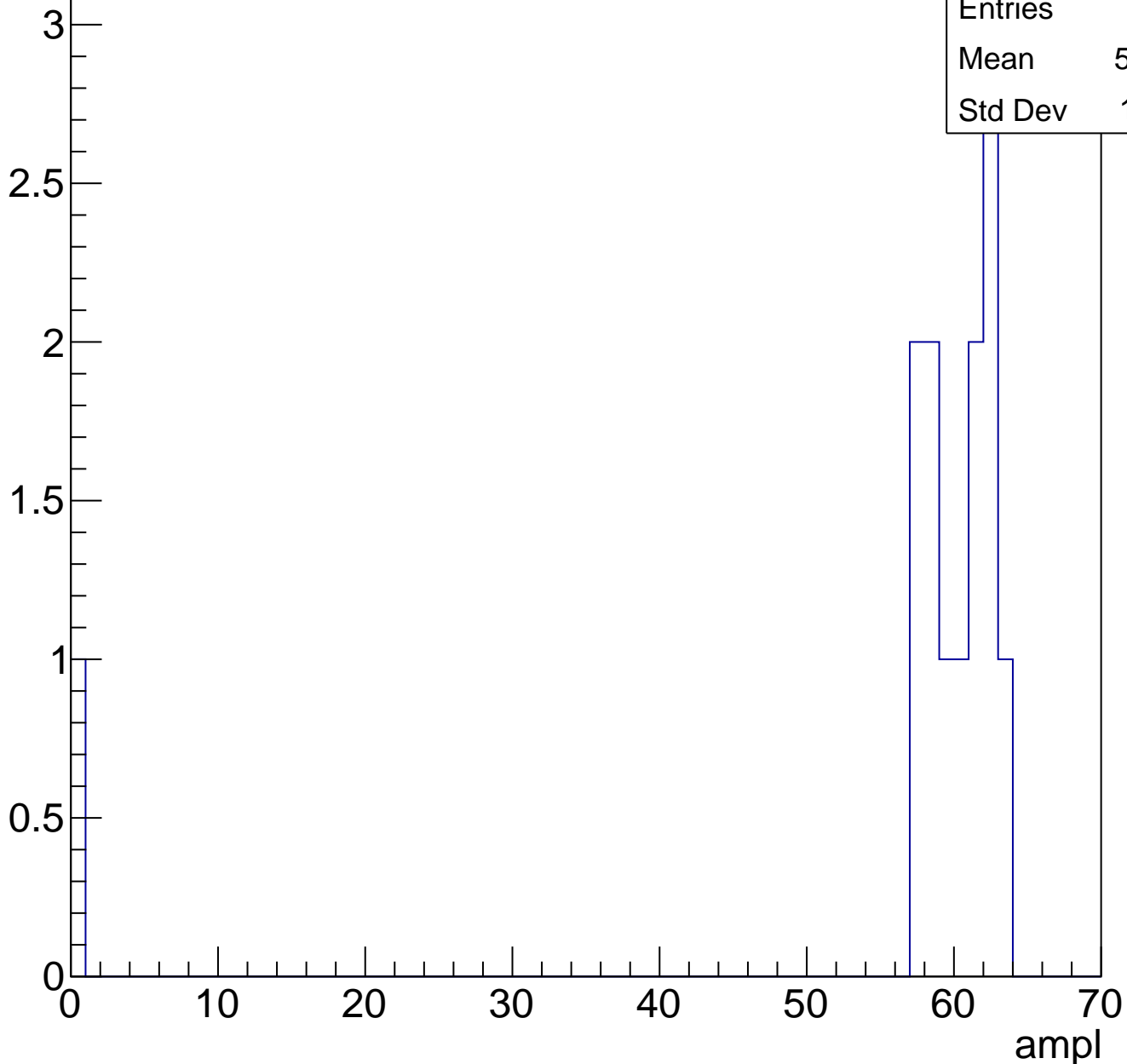
0 10 20 30 40 50 60 70



# B1L003S, U11-ch116, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	13
Mean	55.38
Std Dev	16.11



# B1L003S, U11-ch116, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U11-ch117, adc0

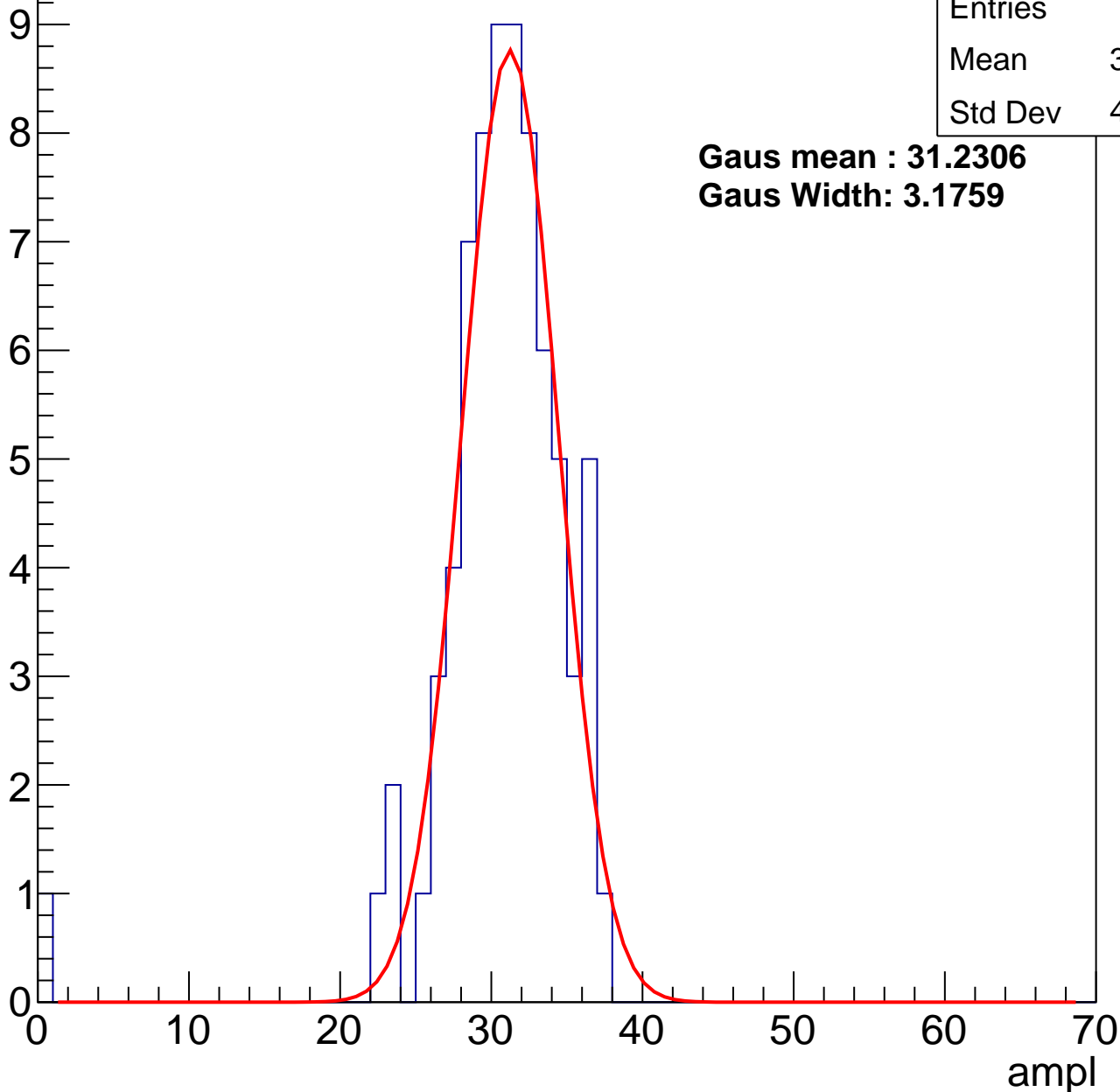
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	73
Mean	30.16
Std Dev	4.803

**Gaus mean : 31.2306**

**Gaus Width: 3.1759**



# B1L003S, U11-ch117, adc1

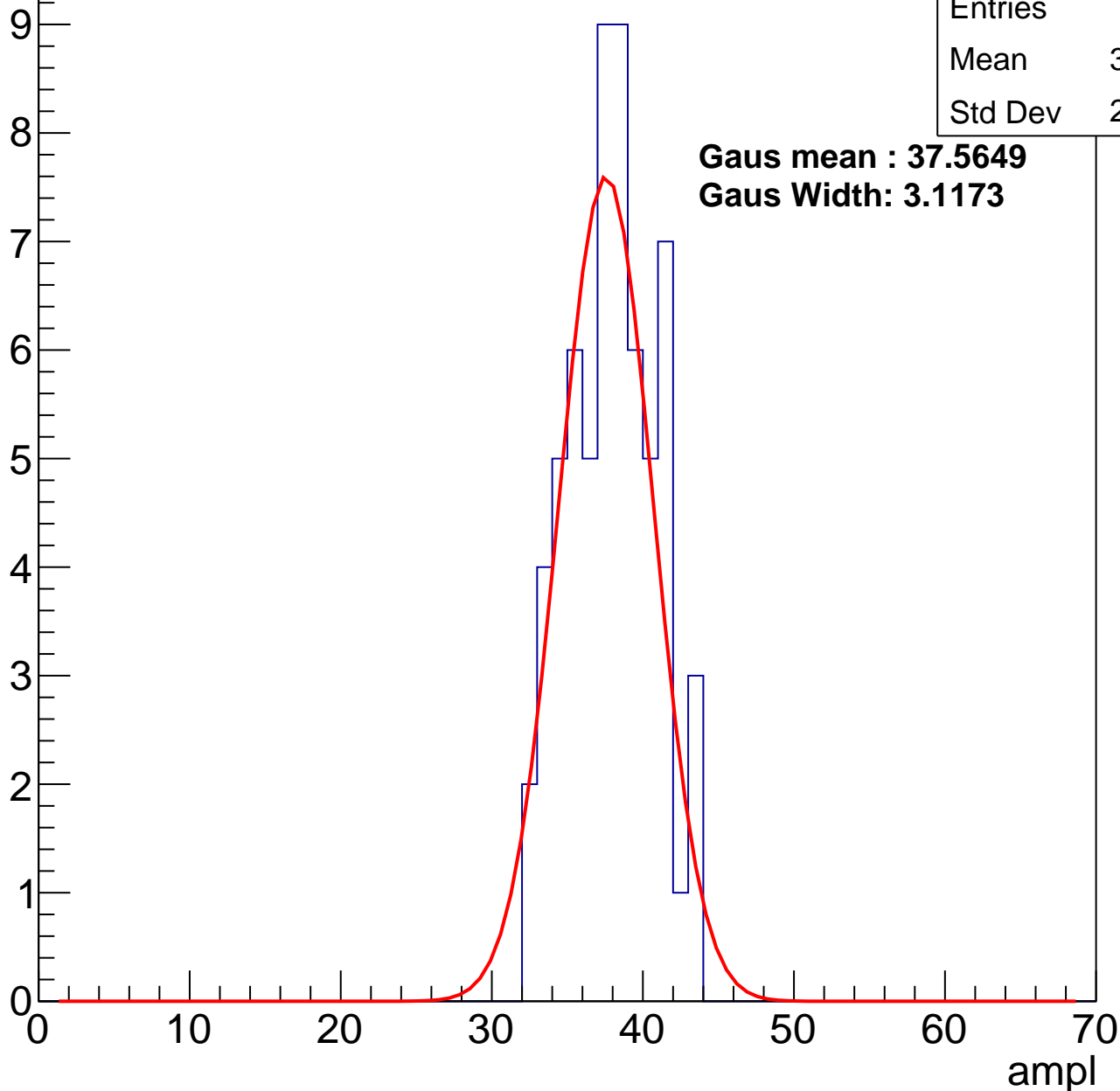
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	37.47
Std Dev	2.833

**Gaus mean : 37.5649**

**Gaus Width: 3.1173**



# B1L003S, U11-ch117, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	63
Mean	43.56
Std Dev	3.059

**Gaus mean : 44.1987**

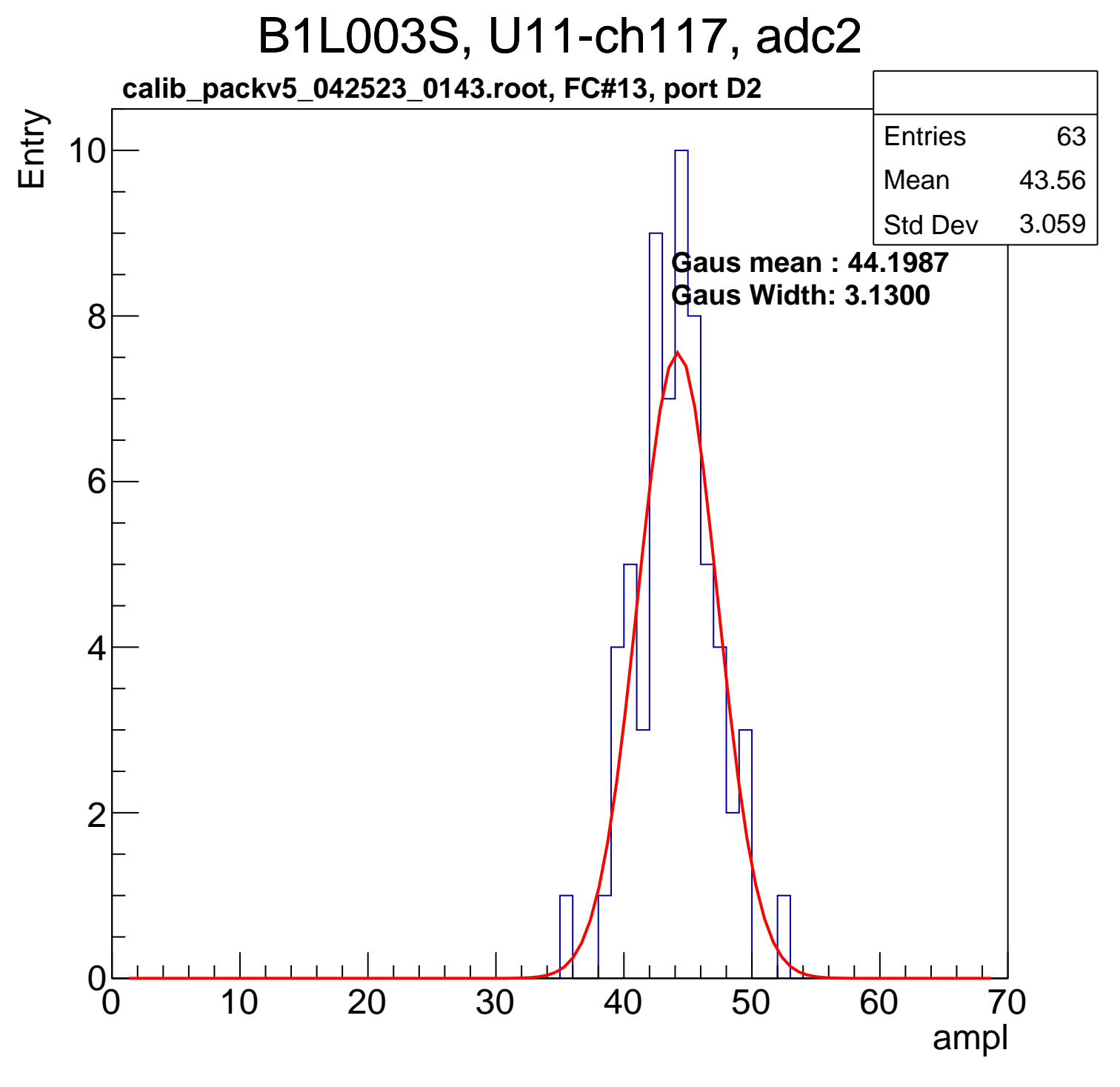
**Gaus Width: 3.1300**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

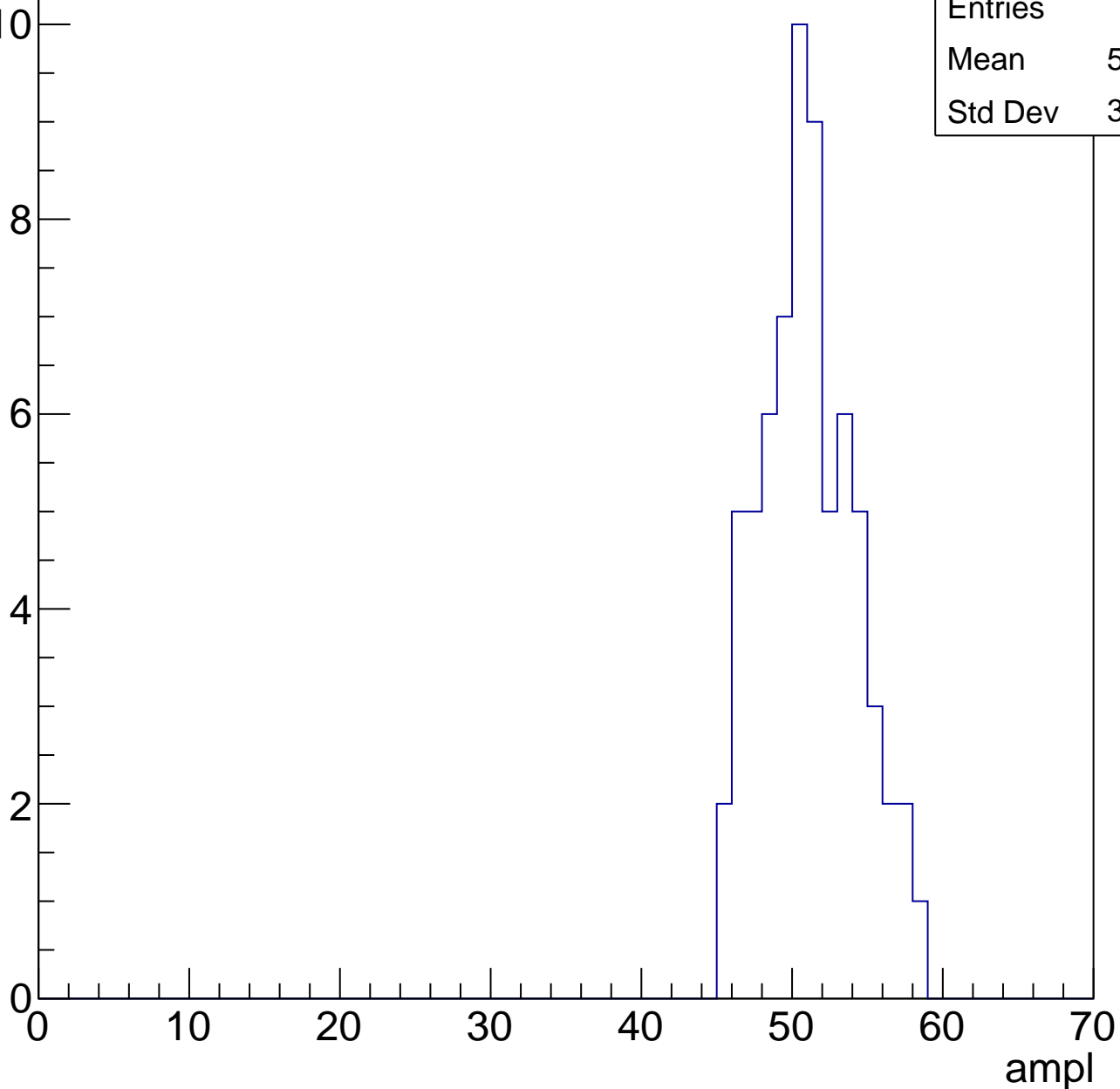


# B1L003S, U11-ch117, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	50.62
Std Dev	3.097

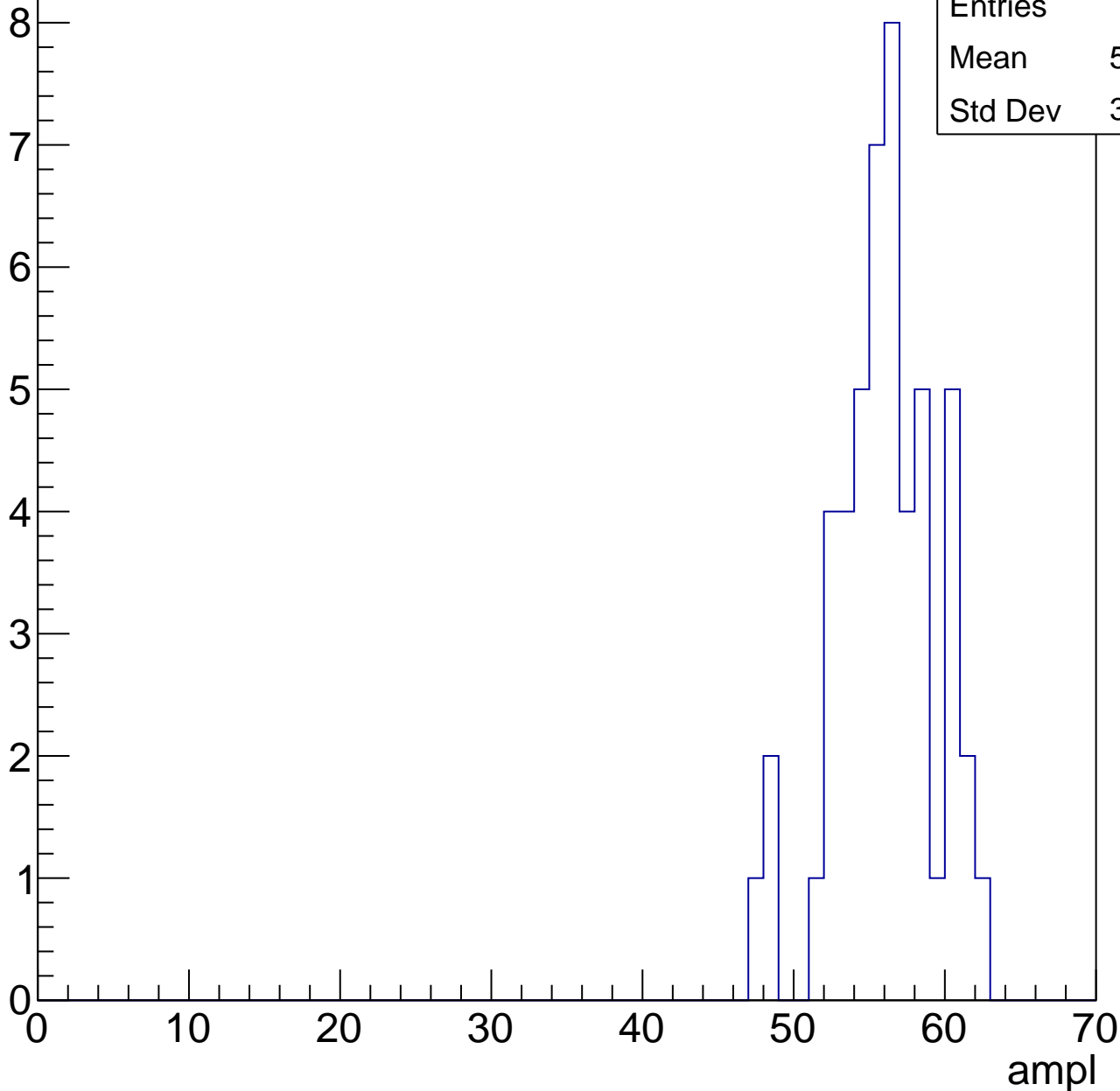


# B1L003S, U11-ch117, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

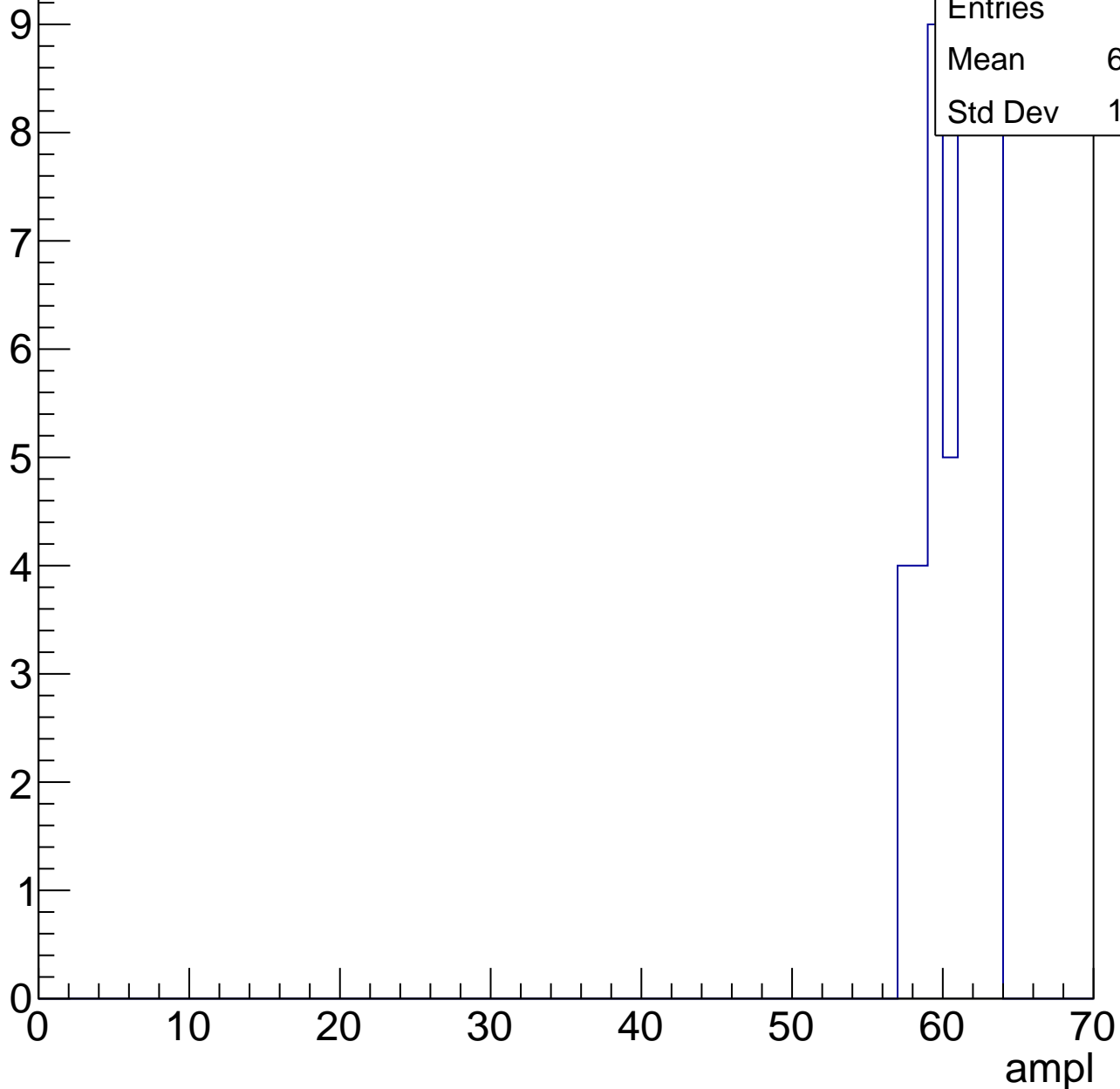
Entries	50
Mean	55.56
Std Dev	3.318



# B1L003S, U11-ch117, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U11-ch117, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch117, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U11-ch118, adc0

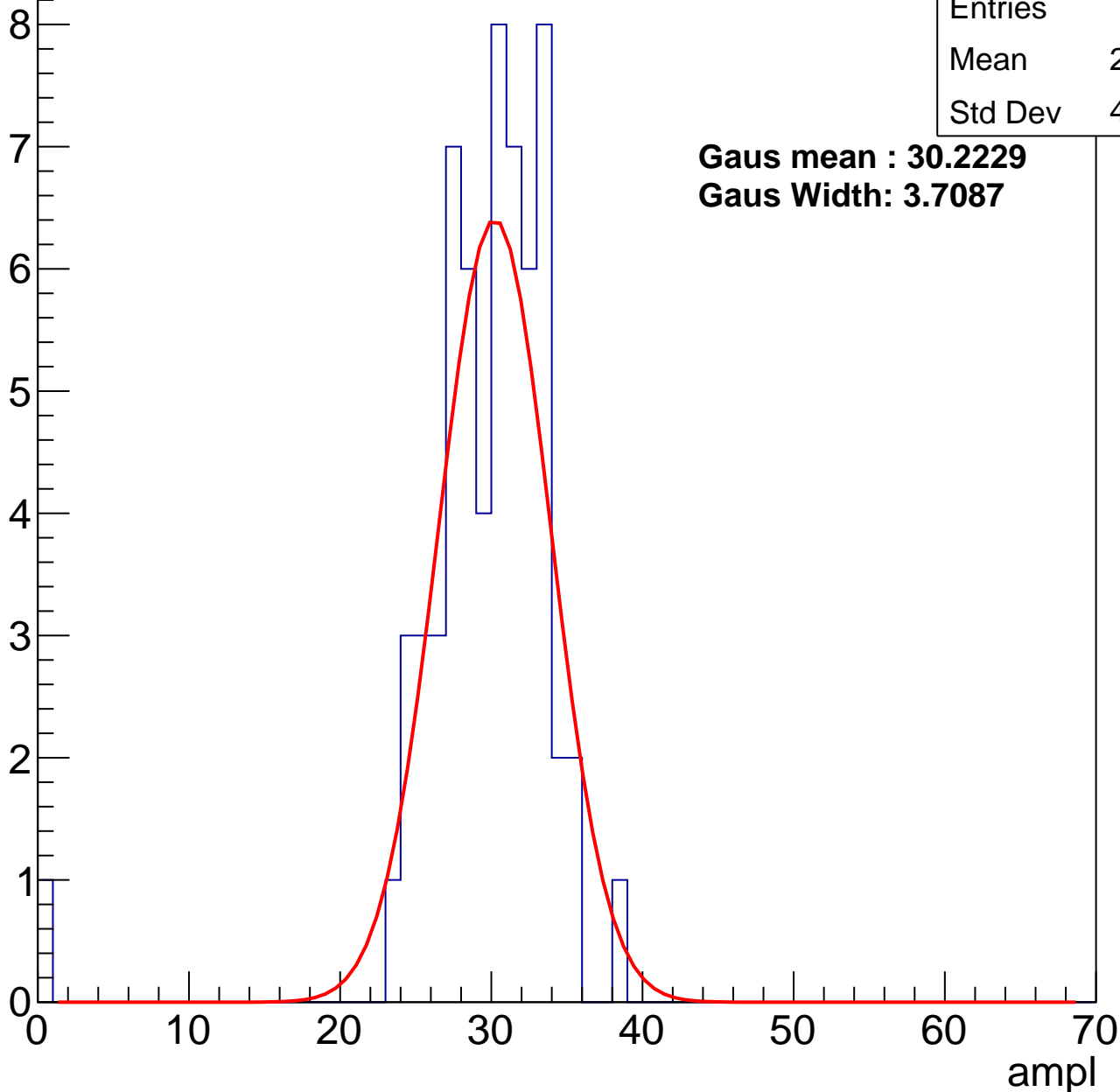
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	29.19
Std Dev	4.885

**Gaus mean : 30.2229**

**Gaus Width: 3.7087**



# B1L003S, U11-ch118, adc1

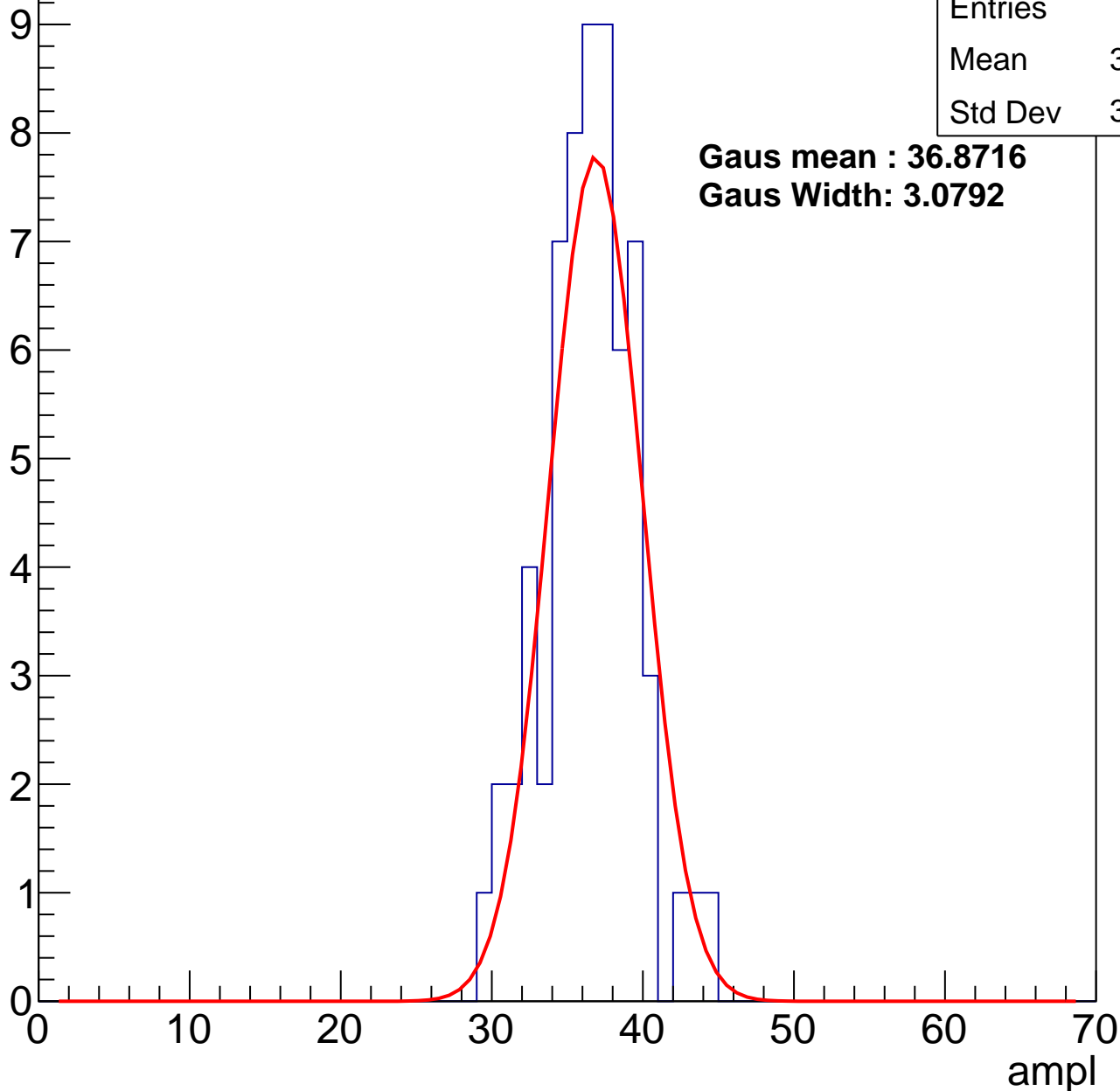
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	36.03
Std Dev	3.039

**Gaus mean : 36.8716**

**Gaus Width: 3.0792**



# B1L003S, U11-ch118, adc2

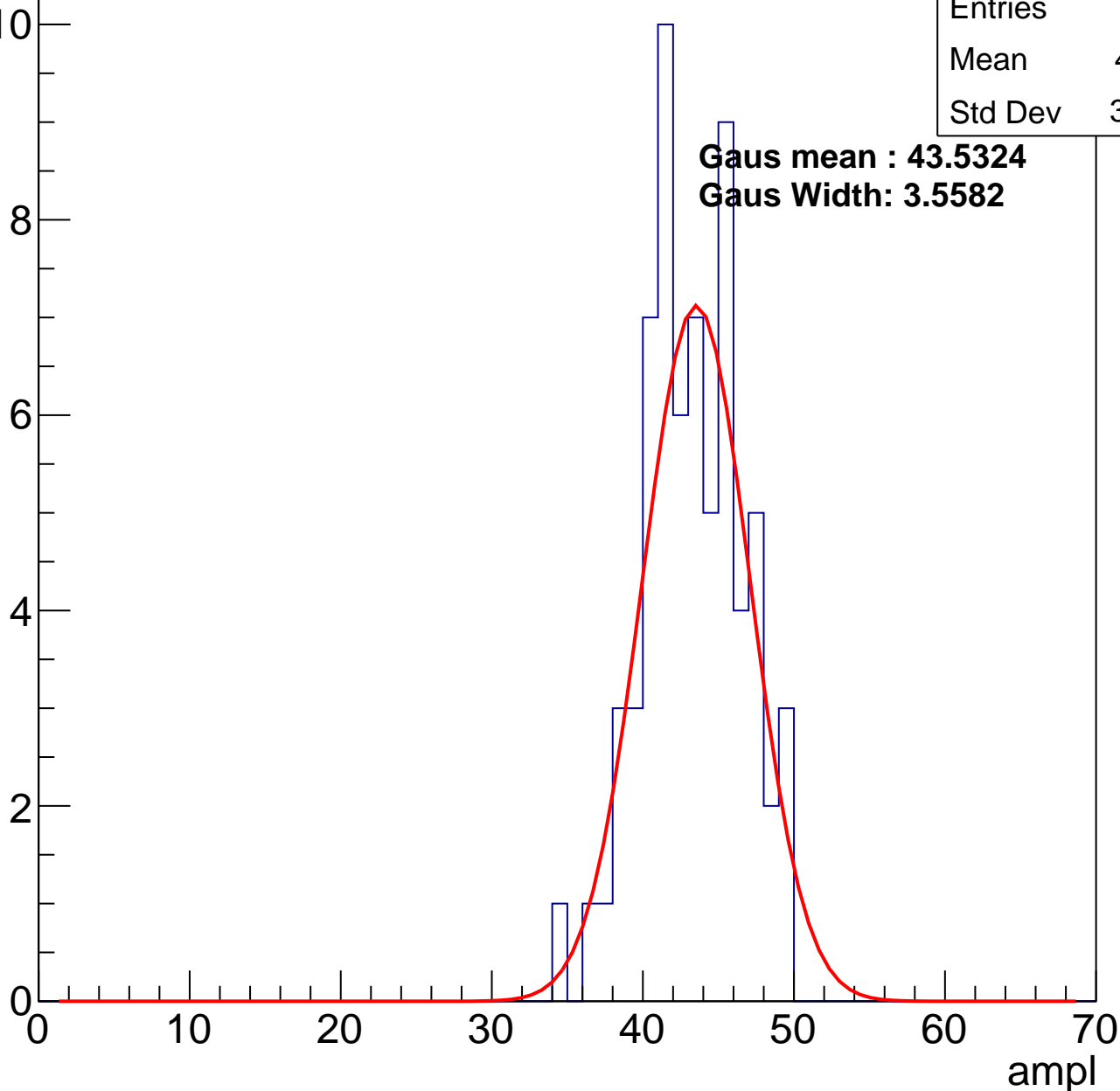
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	42.81
Std Dev	3.256

**Gaus mean : 43.5324**

**Gaus Width: 3.5582**

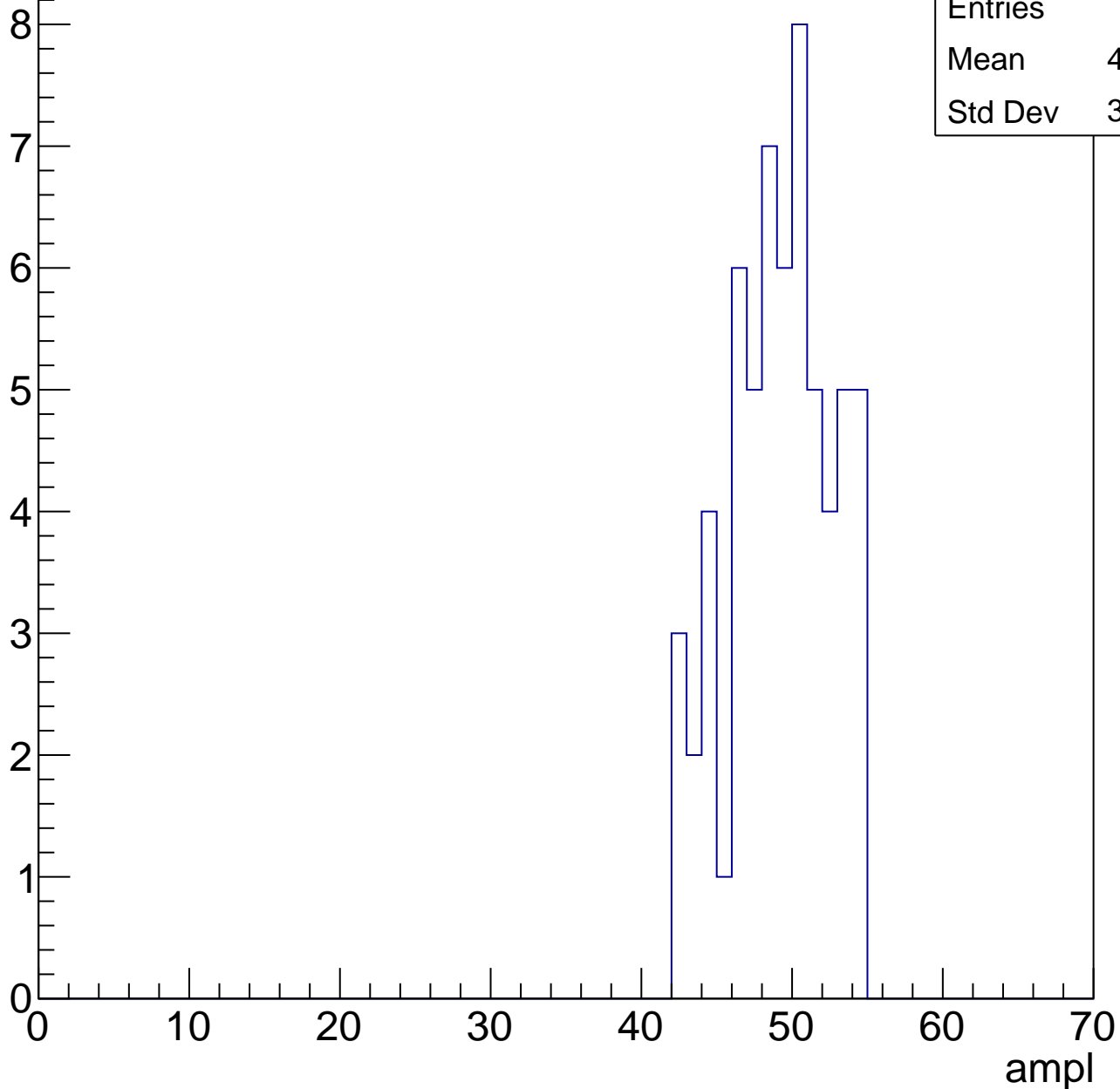


# B1L003S, U11-ch118, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	48.72
Std Dev	3.339

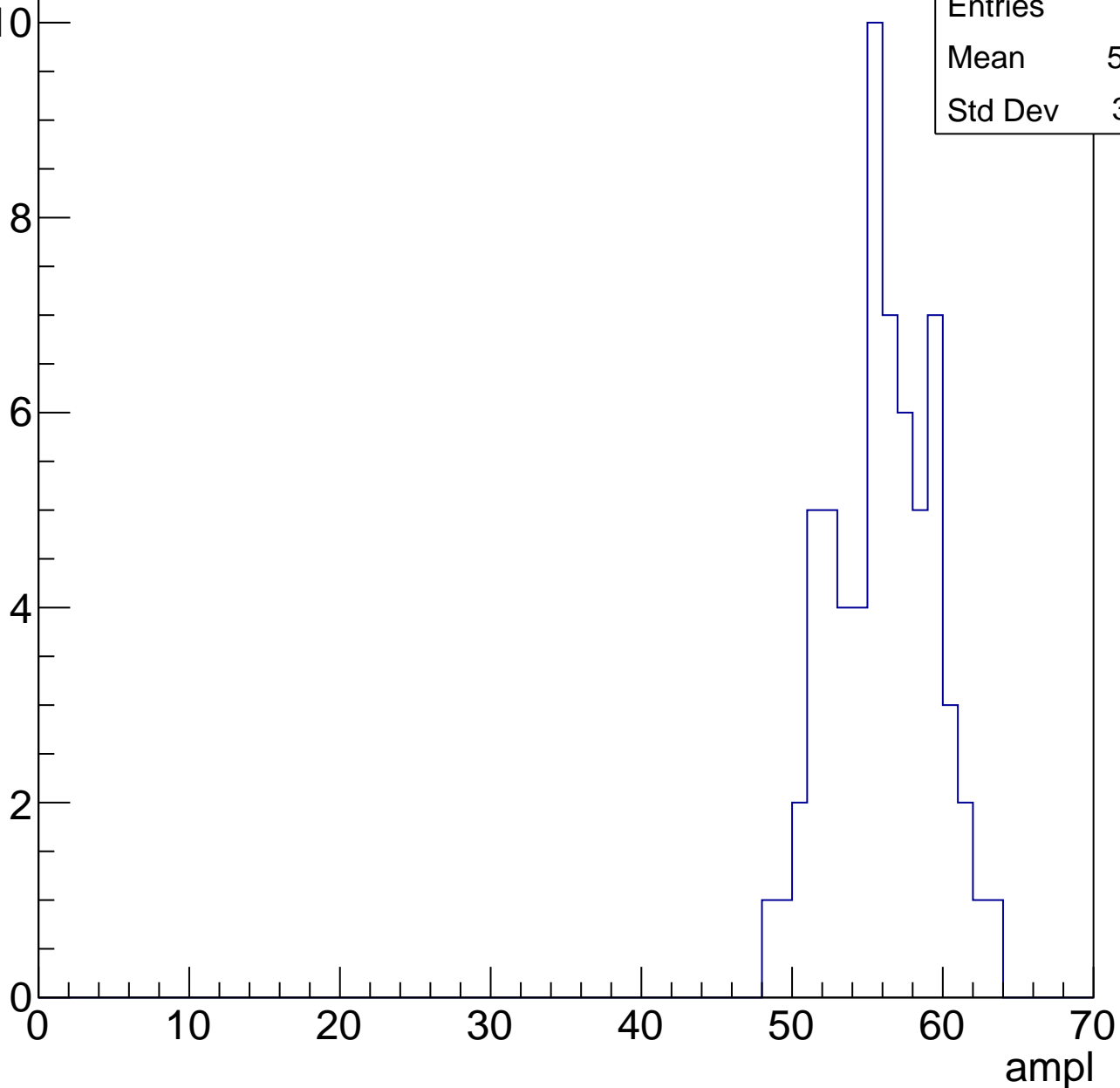


# B1L003S, U11-ch118, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	55.53
Std Dev	3.331

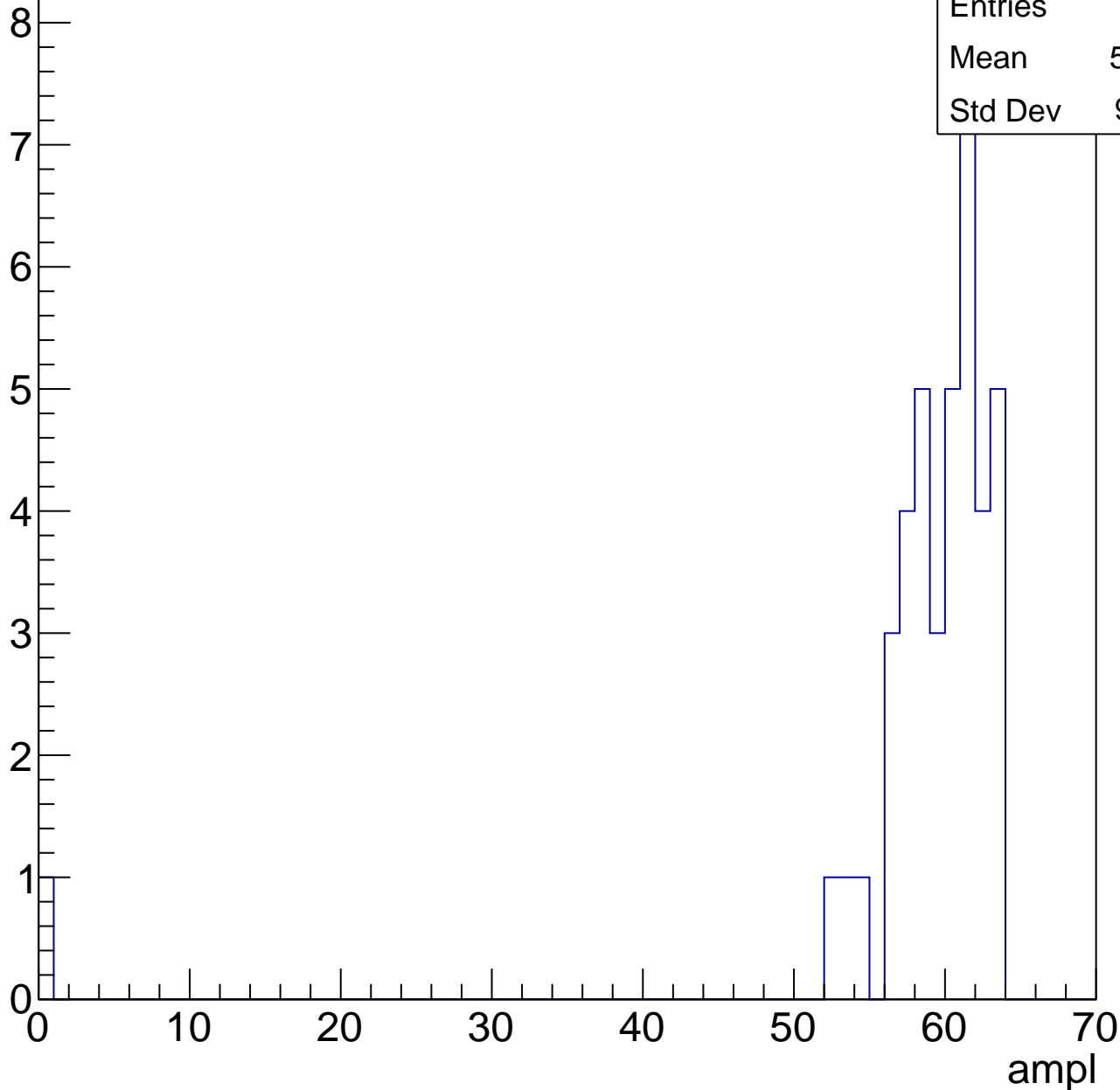


# B1L003S, U11-ch118, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	41
Mean	57.88
Std Dev	9.551

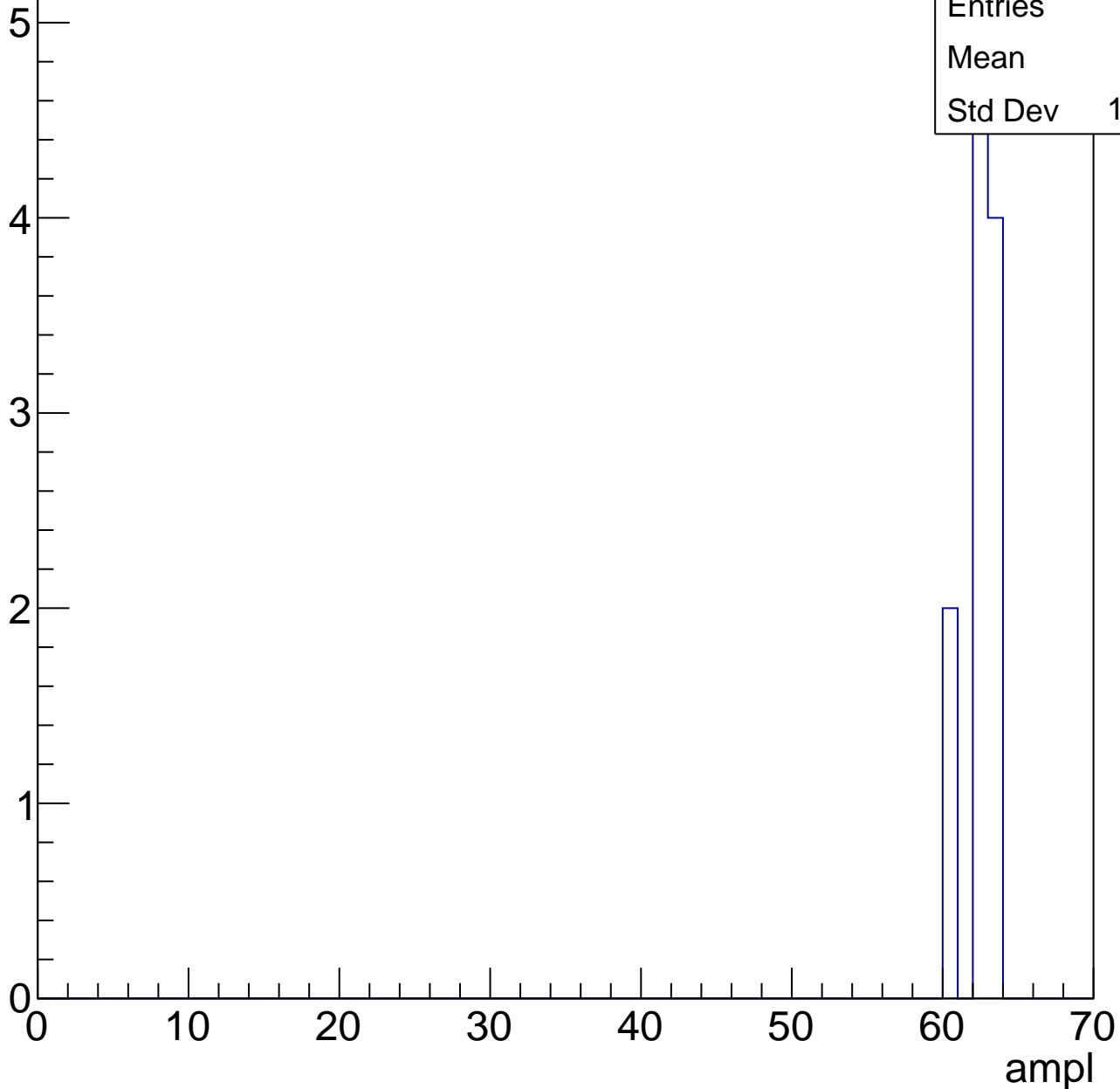


# B1L003S, U11-ch118, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	11
Mean	62
Std Dev	1.044





# B1L003S, U11-ch118, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U11-ch119, adc0

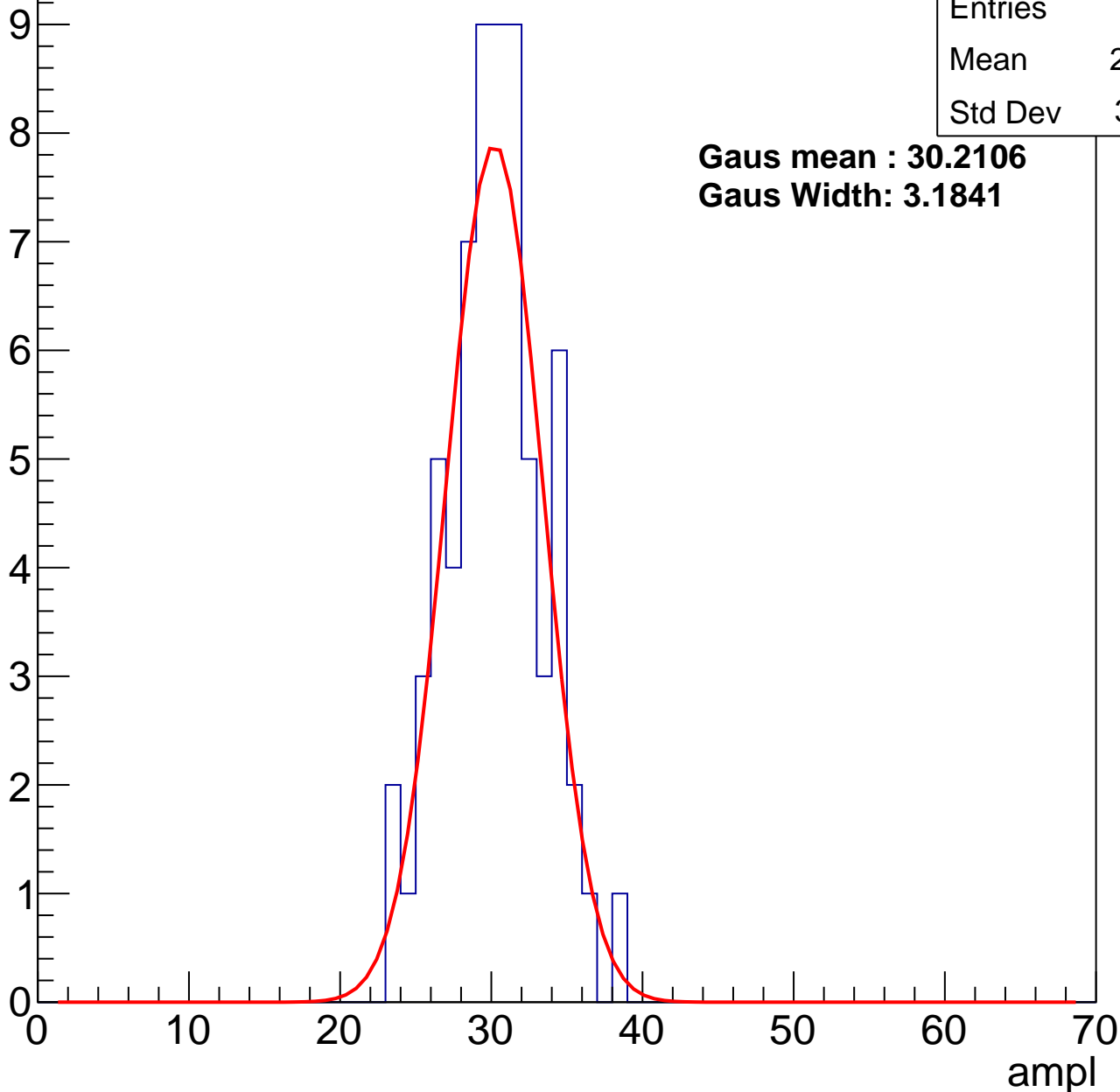
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	29.79
Std Dev	3.141

**Gaus mean : 30.2106**

**Gaus Width: 3.1841**



# B1L003S, U11-ch119, adc1

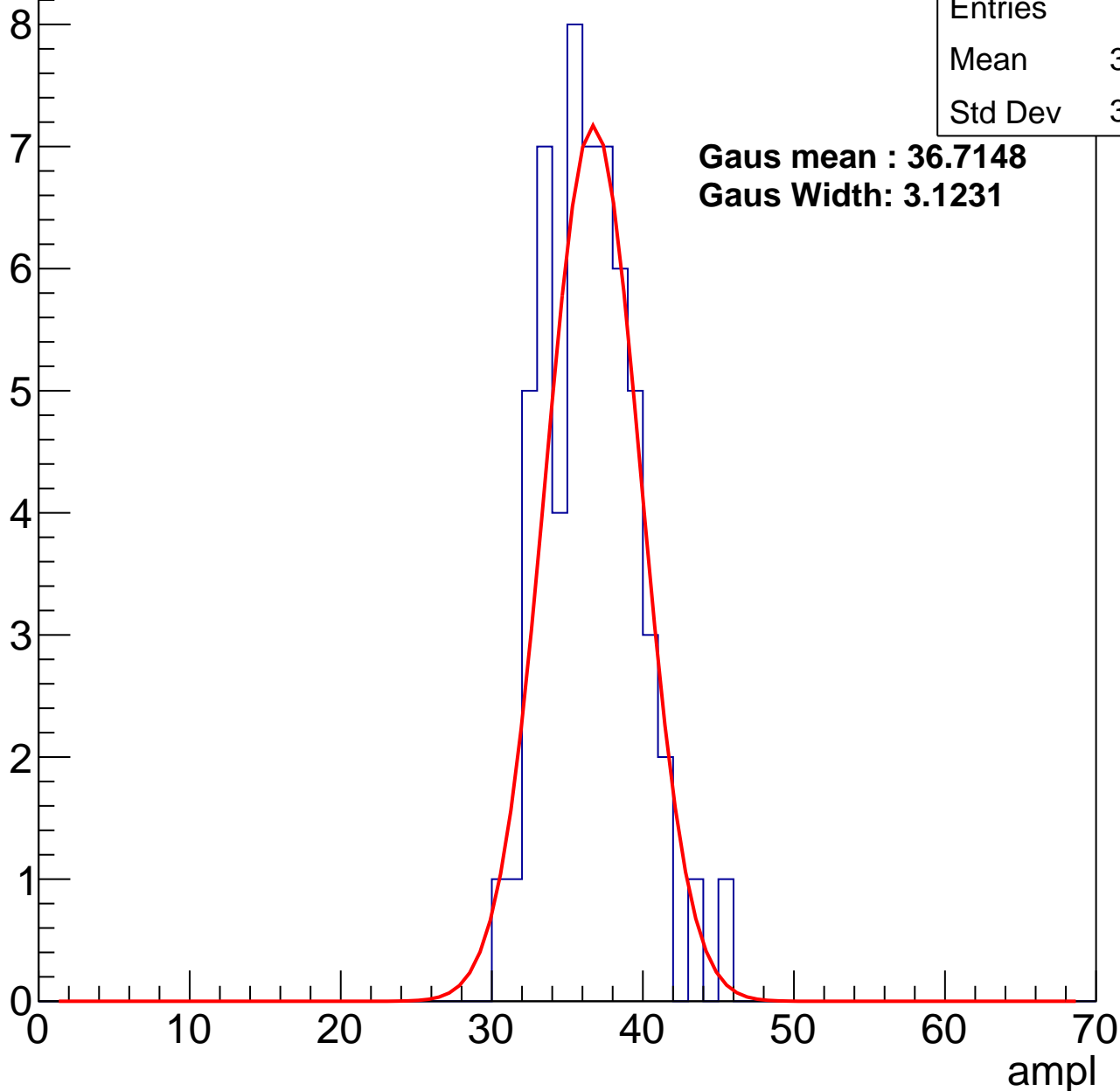
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	36.07
Std Dev	3.028

**Gaus mean : 36.7148**

**Gaus Width: 3.1231**



# B1L003S, U11-ch119, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	77
Mean	42.88
Std Dev	3.56

**Gaus mean : 43.2714**

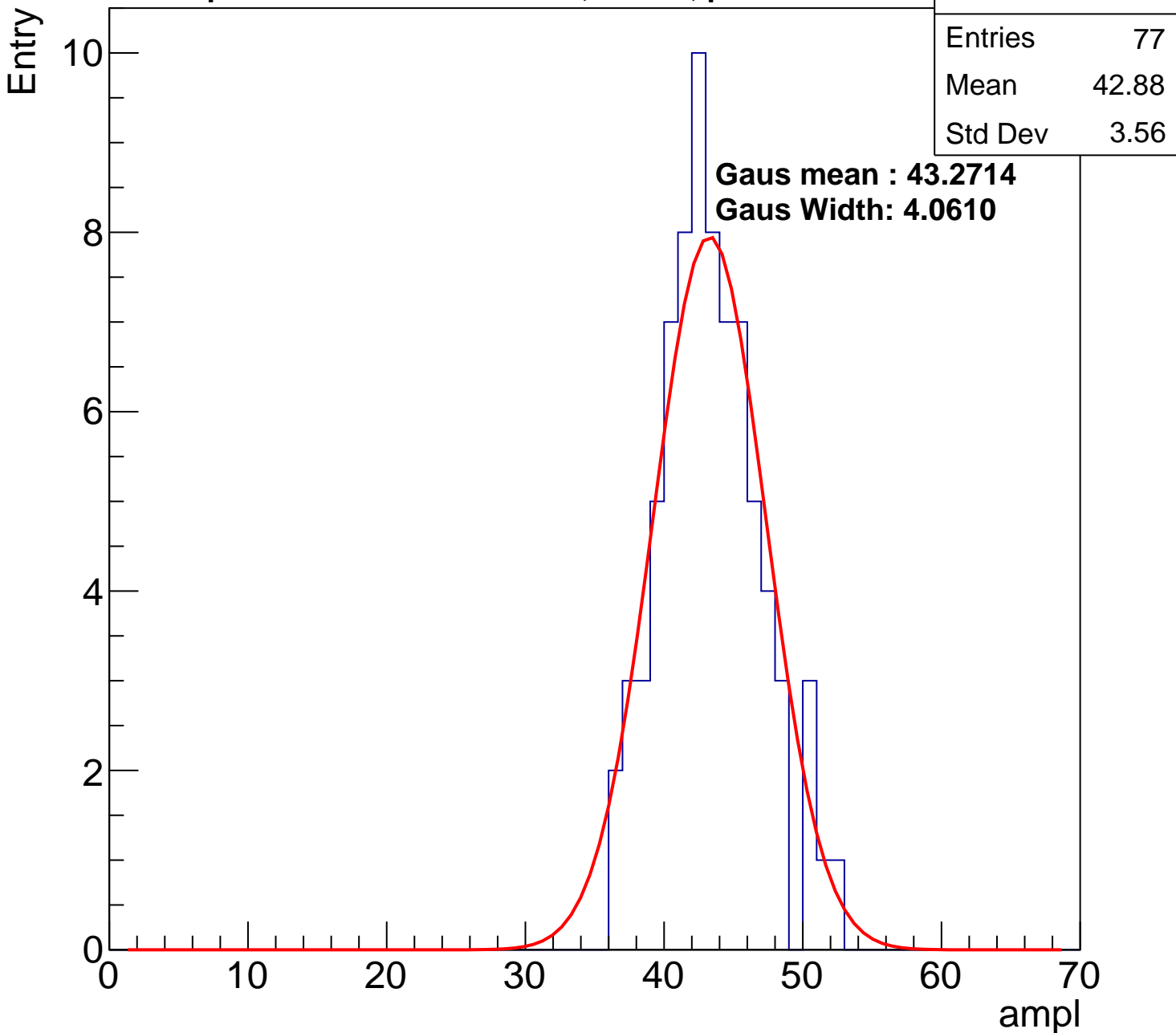
**Gaus Width: 4.0610**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

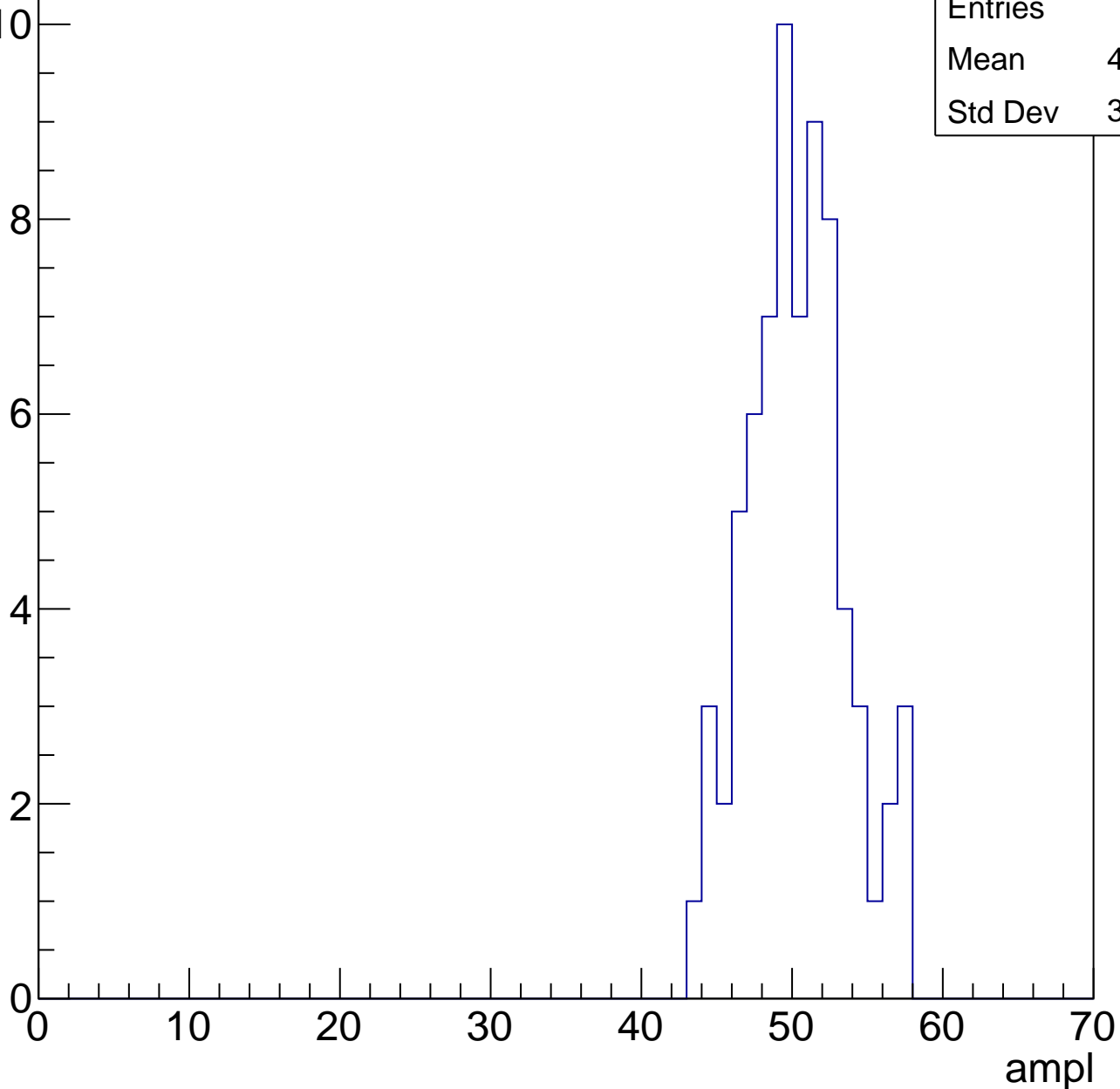


# B1L003S, U11-ch119, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	71
Mean	49.86
Std Dev	3.243

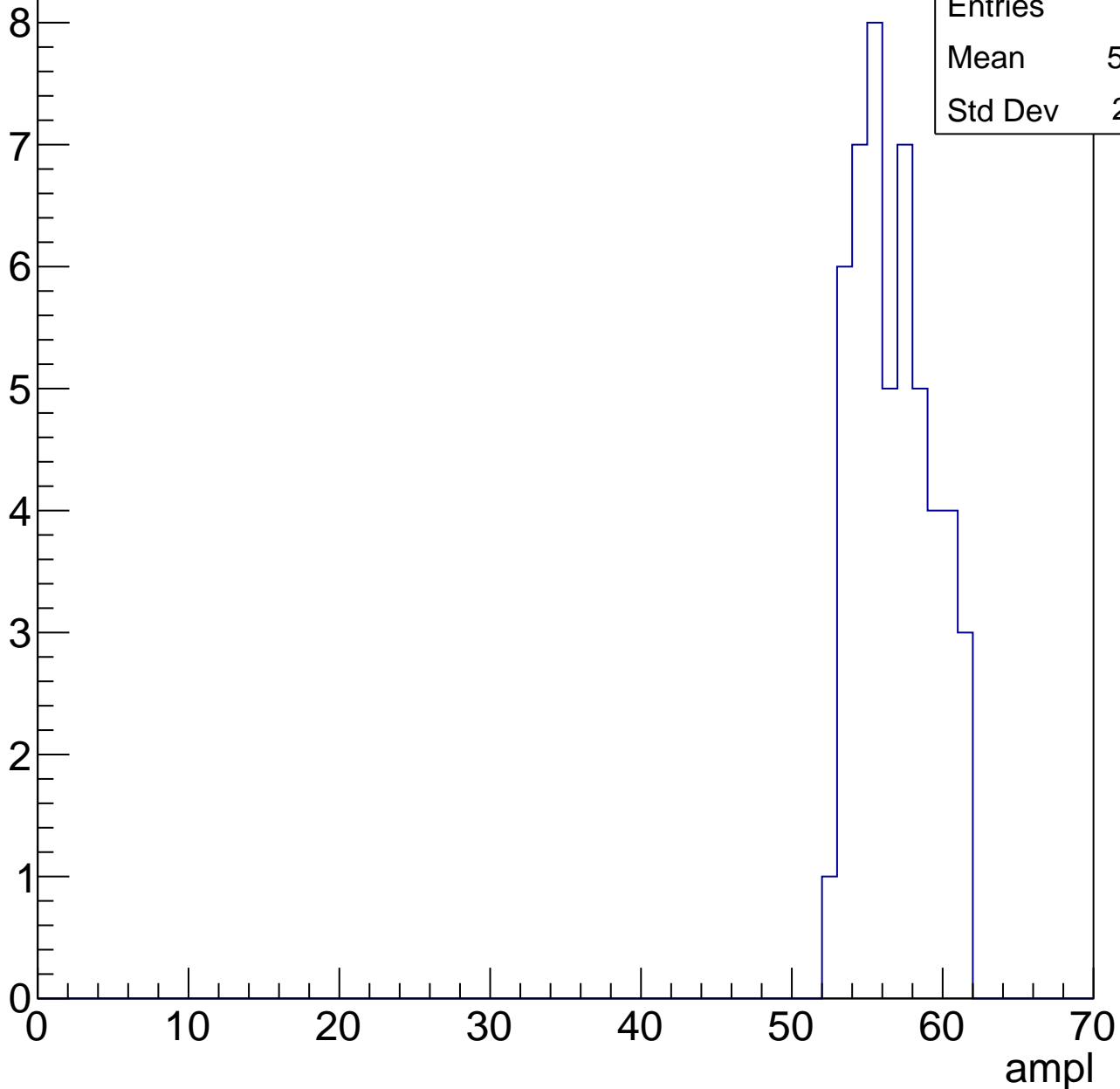


# B1L003S, U11-ch119, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	50
Mean	56.32
Std Dev	2.461

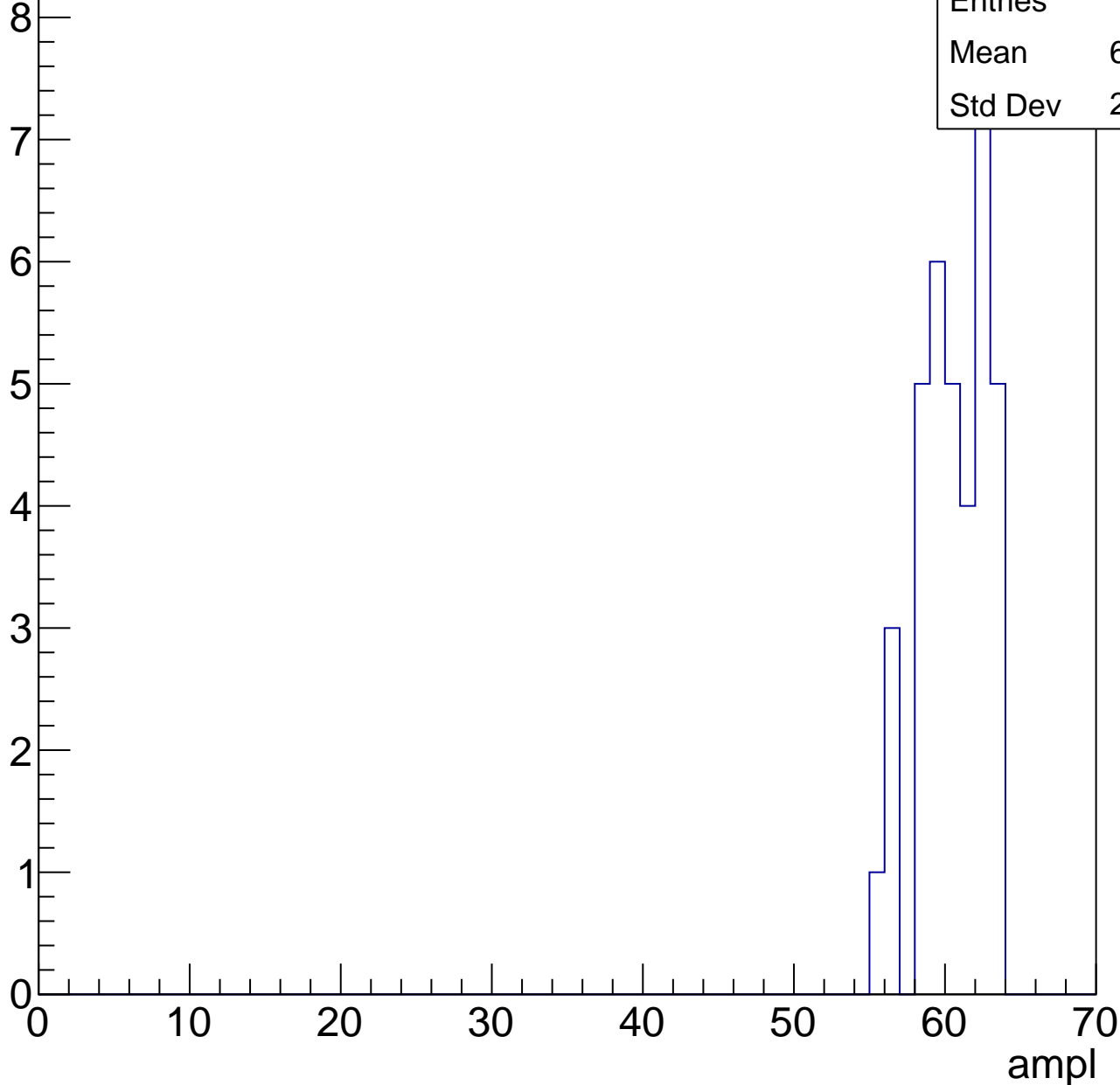


# B1L003S, U11-ch119, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	37
Mean	60.05
Std Dev	2.205

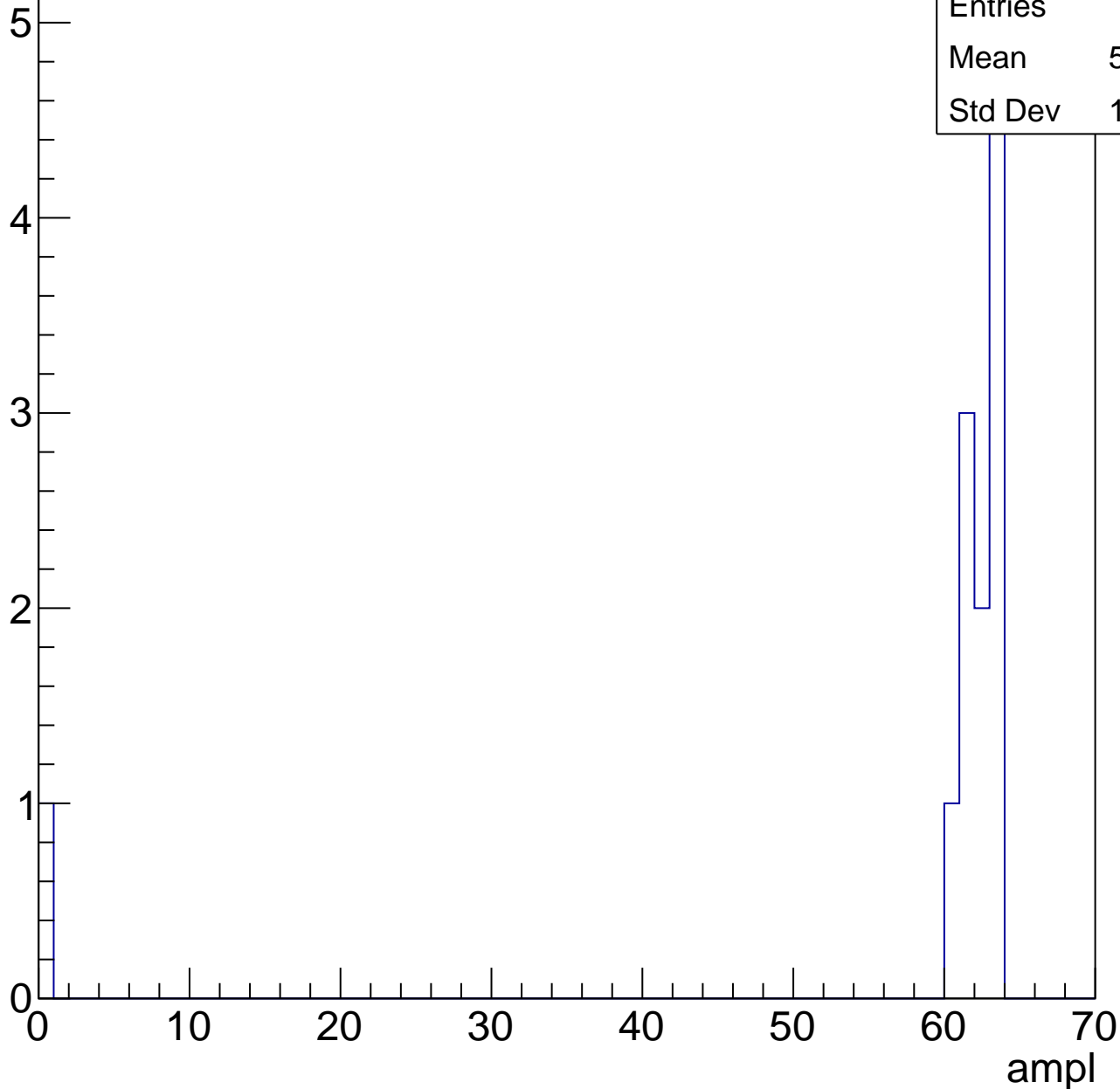


# B1L003S, U11-ch119, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	12
Mean	56.83
Std Dev	17.17





# B1L003S, U11-ch119, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L003S, U11-ch120, adc0

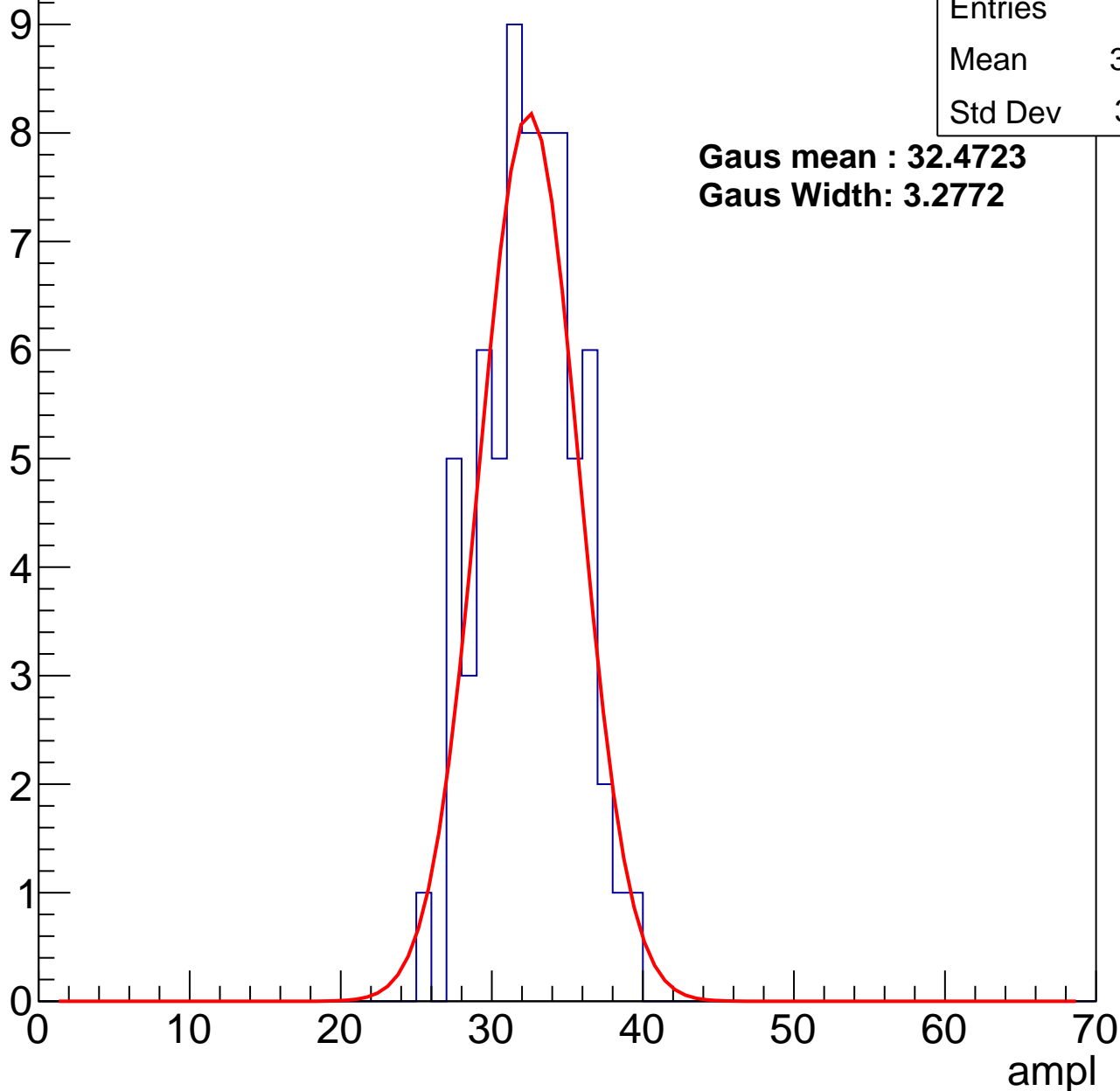
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	32.07
Std Dev	3.021

**Gaus mean : 32.4723**

**Gaus Width: 3.2772**



# B1L003S, U11-ch120, adc1

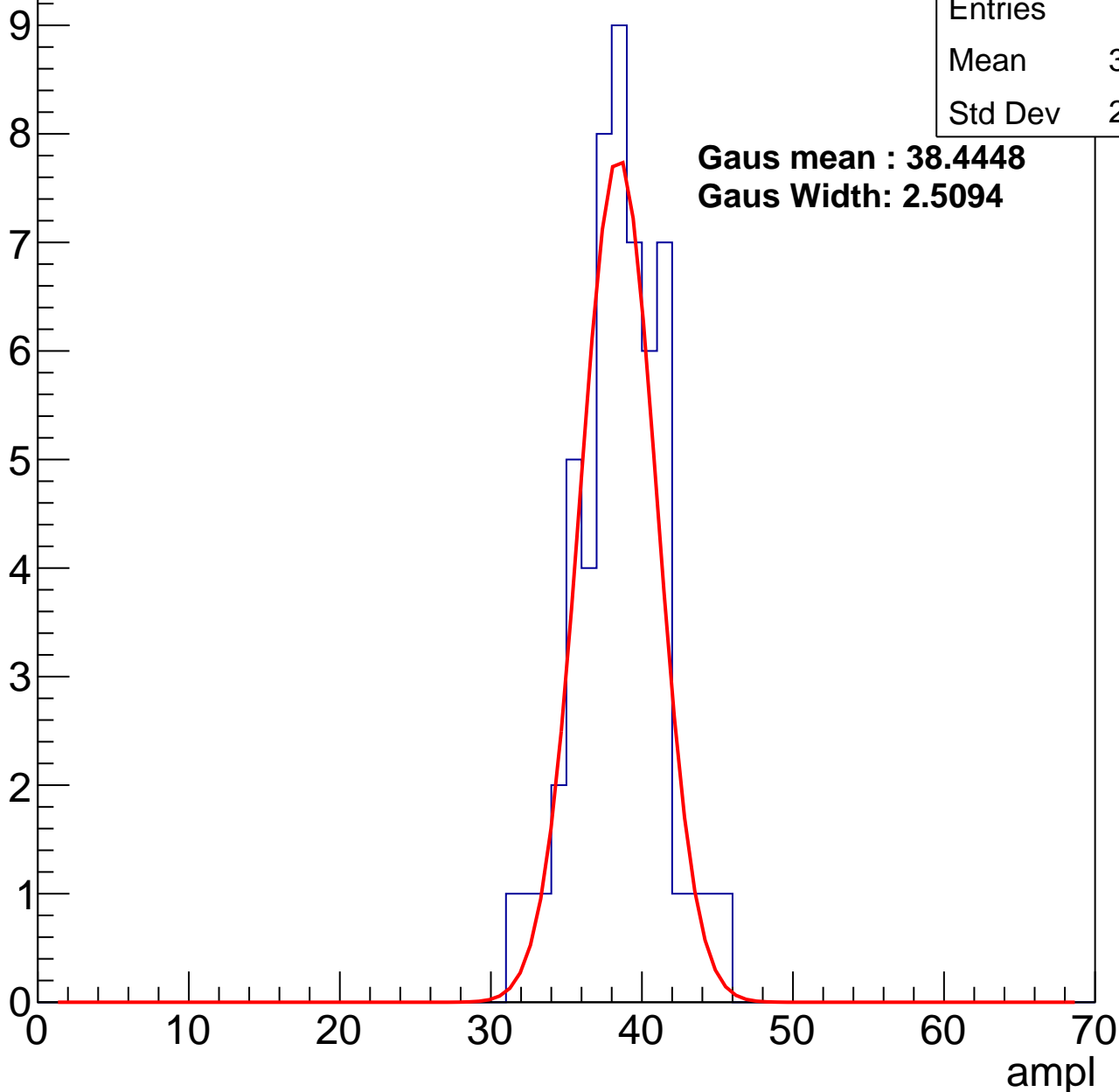
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	38.09
Std Dev	2.798

**Gaus mean : 38.4448**

**Gaus Width: 2.5094**



# B1L003S, U11-ch120, adc2

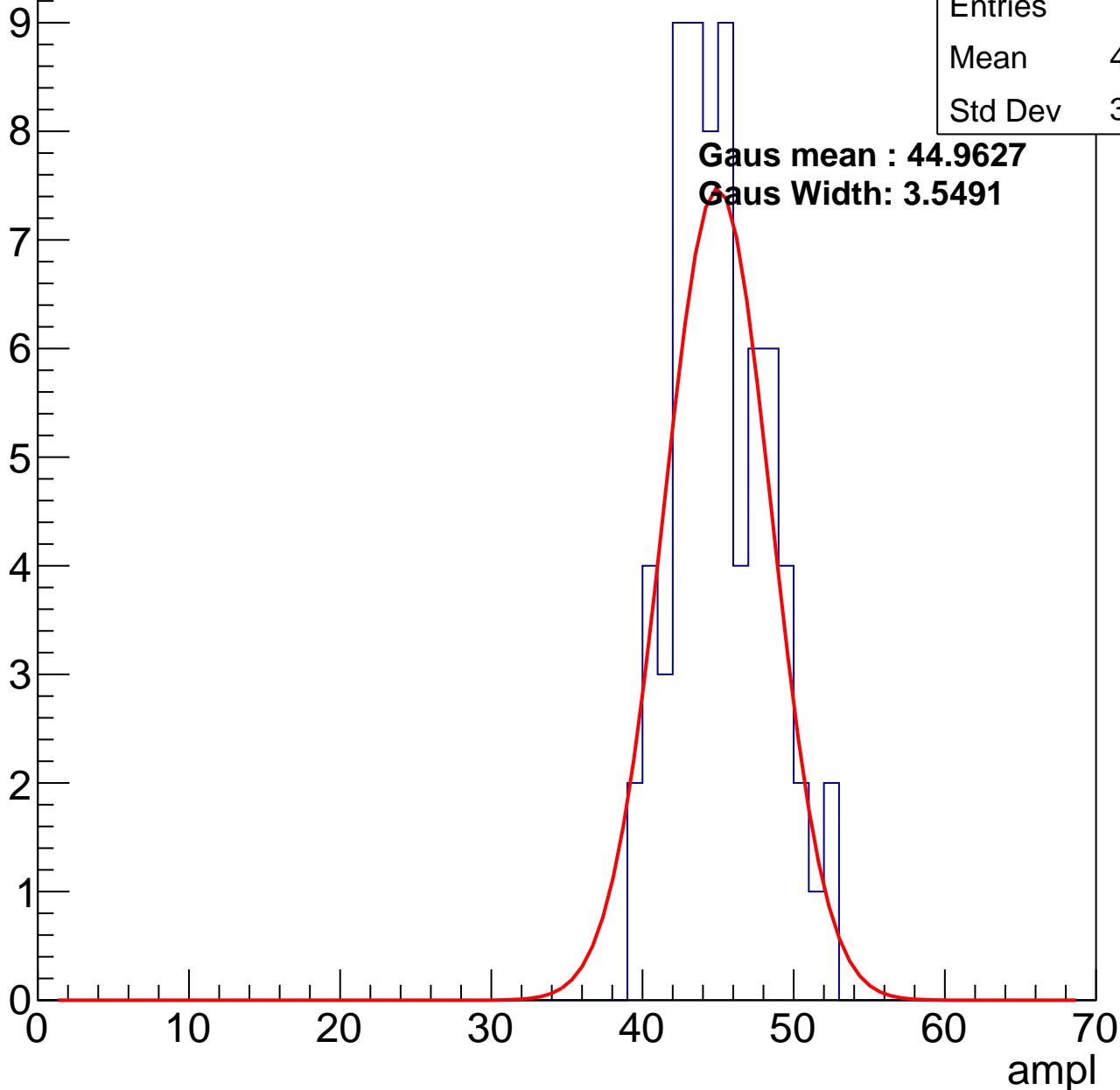
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	44.75
Std Dev	3.118

**Gaus mean : 44.9627**

**Gaus Width: 3.5491**

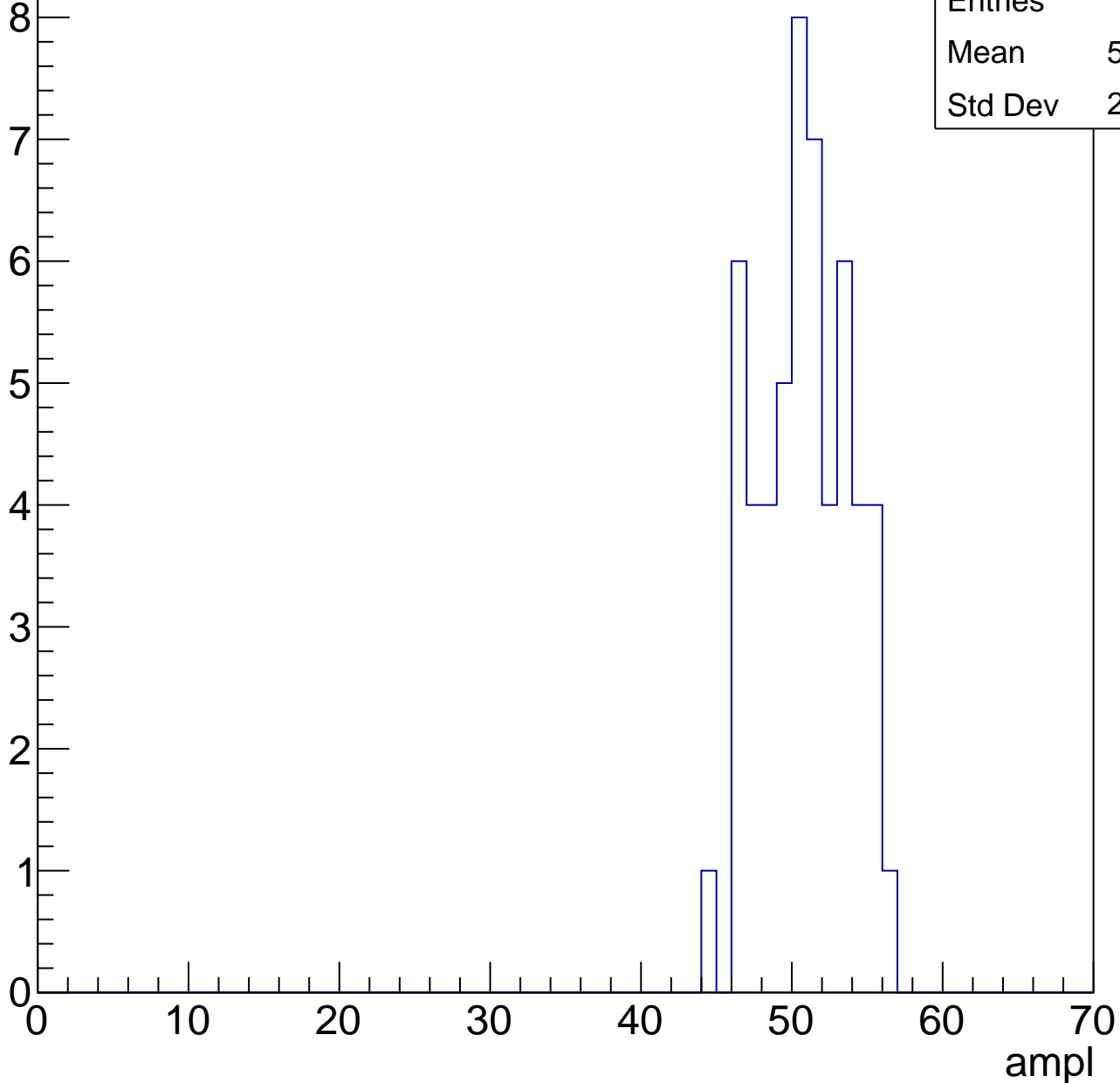


# B1L003S, U11-ch120, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	54
Mean	50.37
Std Dev	2.914

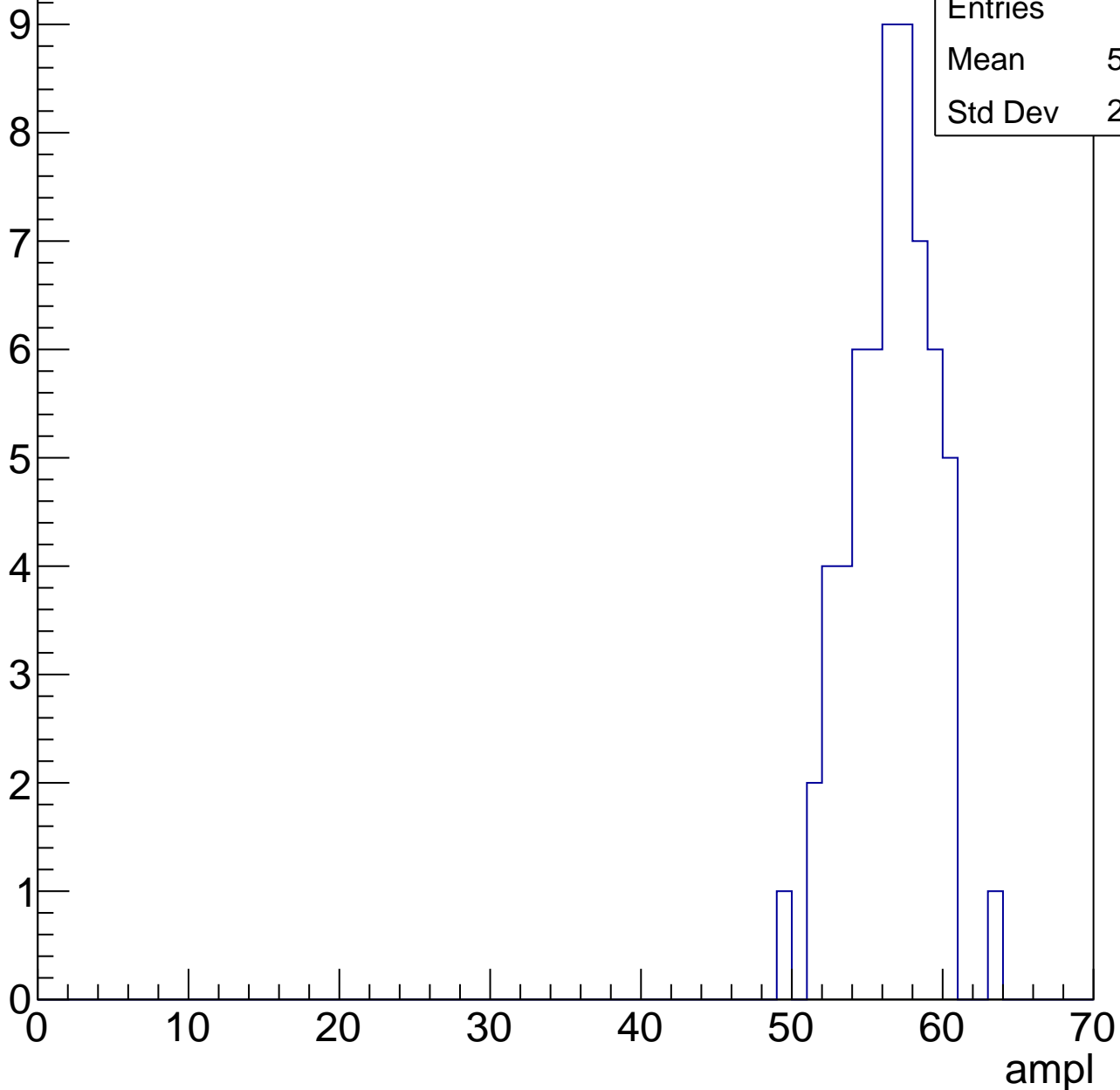


# B1L003S, U11-ch120, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

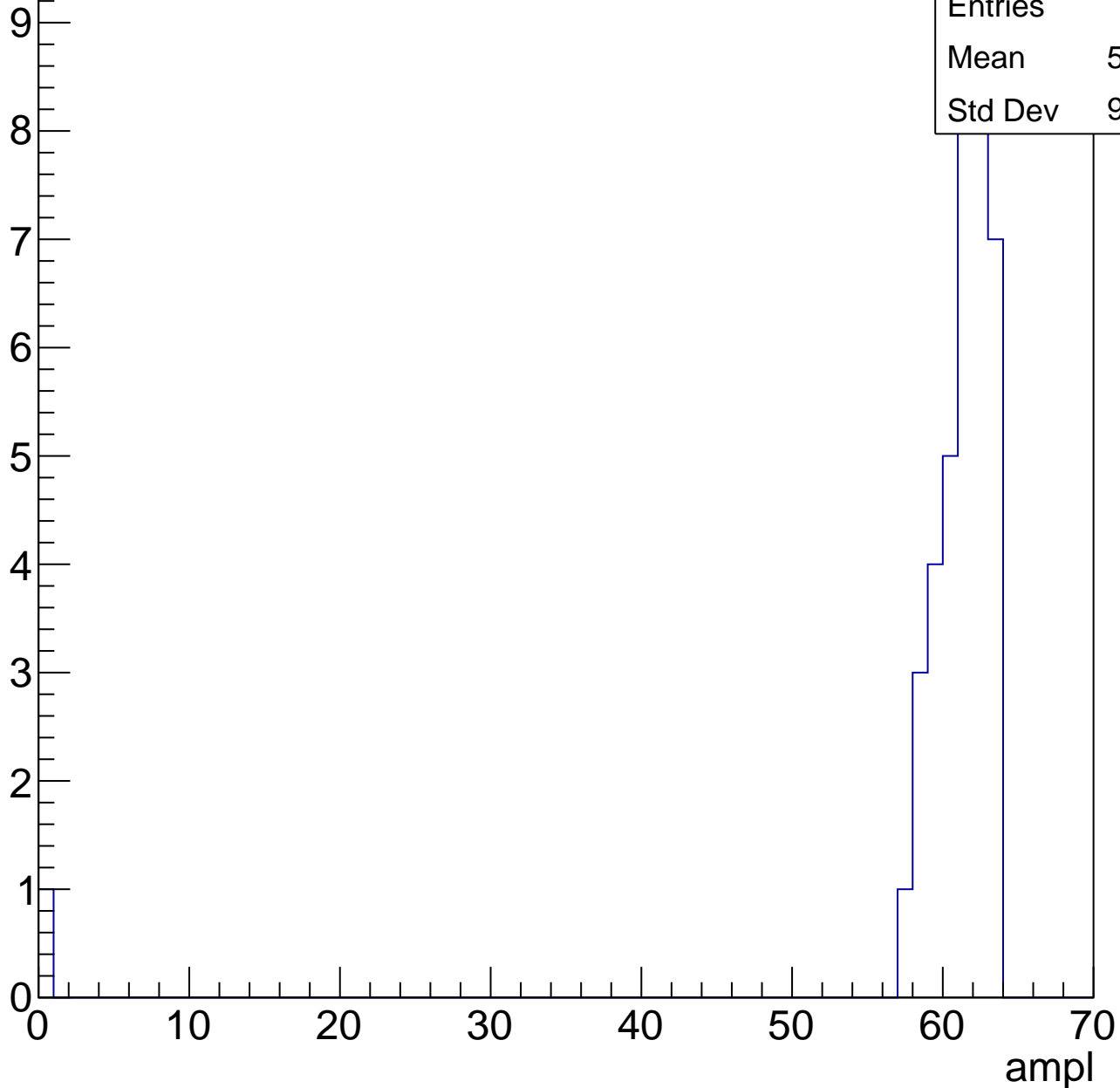
Entries	60
Mean	56.08
Std Dev	2.734



# B1L003S, U11-ch120, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

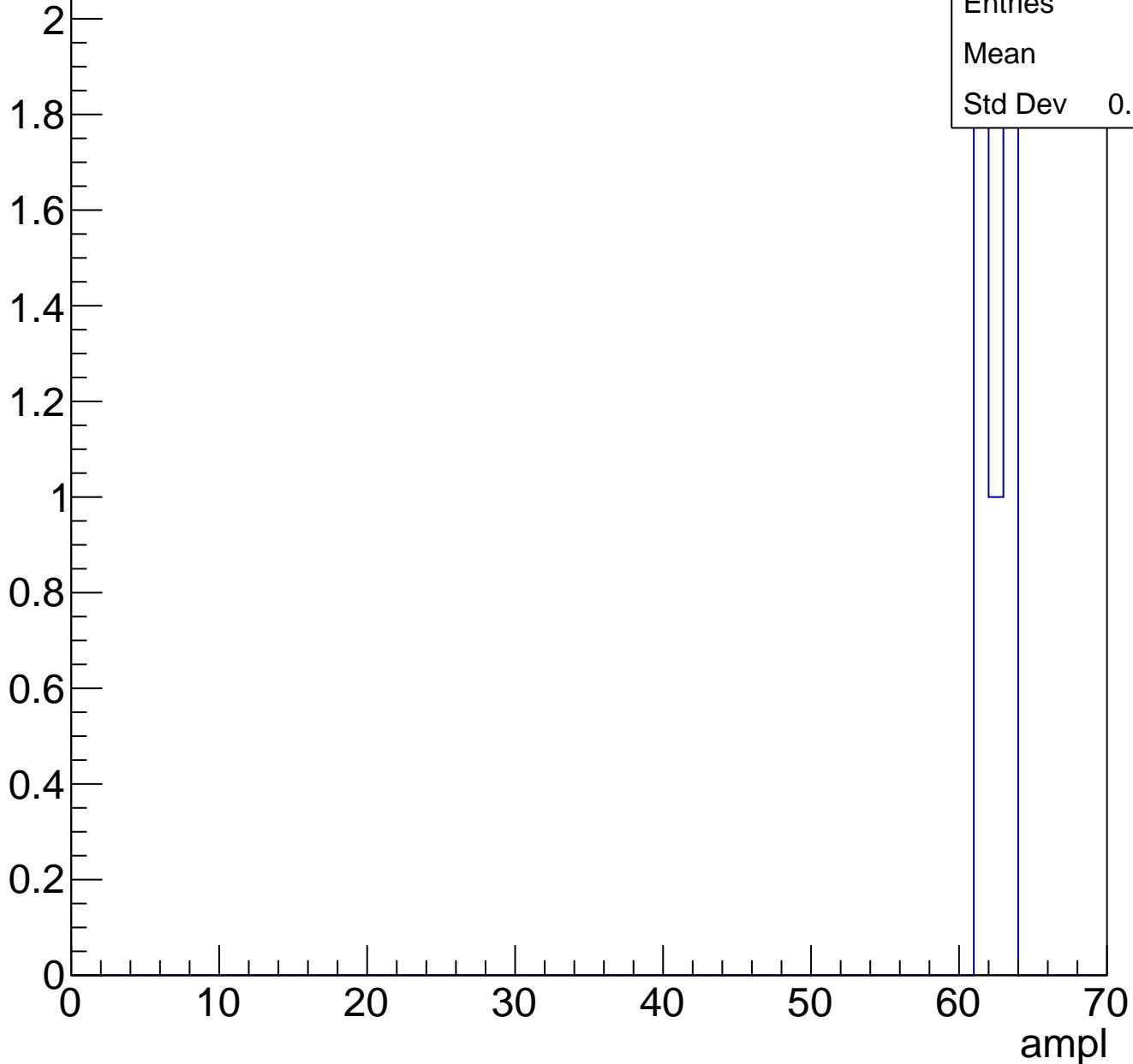
Entry



# B1L003S, U11-ch120, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch120, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	12.5
Std Dev	12.5

# B1L003S, U11-ch121, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	96
Mean	28.74
Std Dev	3.922

**Gaus mean : 29.4812**

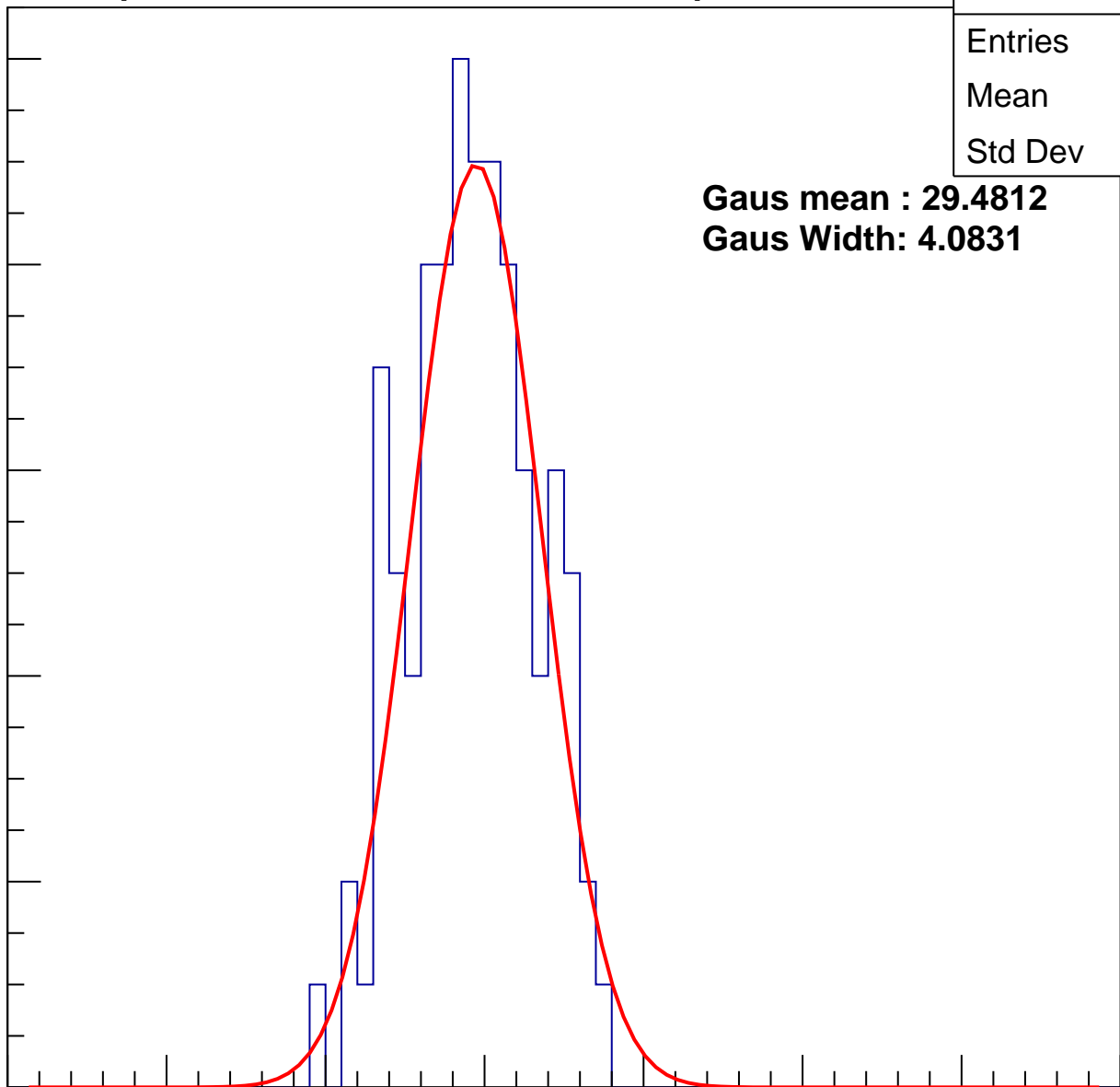
**Gaus Width: 4.0831**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U11-ch121, adc1

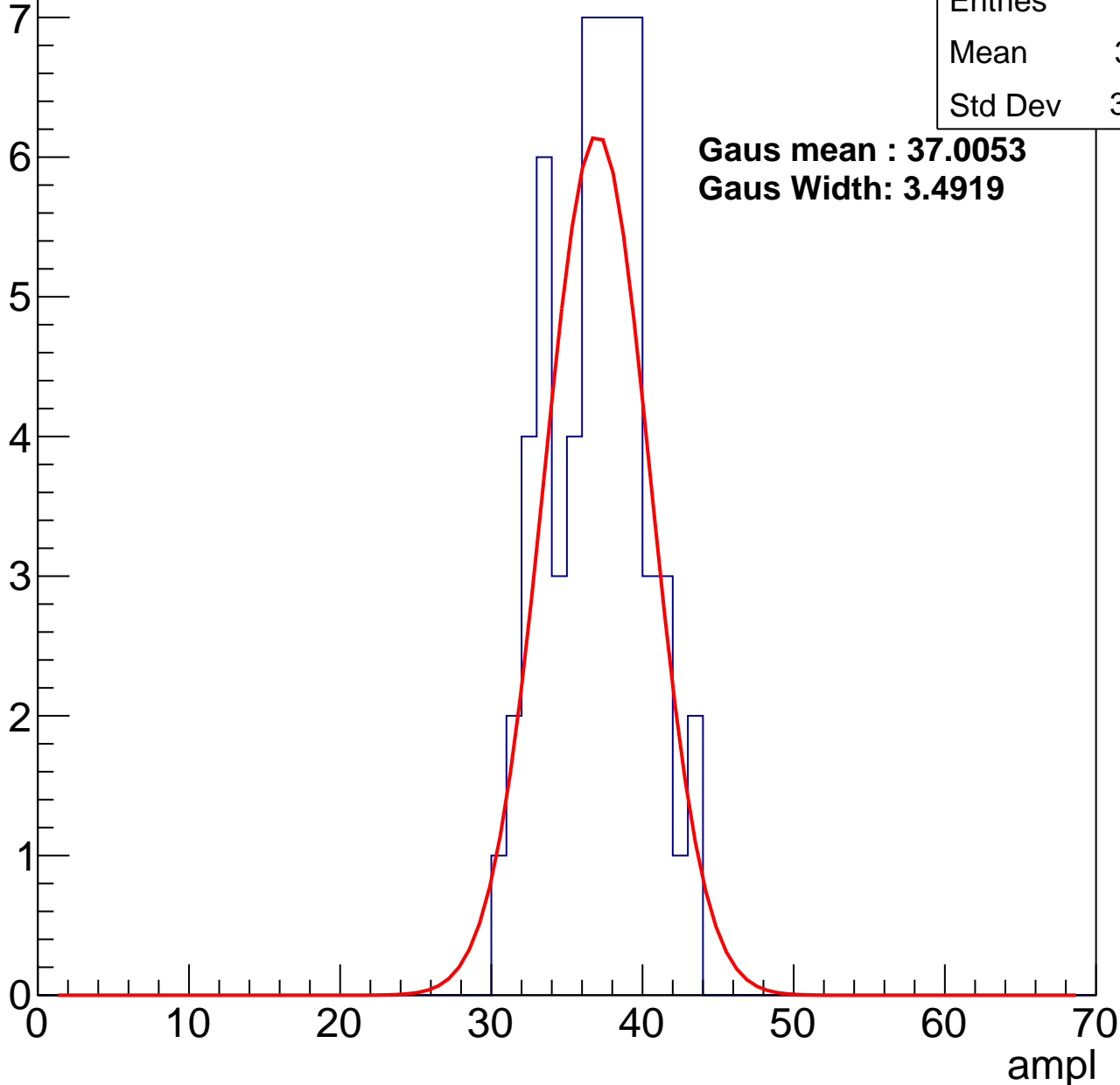
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	36.51
Std Dev	3.135

**Gaus mean : 37.0053**

**Gaus Width: 3.4919**



# B1L003S, U11-ch121, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	71
Mean	42.65
Std Dev	3.328

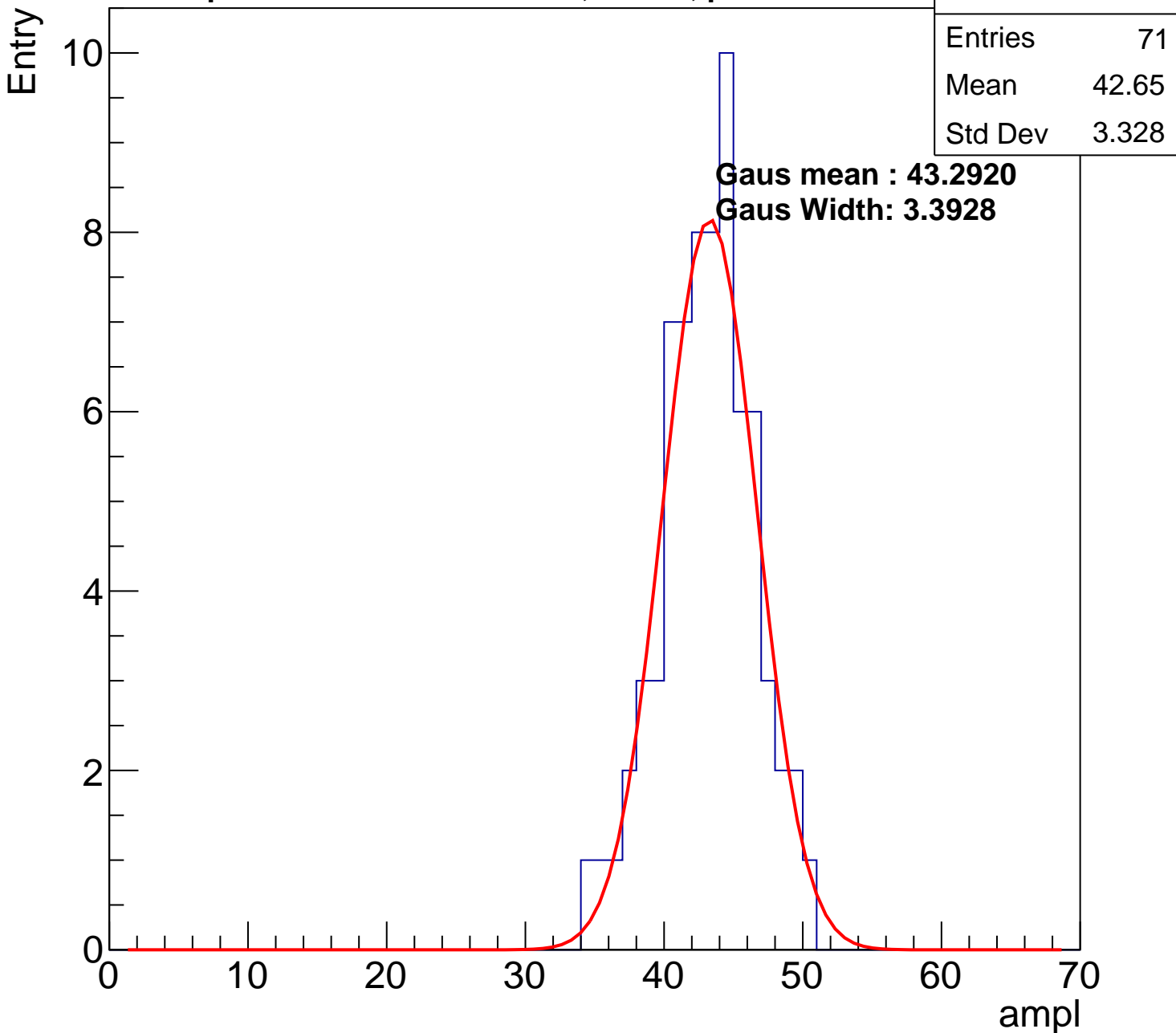
**Gaus mean : 43.2920**

**Gaus Width: 3.3928**

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

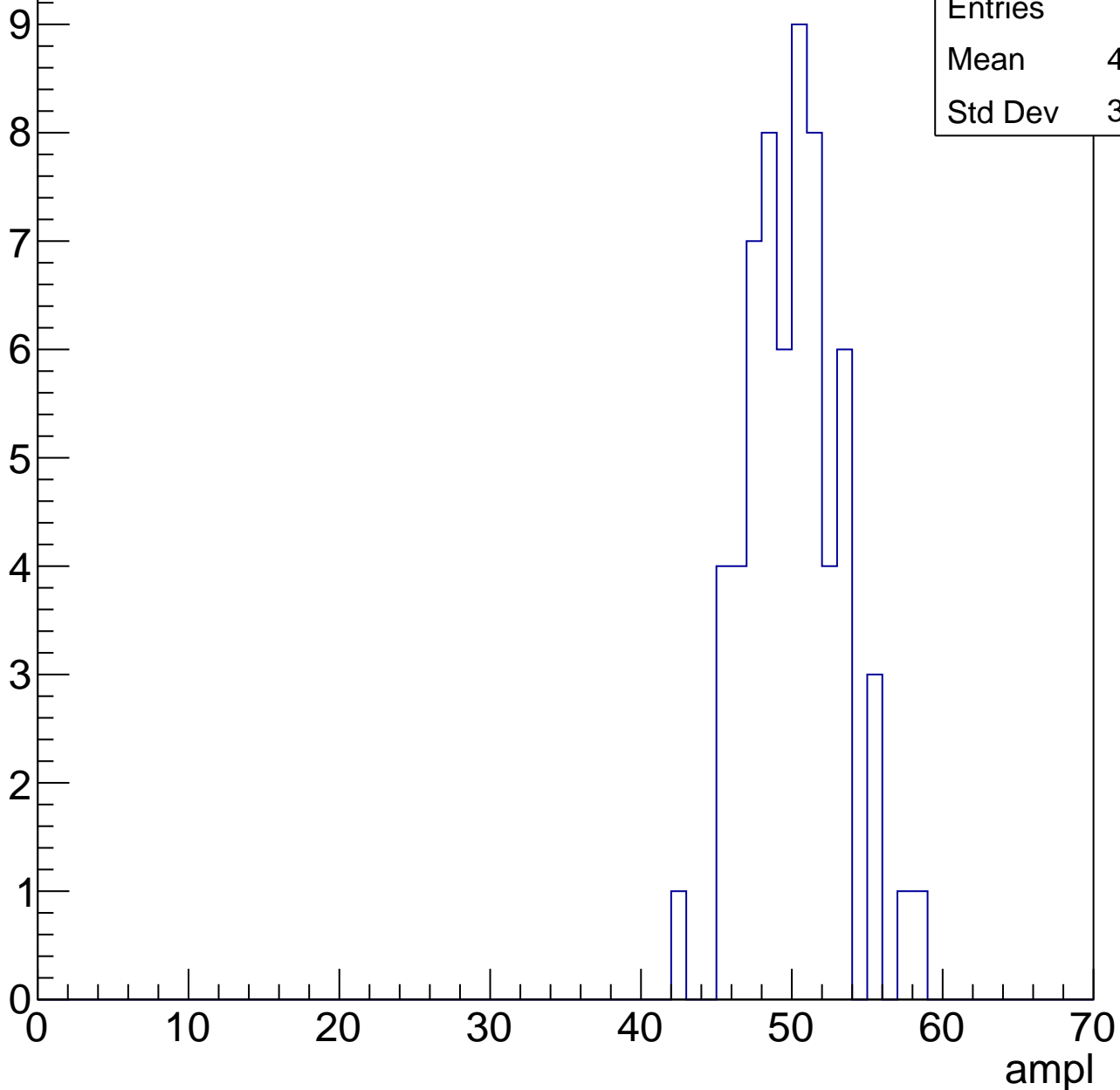


# B1L003S, U11-ch121, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	49.63
Std Dev	3.076

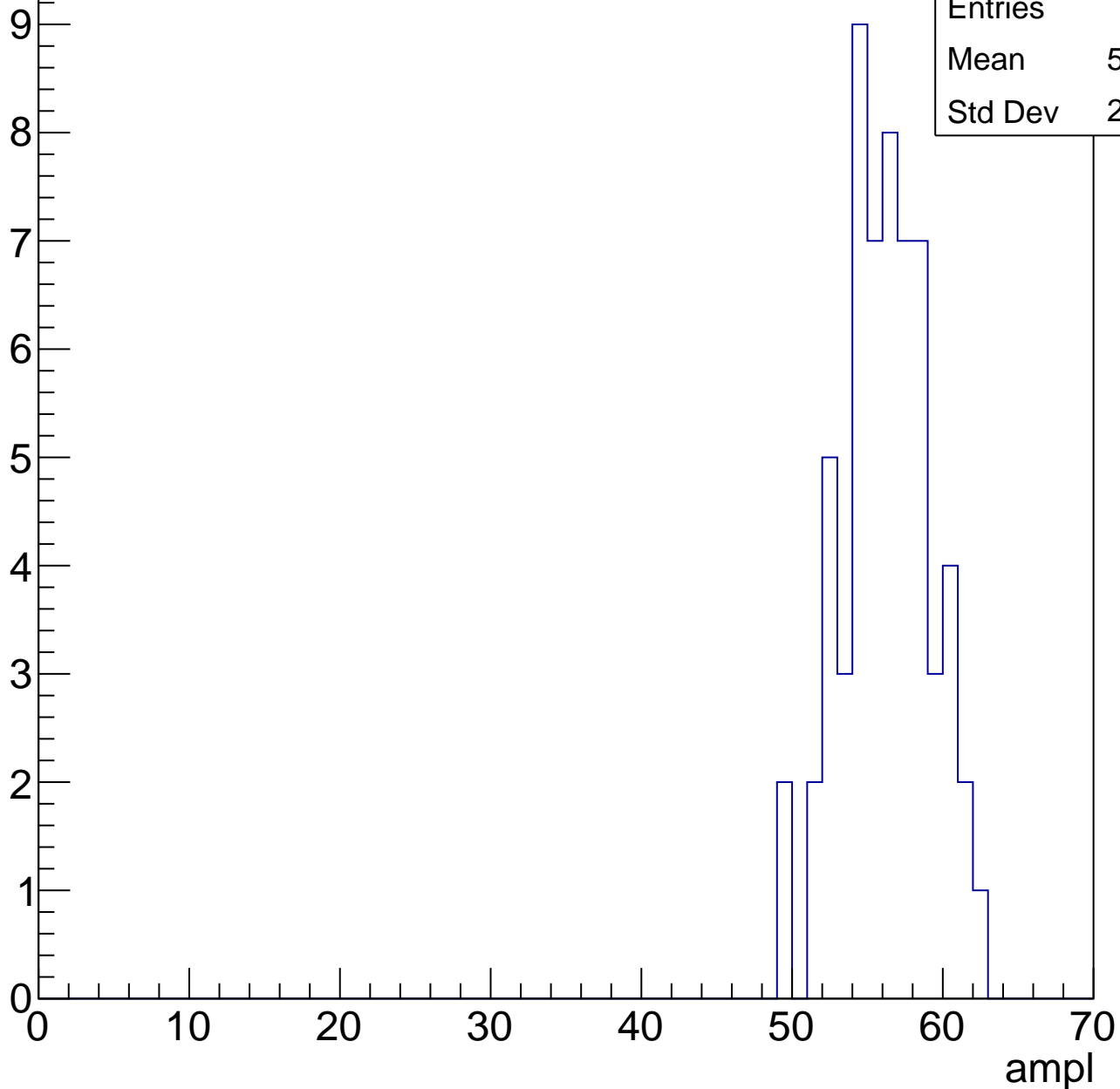


# B1L003S, U11-ch121, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	55.73
Std Dev	2.903

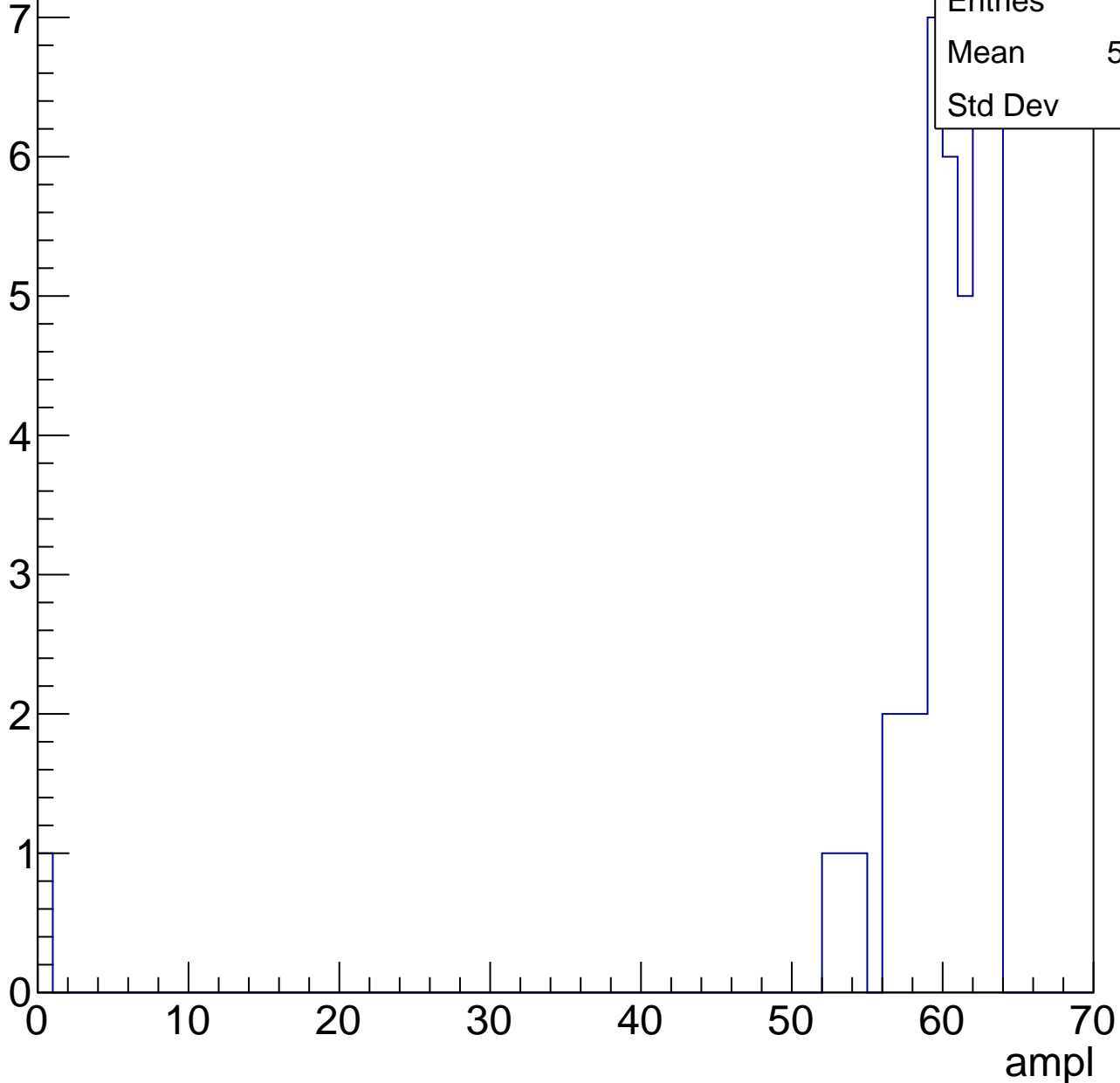


# B1L003S, U11-ch121, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

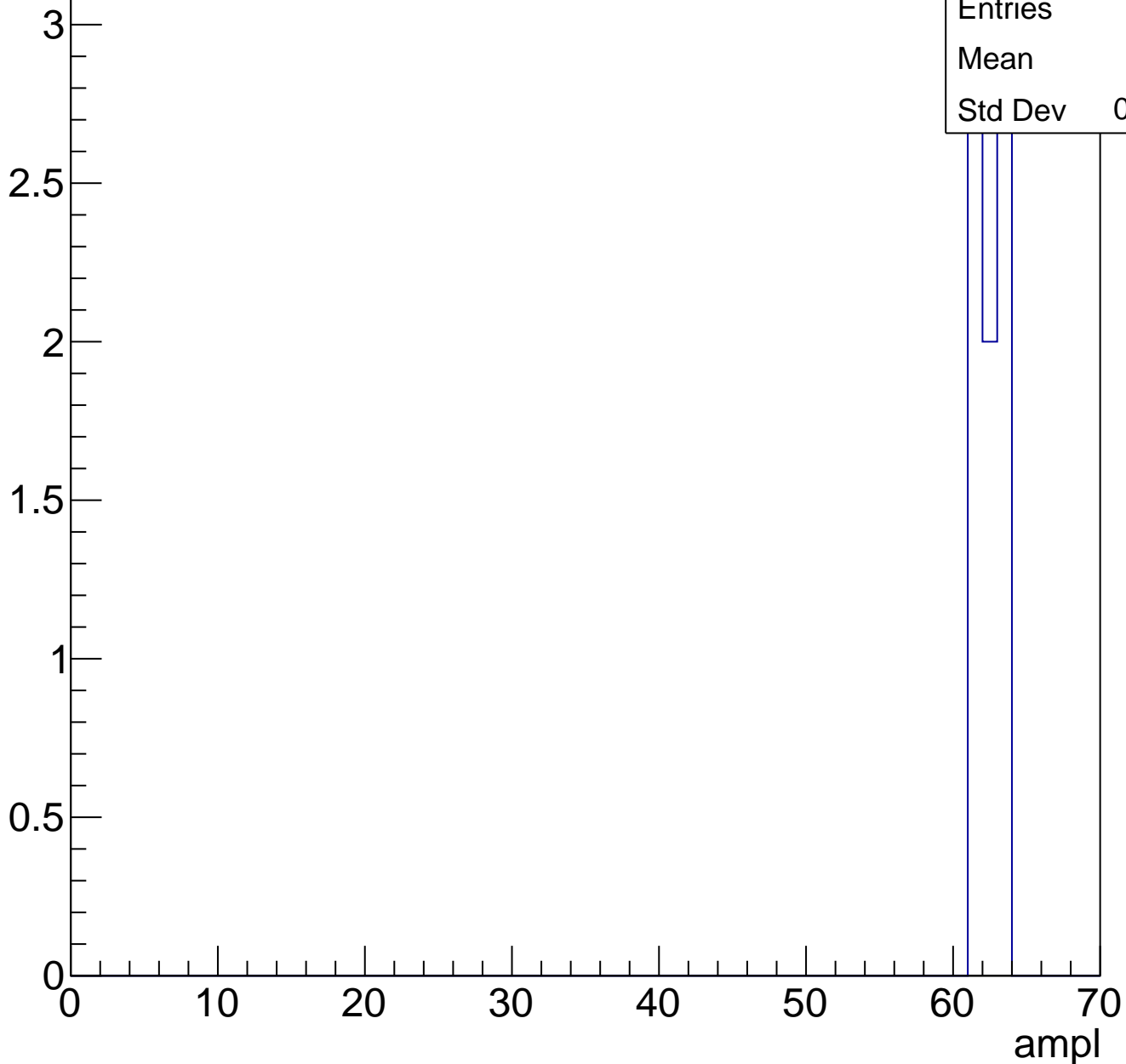
Entries	42
Mean	58.43
Std Dev	9.52



# B1L003S, U11-ch121, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch121, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U11-ch122, adc0

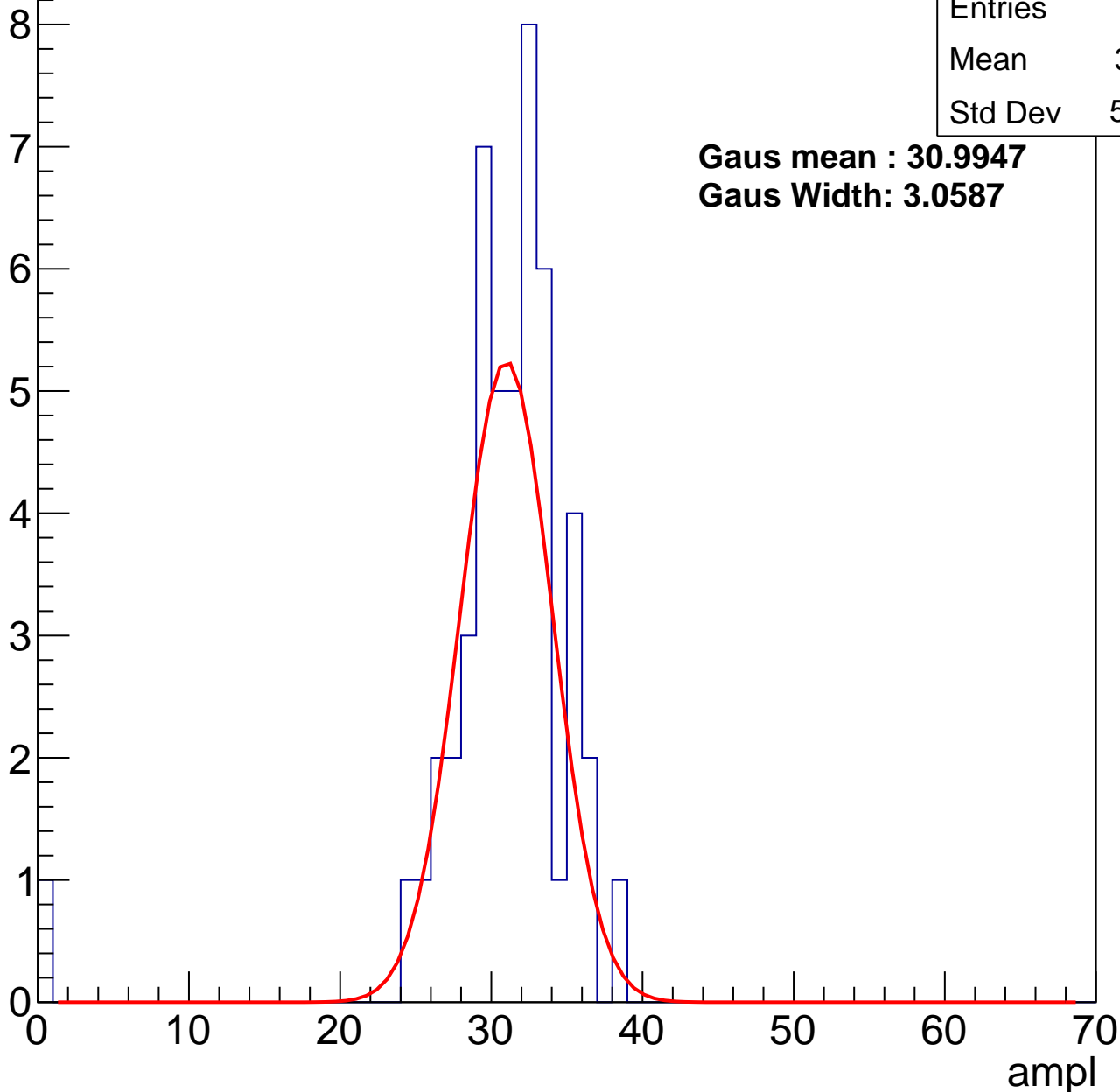
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	49
Mean	30.31
Std Dev	5.285

**Gaus mean : 30.9947**

**Gaus Width: 3.0587**



# B1L003S, U11-ch122, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	85
Mean	37.54
Std Dev	3.493

**Gaus mean : 38.0311**

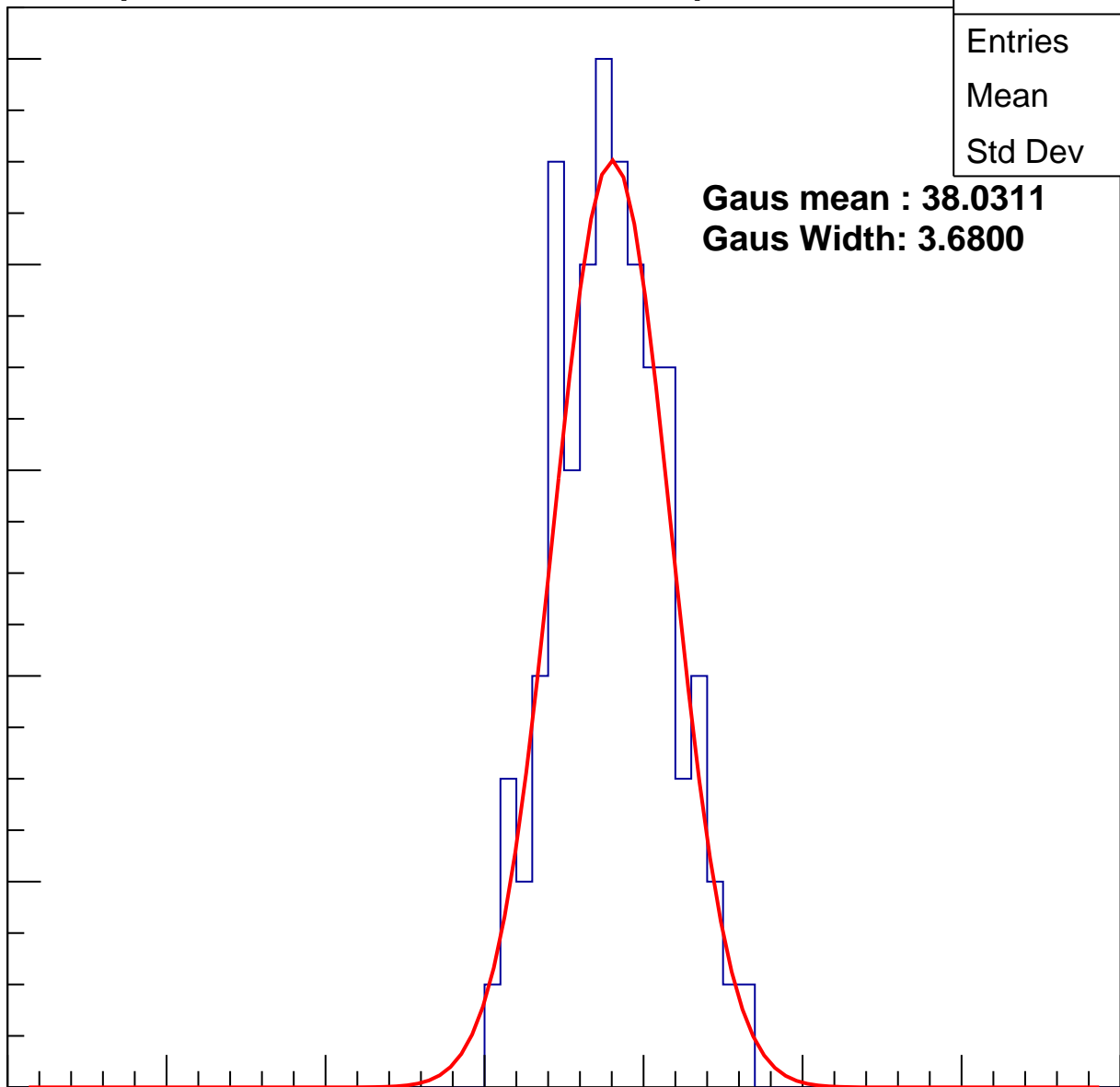
**Gaus Width: 3.6800**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U11-ch122, adc2

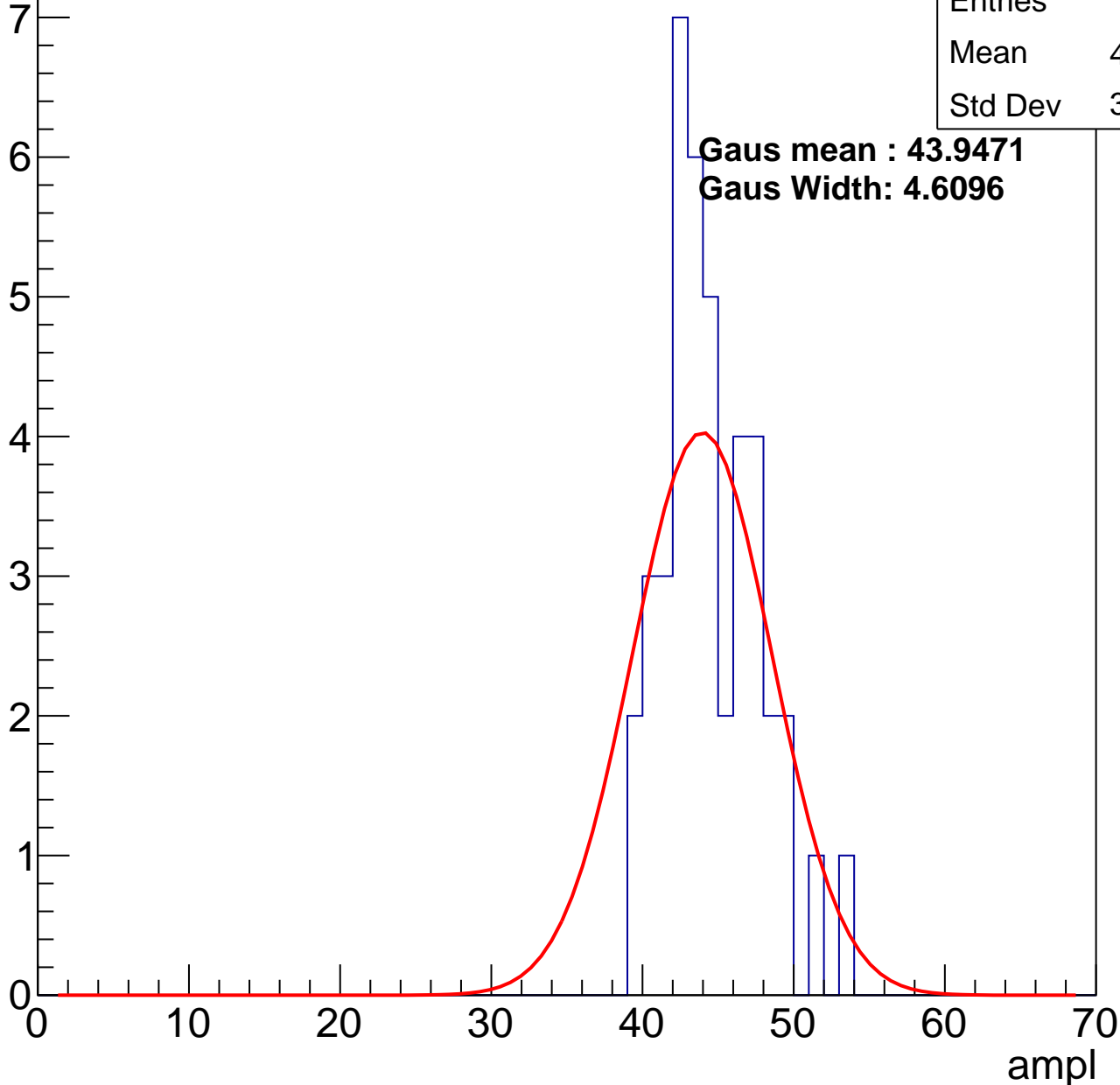
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	42
Mean	44.12
Std Dev	3.179

**Gaus mean : 43.9471**

**Gaus Width: 4.6096**

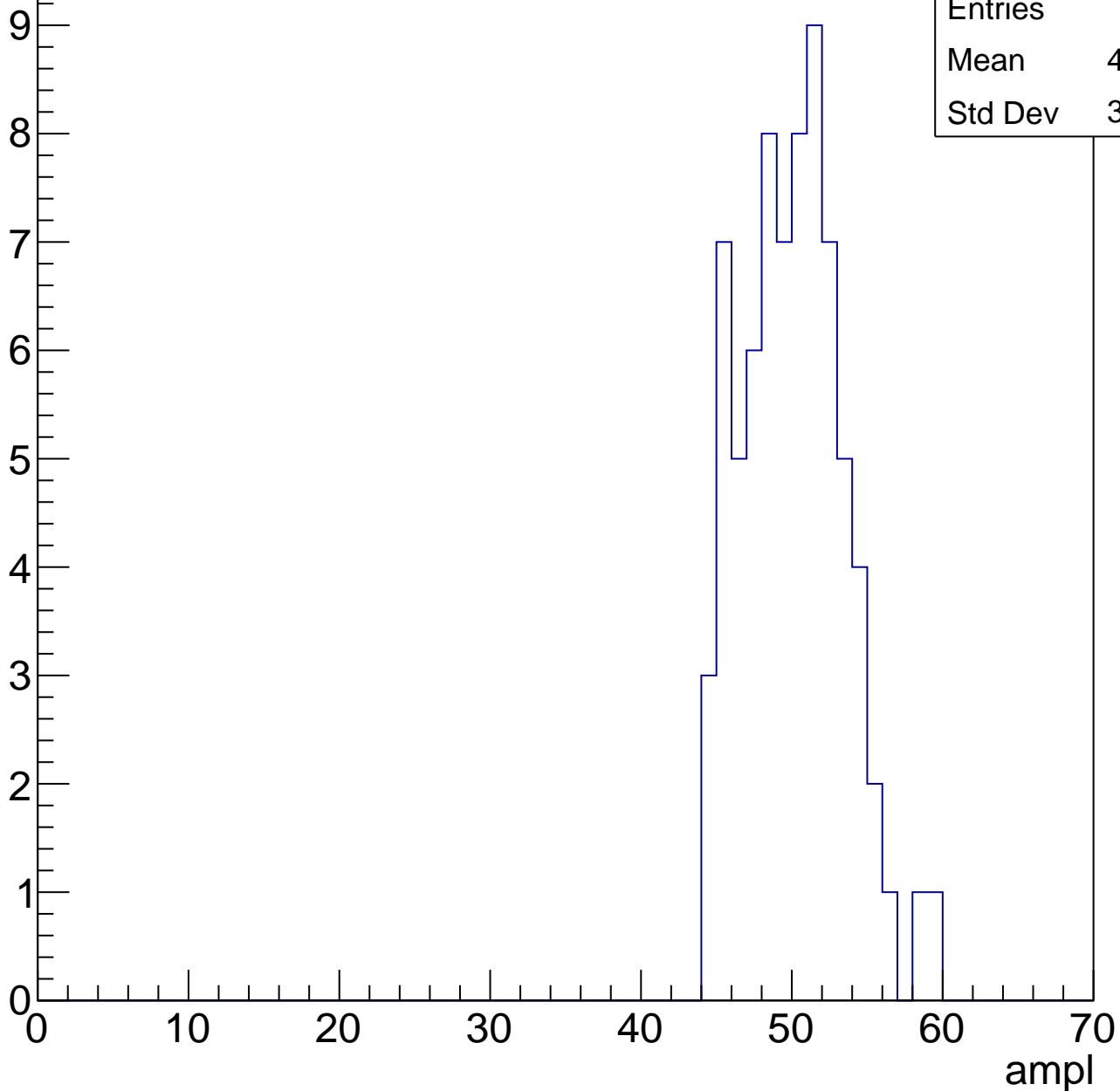


# B1L003S, U11-ch122, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	74
Mean	49.64
Std Dev	3.335



# B1L003S, U11-ch122, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

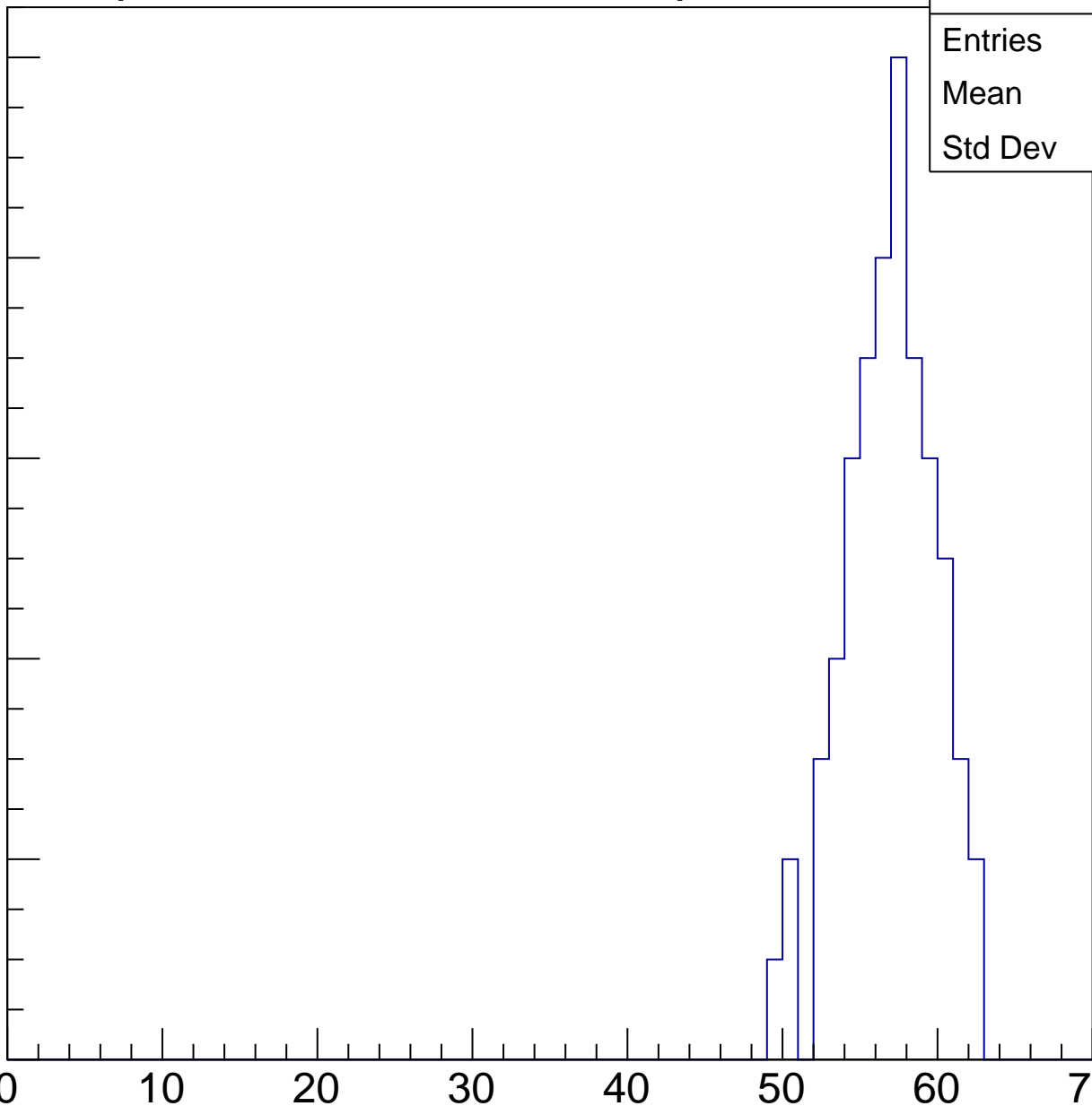
Entries	64
Mean	56.42
Std Dev	2.914

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

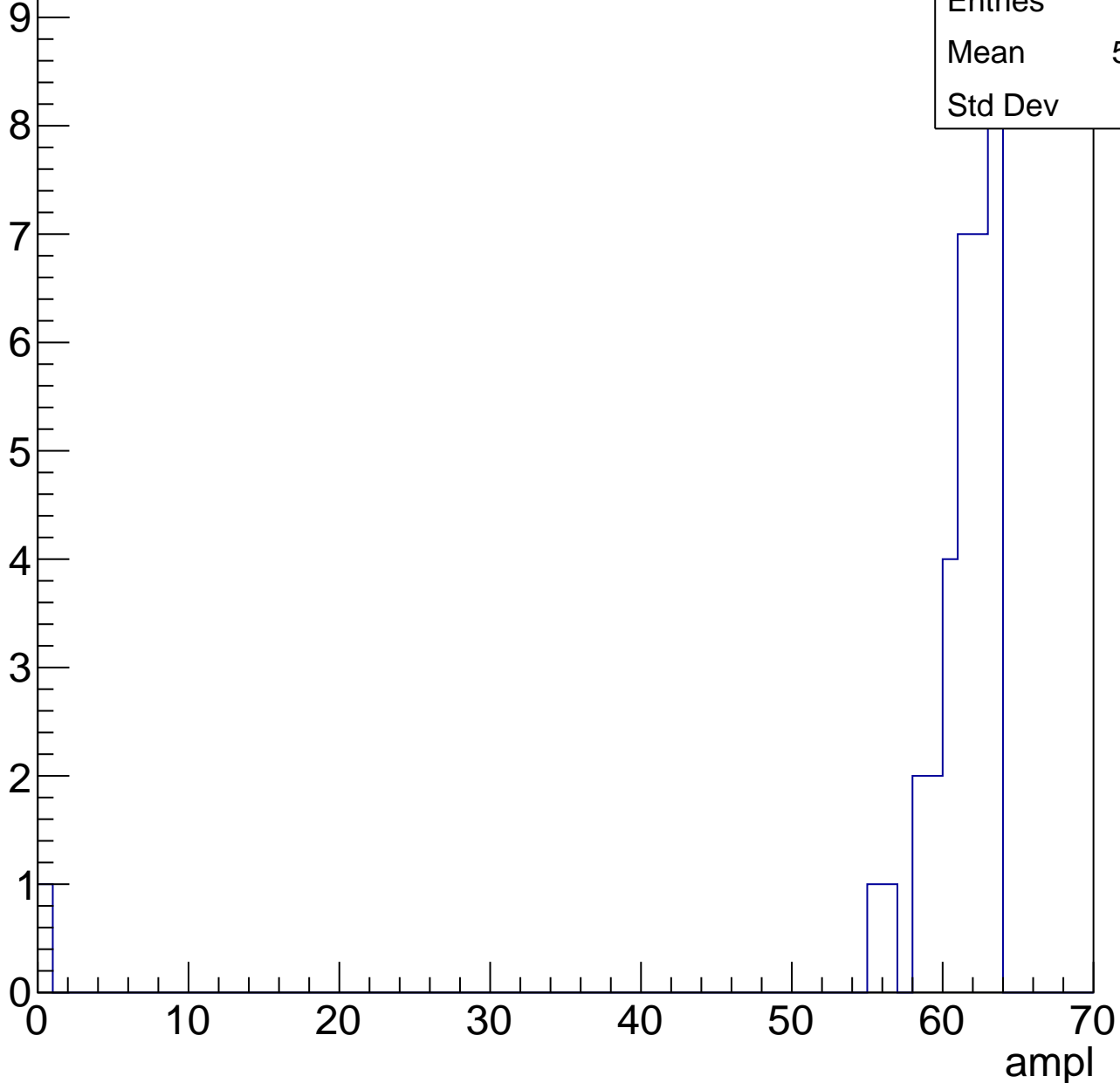


# B1L003S, U11-ch122, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

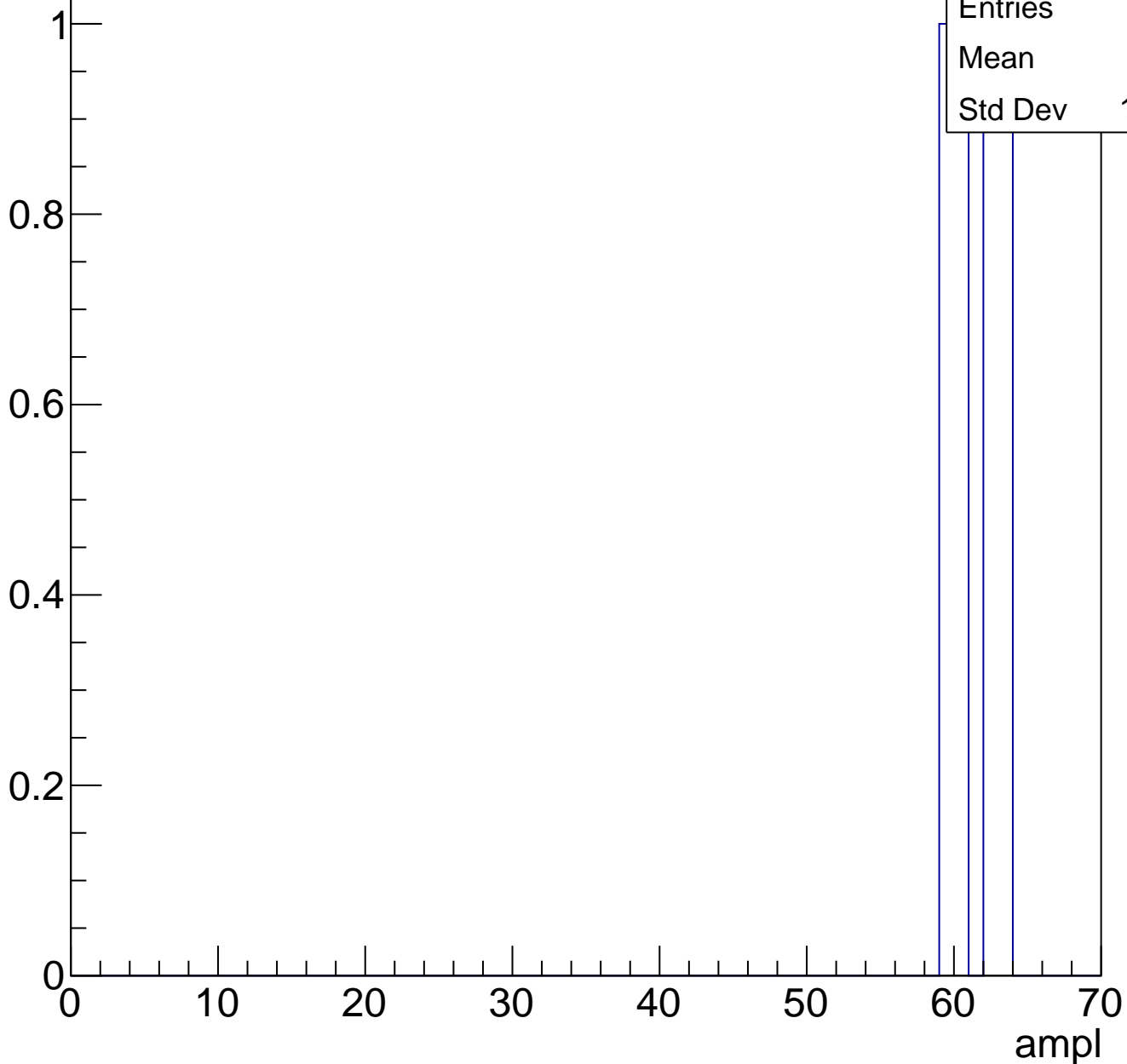
Entries	34
Mean	59.21
Std Dev	10.5



# B1L003S, U11-ch122, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch122, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U11-ch123, adc0

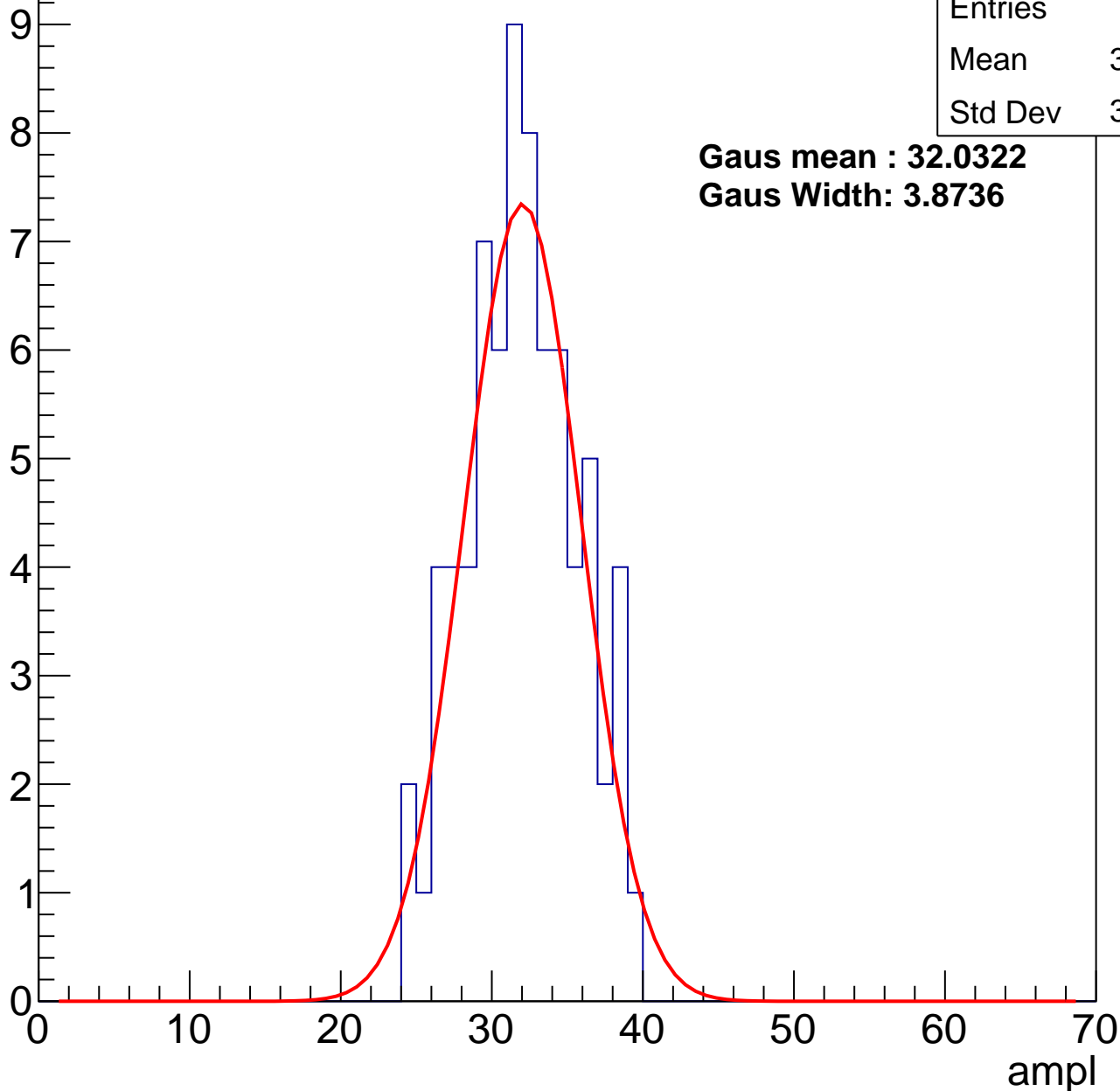
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	73
Mean	31.53
Std Dev	3.615

**Gaus mean : 32.0322**

**Gaus Width: 3.8736**



# B1L003S, U11-ch123, adc1

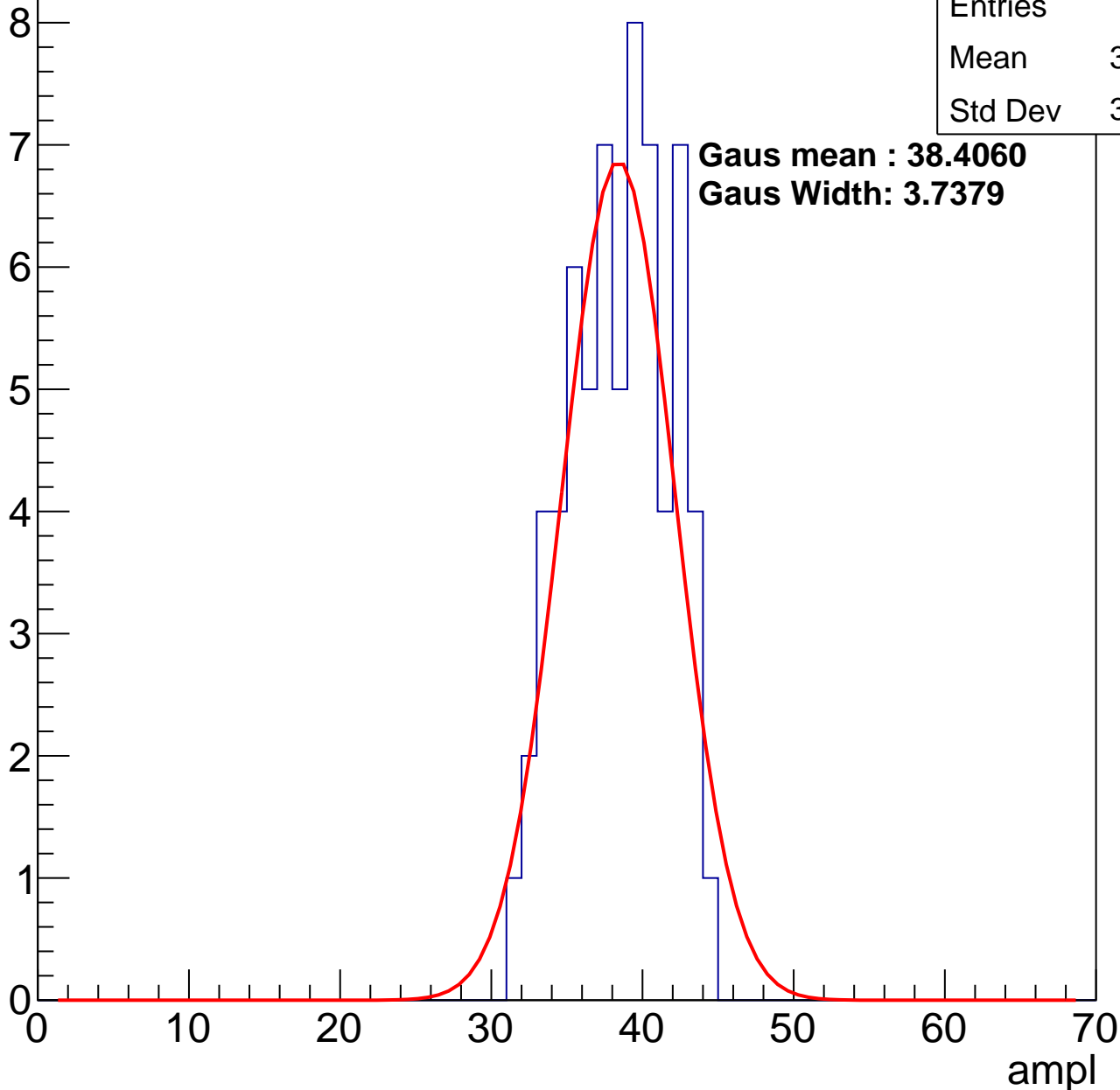
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	37.97
Std Dev	3.249

**Gaus mean : 38.4060**

**Gaus Width: 3.7379**



# B1L003S, U11-ch123, adc2

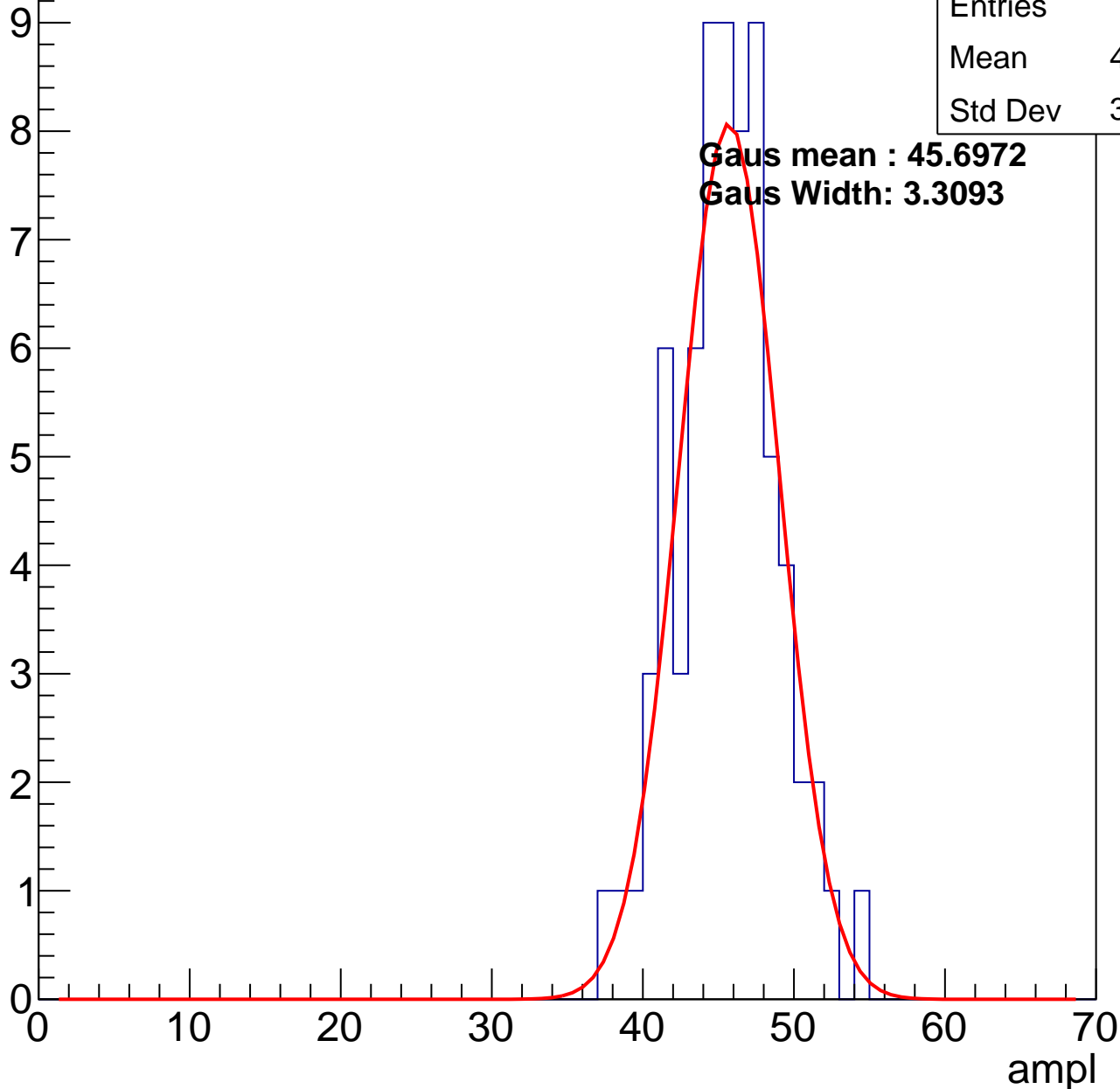
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	71
Mean	45.07
Std Dev	3.324

**Gaus mean : 45.6972**

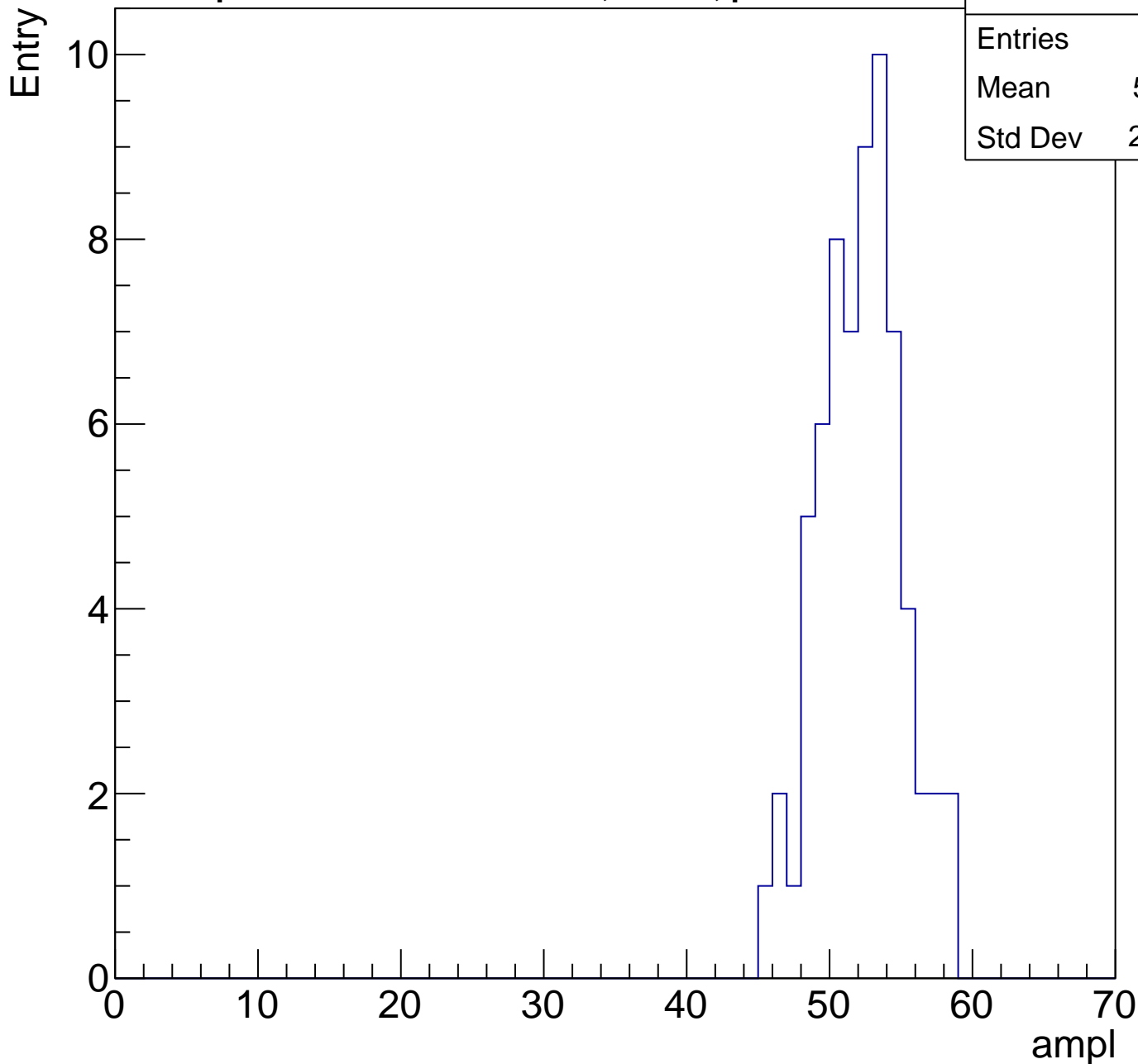
**Gaus Width: 3.3093**



# B1L003S, U11-ch123, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	66
Mean	51.71
Std Dev	2.864

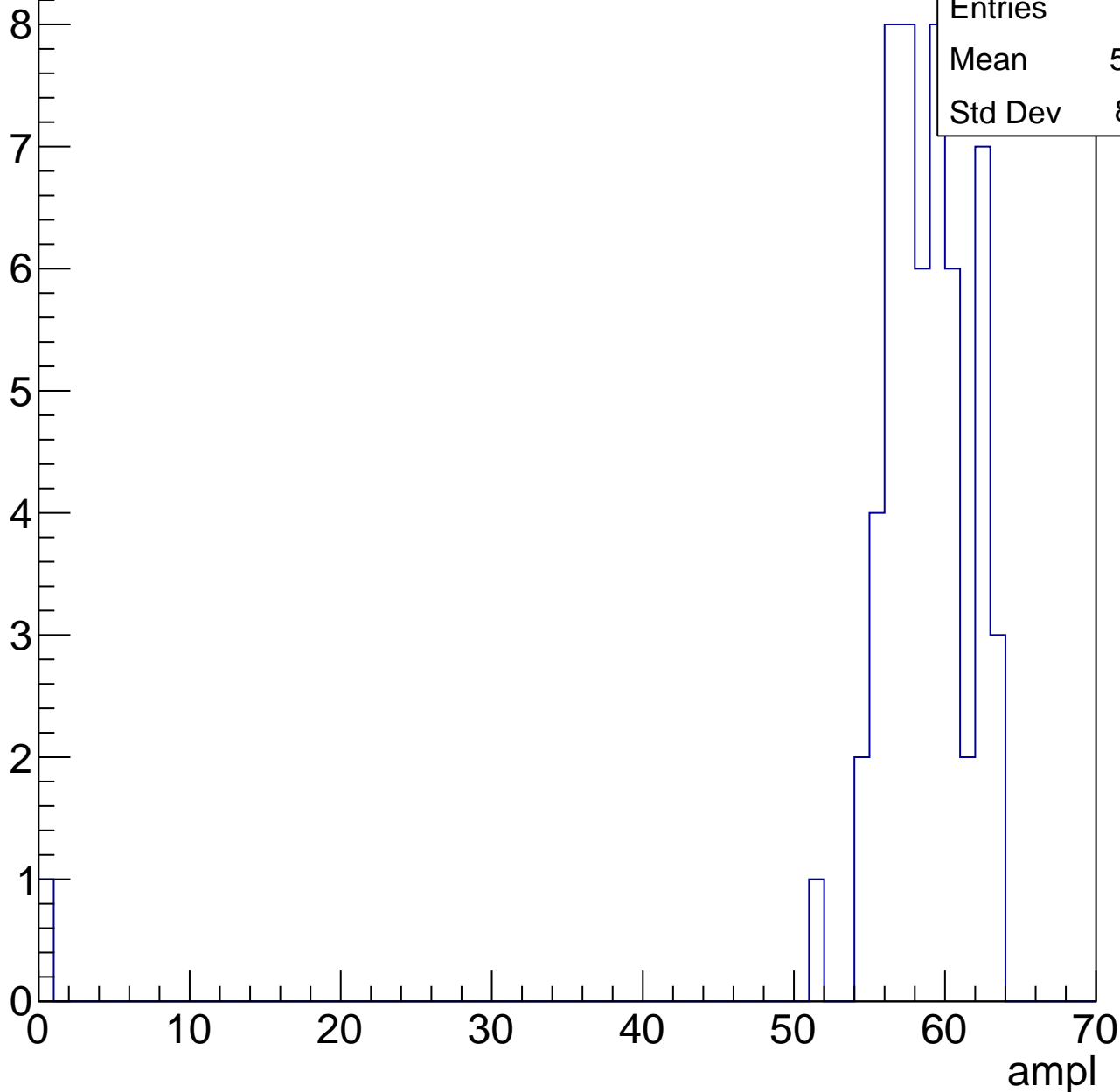


# B1L003S, U11-ch123, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	57.29
Std Dev	8.161

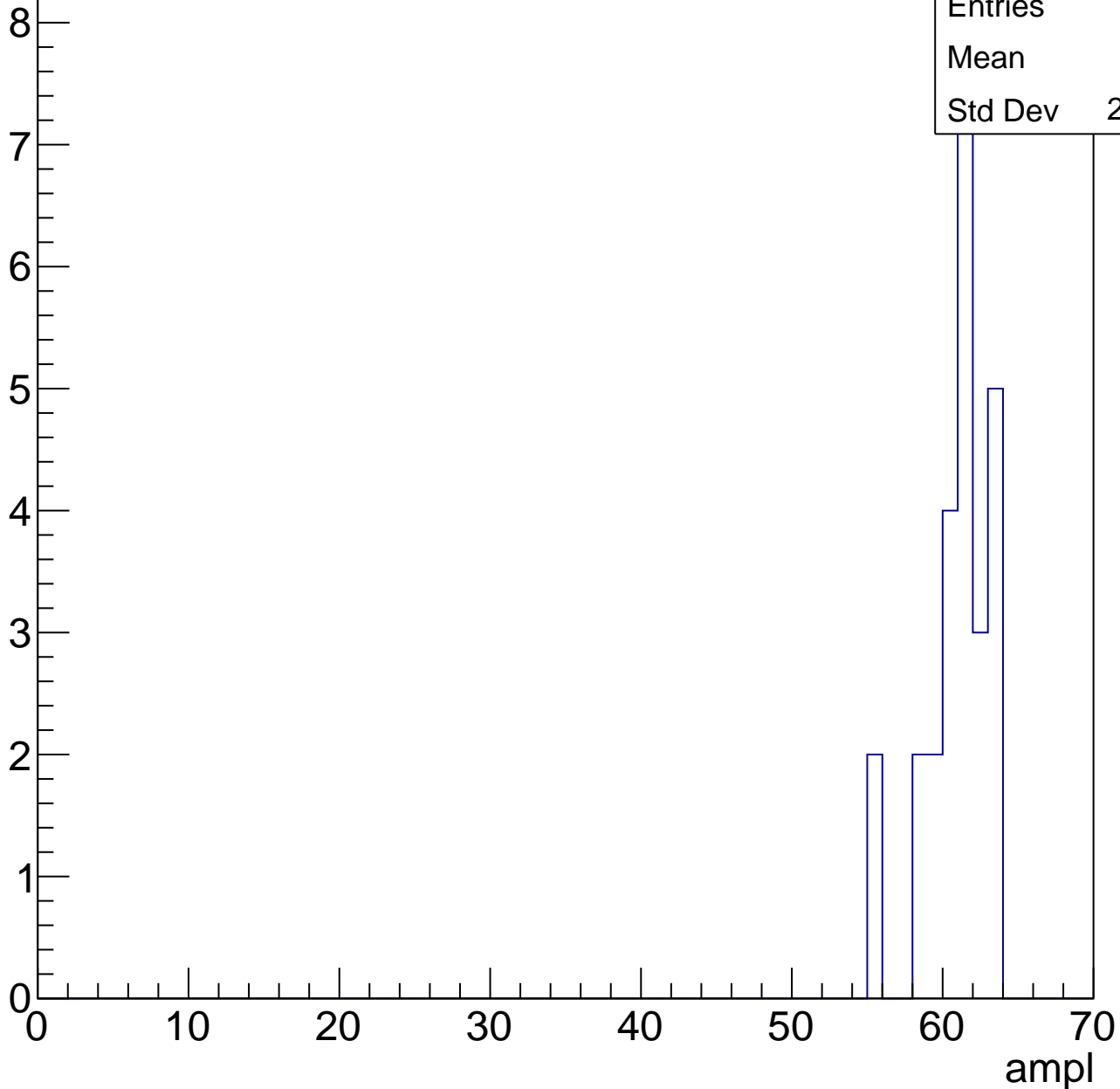


# B1L003S, U11-ch123, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	26
Mean	60.5
Std Dev	2.135



# B1L003S, U11-ch123, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch123, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U11-ch124, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	64
Mean	29.58
Std Dev	2.887

**Gaus mean : 29.3789**

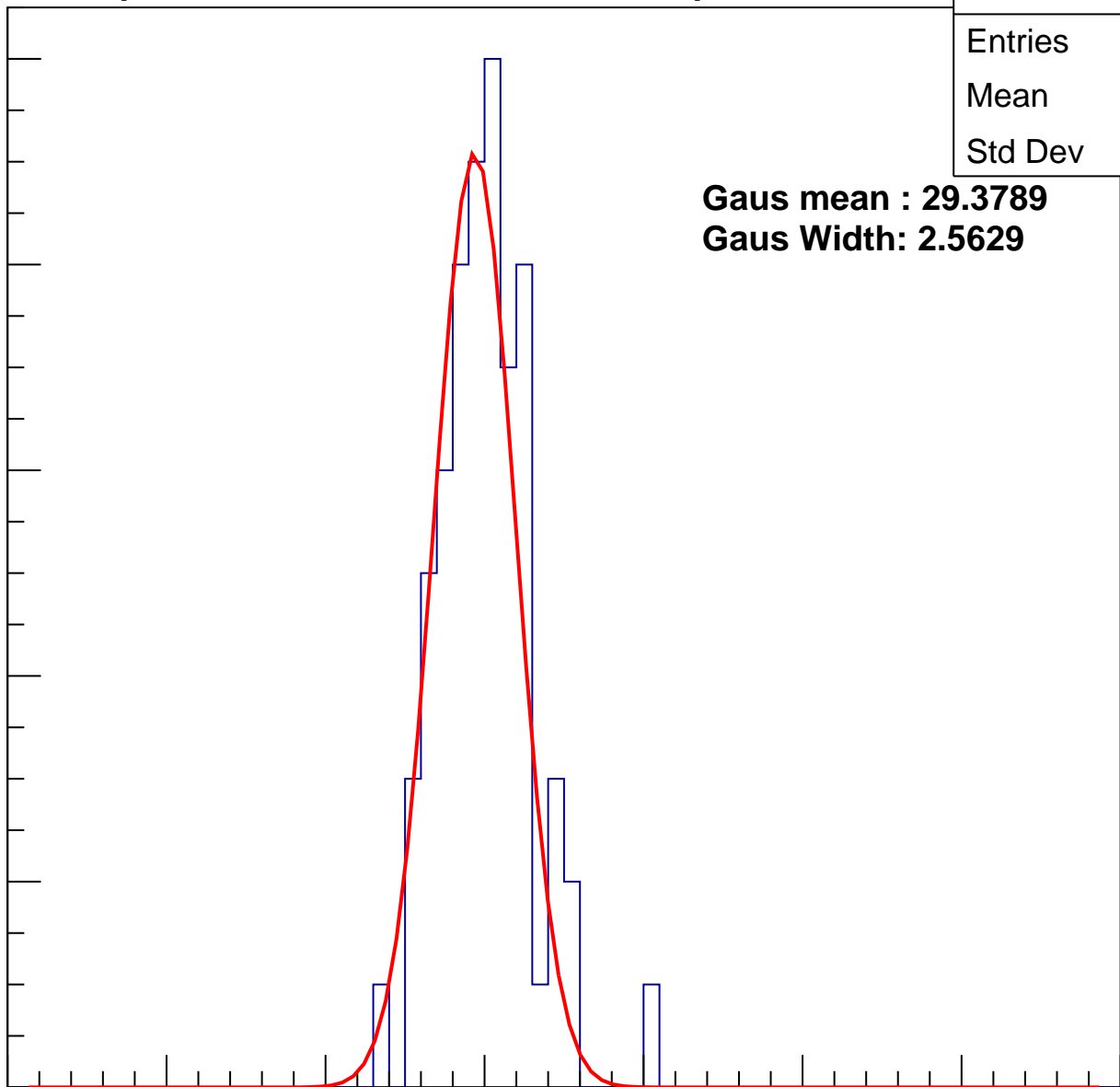
**Gaus Width: 2.5629**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

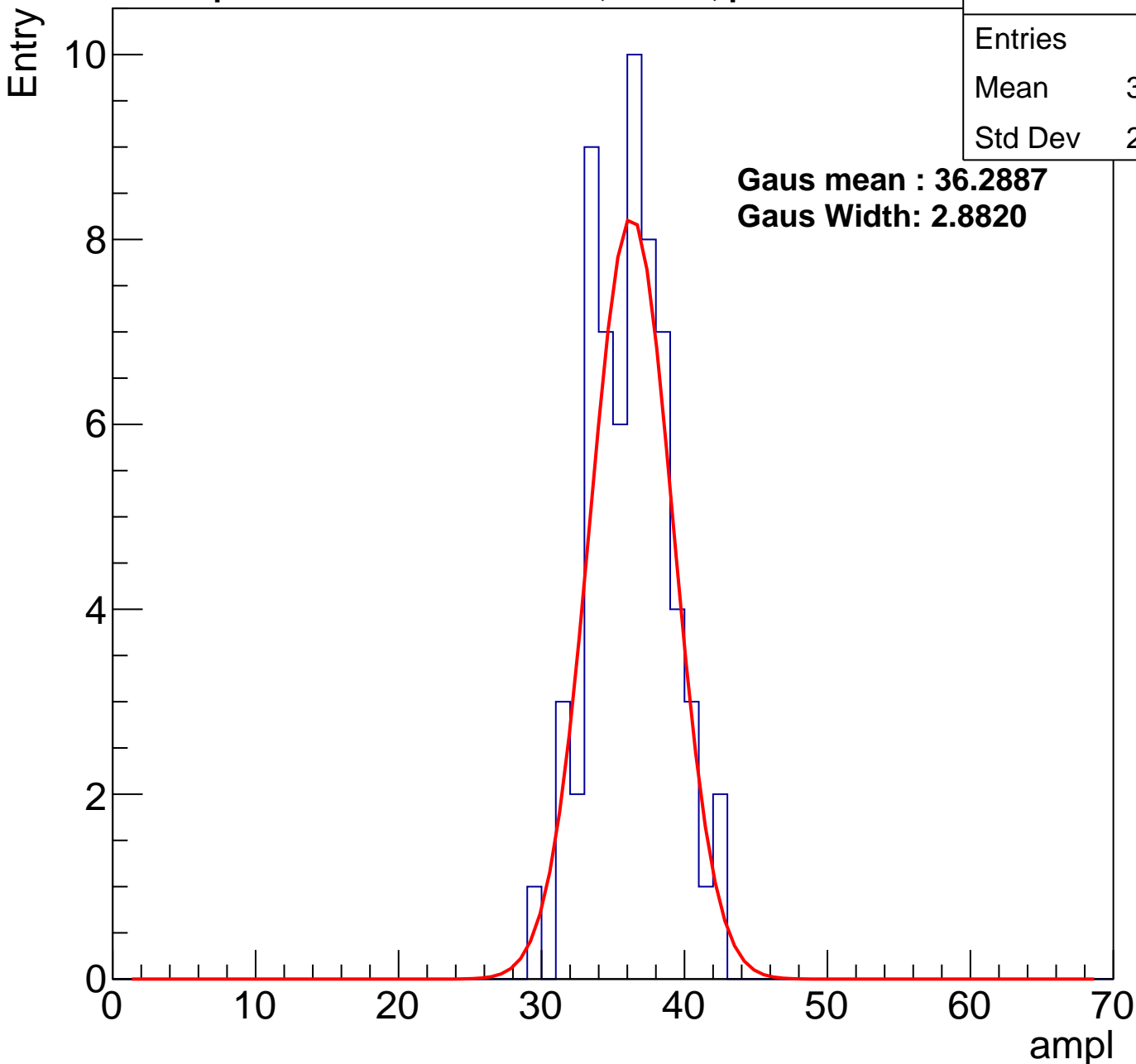


# B1L003S, U11-ch124, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	63
Mean	35.78
Std Dev	2.774

**Gaus mean : 36.2887**  
**Gaus Width: 2.8820**



# B1L003S, U11-ch124, adc2

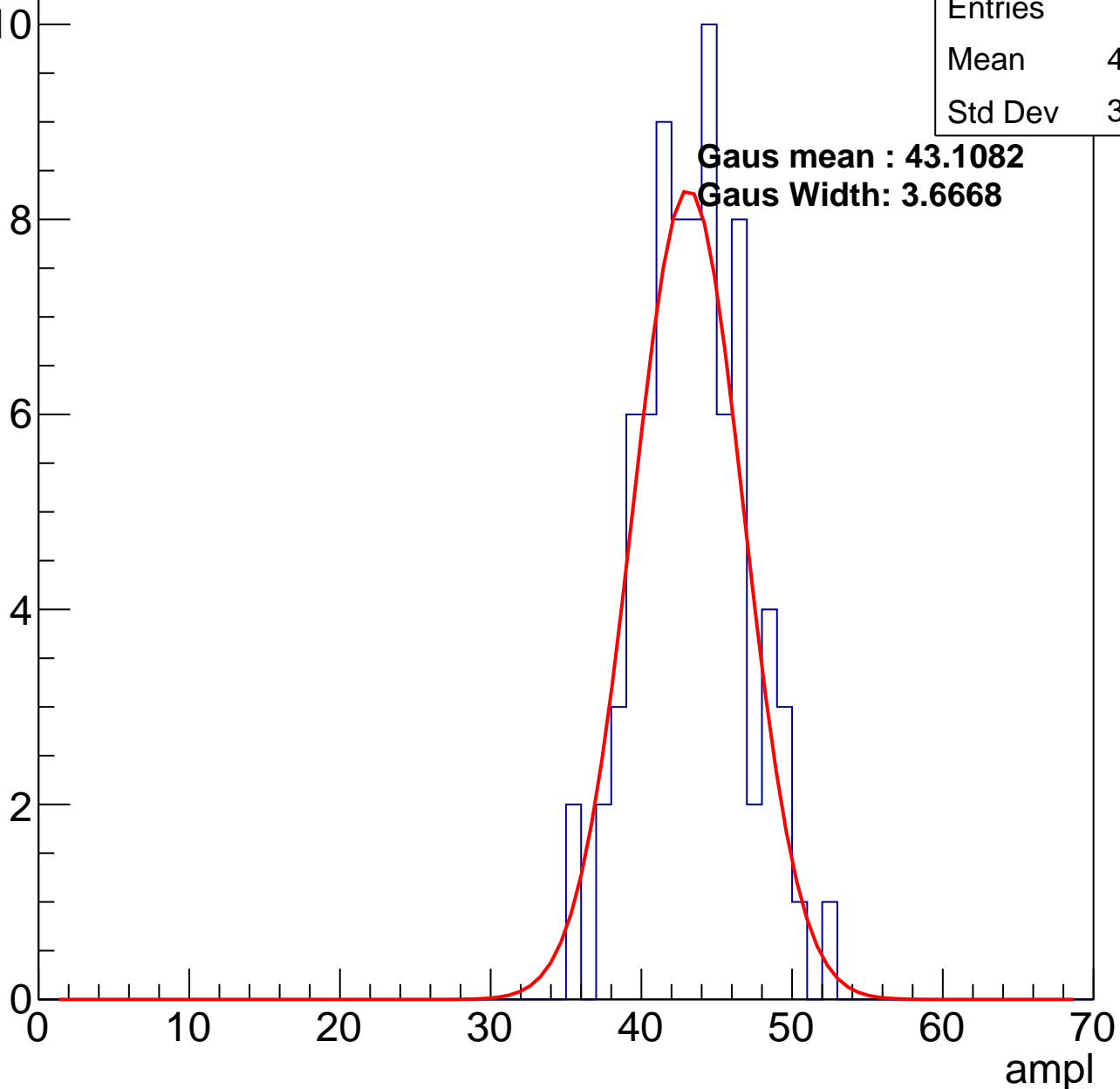
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	79
Mean	42.96
Std Dev	3.458

**Gaus mean : 43.1082**

**Gaus Width: 3.6668**

Entry

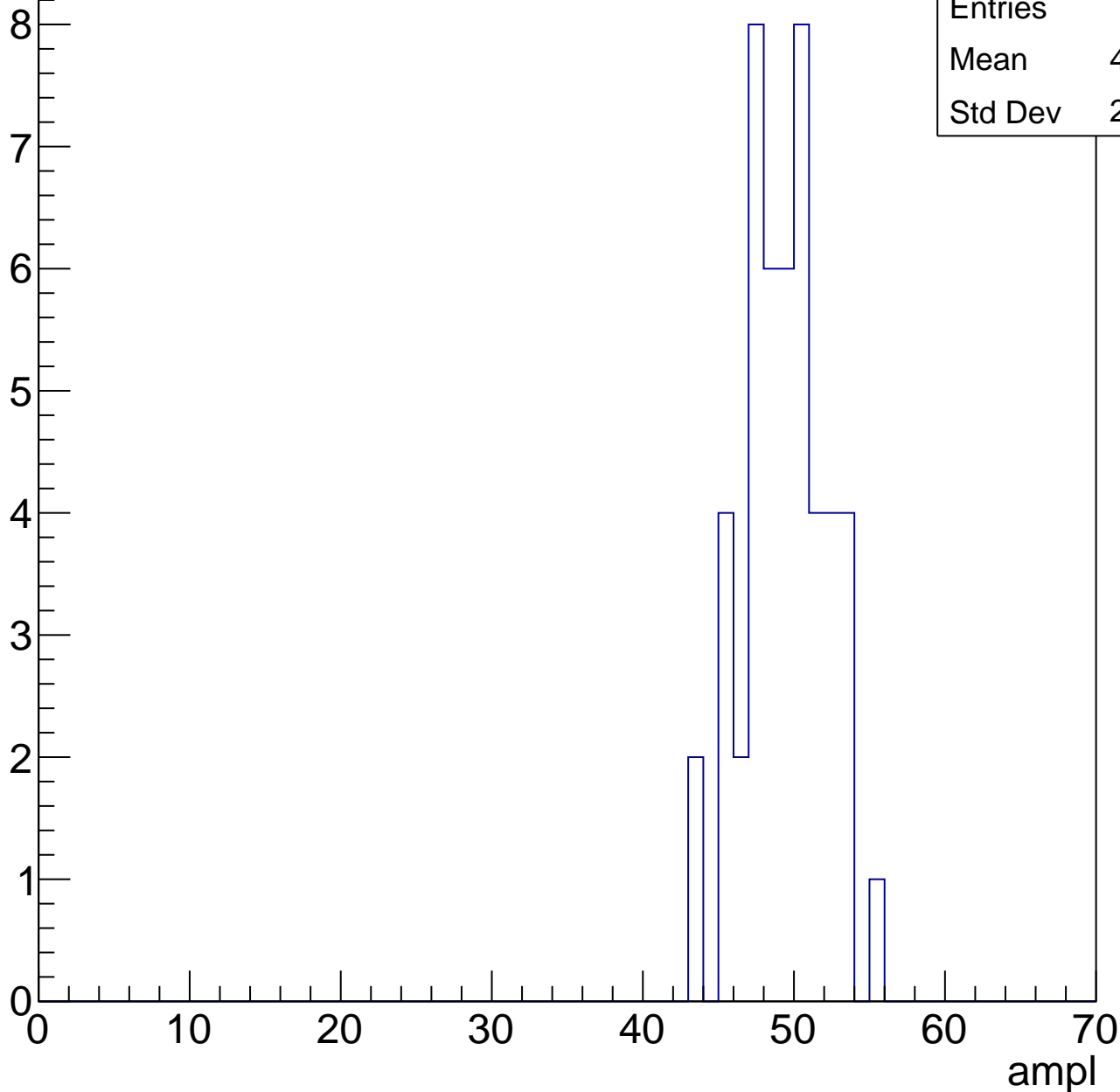


# B1L003S, U11-ch124, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	49
Mean	48.88
Std Dev	2.677

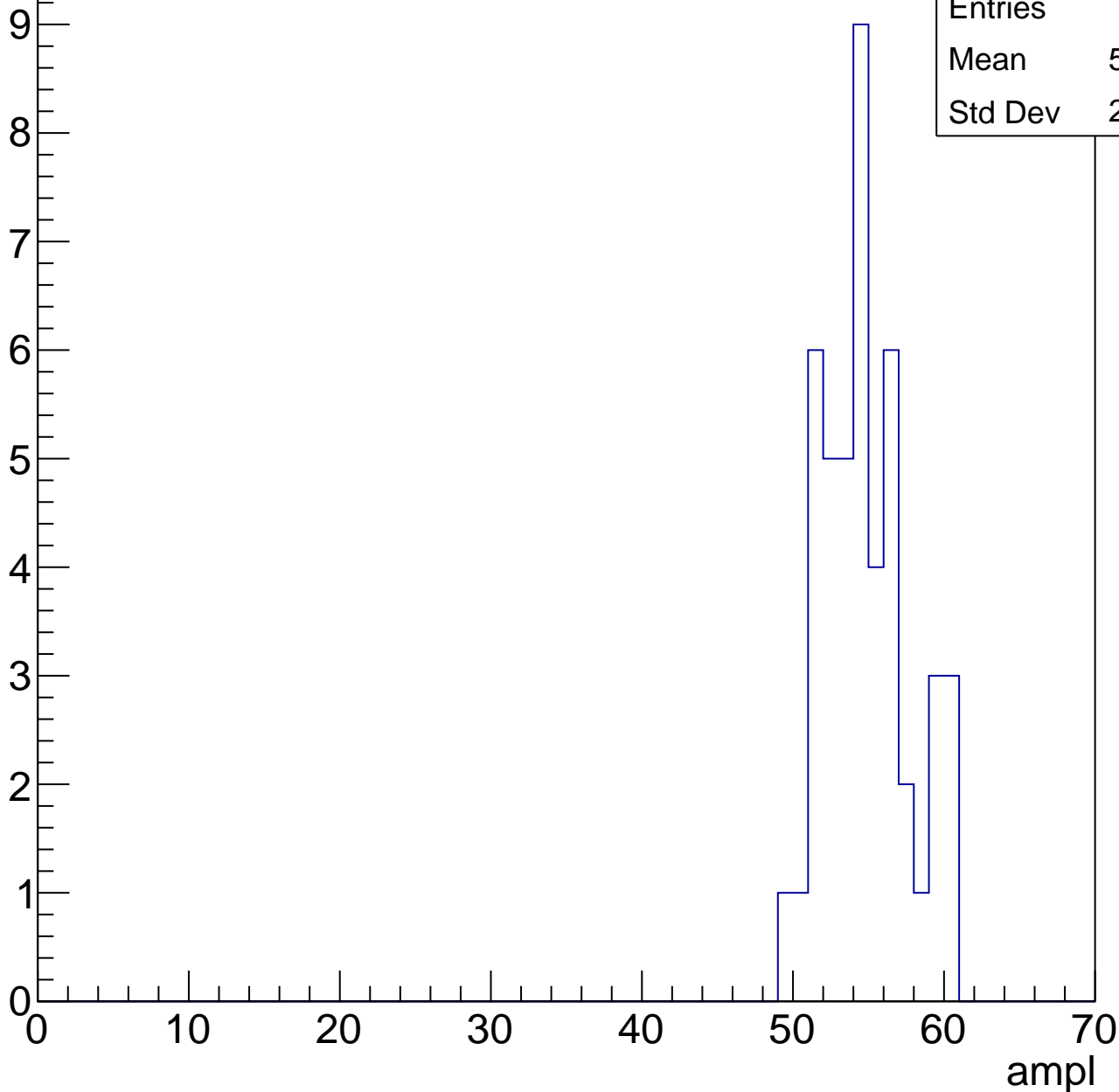


# B1L003S, U11-ch124, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	46
Mean	54.37
Std Dev	2.793

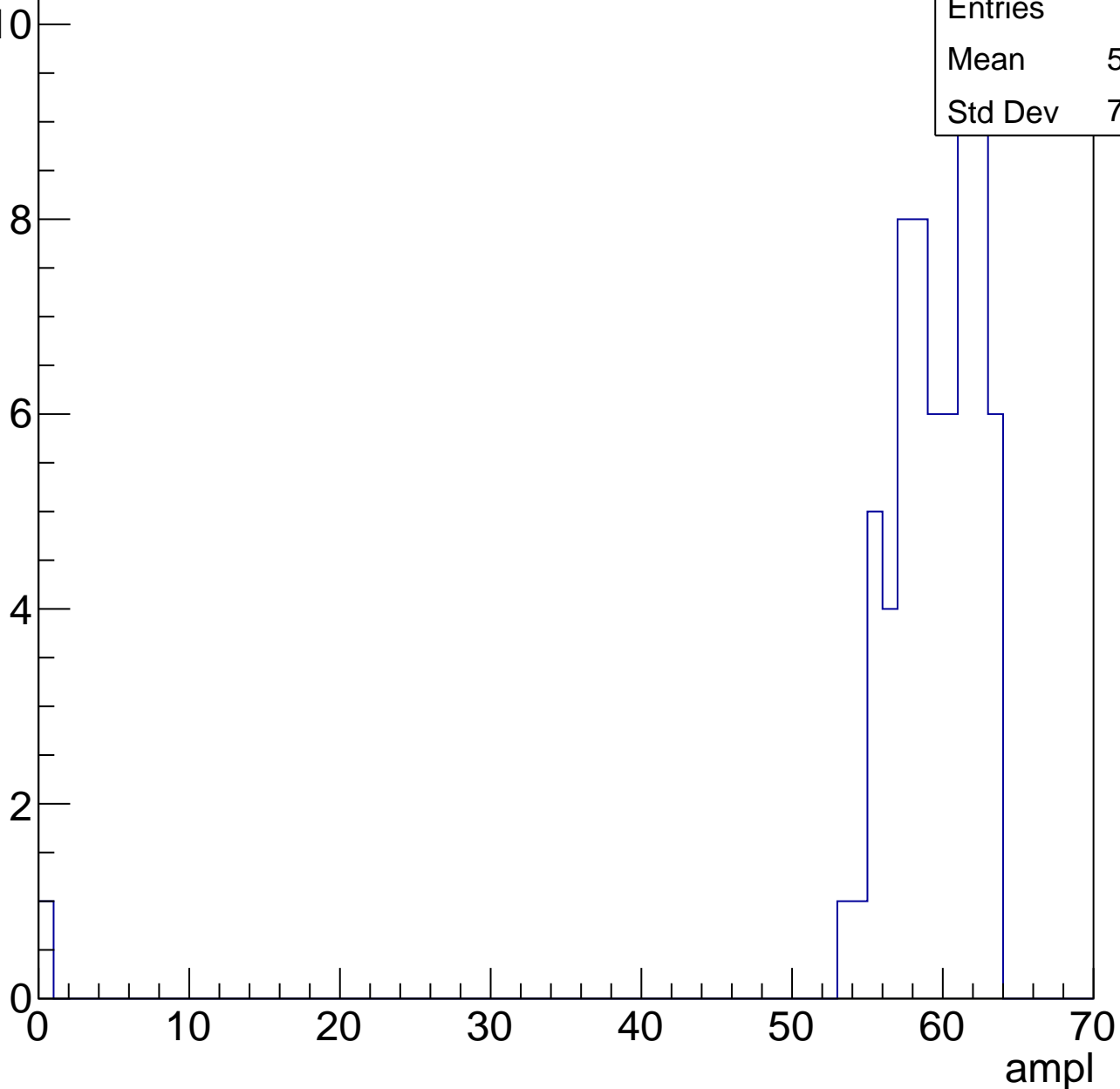


# B1L003S, U11-ch124, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

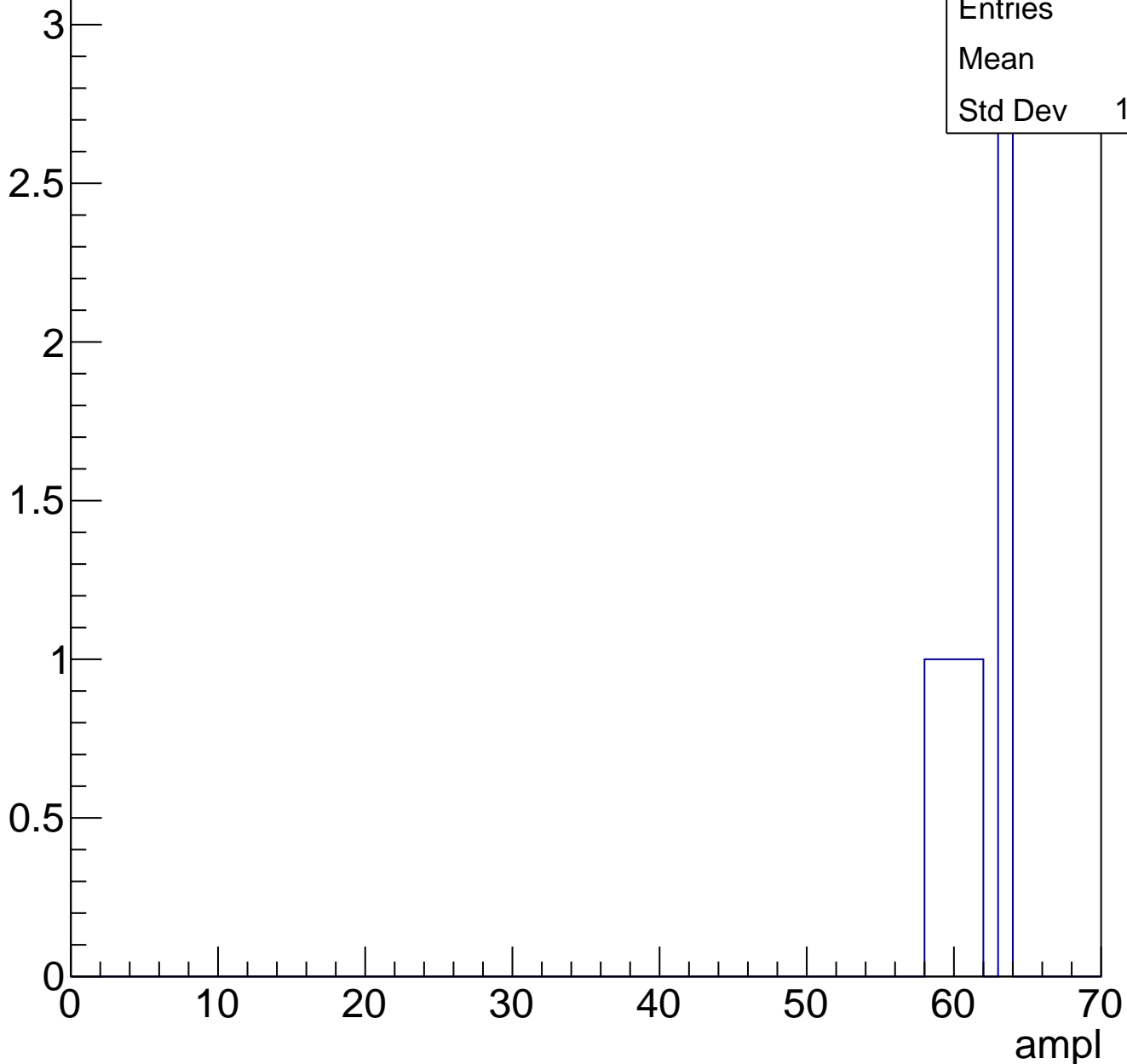
Entries	65
Mean	58.26
Std Dev	7.737



# B1L003S, U11-ch124, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

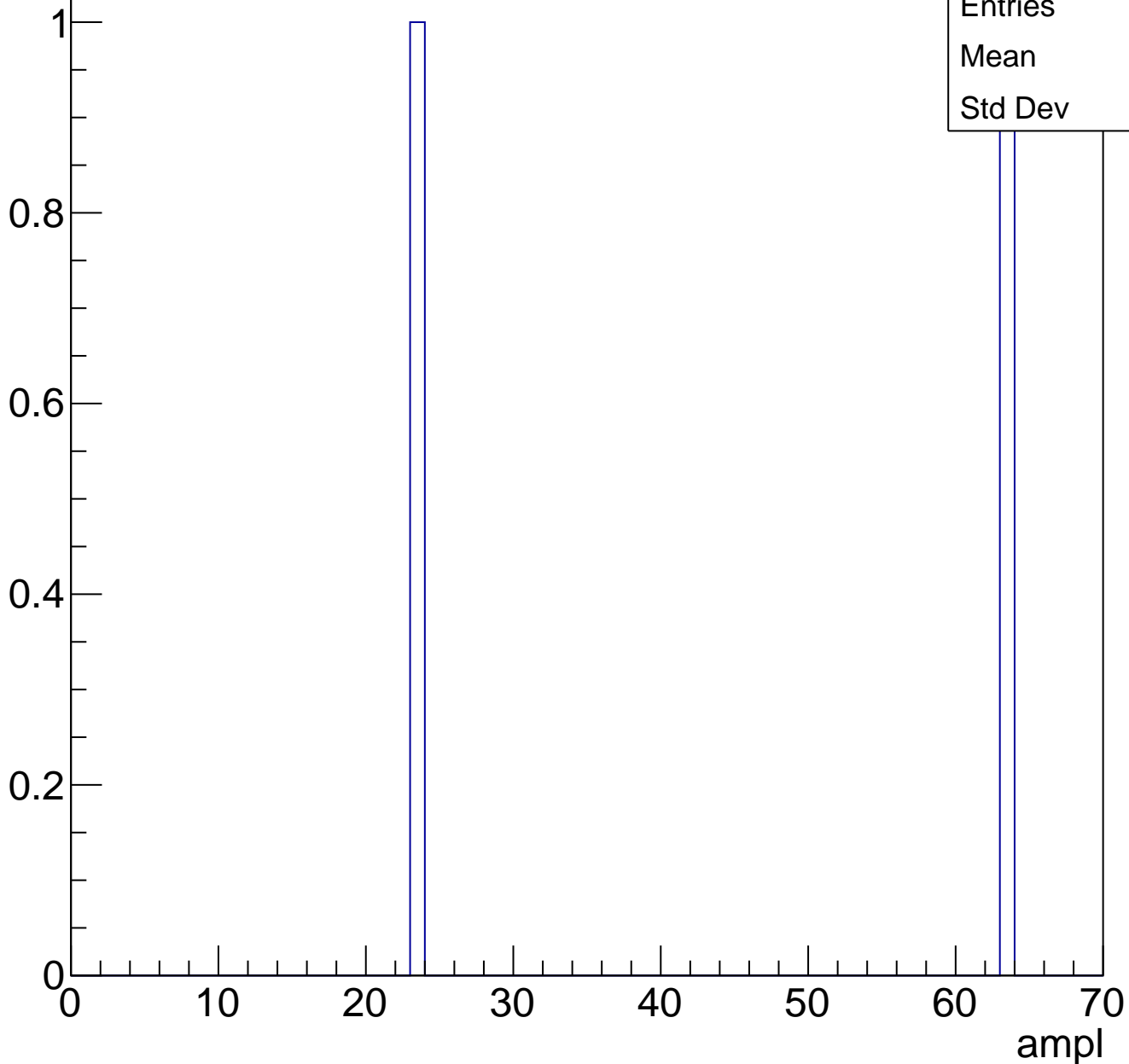




# B1L003S, U11-ch124, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U11-ch125, adc0

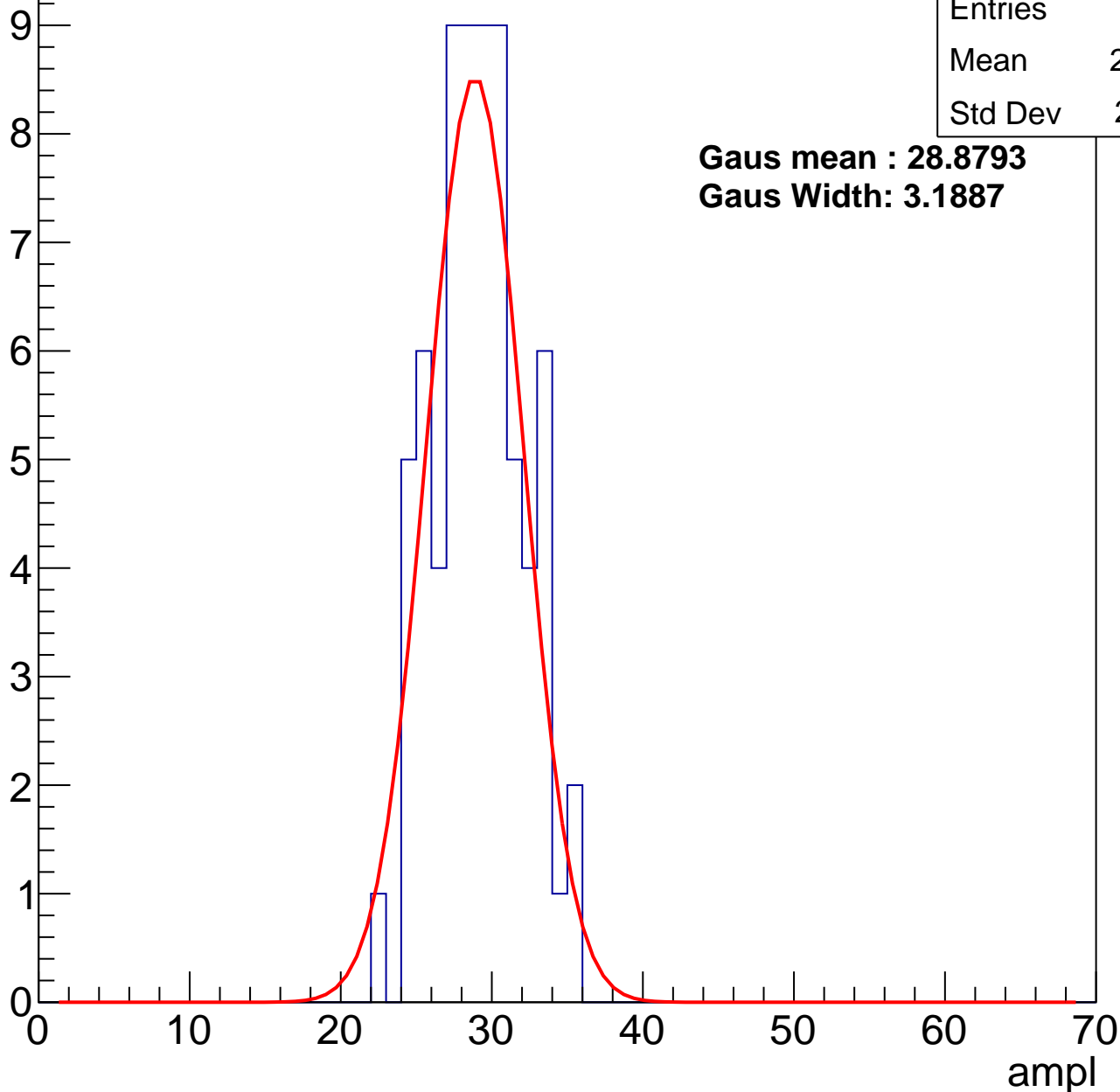
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	28.67
Std Dev	2.931

**Gaus mean : 28.8793**

**Gaus Width: 3.1887**



# B1L003S, U11-ch125, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	76
Mean	36.25
Std Dev	3.66

**Gaus mean : 36.5456**

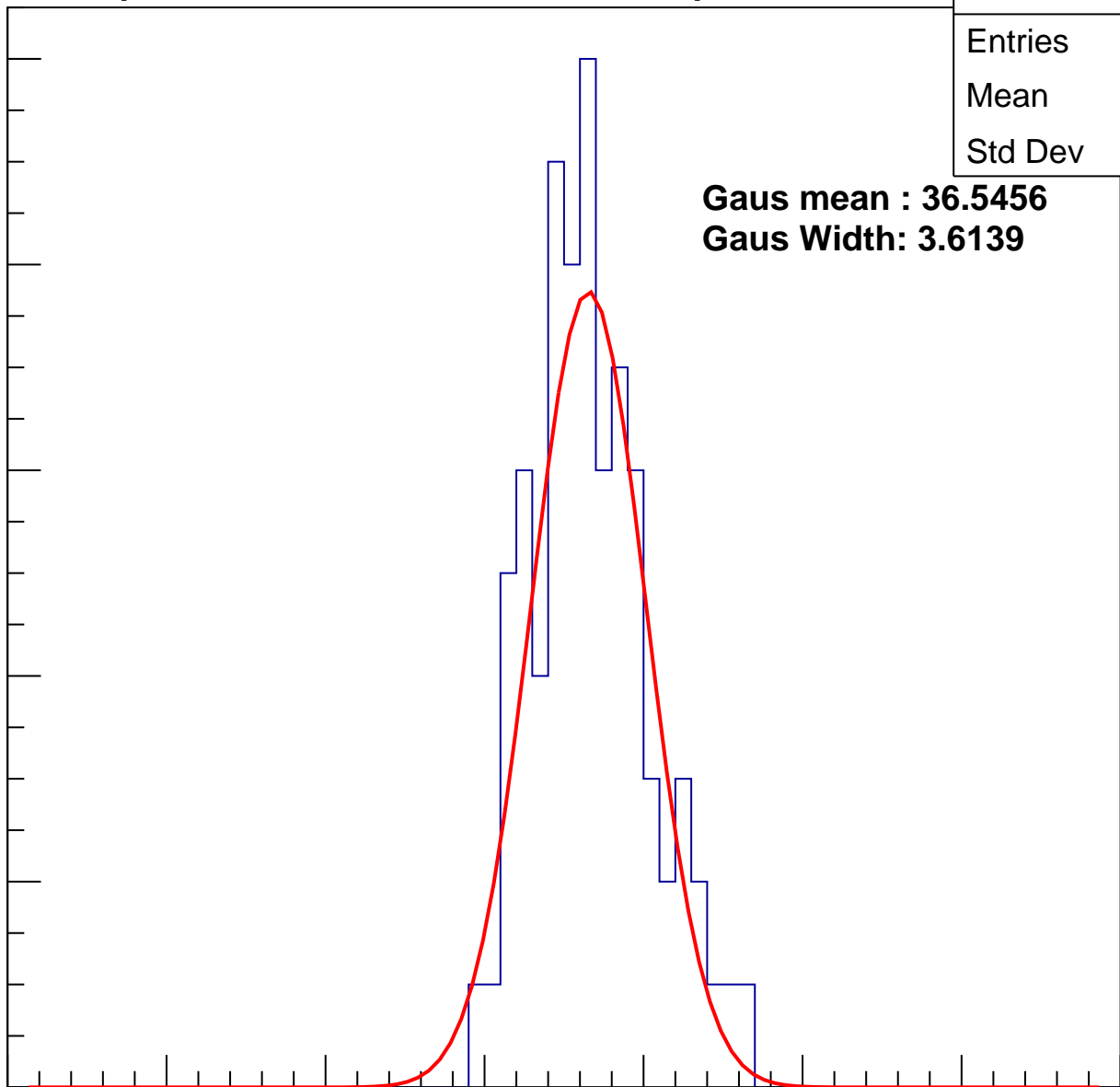
**Gaus Width: 3.6139**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L003S, U11-ch125, adc2

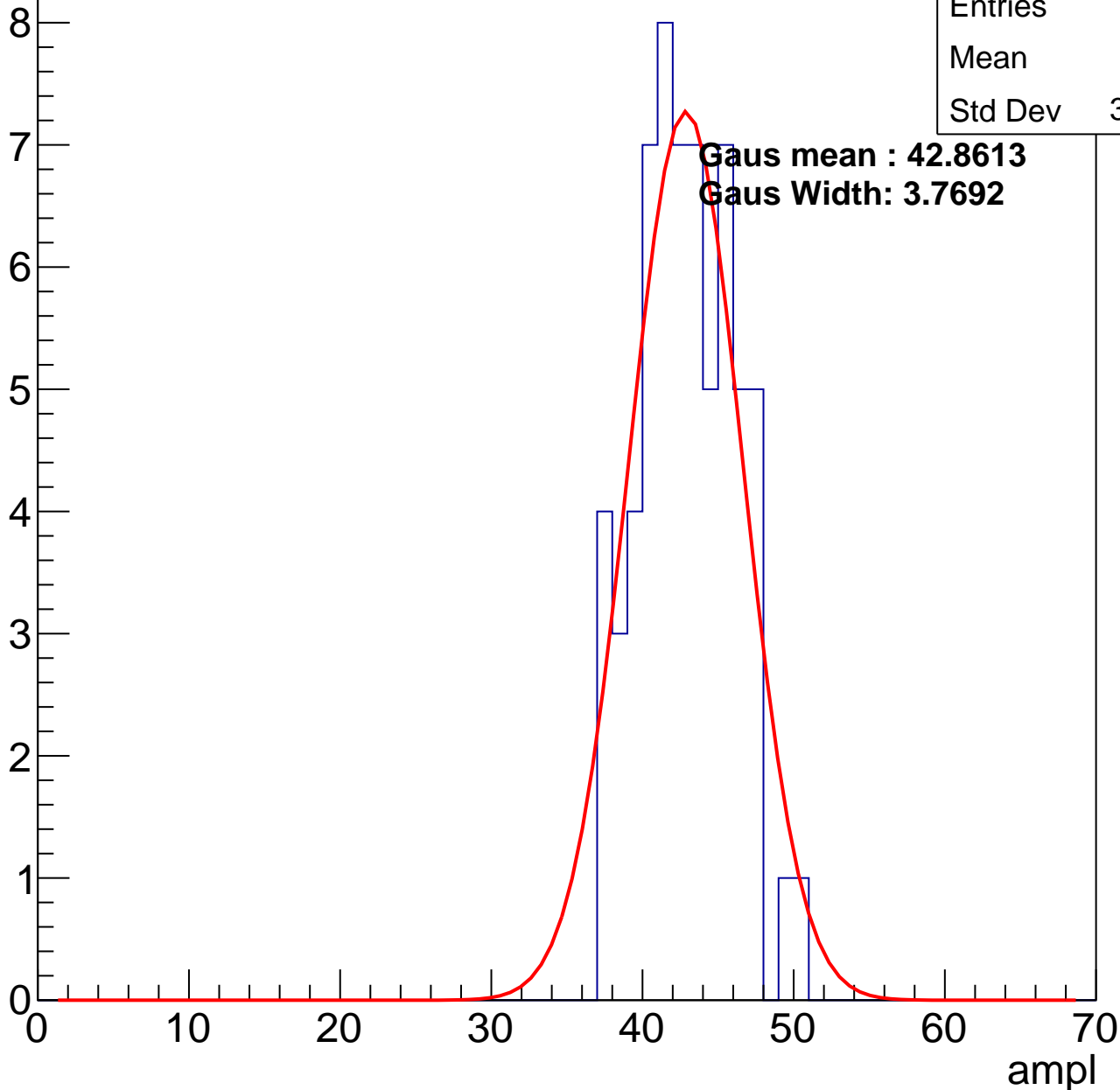
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	42.5
Std Dev	3.092

**Gaus mean : 42.8613**

**Gaus Width: 3.7692**

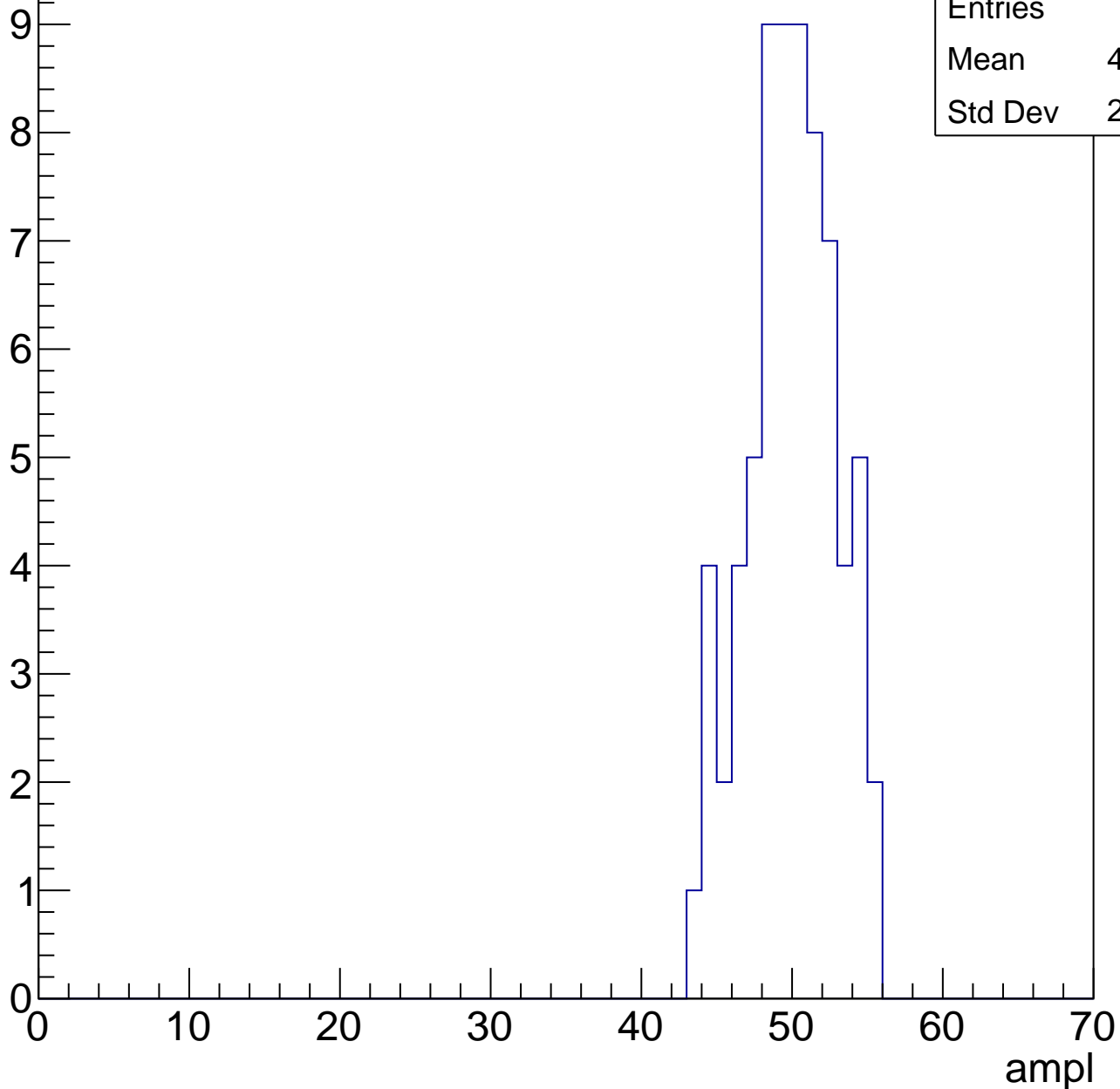


# B1L003S, U11-ch125, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	49.49
Std Dev	2.902



# B1L003S, U11-ch125, adc4

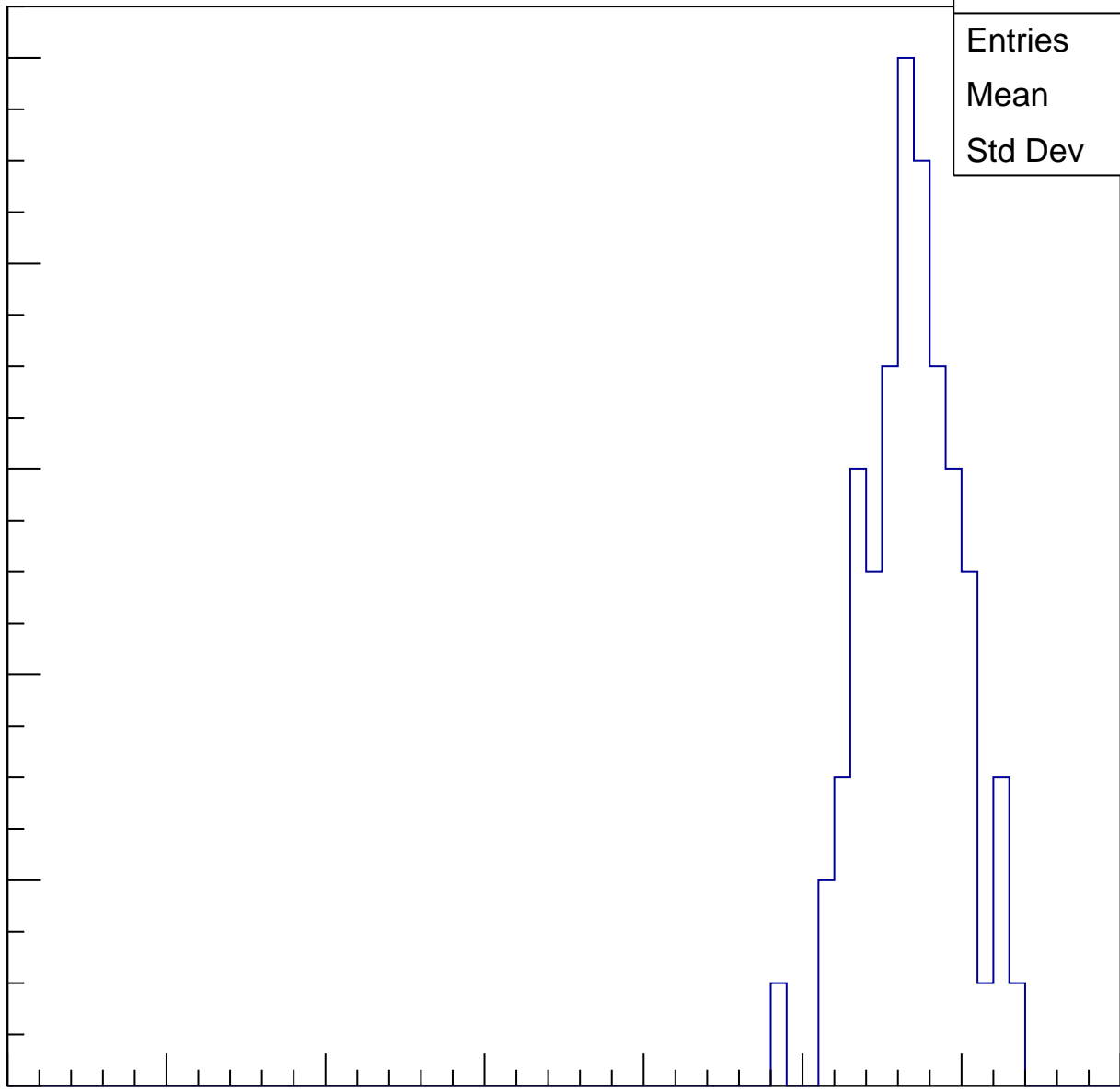
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	66
Mean	56.39
Std Dev	2.979

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70  
ampl

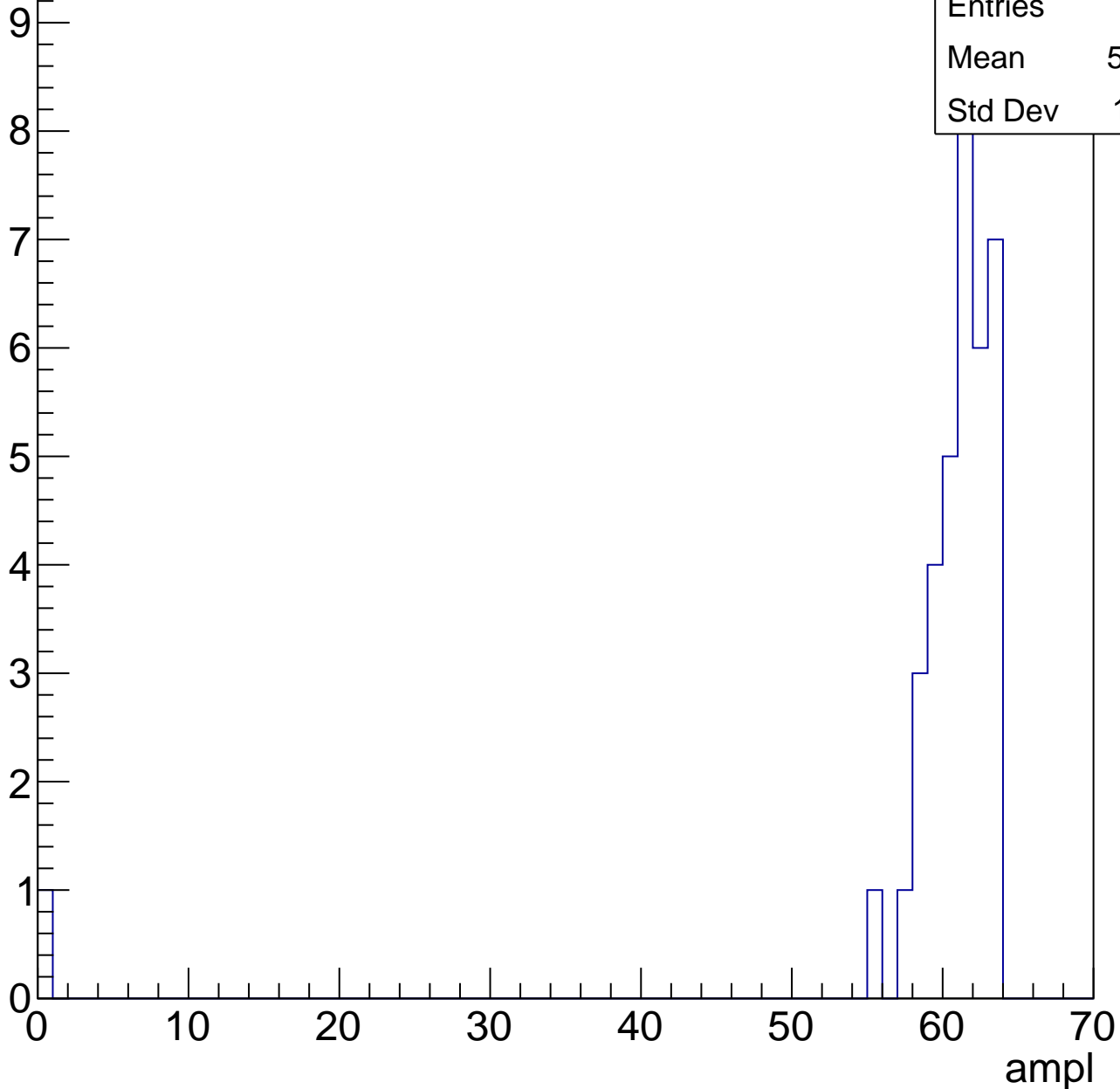


# B1L003S, U11-ch125, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	37
Mean	59.03
Std Dev	10.01



# B1L003S, U11-ch125, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch125, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U11-ch126, adc0

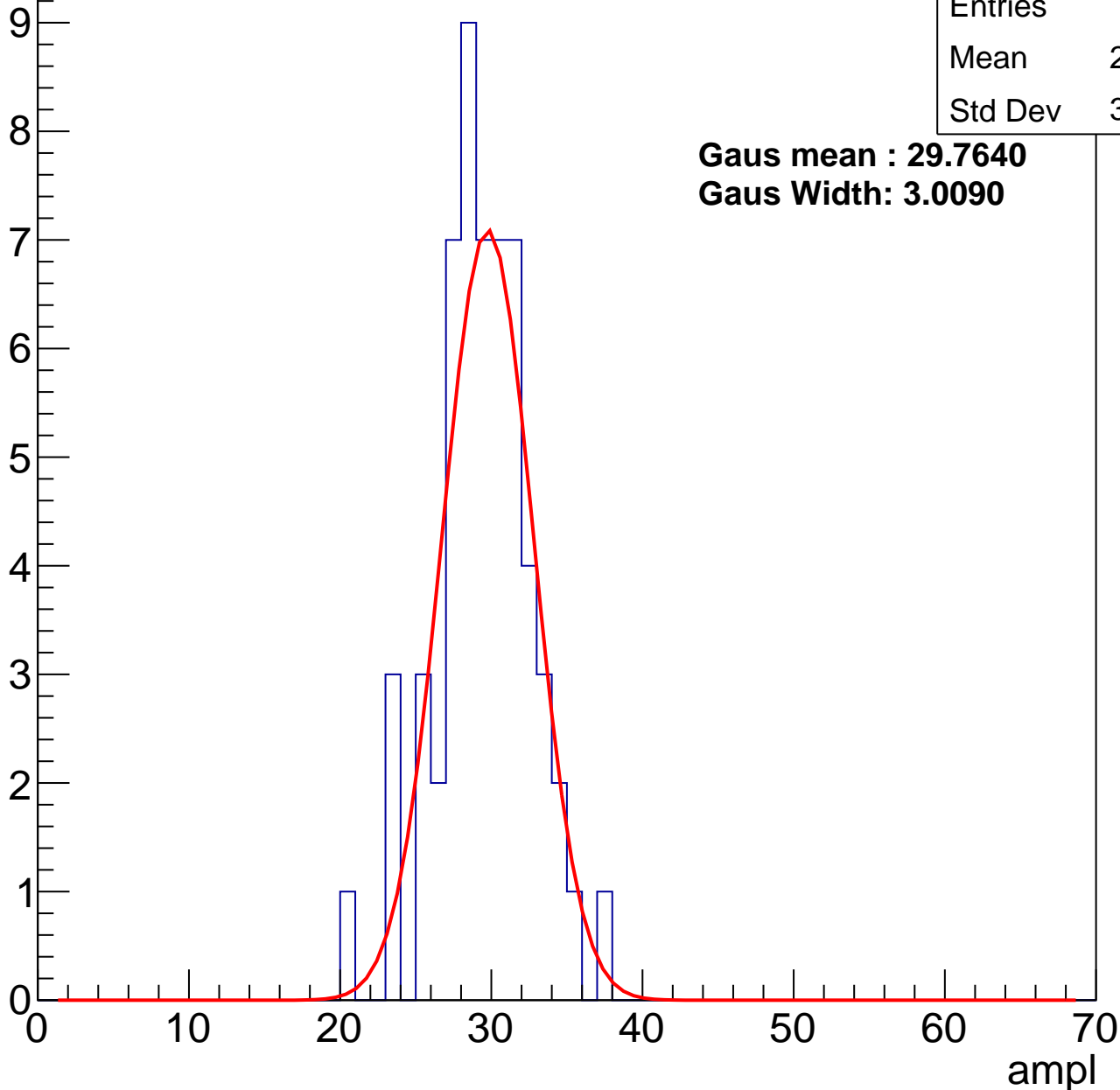
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	29.02
Std Dev	3.137

**Gaus mean : 29.7640**

**Gaus Width: 3.0090**



# B1L003S, U11-ch126, adc1

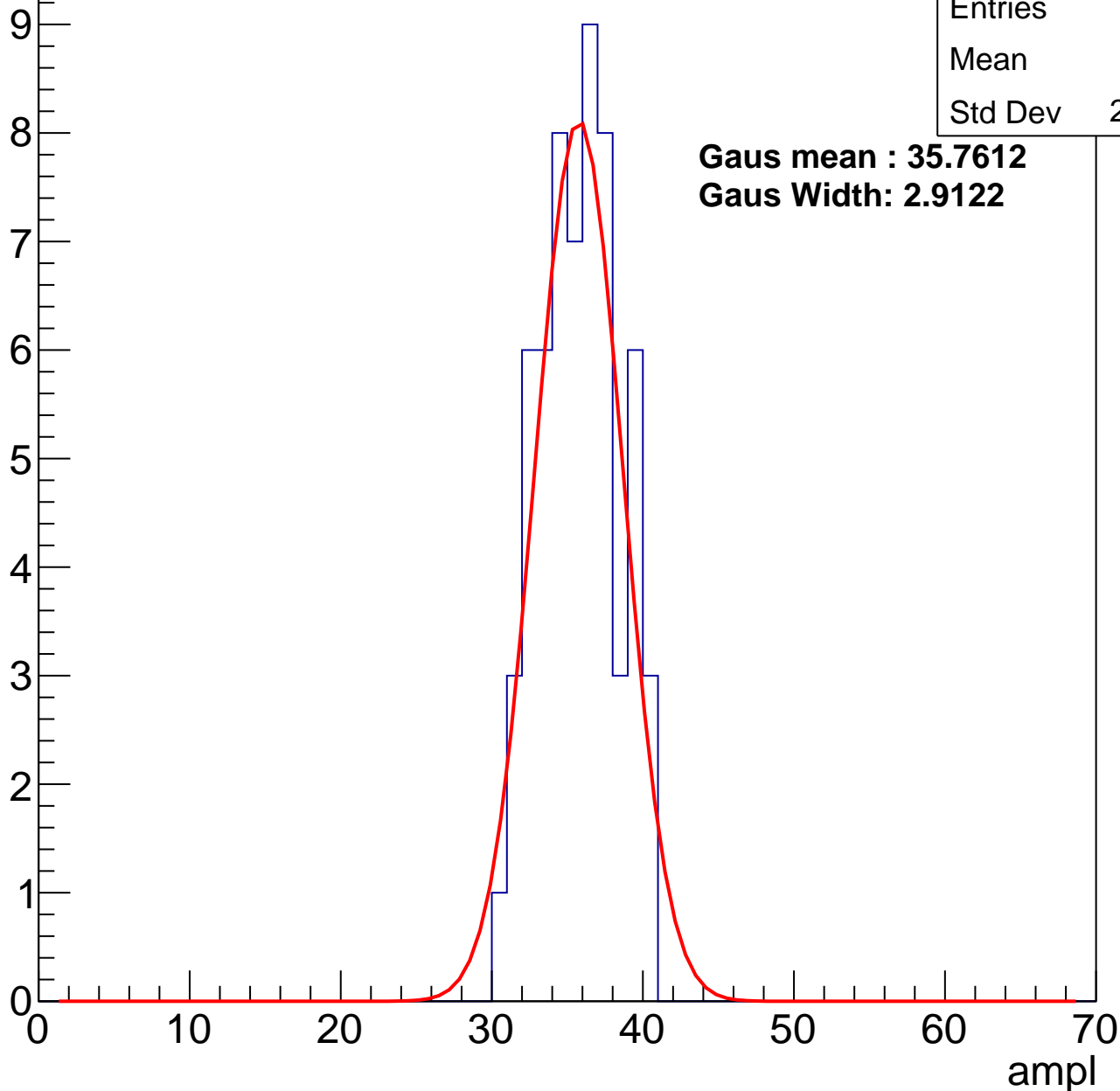
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	35.3
Std Dev	2.558

**Gaus mean : 35.7612**

**Gaus Width: 2.9122**



# B1L003S, U11-ch126, adc2

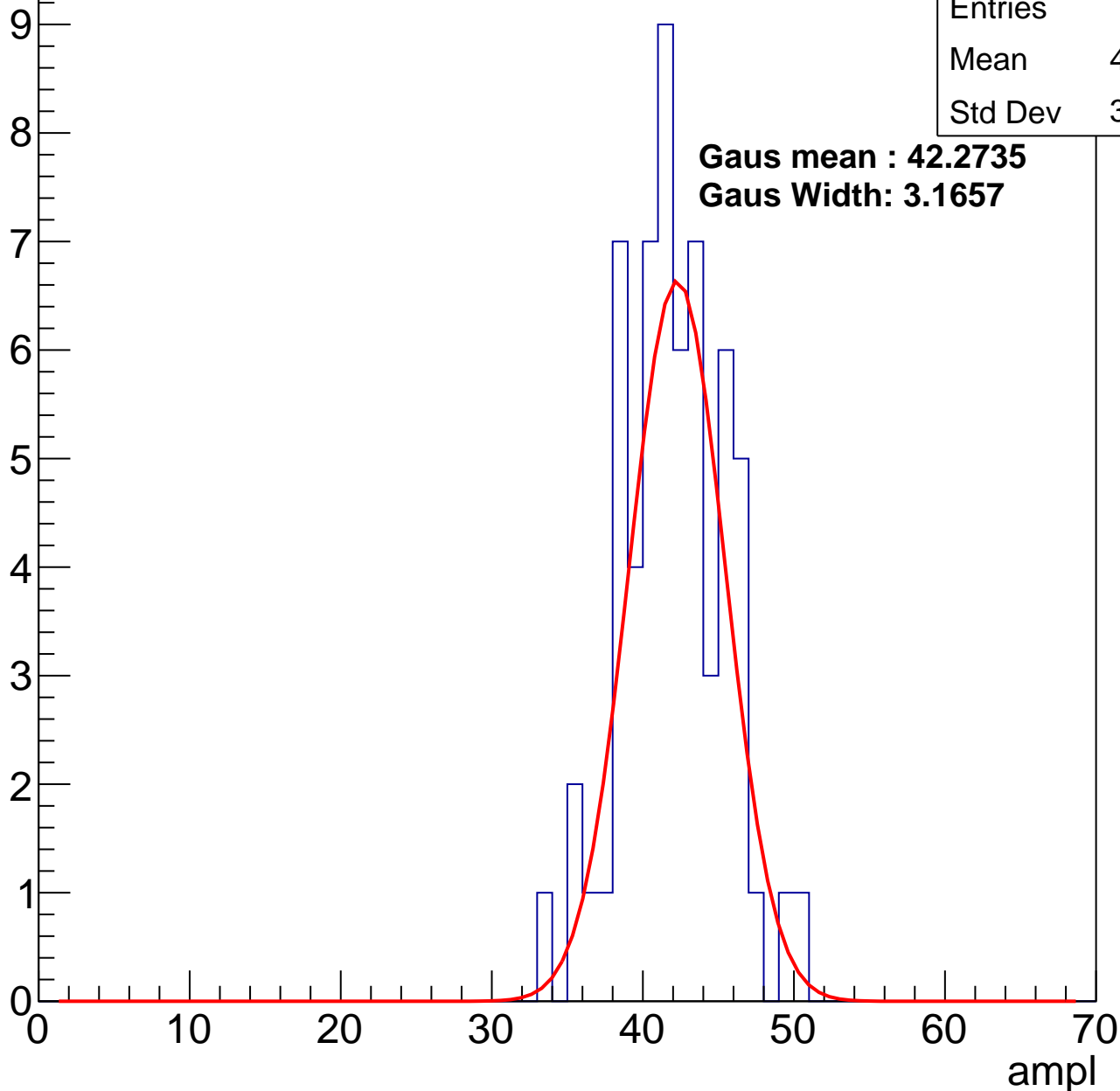
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	41.58
Std Dev	3.372

**Gaus mean : 42.2735**

**Gaus Width: 3.1657**

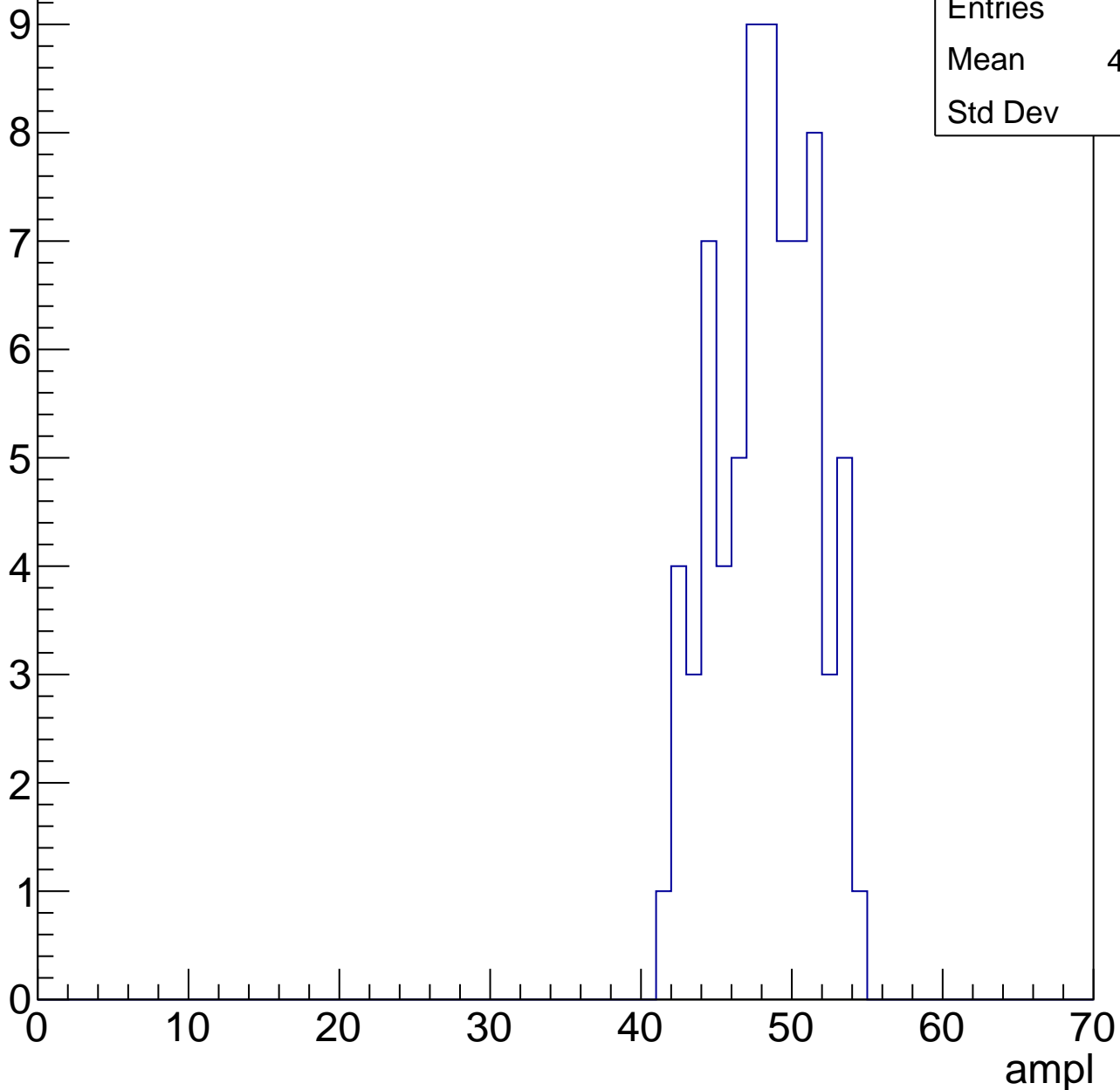


# B1L003S, U11-ch126, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

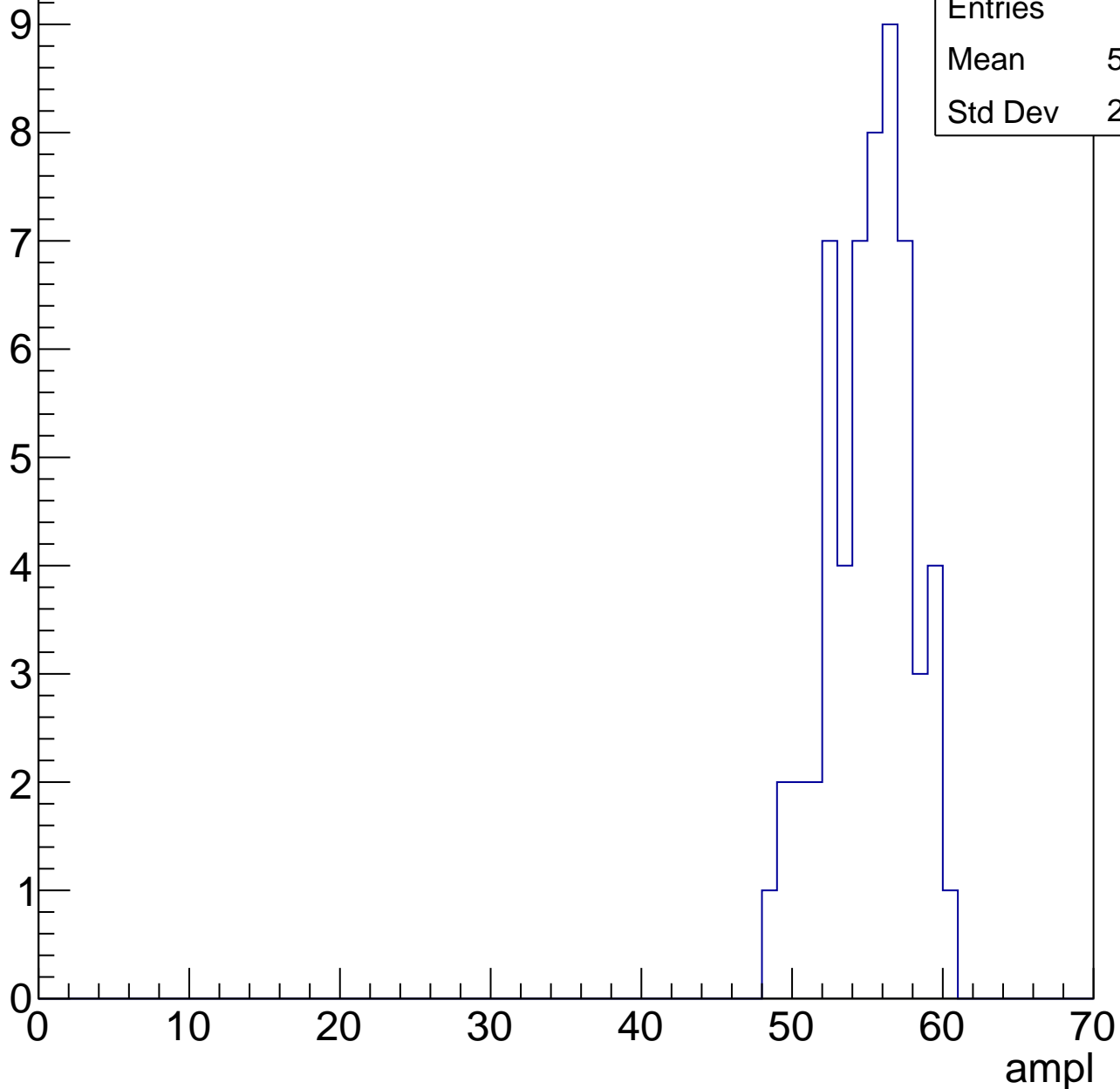
Entries	73
Mean	47.77
Std Dev	3.22



# B1L003S, U11-ch126, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U11-ch126, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	54
Mean	58.46
Std Dev	8.392

Entry

10

8

6

4

2

0

0

10

20

30

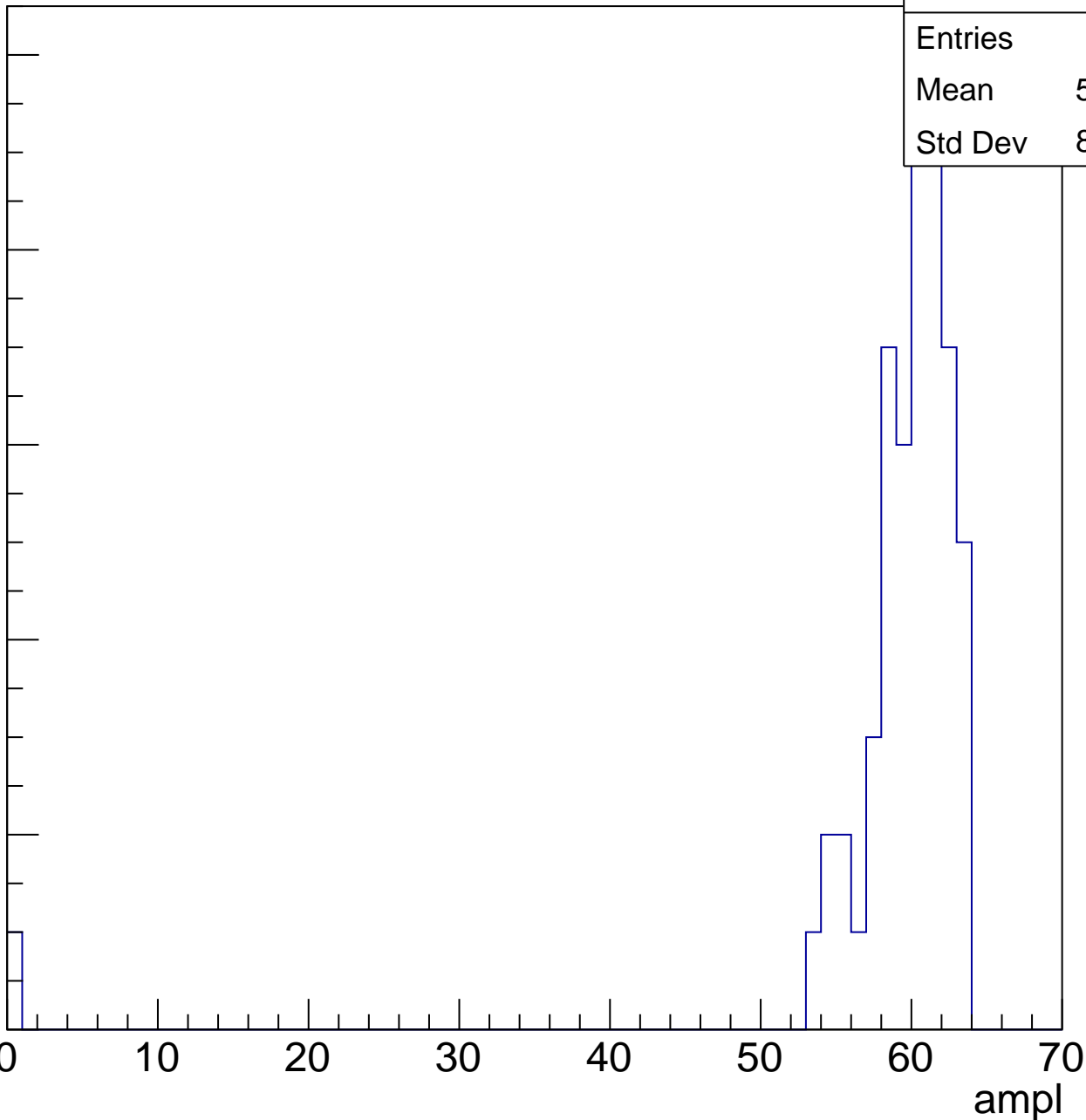
40

50

60

70

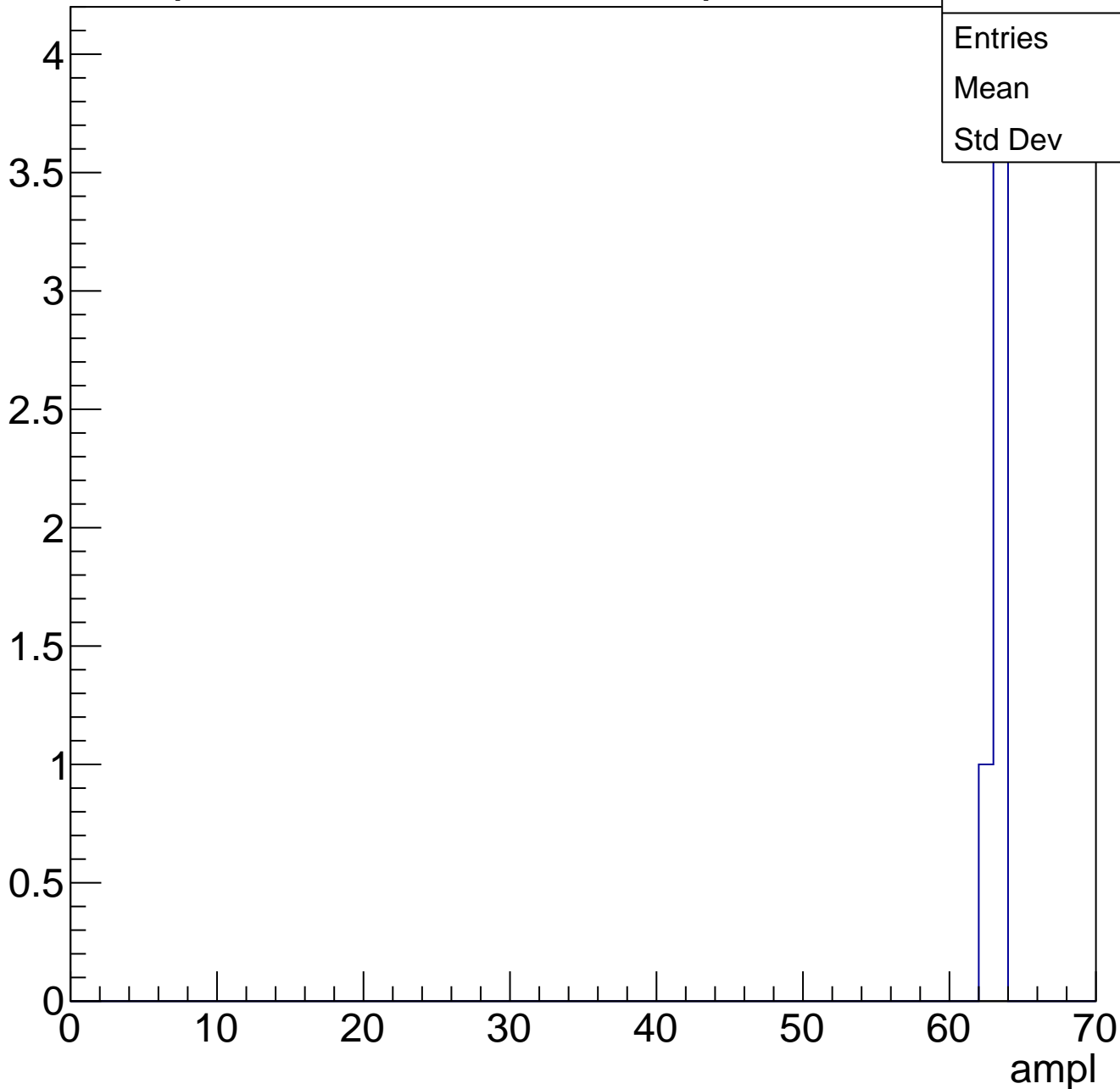
ampl



# B1L003S, U11-ch126, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch126, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

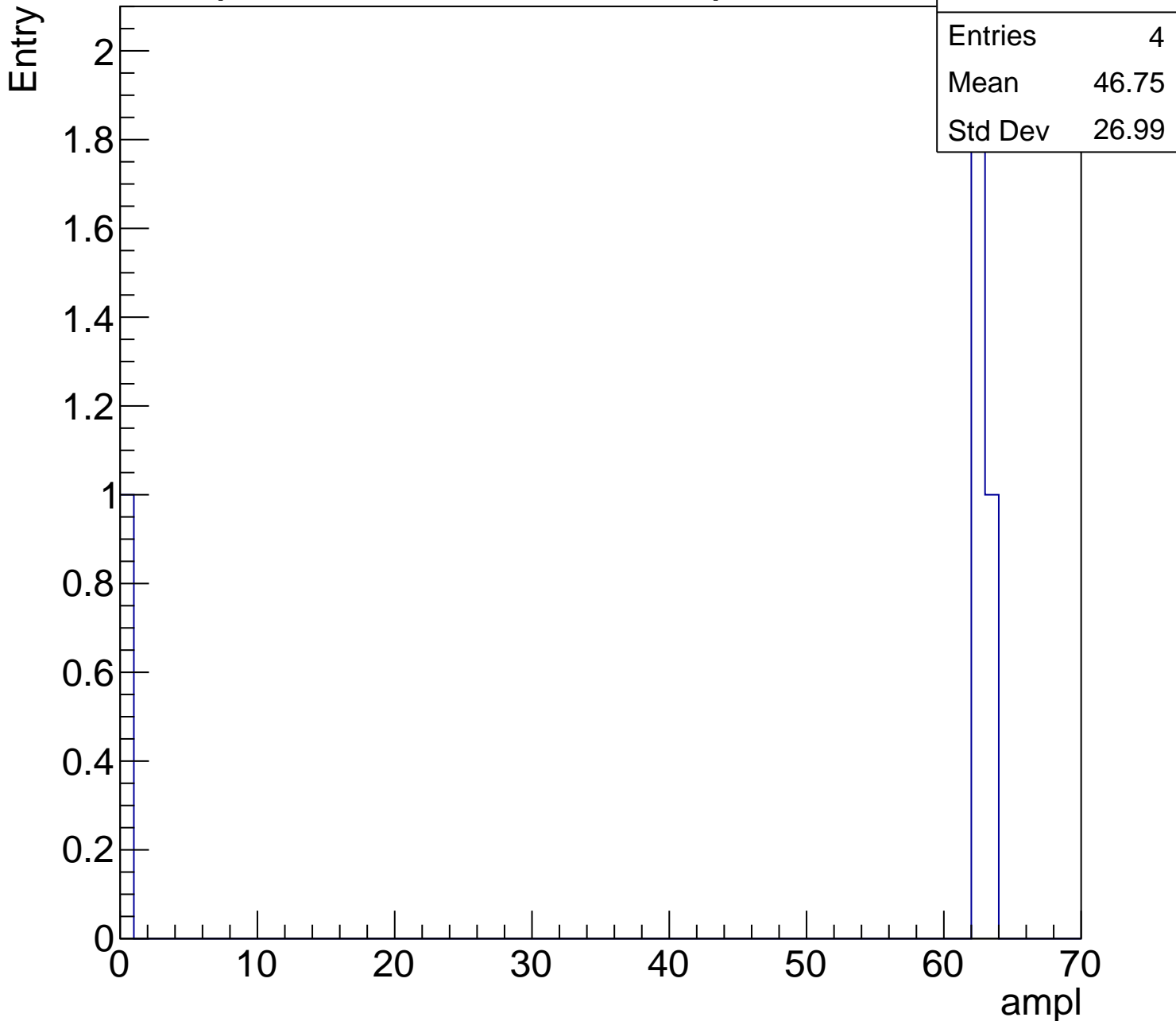
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	46.75
Std Dev	26.99

0 10 20 30 40 50 60 70

ampl



# B1L003S, U11-ch127, adc0

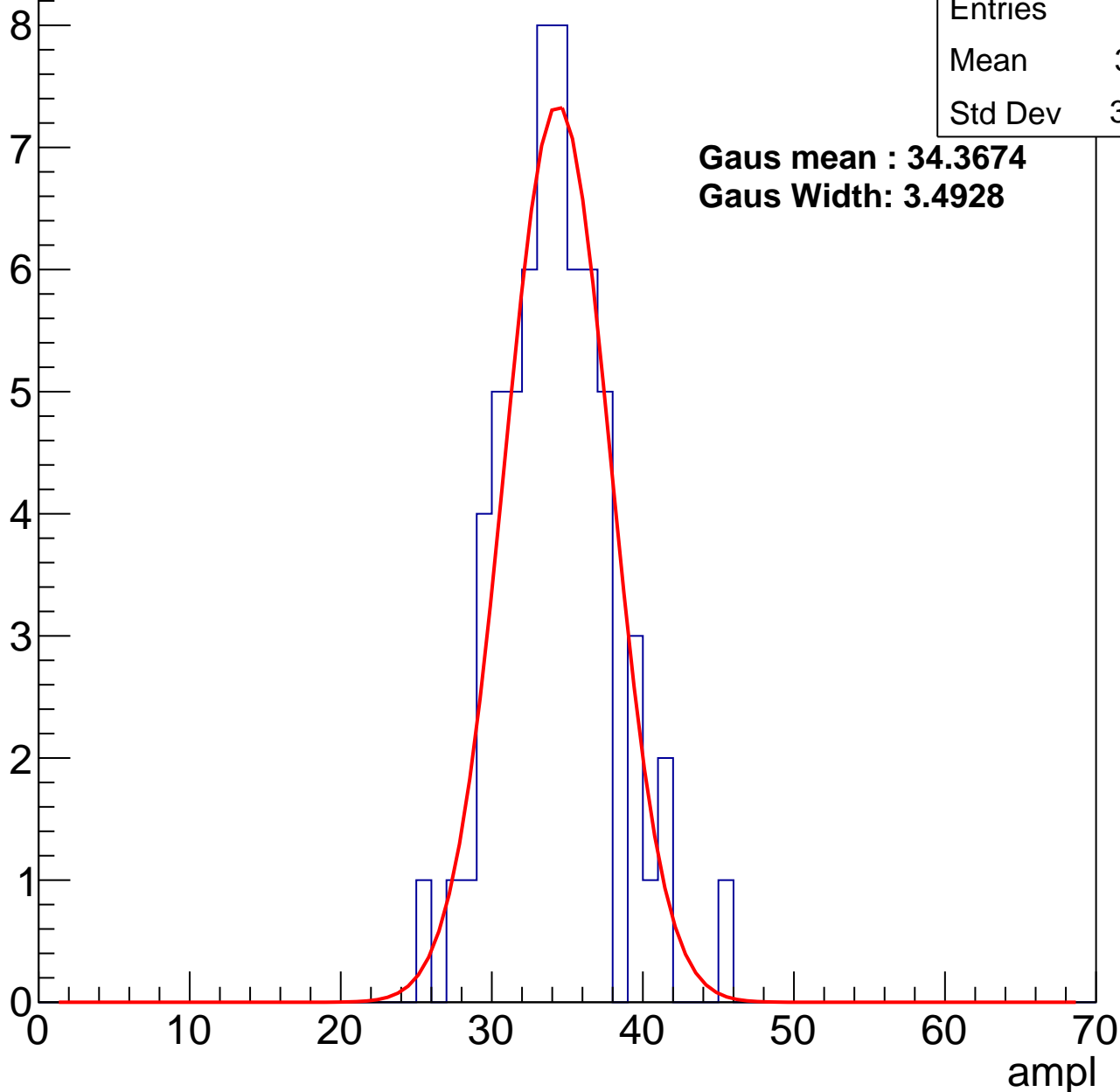
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	33.71
Std Dev	3.614

**Gaus mean : 34.3674**

**Gaus Width: 3.4928**



# B1L003S, U11-ch127, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	55
Mean	38.64
Std Dev	3.118

**Gaus mean : 39.2077**

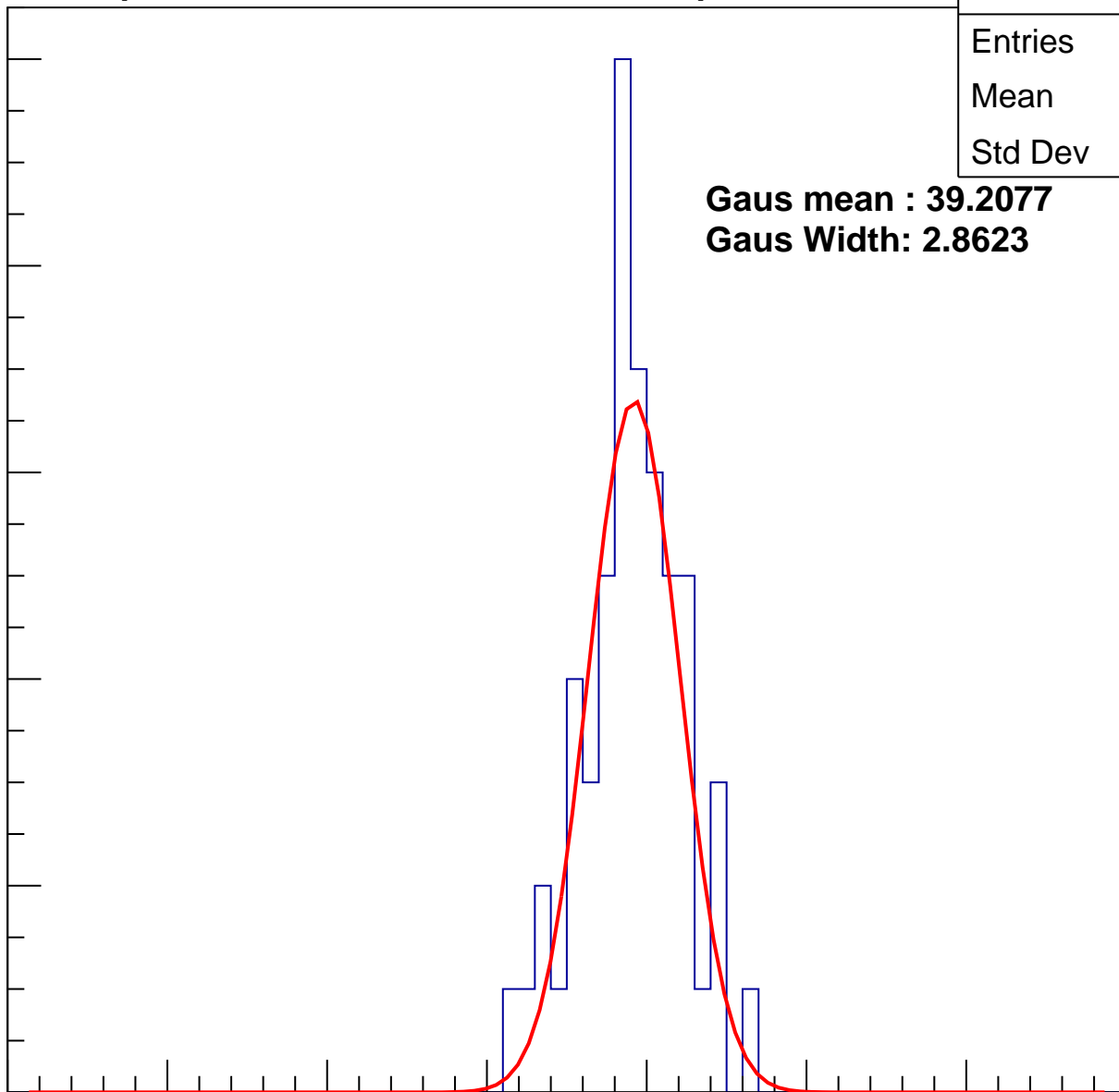
**Gaus Width: 2.8623**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L003S, U11-ch127, adc2

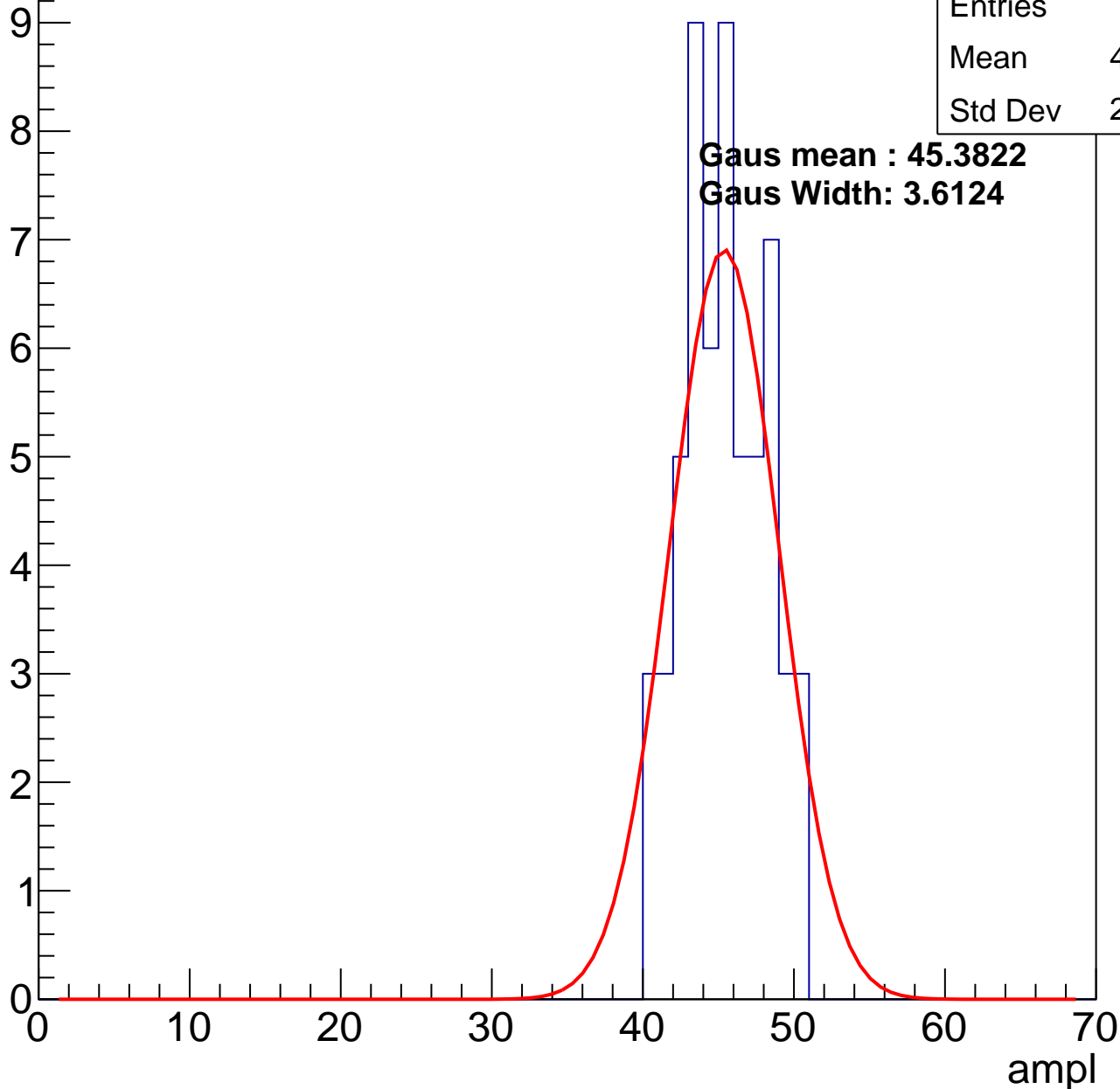
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	44.95
Std Dev	2.694

**Gaus mean : 45.3822**

**Gaus Width: 3.6124**



# B1L003S, U11-ch127, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

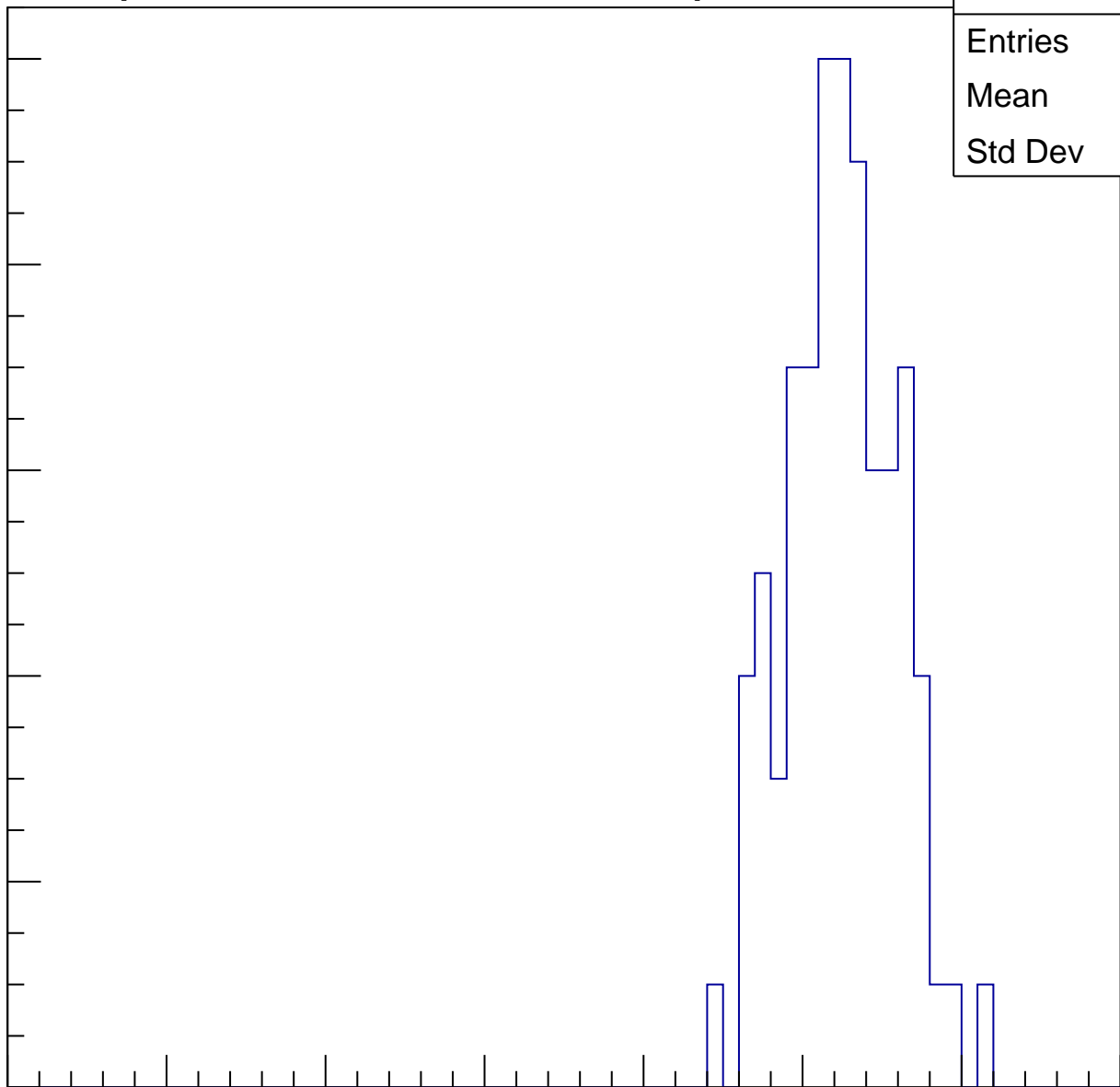
Entries	82
Mean	51.94
Std Dev	3.398

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

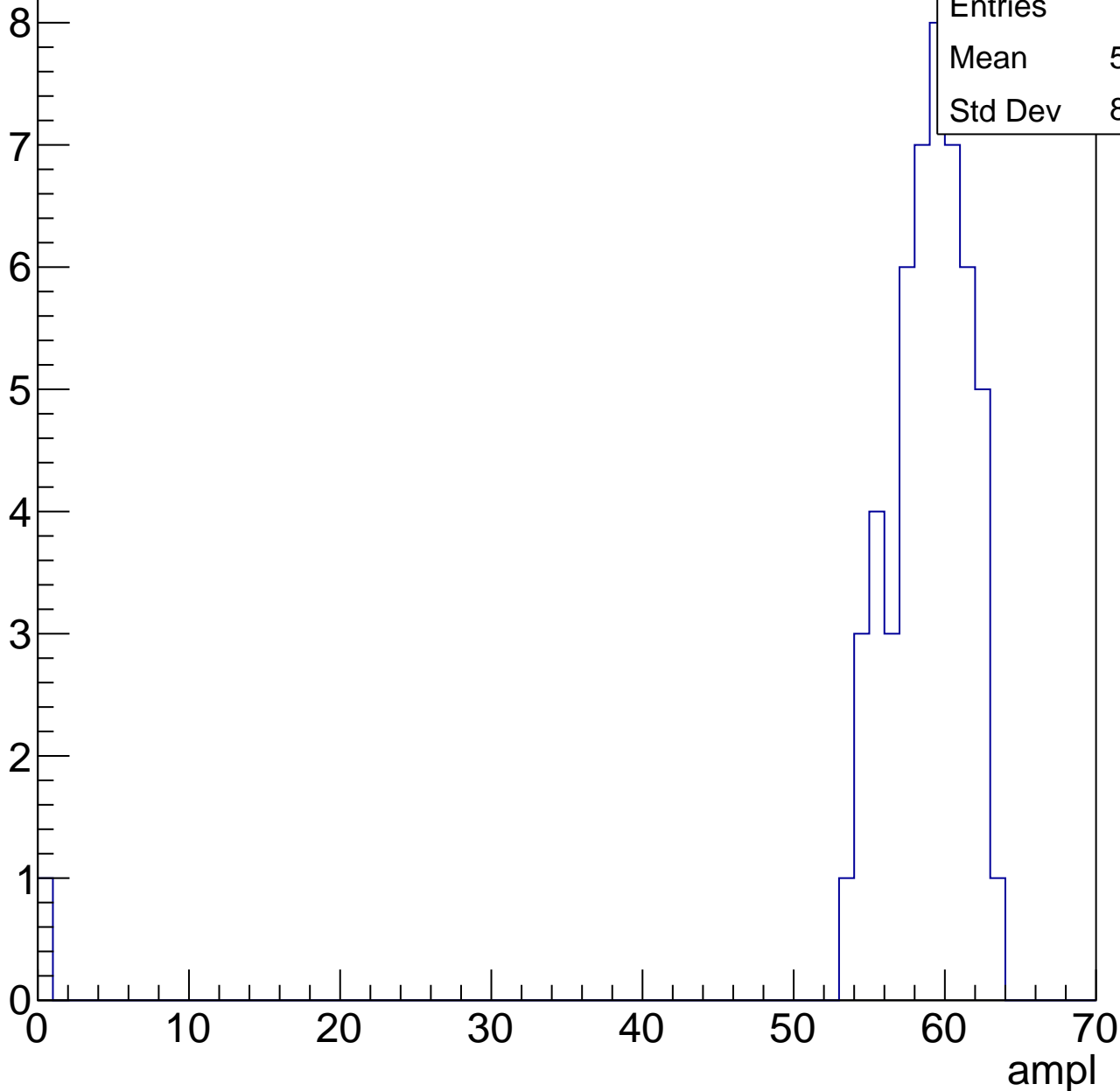


# B1L003S, U11-ch127, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	52
Mean	57.35
Std Dev	8.394

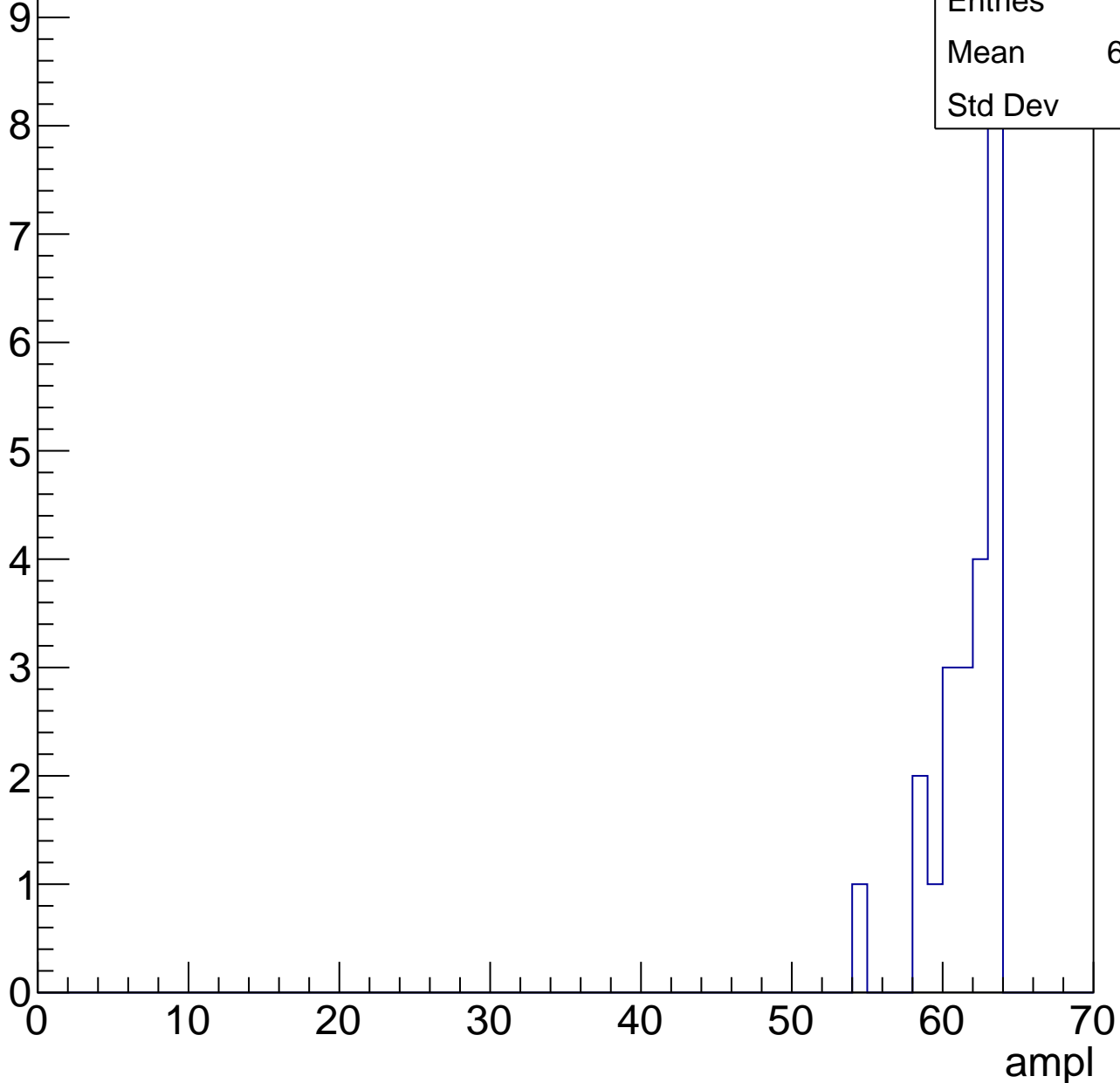


# B1L003S, U11-ch127, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	23
Mean	61.17
Std Dev	2.22



# B1L003S, U11-ch127, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U11-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U11-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0