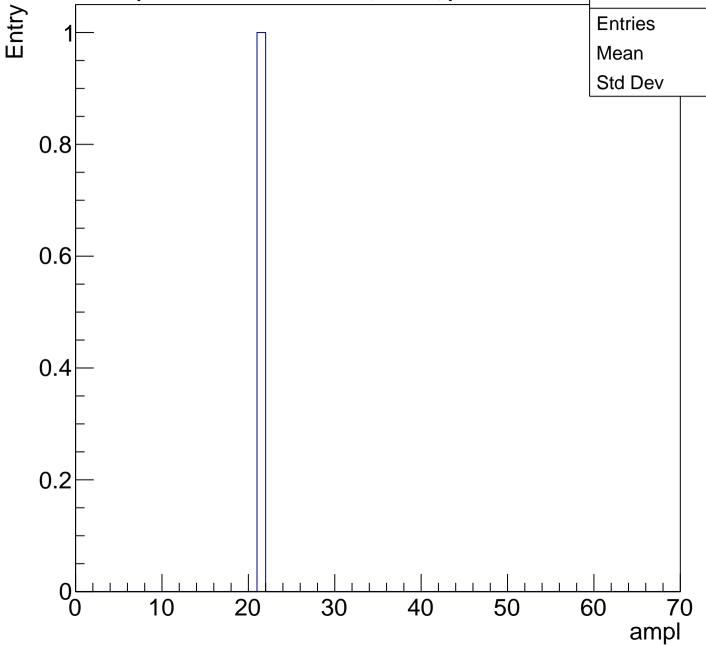


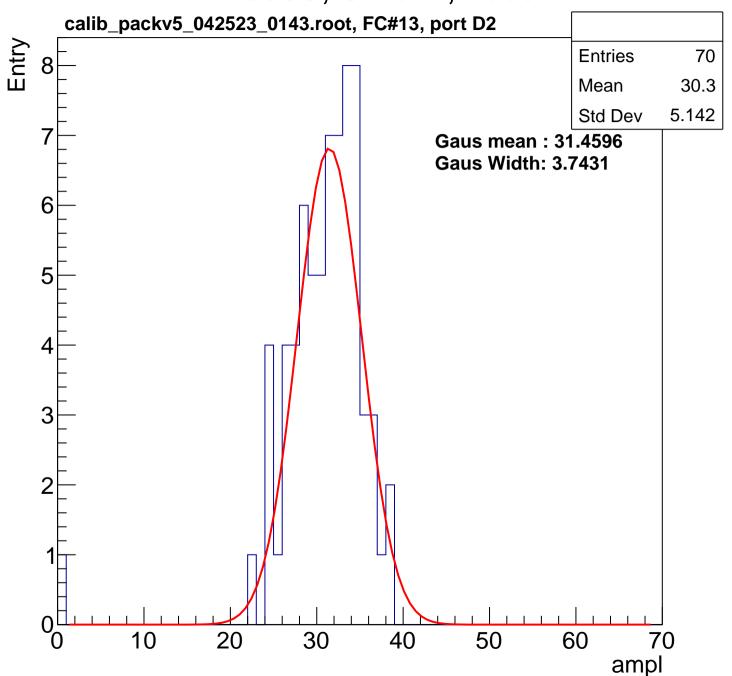
B1L003S, U2-ch0, adc7 calib_packv5_042523_0143.root, FC#13, port D2 **Entries** Mean

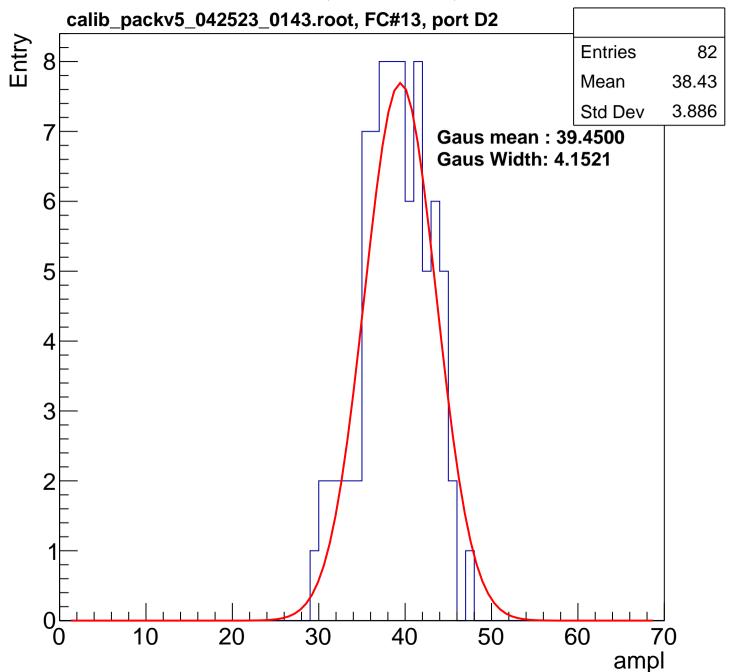
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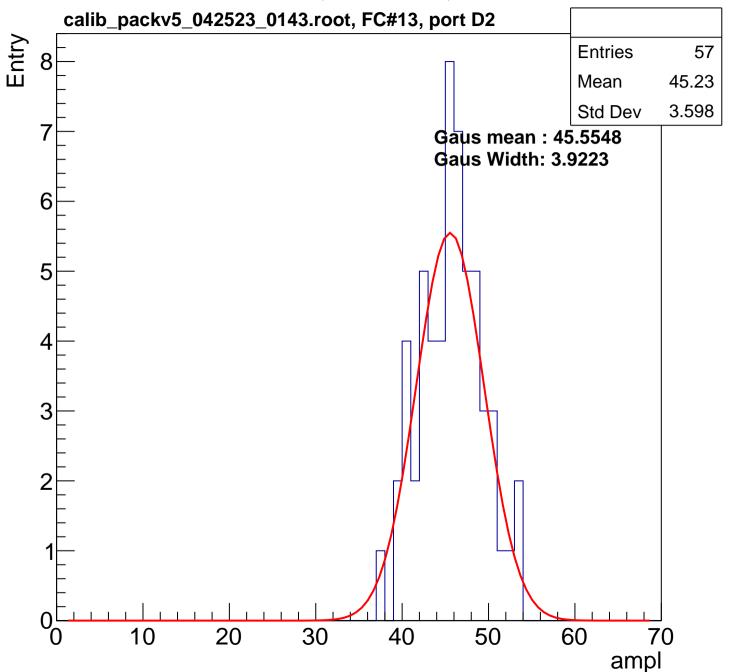
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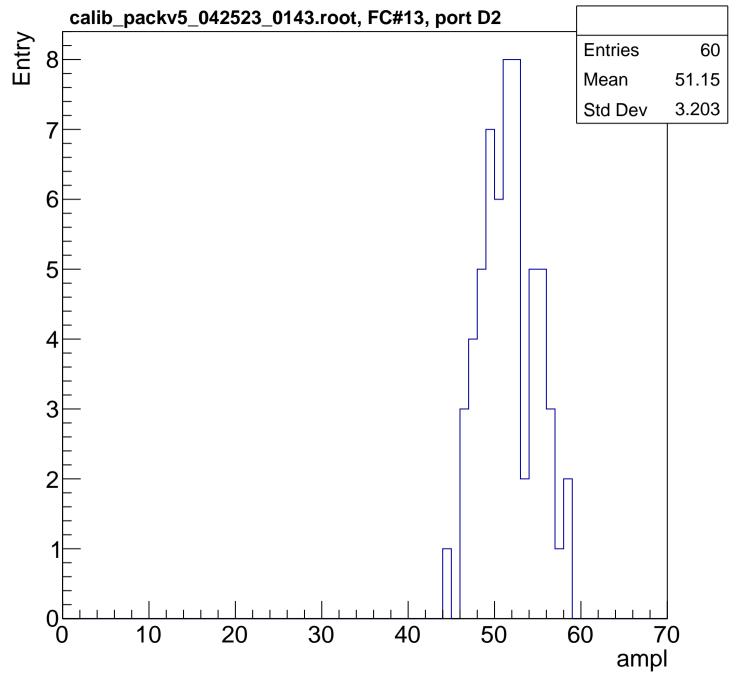
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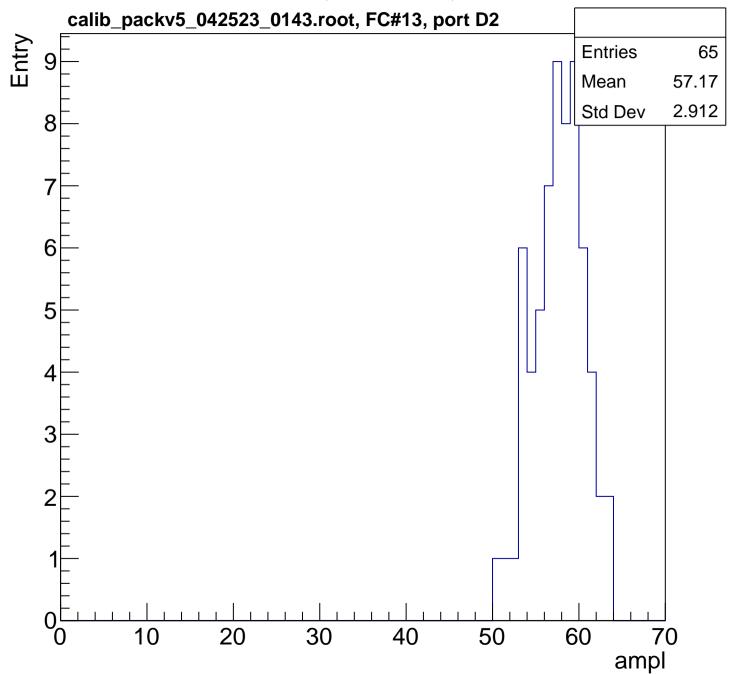


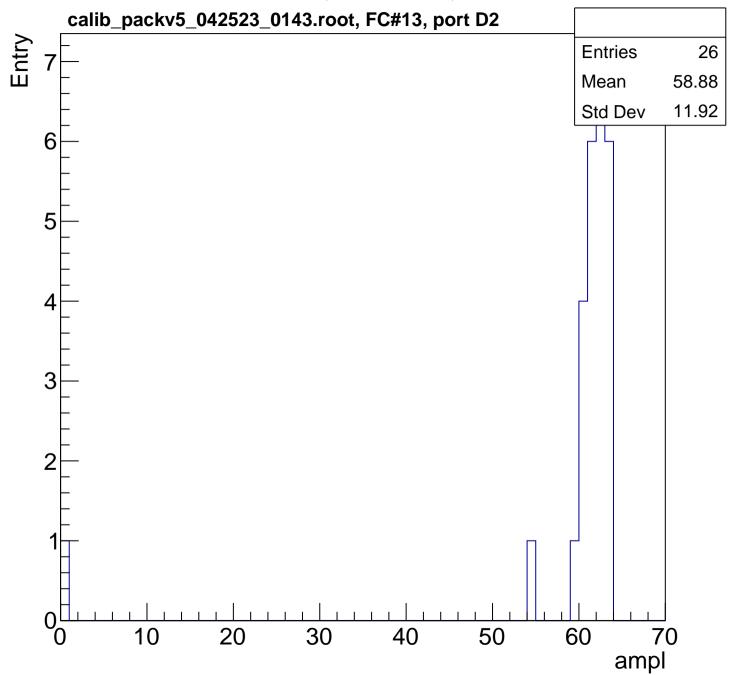


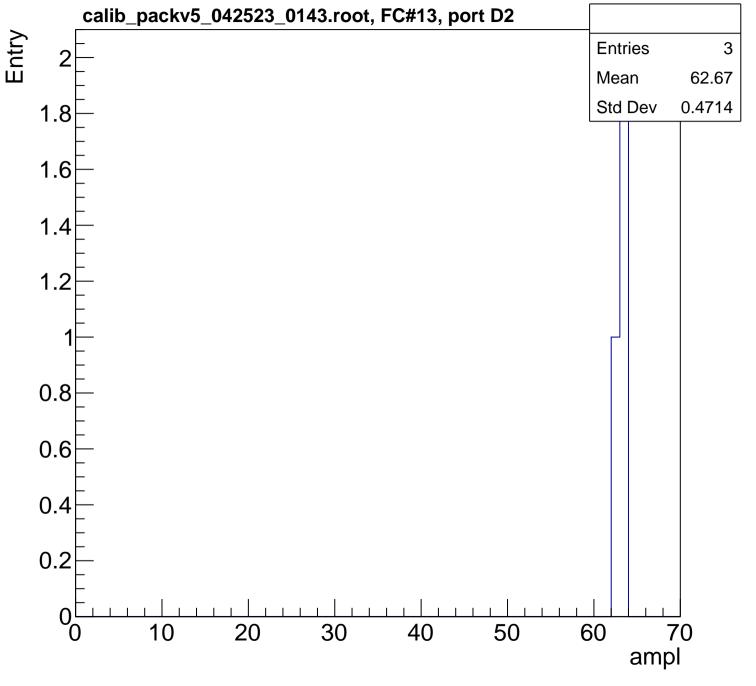




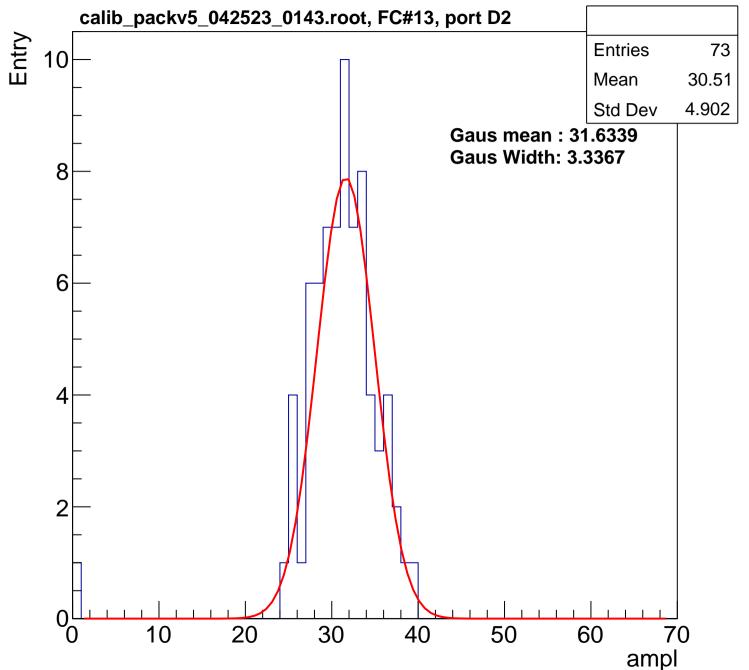


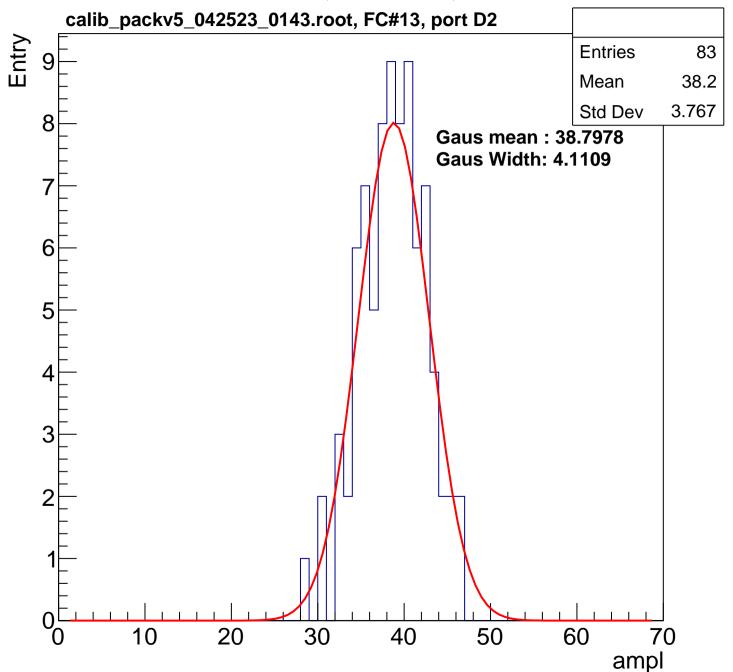


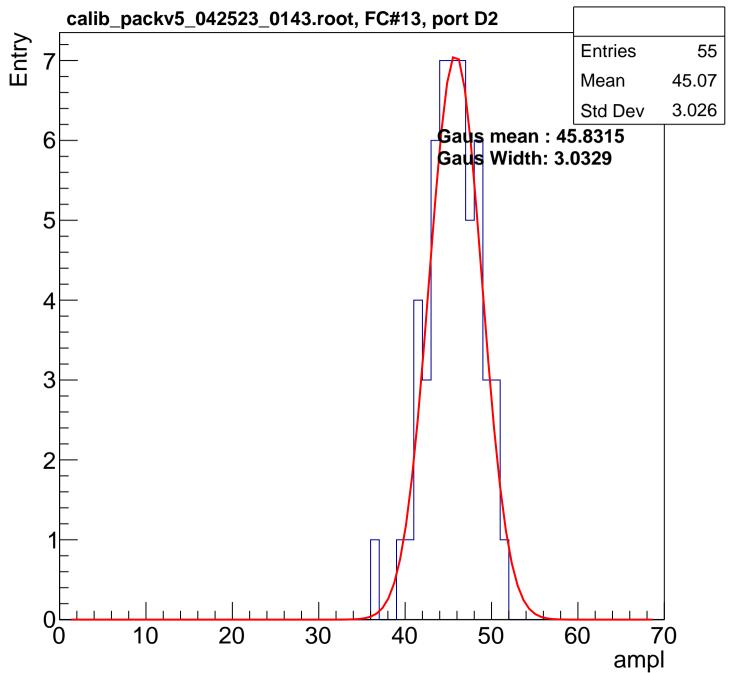


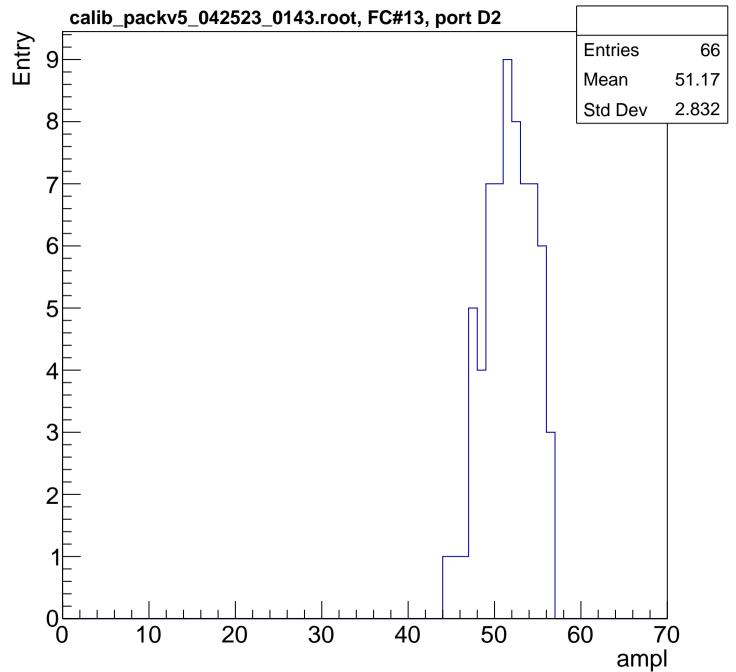


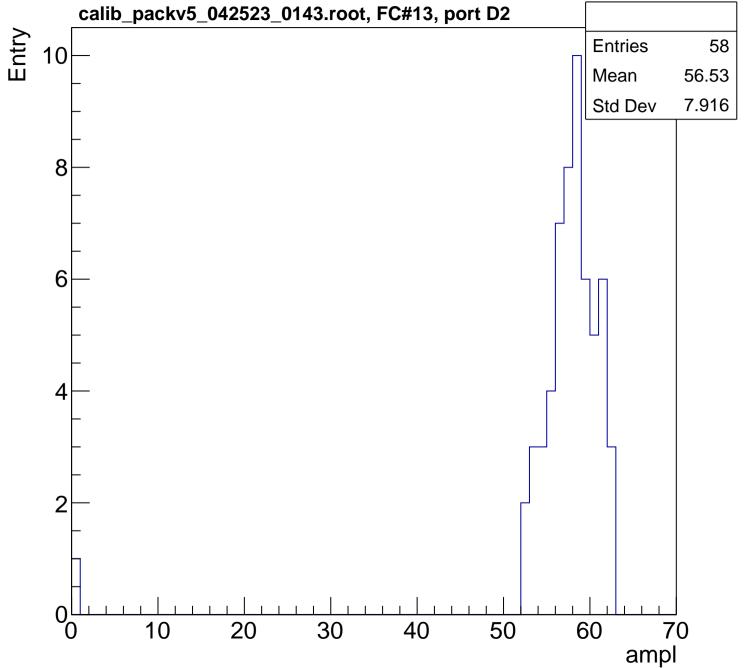
B1L003S, U2-ch1, adc7 calib_packv5_042523_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

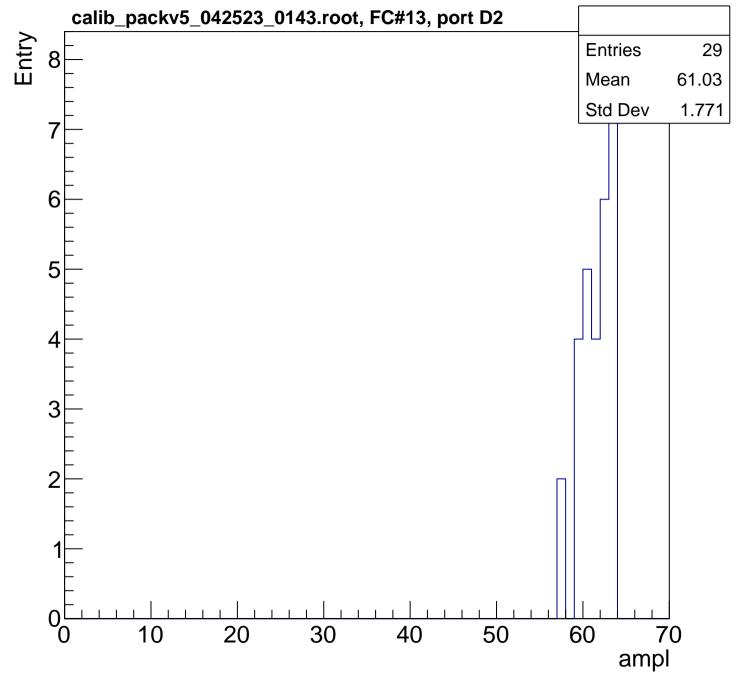


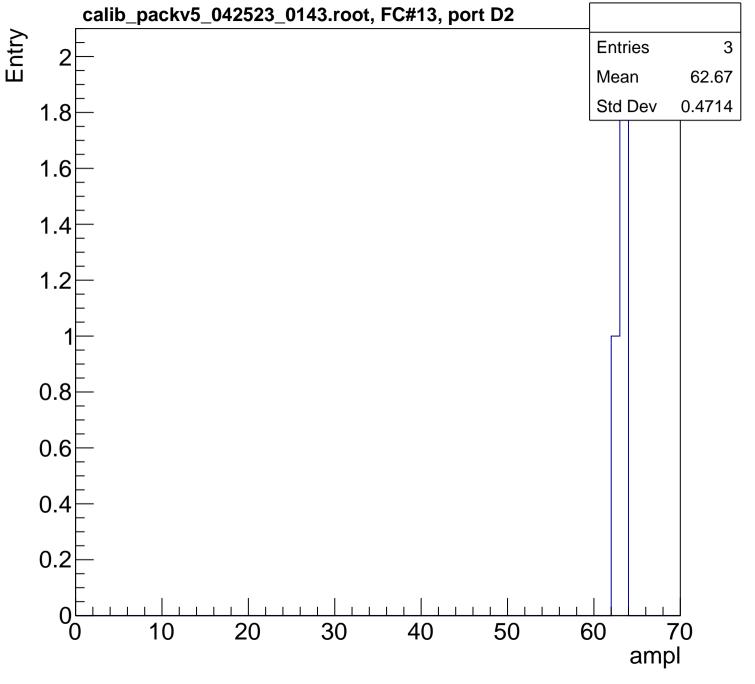


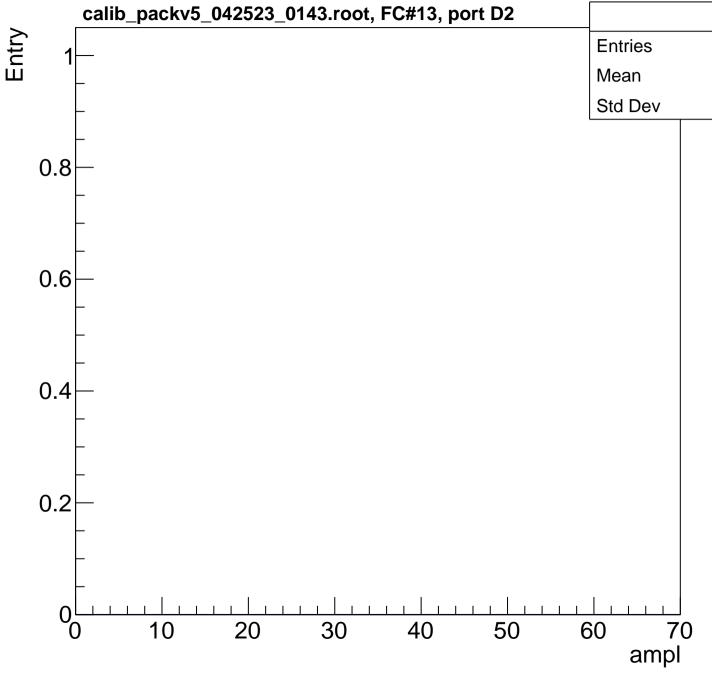


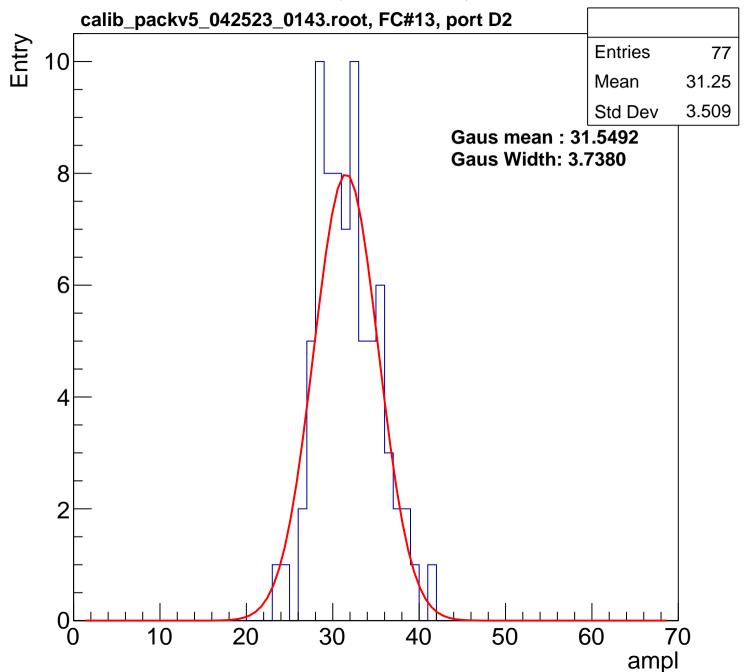


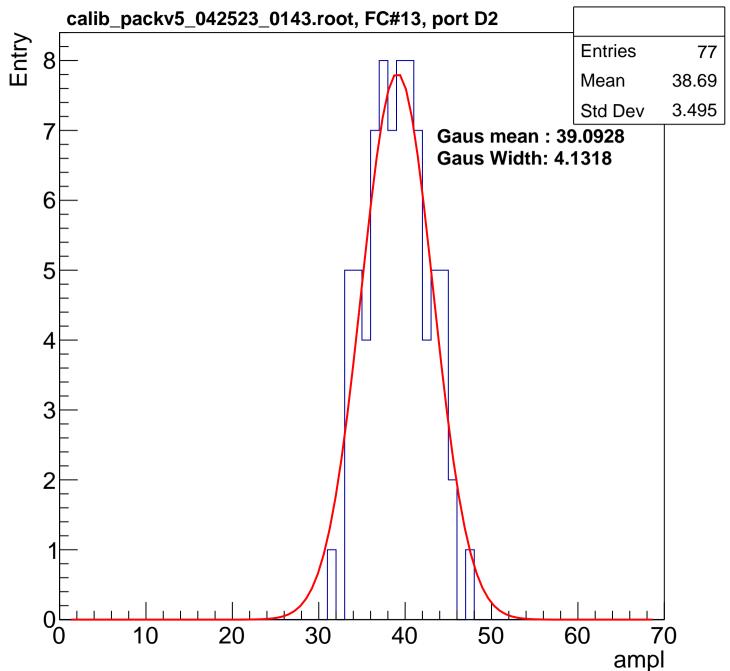


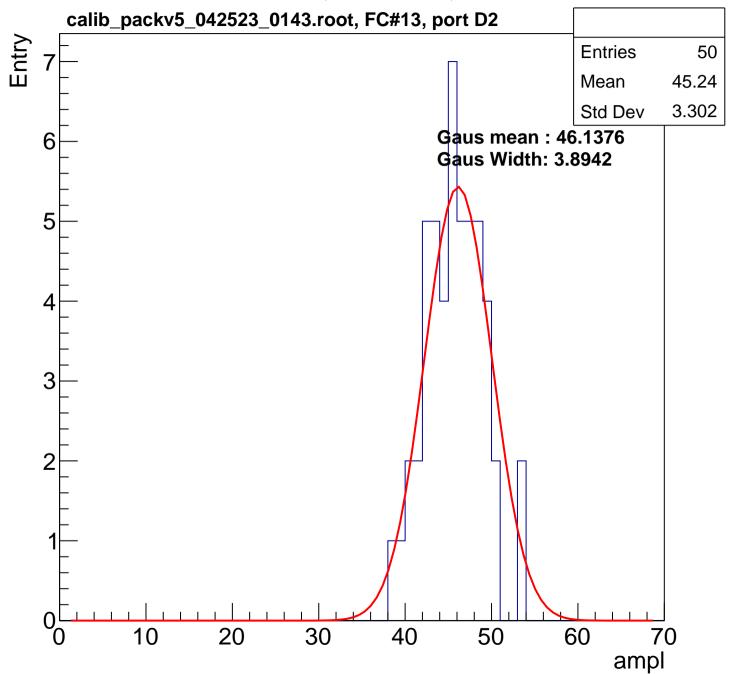


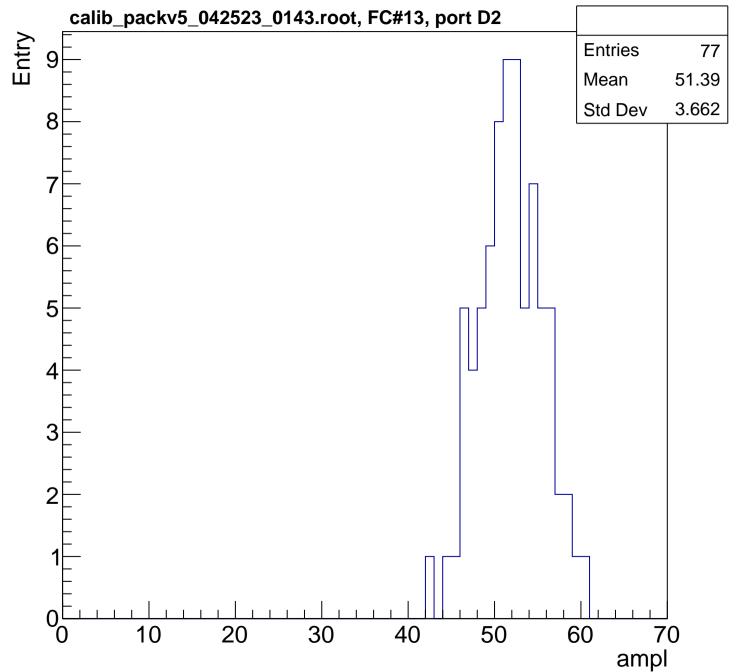


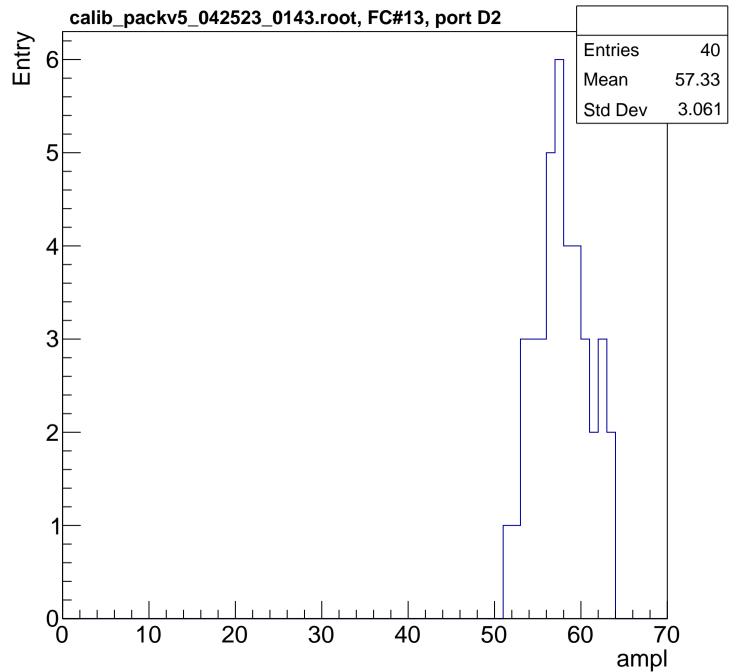


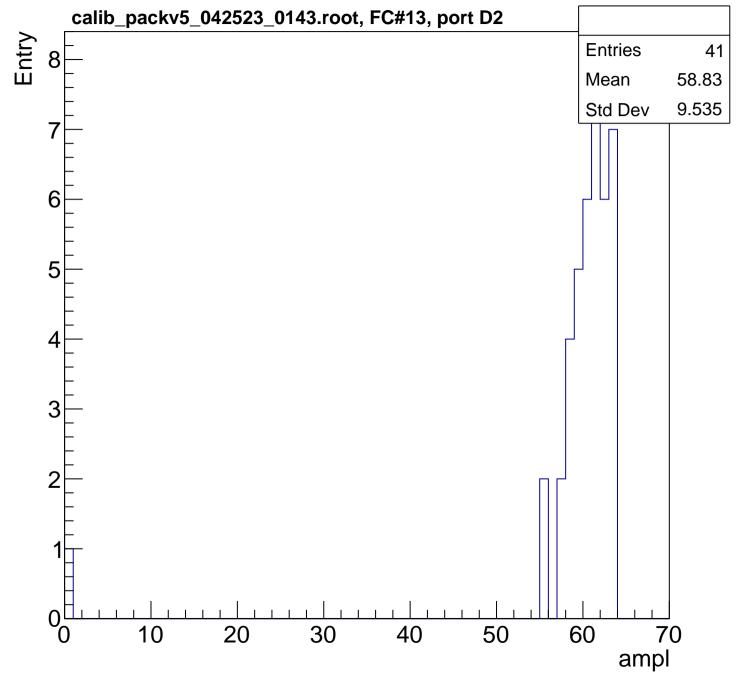


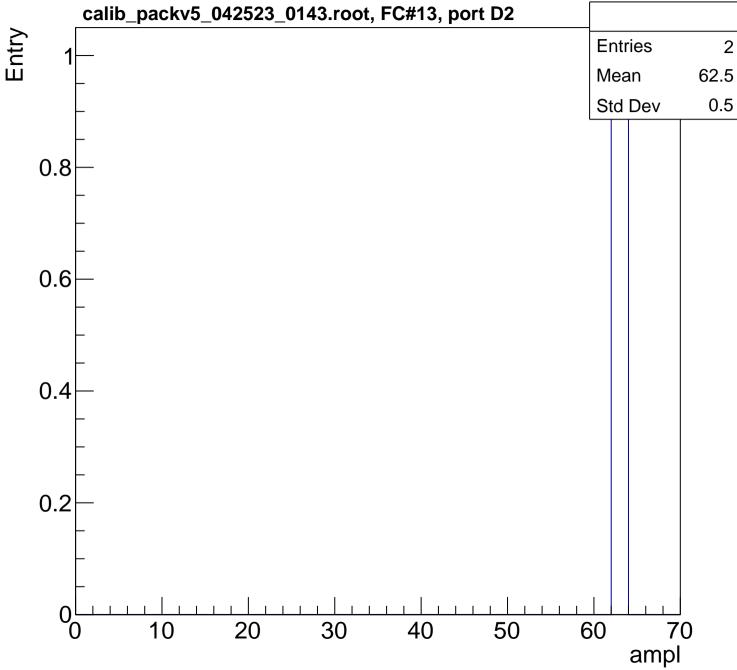


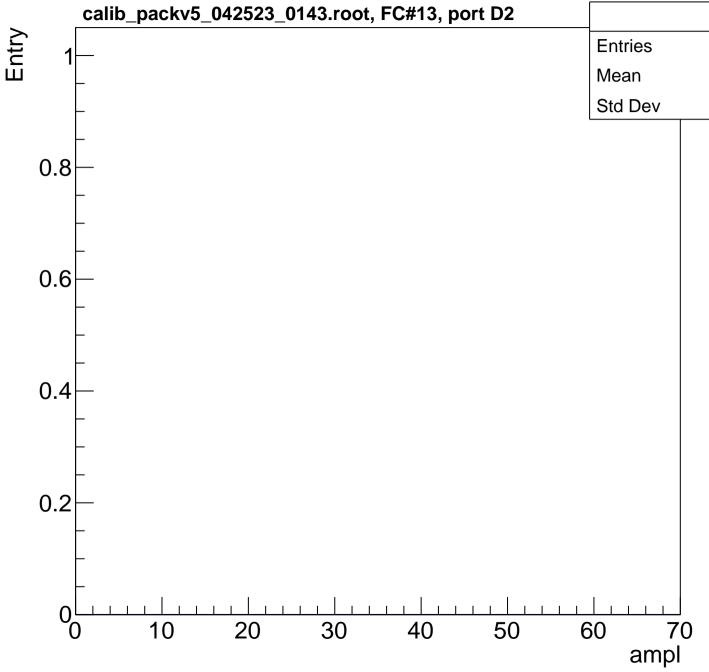


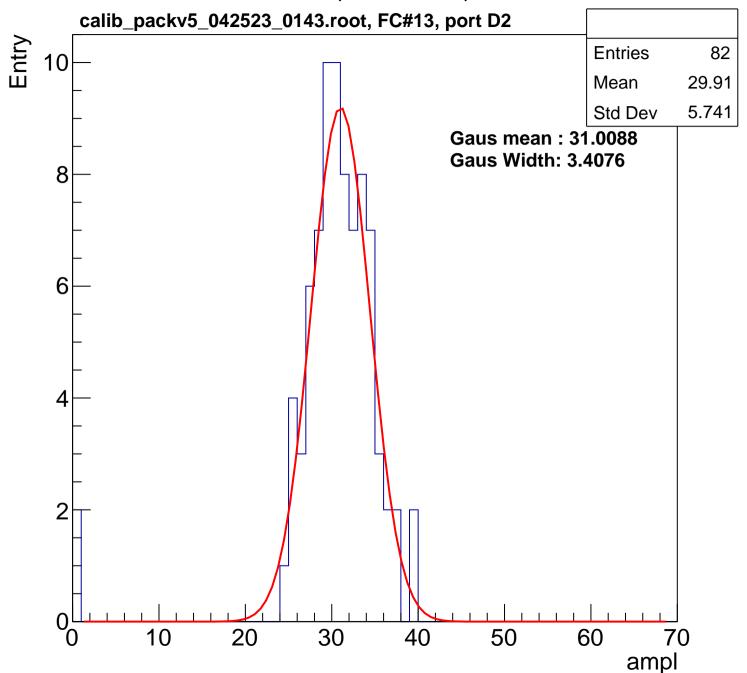


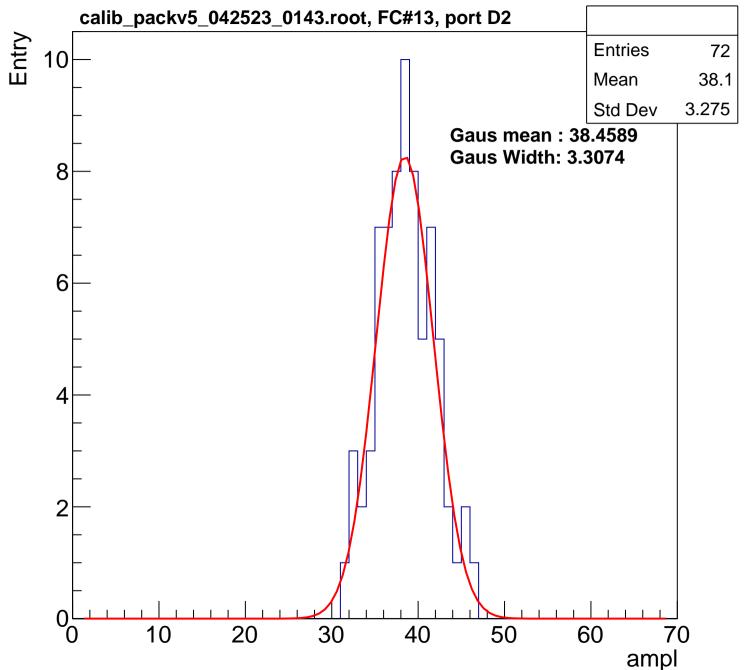


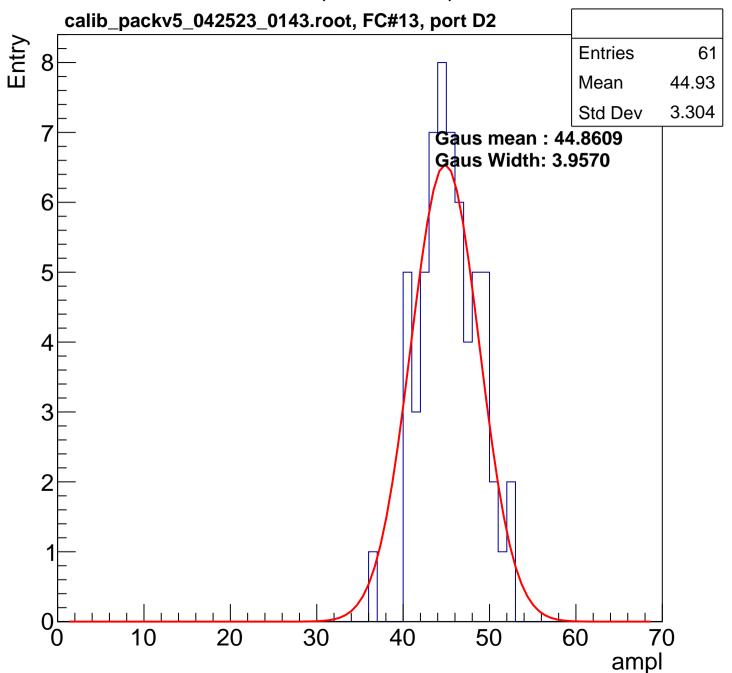


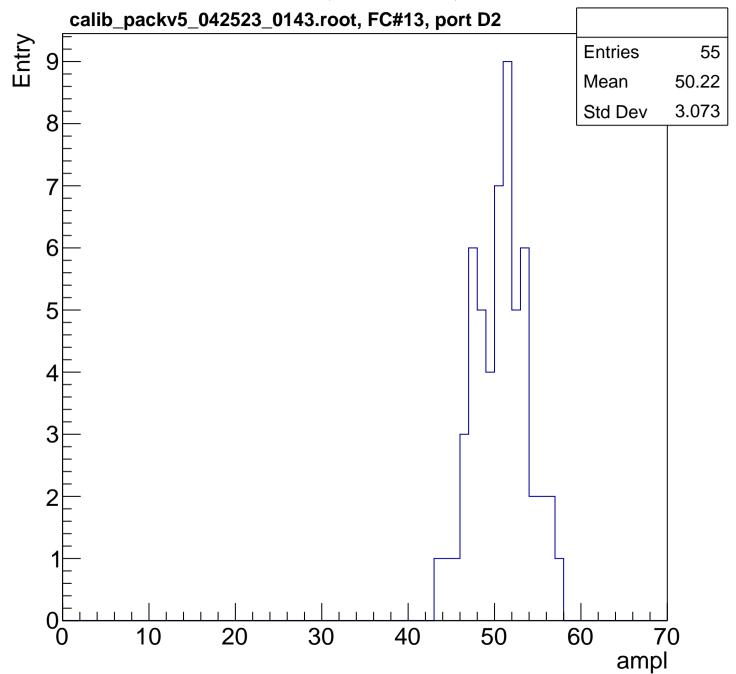


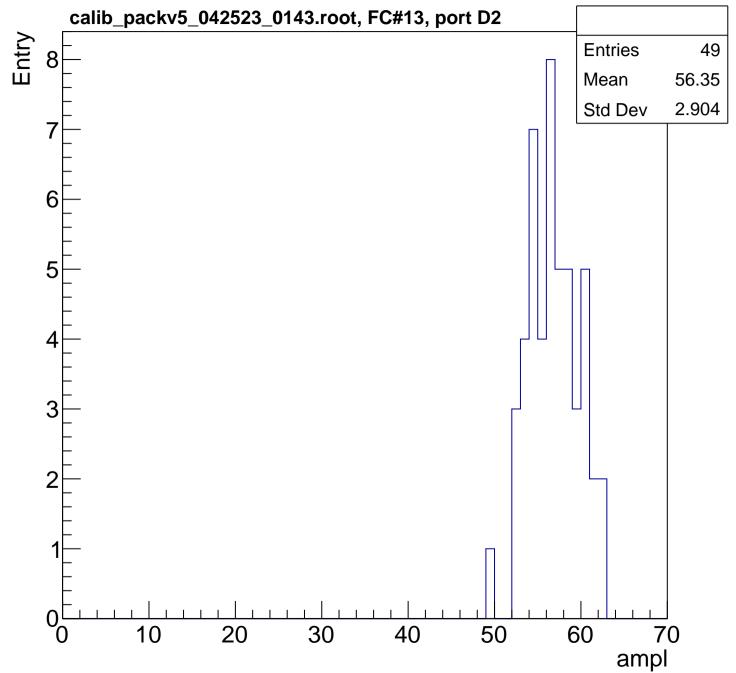


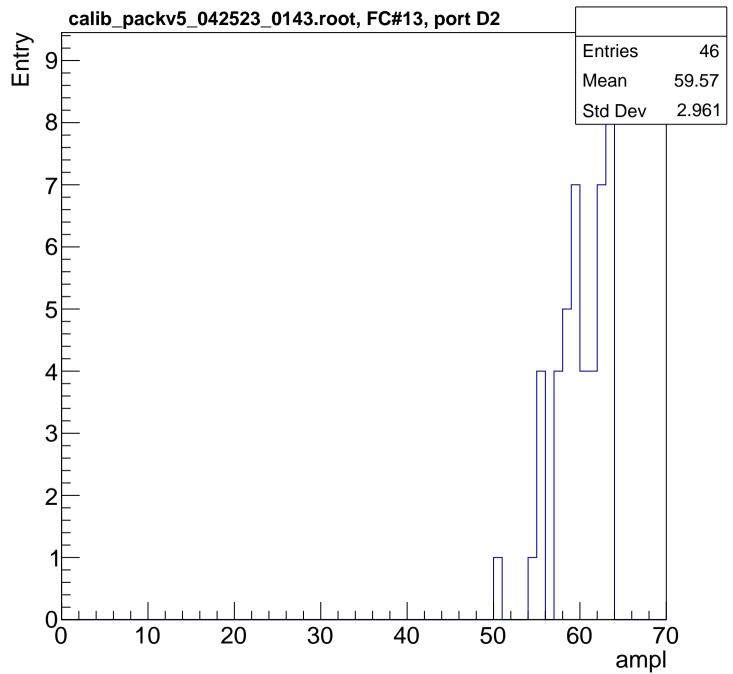


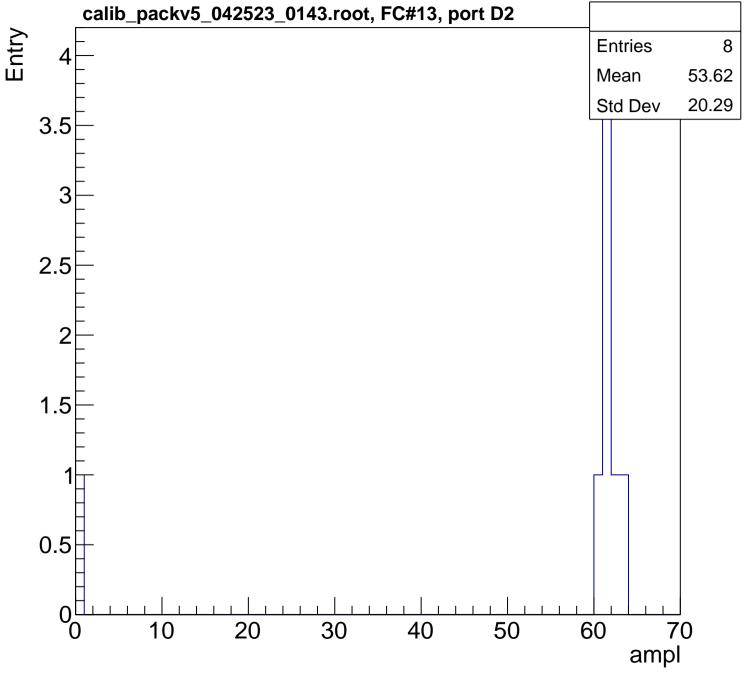


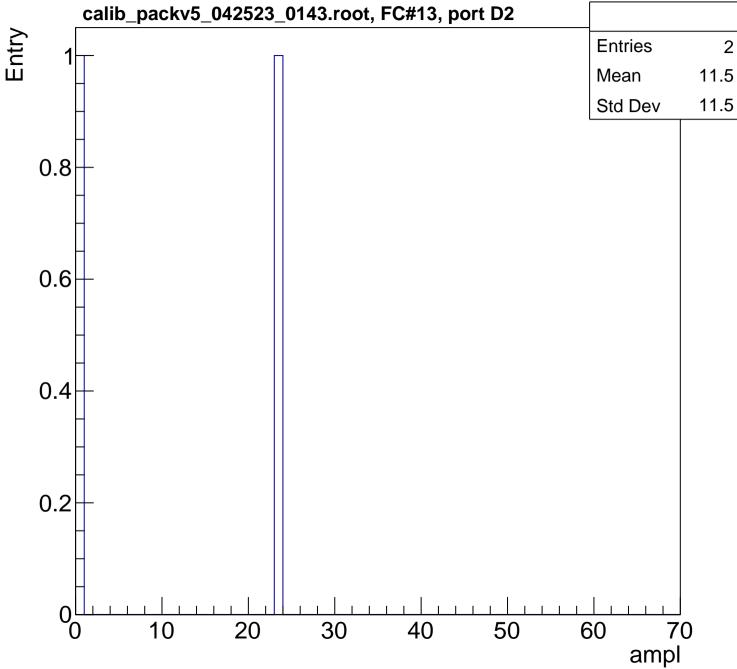


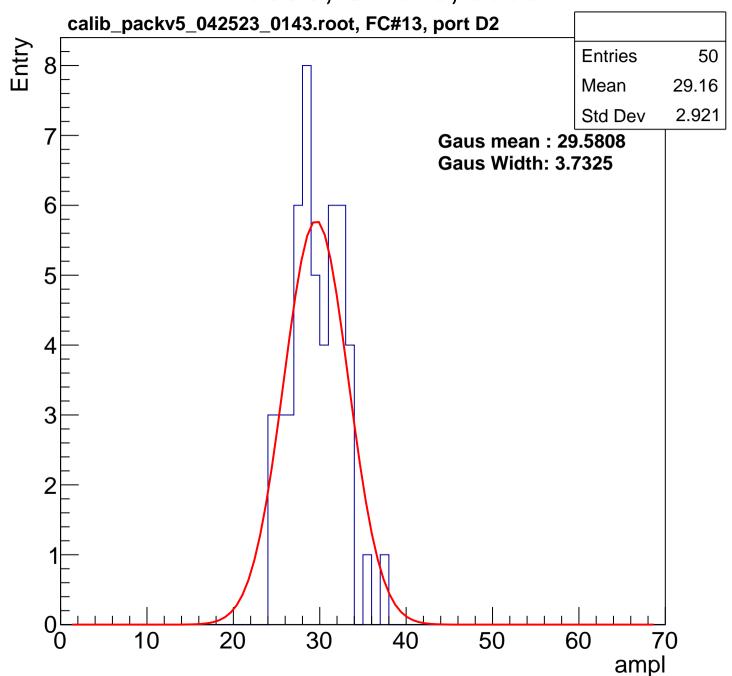


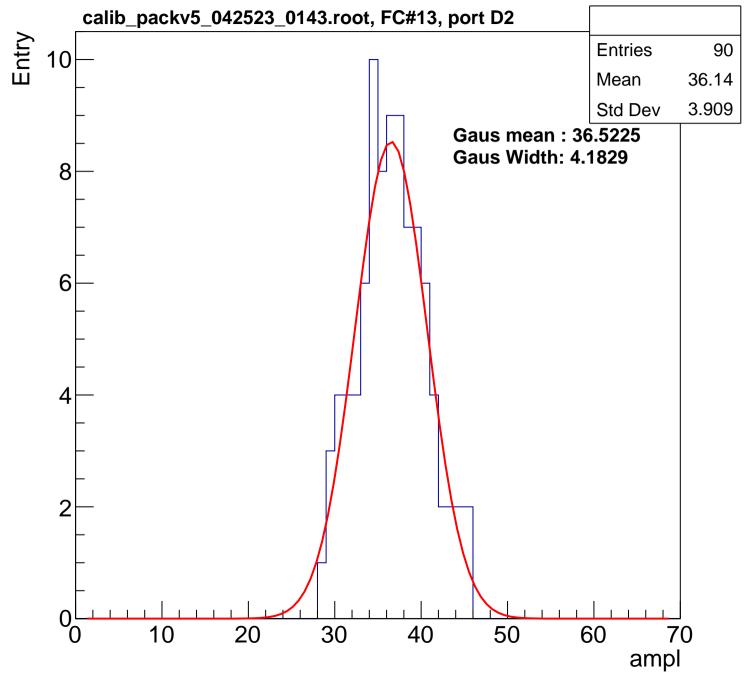


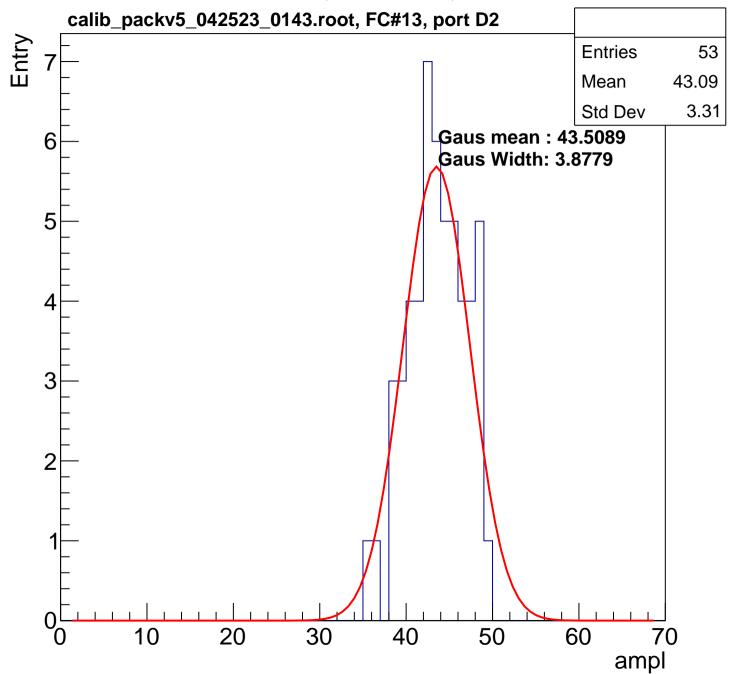


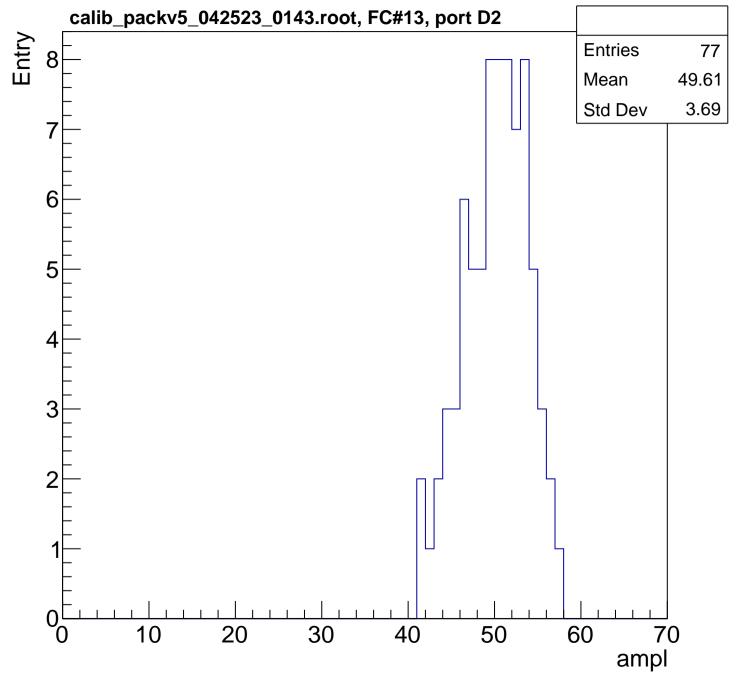


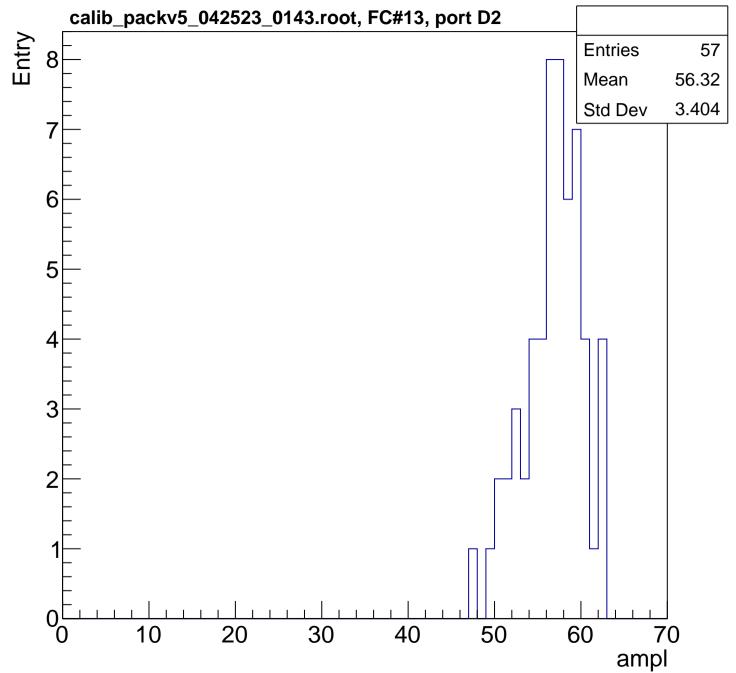


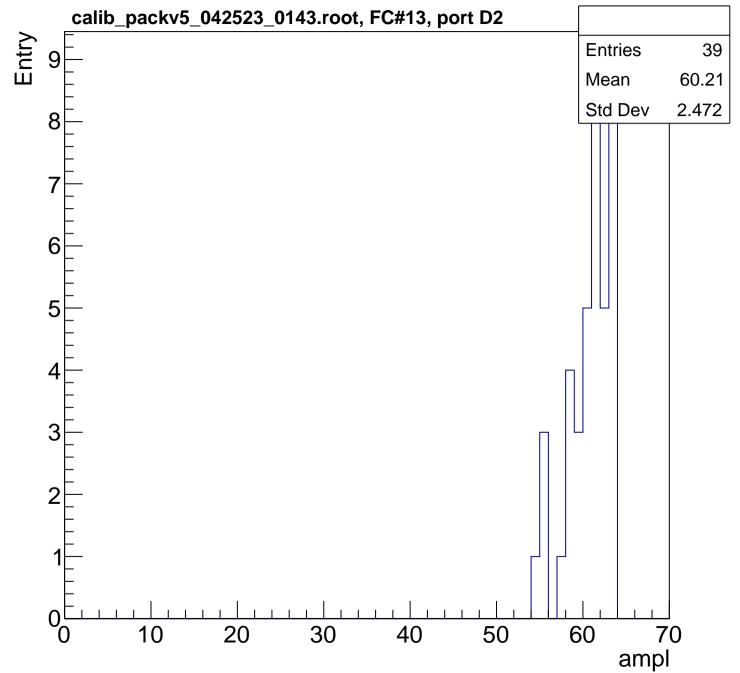


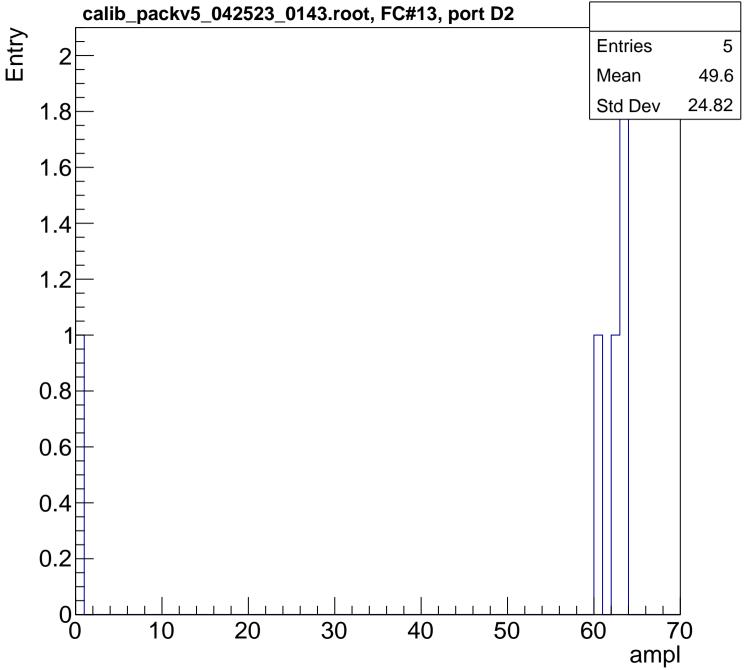


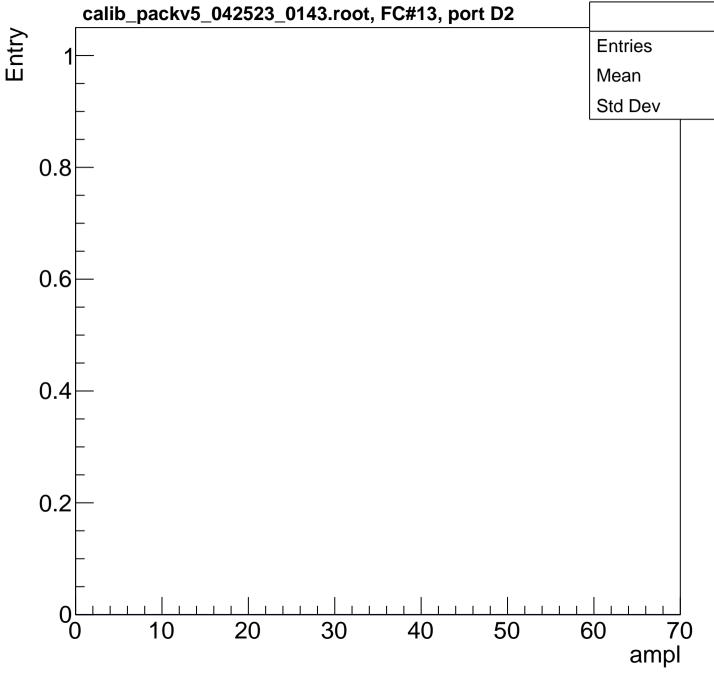


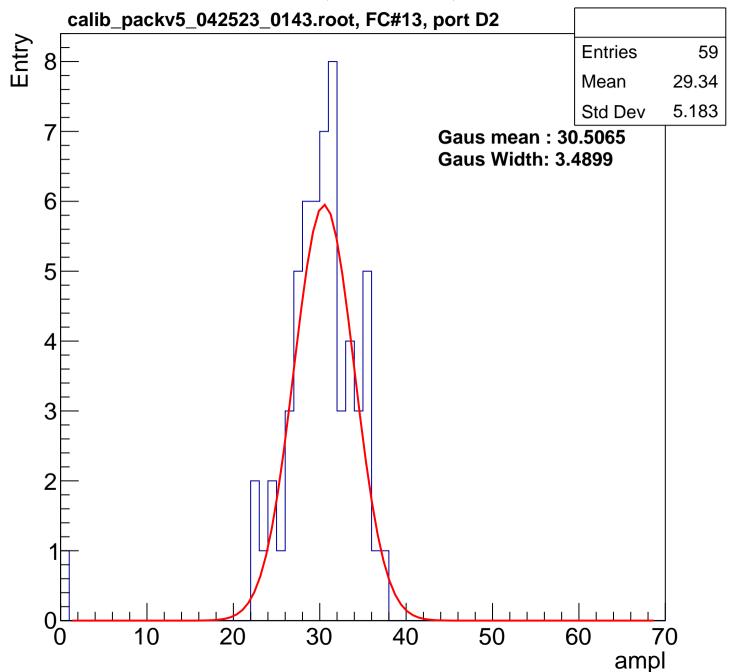


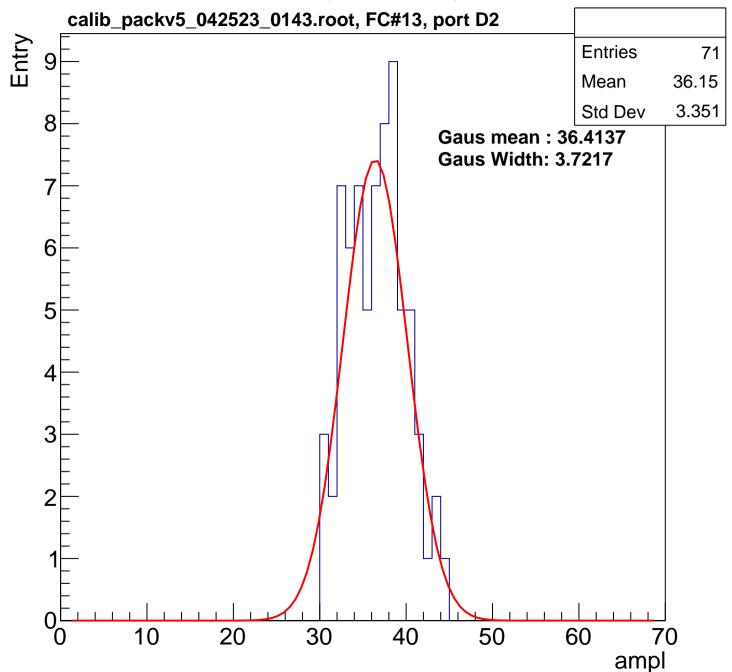


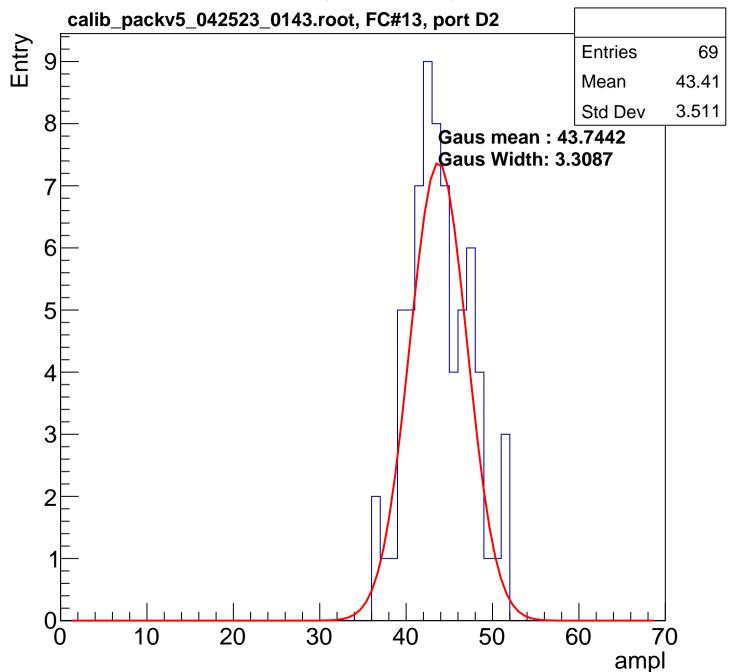


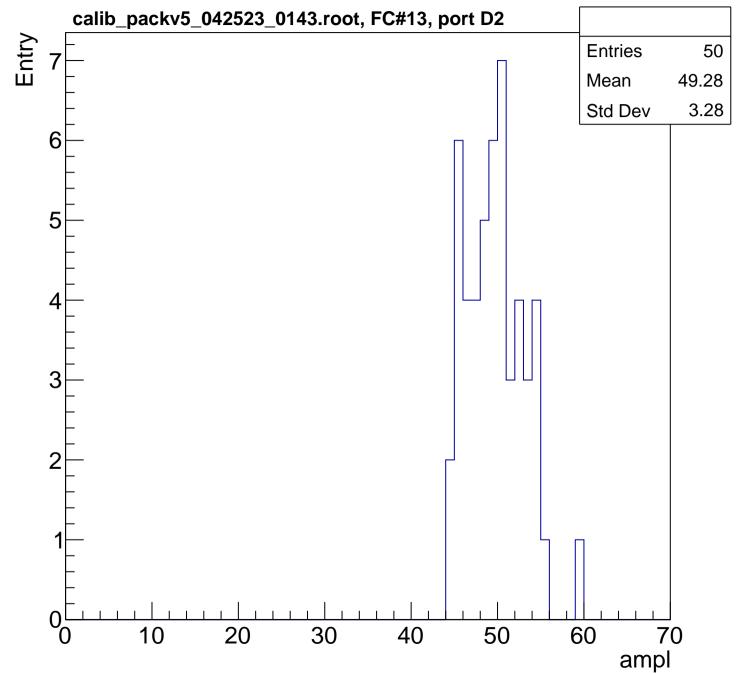


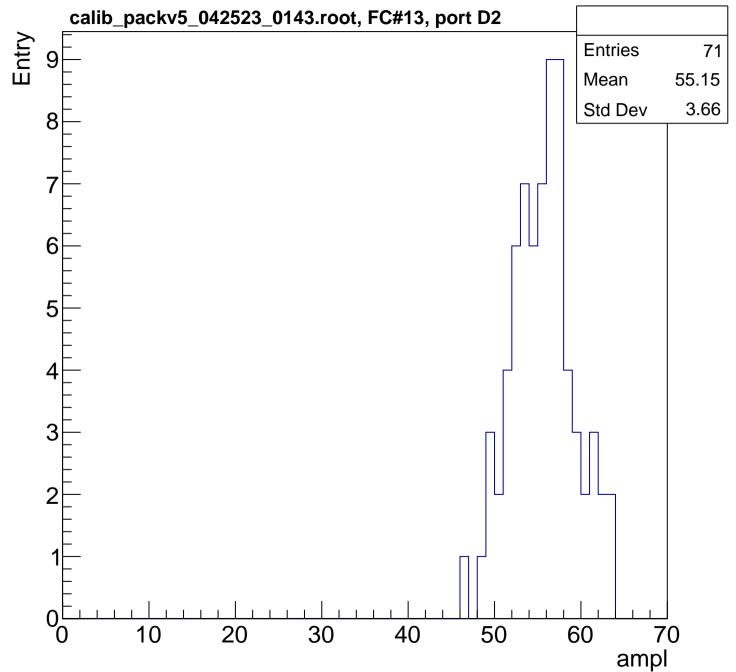


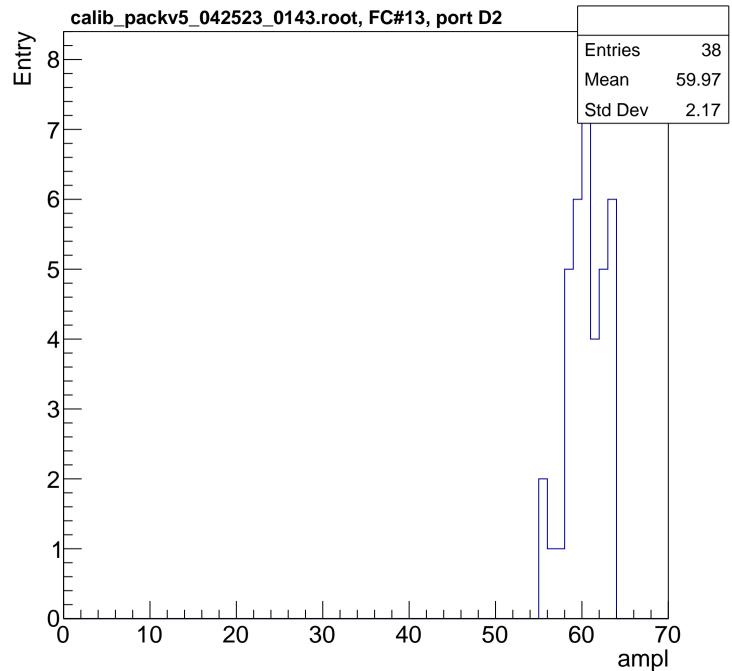


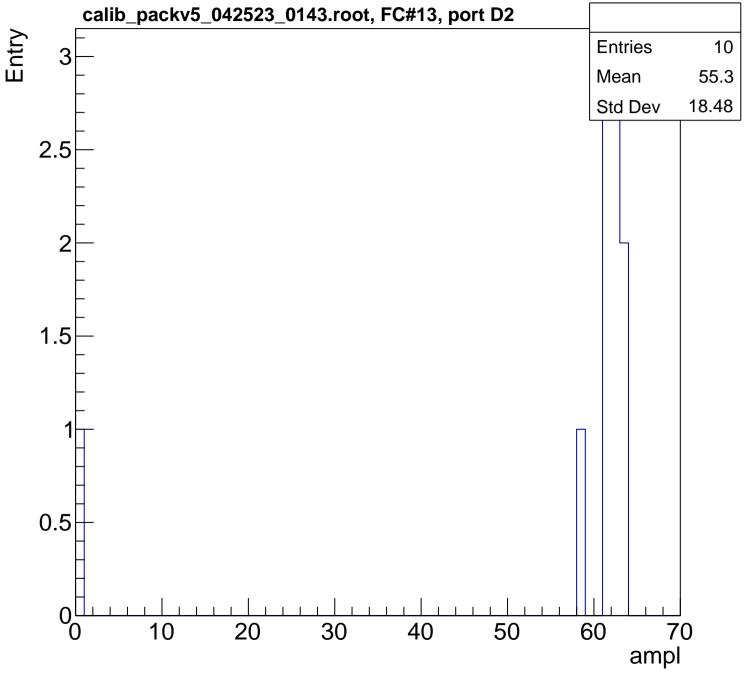




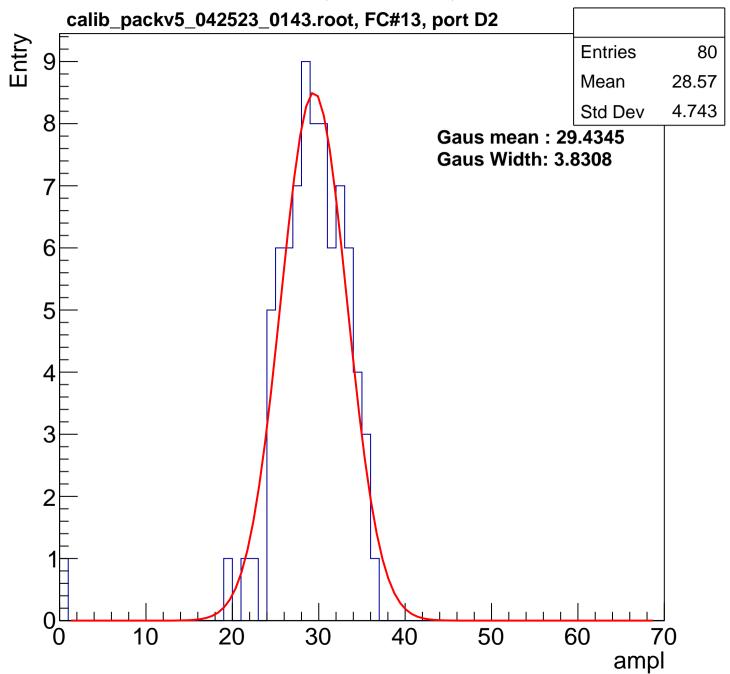


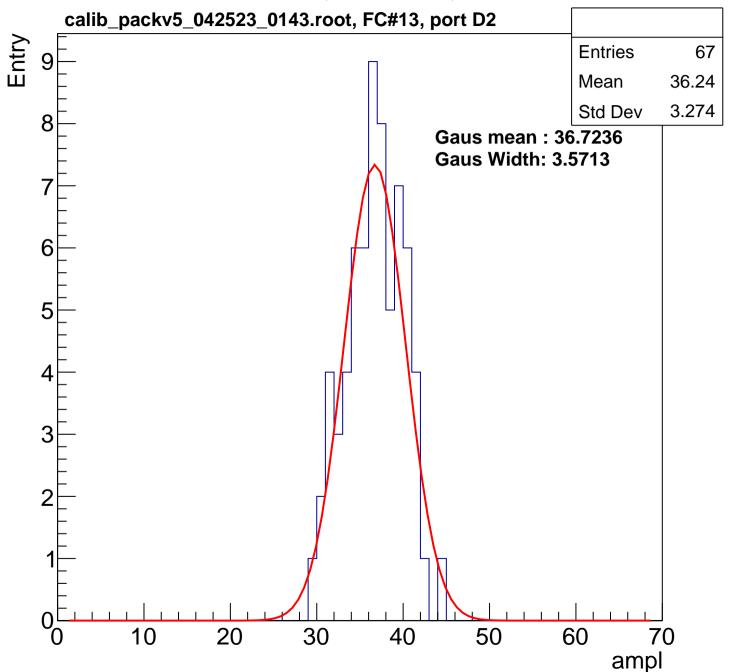


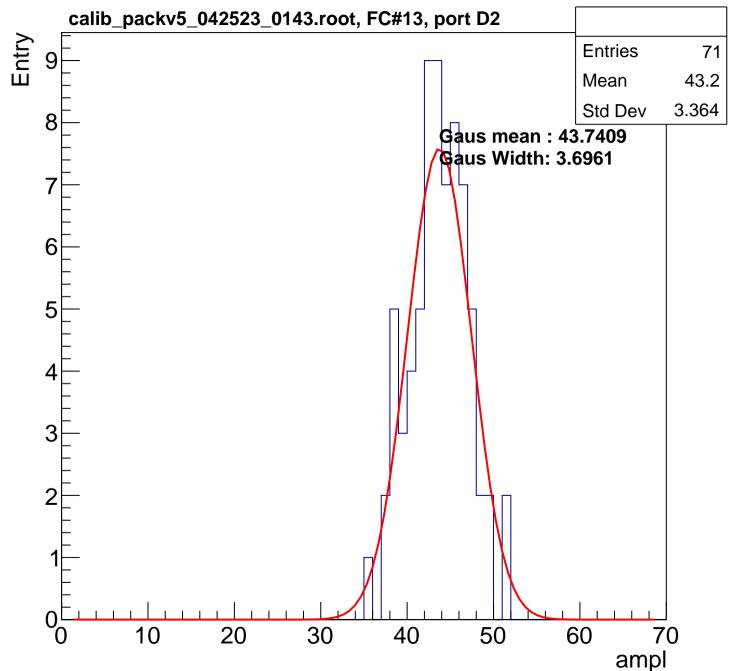


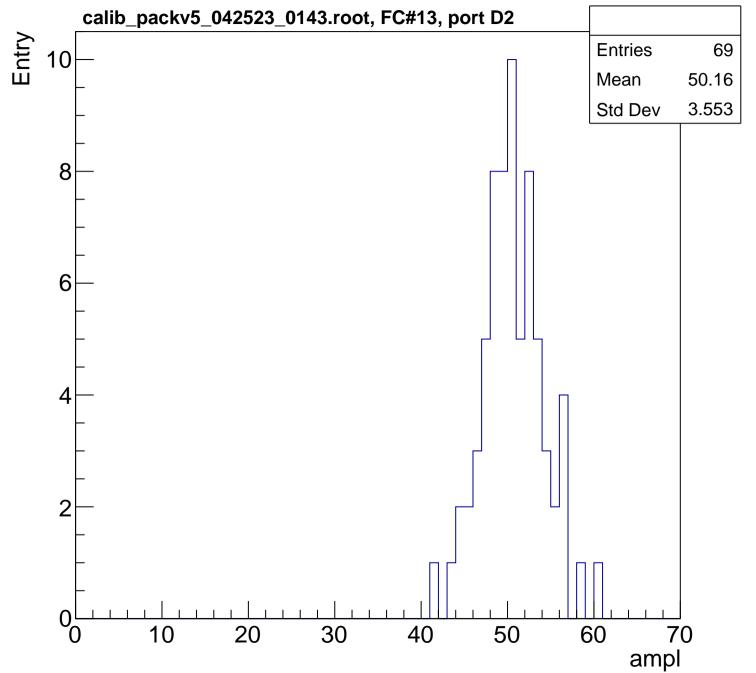


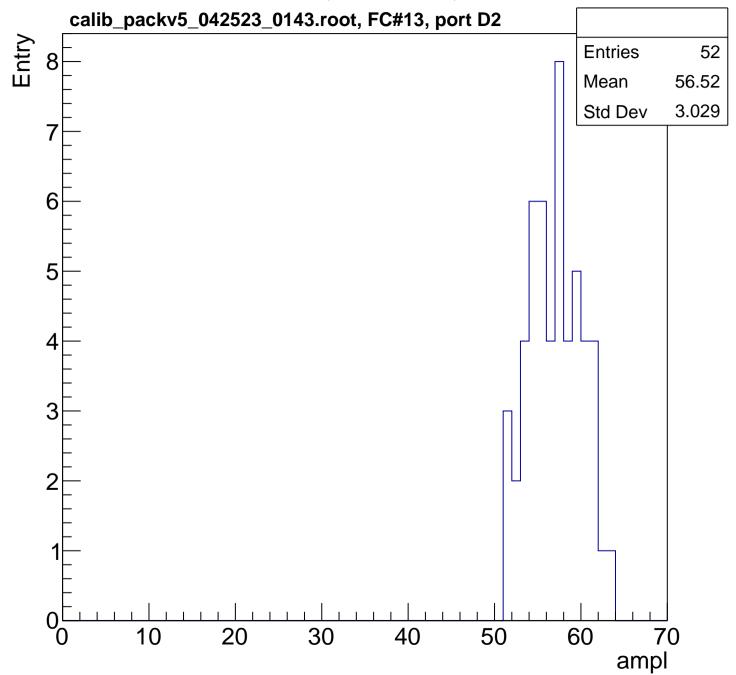


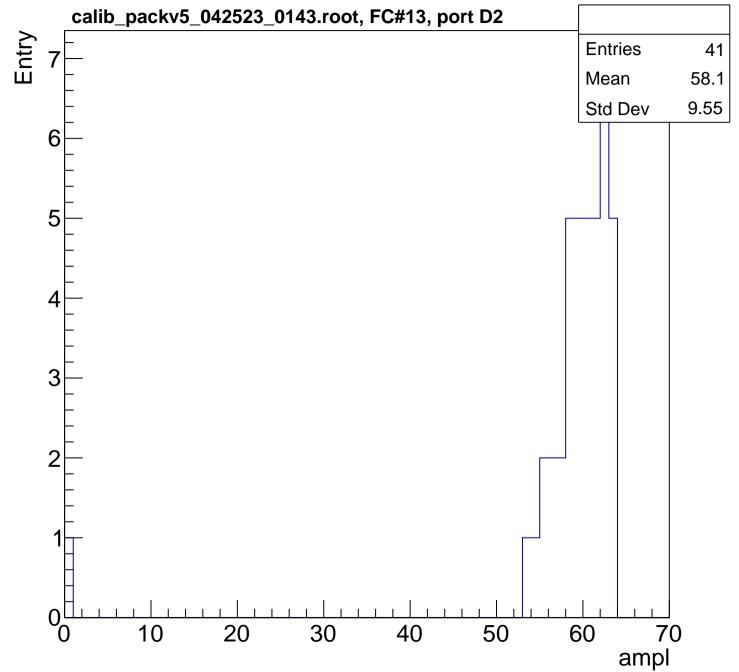


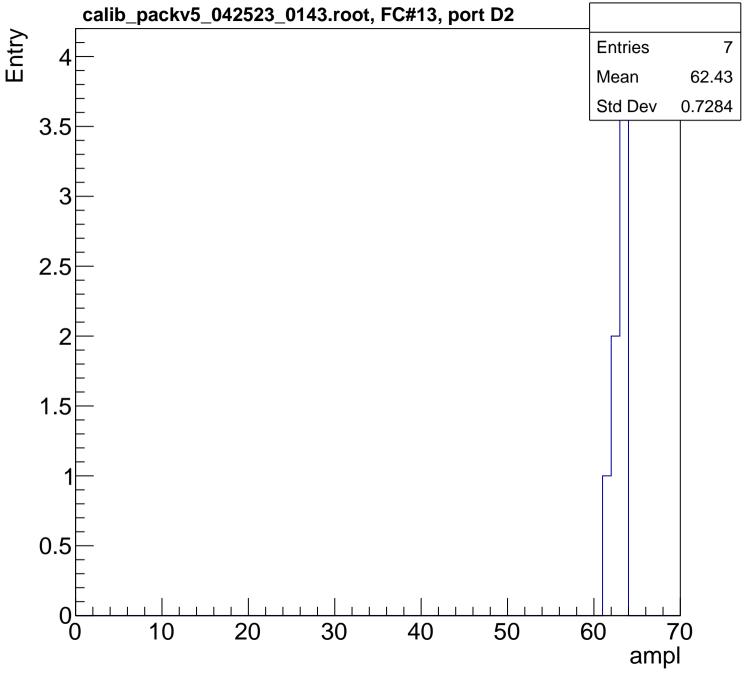




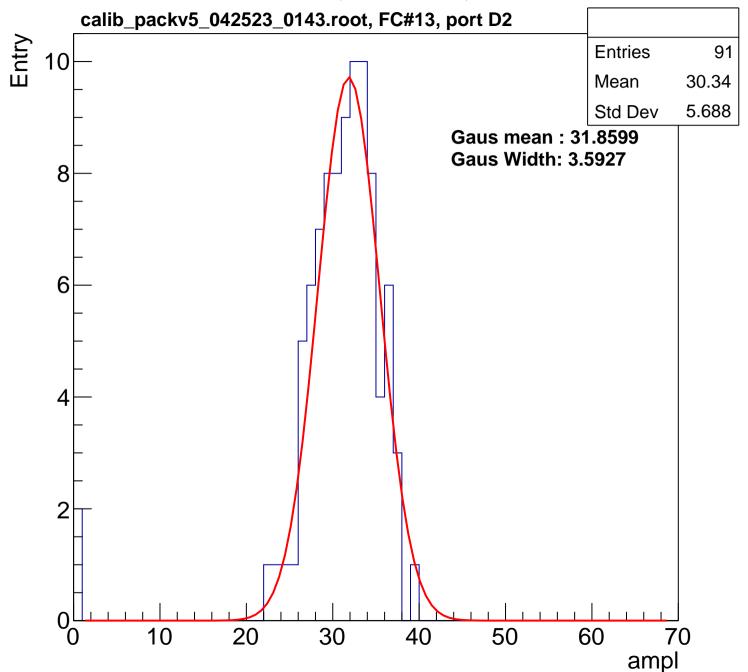


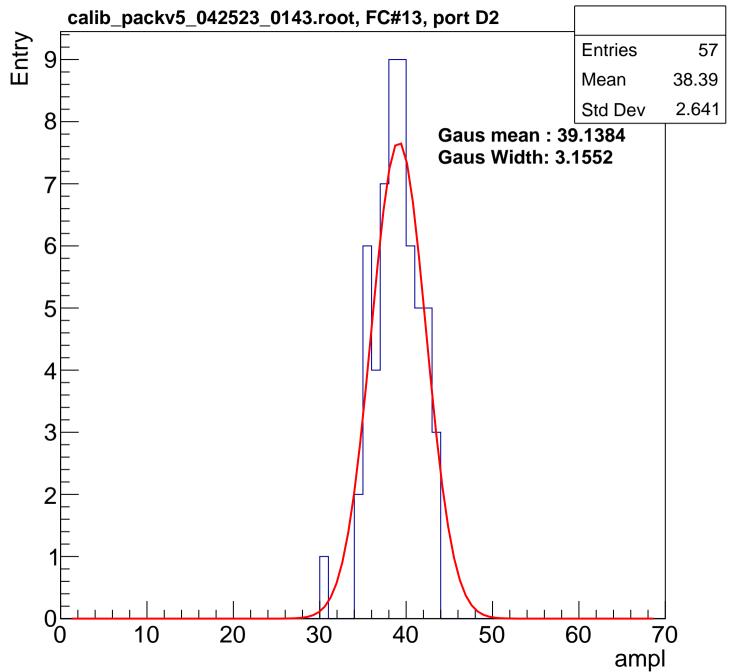


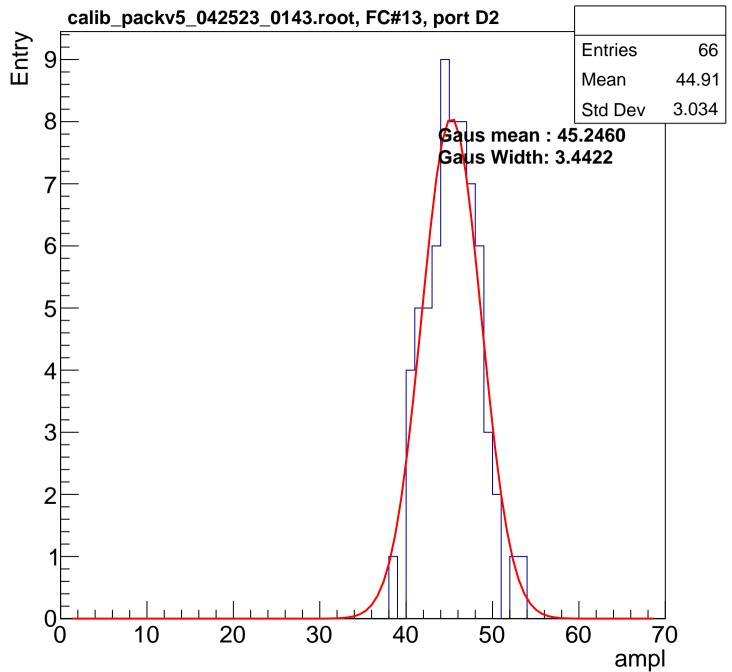


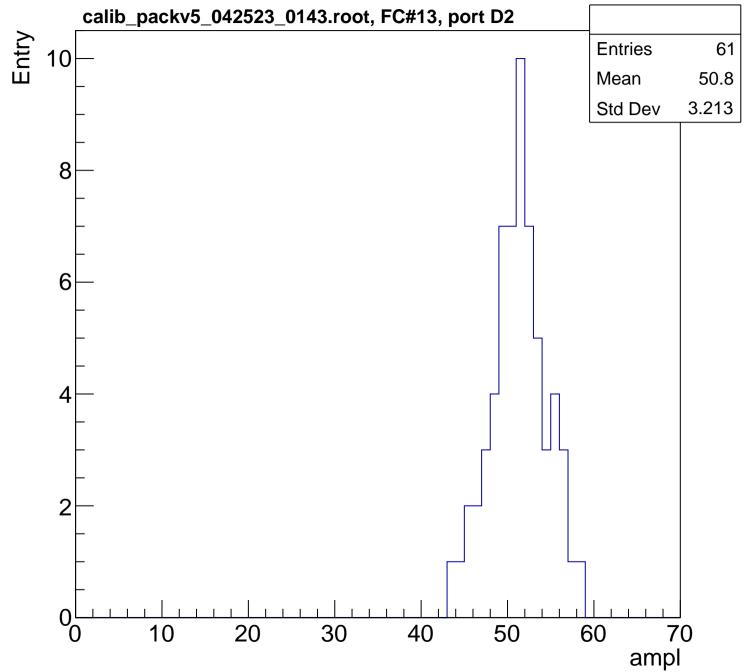


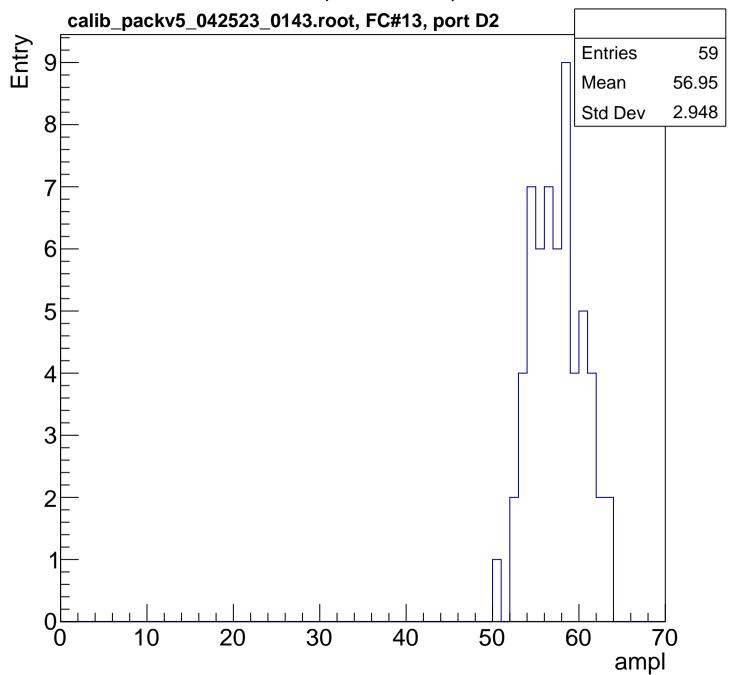
B1L003S, U2-ch7, adc7 calib_packv5_042523_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

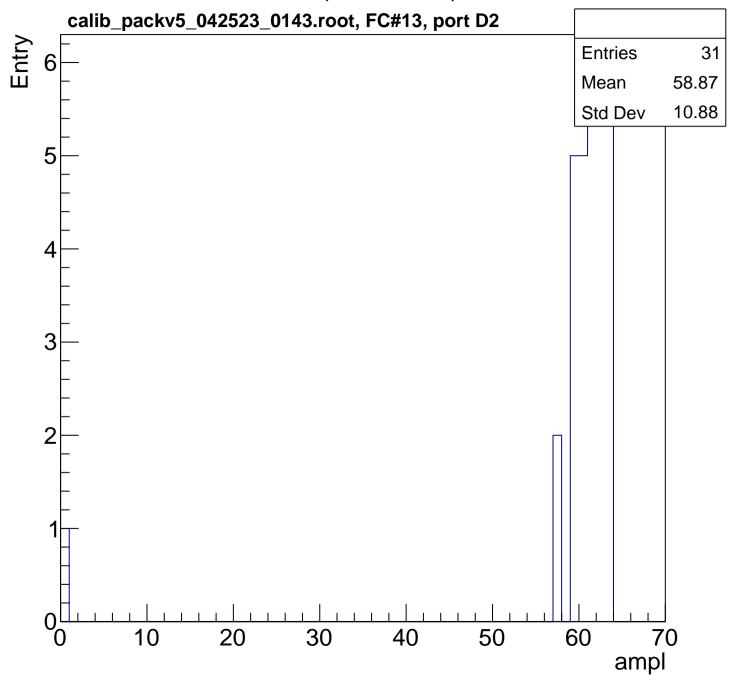


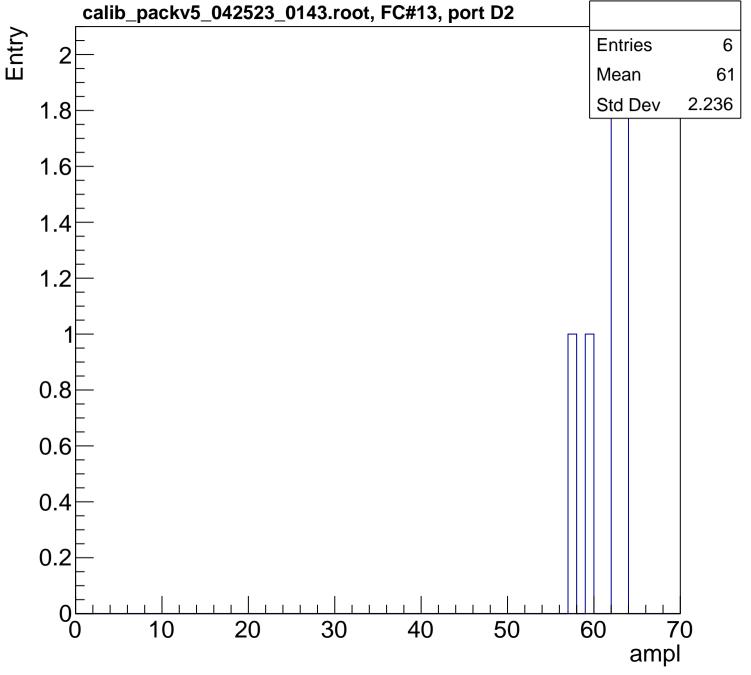


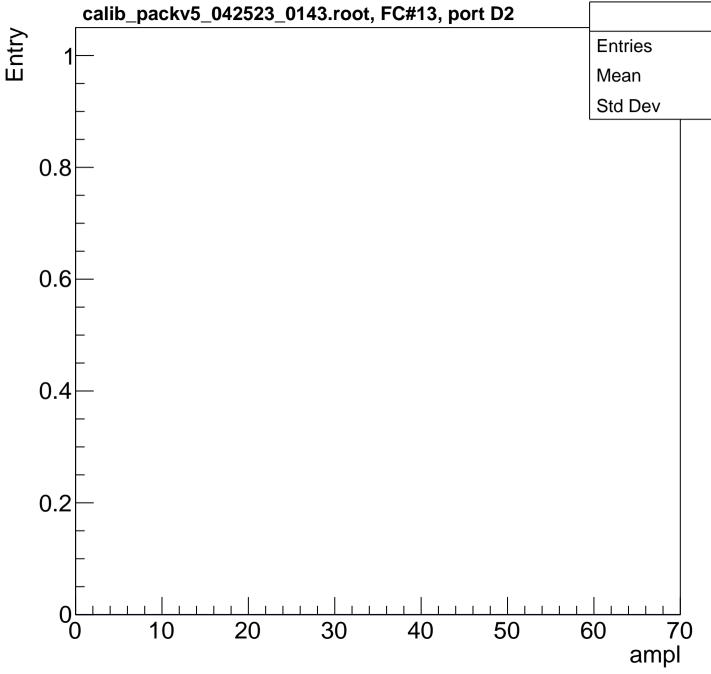


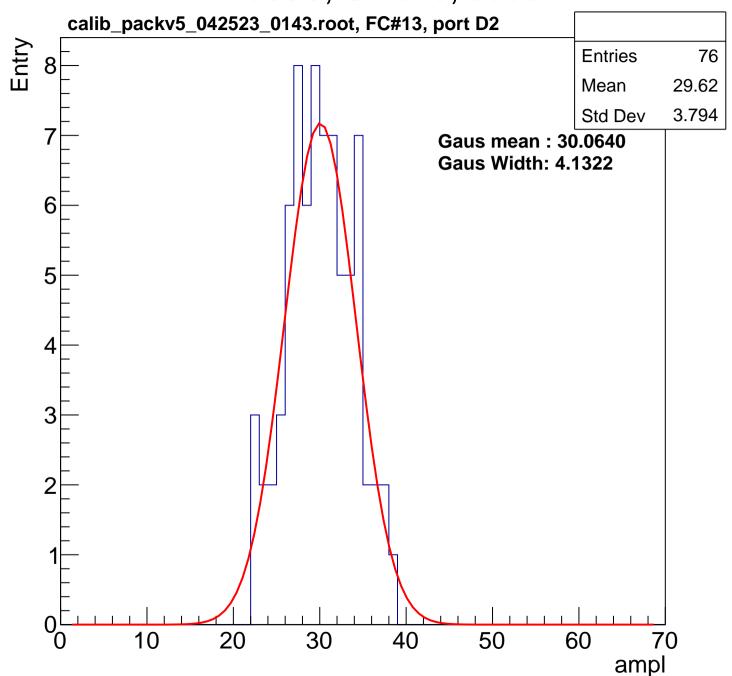


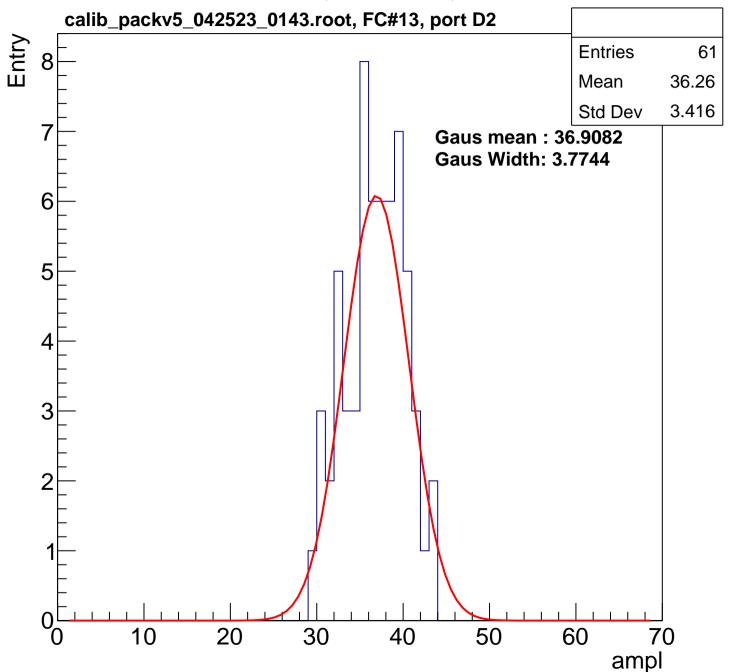


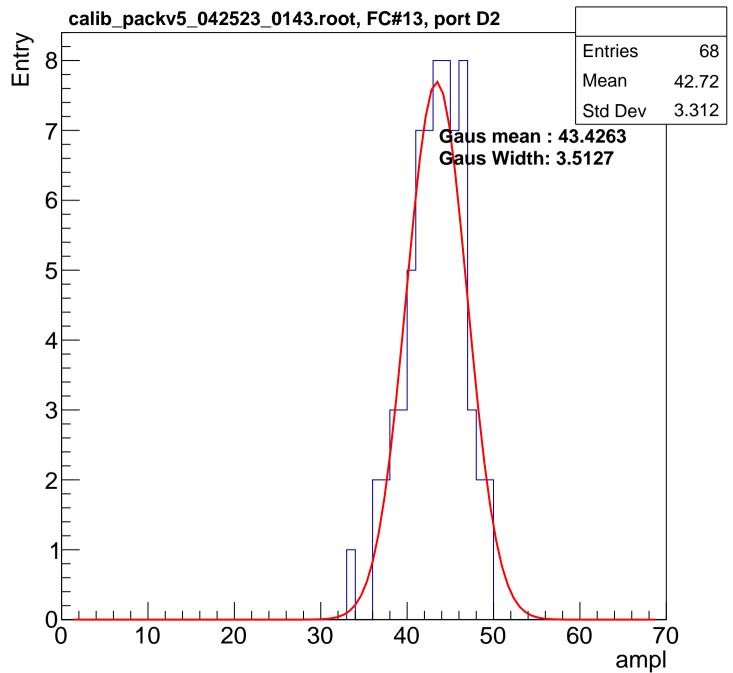


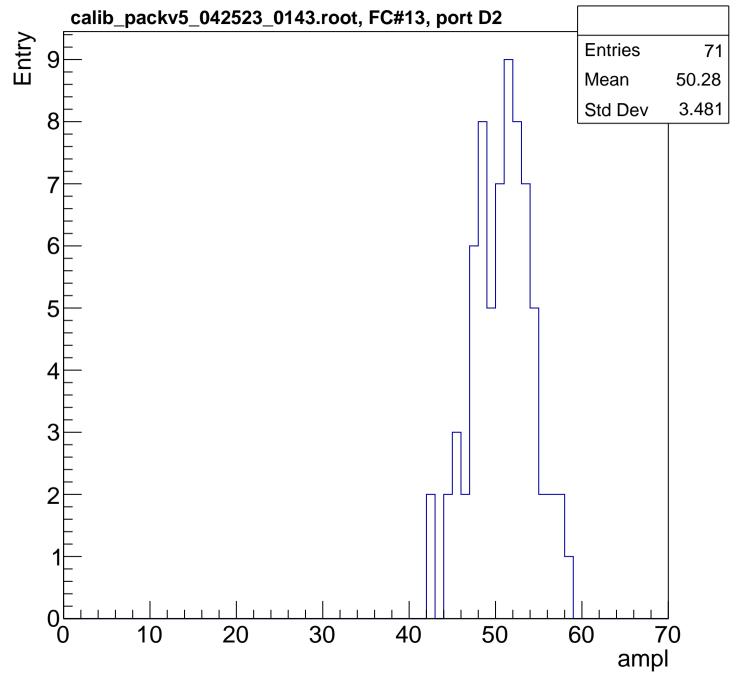


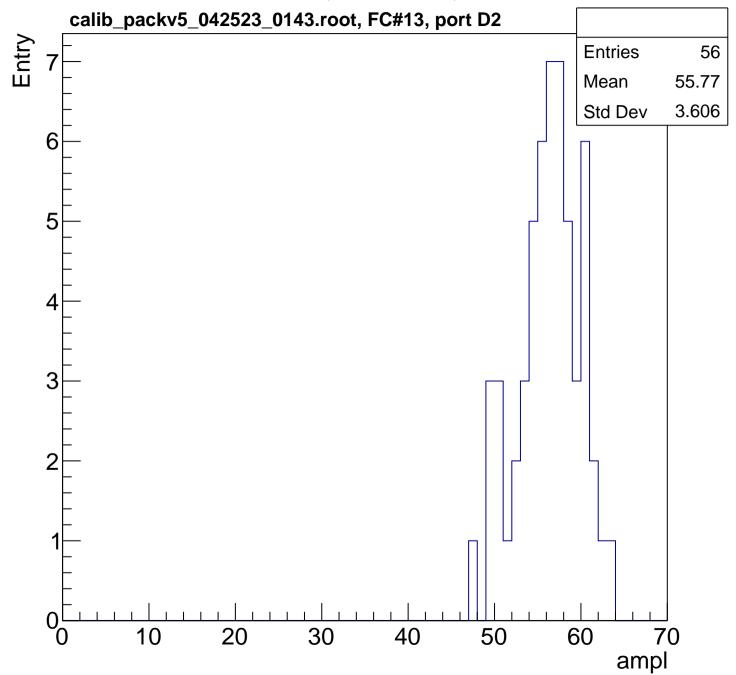


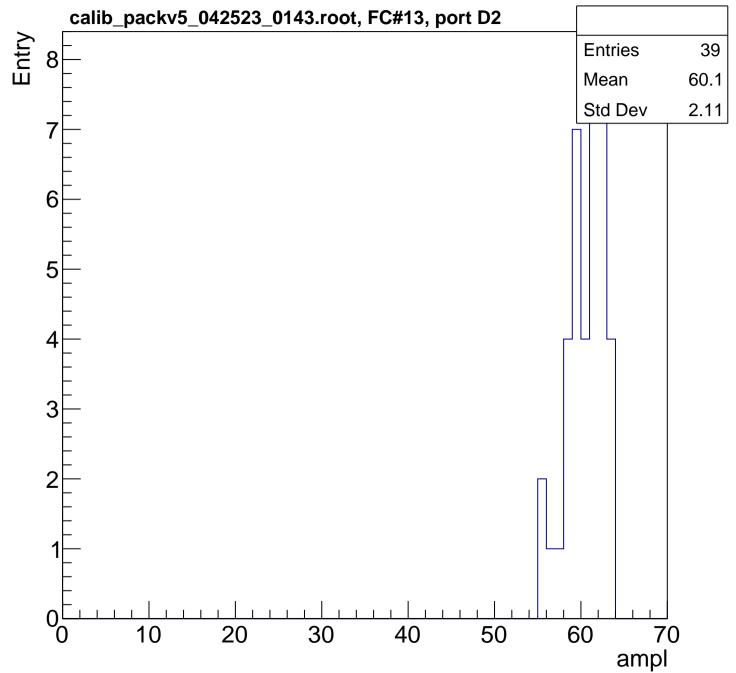


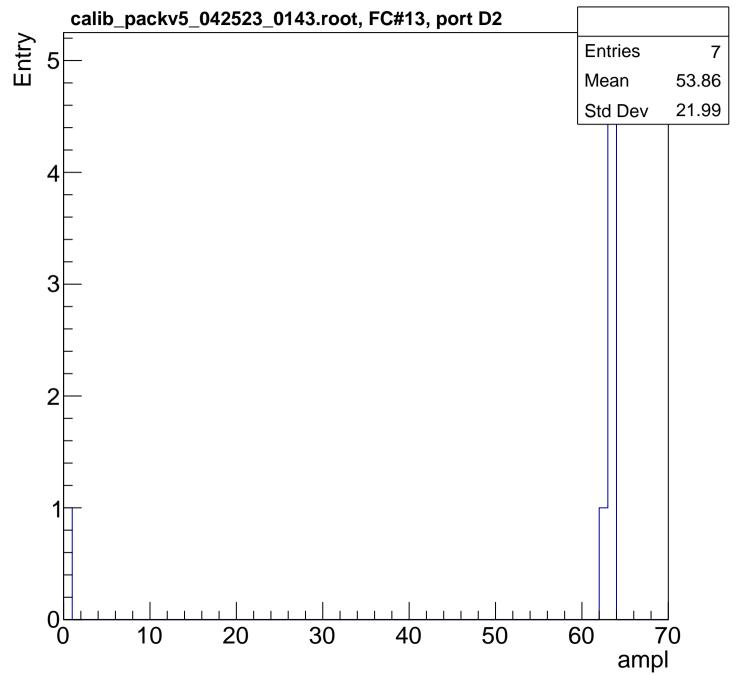




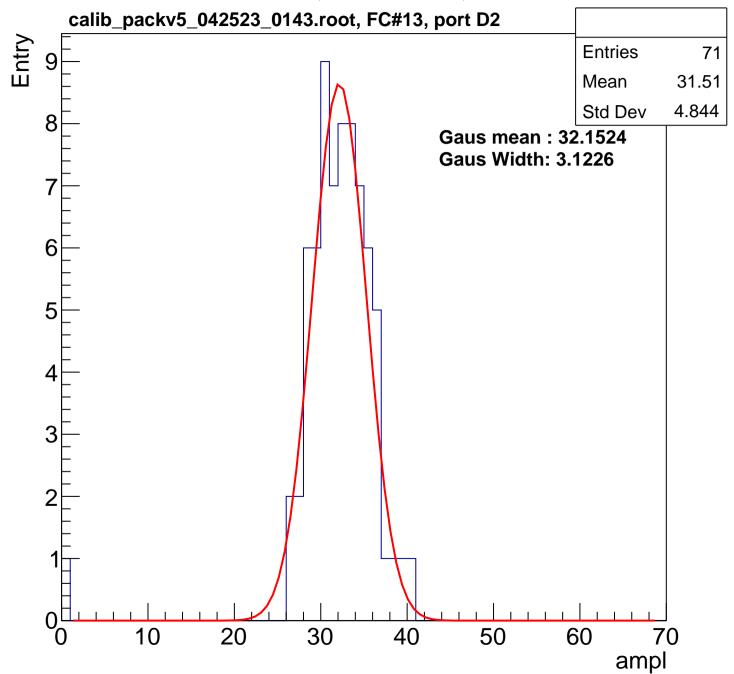


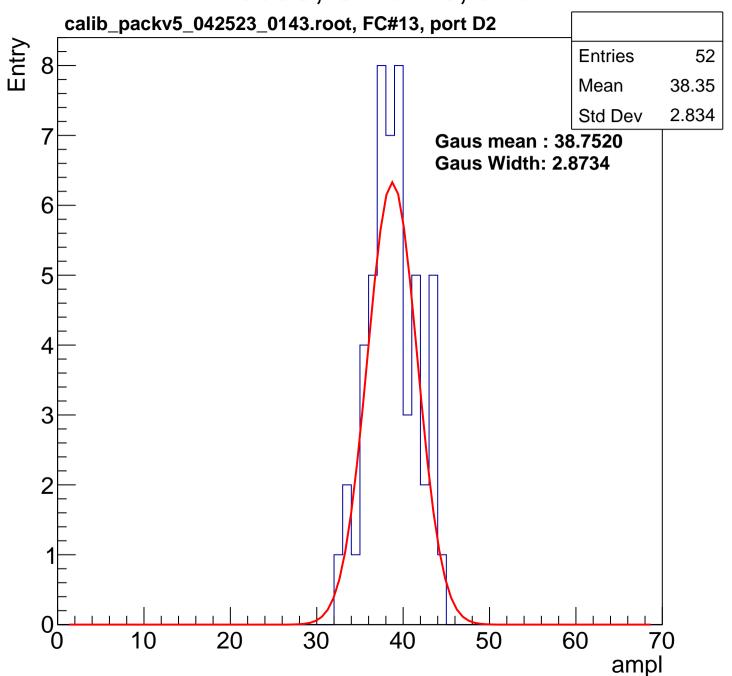


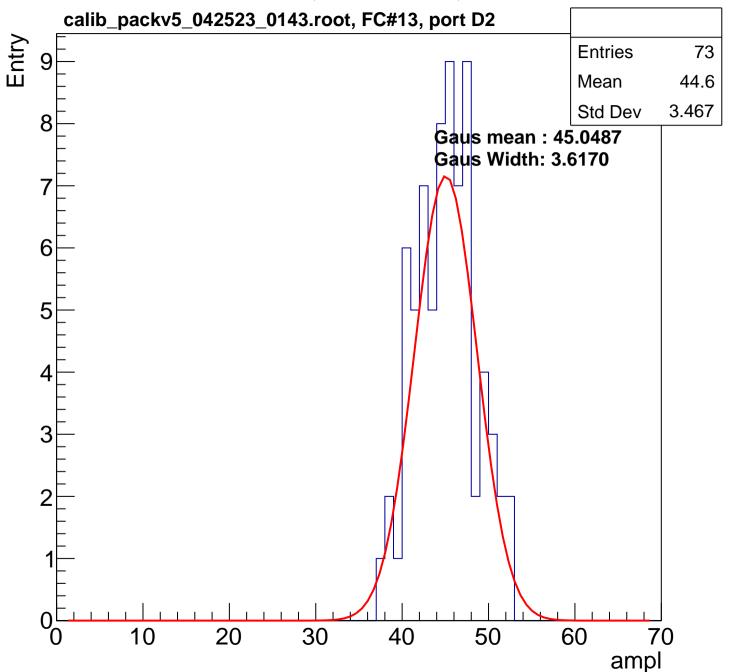


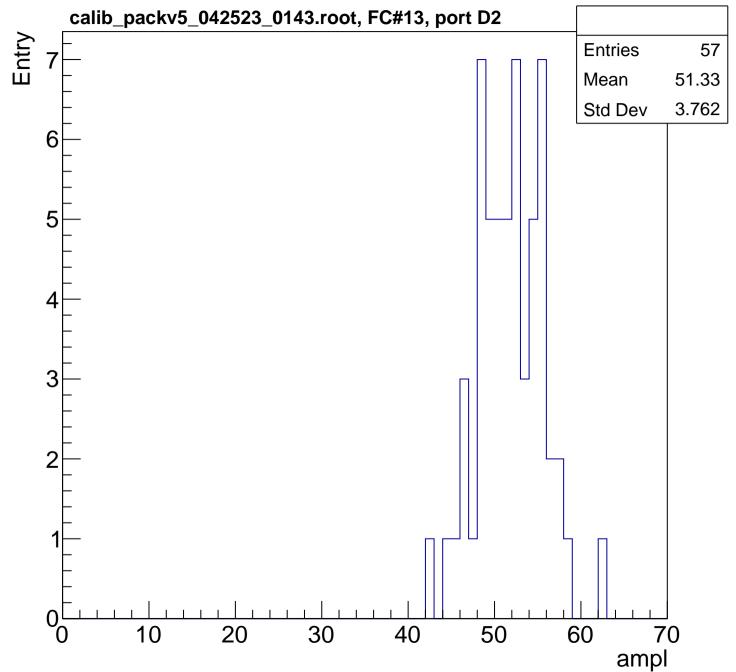


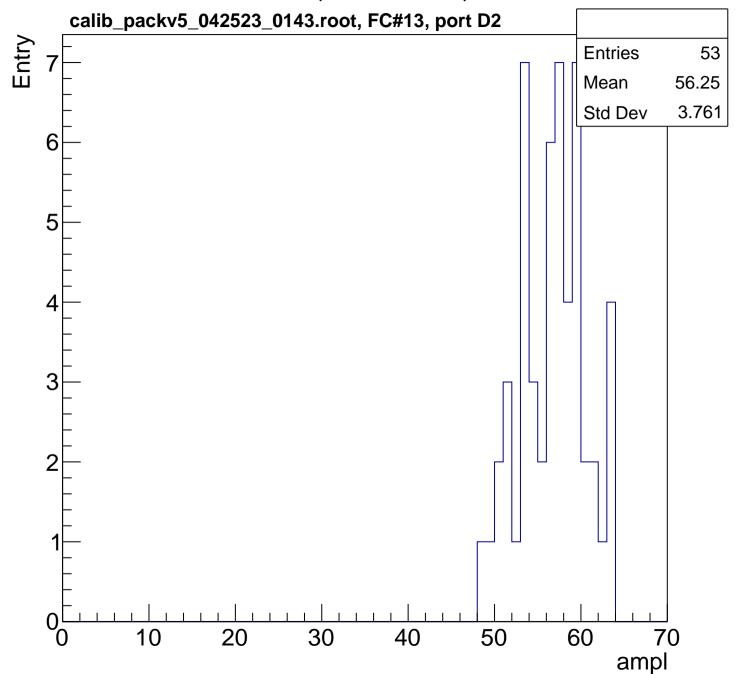
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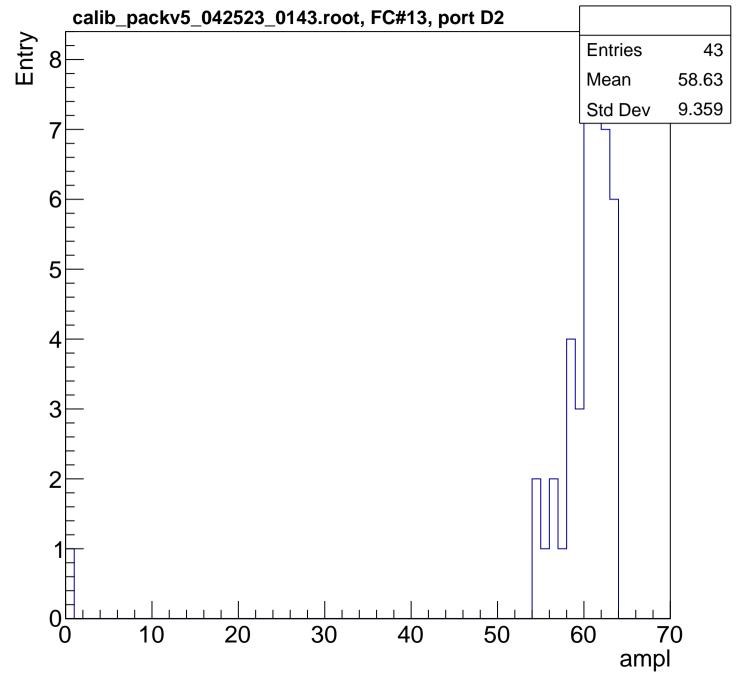


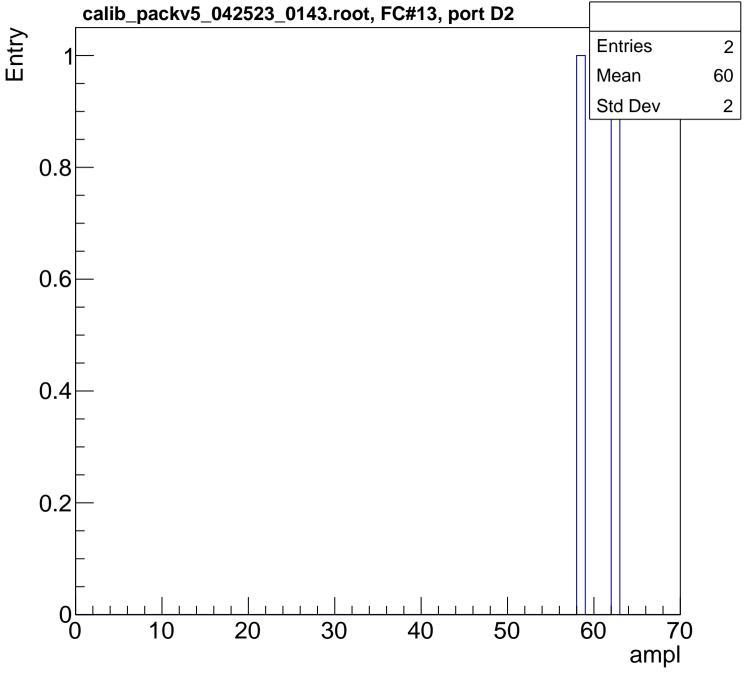




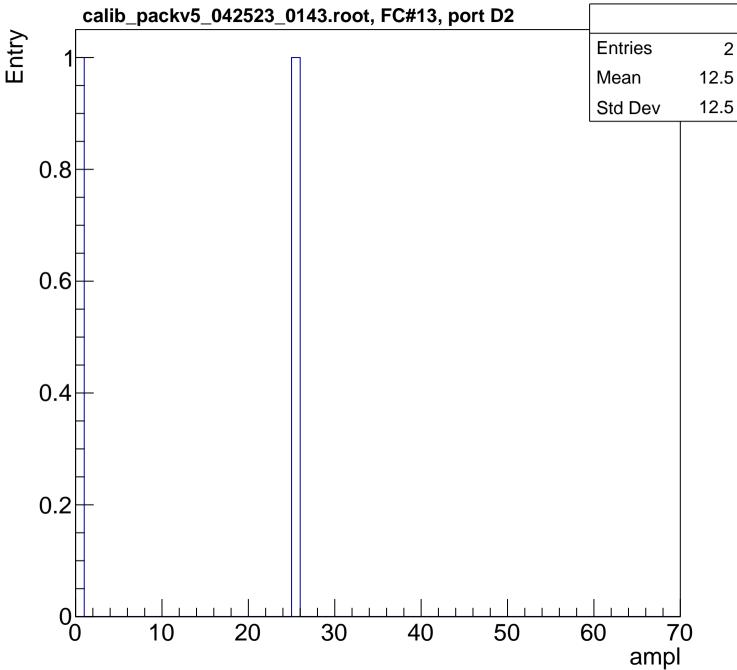


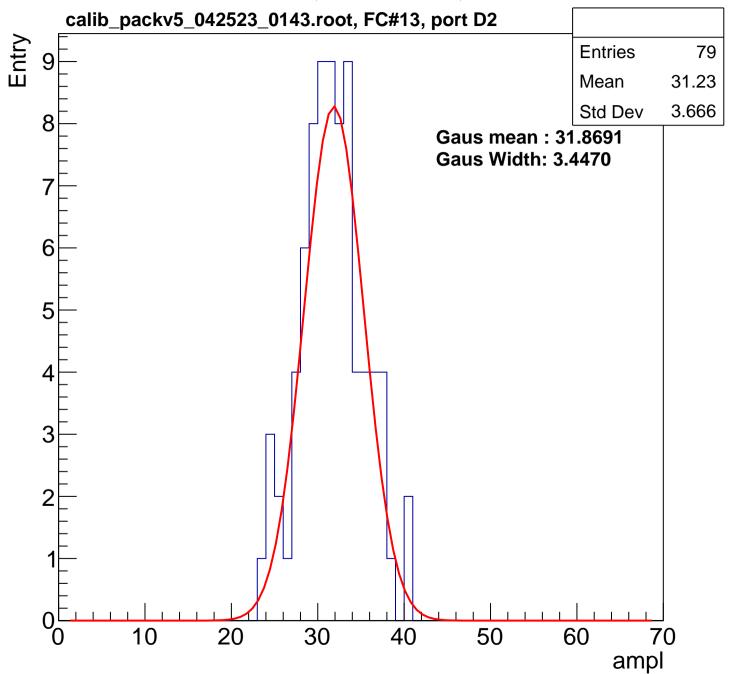


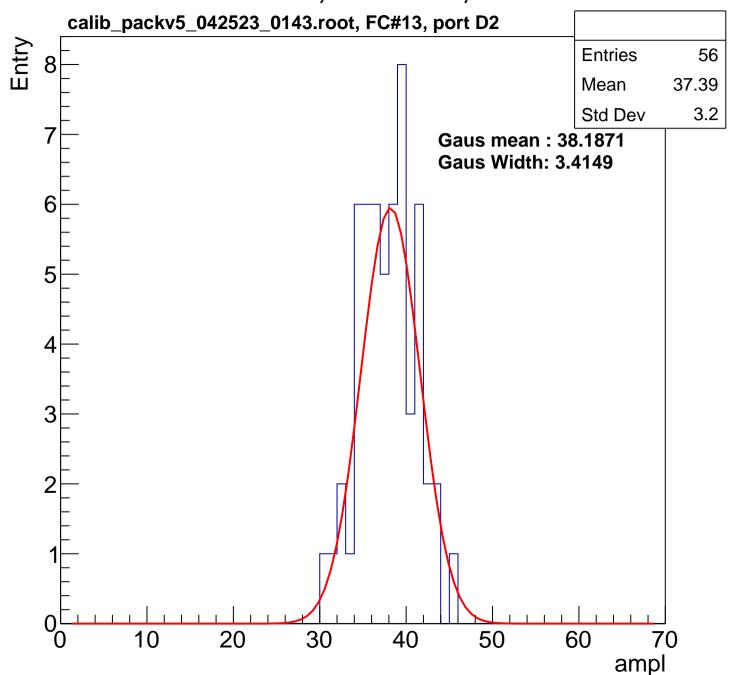


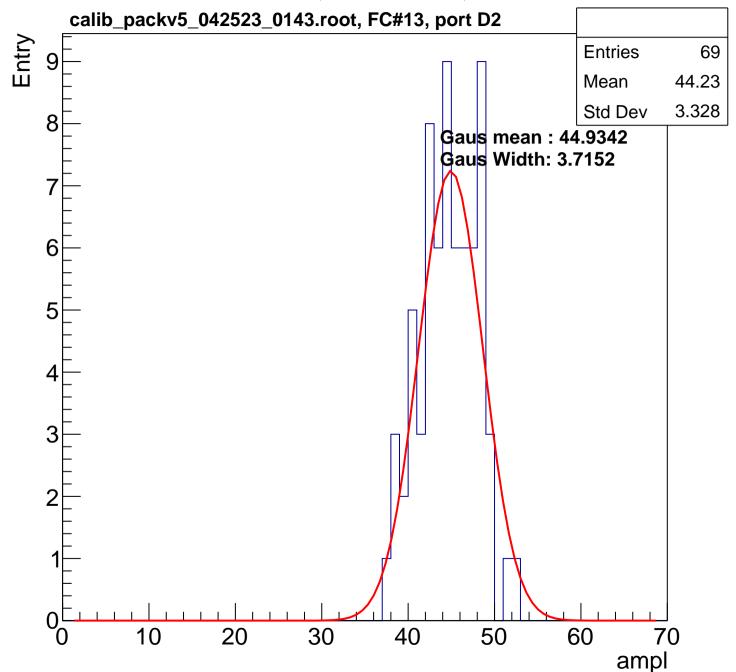


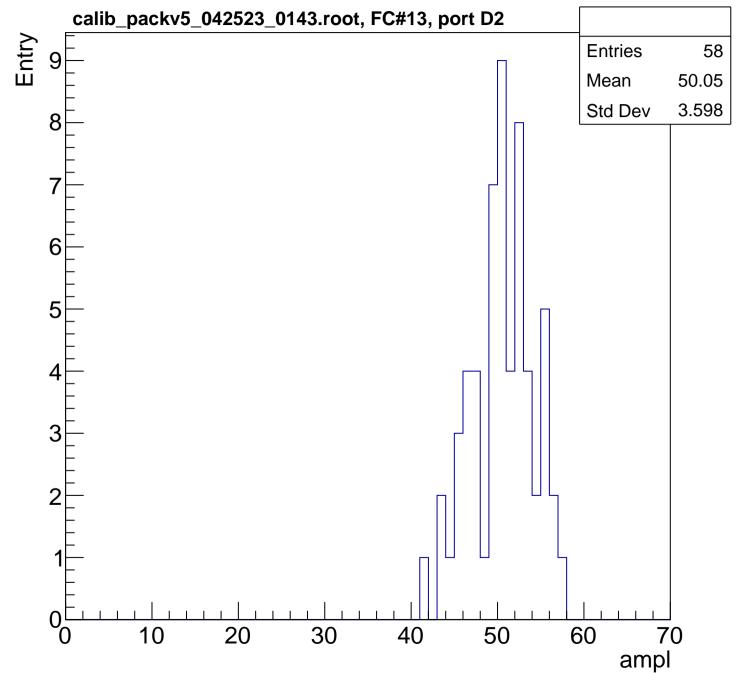
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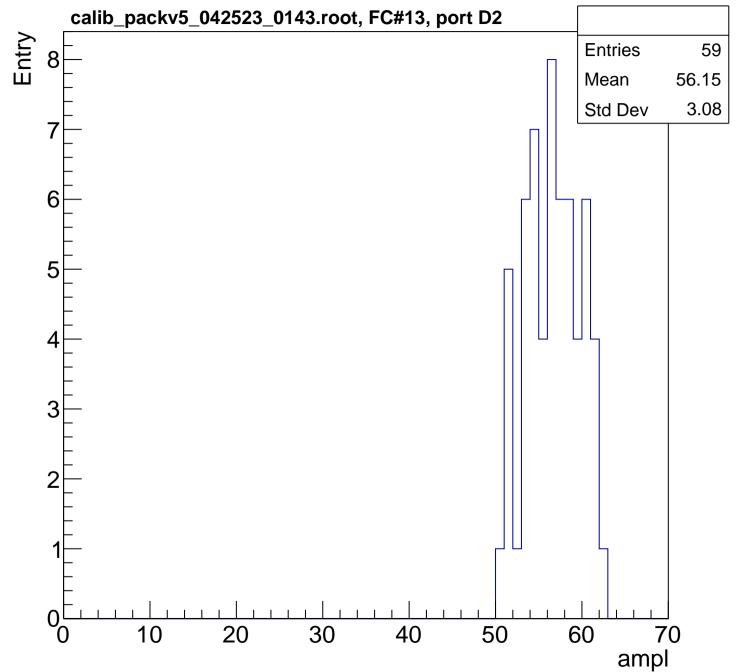


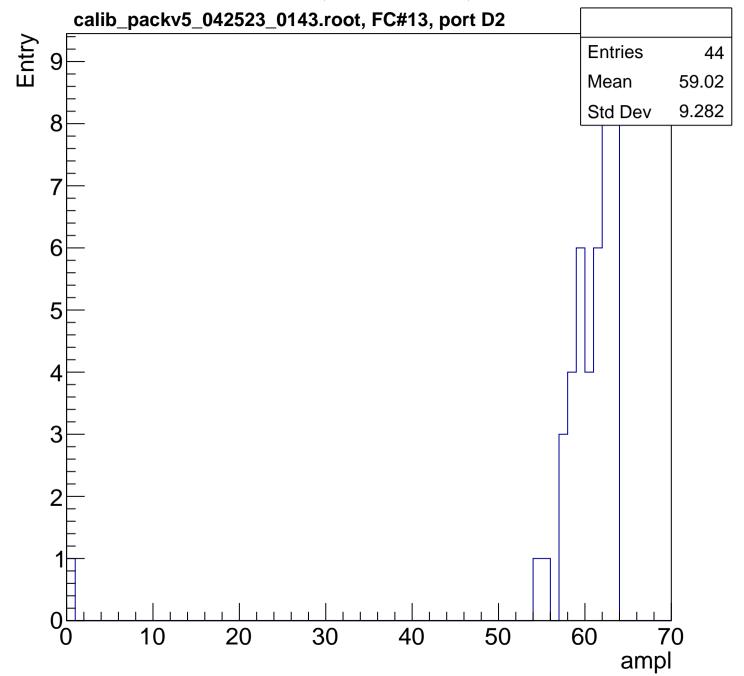


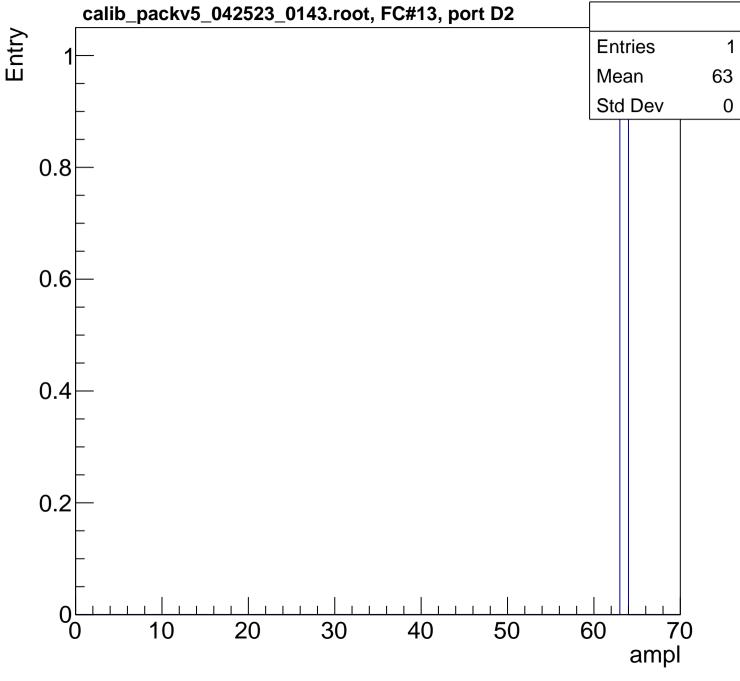


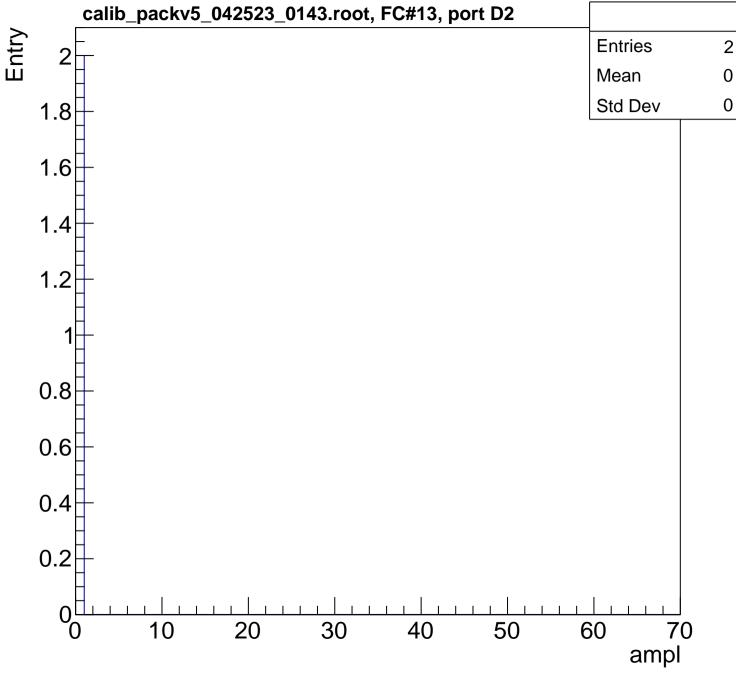


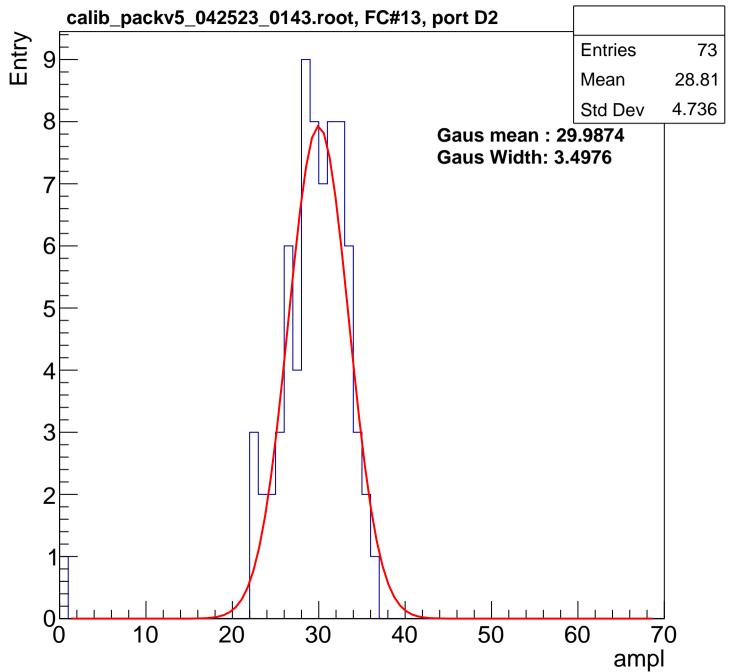


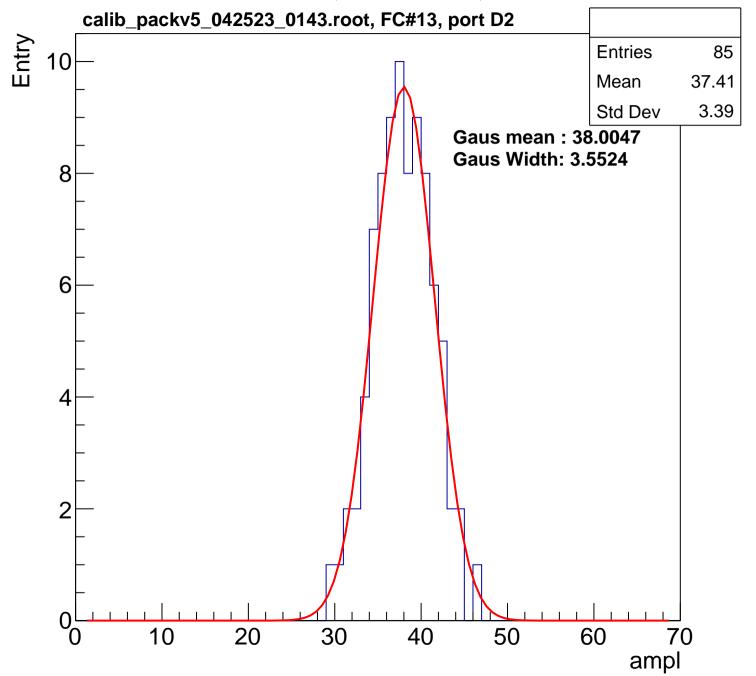


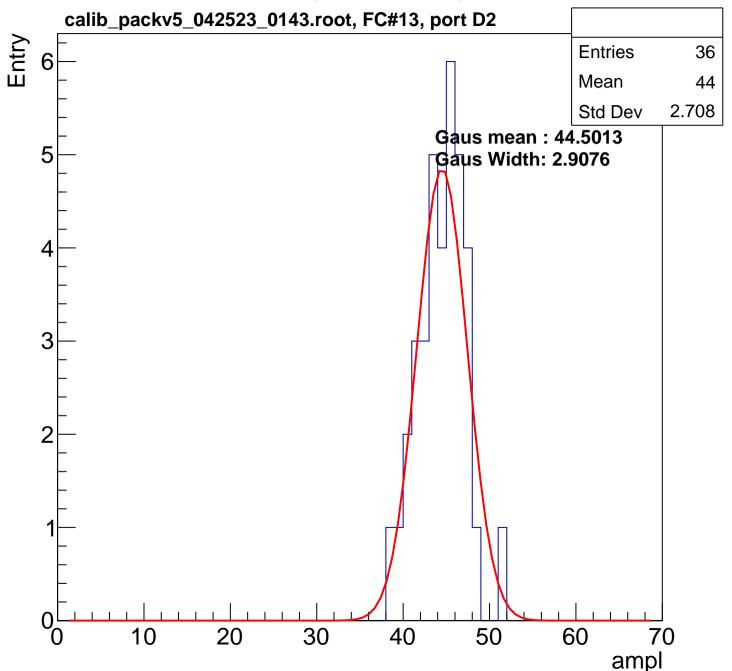


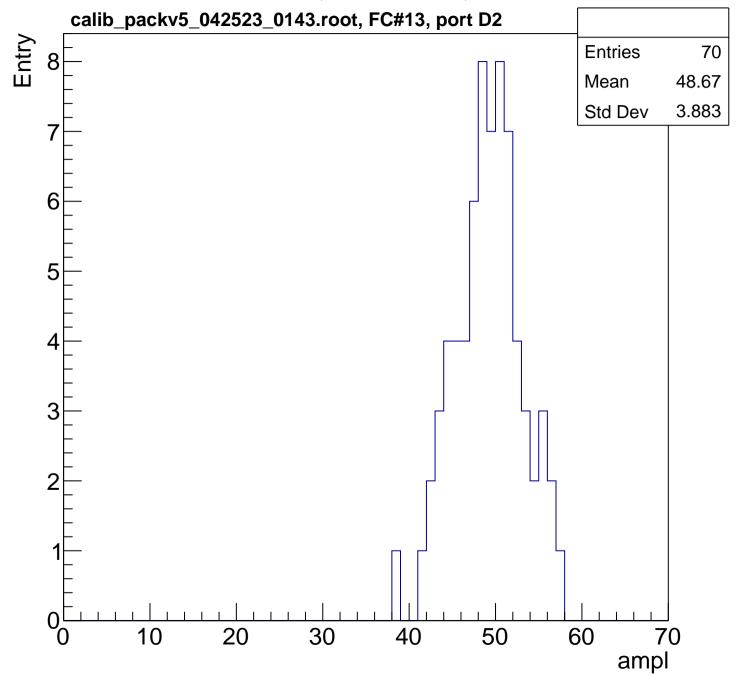


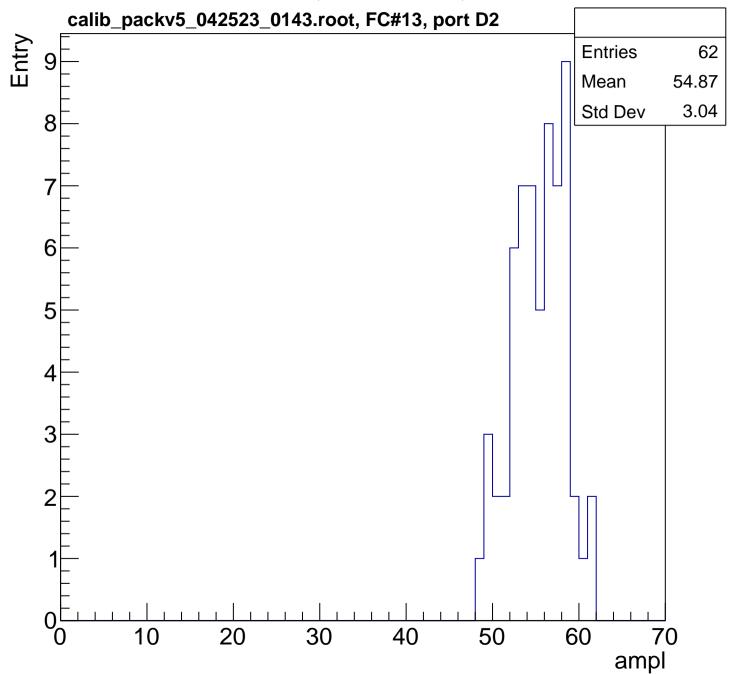


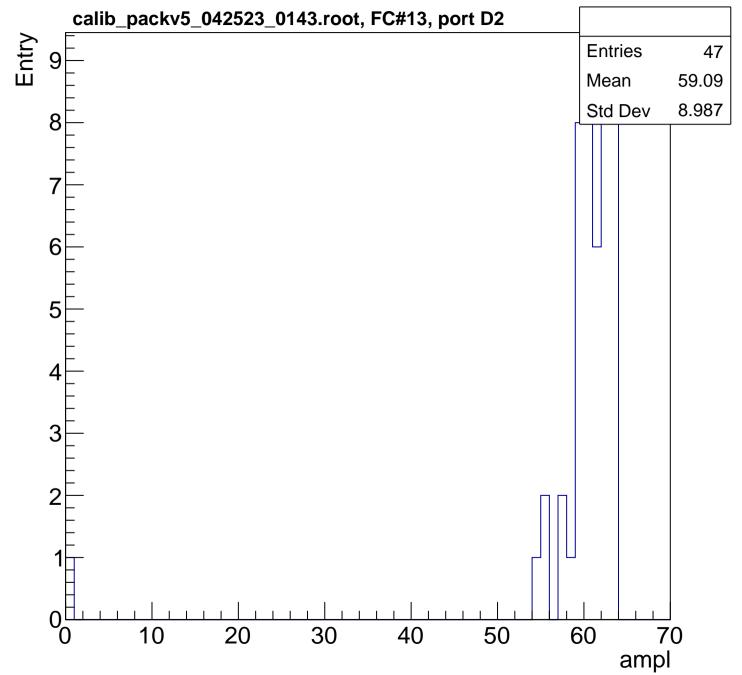


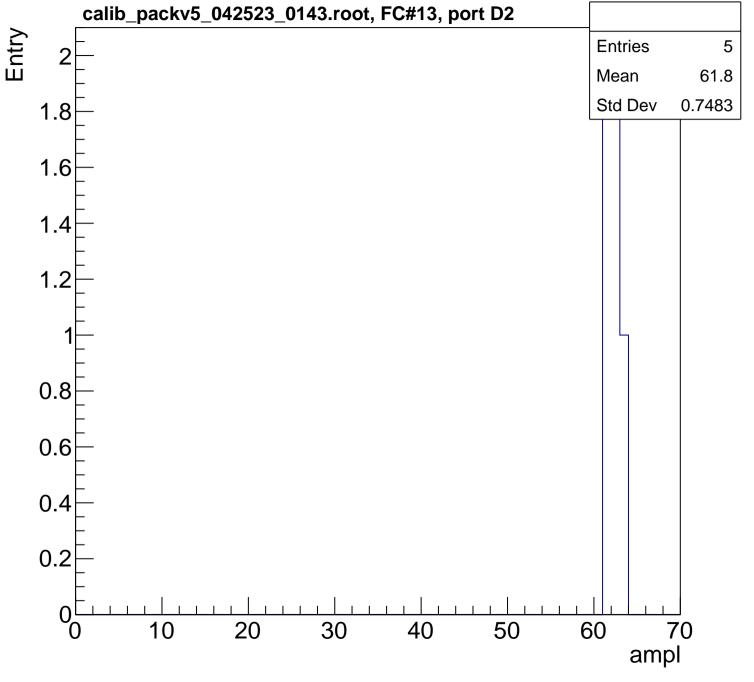




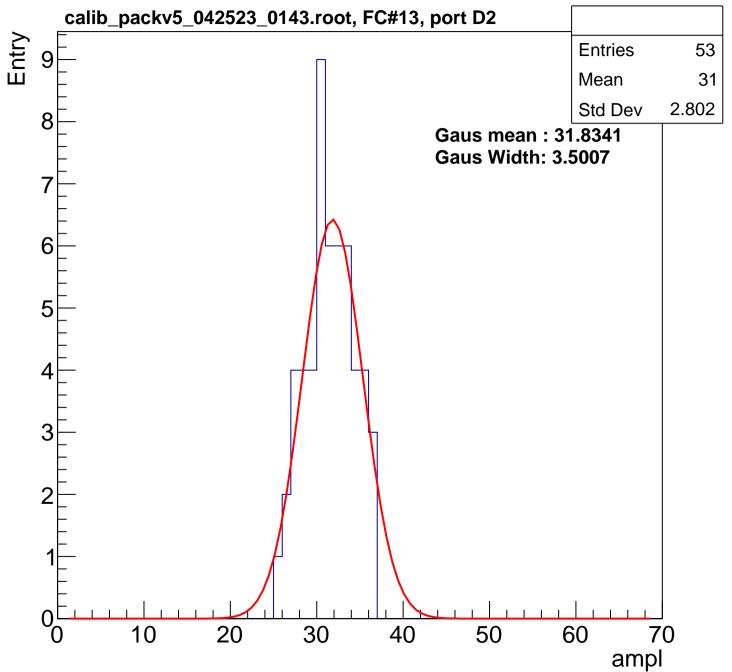


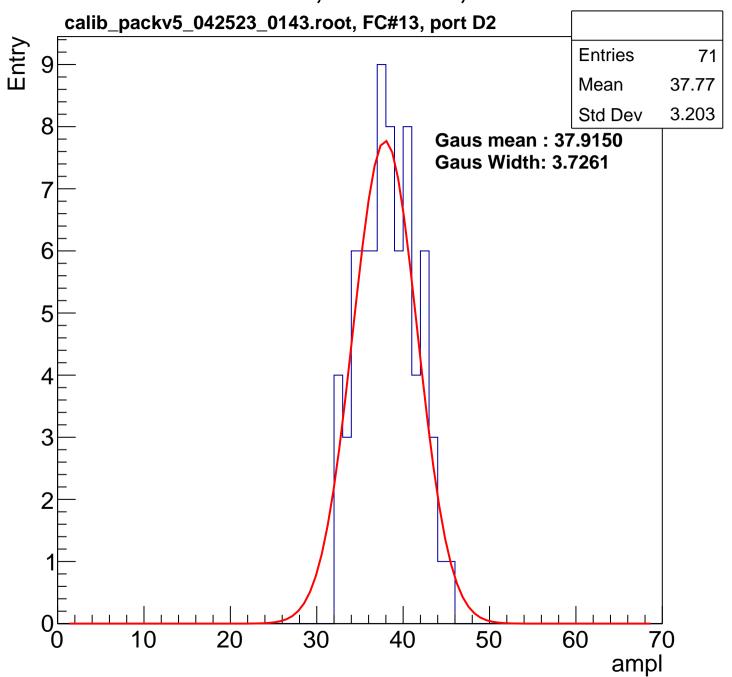


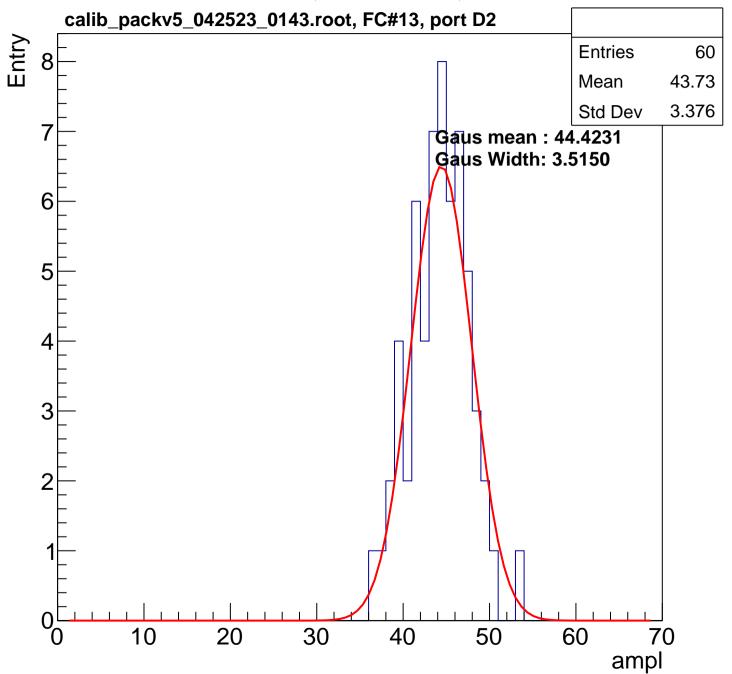


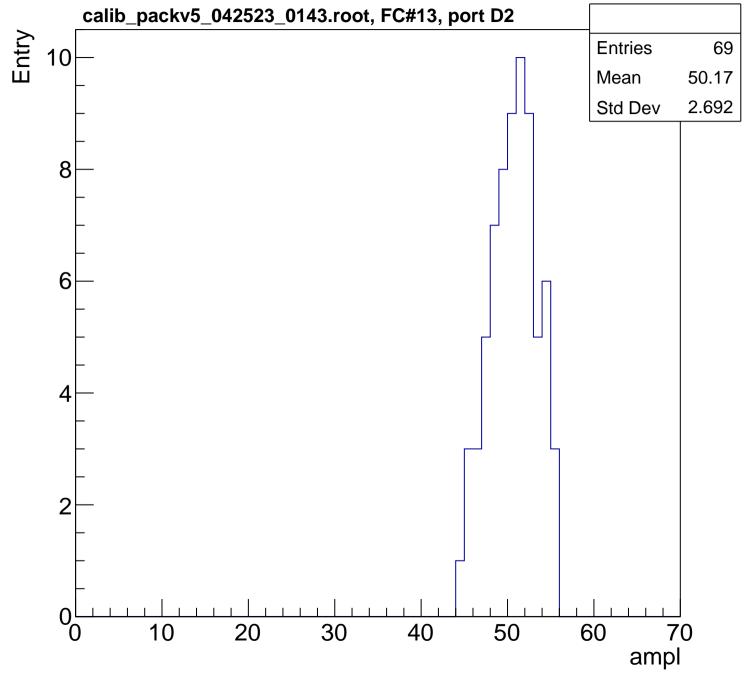


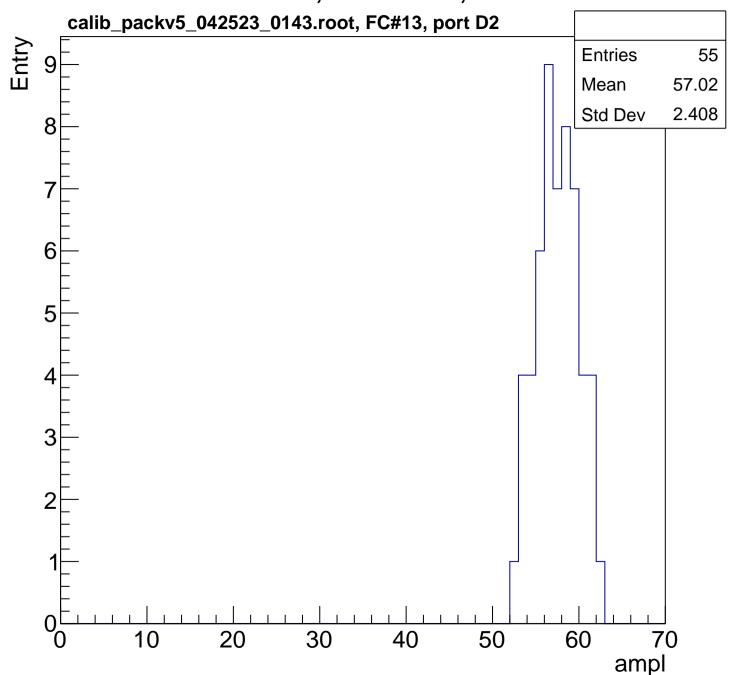


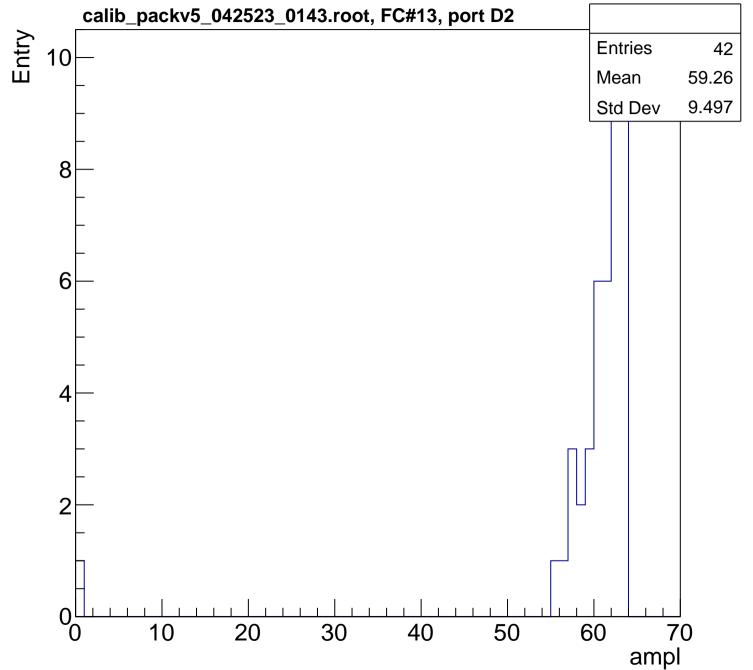


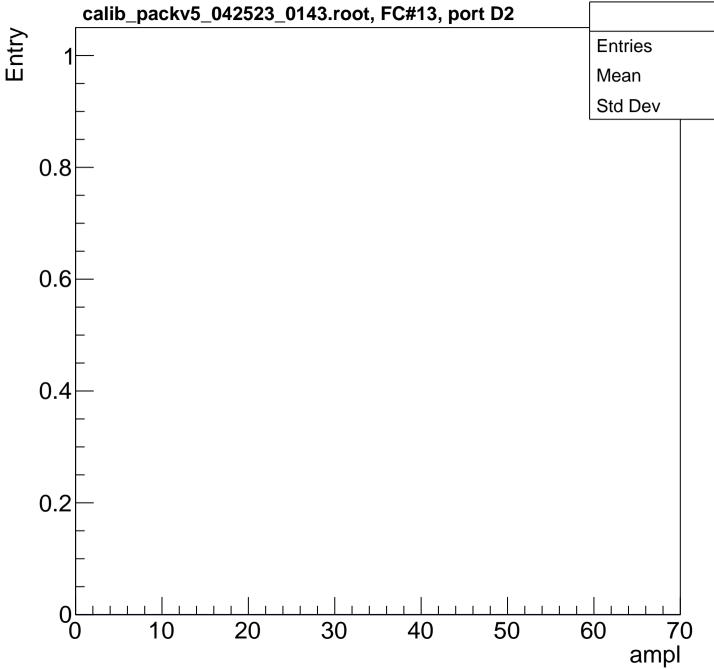


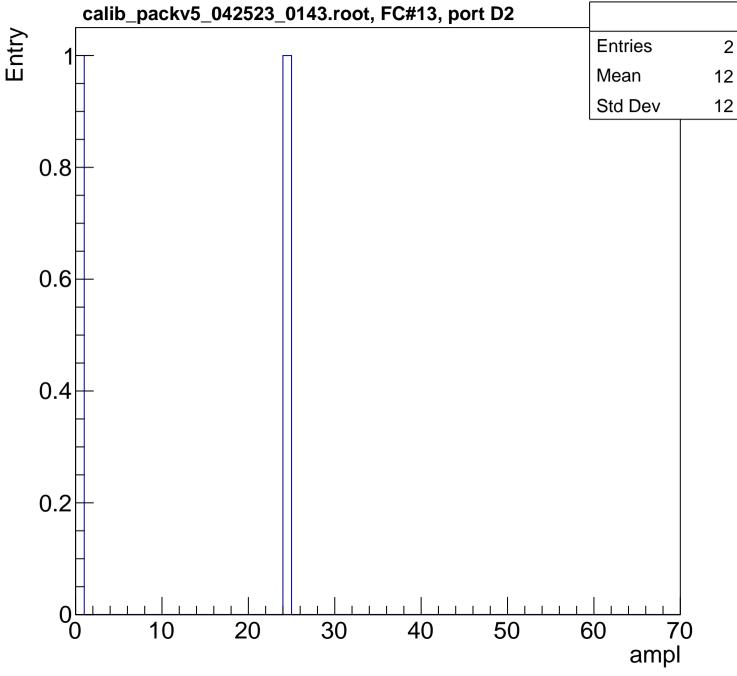


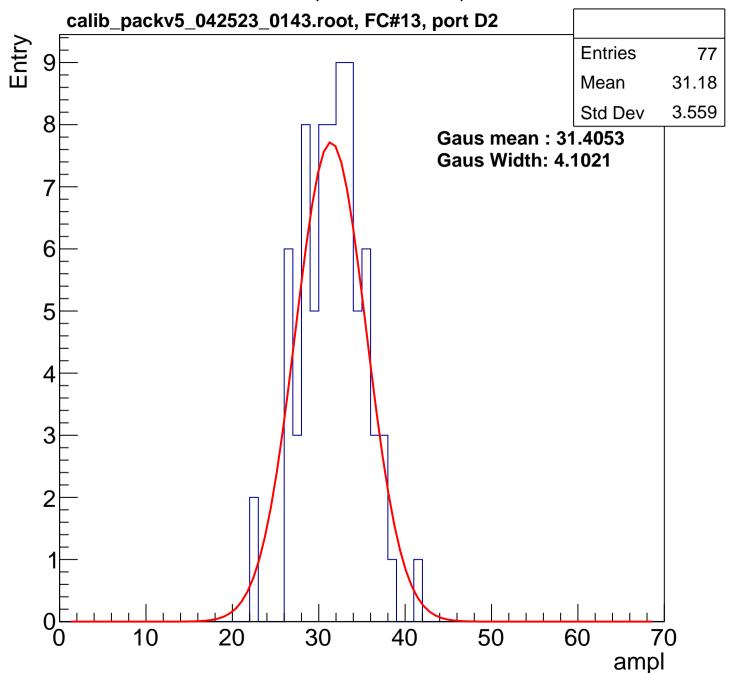


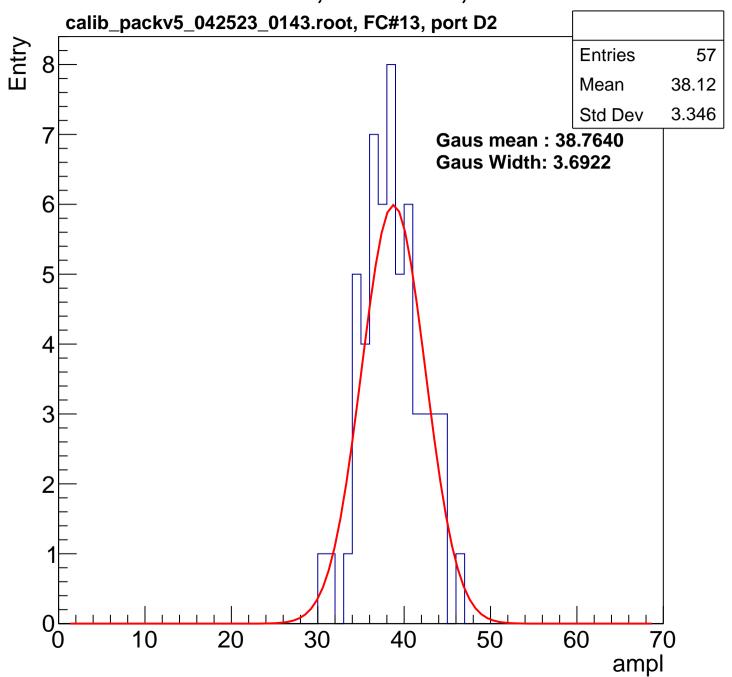


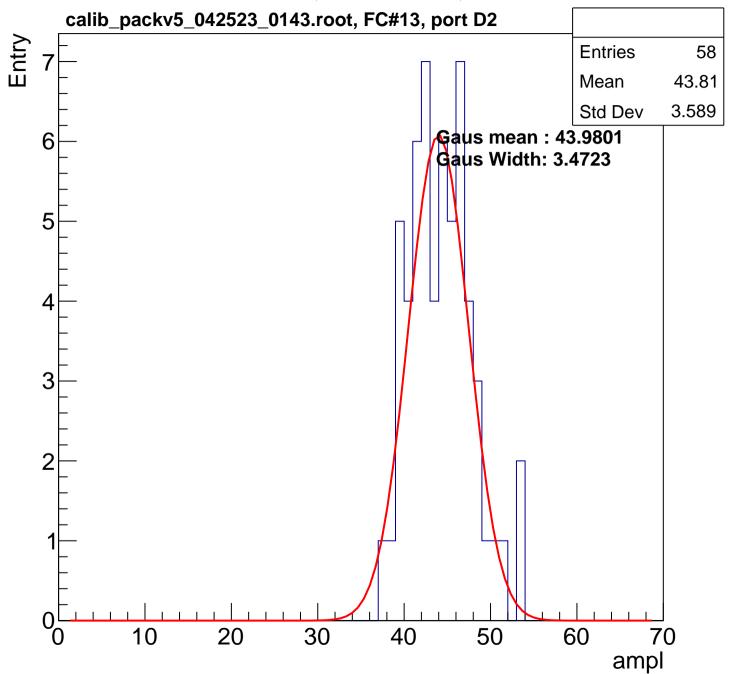


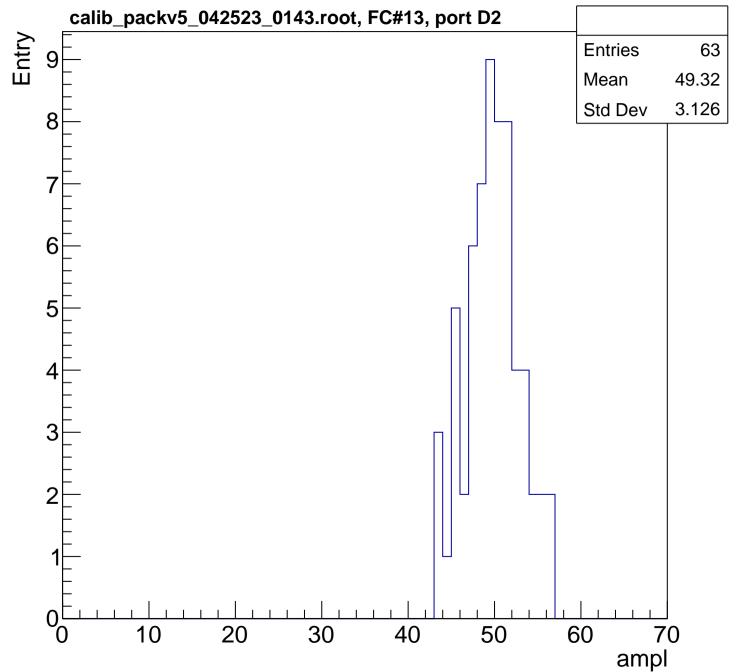


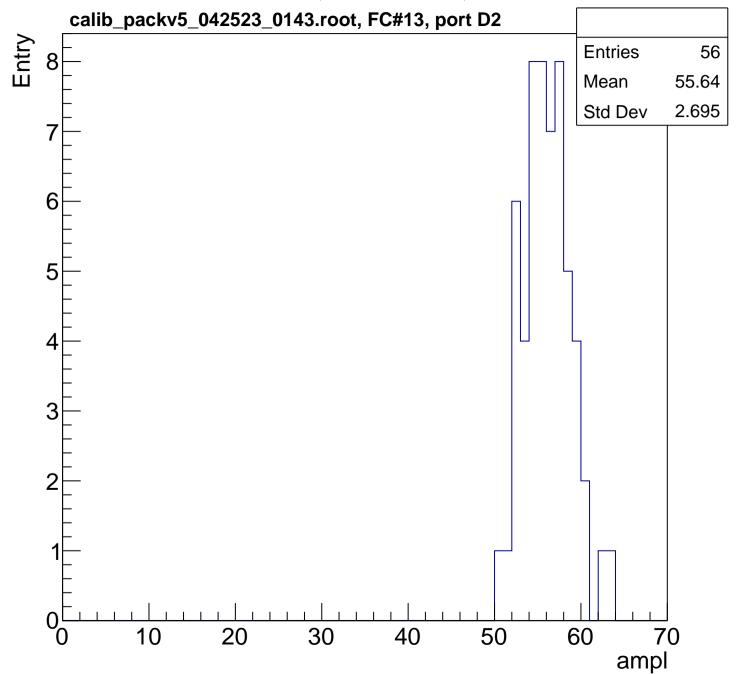


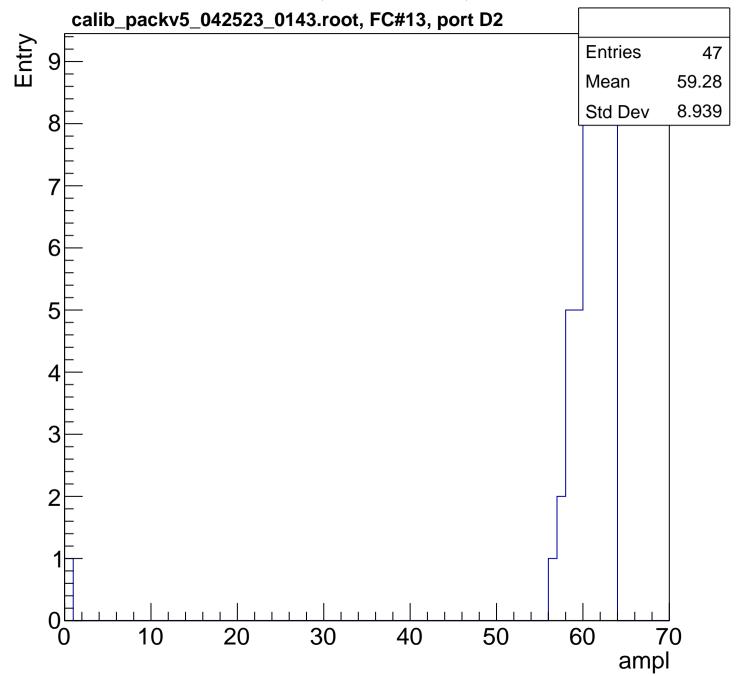


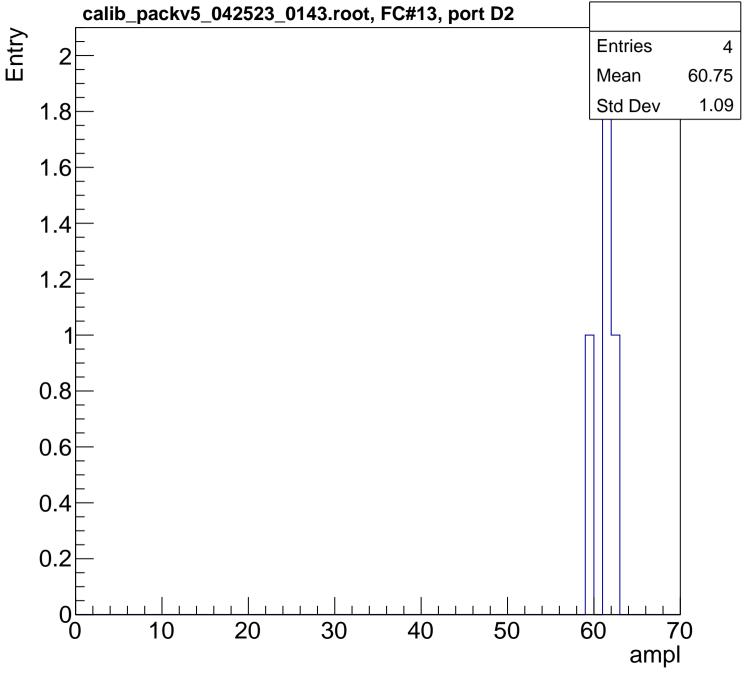




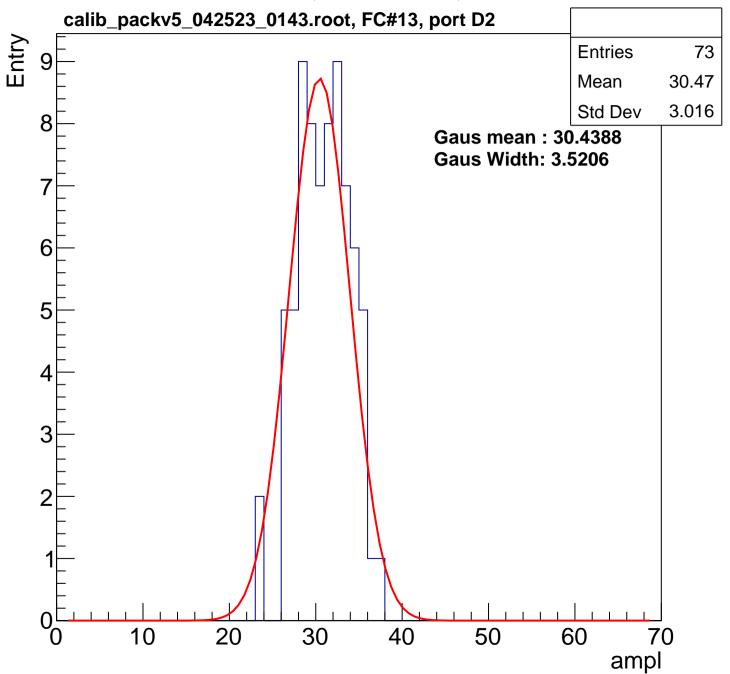


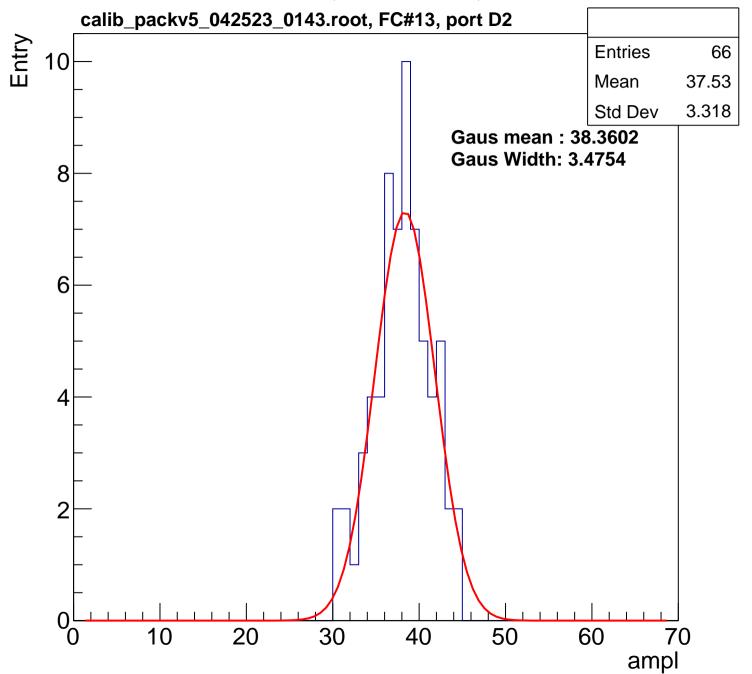


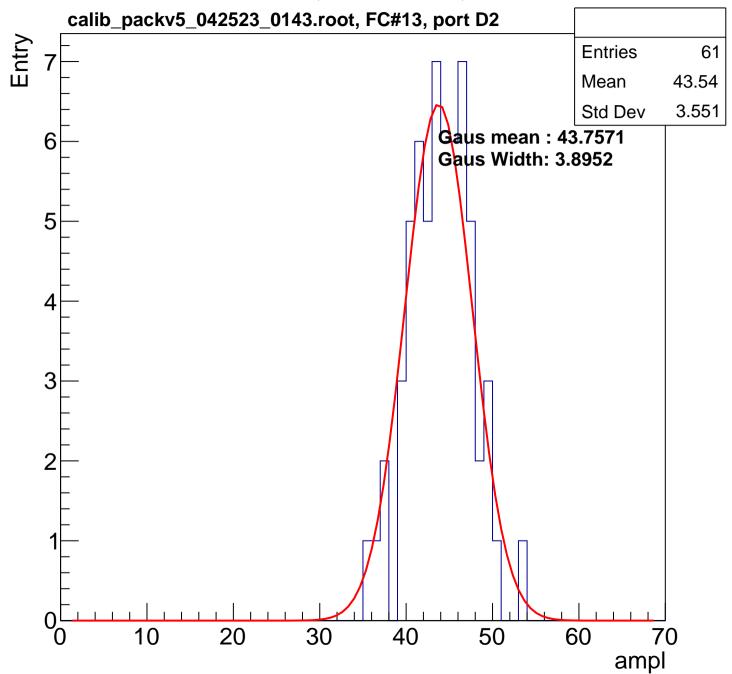


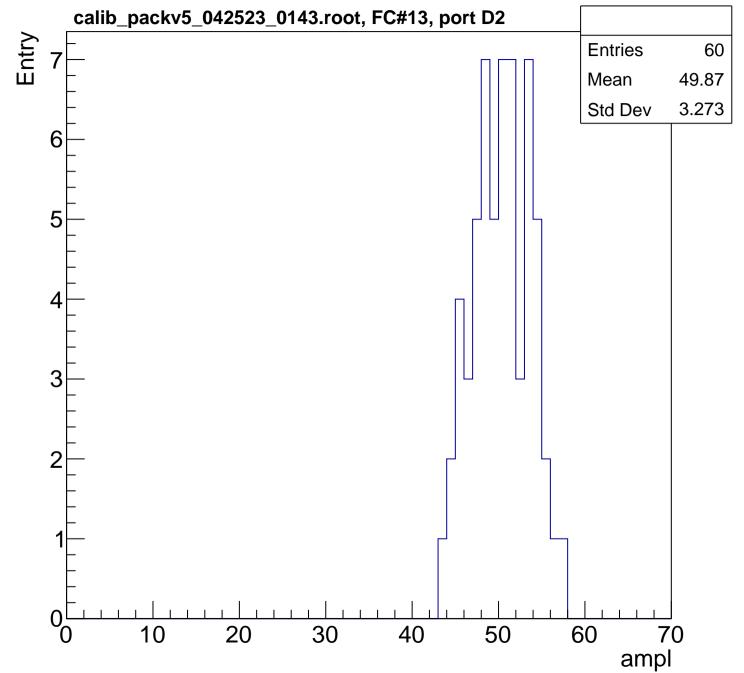


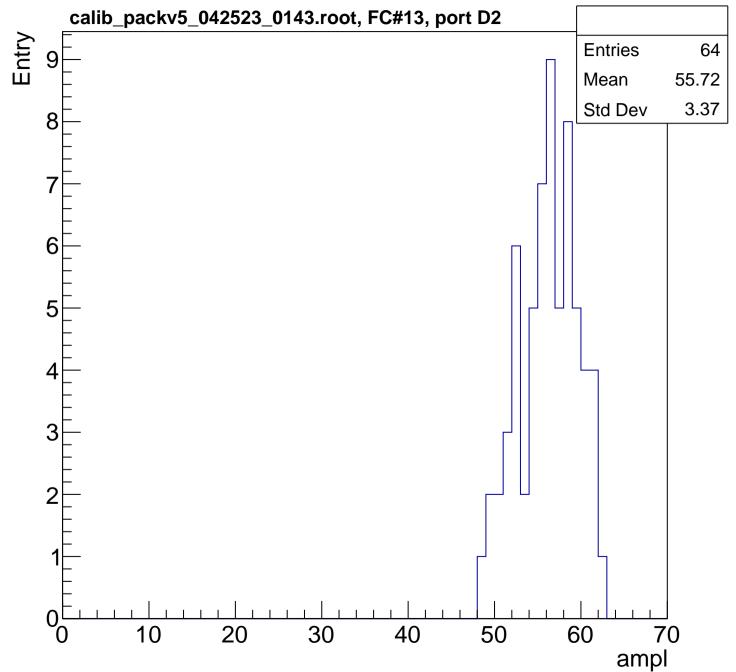


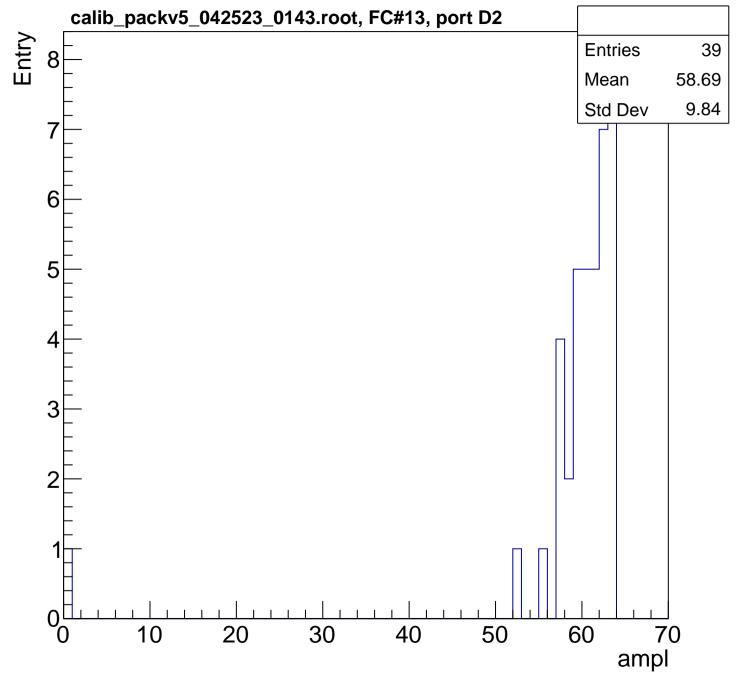


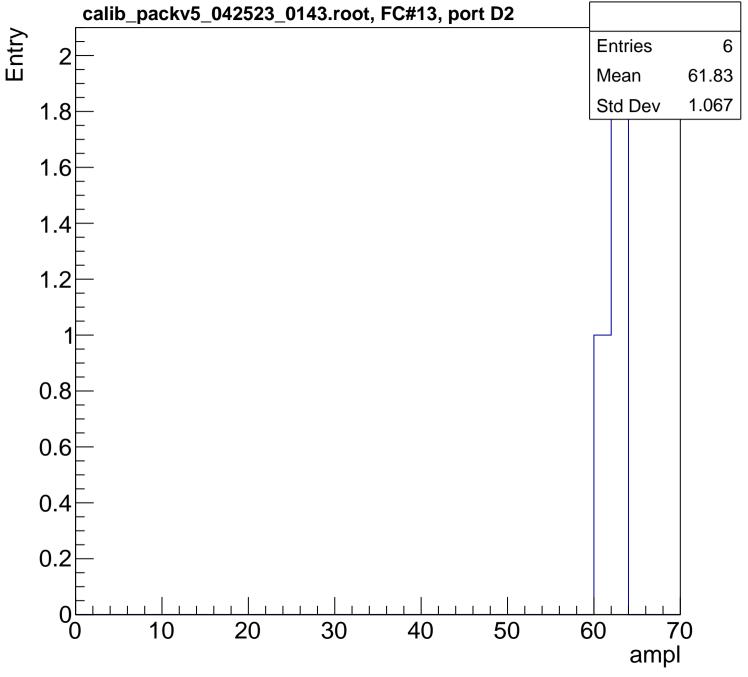




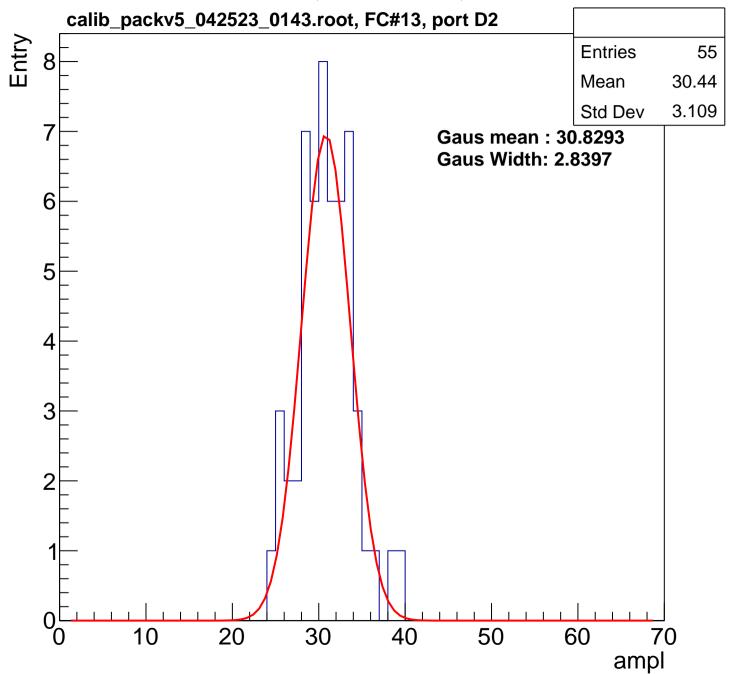


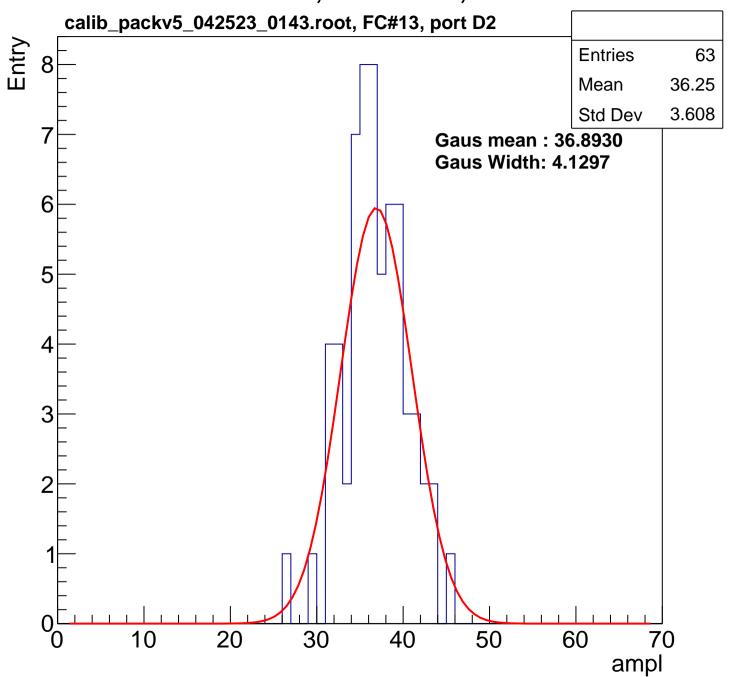


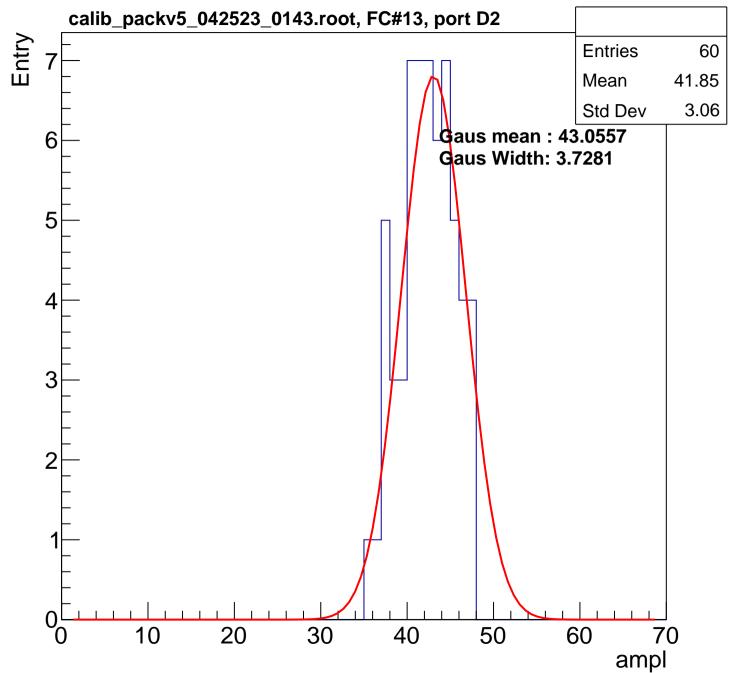


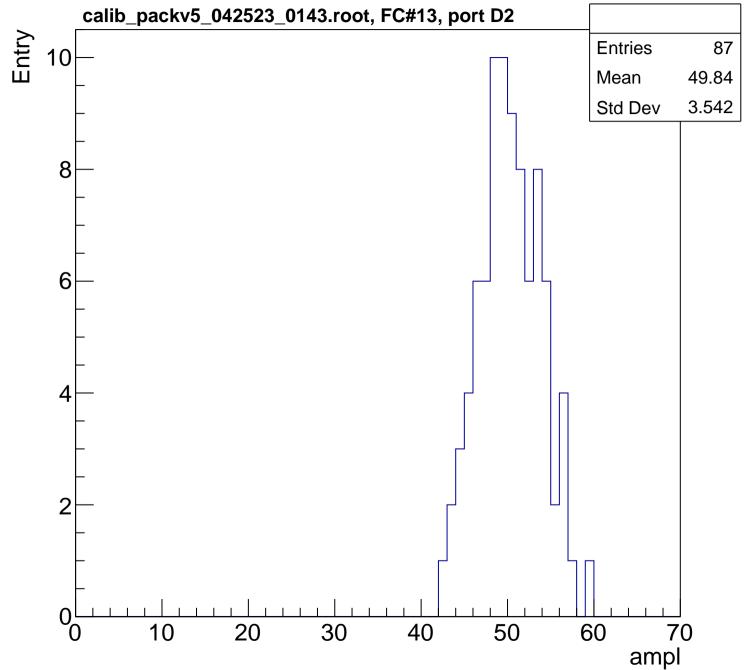


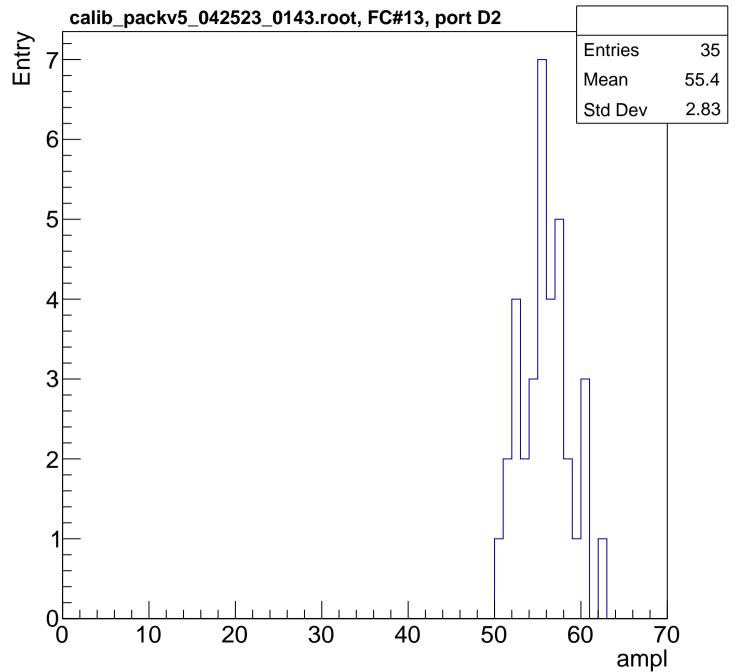


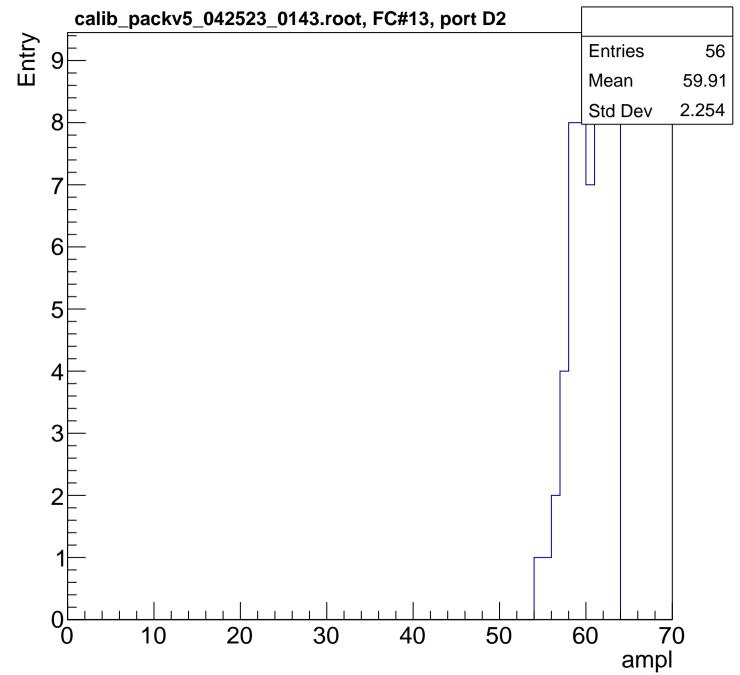


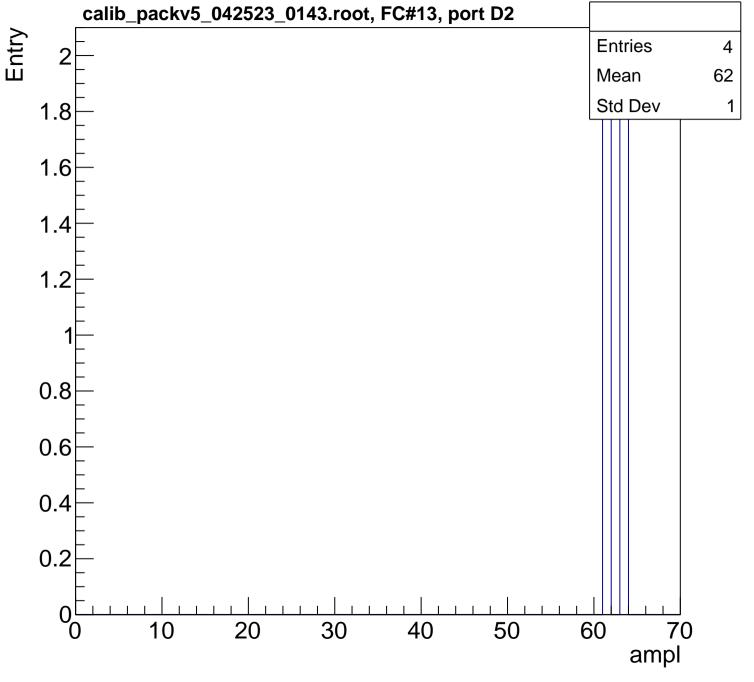




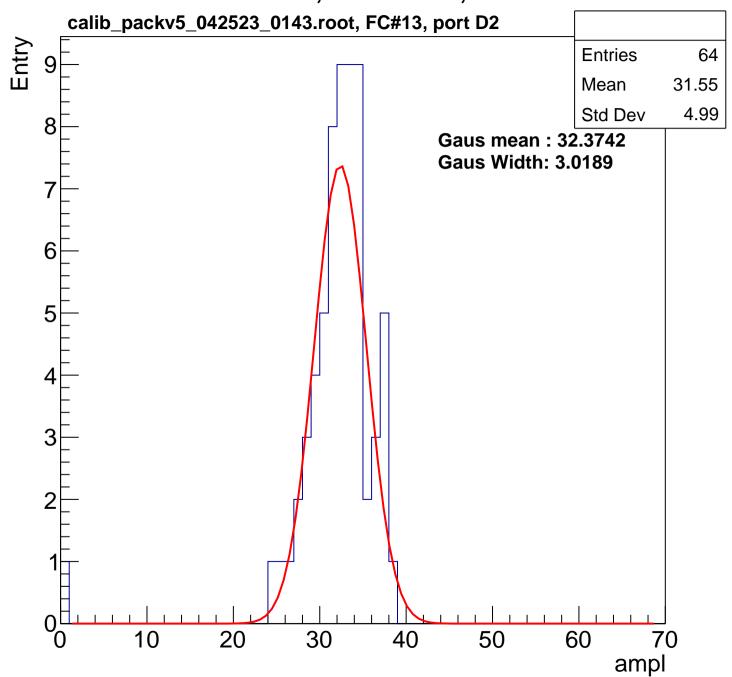


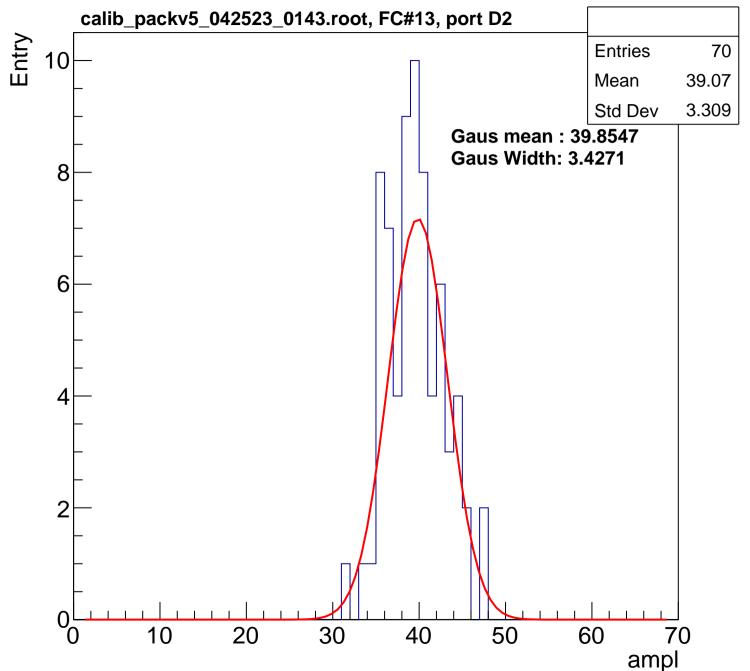


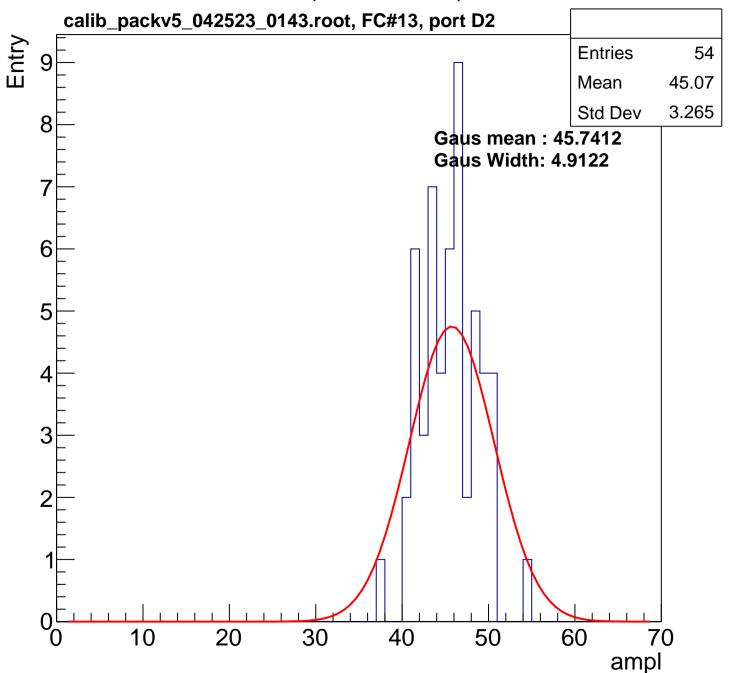


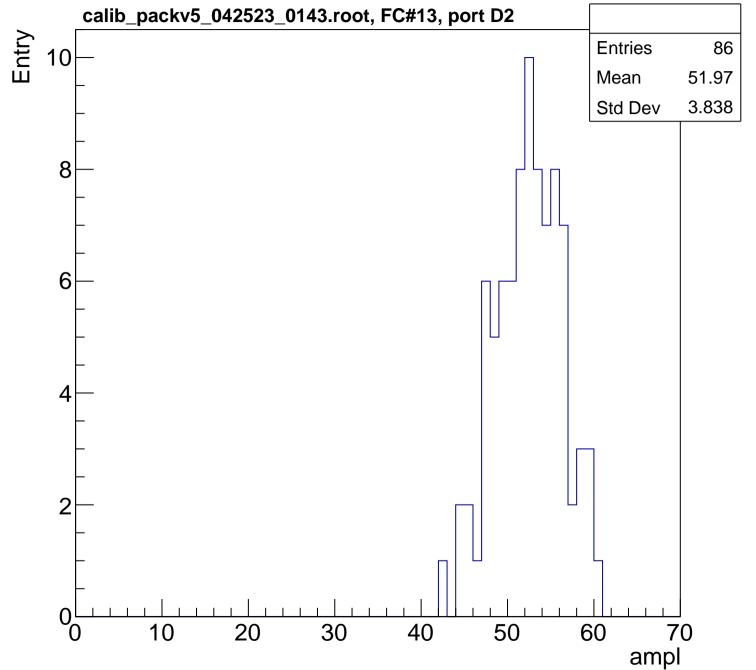


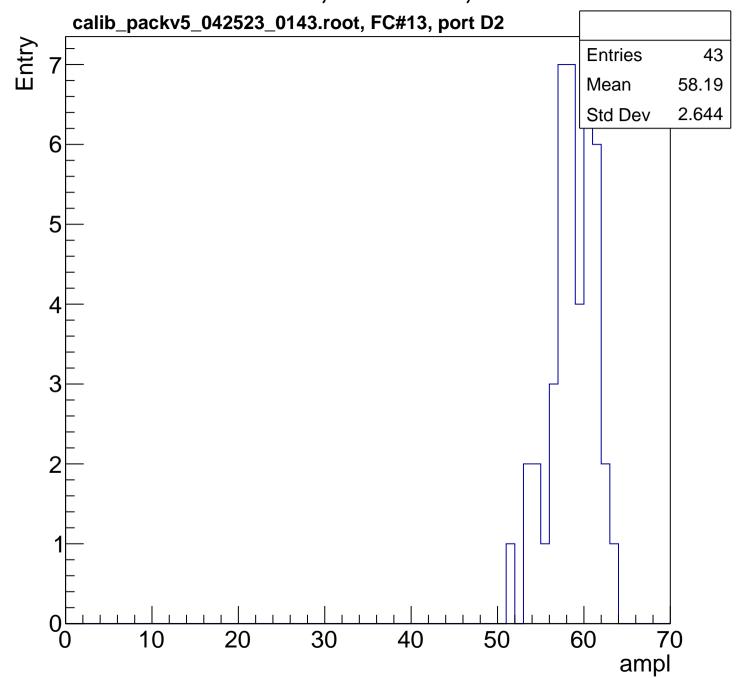


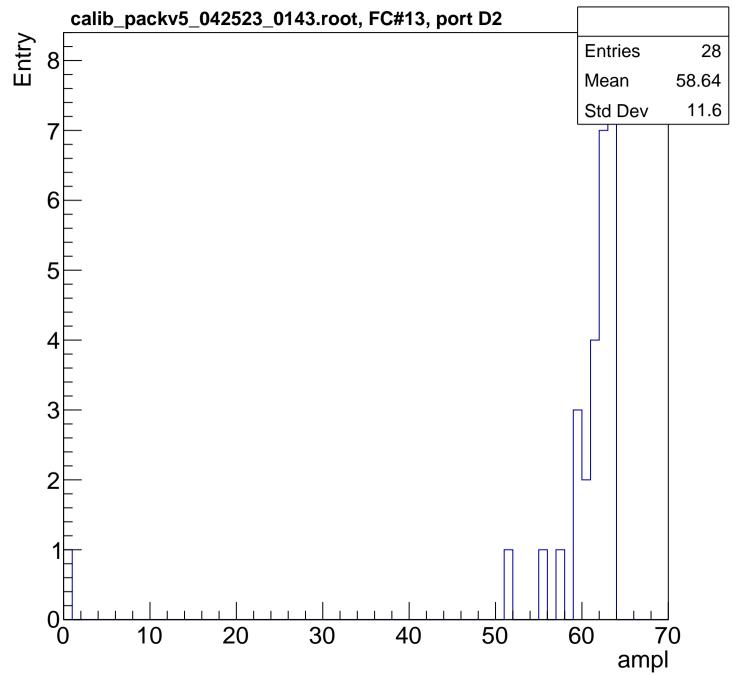


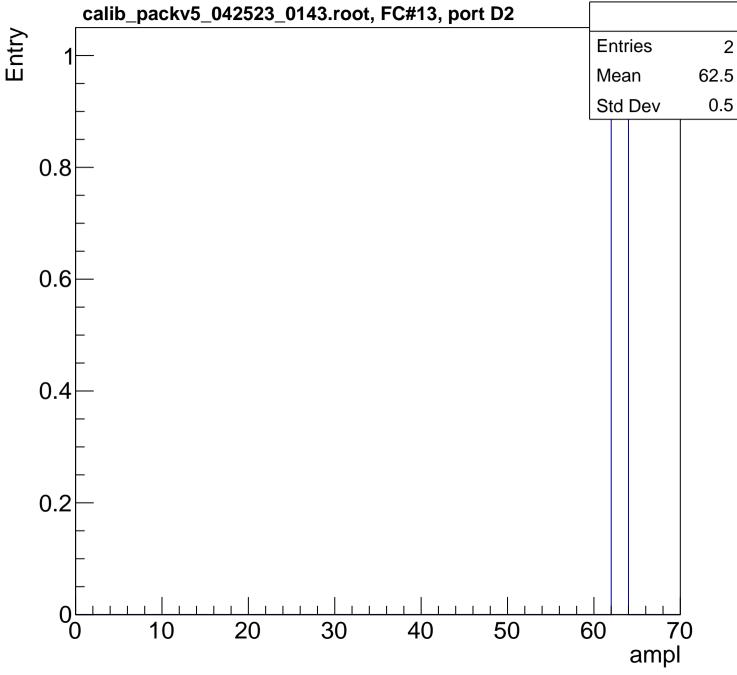


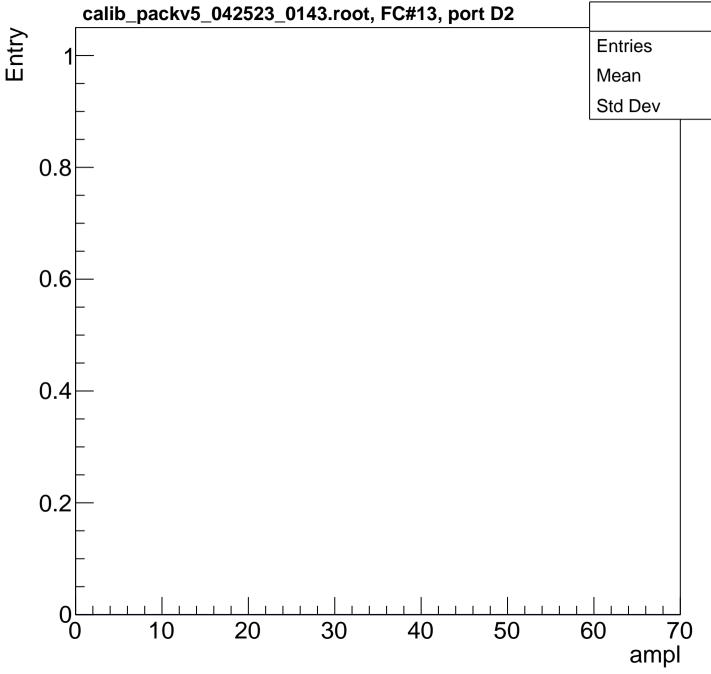


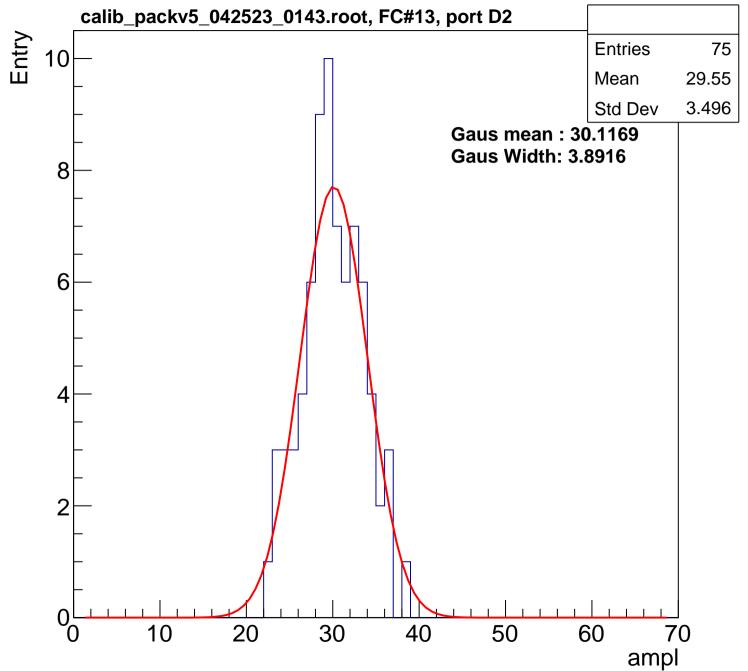


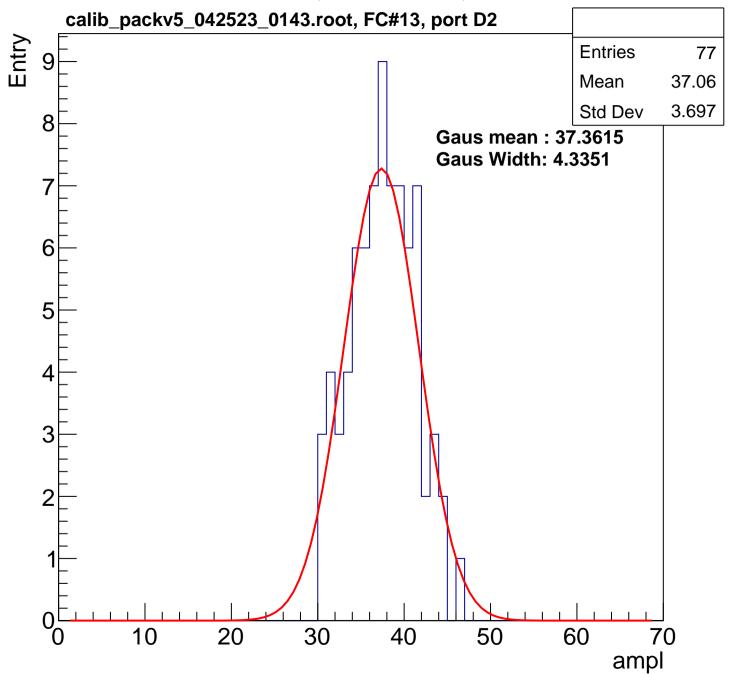


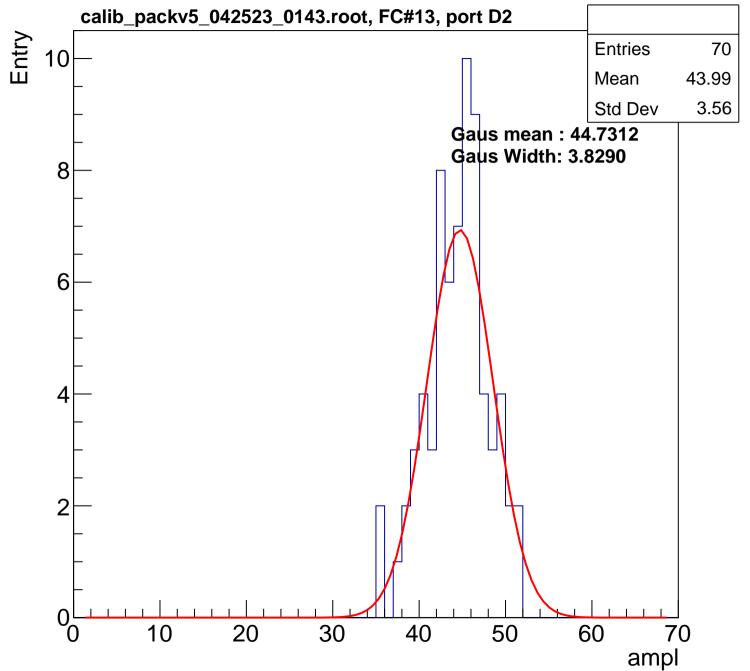


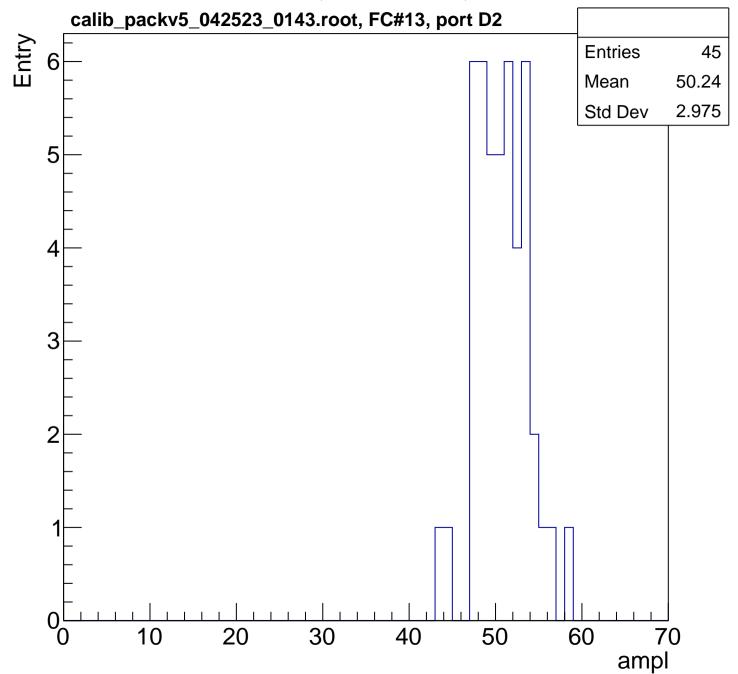


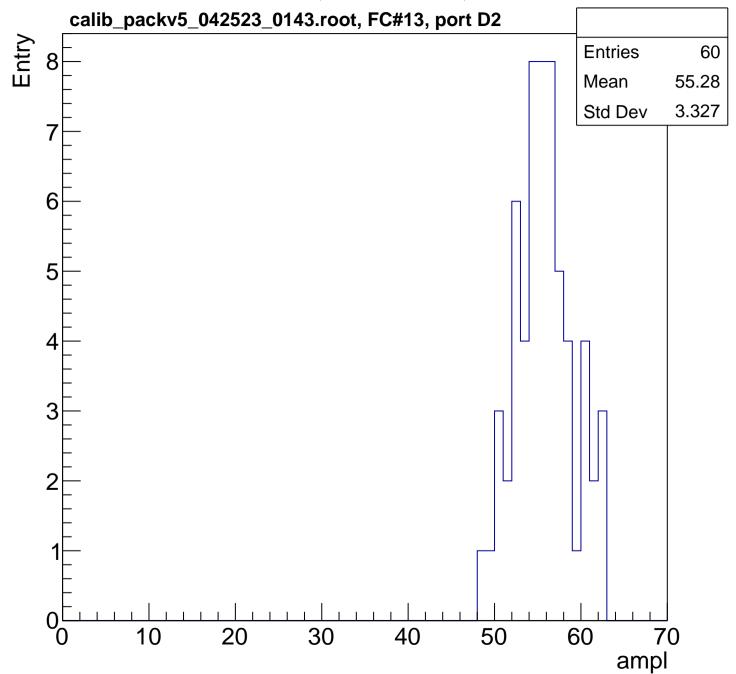


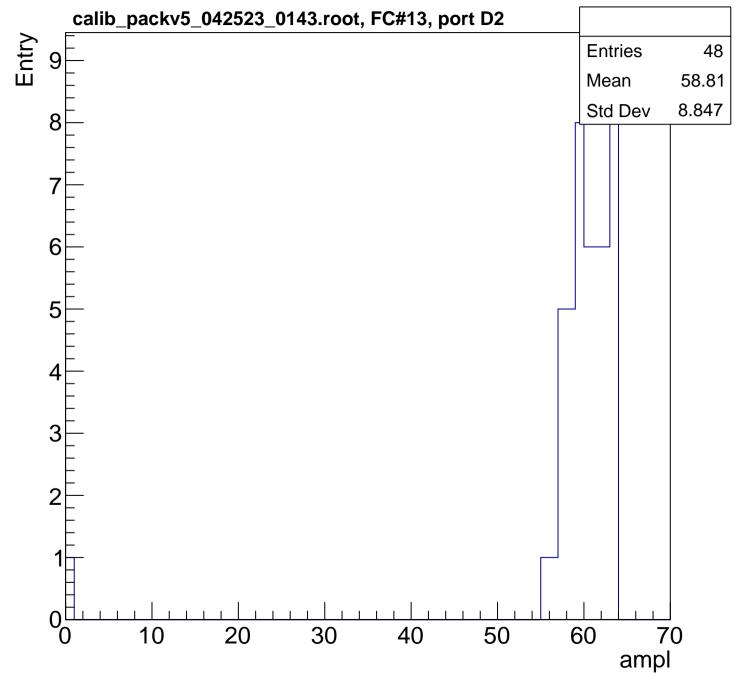


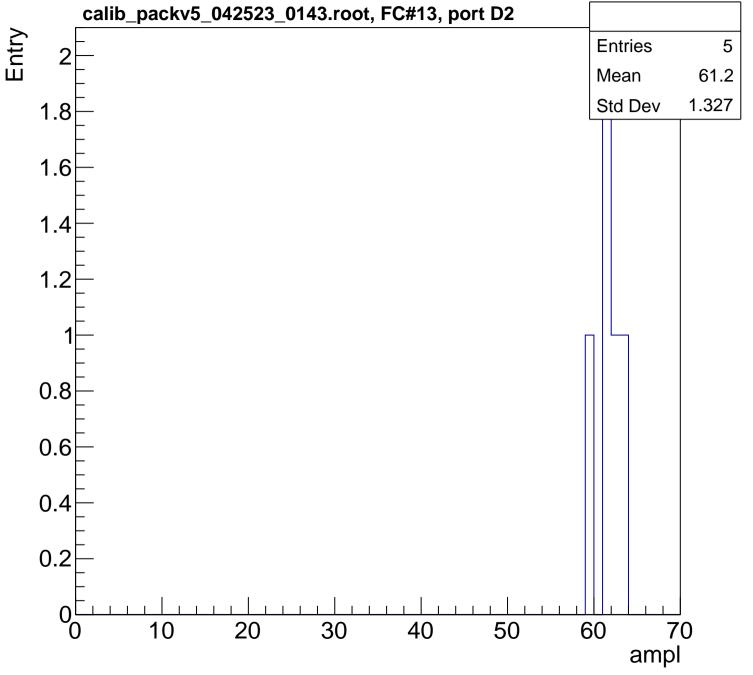


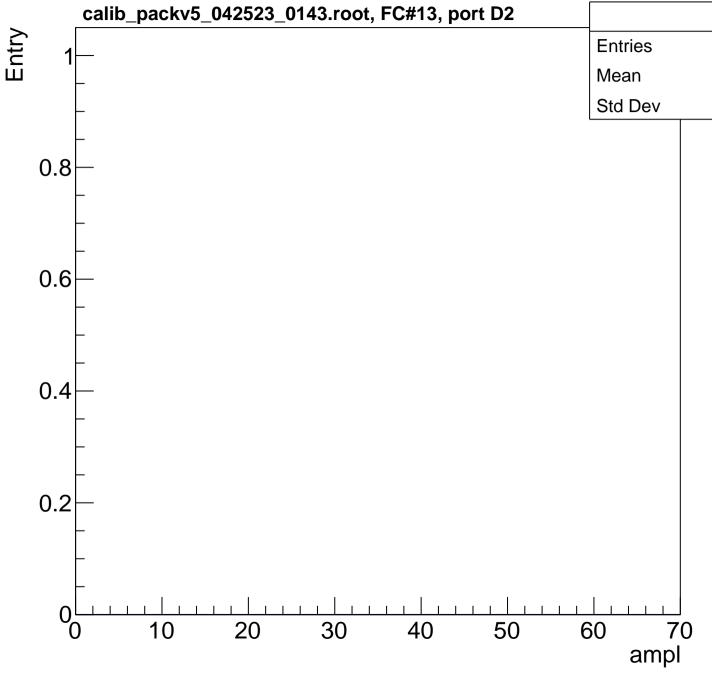


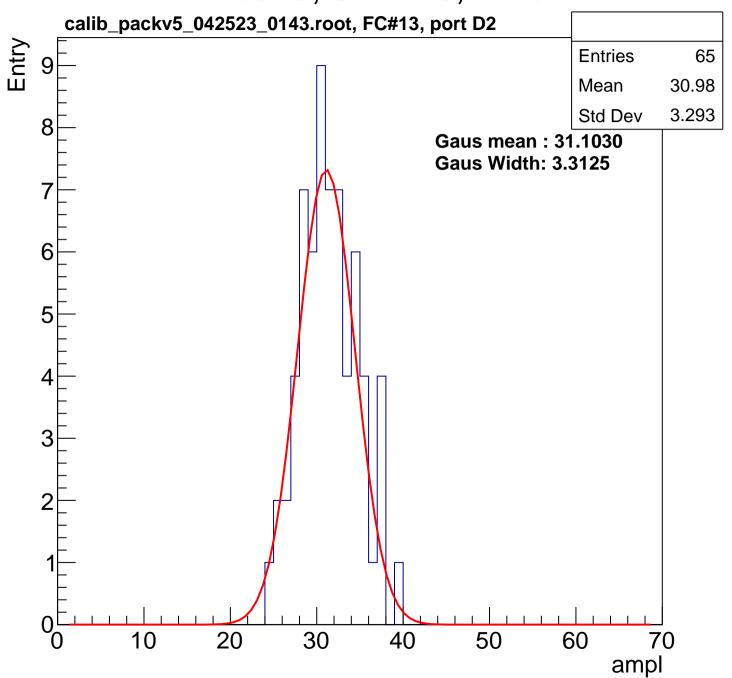


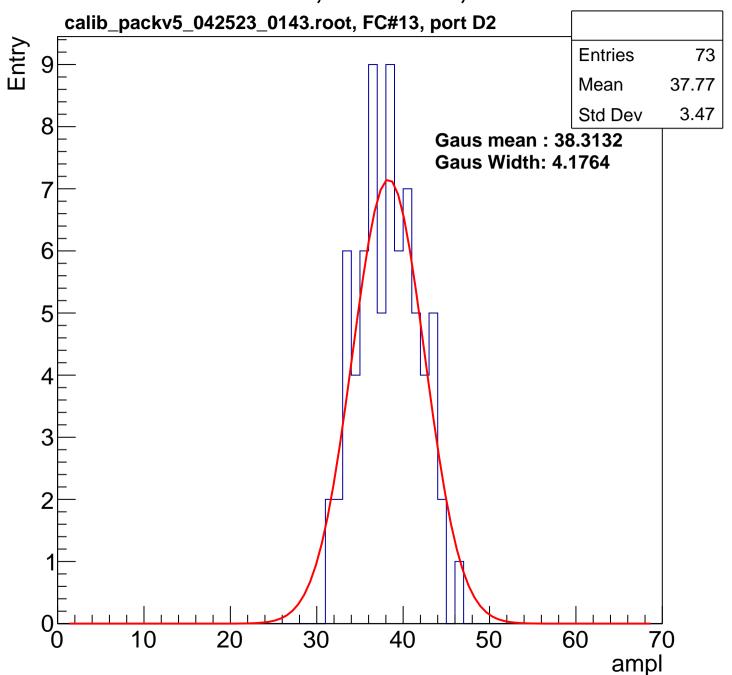


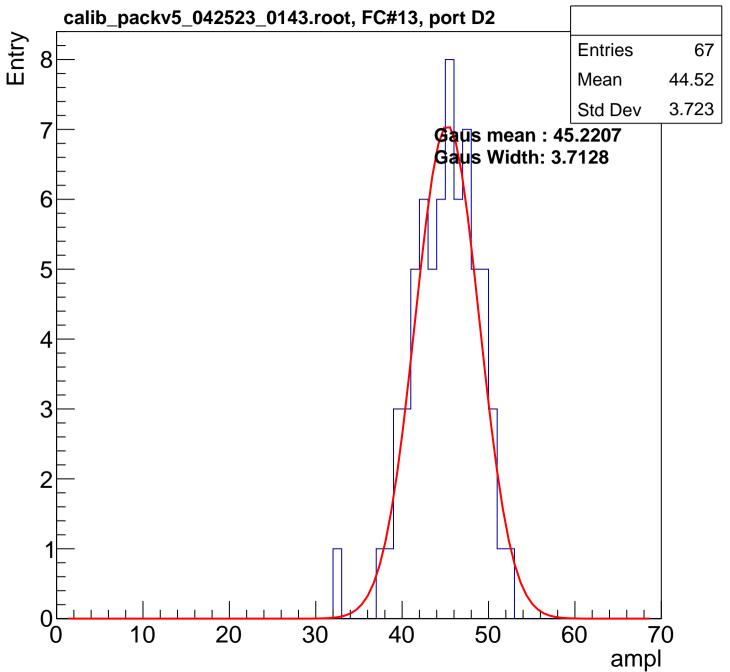


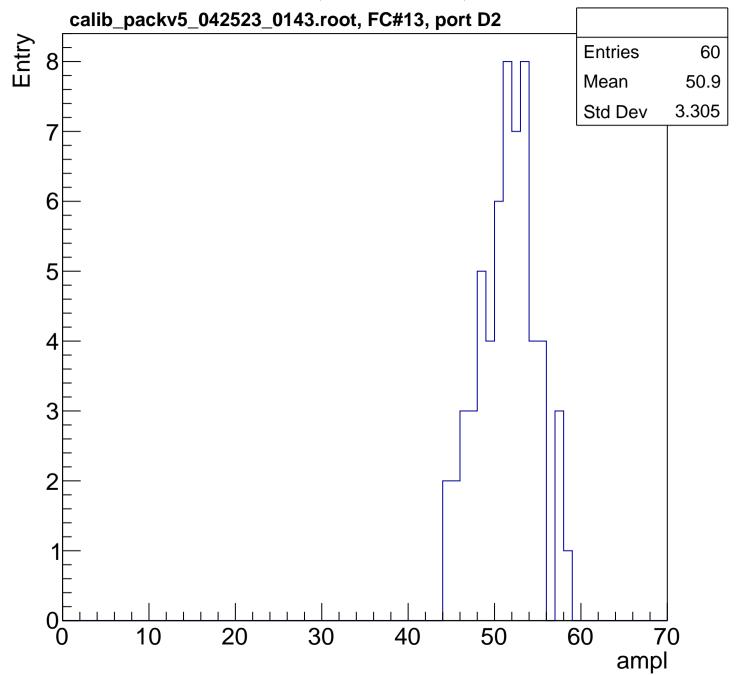


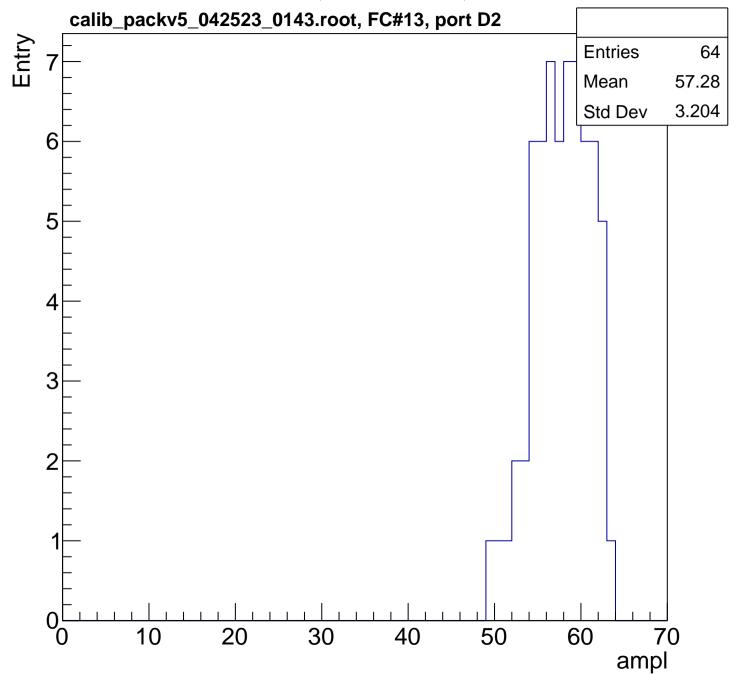


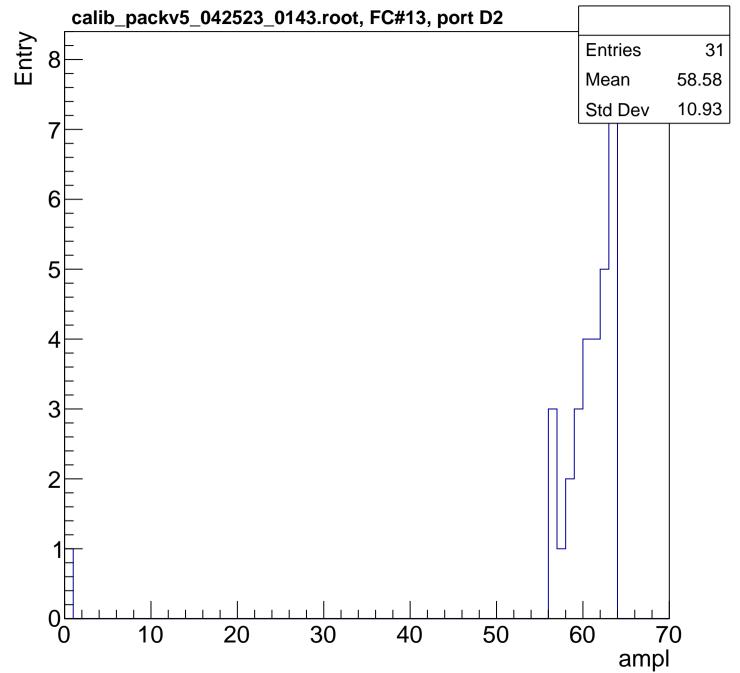


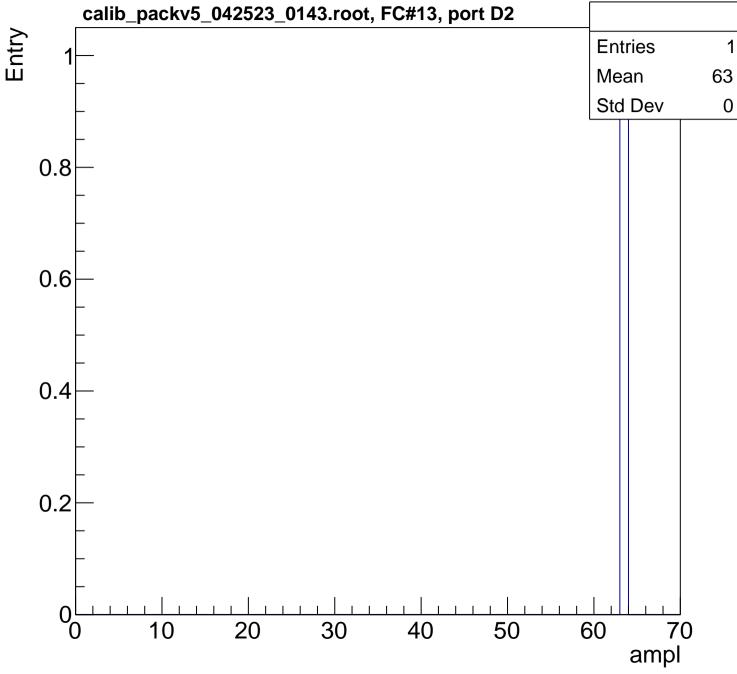


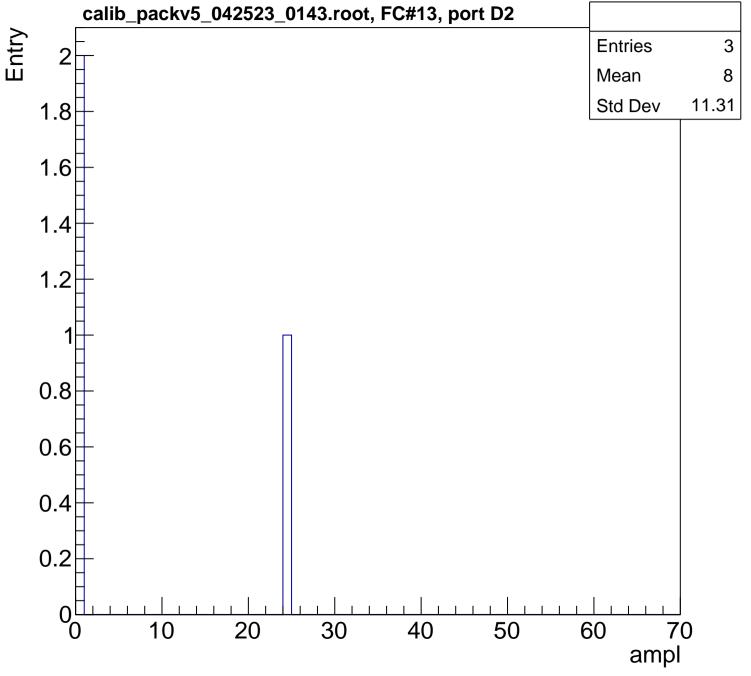


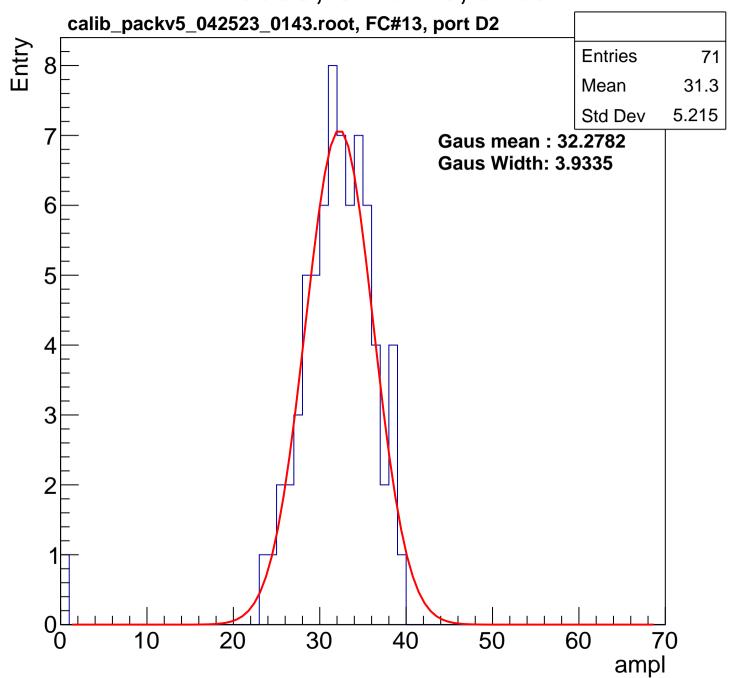


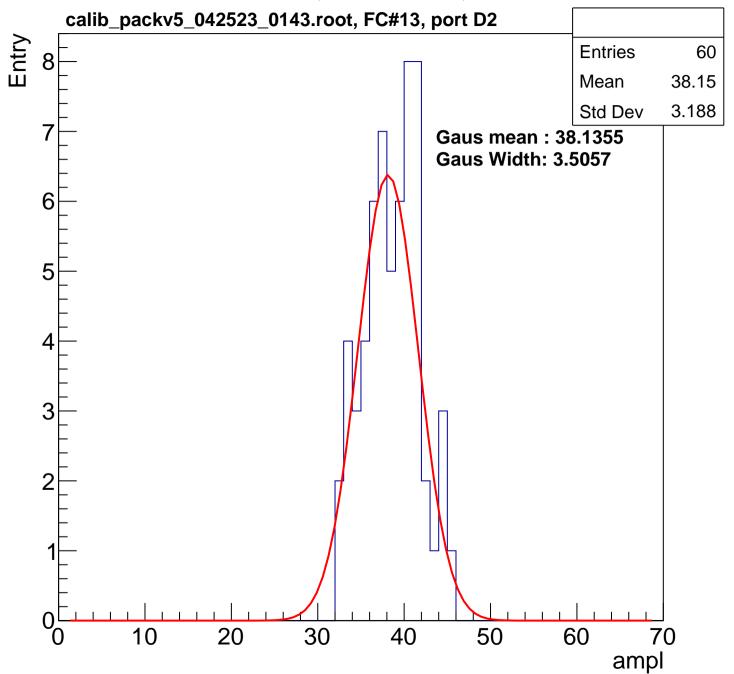


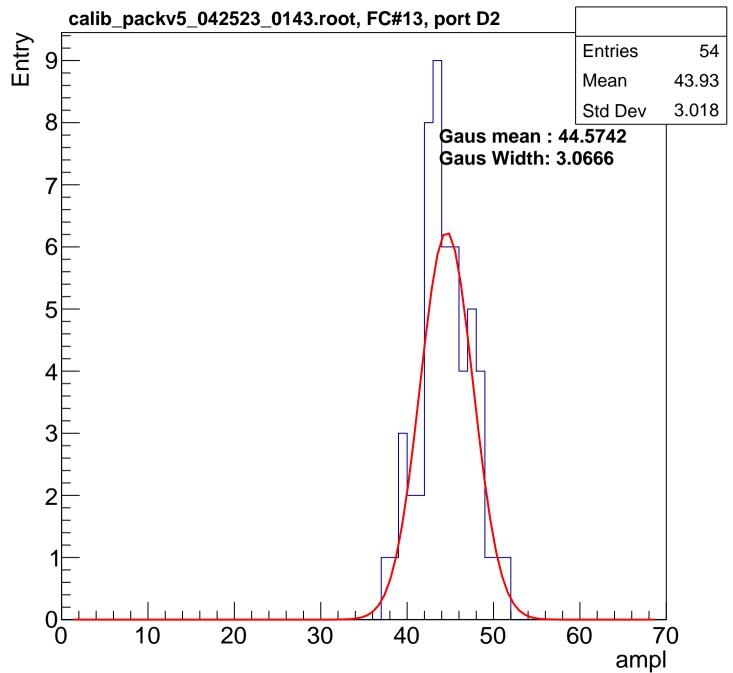


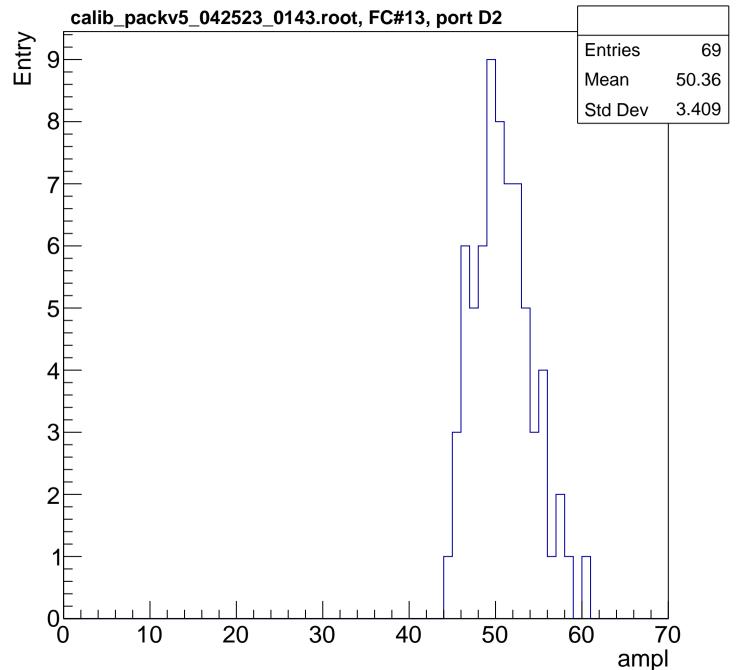


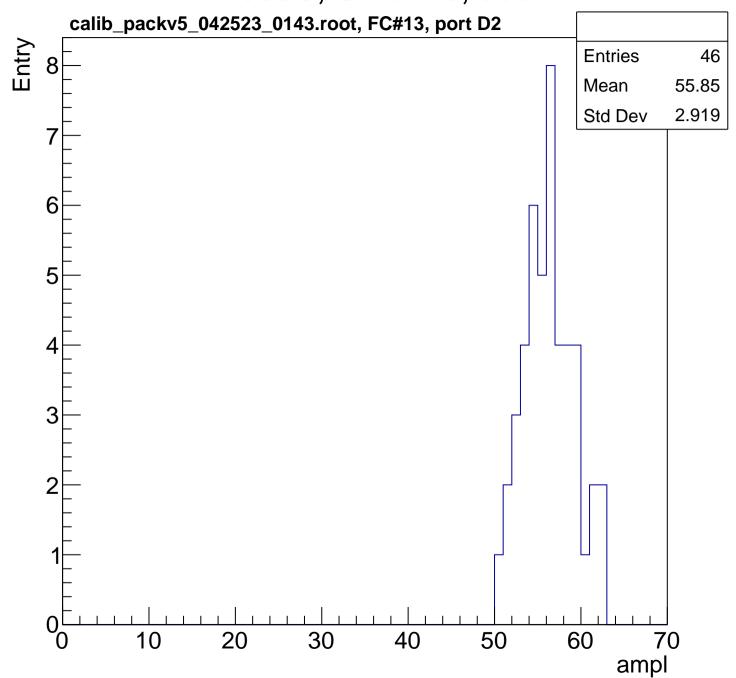


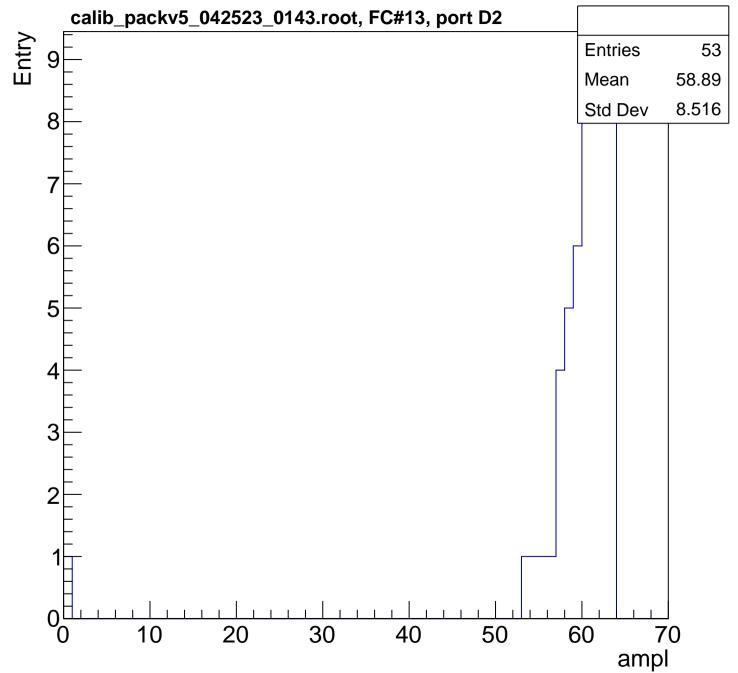


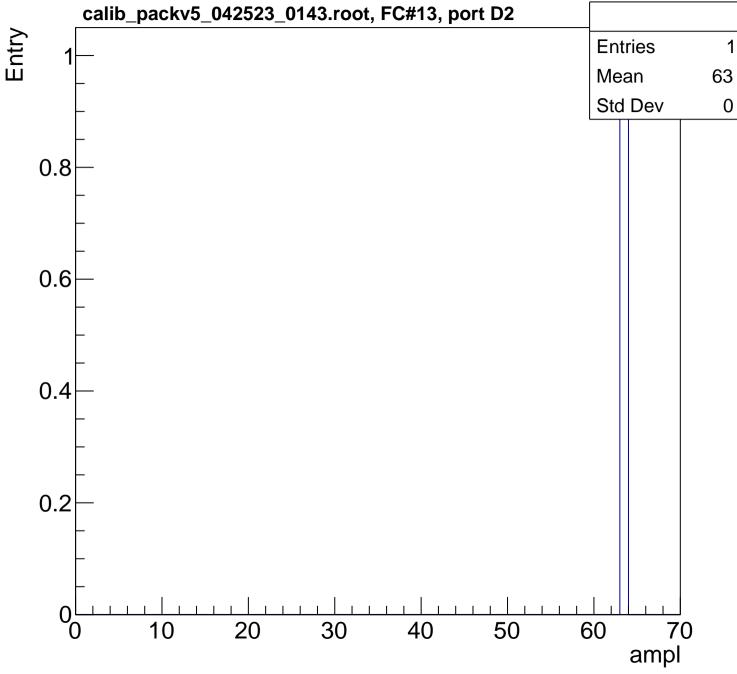




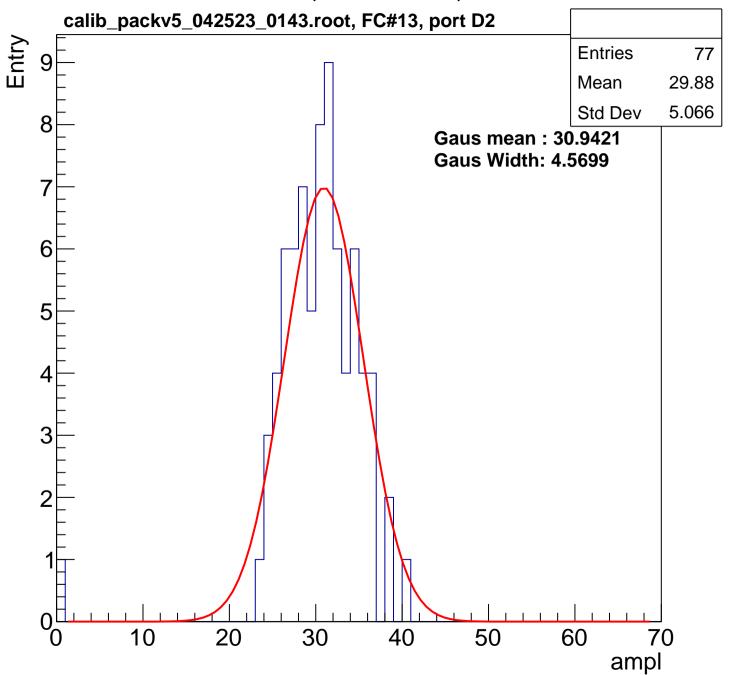


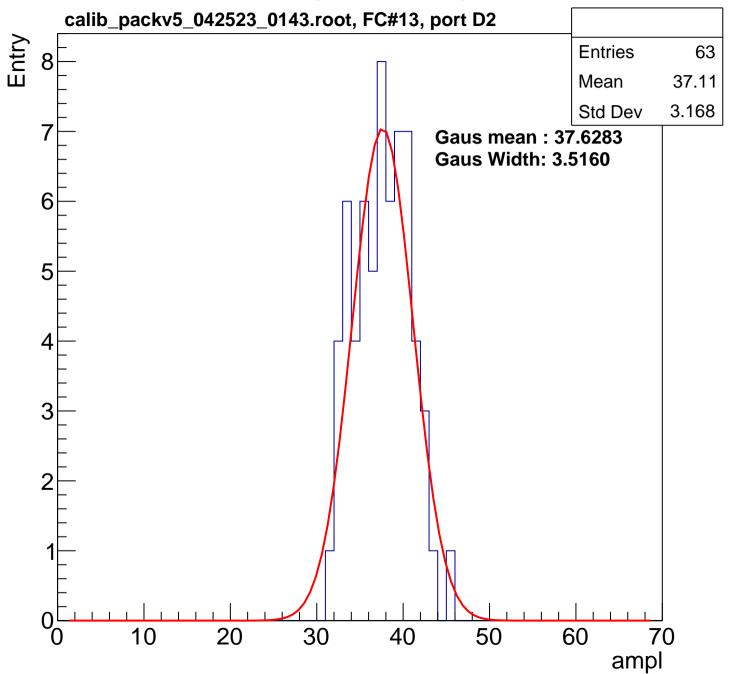


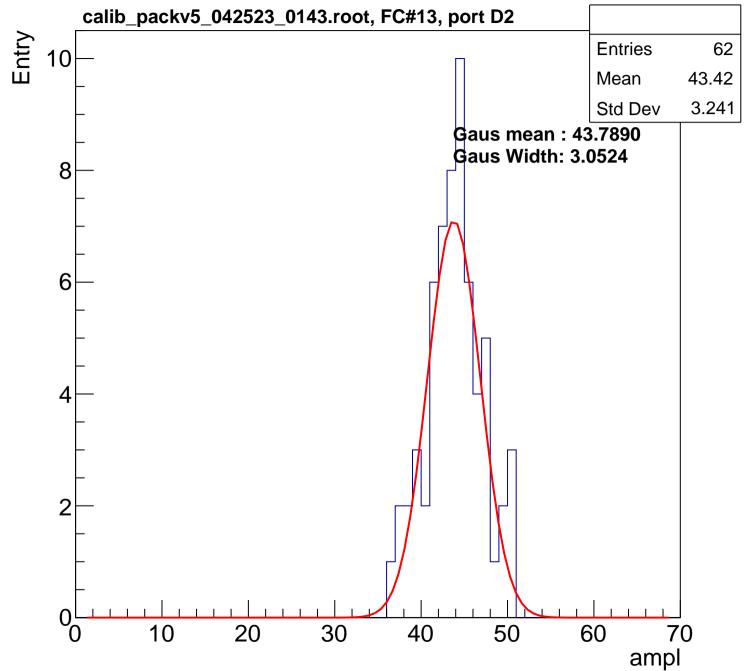


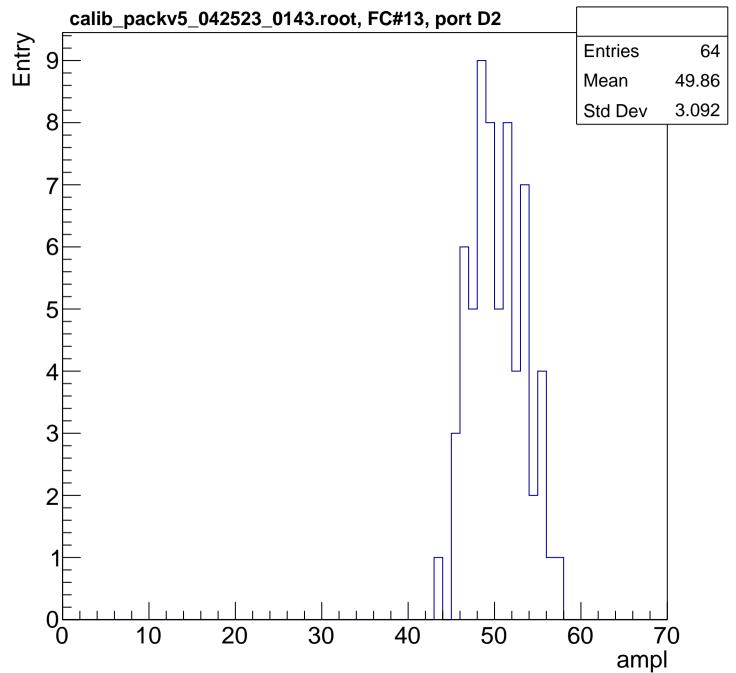


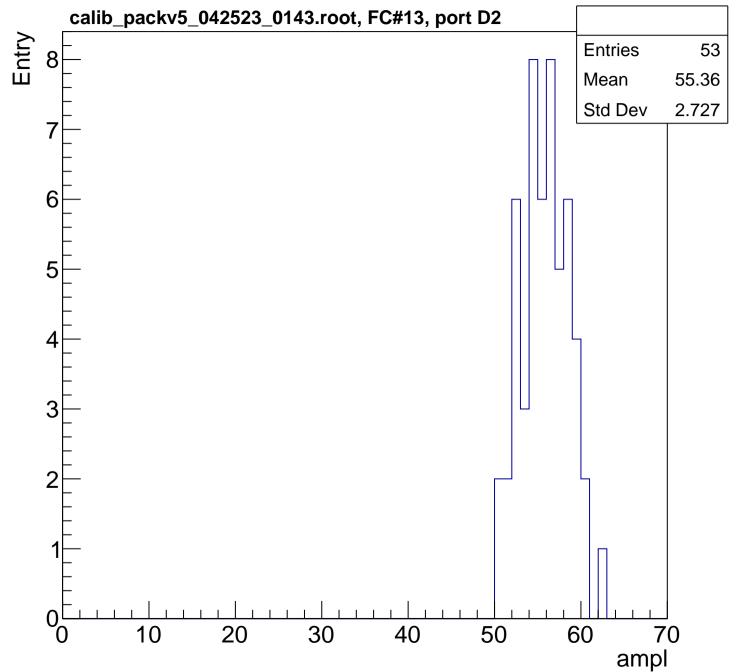
B1L003S, U2-ch20, adc7 calib_packv5_042523_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

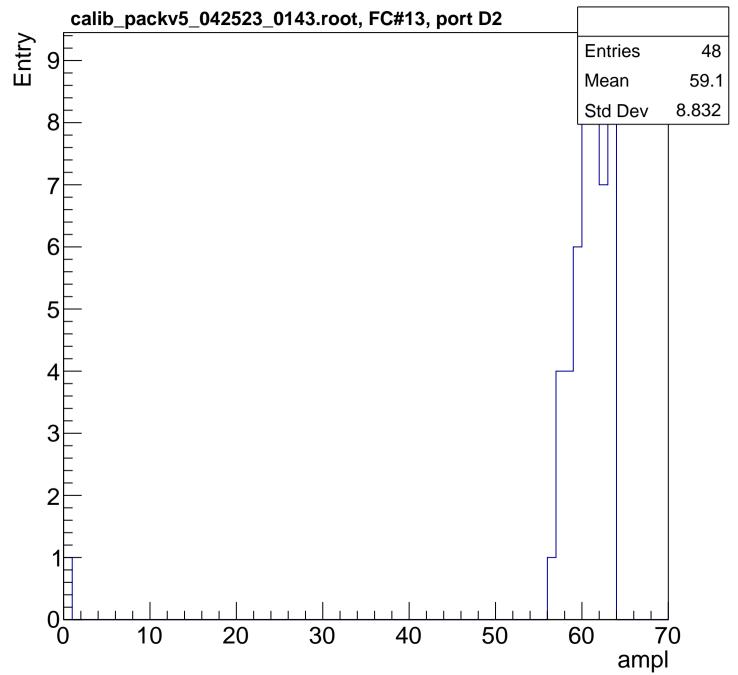


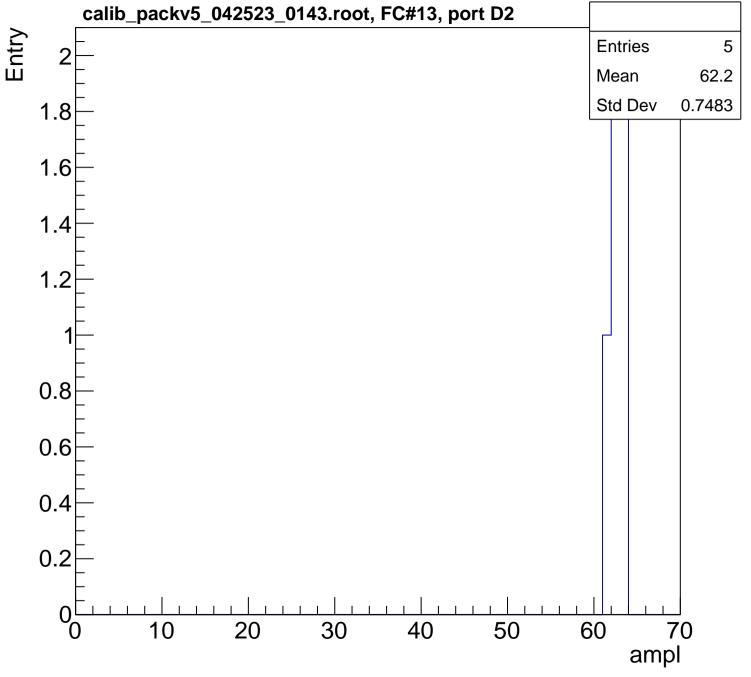




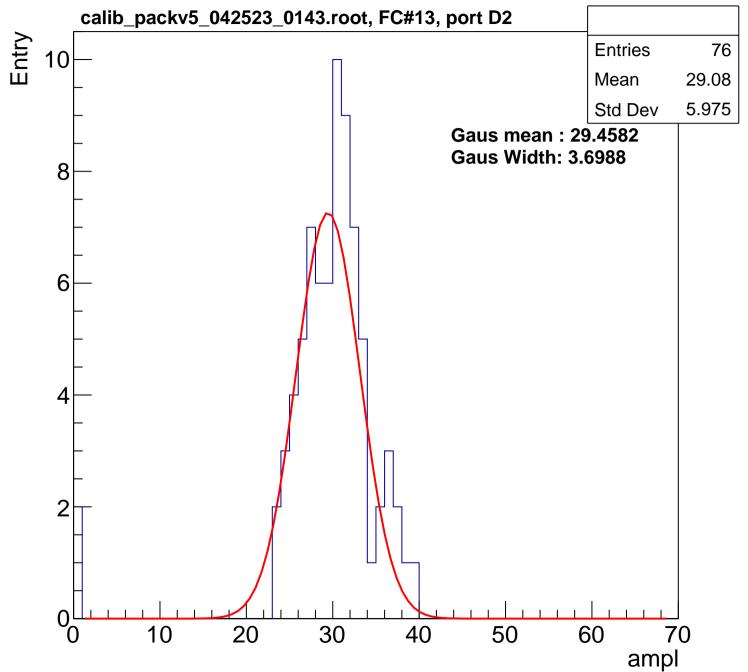


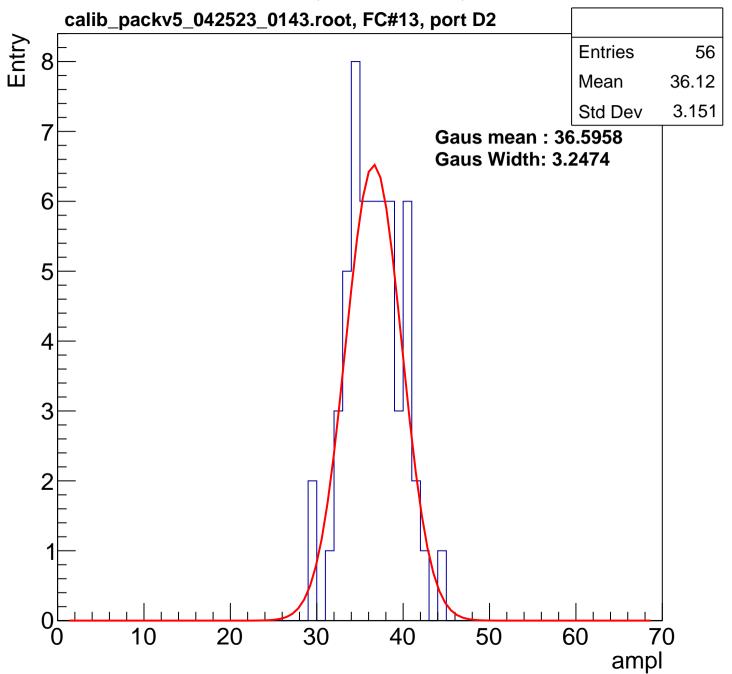


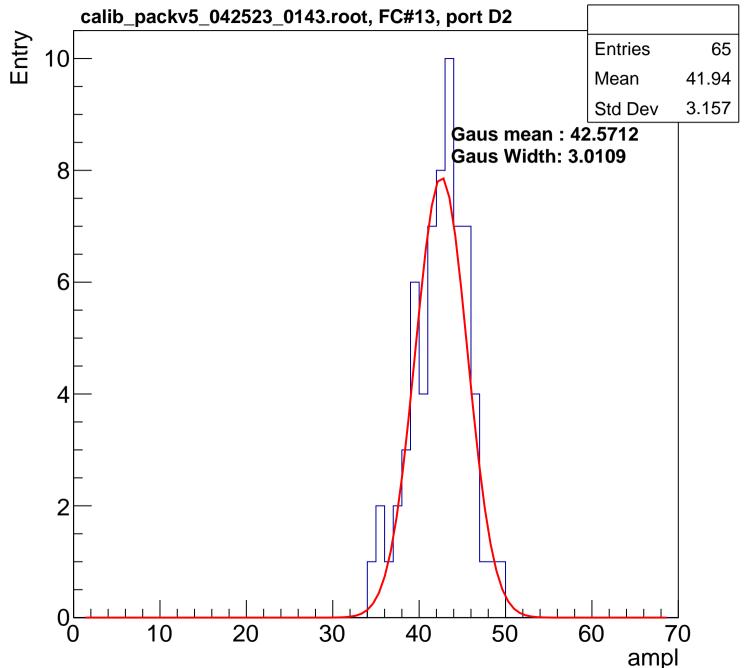


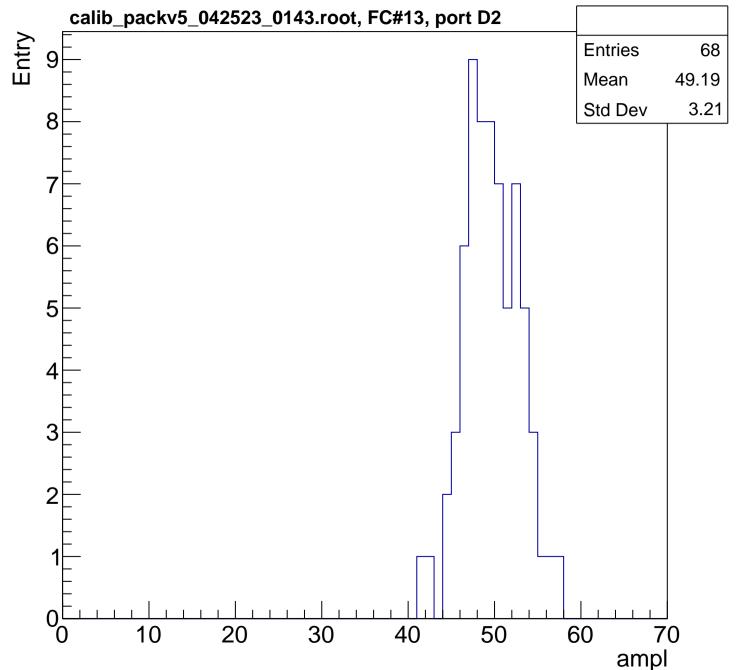


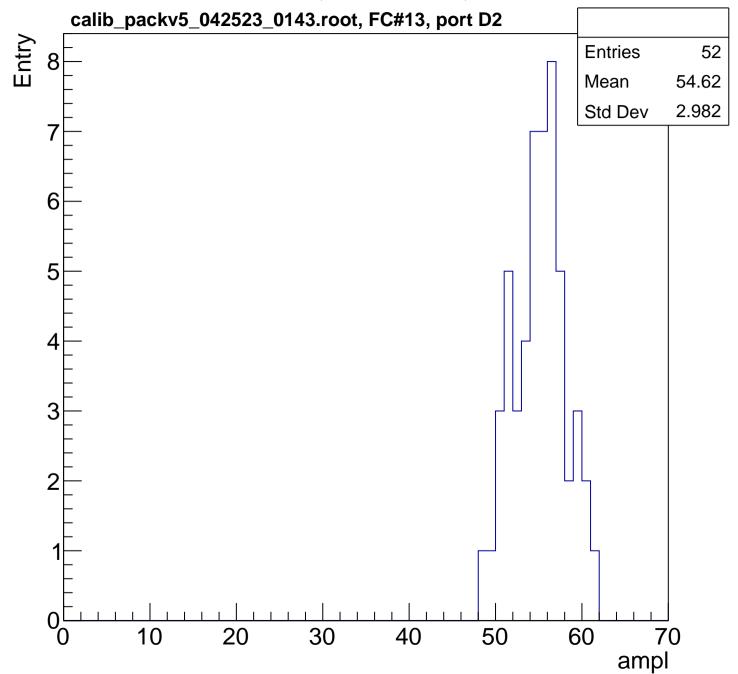


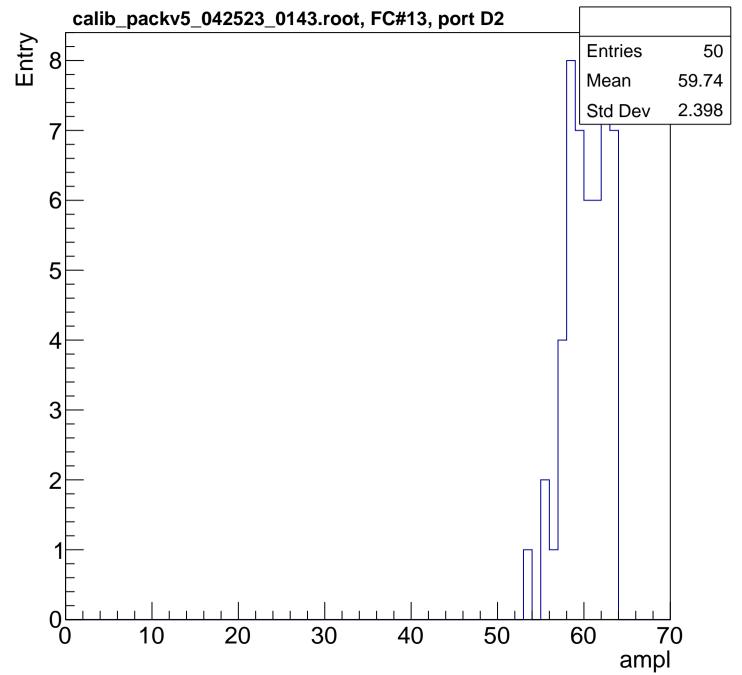


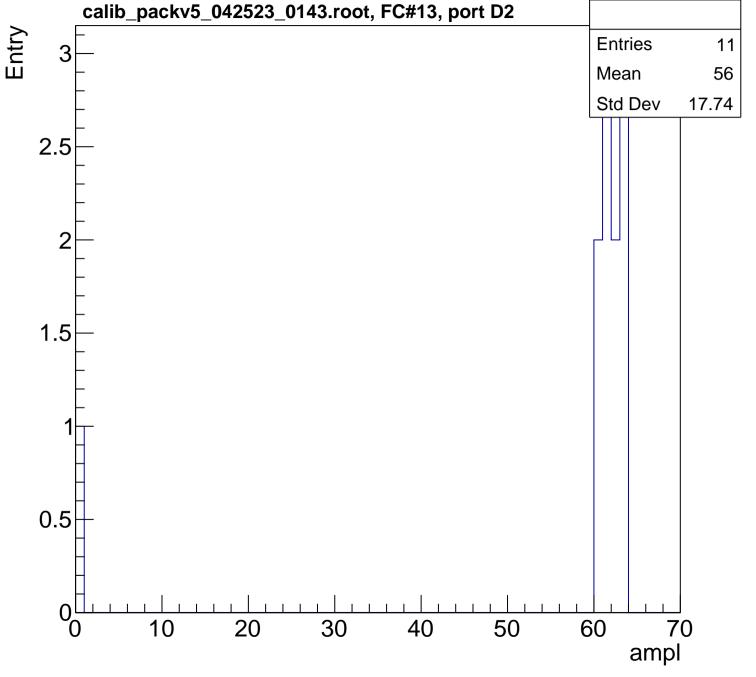


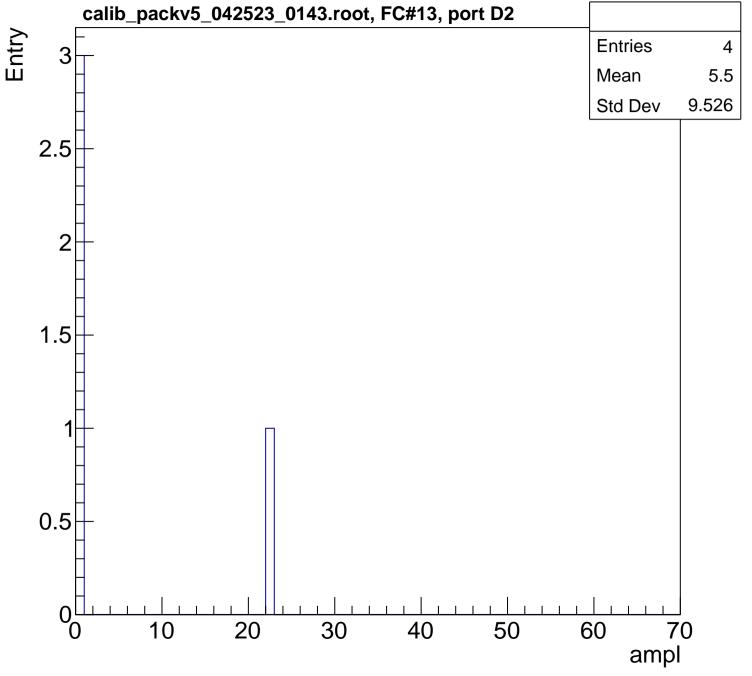


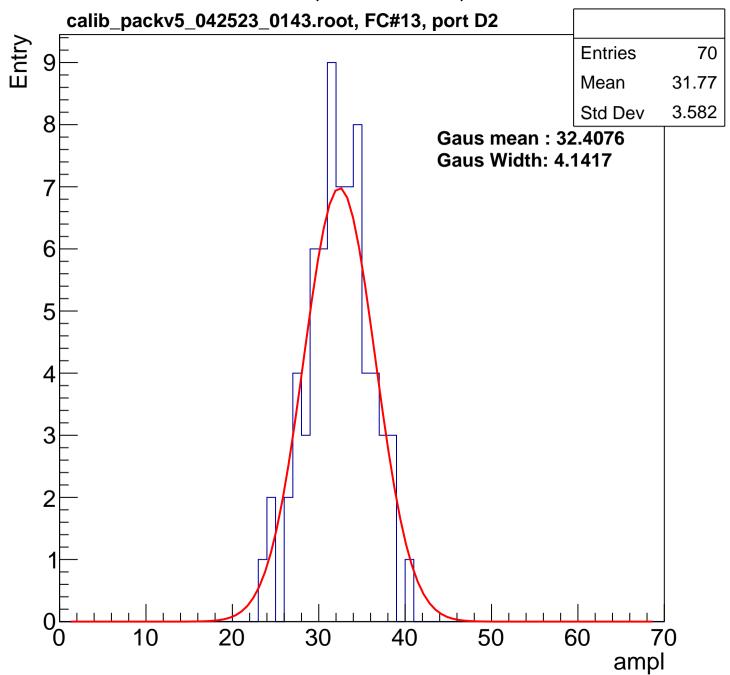


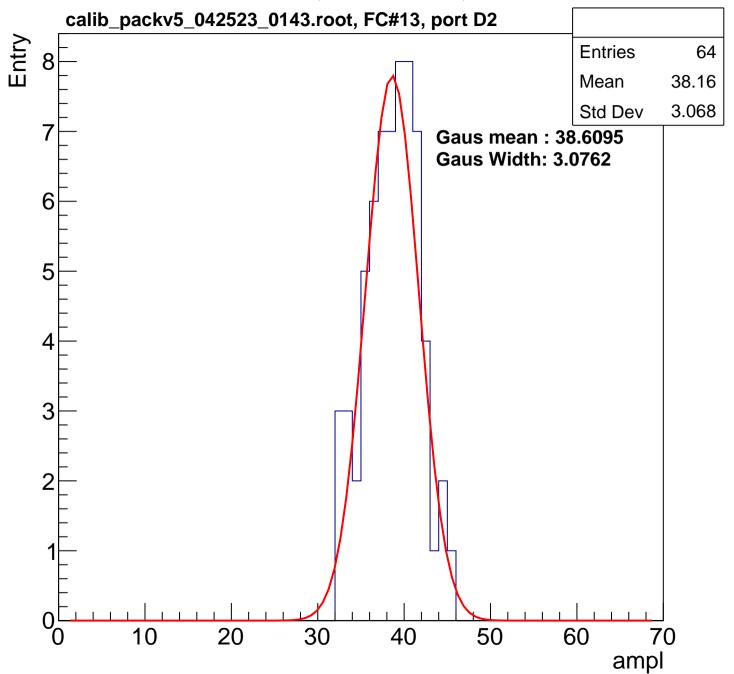


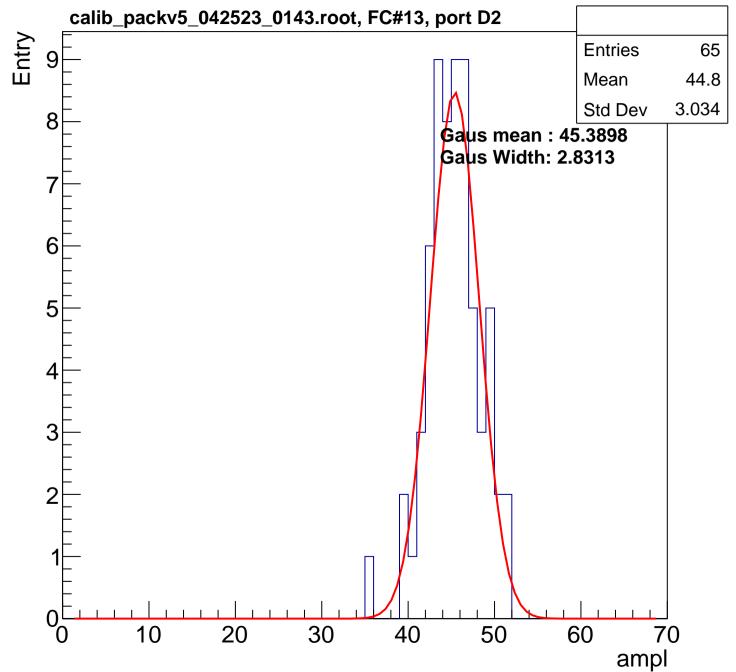


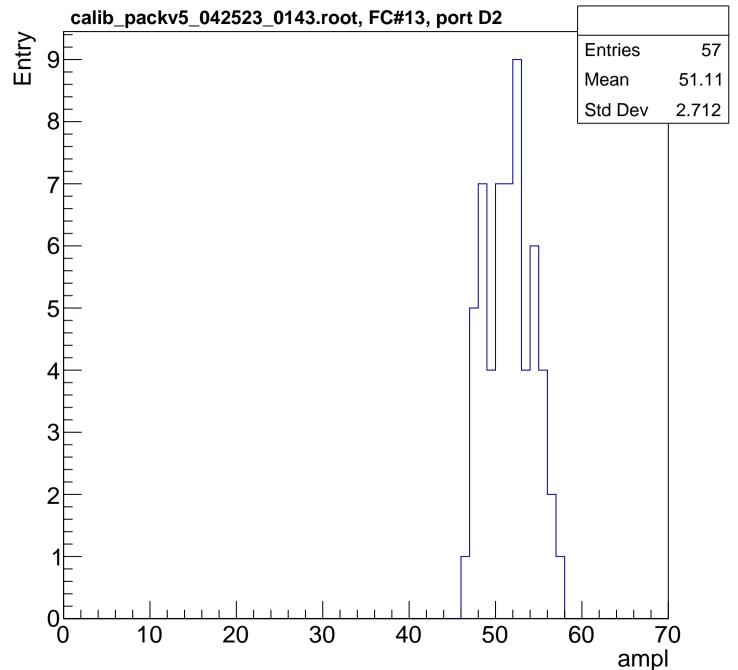


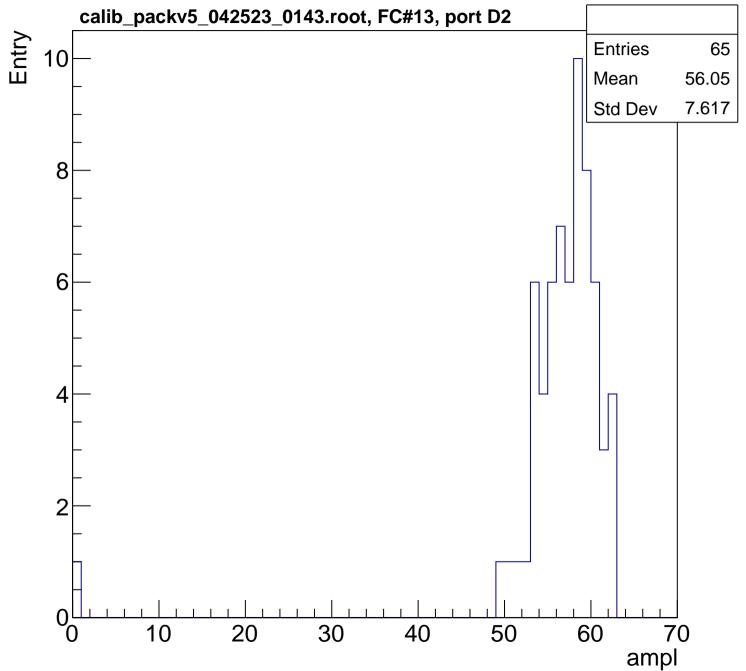


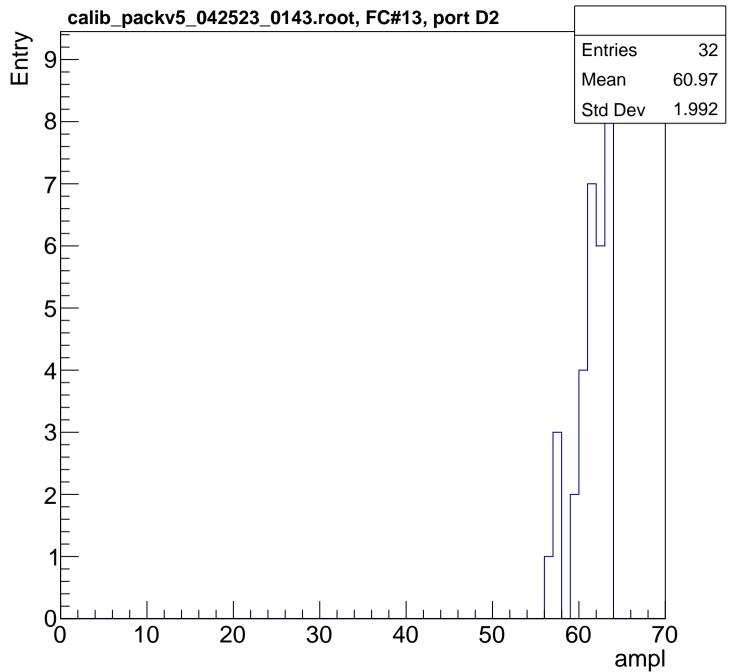


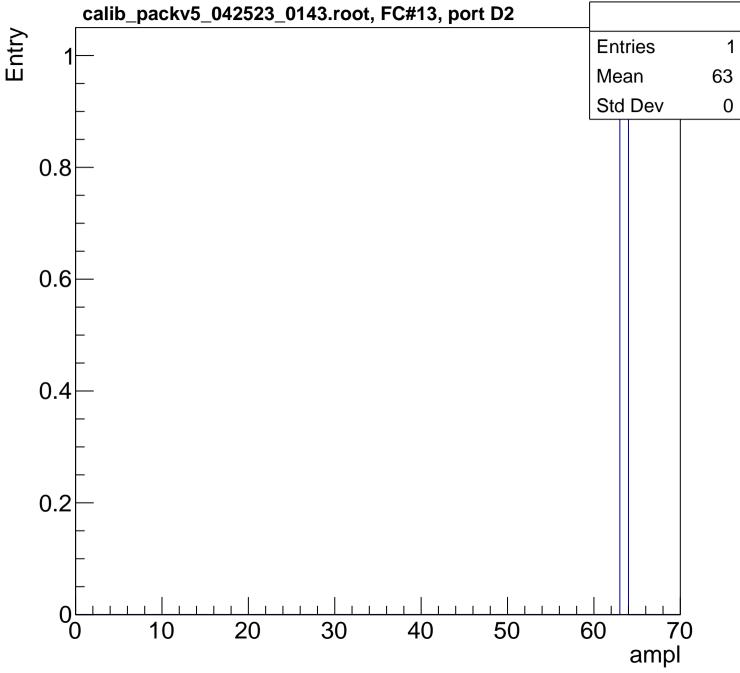




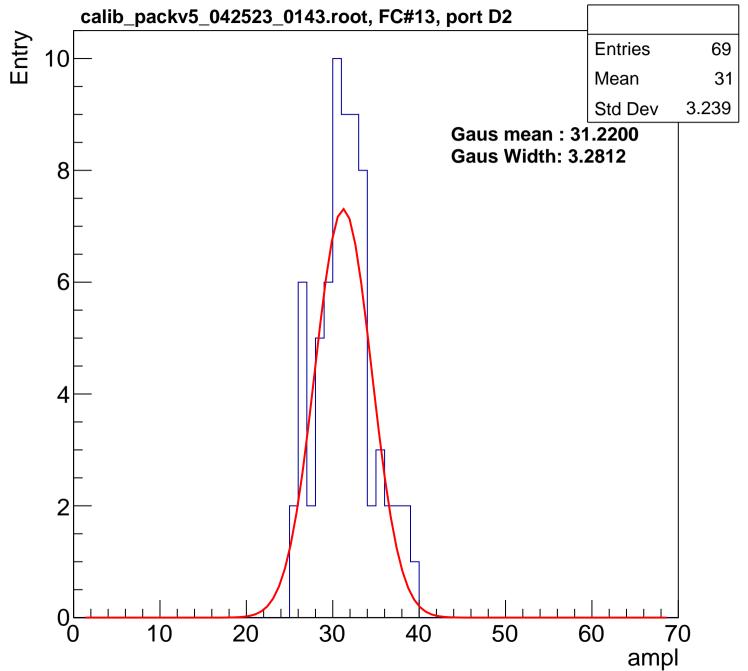


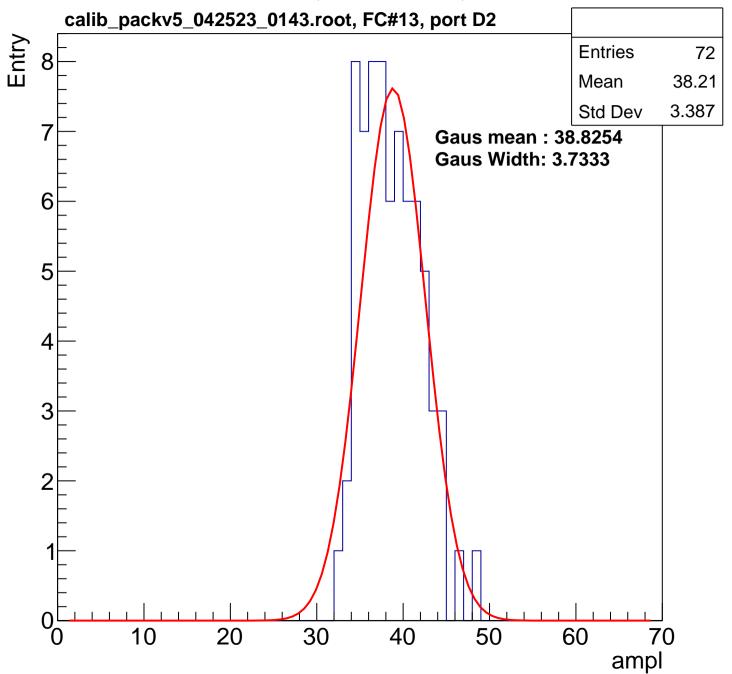


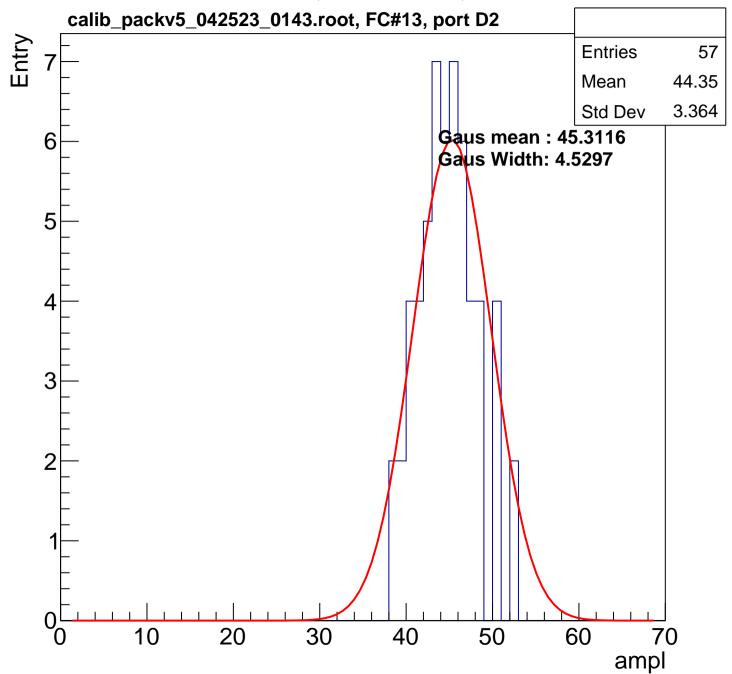


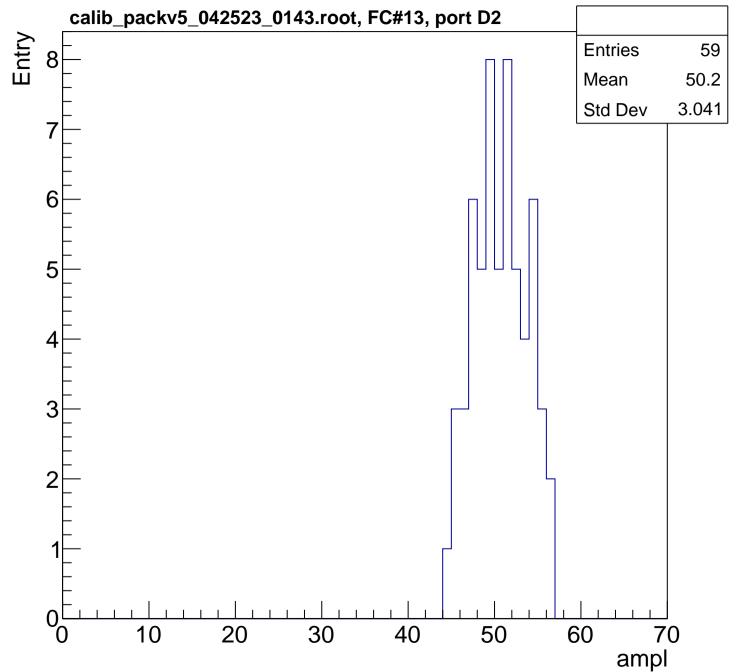


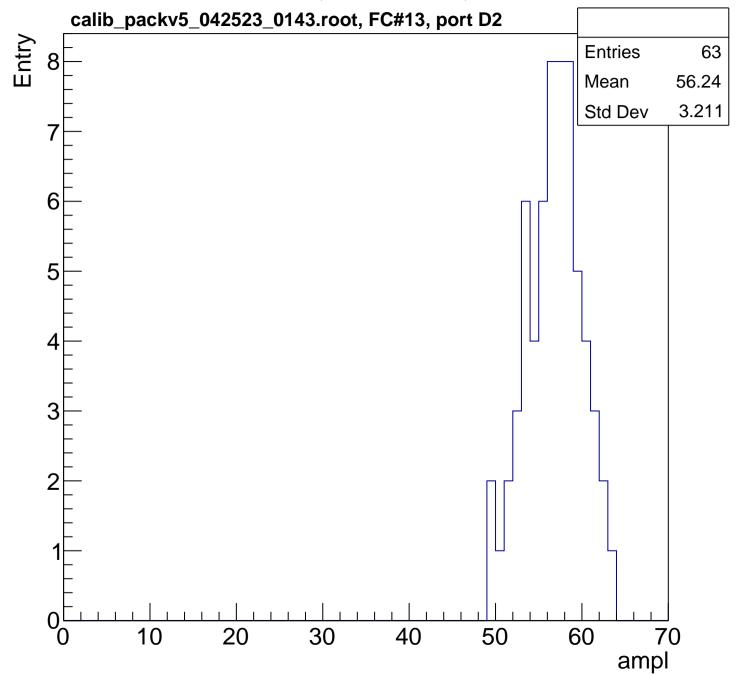
B1L003S, U2-ch23, adc7 calib_packv5_042523_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

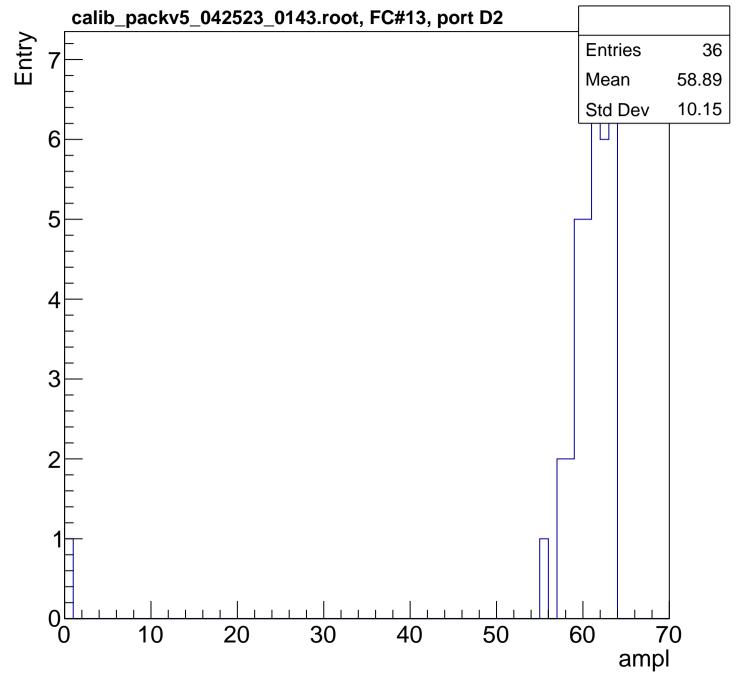


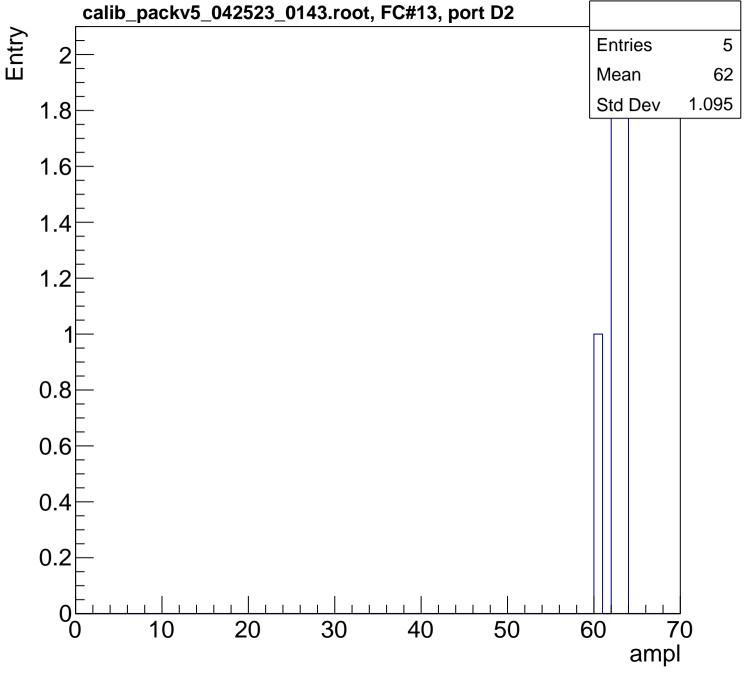


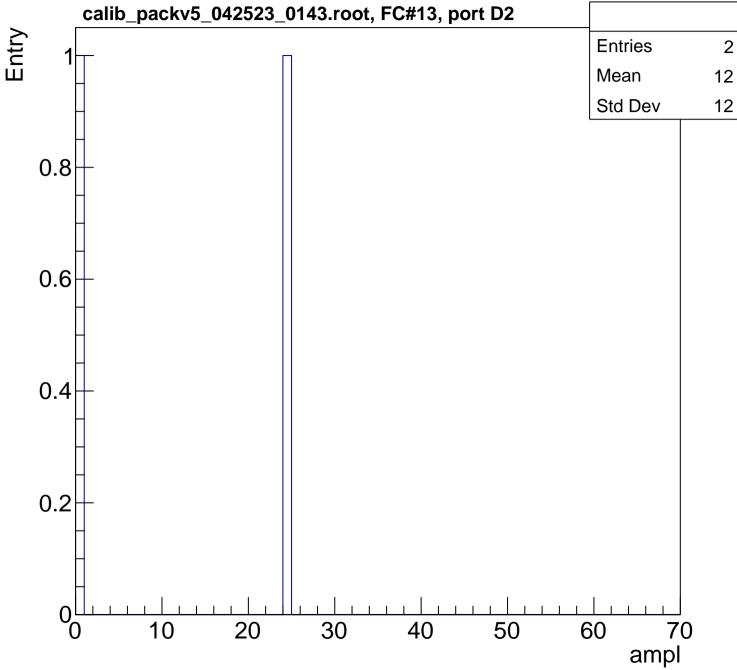


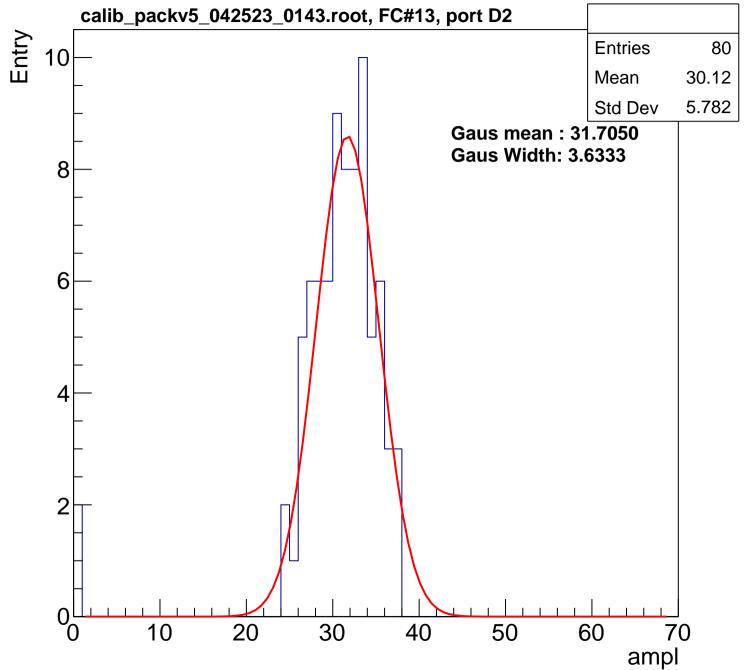


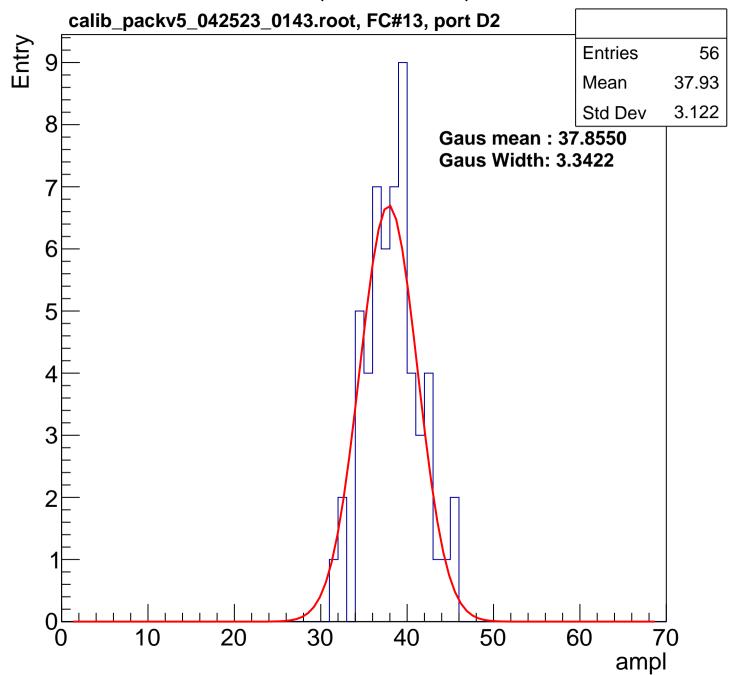


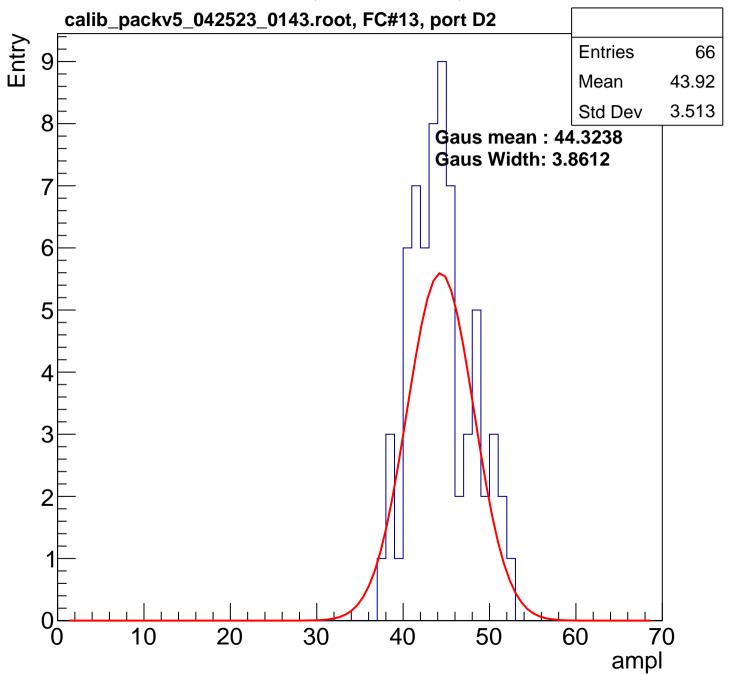


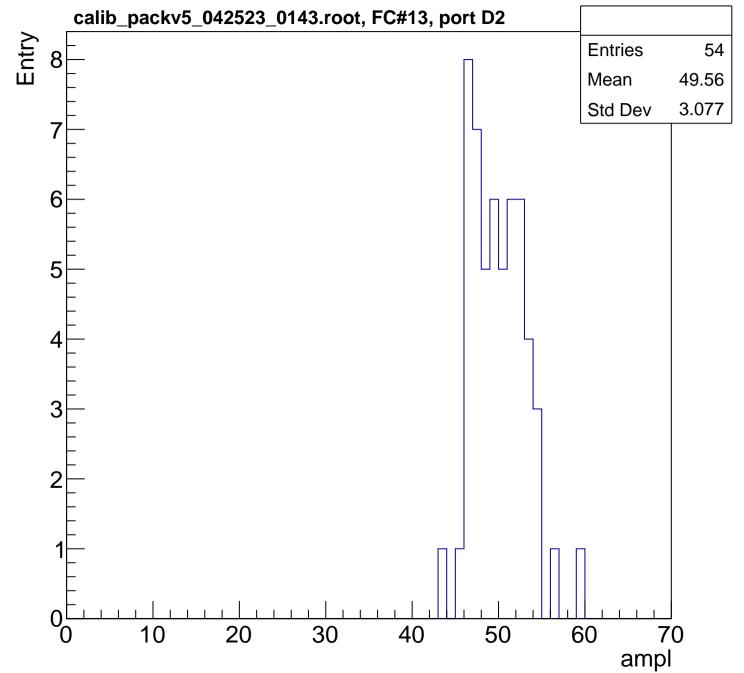


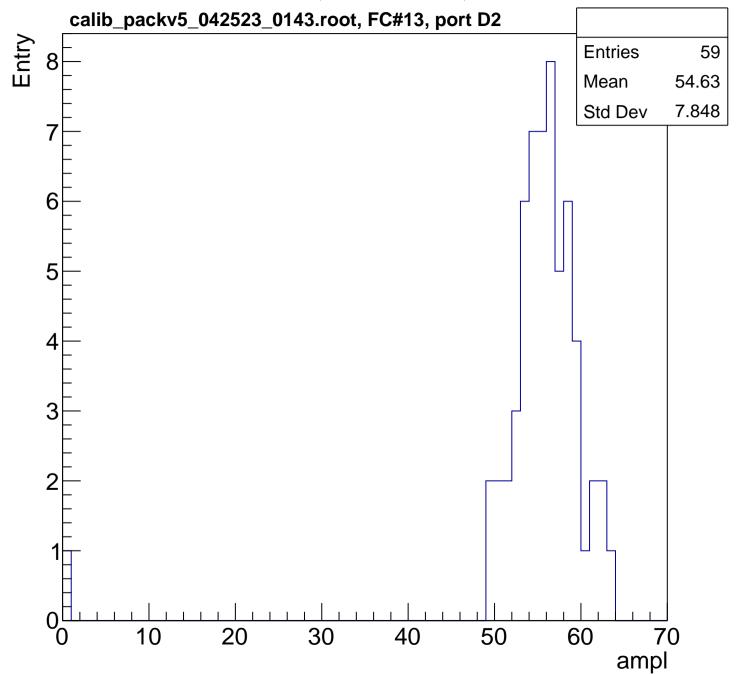


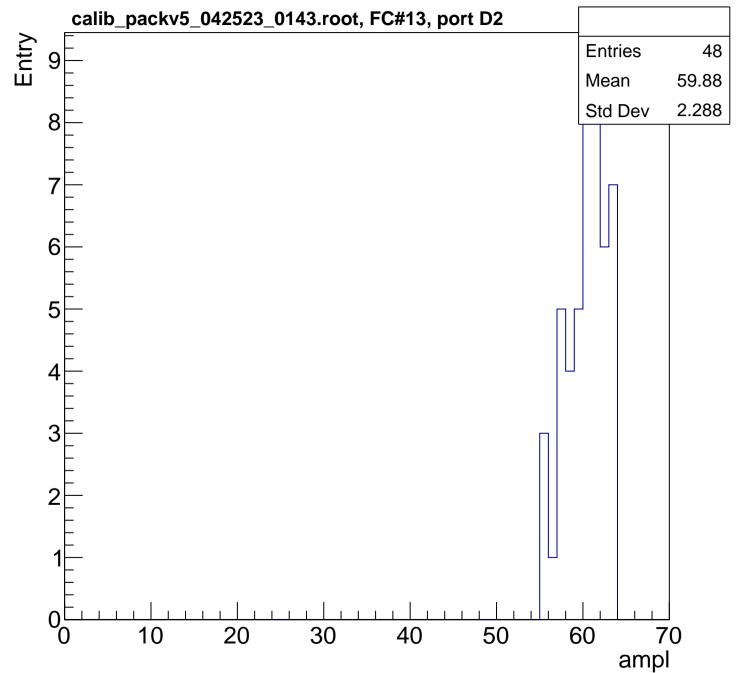


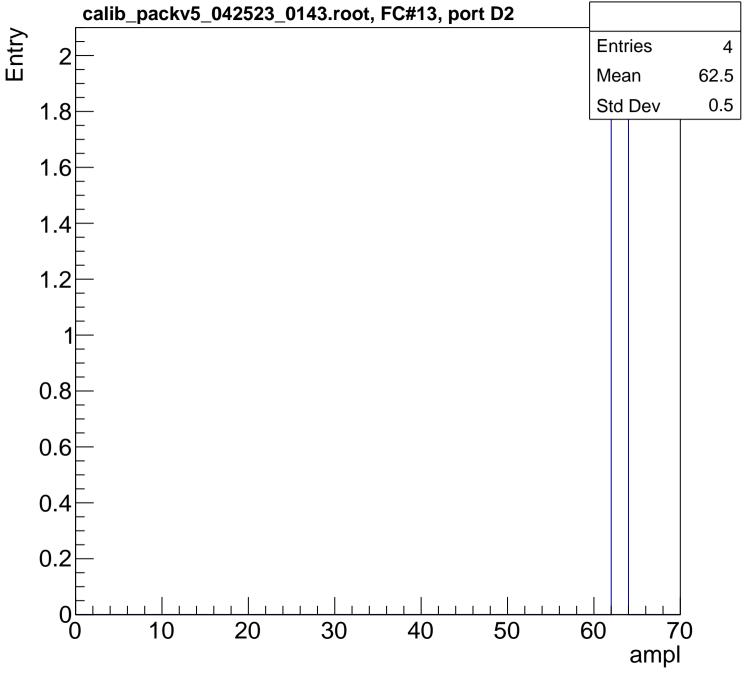




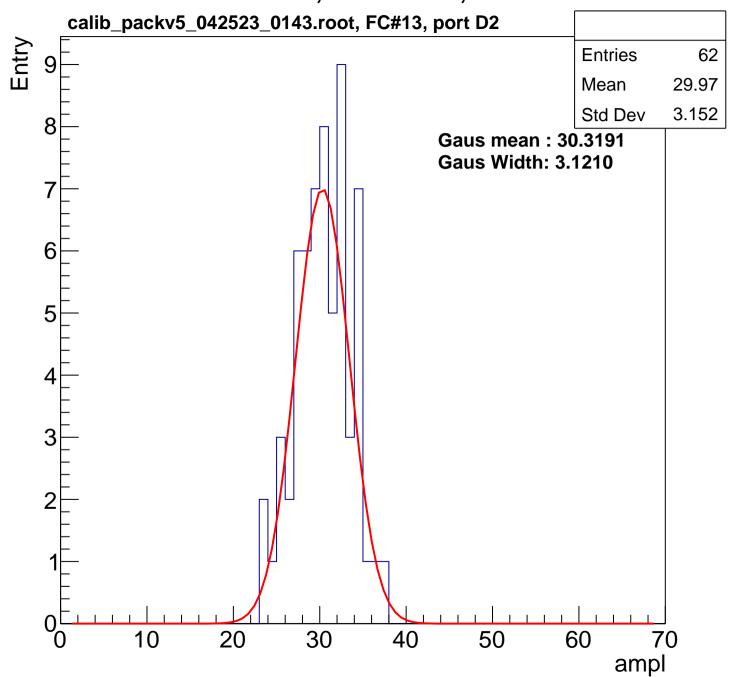


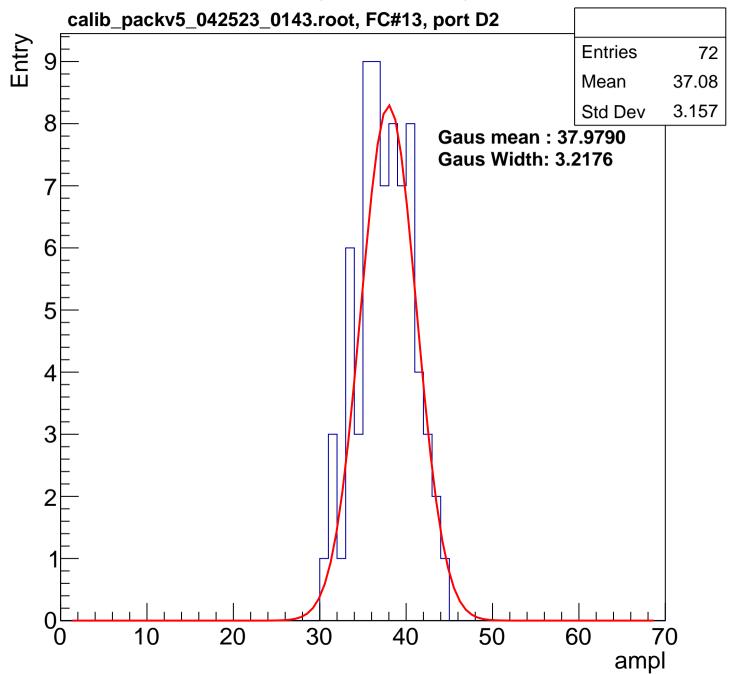


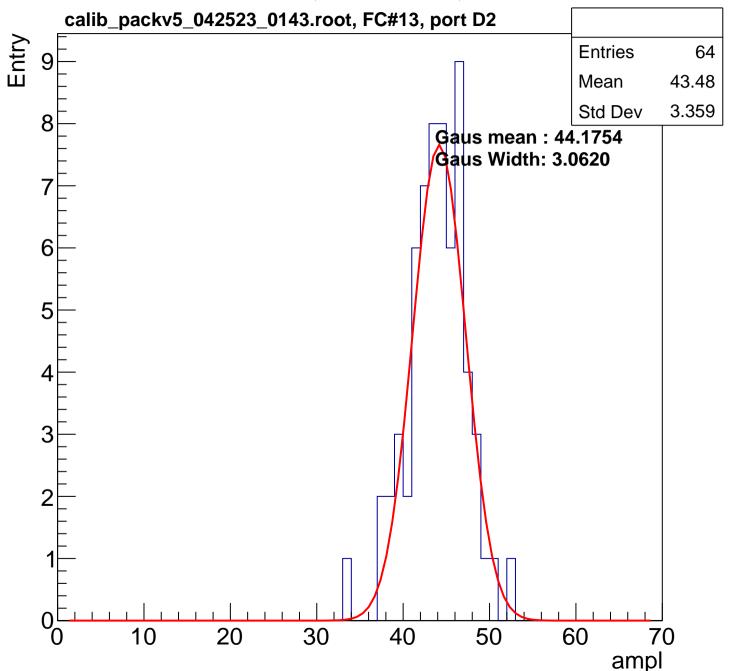


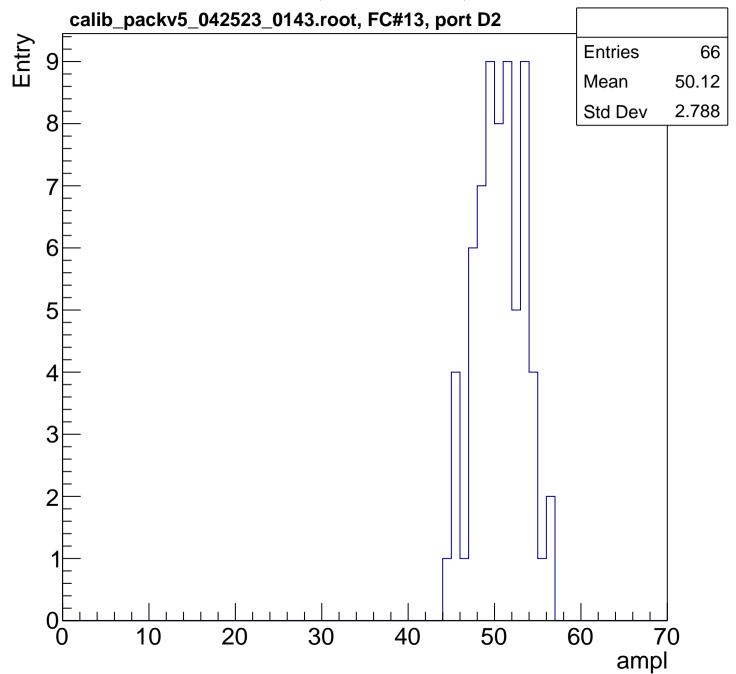


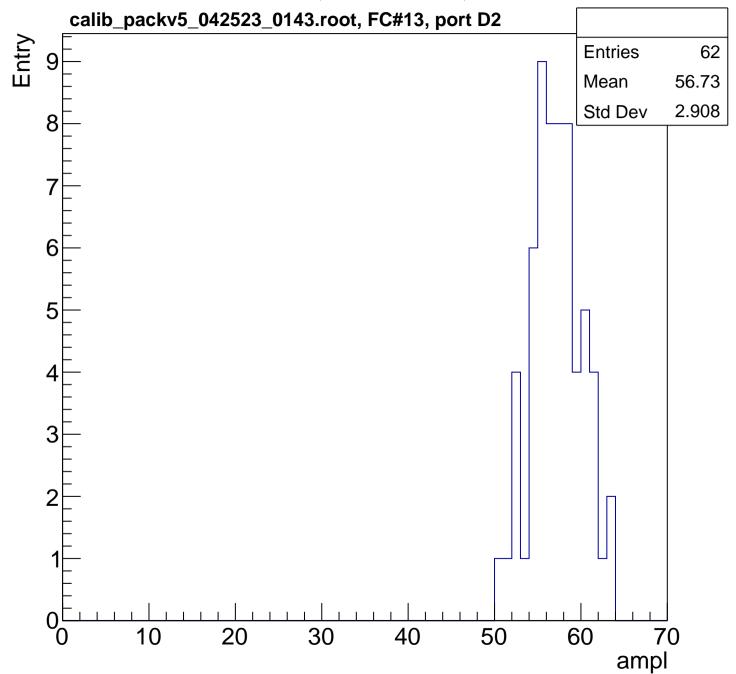


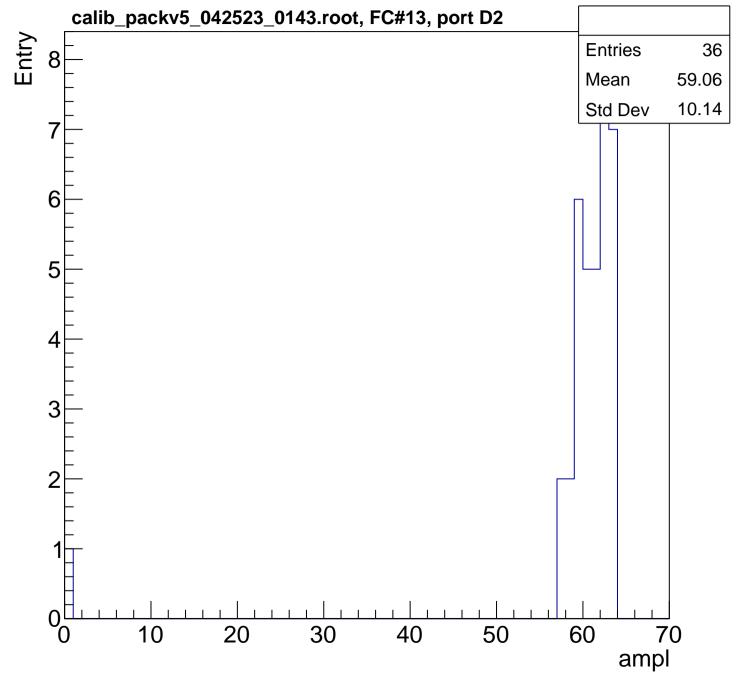


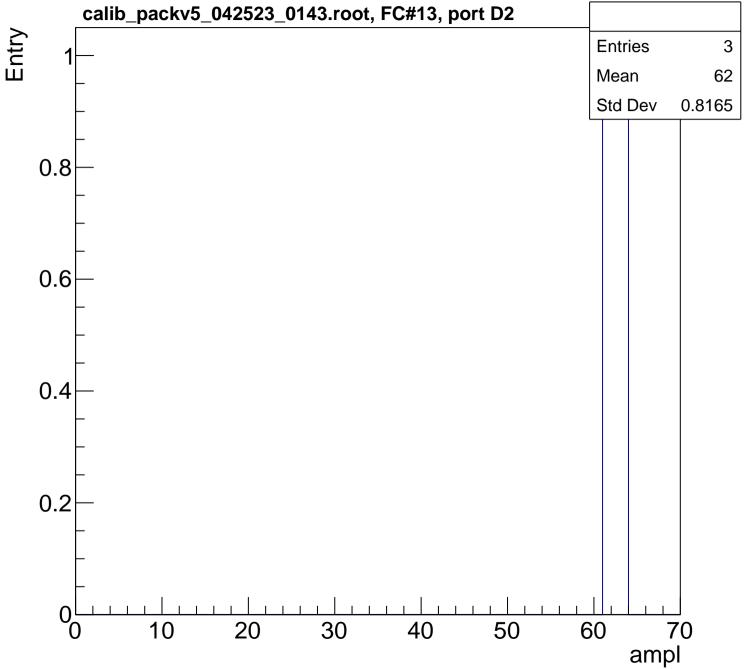




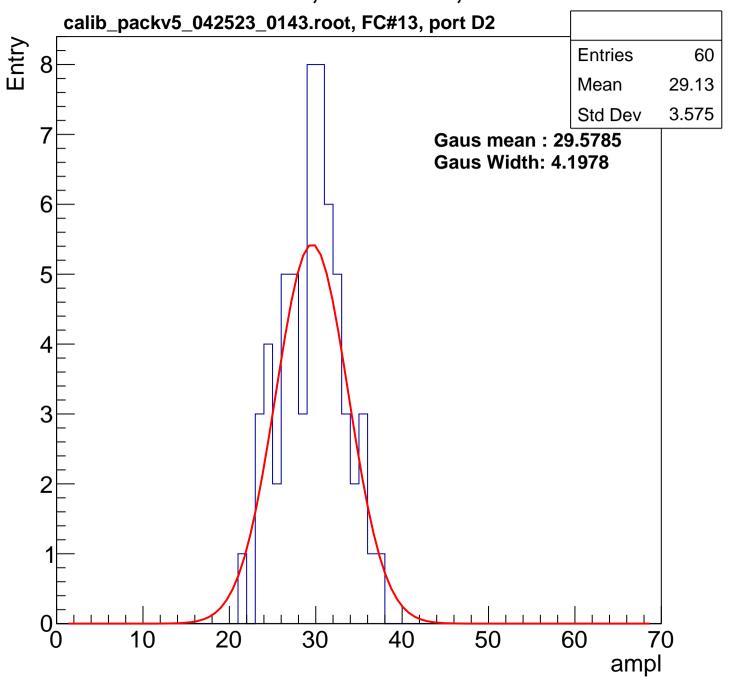


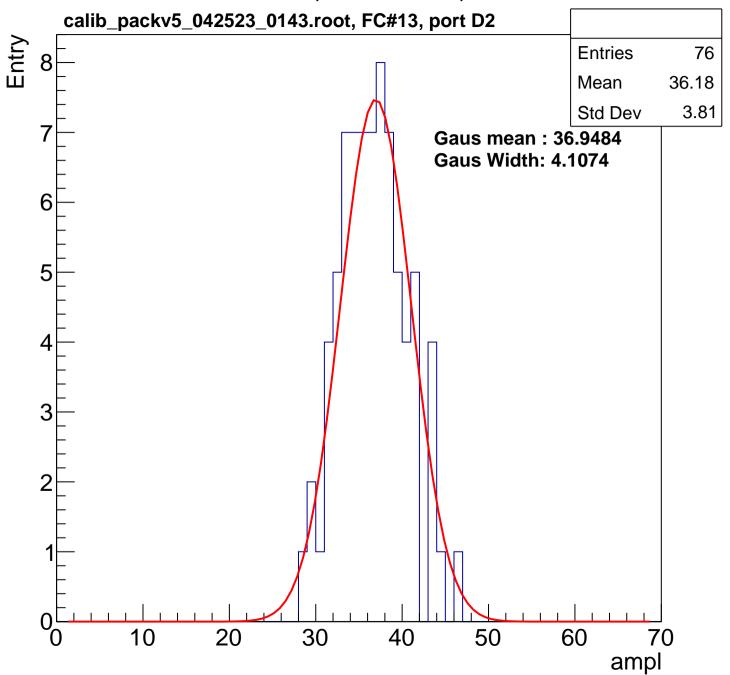


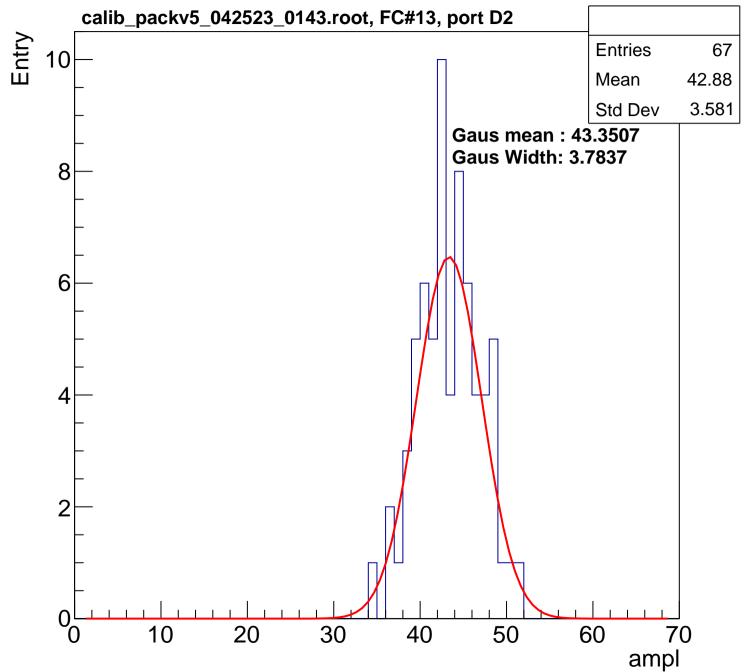


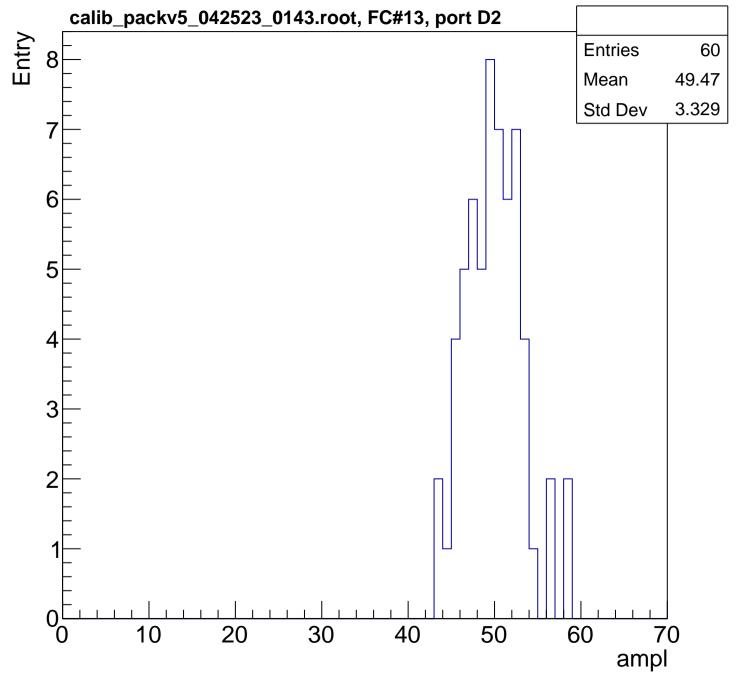


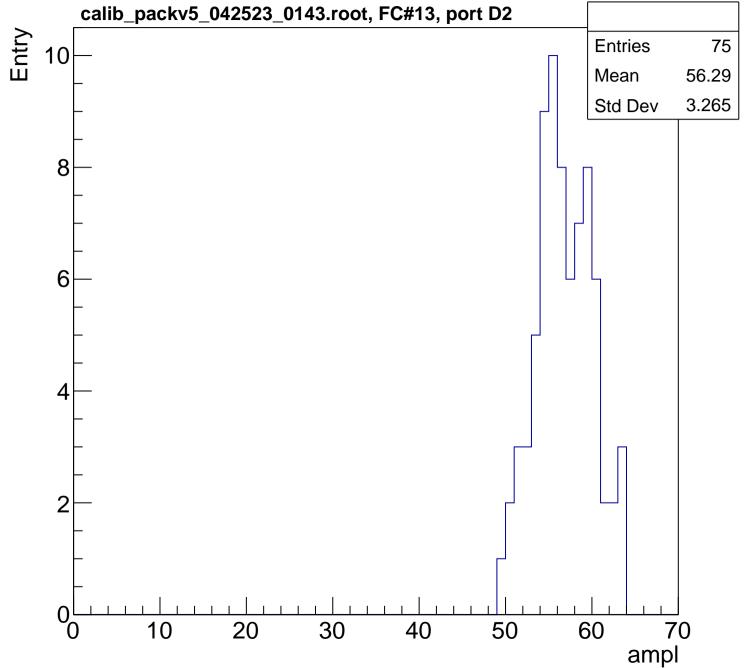


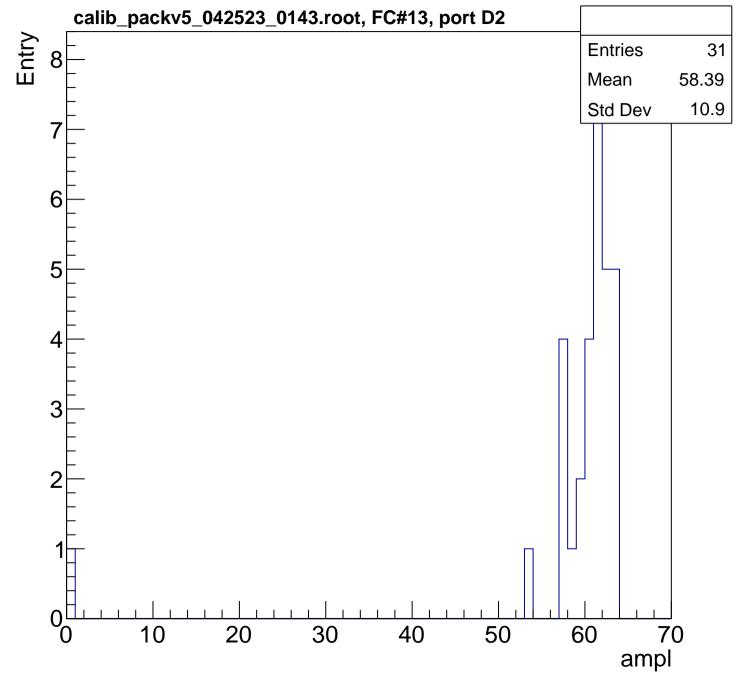


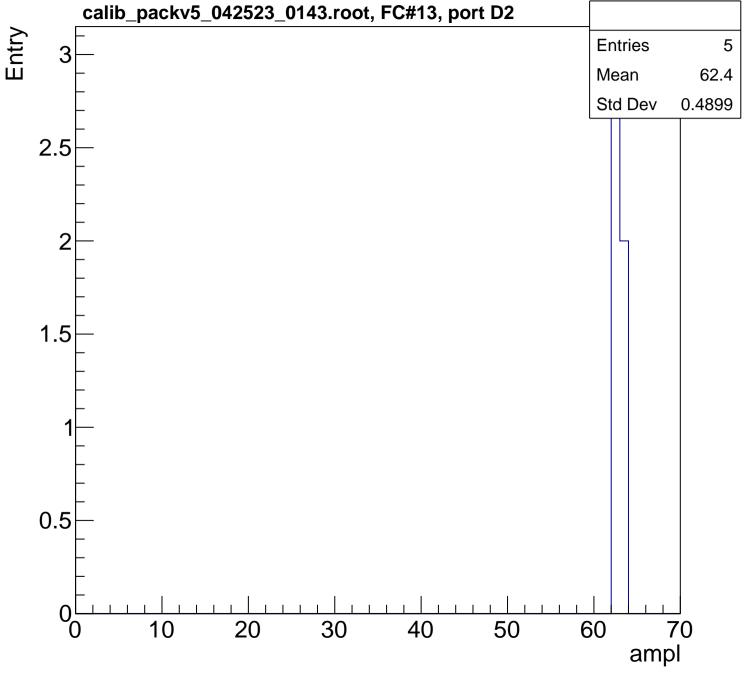


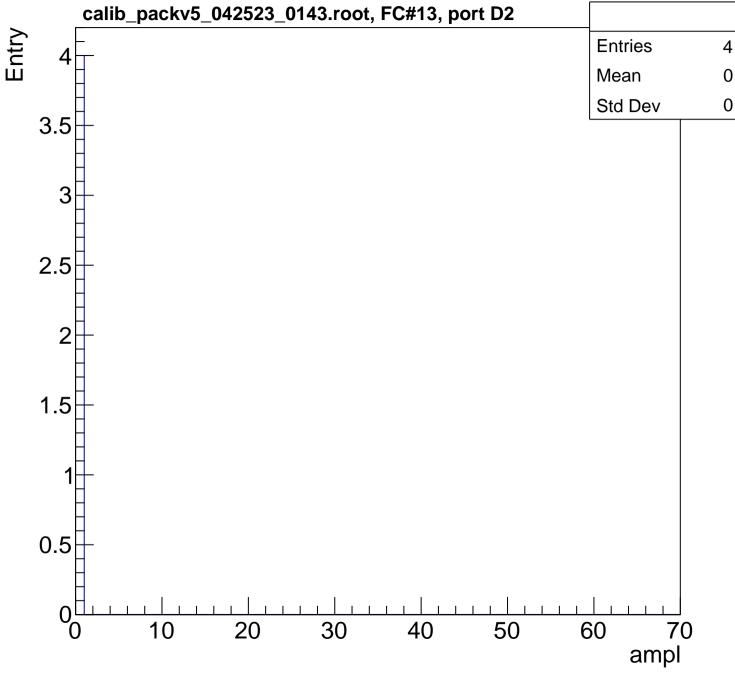


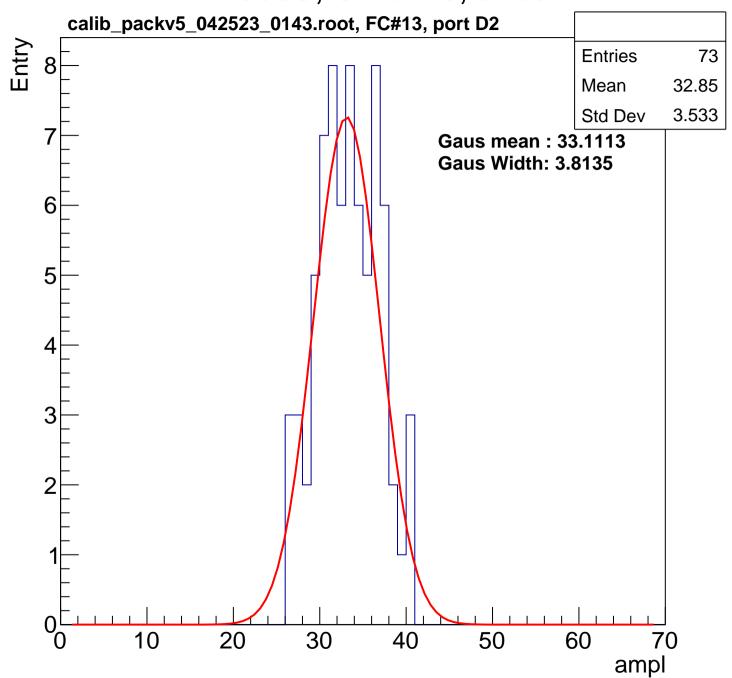


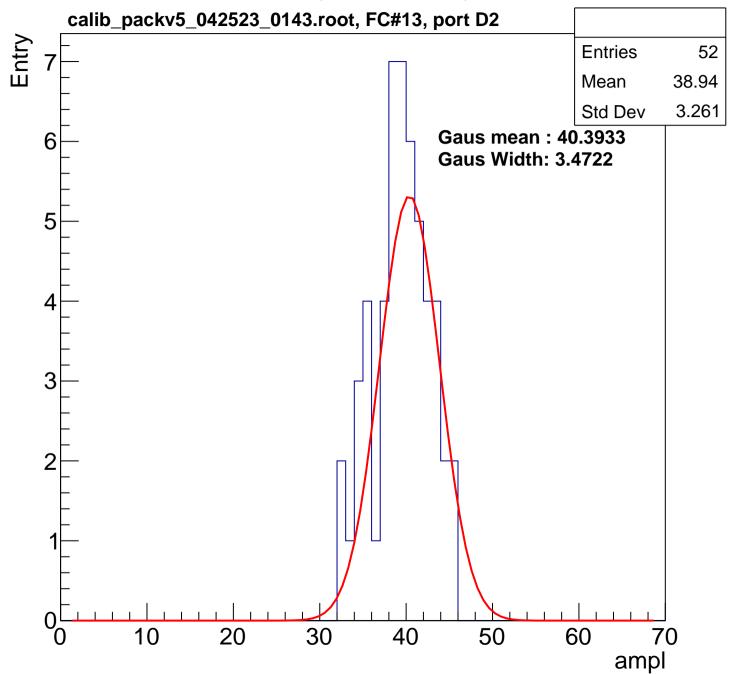


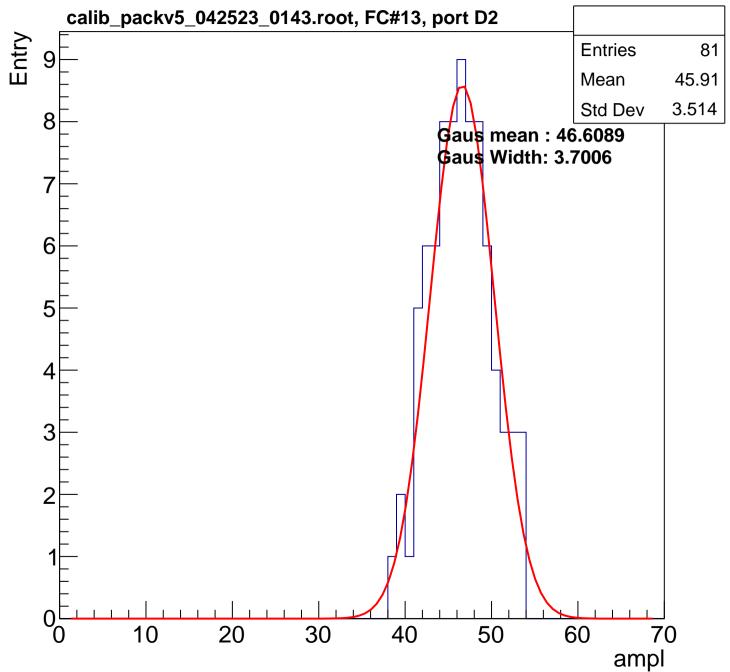


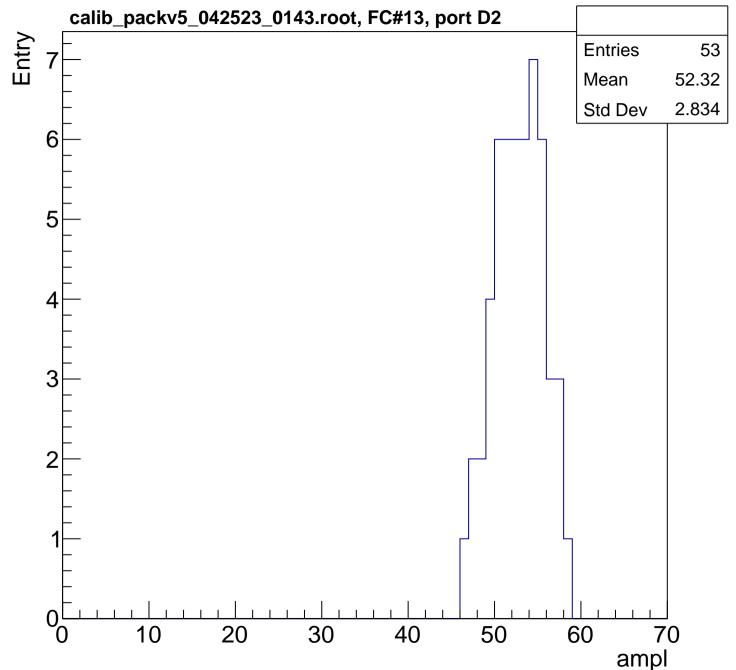


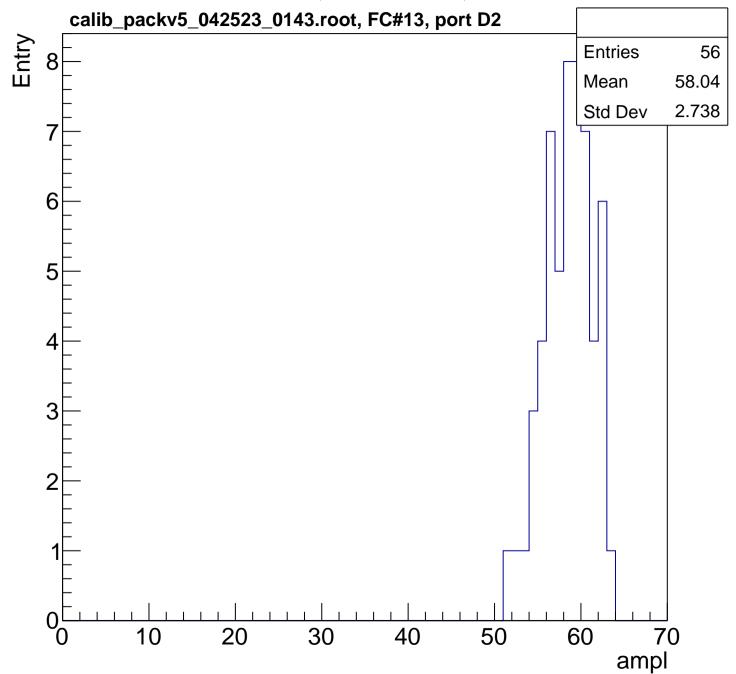


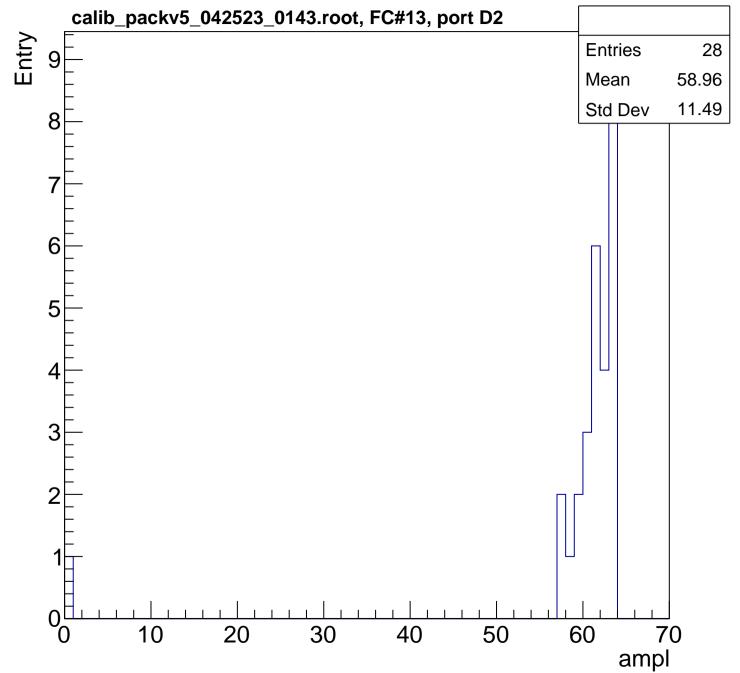


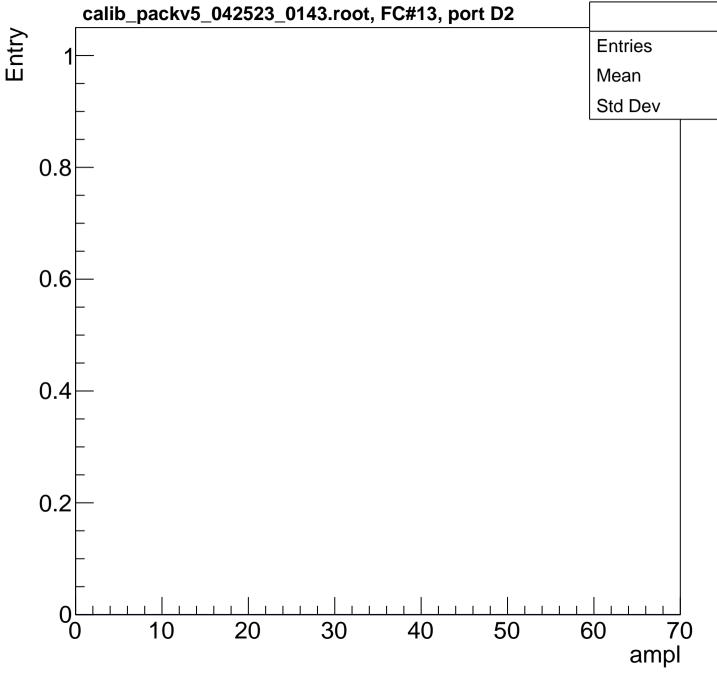




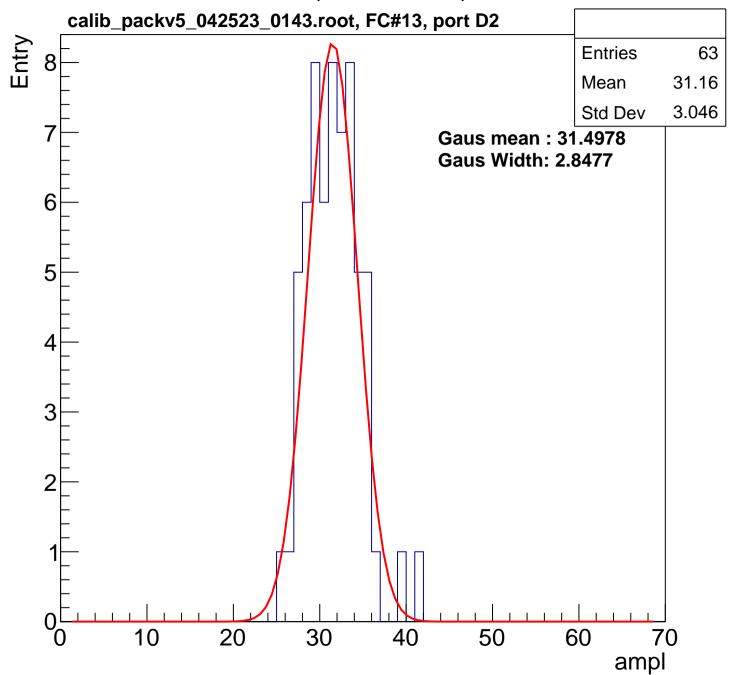


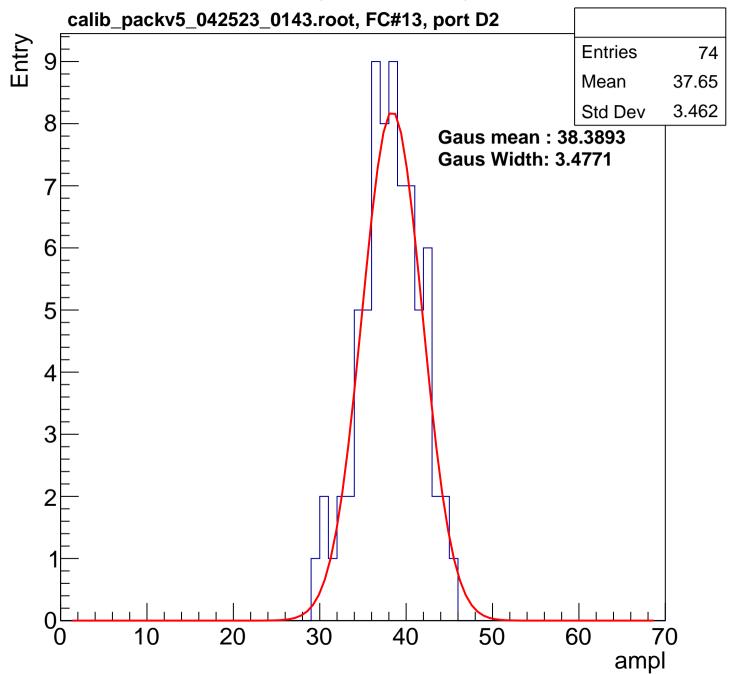


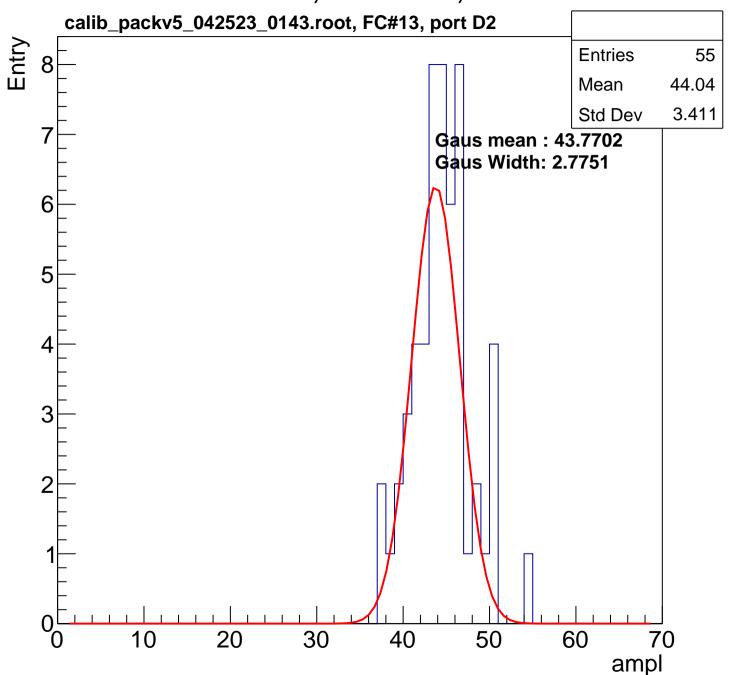


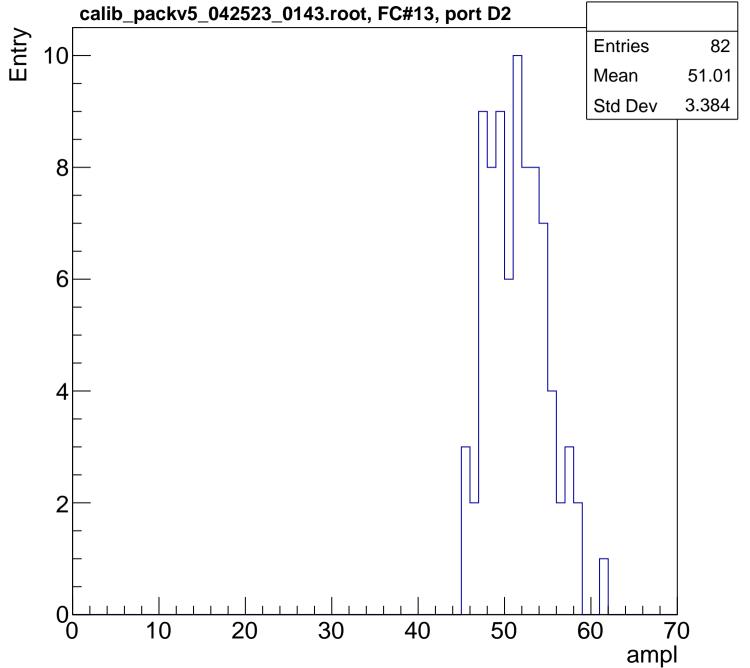


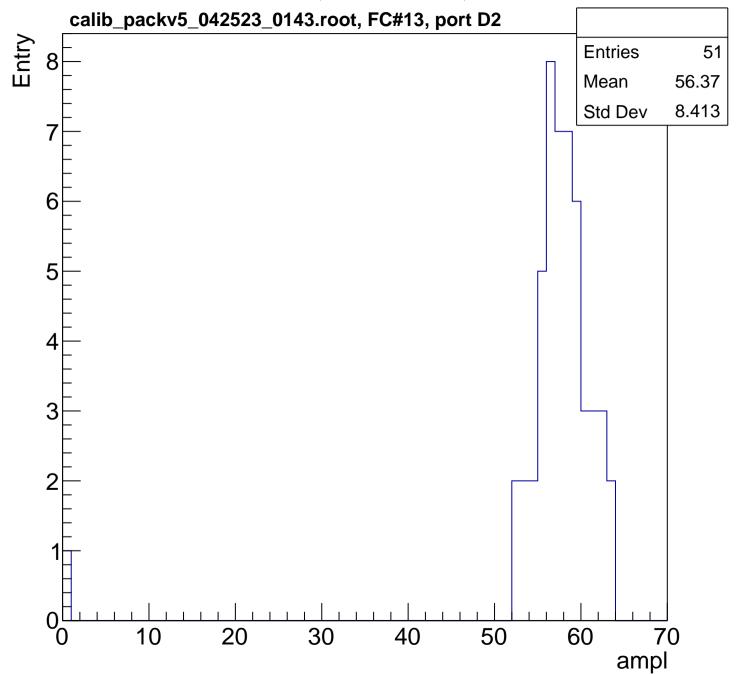


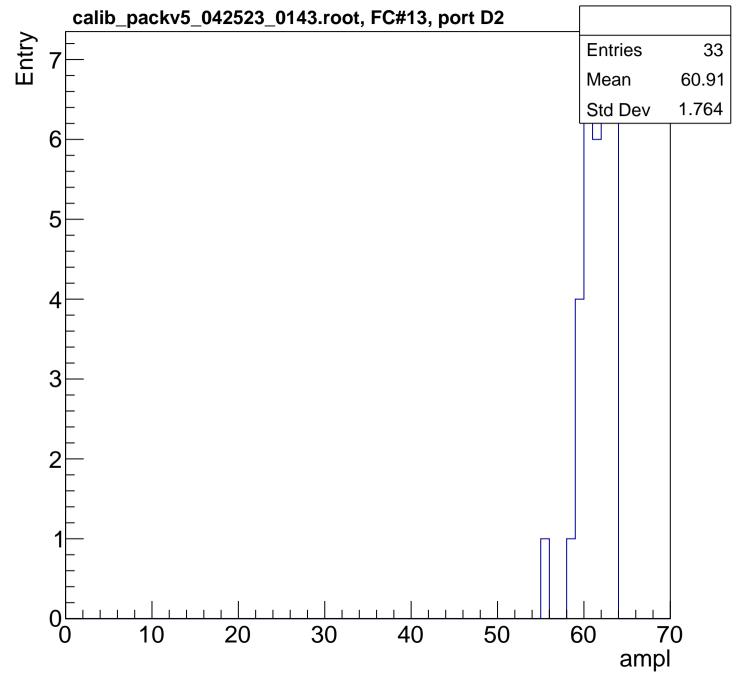


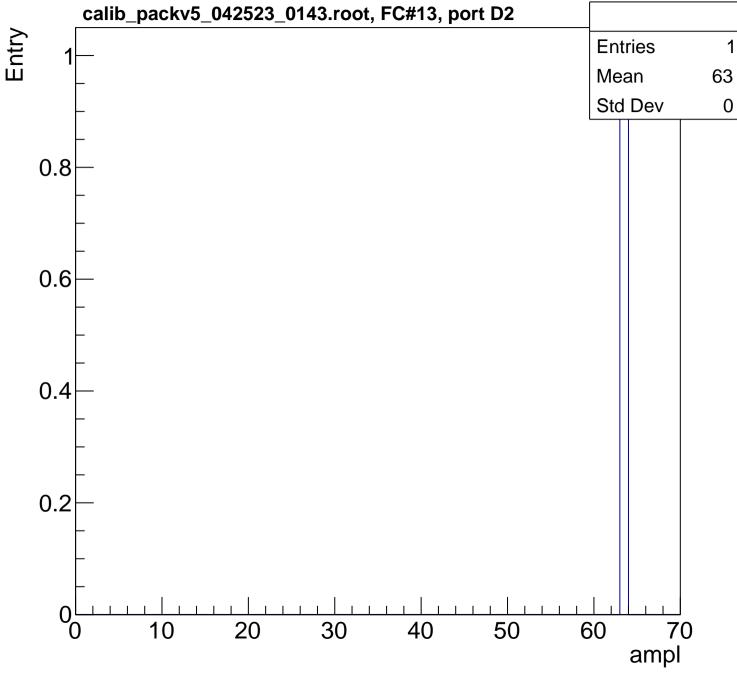


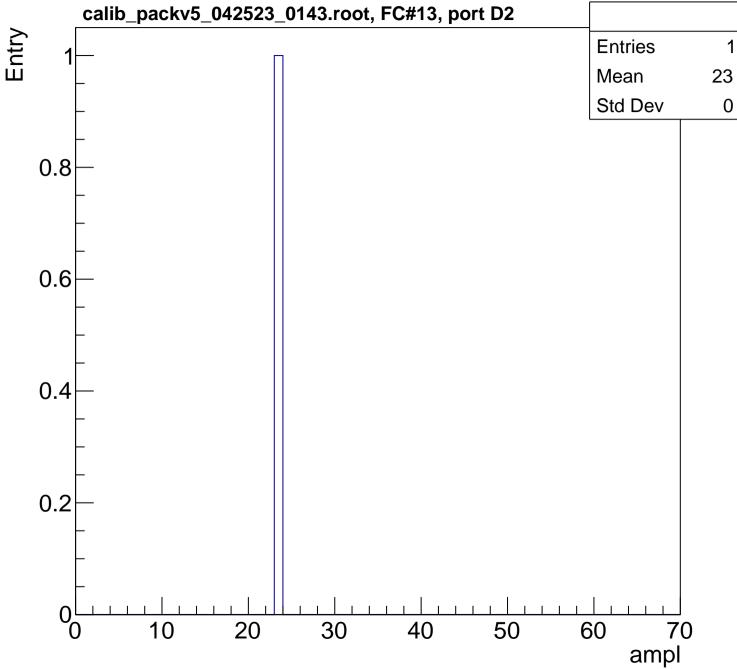


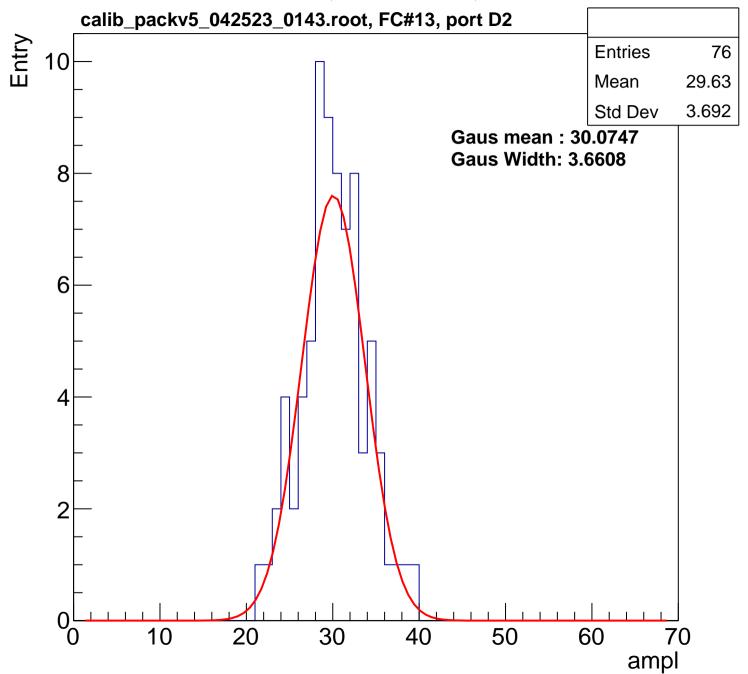


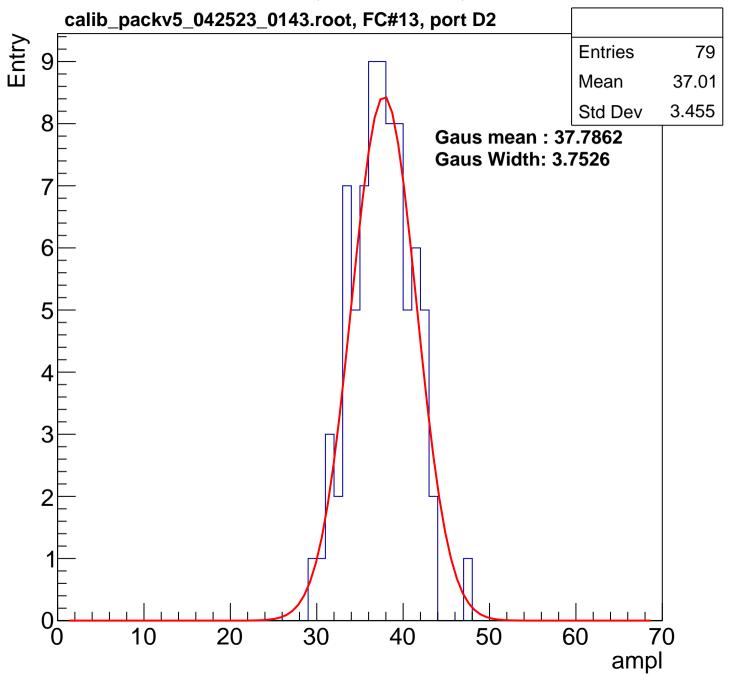


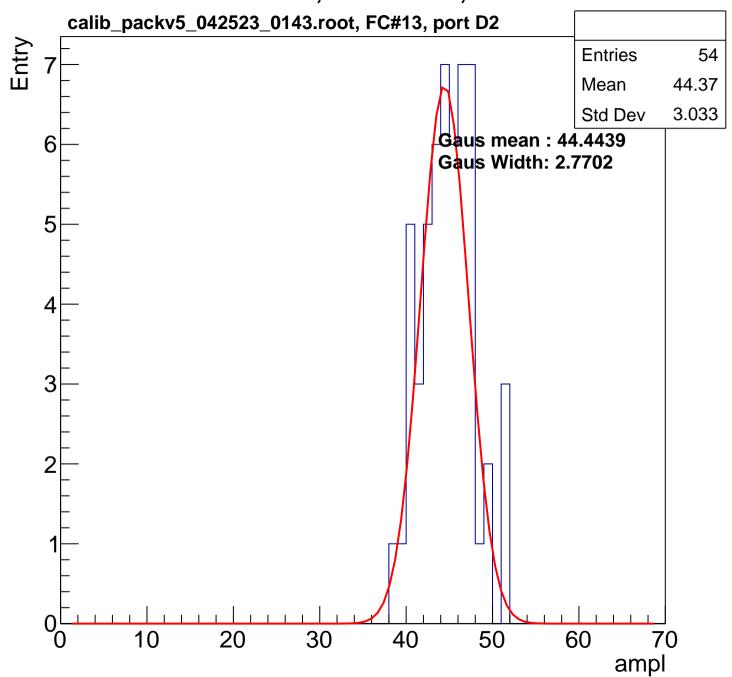


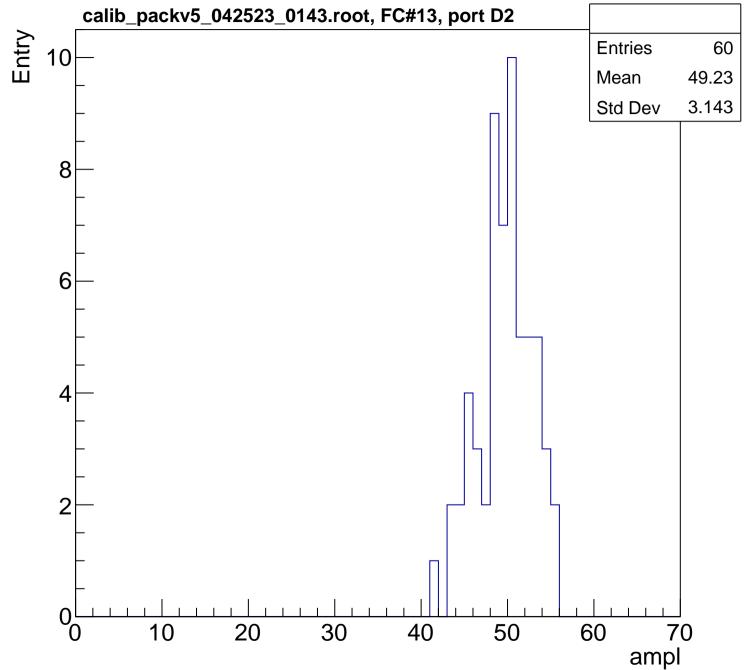


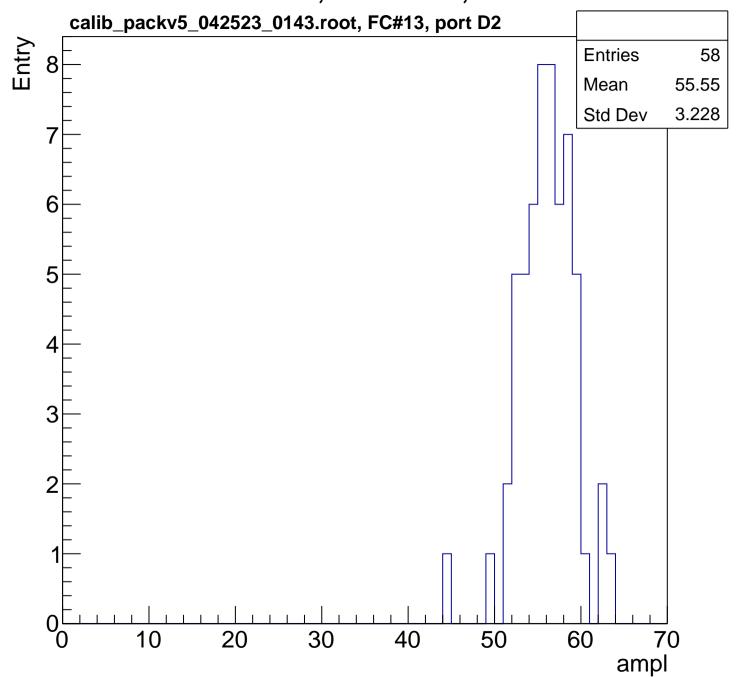


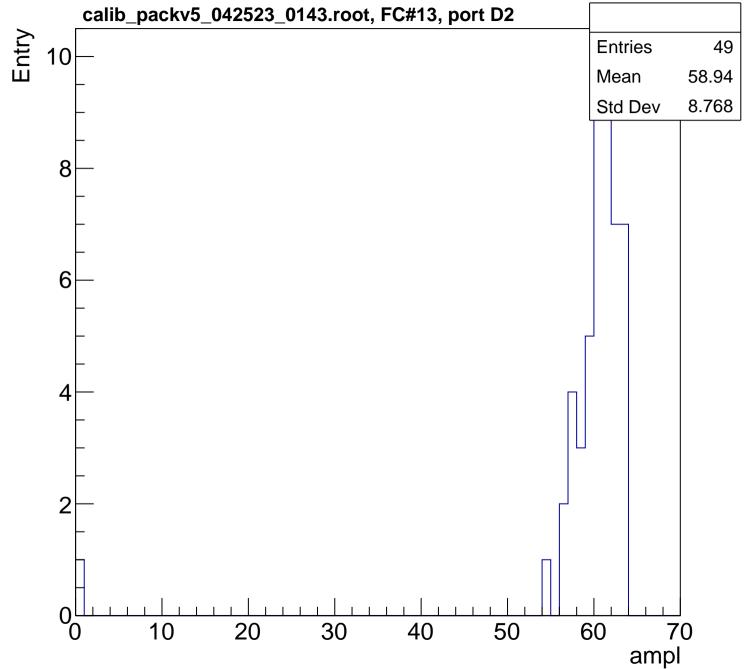


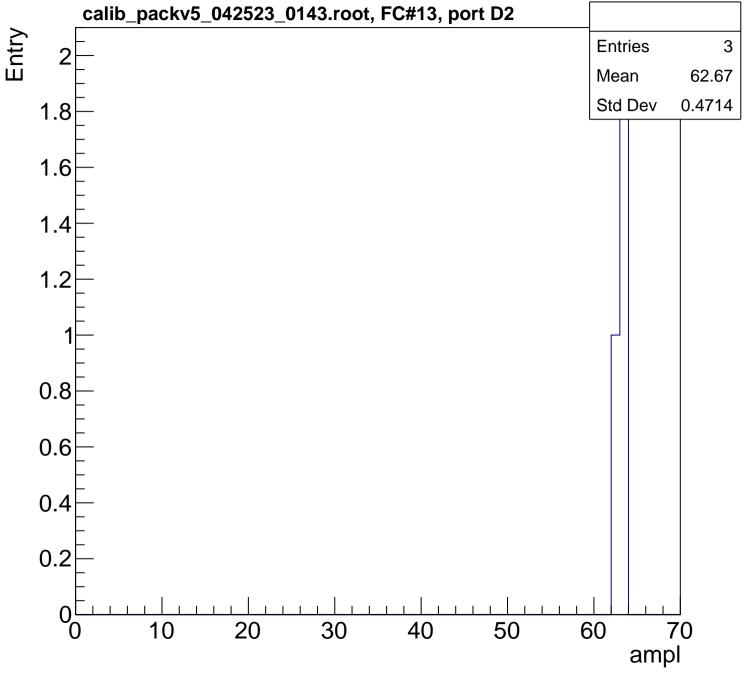




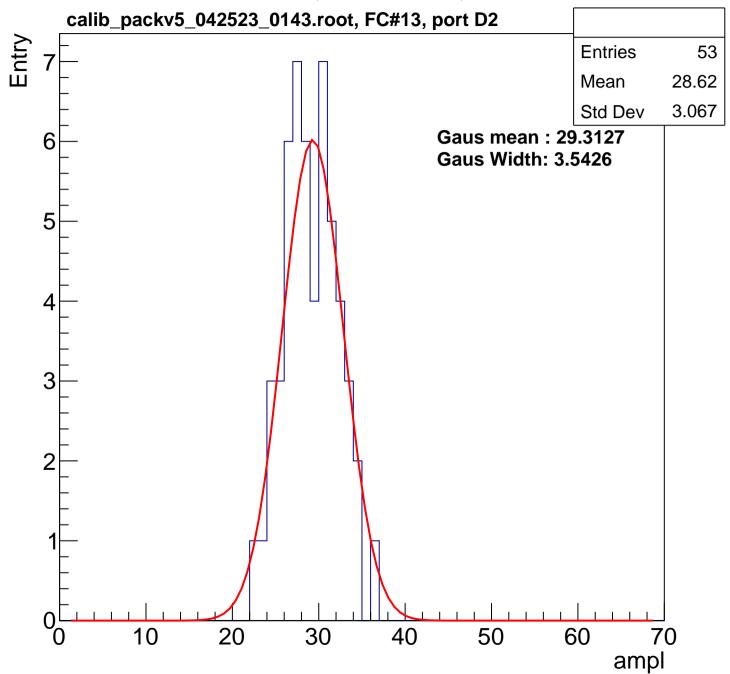


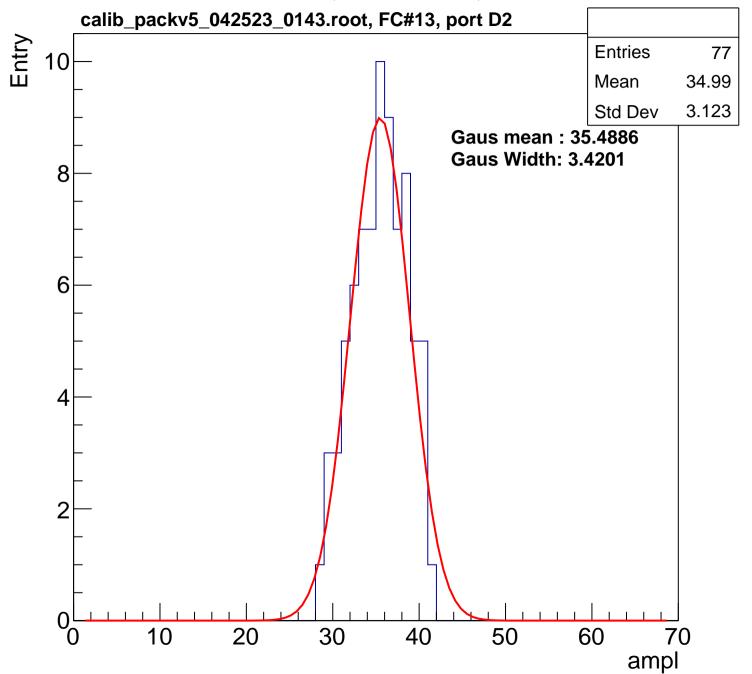


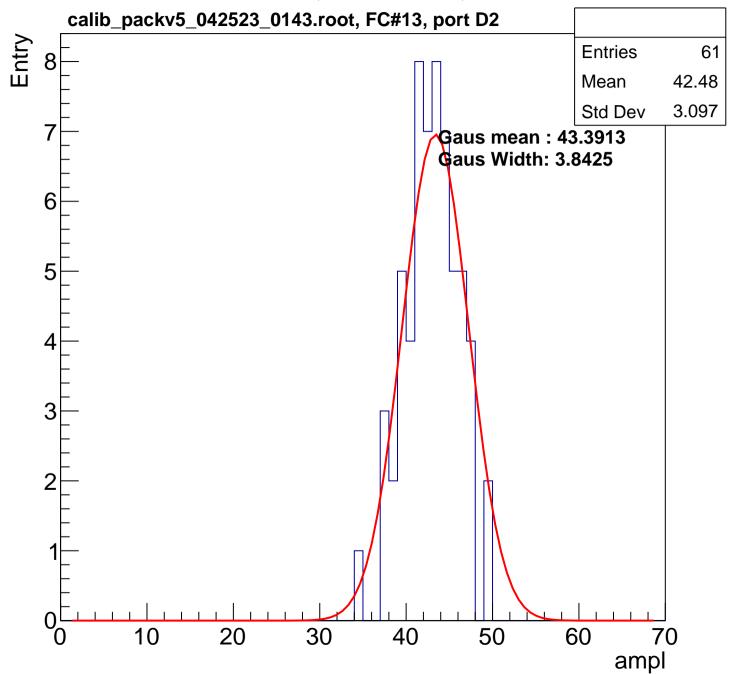


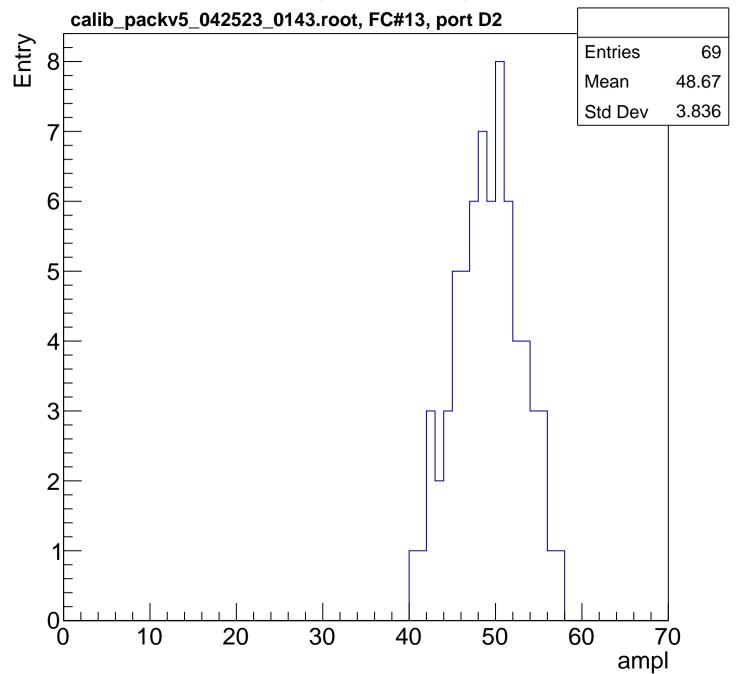


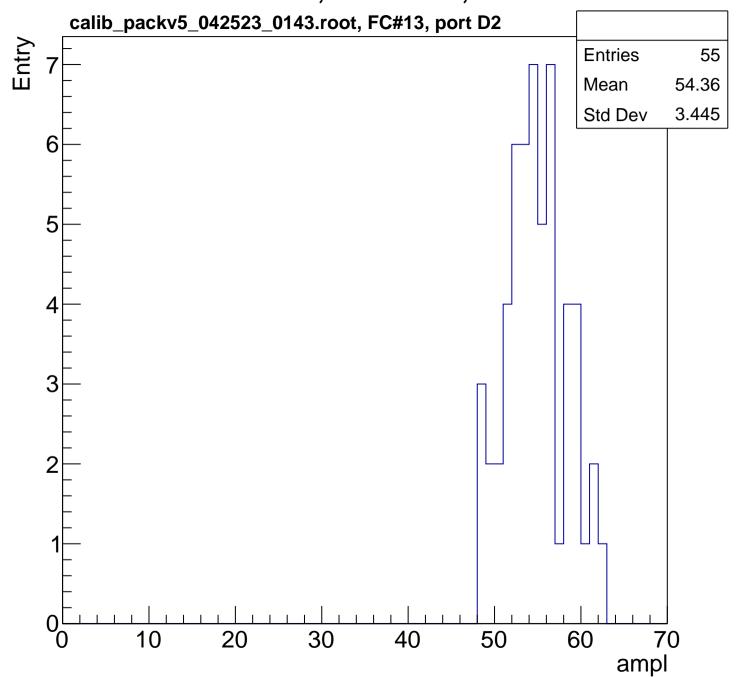
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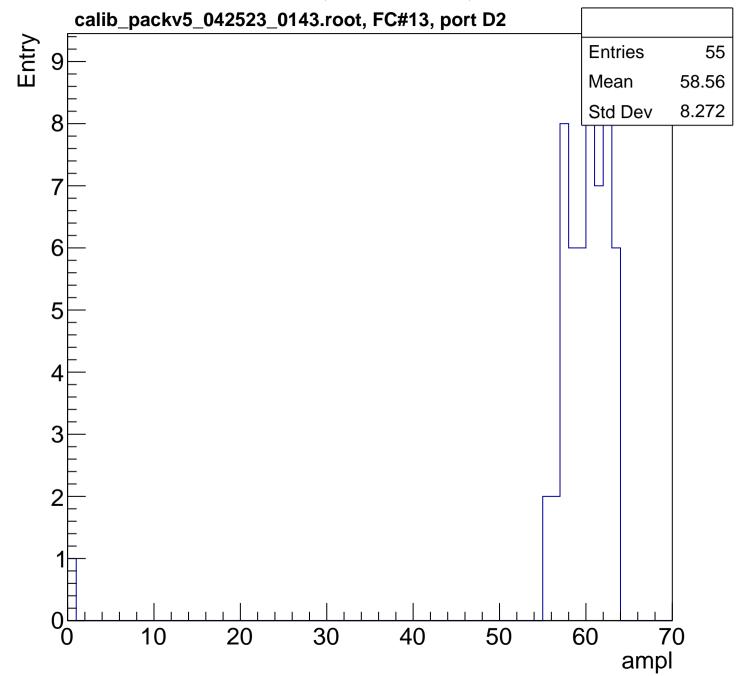


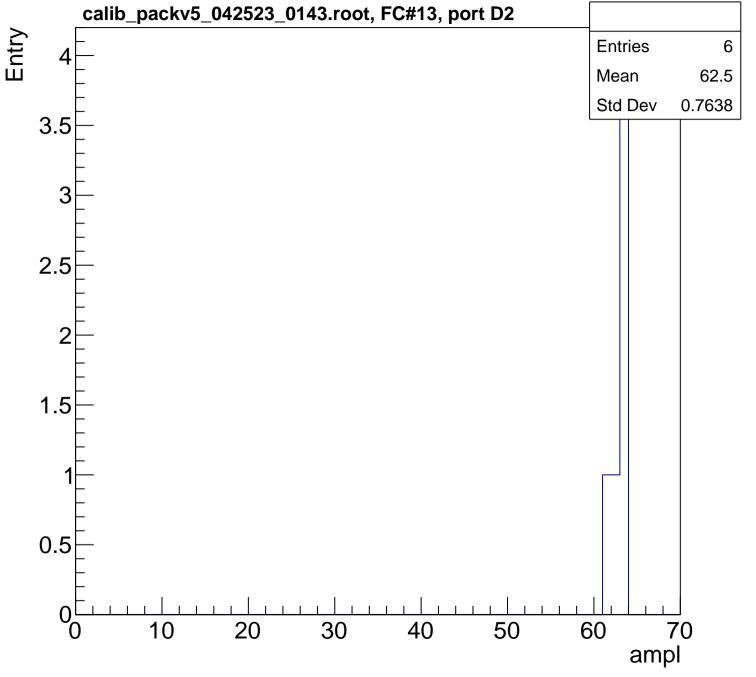




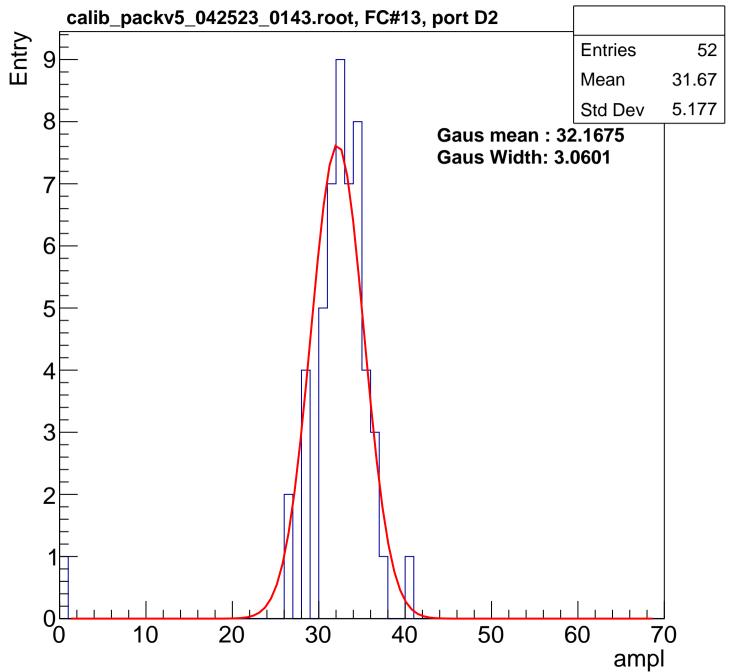


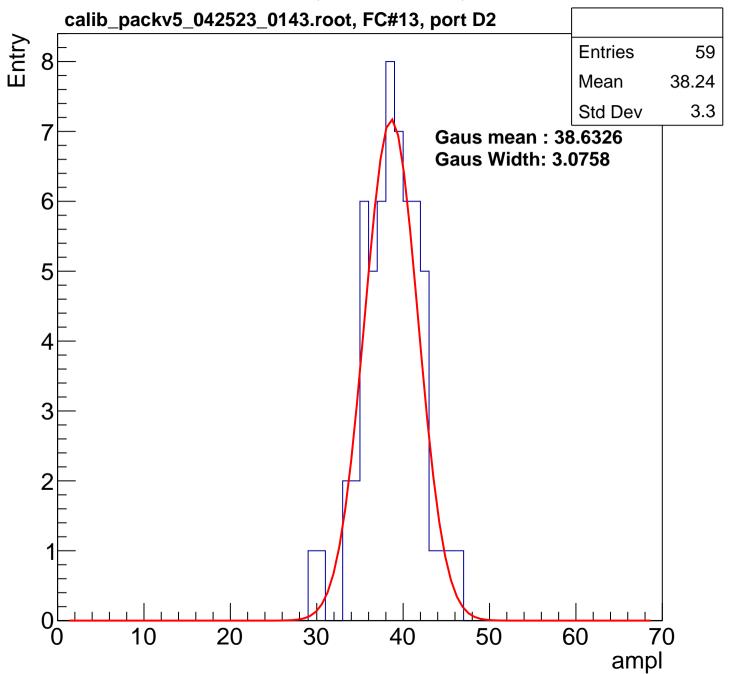


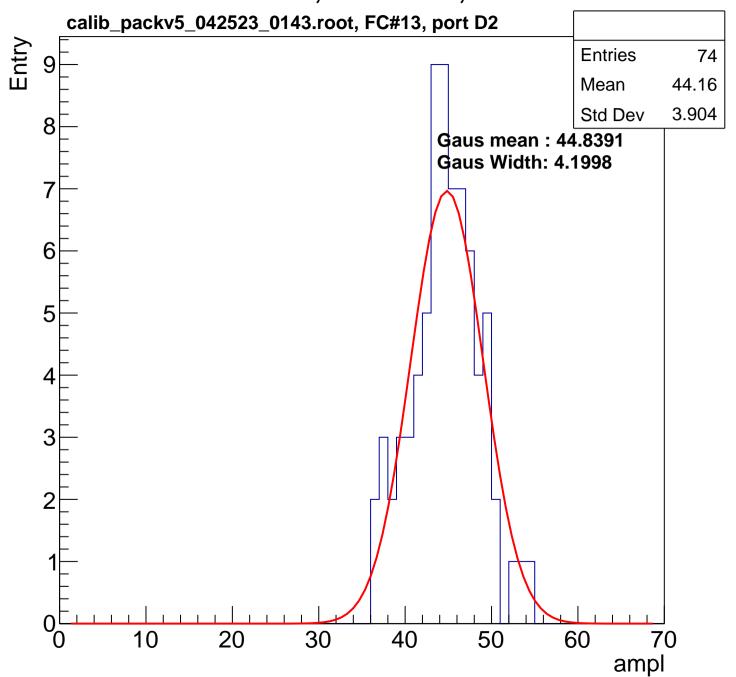


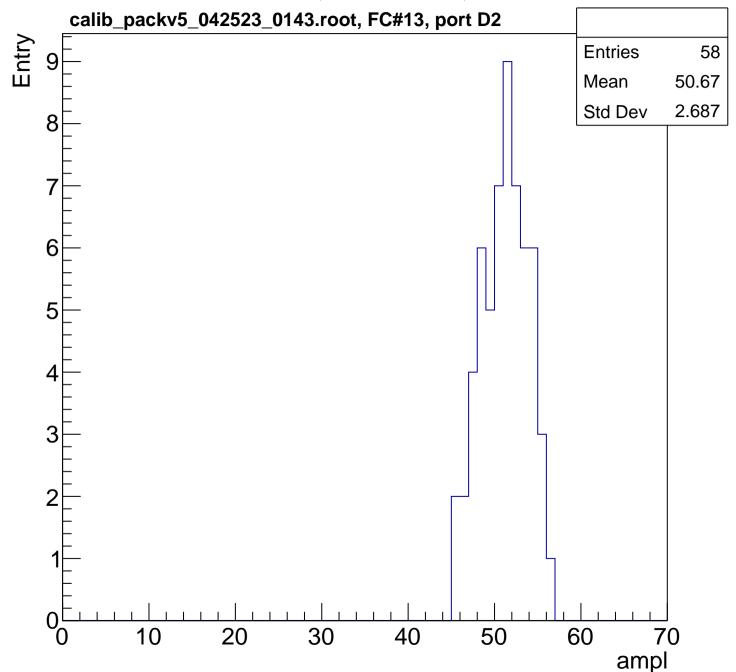


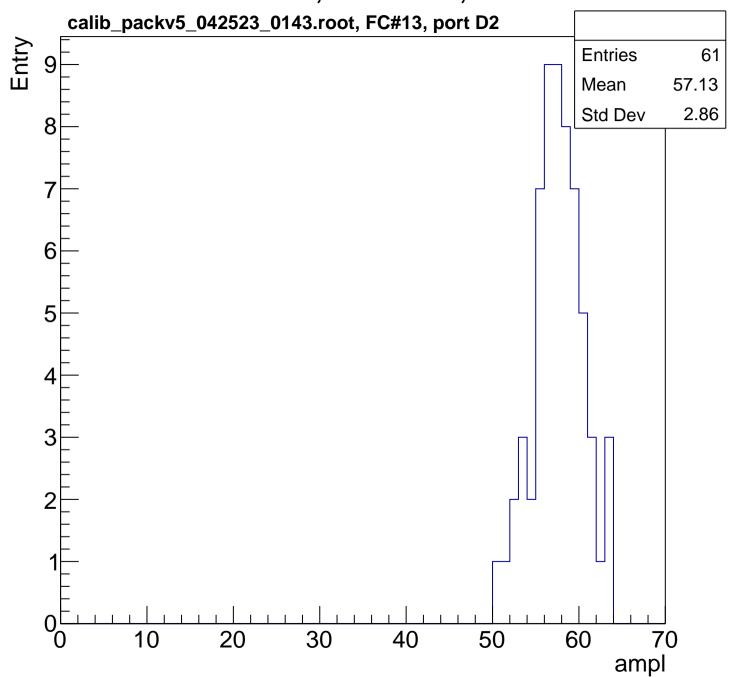
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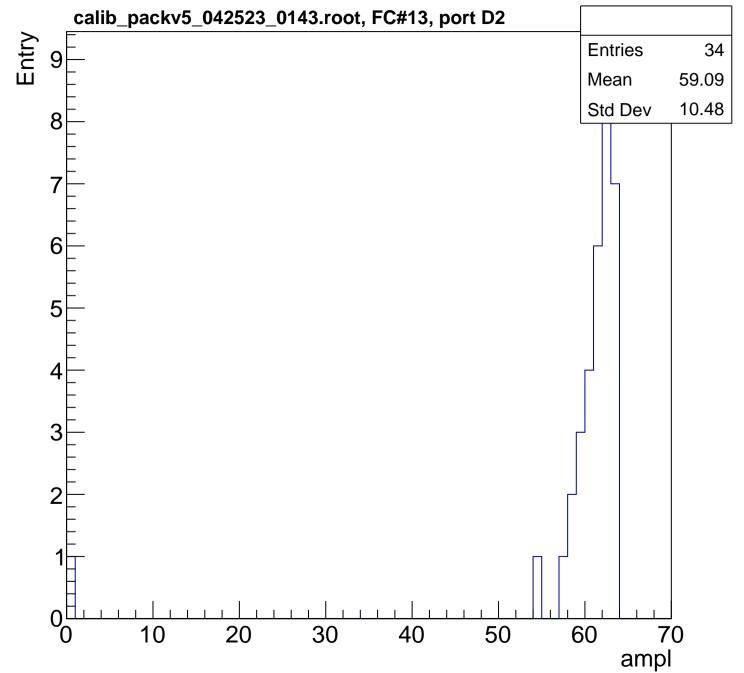


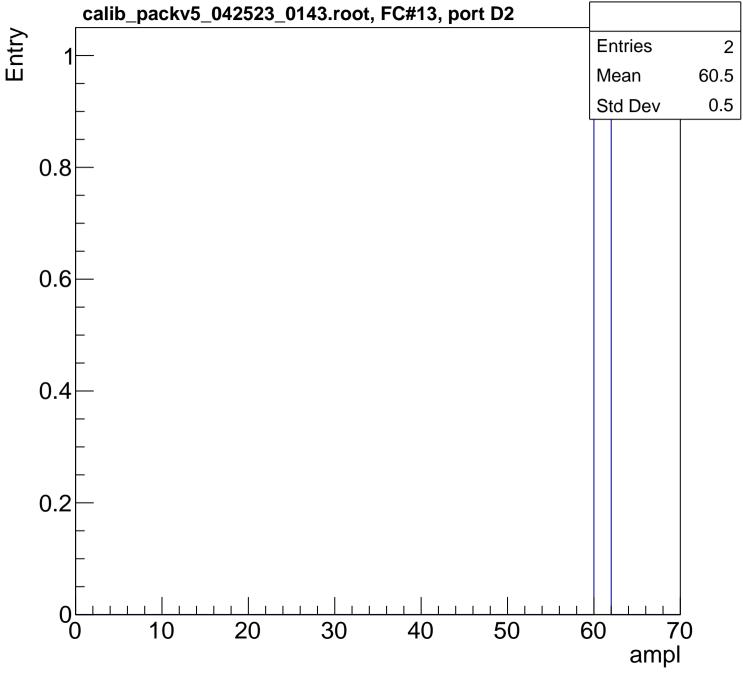




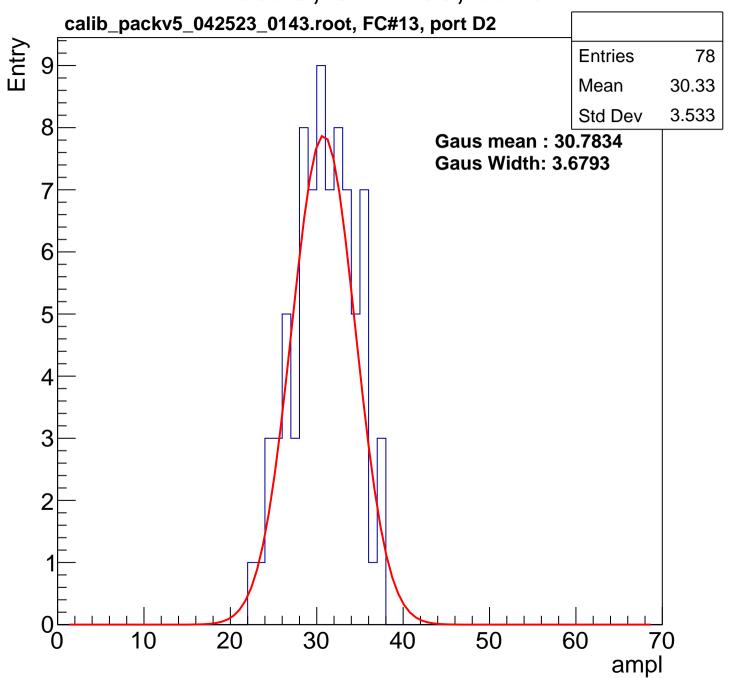


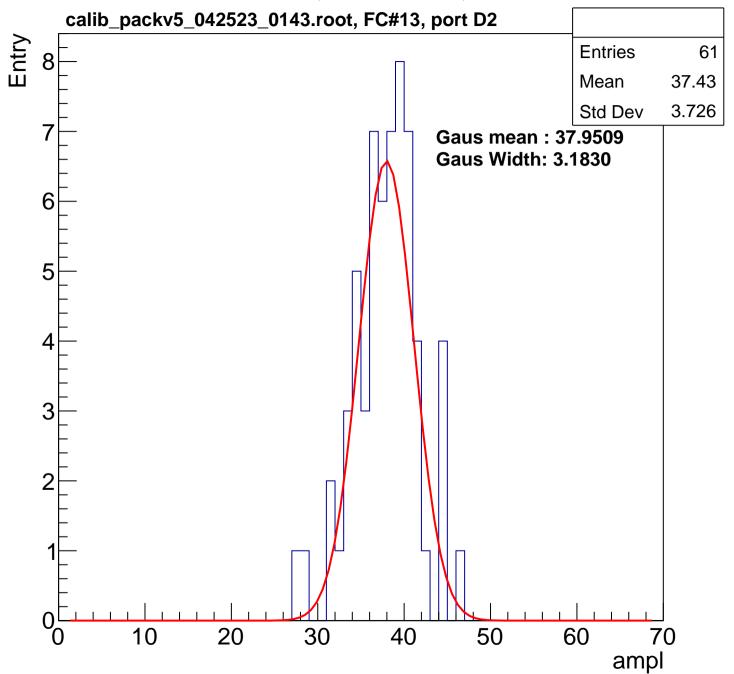


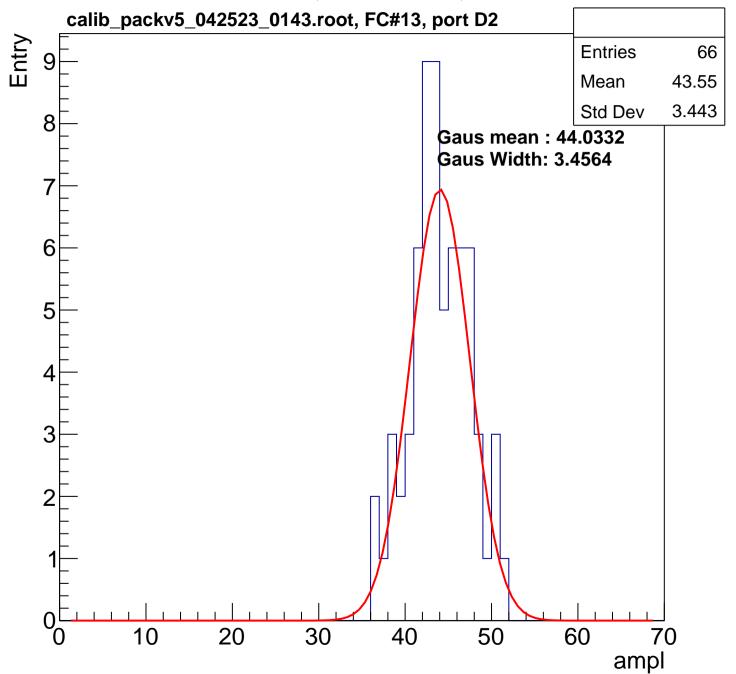


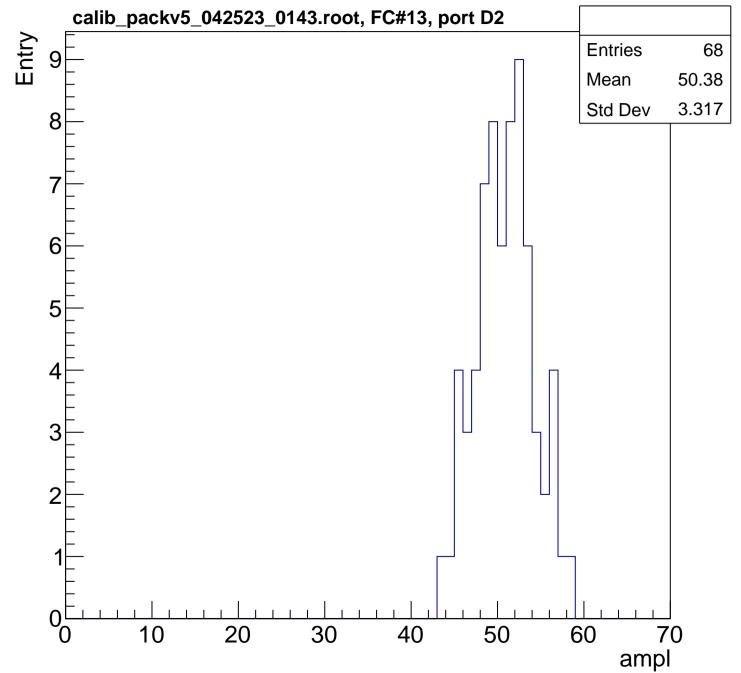


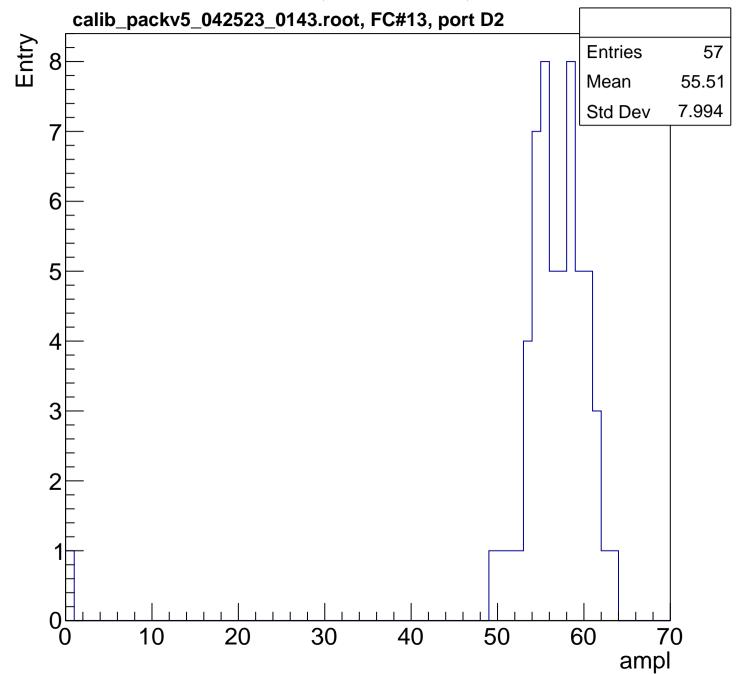
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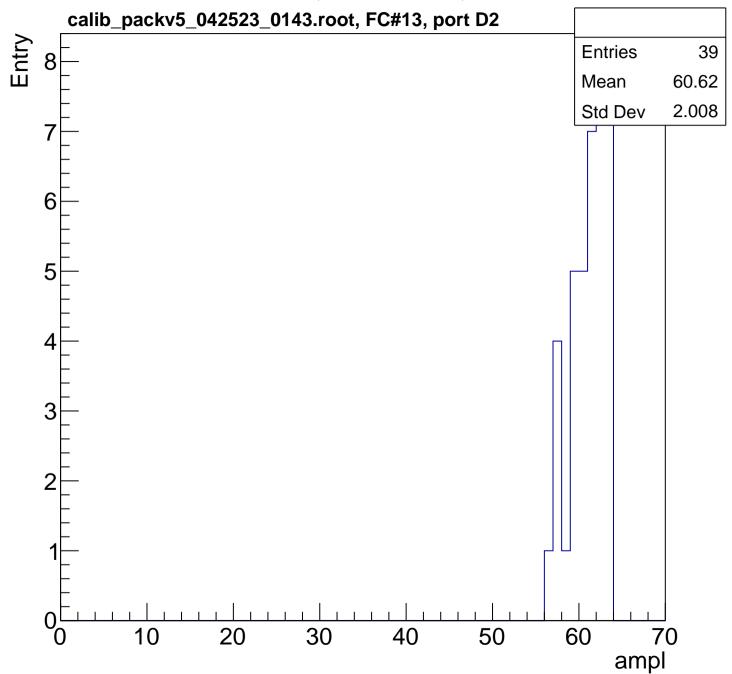


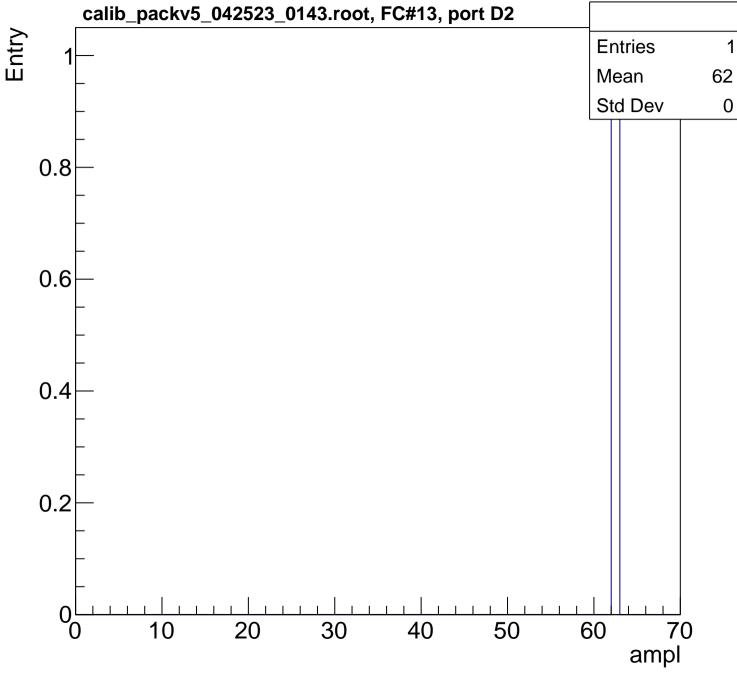


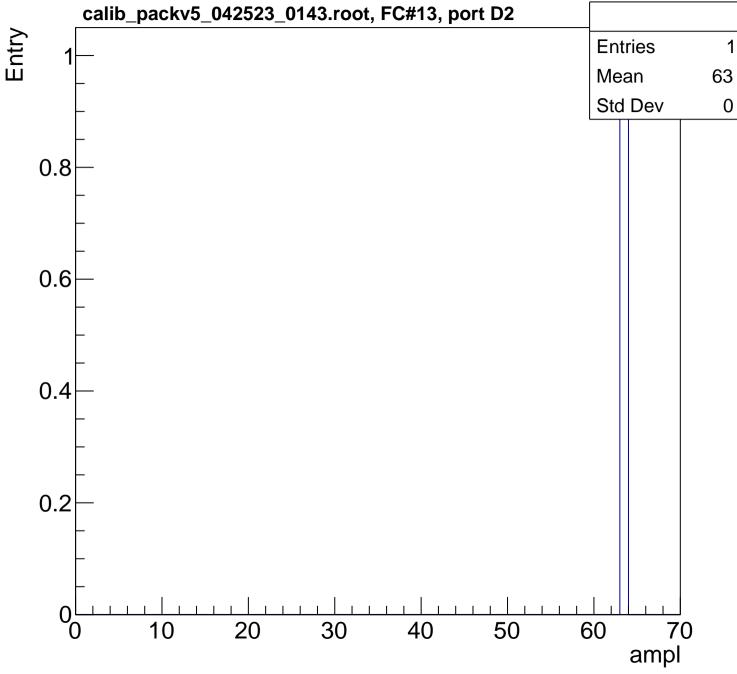


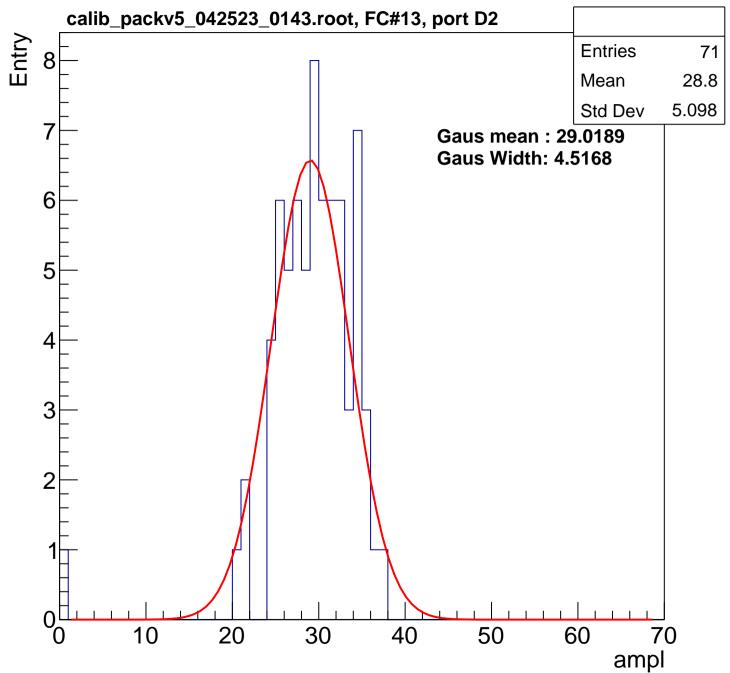


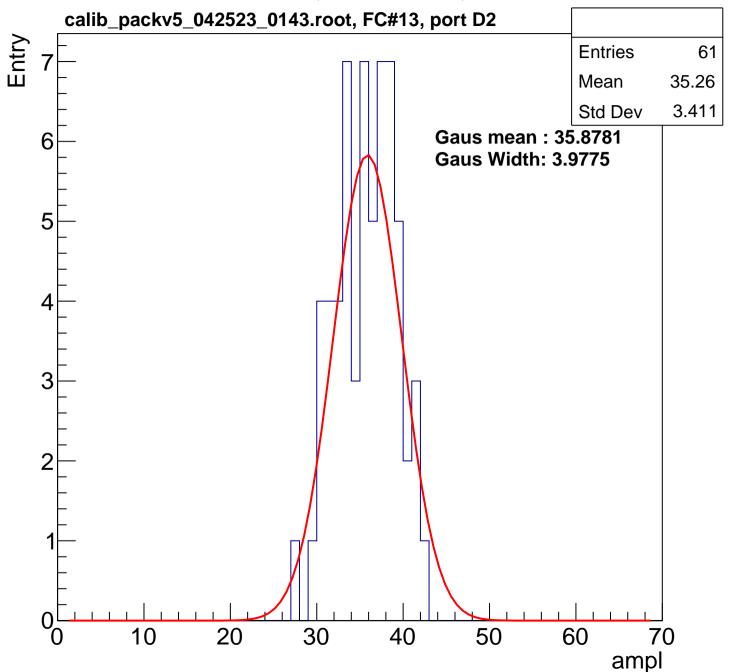


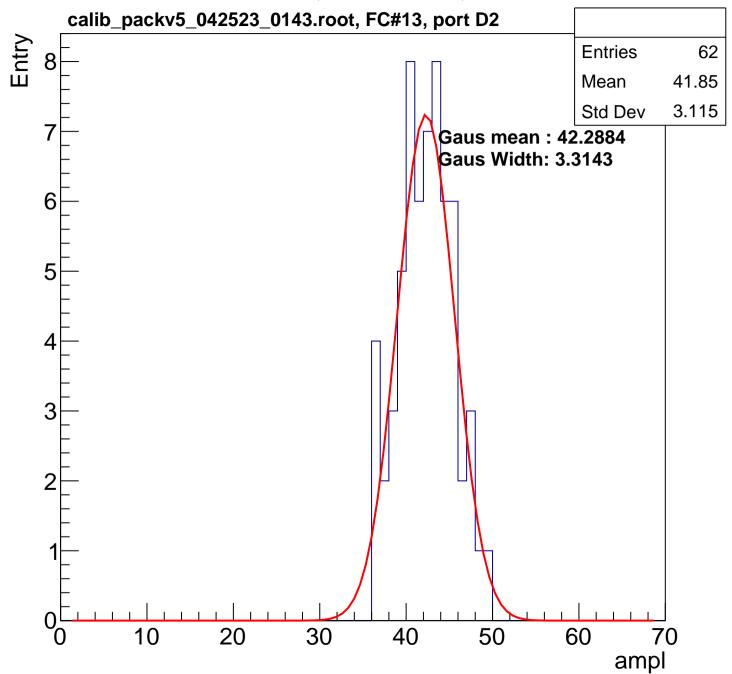


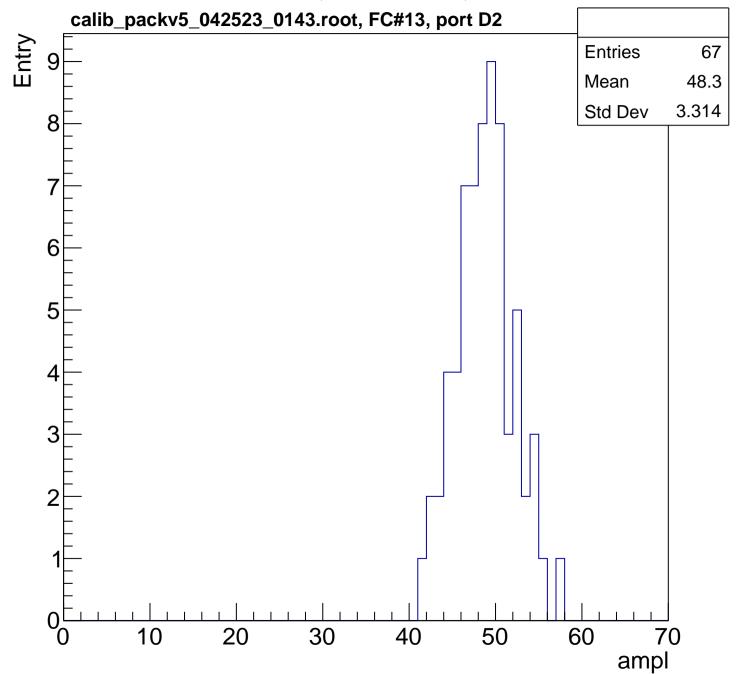


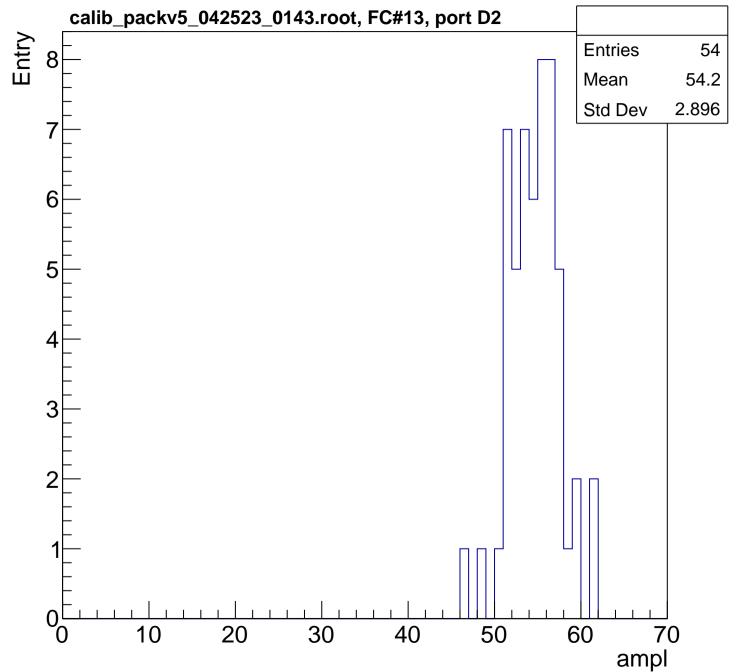


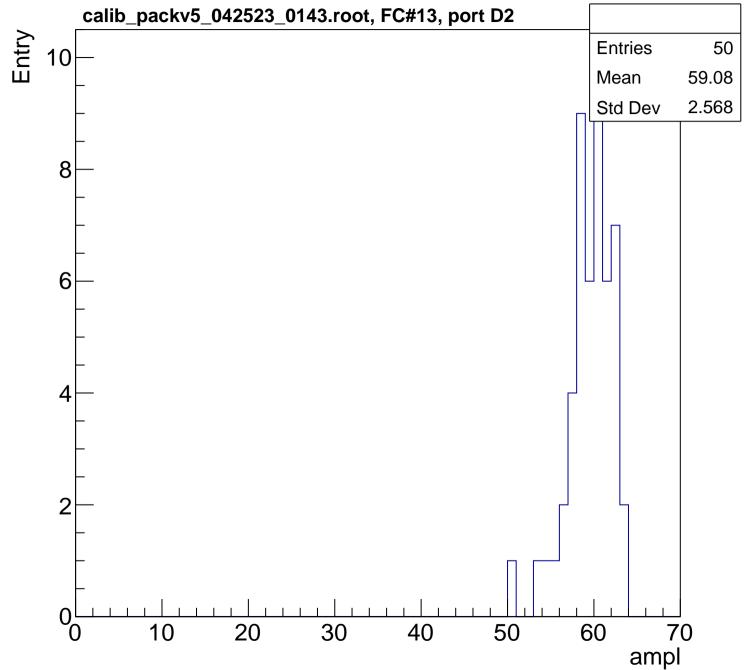


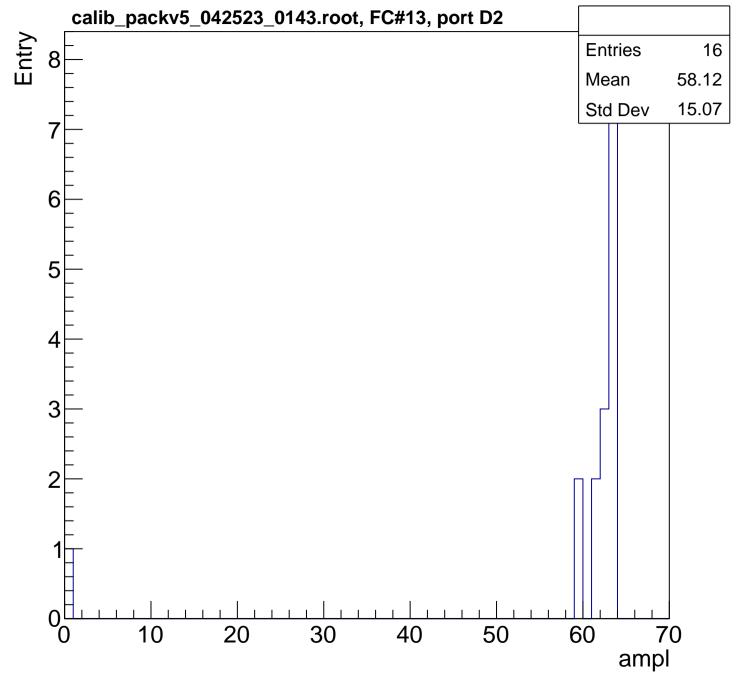


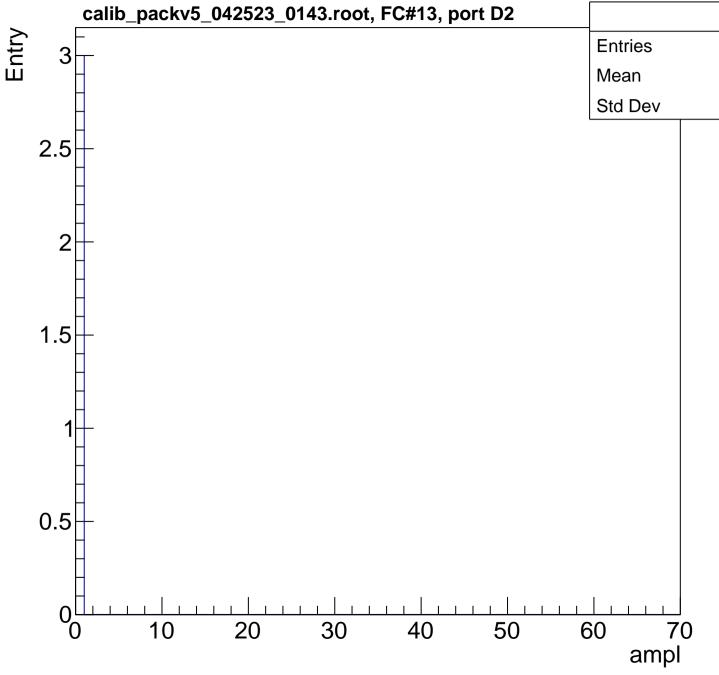


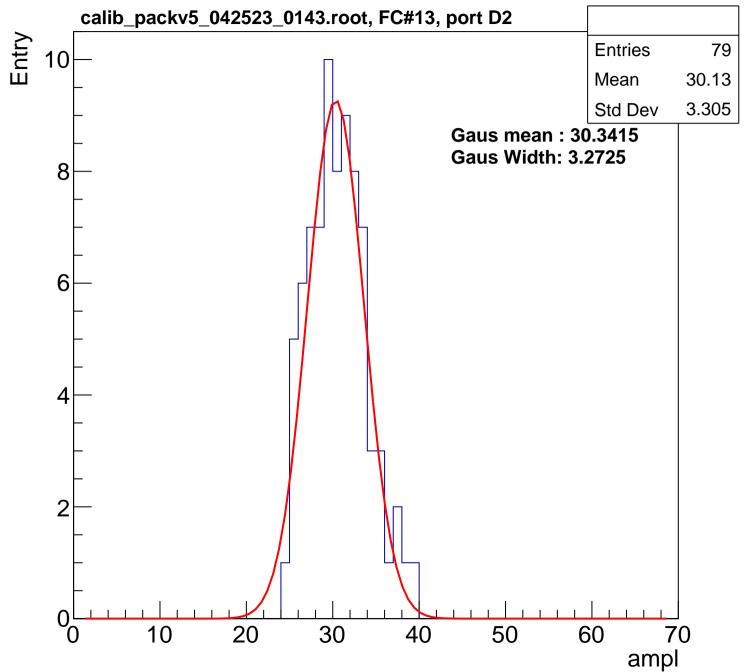


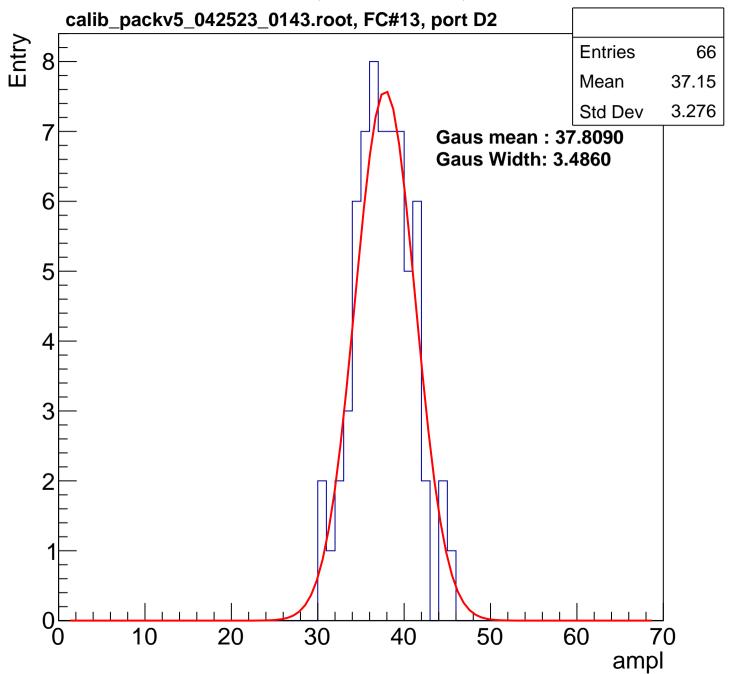


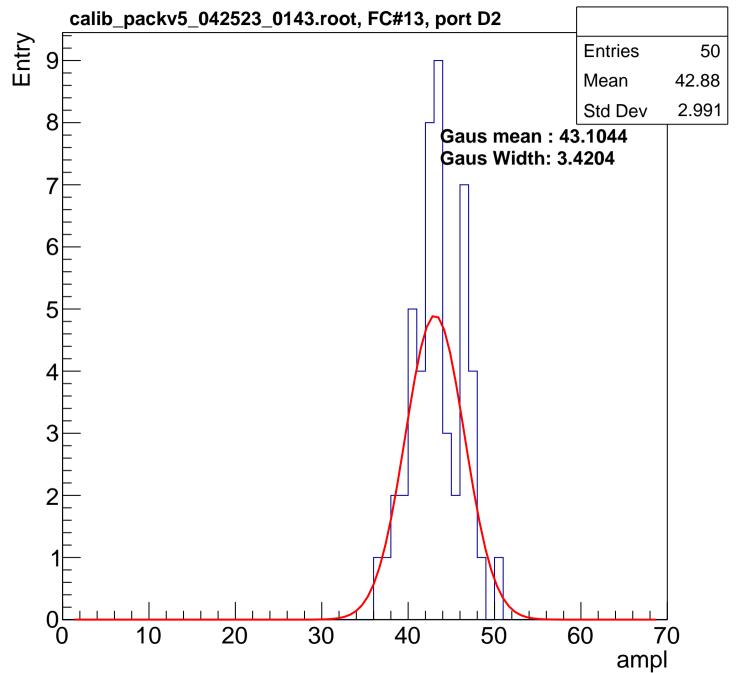


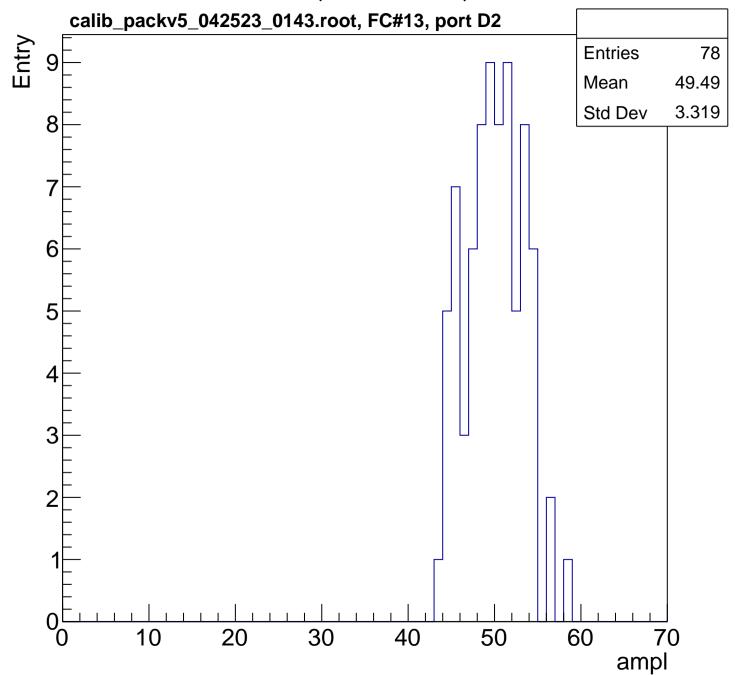


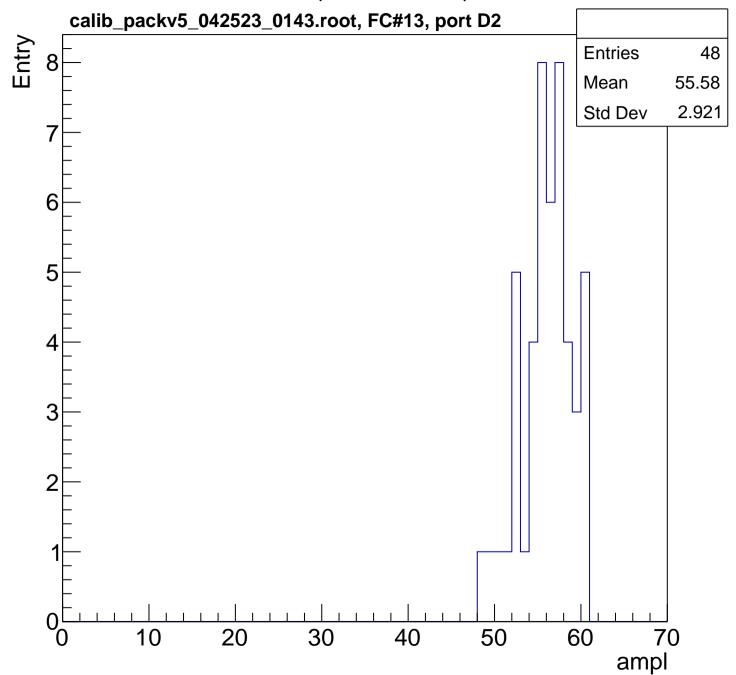


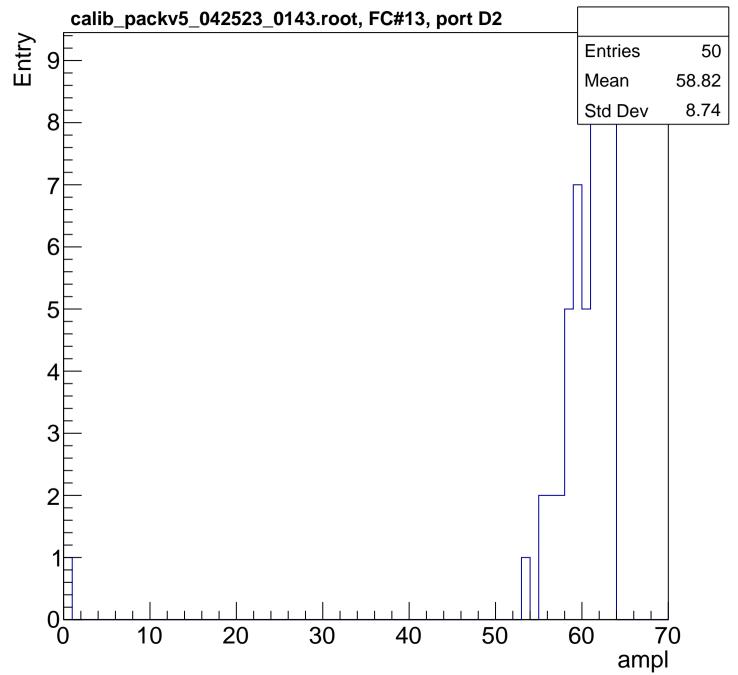


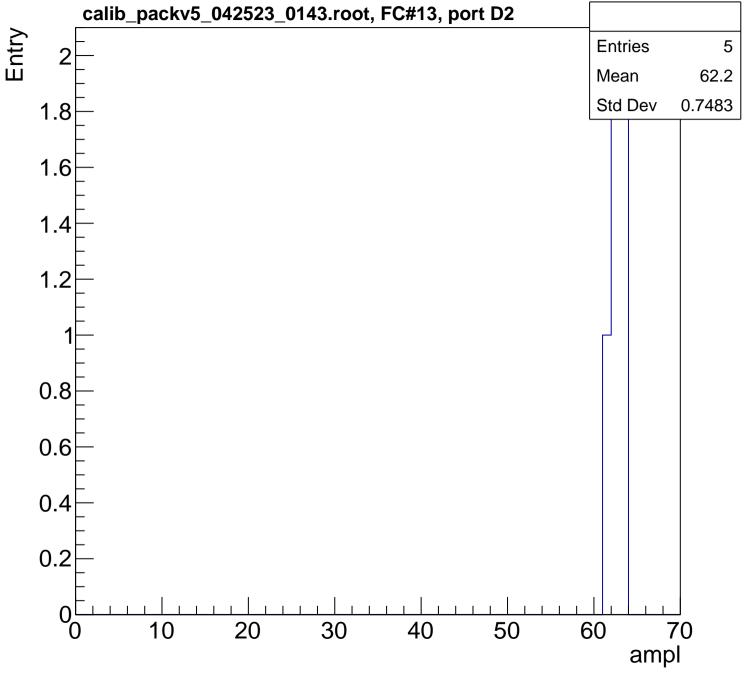




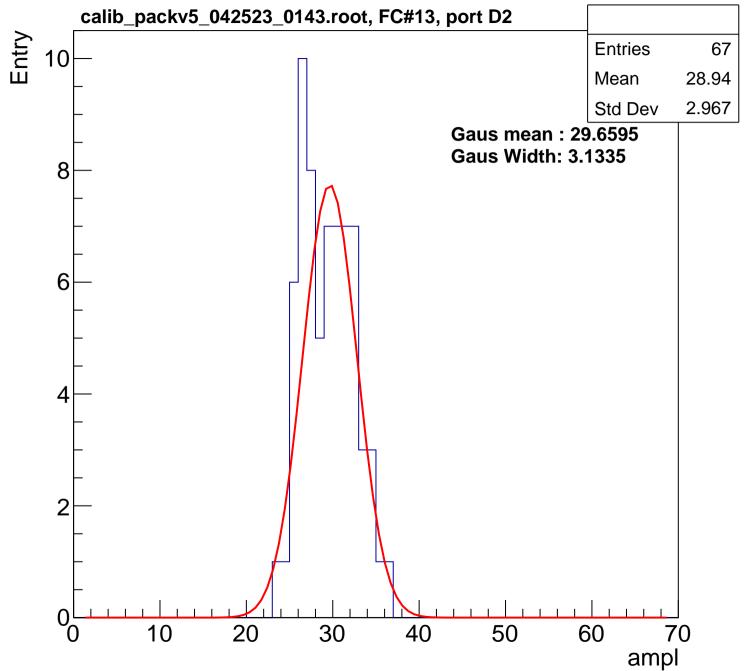


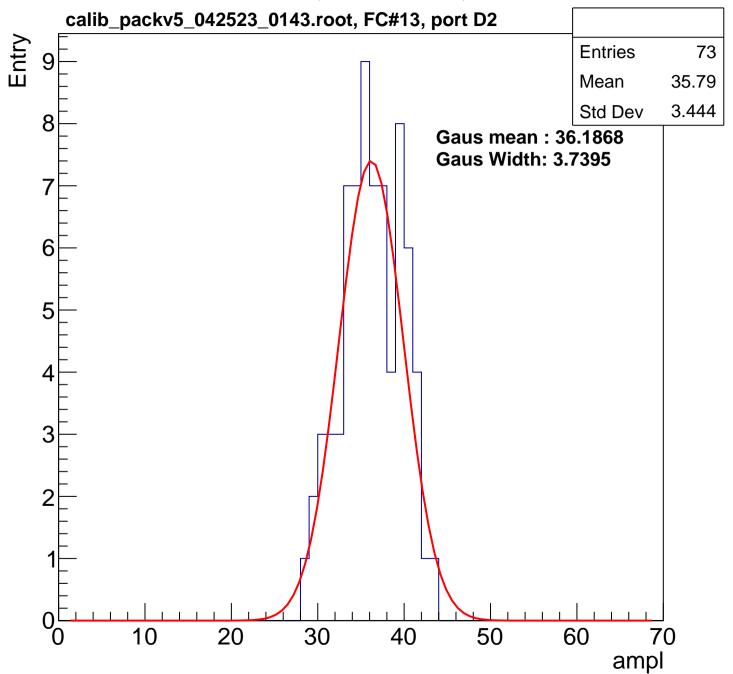


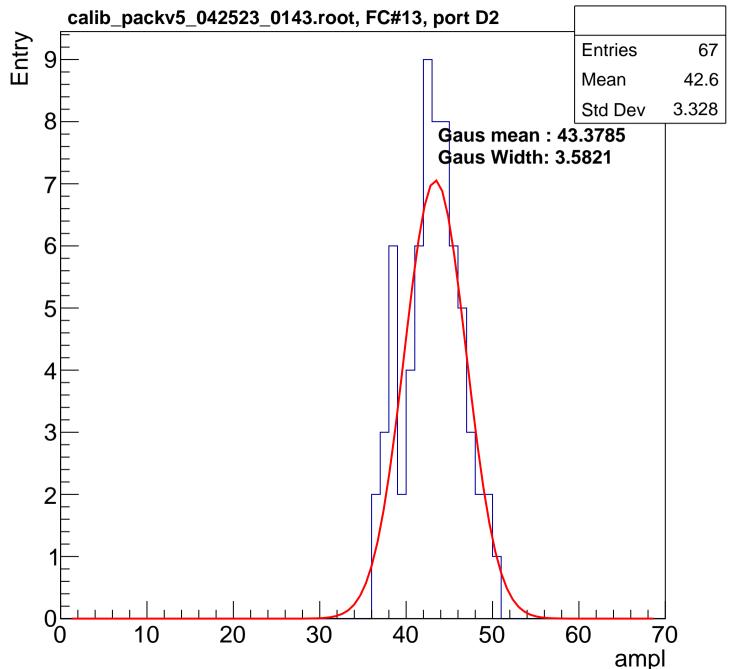


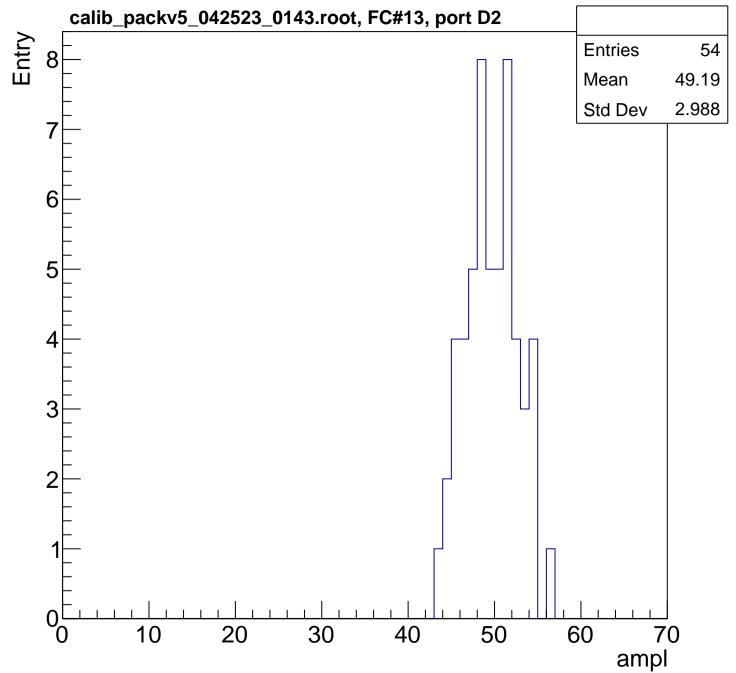


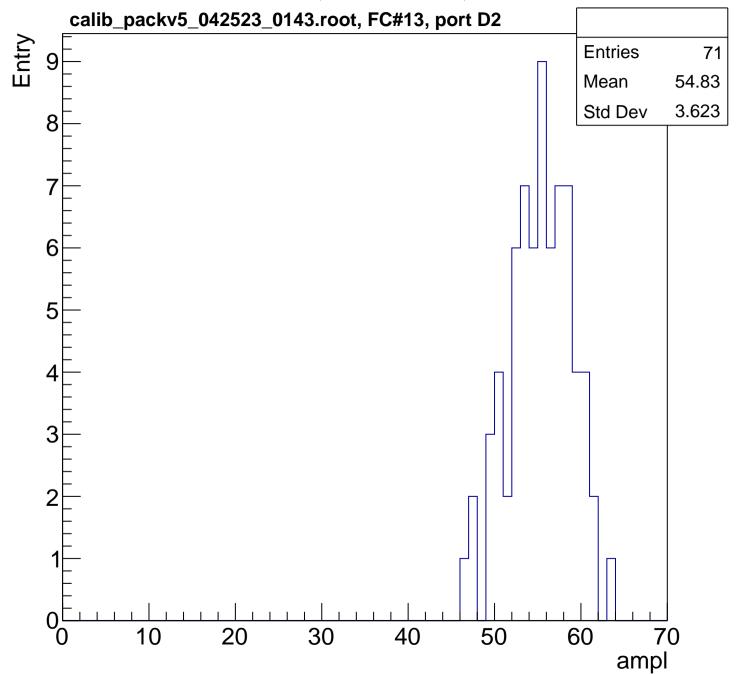
B1L003S, U2-ch35, adc7 calib_packv5_042523_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

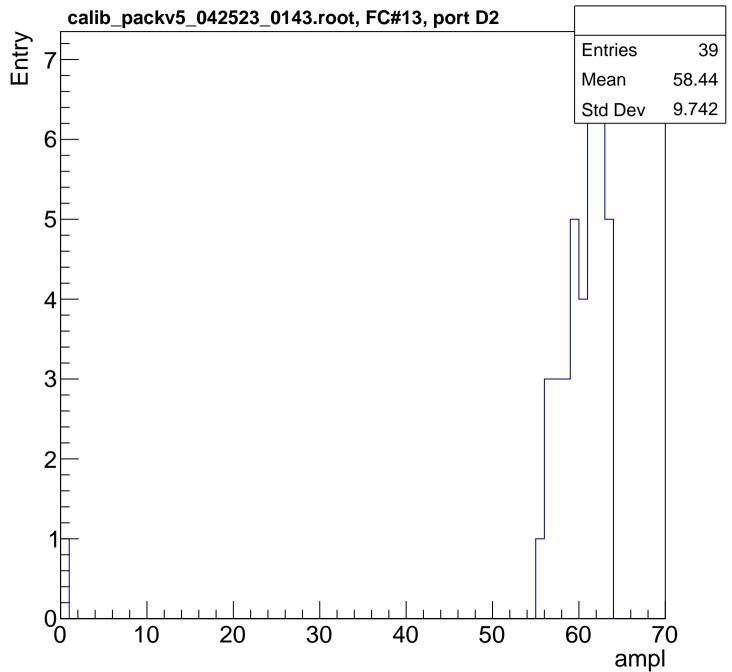


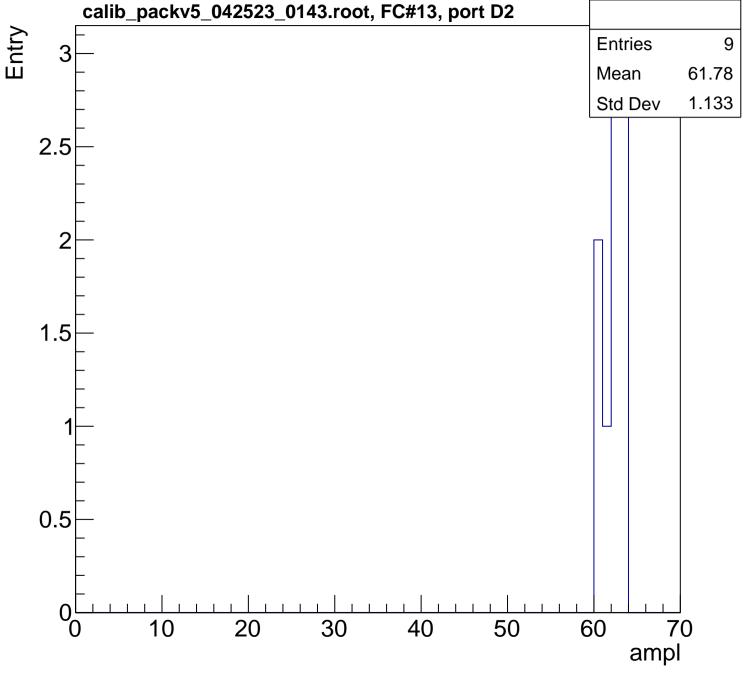


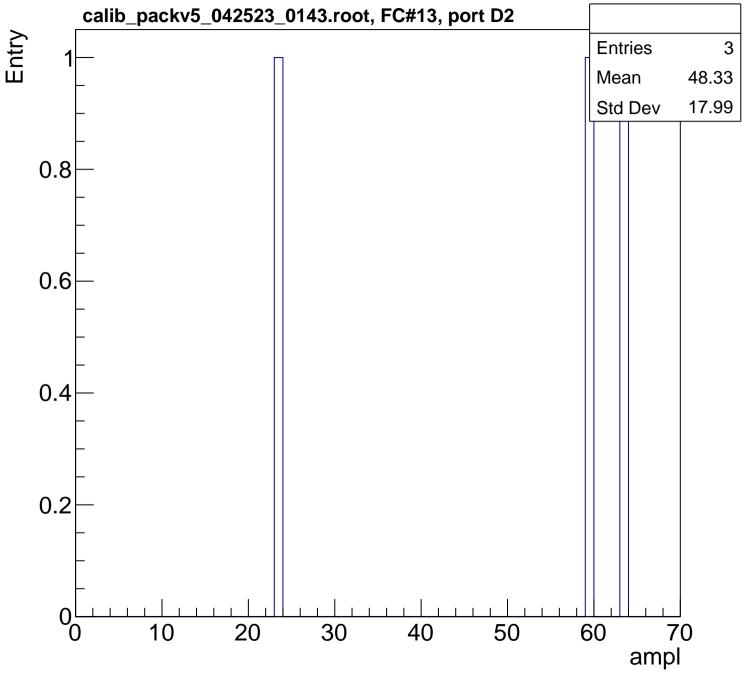


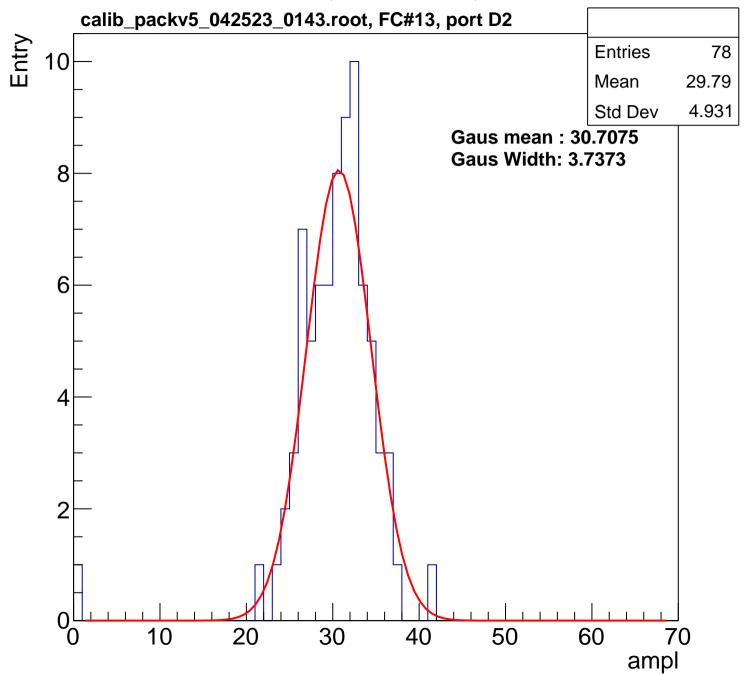


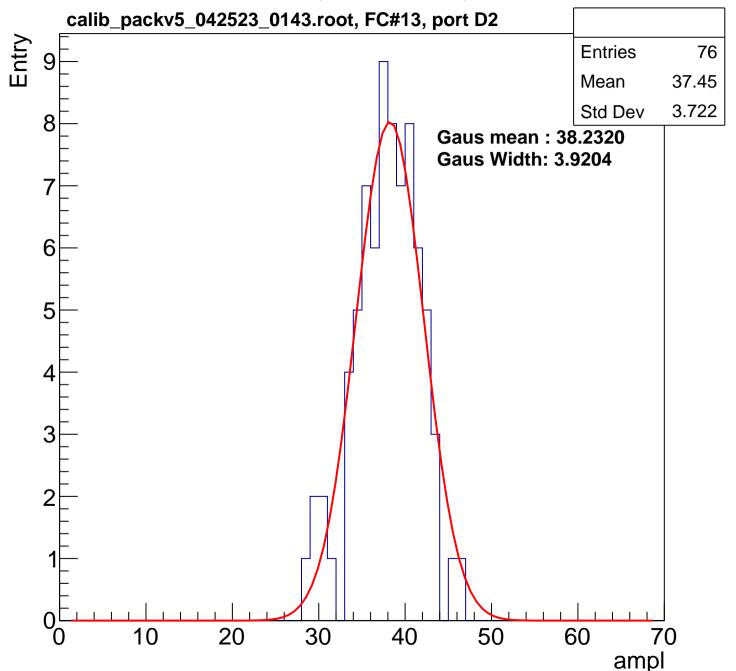


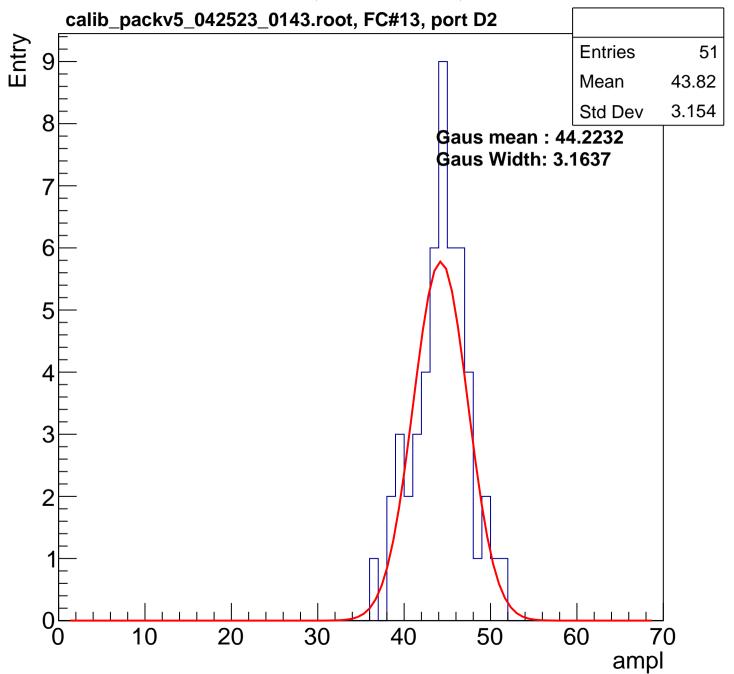


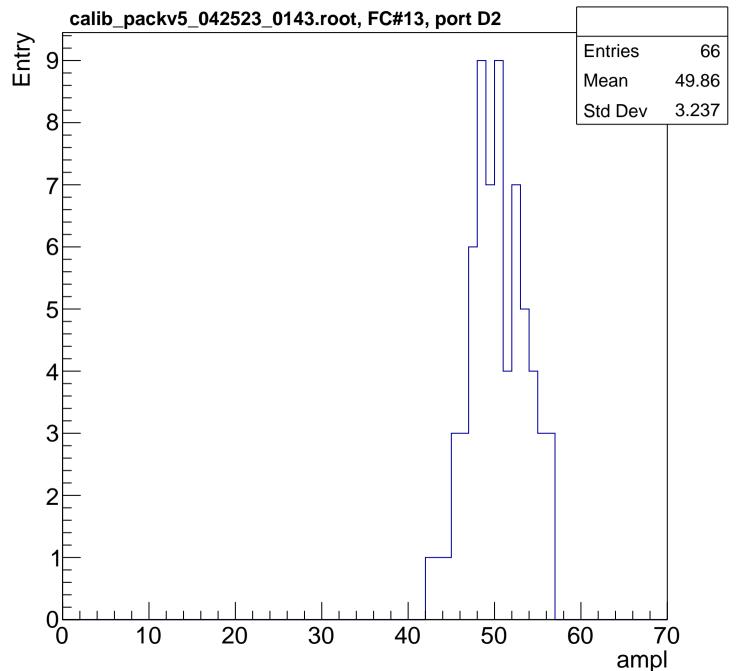


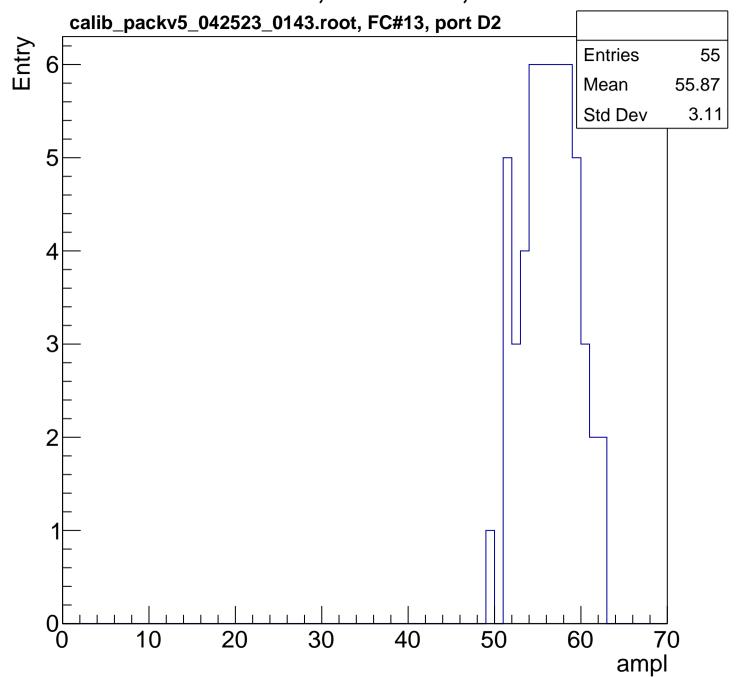


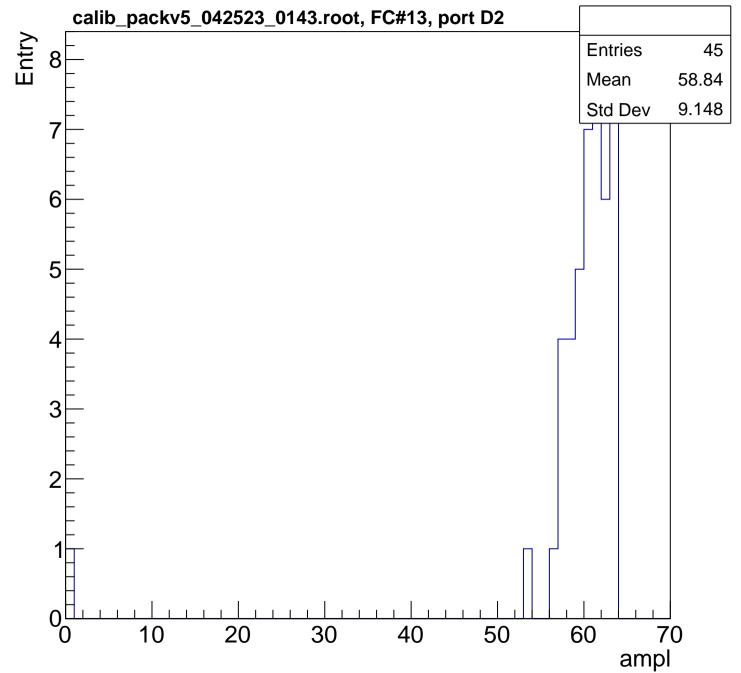


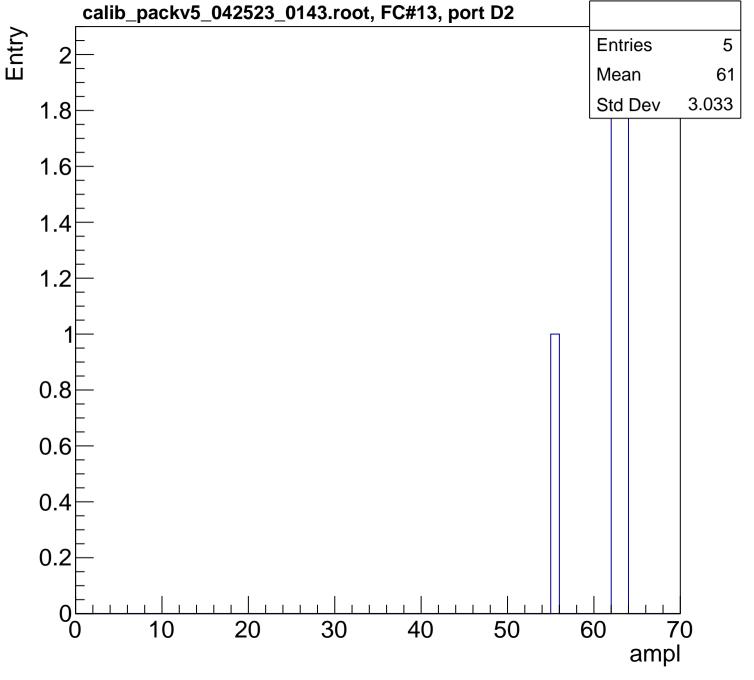


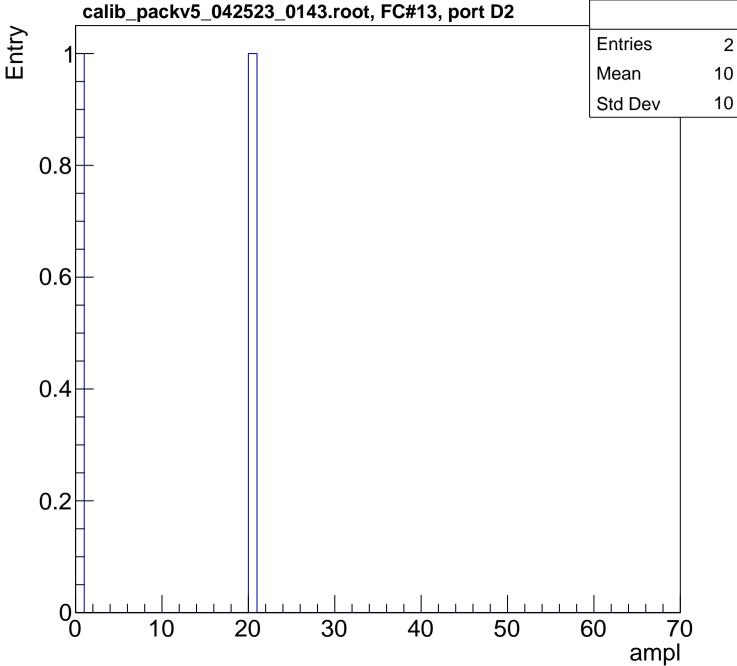


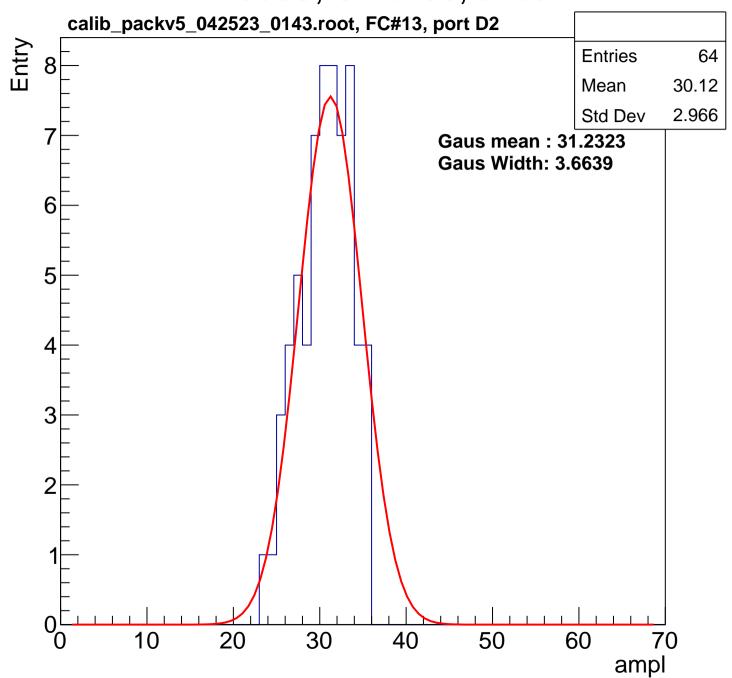


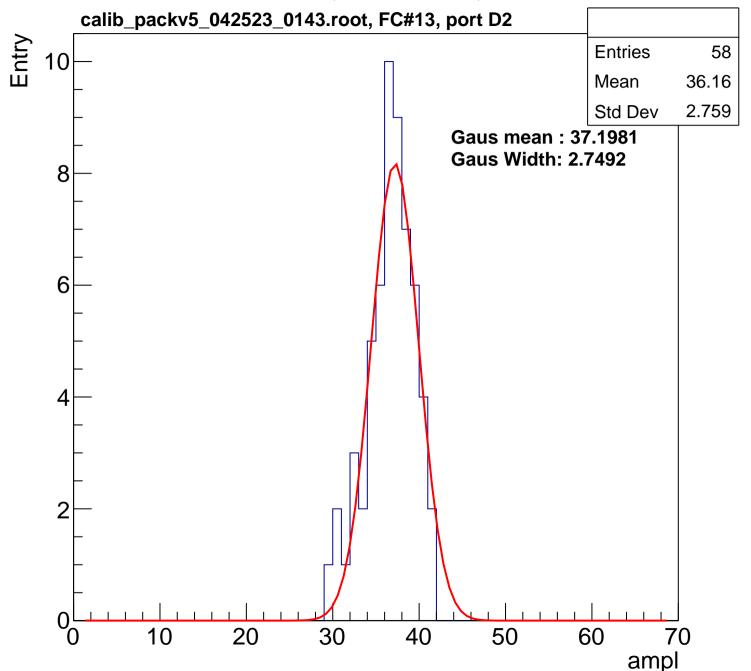


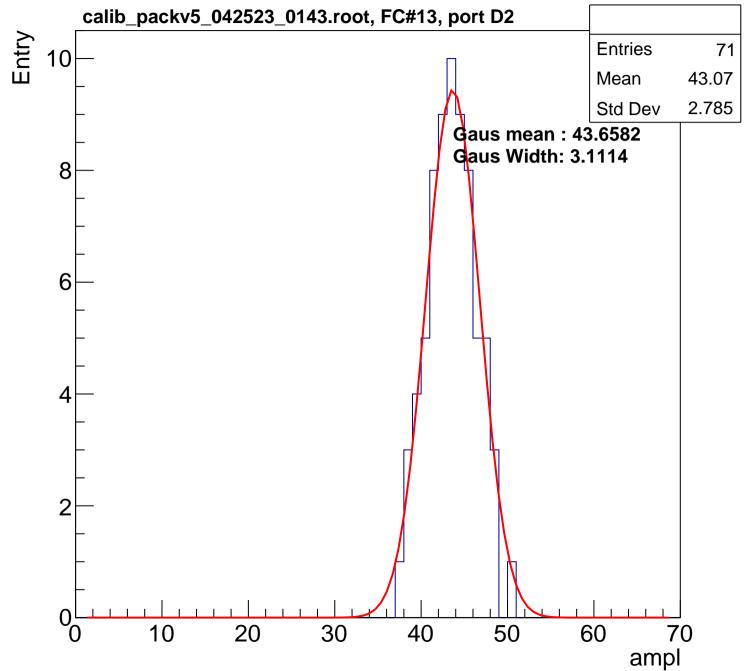


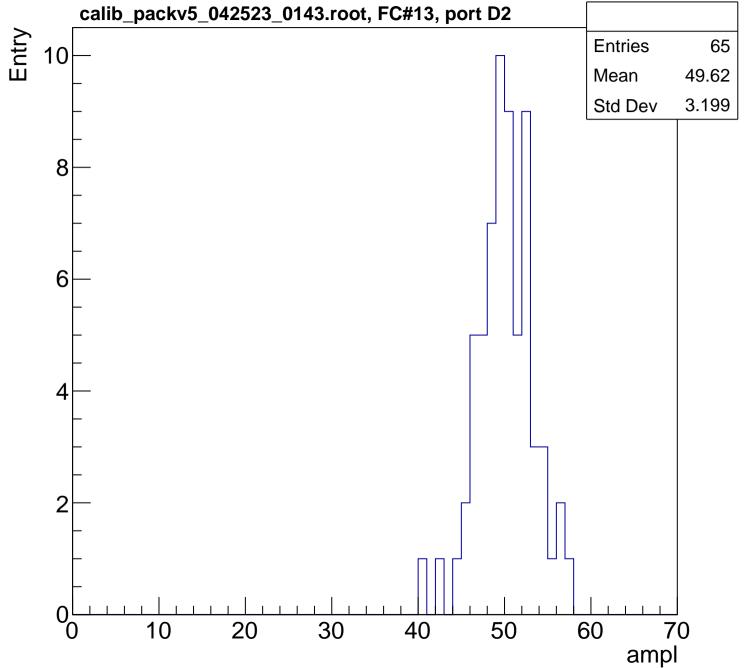


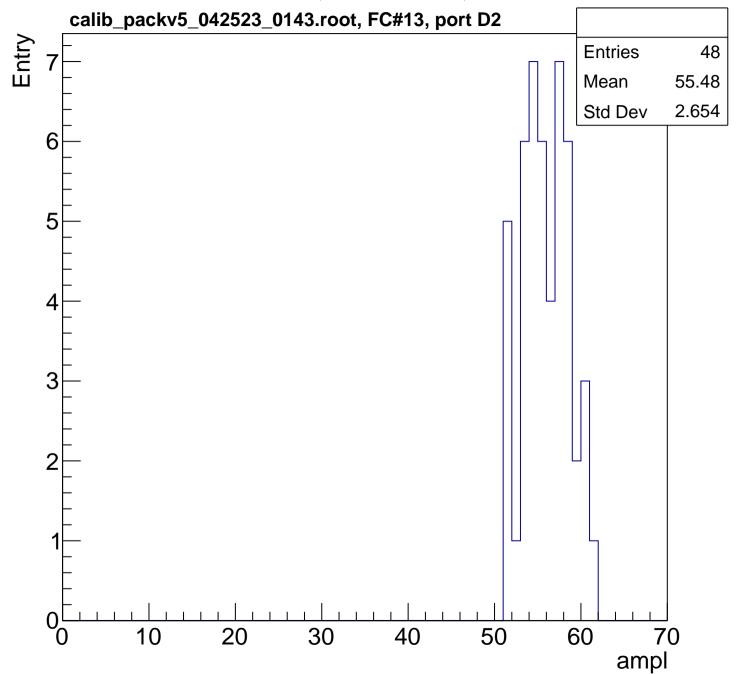


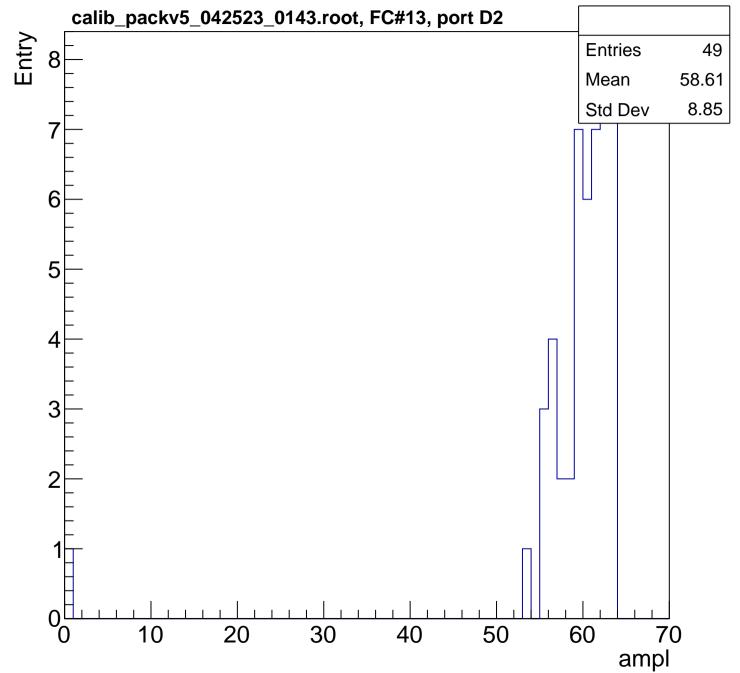


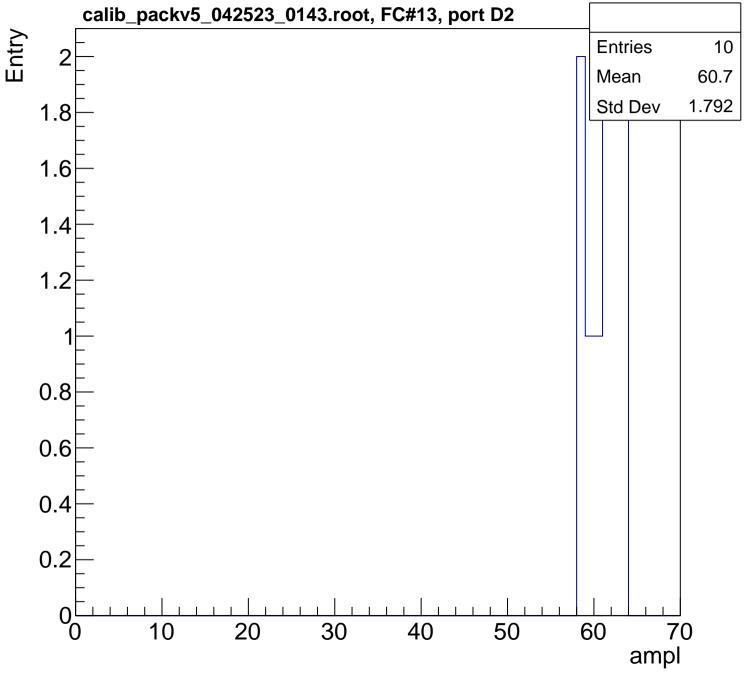




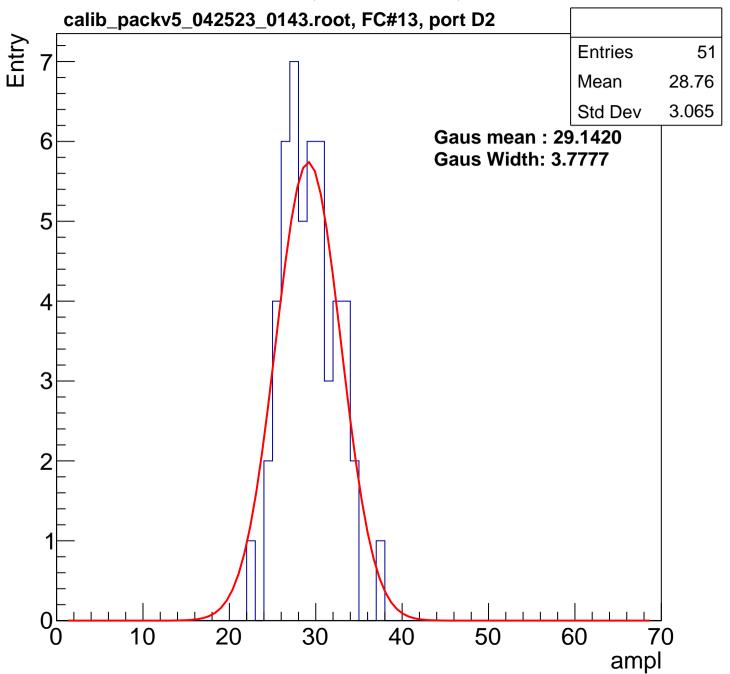


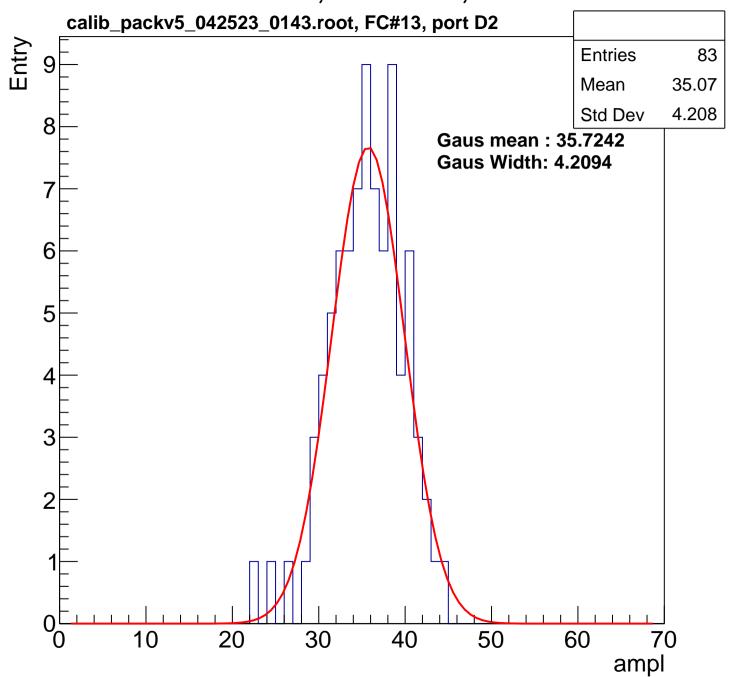


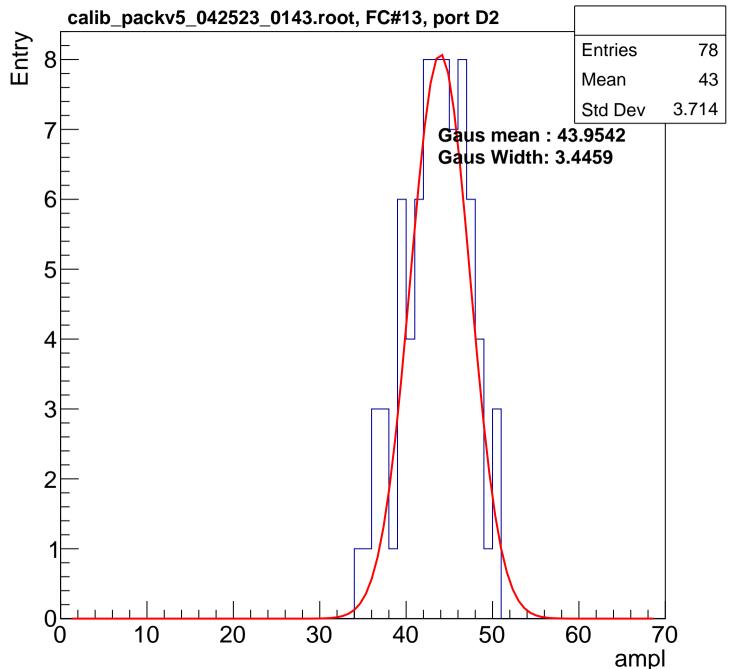


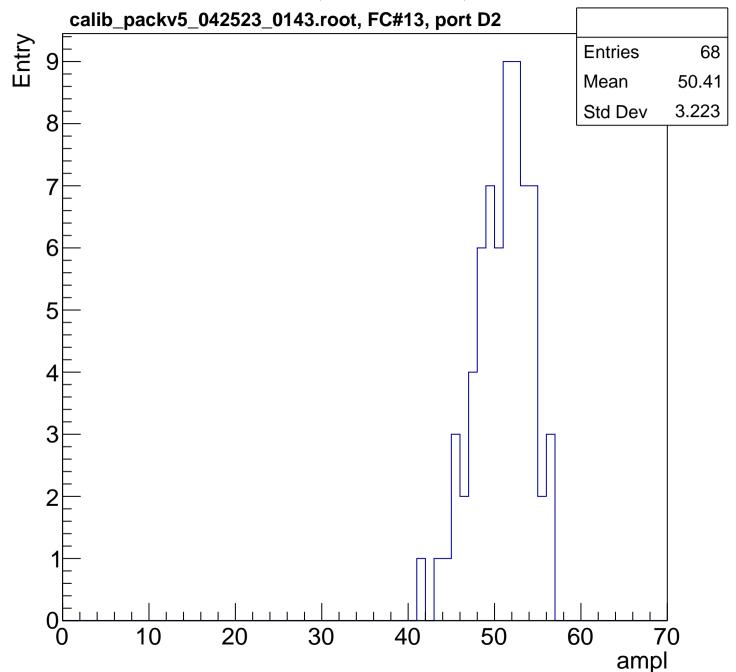


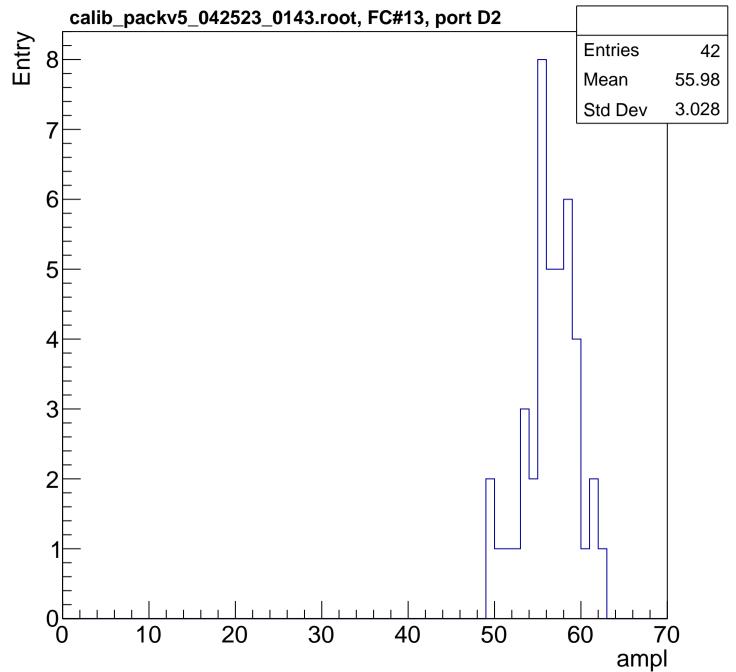
B1L003S, U2-ch38, adc7 calib_packv5_042523_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

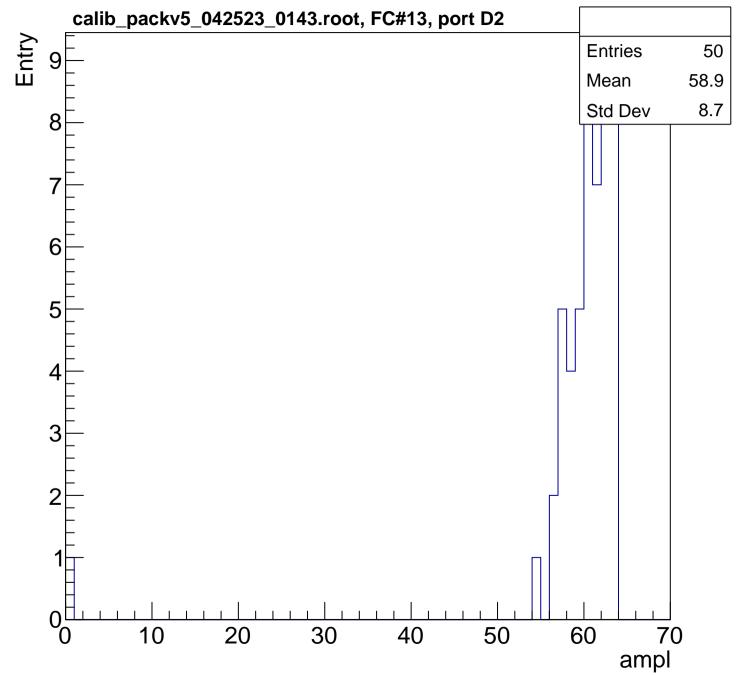


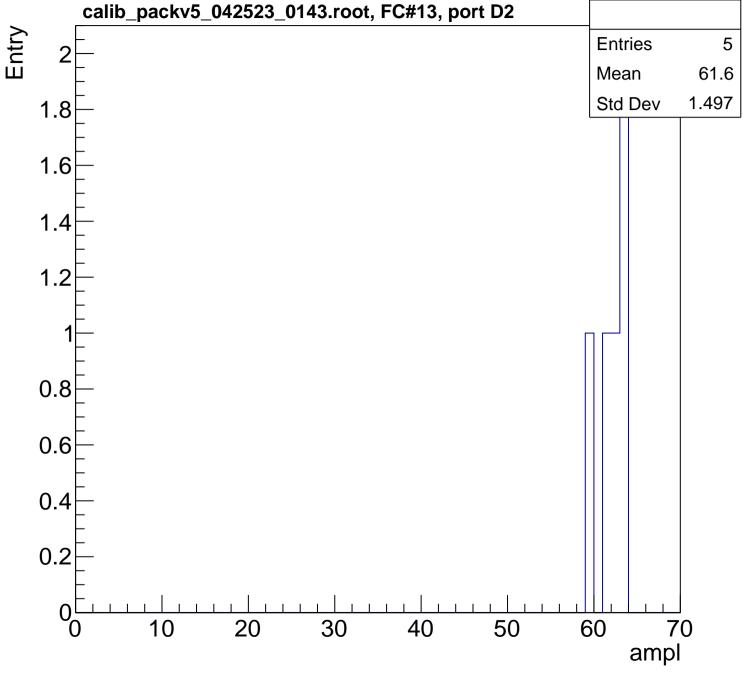


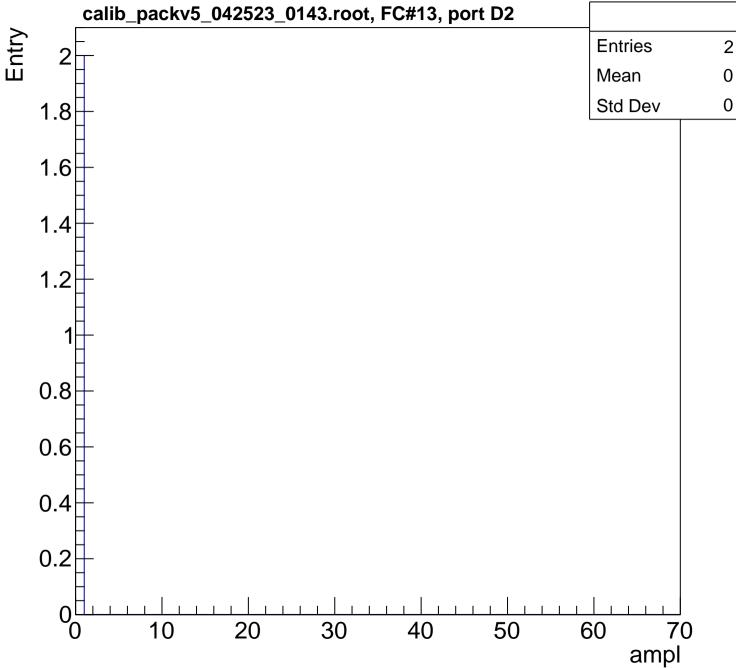


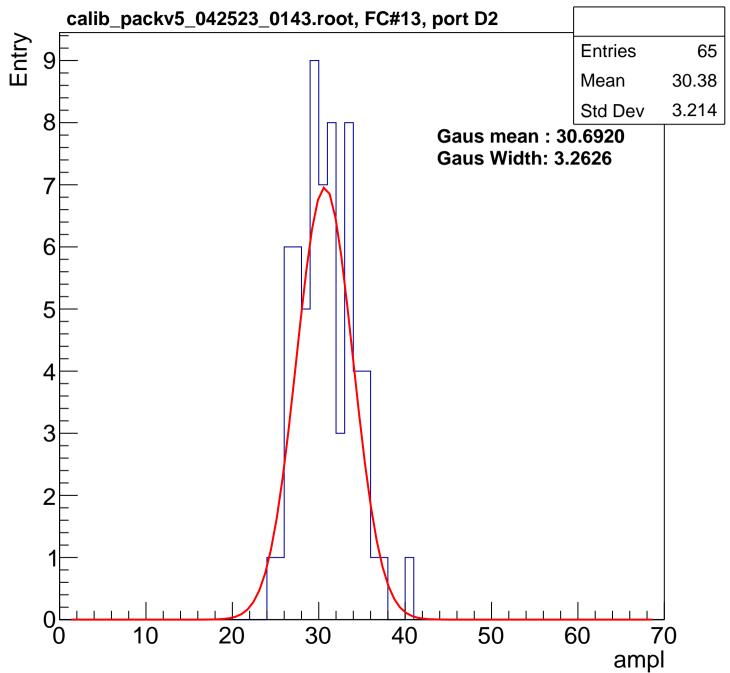


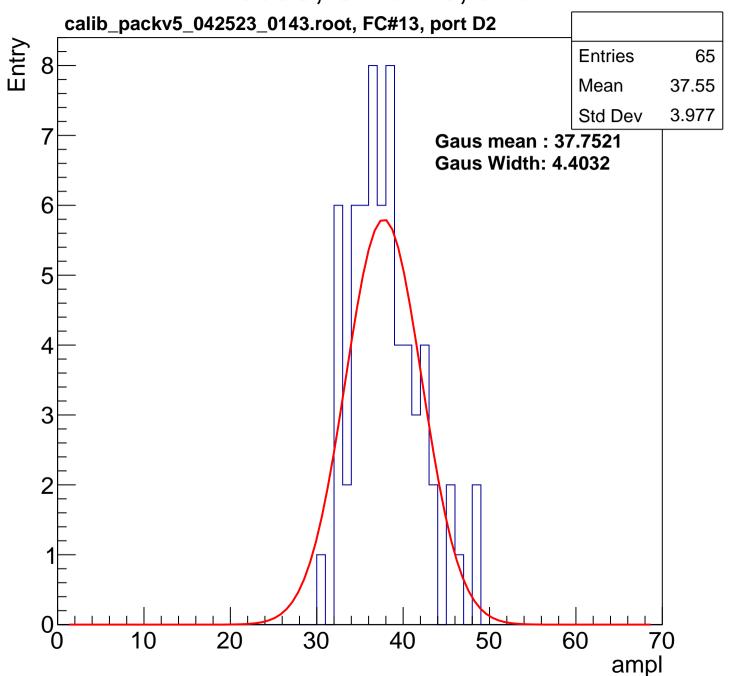


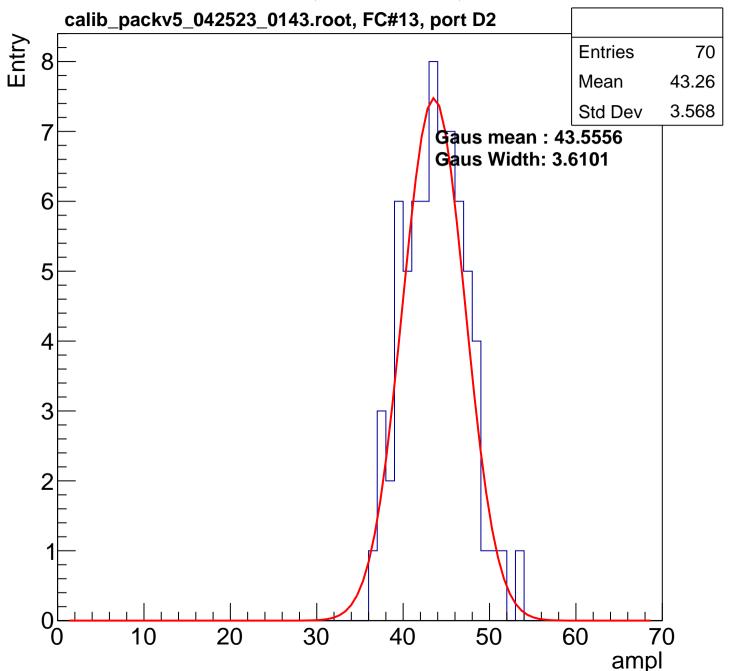


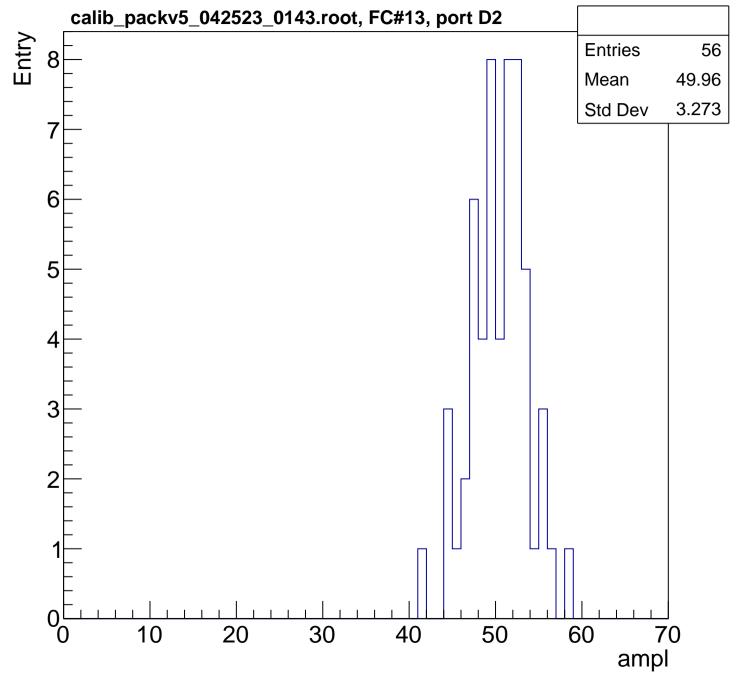


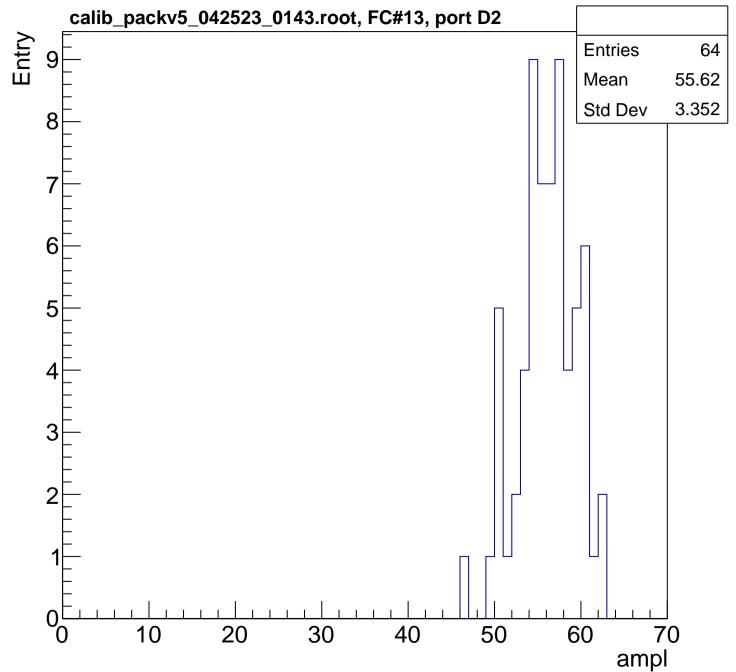


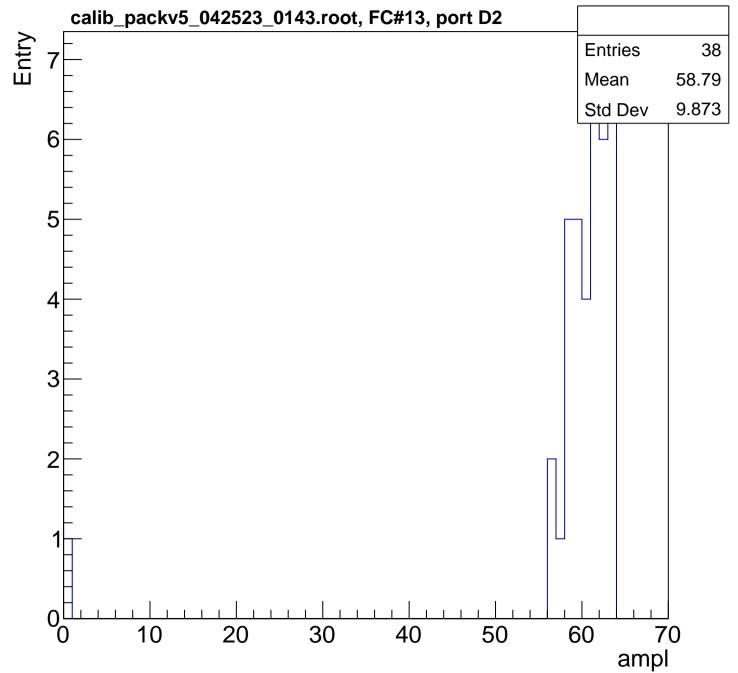


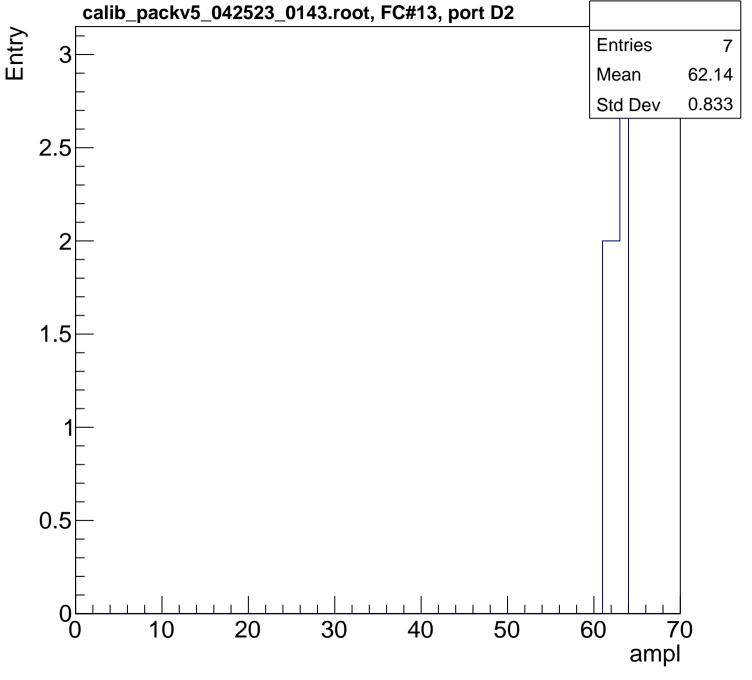


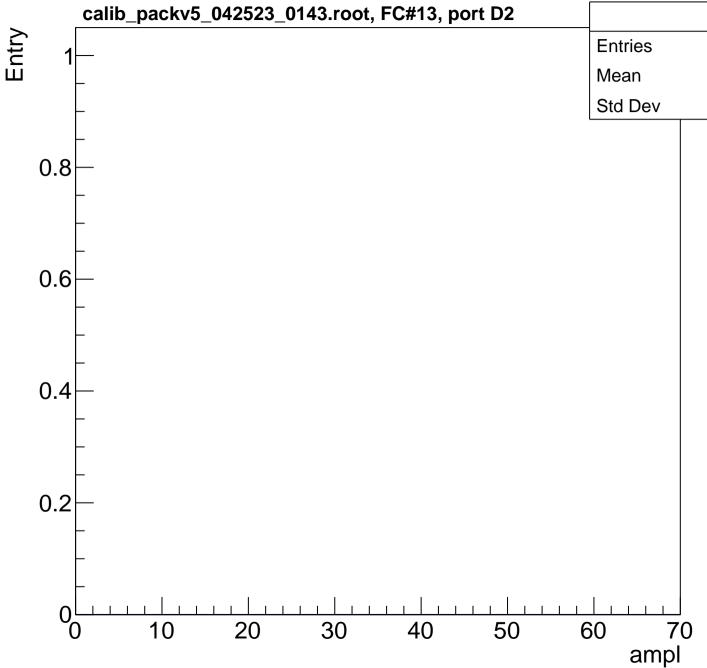


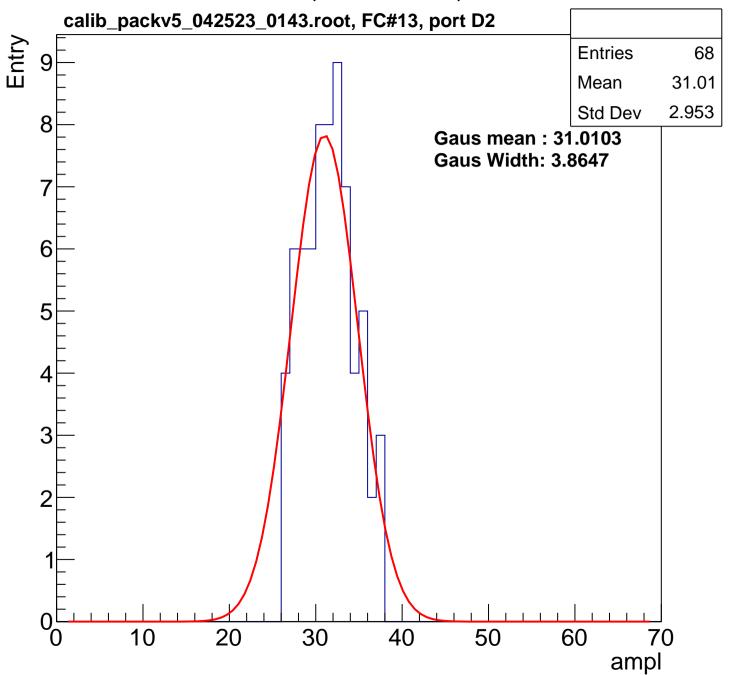


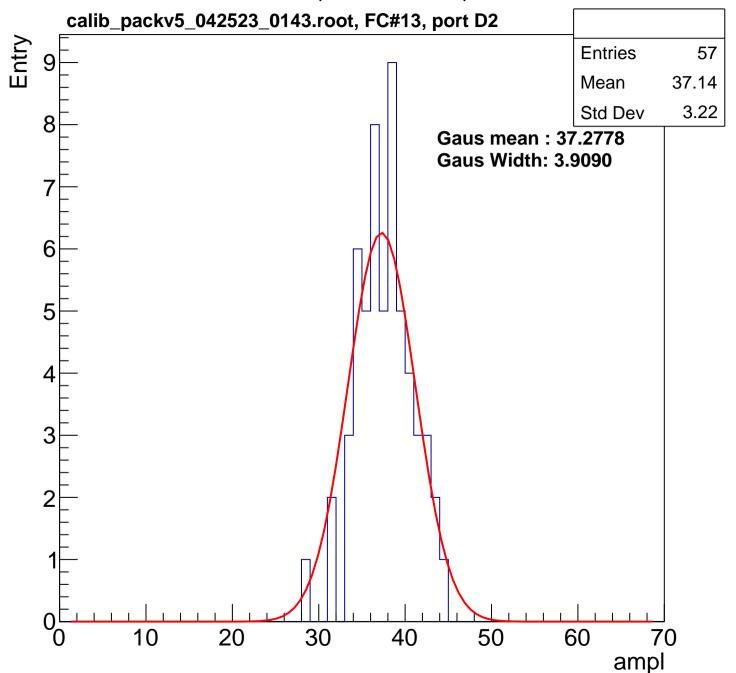


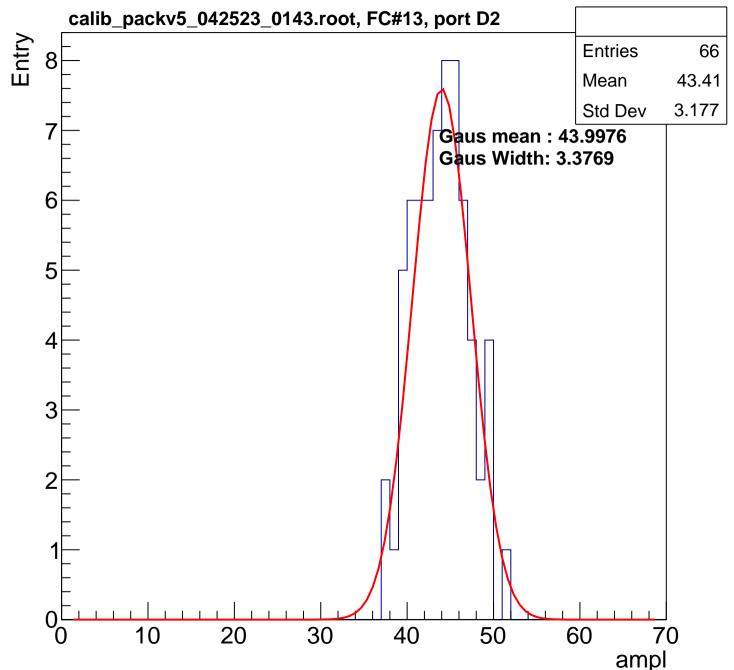


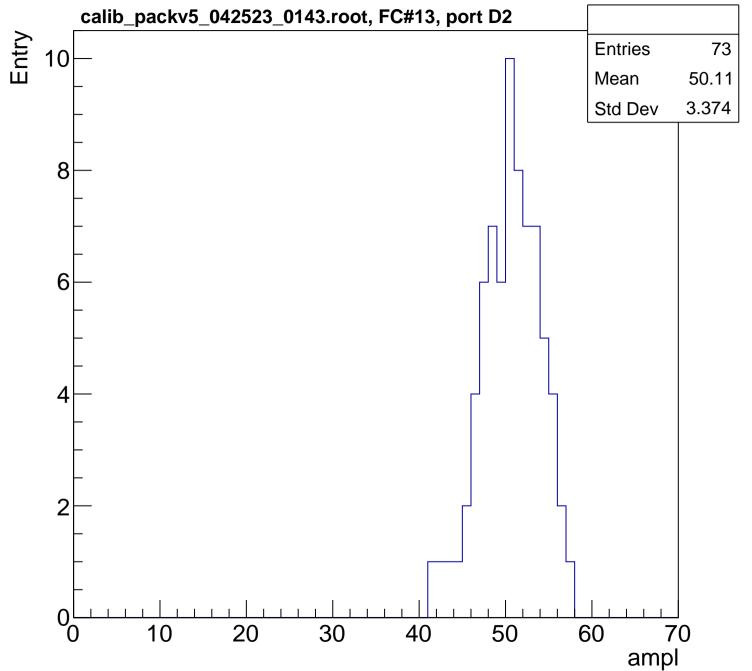


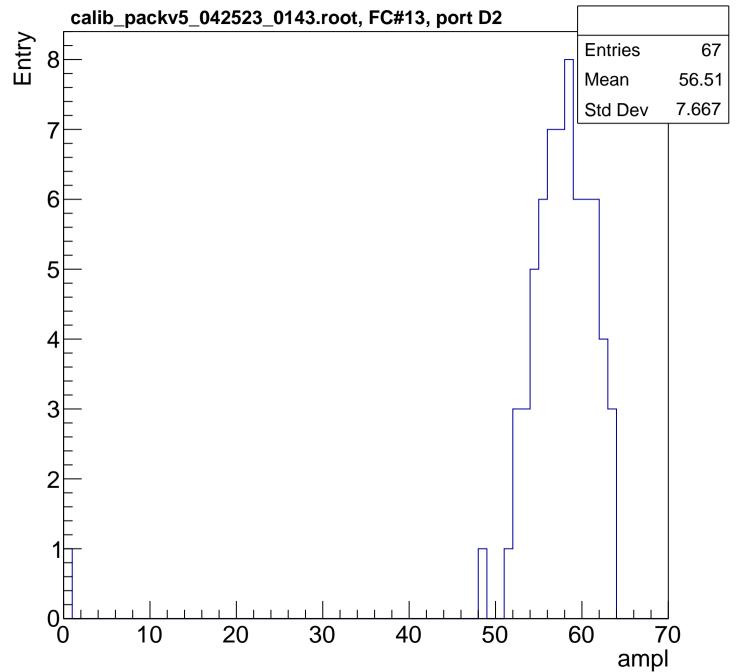


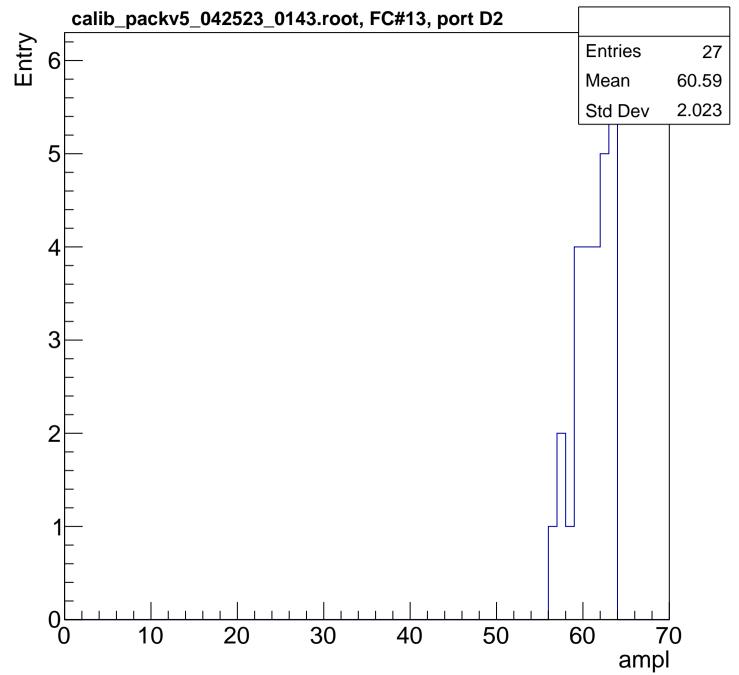


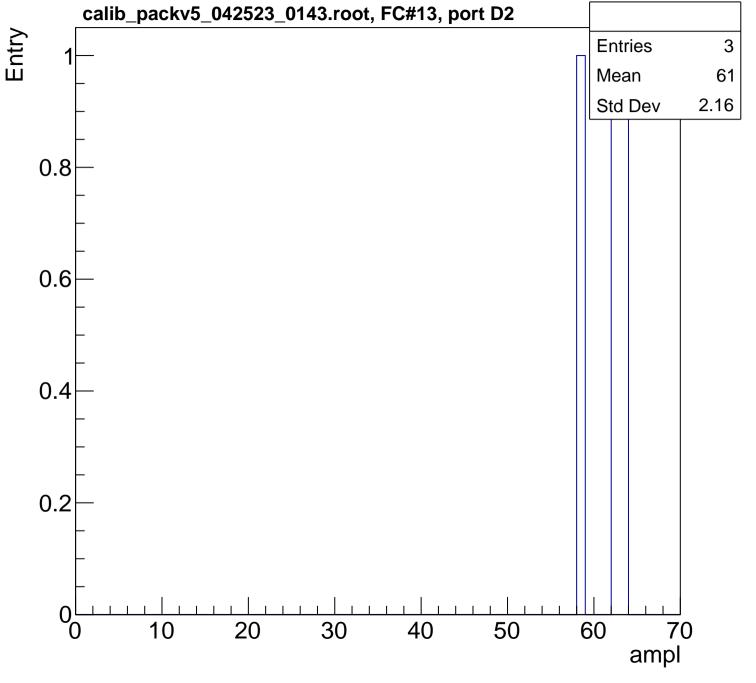




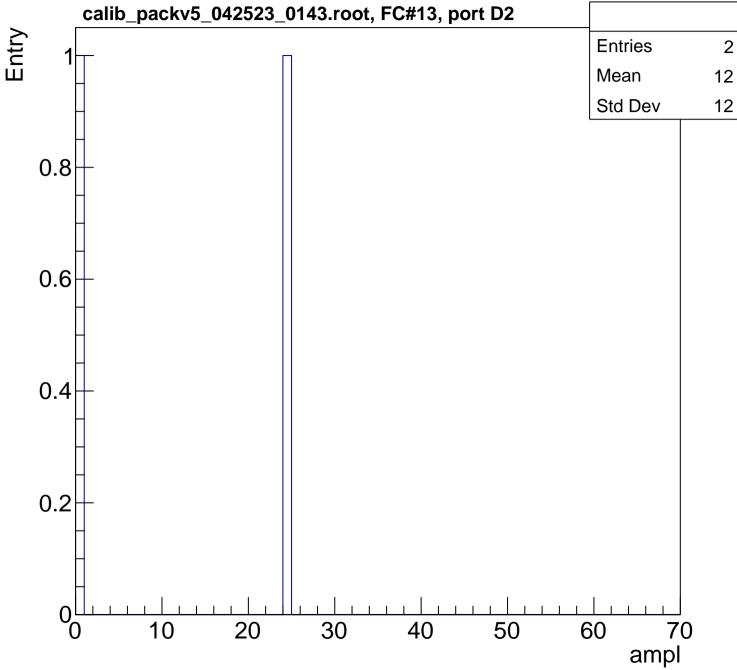


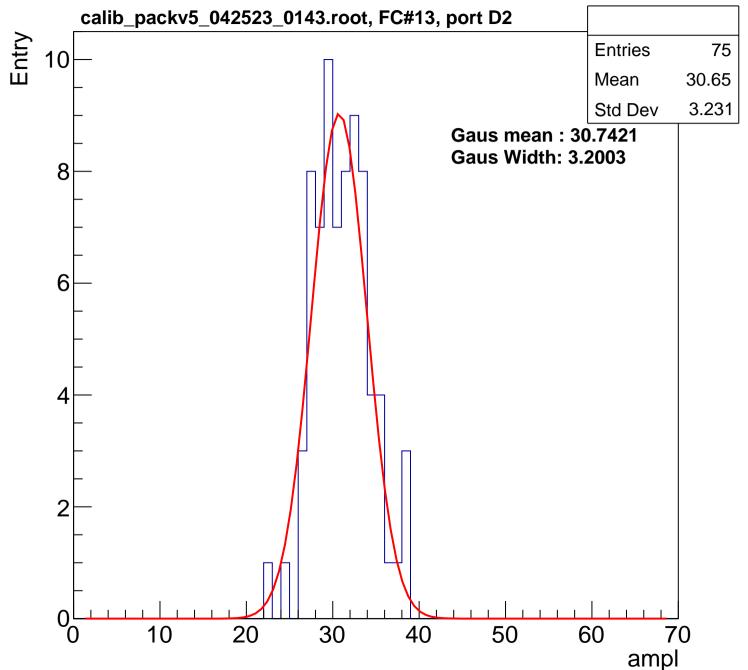


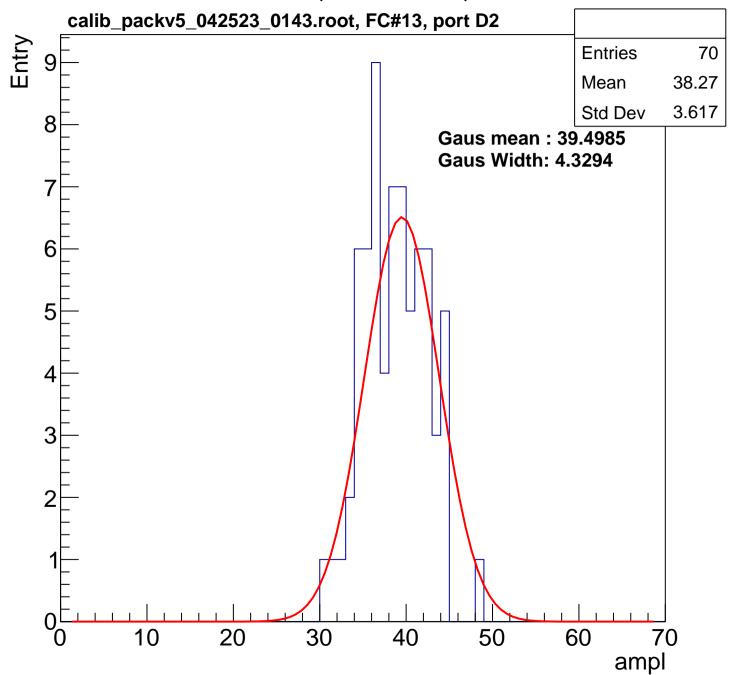


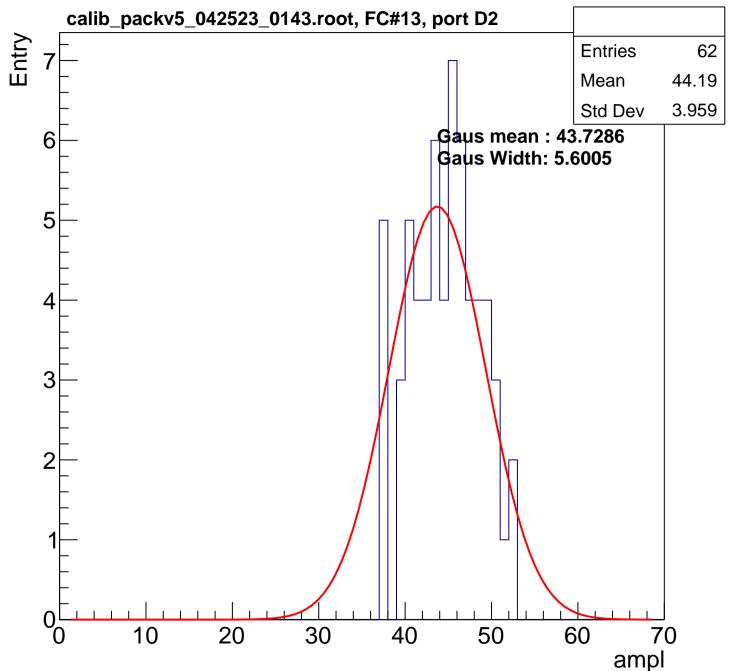


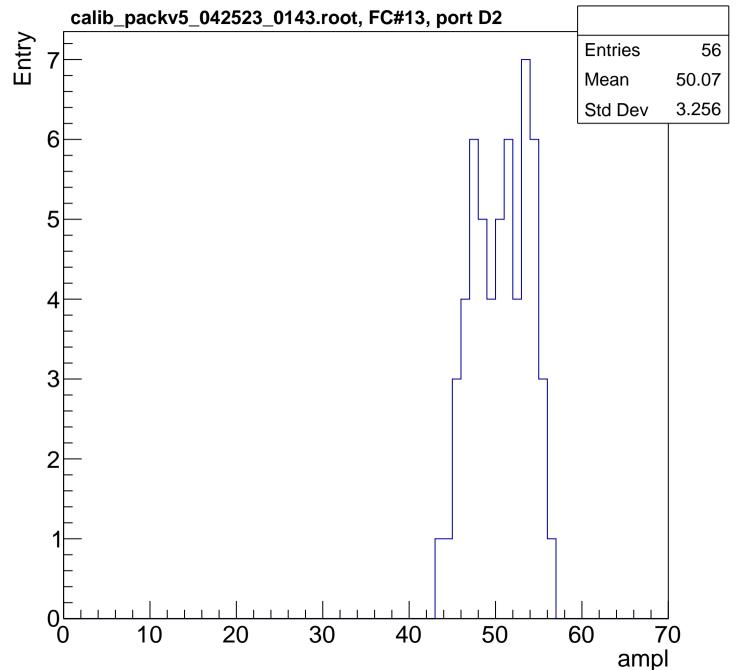
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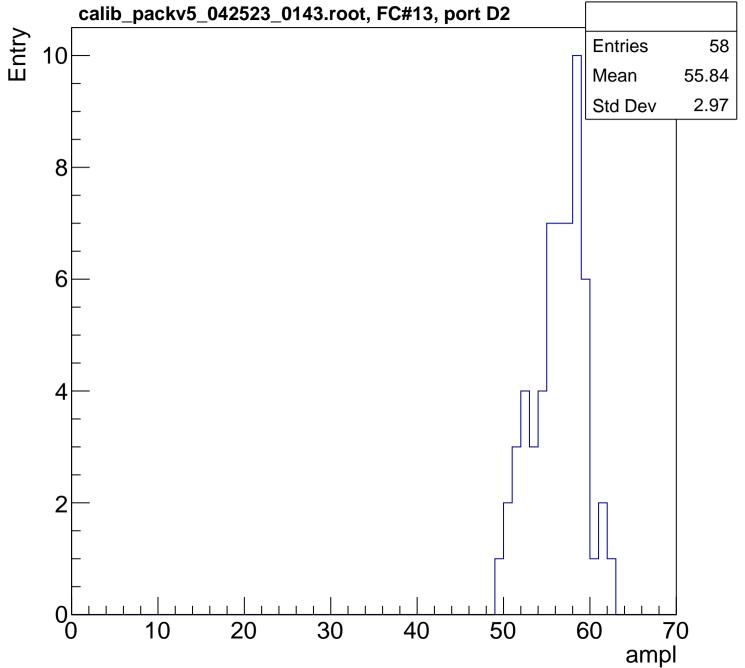


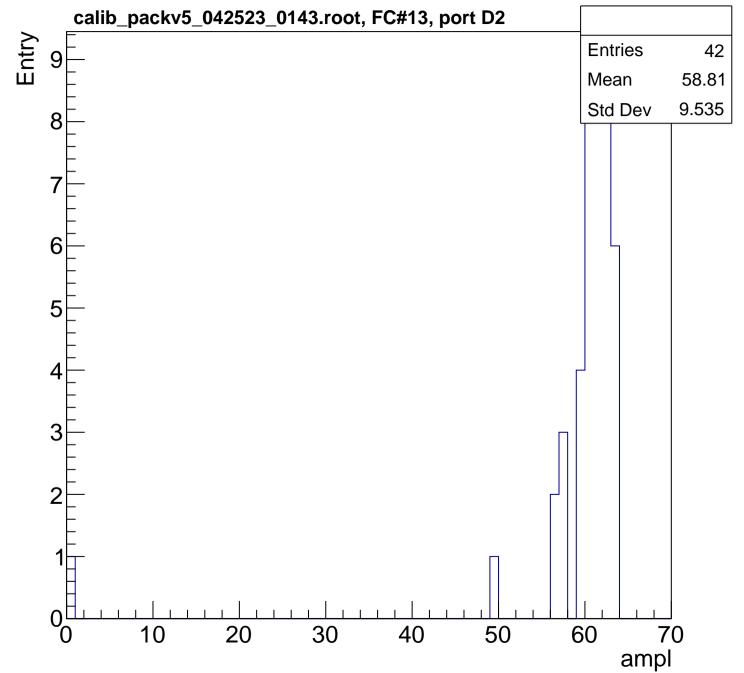


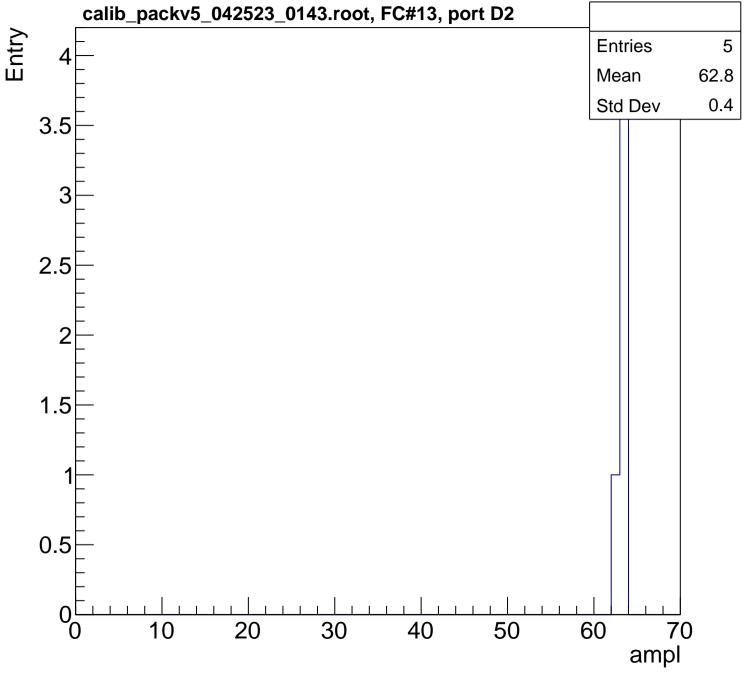


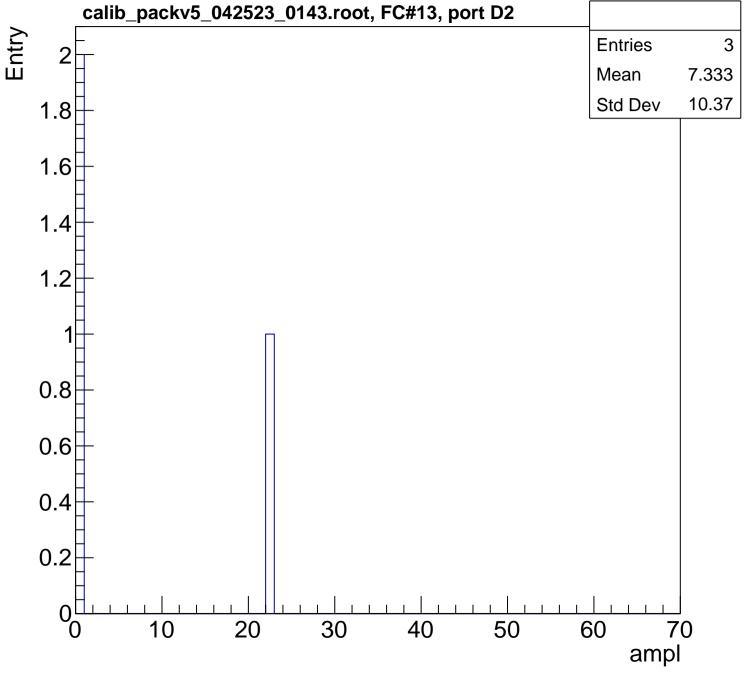


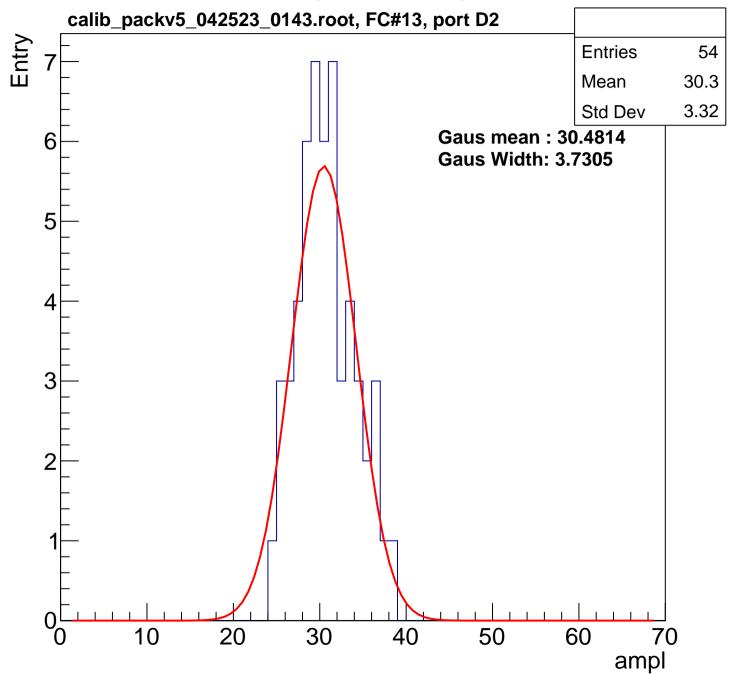


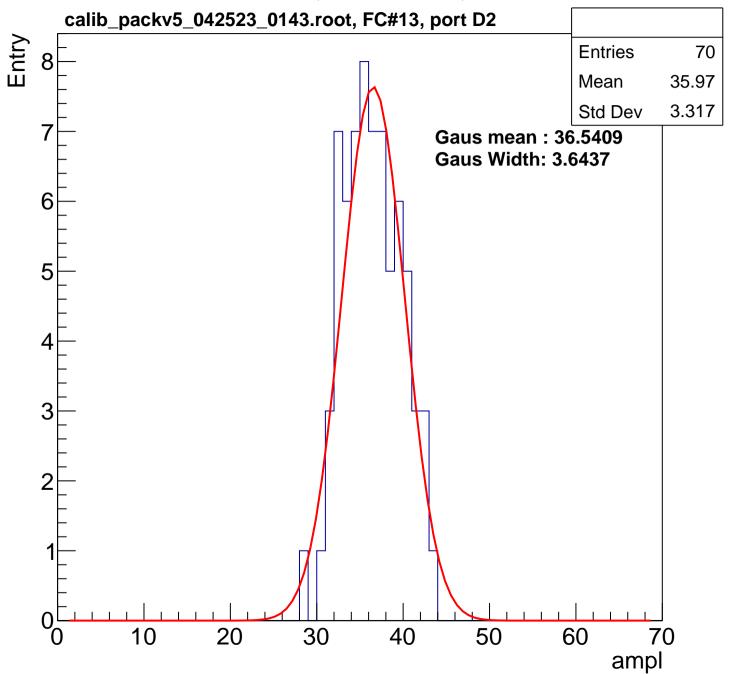


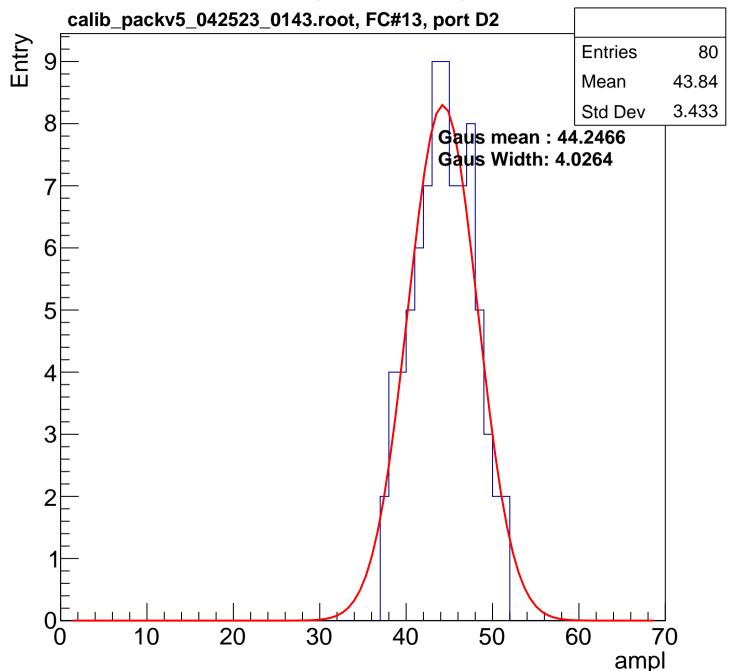


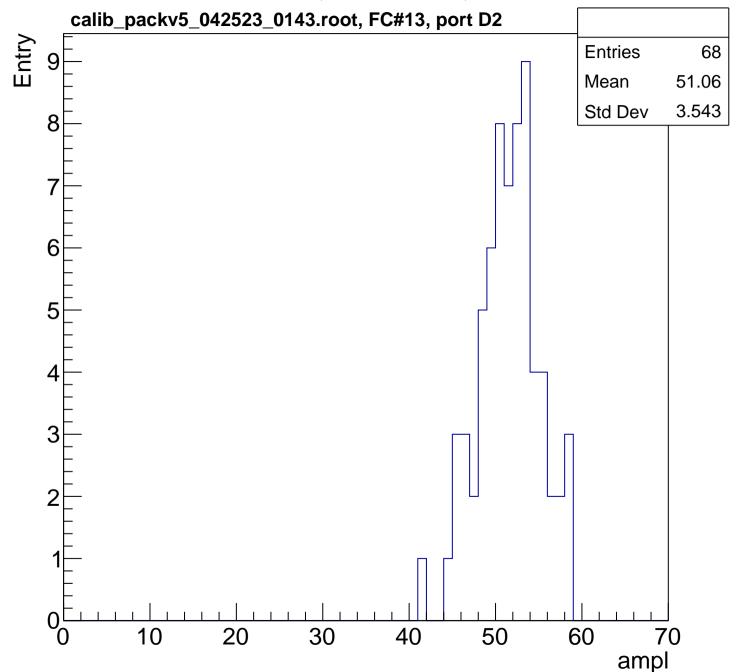


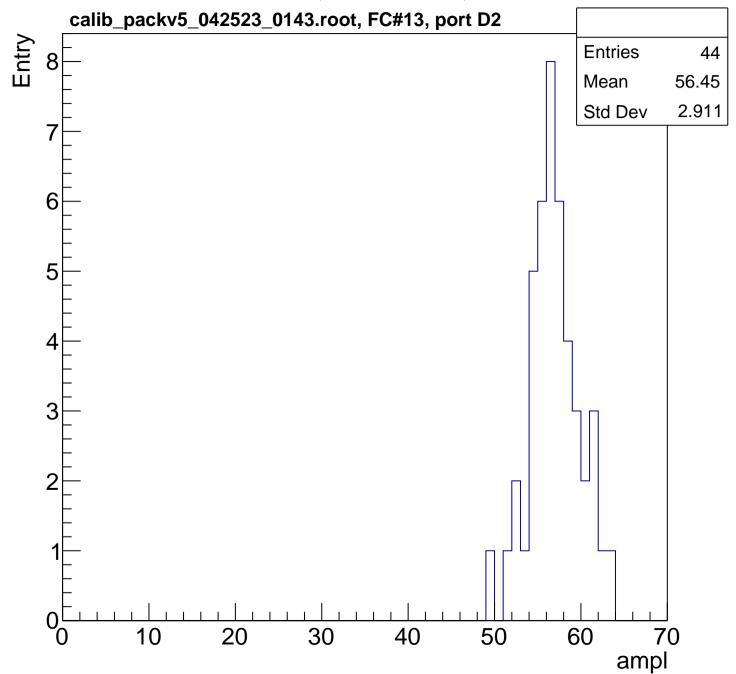


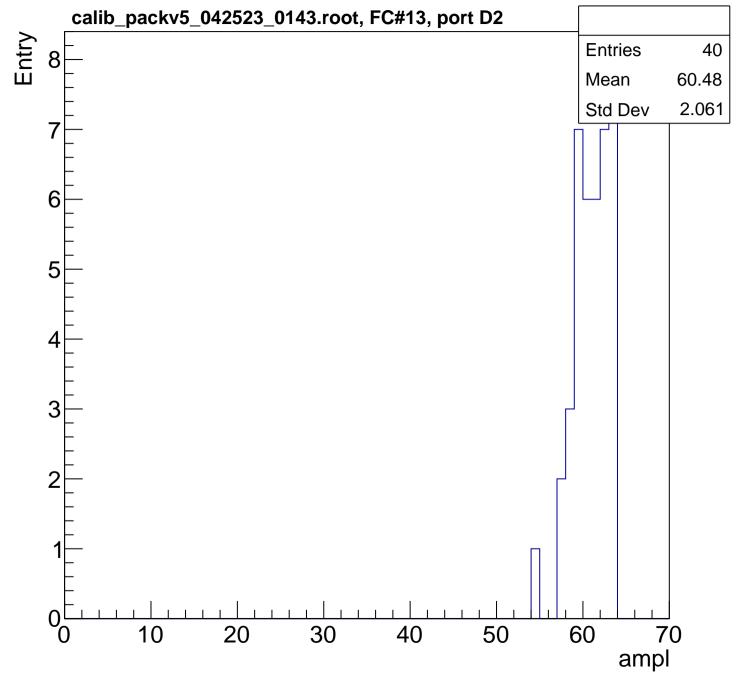


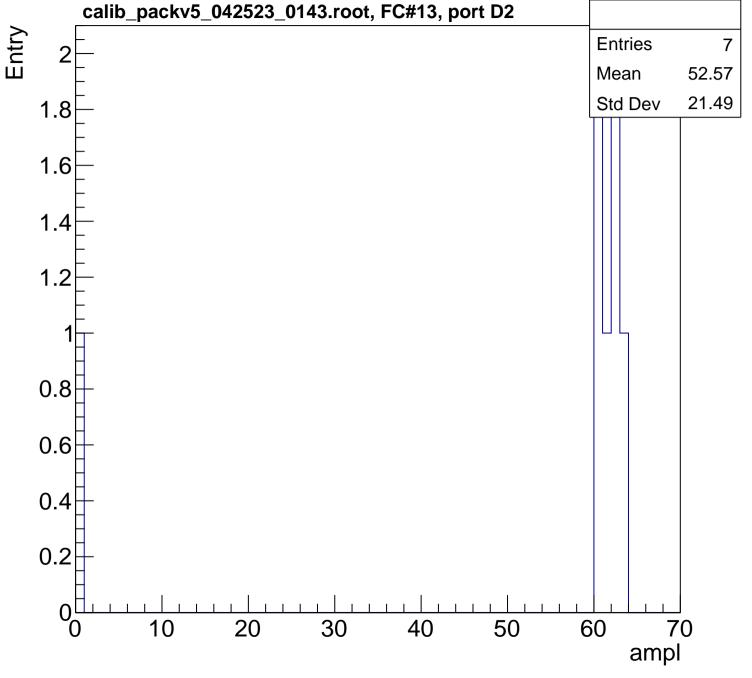




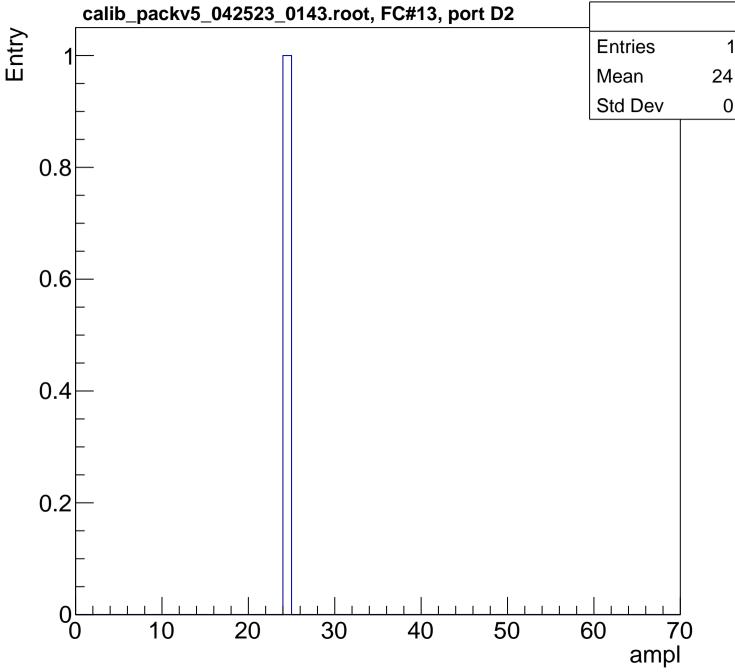


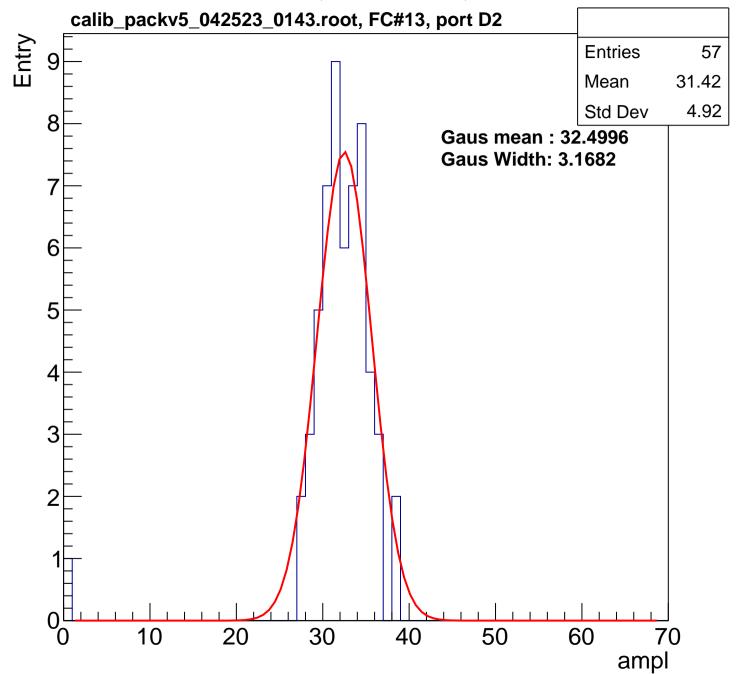


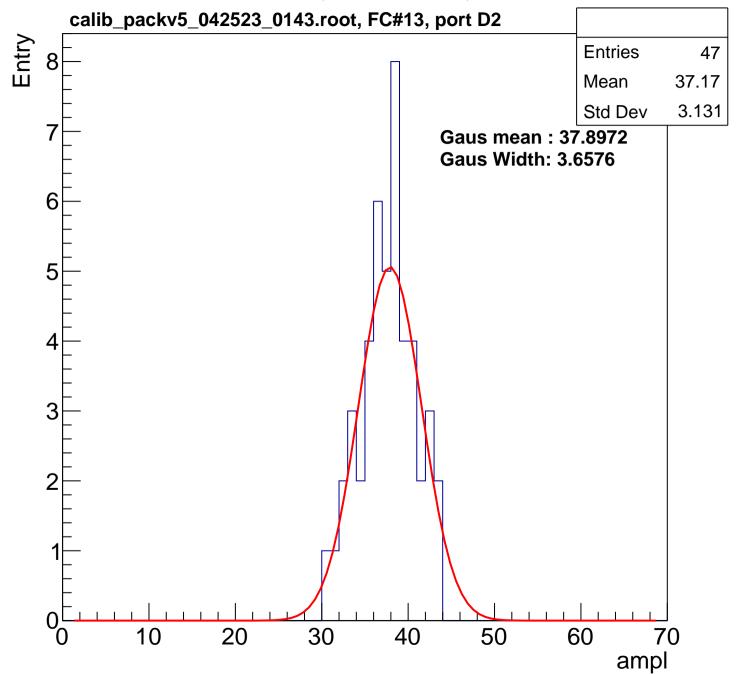


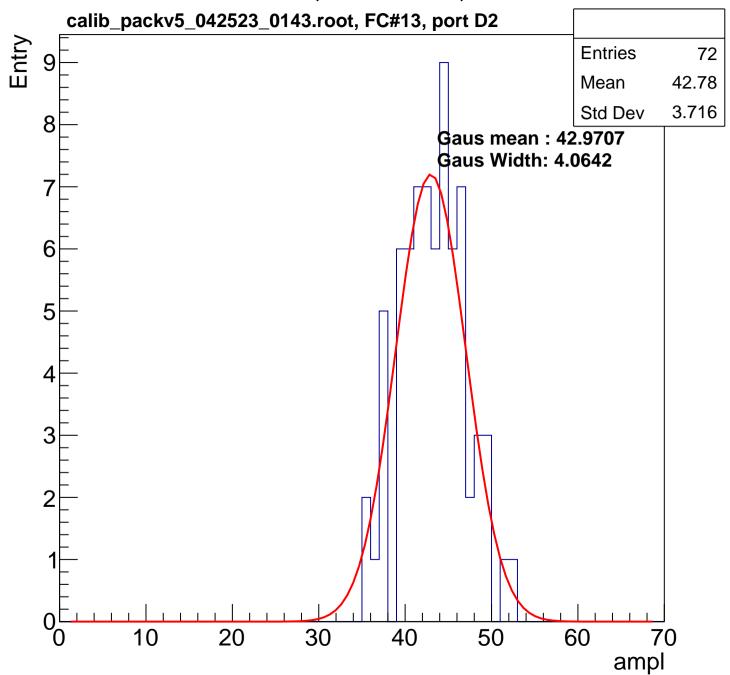


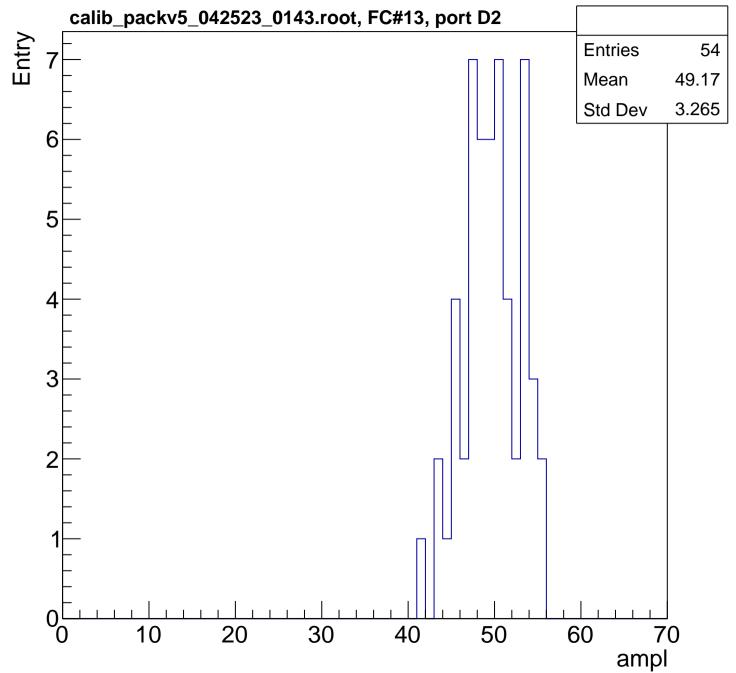
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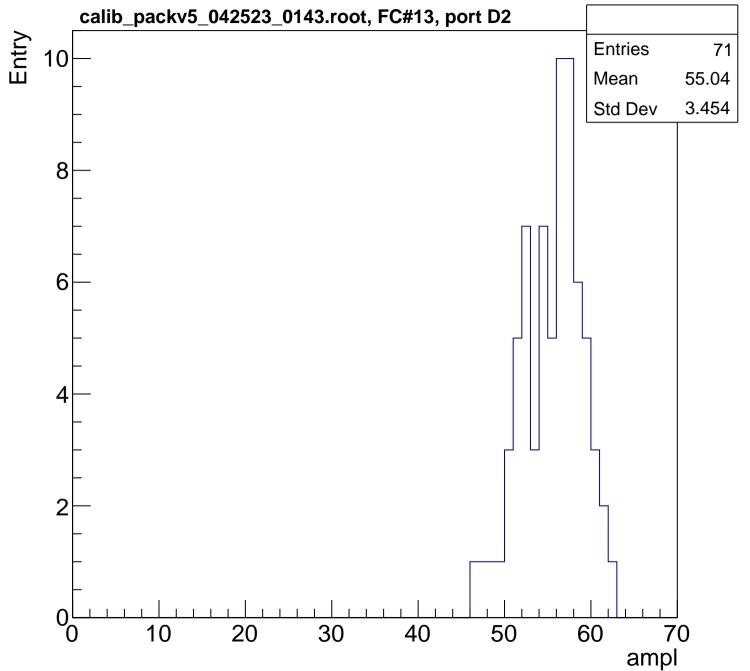


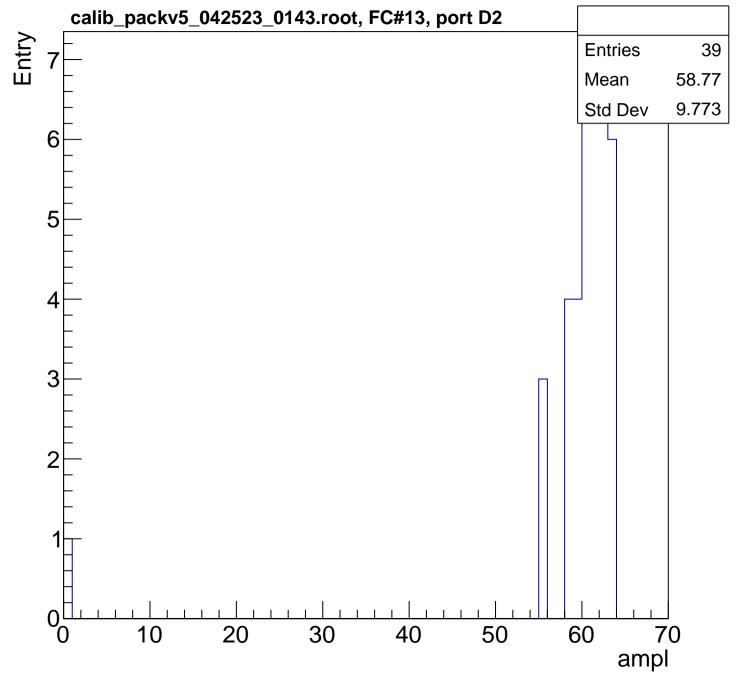


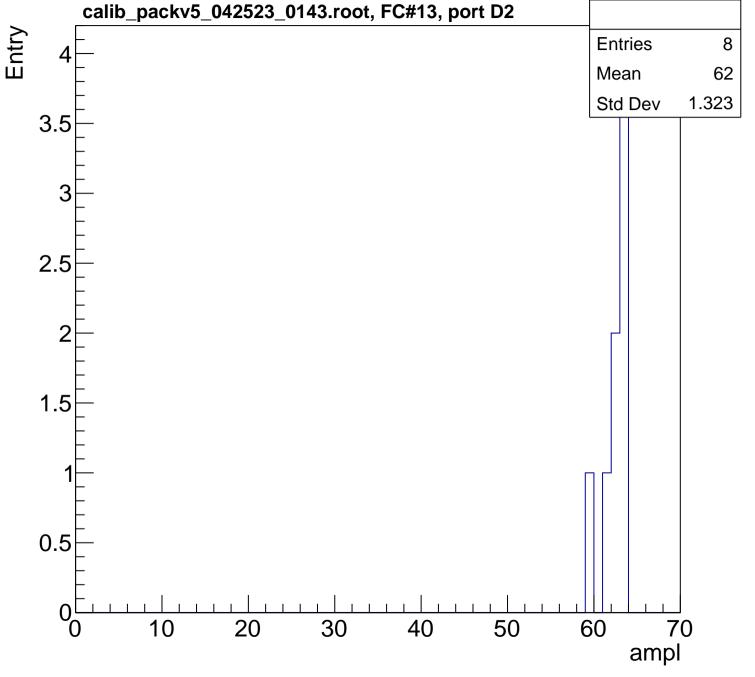




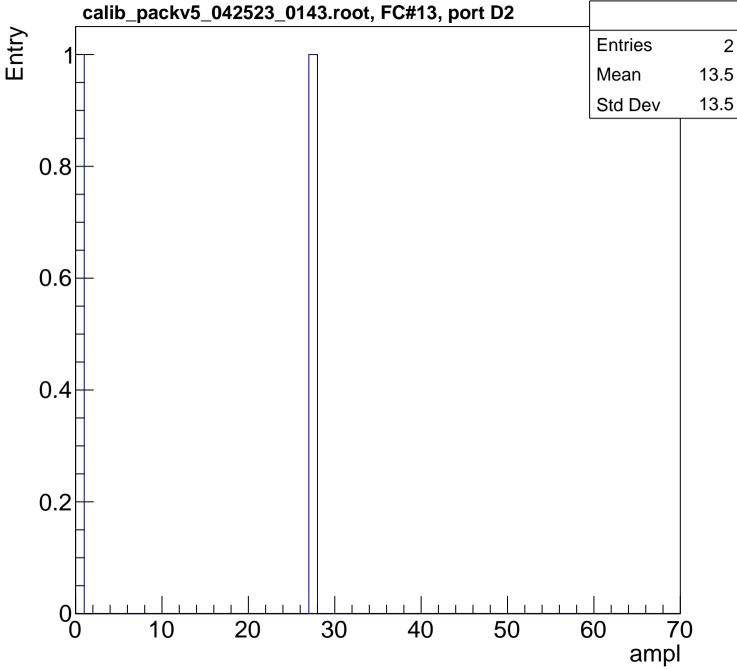


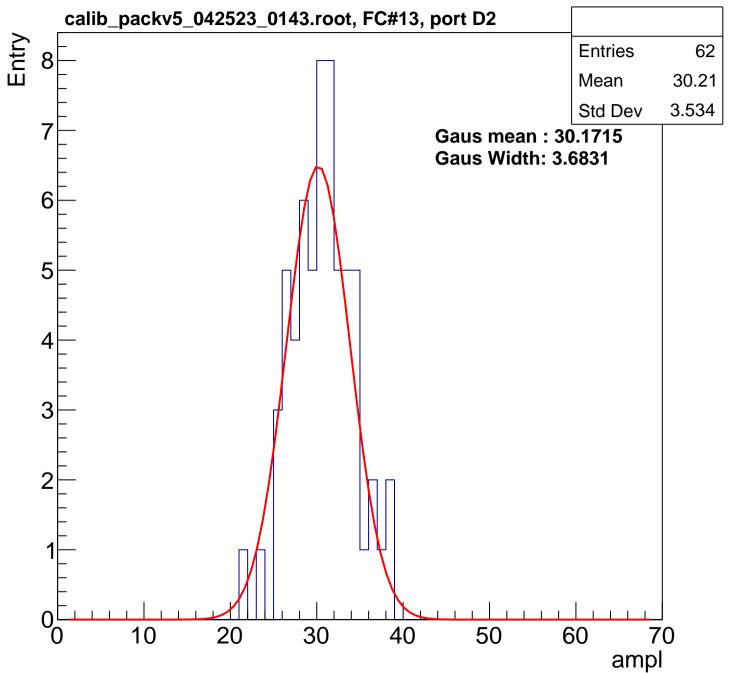


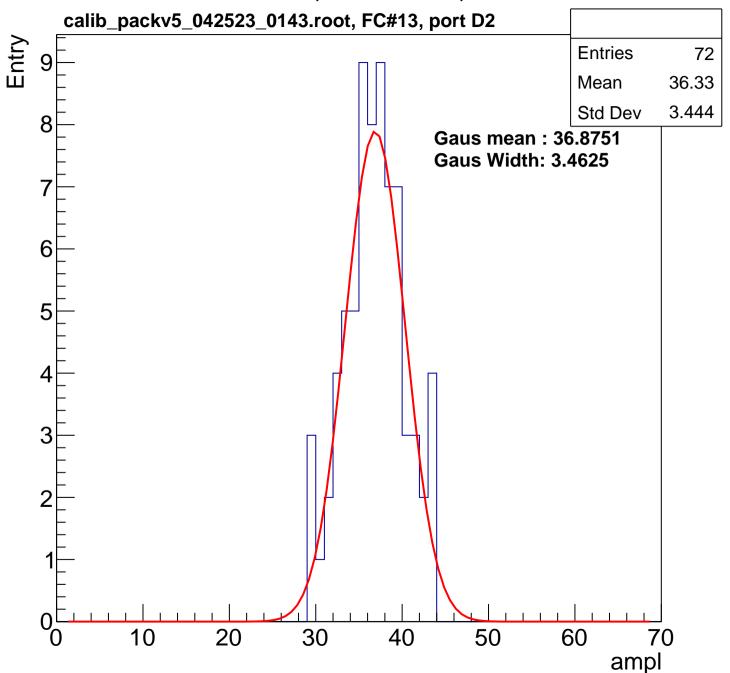


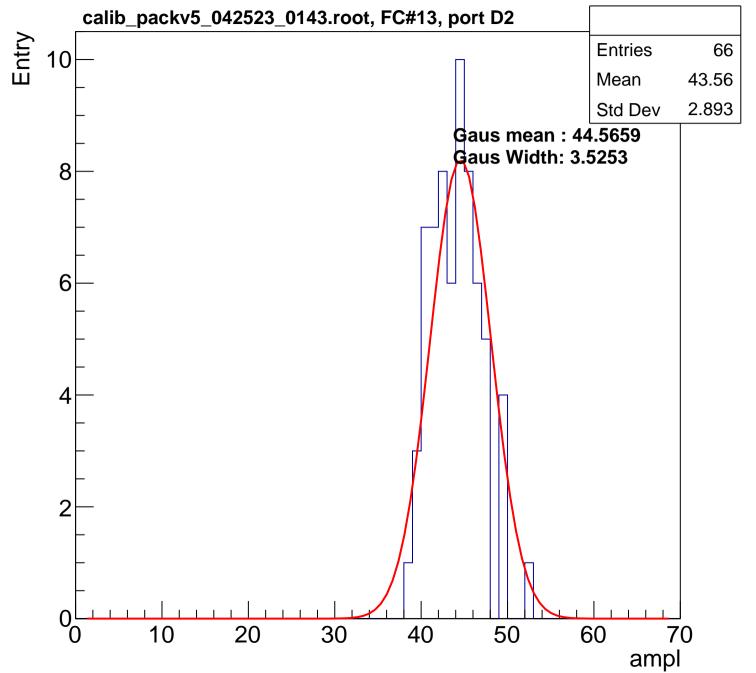


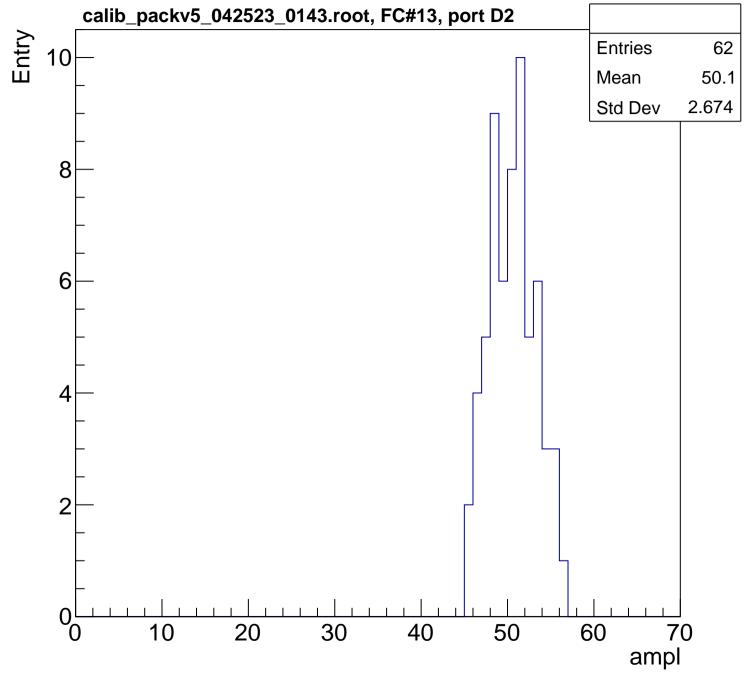
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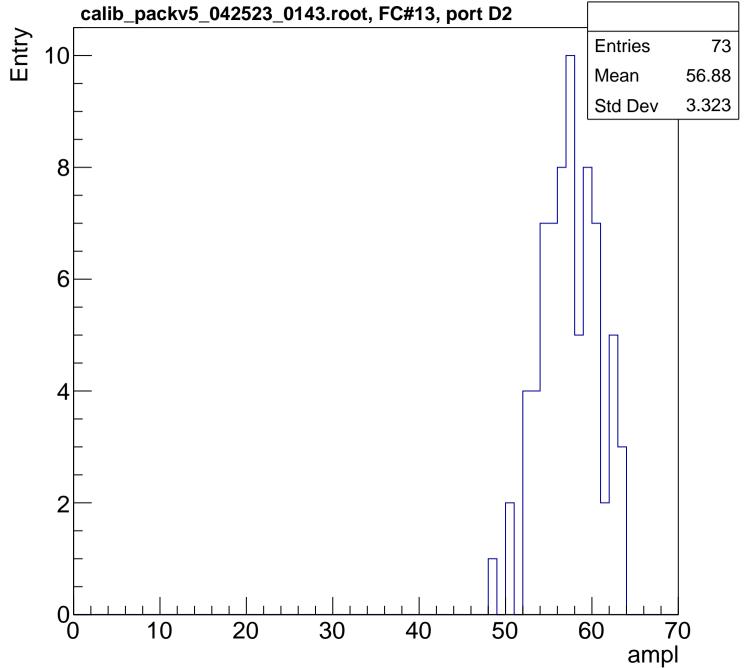


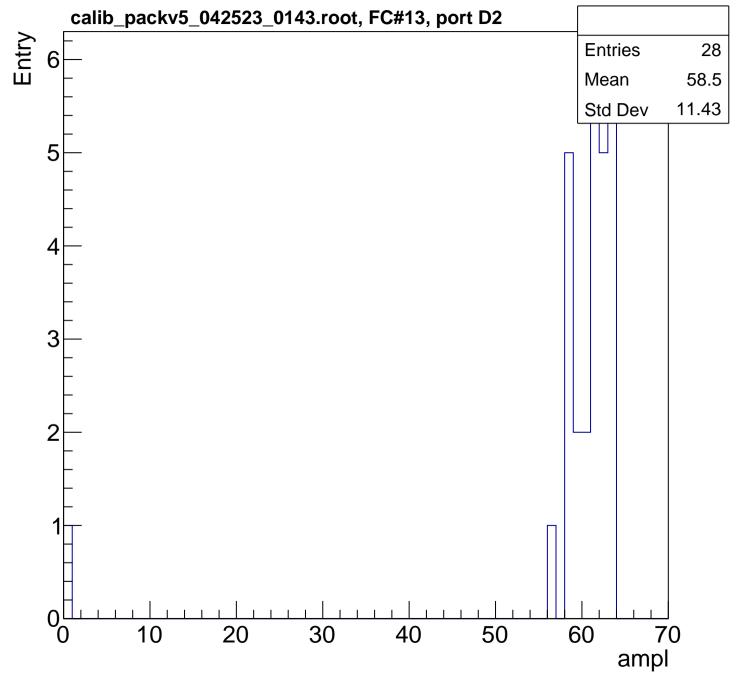


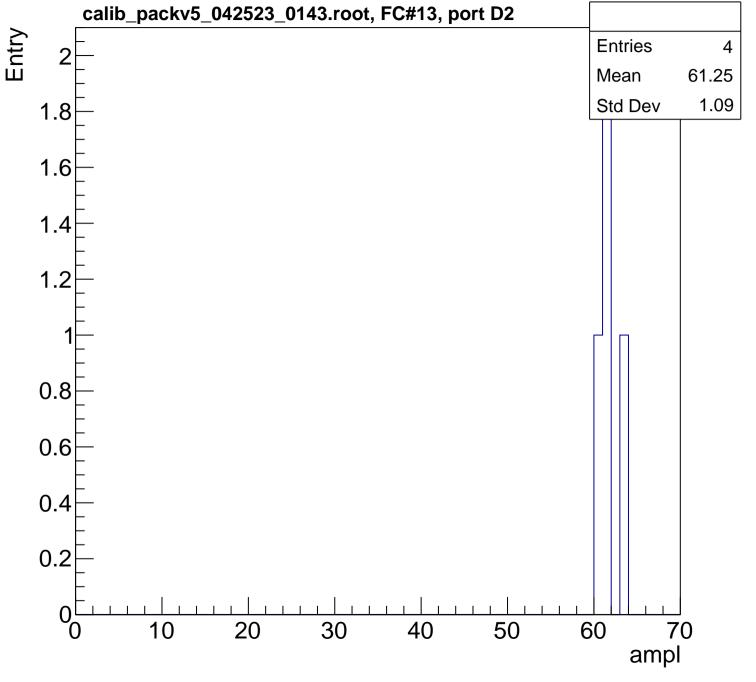


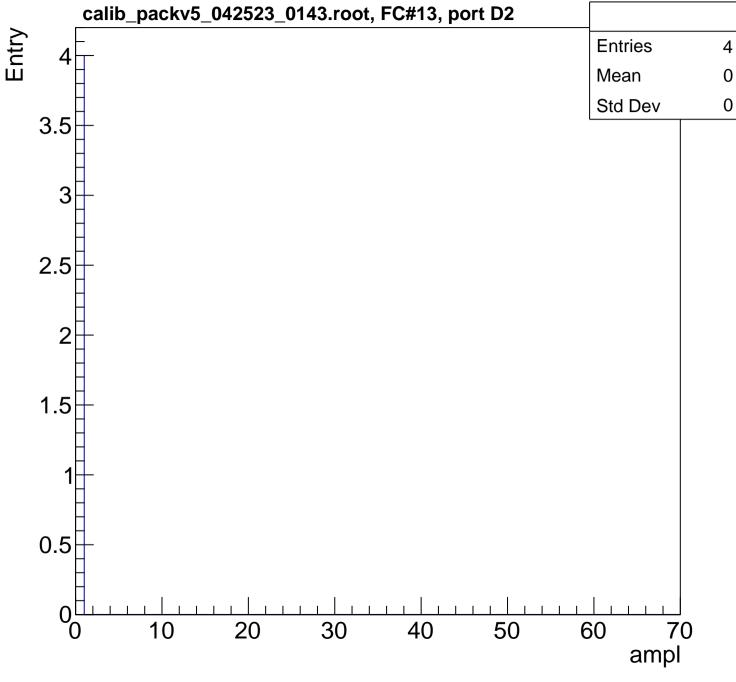


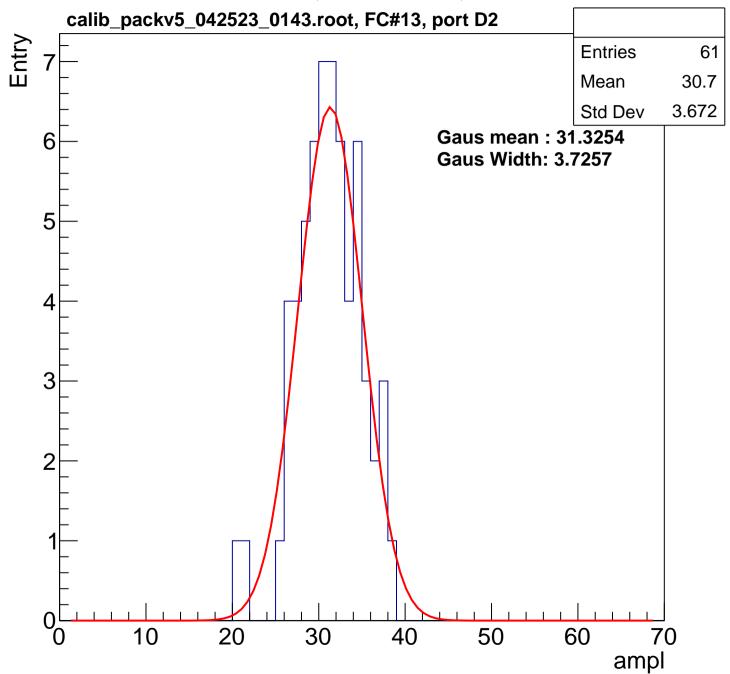


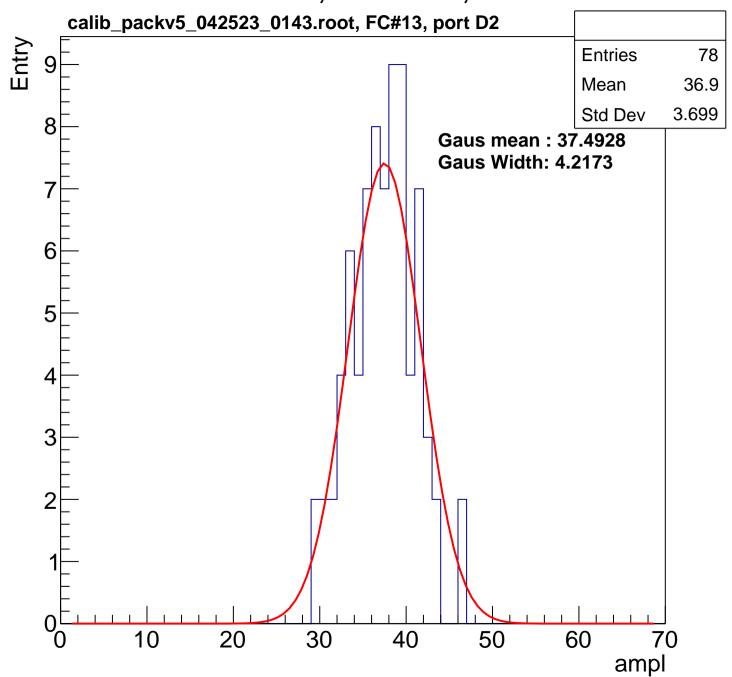


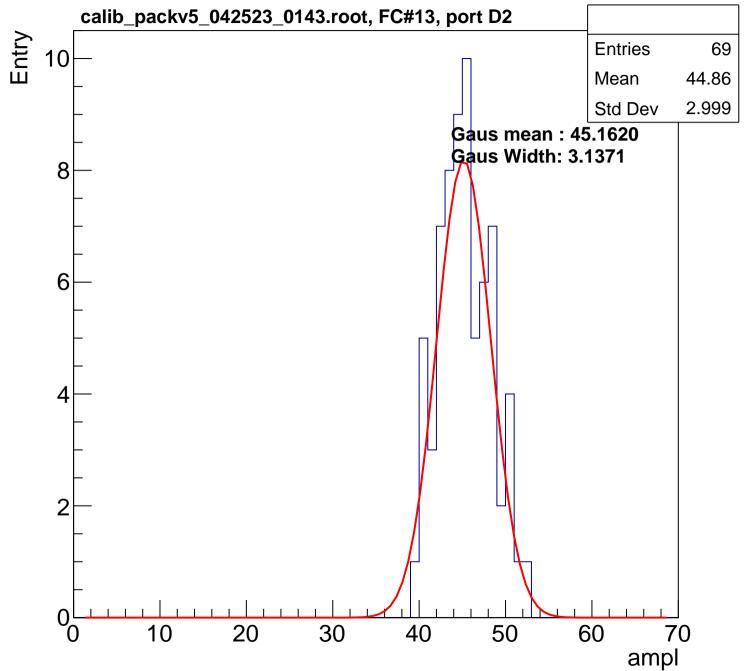


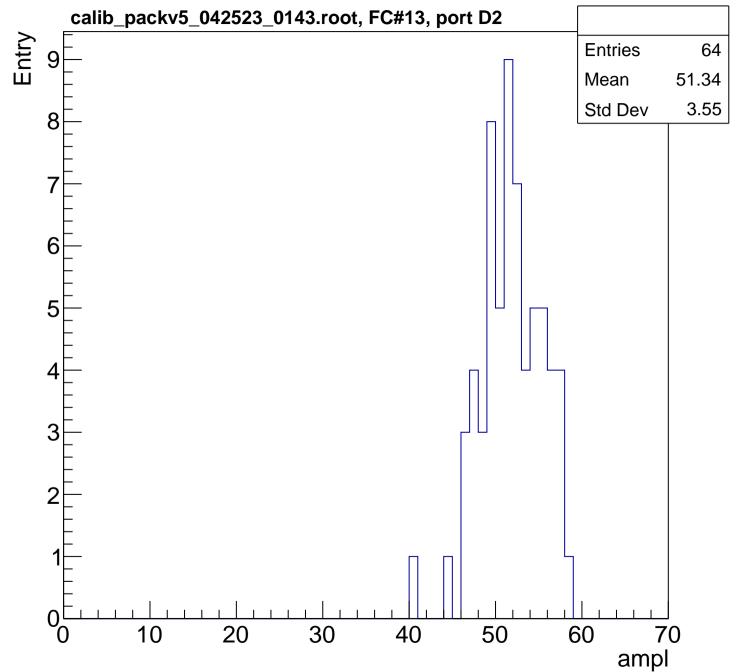


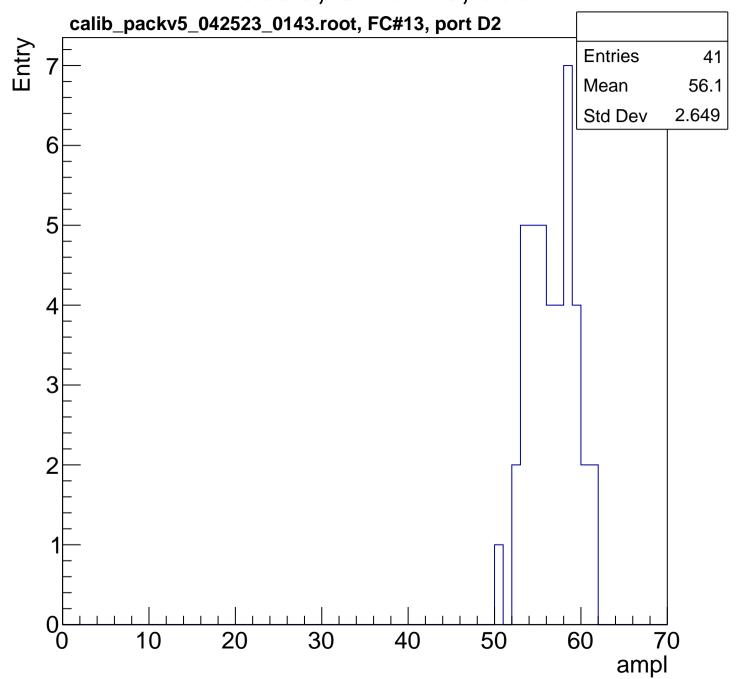


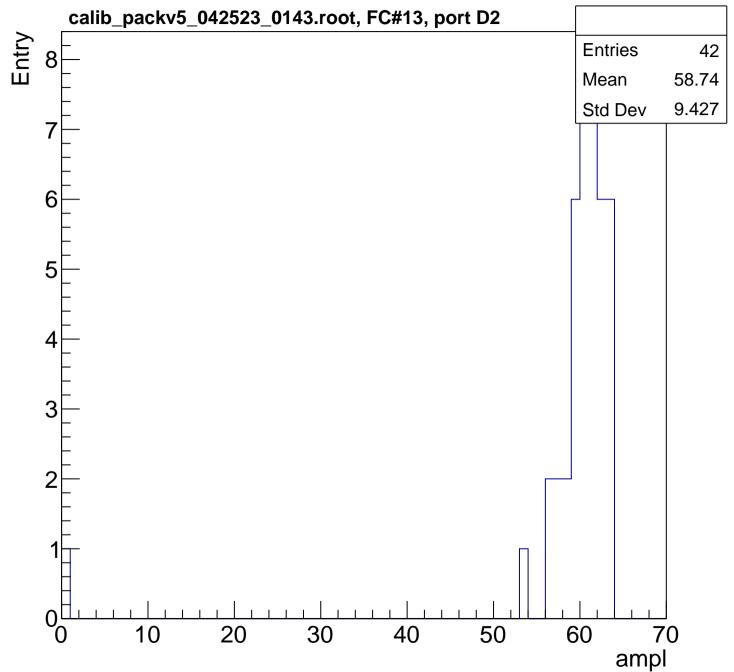


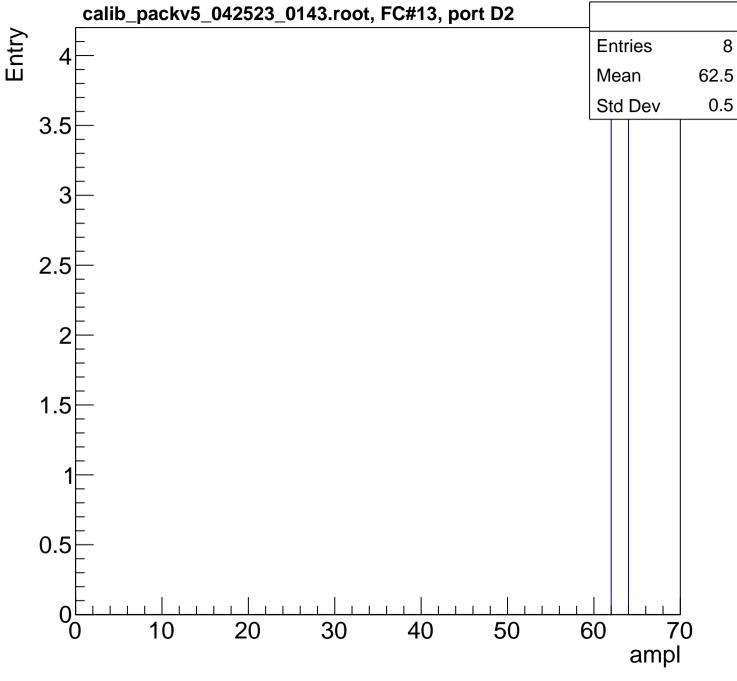


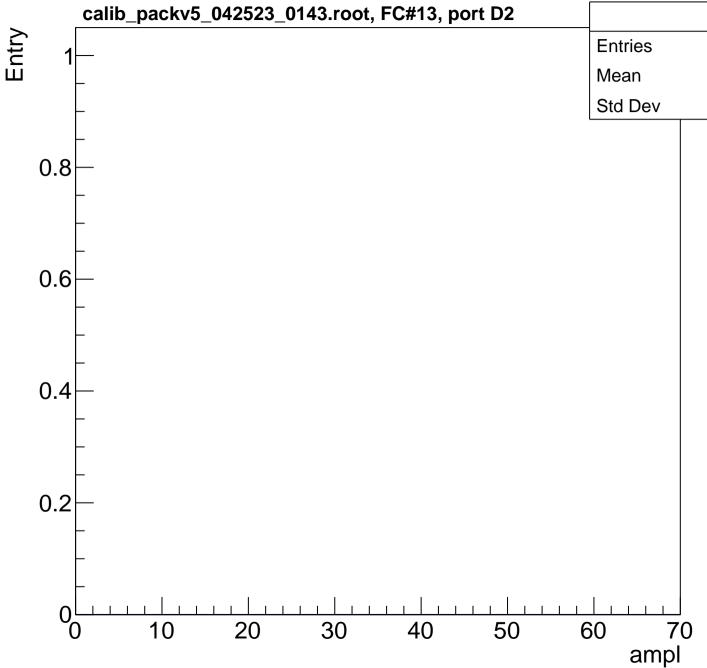


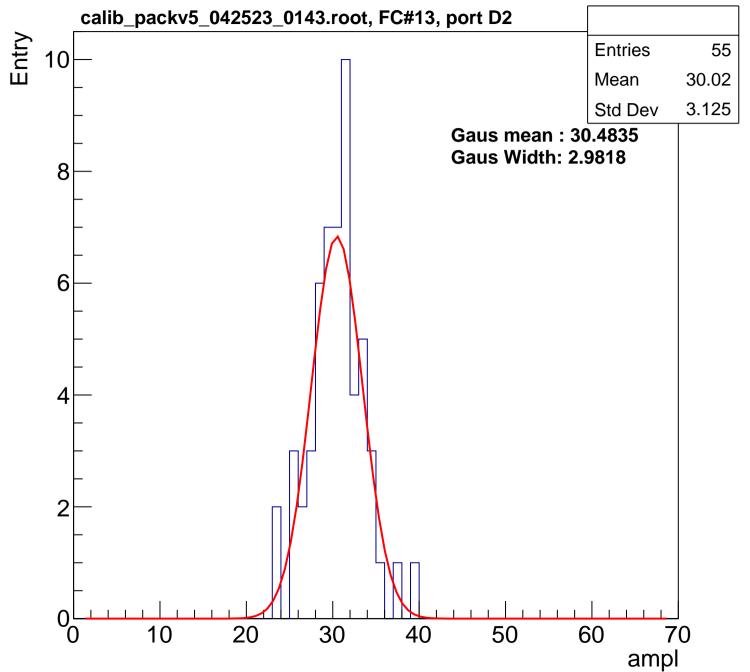


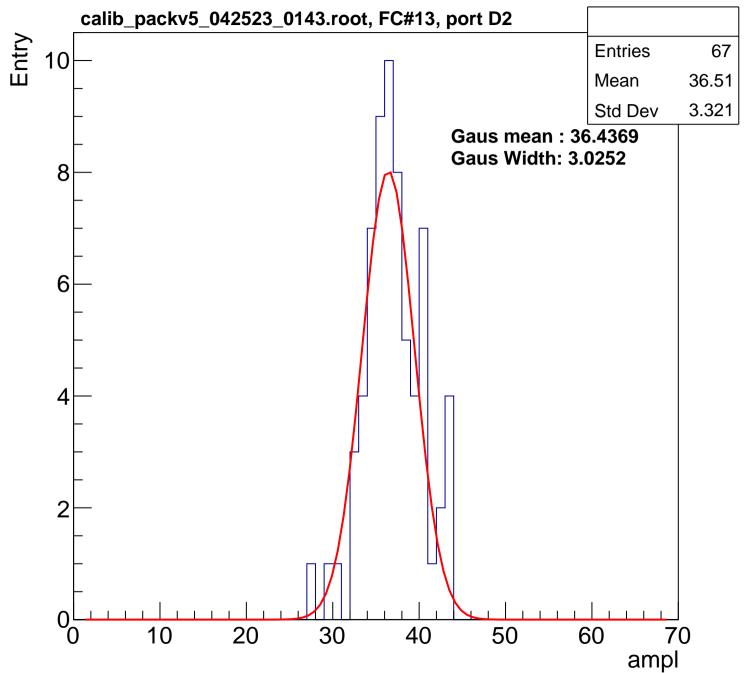


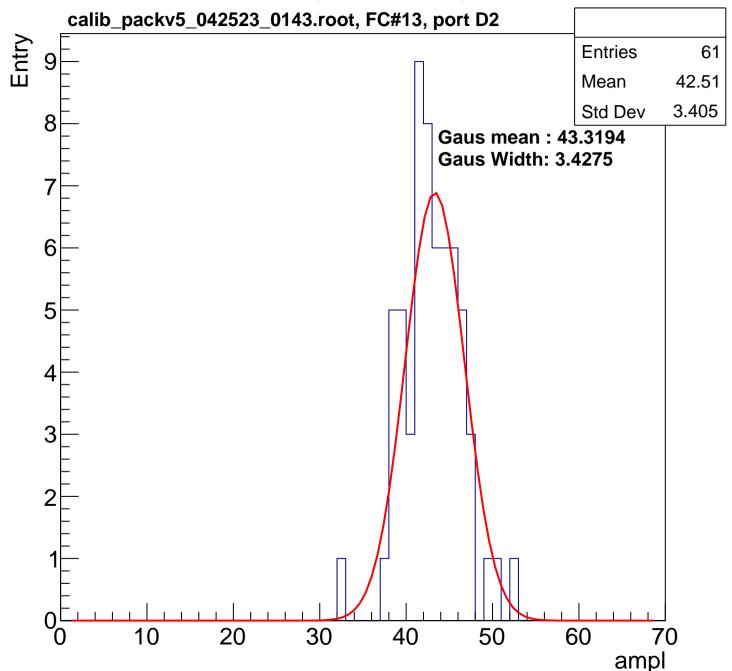


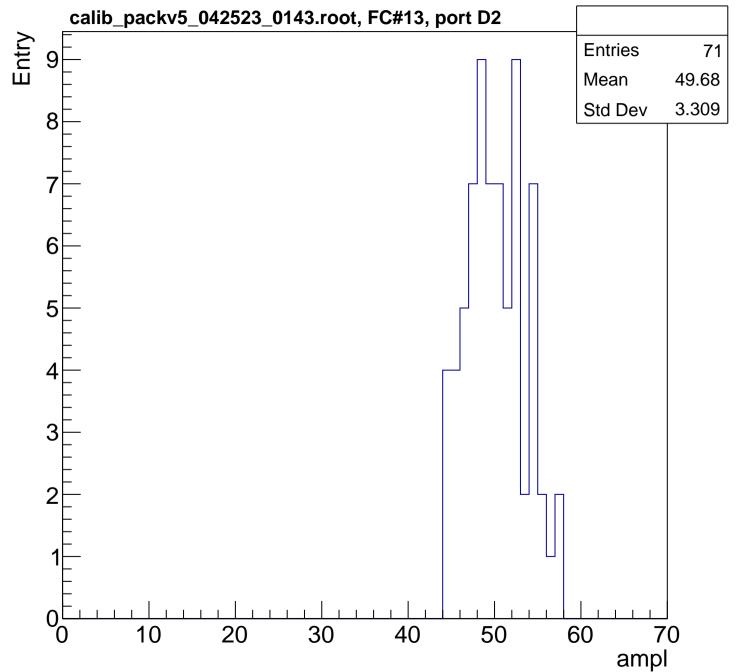


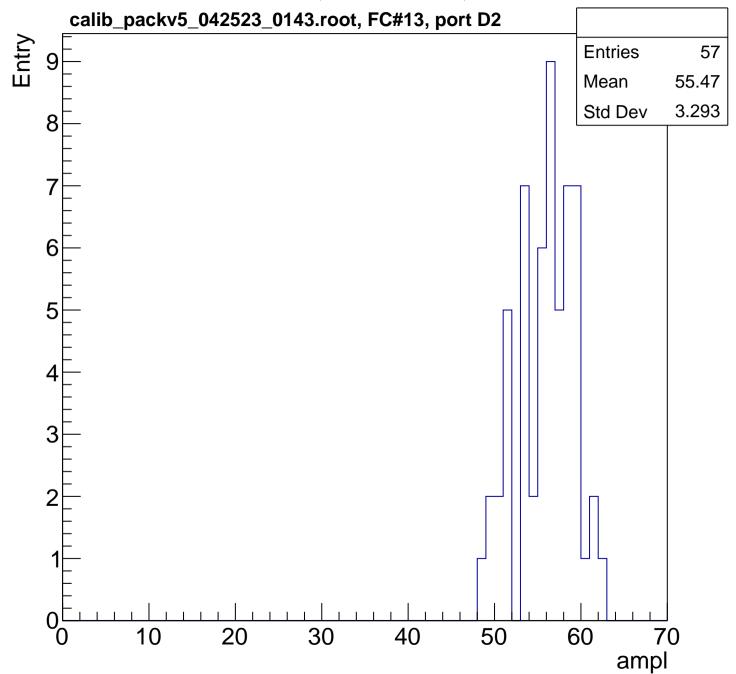


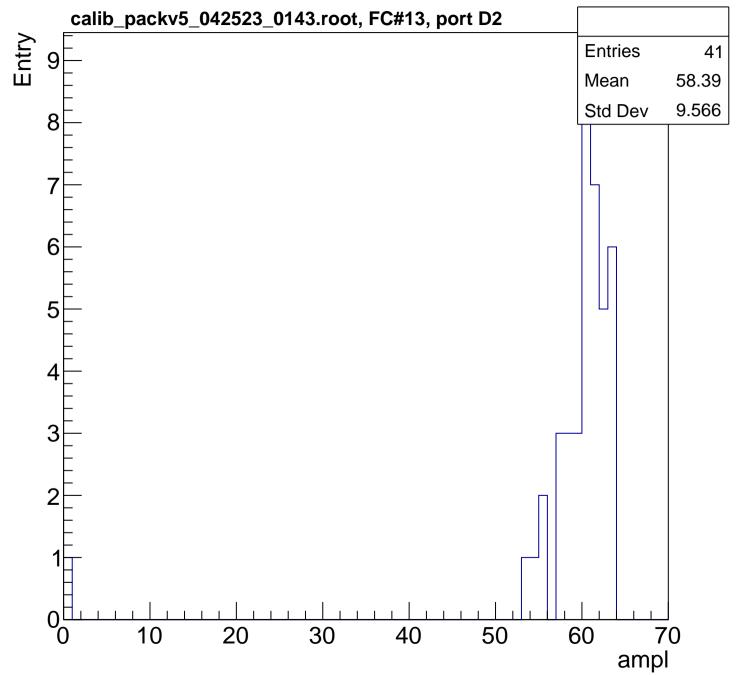


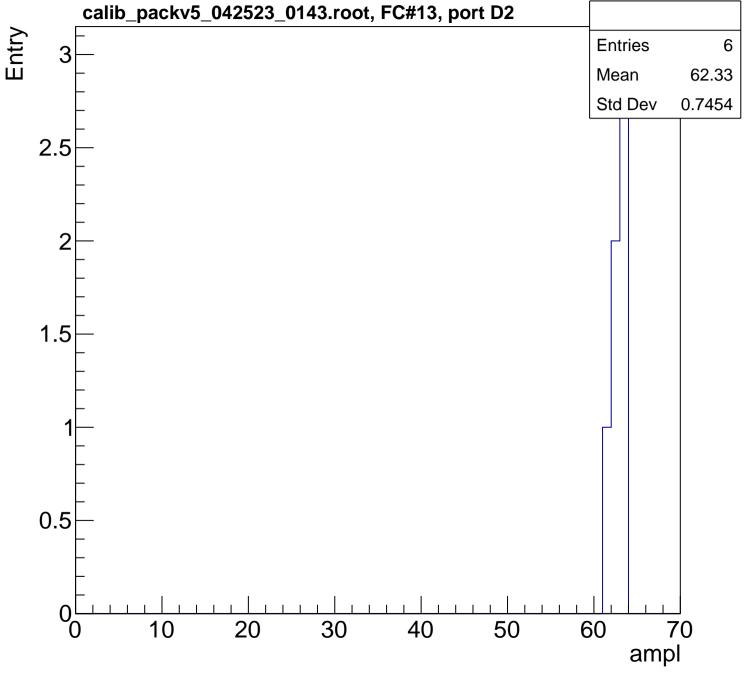


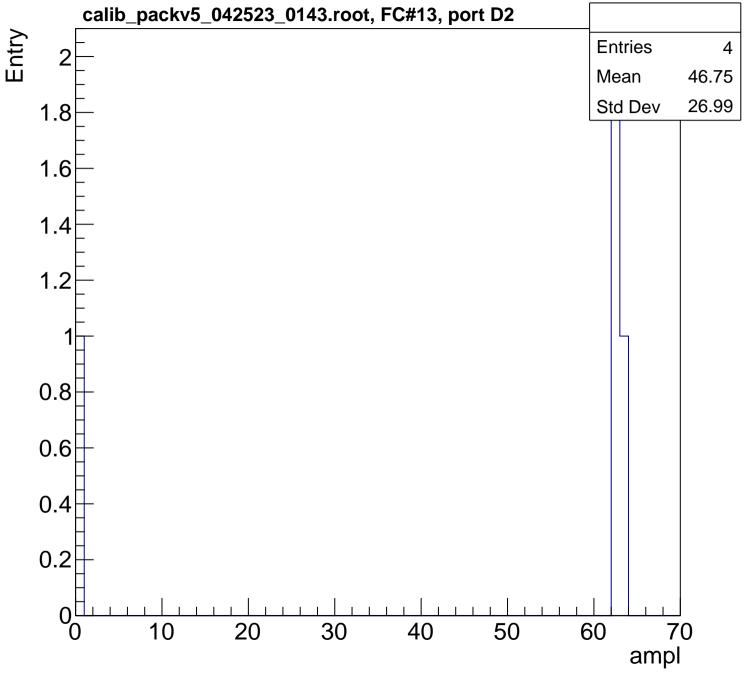


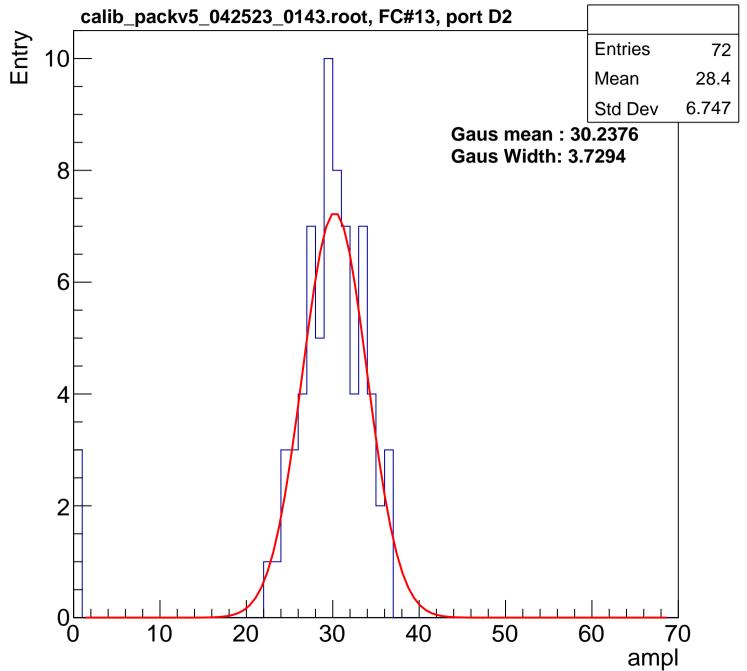


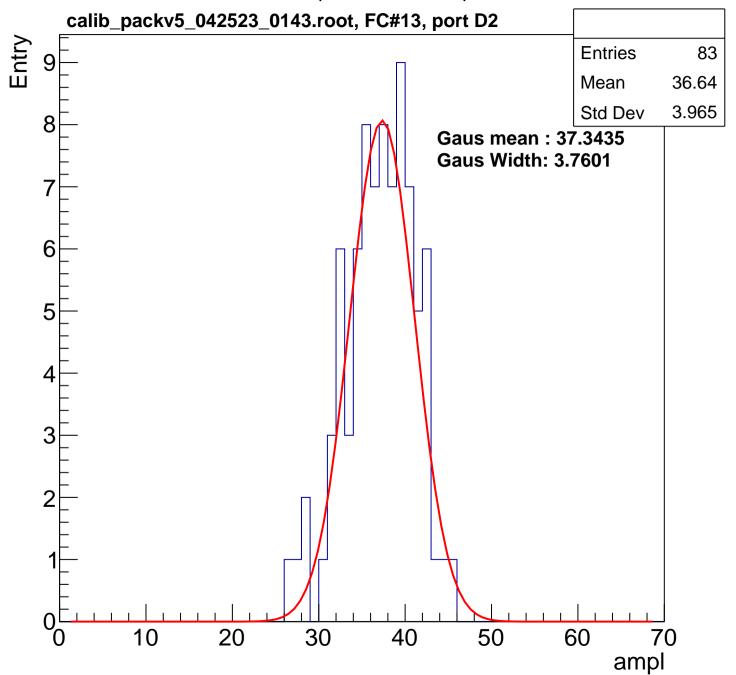


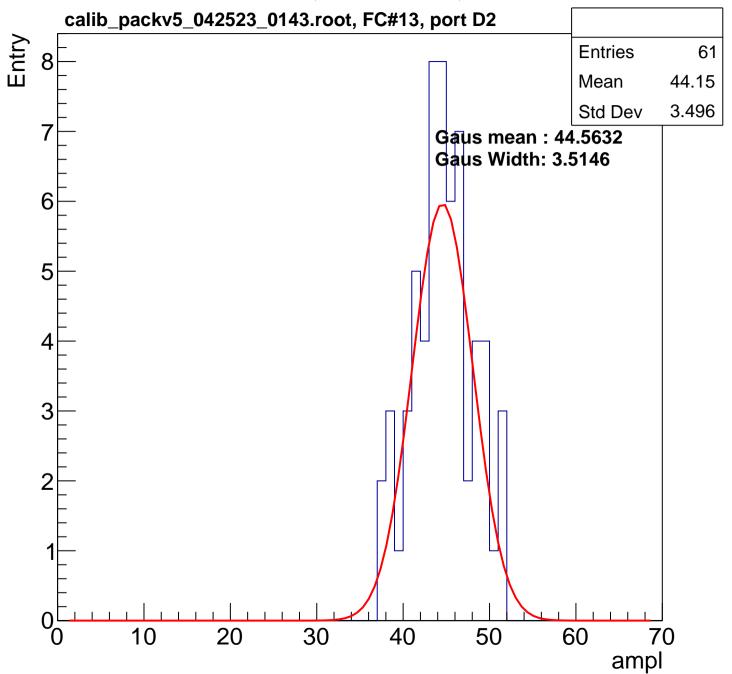


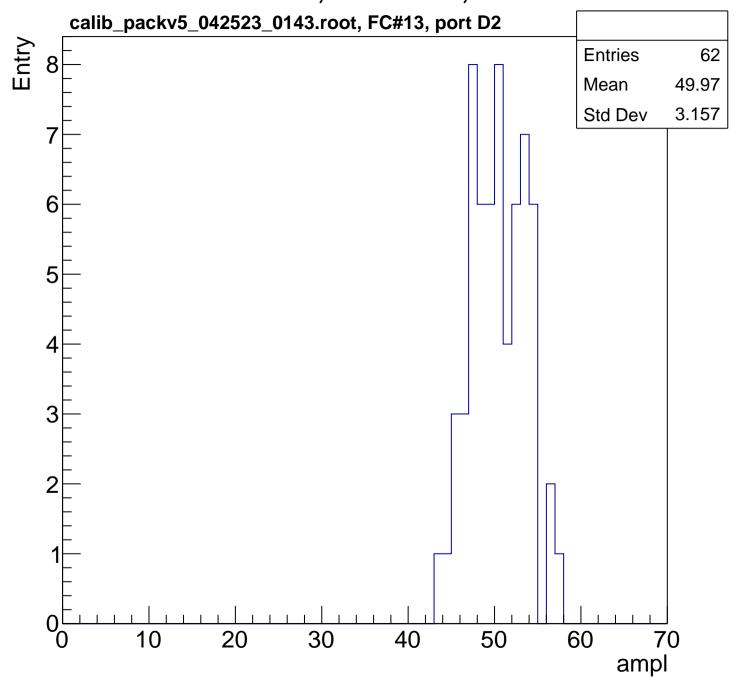


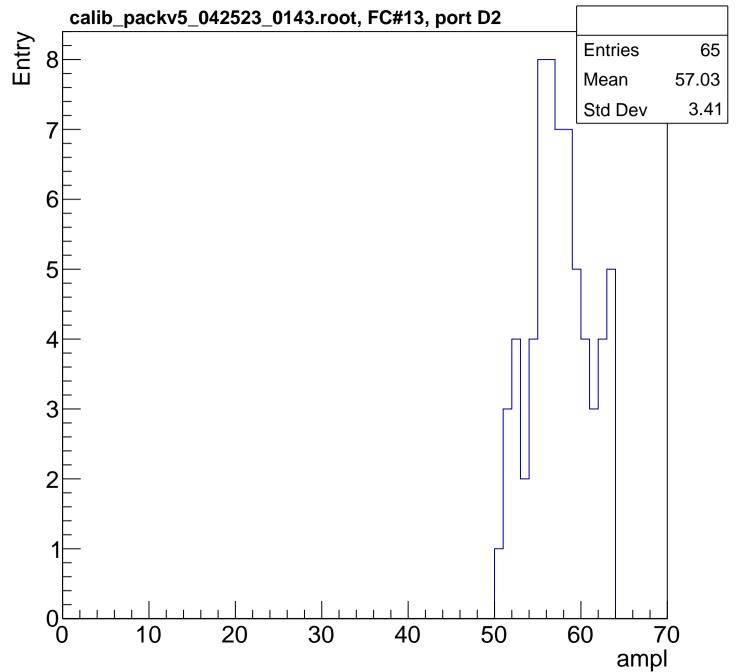


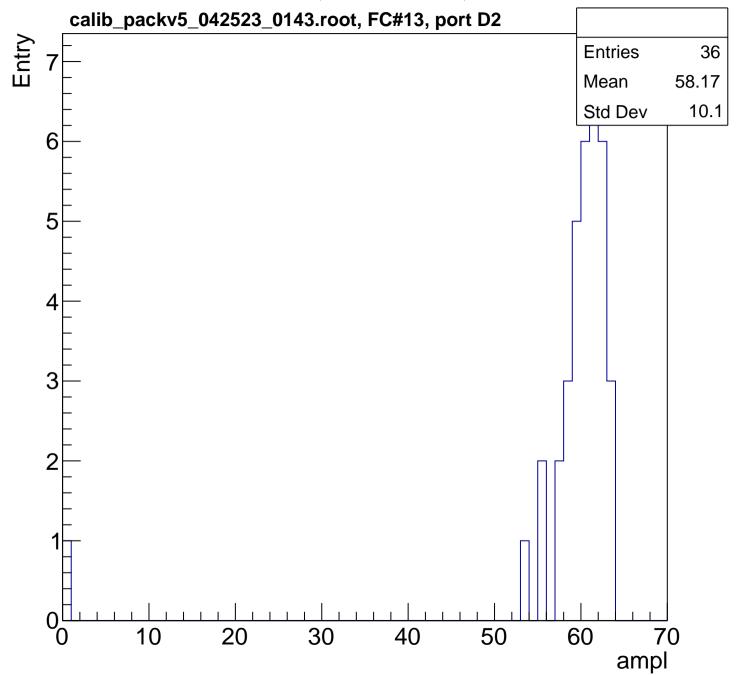


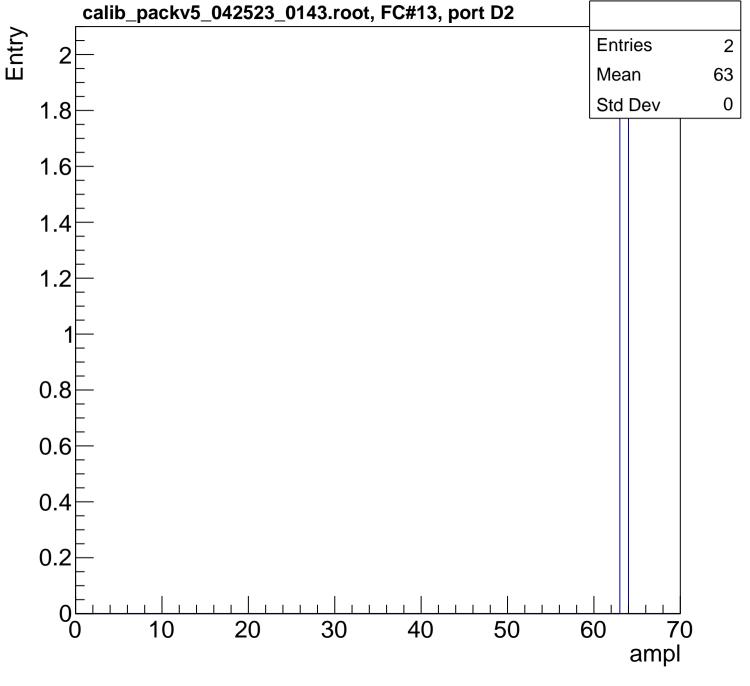




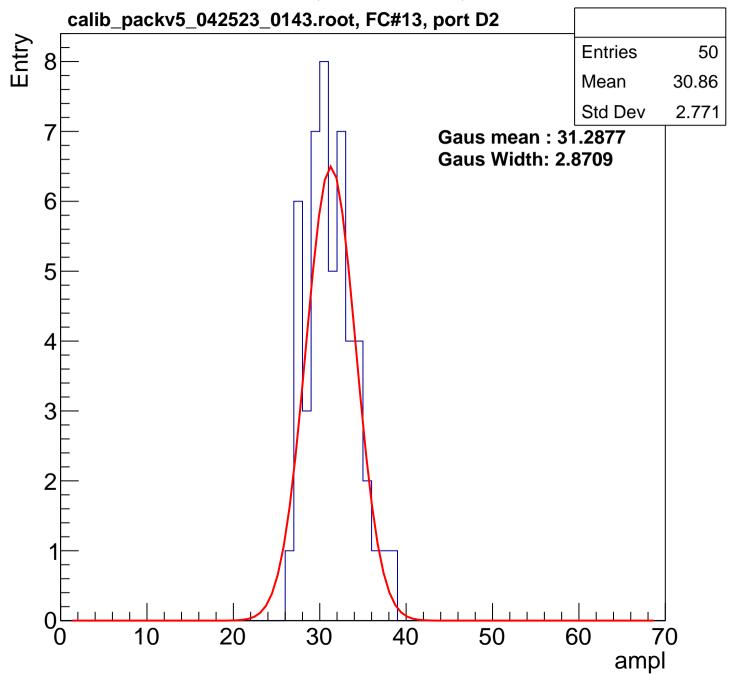


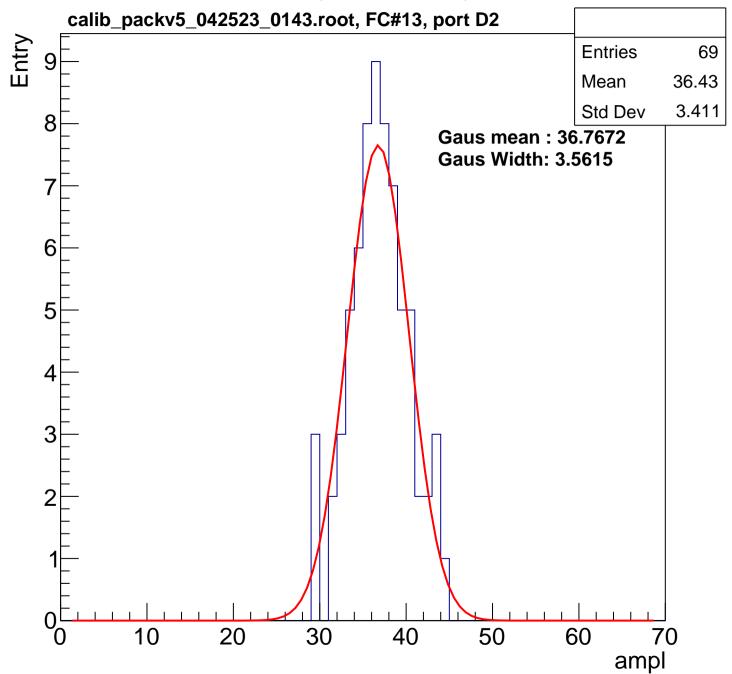


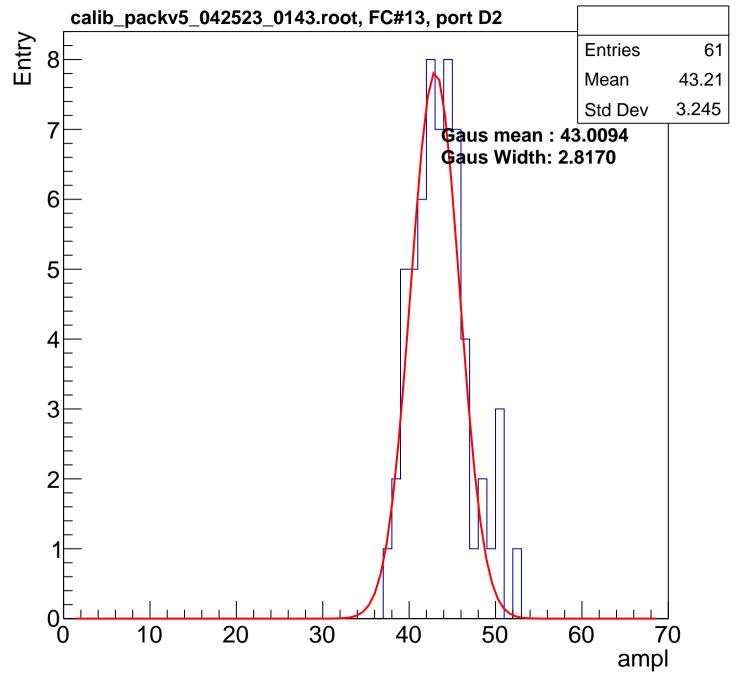


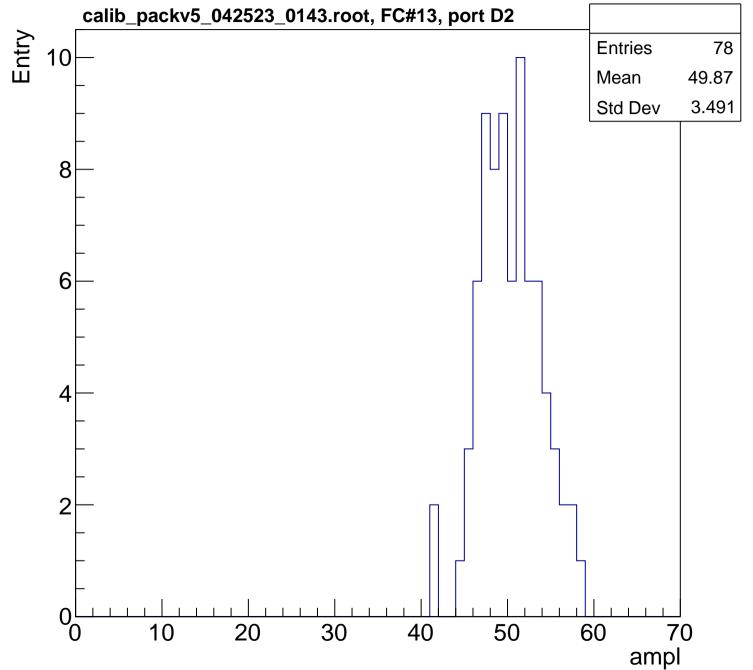


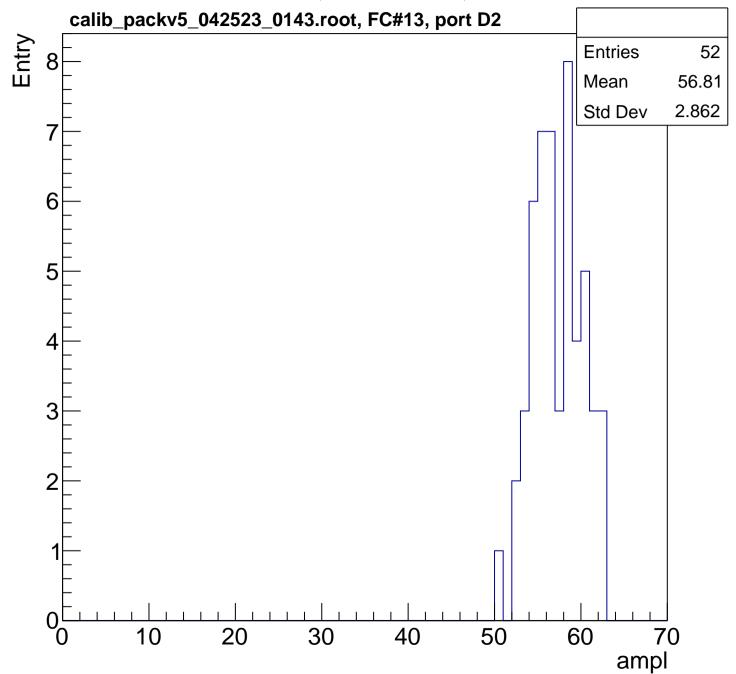


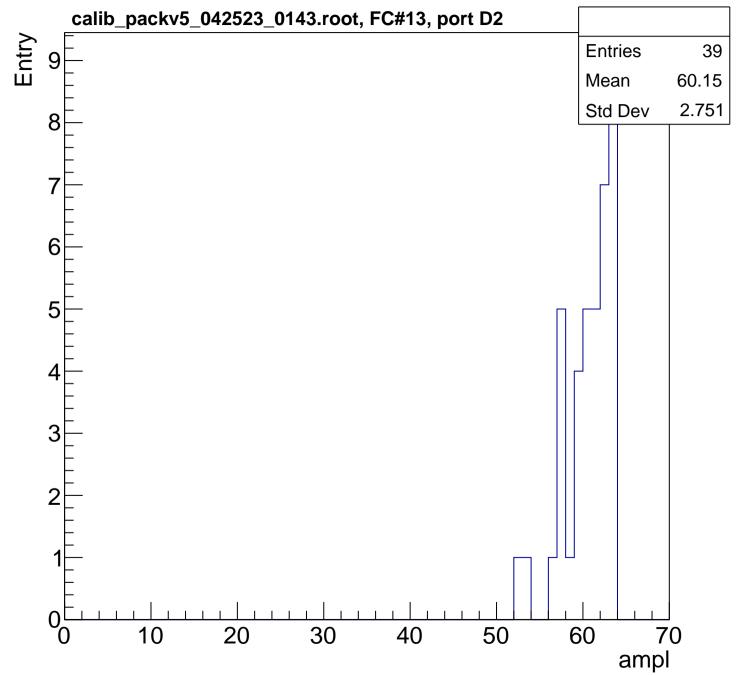


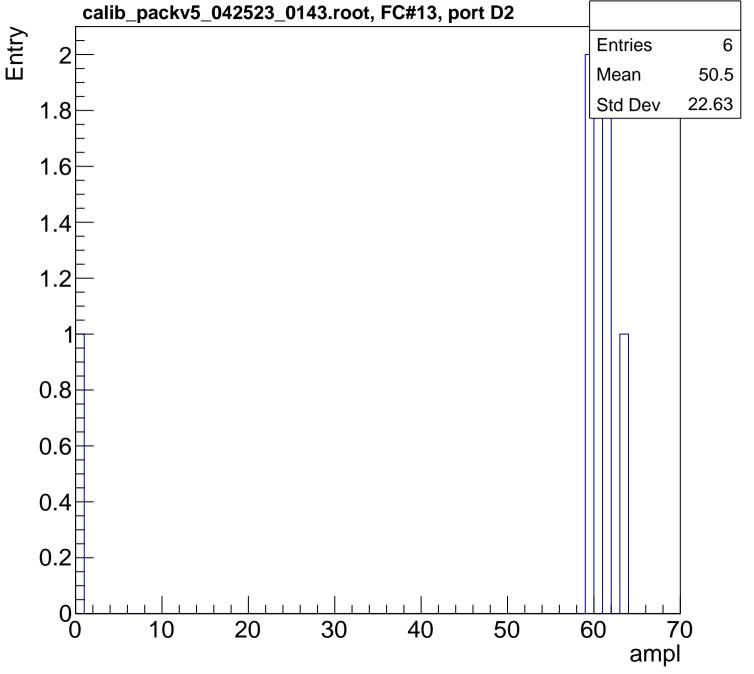


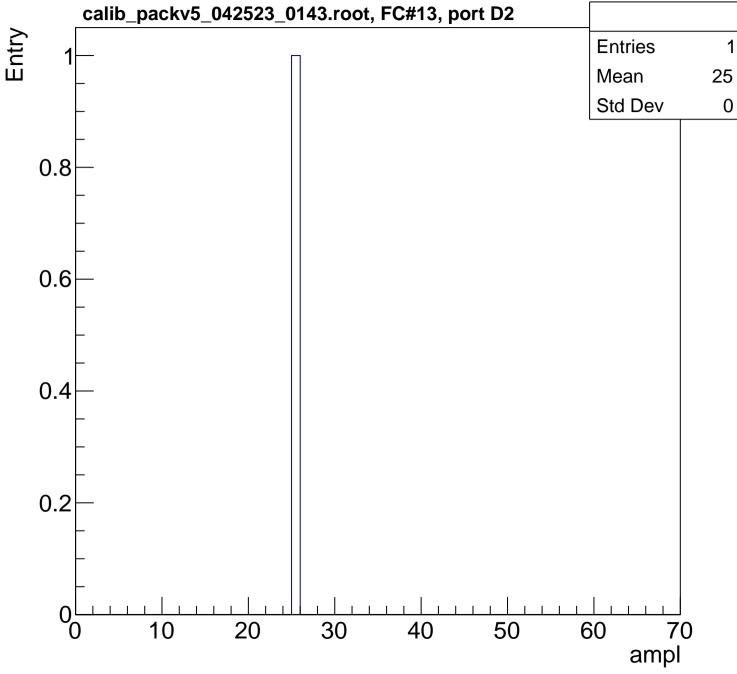


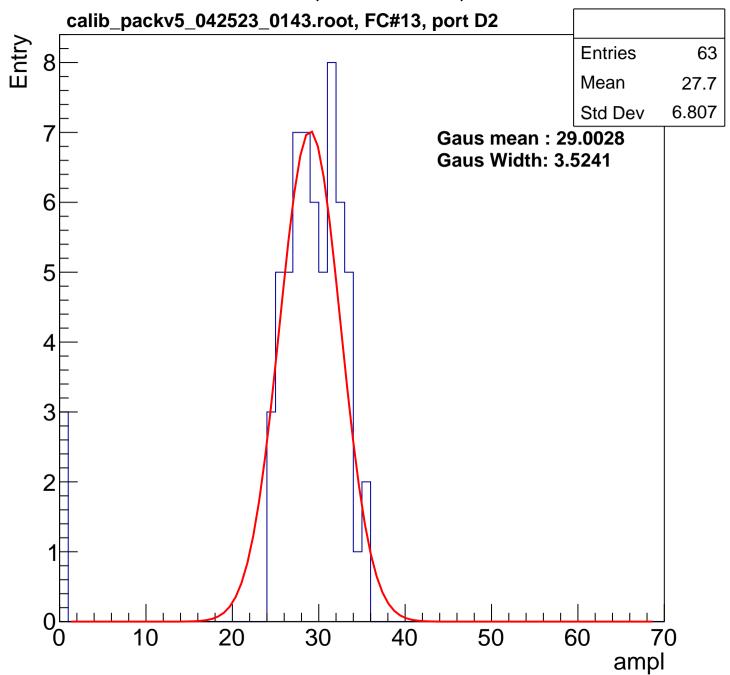


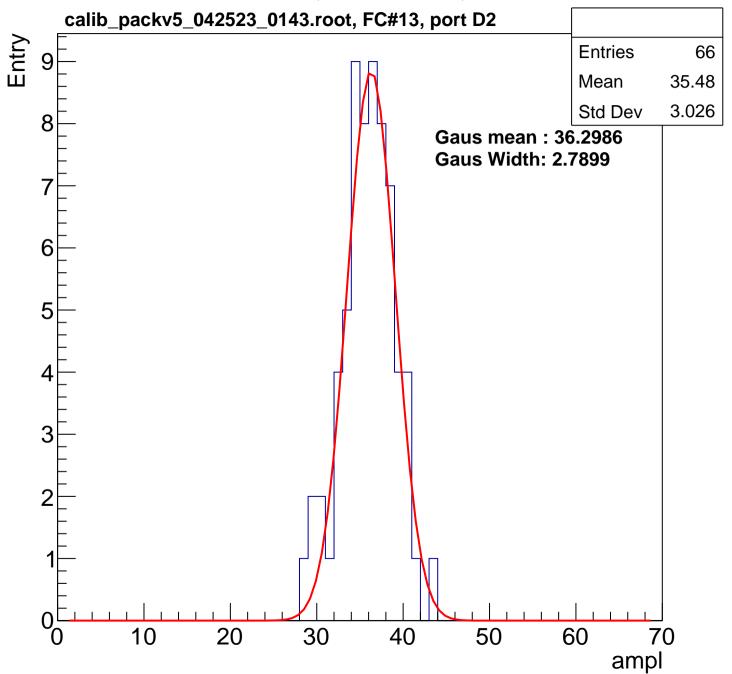


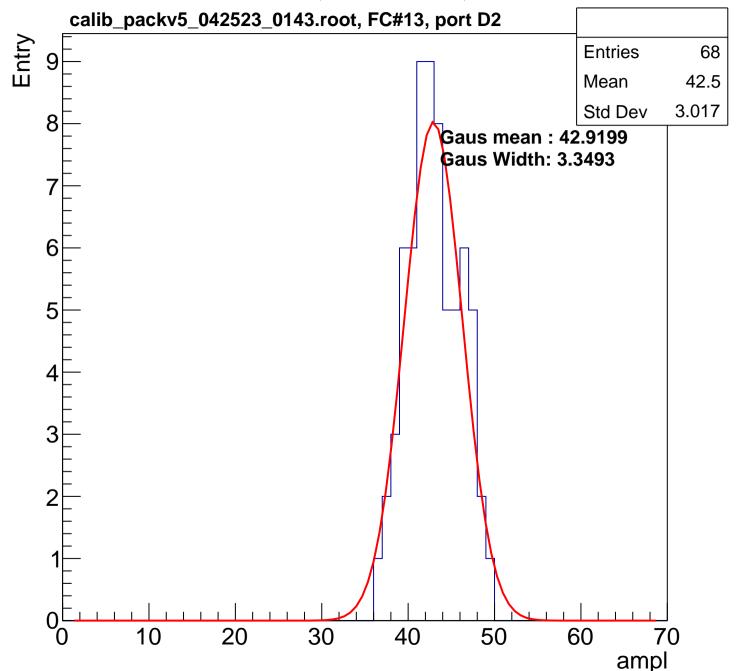


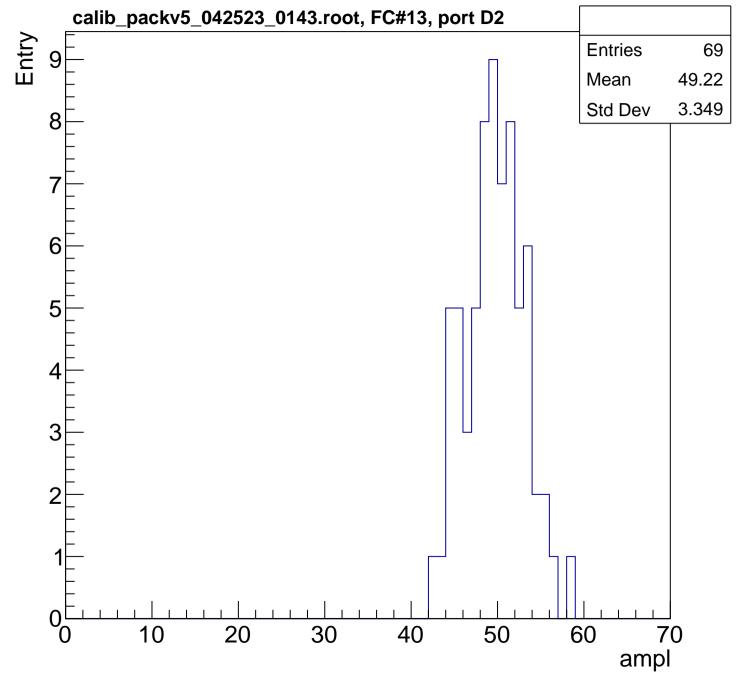


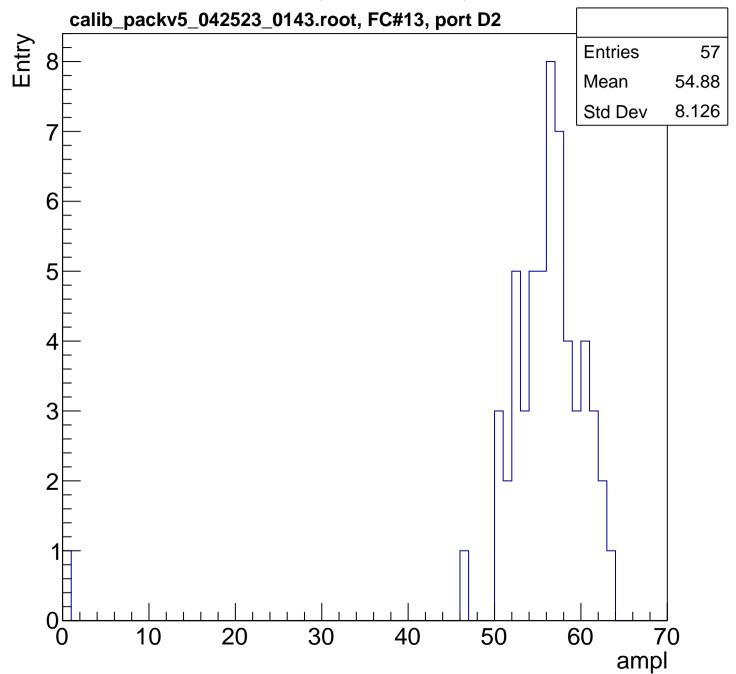


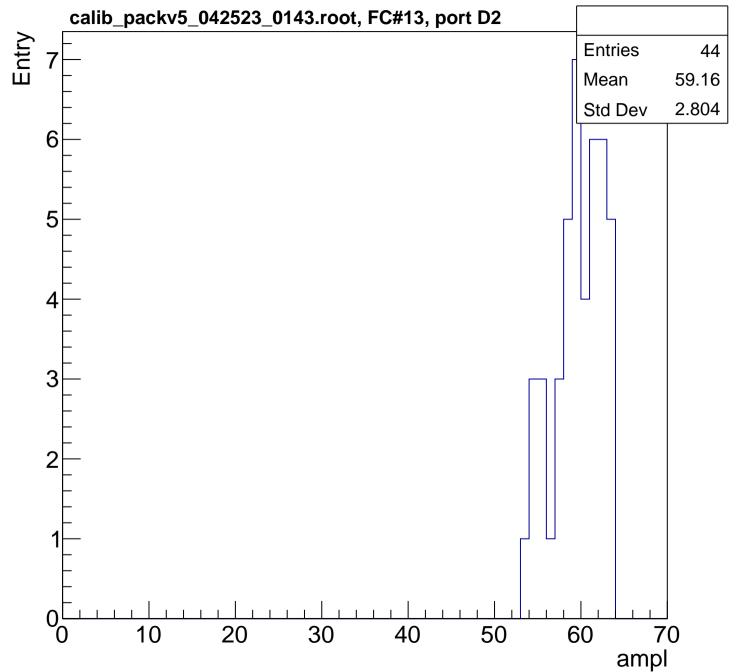


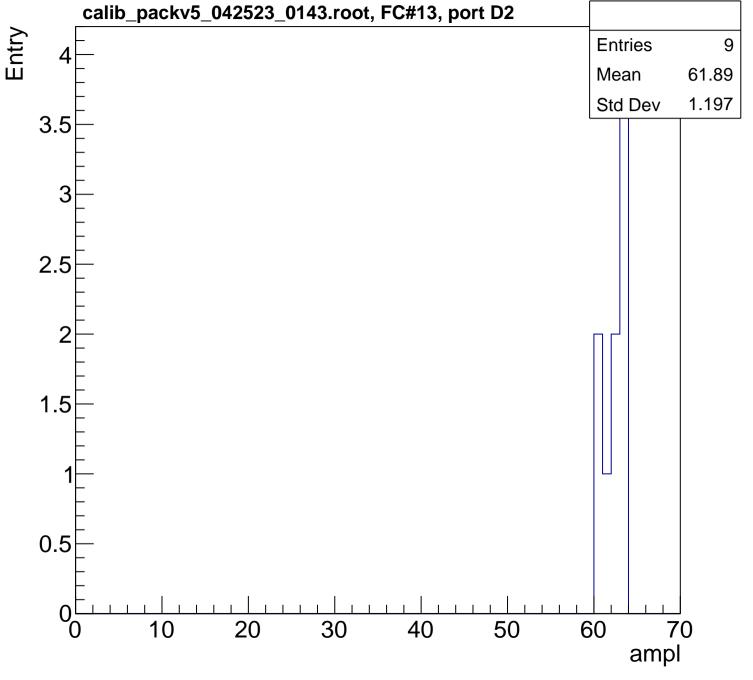




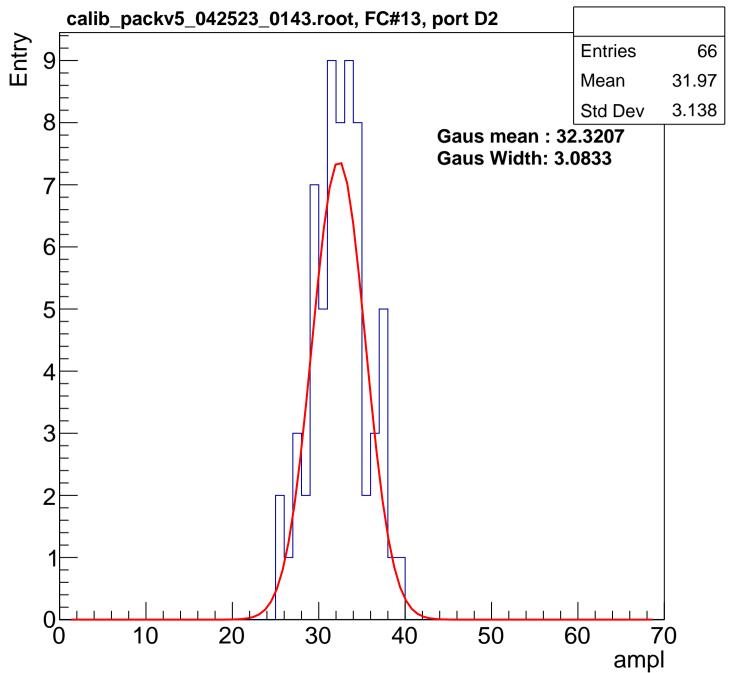


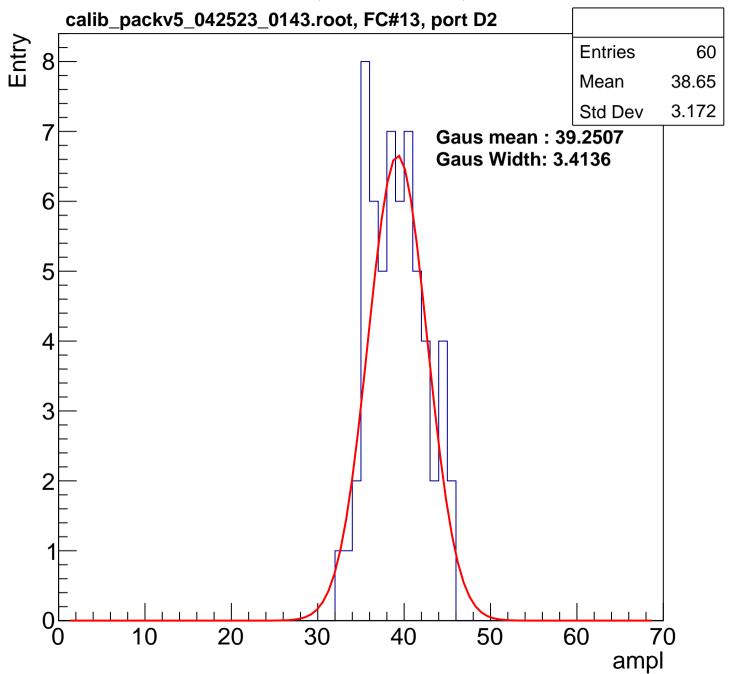


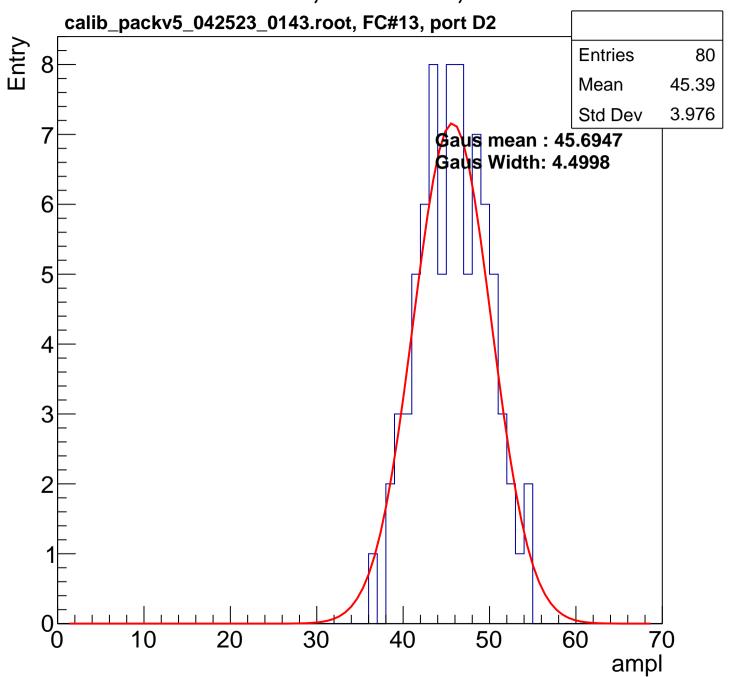


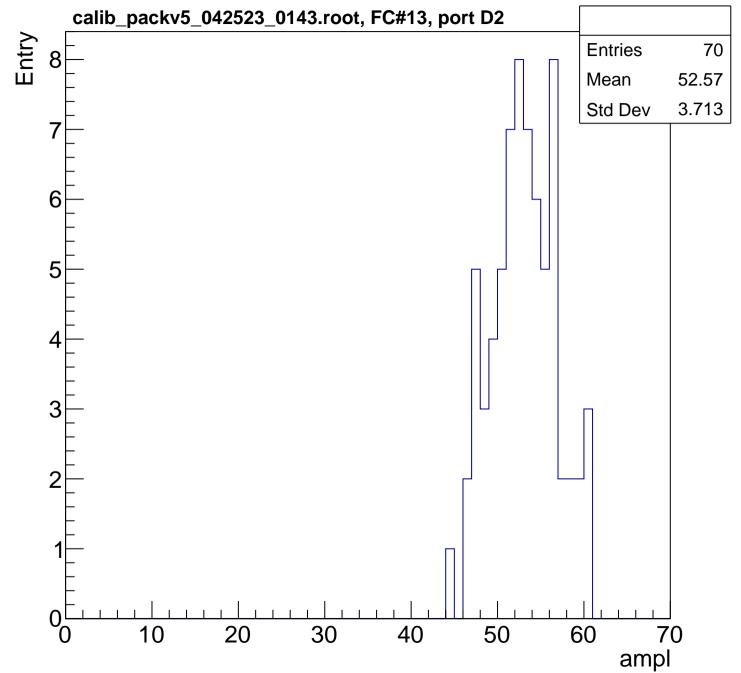


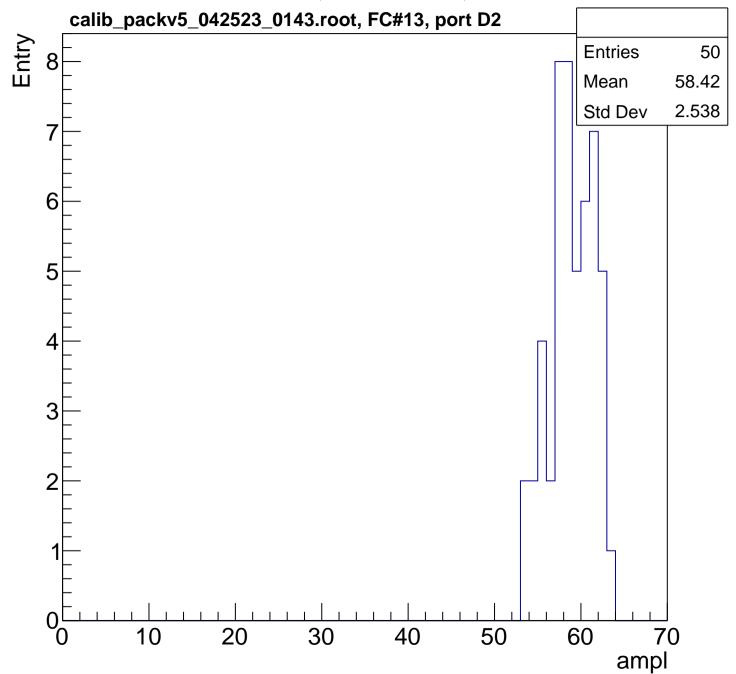


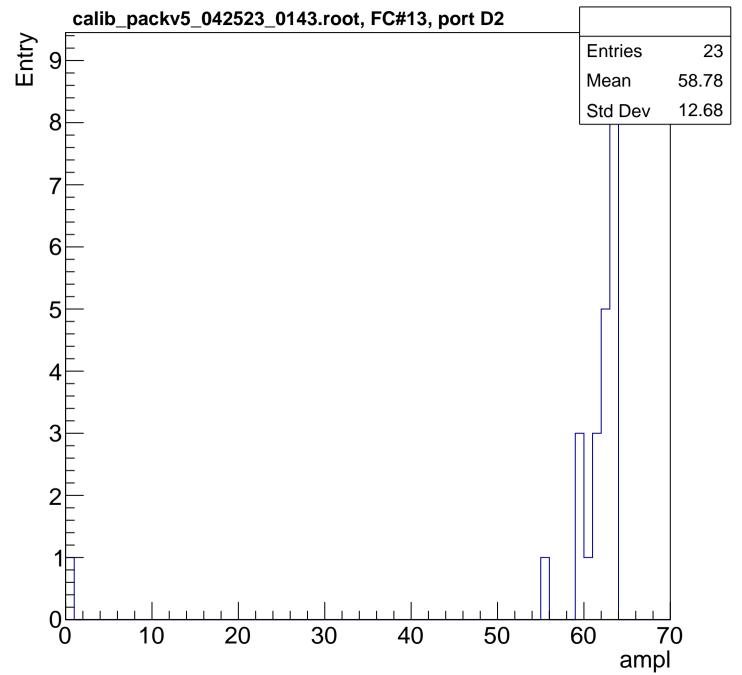






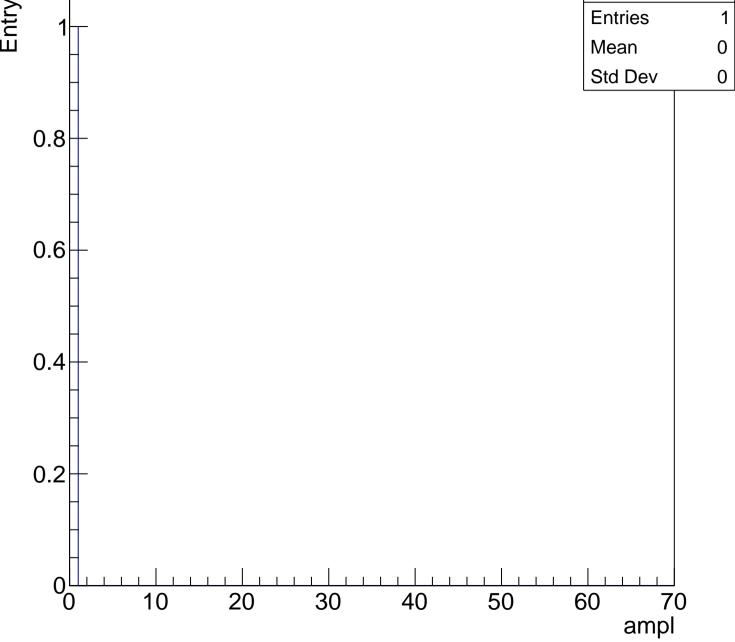


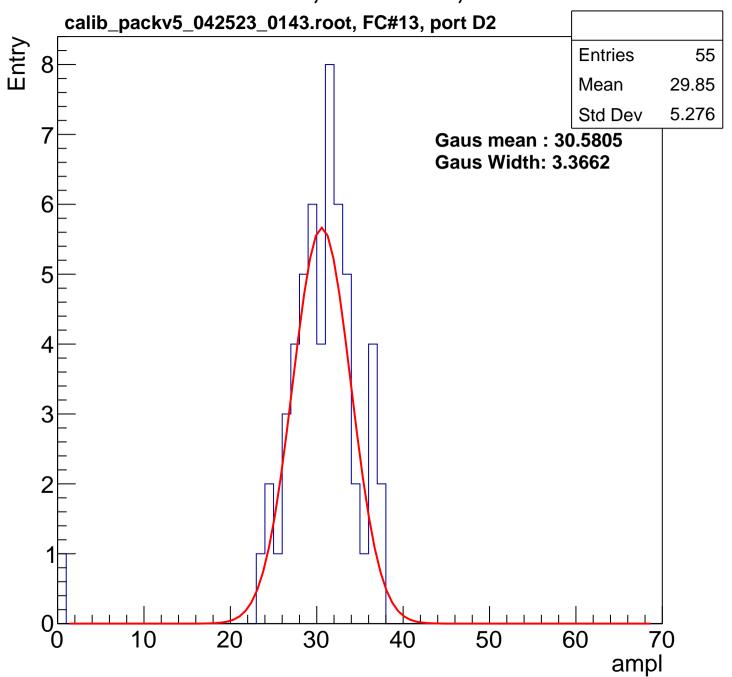


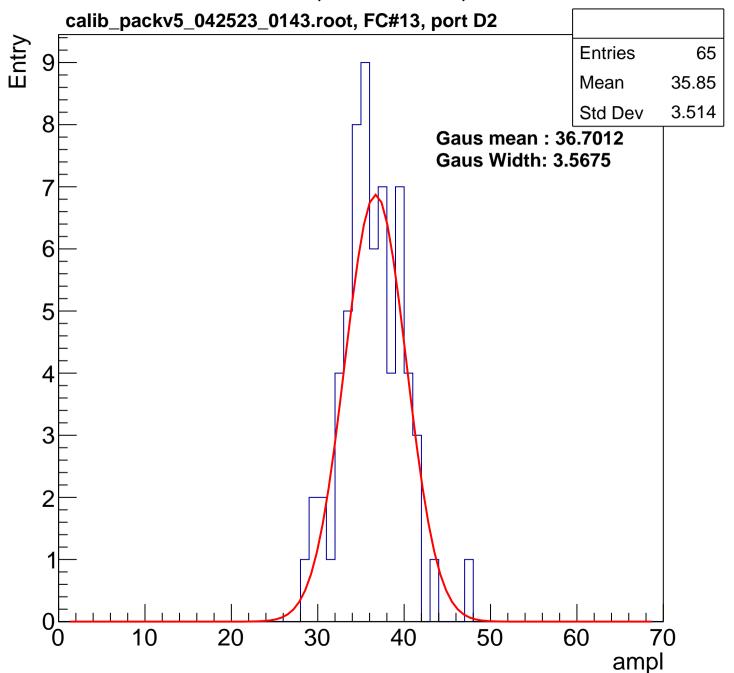


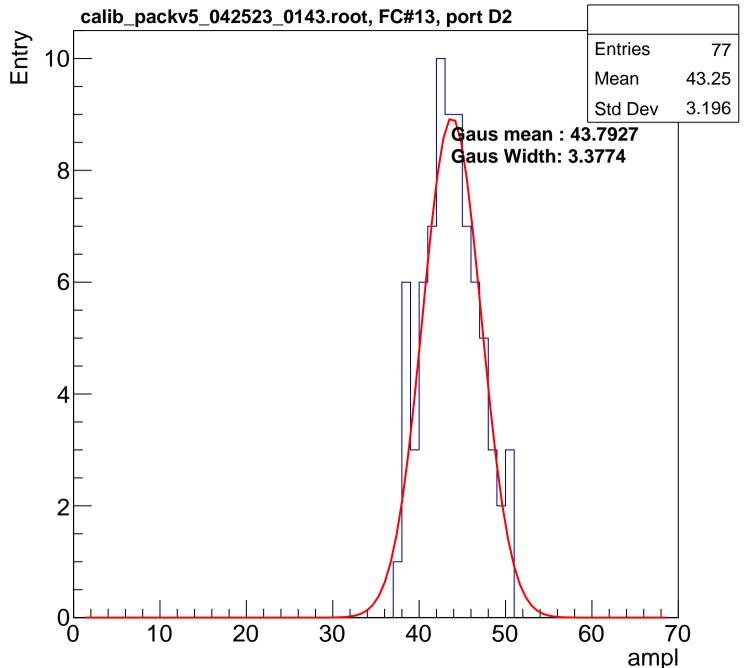


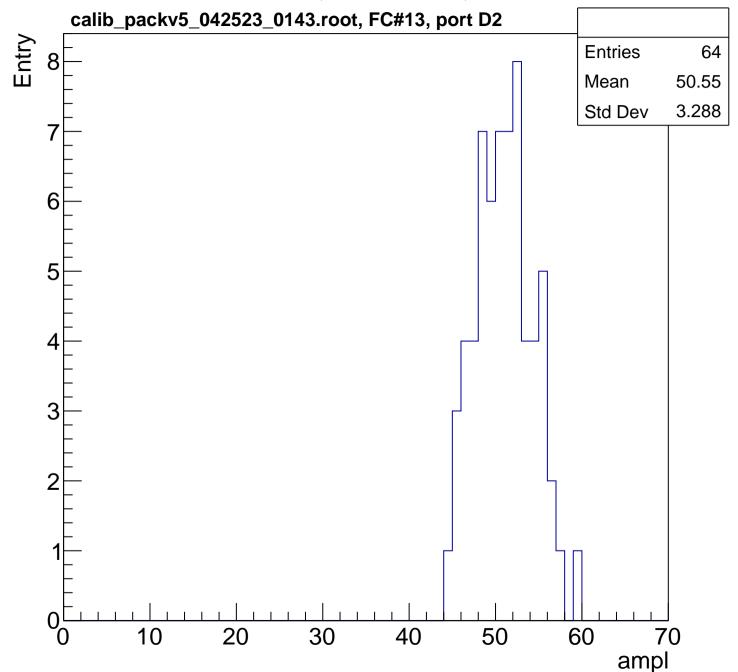
B1L003S, U2-ch51, adc7 calib_packv5_042523_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2

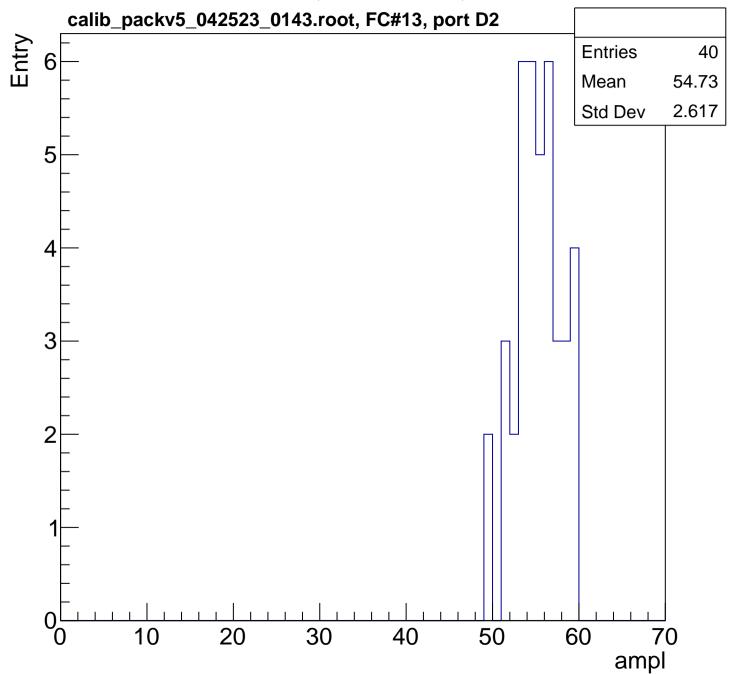


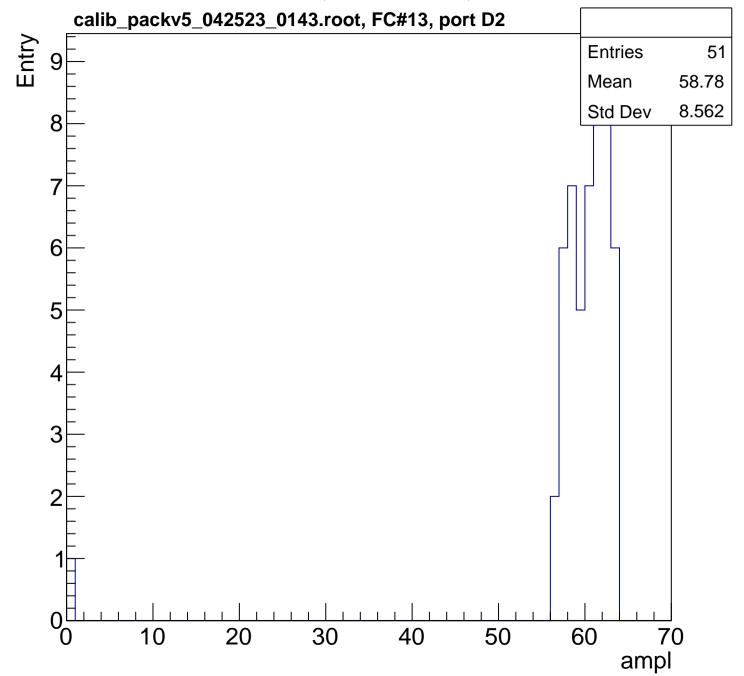


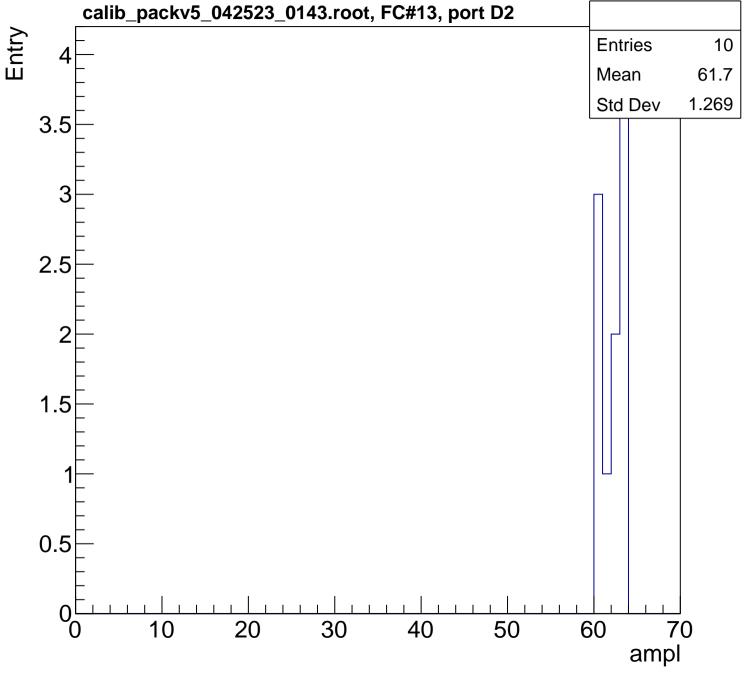


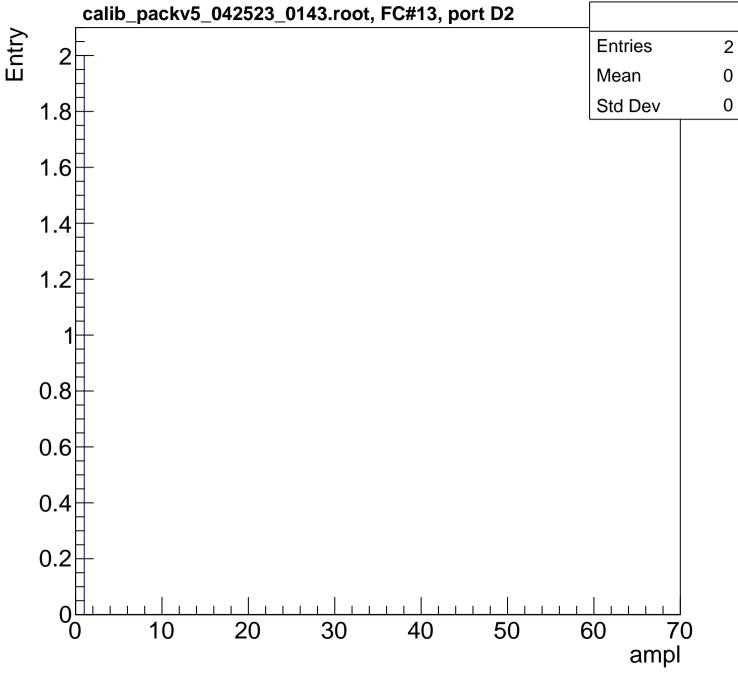


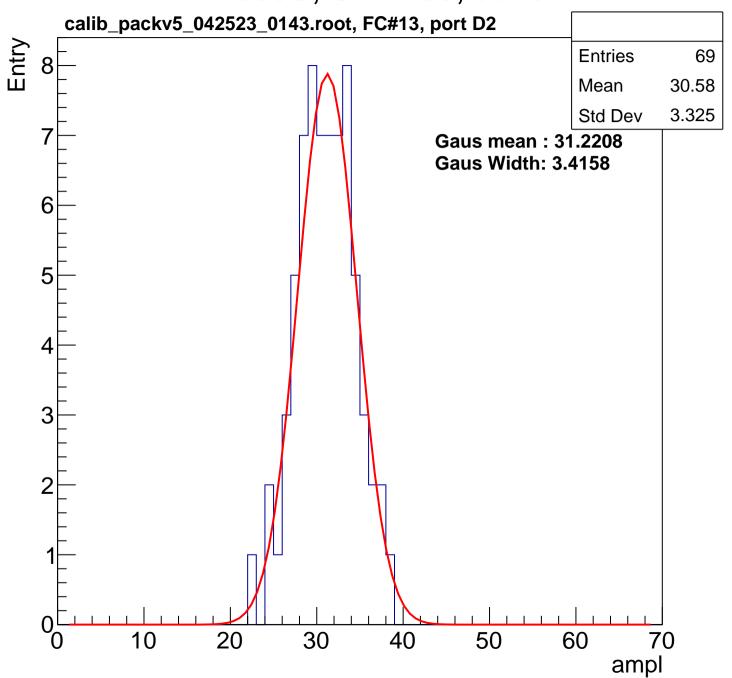


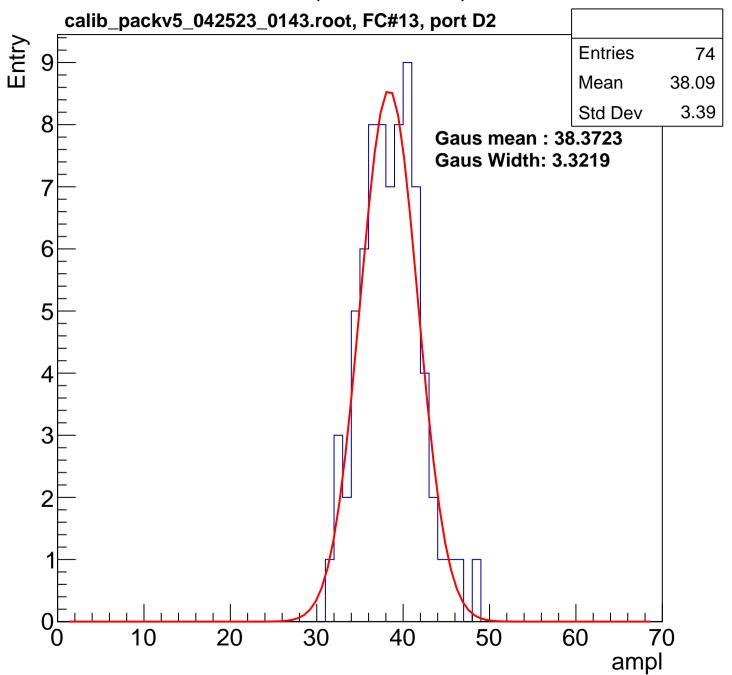


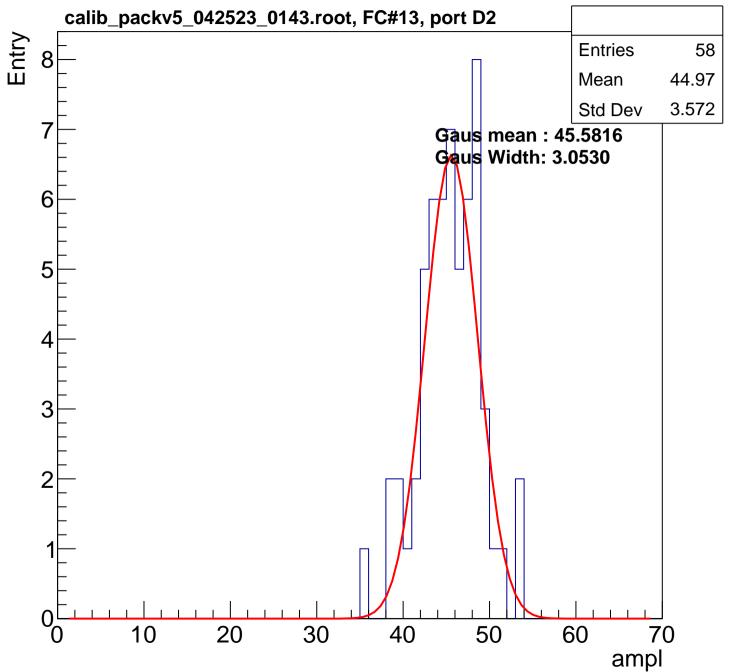


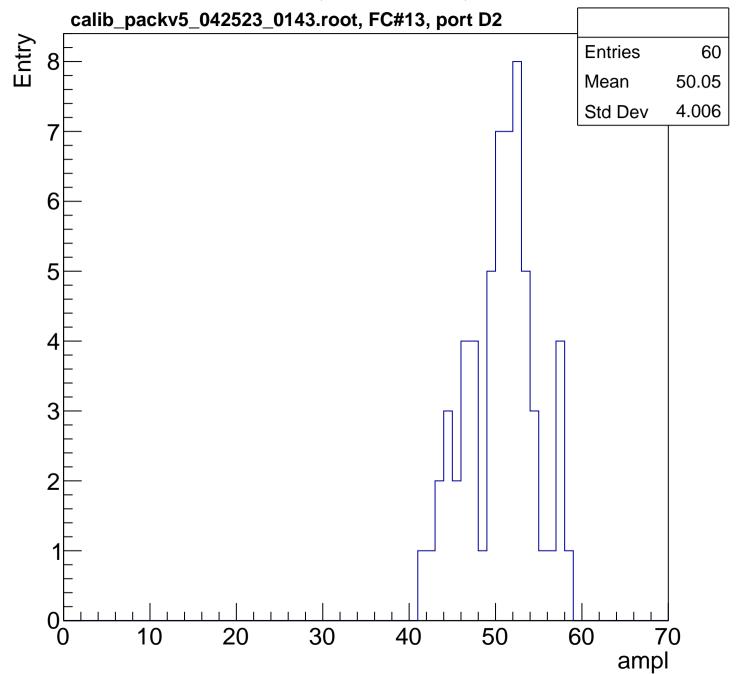


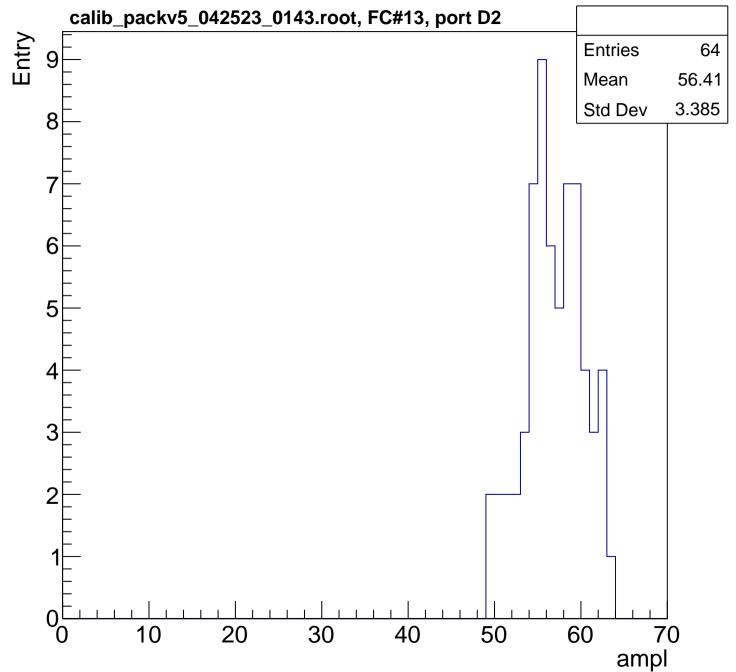


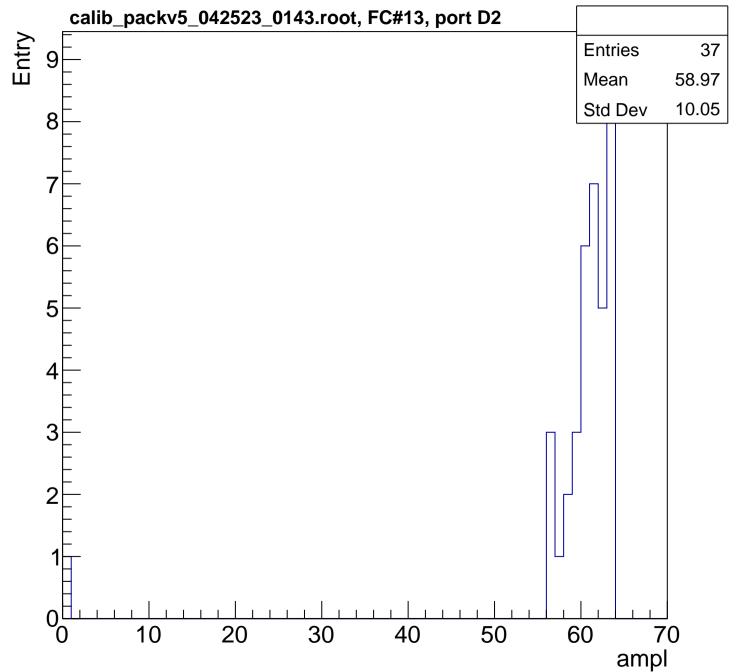


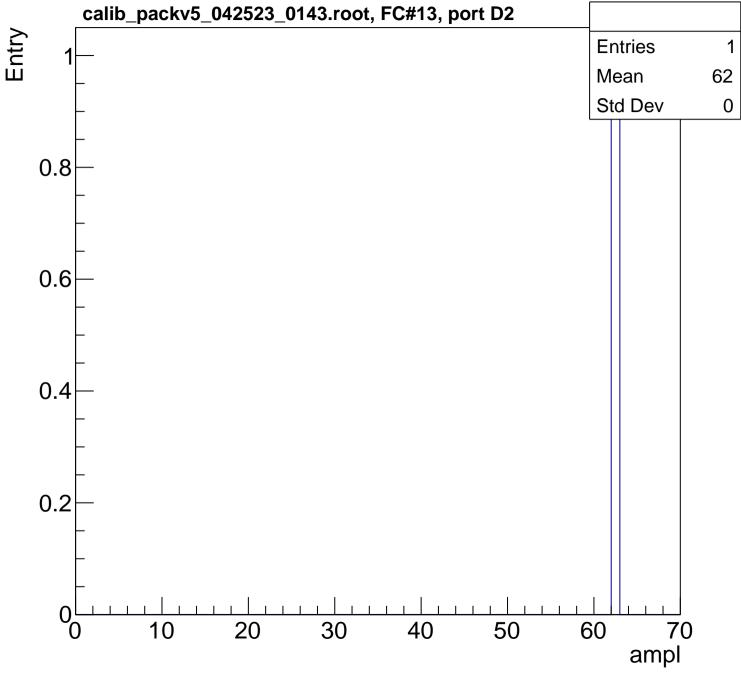




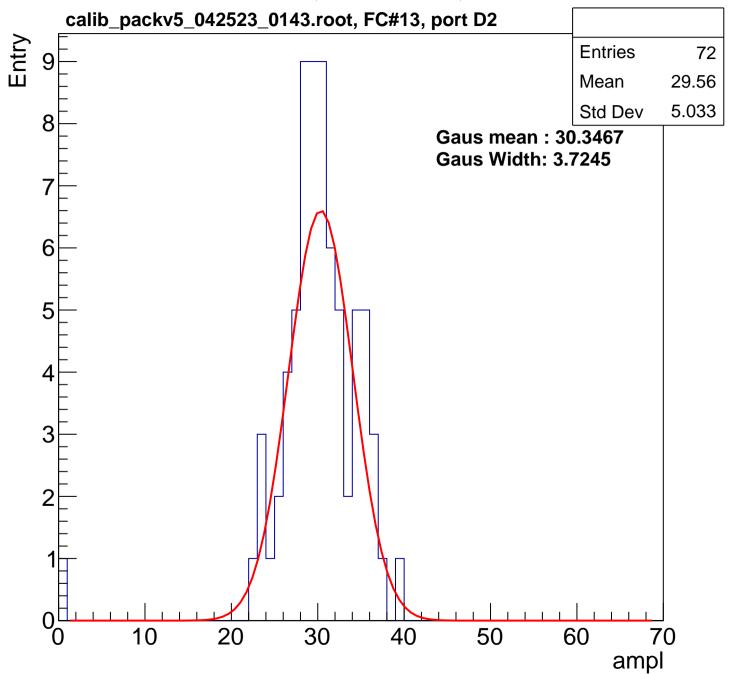


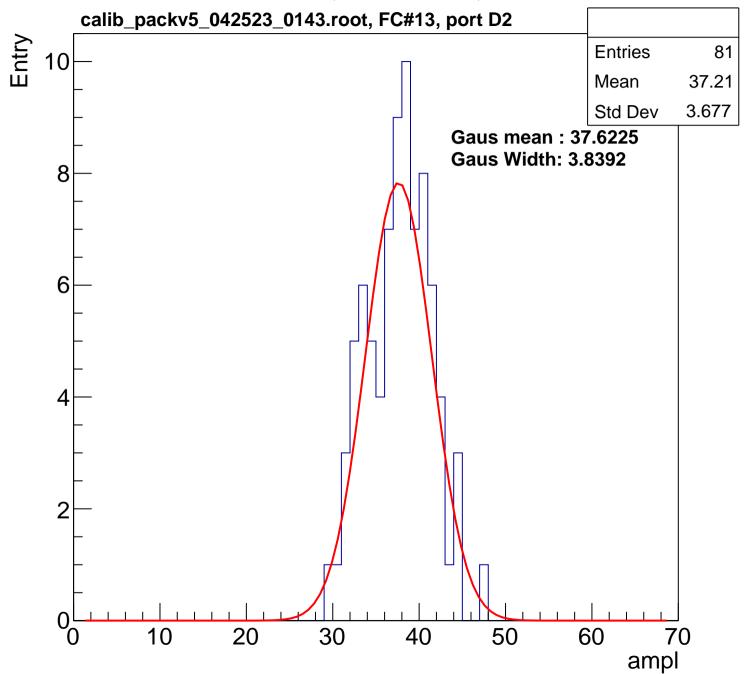


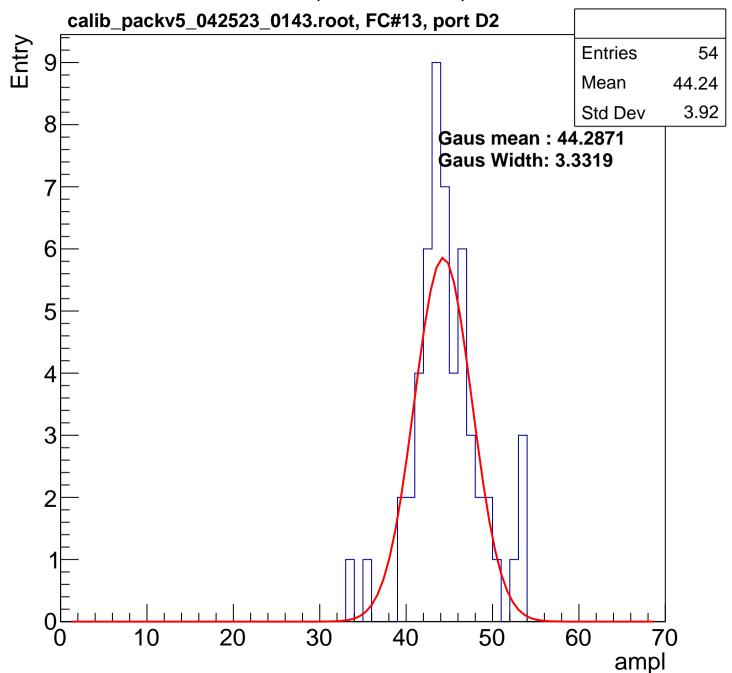


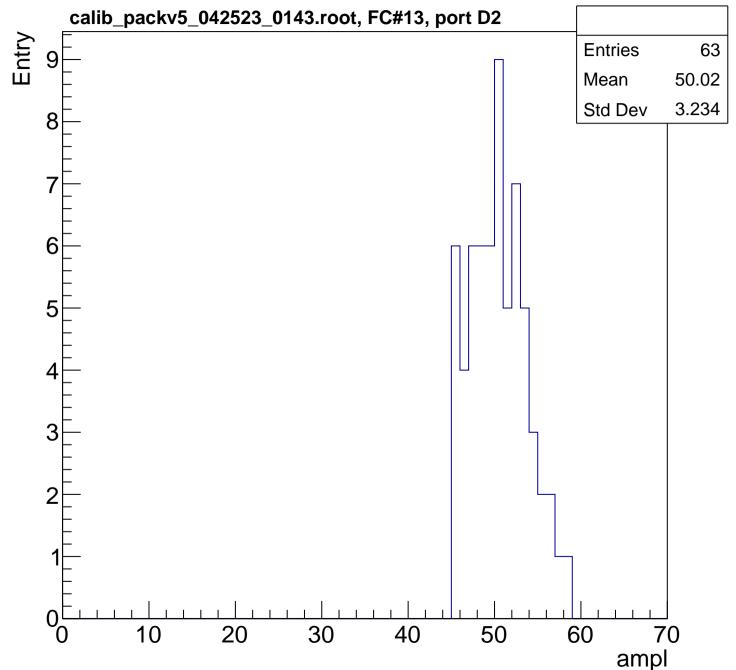


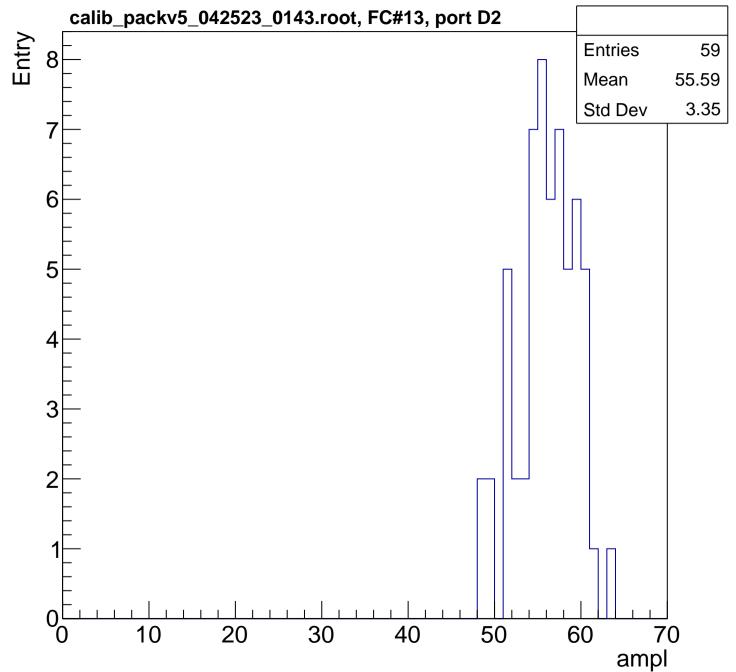


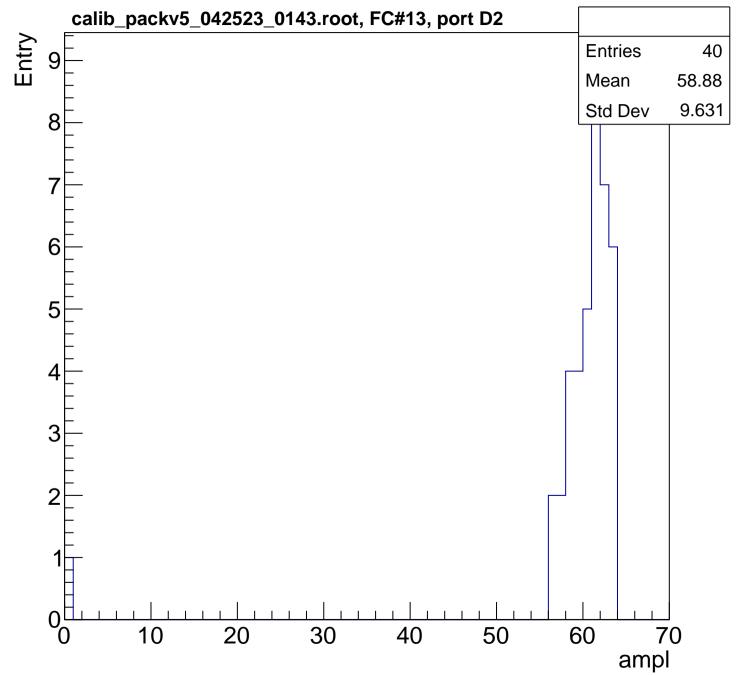


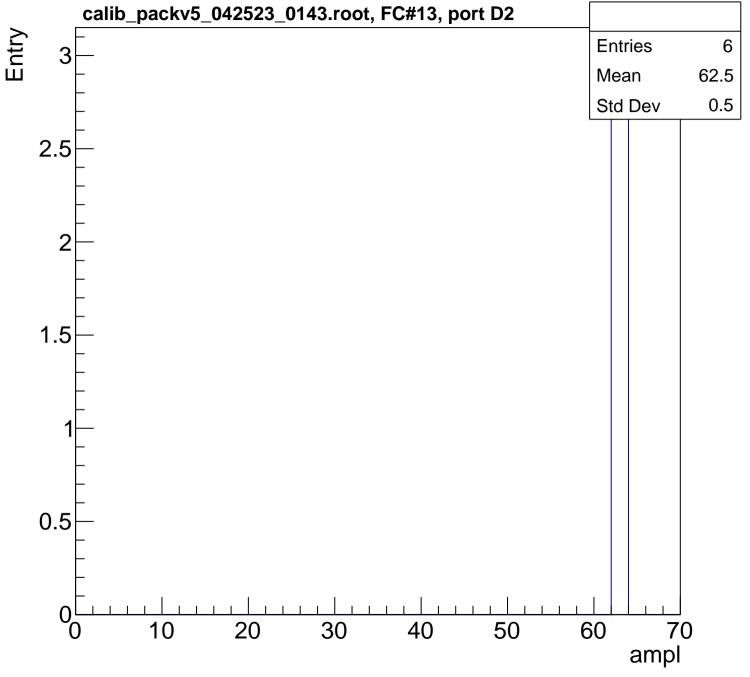




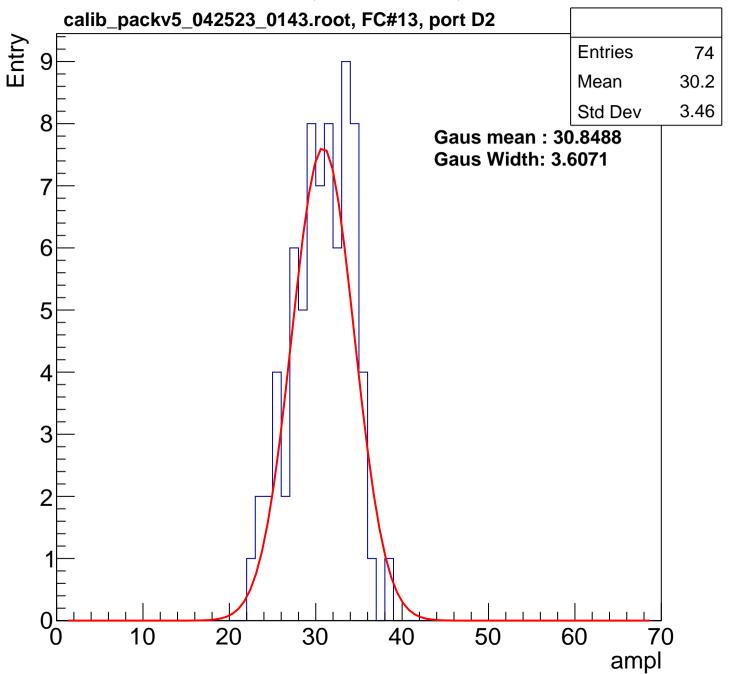


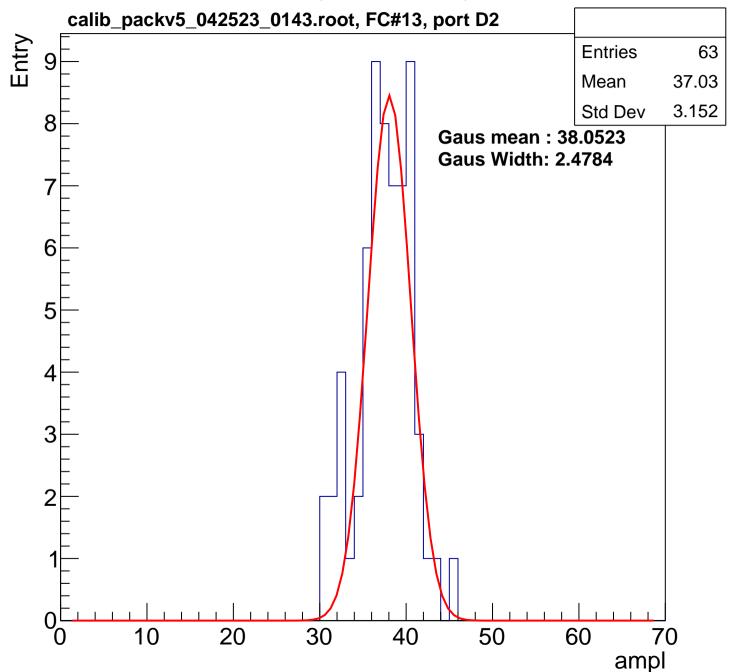


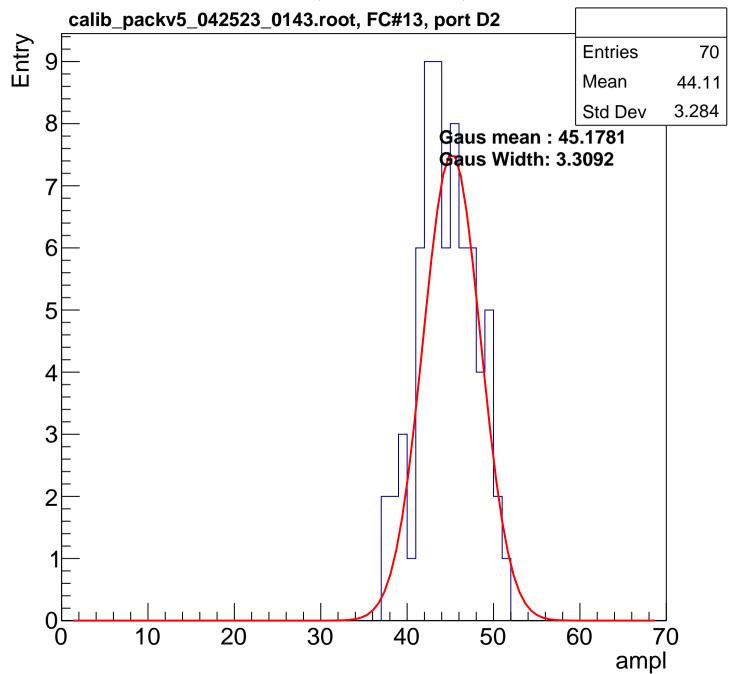


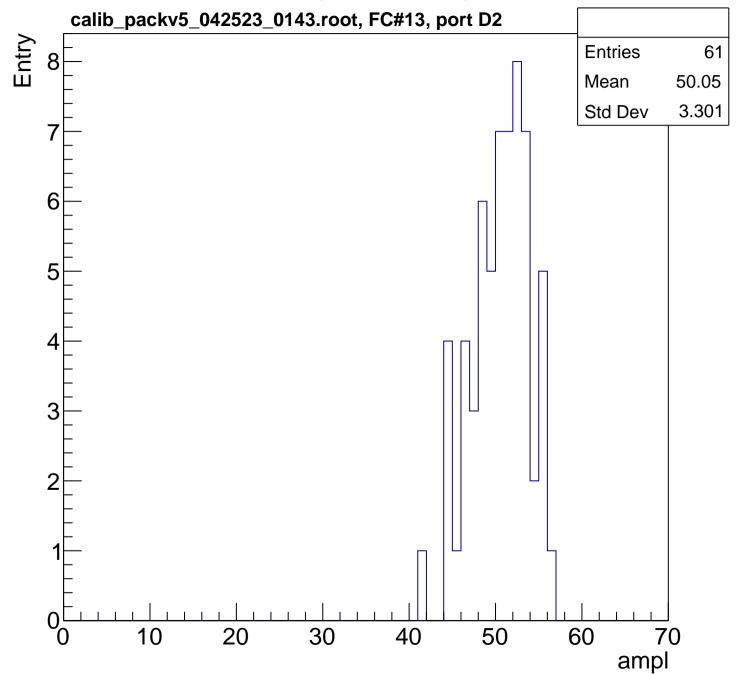


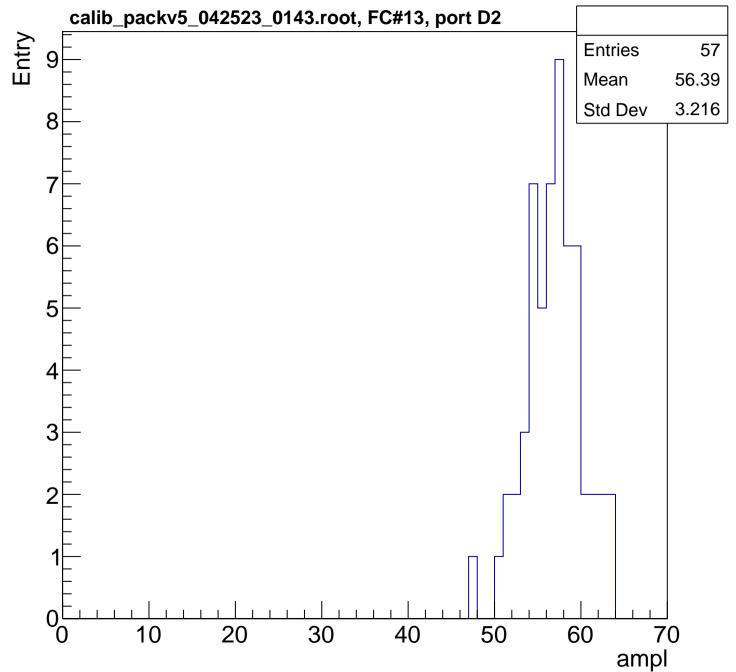
B1L003S, U2-ch54, adc7 calib_packv5_042523_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

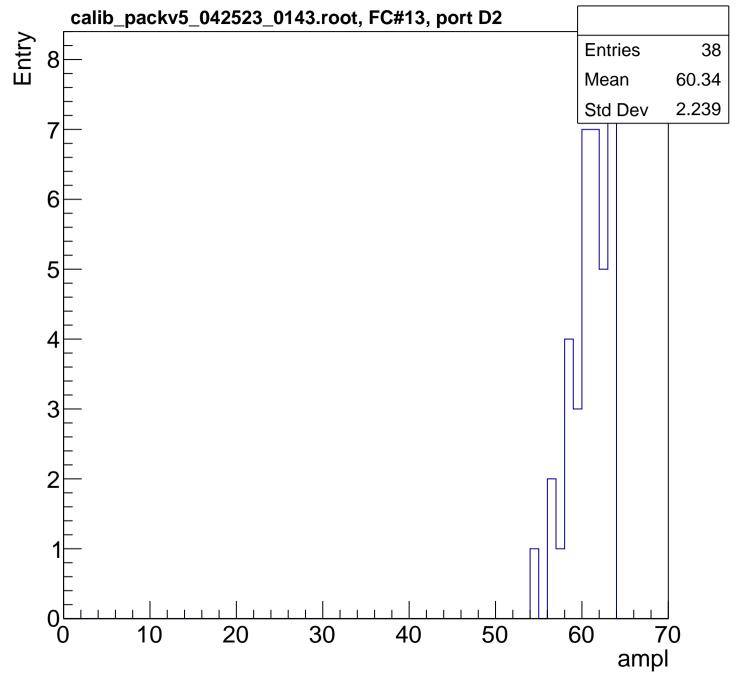


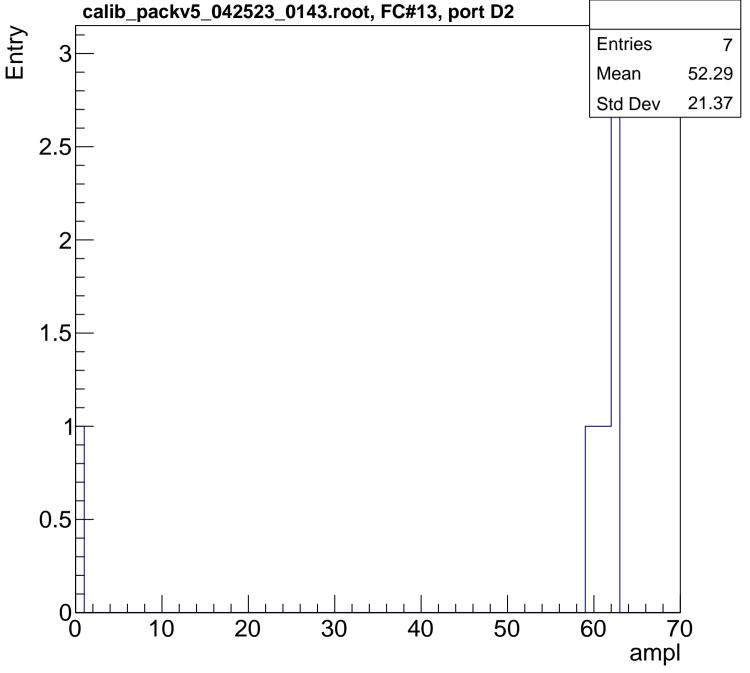




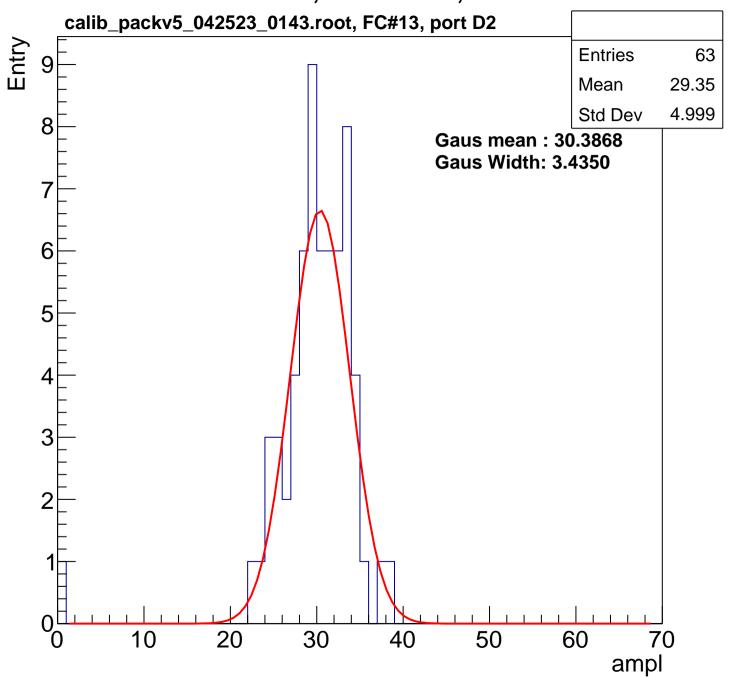


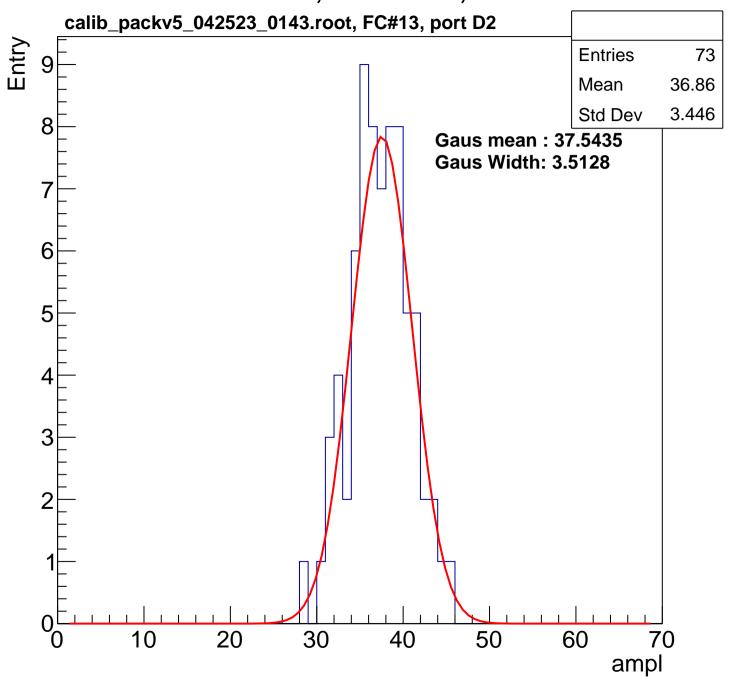


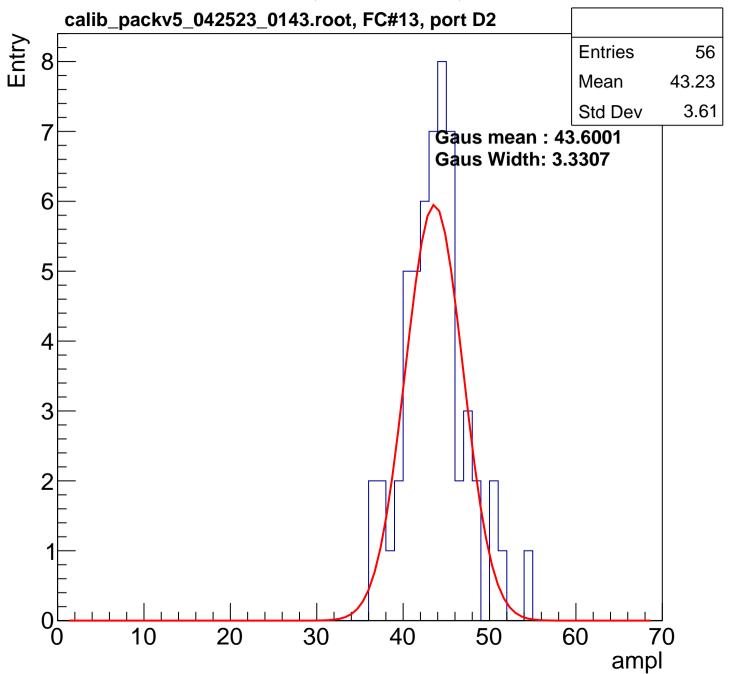


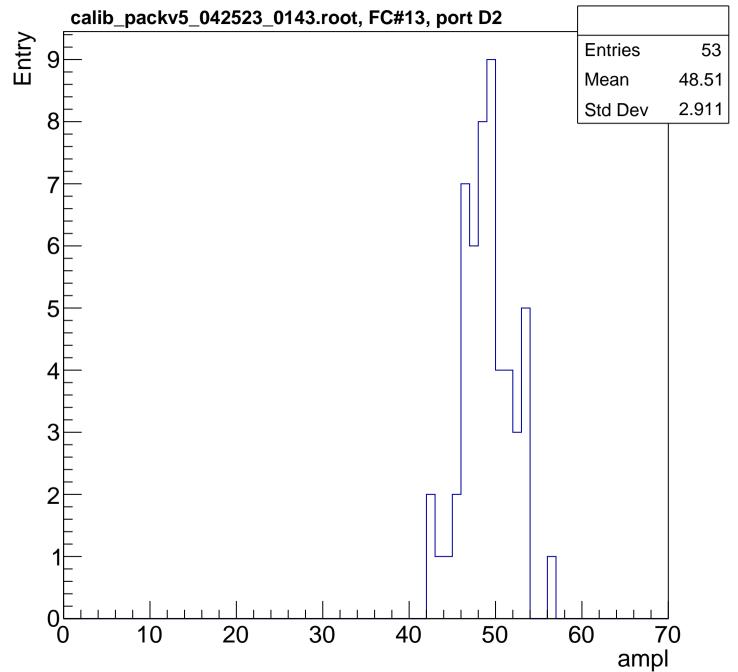


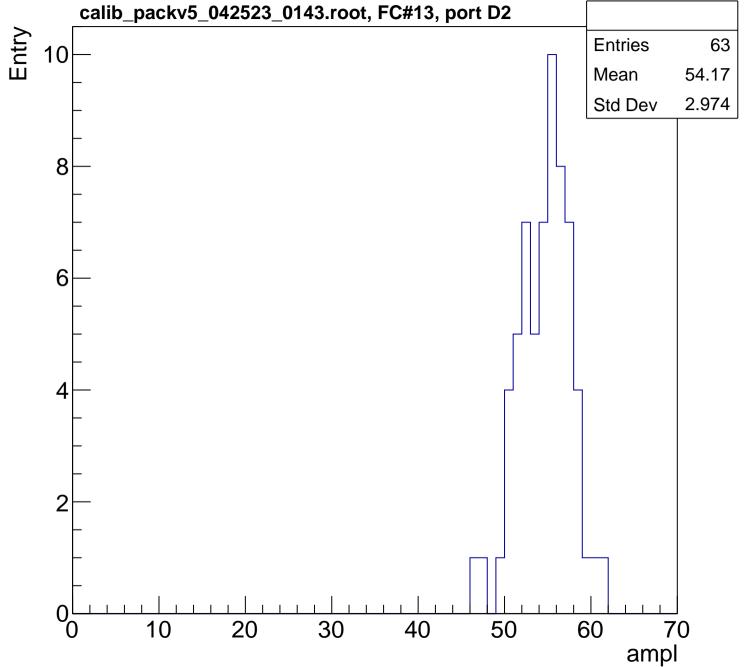


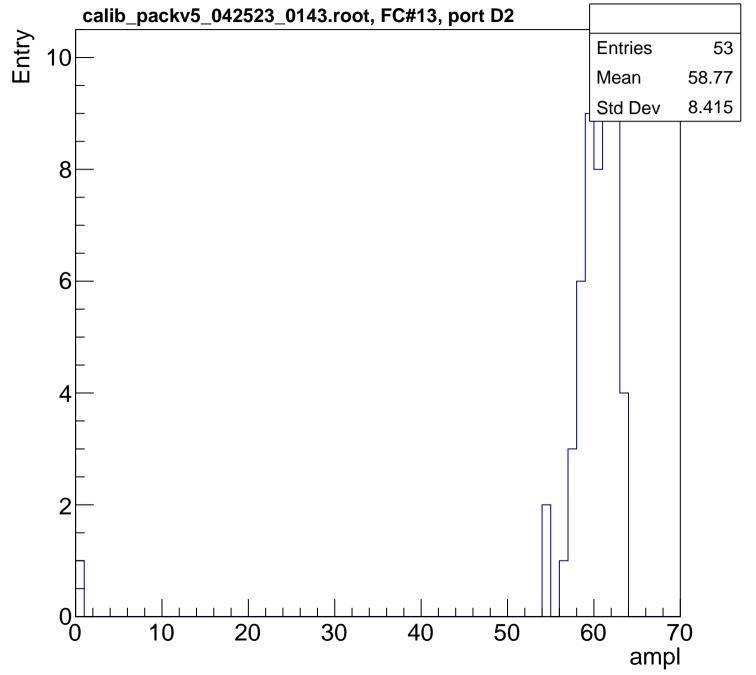


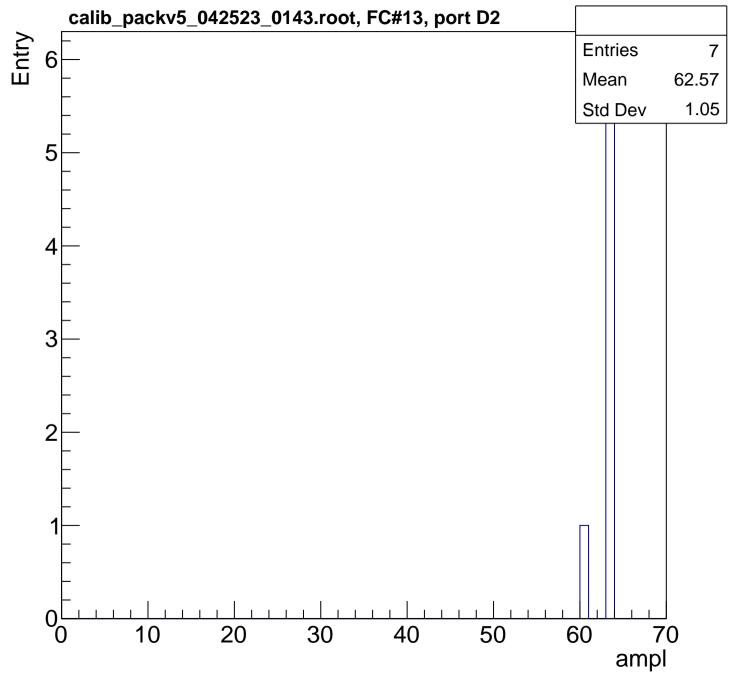


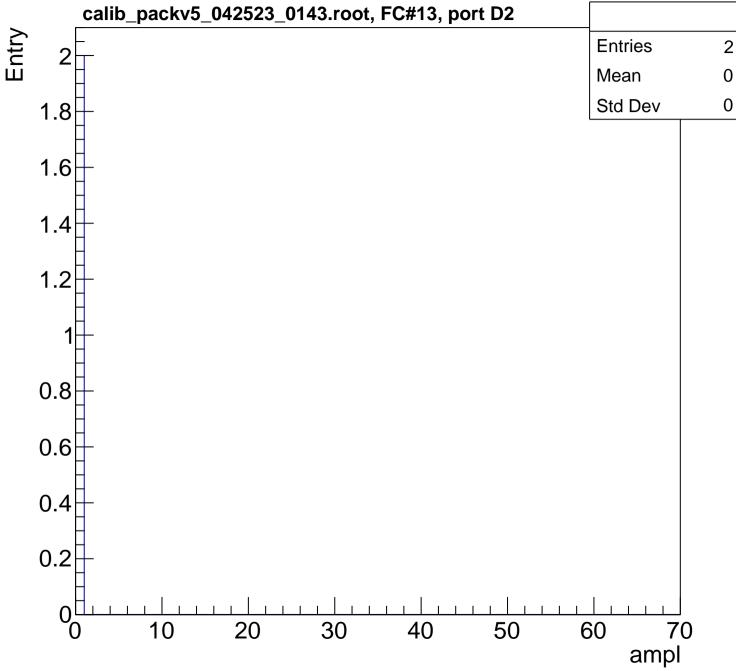


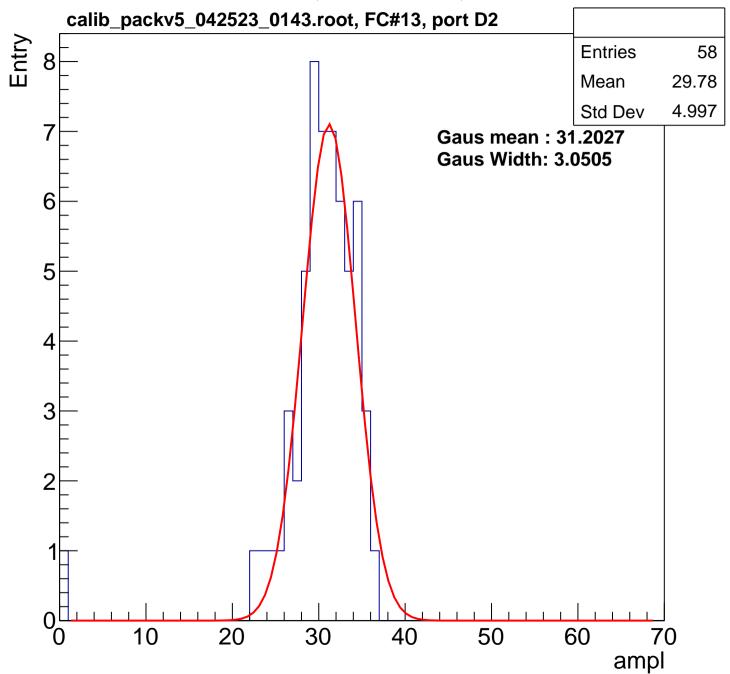


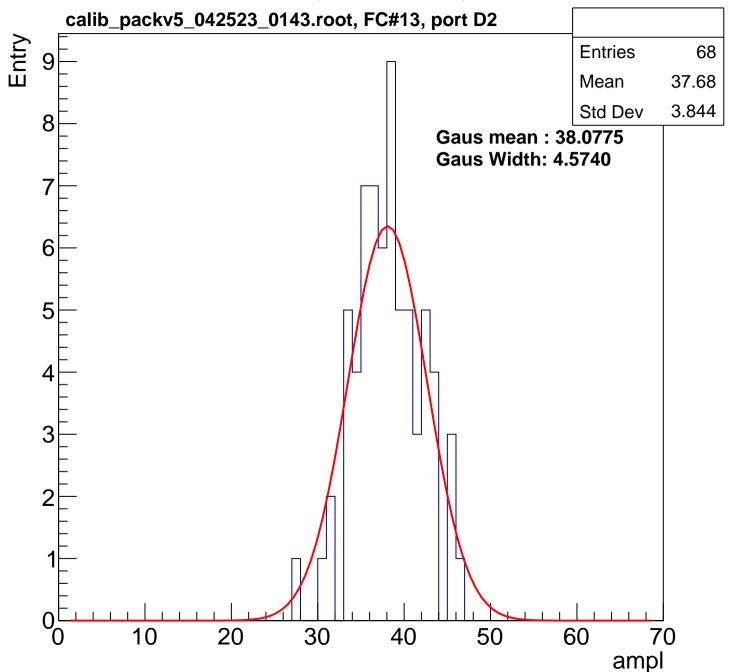


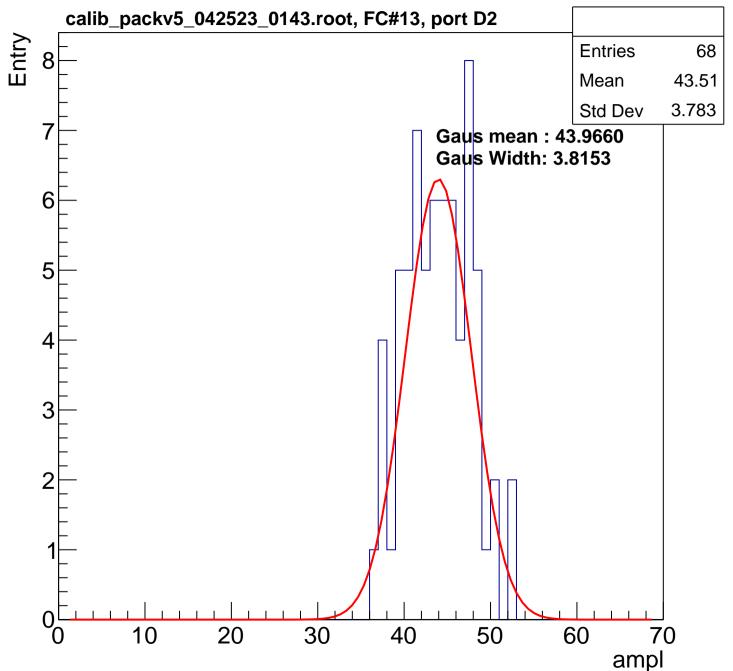


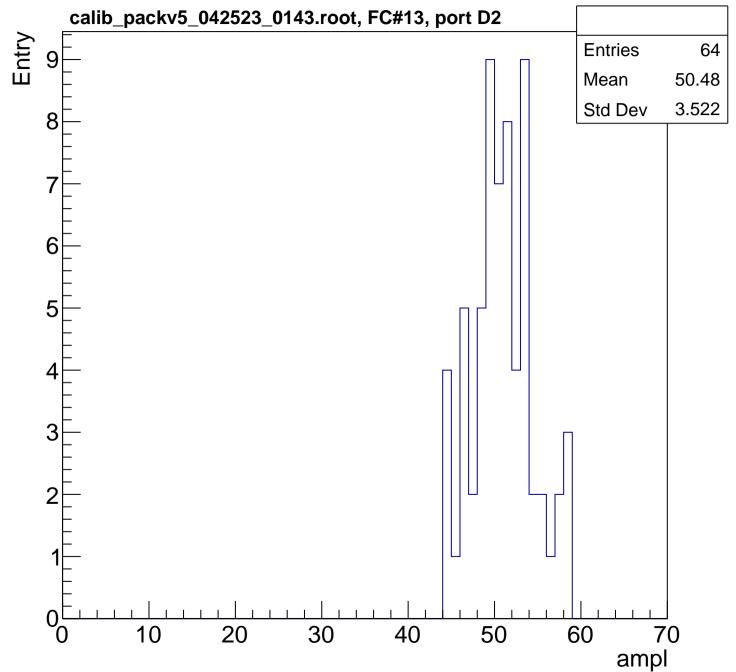


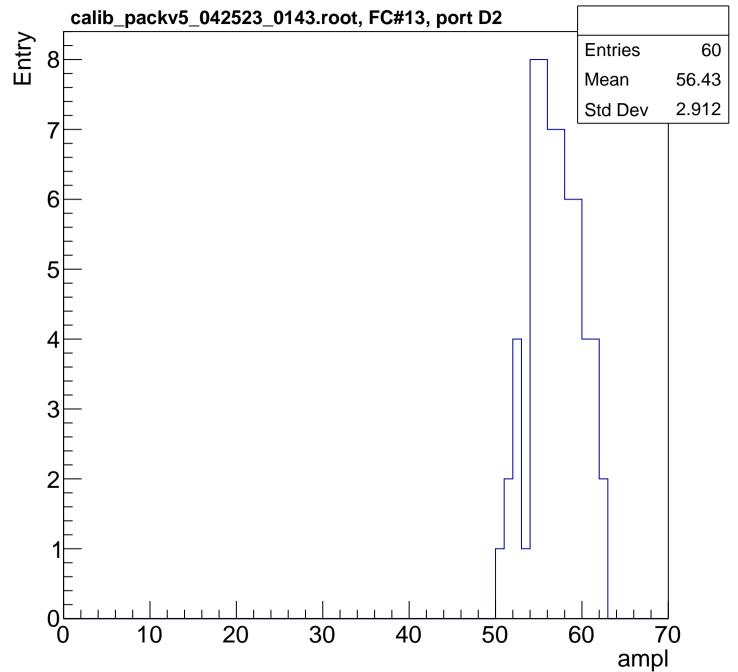


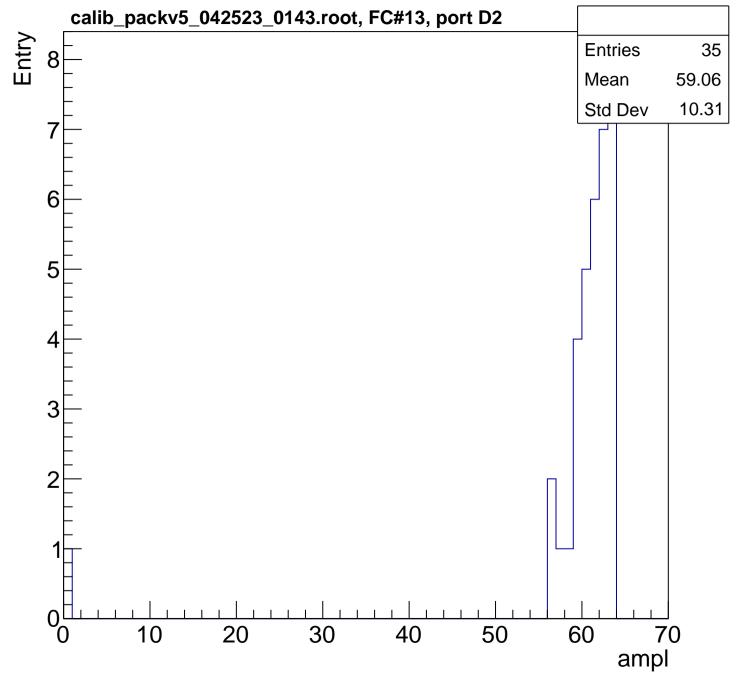


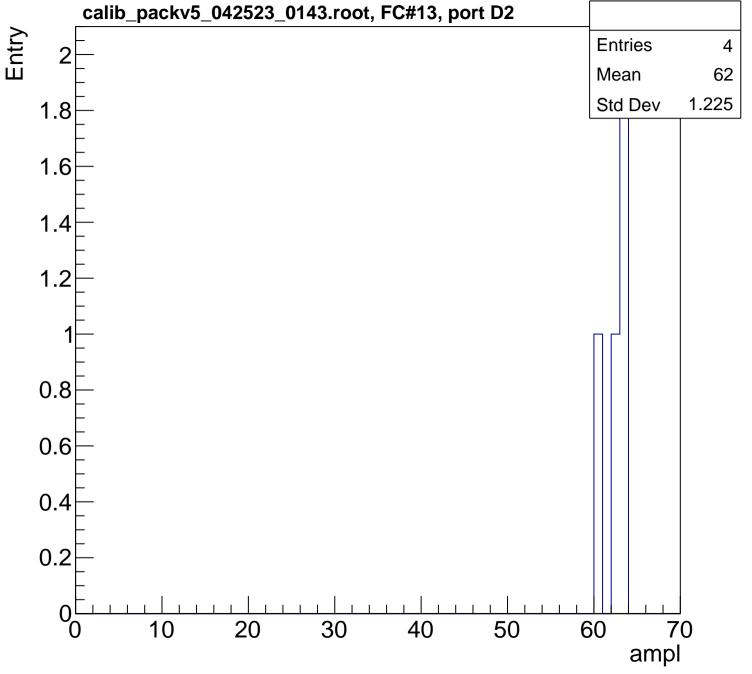




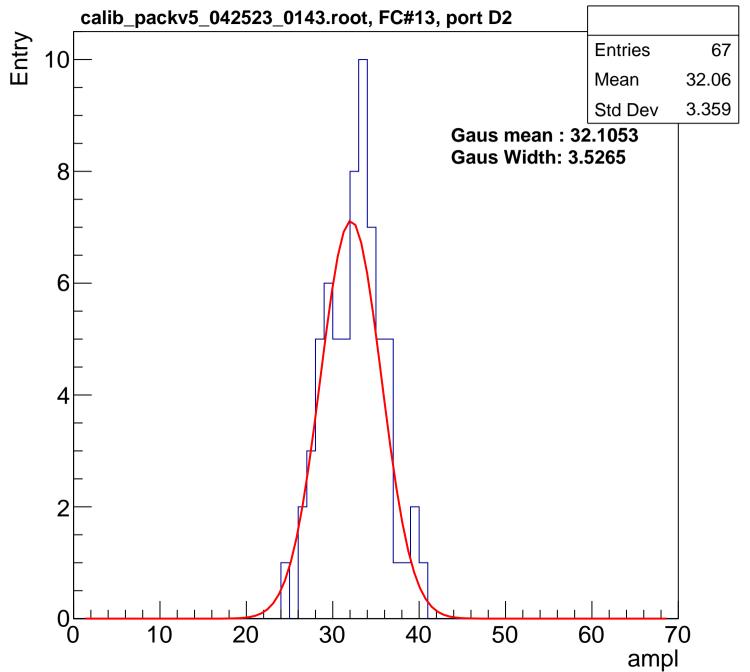


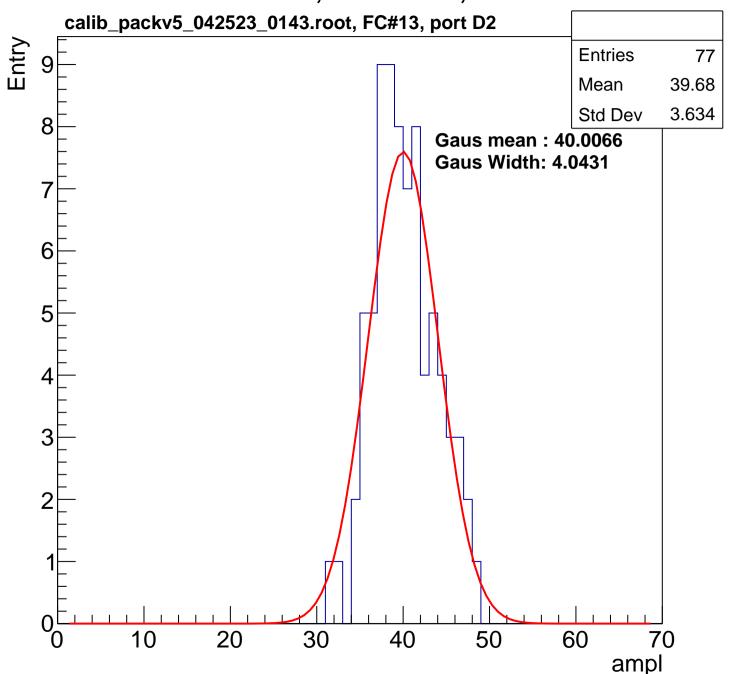


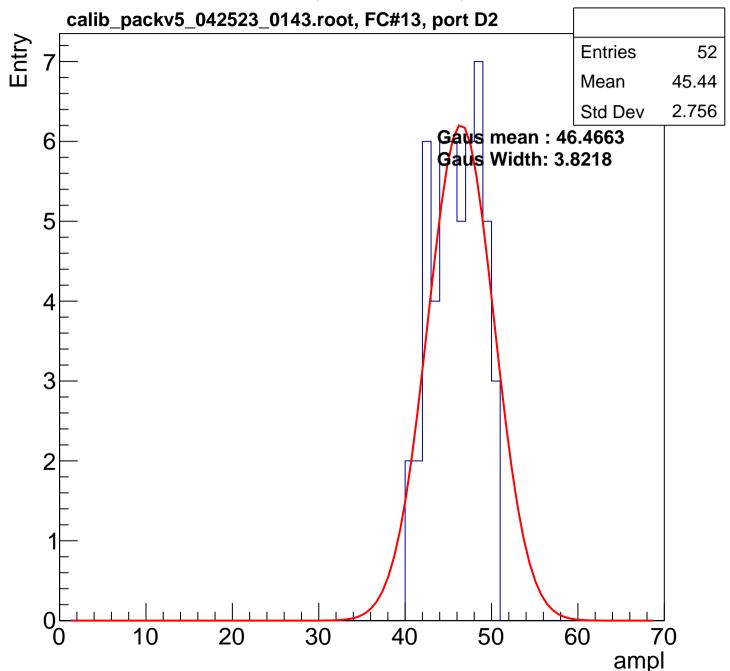


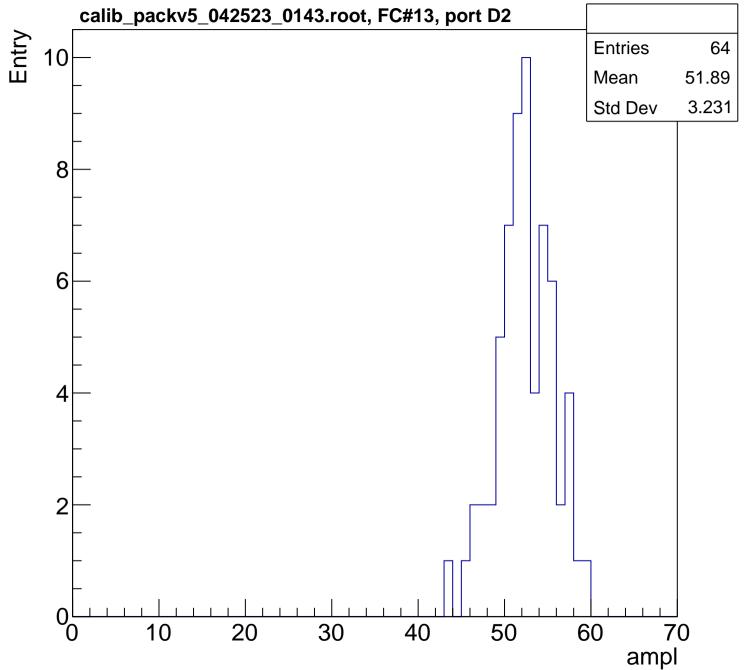


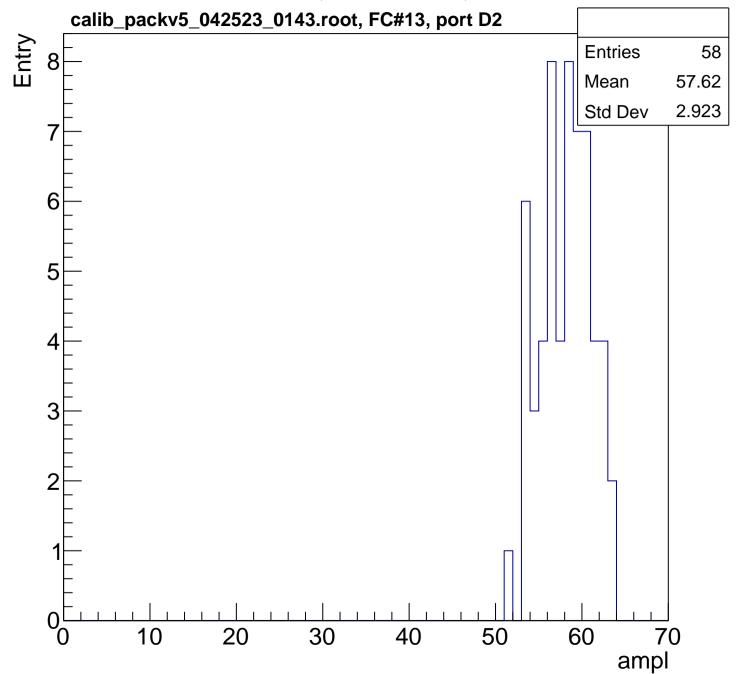
B1L003S, U2-ch57, adc7 calib_packv5_042523_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

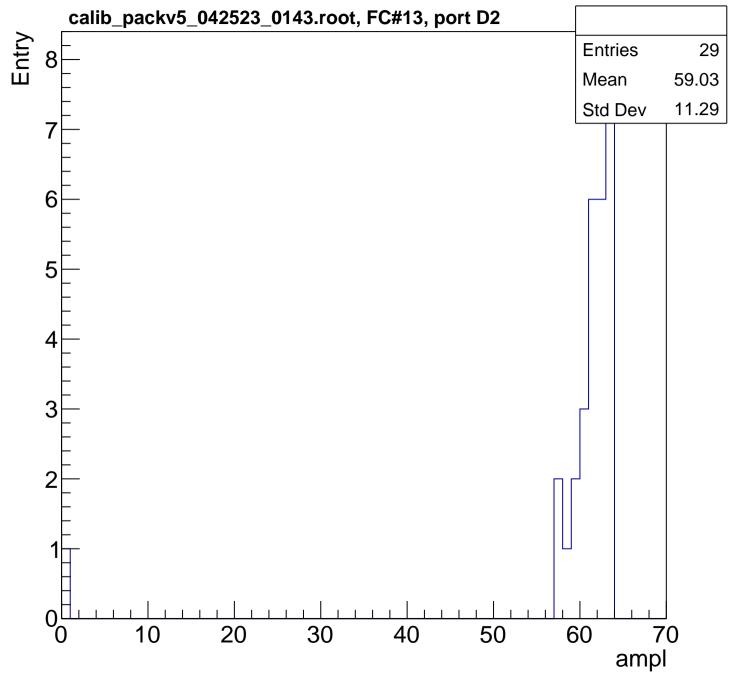


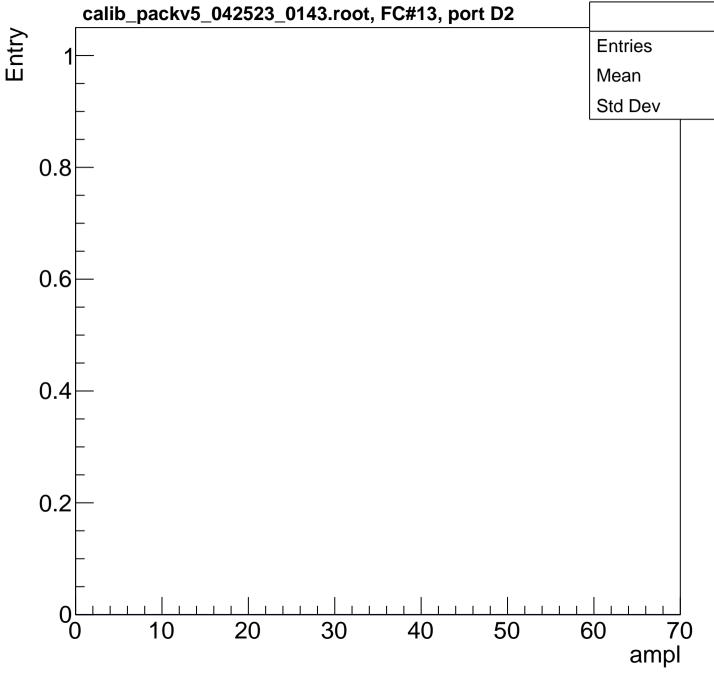




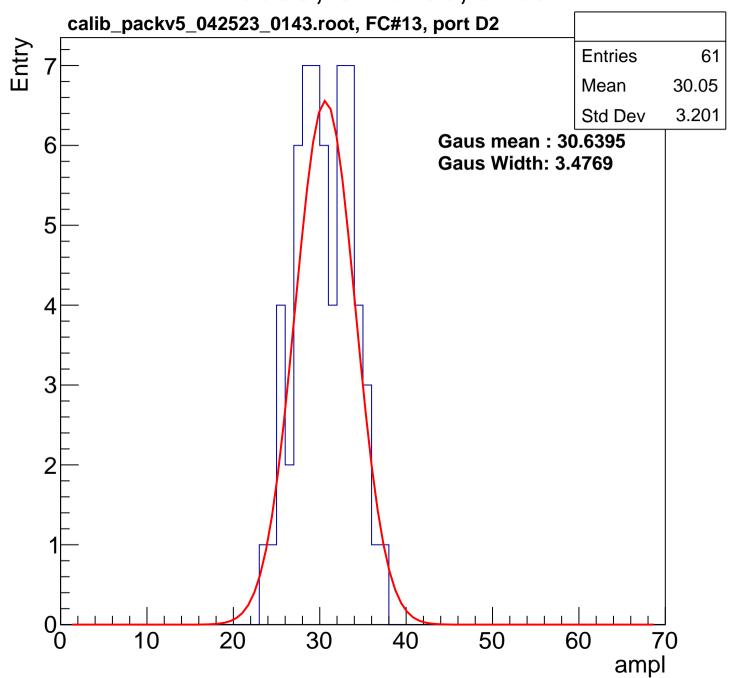


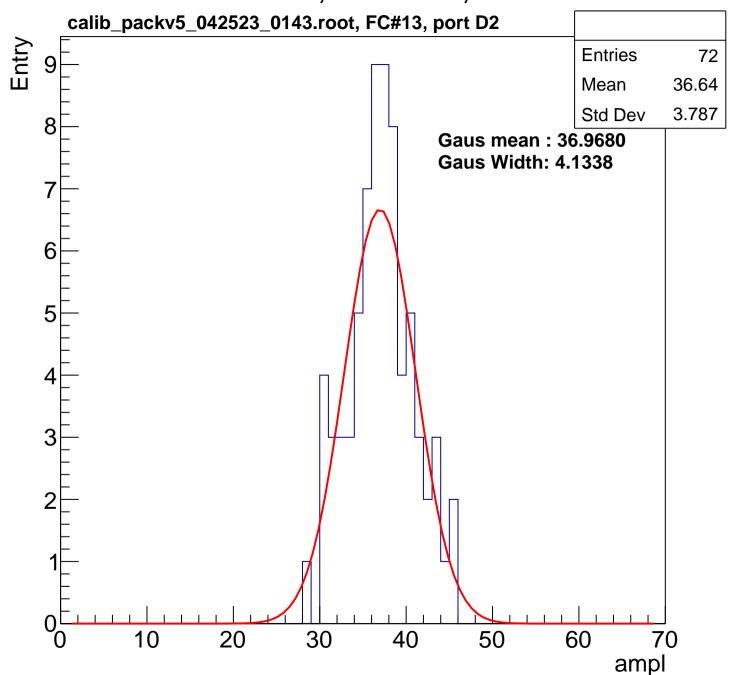


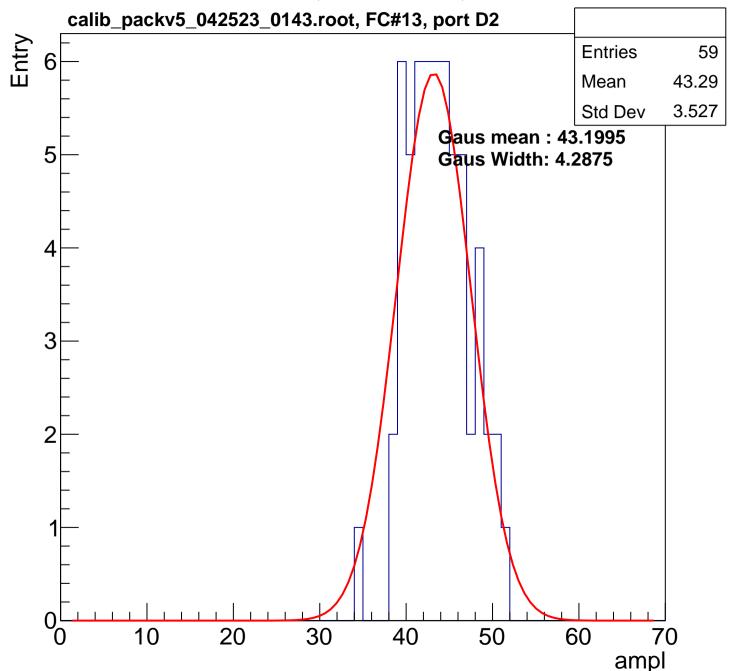


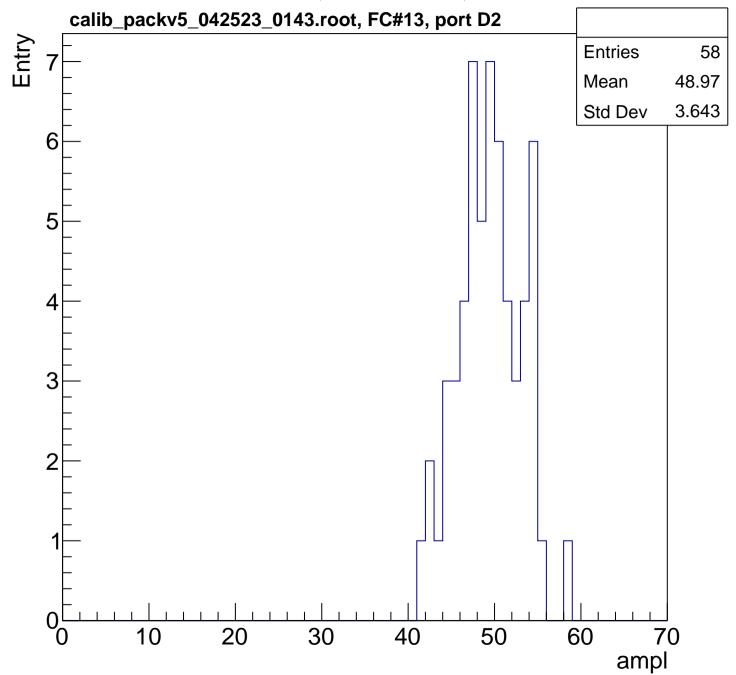


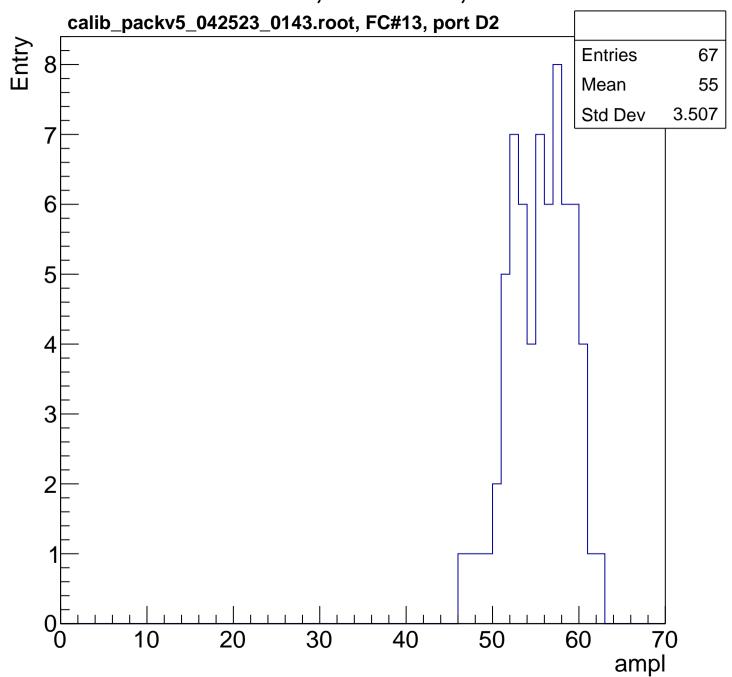
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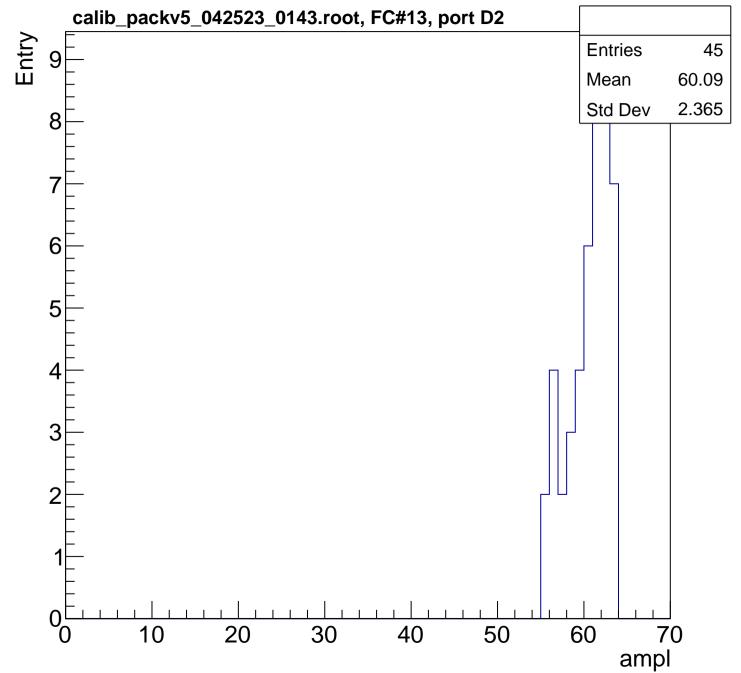


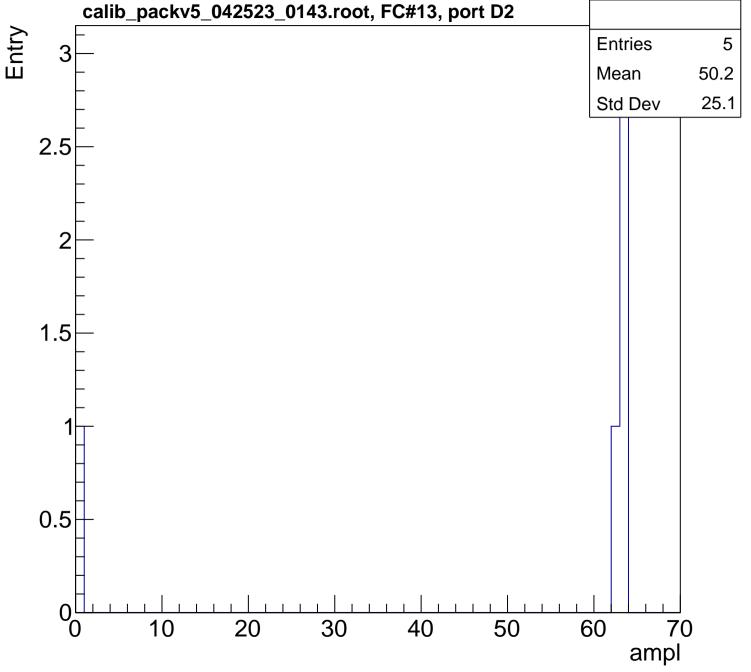




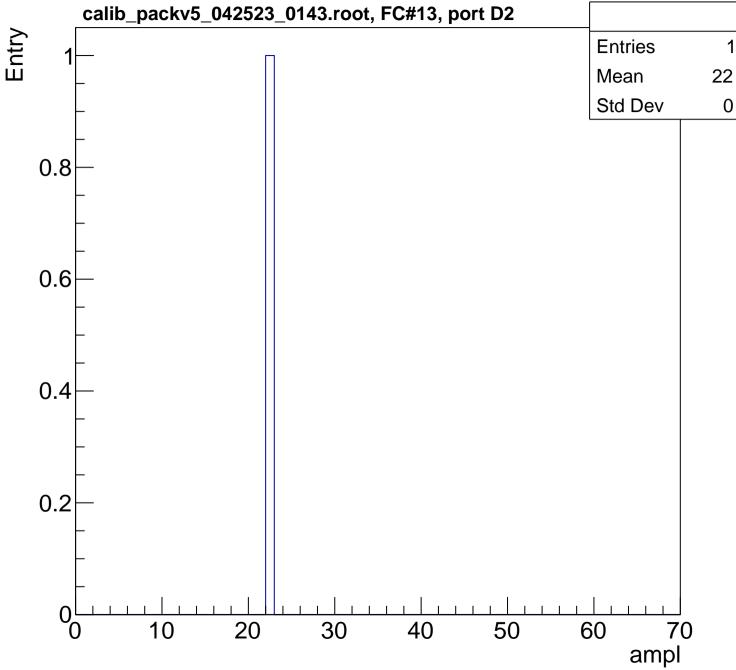


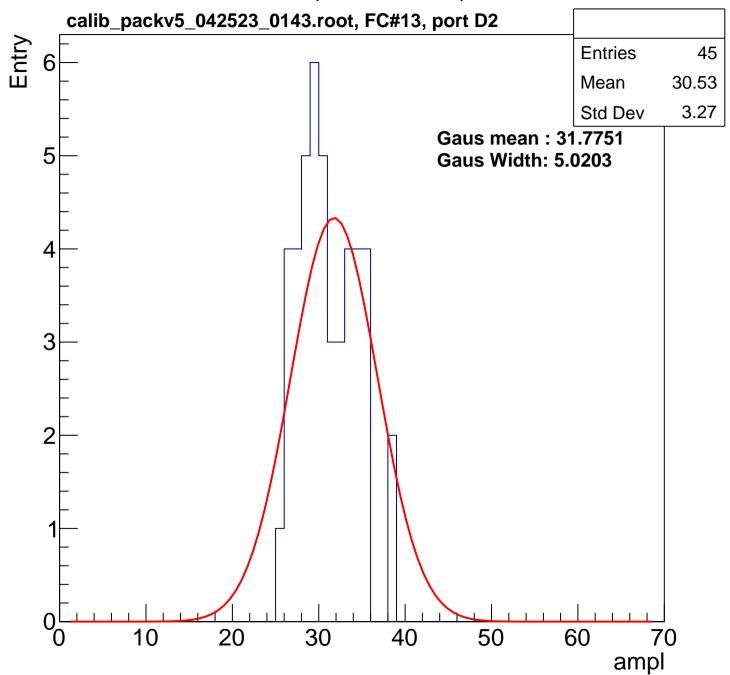


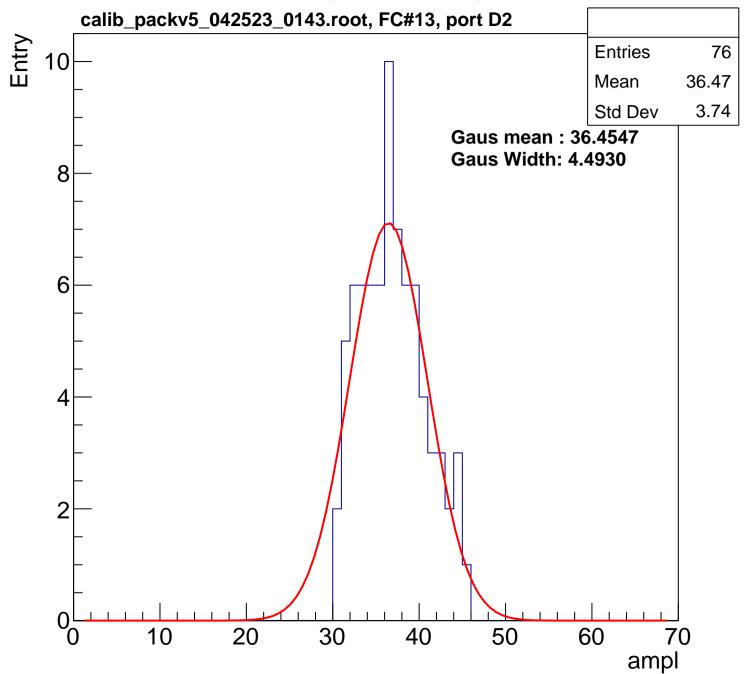


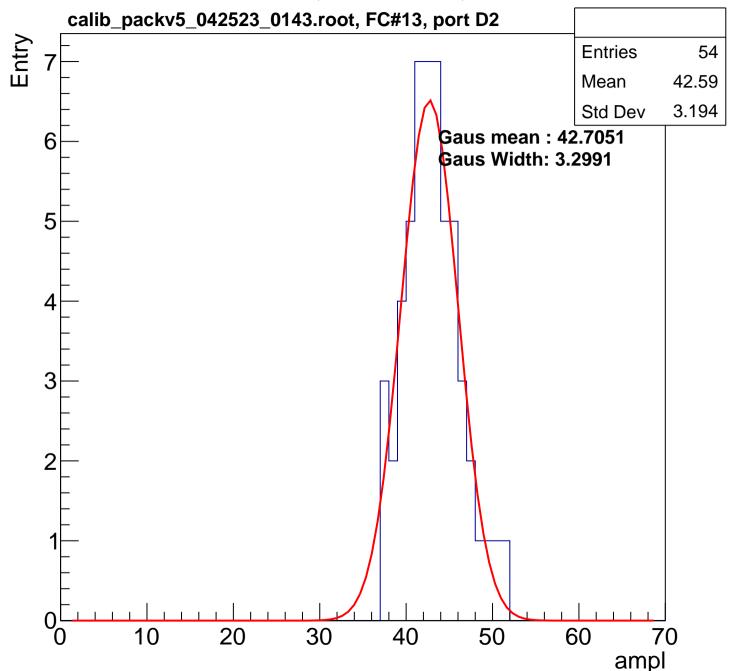


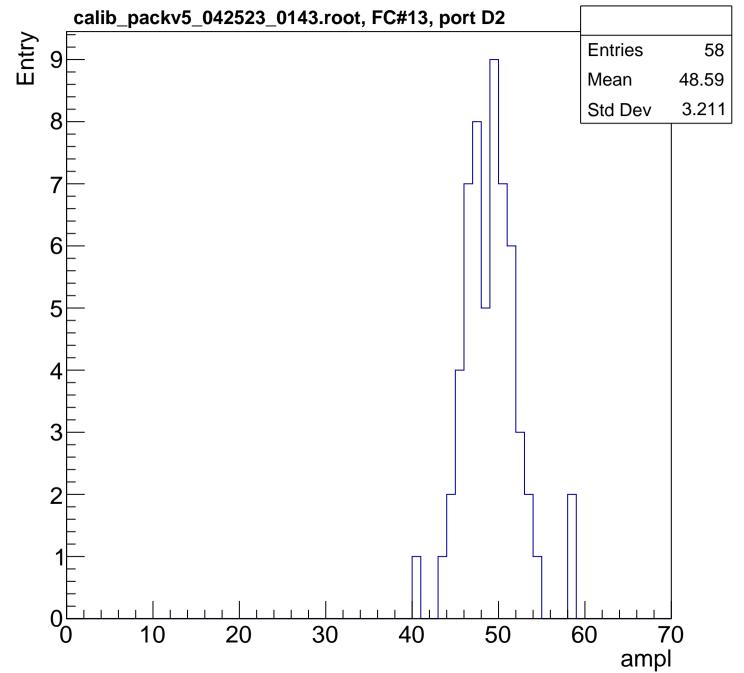
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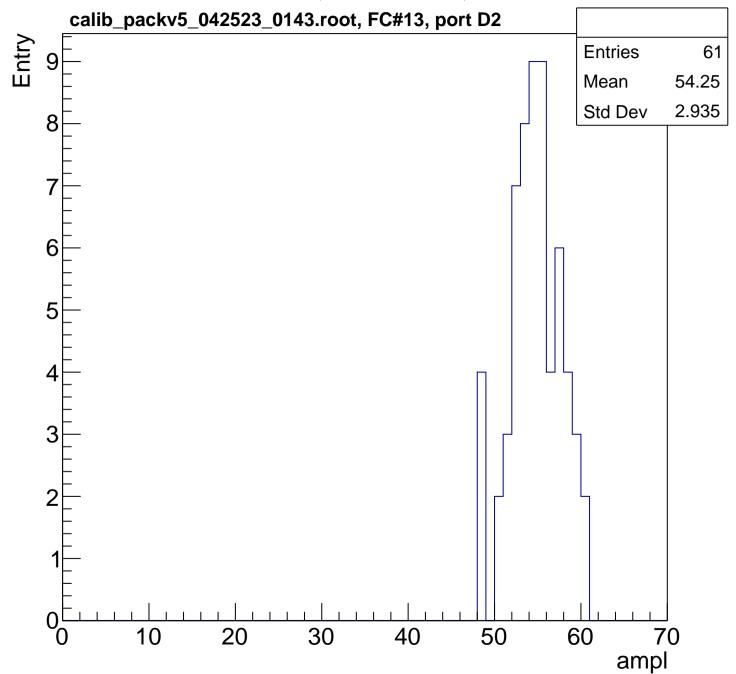


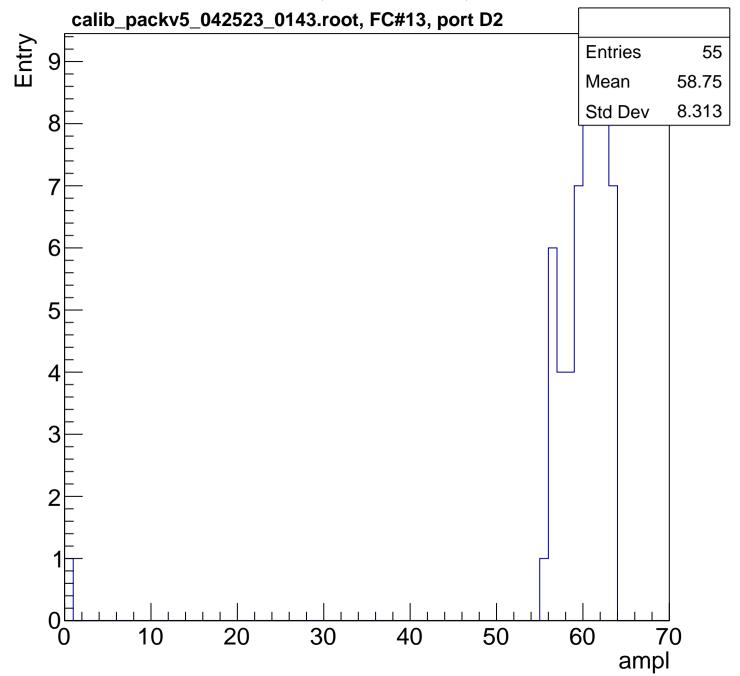


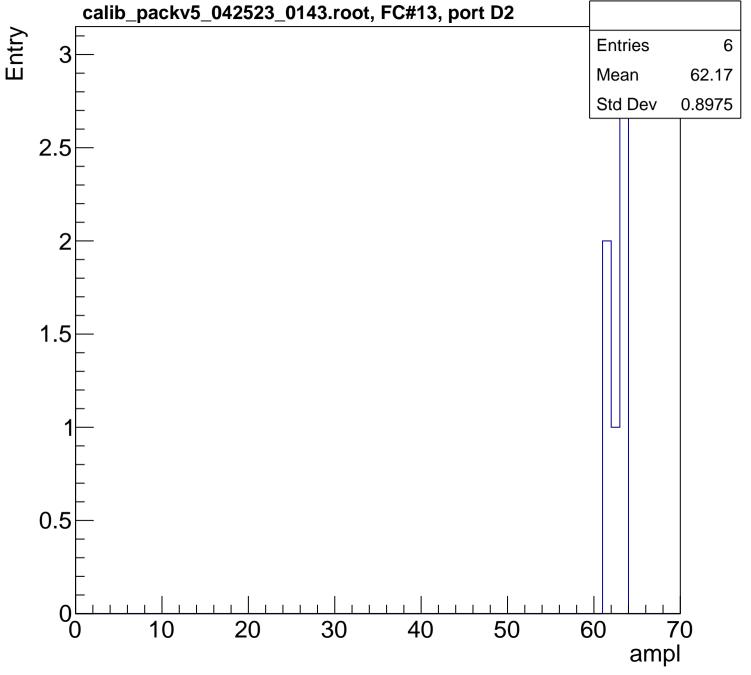




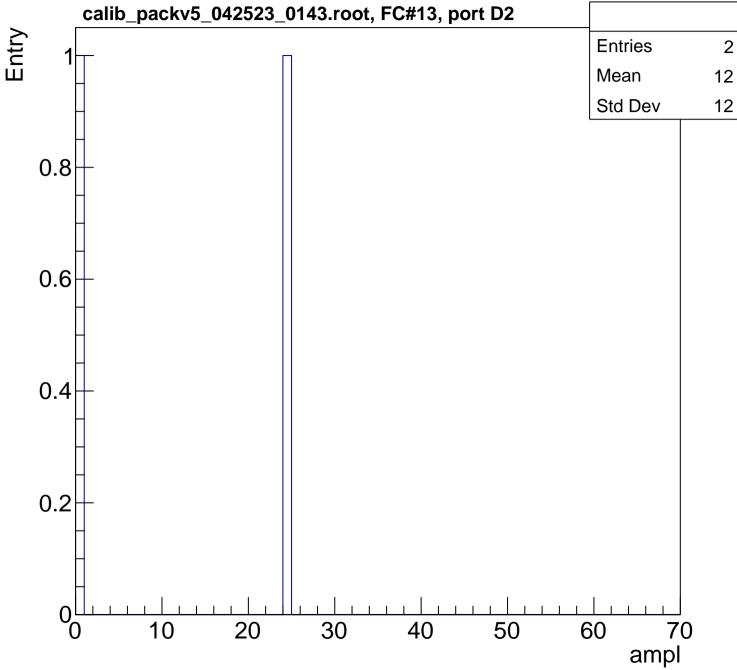


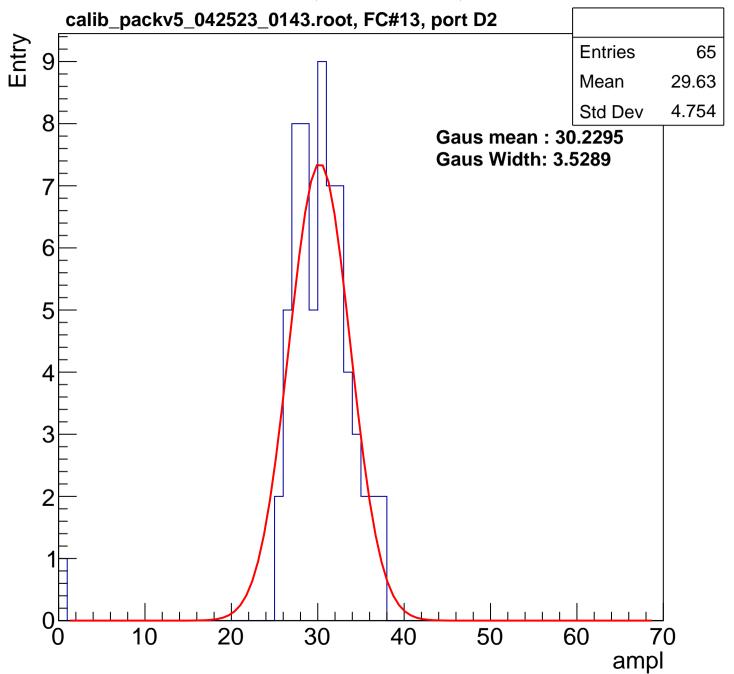


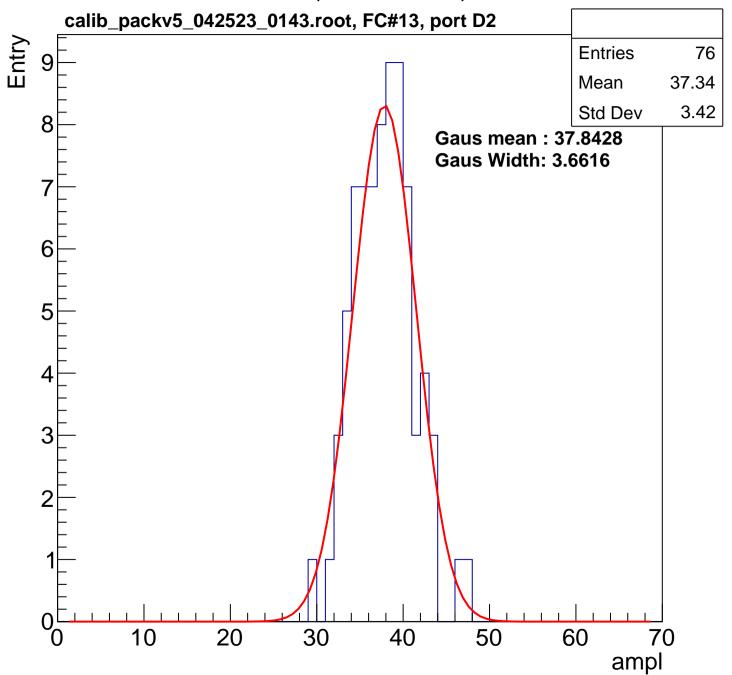


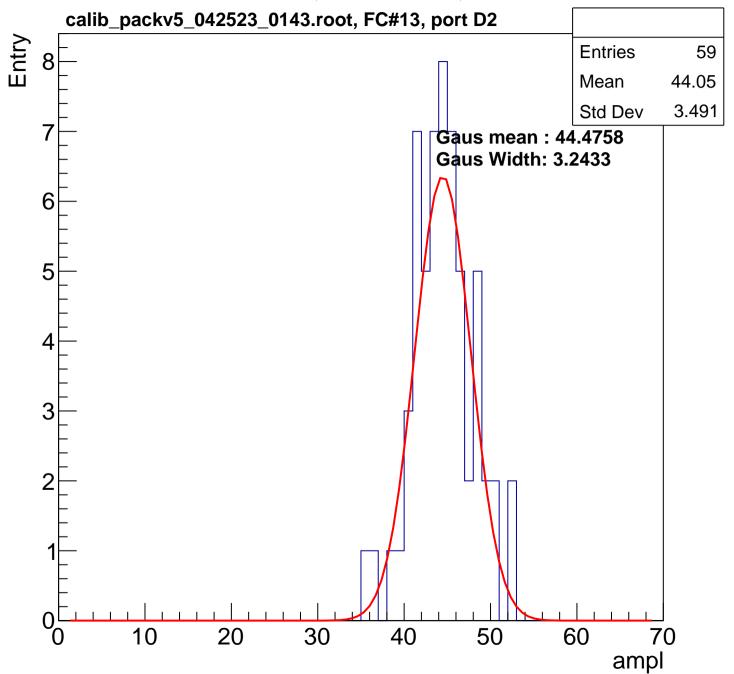


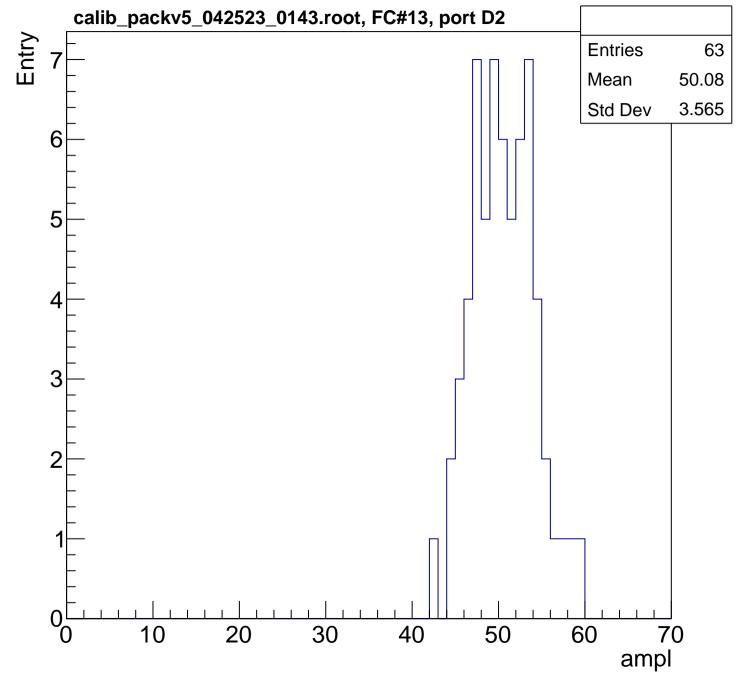
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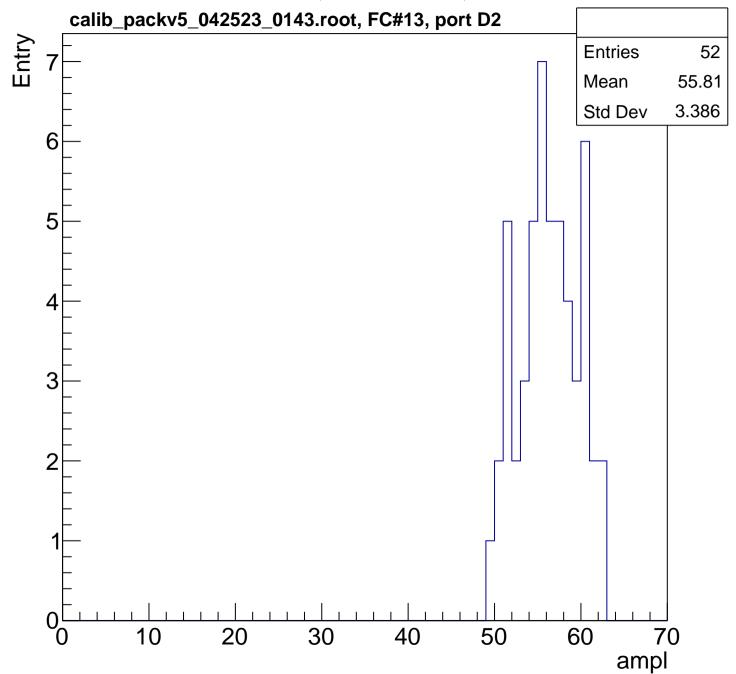


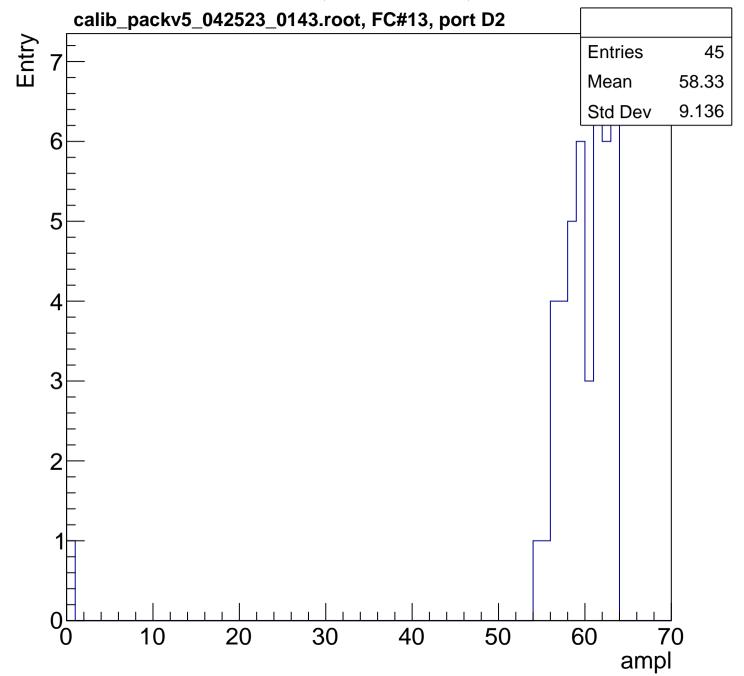


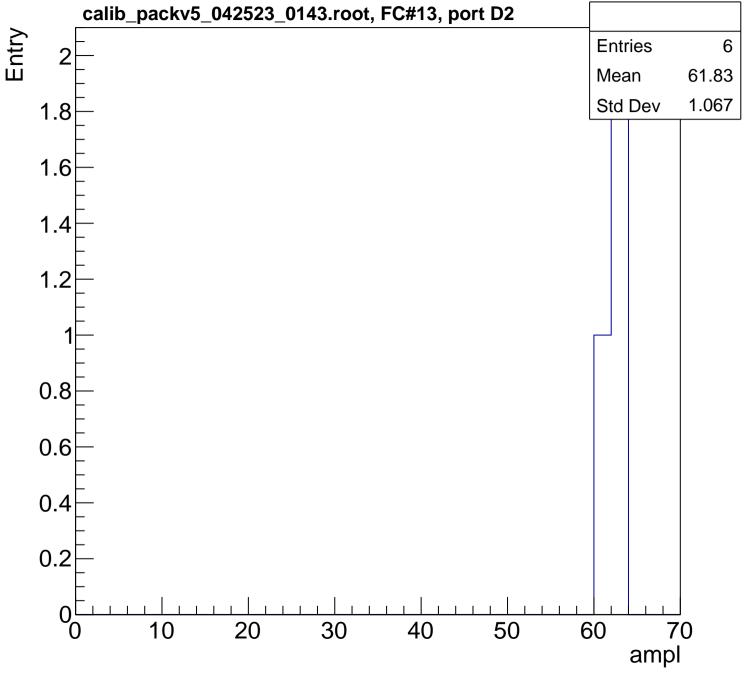


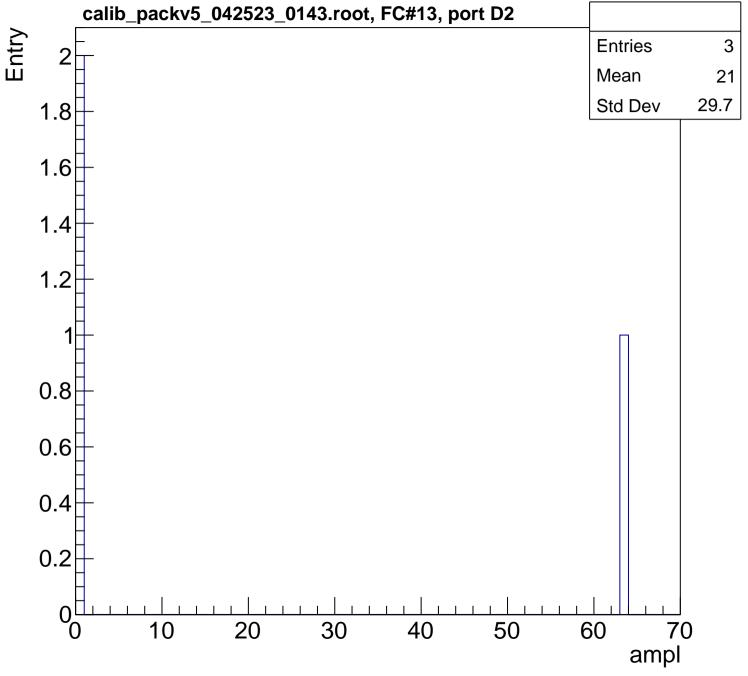


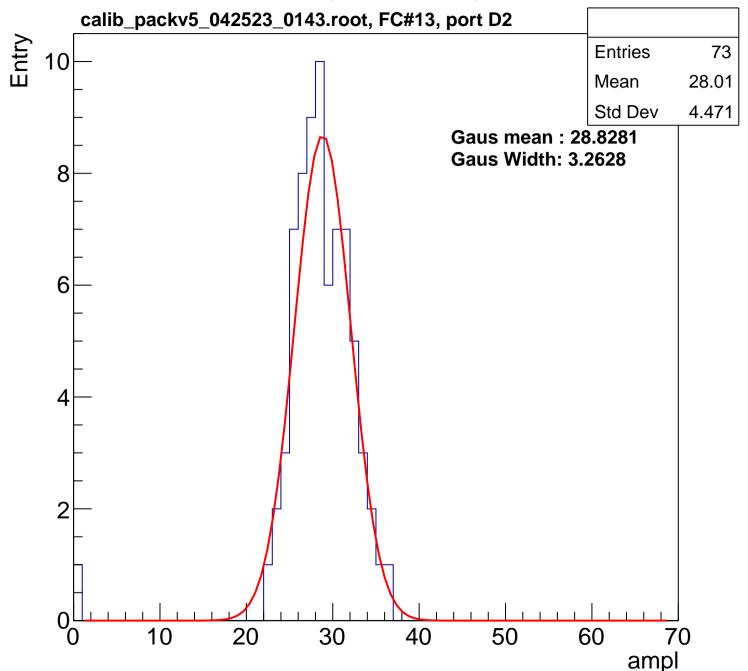


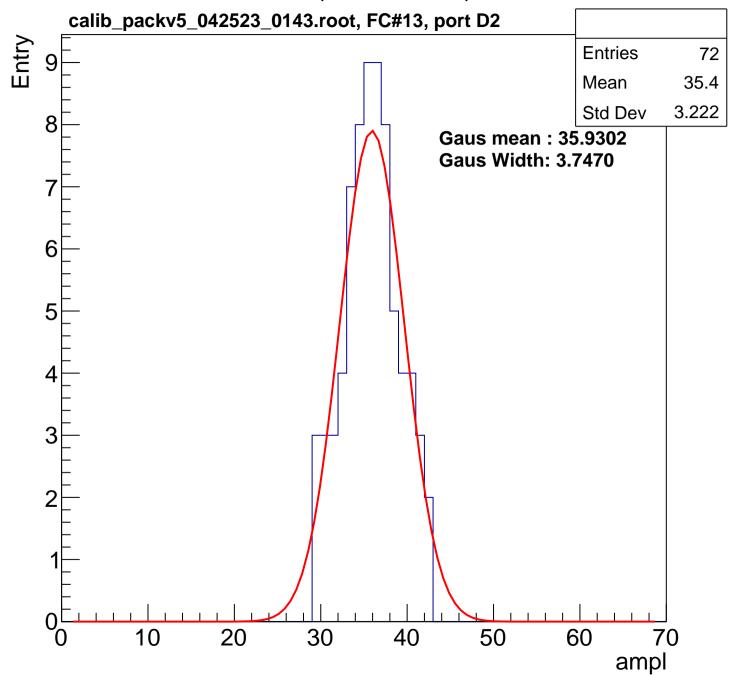


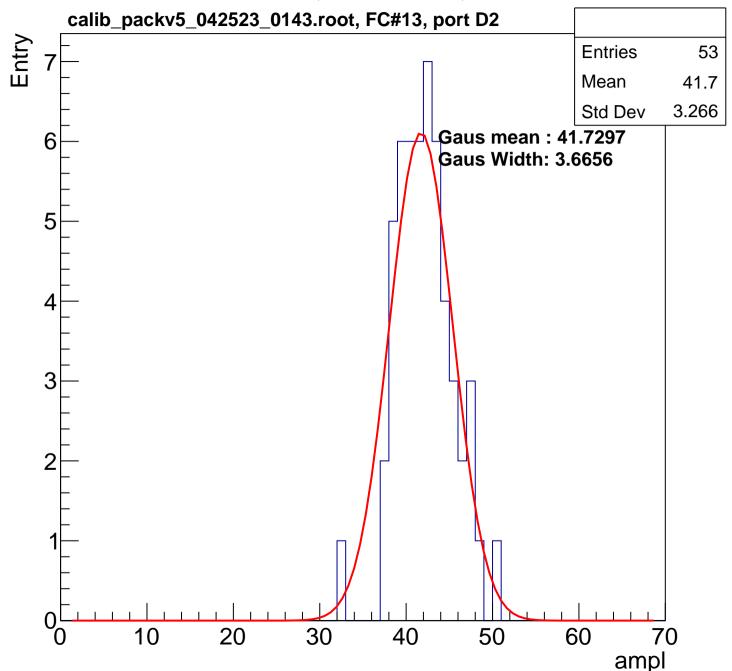


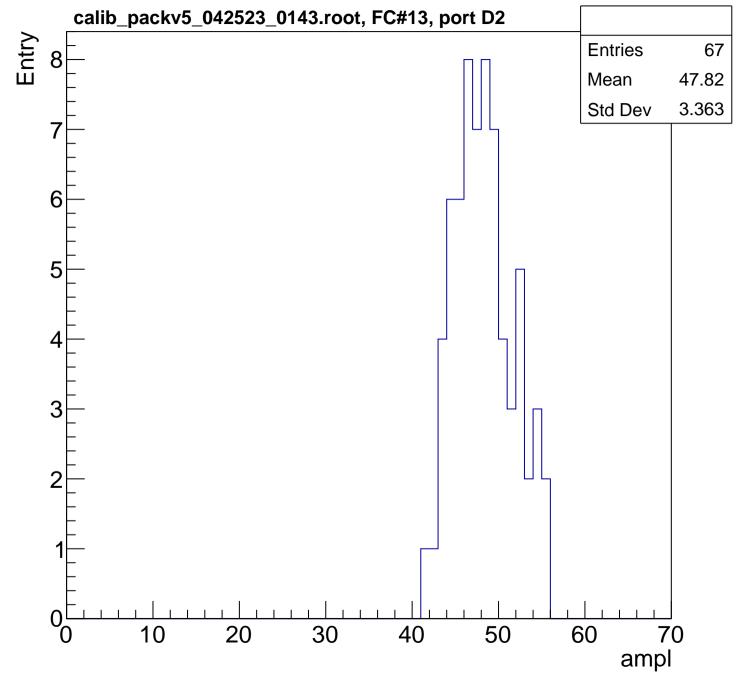


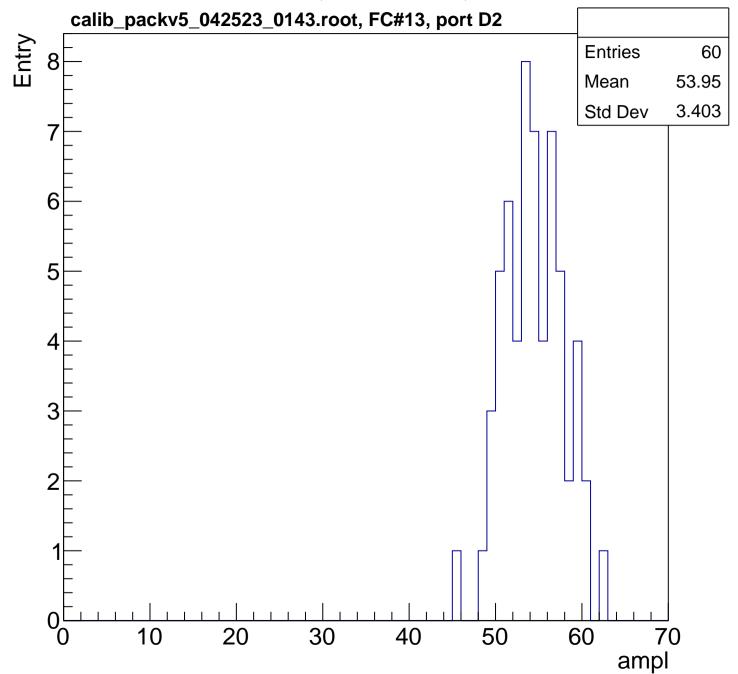


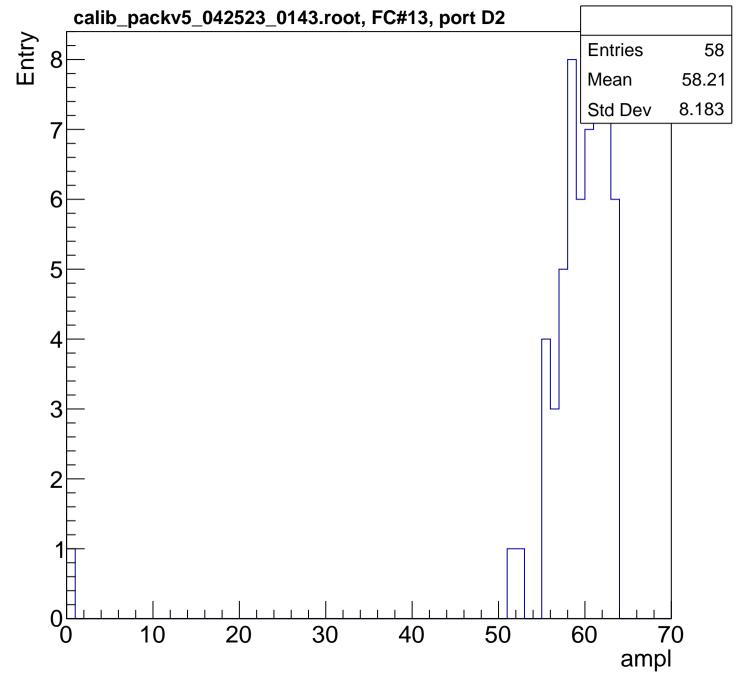


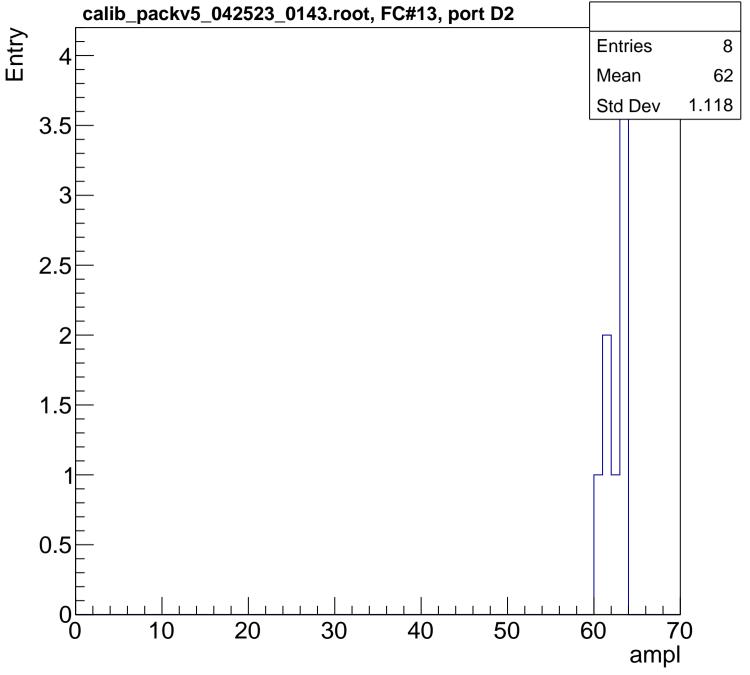




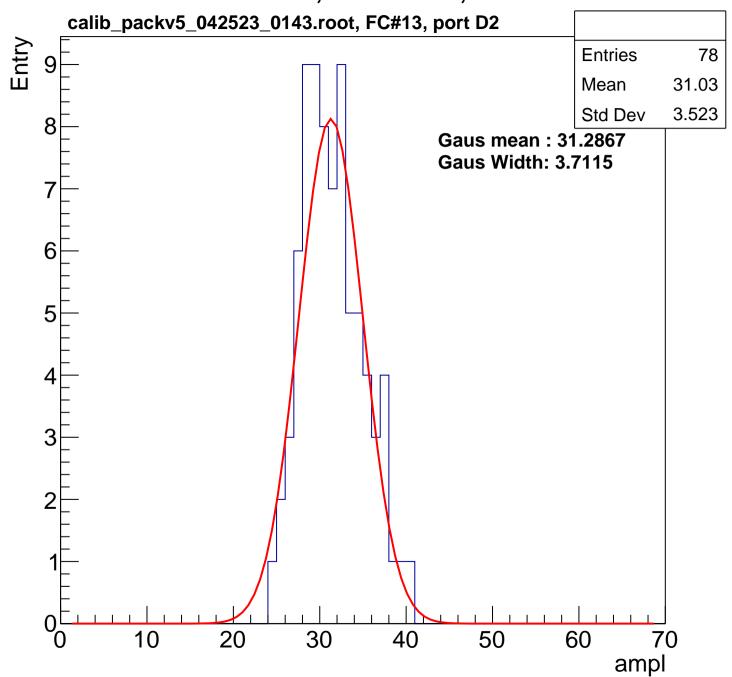


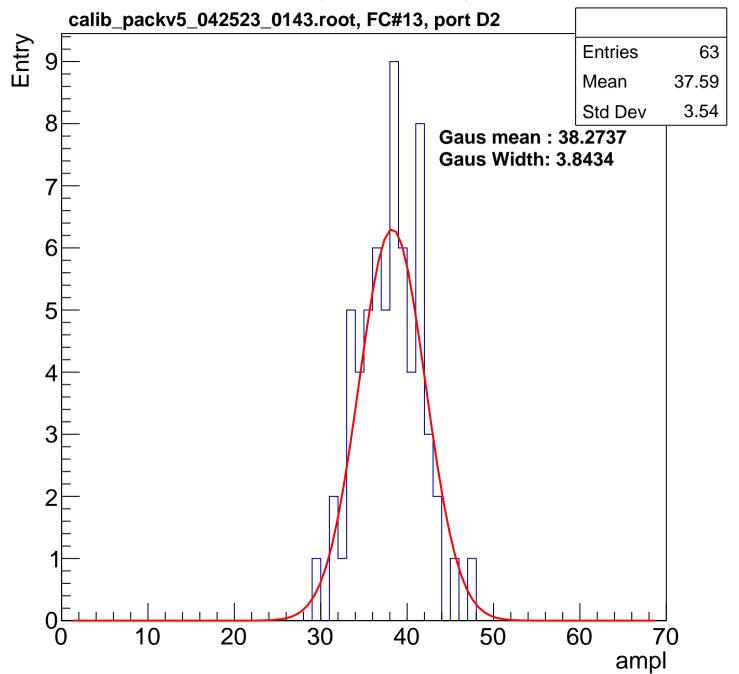


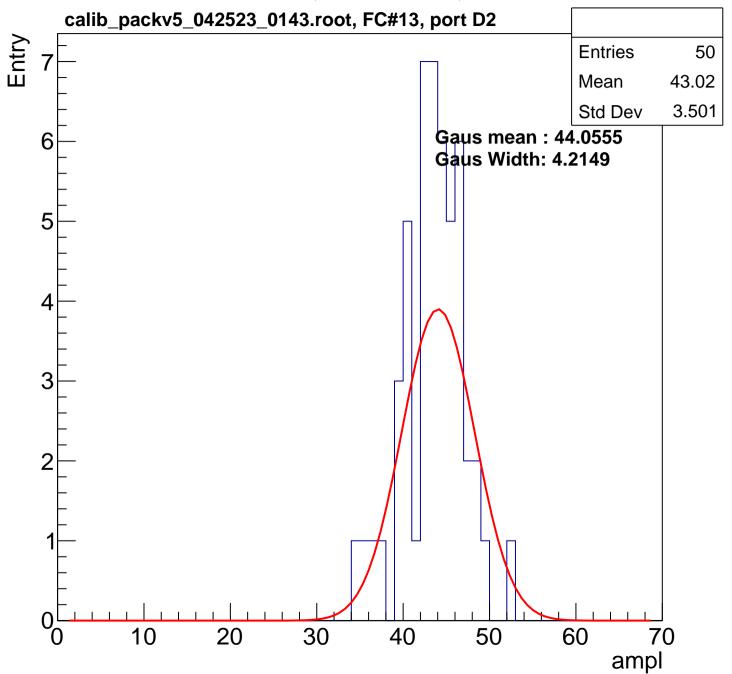


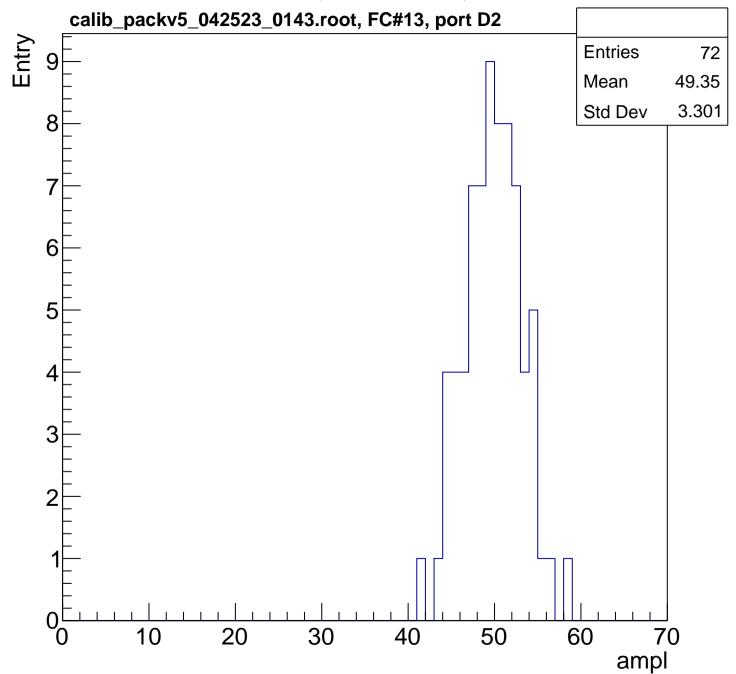


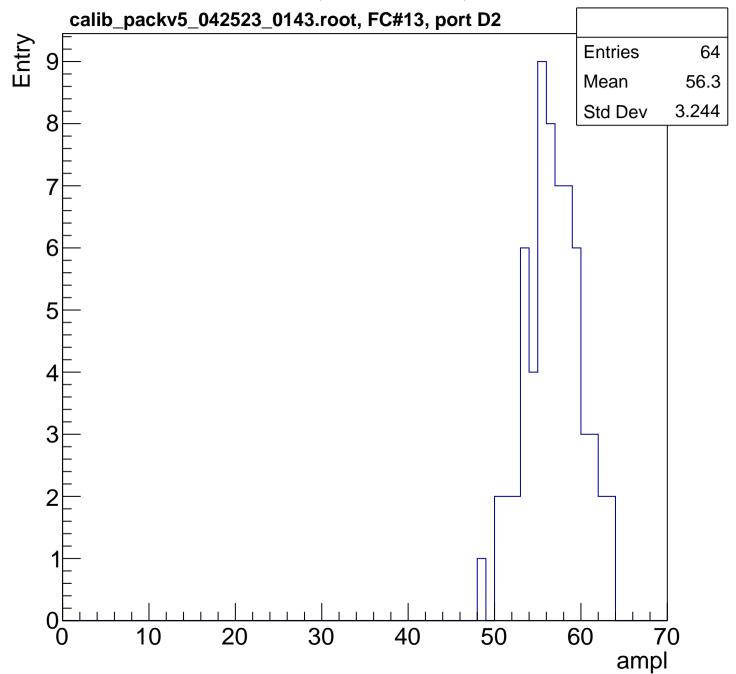
B1L003S, U2-ch62, adc7 calib_packv5_042523_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

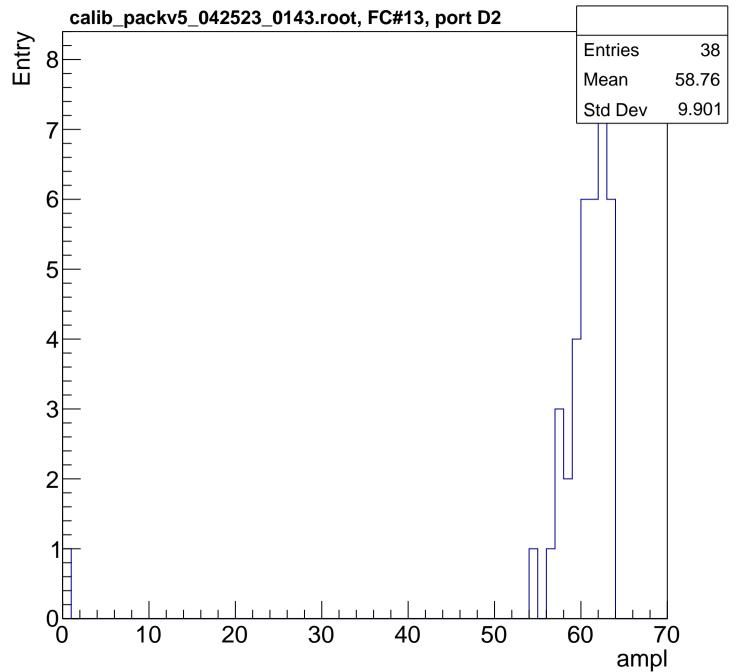


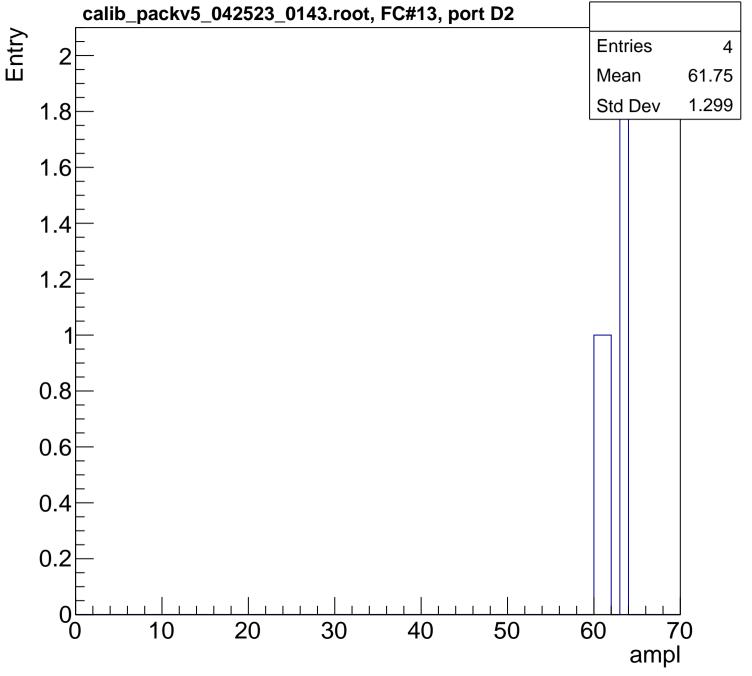


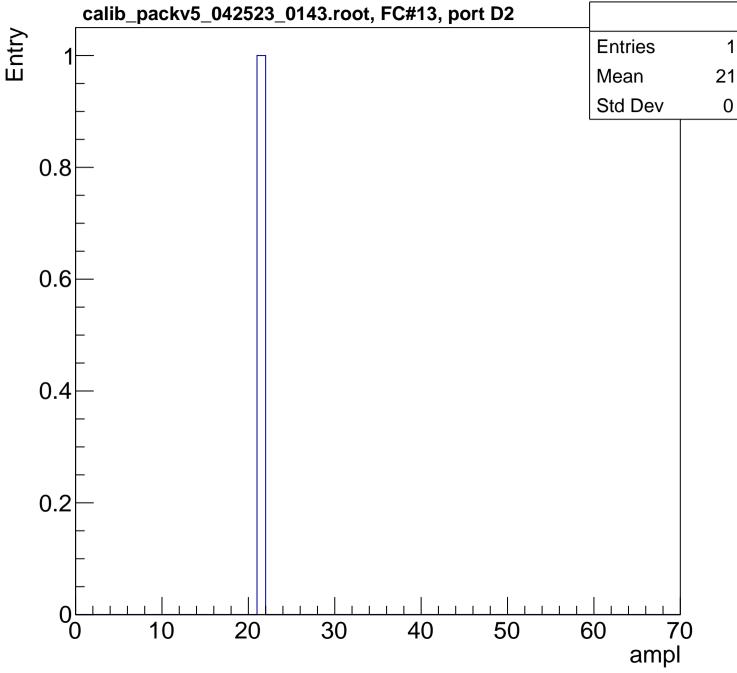


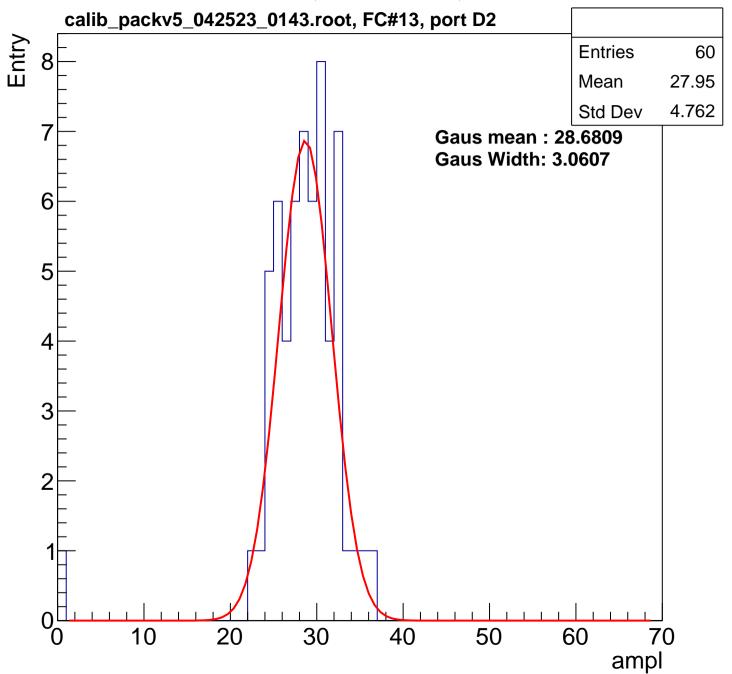


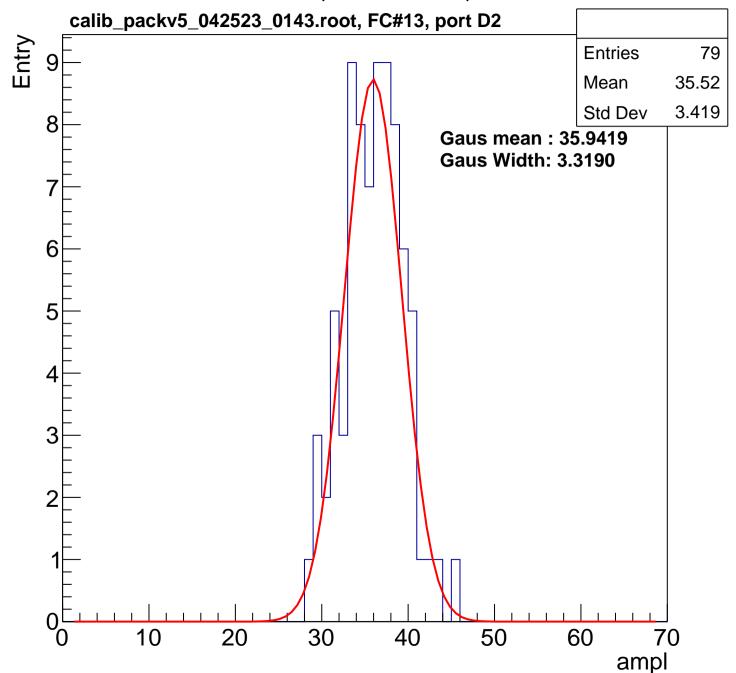


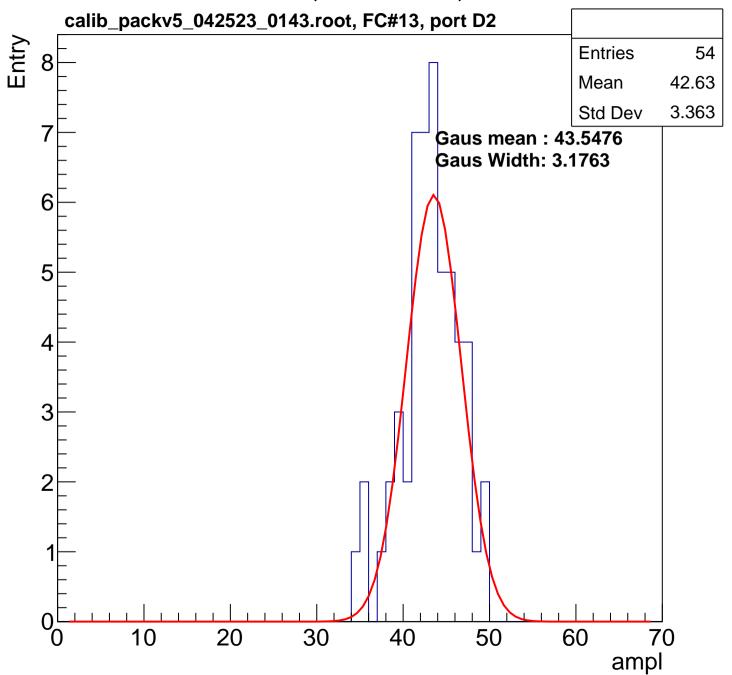


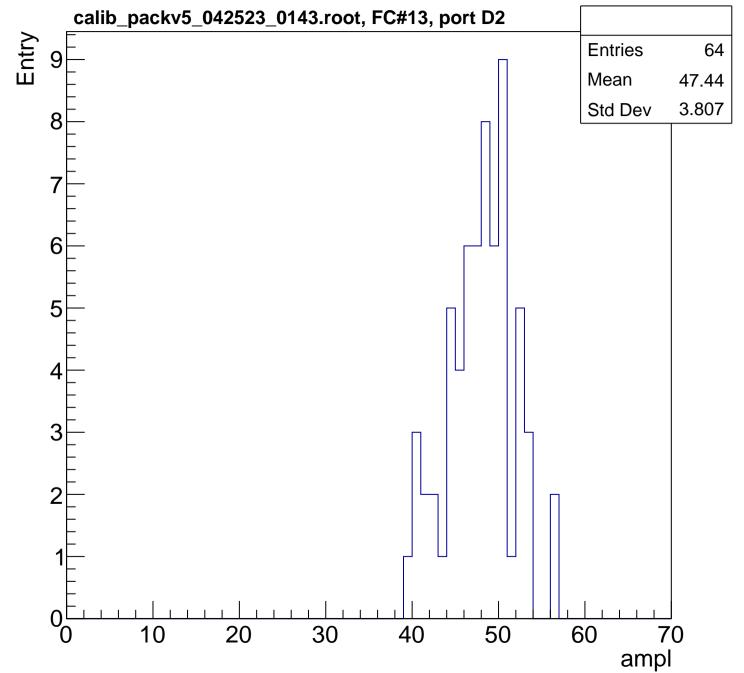


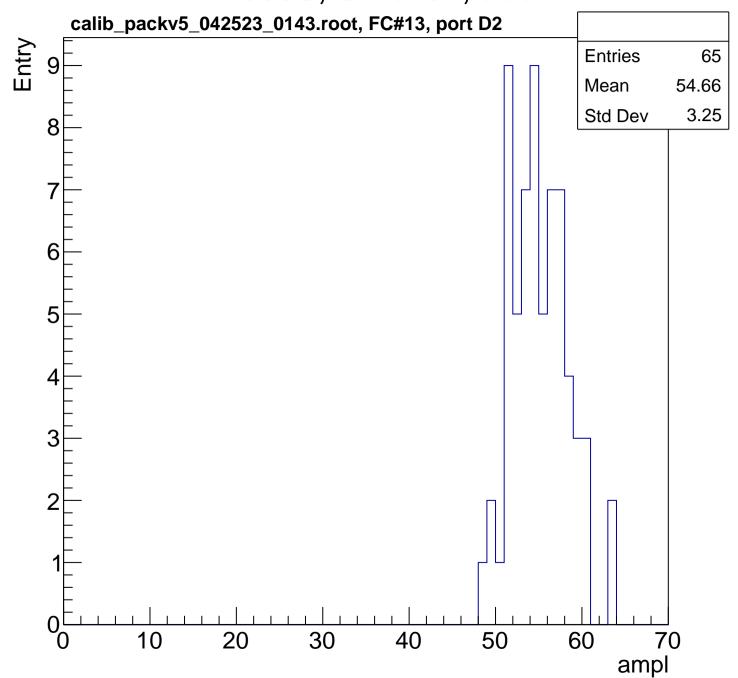


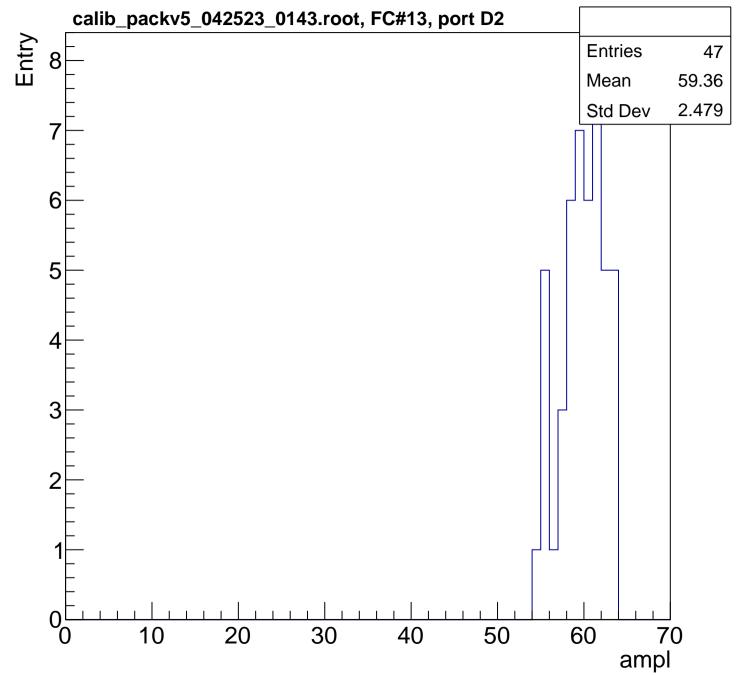


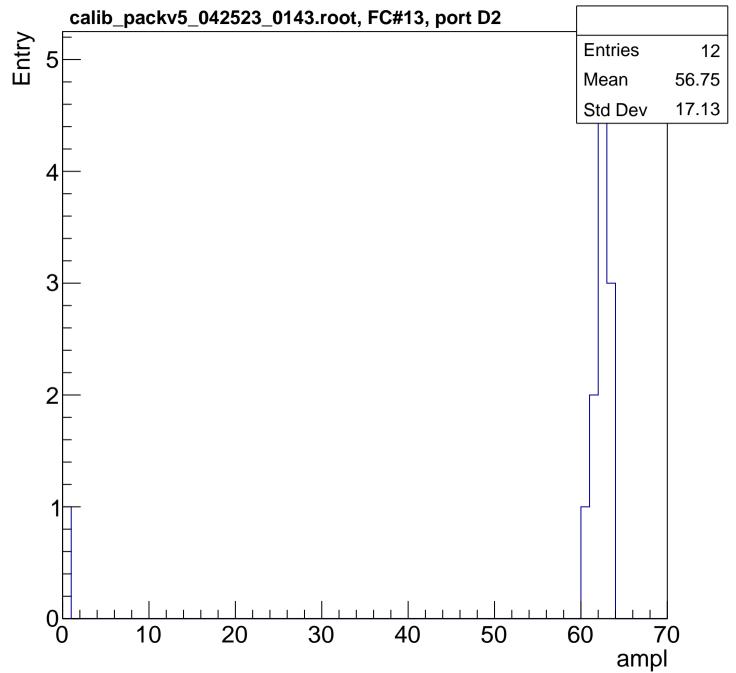


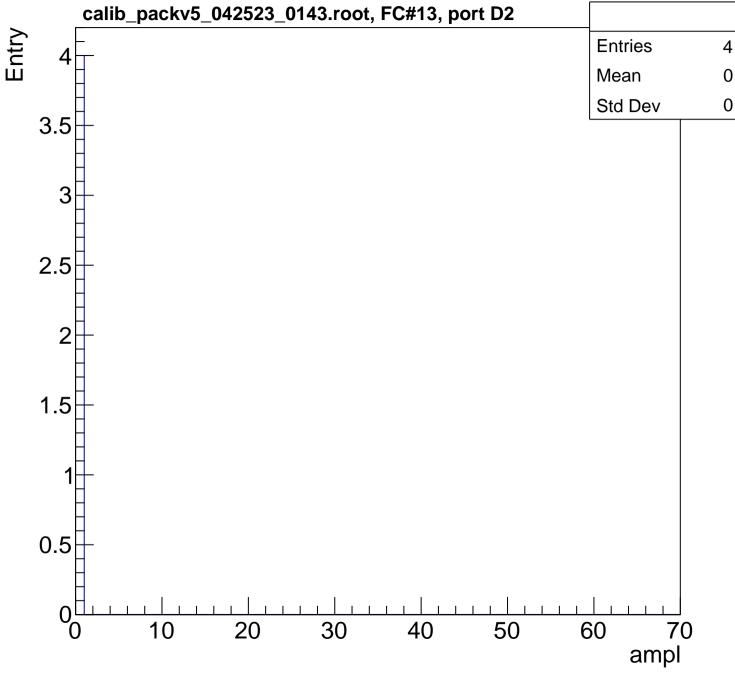


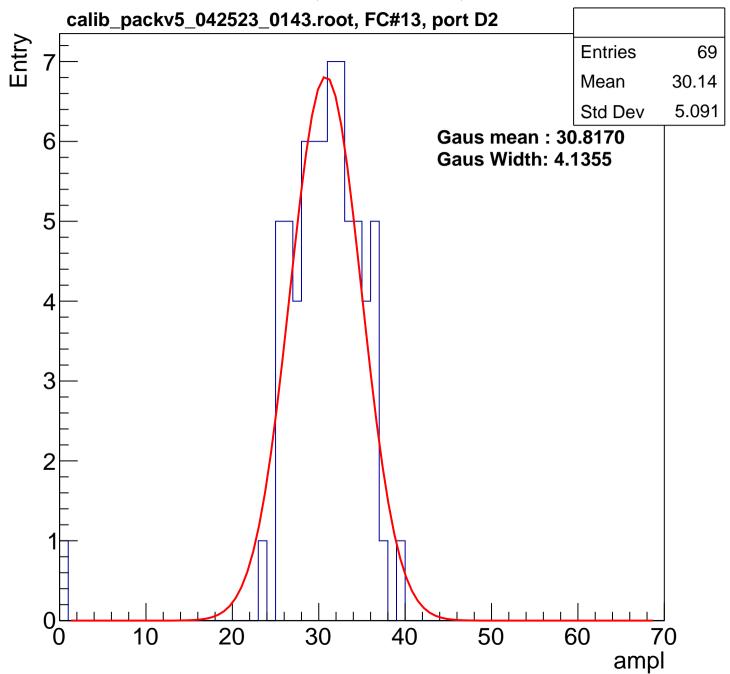


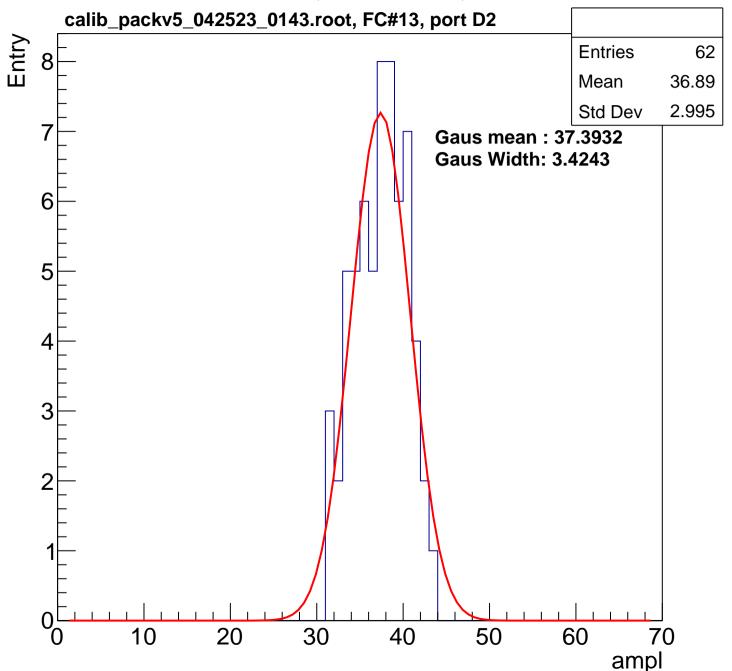


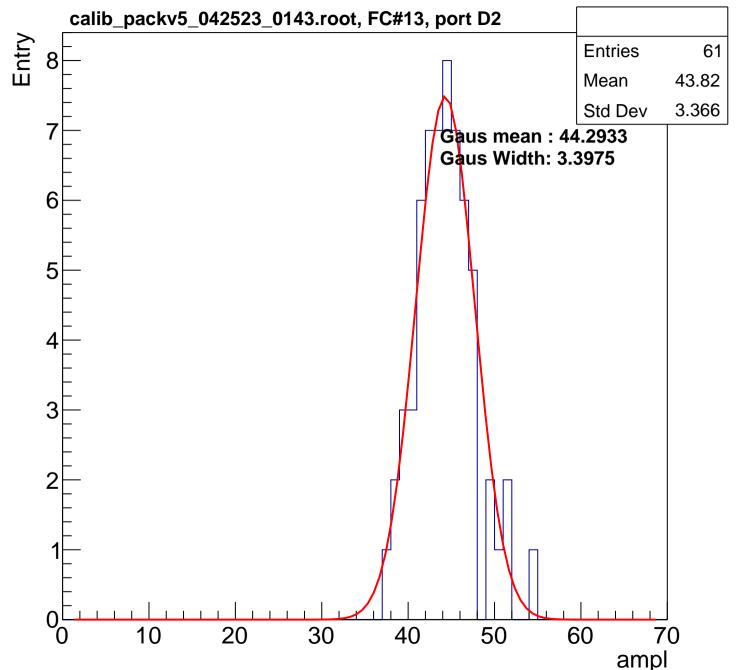


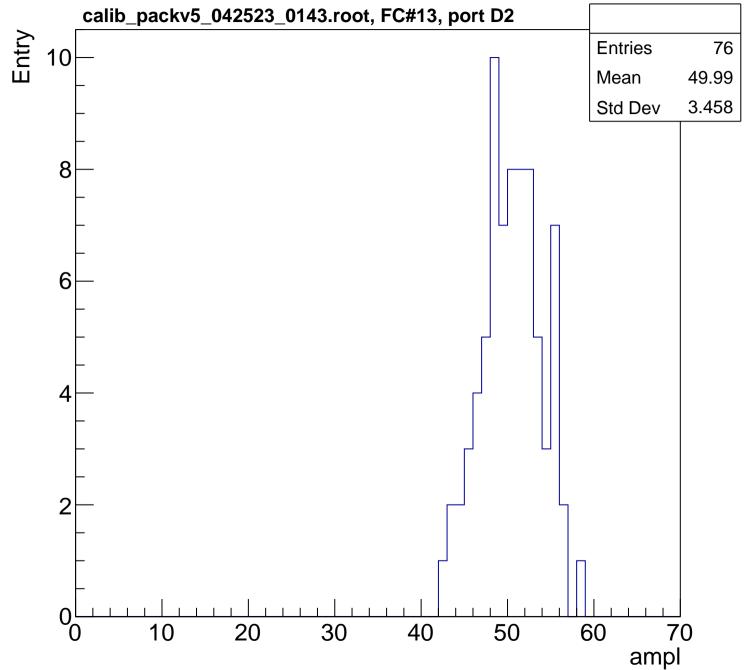


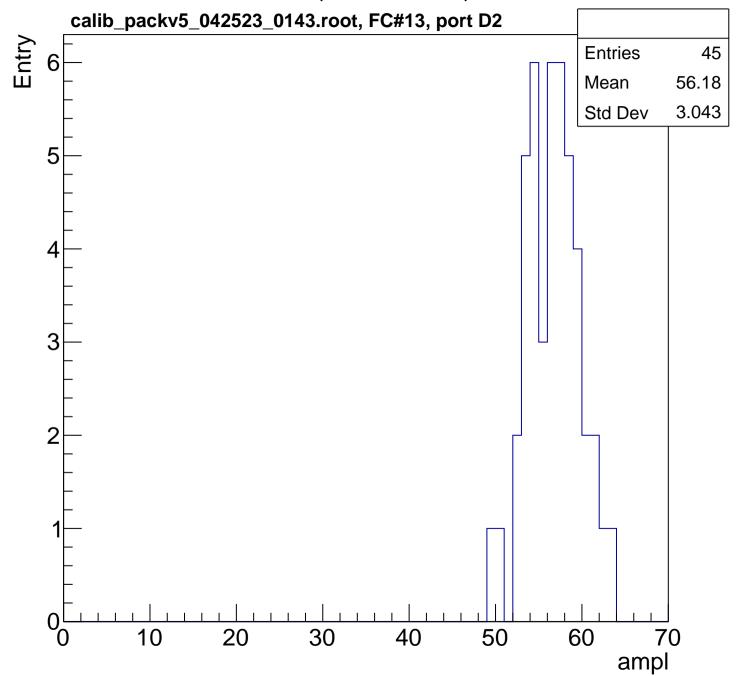


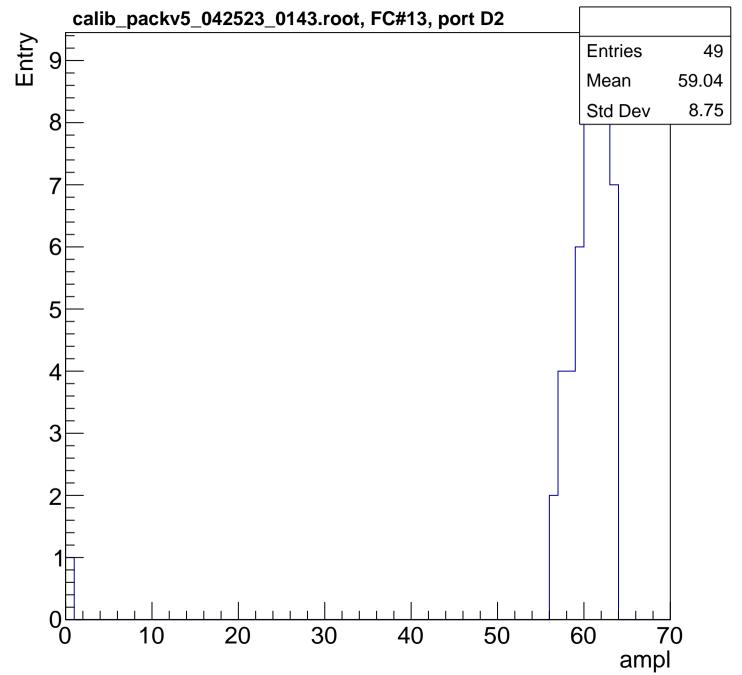


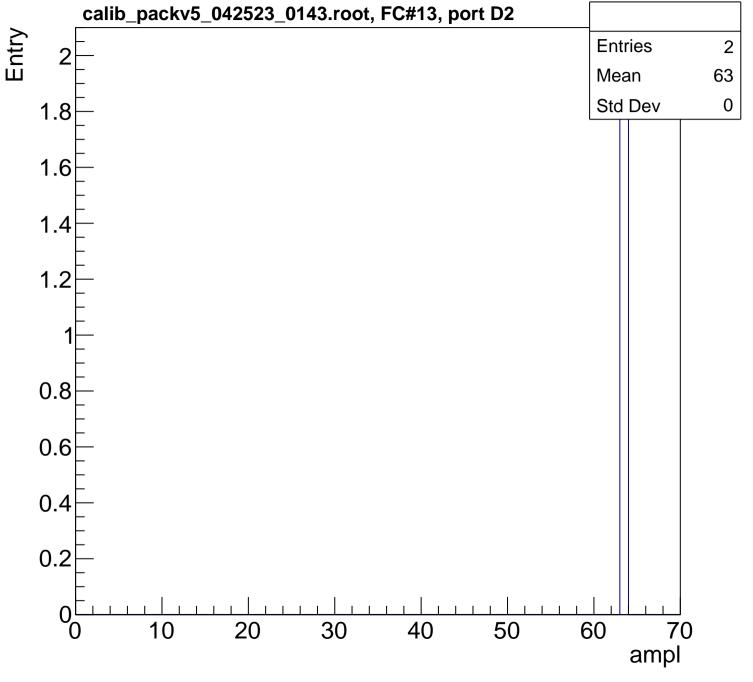


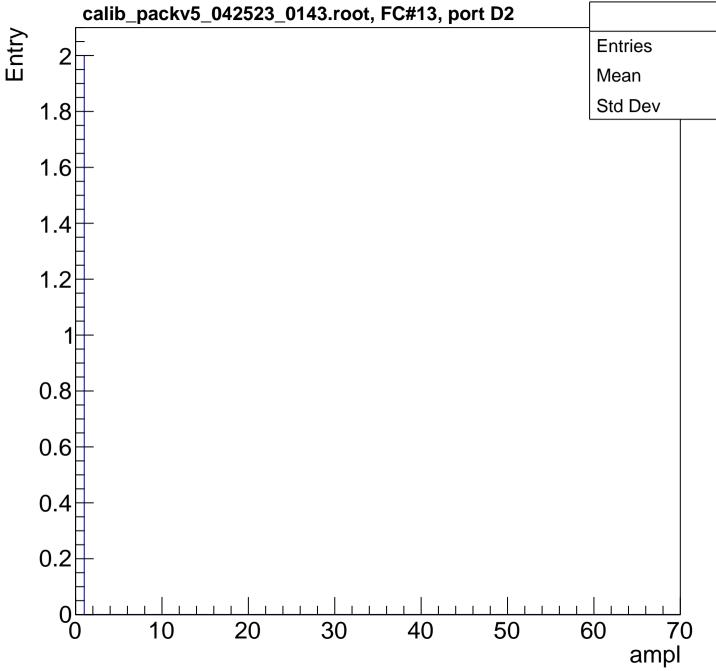


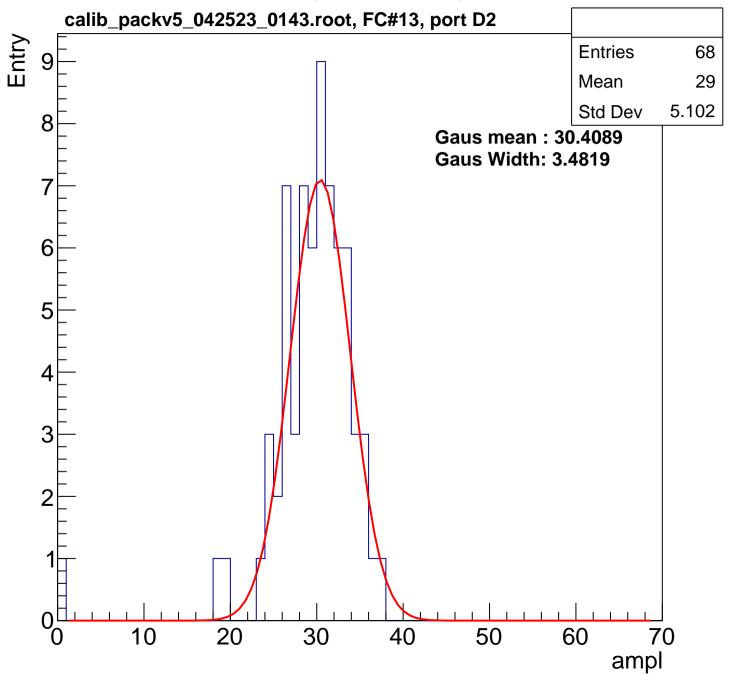


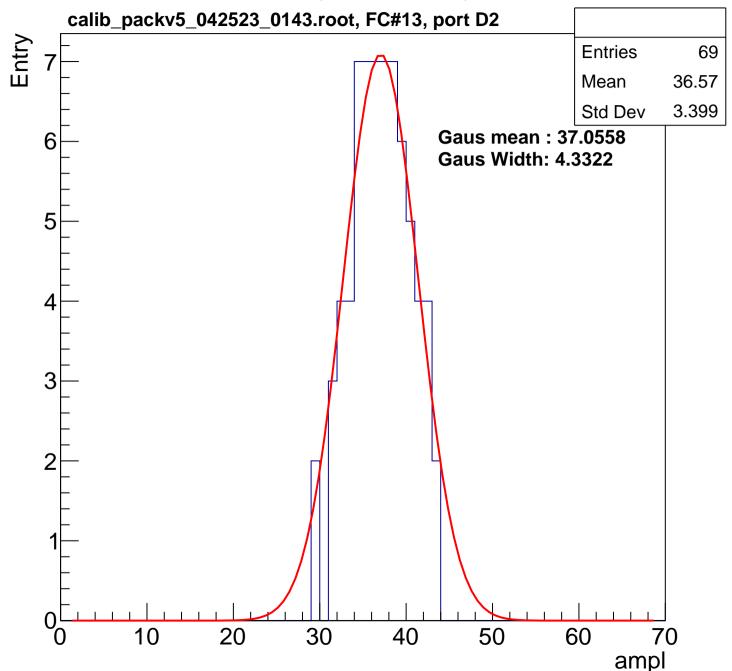


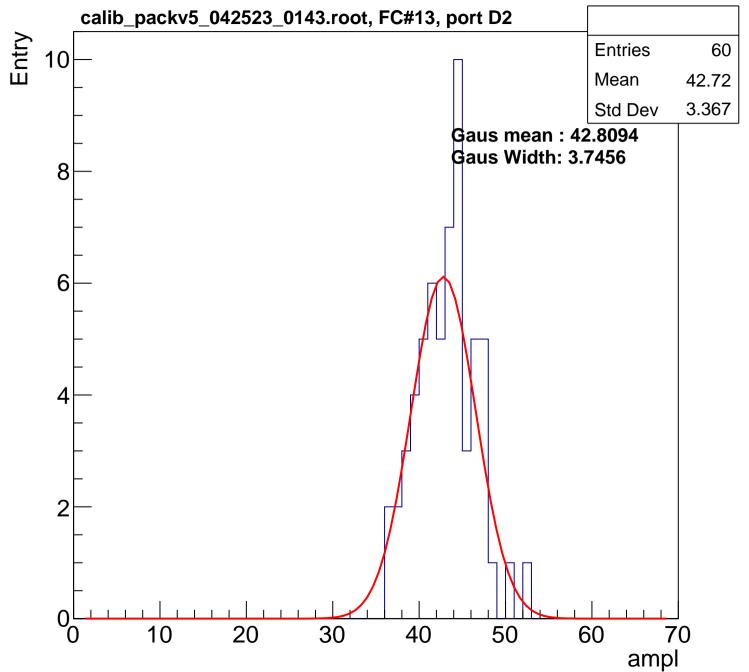


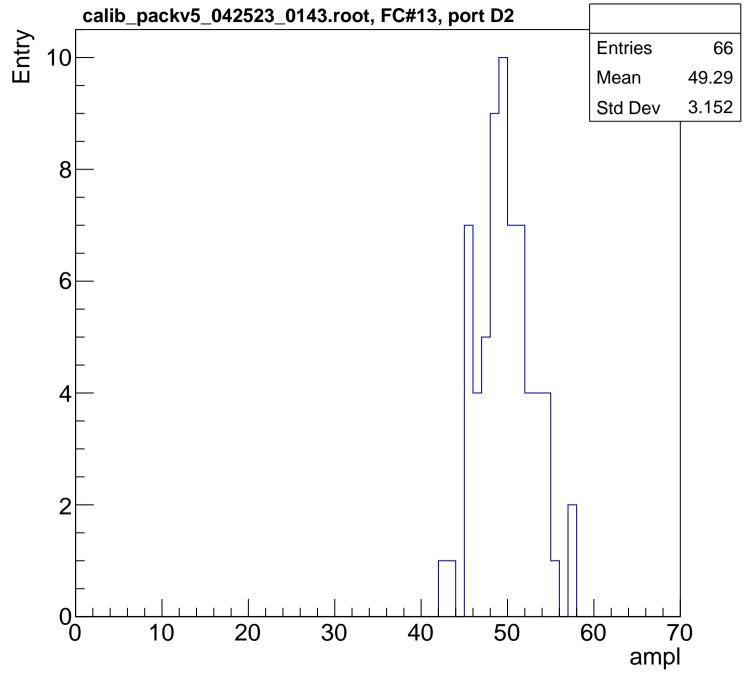


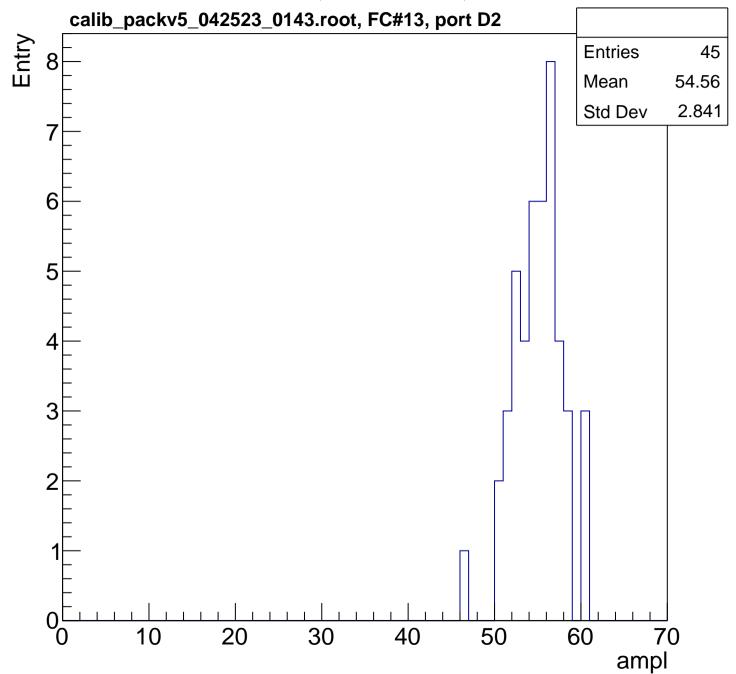


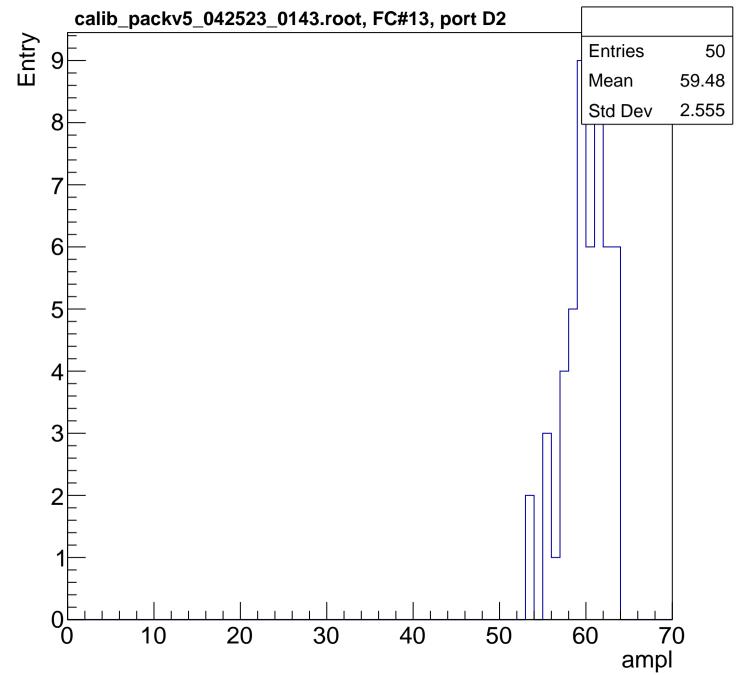


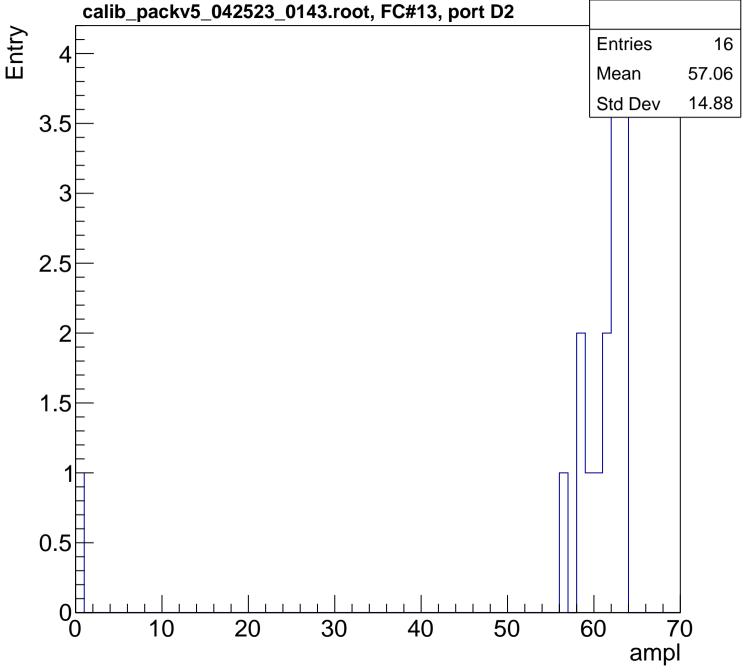




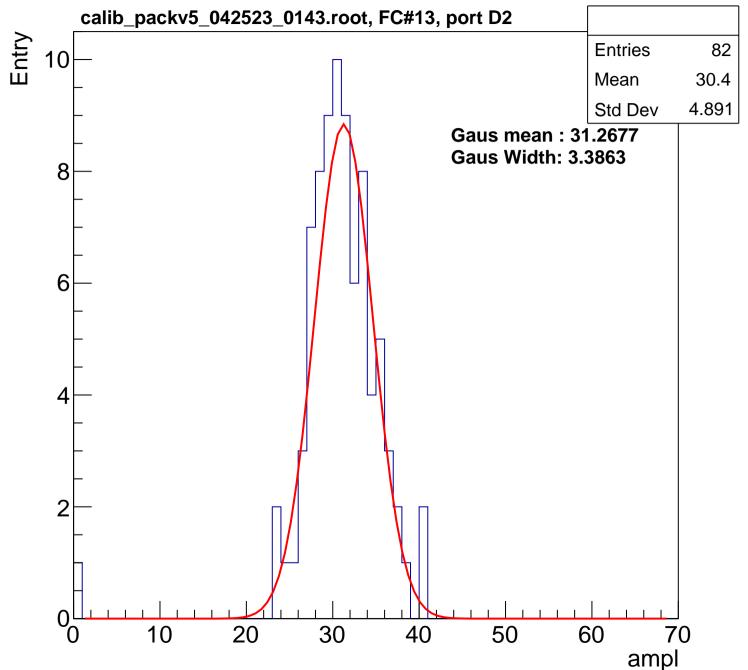


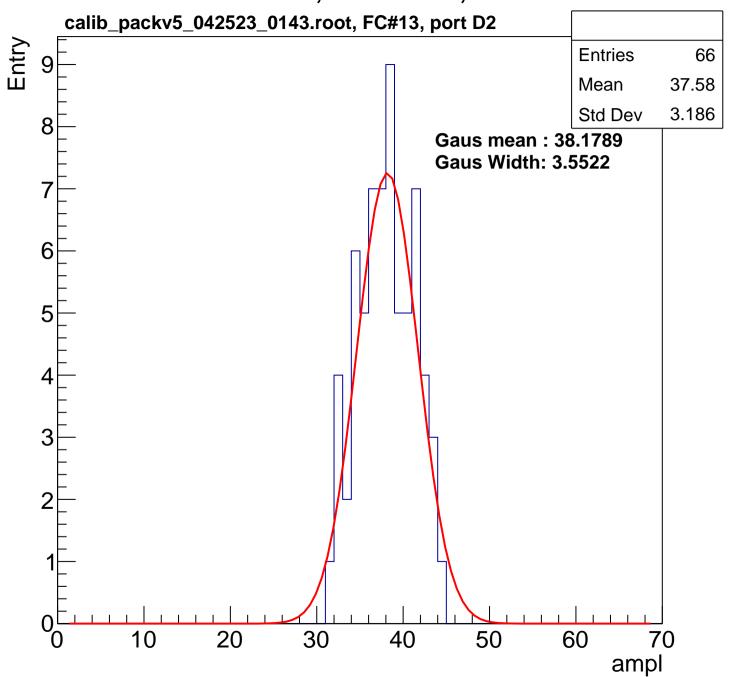


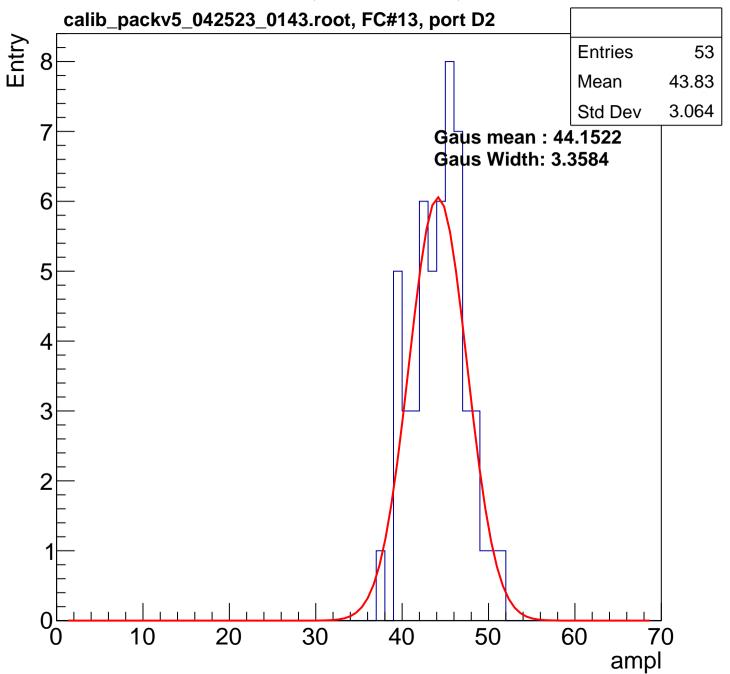


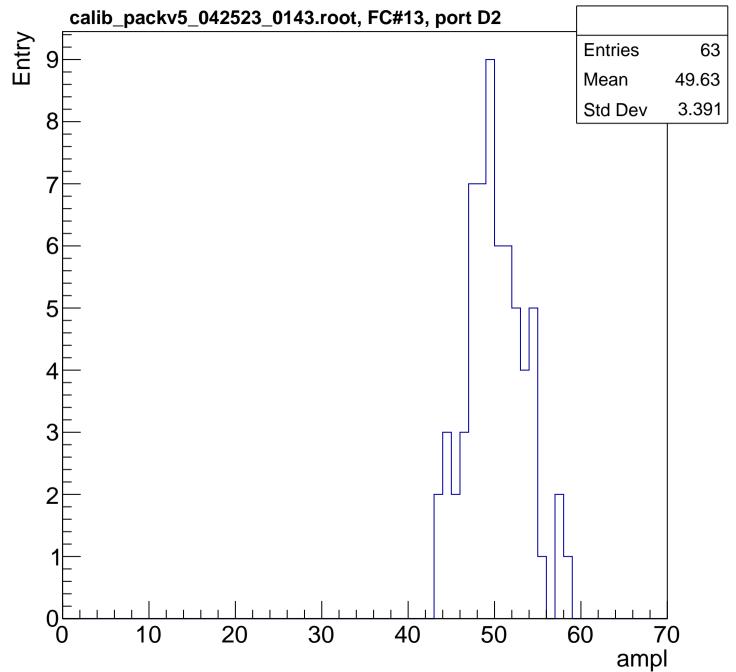


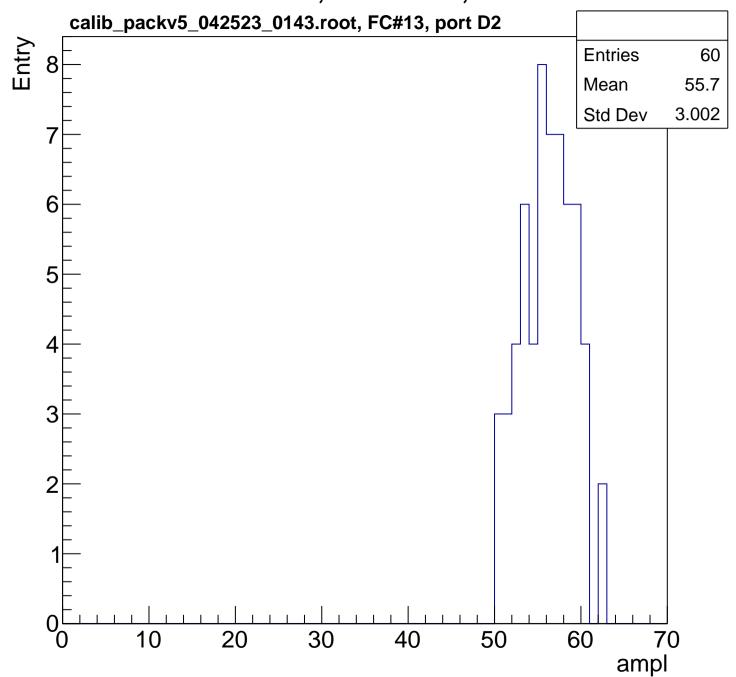


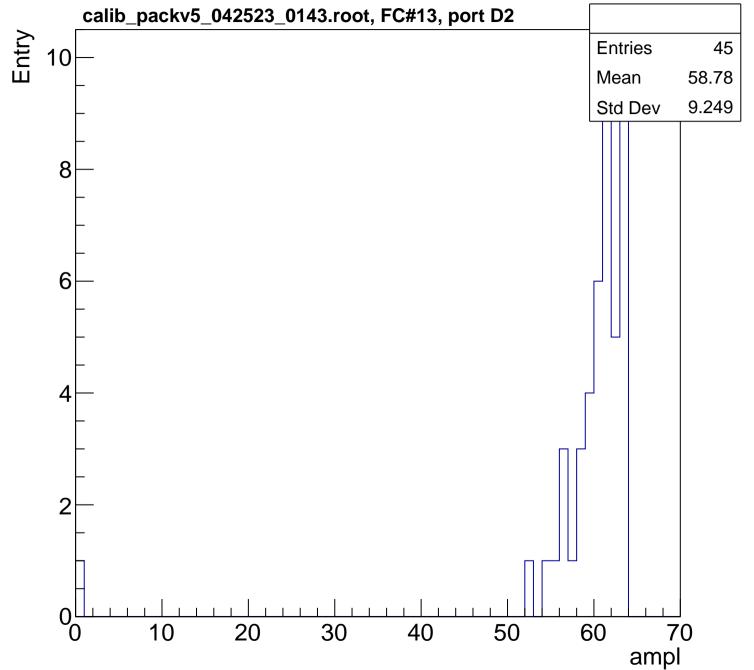


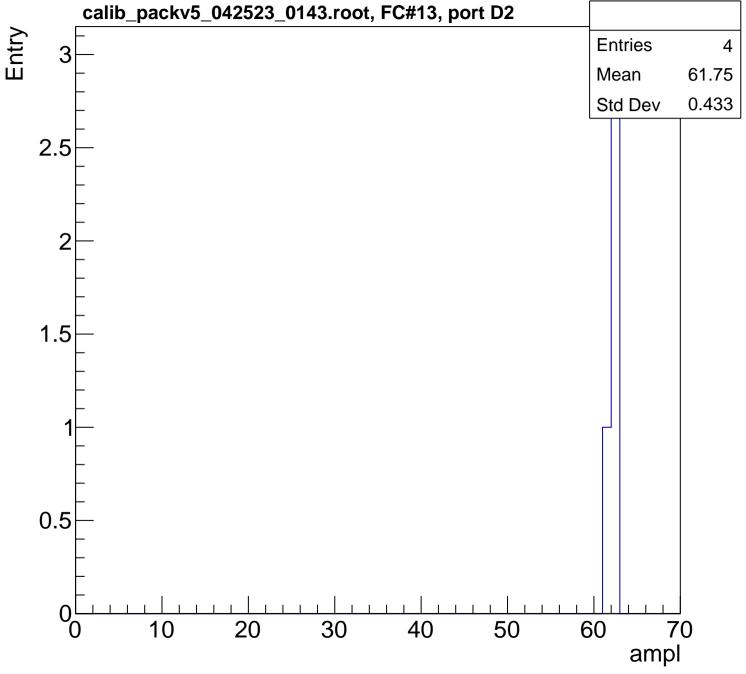




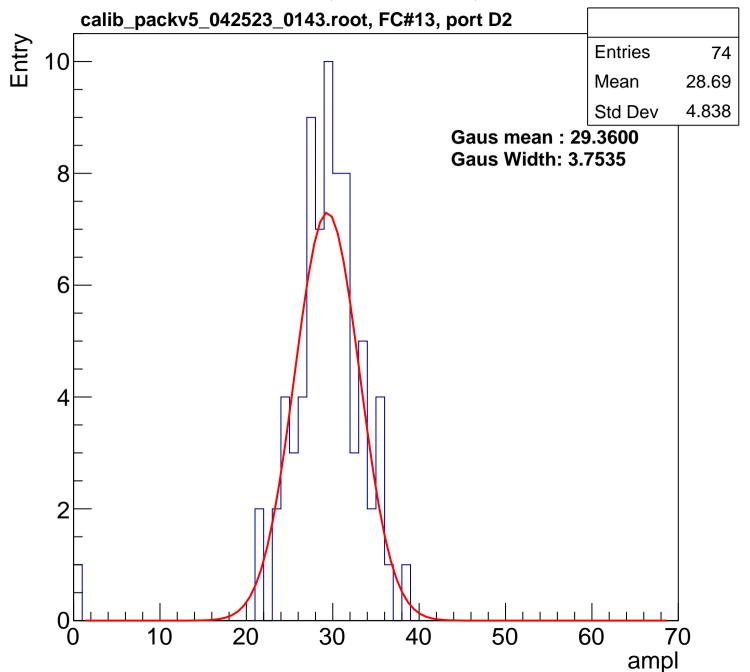


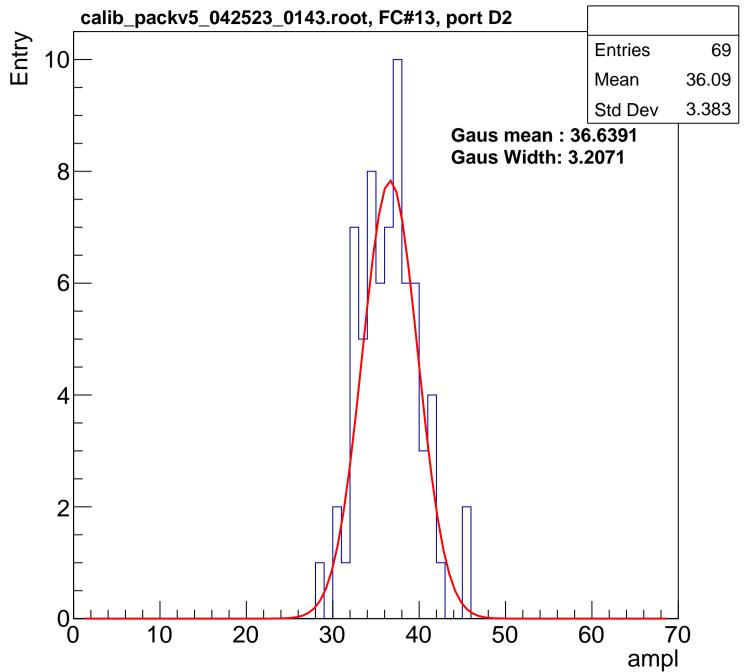


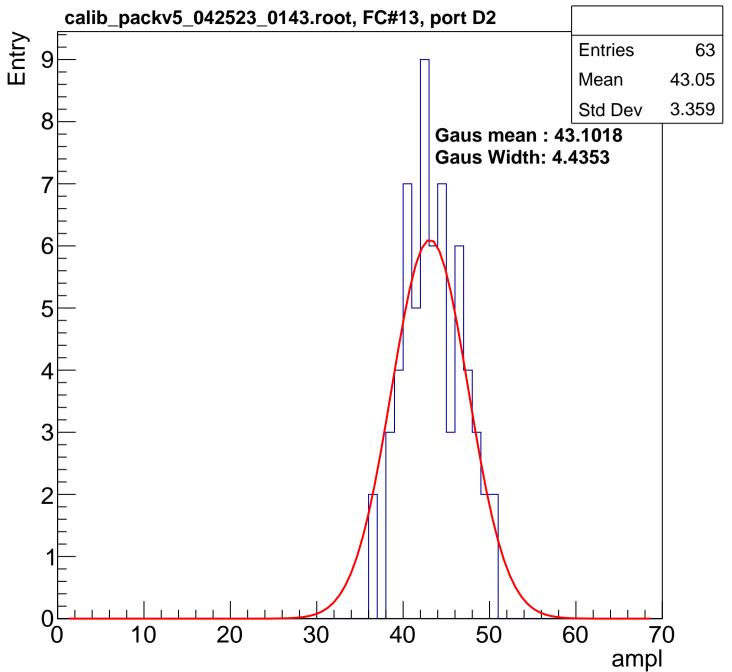


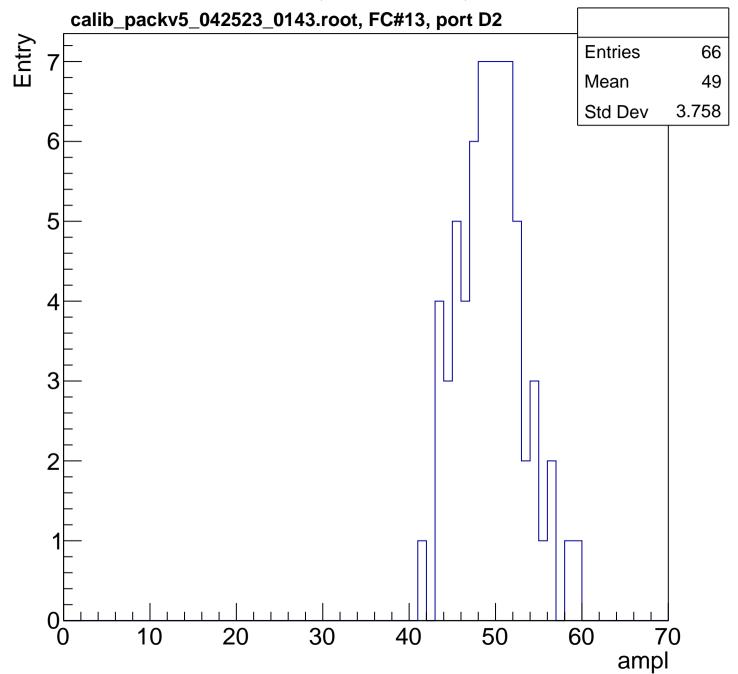


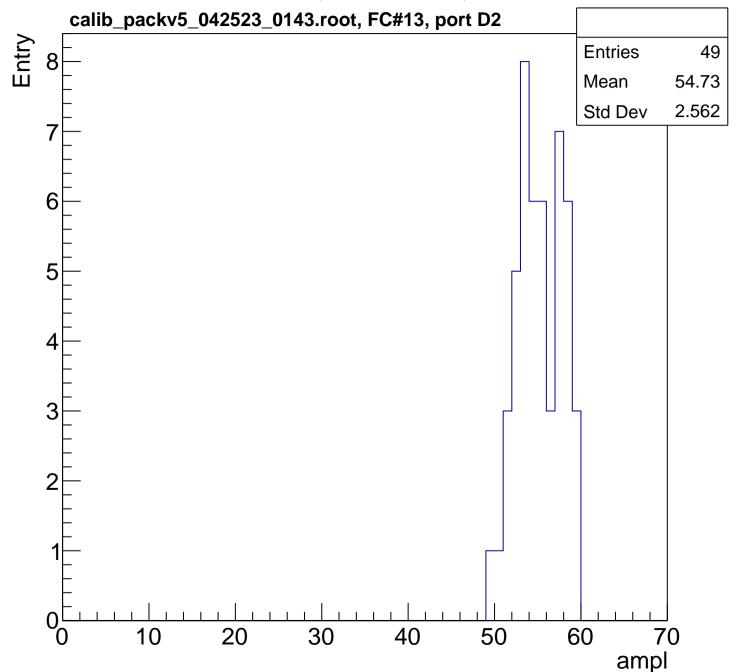
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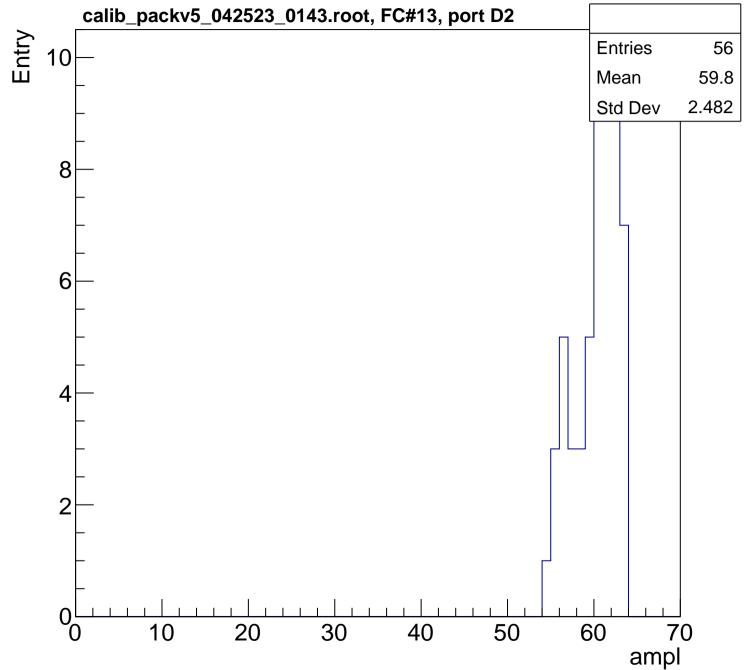


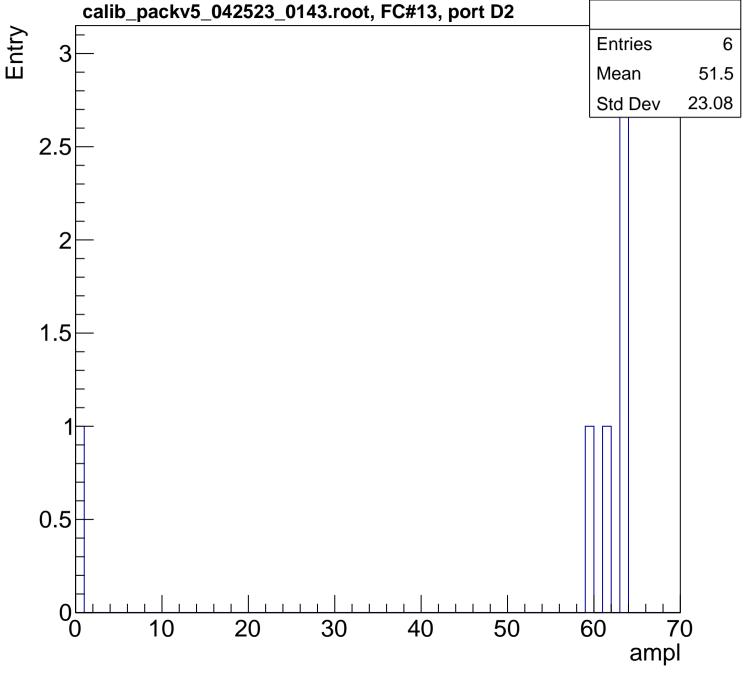




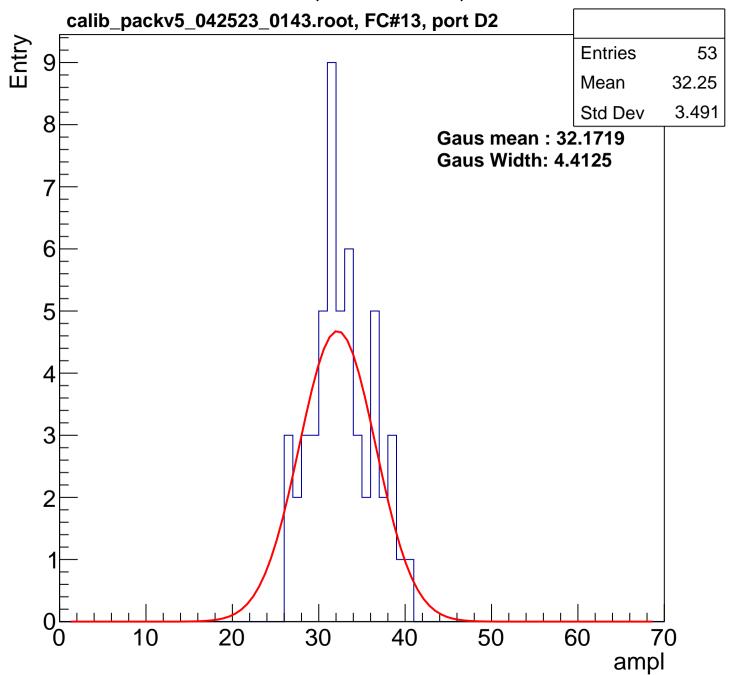


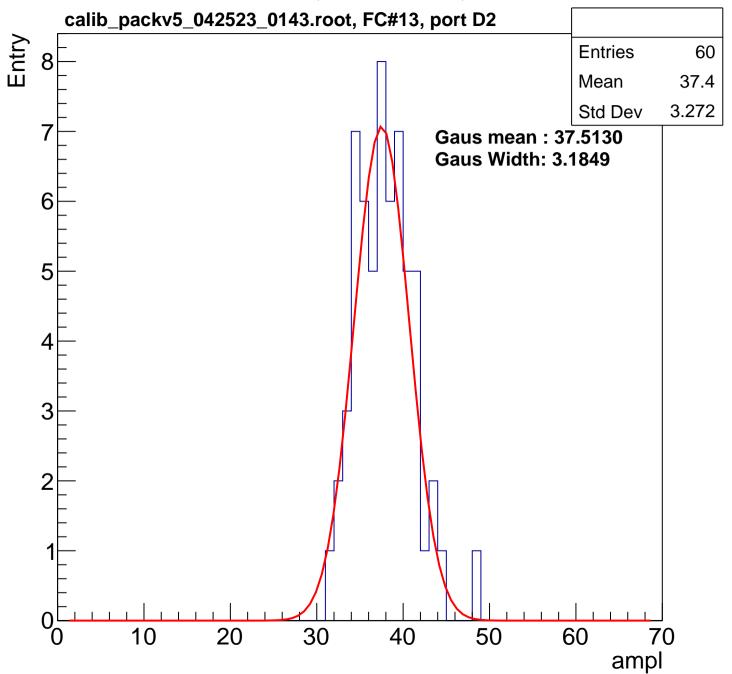


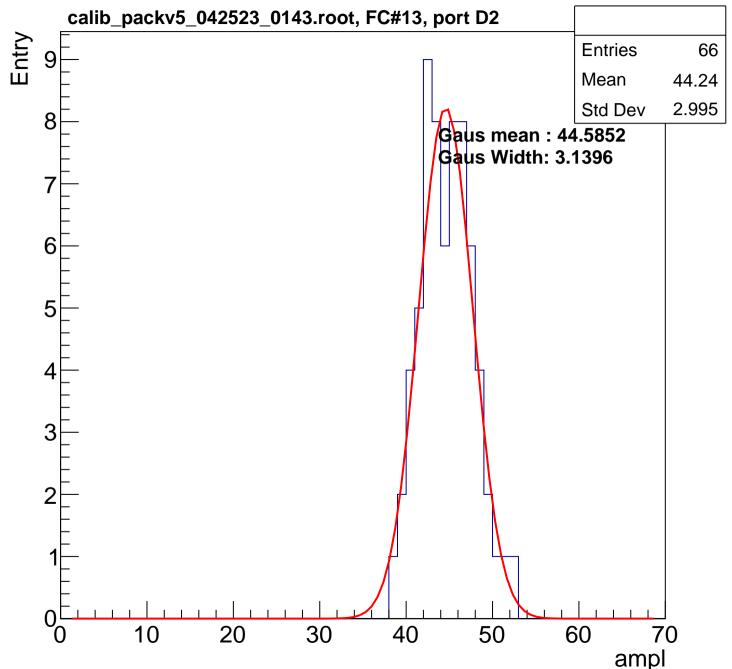


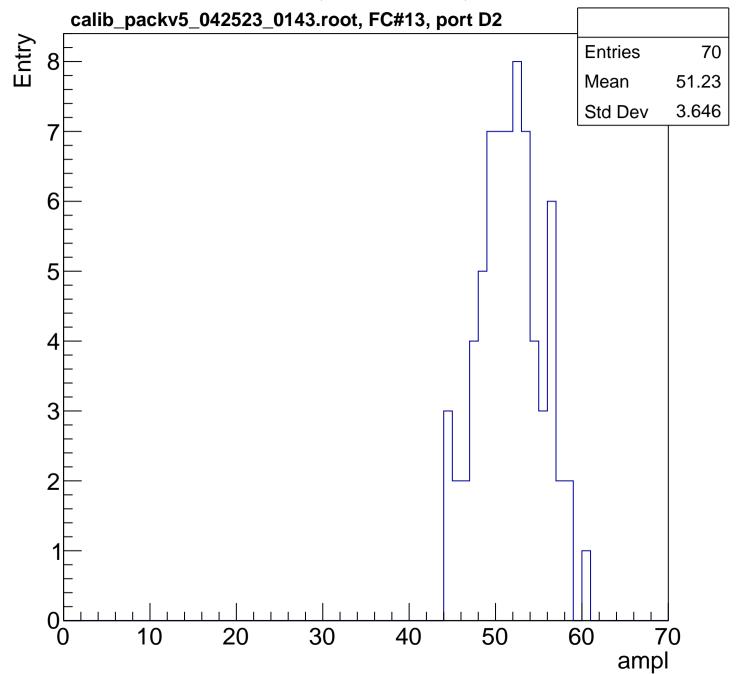


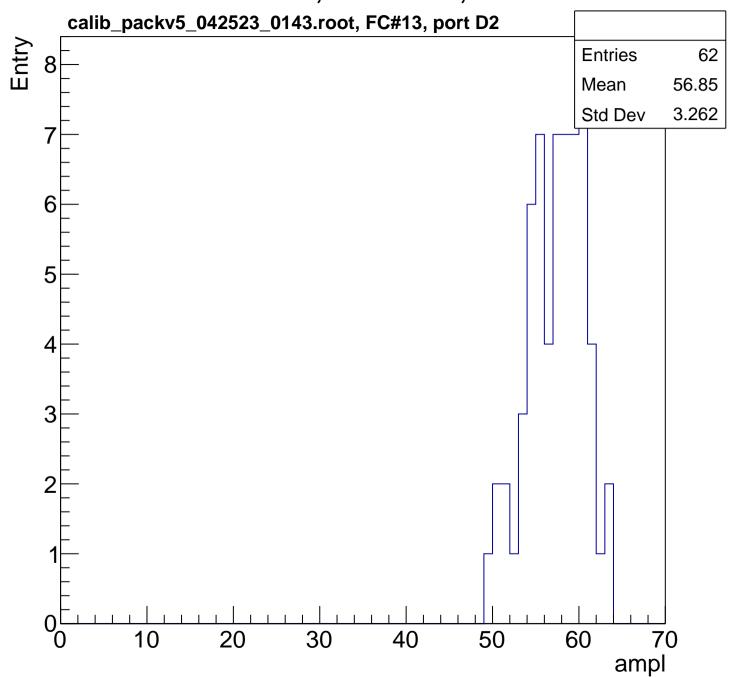
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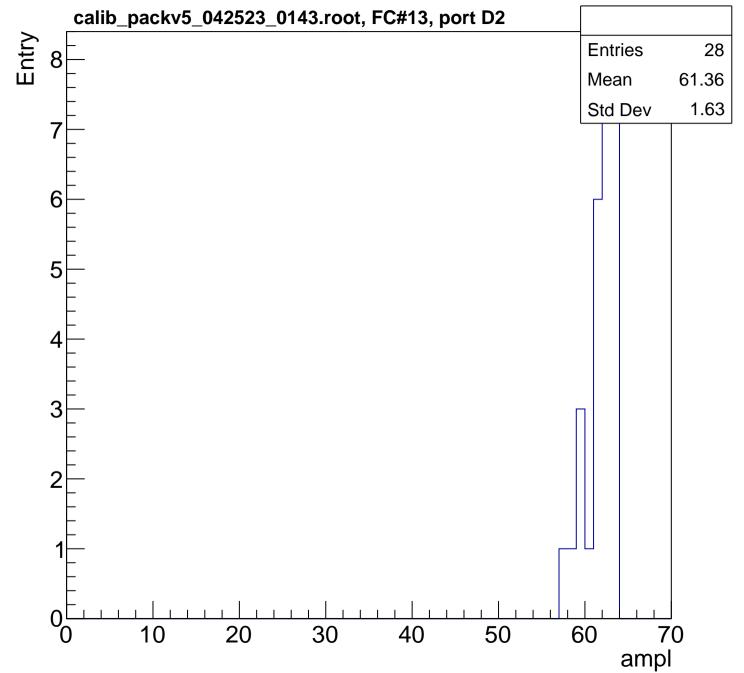


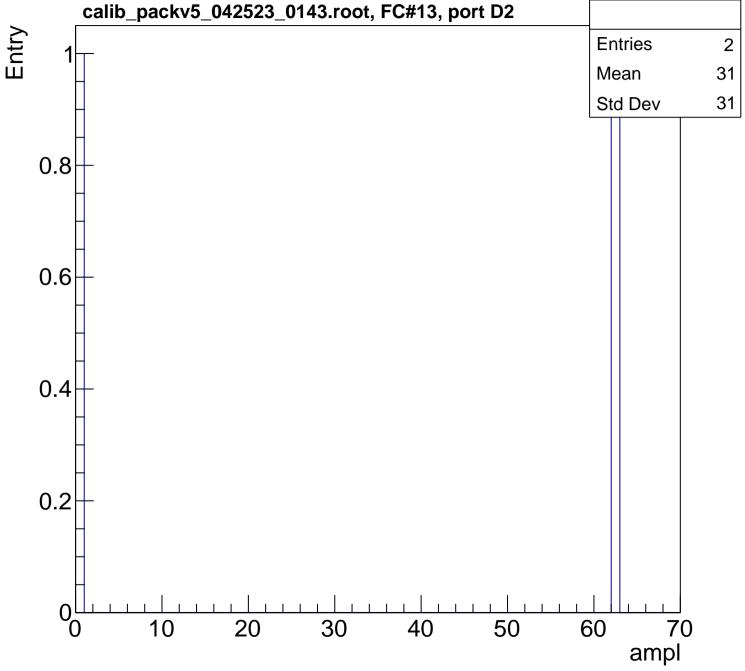


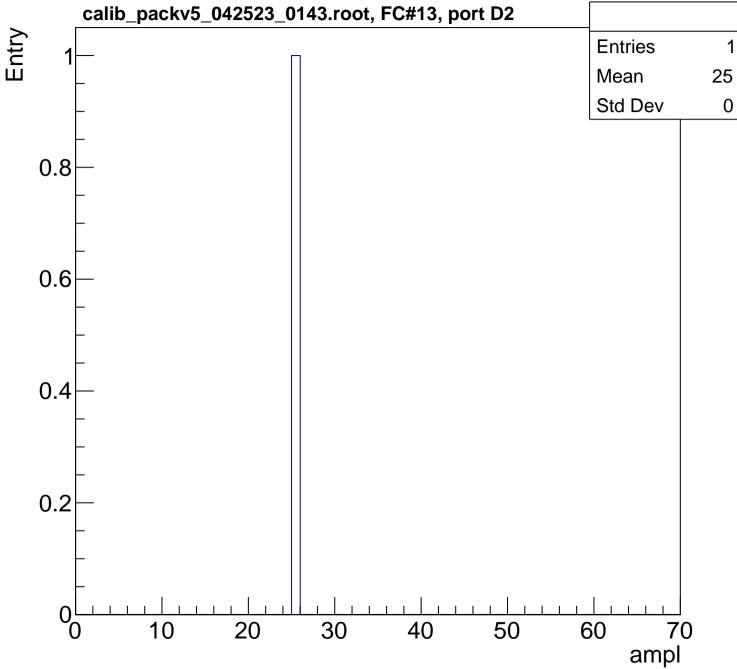


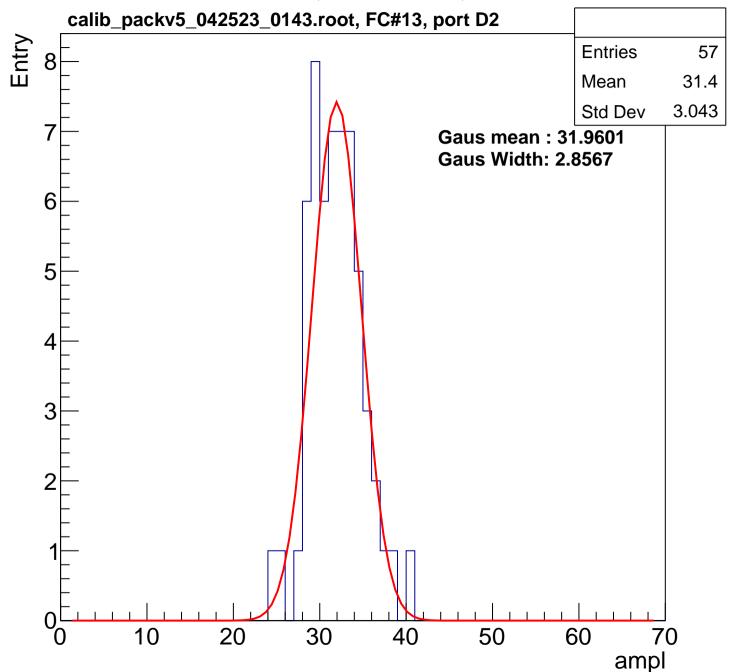


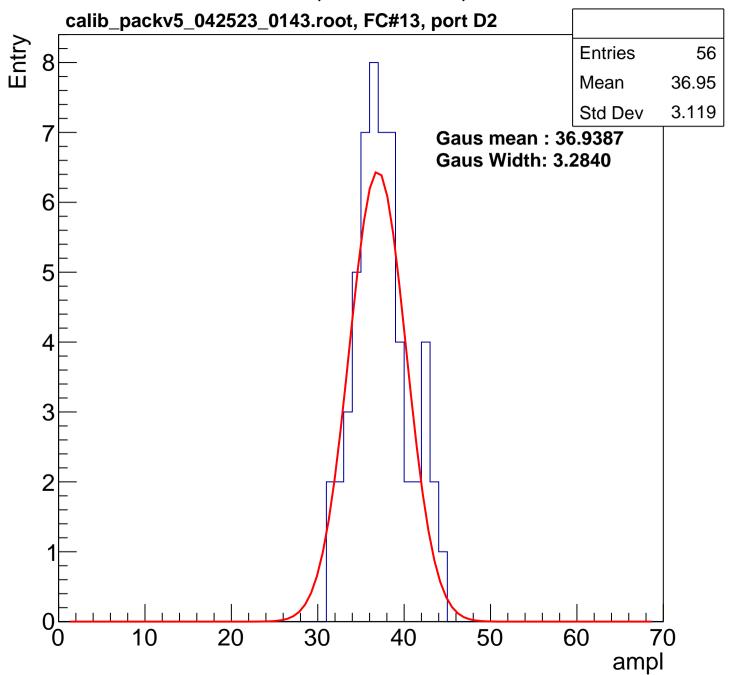


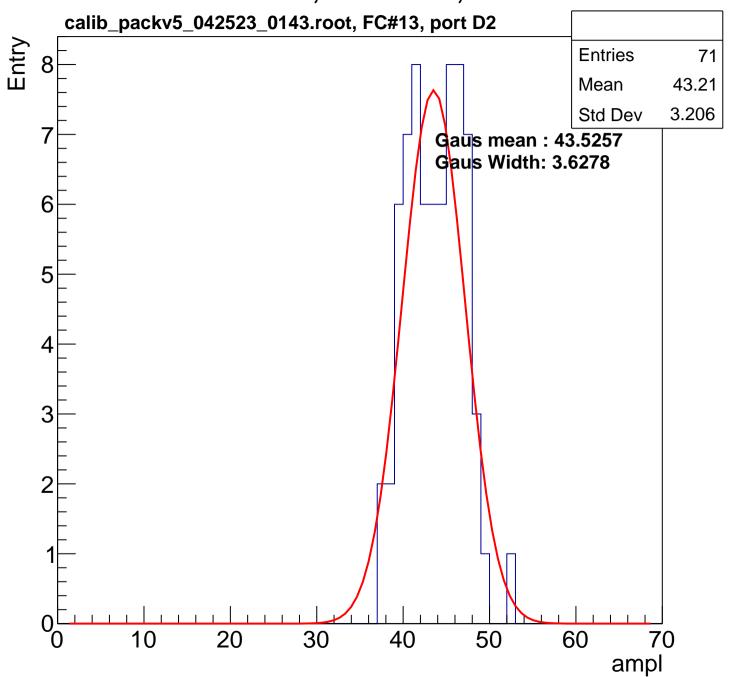


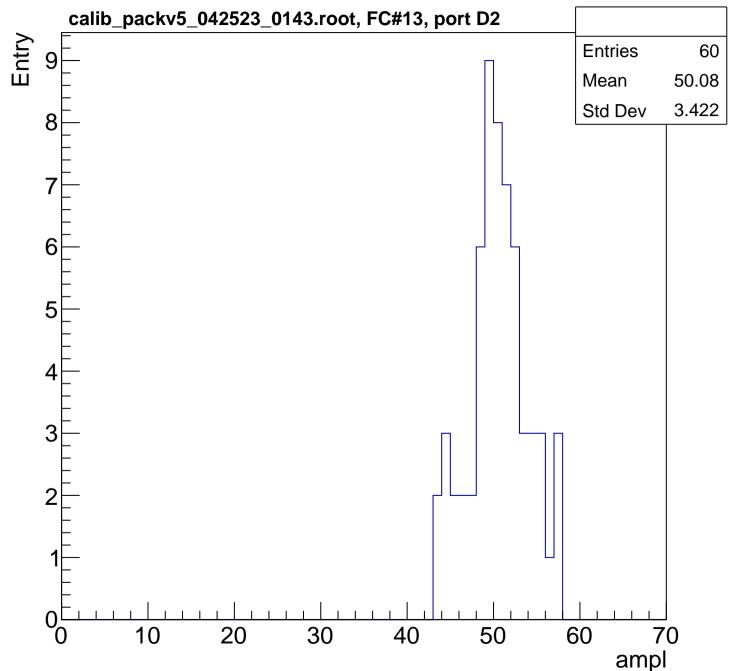


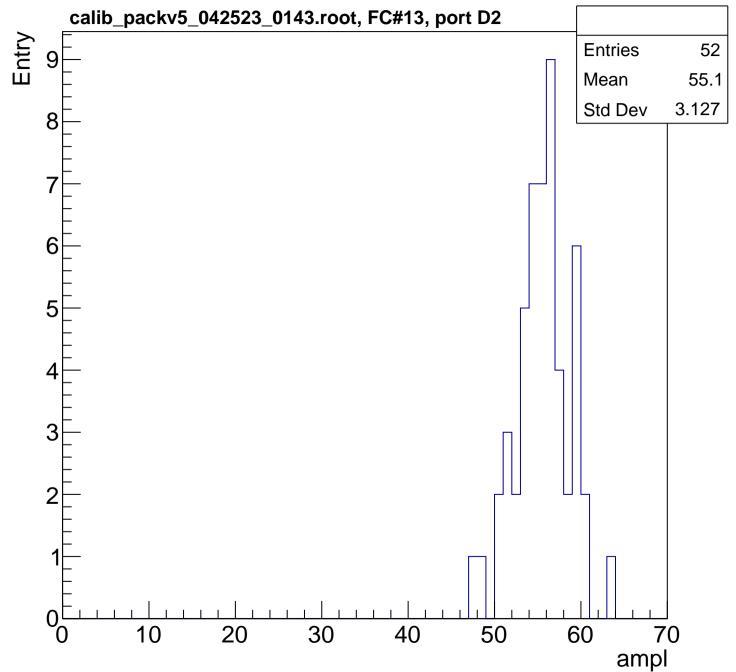


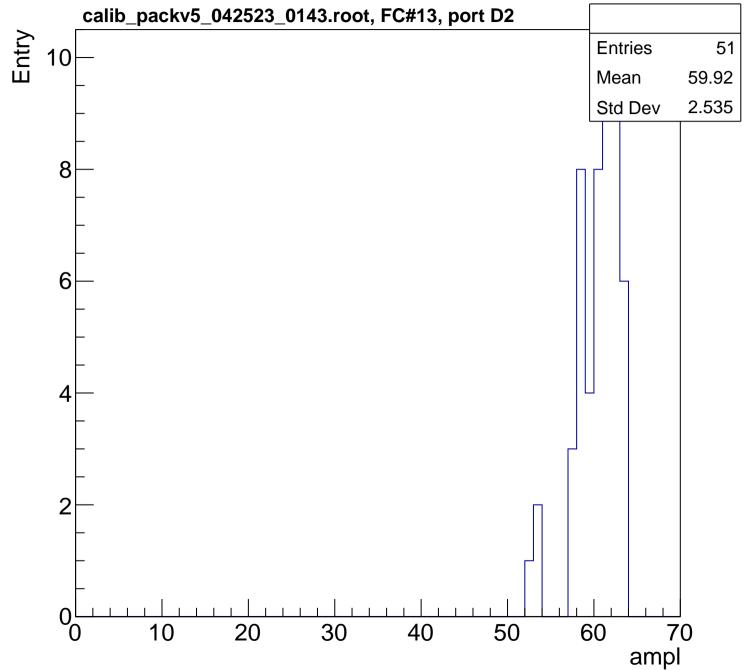


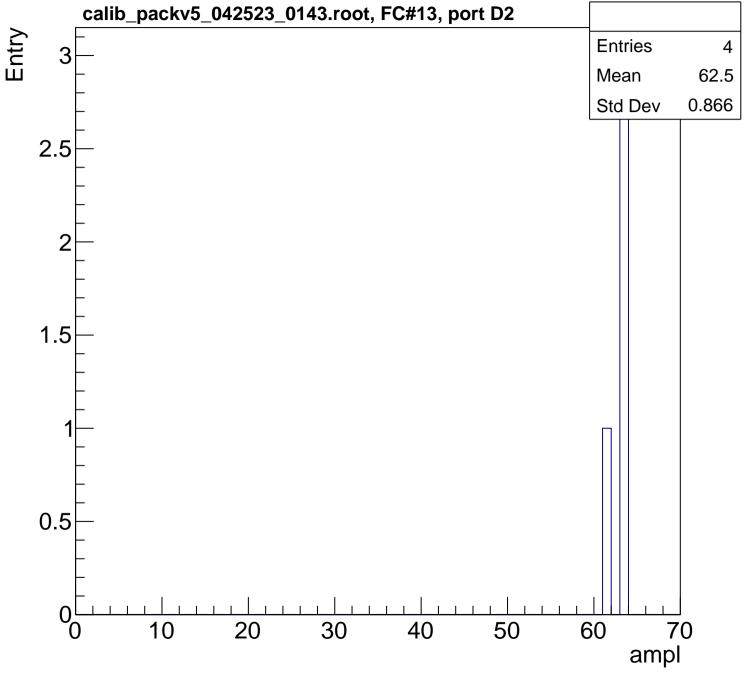


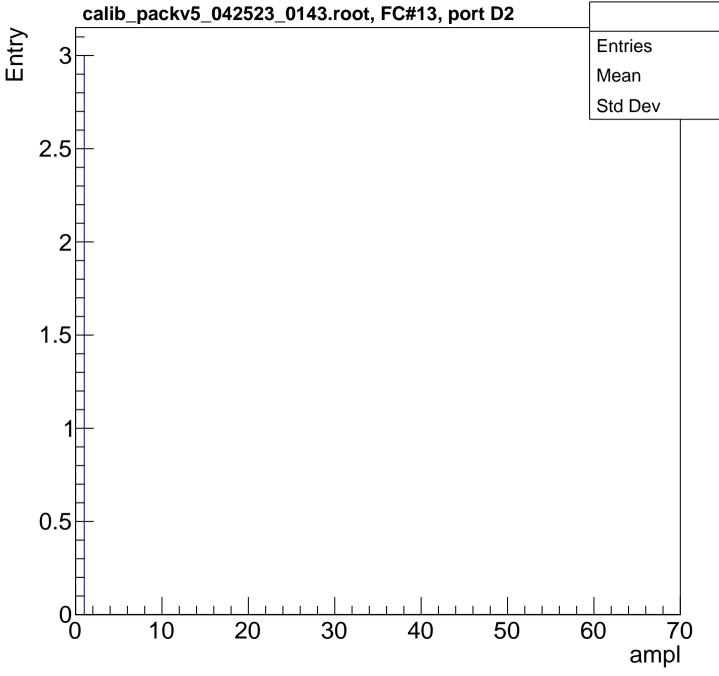


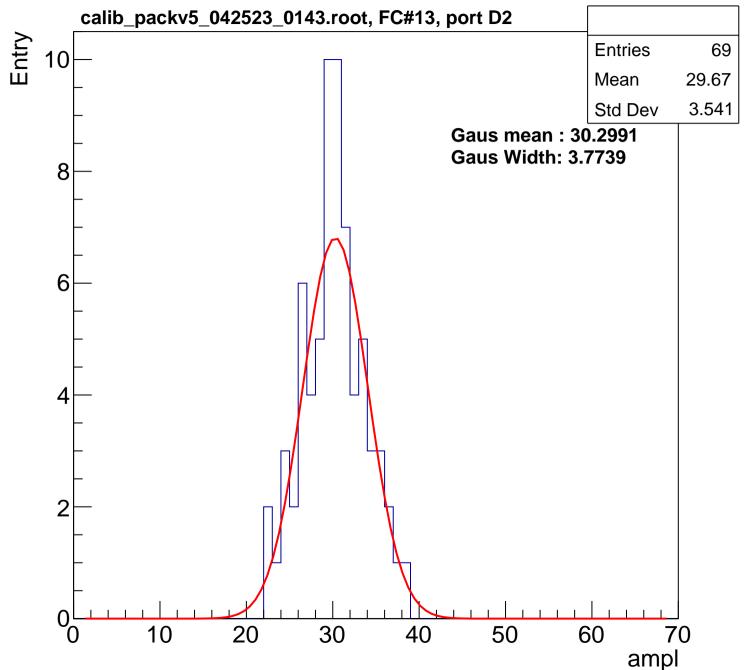


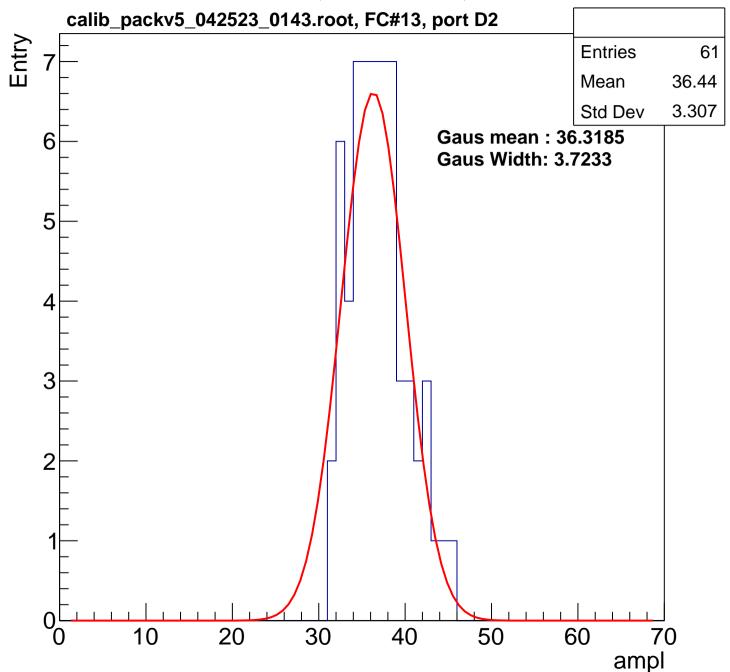


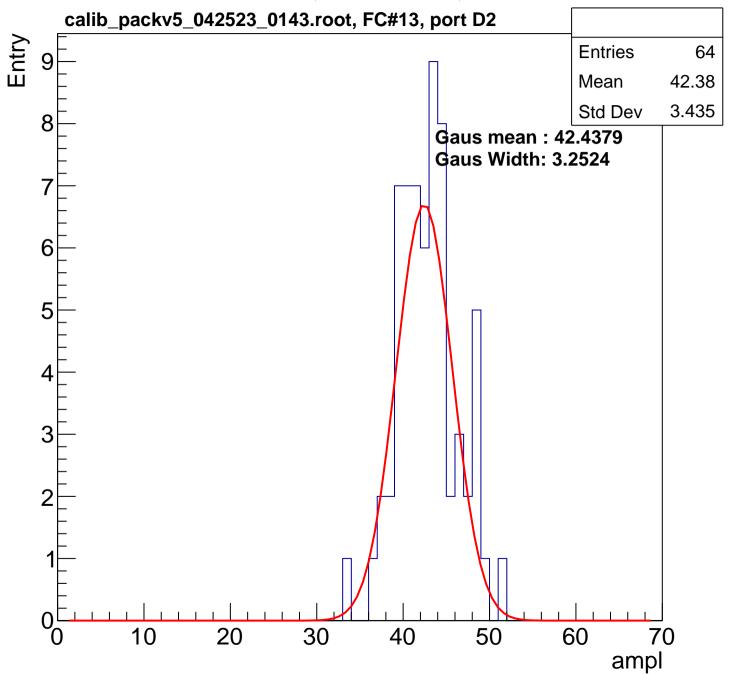


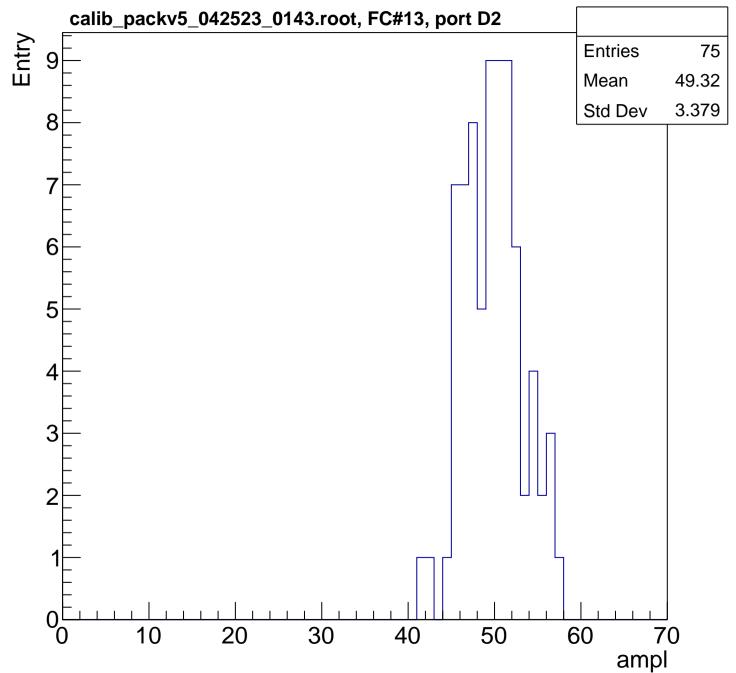


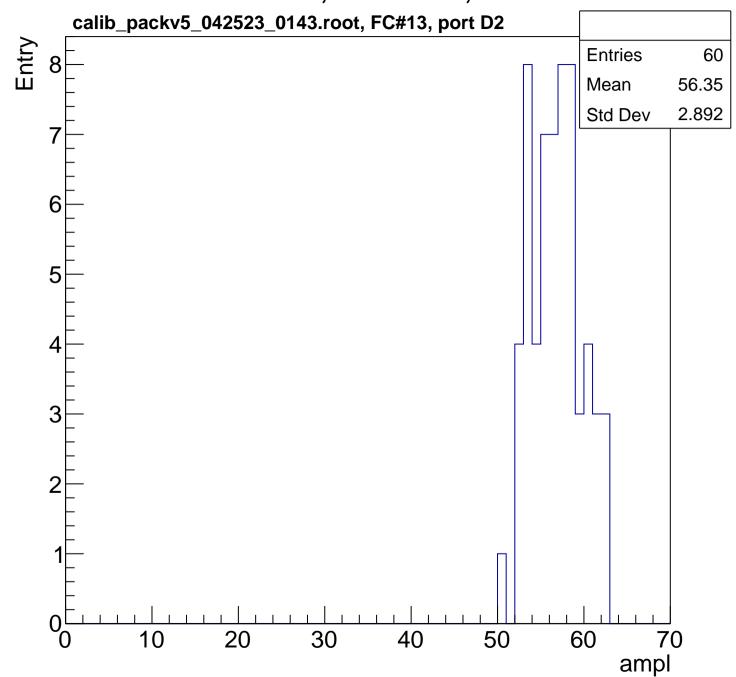


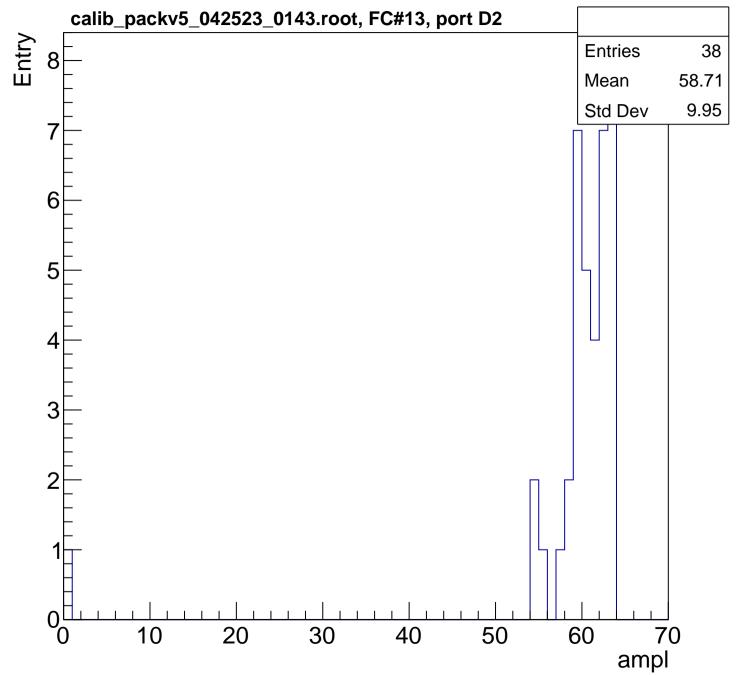


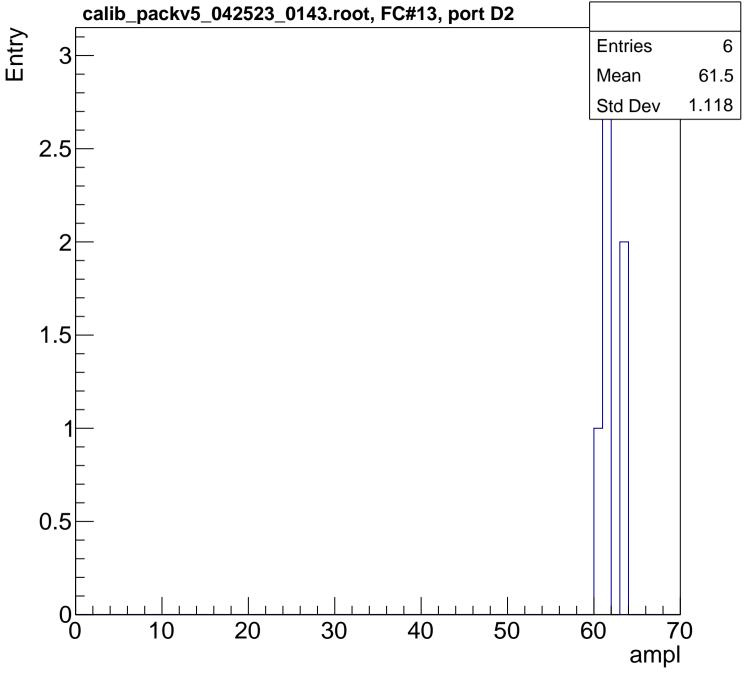




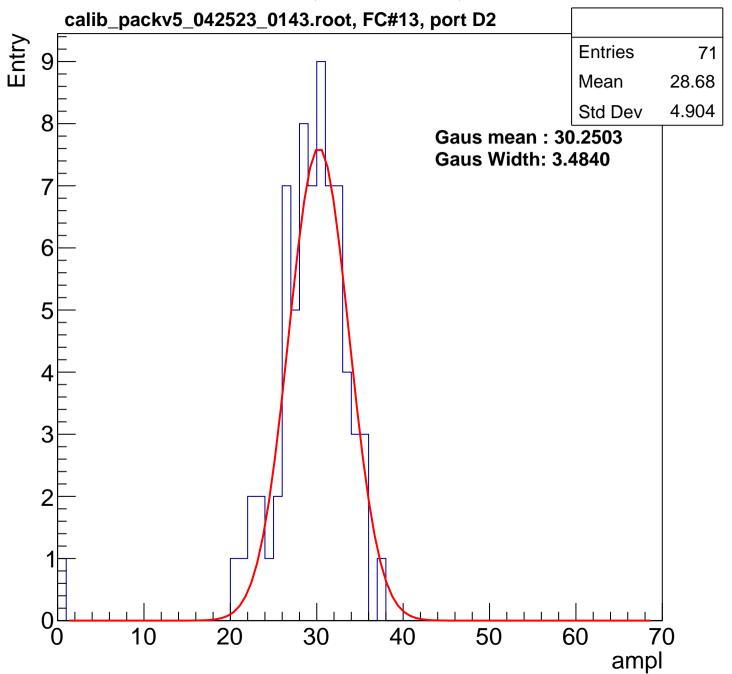


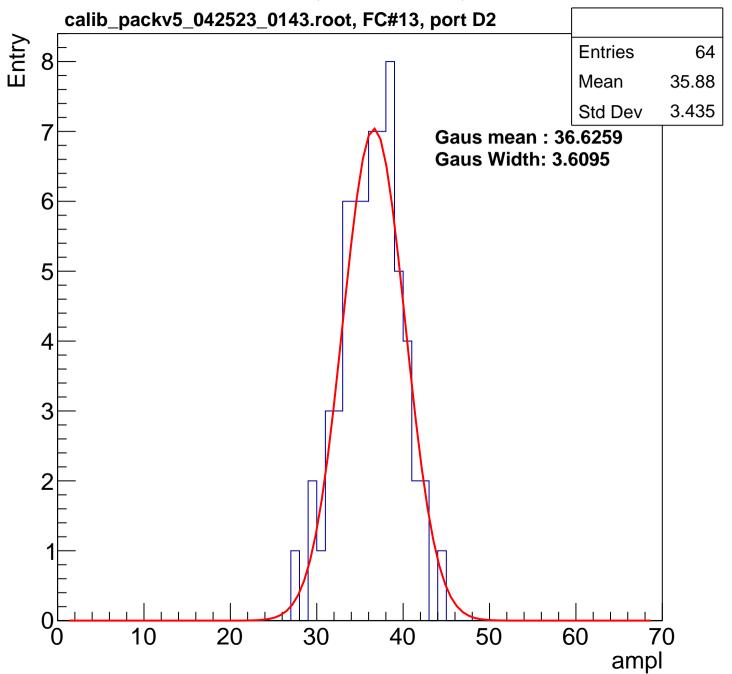


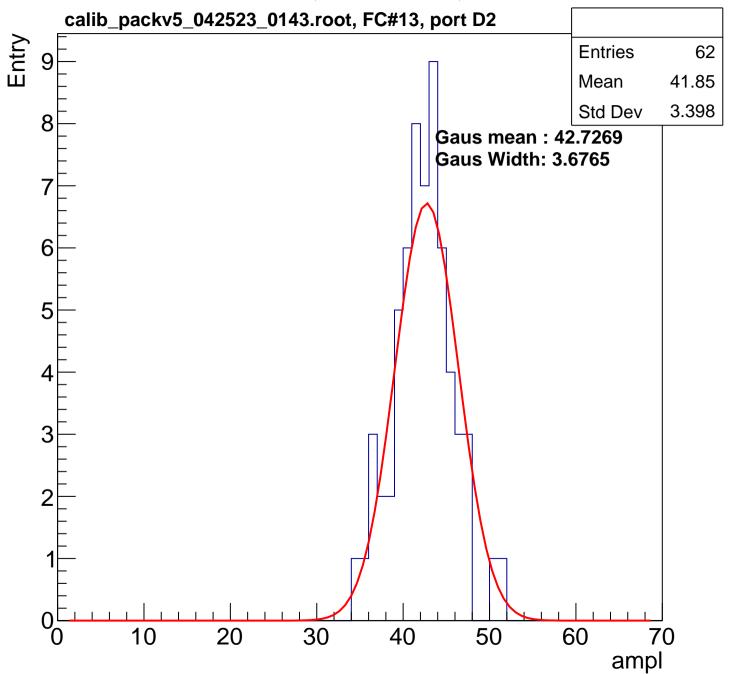


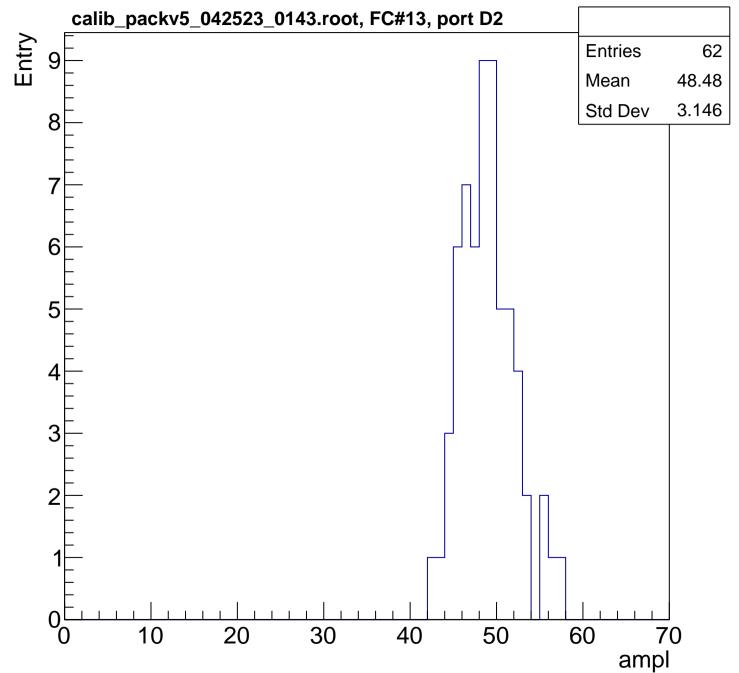


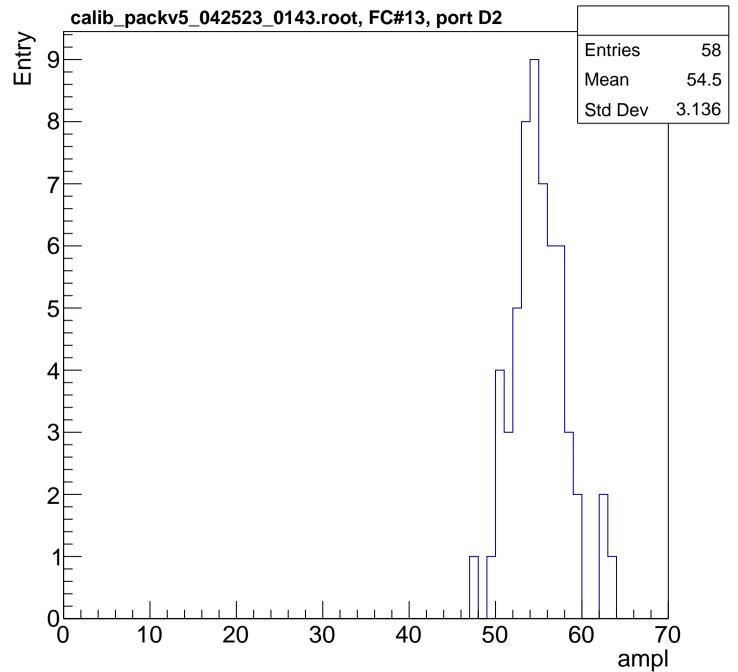
B1L003S, U2-ch71, adc7 calib_packv5_042523_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

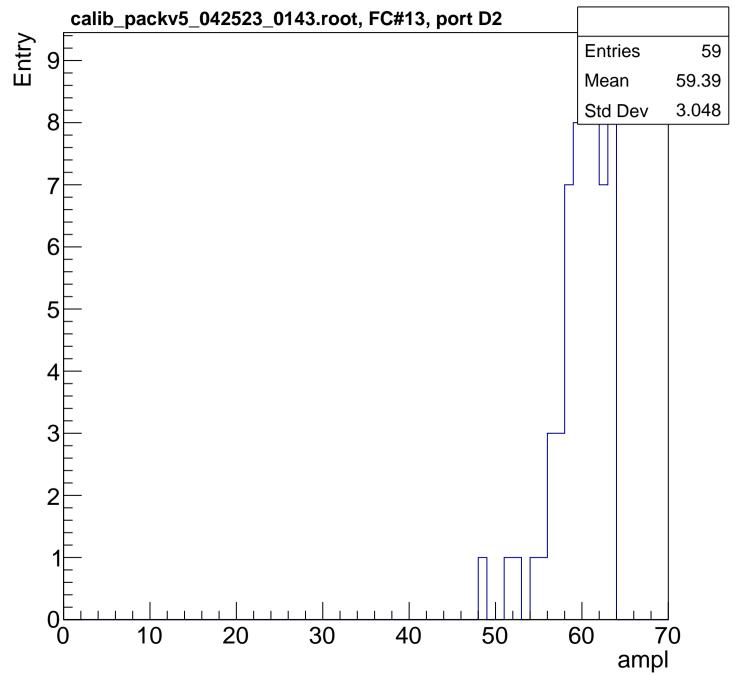


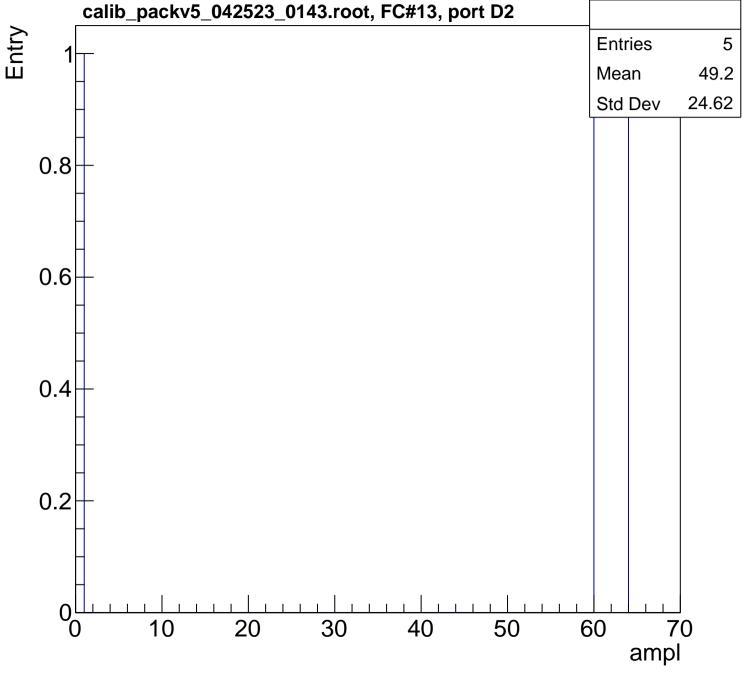


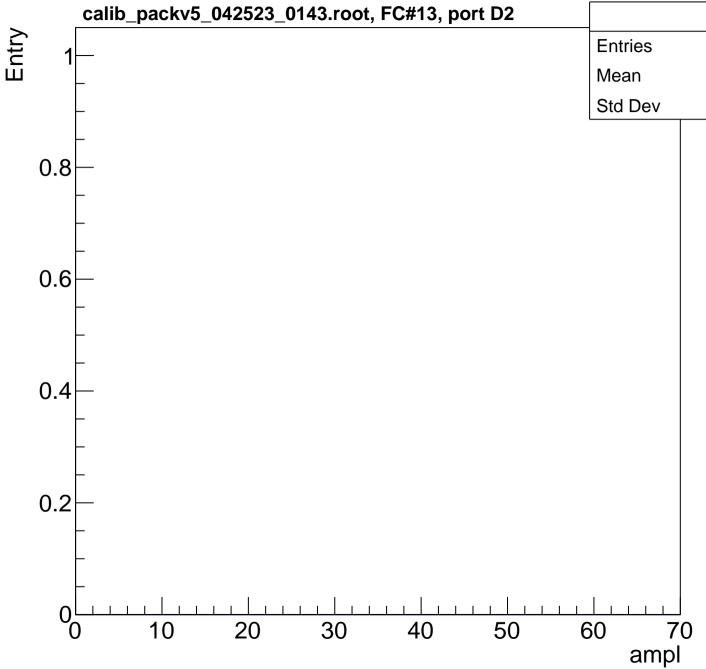


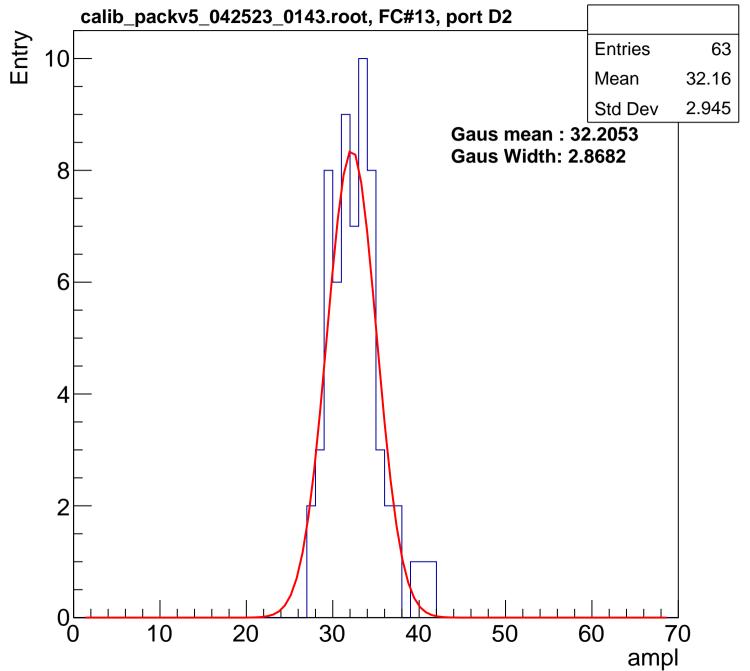


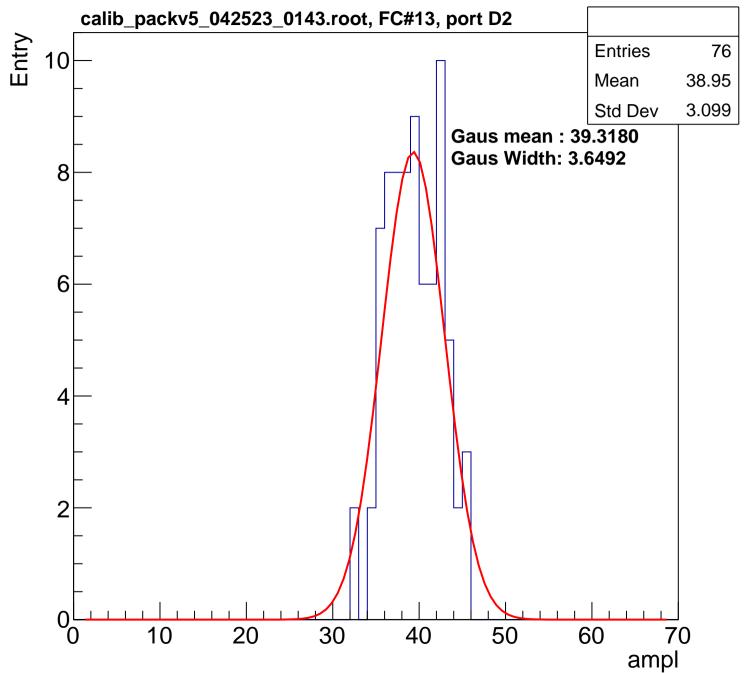


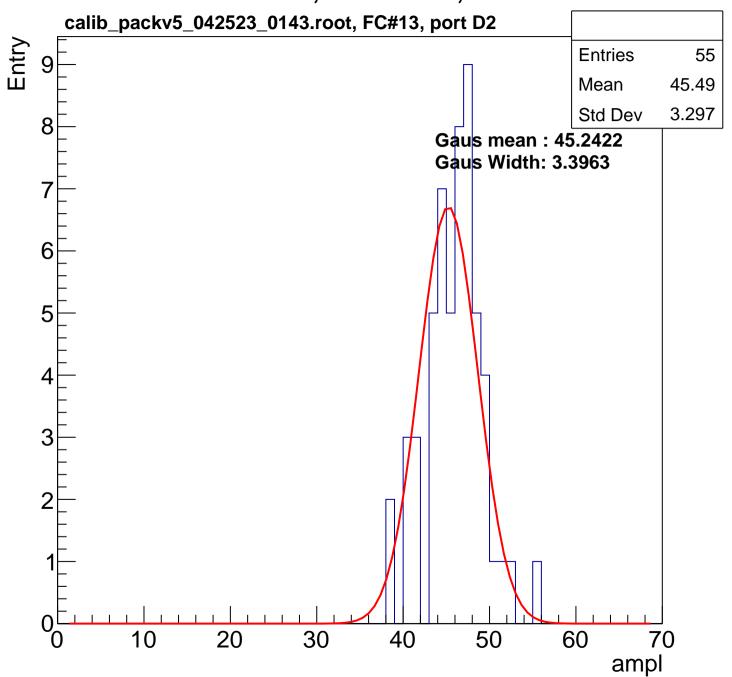


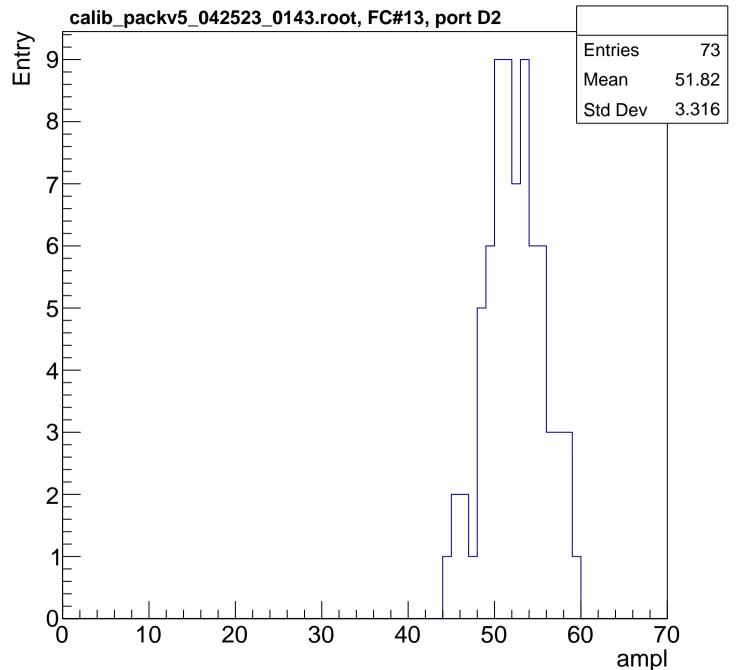


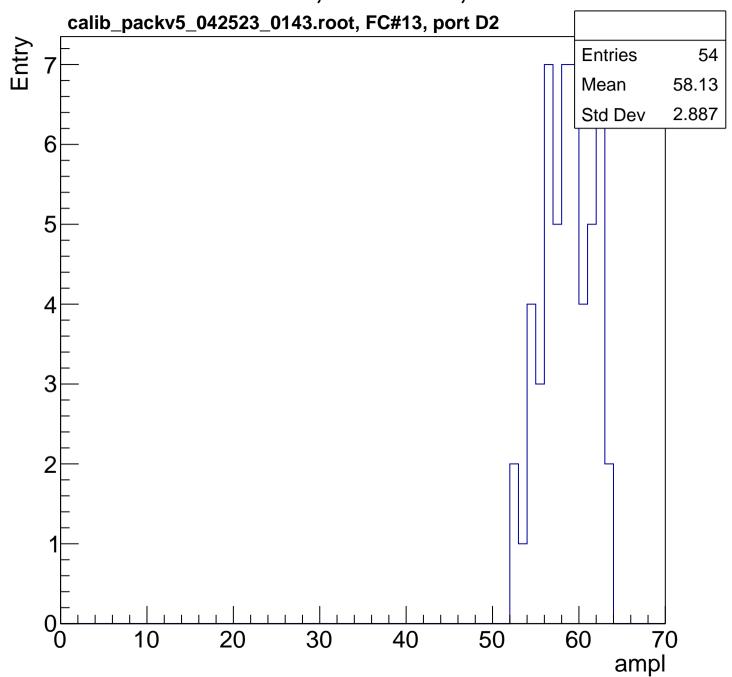


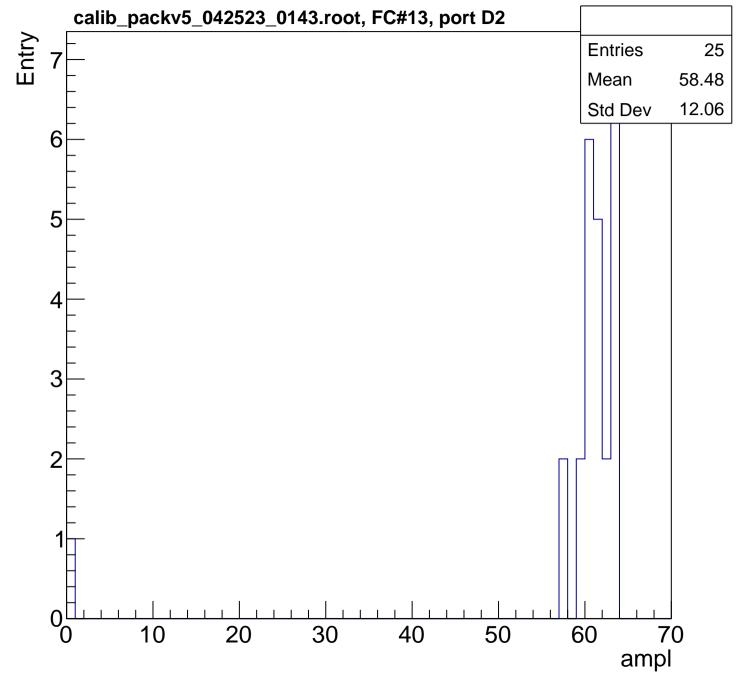


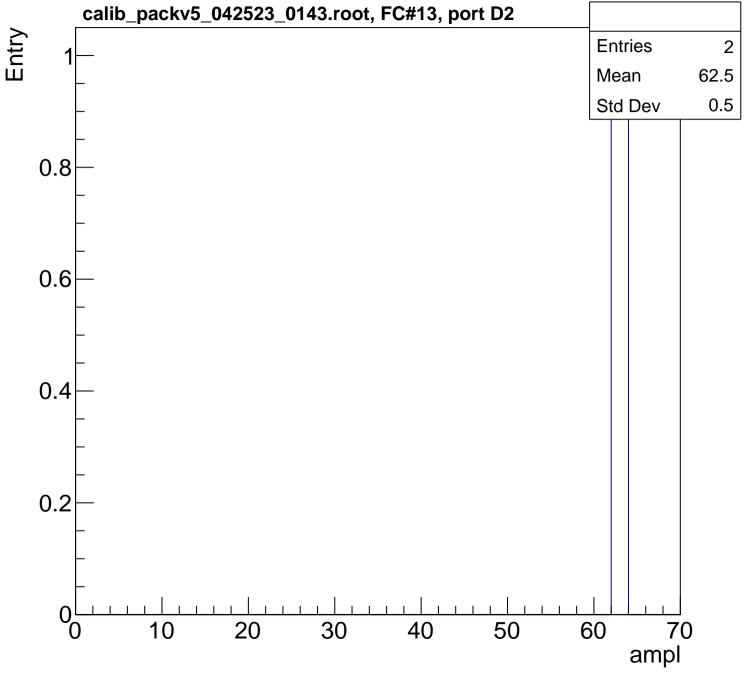


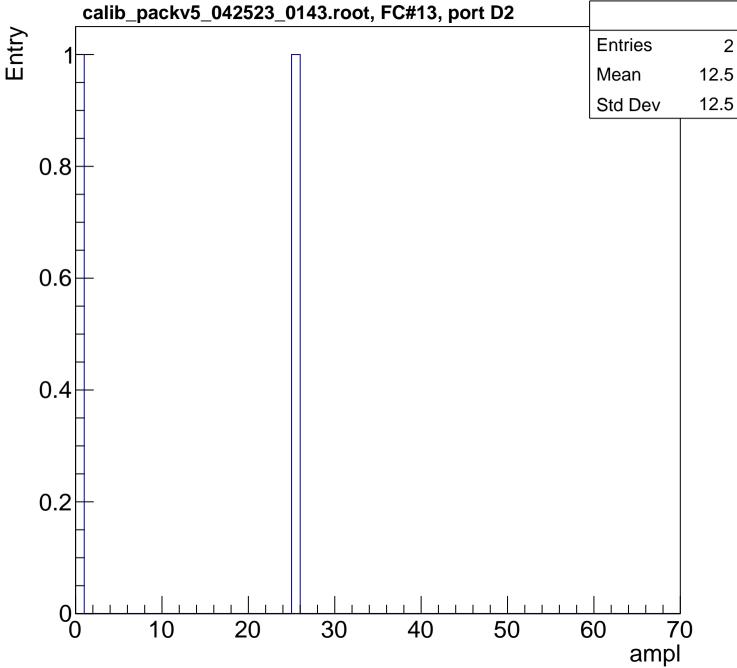


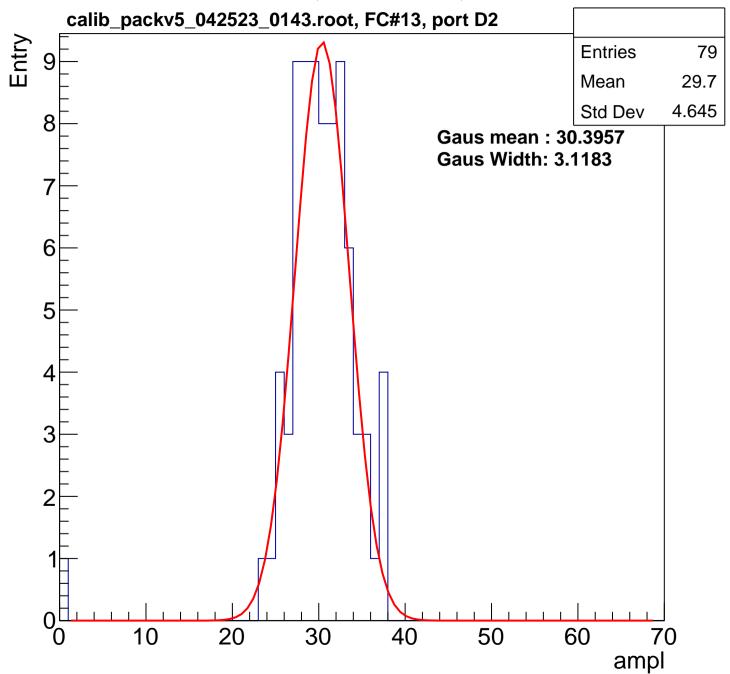


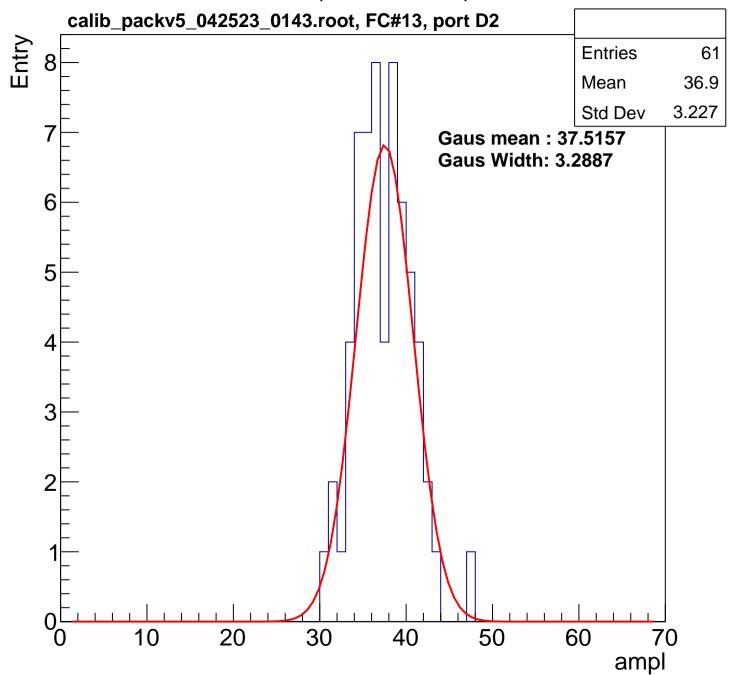


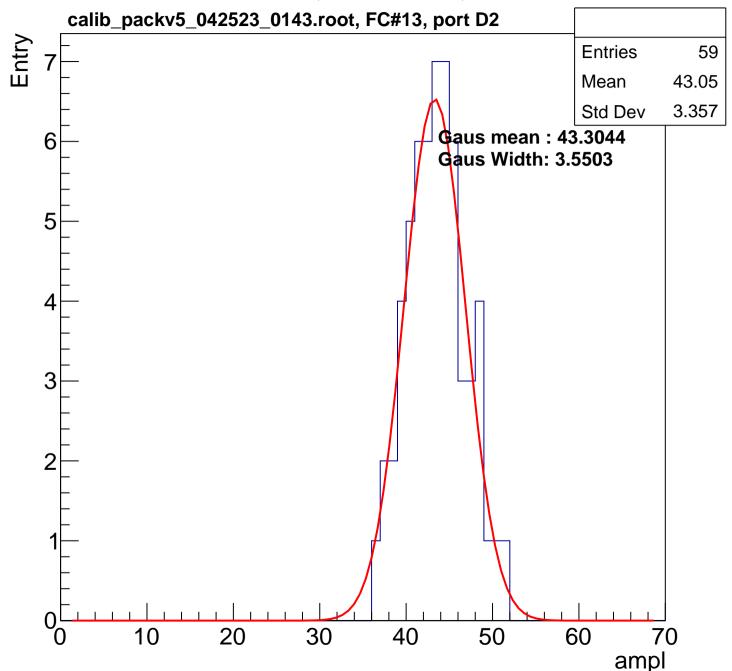


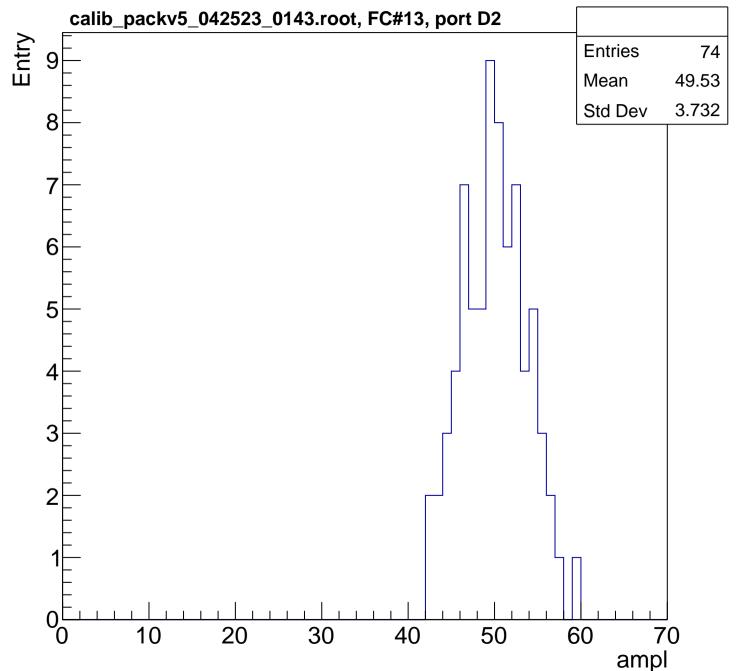


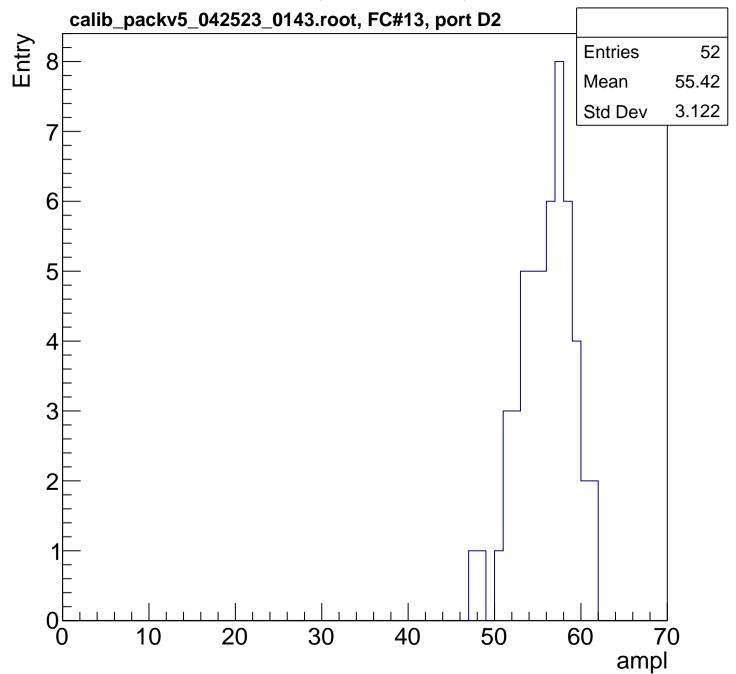


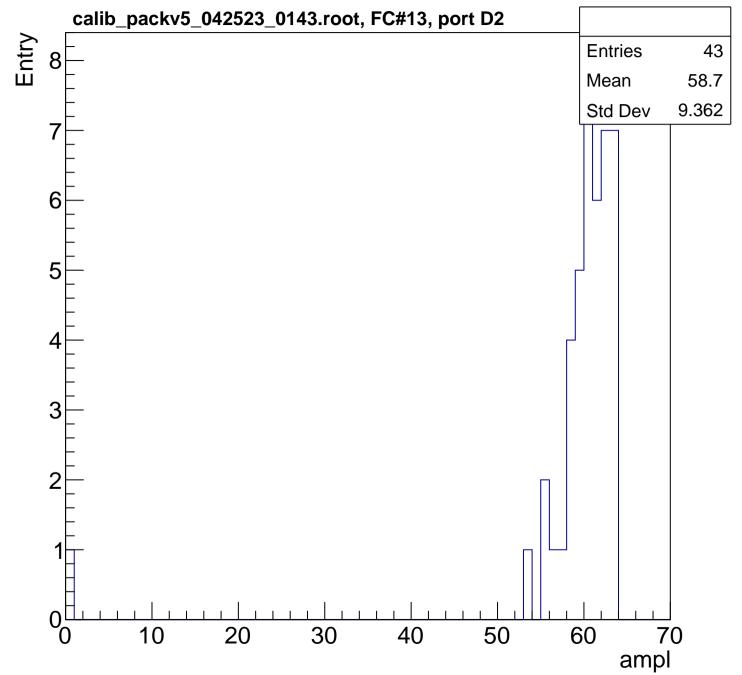


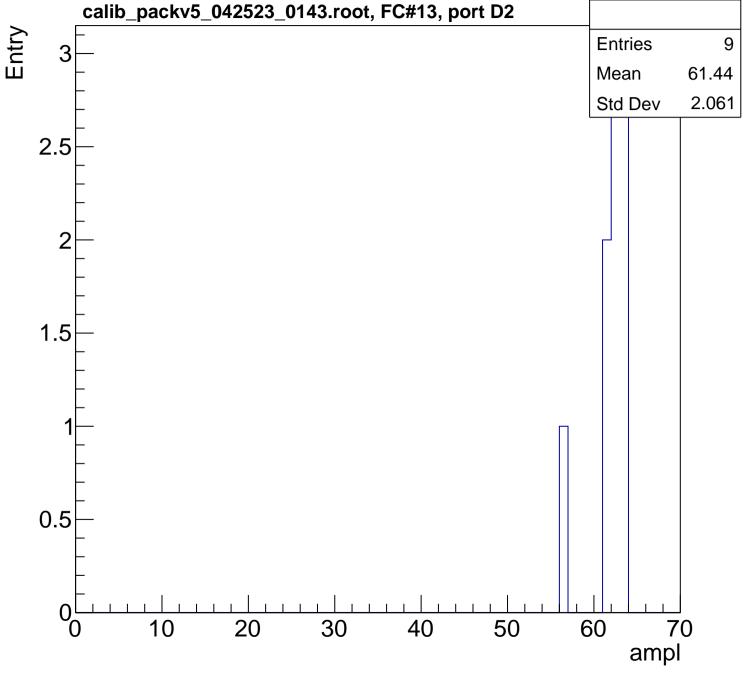


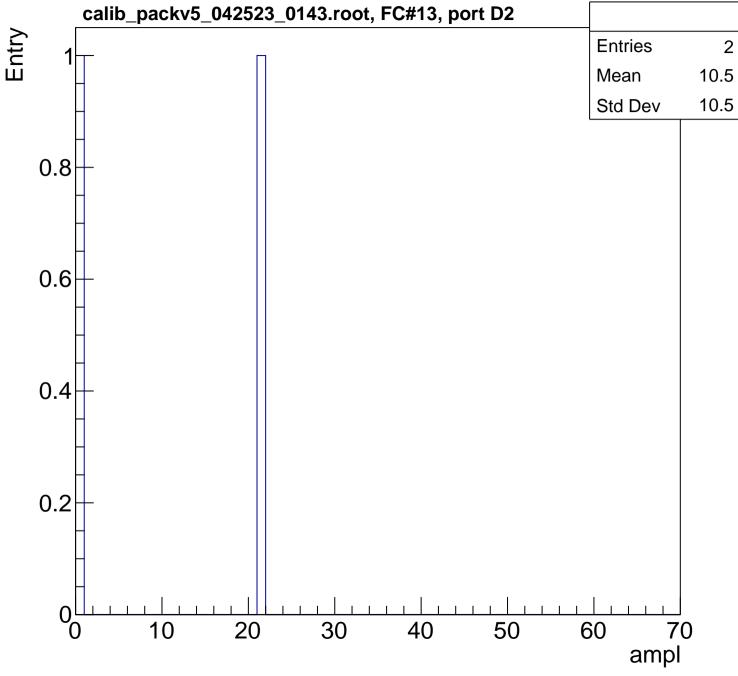


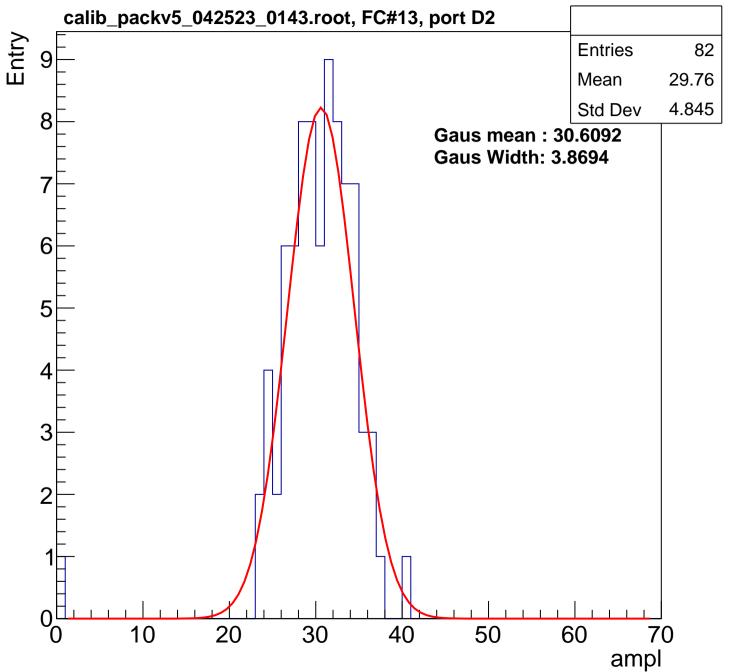


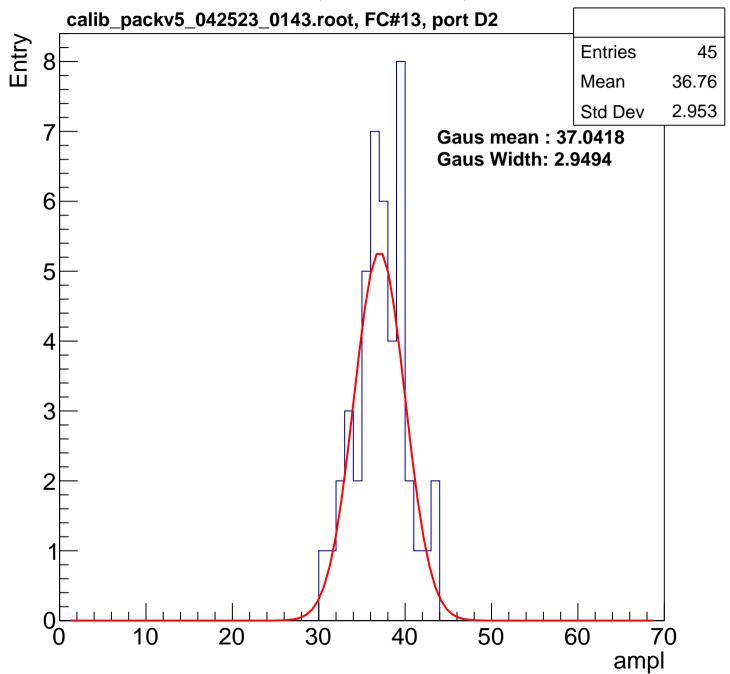


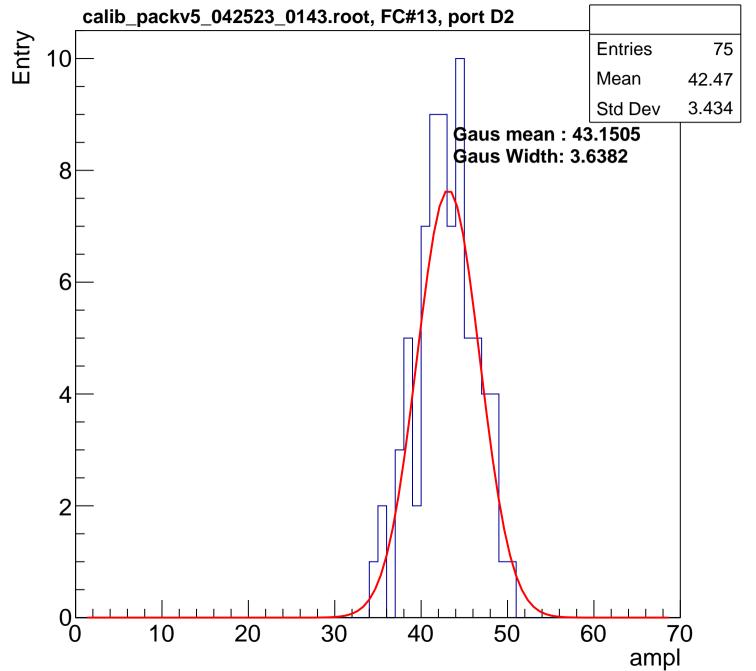


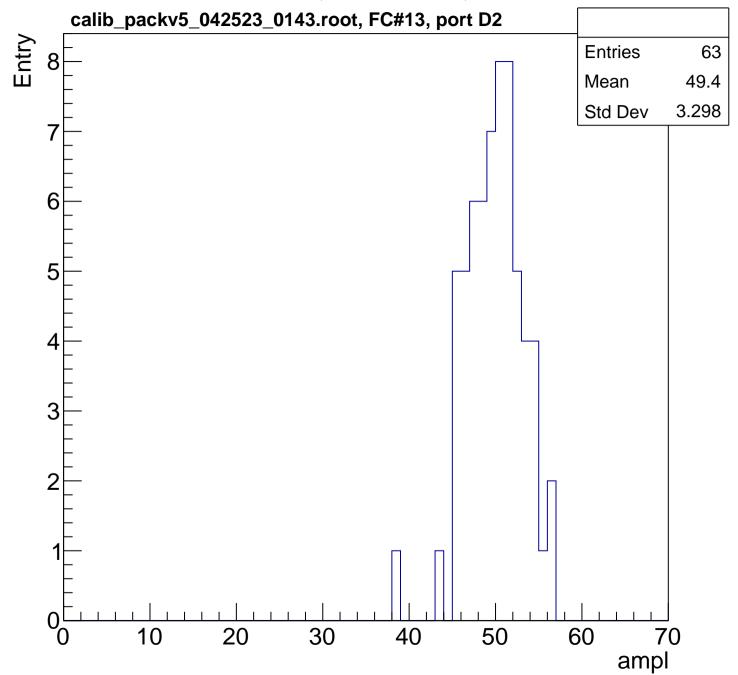


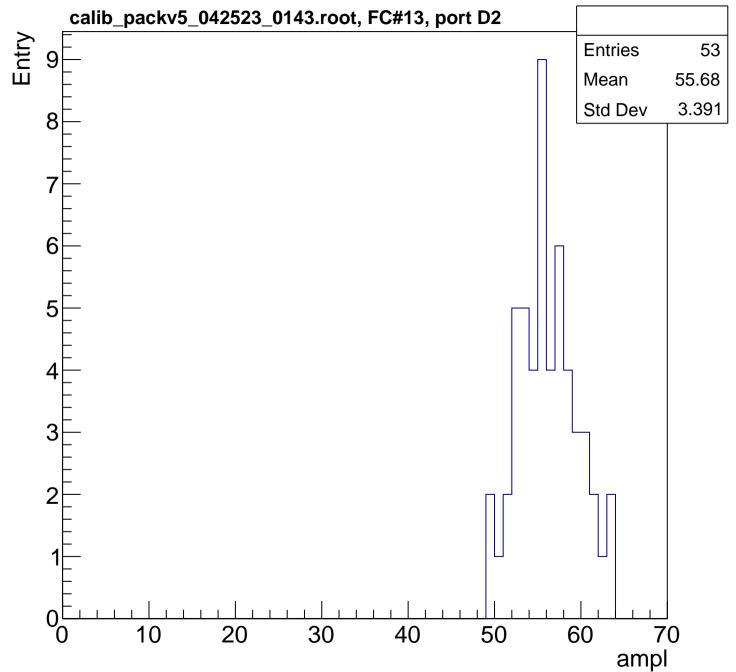


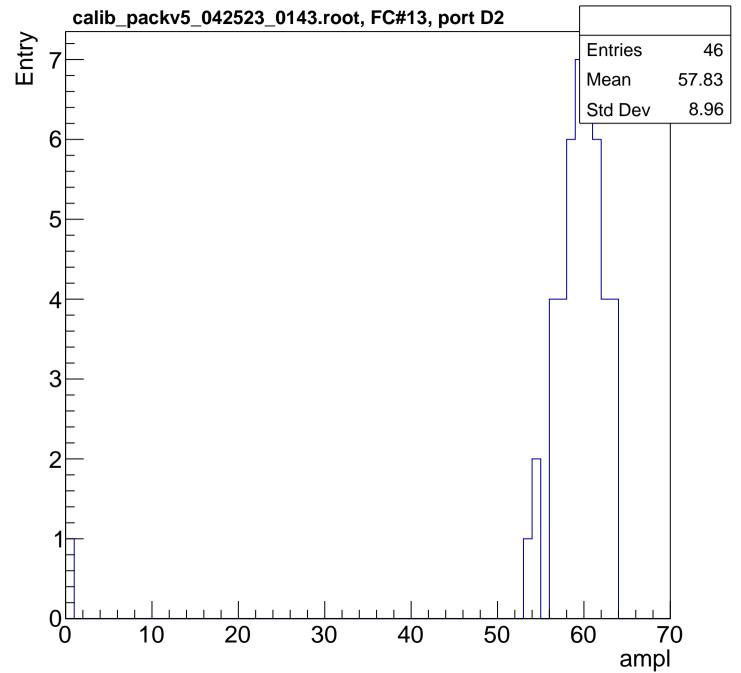


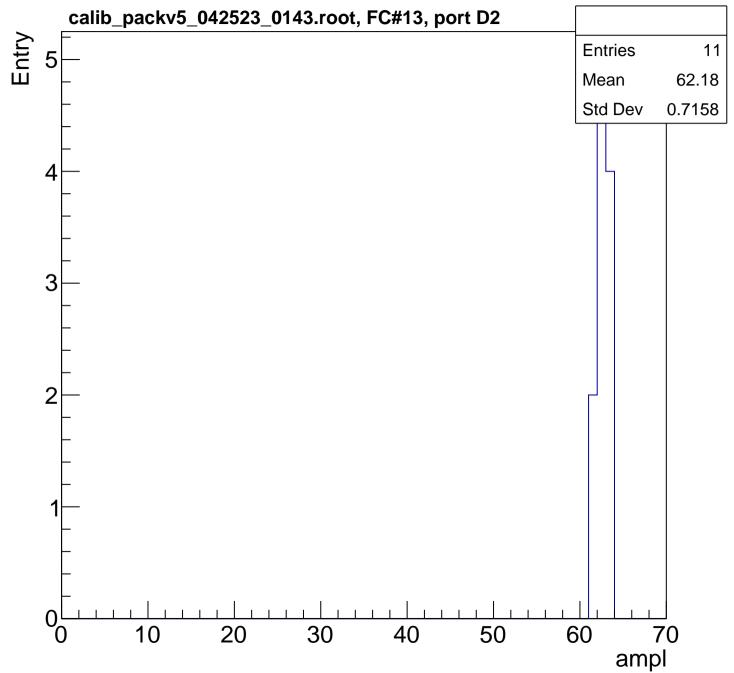




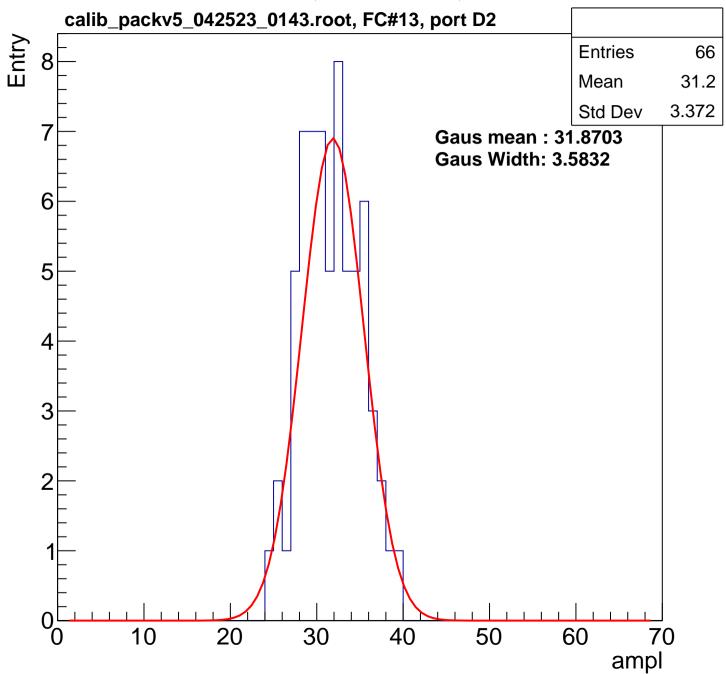


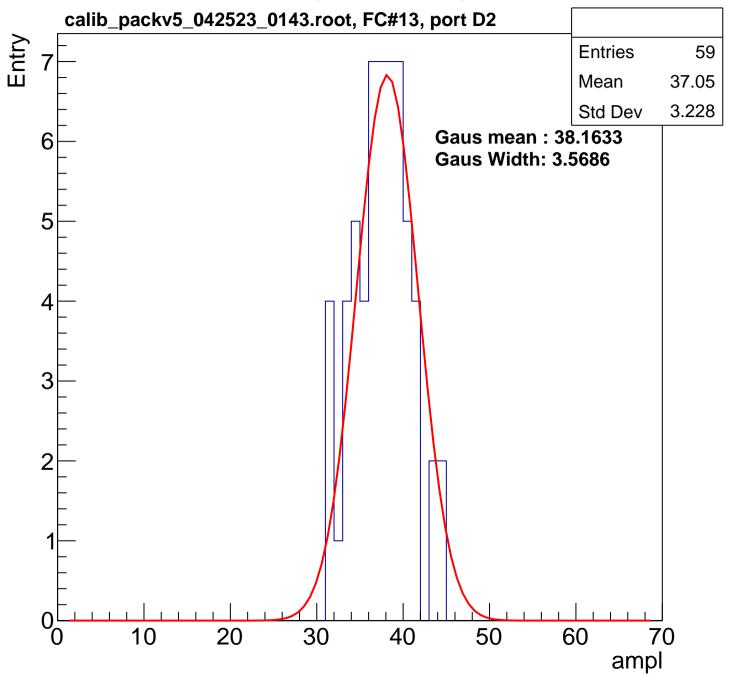


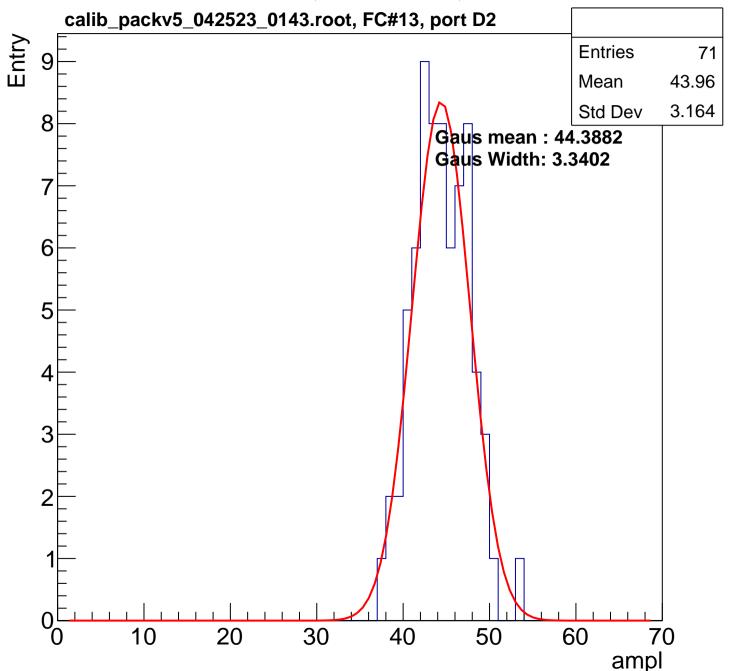


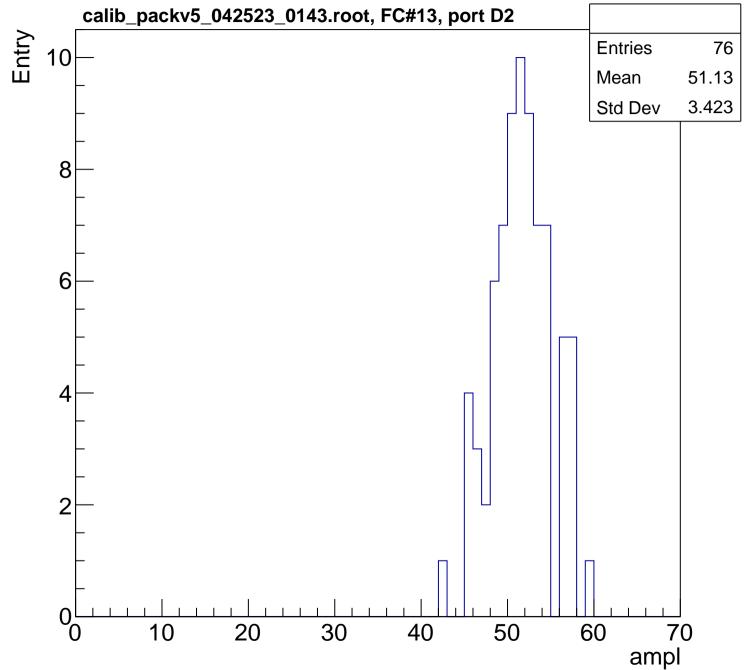


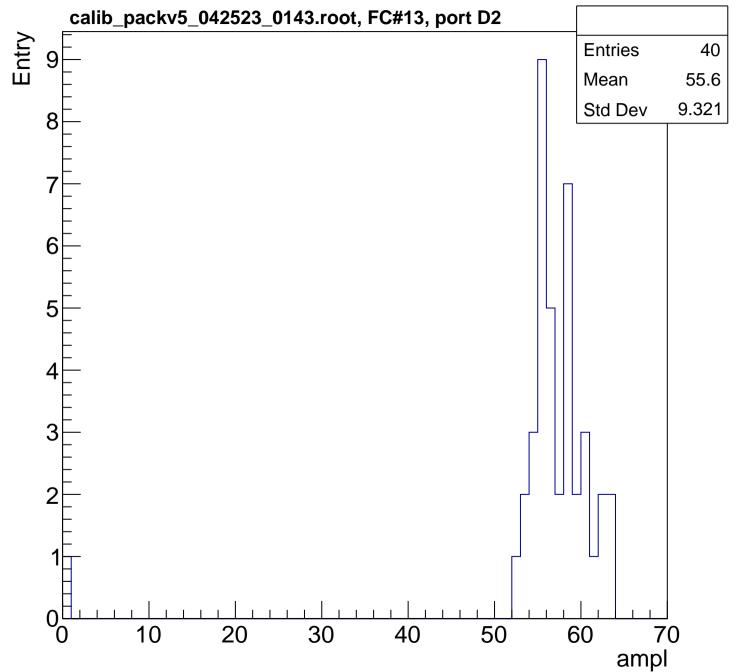


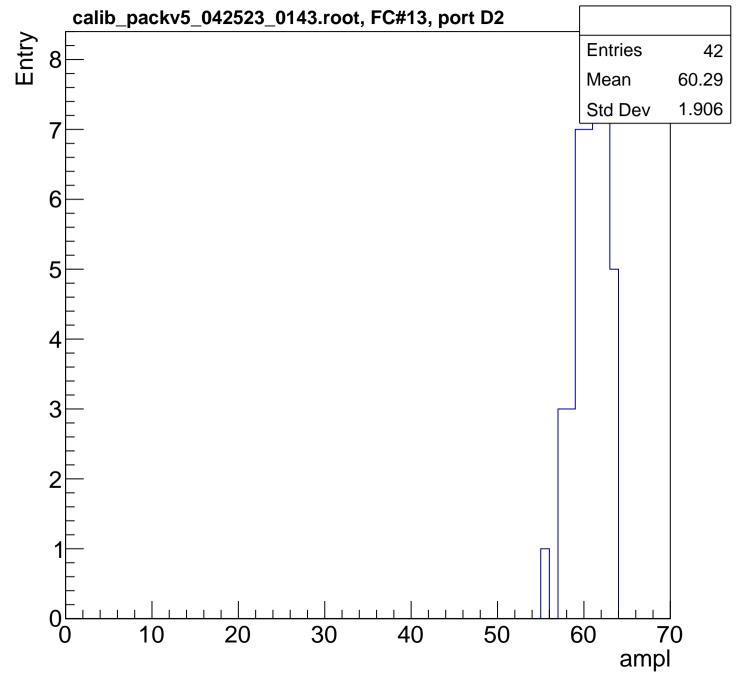


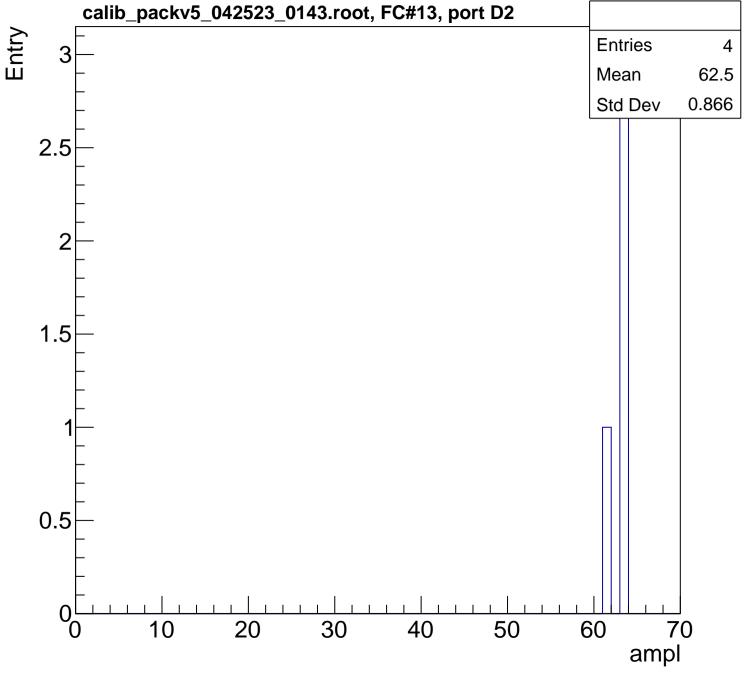


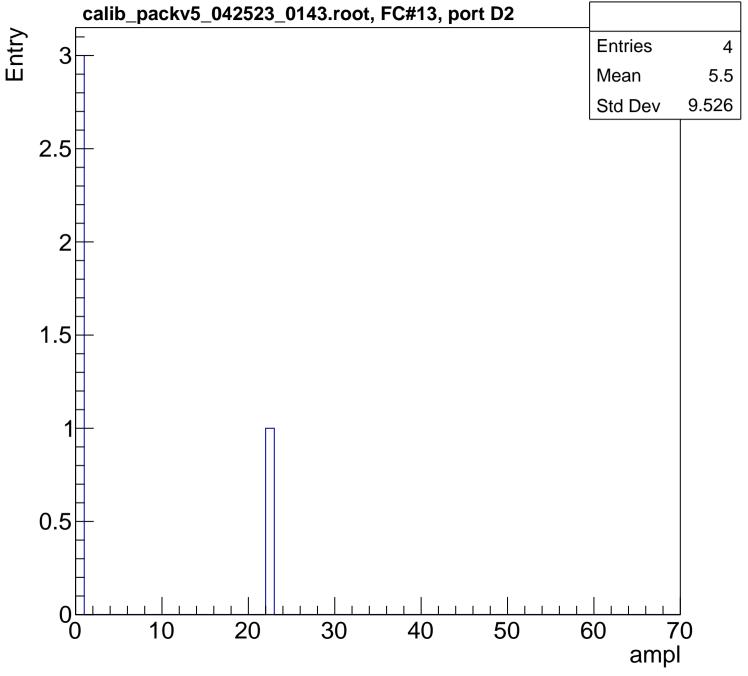


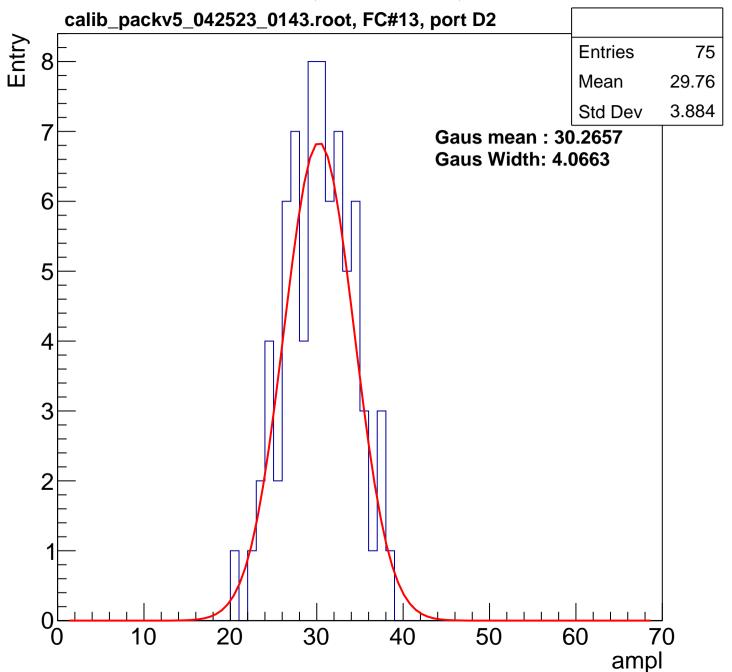


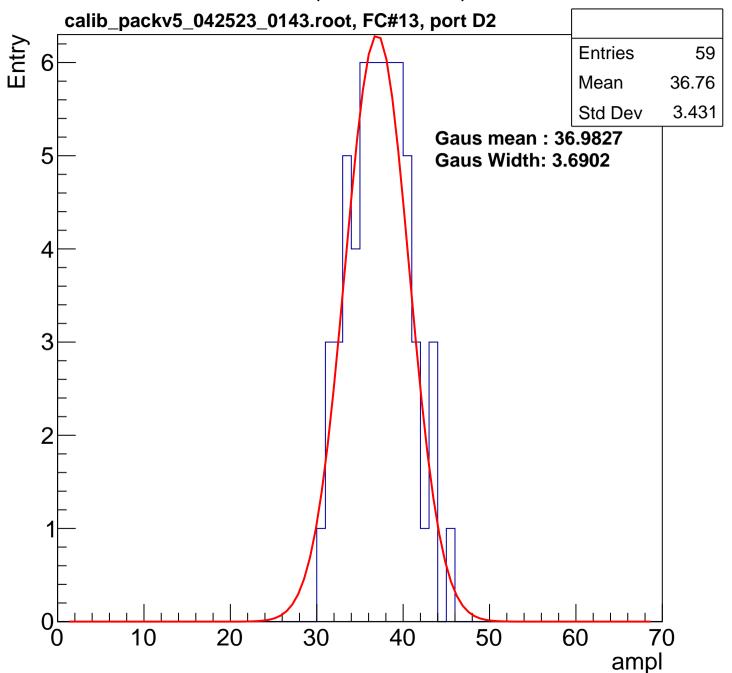


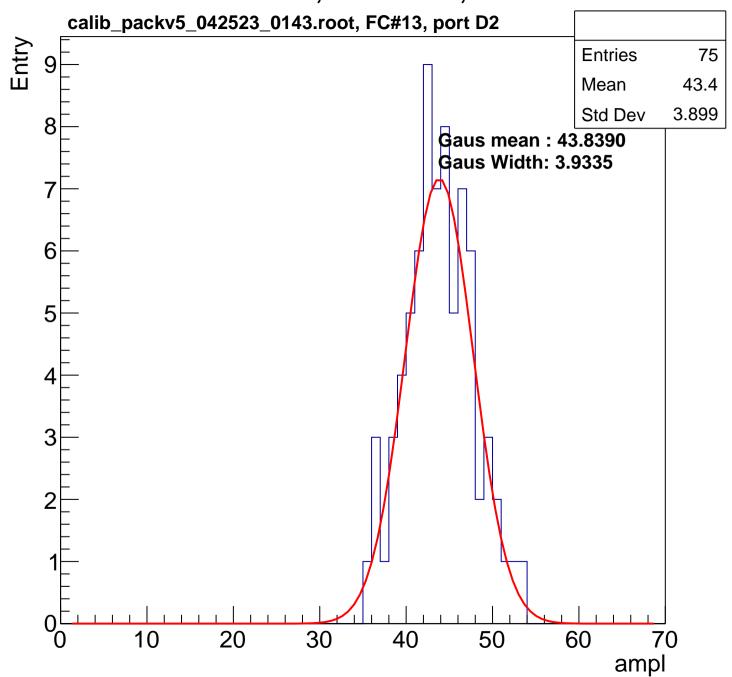


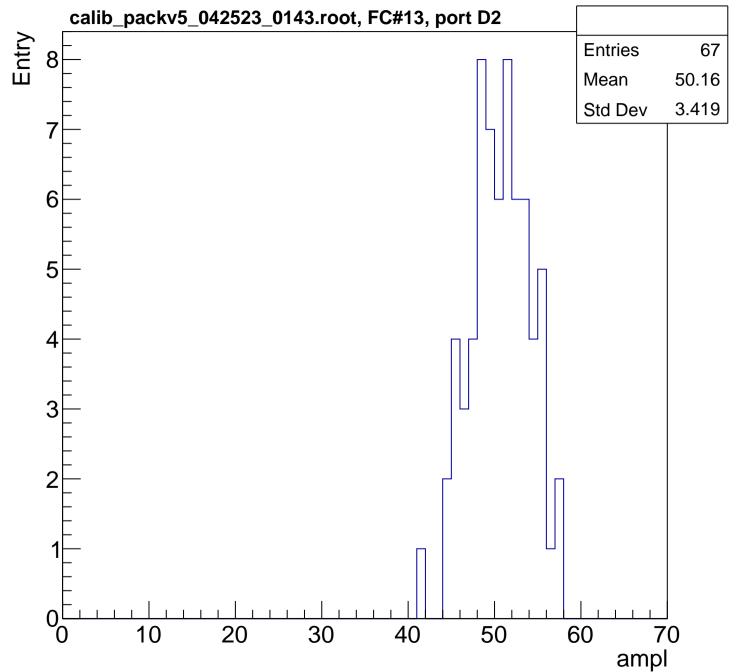


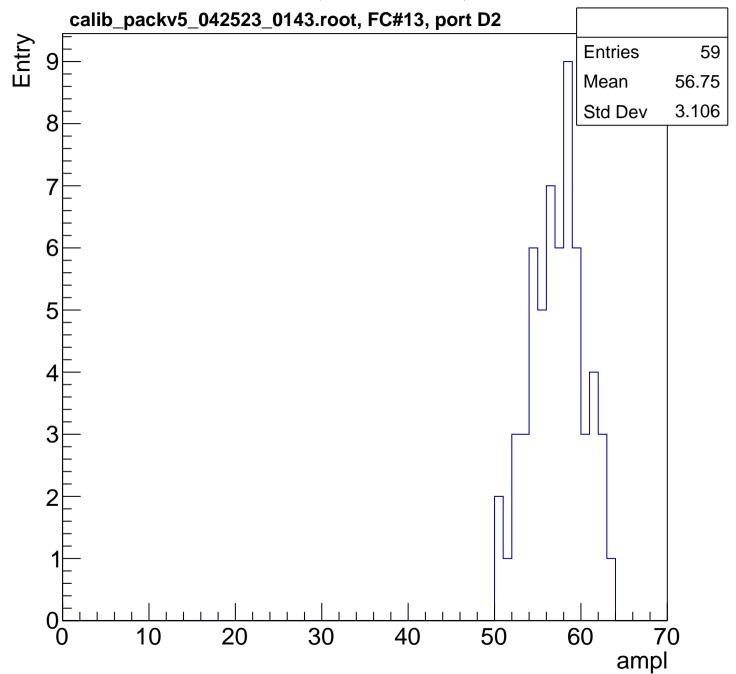


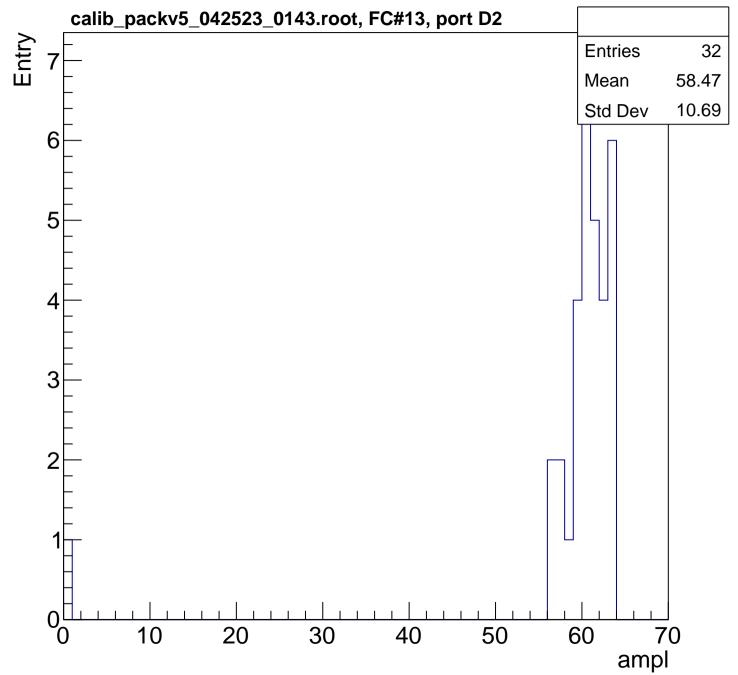


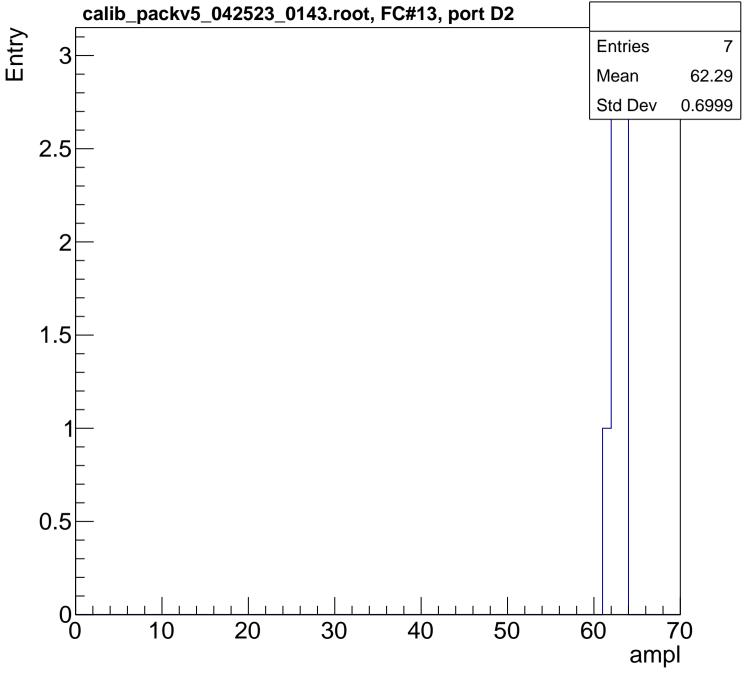






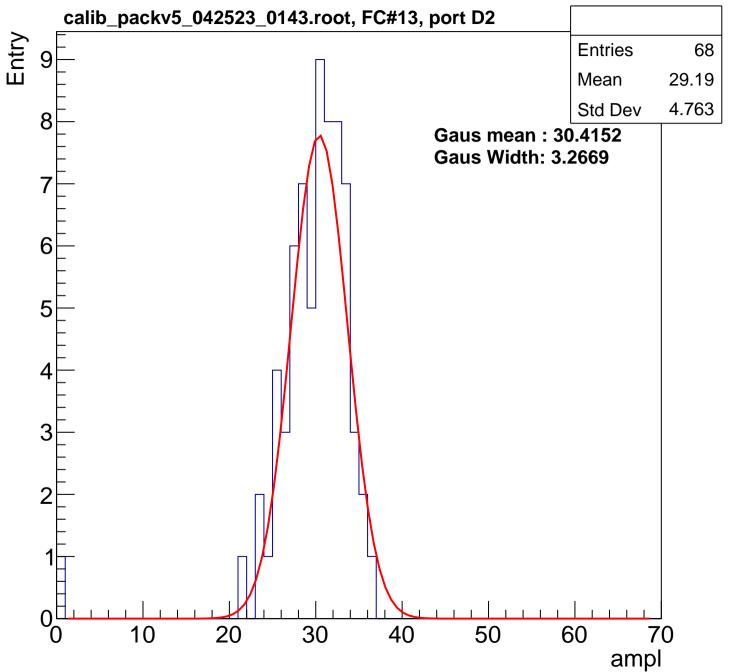


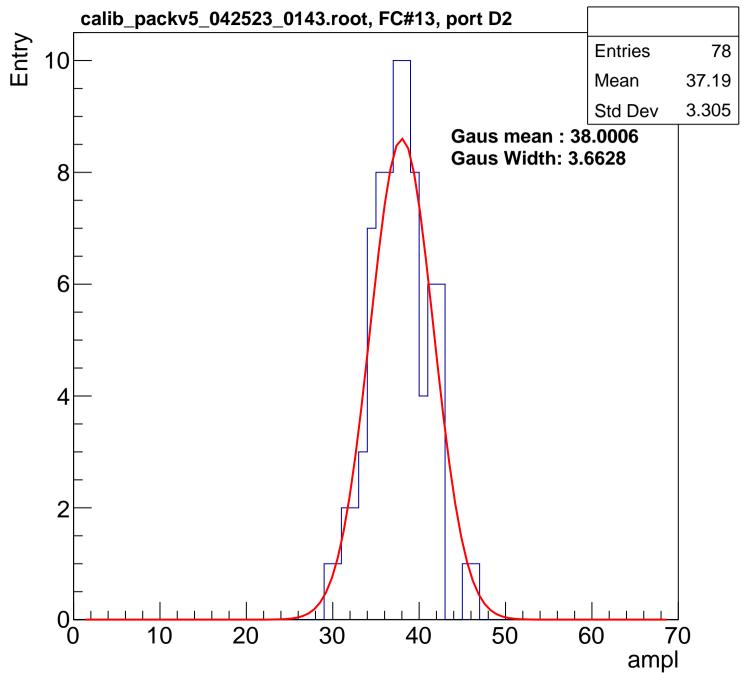


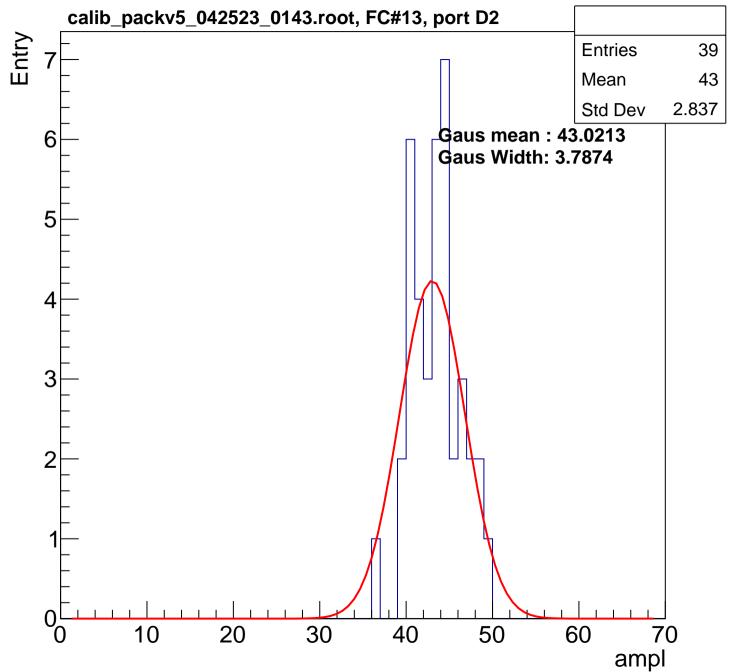


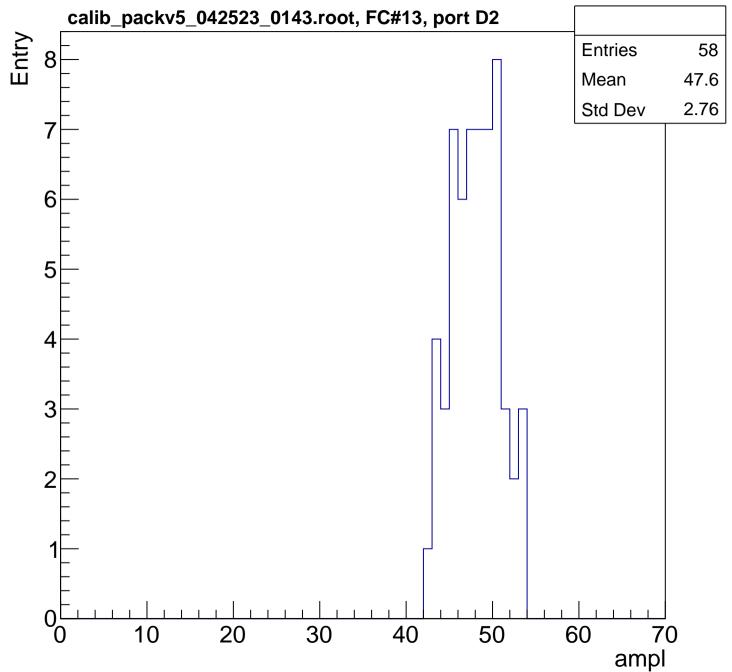
B1L003S, U2-ch77, adc7 calib_packv5_042523_0143.root, FC#13, port D2 Entry **Entries** Mean 18 Std Dev 0 8.0 0.6 0.4 0.2 10 20 30 40 50 60 70

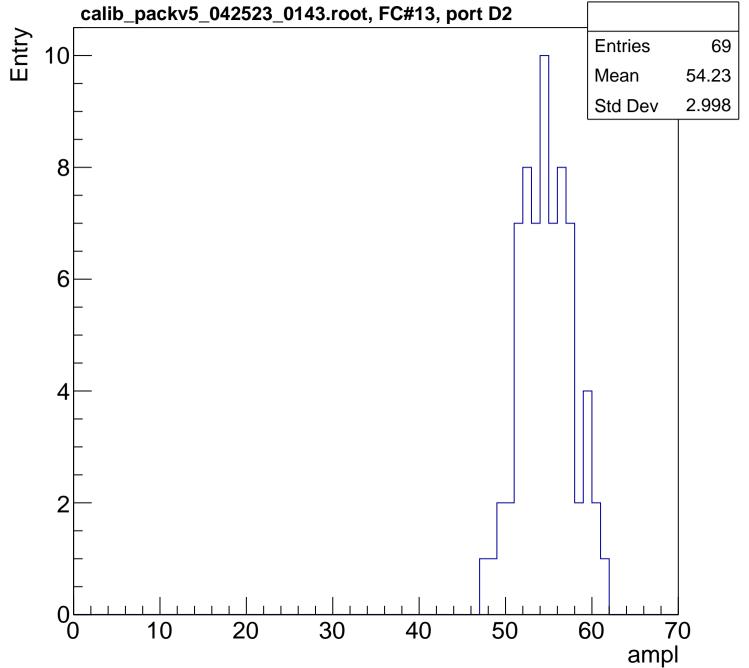
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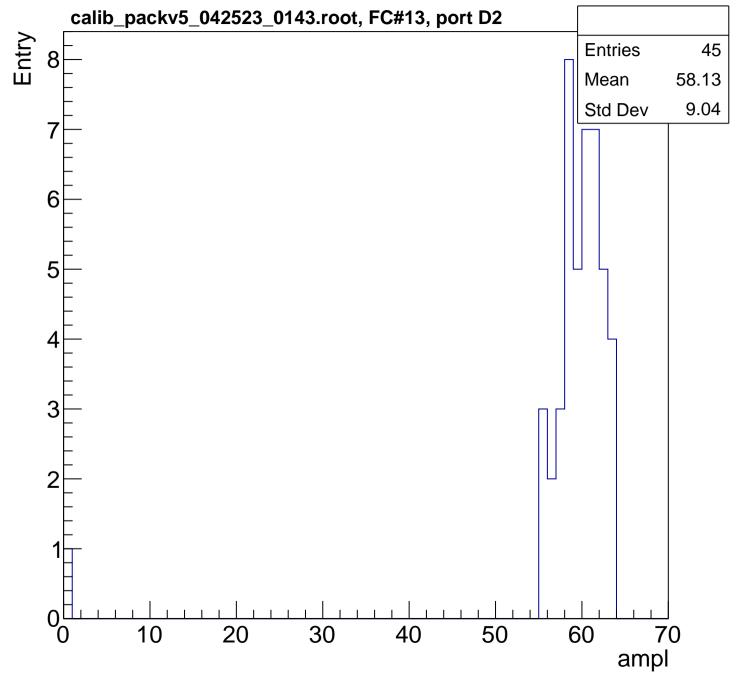


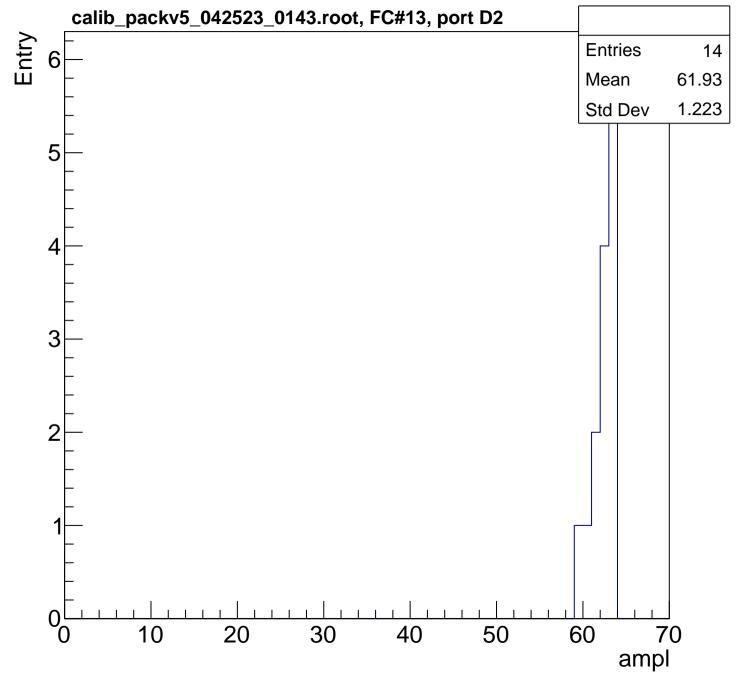




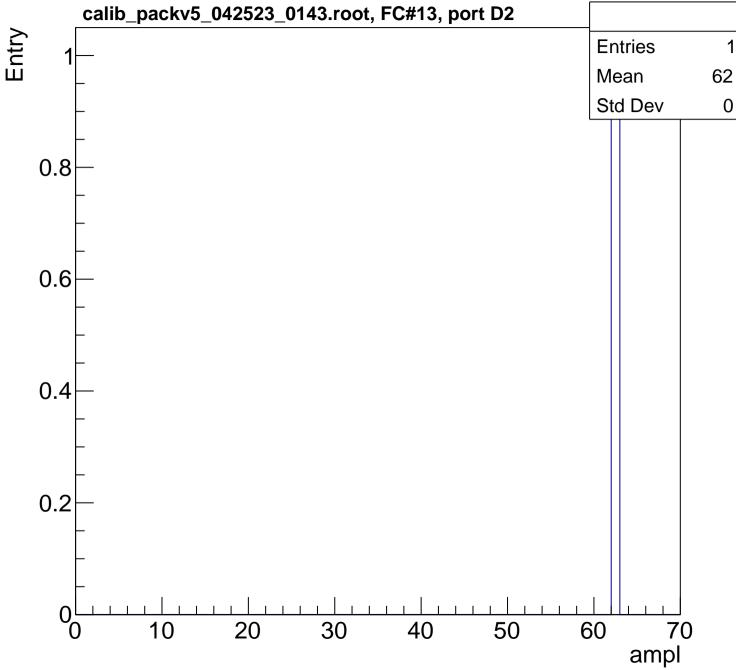


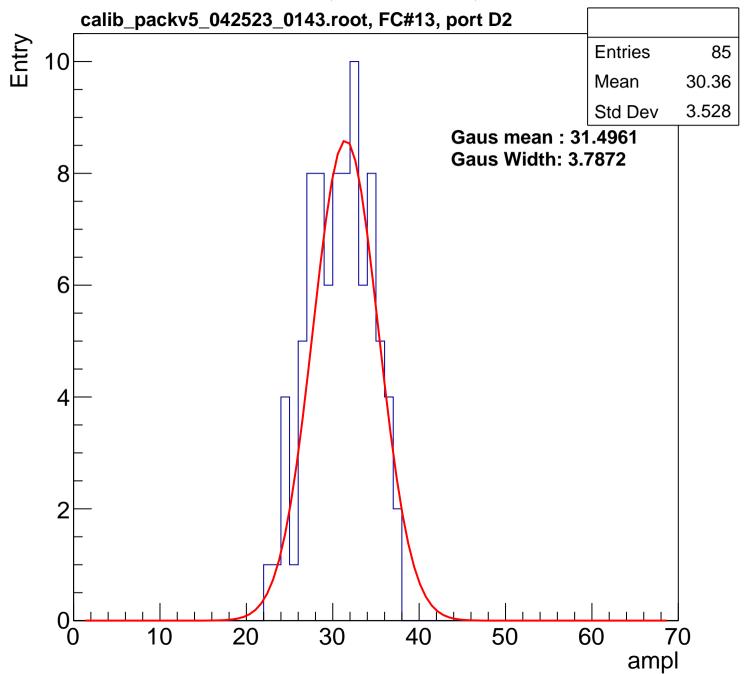


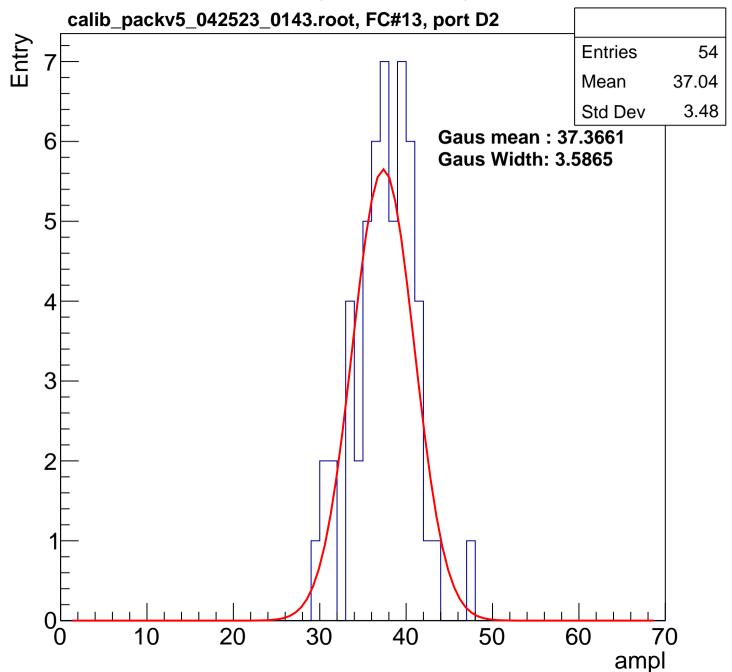


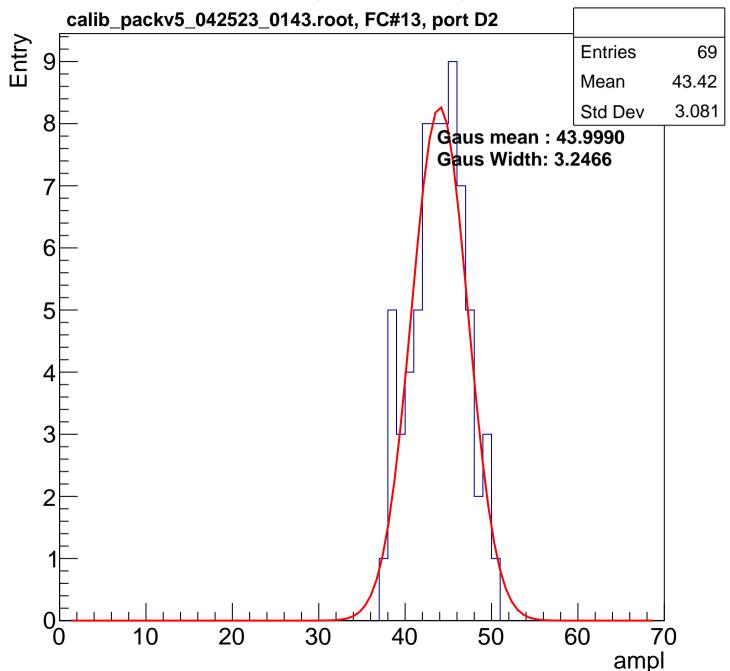


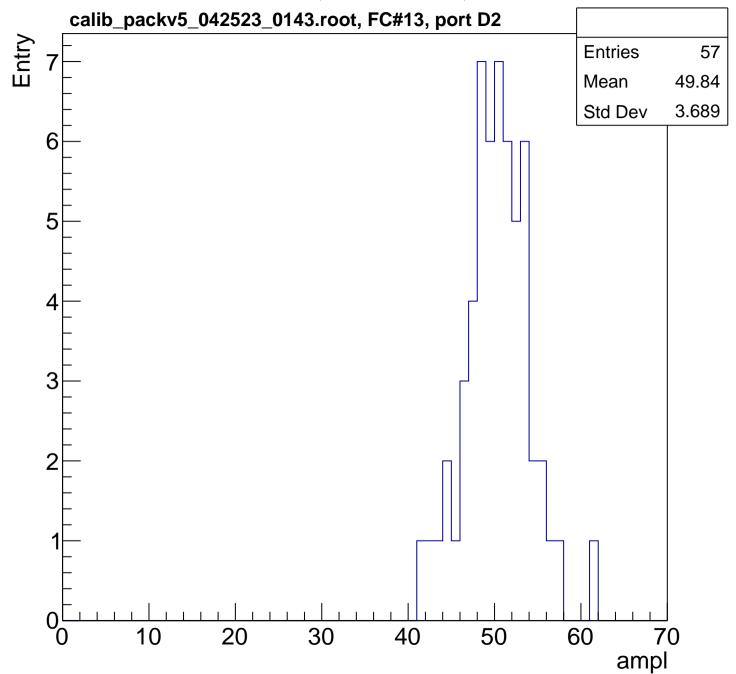
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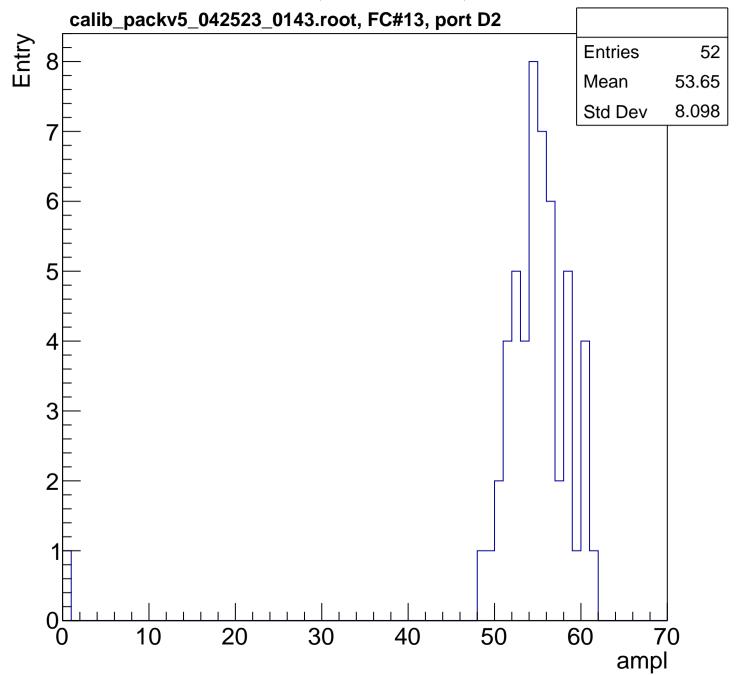


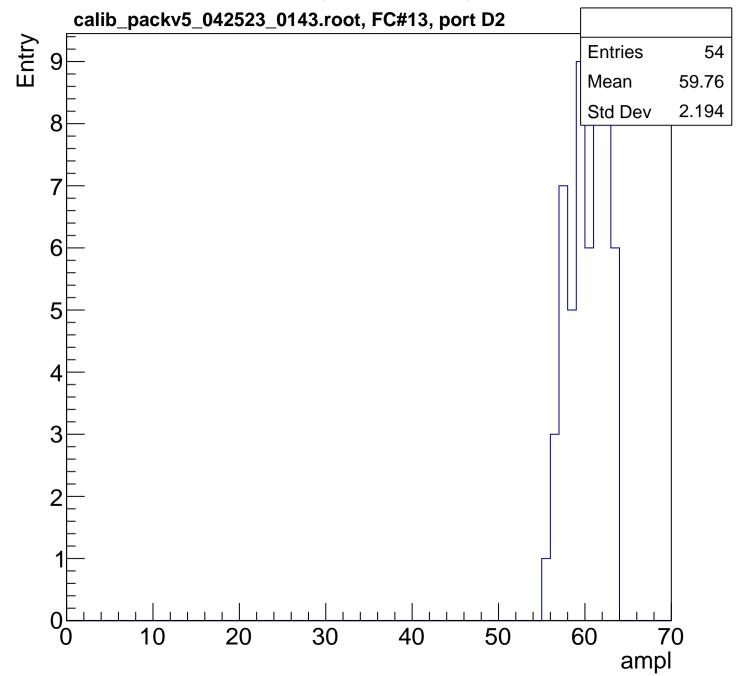


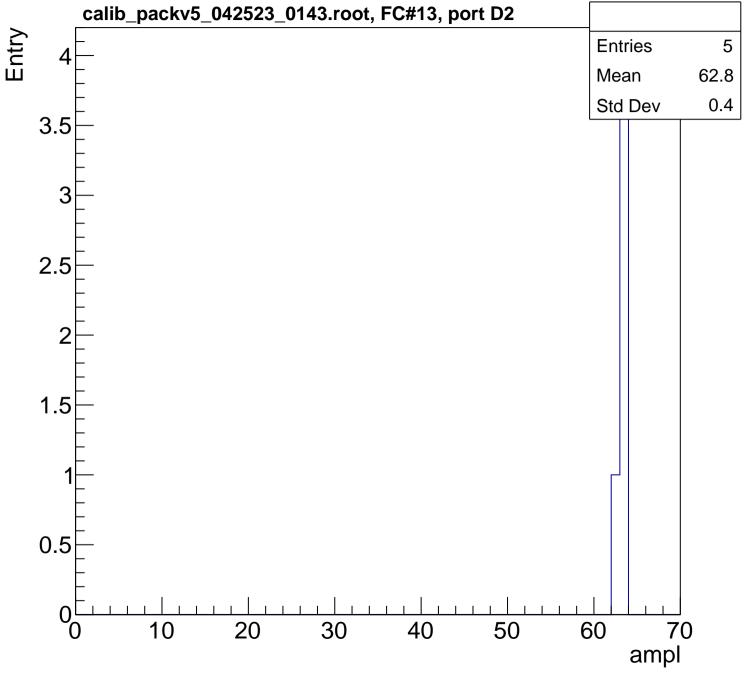




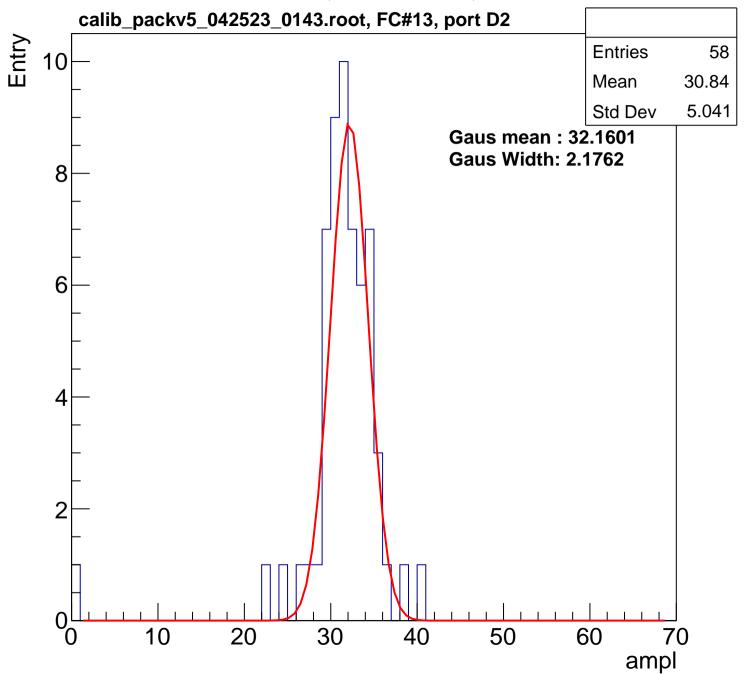


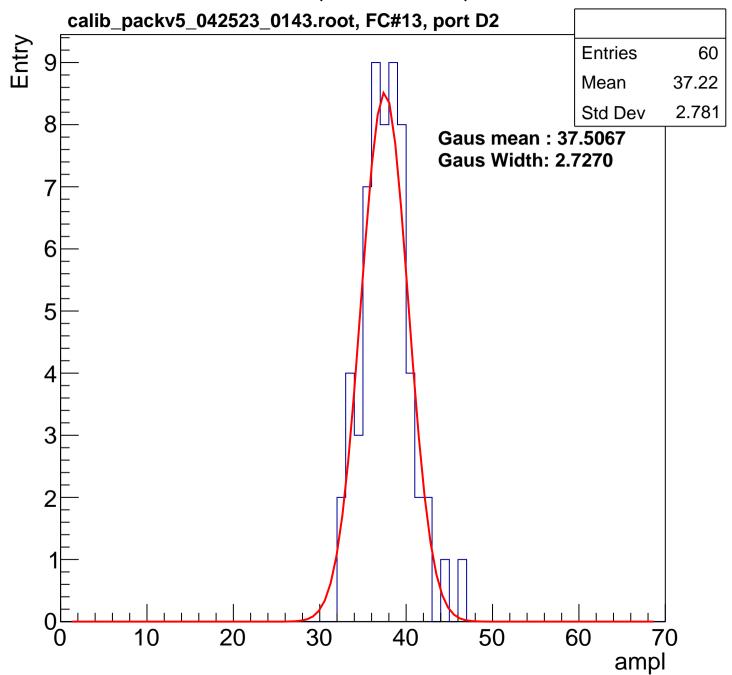


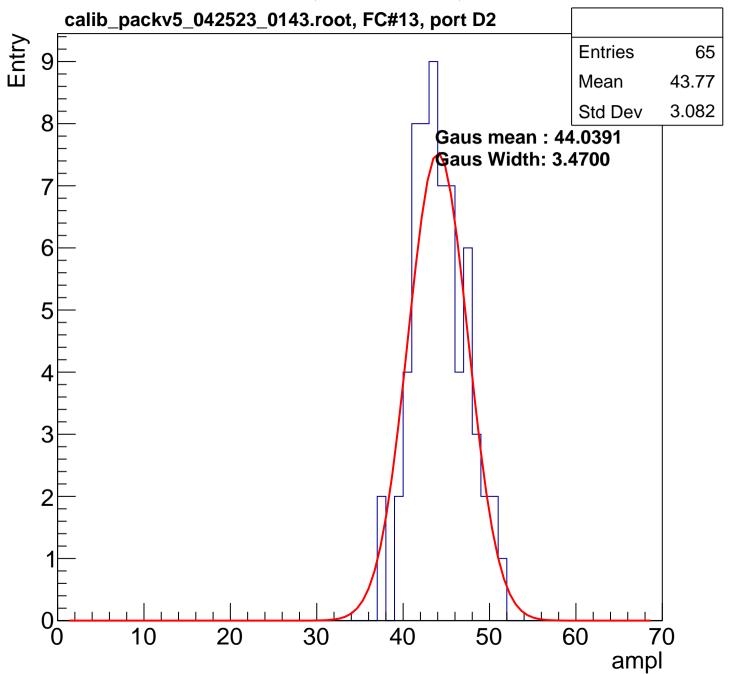


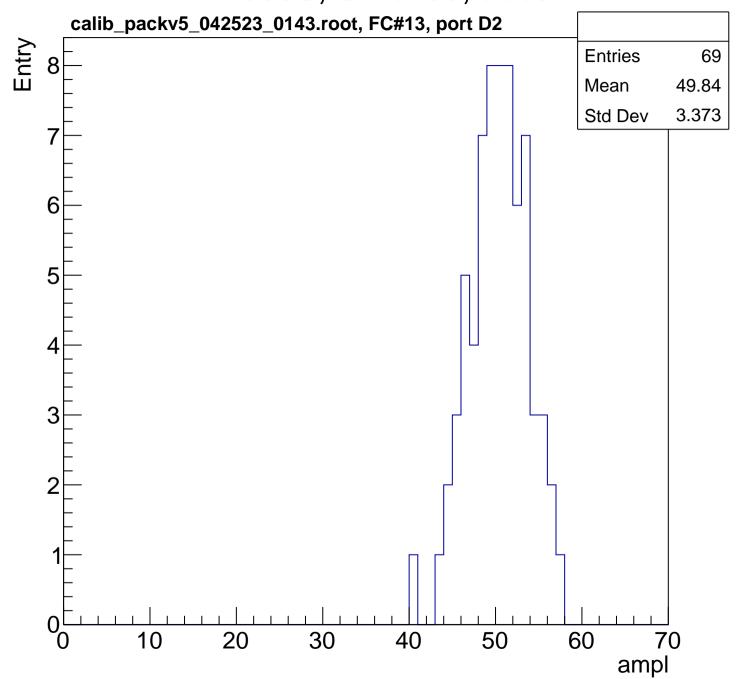


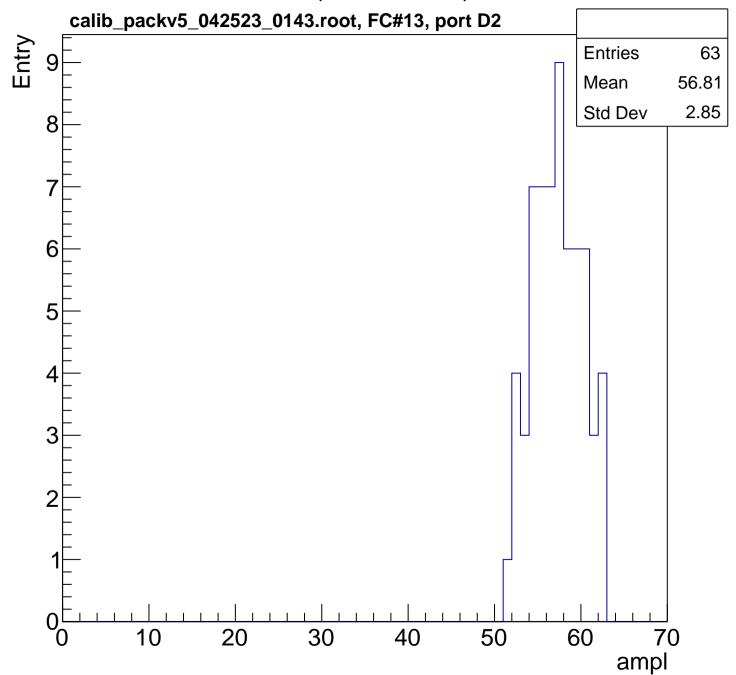
B1L003S, U2-ch79, adc7 calib_packv5_042523_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

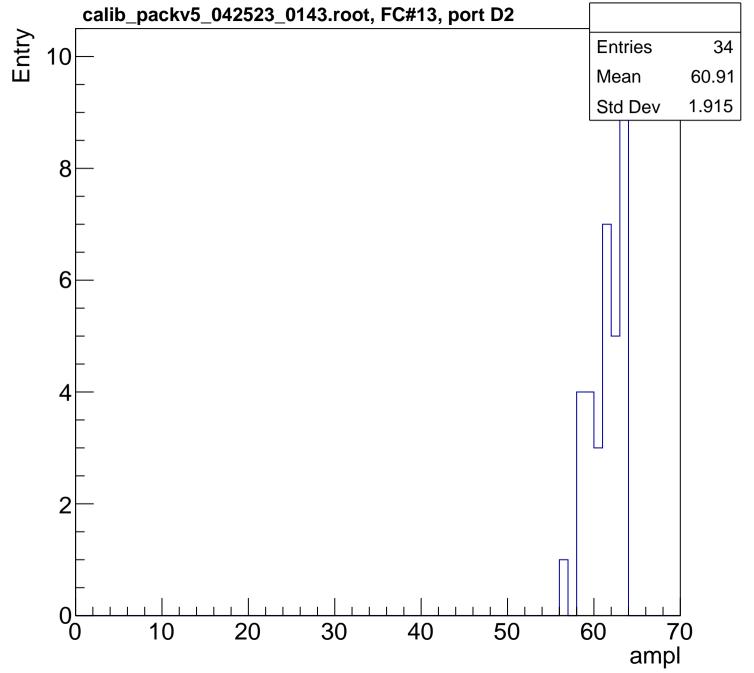


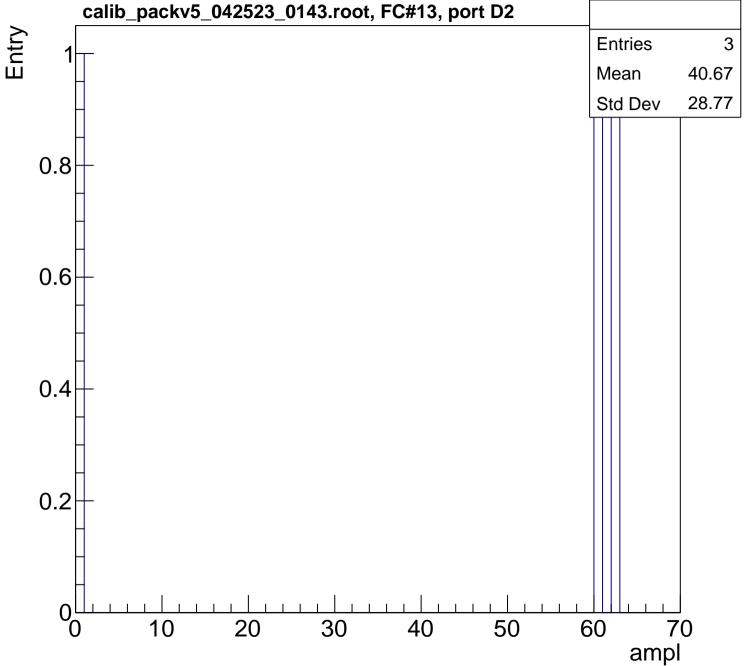




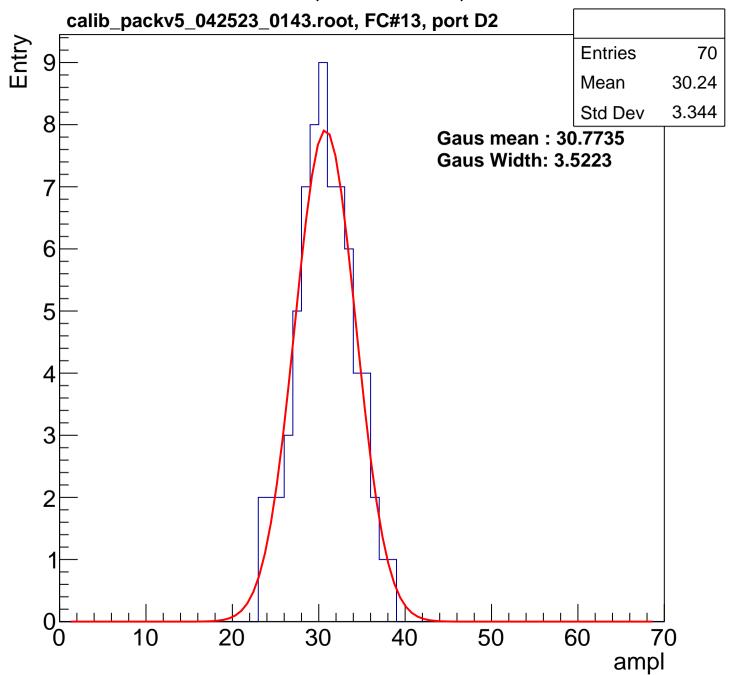


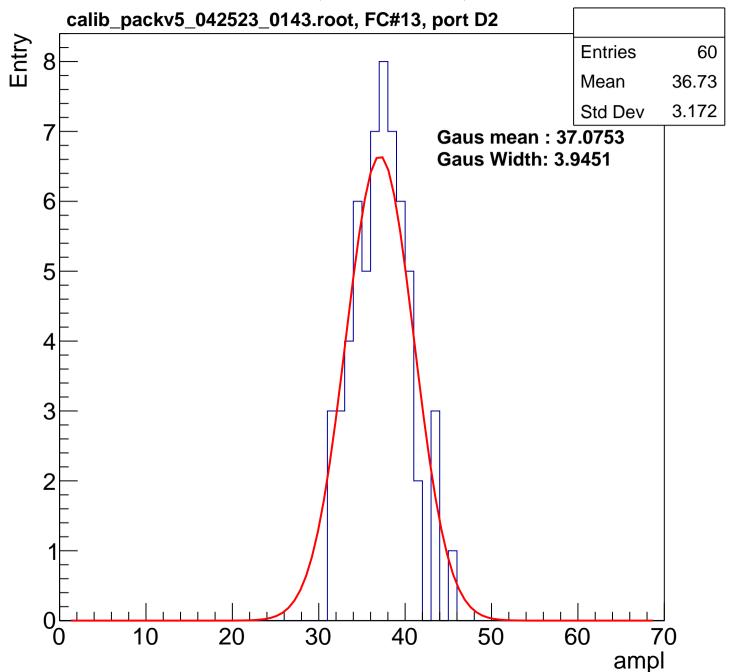


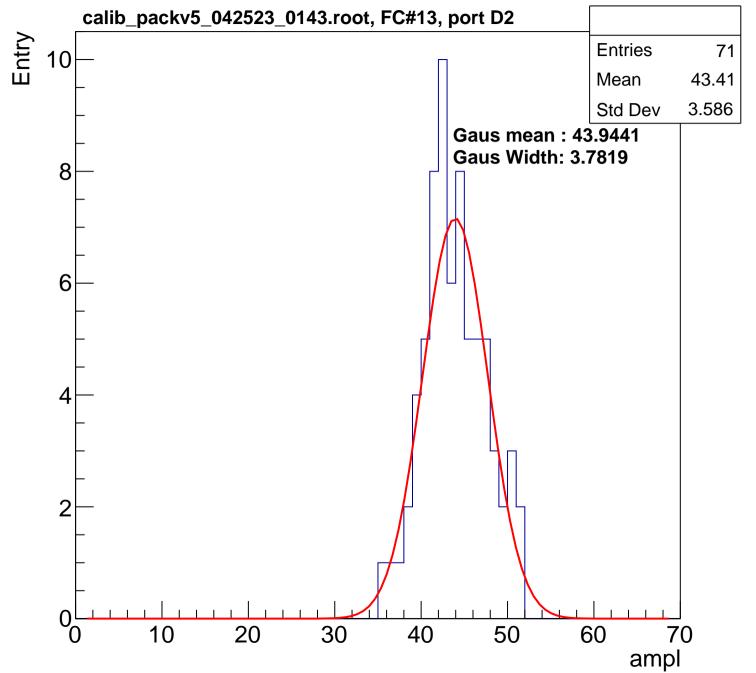


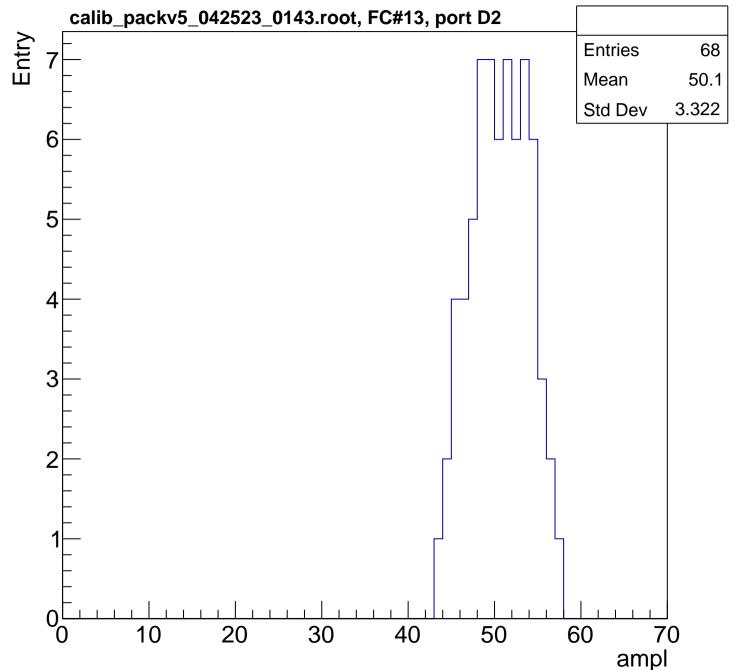


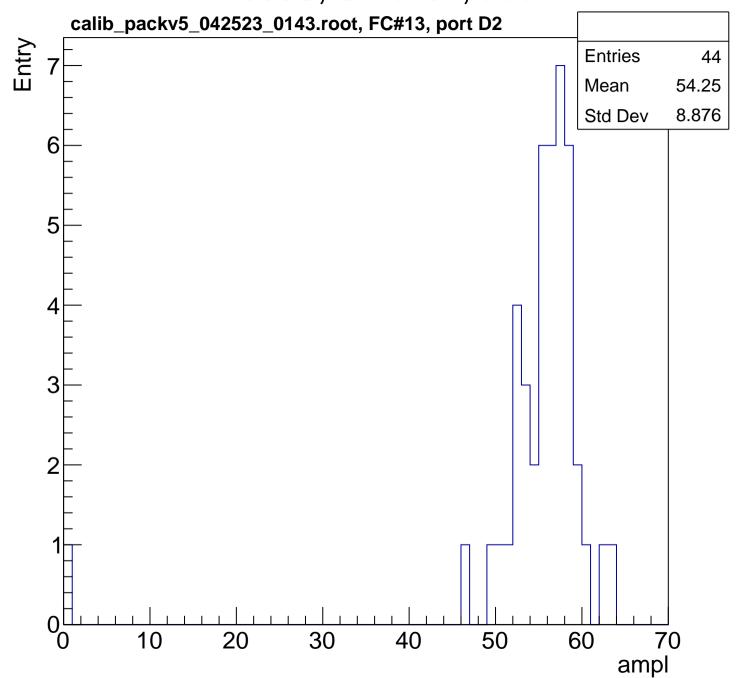
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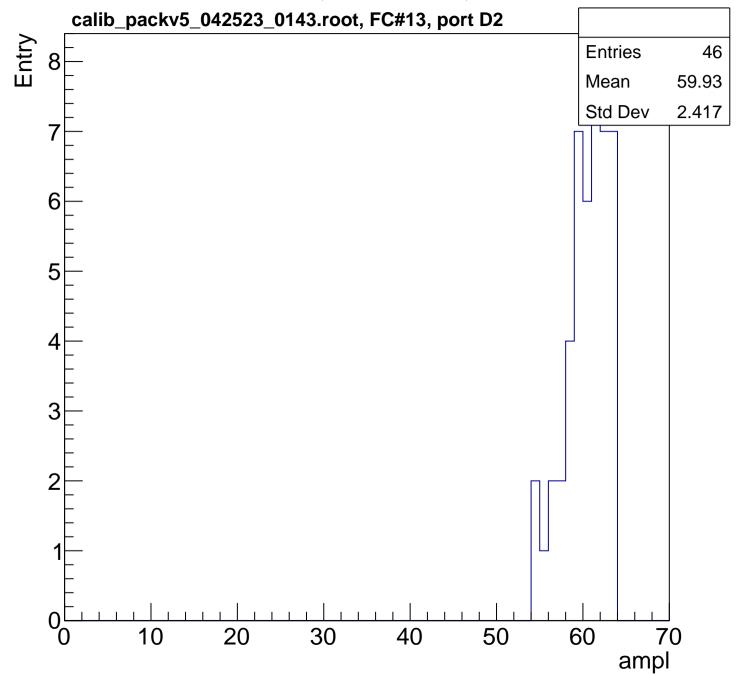


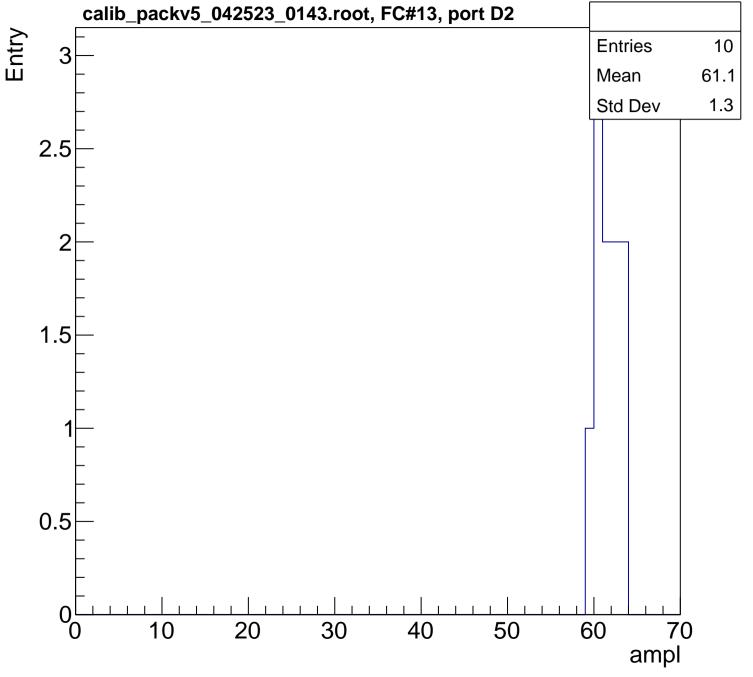




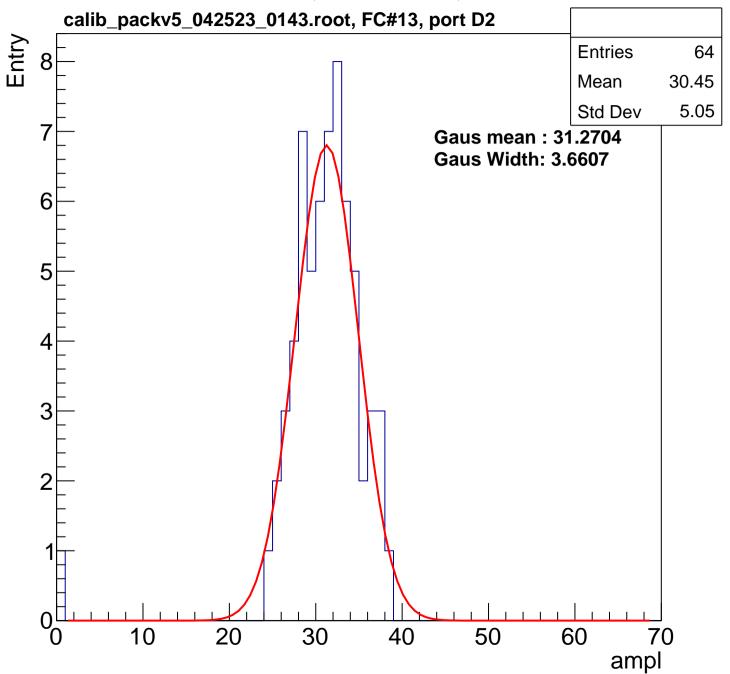


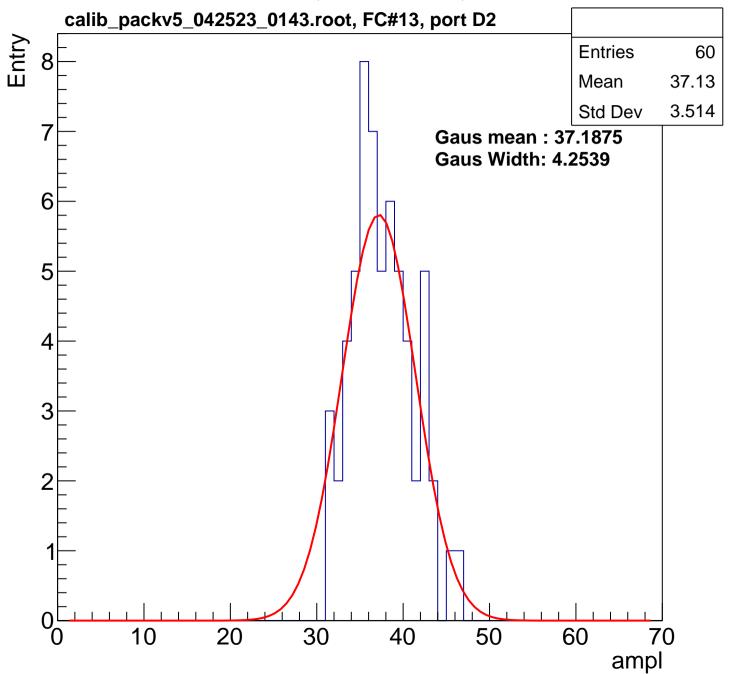


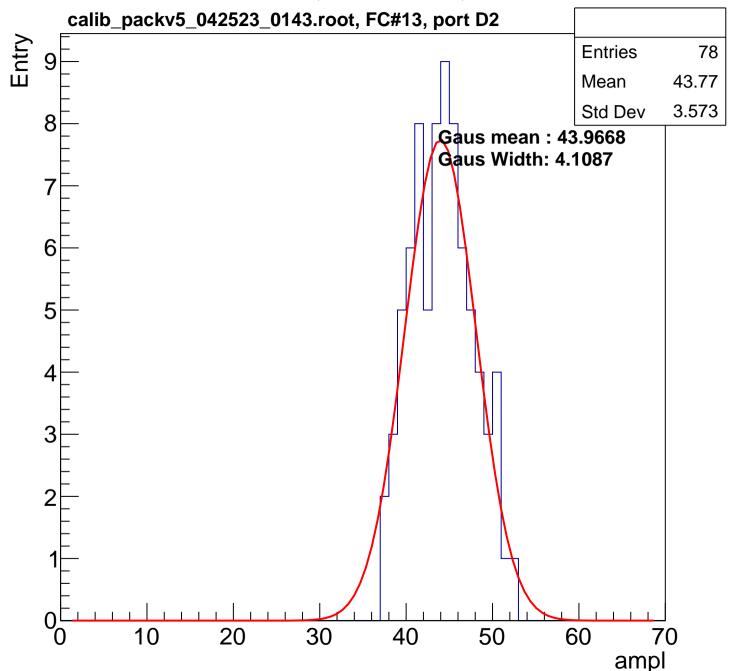


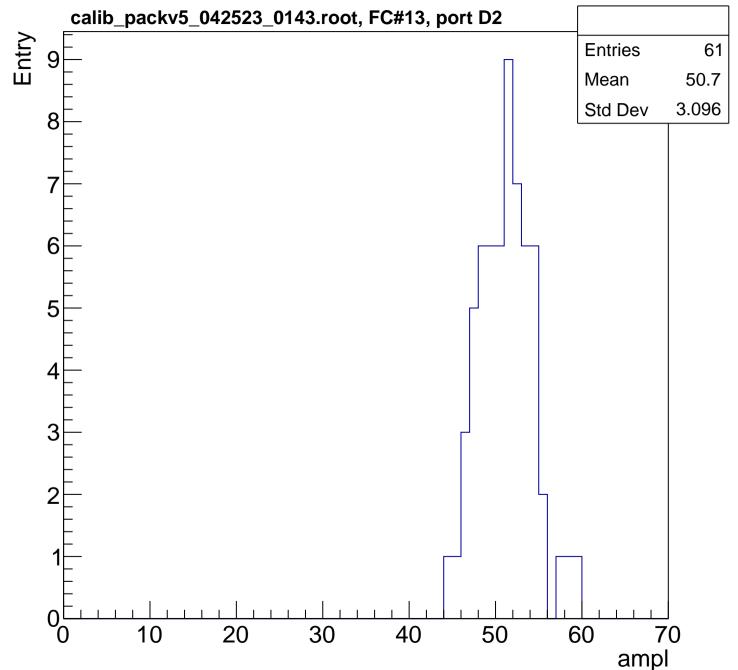


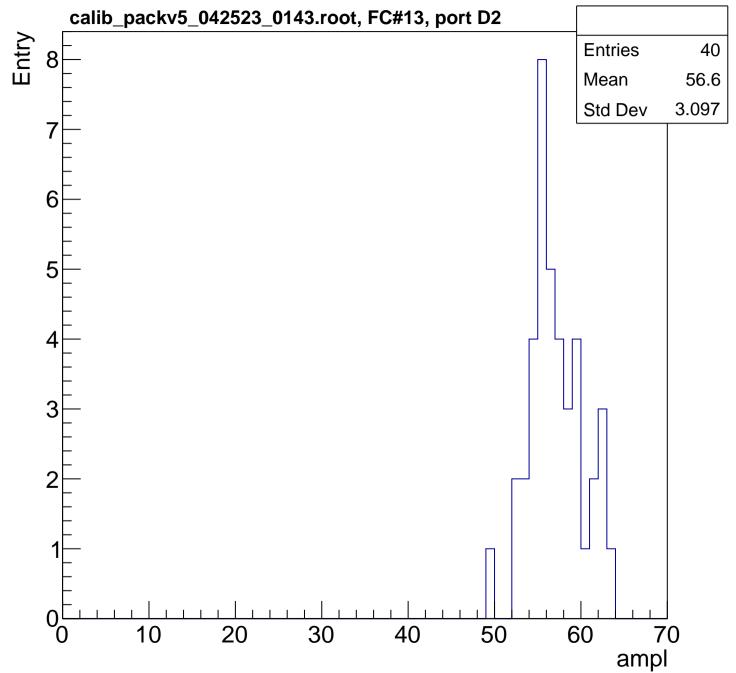
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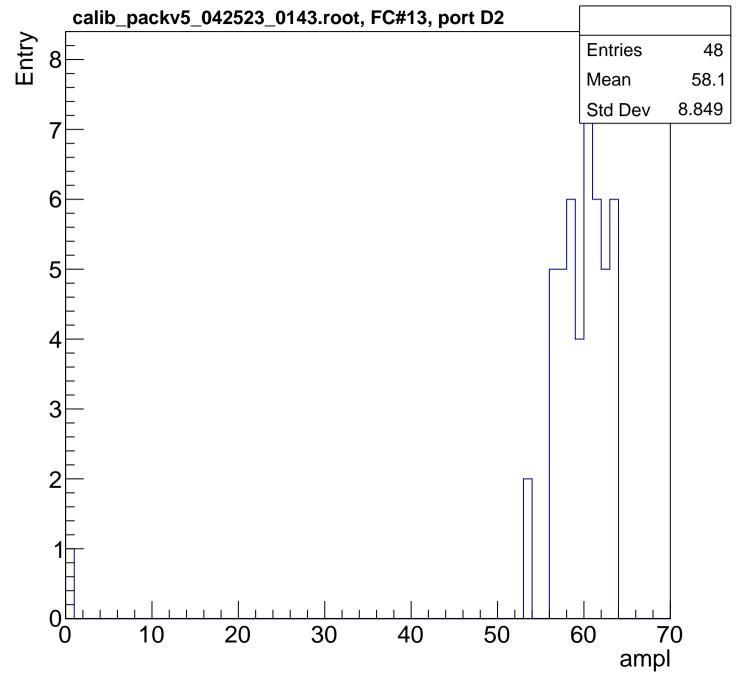


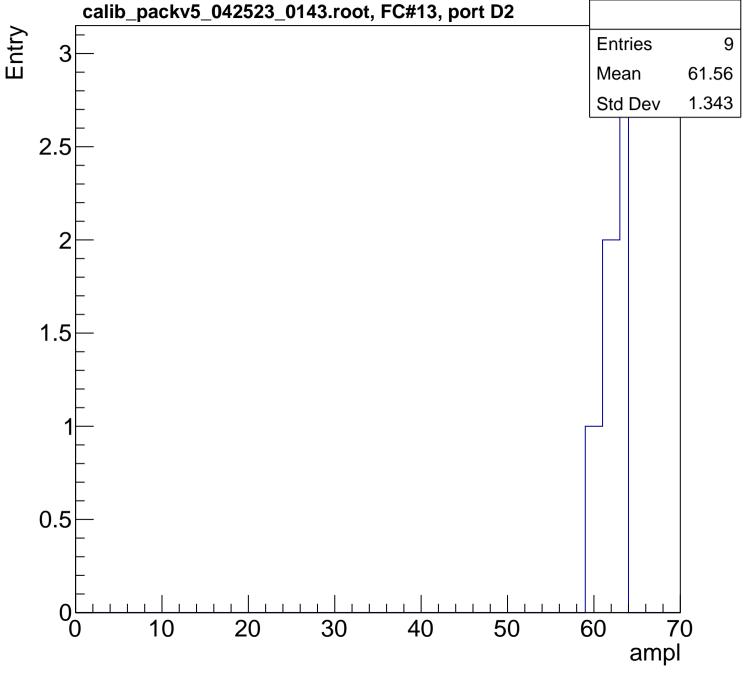


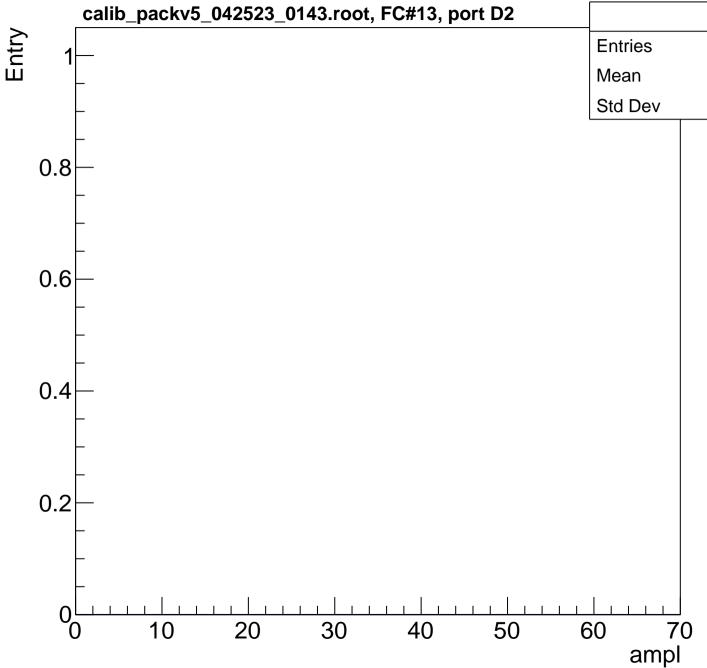


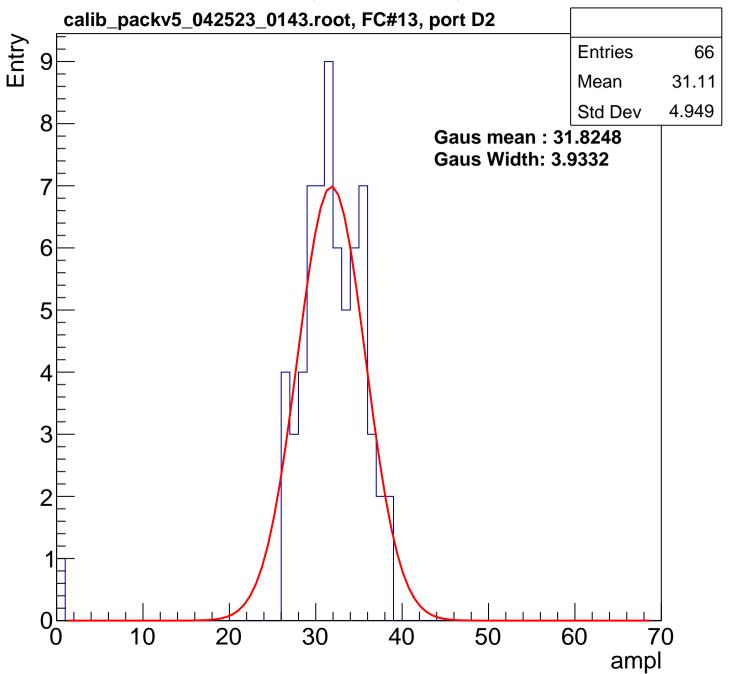


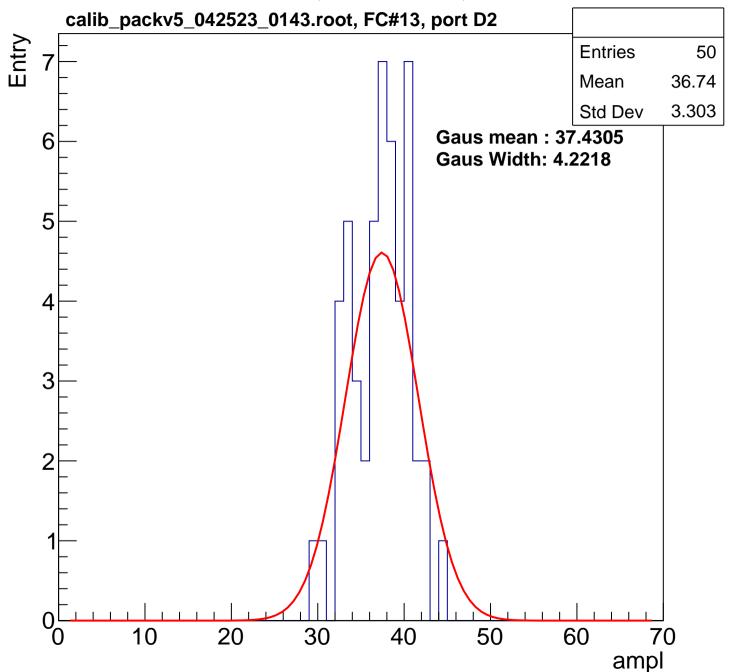


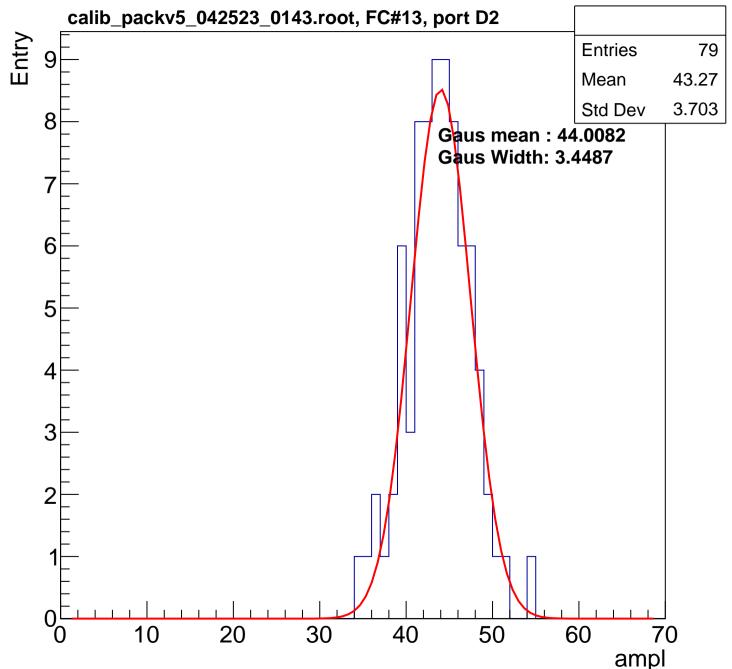


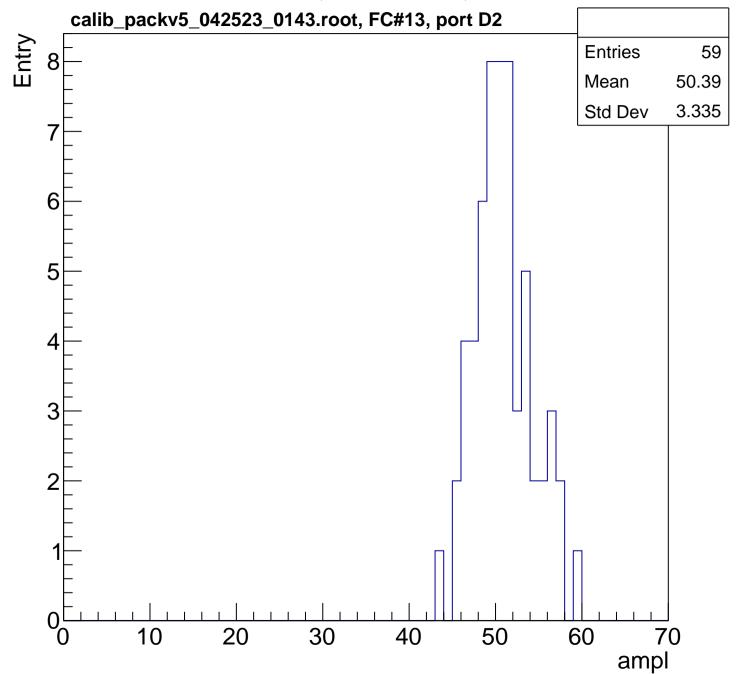


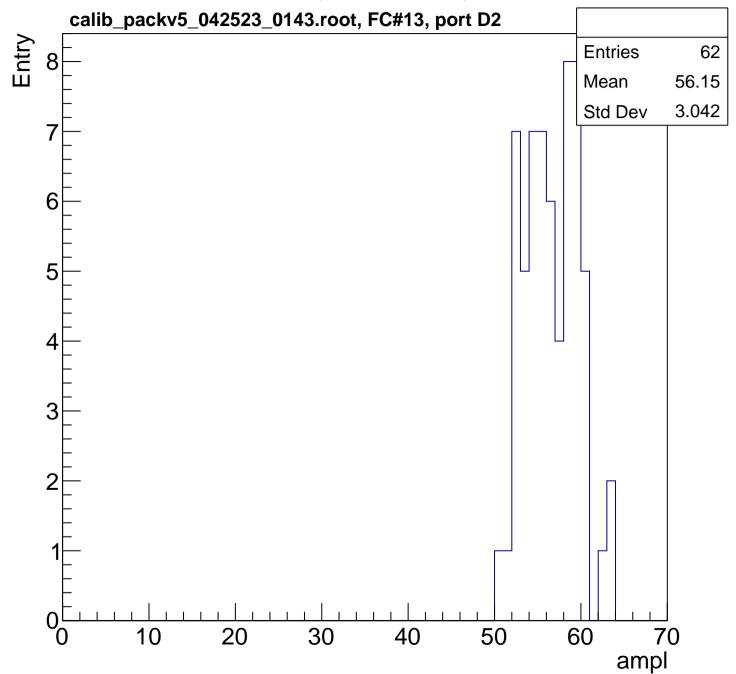


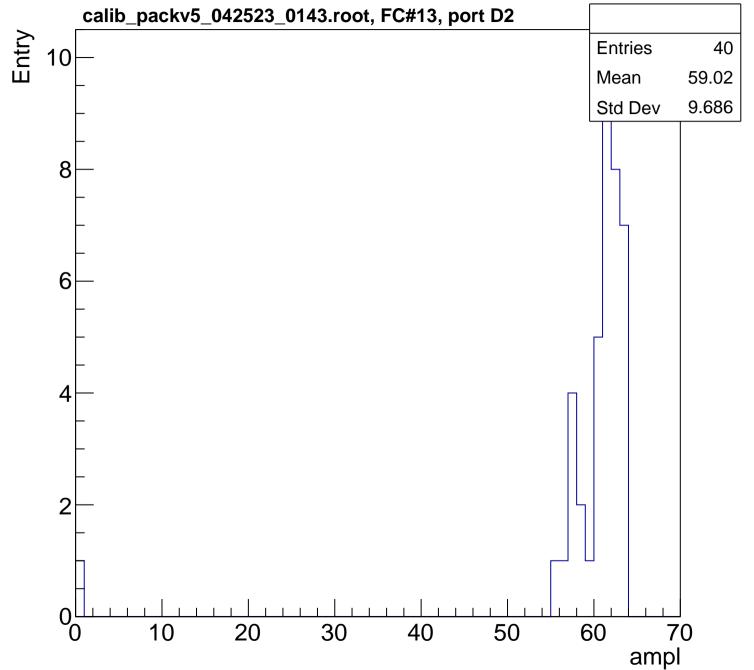


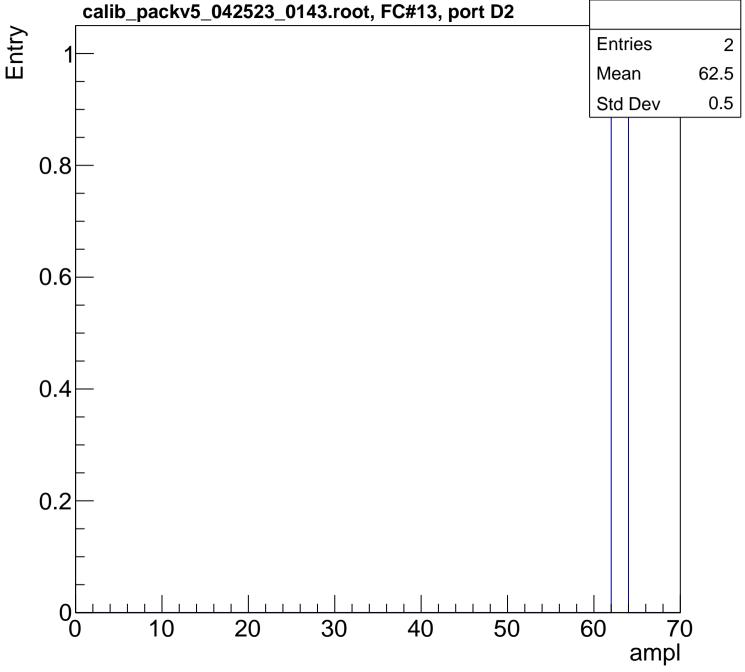


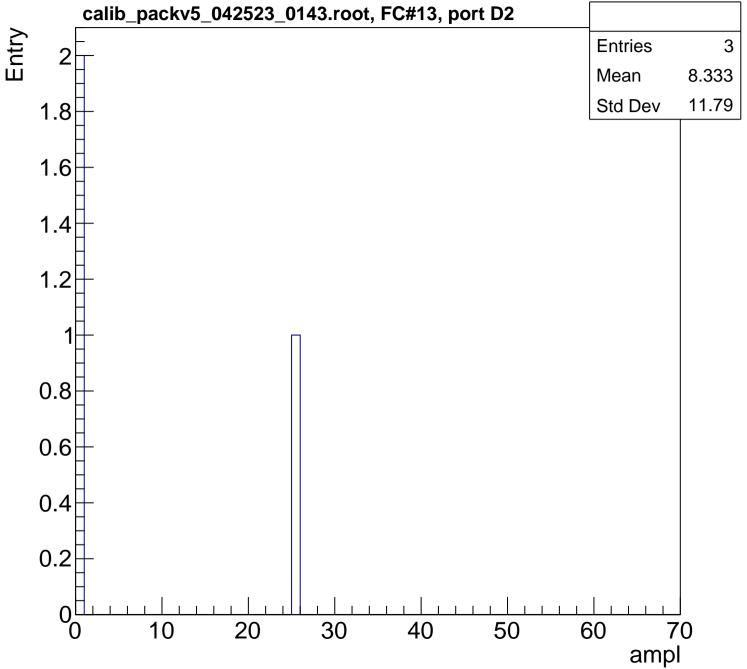


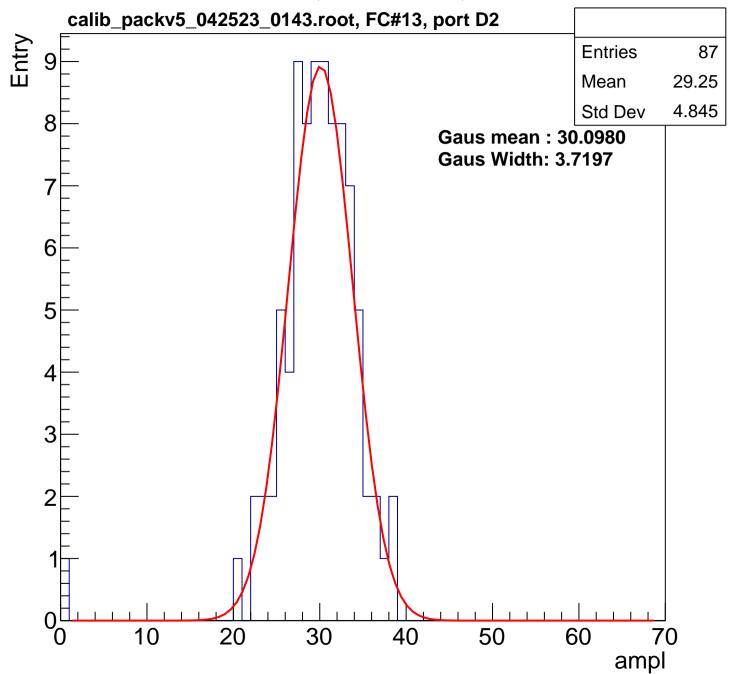


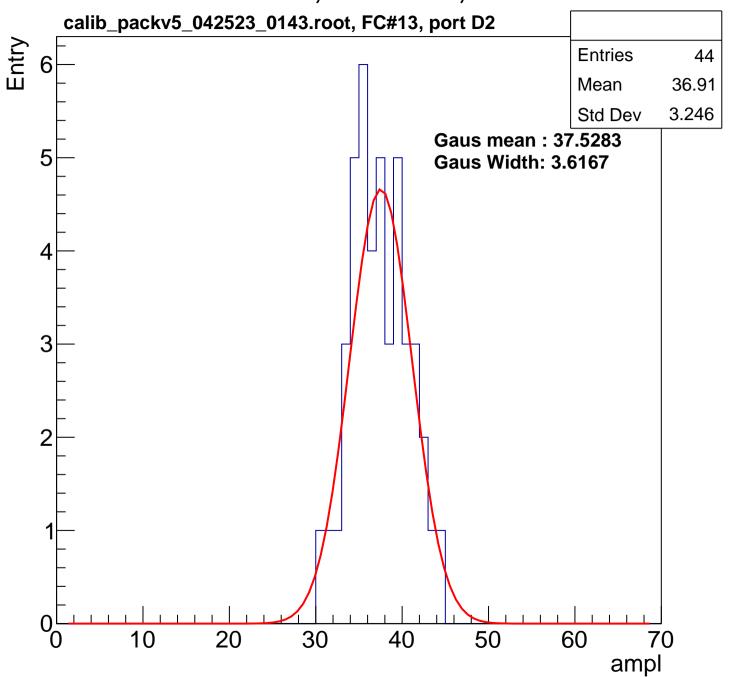


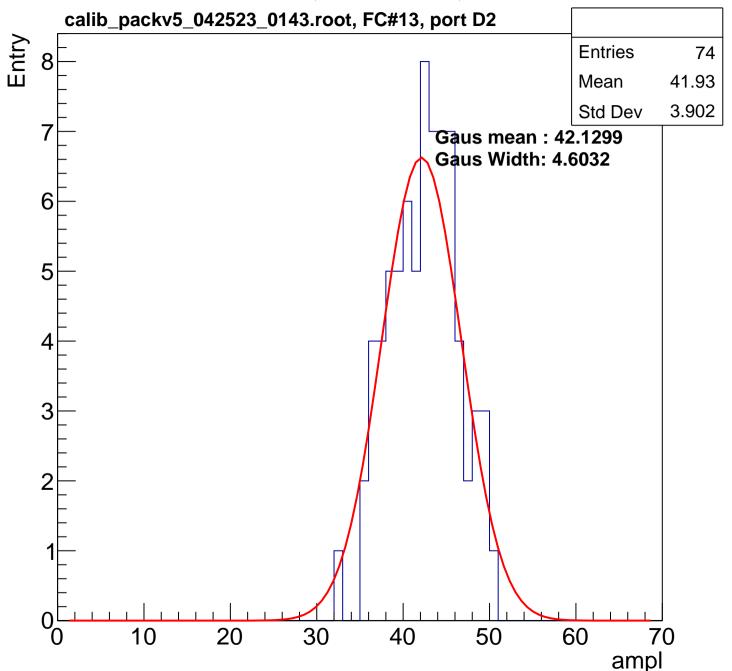


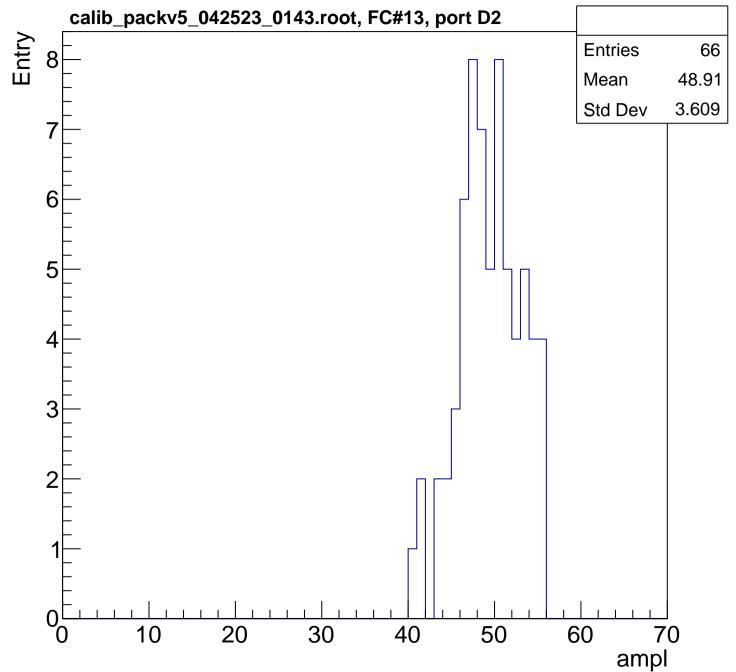


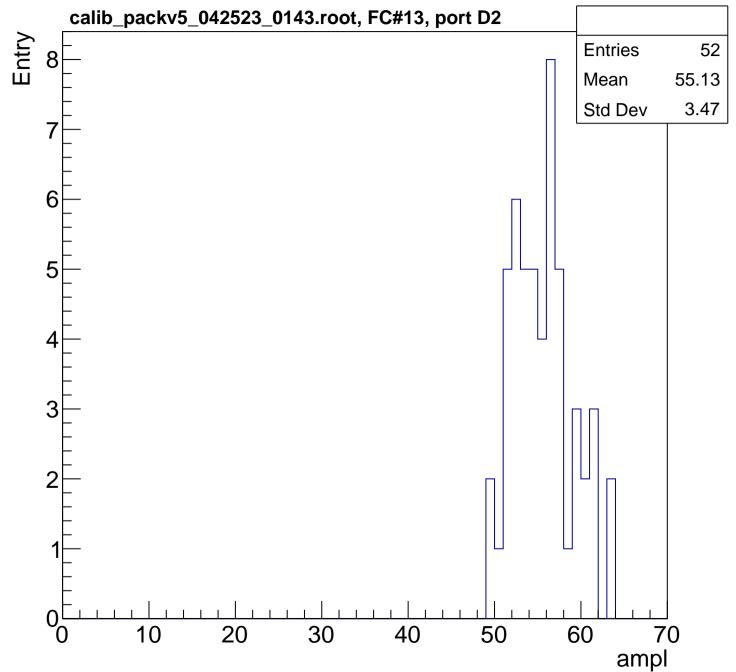


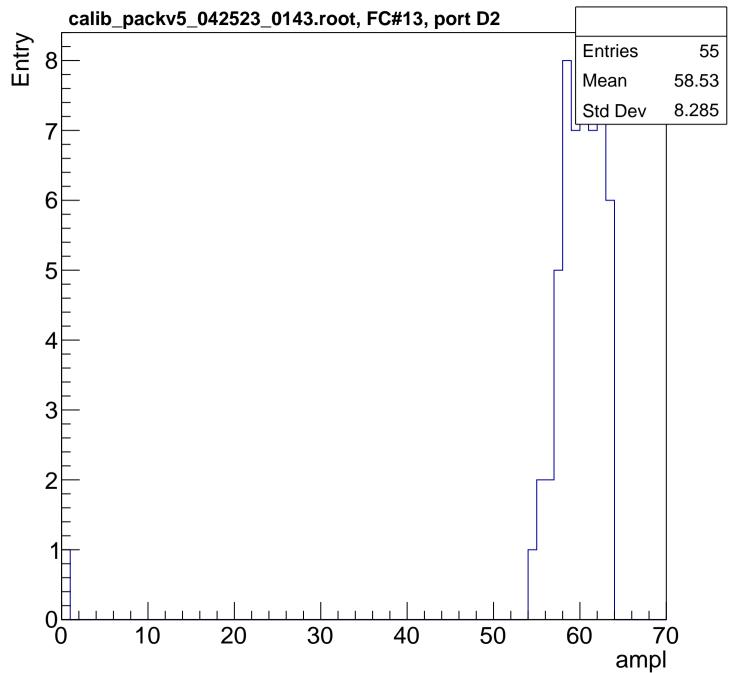


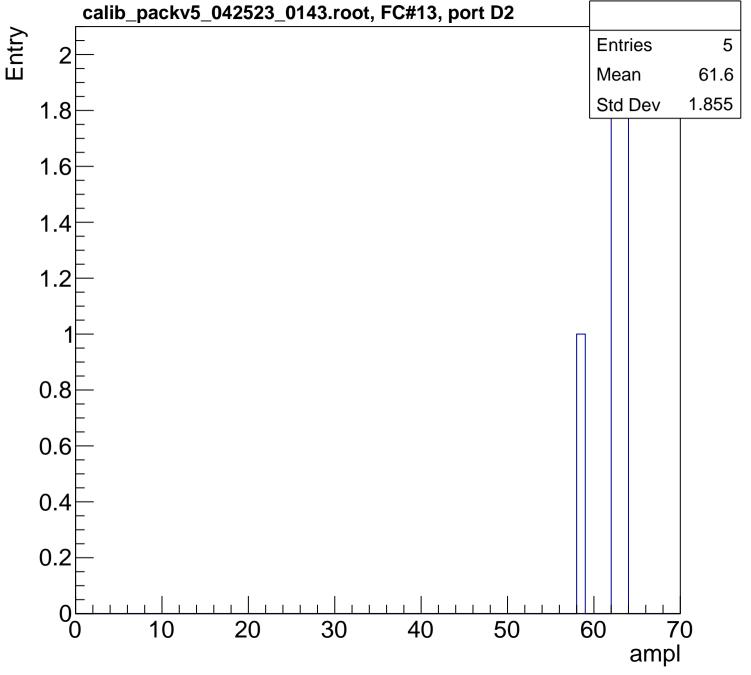




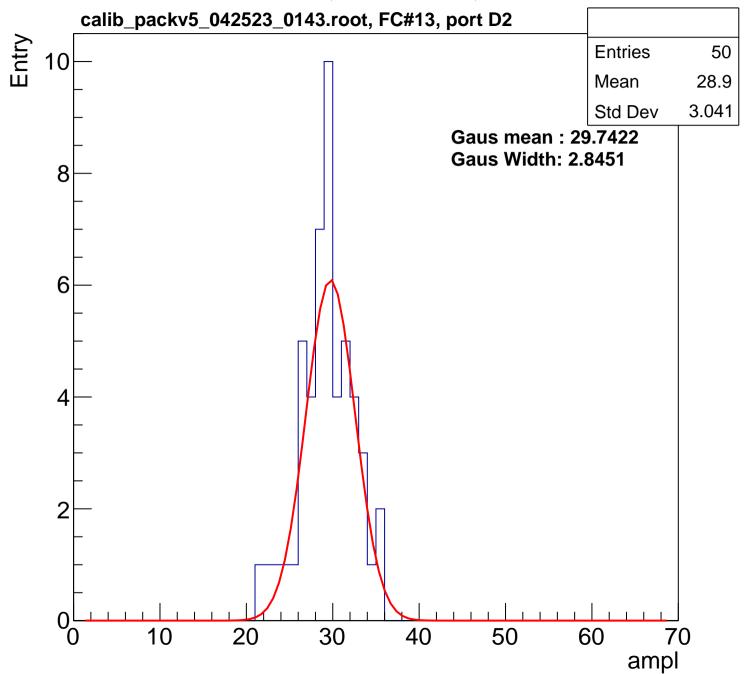


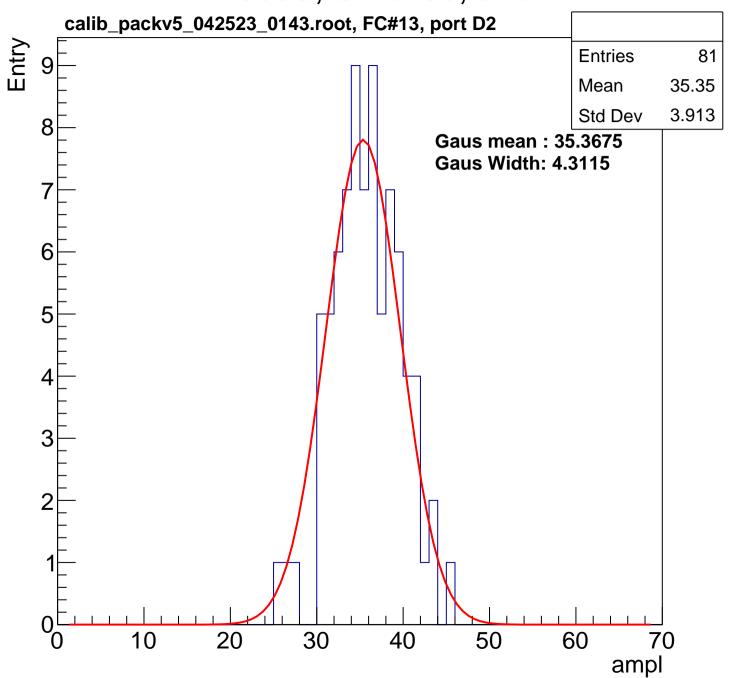


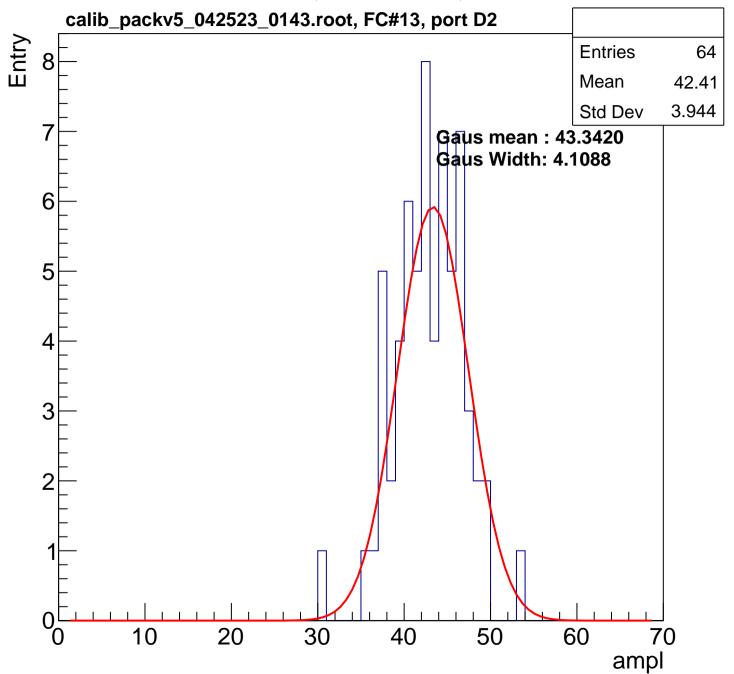


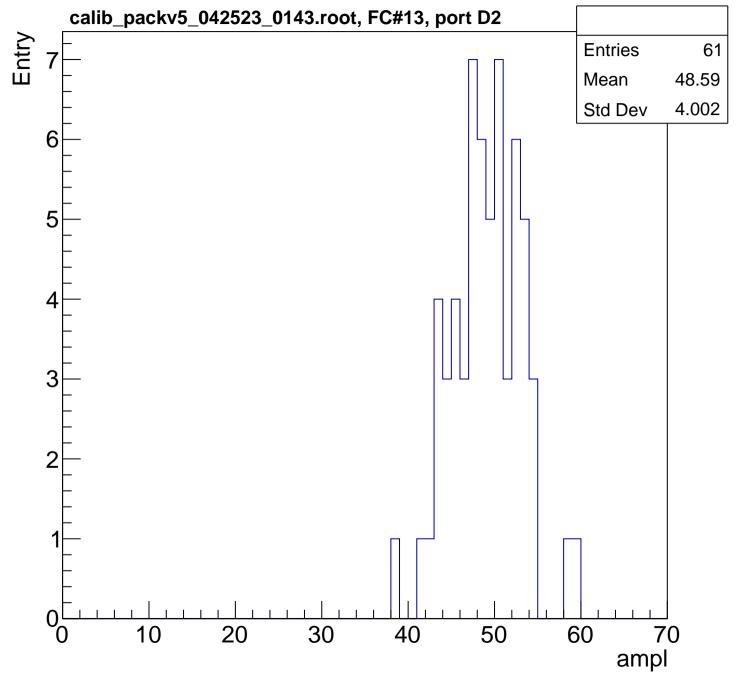


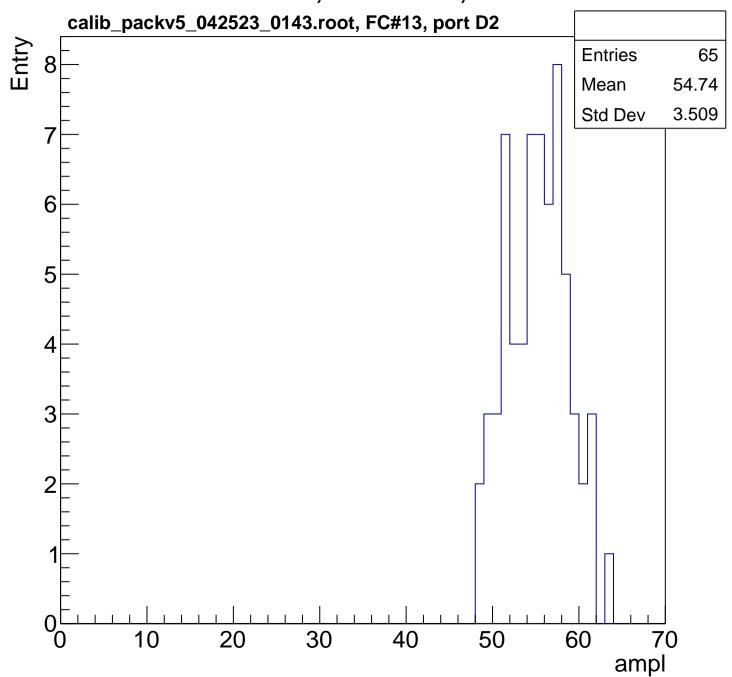
B1L003S, U2-ch84, adc7 calib_packv5_042523_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

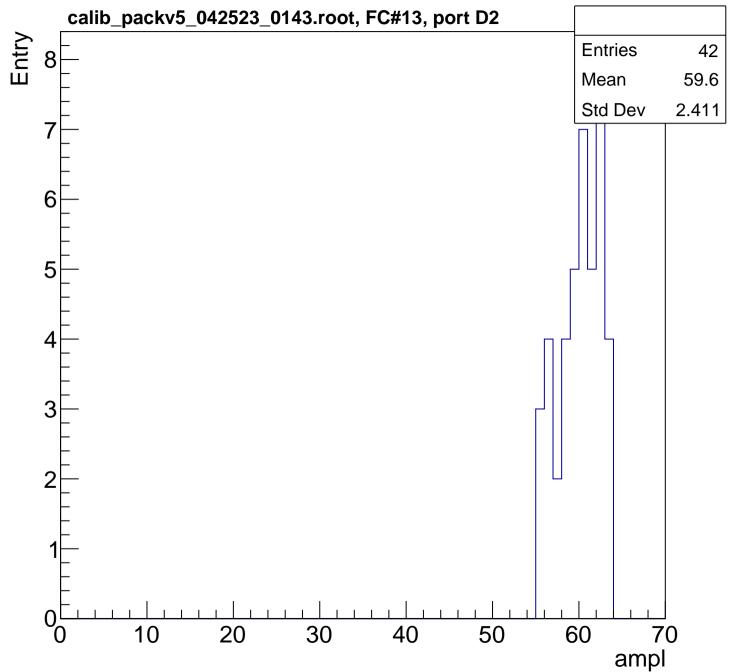


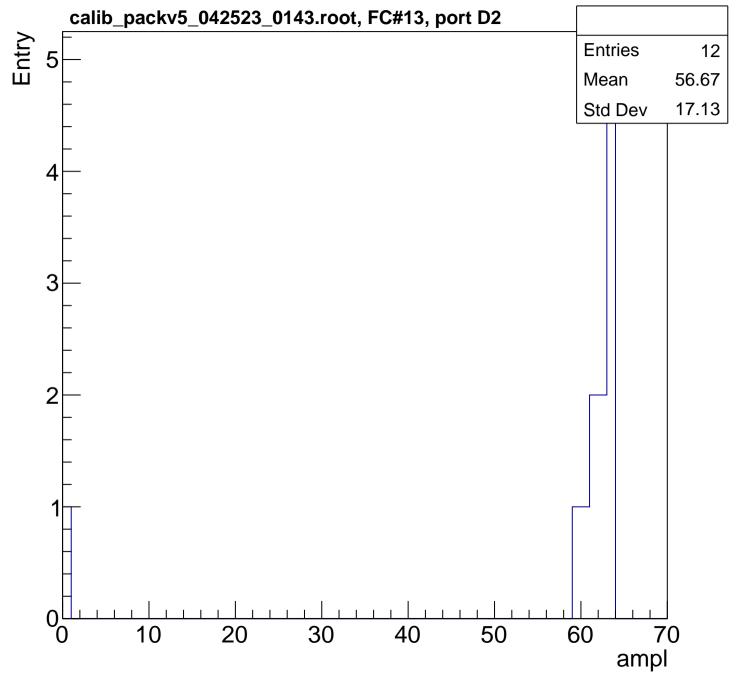




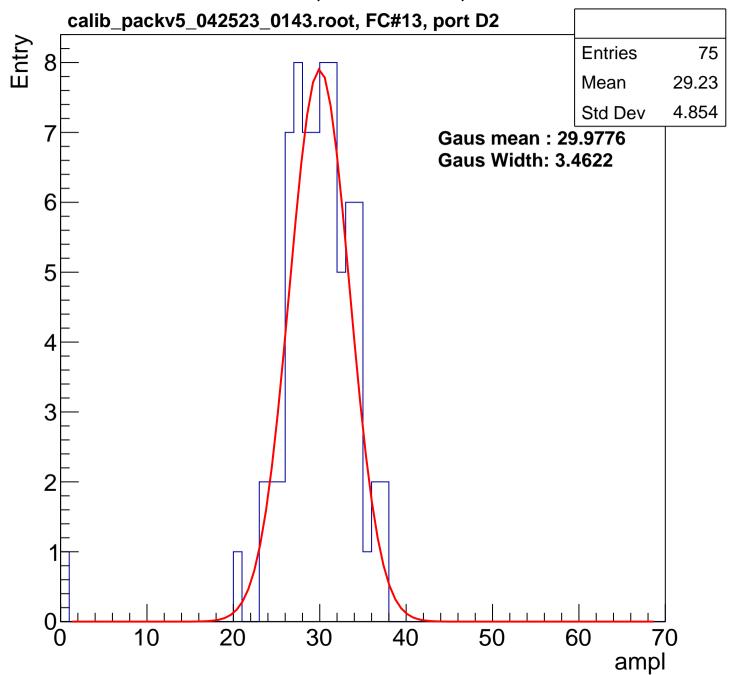


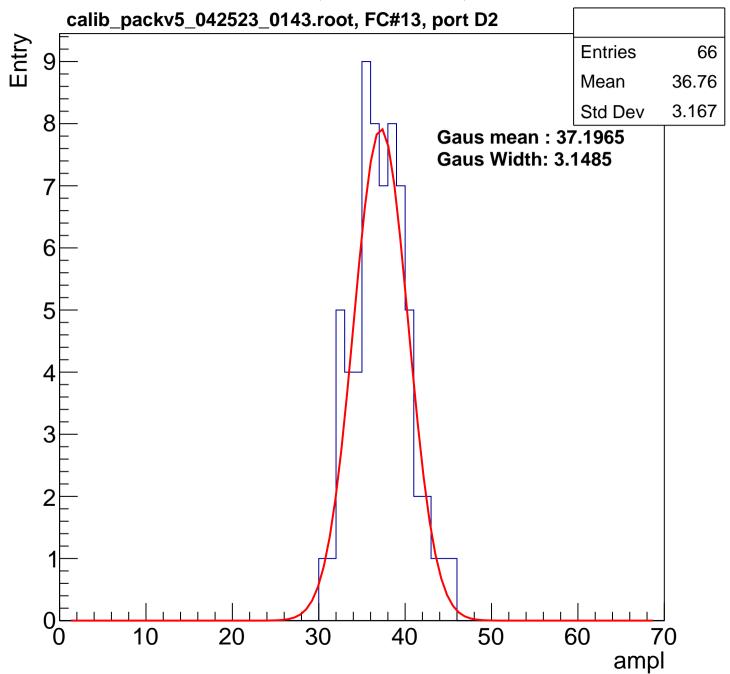


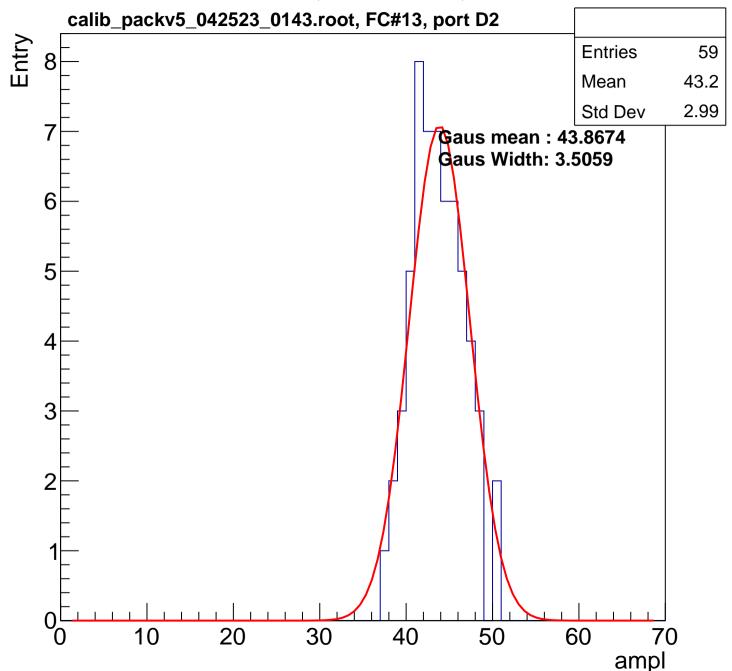


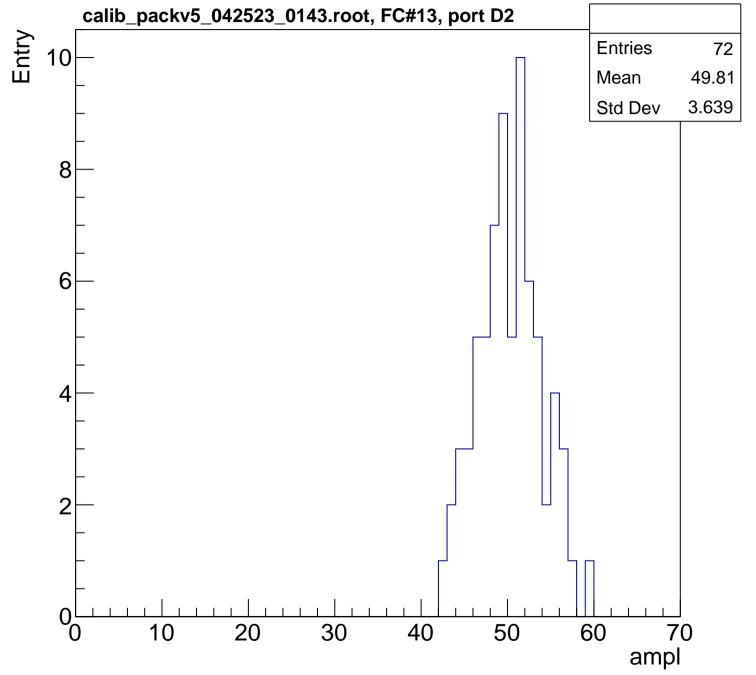


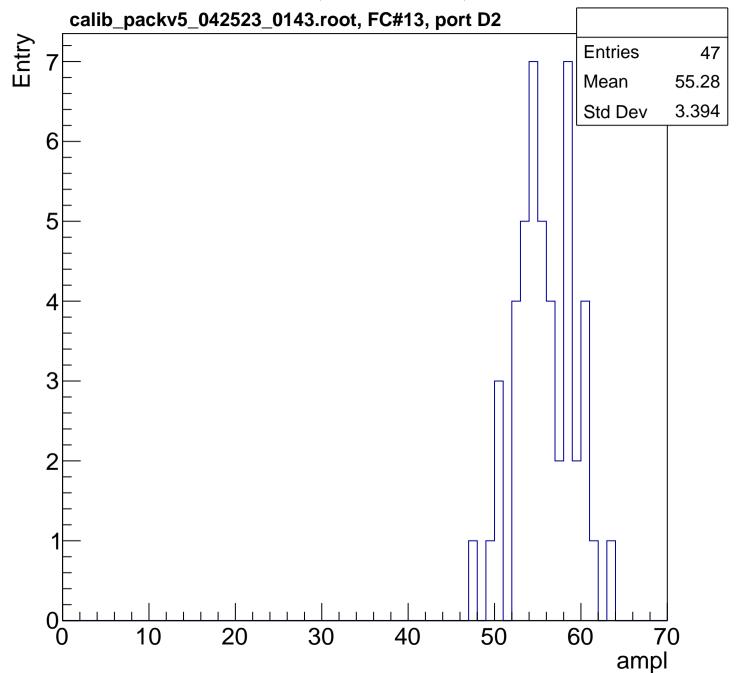
B1L003S, U2-ch85, adc7 calib_packv5_042523_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

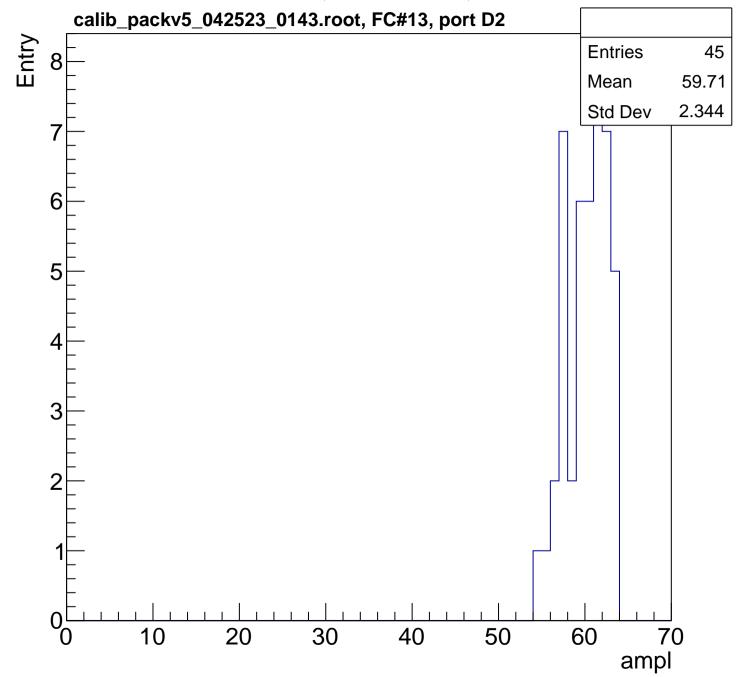


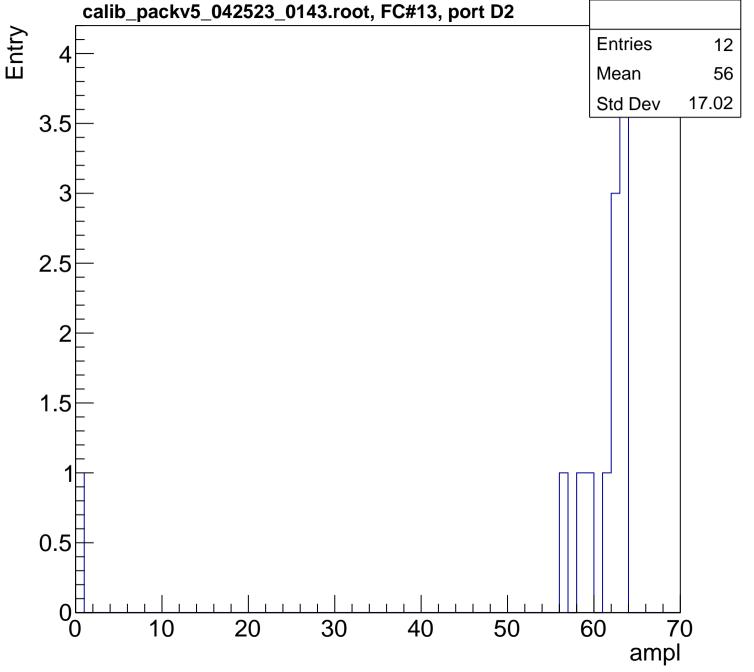




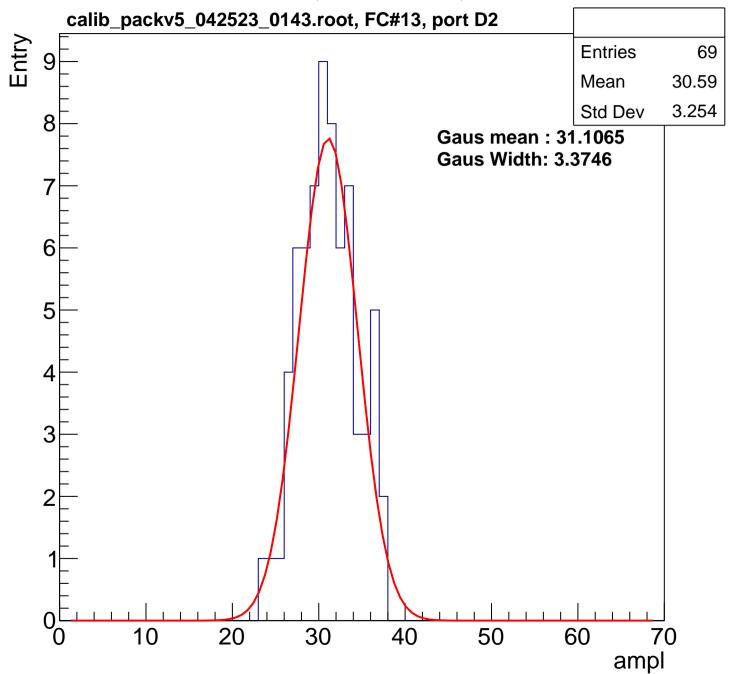


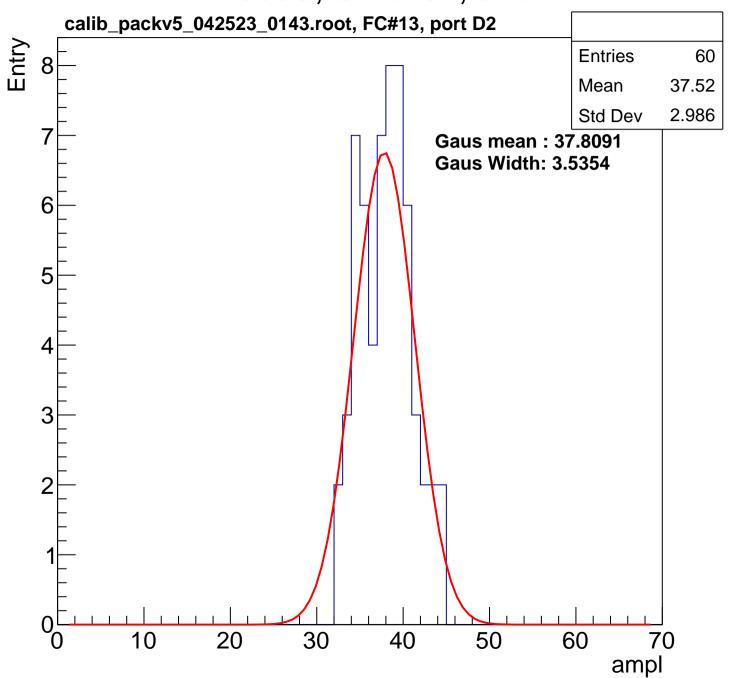


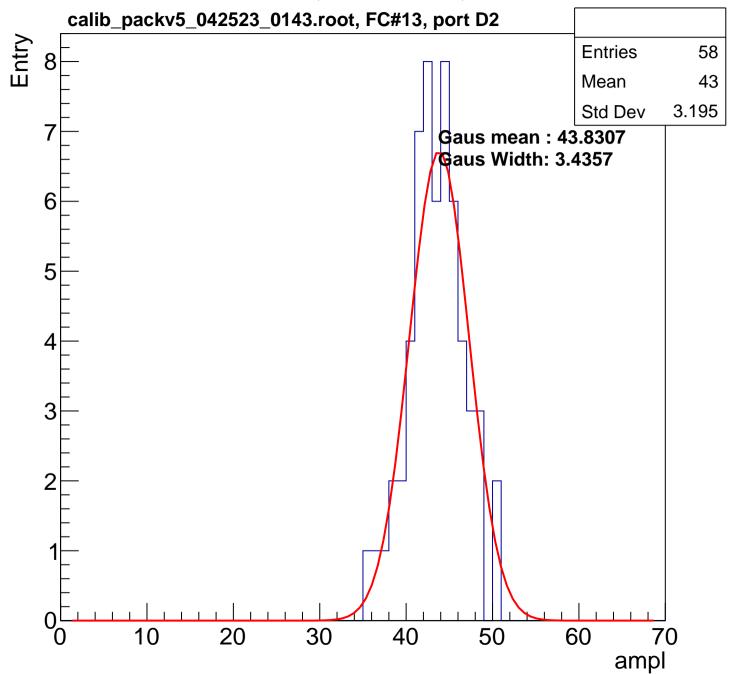


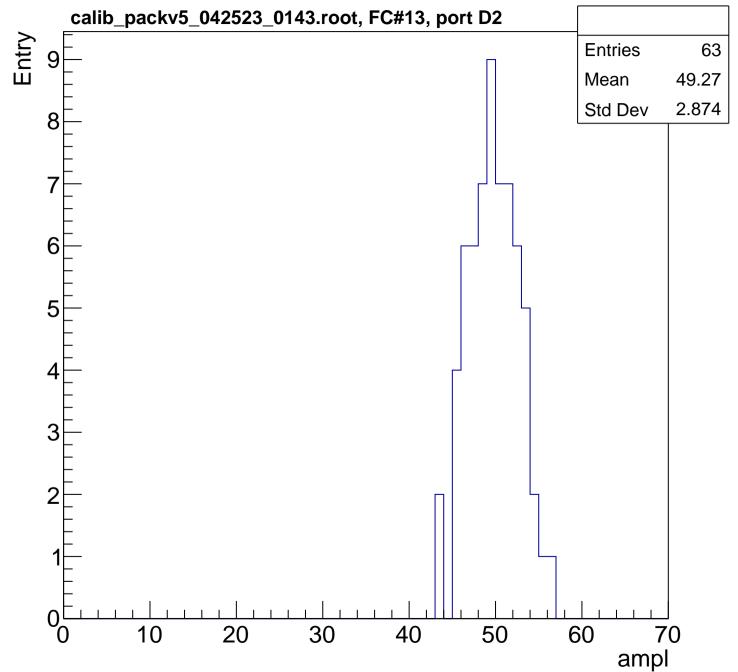


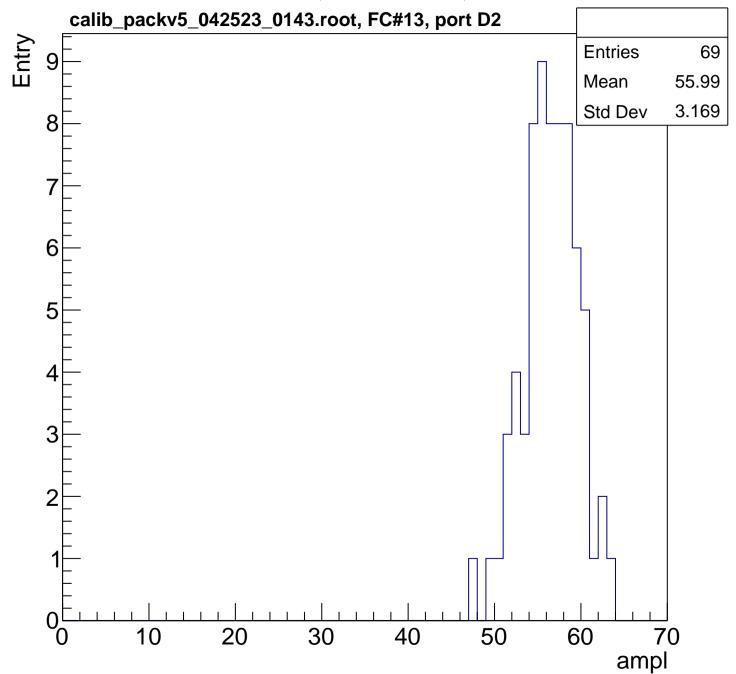
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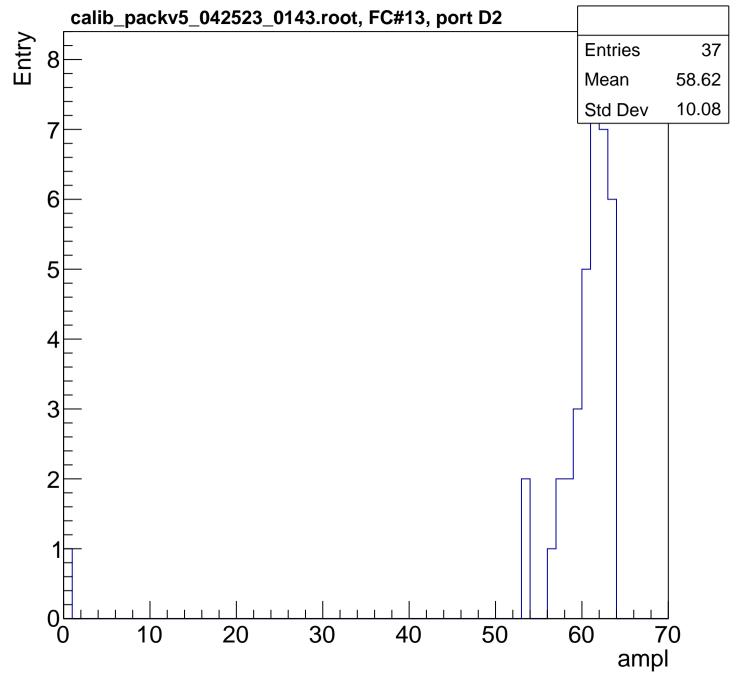


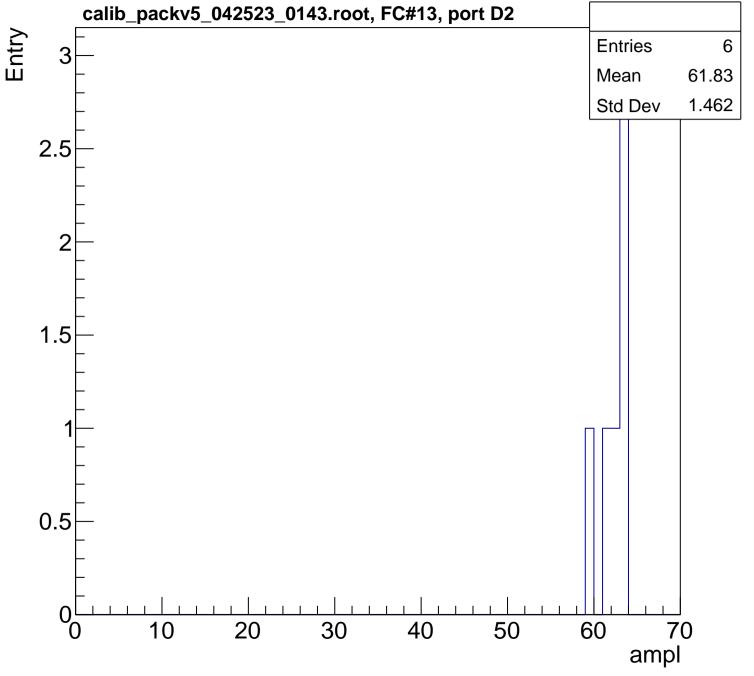


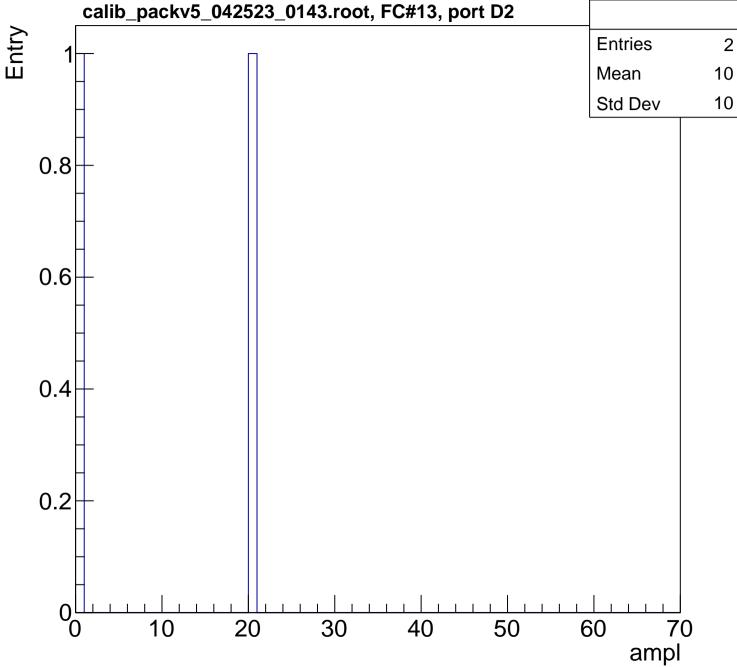


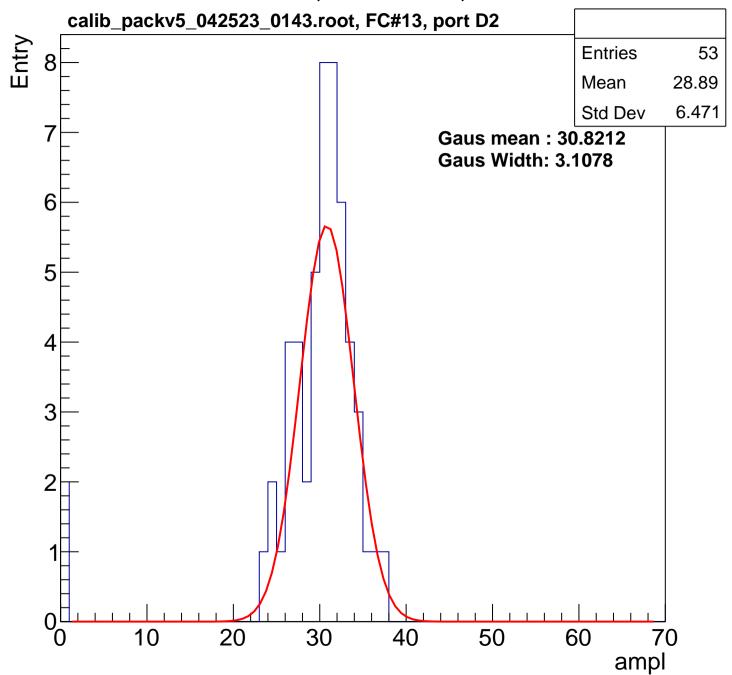


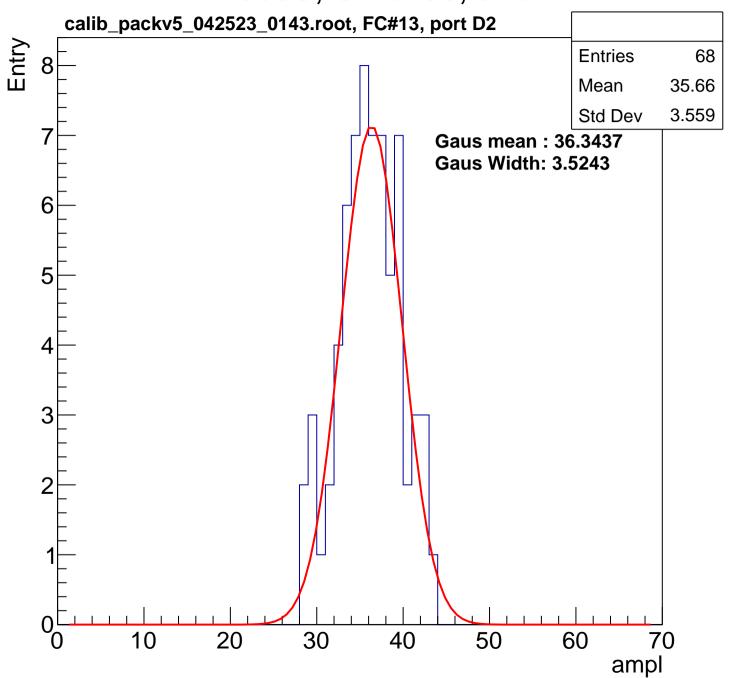


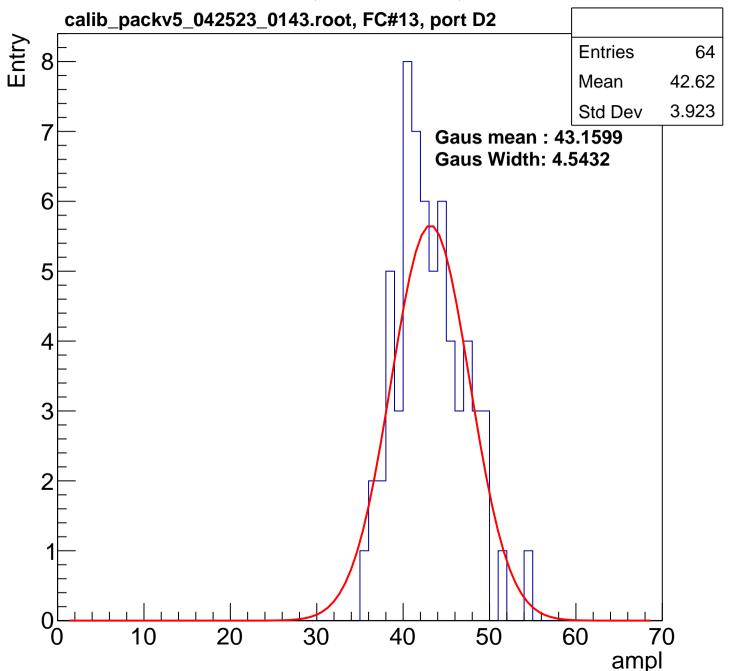


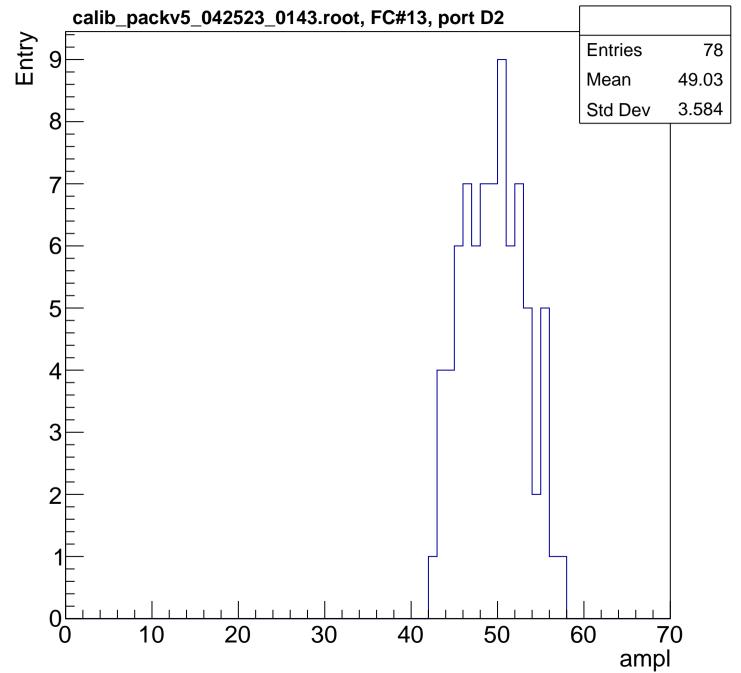


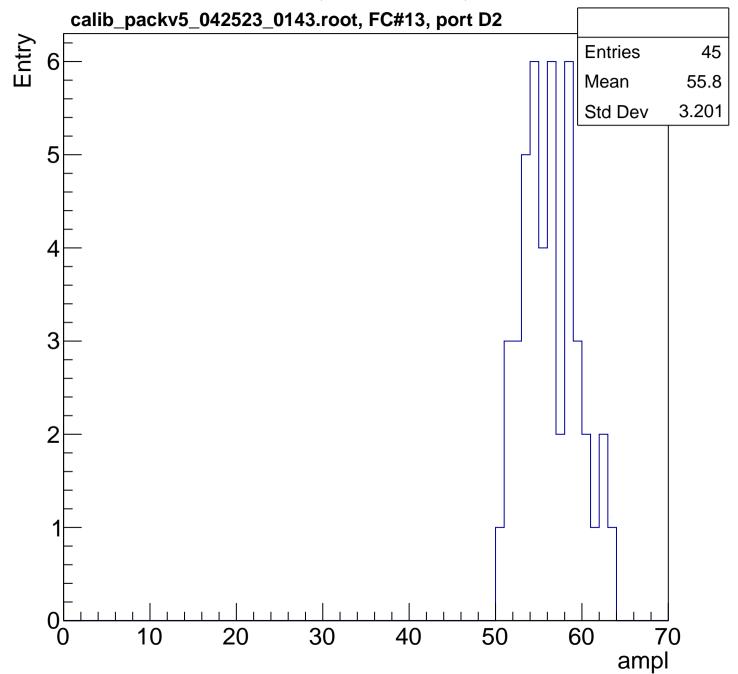


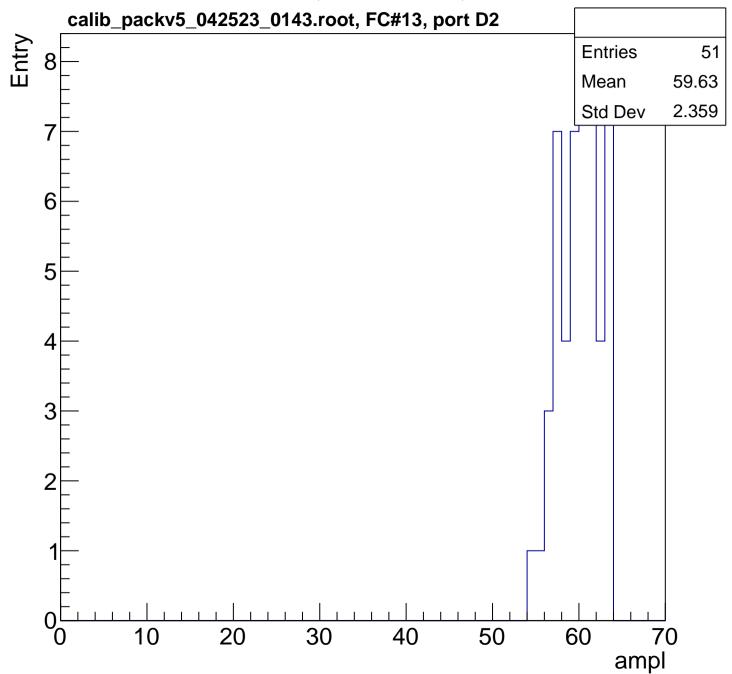


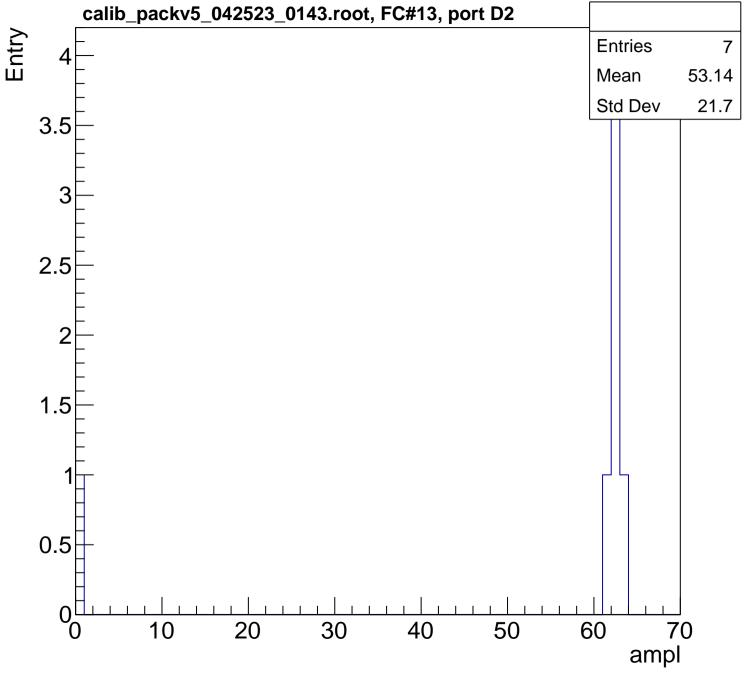




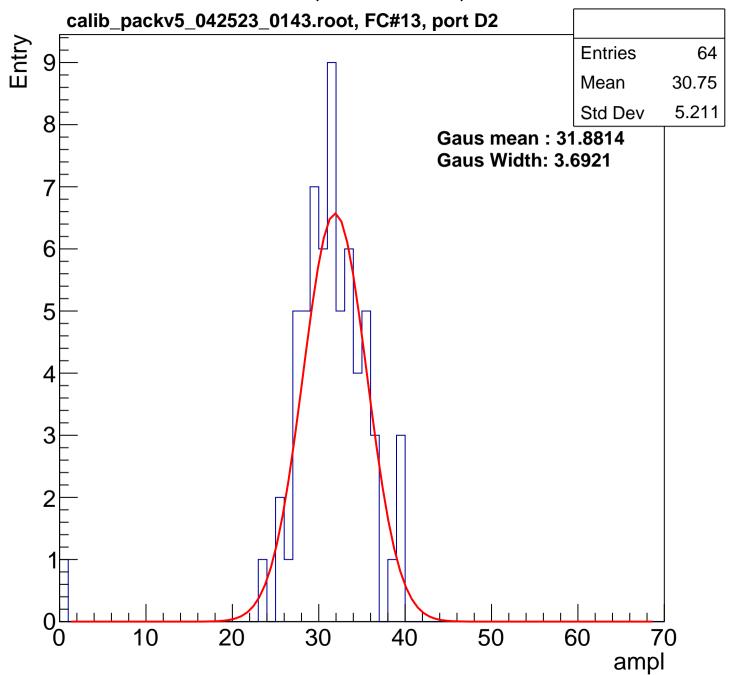


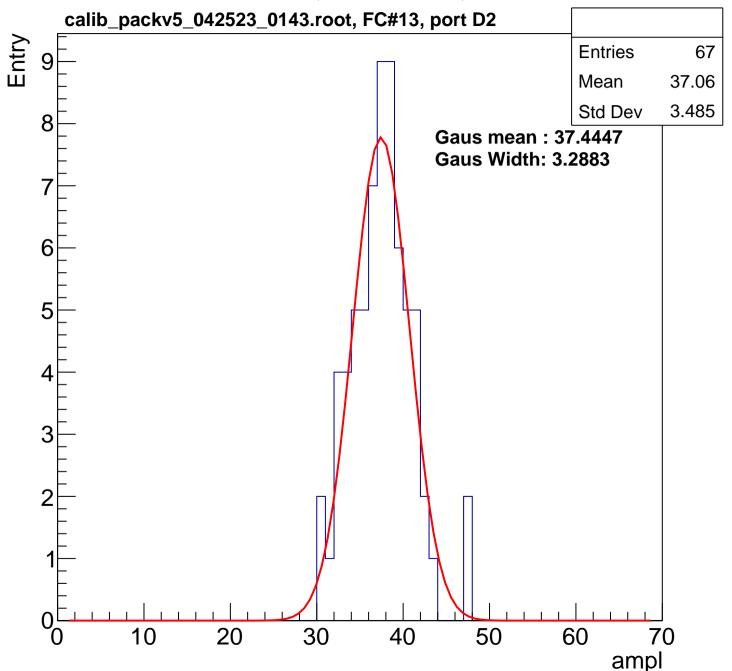


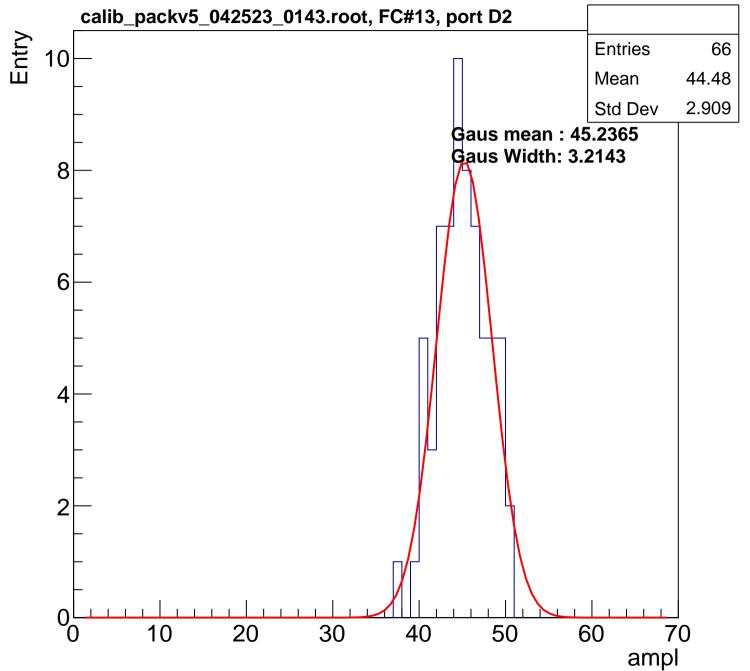


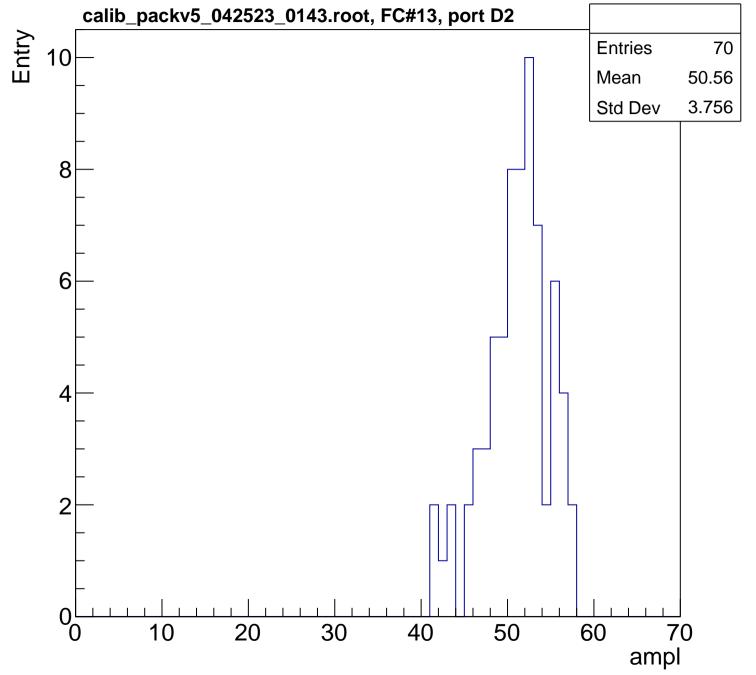


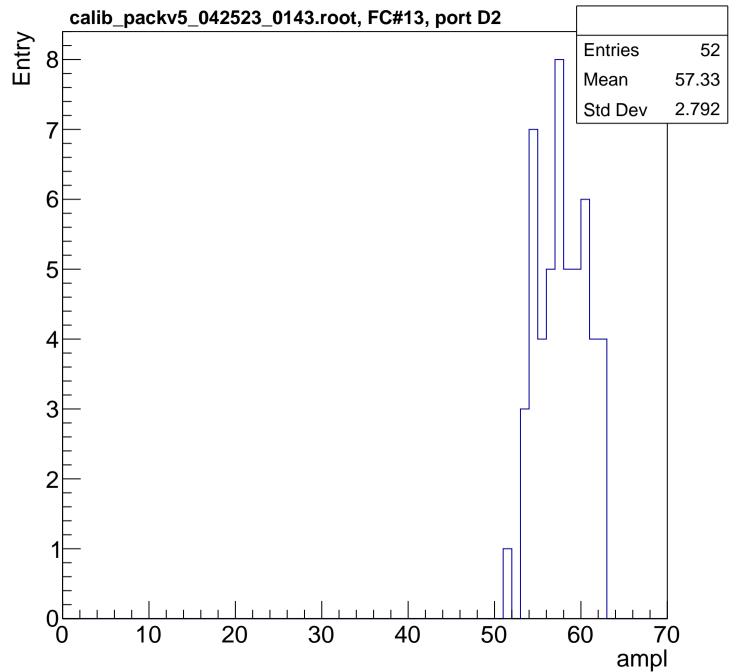
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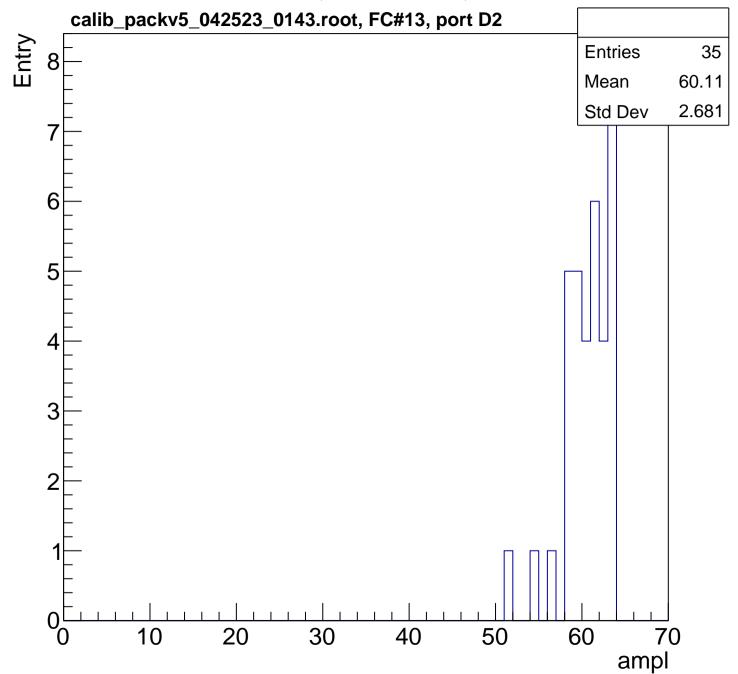


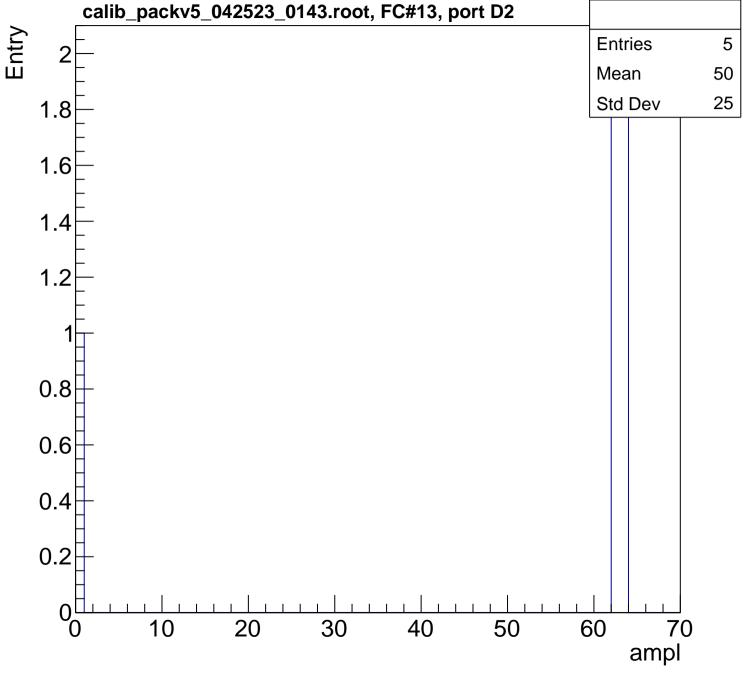


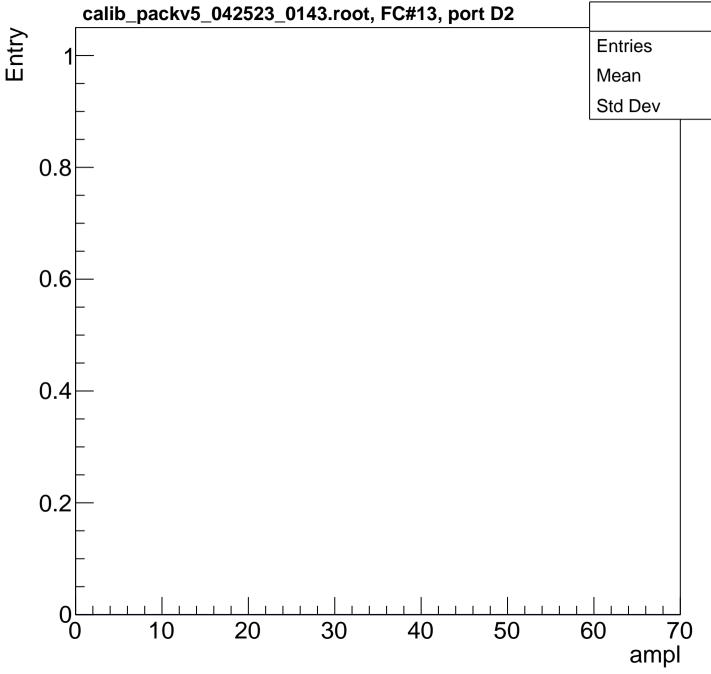


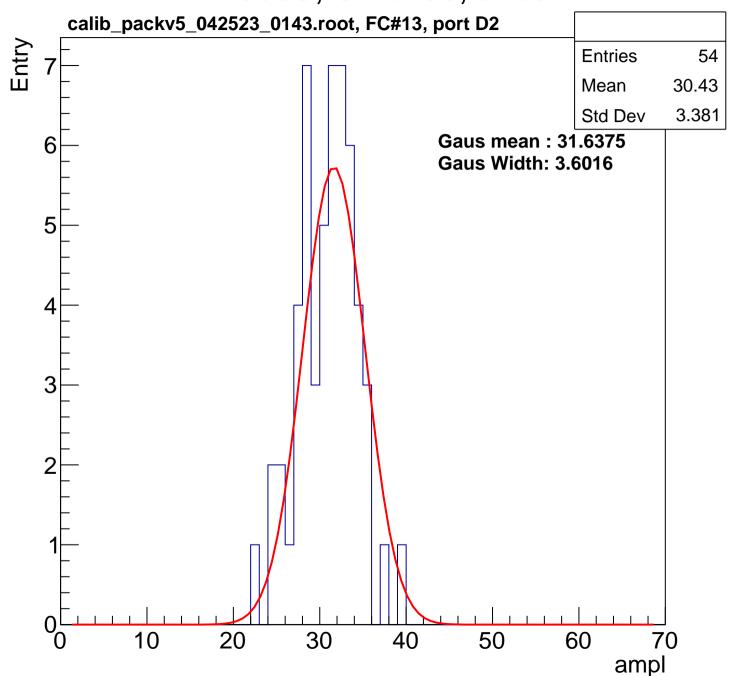


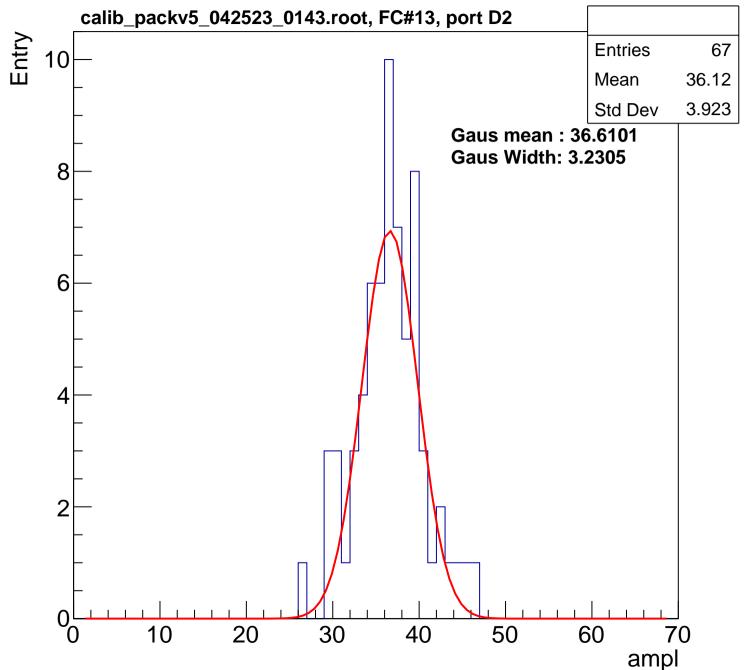


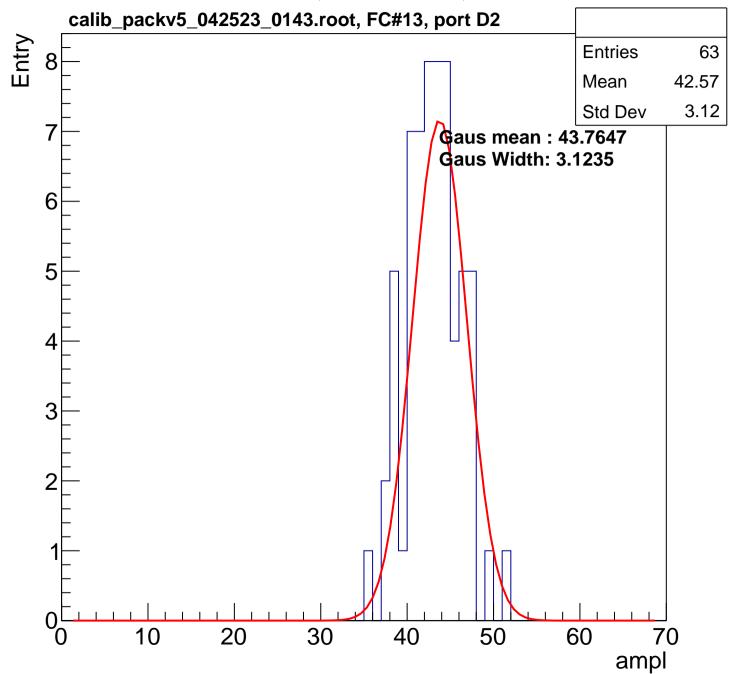


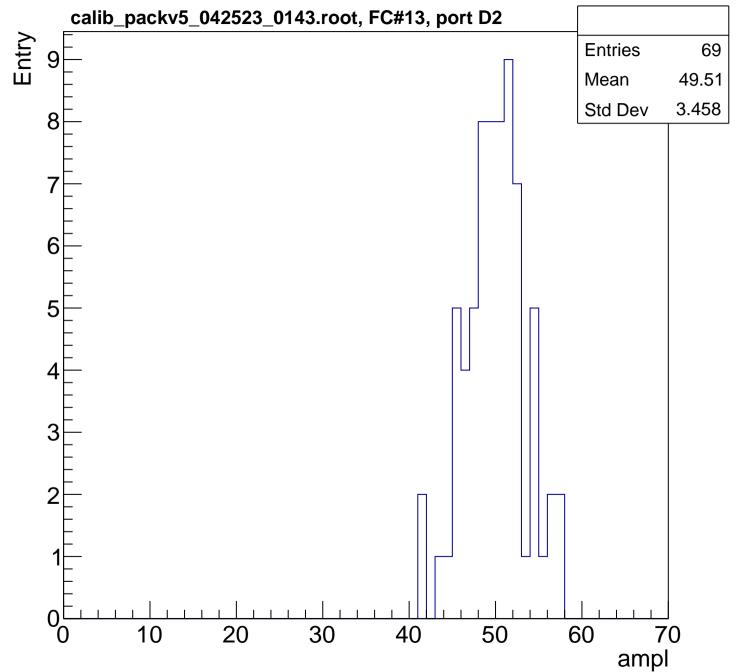


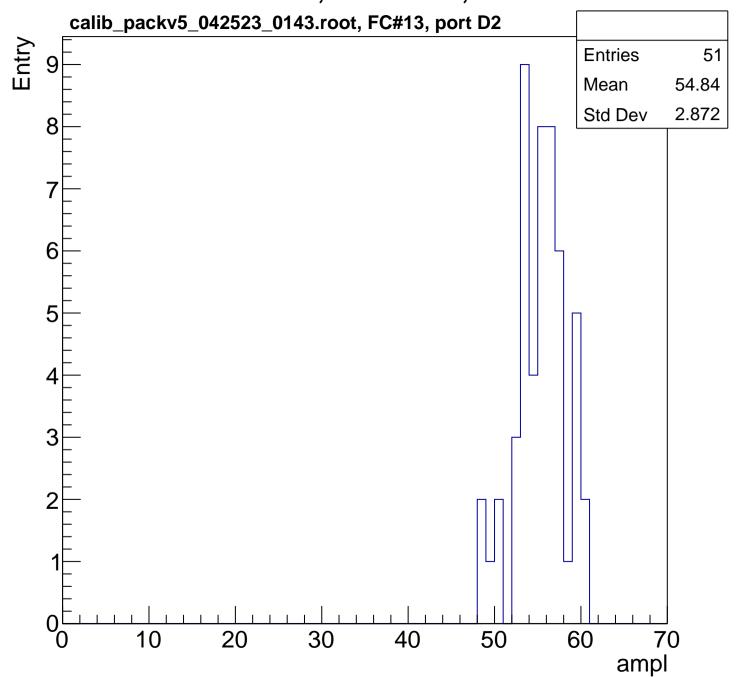


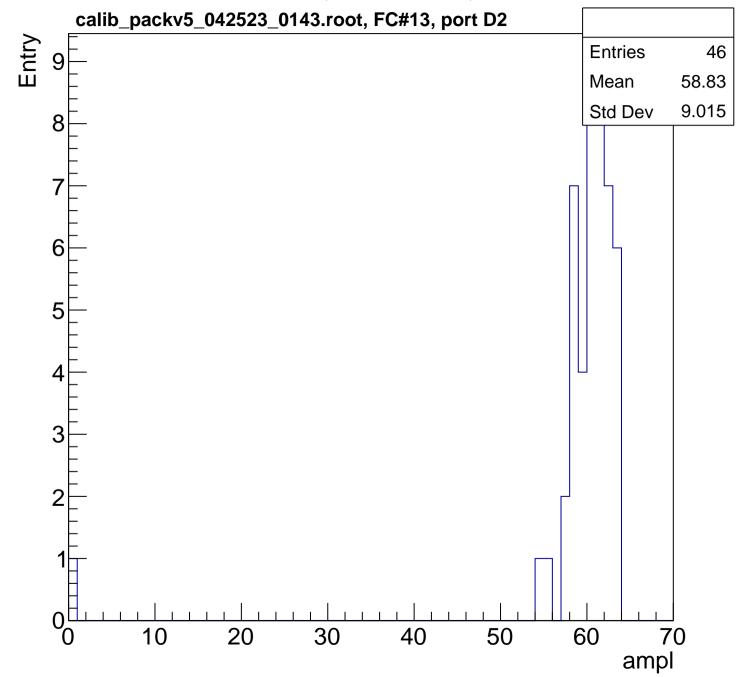


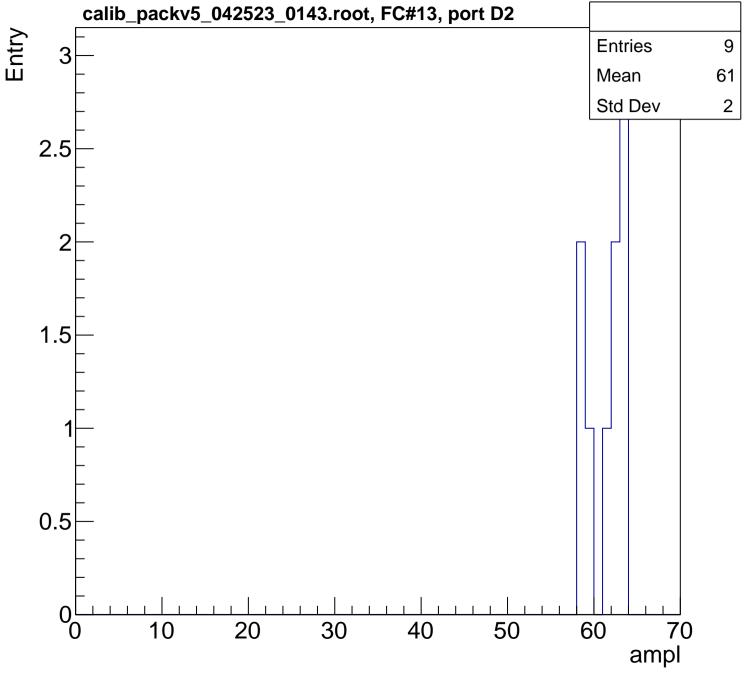


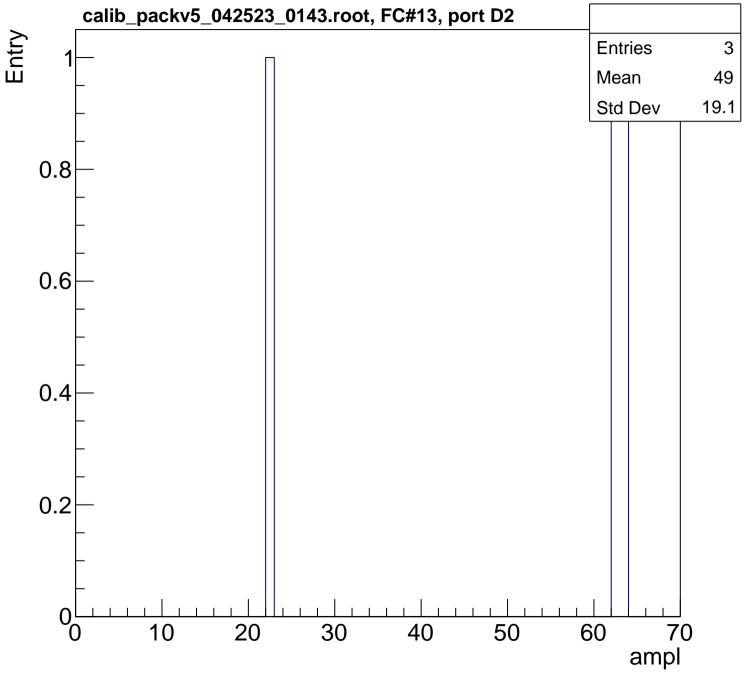


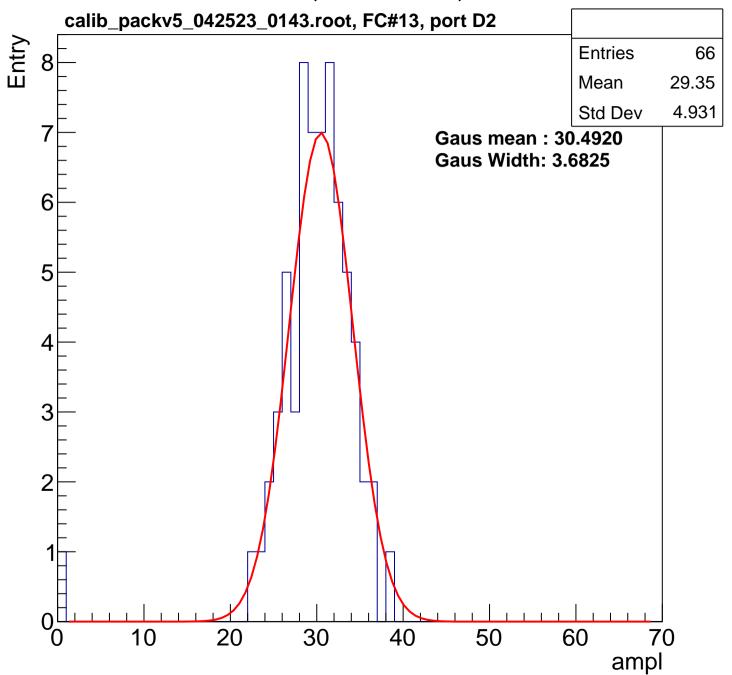


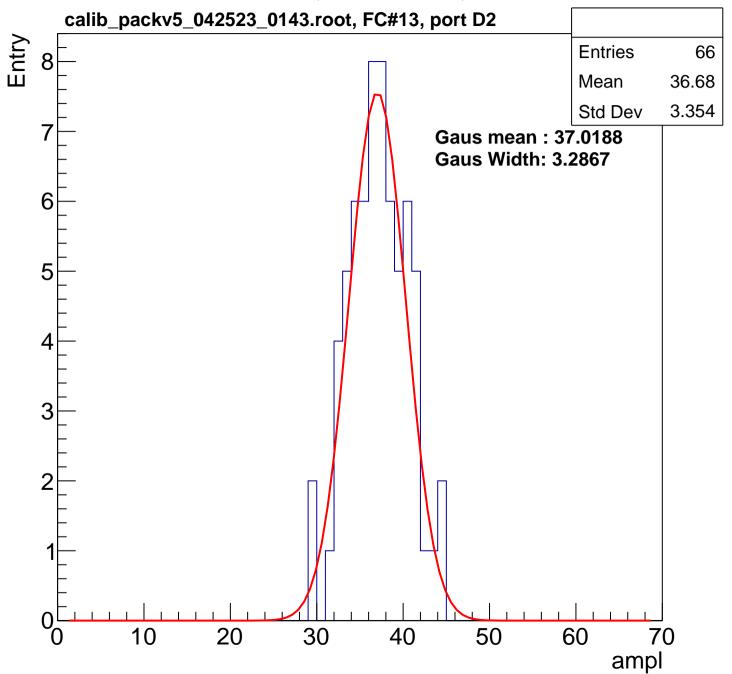


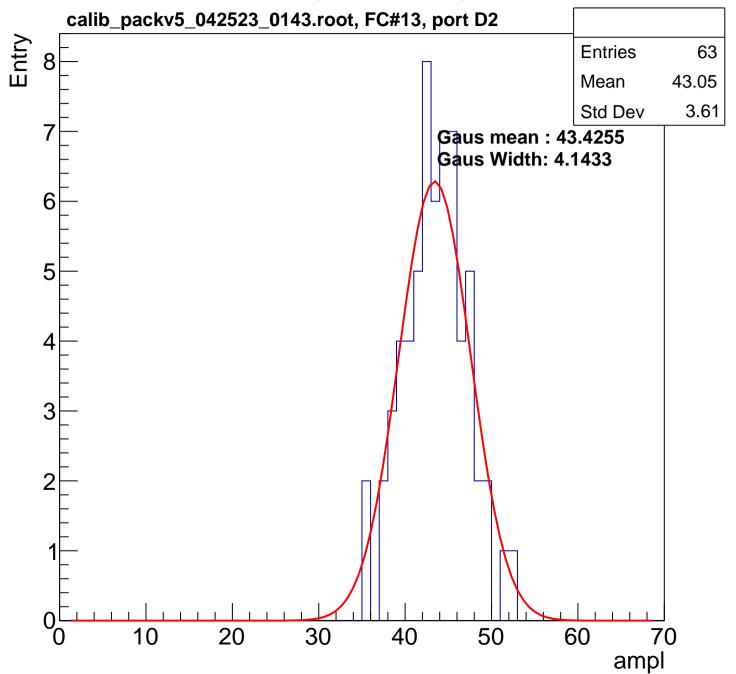


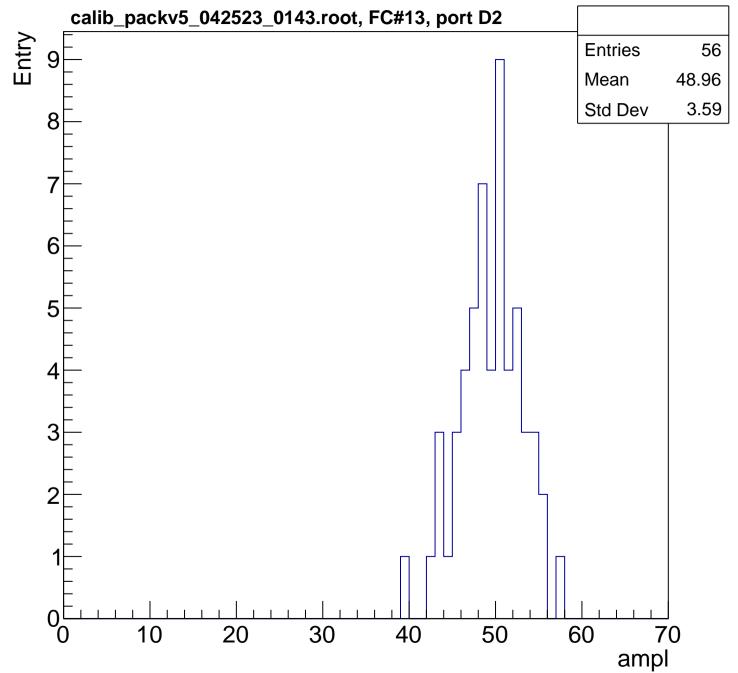


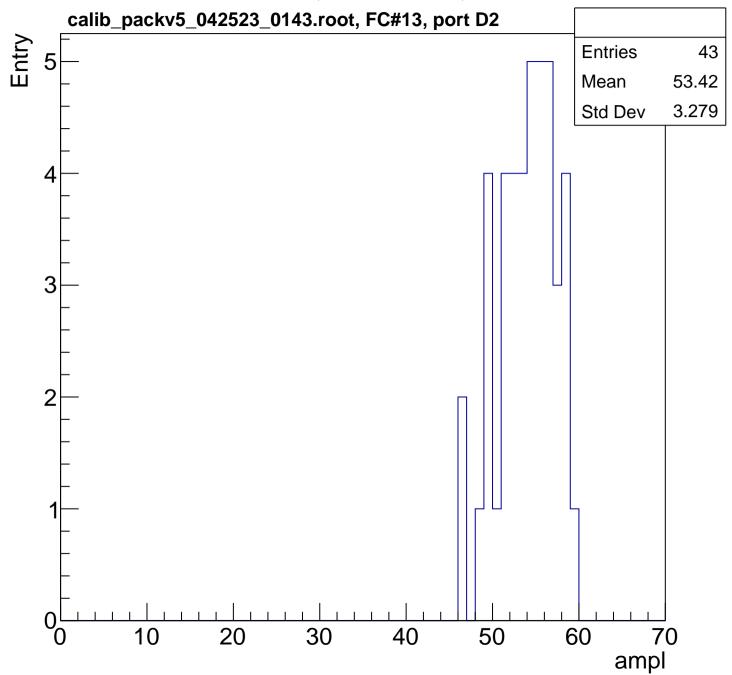


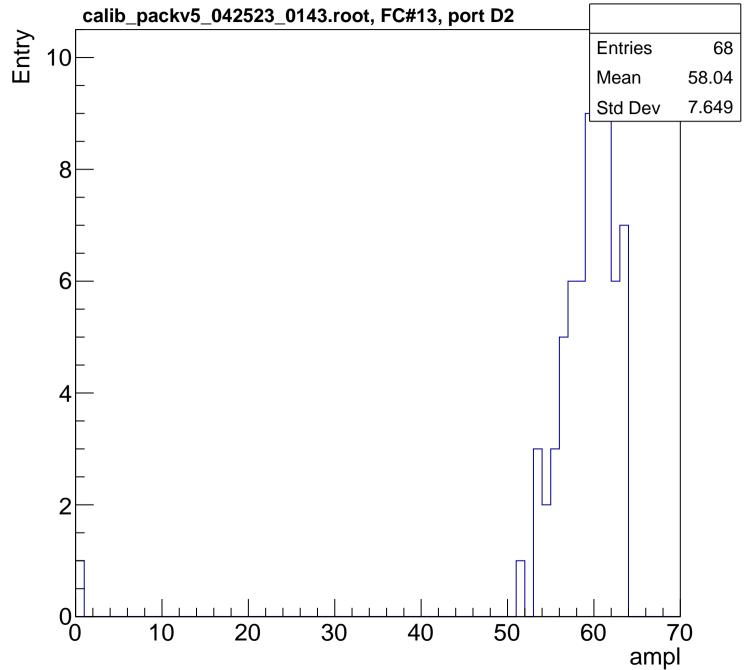


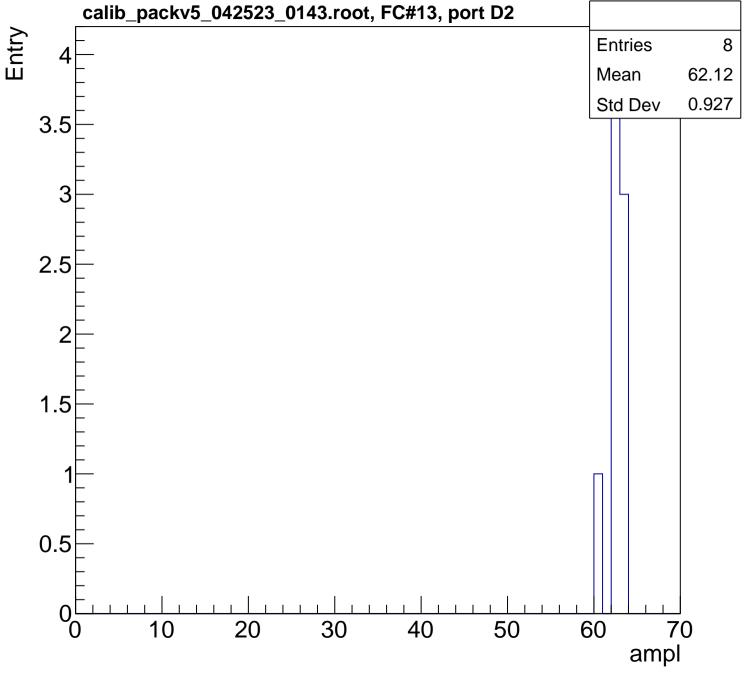




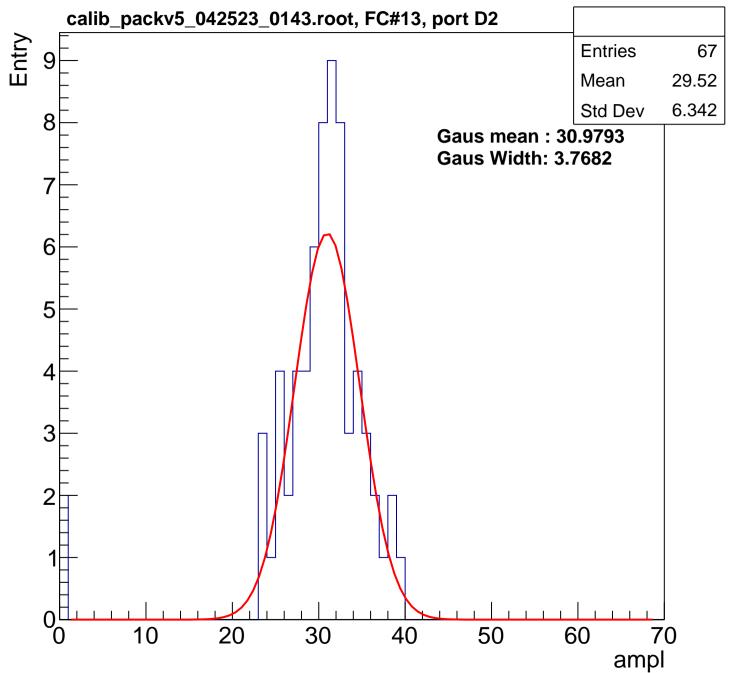


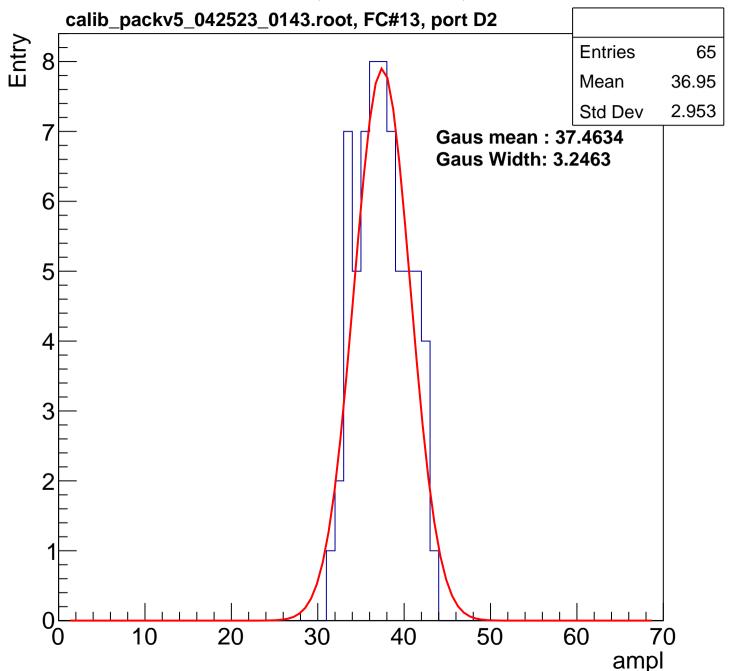


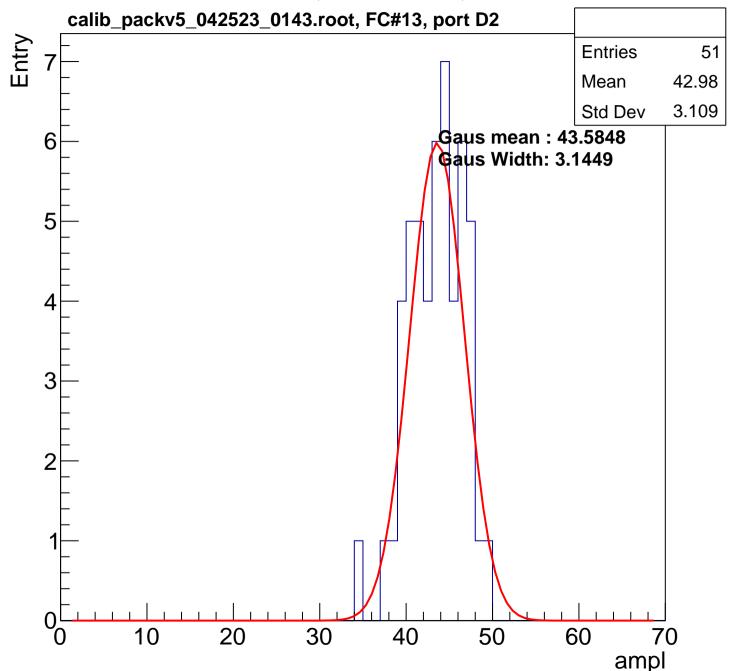


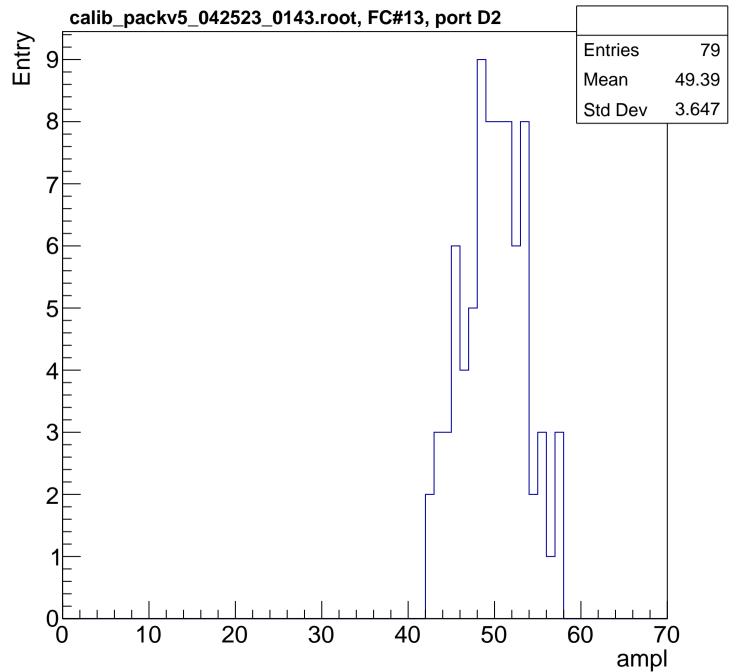


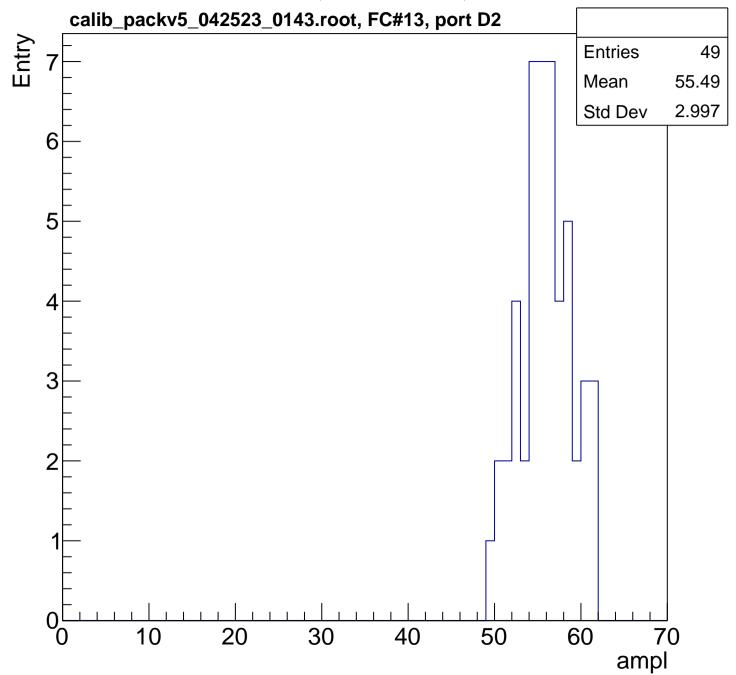
B1L003S, U2-ch91, adc7 calib_packv5_042523_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

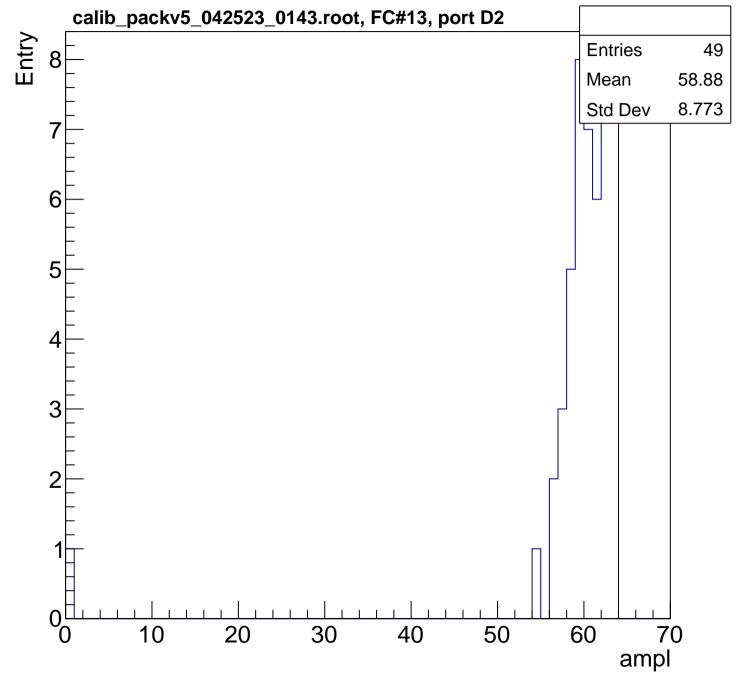


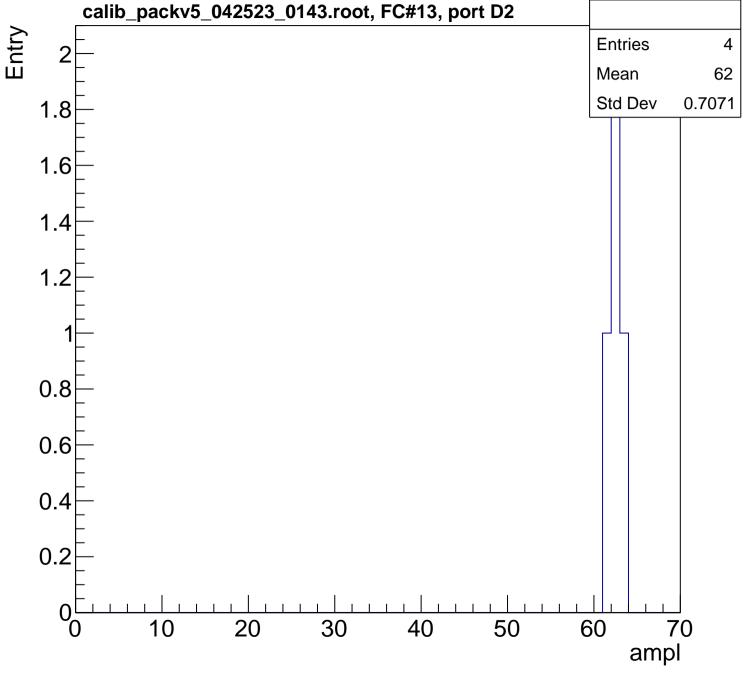


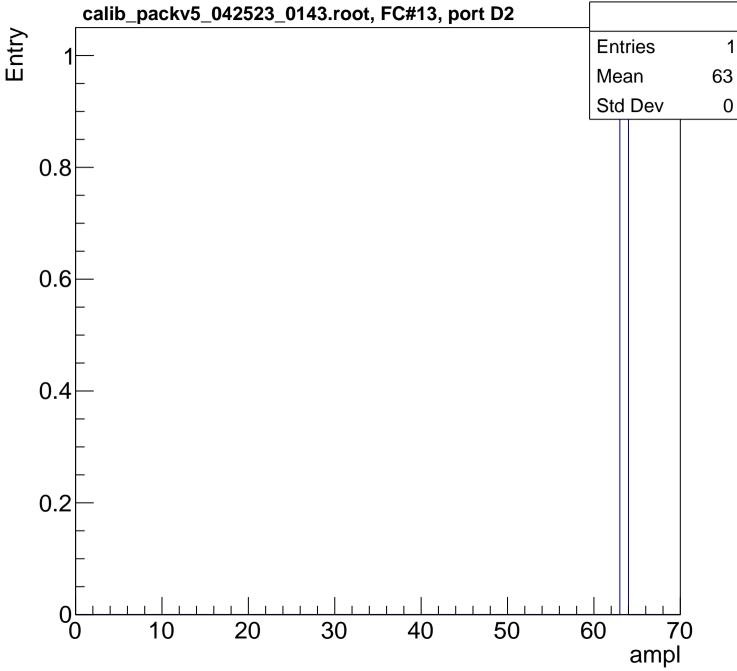


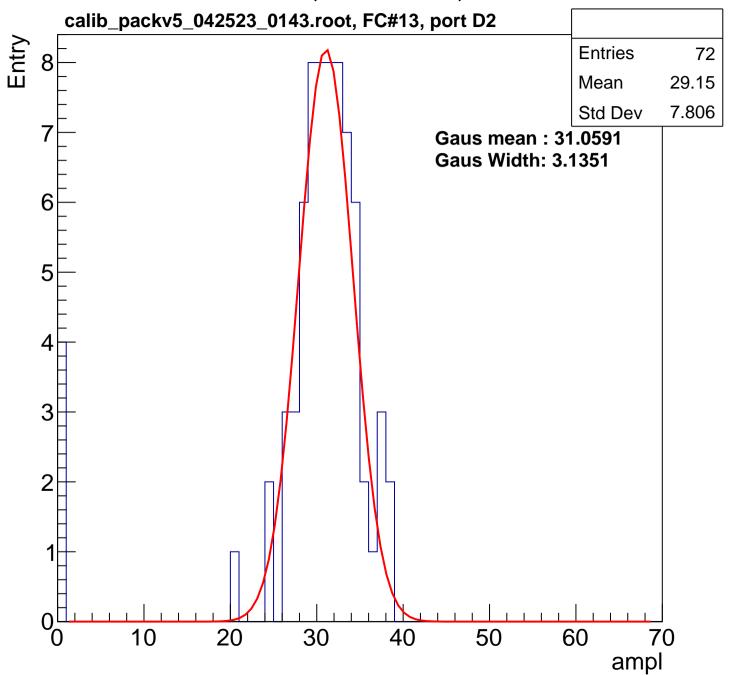


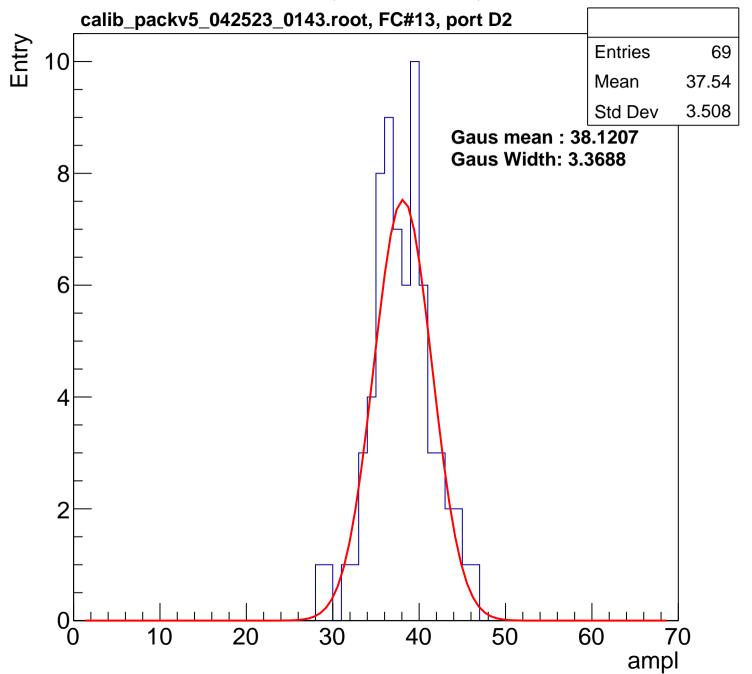


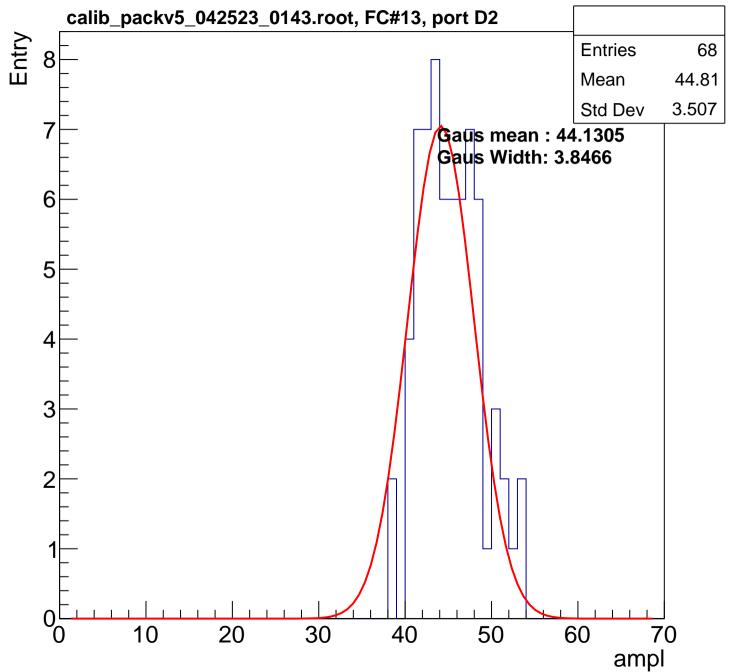


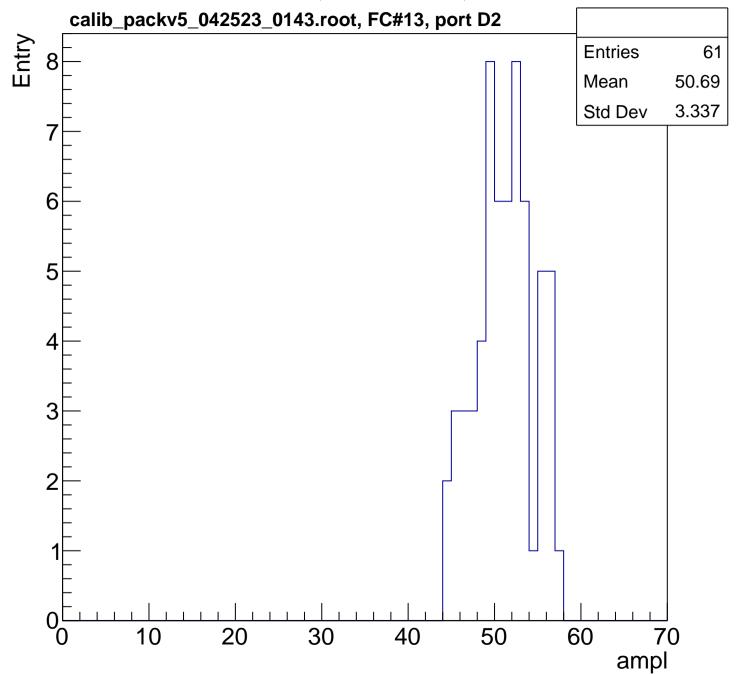


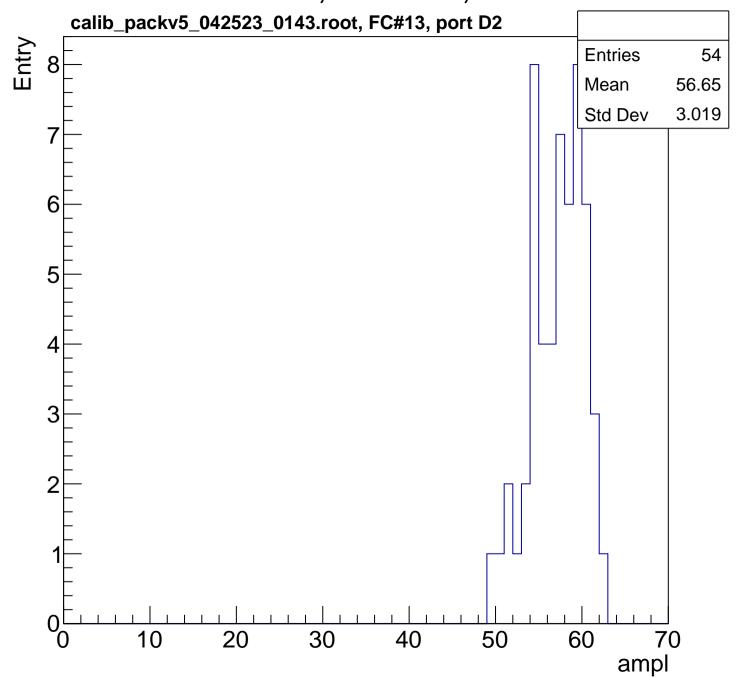


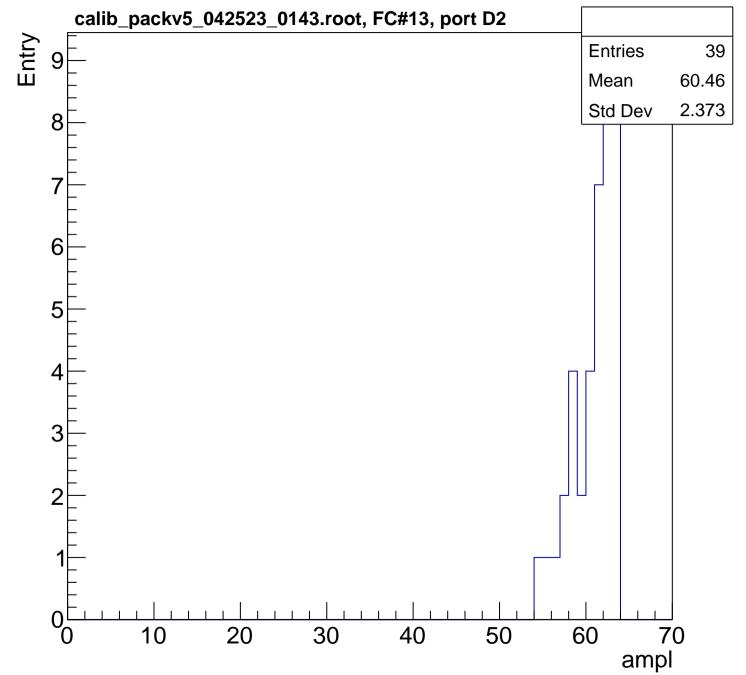


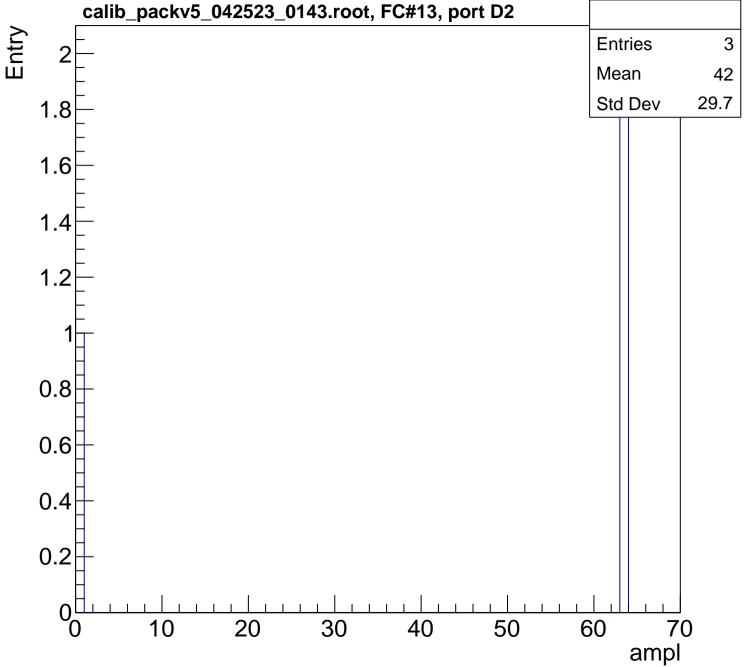




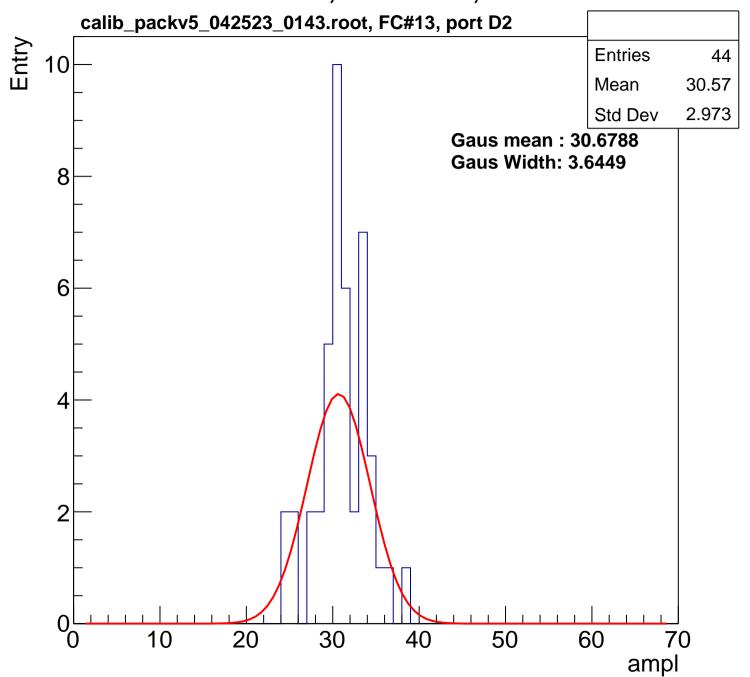


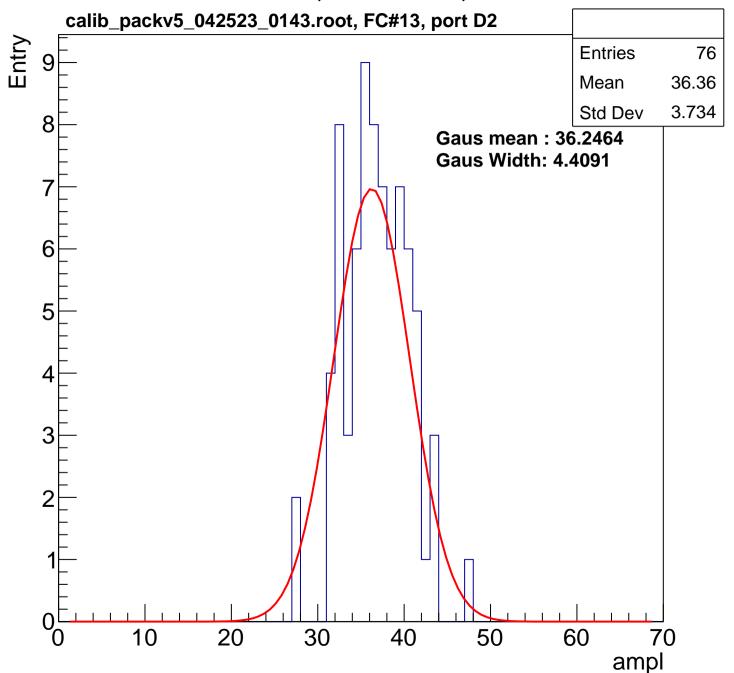


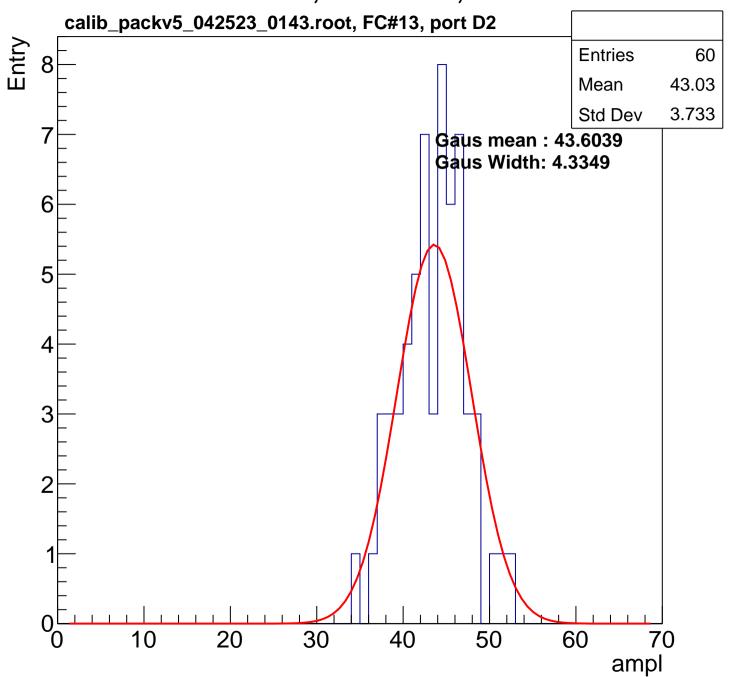


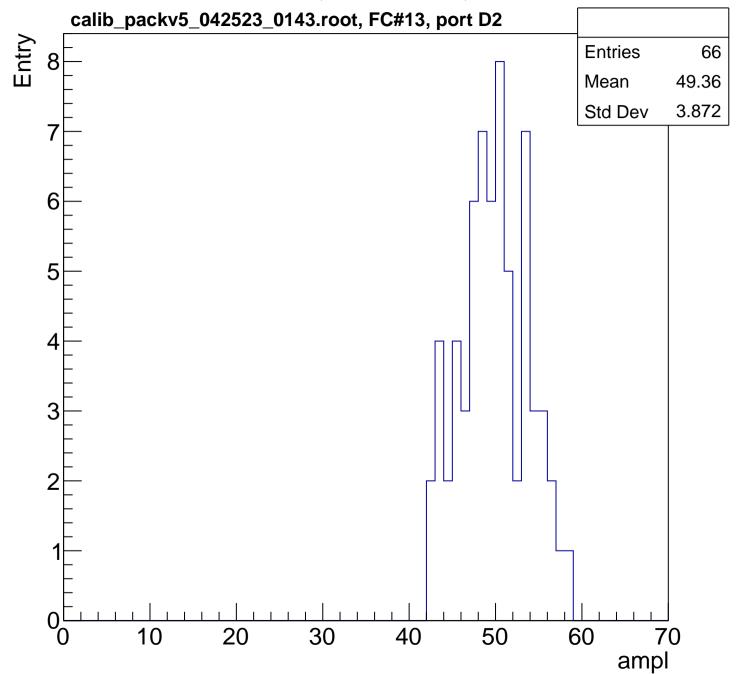


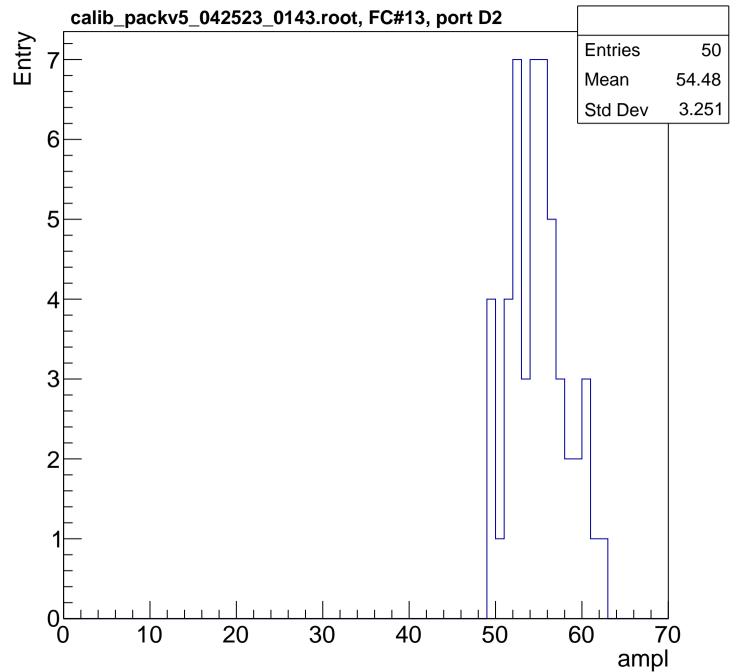
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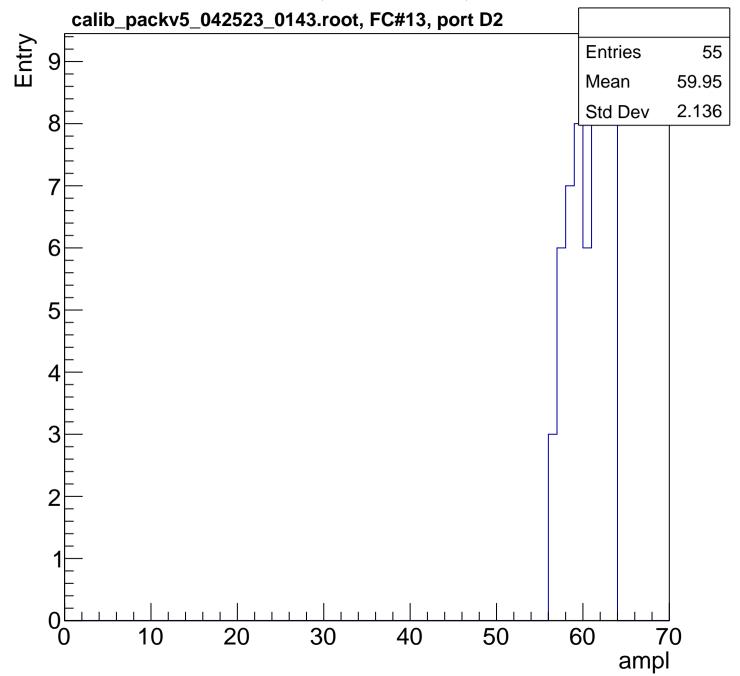


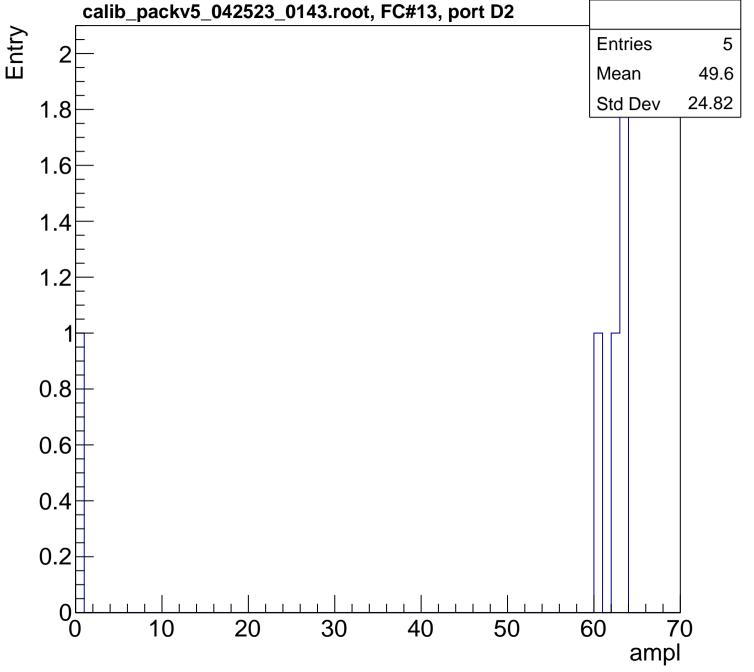




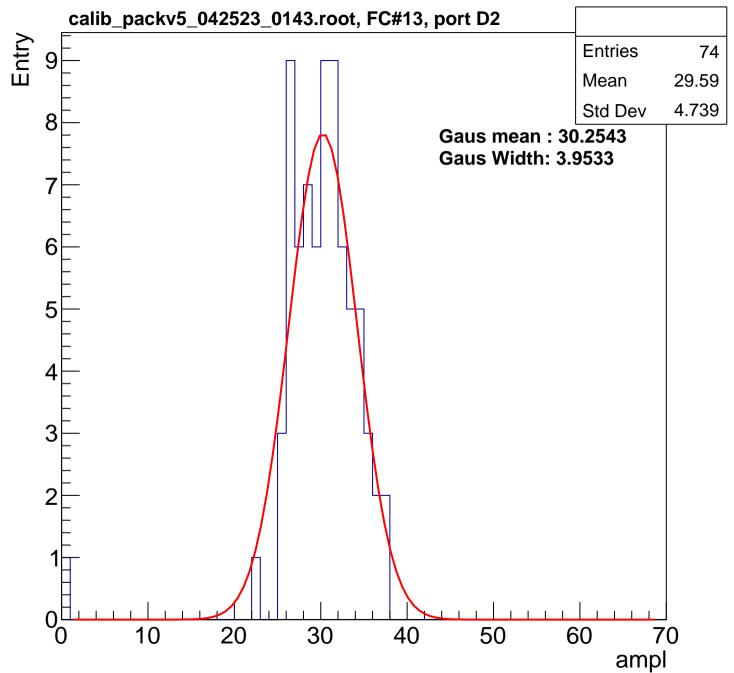


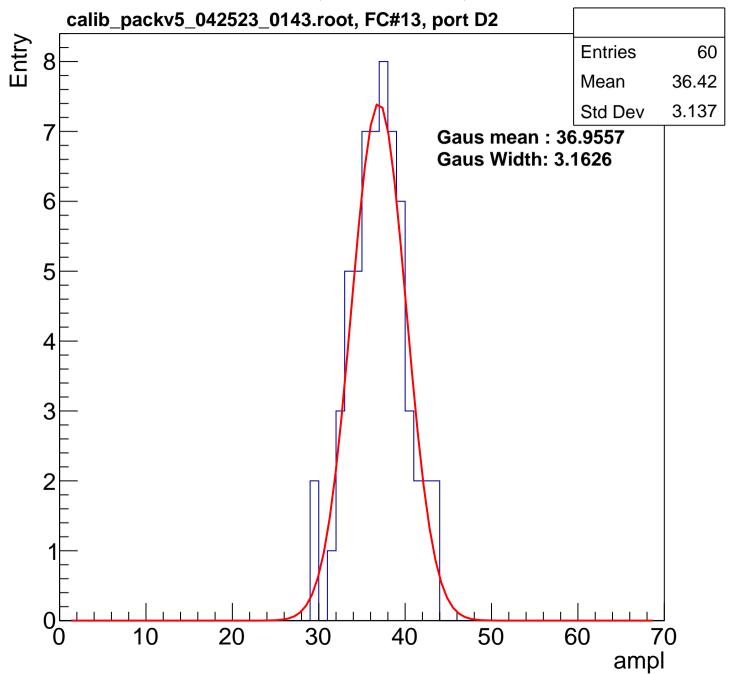


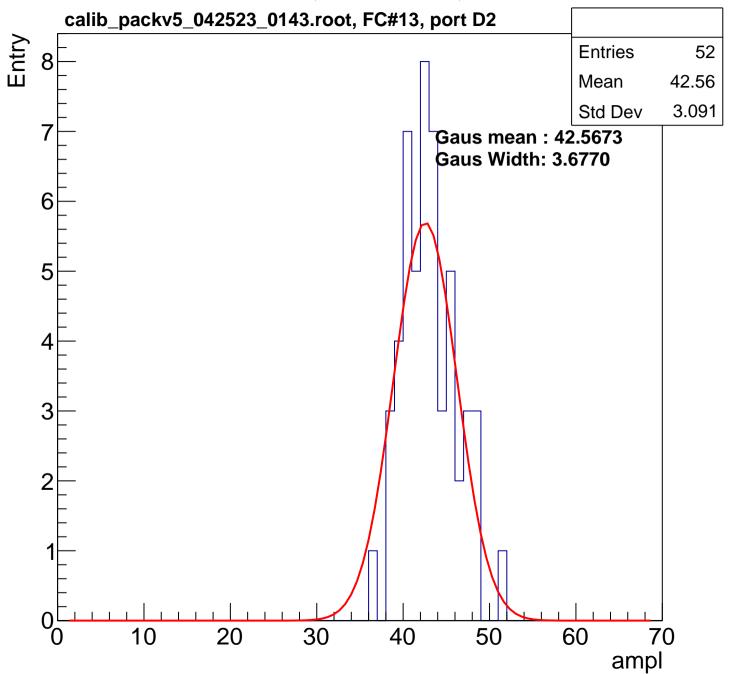


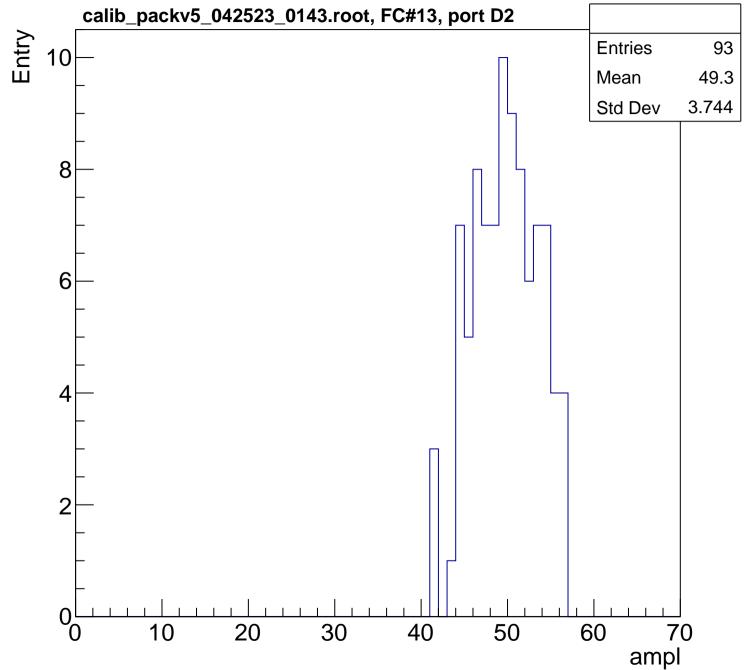


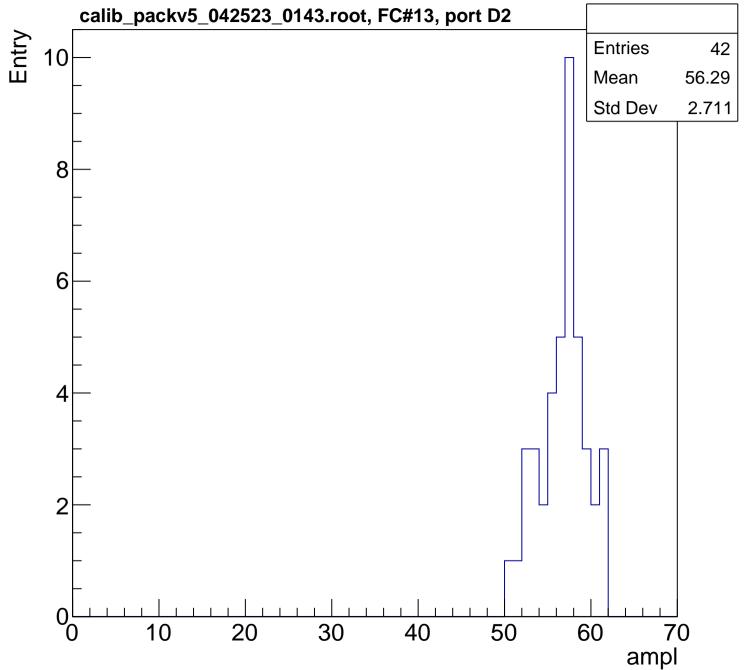
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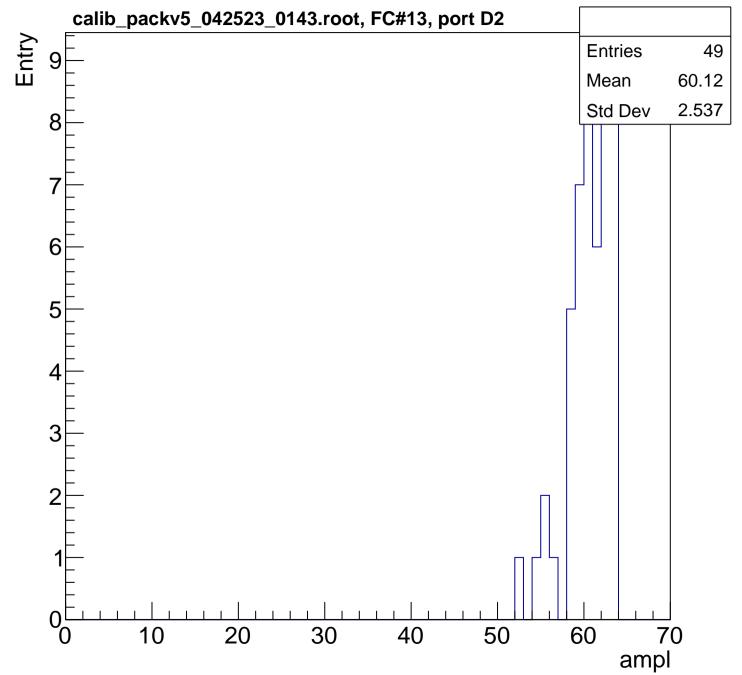


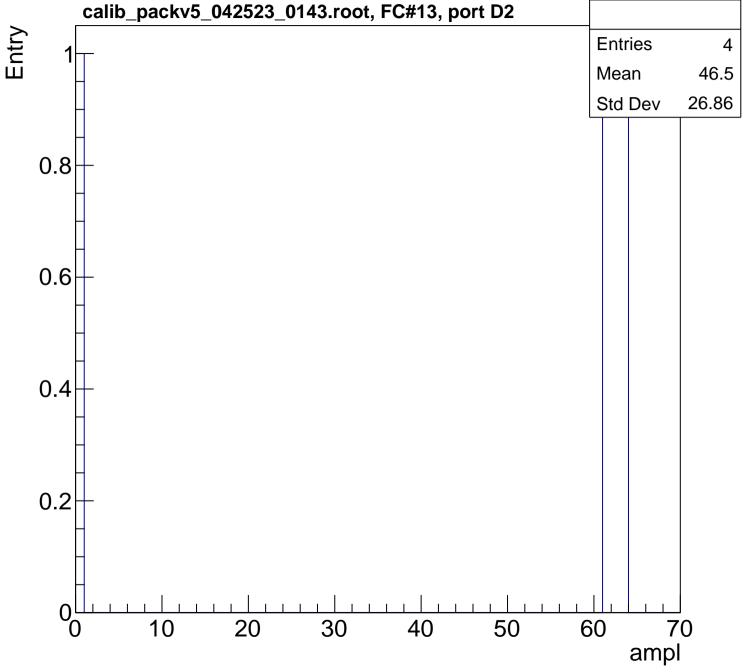




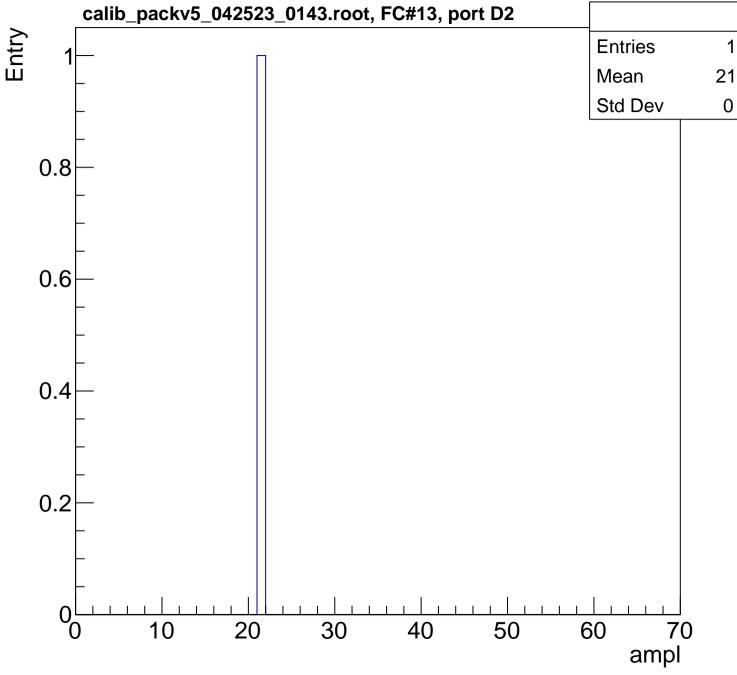


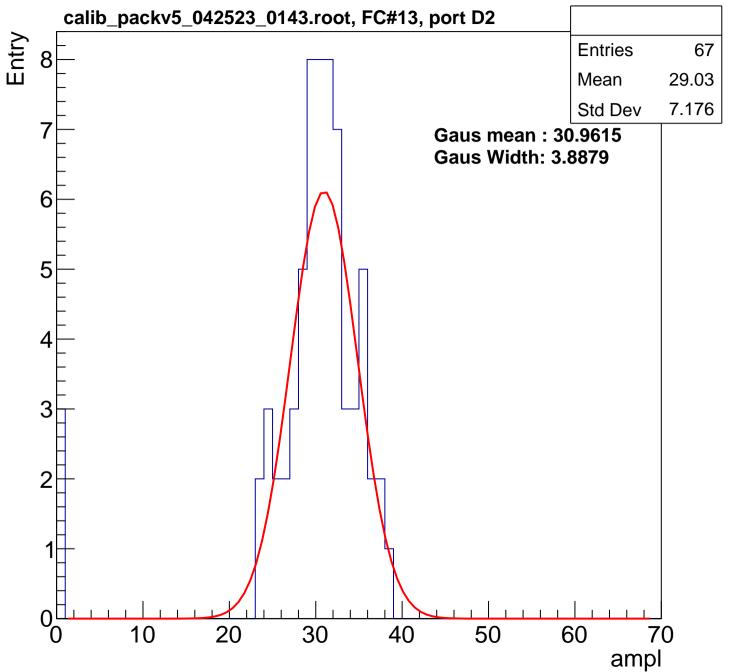


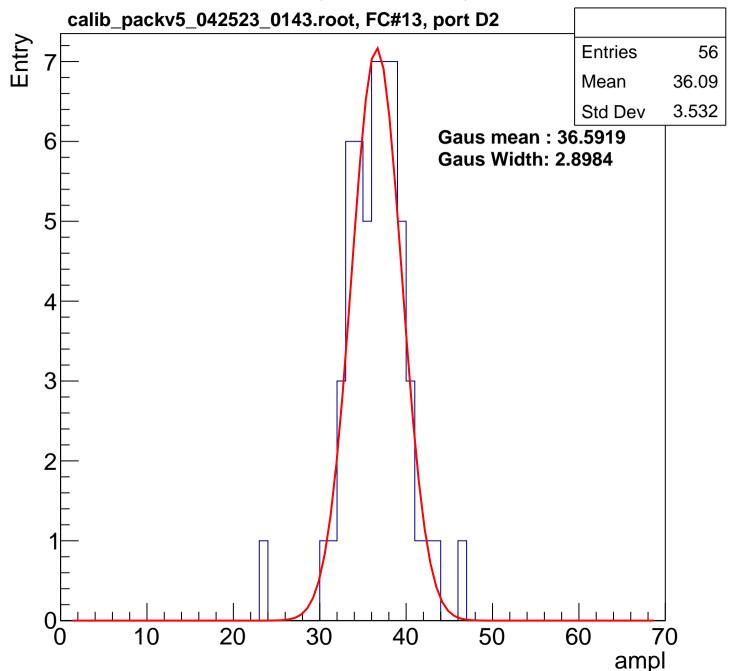


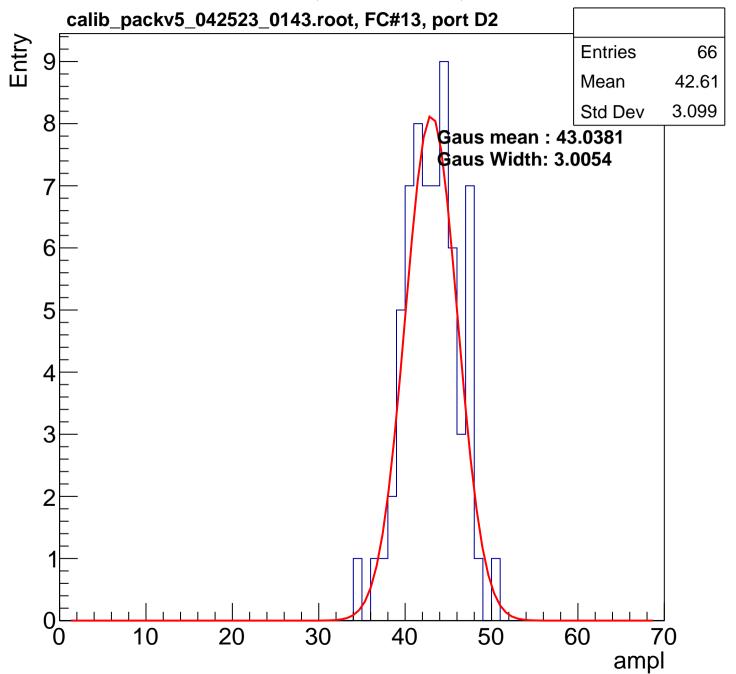


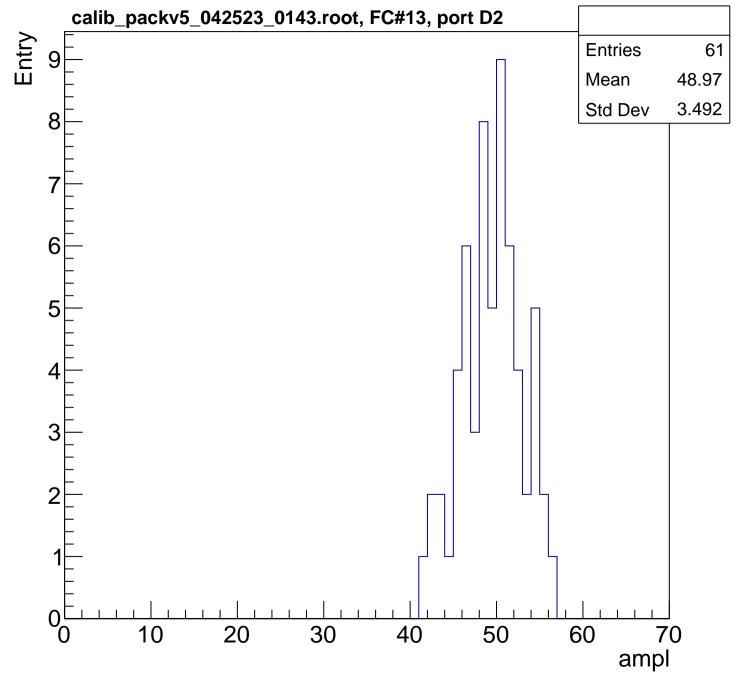
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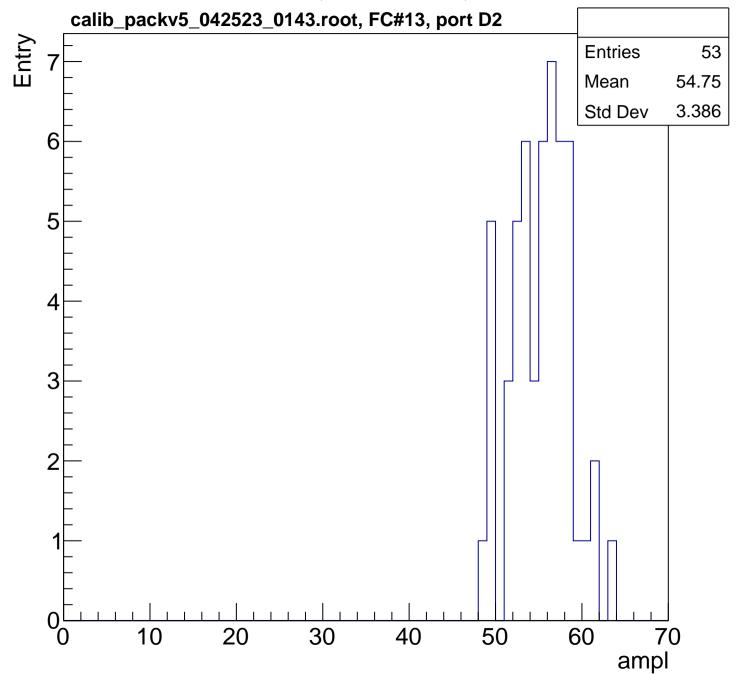


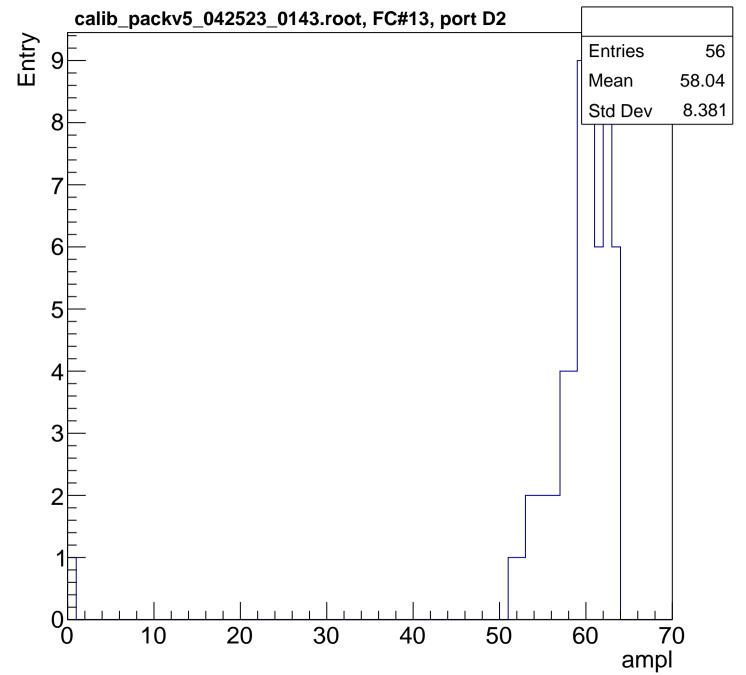


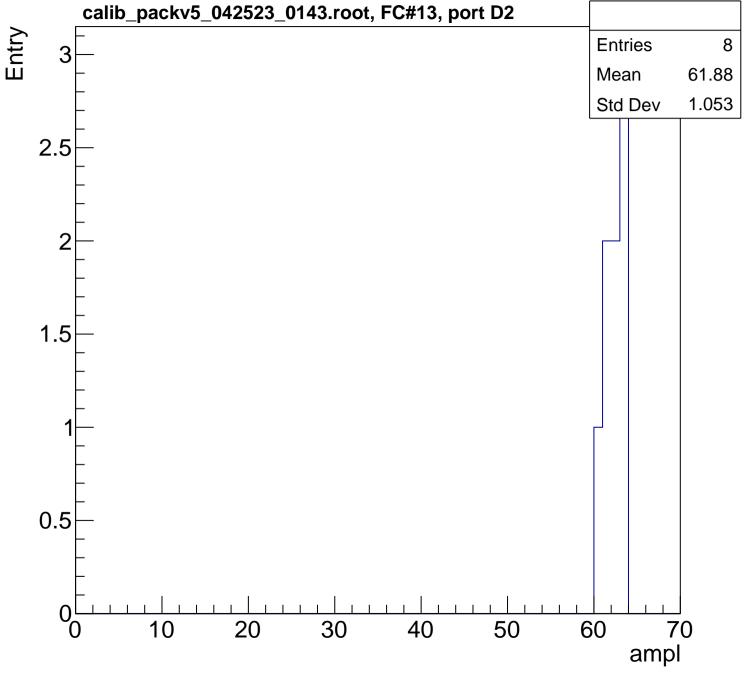




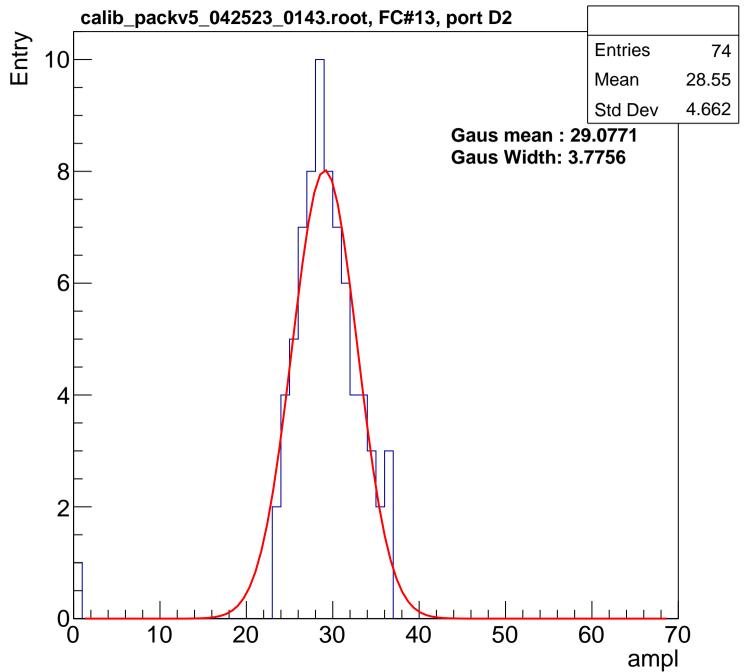


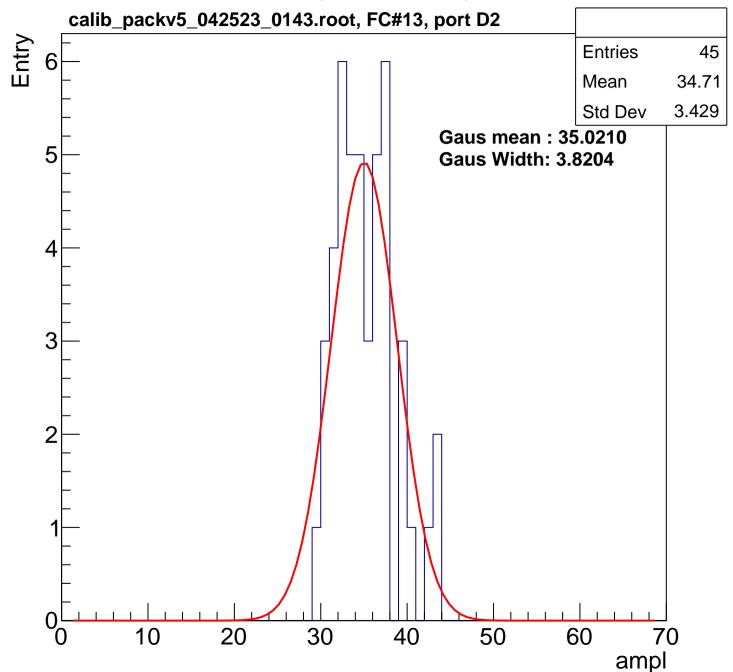


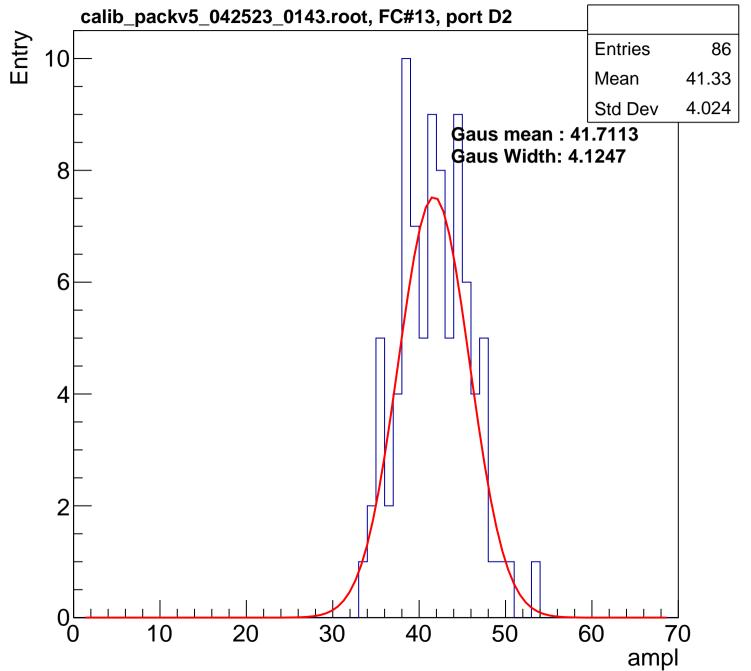


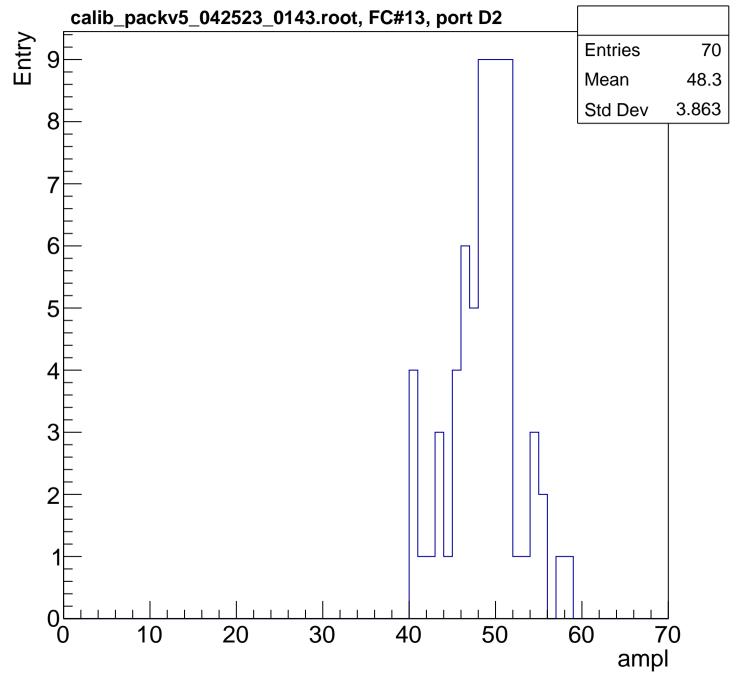


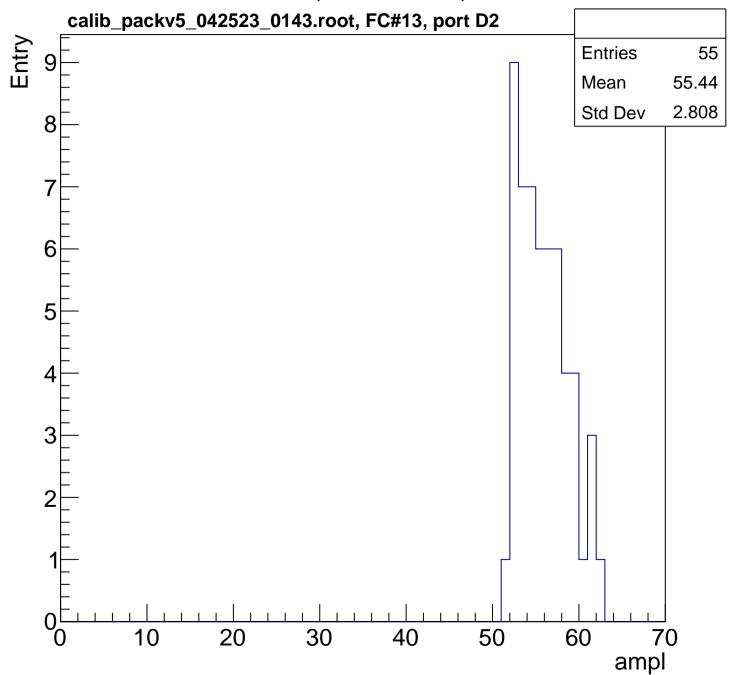


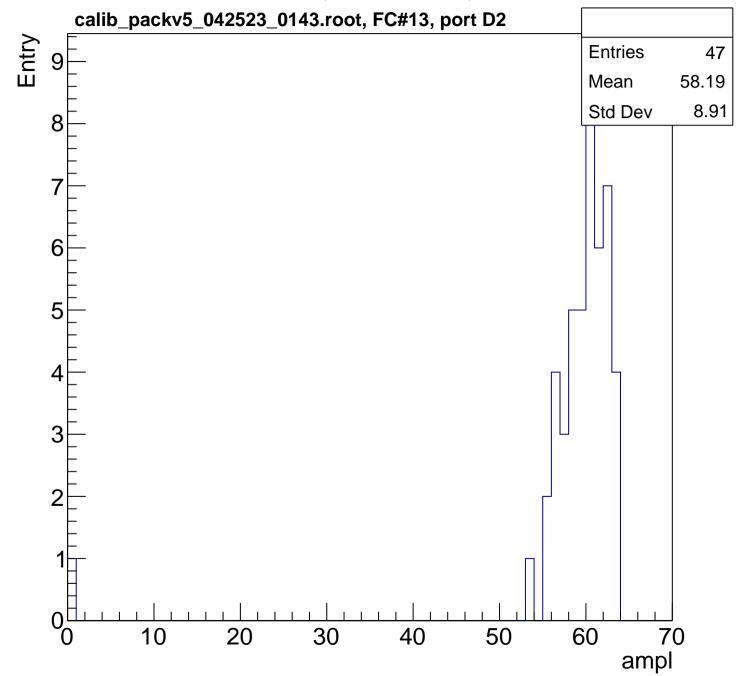


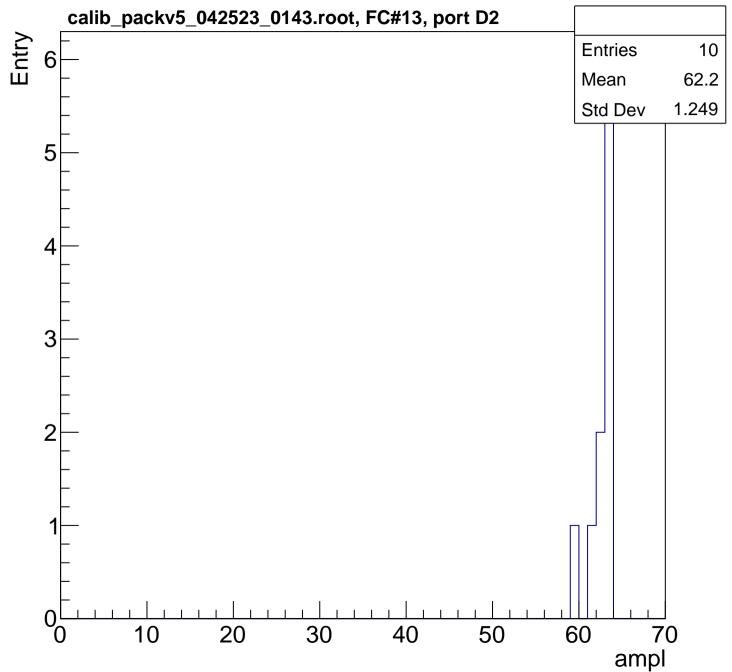




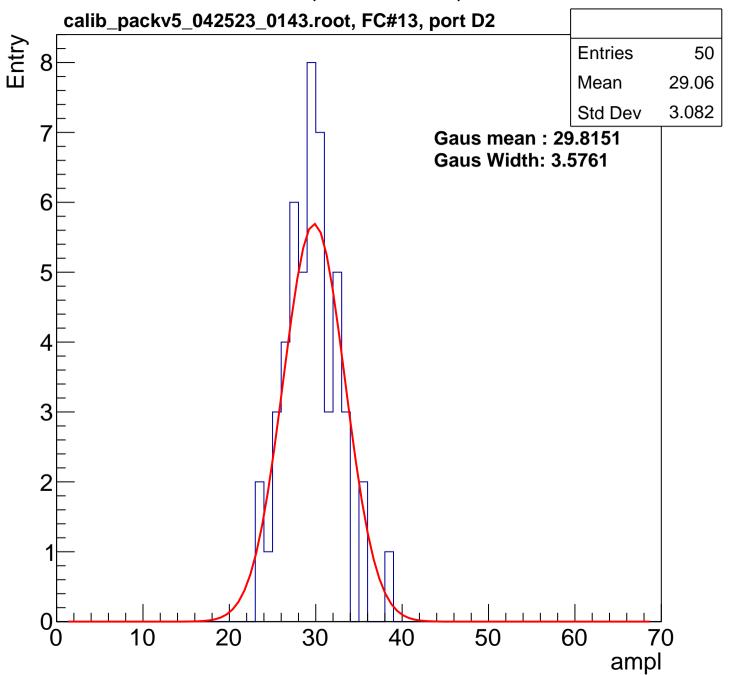


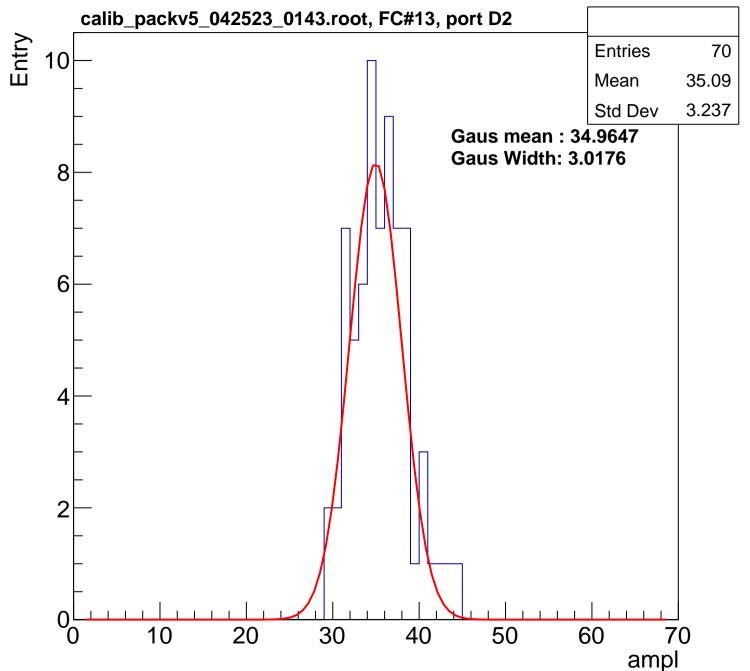


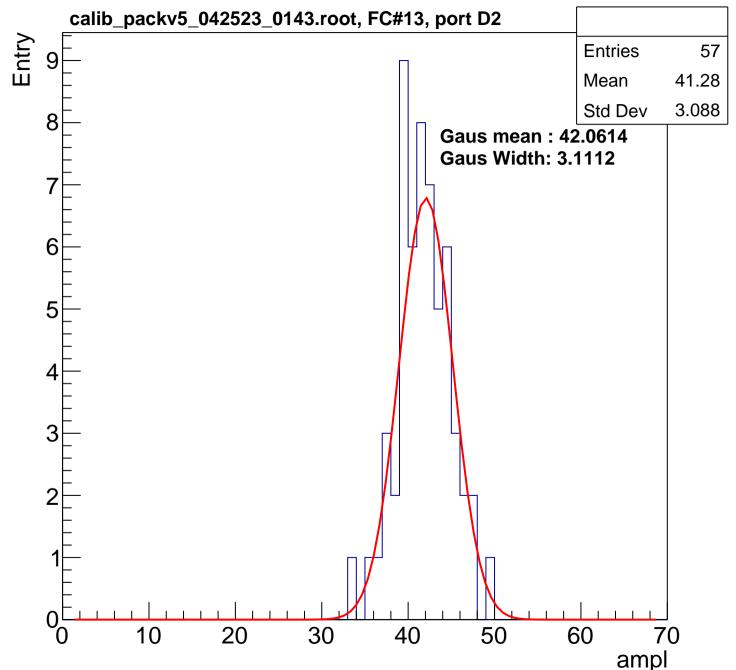


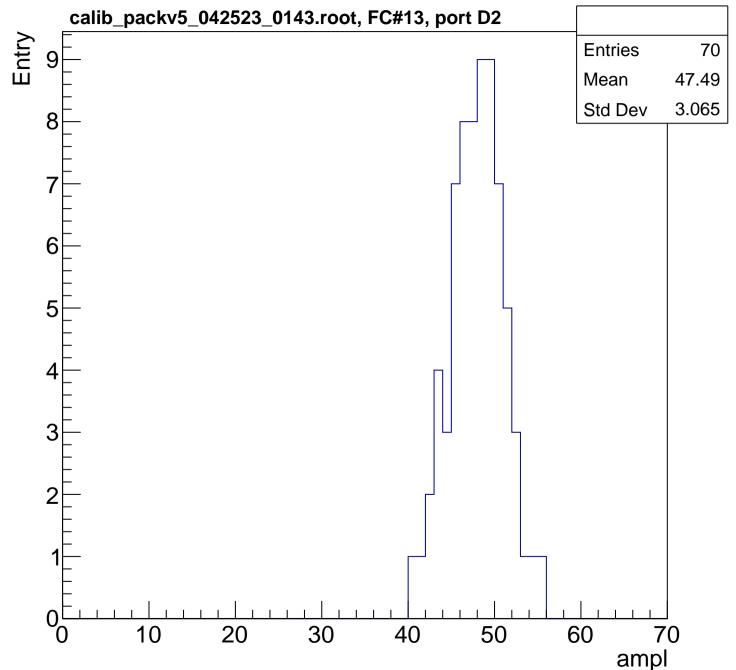


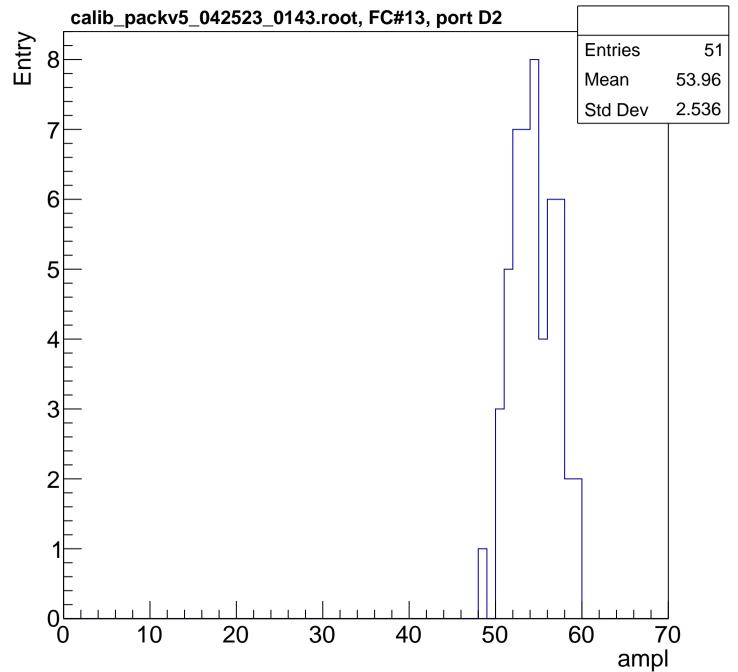


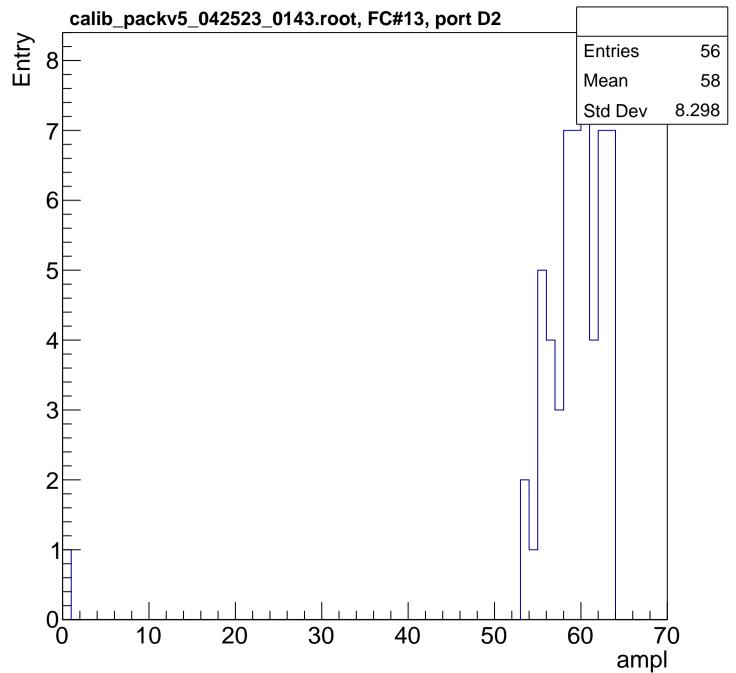


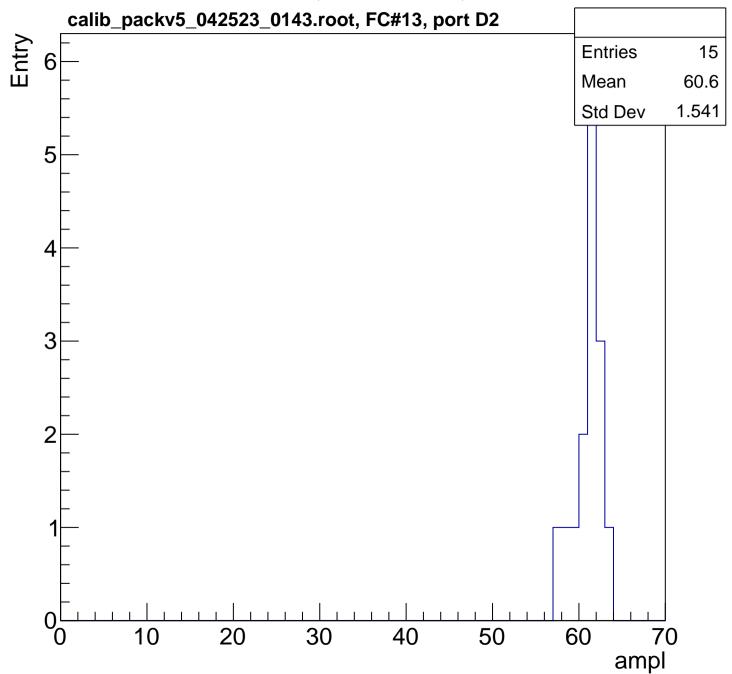


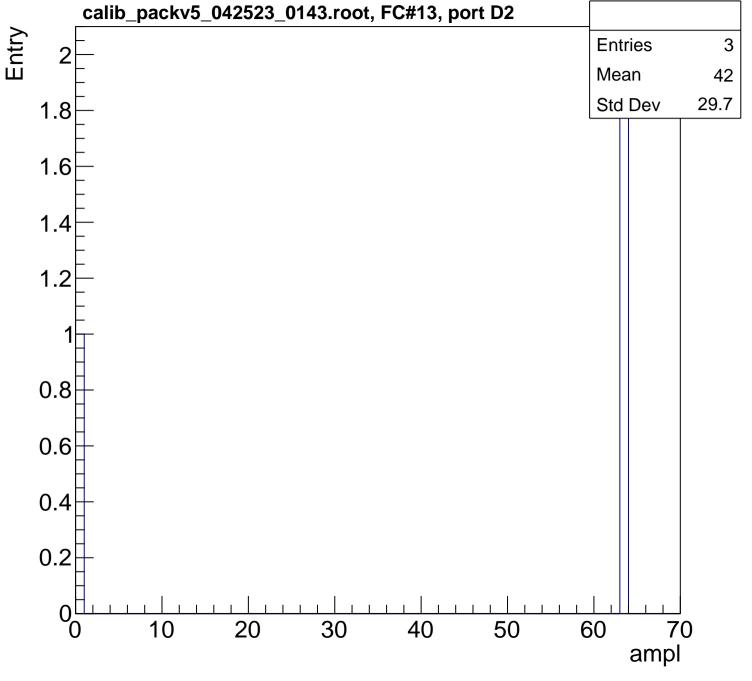


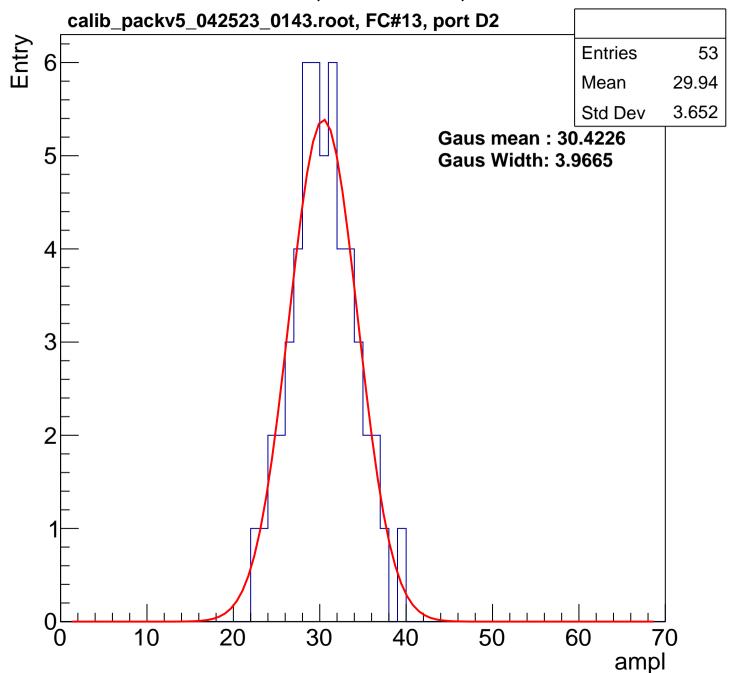


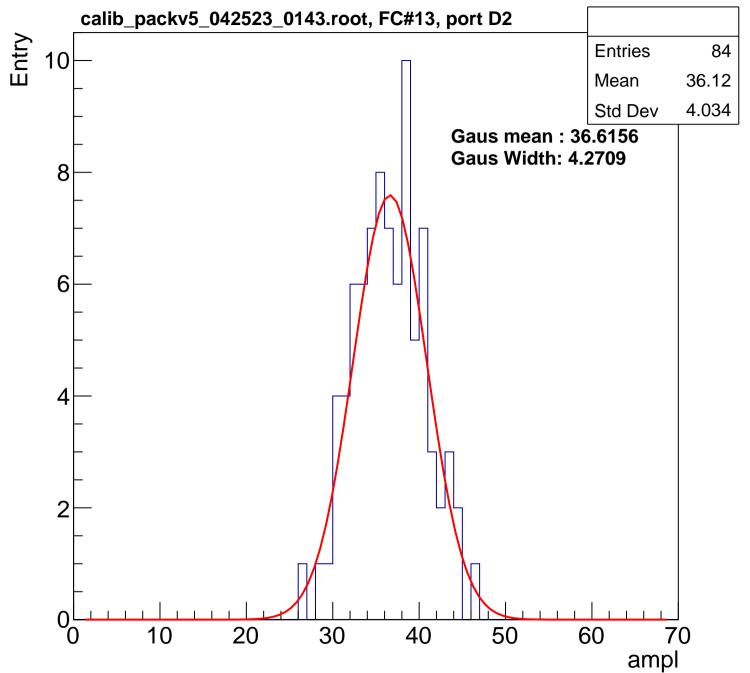


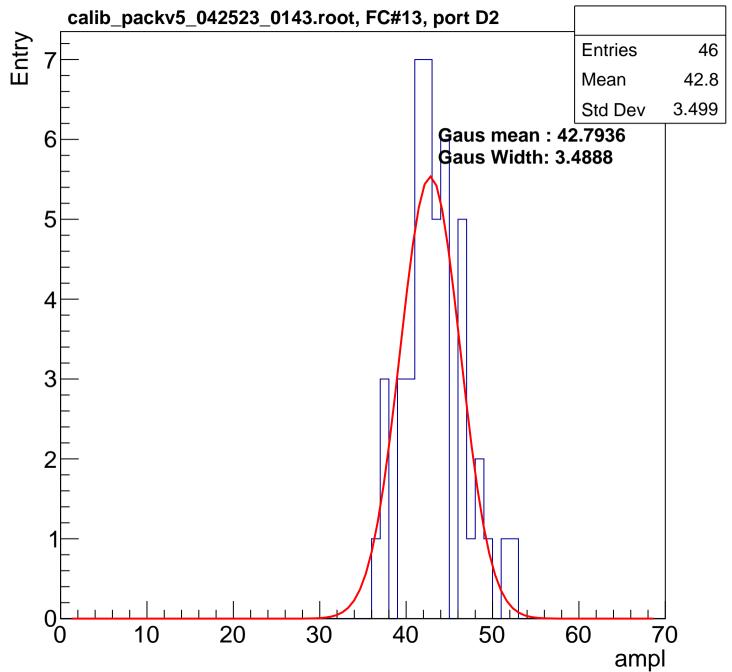


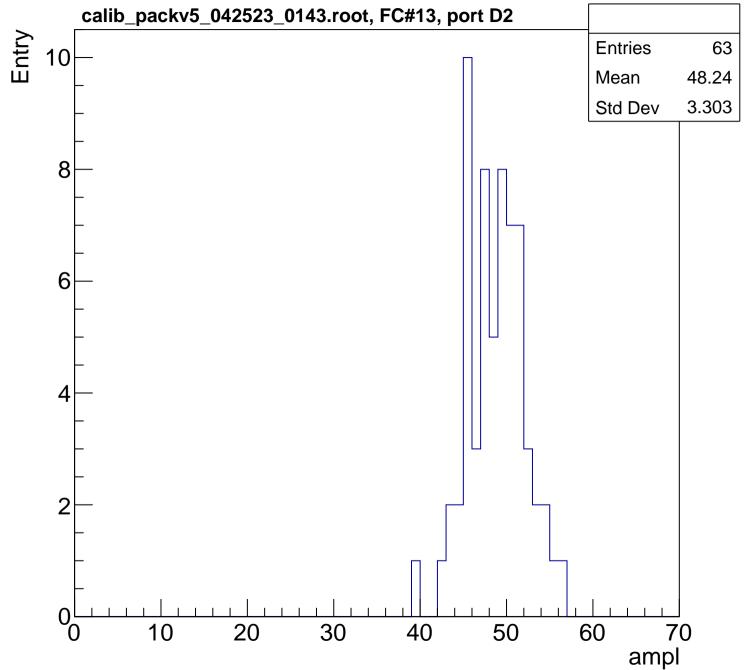


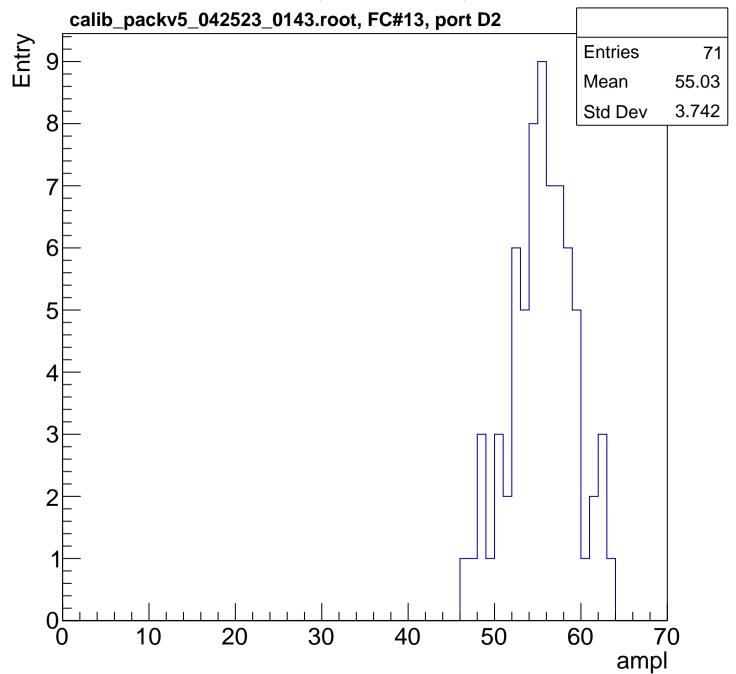


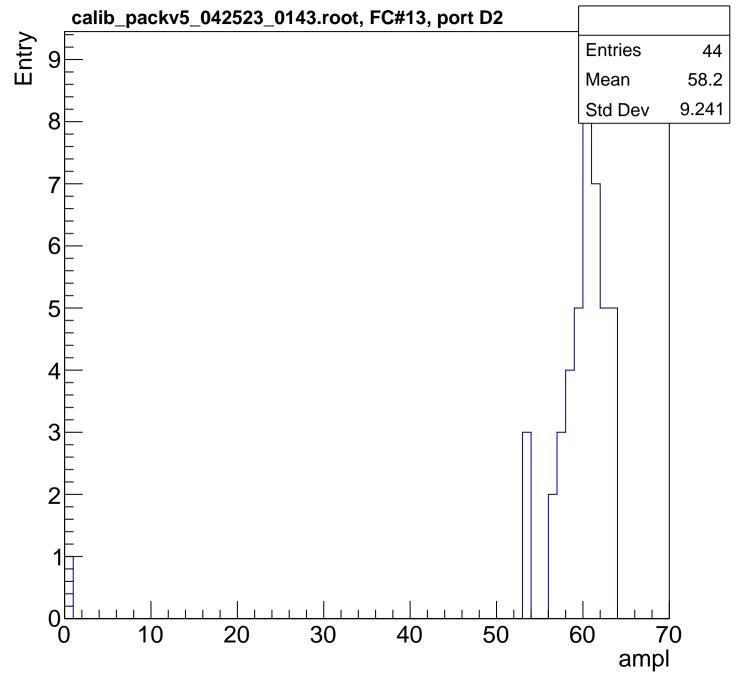


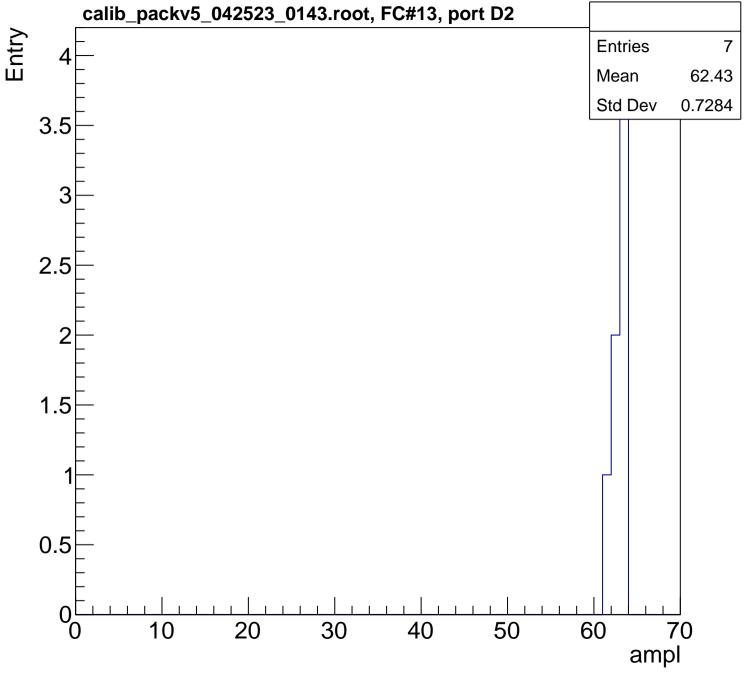




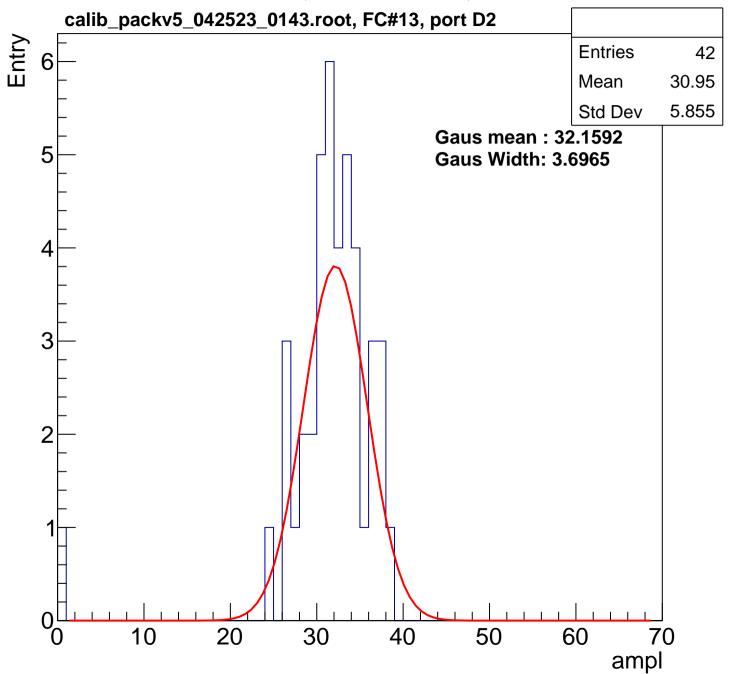


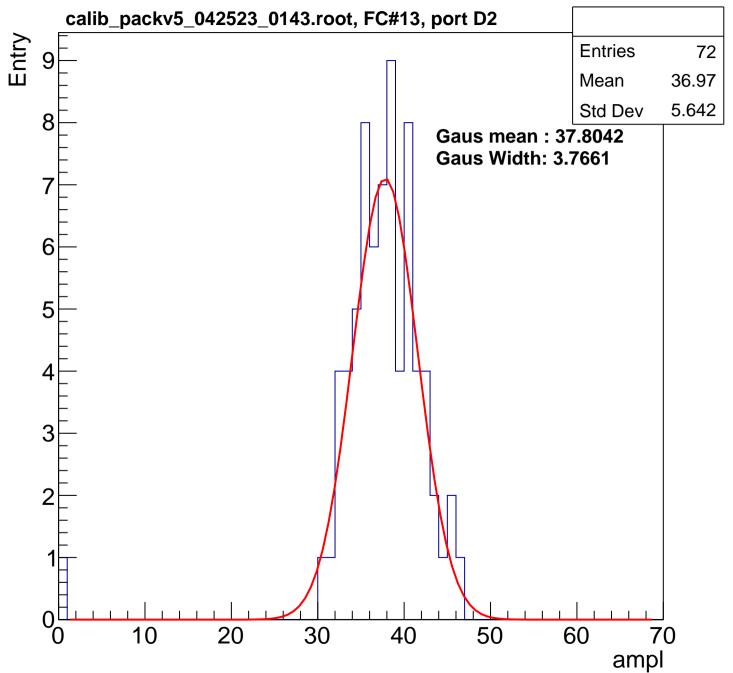


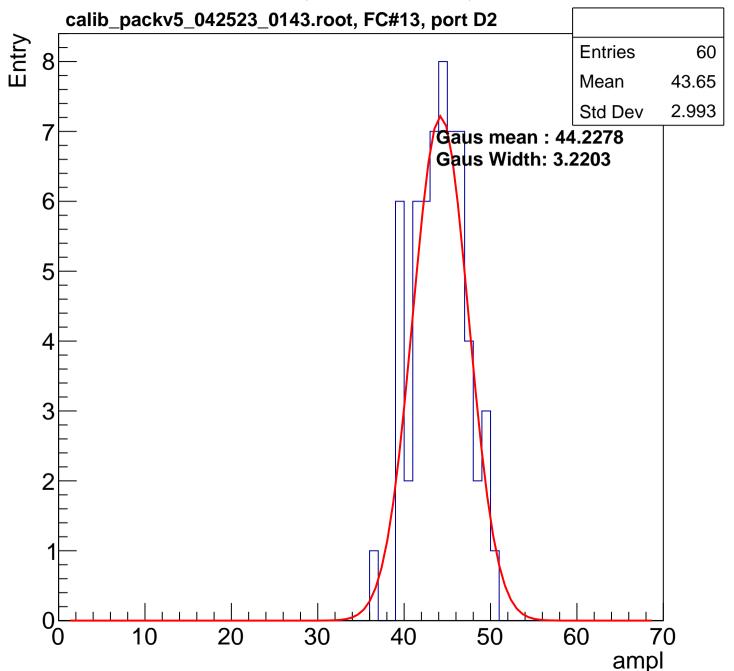


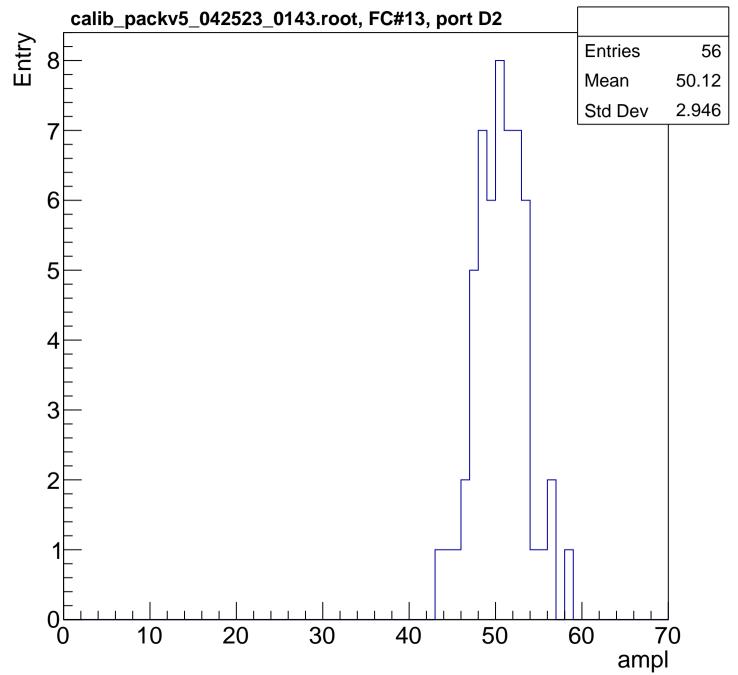


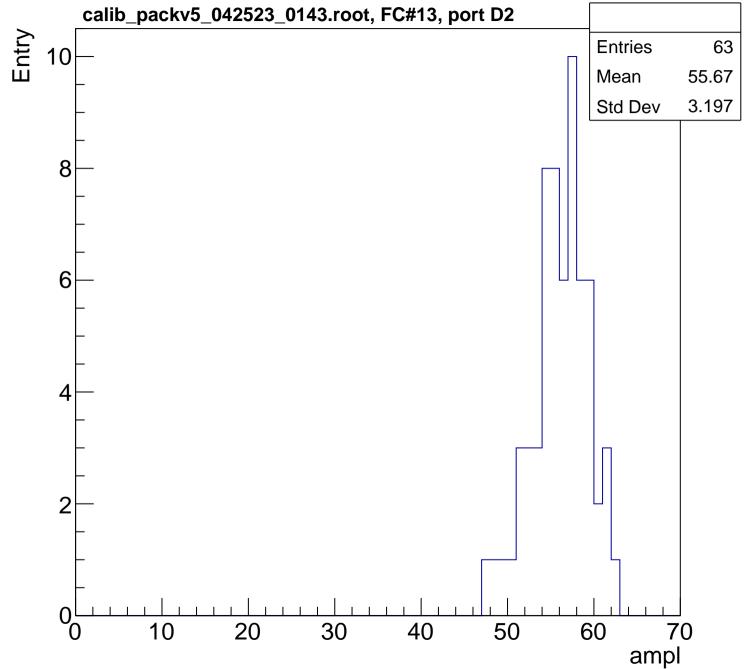
B1L003S, U2-ch99, adc7 calib_packv5_042523_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

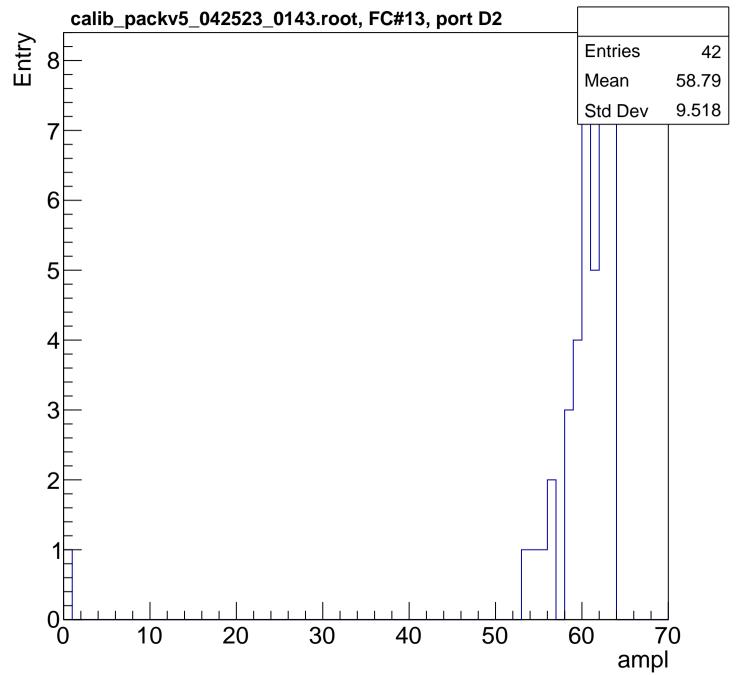


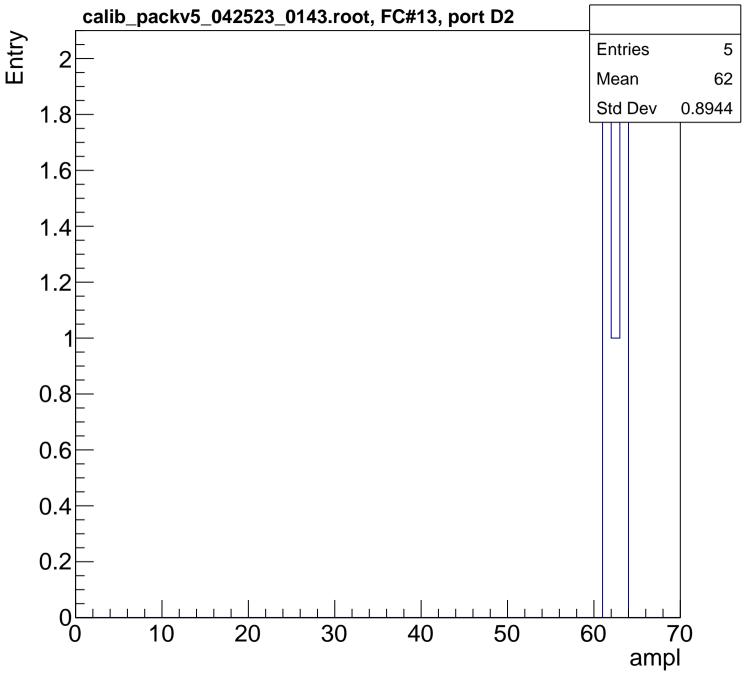


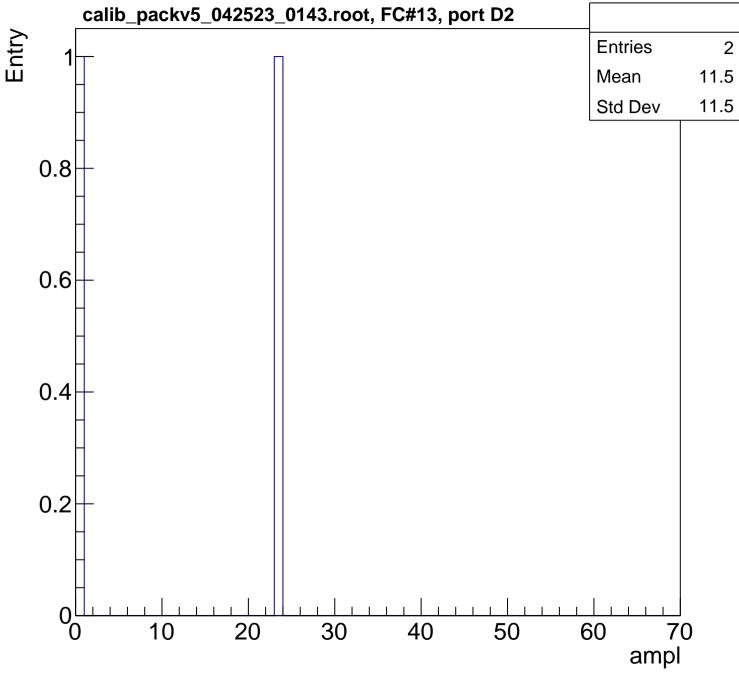


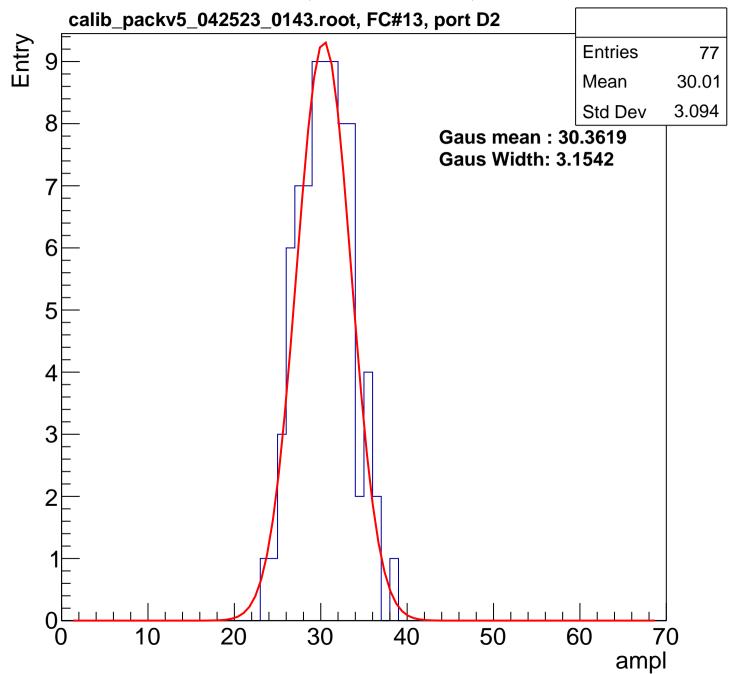


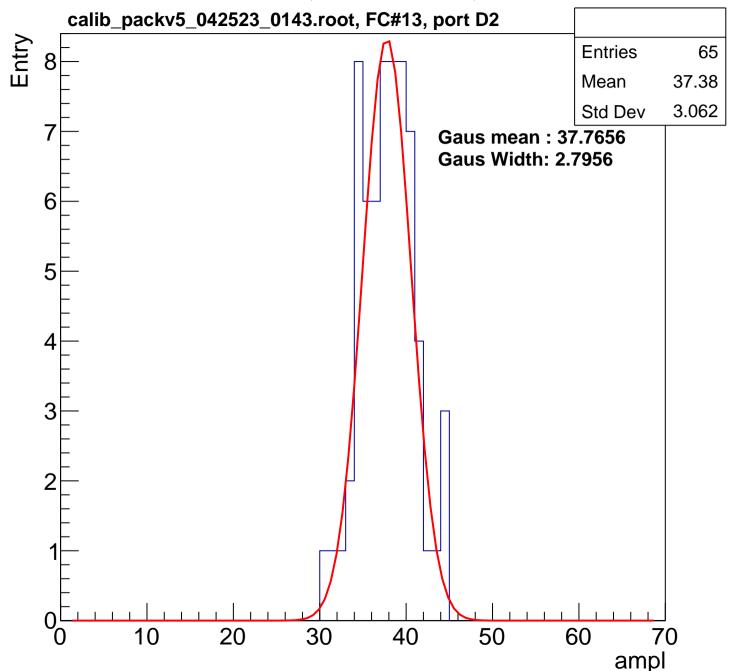


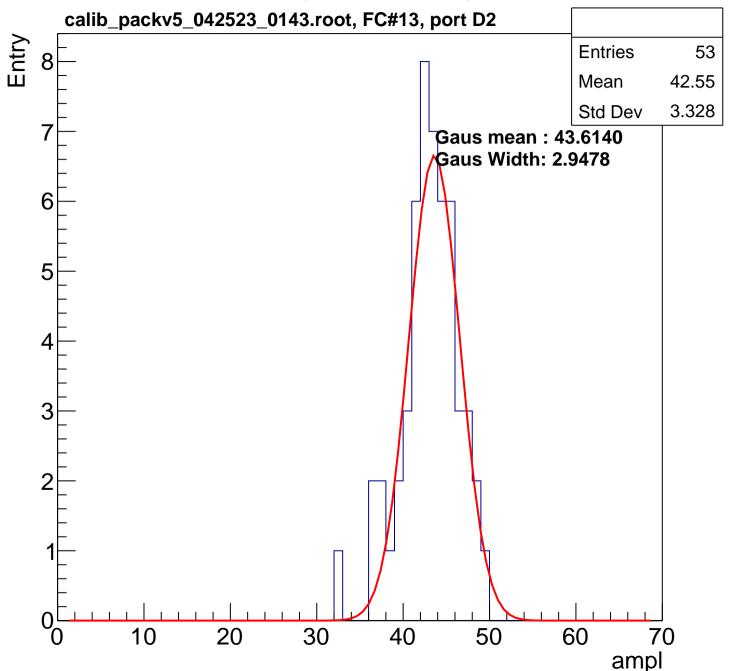


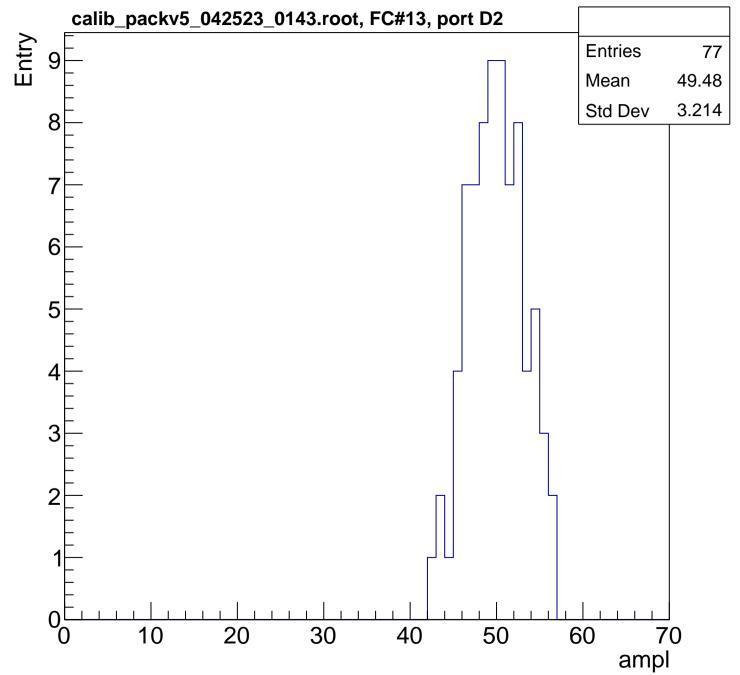


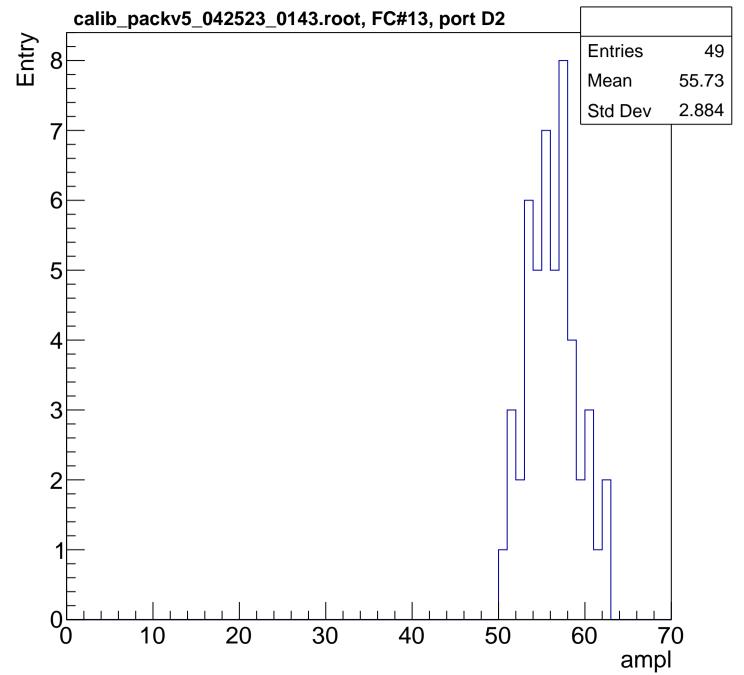


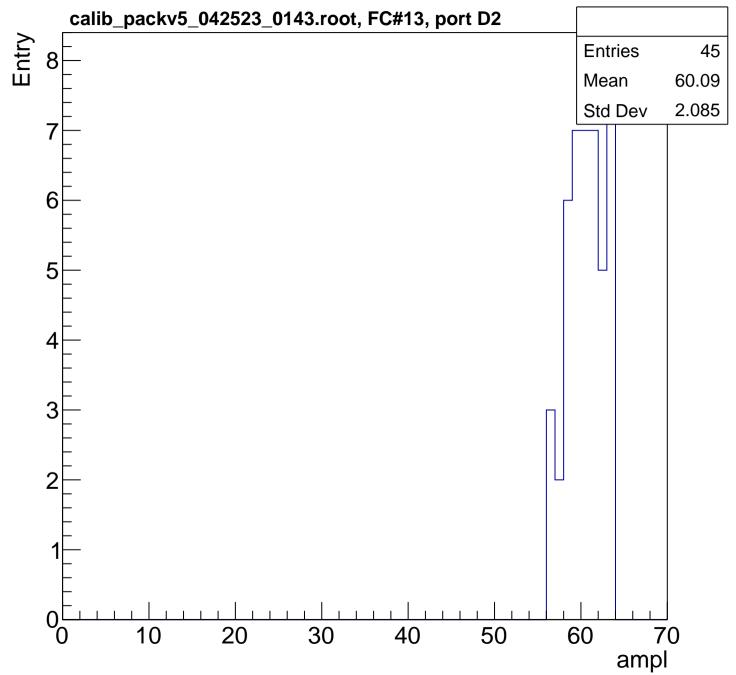


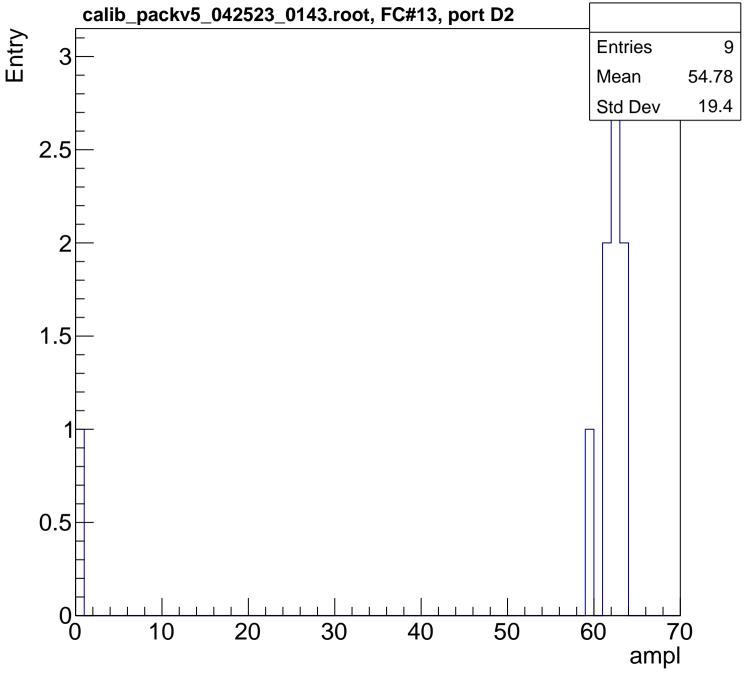












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