



# B1L003S, U7-ch0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	361
Mean	45.03
Std Dev	11.48

**Turn on : 28.6485**

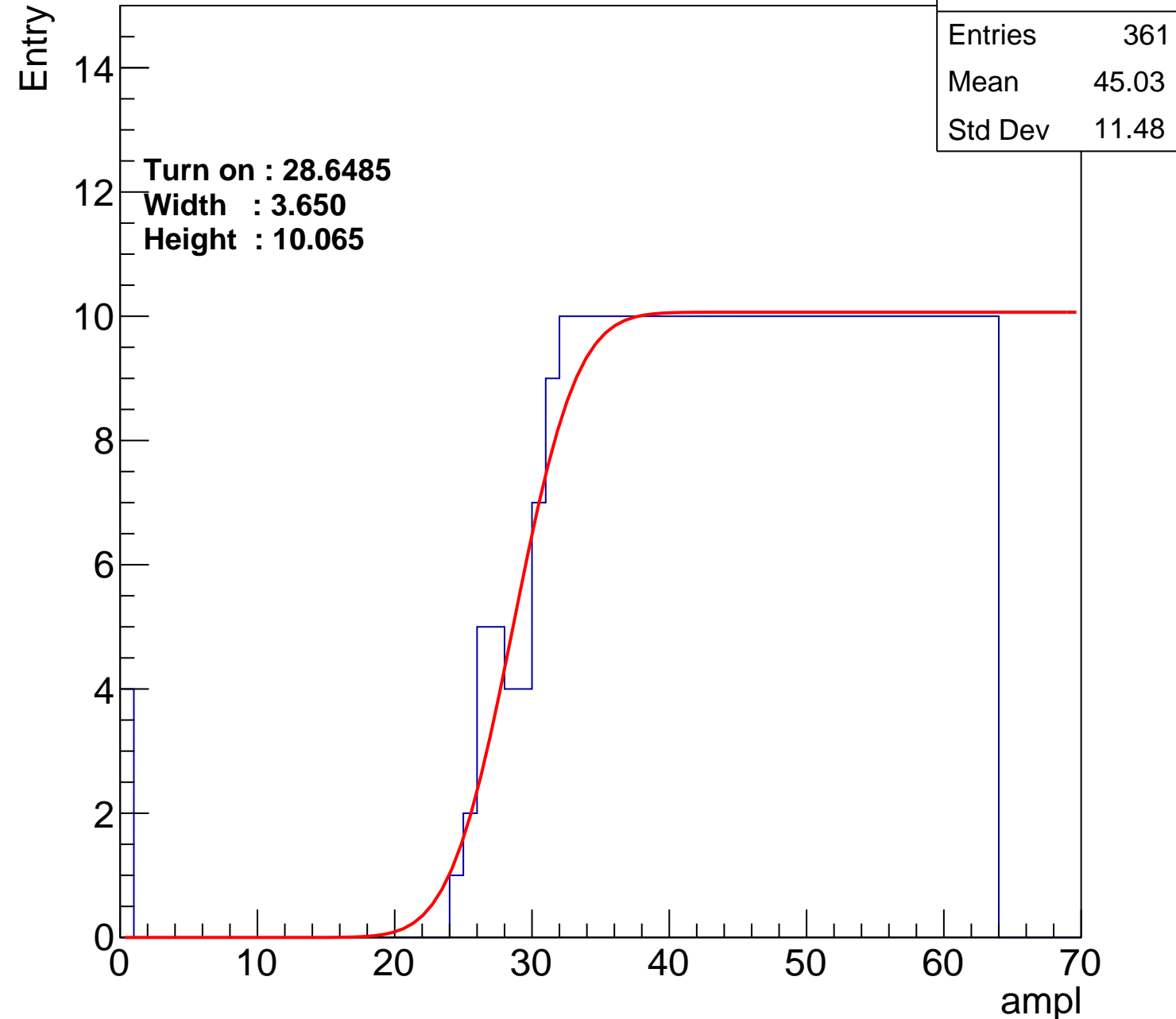
**Width : 3.650**

**Height : 10.065**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



**calib\_packv5\_042523\_0143.root, FC#13, port D2**

Turn on : 27.4328  
Width : 2.166  
Height : 9.995



# B1L003S, U7-ch2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	346
Mean	45.76
Std Dev	11.16

Turn on : 30.4384

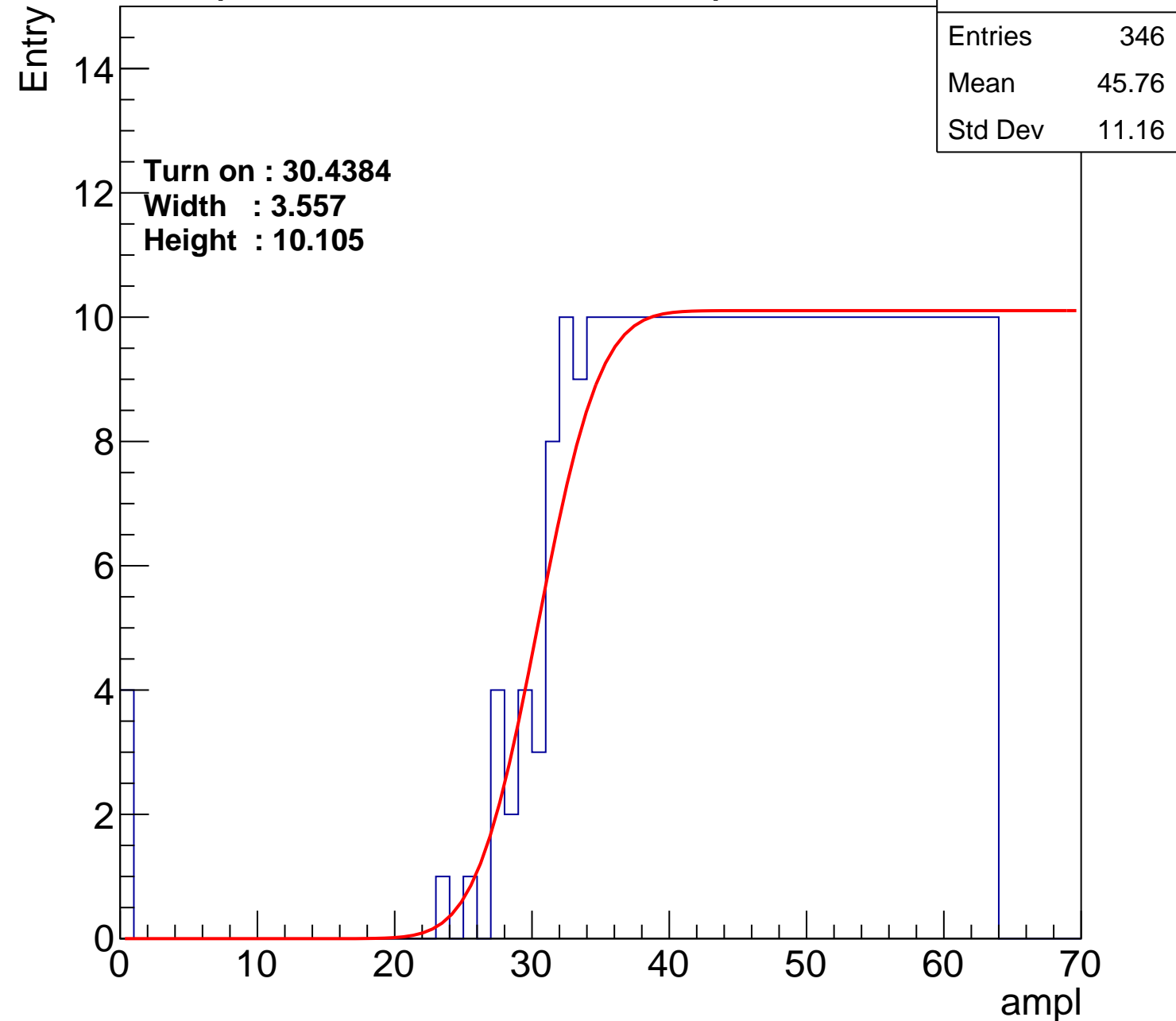
Width : 3.557

Height : 10.105

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch3

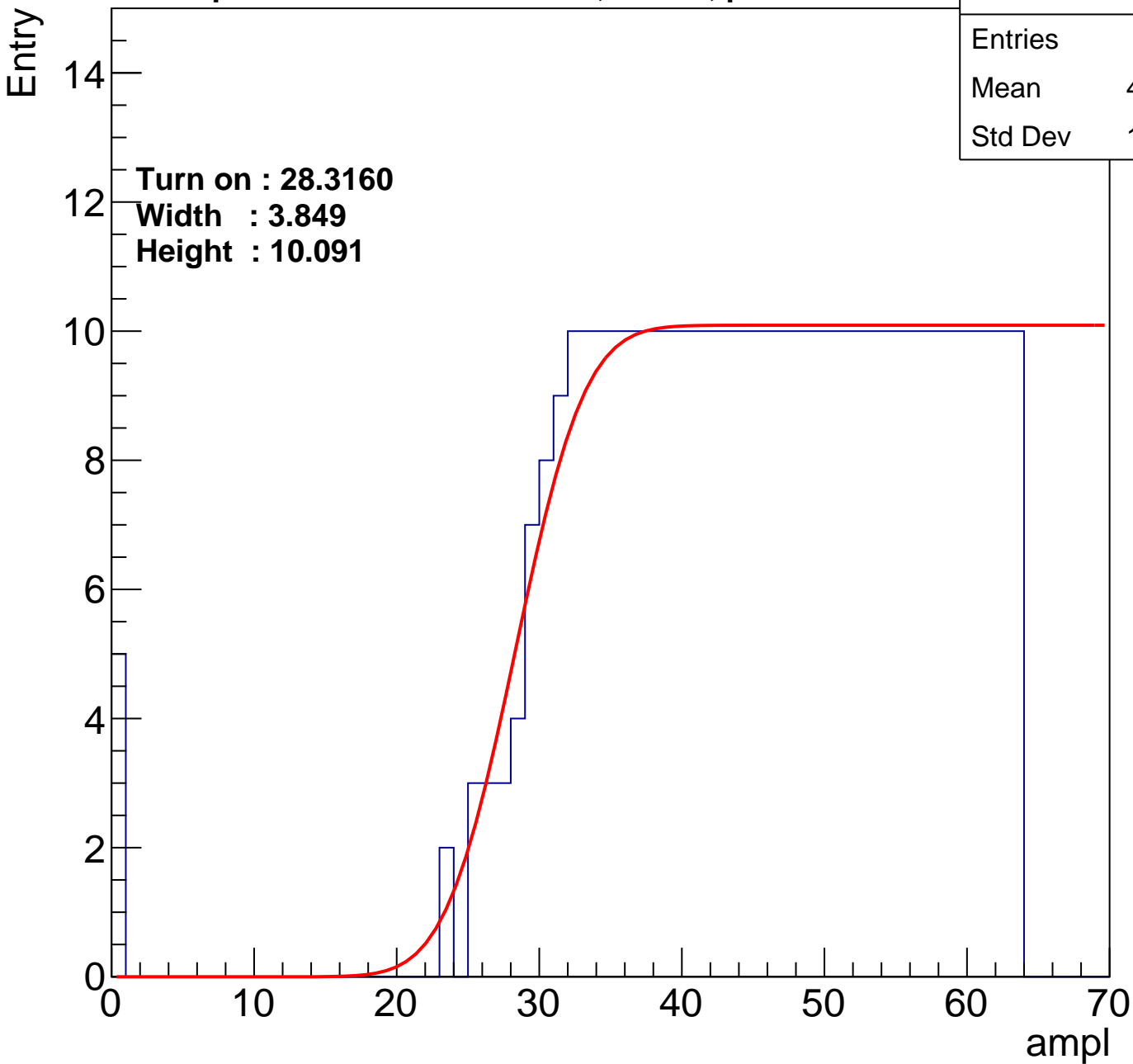
**calib\_packv5\_042523\_0143.root, FC#13, port D2**

**Turn on : 28.3160**

**Width : 3.849**

**Height : 10.091**

Entries	364
Mean	44.82
Std Dev	11.74



# B1L003S, U7-ch4

calib\_packv5\_042523\_0143.root, FC#13, port D2

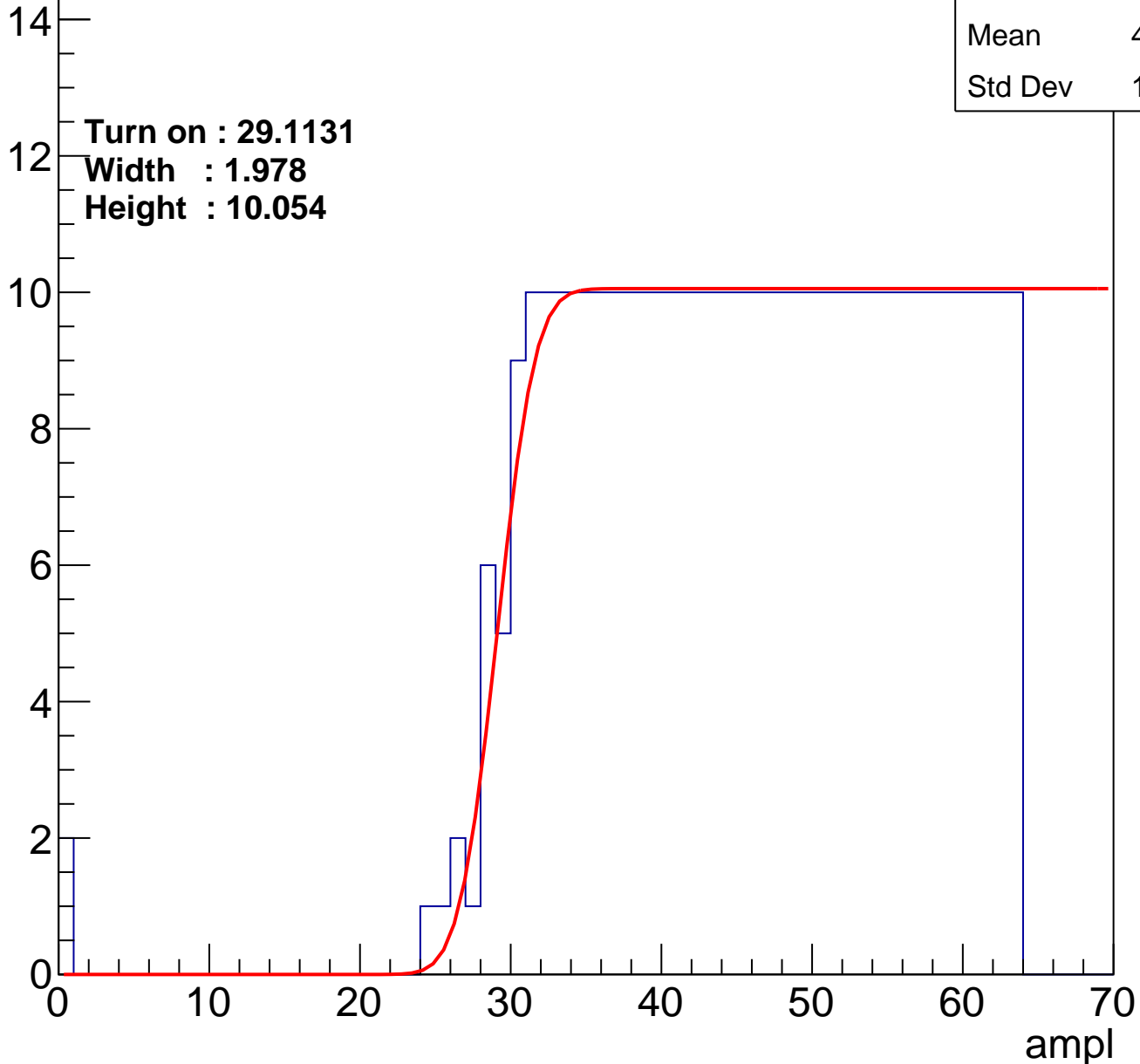
Entries	357
Mean	45.44
Std Dev	10.87

Turn on : 29.1131

Width : 1.978

Height : 10.054

Entry



# B1L003S, U7-ch5

calib\_packv5\_042523\_0143.root, FC#13, port D2

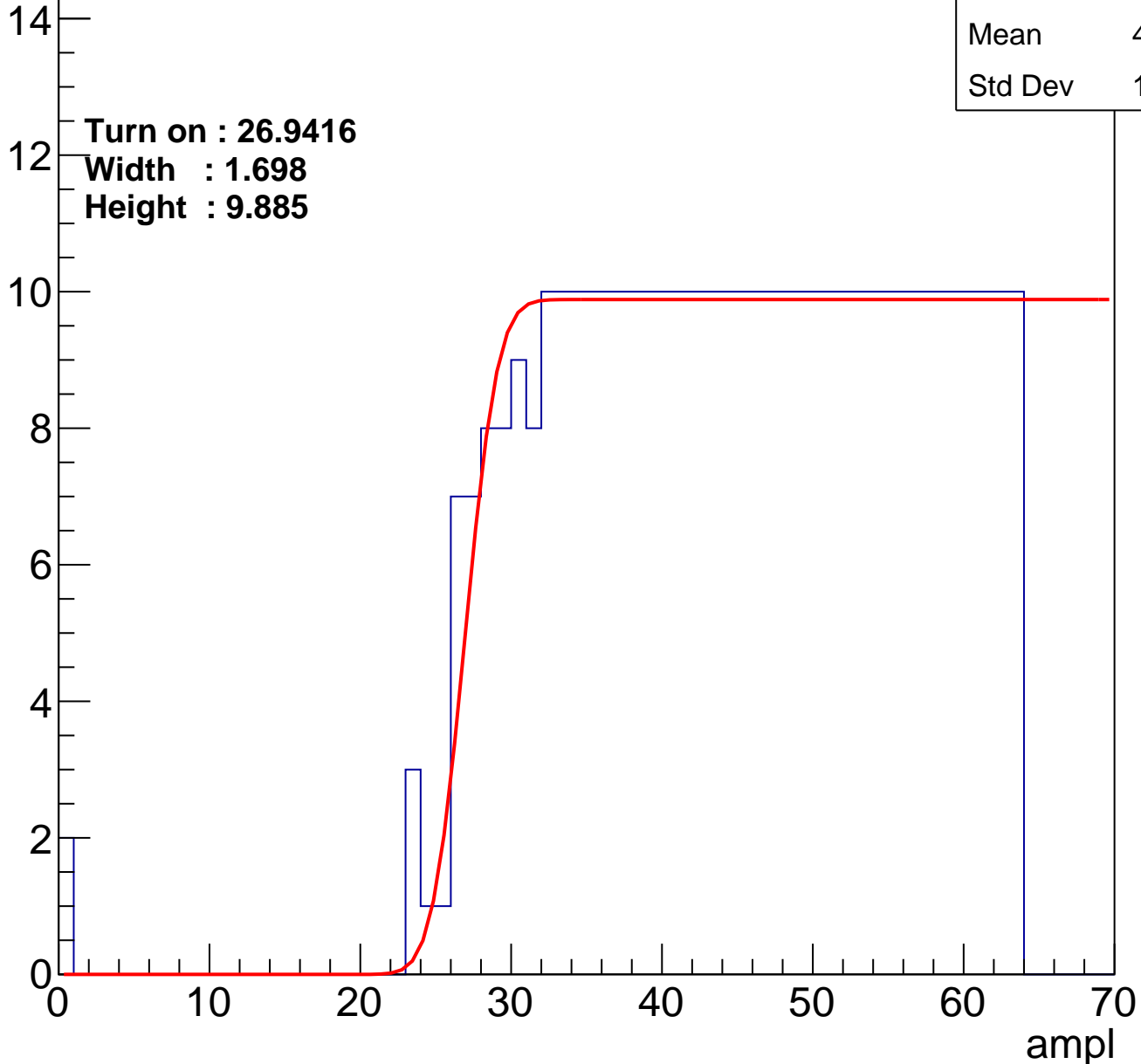
Entries	374
Mean	44.55
Std Dev	11.36

Turn on : 26.9416

Width : 1.698

Height : 9.885

Entry



# B1L003S, U7-ch6

calib\_packv5\_042523\_0143.root, FC#13, port D2

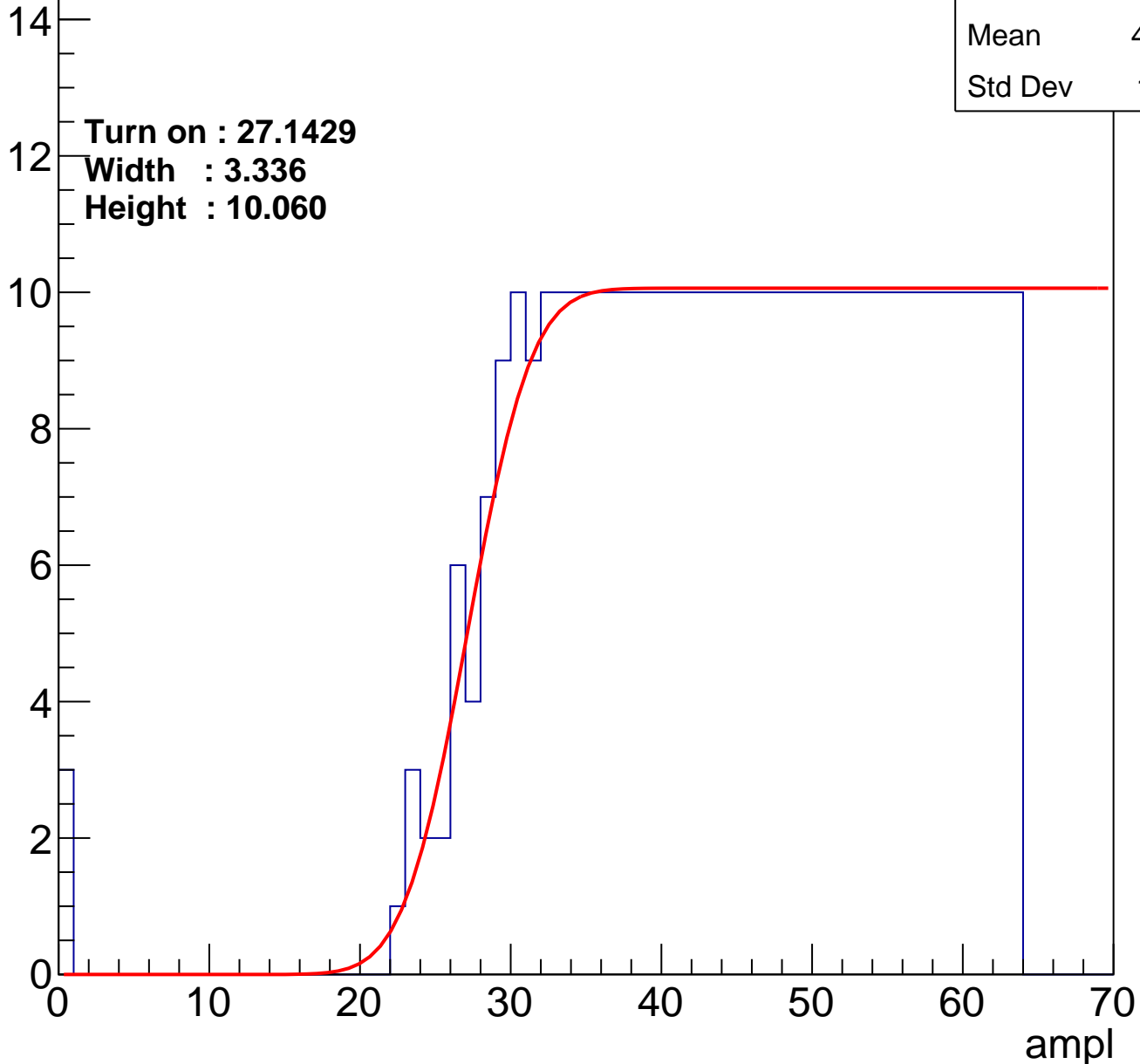
Entries	376
Mean	44.39
Std Dev	11.61

Turn on : 27.1429

Width : 3.336

Height : 10.060

Entry





# B1L003S, U7-ch7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	347
Mean	45.91
Std Dev	10.65

**Turn on : 29.7203**

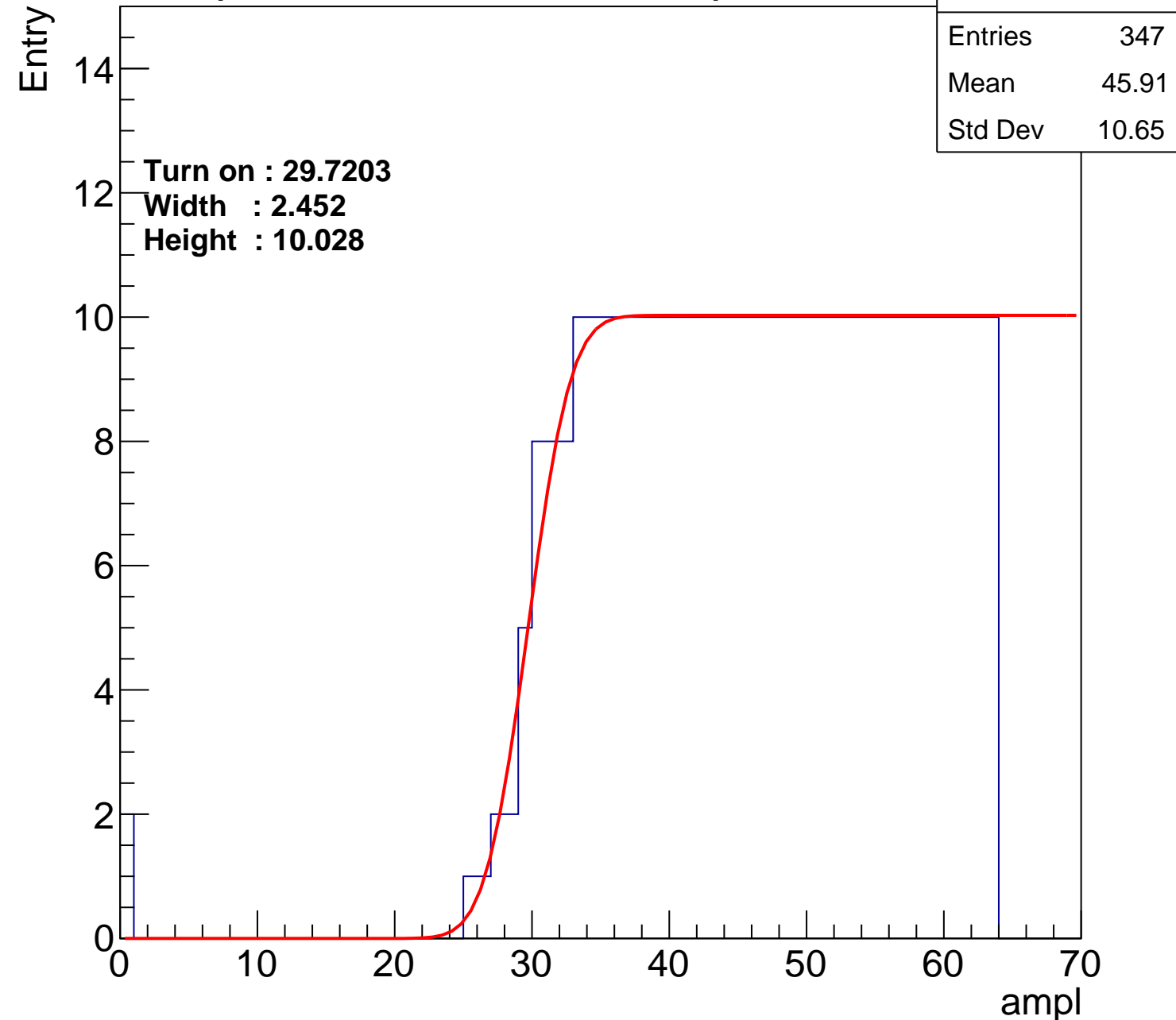
**Width : 2.452**

**Height : 10.028**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch8

calib\_packv5\_042523\_0143.root, FC#13, port D2

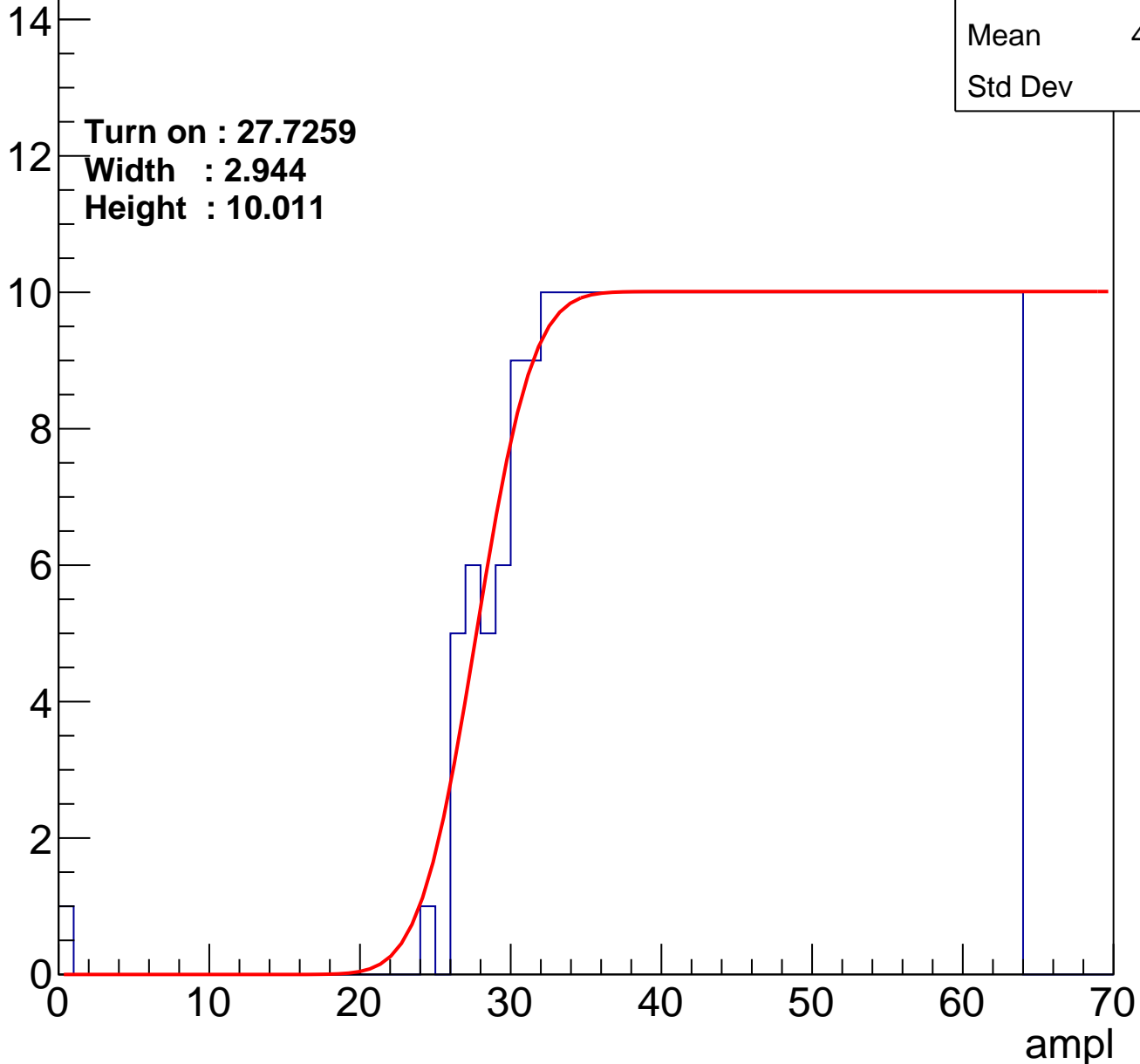
Entries	362
Mean	45.25
Std Dev	10.8

Turn on : 27.7259

Width : 2.944

Height : 10.011

Entry



# B1L003S, U7-ch9

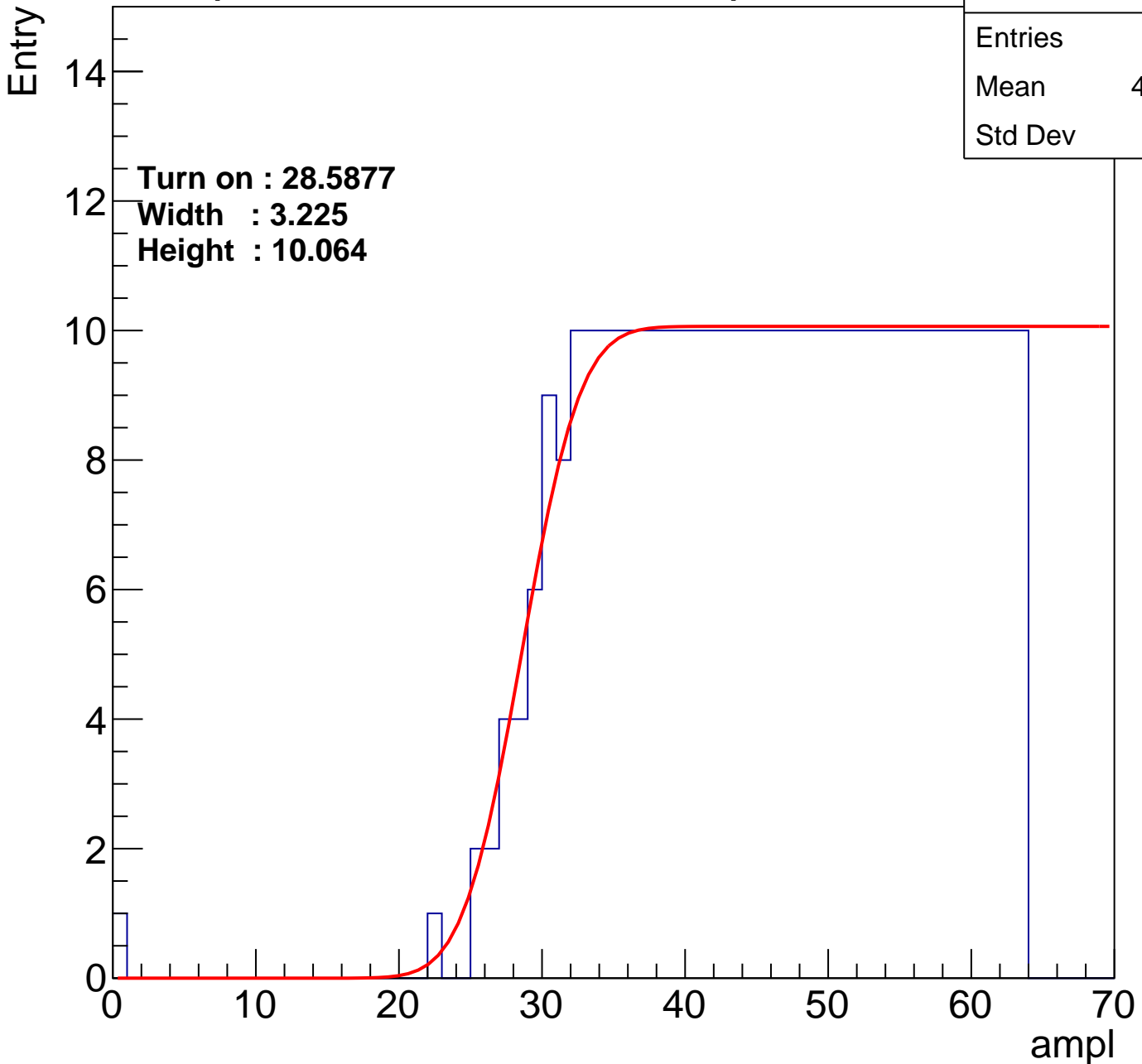
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	357
Mean	45.48
Std Dev	10.7

Turn on : 28.5877

Width : 3.225

Height : 10.064



# B1L003S, U7-ch10

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	375
Mean	44.53
Std Dev	11.36

**Turn on : 27.2693**

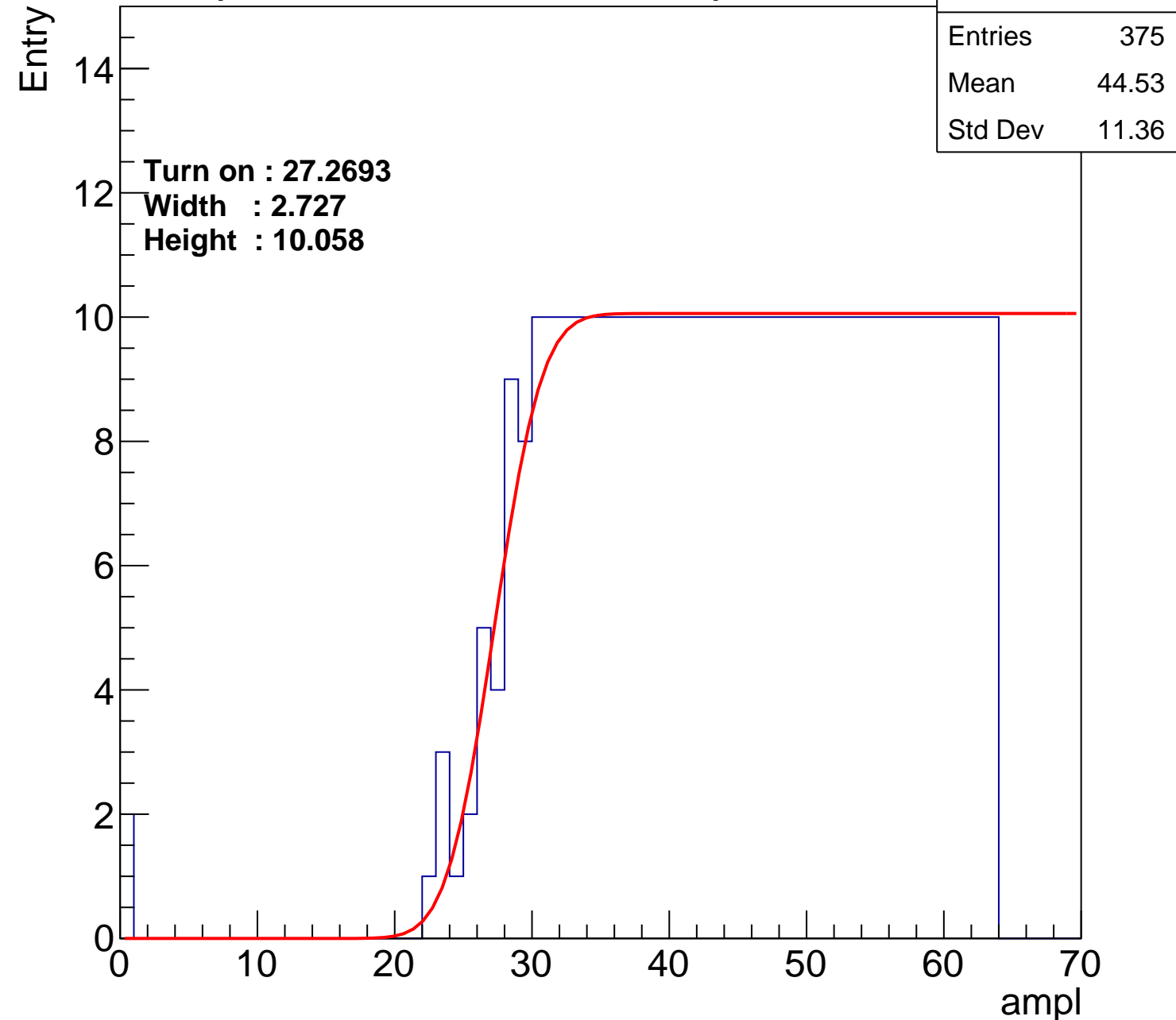
**Width : 2.727**

**Height : 10.058**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch11

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	376
Mean	44.24
Std Dev	11.98

Turn on : 27.6532

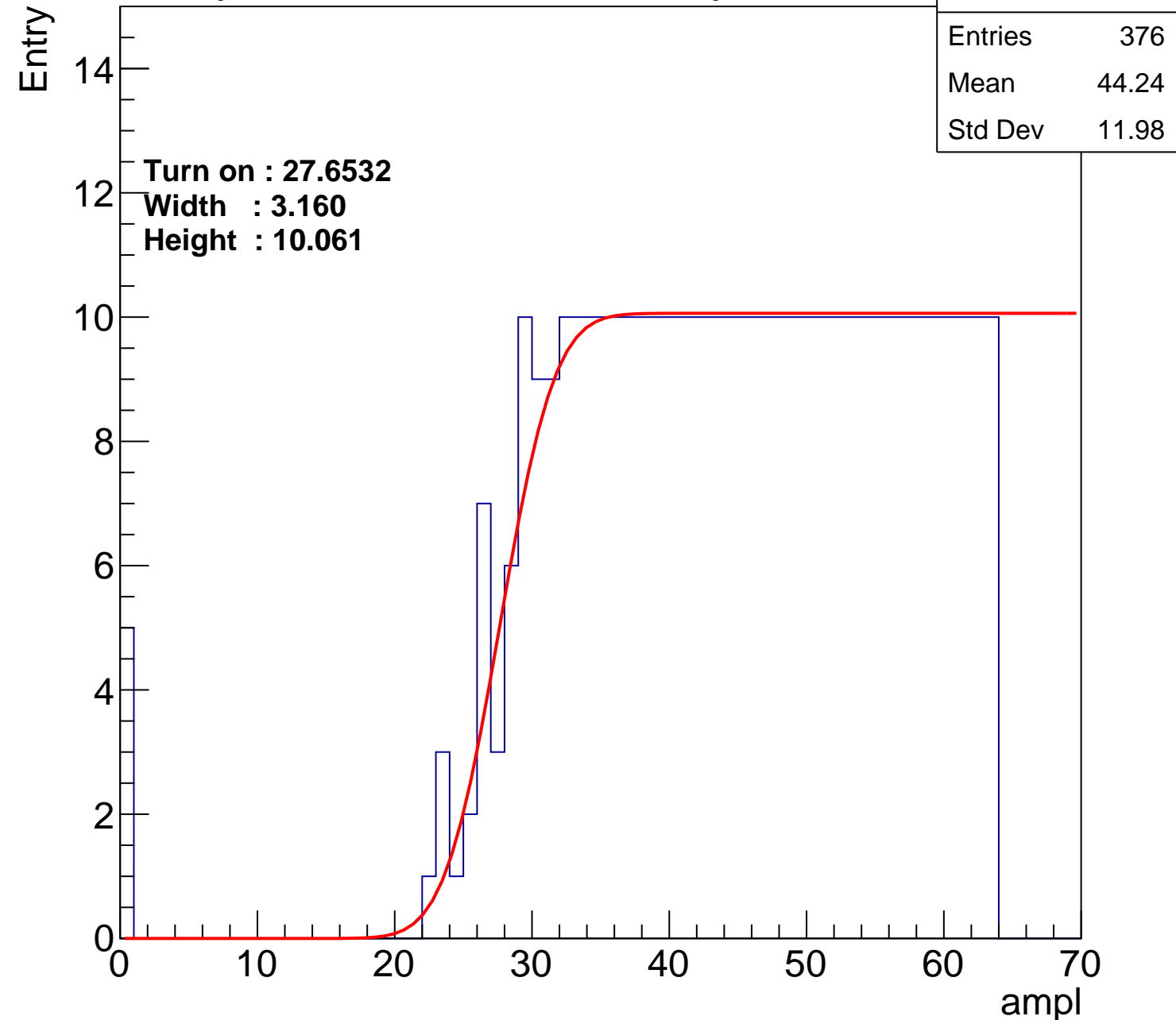
Width : 3.160

Height : 10.061

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch12

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	369
Mean	44.9
Std Dev	10.99

Turn on : 27.0076

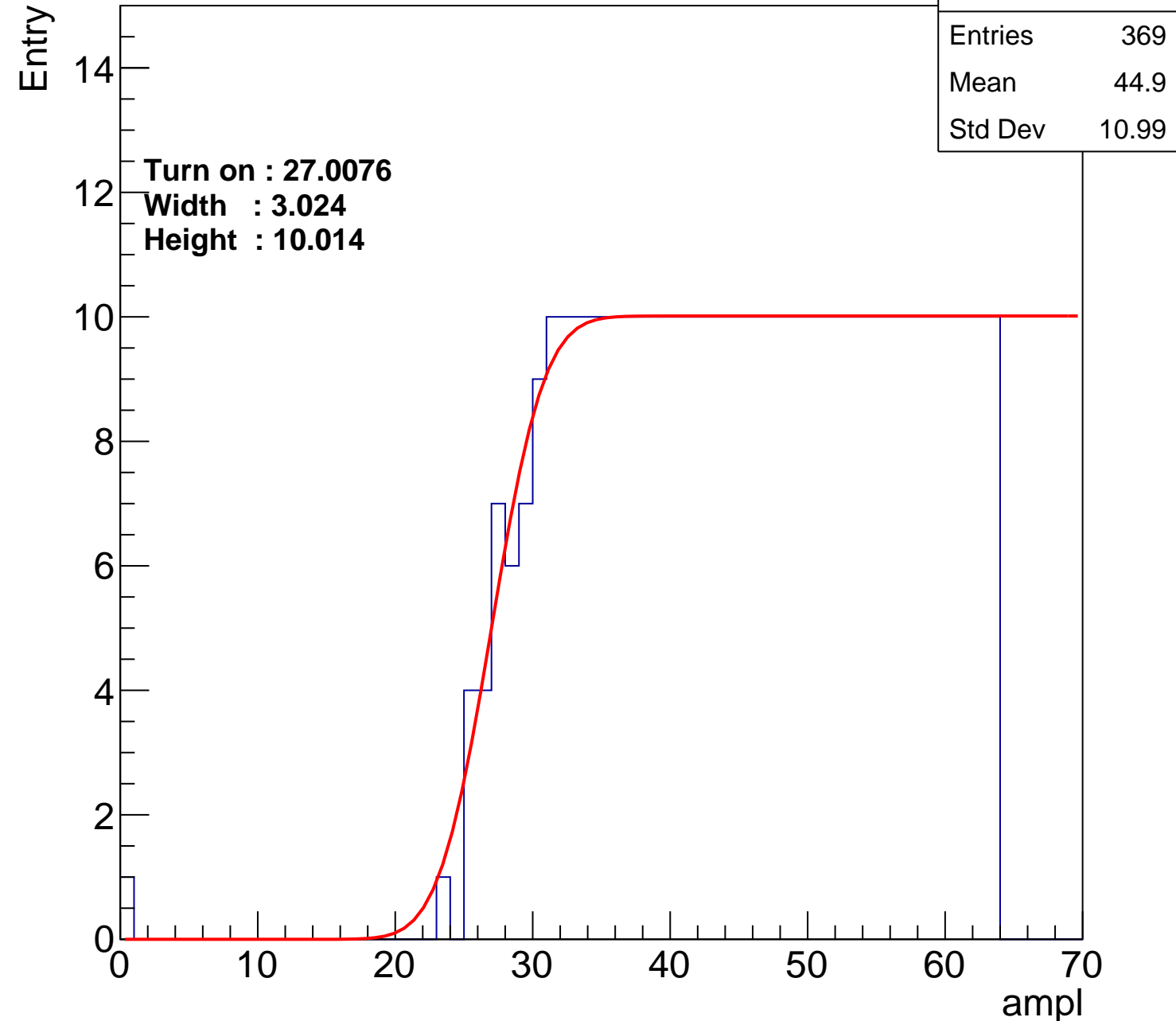
Width : 3.024

Height : 10.014

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch13

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	361
Mean	45.12
Std Dev	11.25

**Turn on : 28.3920**

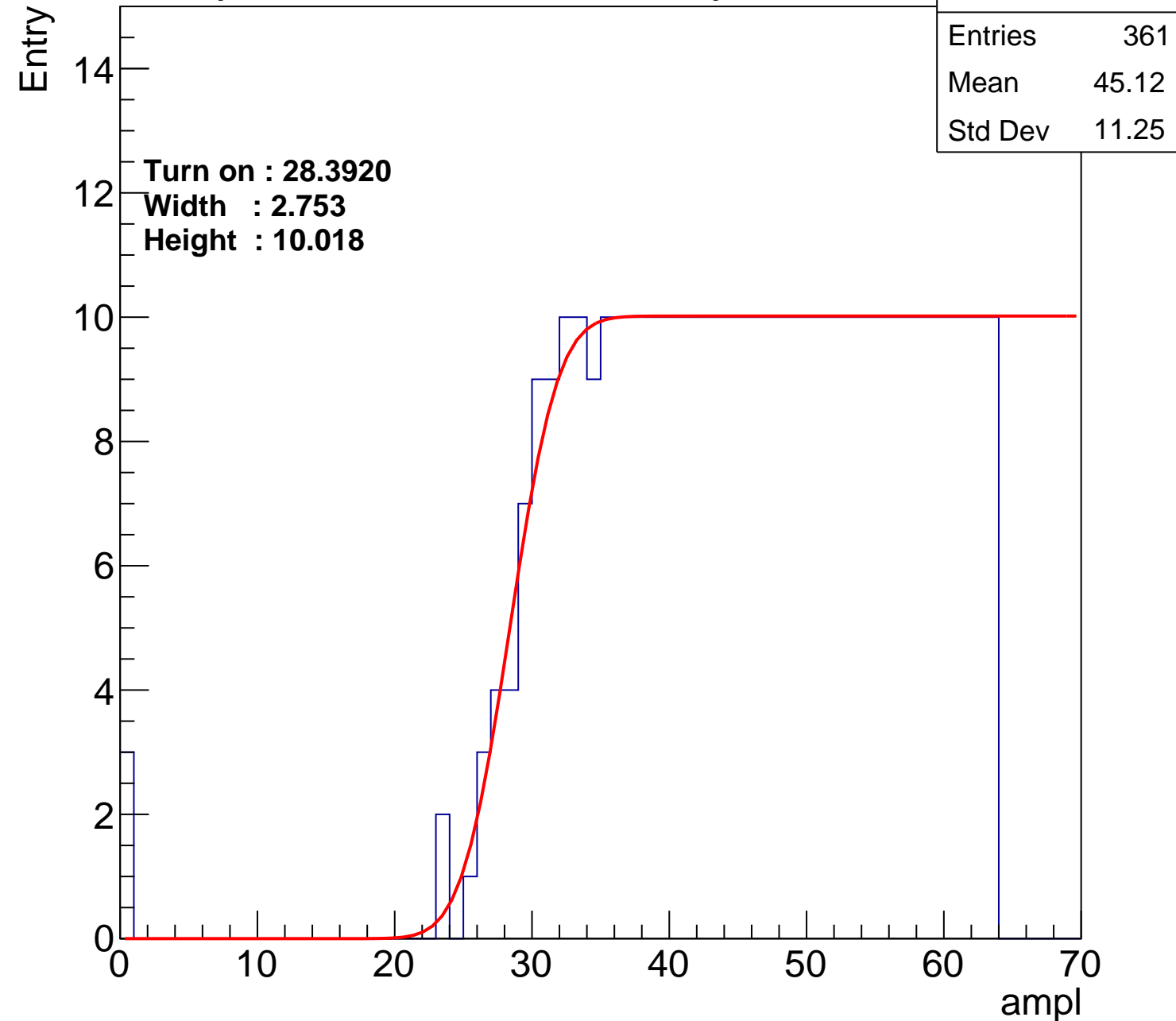
**Width : 2.753**

**Height : 10.018**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch14

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	373
Mean	44.63
Std Dev	11.3

Turn on : 26.2975

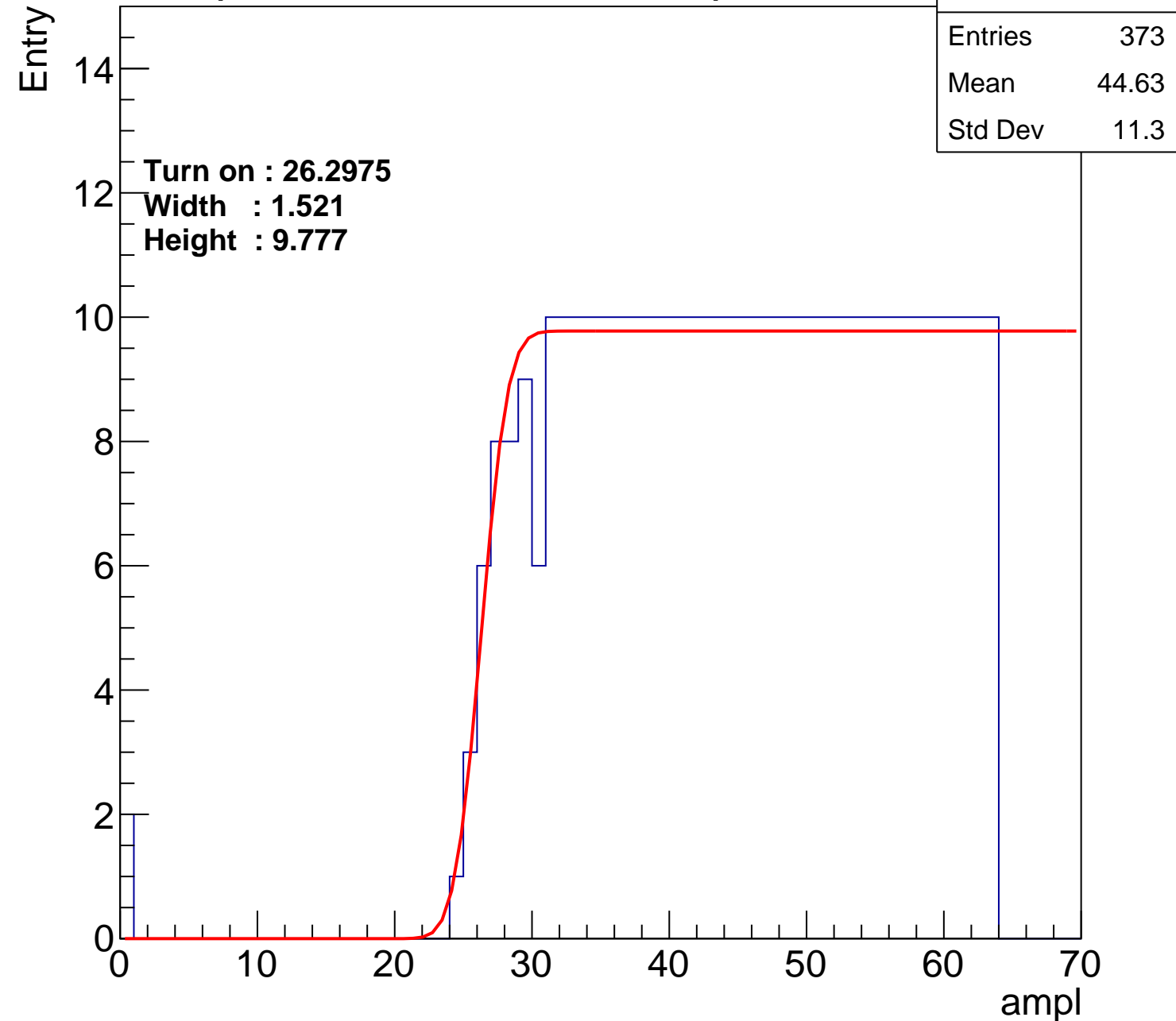
Width : 1.521

Height : 9.777

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L003S, U7-ch15

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	364
Mean	44.98
Std Dev	11.3

Turn on : 27.4138

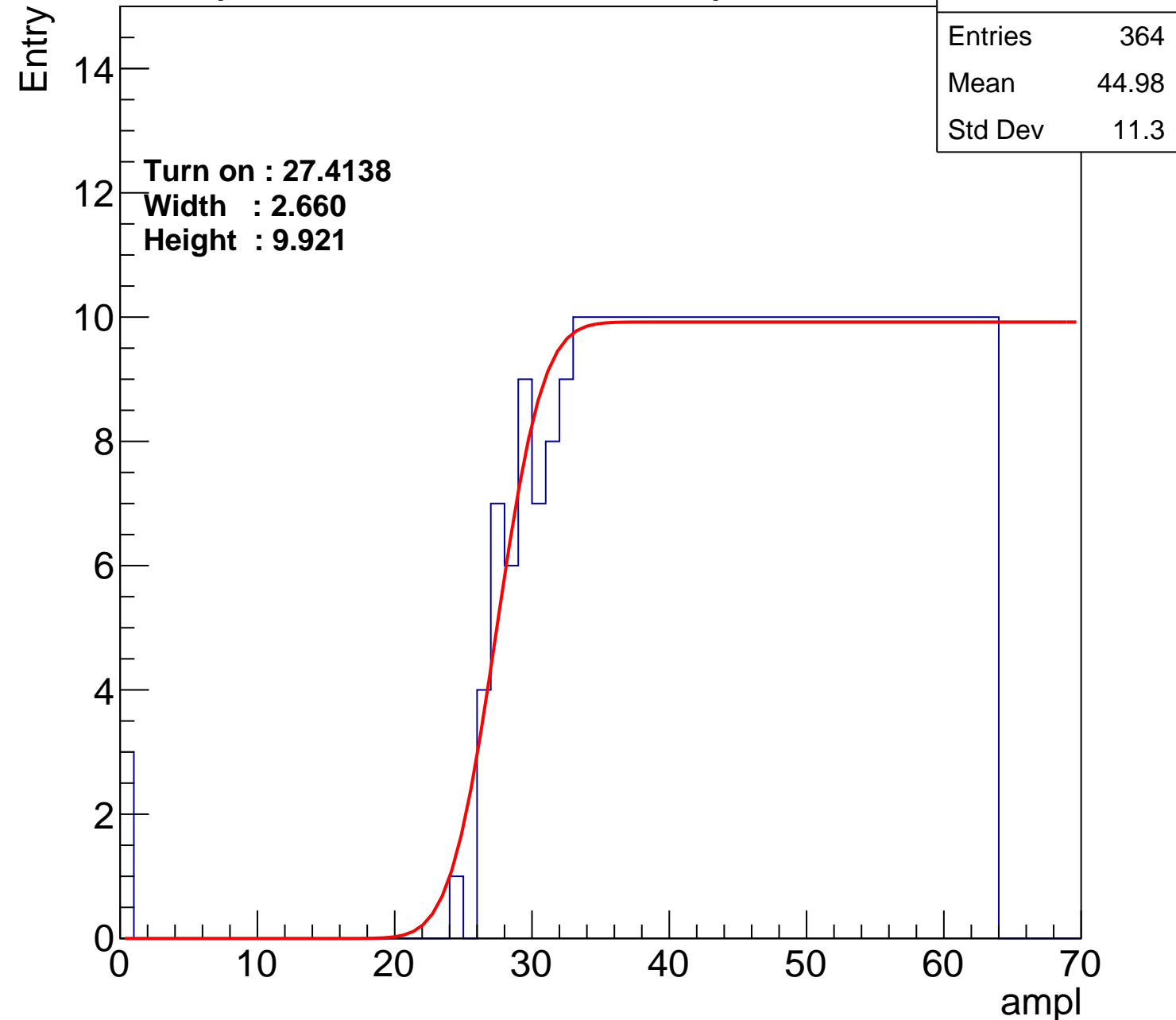
Width : 2.660

Height : 9.921

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch16

calib\_packv5\_042523\_0143.root, FC#13, port D2

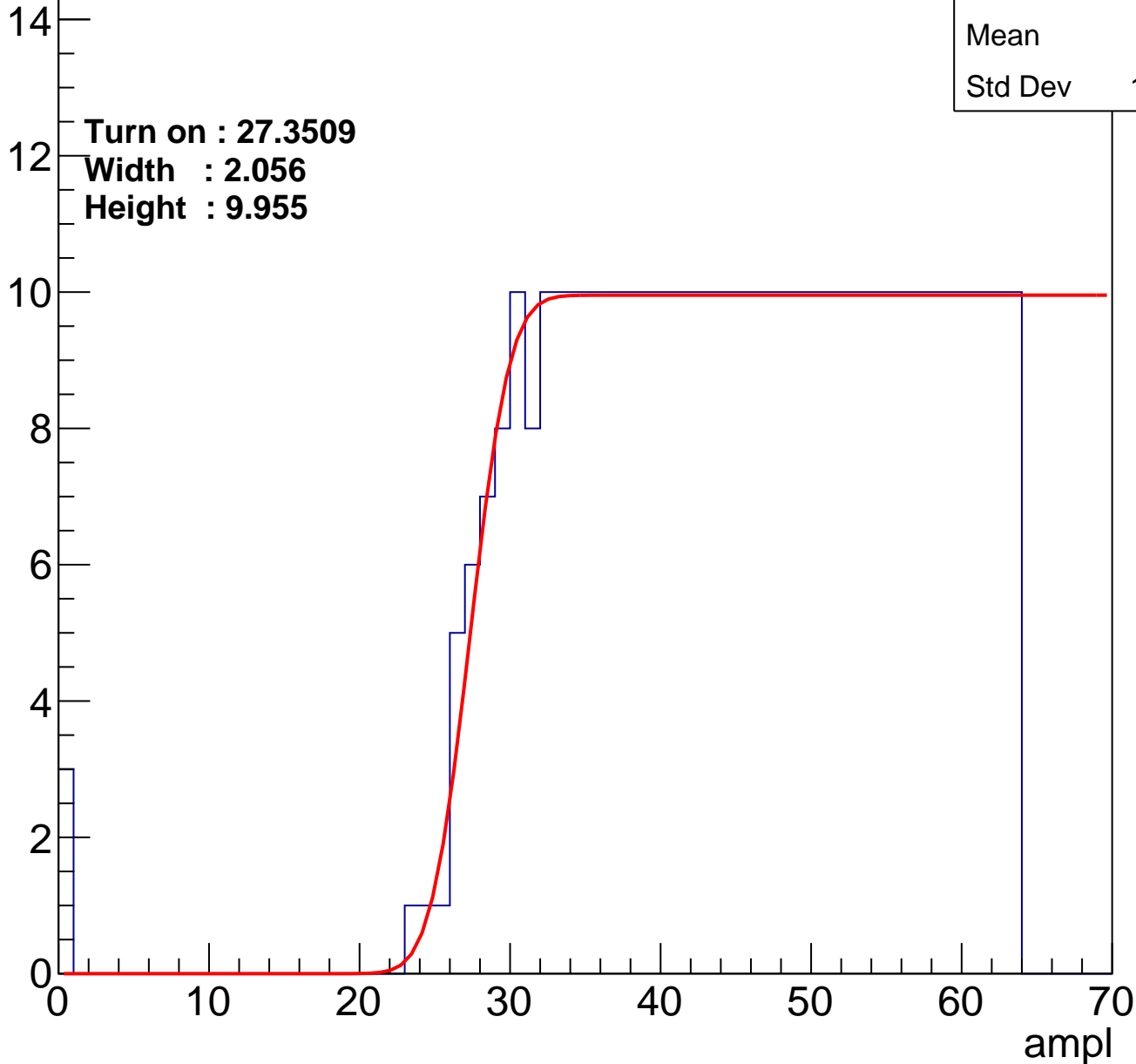
Entry

Entries	370
Mean	44.7
Std Dev	11.42

Turn on : 27.3509

Width : 2.056

Height : 9.955



# B1L003S, U7-ch17

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	359
Mean	45.38
Std Dev	10.75

Turn on : 27.9470

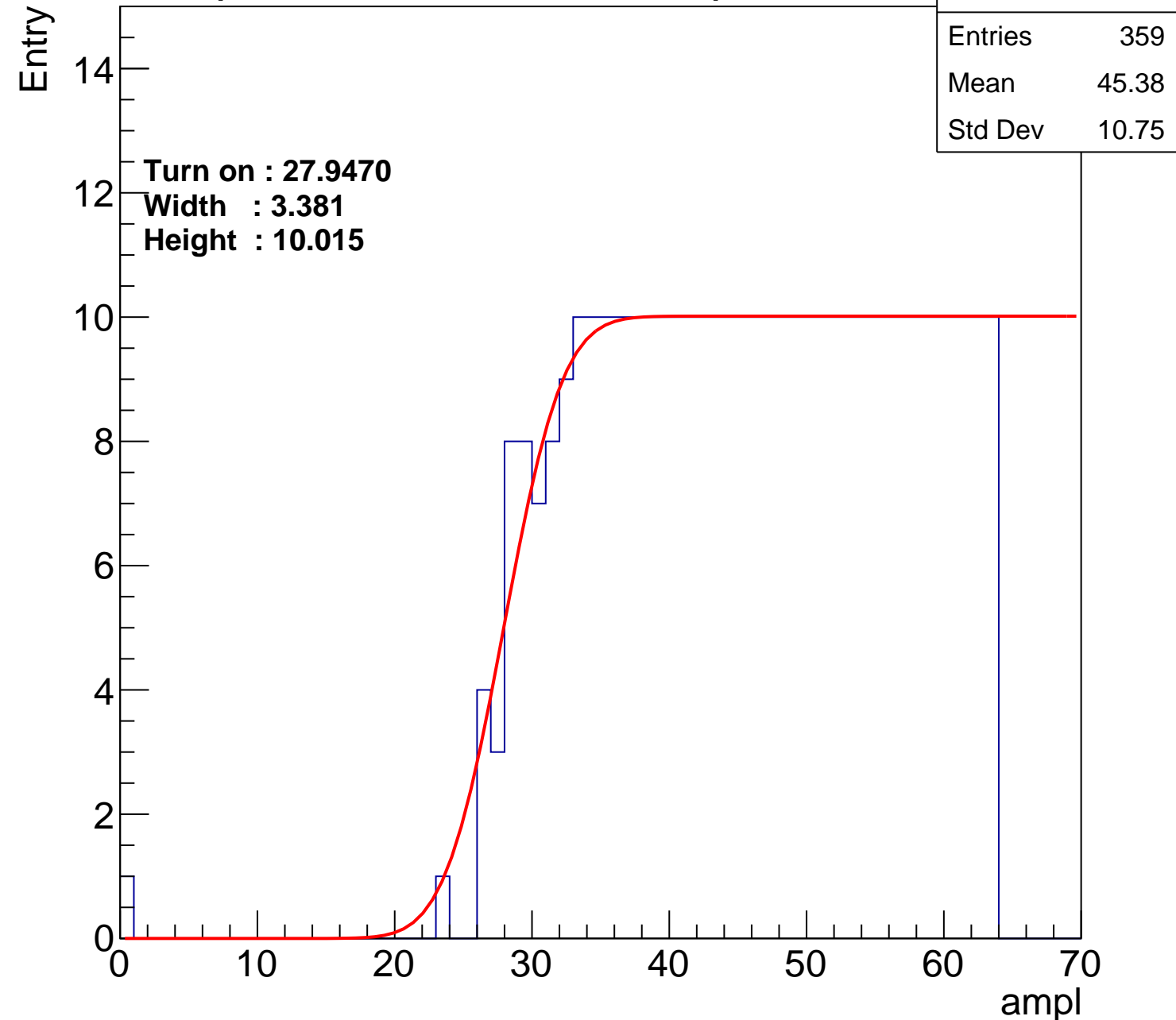
Width : 3.381

Height : 10.015

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch18

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	365
Mean	45
Std Dev	11.13

Turn on : 28.7112

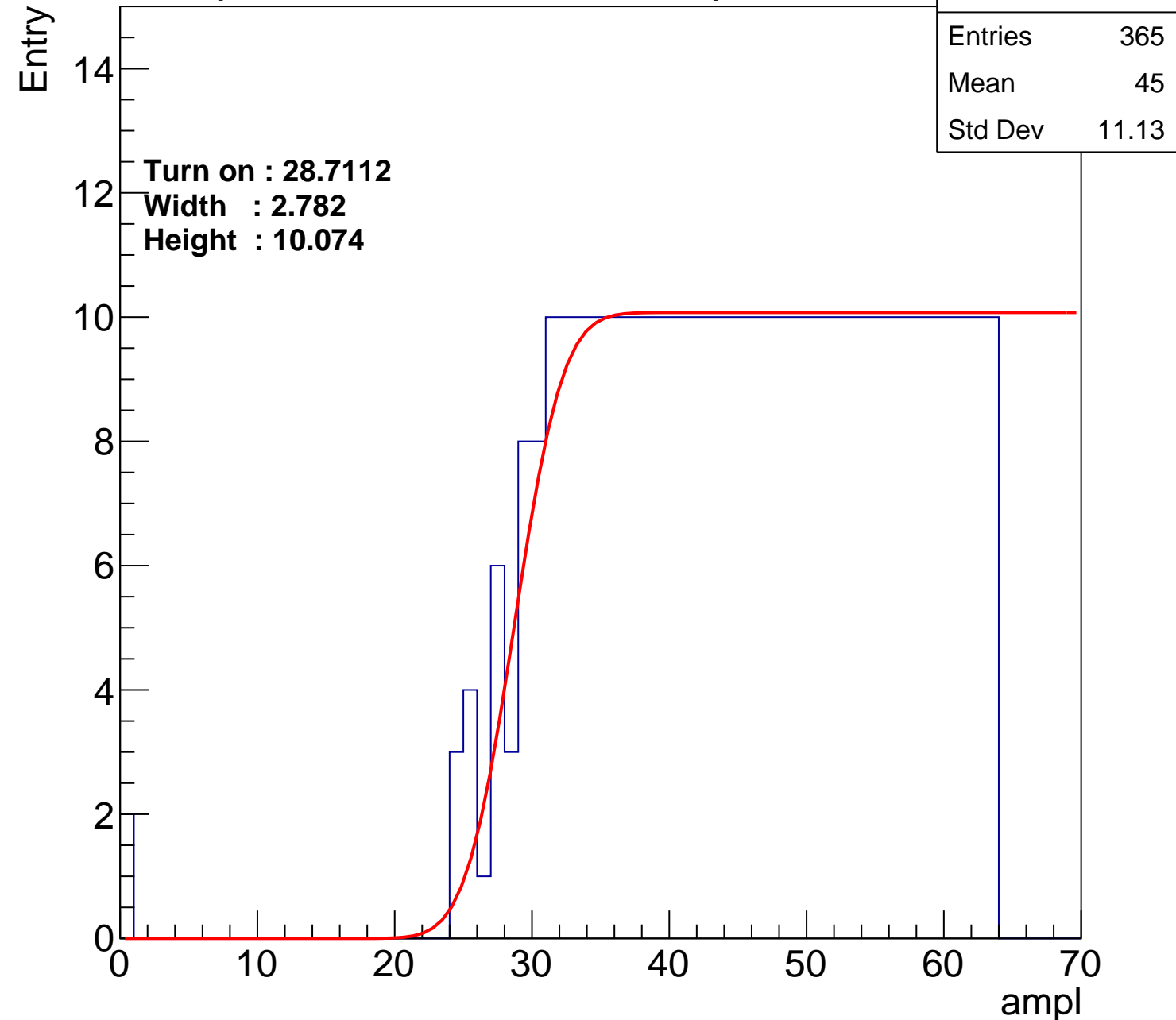
Width : 2.782

Height : 10.074

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch19

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	357
Mean	45.29
Std Dev	11.2

**Turn on : 28.8605**

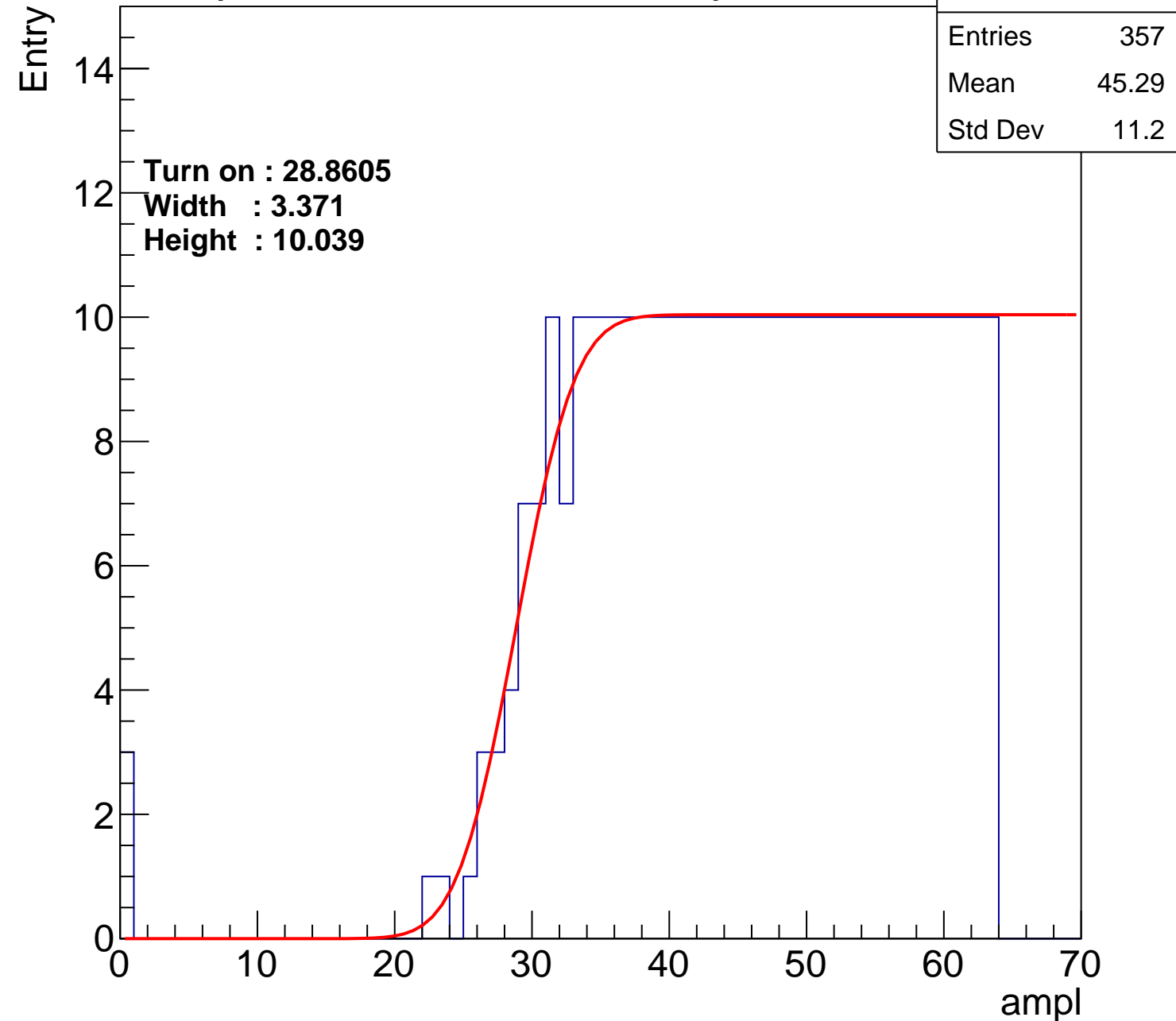
**Width : 3.371**

**Height : 10.039**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch20

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	376
Mean	44.41
Std Dev	11.57

**Turn on : 26.9572**

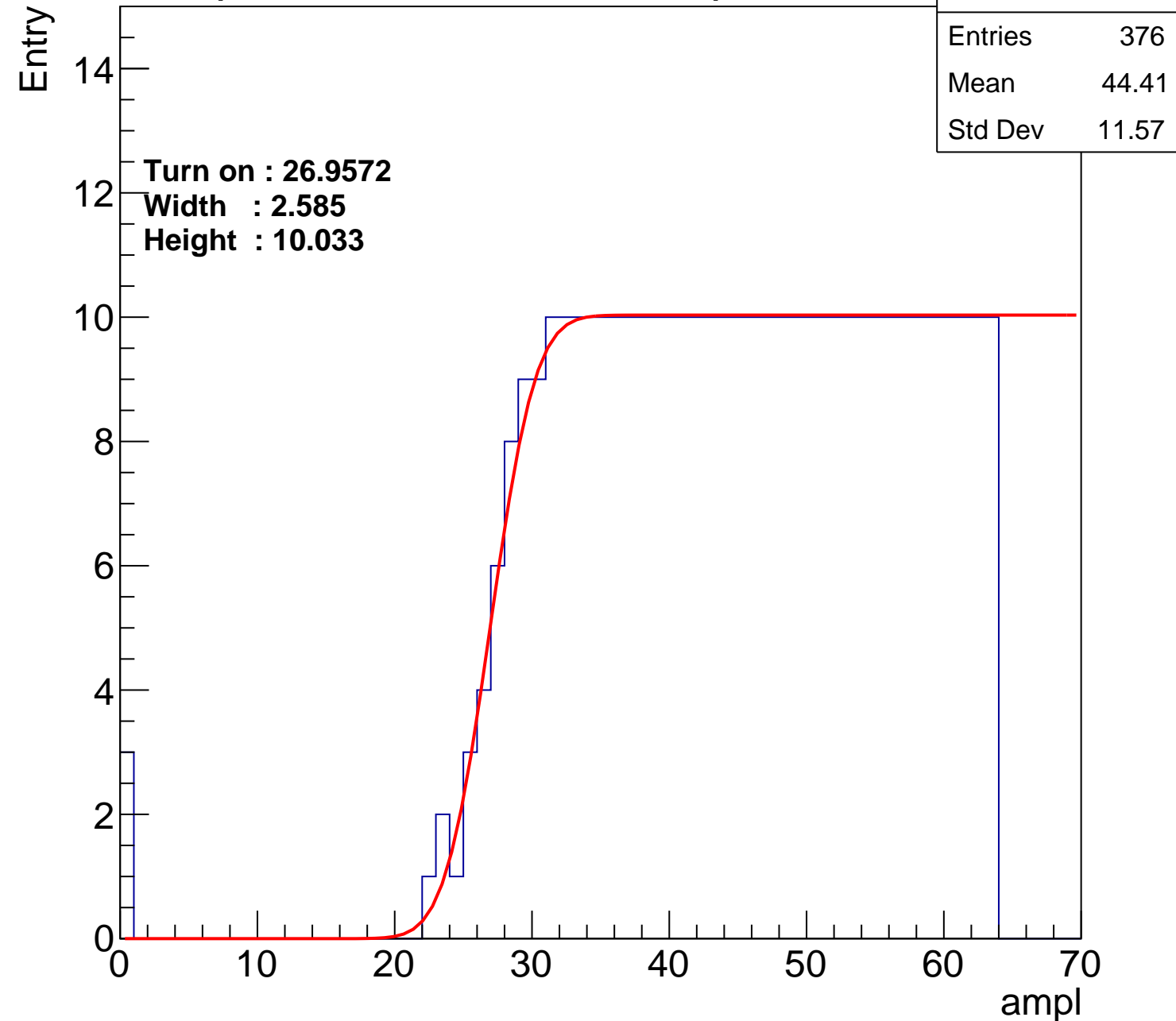
**Width : 2.585**

**Height : 10.033**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch21

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	363
Mean	45.1
Std Dev	11.07

Turn on : 27.9921

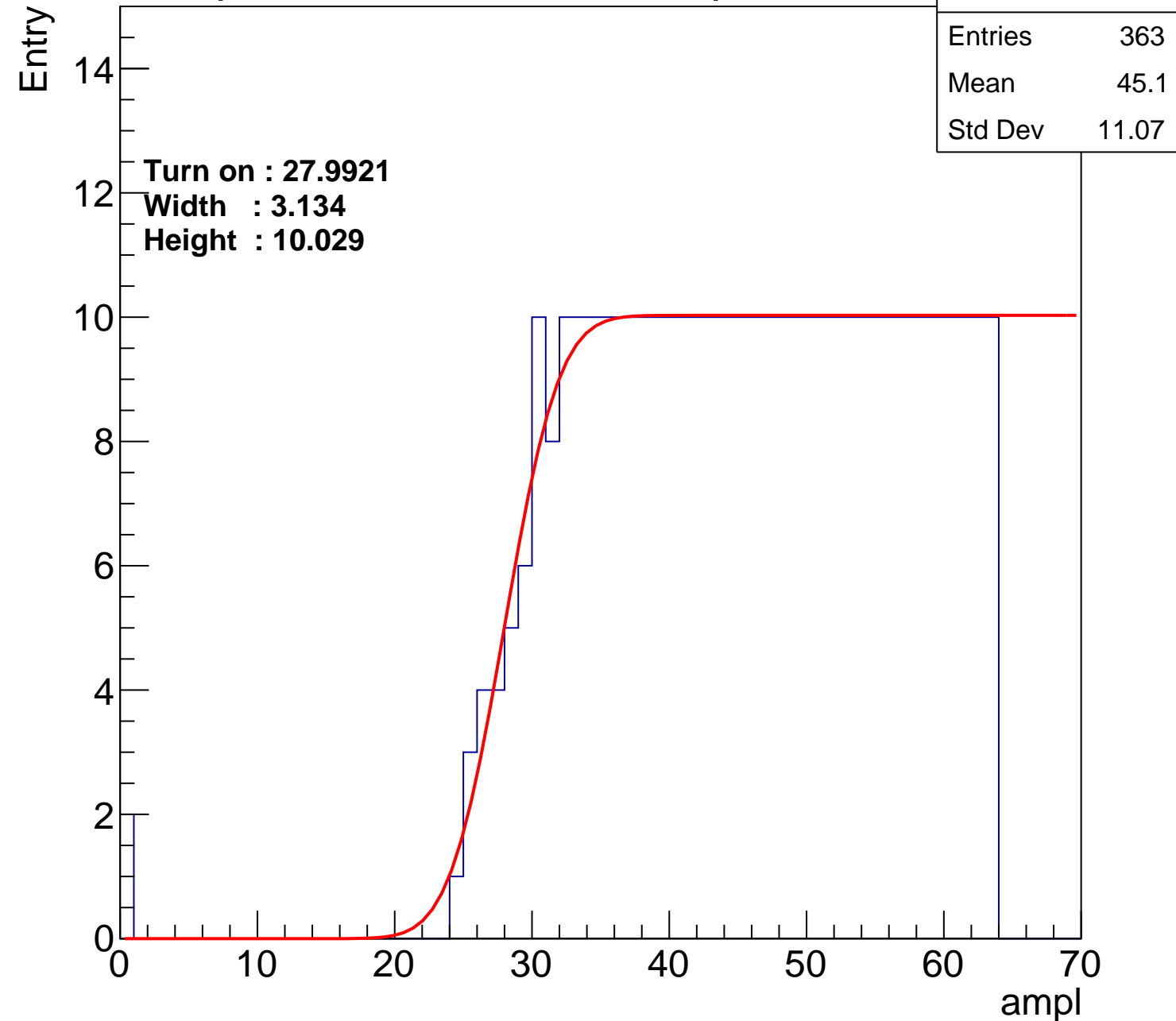
Width : 3.134

Height : 10.029

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch22

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	382
Mean	44.03
Std Dev	11.92

**Turn on : 26.8879**

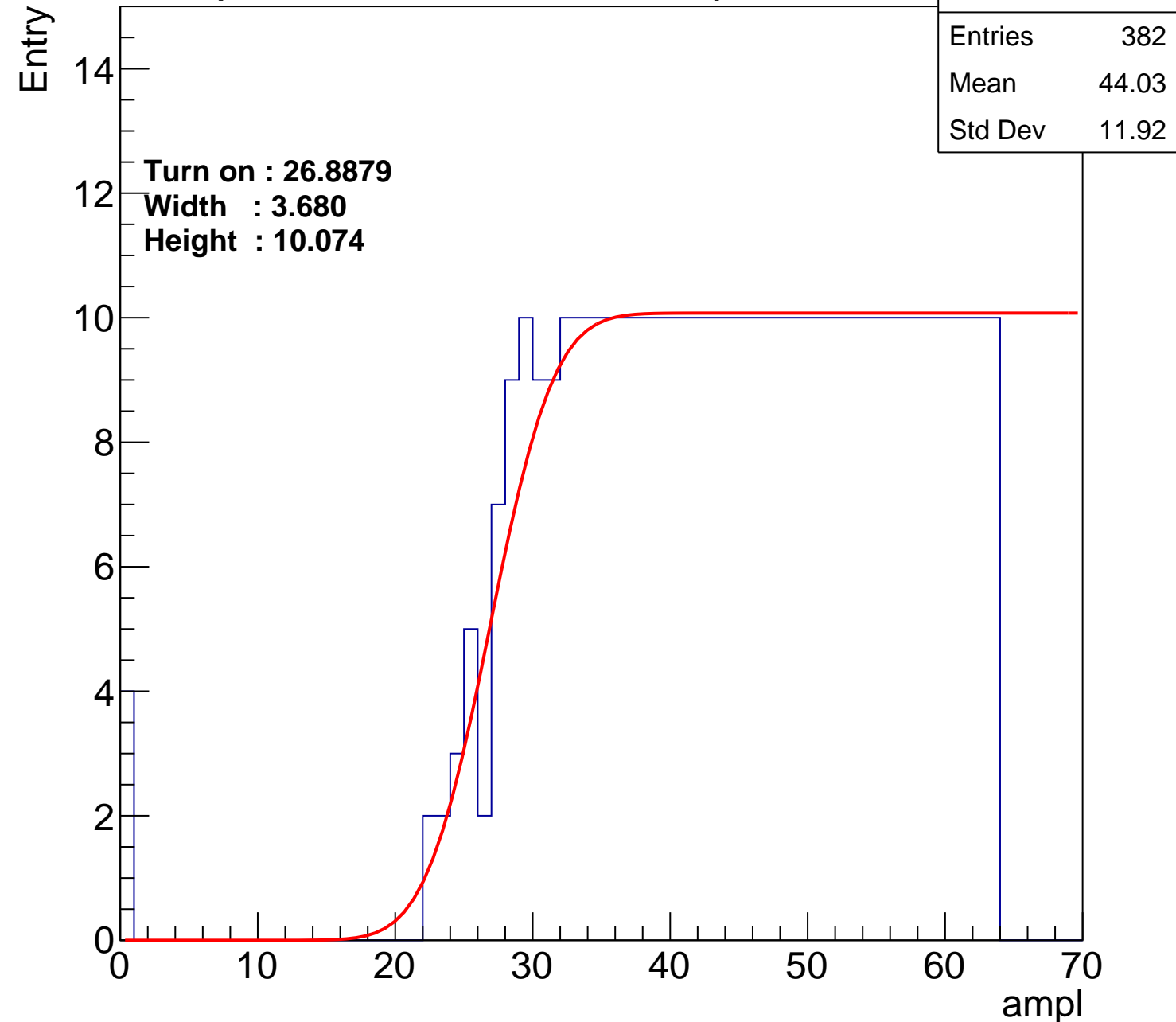
**Width : 3.680**

**Height : 10.074**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L003S, U7-ch23

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	375
Mean	44.49
Std Dev	11.5

**Turn on : 27.0280**

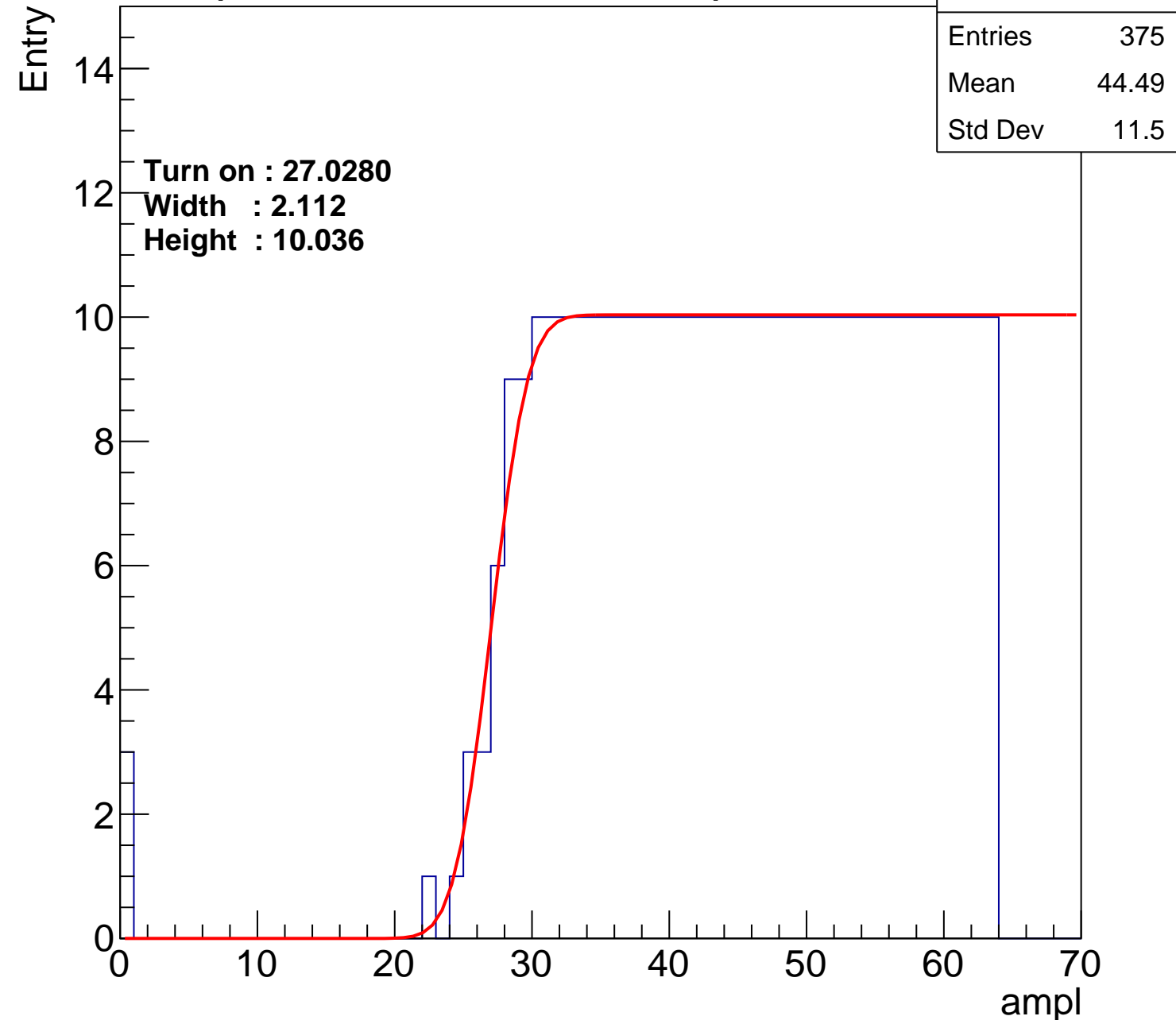
**Width : 2.112**

**Height : 10.036**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch24

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	363
Mean	44.95
Std Dev	11.49

Turn on : 28.3158

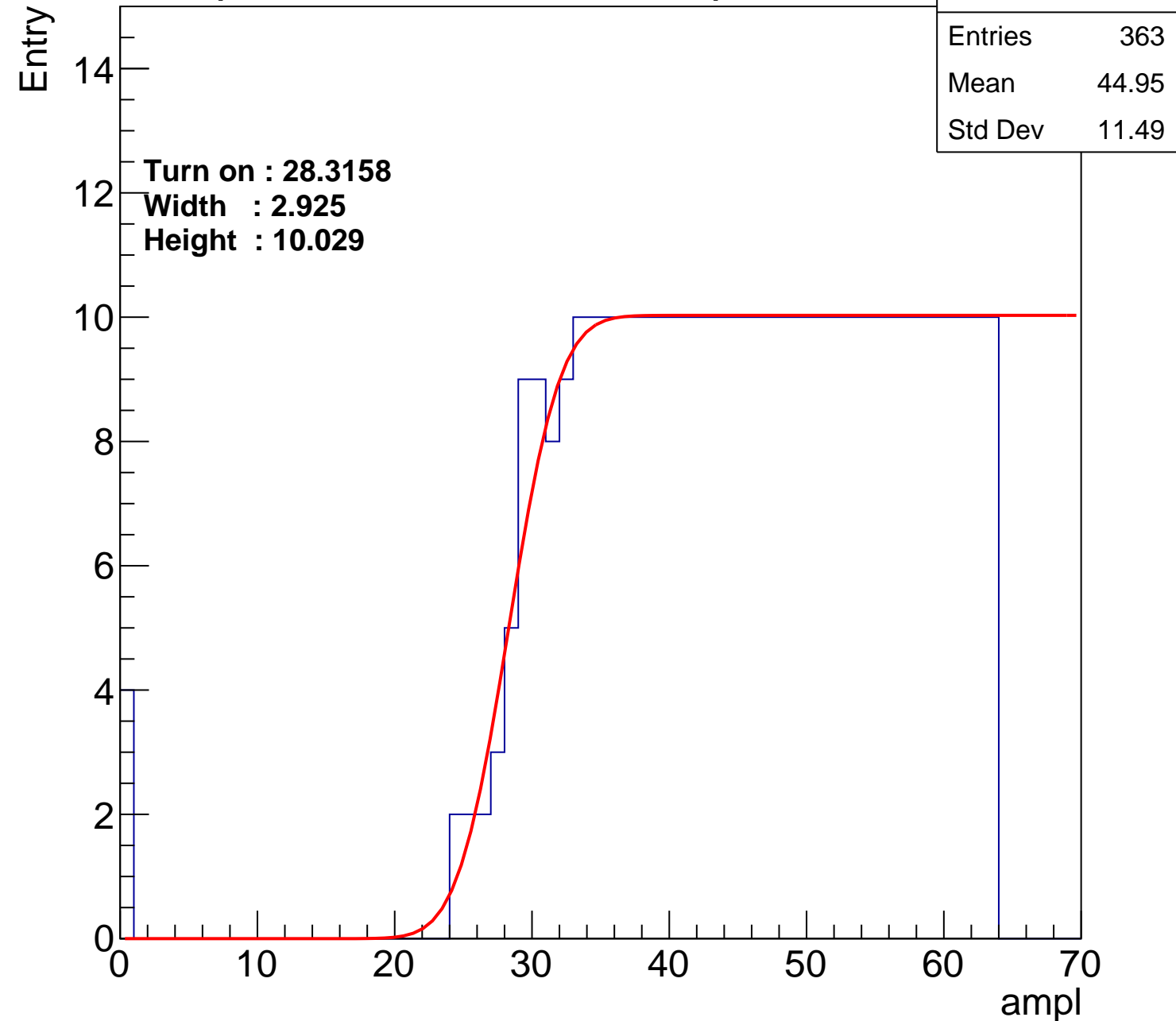
Width : 2.925

Height : 10.029

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch25

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	367
Mean	44.86
Std Dev	11.33

Turn on : 27.5297

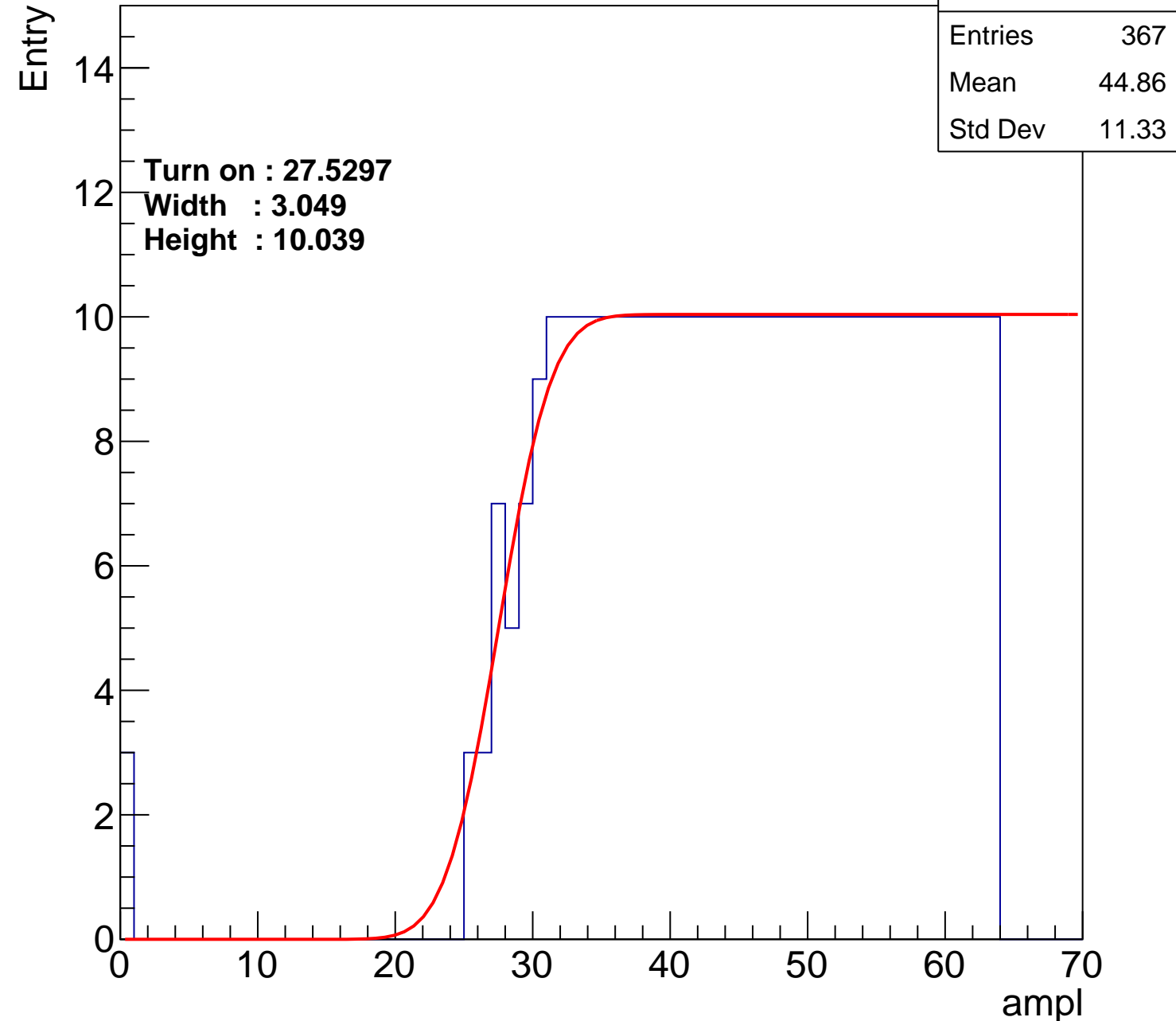
Width : 3.049

Height : 10.039

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch26

calib\_packv5\_042523\_0143.root, FC#13, port D2

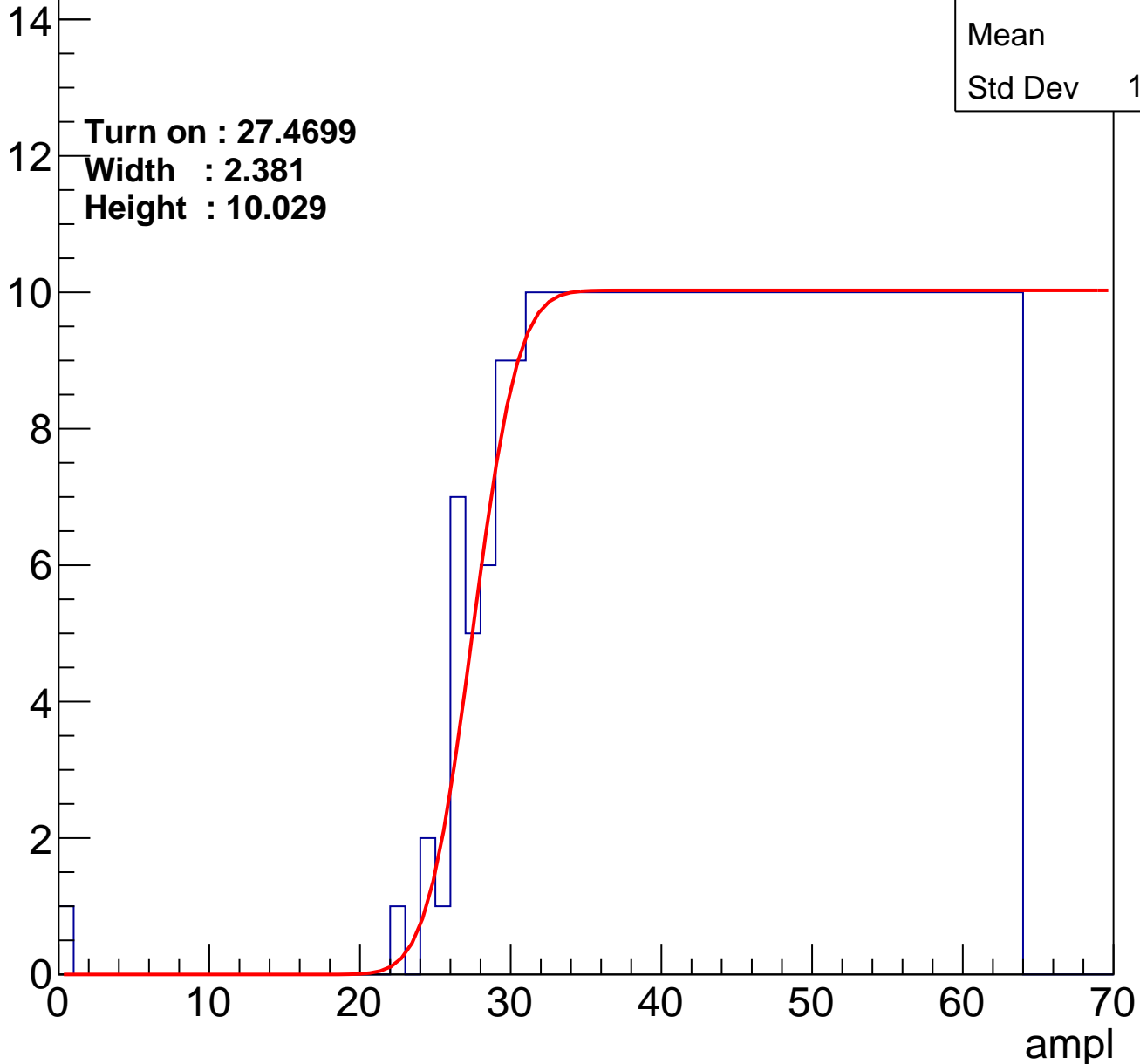
Entries	371
Mean	44.8
Std Dev	11.05

Turn on : 27.4699

Width : 2.381

Height : 10.029

Entry



# B1L003S, U7-ch27

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	375
Mean	44.54
Std Dev	11.34

Turn on : 26.8216

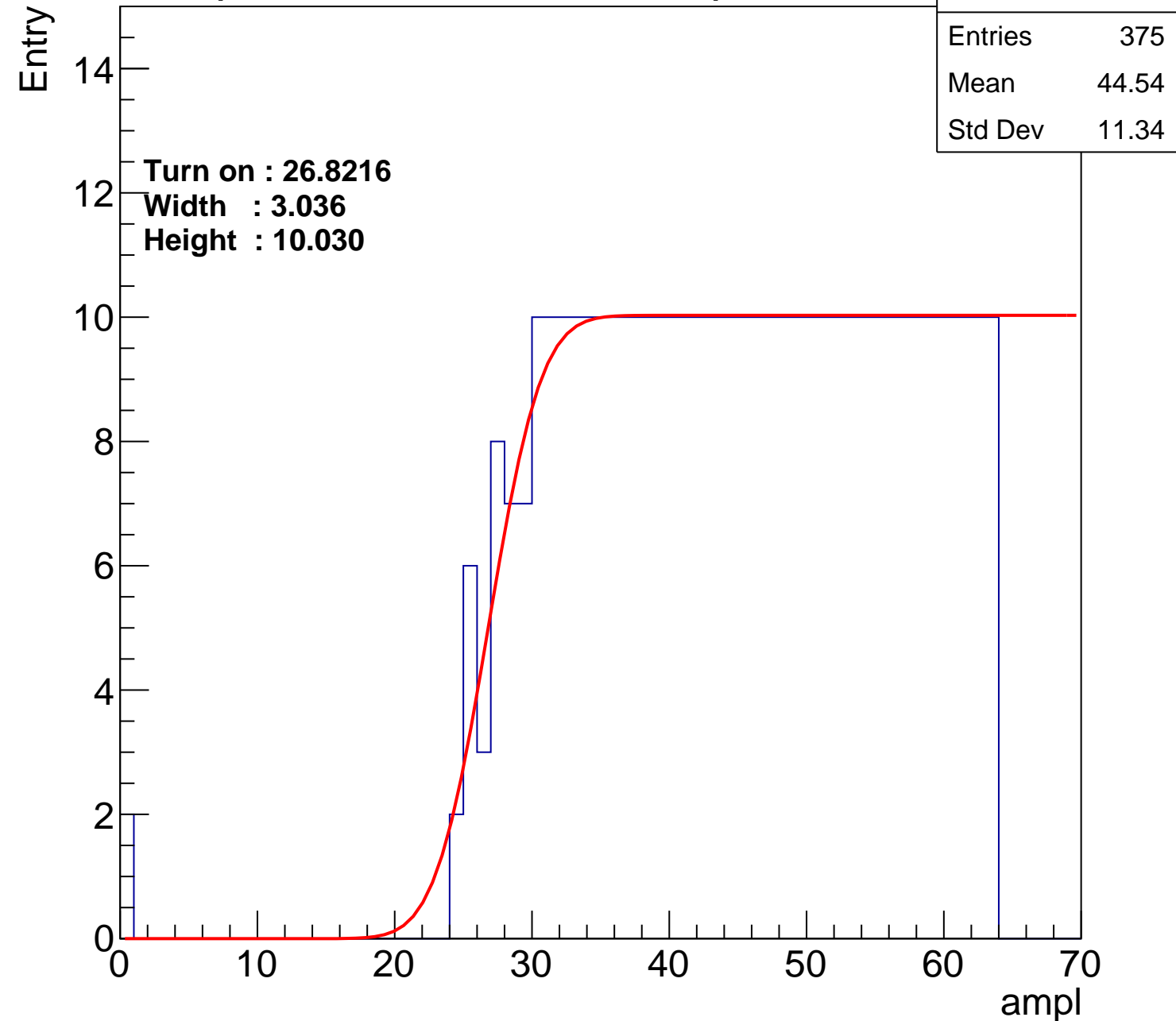
Width : 3.036

Height : 10.030

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch28

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	377
Mean	44.32
Std Dev	11.66

**Turn on : 27.0307**

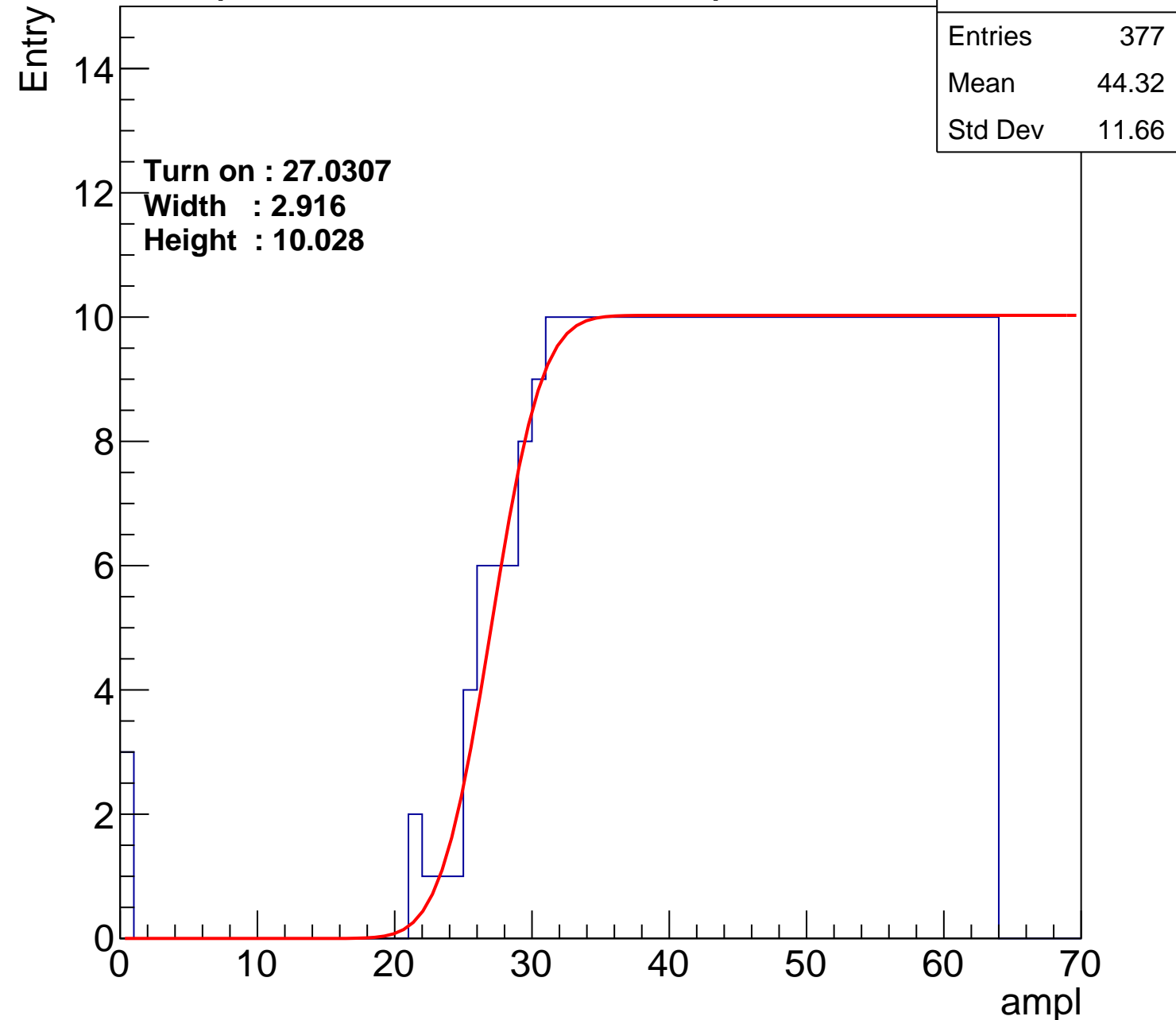
**Width : 2.916**

**Height : 10.028**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch29

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	370
Mean	44.86
Std Dev	11

**Turn on : 27.7507**

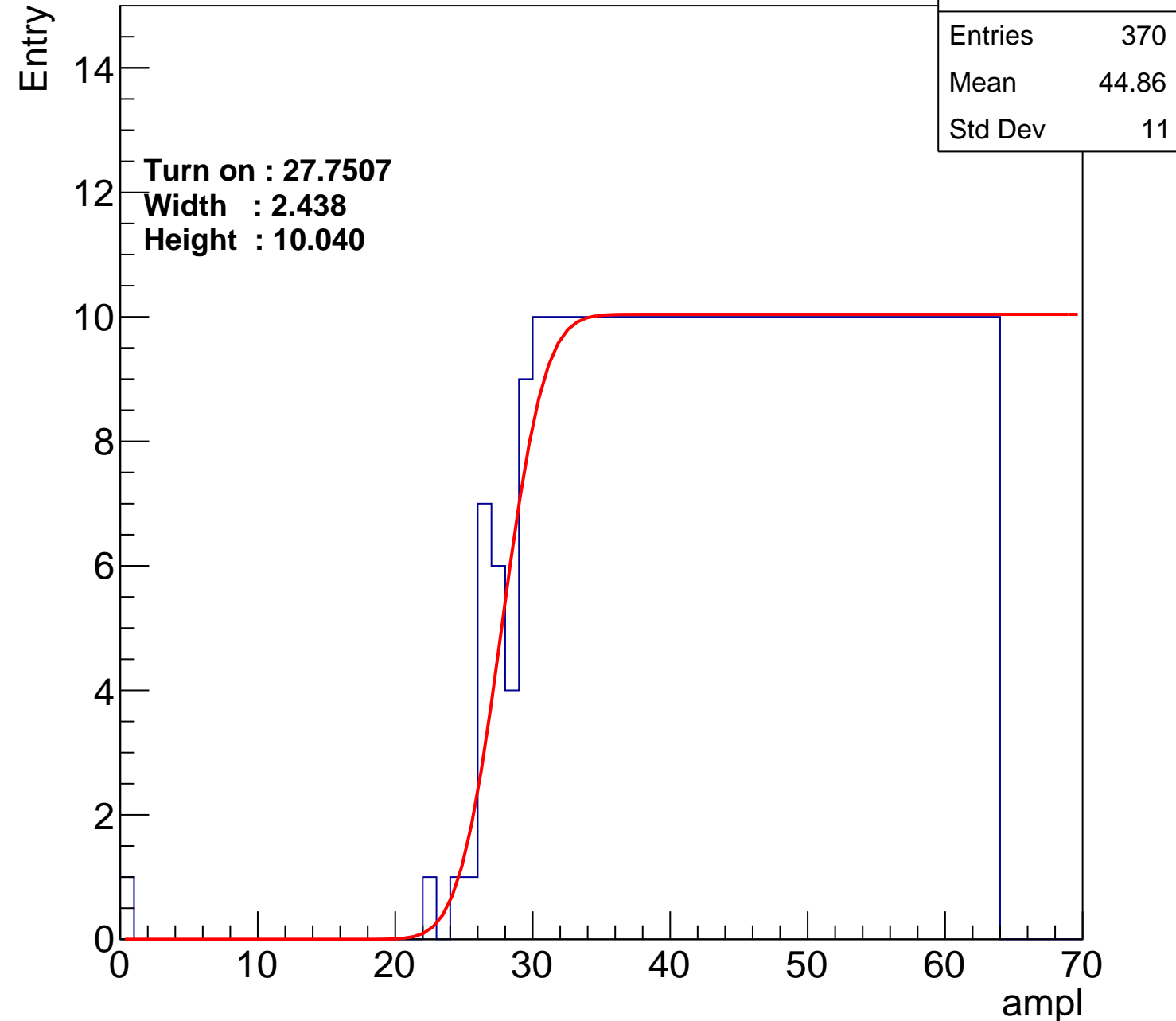
**Width : 2.438**

**Height : 10.040**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch30

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	362
Mean	45.23
Std Dev	10.83

Turn on : 27.8505

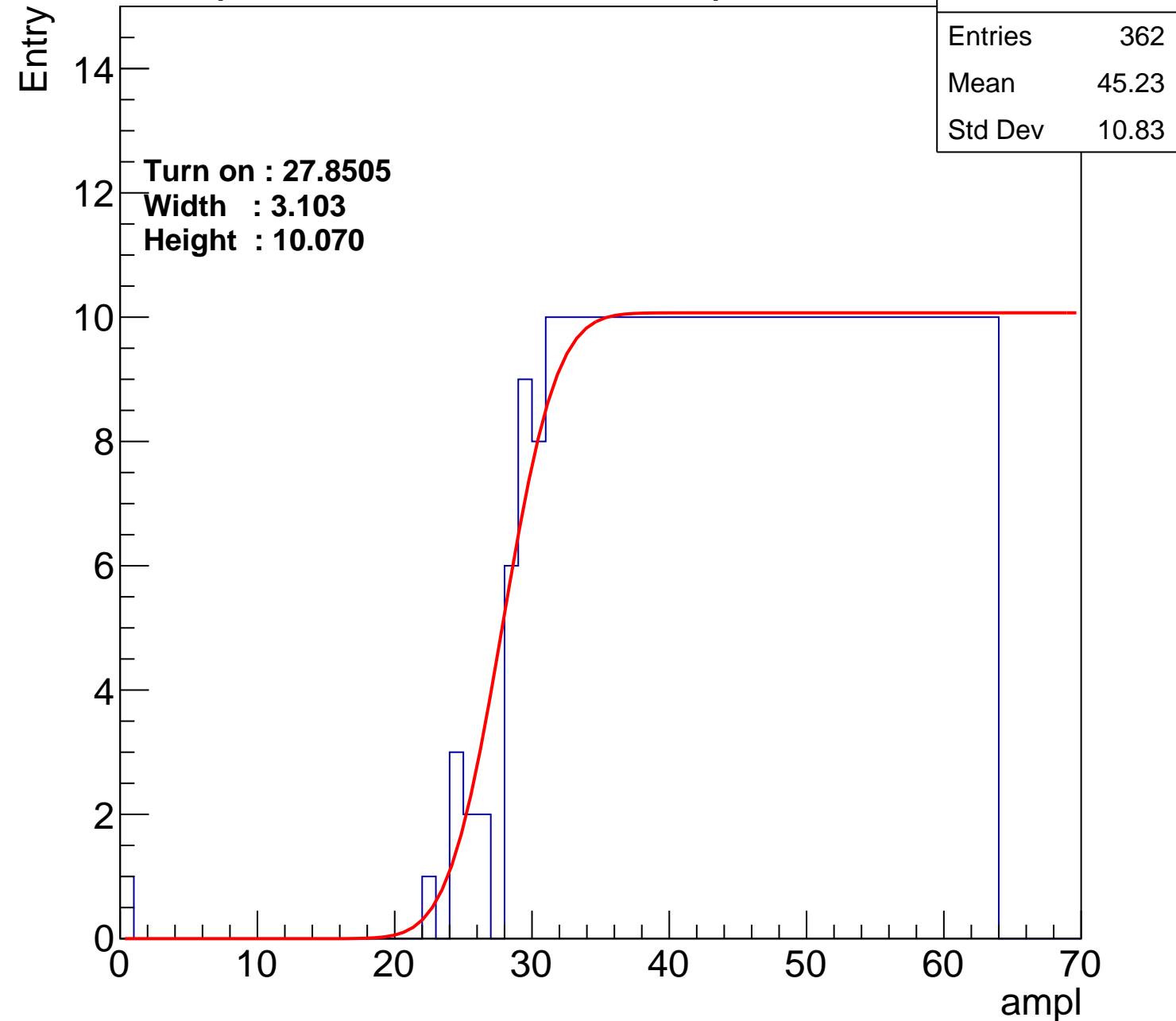
Width : 3.103

Height : 10.070

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L003S, U7-ch31

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	369
Mean	44.6
Std Dev	11.8

Turn on : 27.6563

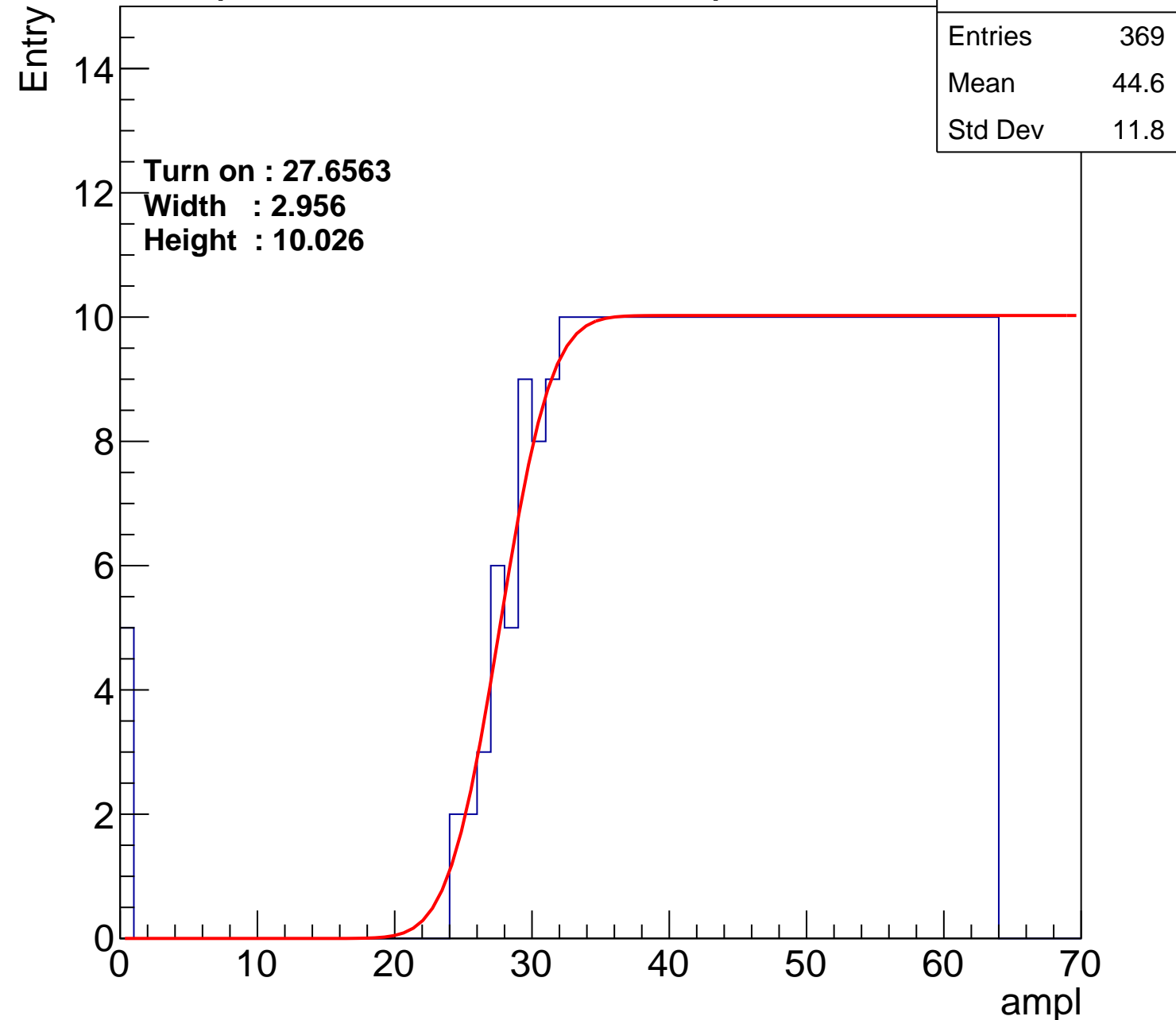
Width : 2.956

Height : 10.026

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch32

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	364
Mean	45.1
Std Dev	10.94

Turn on : 27.9293

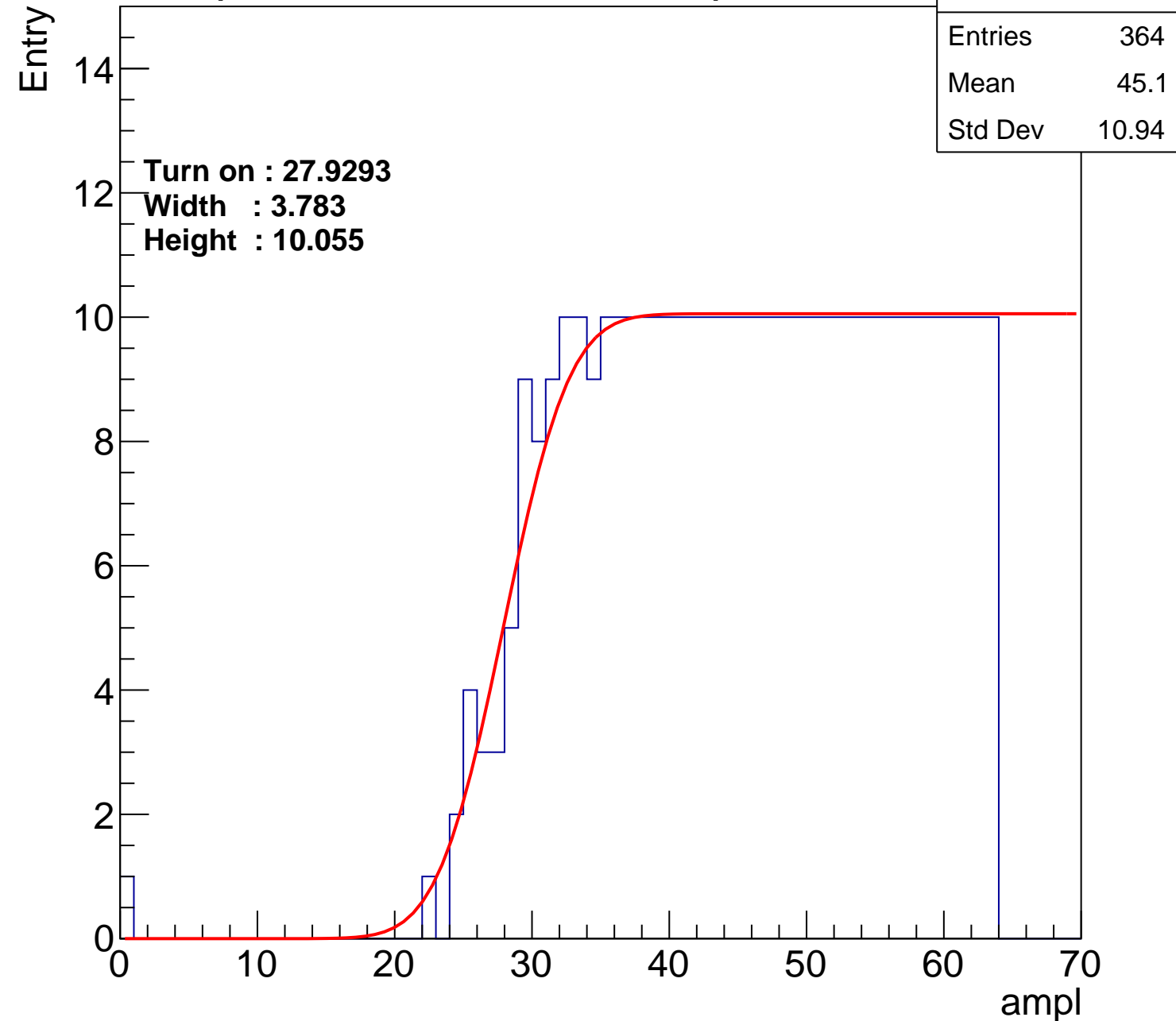
Width : 3.783

Height : 10.055

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch33

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	372
Mean	44.56
Std Dev	11.63

Turn on : 27.4108

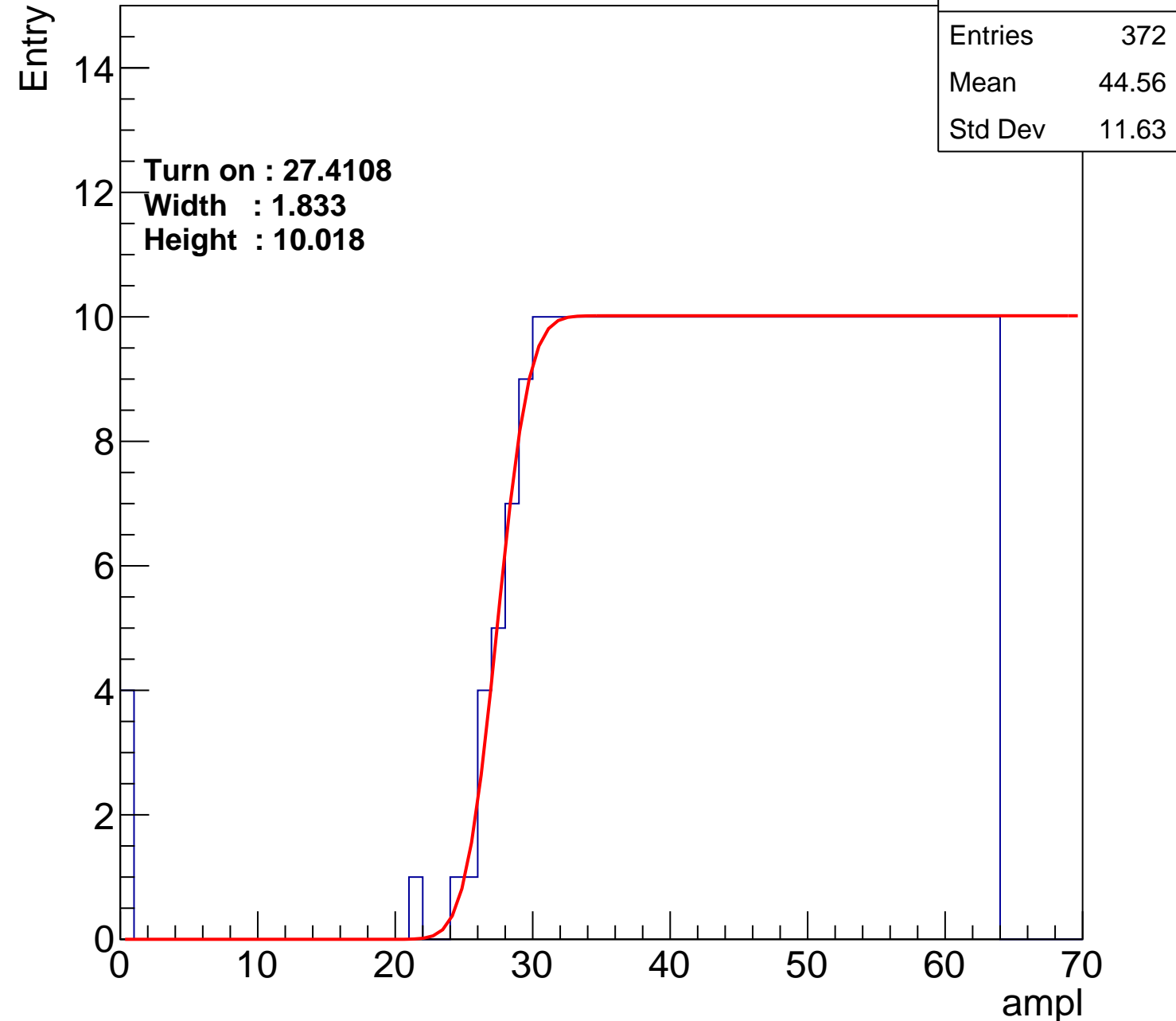
Width : 1.833

Height : 10.018

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch34

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	355
Mean	45.41
Std Dev	11.11

Turn on : 28.9799

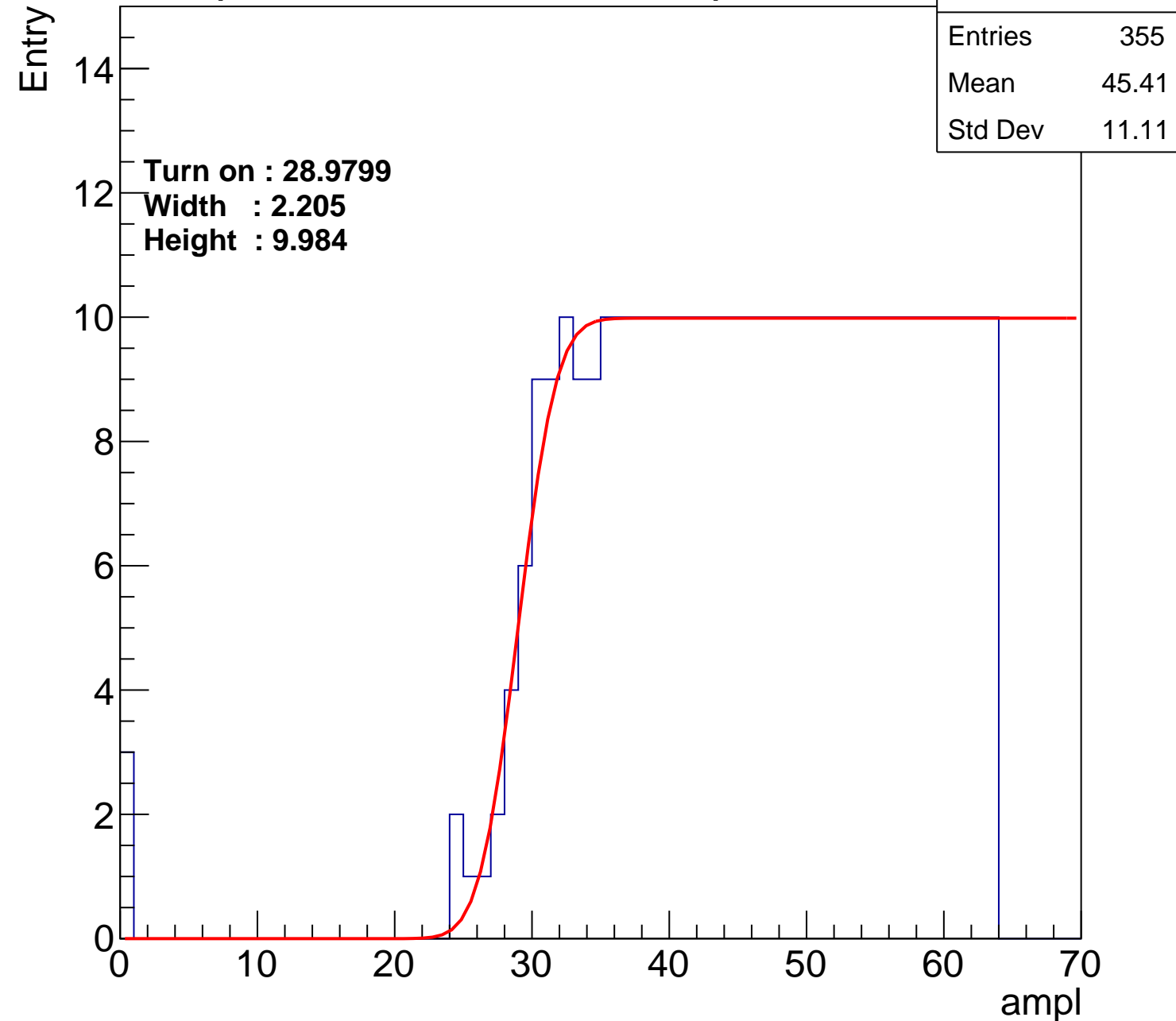
Width : 2.205

Height : 9.984

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch35

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	369
Mean	44.87
Std Dev	11.04

Turn on : 27.4740

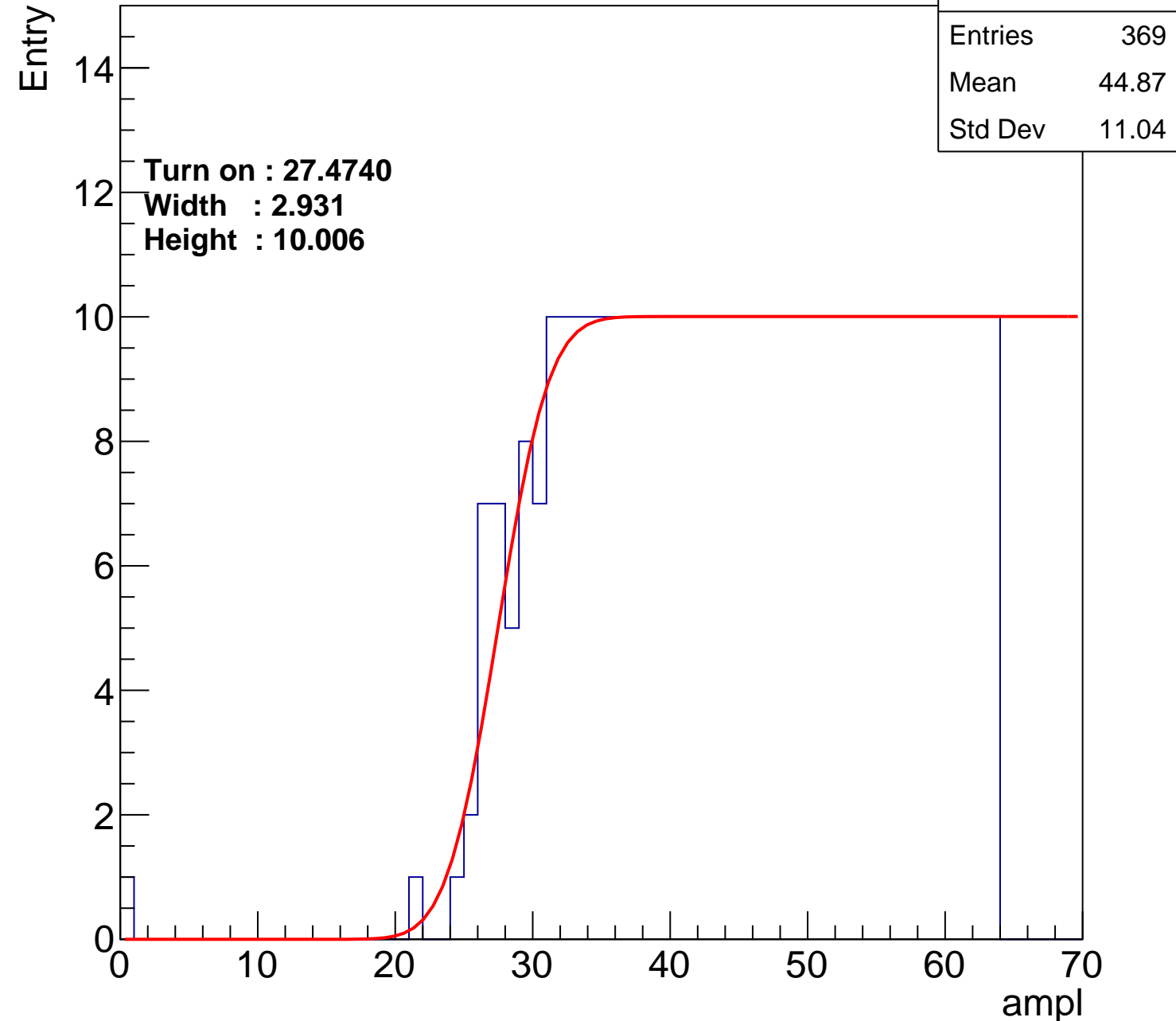
Width : 2.931

Height : 10.006

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch36

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	365
Mean	44.78
Std Dev	11.66

**Turn on : 27.7667**

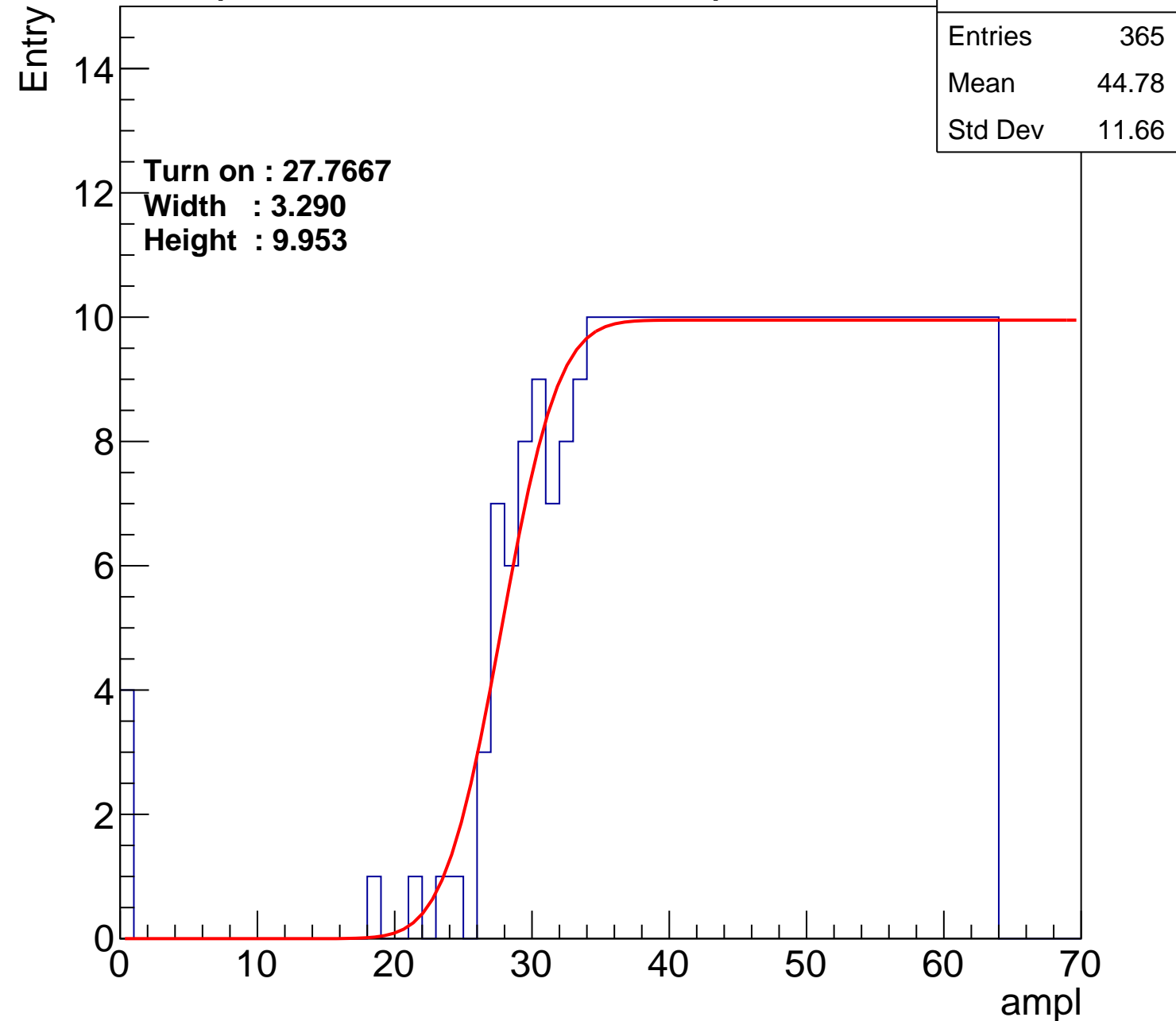
**Width : 3.290**

**Height : 9.953**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch37

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	374
Mean	44.47
Std Dev	11.57

Turn on : 27.3228

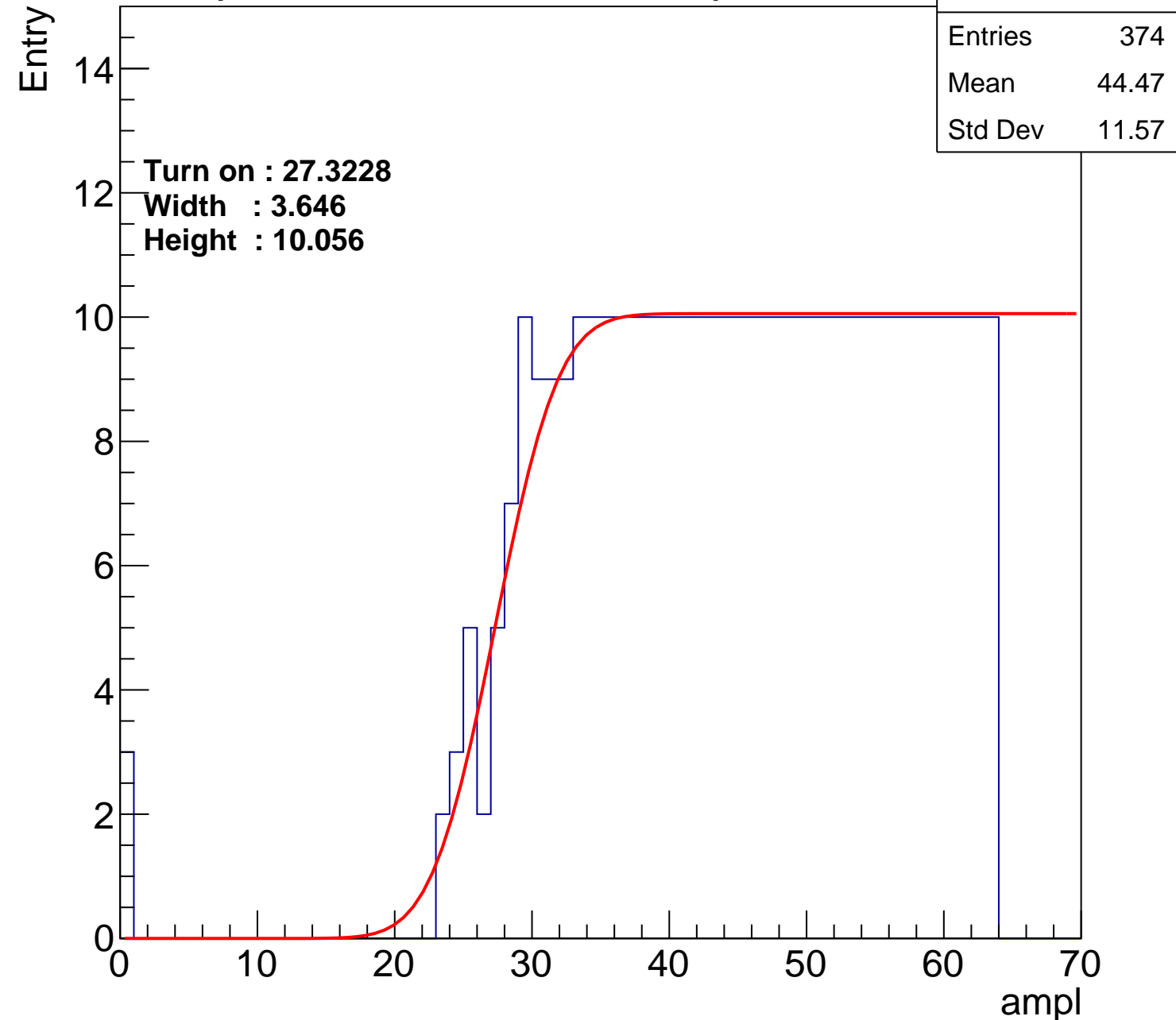
Width : 3.646

Height : 10.056

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch38

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	348
Mean	45.83
Std Dev	10.72

Turn on : 30.8395

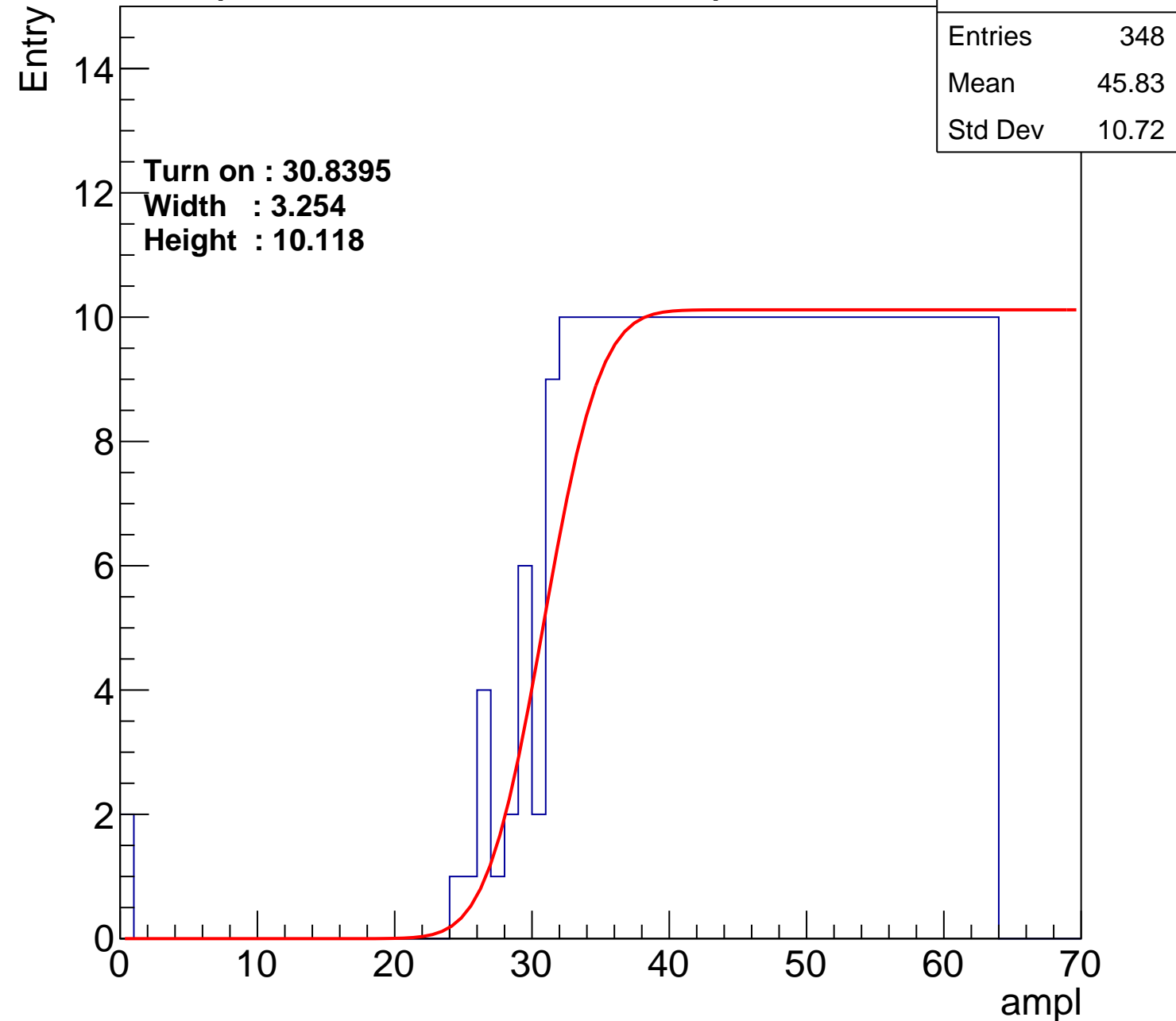
Width : 3.254

Height : 10.118

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L003S, U7-ch39

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	367
Mean	44.9
Std Dev	11.19

Turn on : 27.9883

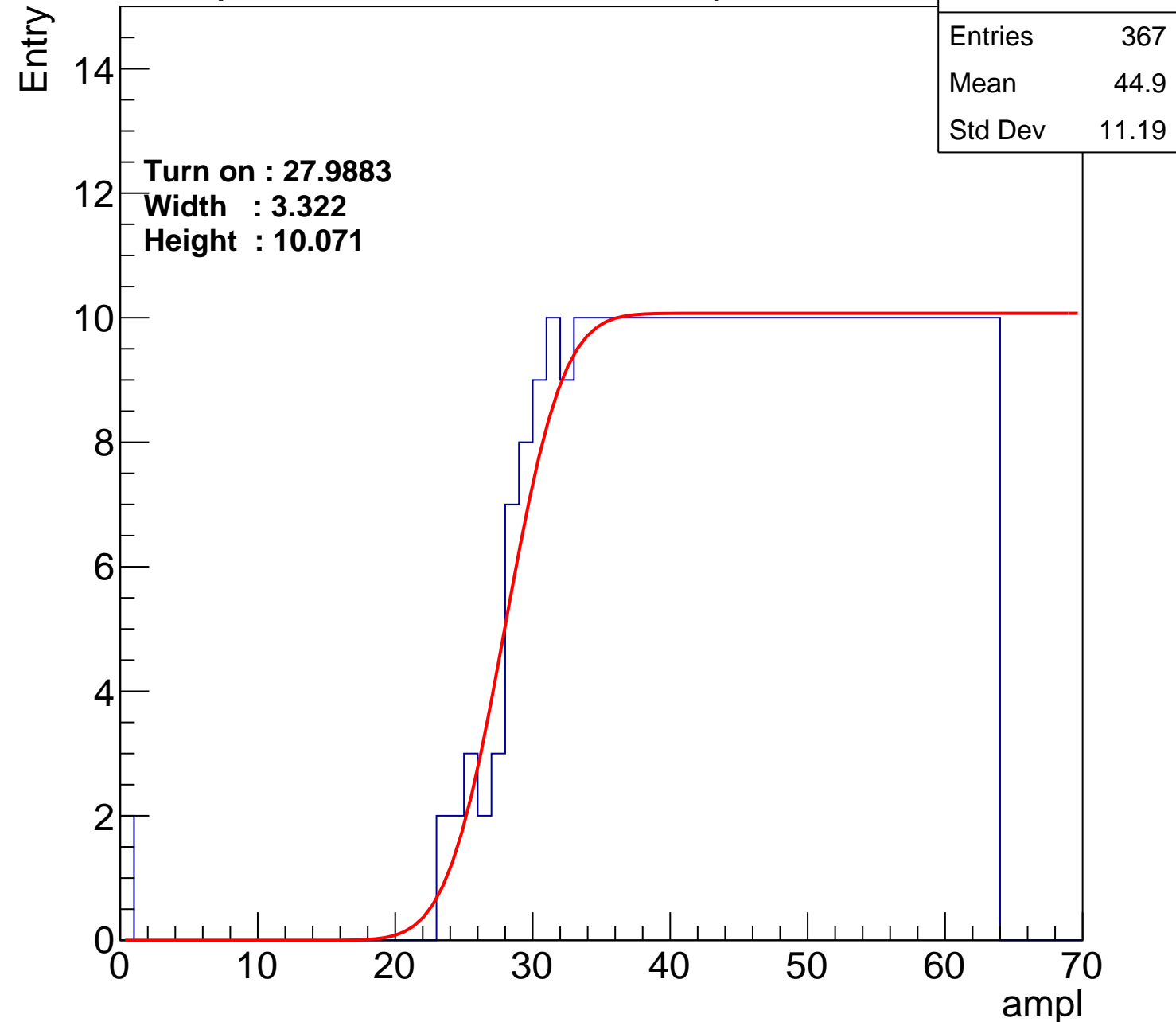
Width : 3.322

Height : 10.071

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch40

calib\_packv5\_042523\_0143.root, FC#13, port D2

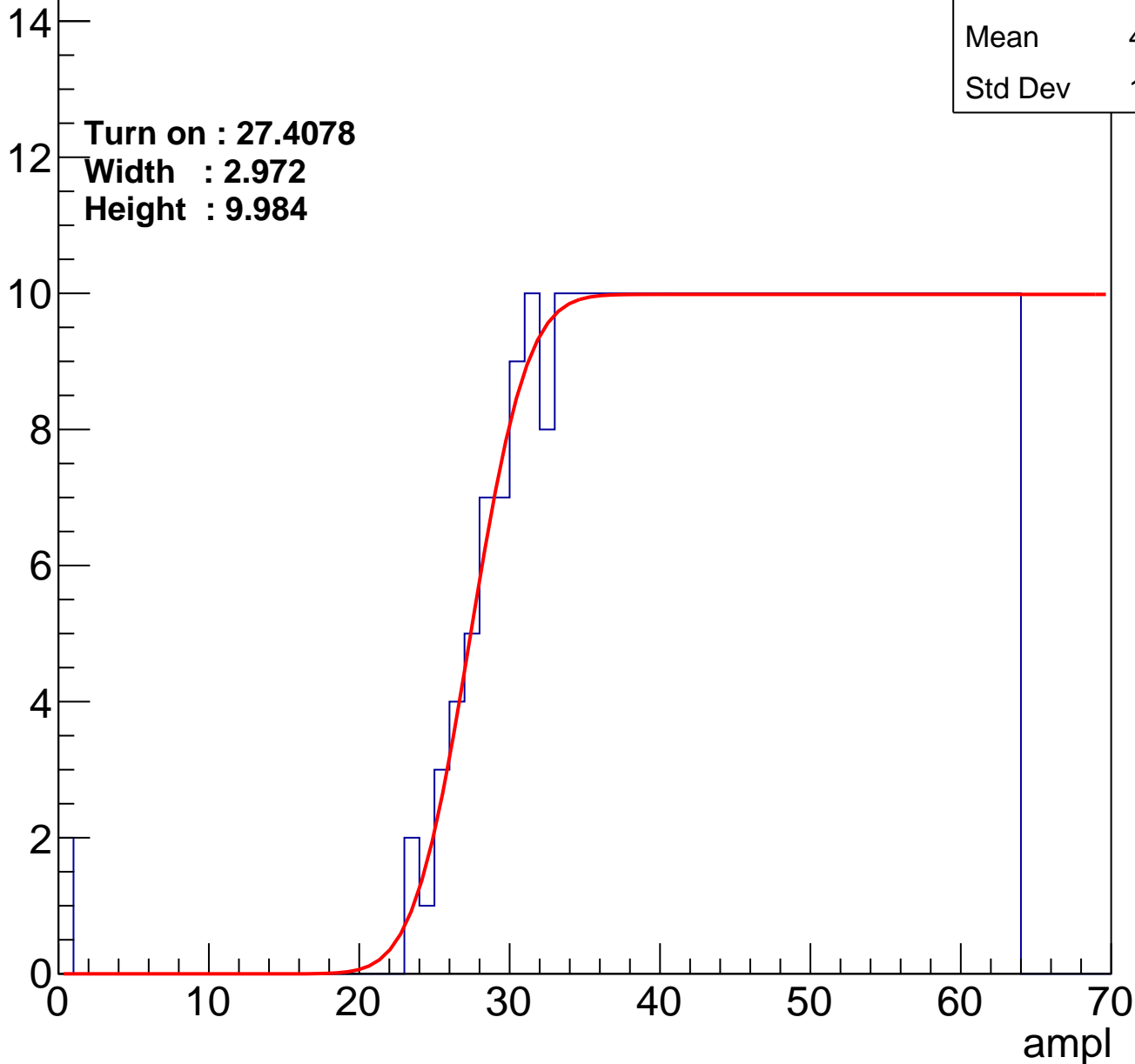
Entry

Entries	368
Mean	44.83
Std Dev	11.24

Turn on : 27.4078

Width : 2.972

Height : 9.984



# B1L003S, U7-ch41

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	383
Mean	43.83
Std Dev	12.3

Turn on : 26.6727

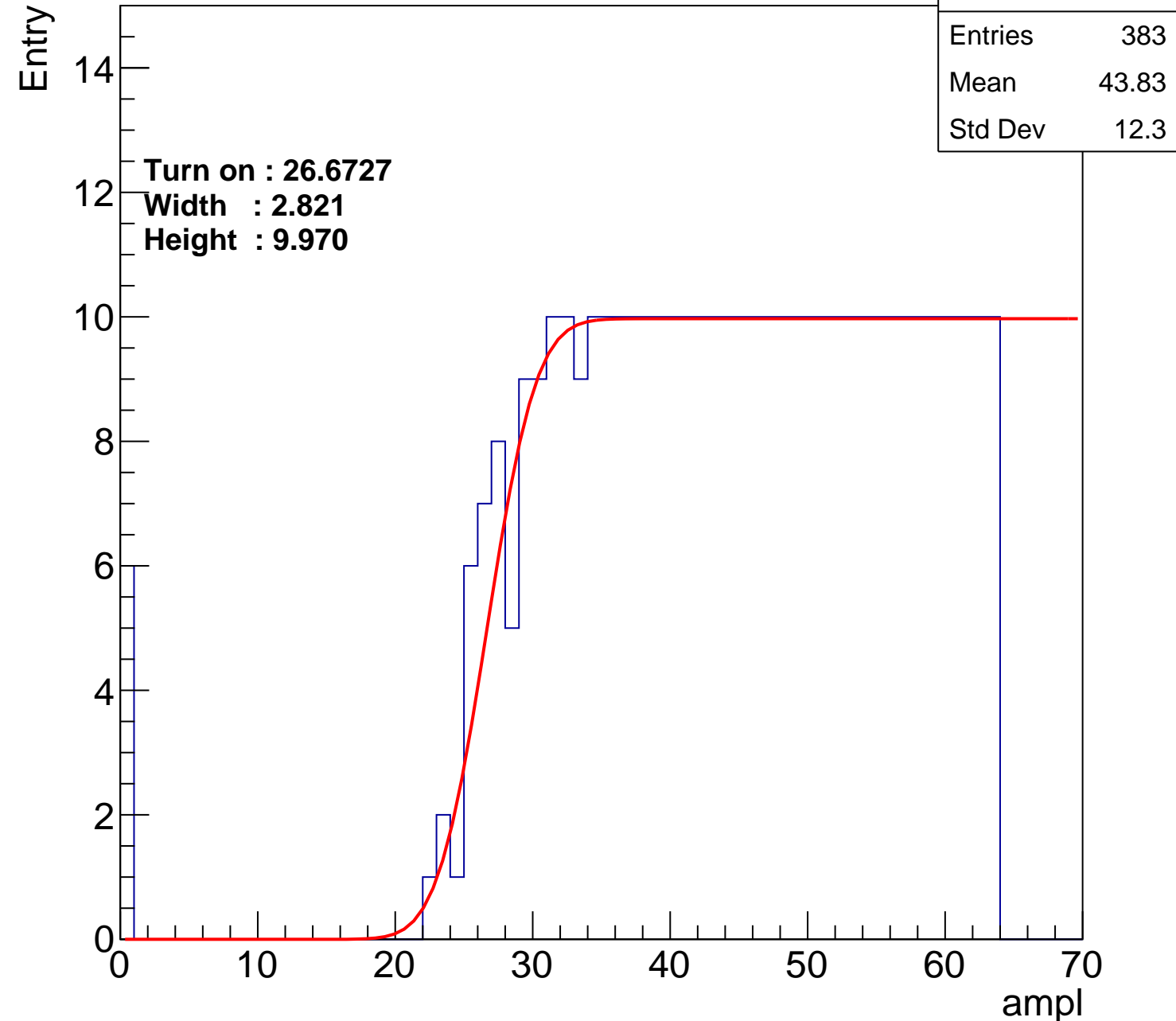
Width : 2.821

Height : 9.970

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch42

calib\_packv5\_042523\_0143.root, FC#13, port D2

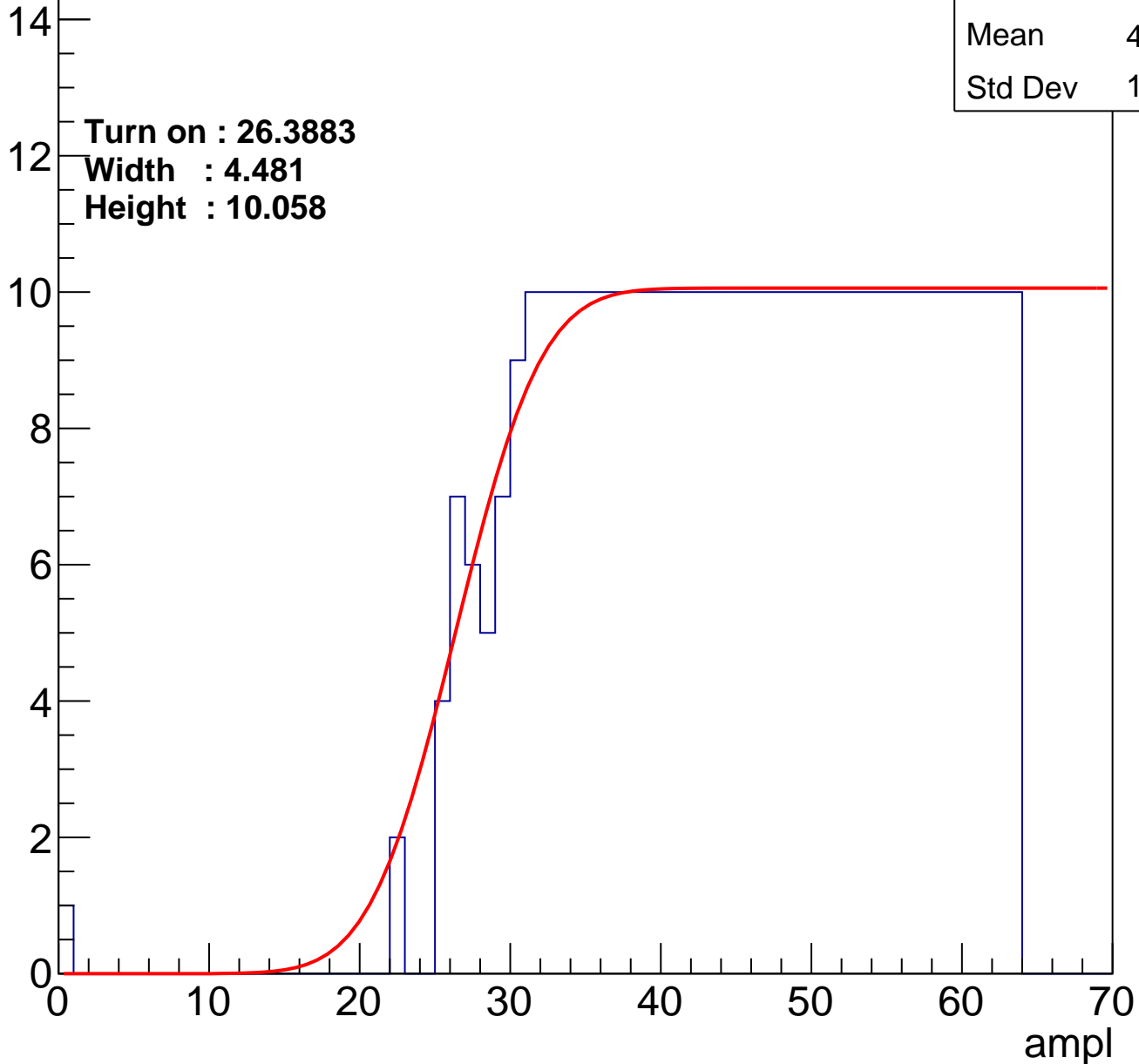
Entries	371
Mean	44.77
Std Dev	11.09

**Turn on : 26.3883**

**Width : 4.481**

**Height : 10.058**

Entry



# B1L003S, U7-ch43

calib\_packv5\_042523\_0143.root, FC#13, port D2

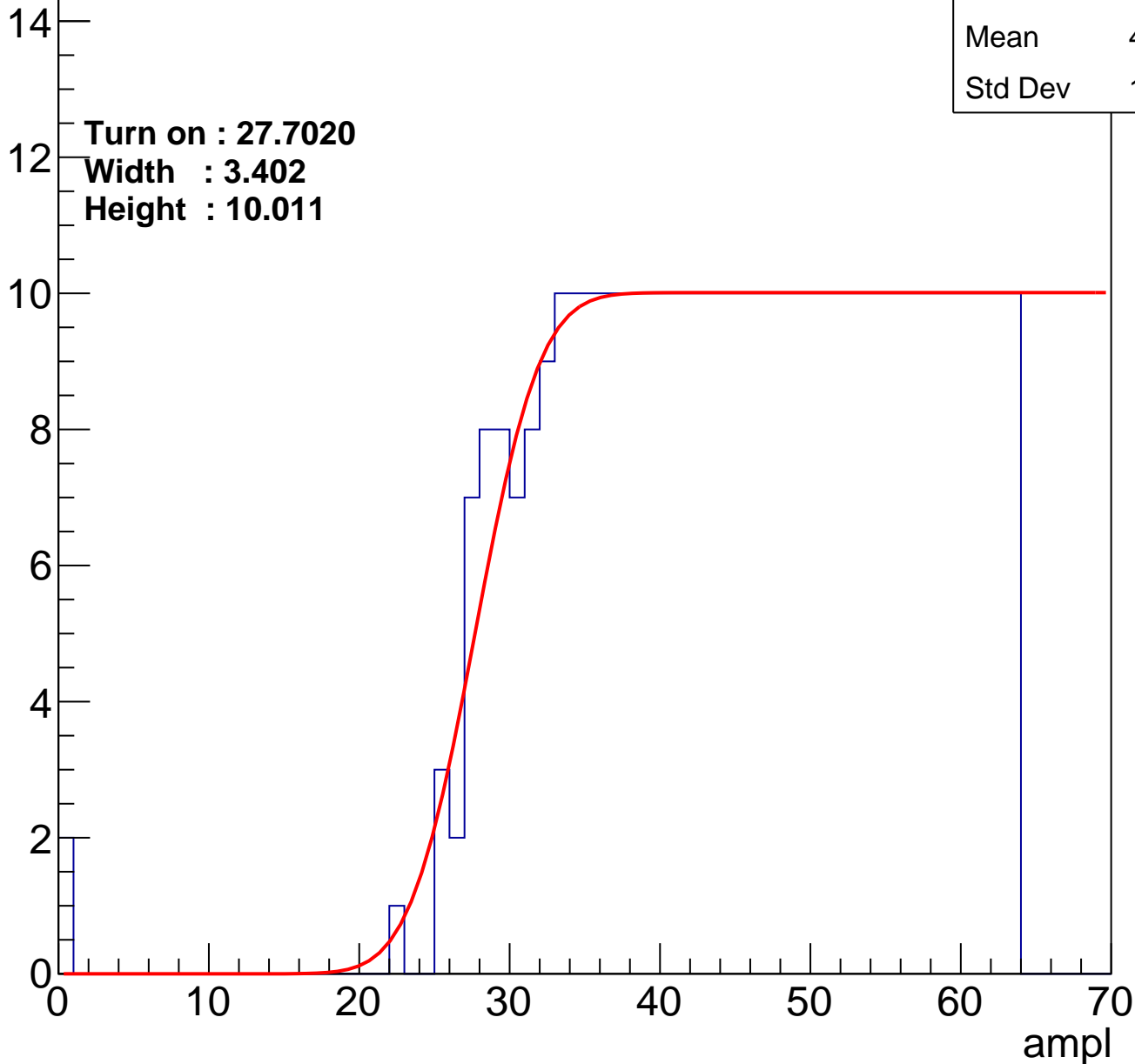
Entry

Entries	365
Mean	44.99
Std Dev	11.15

Turn on : 27.7020

Width : 3.402

Height : 10.011



# B1L003S, U7-ch44

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	357
Mean	45.31
Std Dev	11.16

Turn on : 28.9258

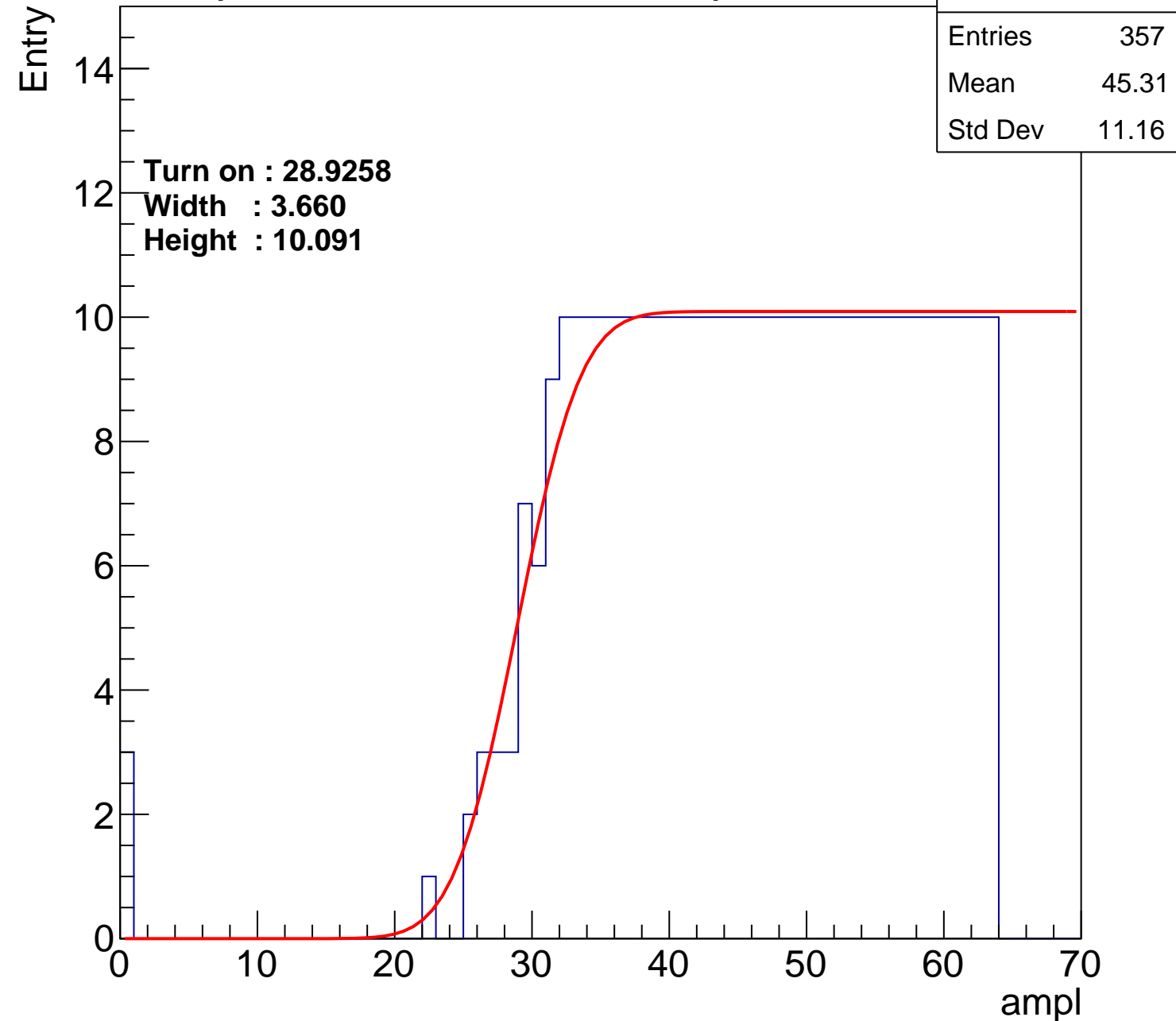
Width : 3.660

Height : 10.091

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch45

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	364
Mean	45.15
Std Dev	10.85

Turn on : 27.5328

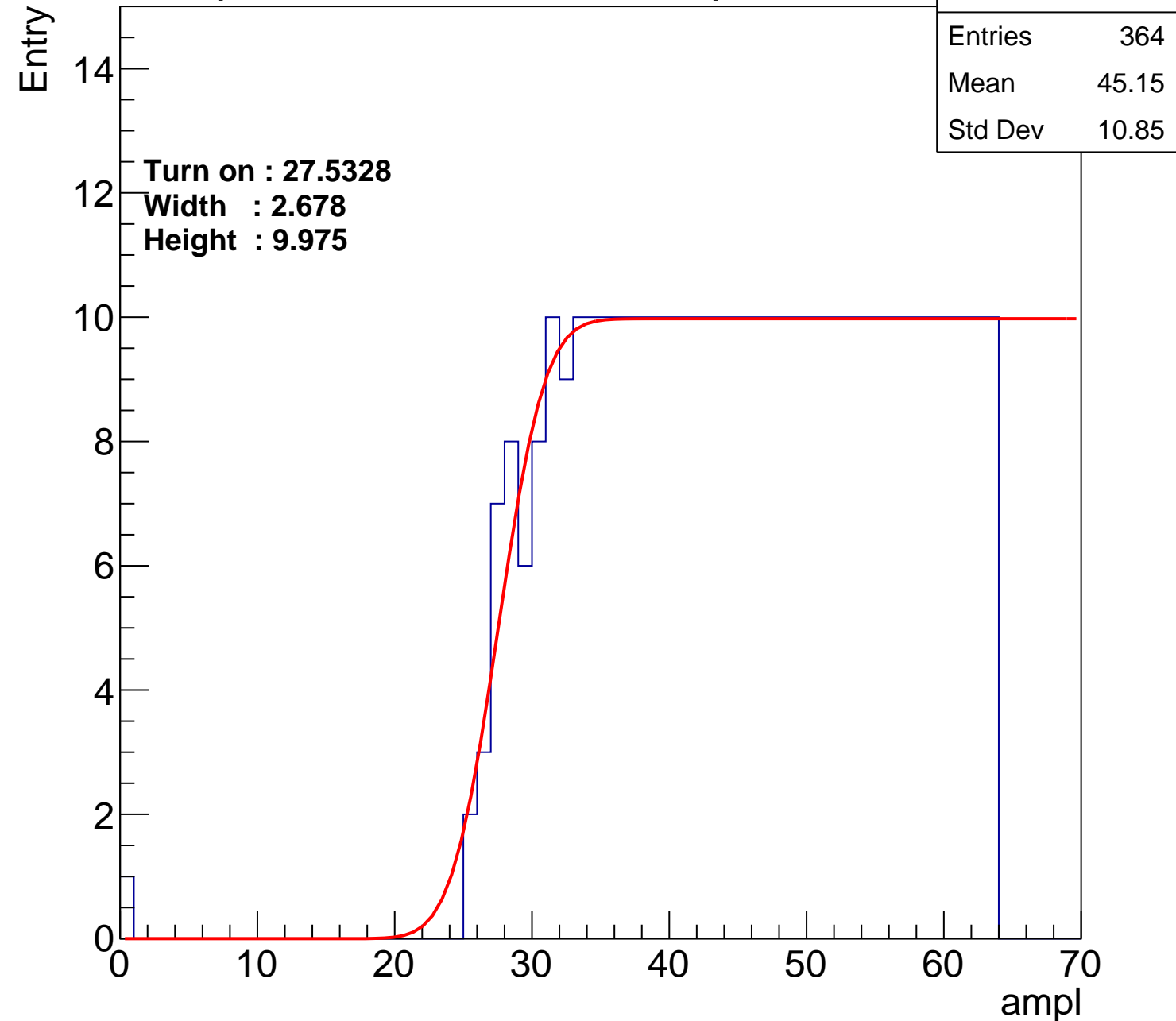
Width : 2.678

Height : 9.975

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch46

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	377
Mean	44.46
Std Dev	11.36

Turn on : 26.1415

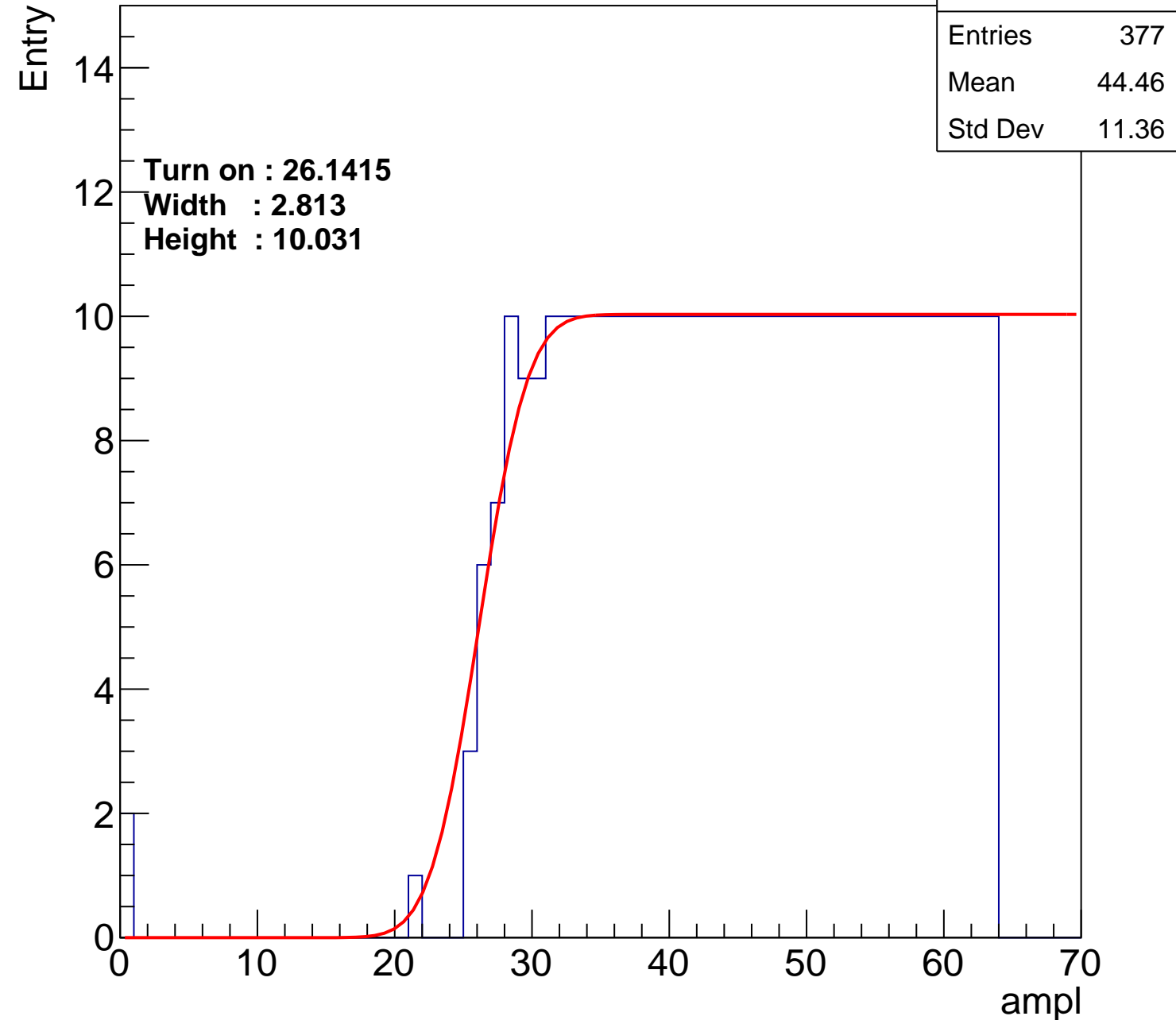
Width : 2.813

Height : 10.031

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L003S, U7-ch47

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	392
Mean	43.69
Std Dev	11.79

Turn on : 25.1554

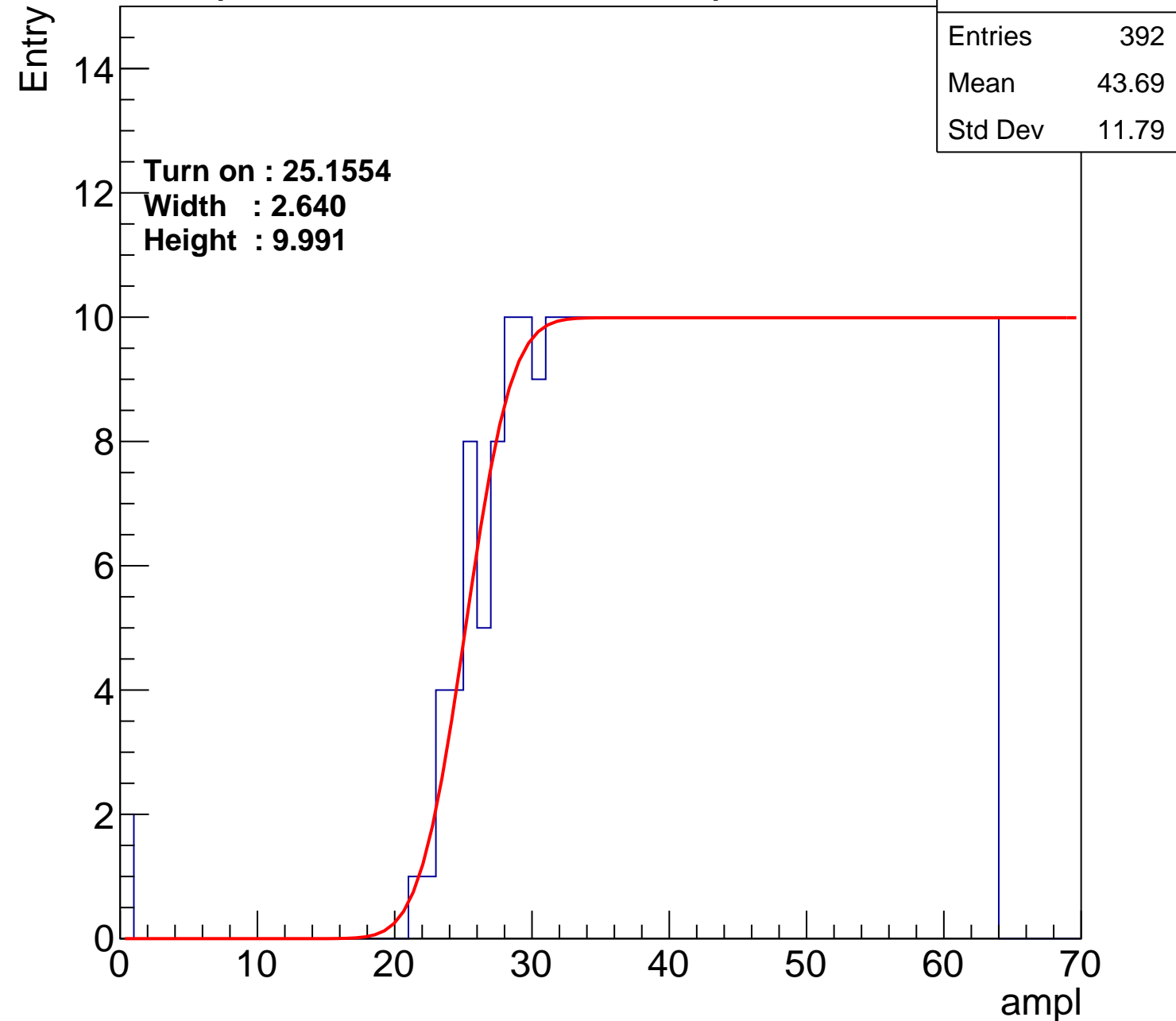
Width : 2.640

Height : 9.991

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch48

calib\_packv5\_042523\_0143.root, FC#13, port D2

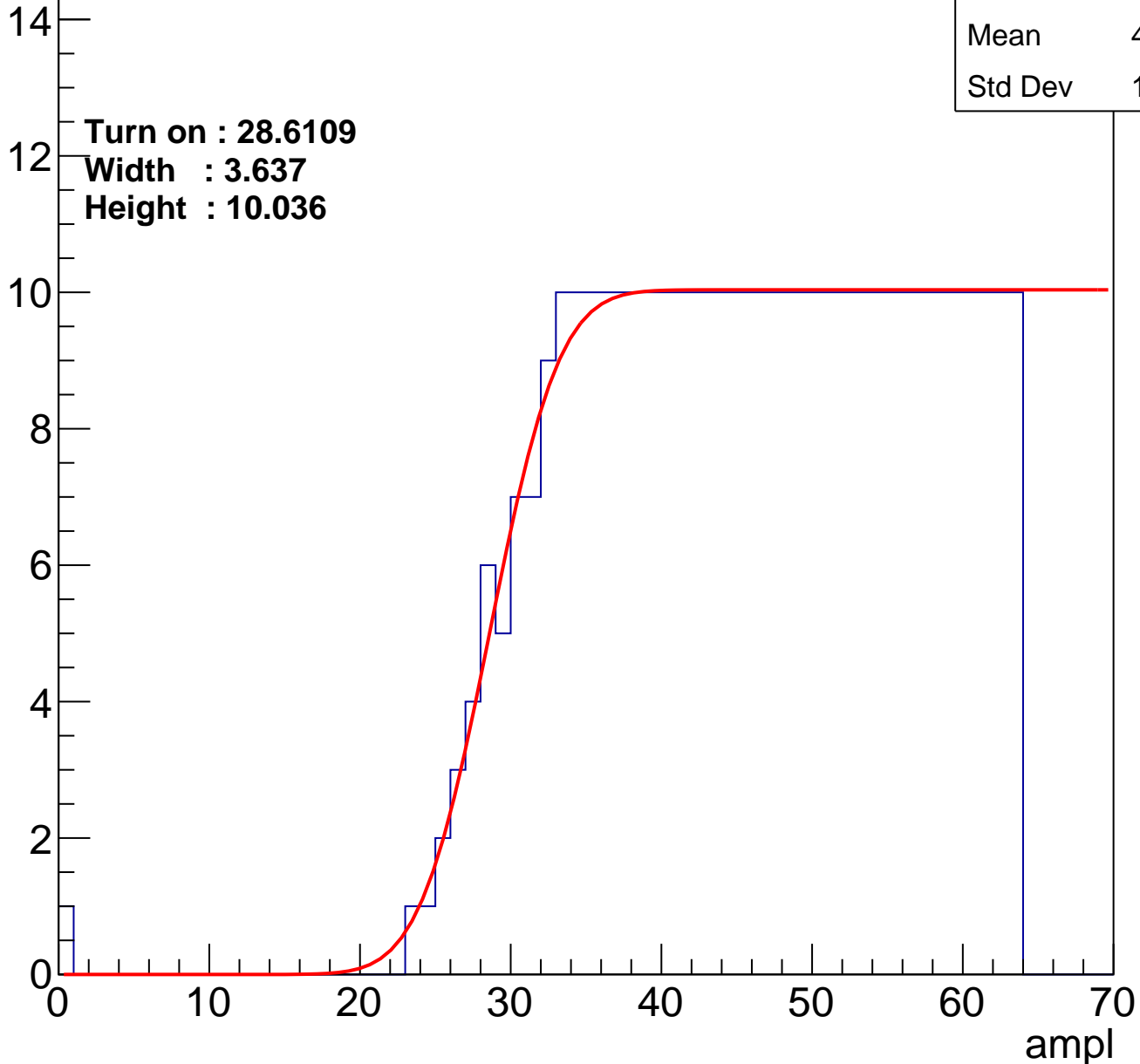
Entries	356
Mean	45.48
Std Dev	10.75

Turn on : 28.6109

Width : 3.637

Height : 10.036

Entry



# B1L003S, U7-ch49

calib\_packv5\_042523\_0143.root, FC#13, port D2

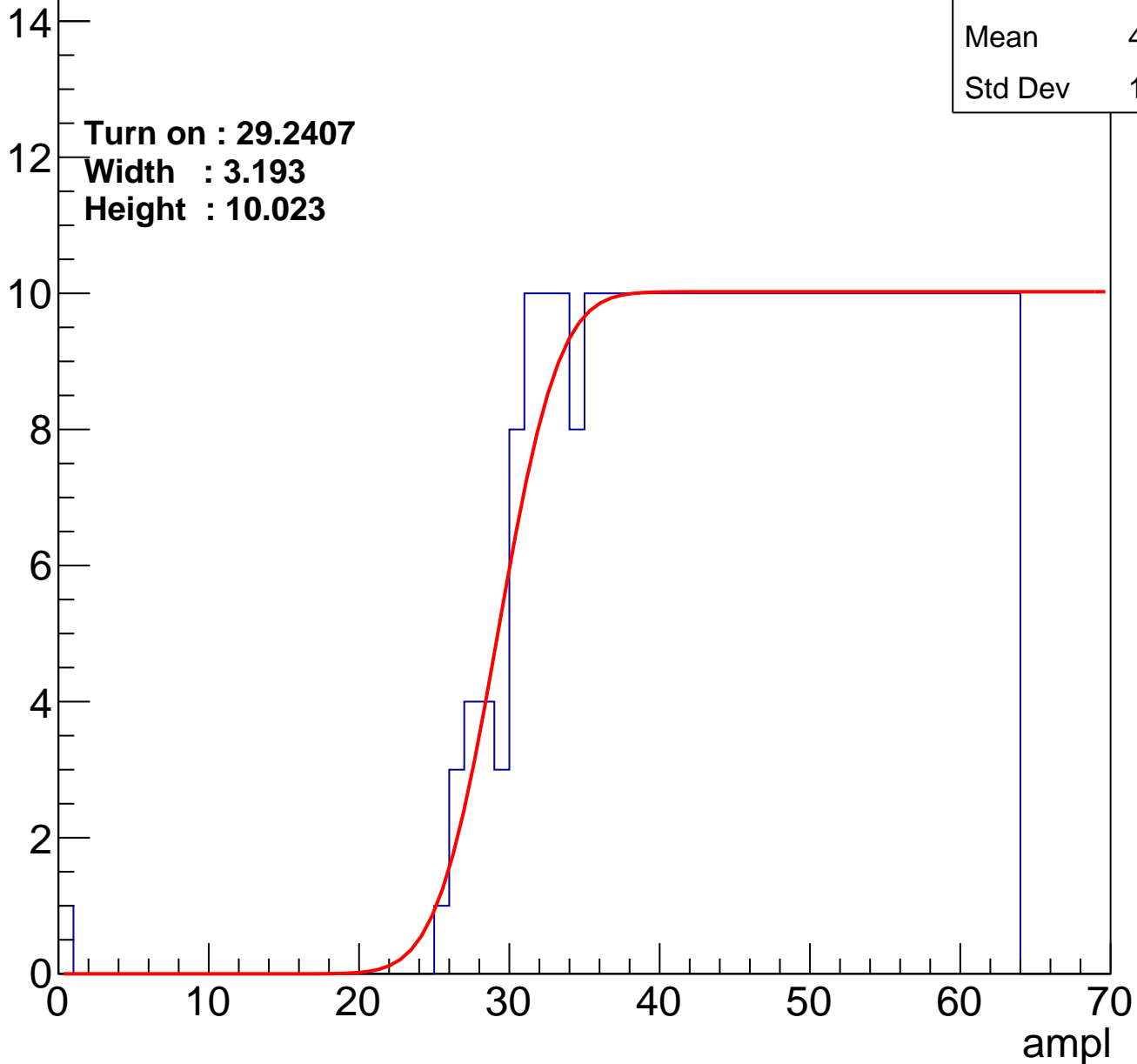
Entry

Entries	352
Mean	45.72
Std Dev	10.57

Turn on : 29.2407

Width : 3.193

Height : 10.023



# B1L003S, U7-ch50

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	369
Mean	44.81
Std Dev	11.22

Turn on : 27.8395

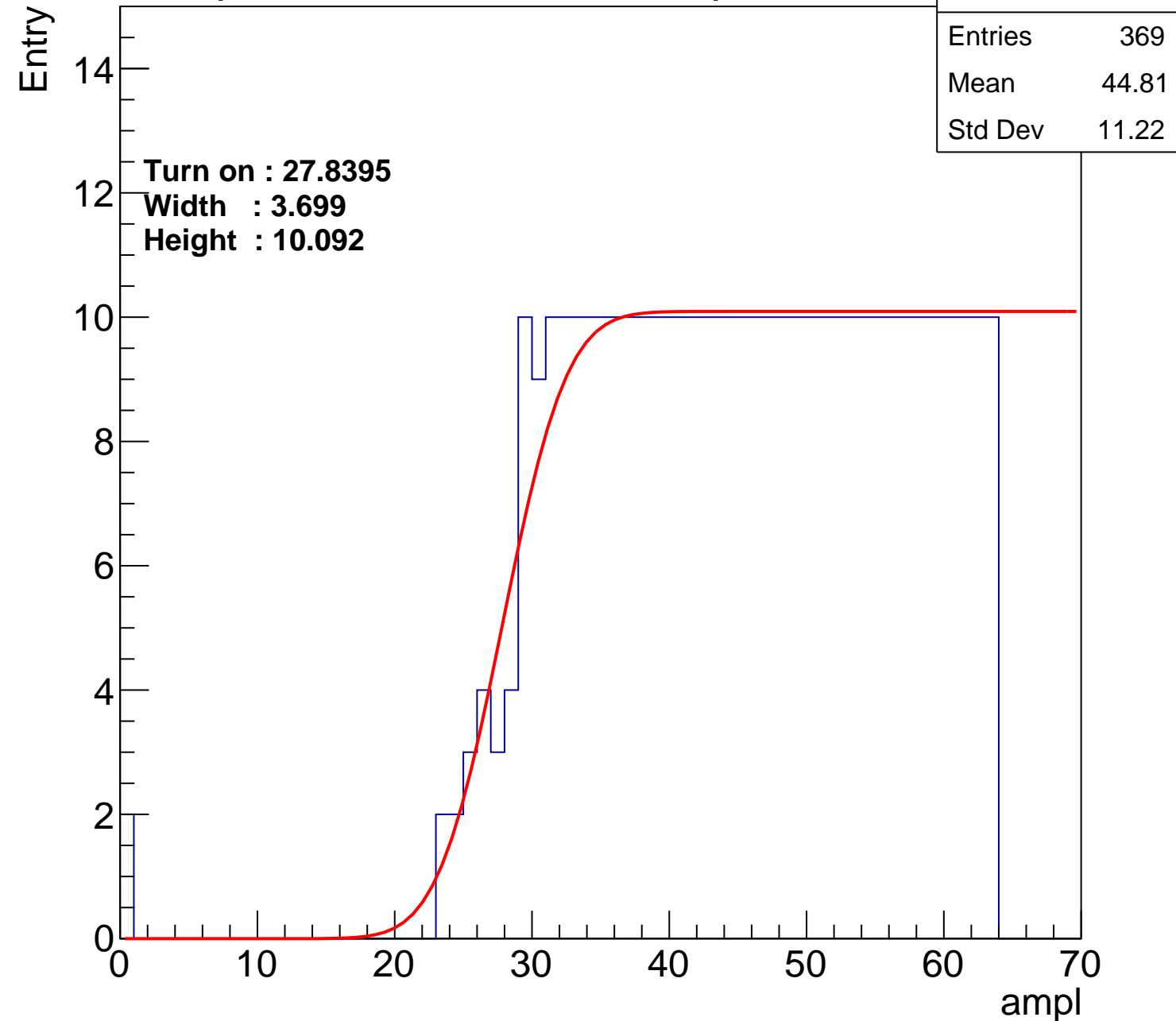
Width : 3.699

Height : 10.092

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch51

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	370
Mean	44.74
Std Dev	11.28

Turn on : 27.1071

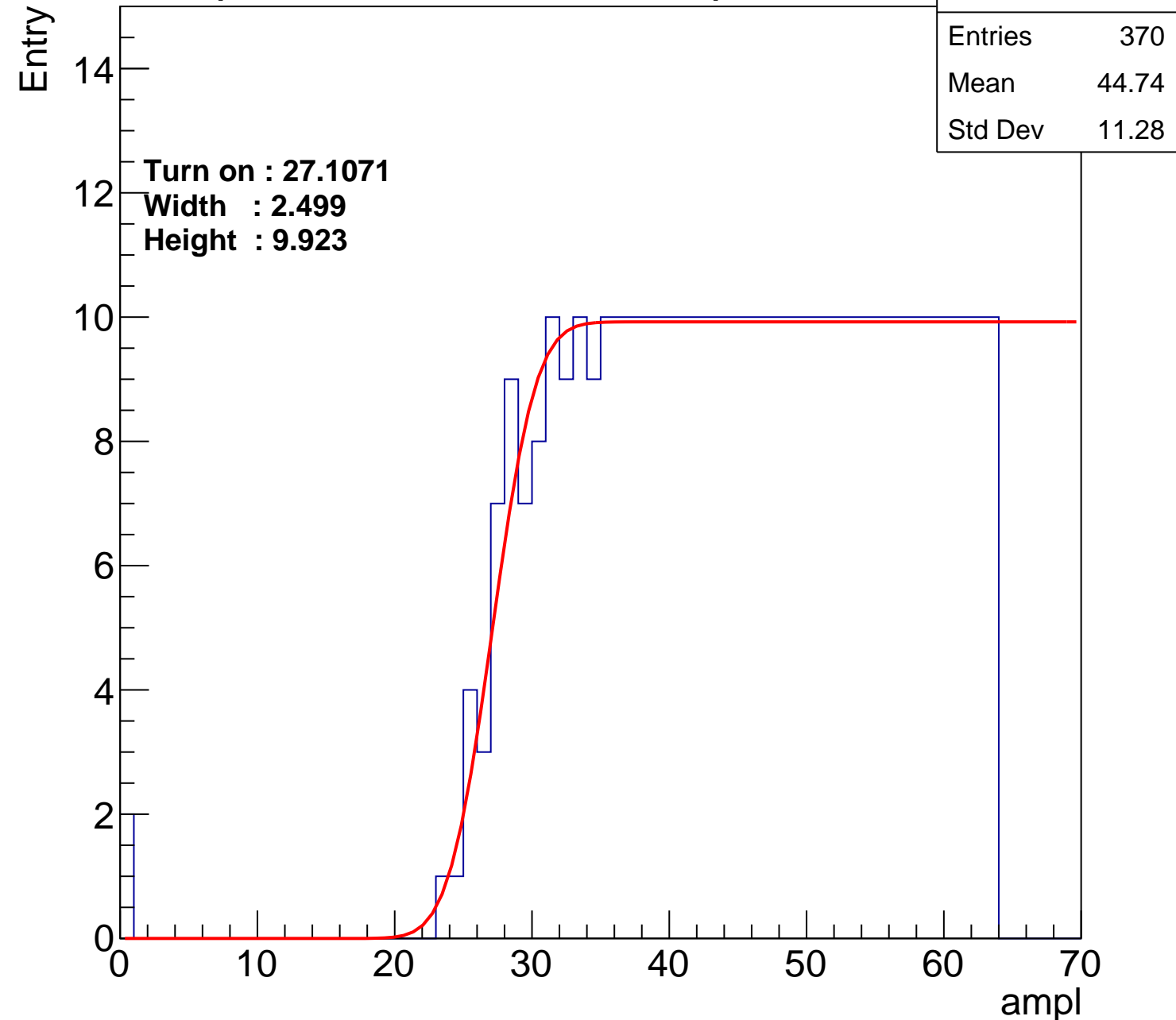
Width : 2.499

Height : 9.923

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch52

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	359
Mean	45.29
Std Dev	10.99

Turn on : 28.0752

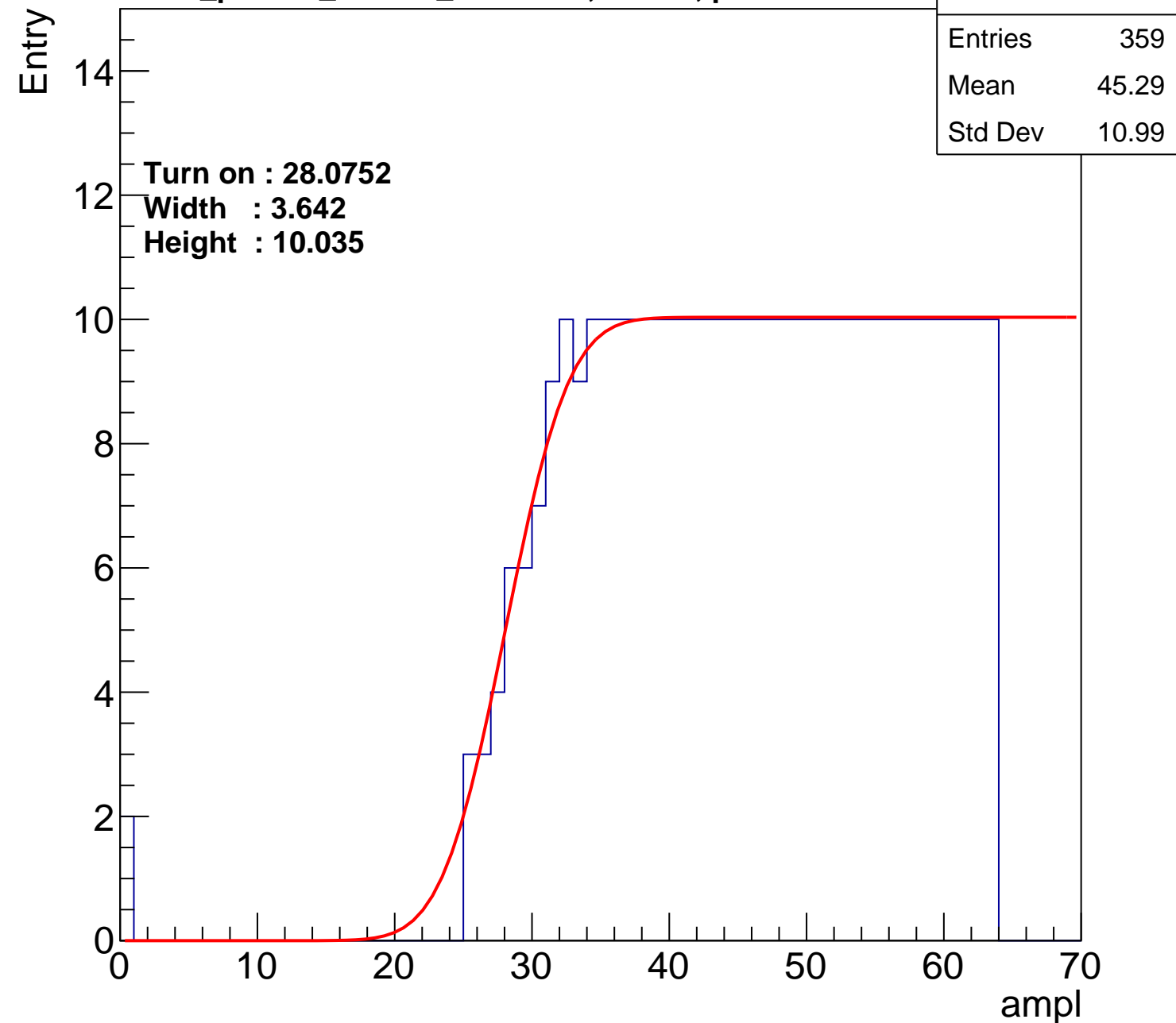
Width : 3.642

Height : 10.035

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch53

calib\_packv5\_042523\_0143.root, FC#13, port D2

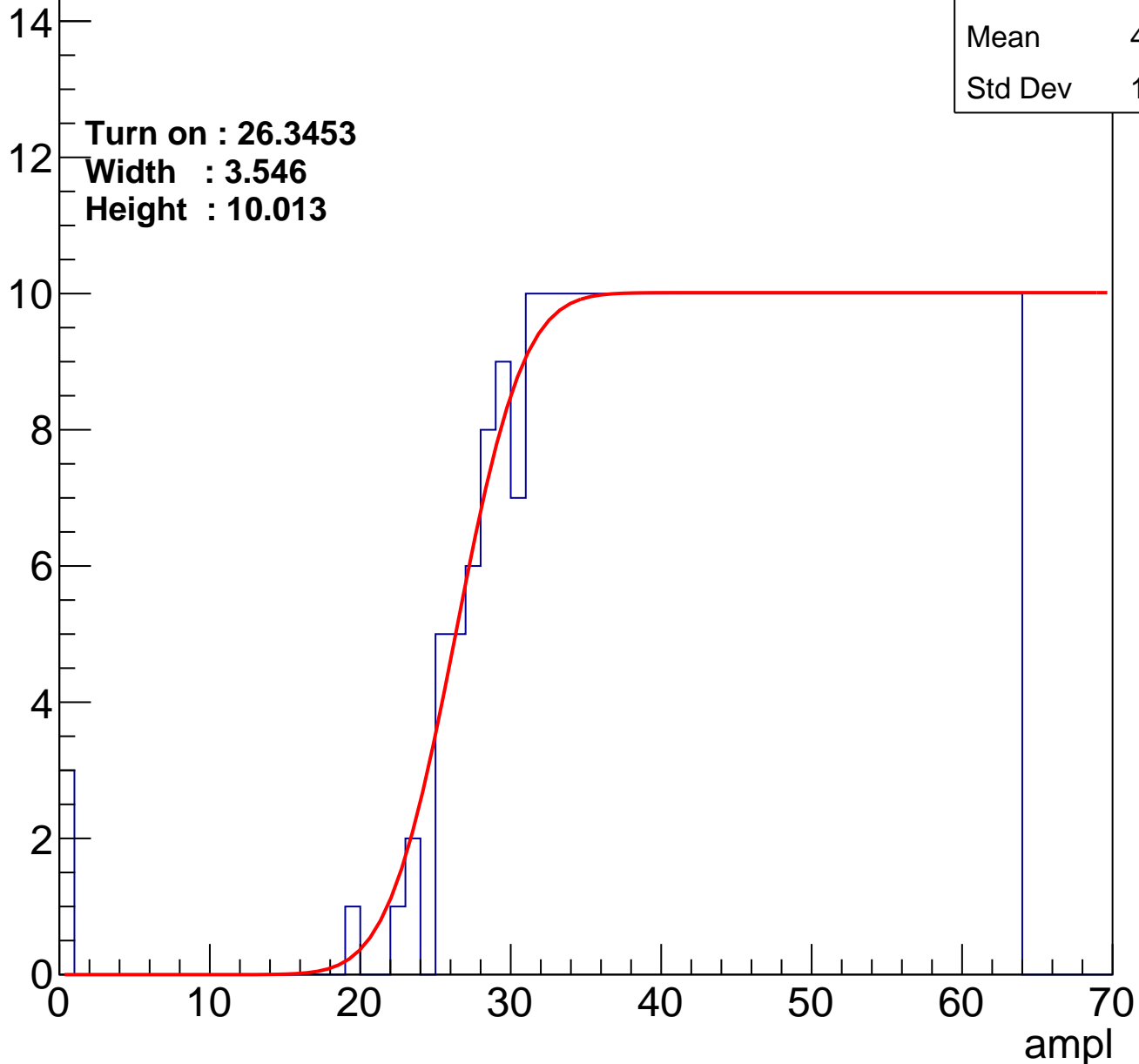
Entries	377
Mean	44.32
Std Dev	11.66

Turn on : 26.3453

Width : 3.546

Height : 10.013

Entry



# B1L003S, U7-ch54

calib\_packv5\_042523\_0143.root, FC#13, port D2

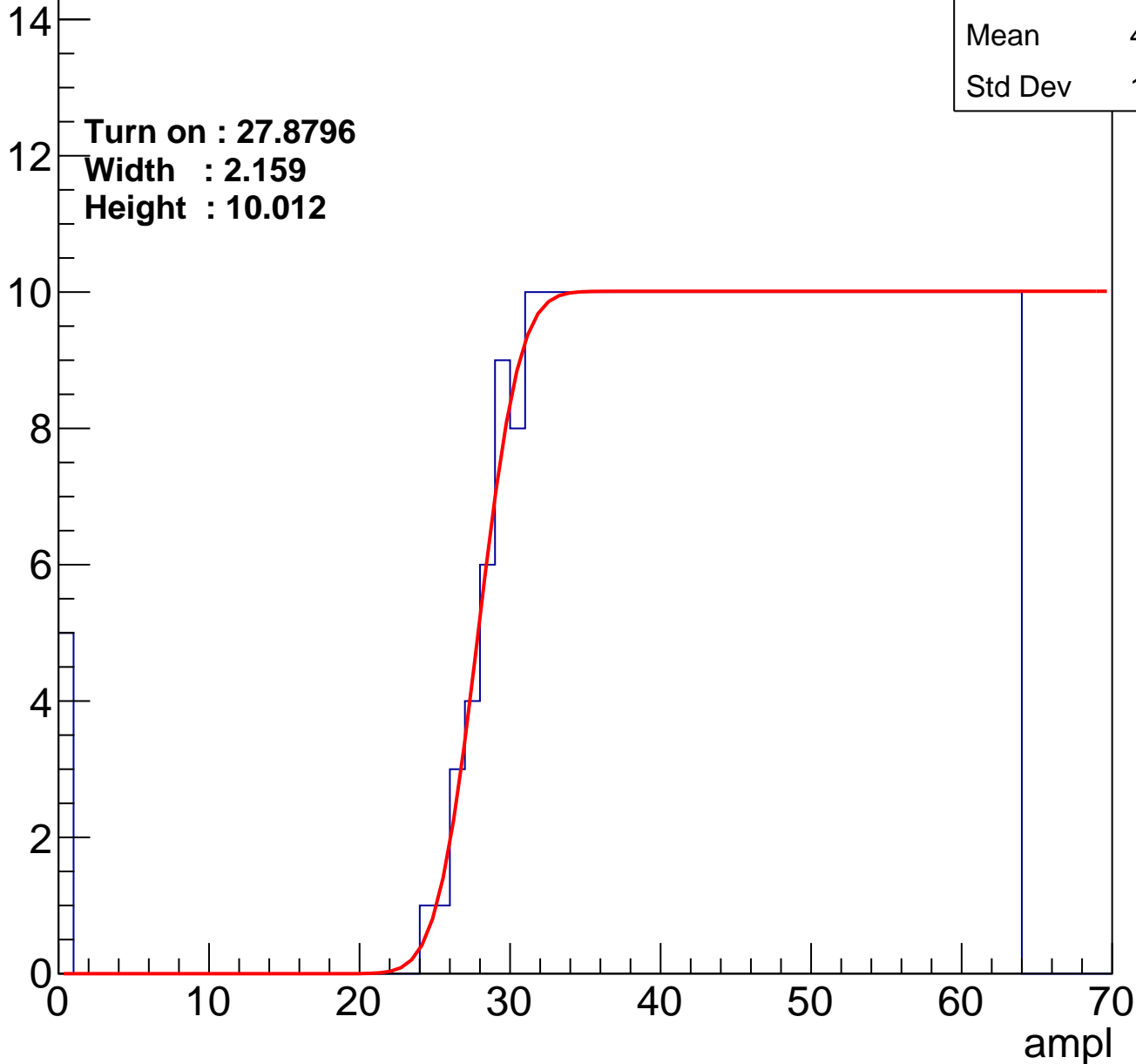
Entry

Entries	367
Mean	44.72
Std Dev	11.72

Turn on : 27.8796

Width : 2.159

Height : 10.012





# B1L003S, U7-ch55

calib\_packv5\_042523\_0143.root, FC#13, port D2

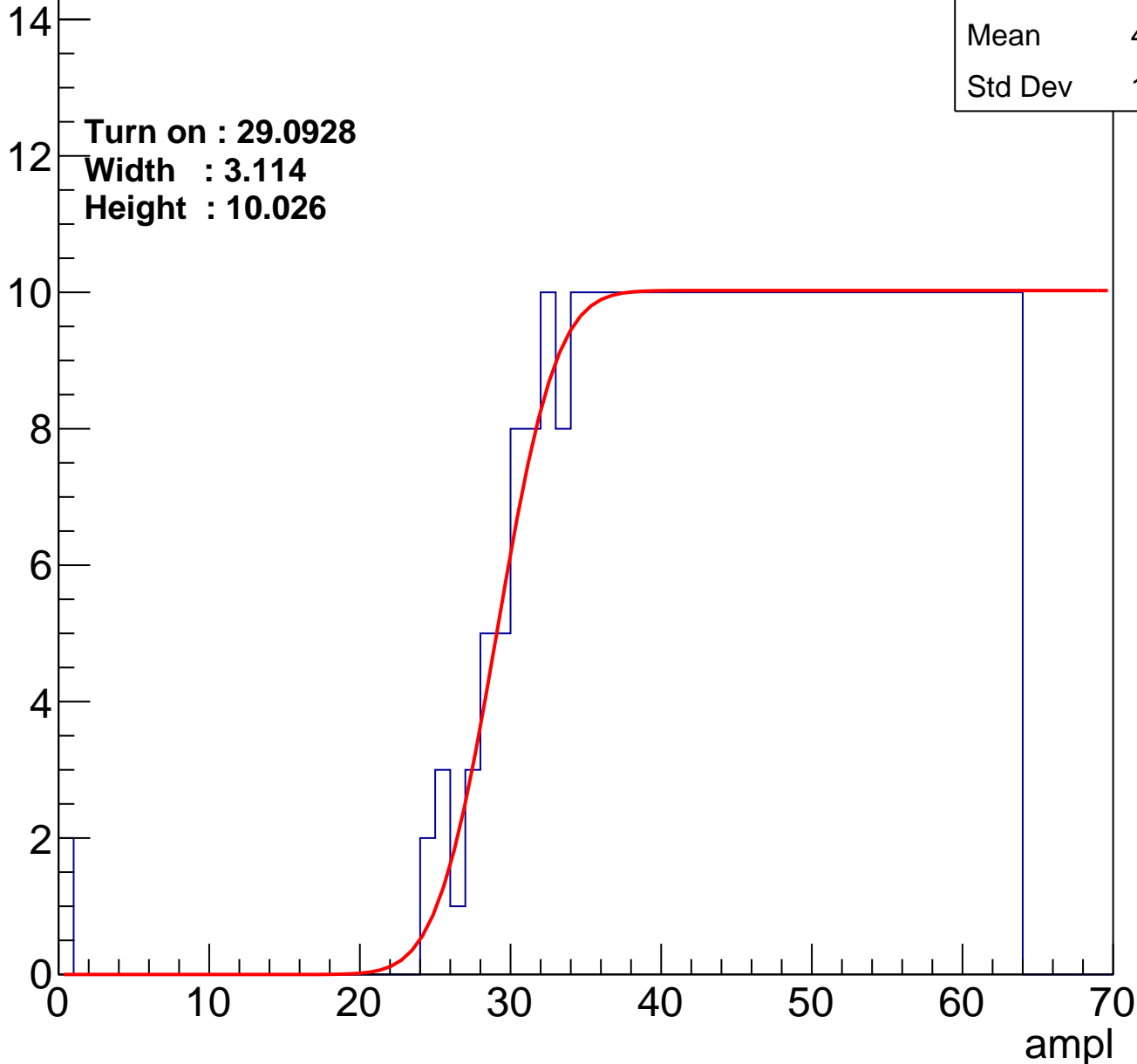
Entries	355
Mean	45.46
Std Dev	10.94

Turn on : 29.0928

Width : 3.114

Height : 10.026

Entry



# B1L003S, U7-ch56

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	367
Mean	44.9
Std Dev	11.18

**Turn on : 27.6932**

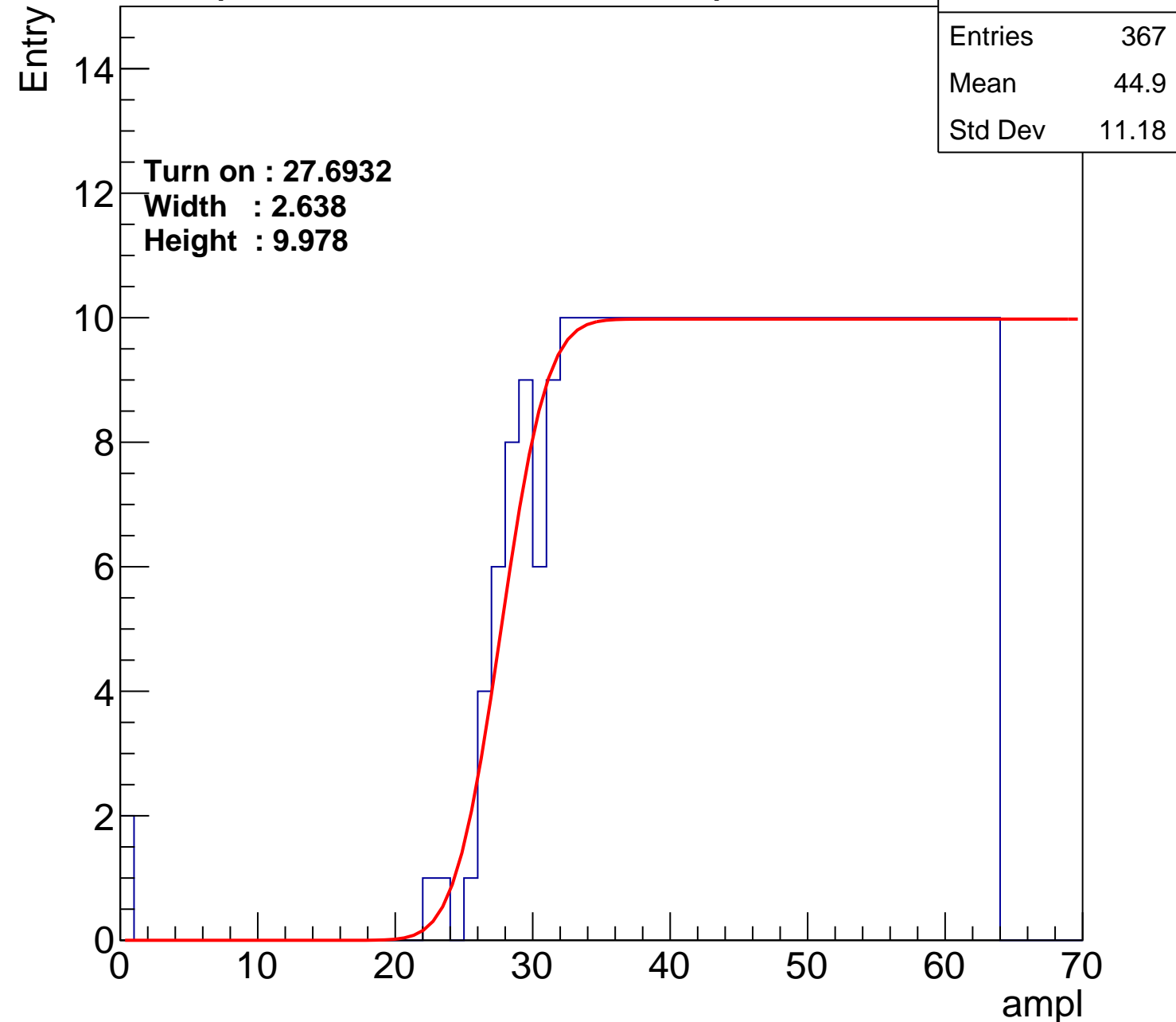
**Width : 2.638**

**Height : 9.978**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch57

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	359
Mean	45.33
Std Dev	10.93

Turn on : 28.3214

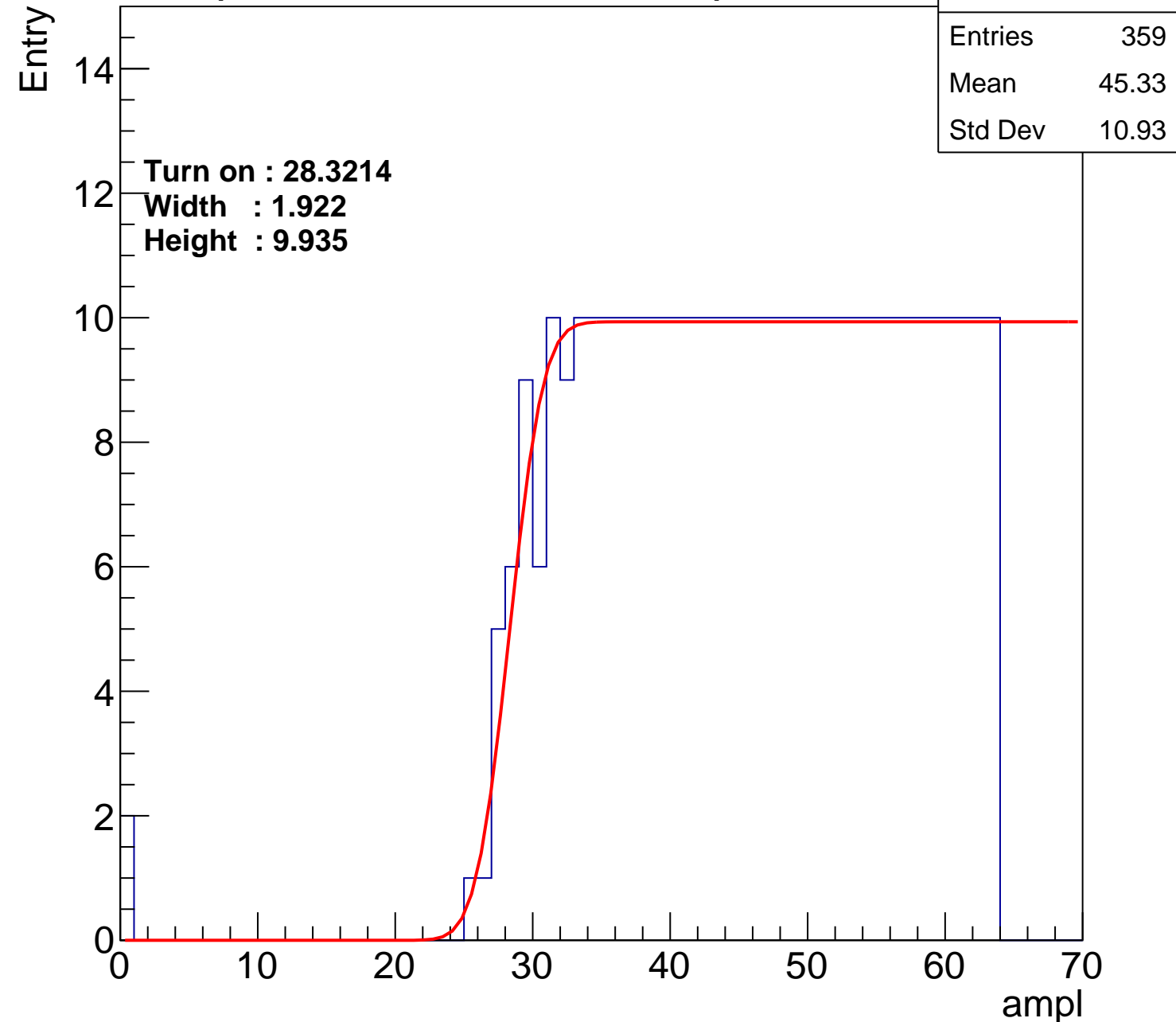
Width : 1.922

Height : 9.935

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch58

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	379
Mean	44.18
Std Dev	11.77

Turn on : 26.4441

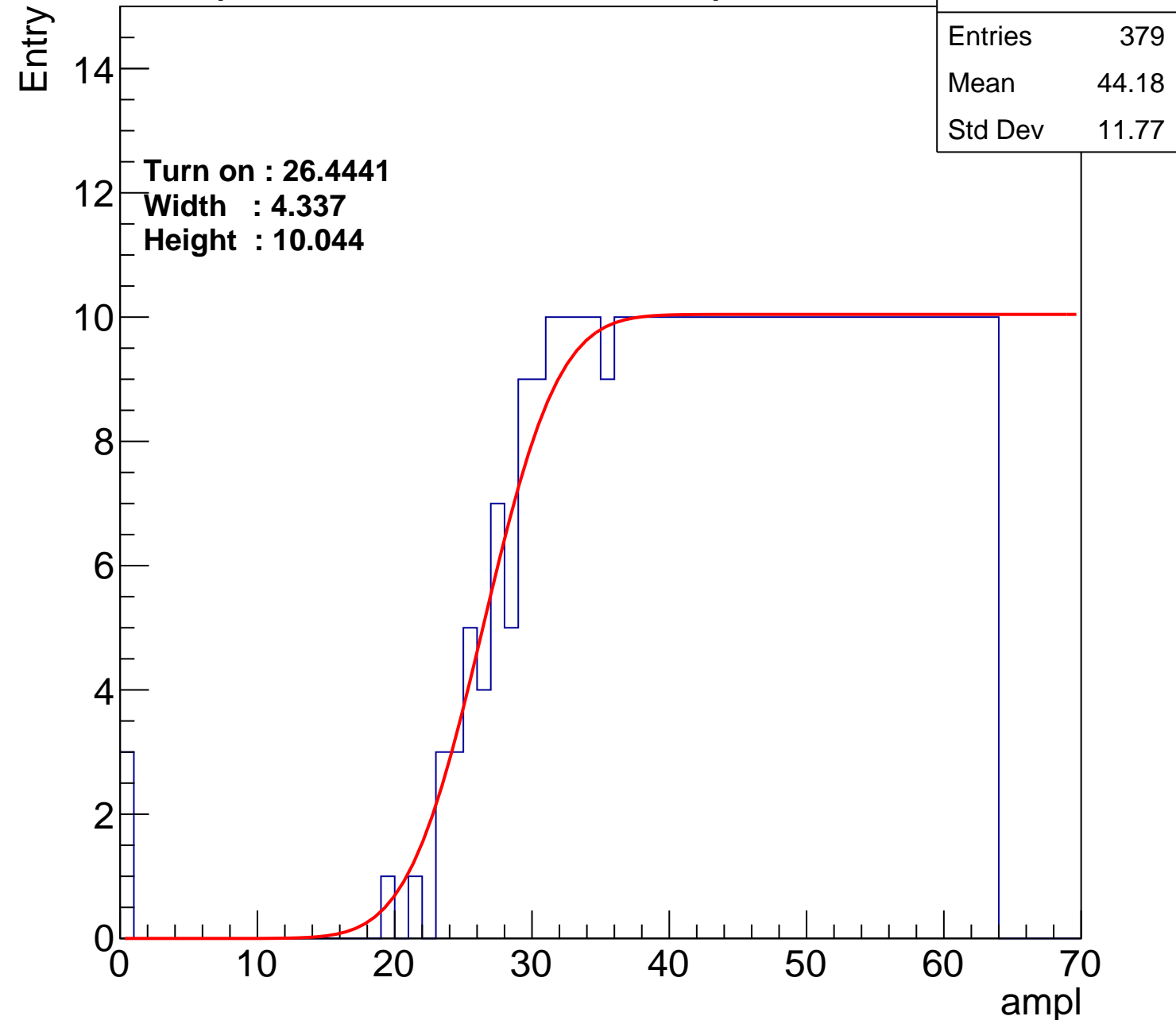
Width : 4.337

Height : 10.044

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch59

**calib\_packv5\_042523\_0143.root, FC#13, port D2**

Entries	381
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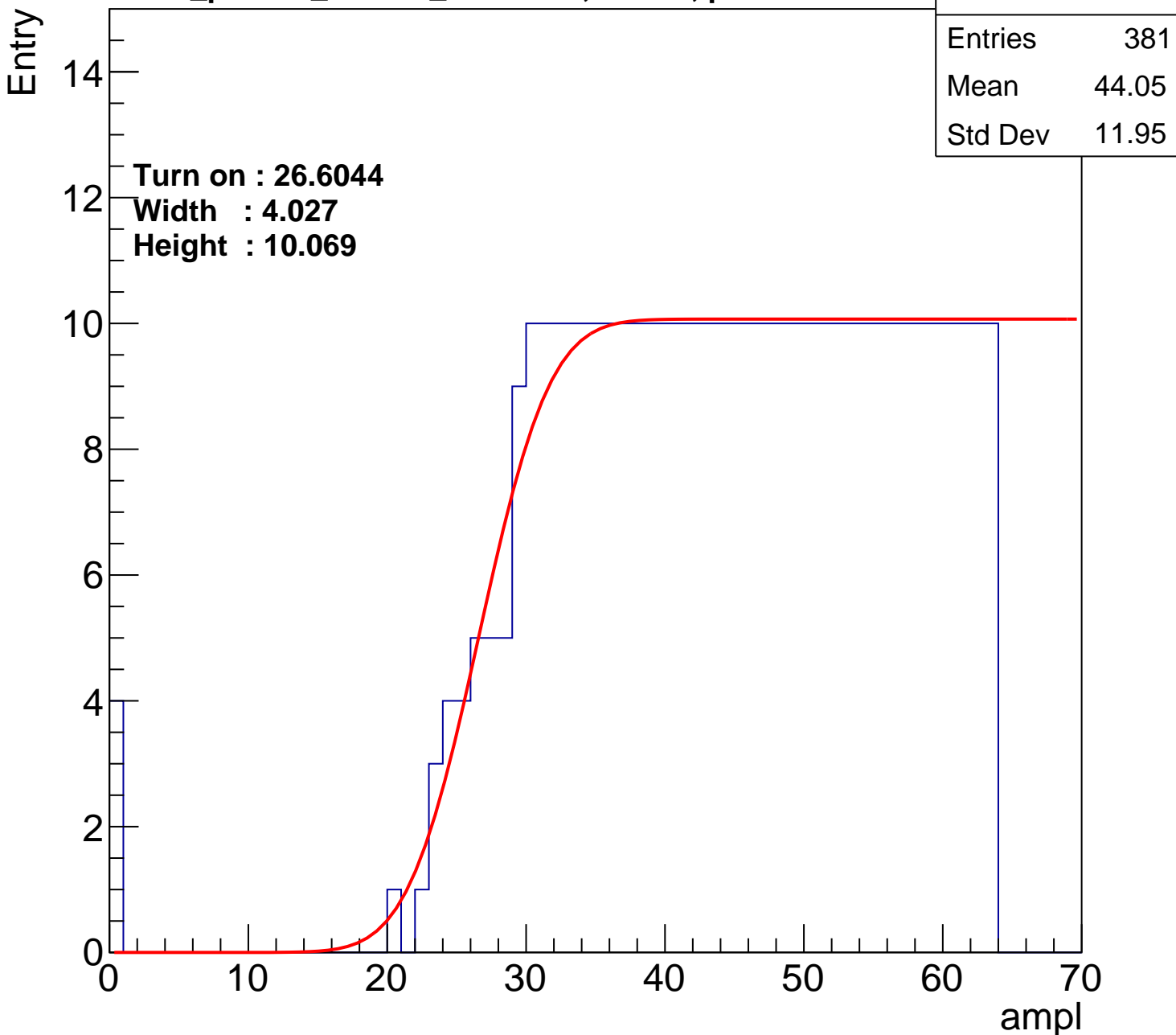
Mean	44.05
------	-------

Std Dev	11.95
---------	-------

Turn on : 26.6044

**Width : 4.027**

**Height : 10.069**



# B1L003S, U7-ch60

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	400
Mean	43.29
Std Dev	12.01

**Turn on : 23.7355**

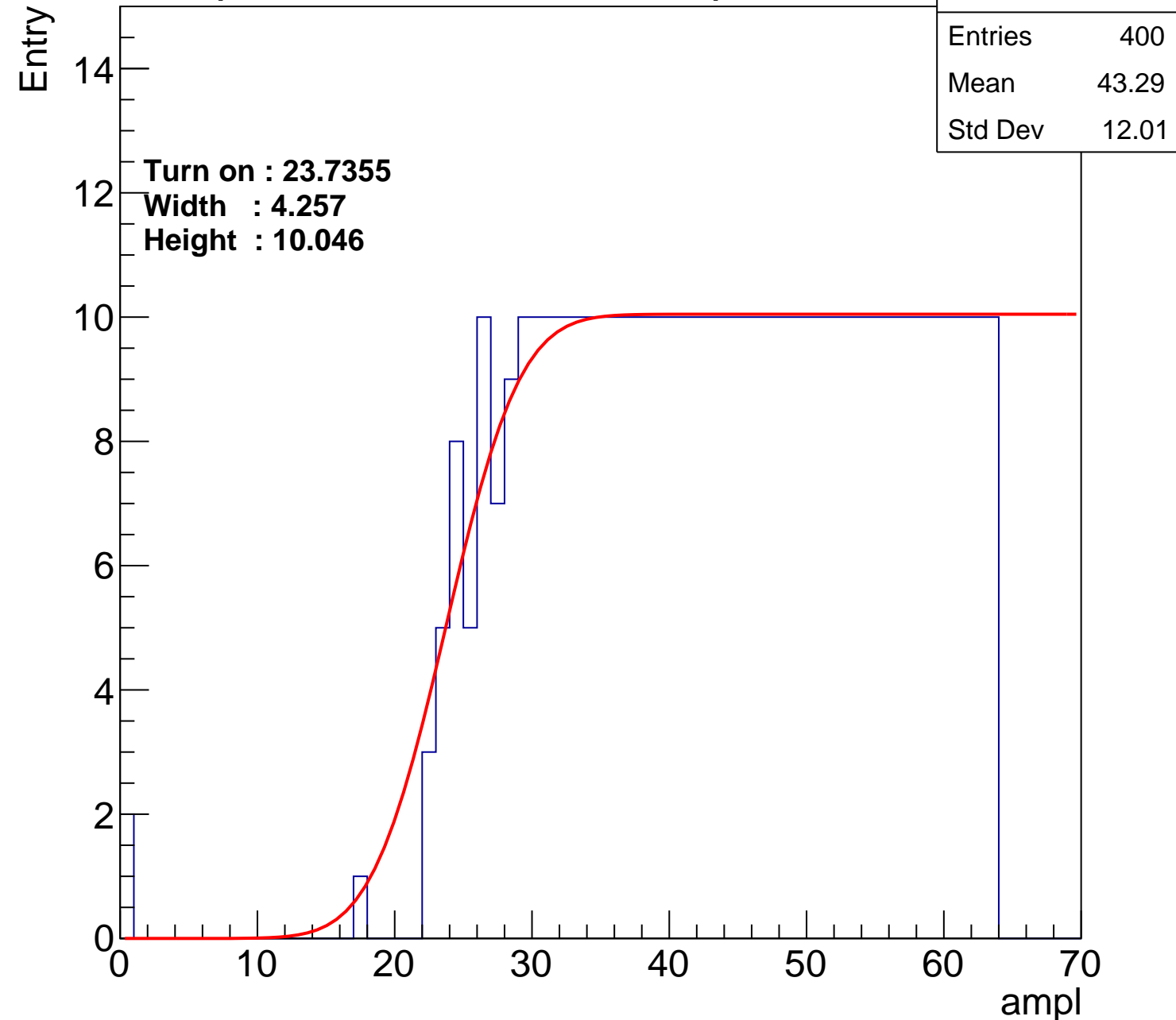
**Width : 4.257**

**Height : 10.046**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch61

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	373
Mean	44.23
Std Dev	12.39

Turn on : 27.6572

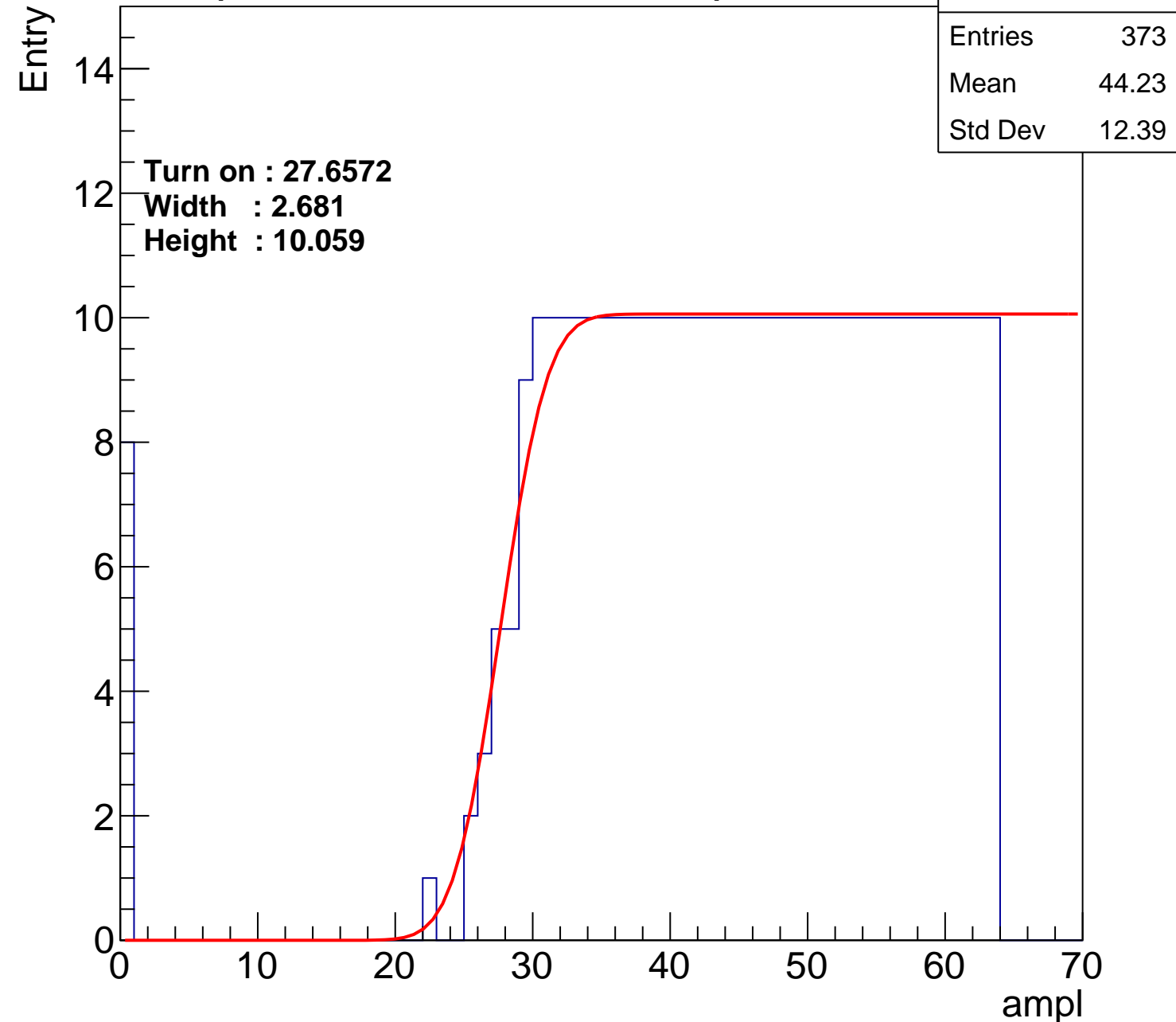
Width : 2.681

Height : 10.059

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch62

calib\_packv5\_042523\_0143.root, FC#13, port D2

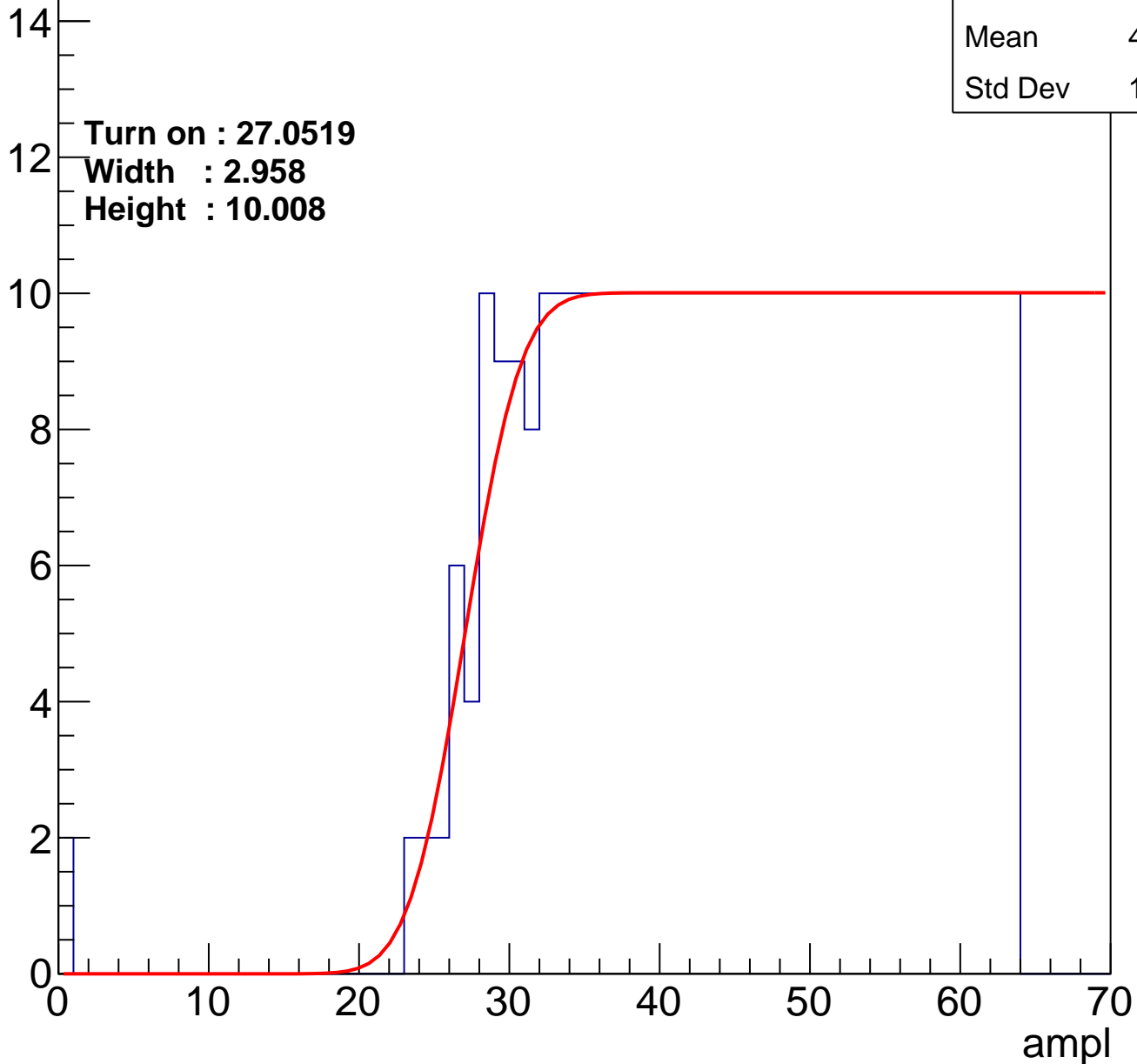
Entry

Entries	374
Mean	44.56
Std Dev	11.35

Turn on : 27.0519

Width : 2.958

Height : 10.008





# B1L003S, U7-ch63

calib\_packv5\_042523\_0143.root, FC#13, port D2

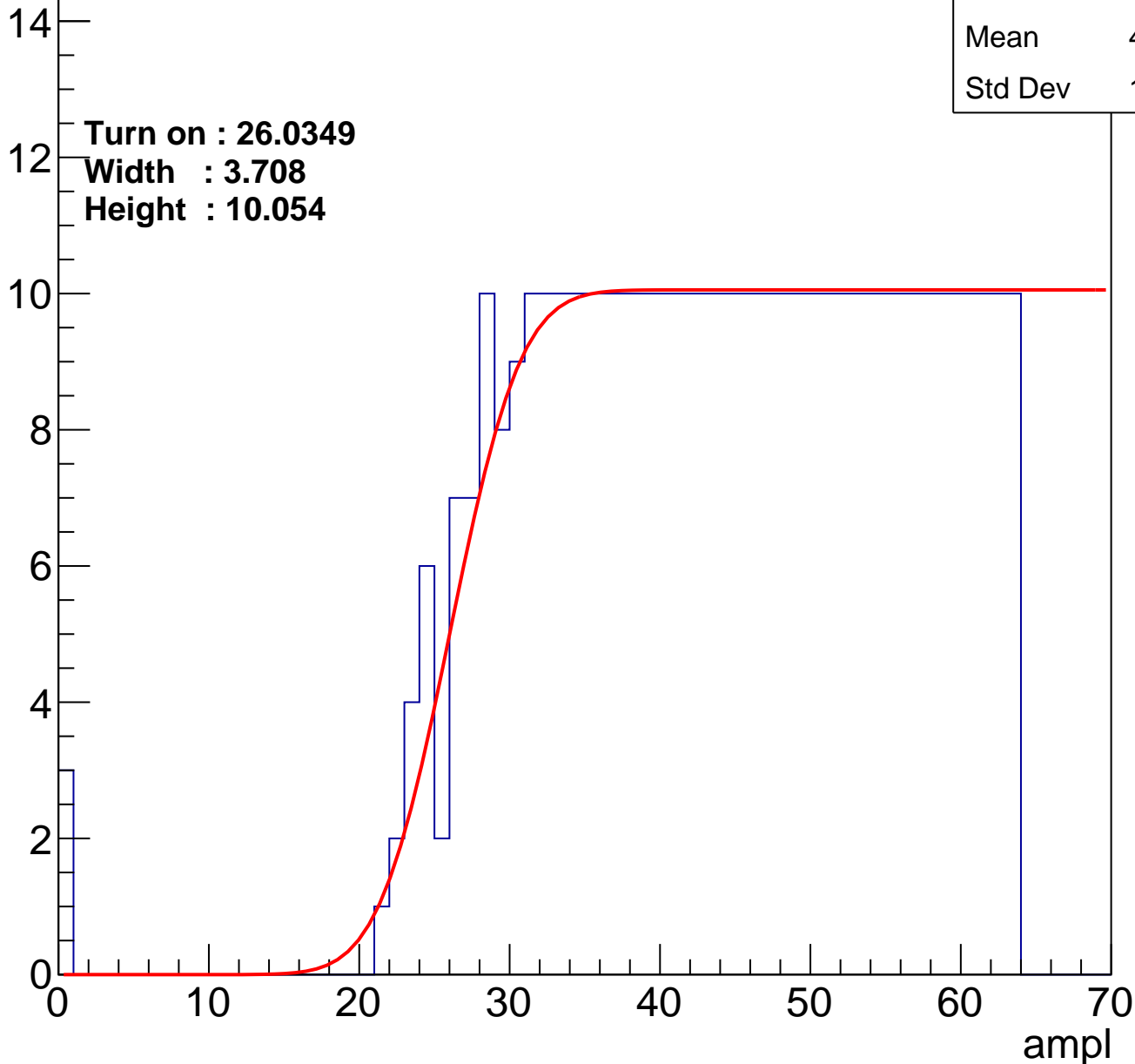
Entry

Entries	389
Mean	43.74
Std Dev	11.94

Turn on : 26.0349

Width : 3.708

Height : 10.054



# B1L003S, U7-ch64

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	342
Mean	46.05
Std Dev	10.82

**Turn on : 29.9675**

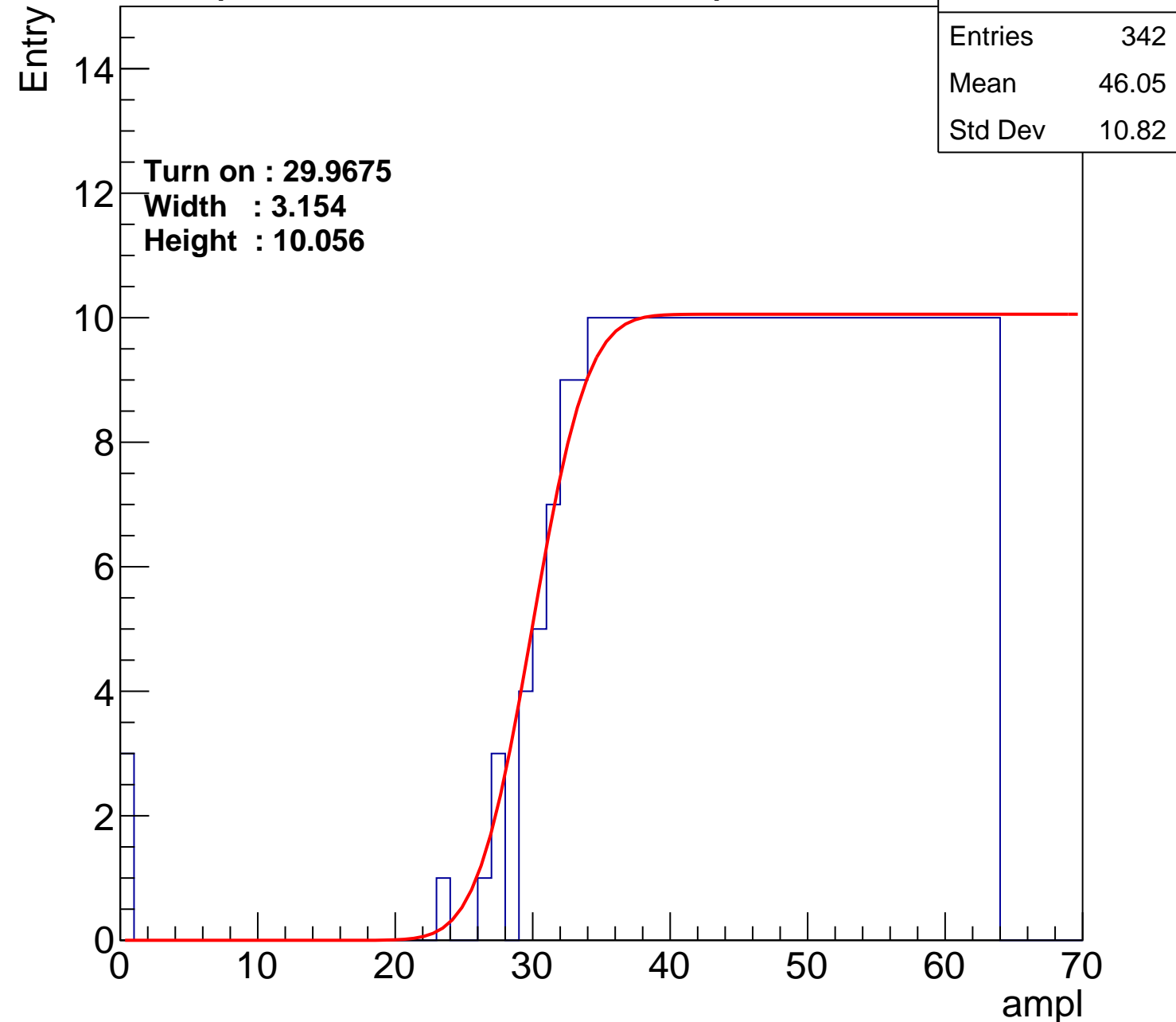
**Width : 3.154**

**Height : 10.056**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch65

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	363
Mean	44.94
Std Dev	11.52

Turn on : 28.6709

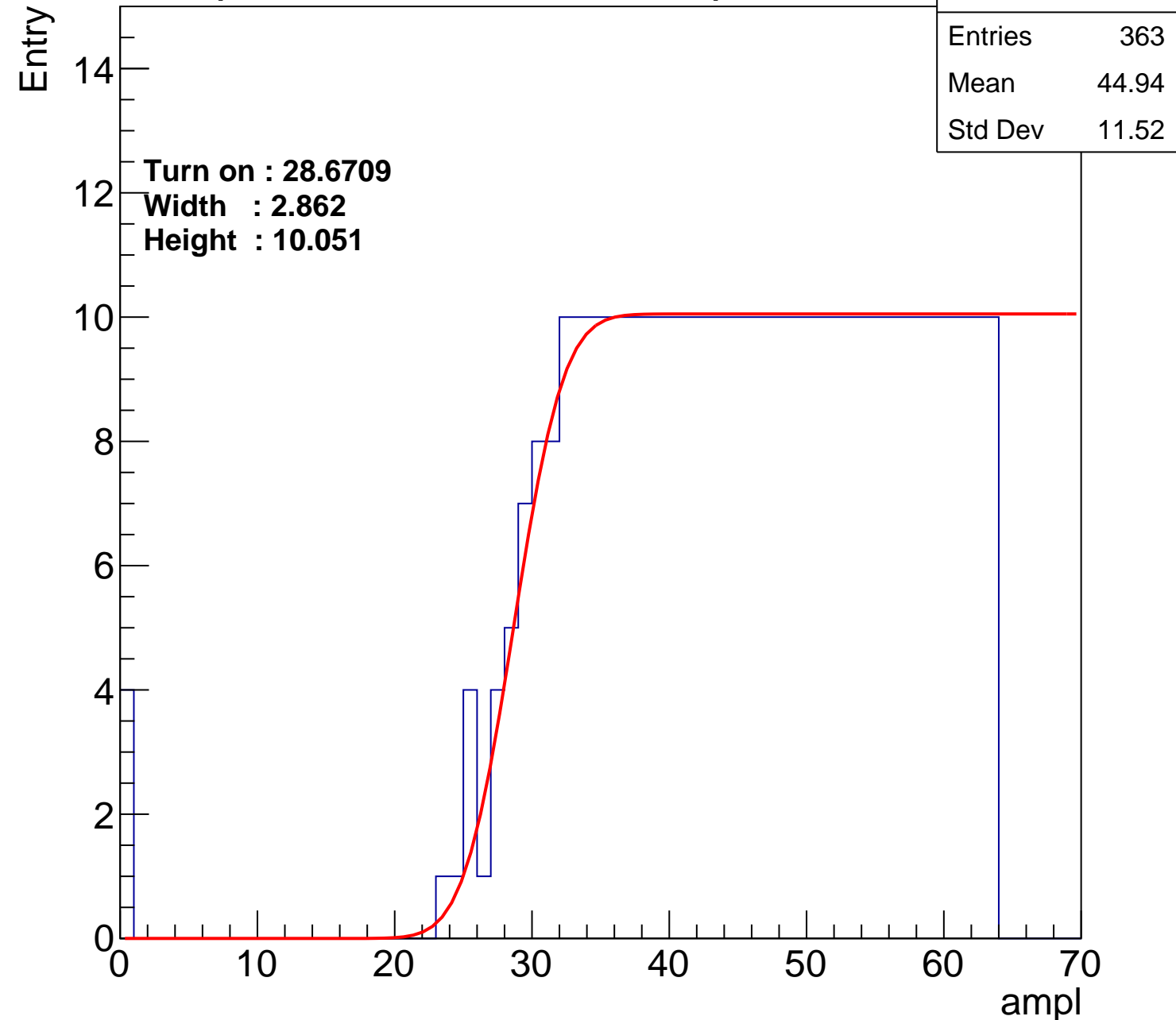
Width : 2.862

Height : 10.051

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch66

calib\_packv5\_042523\_0143.root, FC#13, port D2

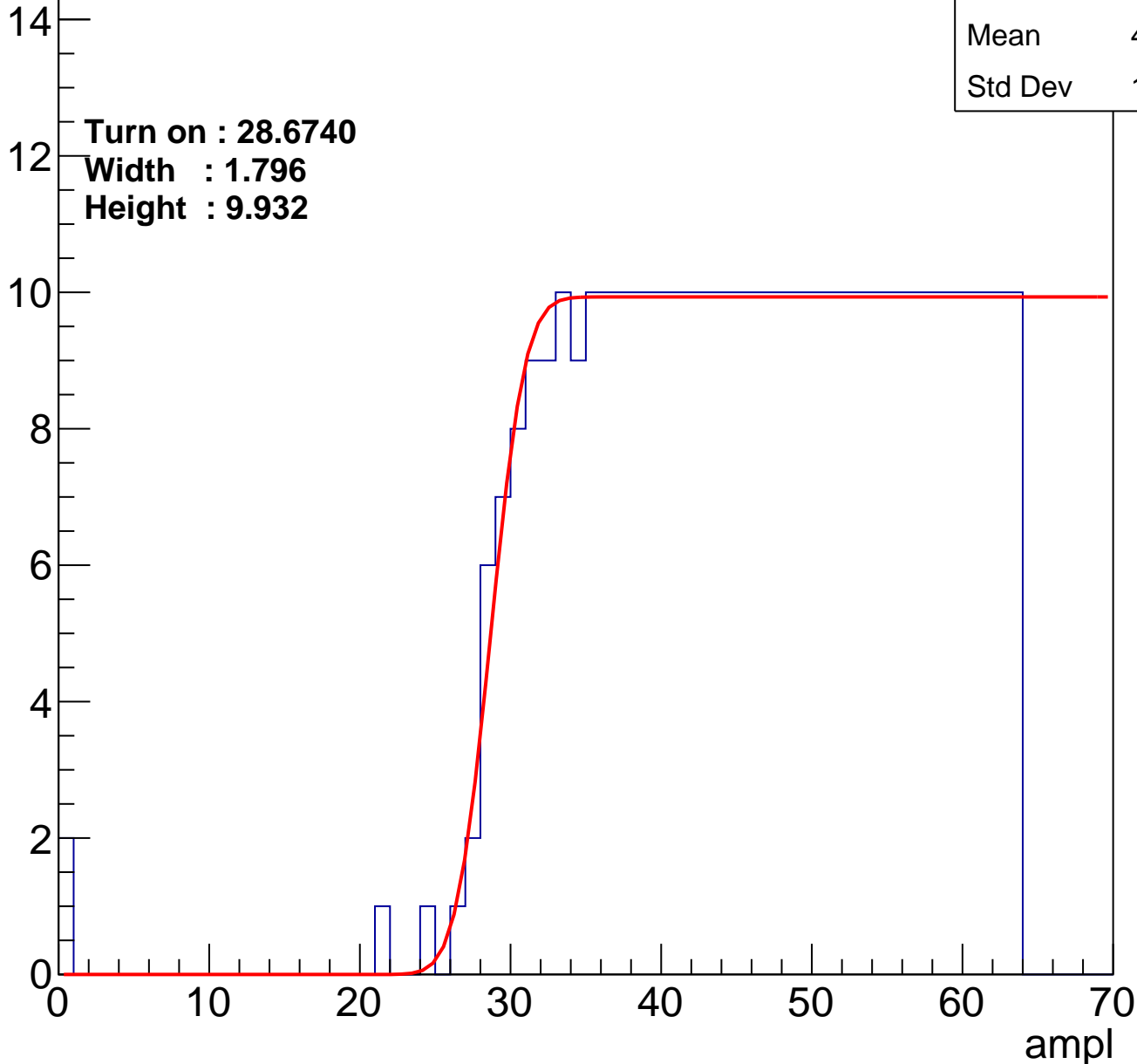
Entry

Entries	355
Mean	45.49
Std Dev	10.89

Turn on : 28.6740

Width : 1.796

Height : 9.932



# B1L003S, U7-ch67

calib\_packv5\_042523\_0143.root, FC#13, port D2

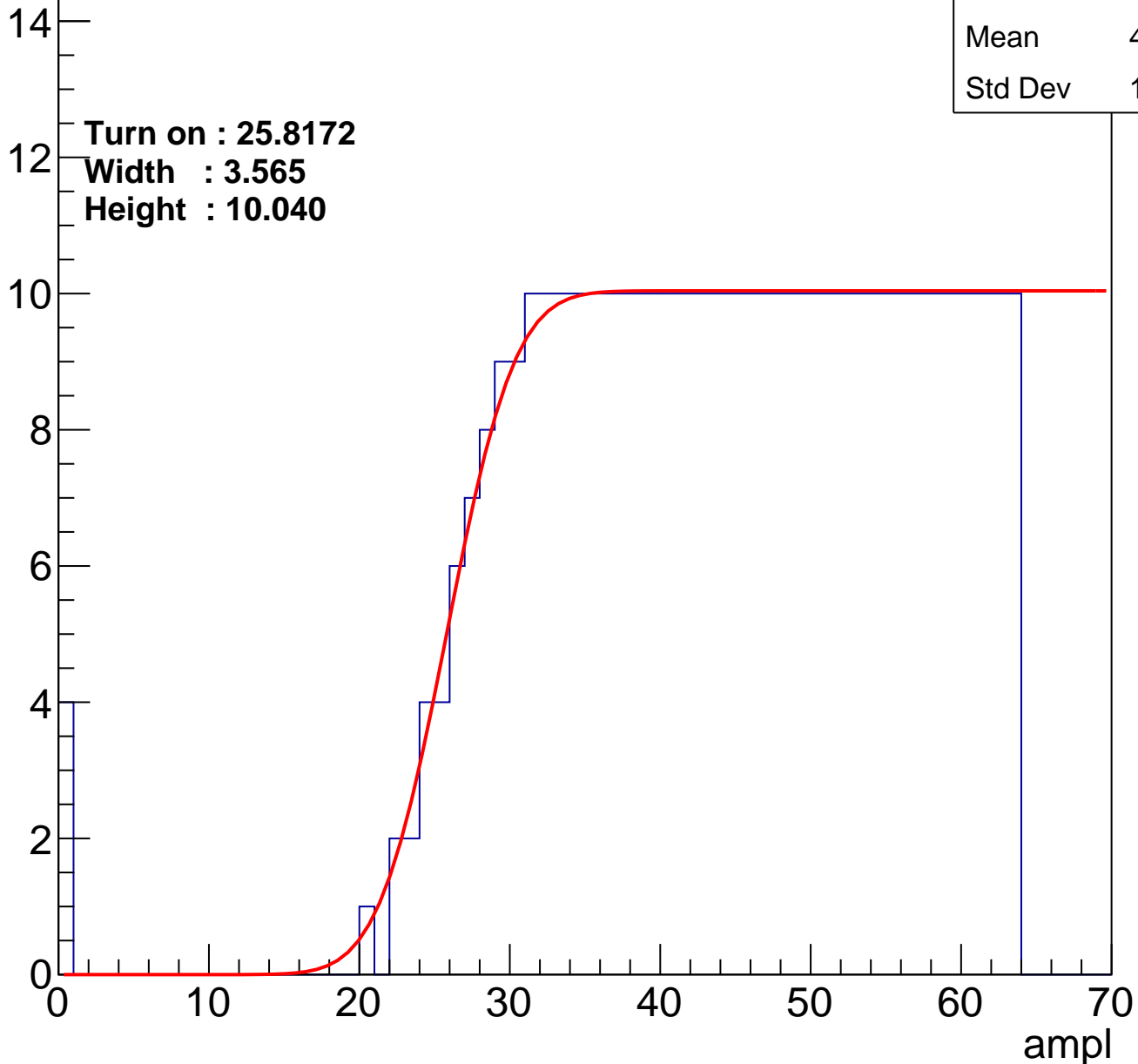
Entries	386
Mean	43.82
Std Dev	12.03

Turn on : 25.8172

Width : 3.565

Height : 10.040

Entry



# B1L003S, U7-ch68

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	373
Mean	44.58
Std Dev	11.39

Turn on : 27.2332

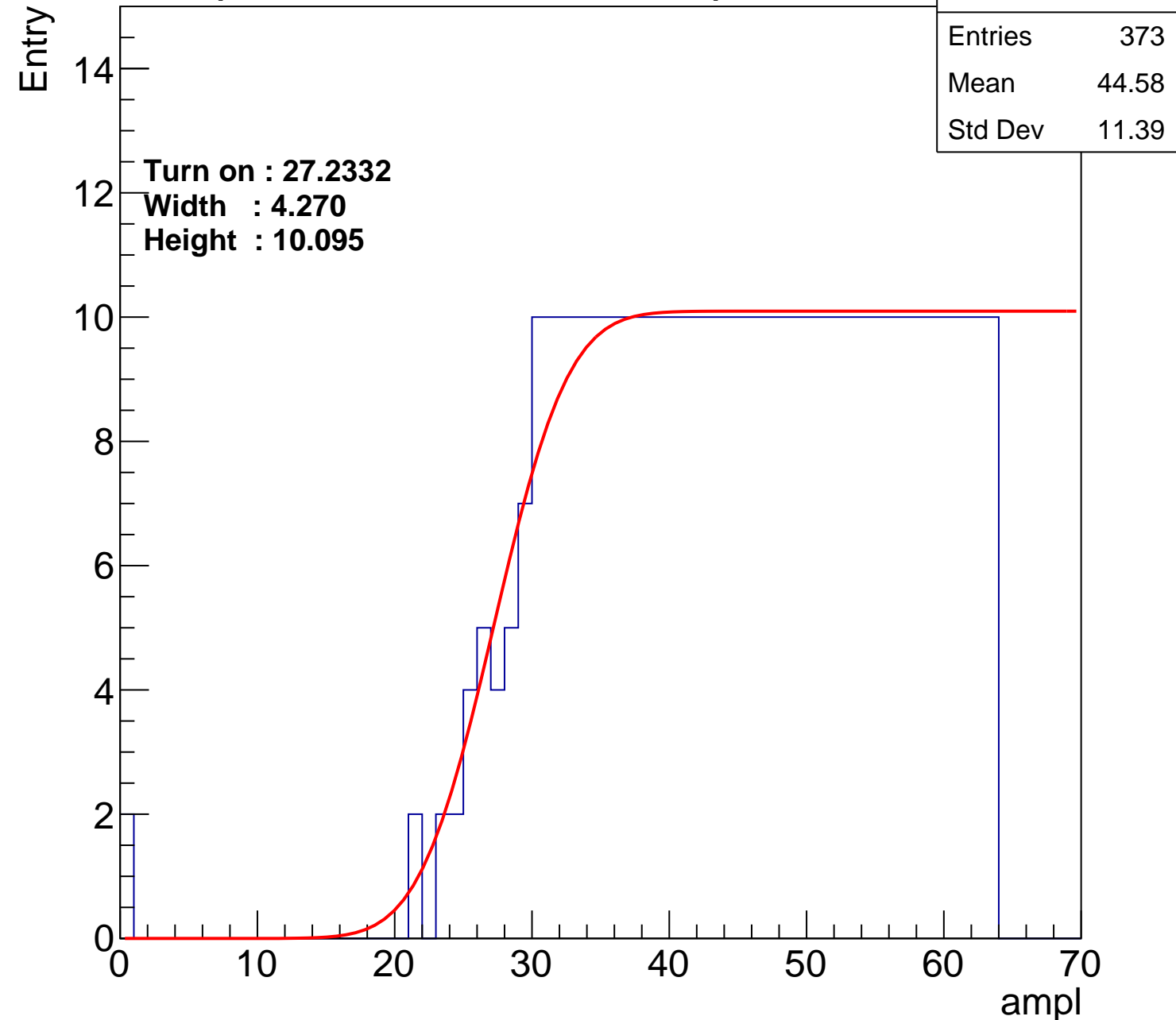
Width : 4.270

Height : 10.095

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch69

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	378
Mean	44.46
Std Dev	11.22

**Turn on : 26.3153**

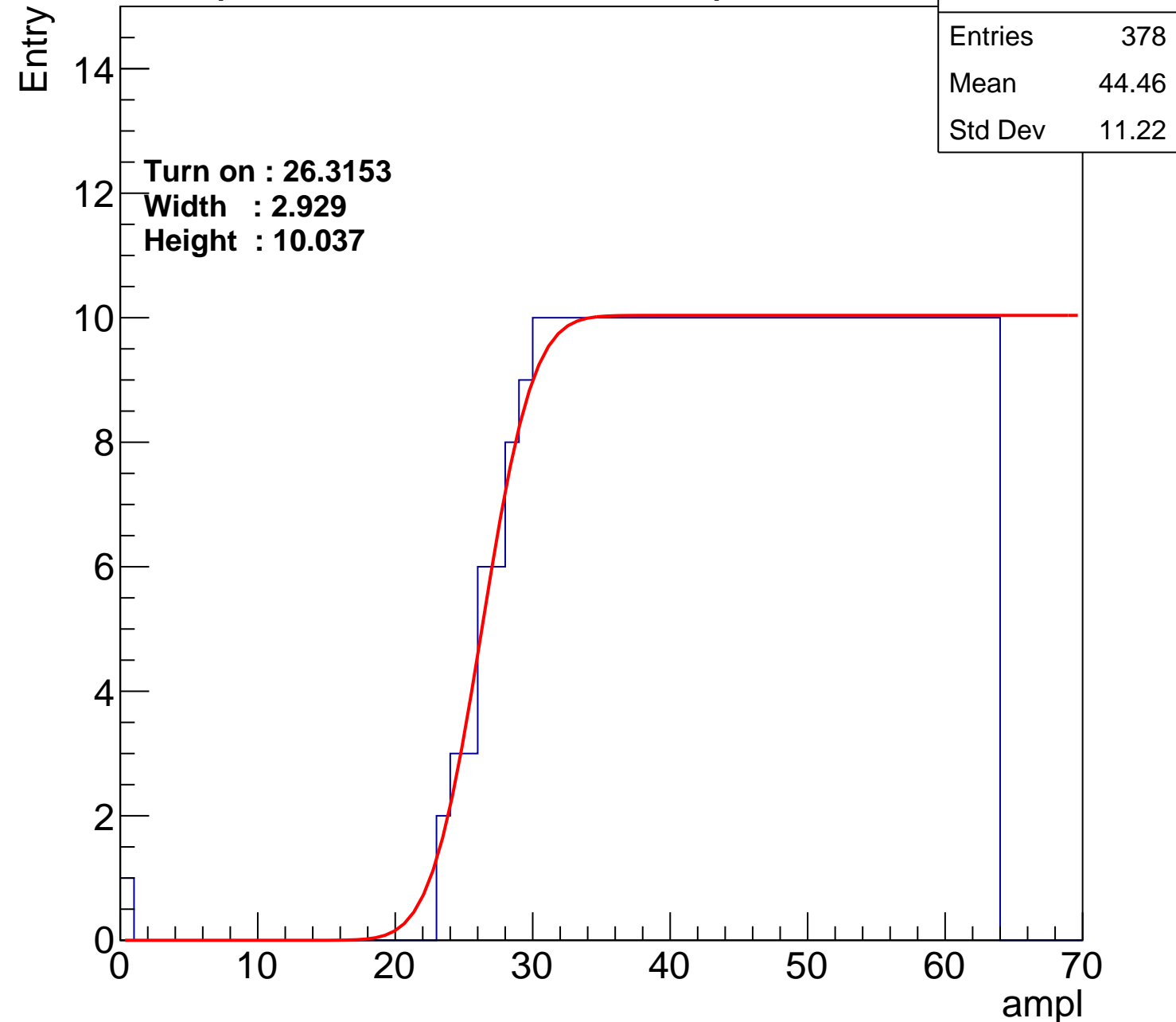
**Width : 2.929**

**Height : 10.037**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch70

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	380
Mean	44.39
Std Dev	11.23

**Turn on : 26.0357**

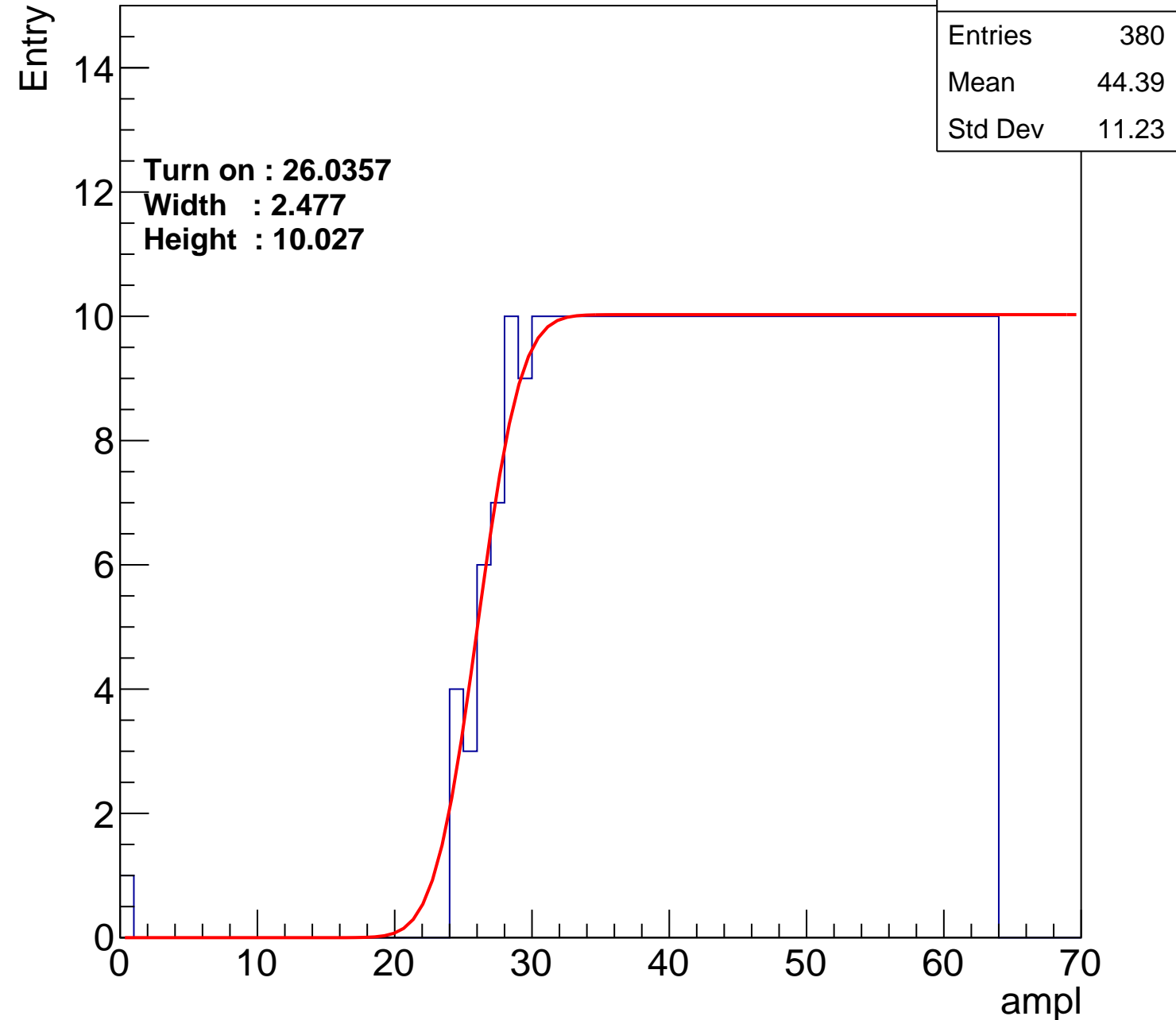
**Width : 2.477**

**Height : 10.027**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L003S, U7-ch71

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	369
Mean	44.8
Std Dev	11.24

Turn on : 28.1250

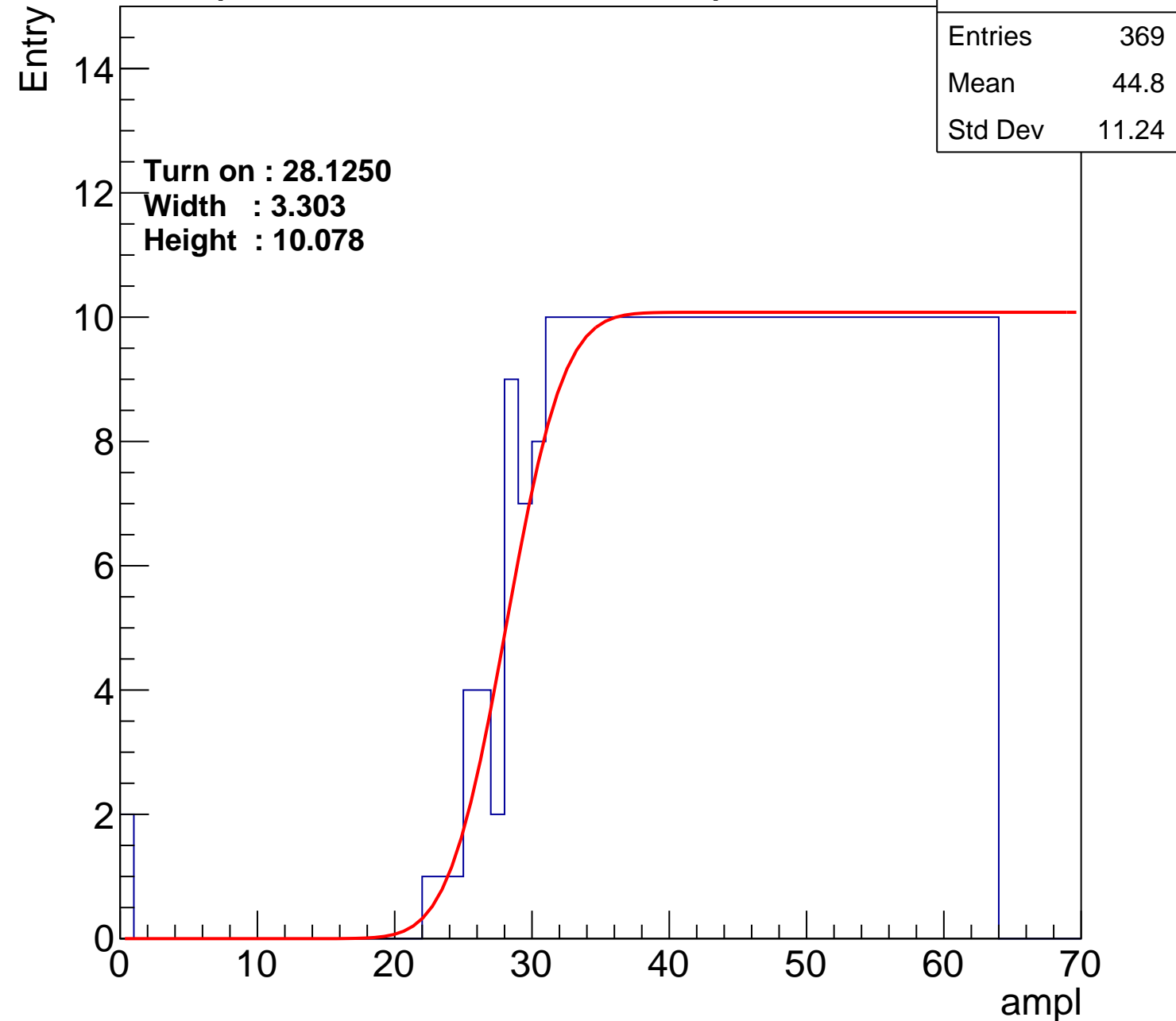
Width : 3.303

Height : 10.078

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch72

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	369
Mean	44.79
Std Dev	11.25

Turn on : 27.2914

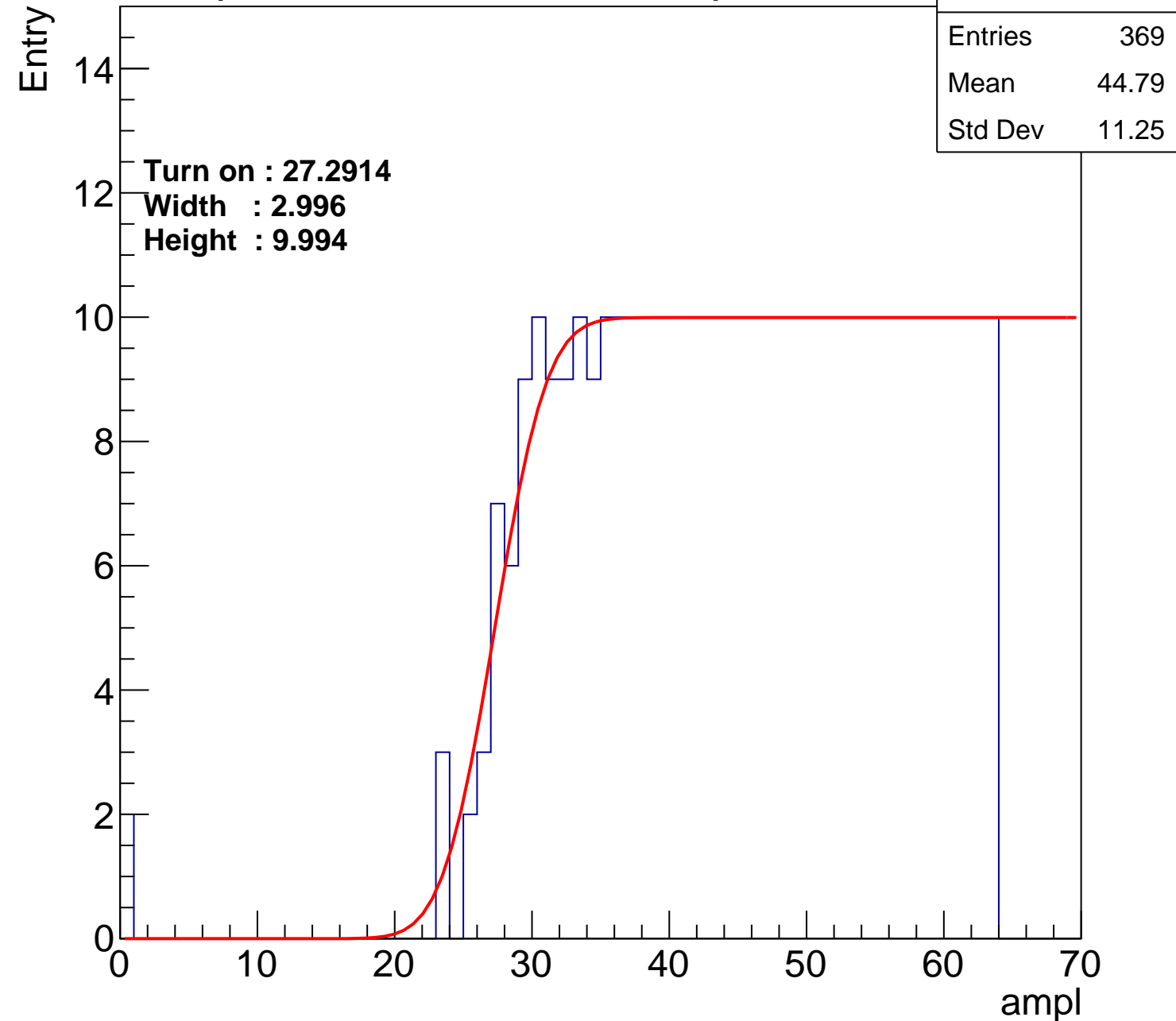
Width : 2.996

Height : 9.994

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch73

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	354
Mean	45.34
Std Dev	11.37

Turn on : 30.2582

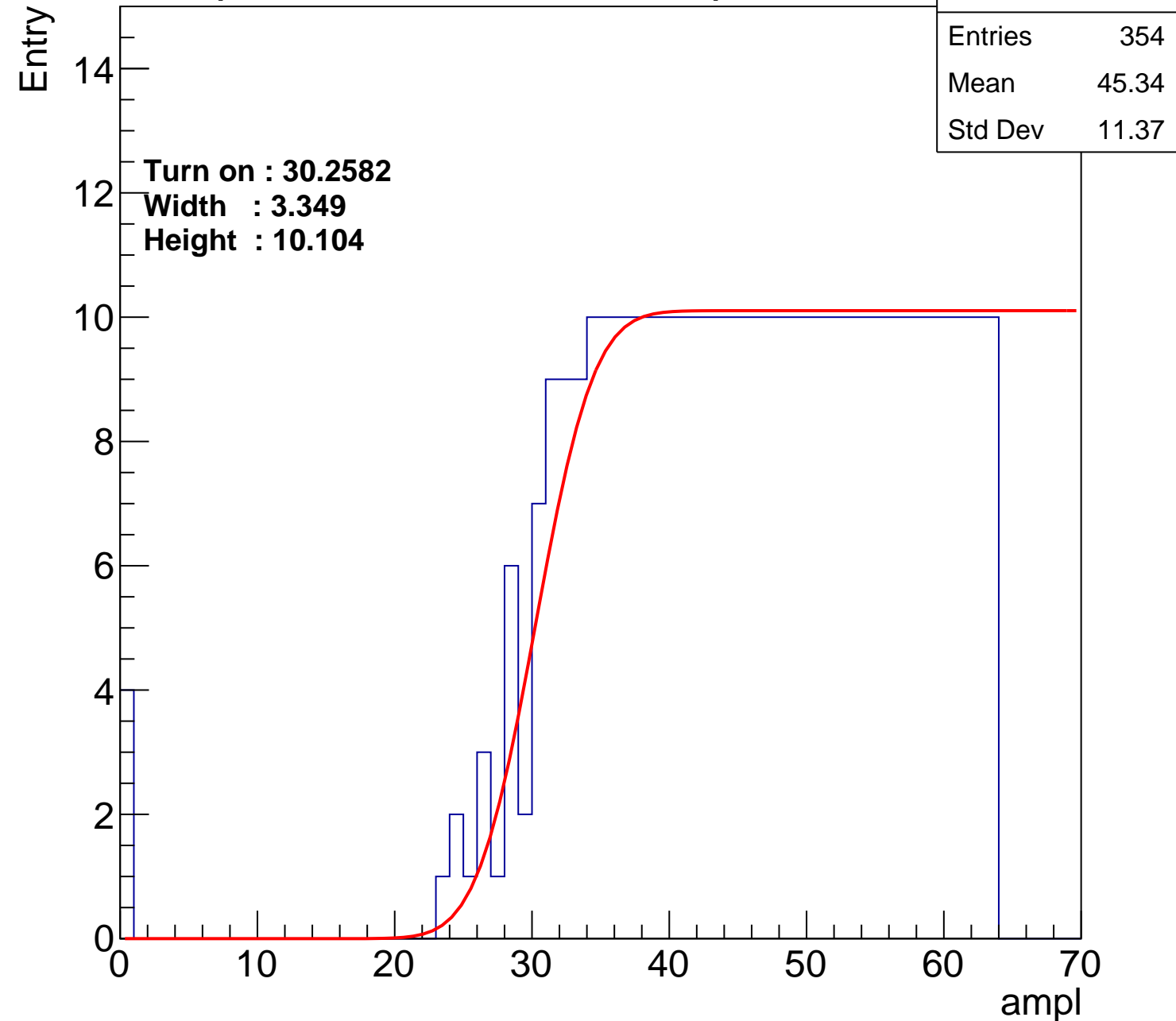
Width : 3.349

Height : 10.104

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch74

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	367
Mean	44.66
Std Dev	11.82

Turn on : 29.2184

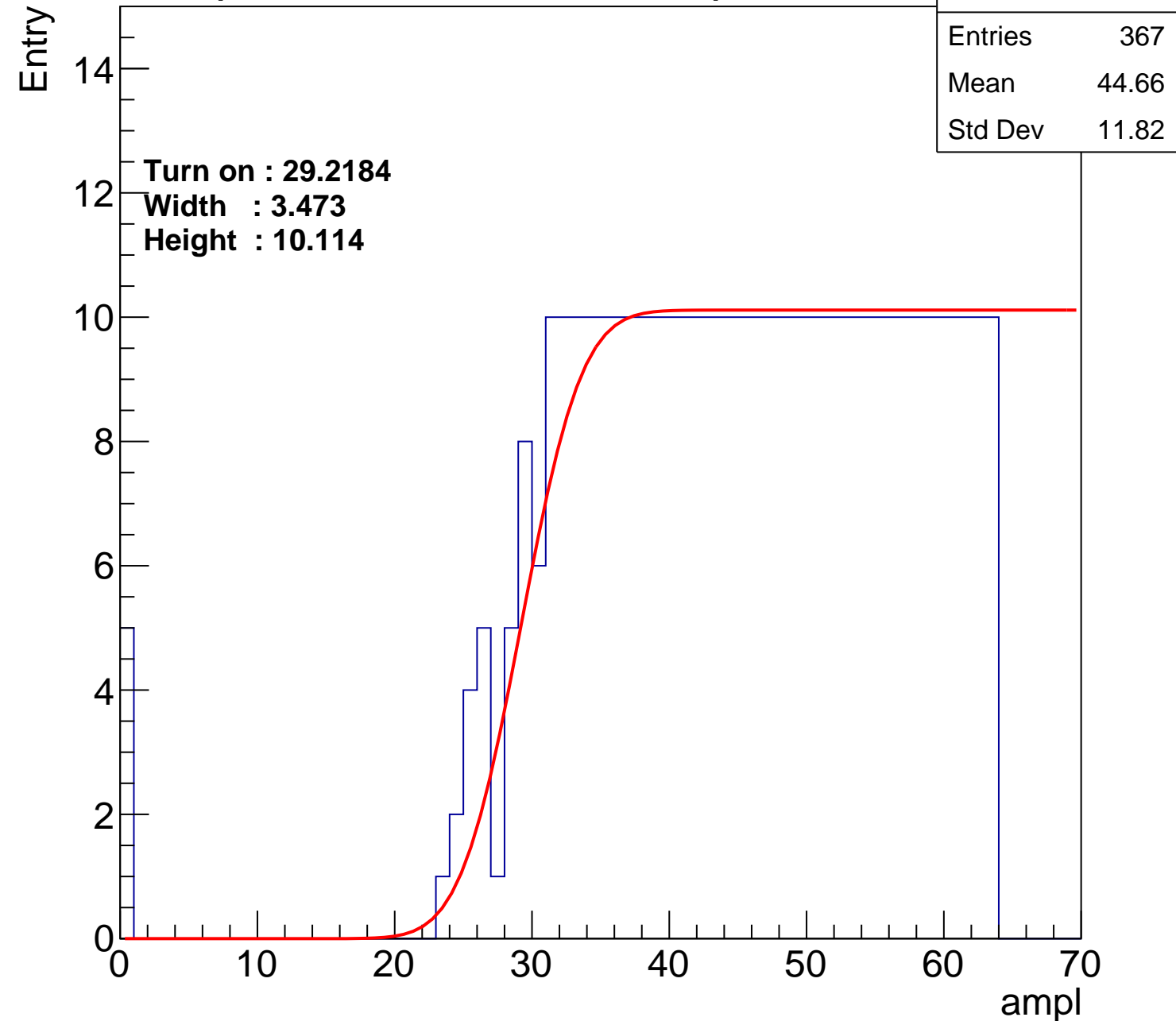
Width : 3.473

Height : 10.114

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch75

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	365
Mean	44.99
Std Dev	11.16

Turn on : 27.9656

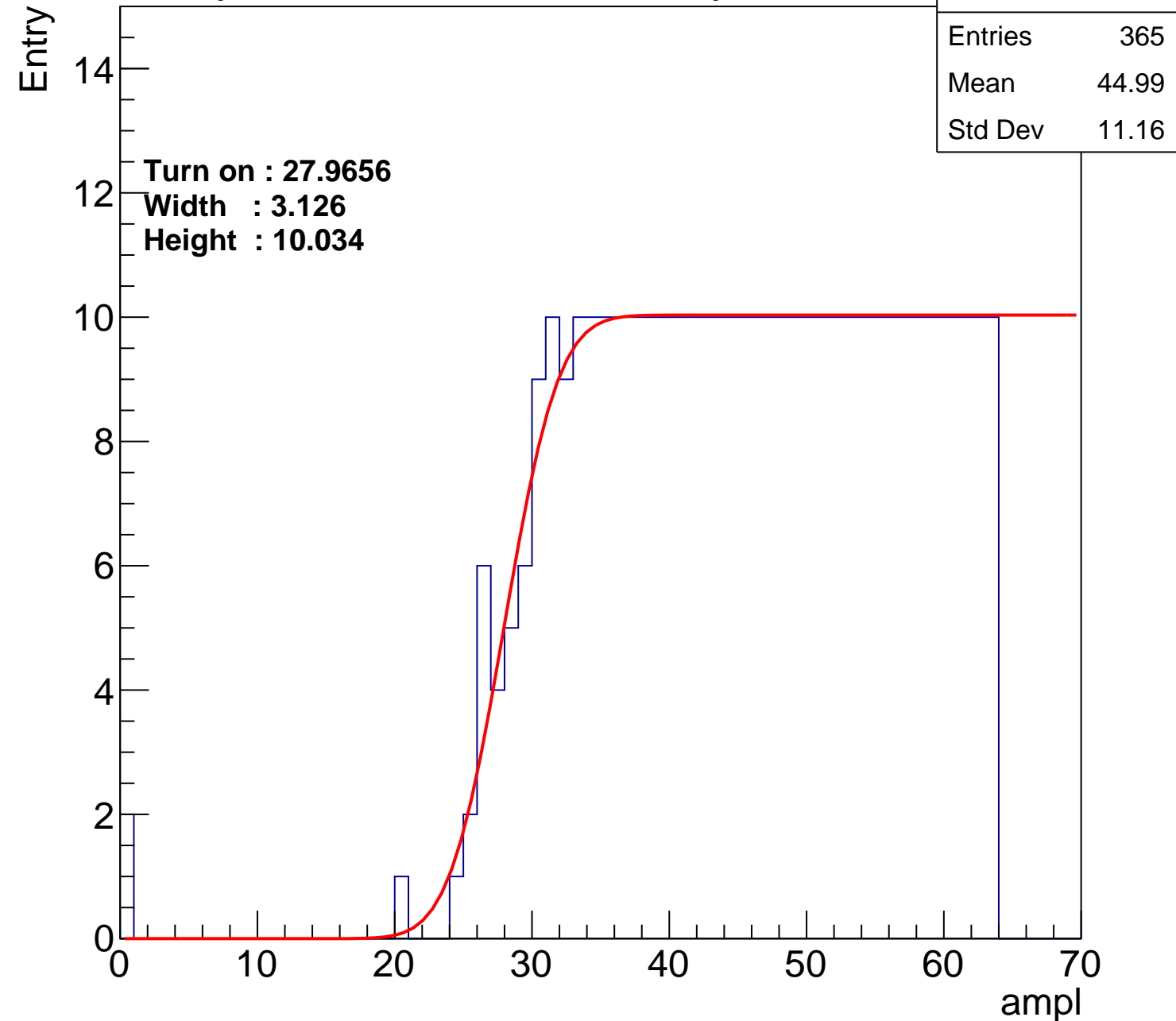
Width : 3.126

Height : 10.034

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch76

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	367
Mean	44.84
Std Dev	11.38

Turn on : 28.4831

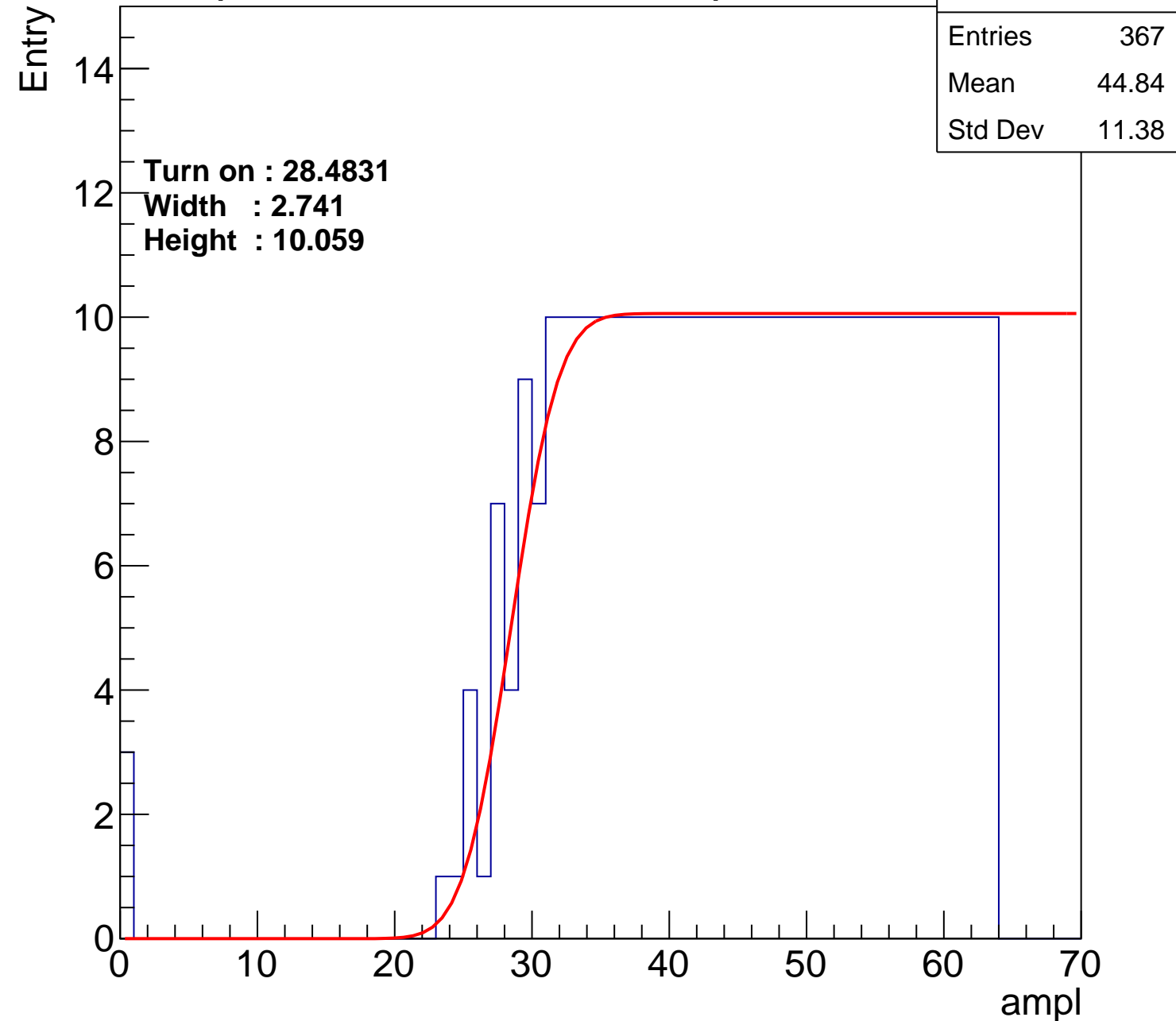
Width : 2.741

Height : 10.059

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch77

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	376
Mean	44.49
Std Dev	11.37

Turn on : 26.9542

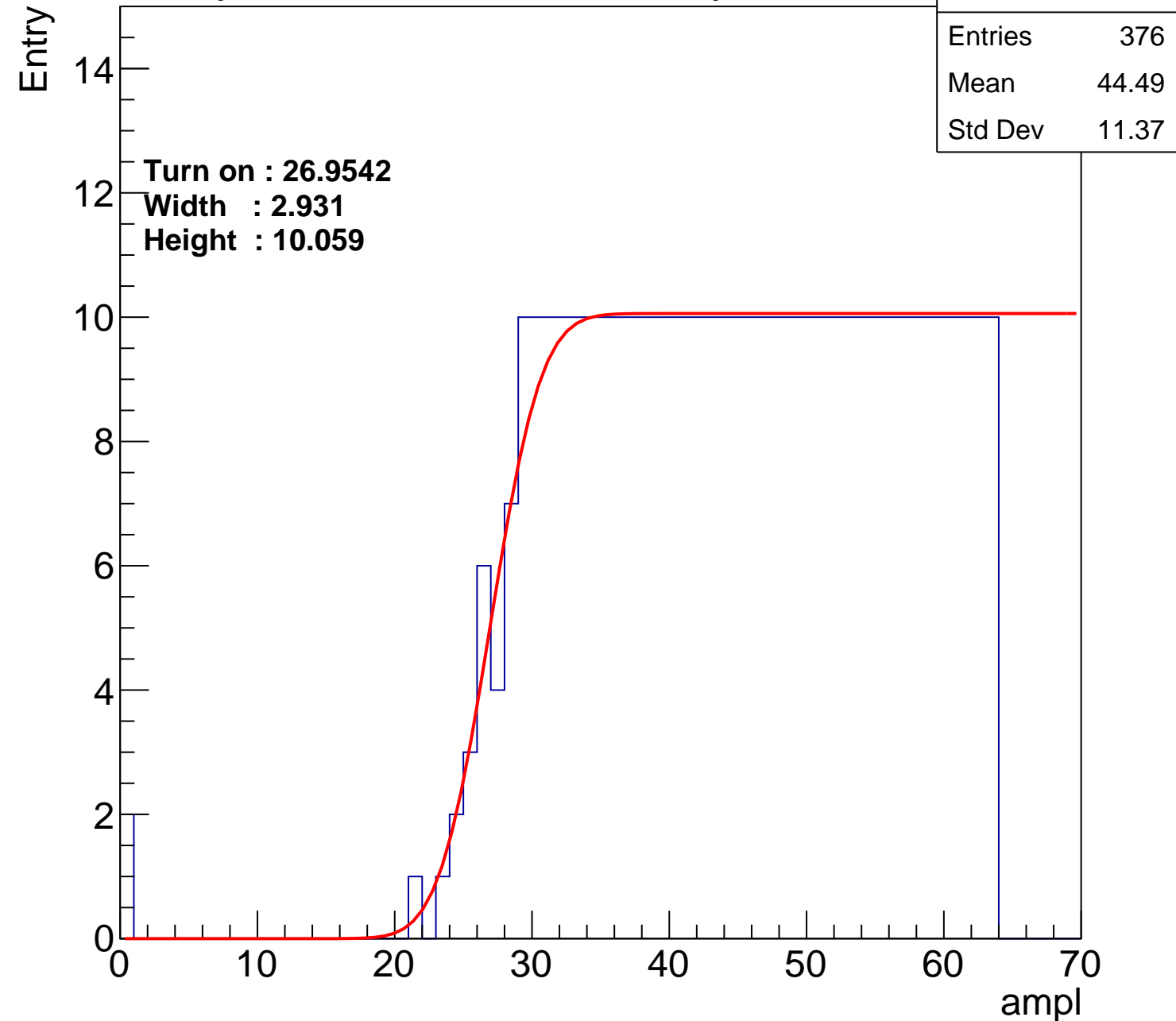
Width : 2.931

Height : 10.059

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



B1L003S, U7-ch78

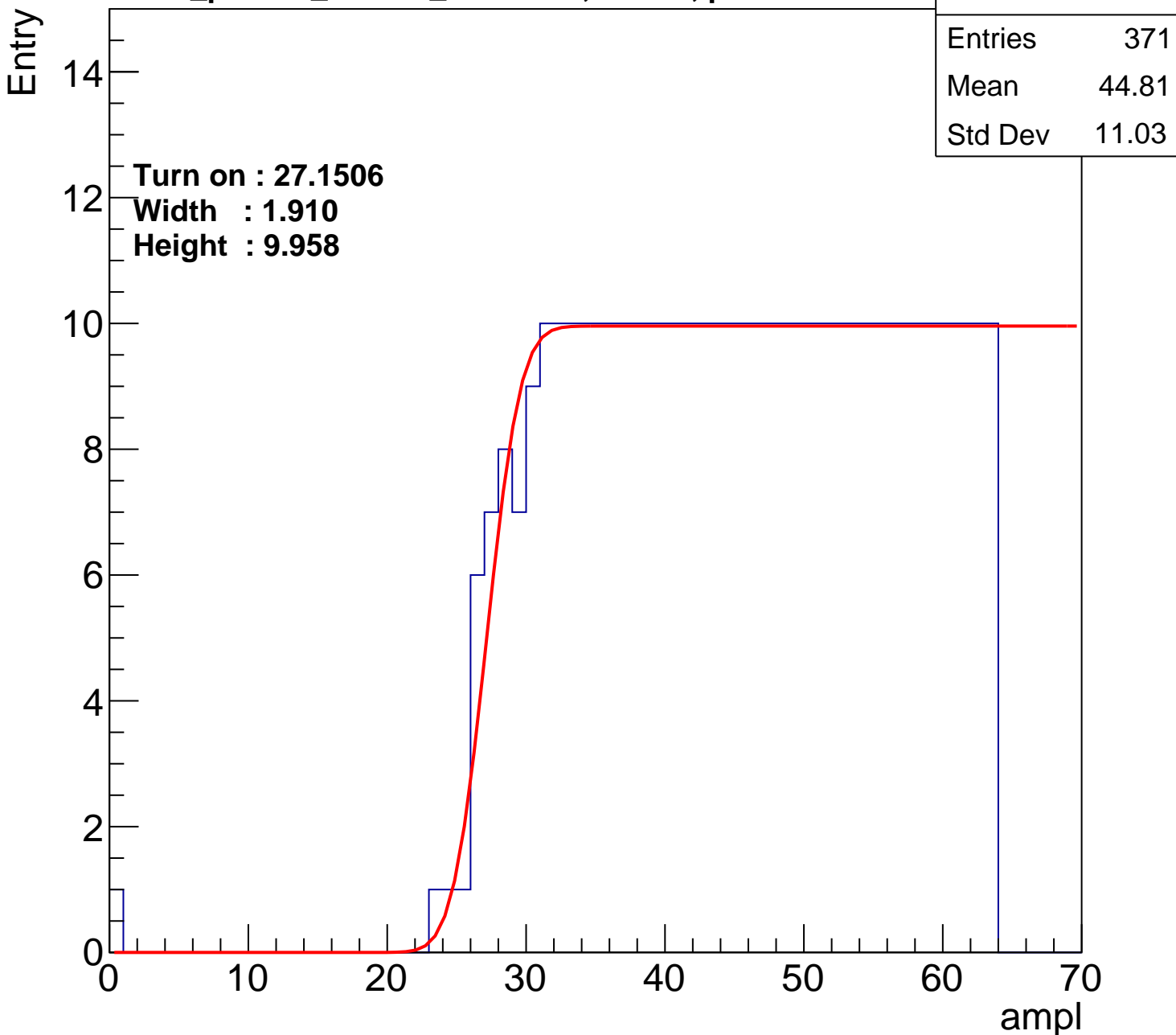
**calib\_packv5\_042523\_0143.root, FC#13, port D2**

**Turn on : 27.1506**

**Width : 1.910**

**Height : 9.958**

Entries	371
Mean	44.81
Std Dev	11.03





# B1L003S, U7-ch79

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	339
Mean	46.32
Std Dev	10.28

Turn on : 30.4811

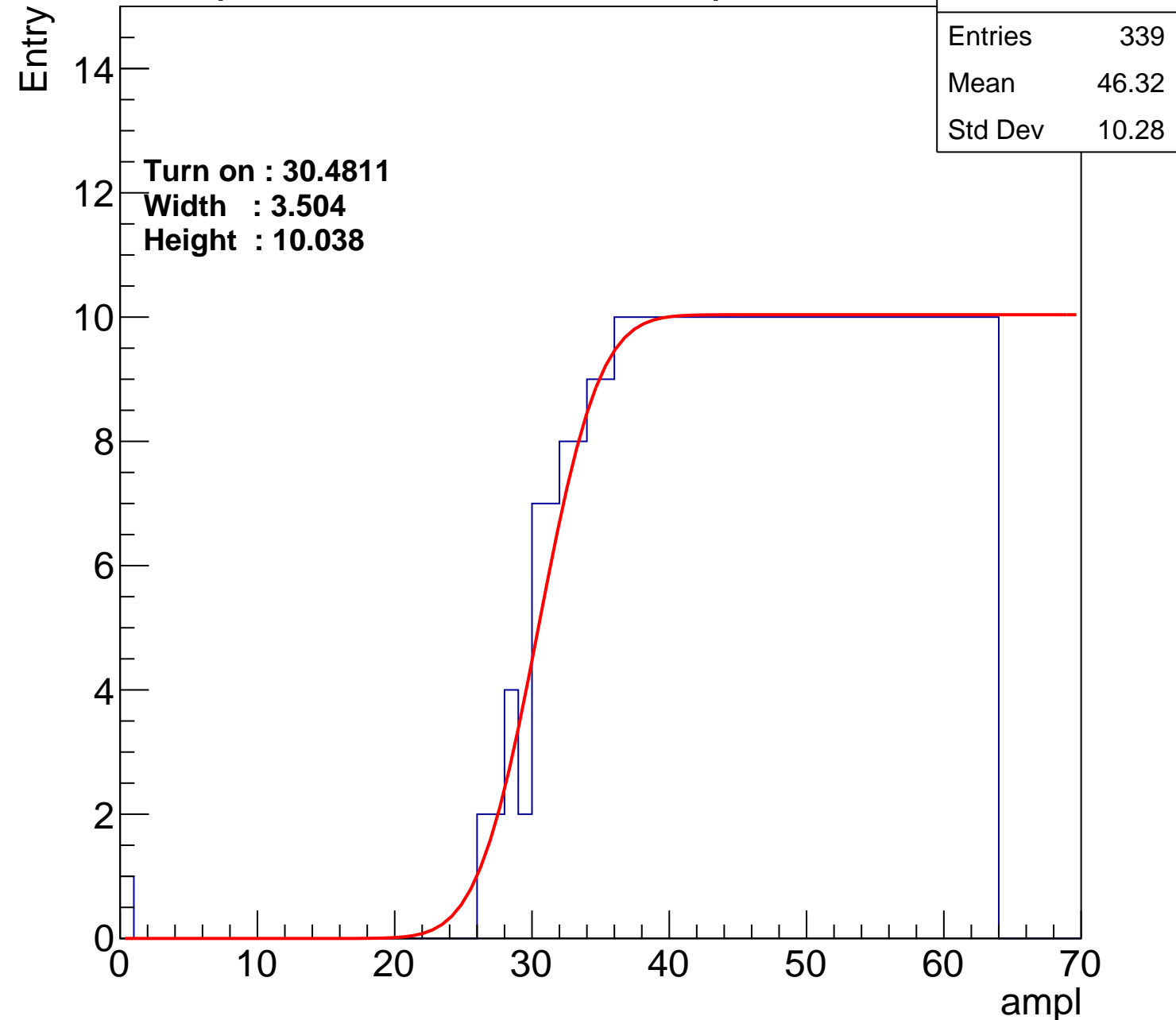
Width : 3.504

Height : 10.038

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch80

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	379
Mean	44.27
Std Dev	11.63

**Turn on : 26.6560**

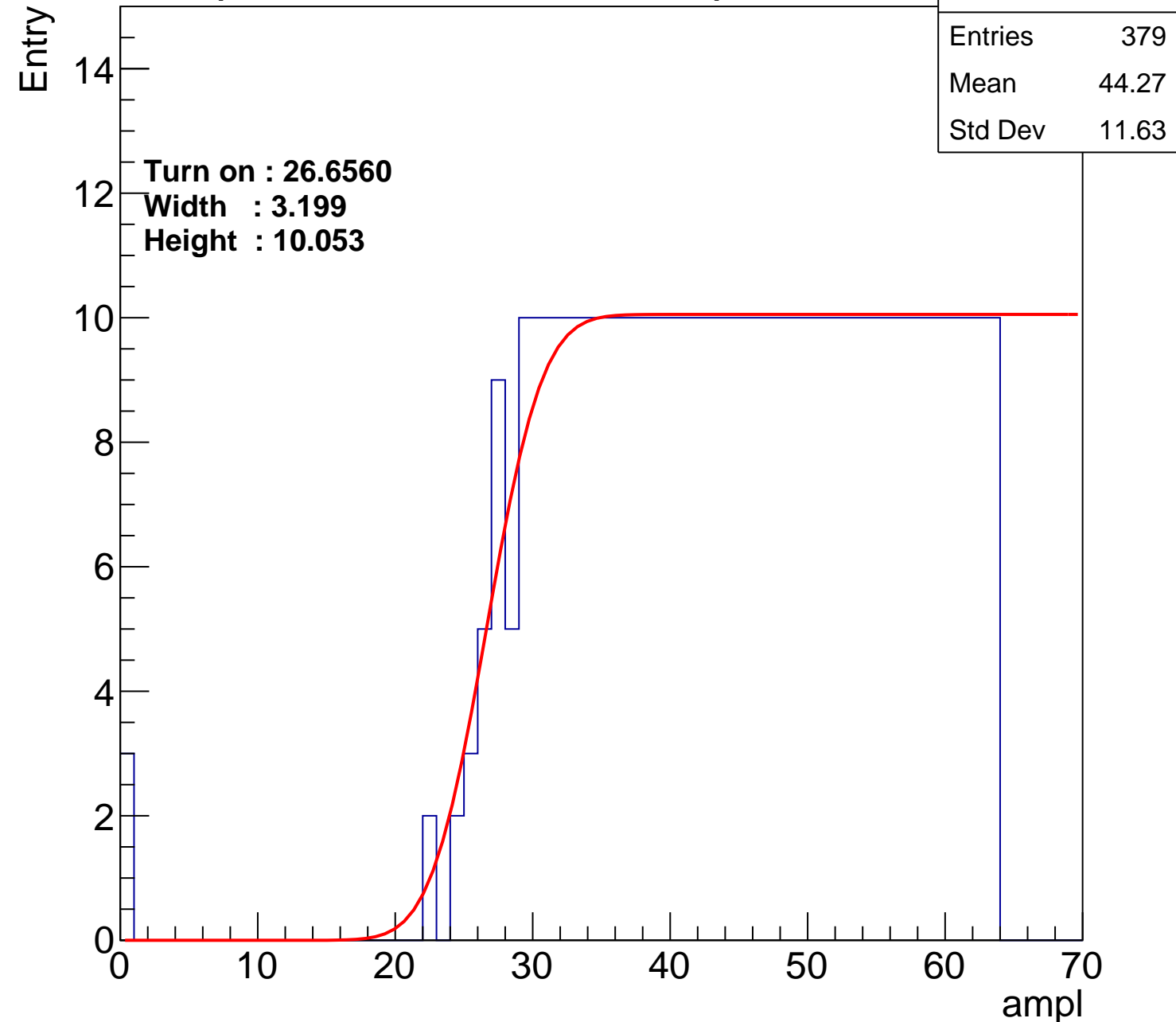
**Width : 3.199**

**Height : 10.053**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch81

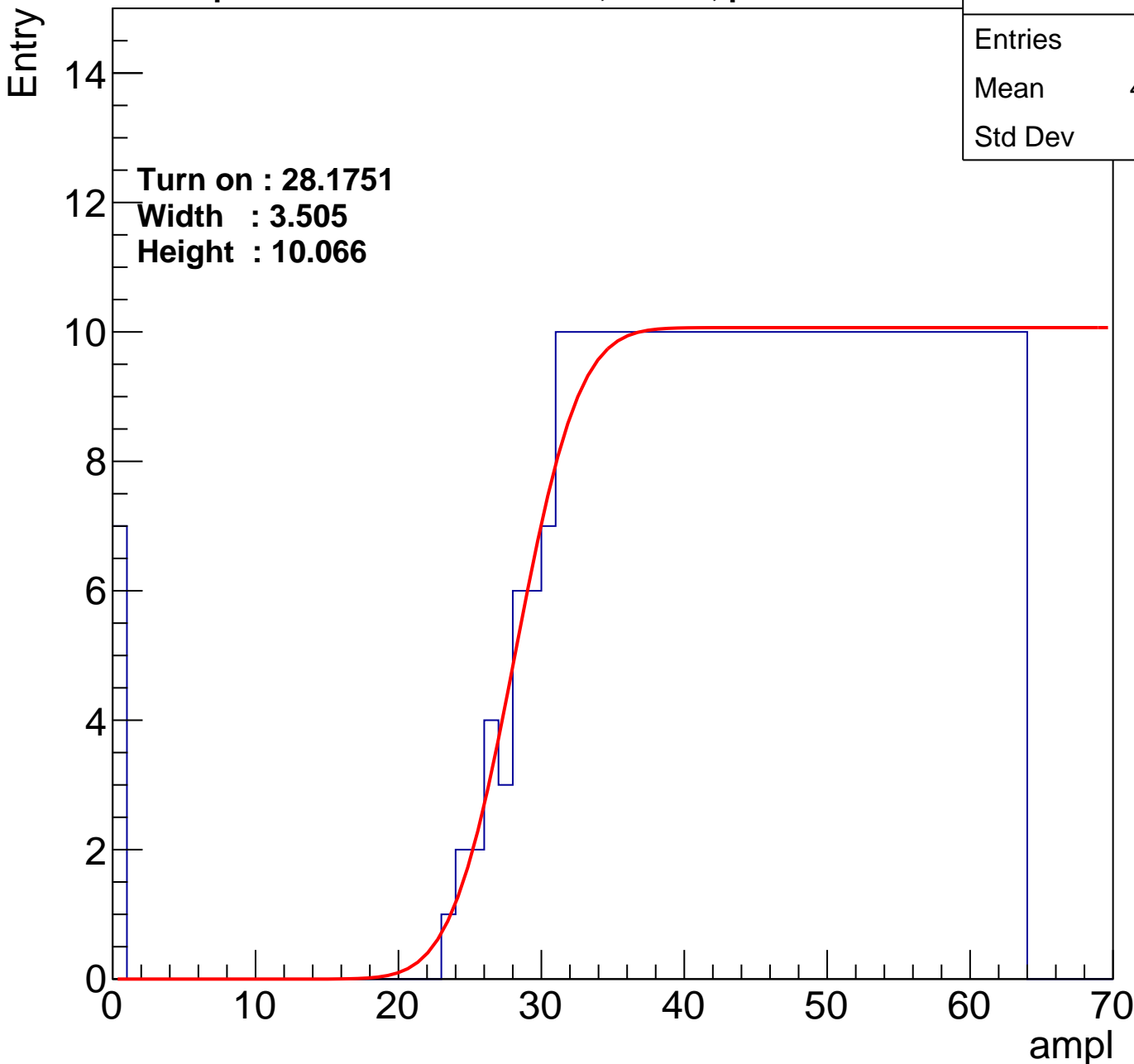
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	368
Mean	44.48
Std Dev	12.2

Turn on : 28.1751

Width : 3.505

Height : 10.066



# B1L003S, U7-ch82

calib\_packv5\_042523\_0143.root, FC#13, port D2

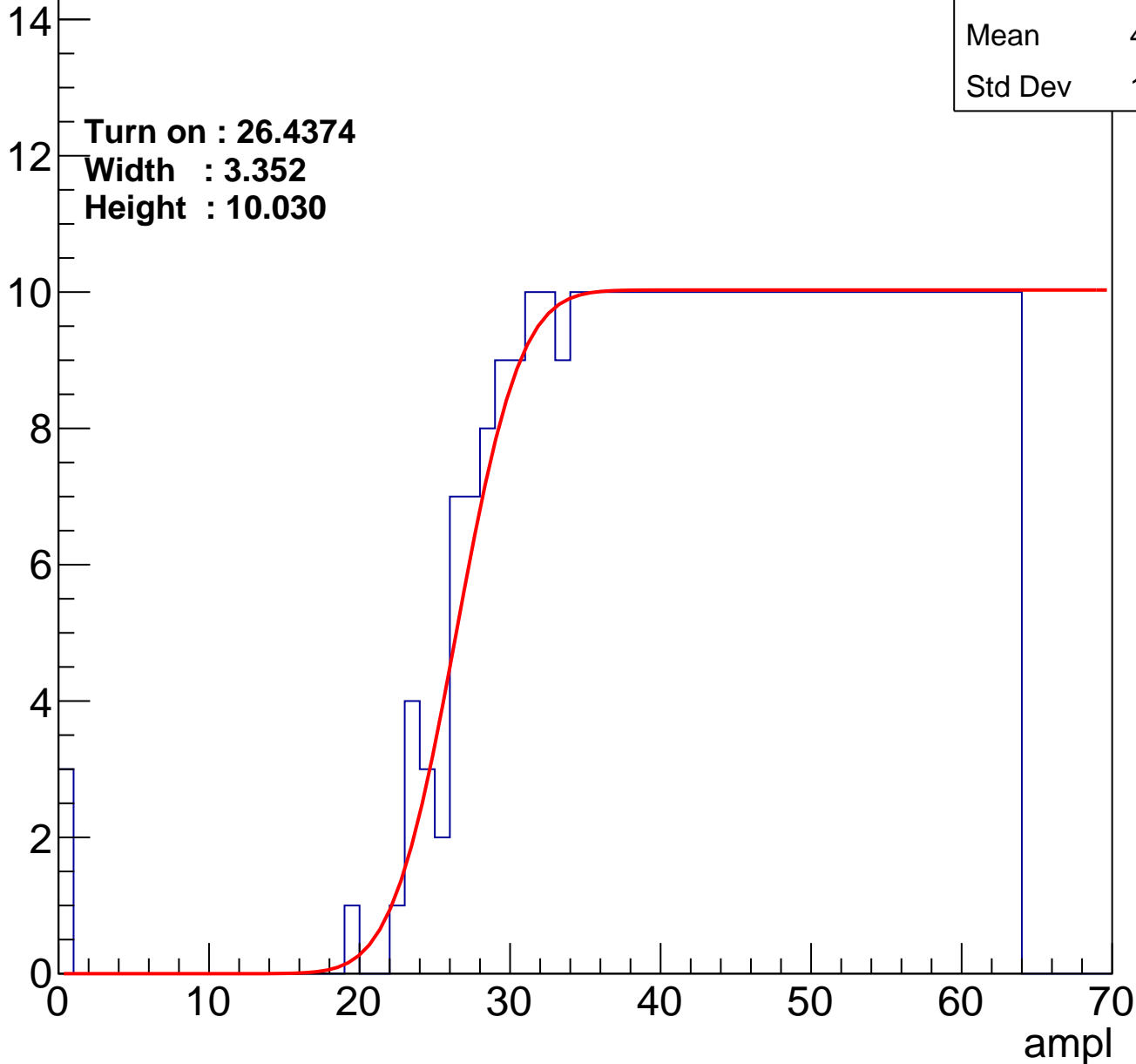
Entries	383
Mean	44.02
Std Dev	11.82

Turn on : 26.4374

Width : 3.352

Height : 10.030

Entry



# B1L003S, U7-ch83

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	345
Mean	45.97
Std Dev	10.67

Turn on : 30.2963

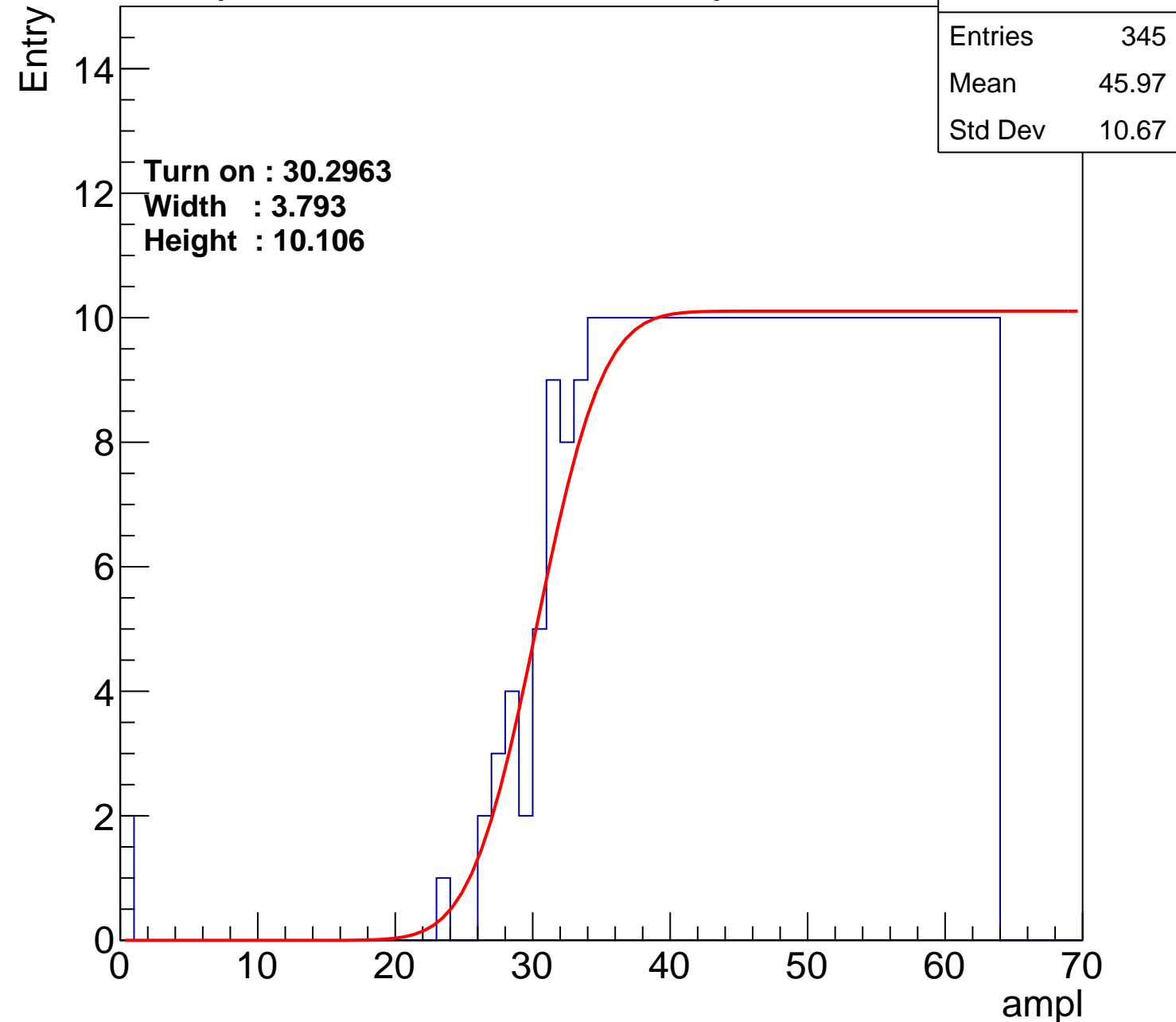
Width : 3.793

Height : 10.106

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch84

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	369
Mean	44.65
Std Dev	11.57

Turn on : 27.8528

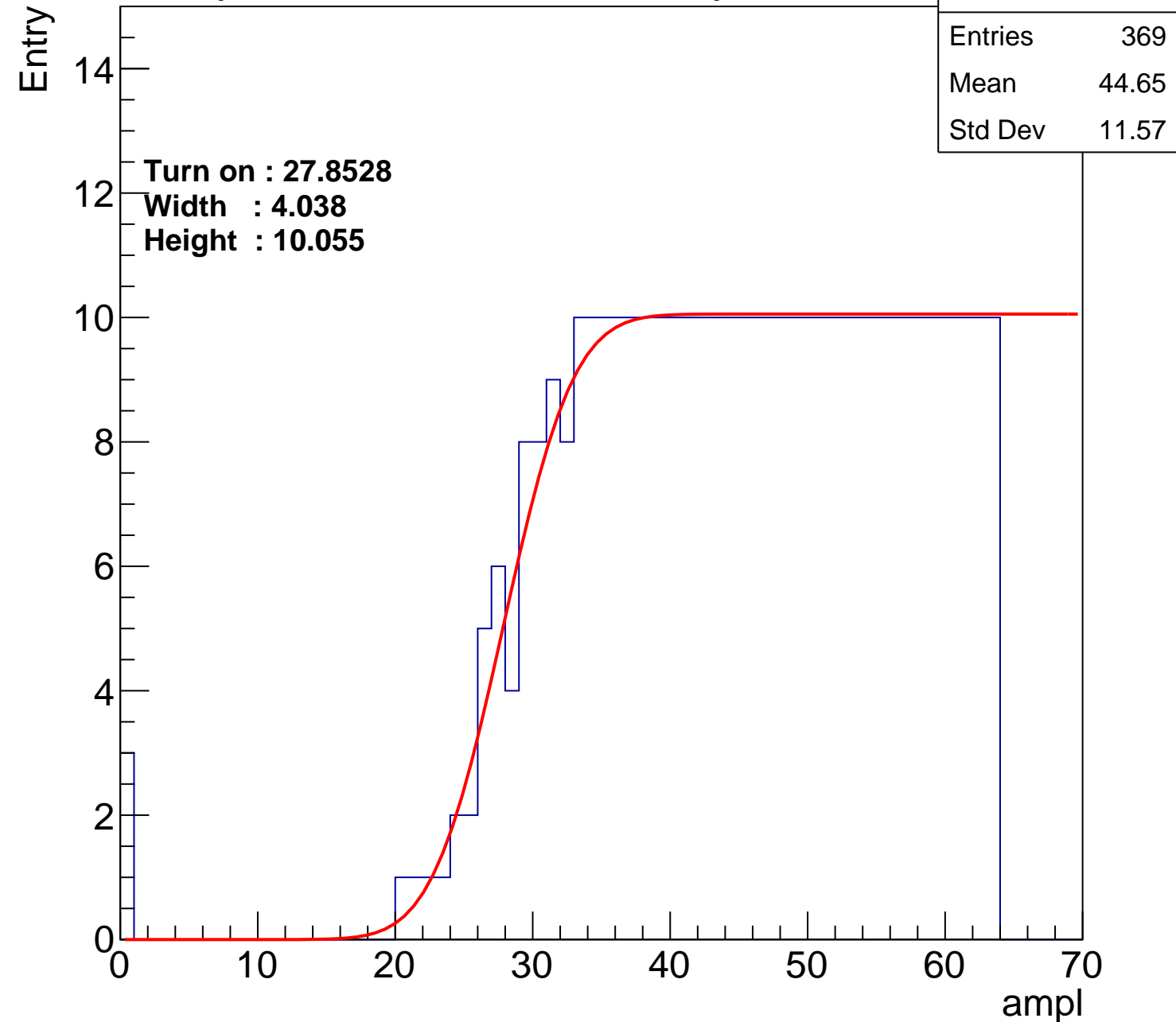
Width : 4.038

Height : 10.055

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch85

calib\_packv5\_042523\_0143.root, FC#13, port D2

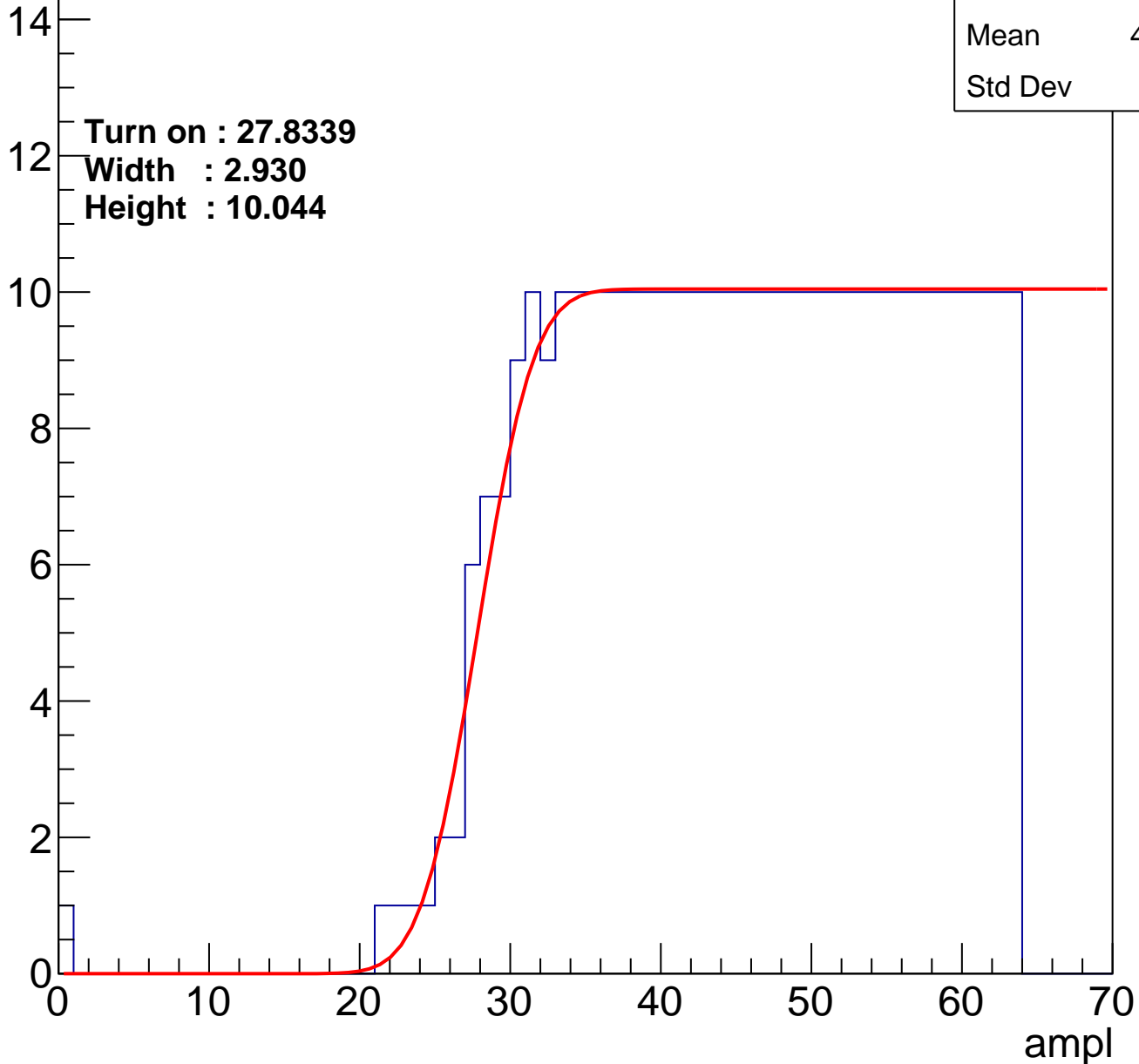
Entries	367
Mean	44.96
Std Dev	11

Turn on : 27.8339

Width : 2.930

Height : 10.044

Entry



# B1L003S, U7-ch86

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	357
Mean	45.41
Std Dev	10.91

**Turn on : 28.9941**

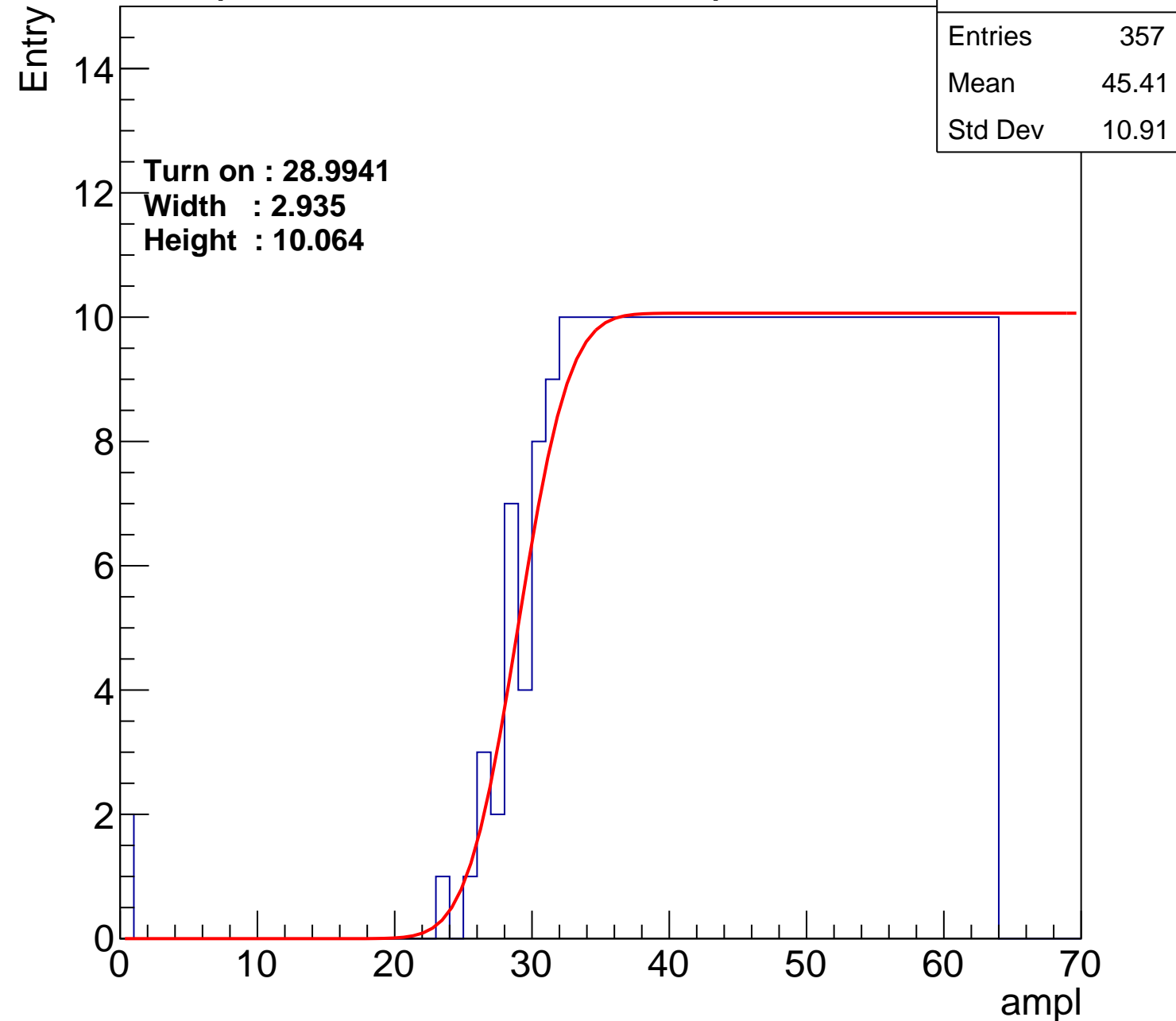
**Width : 2.935**

**Height : 10.064**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L003S, U7-ch87

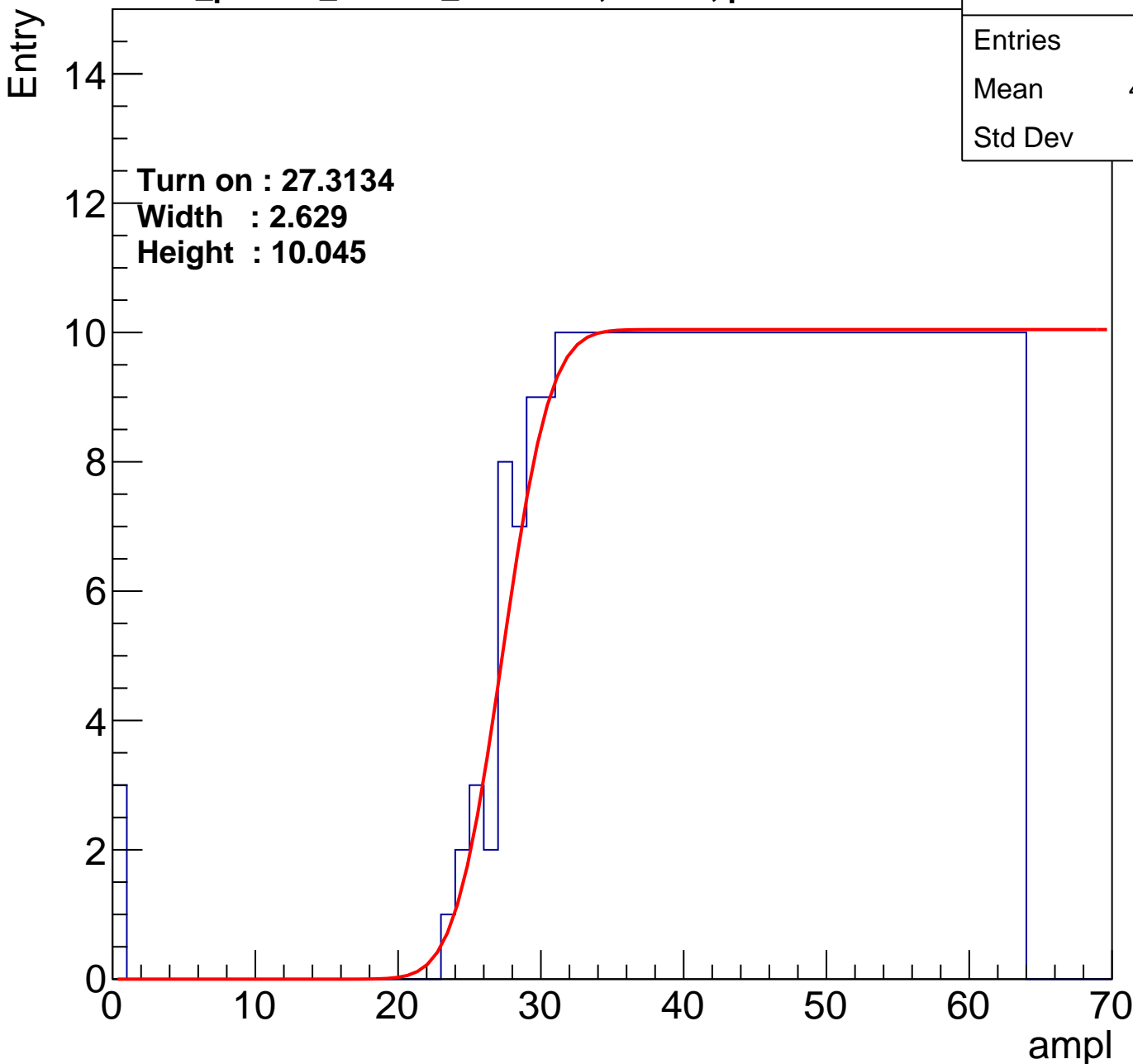
**calib\_packv5\_042523\_0143.root, FC#13, port D2**

Entries	374
Mean	44.52
Std Dev	11.5

**Turn on : 27.3134**

**Width : 2.629**

**Height : 10.045**



# B1L003S, U7-ch88

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	377
Mean	44.42
Std Dev	11.41

**Turn on : 26.4130**

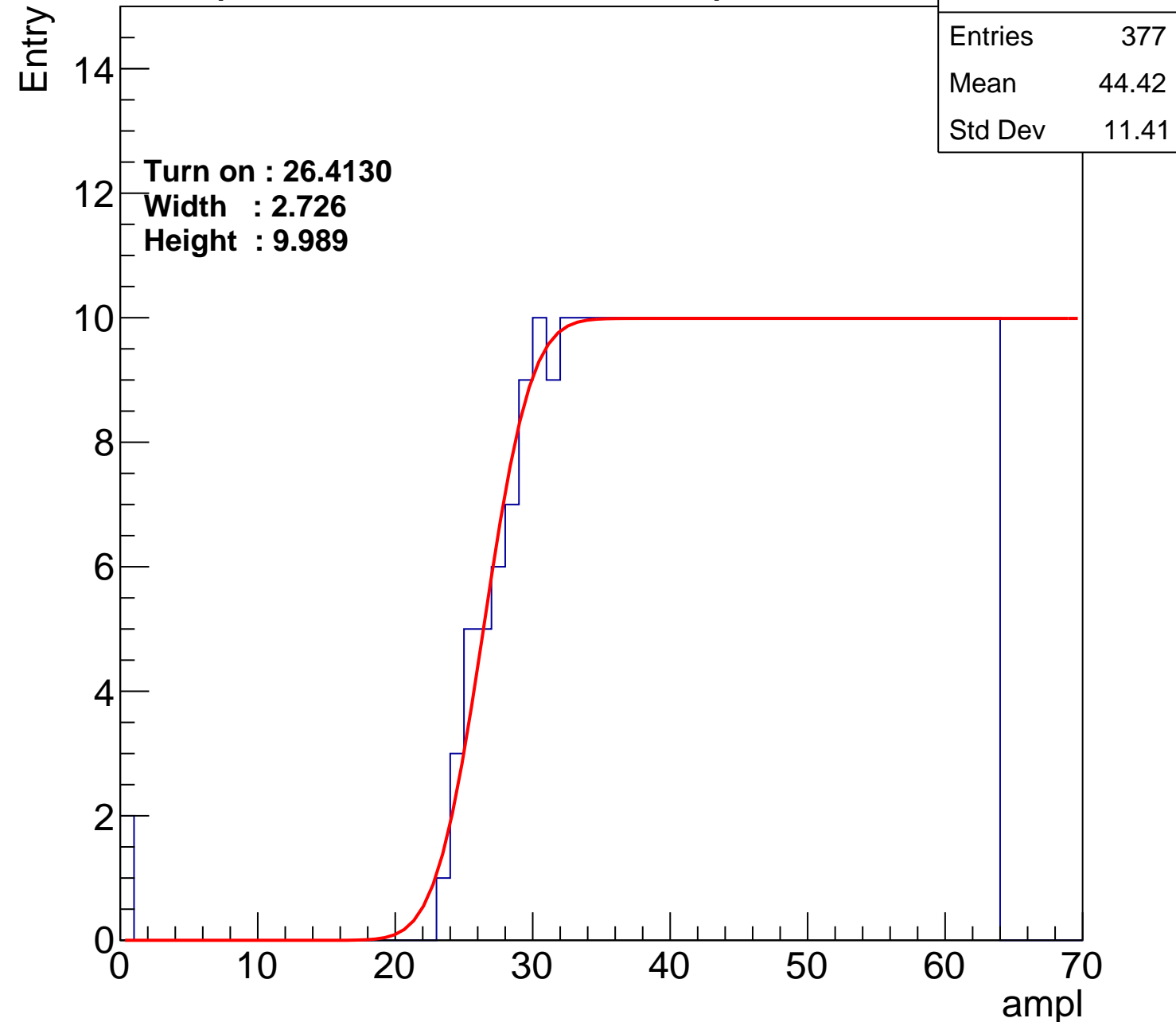
**Width : 2.726**

**Height : 9.989**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch89

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	370
Mean	44.69
Std Dev	11.45

Turn on : 27.7789

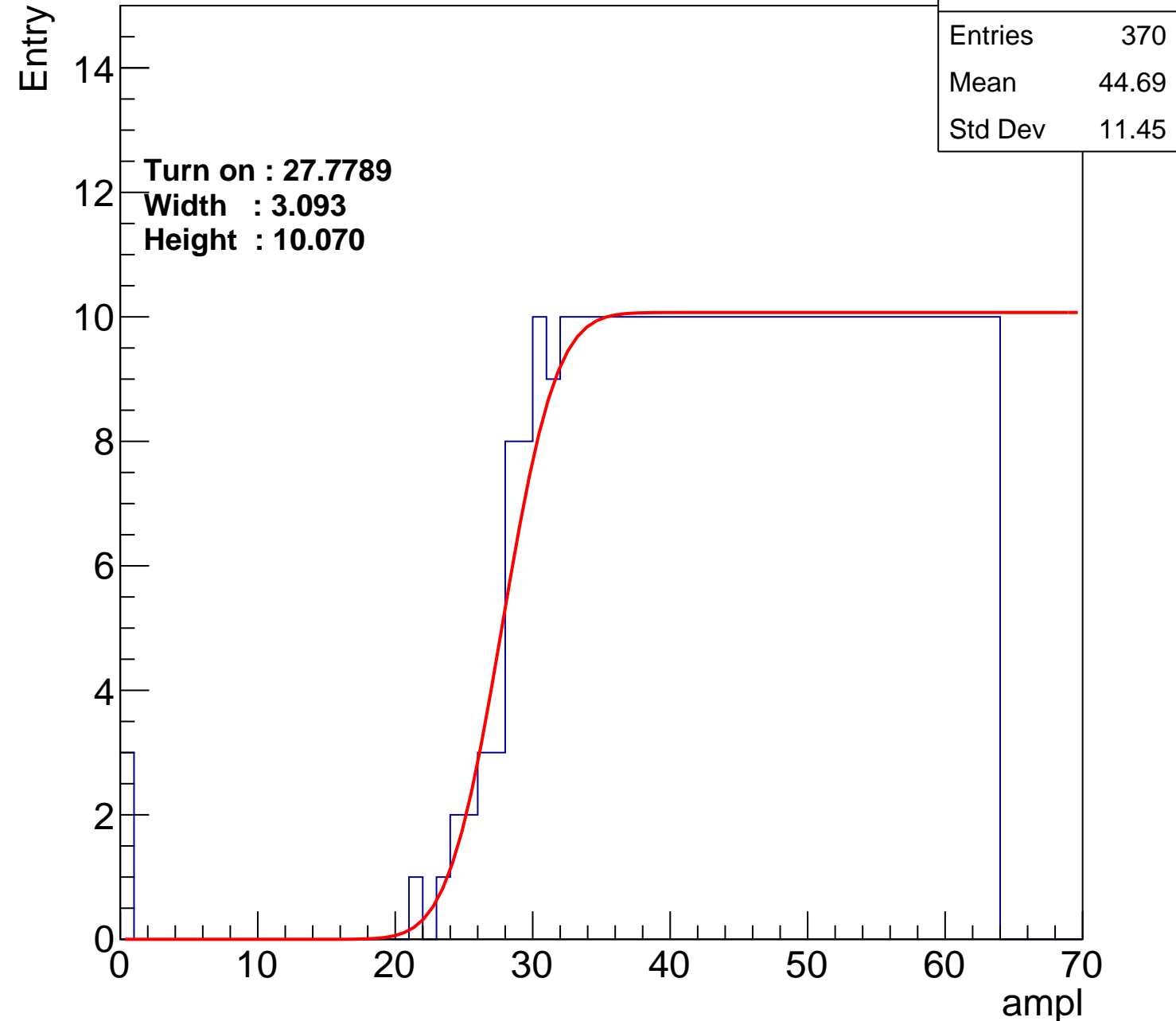
Width : 3.093

Height : 10.070

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch90

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	368
Mean	44.92
Std Dev	11.01

**Turn on : 27.9475**

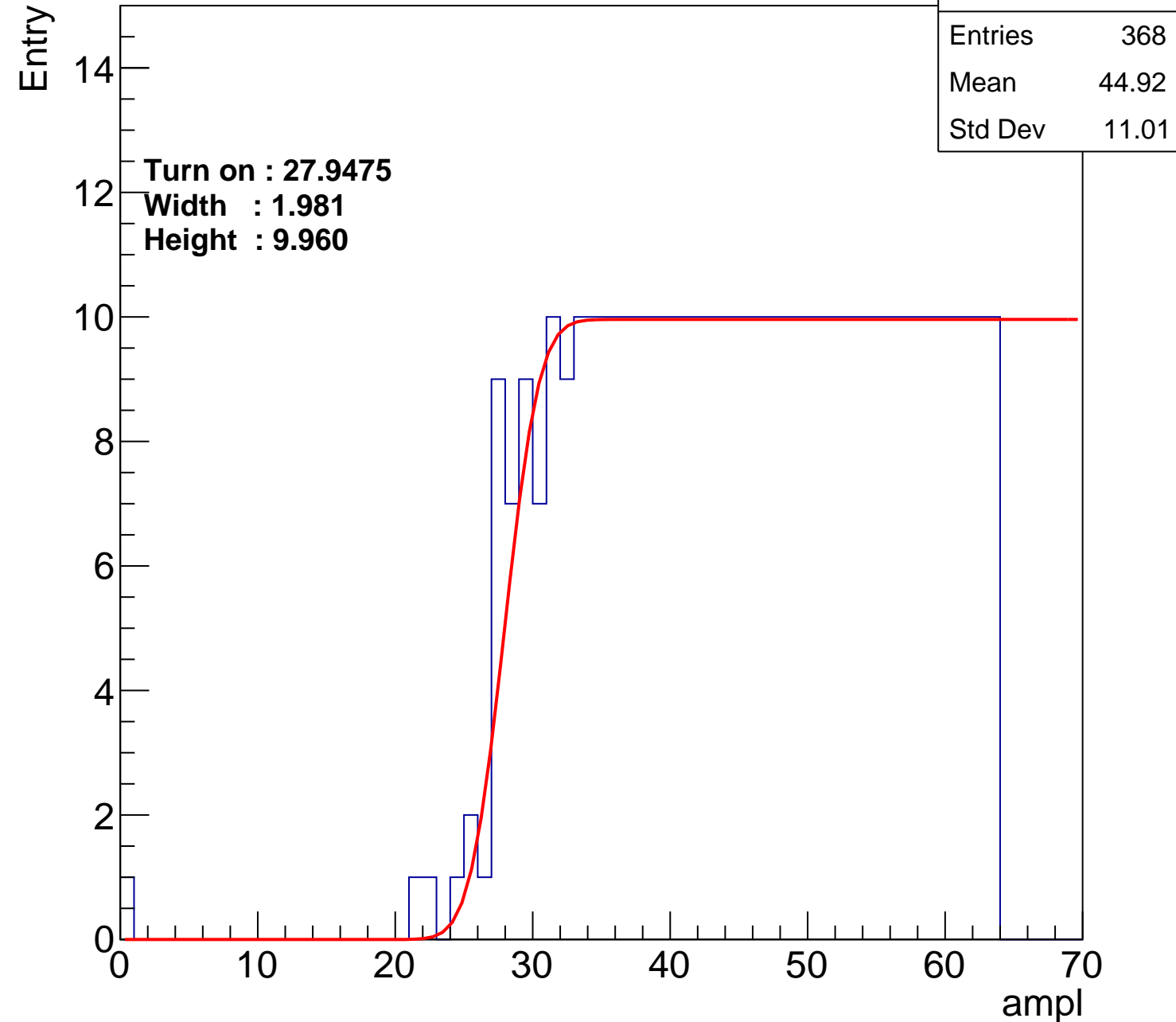
**Width : 1.981**

**Height : 9.960**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch91

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	361
Mean	45.22
Std Dev	10.99

Turn on : 27.8098

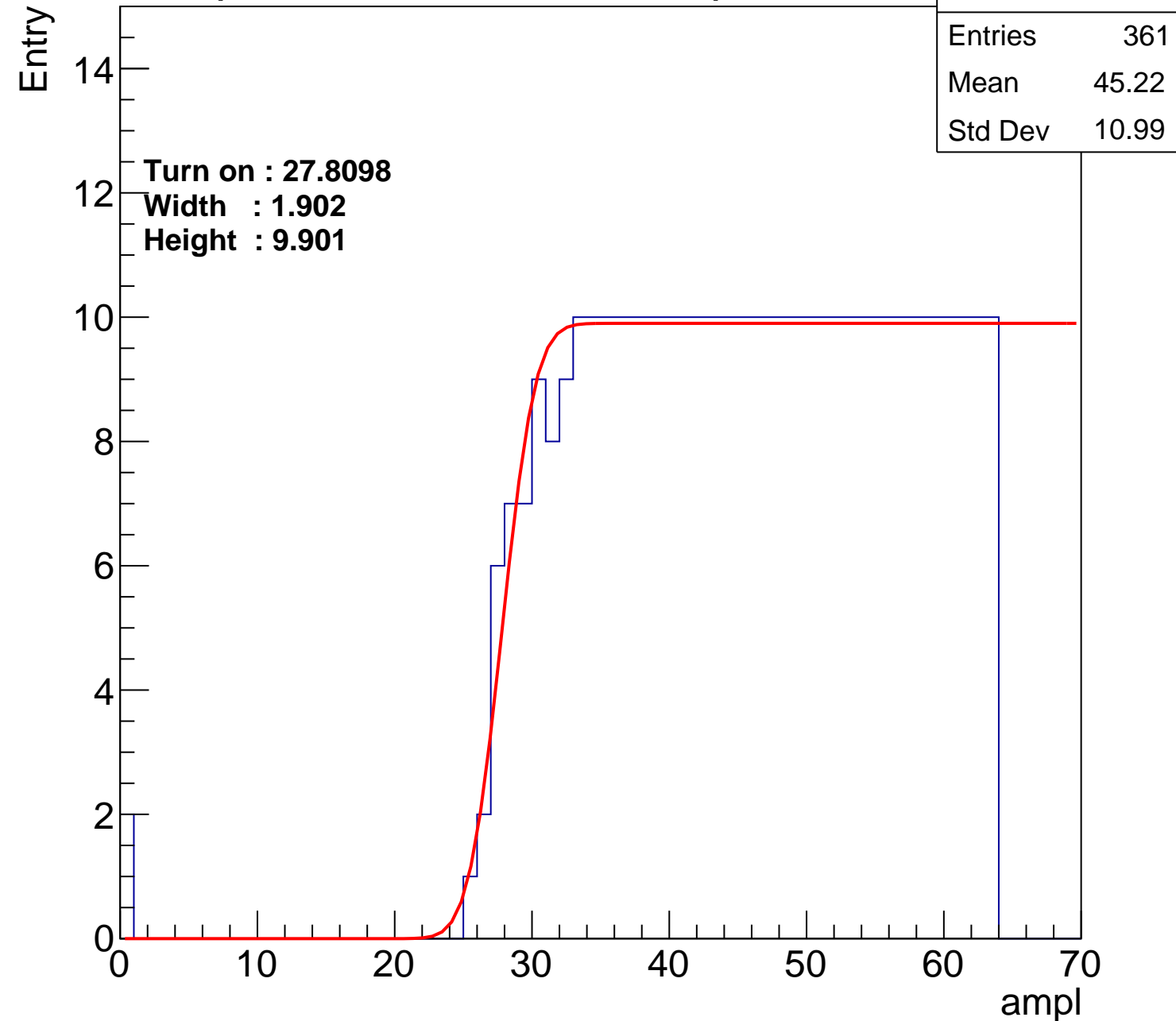
Width : 1.902

Height : 9.901

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch92

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	362
Mean	45.07
Std Dev	11.27

Turn on : 28.4425

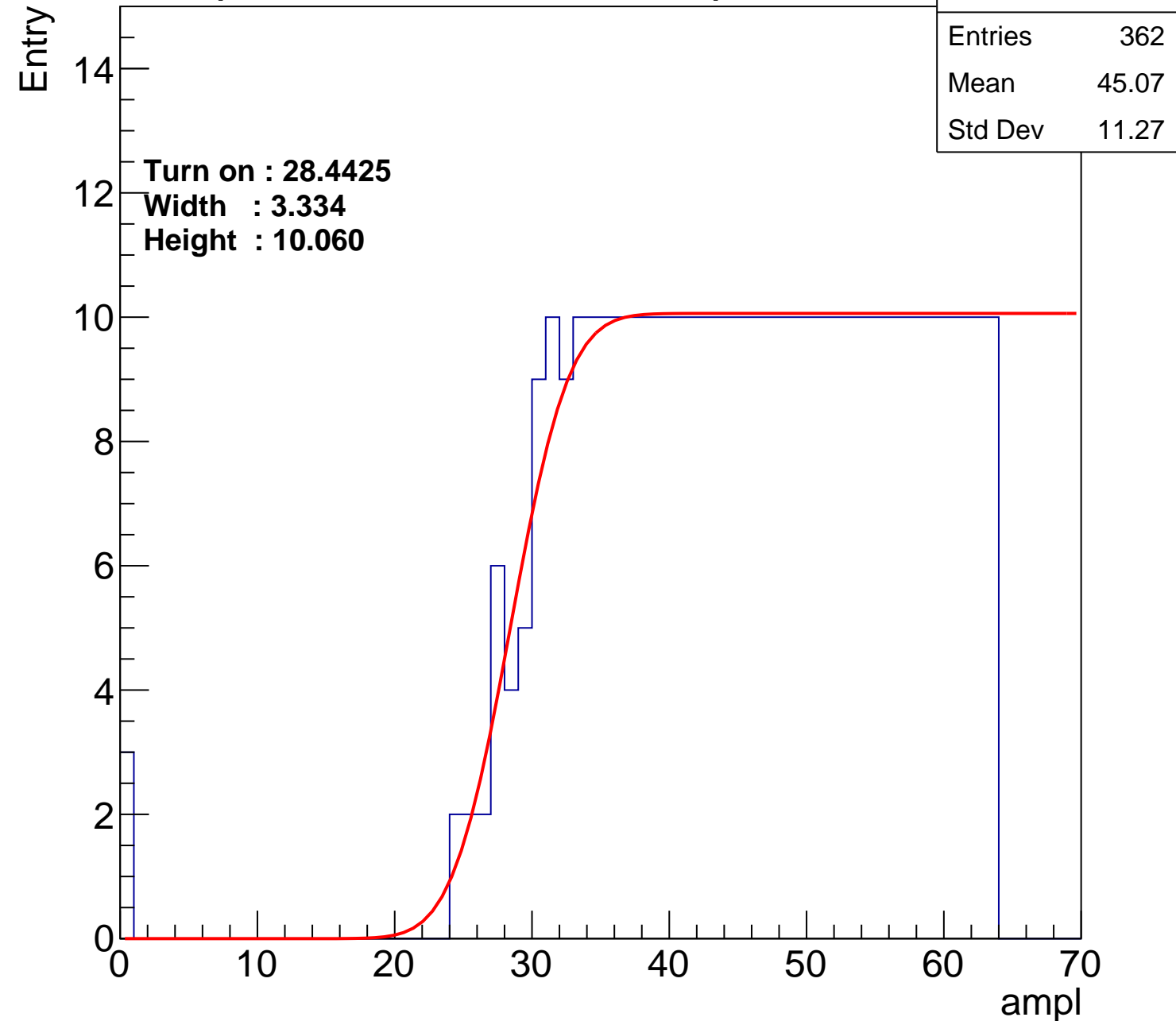
Width : 3.334

Height : 10.060

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch93

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	360
Mean	45.33
Std Dev	10.77

**Turn on : 28.3277**

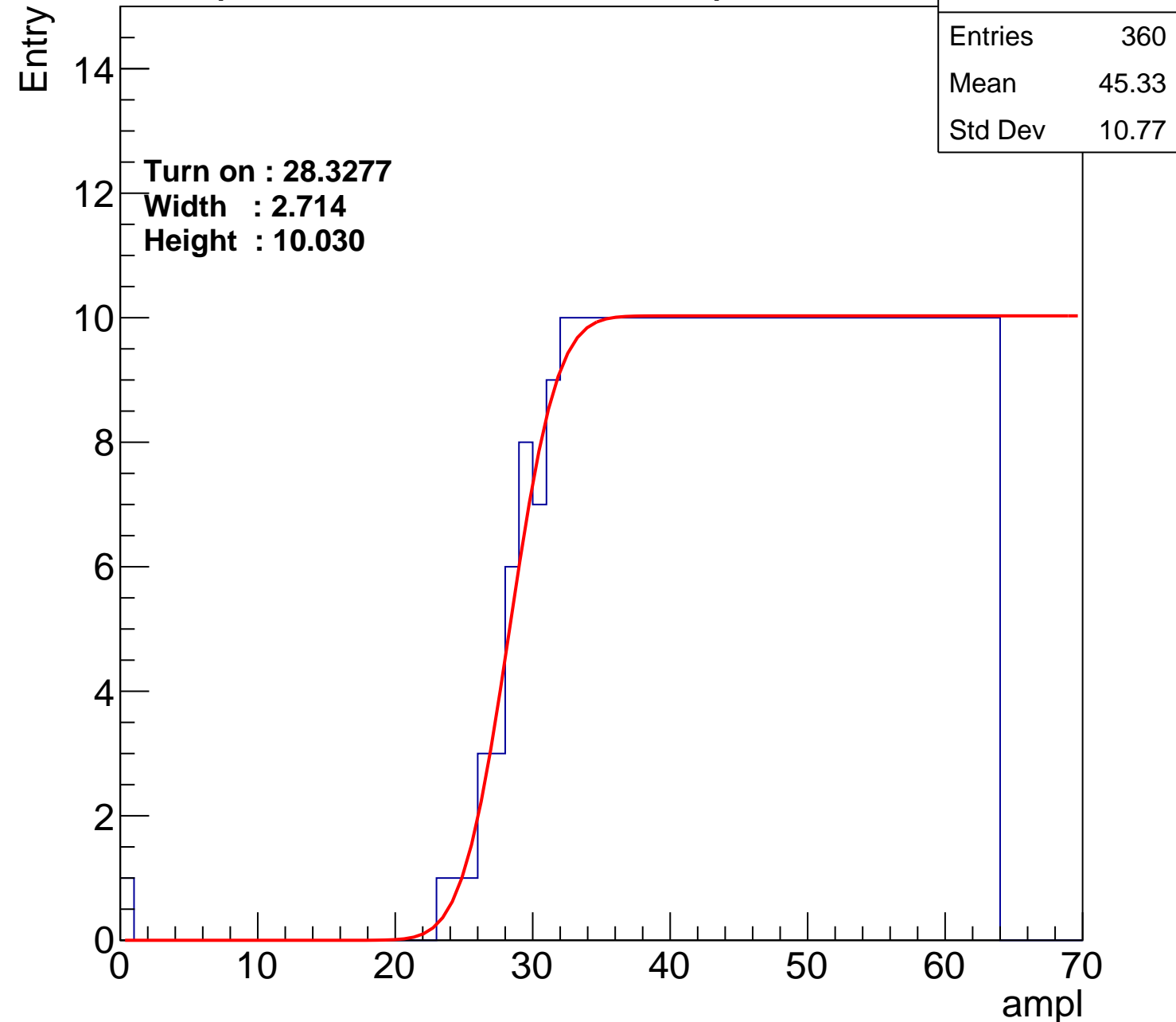
**Width : 2.714**

**Height : 10.030**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



B1L003S, U7-ch94

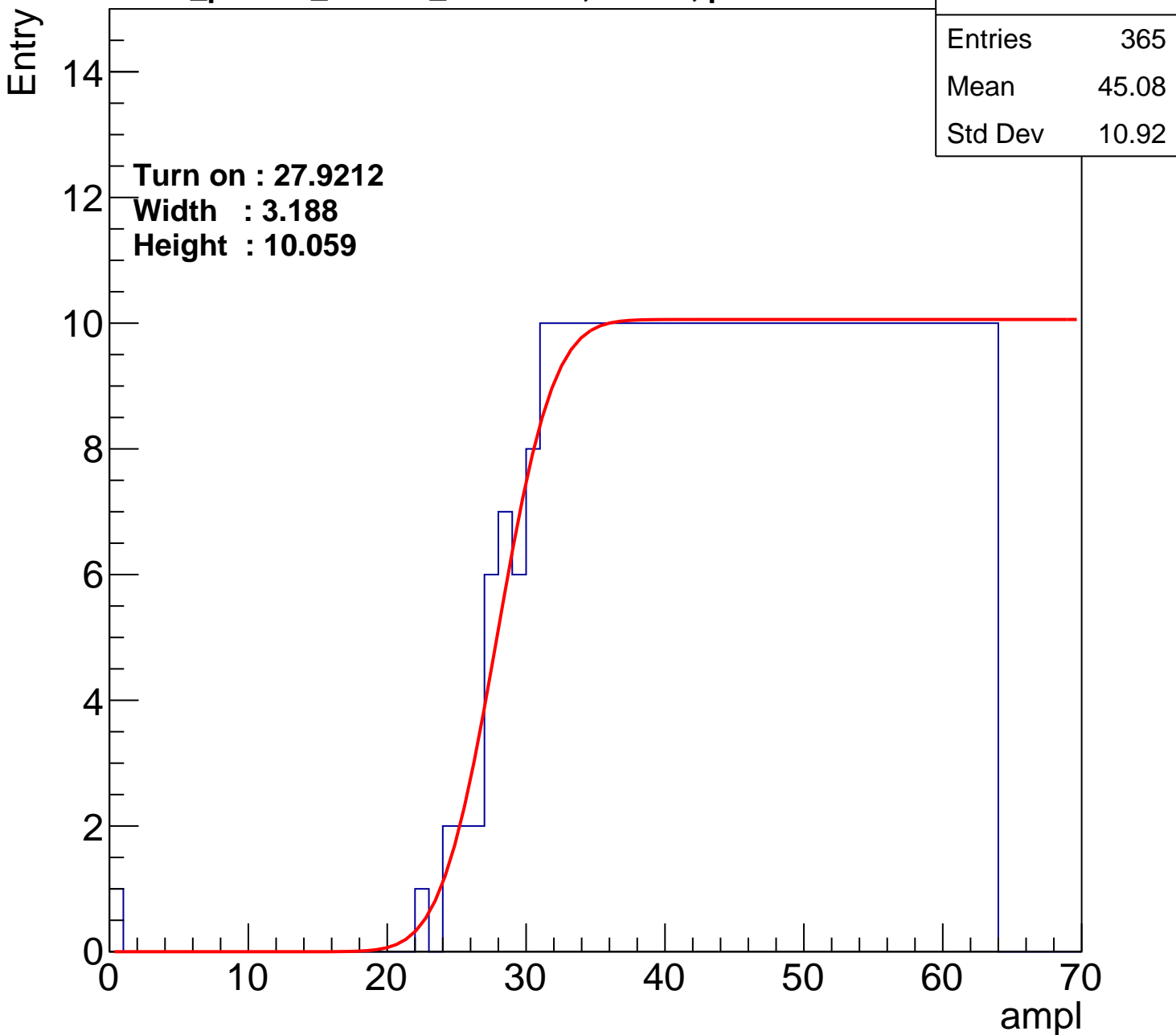
**calib\_packv5\_042523\_0143.root, FC#13, port D2**

**Turn on : 27.9212**

**Width : 3.188**

**Height : 10.059**

Entries	365
Mean	45.08
Std Dev	10.92





# B1L003S, U7-ch95

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	383
Mean	43.96
Std Dev	11.98

Turn on : 26.5269

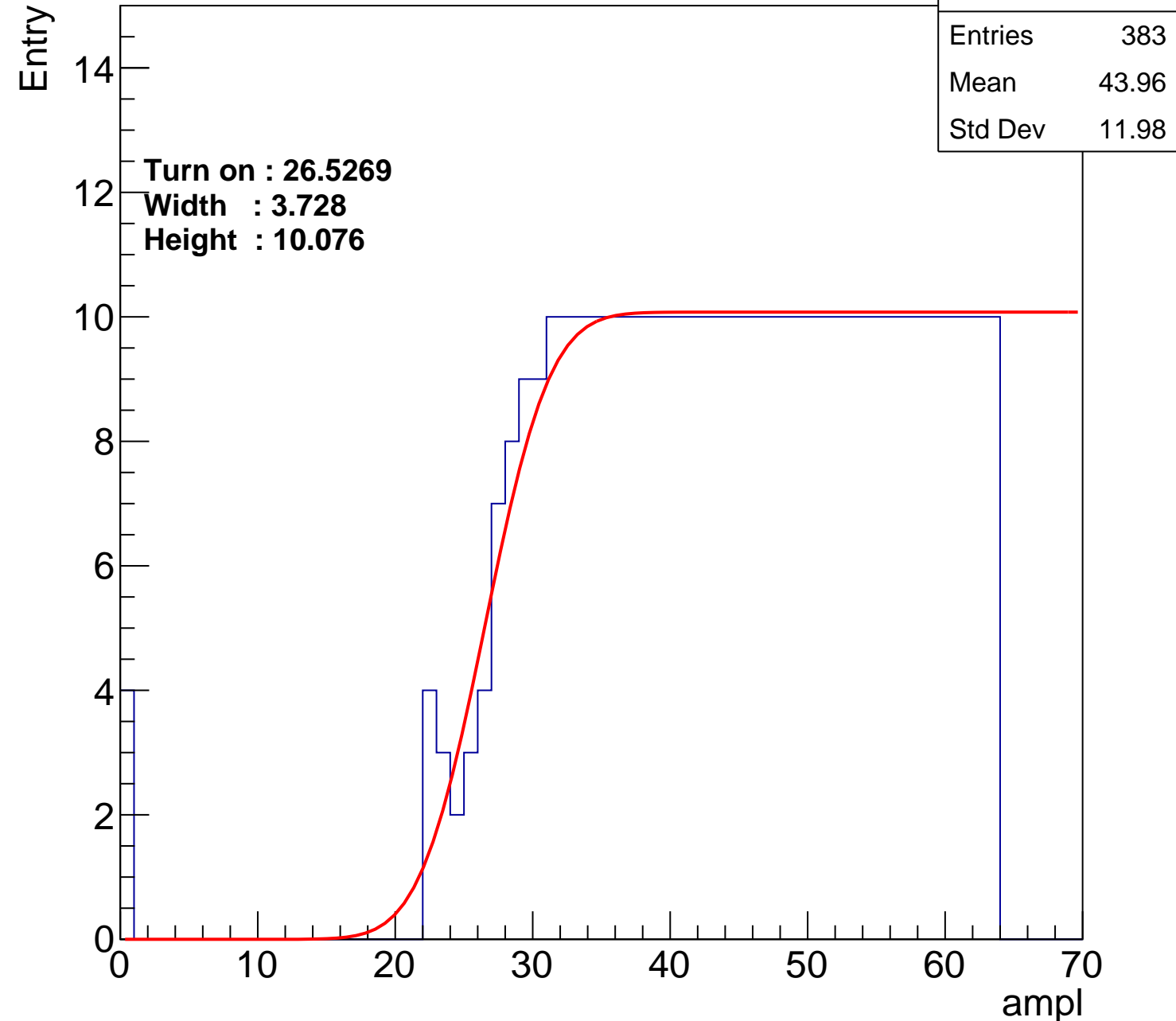
Width : 3.728

Height : 10.076

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch96

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	381
Mean	44.1
Std Dev	11.86

**Turn on : 26.0263**

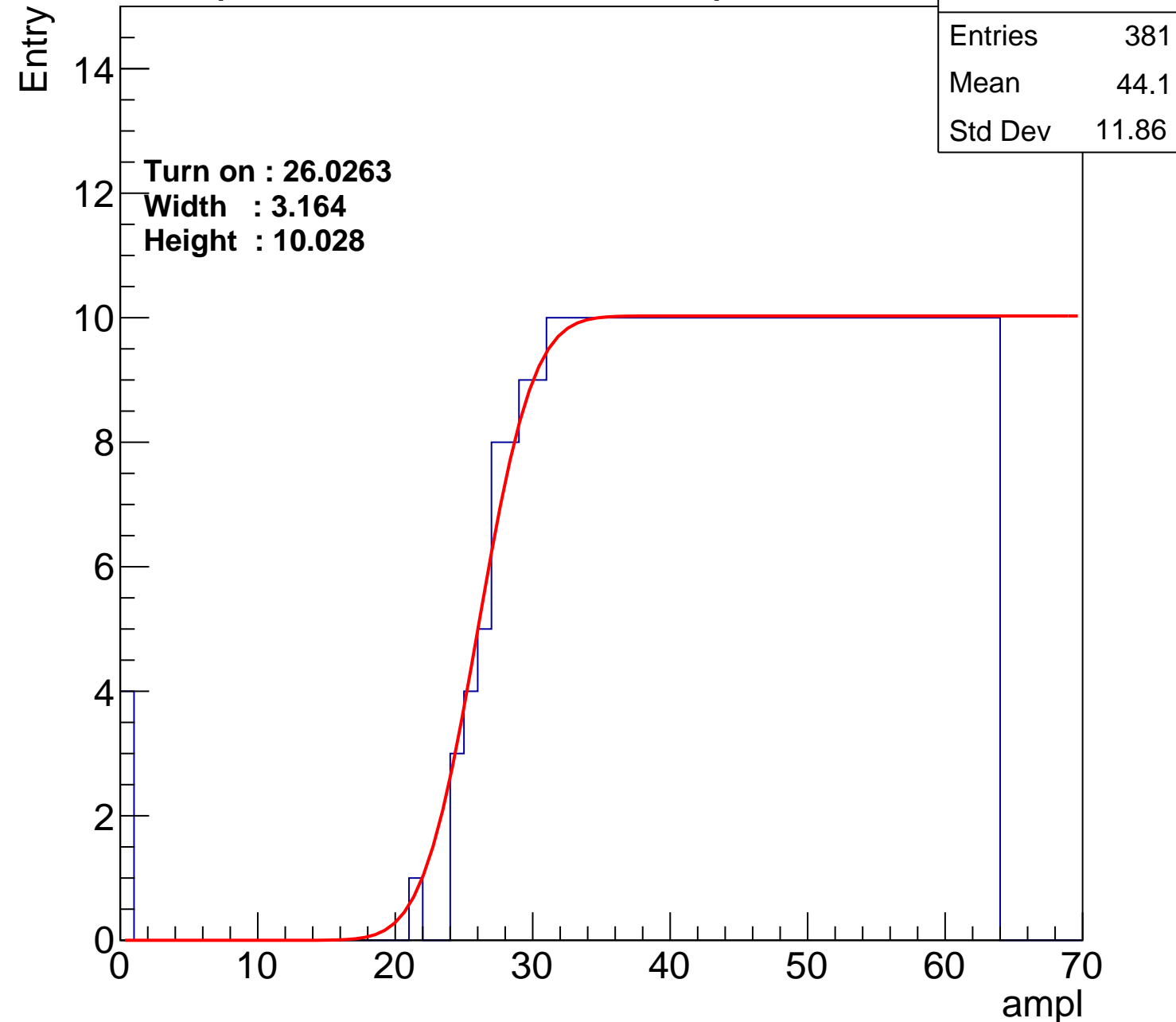
**Width : 3.164**

**Height : 10.028**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch97

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	371
Mean	44.77
Std Dev	11.09

Turn on : 27.4761

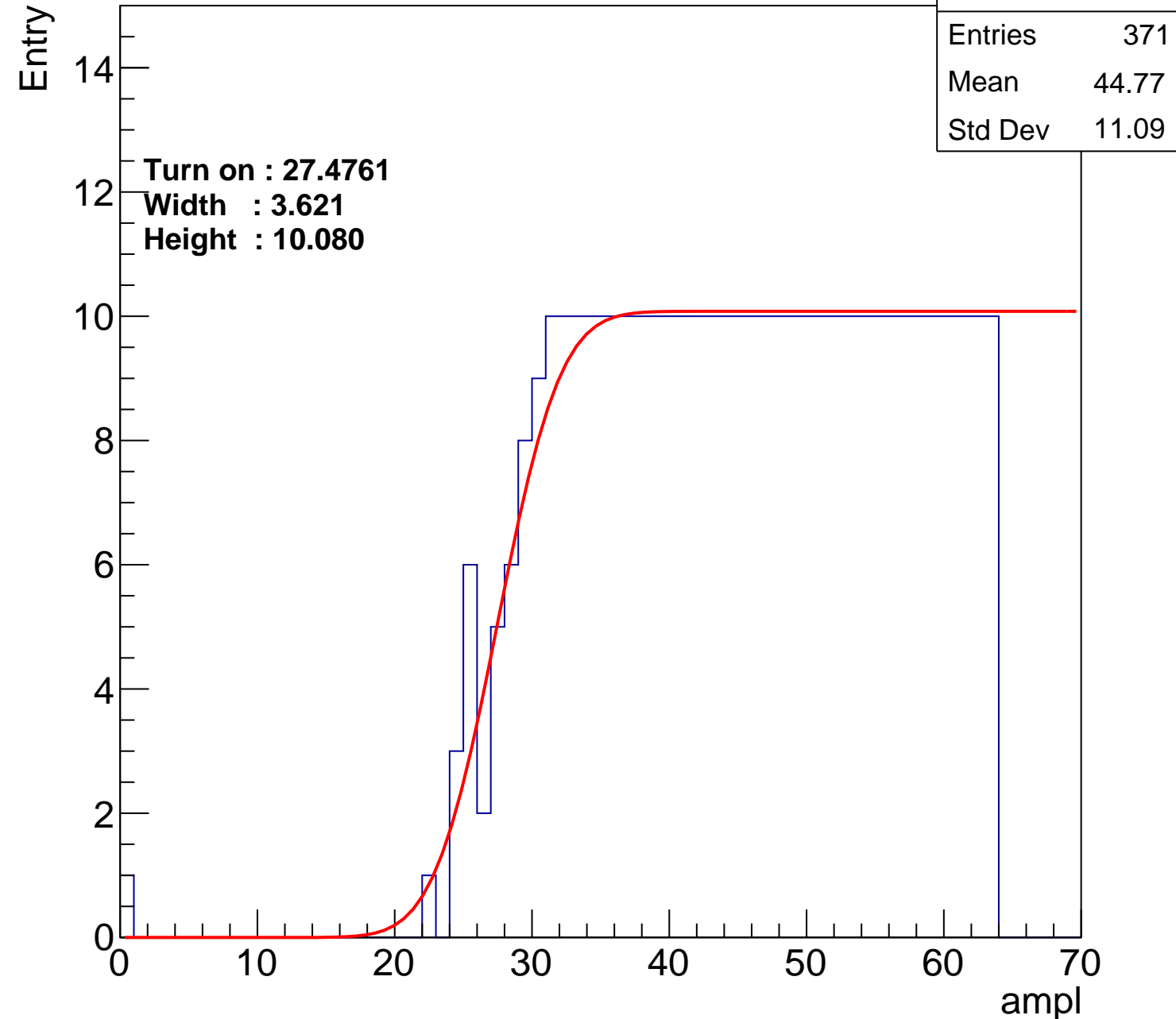
Width : 3.621

Height : 10.080

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch98

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	380
Mean	44.12
Std Dev	11.88

Turn on : 26.5559

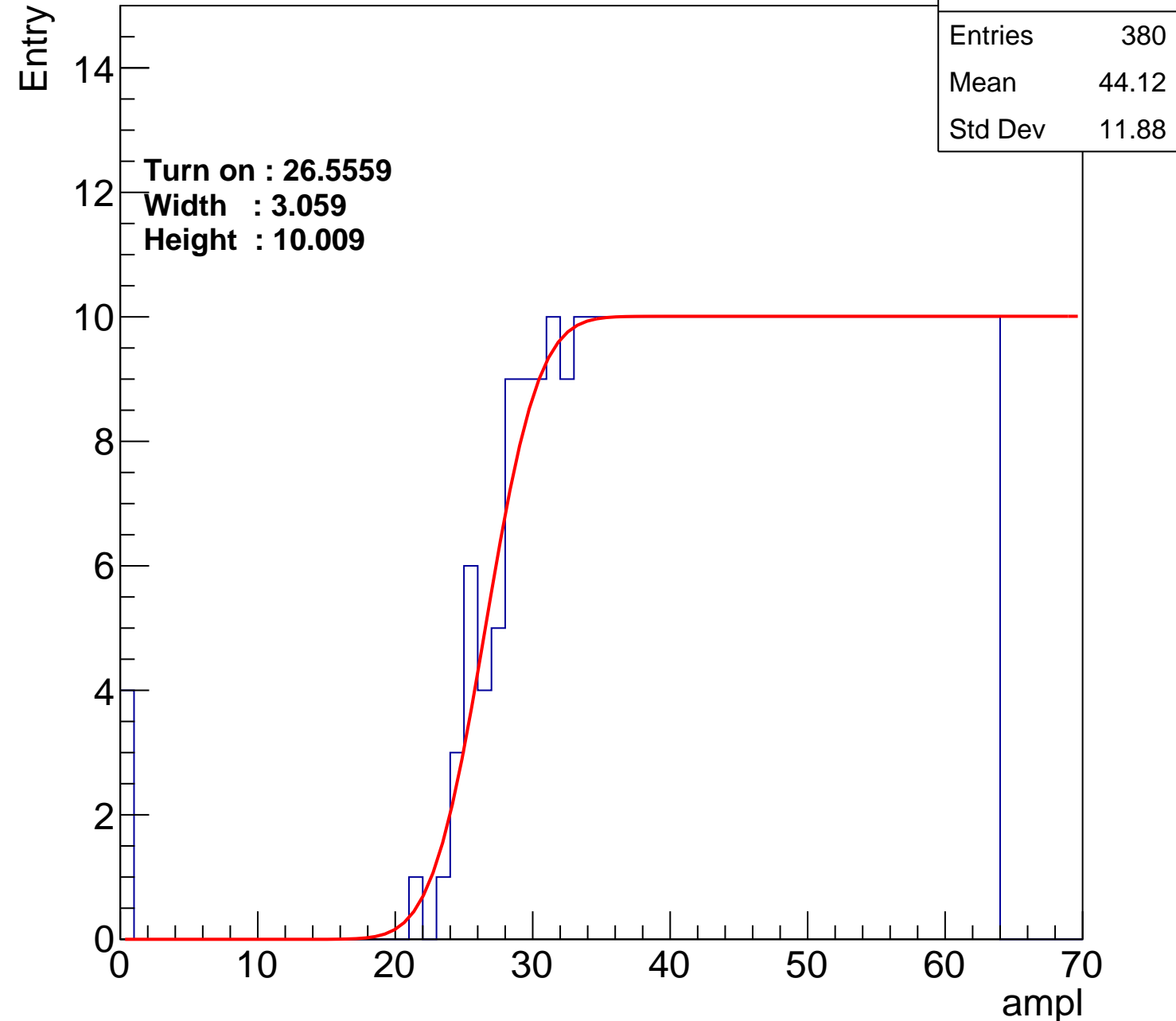
Width : 3.059

Height : 10.009

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch99

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	372
Mean	44.53
Std Dev	11.58

Turn on : 27.4817

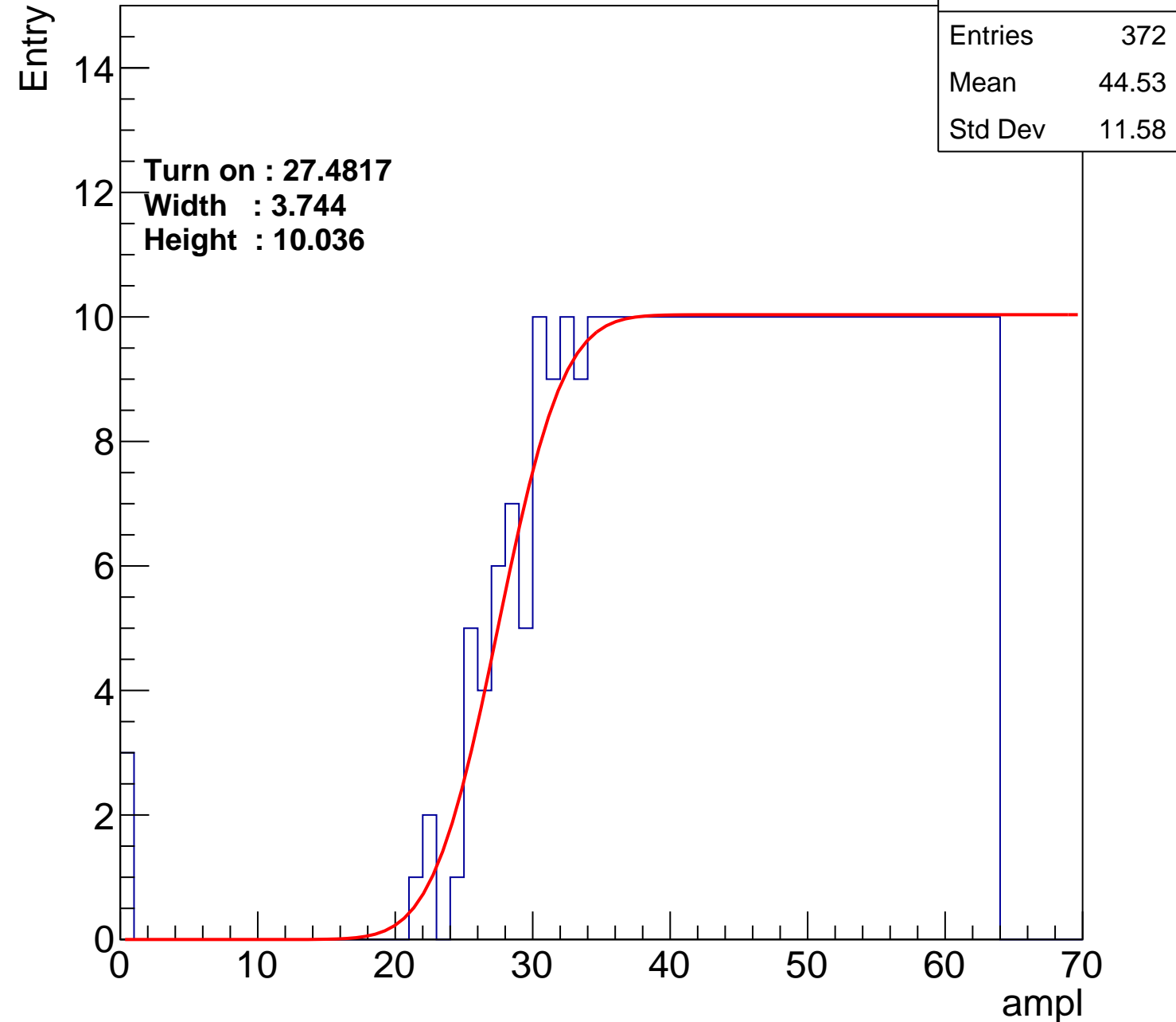
Width : 3.744

Height : 10.036

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch100

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	369
Mean	44.82
Std Dev	11.21

Turn on : 27.3677

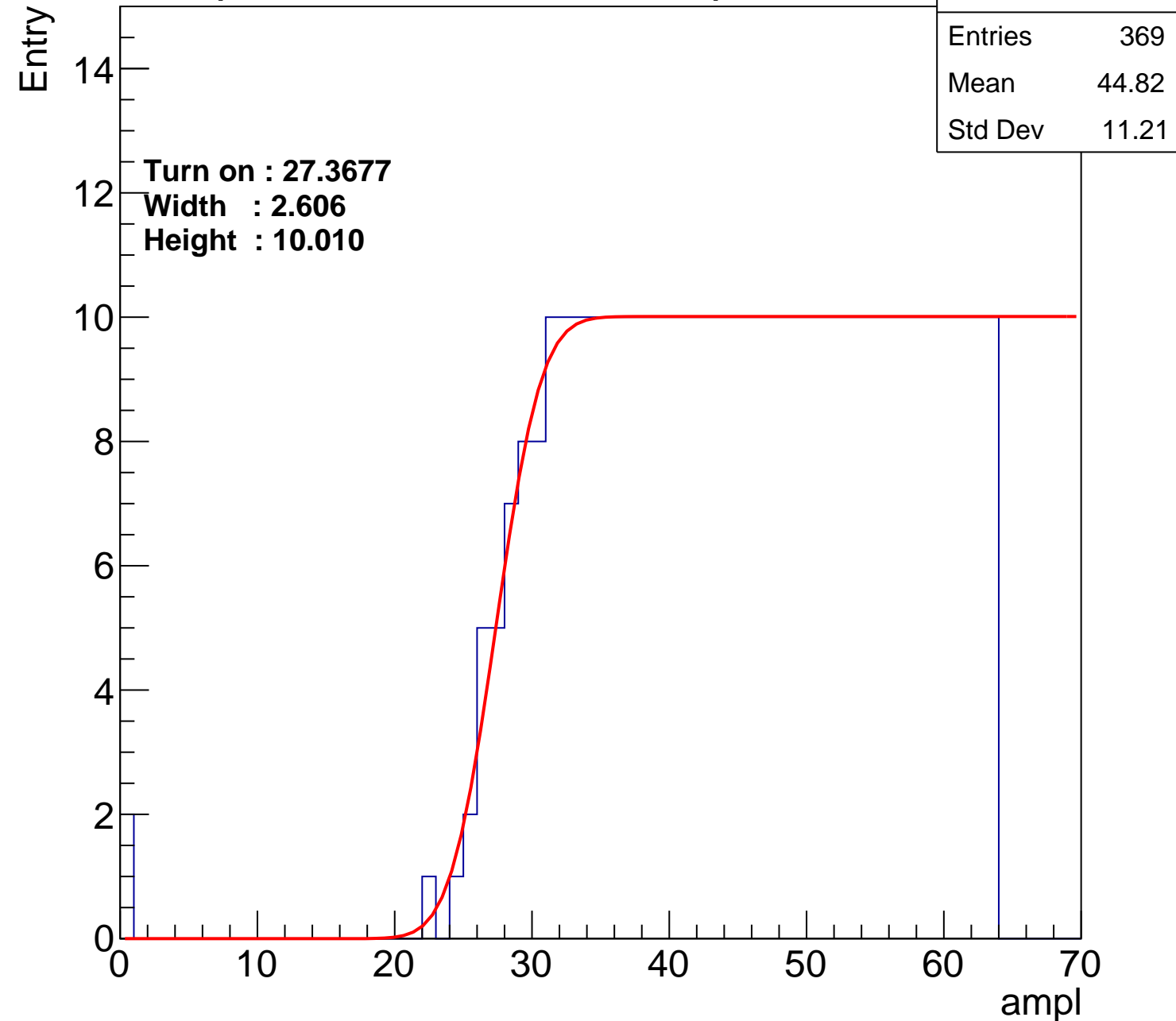
Width : 2.606

Height : 10.010

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch101

calib\_packv5\_042523\_0143.root, FC#13, port D2

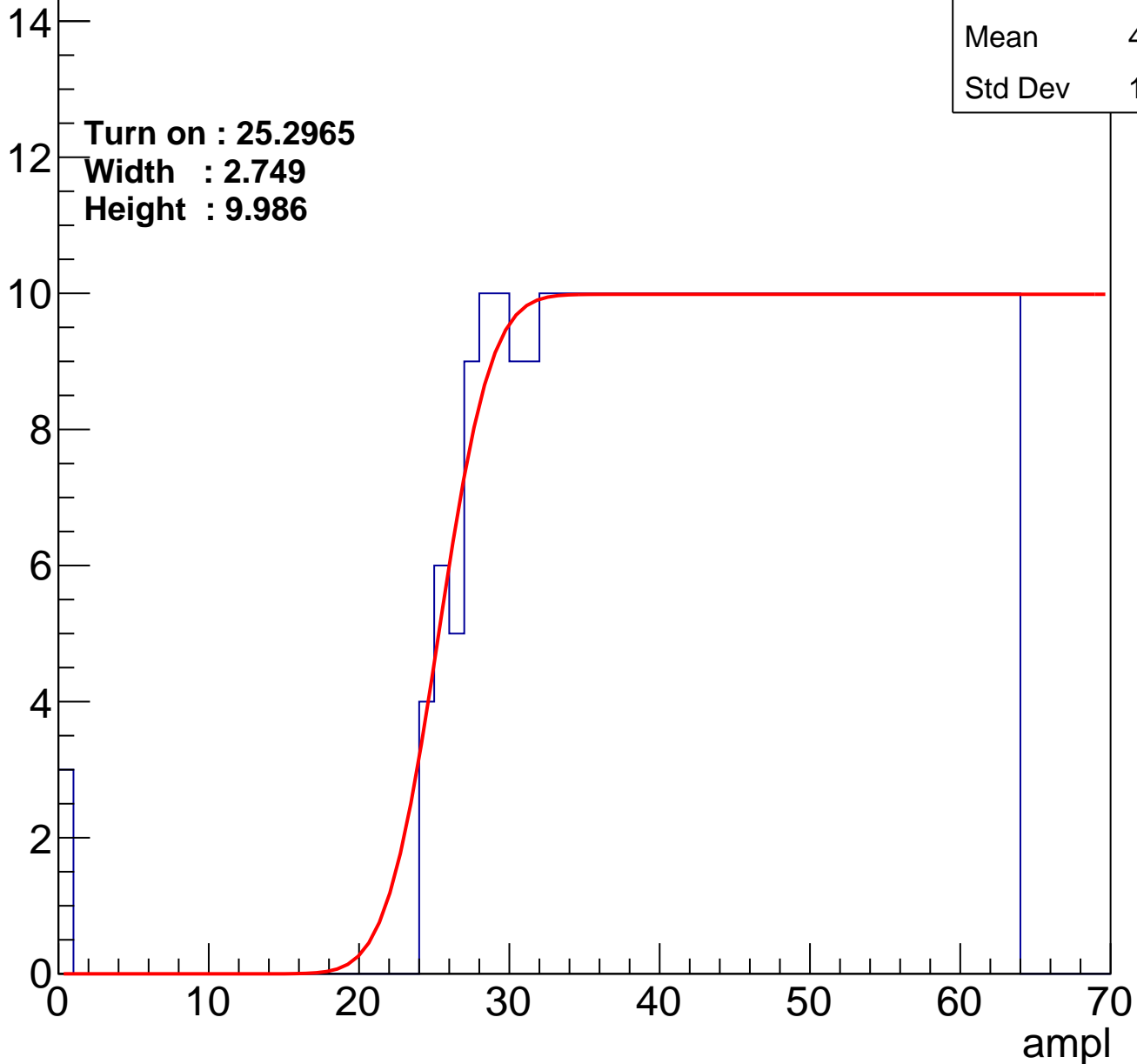
Entries	385
Mean	43.99
Std Dev	11.74

Turn on : 25.2965

Width : 2.749

Height : 9.986

Entry



# B1L003S, U7-ch102

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	364
Mean	45.08
Std Dev	11.06

Turn on : 27.8376

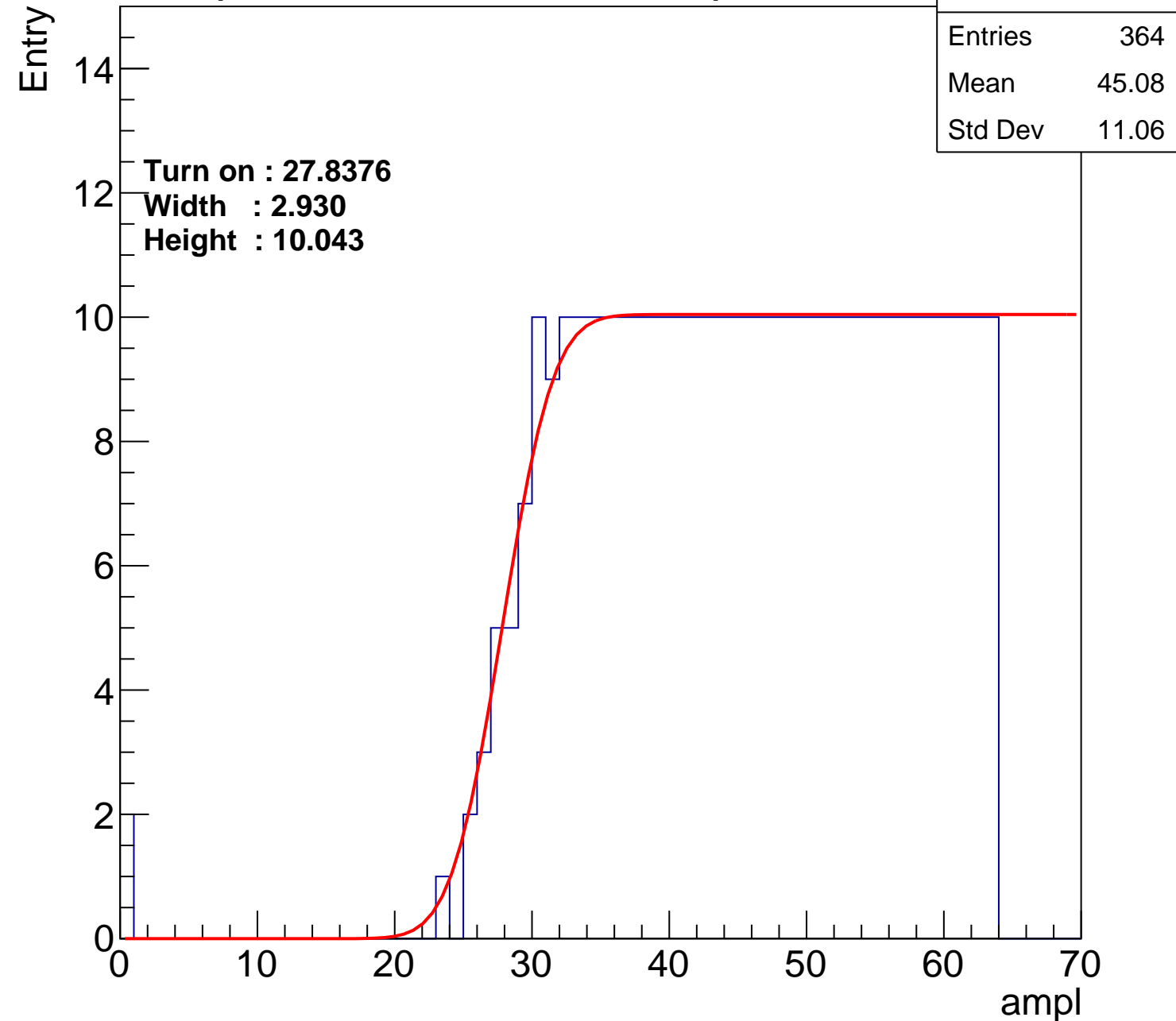
Width : 2.930

Height : 10.043

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L003S, U7-ch103

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	360
Mean	45.34
Std Dev	10.76

Turn on : 28.0912

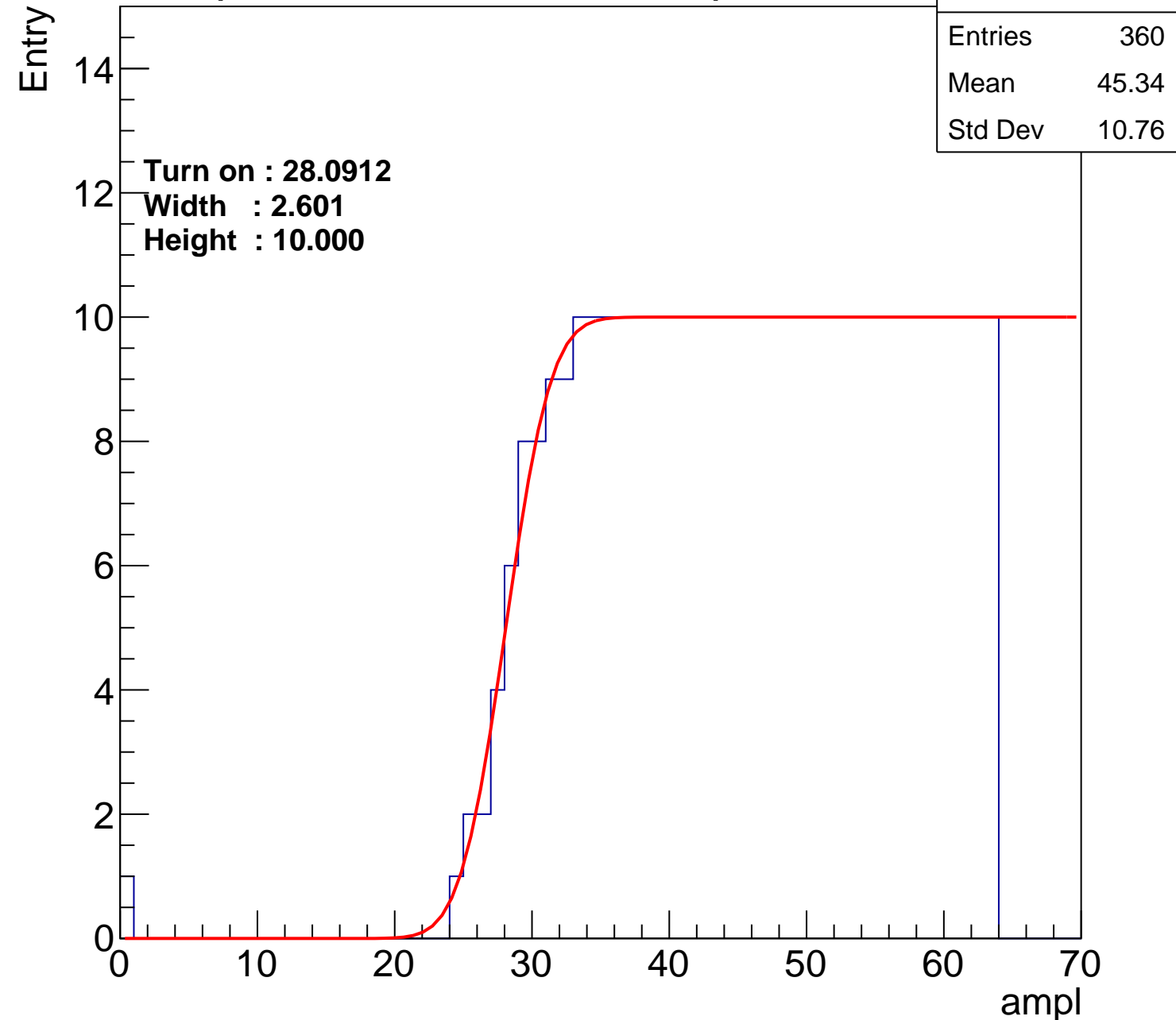
Width : 2.601

Height : 10.000

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch104

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	372
Mean	44.71
Std Dev	11.14

Turn on : 27.0247

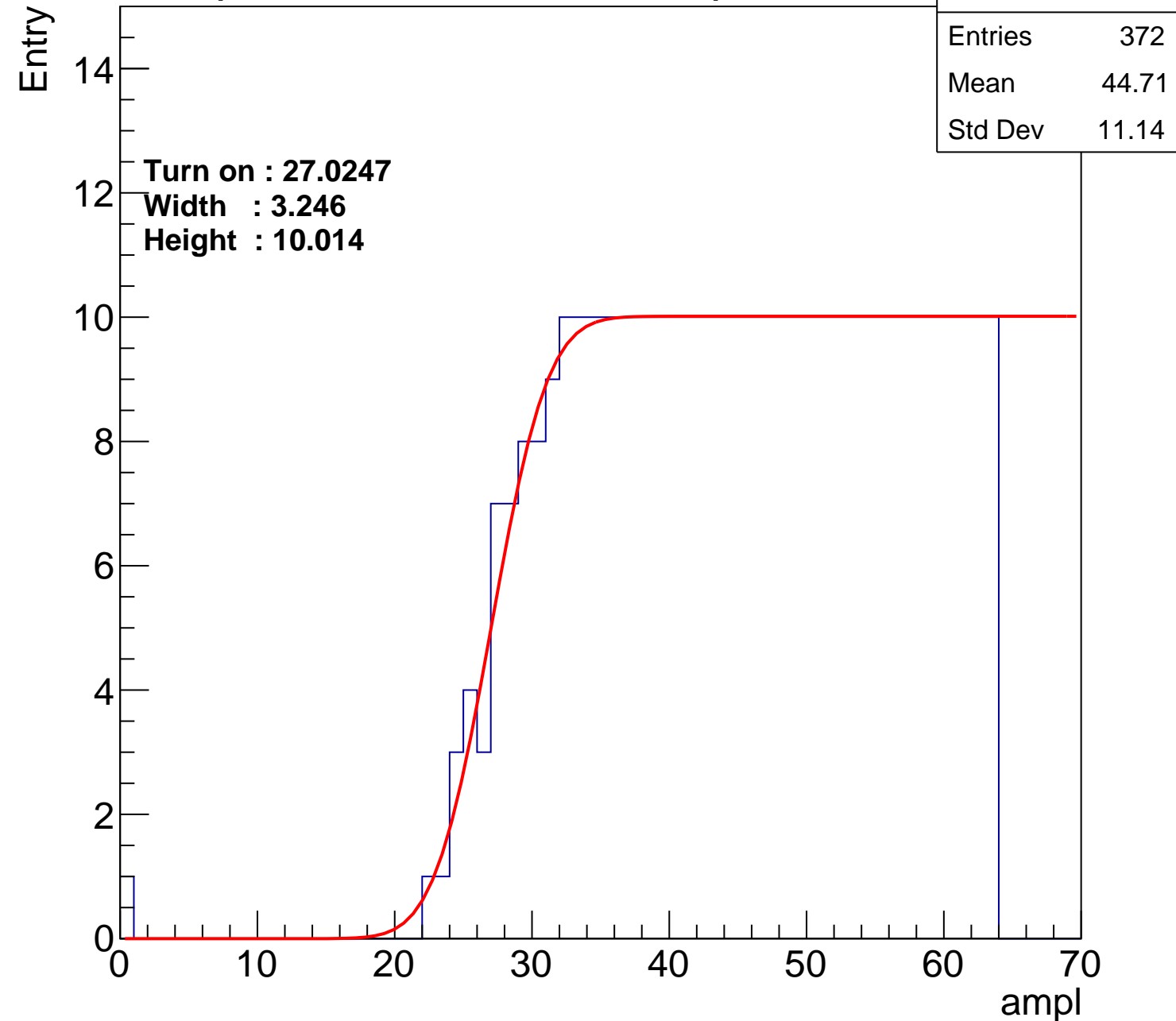
Width : 3.246

Height : 10.014

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch105

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	354
Mean	45.53
Std Dev	10.88

**Turn on : 28.9886**

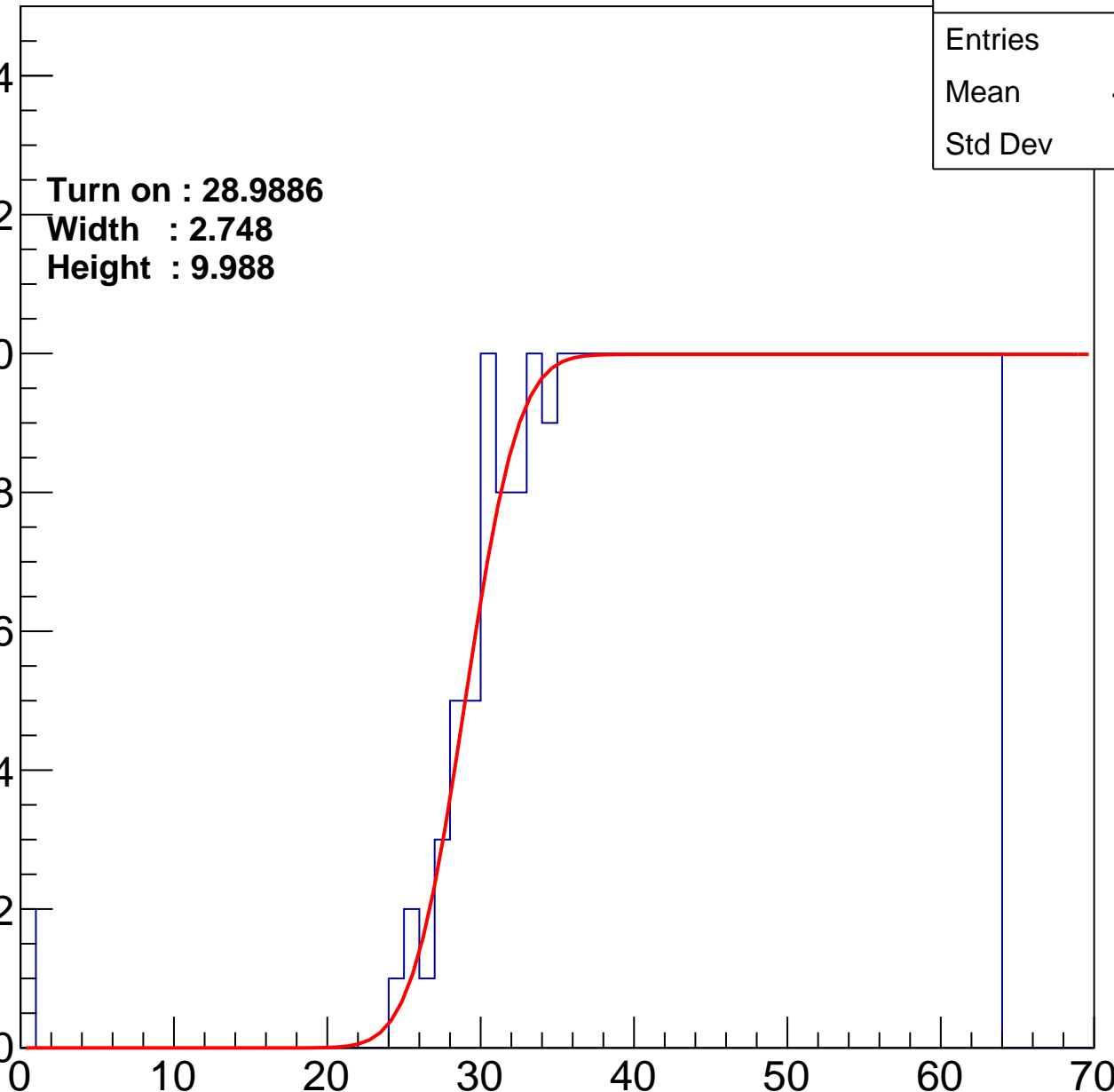
**Width : 2.748**

**Height : 9.988**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch106

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	363
Mean	44.99
Std Dev	11.35

Turn on : 28.2713

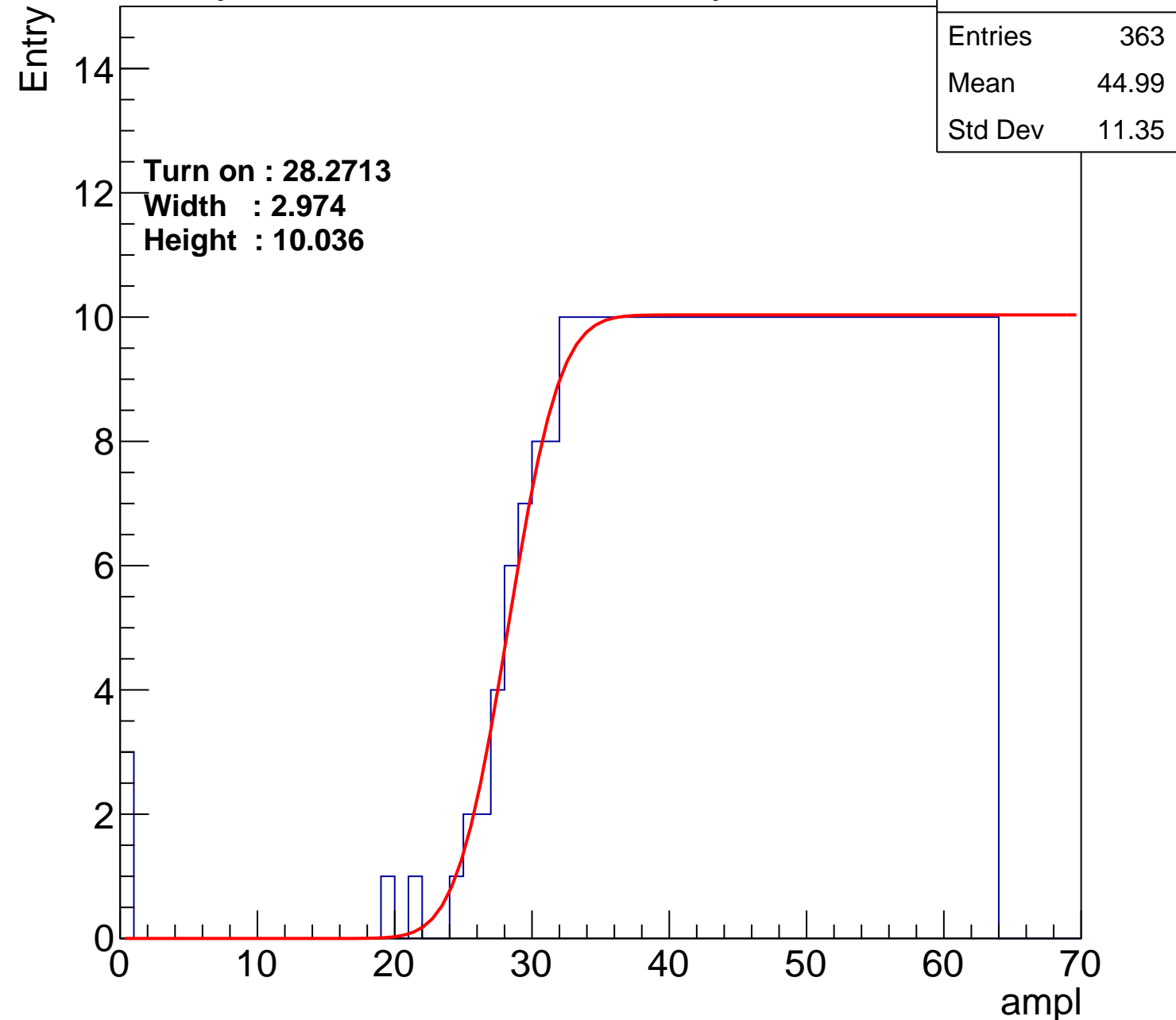
Width : 2.974

Height : 10.036

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch107

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	383
Mean	44.09
Std Dev	11.63

Turn on : 26.4243

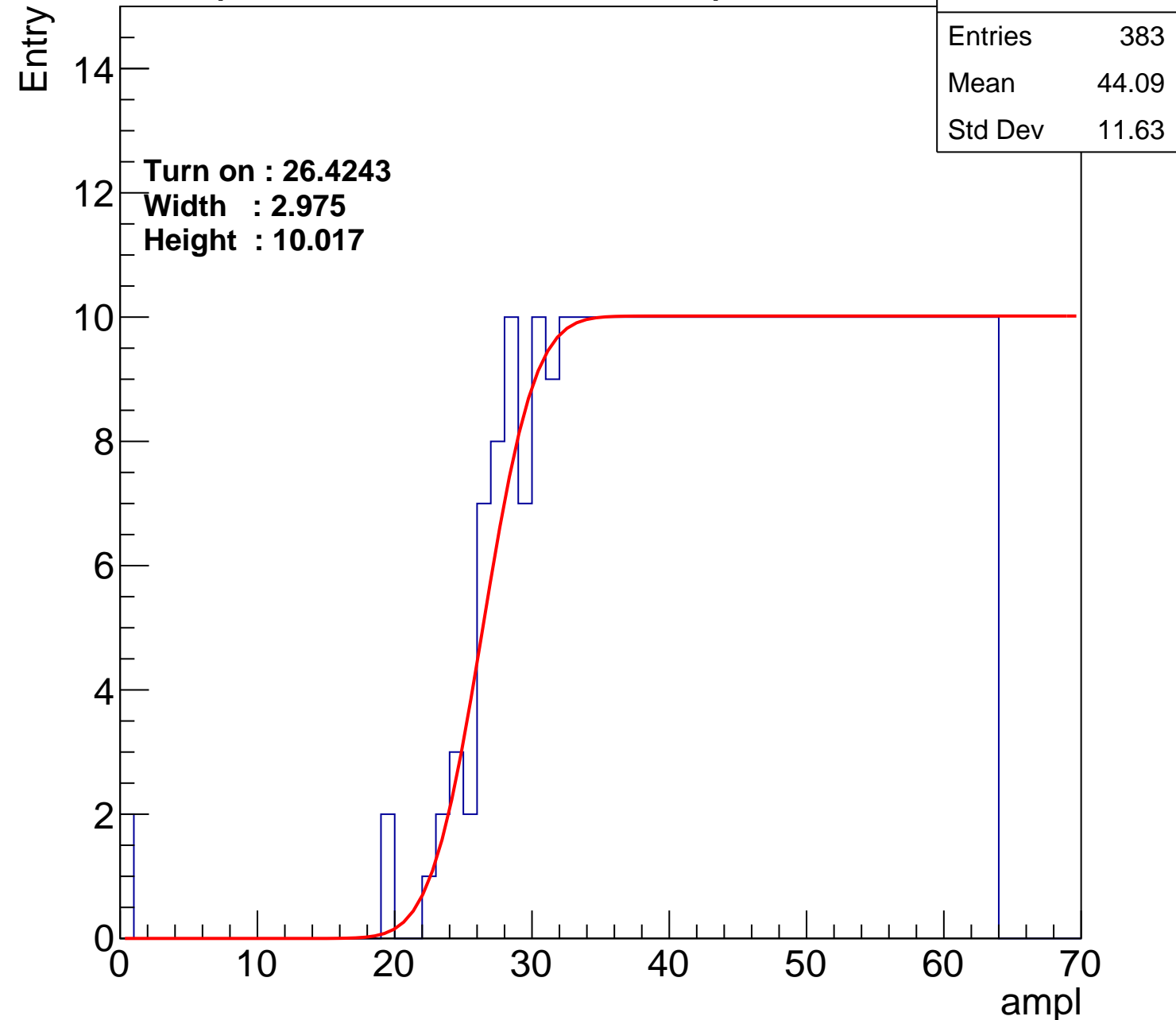
Width : 2.975

Height : 10.017

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch108

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	359
Mean	45.24
Std Dev	11.17

Turn on : 24.7737

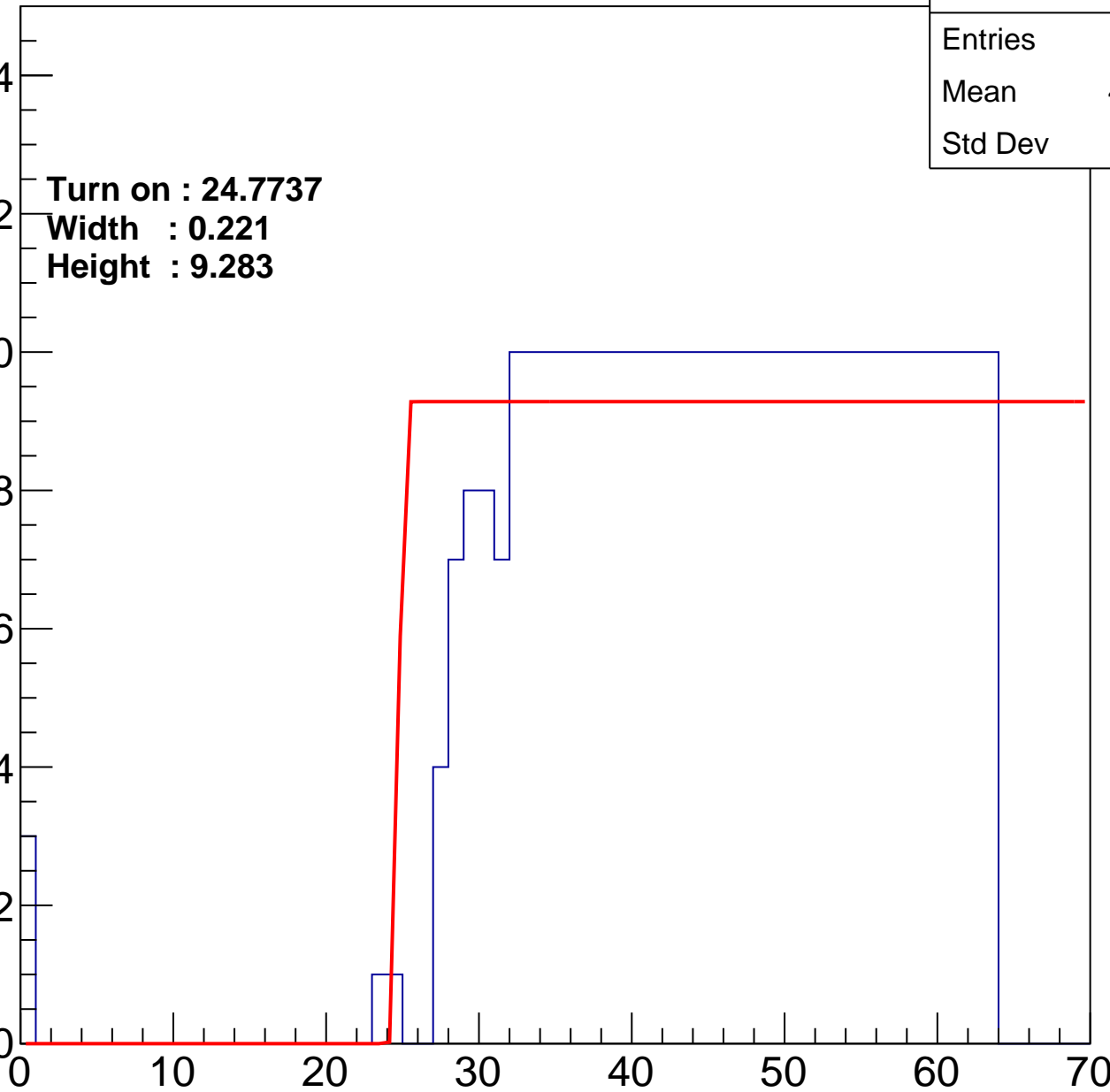
Width : 0.221

Height : 9.283

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch109

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	383
Mean	43.83
Std Dev	12.32

Turn on : 26.4592

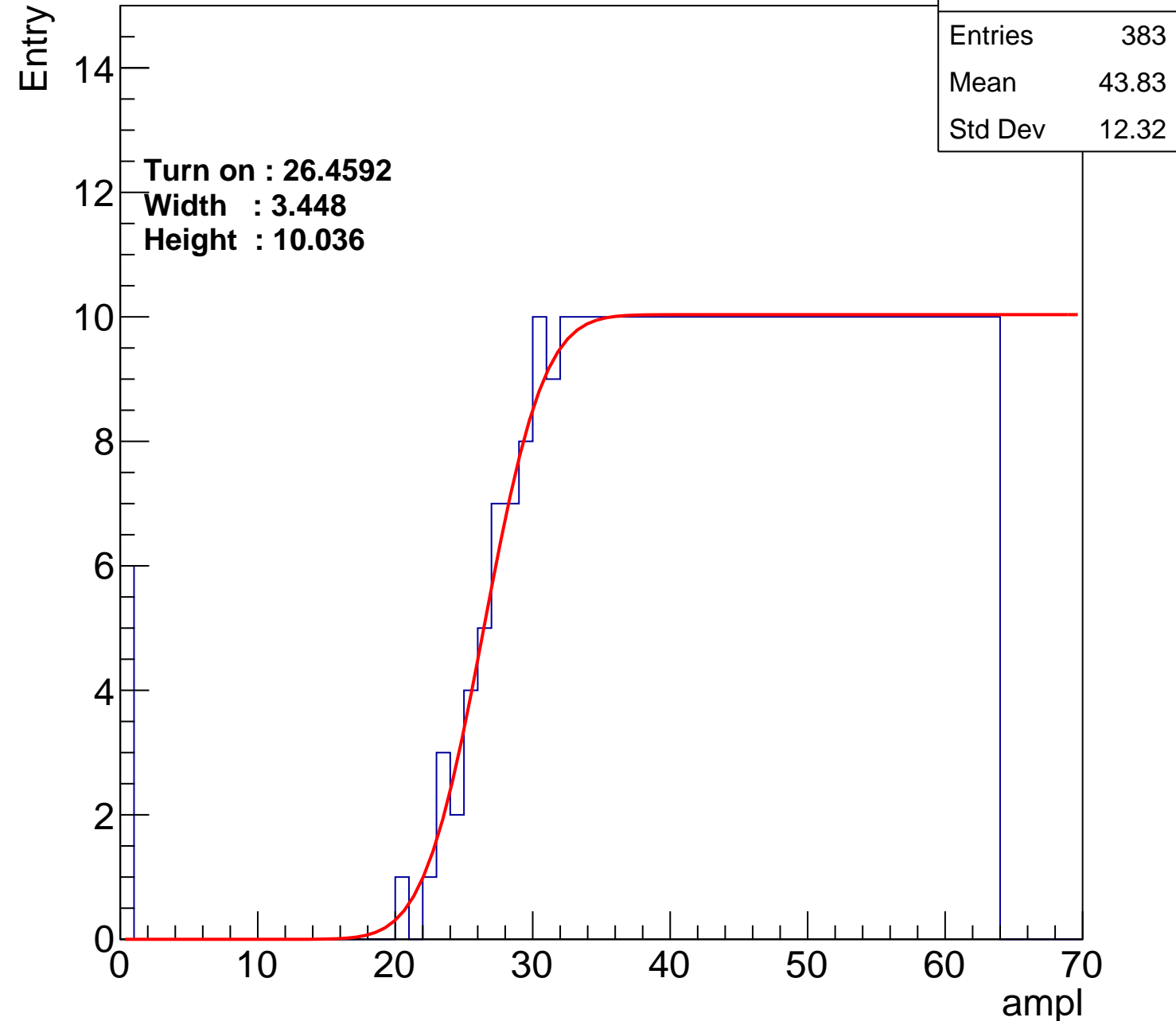
Width : 3.448

Height : 10.036

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch110

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	383
Mean	43.92
Std Dev	12.11

Turn on : 25.9251

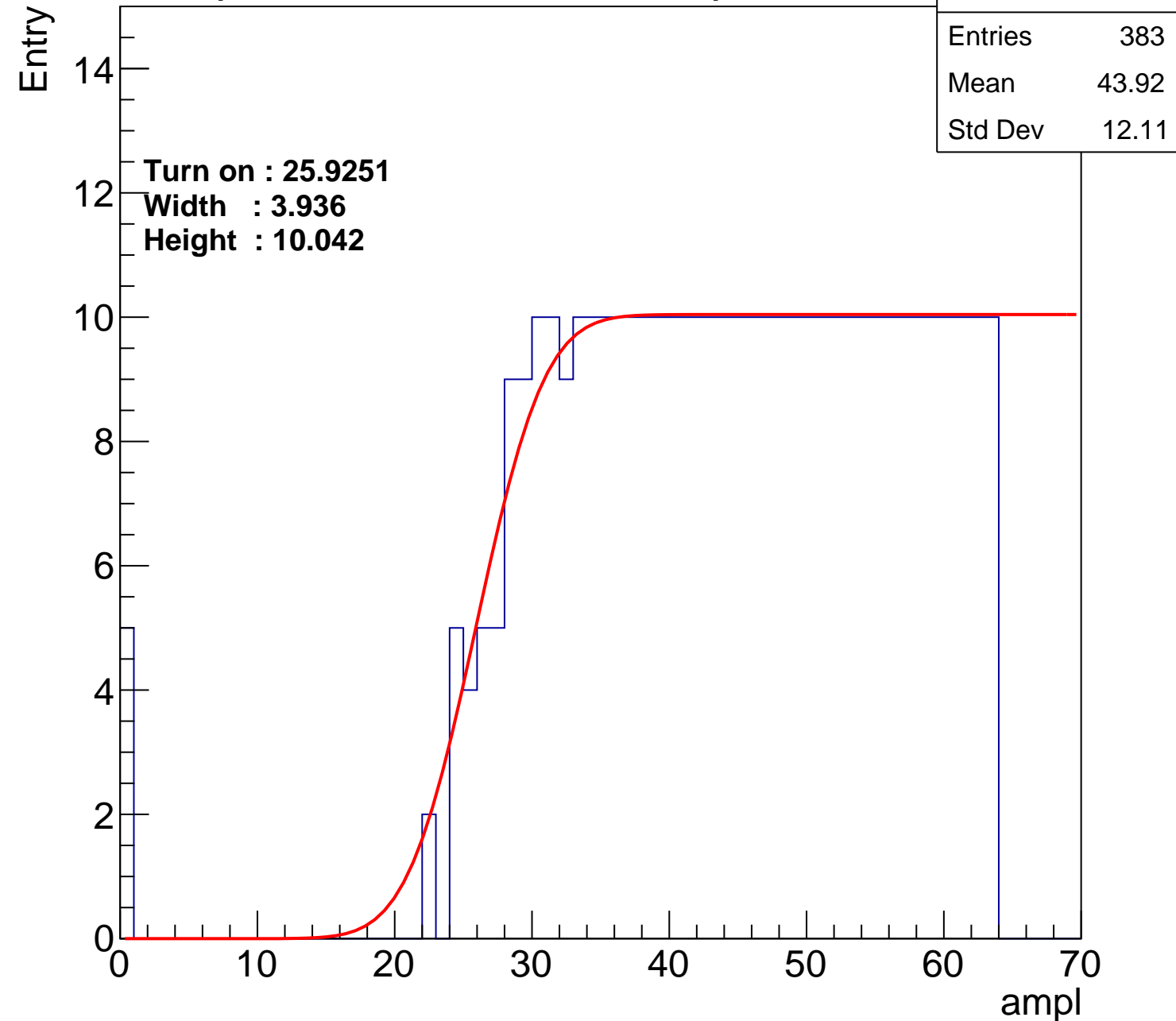
Width : 3.936

Height : 10.042

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L003S, U7-ch111

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	374
Mean	44.61
Std Dev	11.19

Turn on : 27.1716

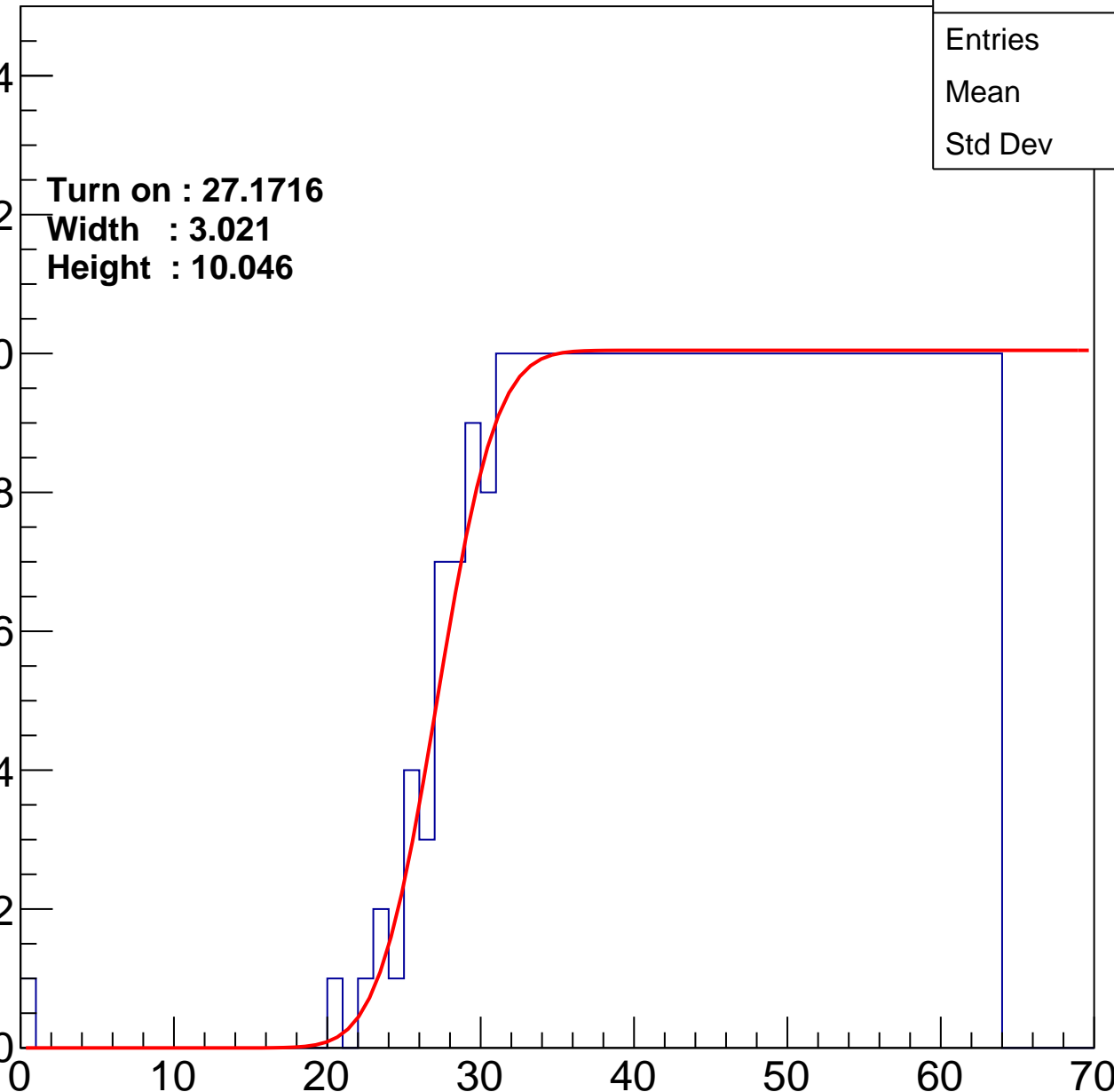
Width : 3.021

Height : 10.046

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch112

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	379
Mean	44.1
Std Dev	11.96

Turn on : 26.3982

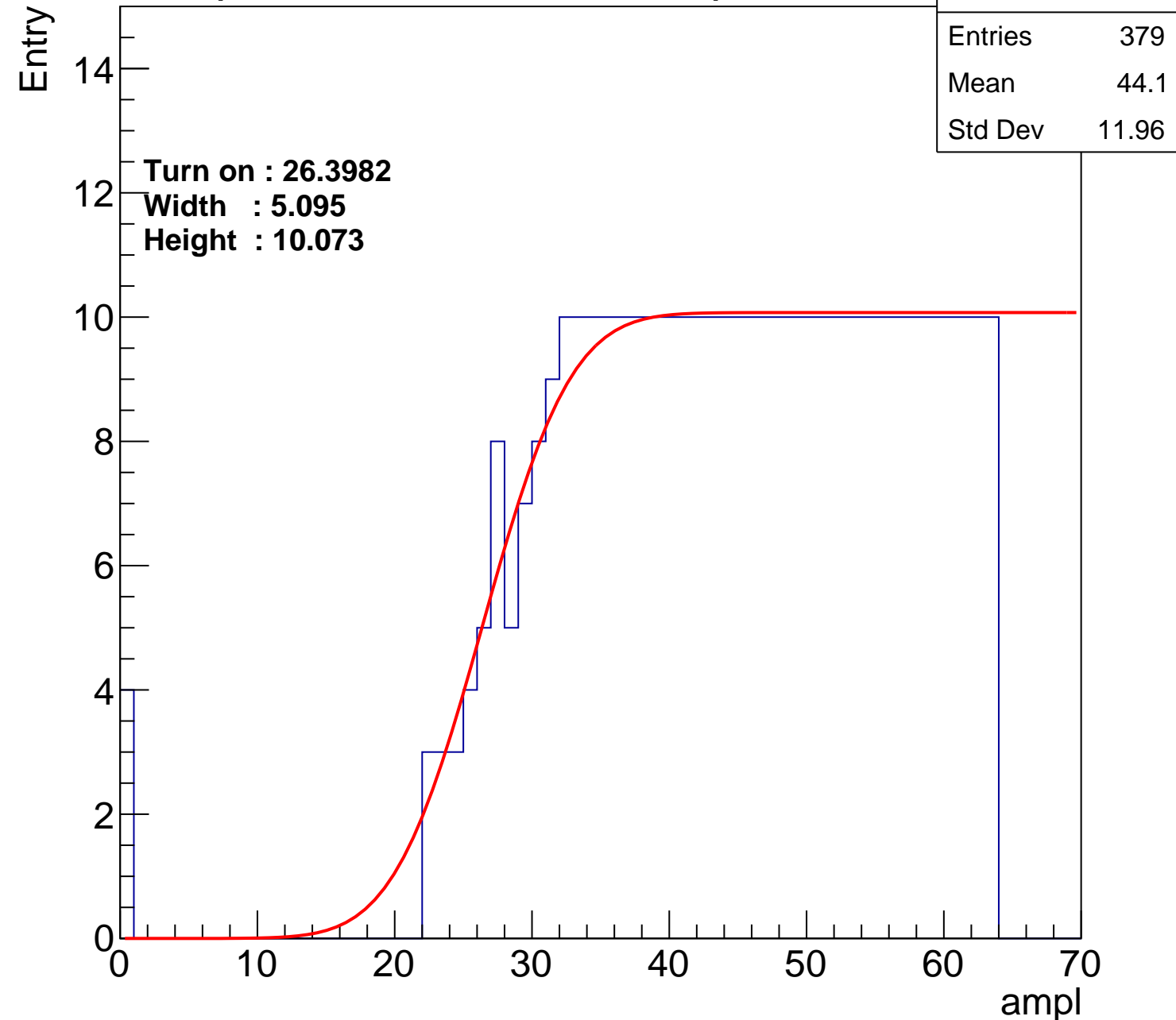
Width : 5.095

Height : 10.073

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch113

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	359
Mean	44.96
Std Dev	11.87

**Turn on : 29.9834**

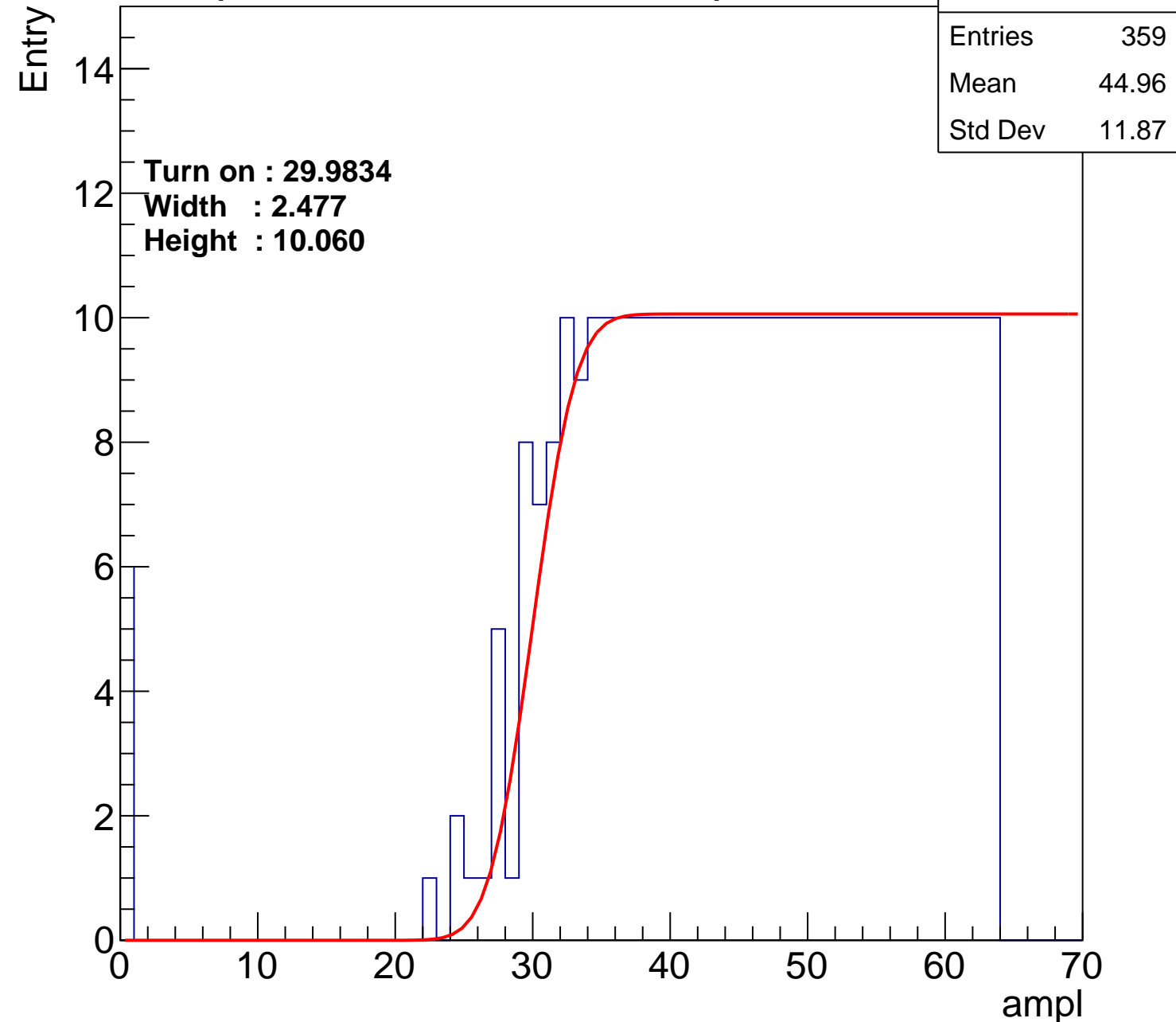
**Width : 2.477**

**Height : 10.060**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



B1L003S, U7-ch114

**calib\_packv5\_042523\_0143.root, FC#13, port D2**

Entries	362
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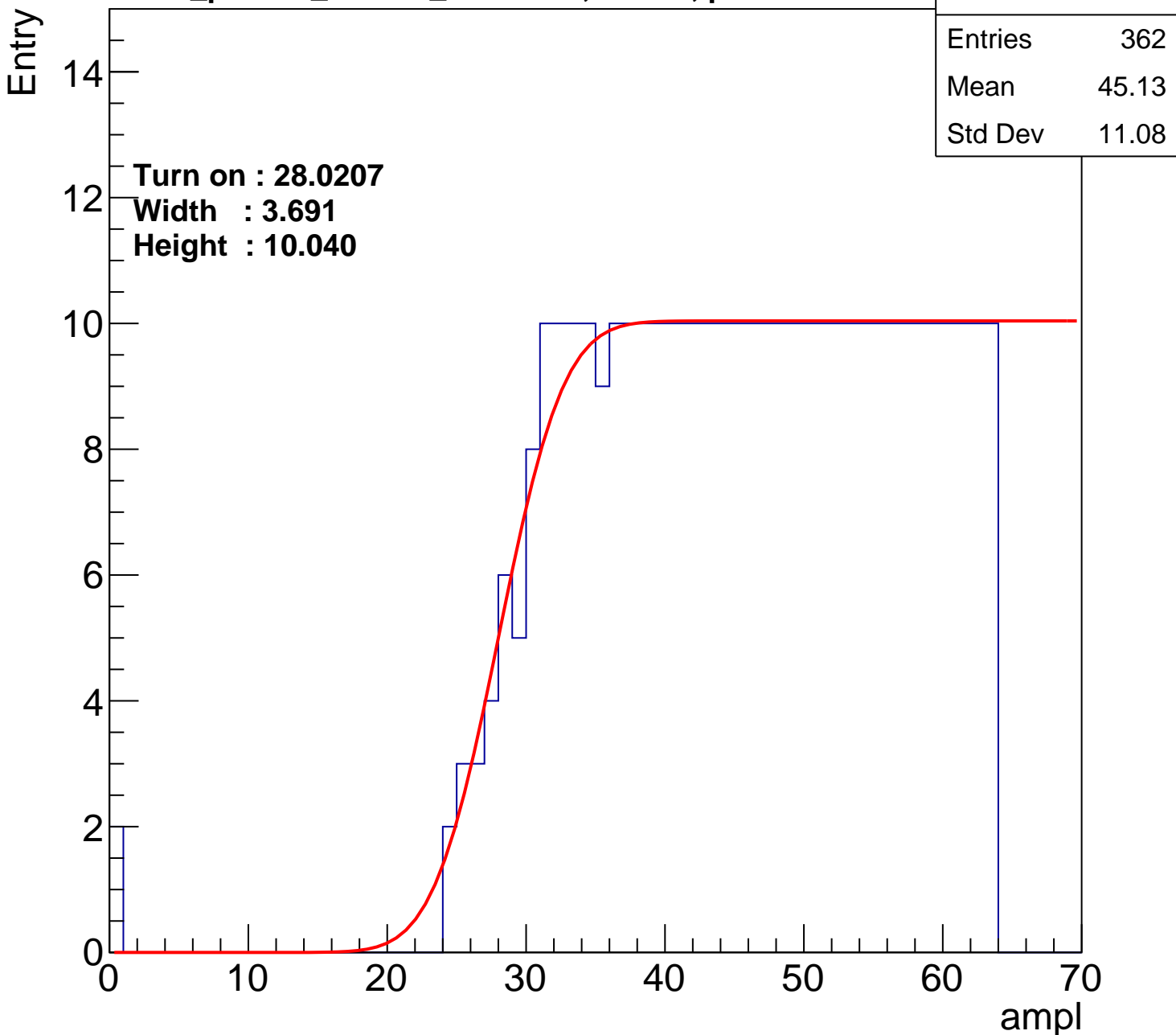
Mean	45.13
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Std Dev	11.08
---------	-------

**Turn on : 28.0207**

**Width : 3.691**

**Height : 10.040**



# B1L003S, U7-ch115

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	354
Mean	45.62
Std Dev	10.63

Turn on : 28.6495

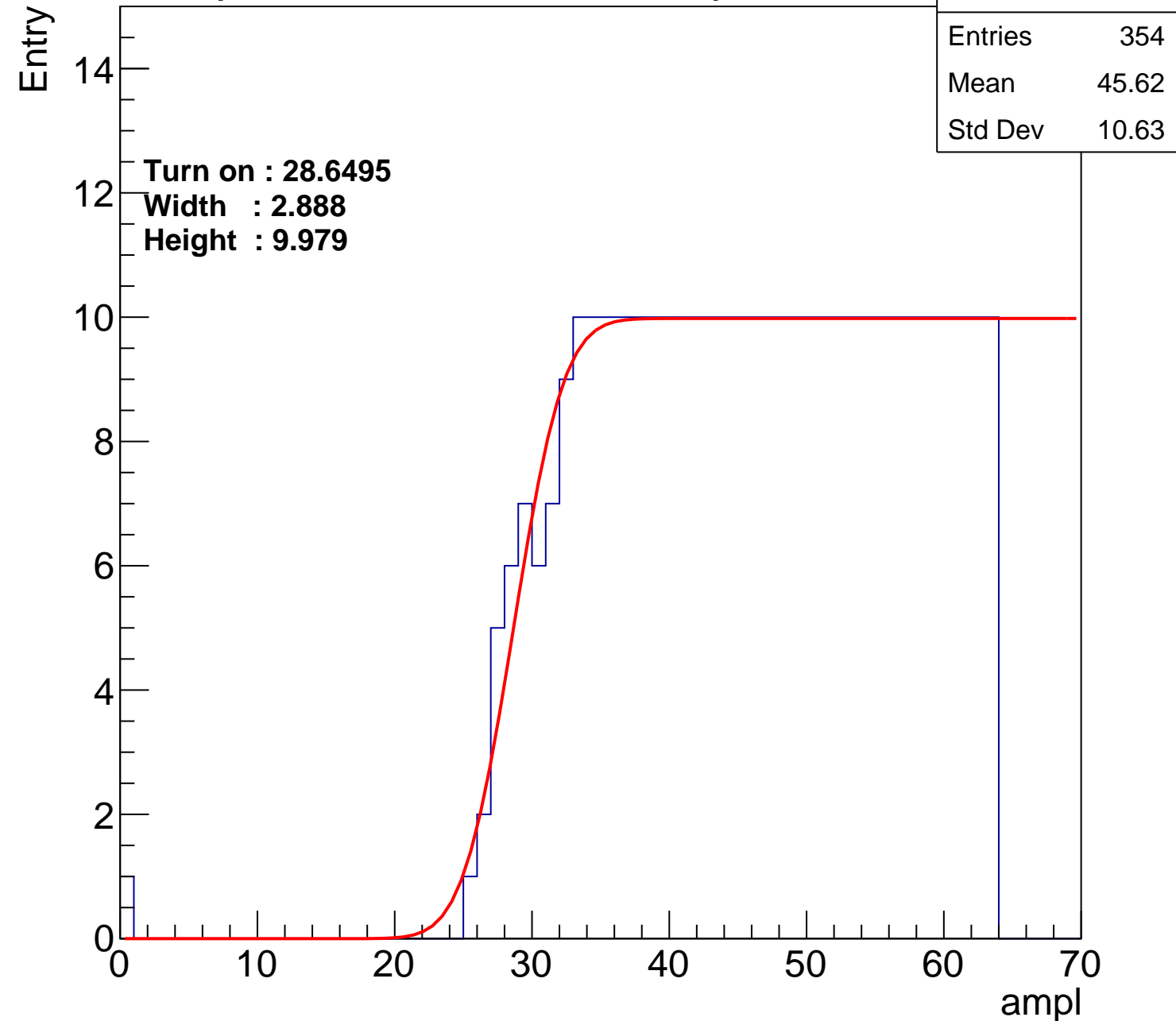
Width : 2.888

Height : 9.979

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch116

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	365
Mean	44.95
Std Dev	11.31

Turn on : 27.8666

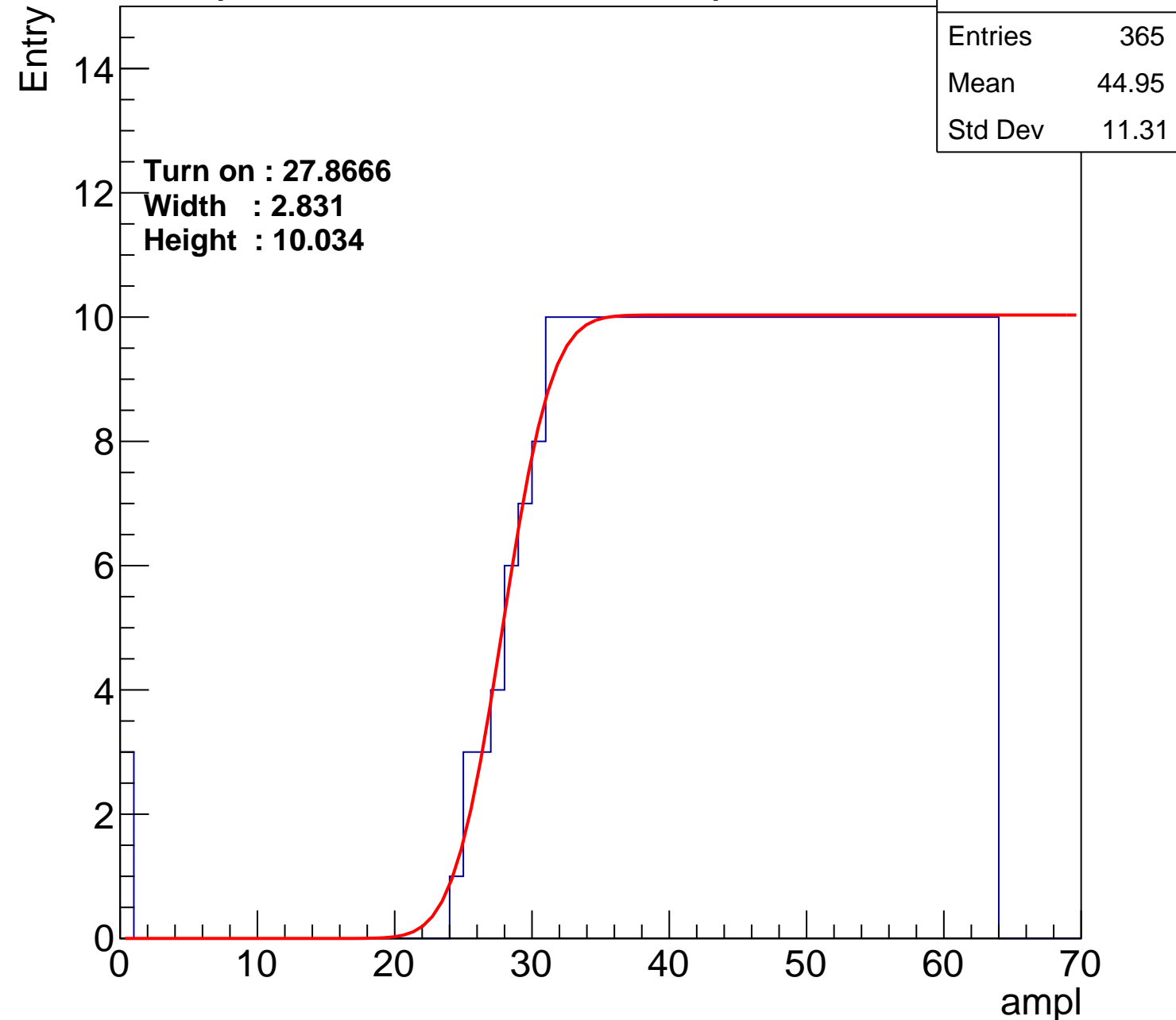
Width : 2.831

Height : 10.034

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



**B1L003S, U7-ch117**

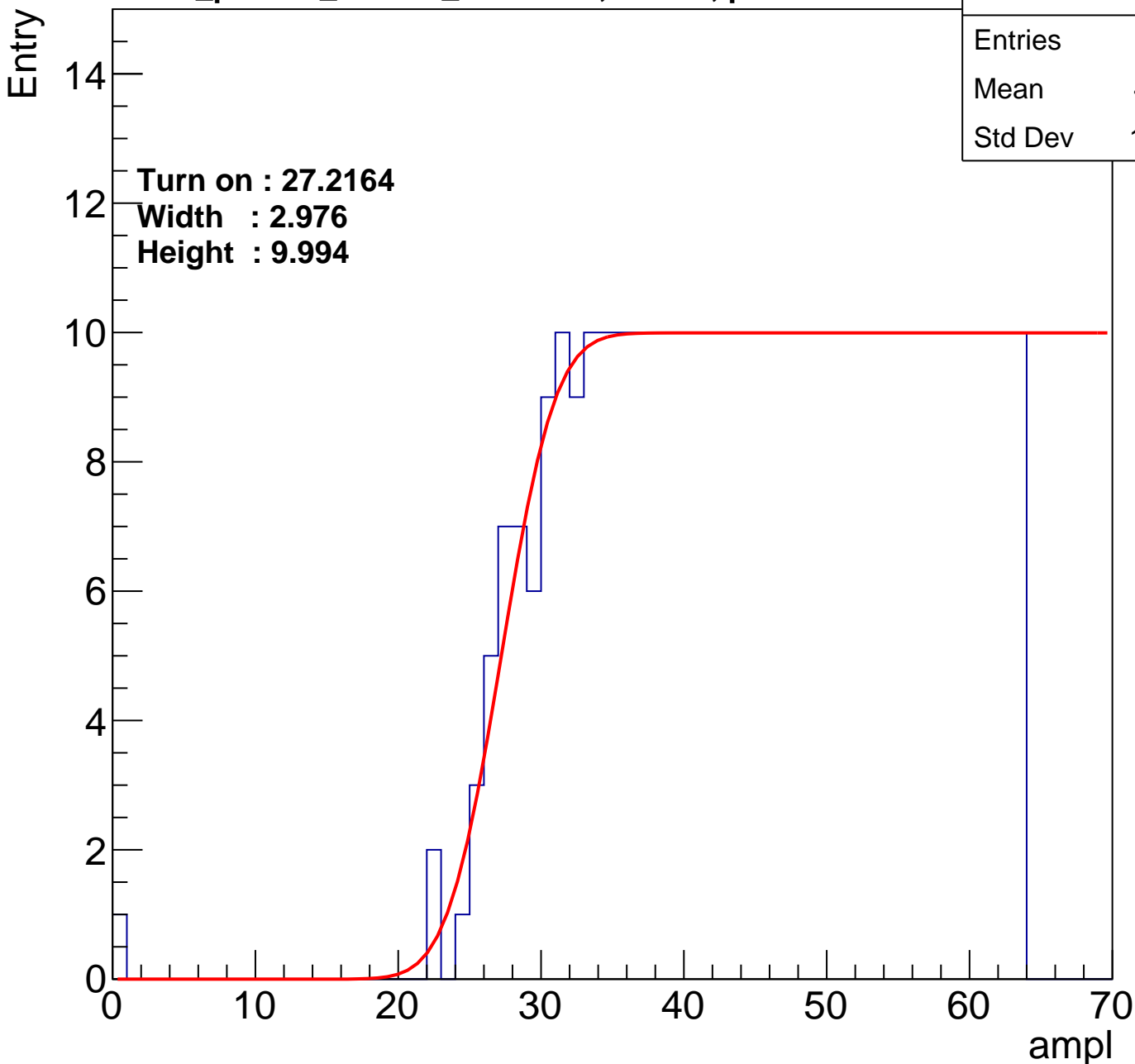
**calib\_packv5\_042523\_0143.root, FC#13, port D2**

Entries	370
Mean	44.81
Std Dev	11.08

**Turn on : 27.2164**

**Width : 2.976**

**Height : 9.994**



# B1L003S, U7-ch118

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	372
Mean	44.47
Std Dev	11.77

Turn on : 27.7647

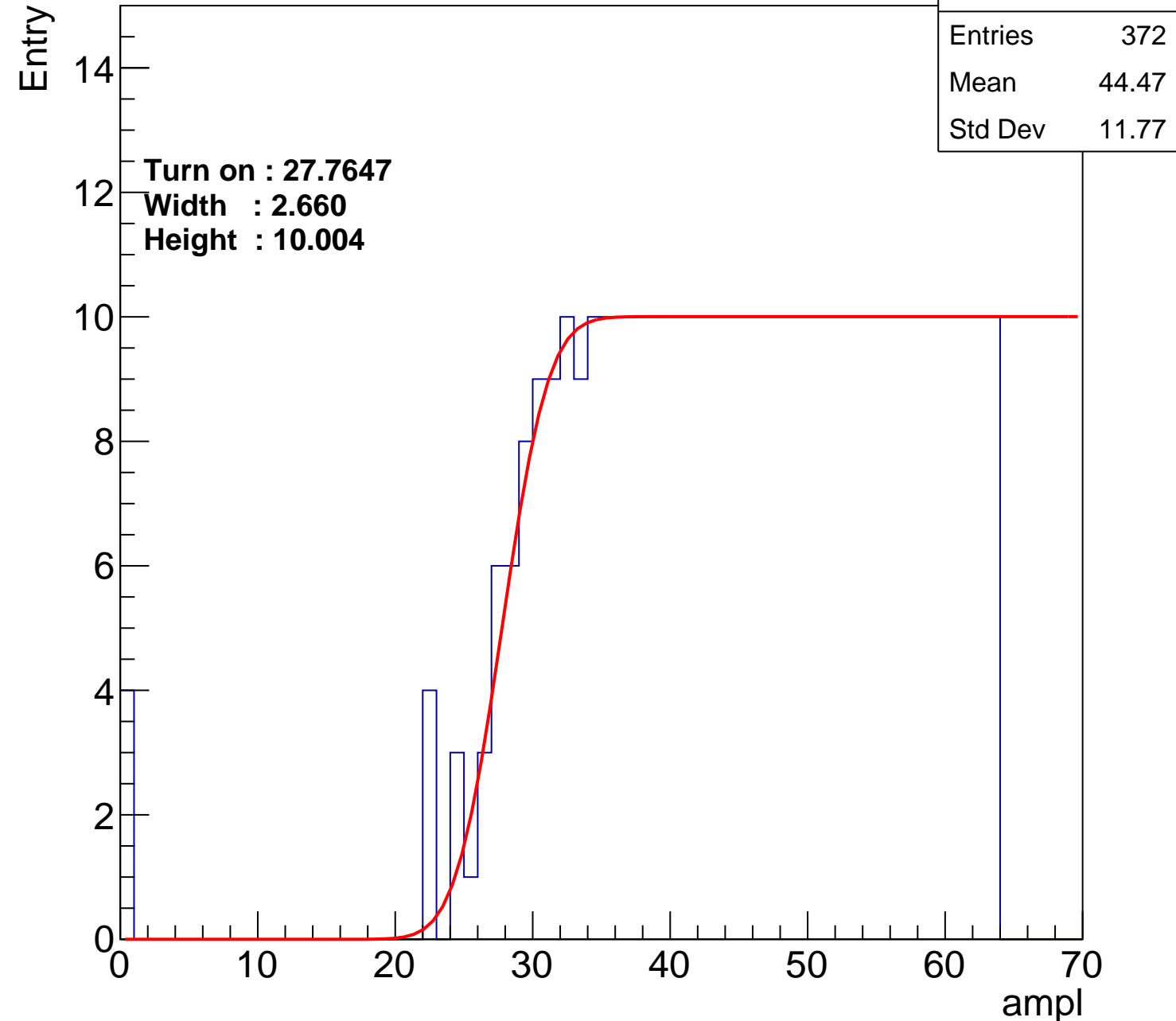
Width : 2.660

Height : 10.004

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L003S, U7-ch119

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	380
Mean	44.22
Std Dev	11.66

Turn on : 26.1256

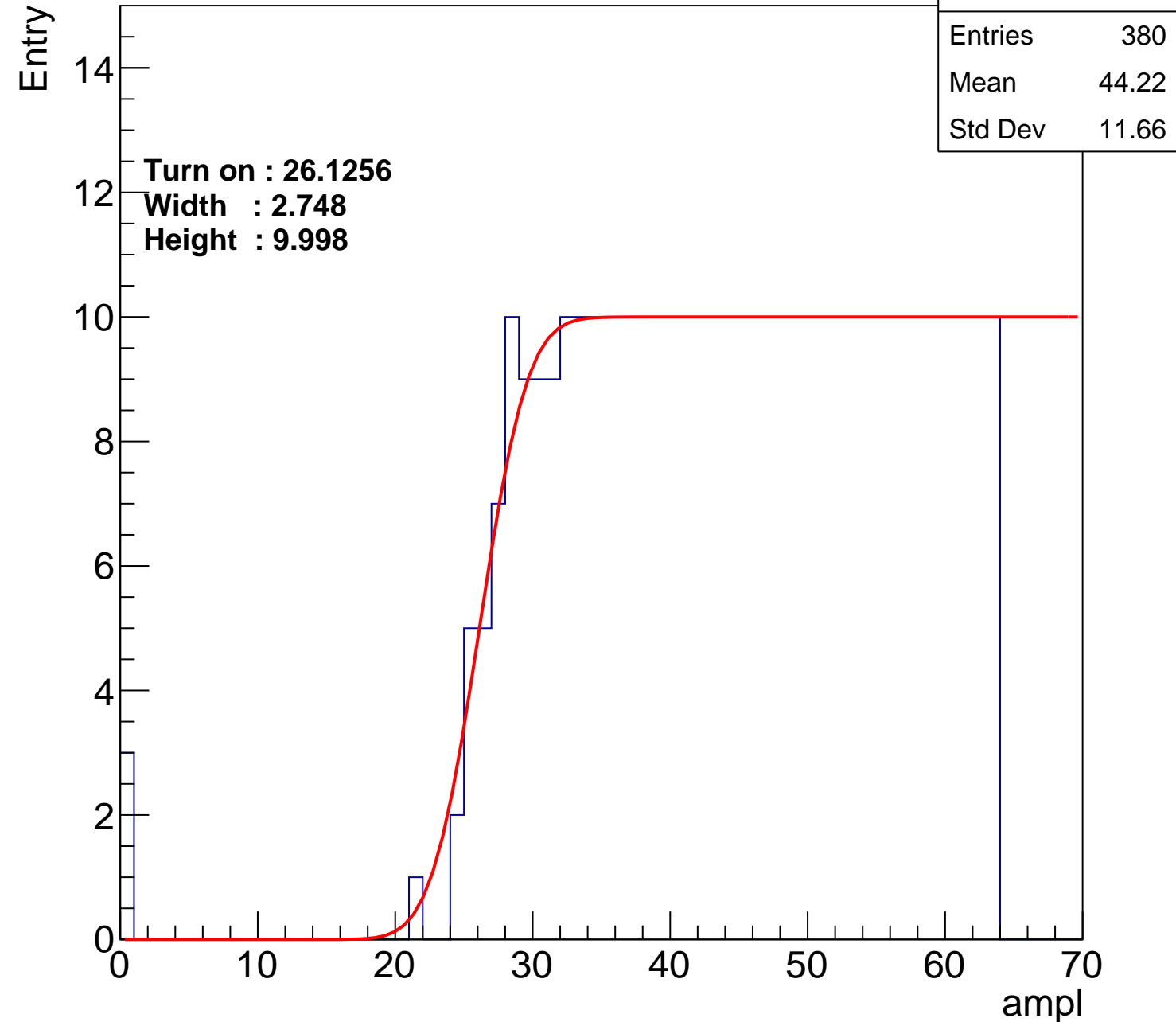
Width : 2.748

Height : 9.998

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch120

calib\_packv5\_042523\_0143.root, FC#13, port D2

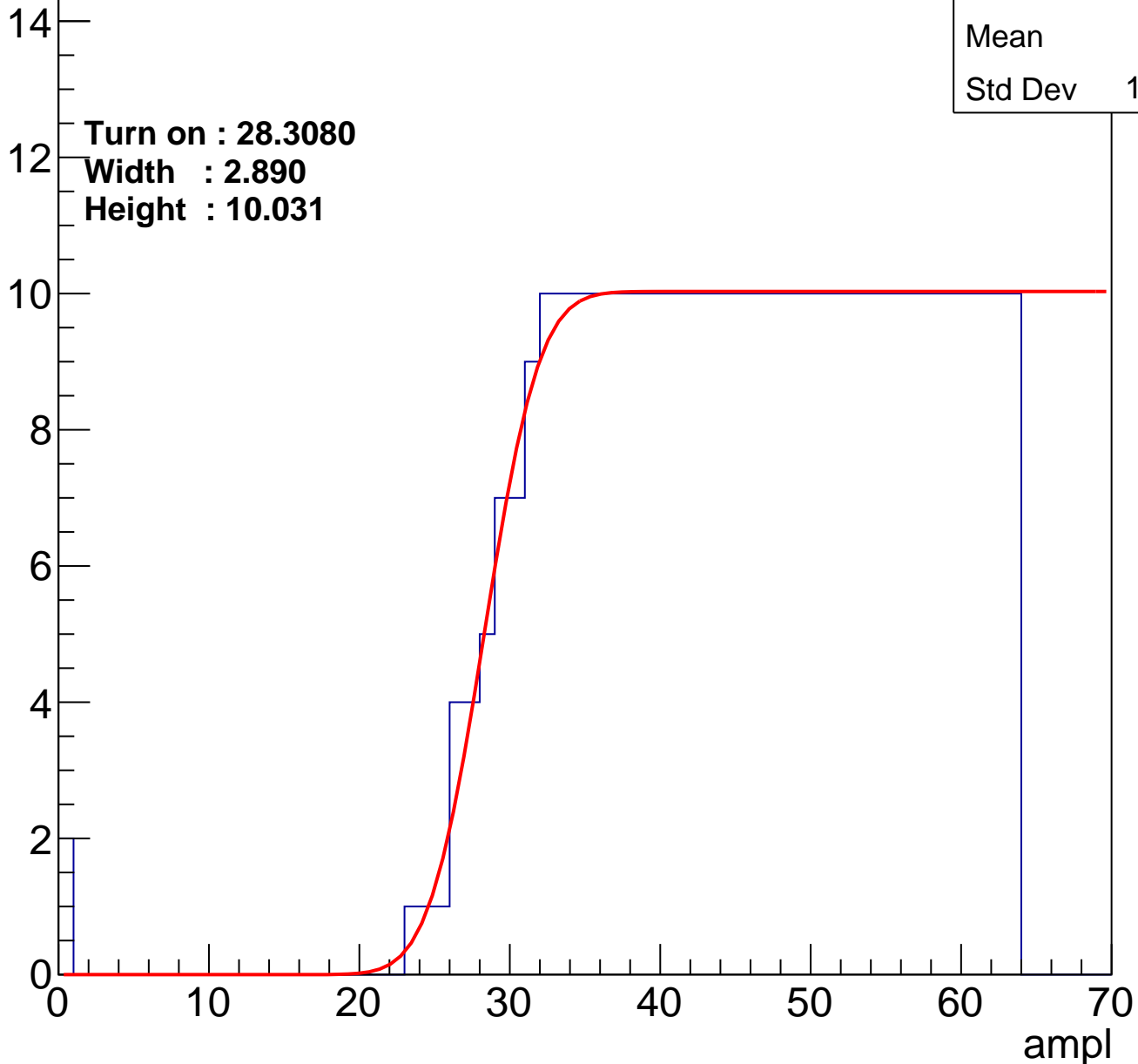
Entries	361
Mean	45.2
Std Dev	11.03

Turn on : 28.3080

Width : 2.890

Height : 10.031

Entry



# B1L003S, U7-ch121

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	364
Mean	44.86
Std Dev	11.58

Turn on : 28.6427

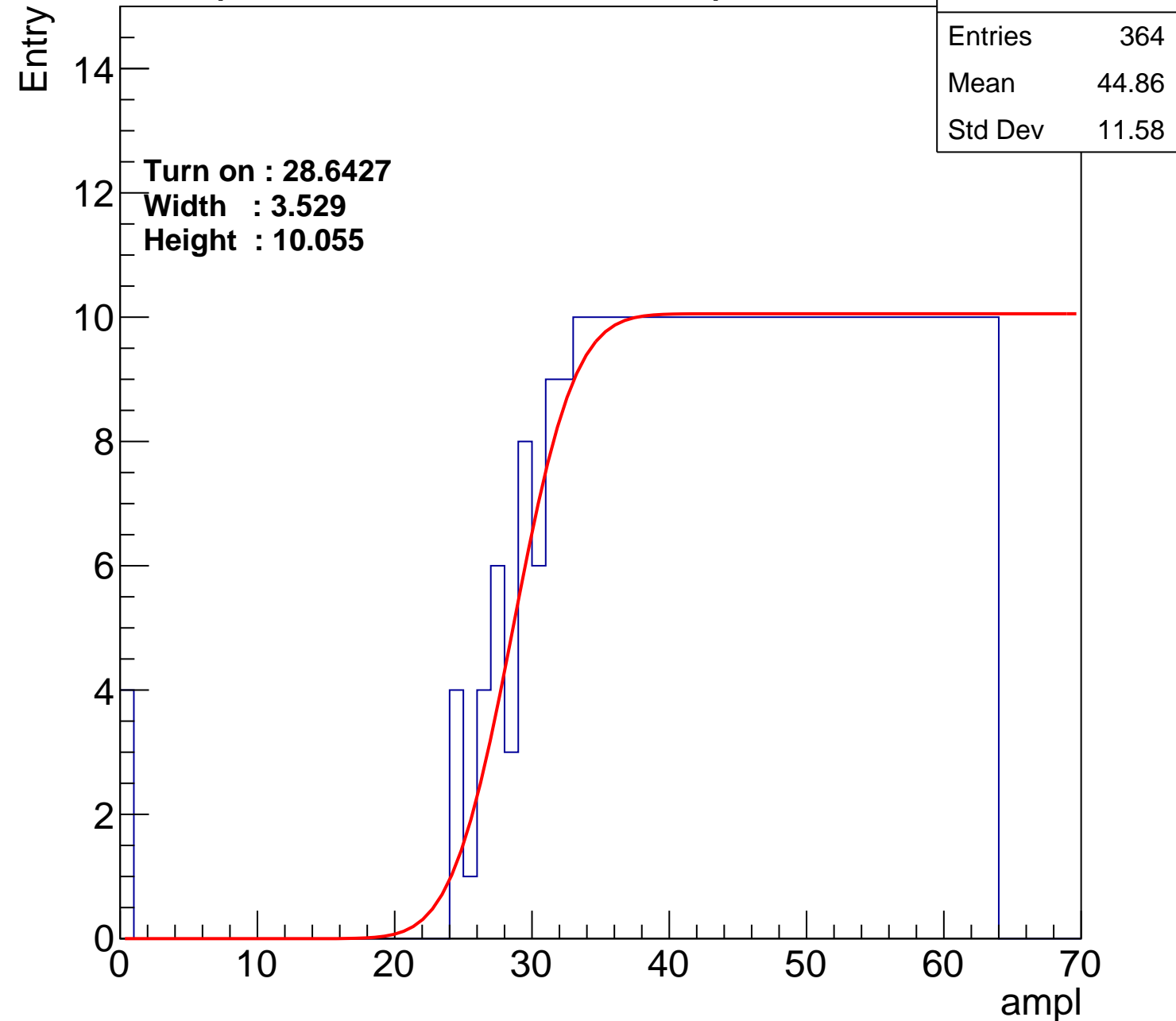
Width : 3.529

Height : 10.055

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch122

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	349
Mean	45.84
Std Dev	10.54

Turn on : 29.4211

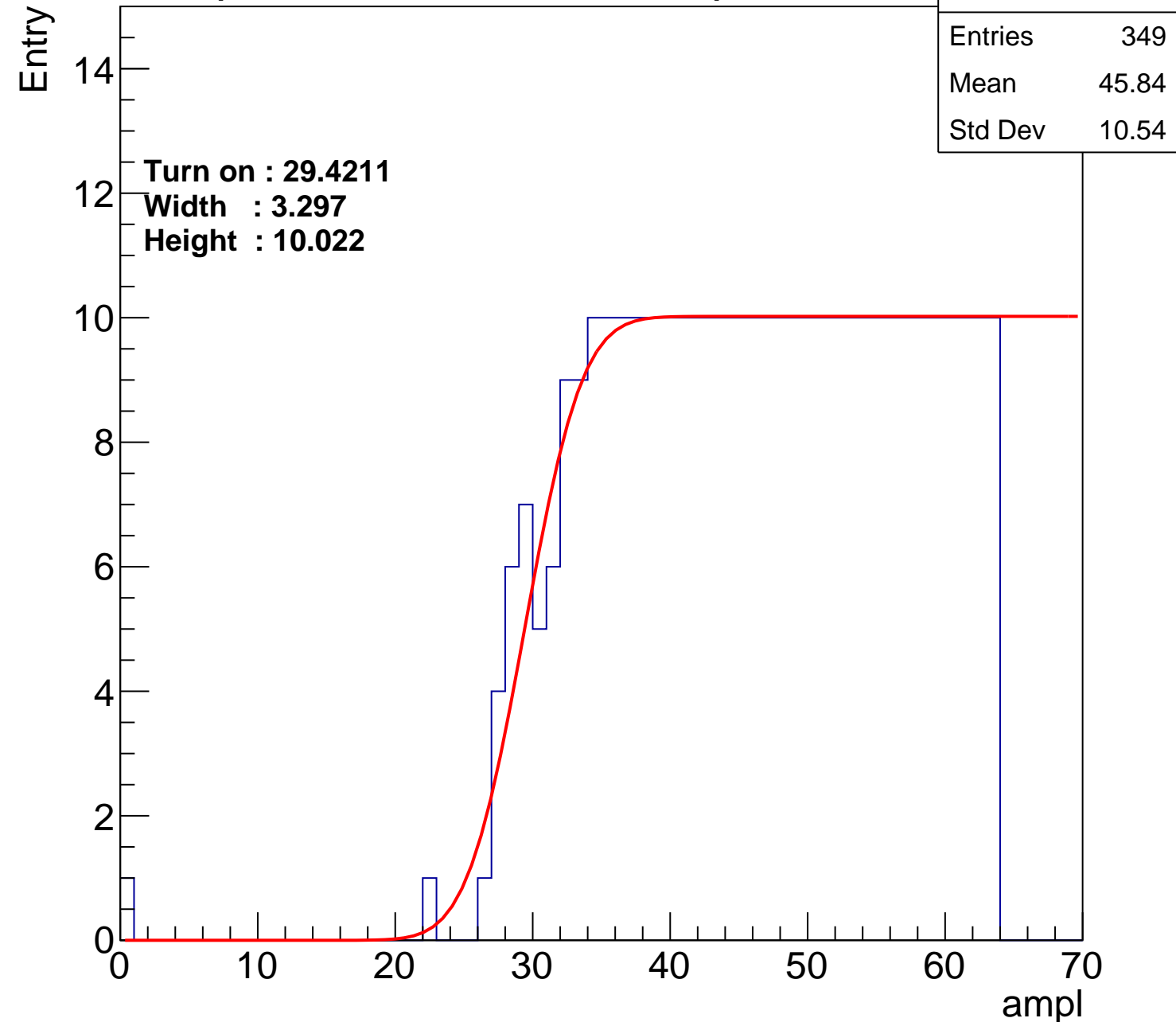
Width : 3.297

Height : 10.022

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch123

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	366
Mean	44.91
Std Dev	11.22

Turn on : 27.5851

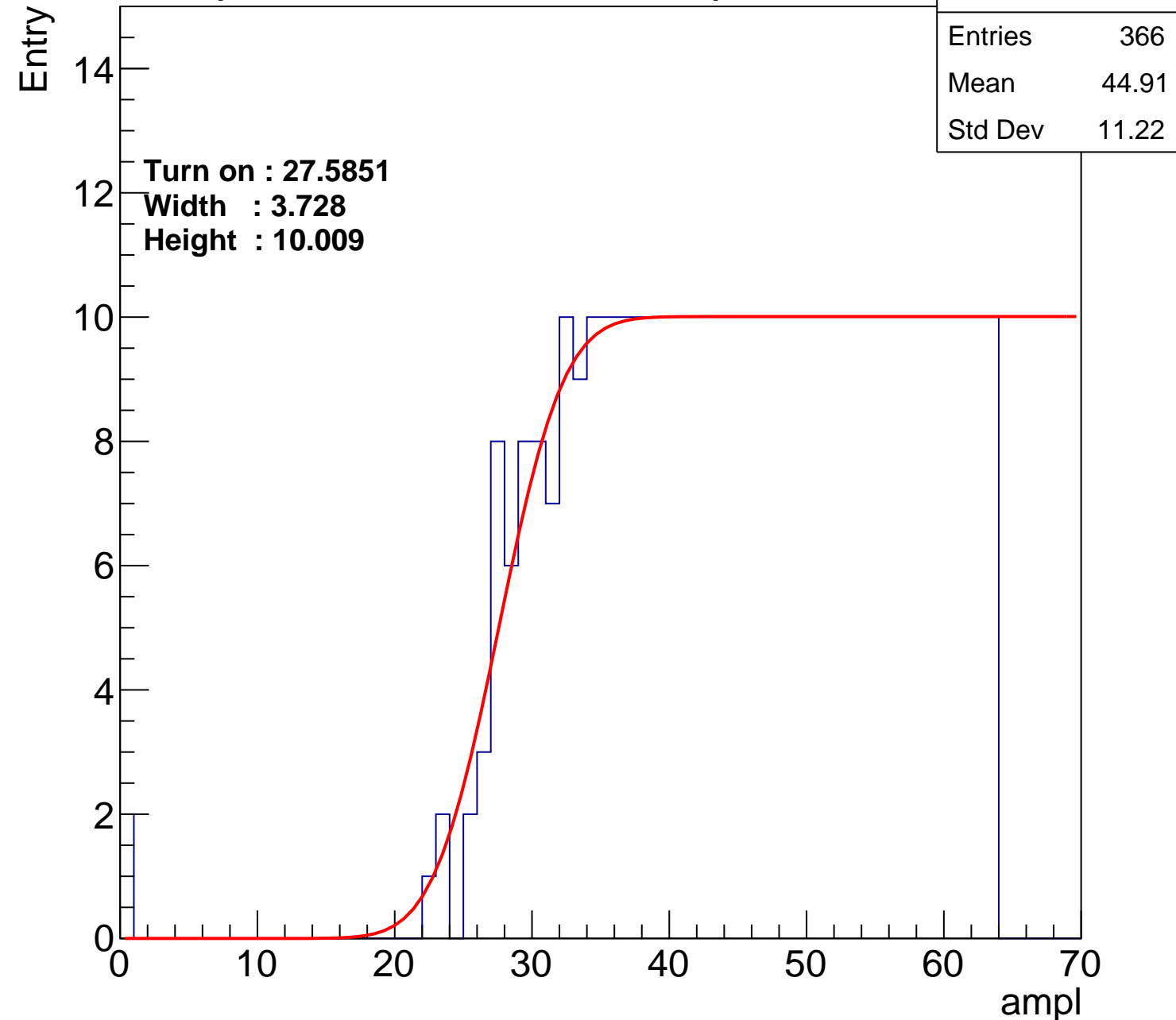
Width : 3.728

Height : 10.009

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch124

calib\_packv5\_042523\_0143.root, FC#13, port D2

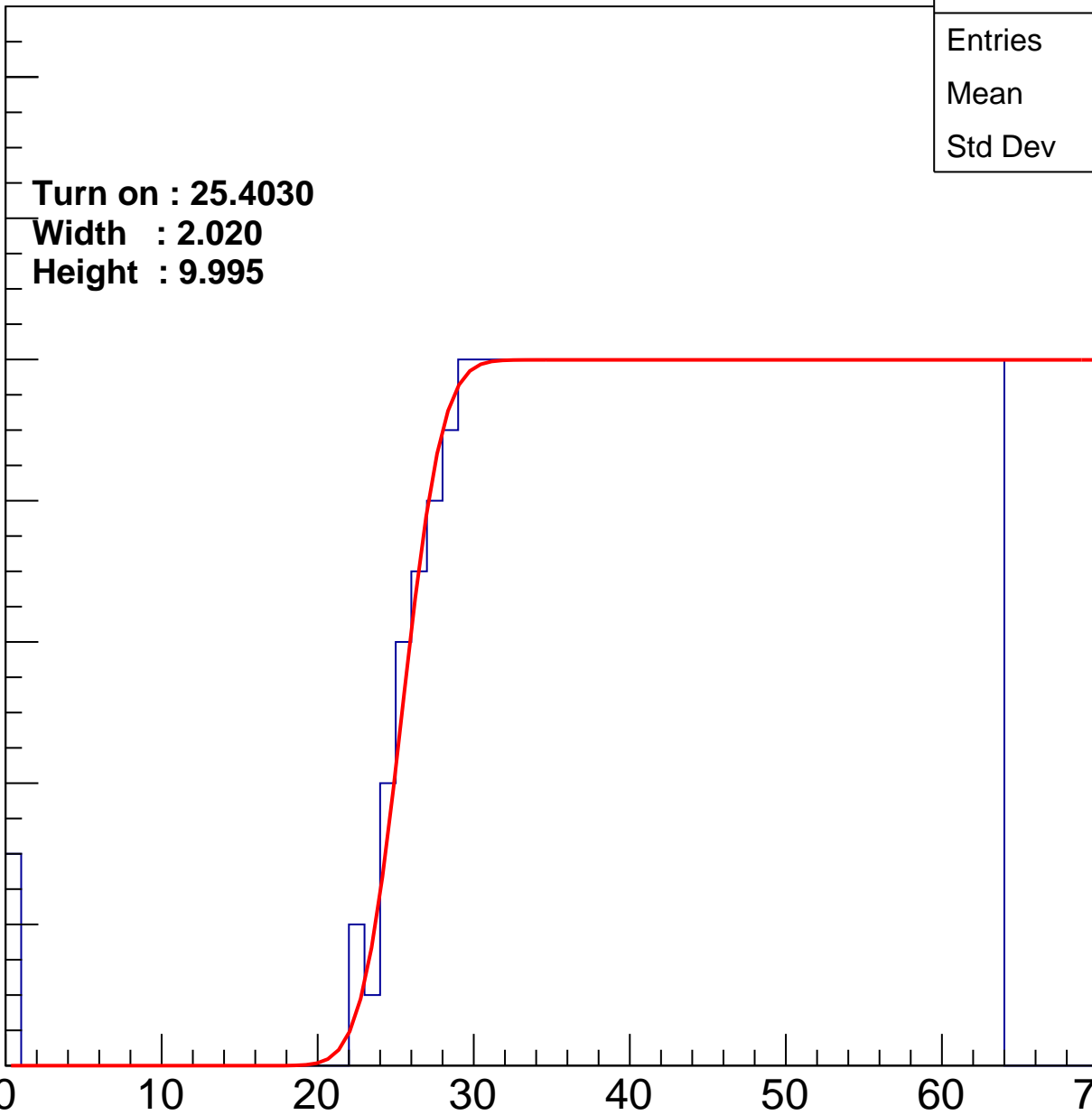
Entry

14  
12  
10  
8  
6  
4  
2  
0

Turn on : 25.4030  
Width : 2.020  
Height : 9.995

Entries	390
Mean	43.75
Std Dev	11.87

ampl



# B1L003S, U7-ch125

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	372
Mean	44.7
Std Dev	11.16

Turn on : 26.8982

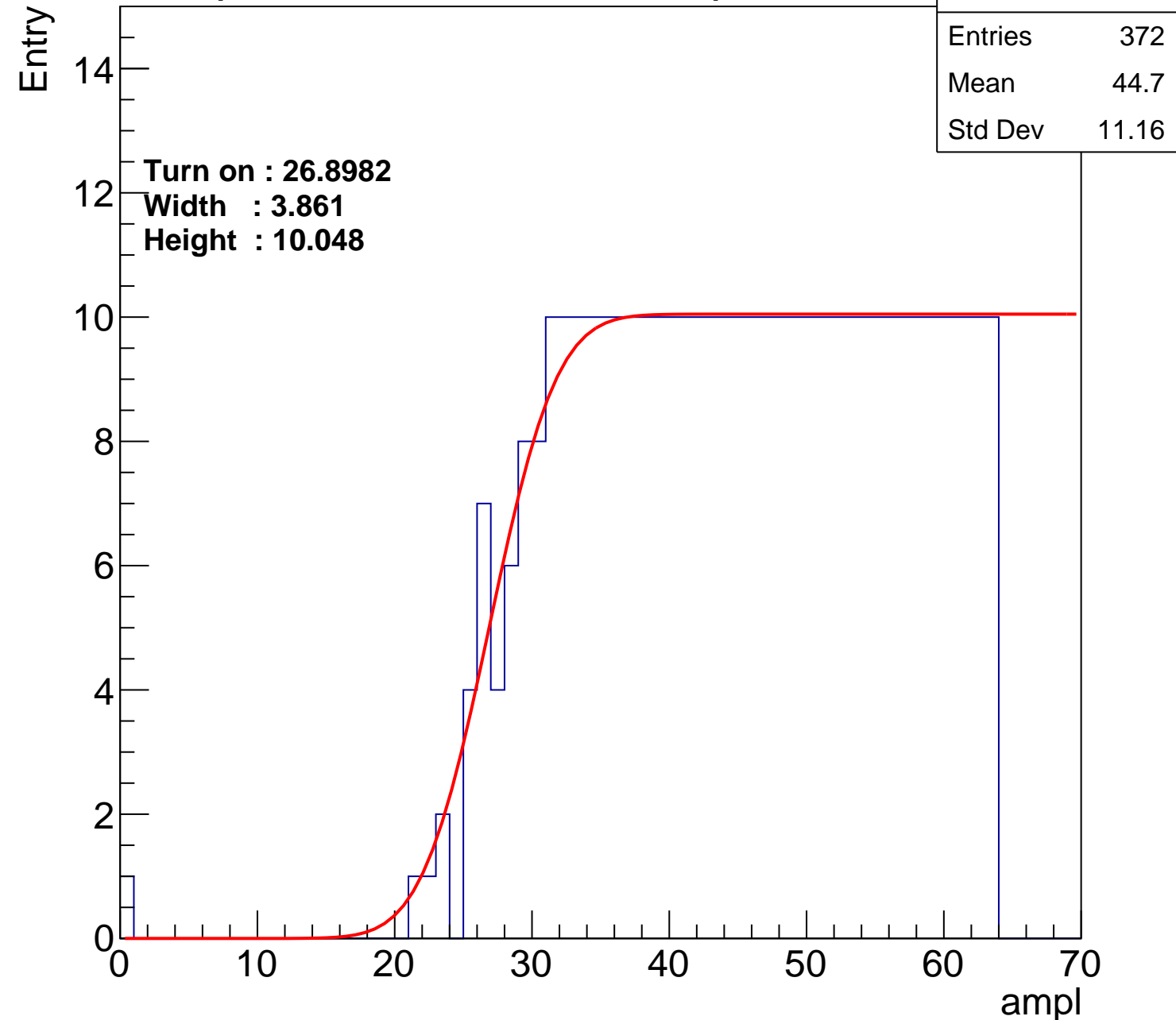
Width : 3.861

Height : 10.048

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch126

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	375
Mean	44.57
Std Dev	11.22

Turn on : 27.1312

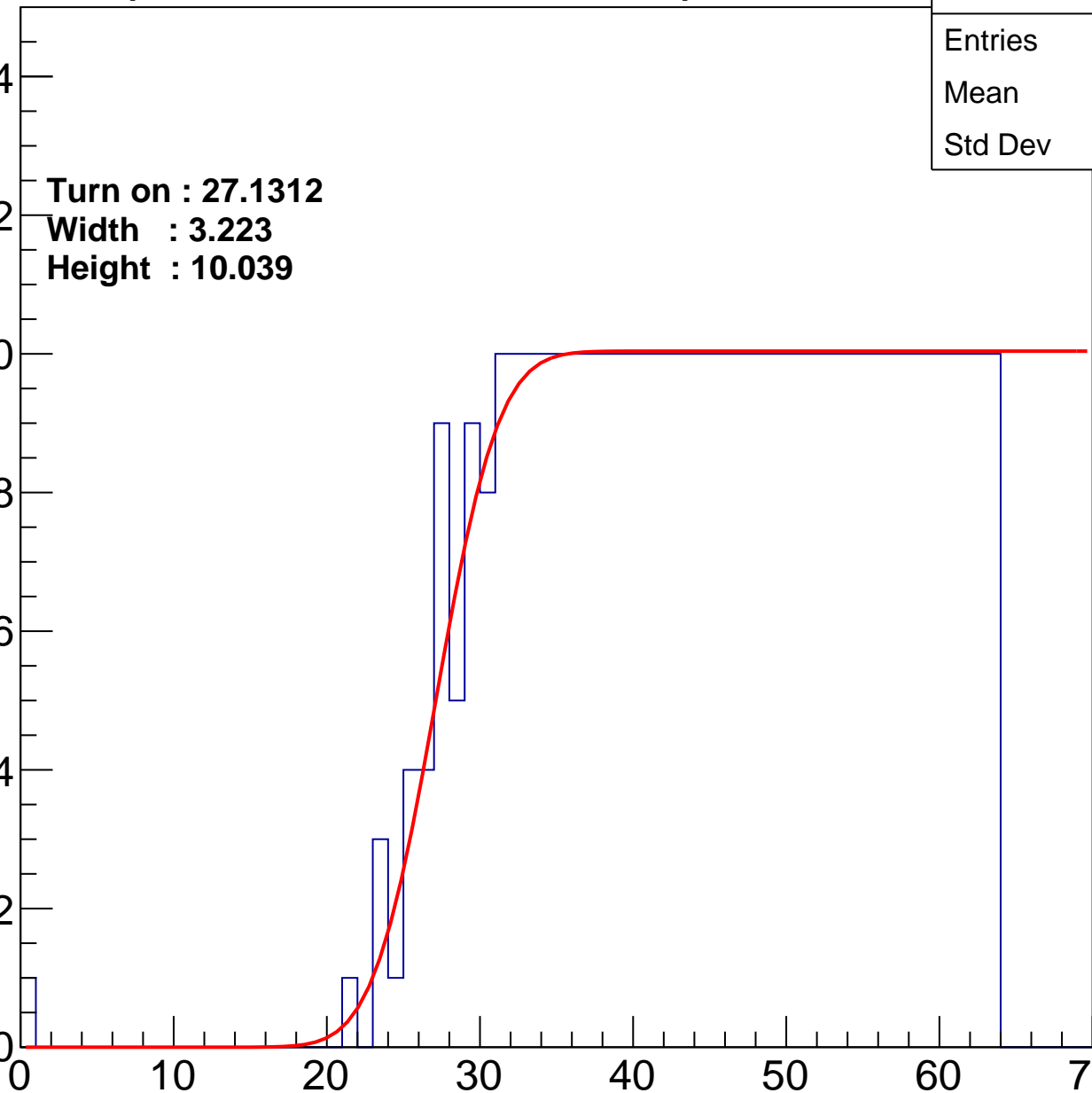
Width : 3.223

Height : 10.039

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L003S, U7-ch127

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	365
Mean	44.89
Std Dev	11.39

Turn on : 28.4562

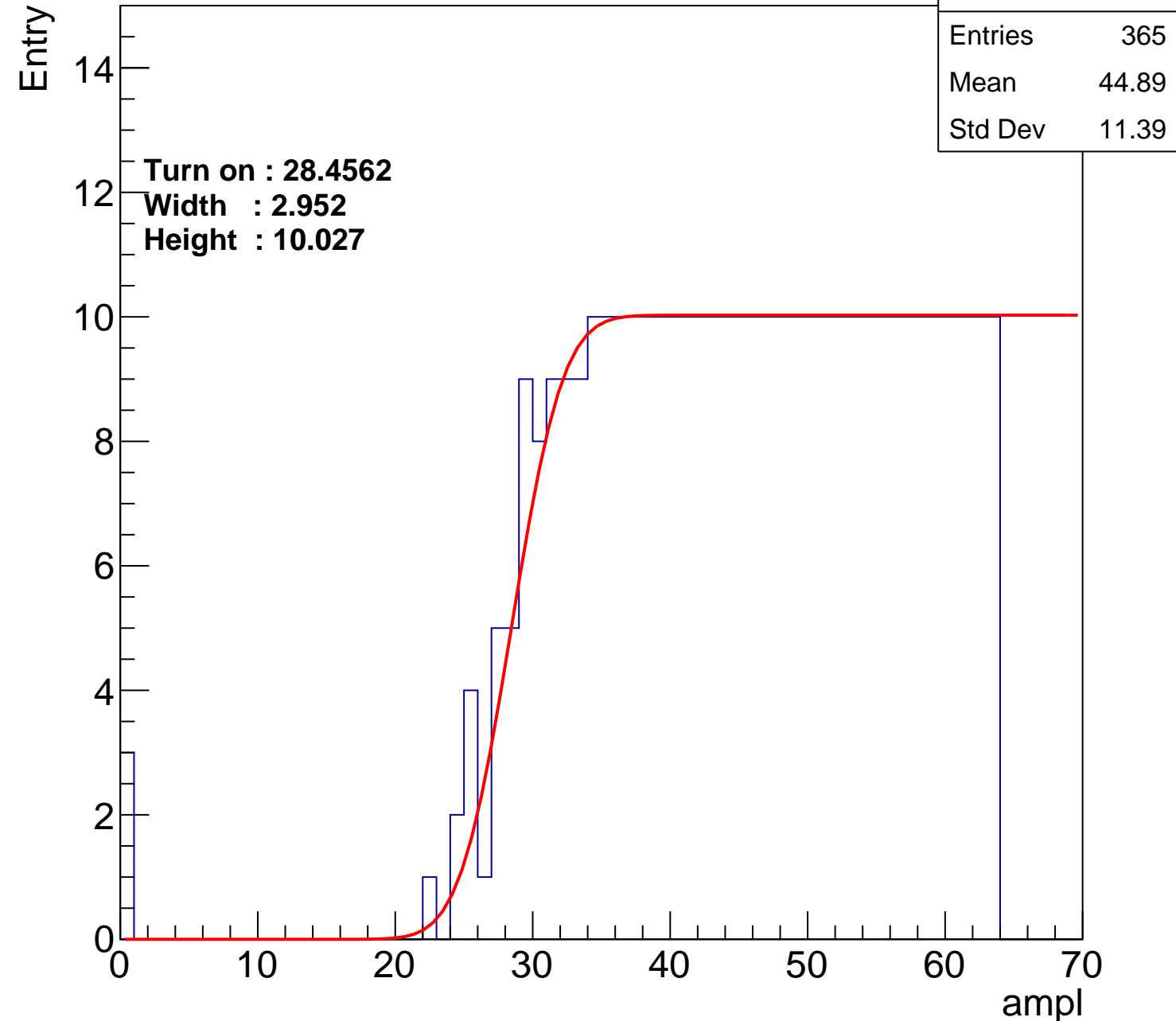
Width : 2.952

Height : 10.027

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L003S, U7-ch127

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	365
Mean	44.89
Std Dev	11.39

Turn on : 28.4562

Width : 2.952

Height : 10.027

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl

