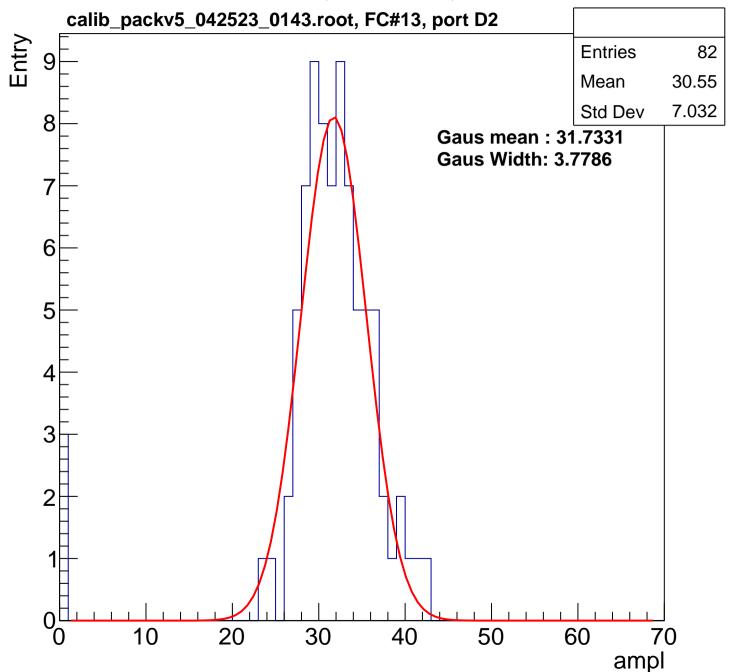
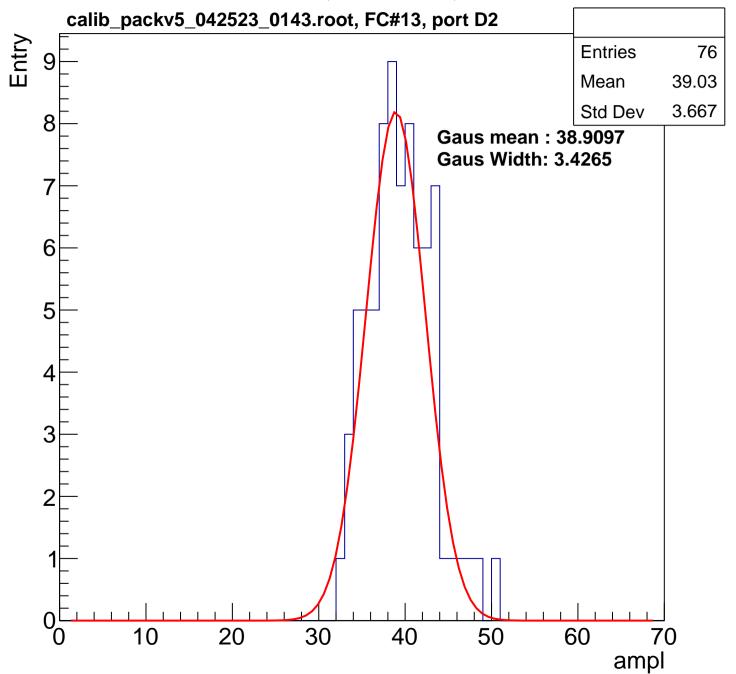
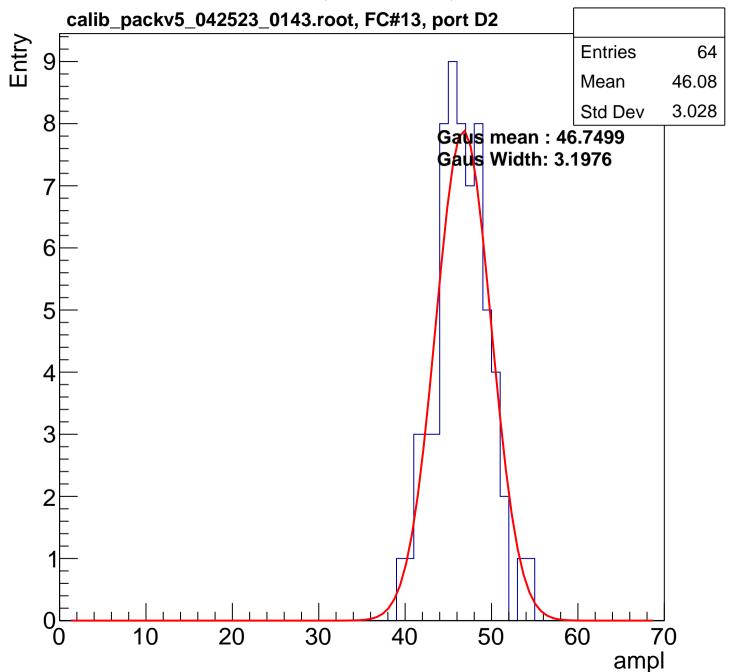
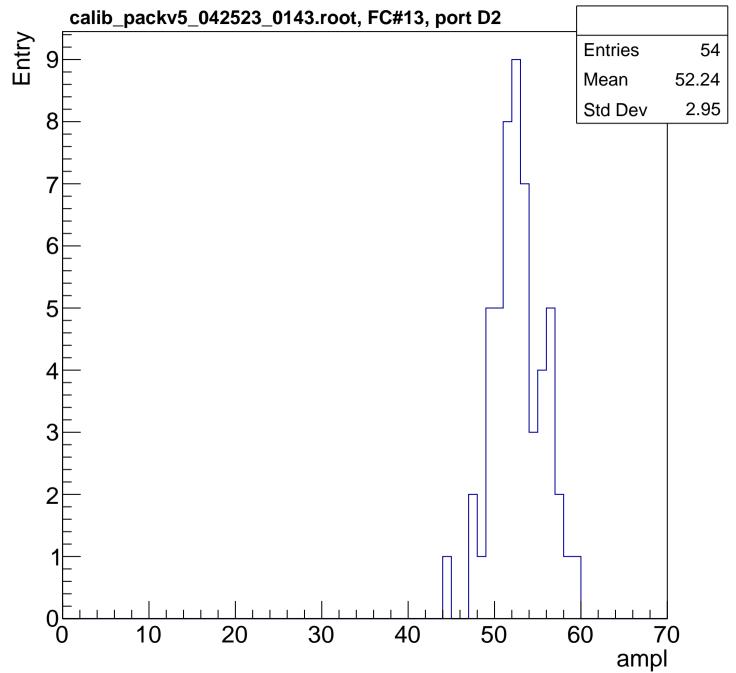


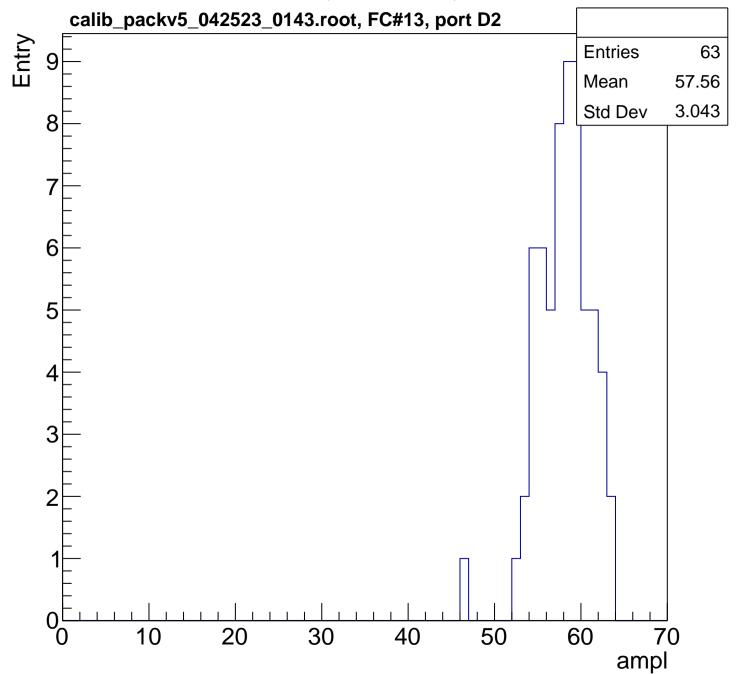
B1L003S, U9-ch2, adc7 calib\_packv5\_042523\_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

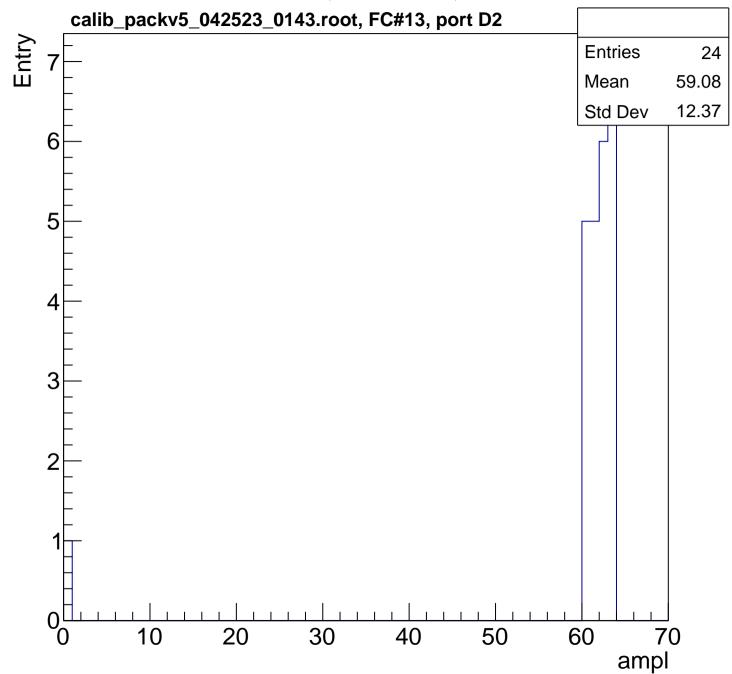


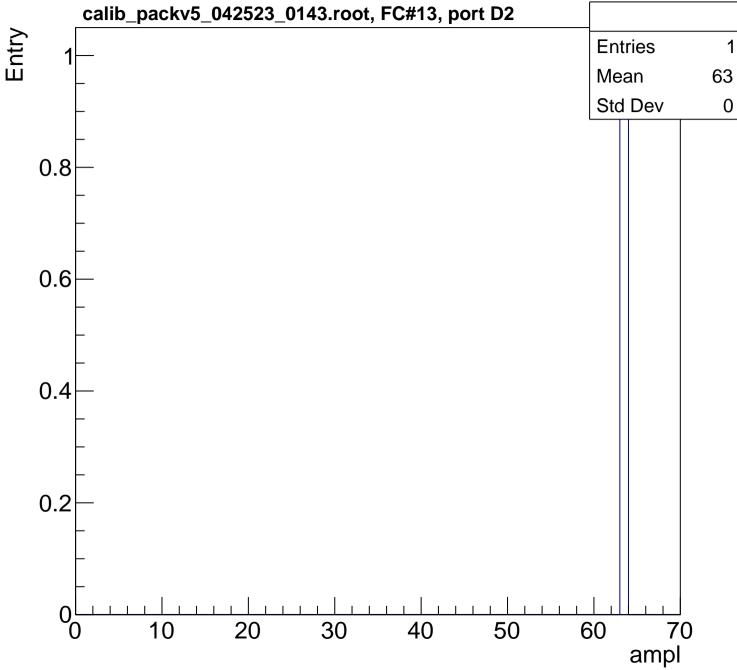




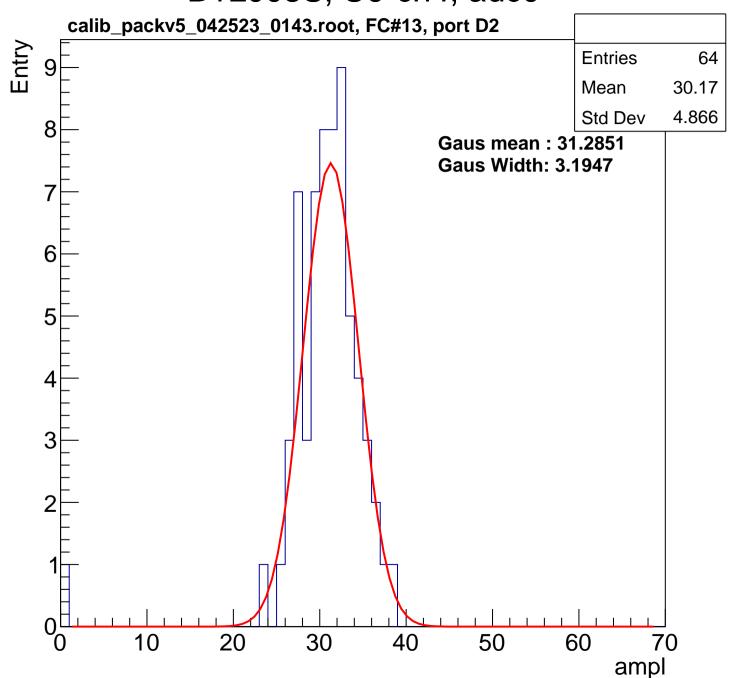


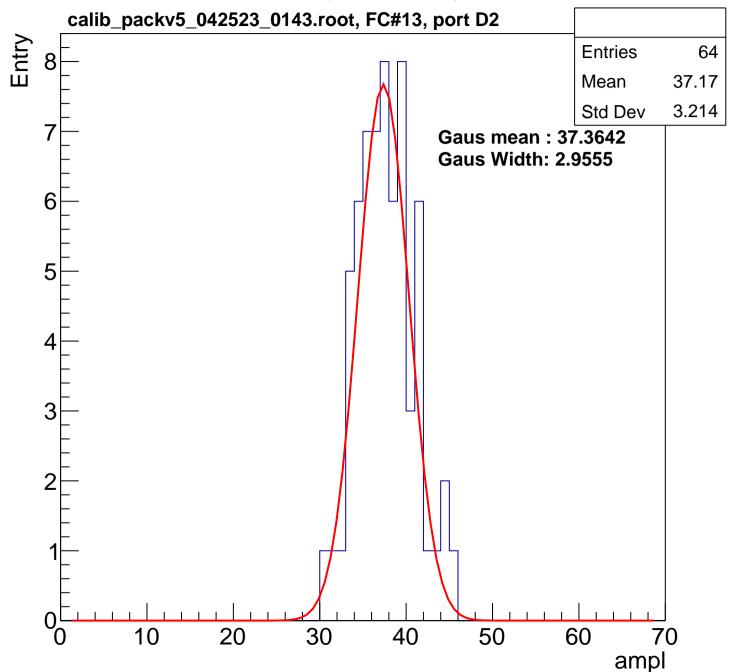


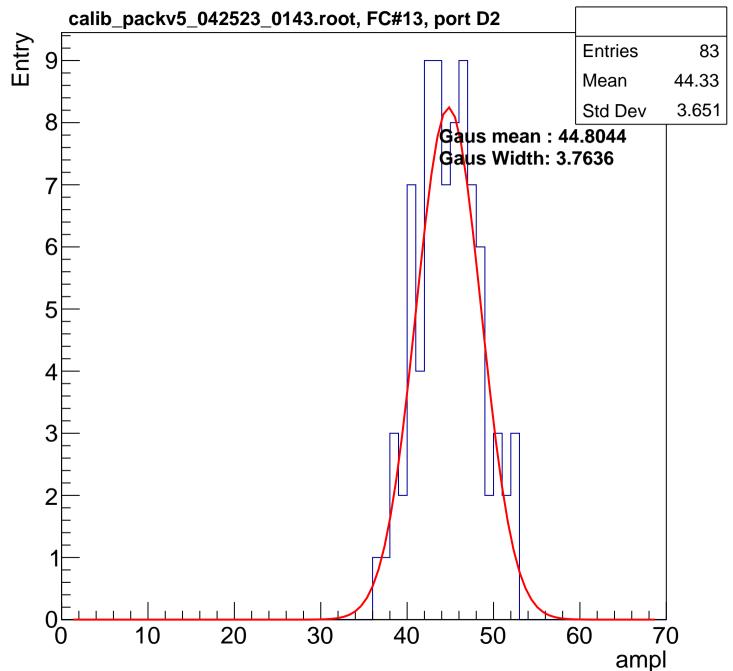


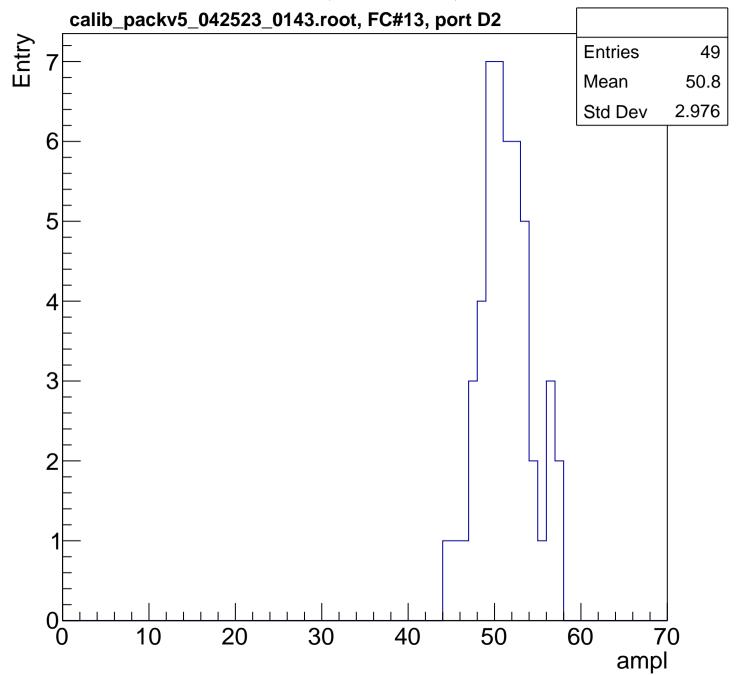


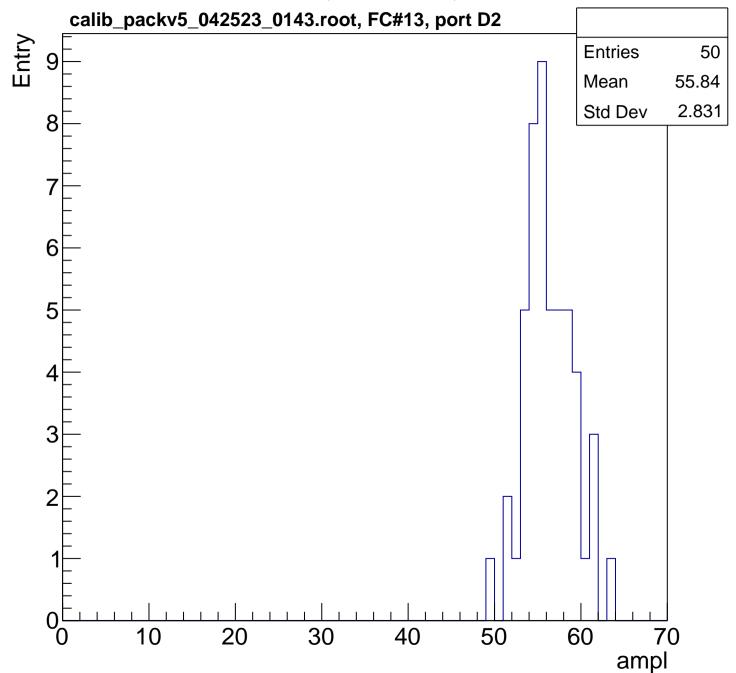
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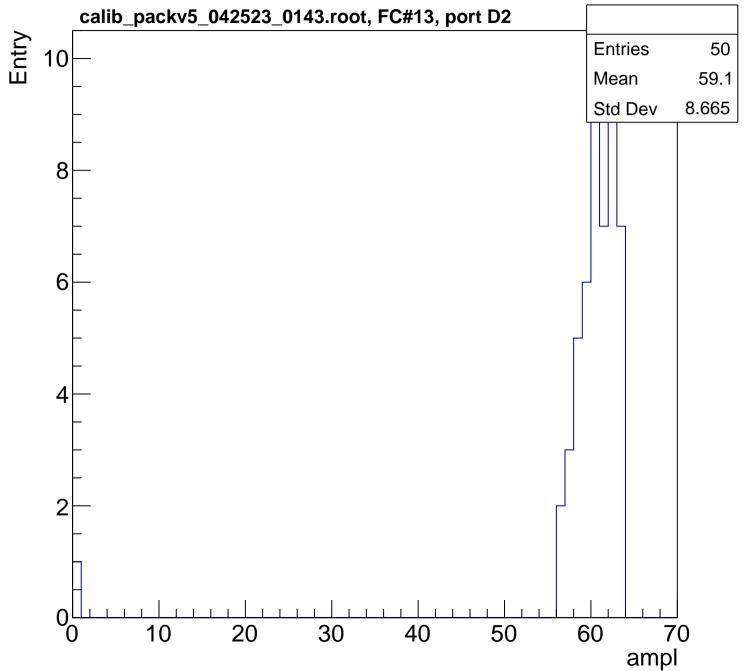


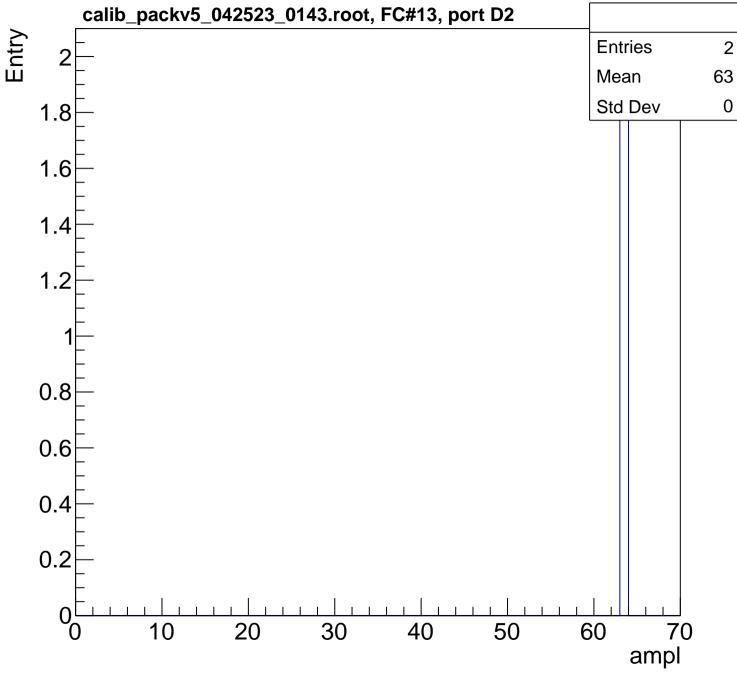


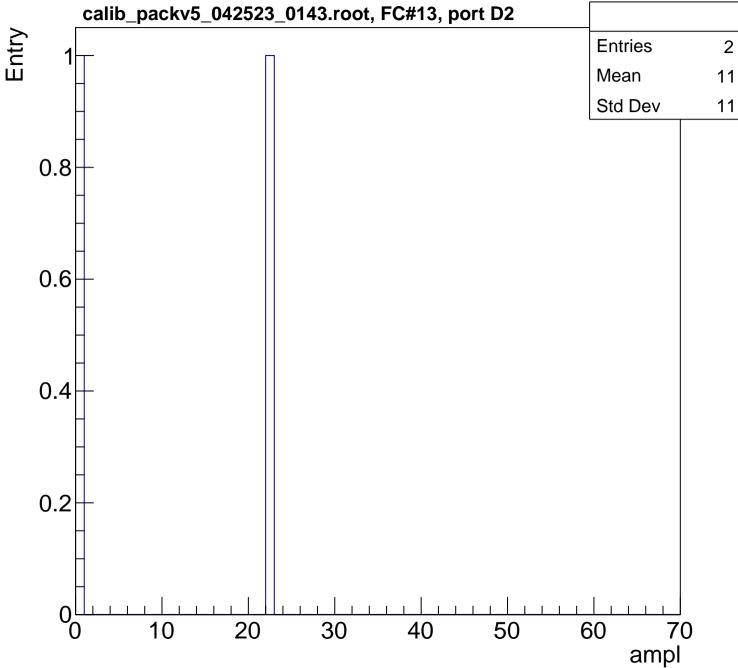


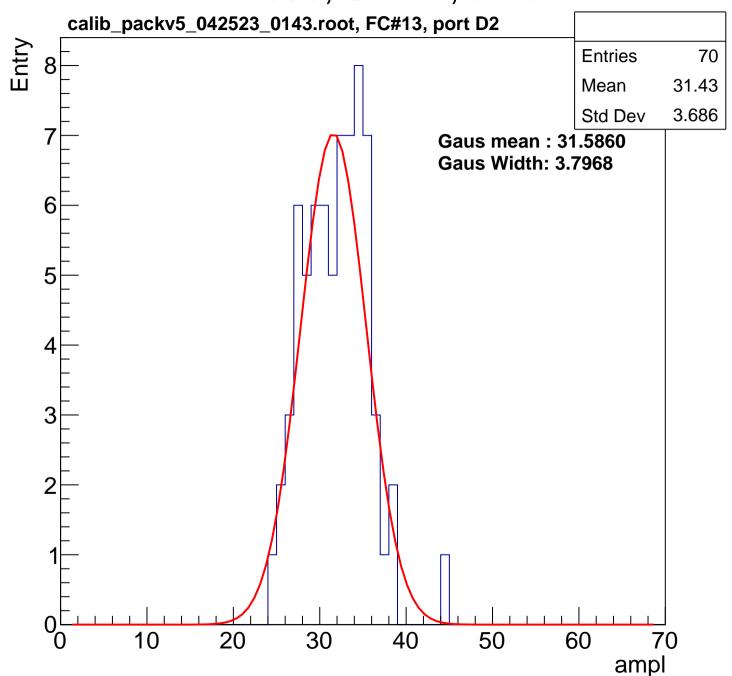


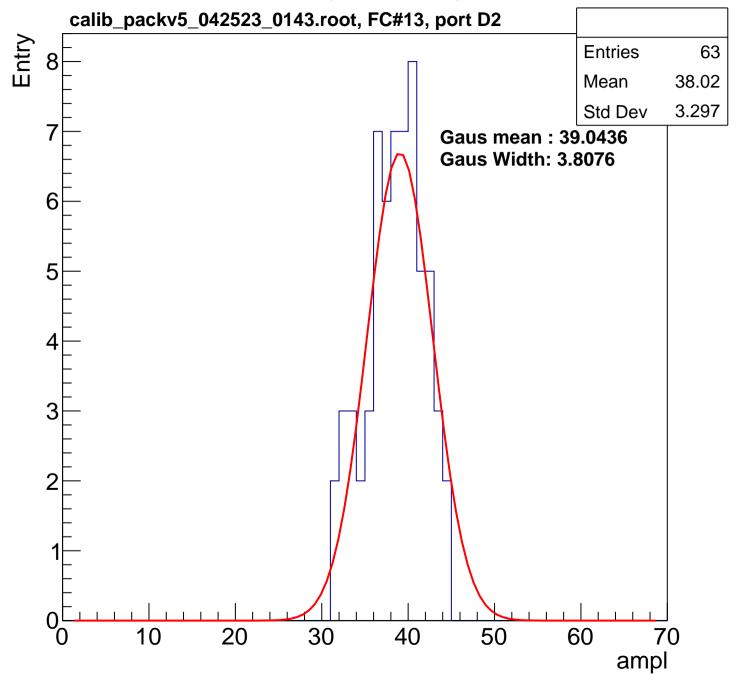


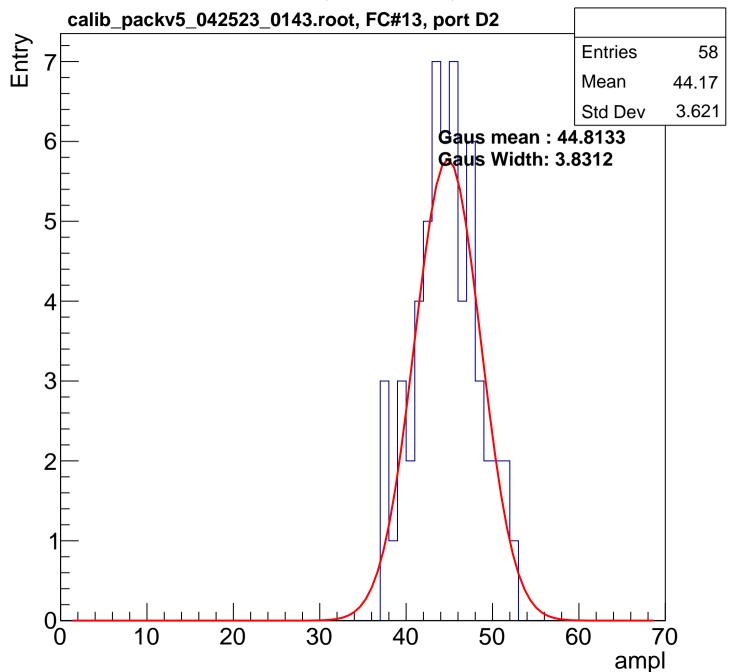


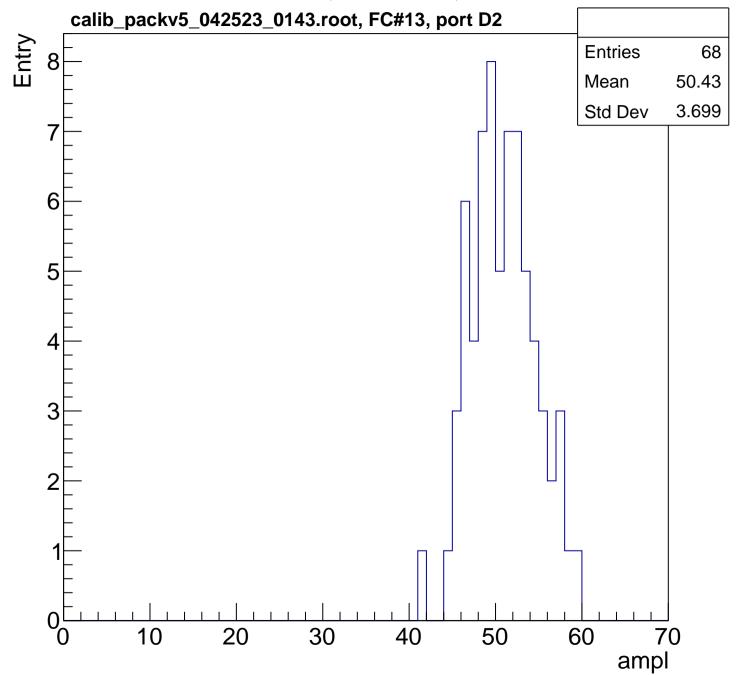


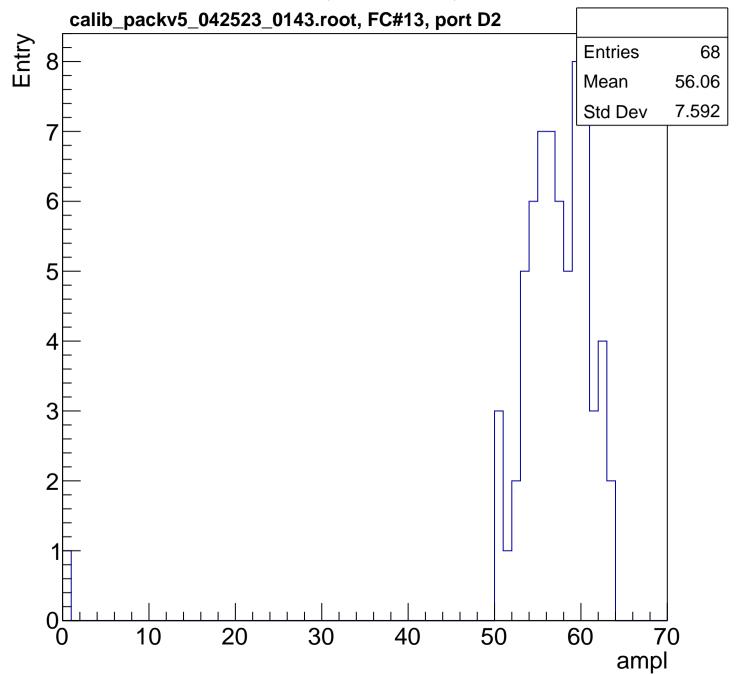


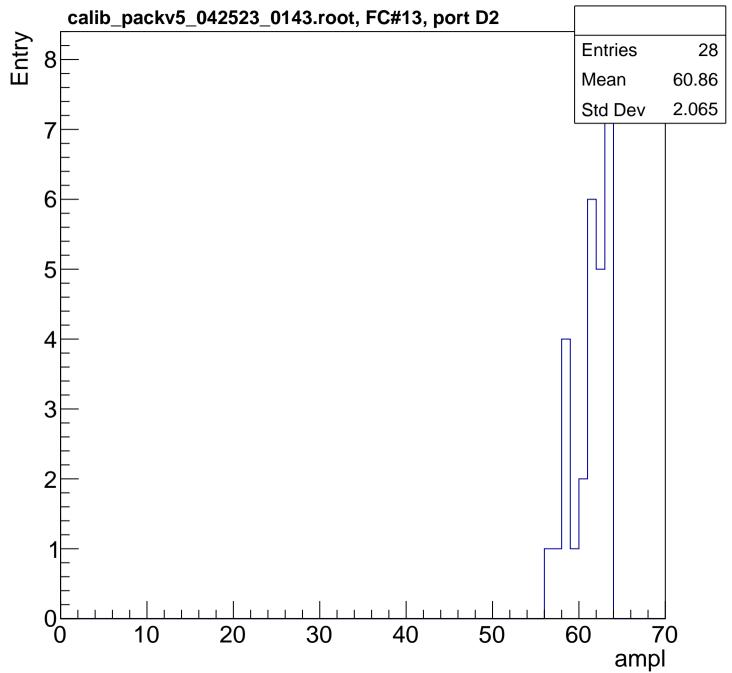


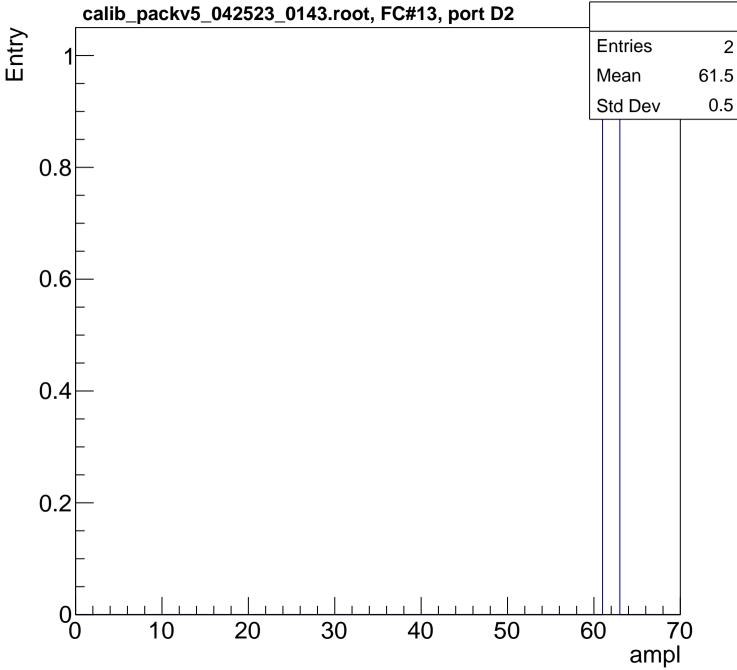


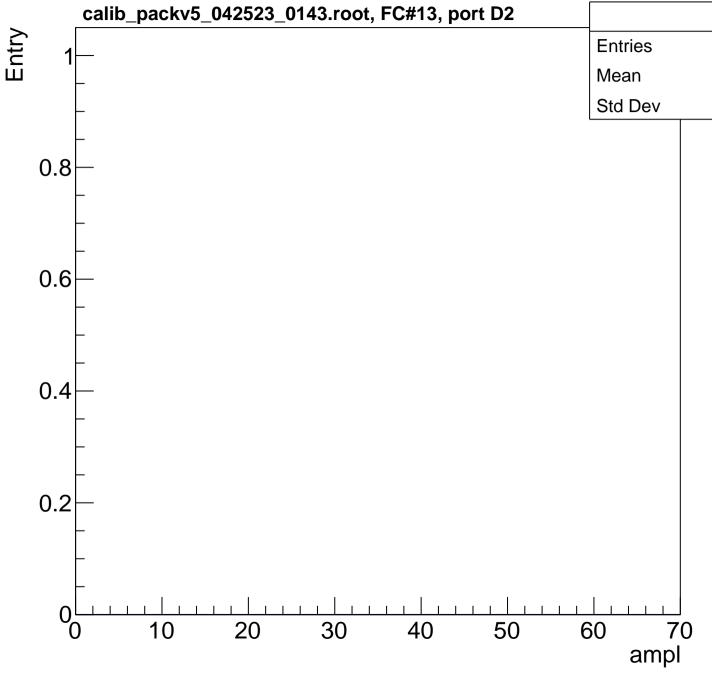


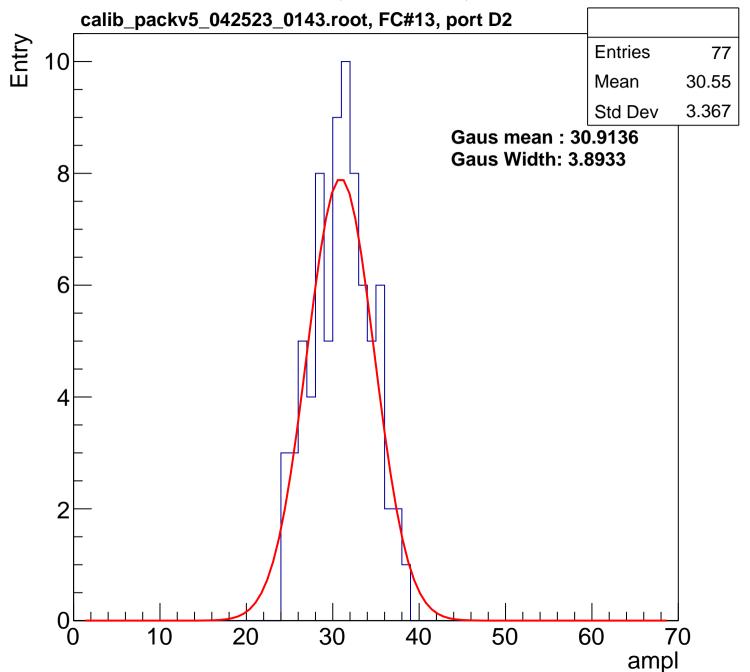


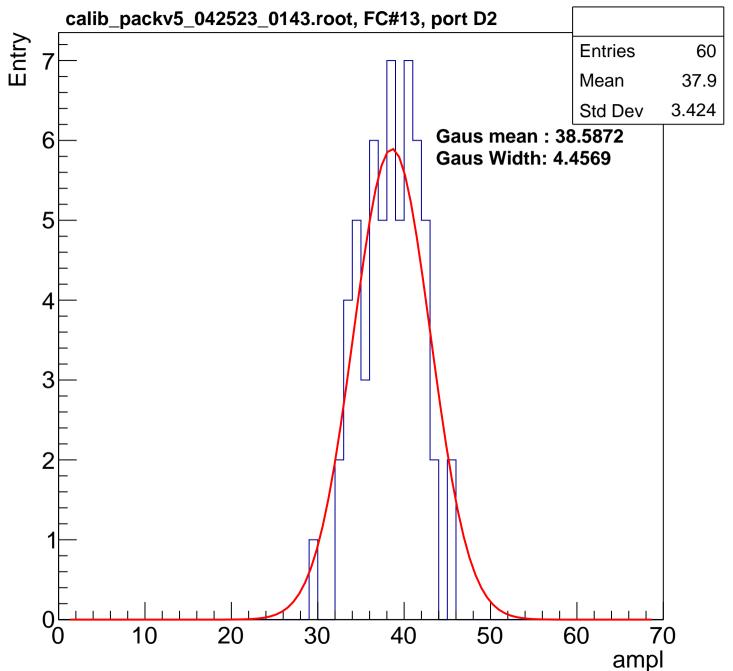


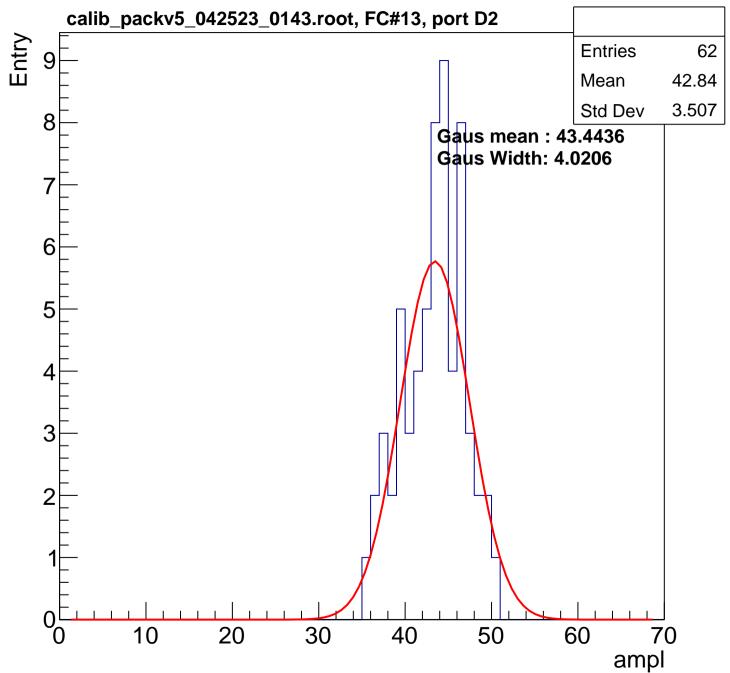


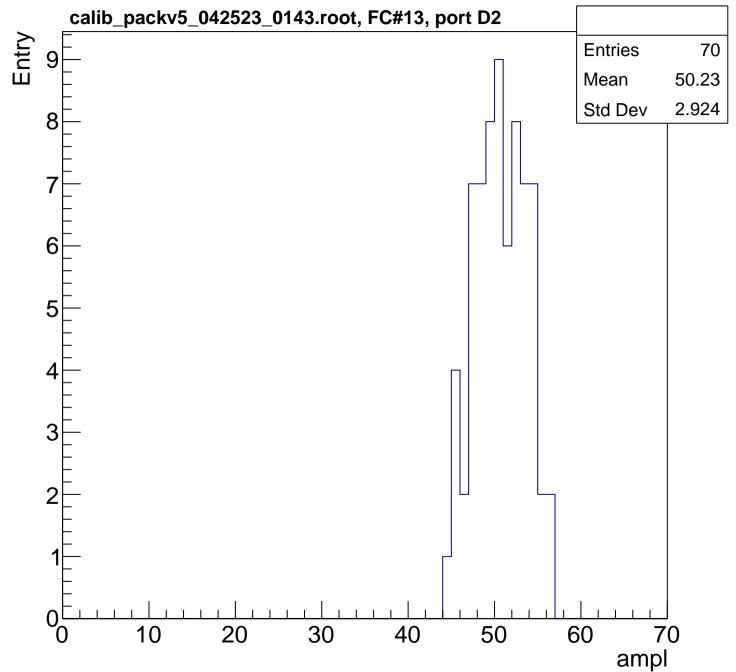


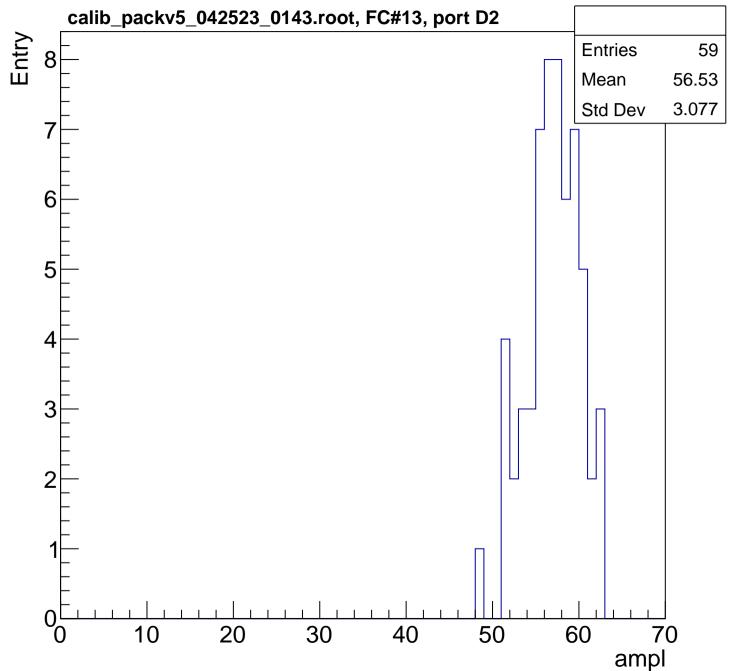


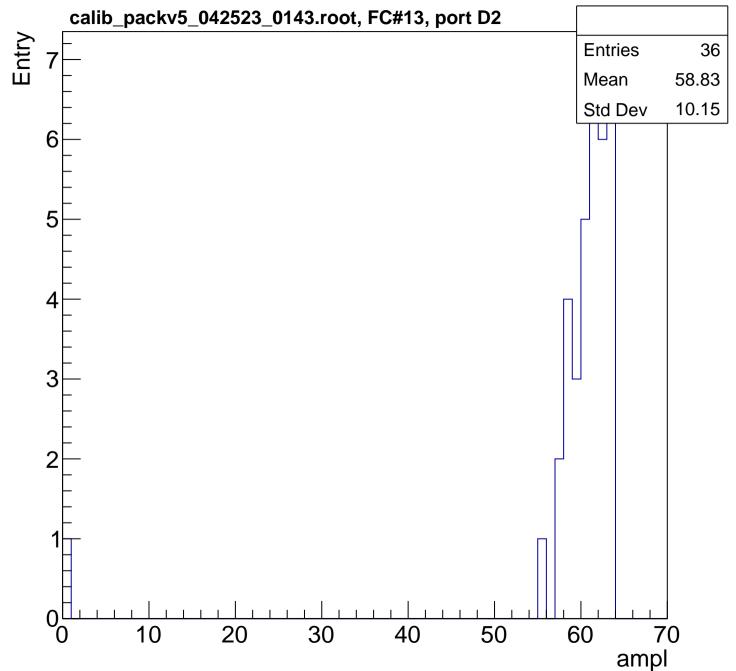


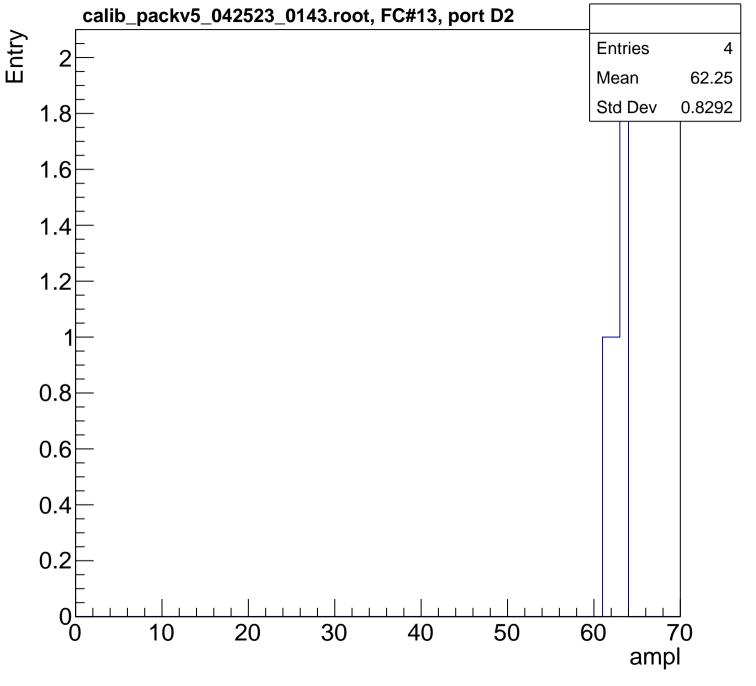


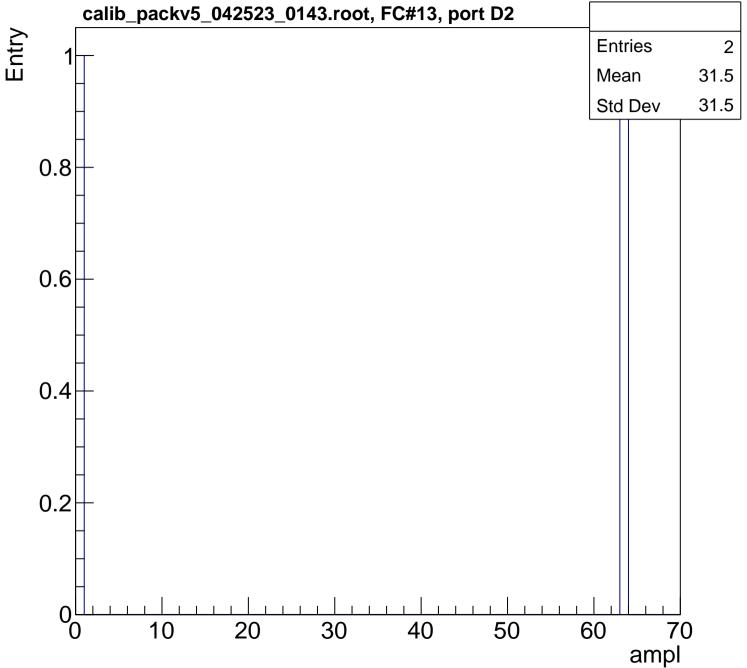


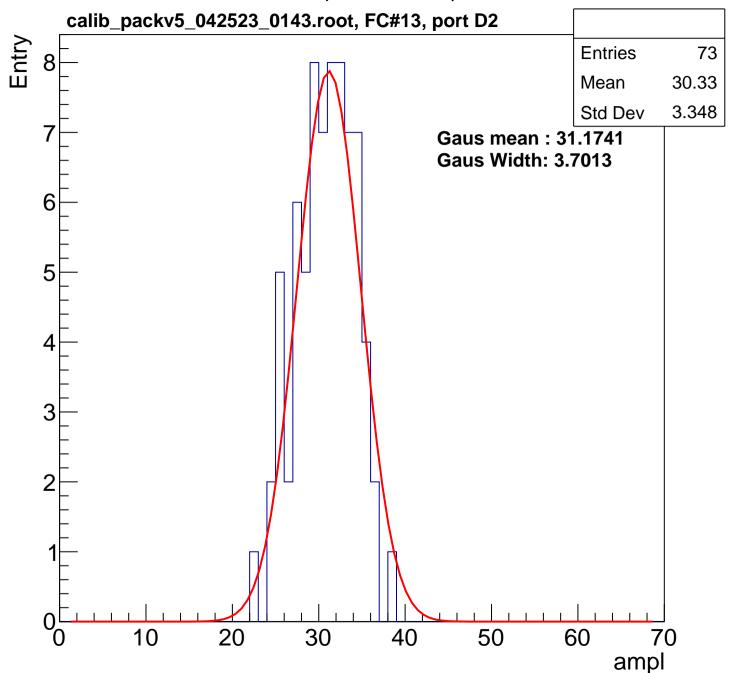


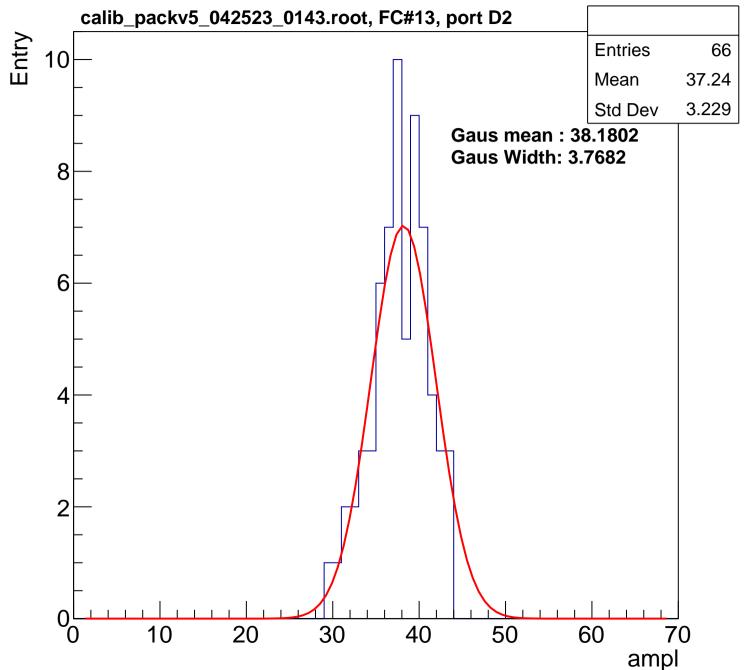


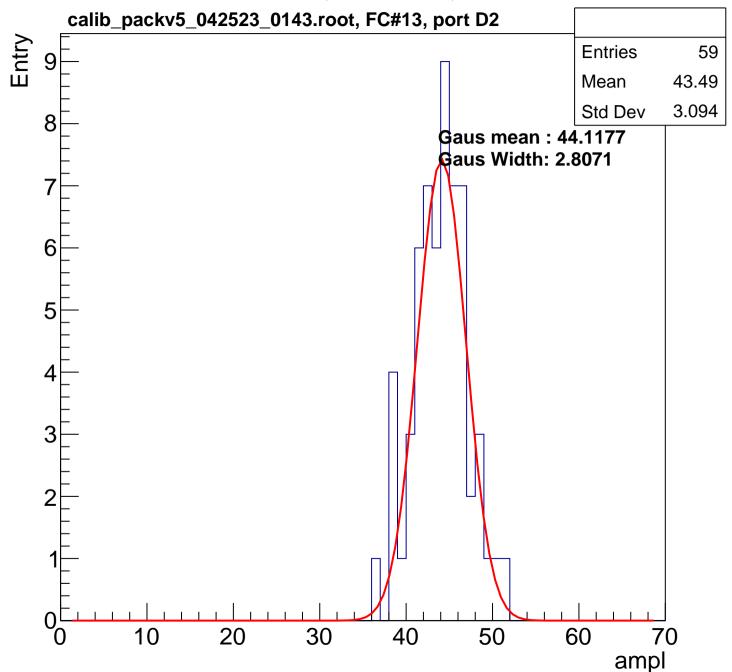


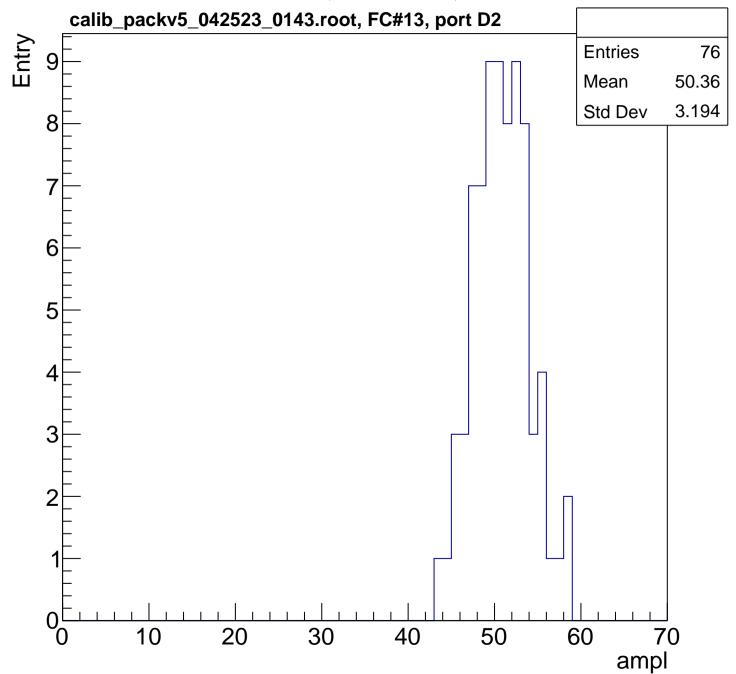


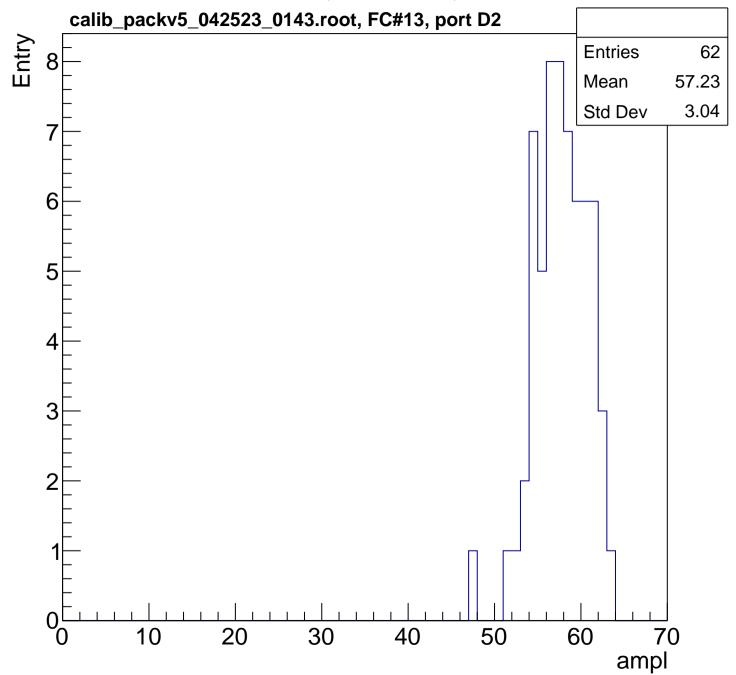


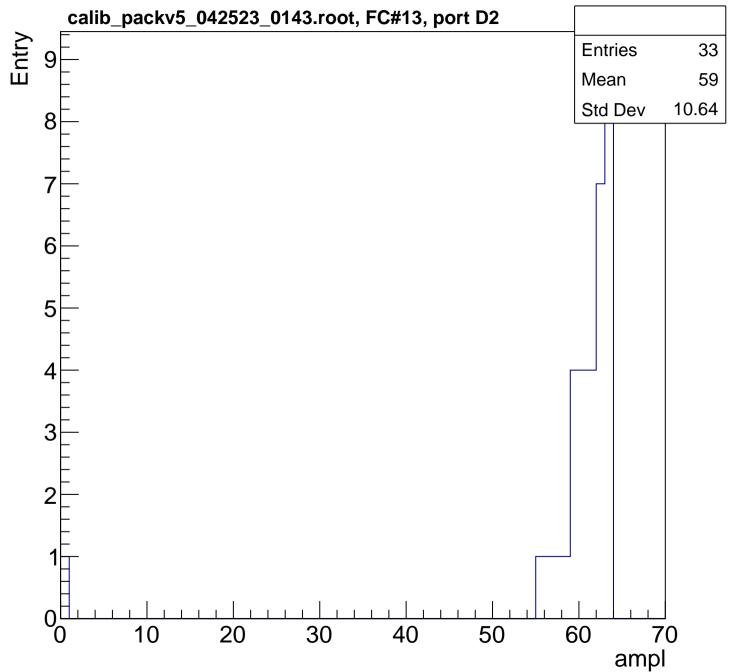


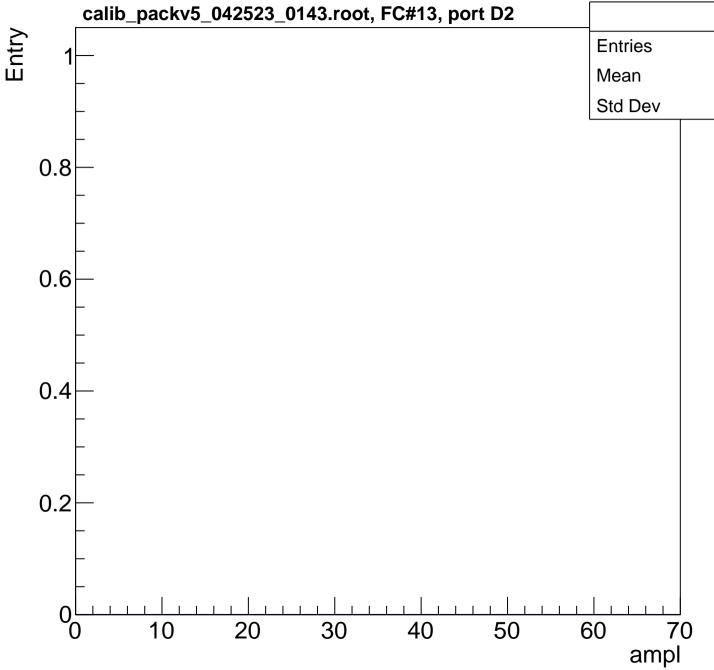




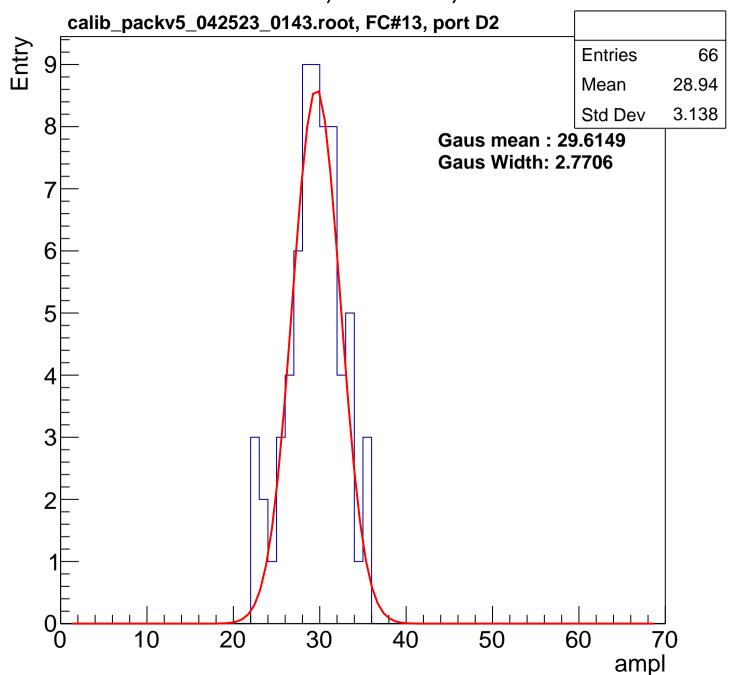


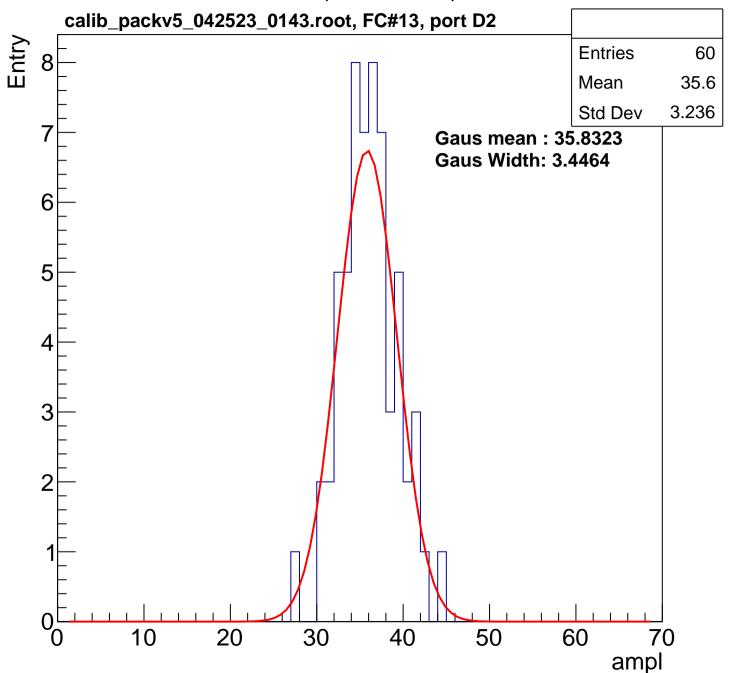


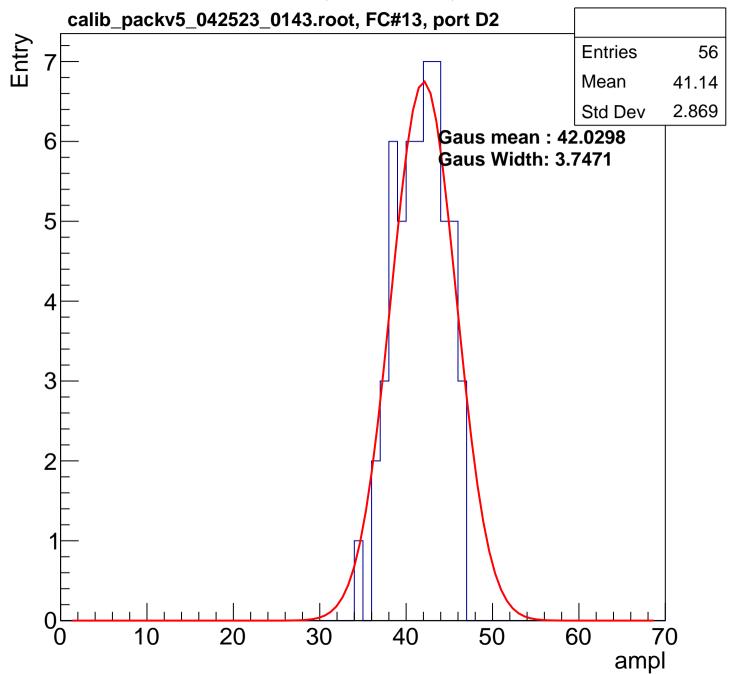


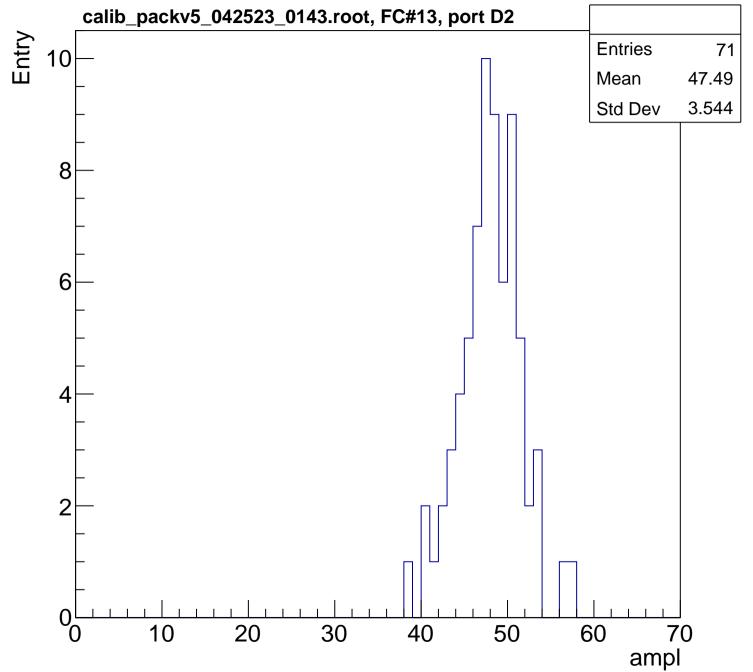


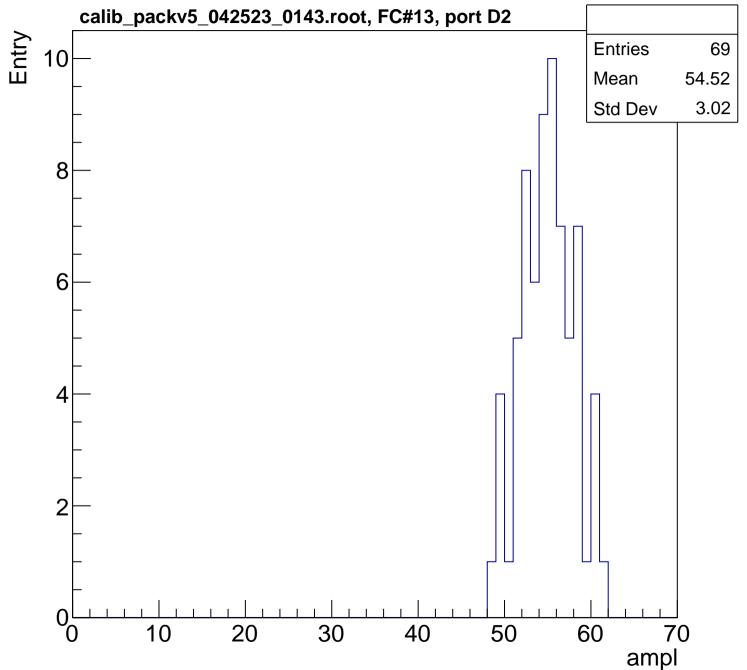
B1L003S, U9-ch7, adc7 calib\_packv5\_042523\_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

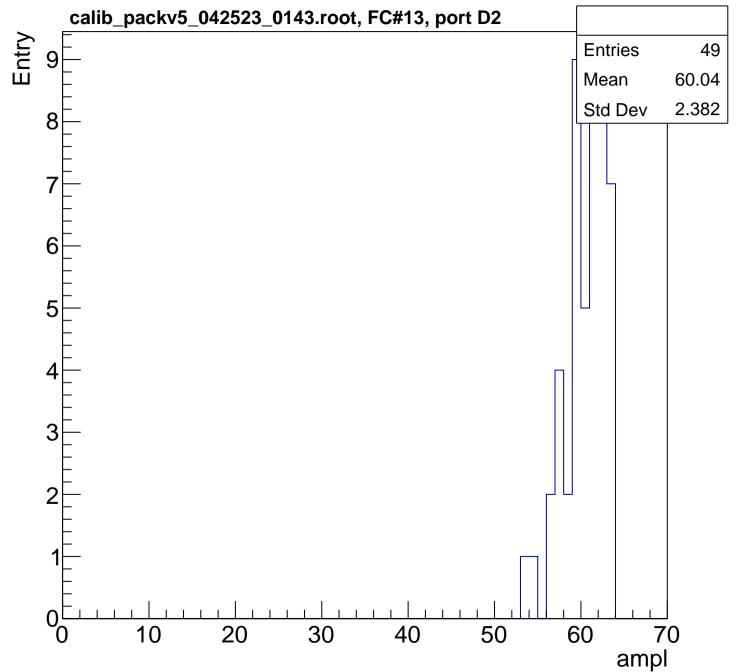


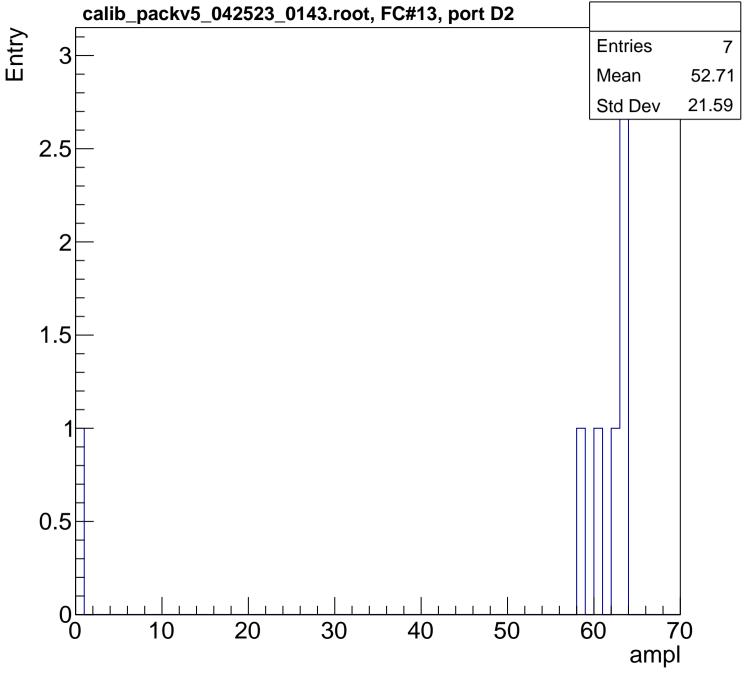


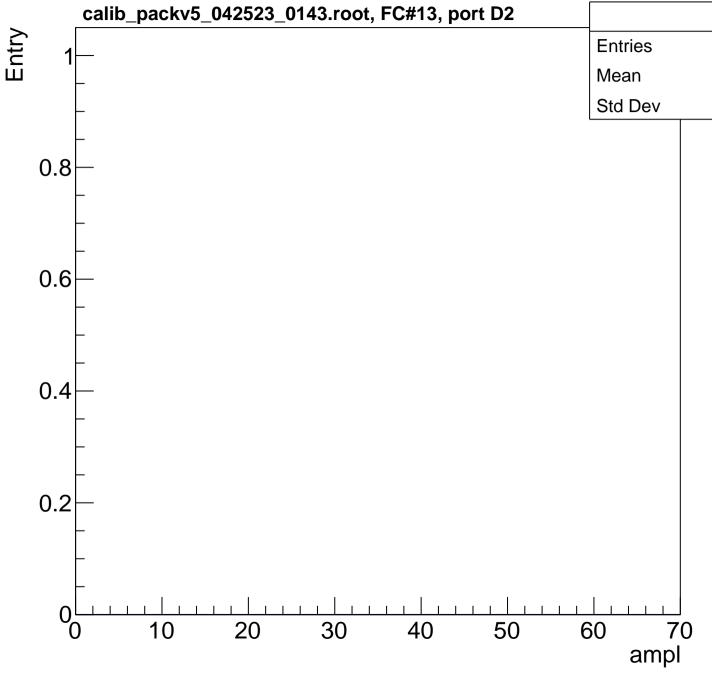


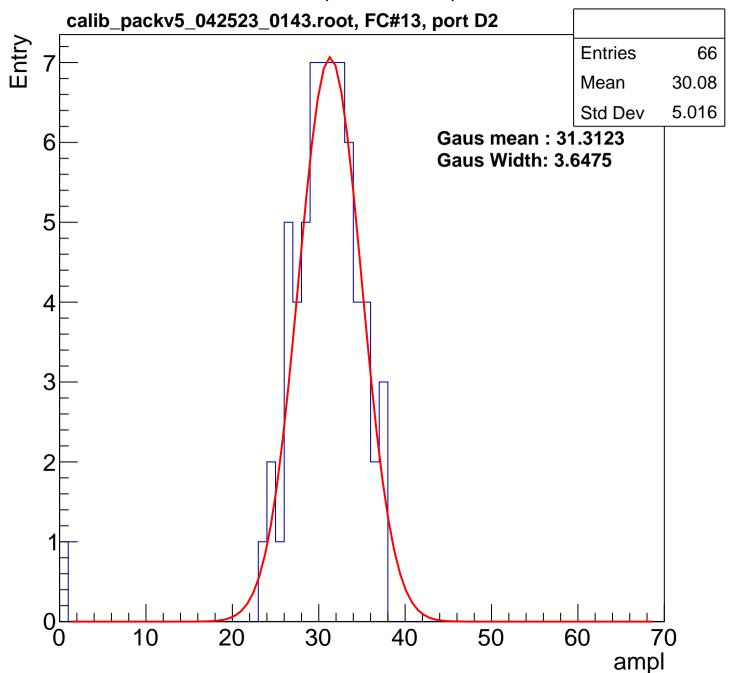


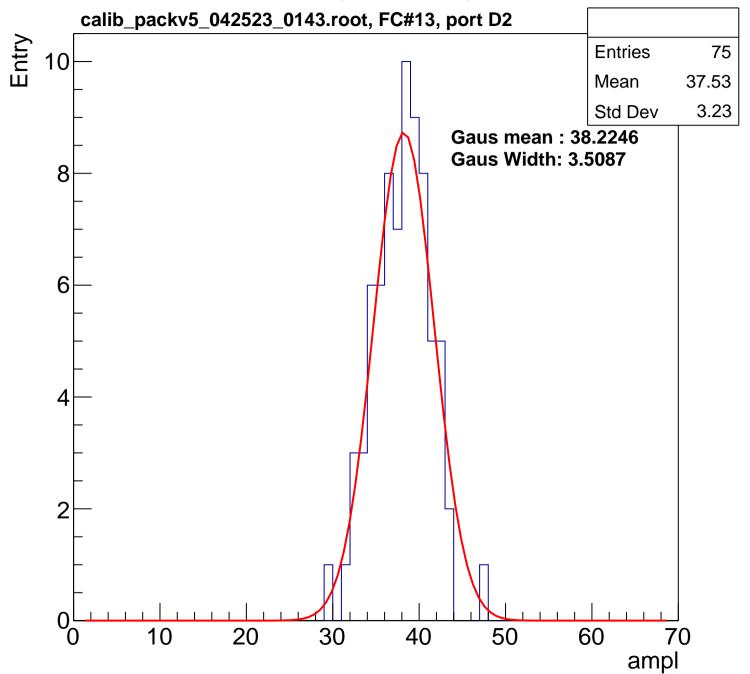


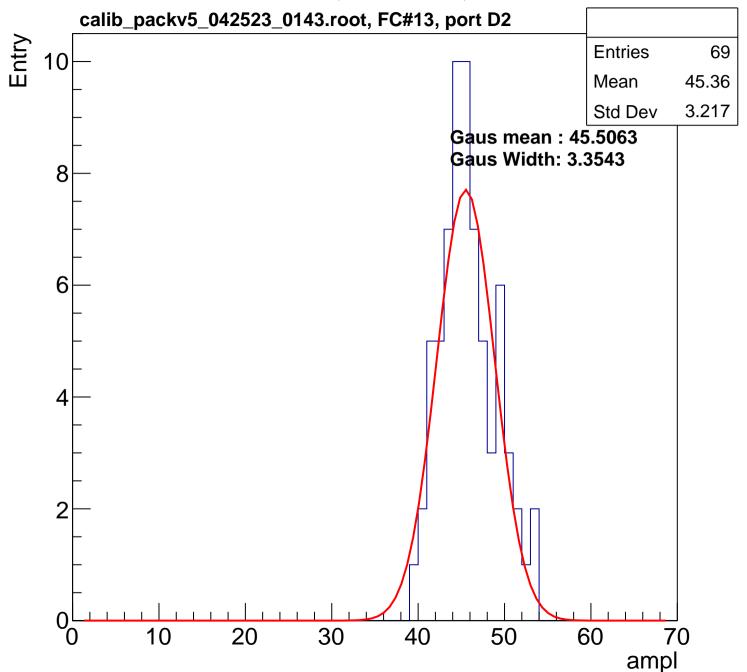


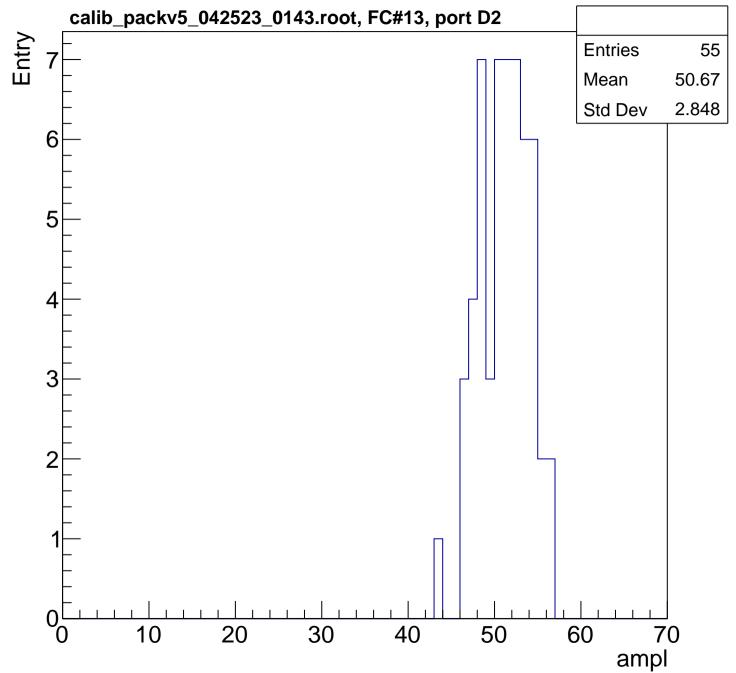


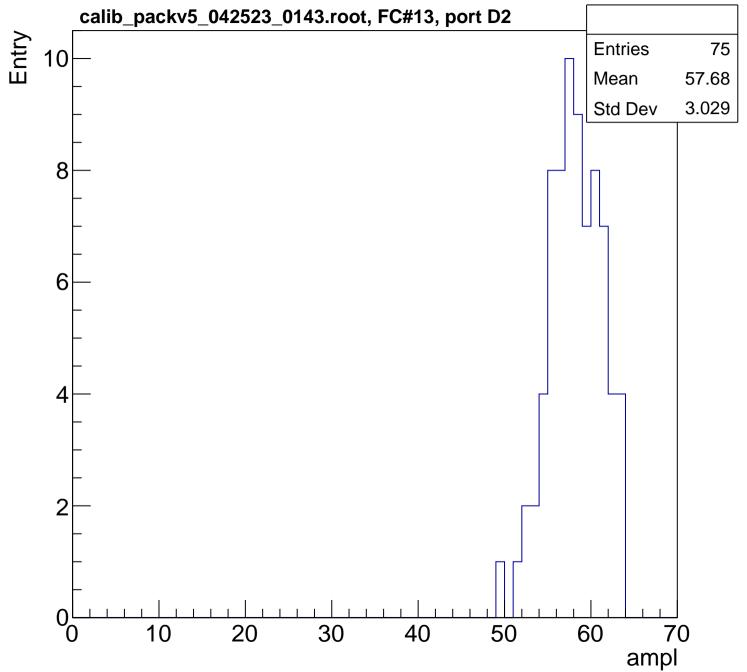


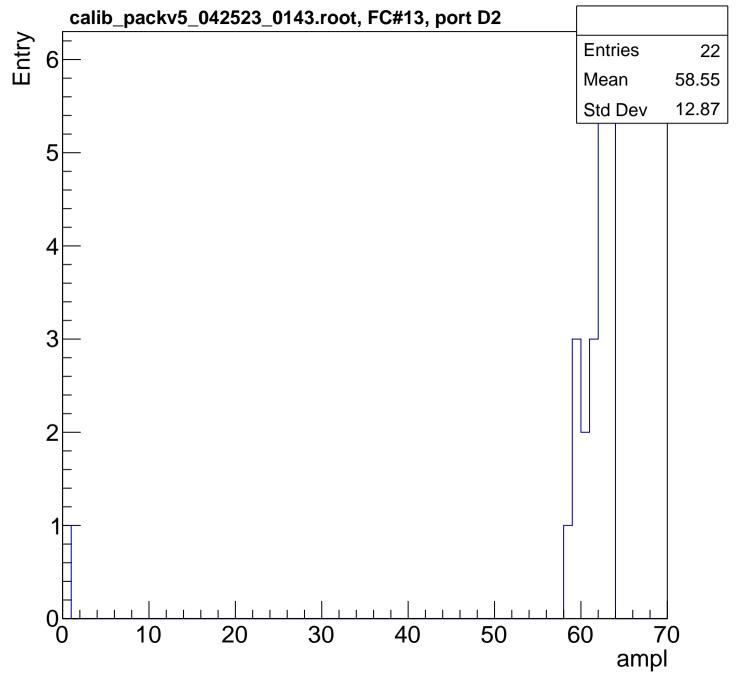


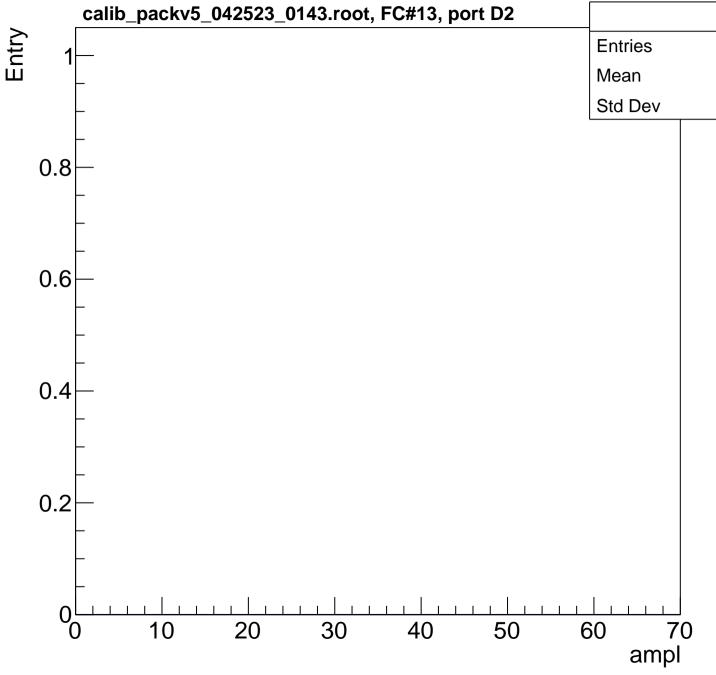


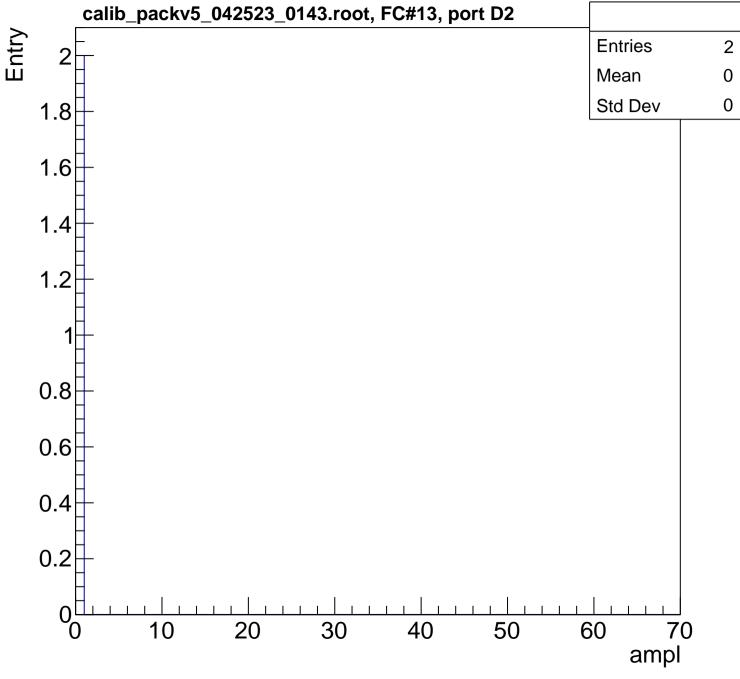


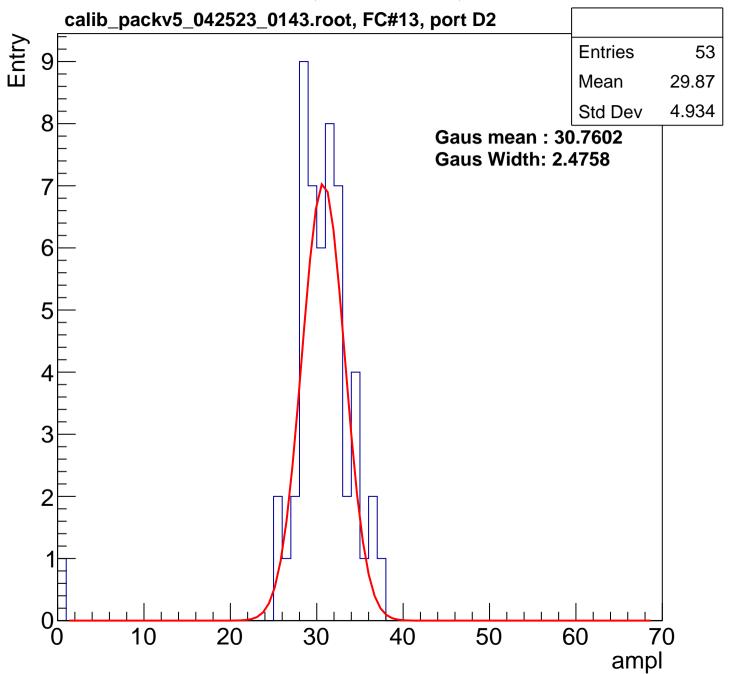


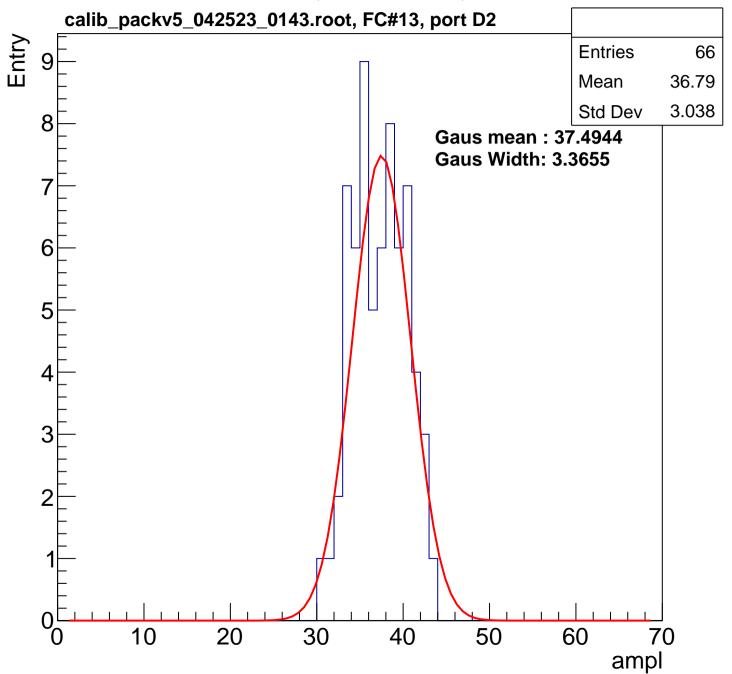


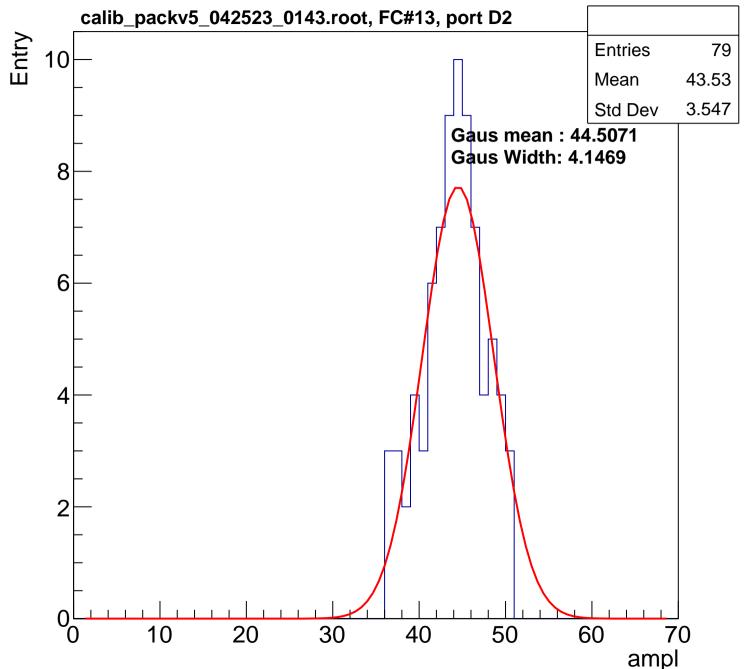


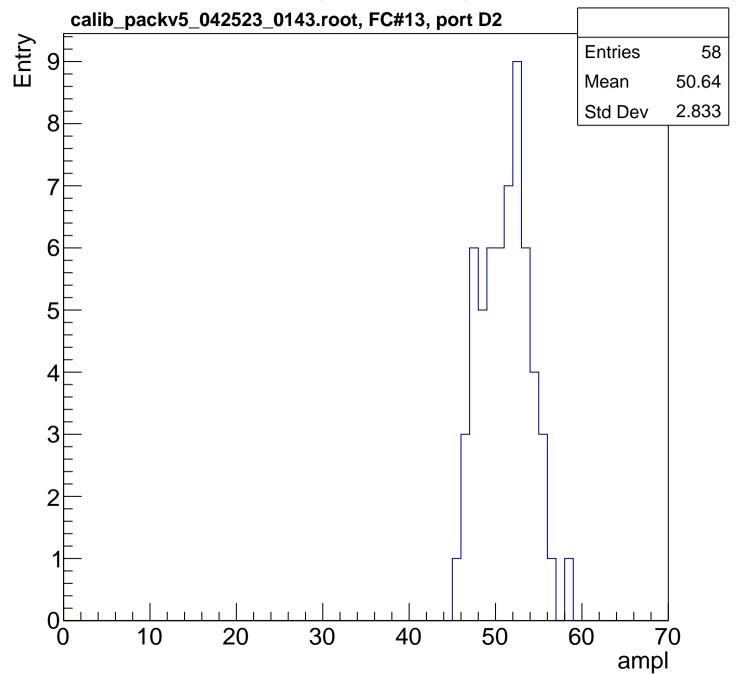


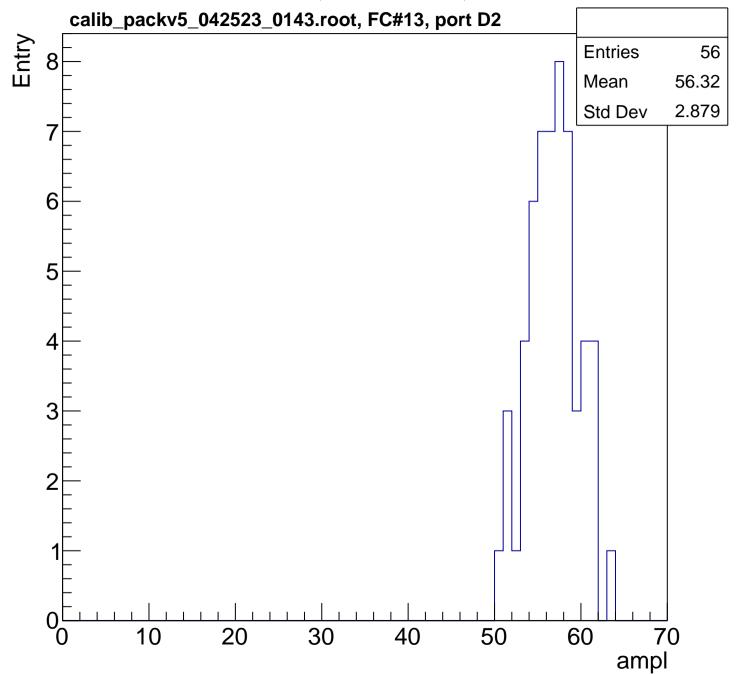


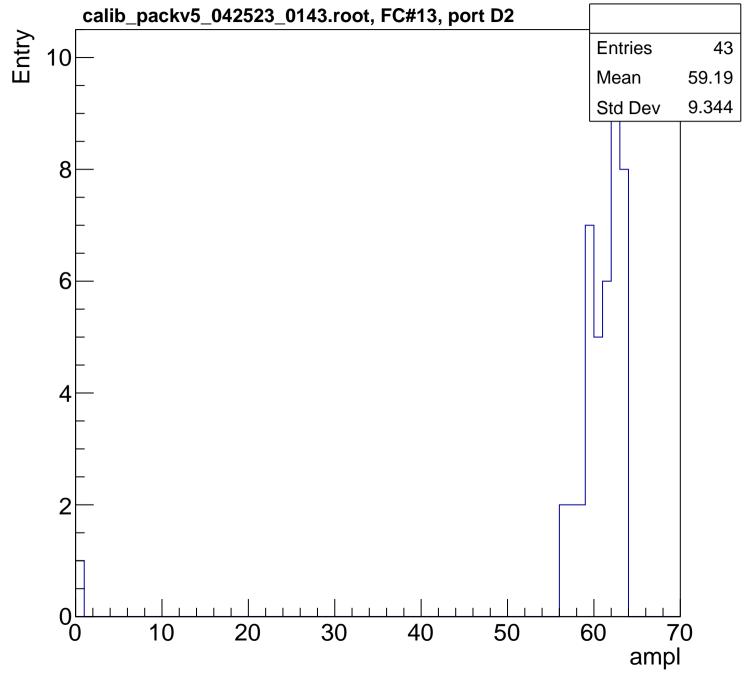


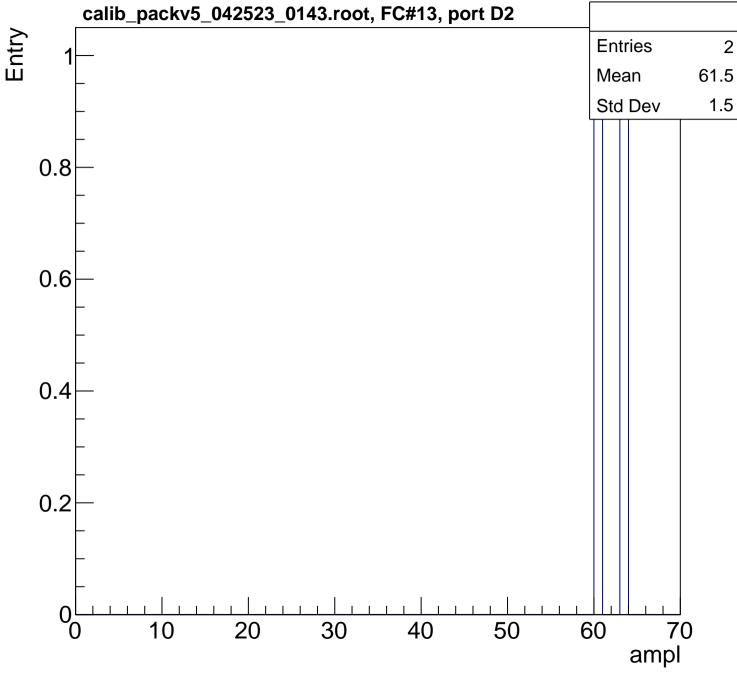




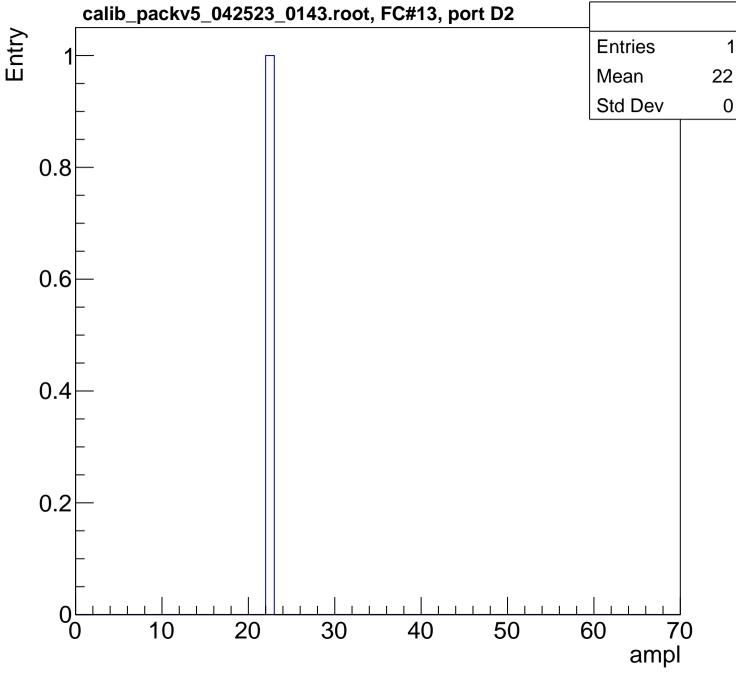


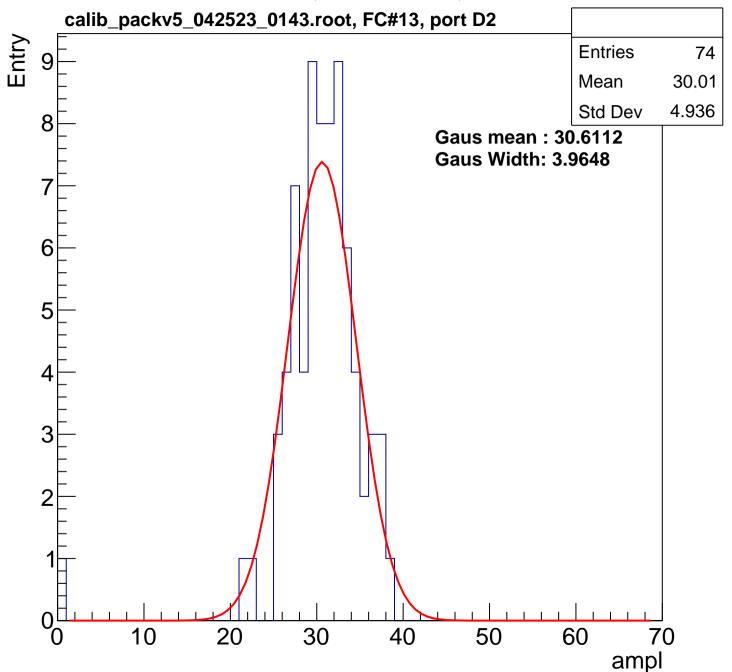


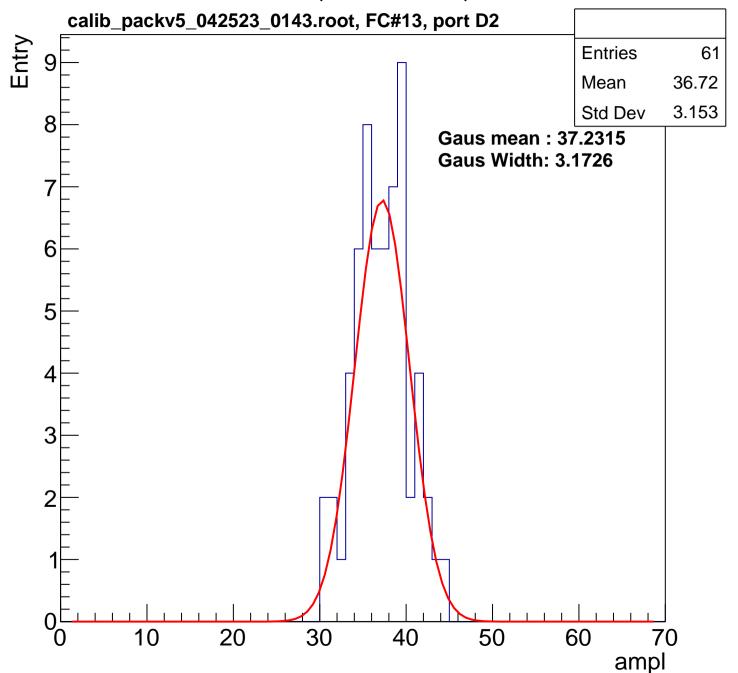


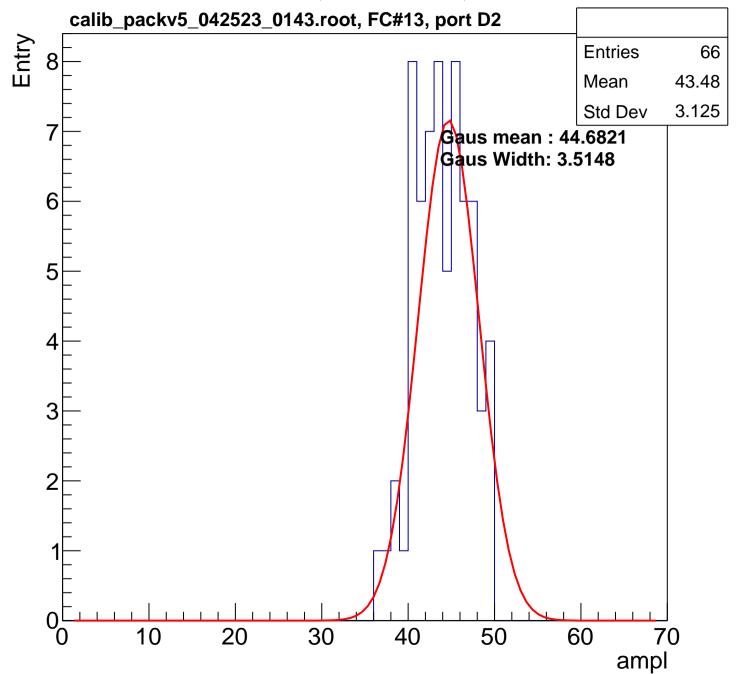


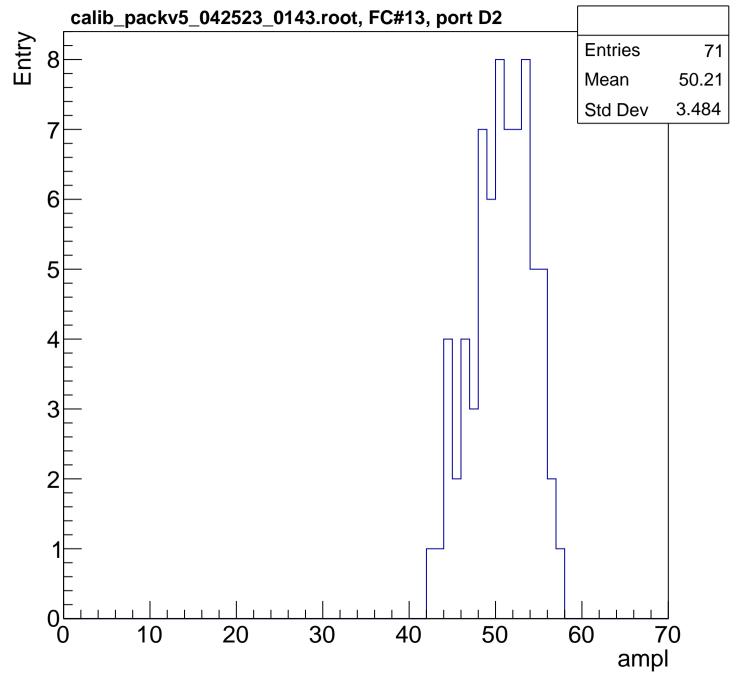
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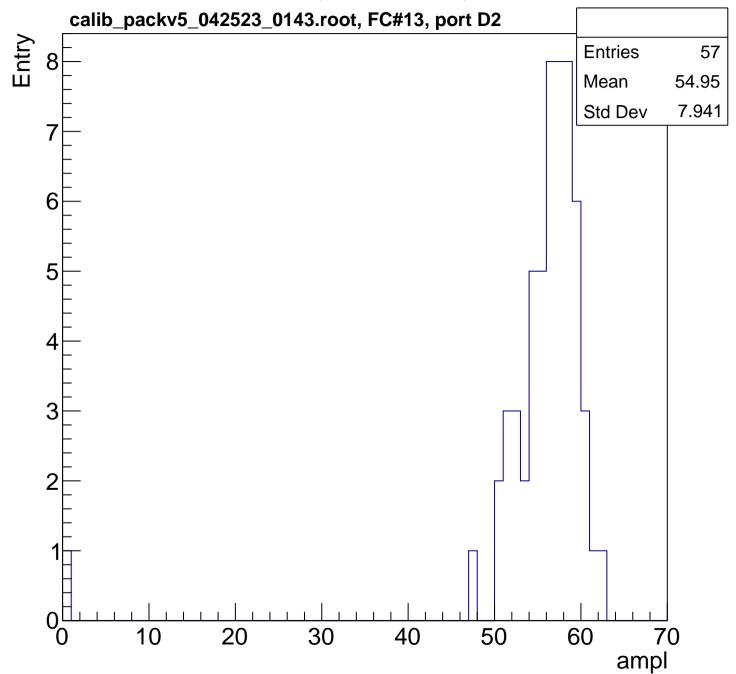


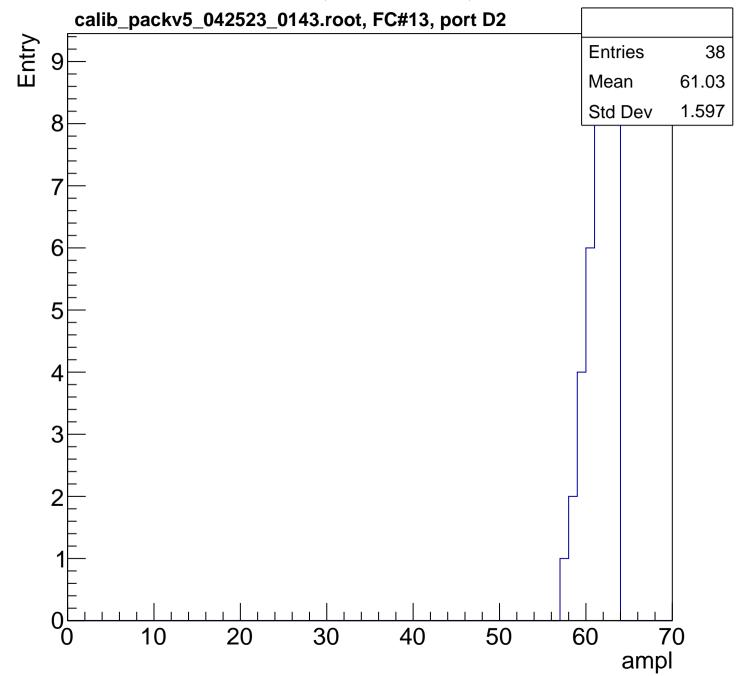


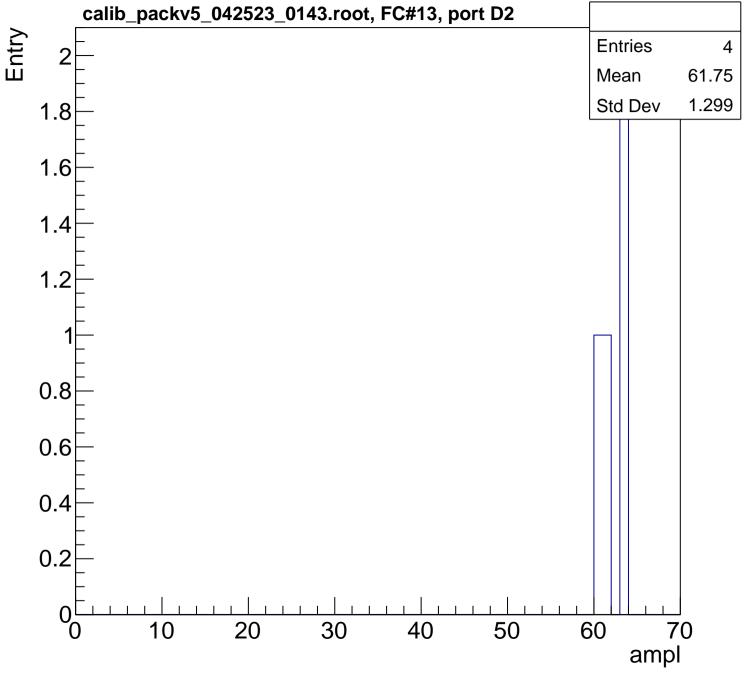


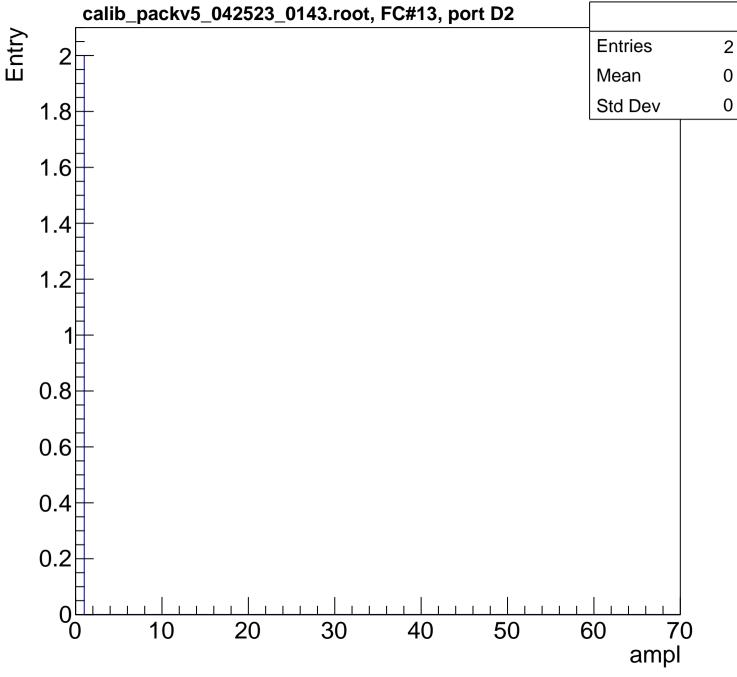


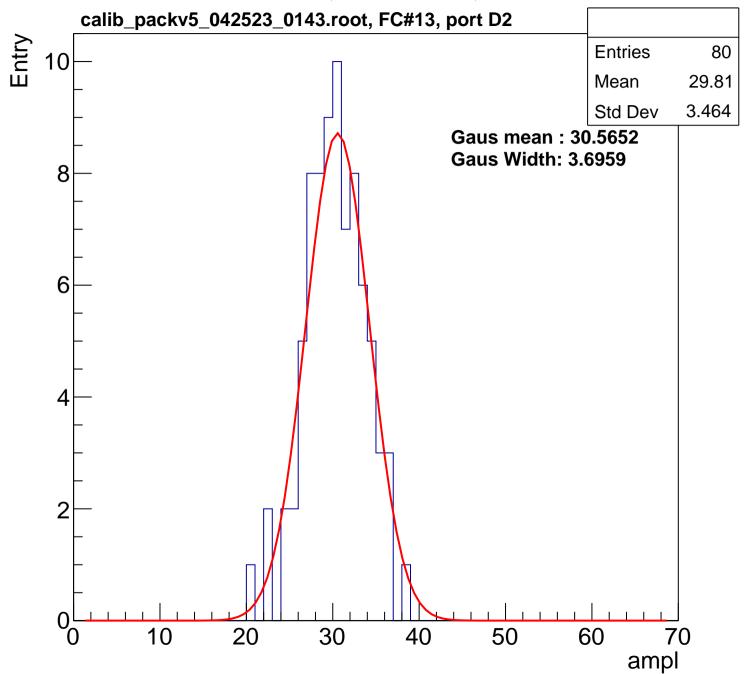


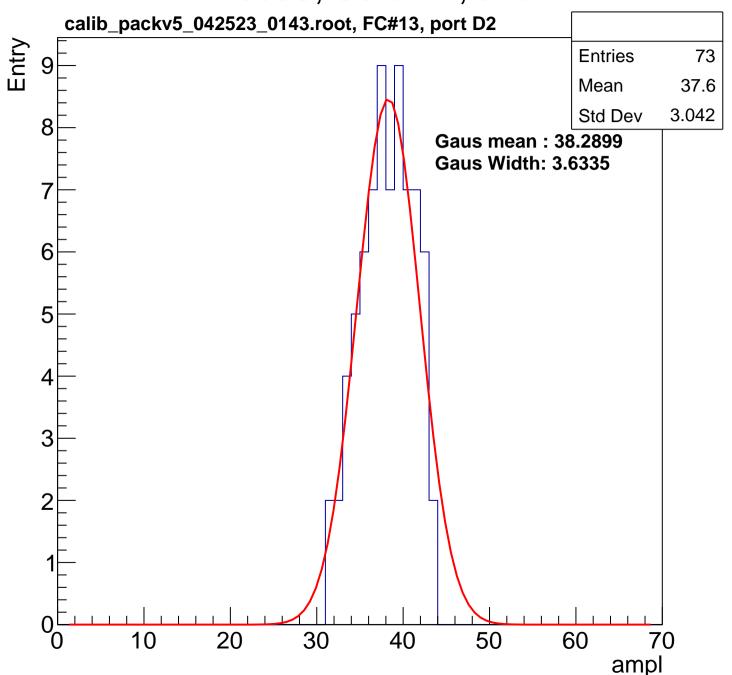


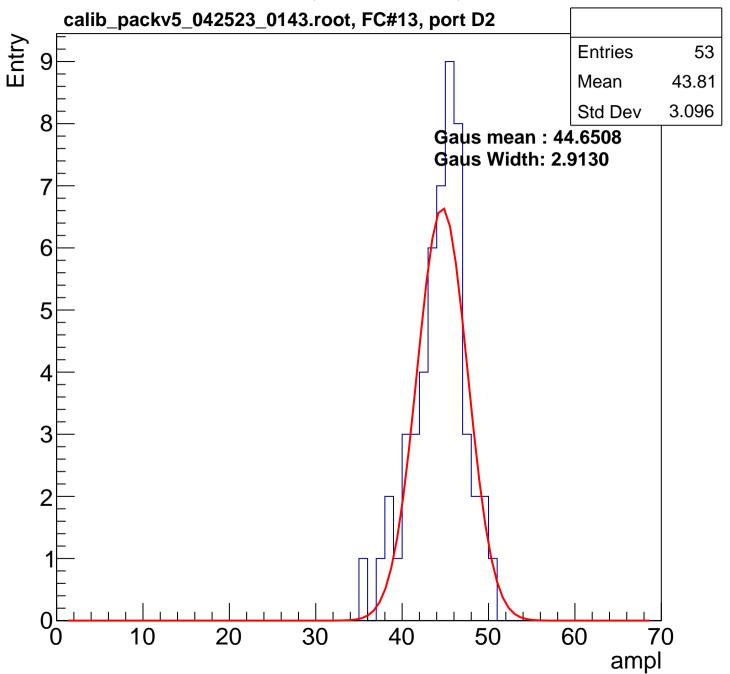


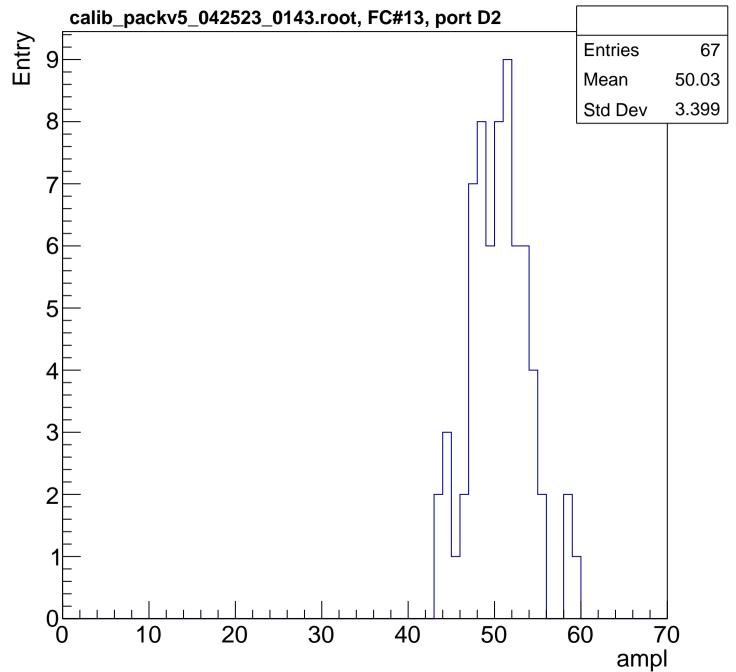


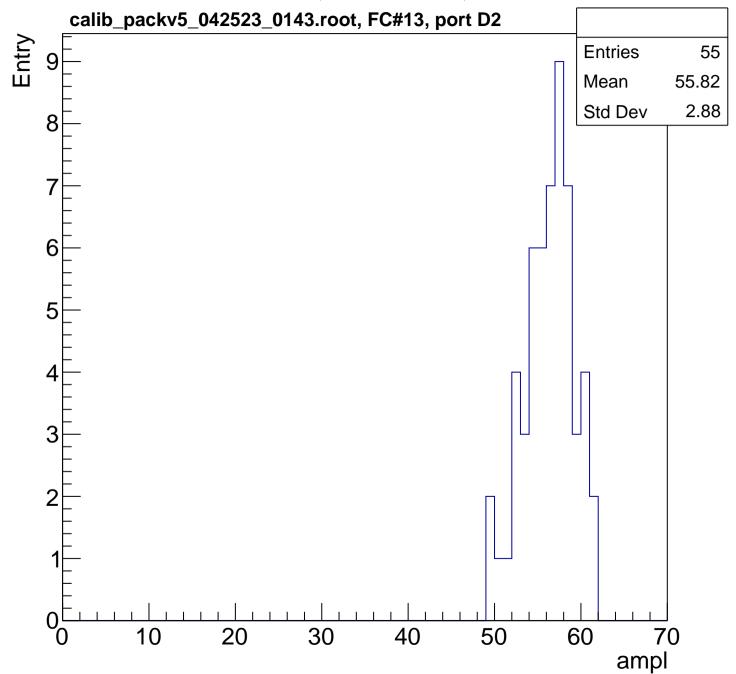


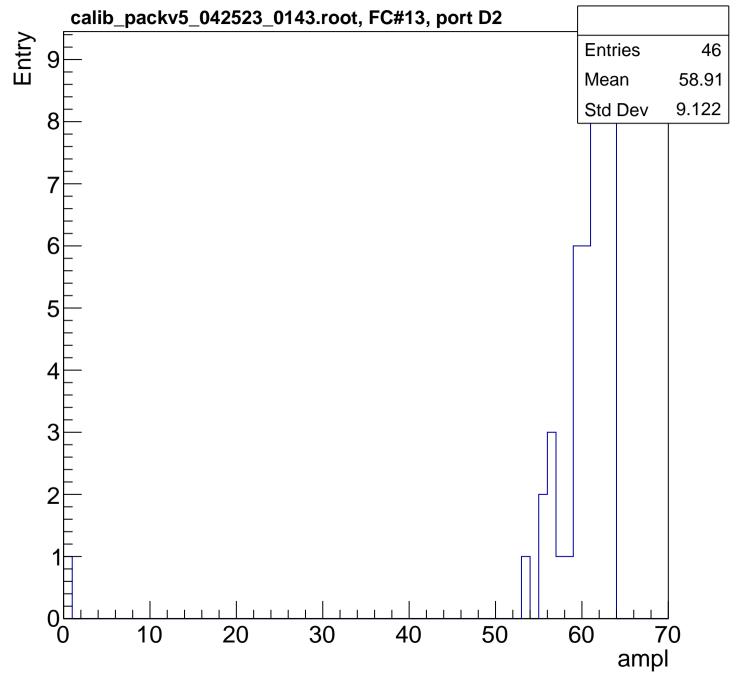


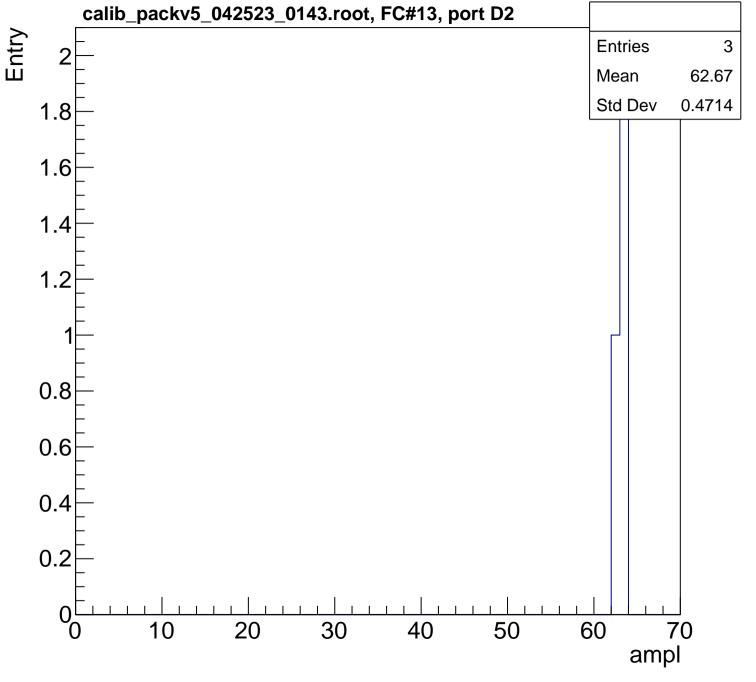




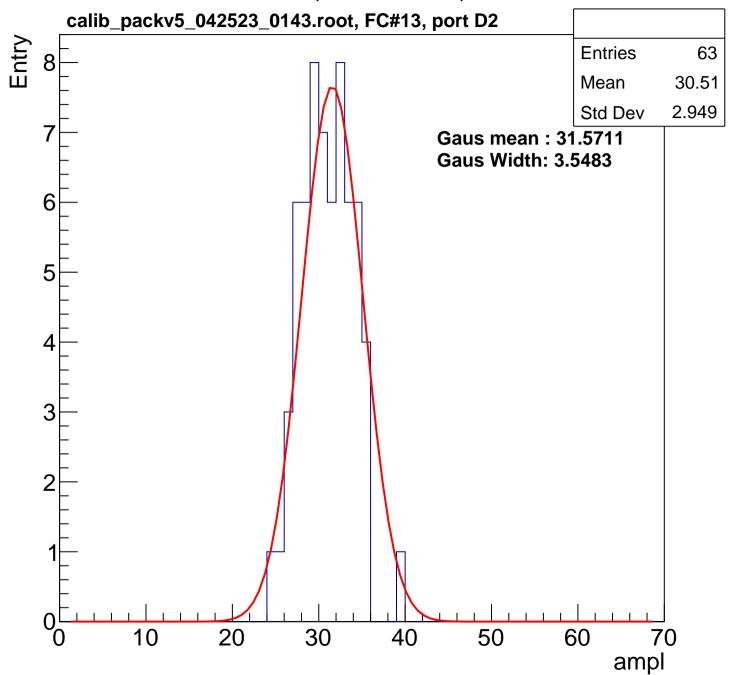


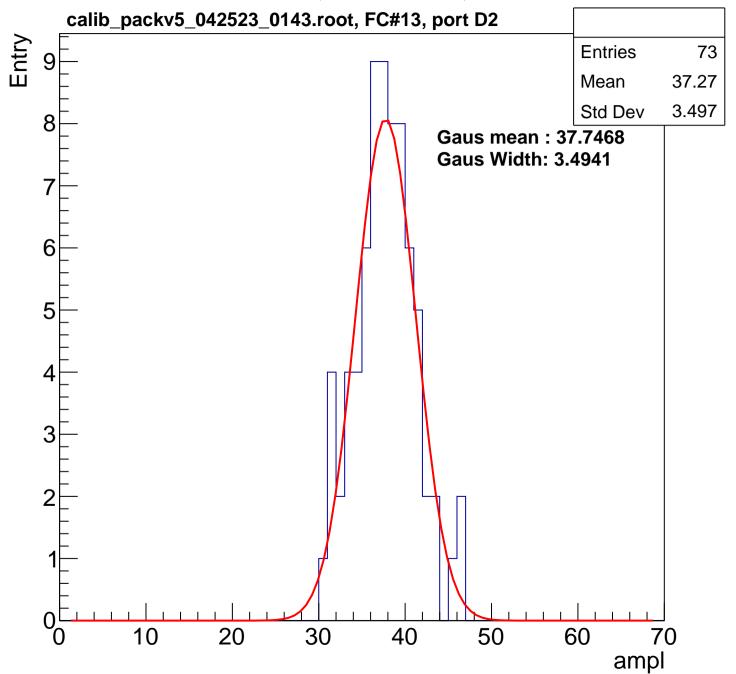


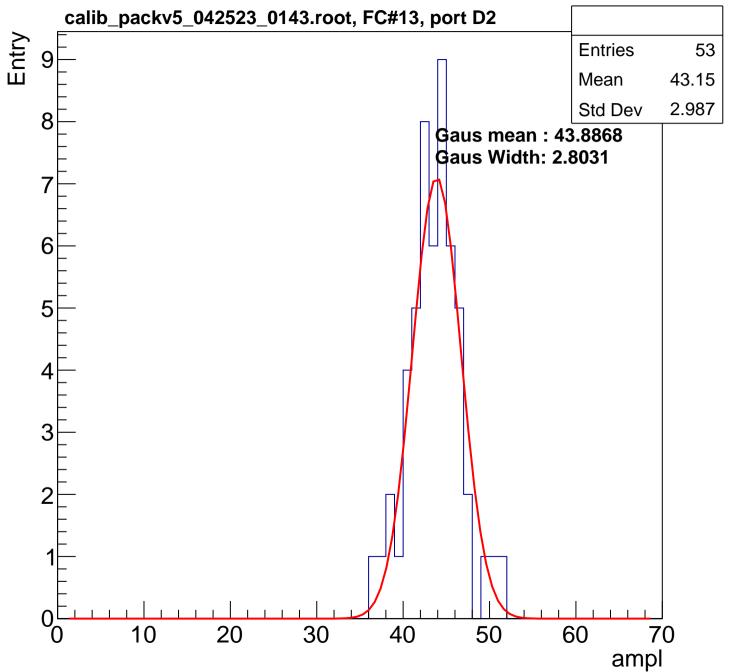


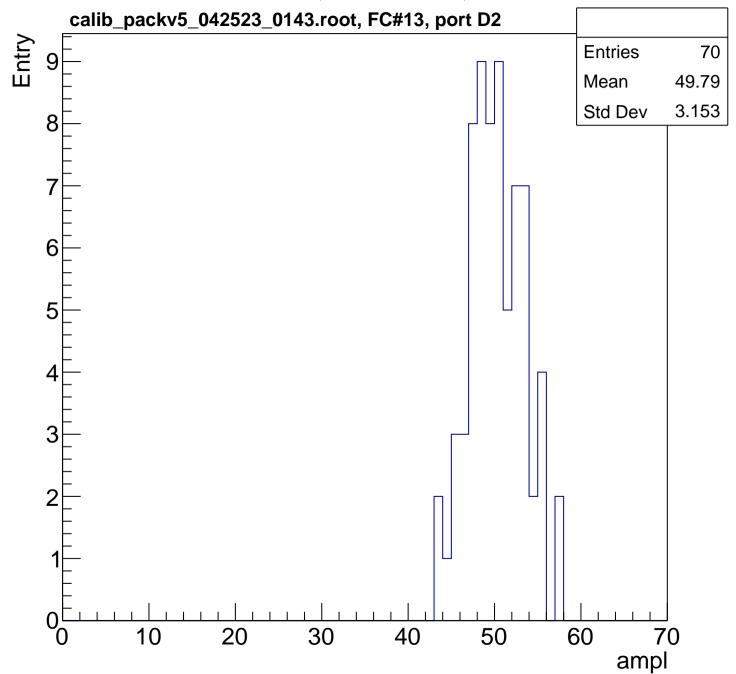


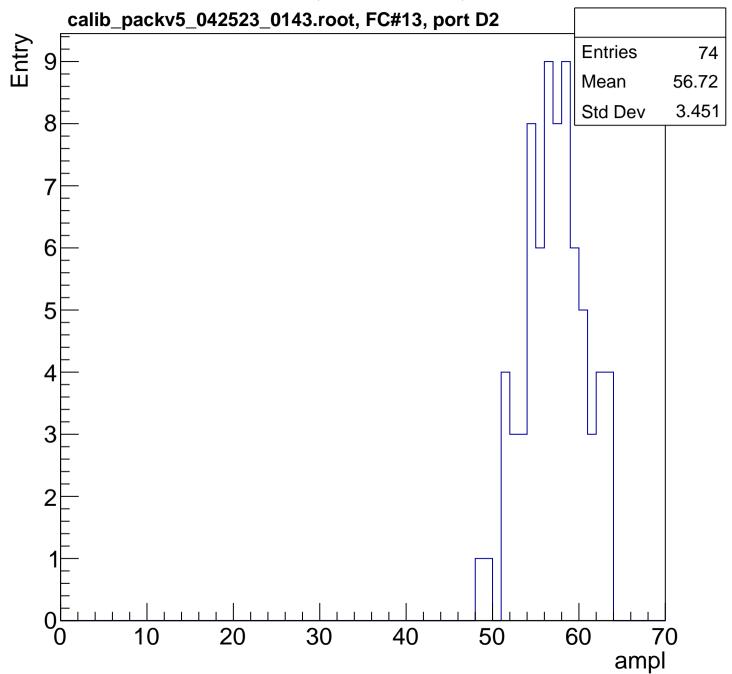
B1L003S, U9-ch12, adc7 calib\_packv5\_042523\_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

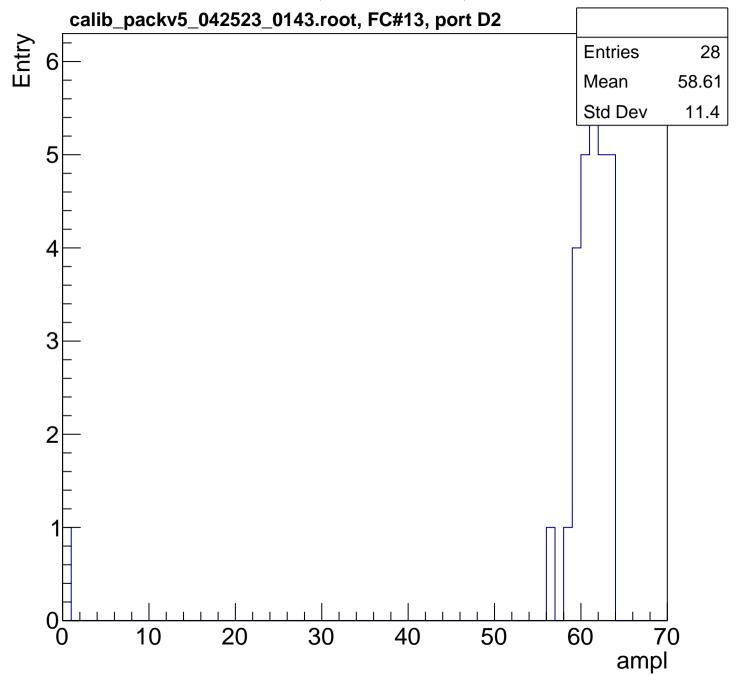


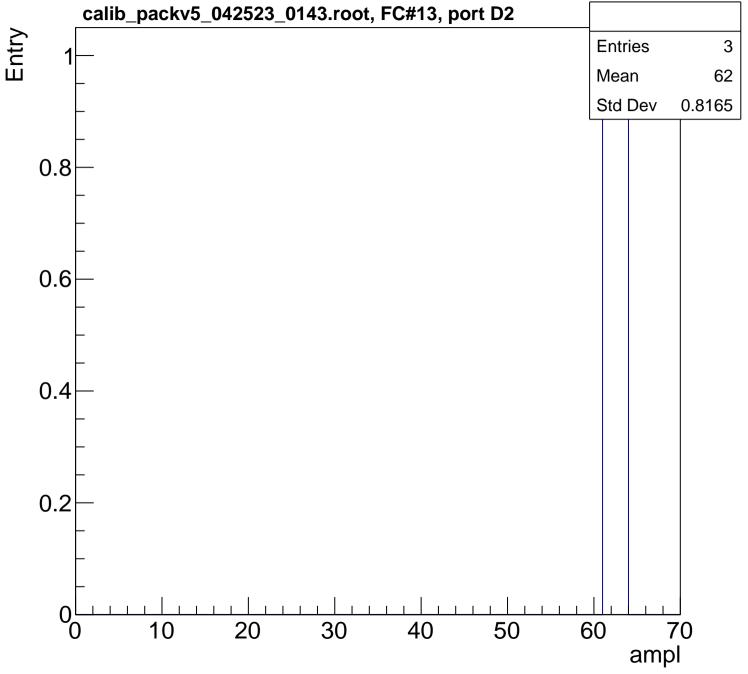


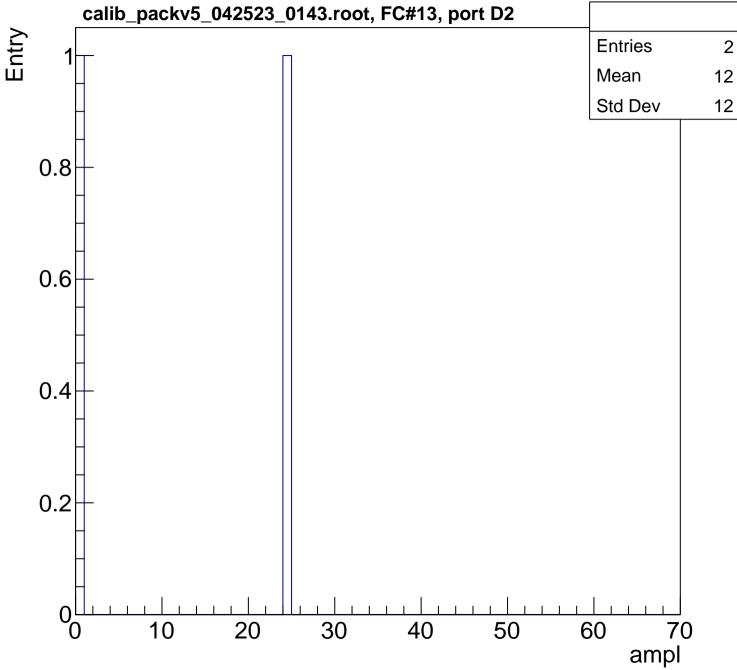


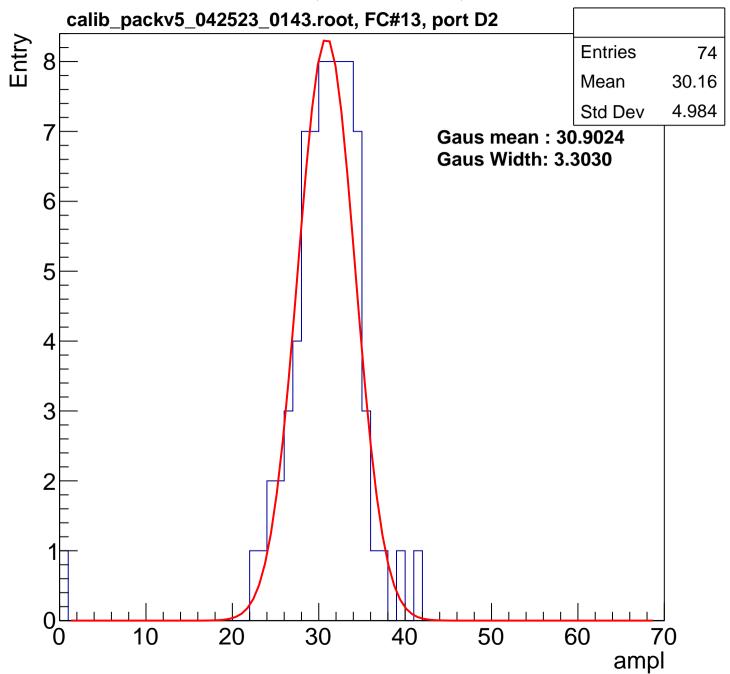


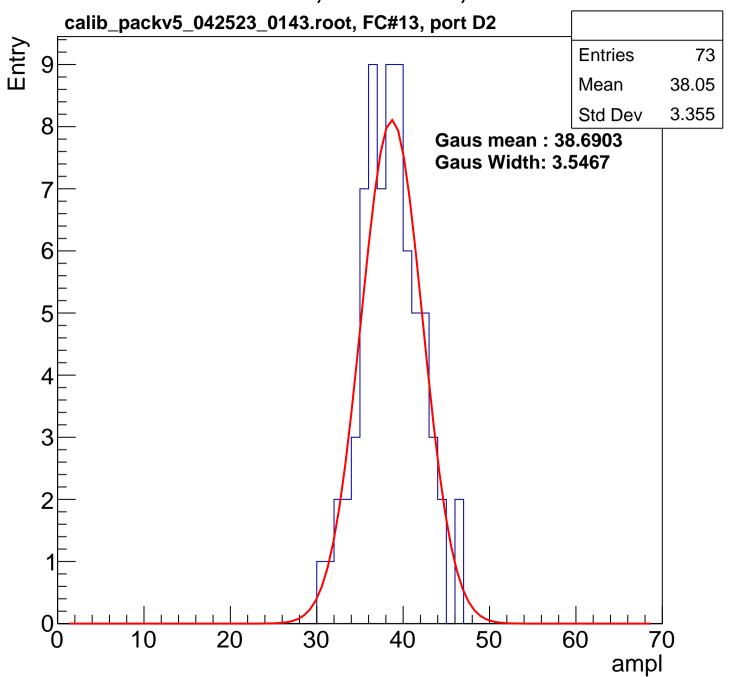


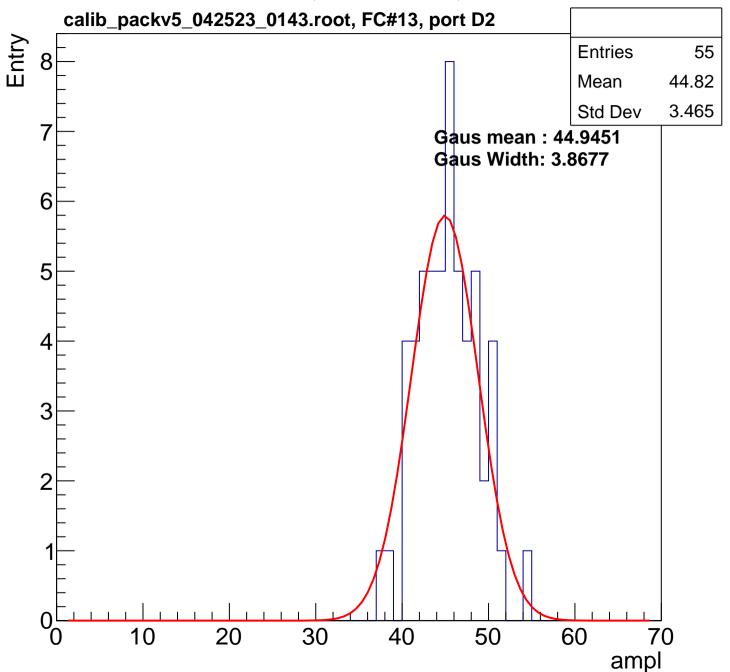


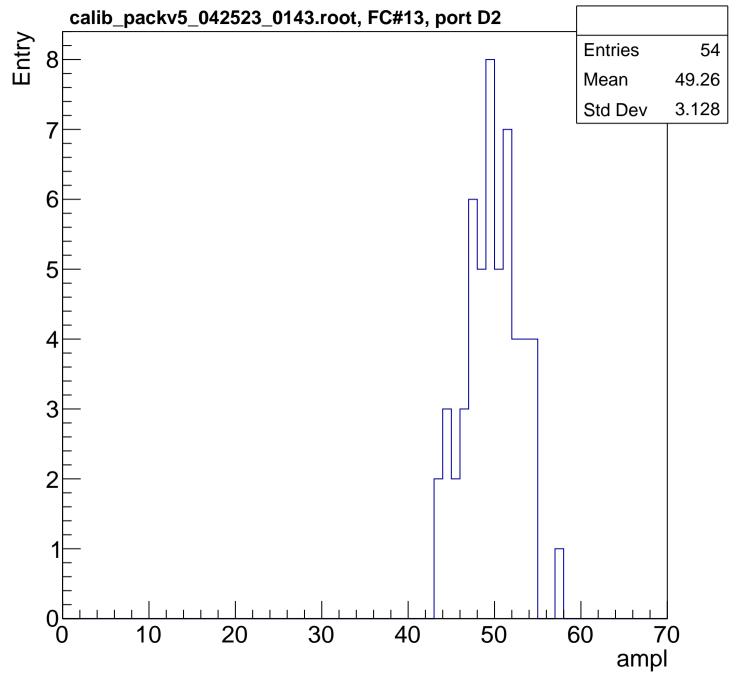


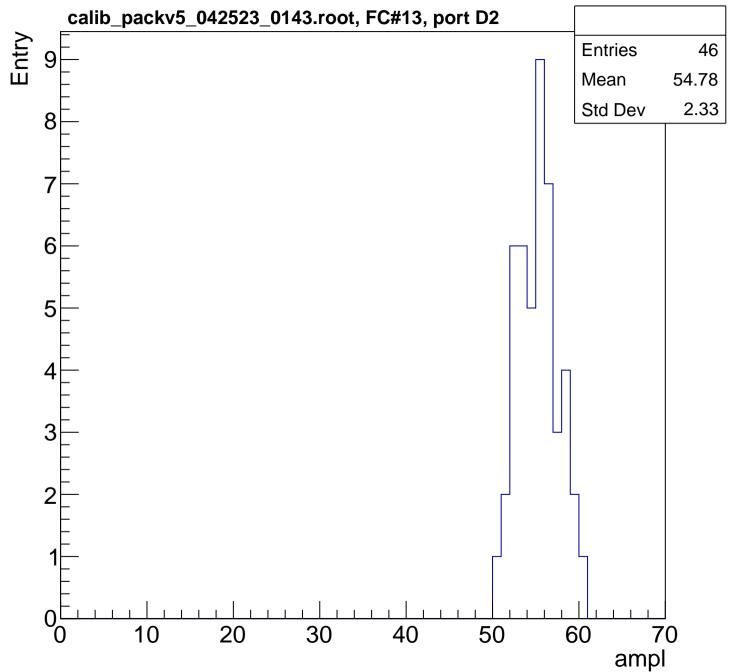


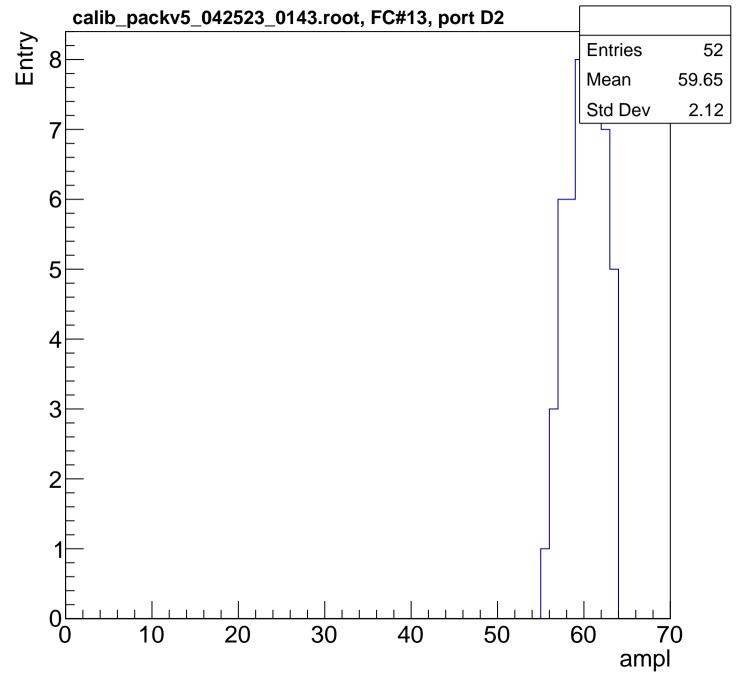


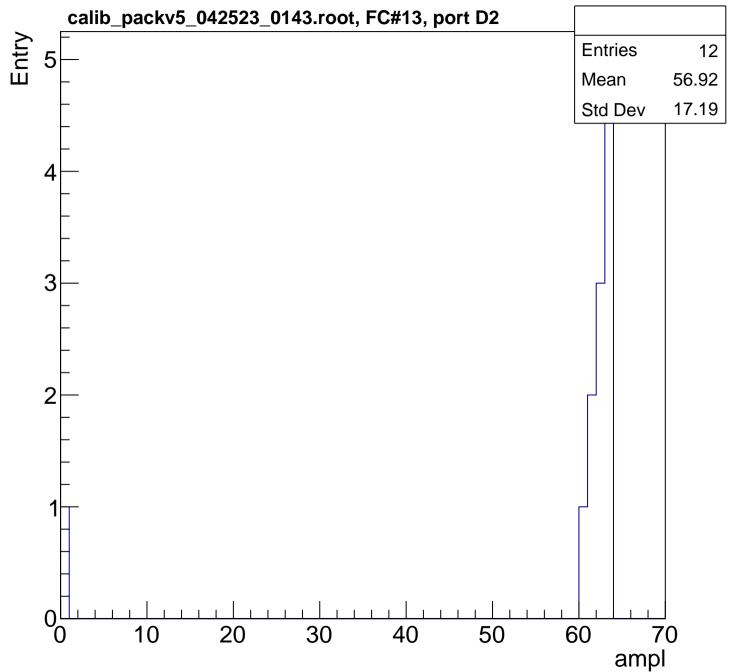




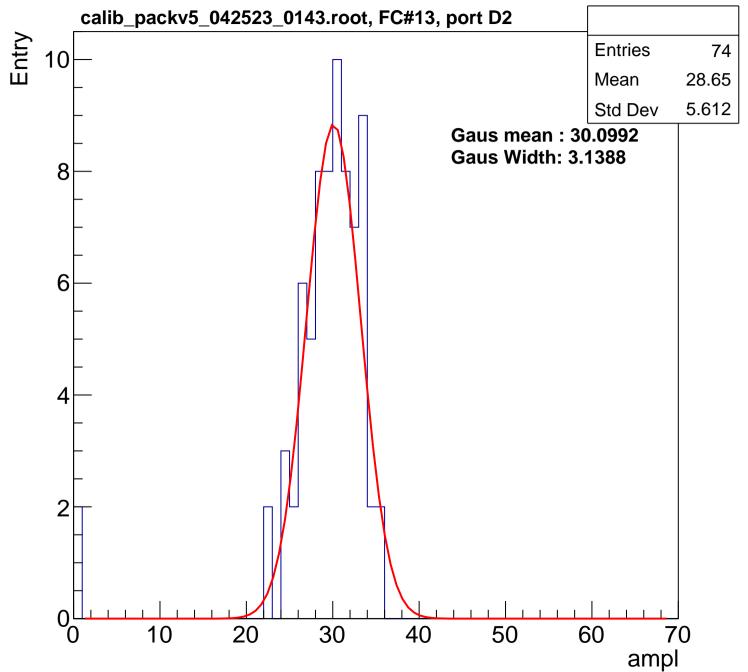


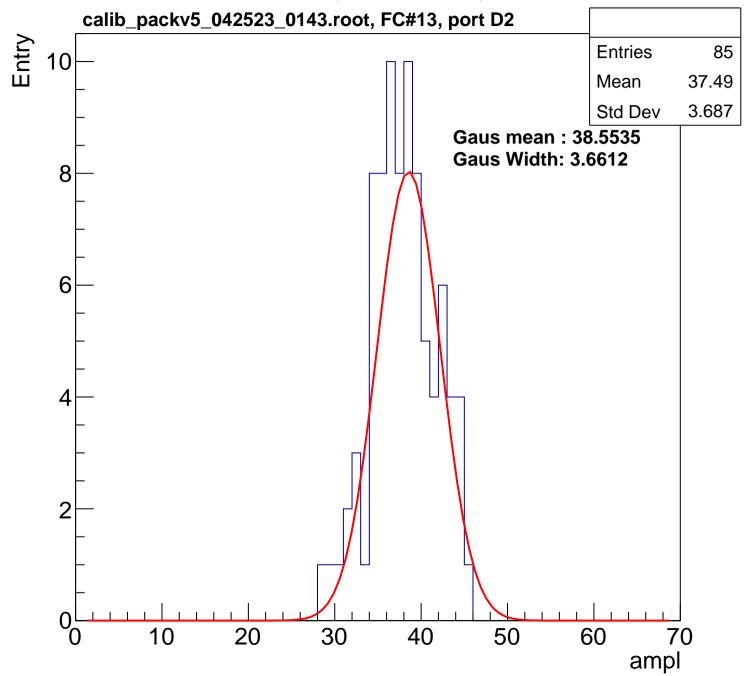


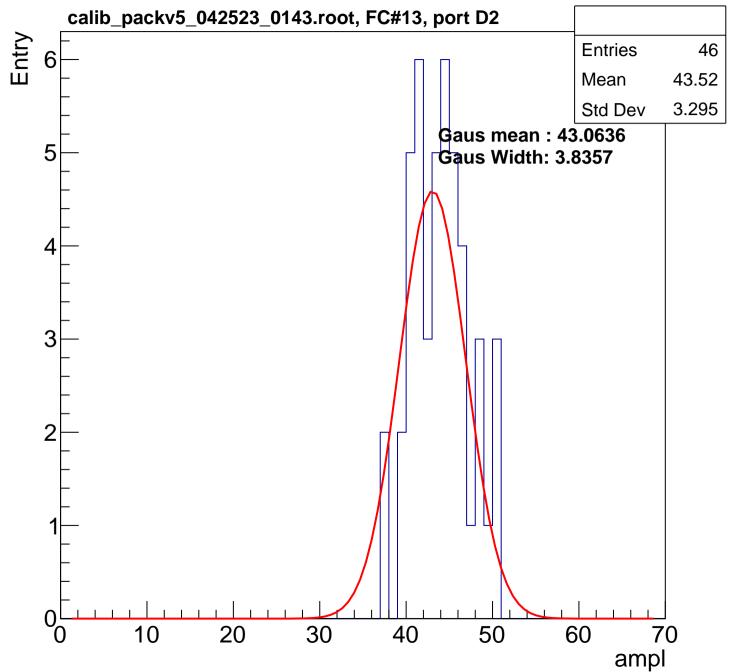


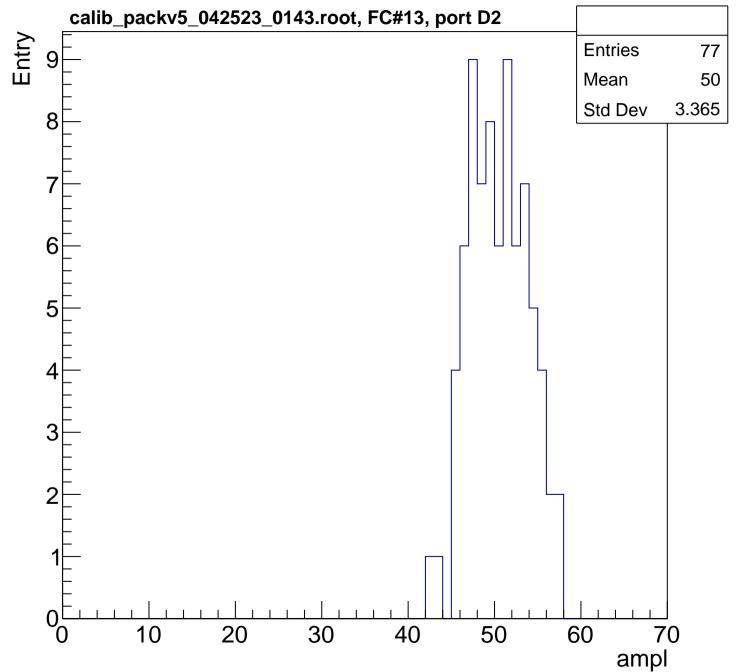


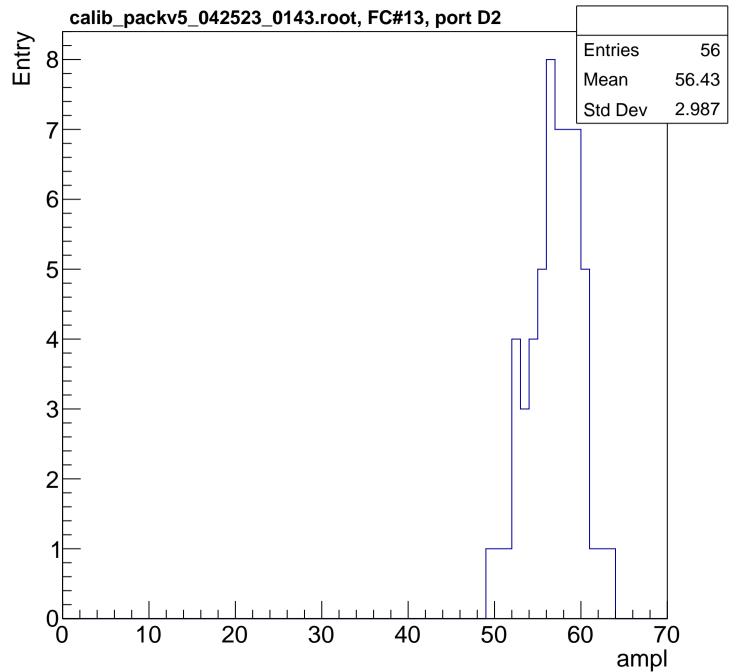
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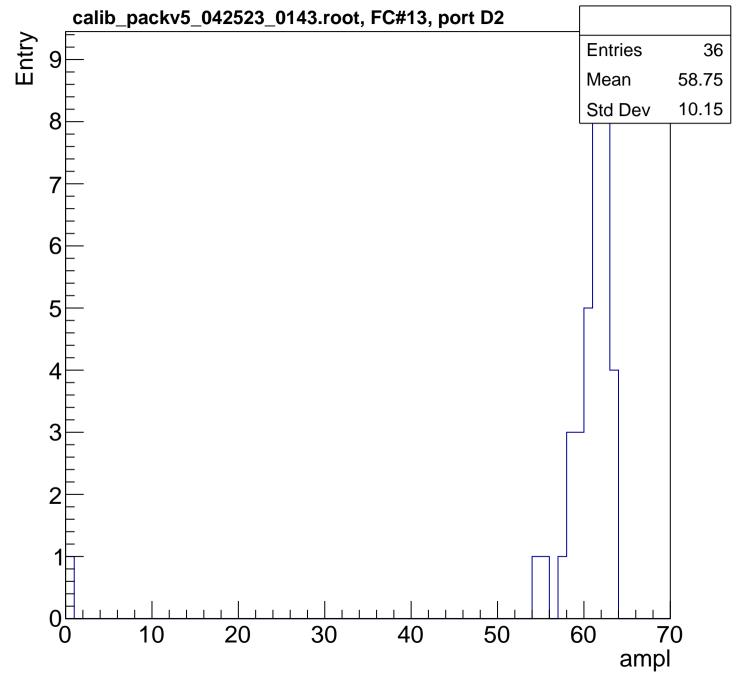


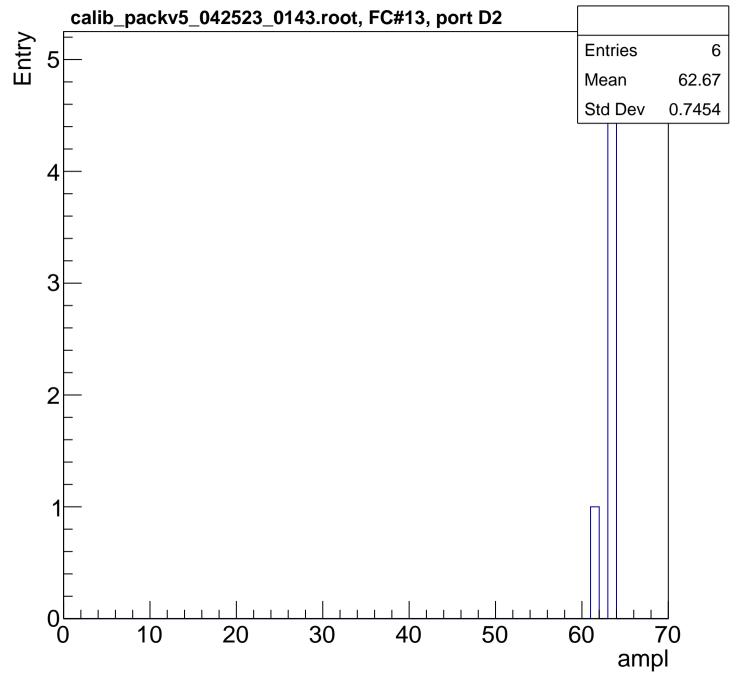




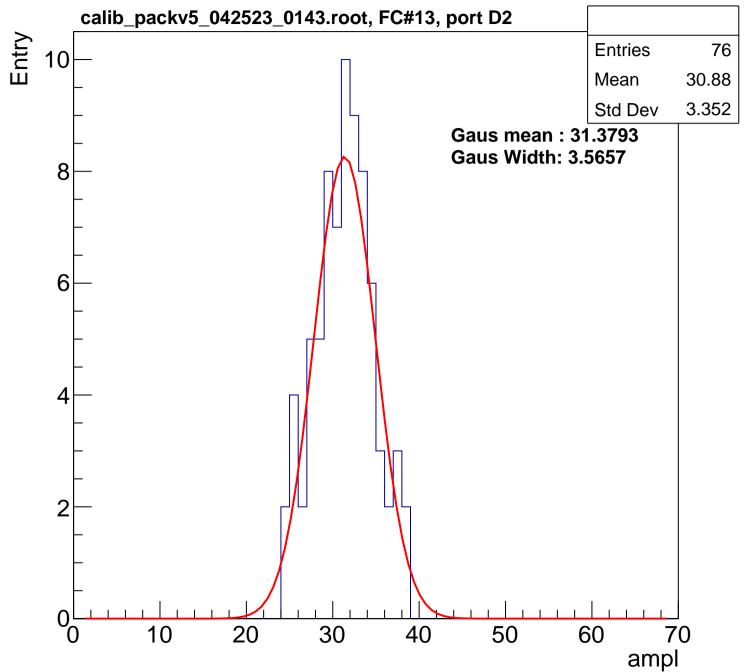


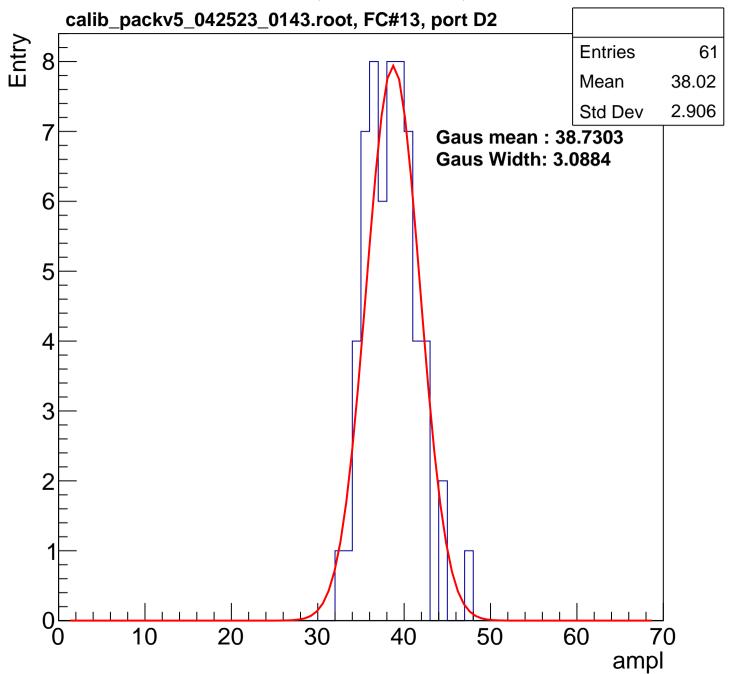


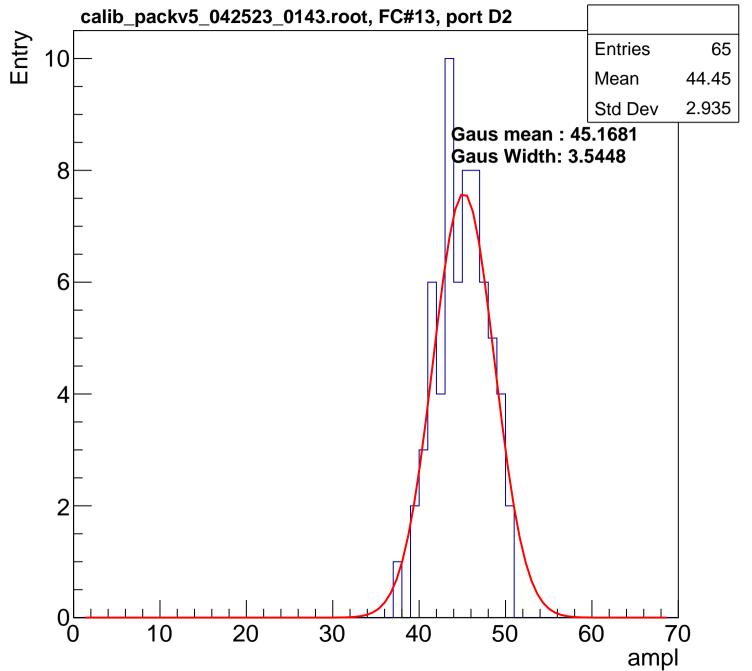


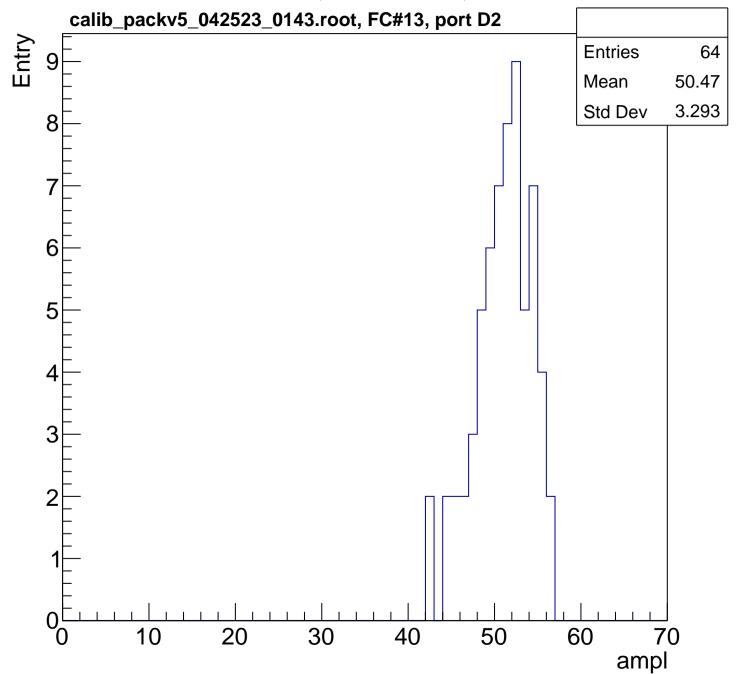


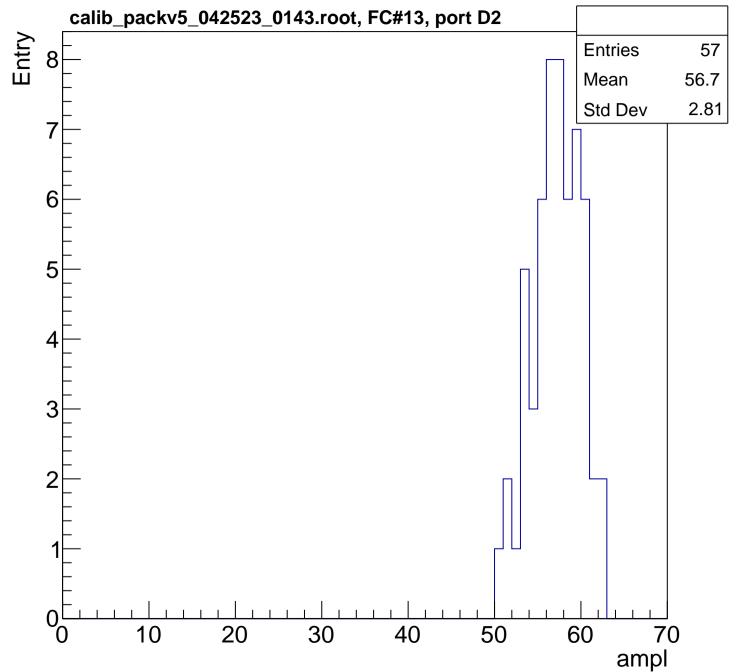


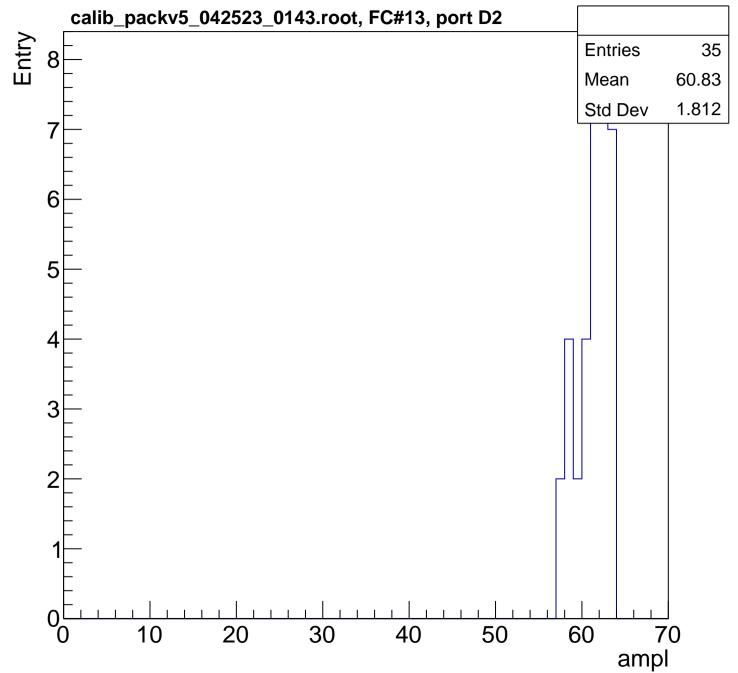


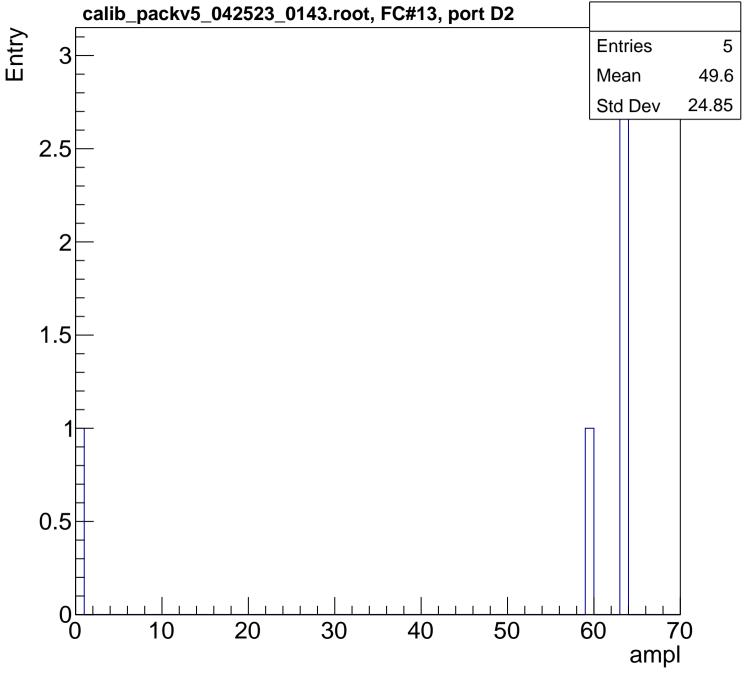




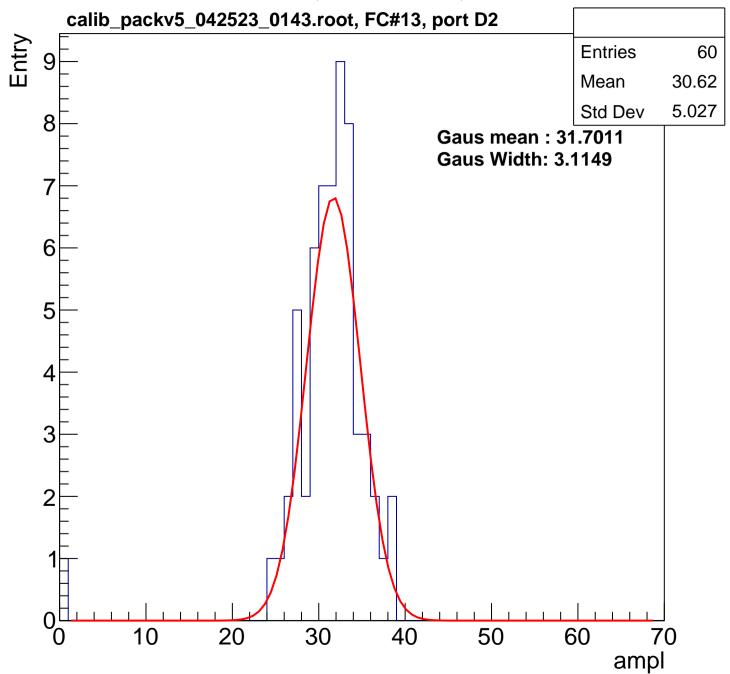


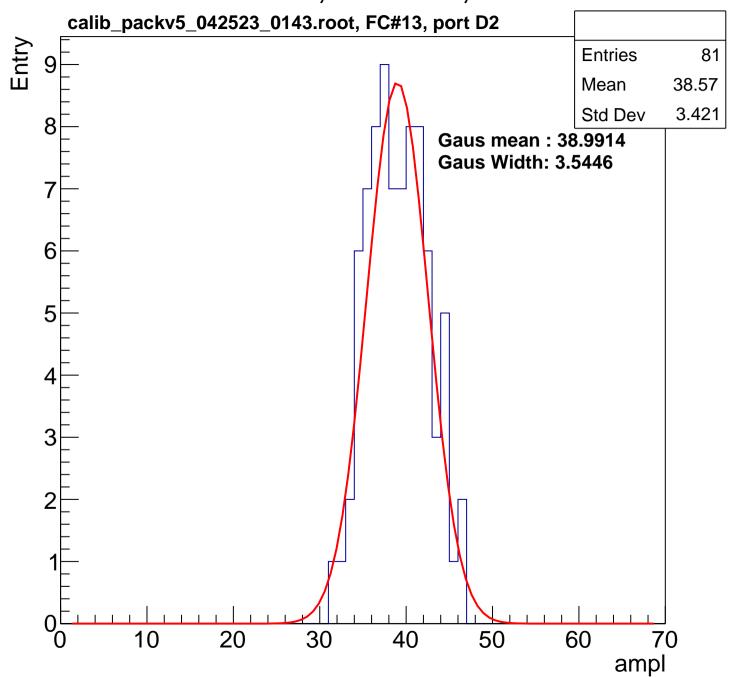


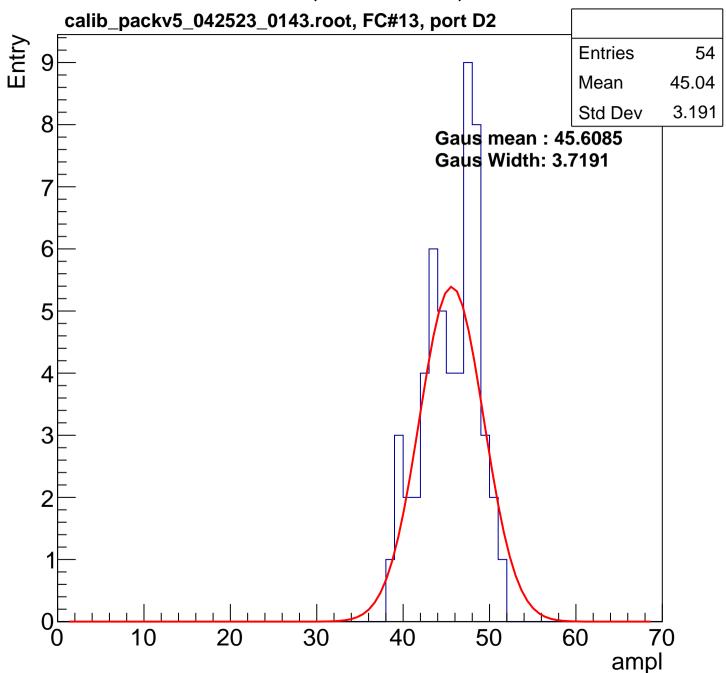


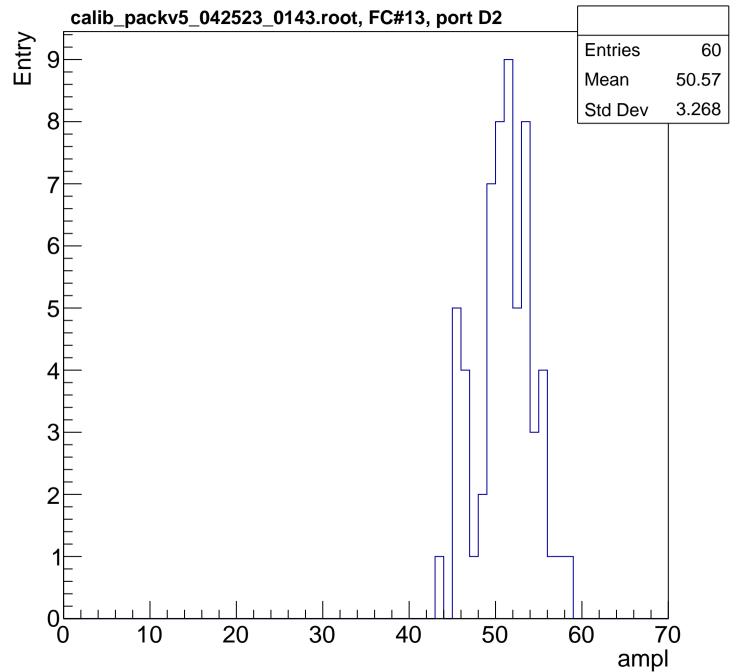


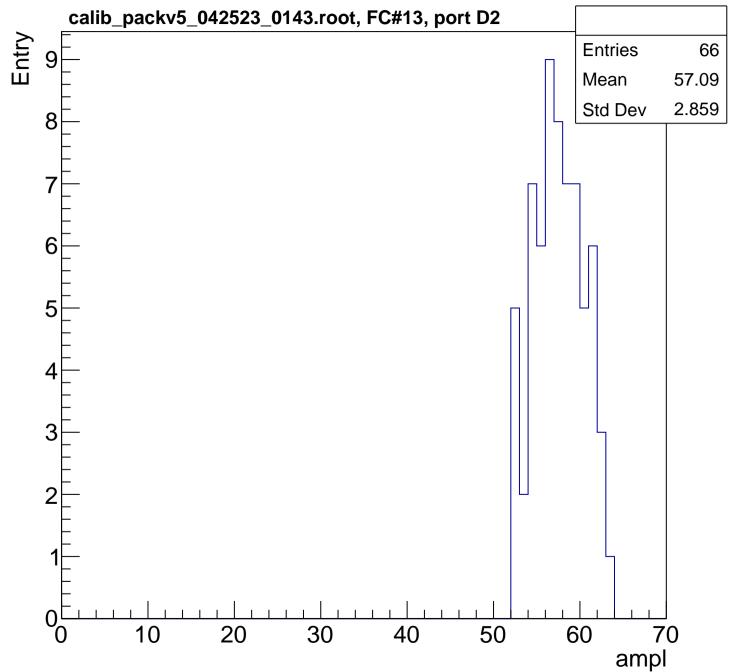


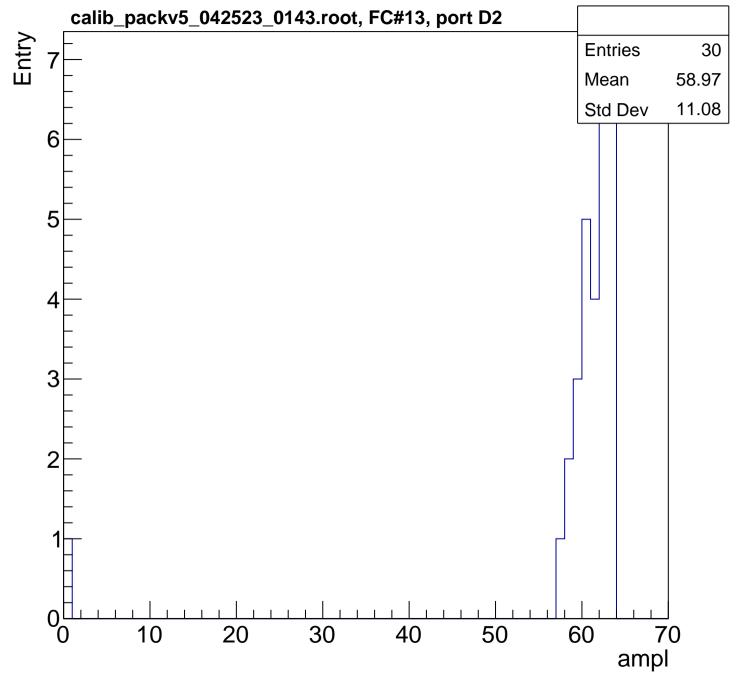


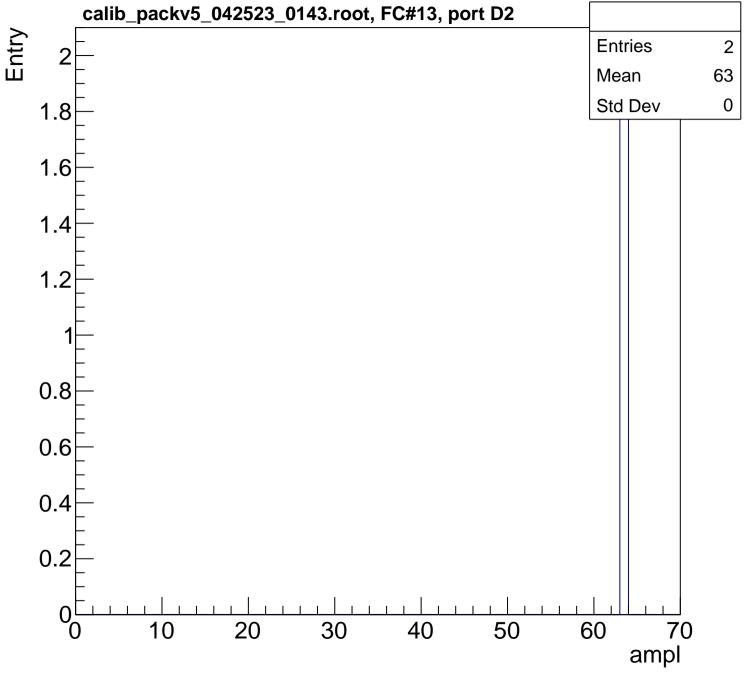


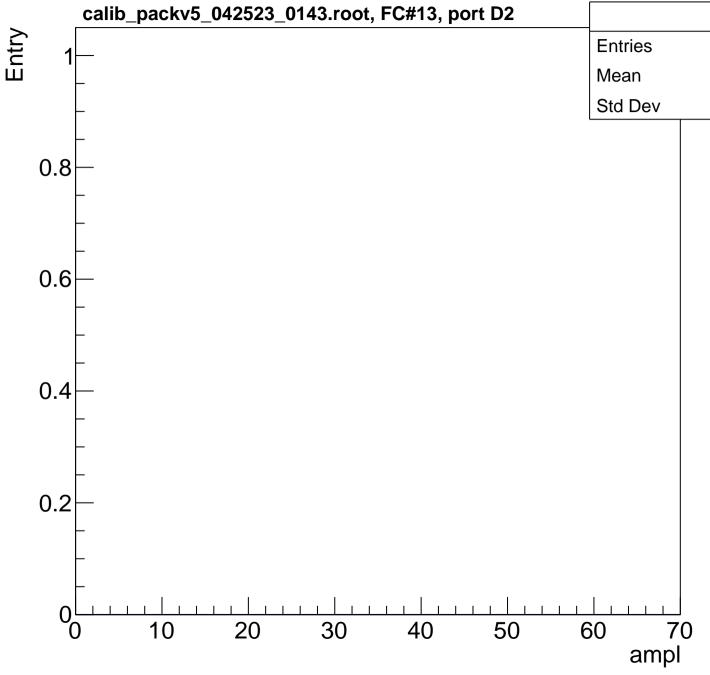


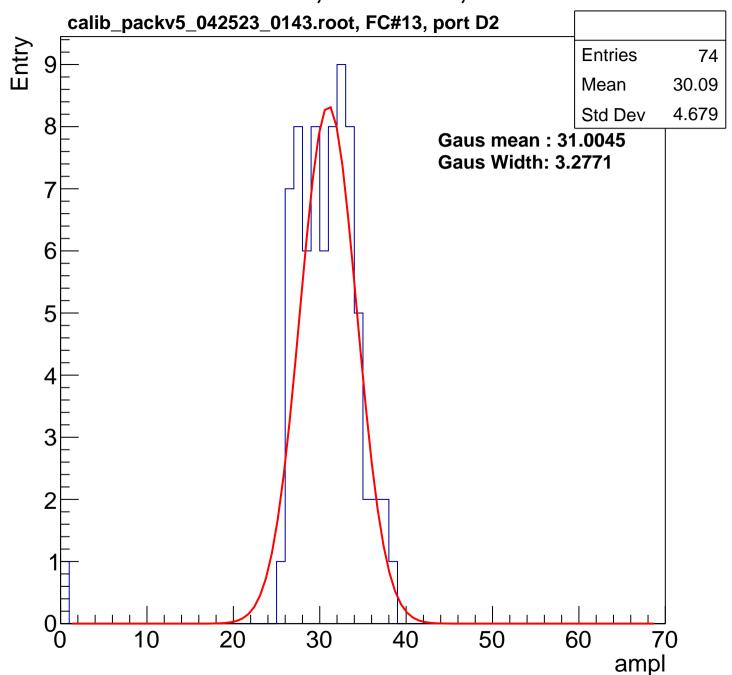


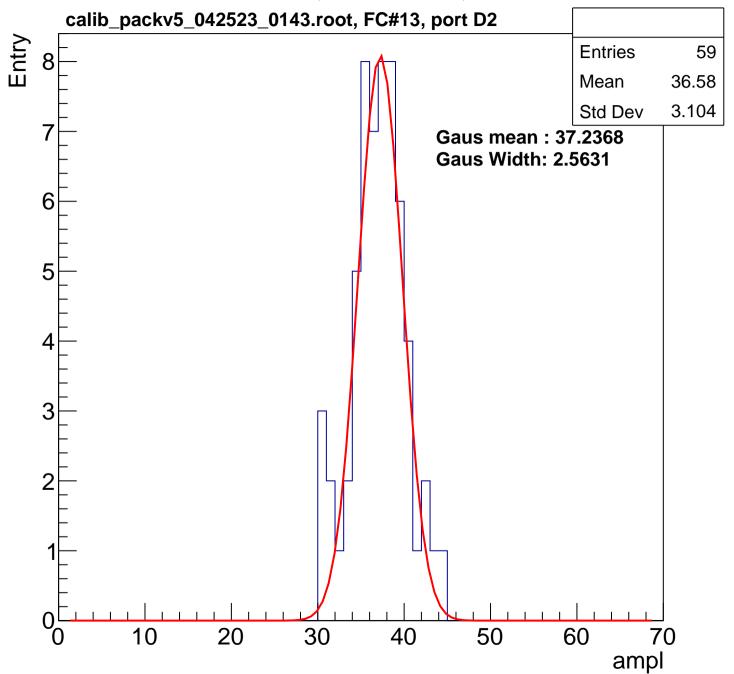


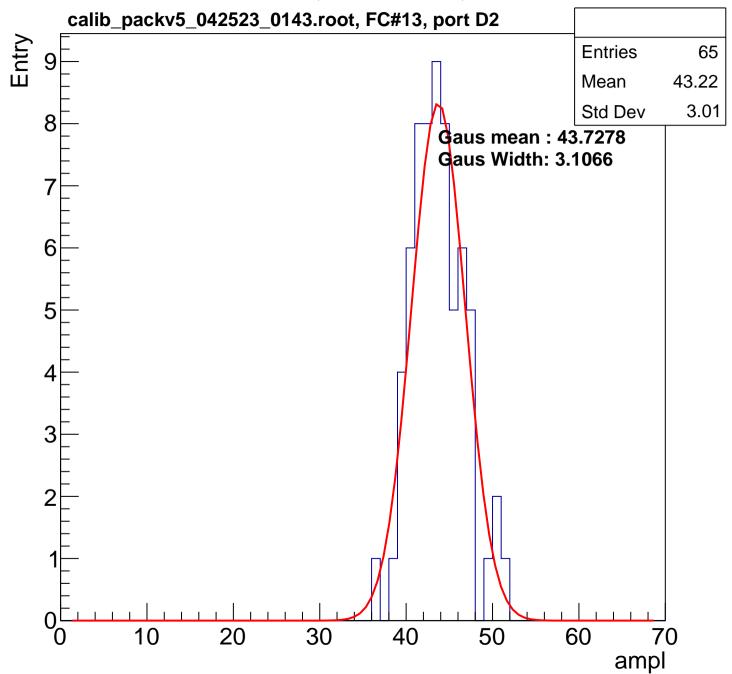


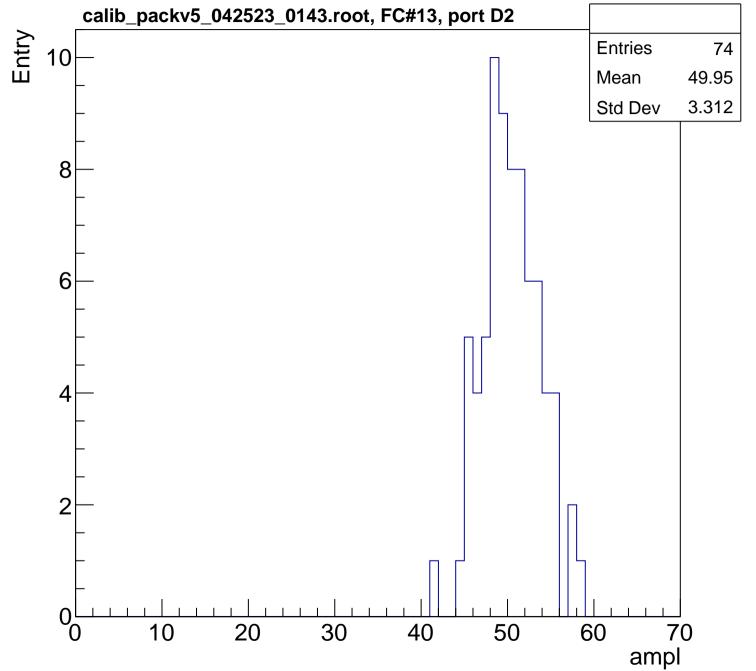


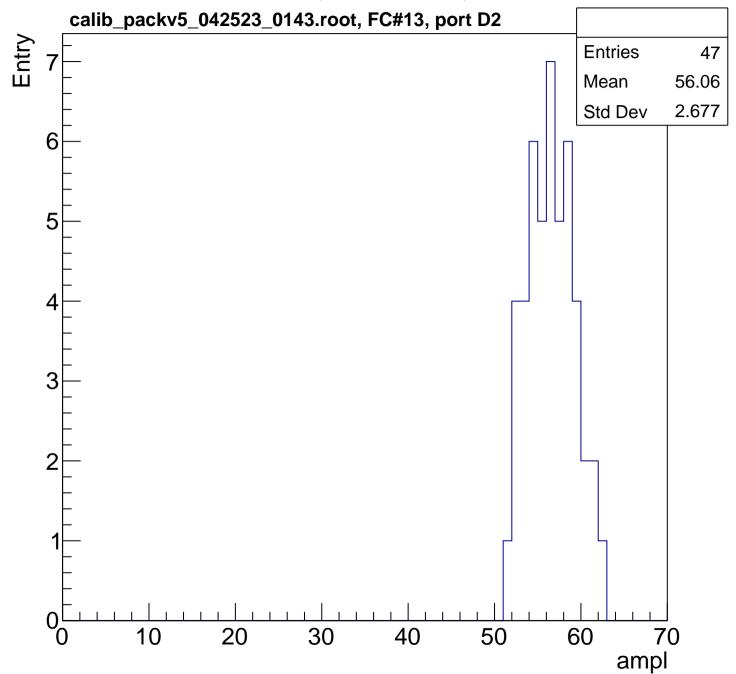


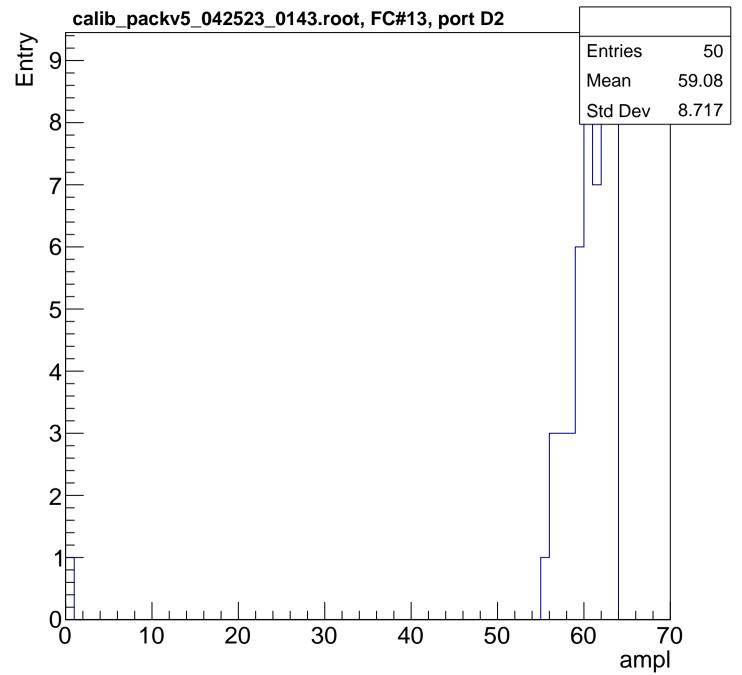


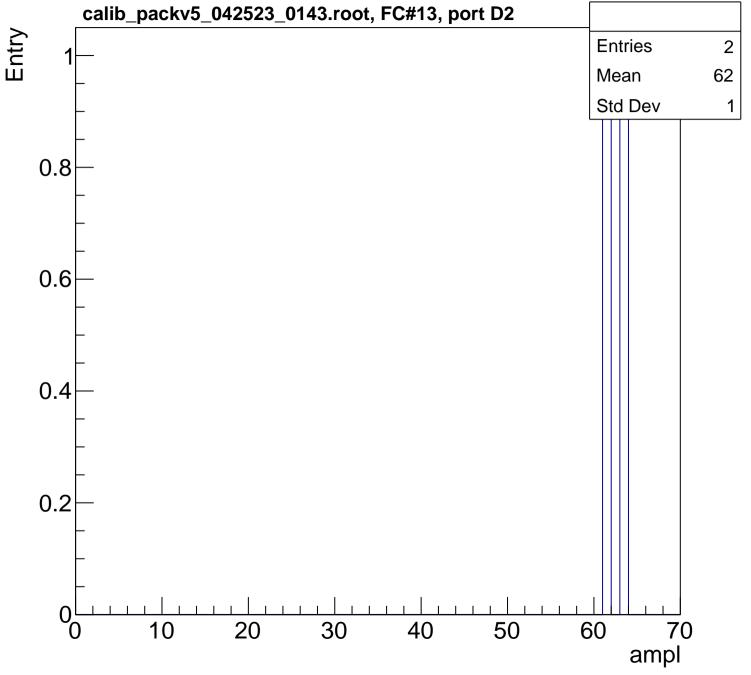


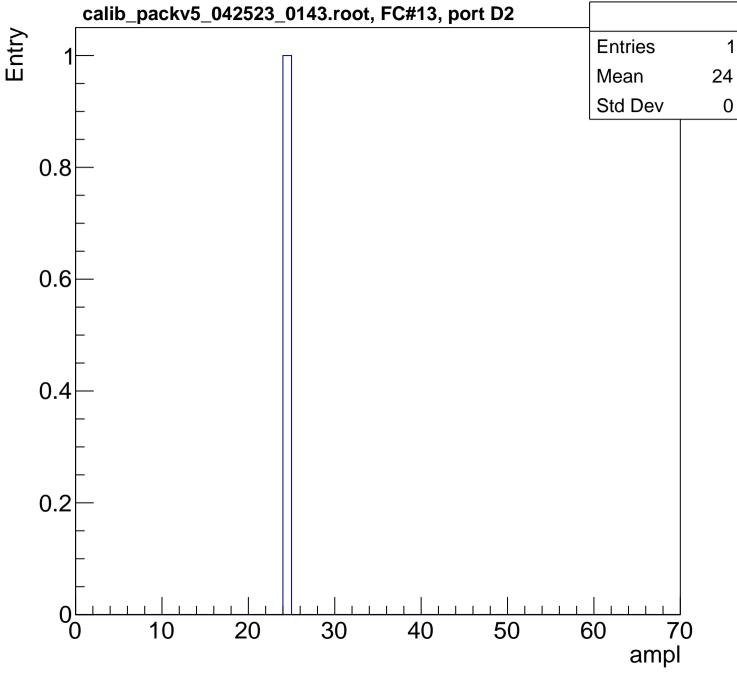


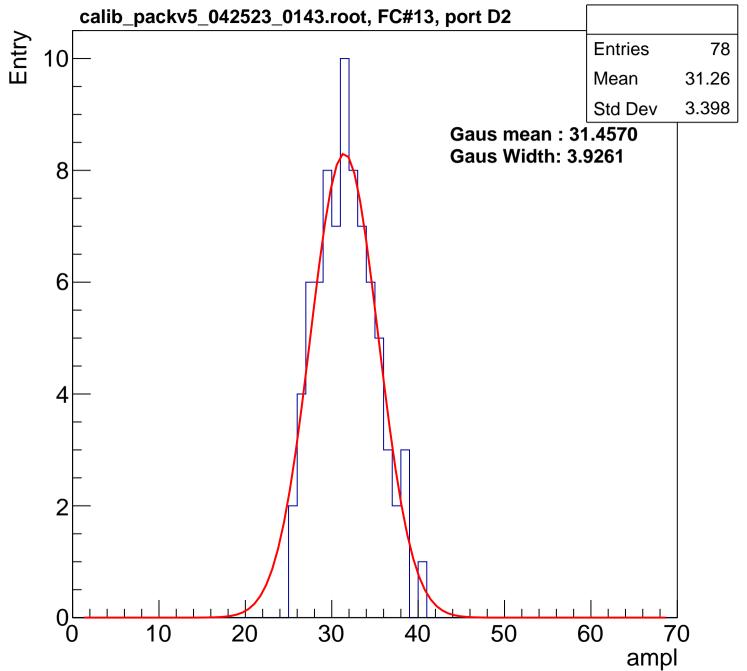


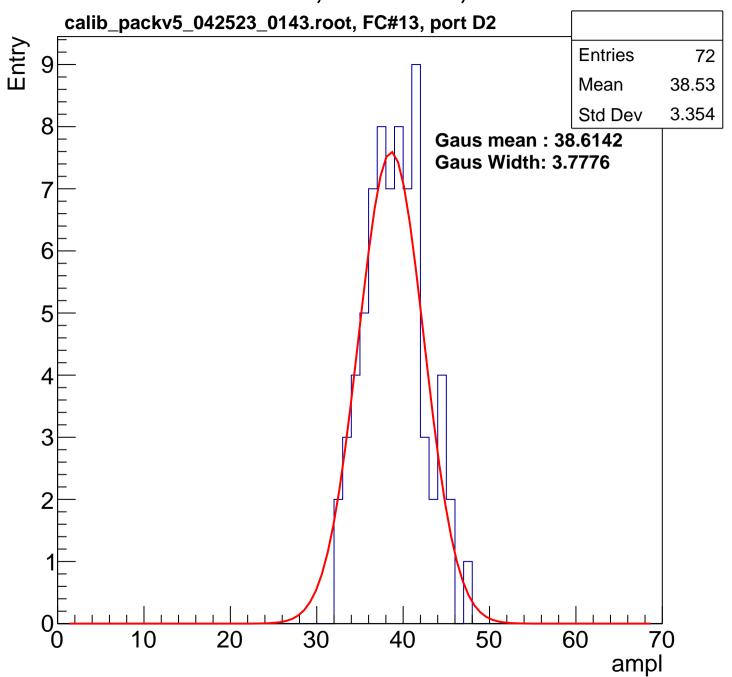


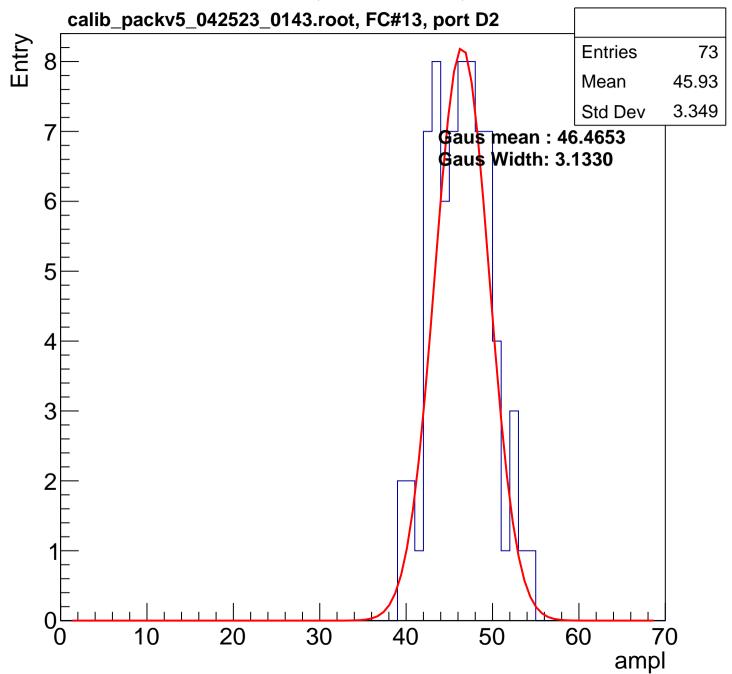


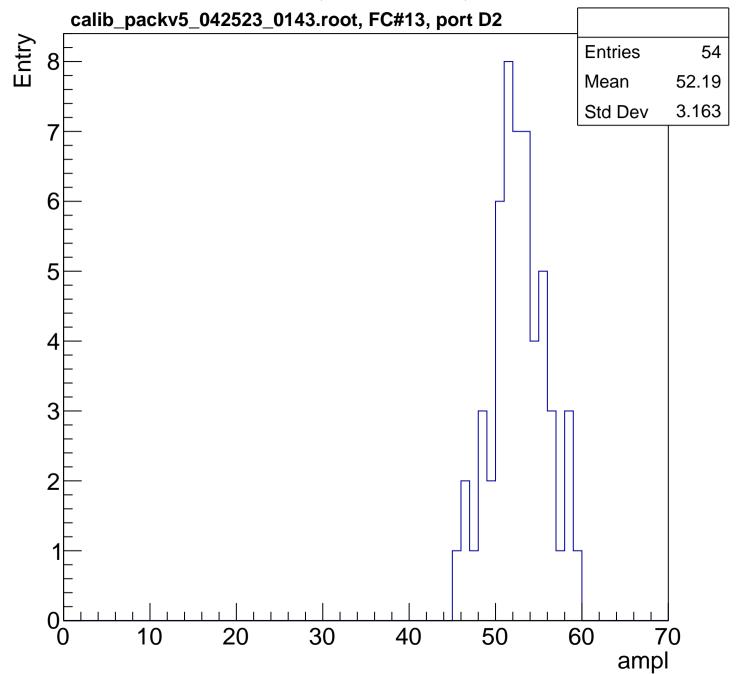


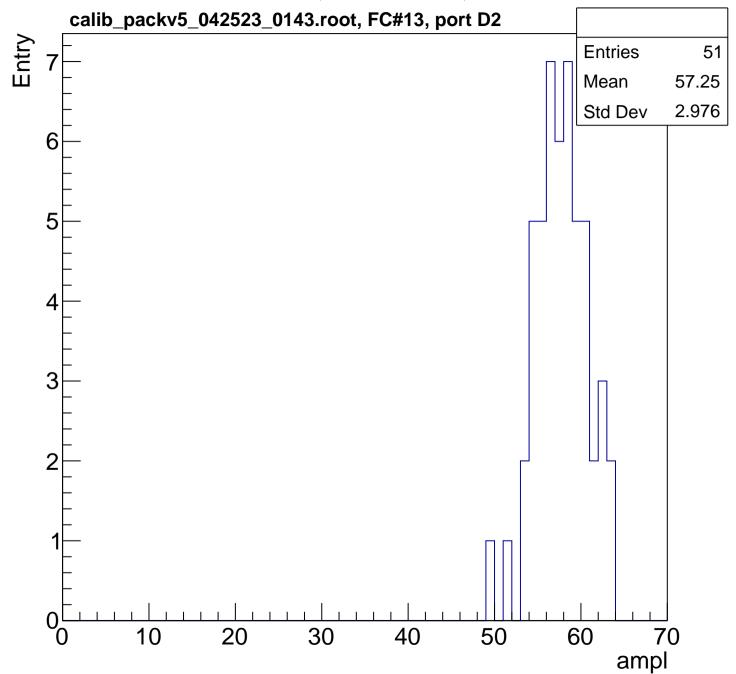


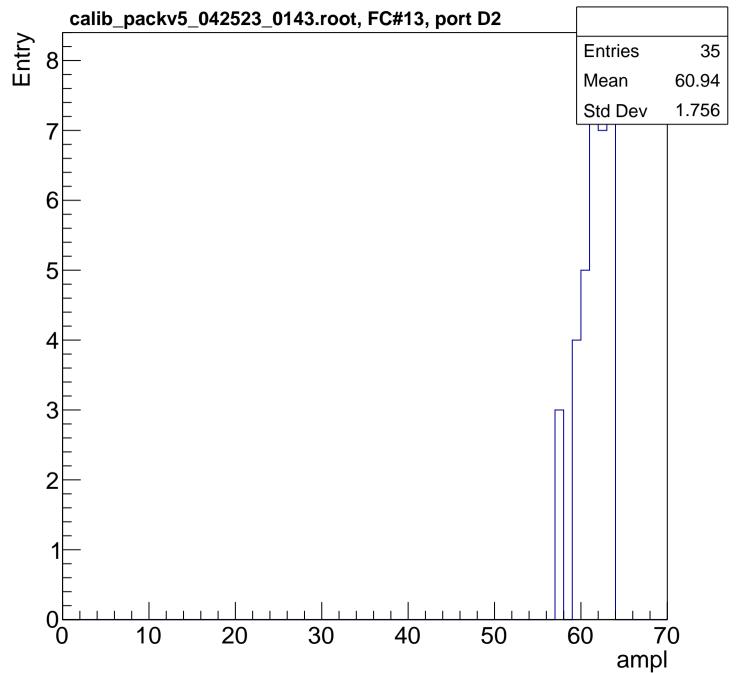






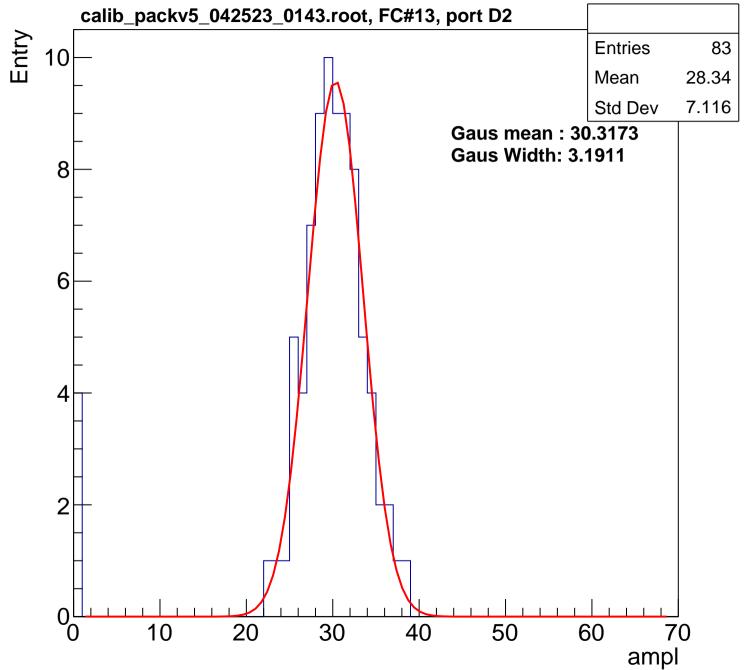


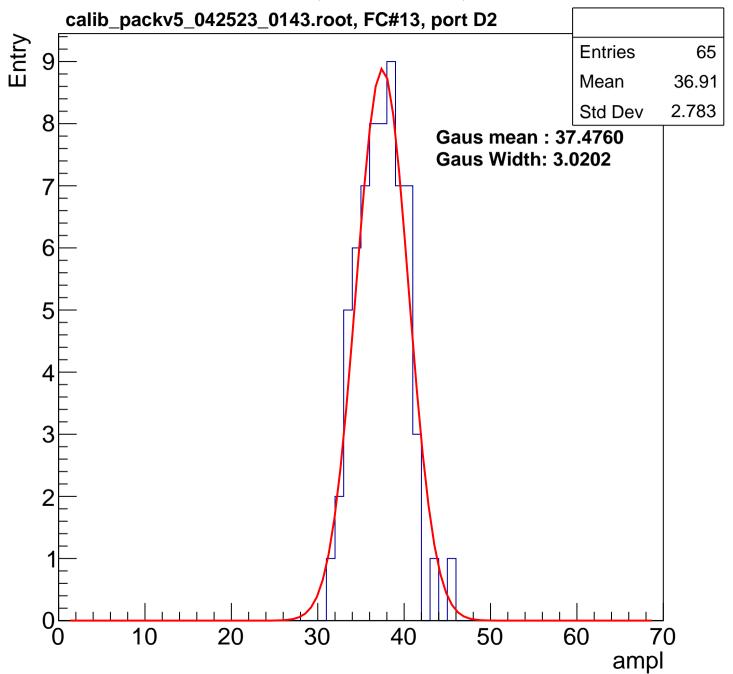


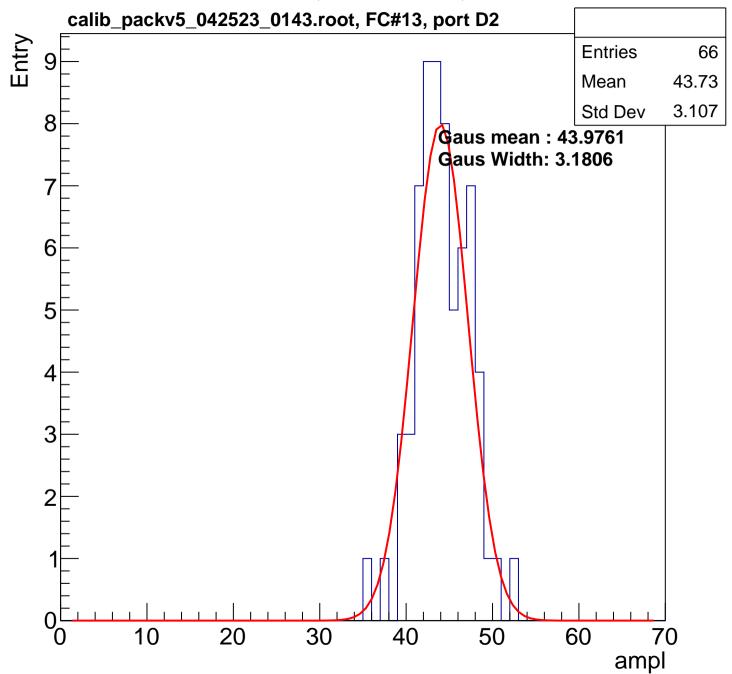


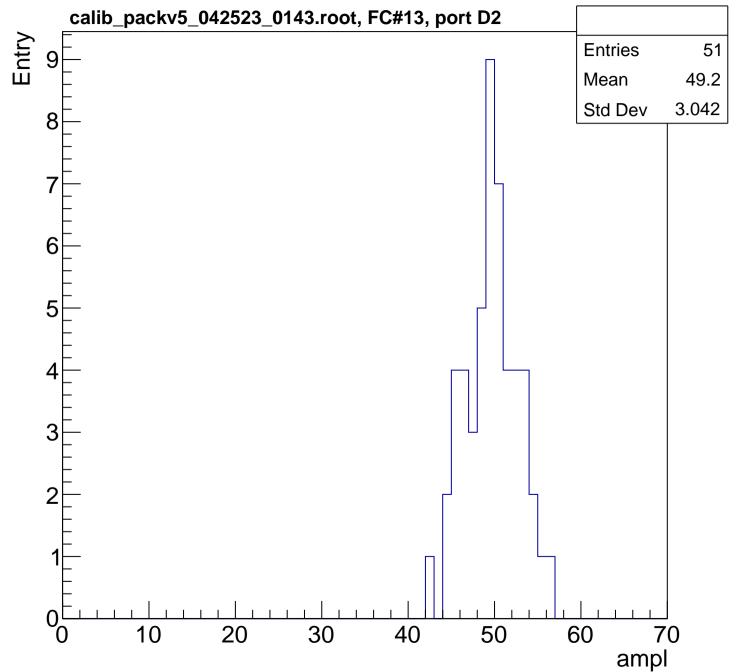


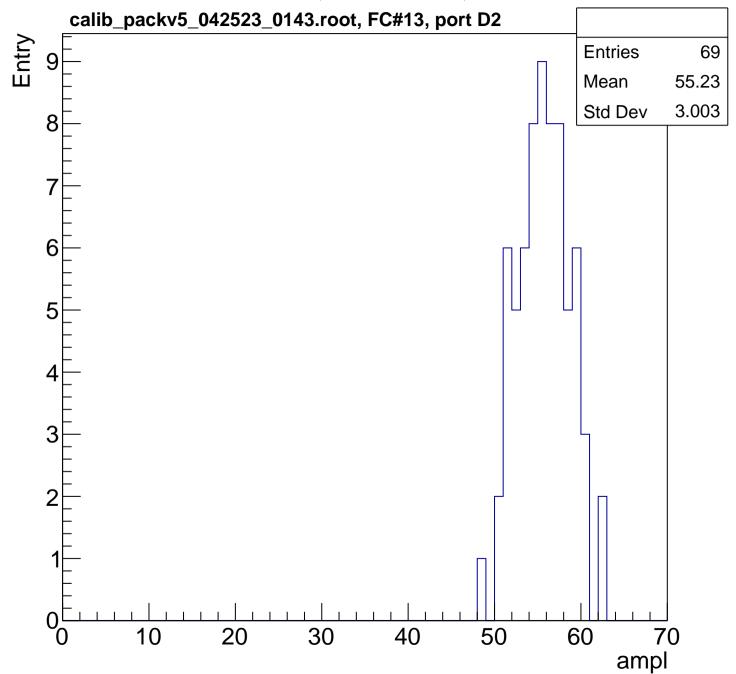
B1L003S, U9-ch19, adc7 calib\_packv5\_042523\_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

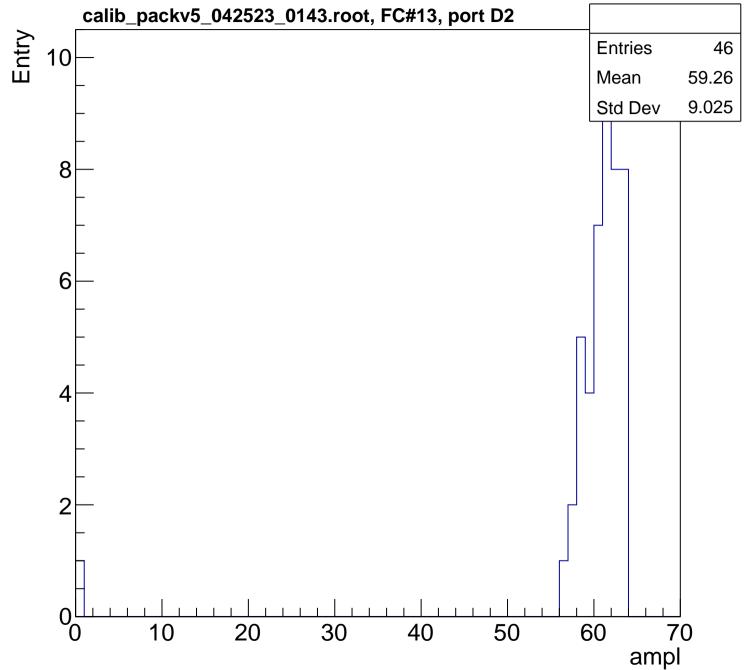


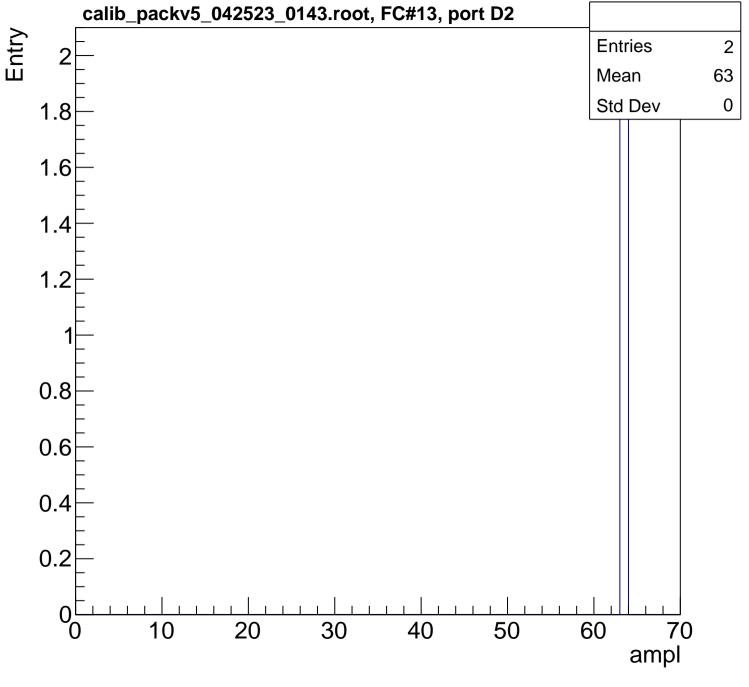




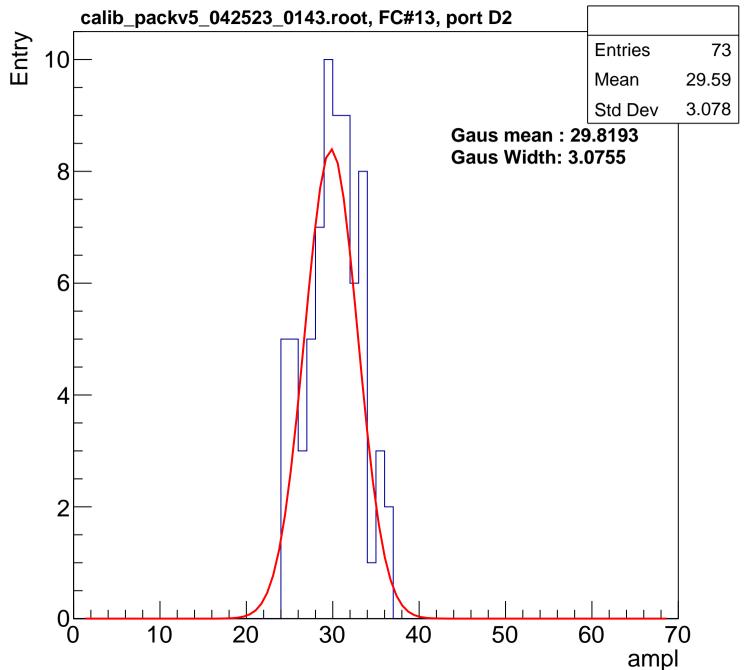


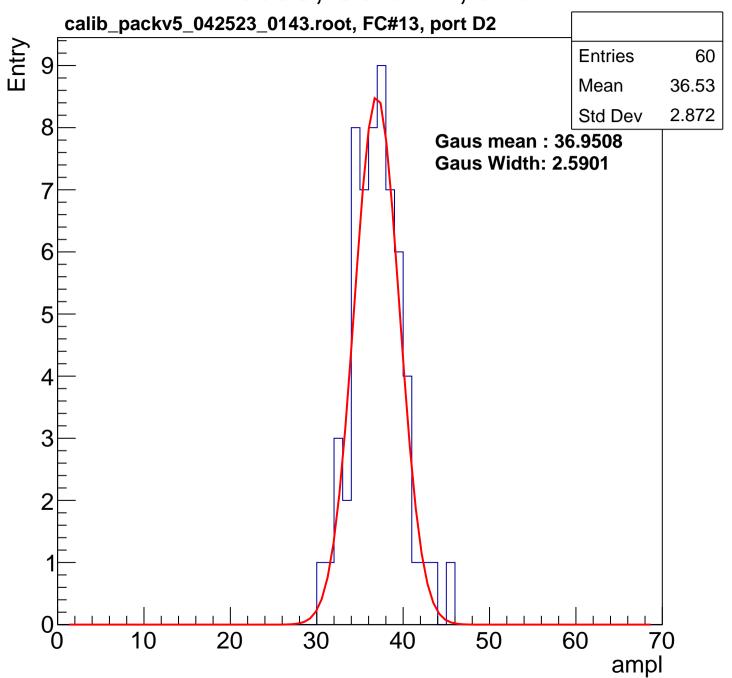


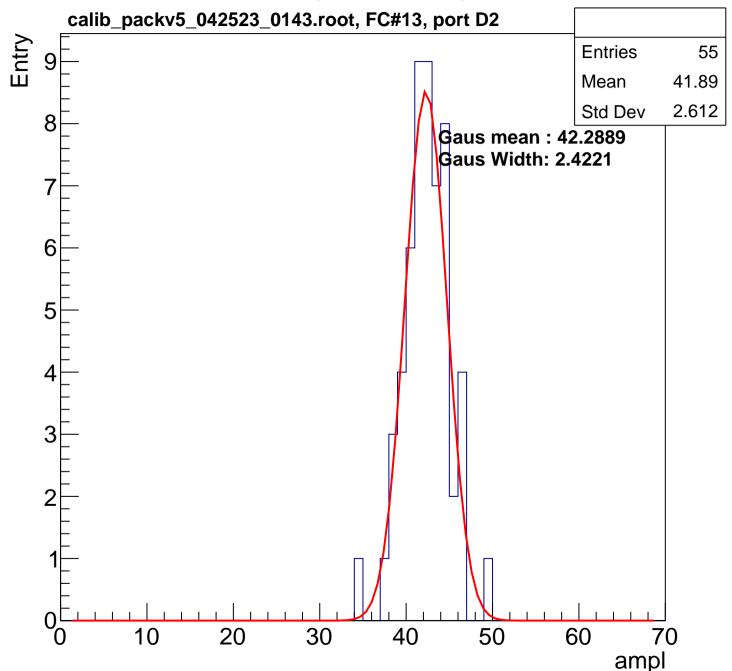


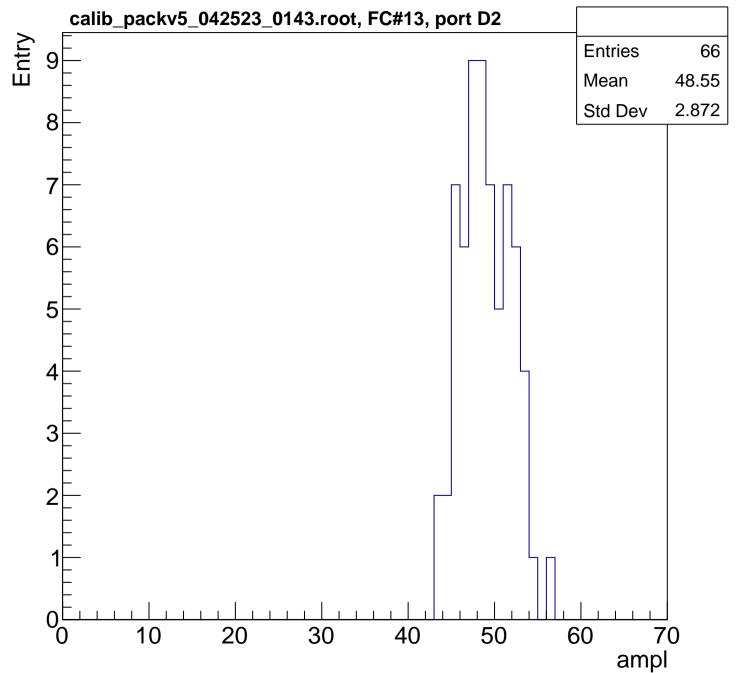


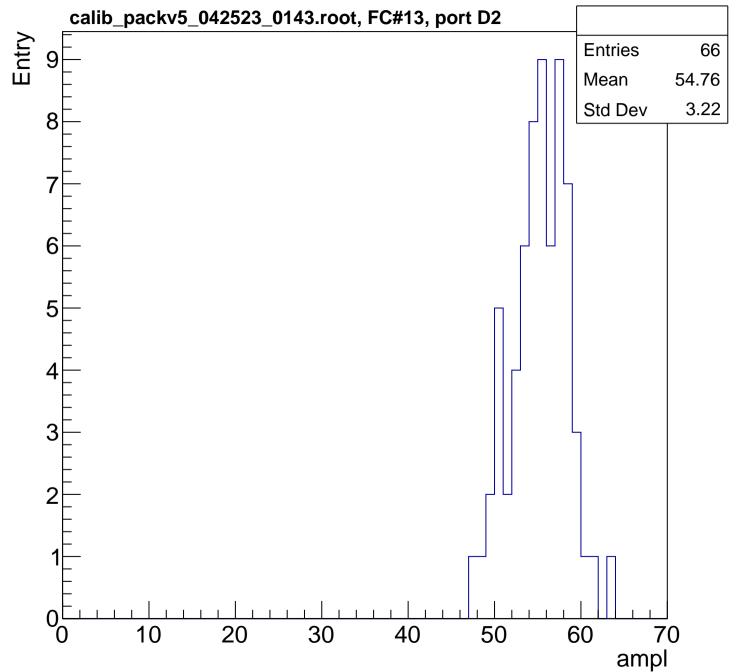


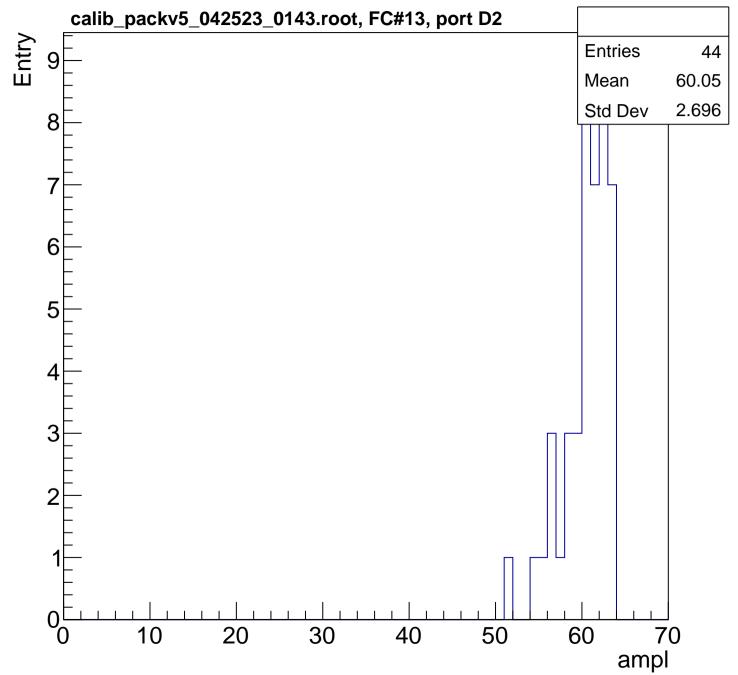


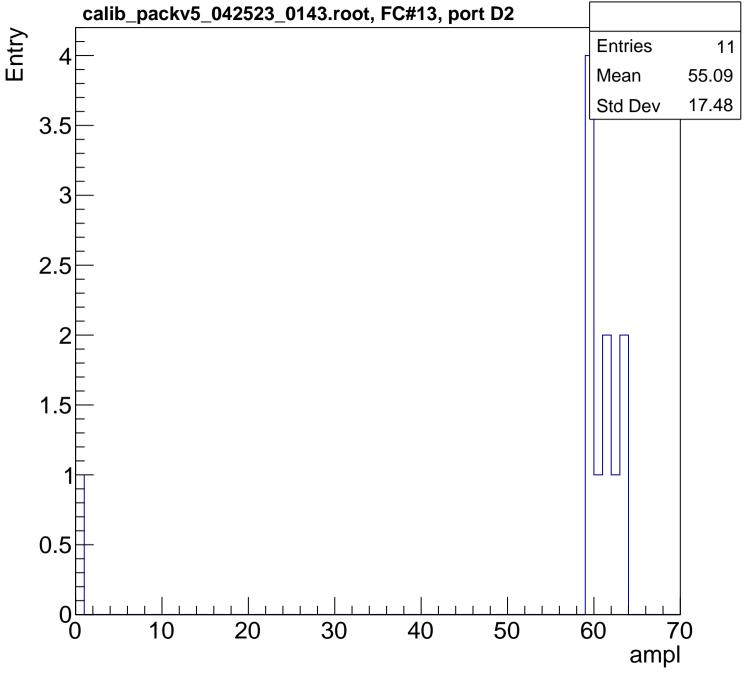


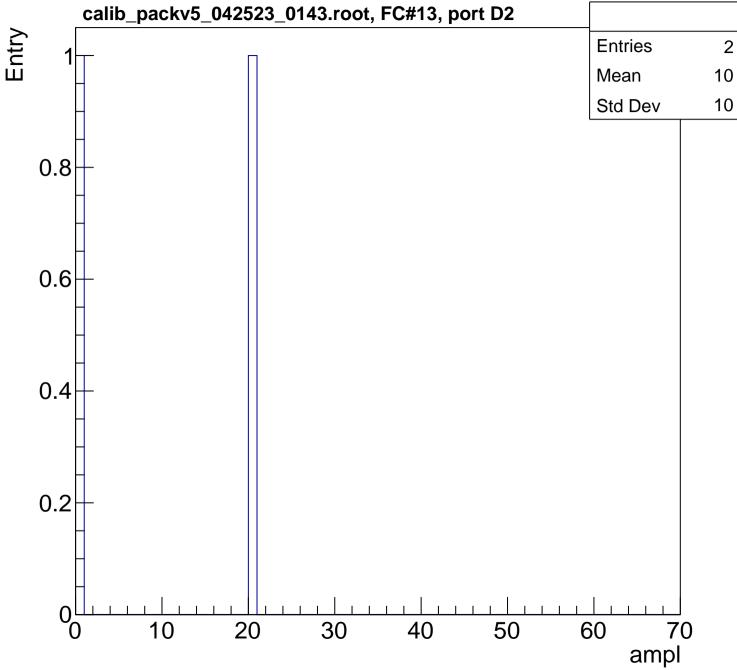


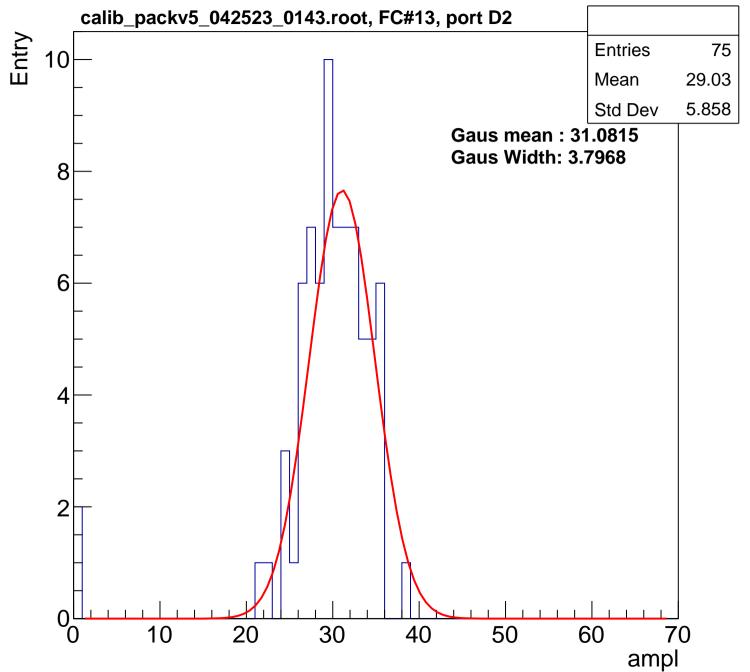


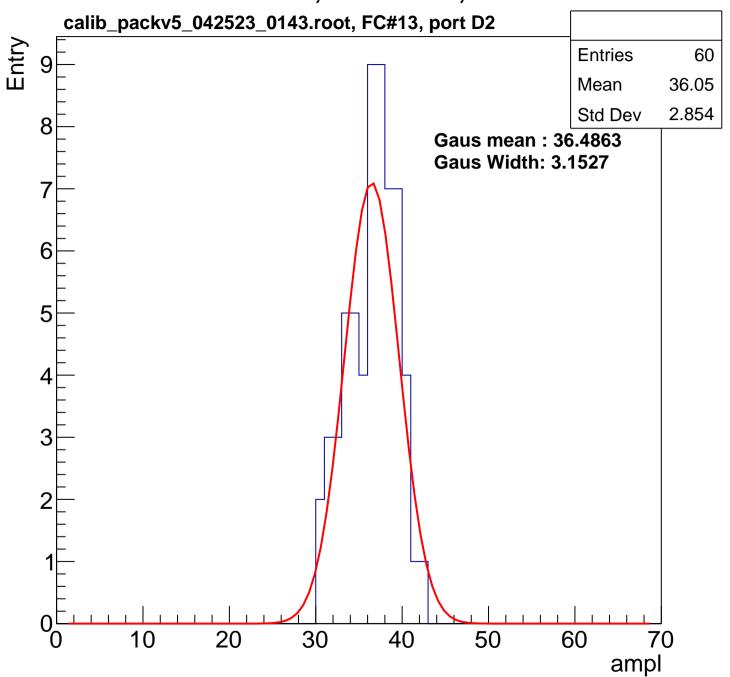


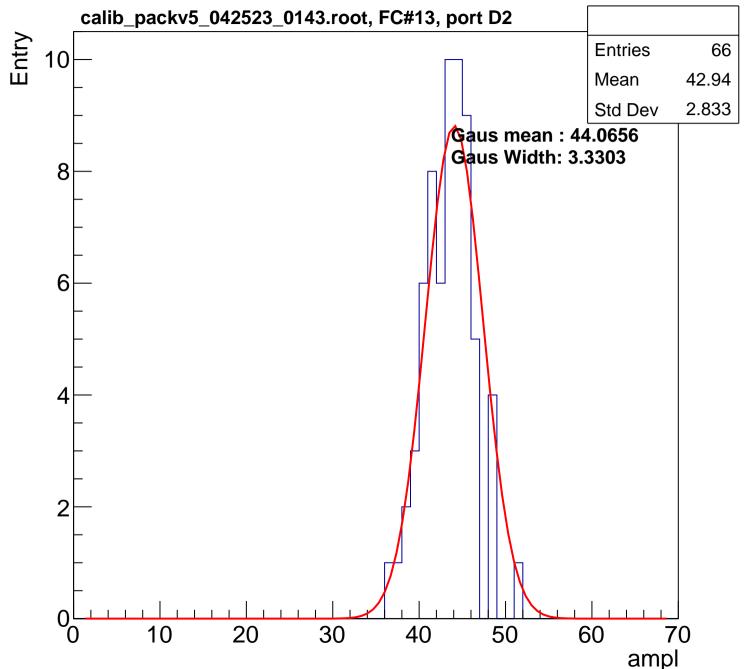


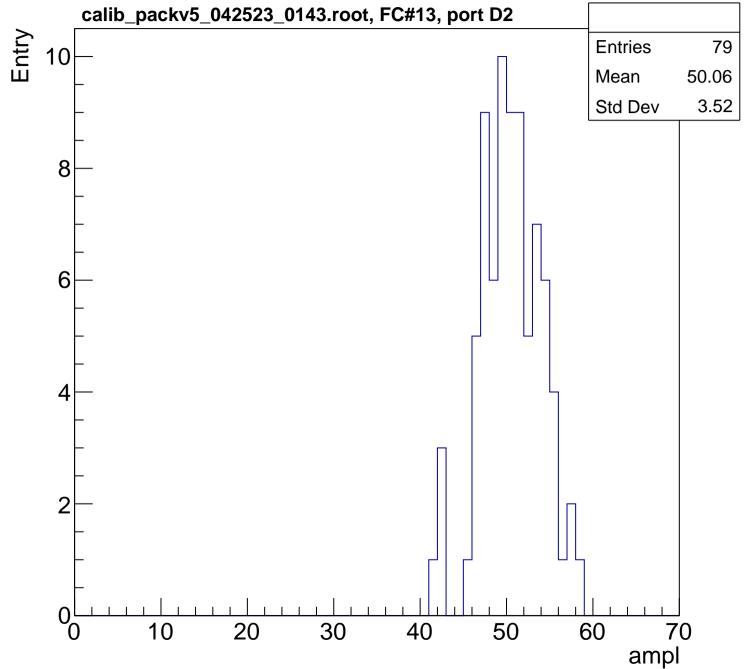


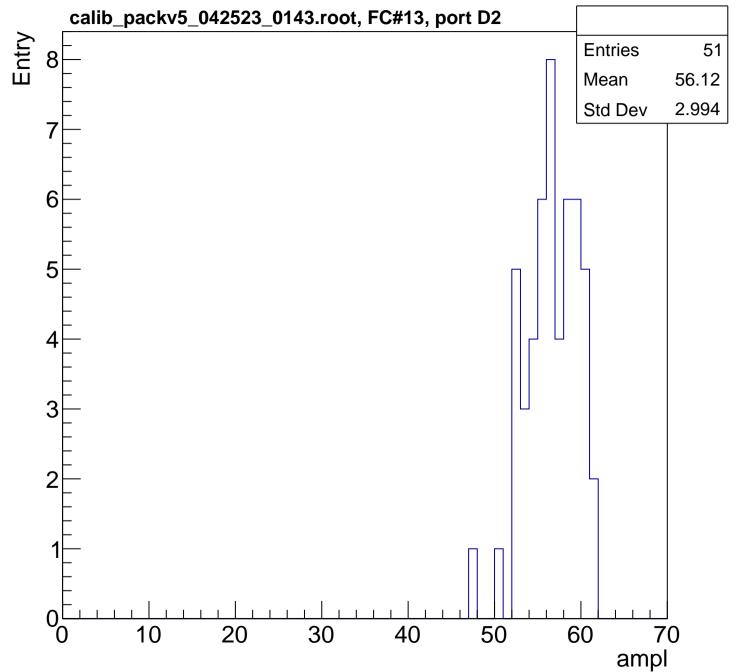


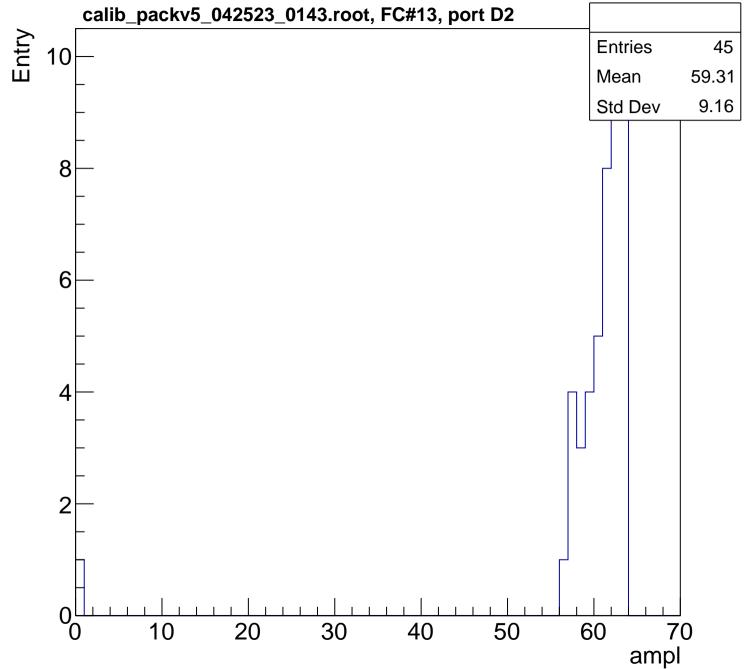


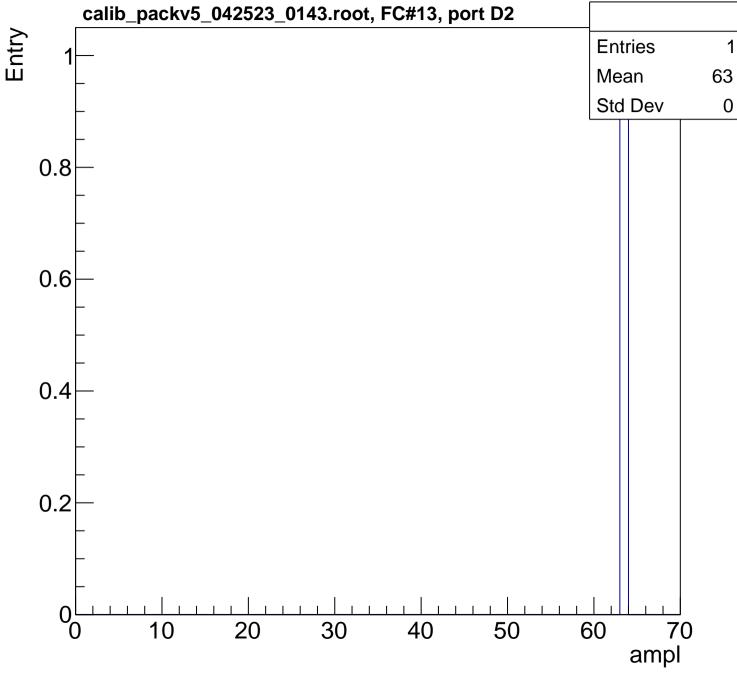


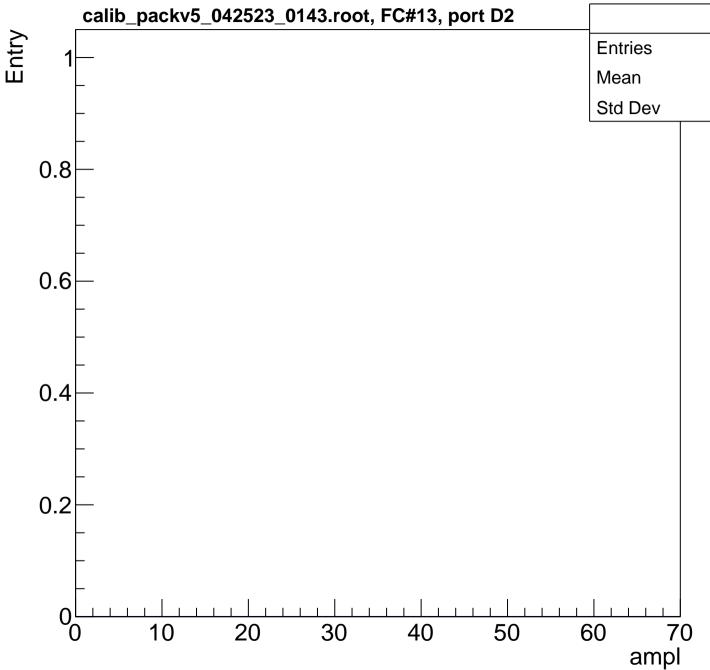


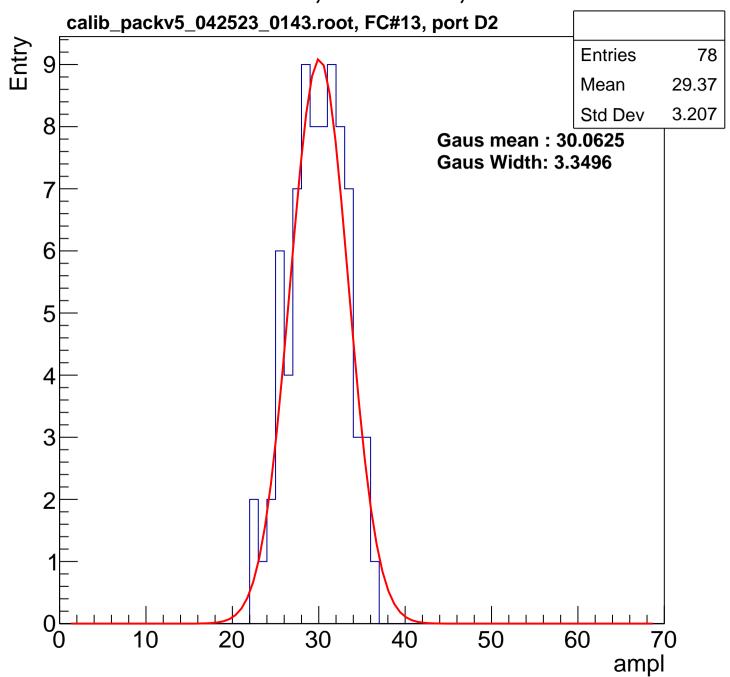


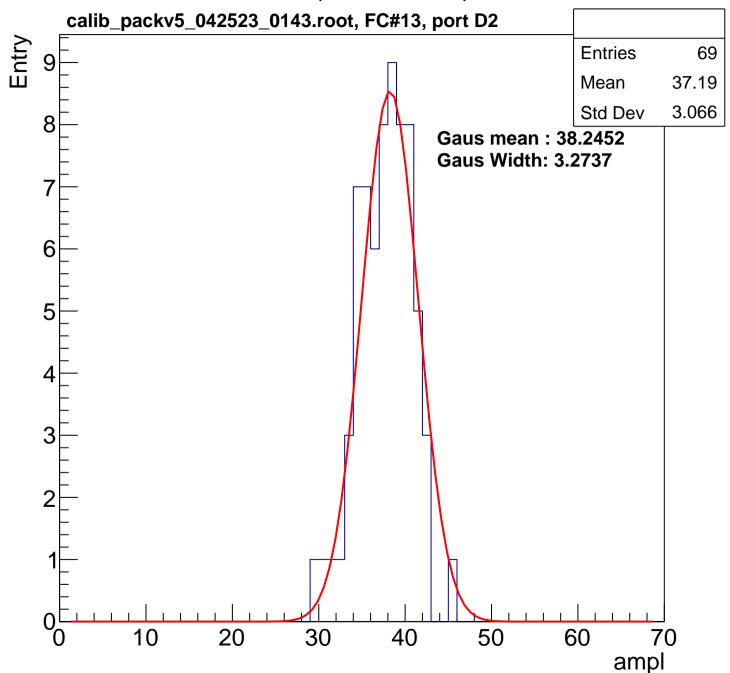


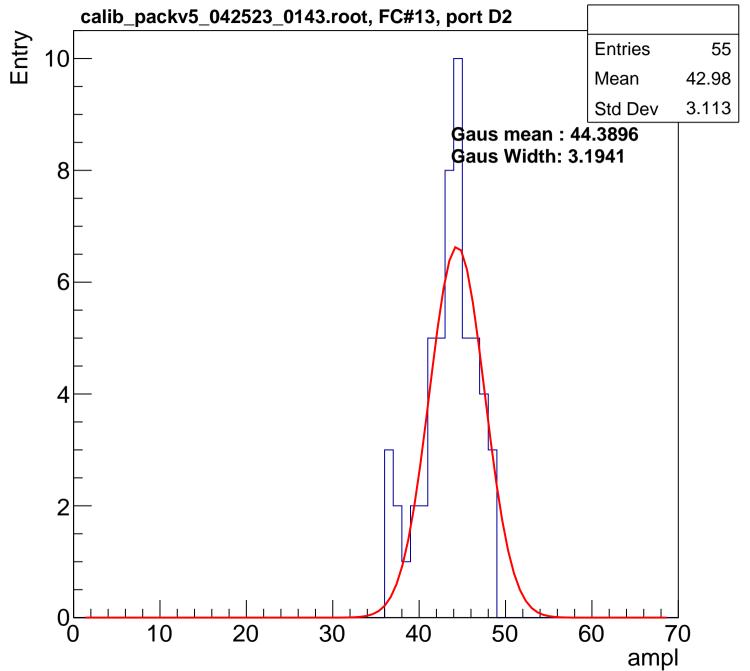


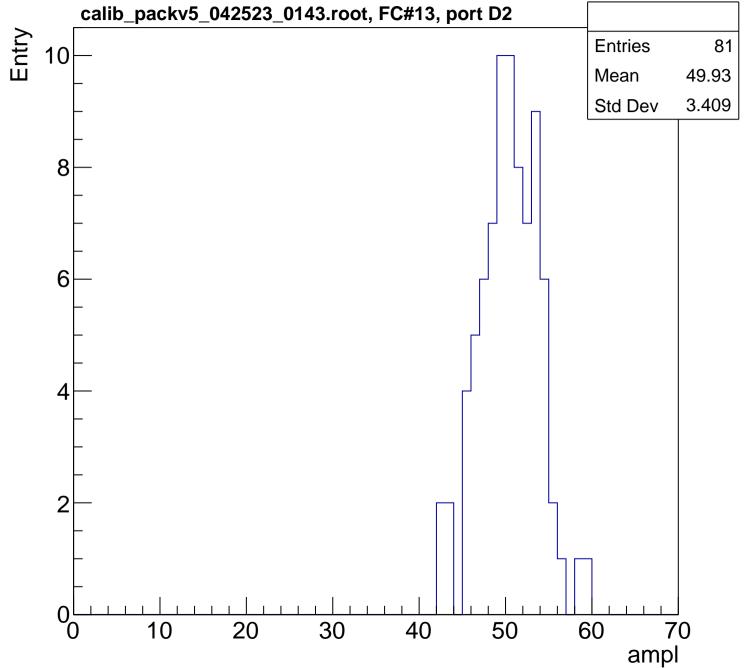


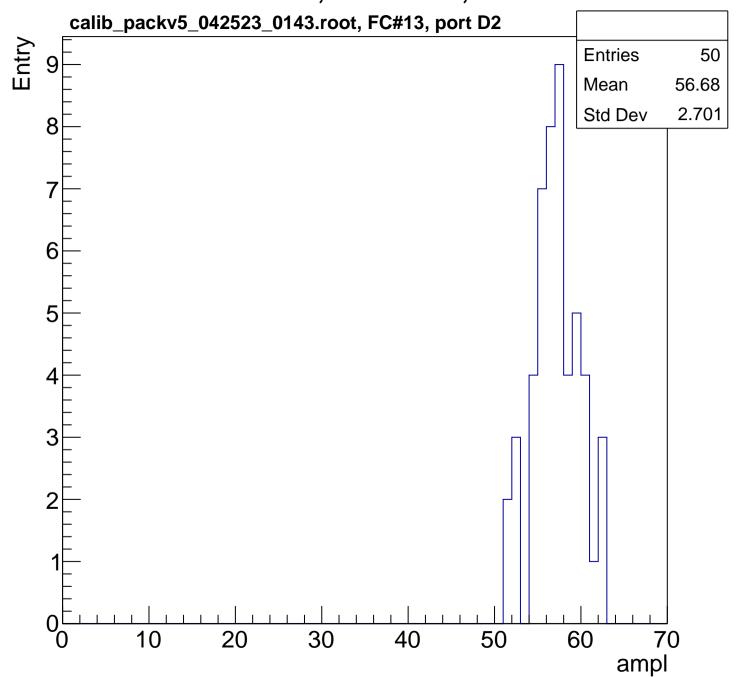


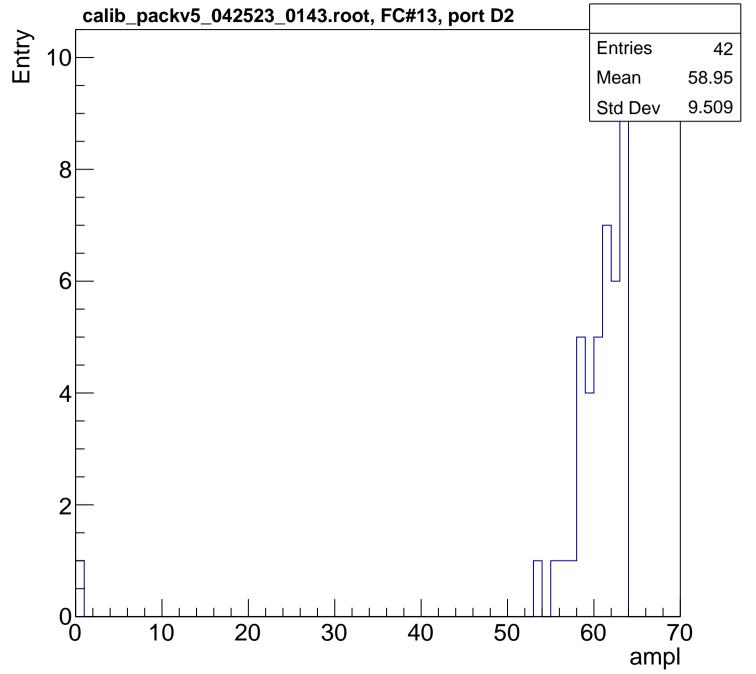


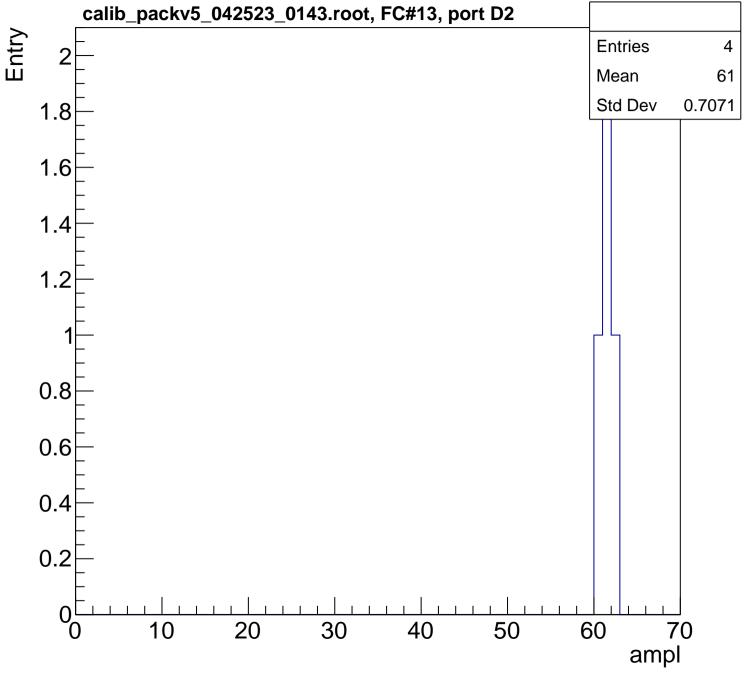


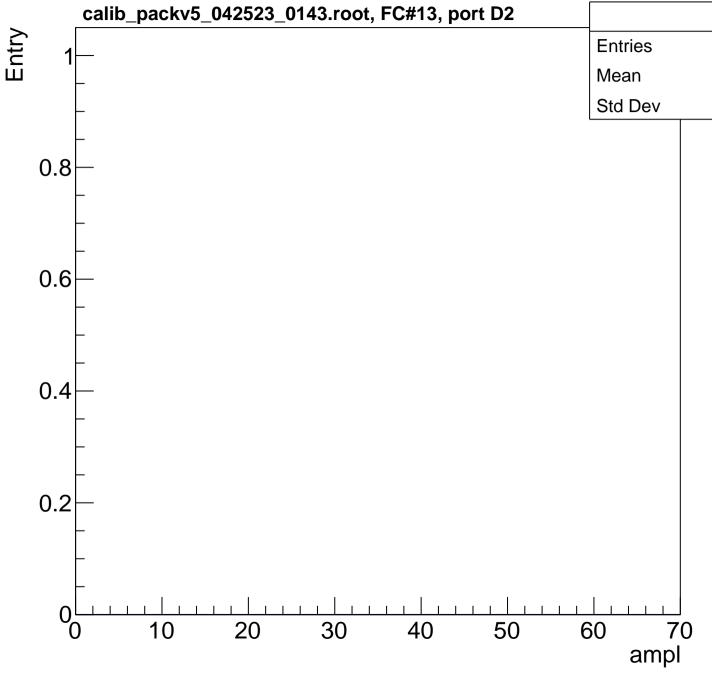


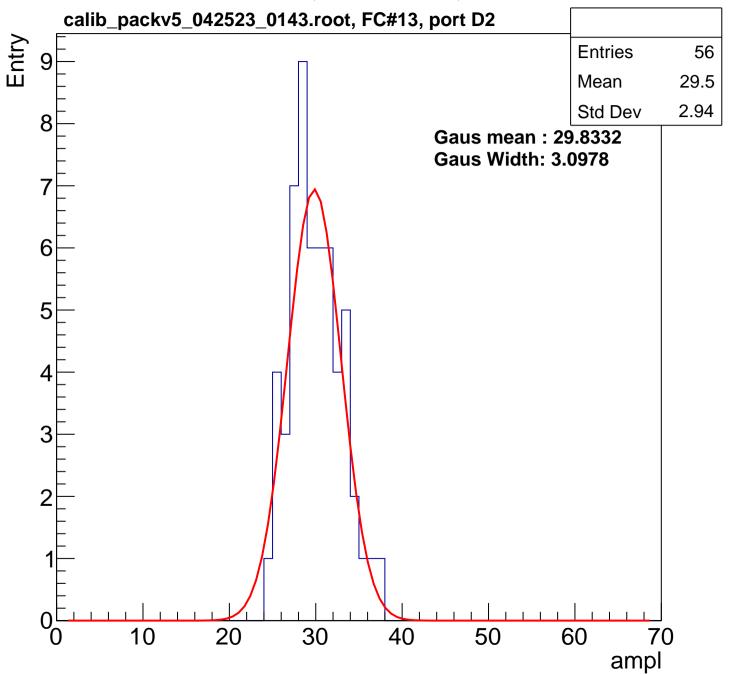


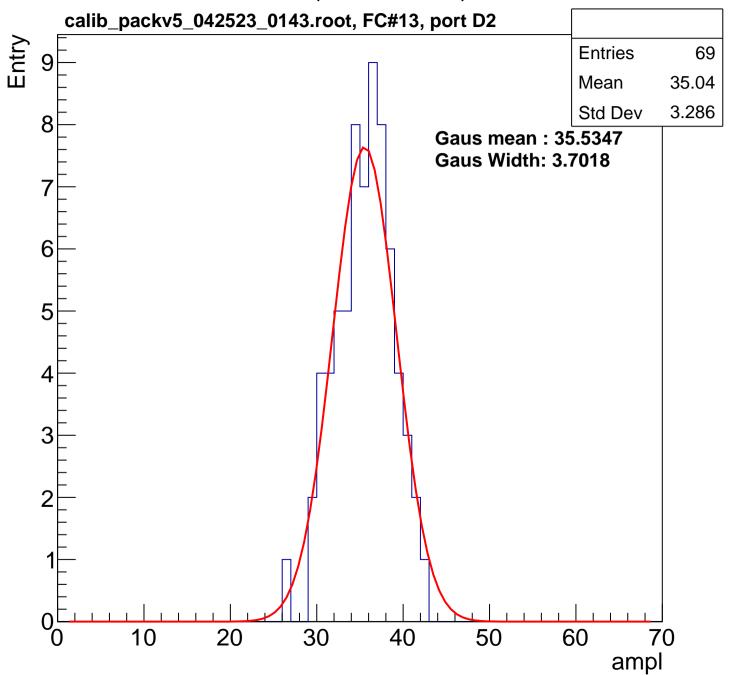


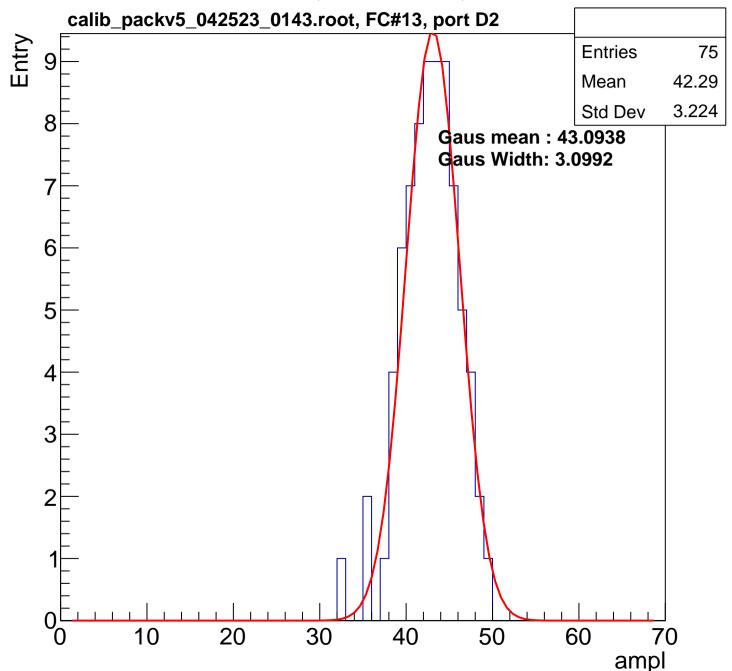


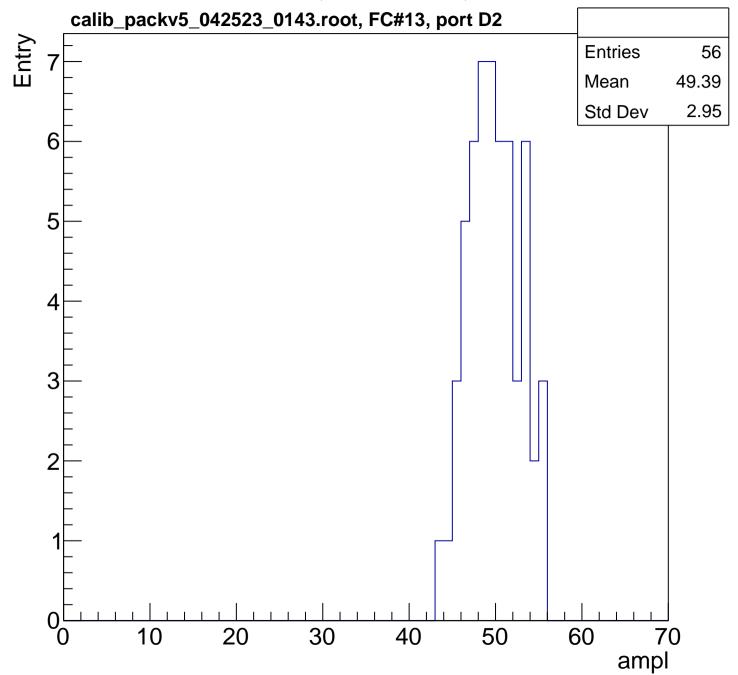


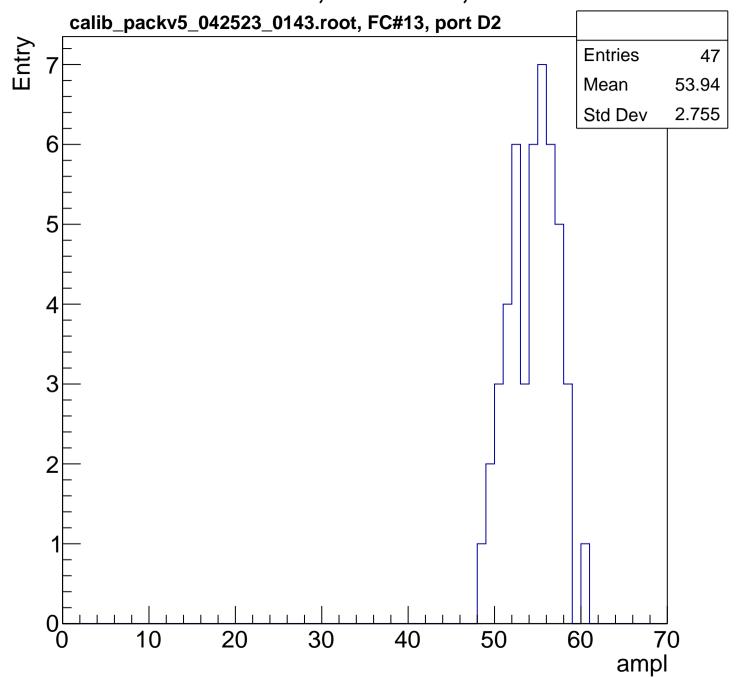


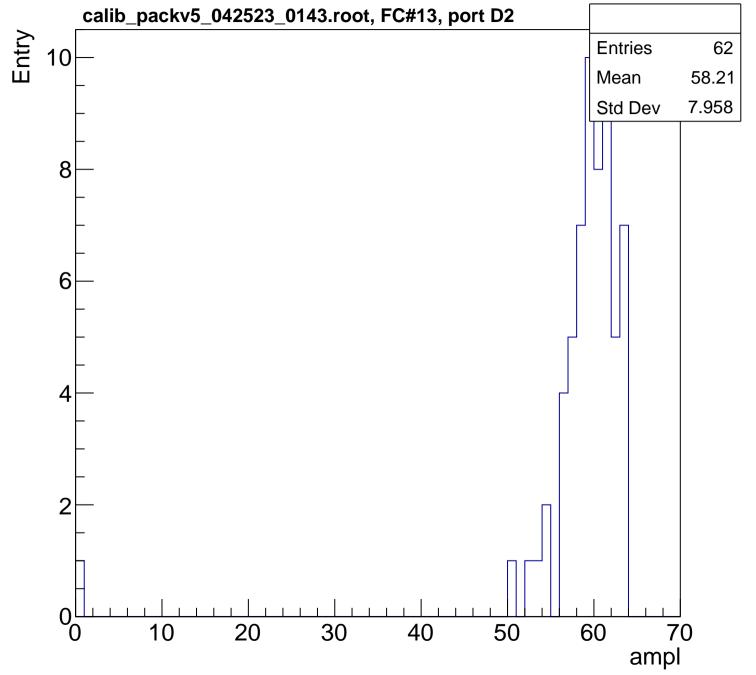


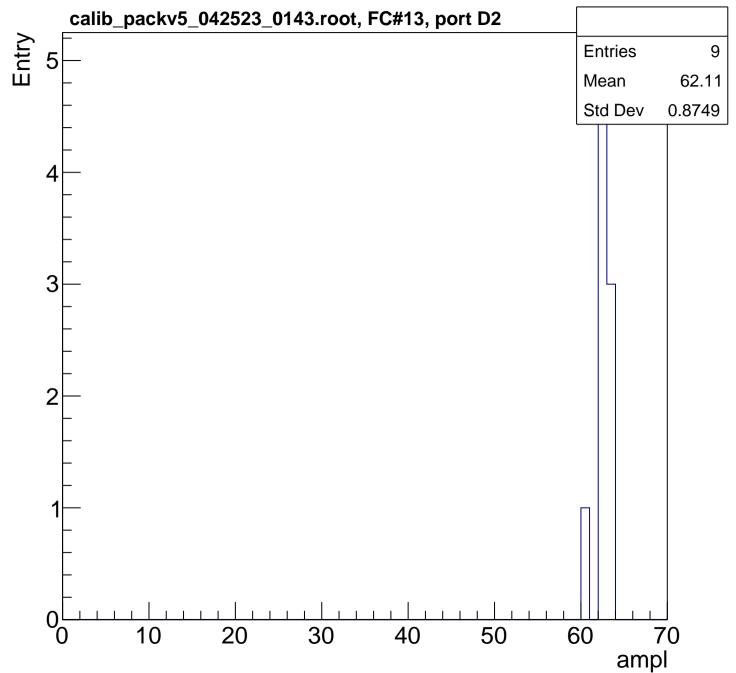




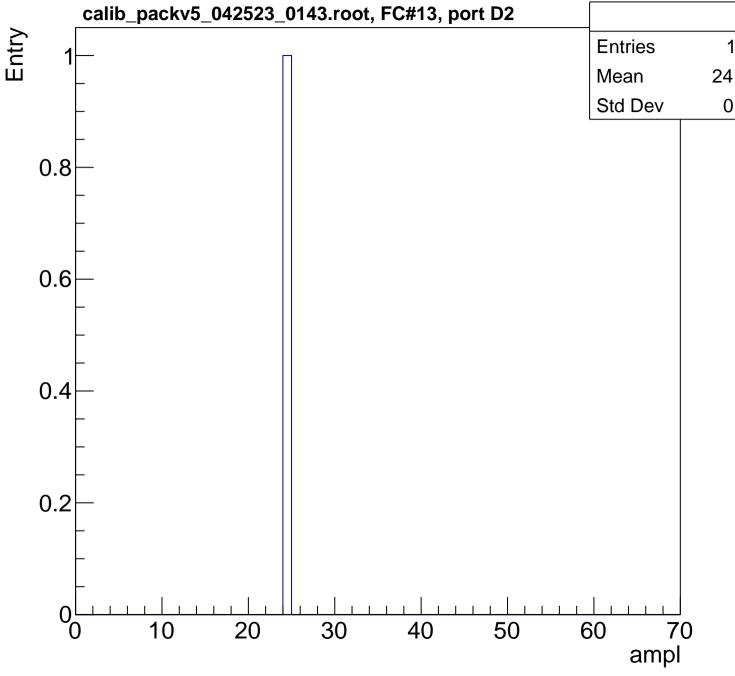


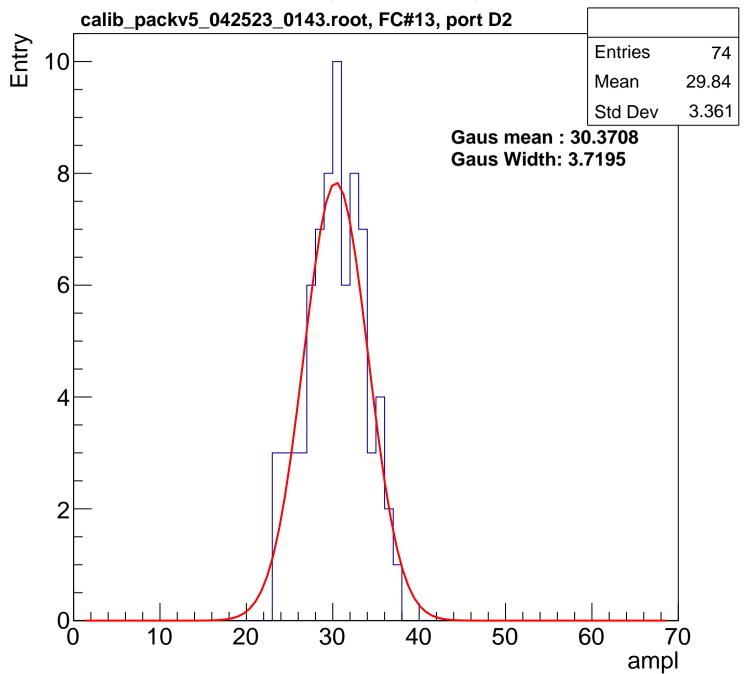


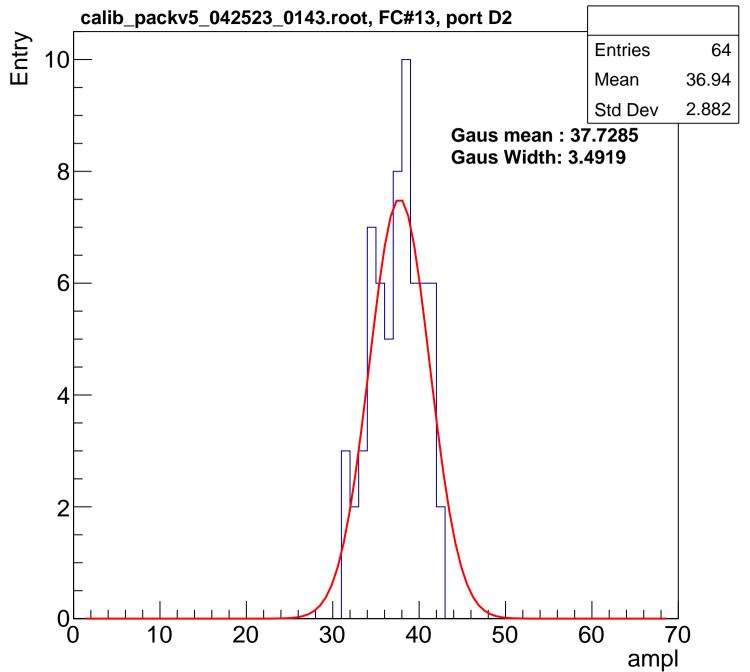


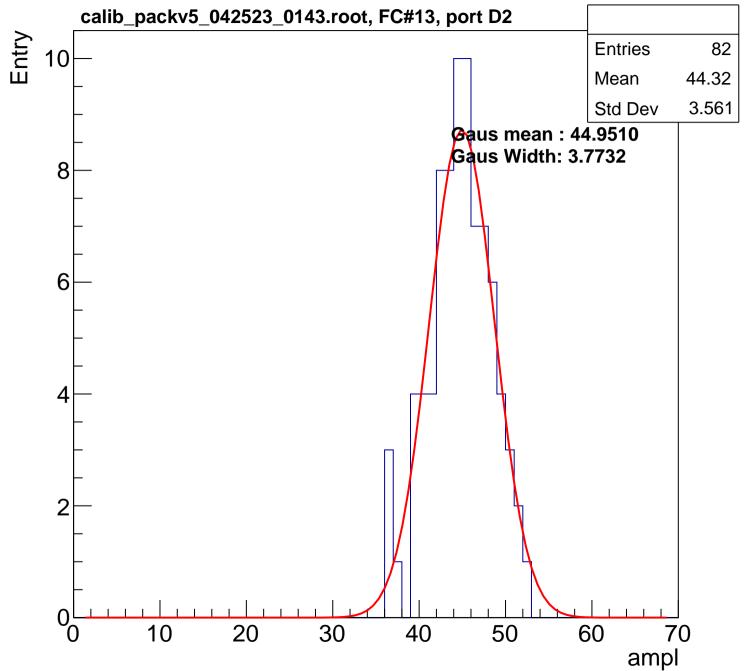


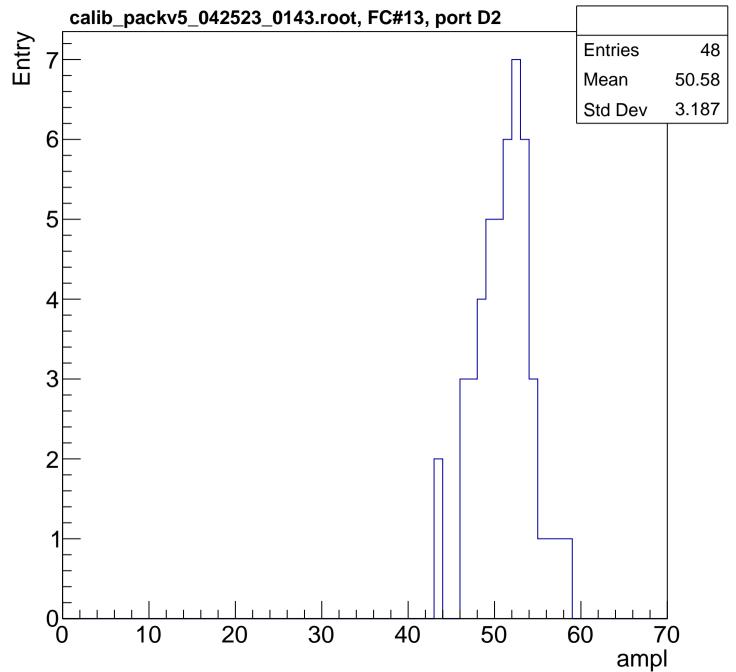
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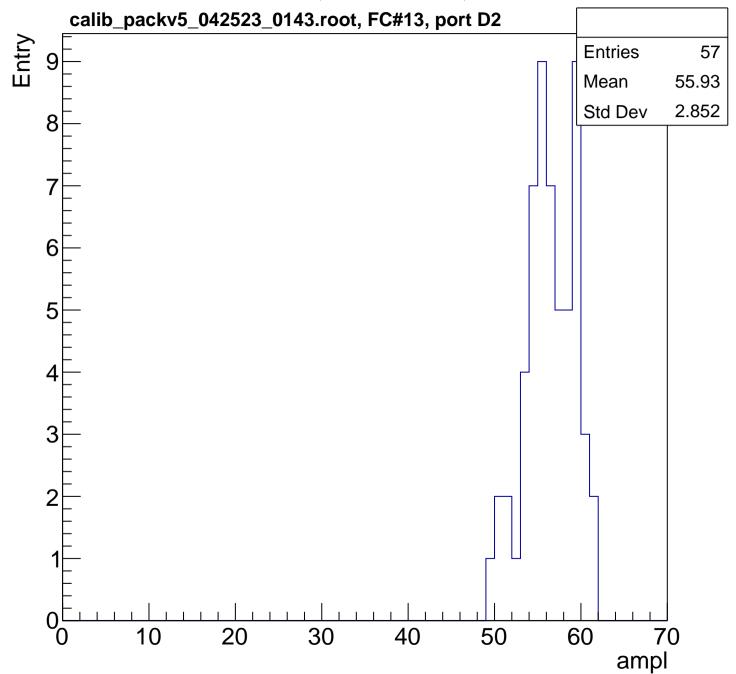


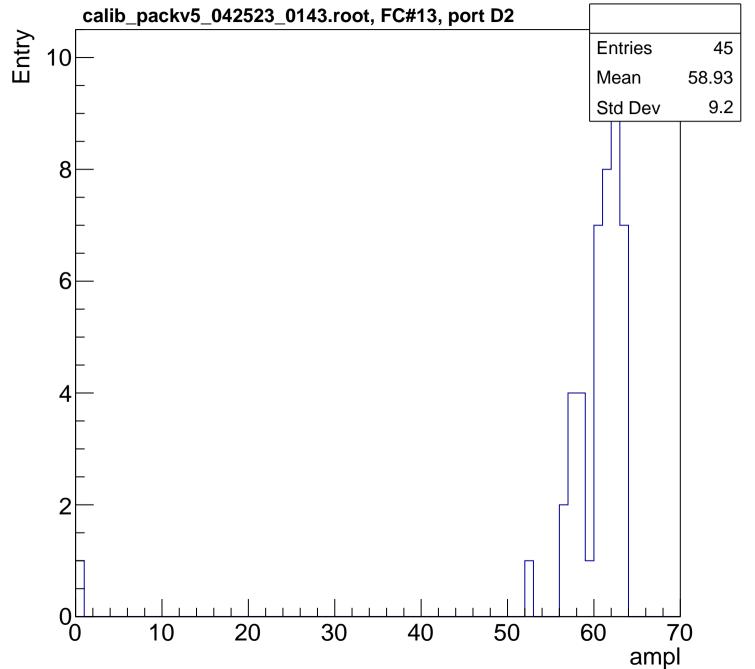


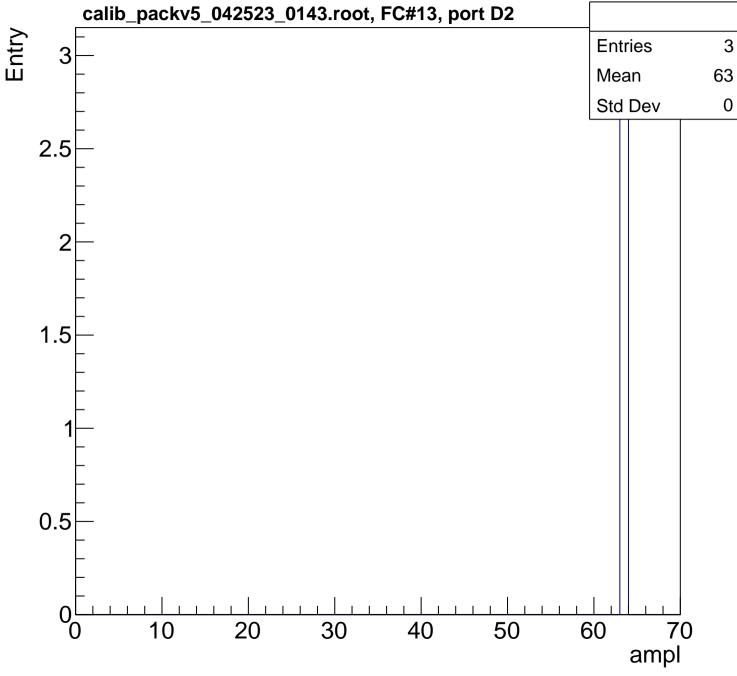




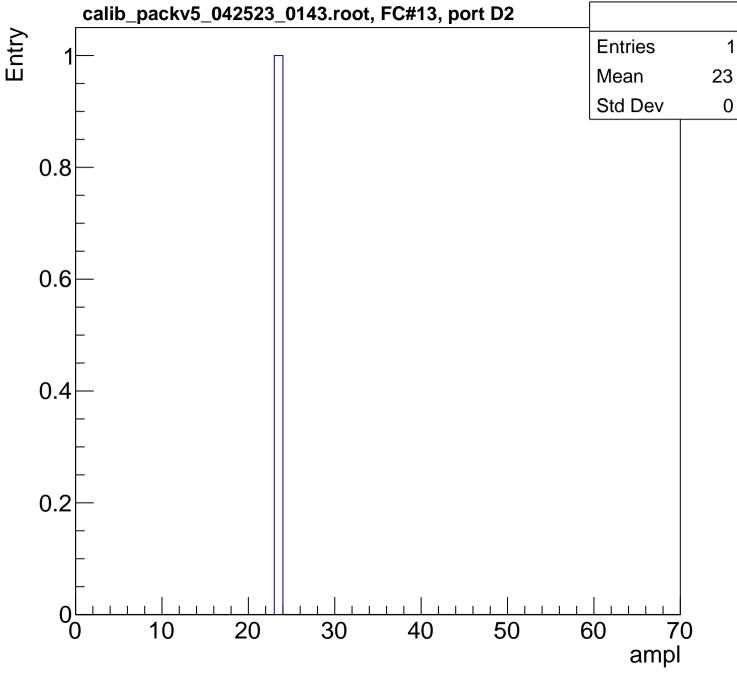


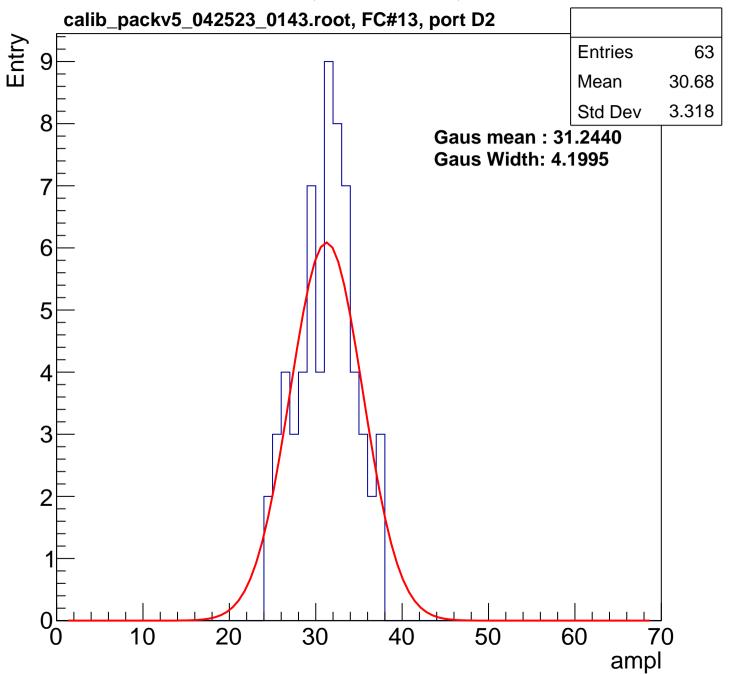


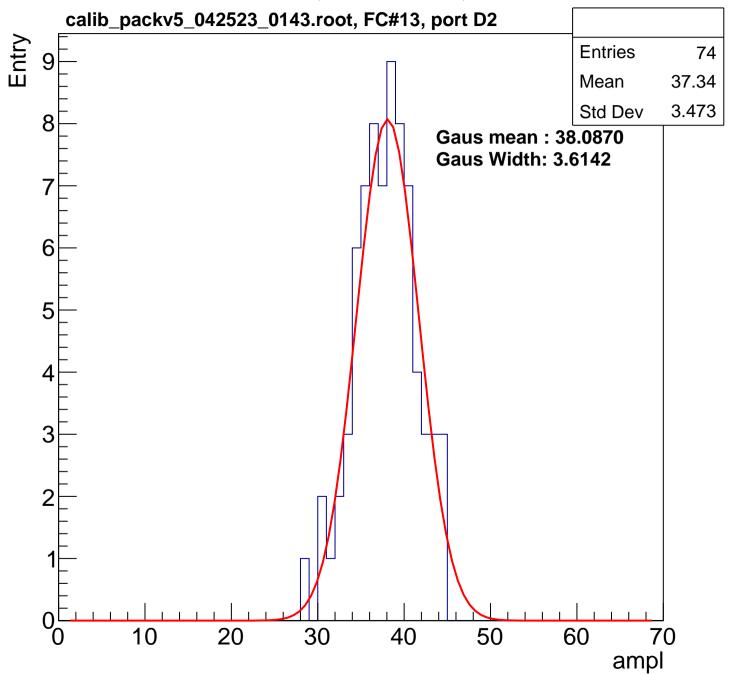


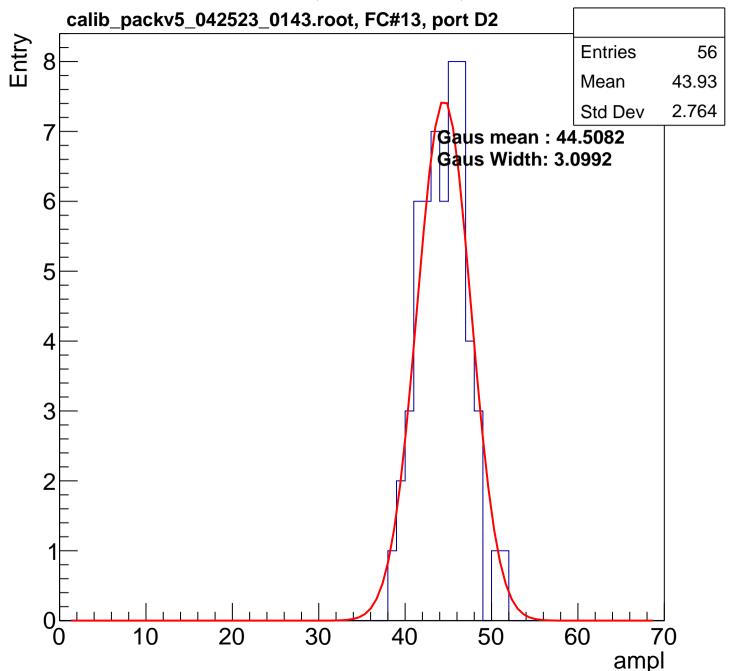


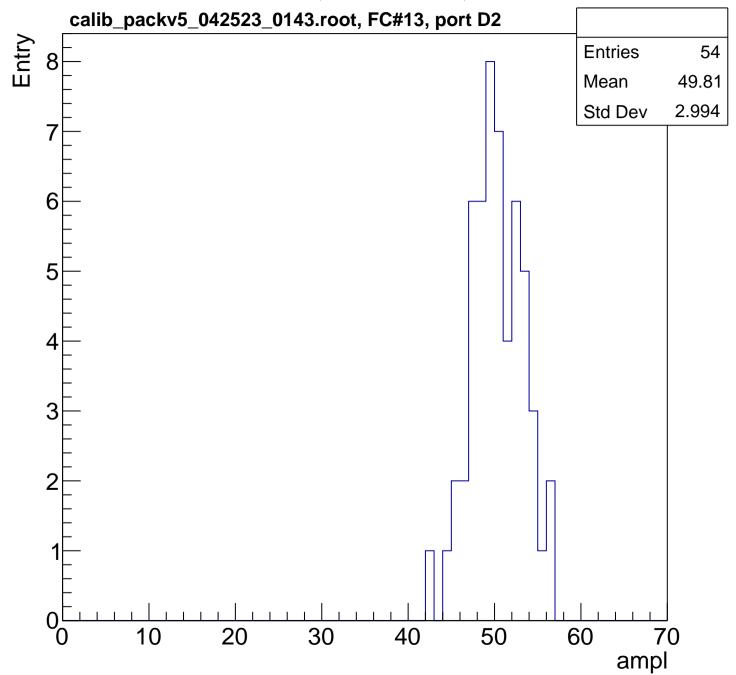
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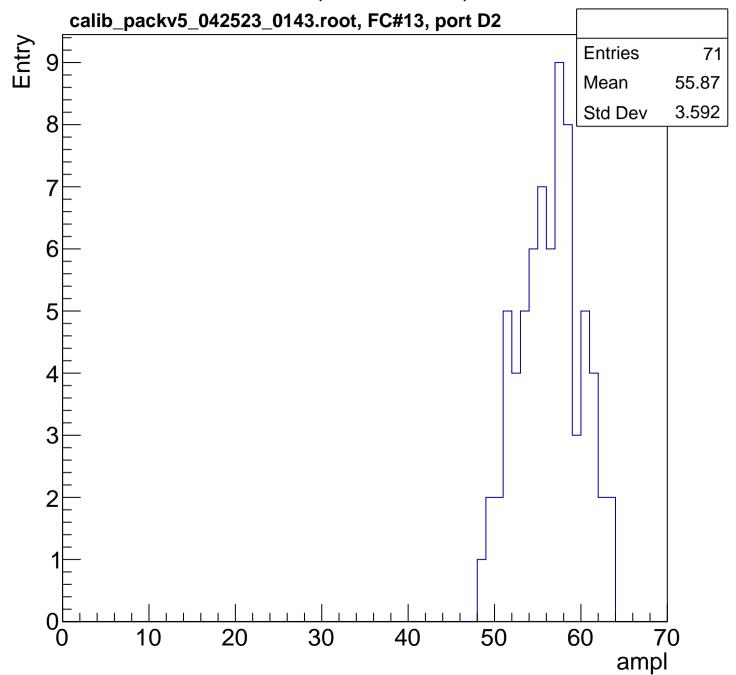


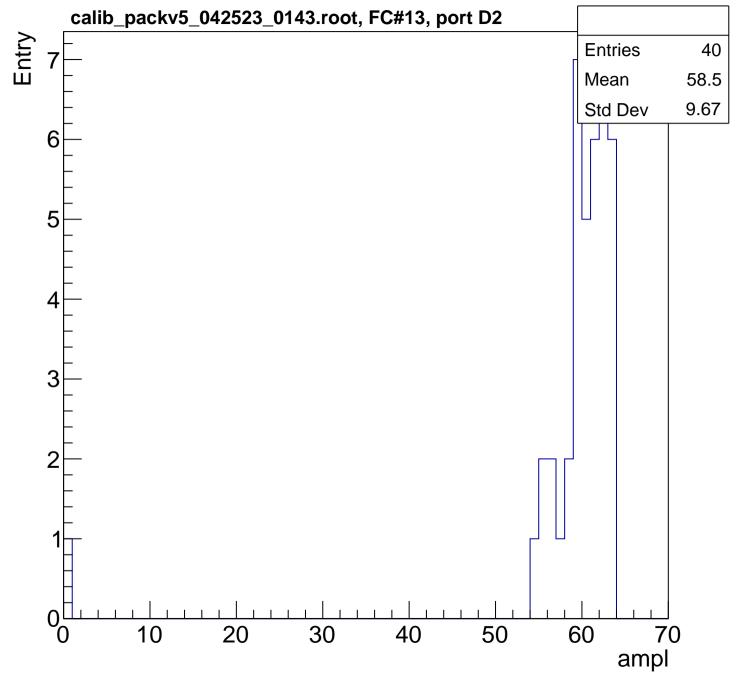


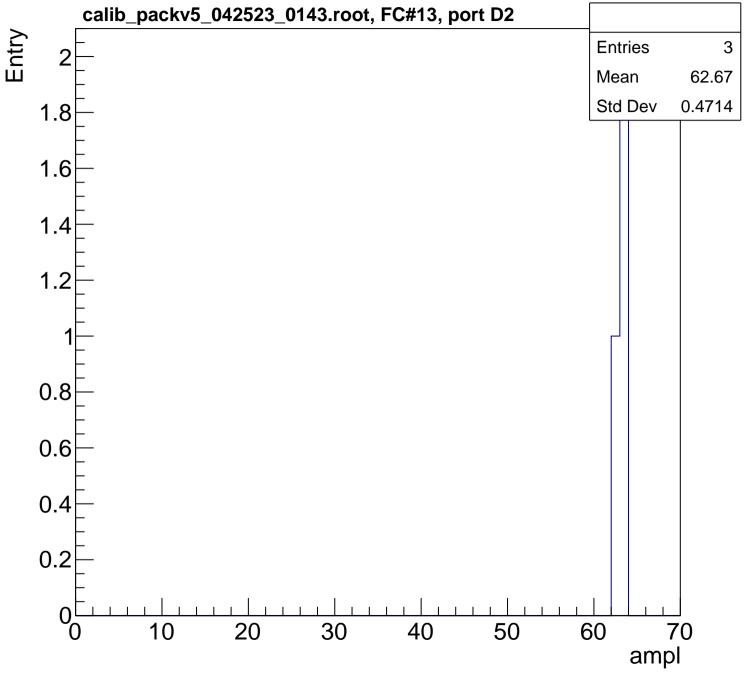




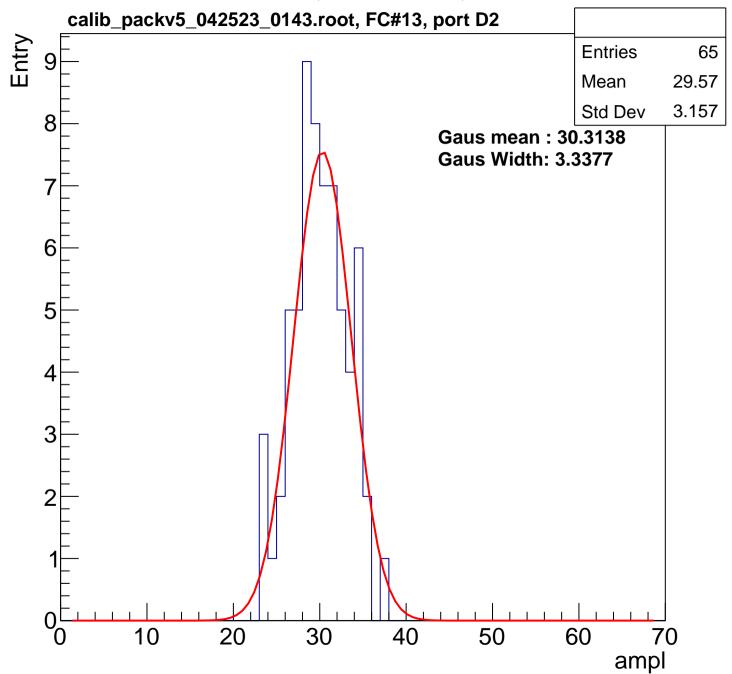


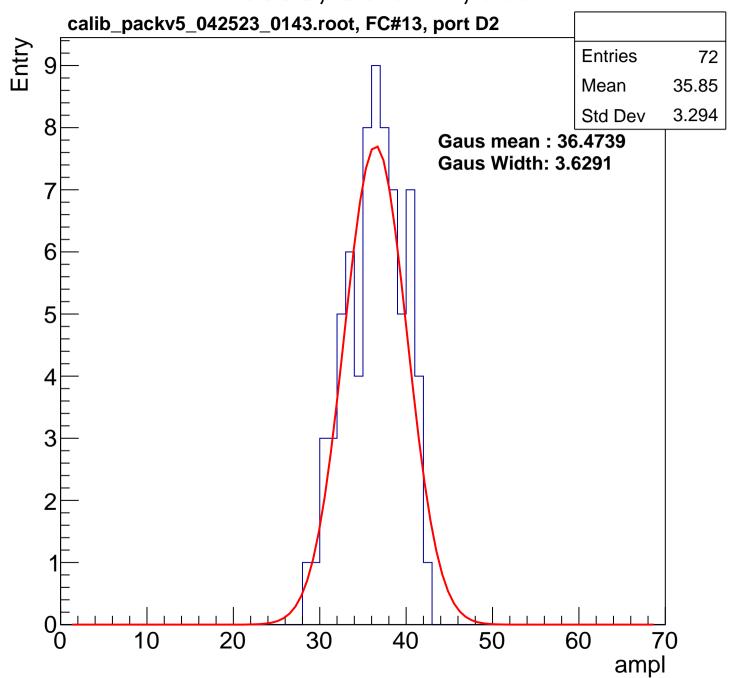


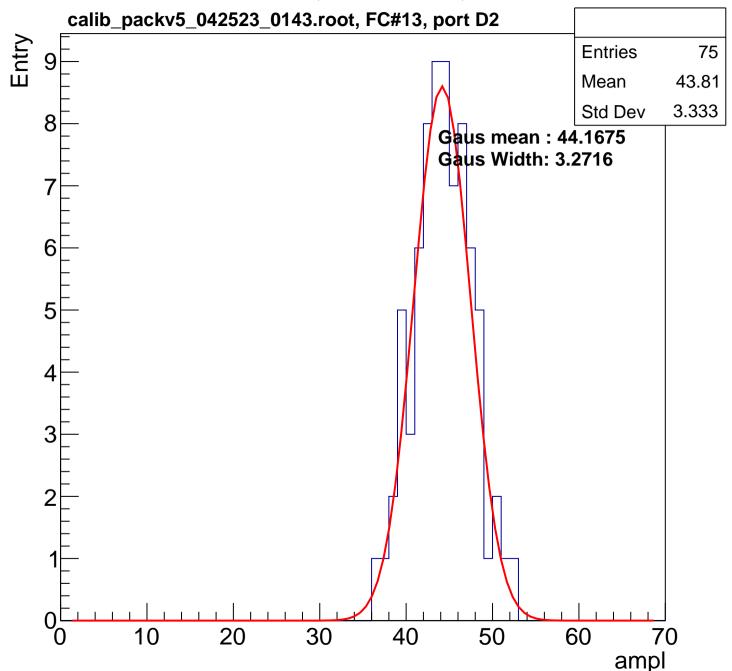


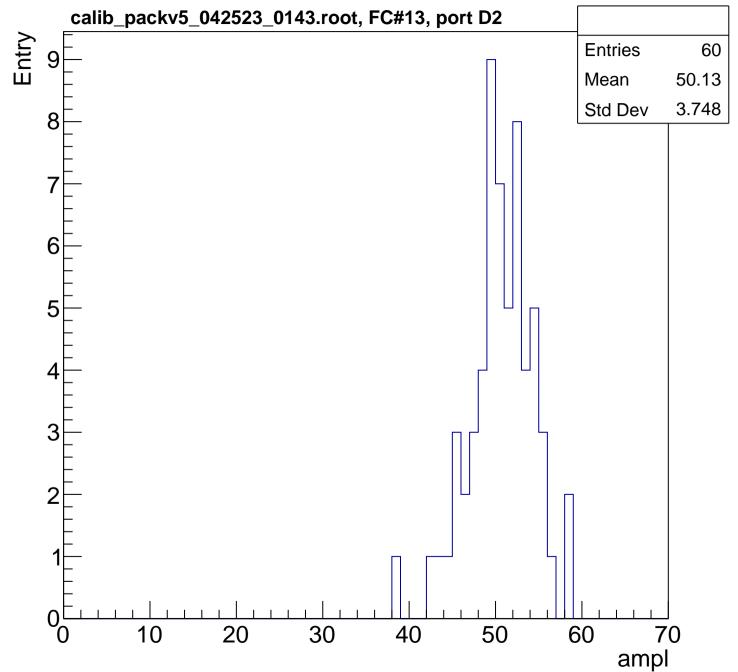


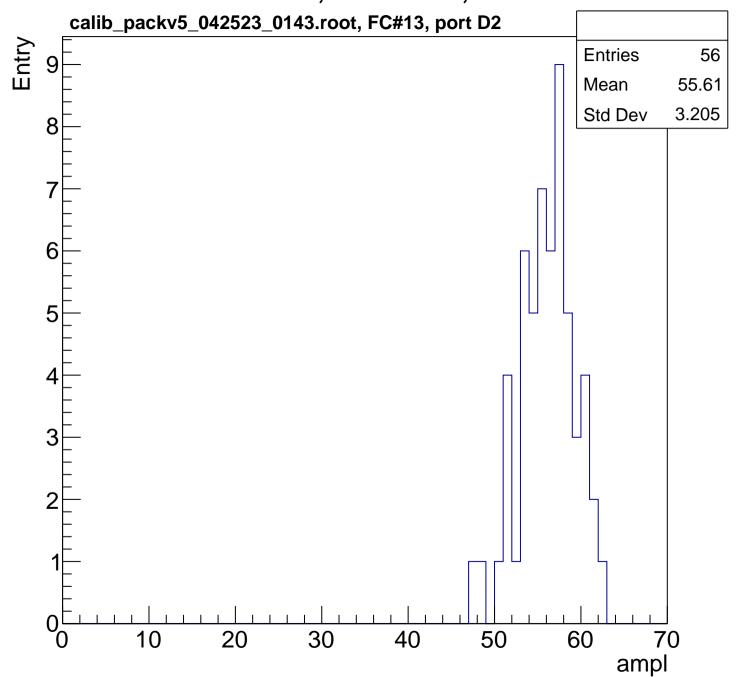


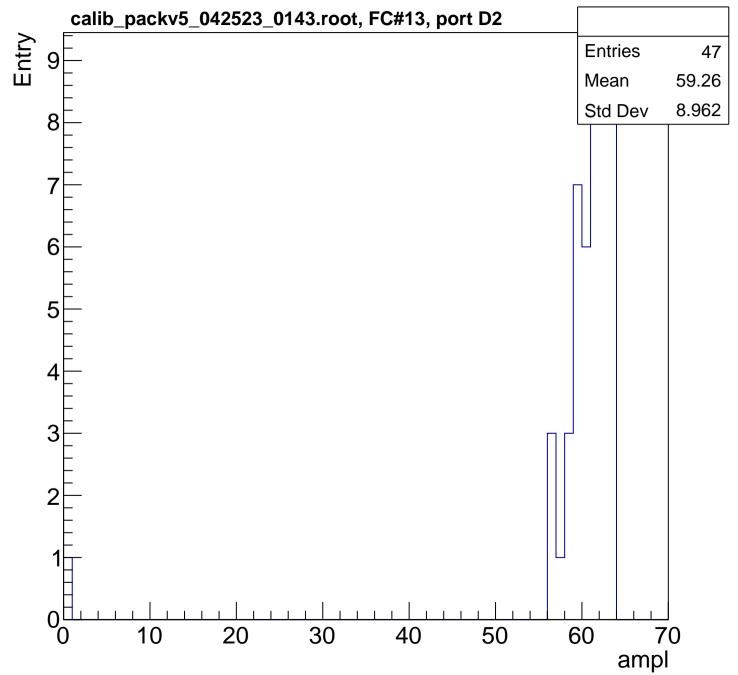


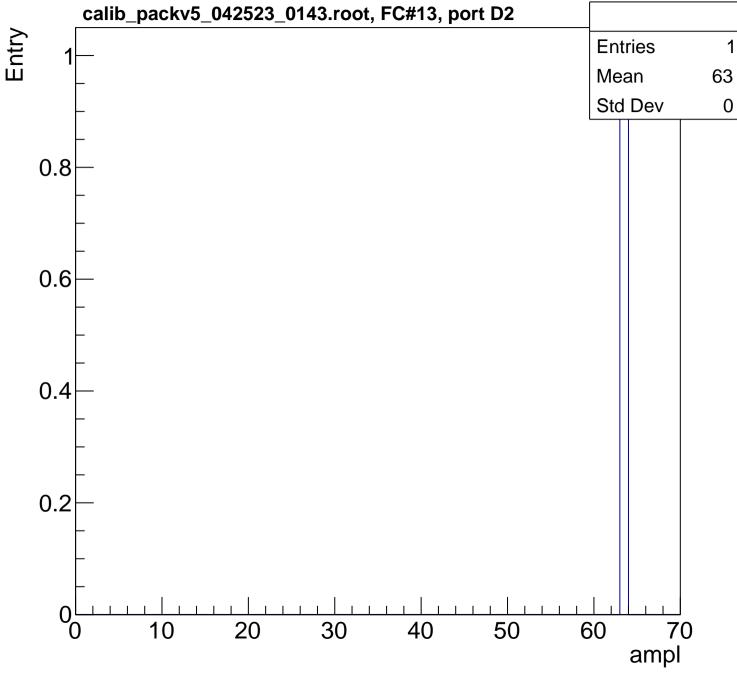




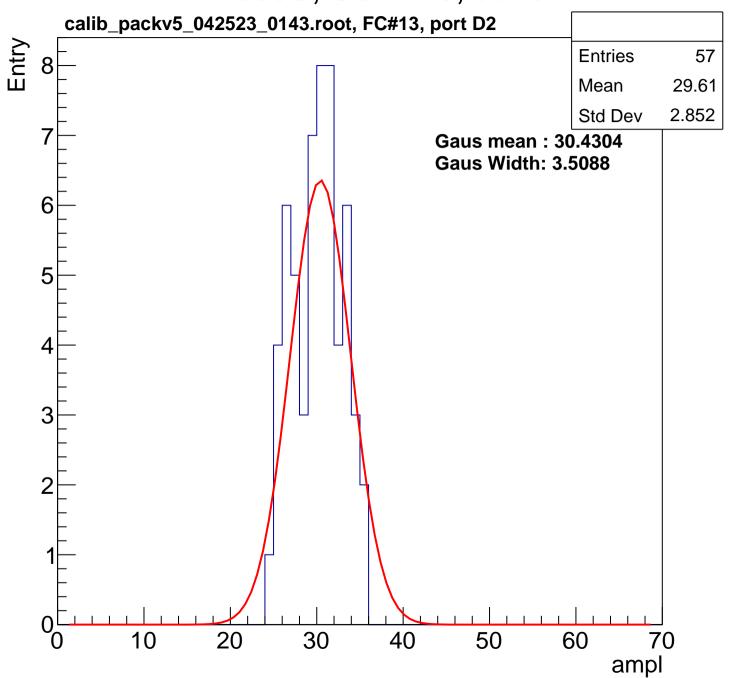


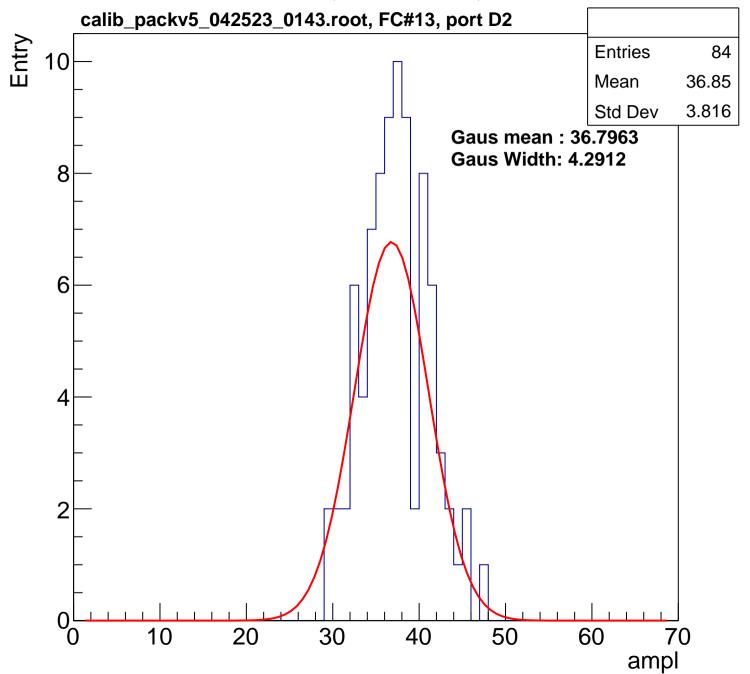


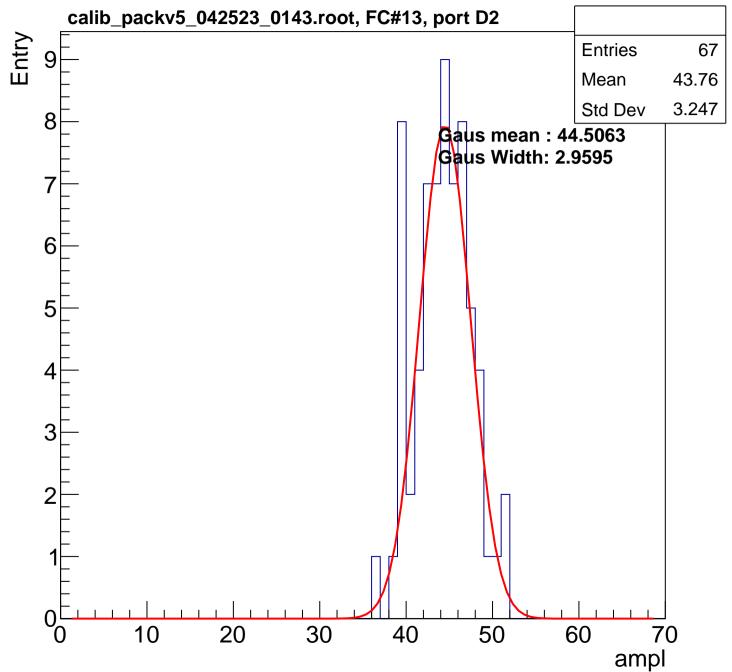


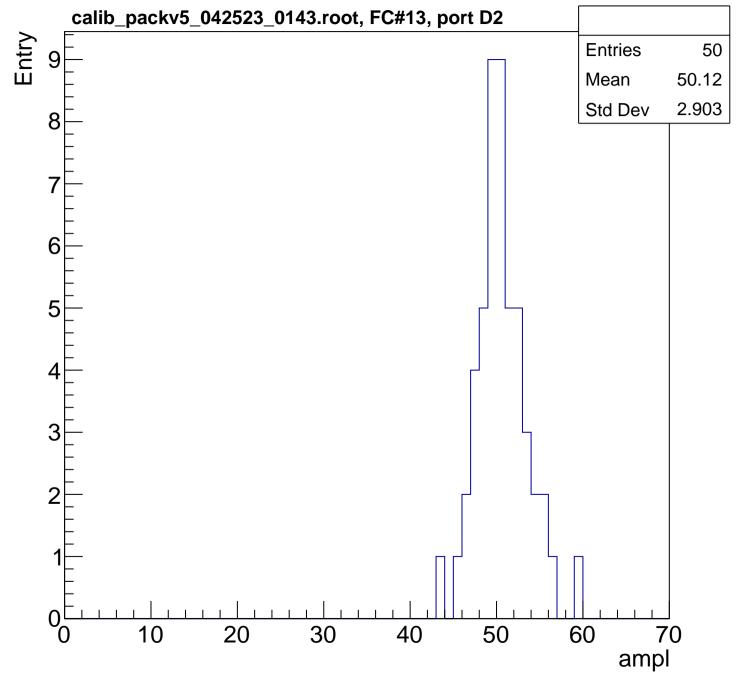


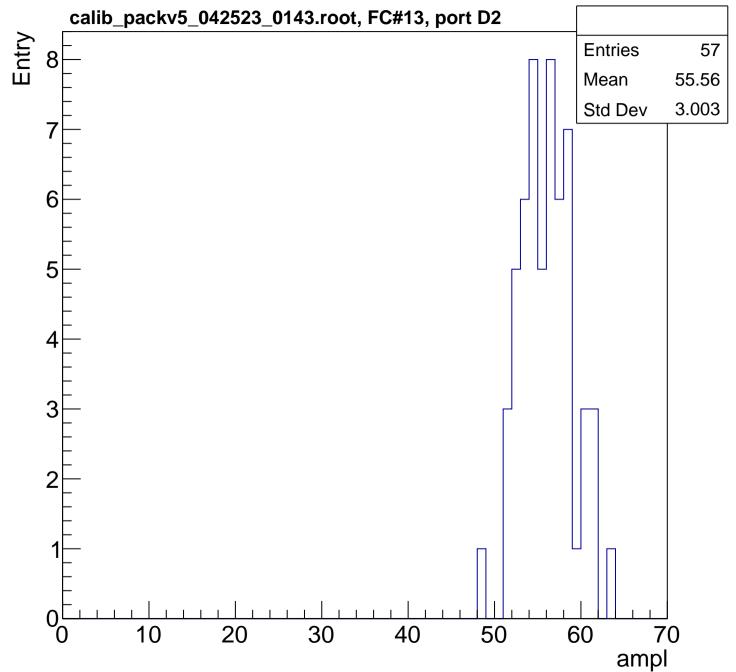


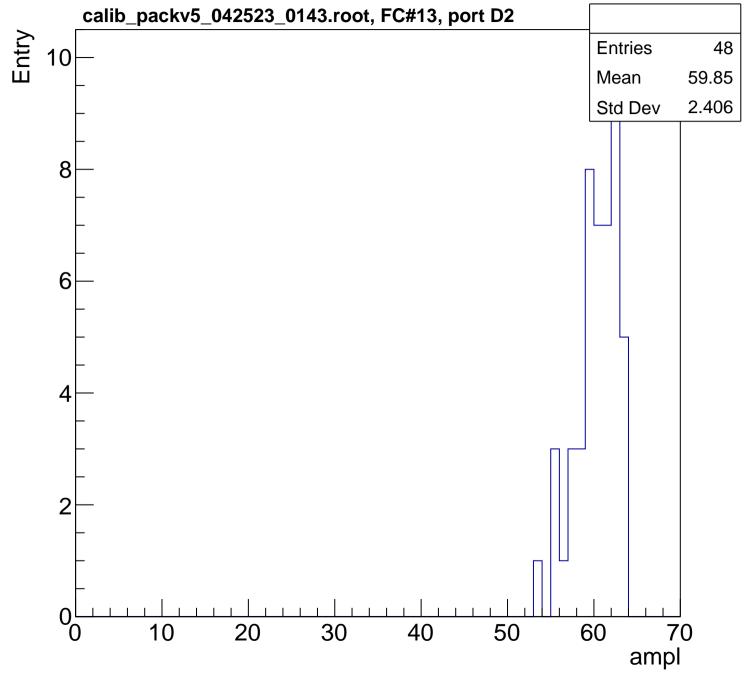


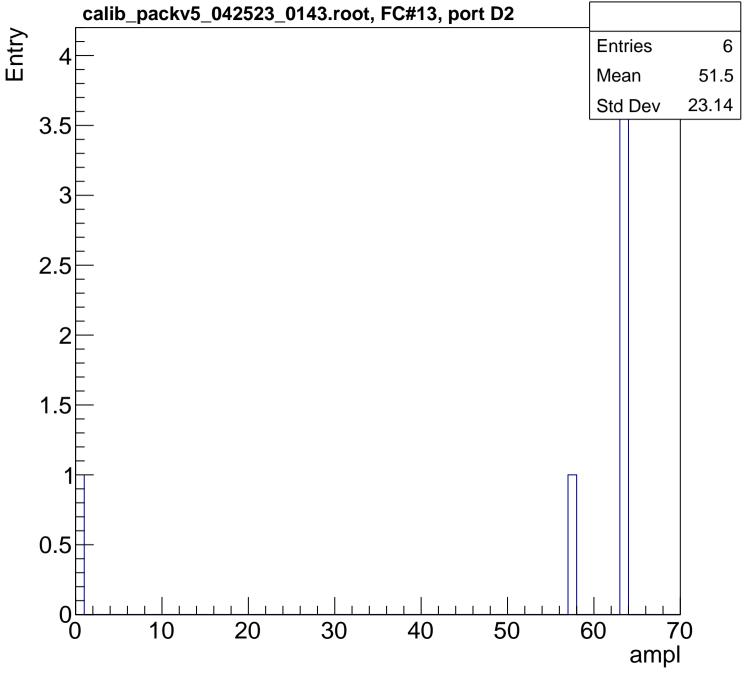




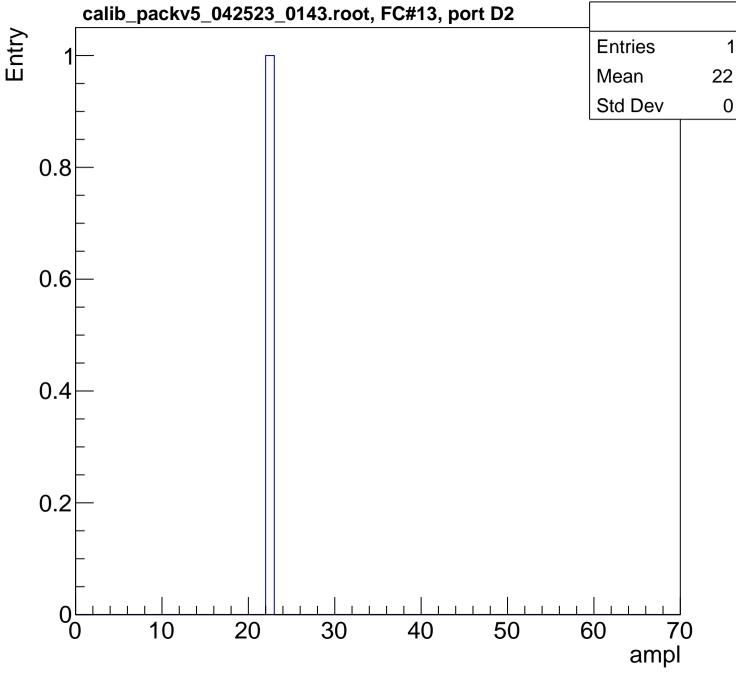


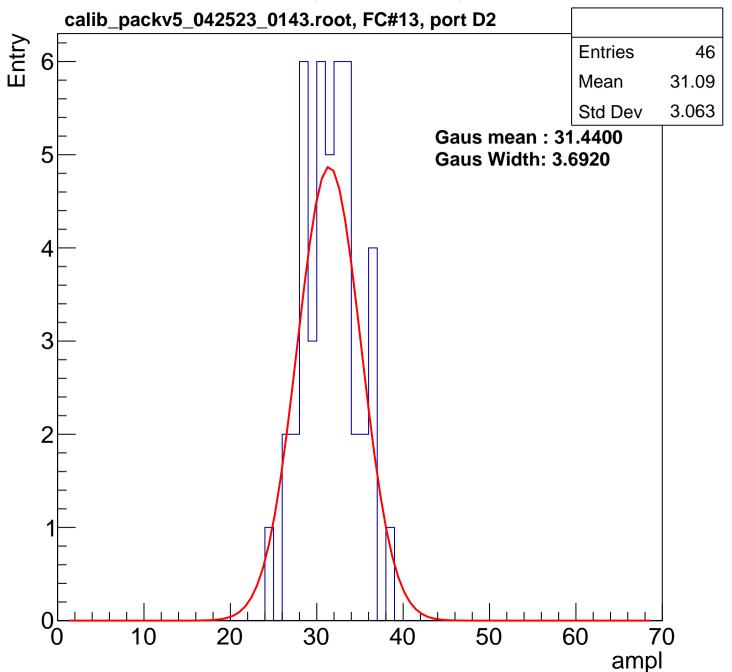


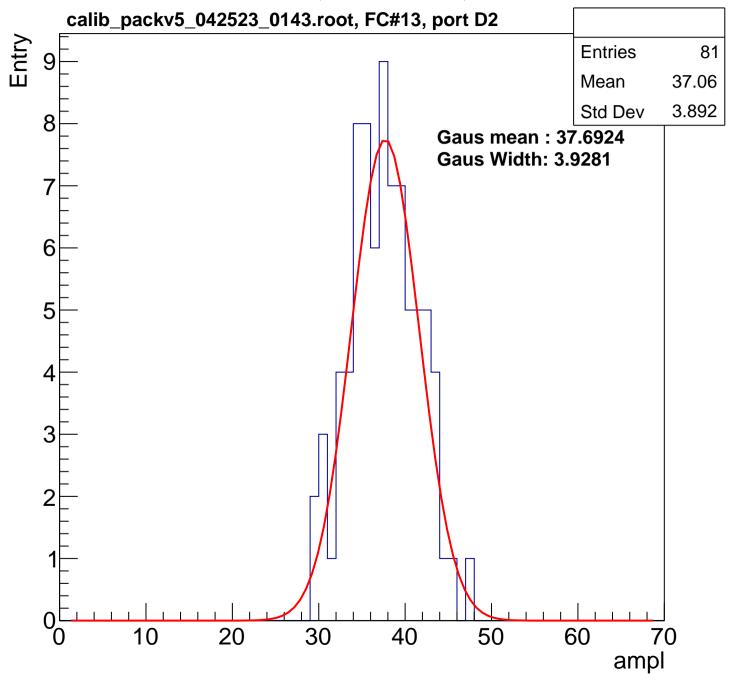


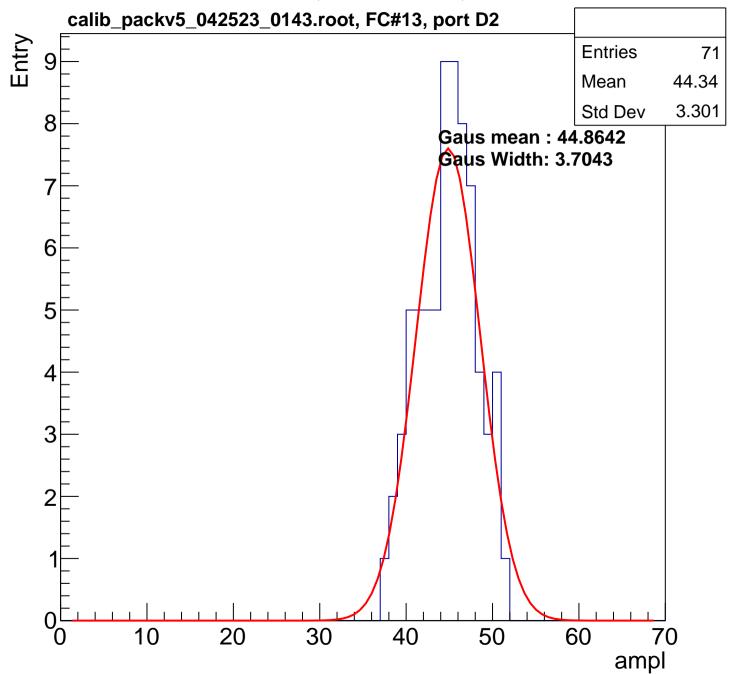


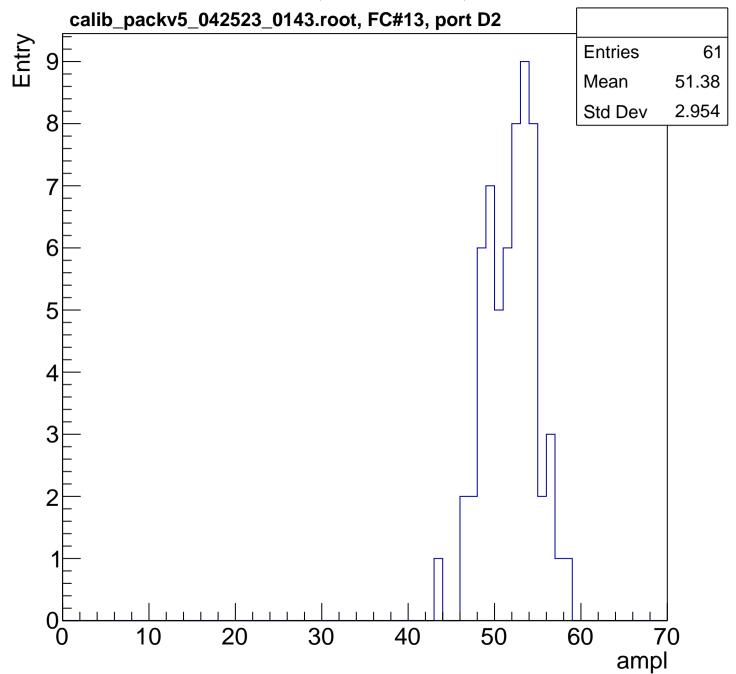
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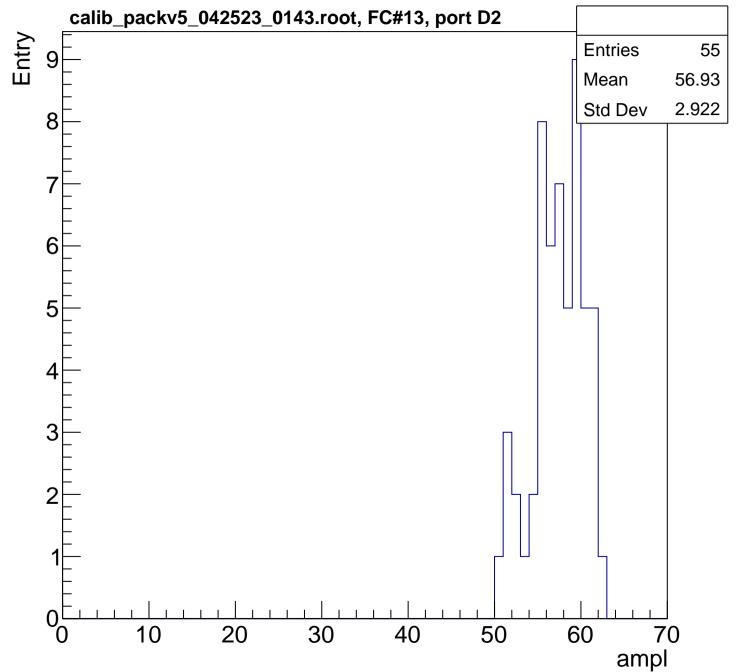


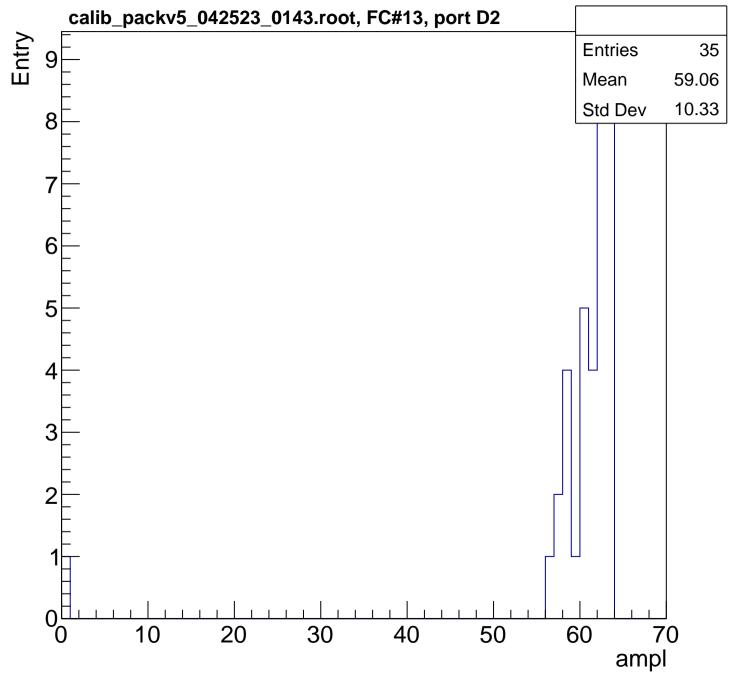


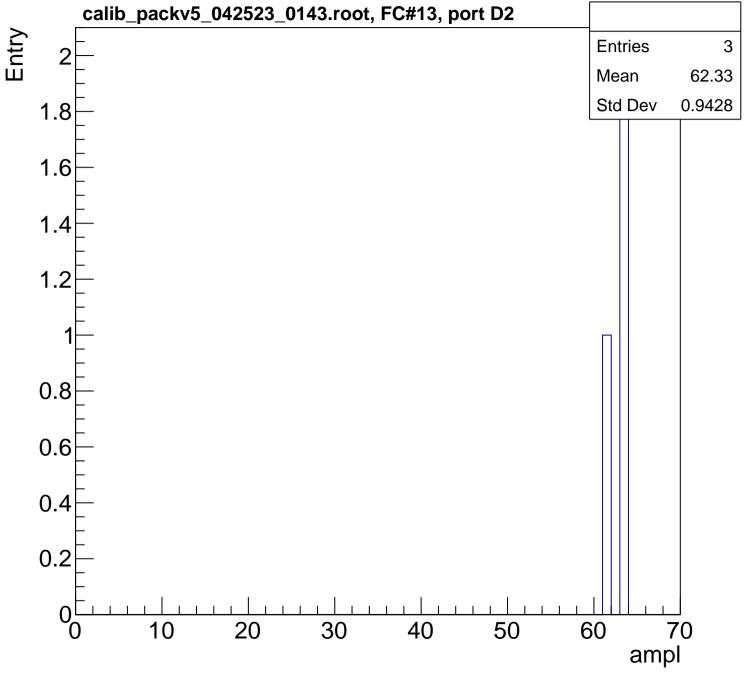


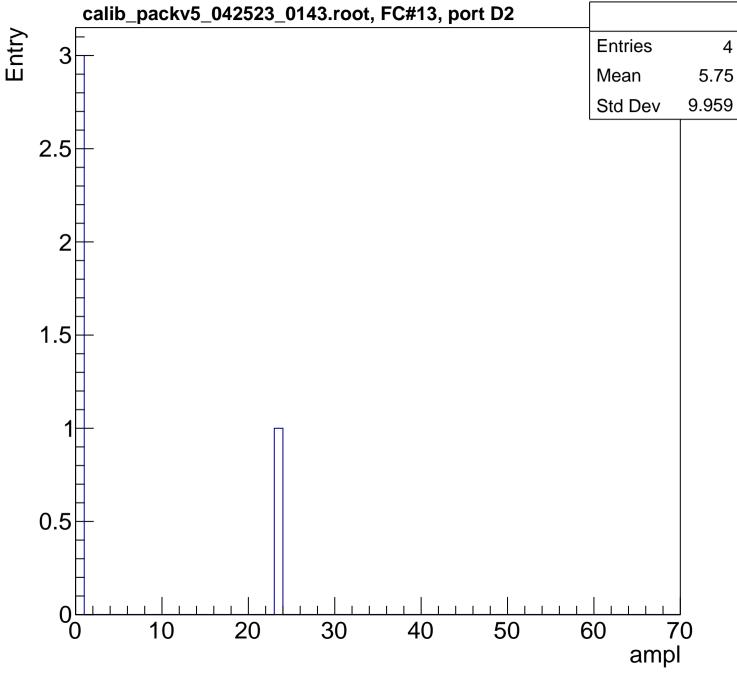


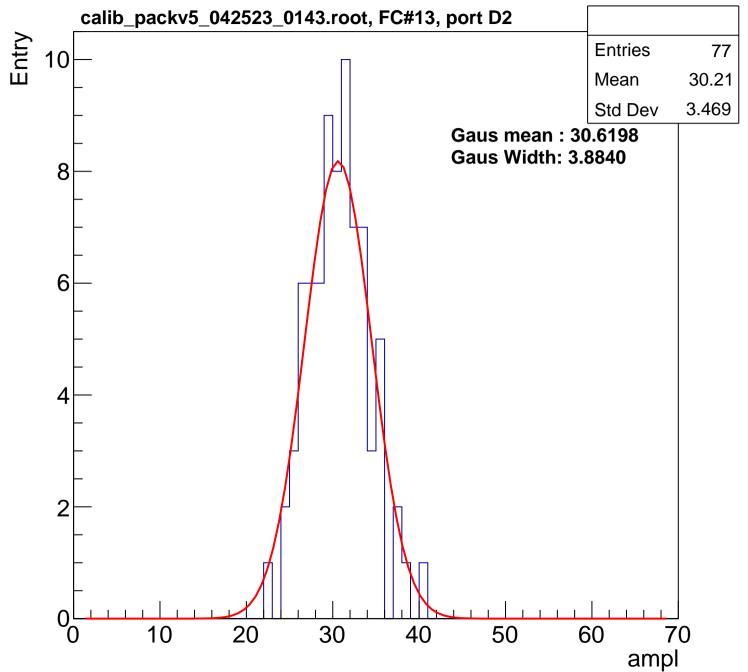


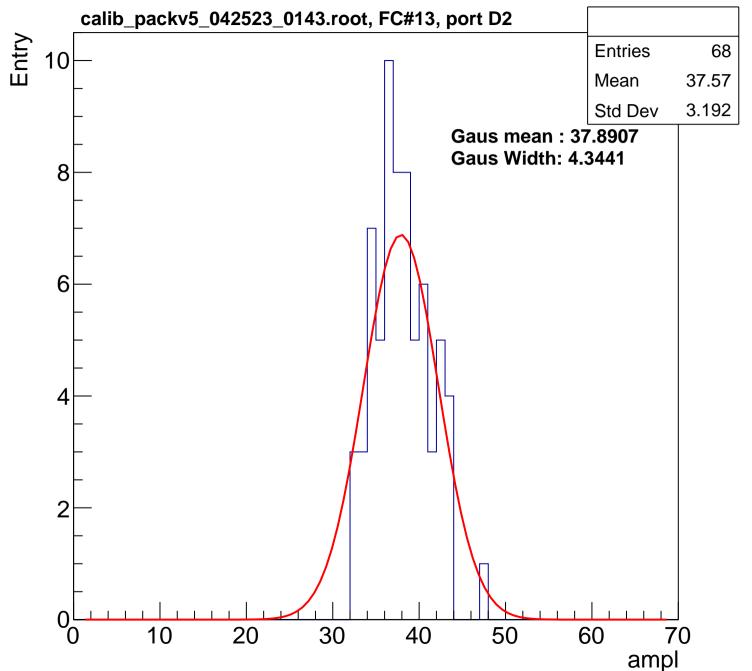


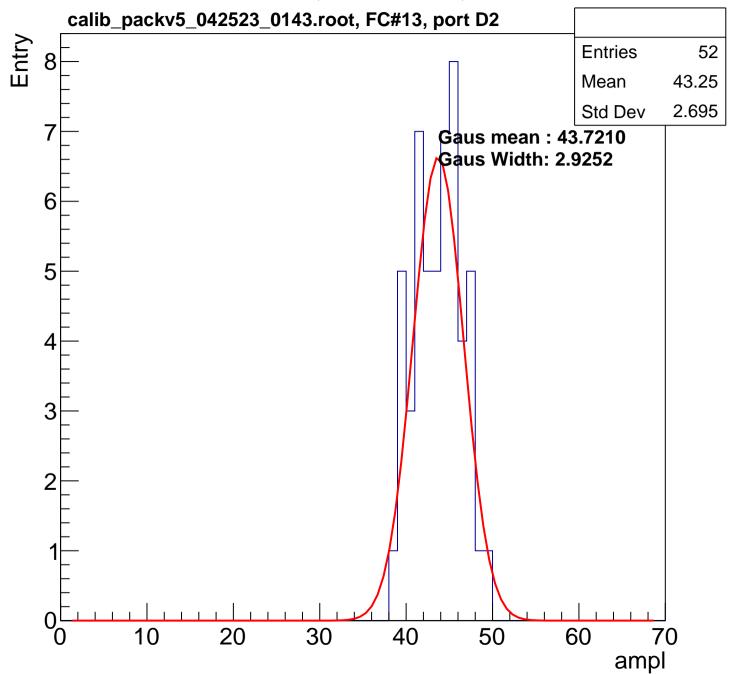


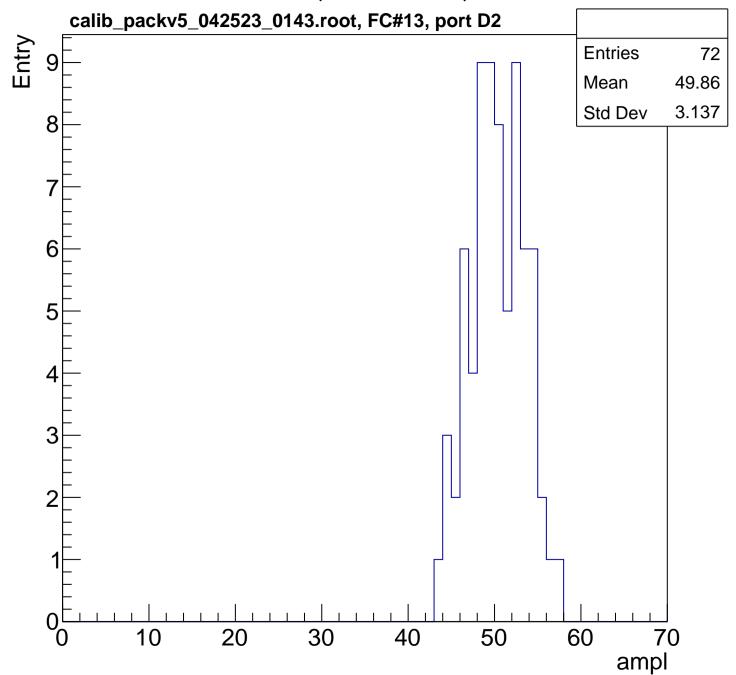


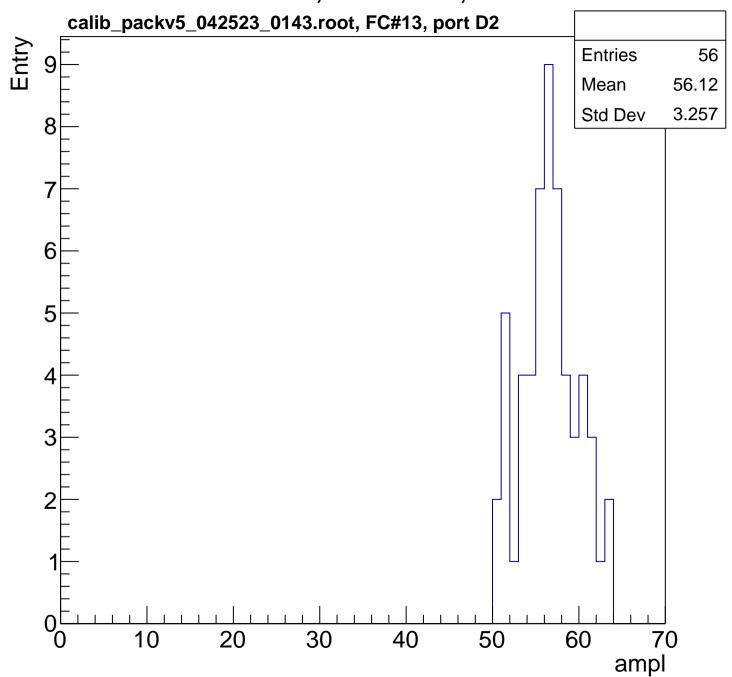


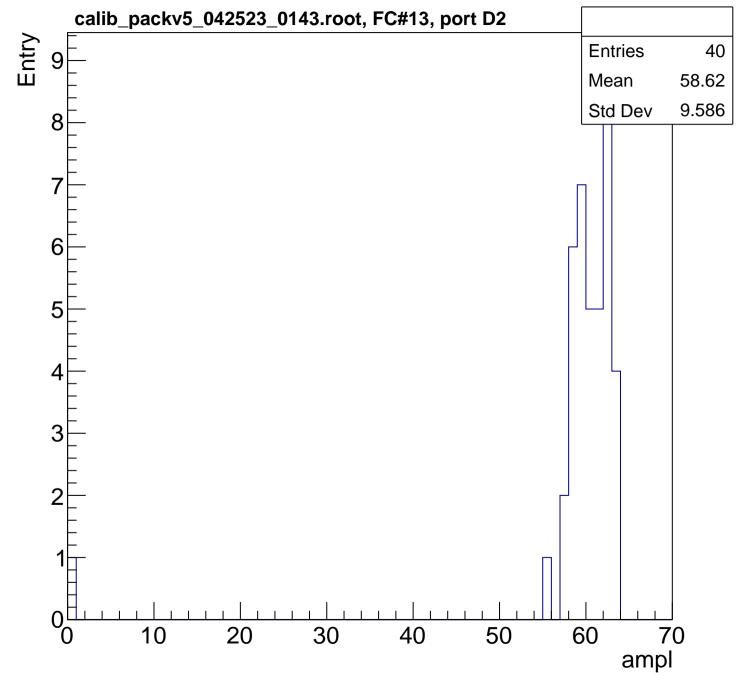


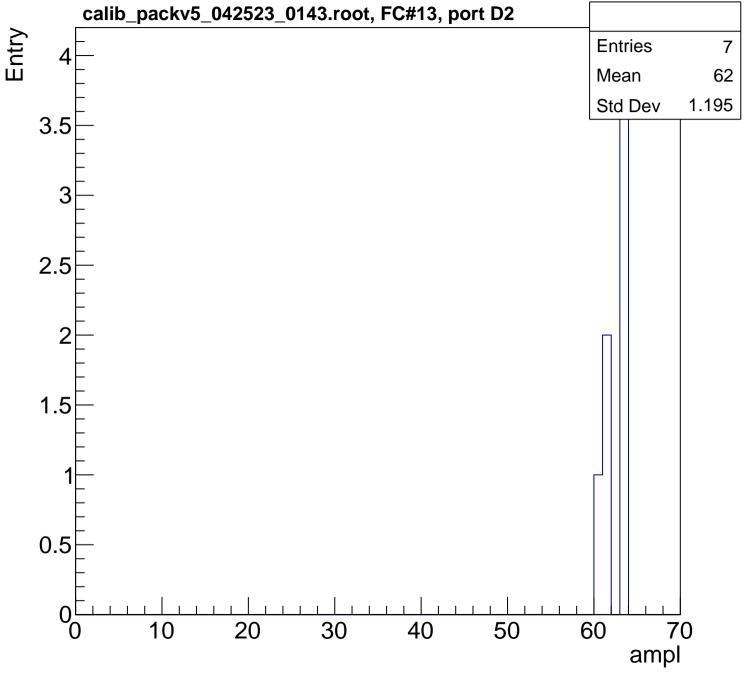


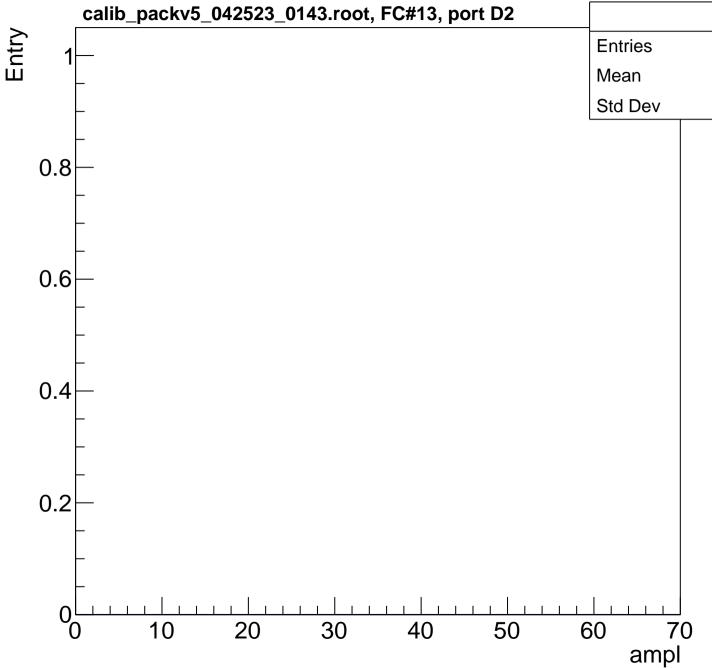


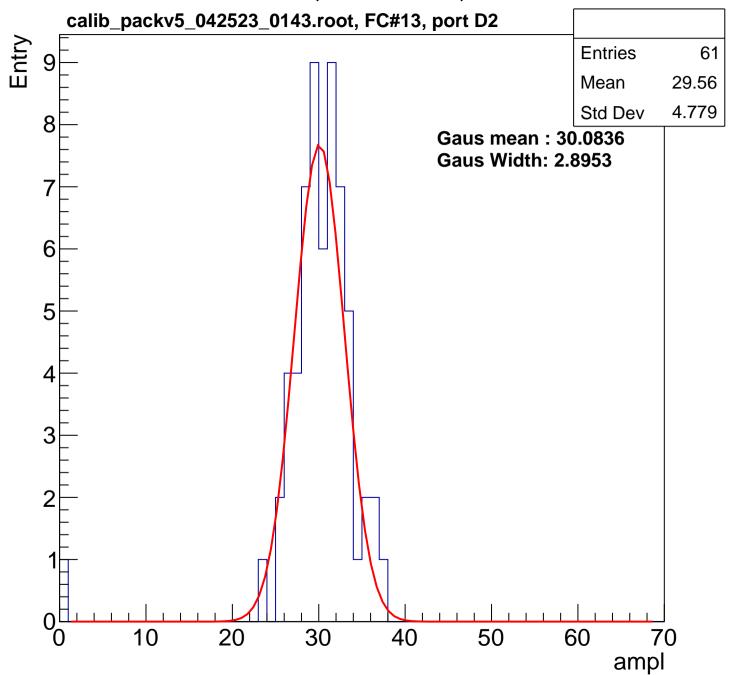


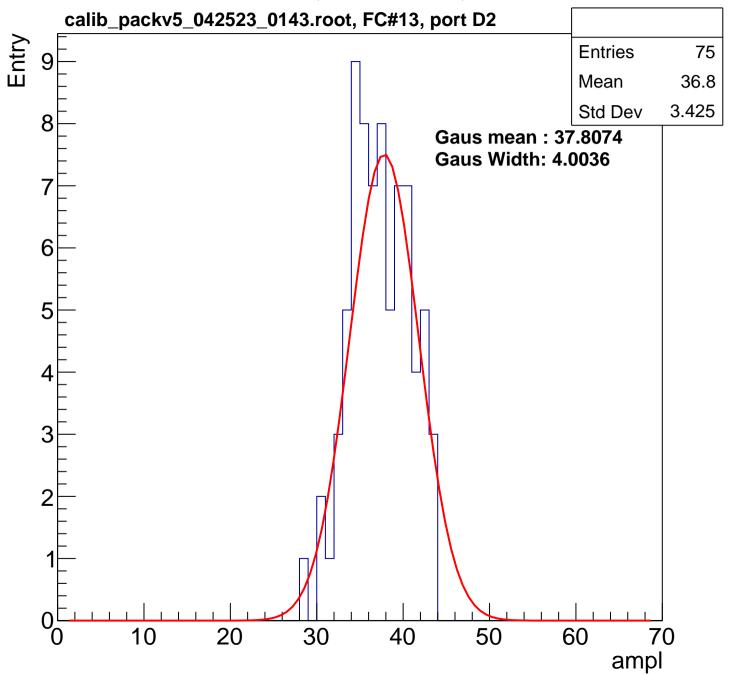


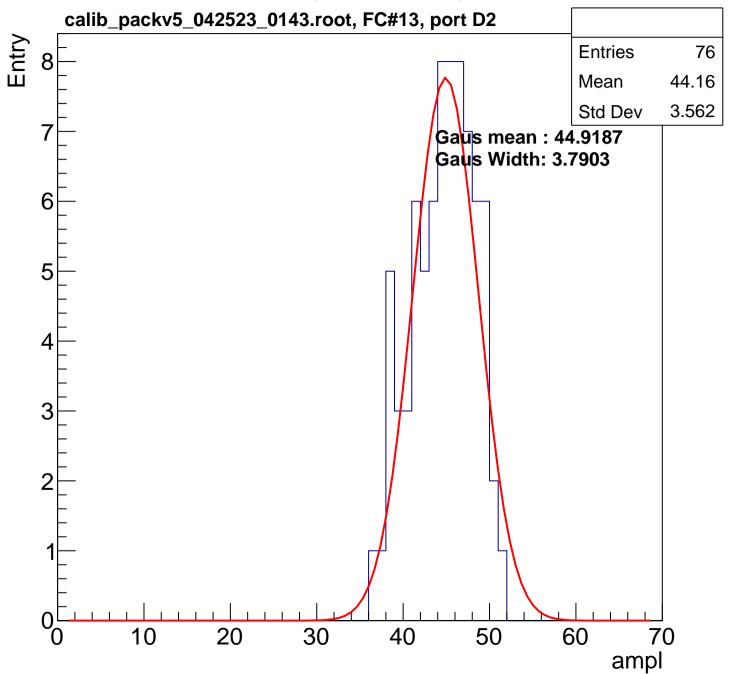


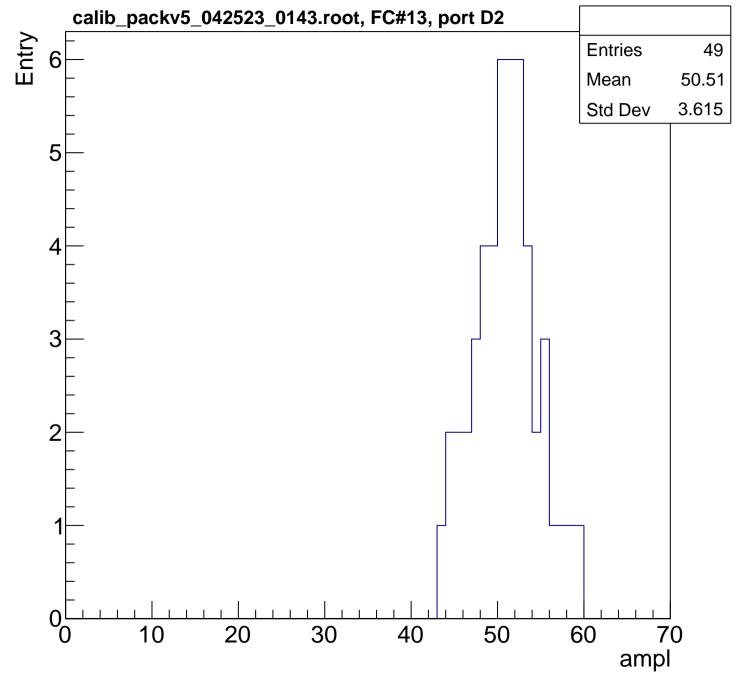


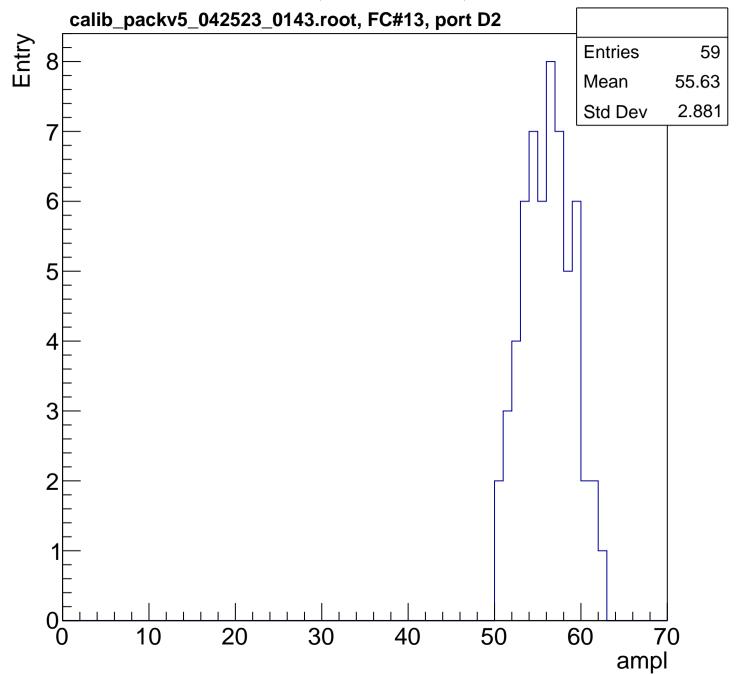


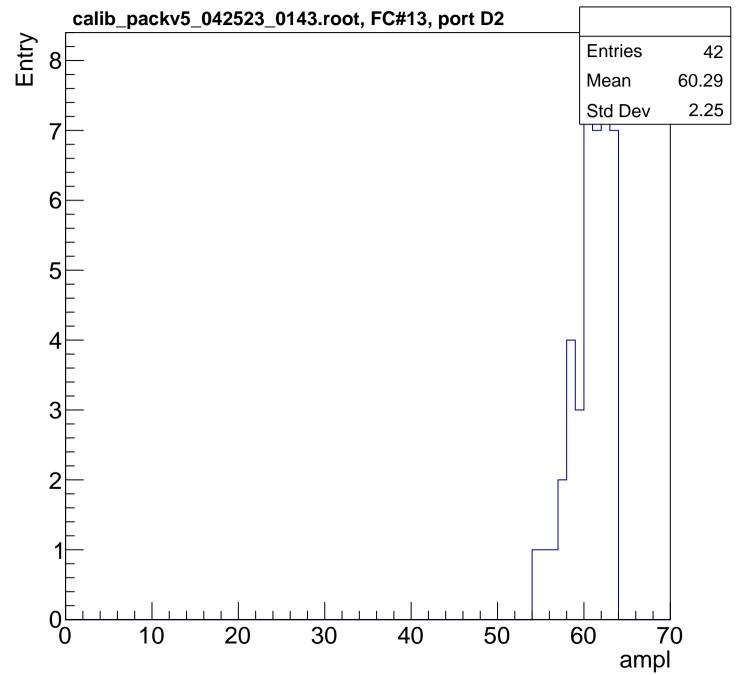


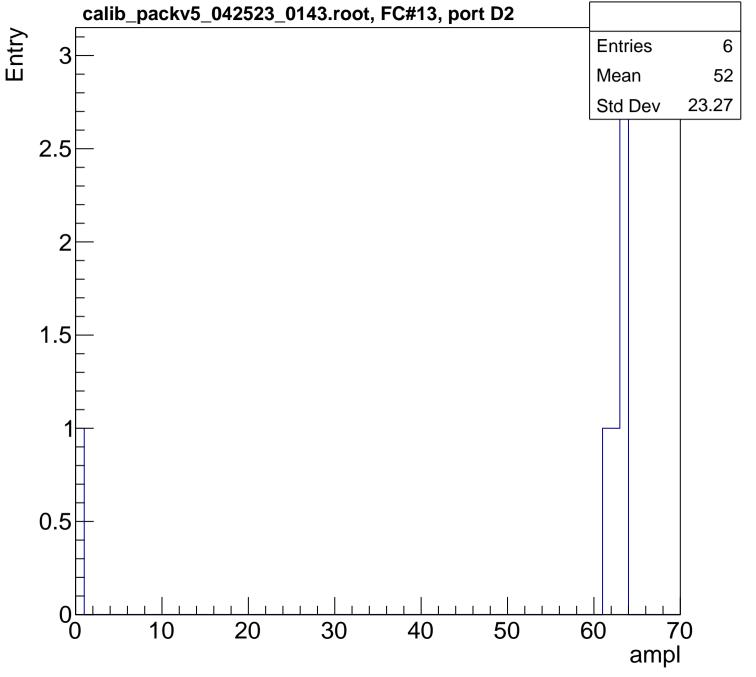




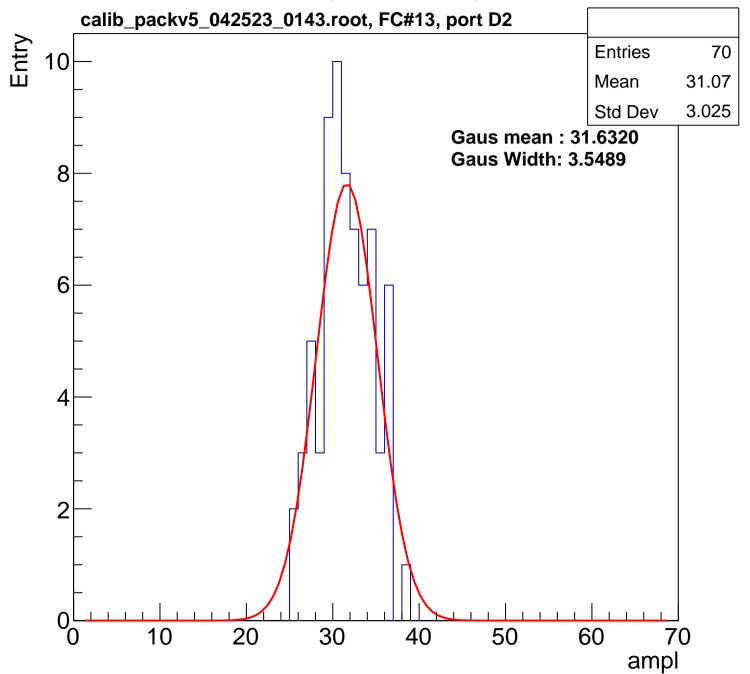


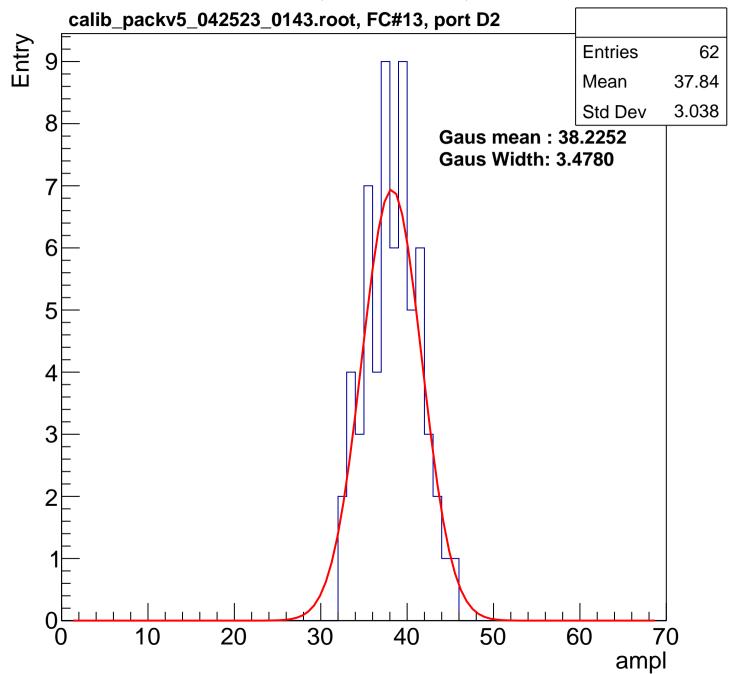


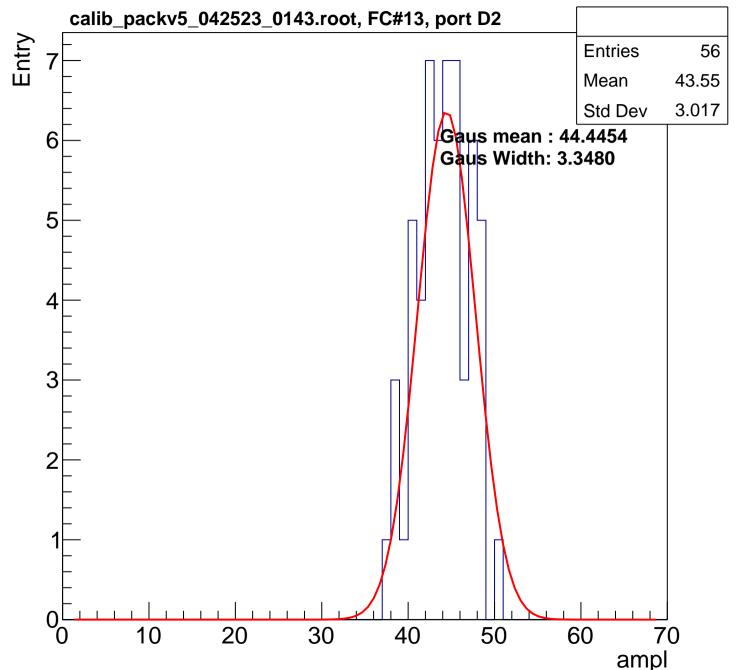


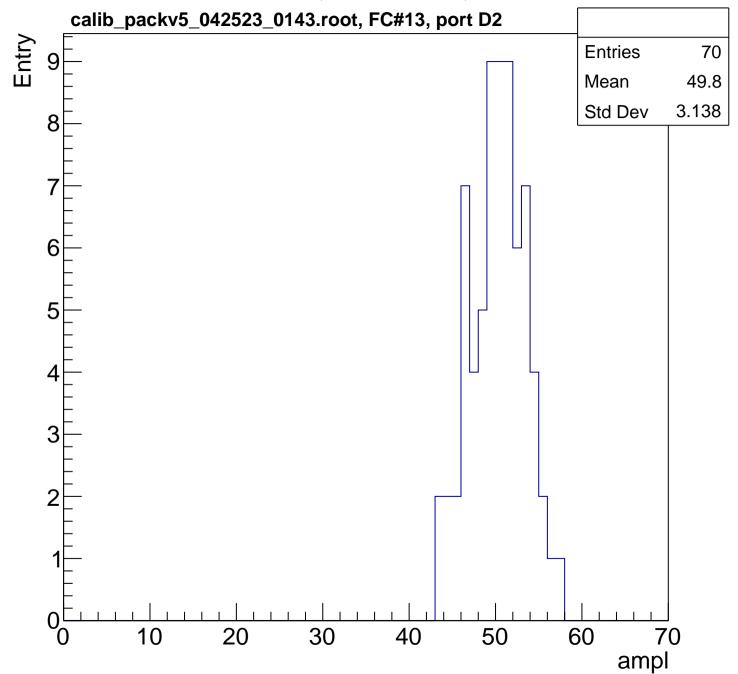


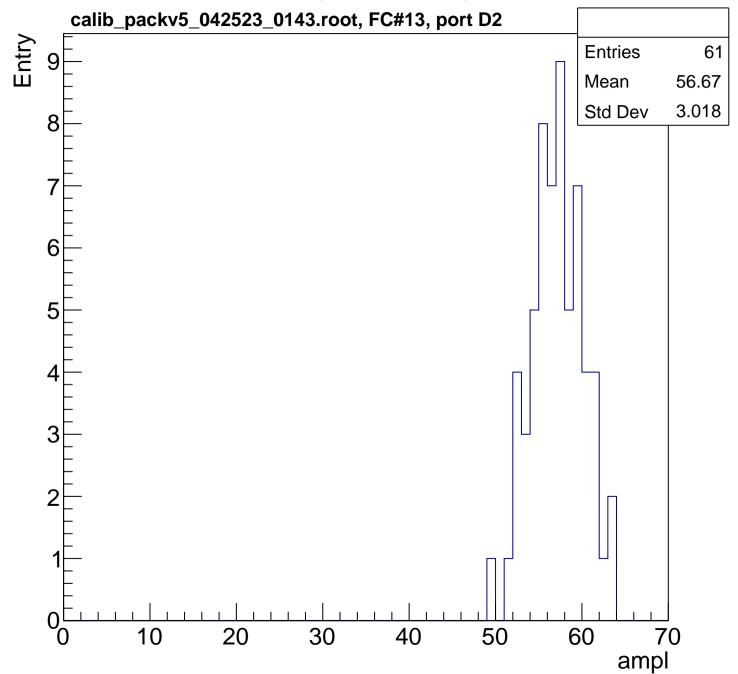
B1L003S, U9-ch31, adc7 calib\_packv5\_042523\_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

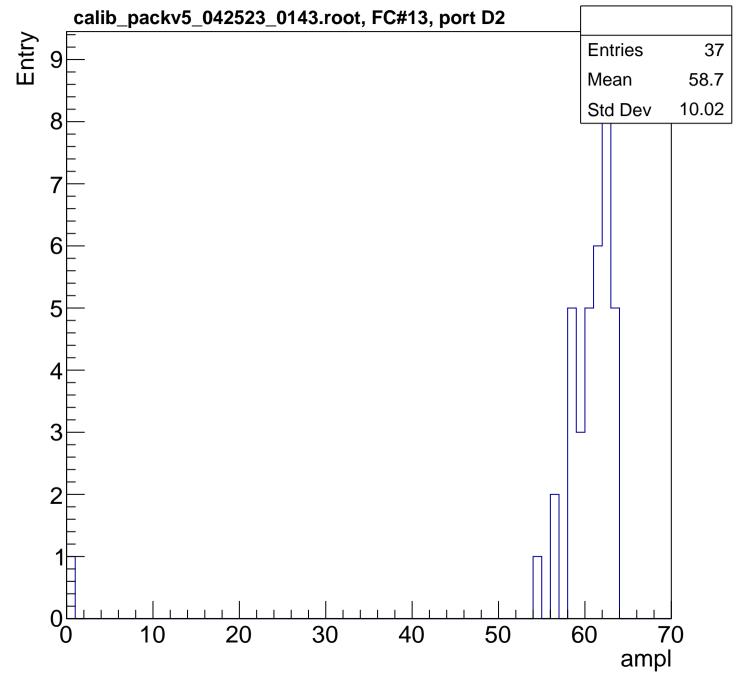


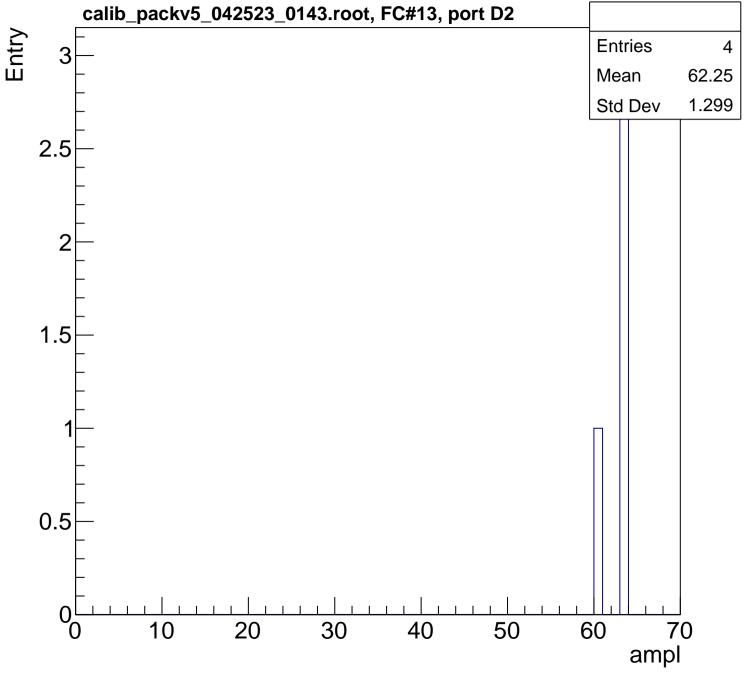




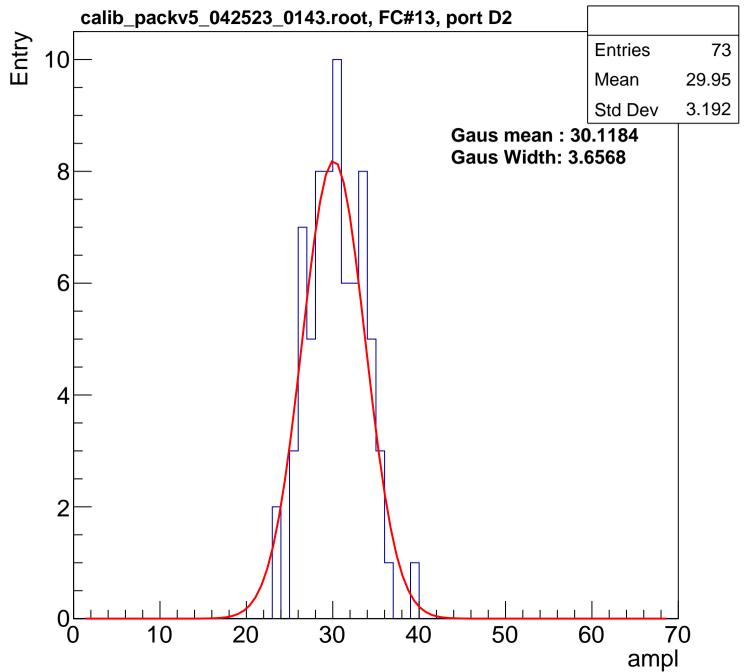


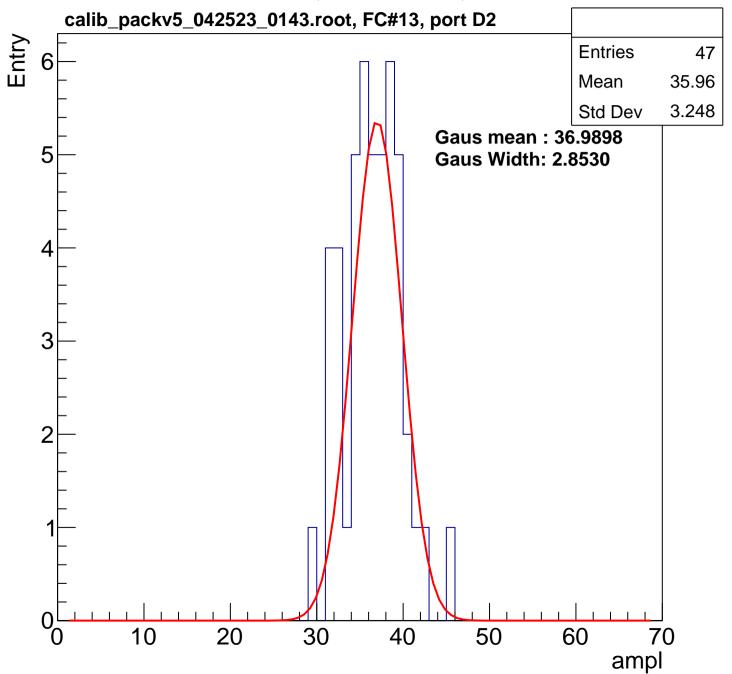


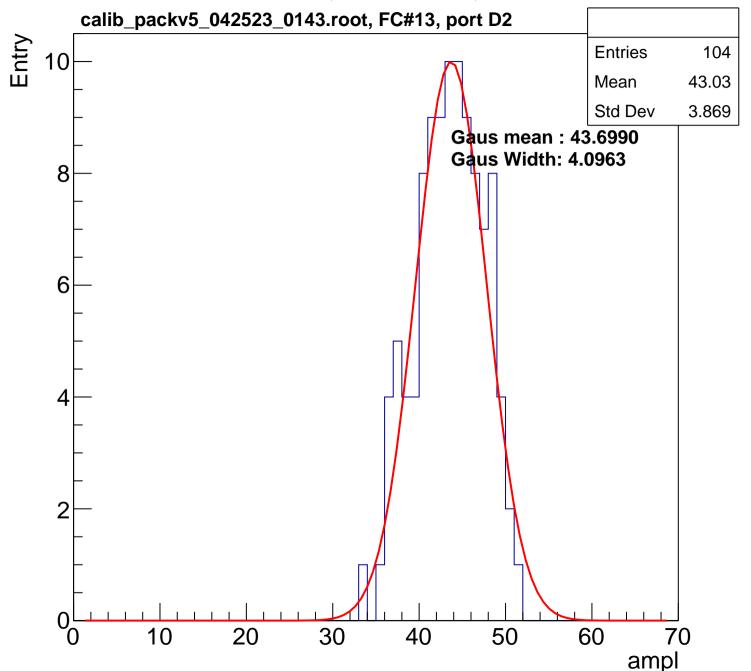


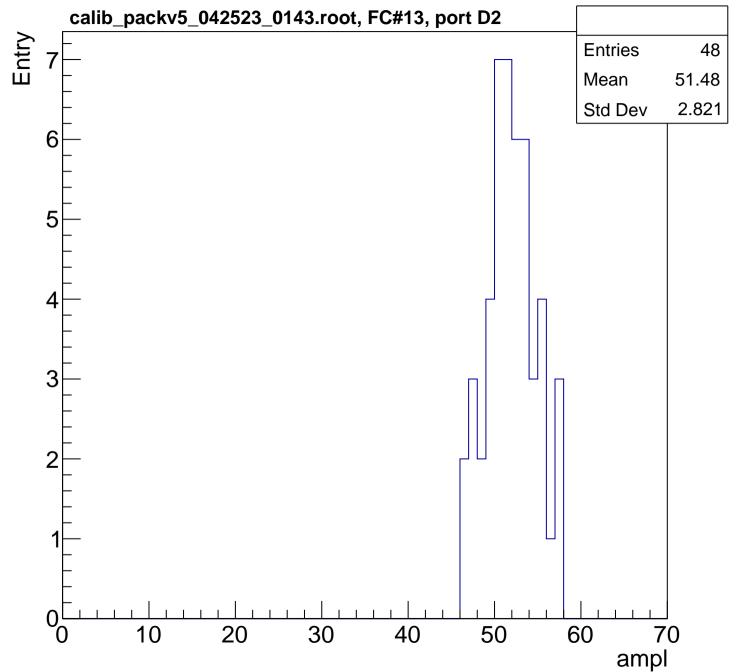


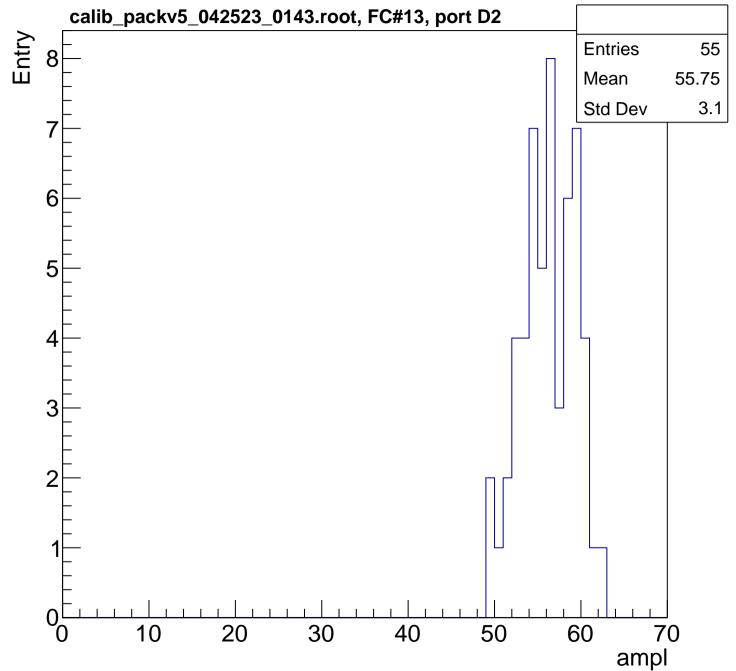
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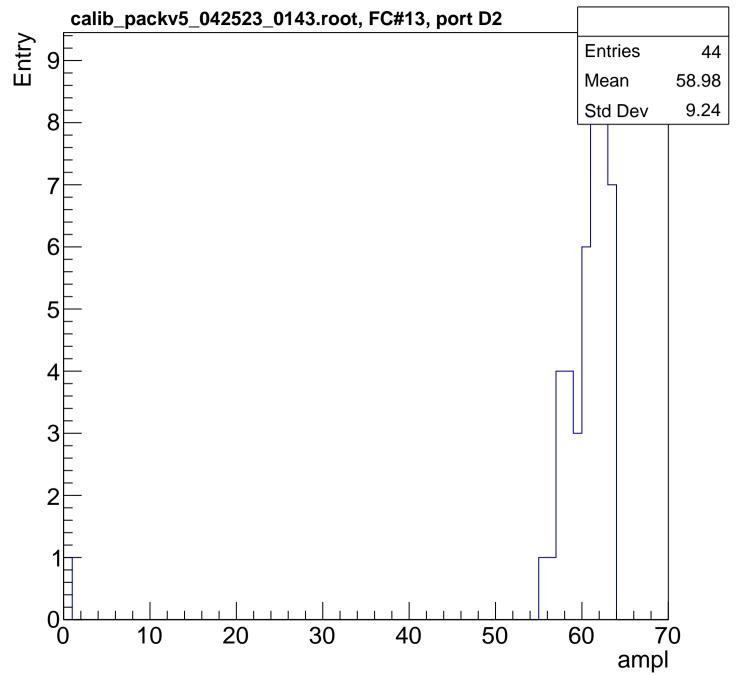


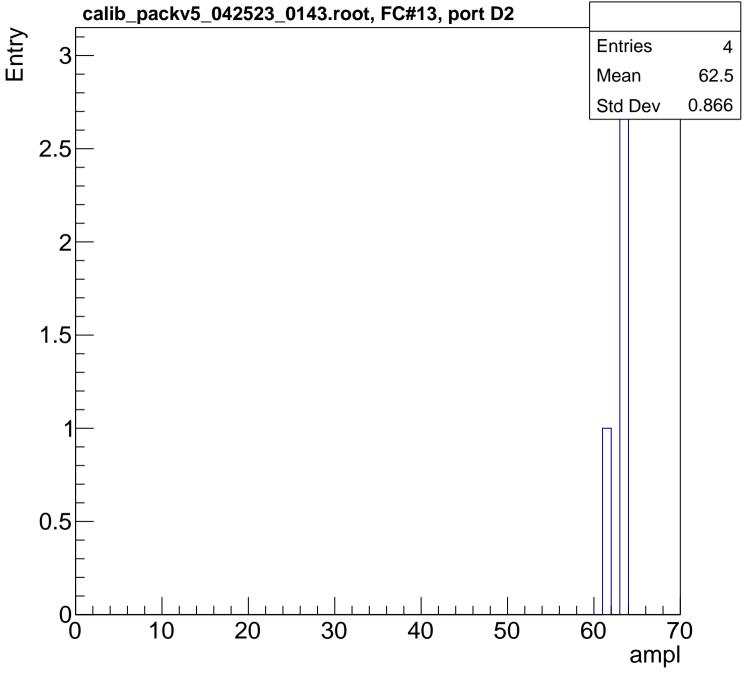




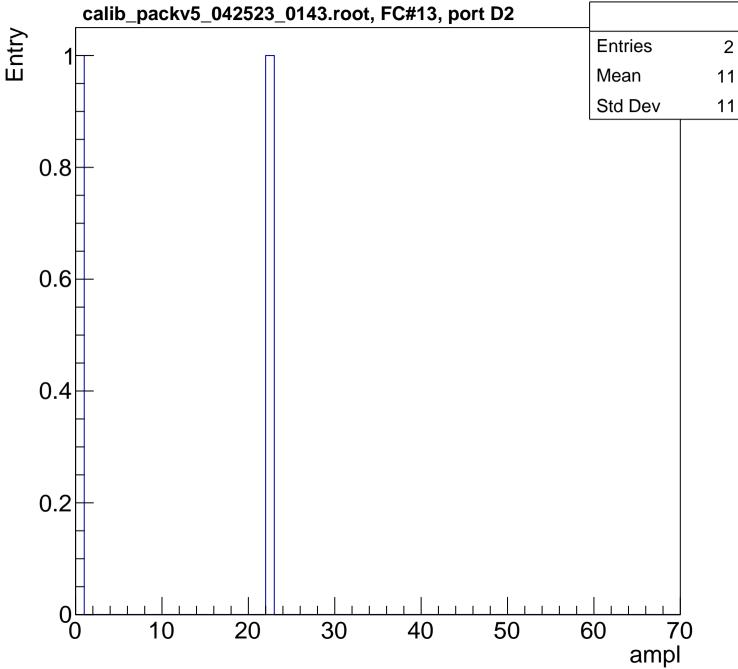


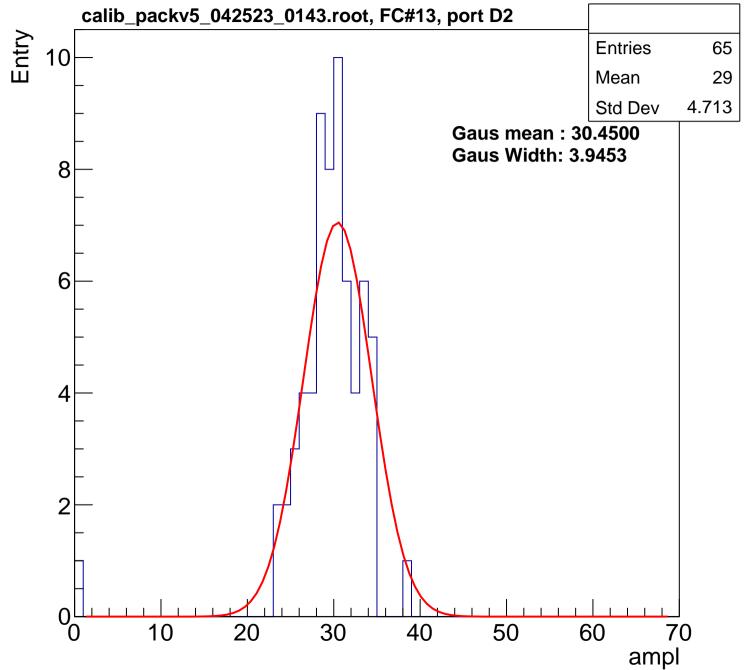


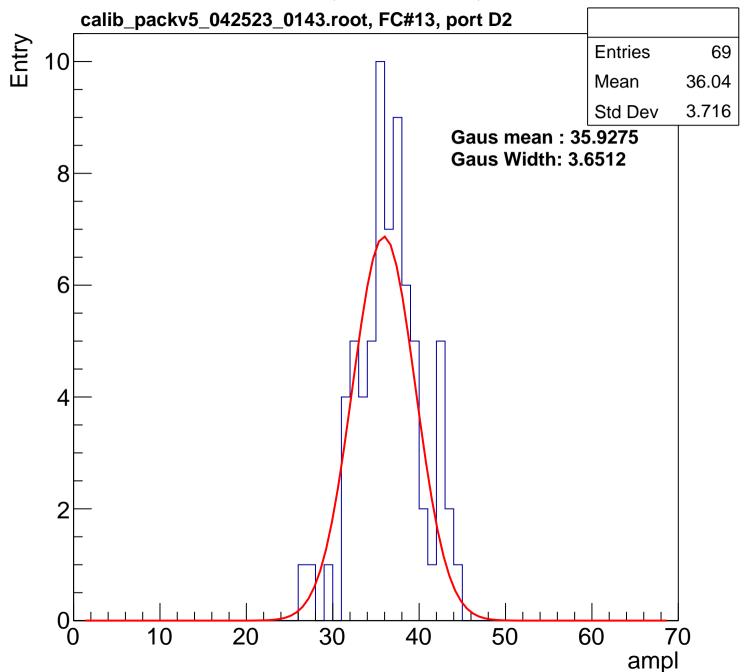


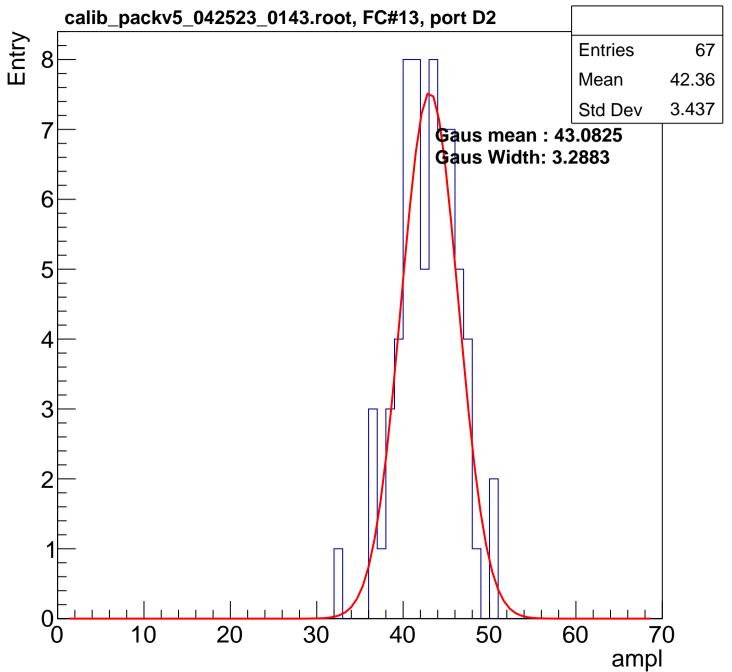


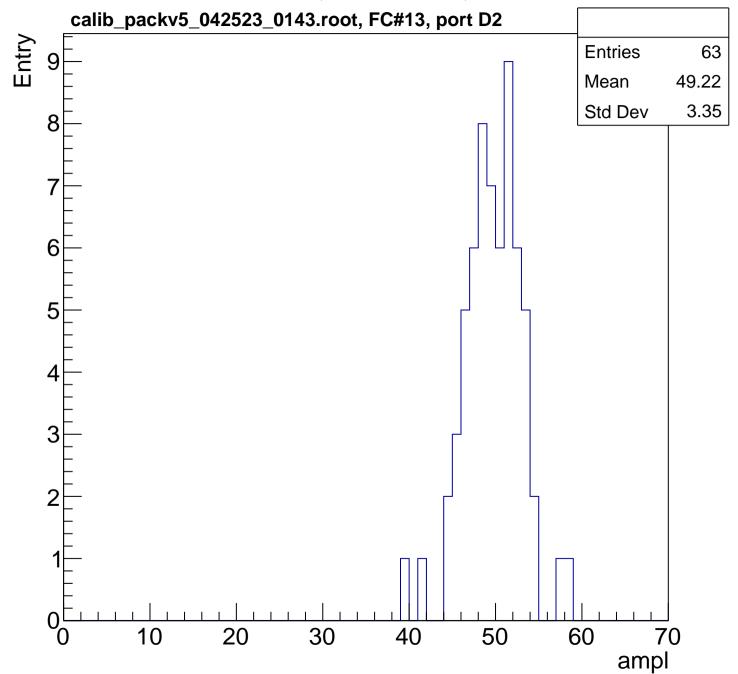
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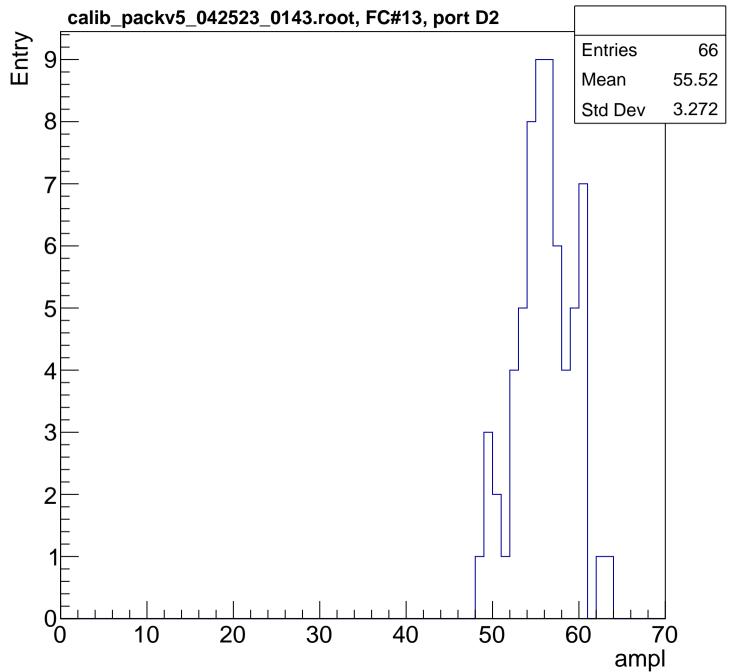


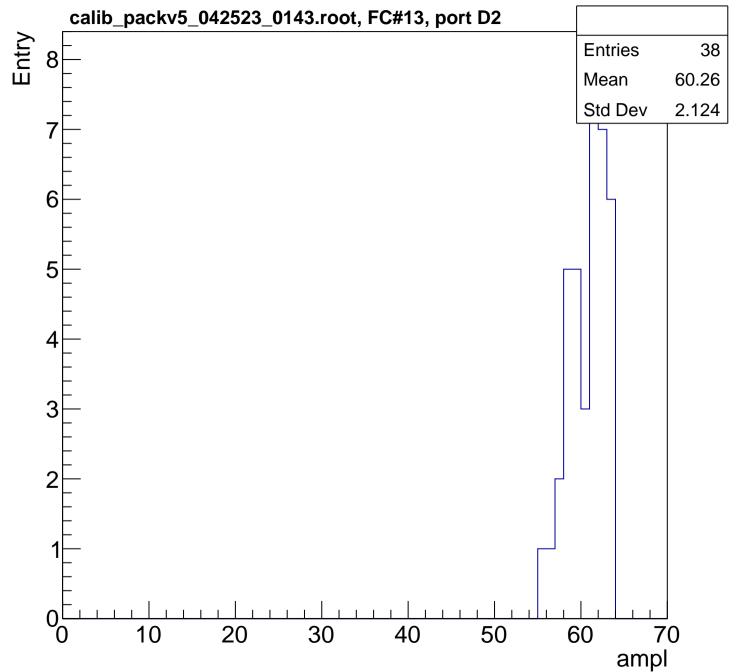


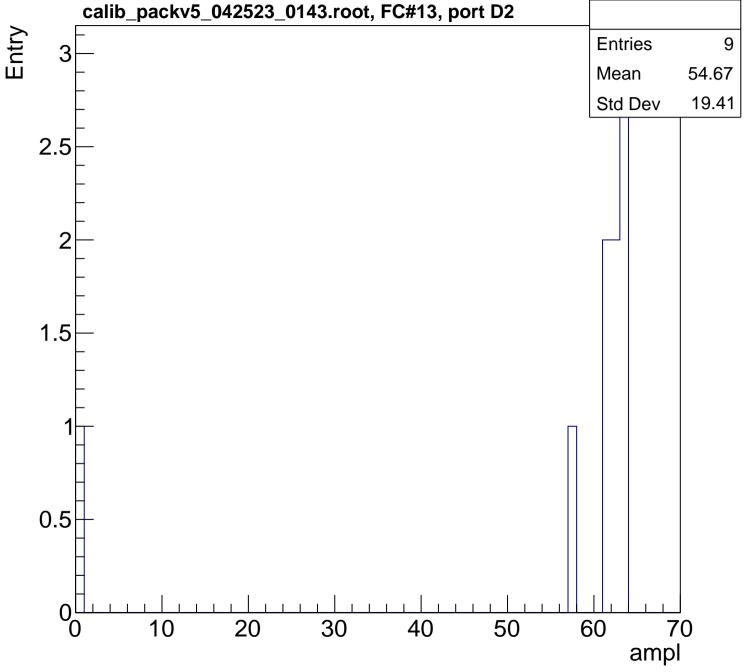


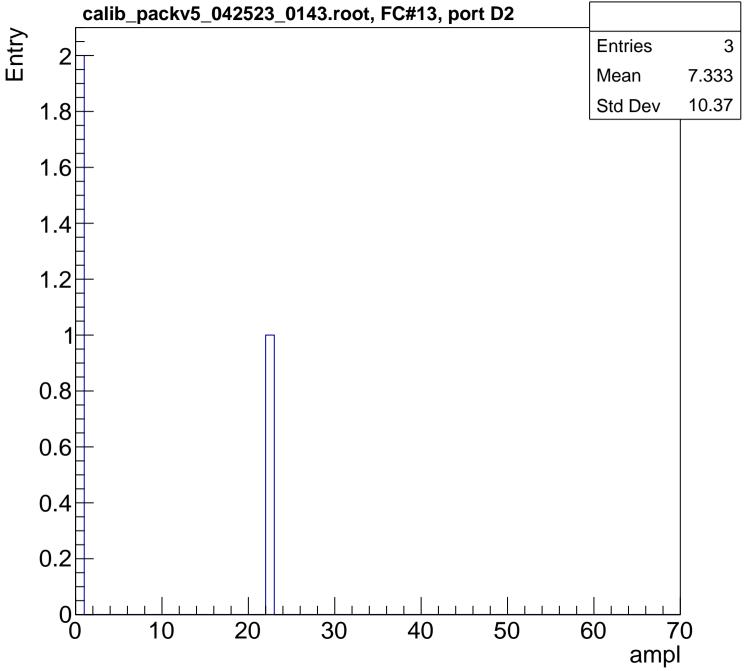


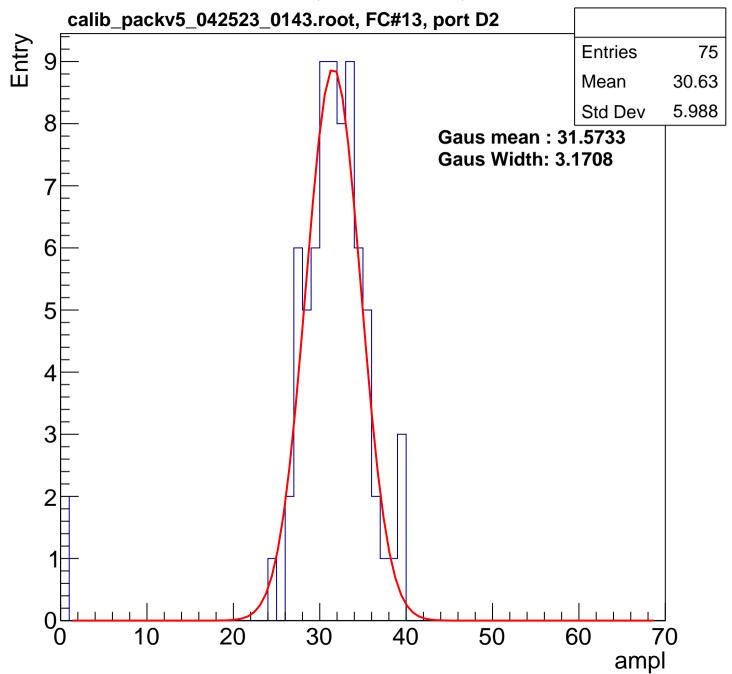


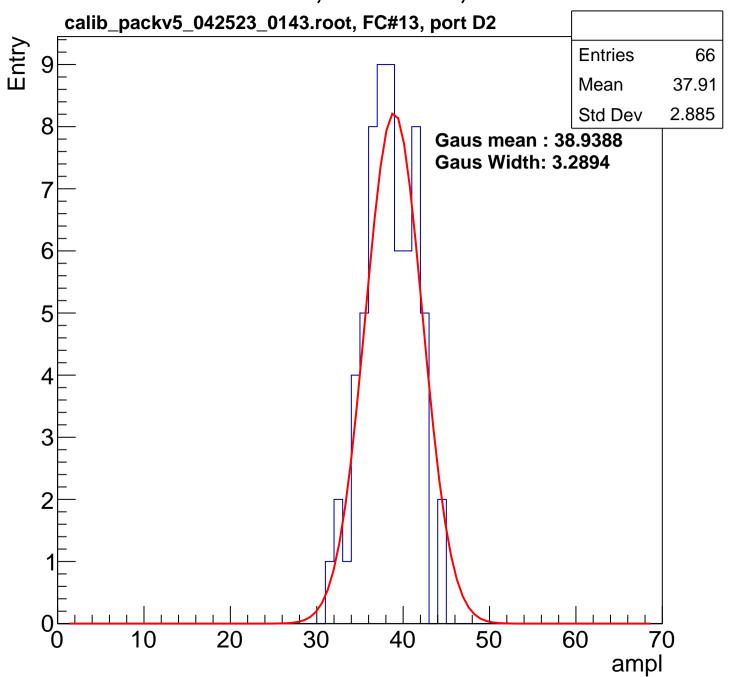


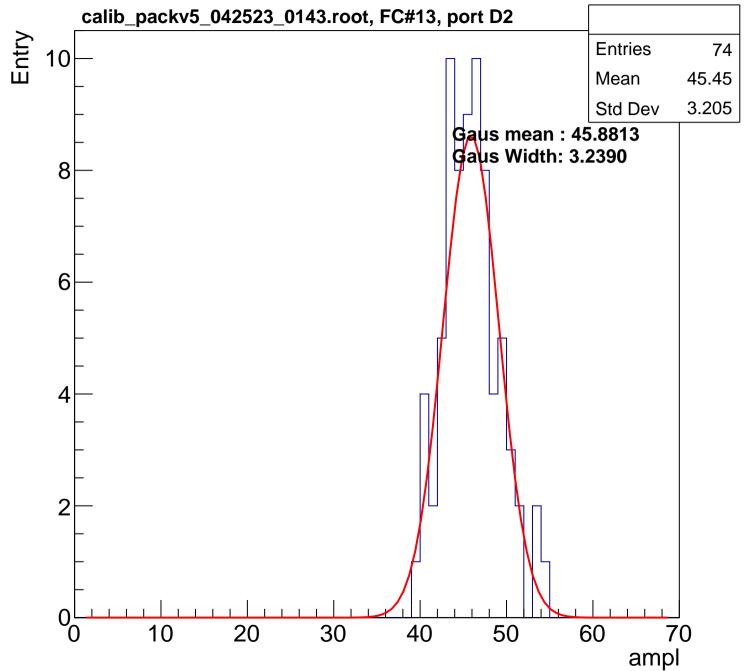


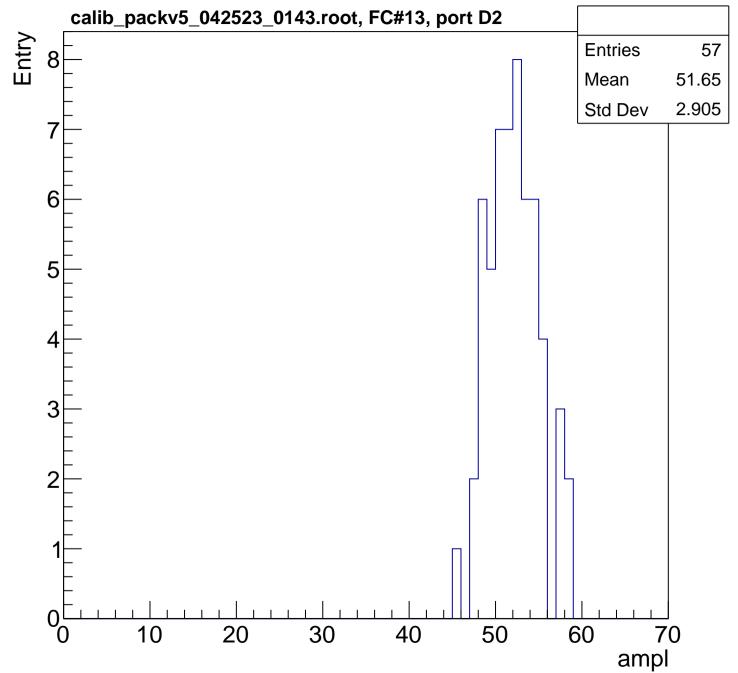


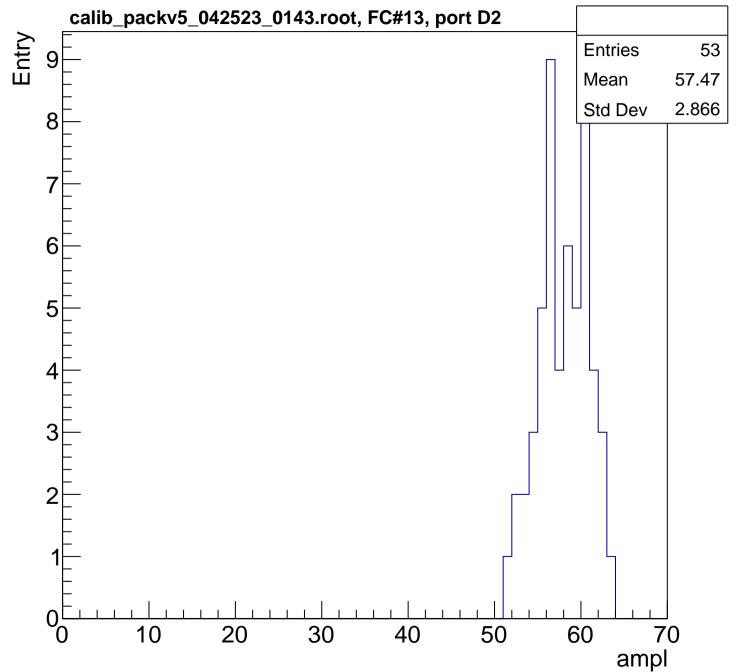


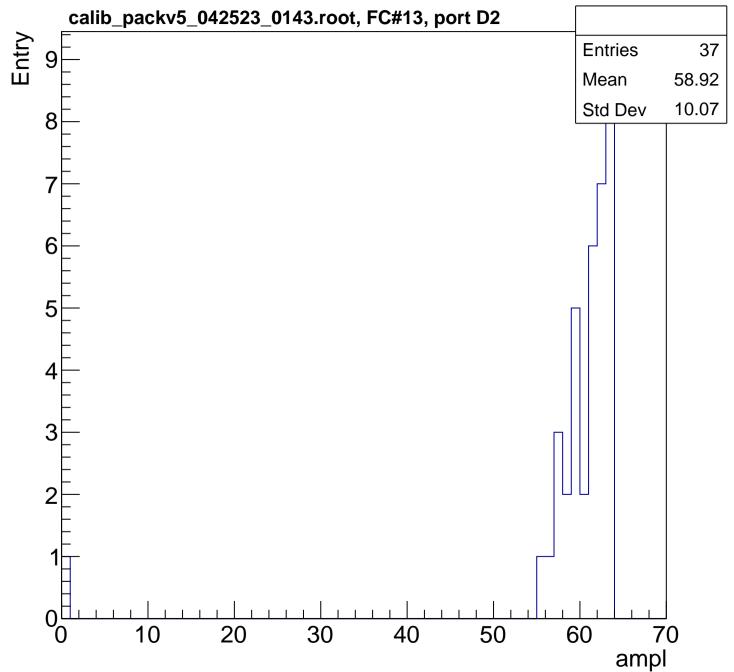


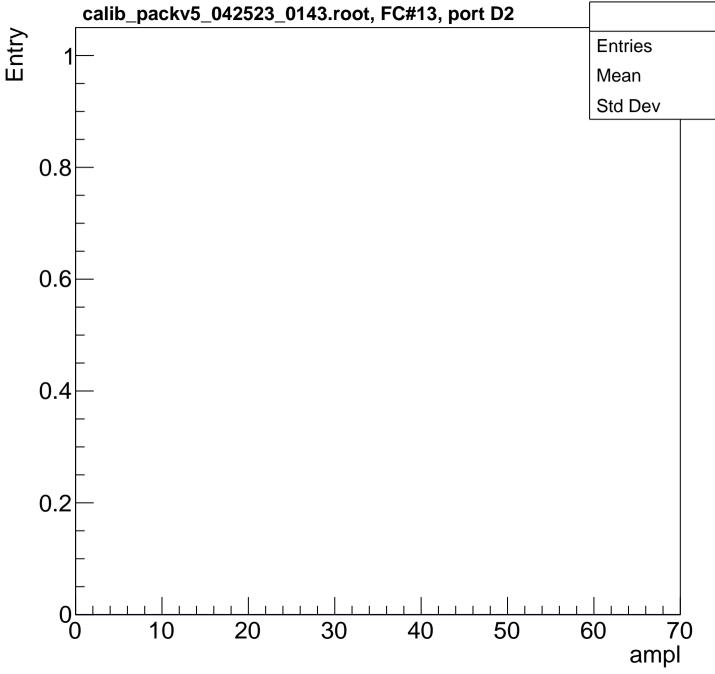


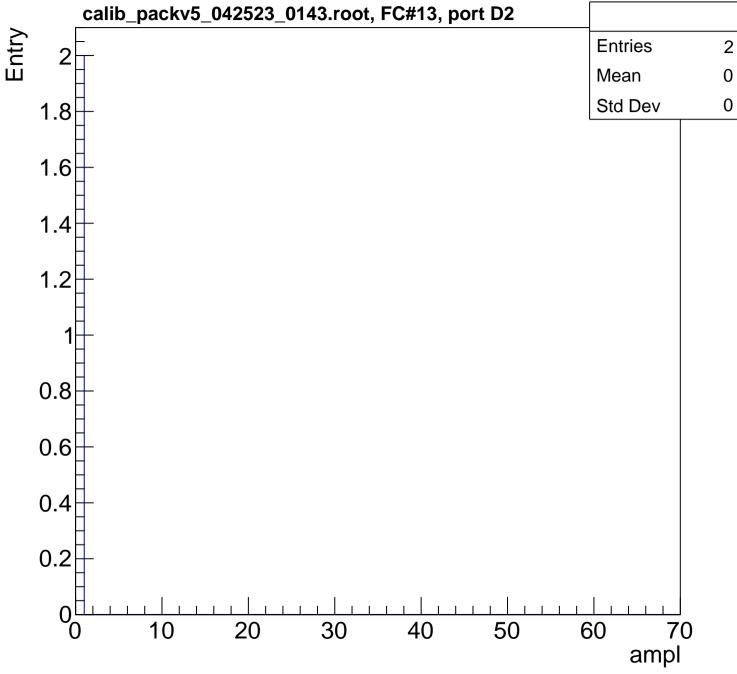


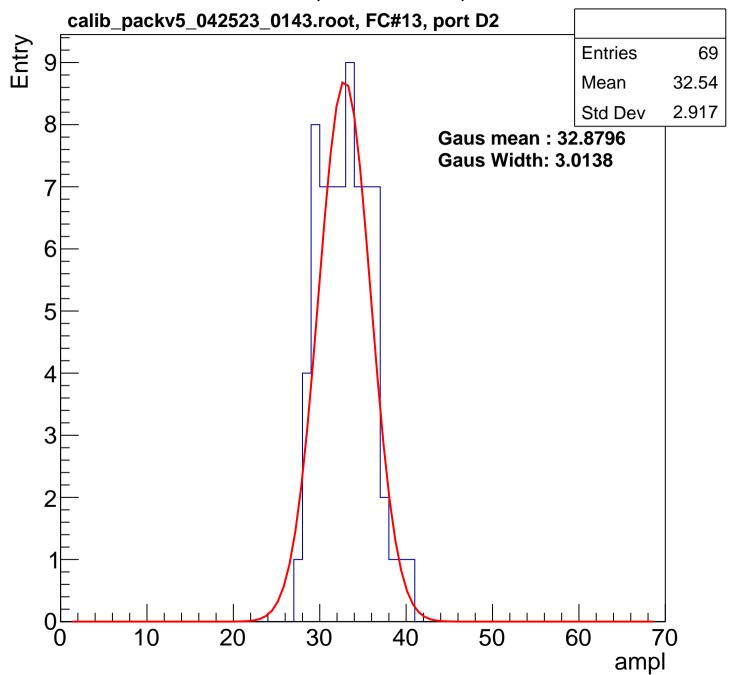


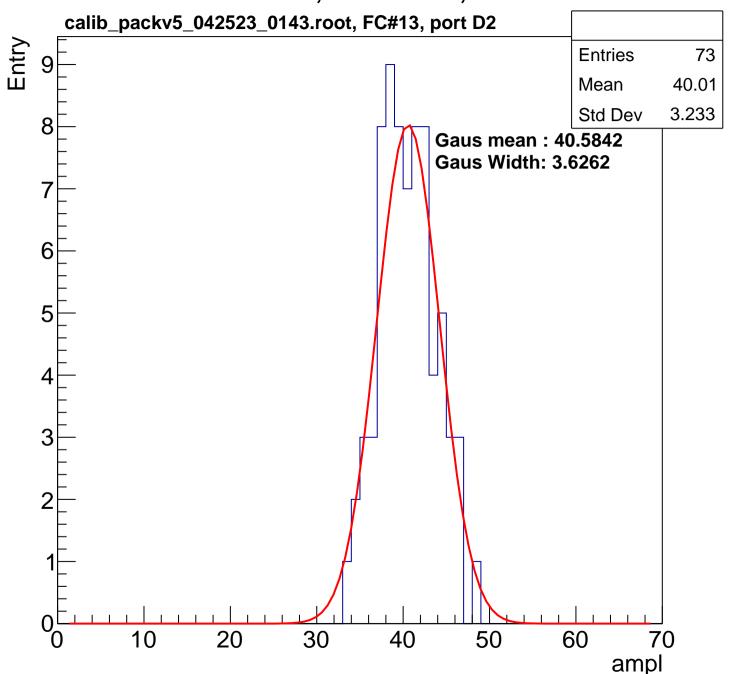


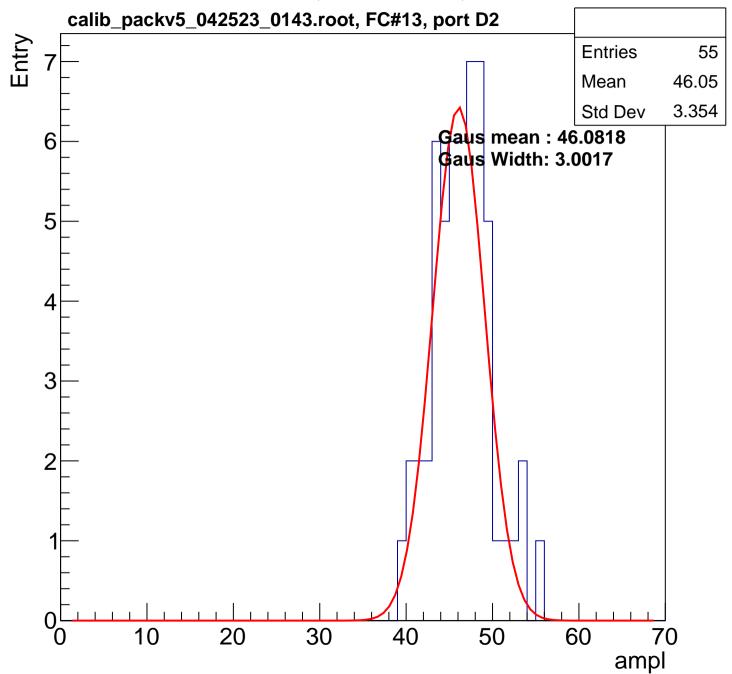


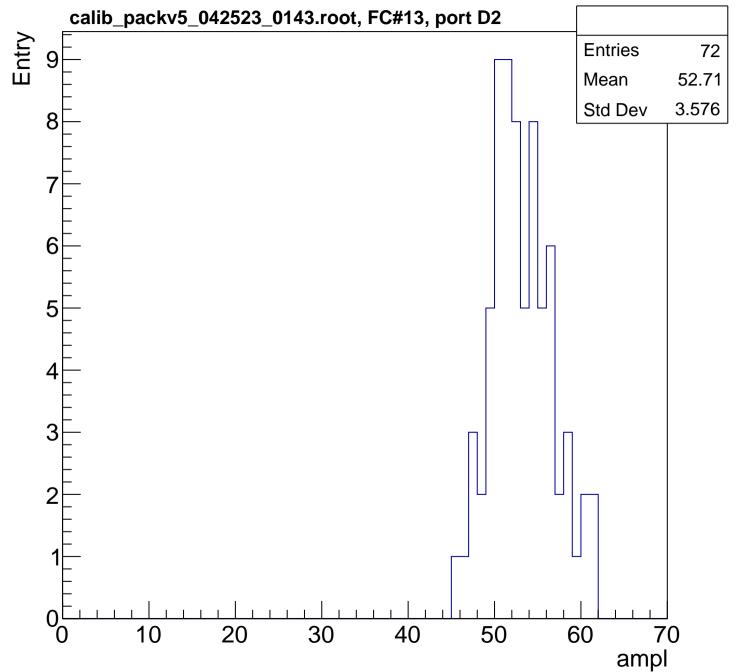


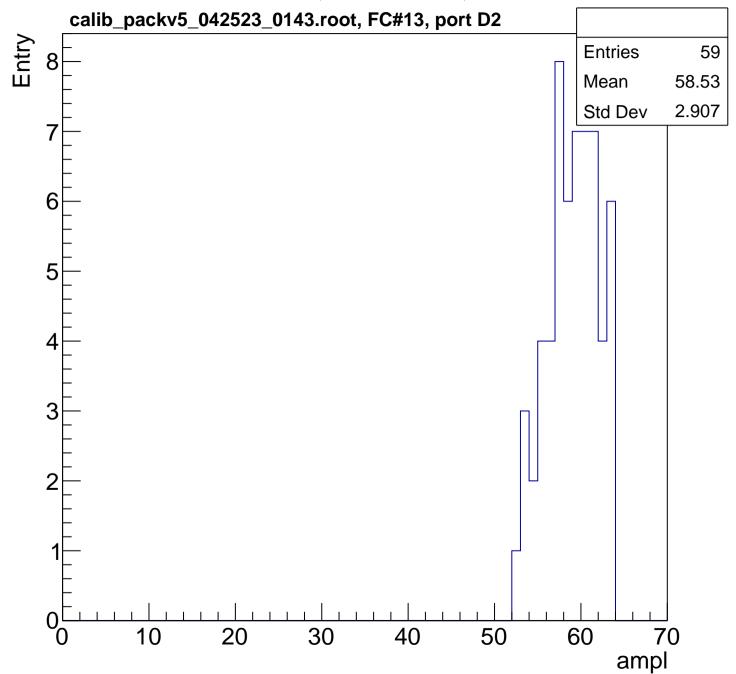


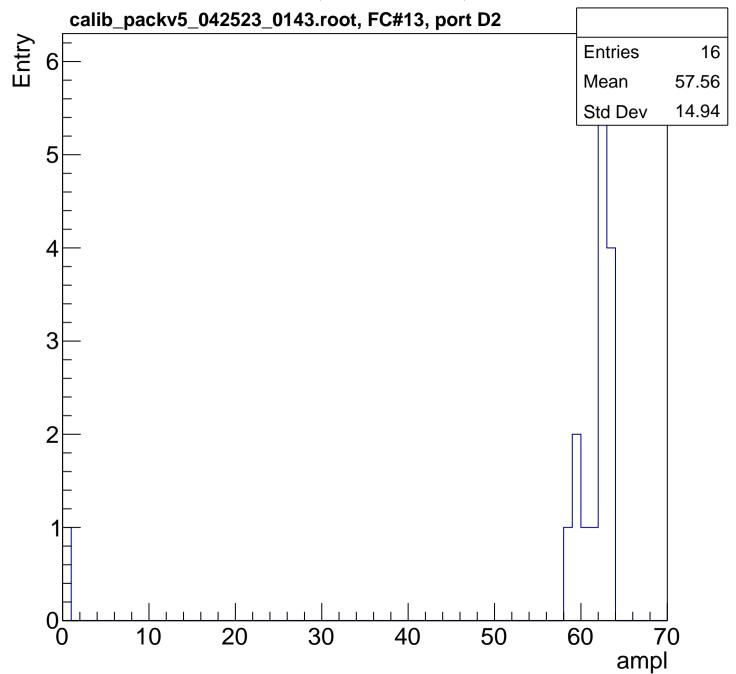


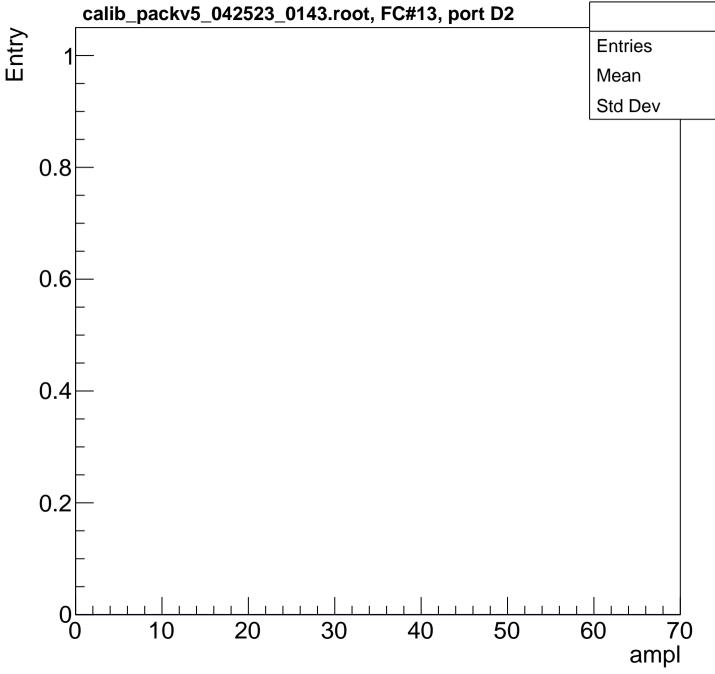




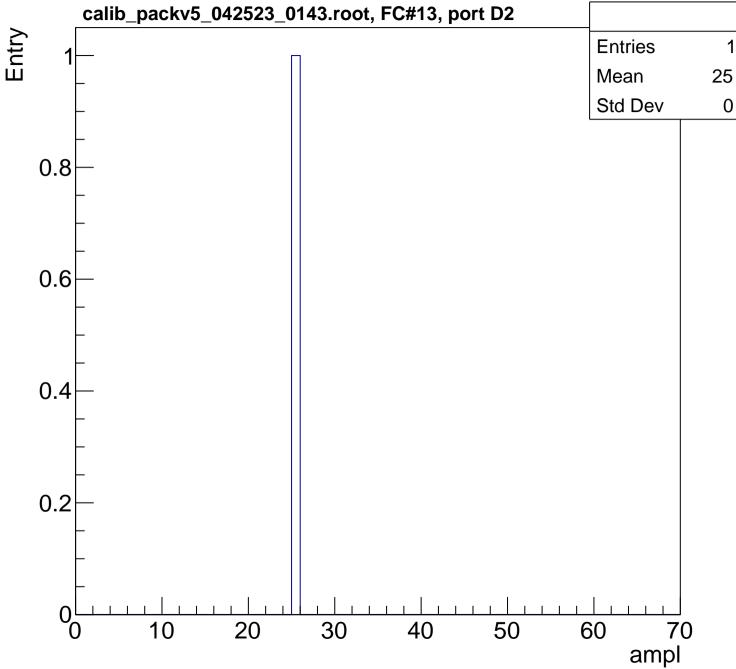


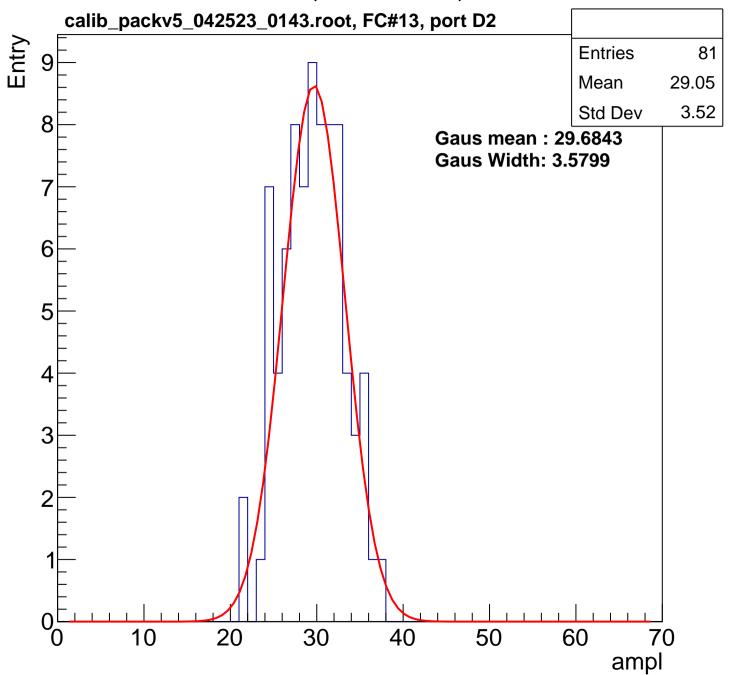


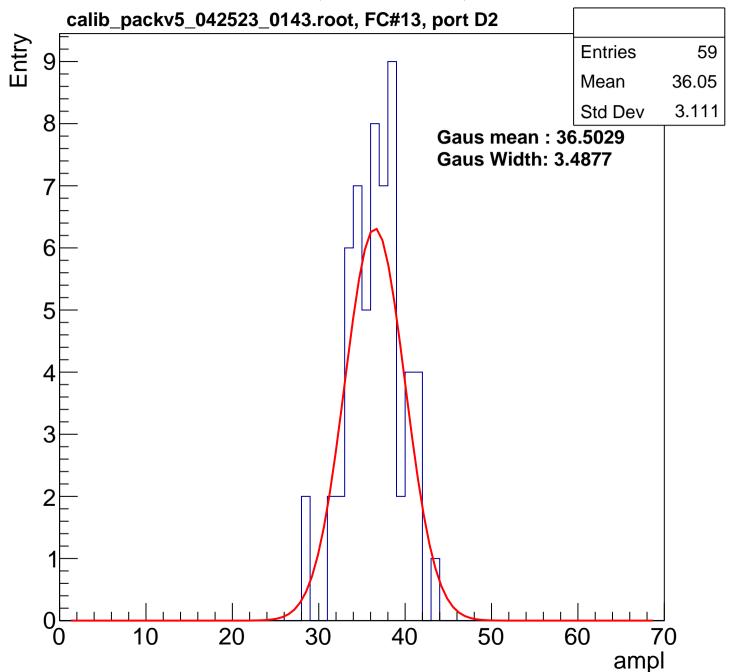


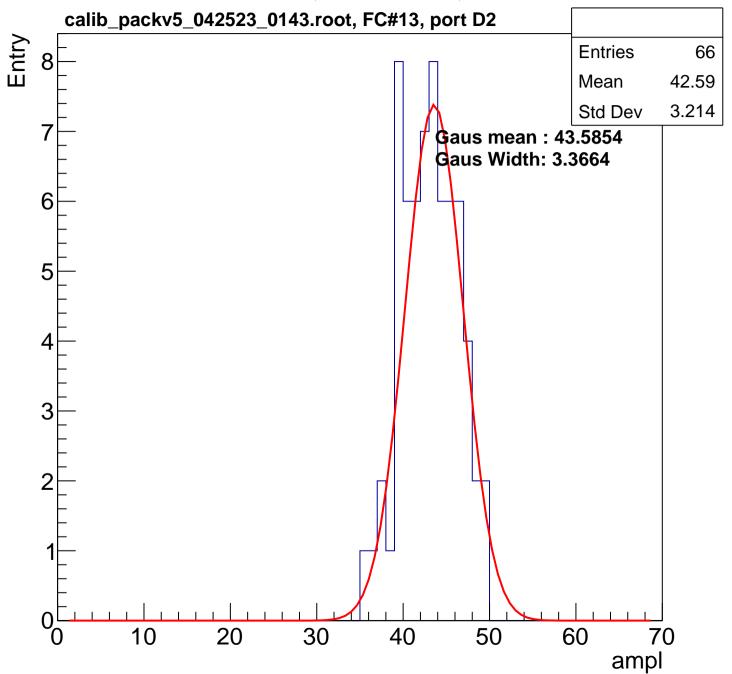


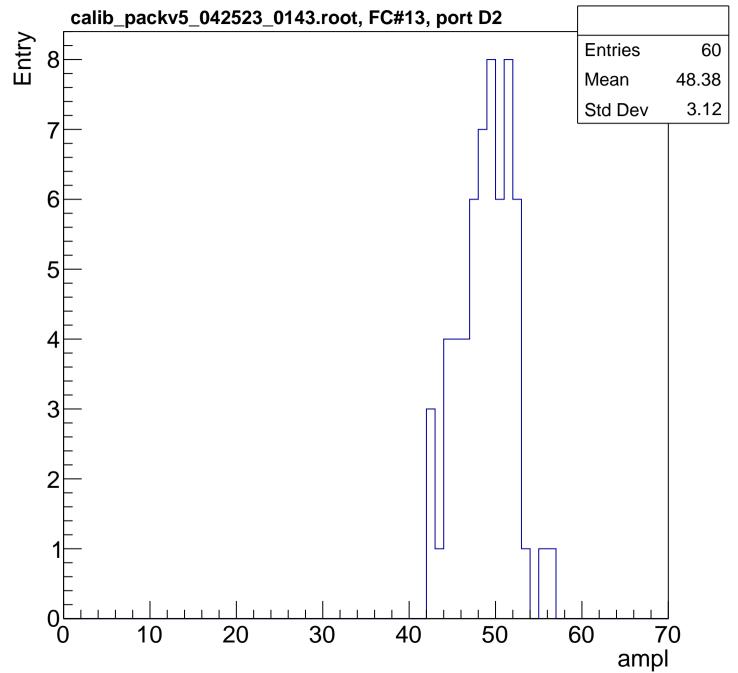
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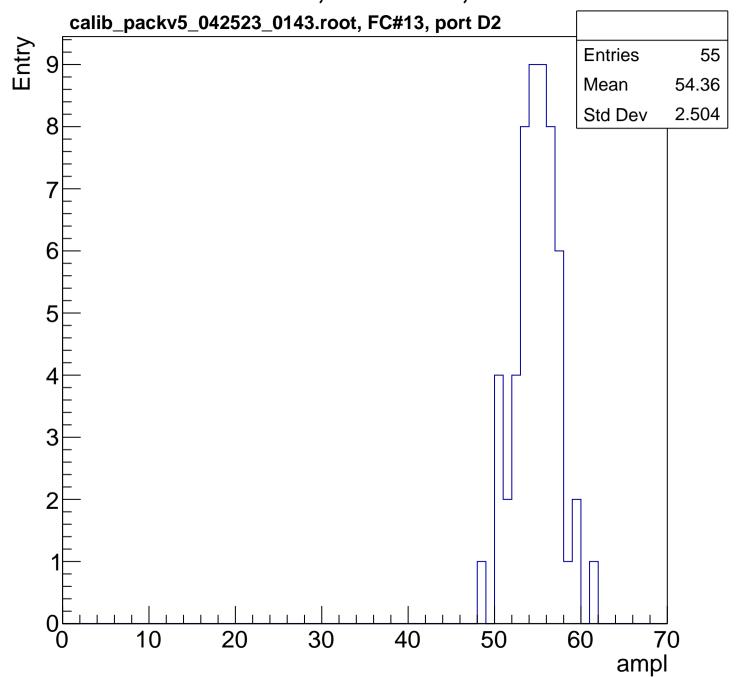


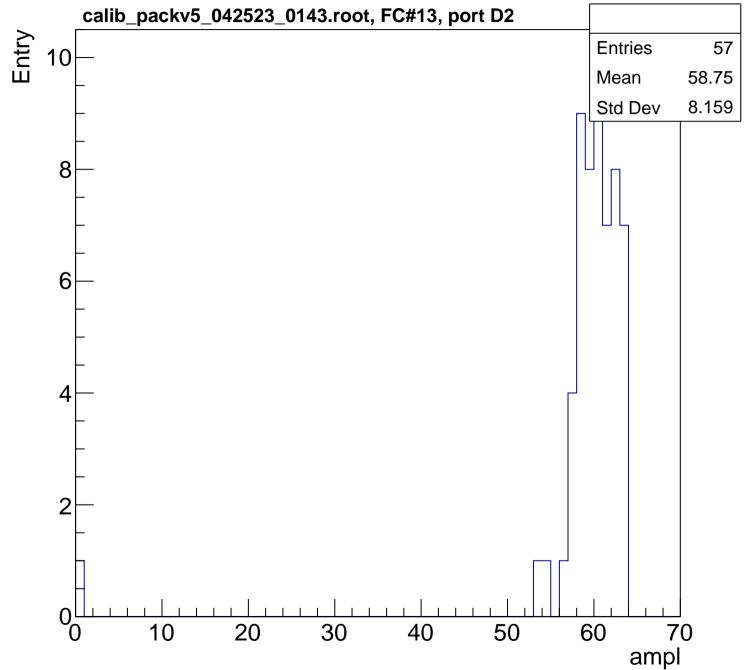


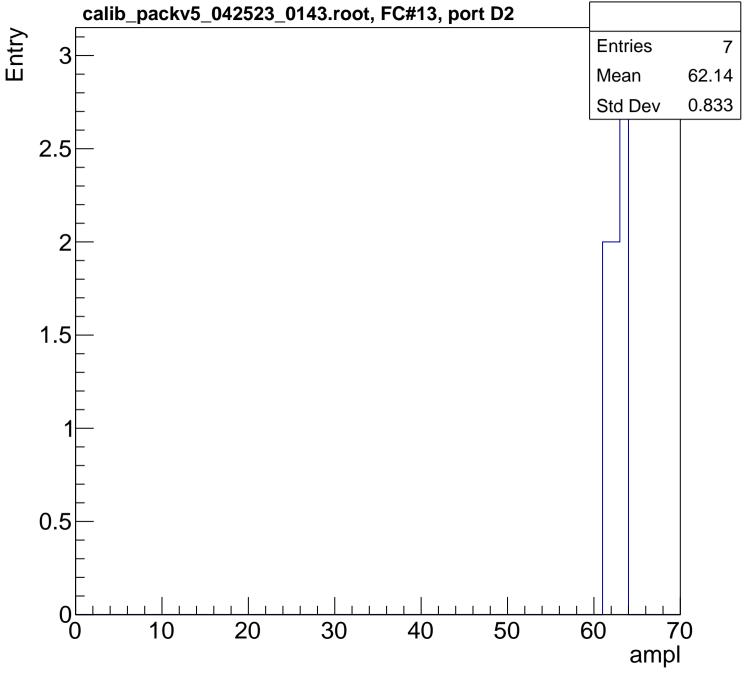




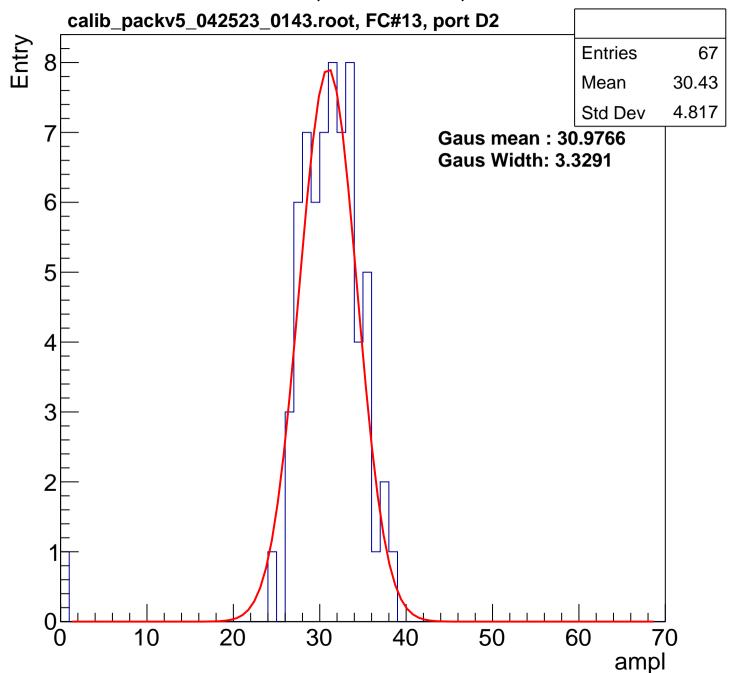


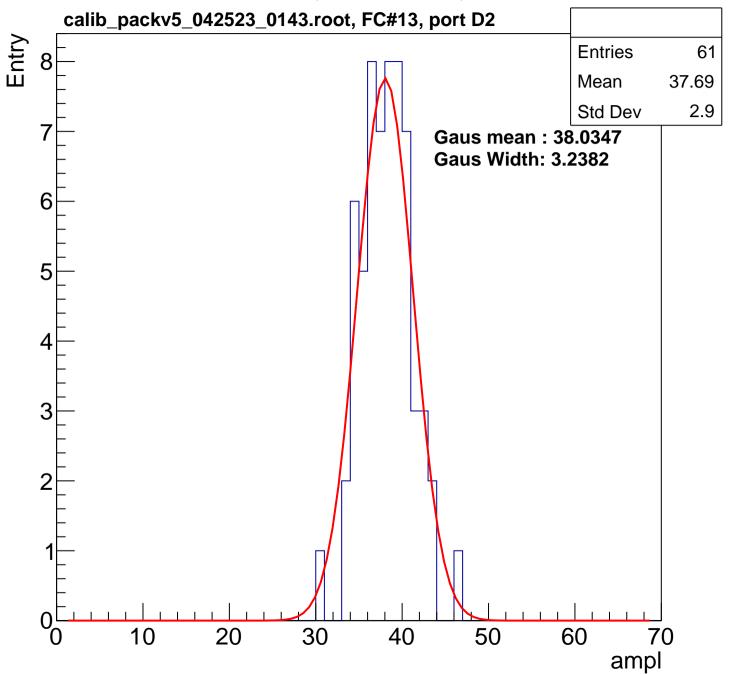


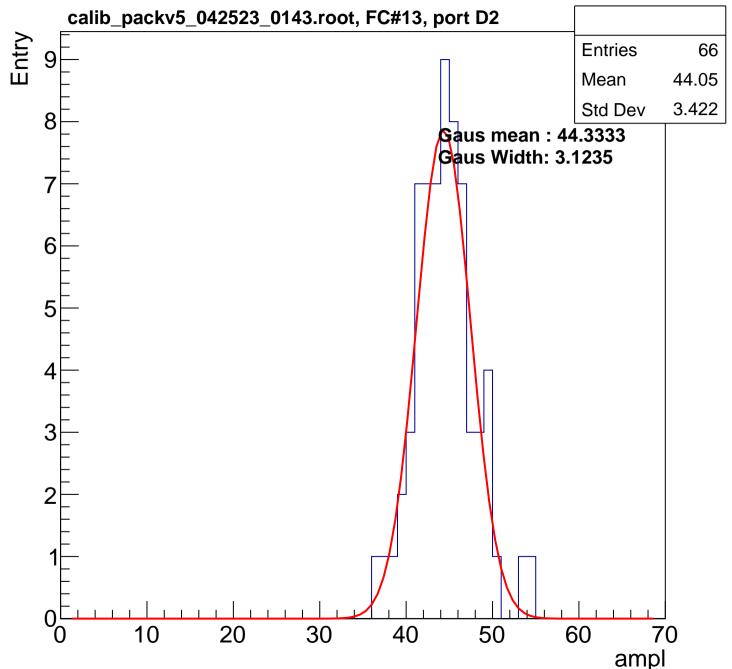


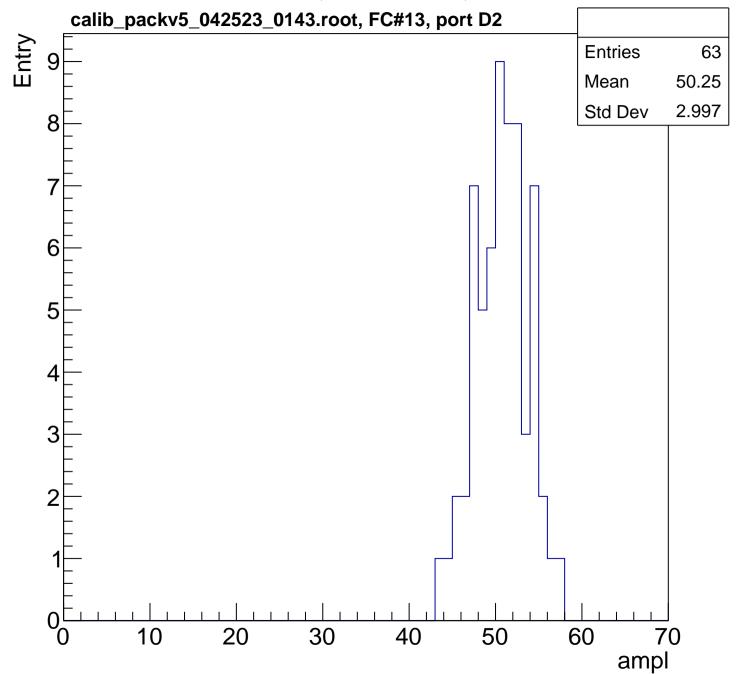


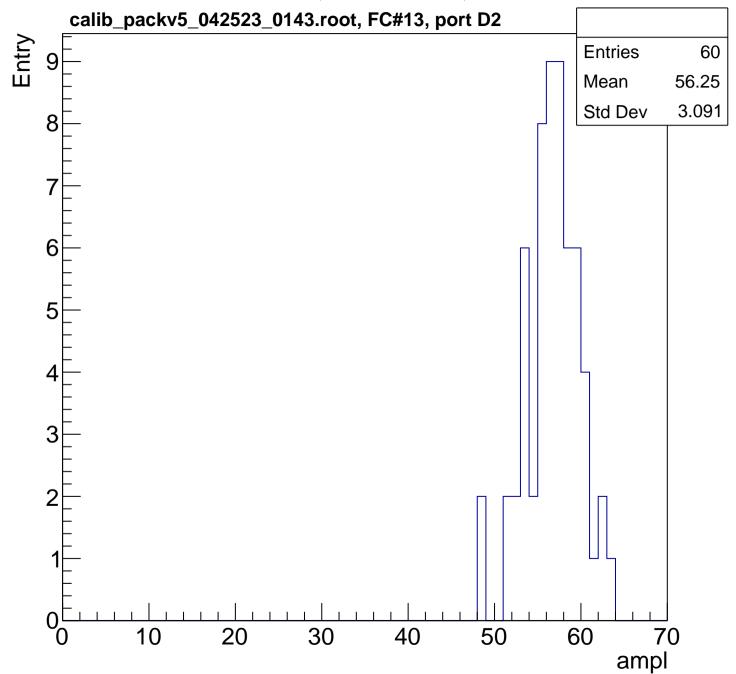
B1L003S, U9-ch37, adc7 calib\_packv5\_042523\_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

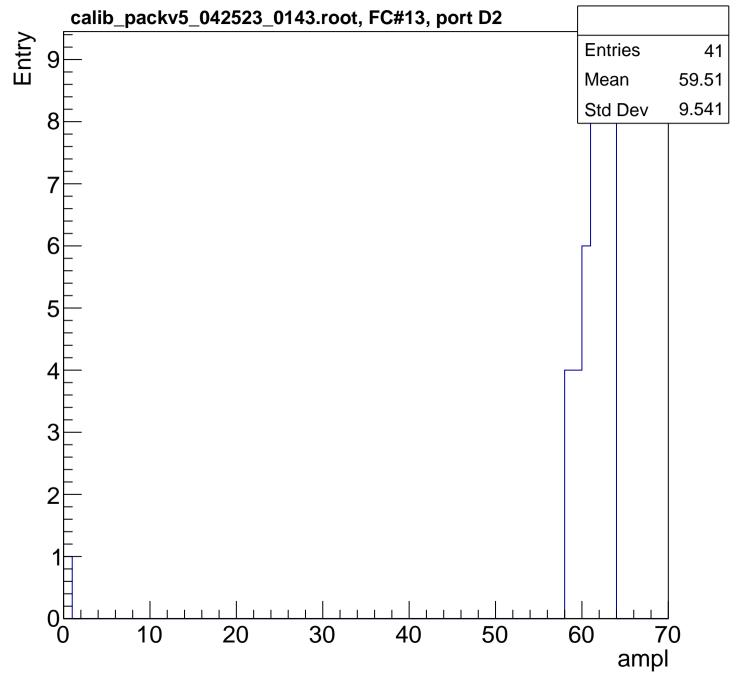


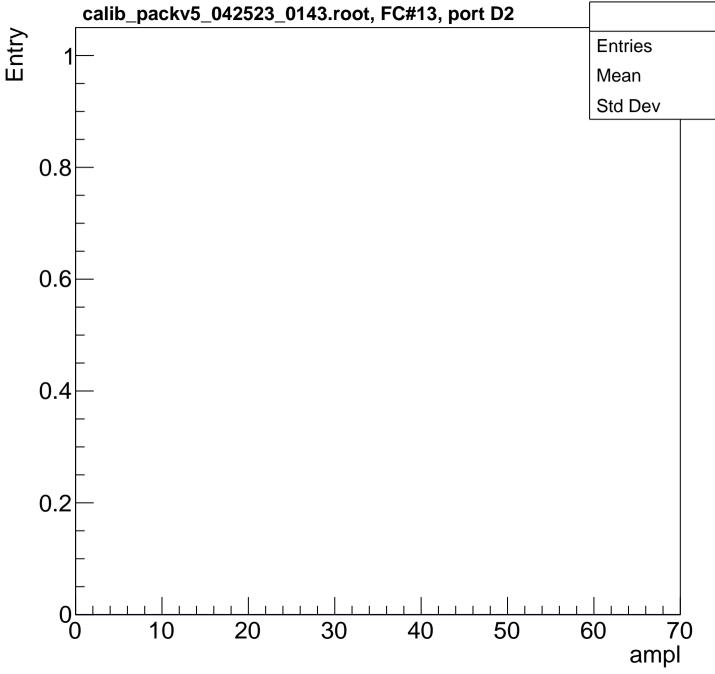




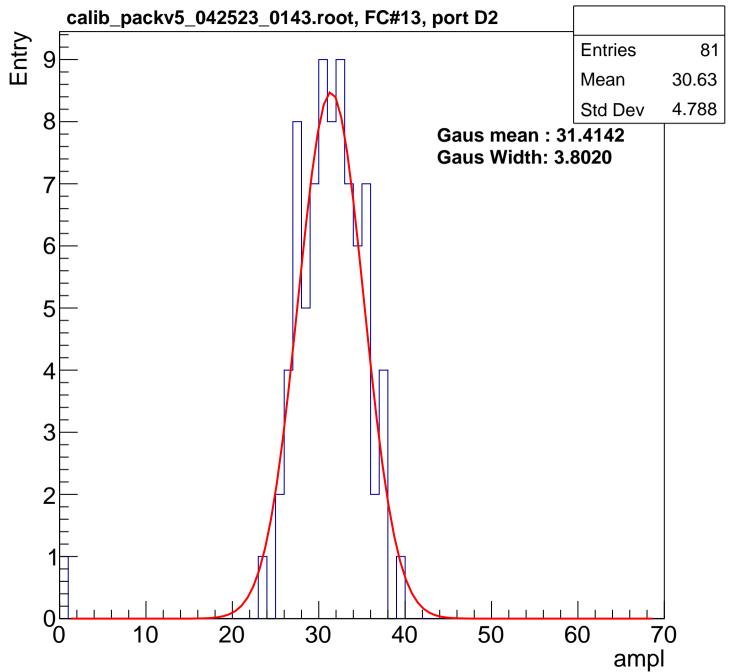


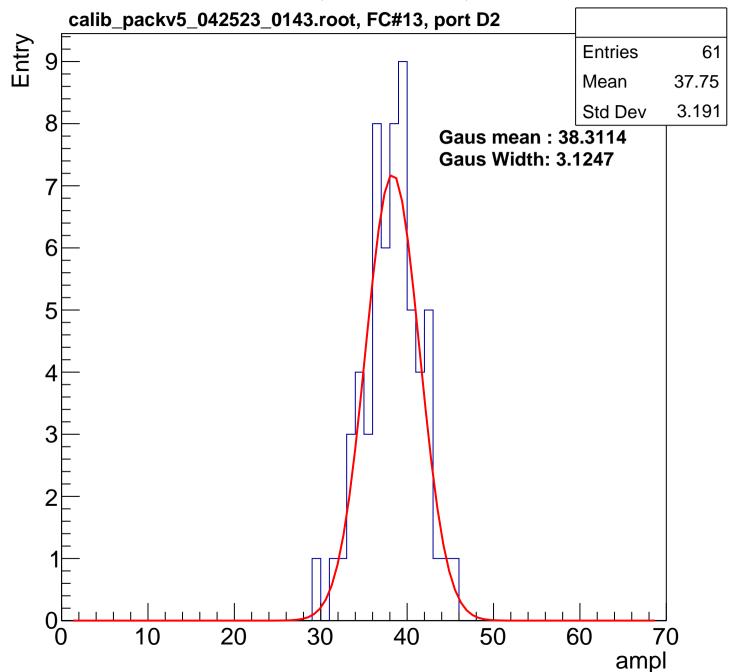


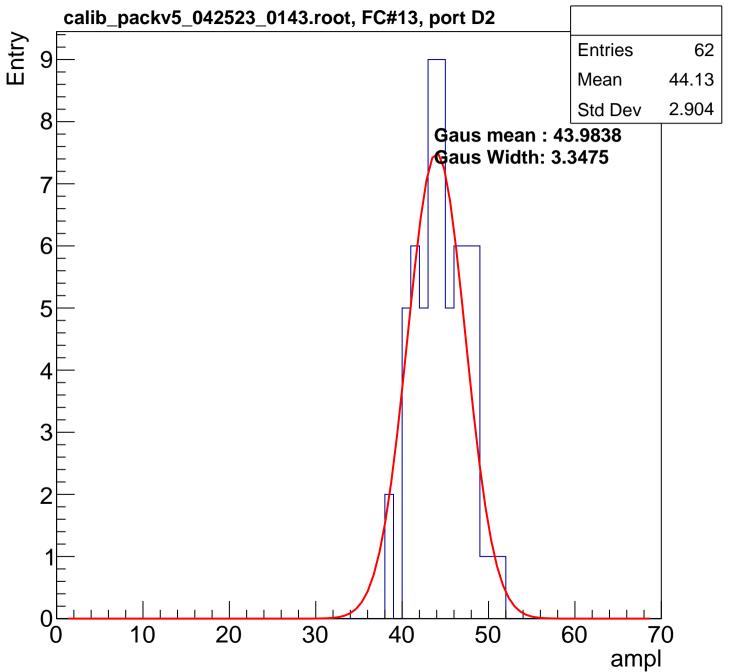


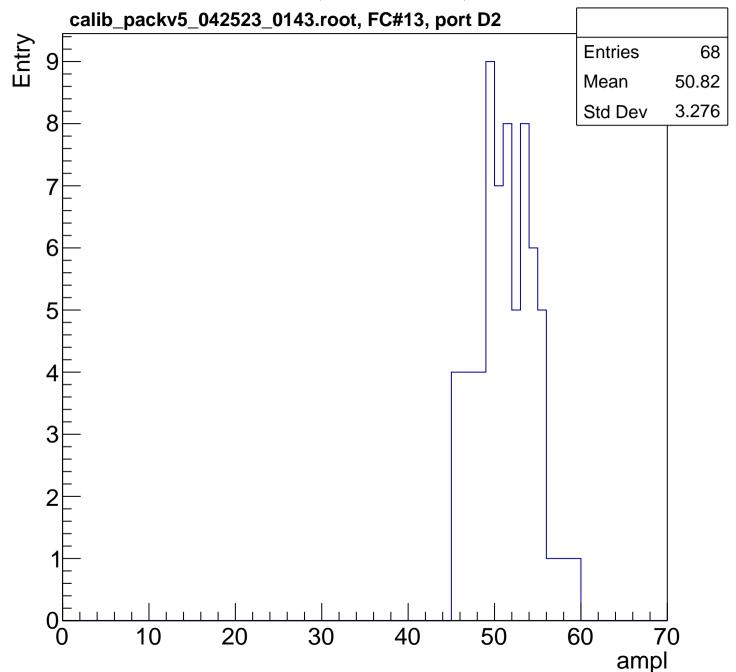


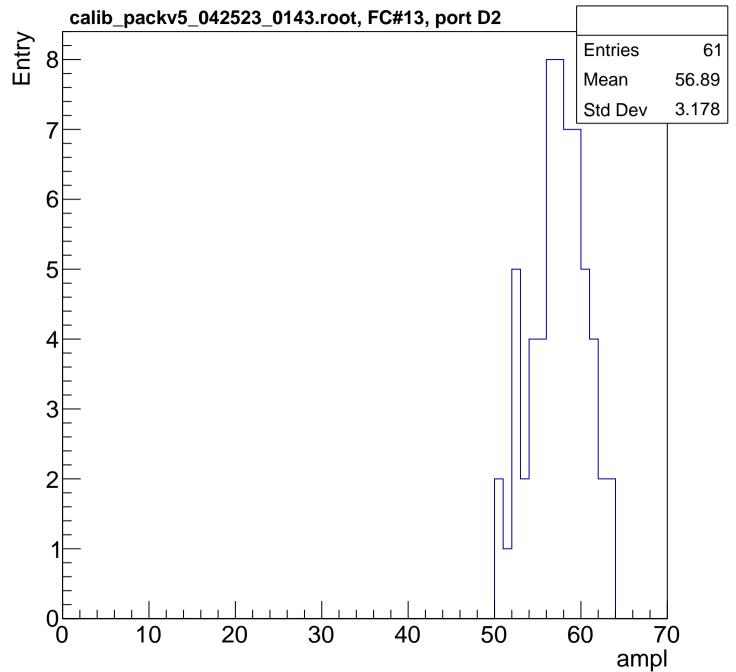
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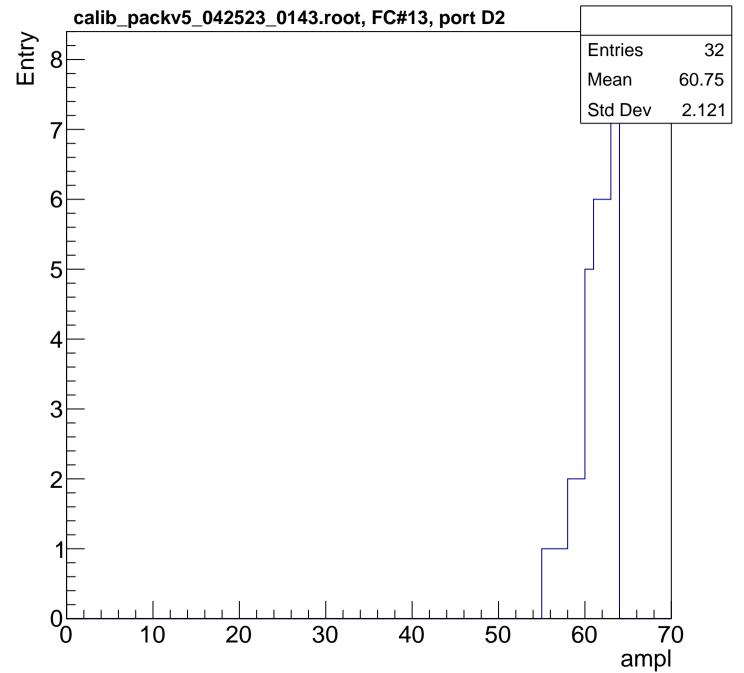


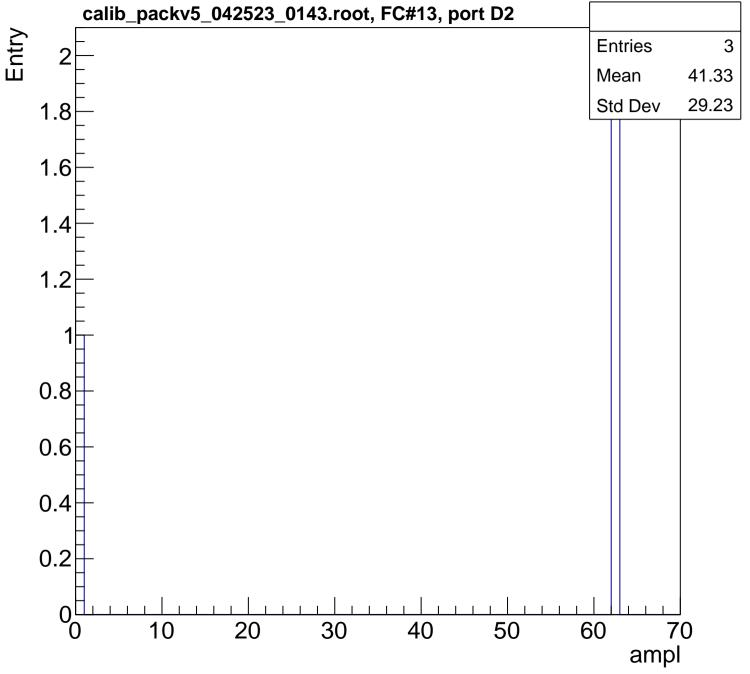


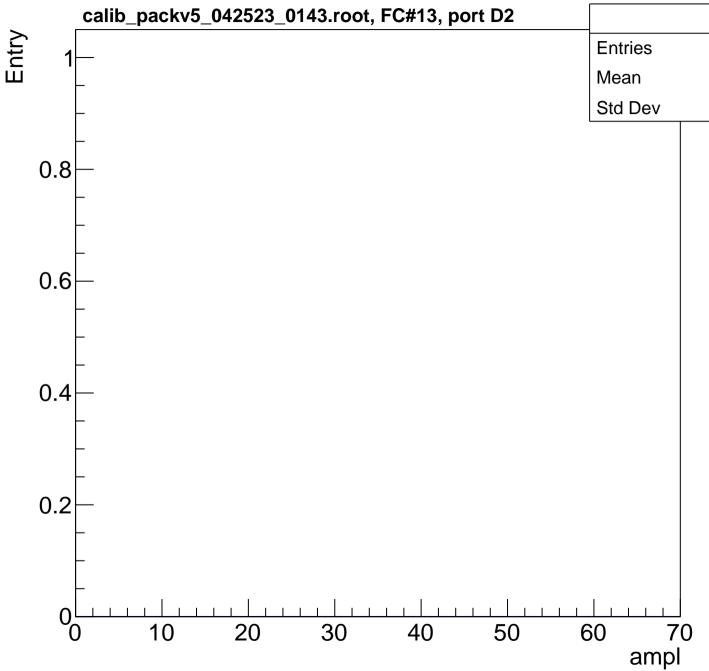


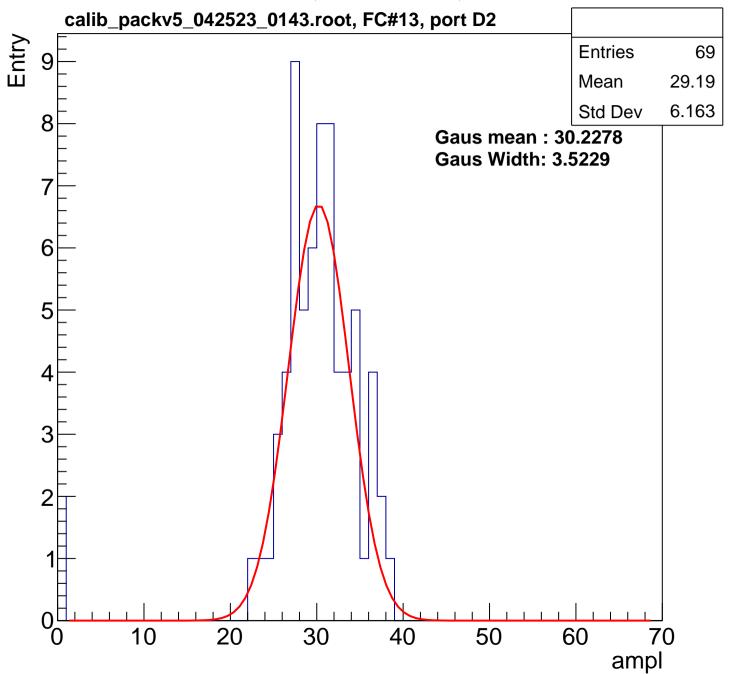


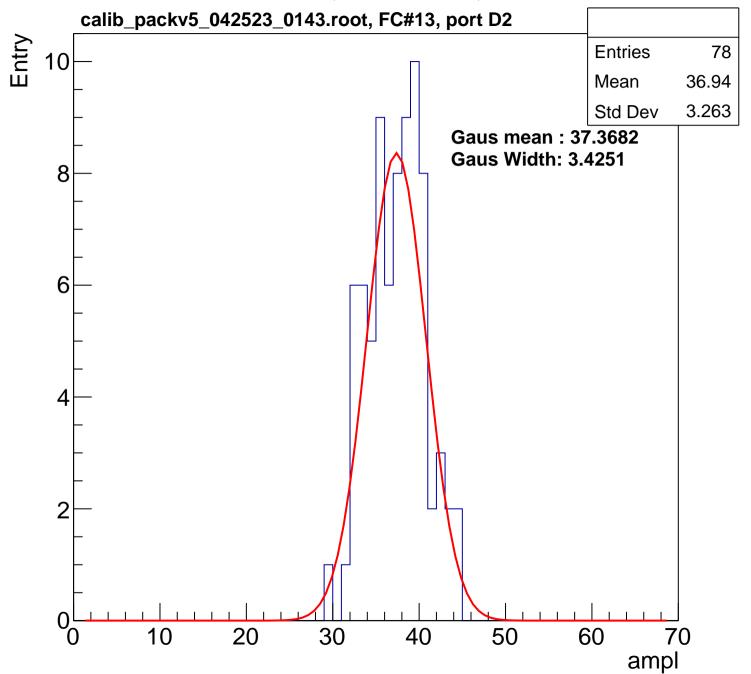


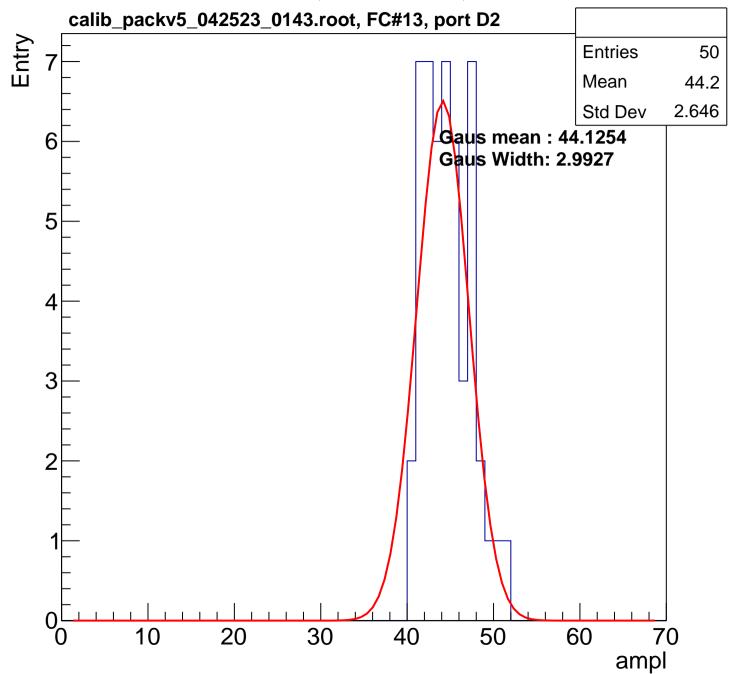


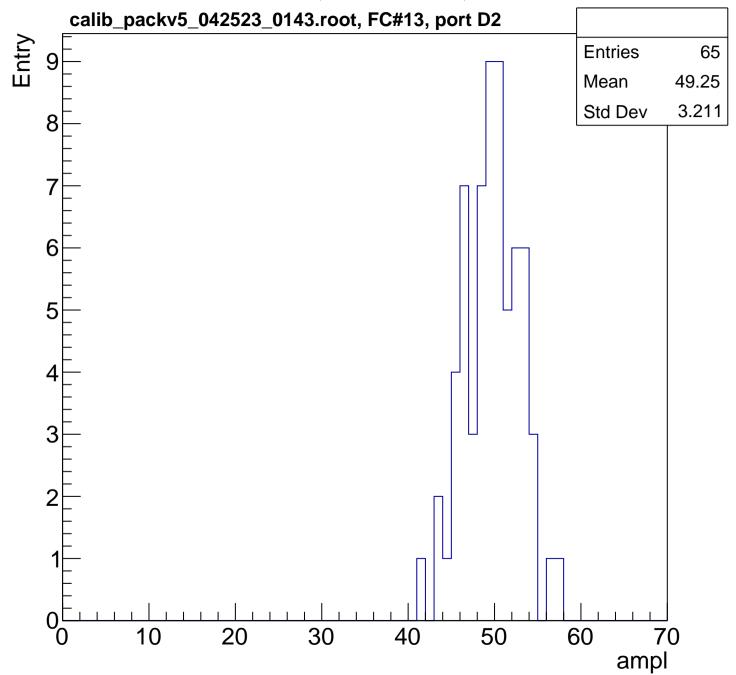


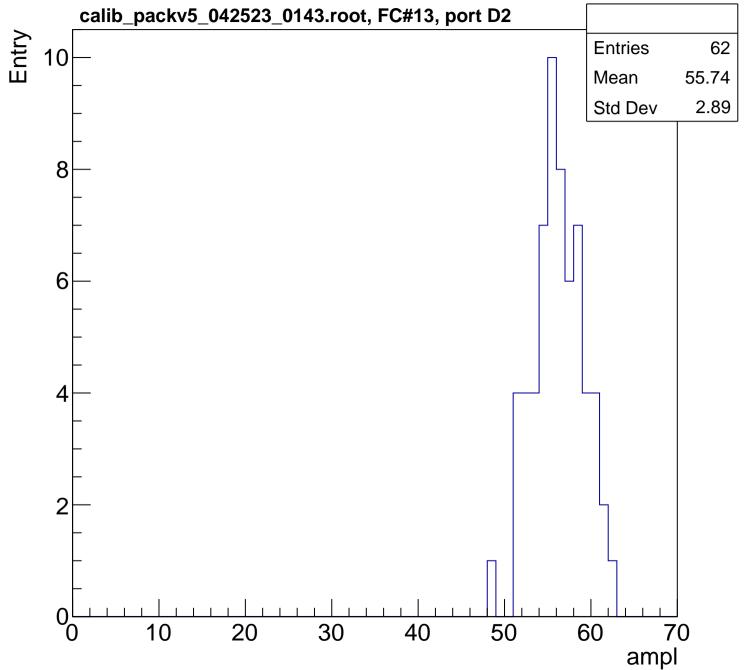


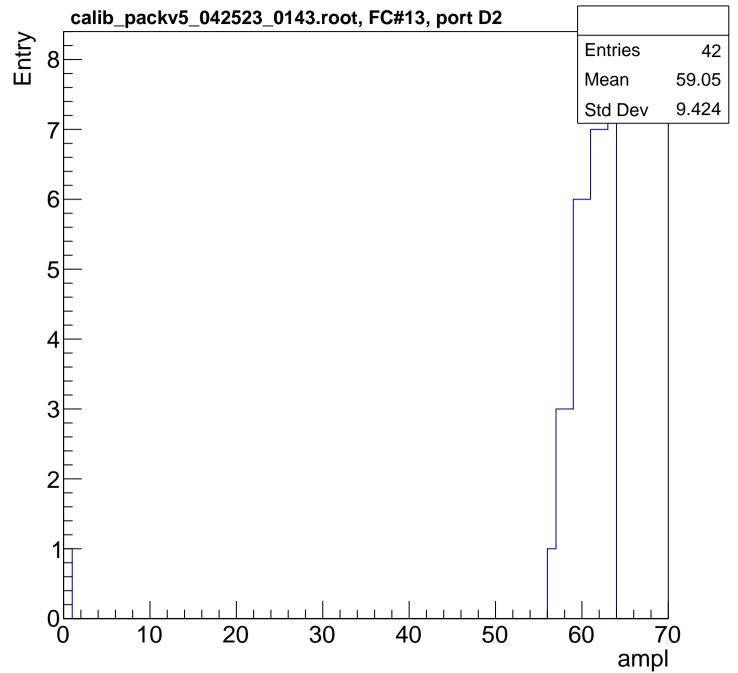


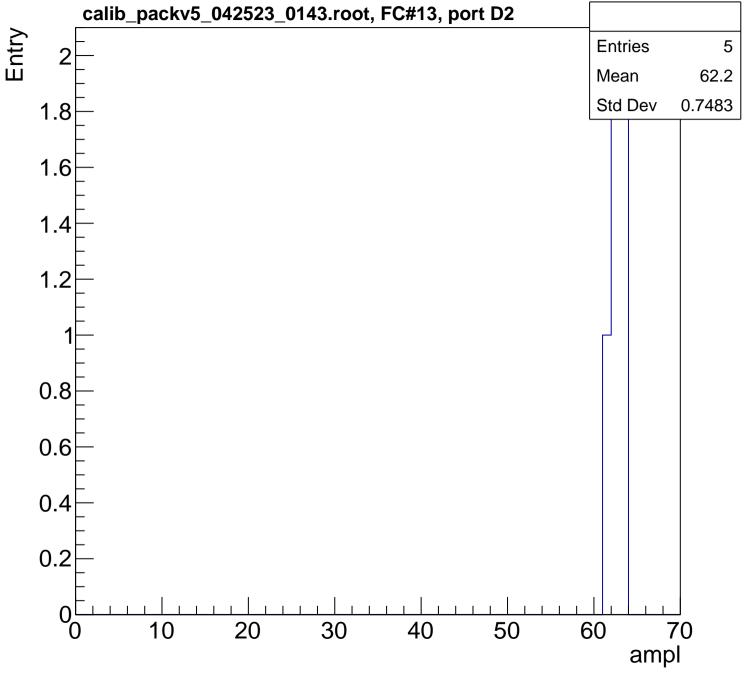


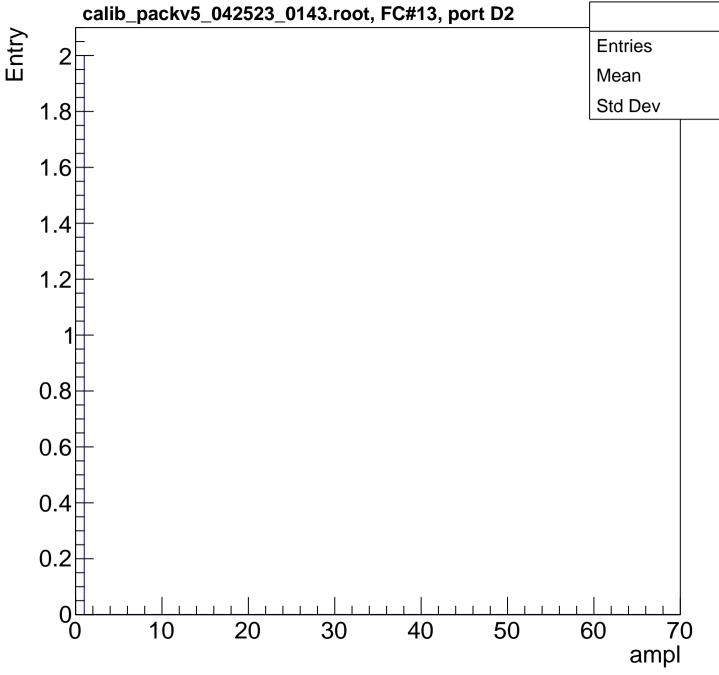


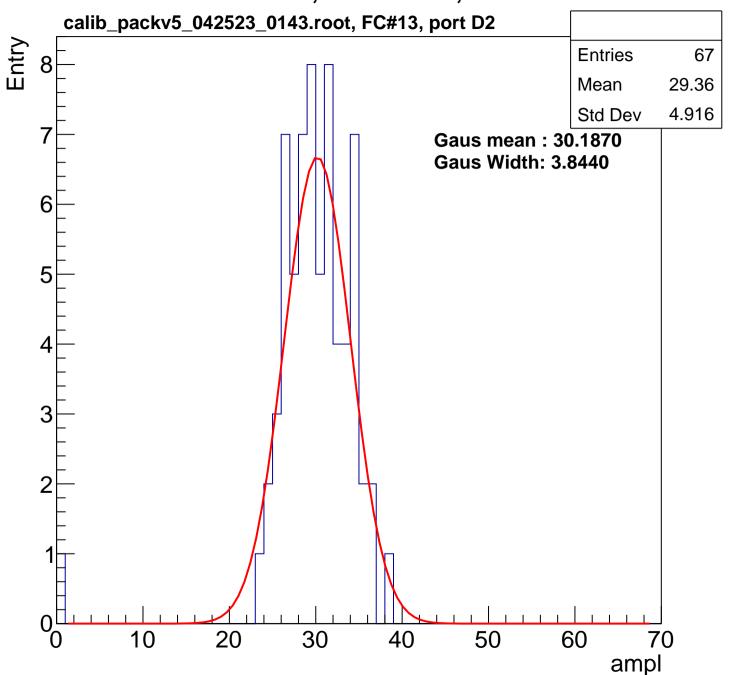


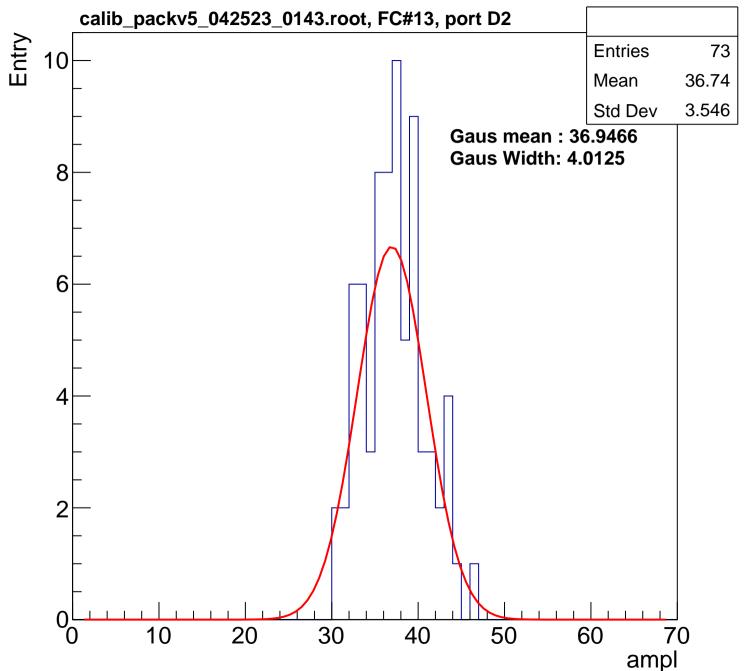


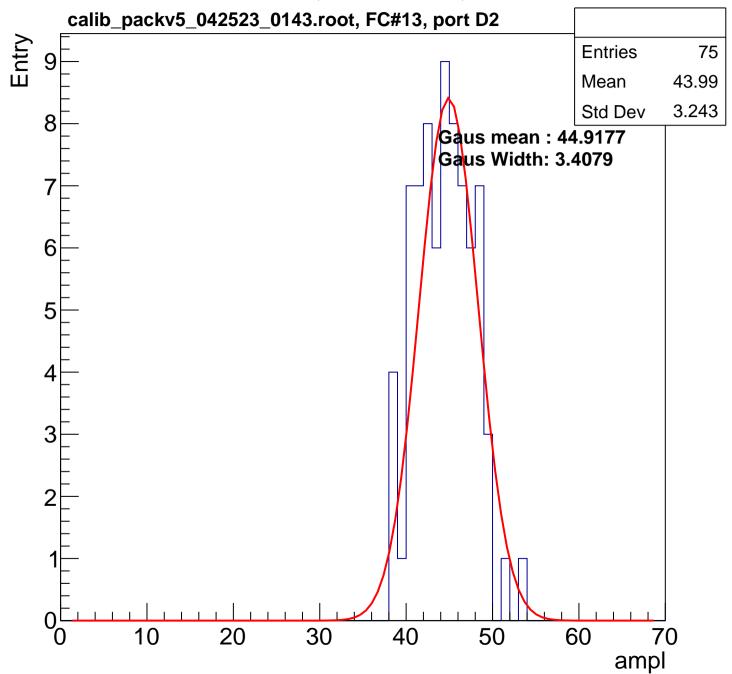


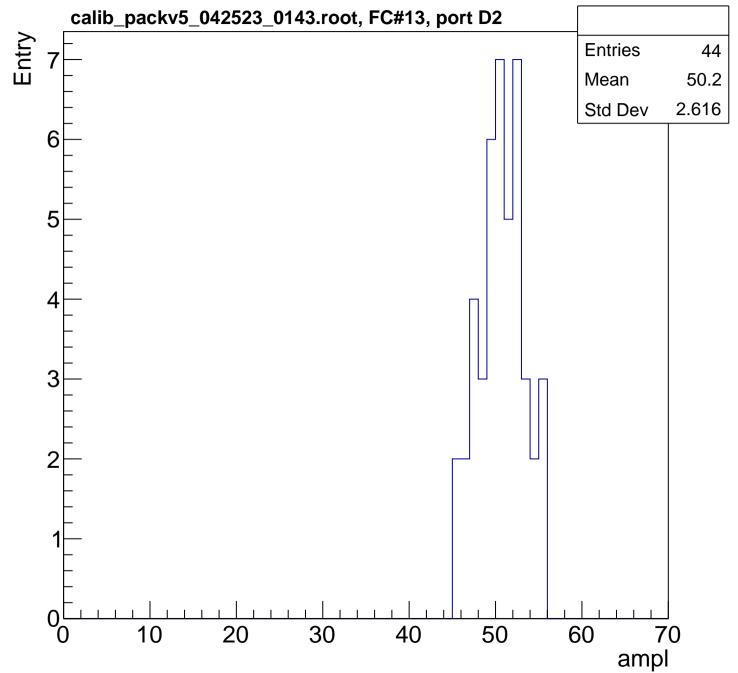


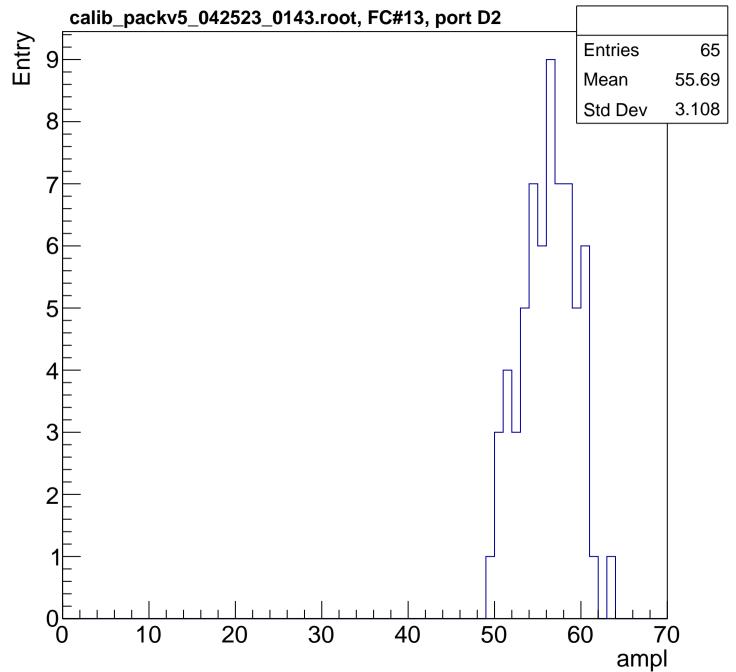


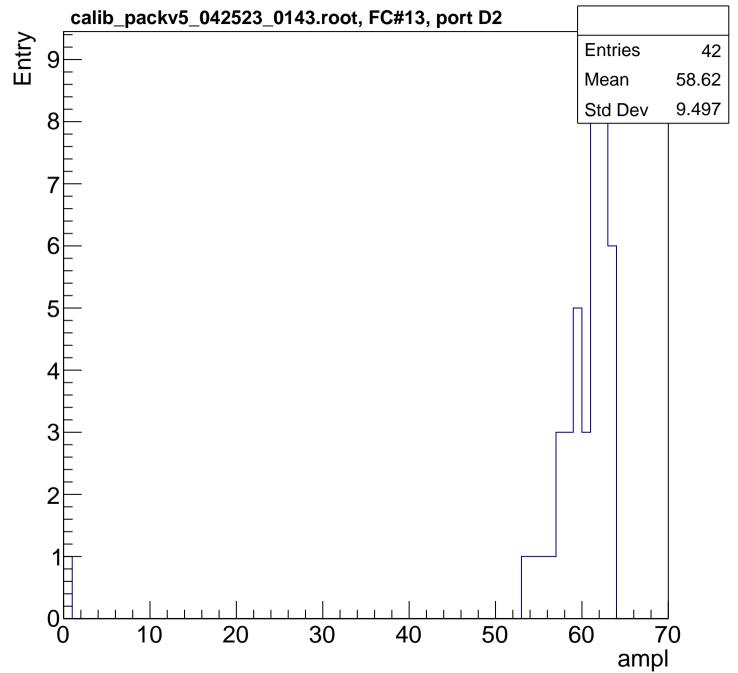


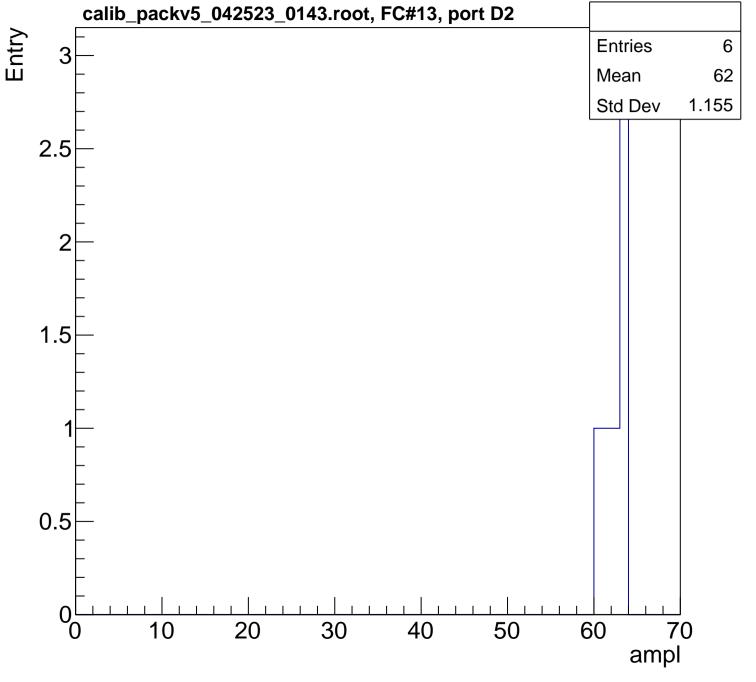


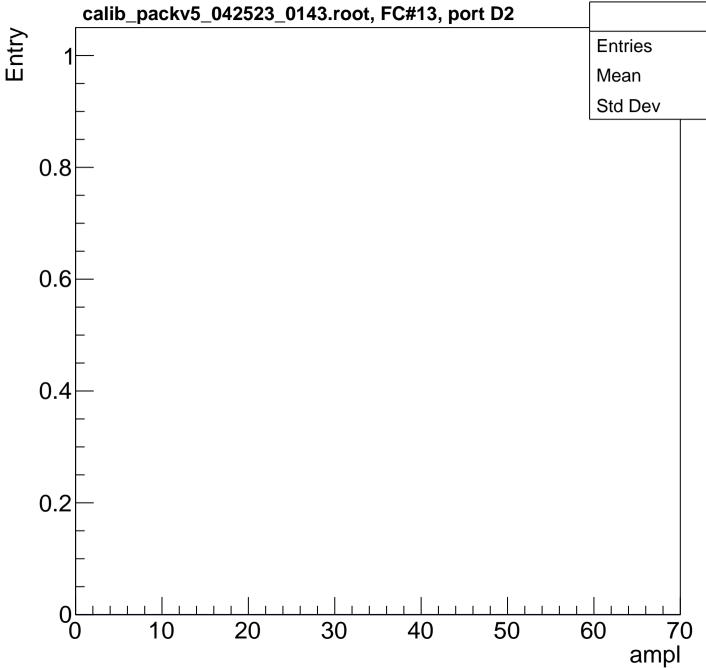


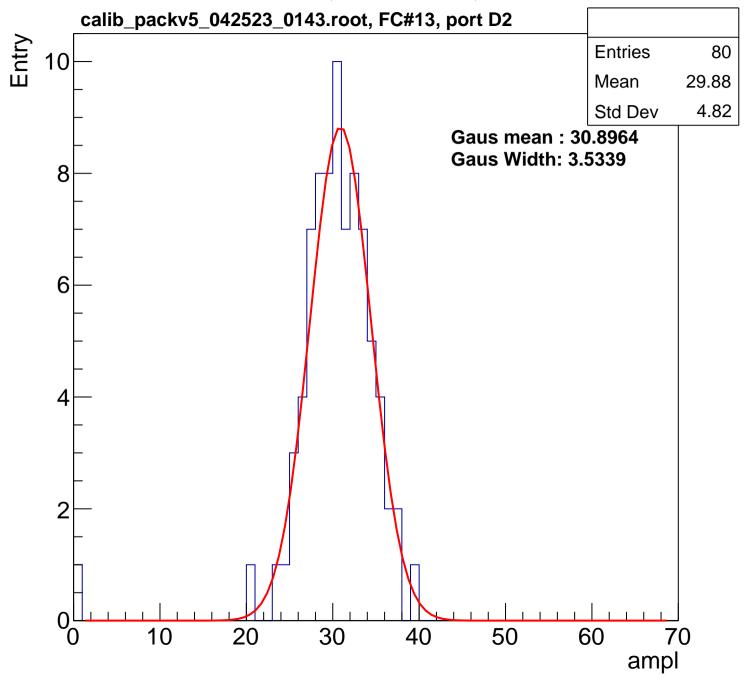


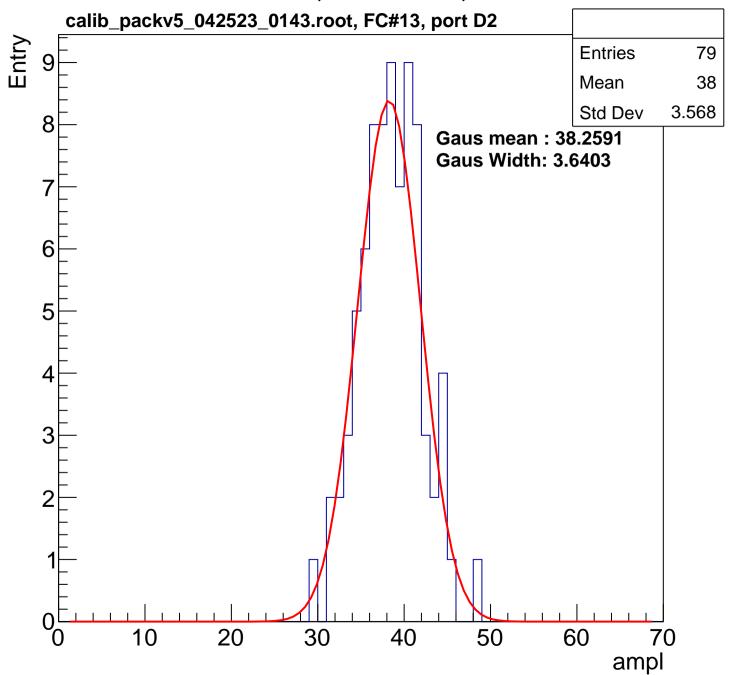


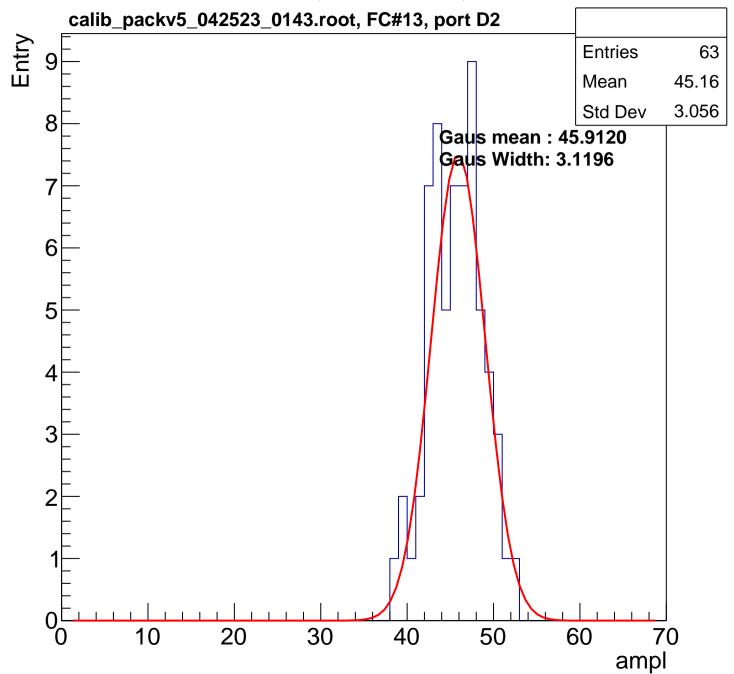


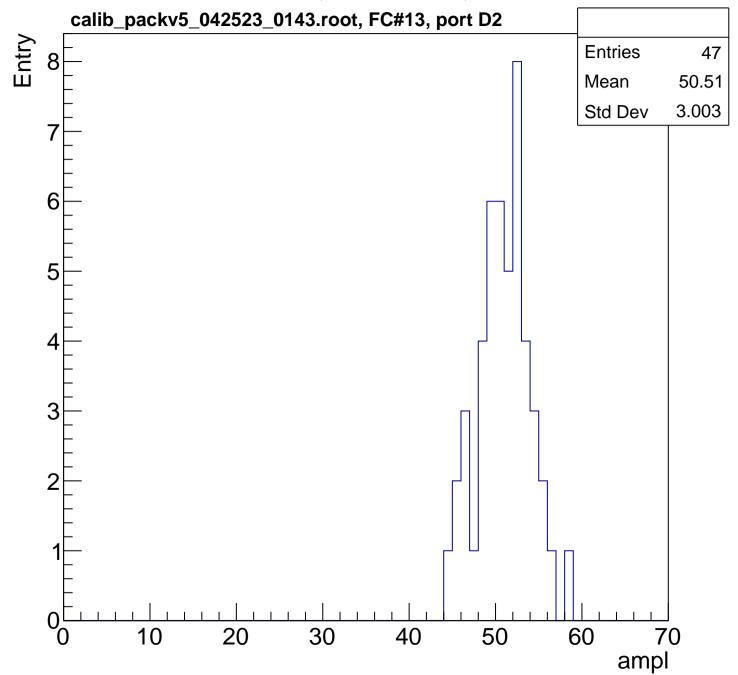


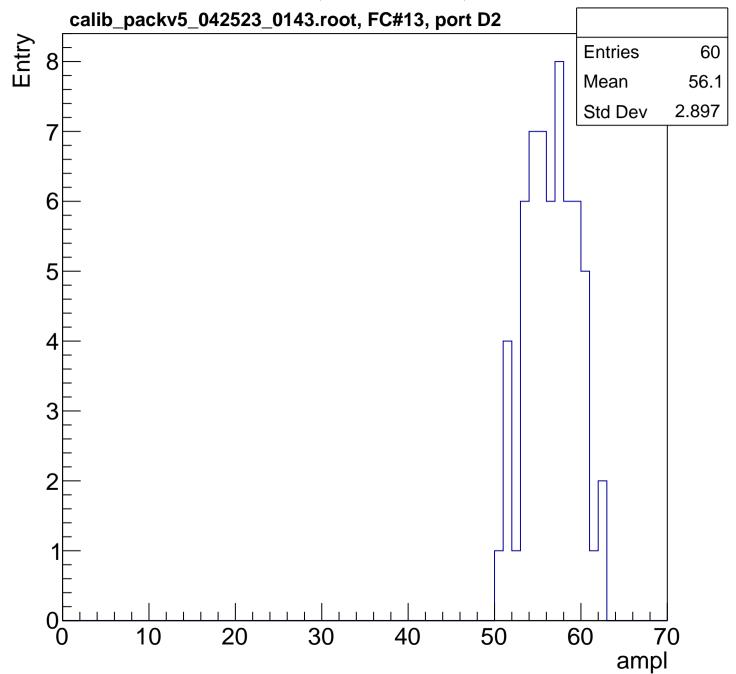


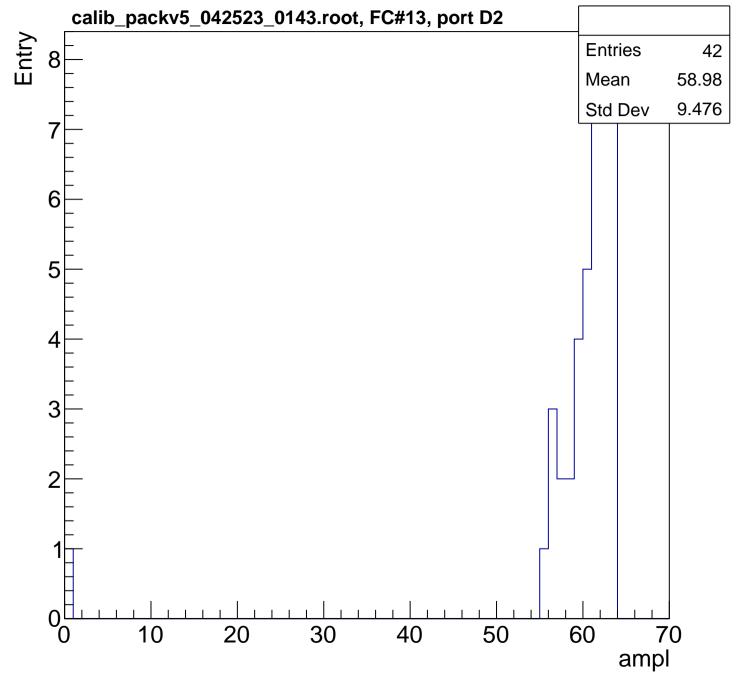


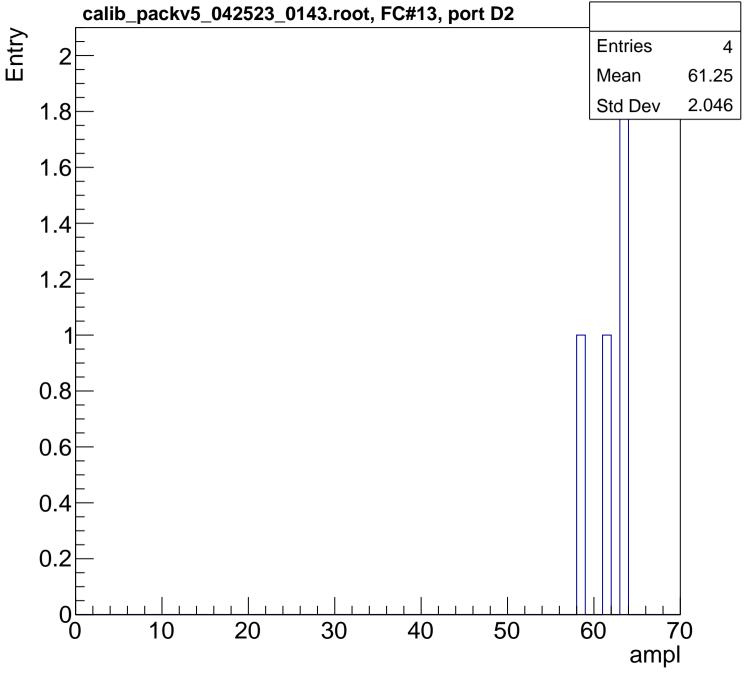




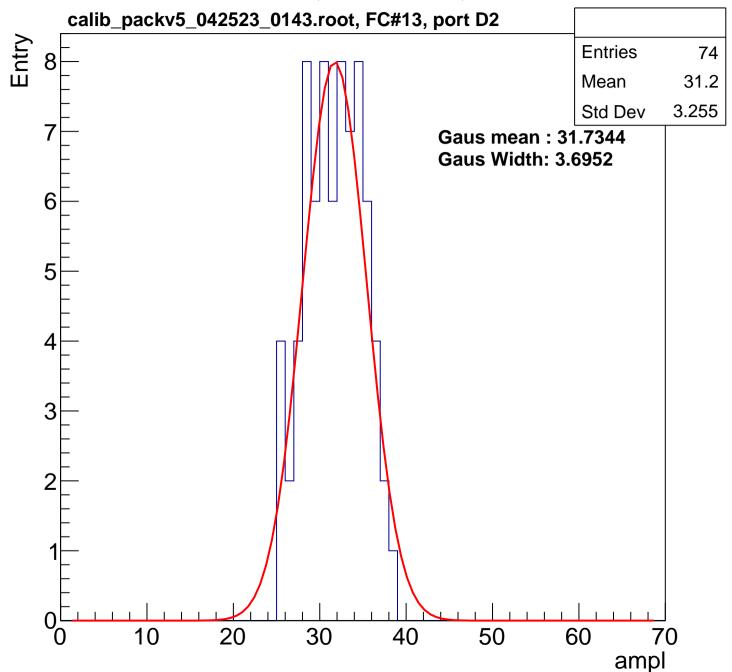


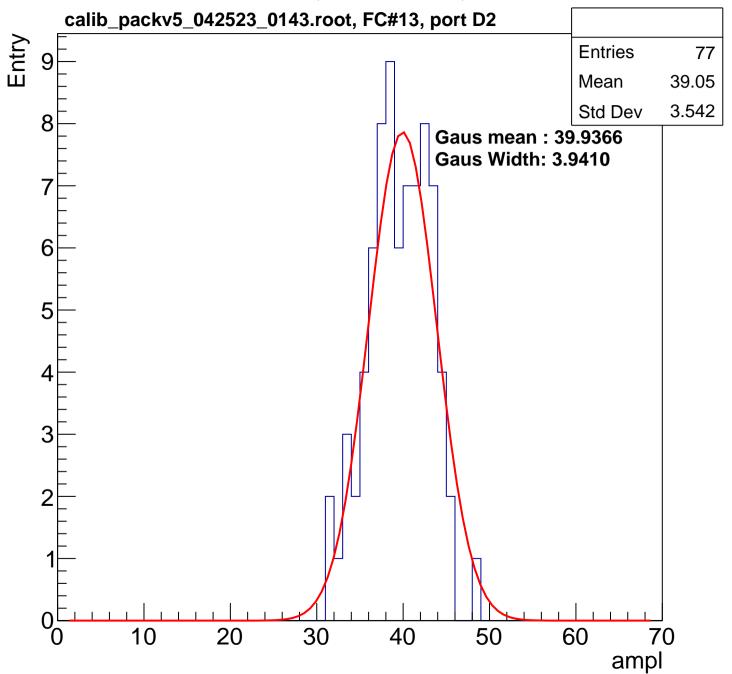


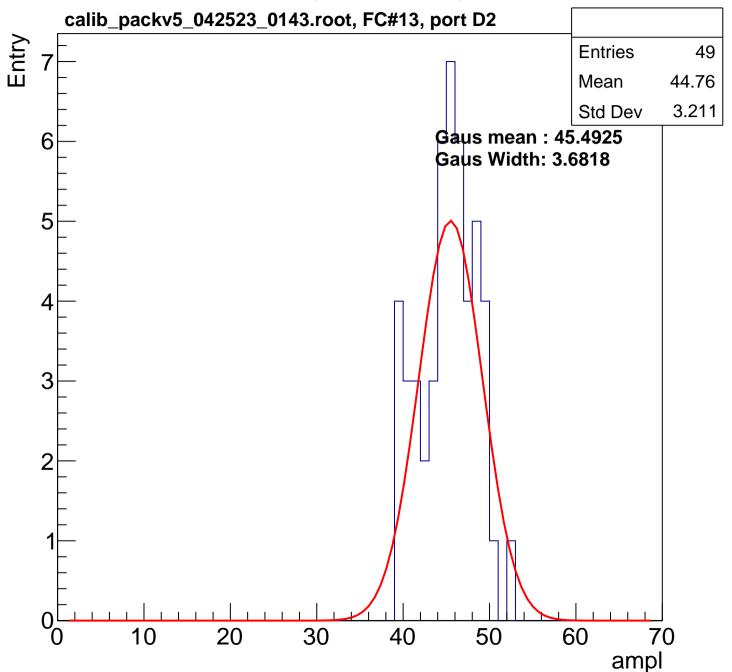


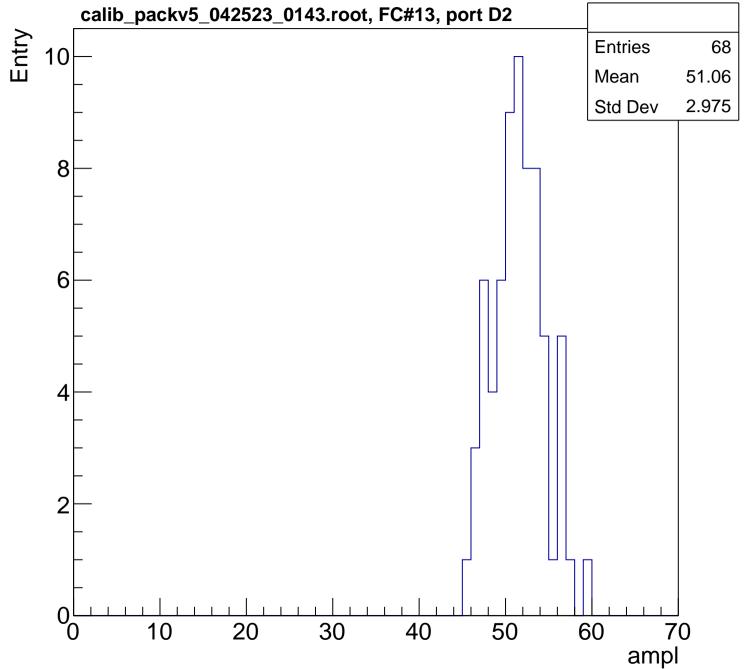


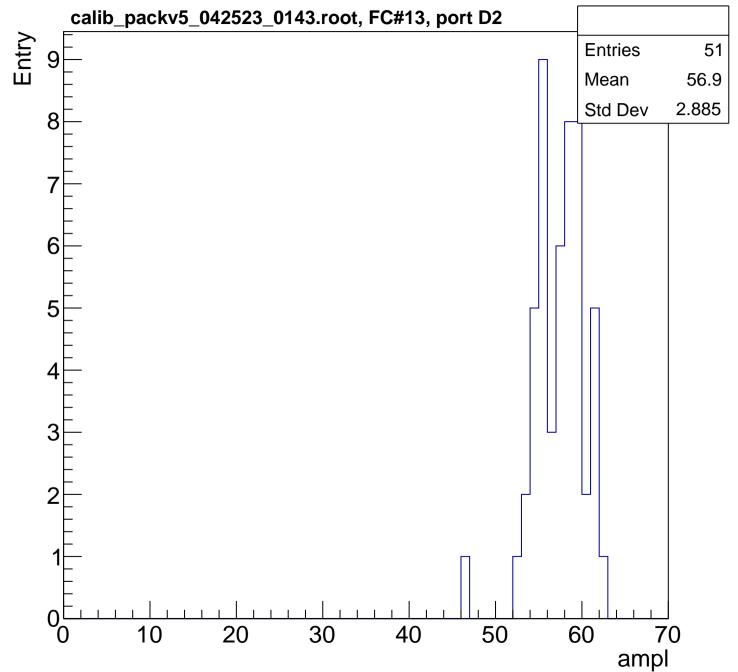


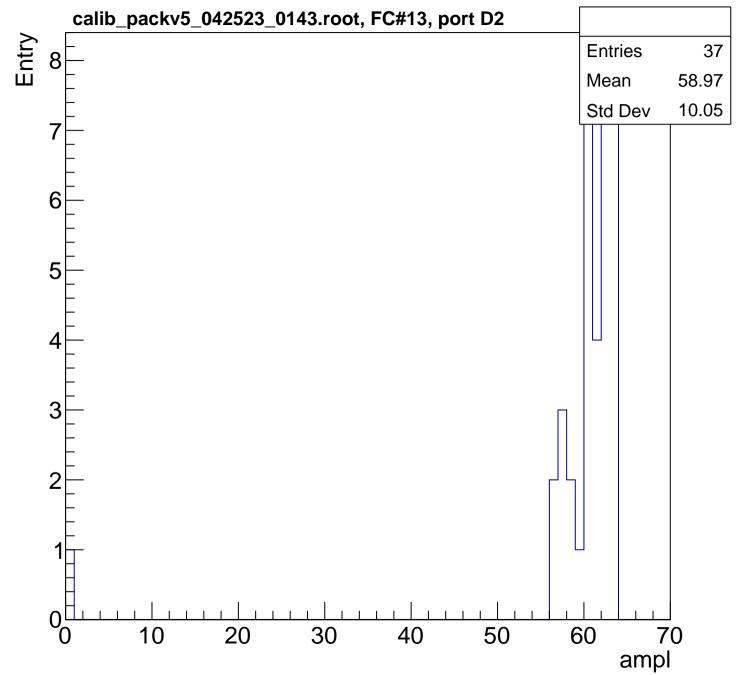


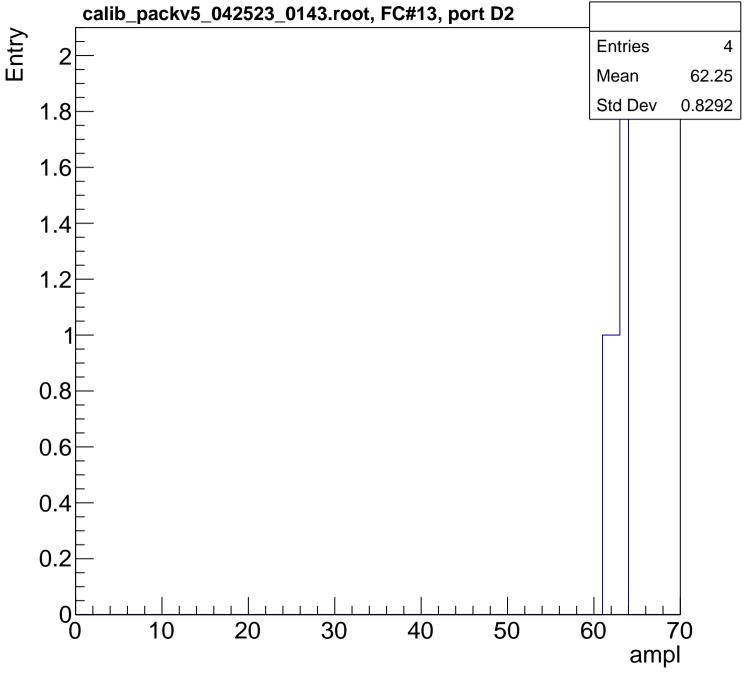


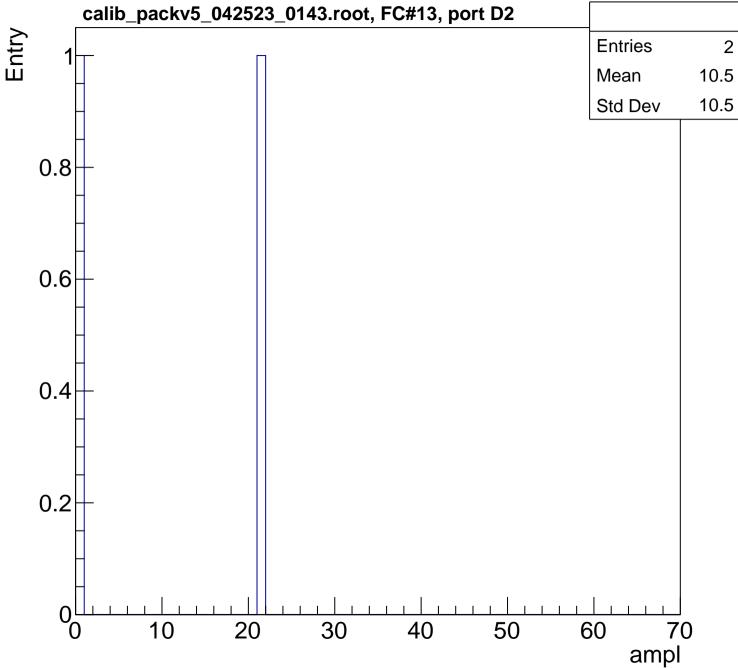


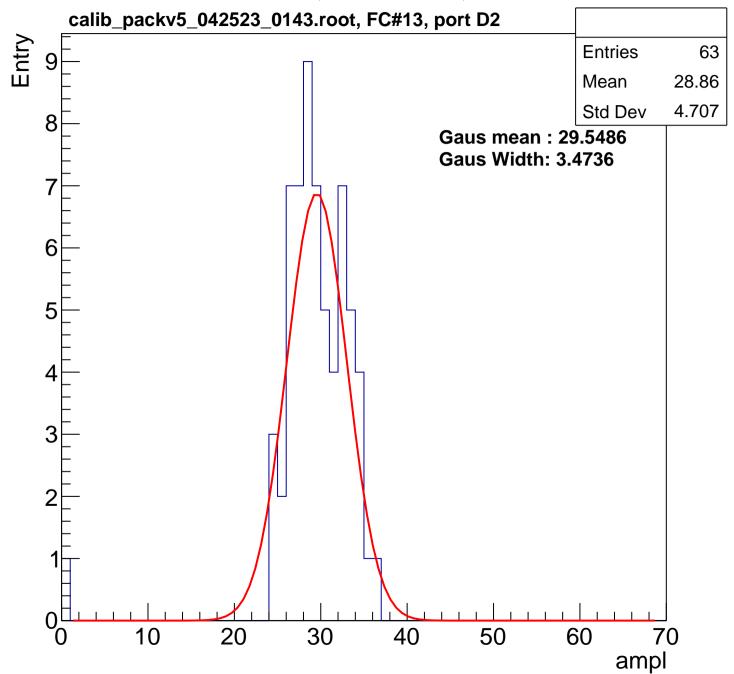


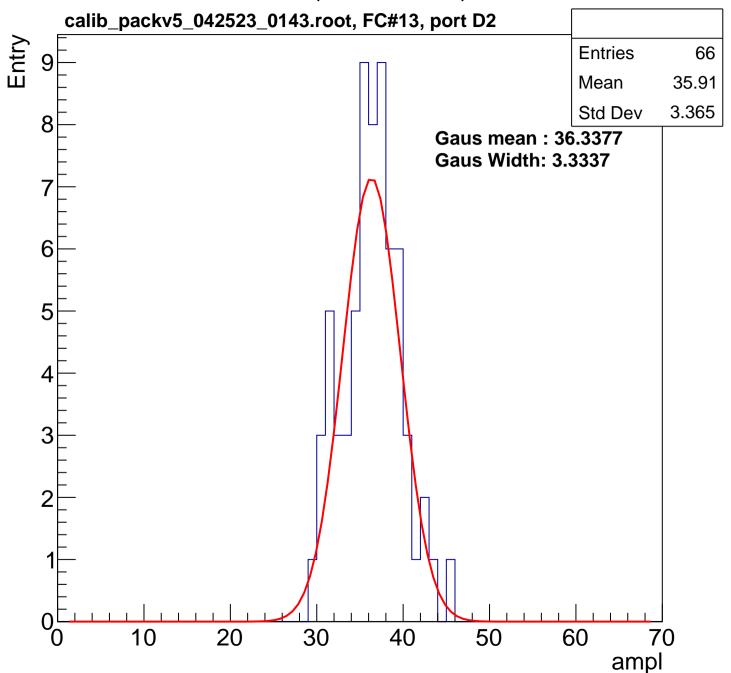


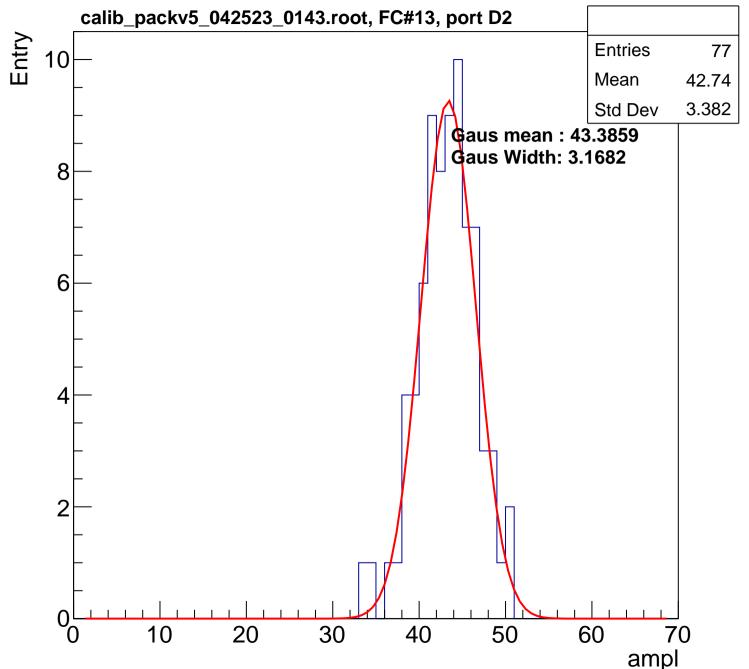


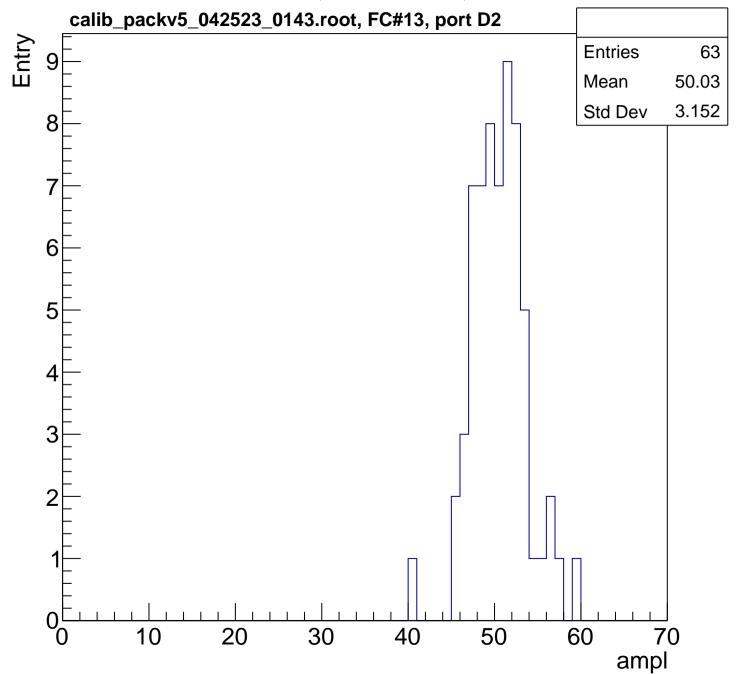


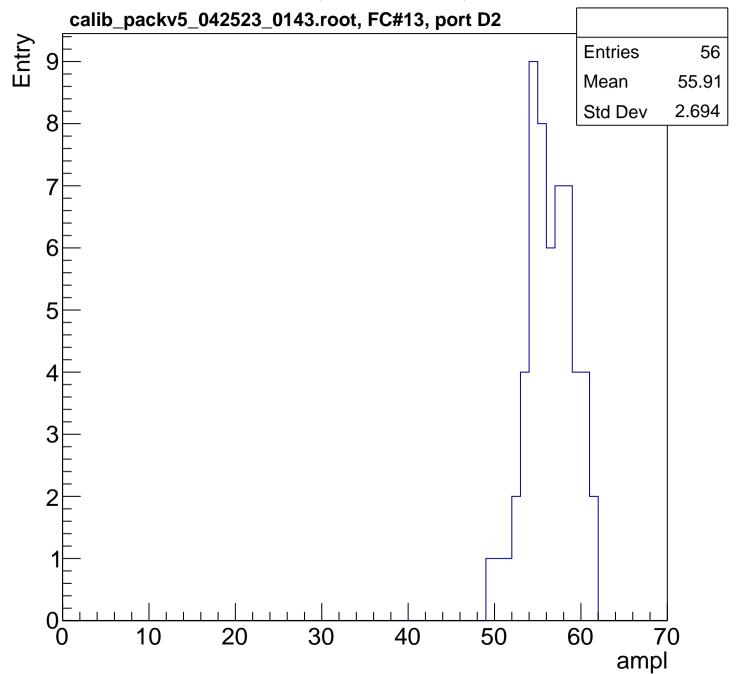


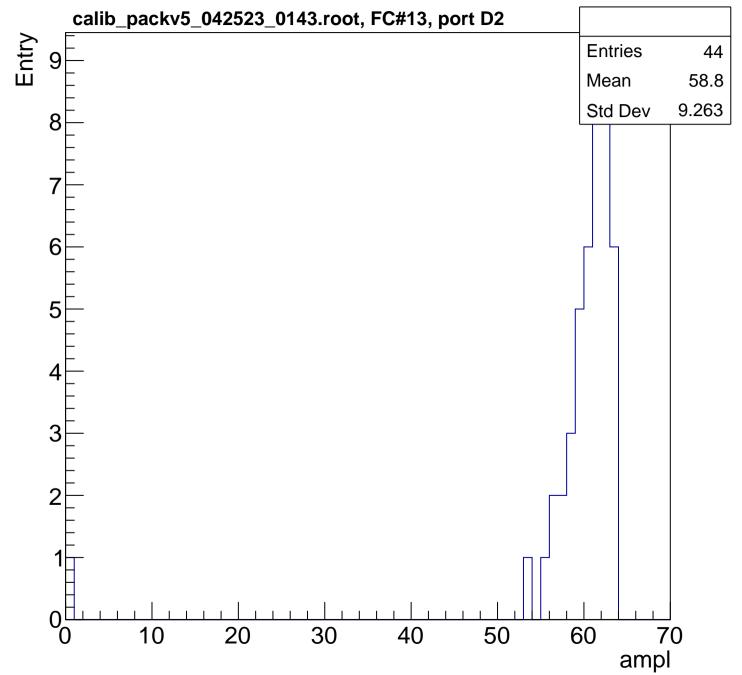


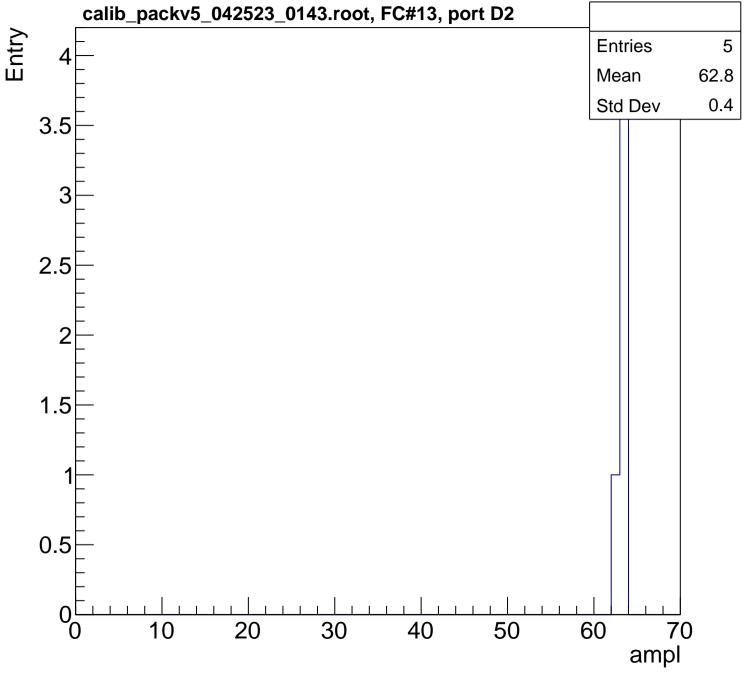




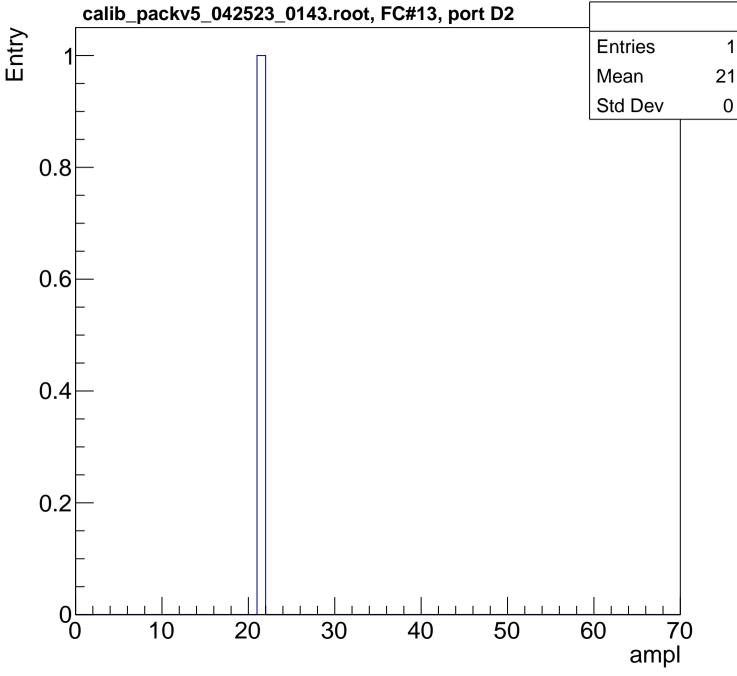


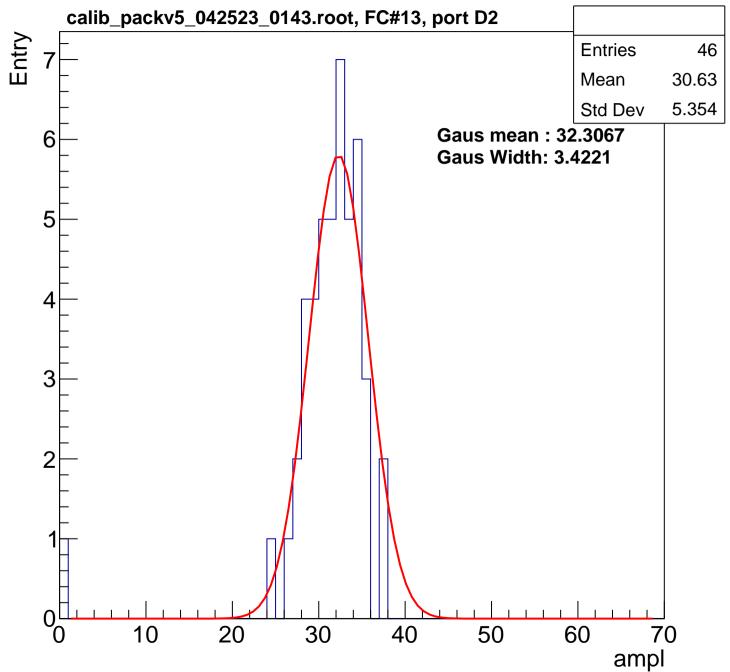


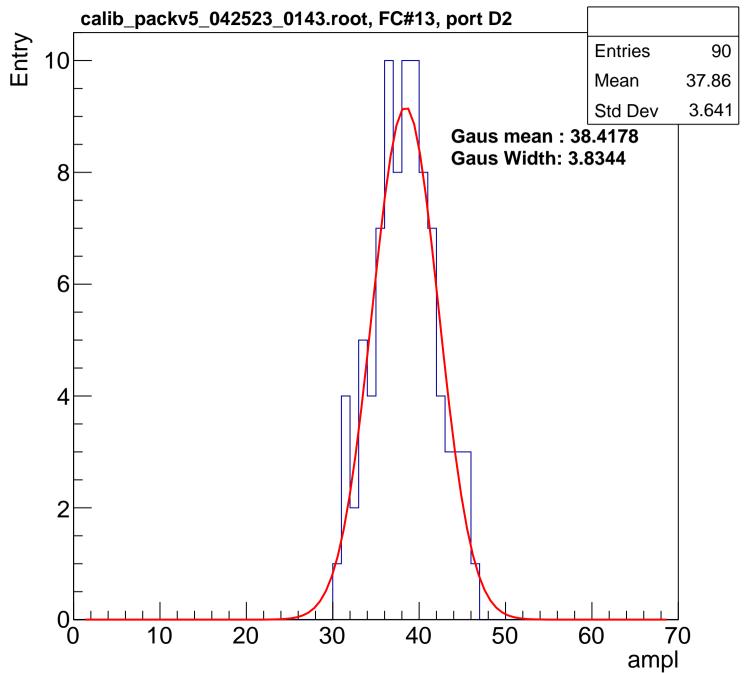


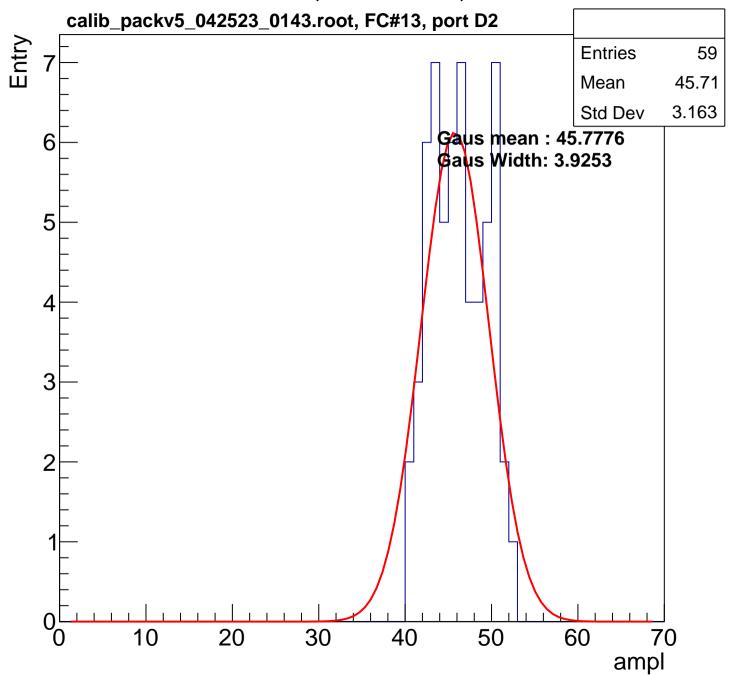


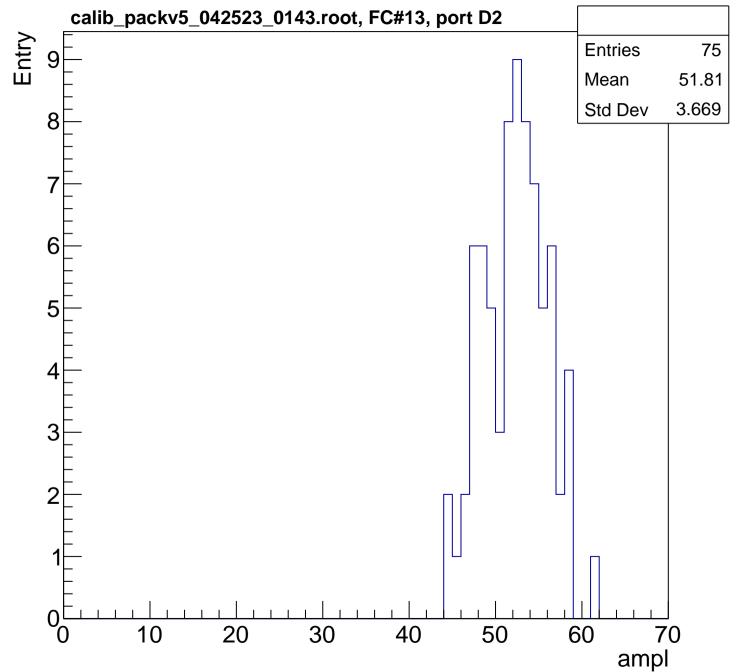
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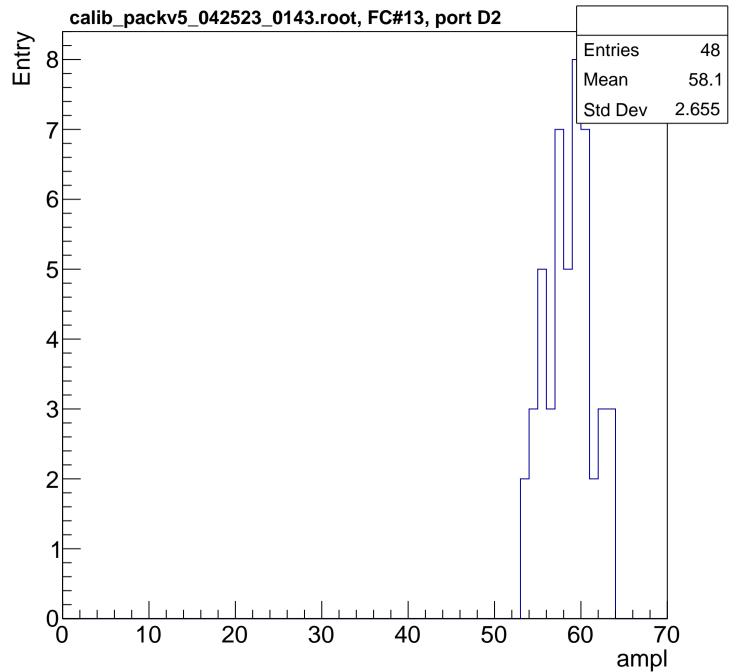


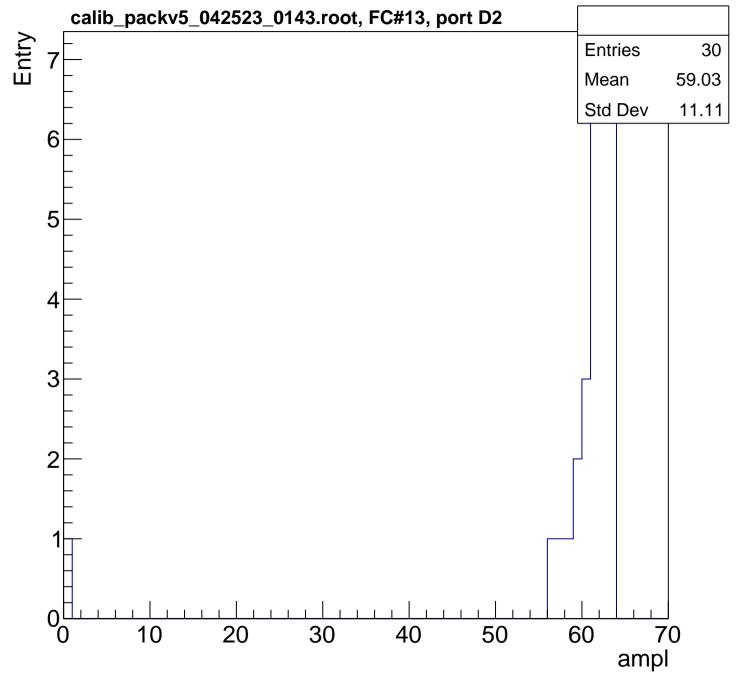


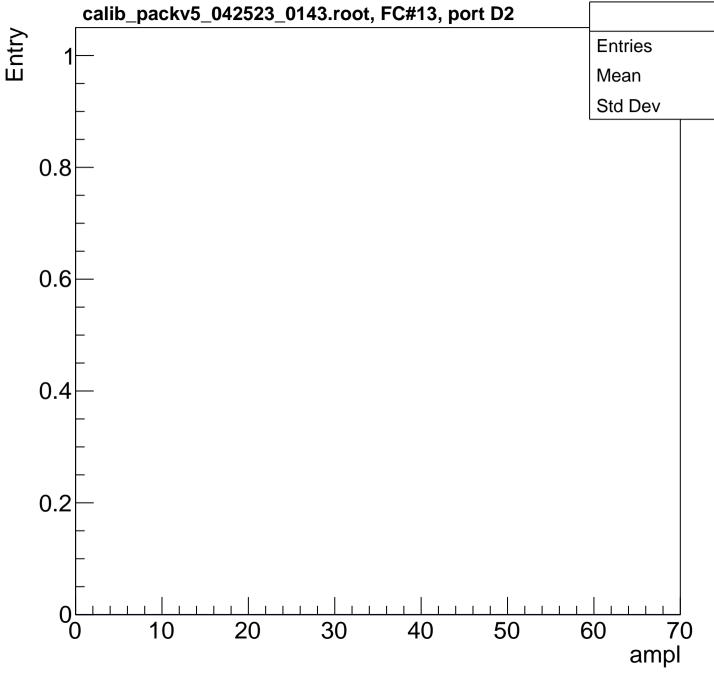




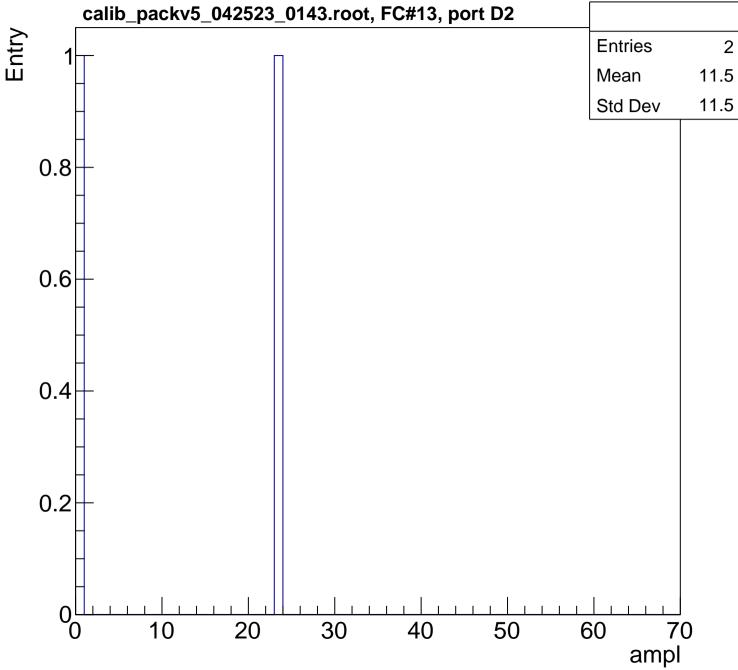


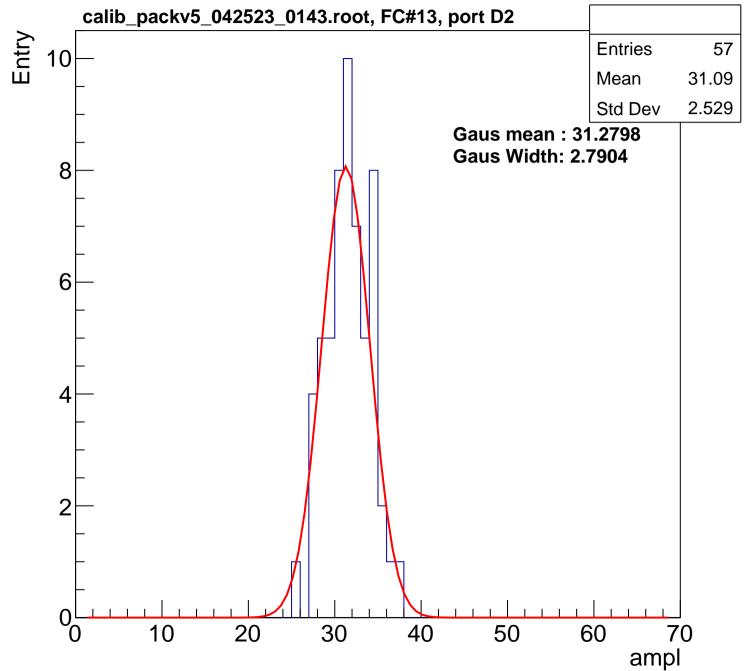


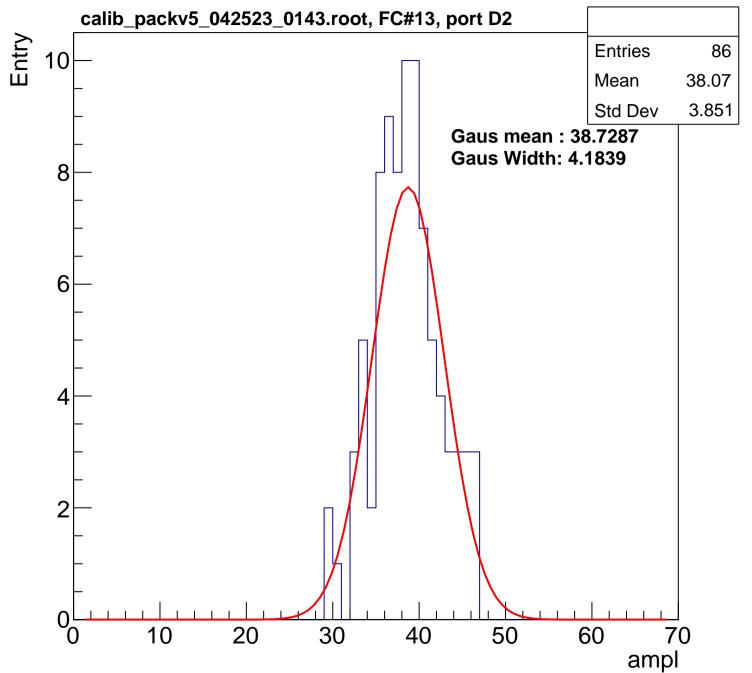


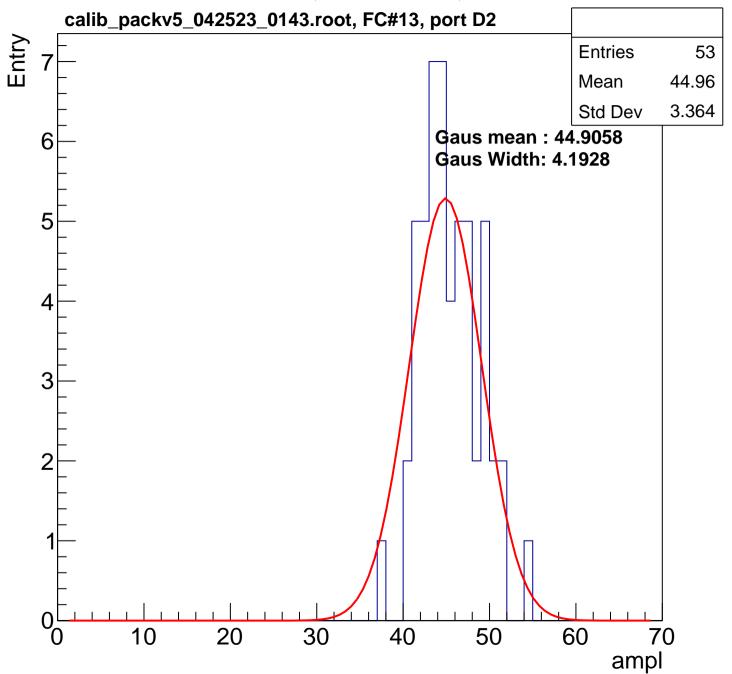


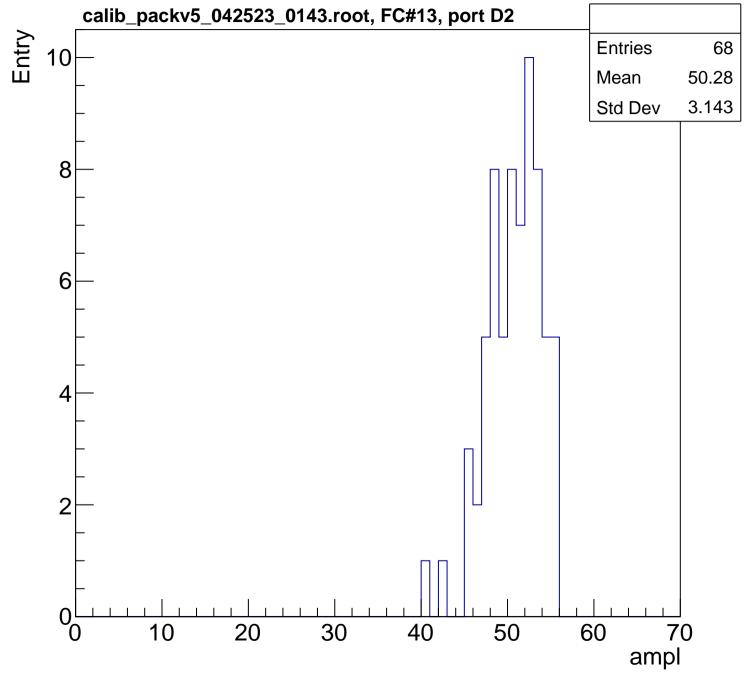
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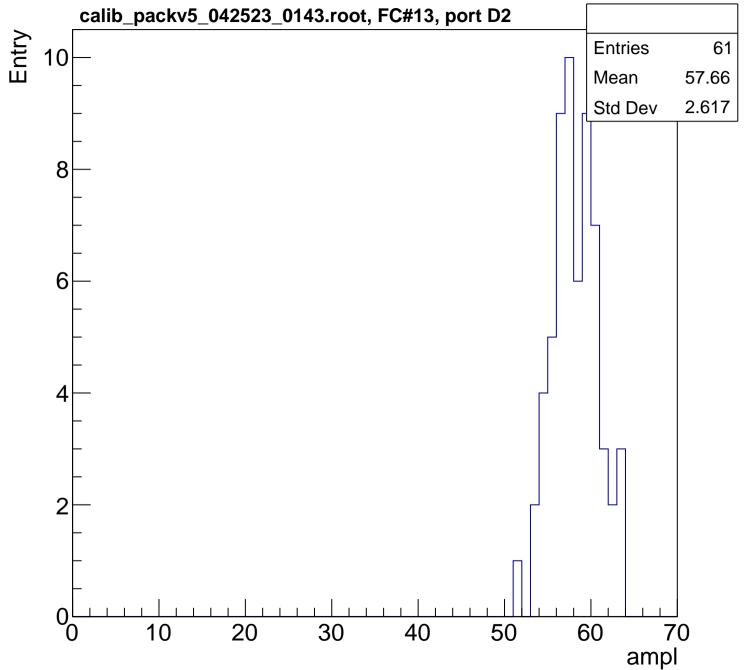


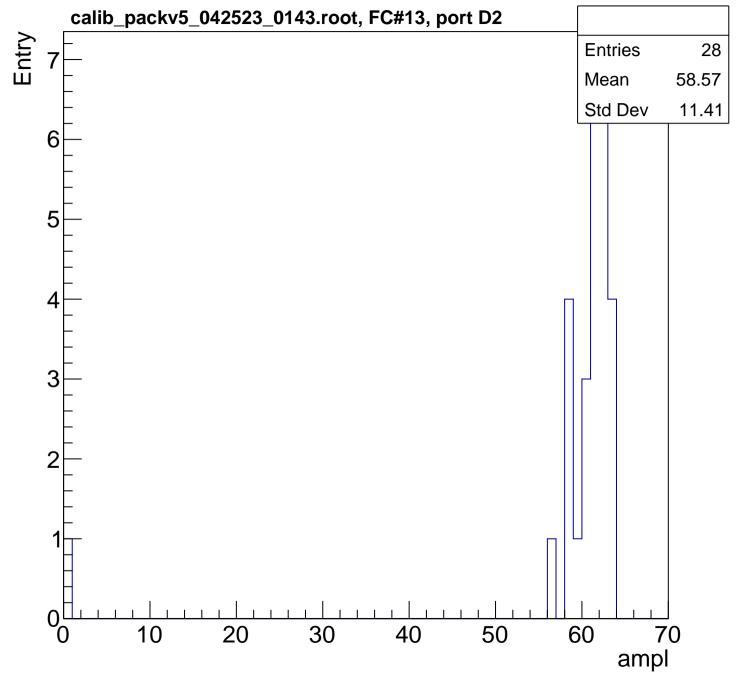


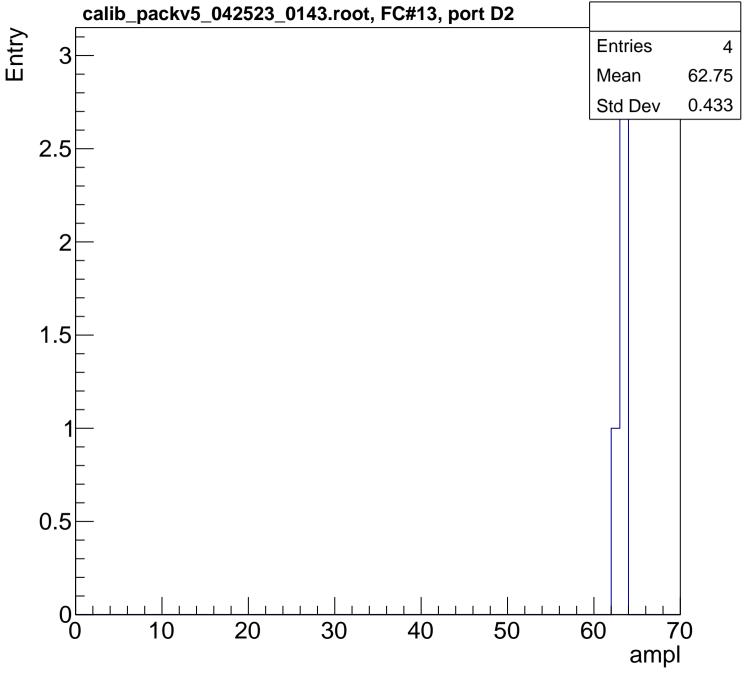




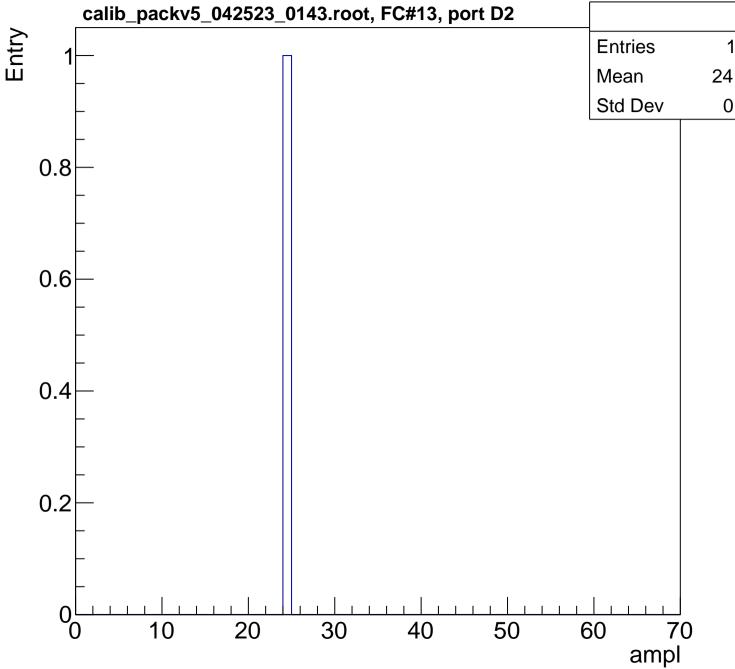


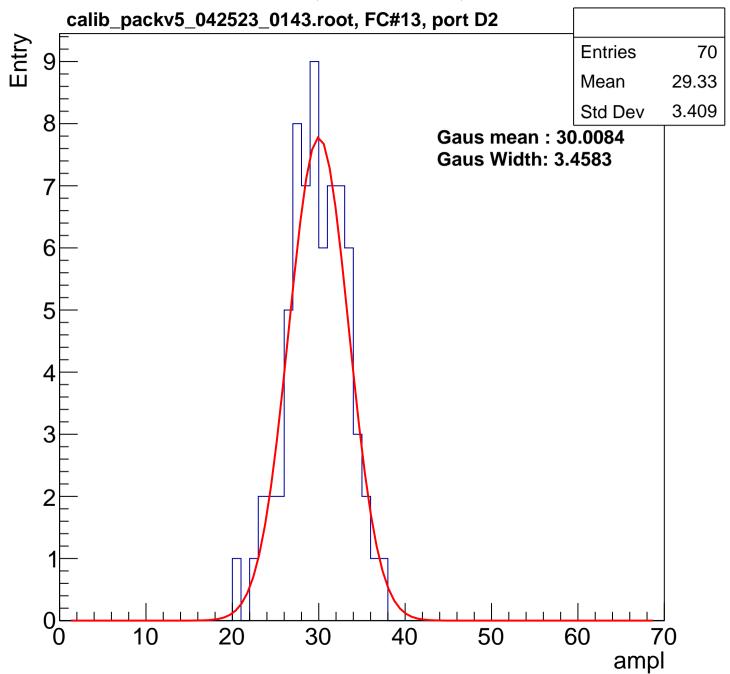


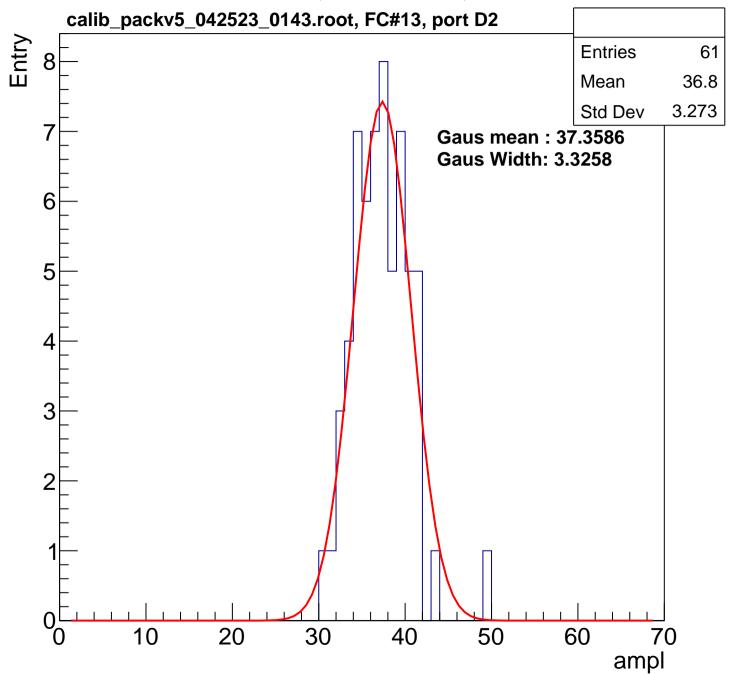


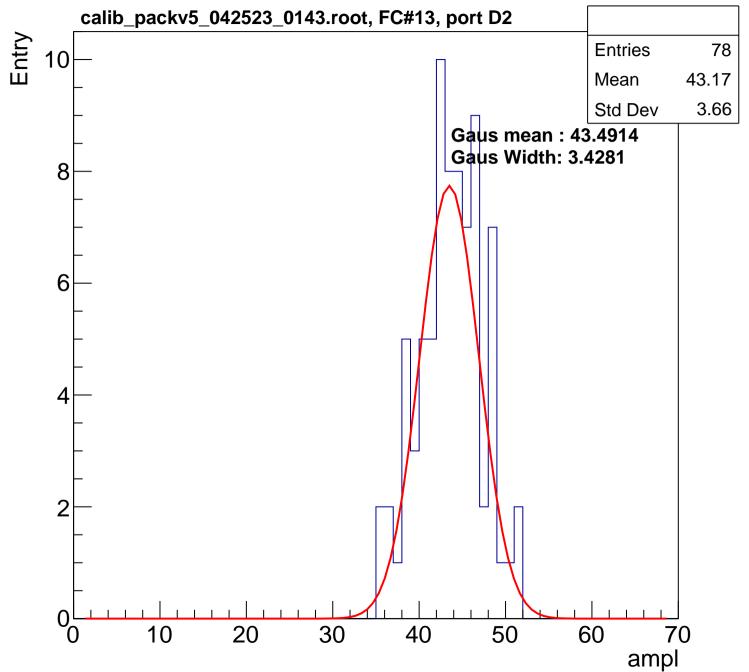


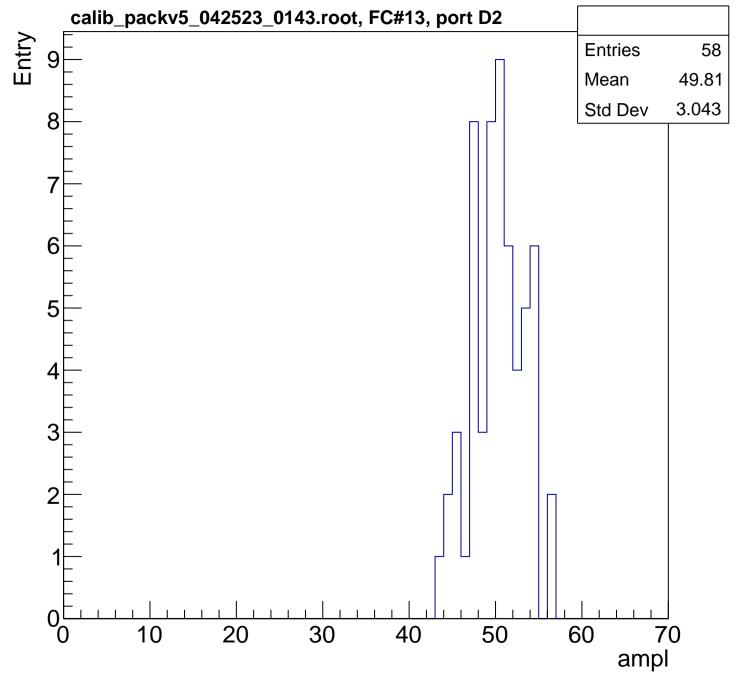
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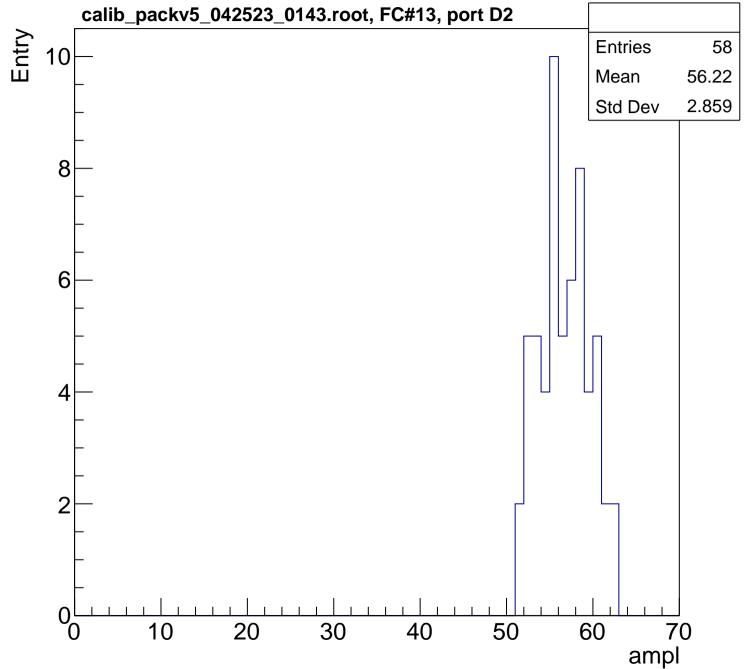


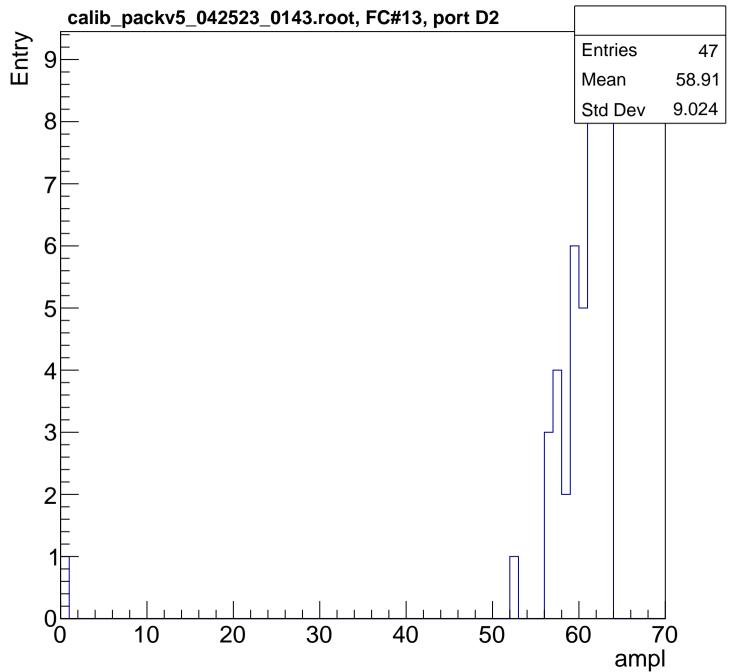


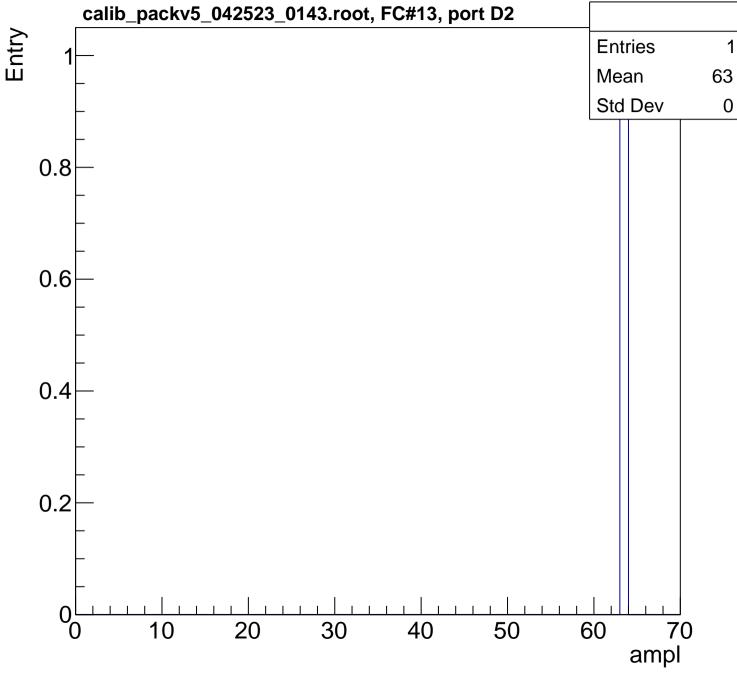




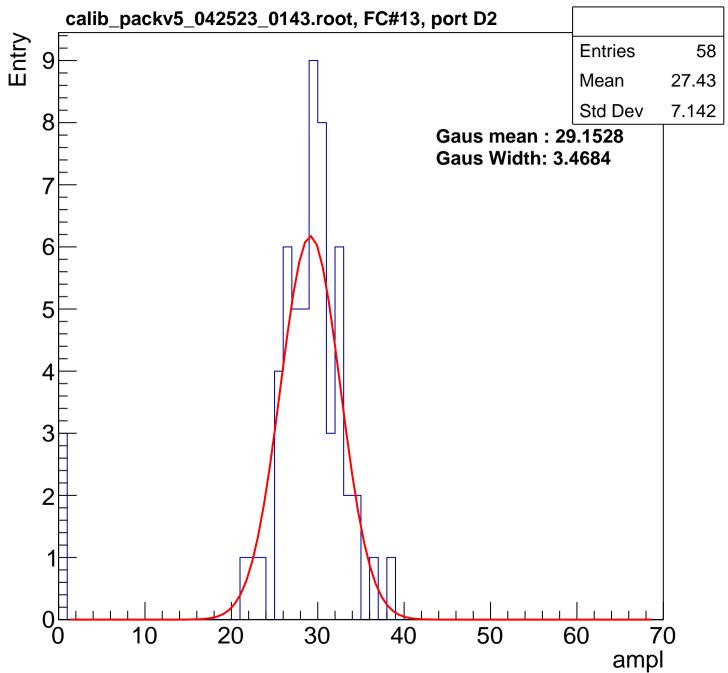


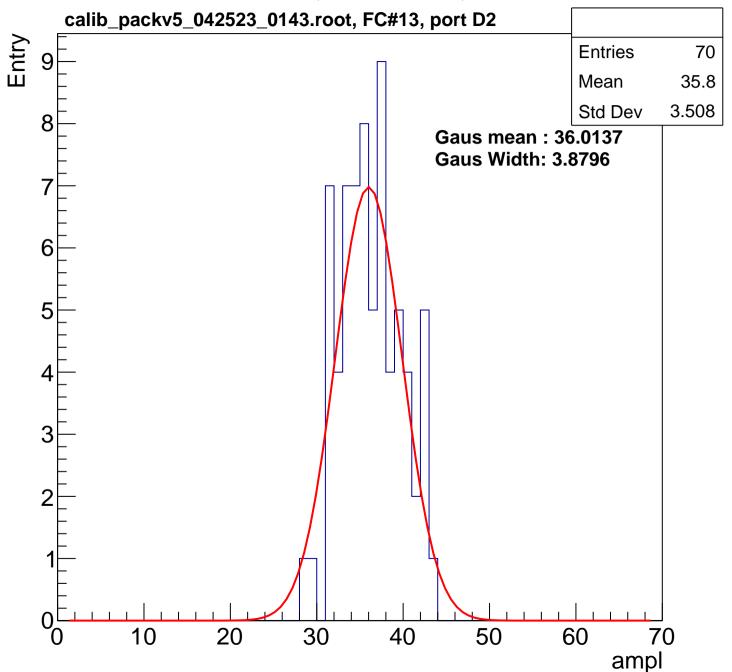


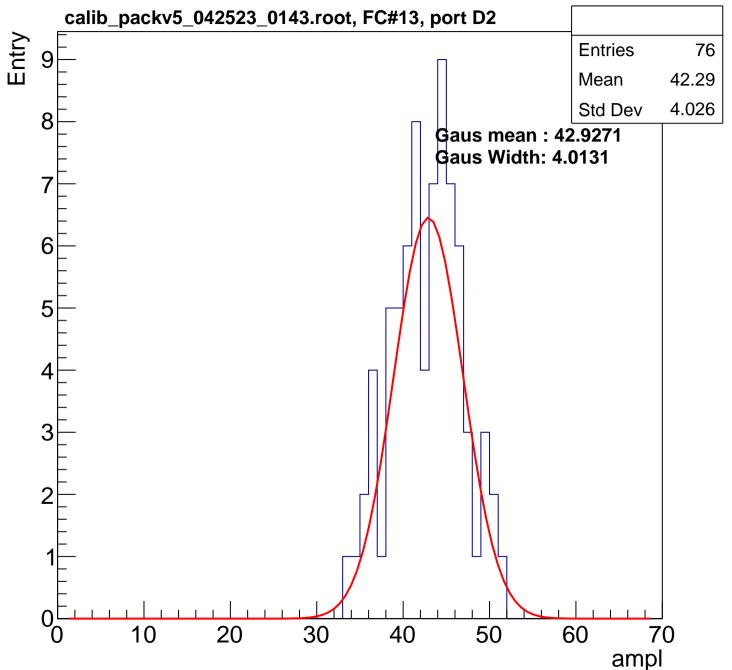


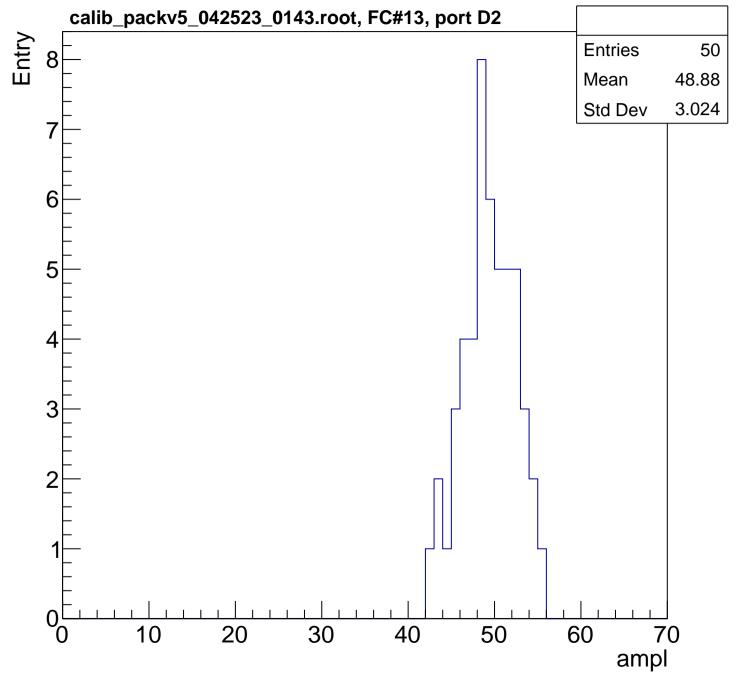


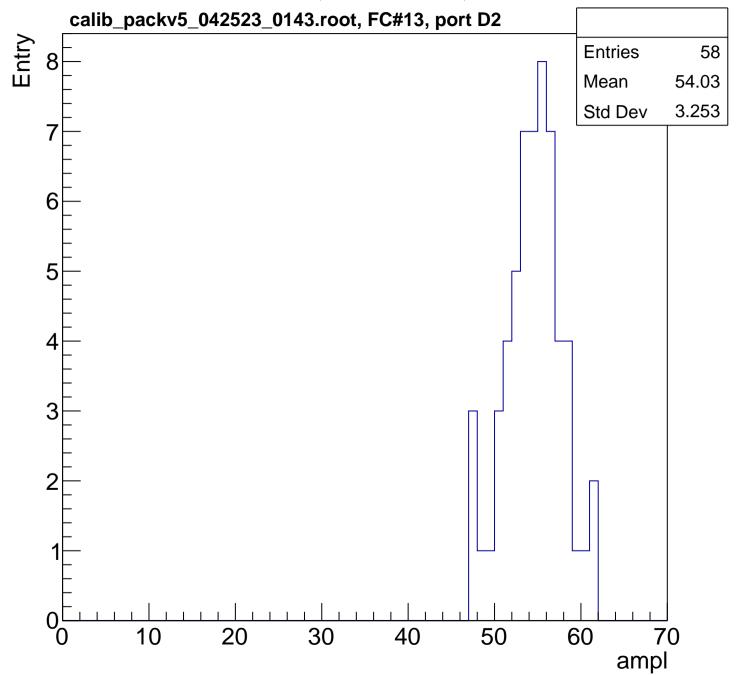


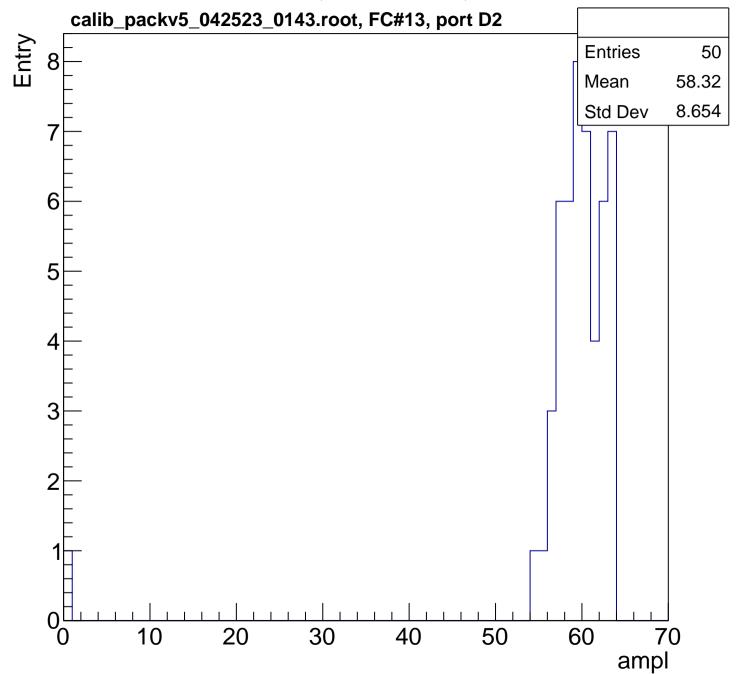


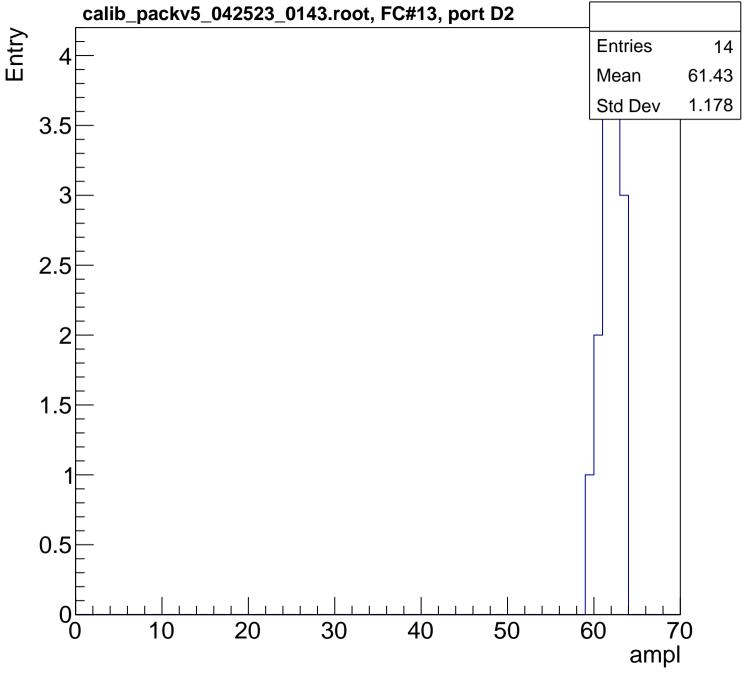




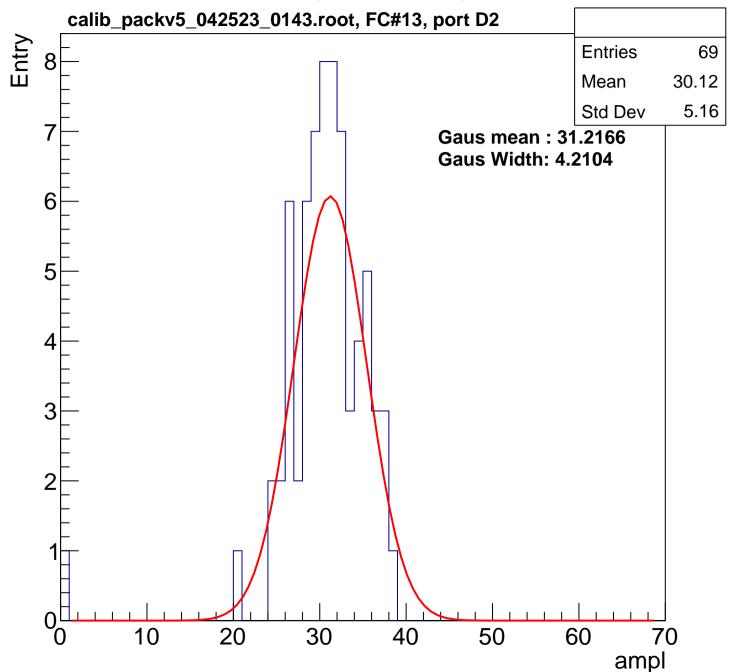


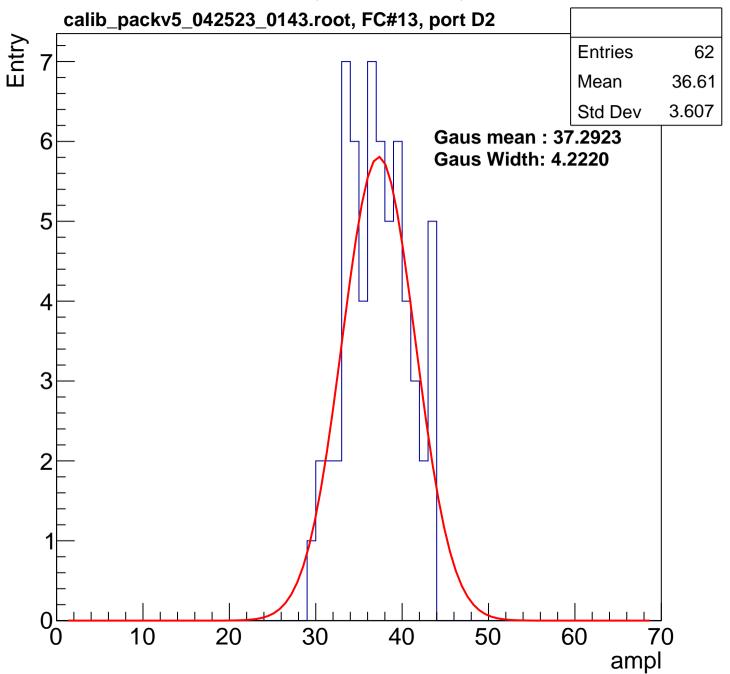


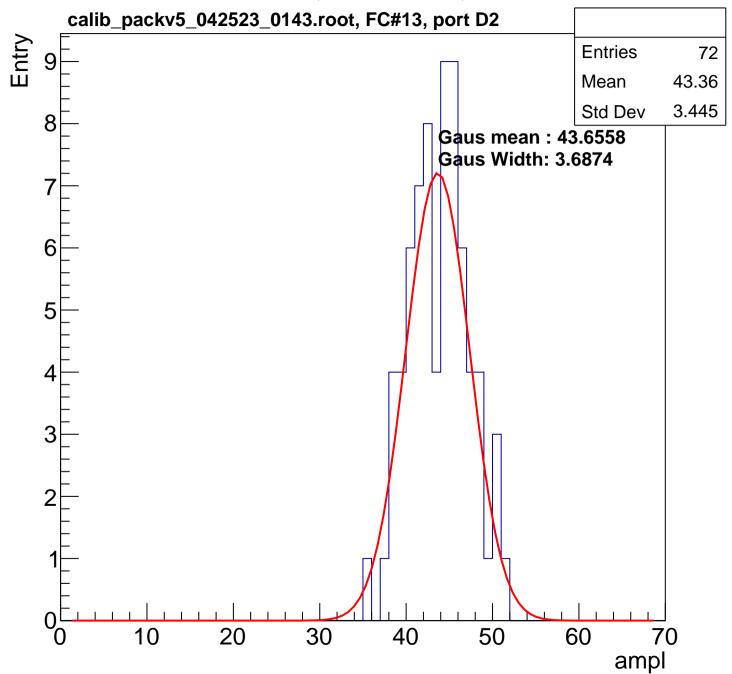


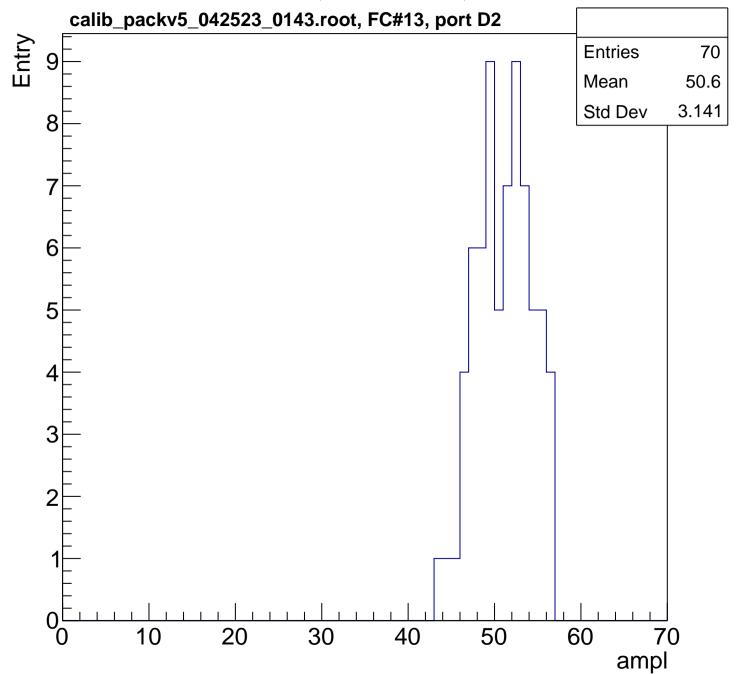


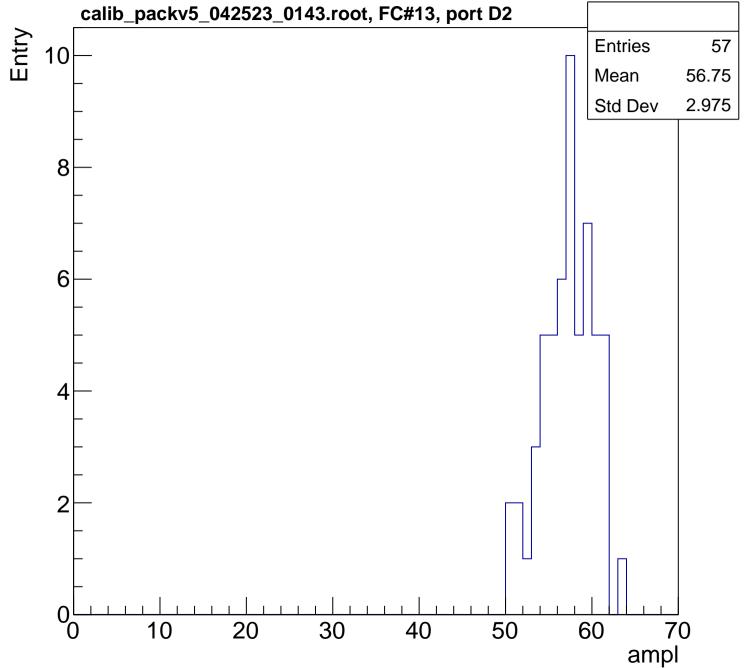
B1L003S, U9-ch48, adc7 calib\_packv5\_042523\_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

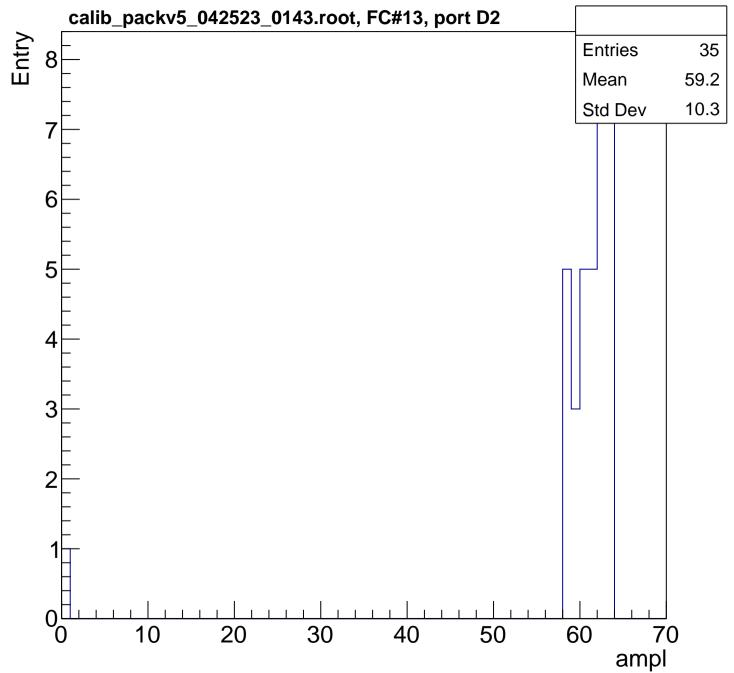


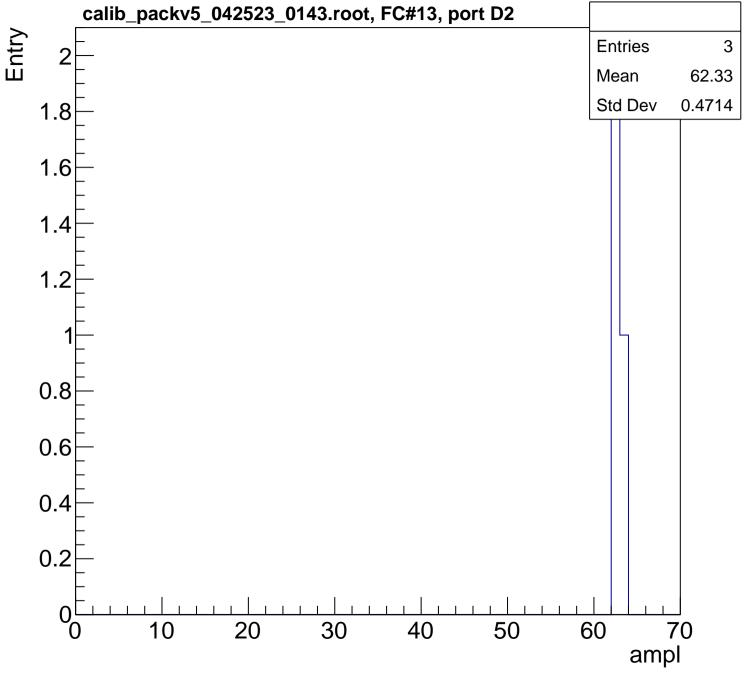




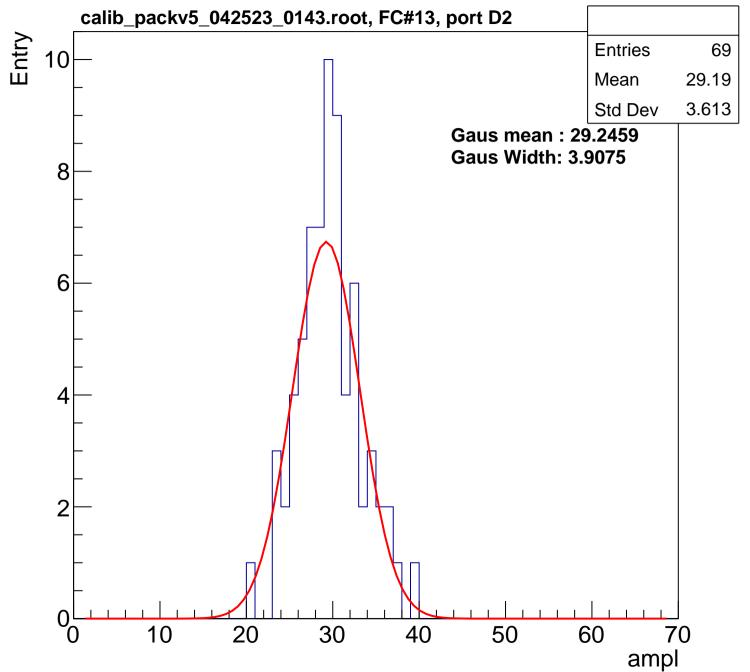


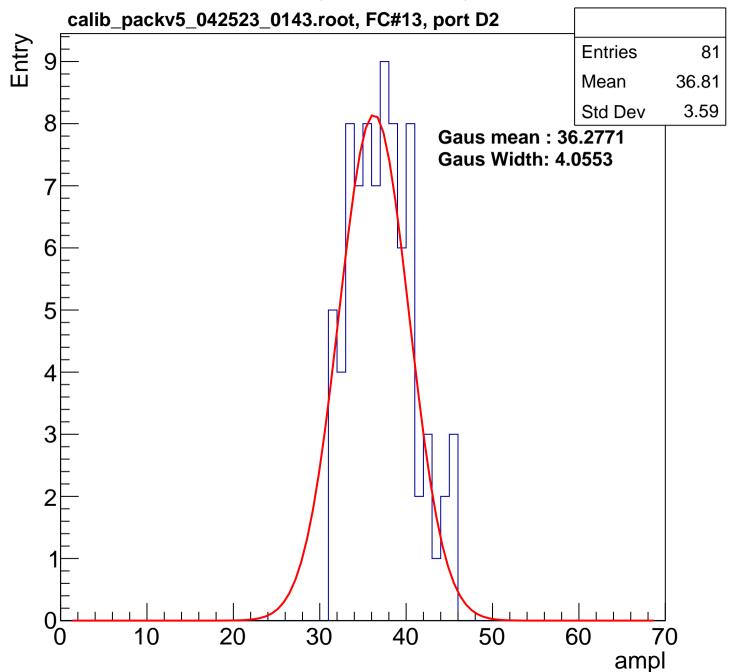


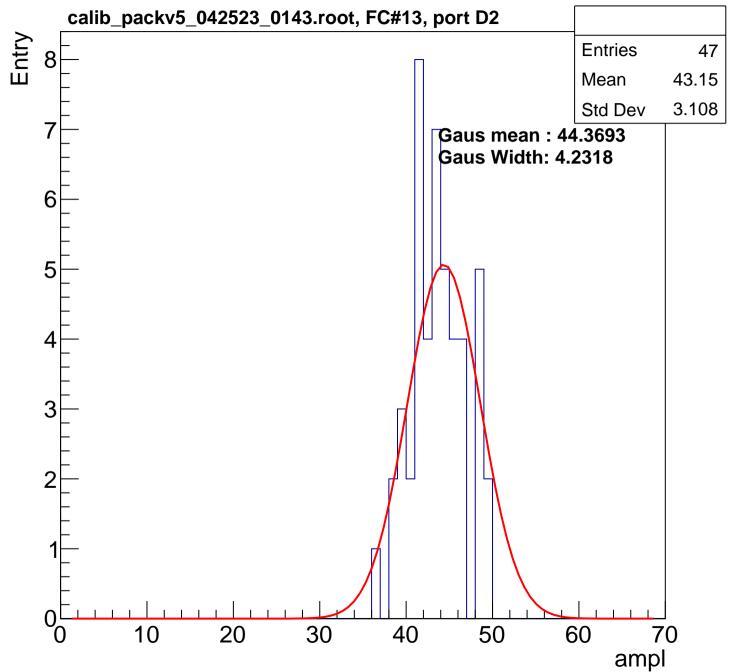


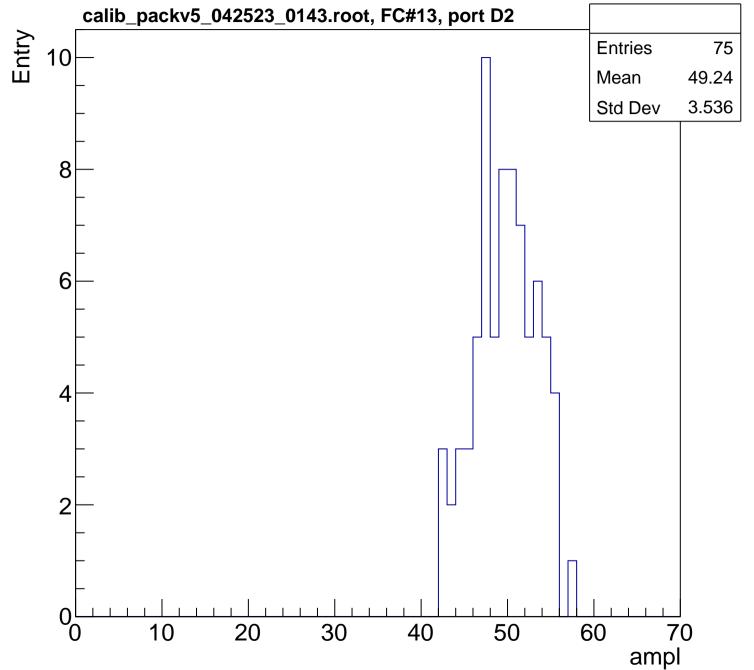


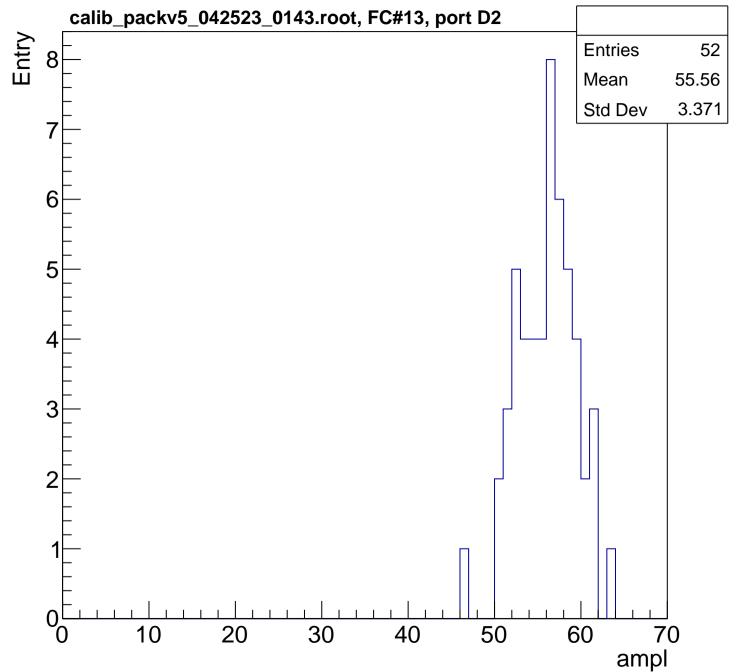


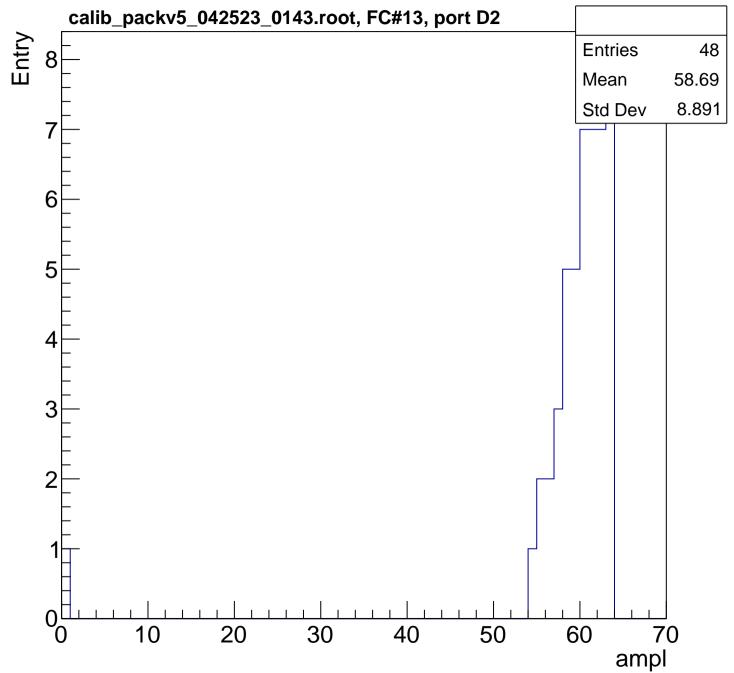


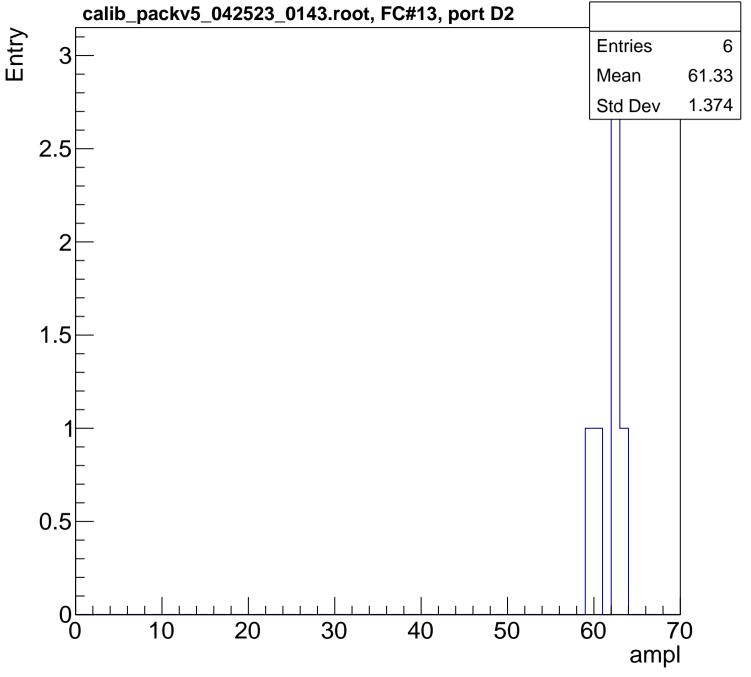




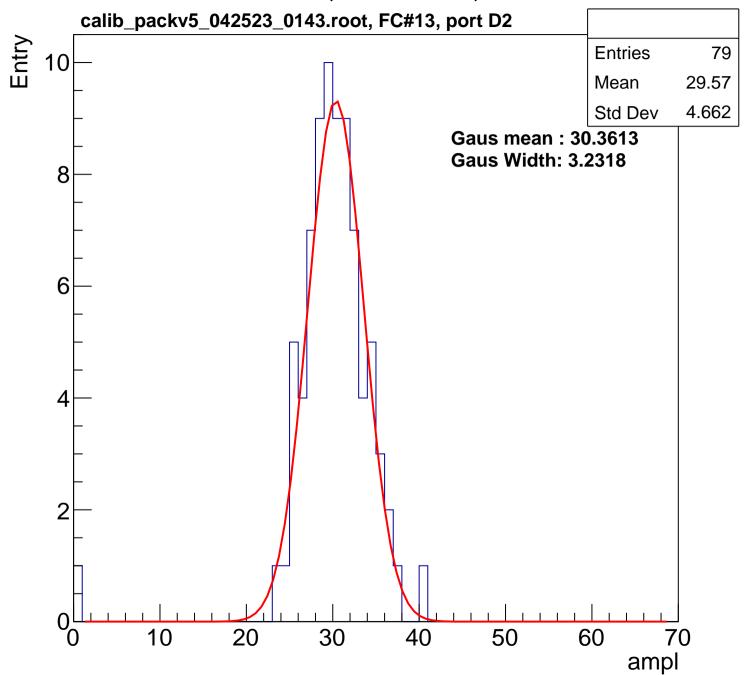


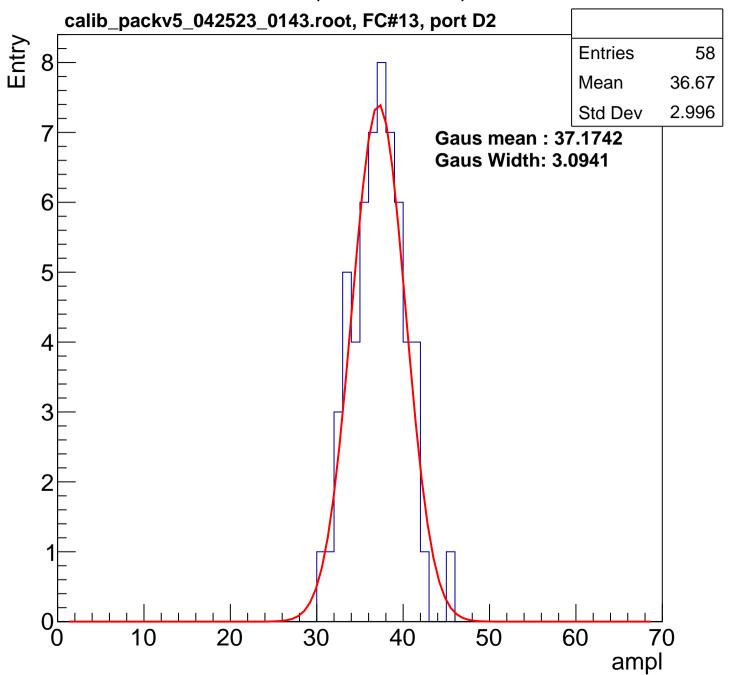


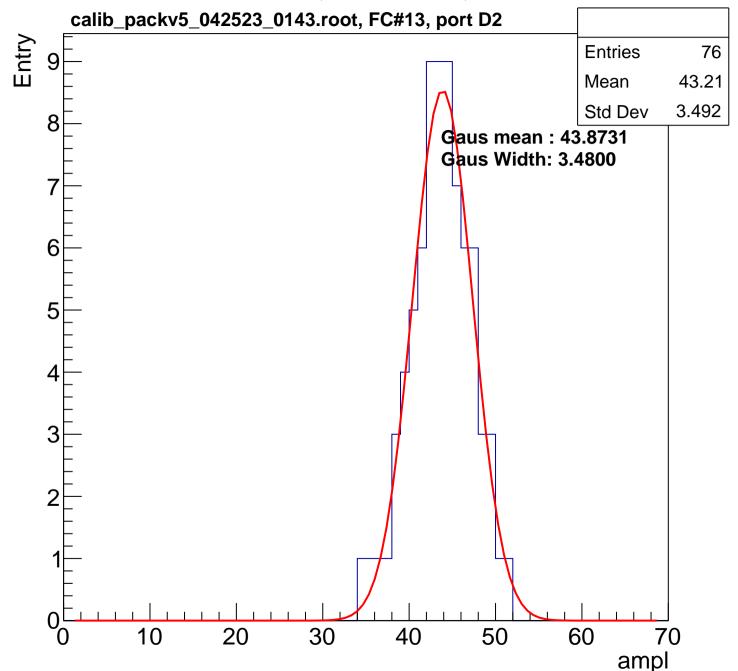


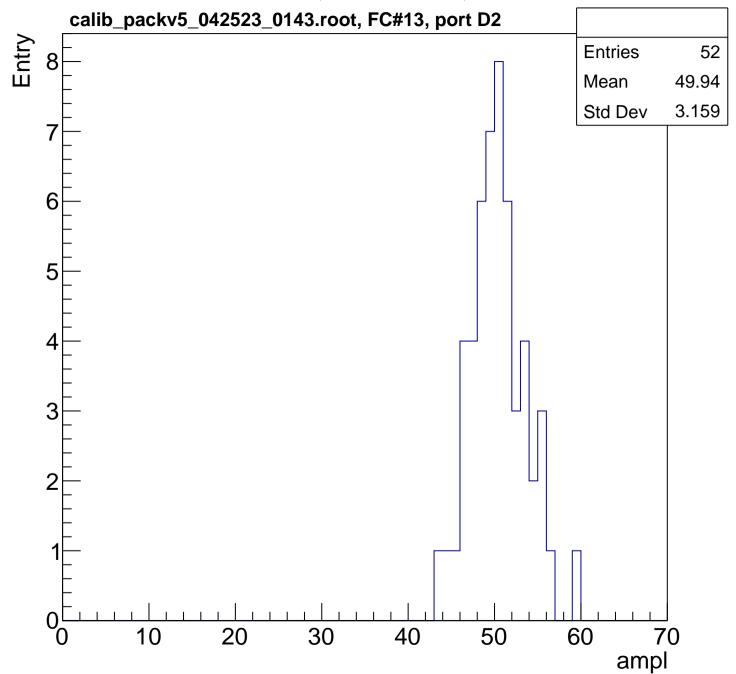


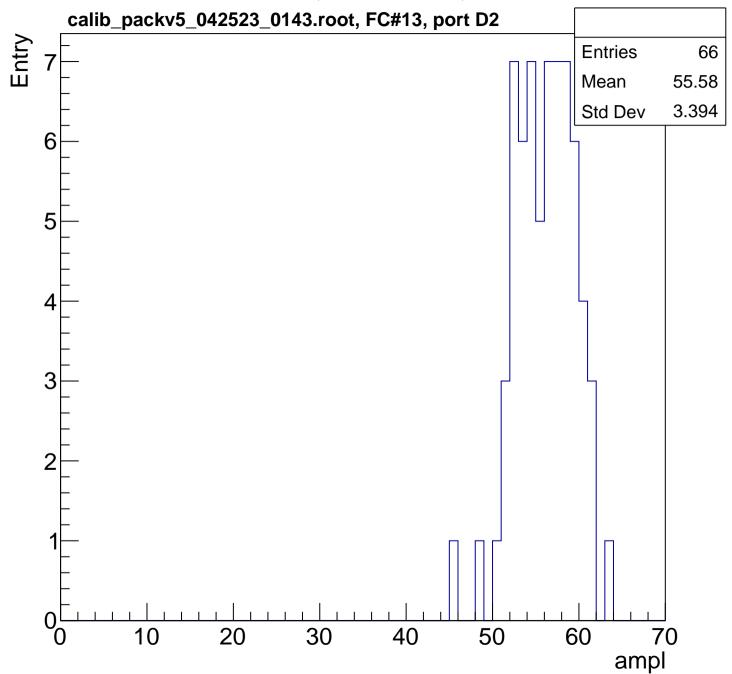


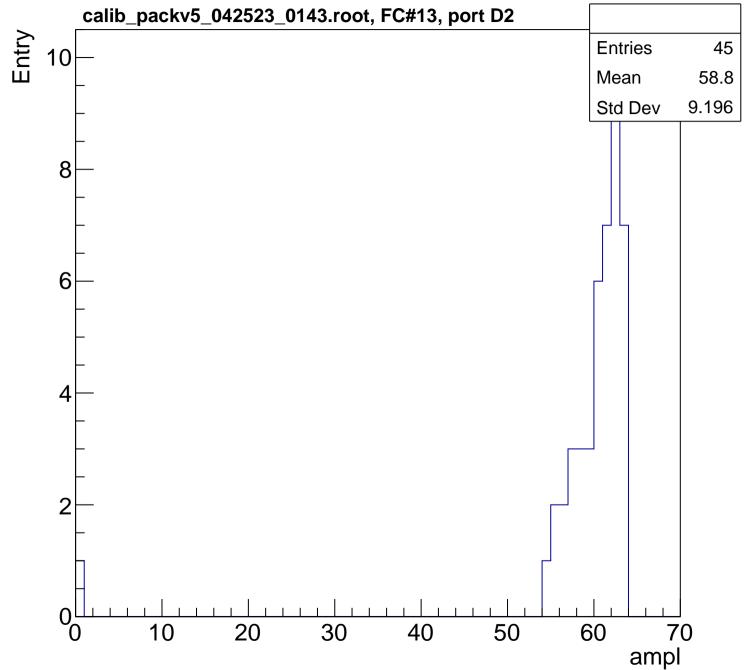


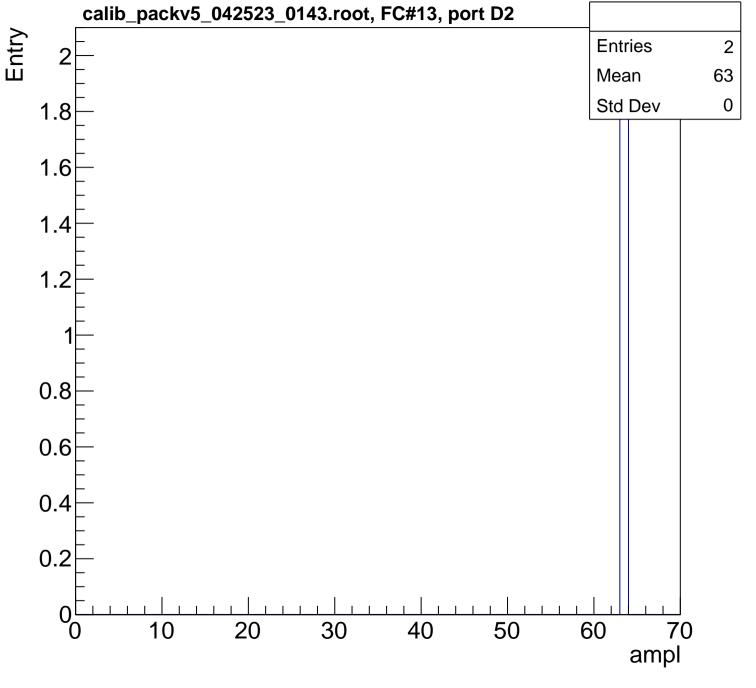




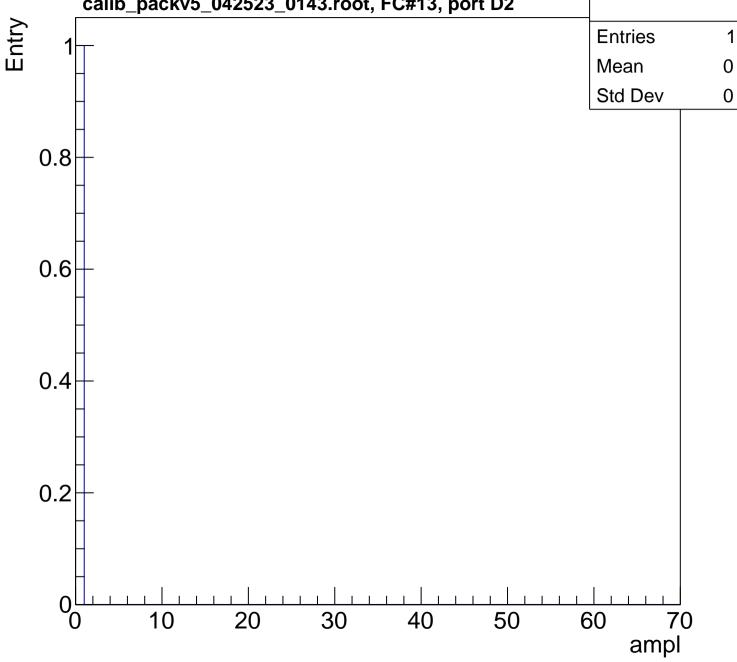


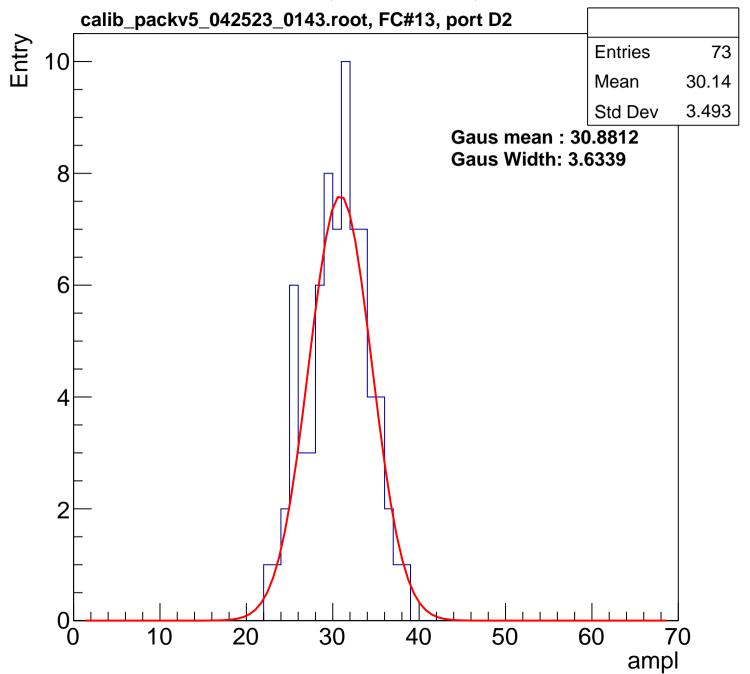


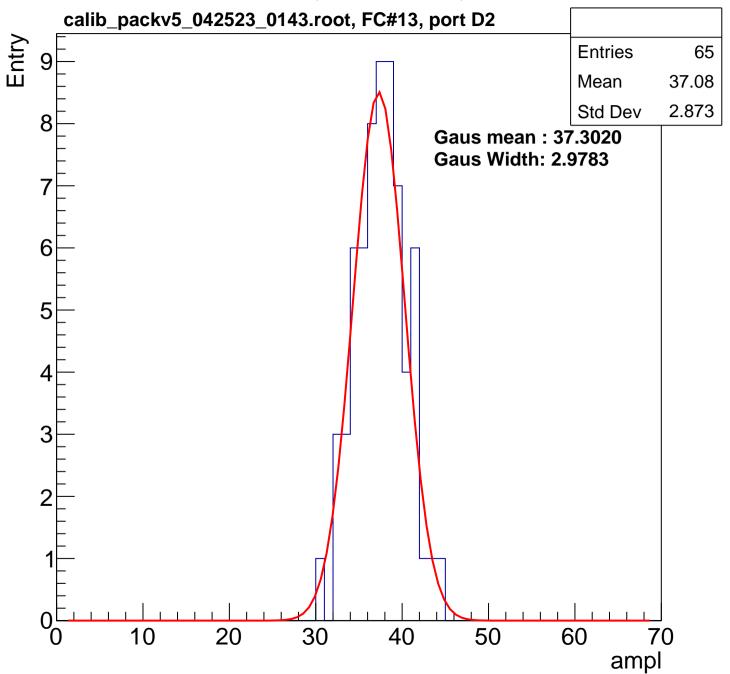


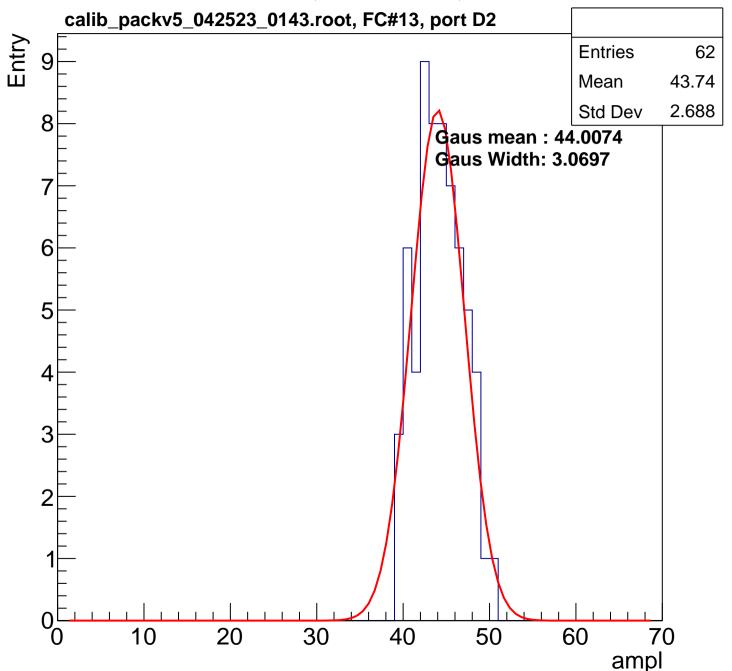


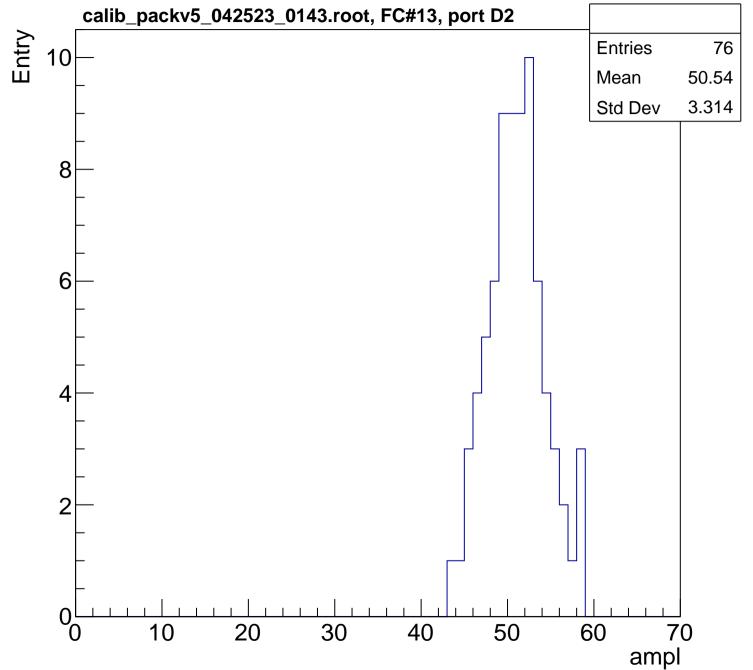
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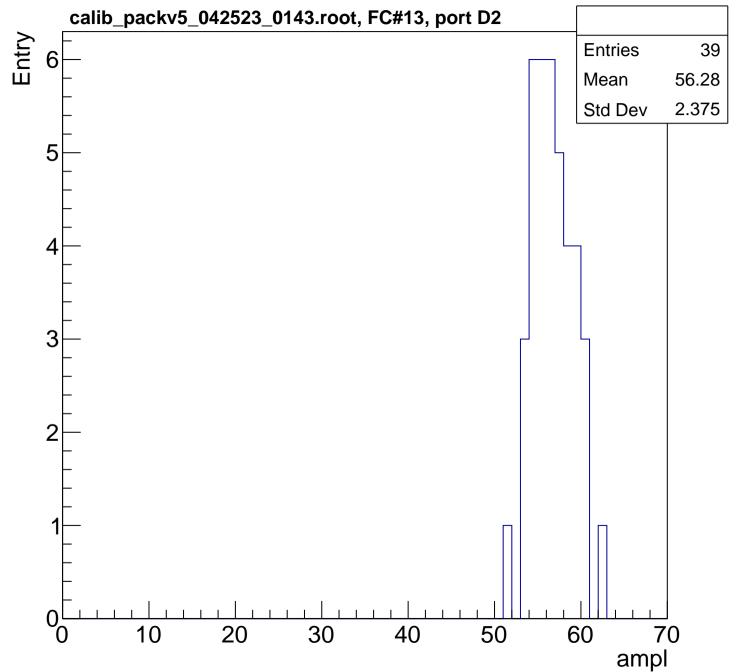


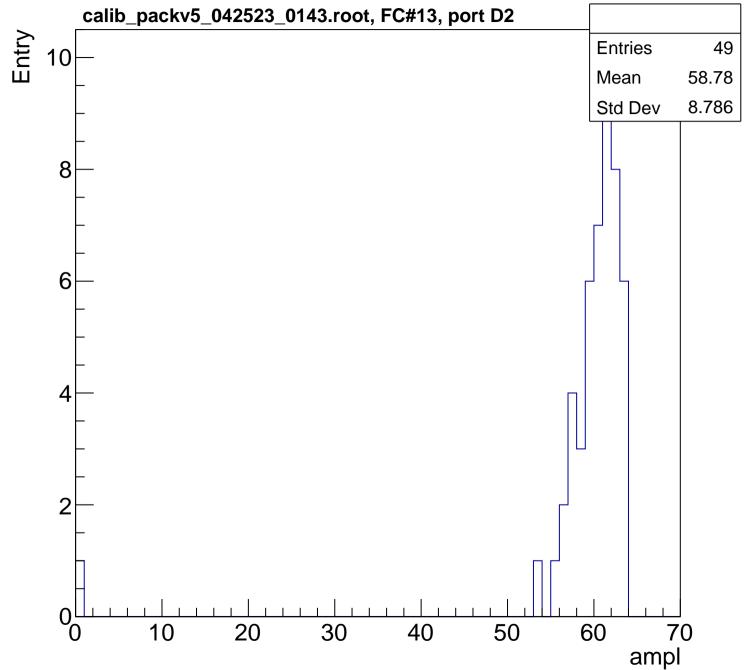


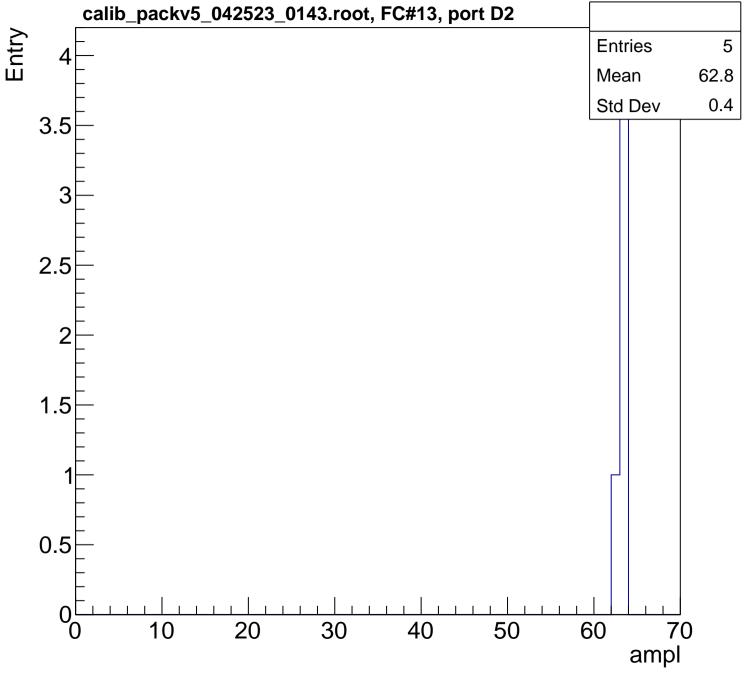


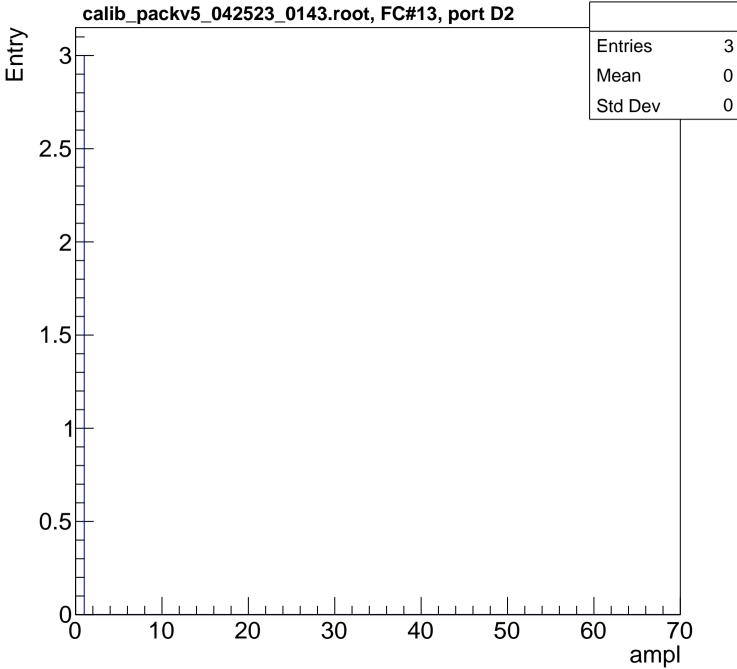


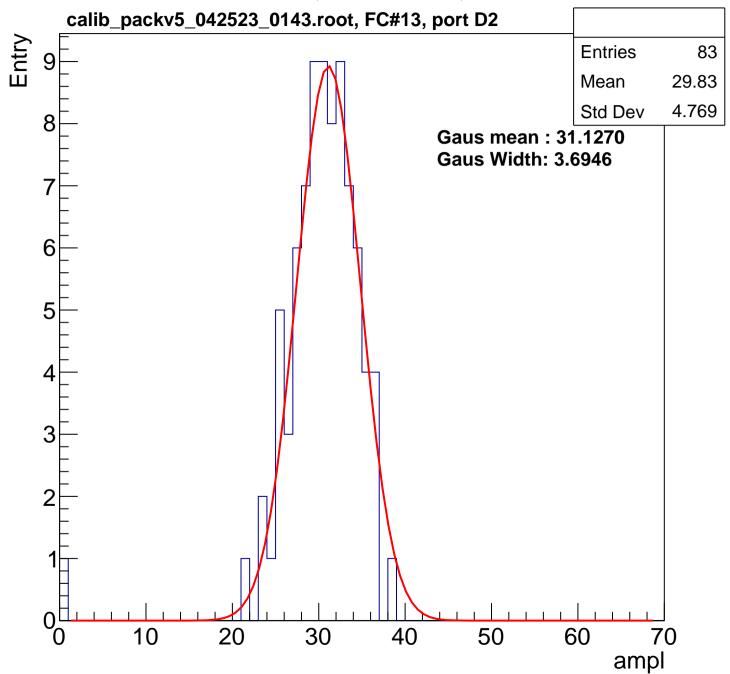


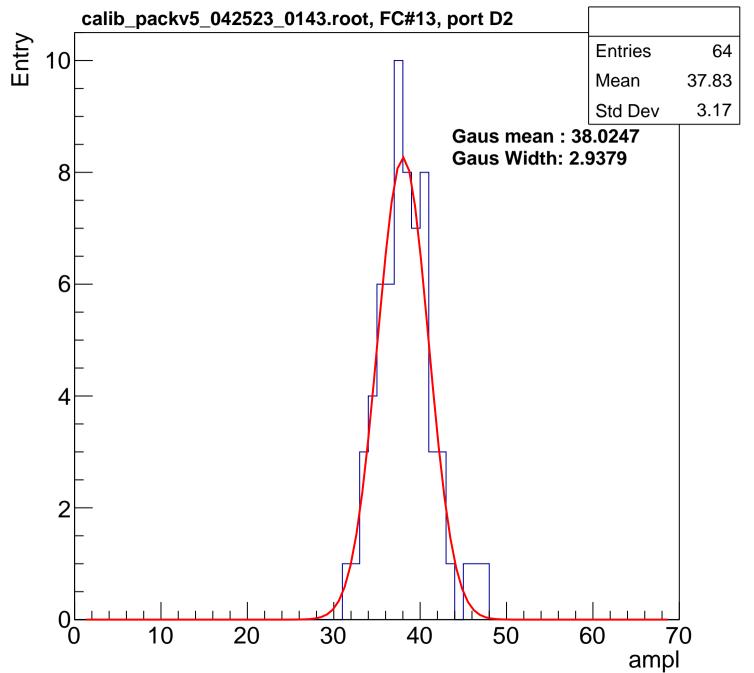


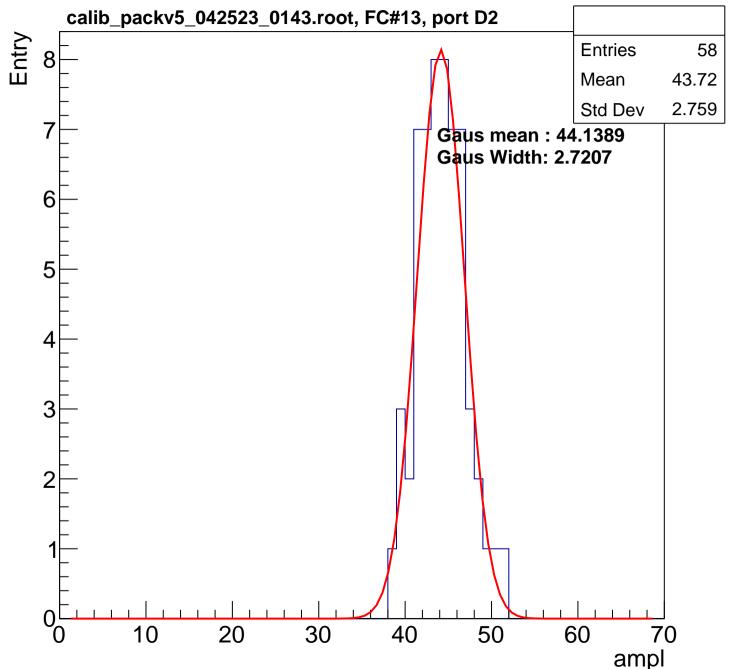


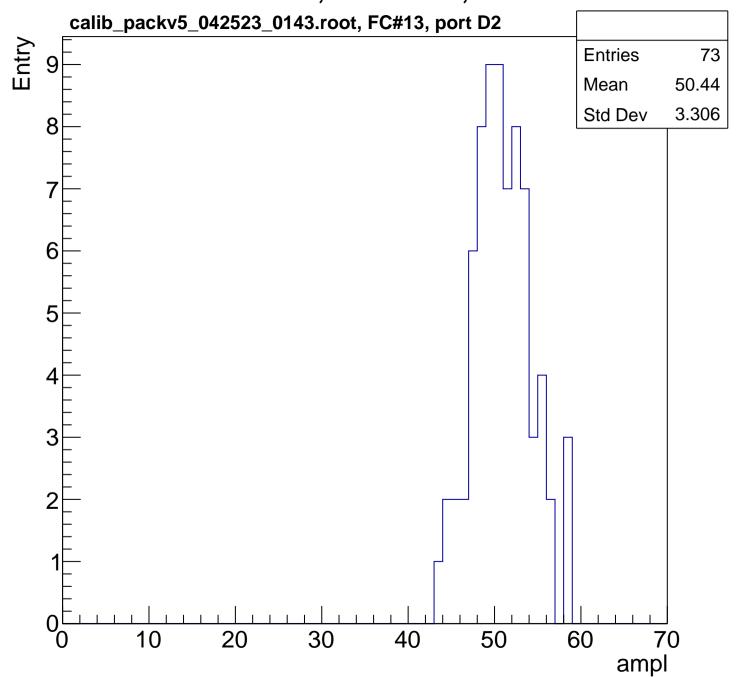


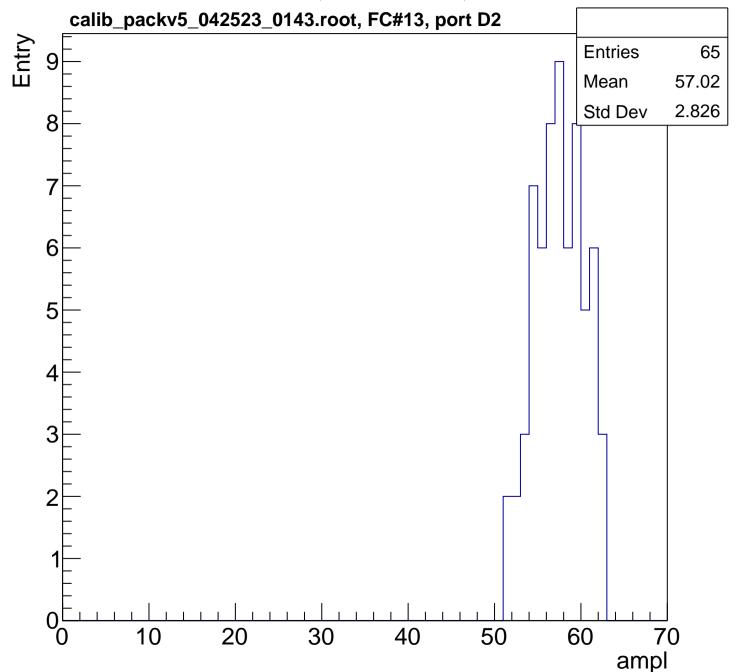


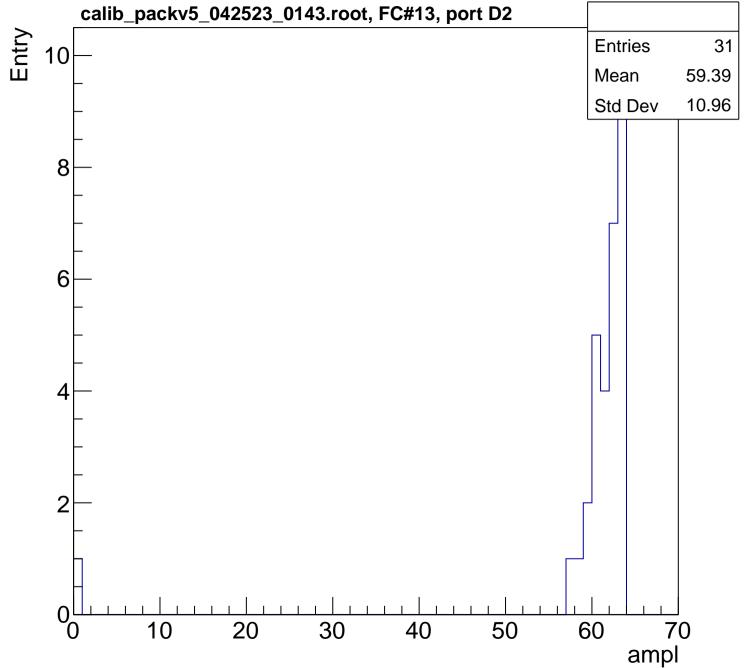


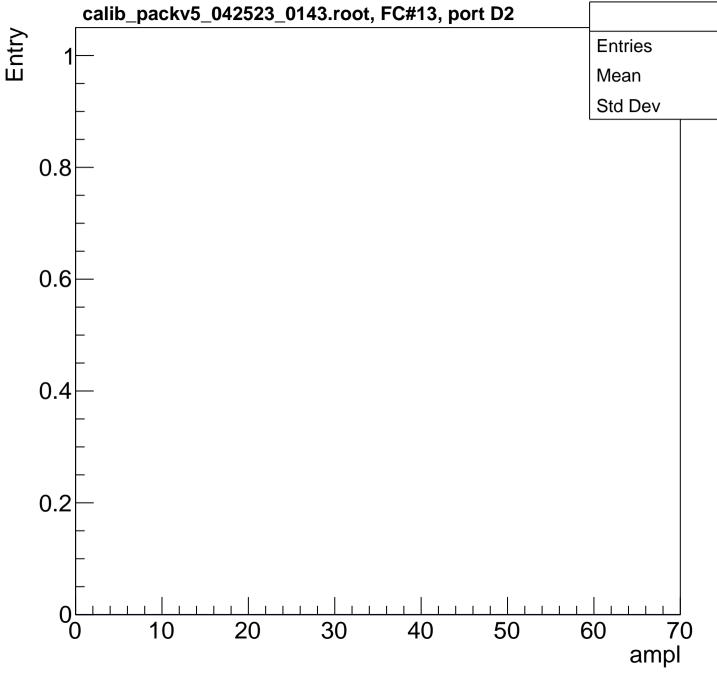




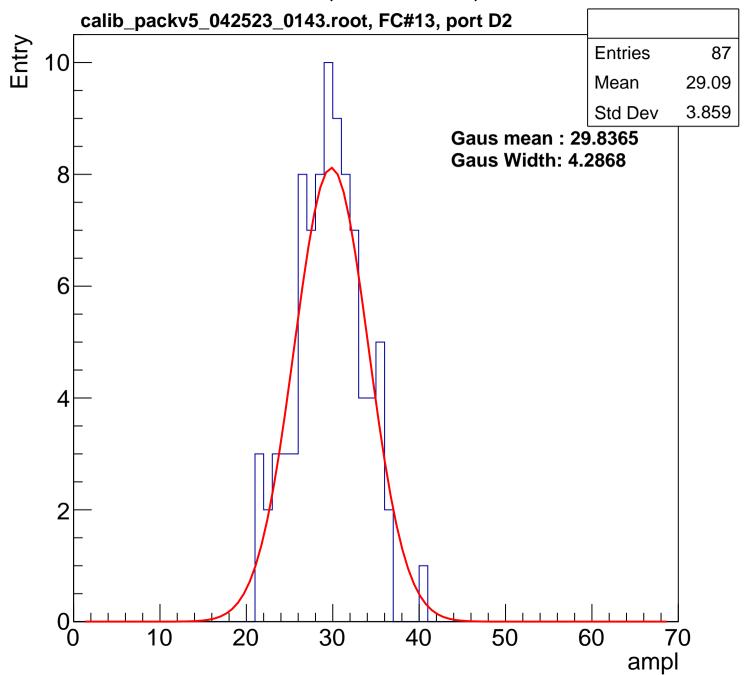


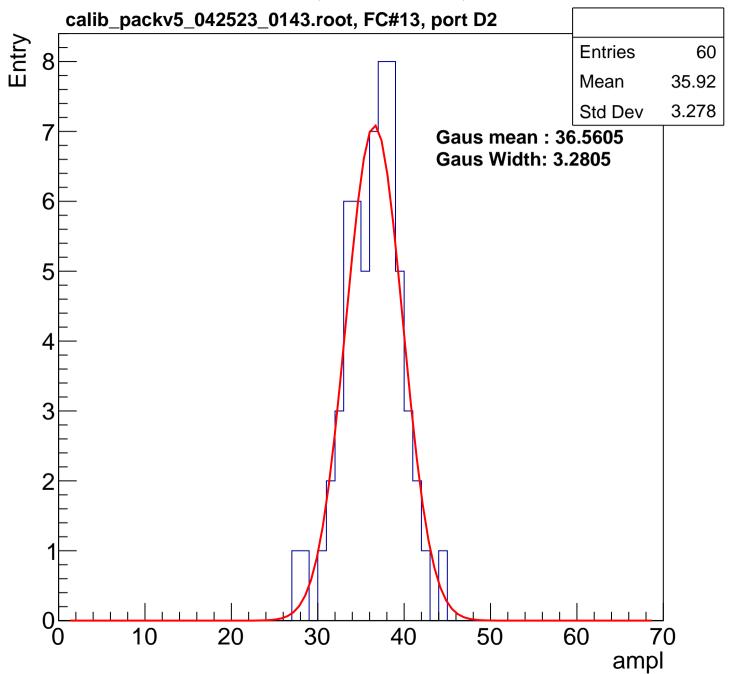


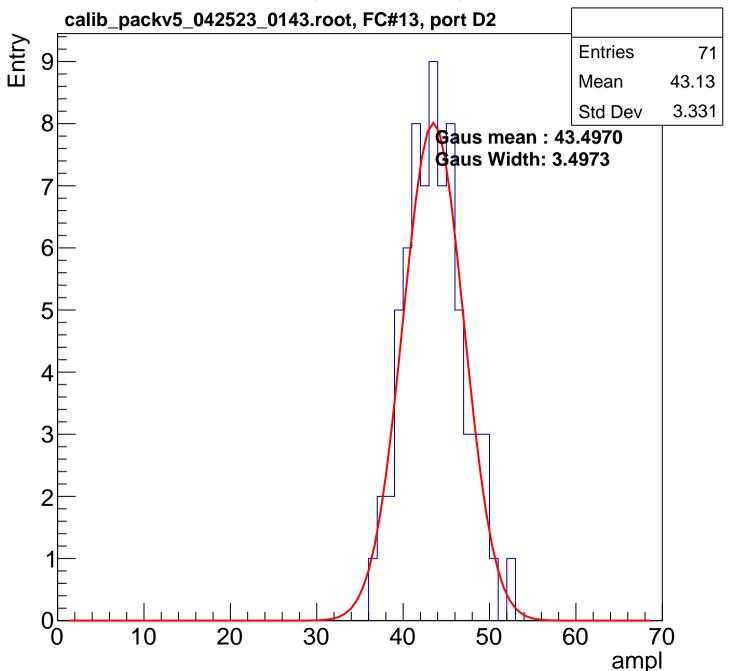


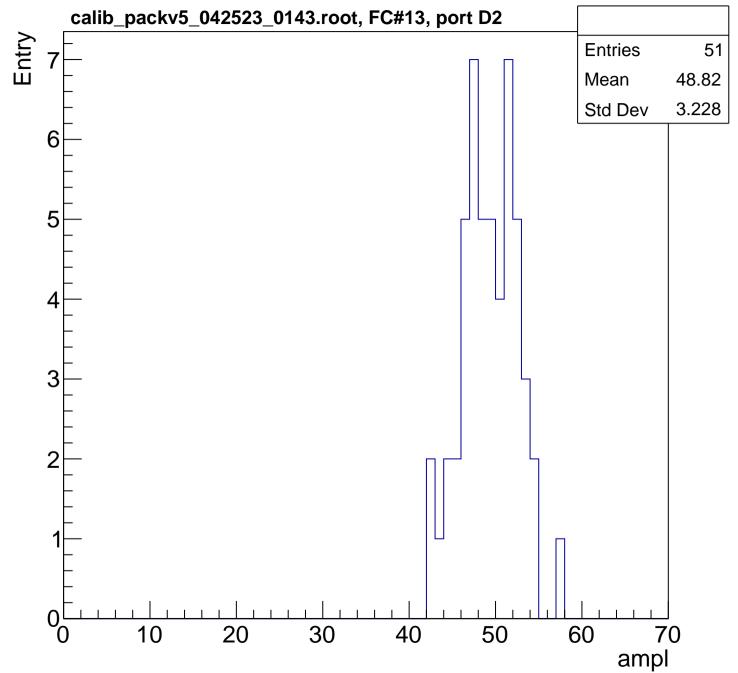


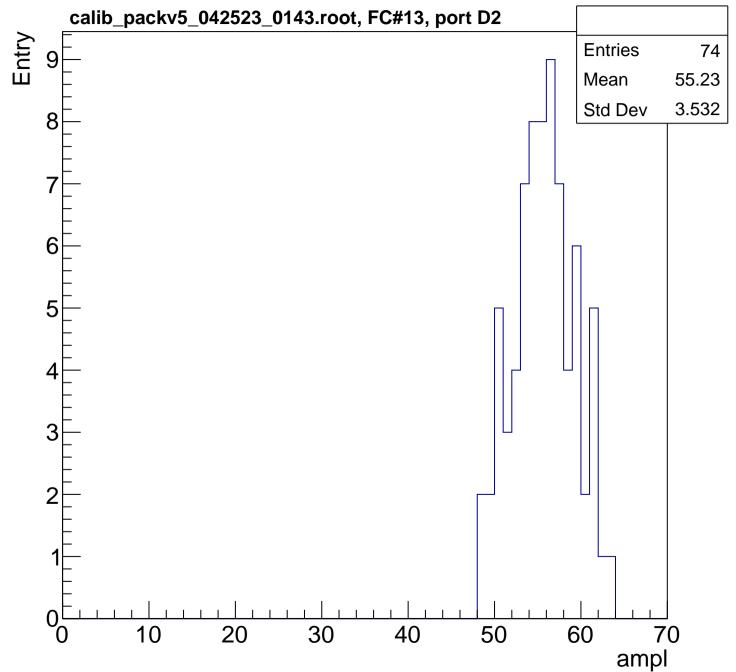


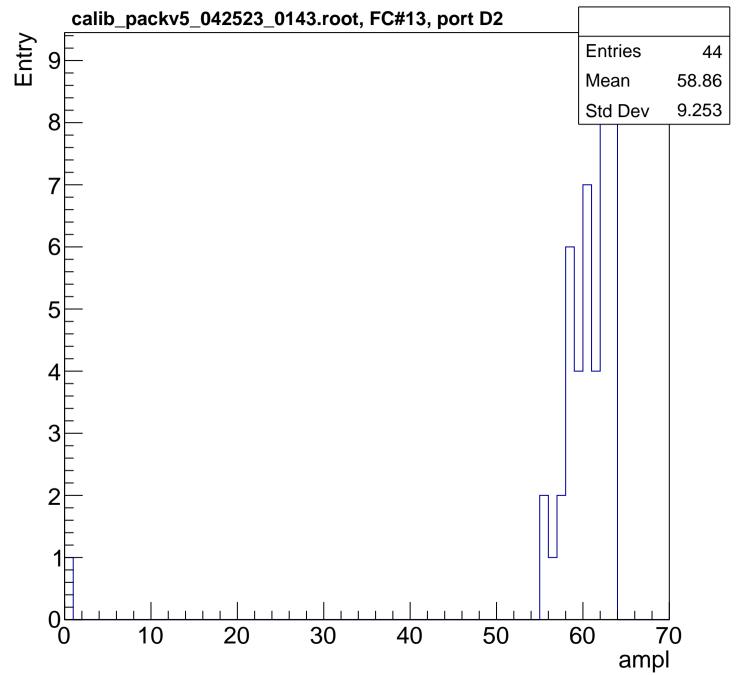


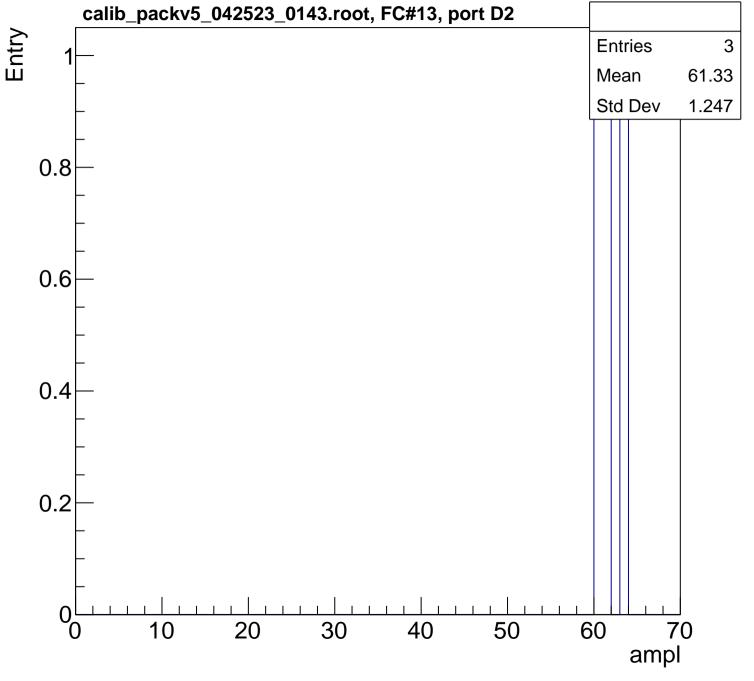


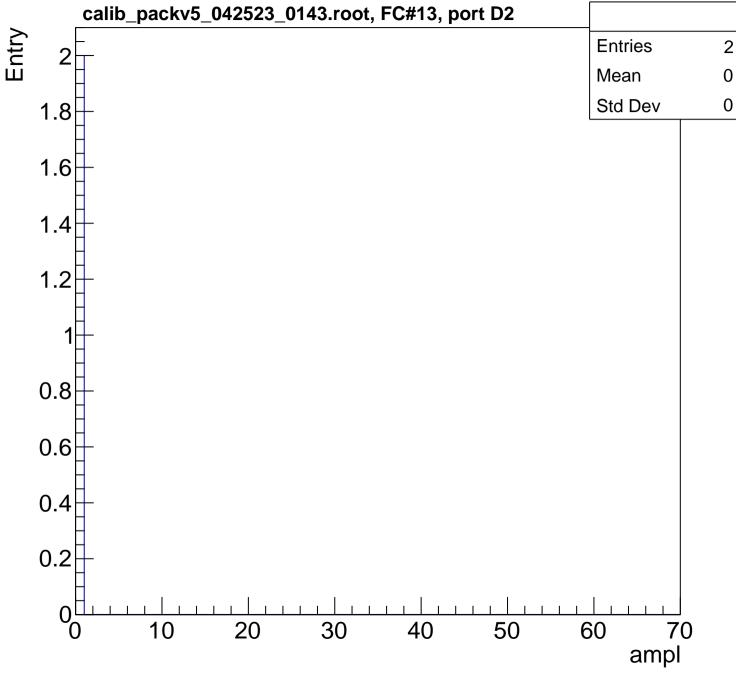


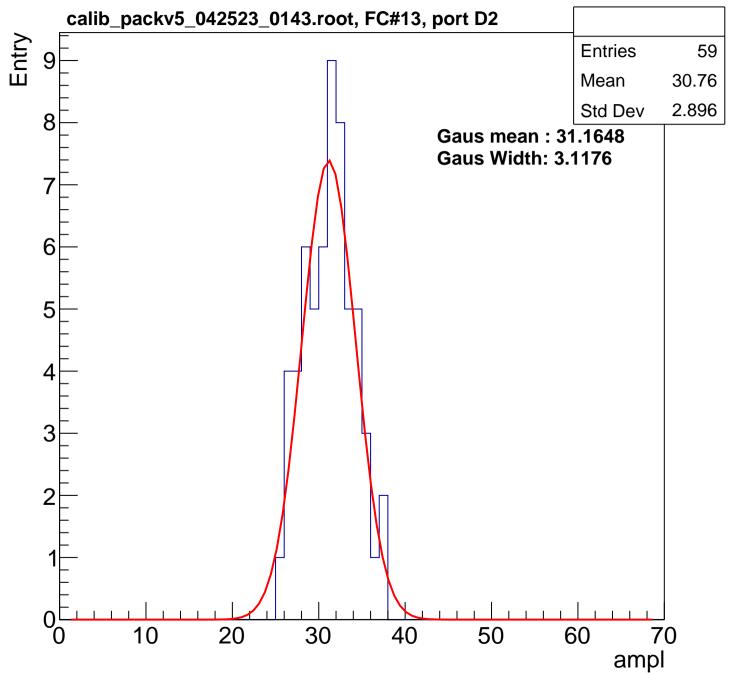


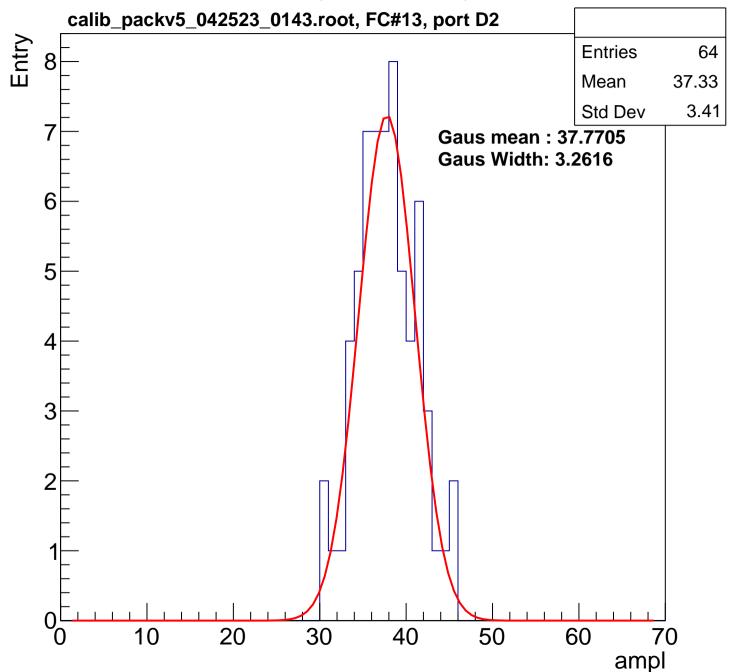


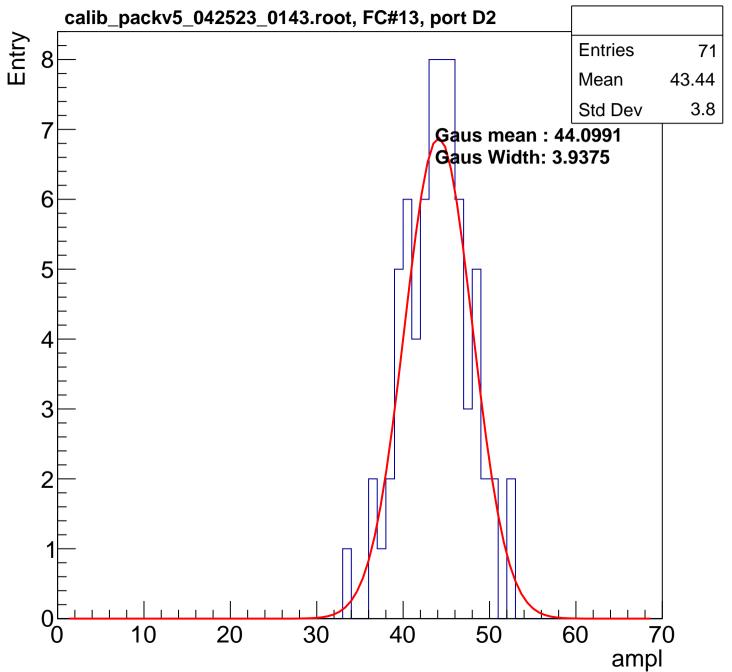


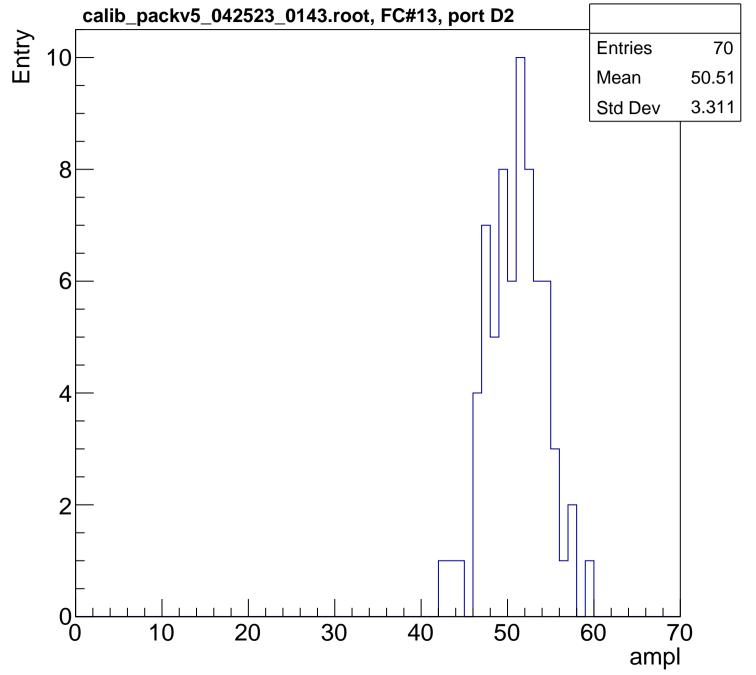


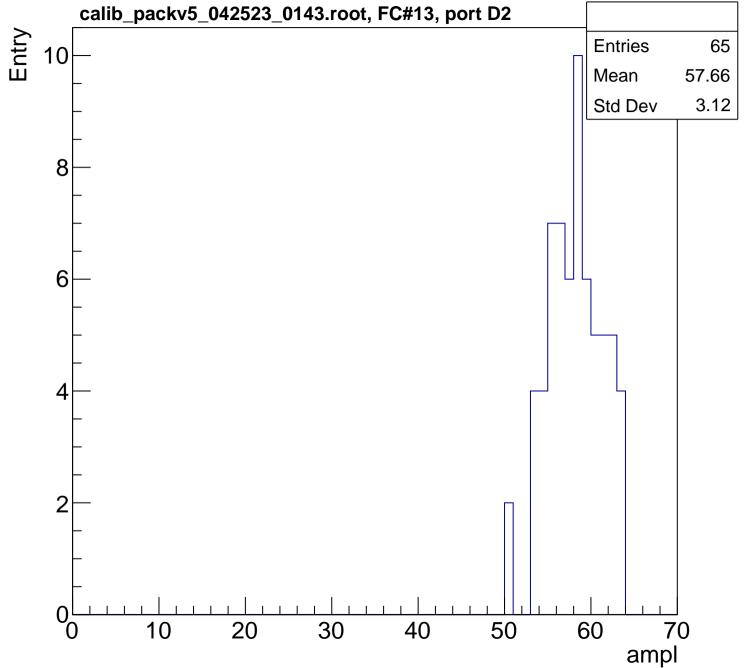


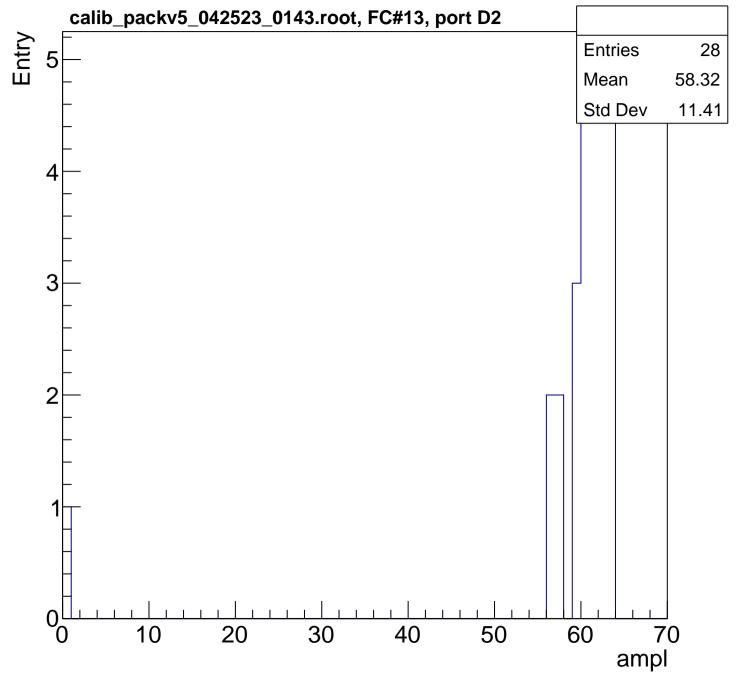


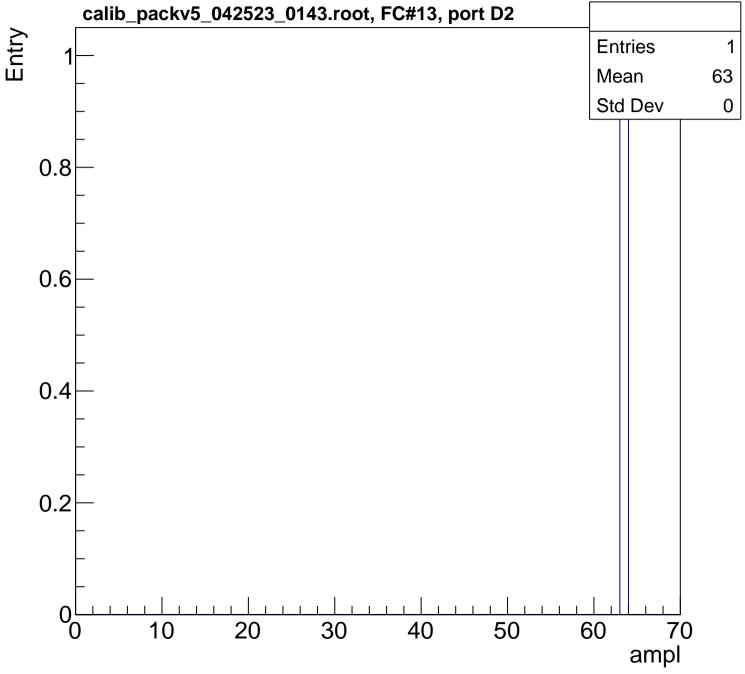


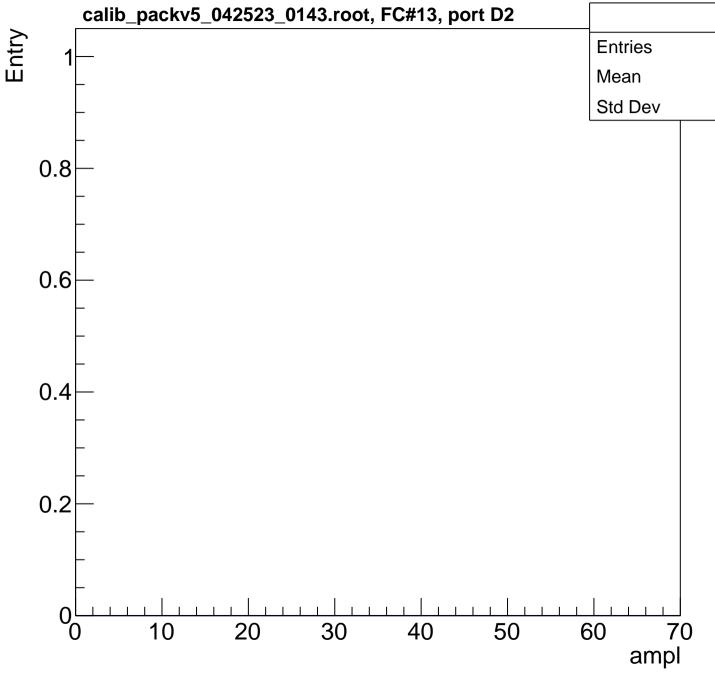


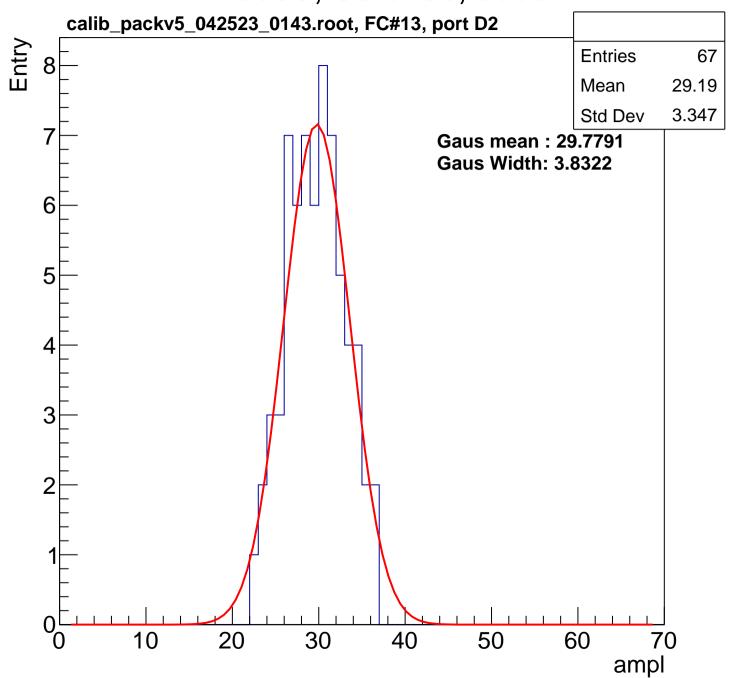


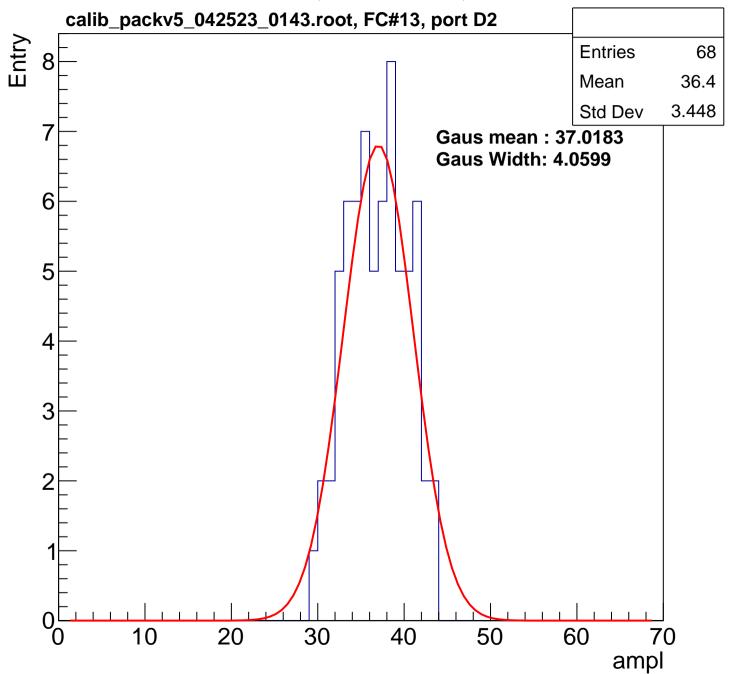


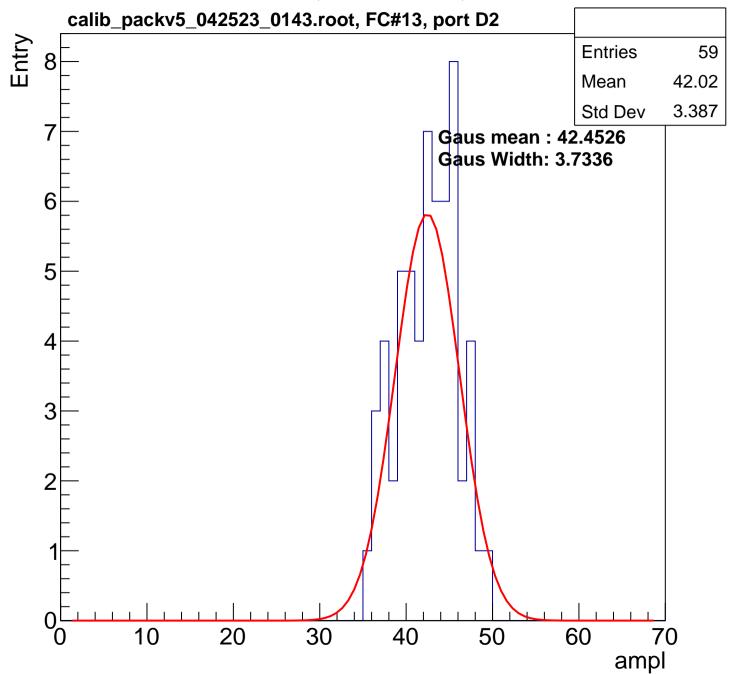


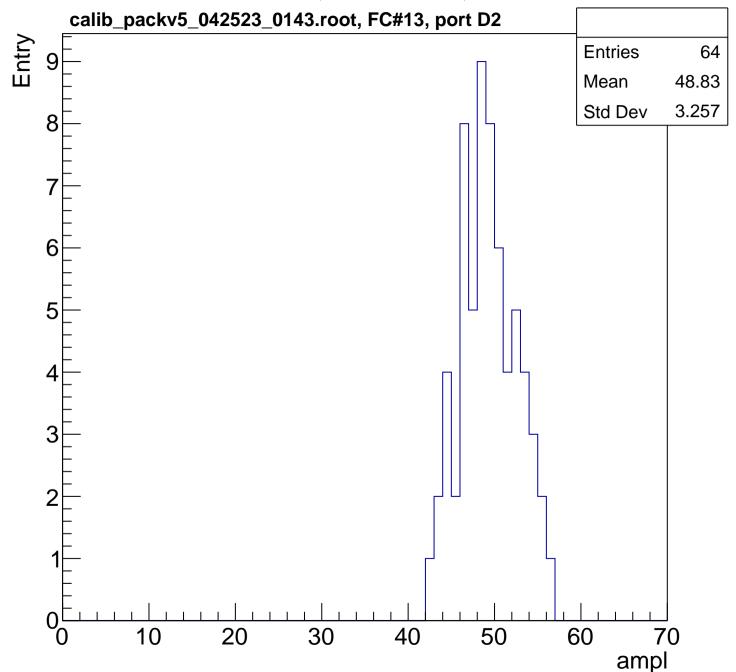


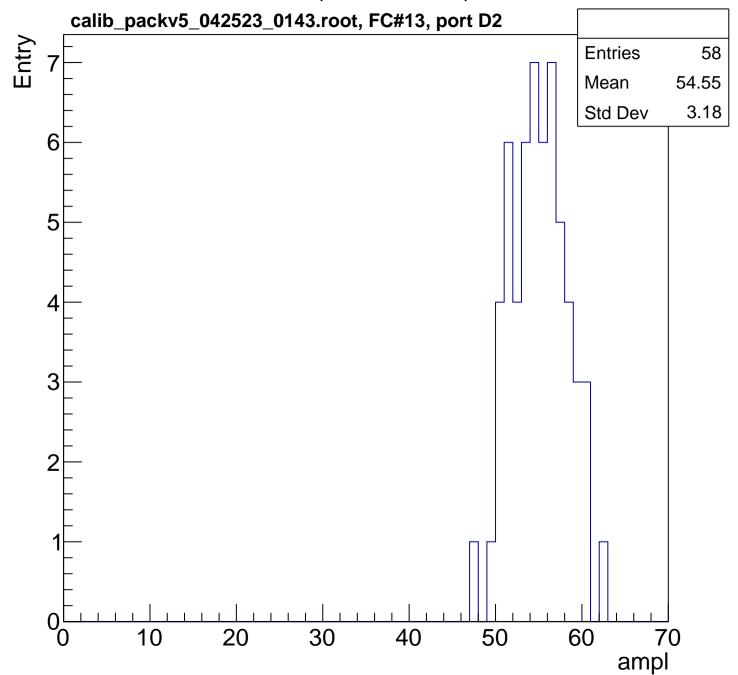


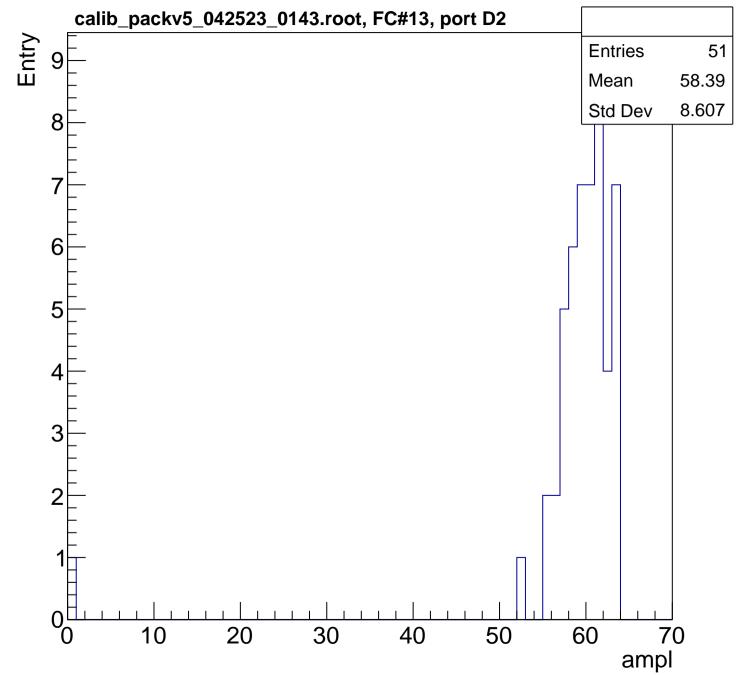


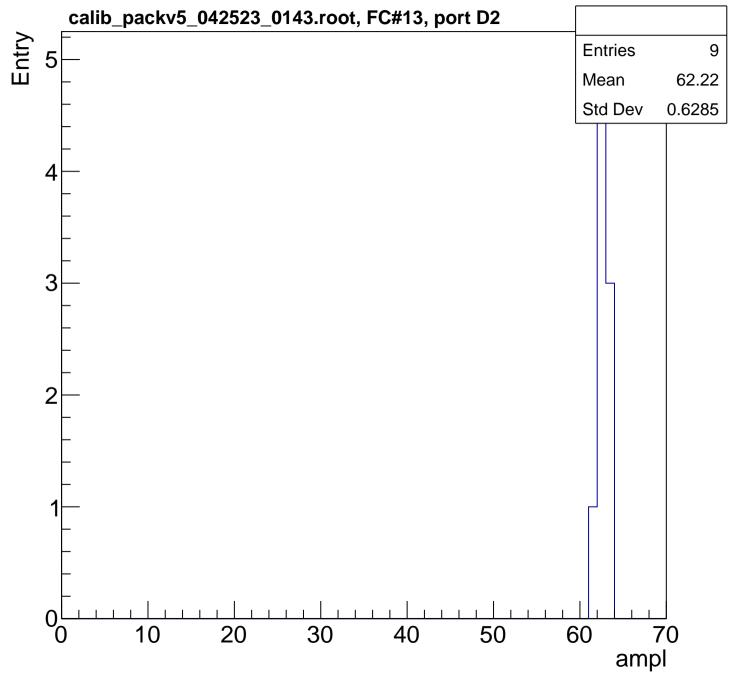




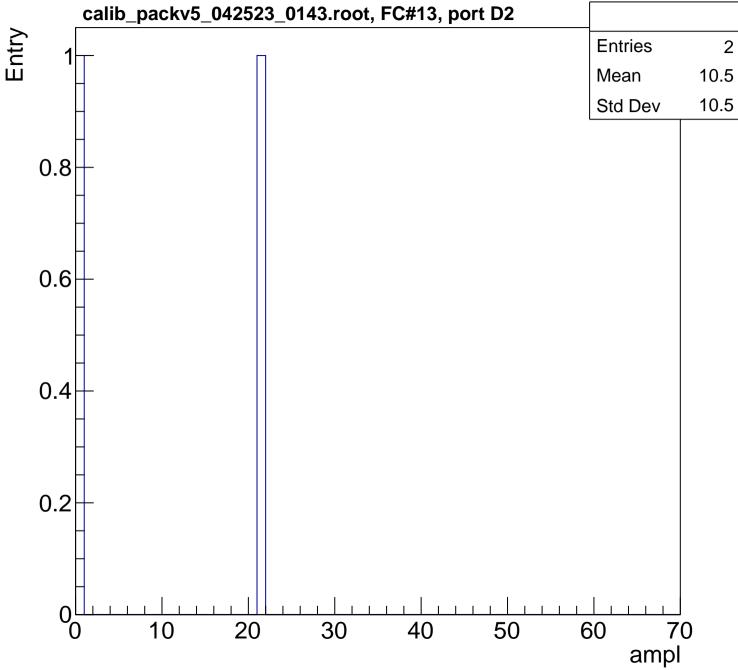


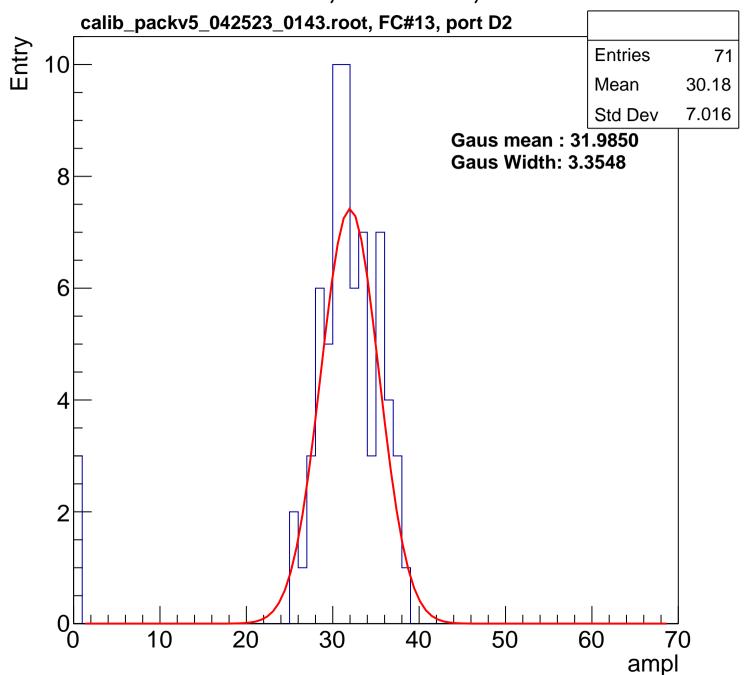


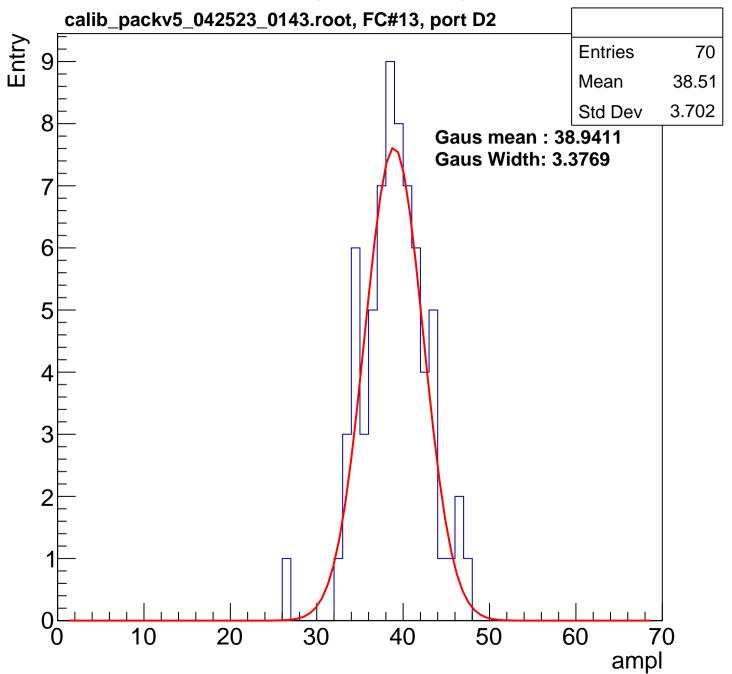


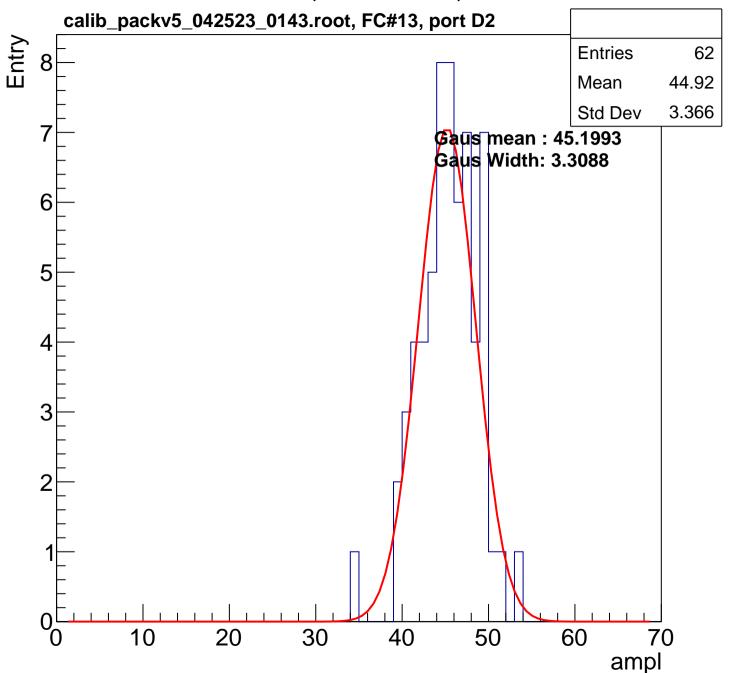


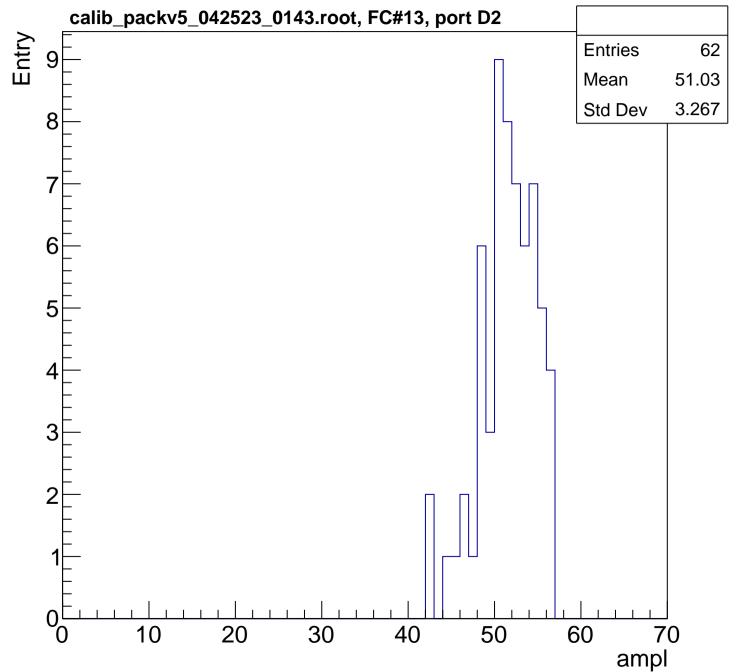
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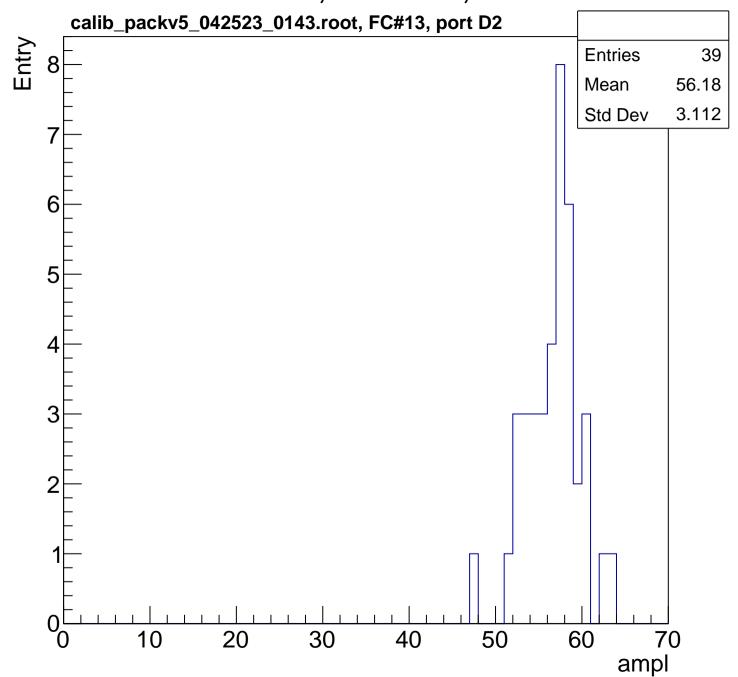


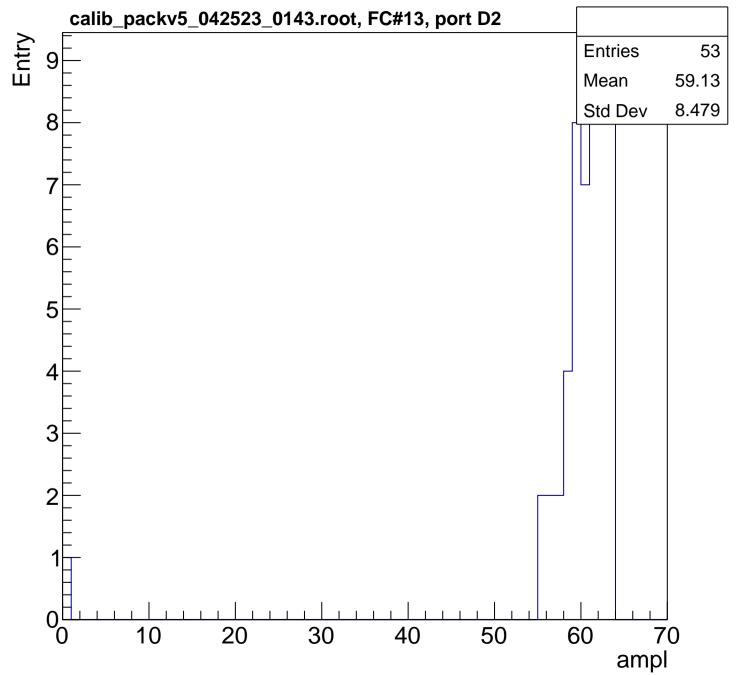


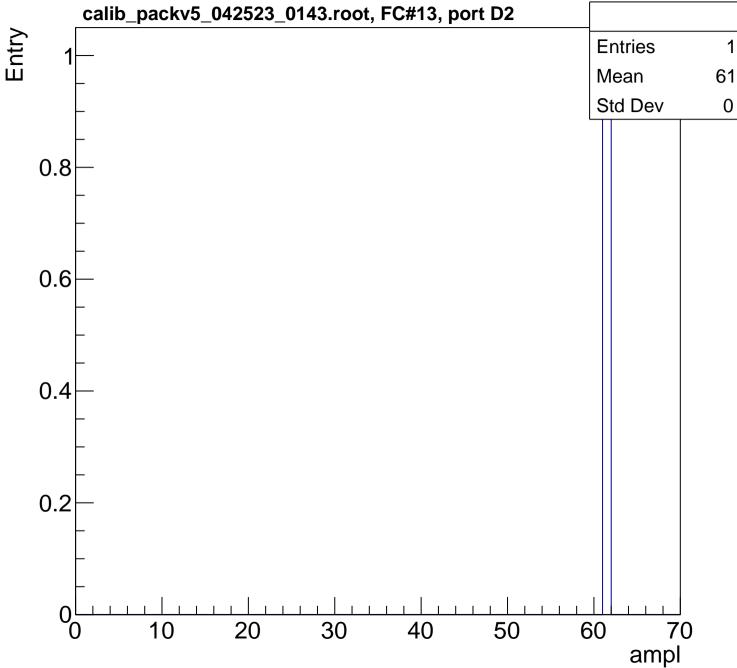




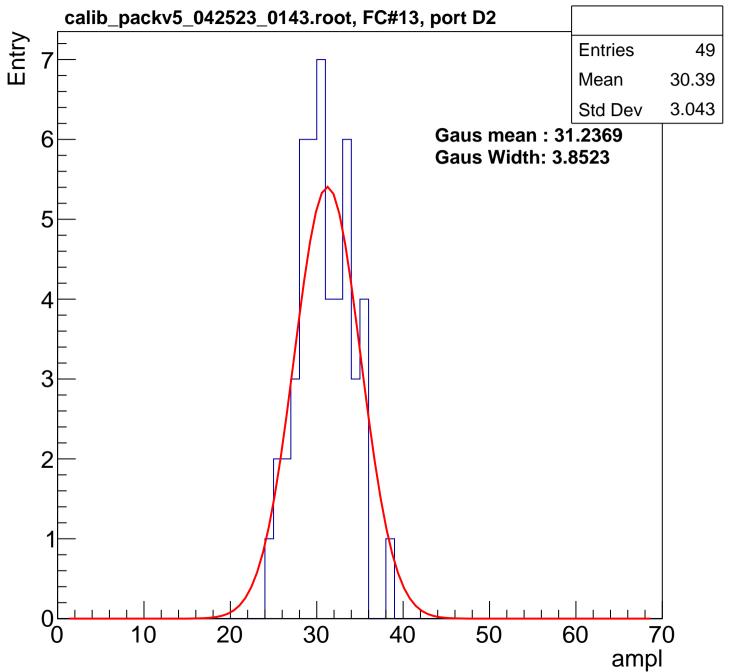


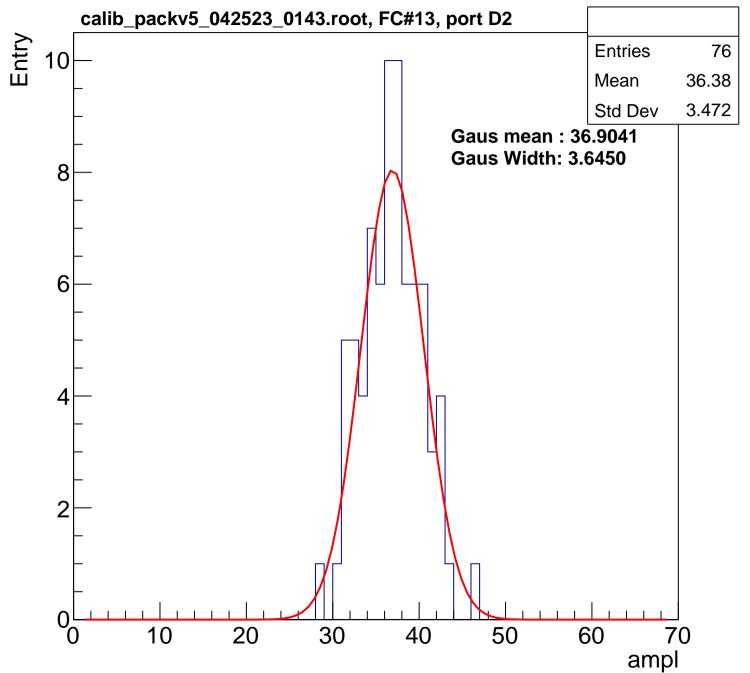


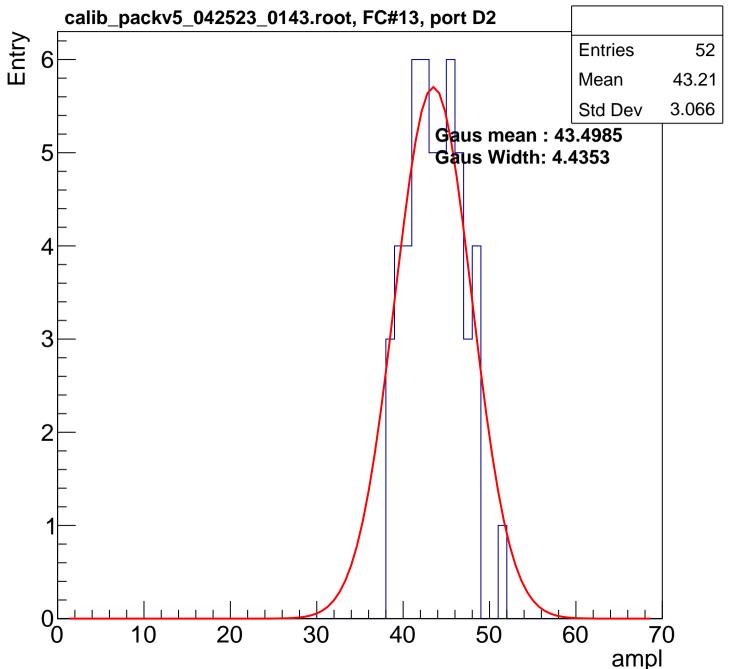


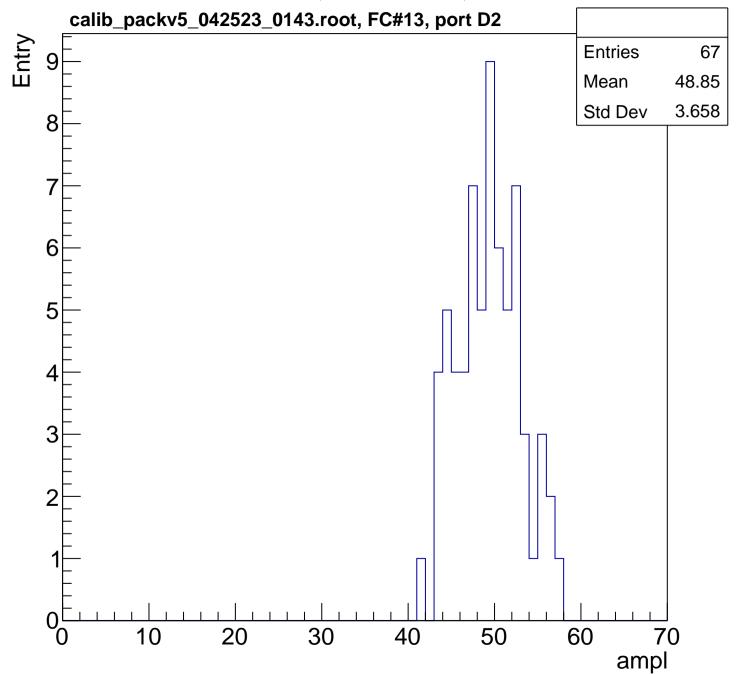


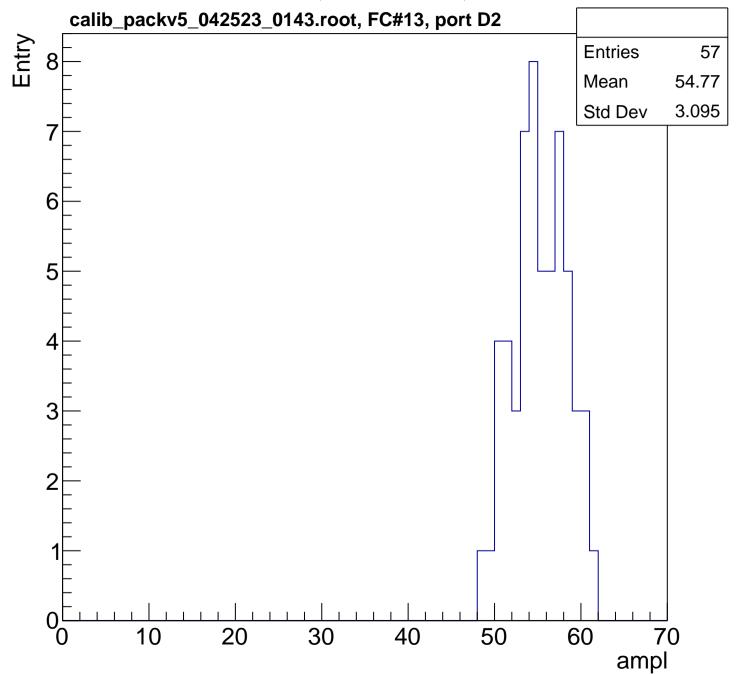
B1L003S, U9-ch57, adc7 calib\_packv5\_042523\_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

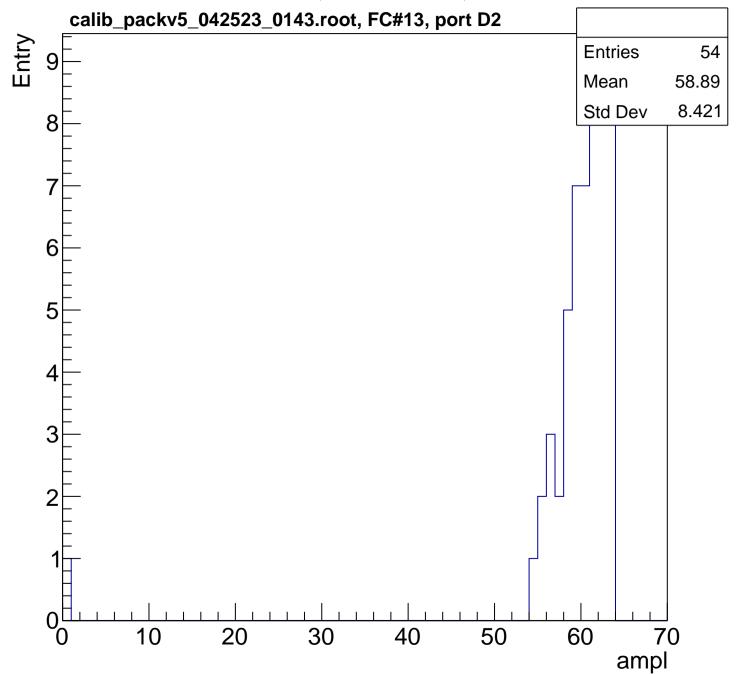


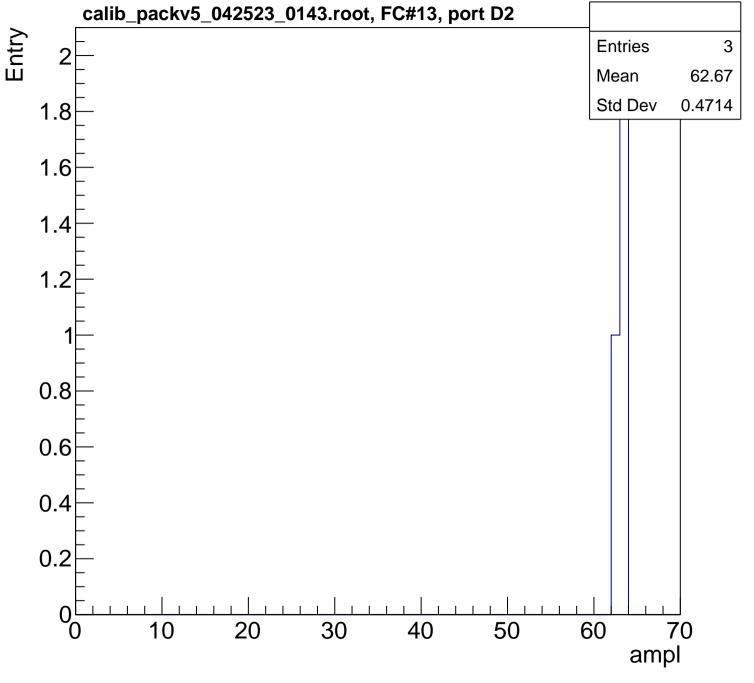


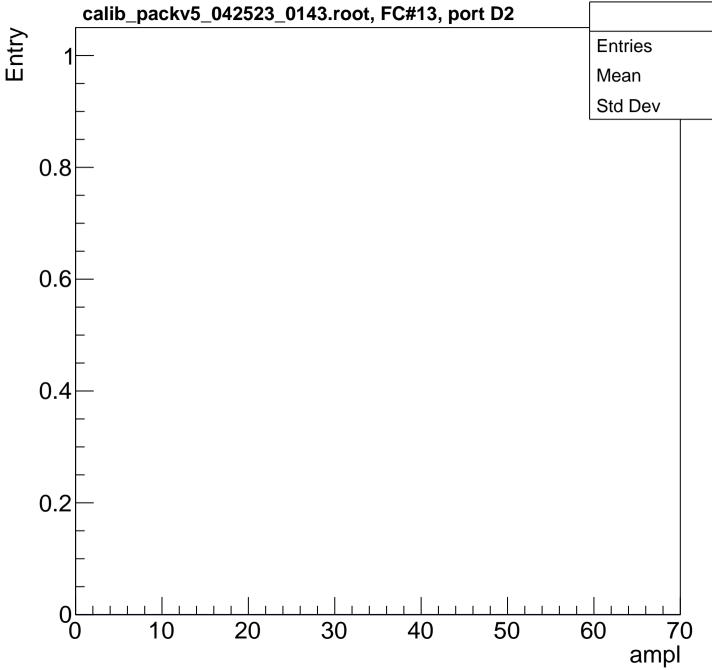


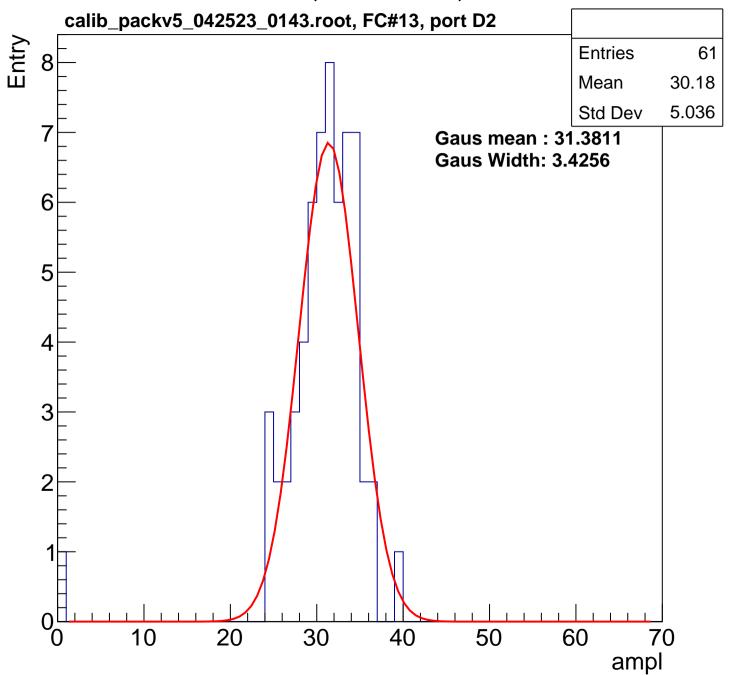


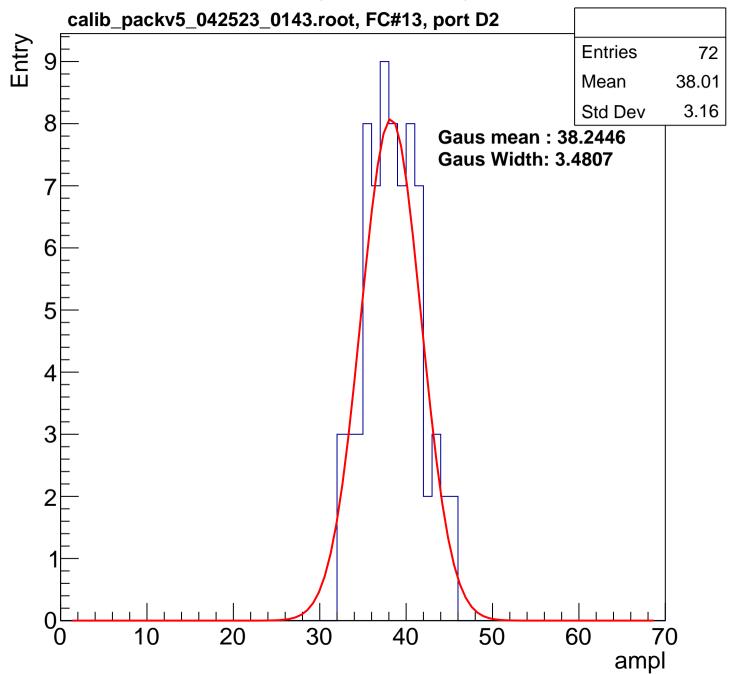


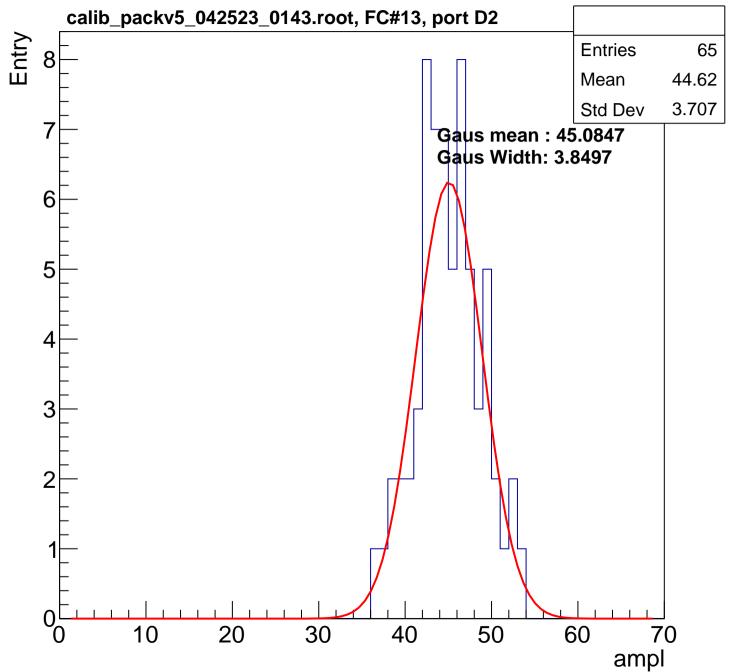


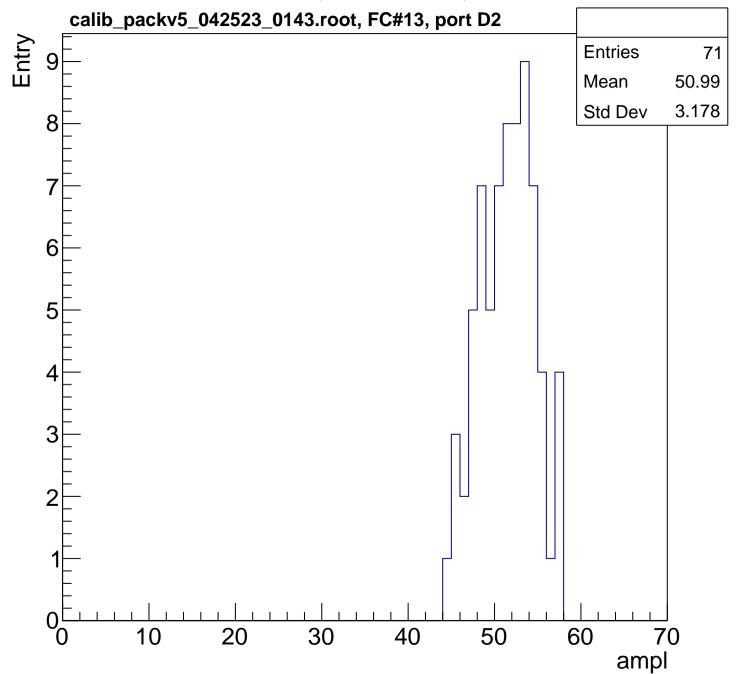


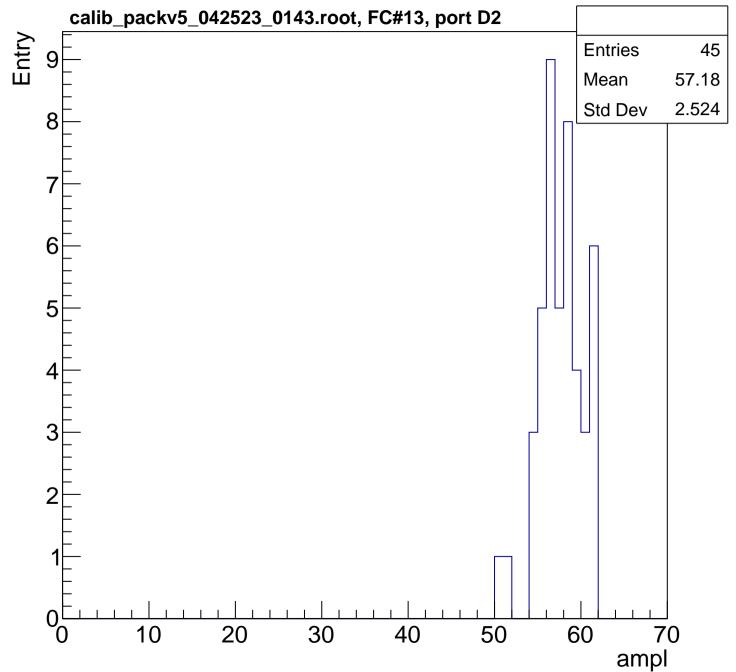


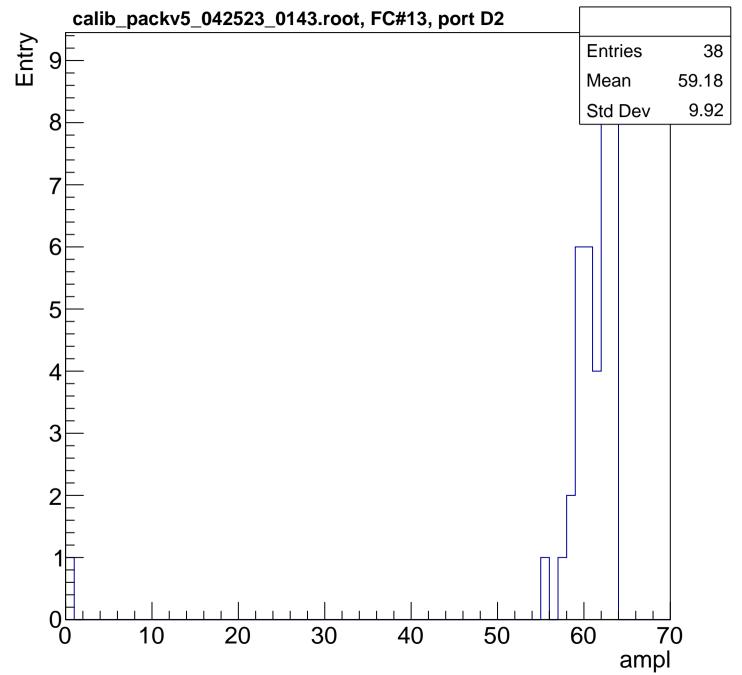


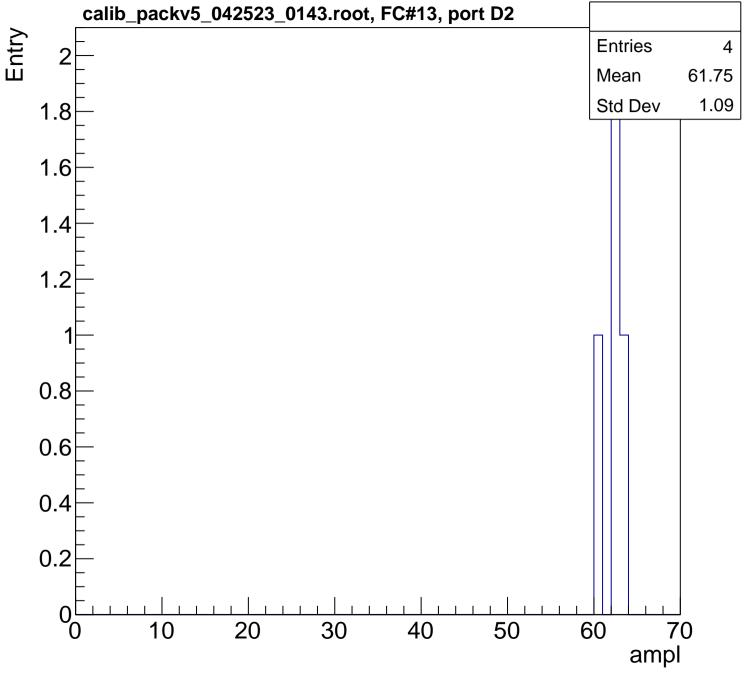




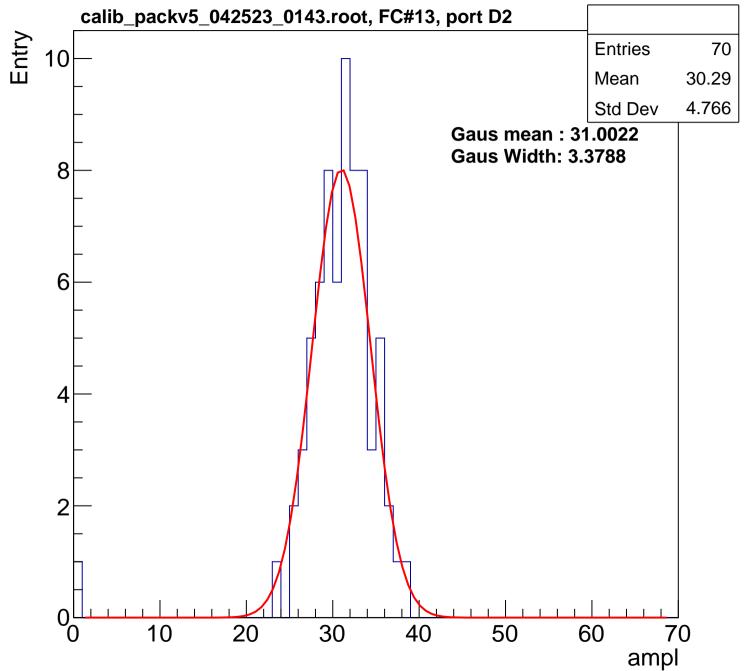


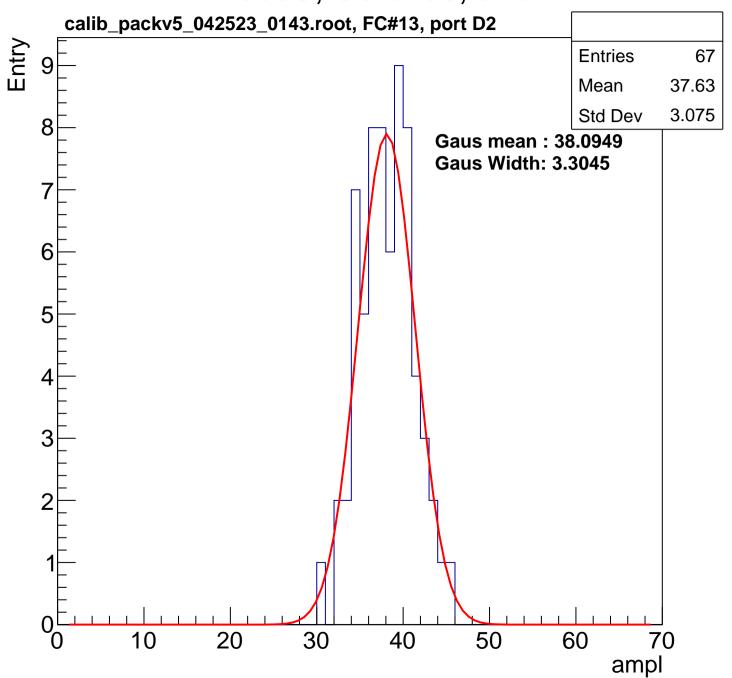


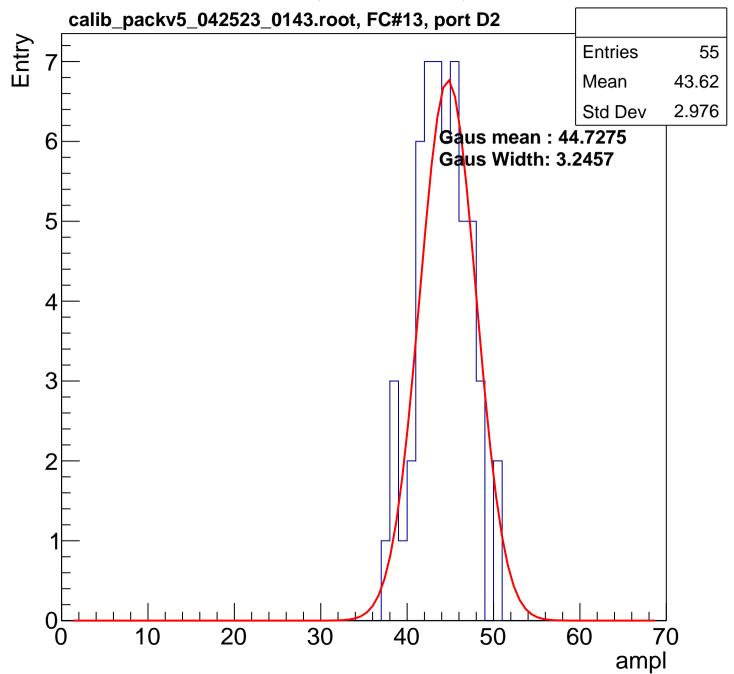


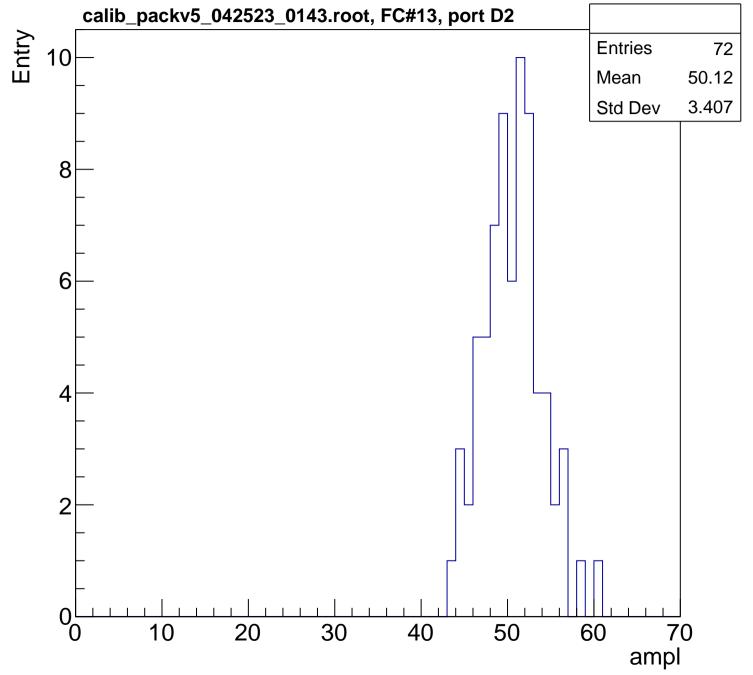


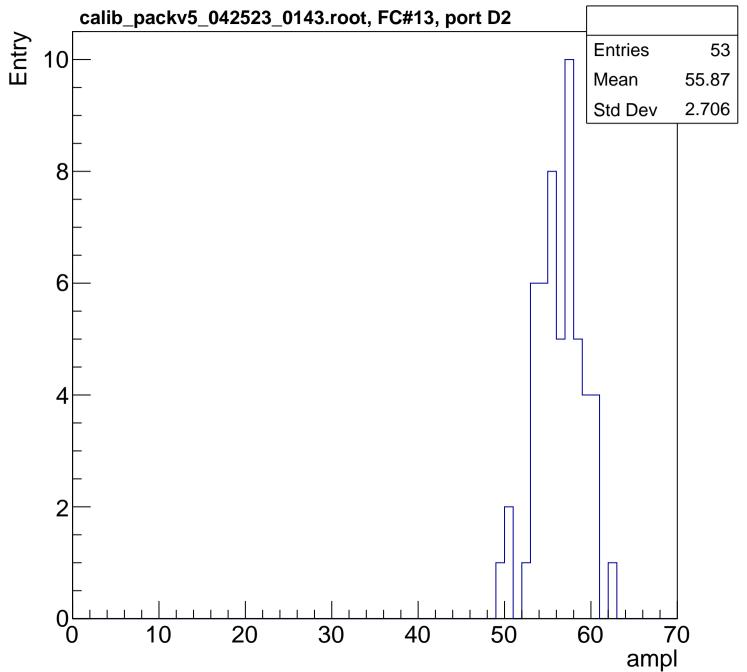


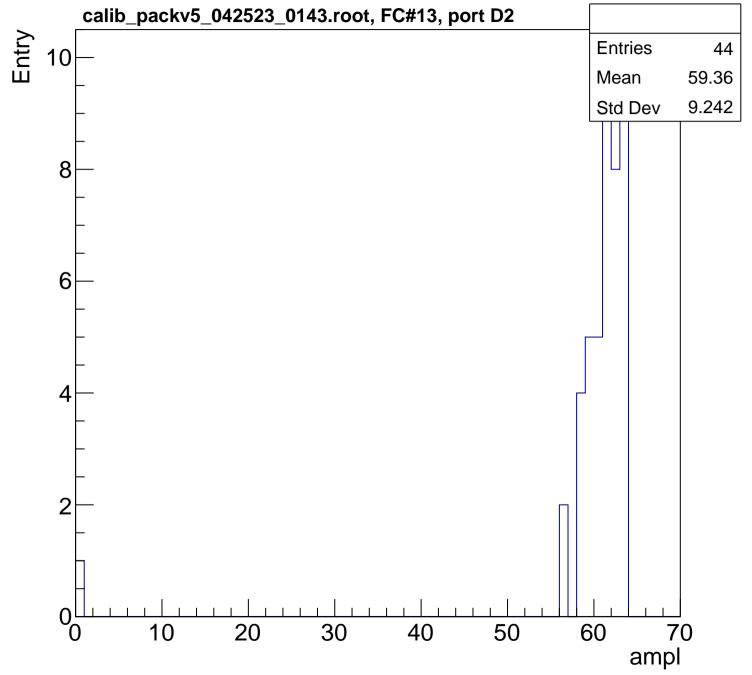


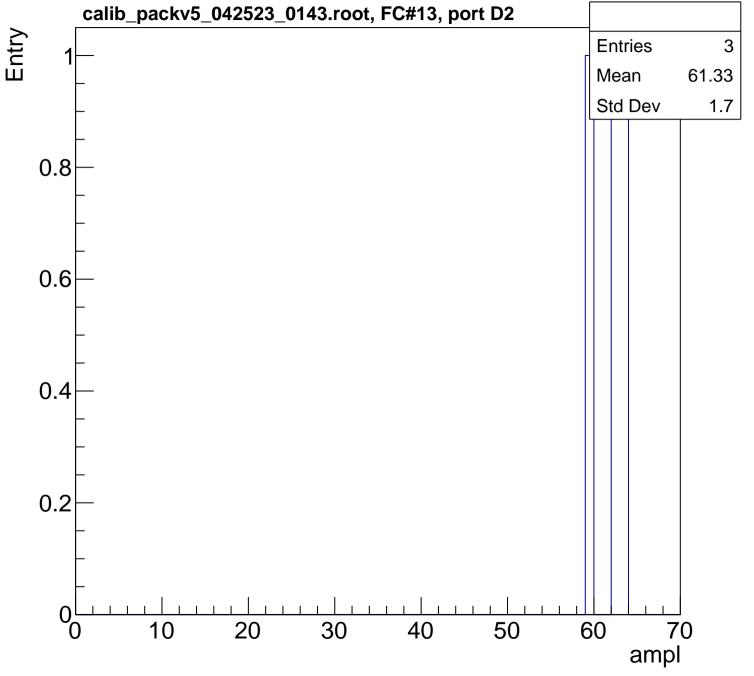




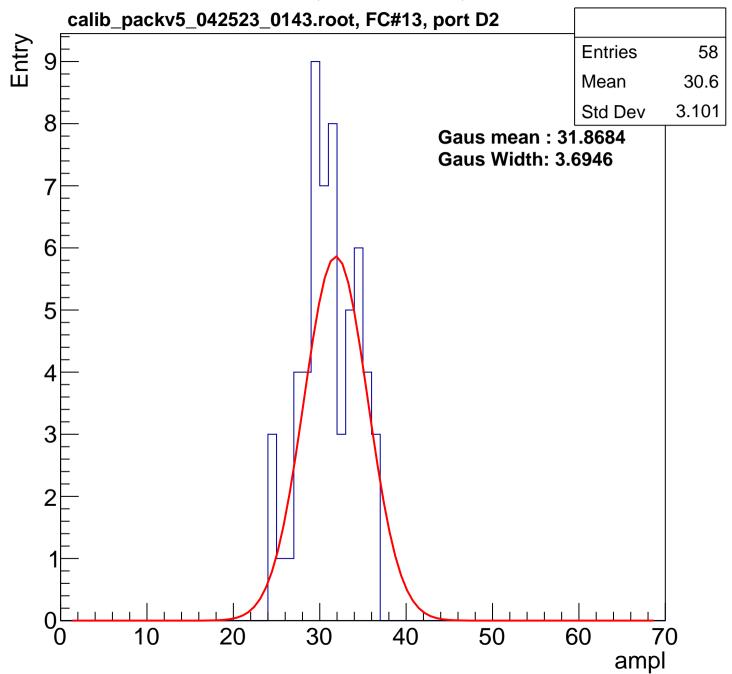


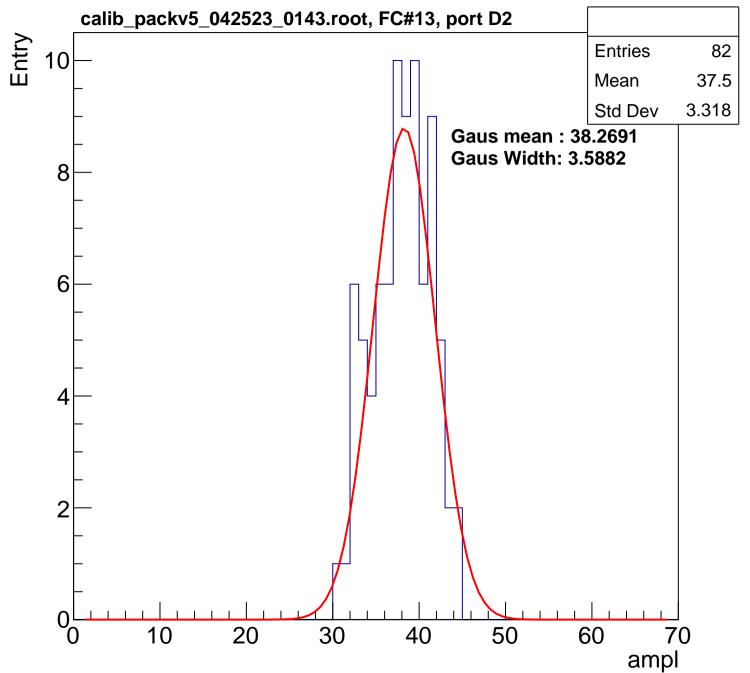


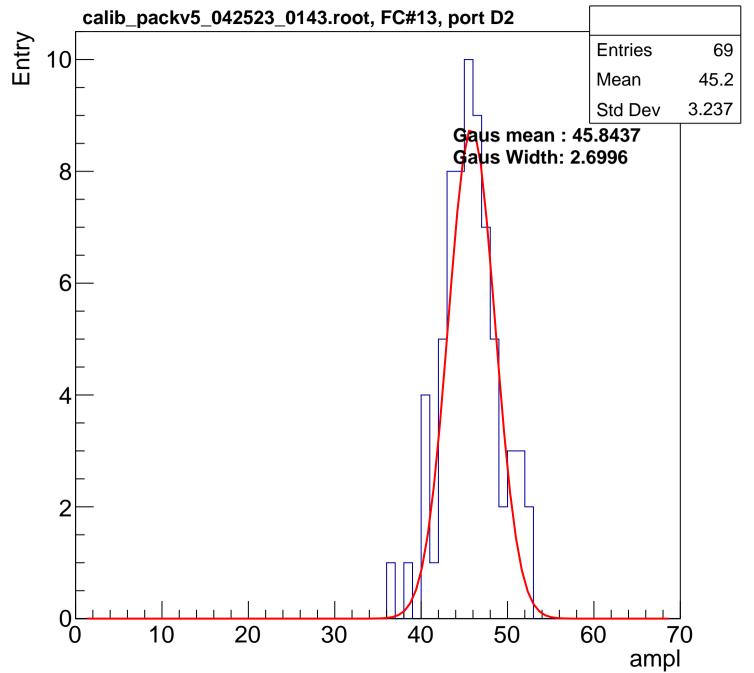


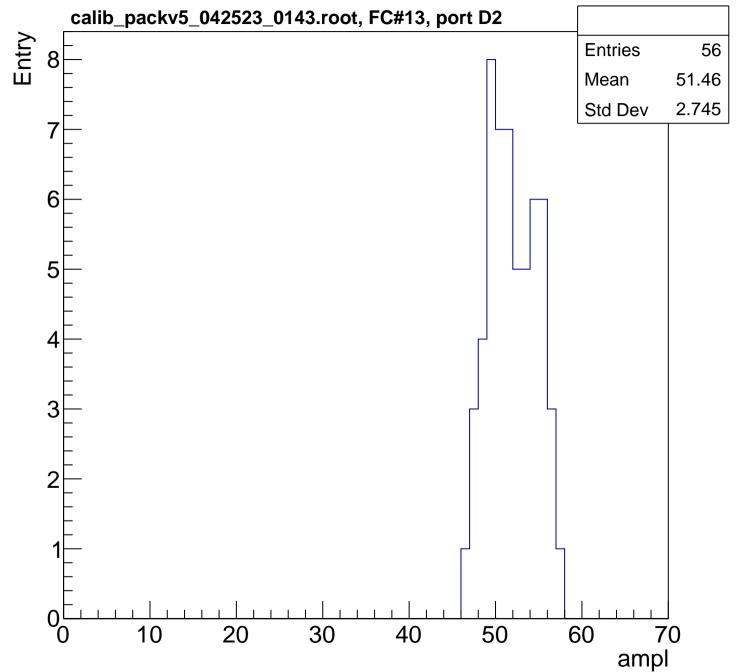


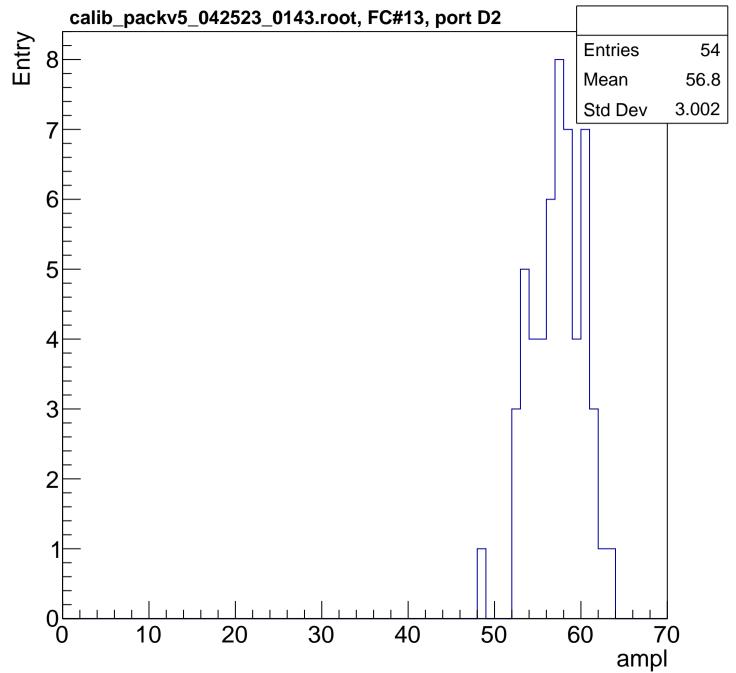


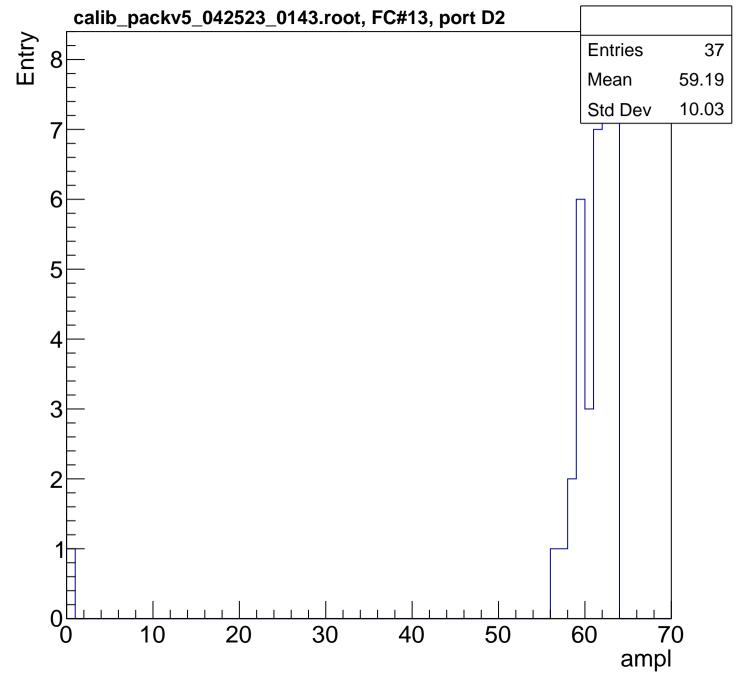


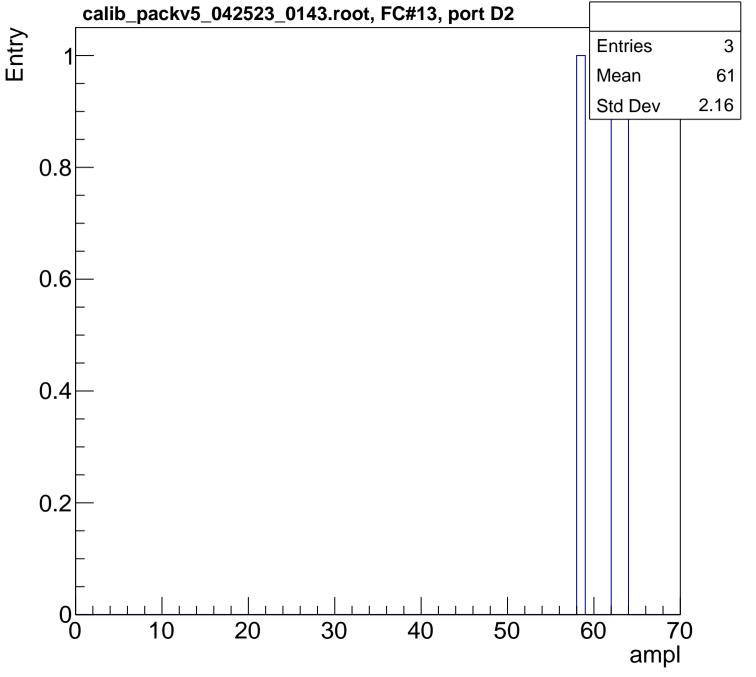


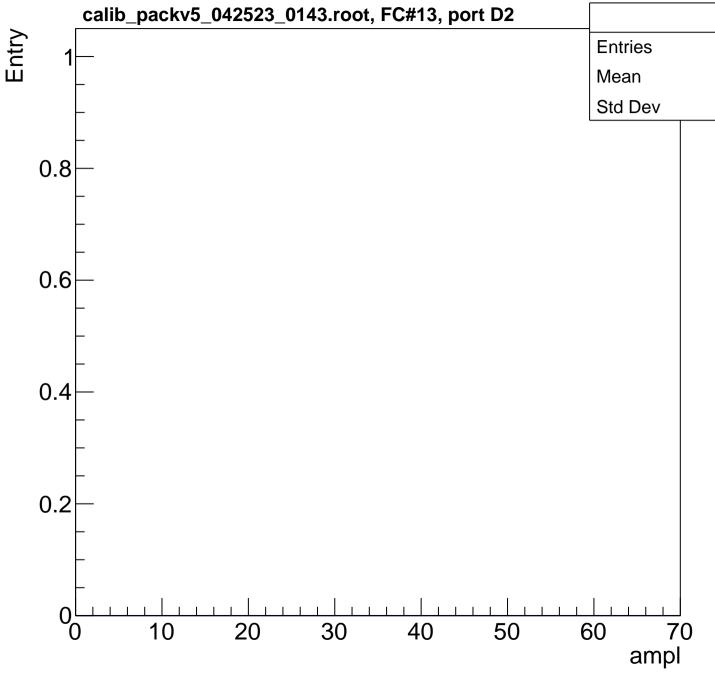


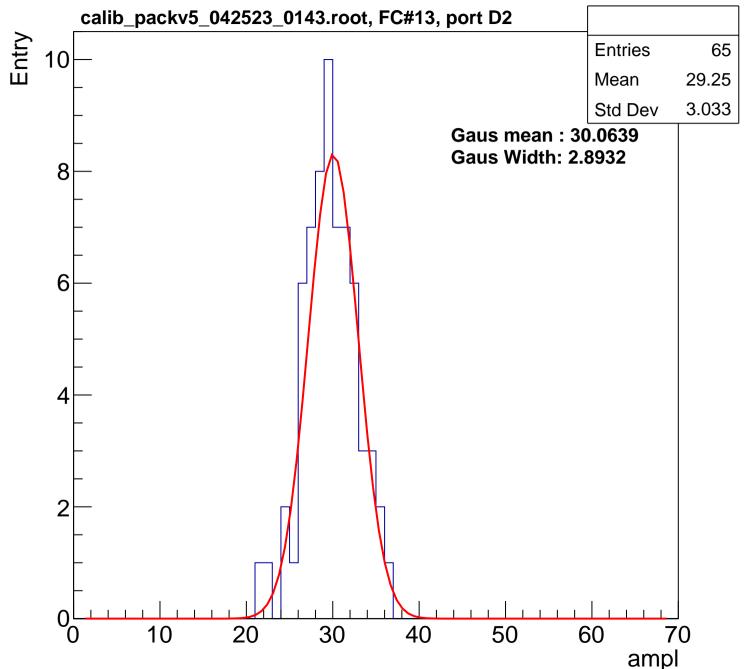


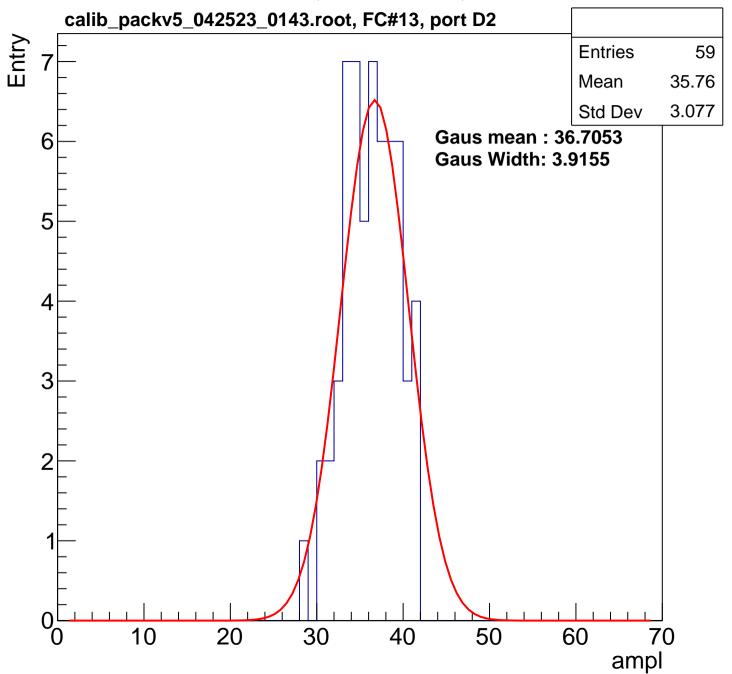


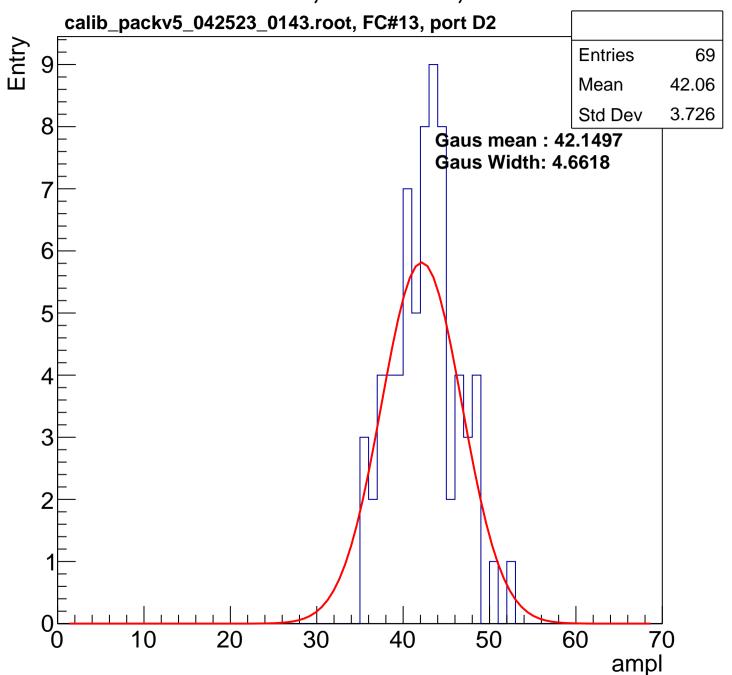


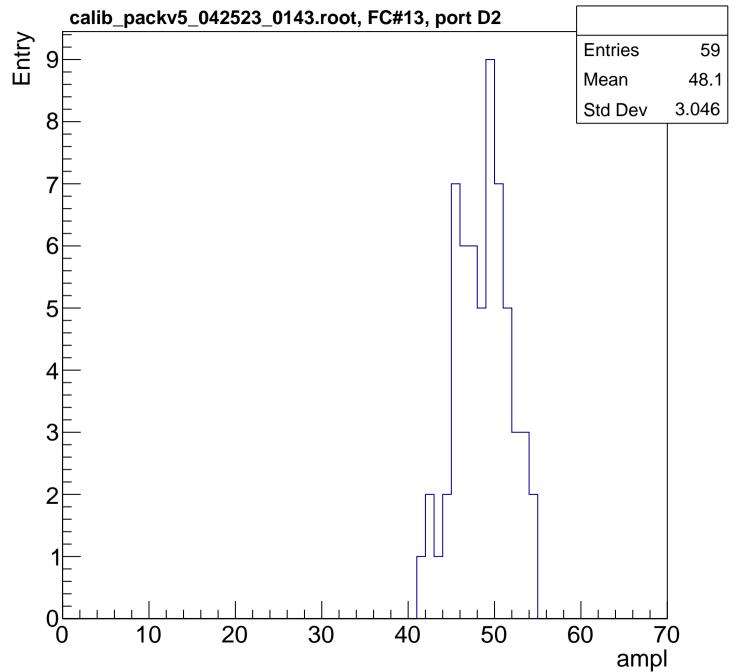


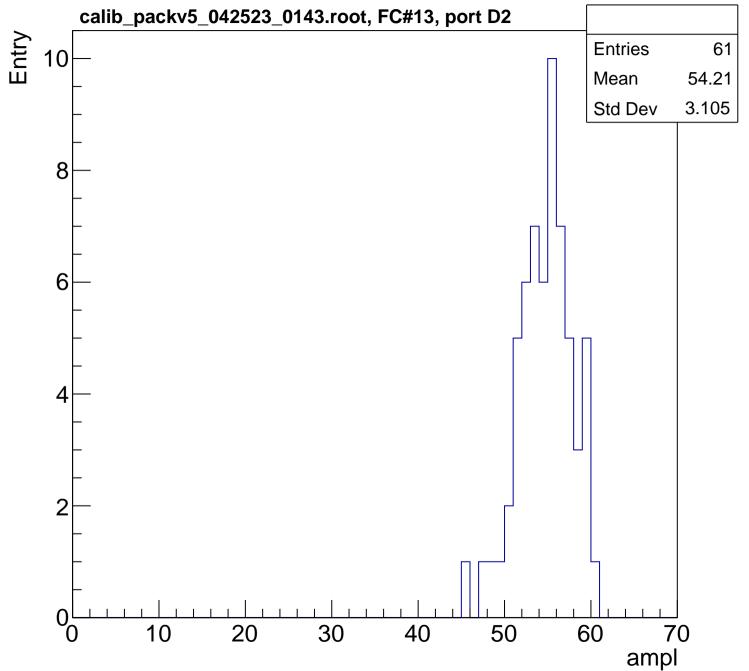


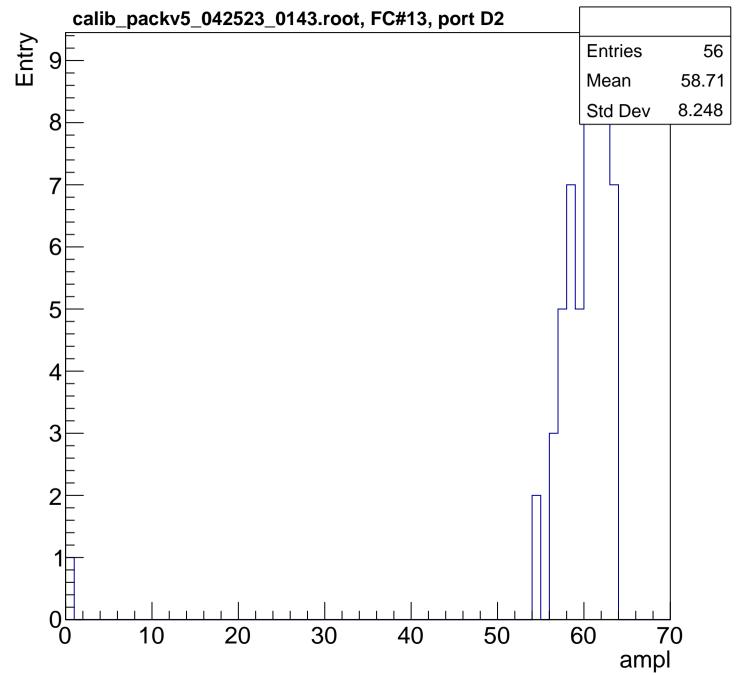


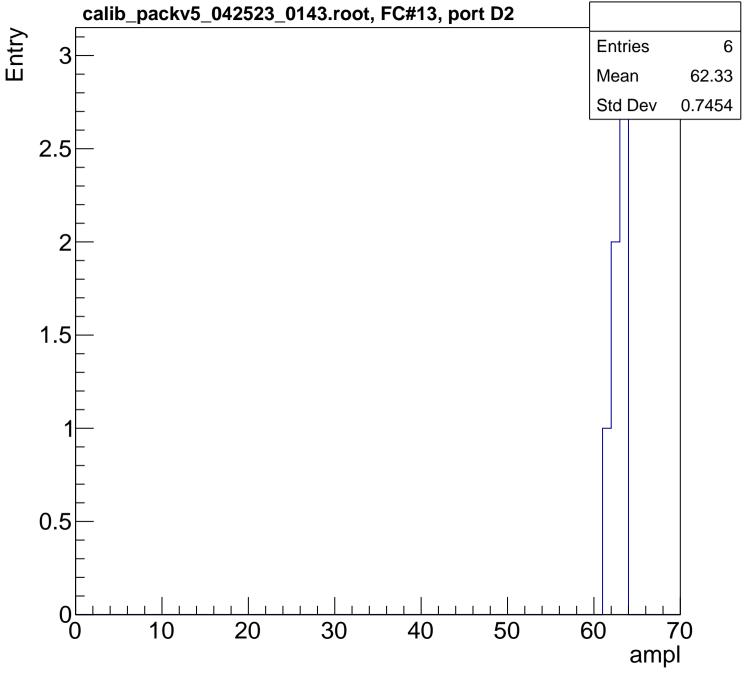




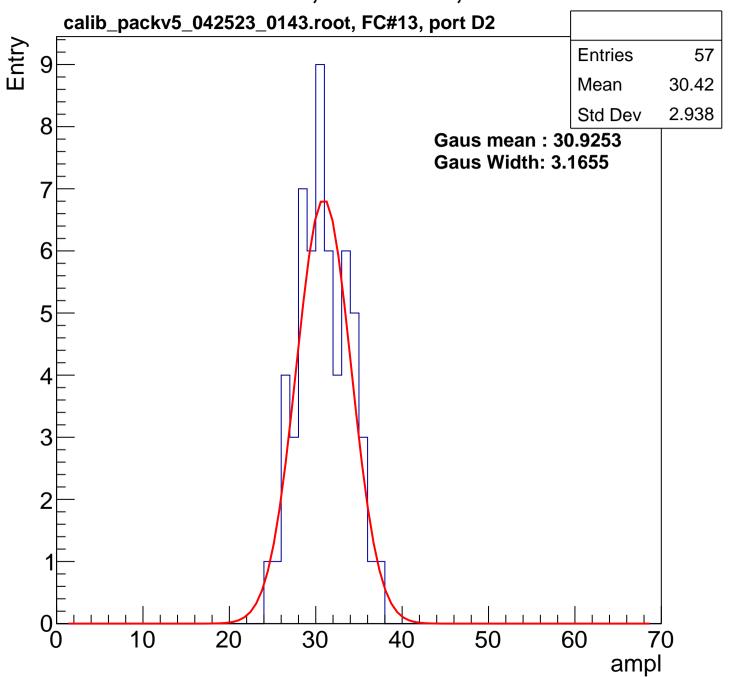


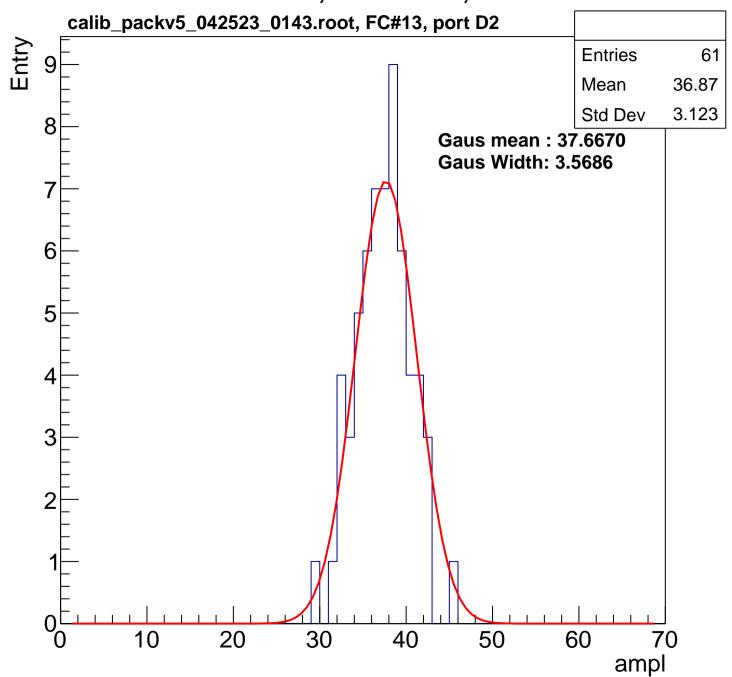


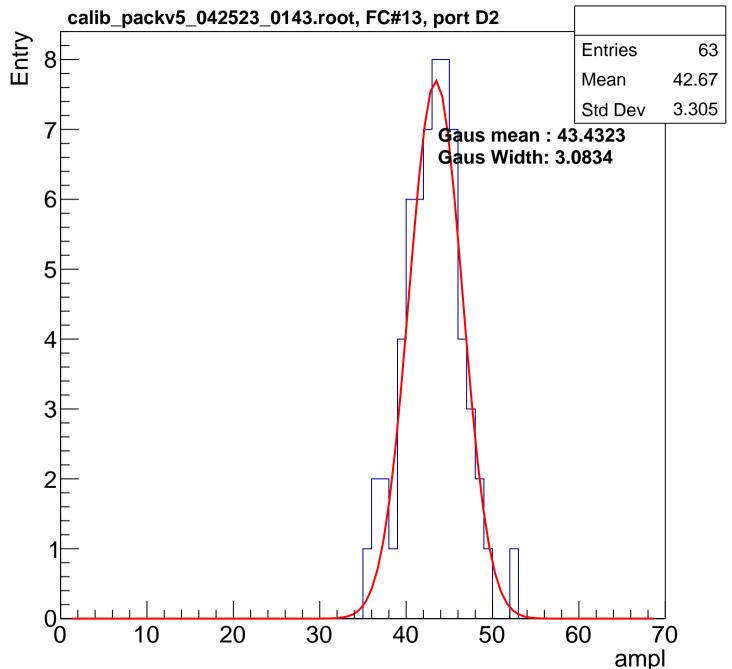


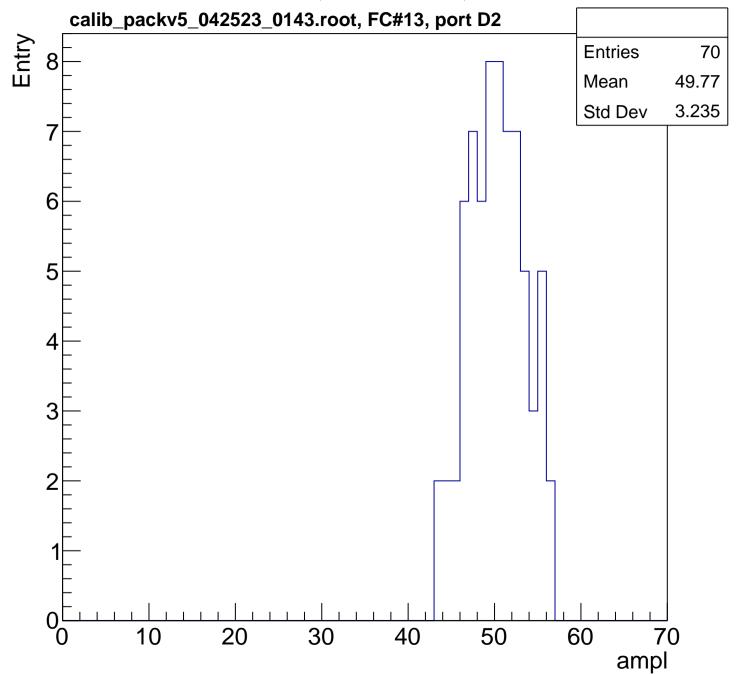


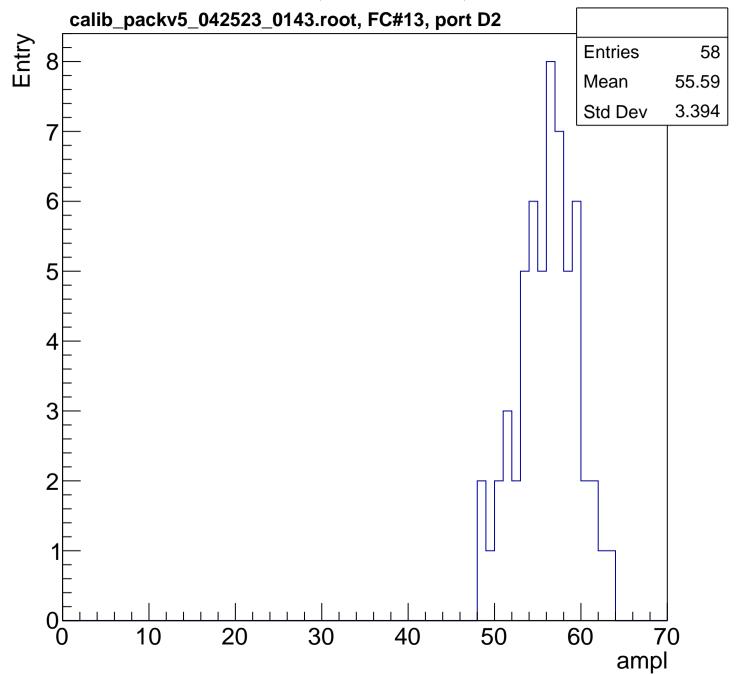


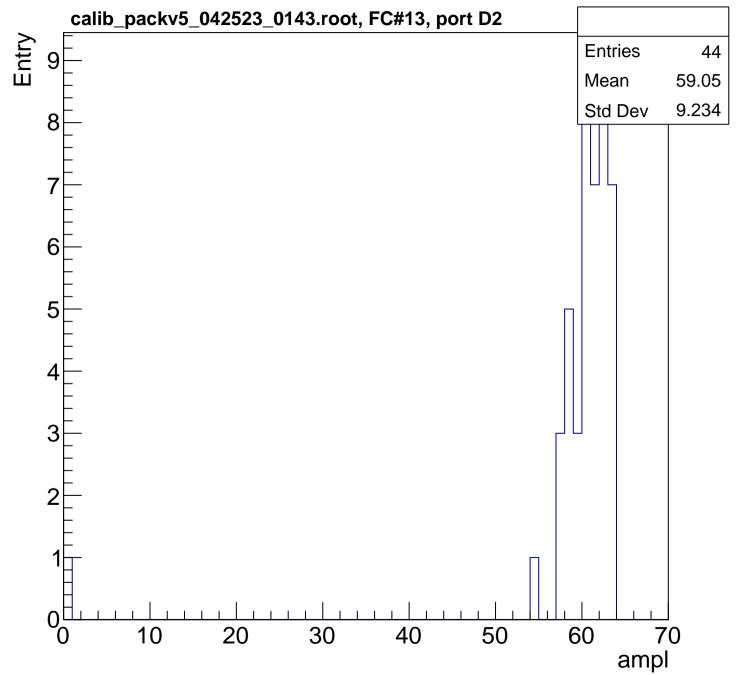


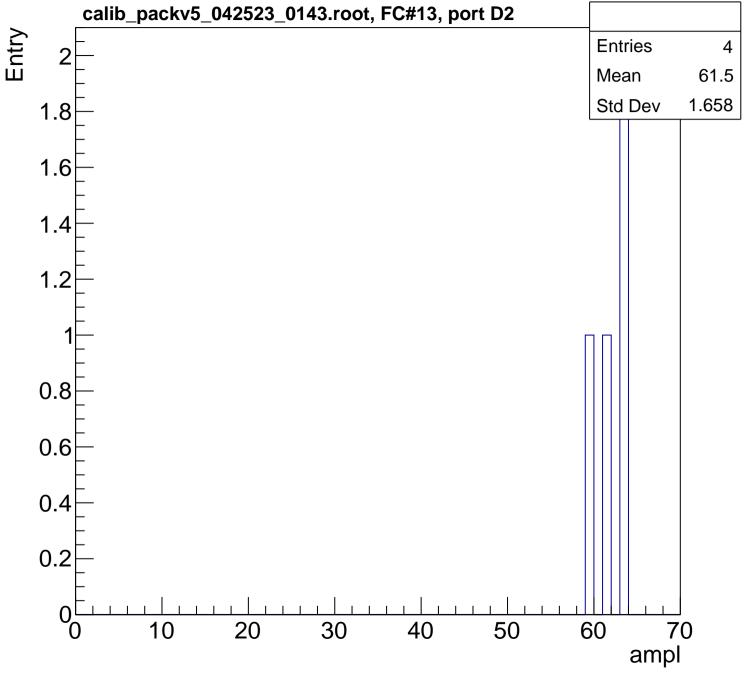


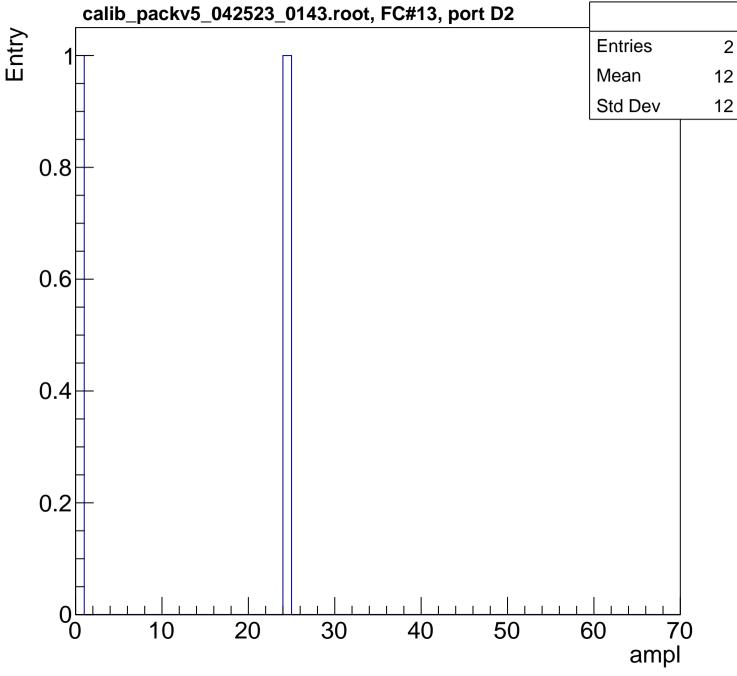


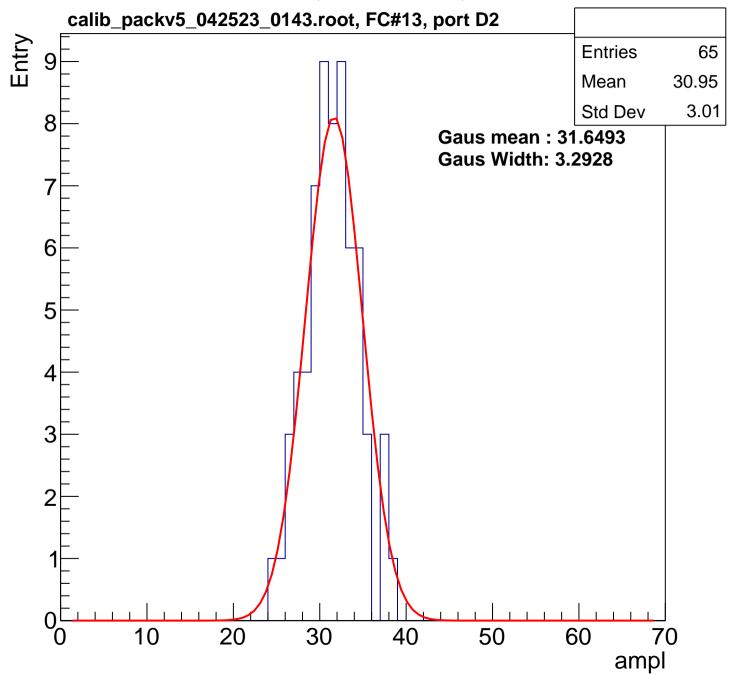


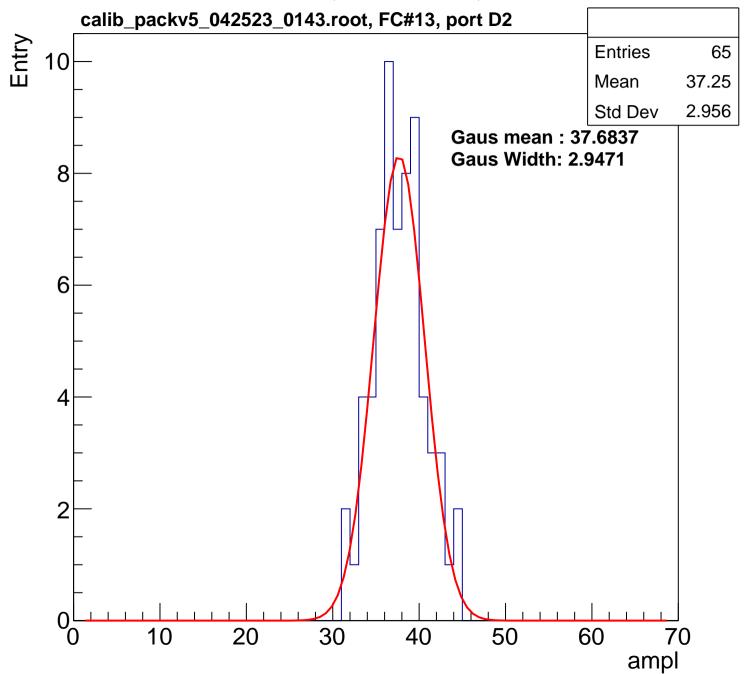


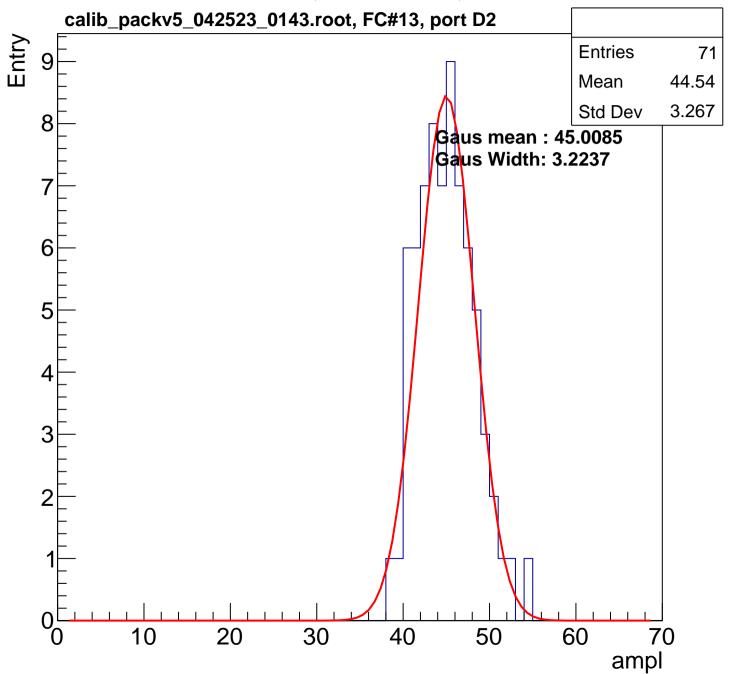


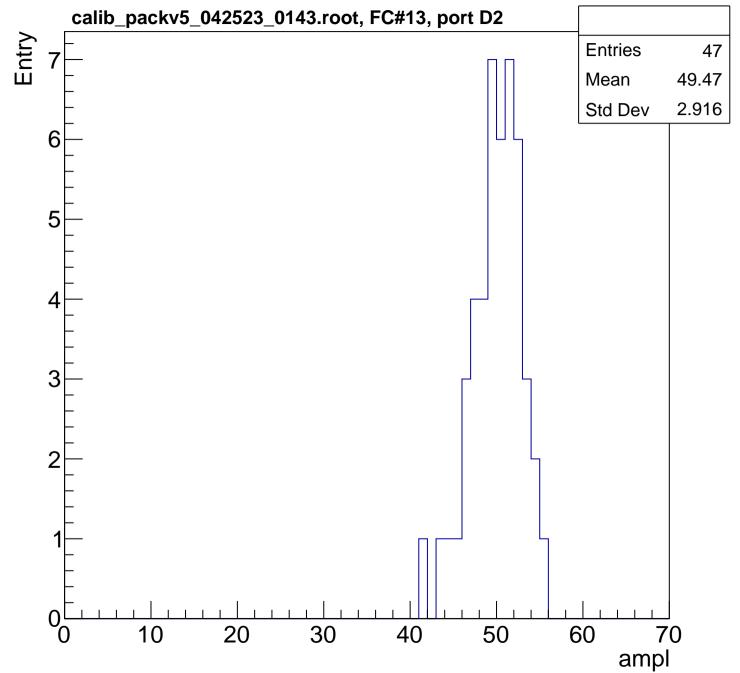


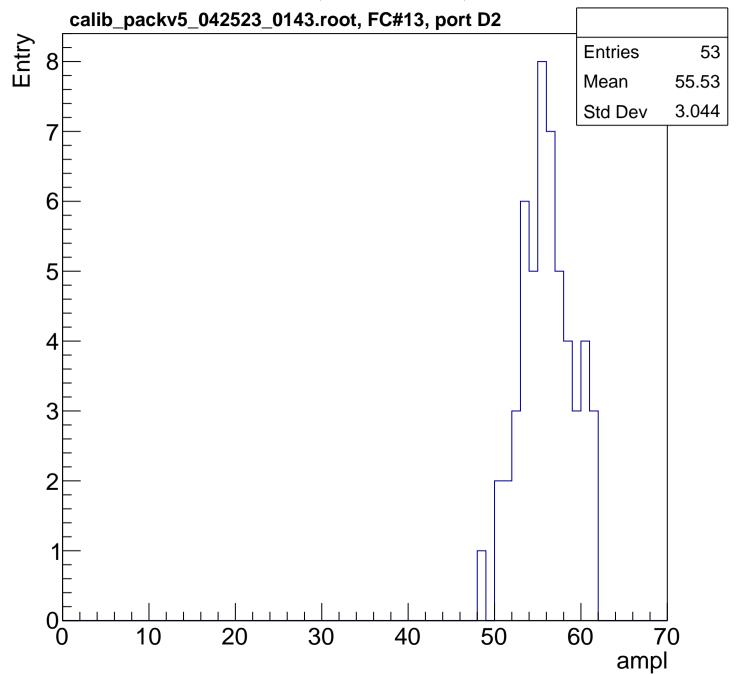


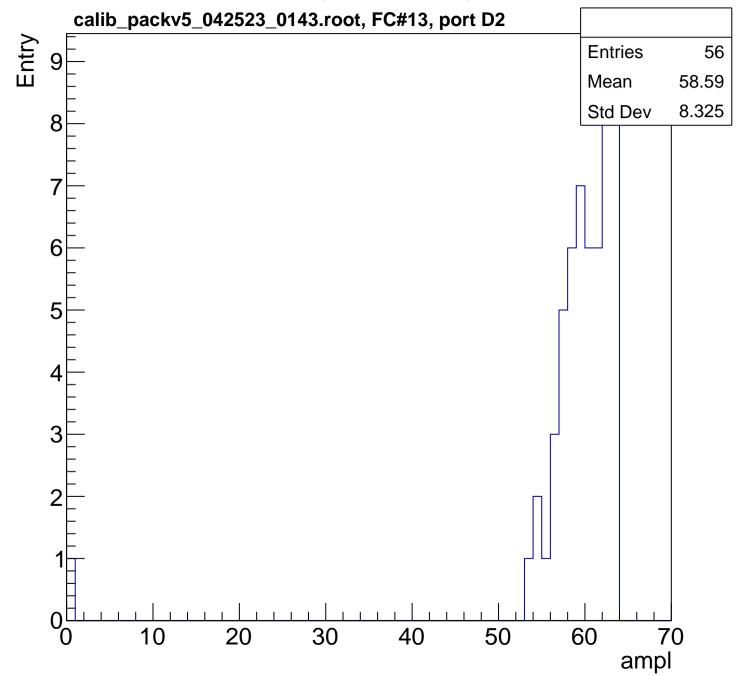


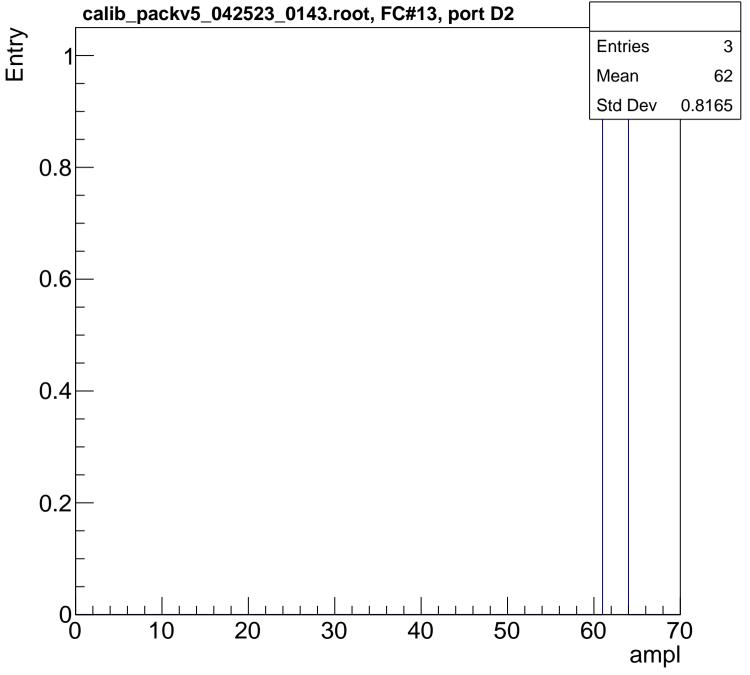




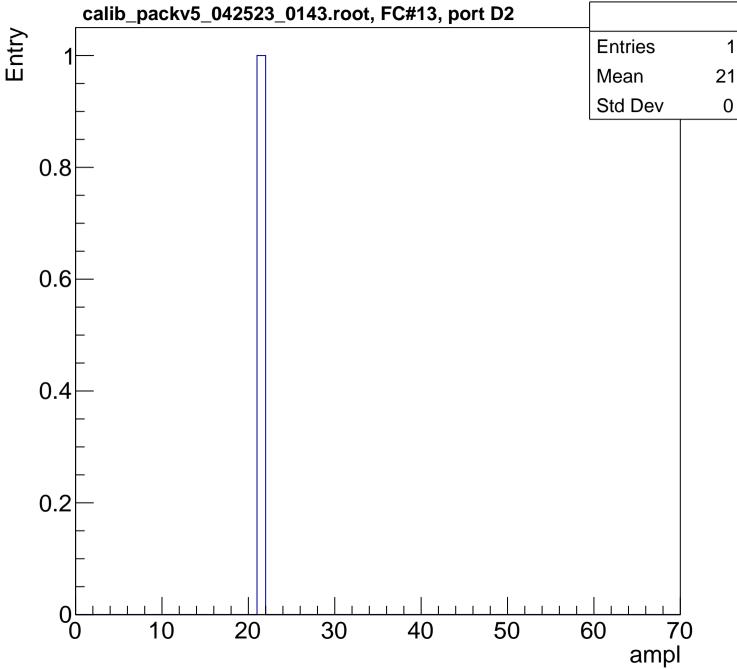


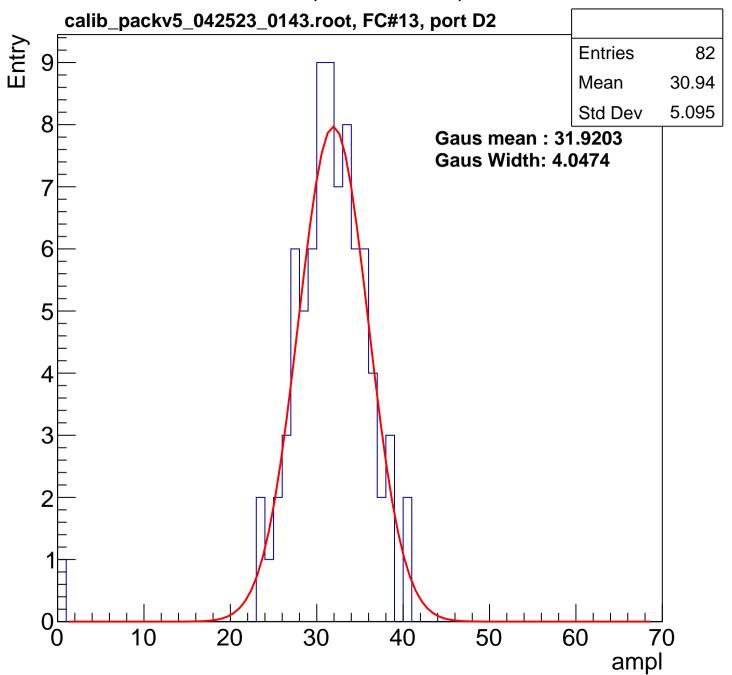


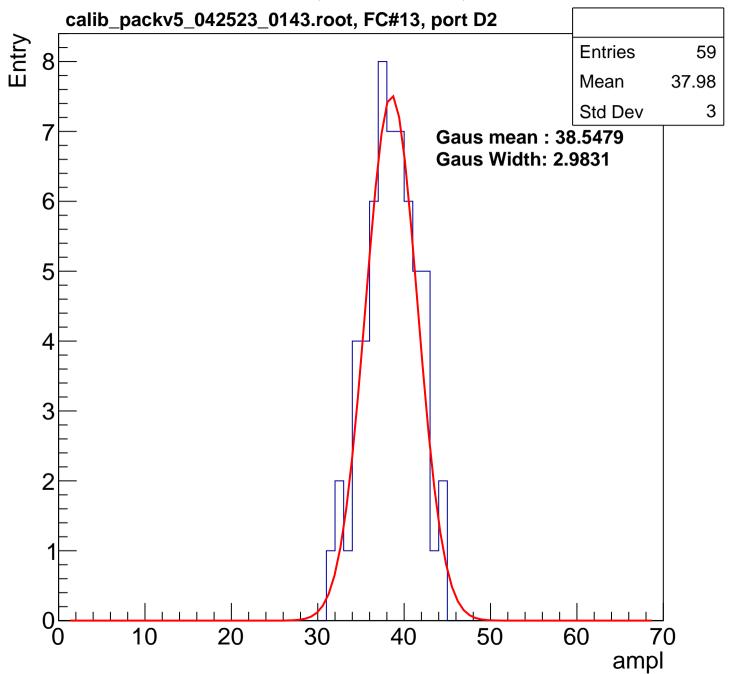


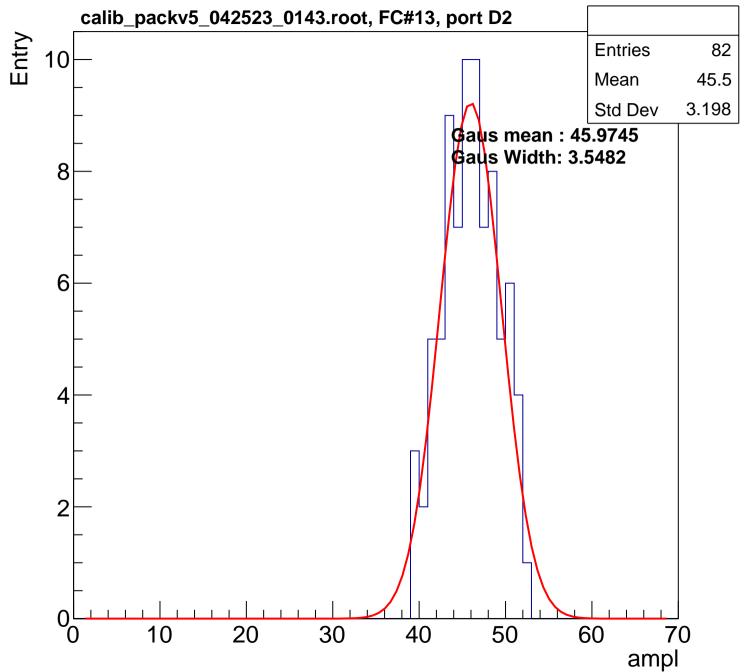


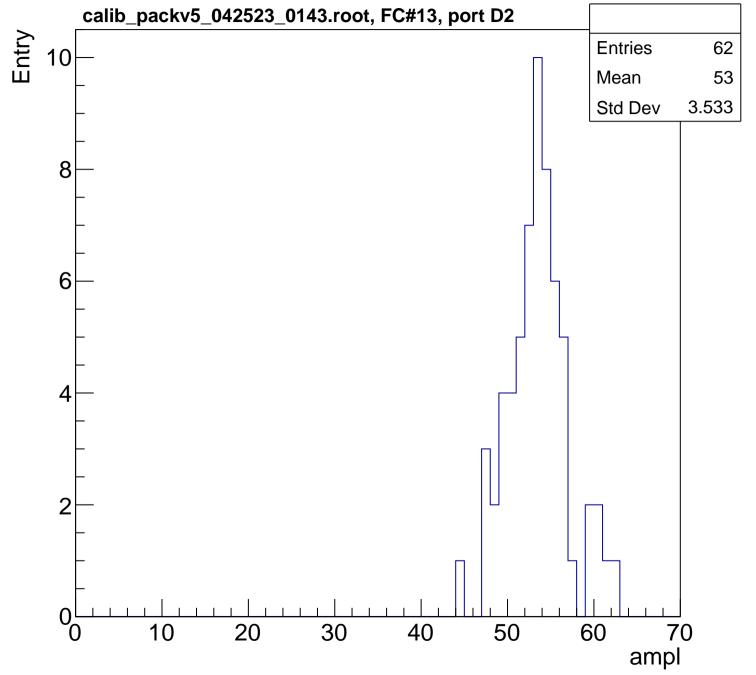
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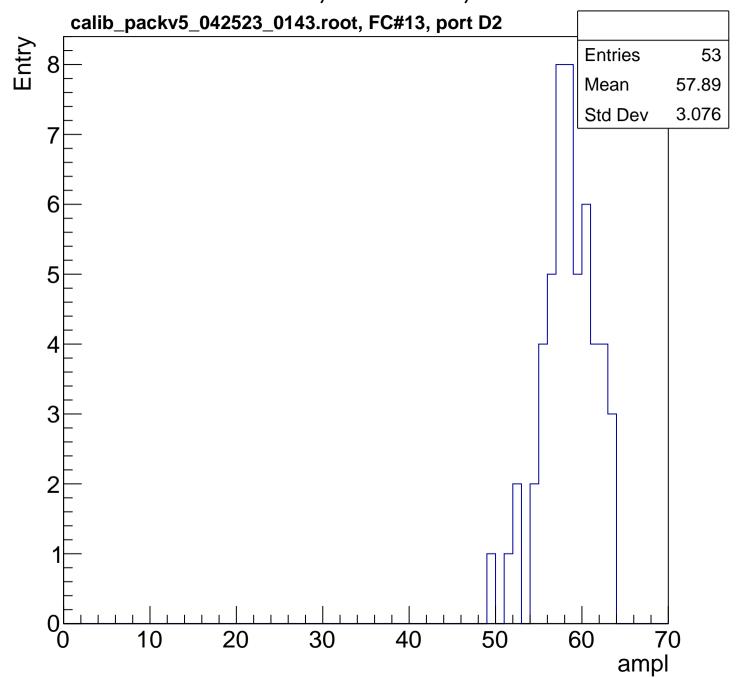


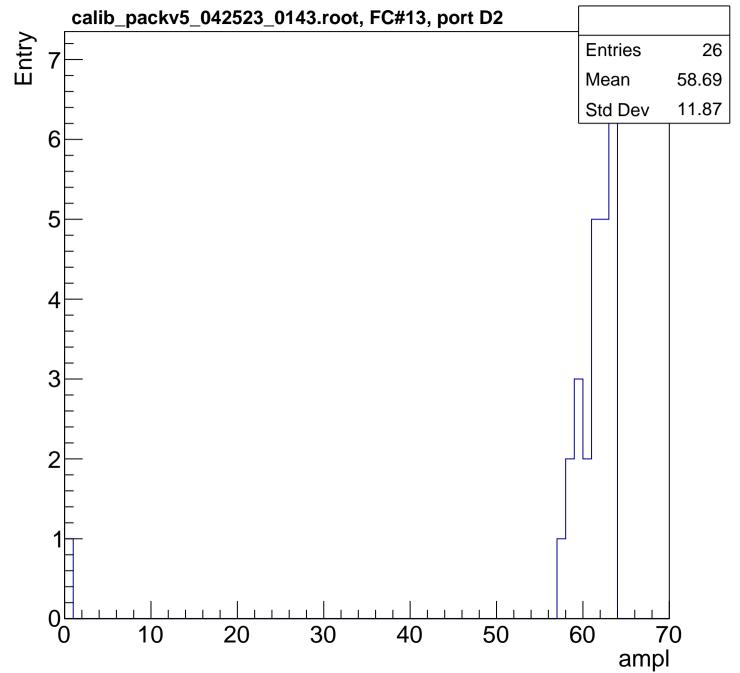


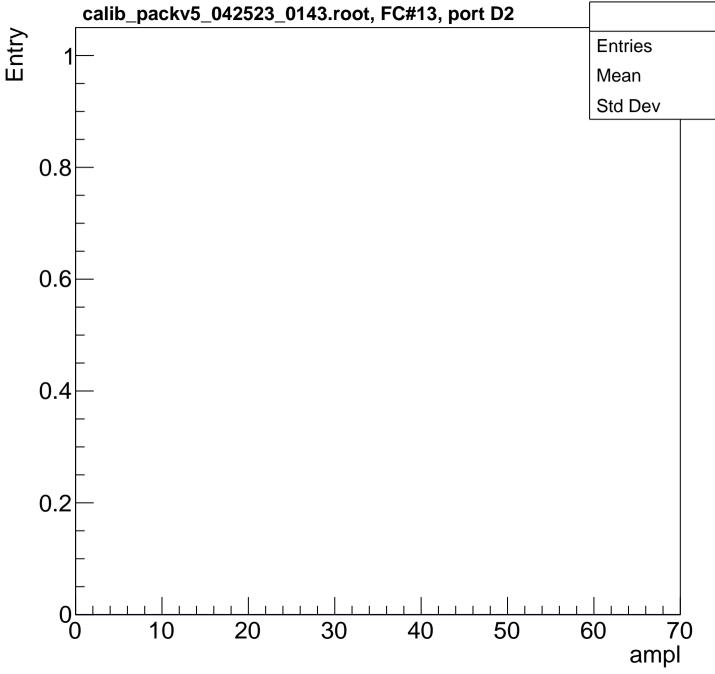


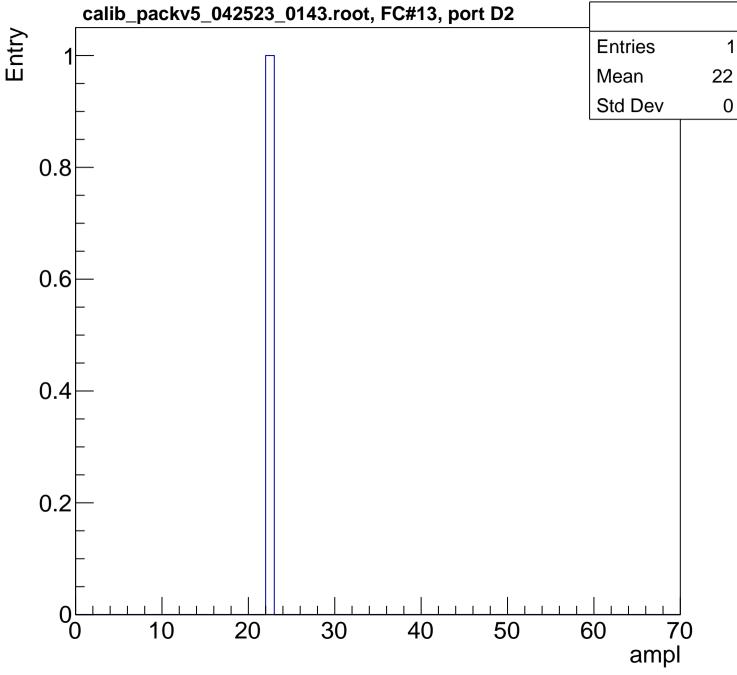


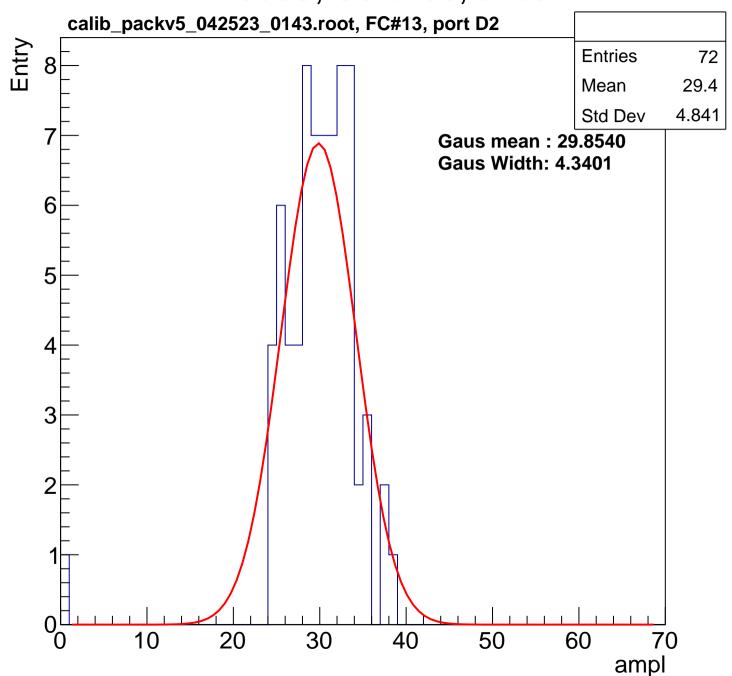


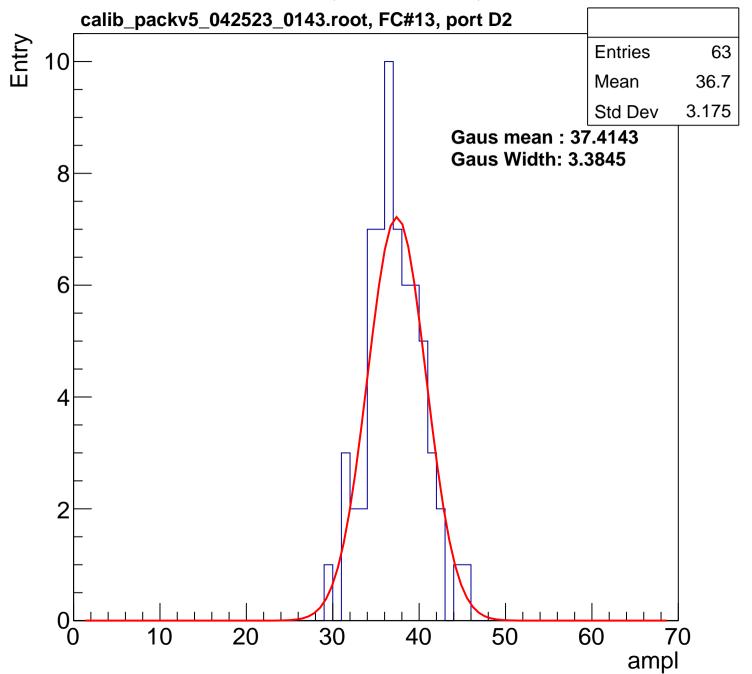


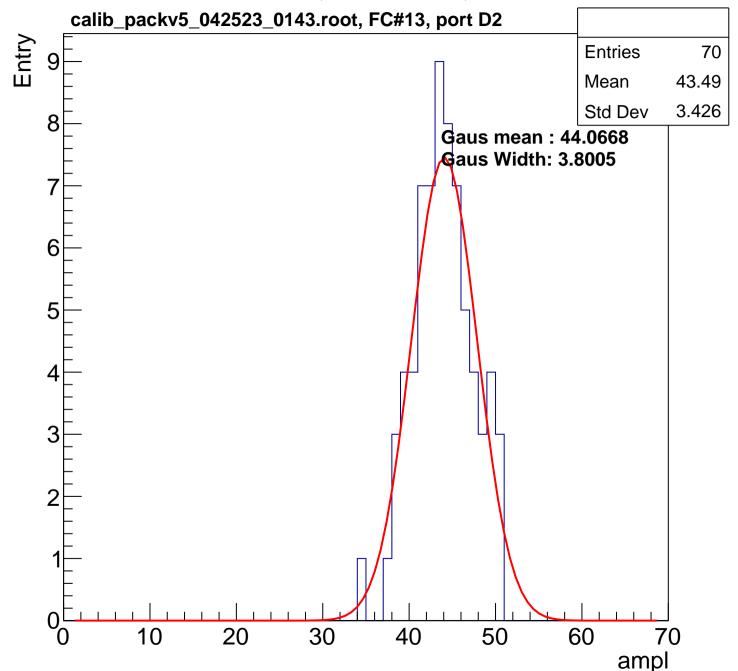


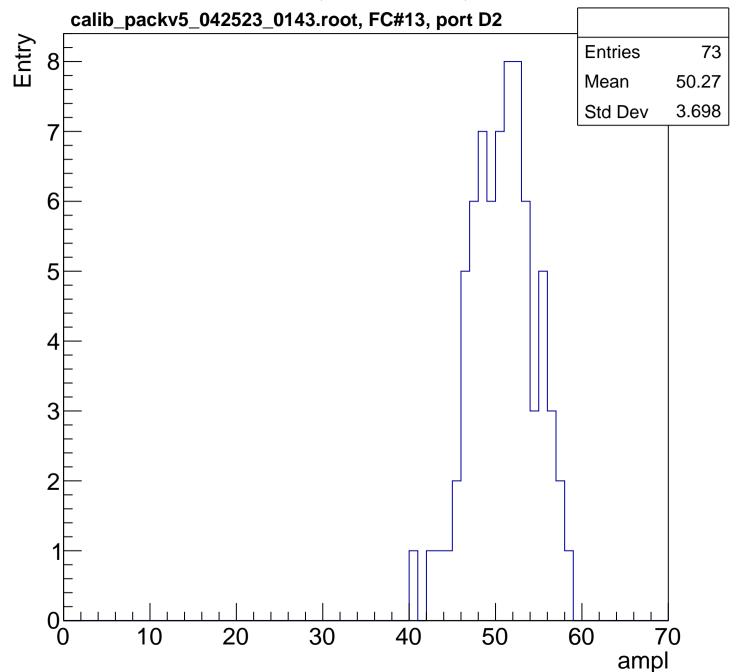


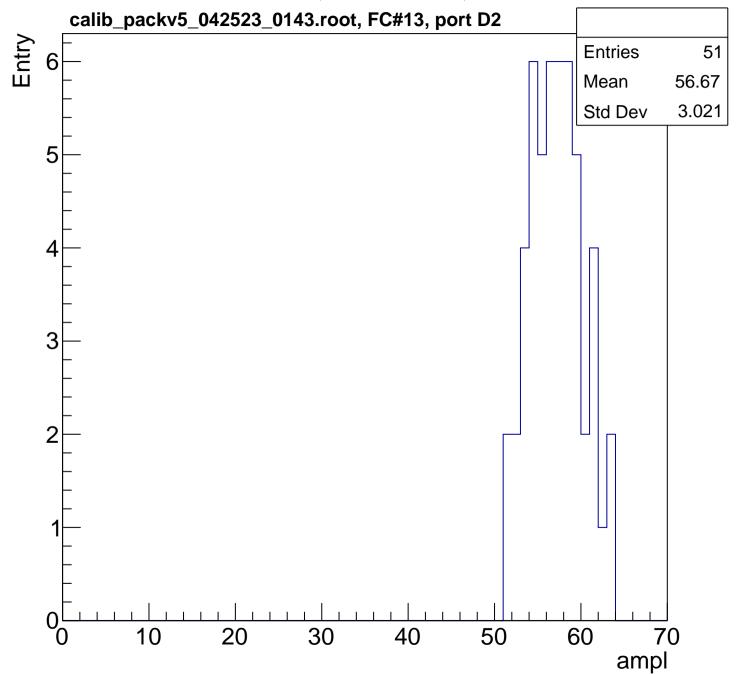


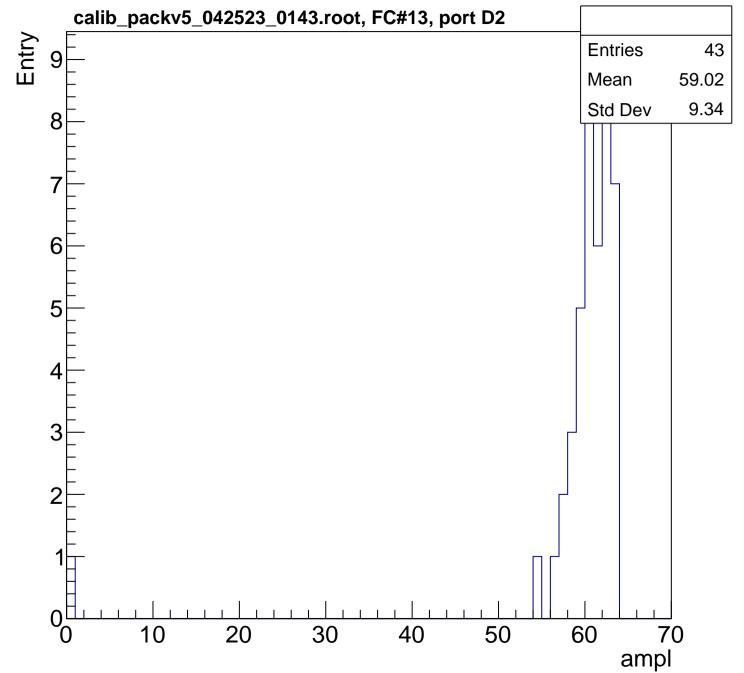


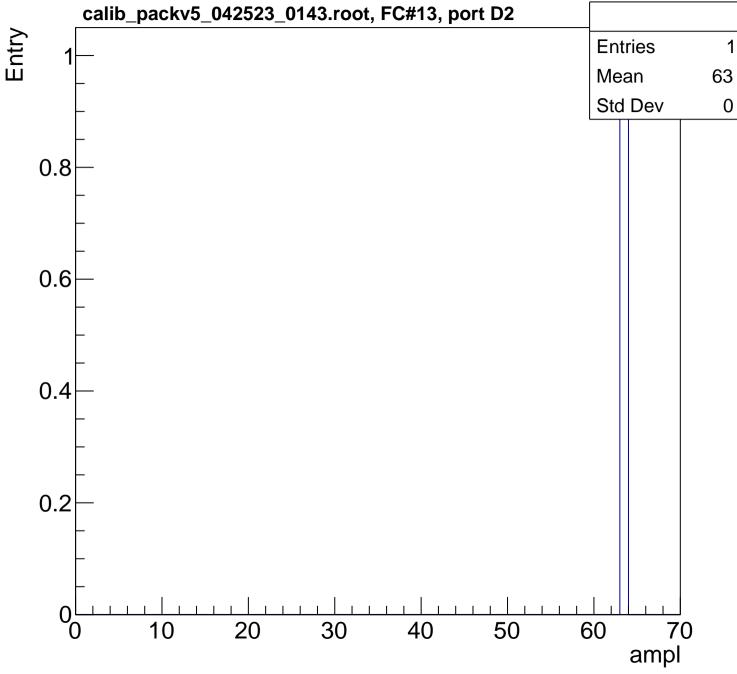


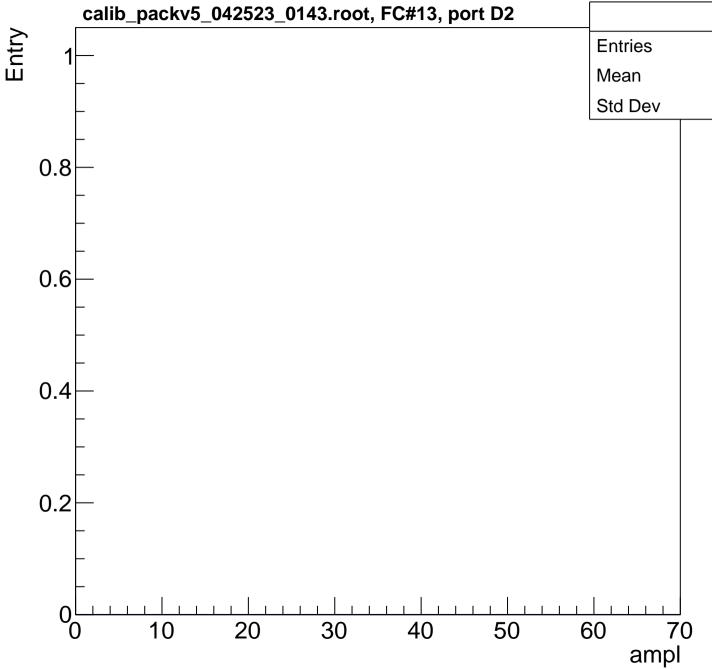


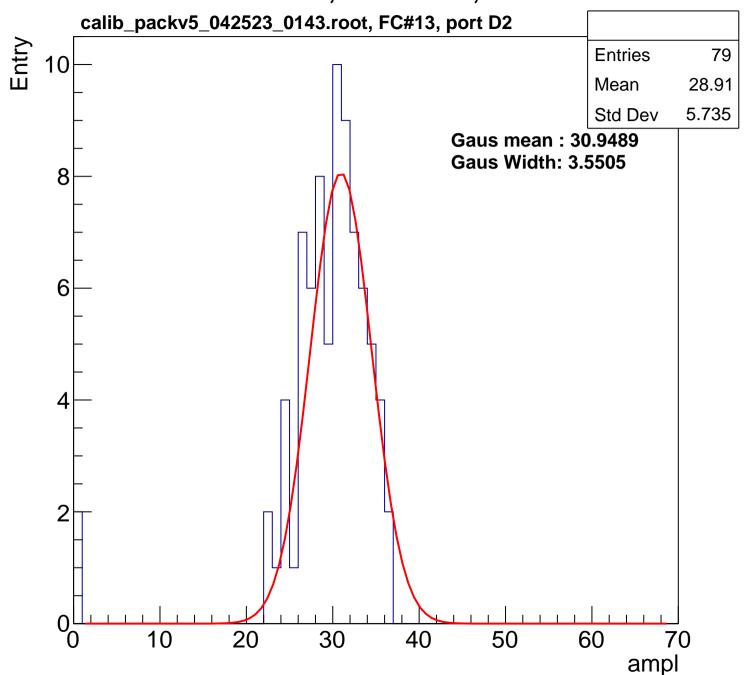


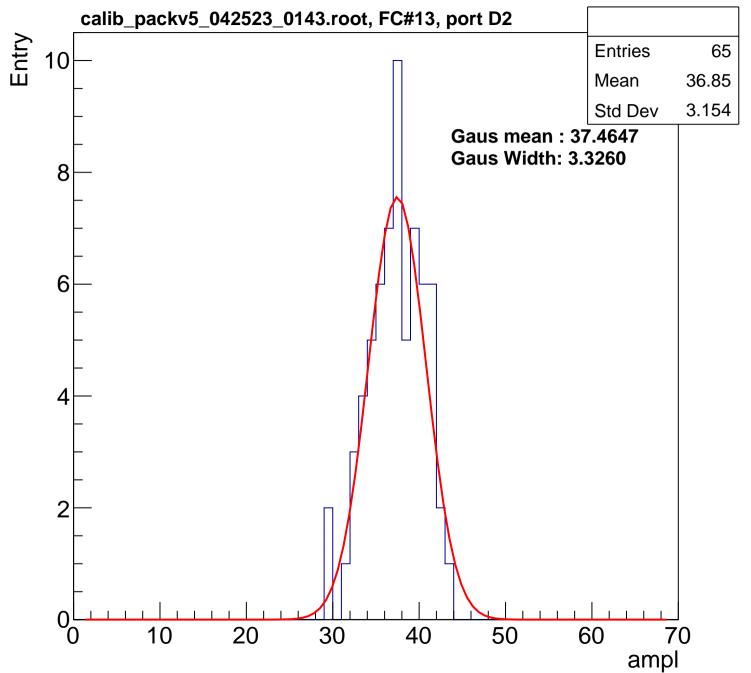


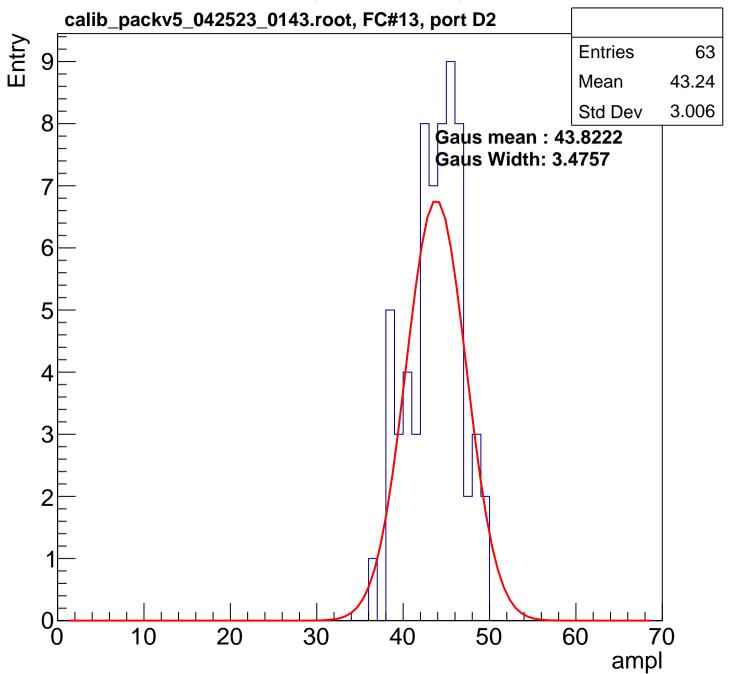


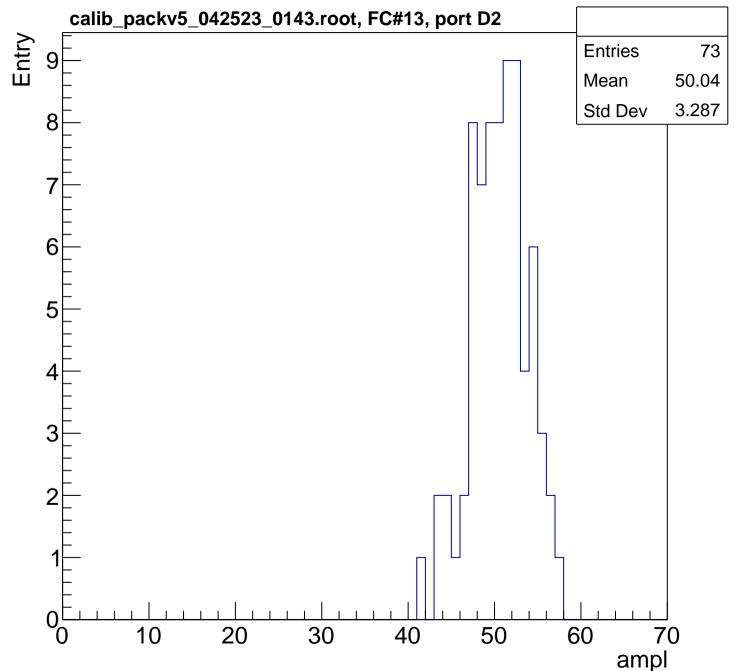


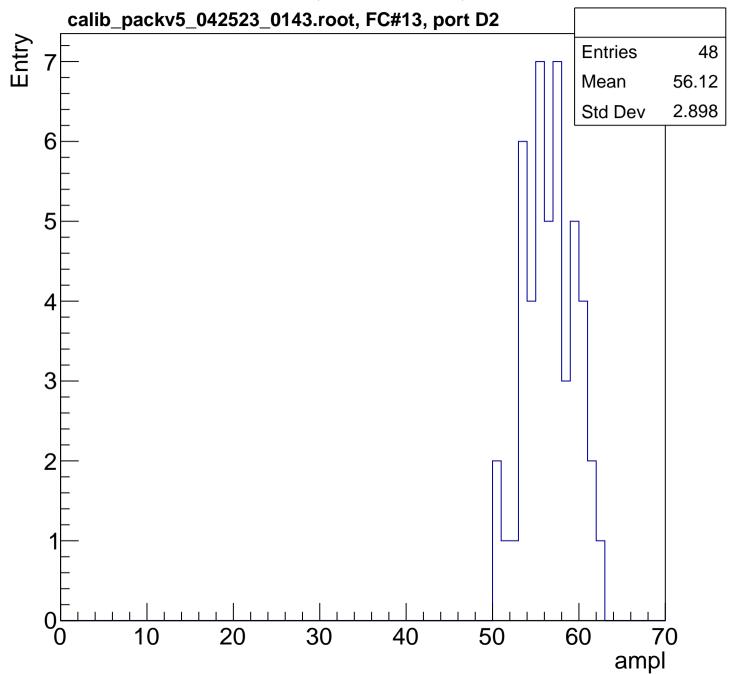


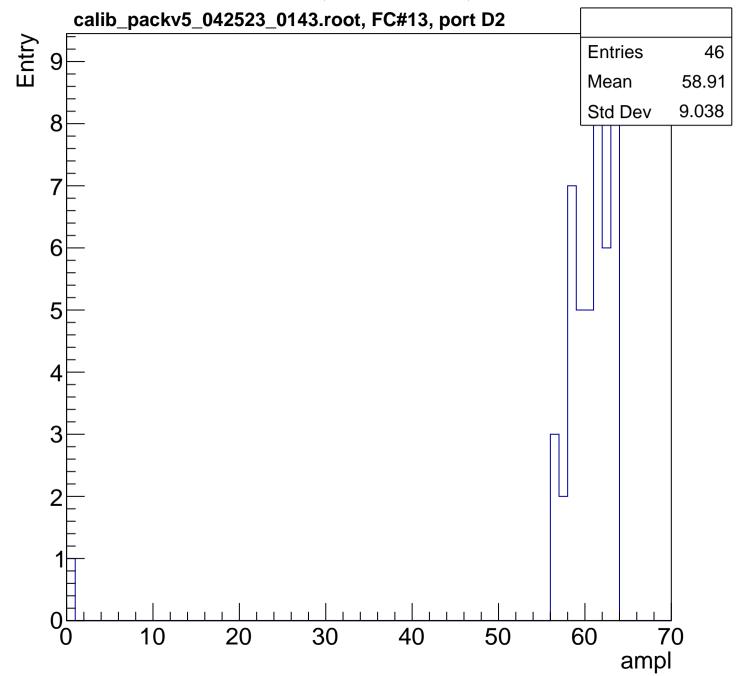


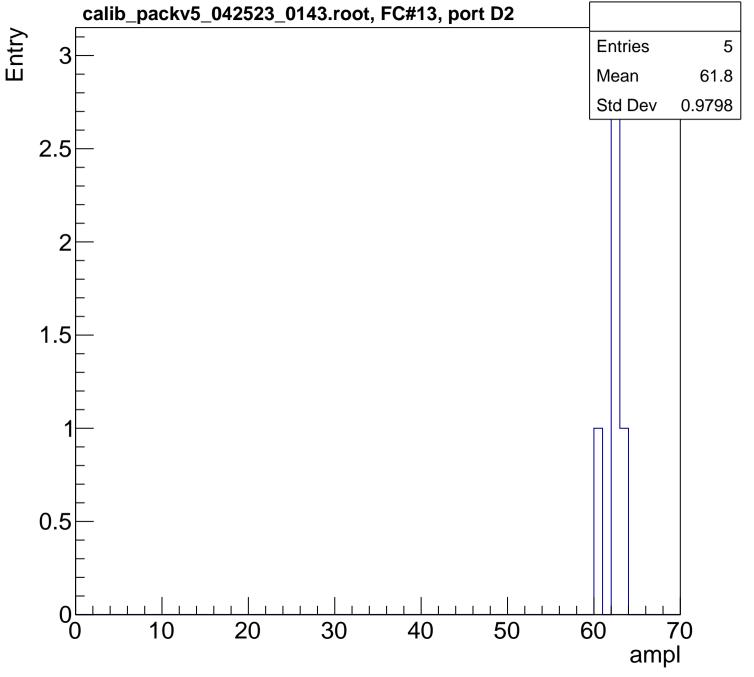




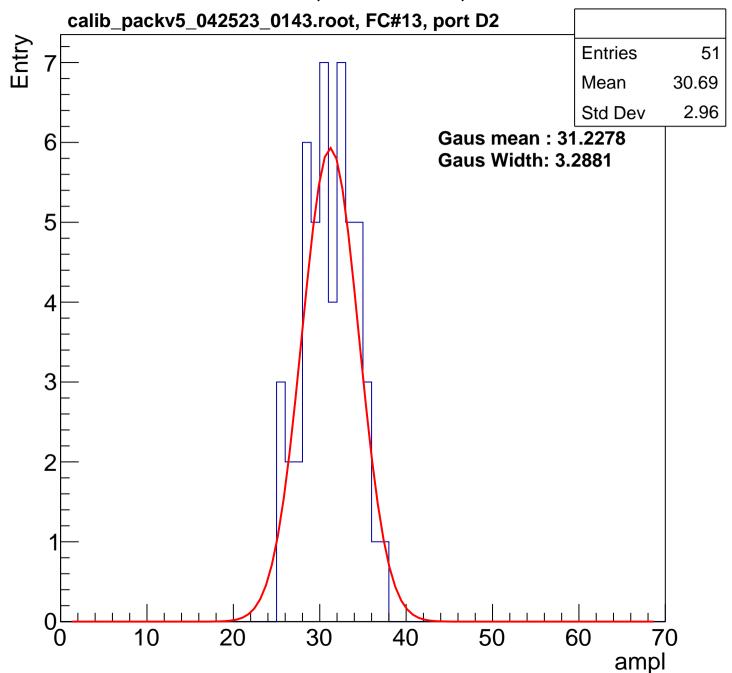


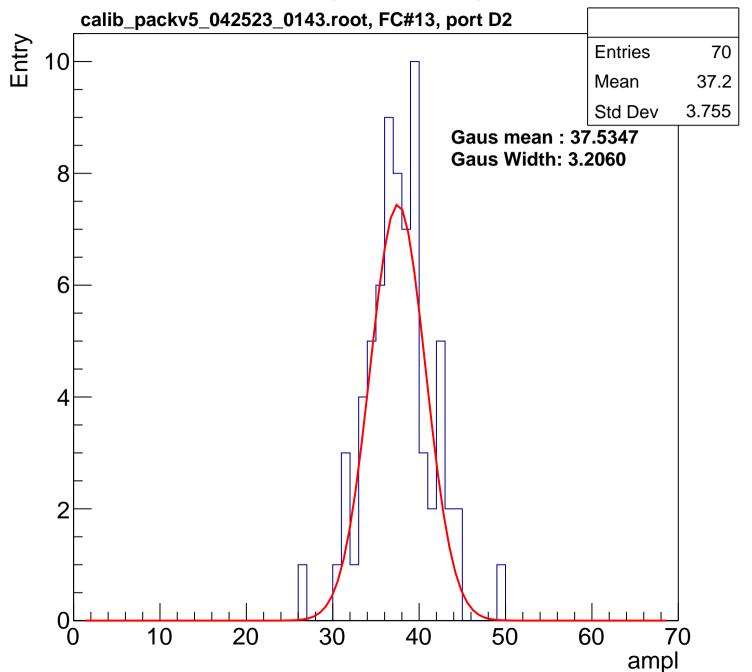


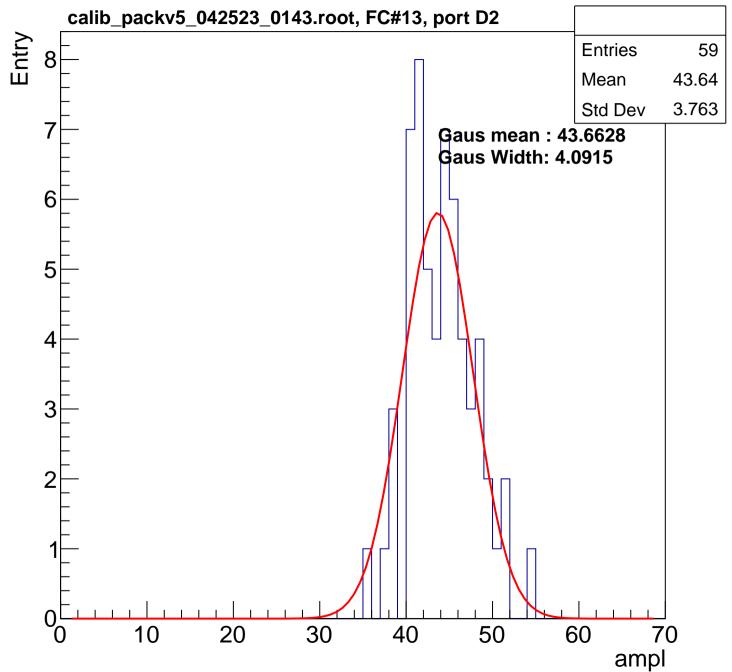


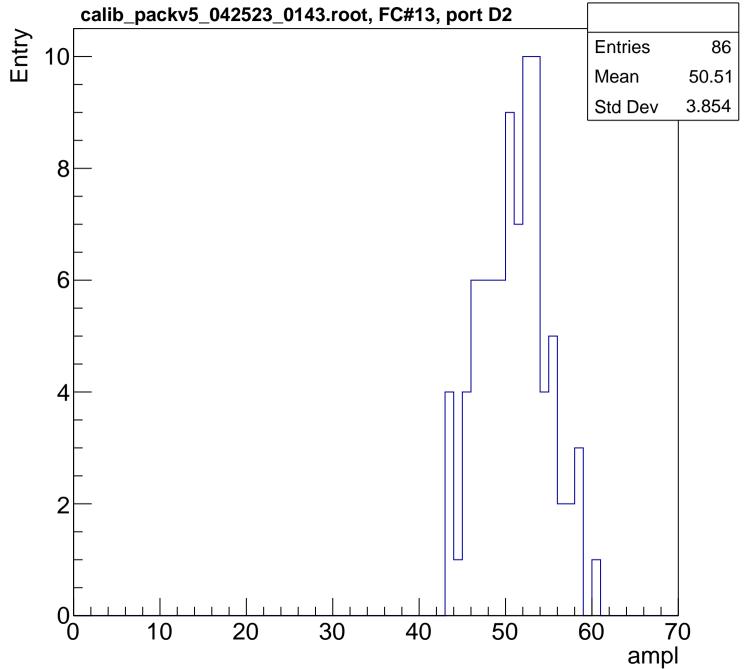


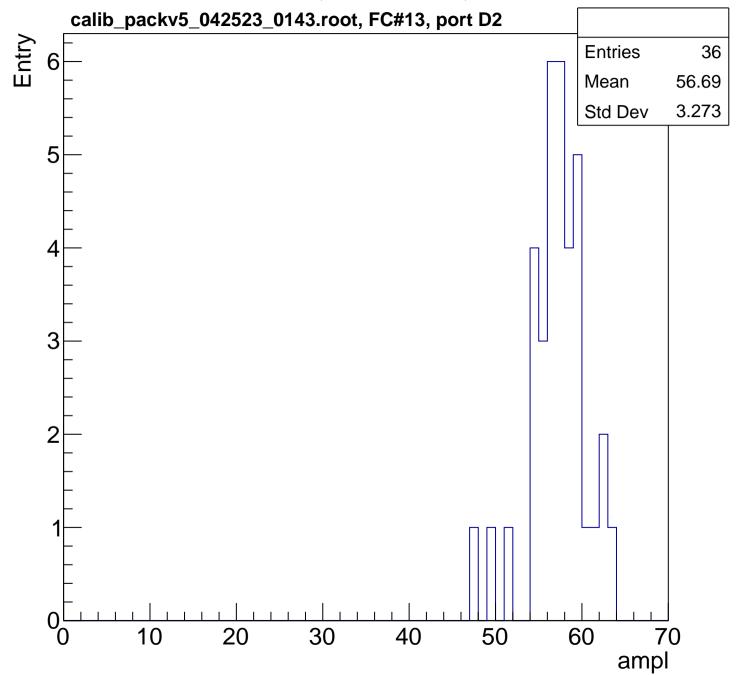


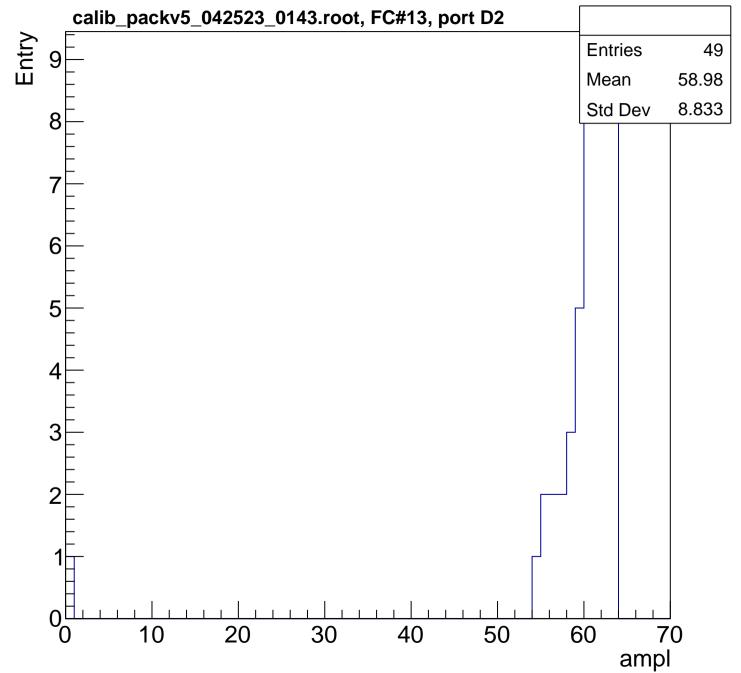


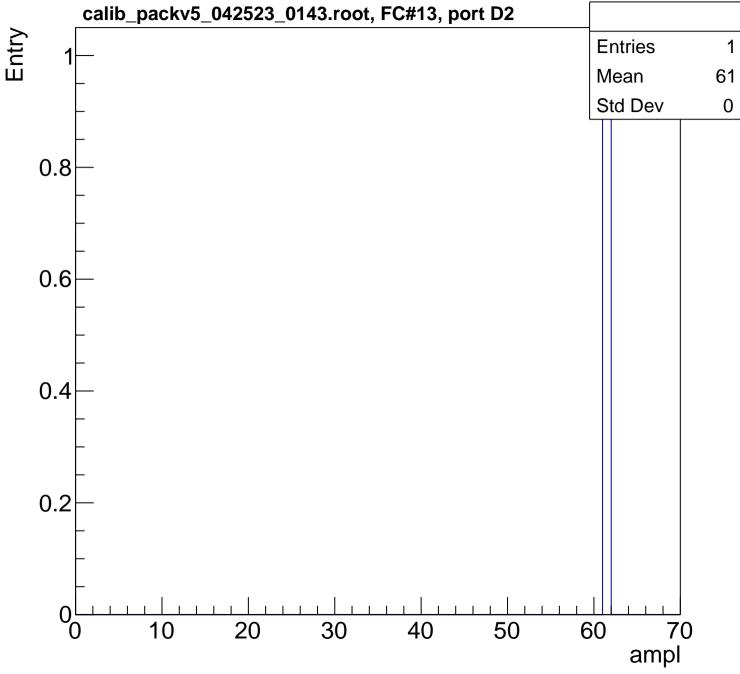


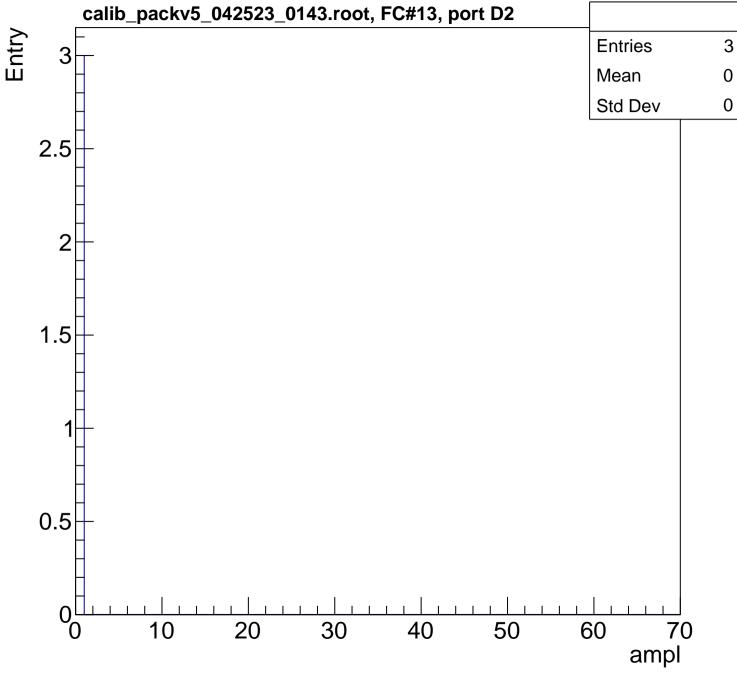


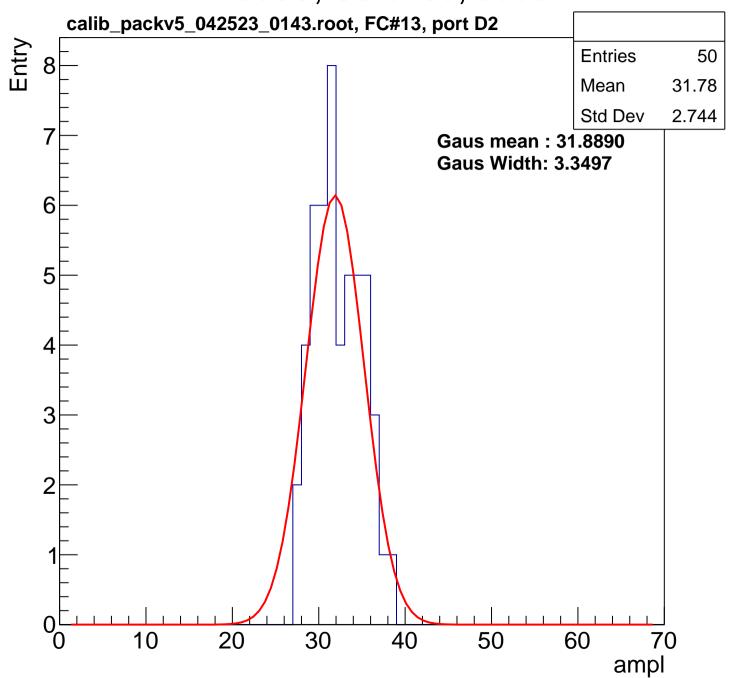


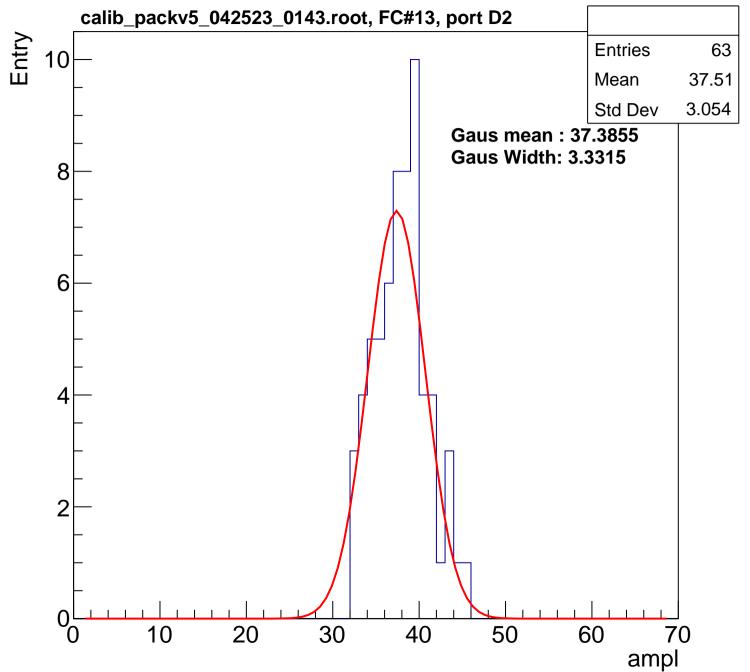


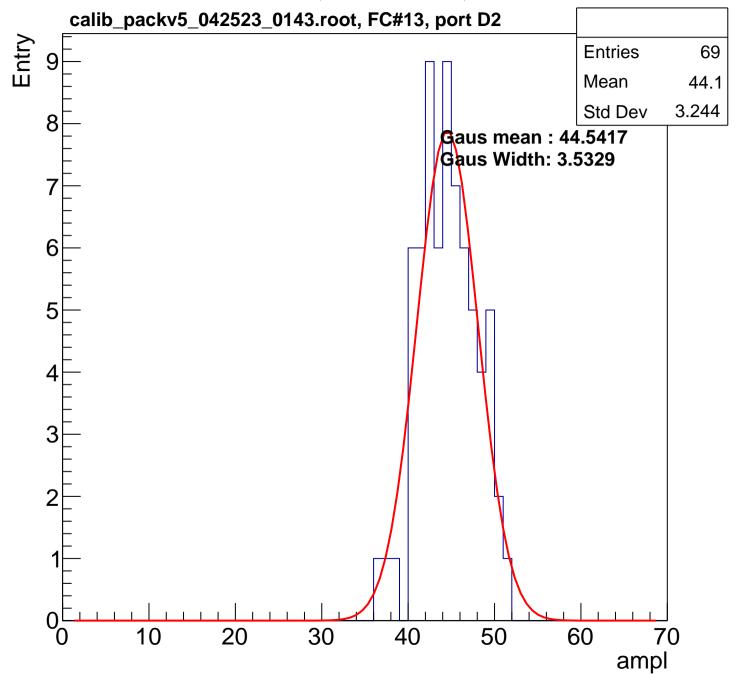


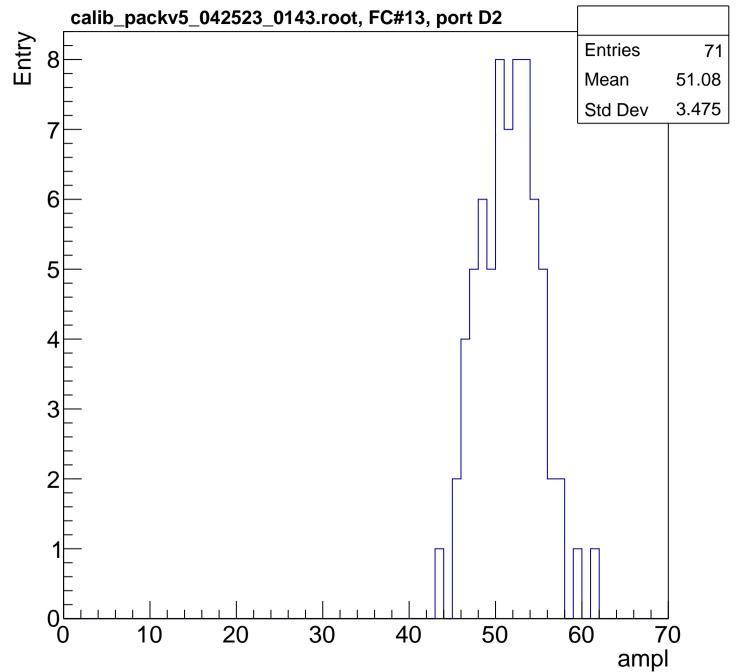


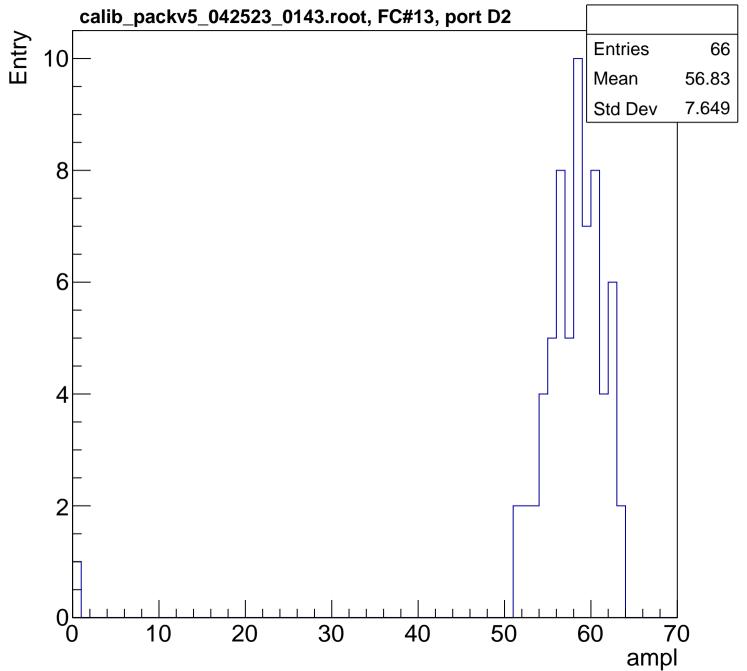


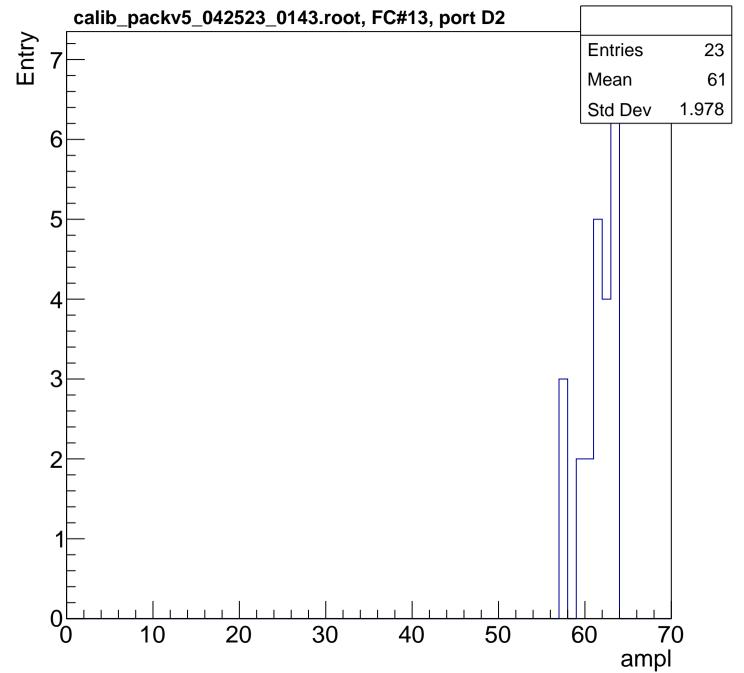


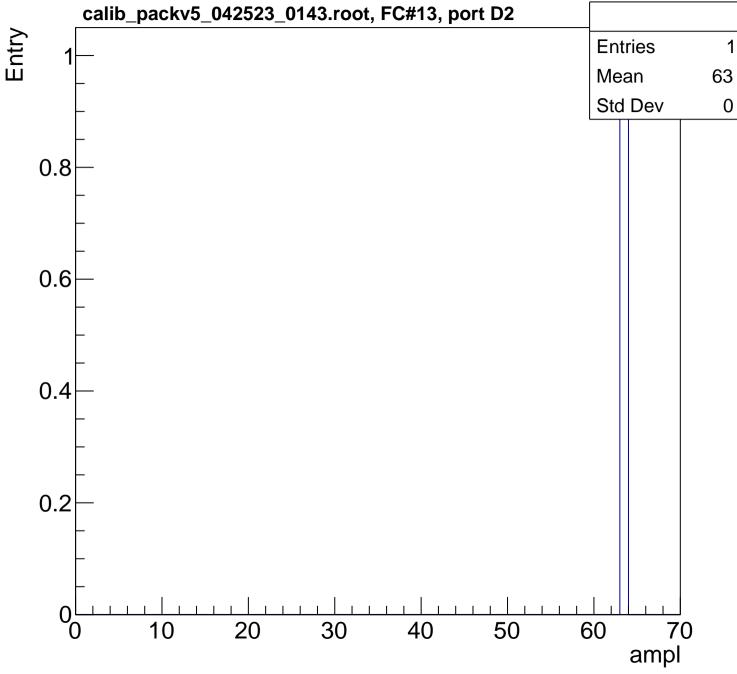




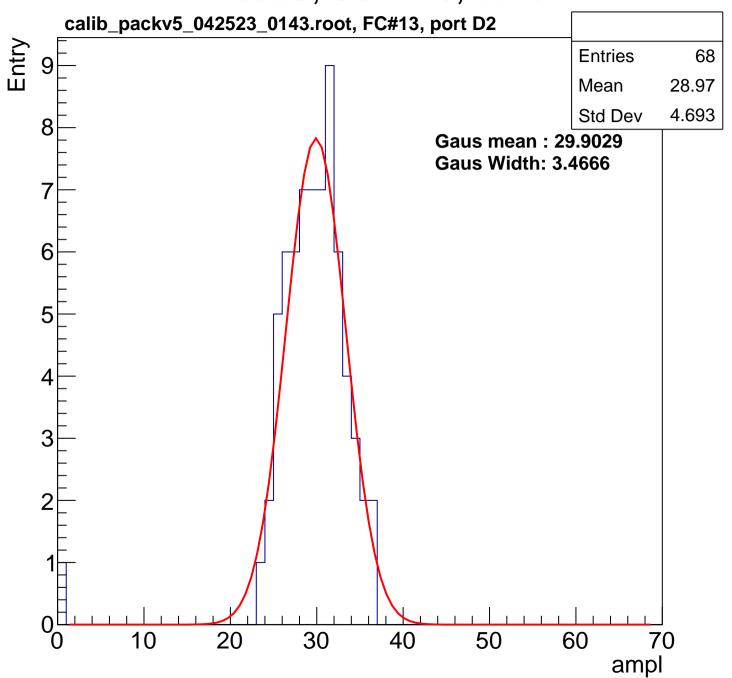


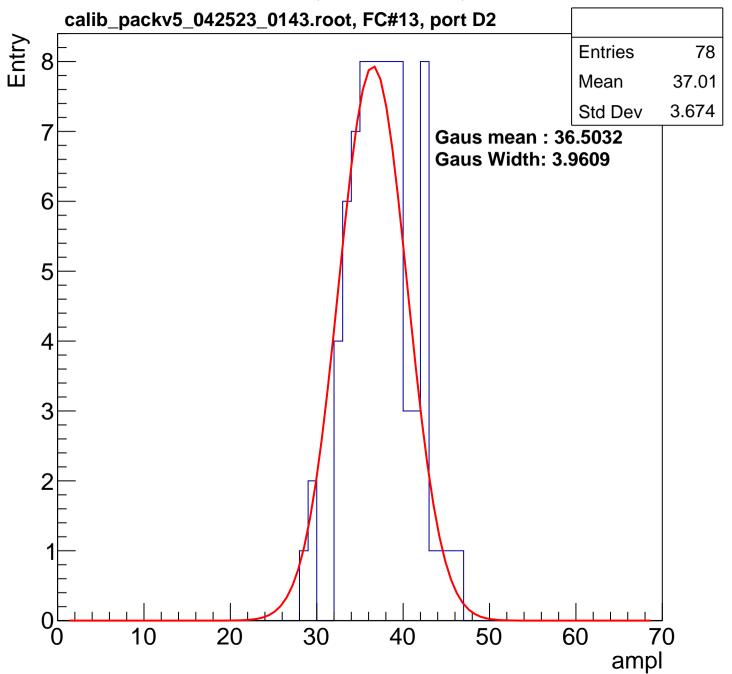


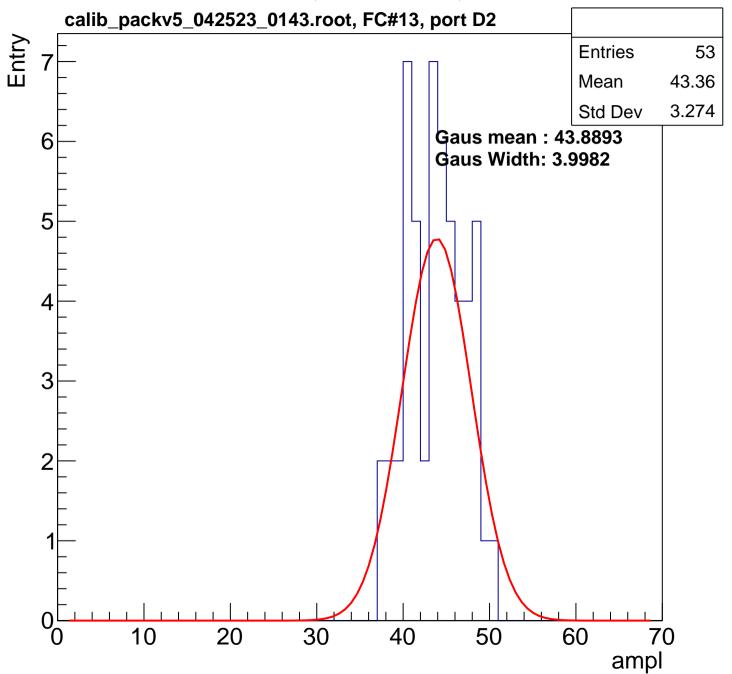


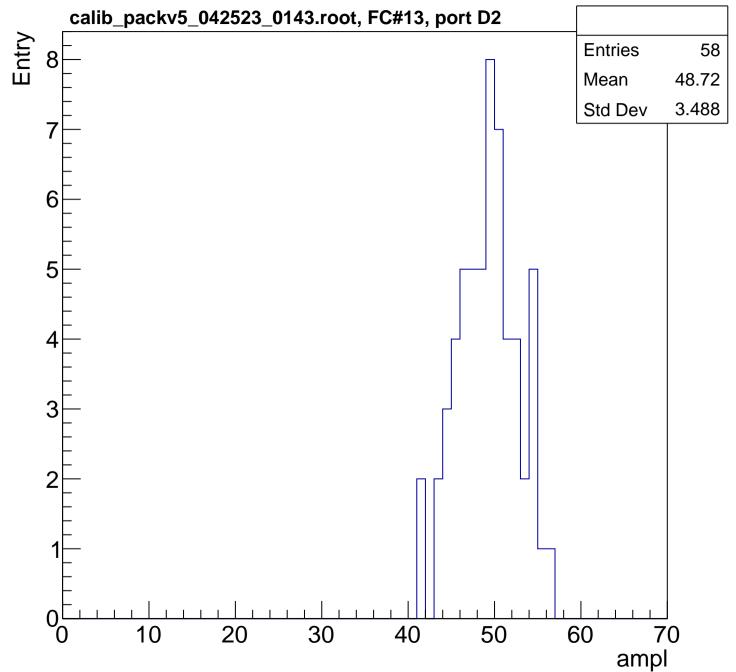


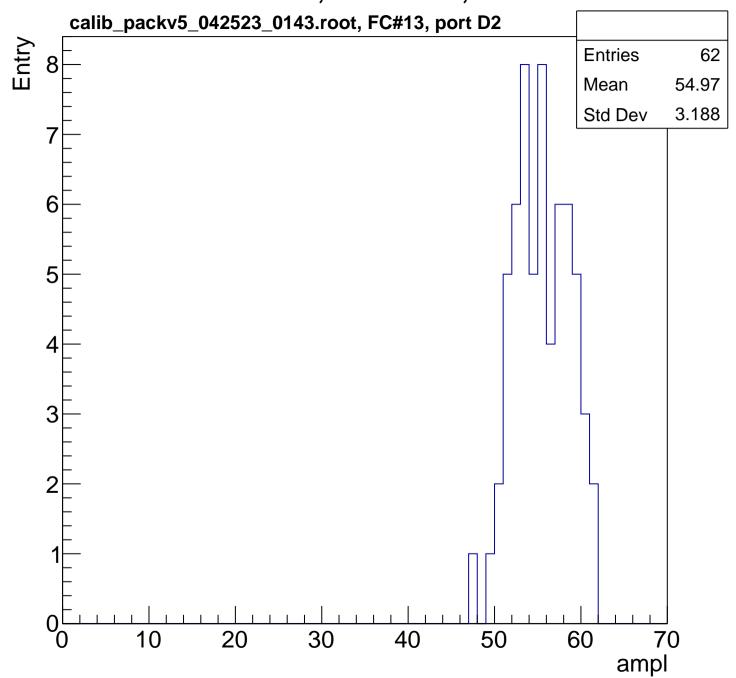


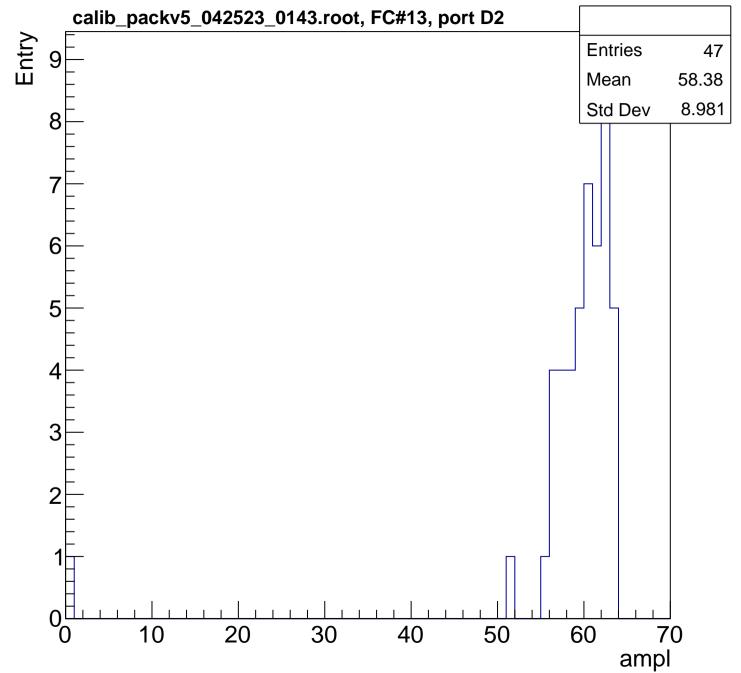


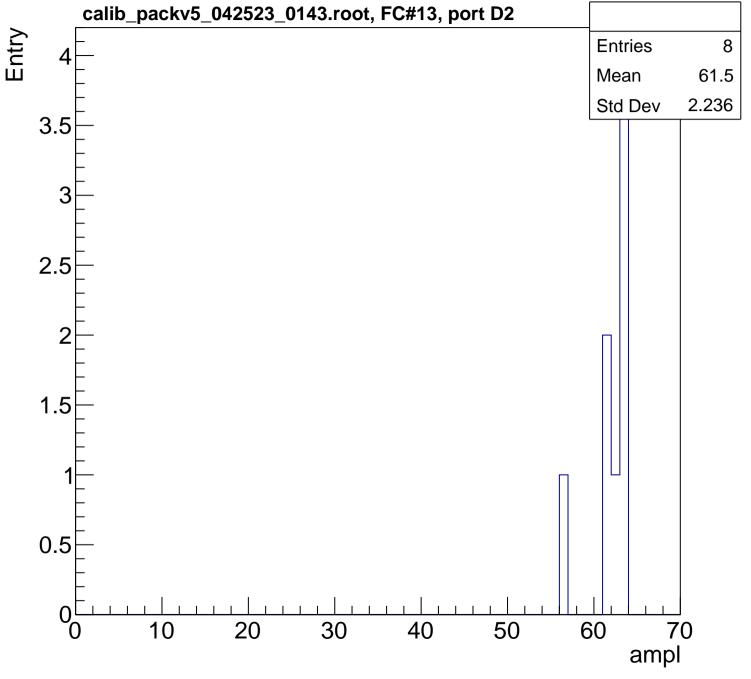


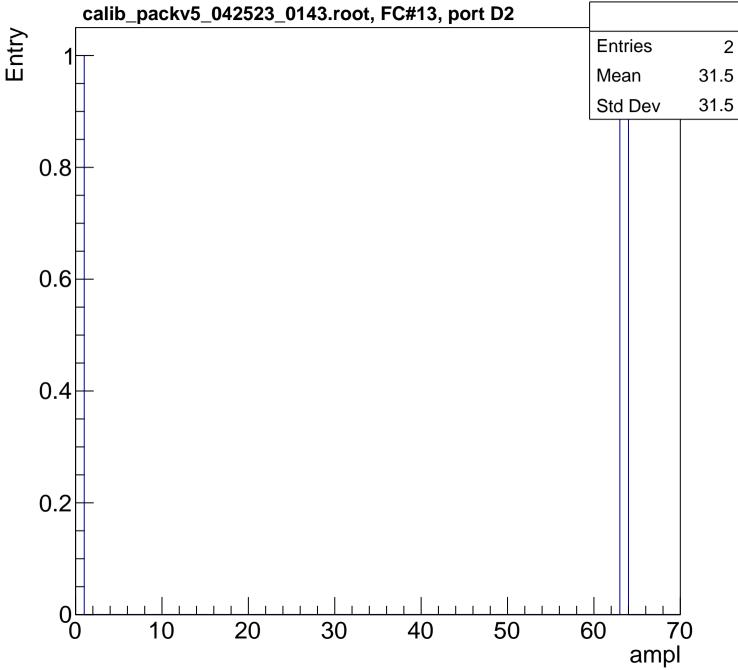


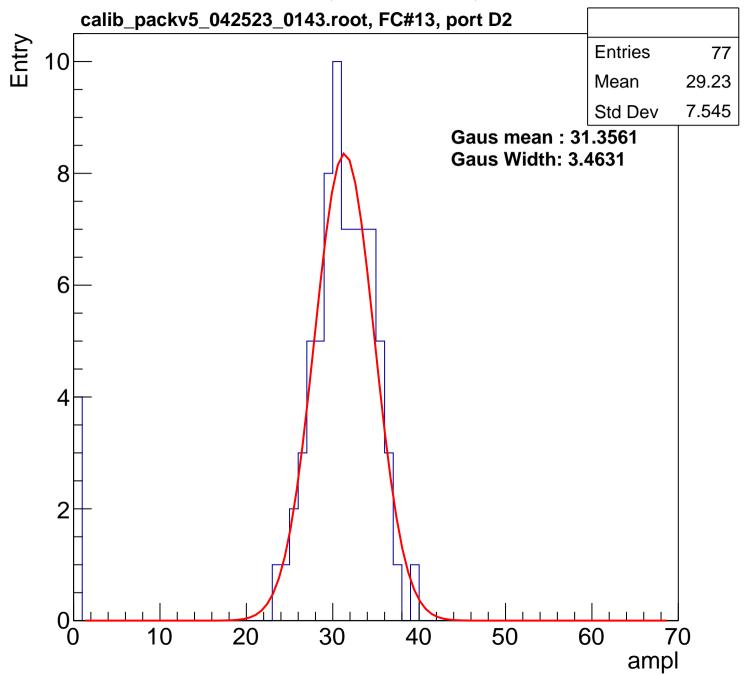


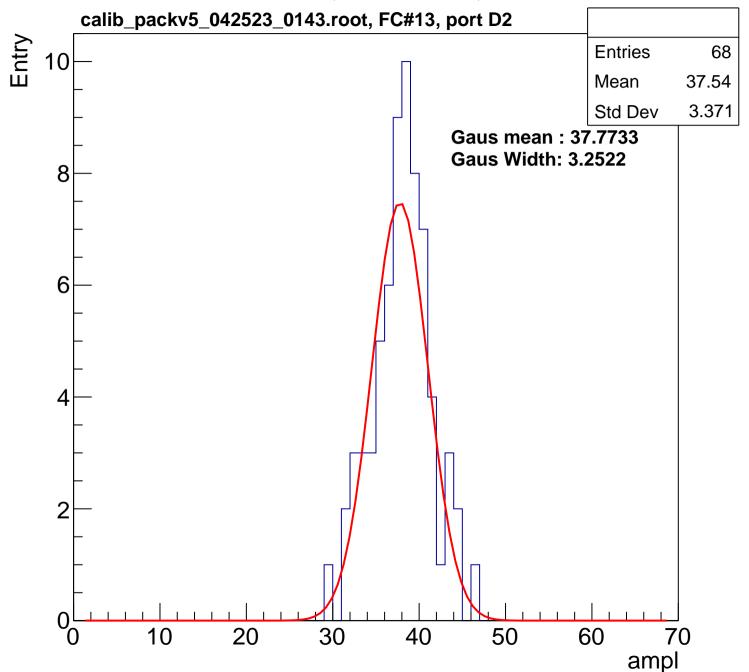


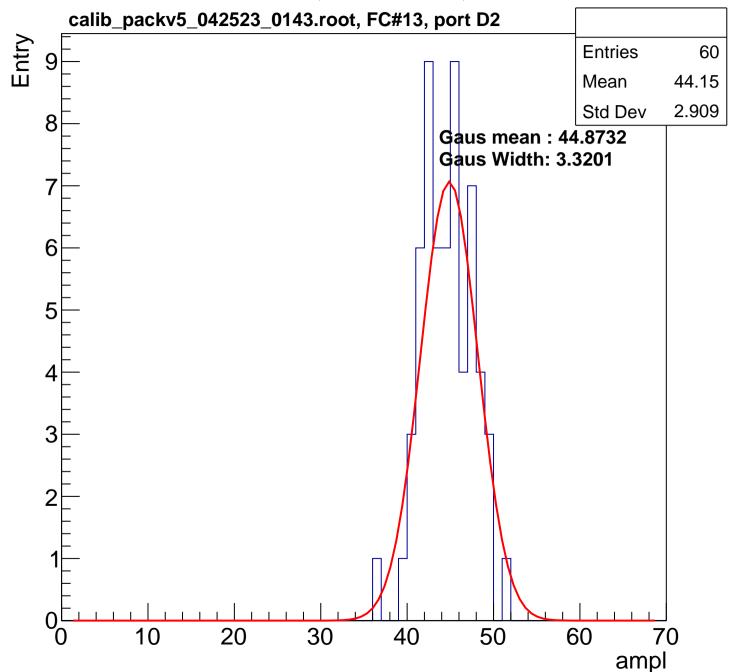


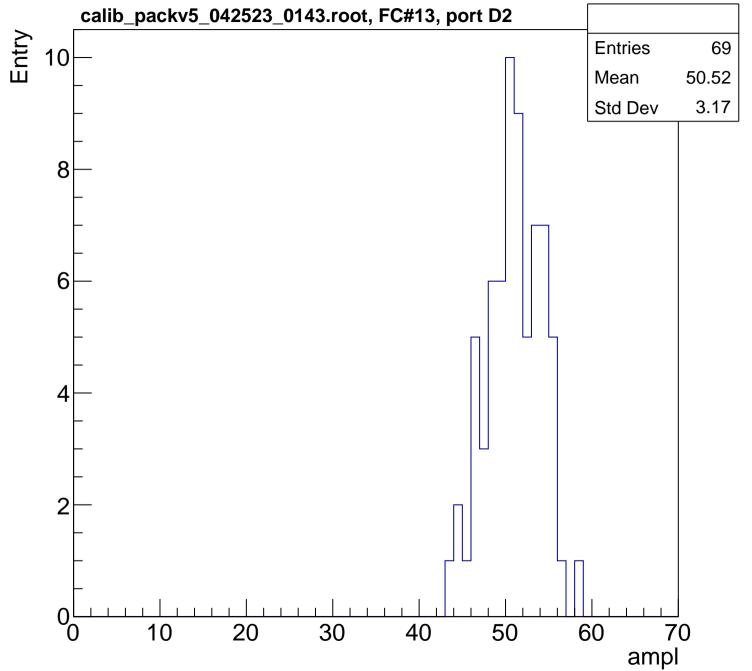


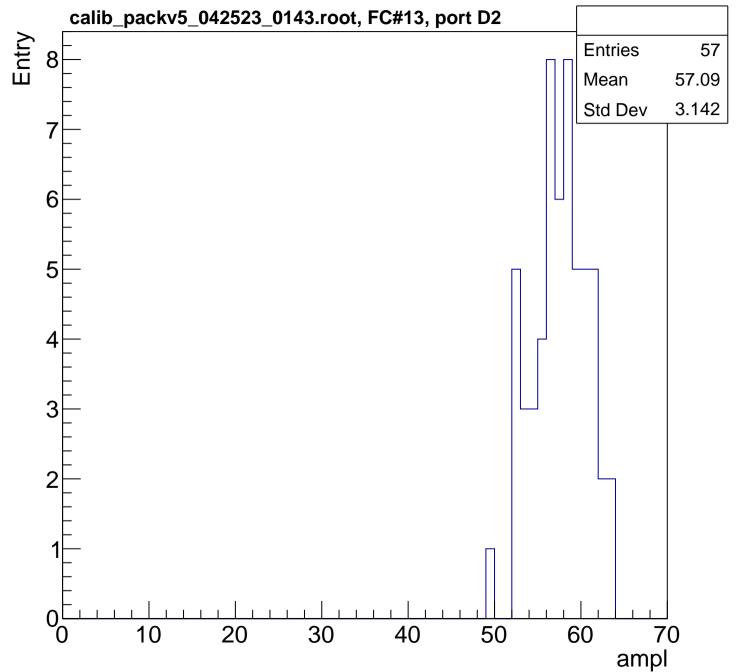


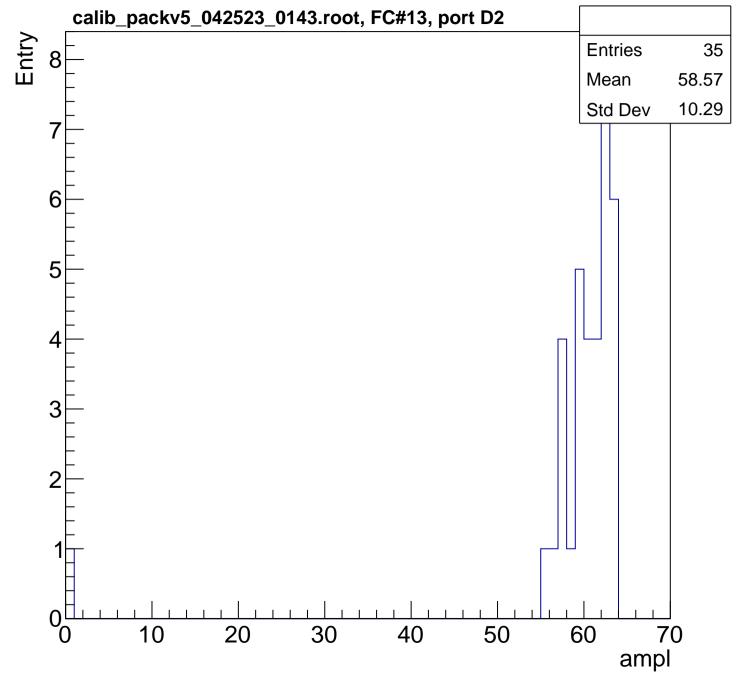


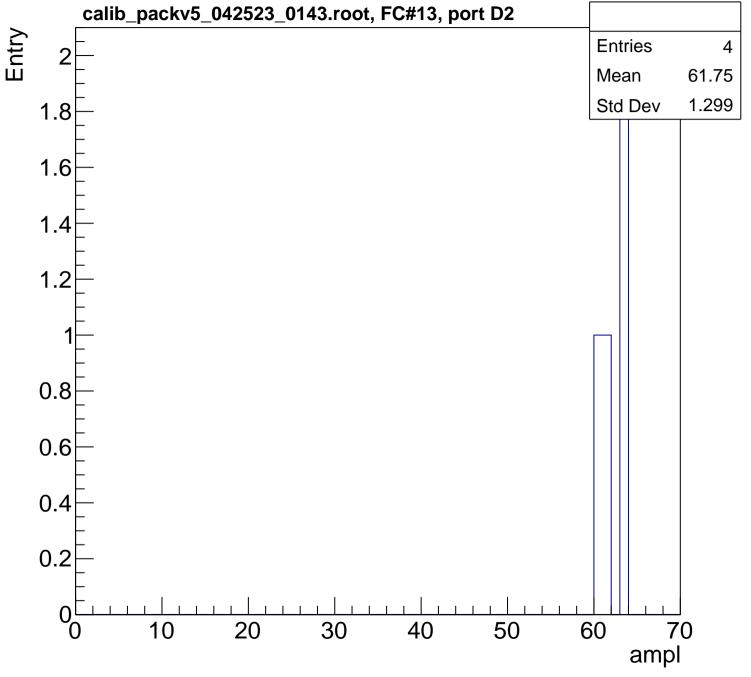




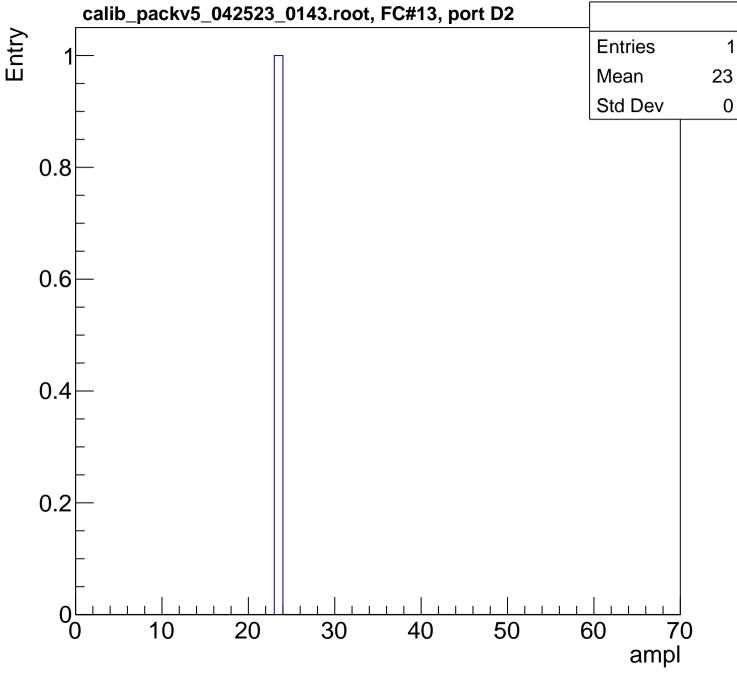


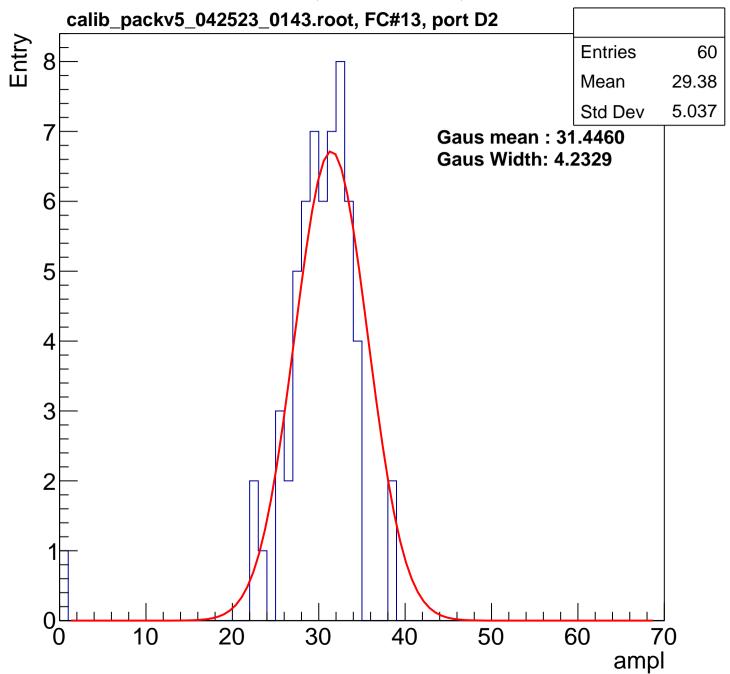


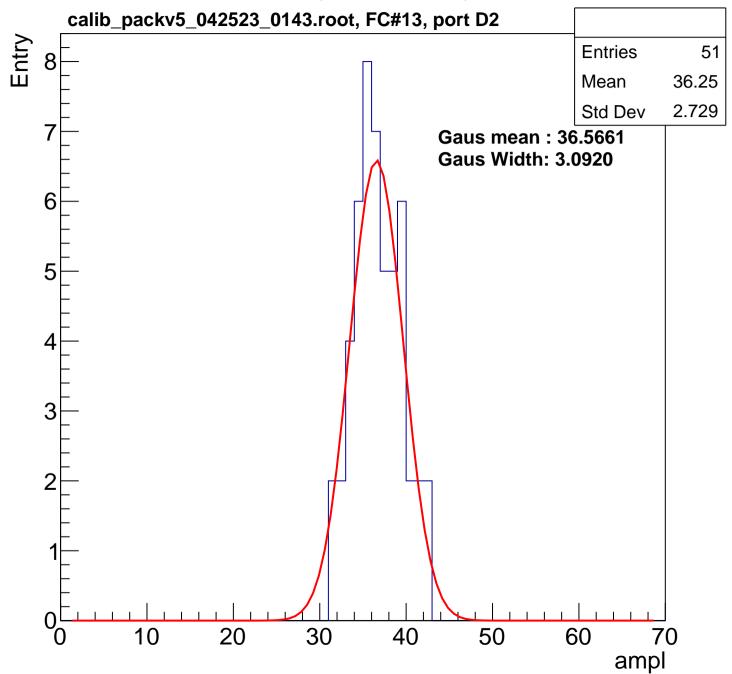


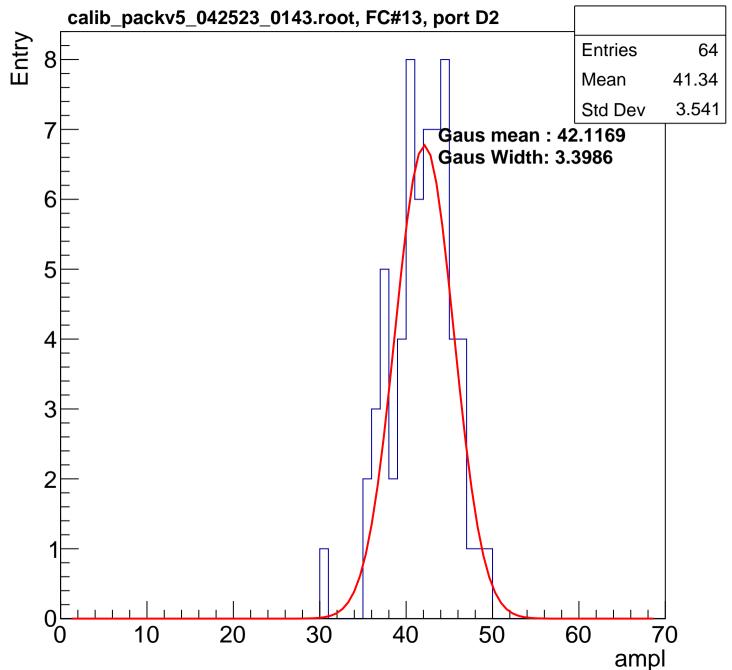


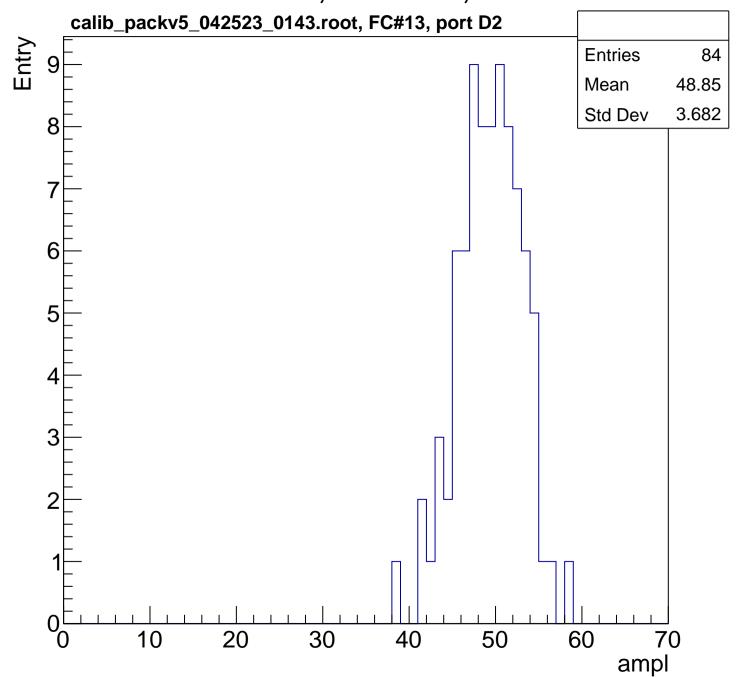
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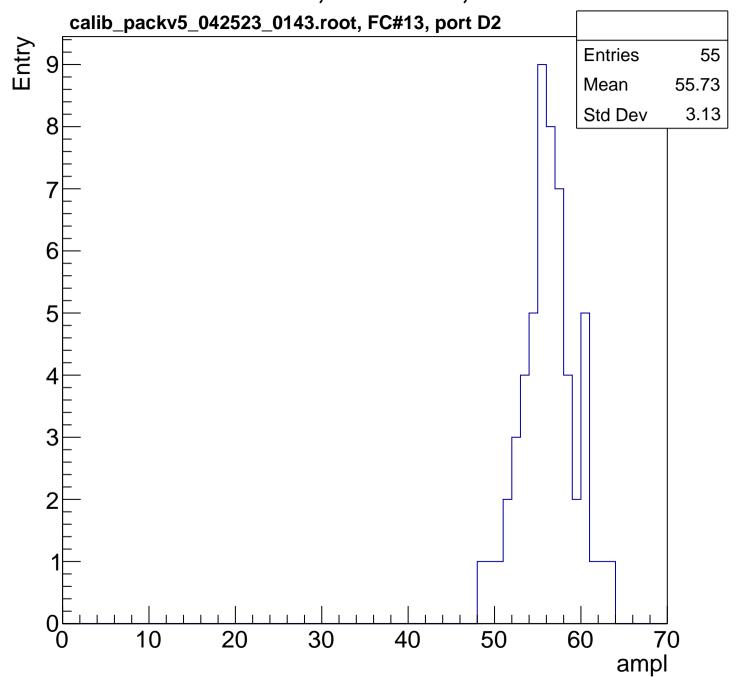


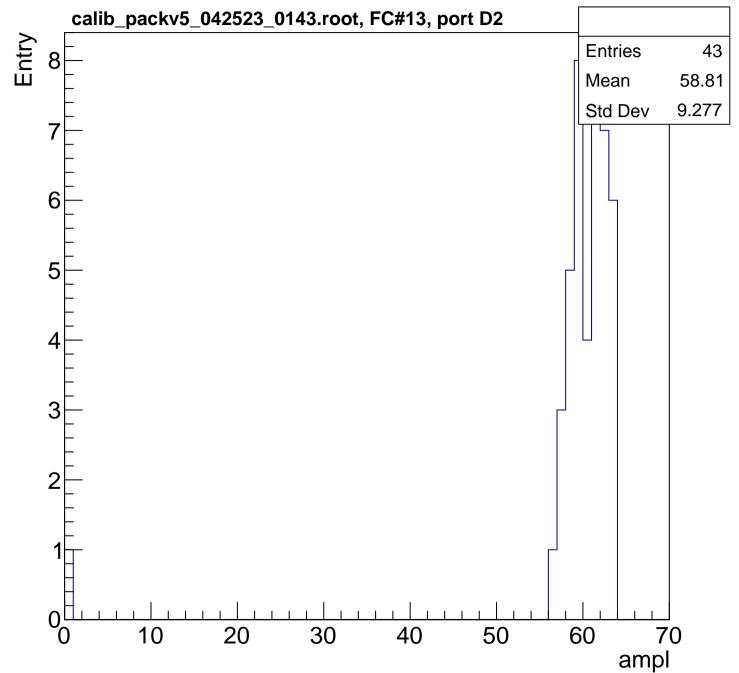


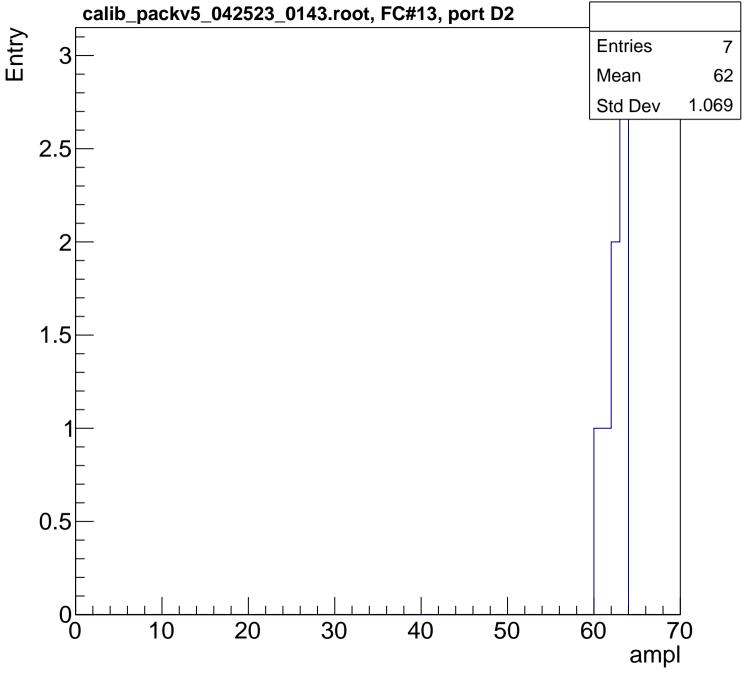


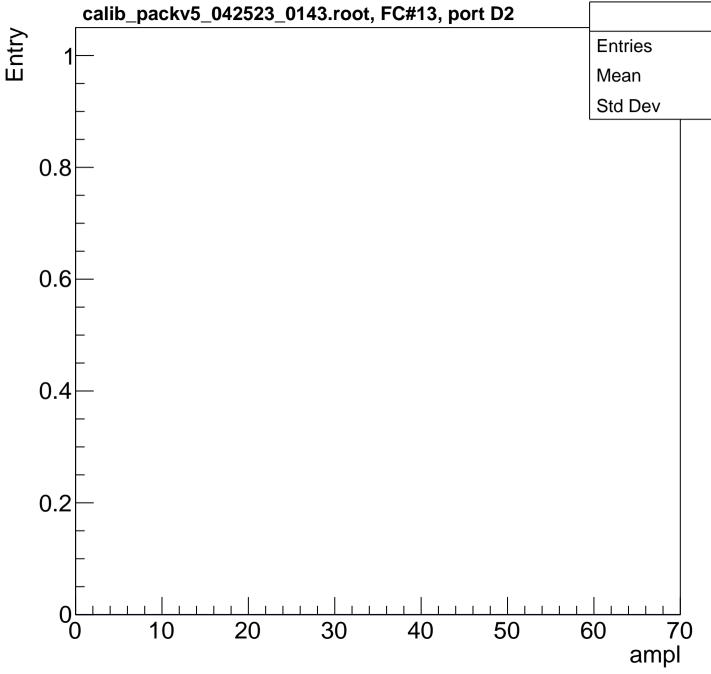


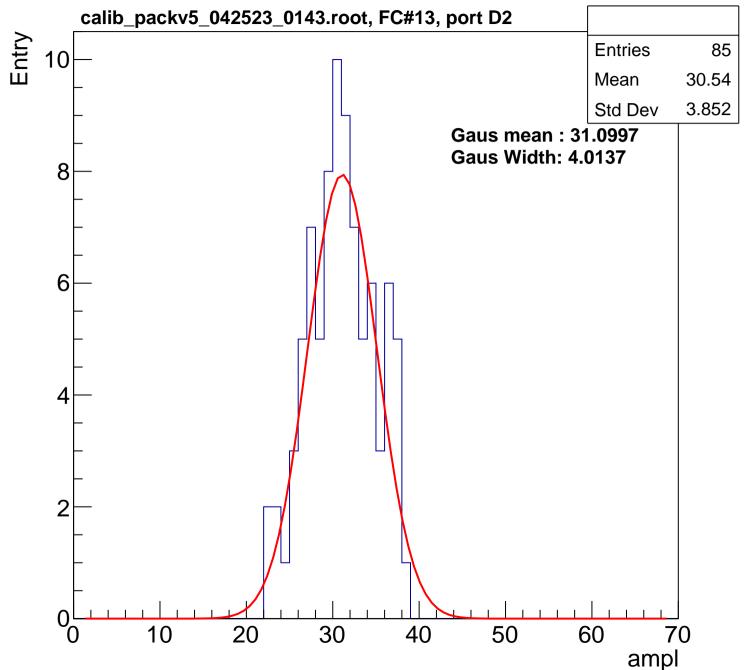


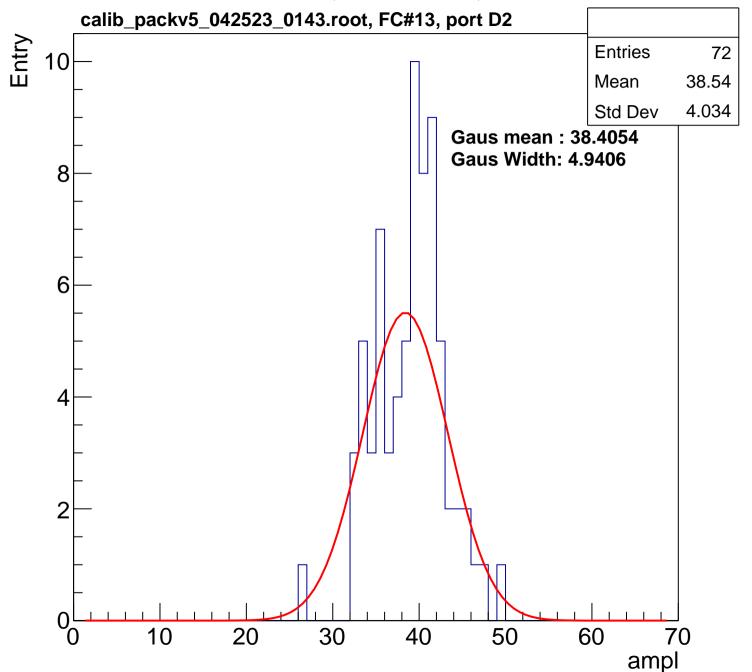


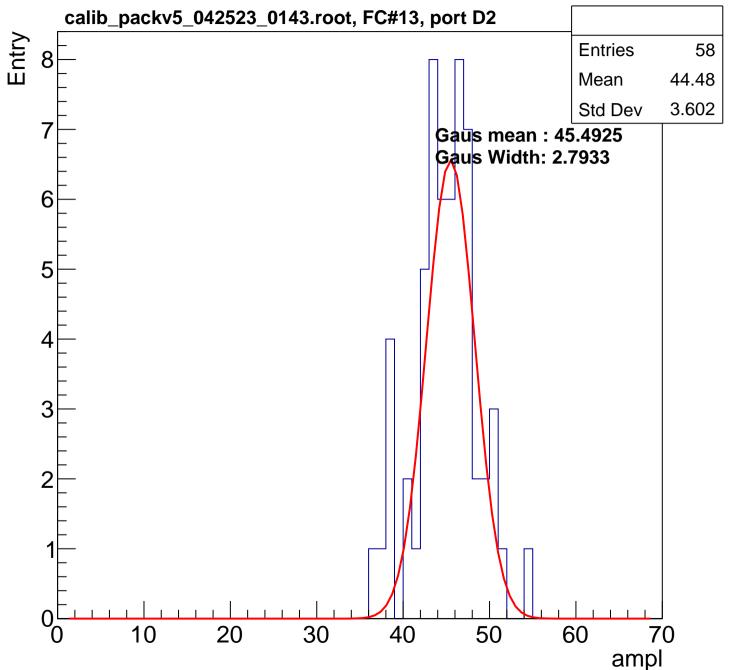


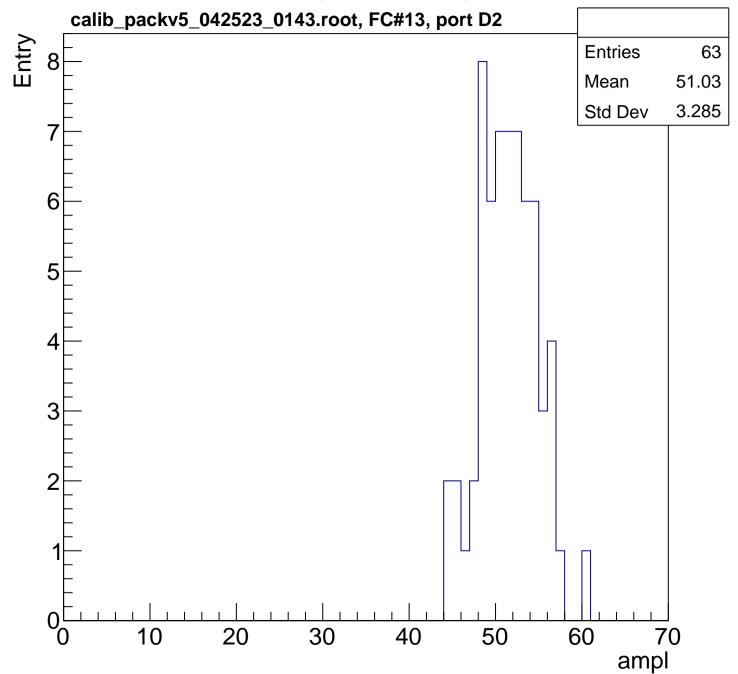


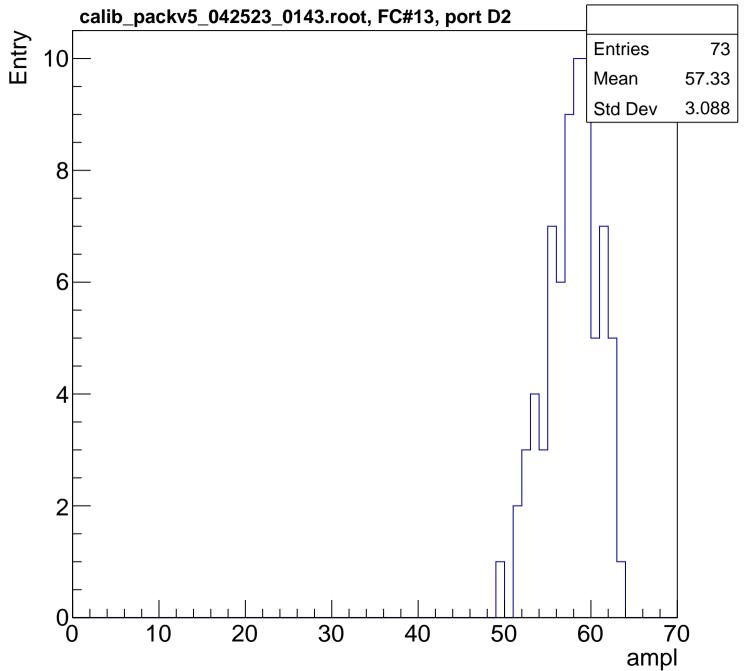


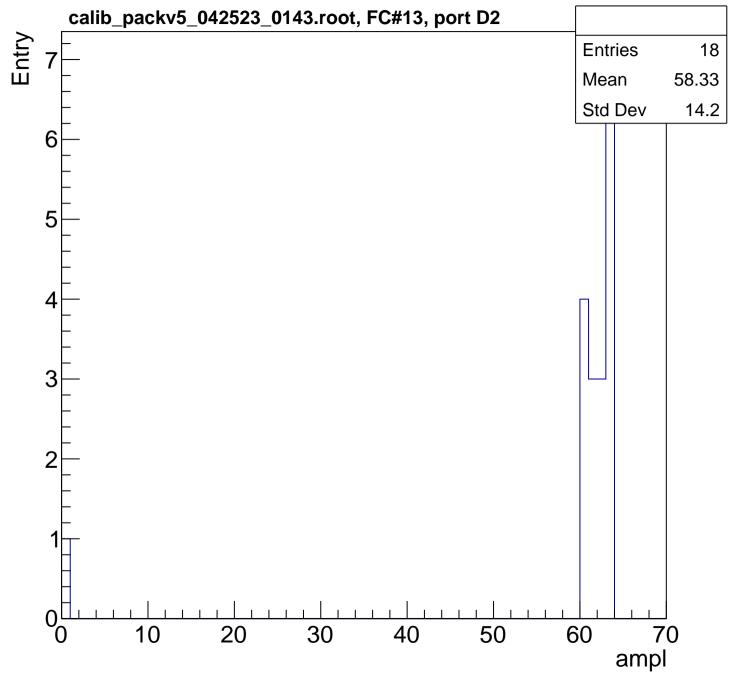


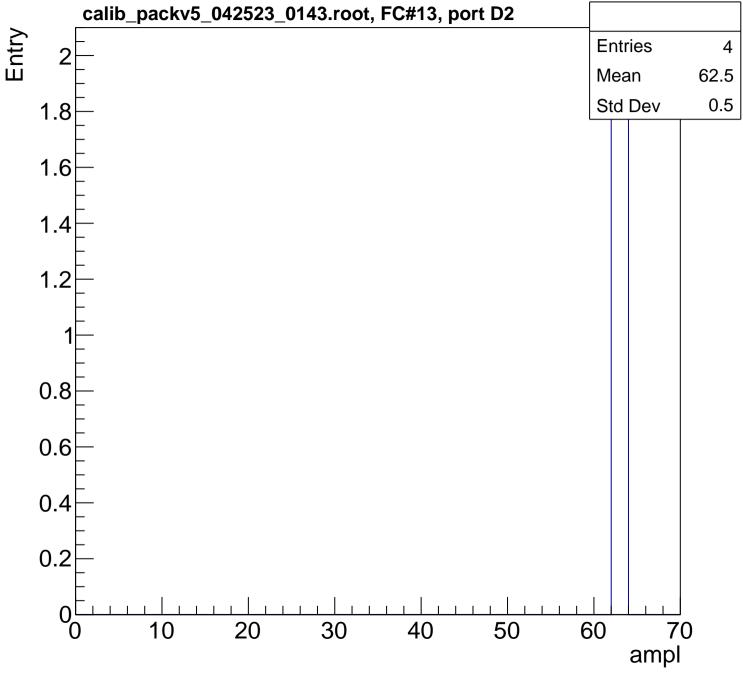




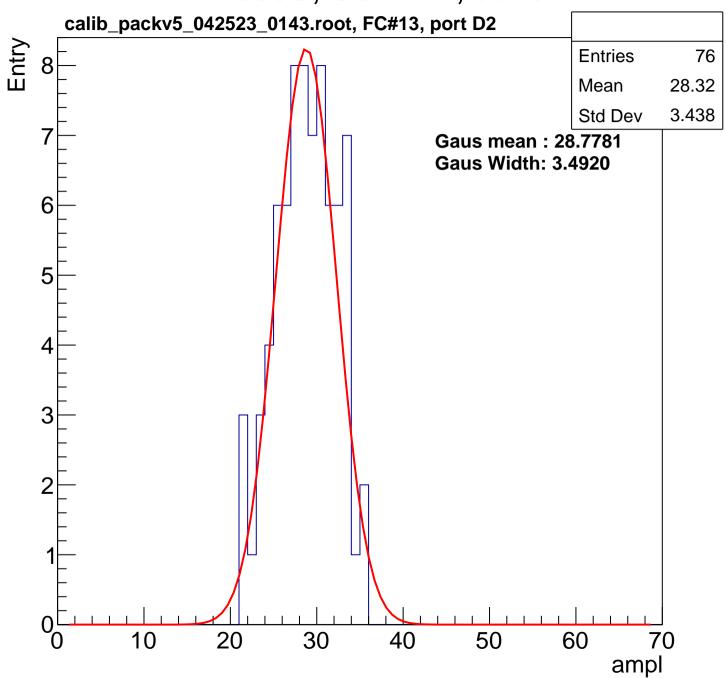


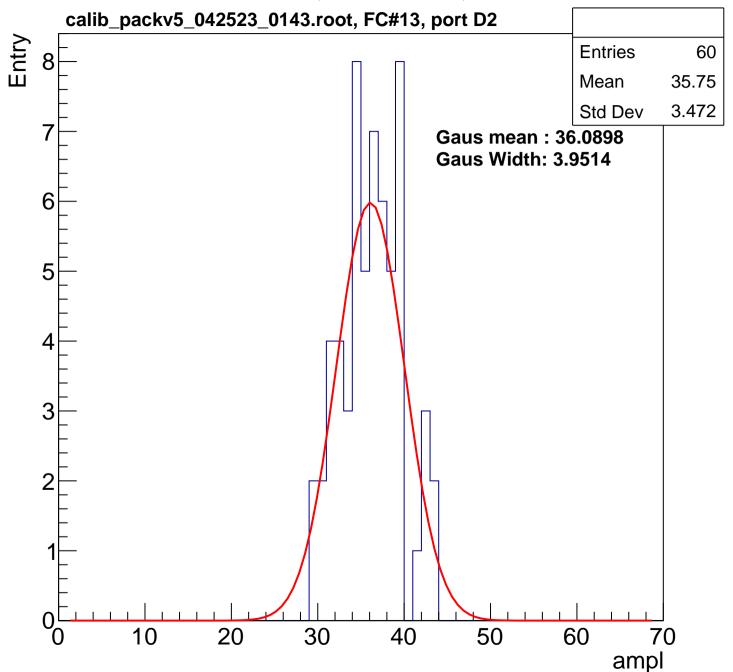


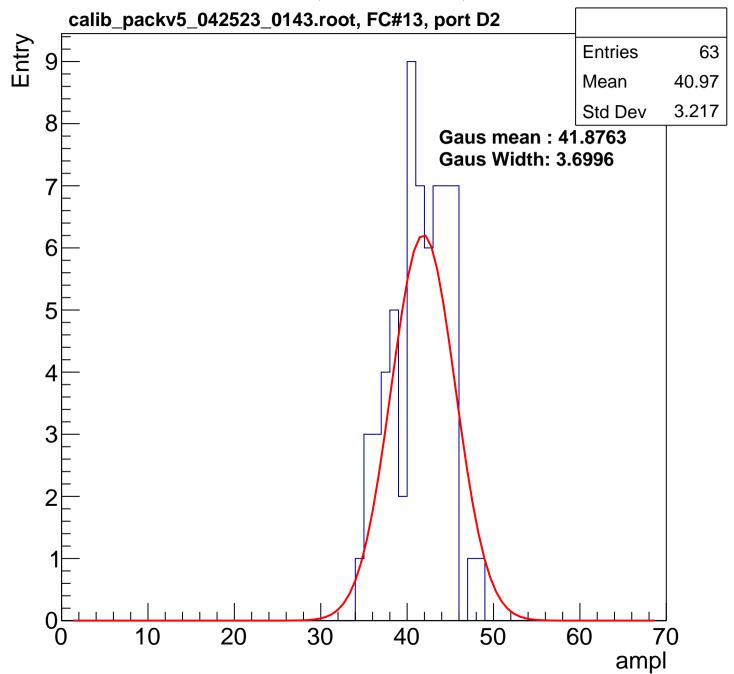


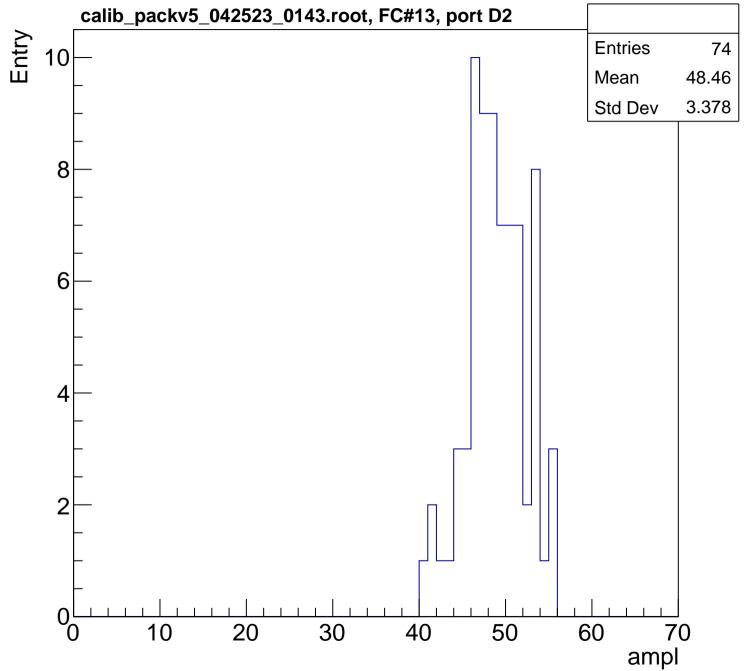


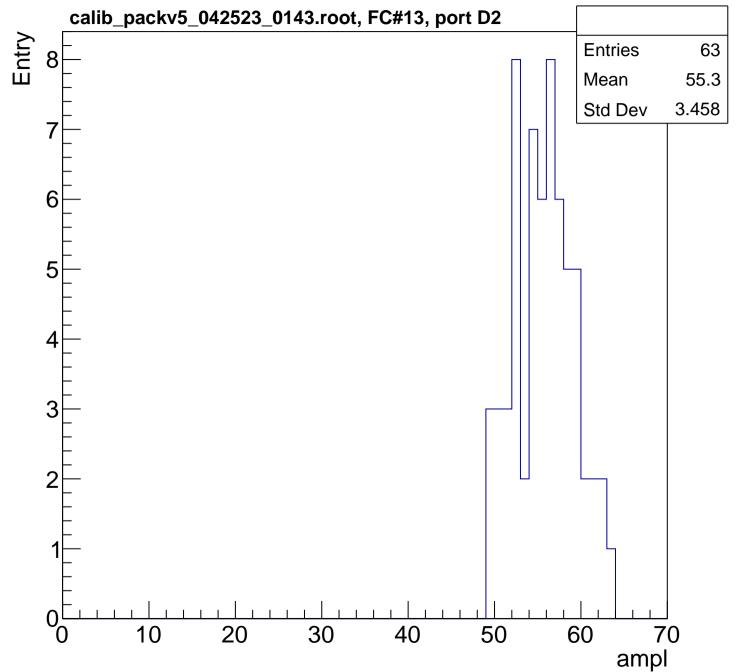


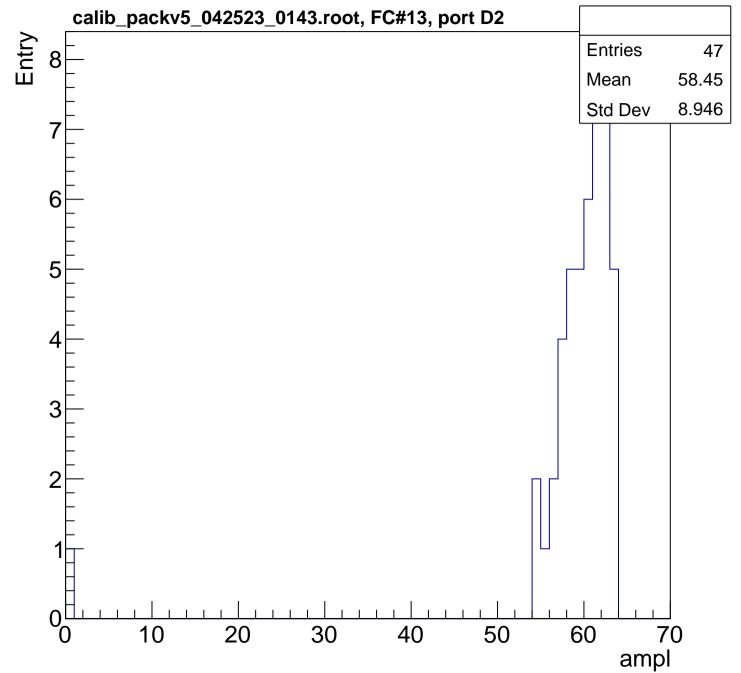


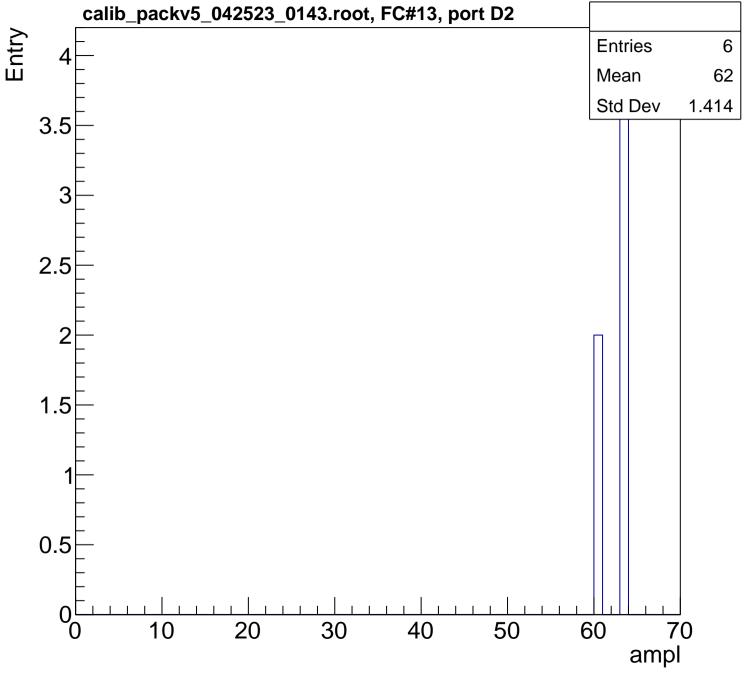




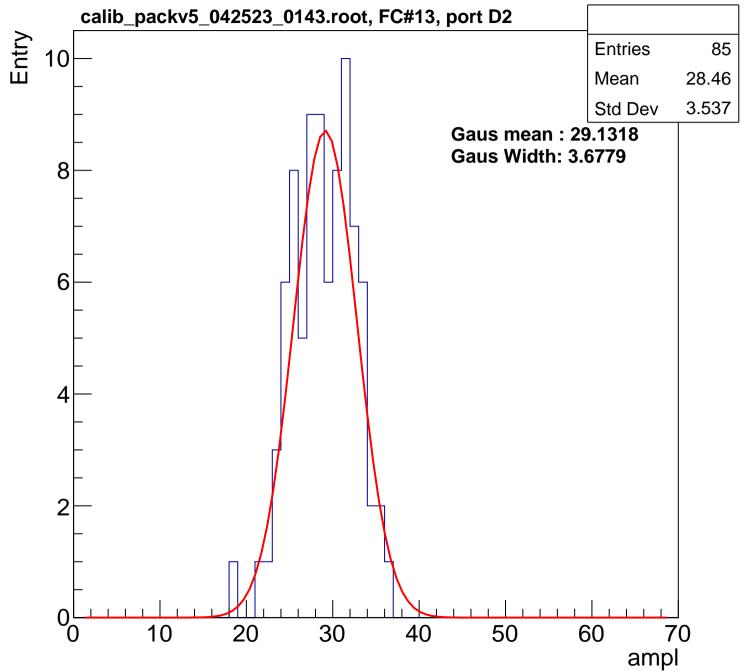


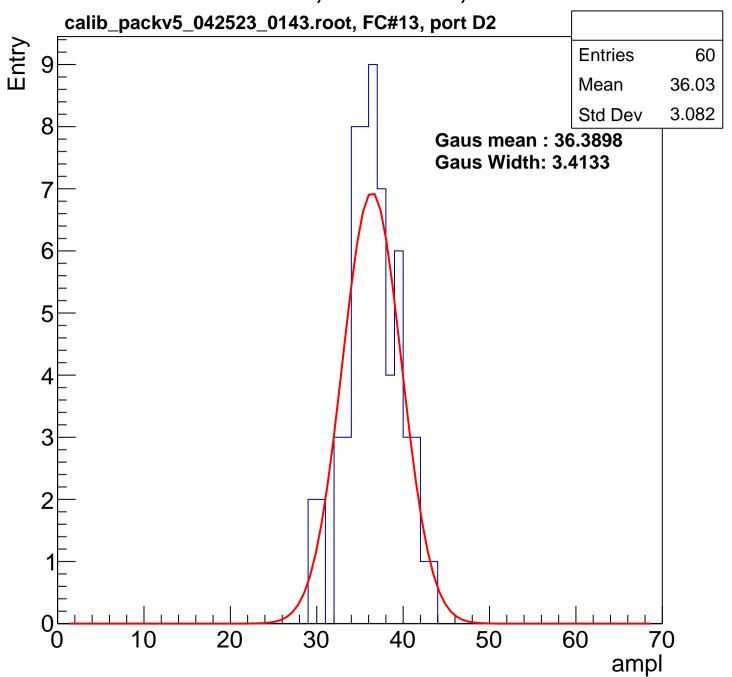


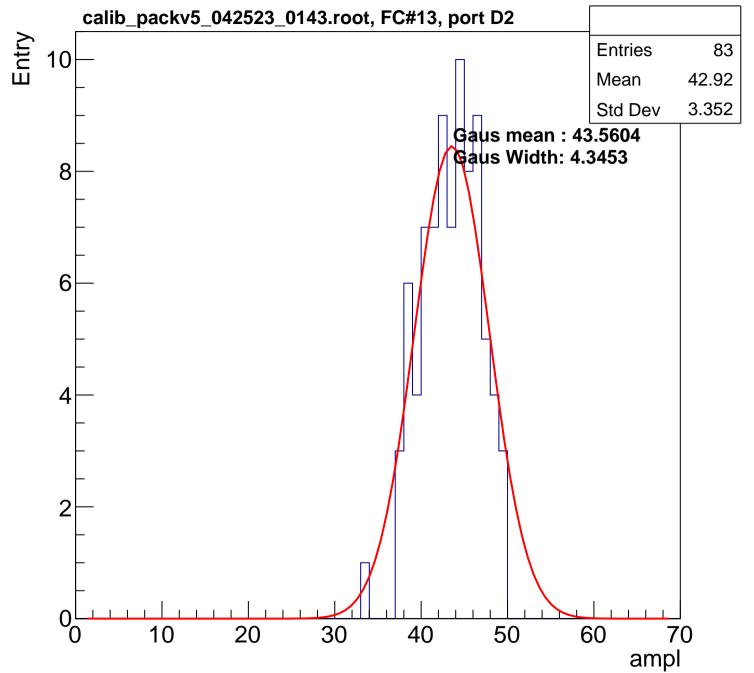


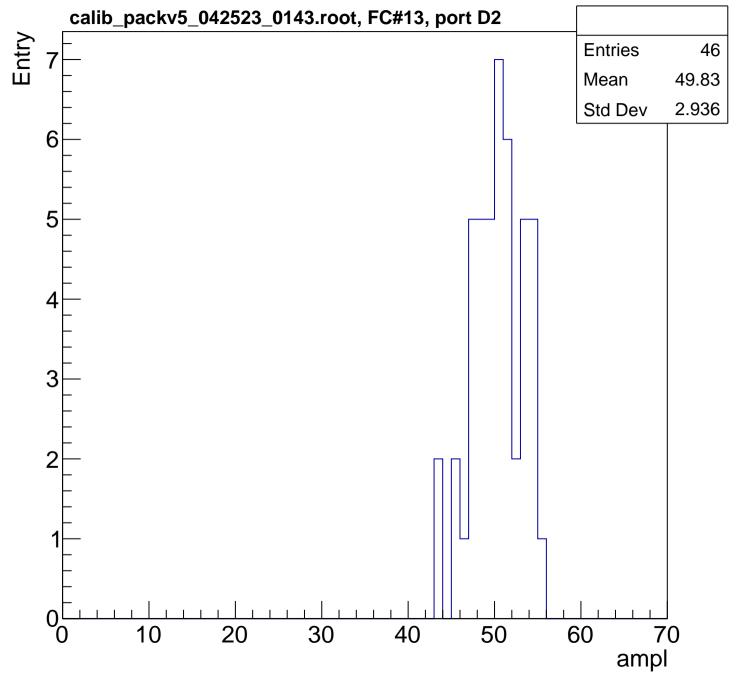


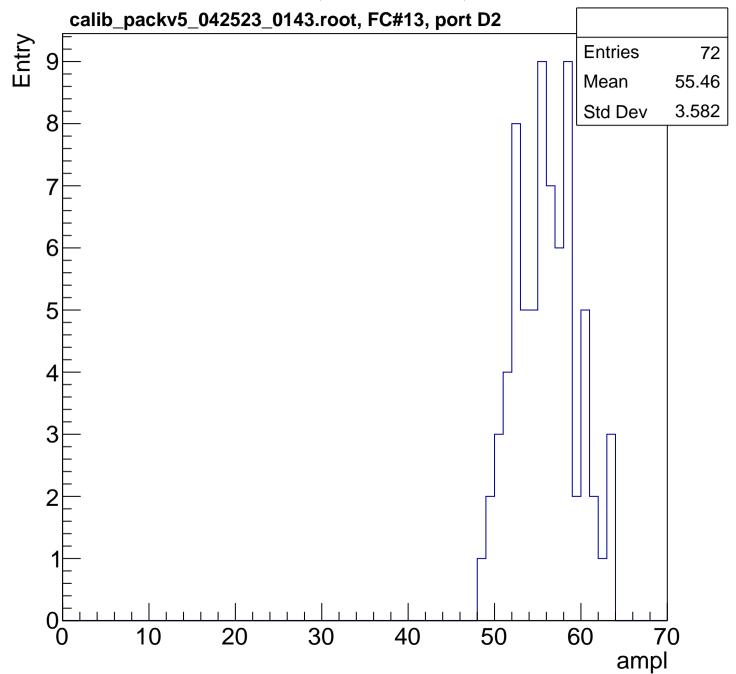
B1L003S, U9-ch74, adc7 calib\_packv5\_042523\_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

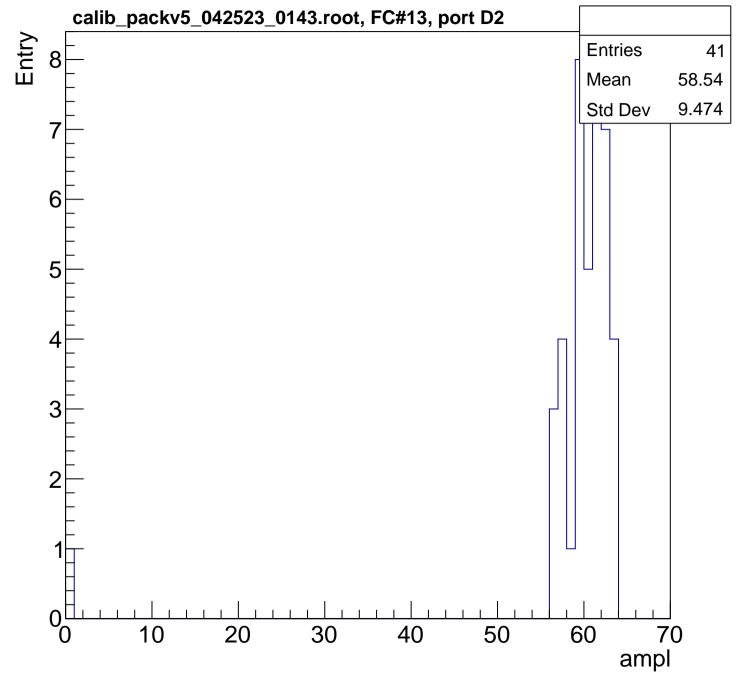


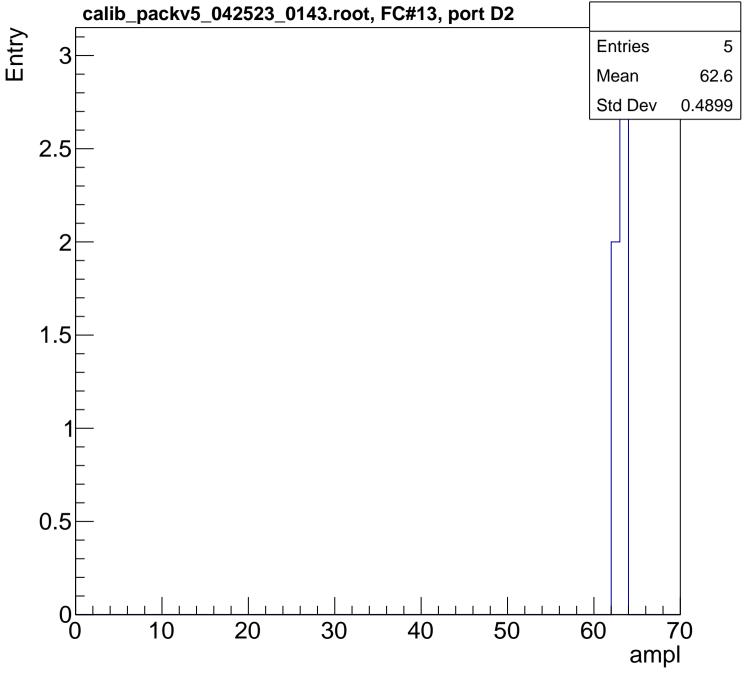




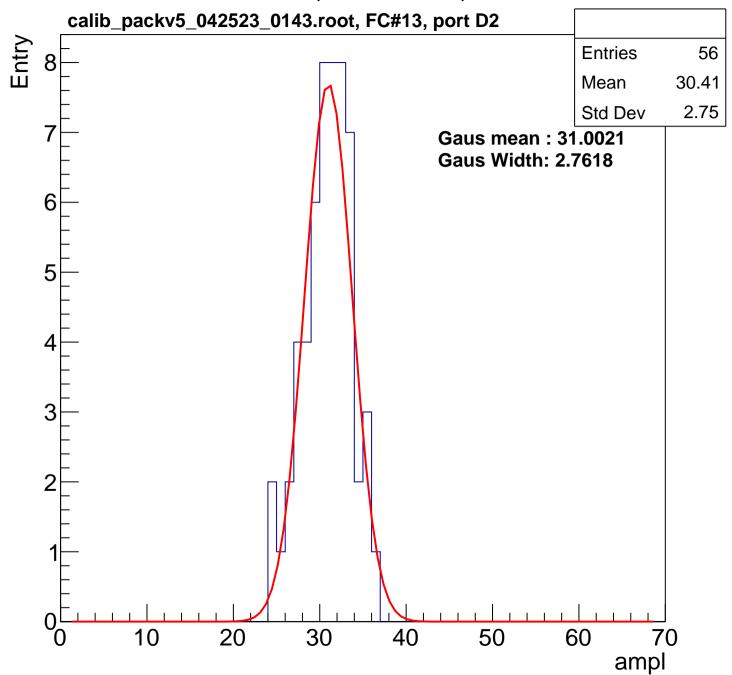


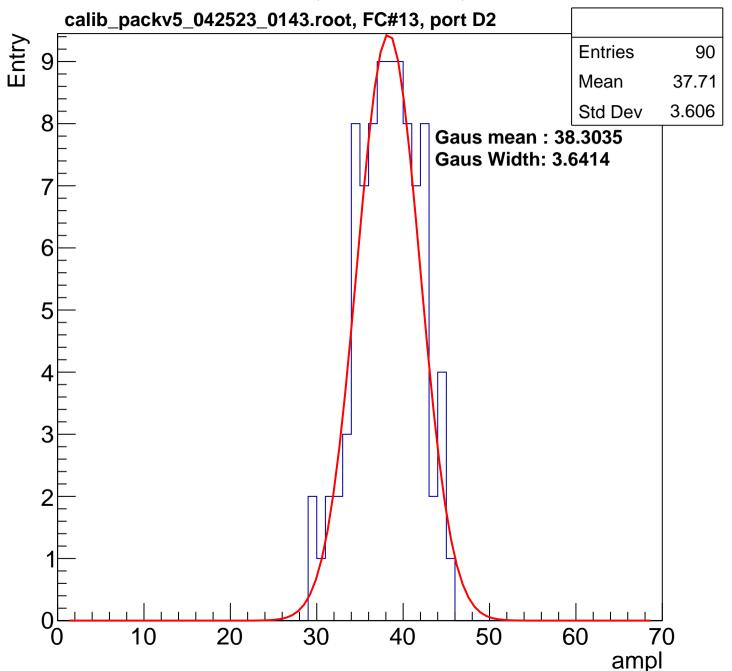


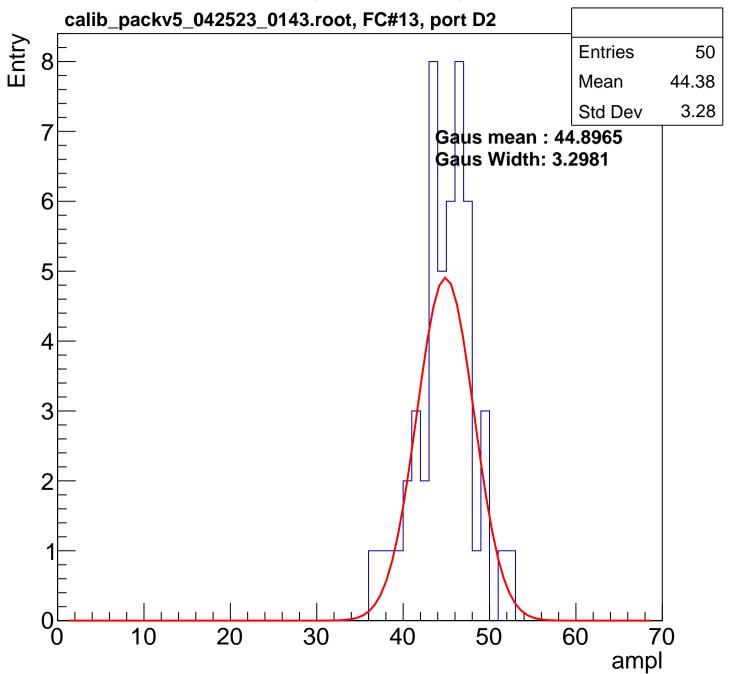


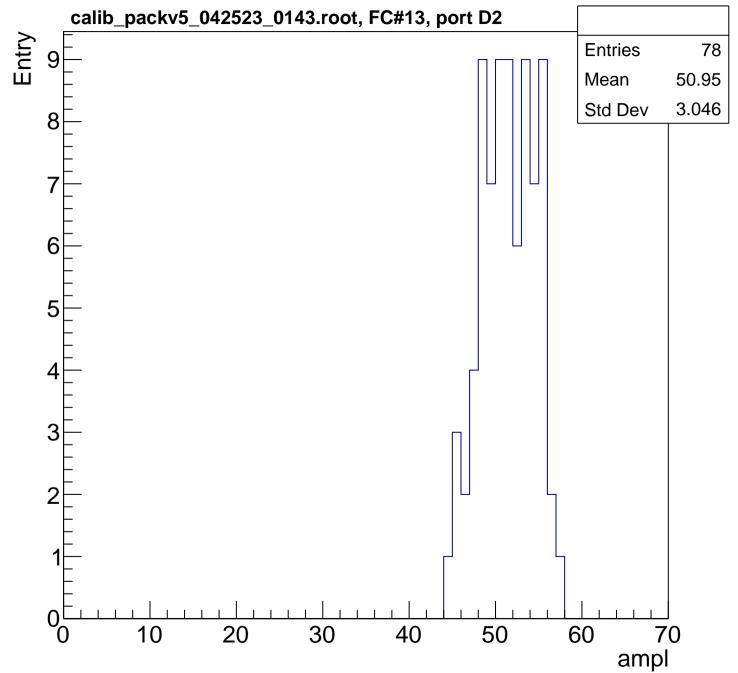


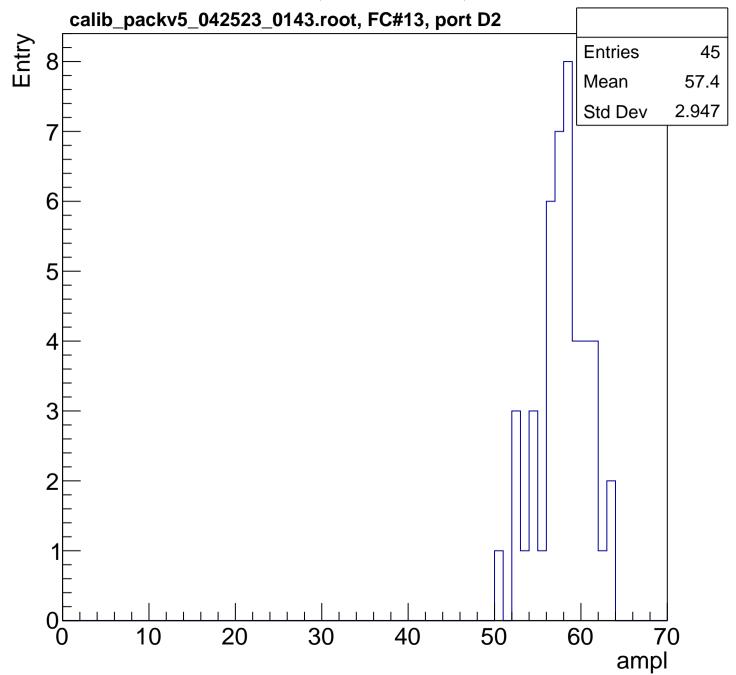


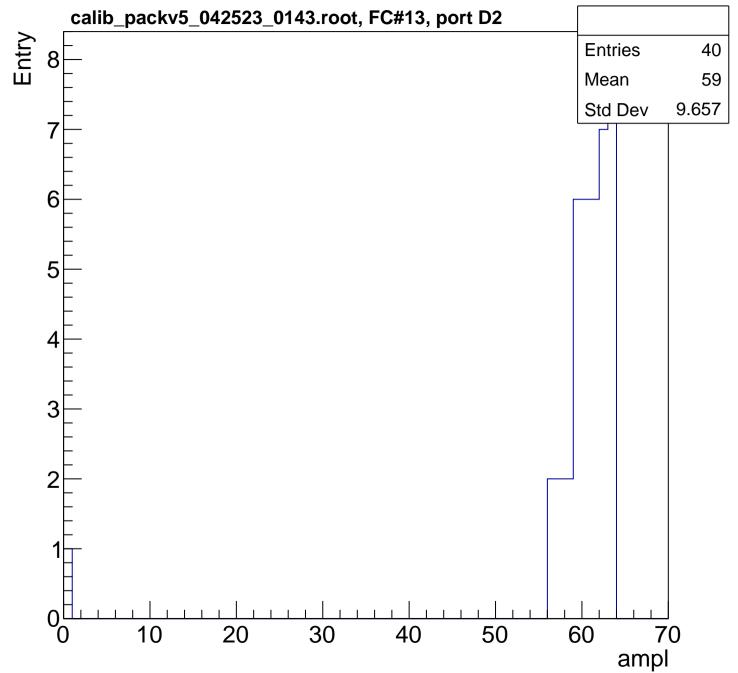


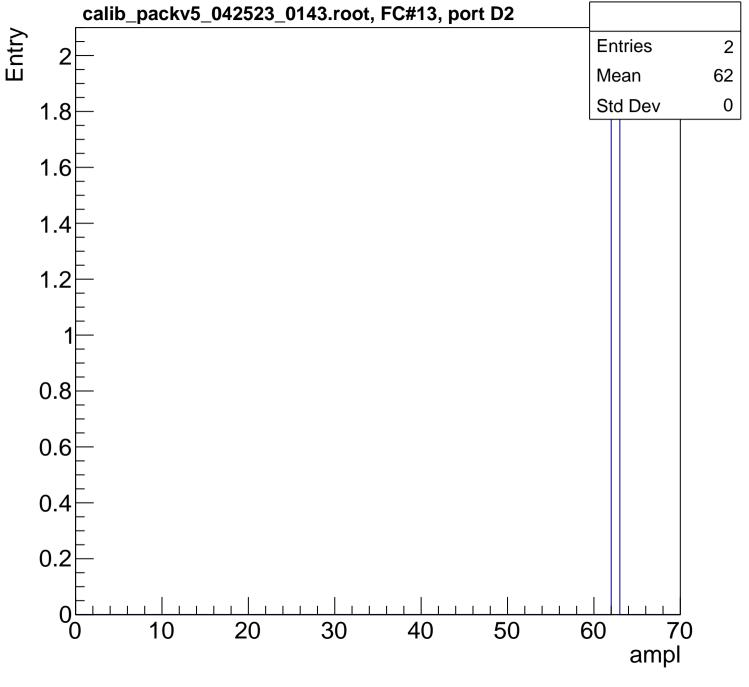




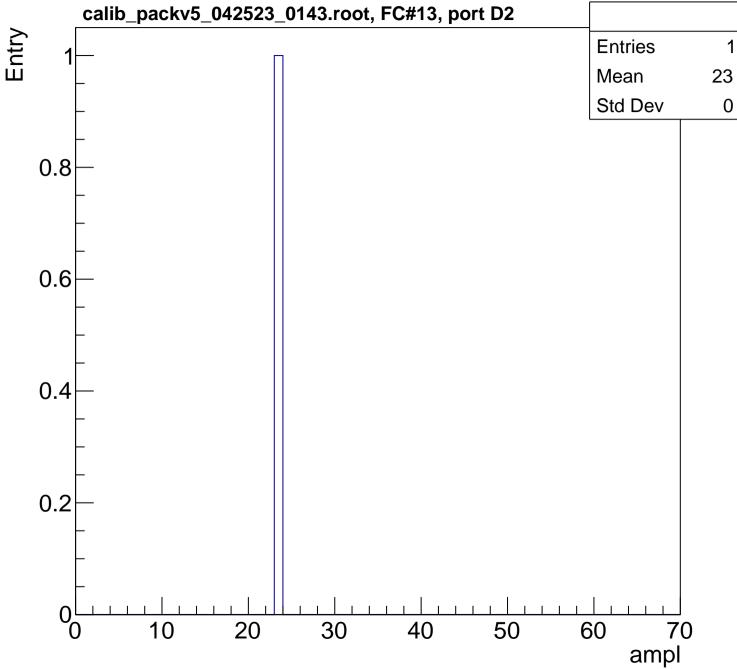


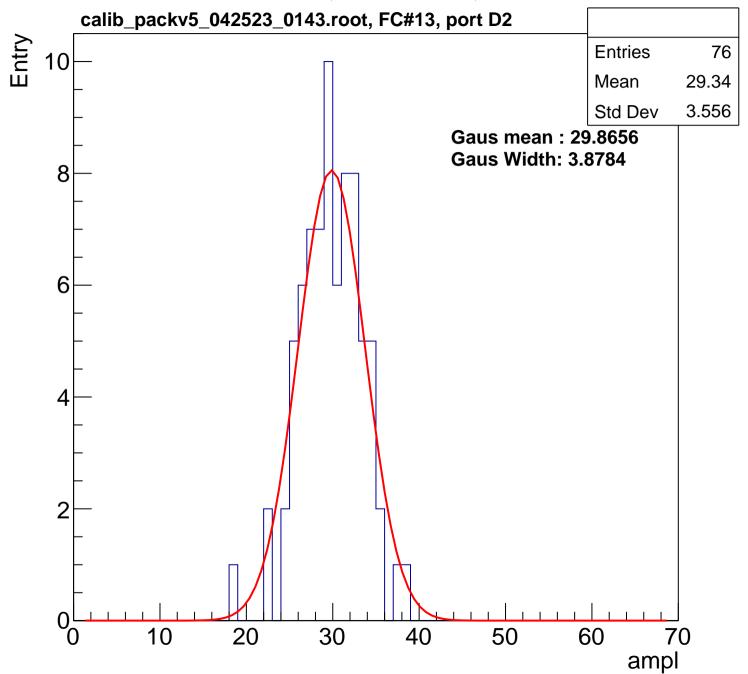


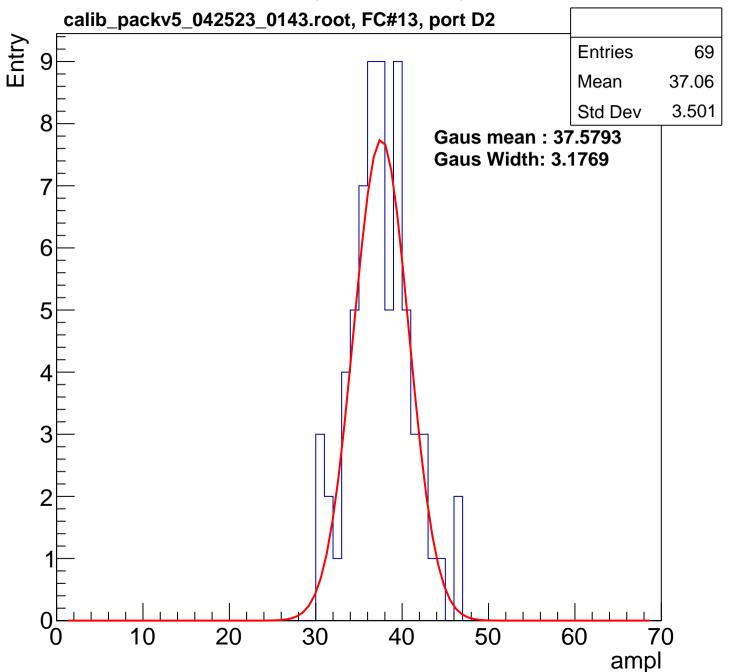


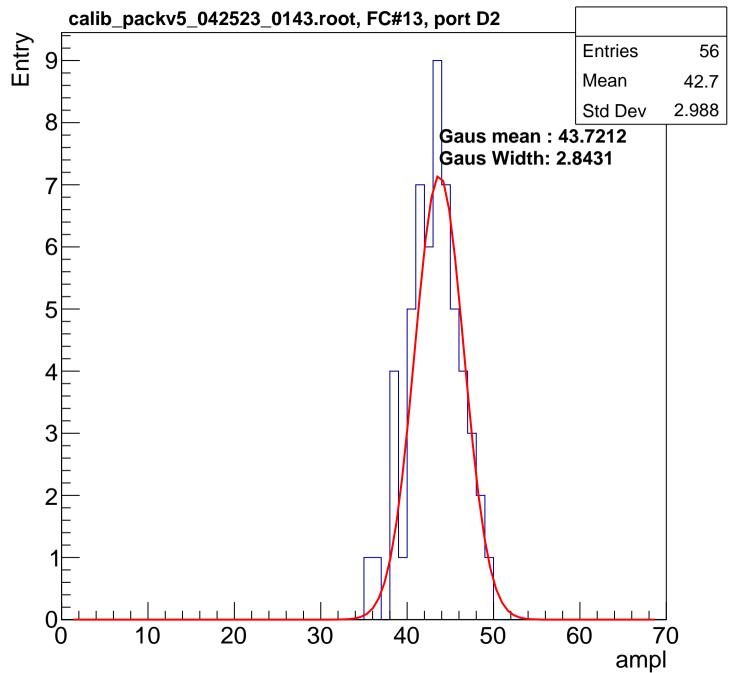


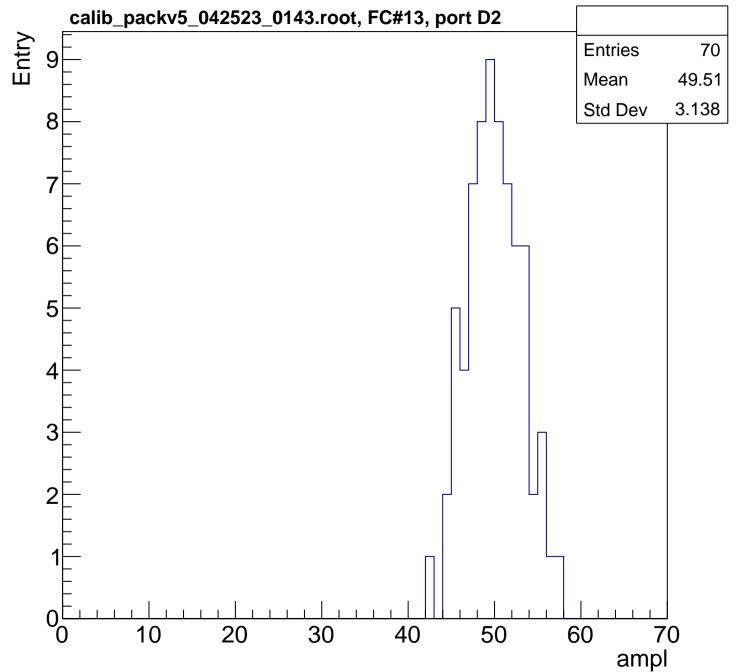
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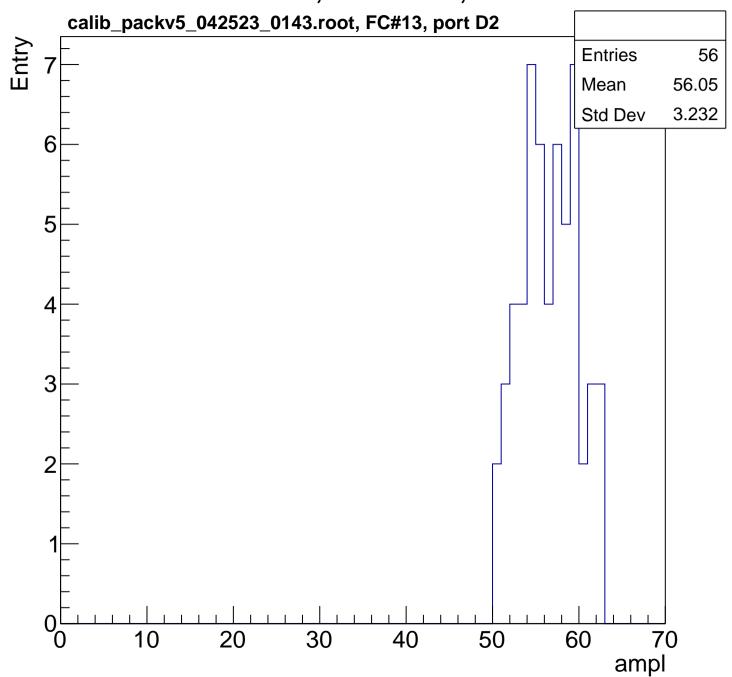


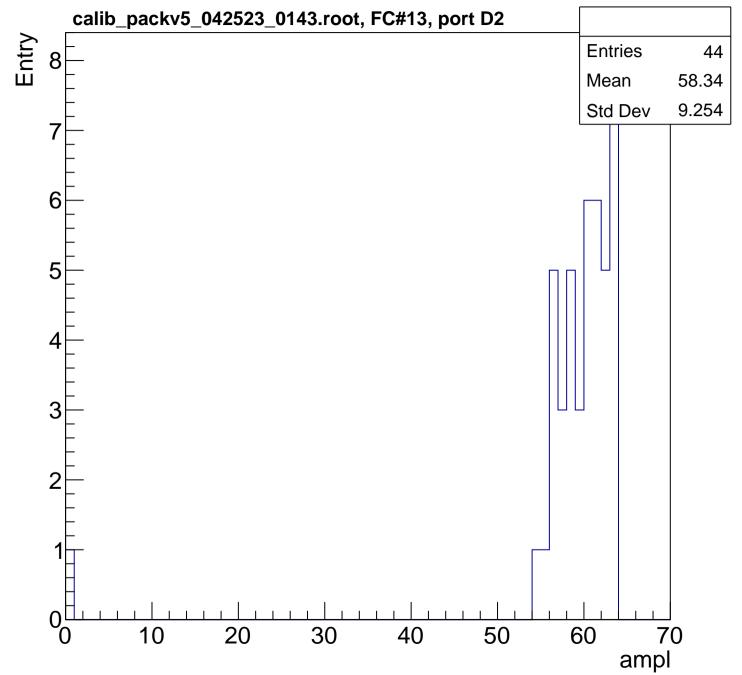


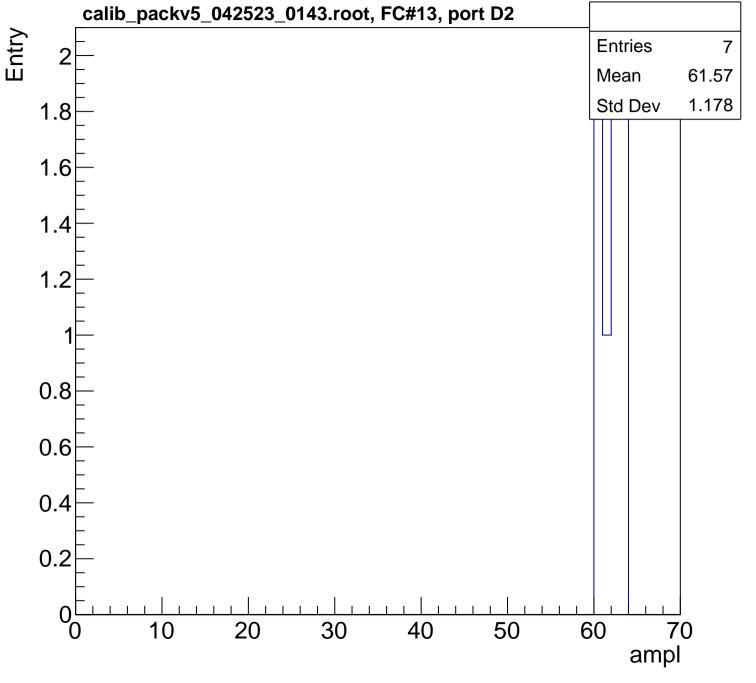


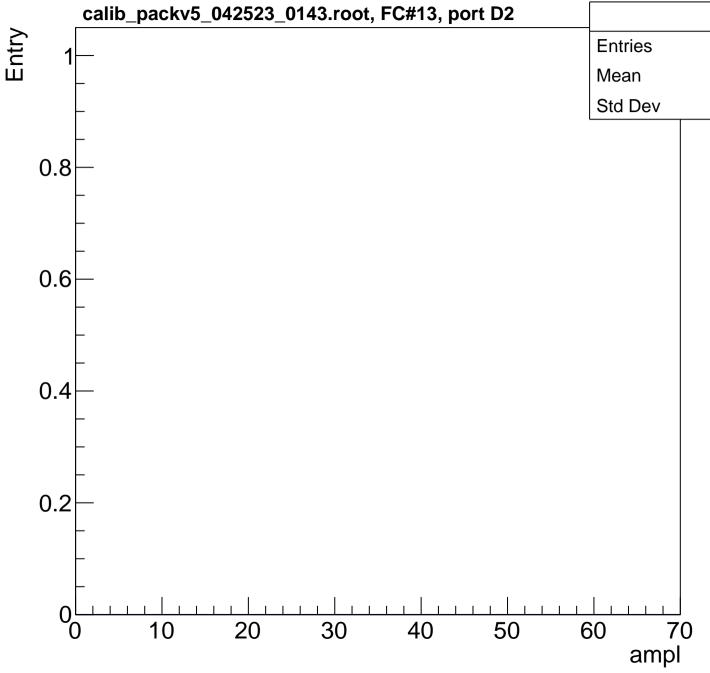


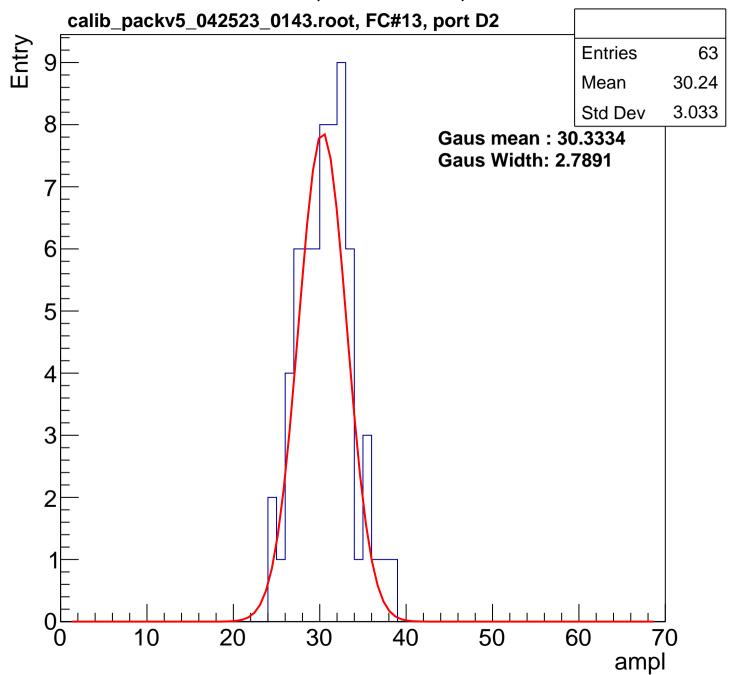


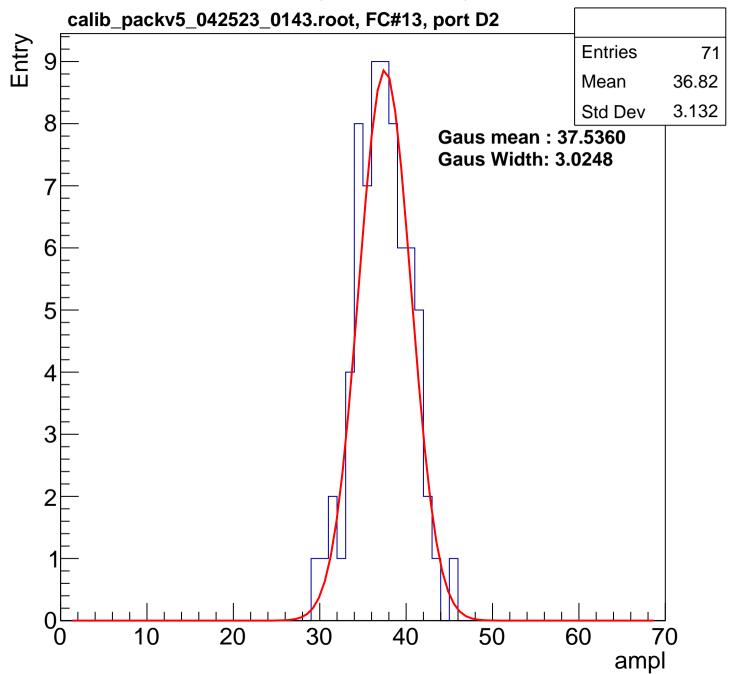


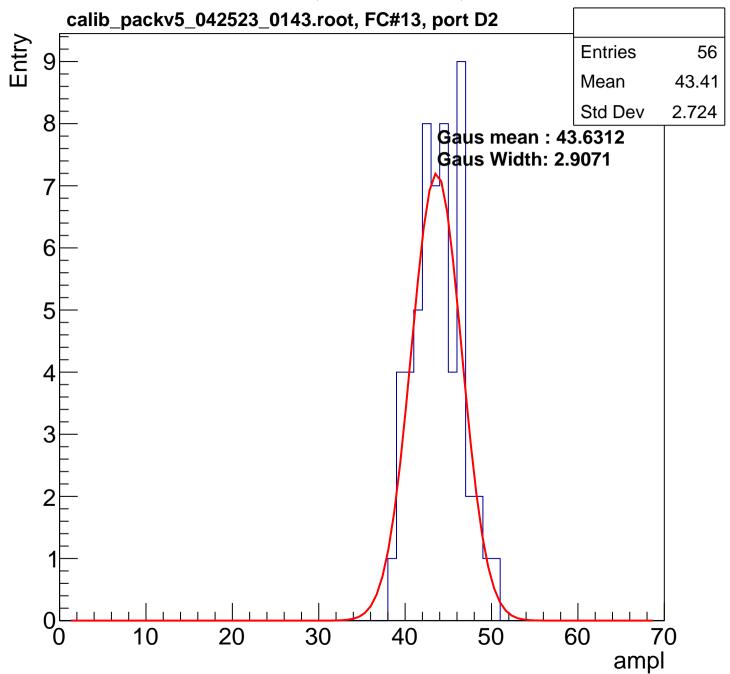


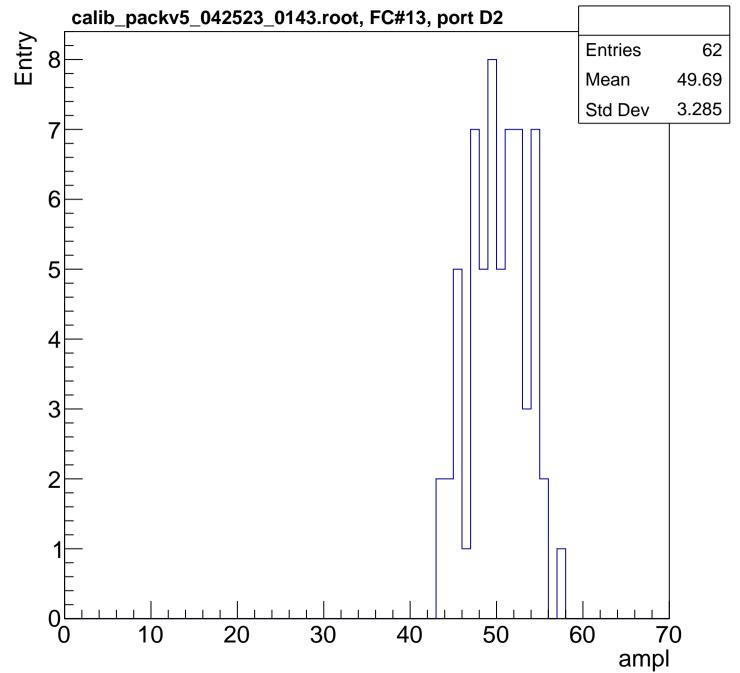


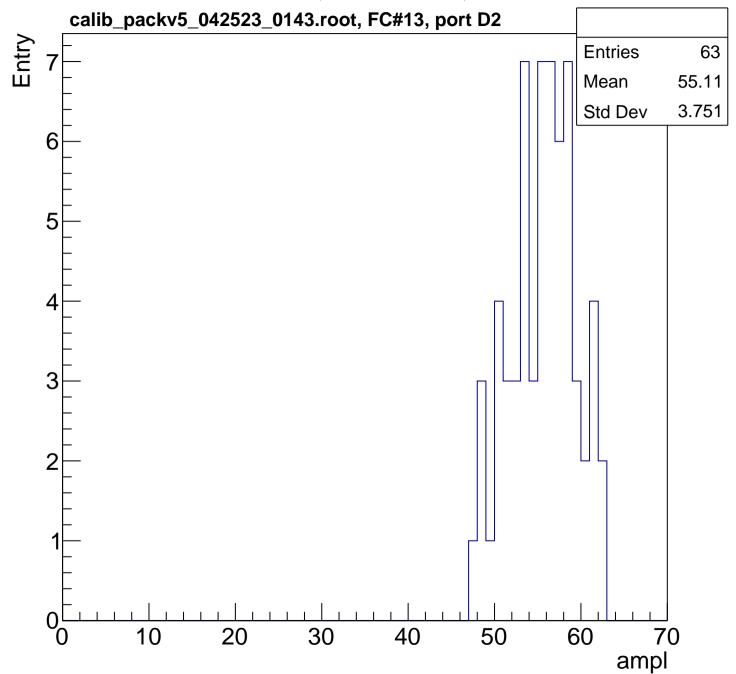


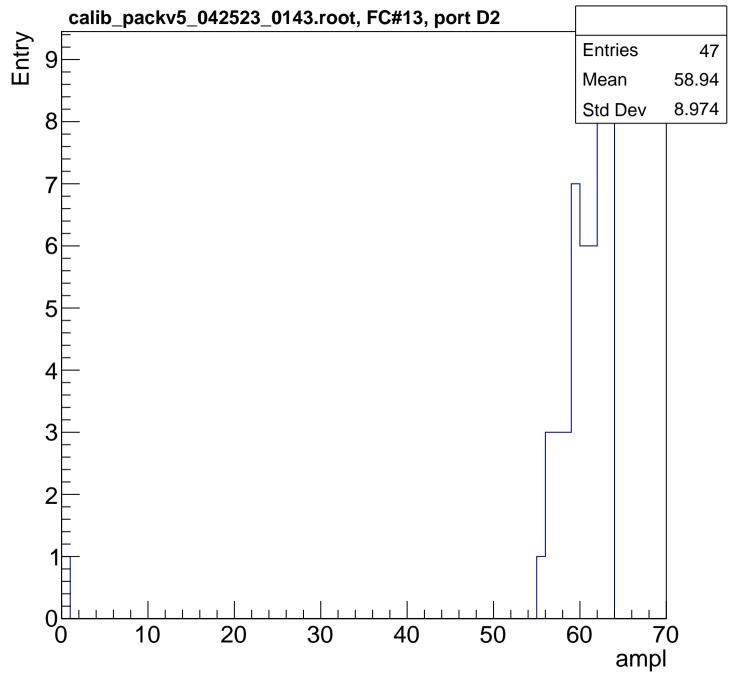


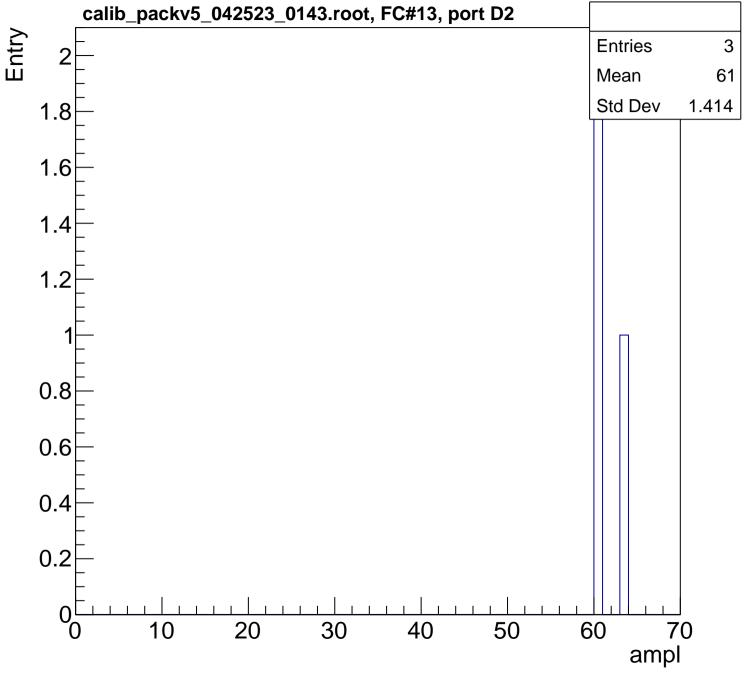




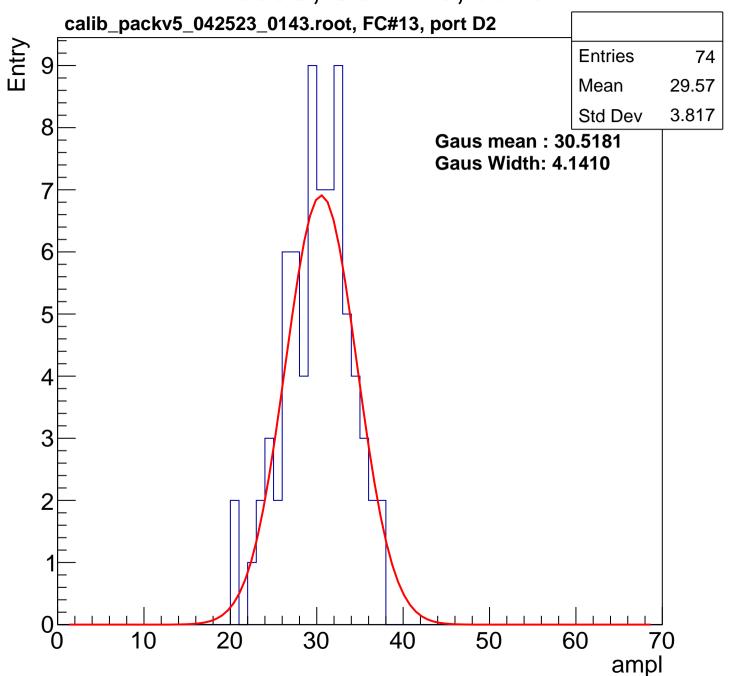


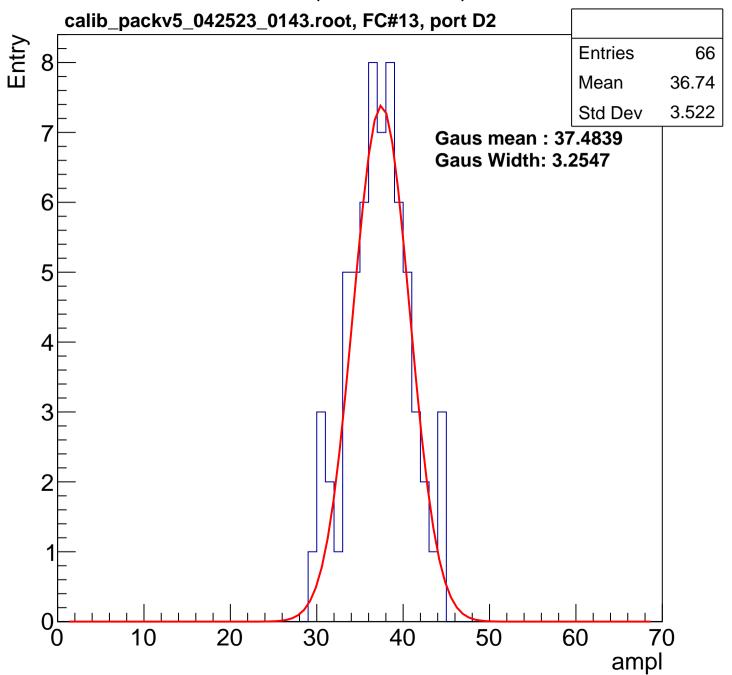


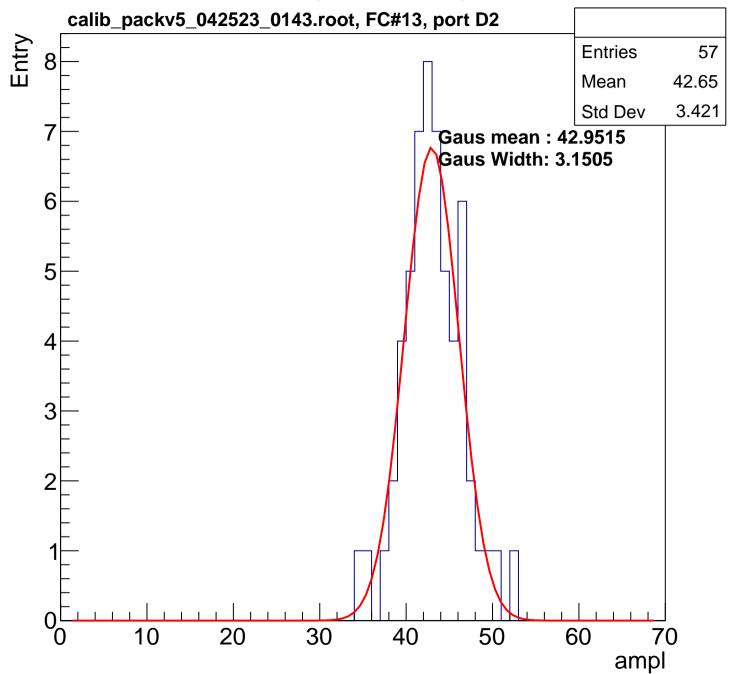


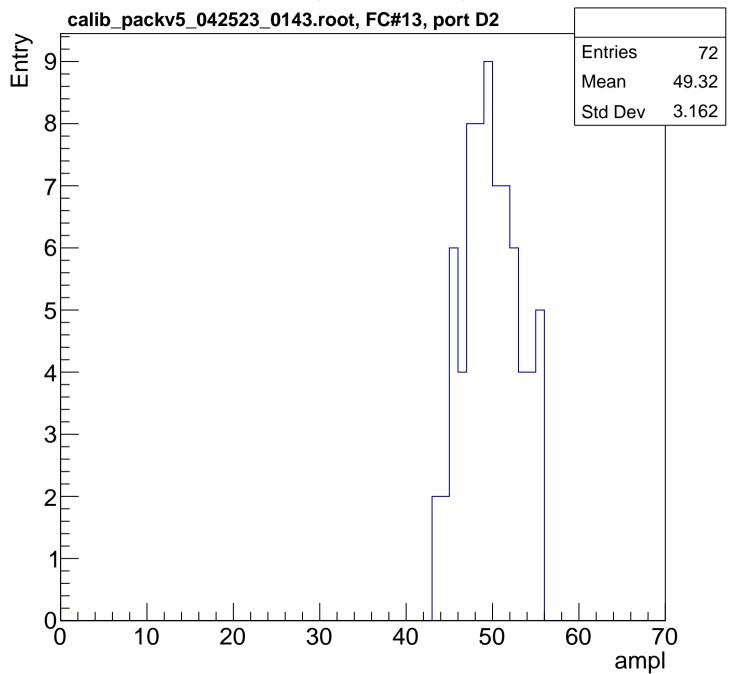


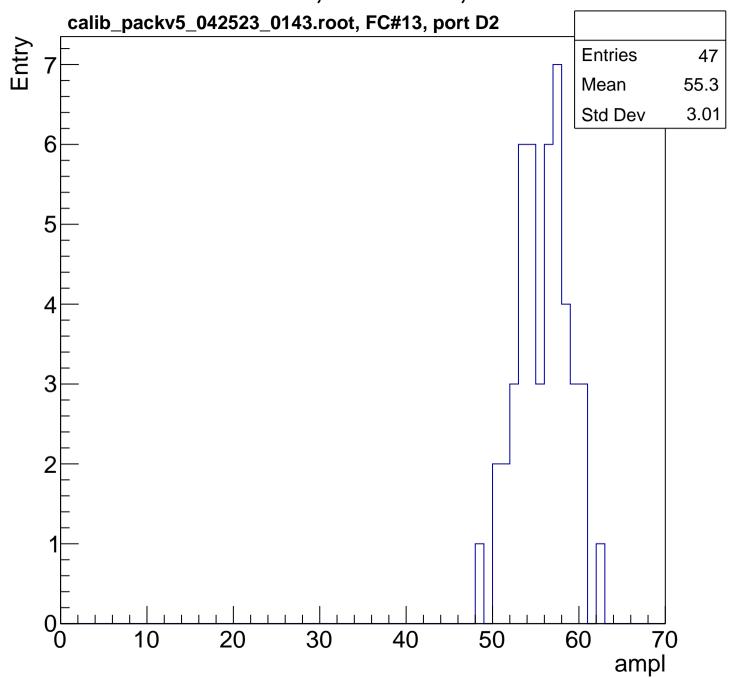


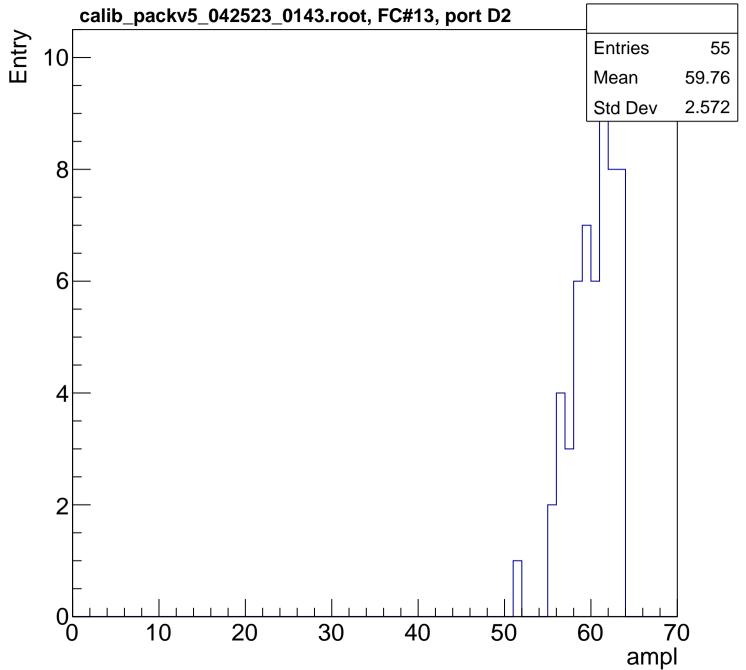


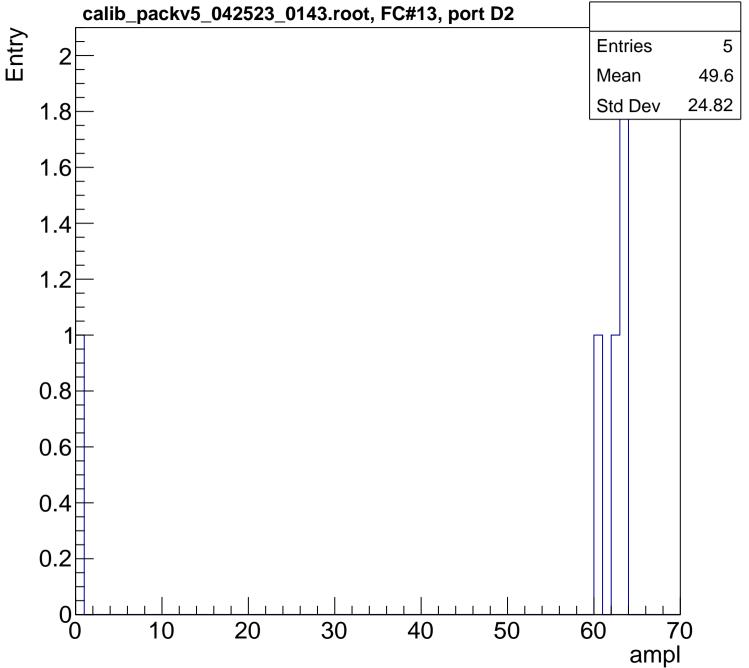




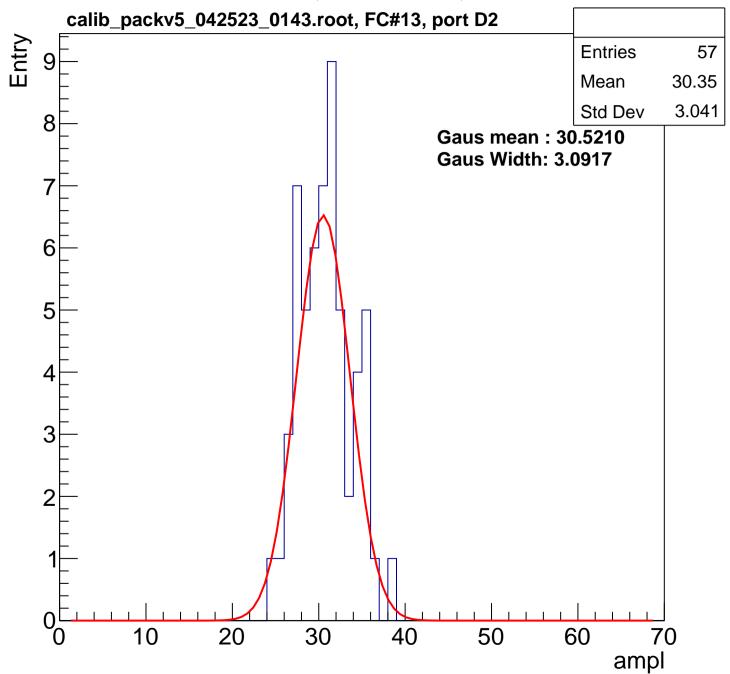


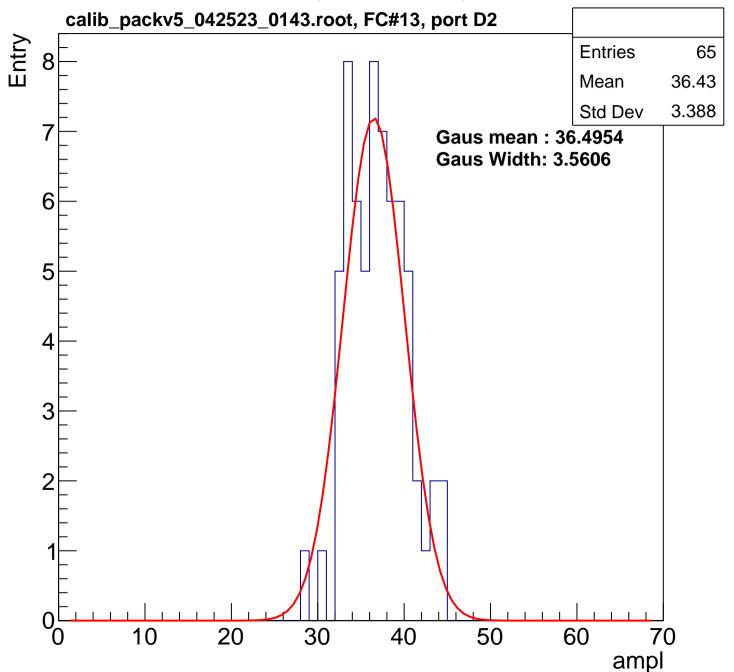


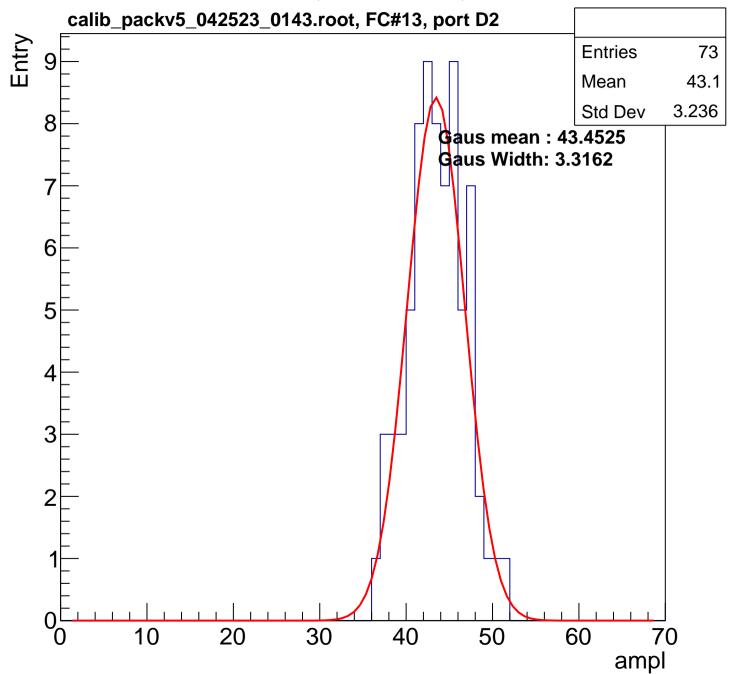


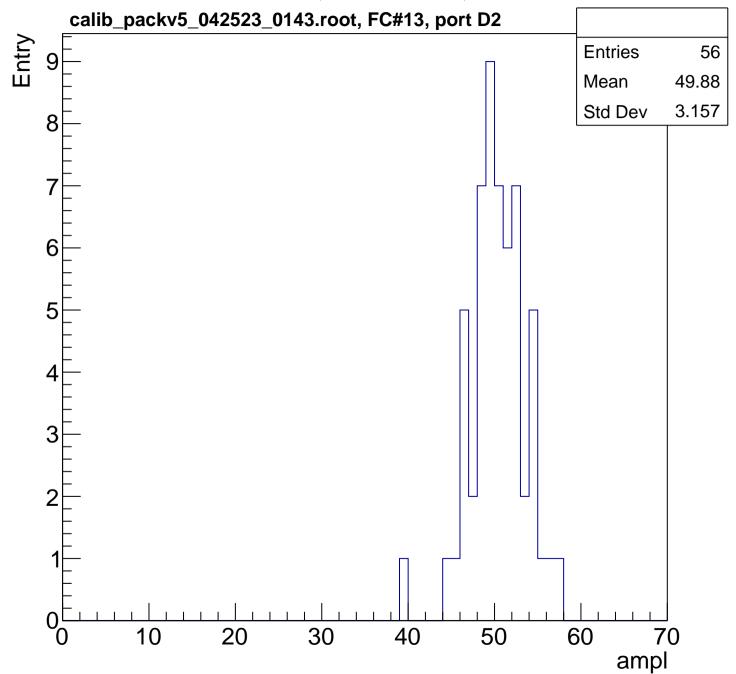


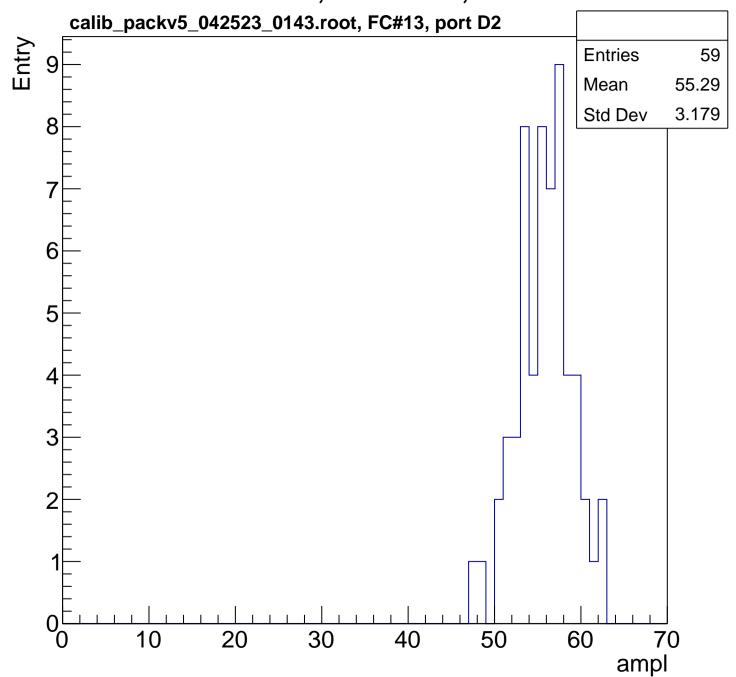


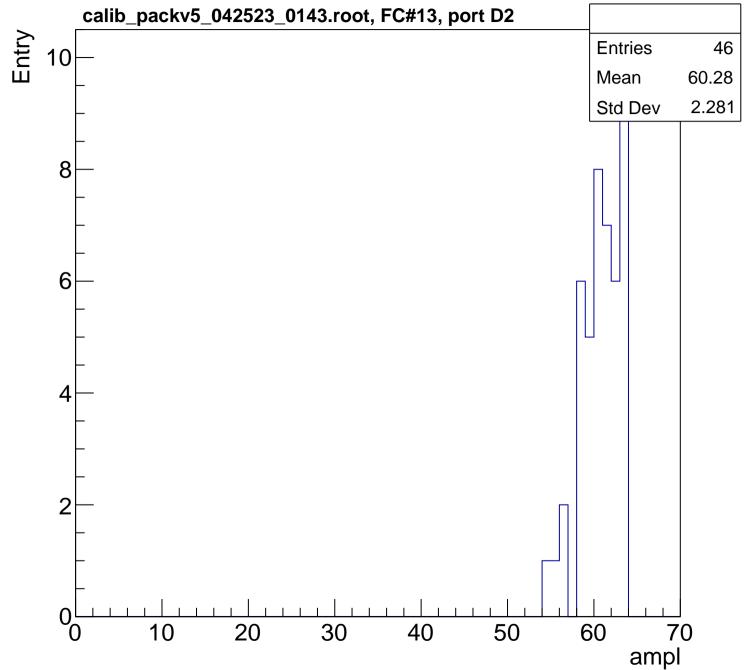


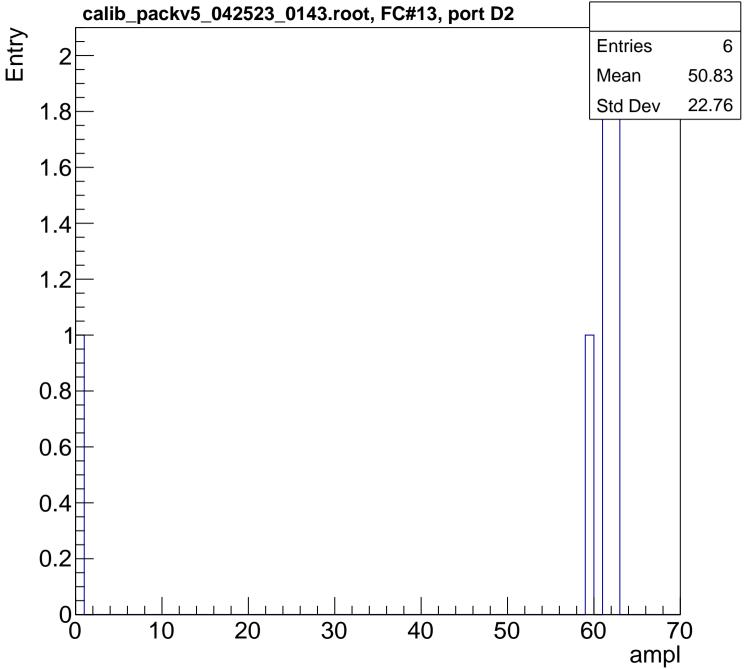




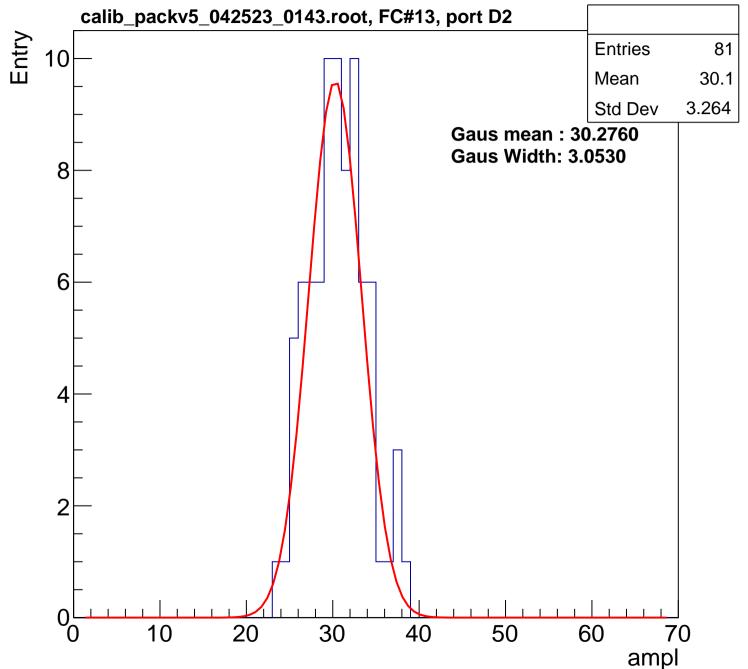


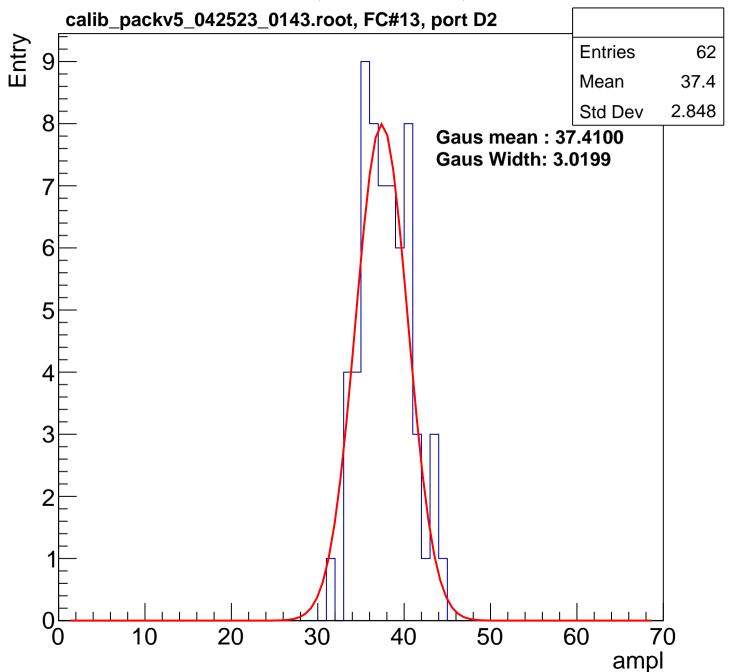


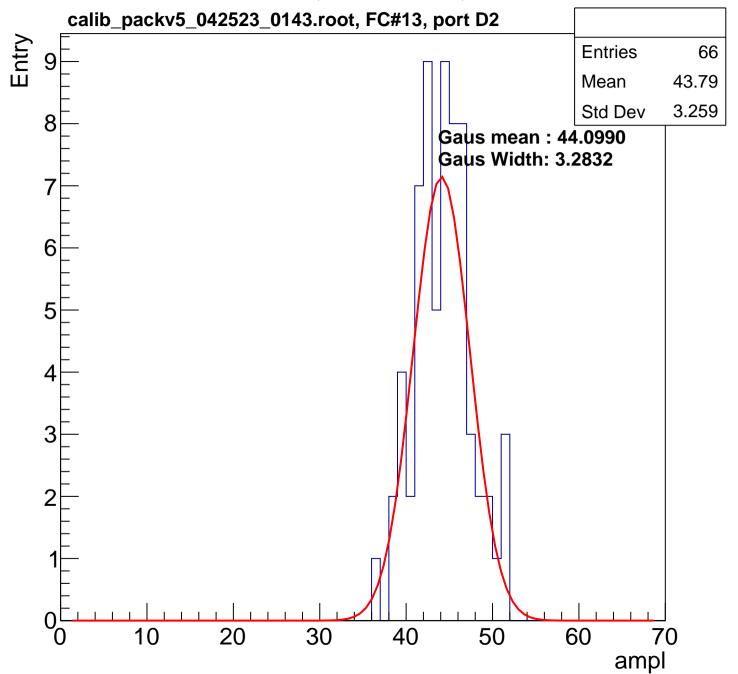


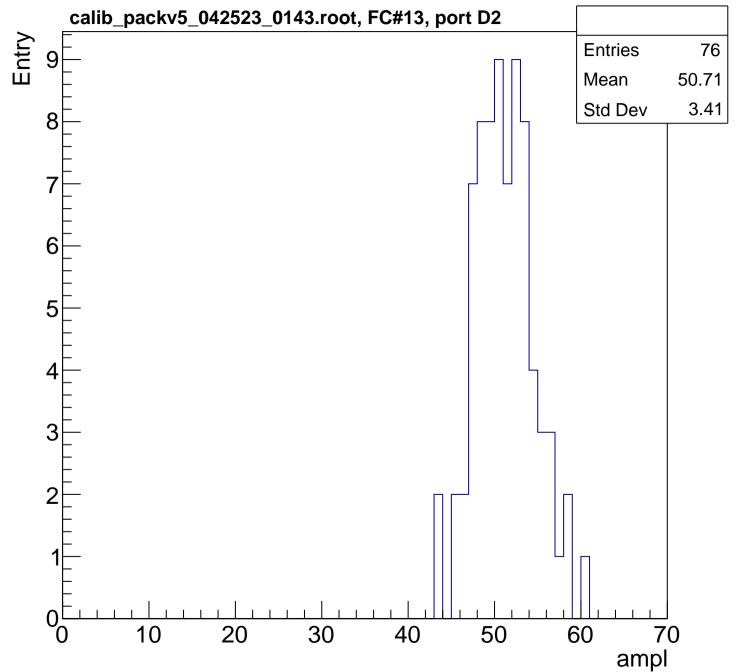


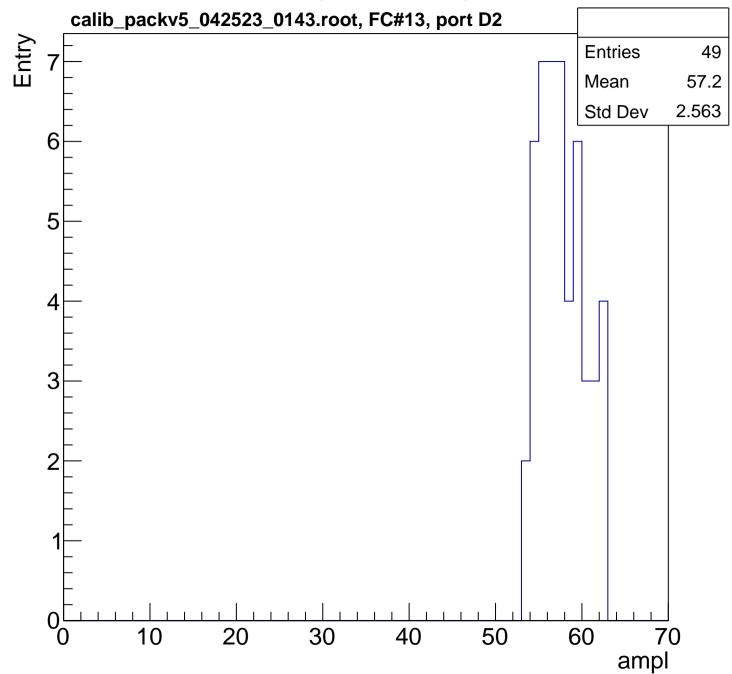


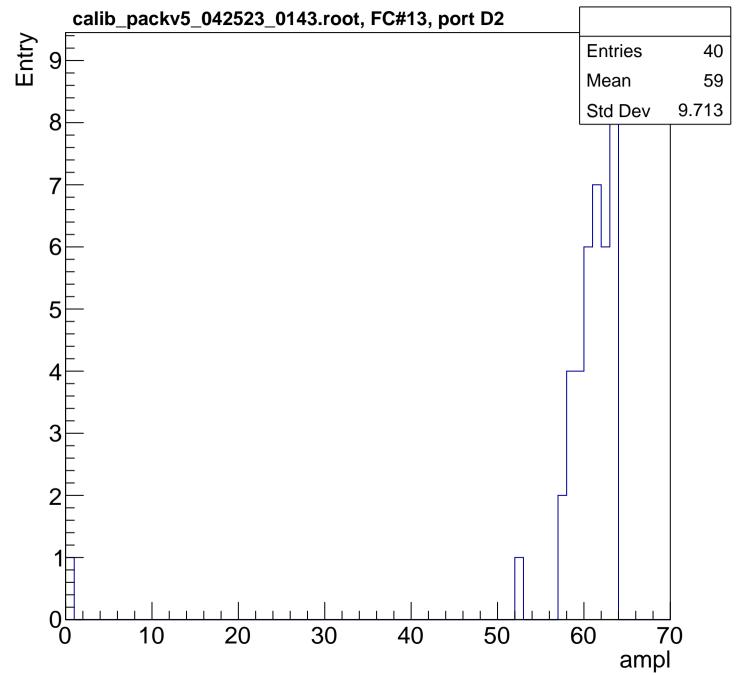


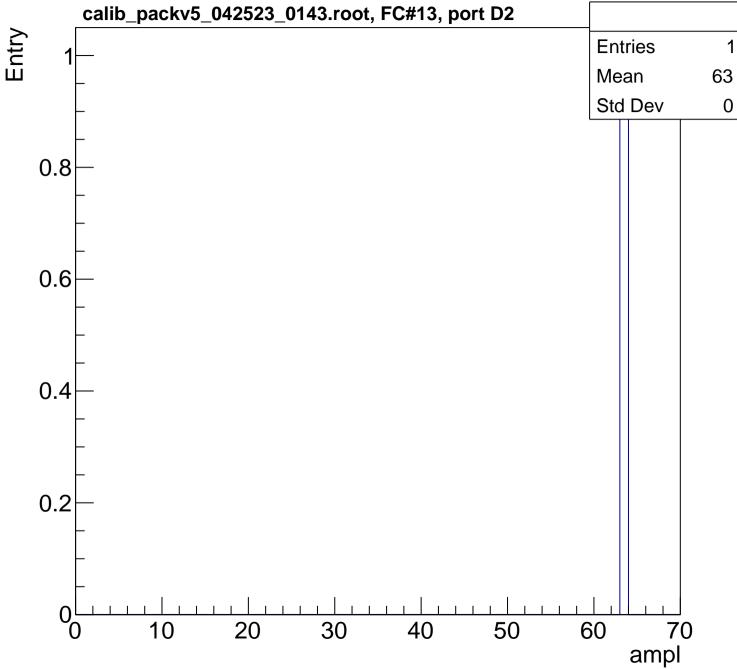


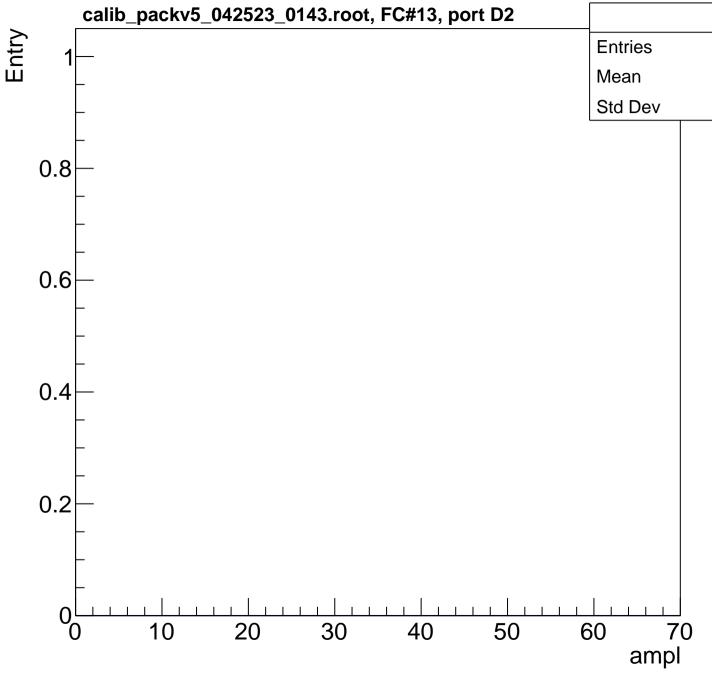


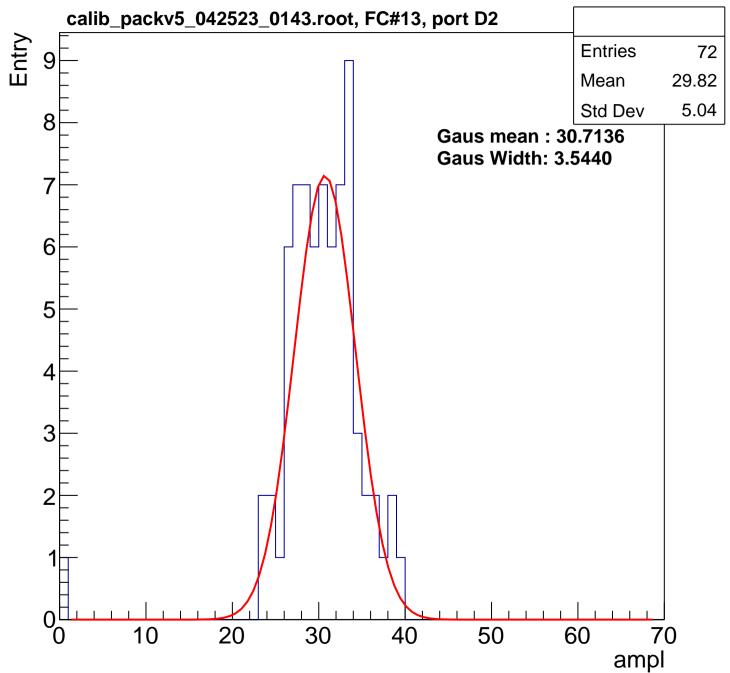


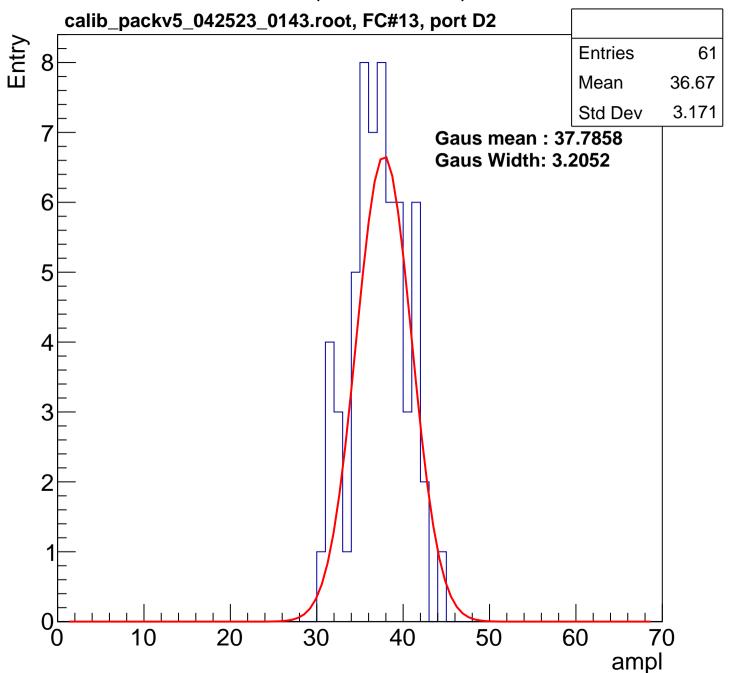


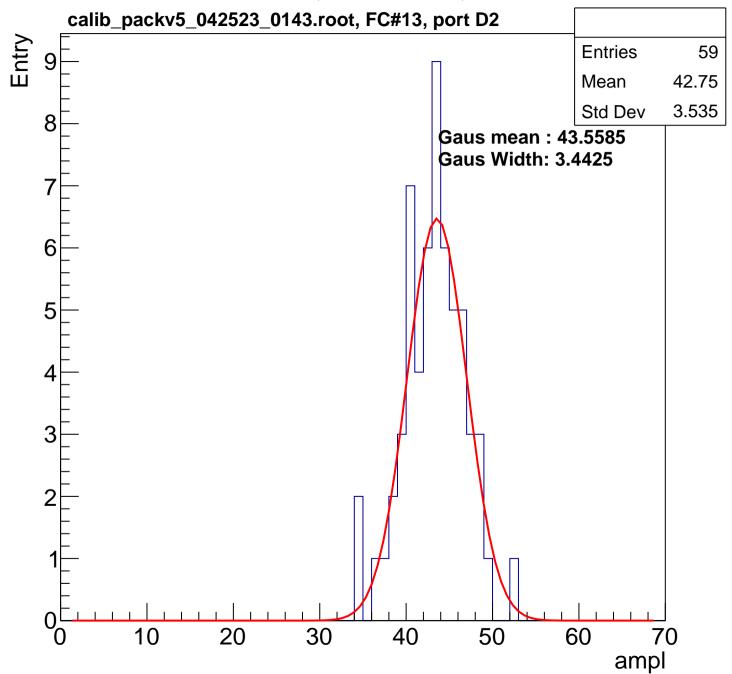


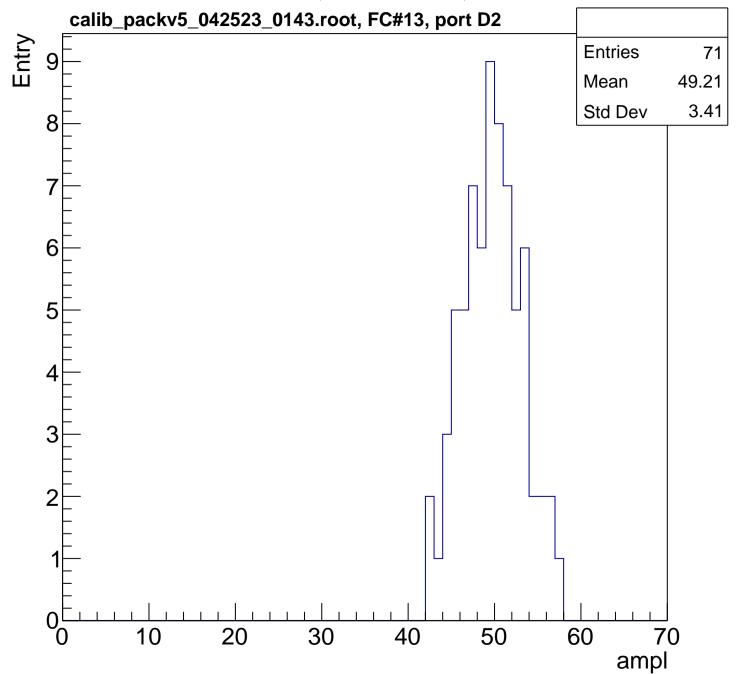


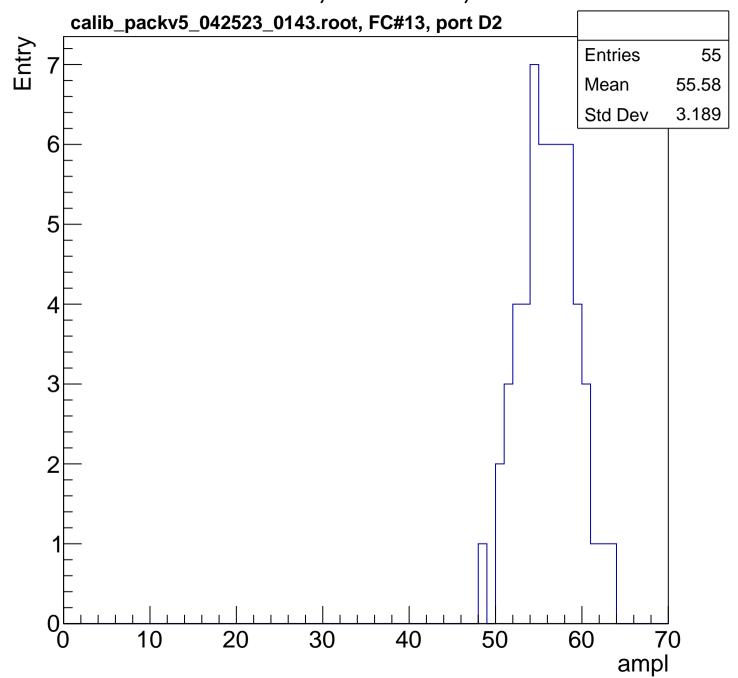


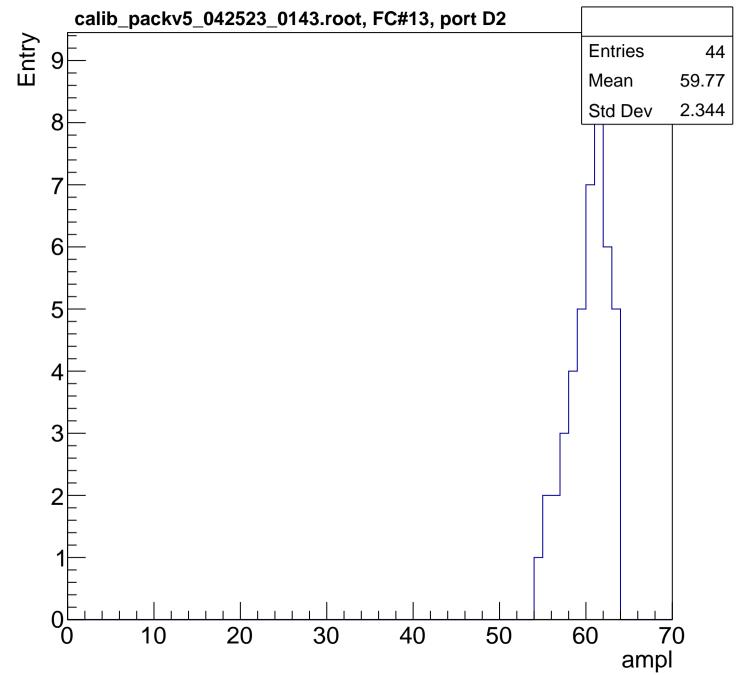


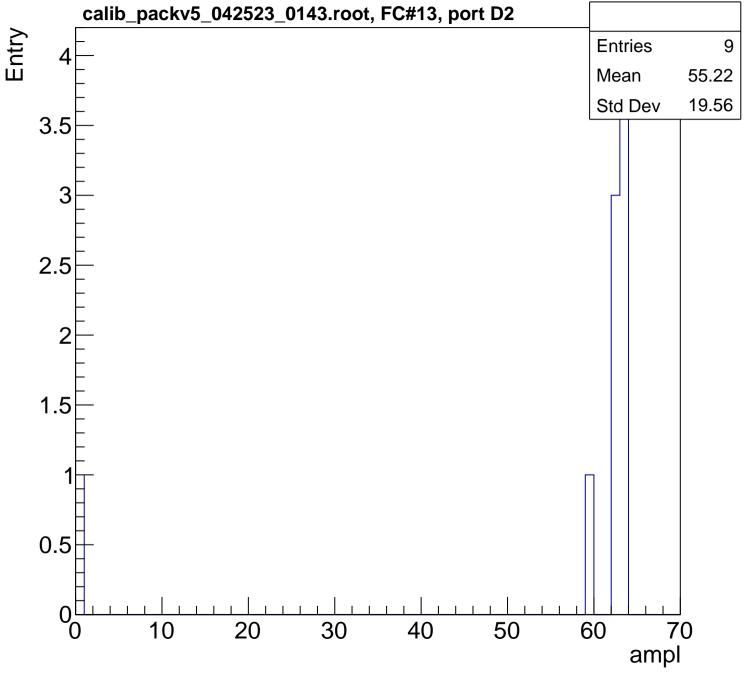


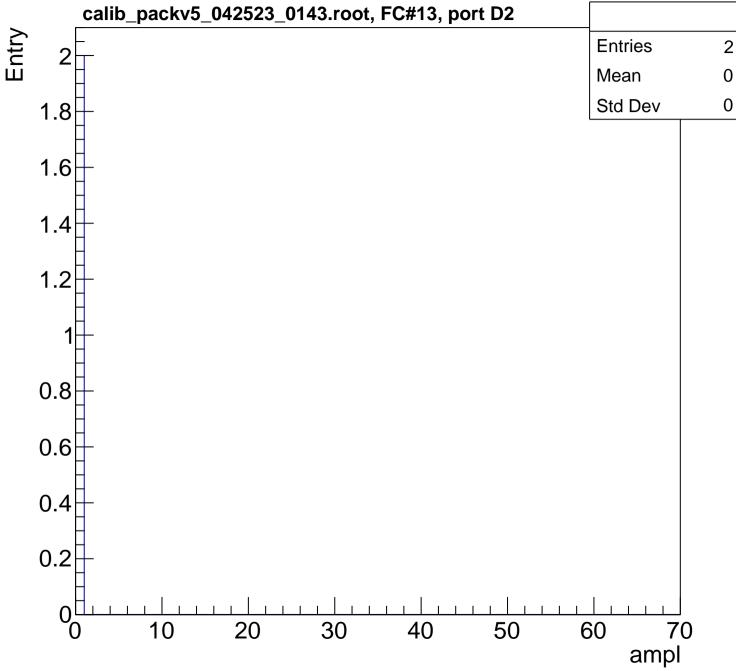


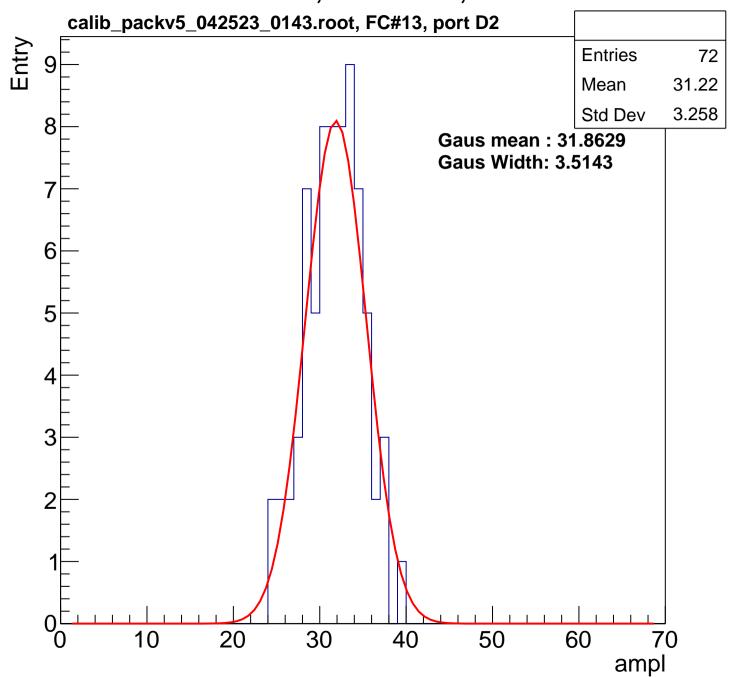


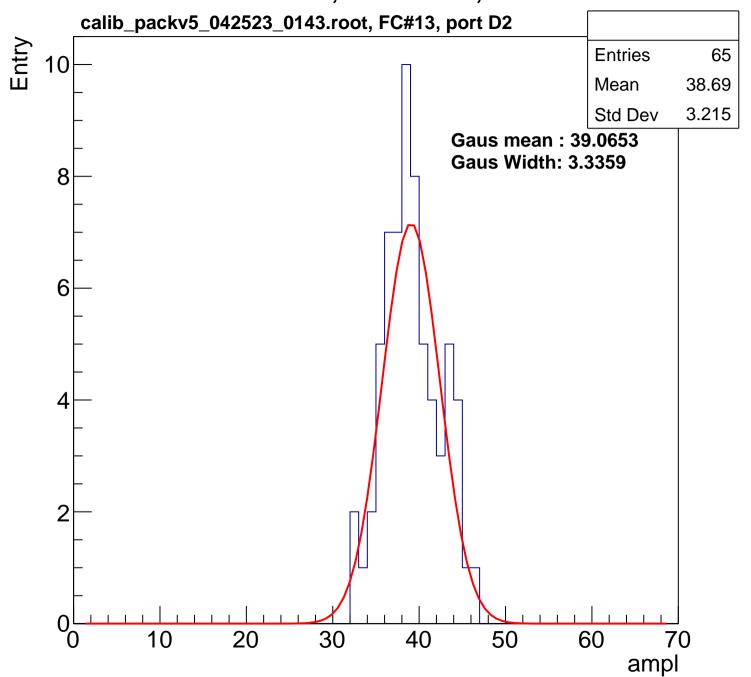


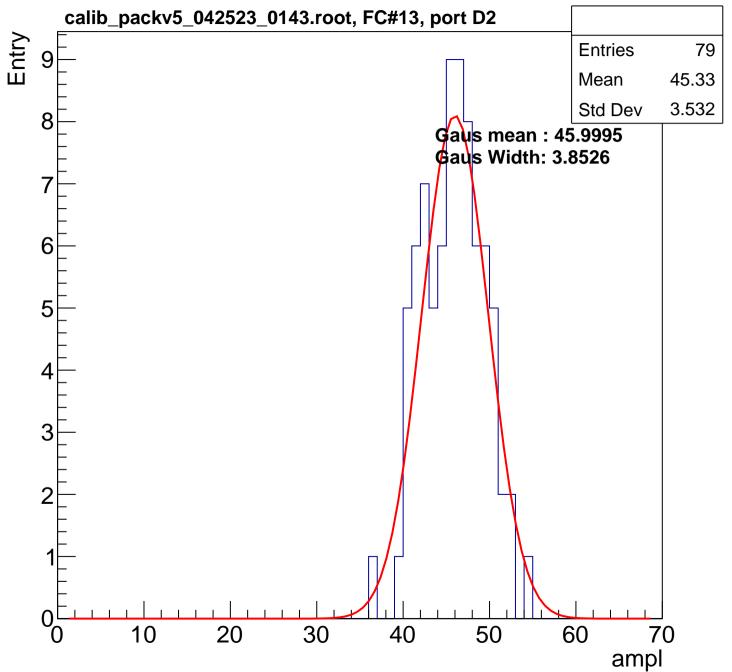


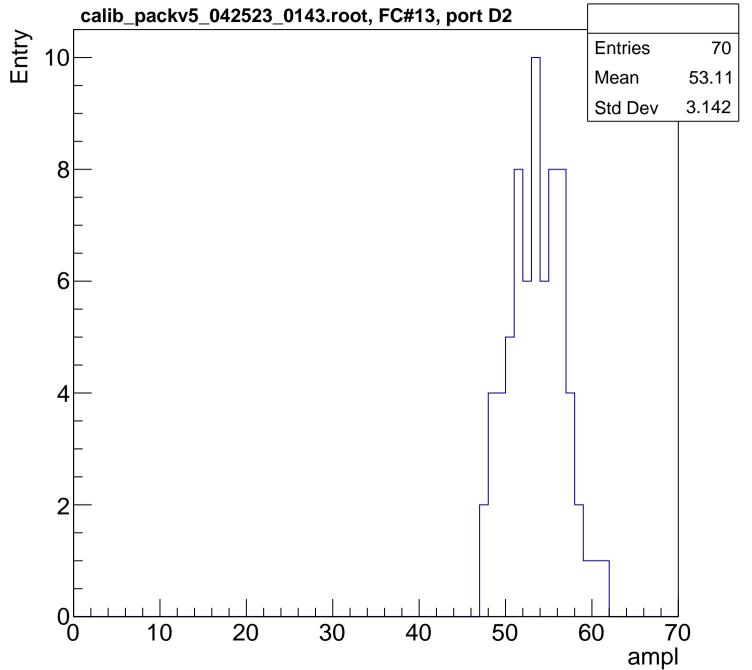


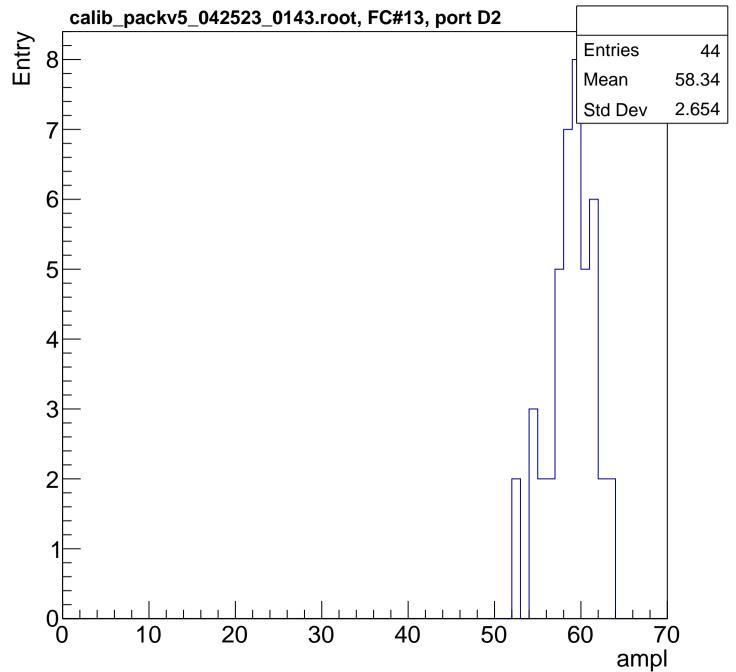


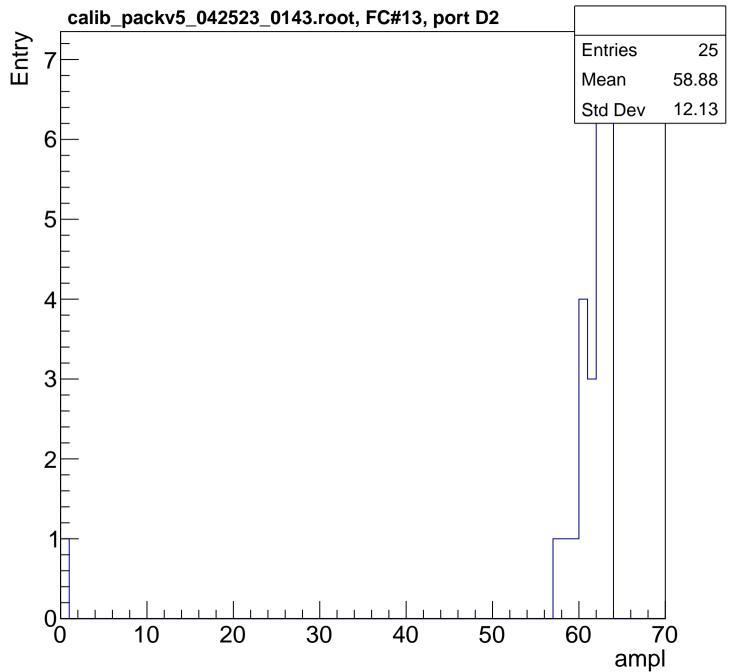


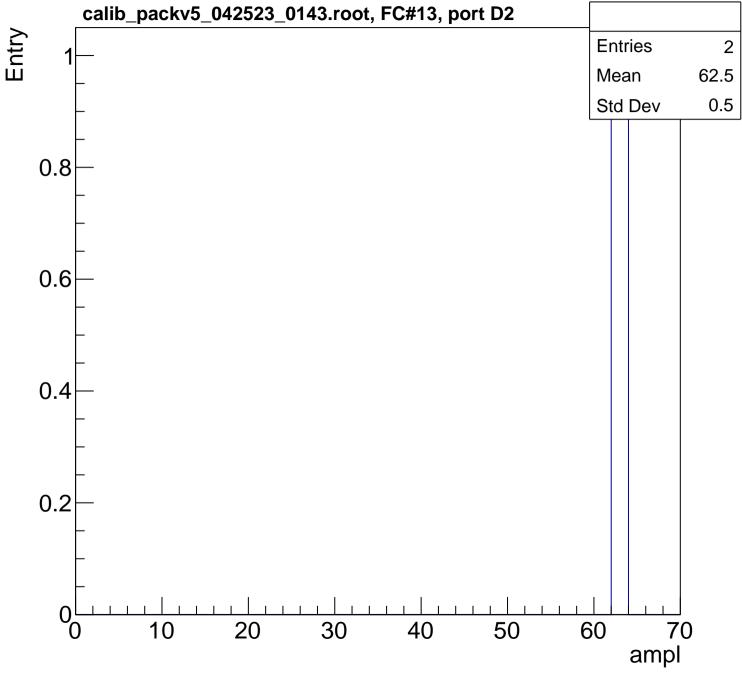




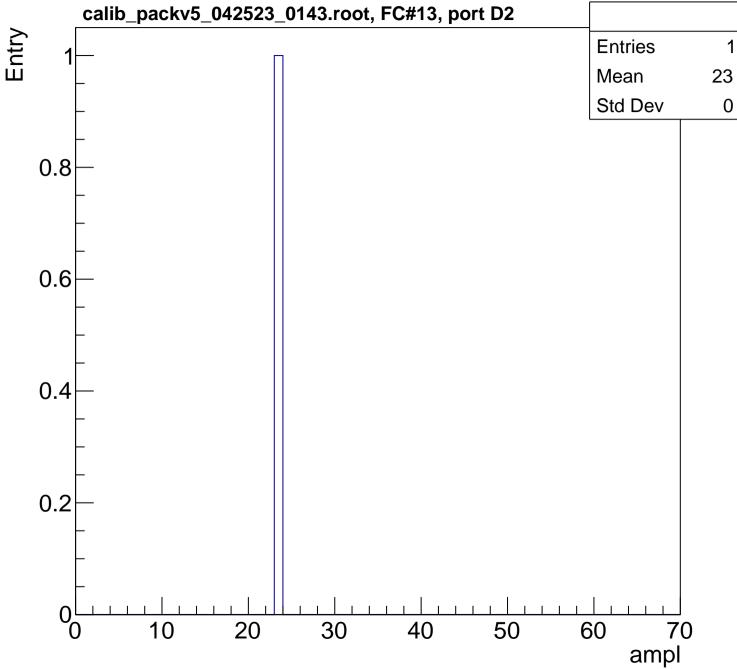


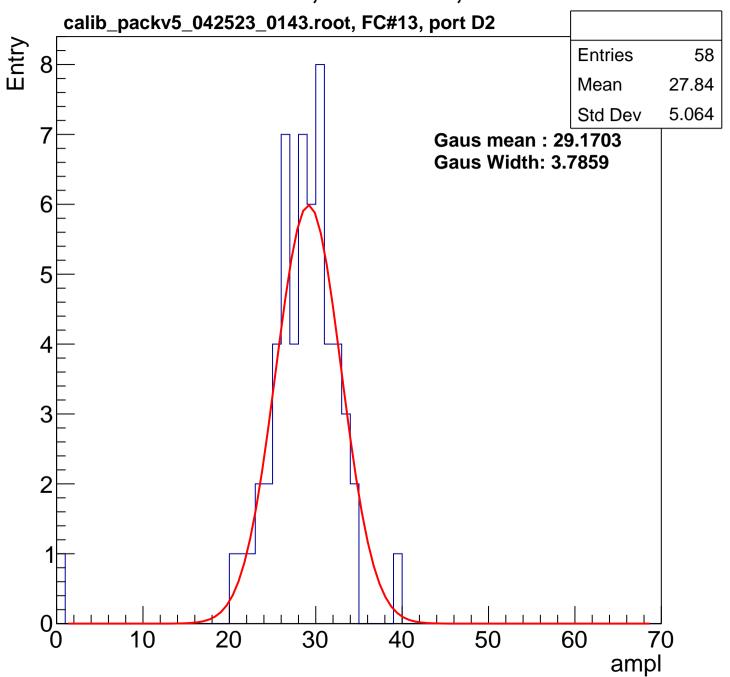


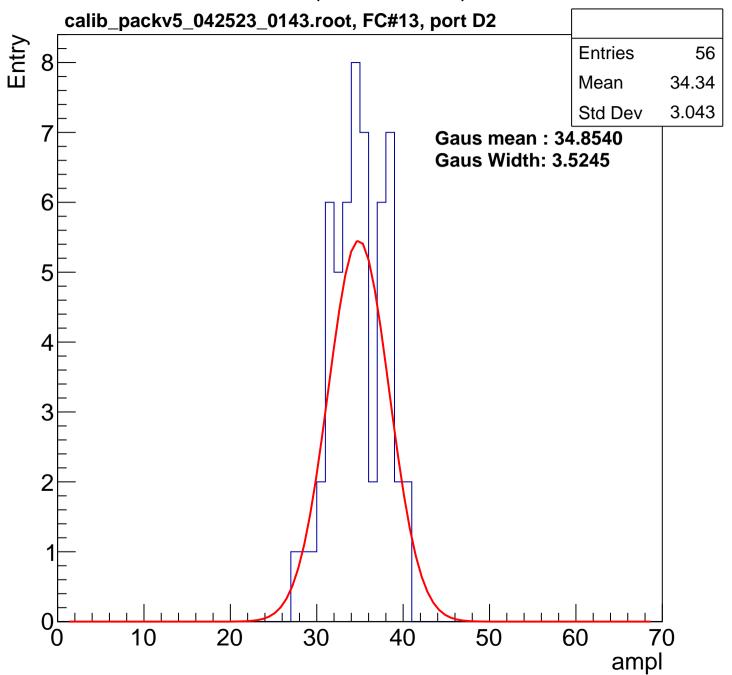


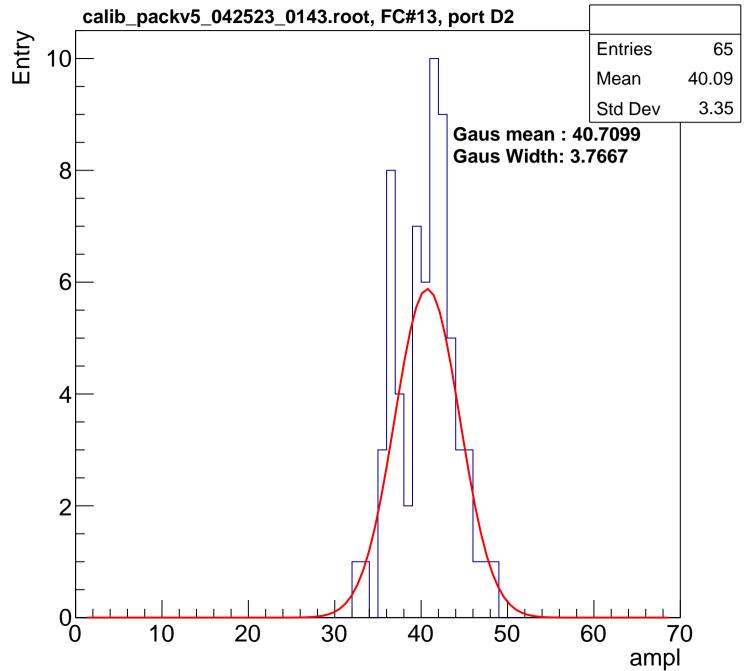


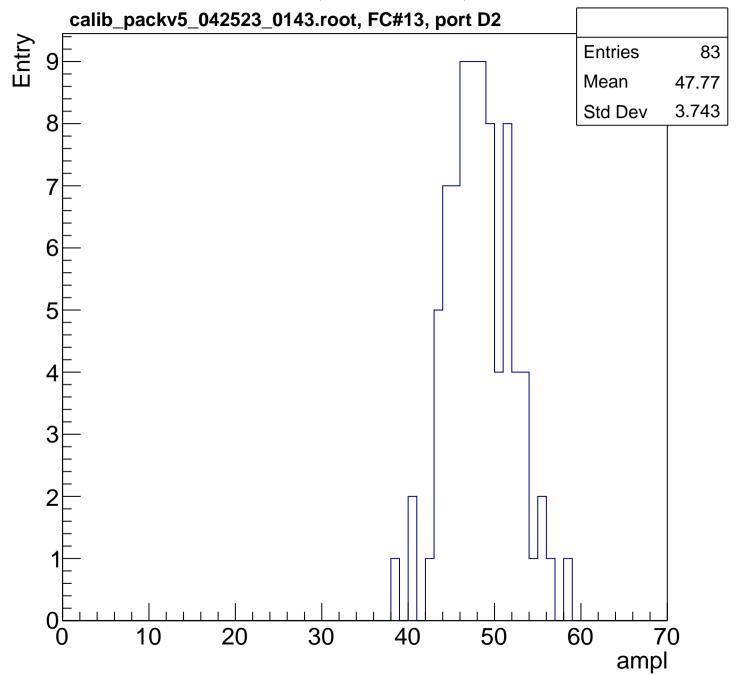
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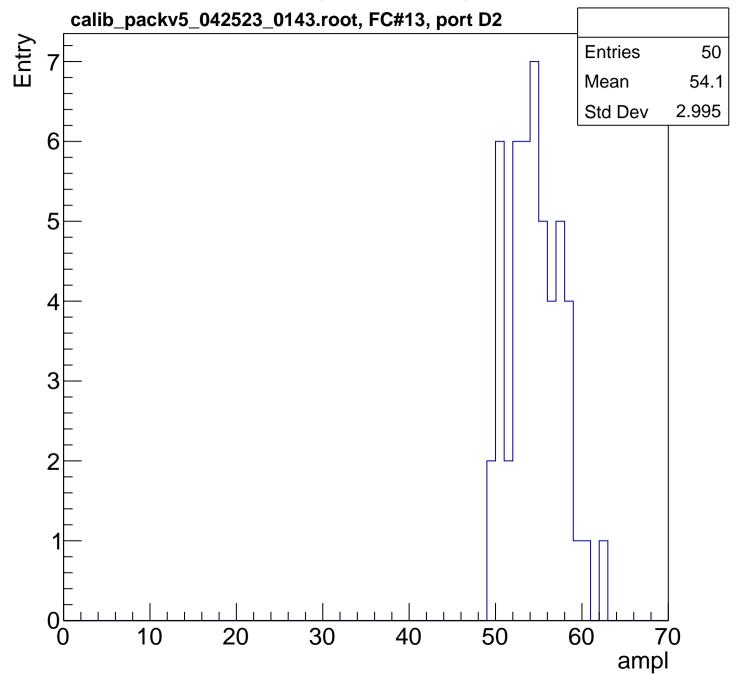


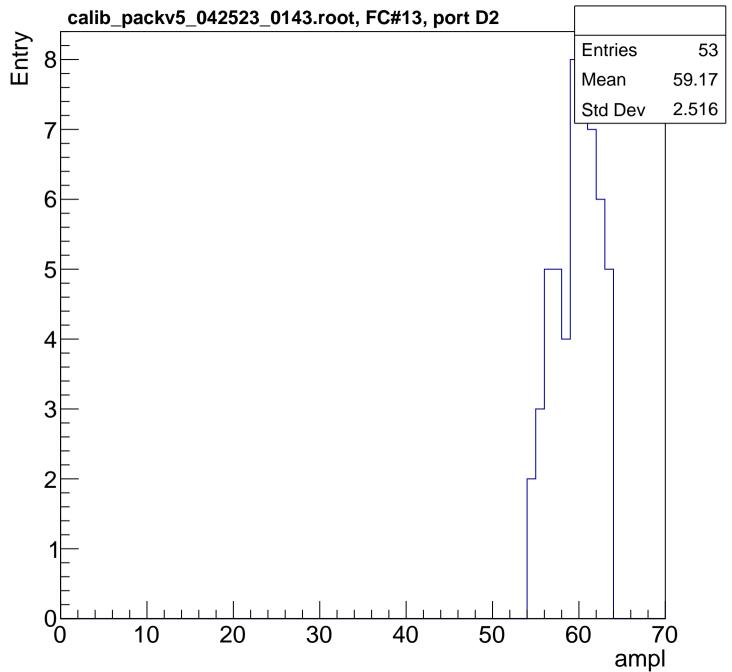


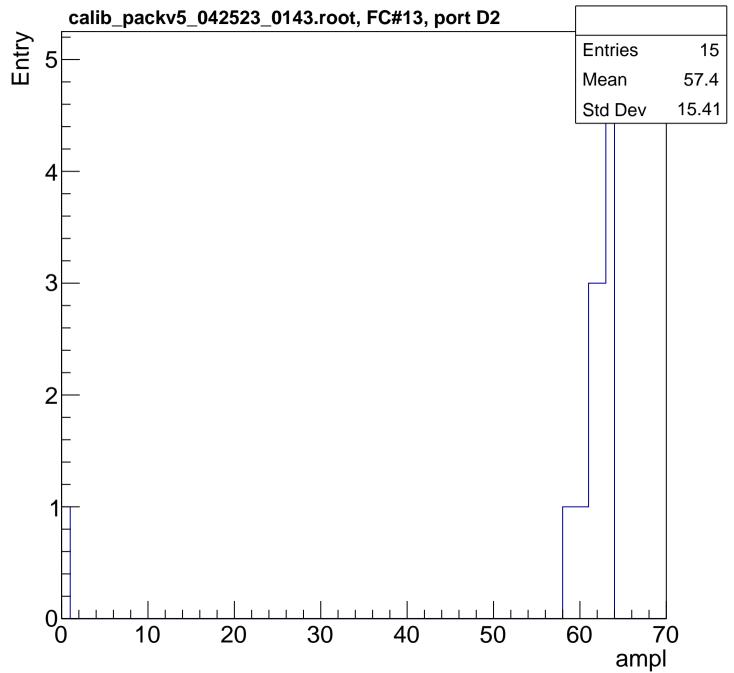




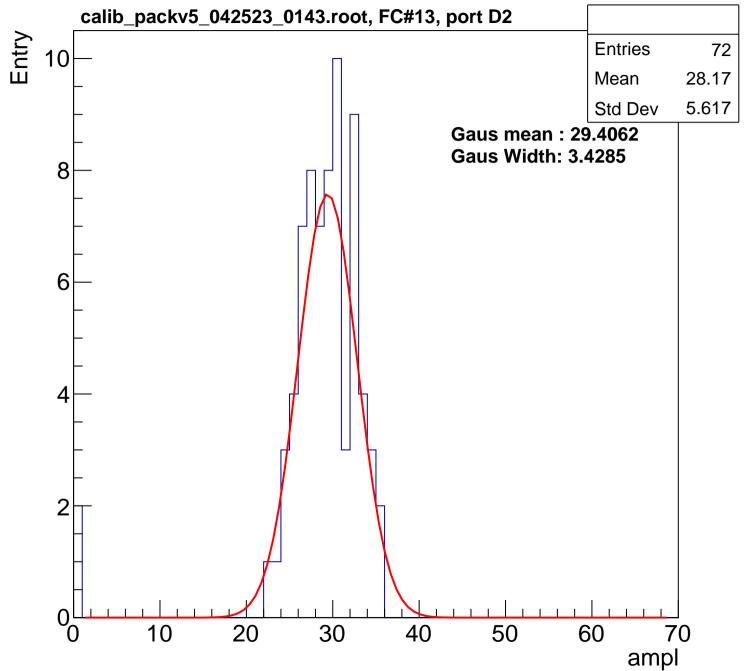


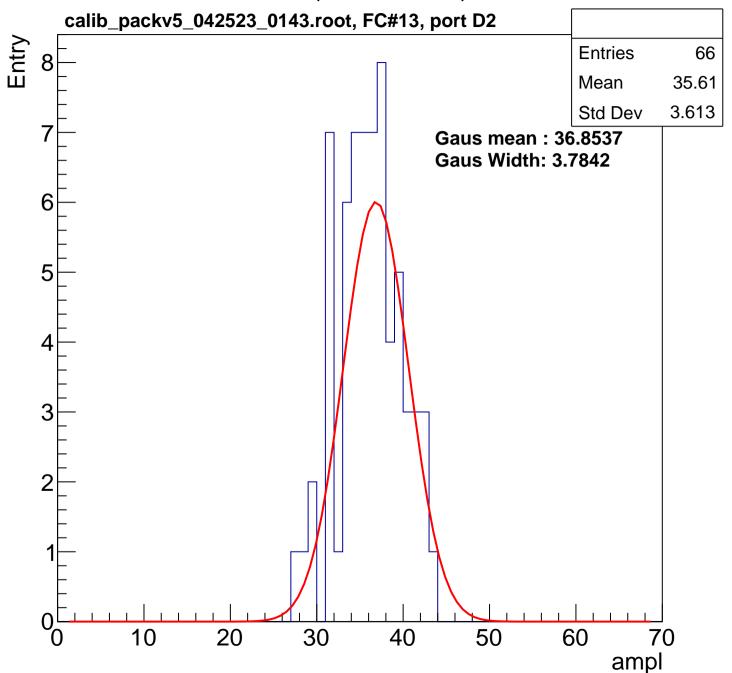


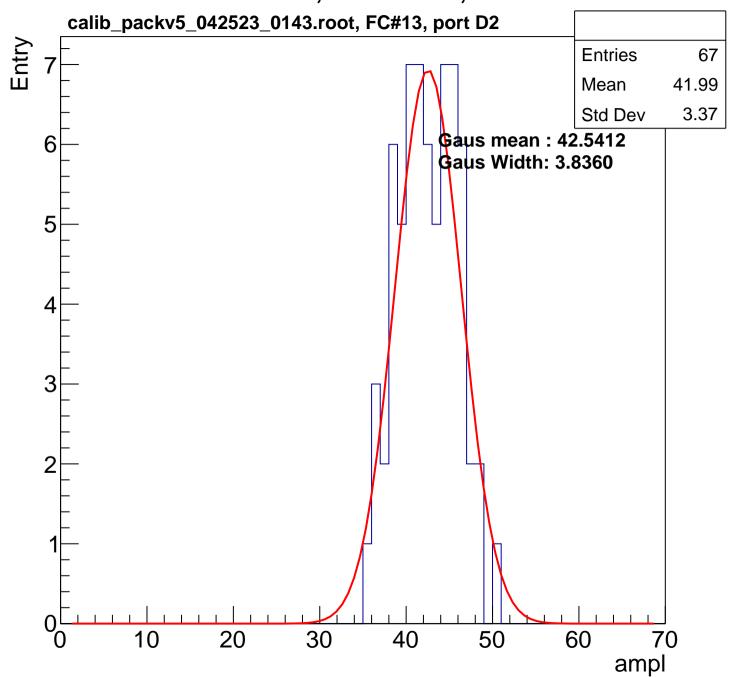


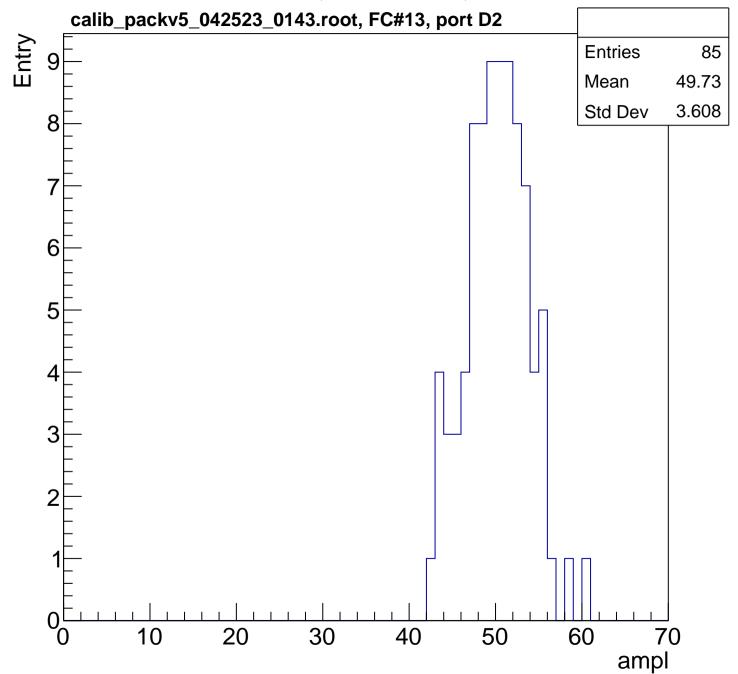


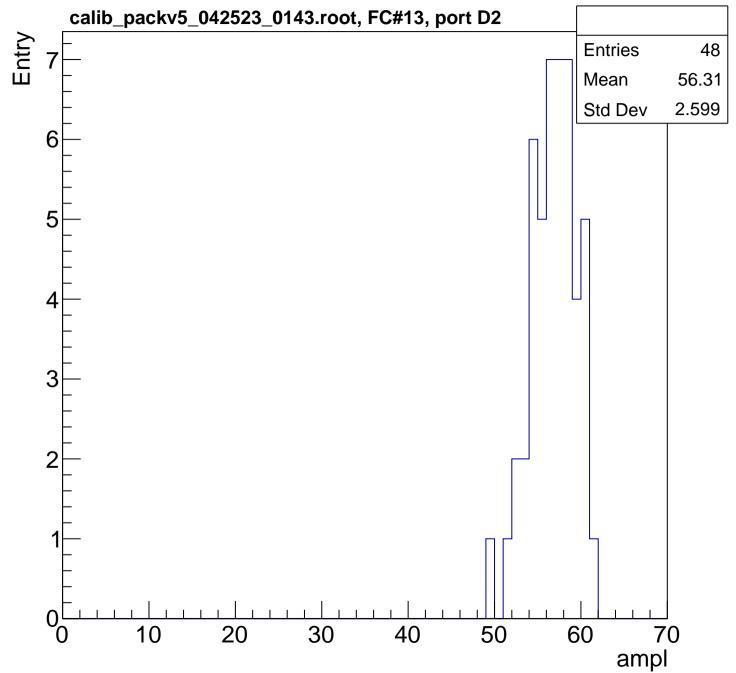
B1L003S, U9-ch84, adc7 calib\_packv5\_042523\_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

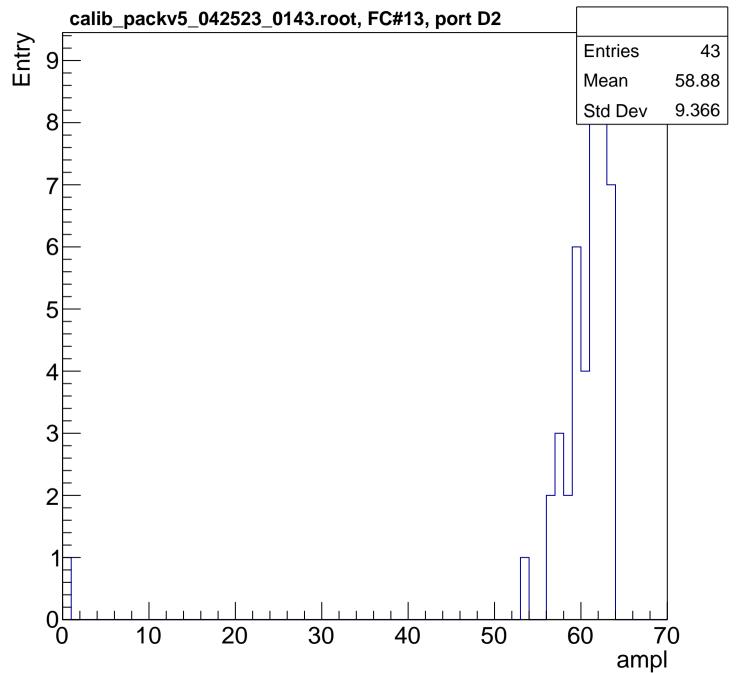


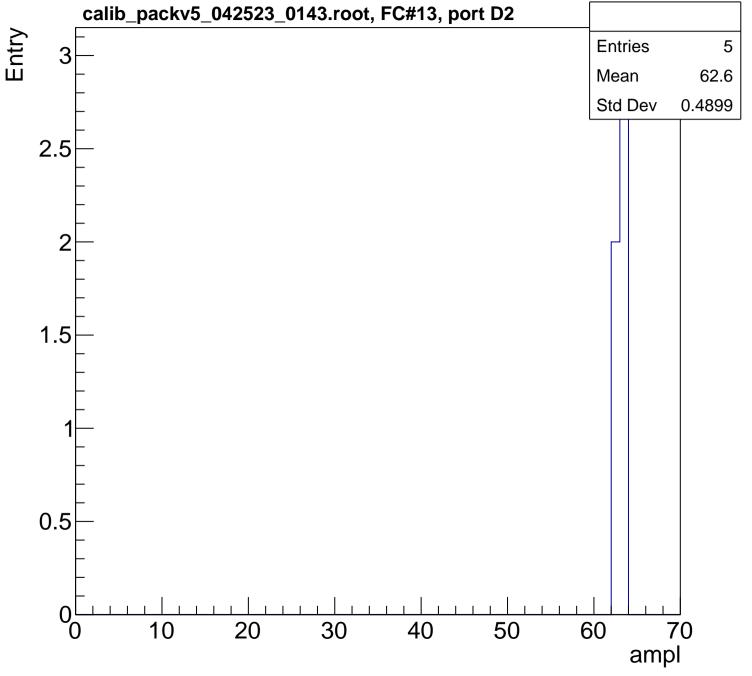




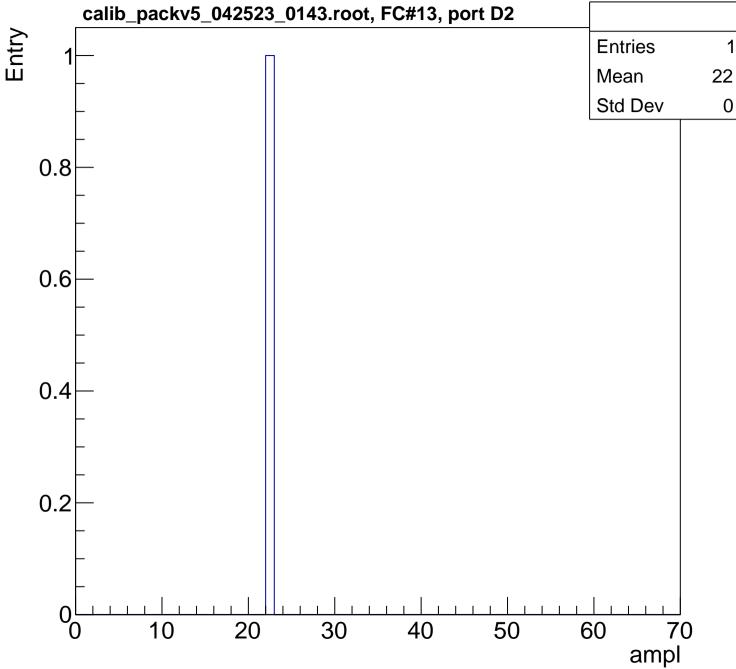


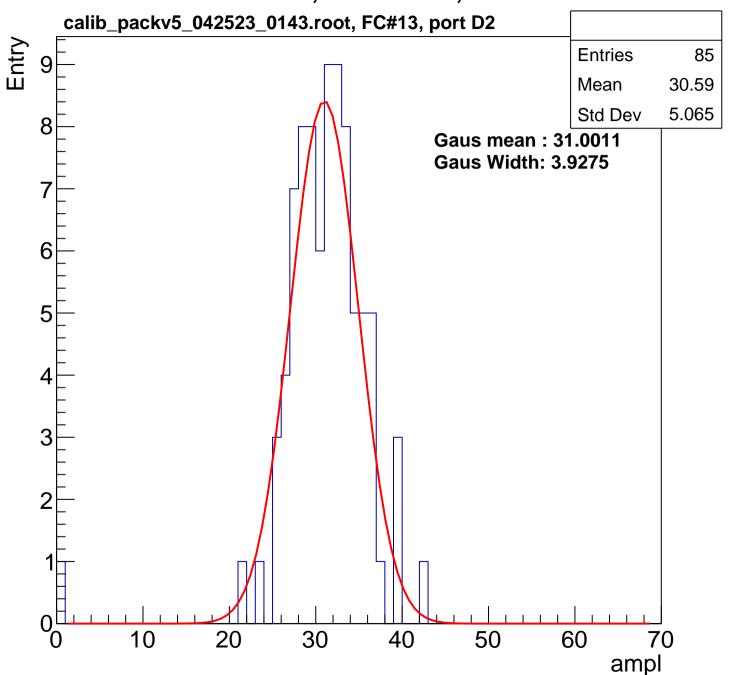


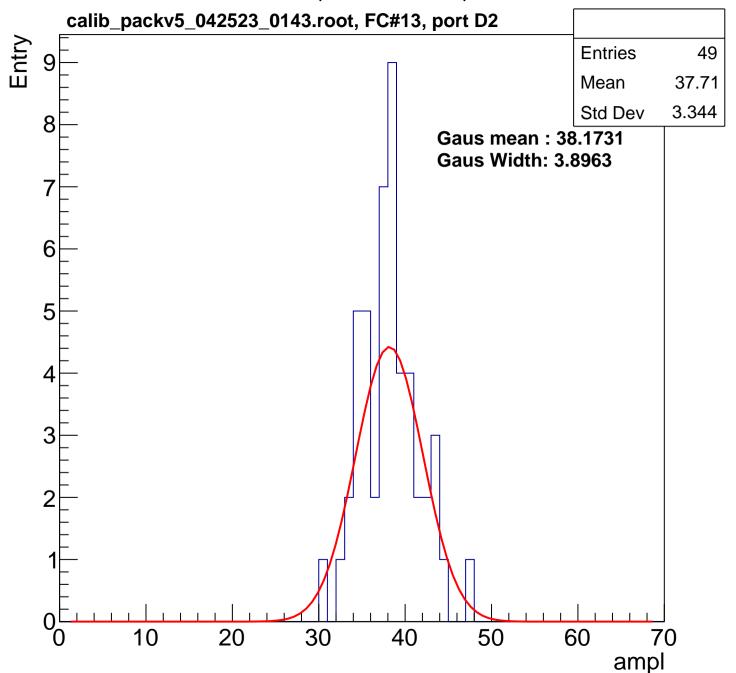


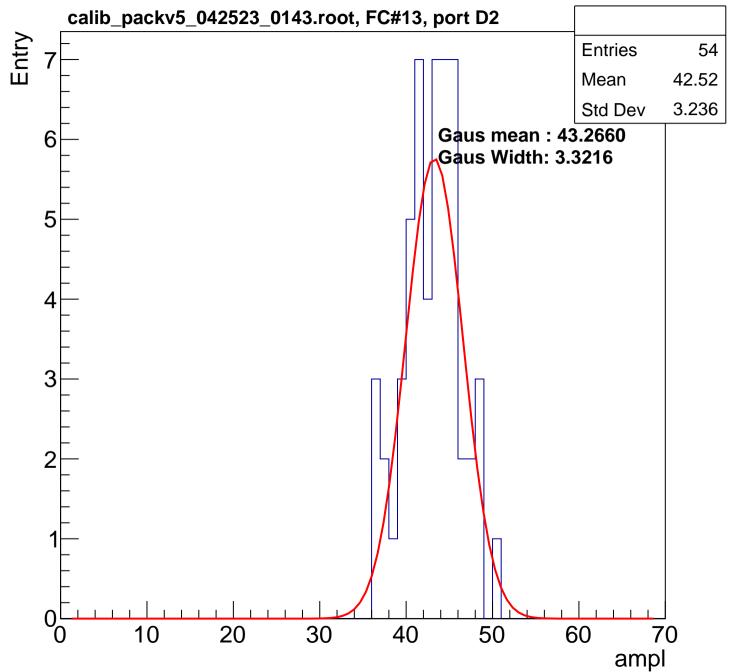


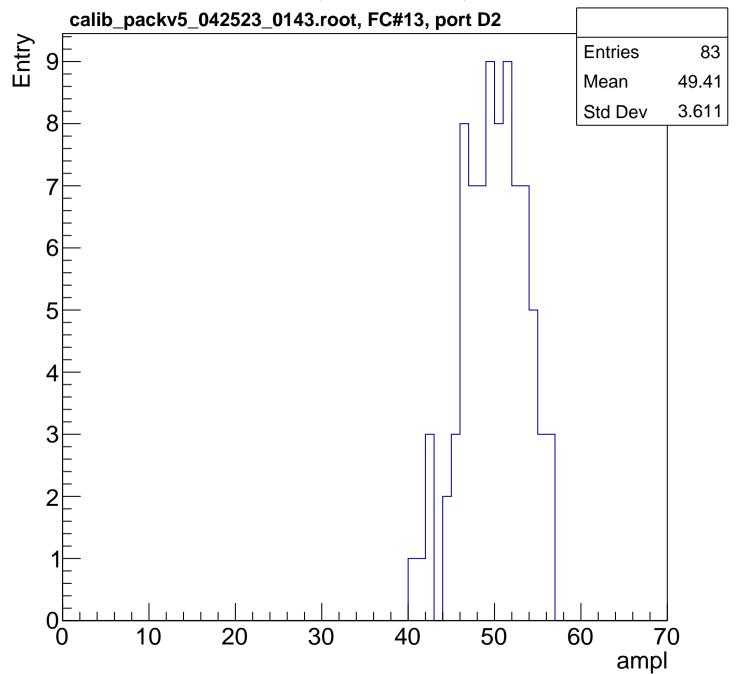
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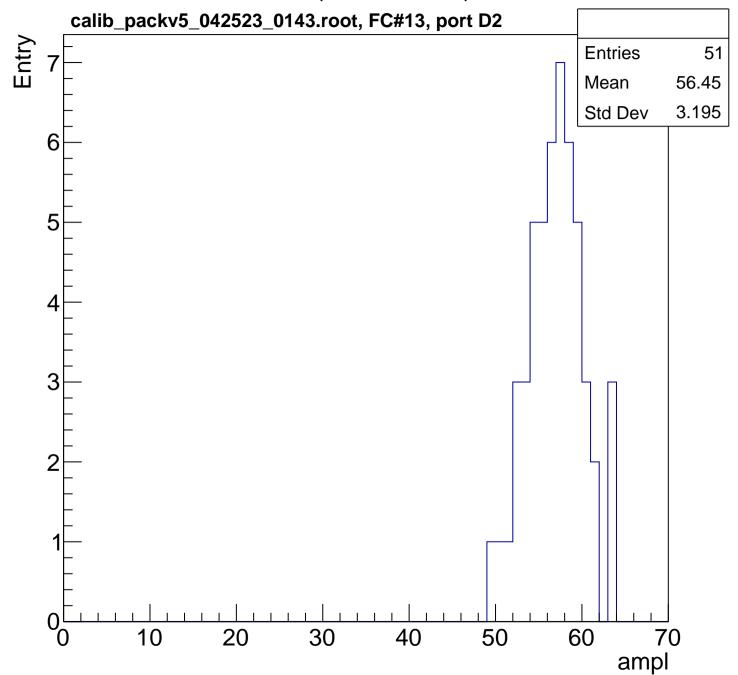


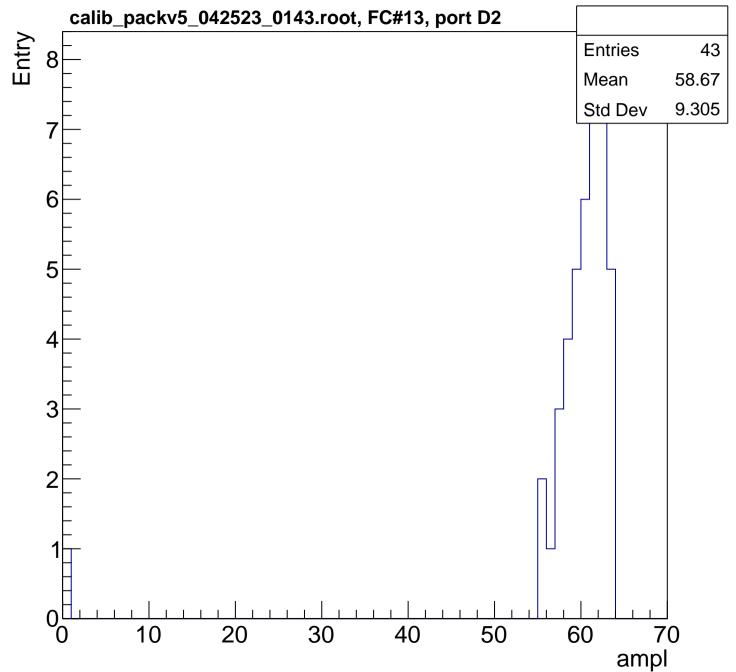


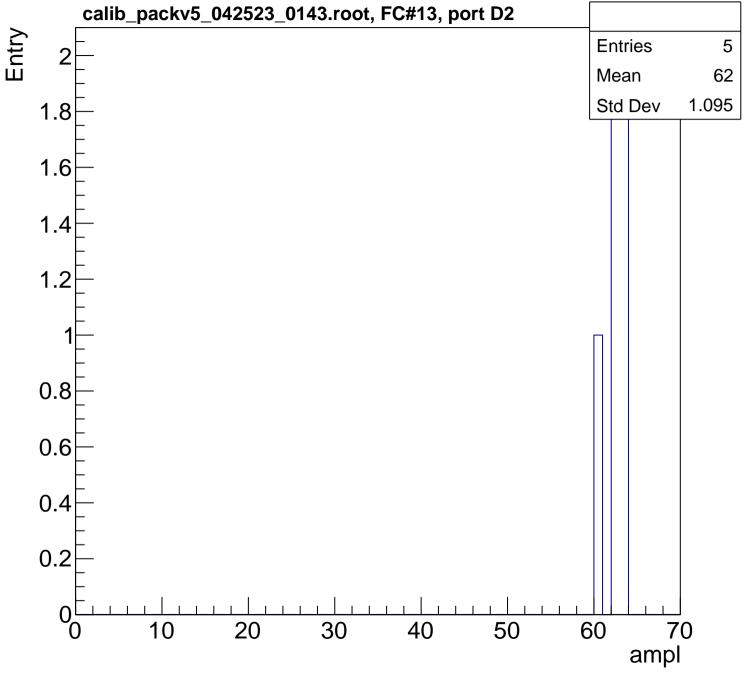




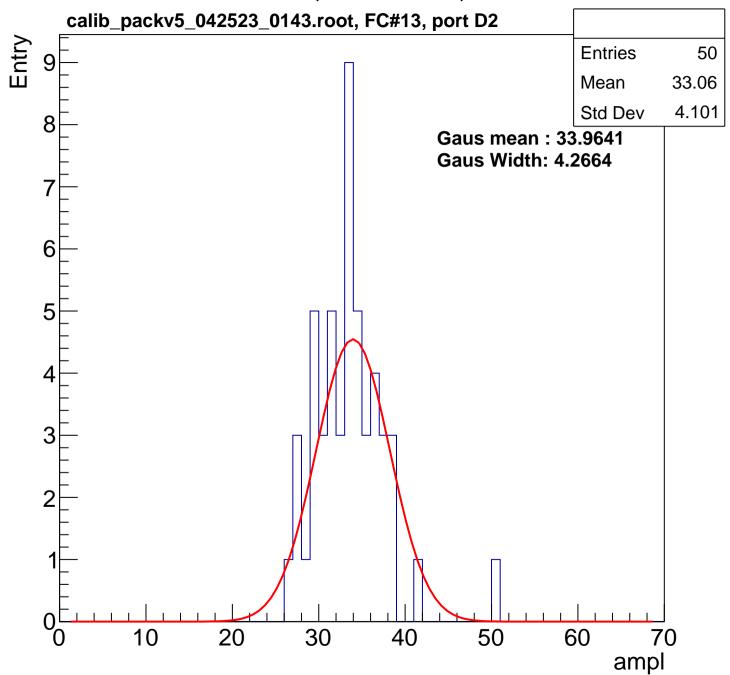


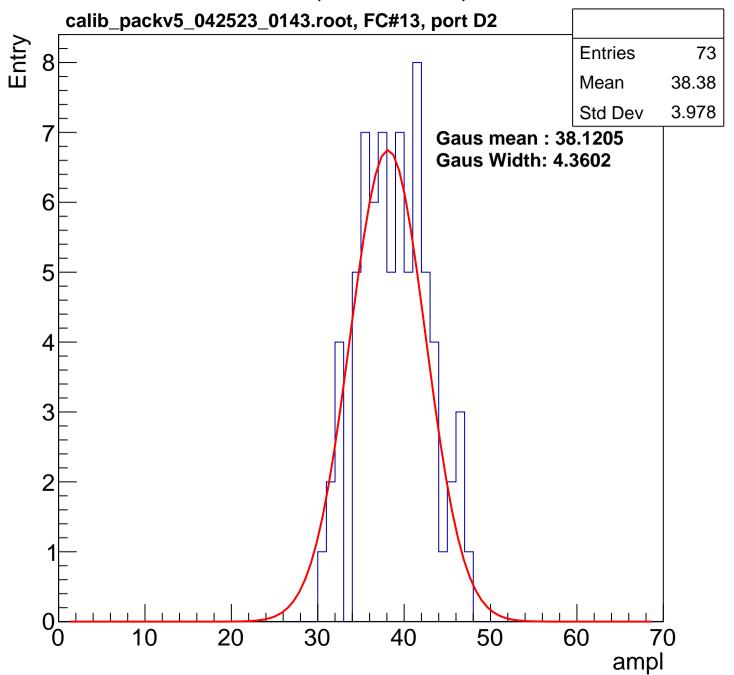


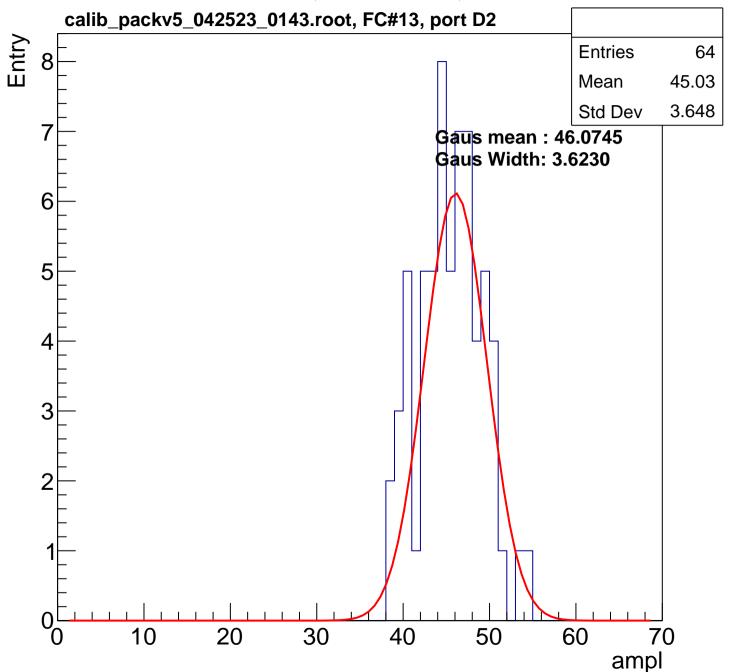


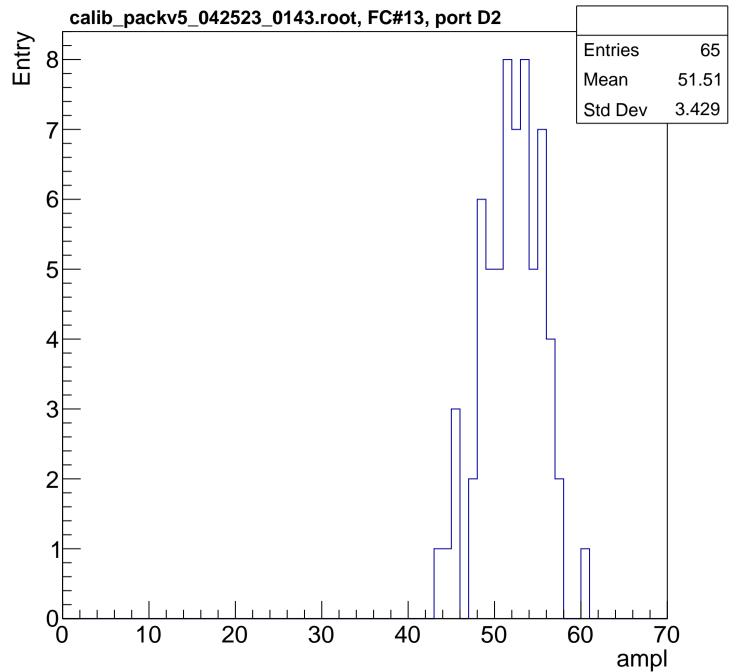


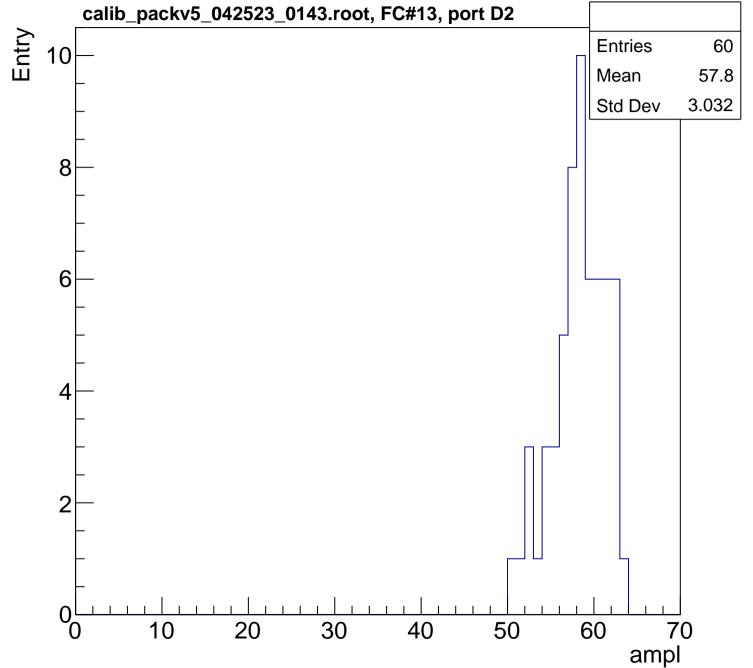
B1L003S, U9-ch86, adc7 calib\_packv5\_042523\_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

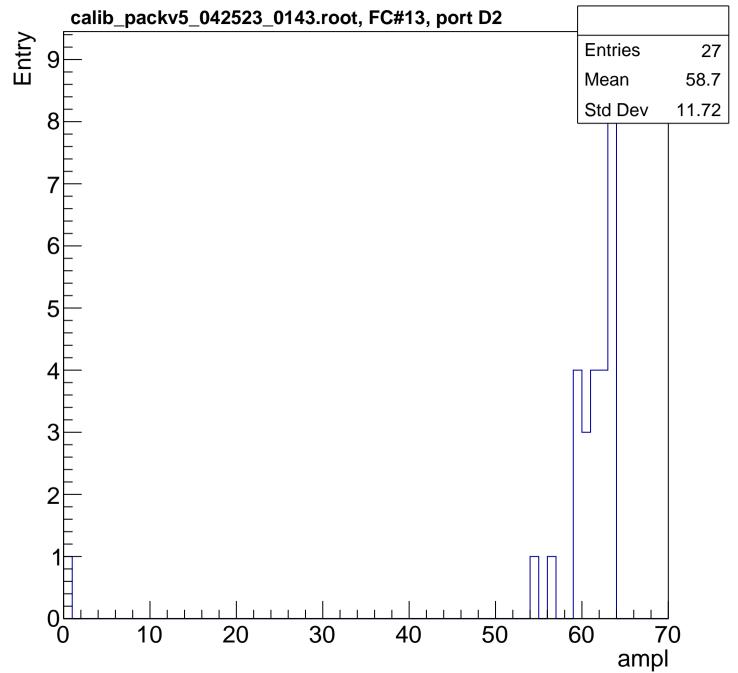


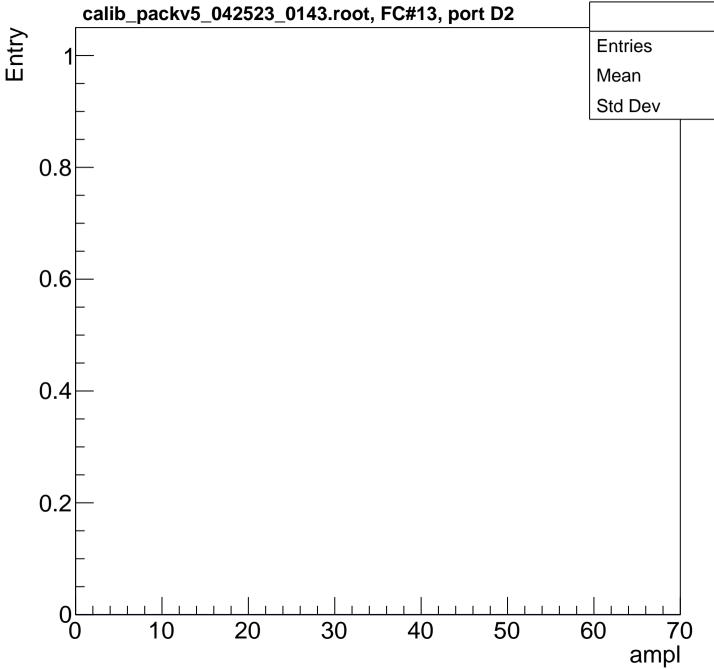


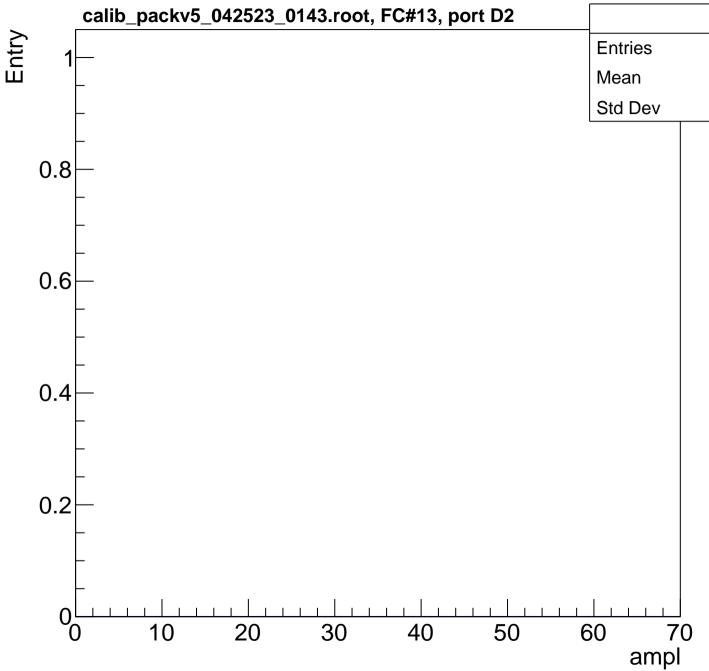


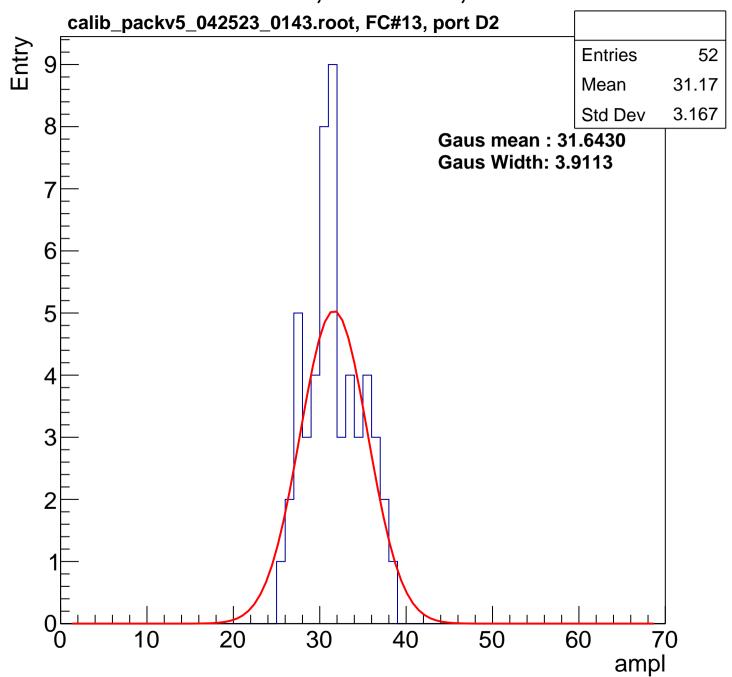


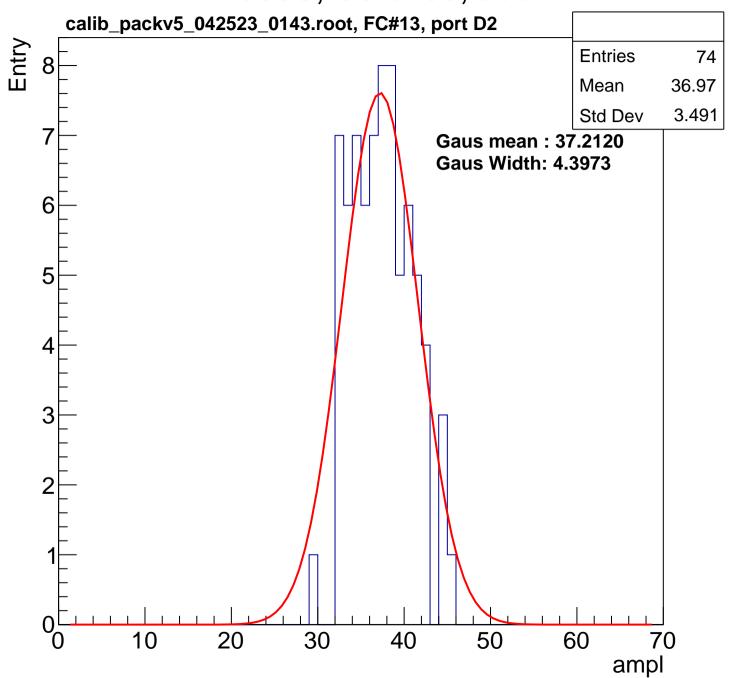


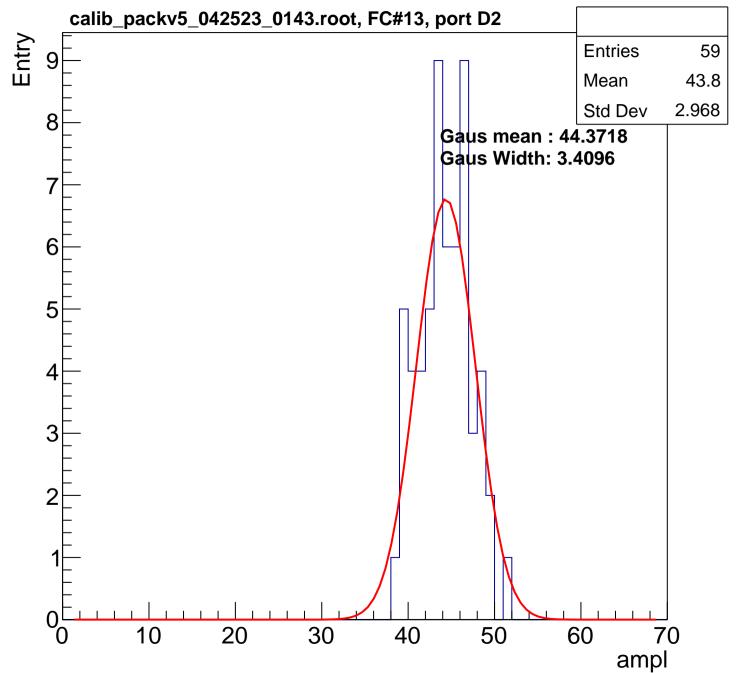


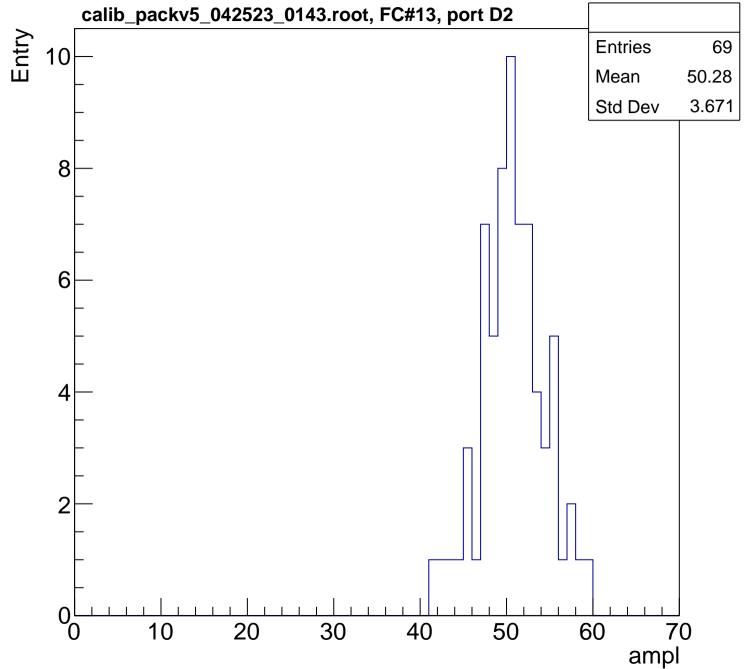


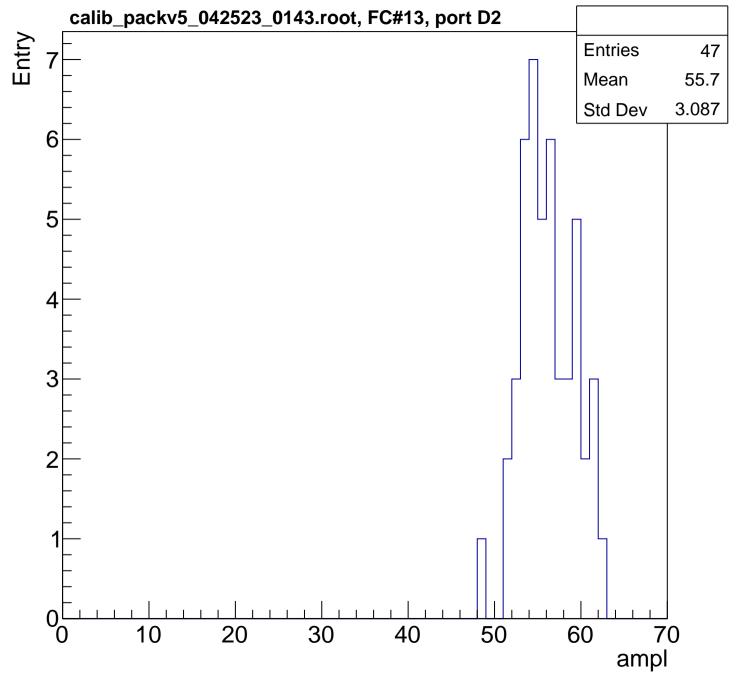


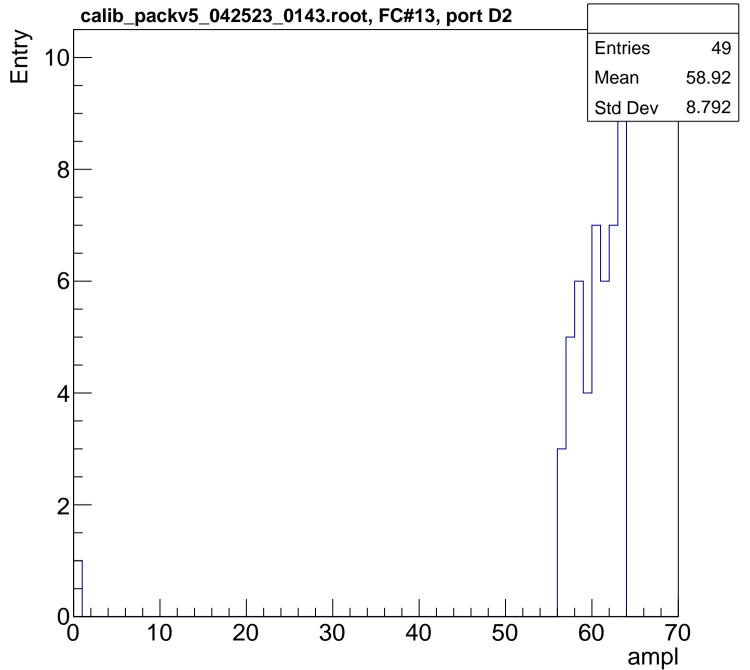


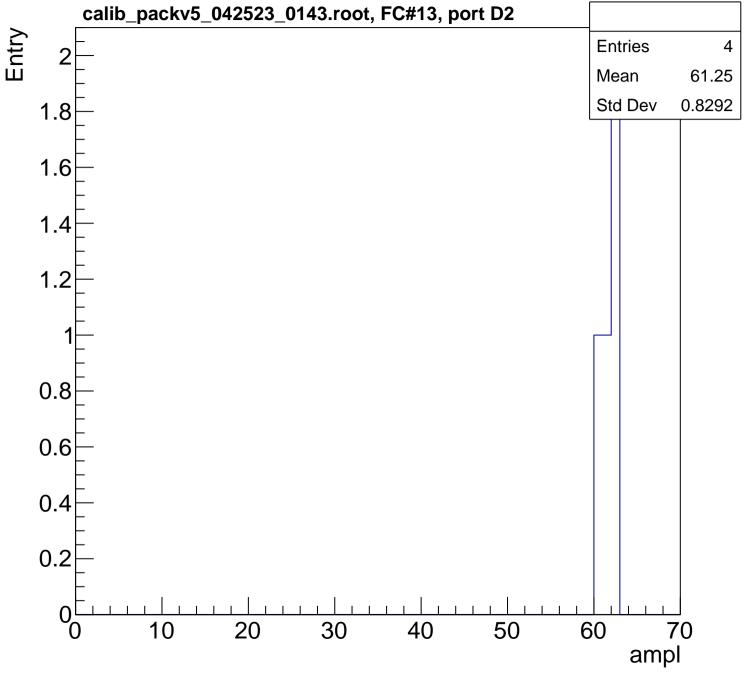


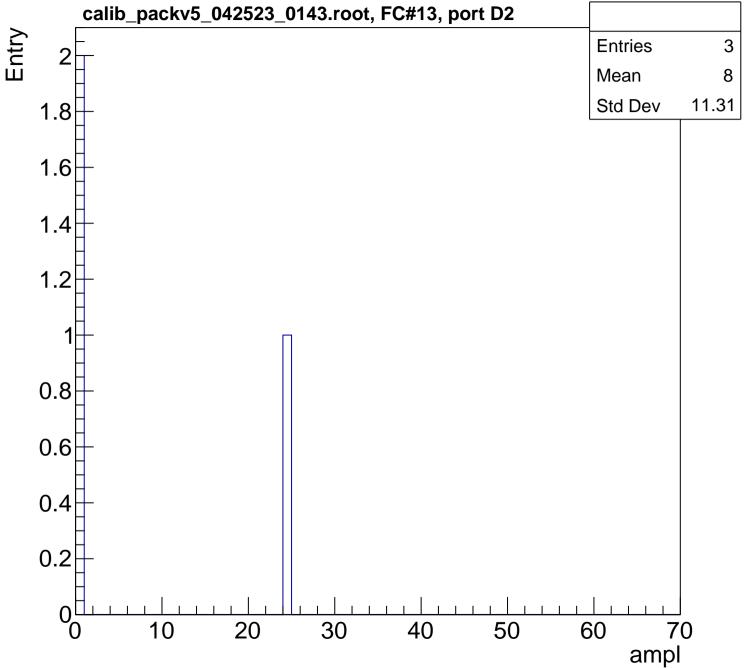


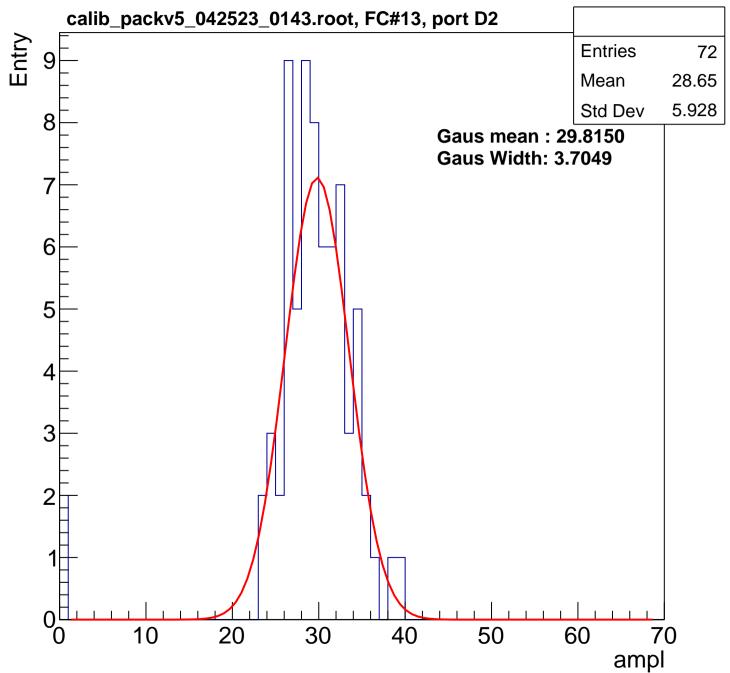


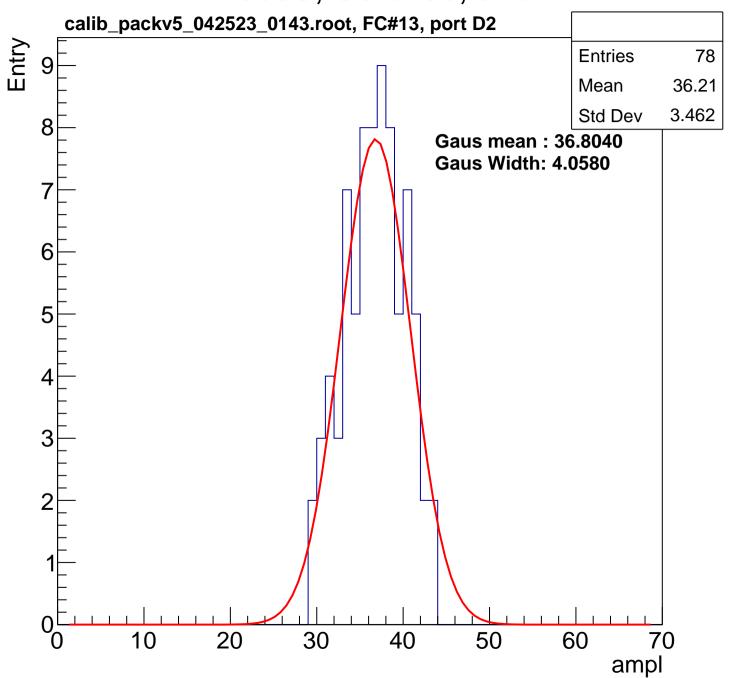


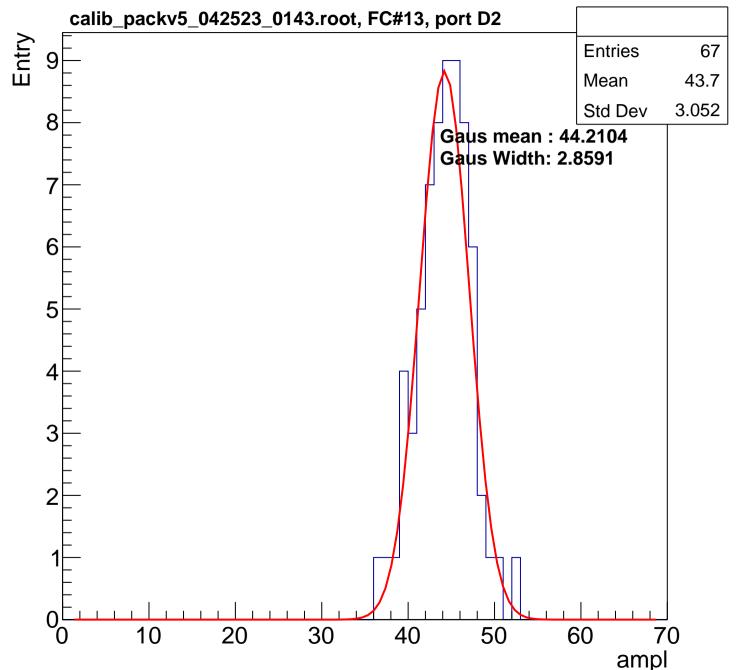


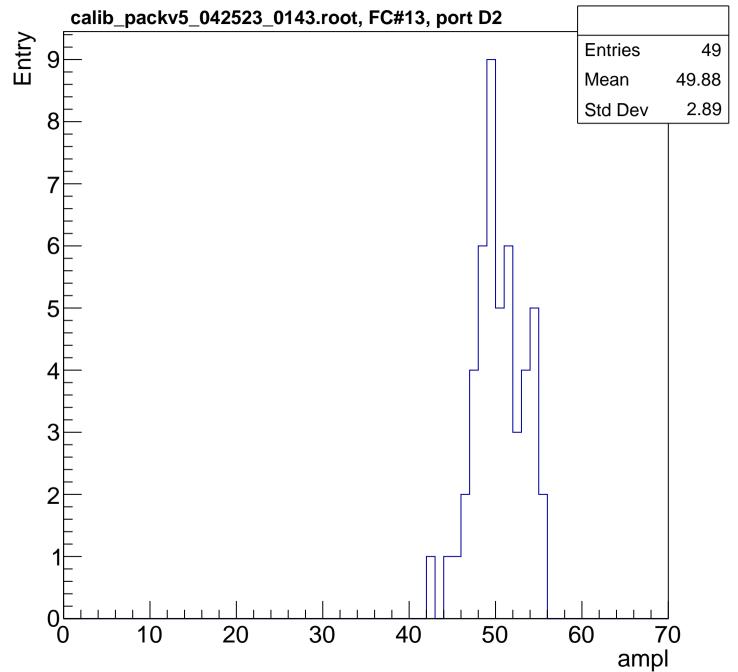


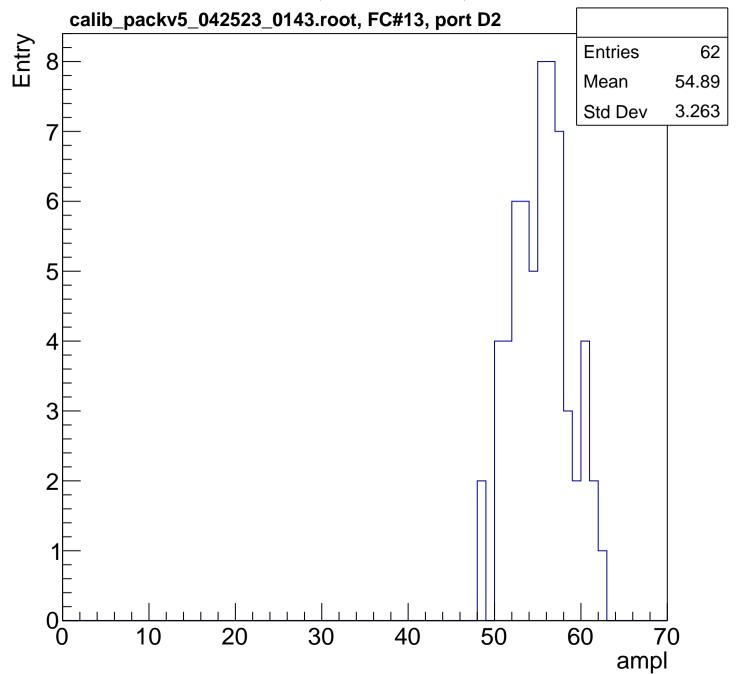


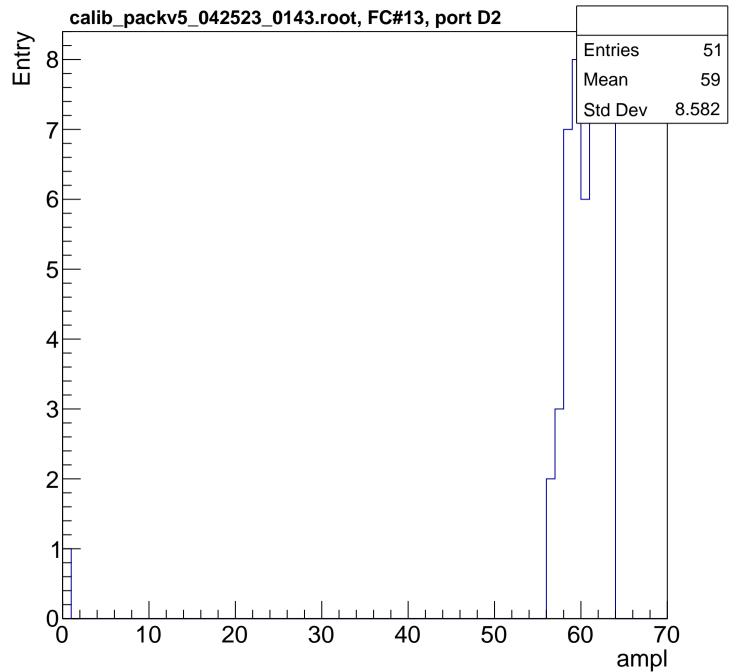


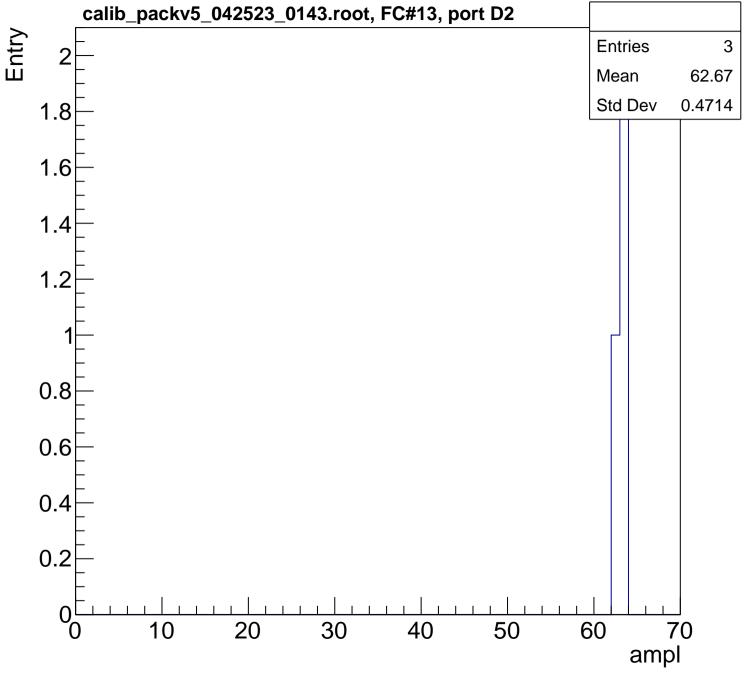




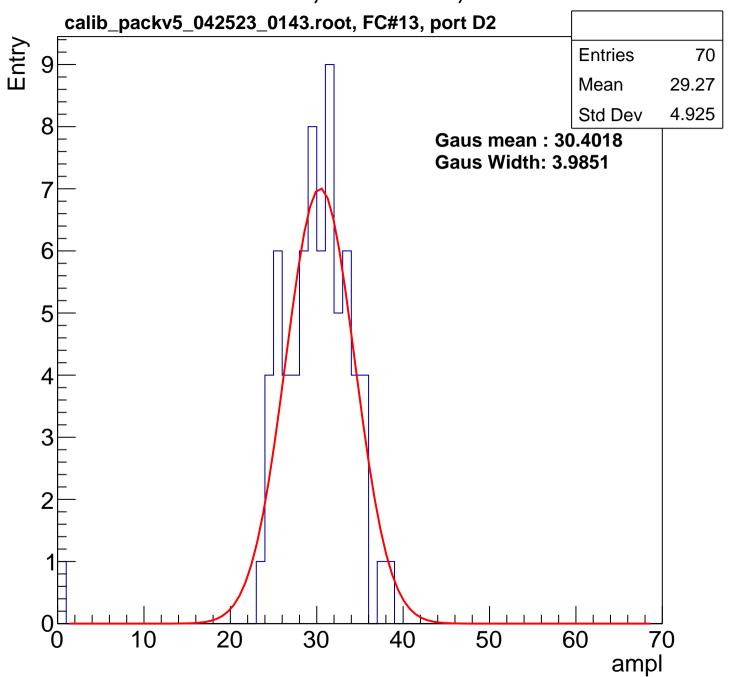


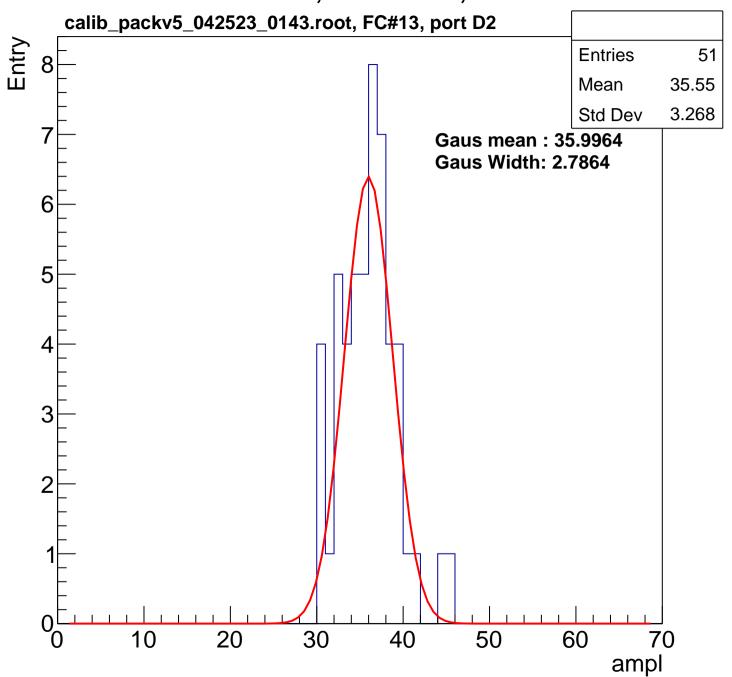


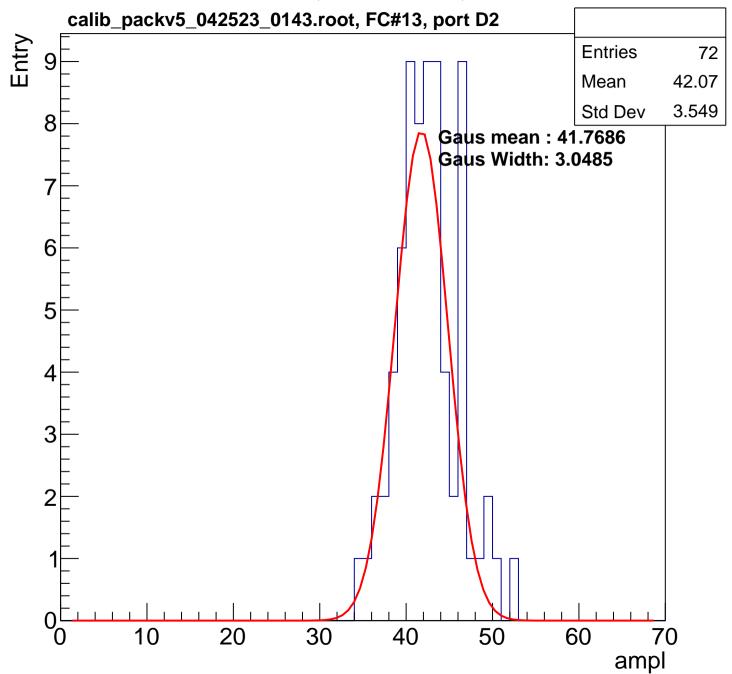


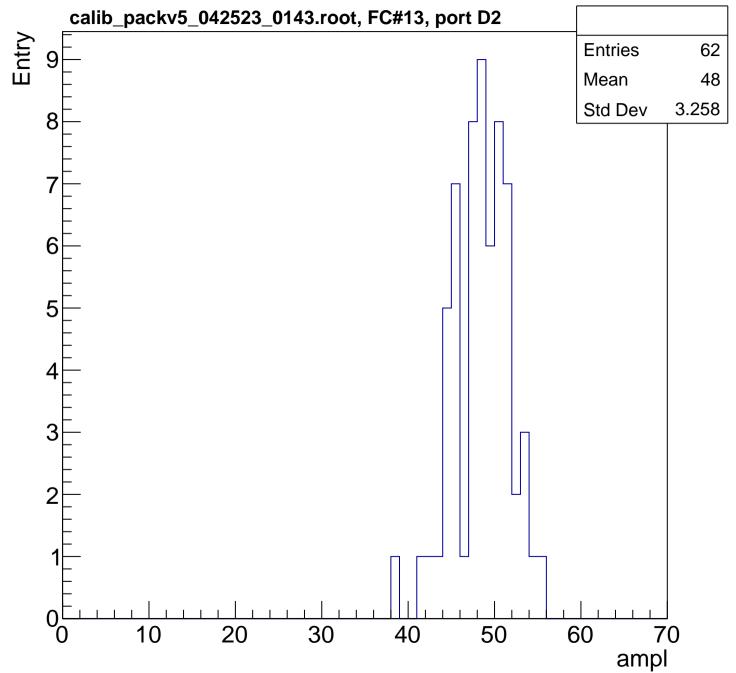


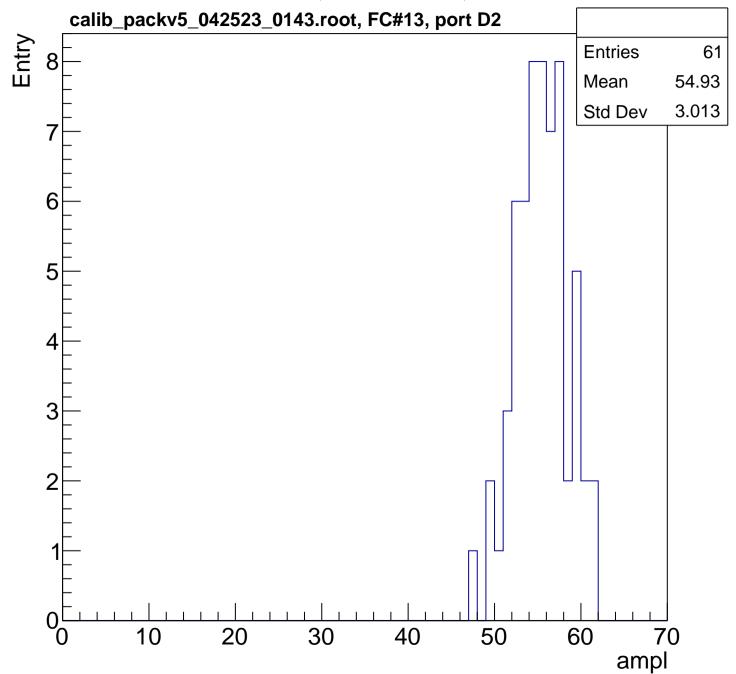


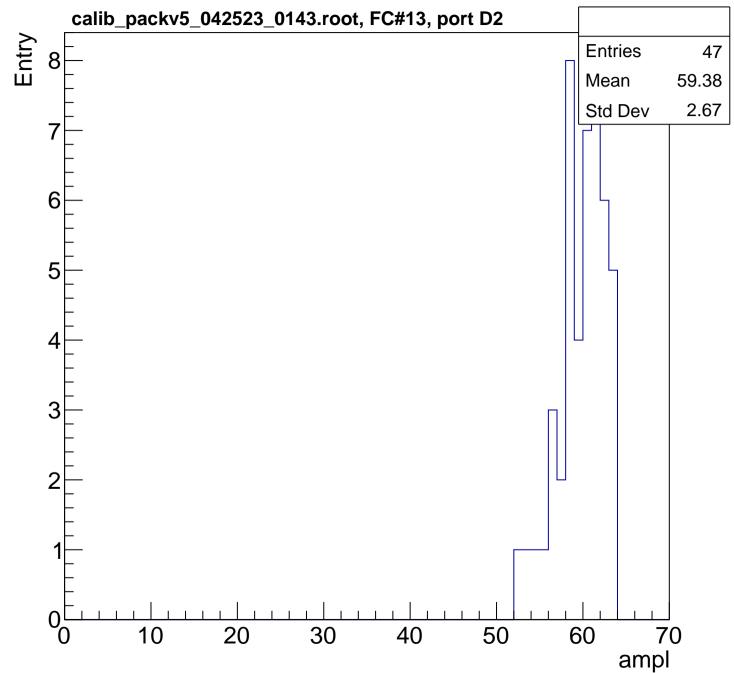


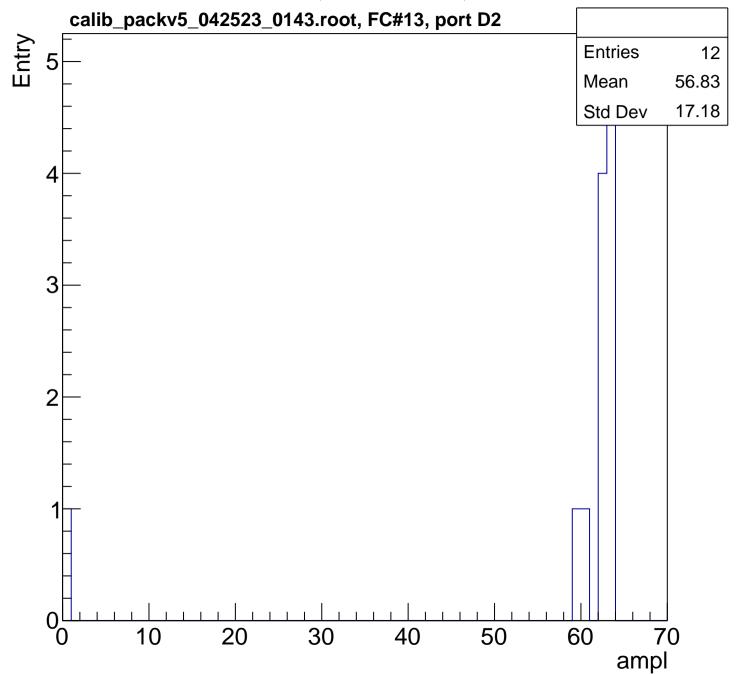


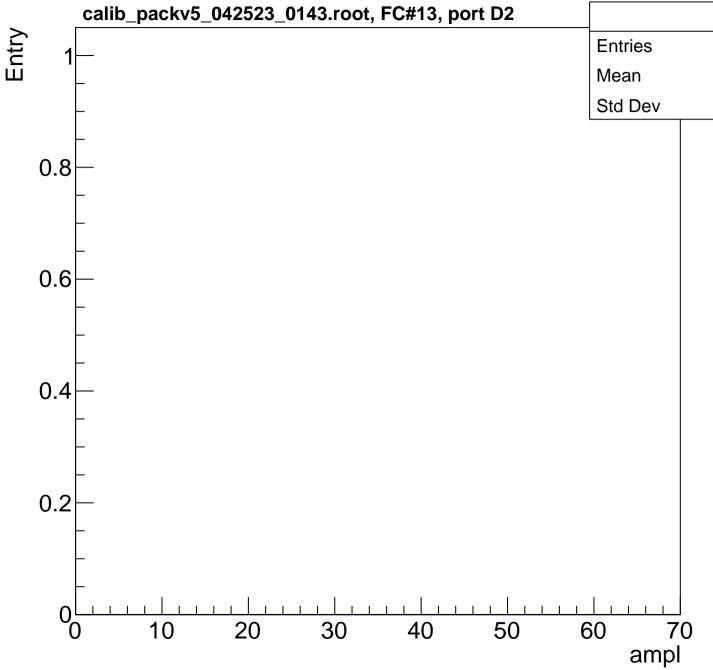


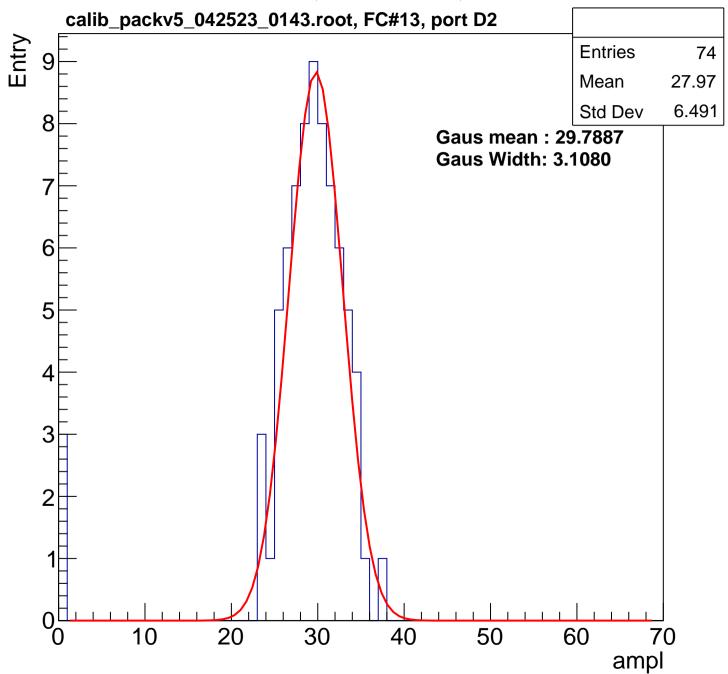


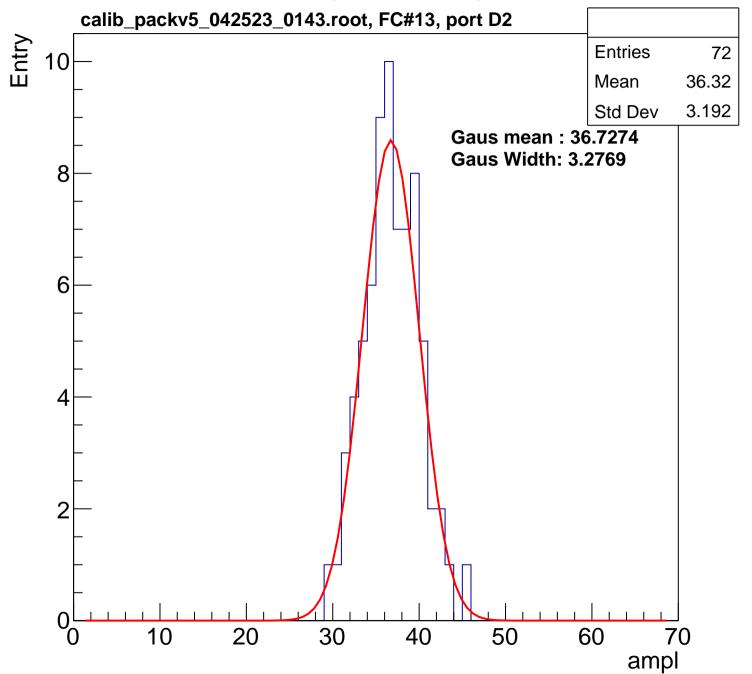


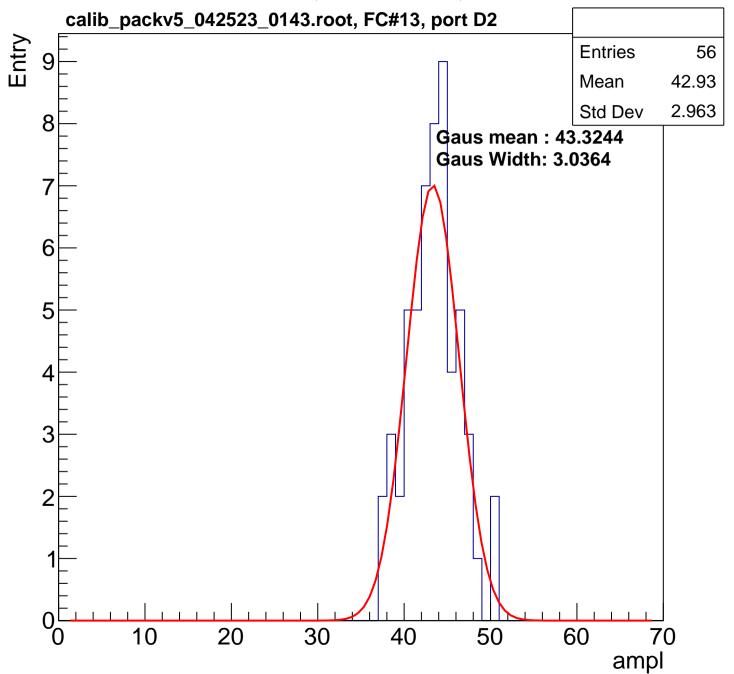


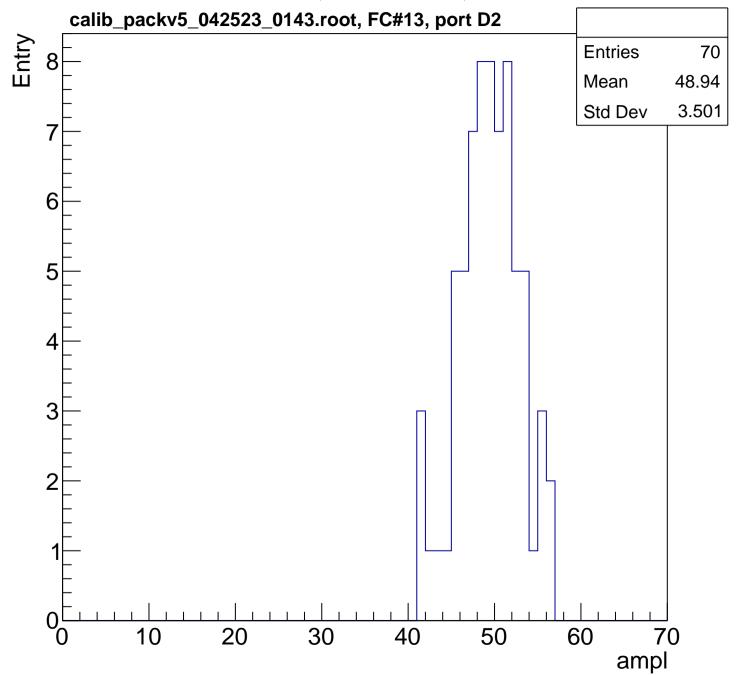


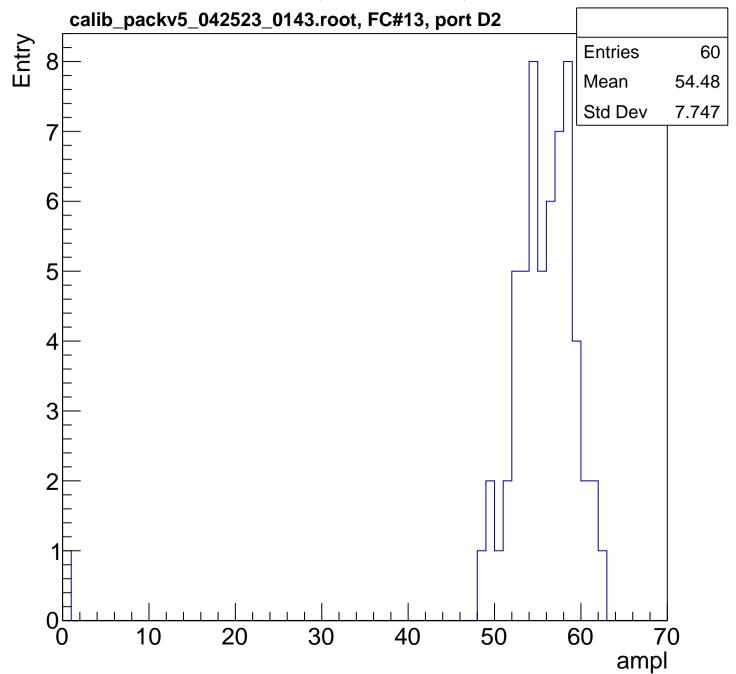


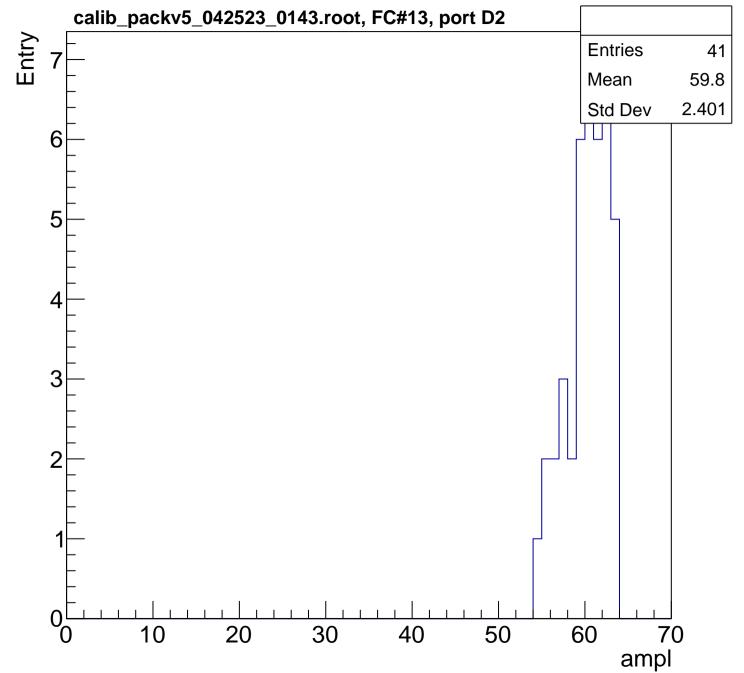


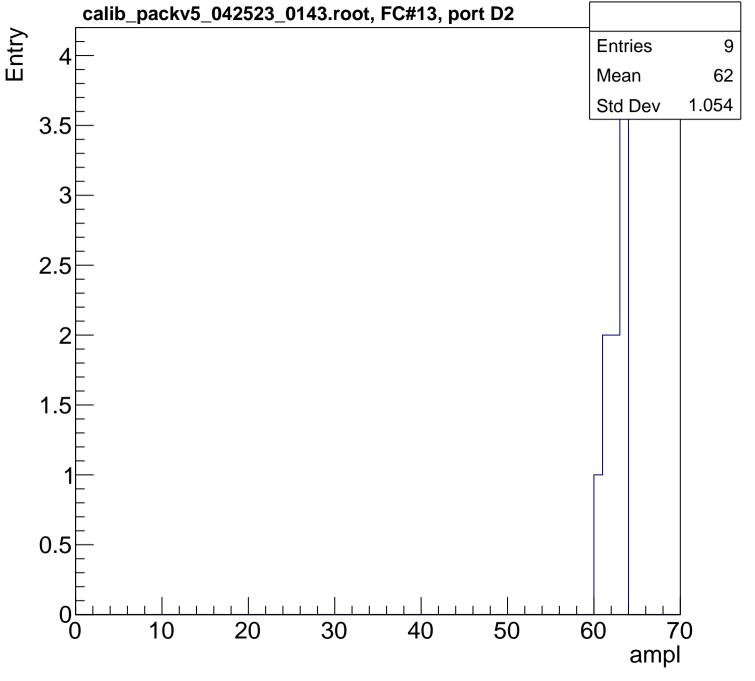


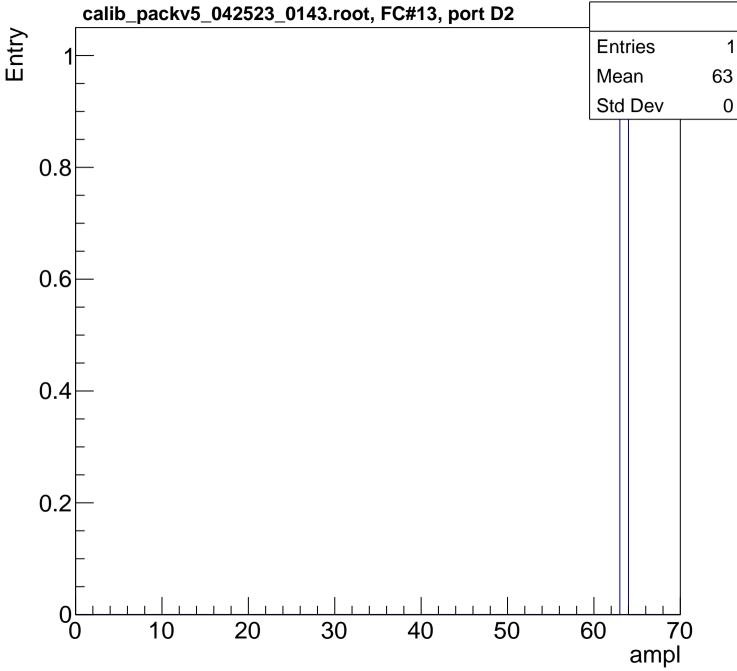


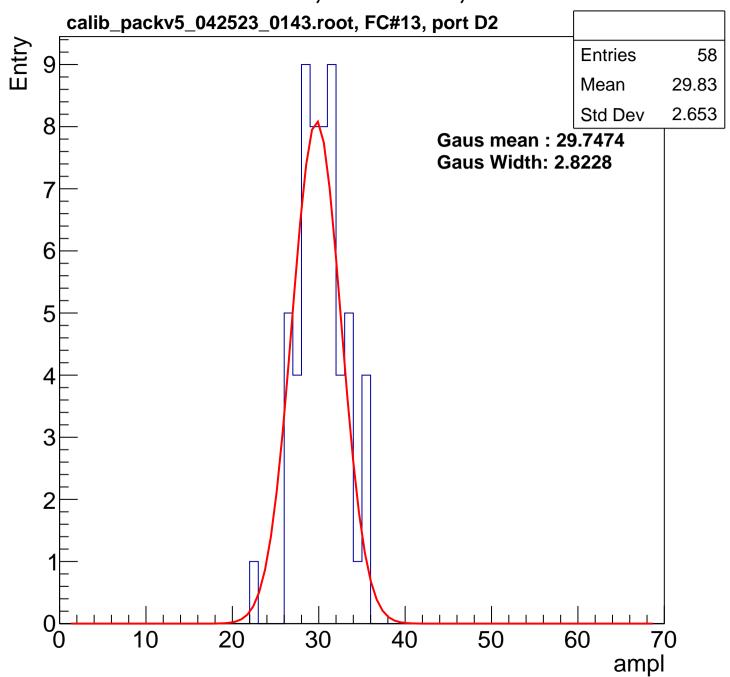


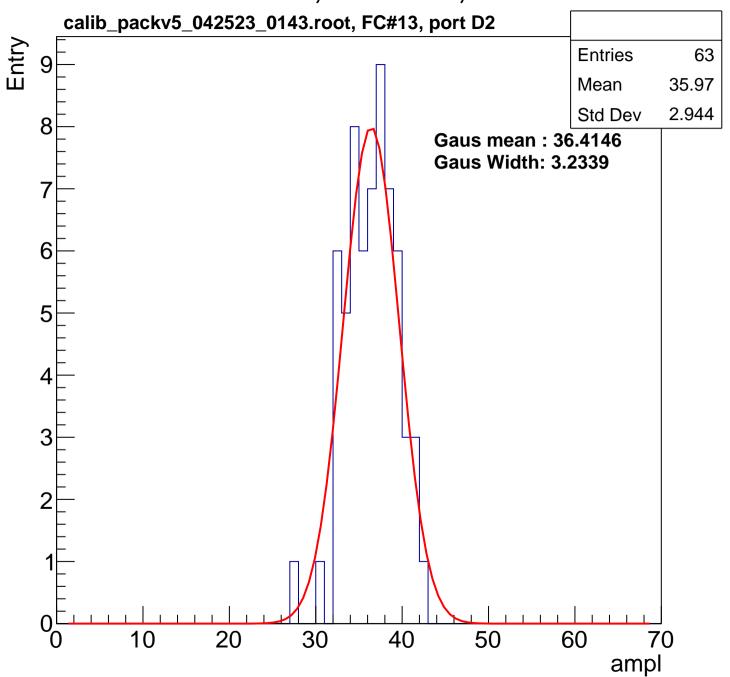


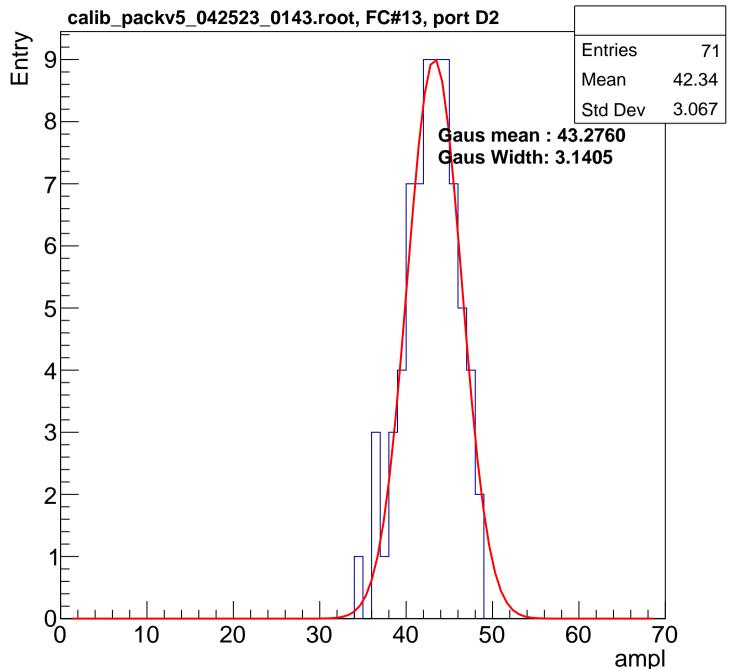


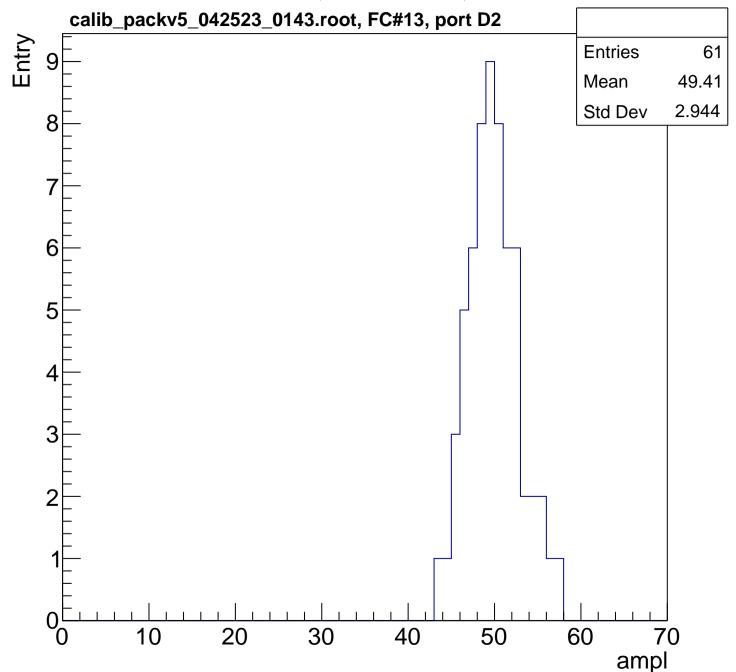


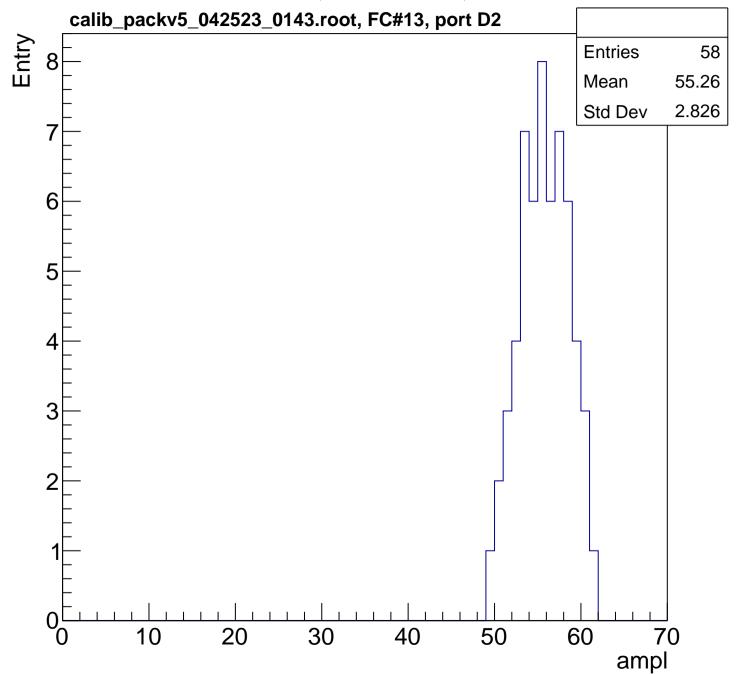


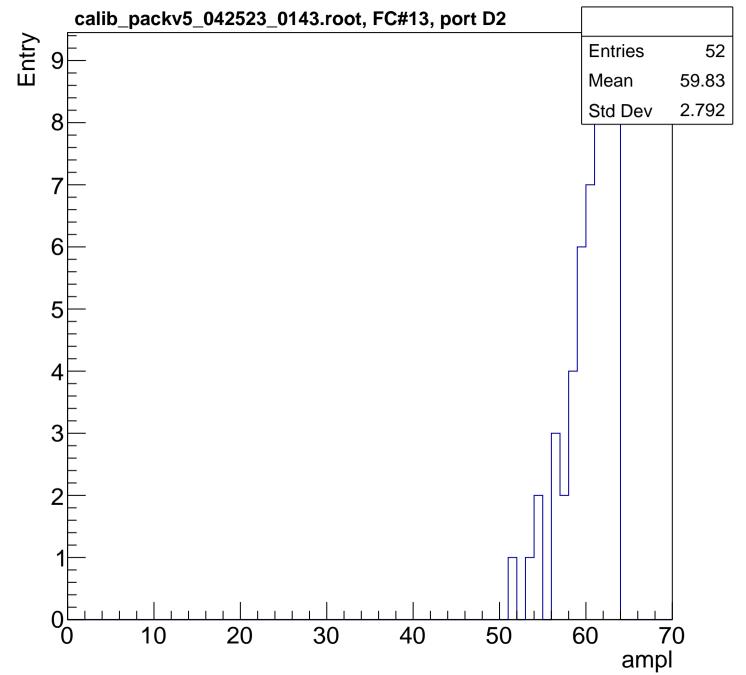


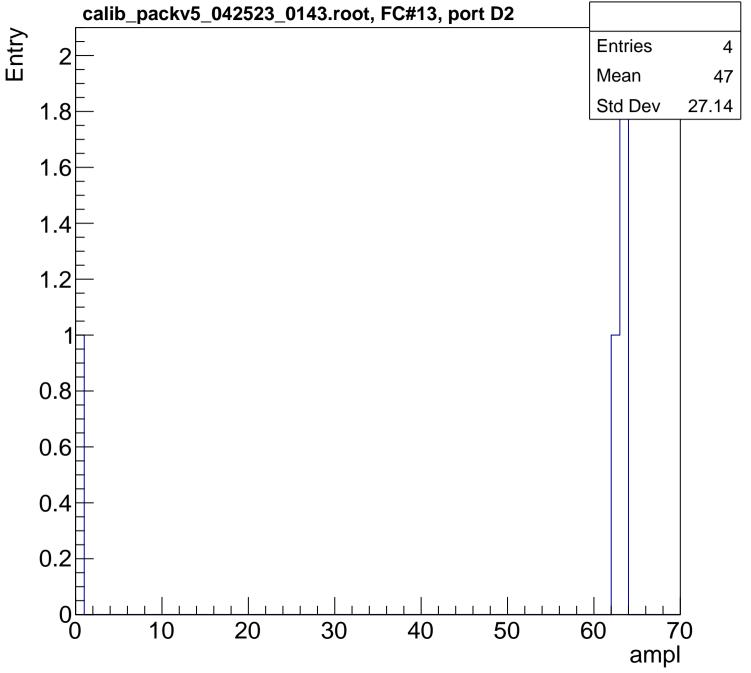




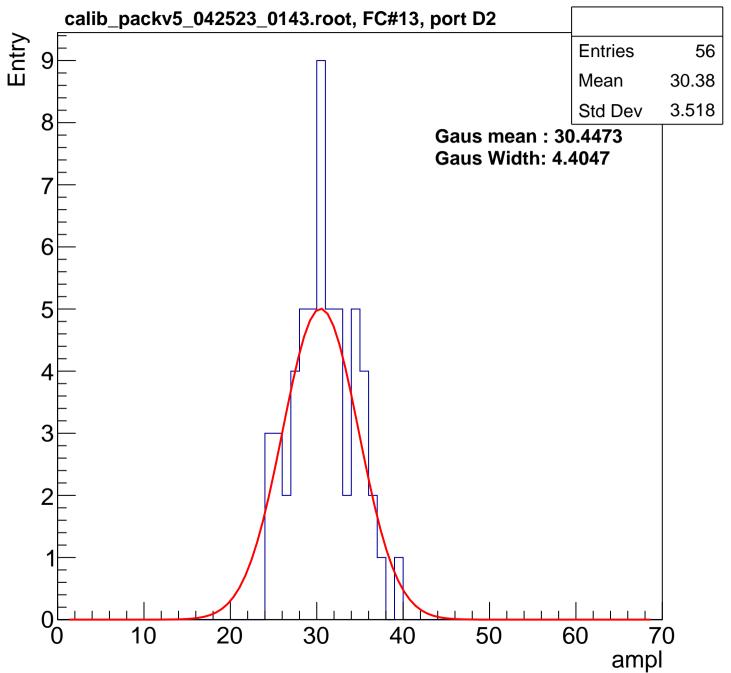


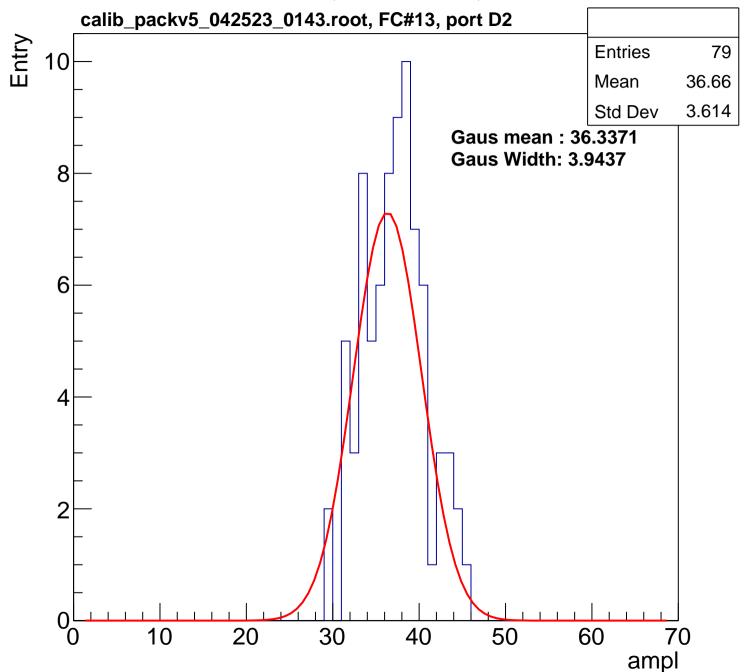


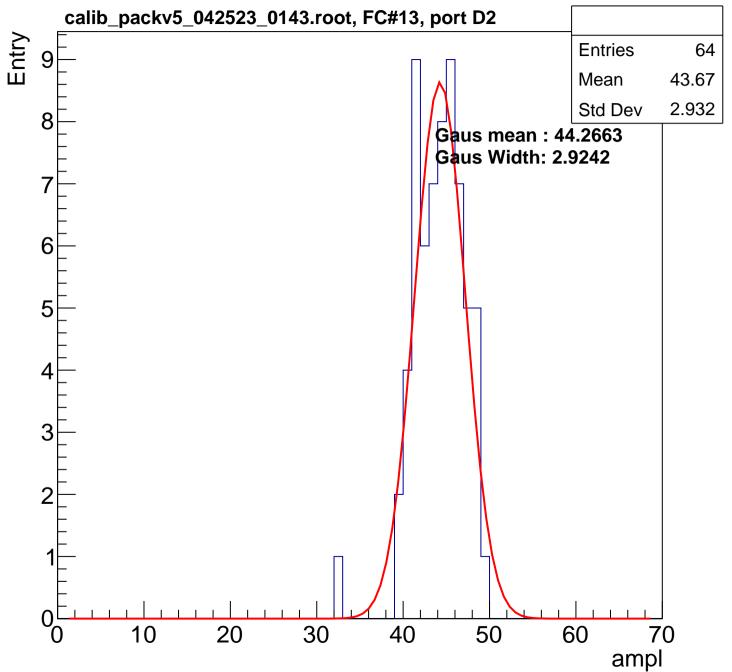


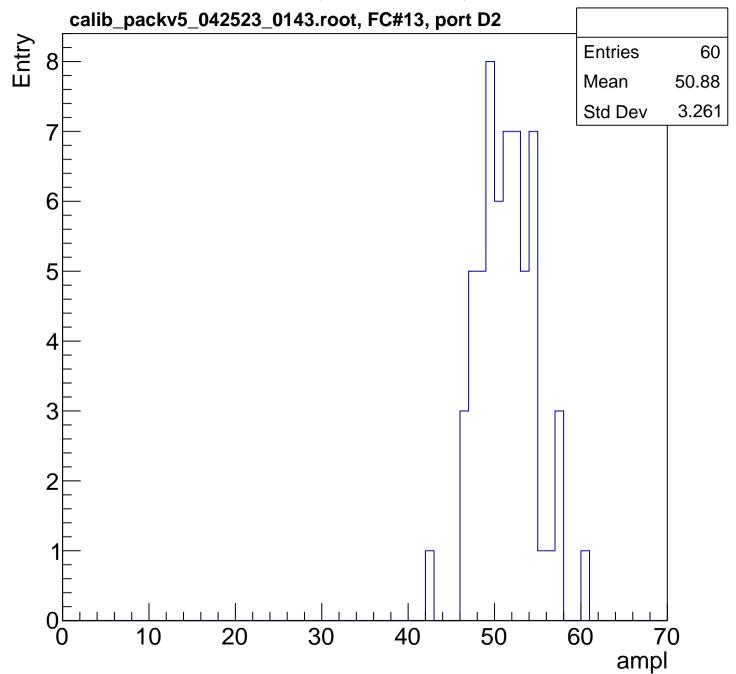


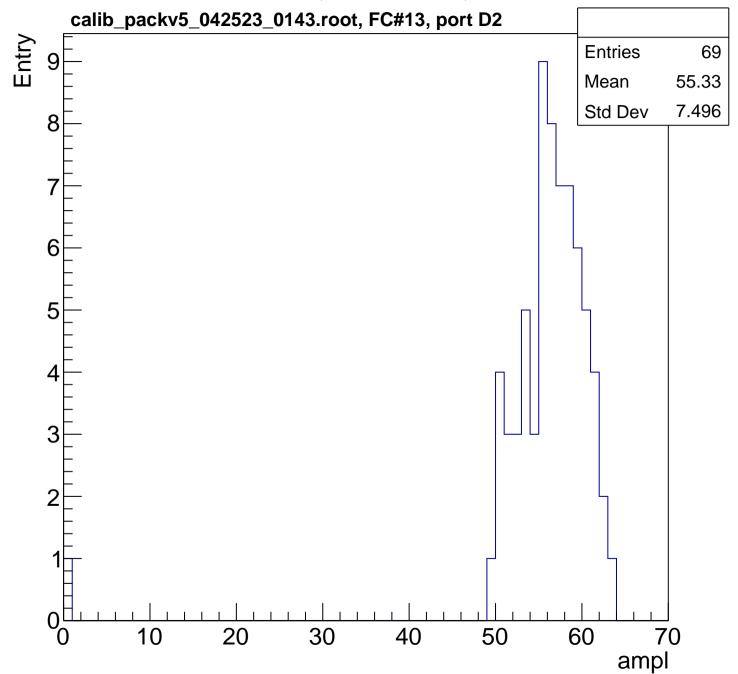
B1L003S, U9-ch92, adc7 calib\_packv5\_042523\_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

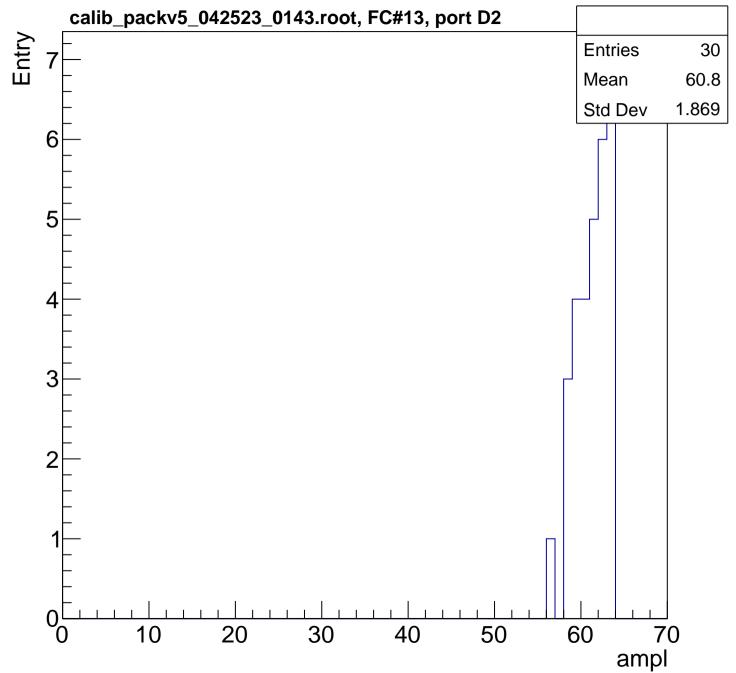


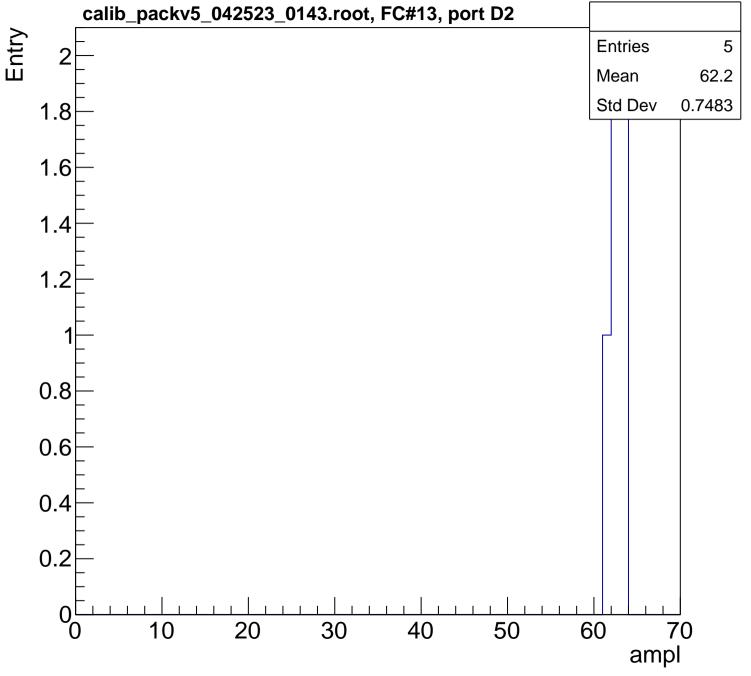


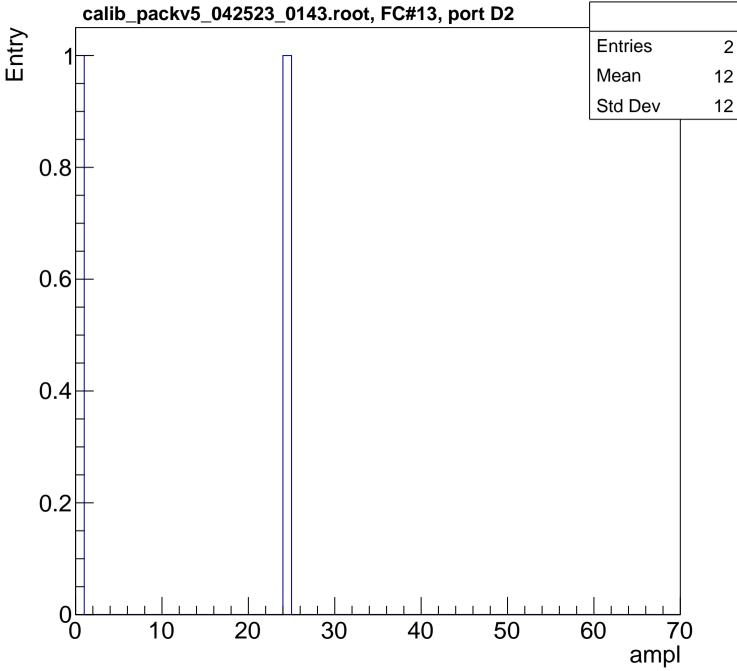


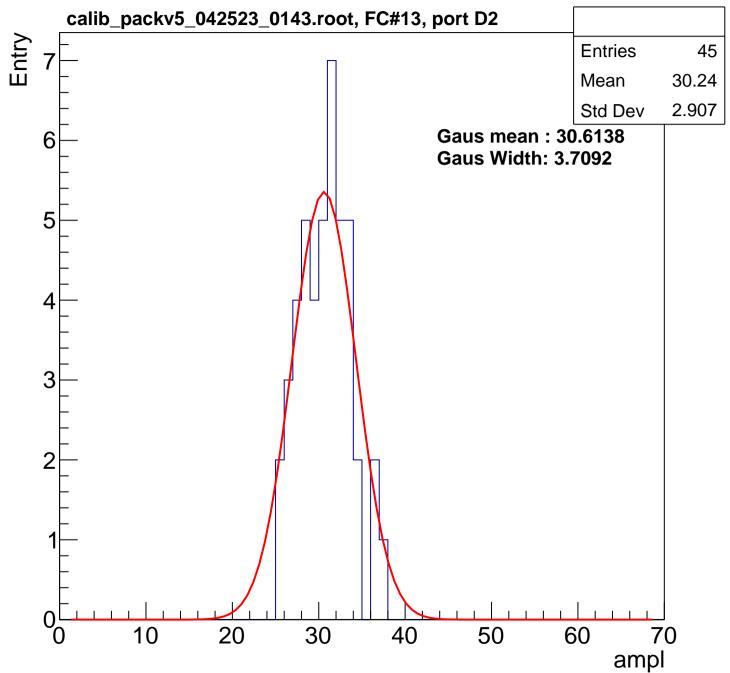


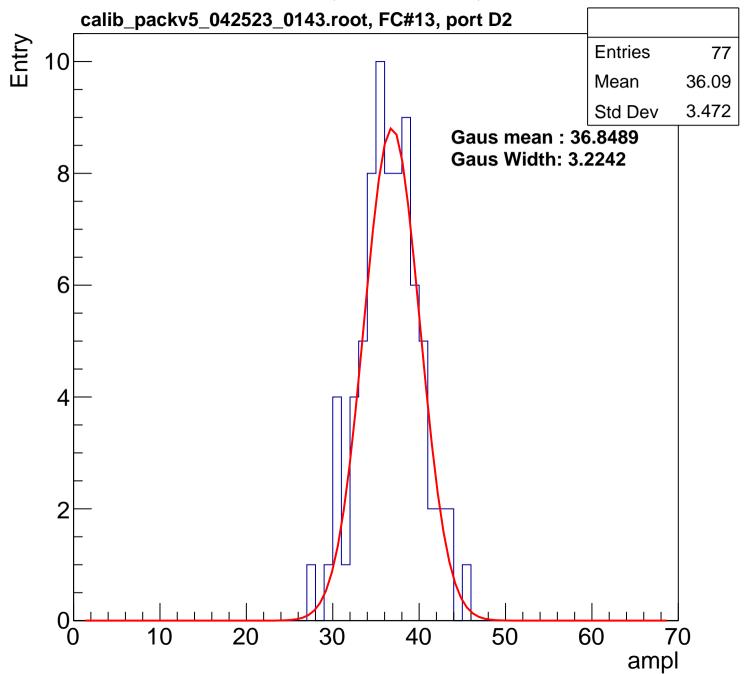


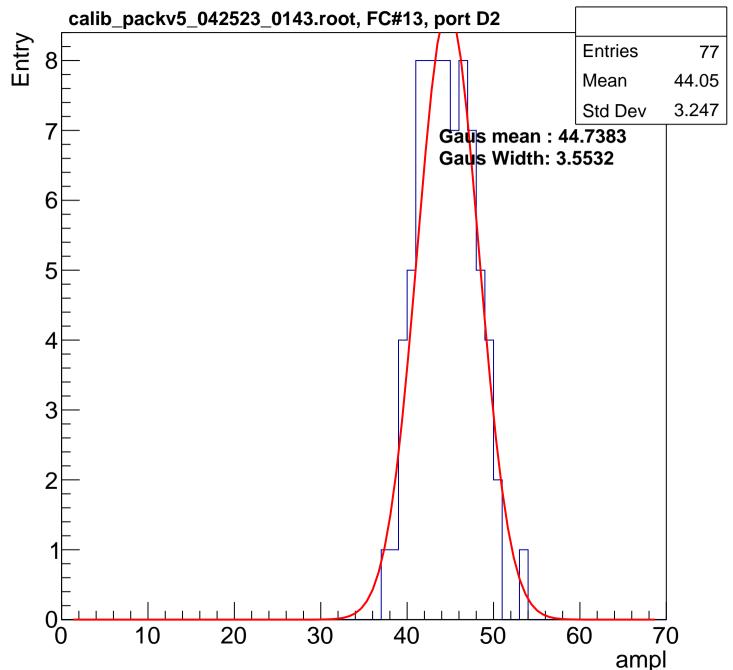


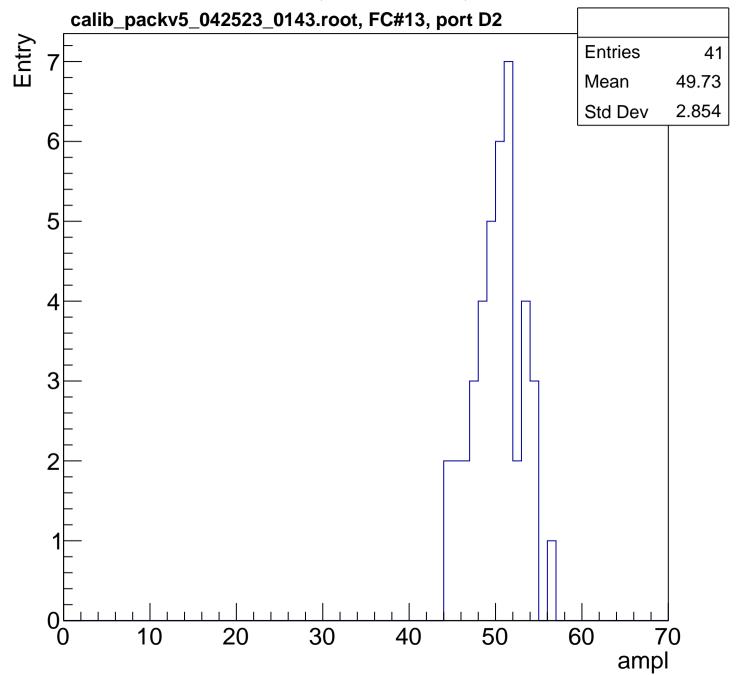


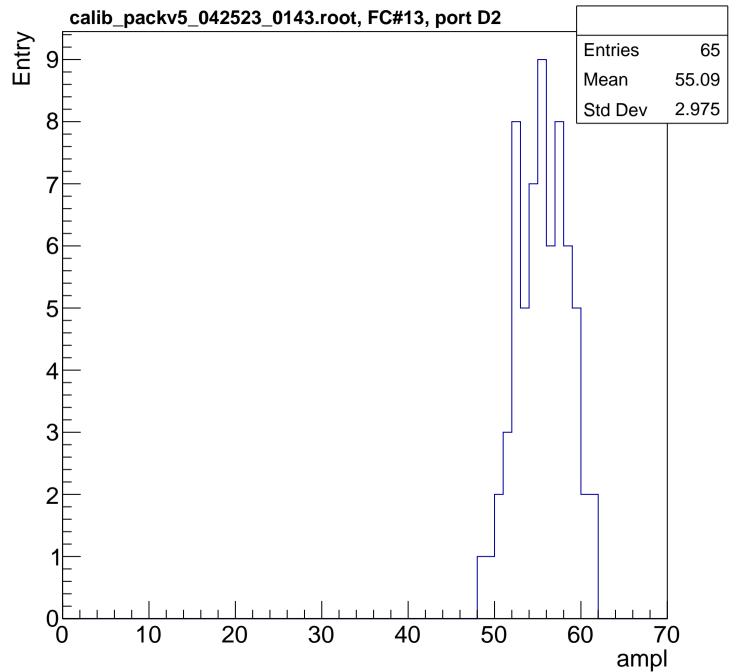


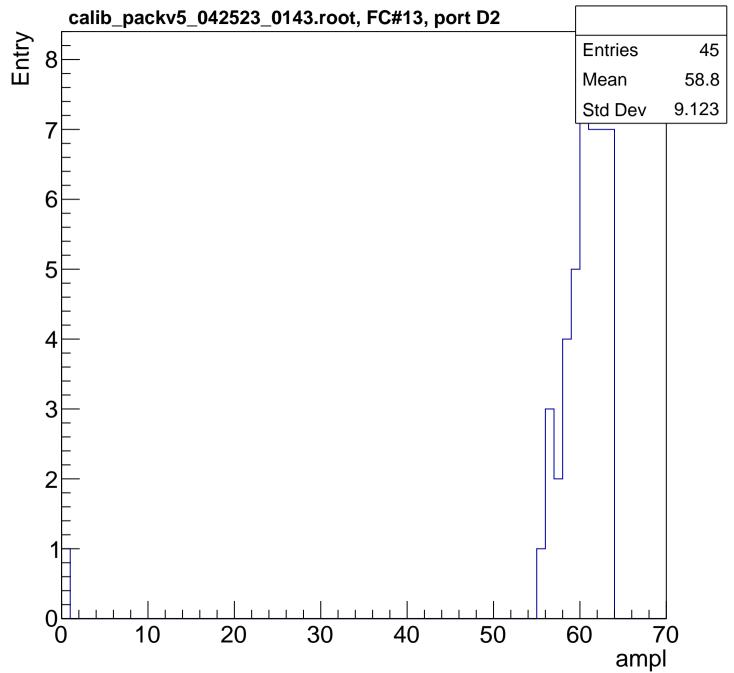


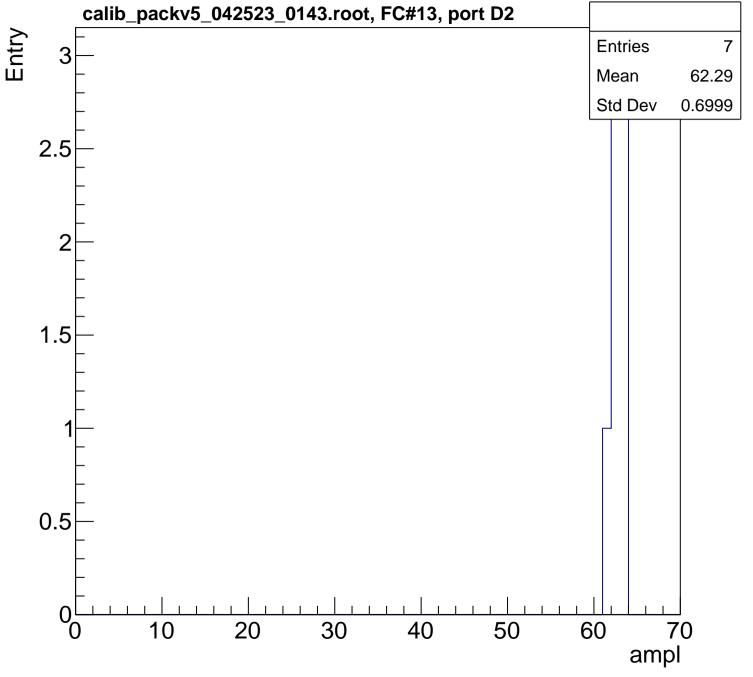




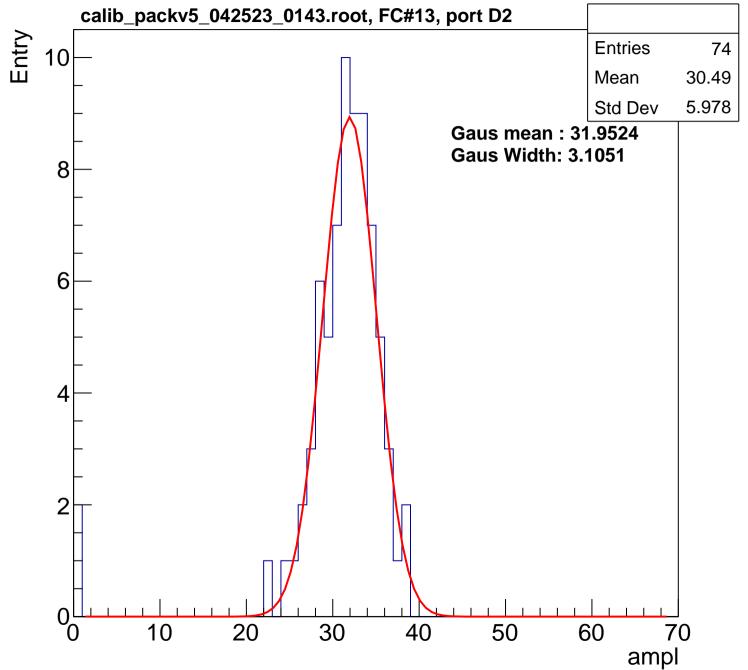


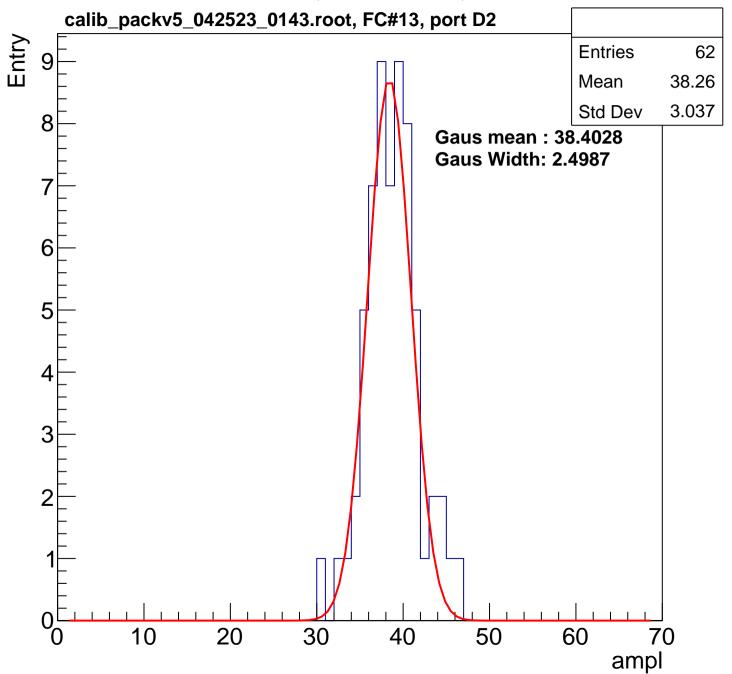


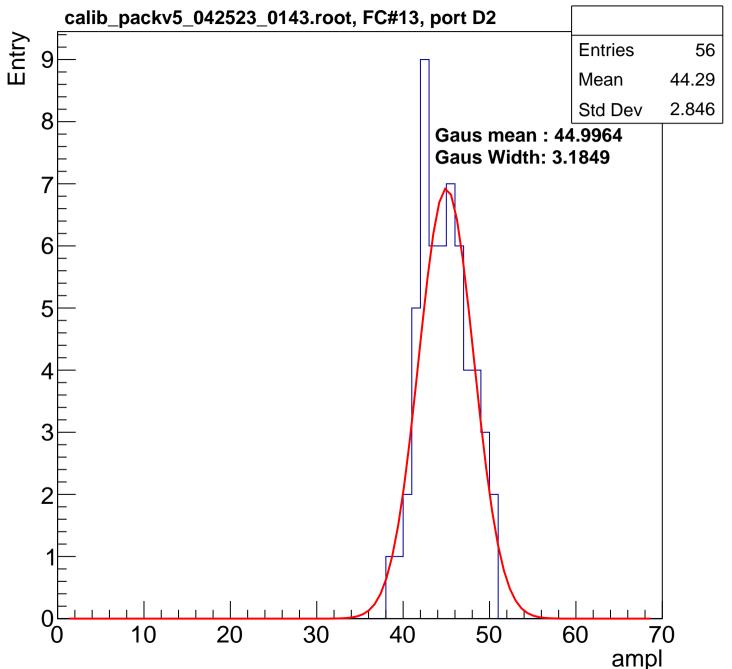


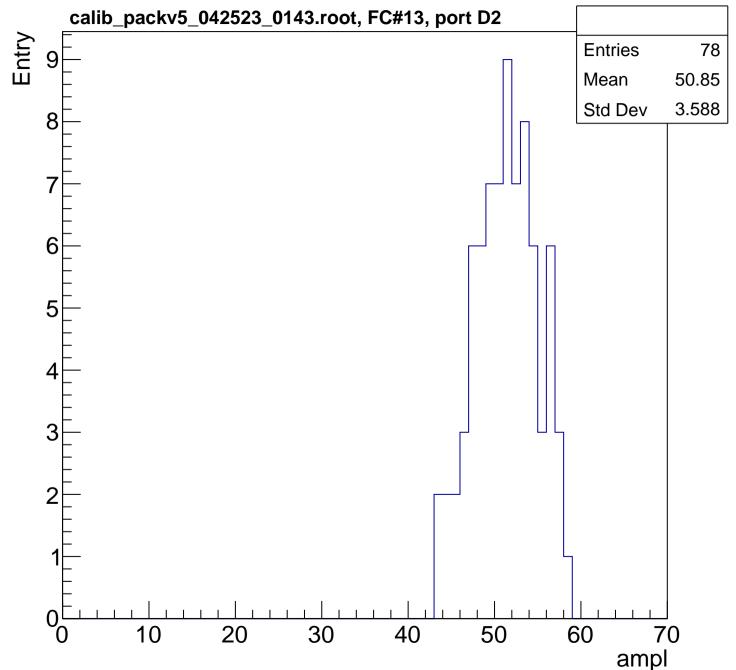


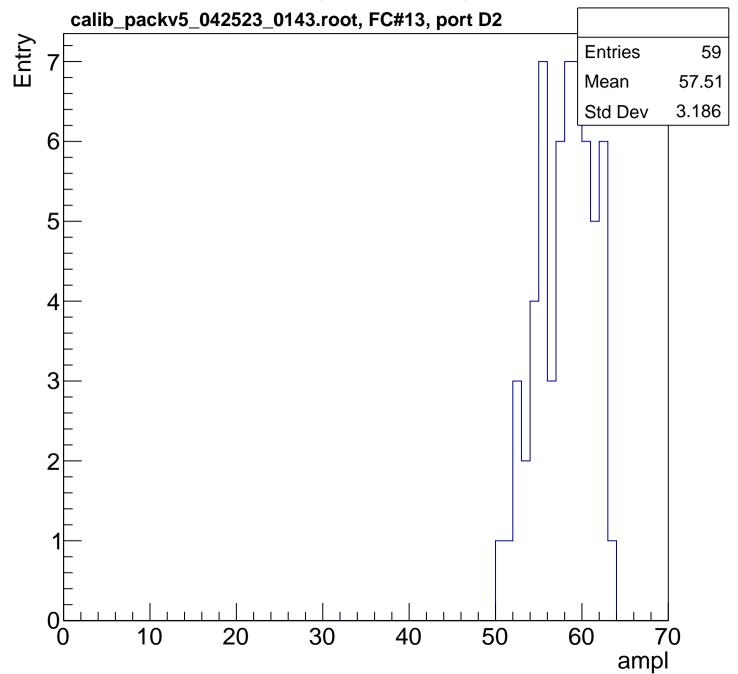
B1L003S, U9-ch94, adc7 calib\_packv5\_042523\_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

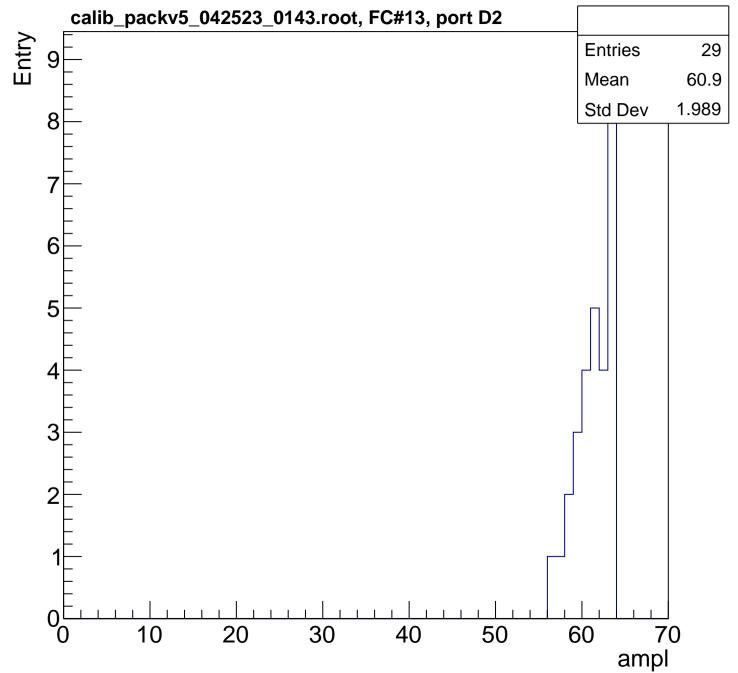






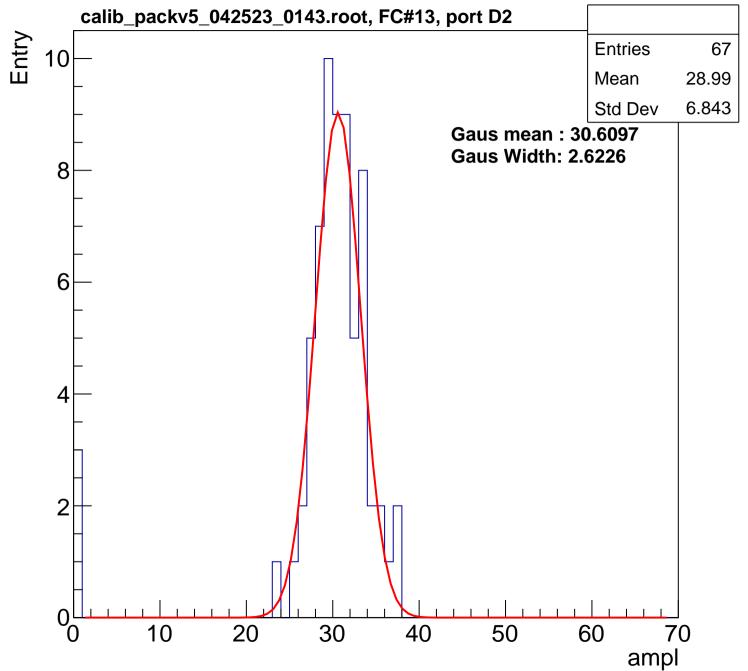


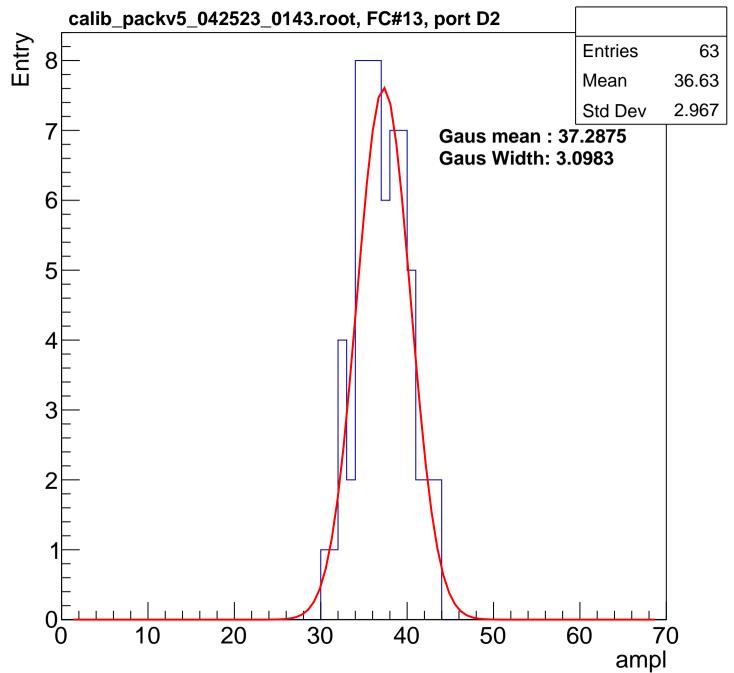


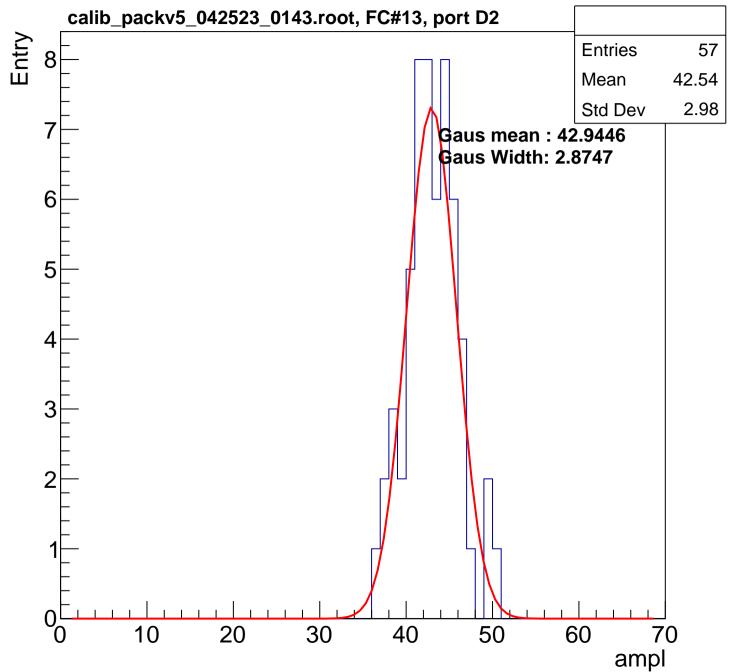


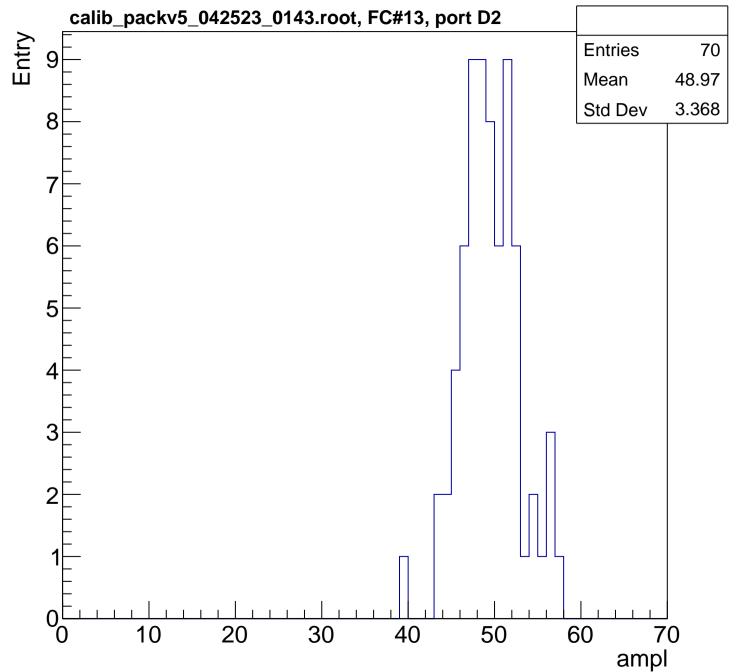


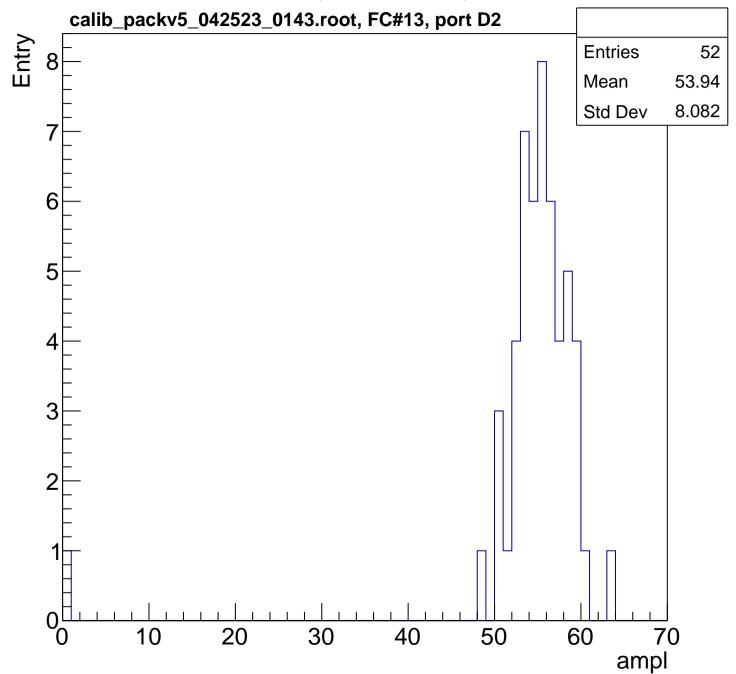


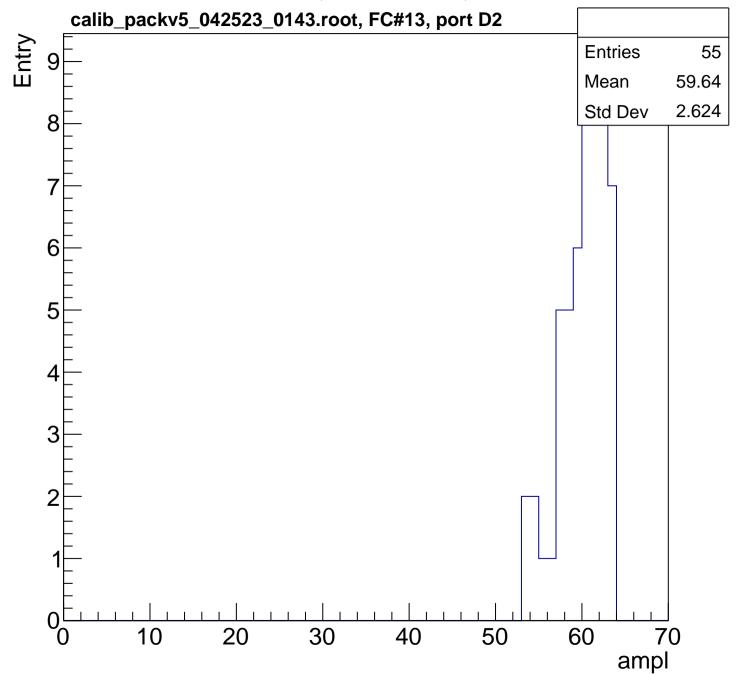


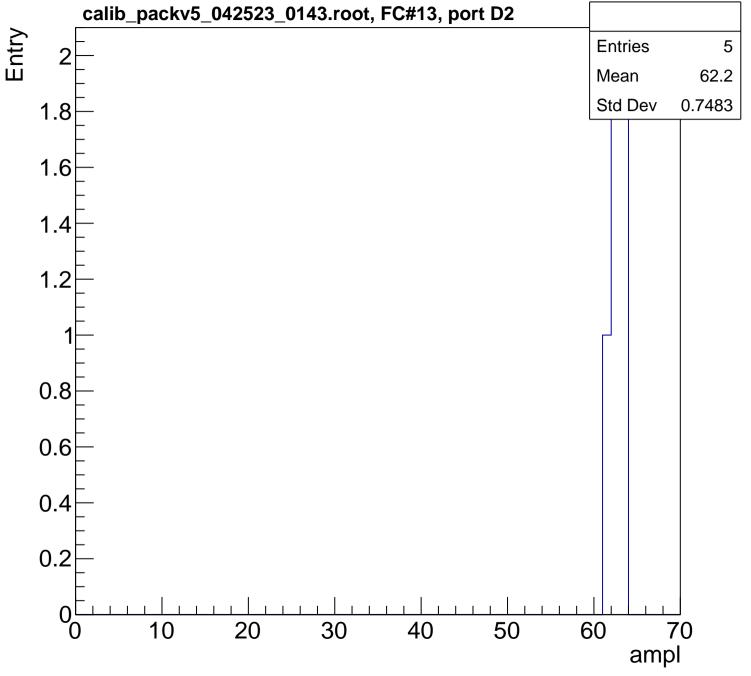


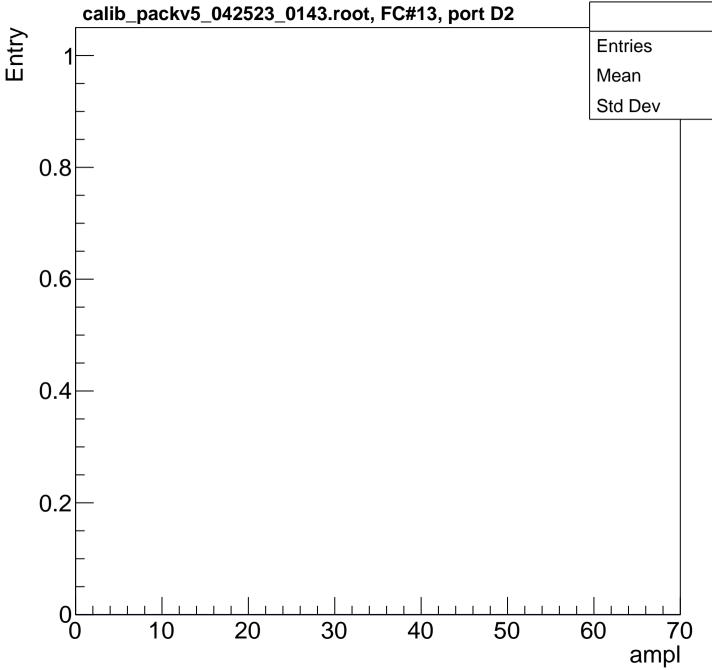


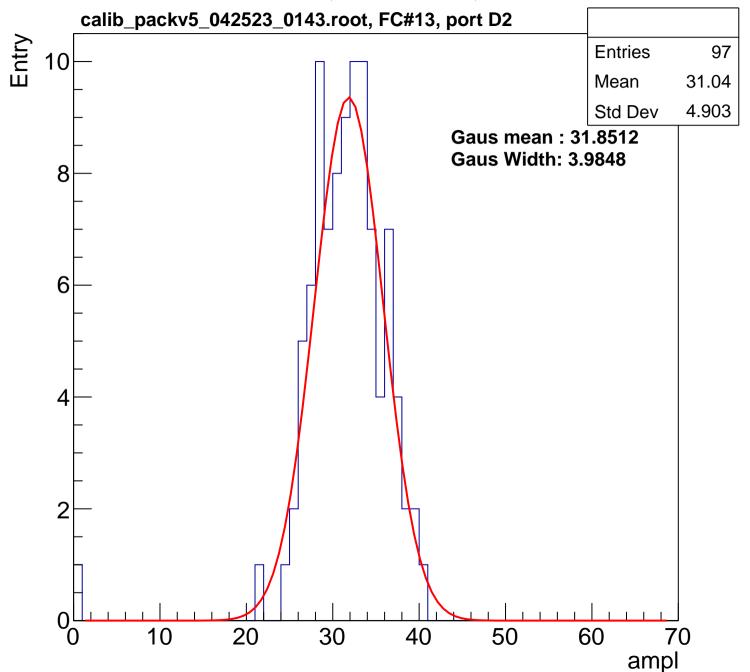


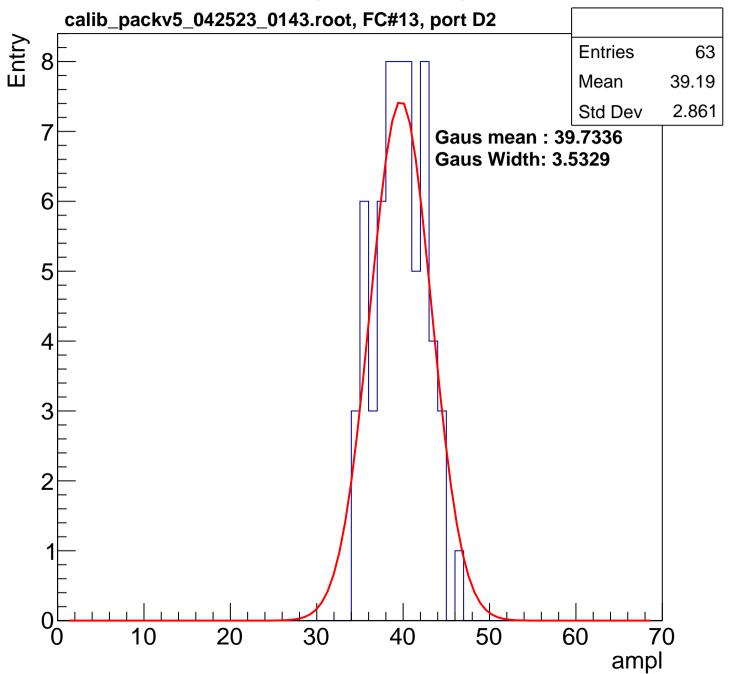


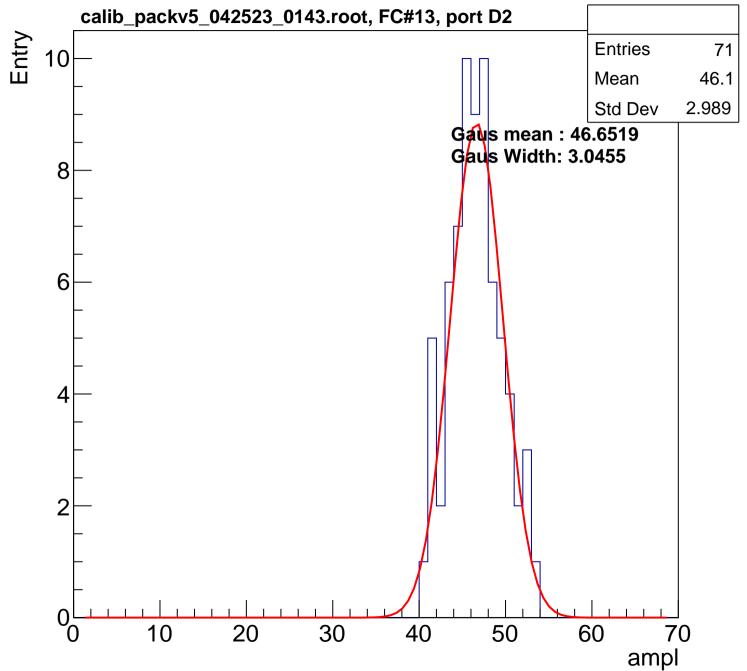


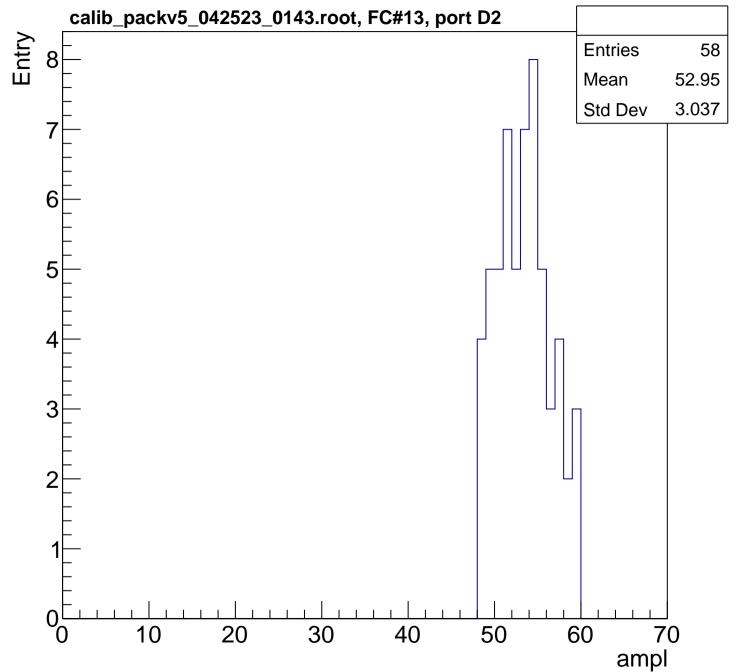


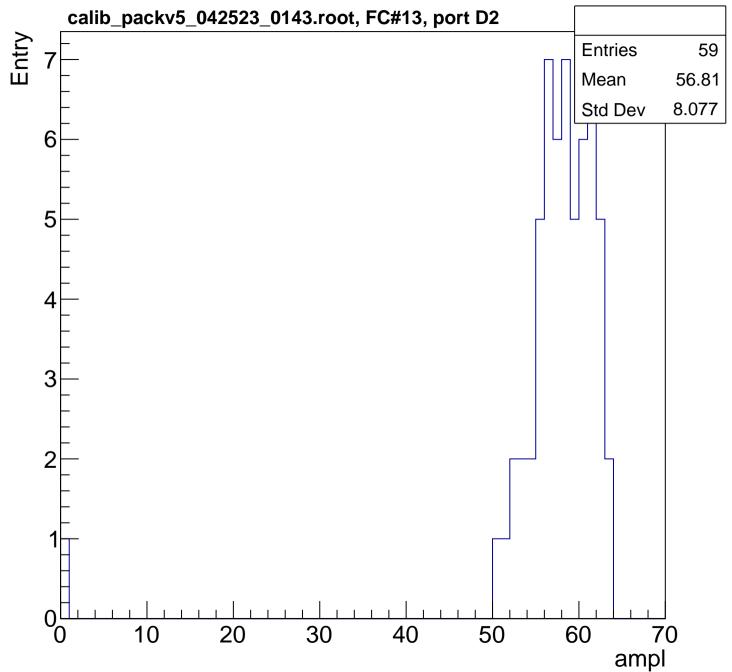


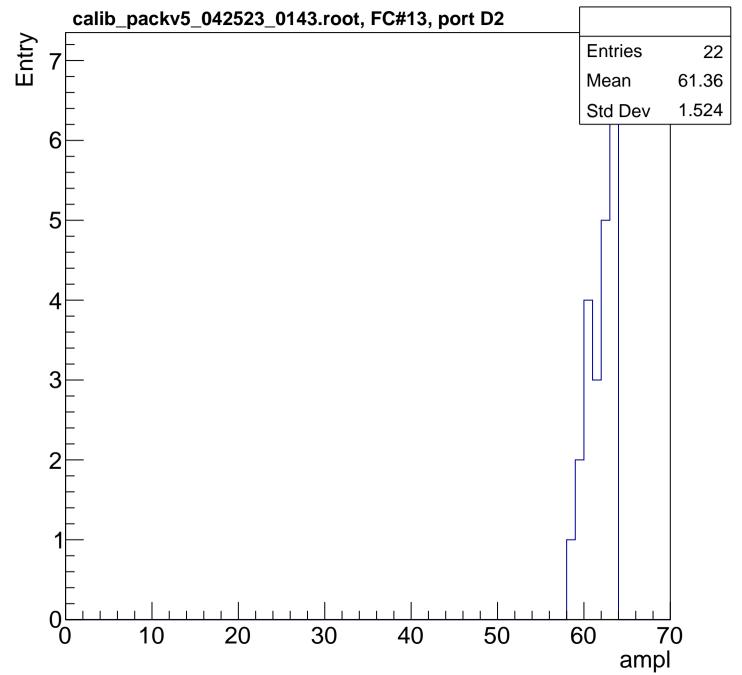


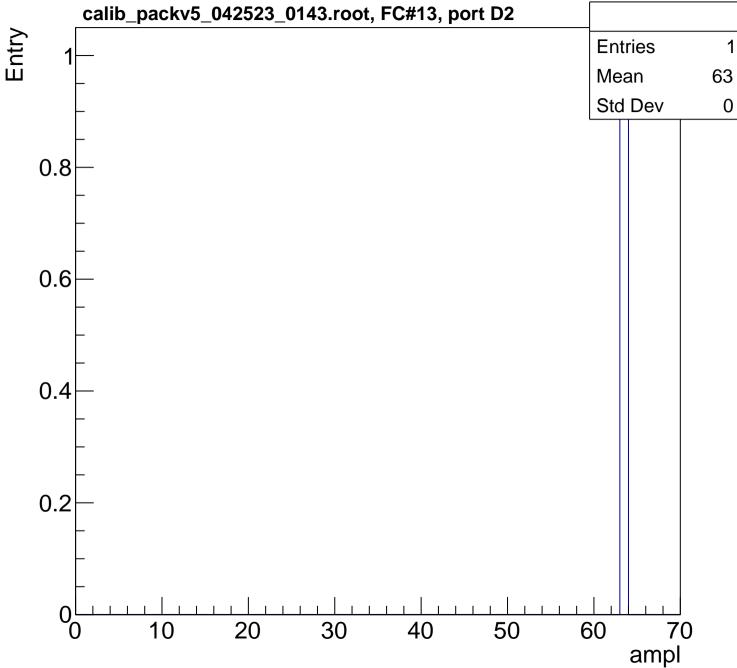




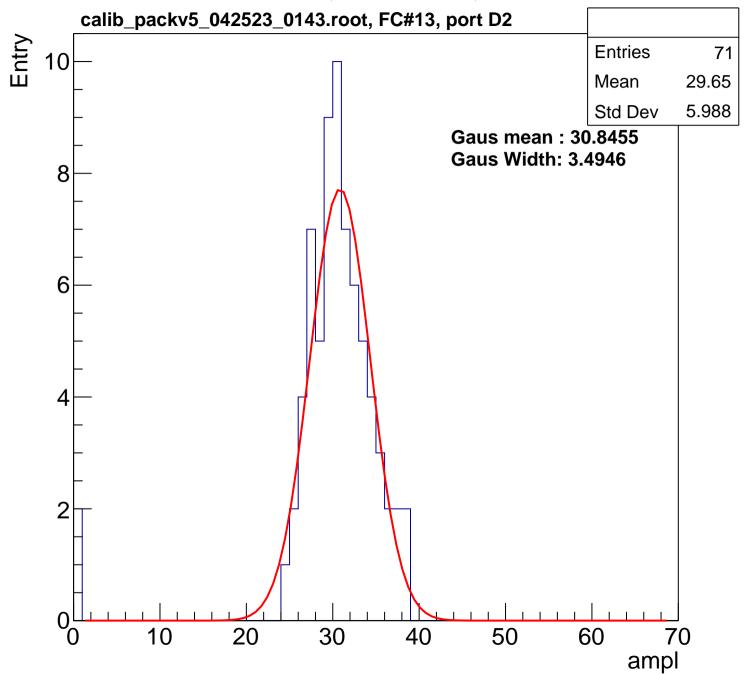


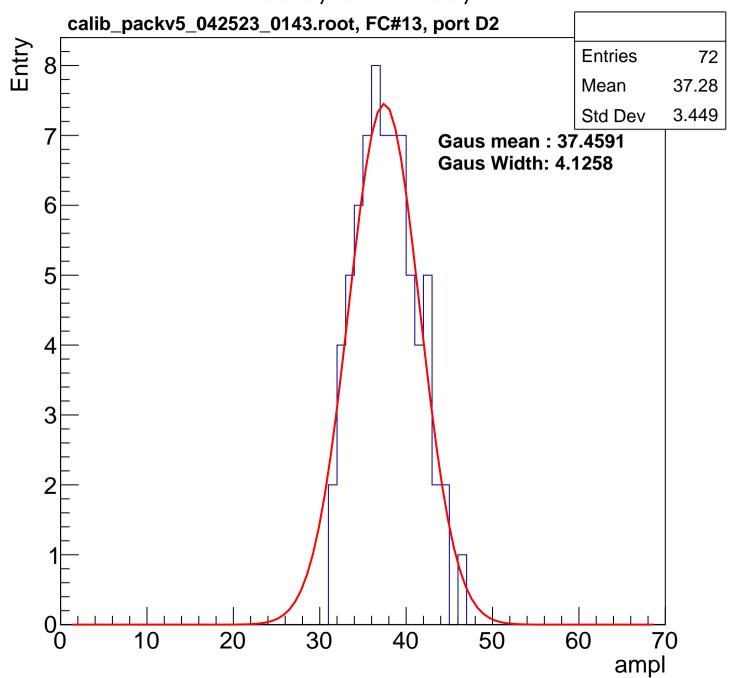


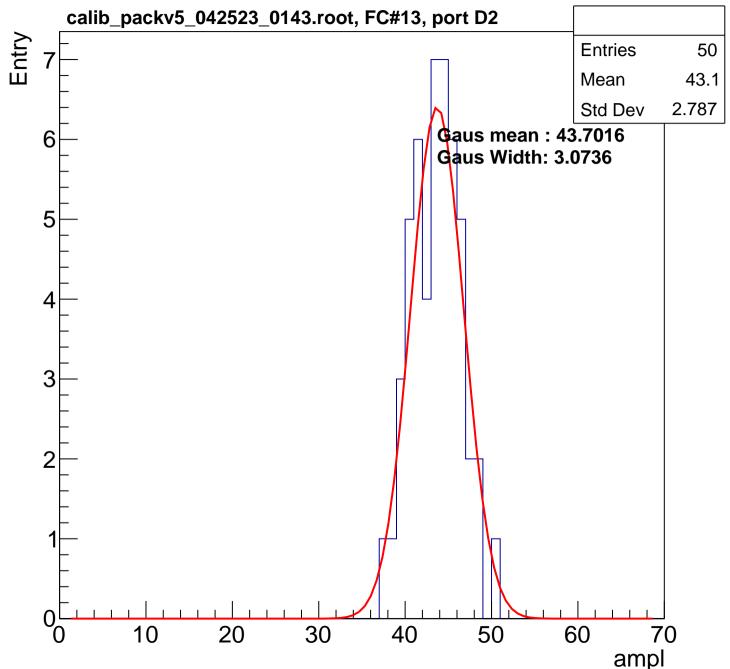


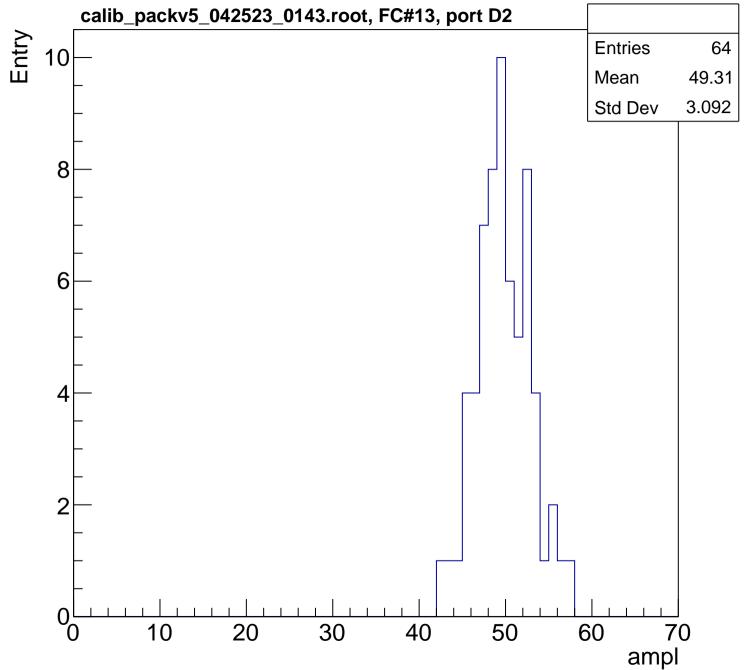


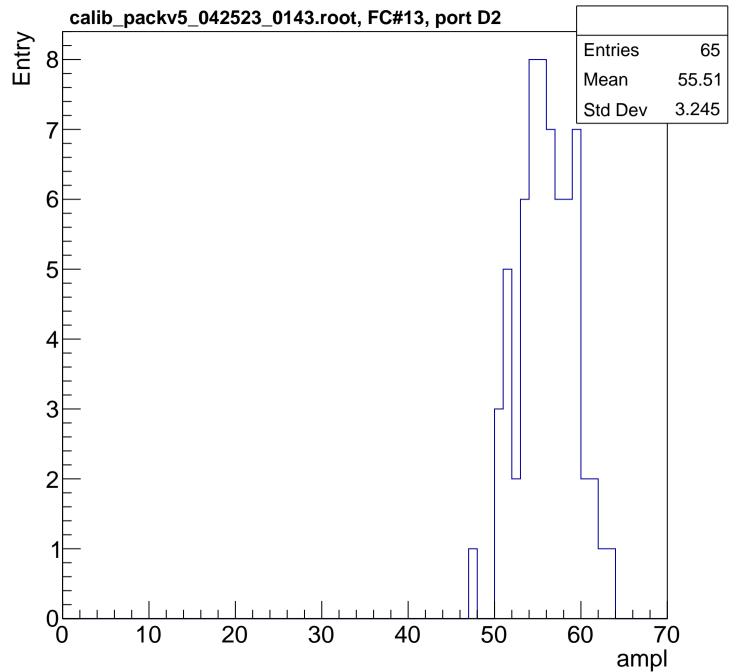


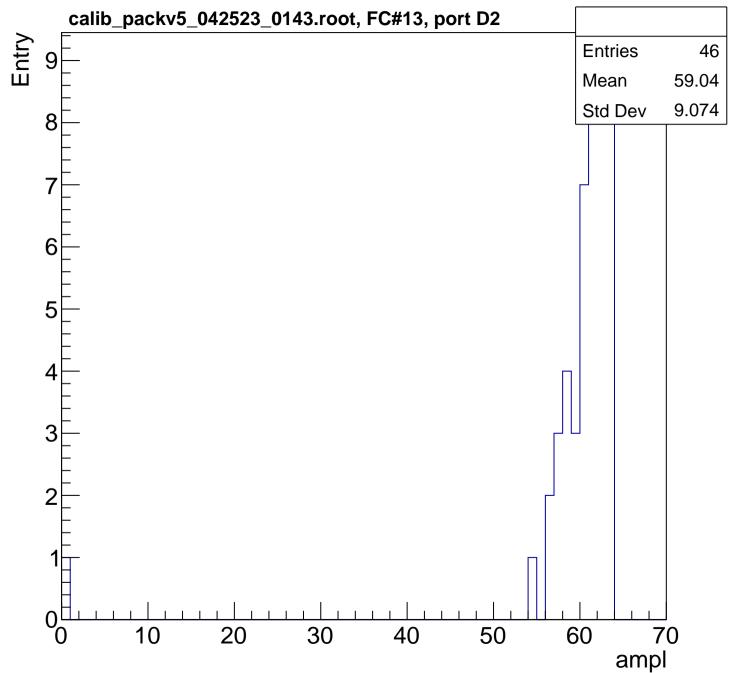


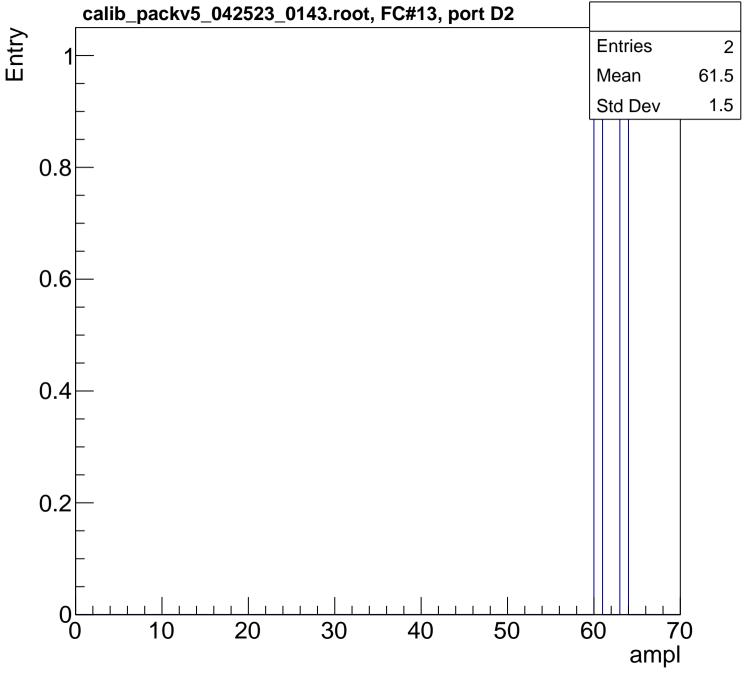




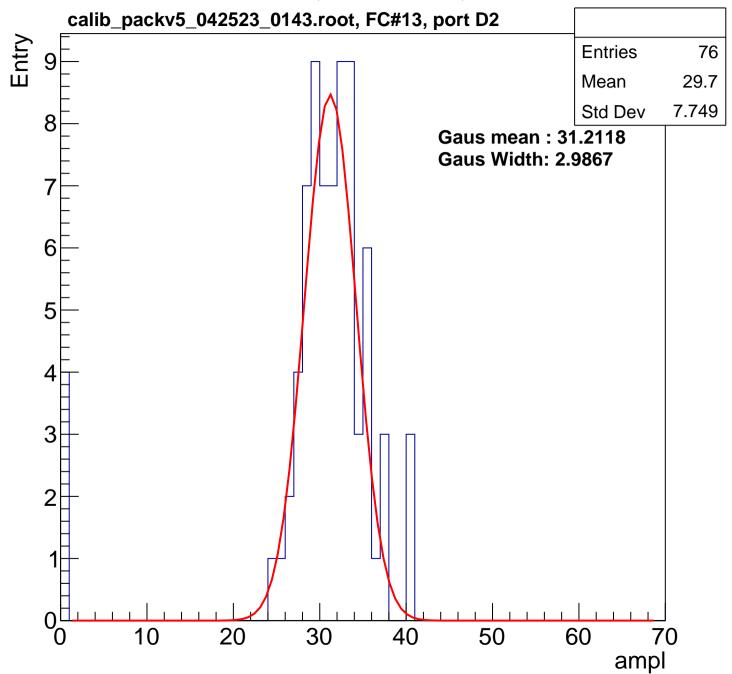


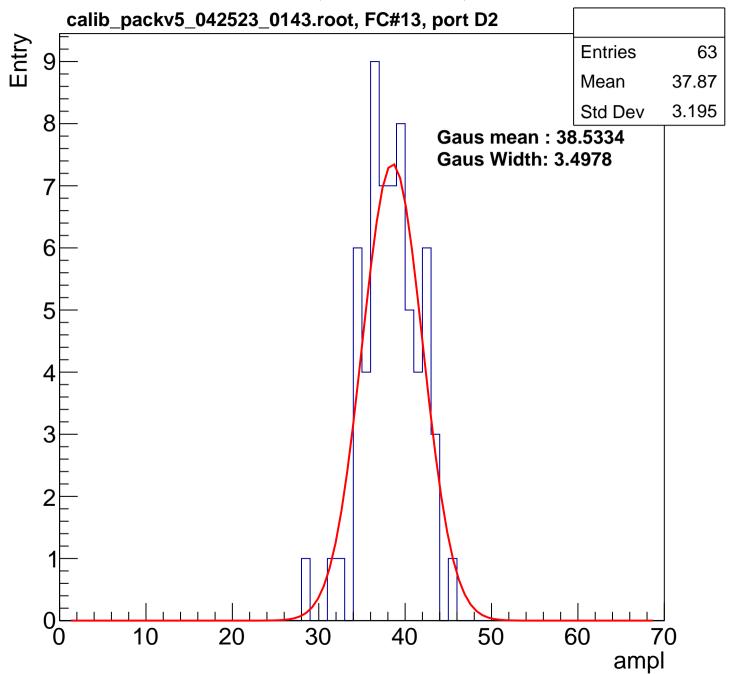


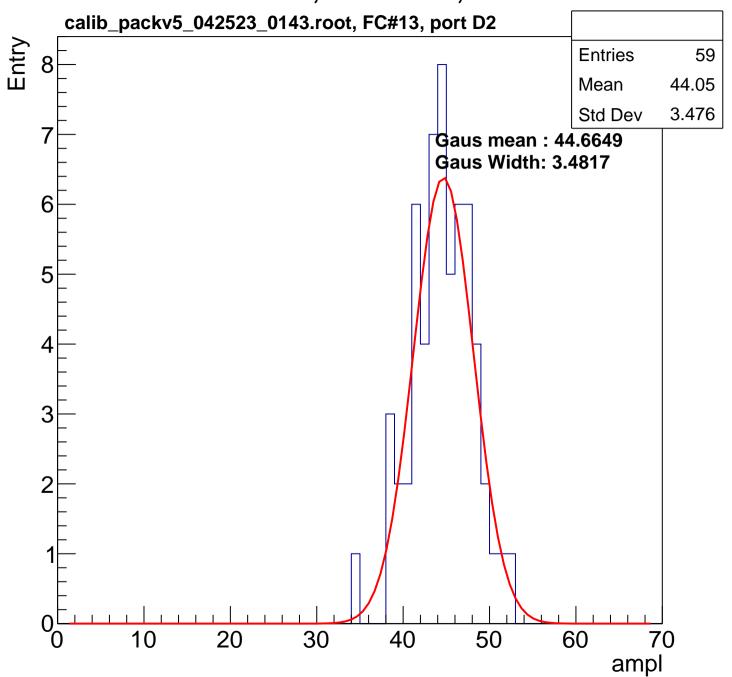


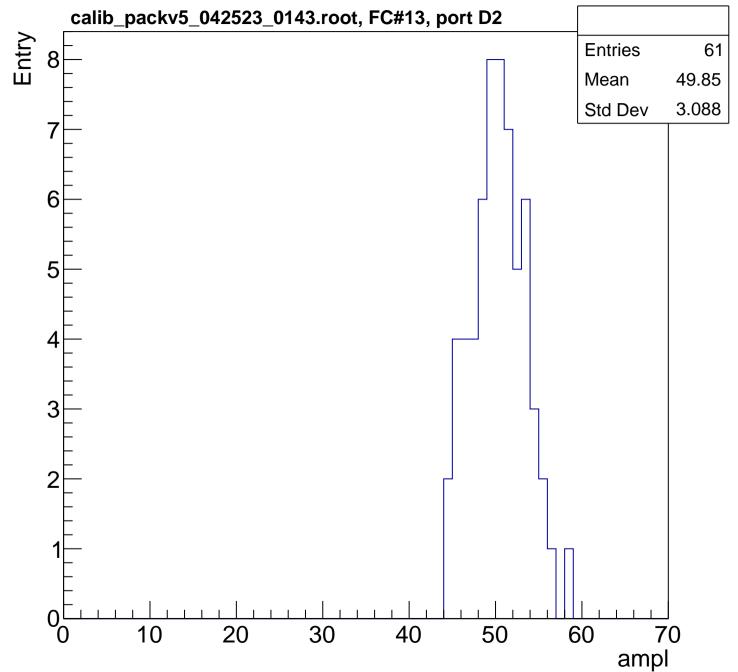


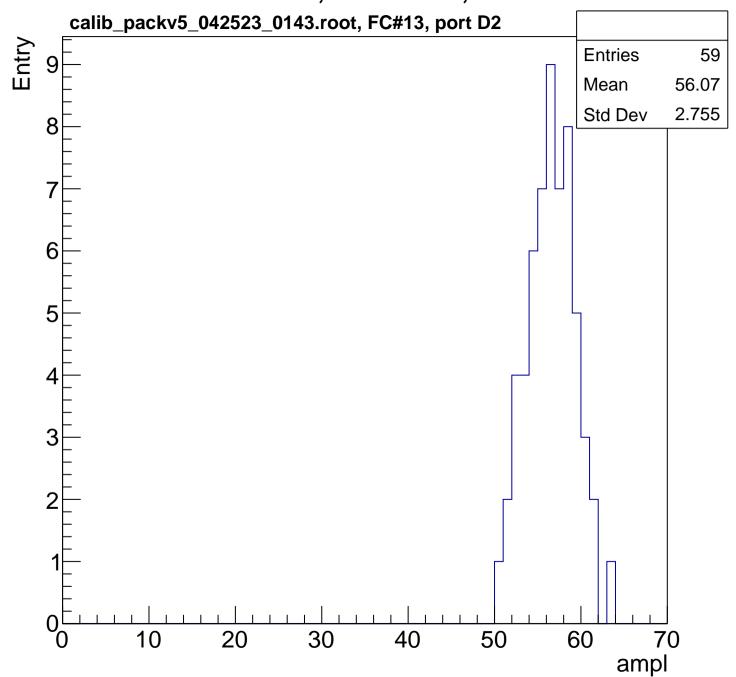
B1L003S, U9-ch98, adc7 calib\_packv5\_042523\_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

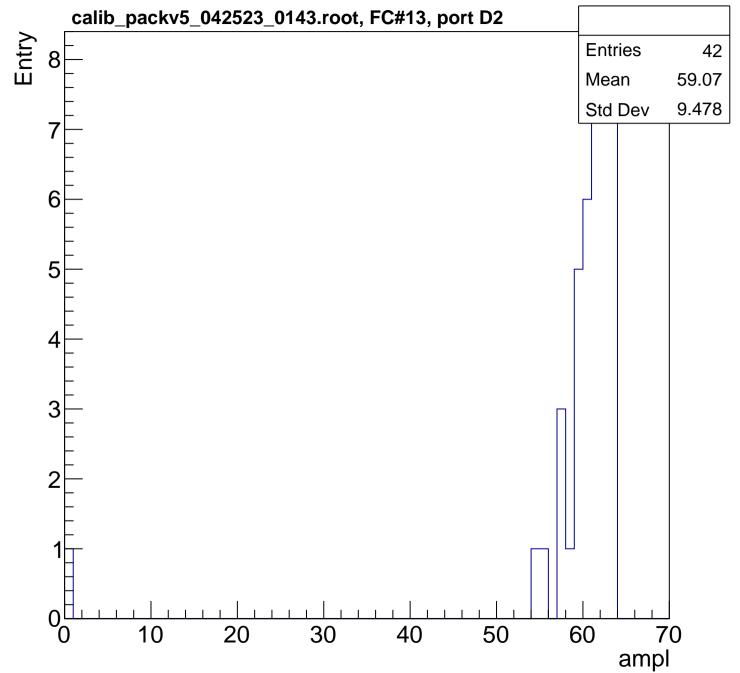


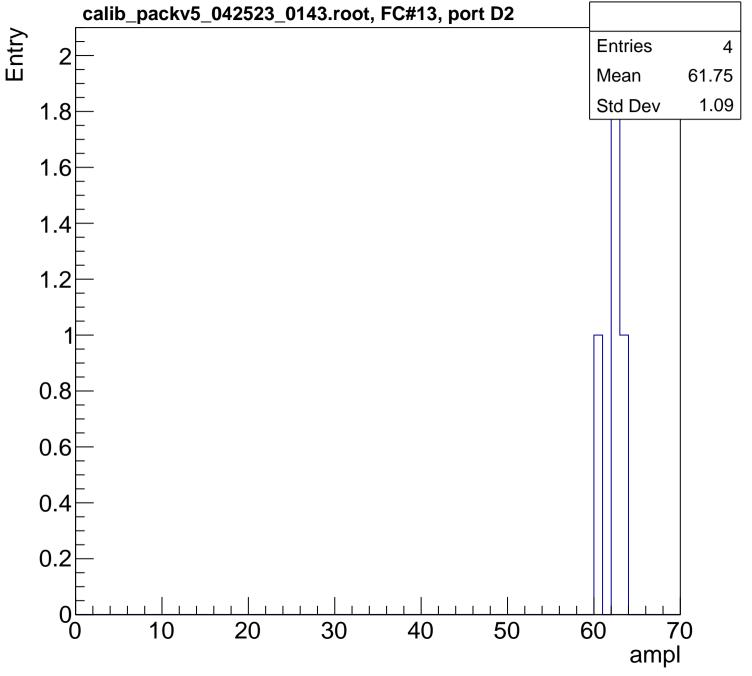


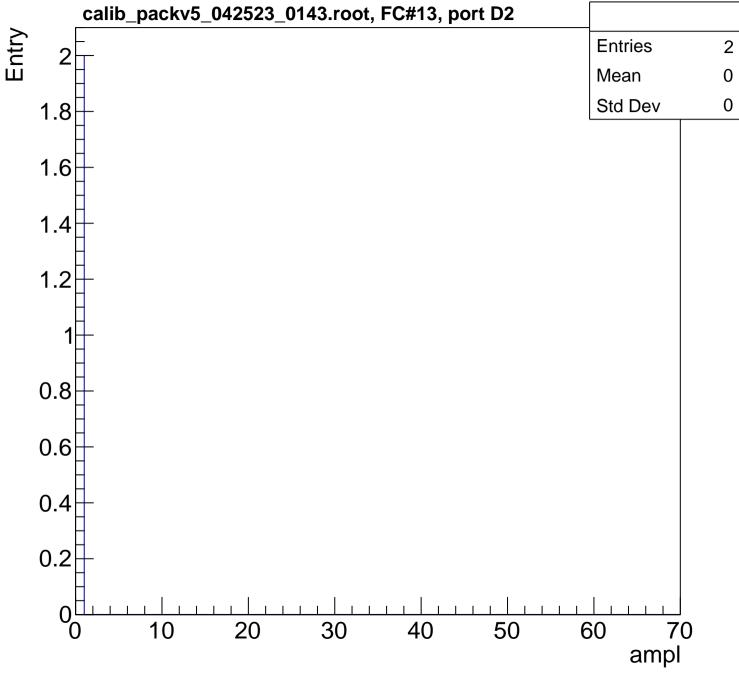


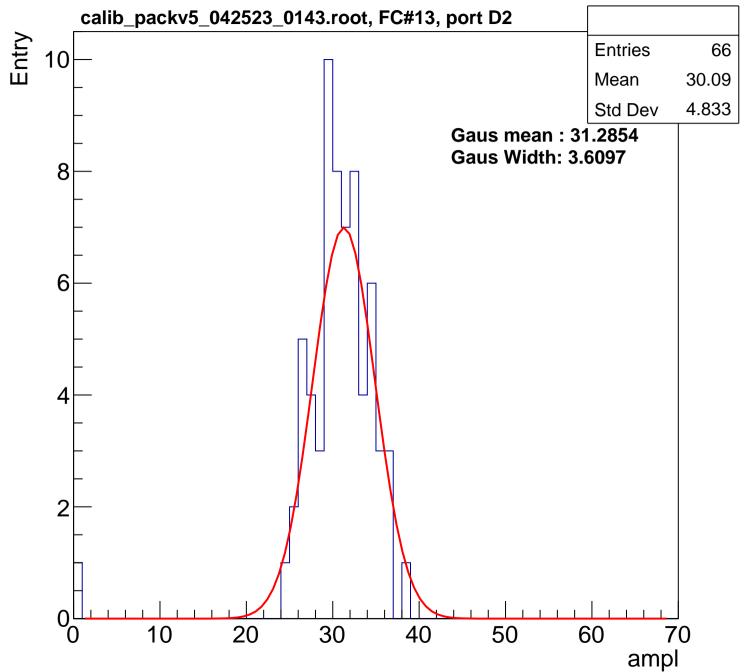


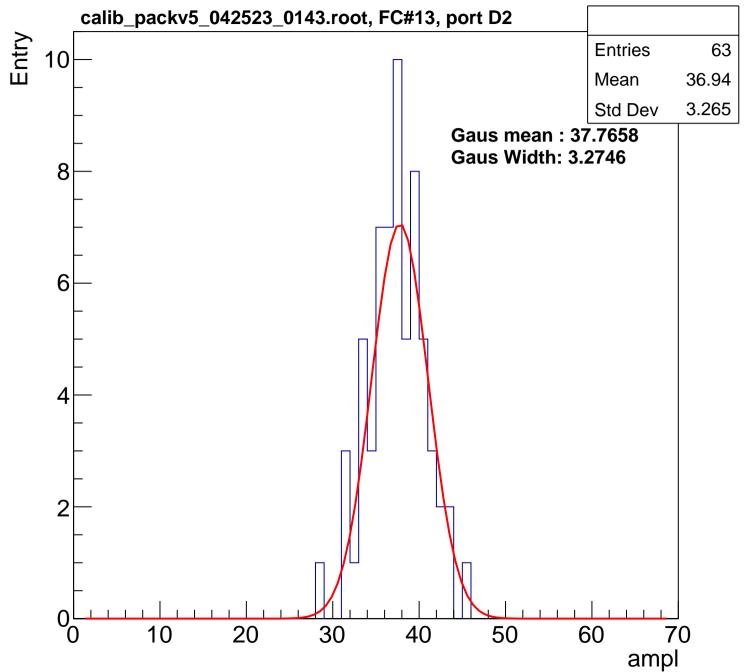


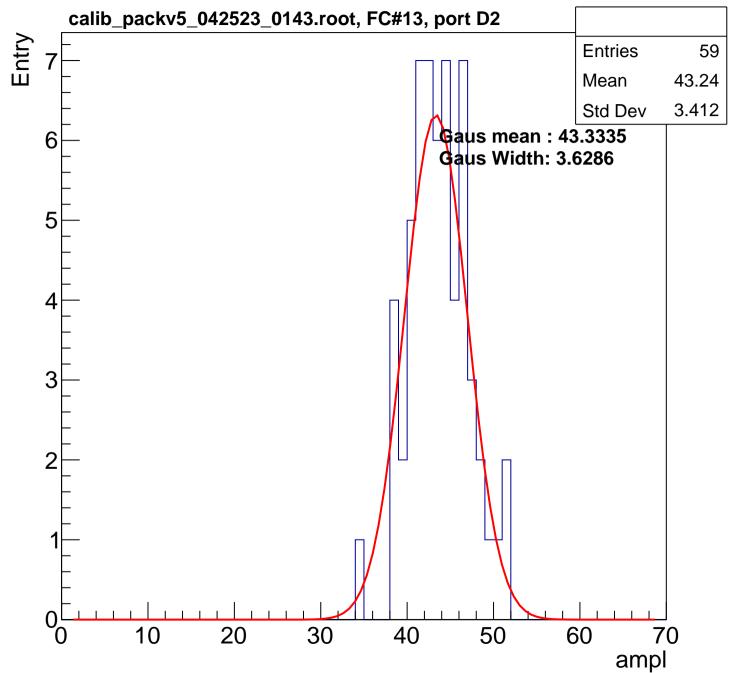


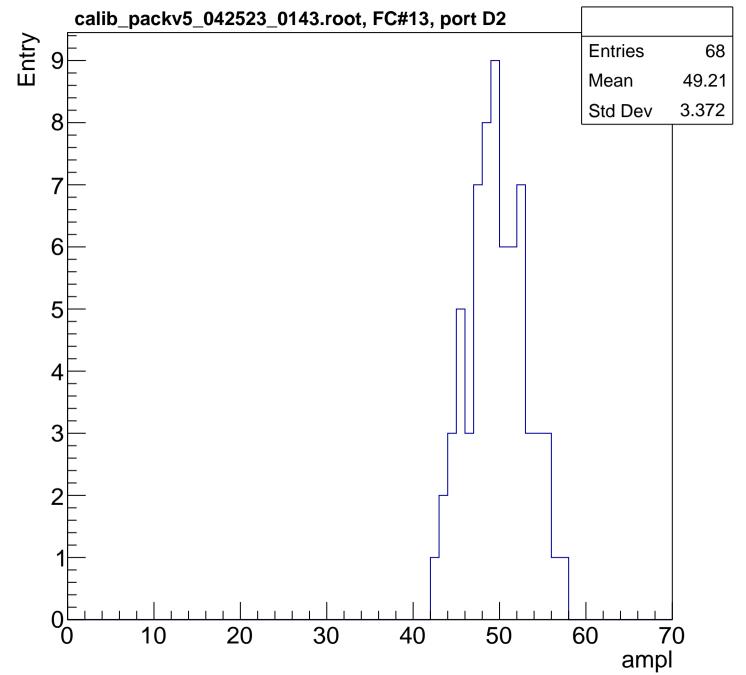


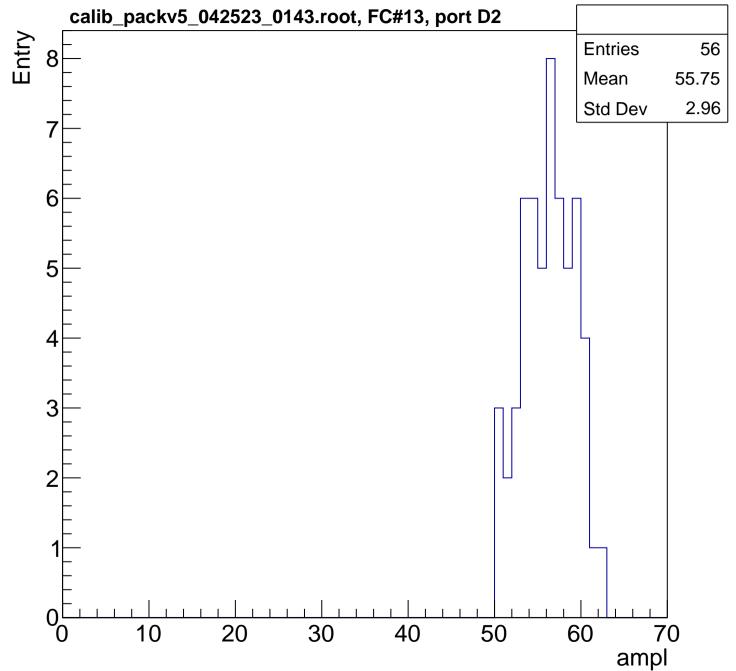


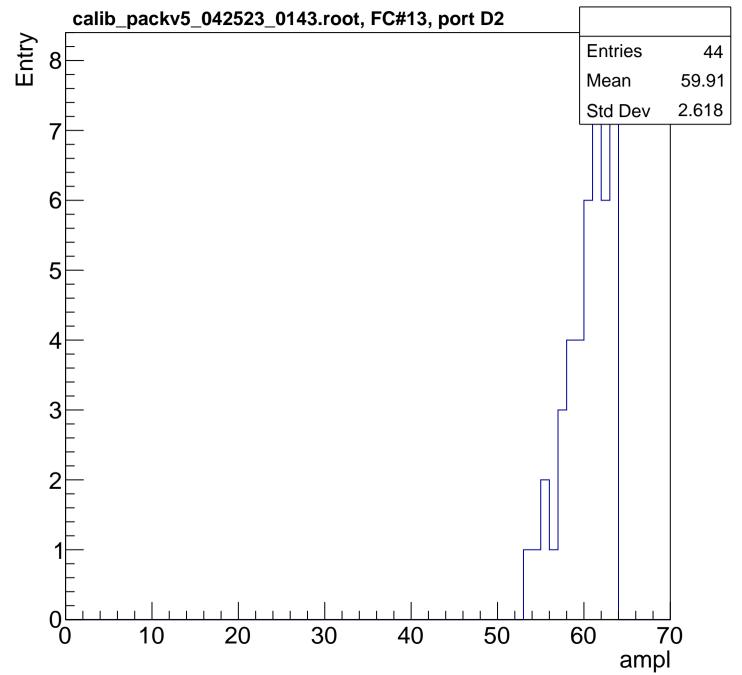


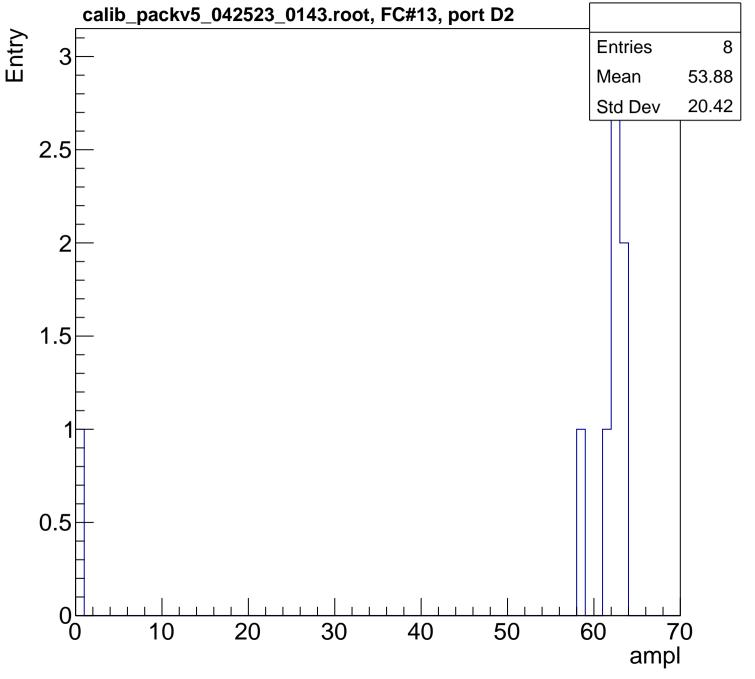


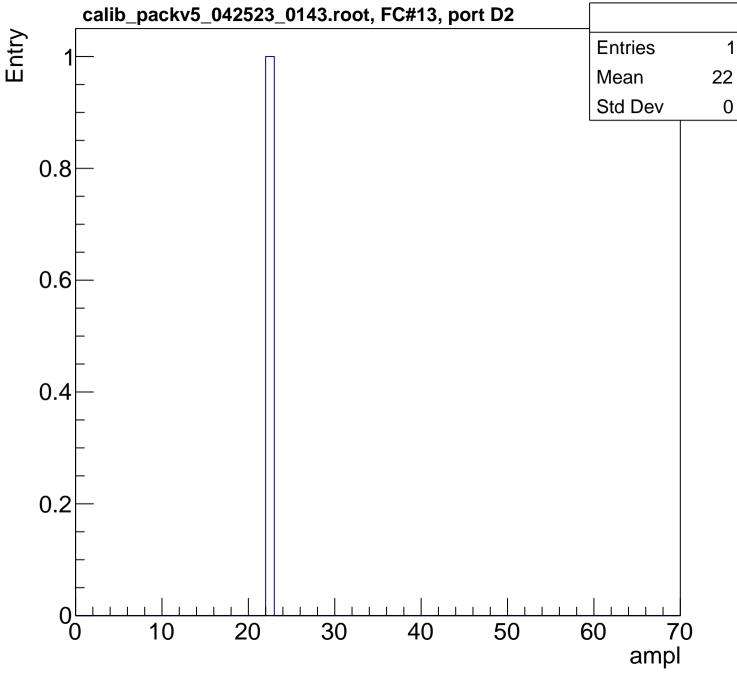


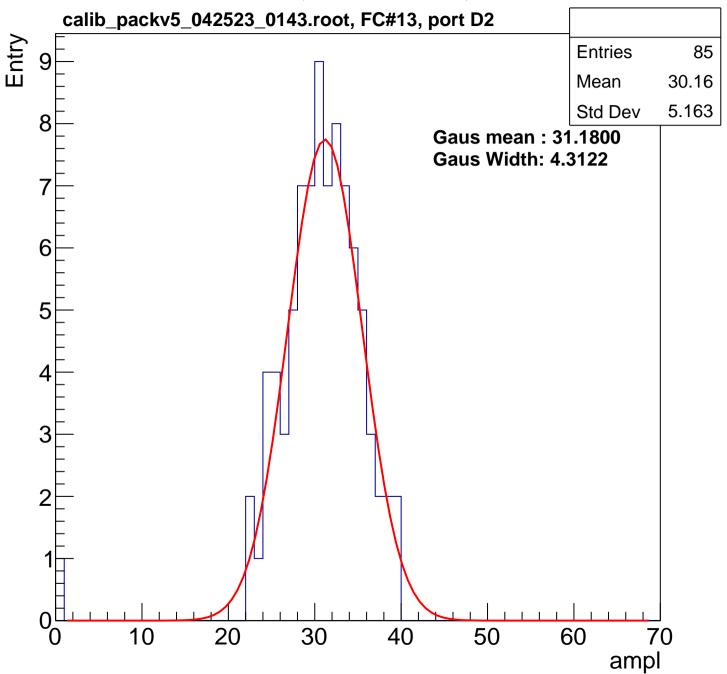


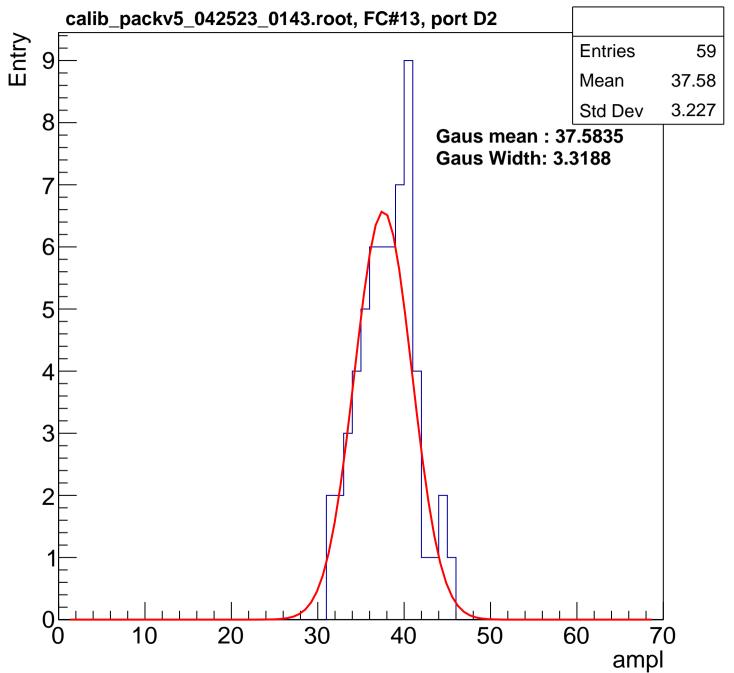


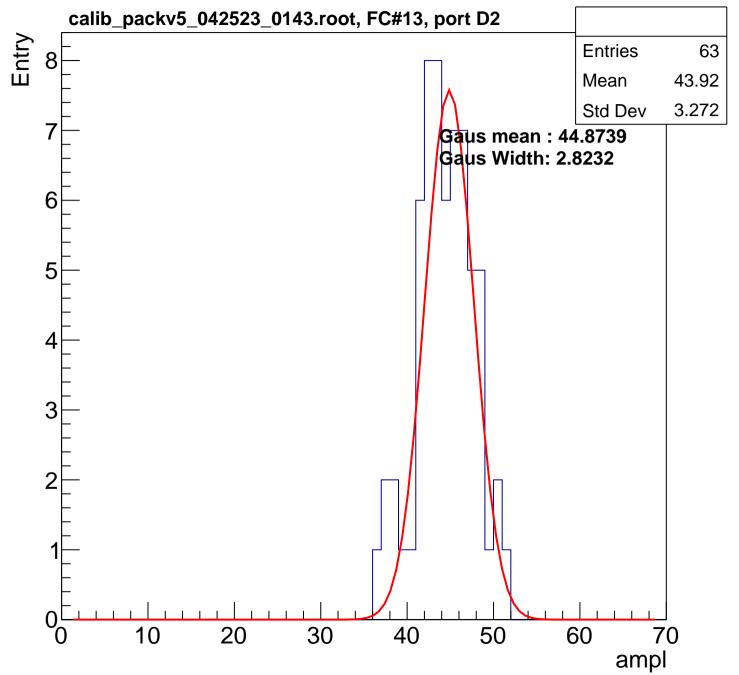


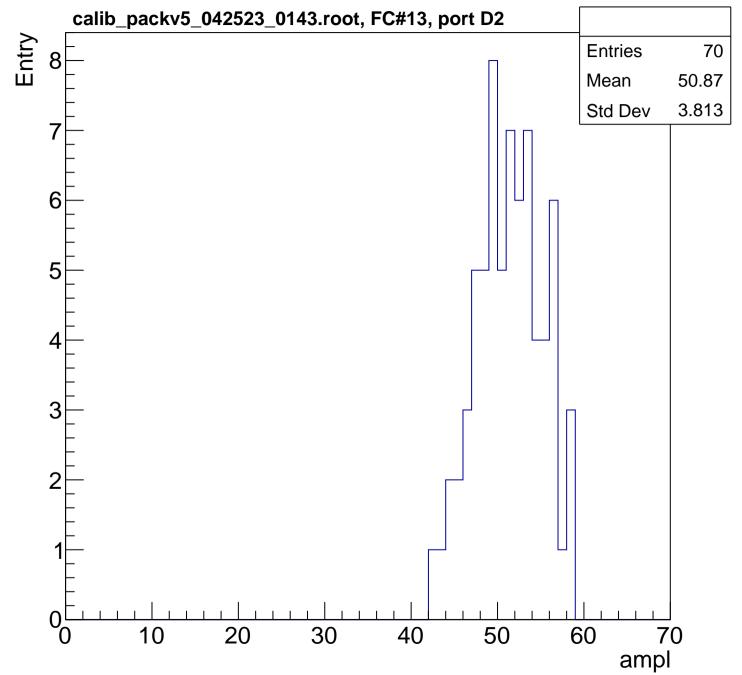


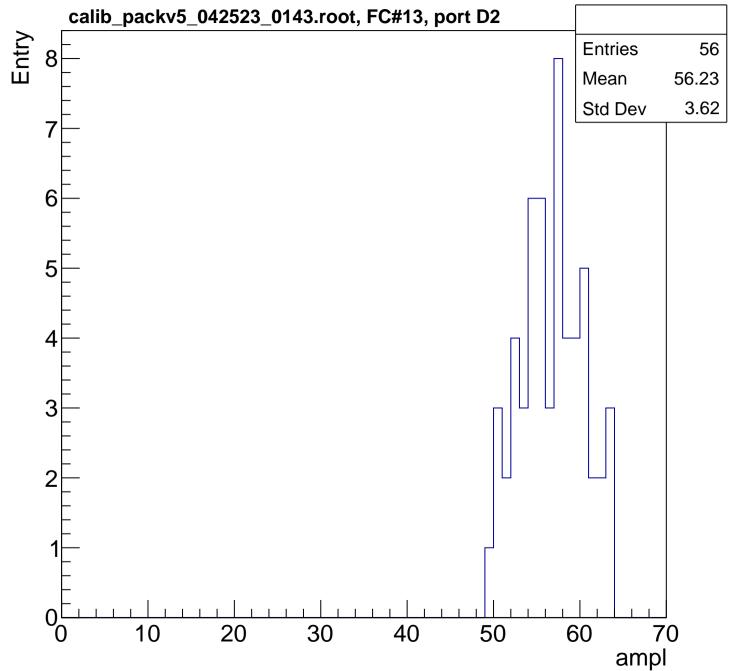


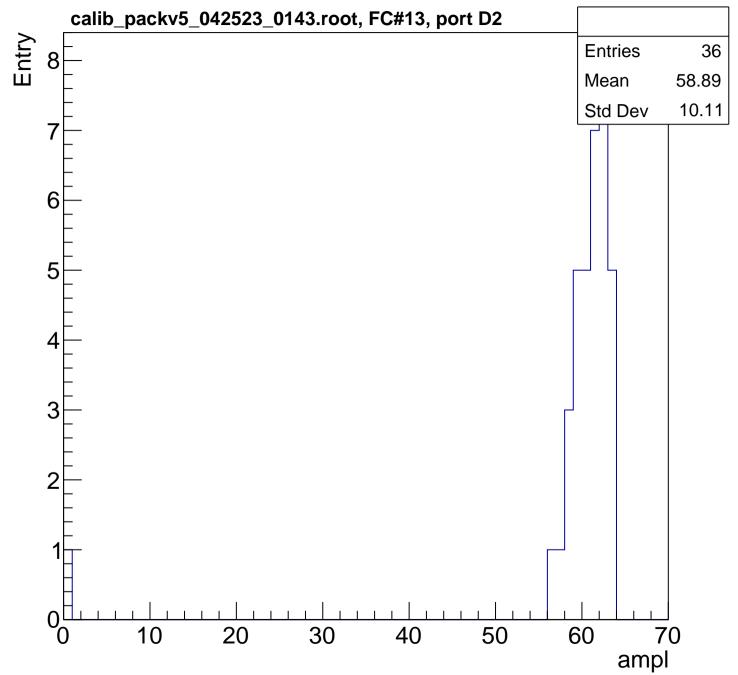


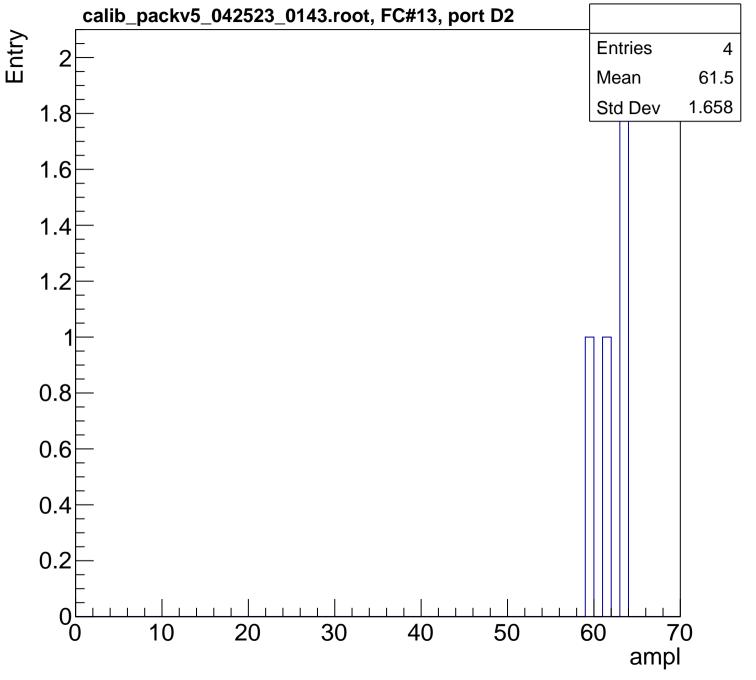


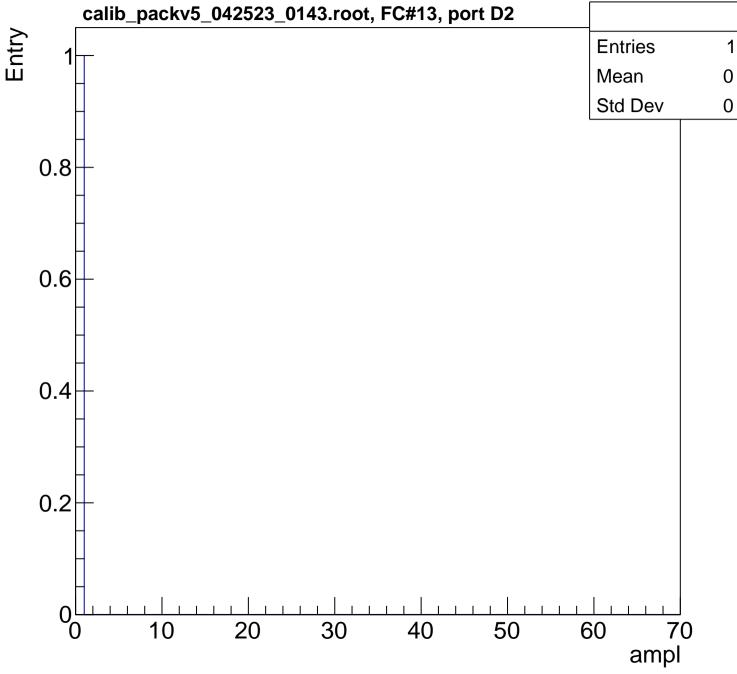


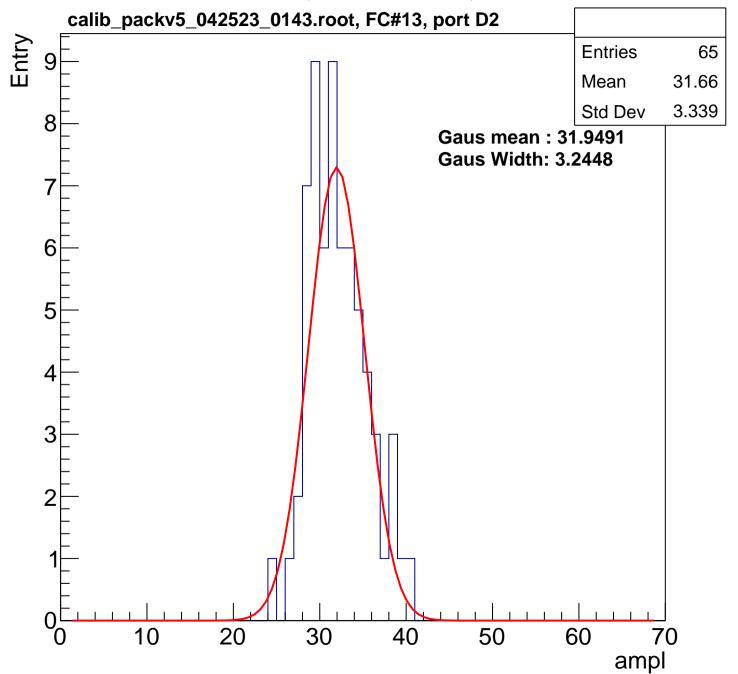


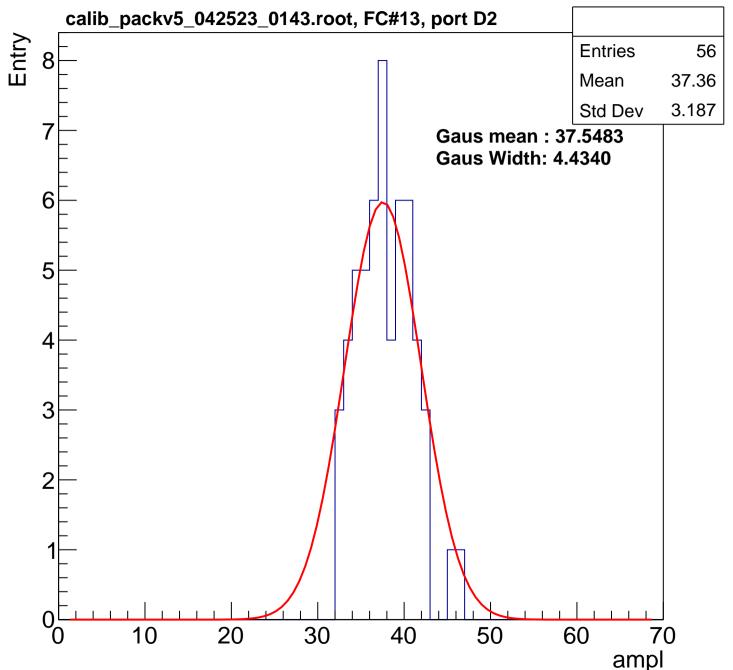


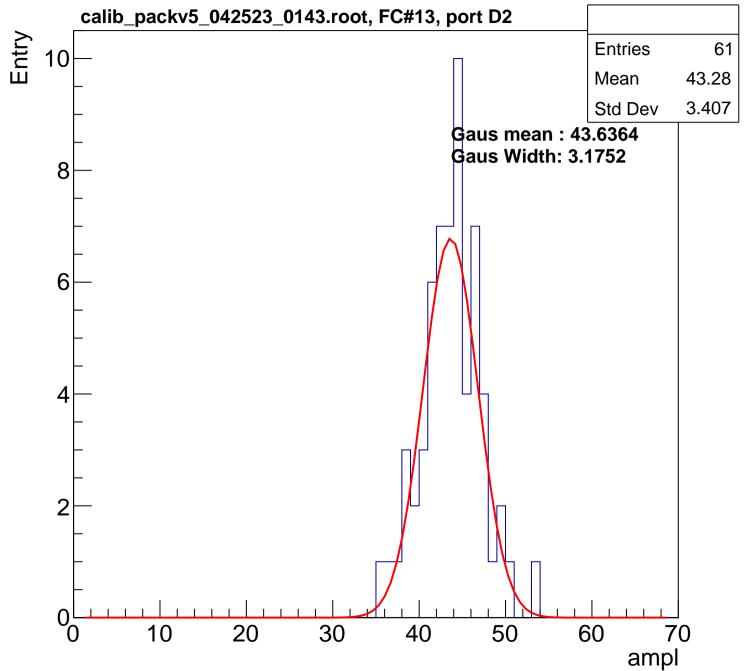


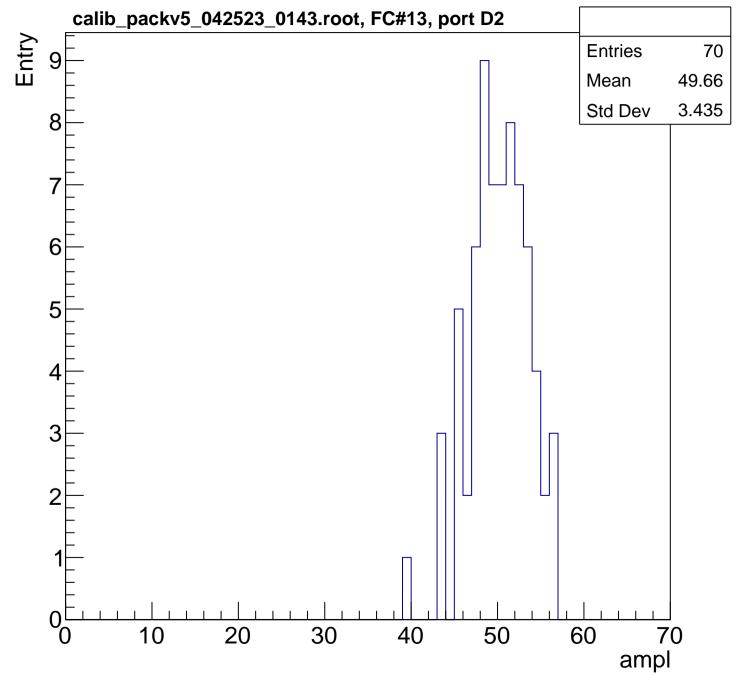


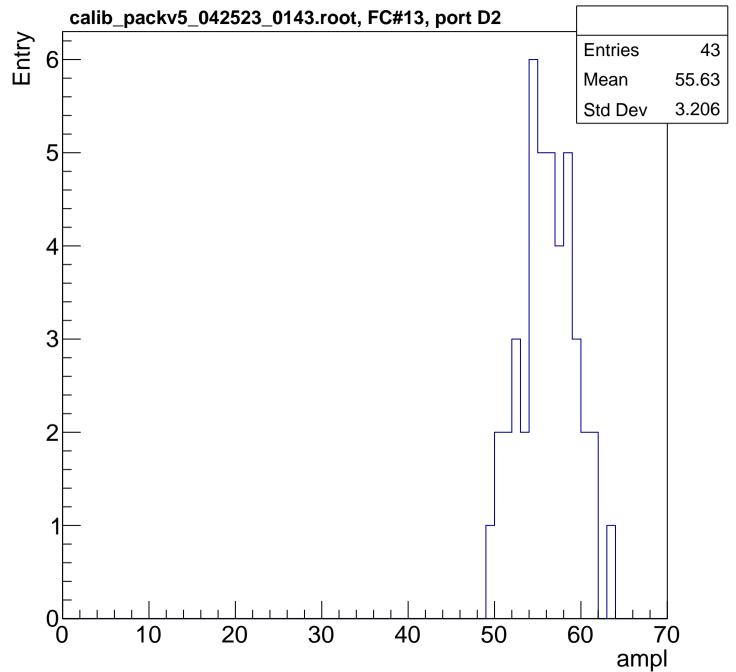


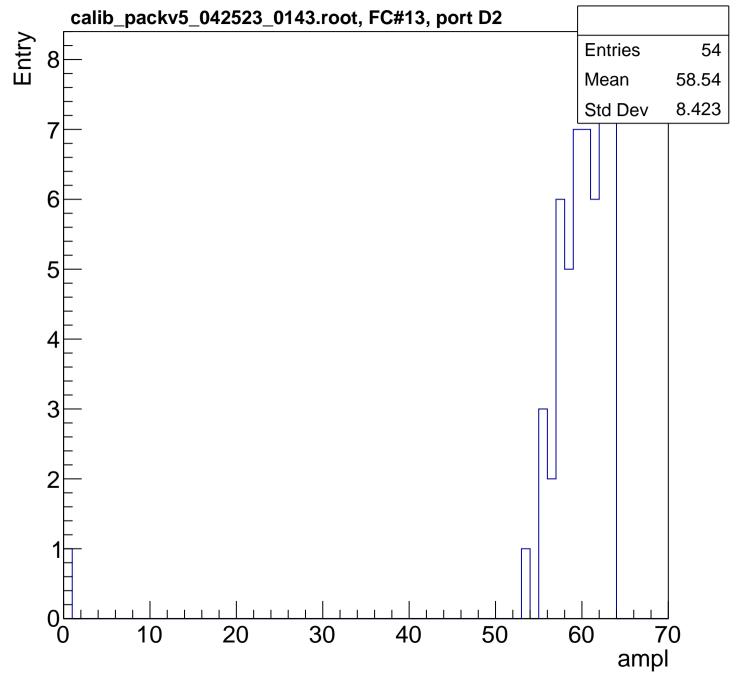


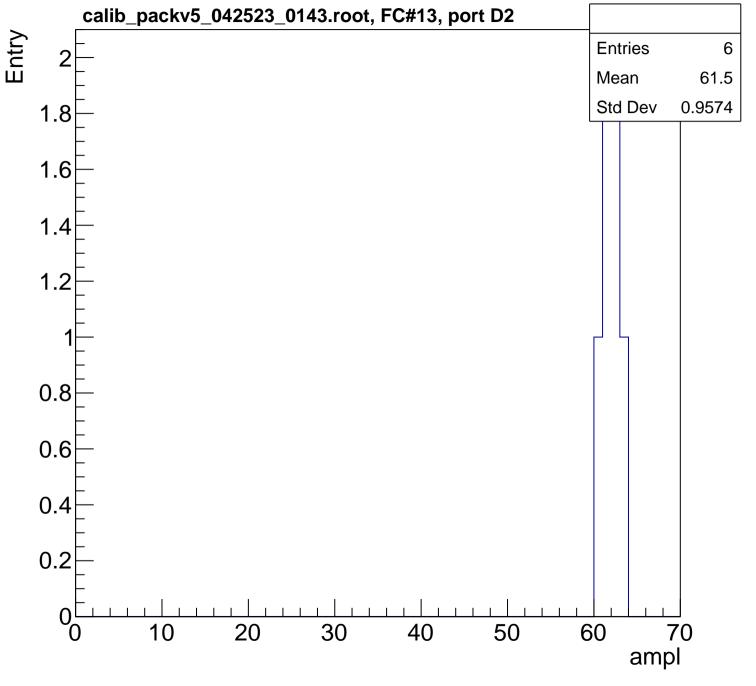


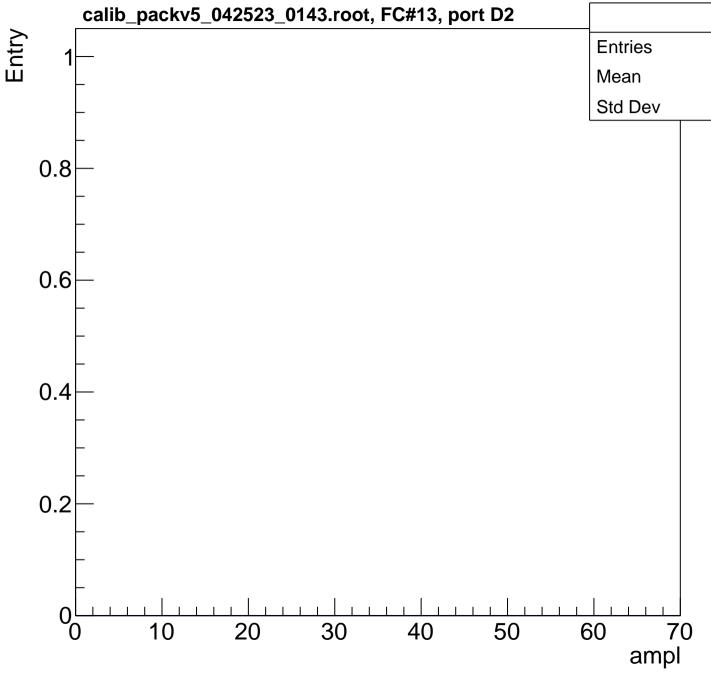


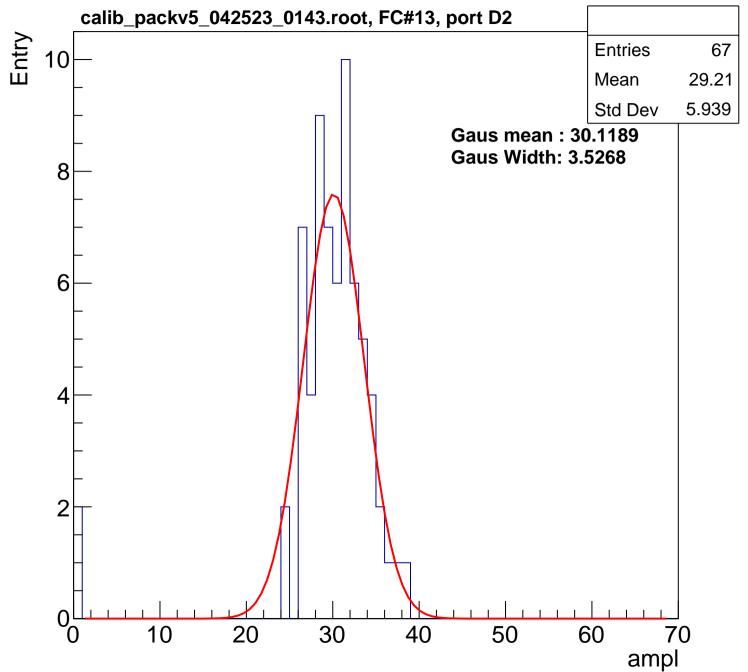


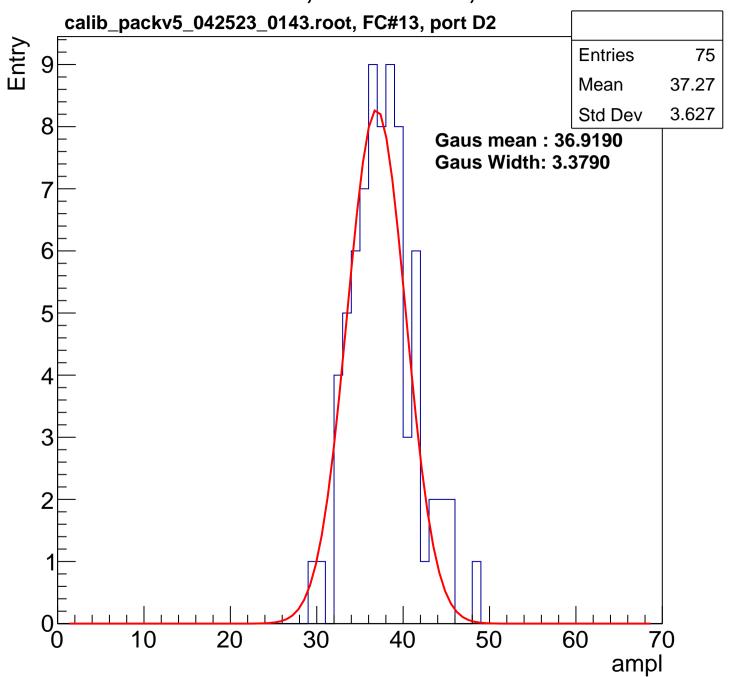


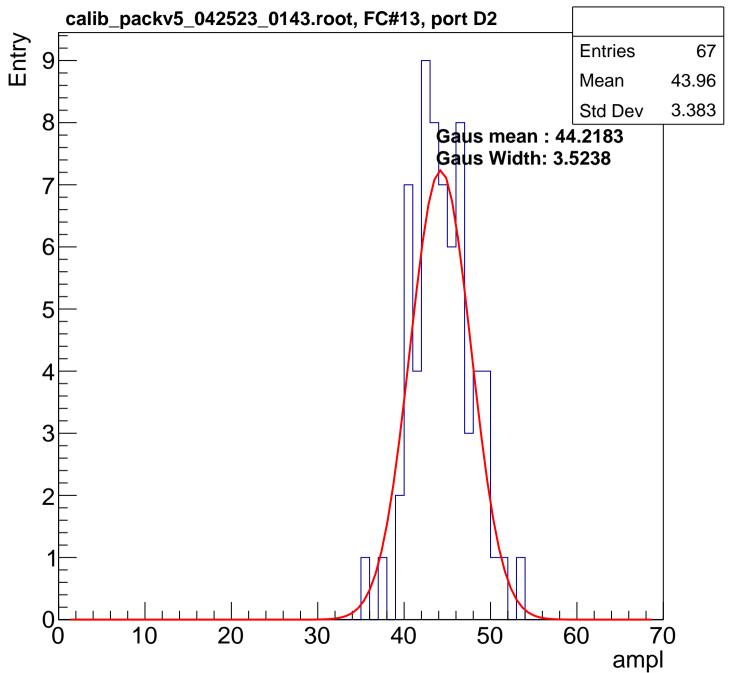


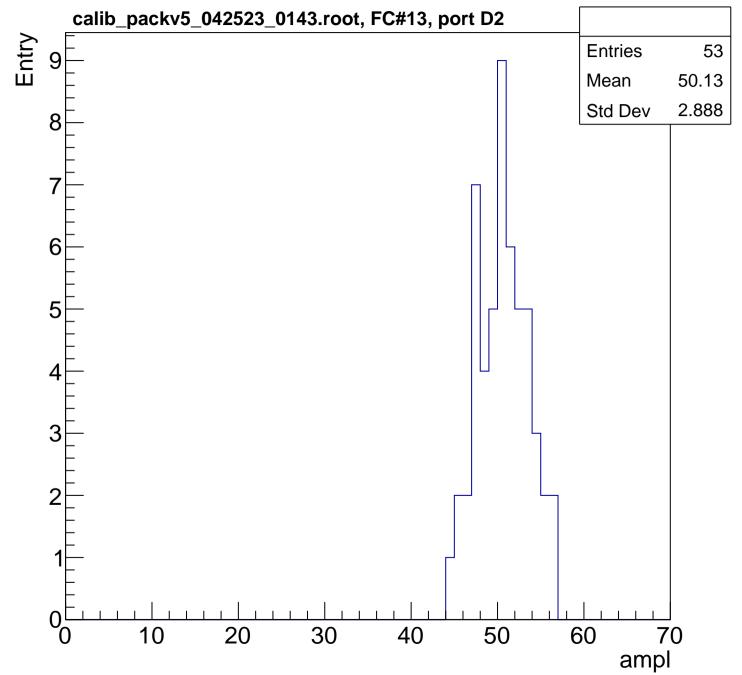


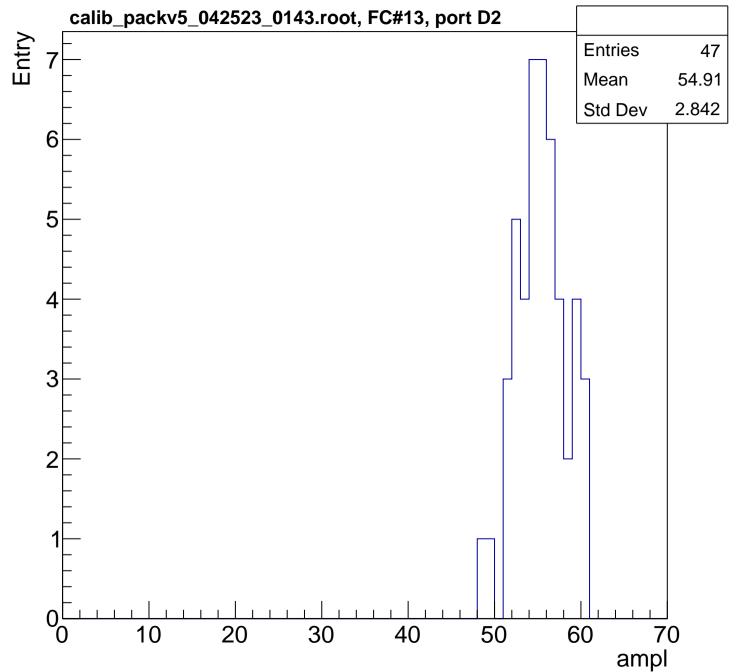


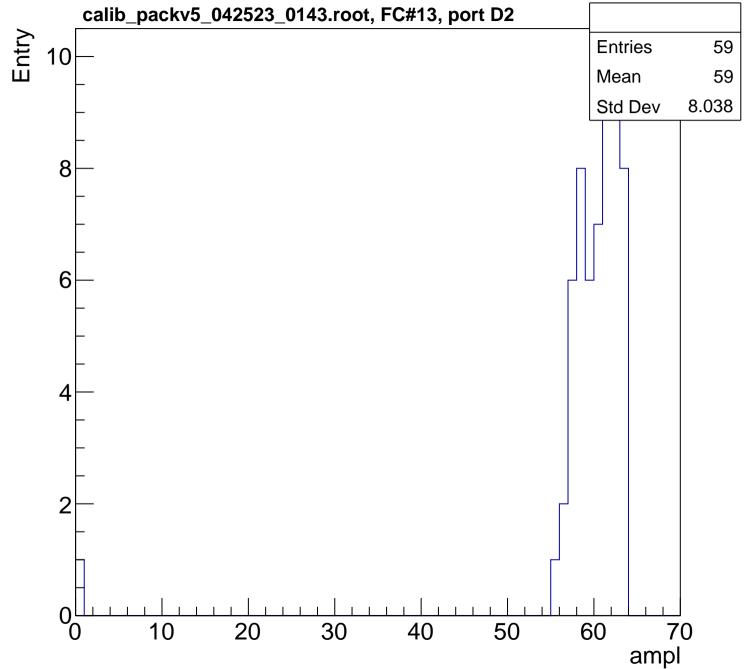


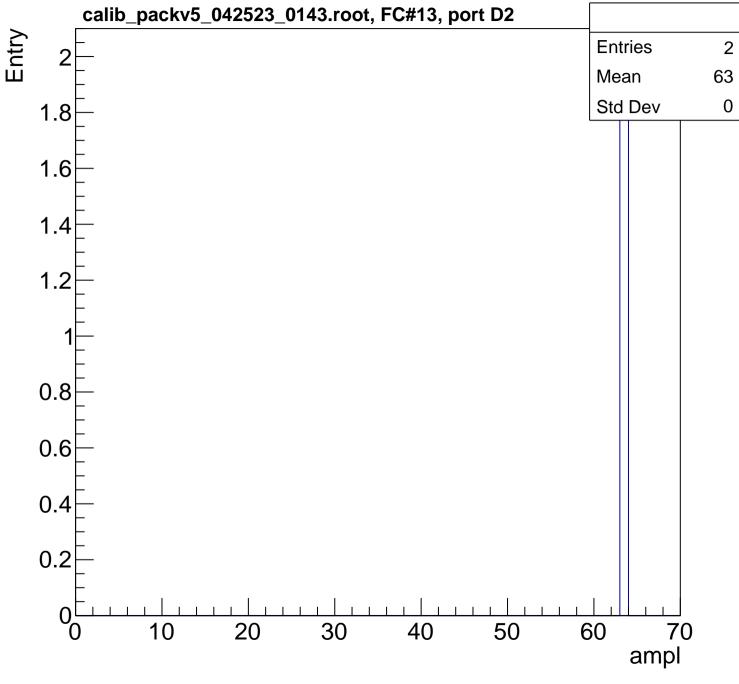




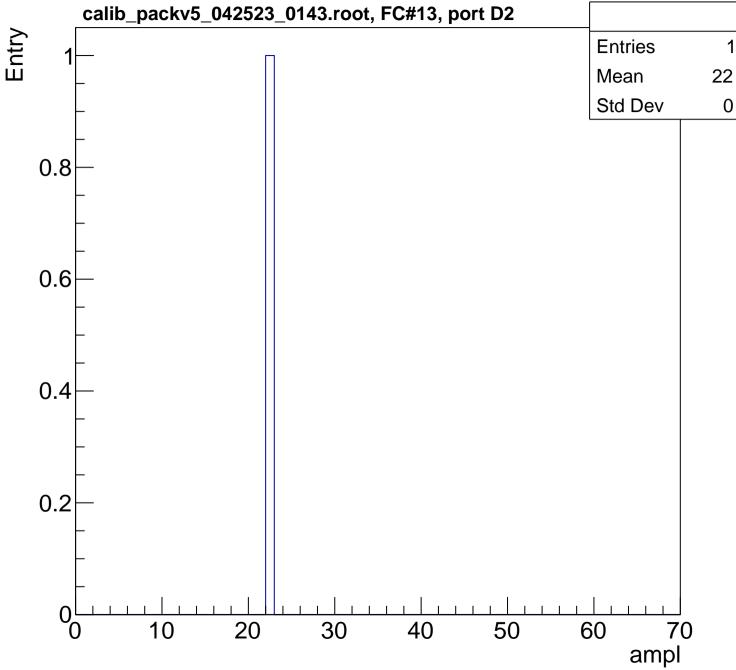


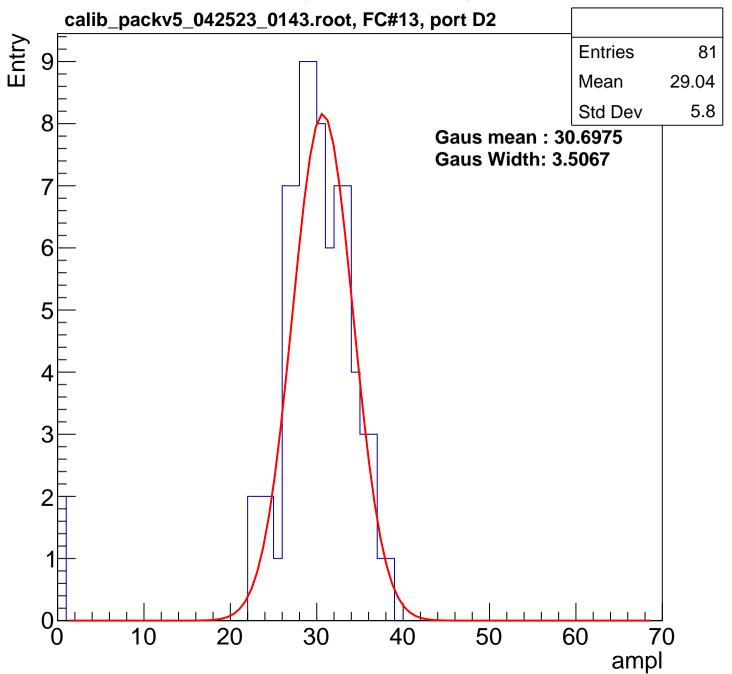


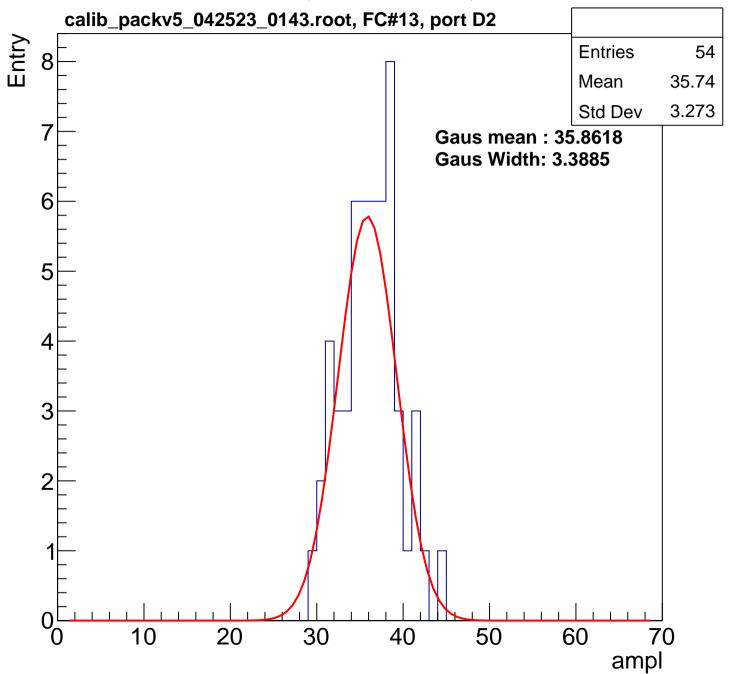


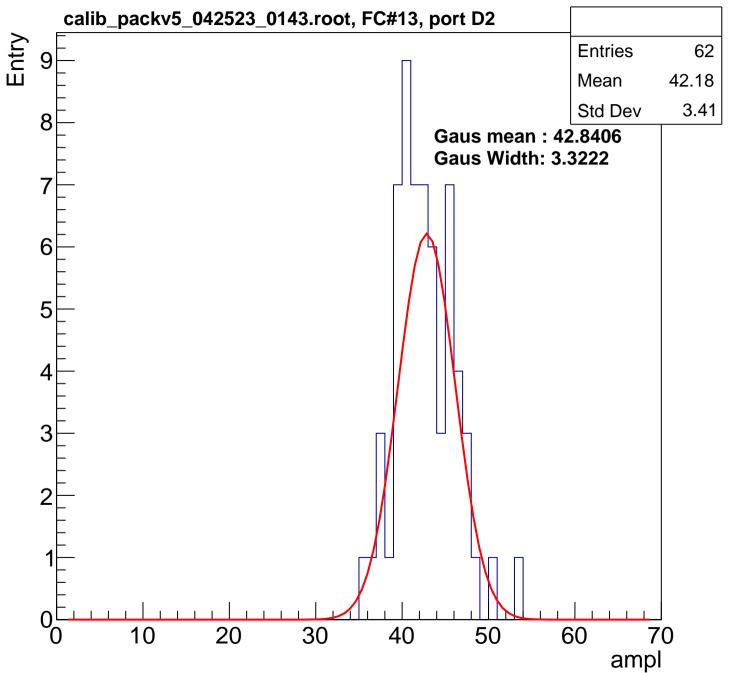


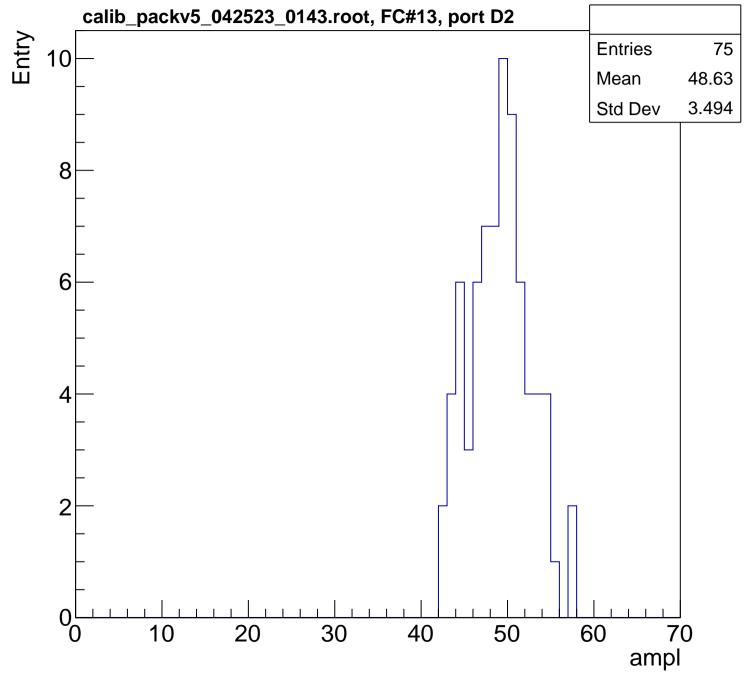
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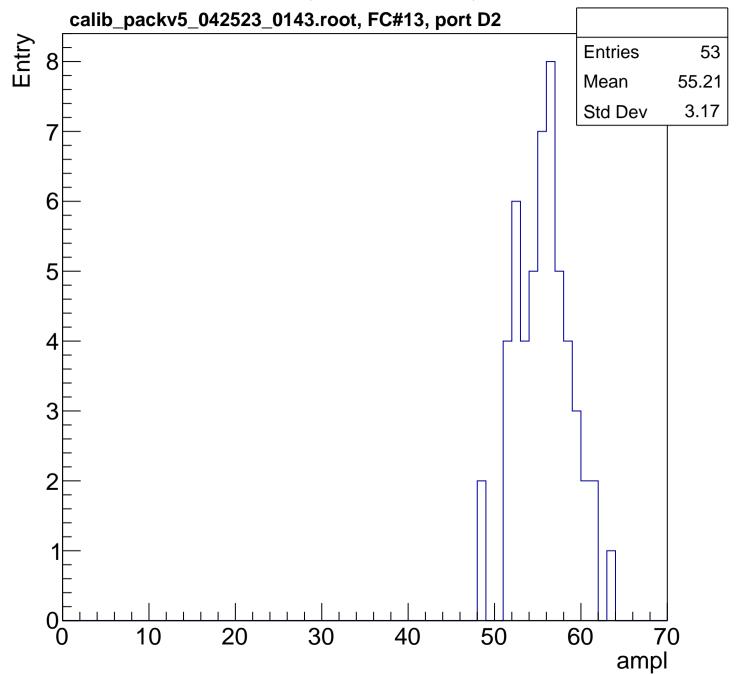


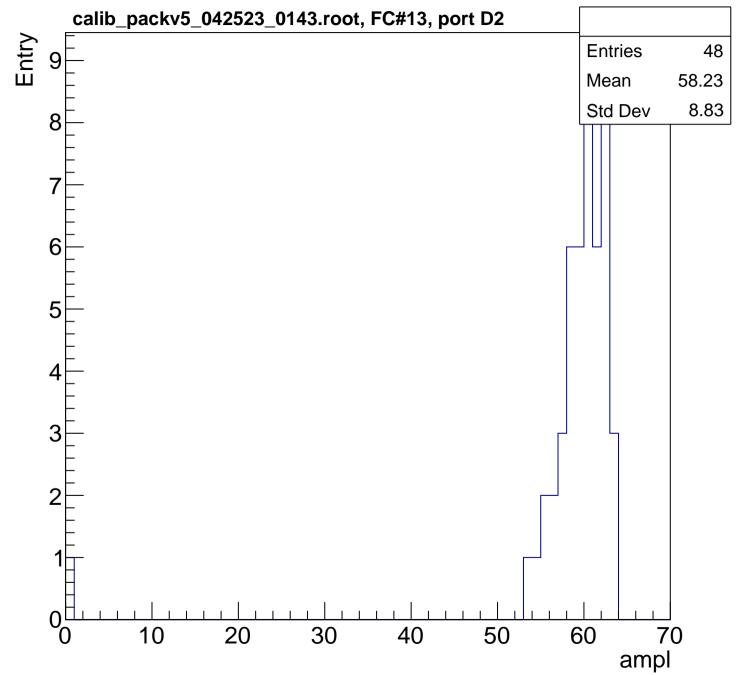


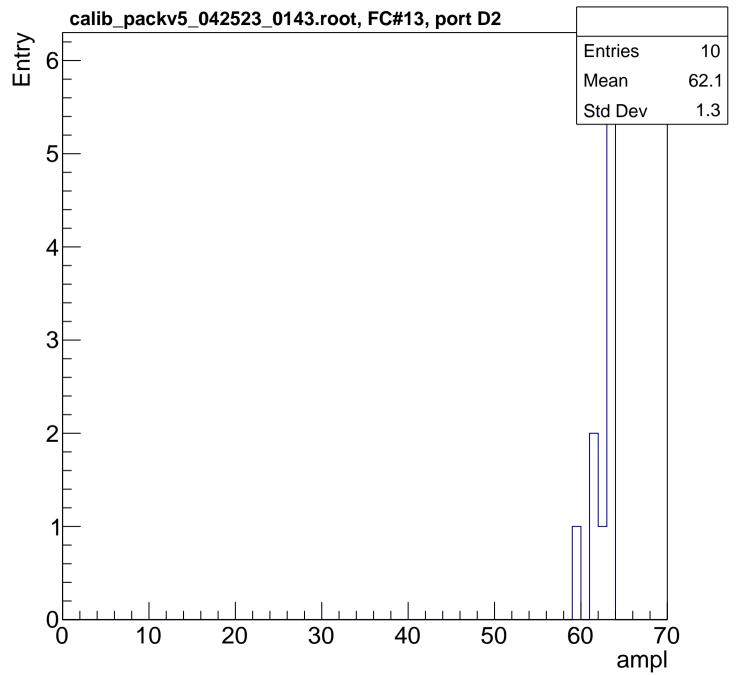


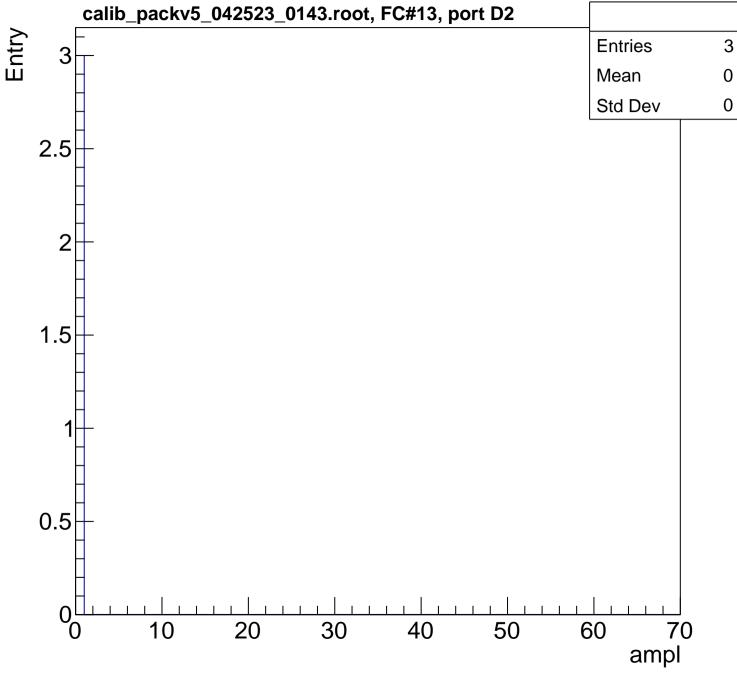


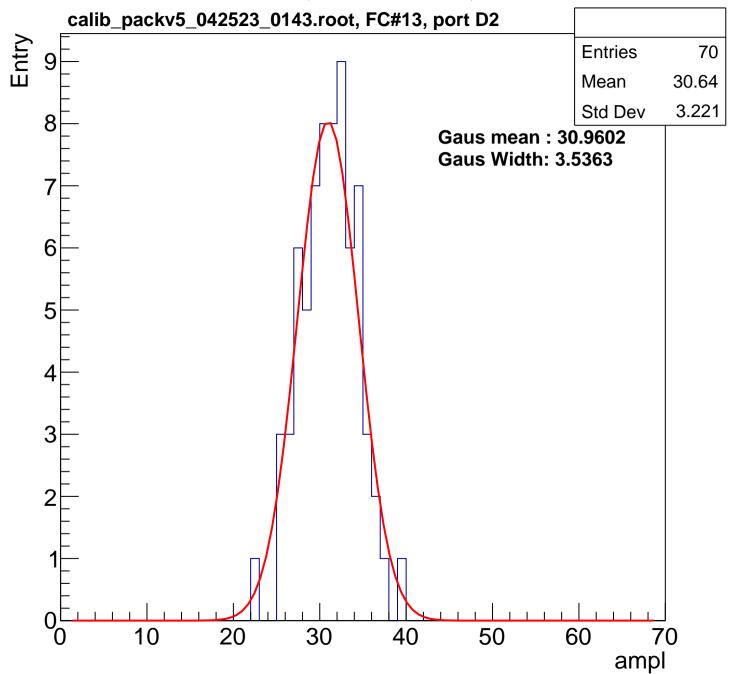


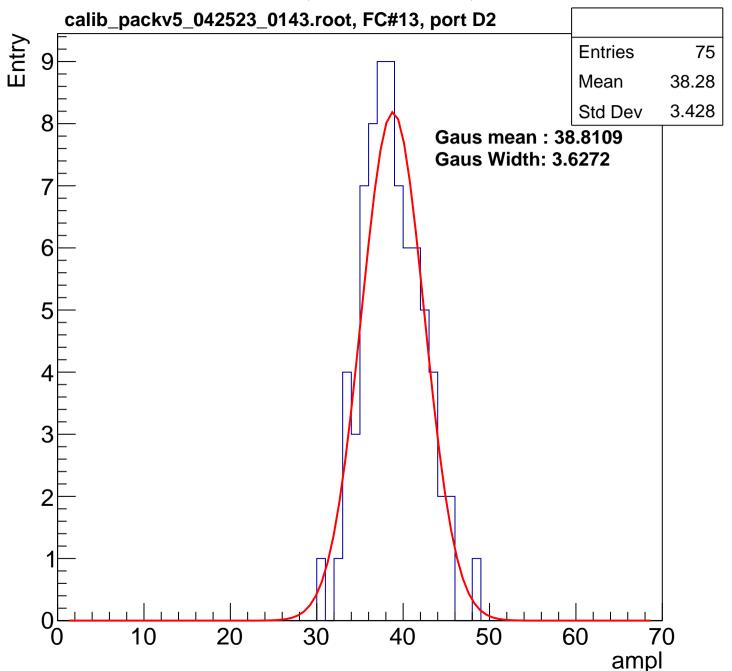


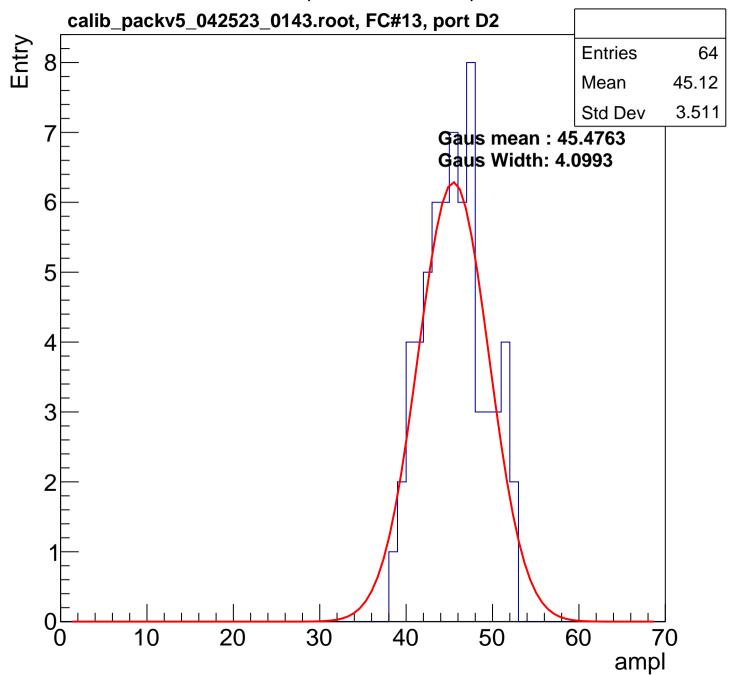


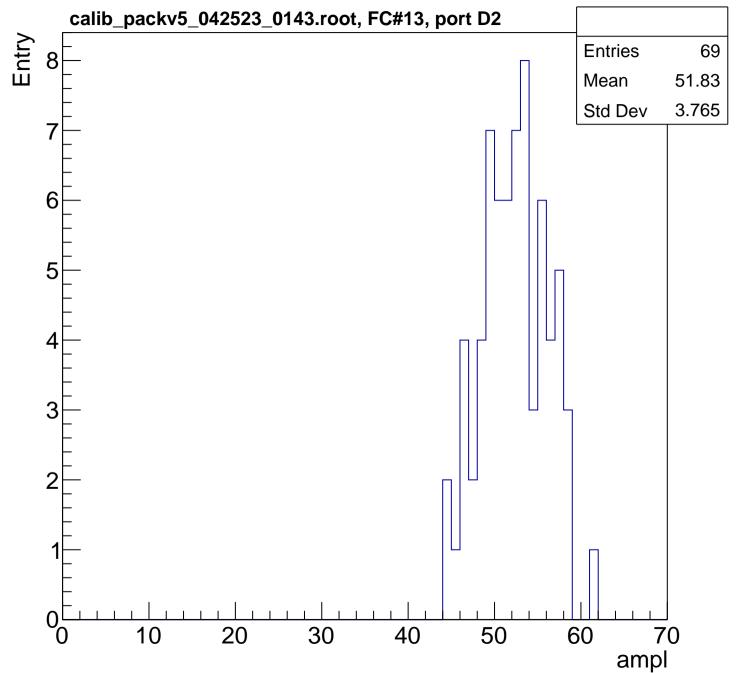


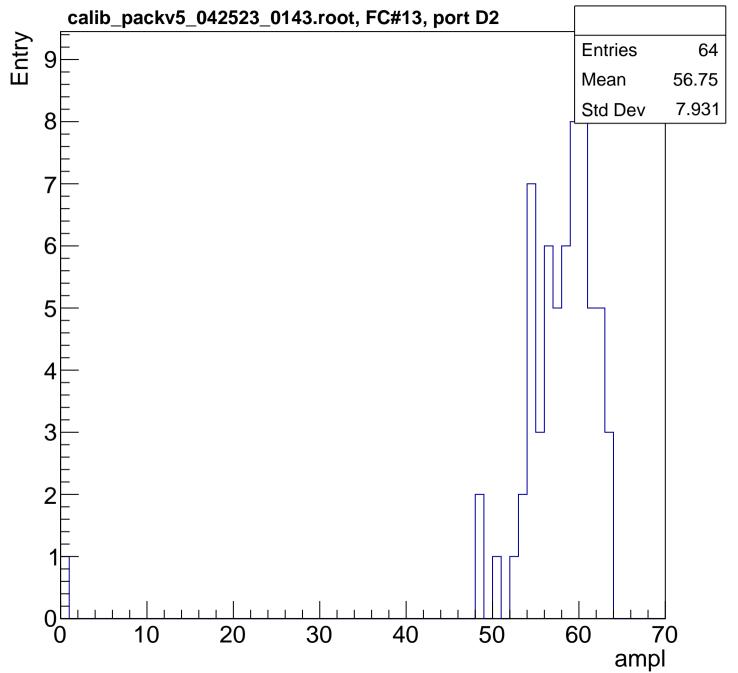


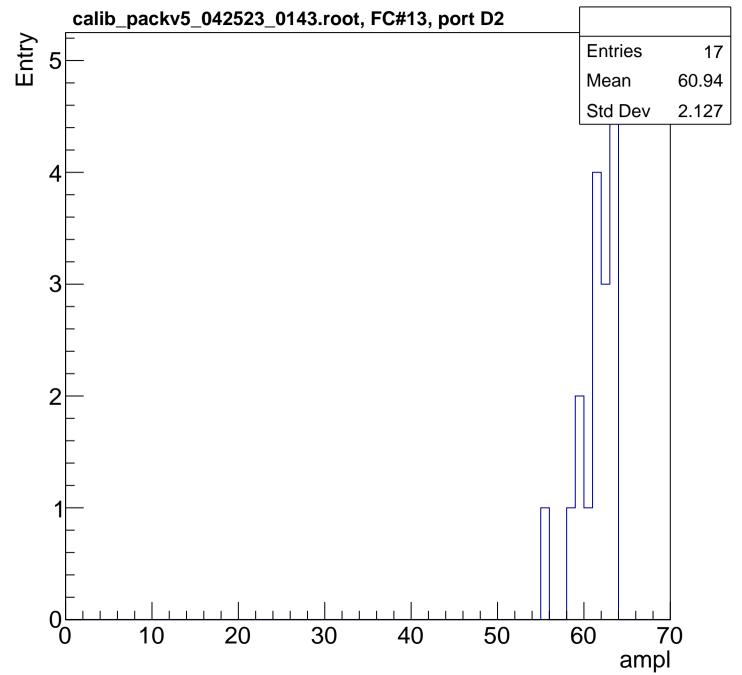


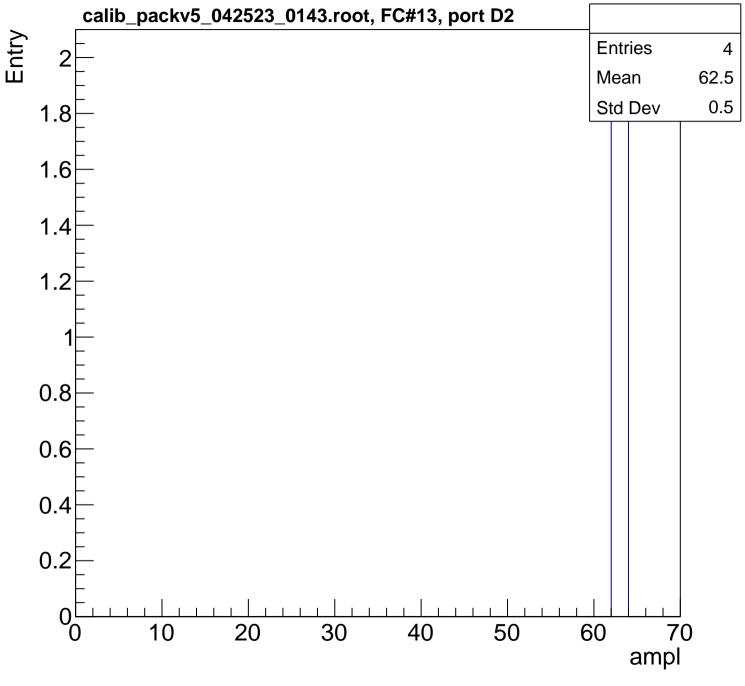




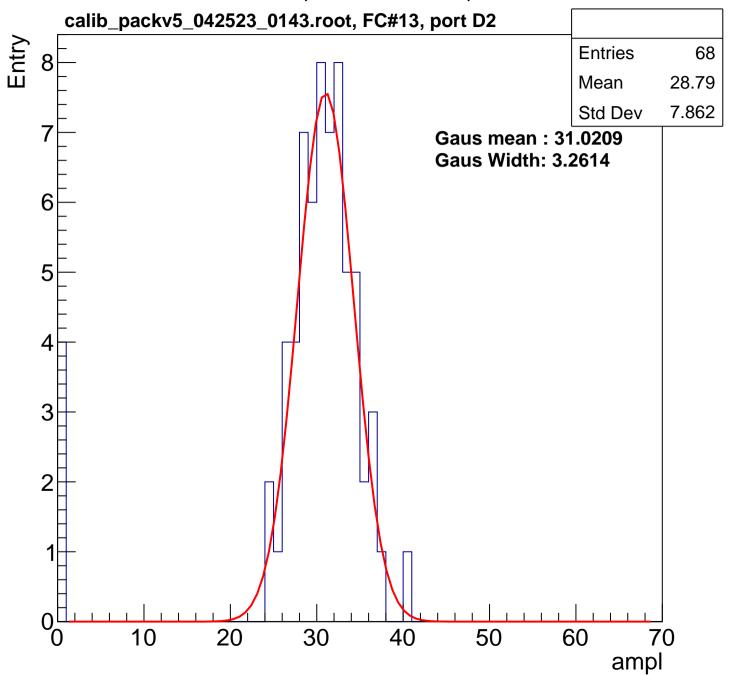


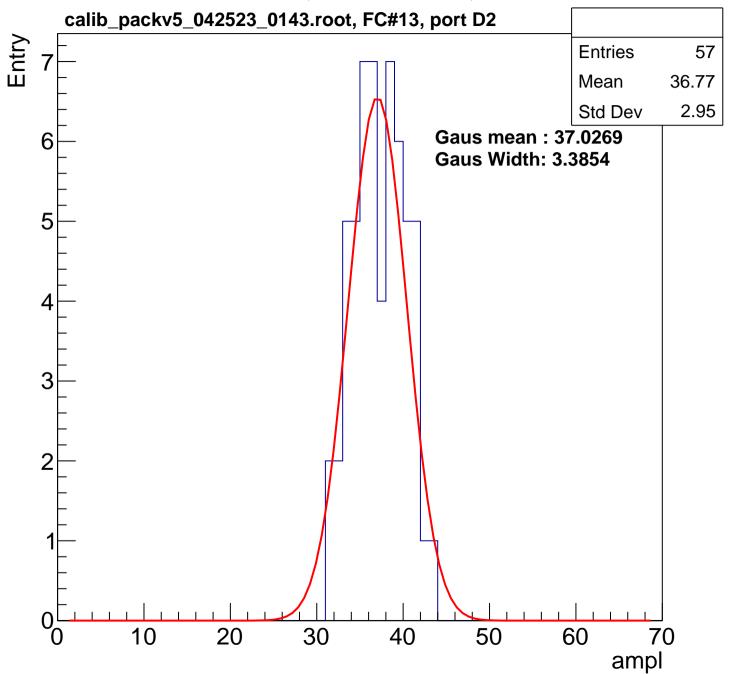


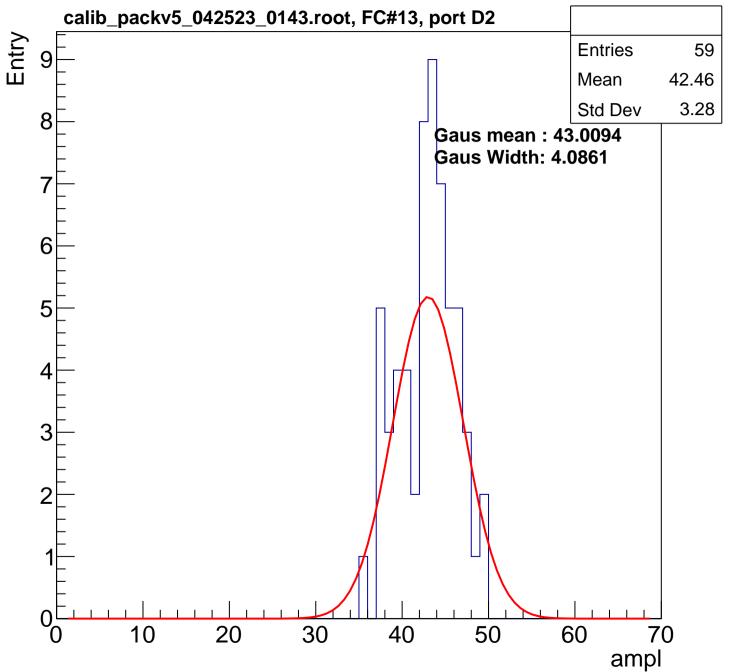


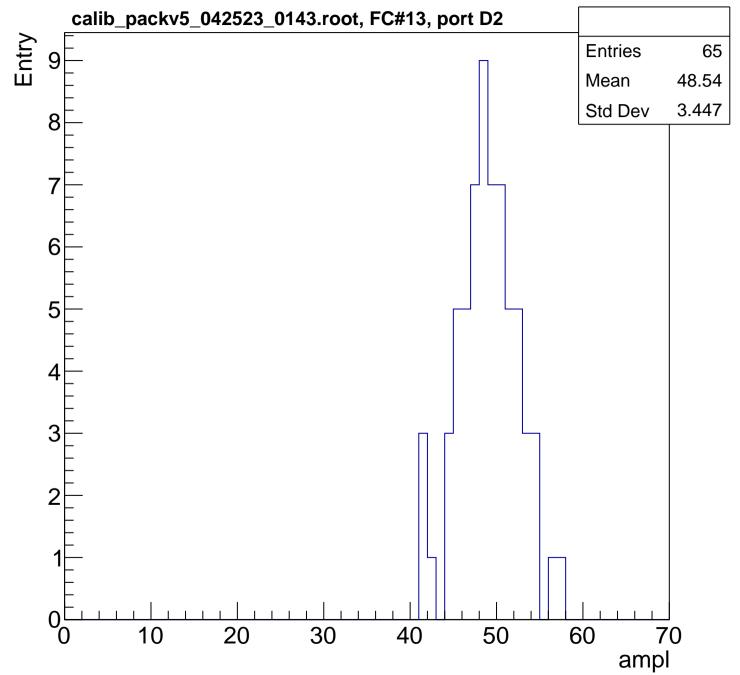


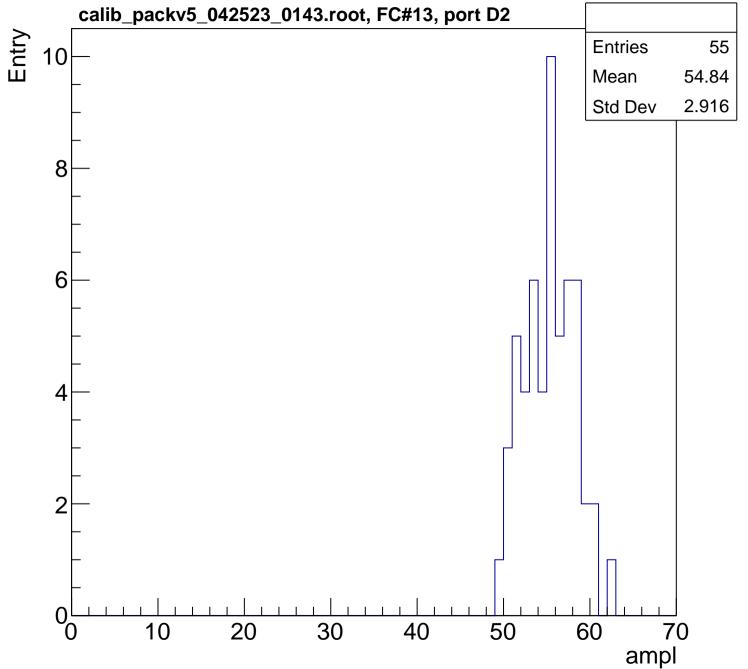


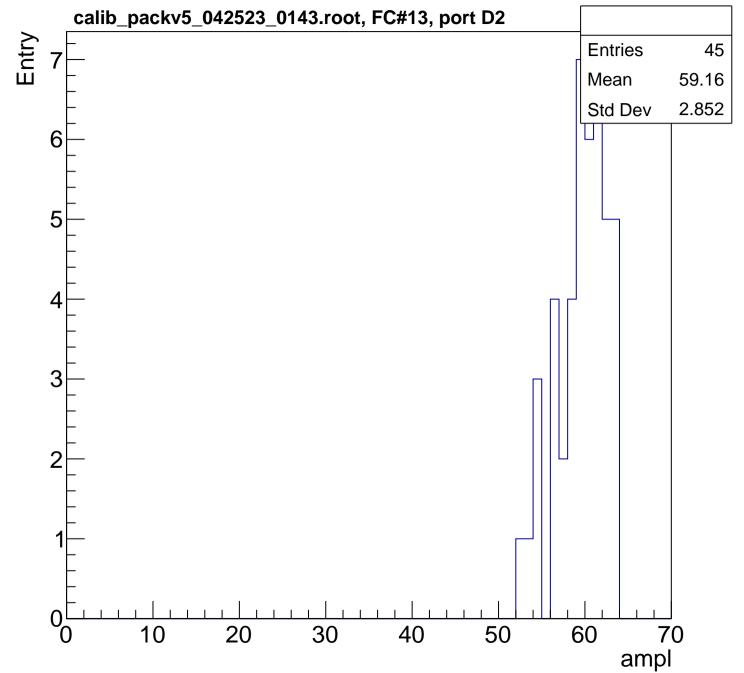


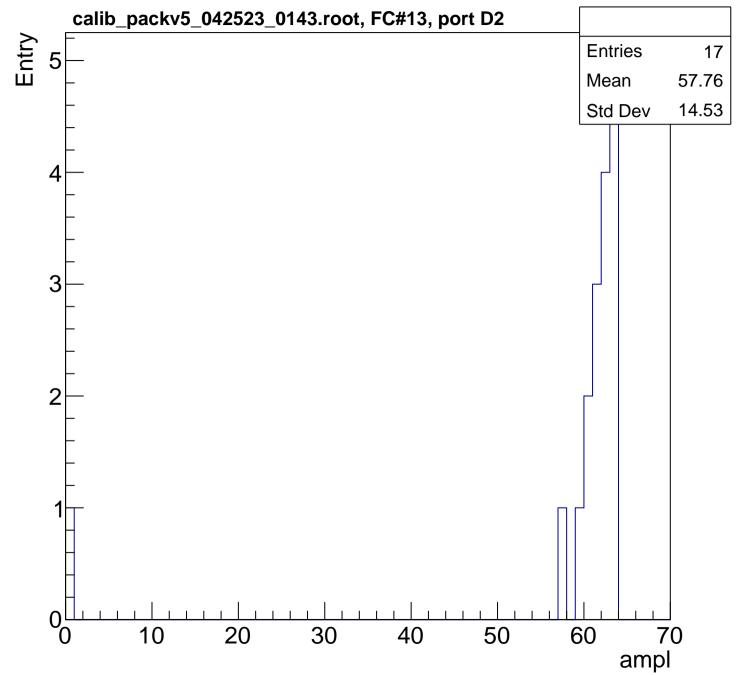




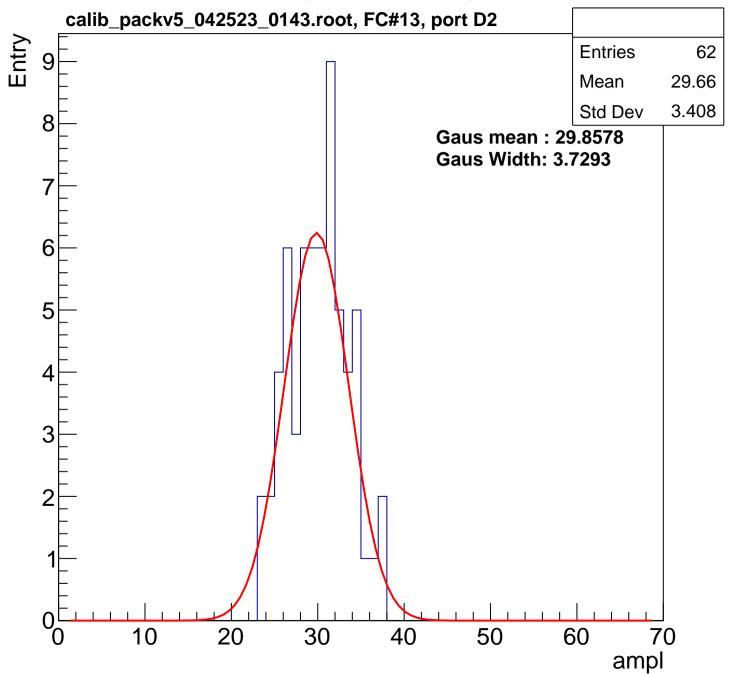


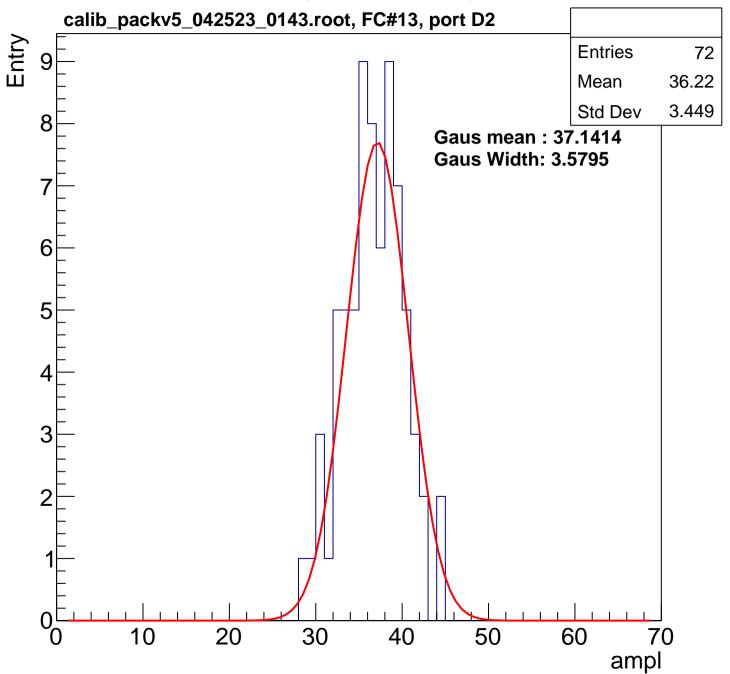


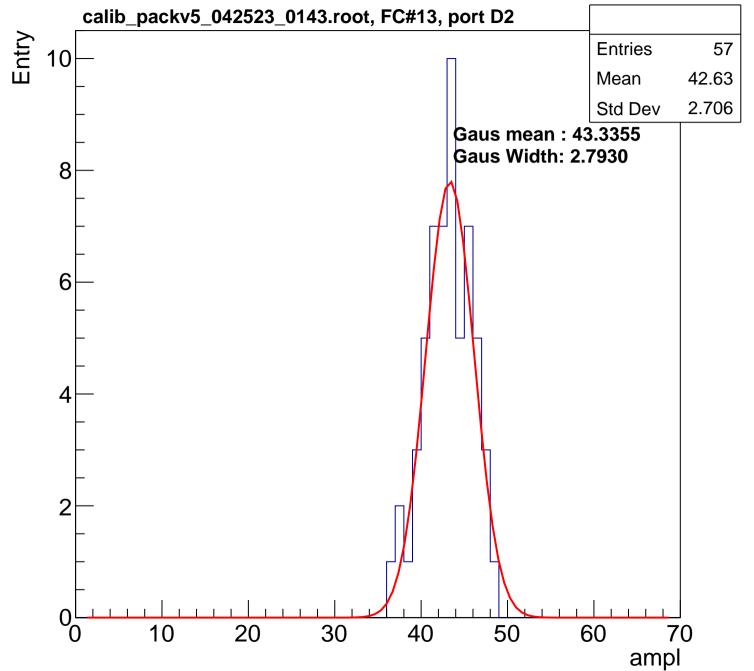


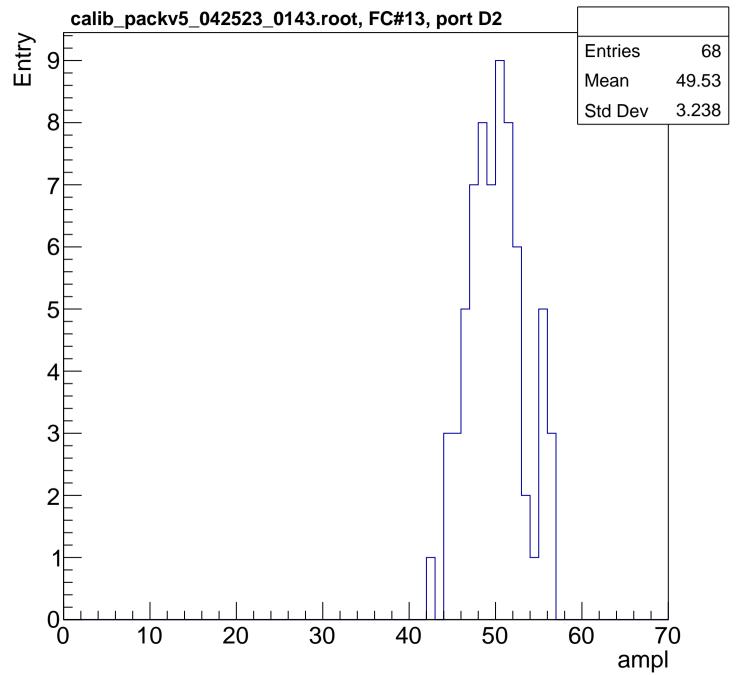


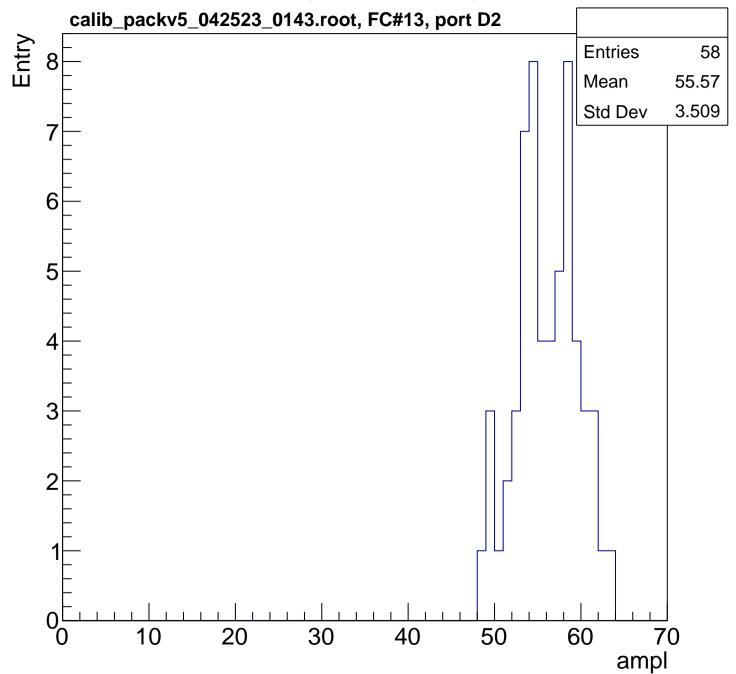


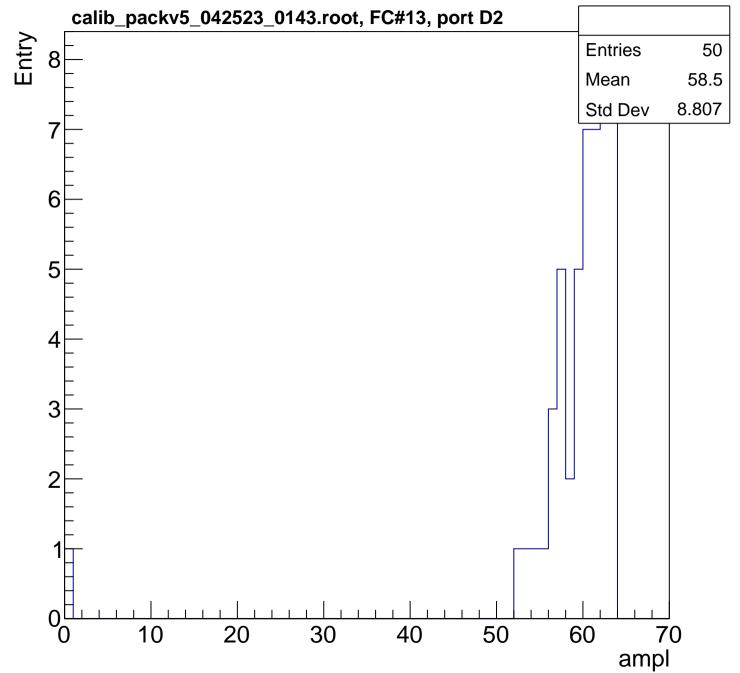


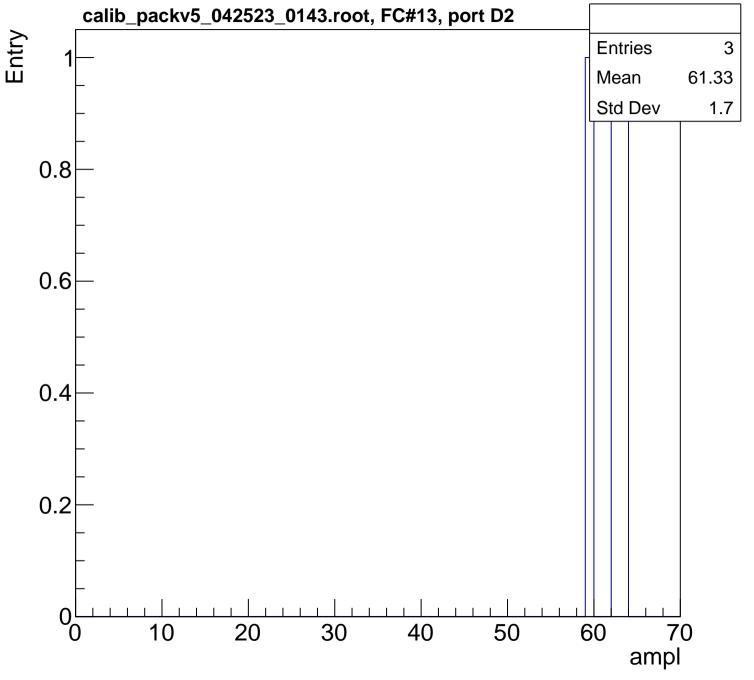


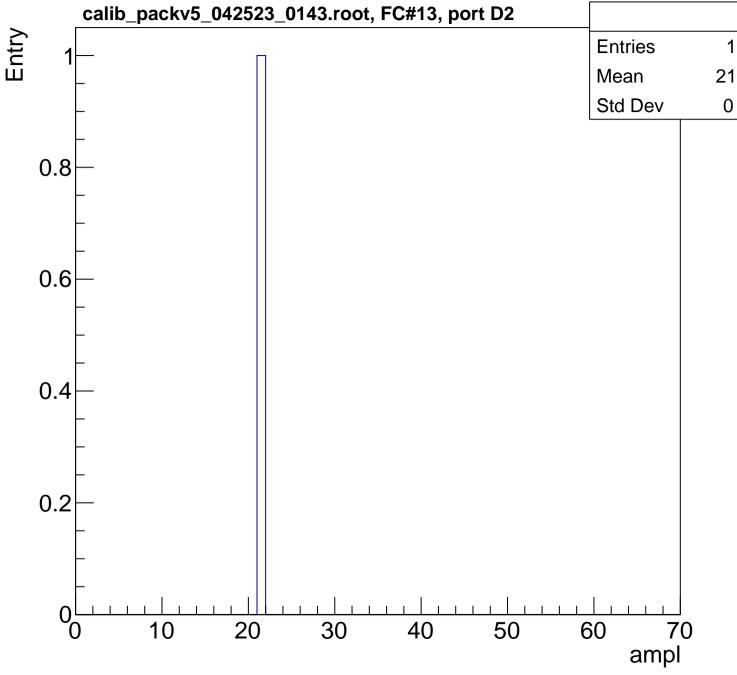


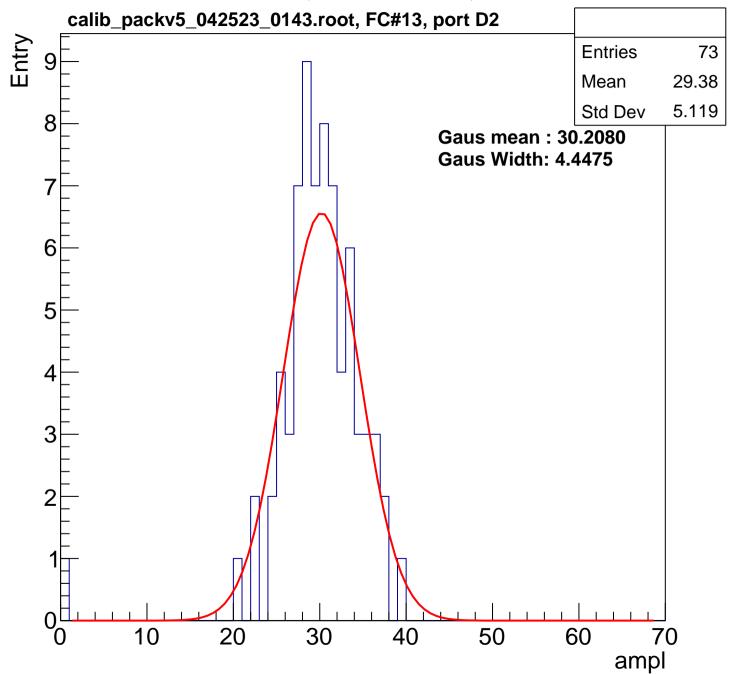


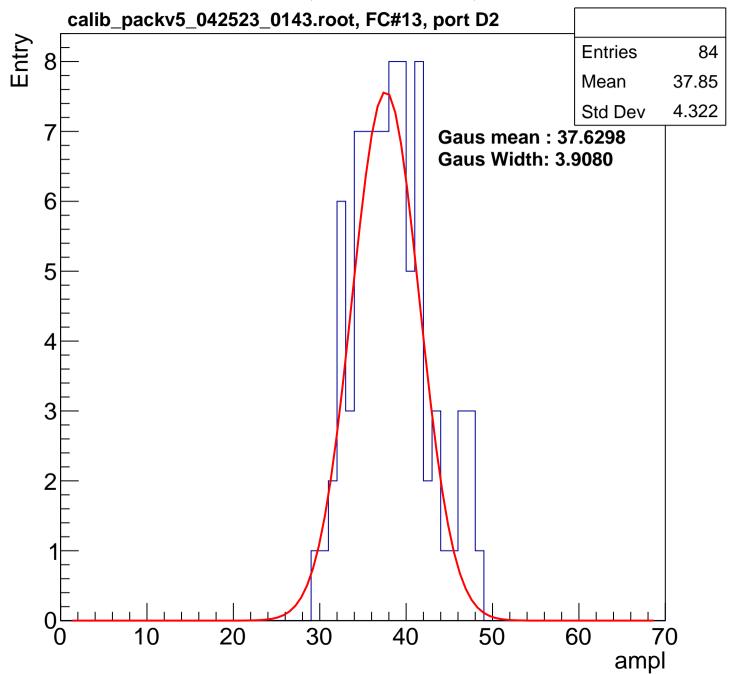


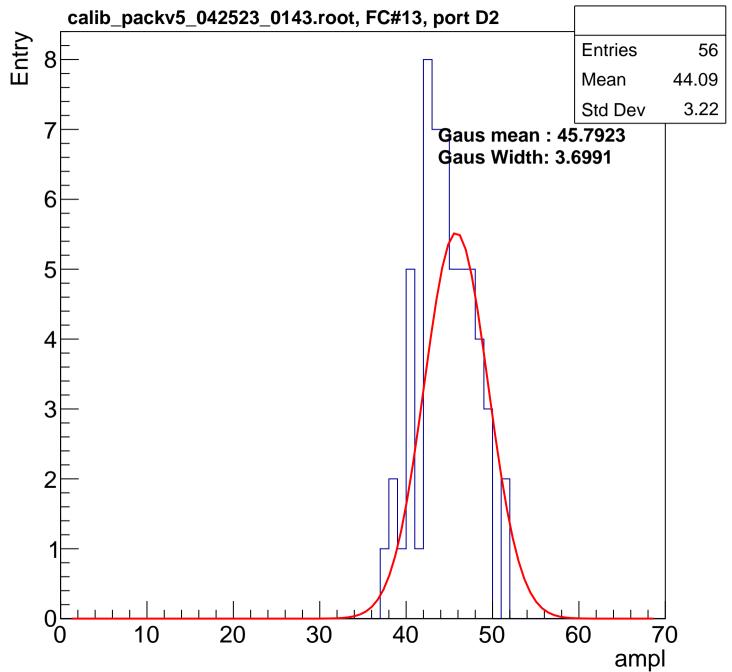


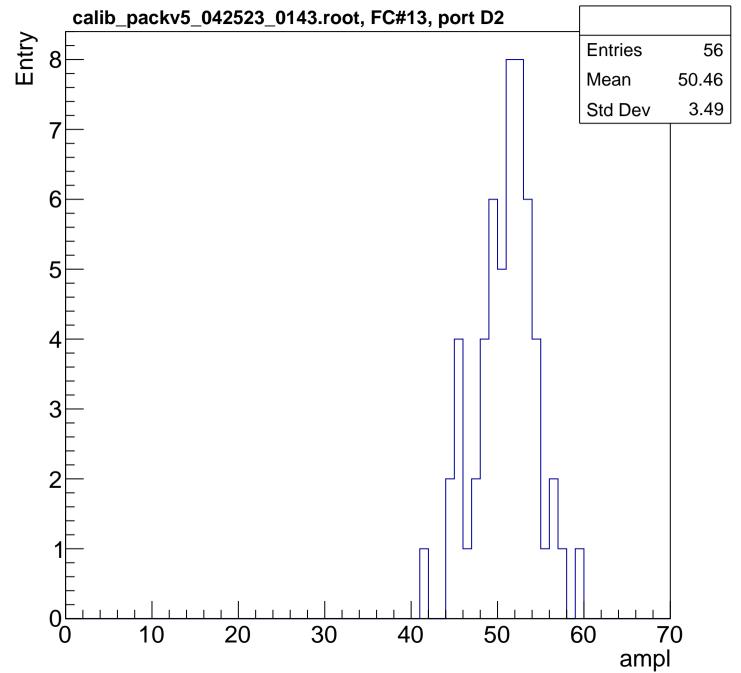


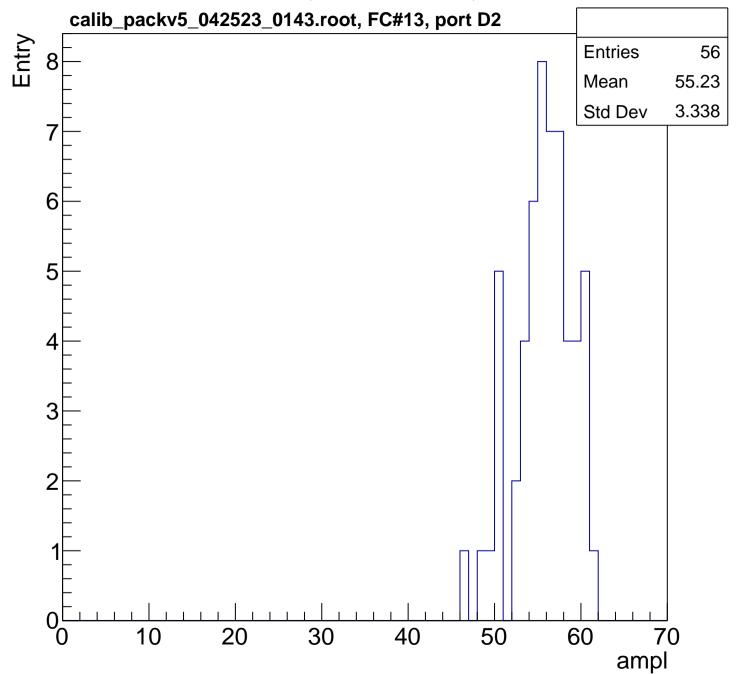


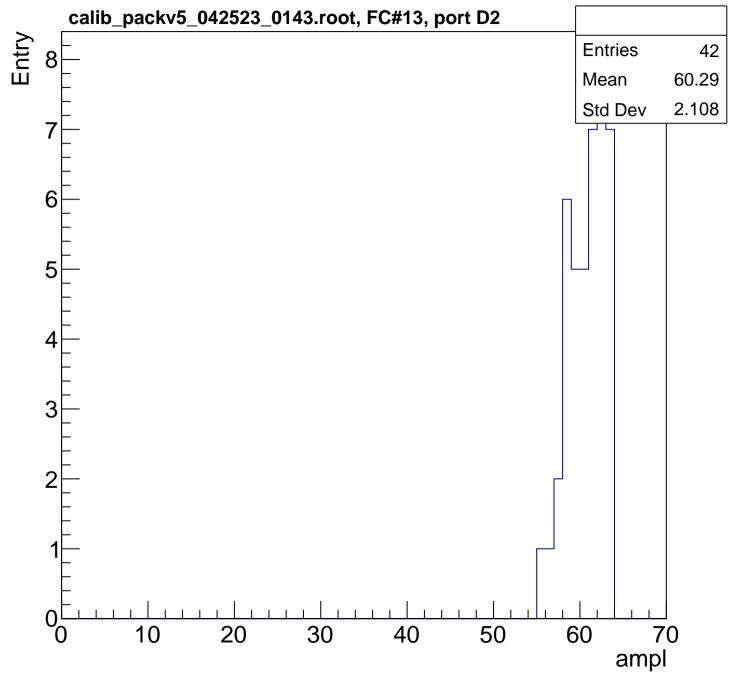


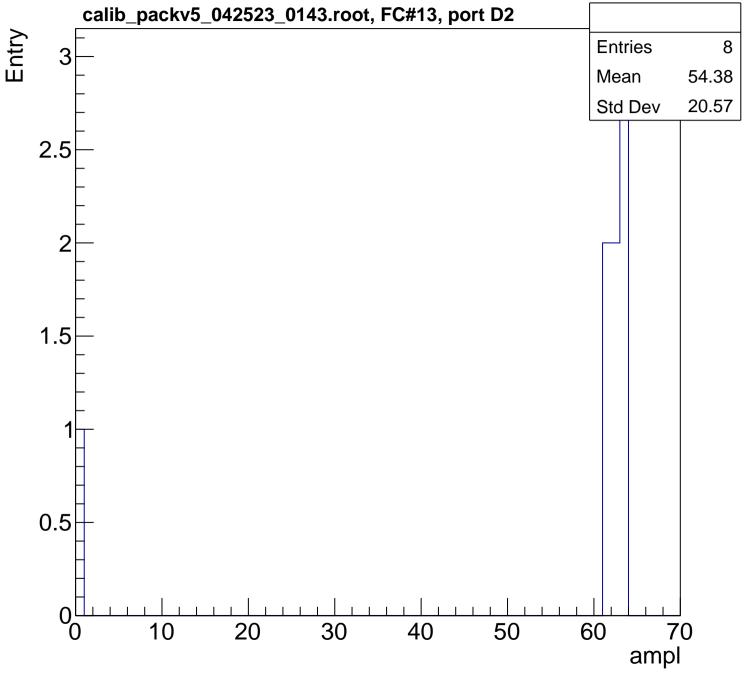




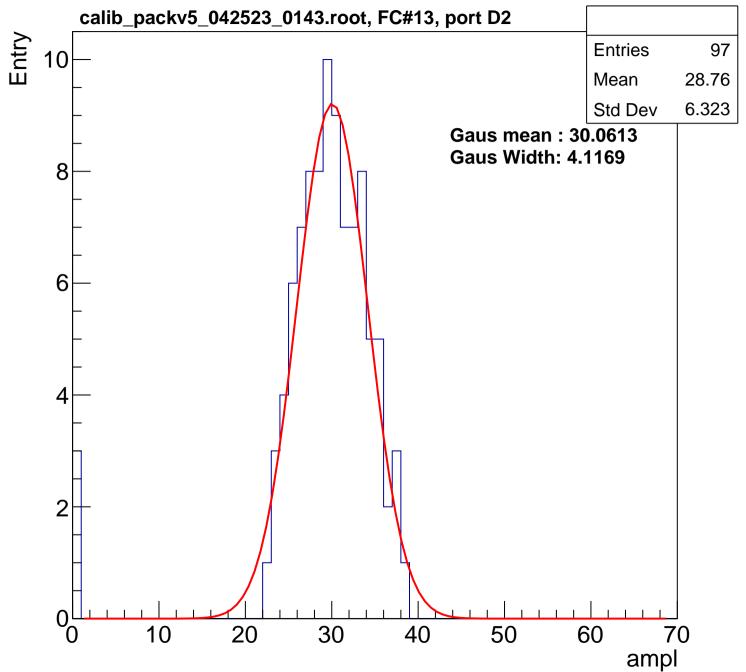


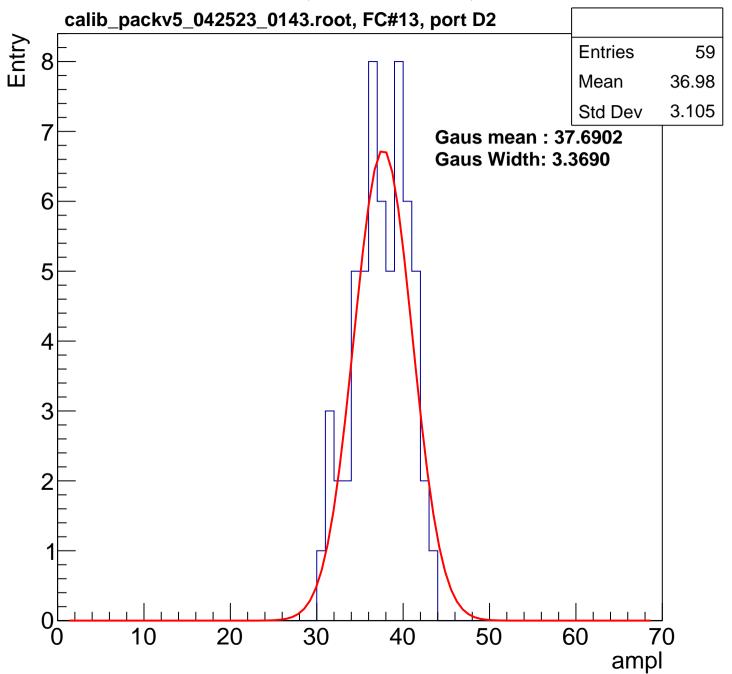


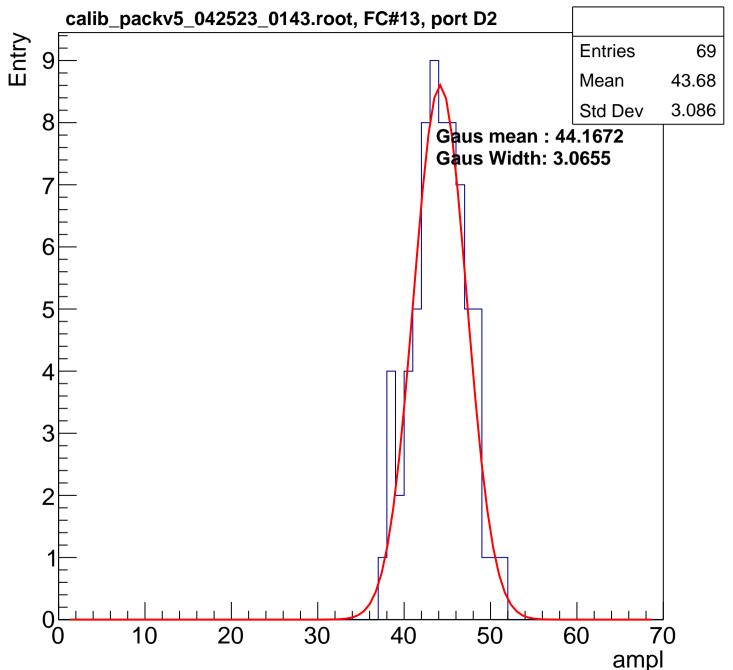


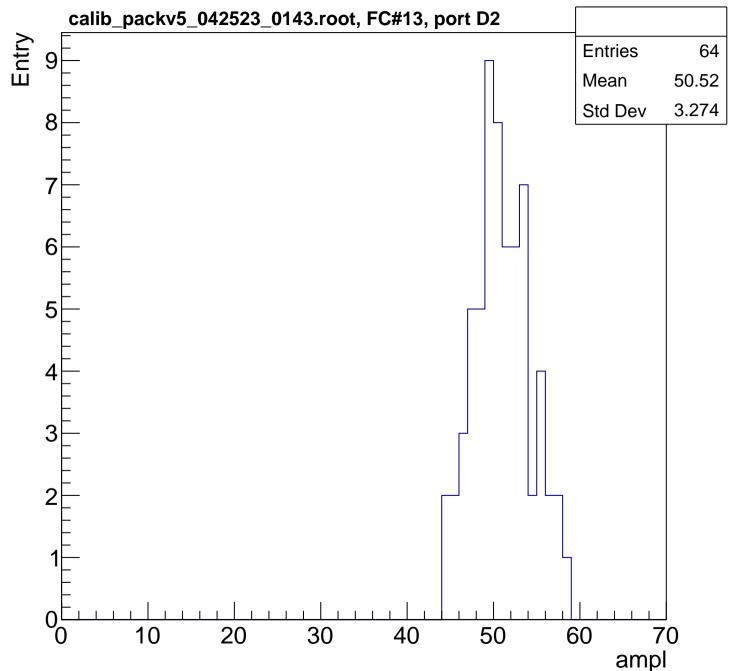


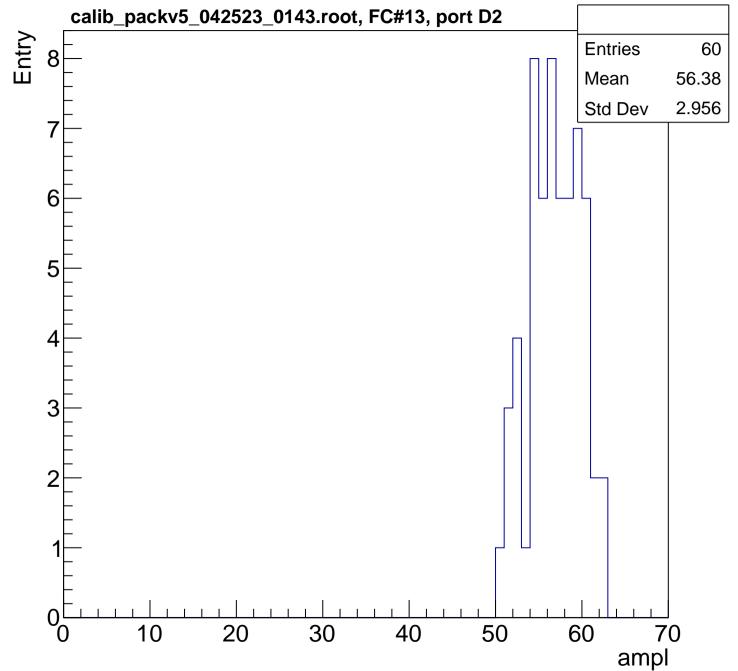


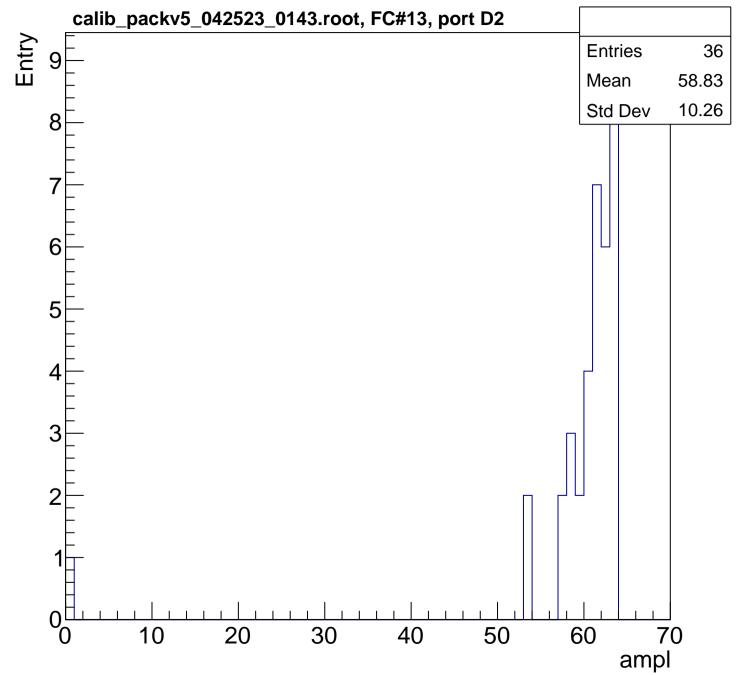


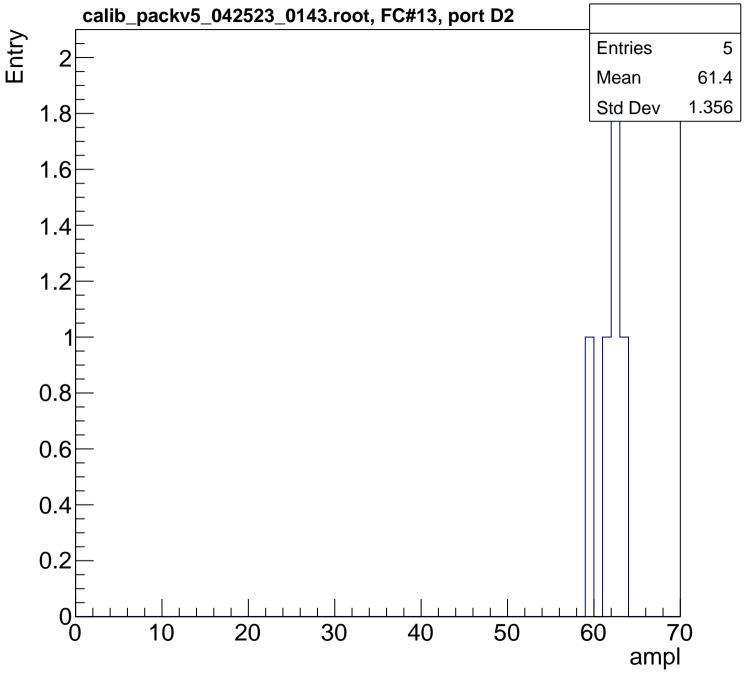


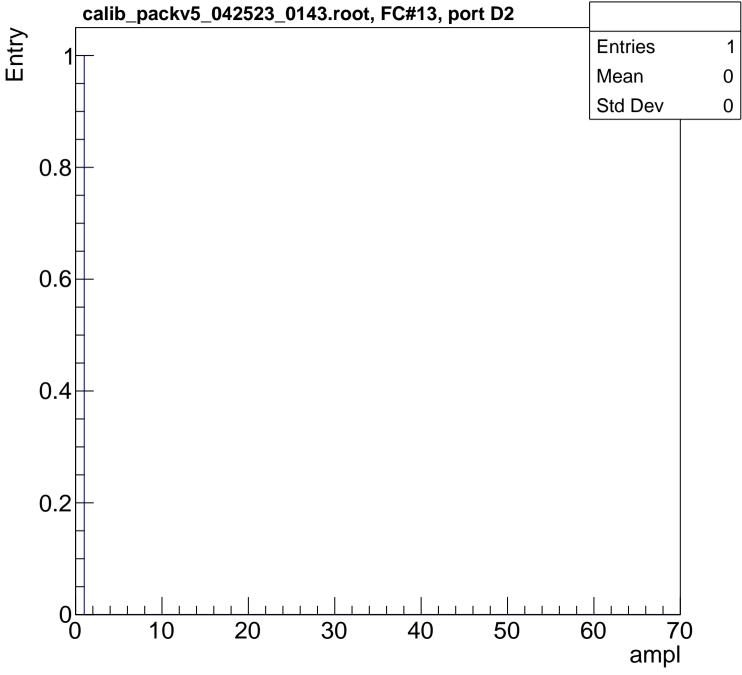


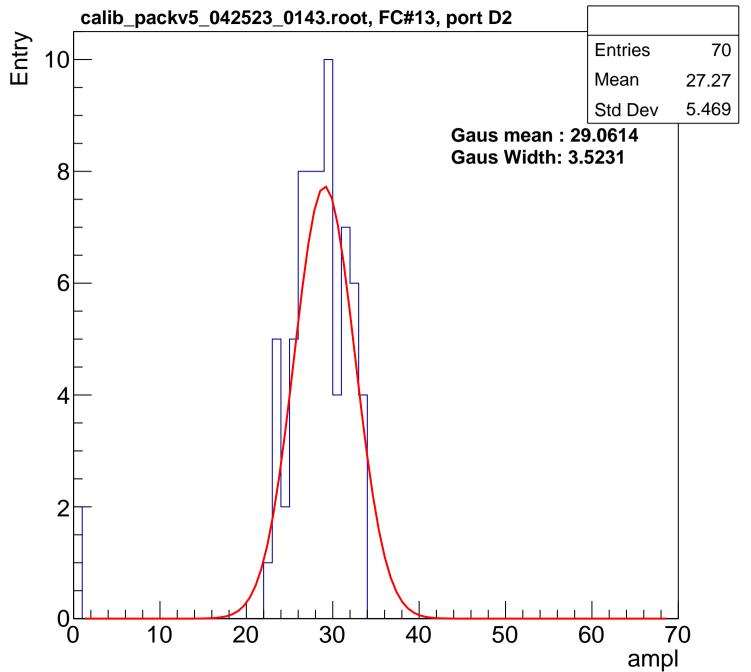


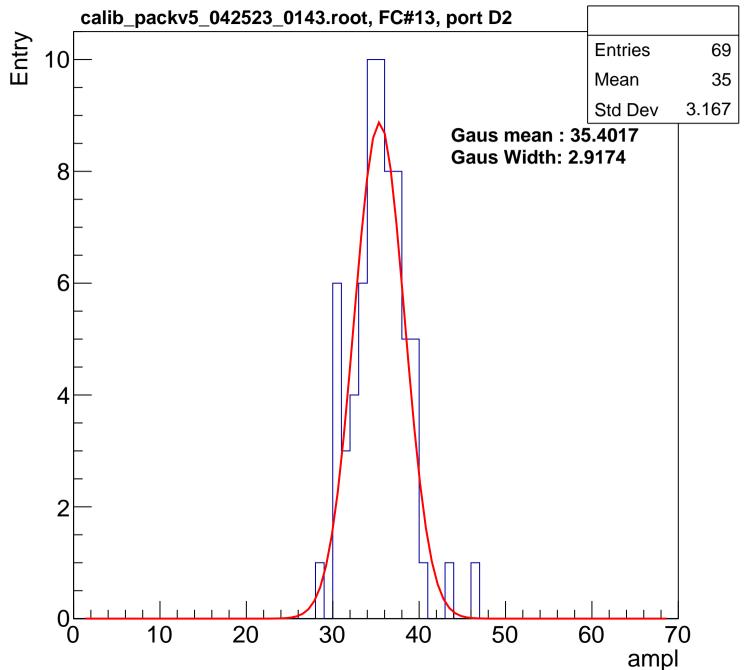


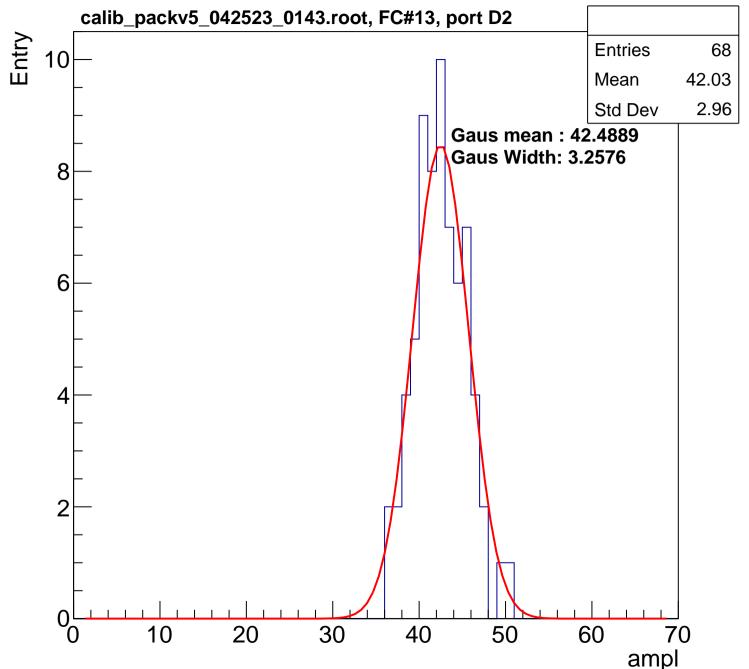


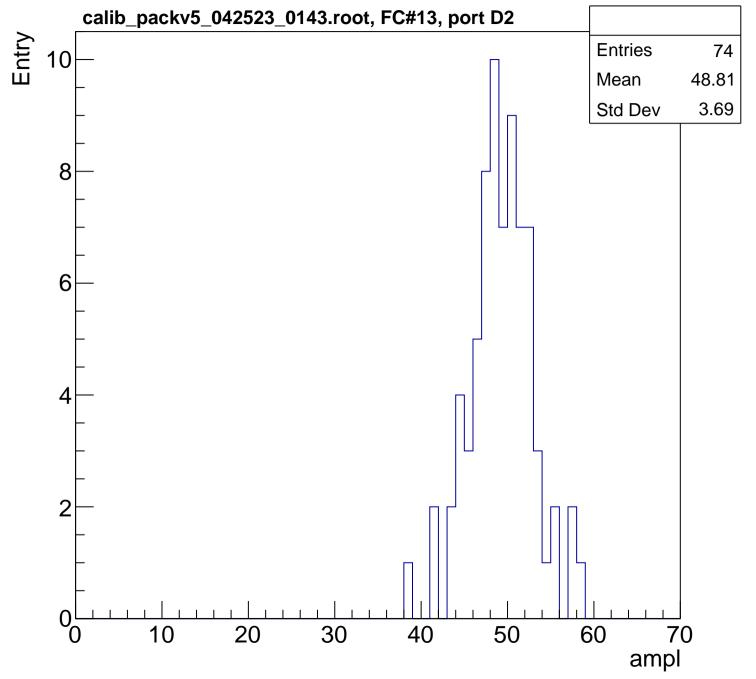


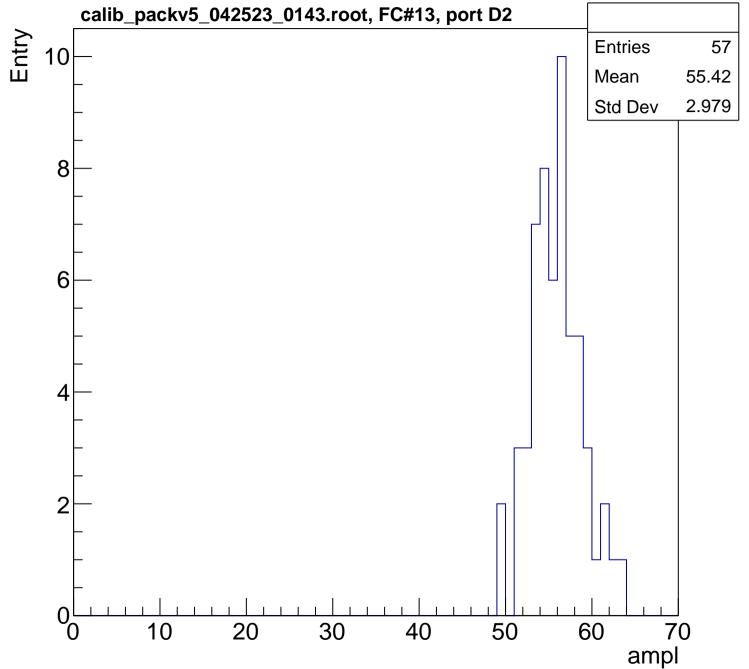


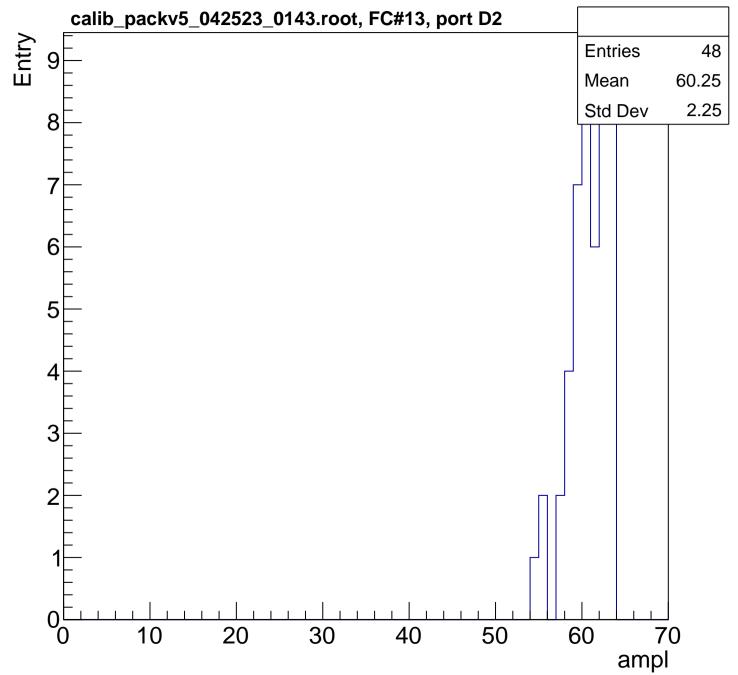


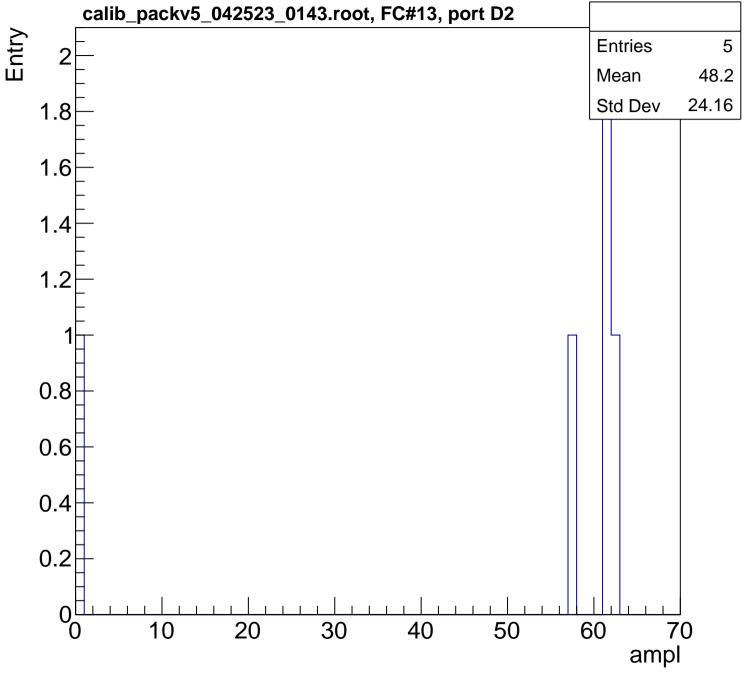


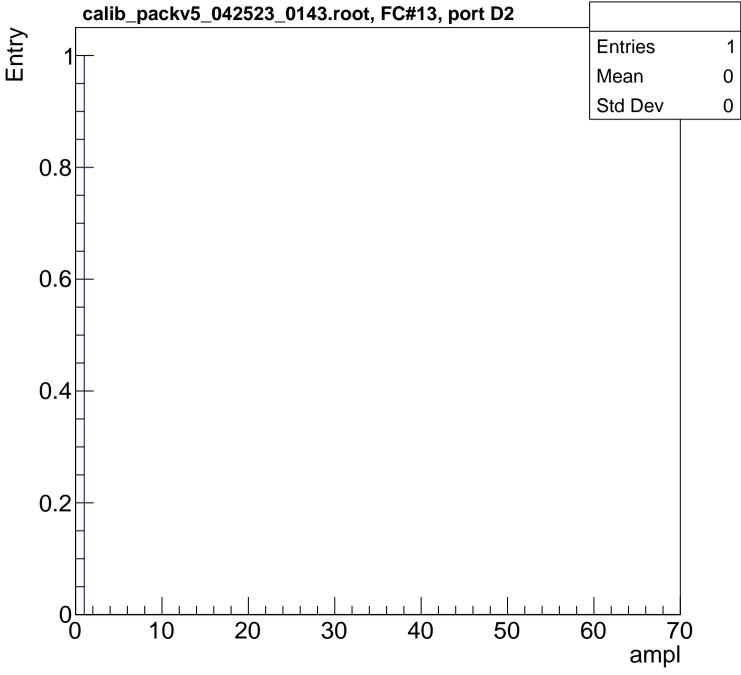


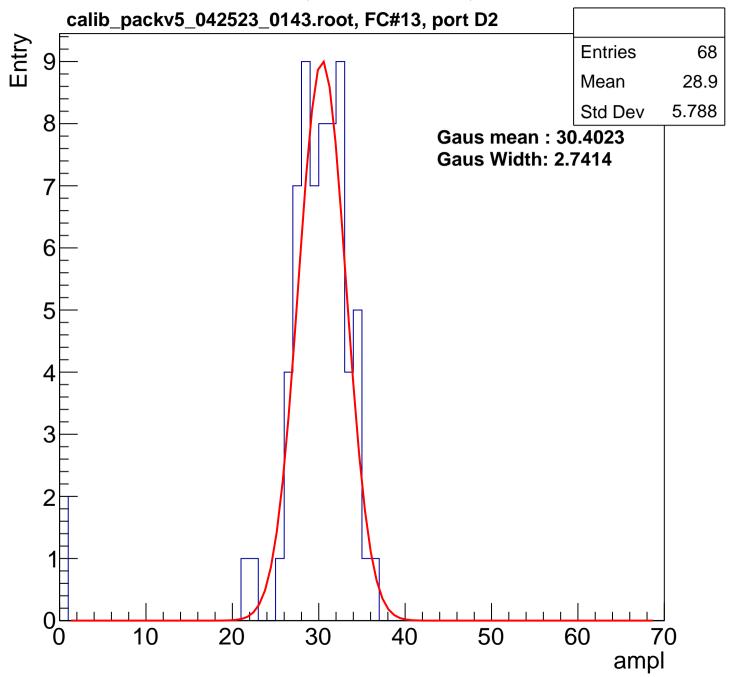


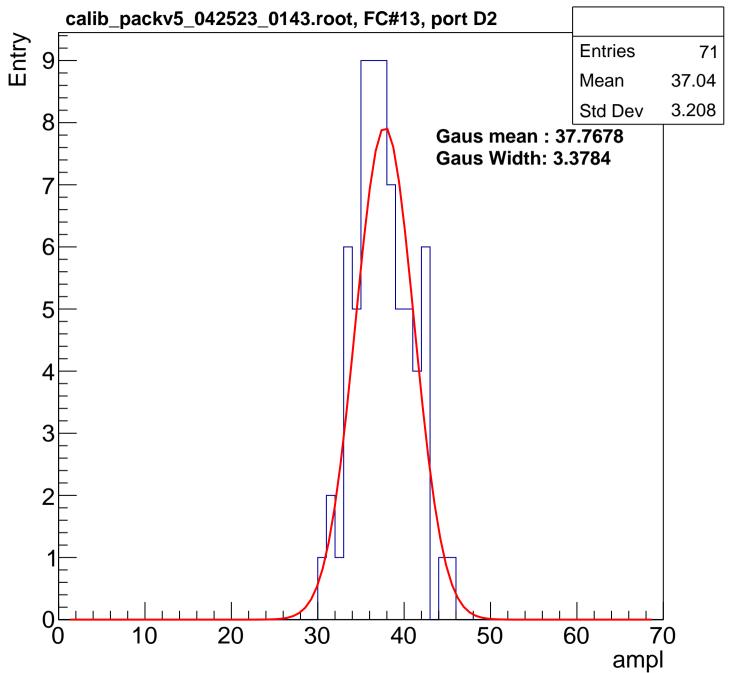


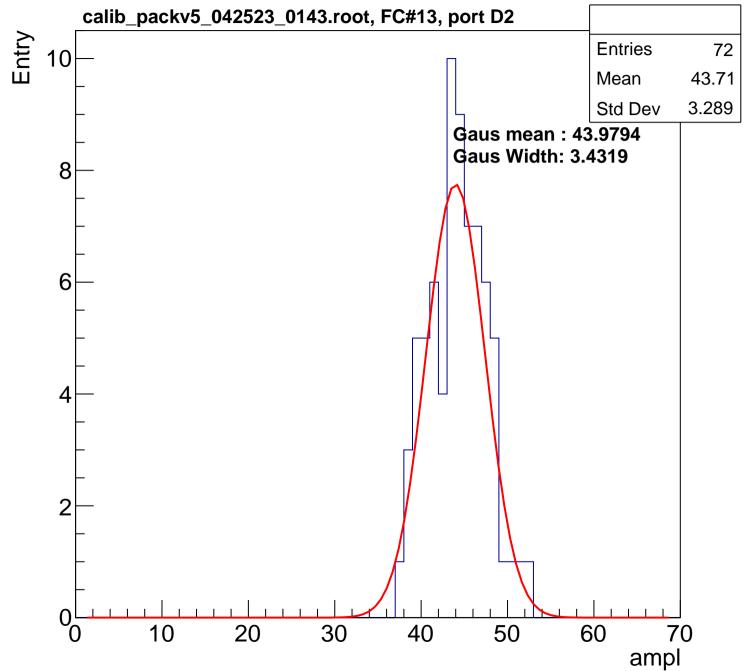


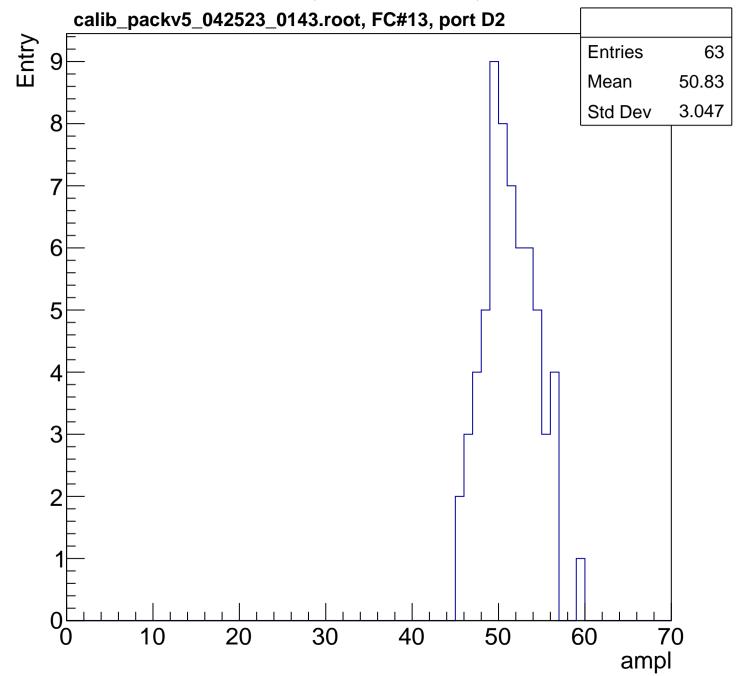


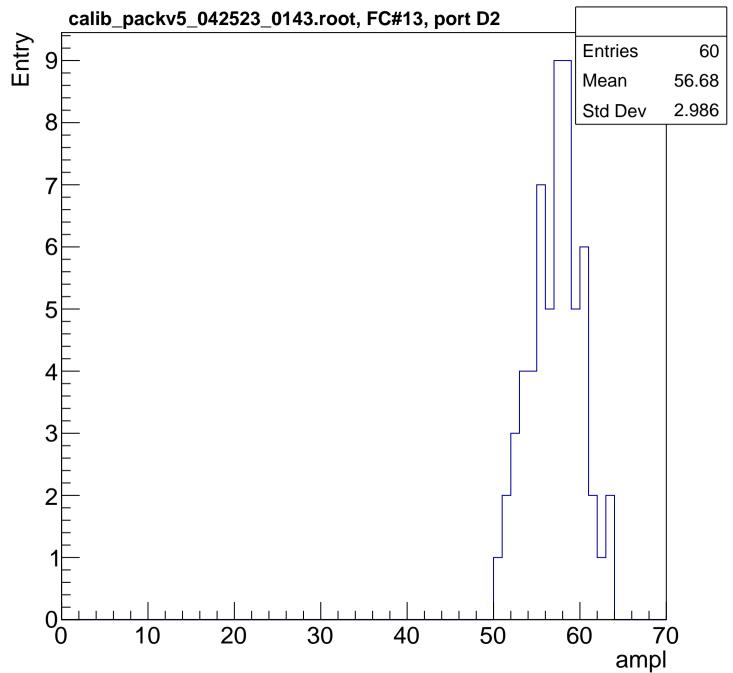


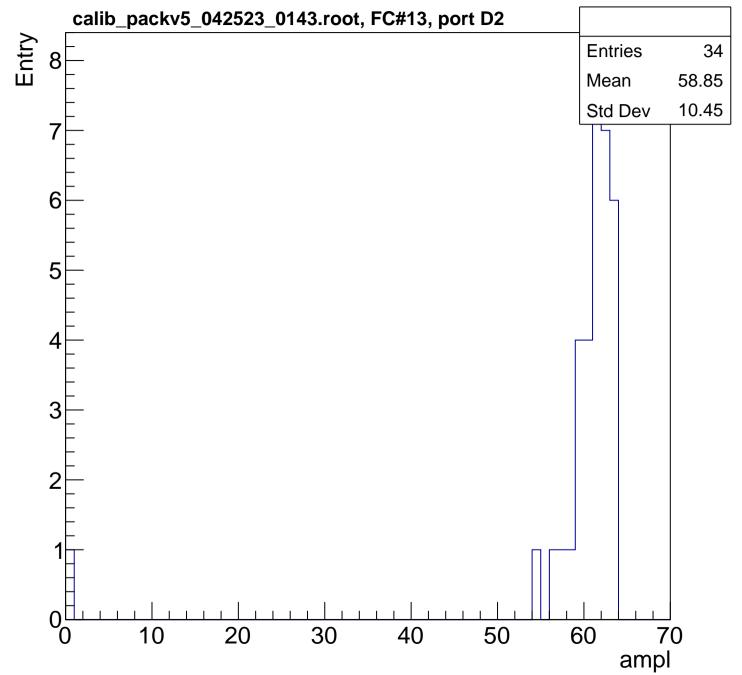


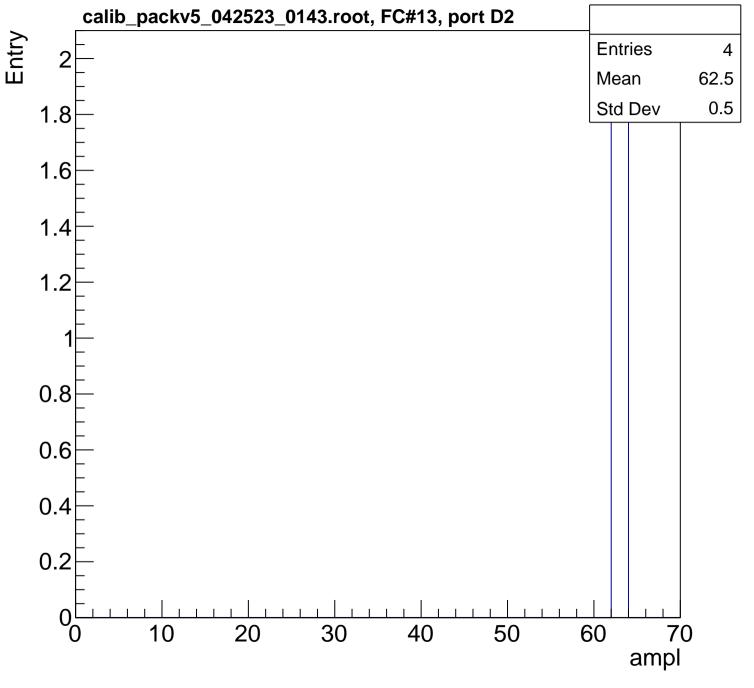


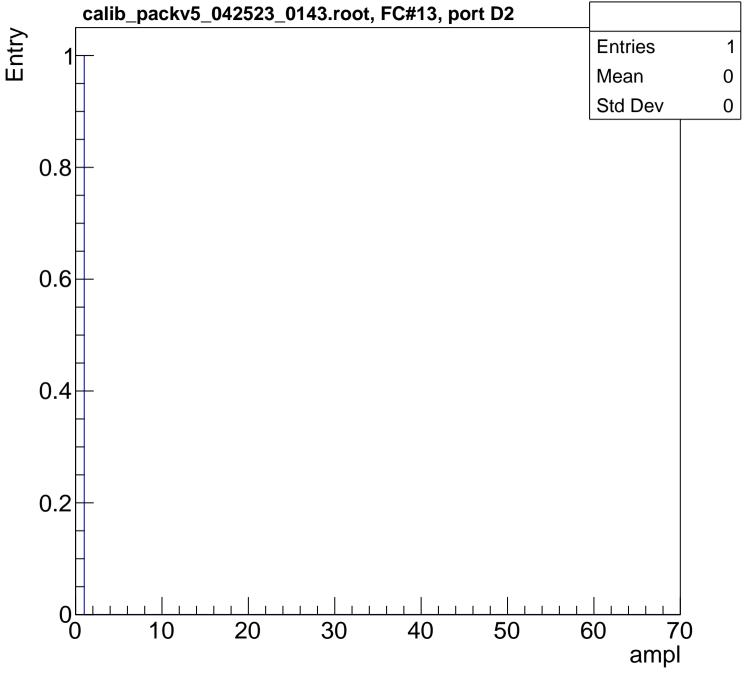


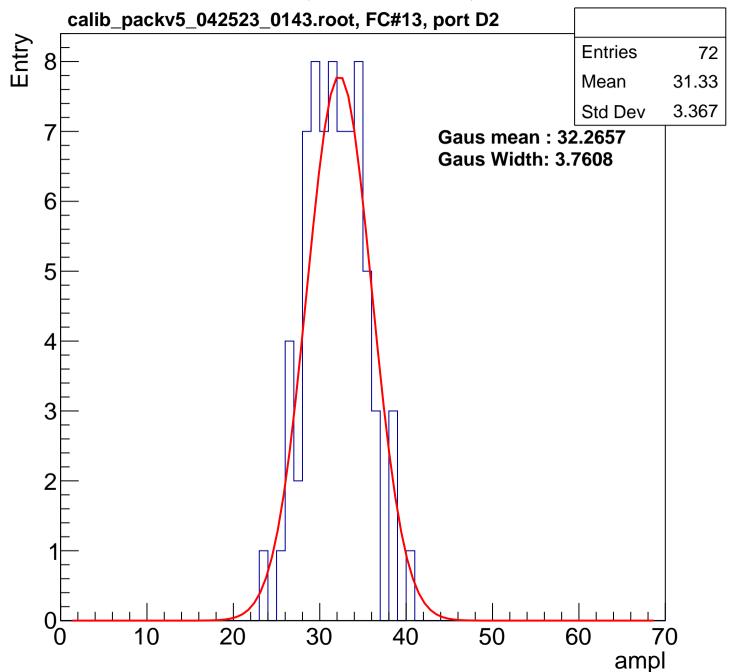


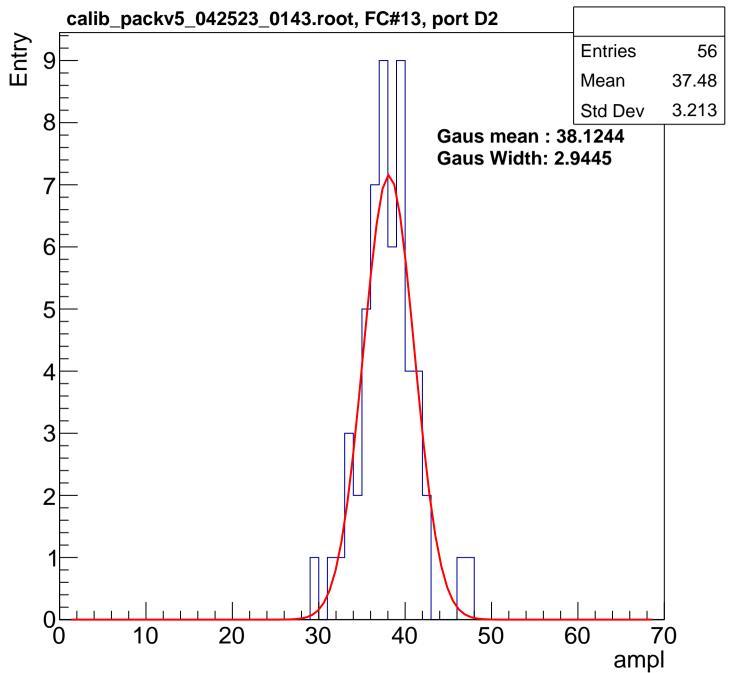


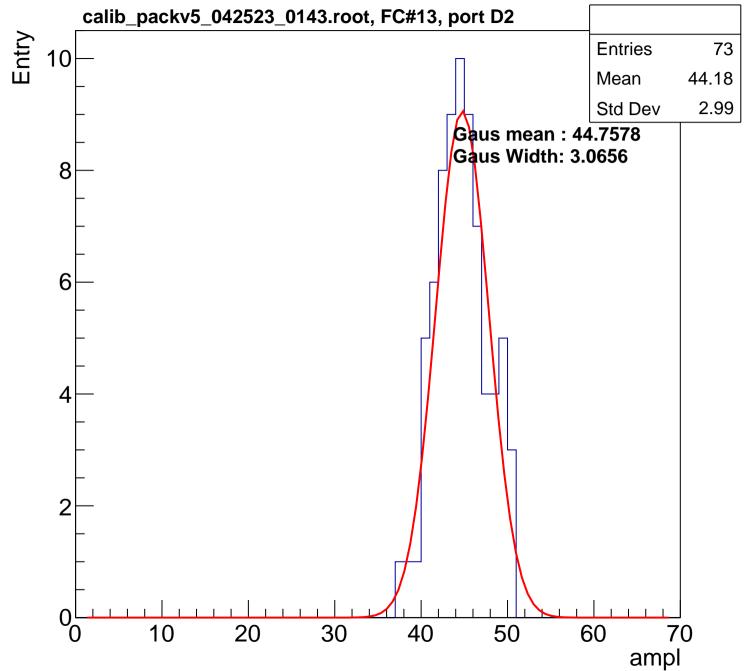


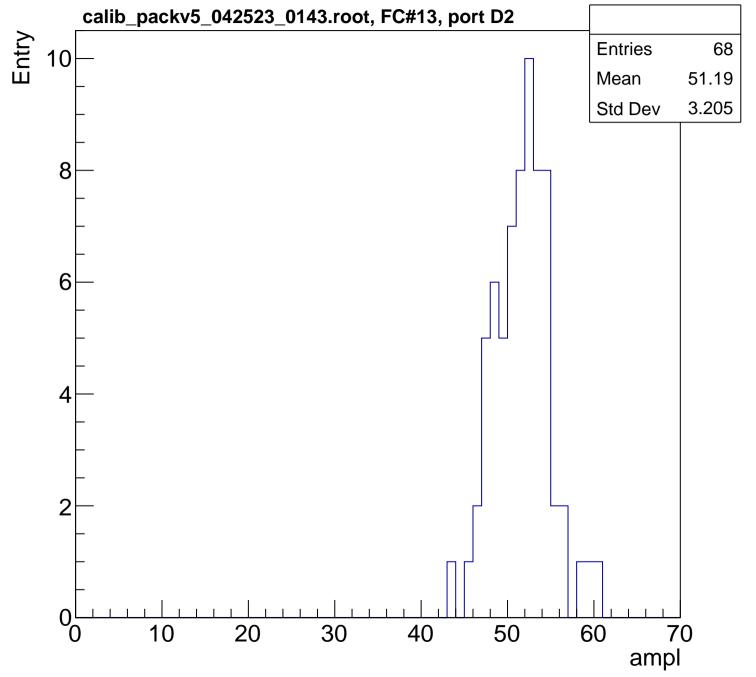


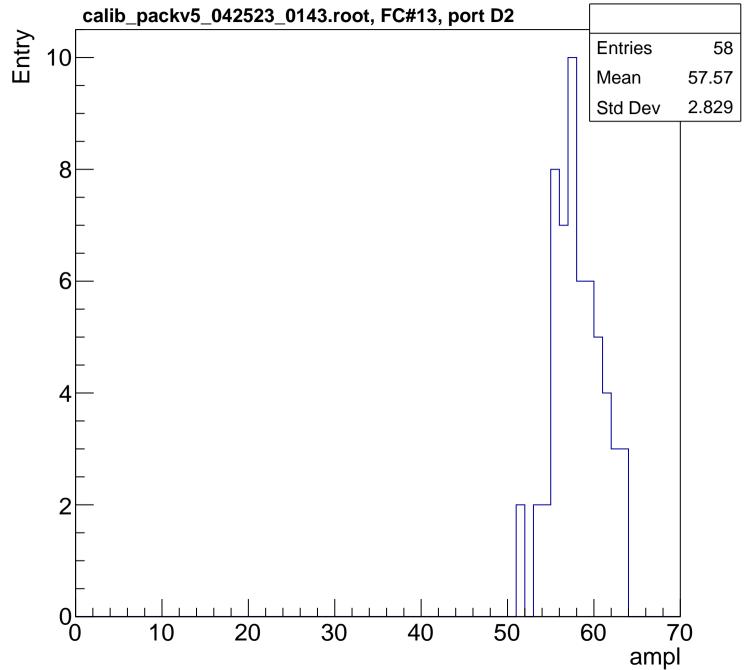


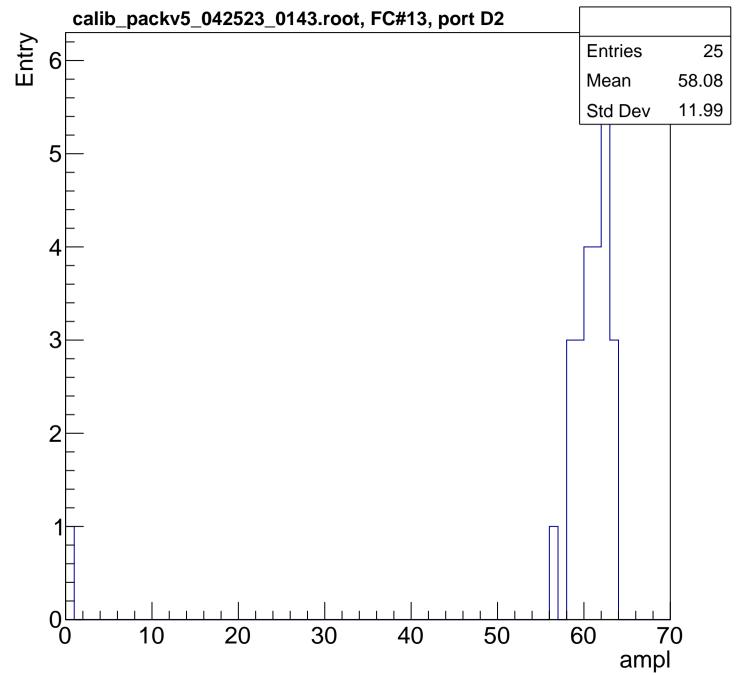


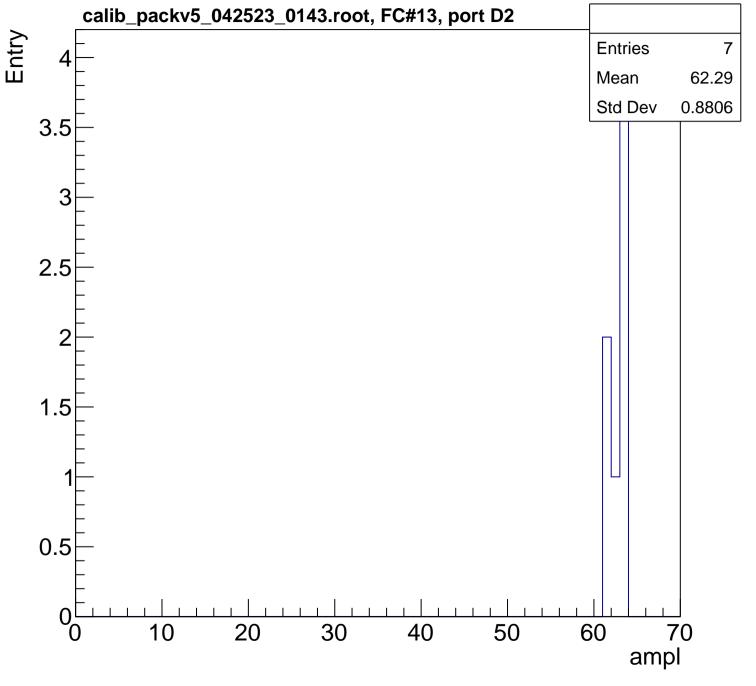


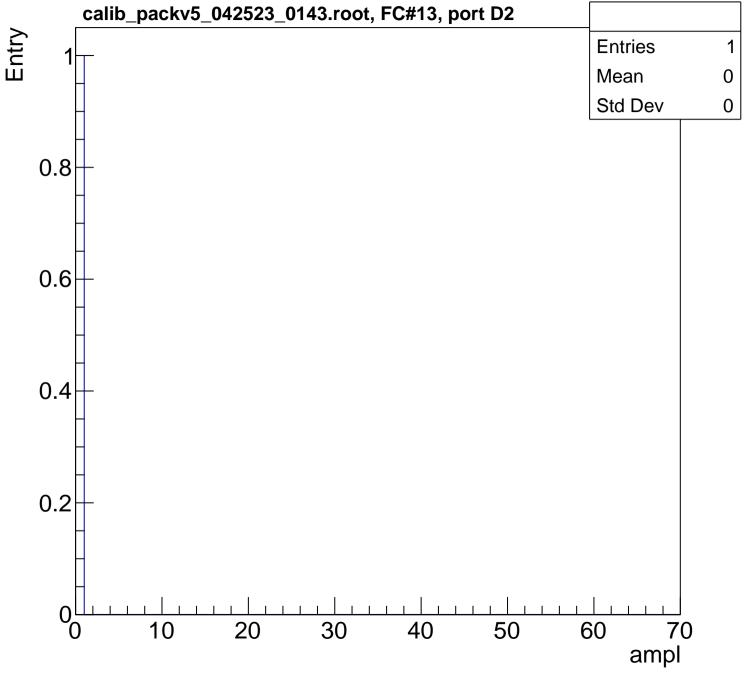


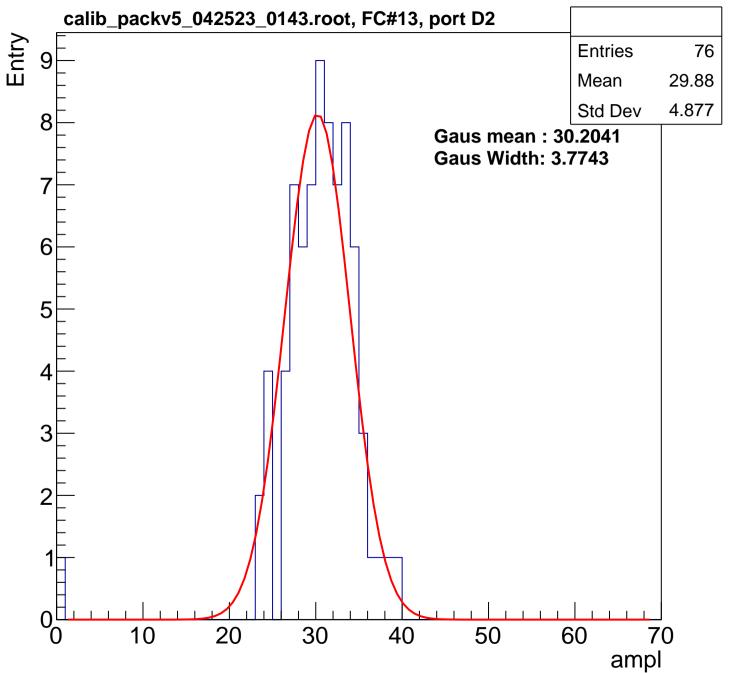


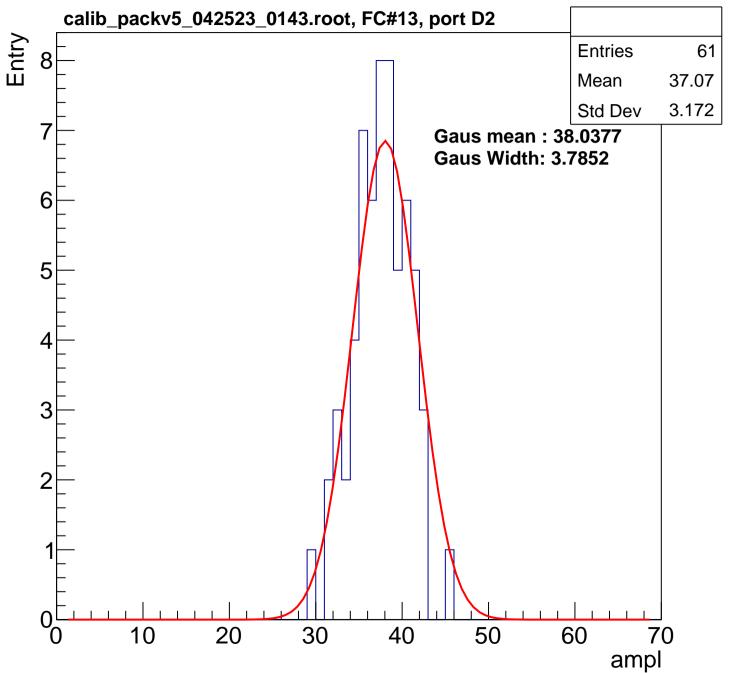


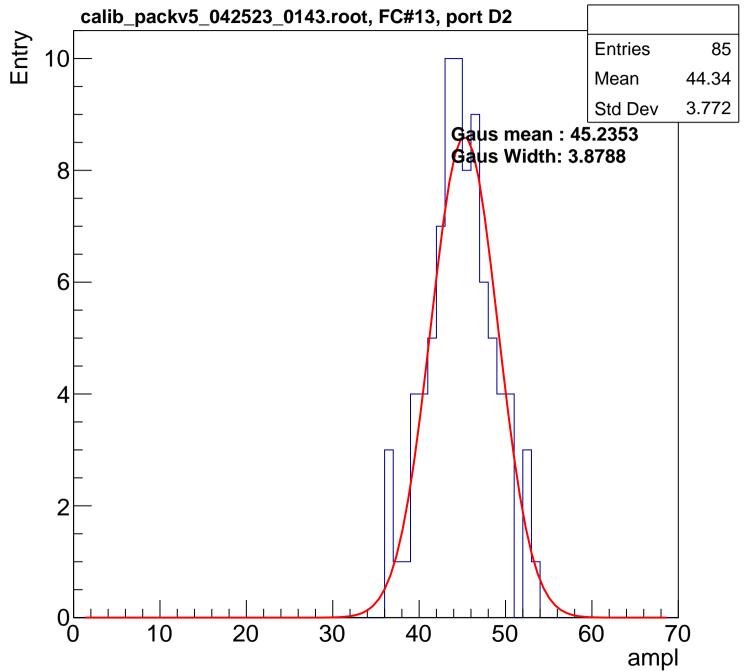


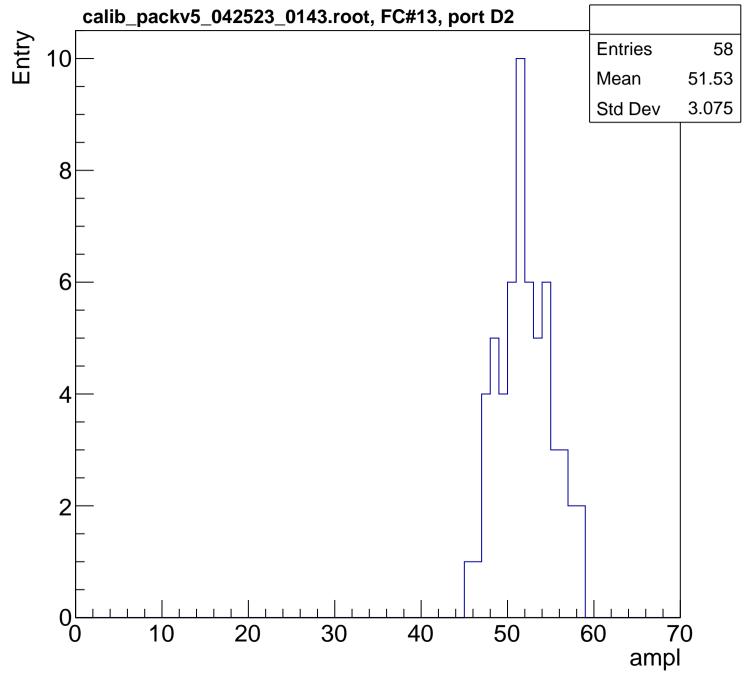


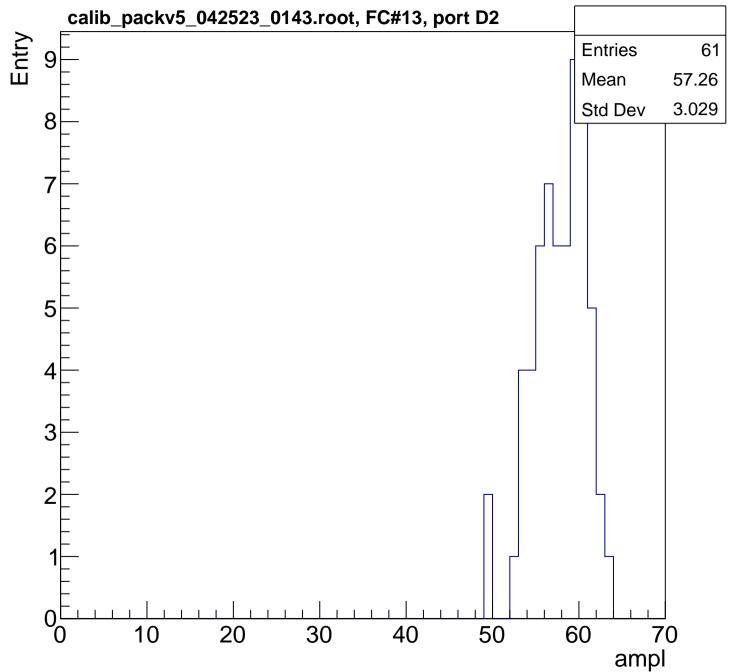


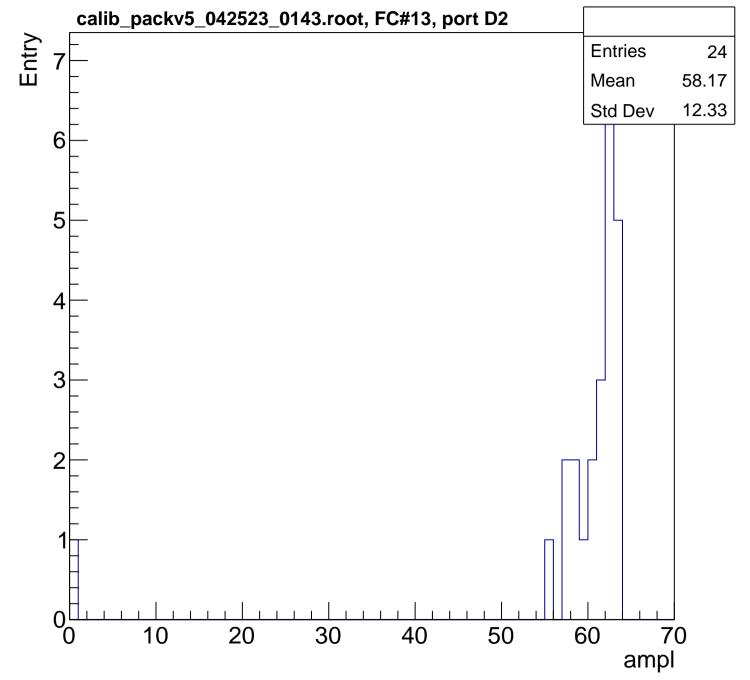


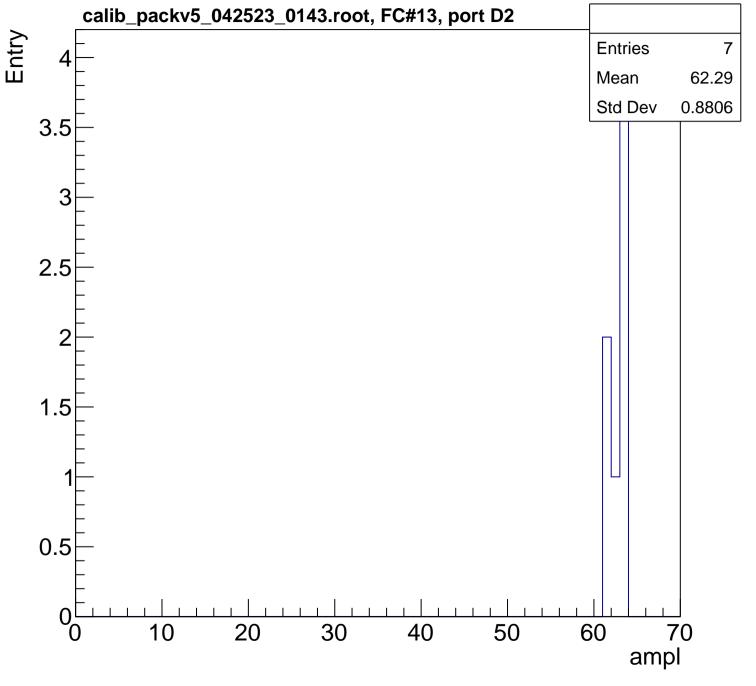












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