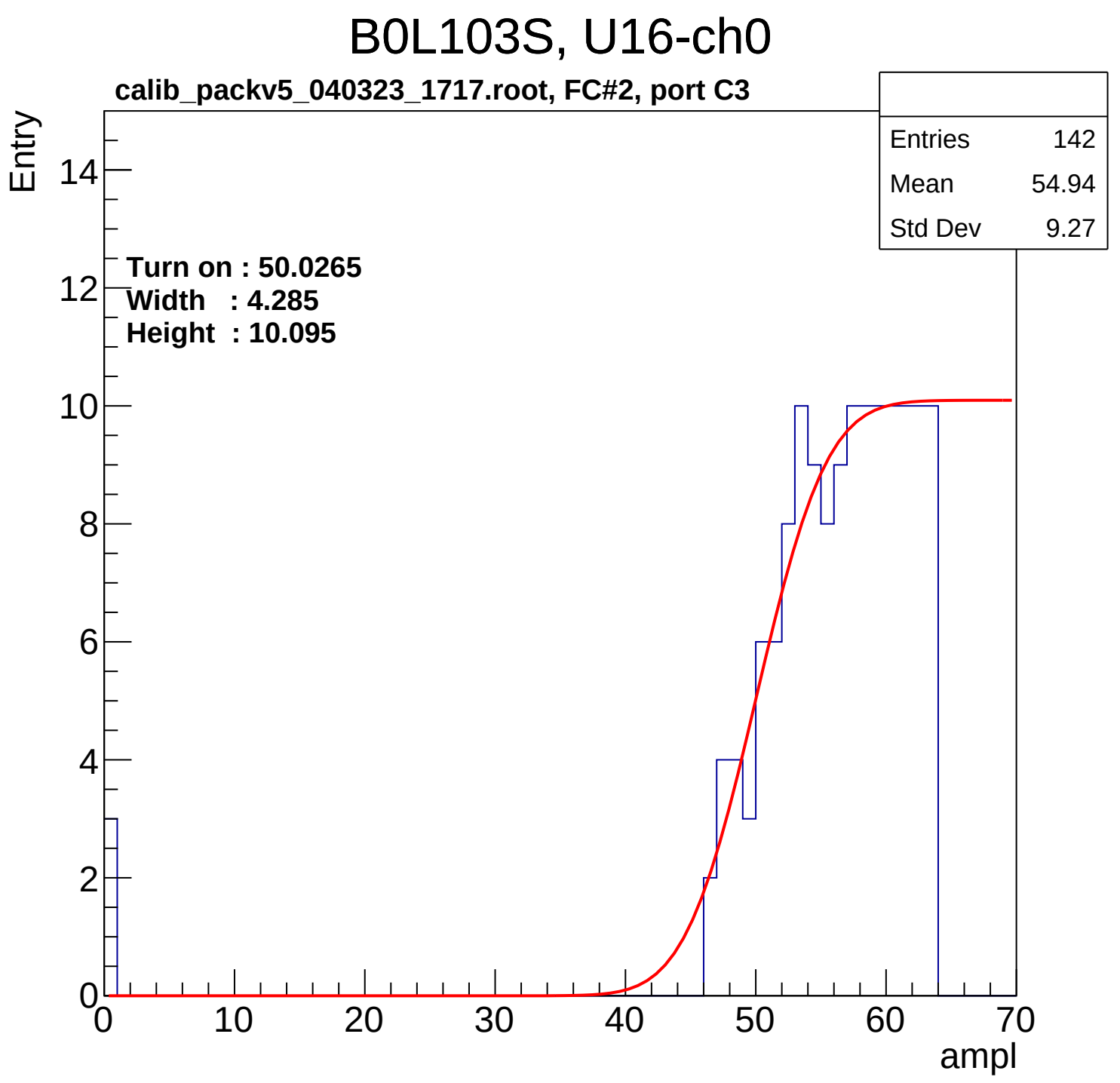
B0L103S, U16-ch0
calib_packv5_040323_1717.root, FC#2, port C3
Entries 142
Mean 54.94
Std Dev 9.27
Turn on : 50.0265
Width : 4.285
Height : 10.095
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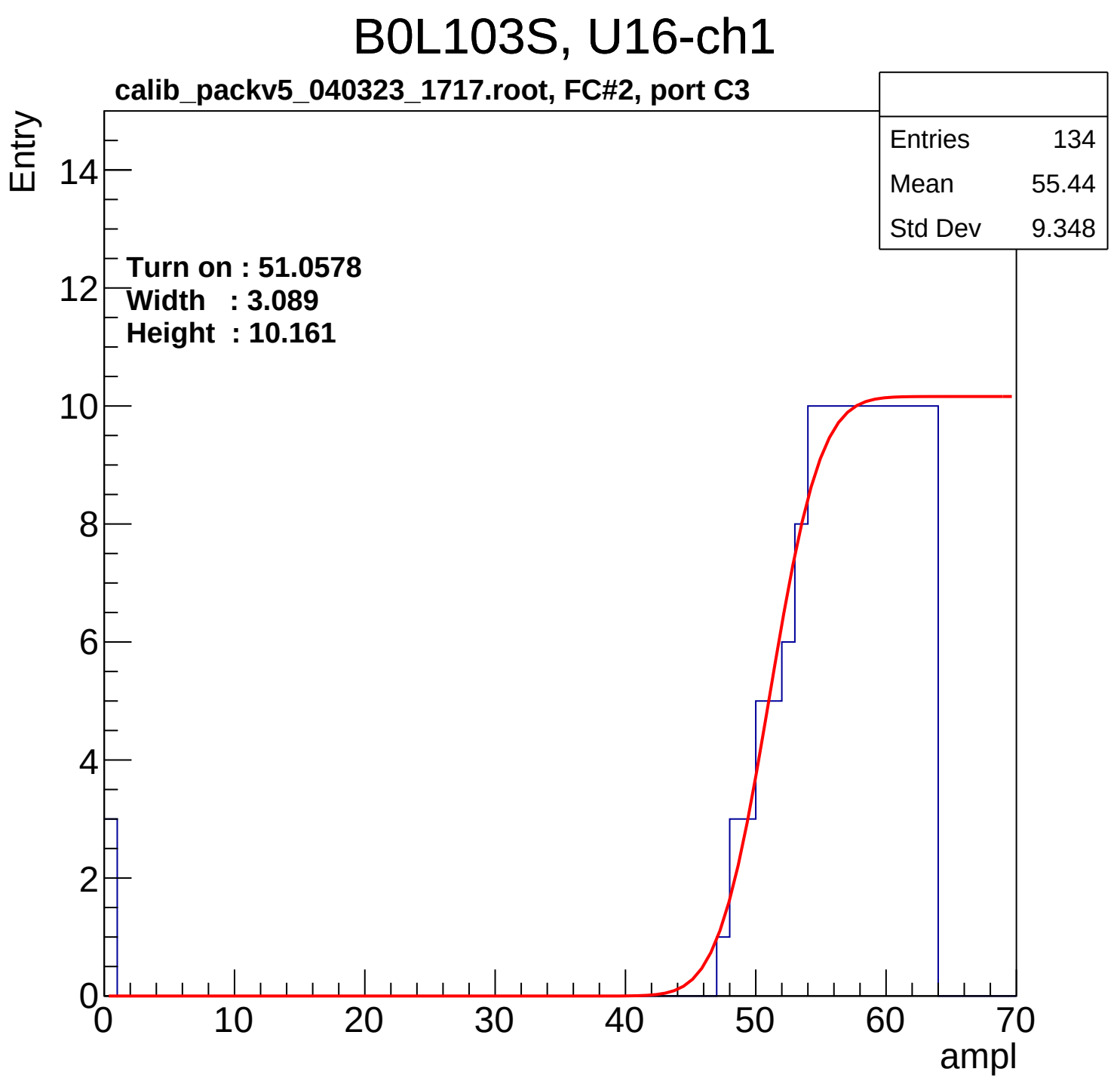
B0L103S, U16-ch1
calib_packv5_040323_1717.root, FC#2, port C3
Entries 134
Mean 55.44
Std Dev 9.348
Turn on : 51.0578
Width : 3.089
Height : 10.161
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ampl
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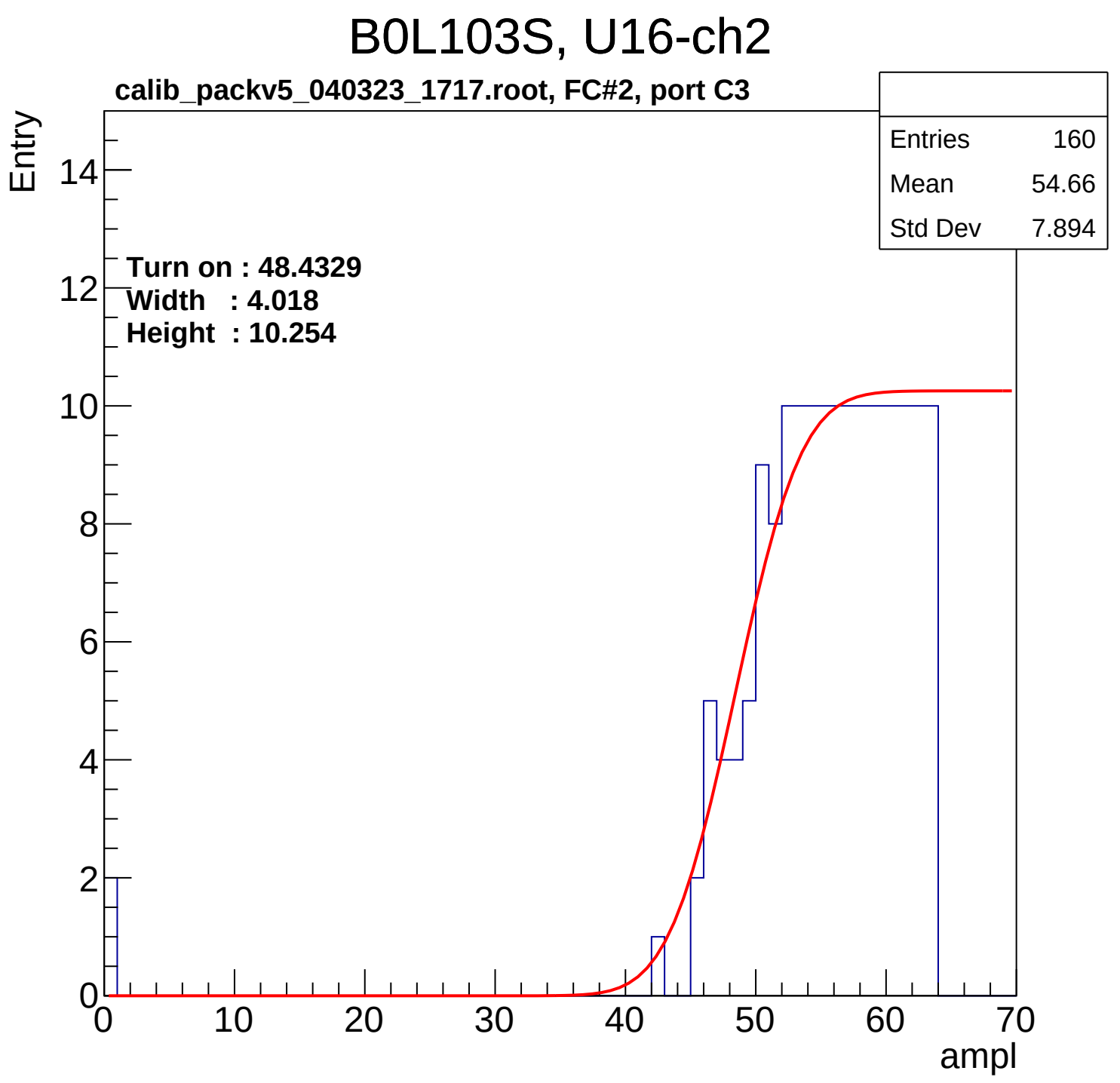
B0L103S, U16-ch2
calib_packv5_040323_1717.root, FC#2, port C3
Entries 160
Mean 54.66
Std Dev 7.894
Turn on : 48.4329
Width : 4.018
Height : 10.254
Entry
ampl
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4
6
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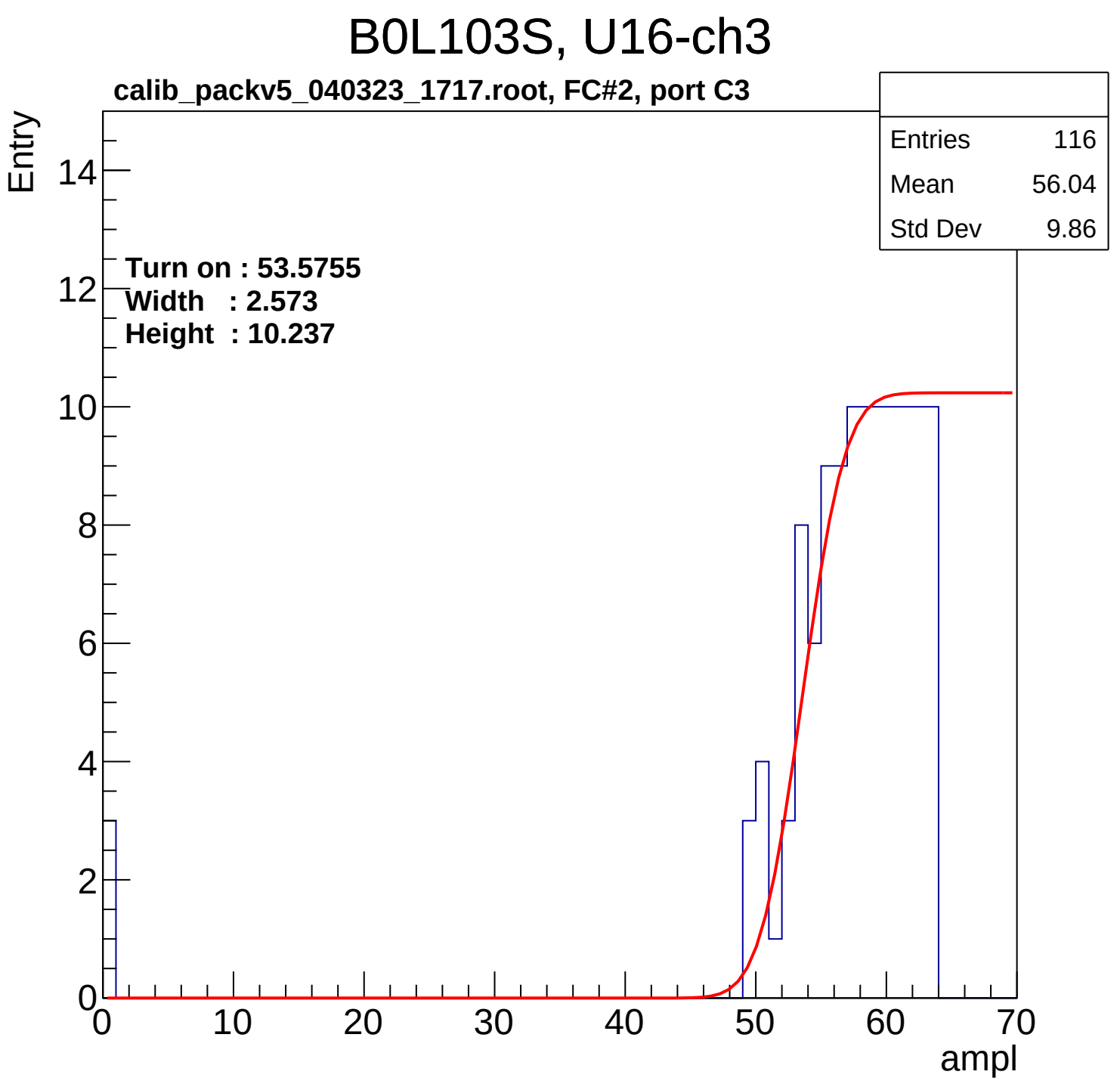
B0L103S, U16-ch3
calib_packv5_040323_1717.root, FC#2, port C3
Entries 116
Mean 56.04
Std Dev 9.86
Turn on : 53.5755
Width : 2.573
Height : 10.237
Entry
ampl
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2
4
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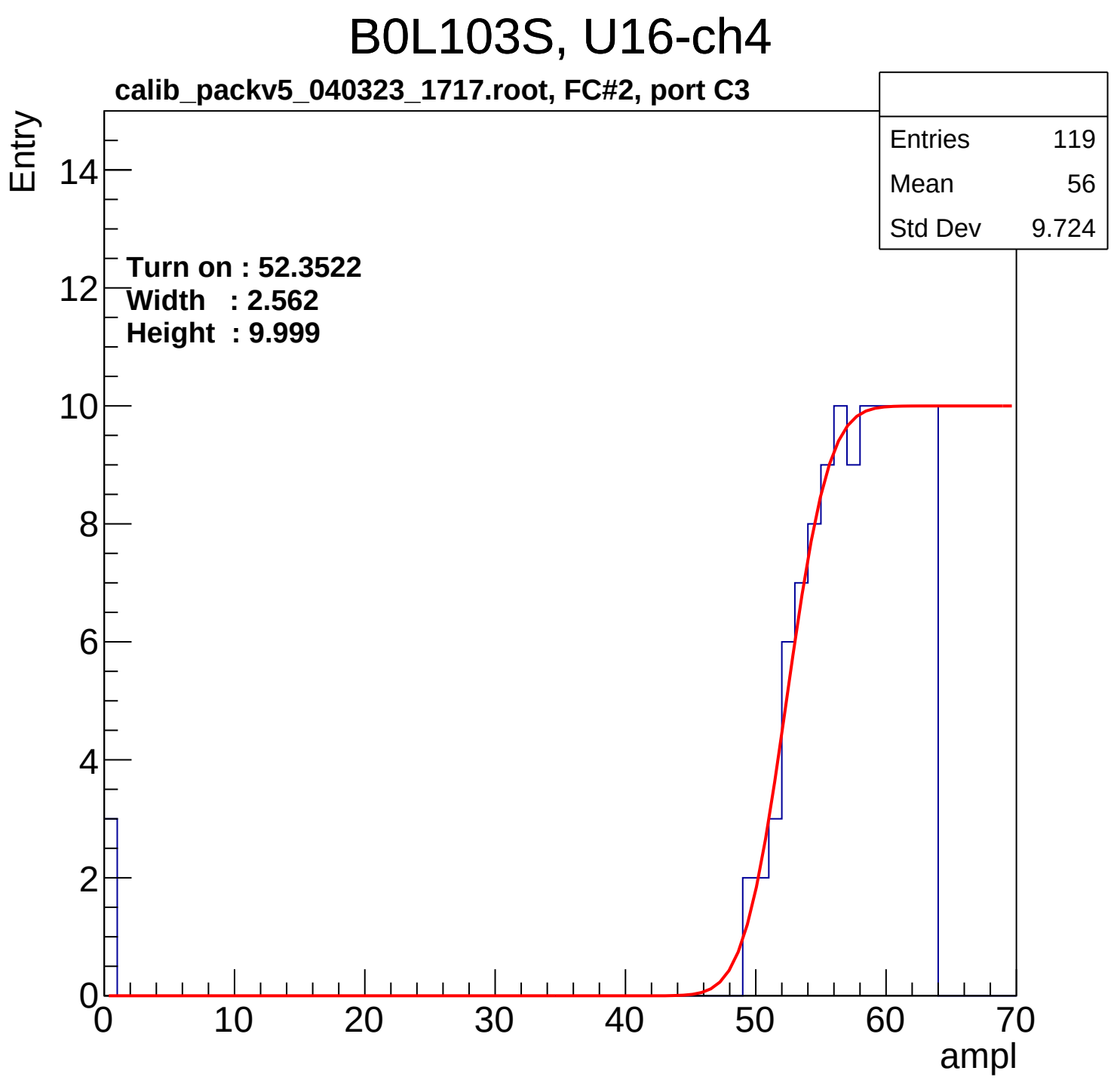
B0L103S, U16-ch4
calib_packv5_040323_1717.root, FC#2, port C3
Entries 119
Mean 56
Std Dev 9.724
Turn on : 52.3522
Width : 2.562
Height : 9.999
Entry
ampl
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2
4
6
8
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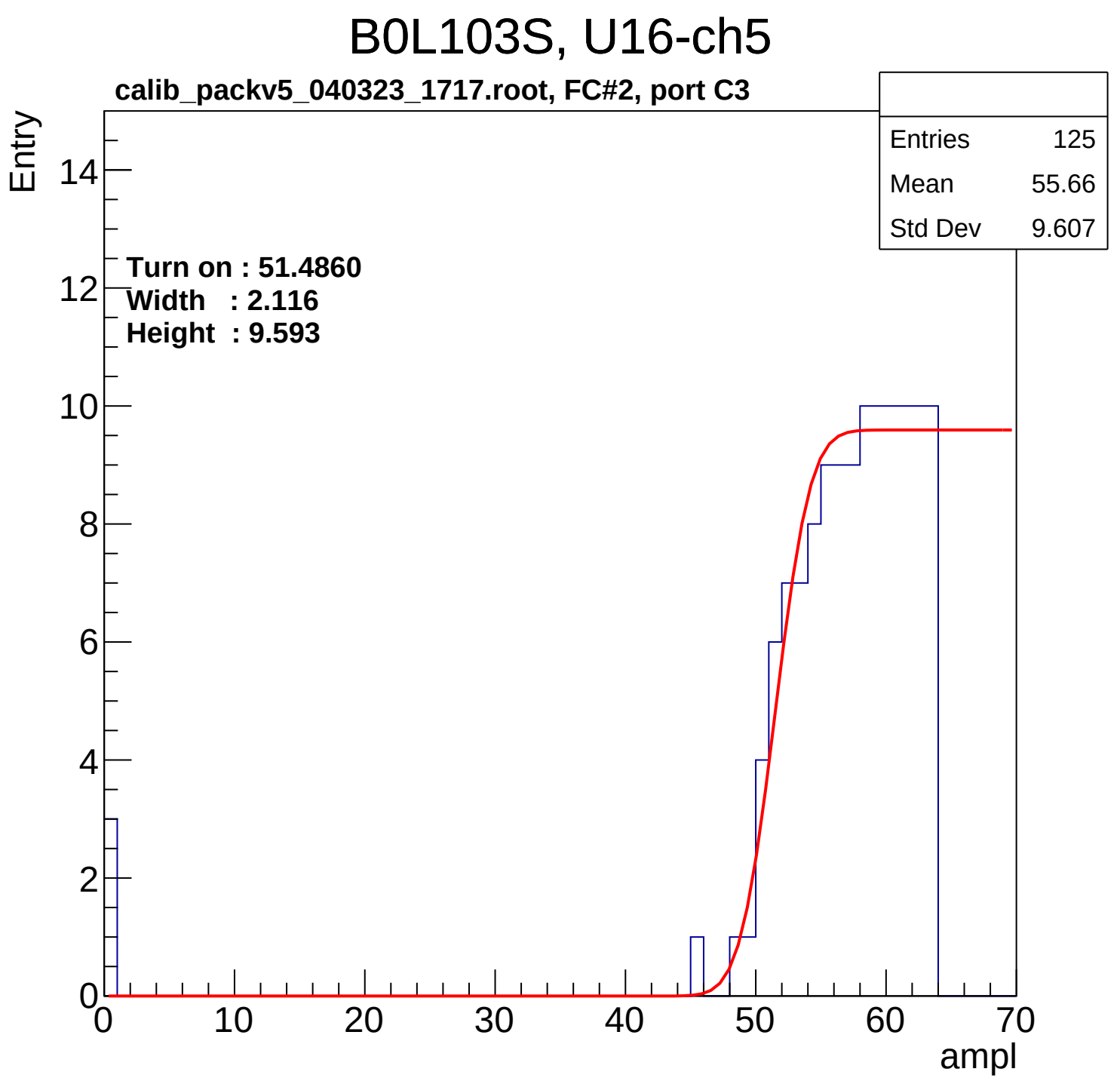
B0L103S, U16-ch5
calib_packv5_040323_1717.root, FC#2, port C3
Entries 125
Mean 55.66
Std Dev 9.607
Turn on : 51.4860
Width : 2.116
Height : 9.593
Entry
ampl
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2
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6
8
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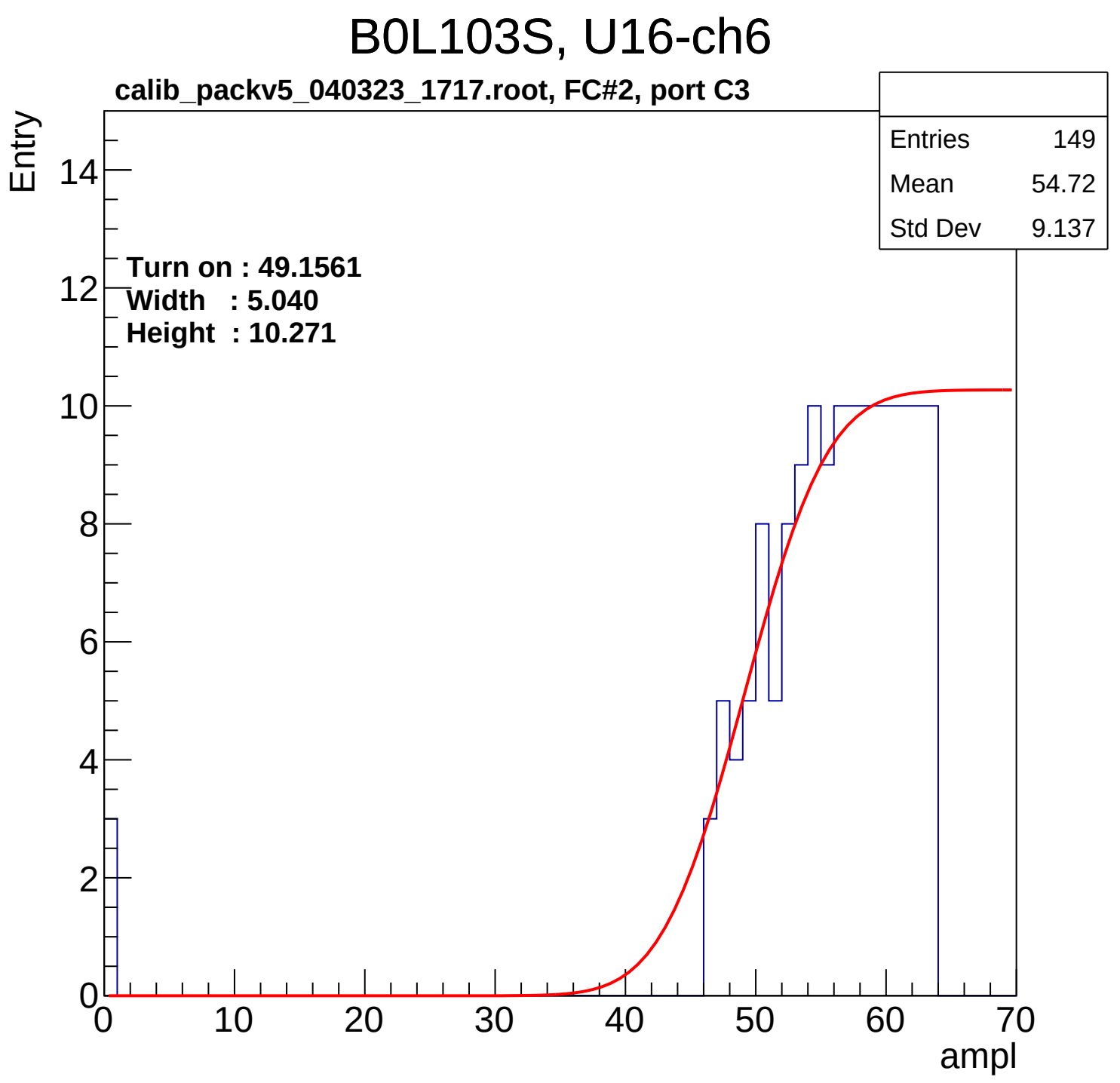
B0L103S, U16-ch6
calib_packv5_040323_1717.root, FC#2, port C3
Entries 149
Mean 54.72
Std Dev 9.137
Turn on : 49.1561
Width : 5.040
Height : 10.271
Entry
ampl
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6
8
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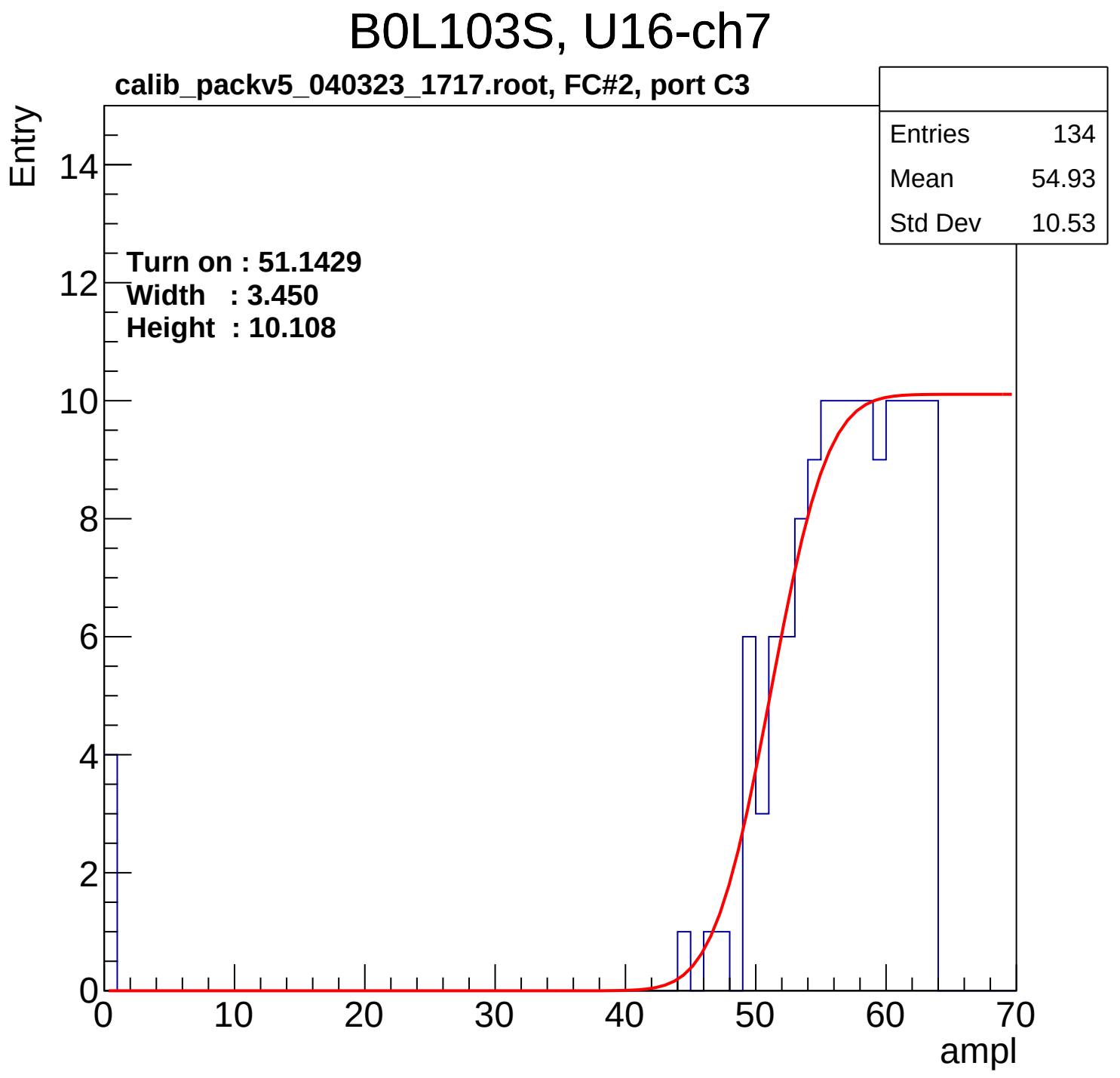
B0L103S, U16-ch7
calib_packv5_040323_1717.root, FC#2, port C3
Entries 134
Mean 54.93
Std Dev 10.53
Turn on : 51.1429
Width : 3.450
Height : 10.108
Entry
ampl
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4
6
8
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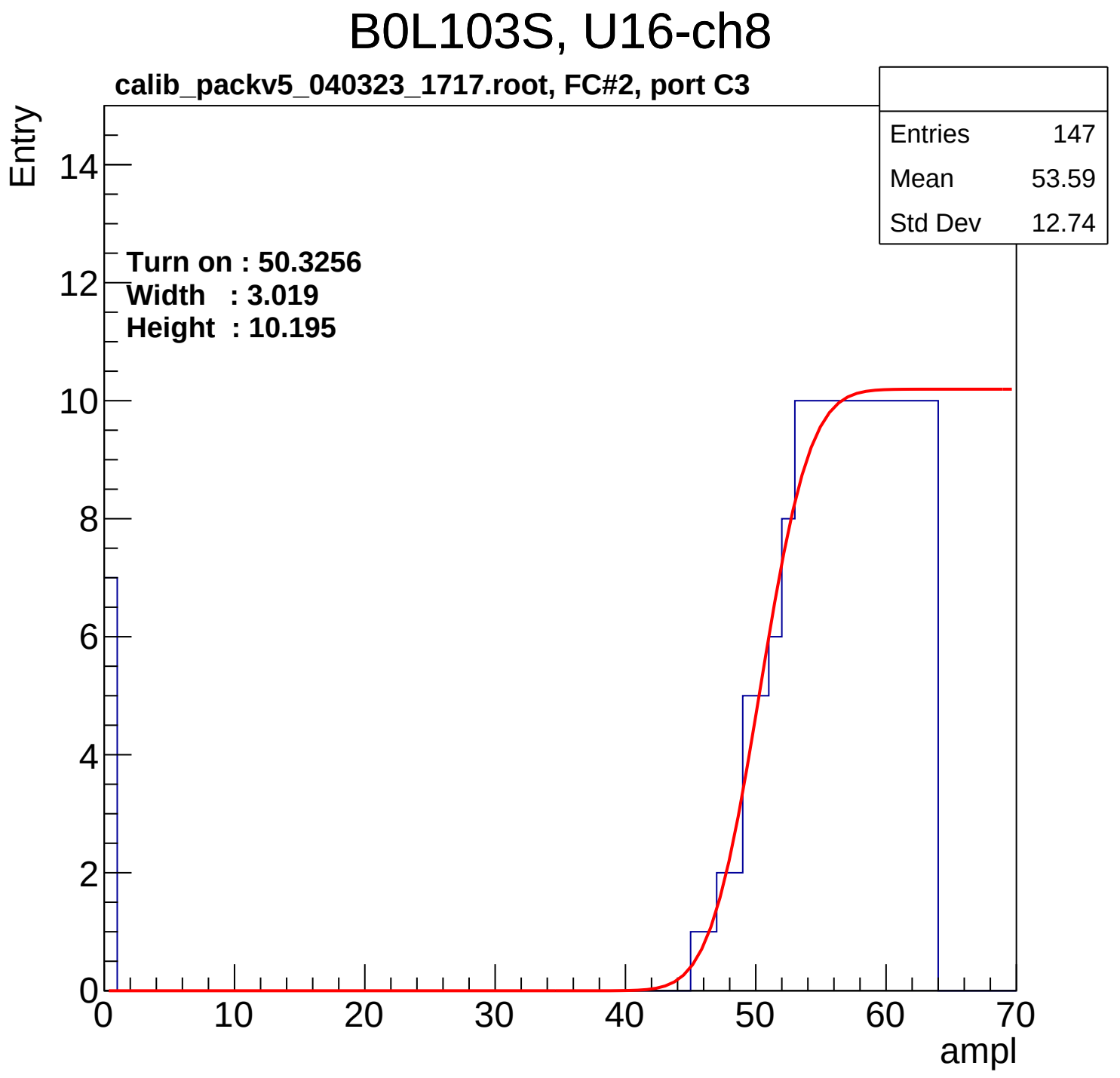
B0L103S, U16-ch8
calib_packv5_040323_1717.root, FC#2, port C3
Entries 147
Mean 53.59
Std Dev 12.74
Turn on : 50.3256
Width : 3.019
Height : 10.195
Entry
ampl
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6
8
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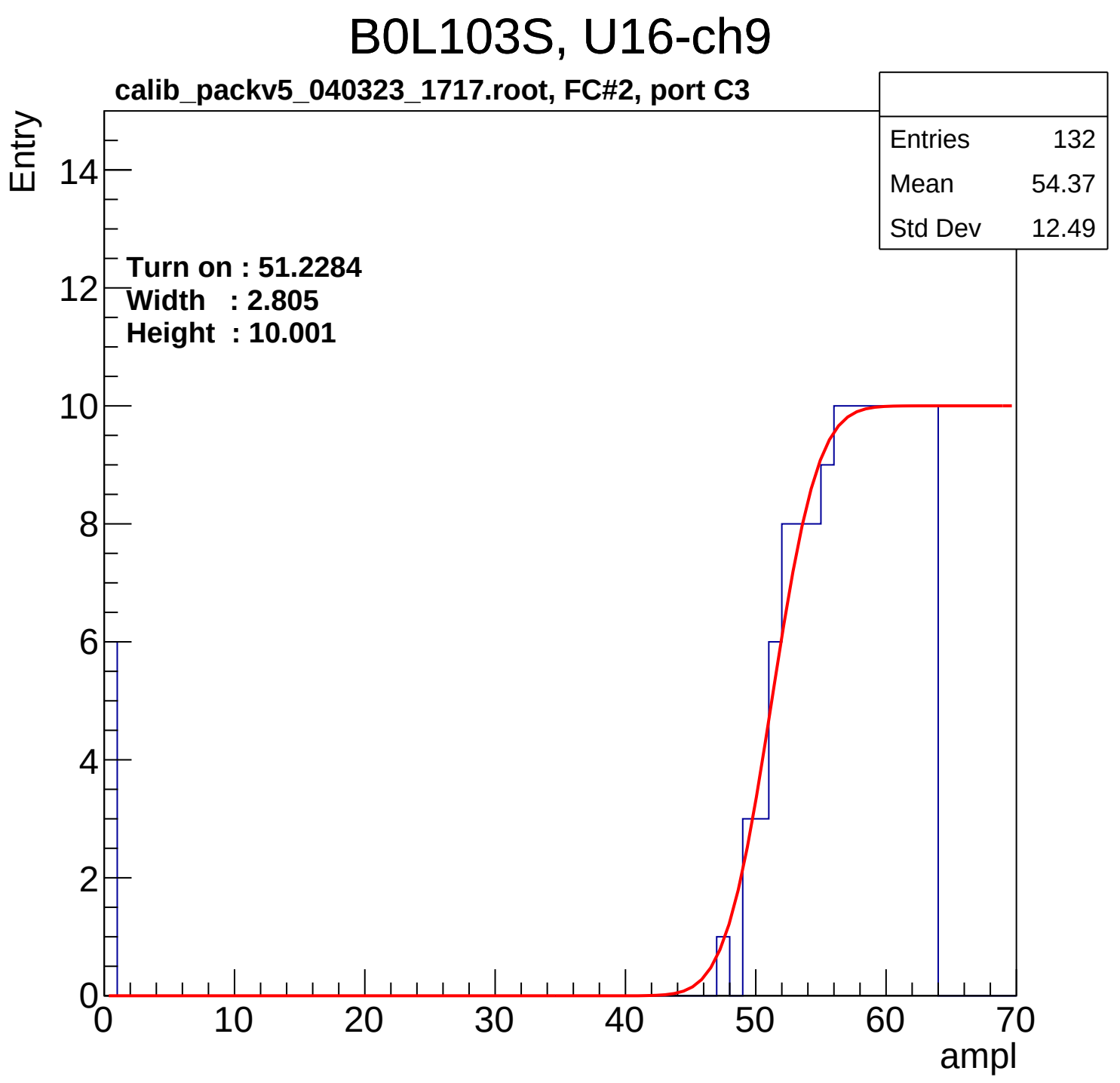
B0L103S, U16-ch9
calib_packv5_040323_1717.root, FC#2, port C3
Entries 132
Mean 54.37
Std Dev 12.49
Turn on : 51.2284
Width : 2.805
Height : 10.001
Entry
ampl
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2
4
6
8
10
12
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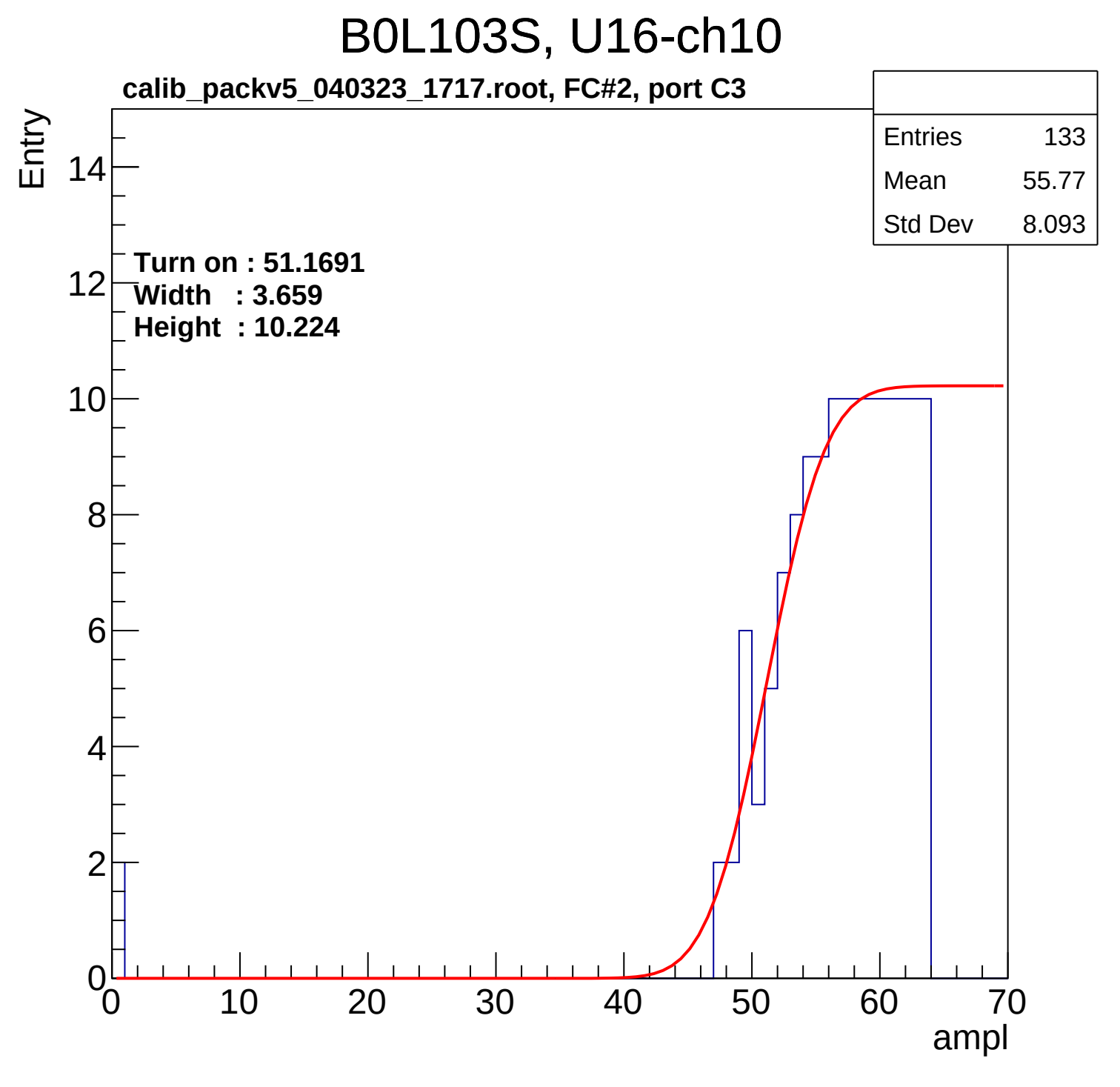
B0L103S, U16-ch10
calib_packv5_040323_1717.root, FC#2, port C3
Entries 133
Mean 55.77
Std Dev 8.093
Turn on : 51.1691
Width : 3.659
Height : 10.224
Entry
ampl
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4
6
8
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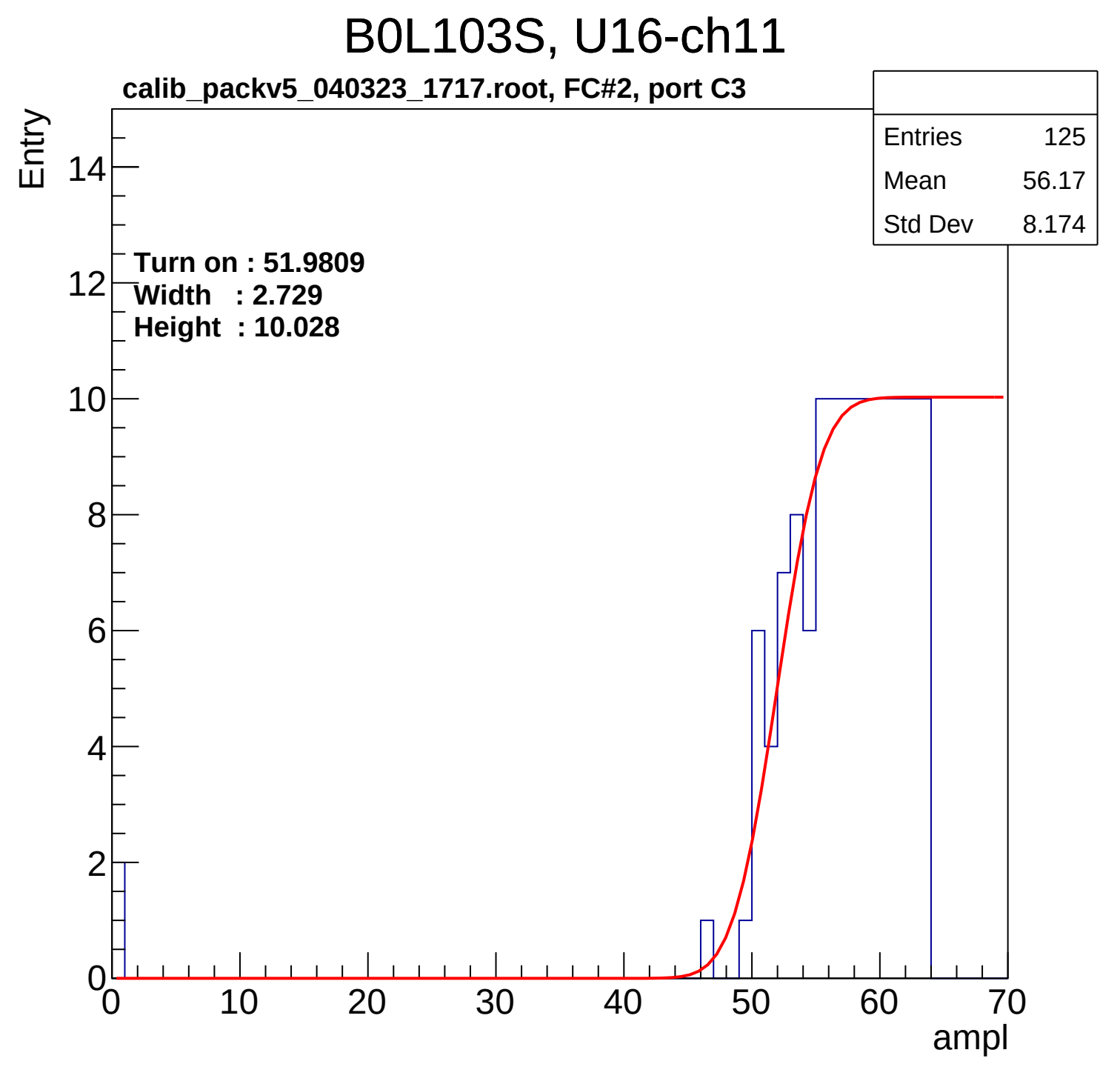
B0L103S, U16-ch11
calib_packv5_040323_1717.root, FC#2, port C3
Entries 125
Mean 56.17
Std Dev 8.174
Turn on : 51.9809
Width : 2.729
Height : 10.028
Entry
ampl
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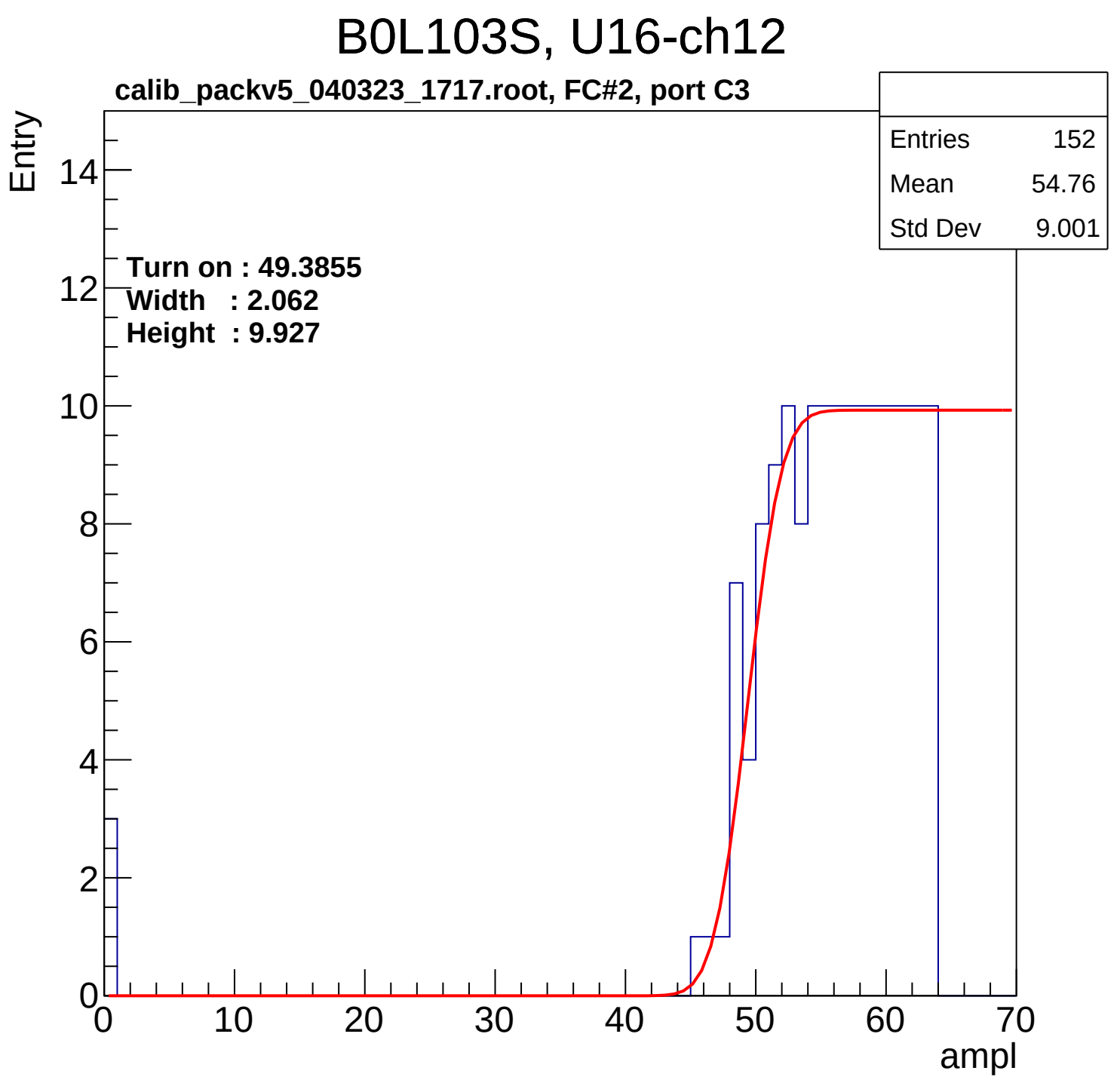
B0L103S, U16-ch12
calib_packv5_040323_1717.root, FC#2, port C3
Entries 152
Mean 54.76
Std Dev 9.001
Turn on : 49.3855
Width : 2.062
Height : 9.927
Entry
ampl
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6
8
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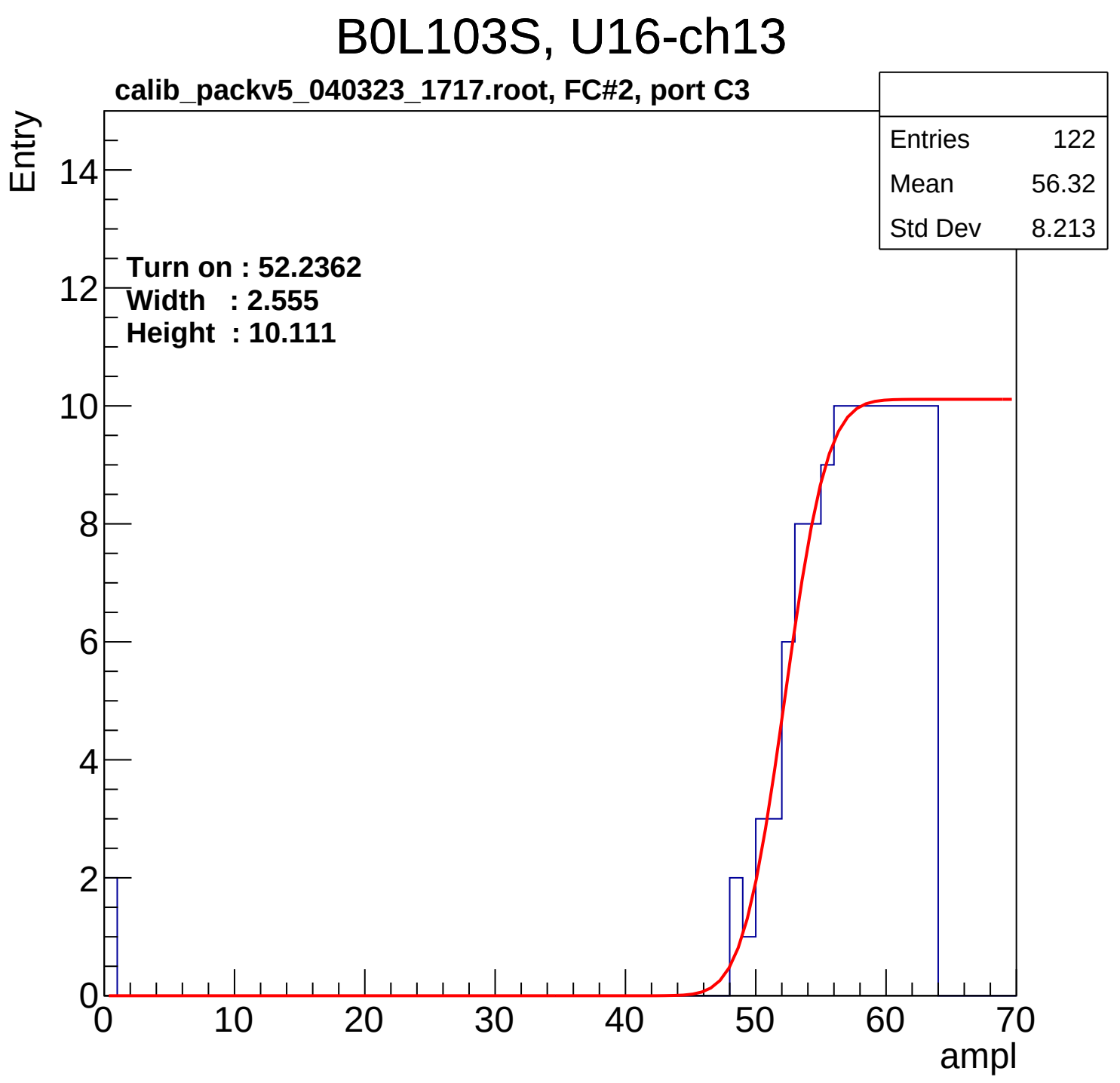
B0L103S, U16-ch13
calib_packv5_040323_1717.root, FC#2, port C3
Entries 122
Mean 56.32
Std Dev 8.213
Turn on : 52.2362
Width : 2.555
Height : 10.111
Entry
ampl
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6
8
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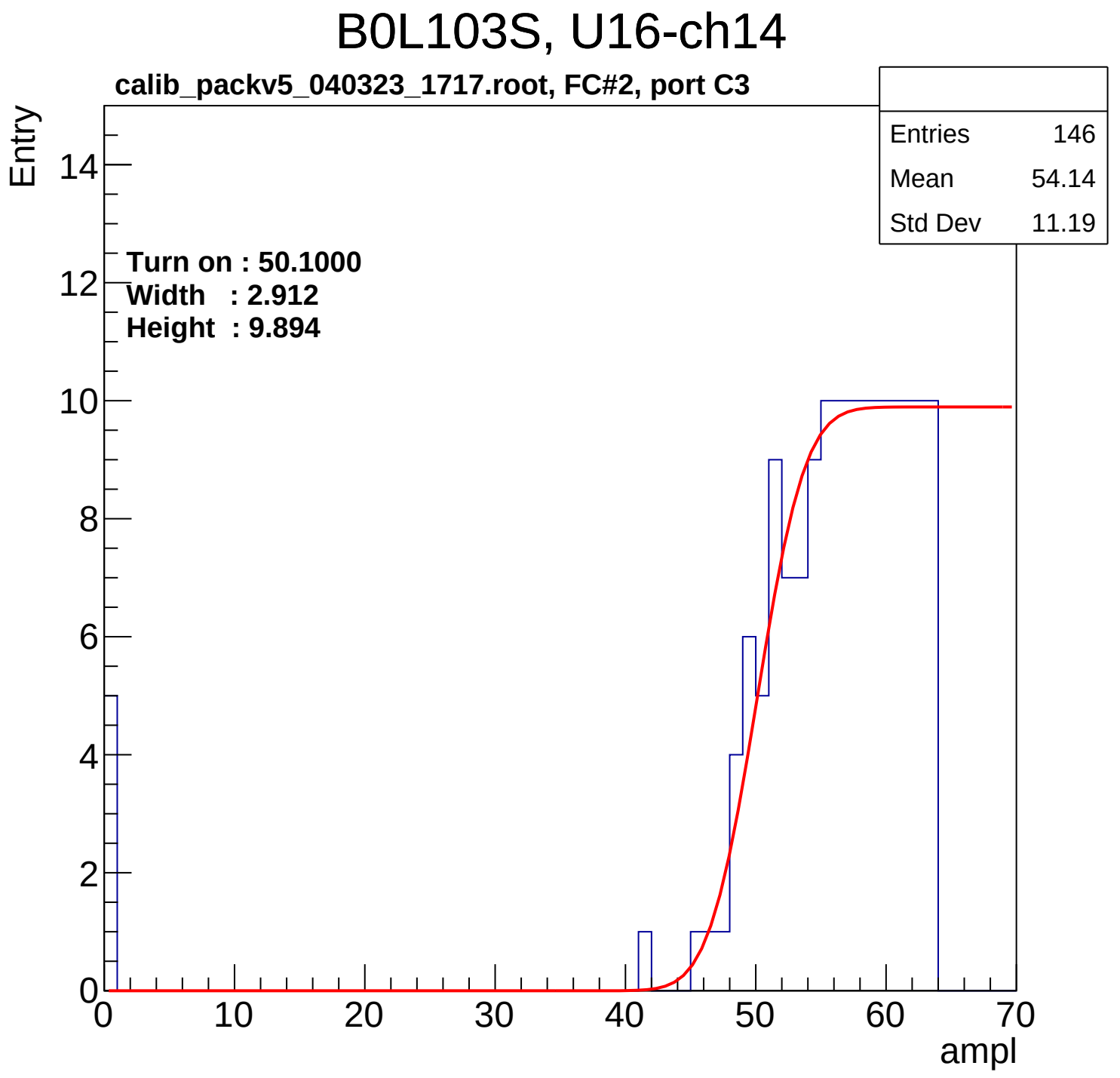
B0L103S, U16-ch14
calib_packv5_040323_1717.root, FC#2, port C3
Entries 146
Mean 54.14
Std Dev 11.19
Turn on : 50.1000
Width : 2.912
Height : 9.894
Entry
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6
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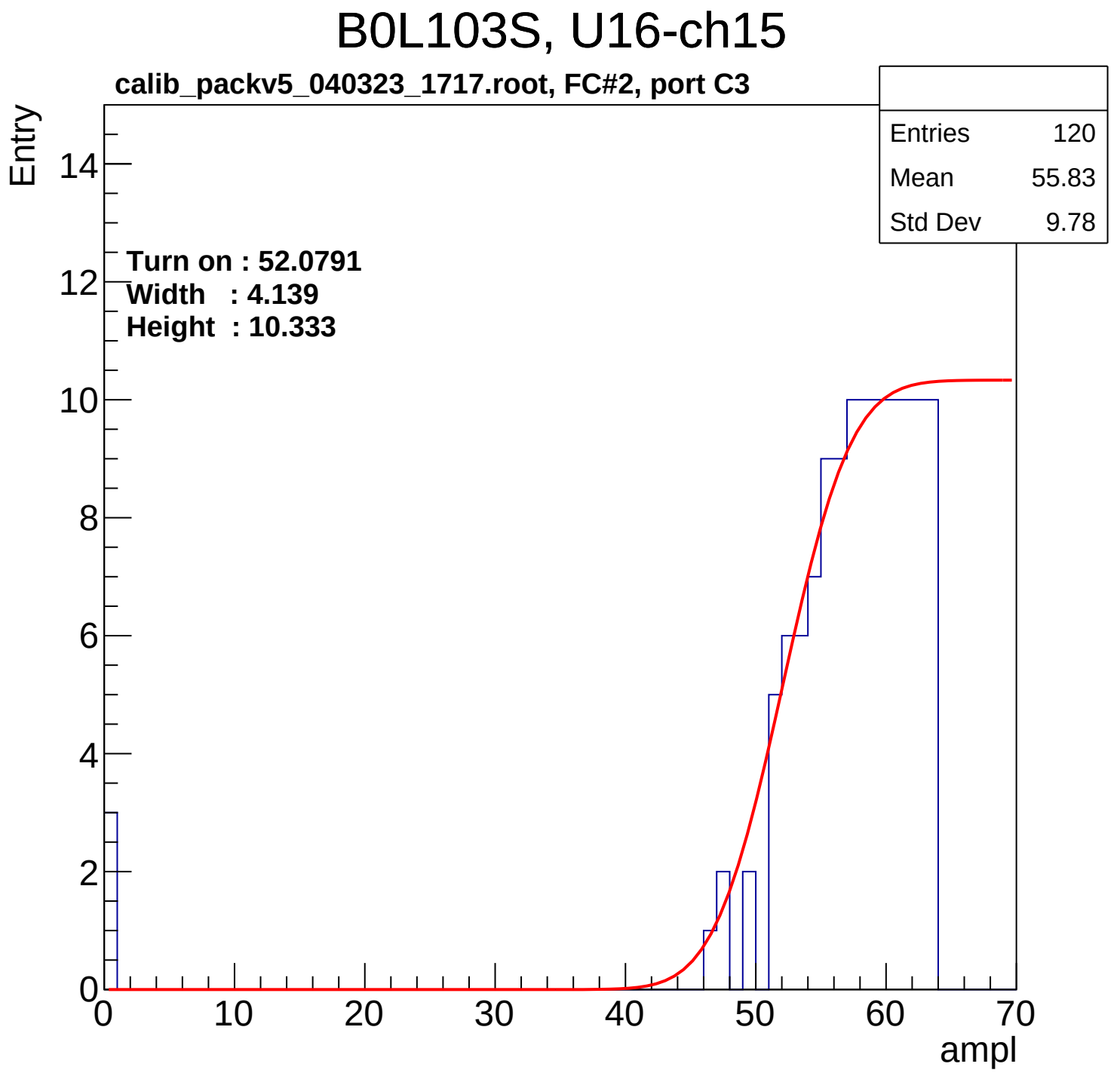
B0L103S, U16-ch15
calib_packv5_040323_1717.root, FC#2, port C3
Entries 120
Mean 55.83
Std Dev 9.78
Turn on : 52.0791
Width : 4.139
Height : 10.333
Entry
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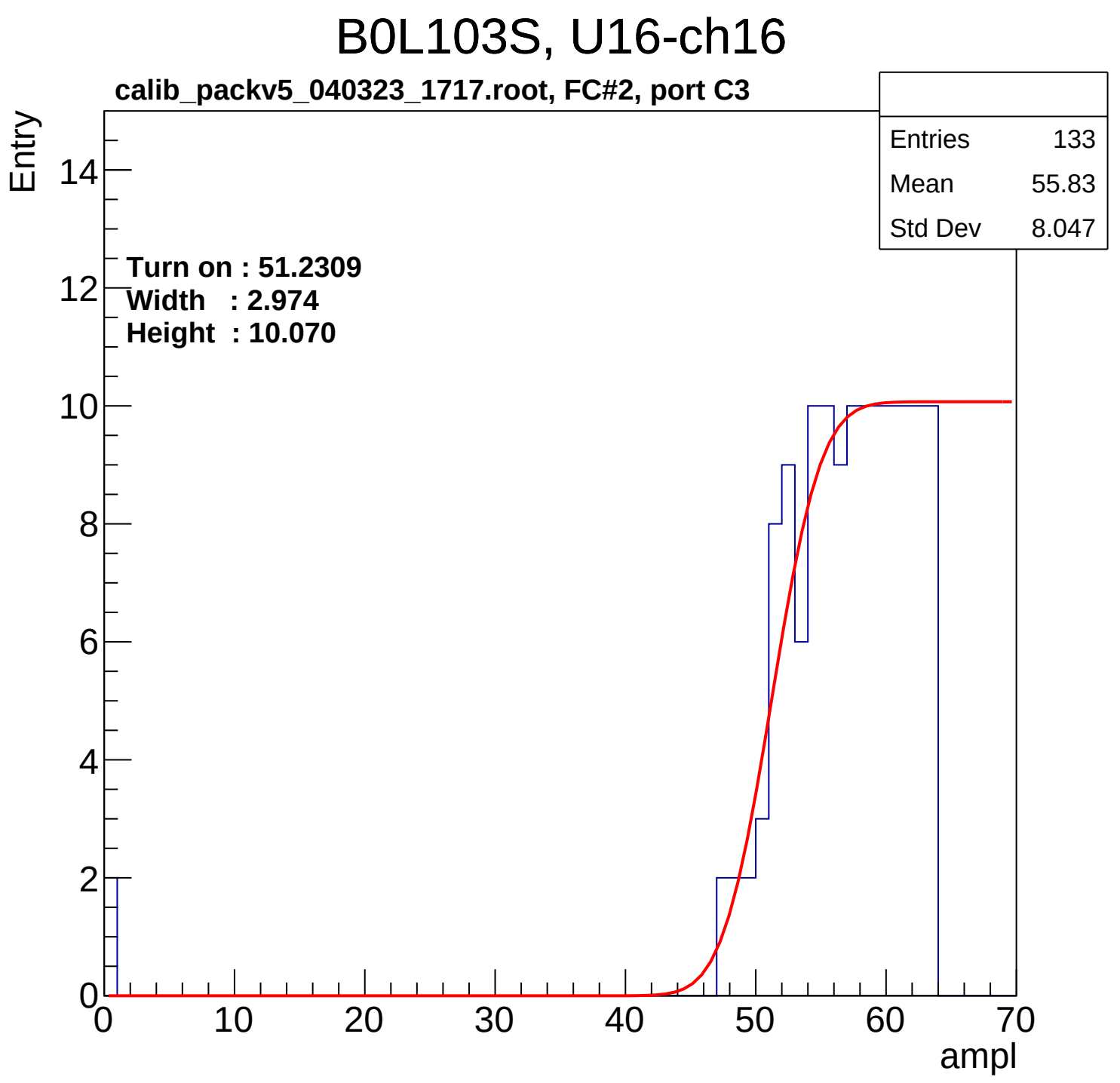
B0L103S, U16-ch16
calib_packv5_040323_1717.root, FC#2, port C3
Entries 133
Mean 55.83
Std Dev 8.047
Turn on : 51.2309
Width : 2.974
Height : 10.070
Entry
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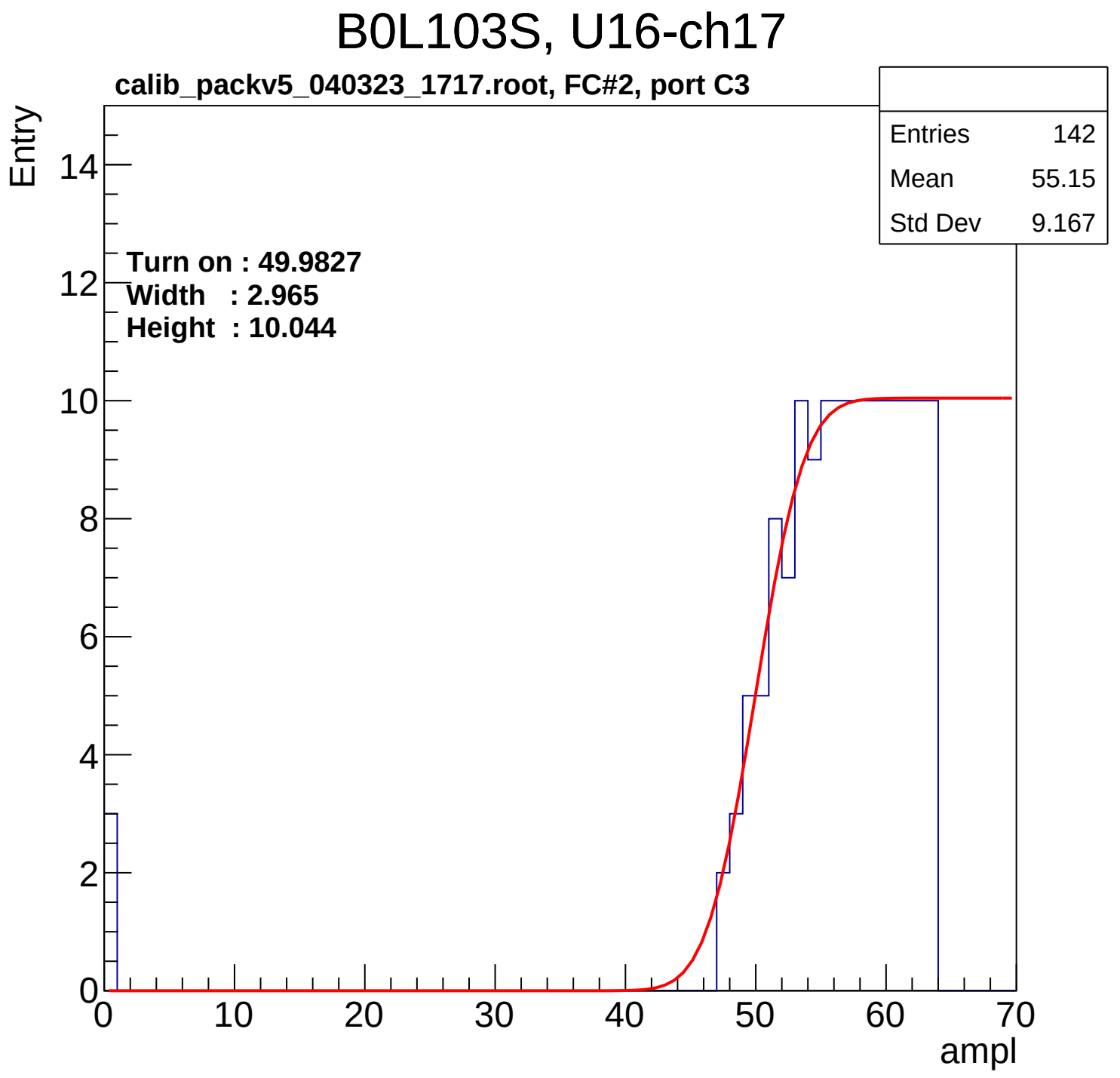
B0L103S, U16-ch17
calib_packv5_040323_1717.root, FC#2, port C3
Entries 142
Mean 55.15
Std Dev 9.167
Turn on : 49.9827
Width : 2.965
Height : 10.044
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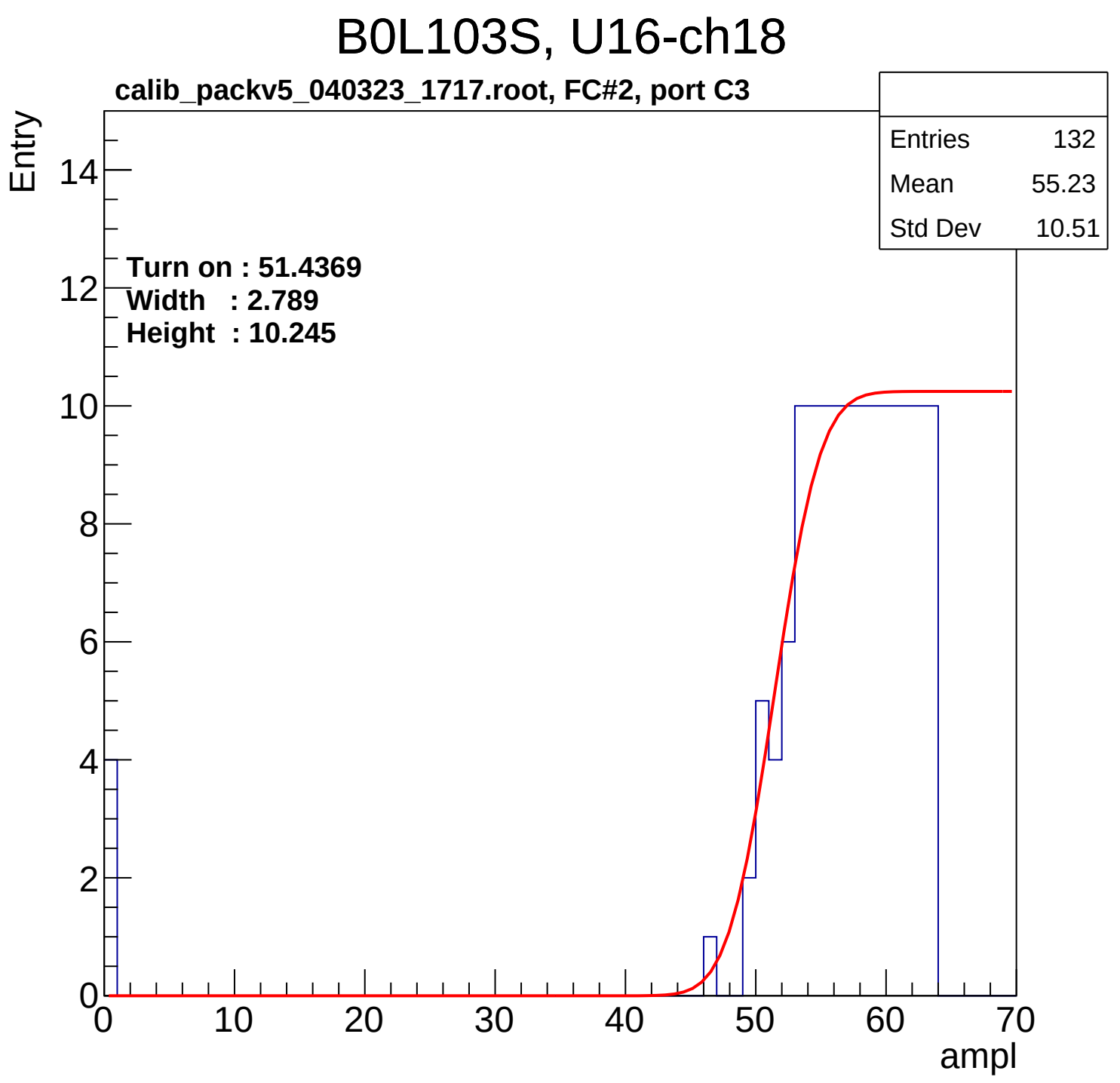
B0L103S, U16-ch18
calib_packv5_040323_1717.root, FC#2, port C3
Entries 132
Mean 55.23
Std Dev 10.51
Turn on : 51.4369
Width : 2.789
Height : 10.245
Entry
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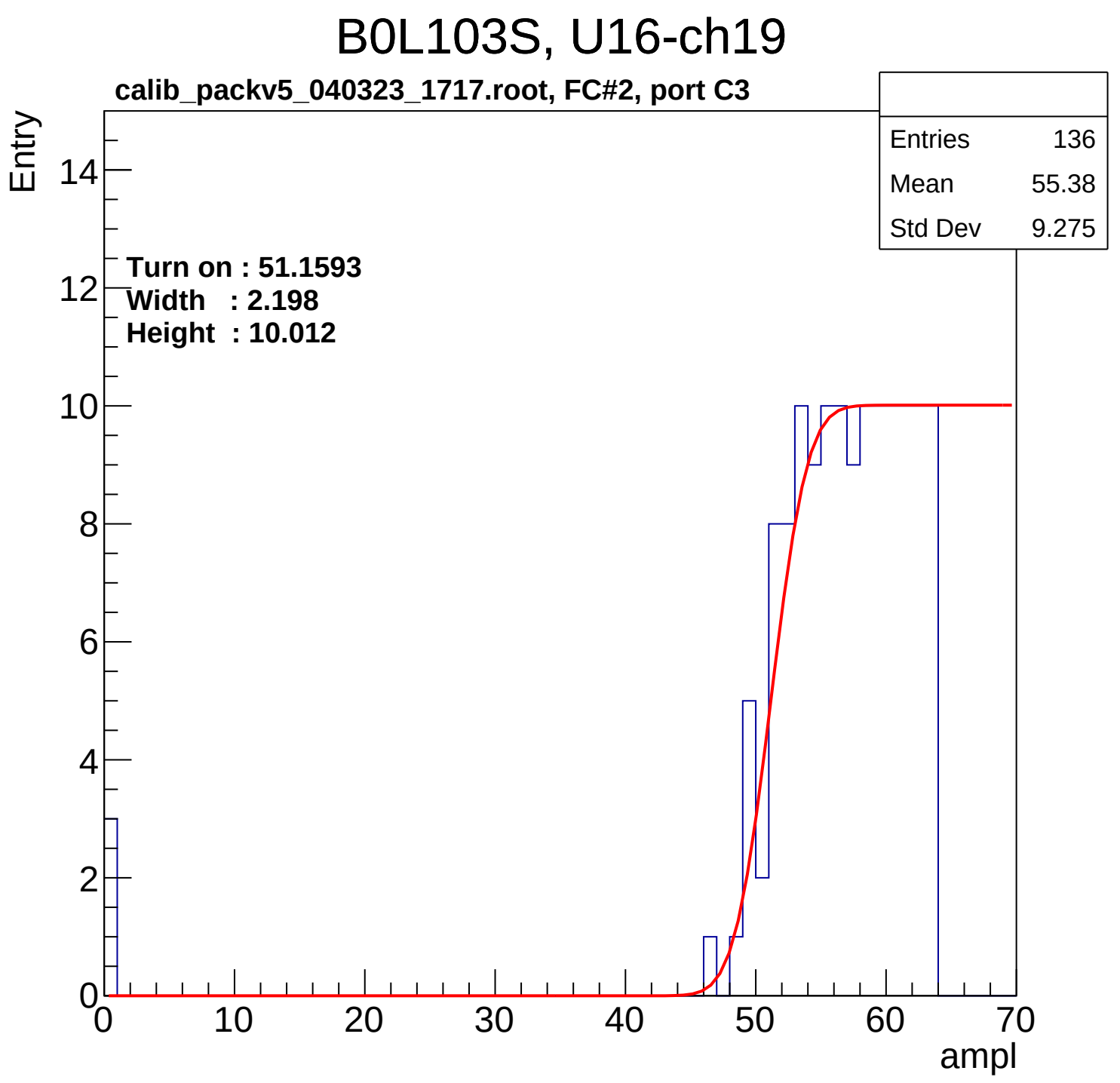
B0L103S, U16-ch19
calib_packv5_040323_1717.root, FC#2, port C3
Entries 136
Mean 55.38
Std Dev 9.275
Turn on : 51.1593
Width : 2.198
Height : 10.012
Entry
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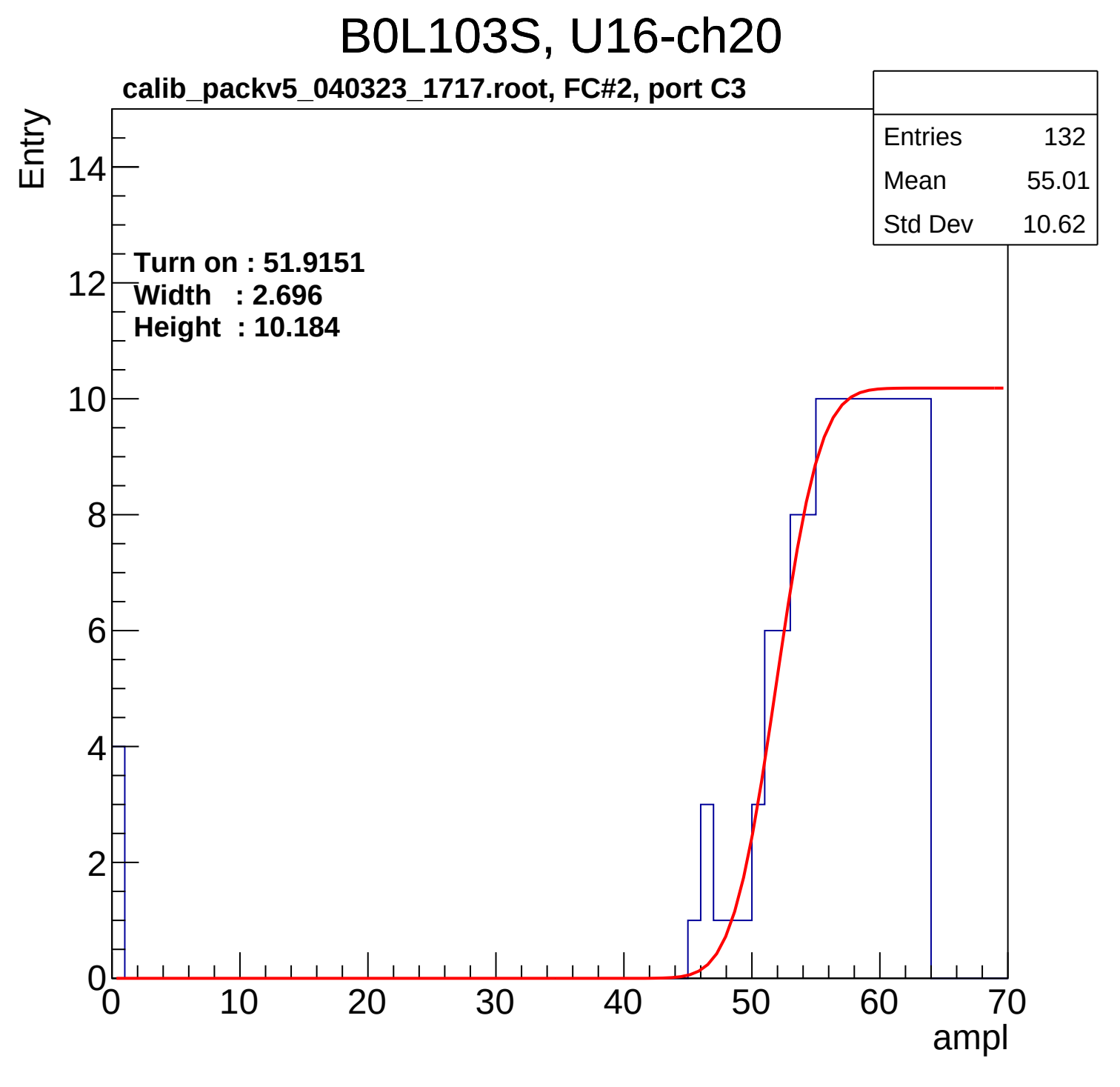
B0L103S, U16-ch20
calib_packv5_040323_1717.root, FC#2, port C3
Entries 132
Mean 55.01
Std Dev 10.62
Turn on : 51.9151
Width : 2.696
Height : 10.184
Entry
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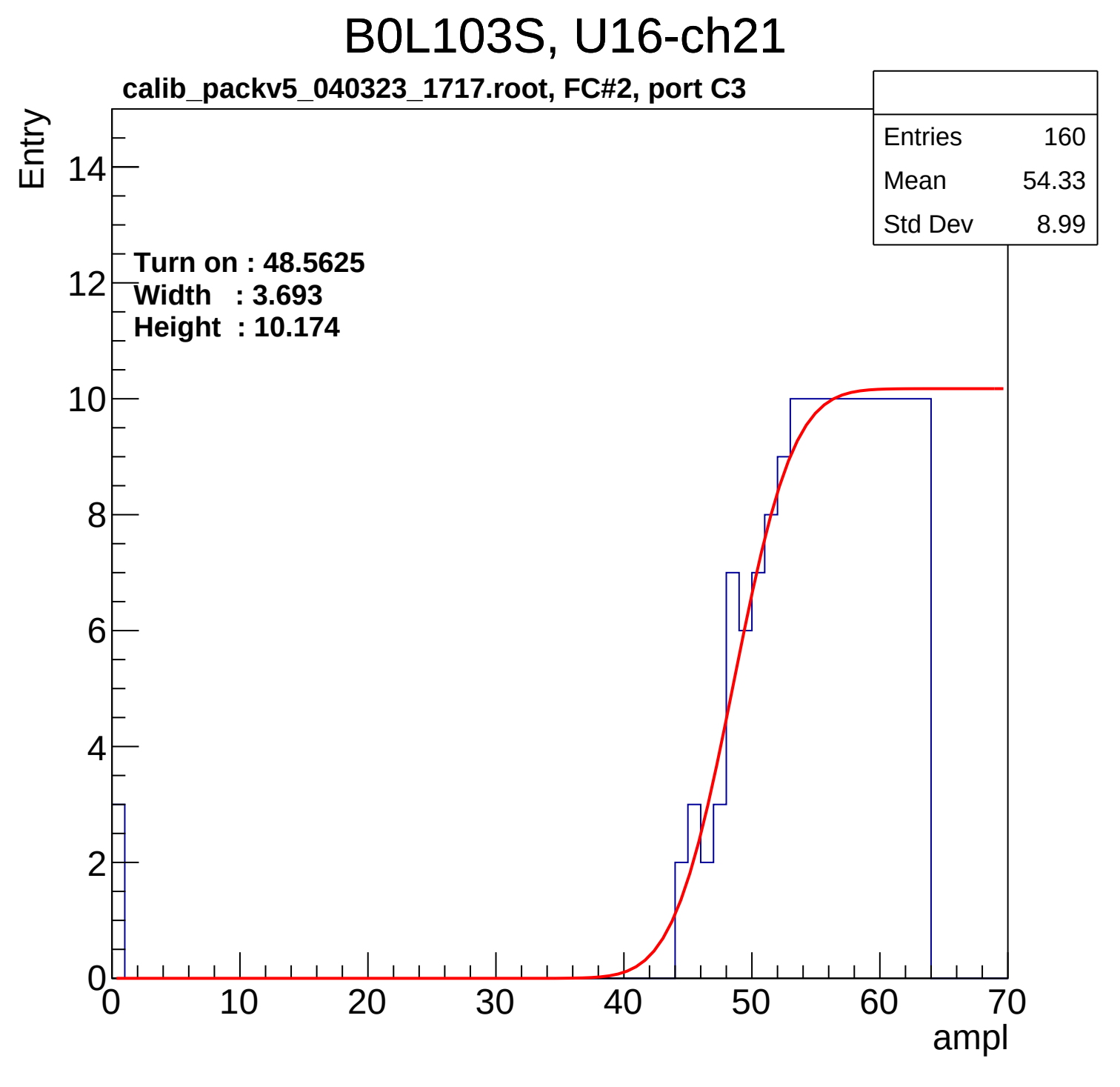
B0L103S, U16-ch21
calib_packv5_040323_1717.root, FC#2, port C3
Entries 160
Mean 54.33
Std Dev 8.99
Turn on : 48.5625
Width : 3.693
Height : 10.174
Entry
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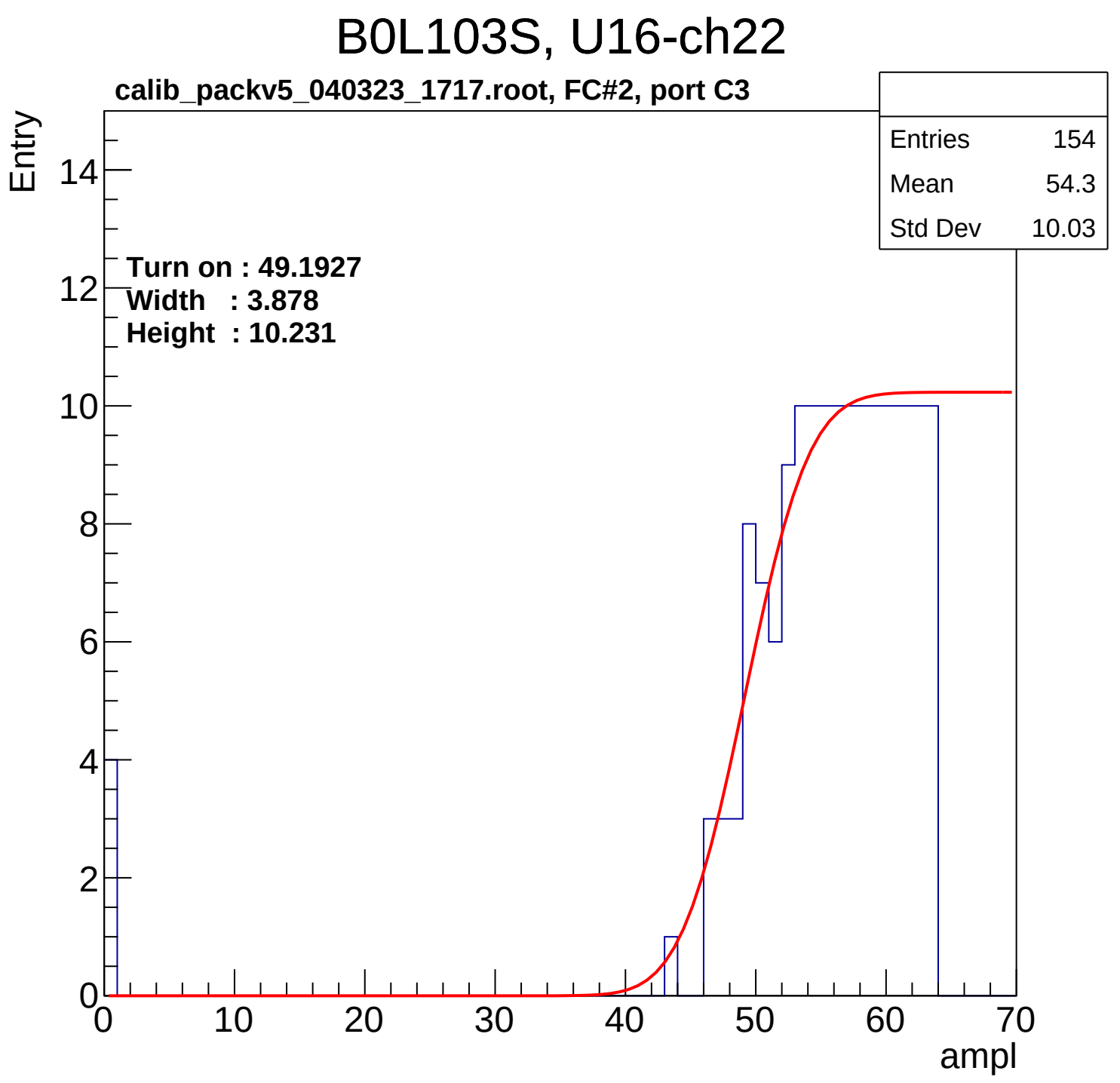
B0L103S, U16-ch22
calib_packv5_040323_1717.root, FC#2, port C3
Entries 154
Mean 54.3
Std Dev 10.03
Turn on : 49.1927
Width : 3.878
Height : 10.231
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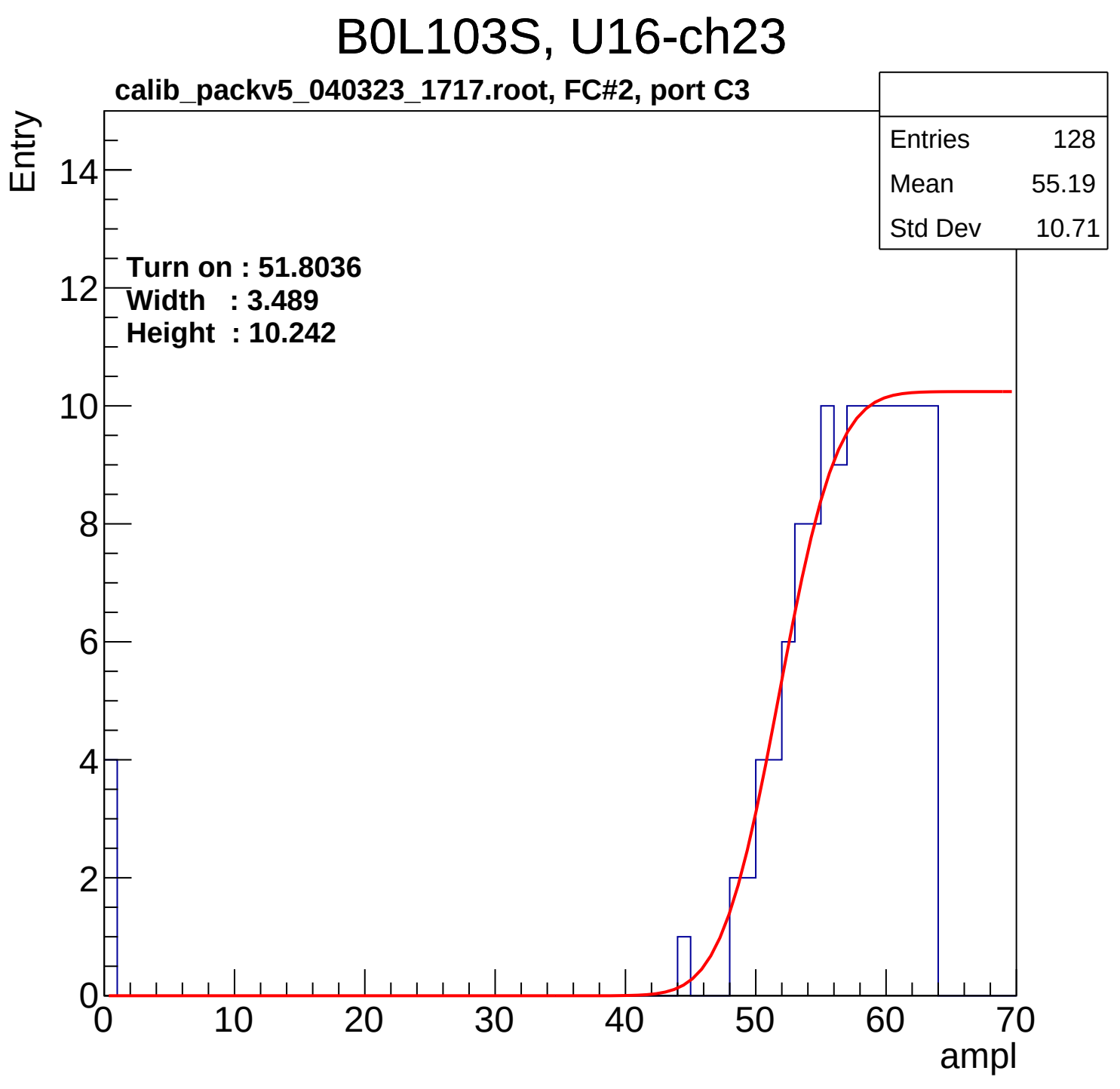
B0L103S, U16-ch23
calib_packv5_040323_1717.root, FC#2, port C3
Entries 128
Mean 55.19
Std Dev 10.71
Turn on : 51.8036
Width : 3.489
Height : 10.242
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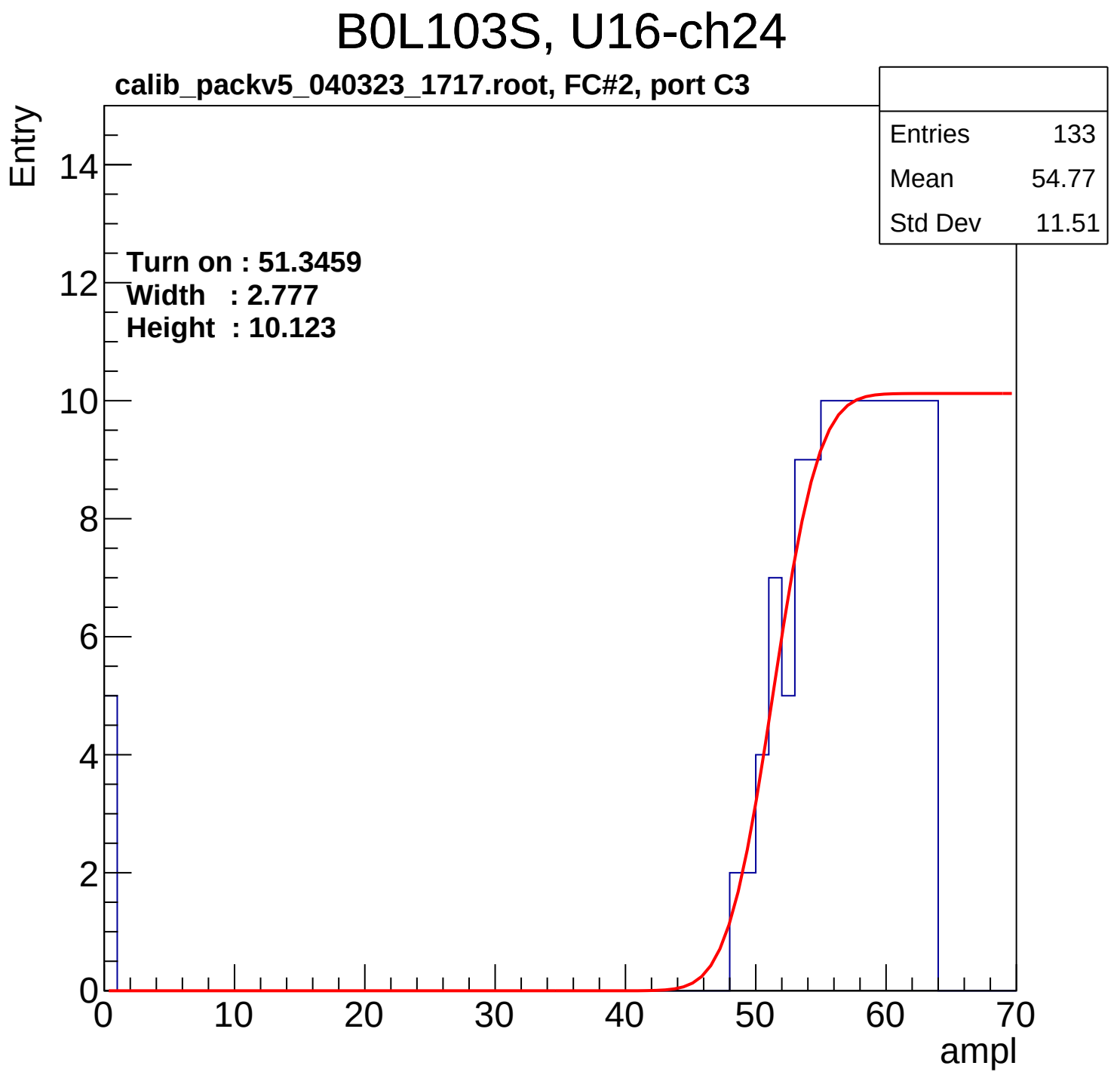
B0L103S, U16-ch24
calib_packv5_040323_1717.root, FC#2, port C3
Entries 133
Mean 54.77
Std Dev 11.51
Turn on : 51.3459
Width : 2.777
Height : 10.123
Entry
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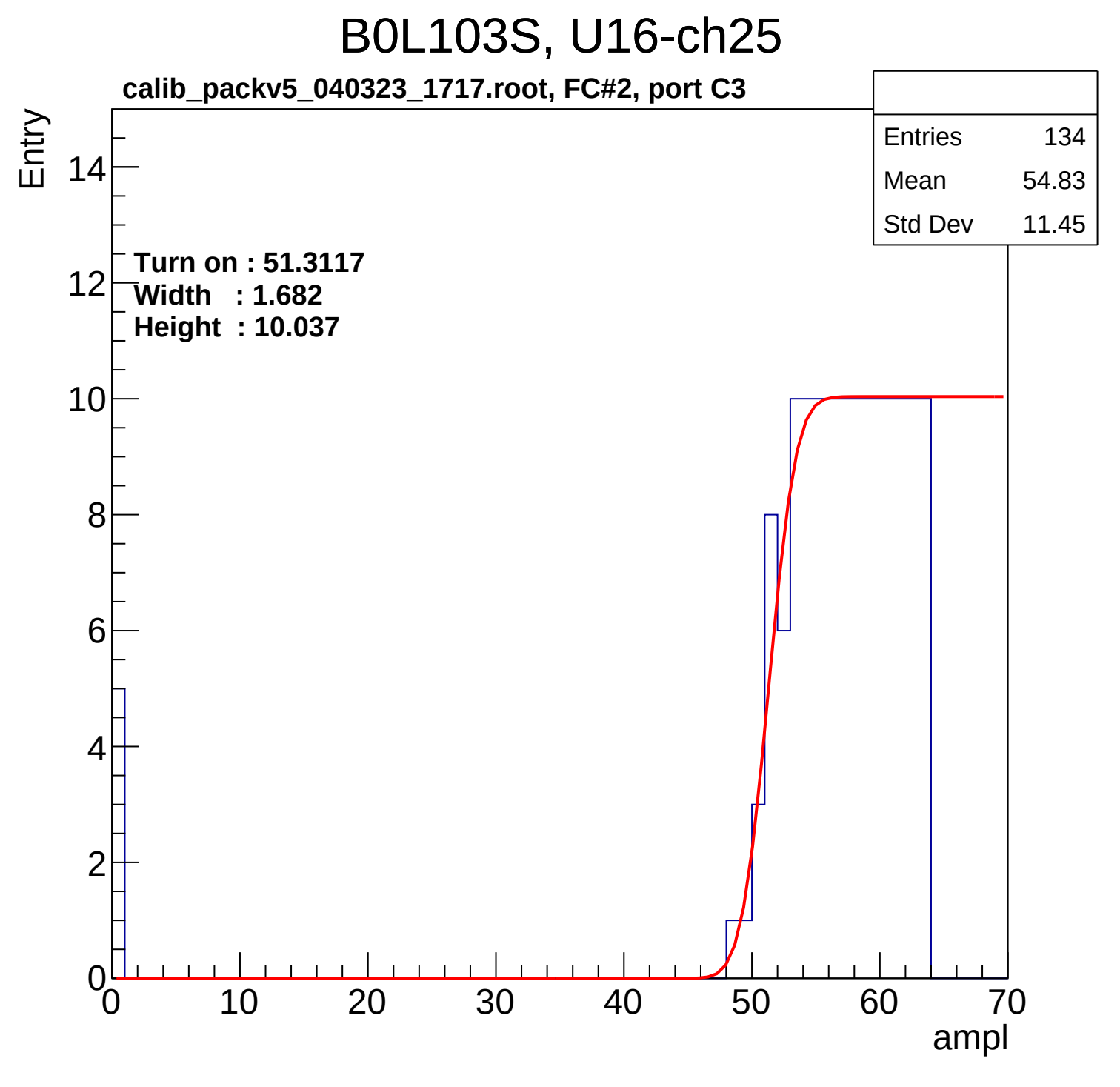
B0L103S, U16-ch25
calib_packv5_040323_1717.root, FC#2, port C3
Entries 134
Mean 54.83
Std Dev 11.45
Turn on : 51.3117
Width : 1.682
Height : 10.037
Entry
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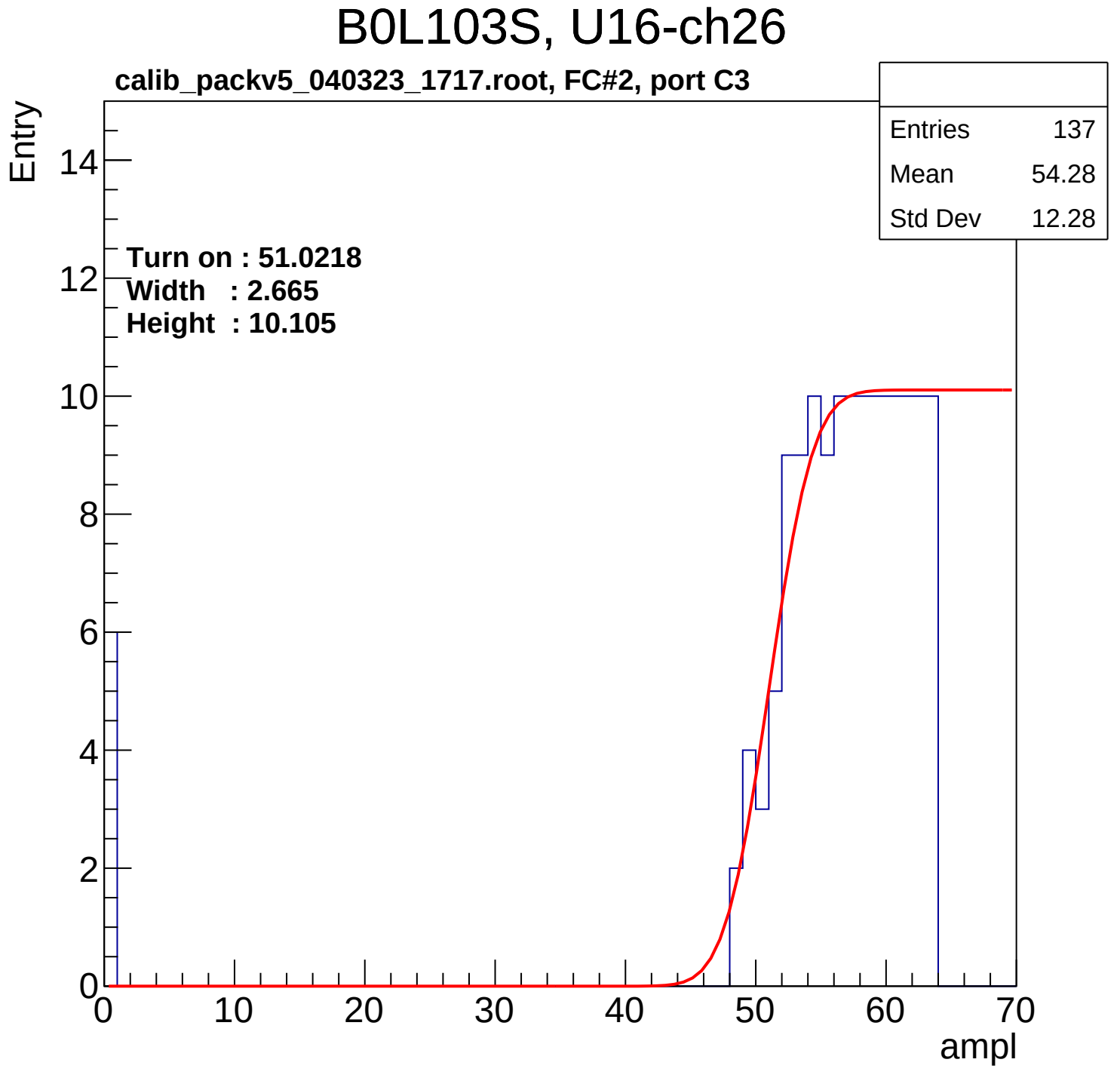
B0L103S, U16-ch26
calib_packv5_040323_1717.root, FC#2, port C3
Entries 137
Mean 54.28
Std Dev 12.28
Turn on : 51.0218
Width : 2.665
Height : 10.105
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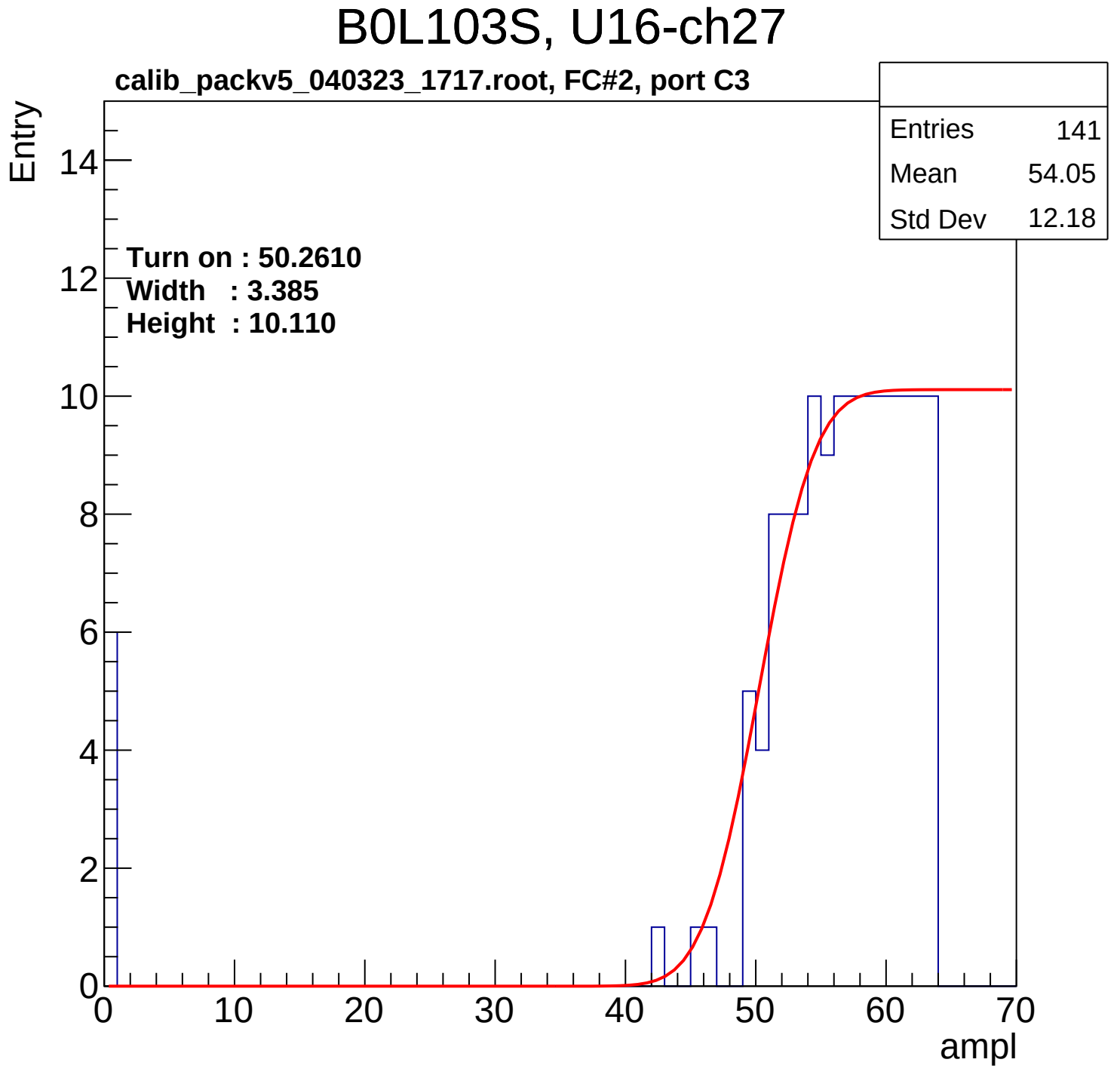
B0L103S, U16-ch27
calib_packv5_040323_1717.root, FC#2, port C3
Entries 141
Mean 54.05
Std Dev 12.18
Turn on : 50.2610
Width : 3.385
Height : 10.110
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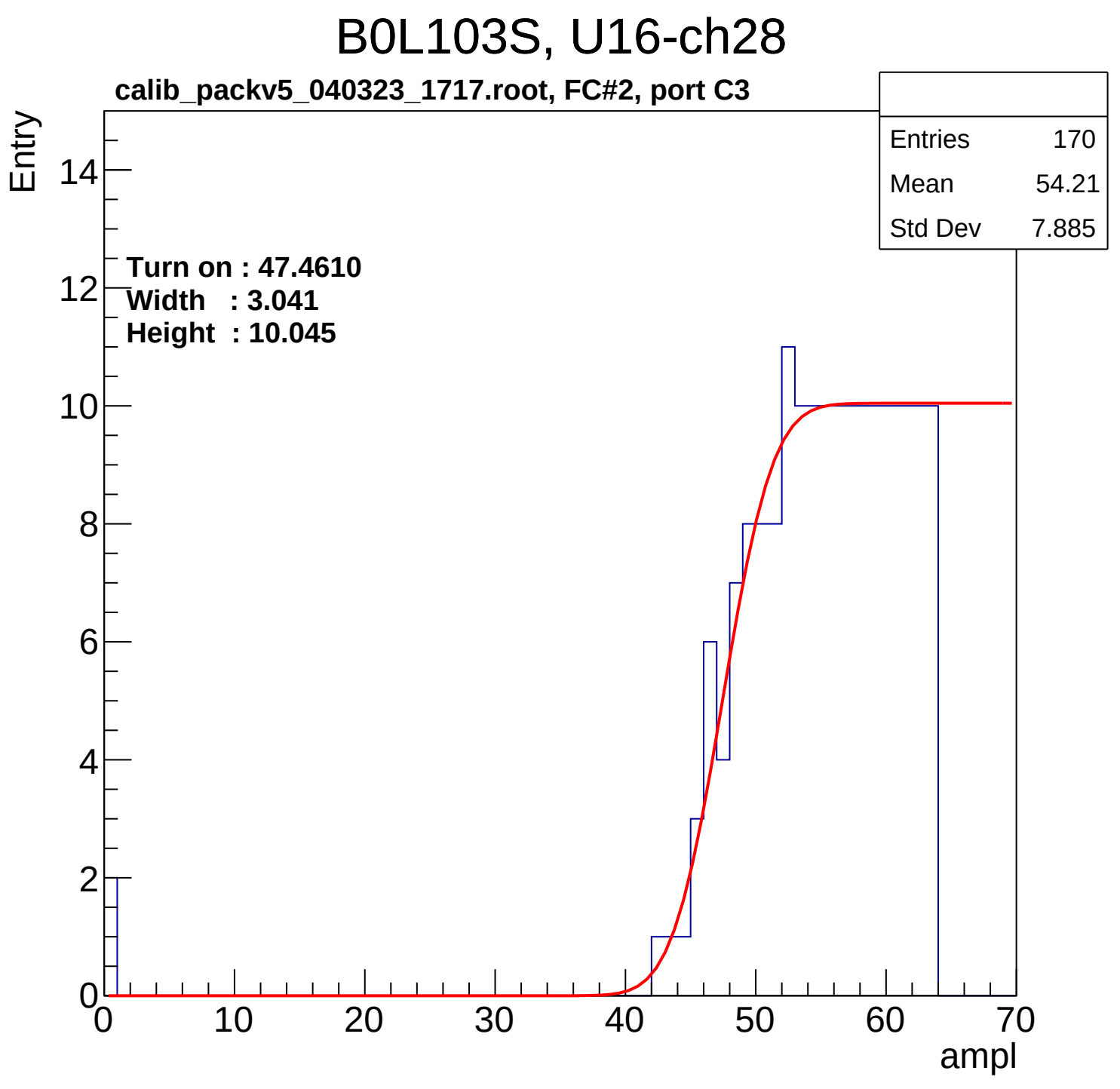
B0L103S, U16-ch28
calib_packv5_040323_1717.root, FC#2, port C3
Entries 170
Mean 54.21
Std Dev 7.885
Turn on : 47.4610
Width : 3.041
Height : 10.045
Entry
ampl
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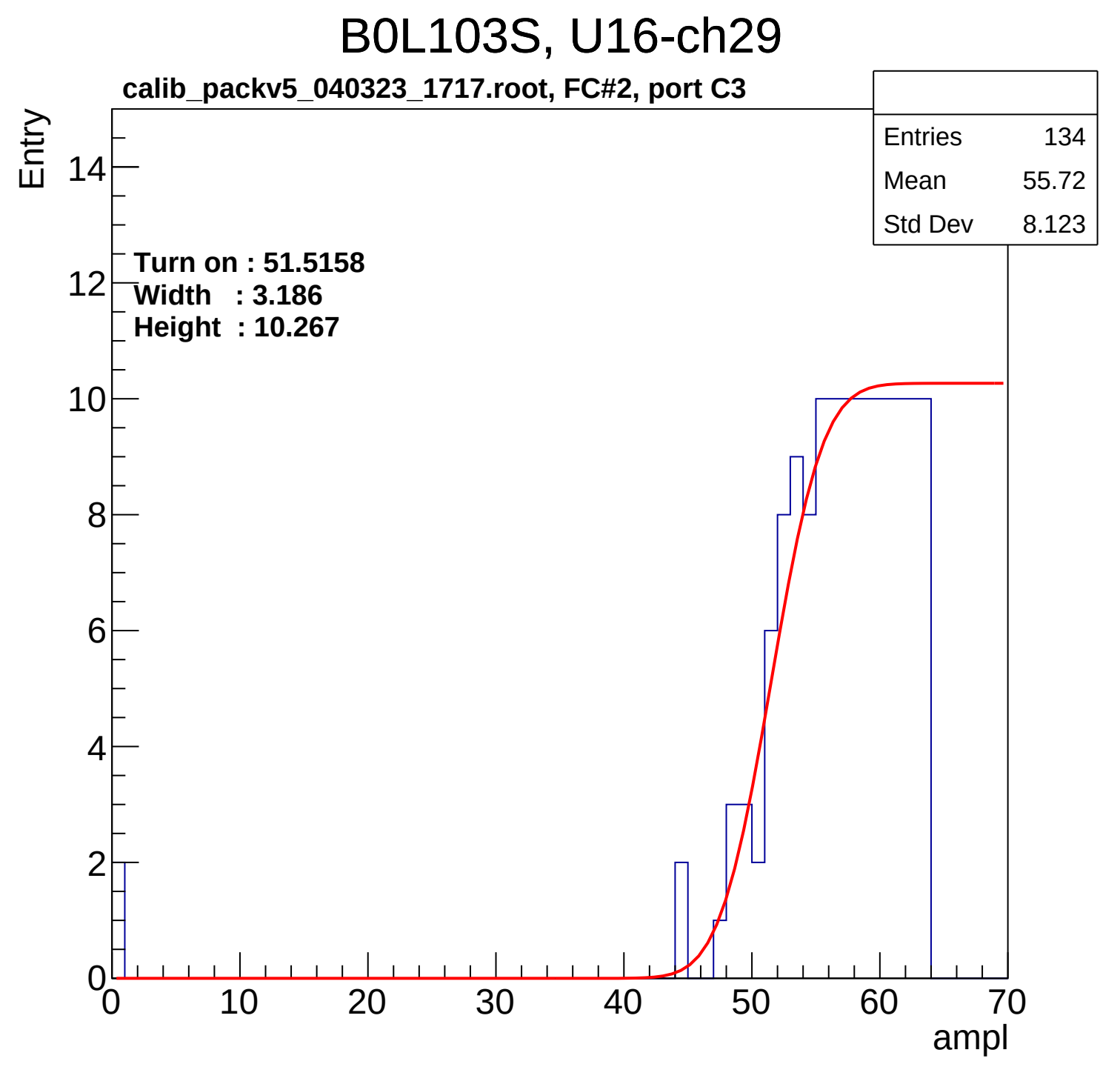
B0L103S, U16-ch29
calib_packv5_040323_1717.root, FC#2, port C3
Entries 134
Mean 55.72
Std Dev 8.123
Turn on : 51.5158
Width : 3.186
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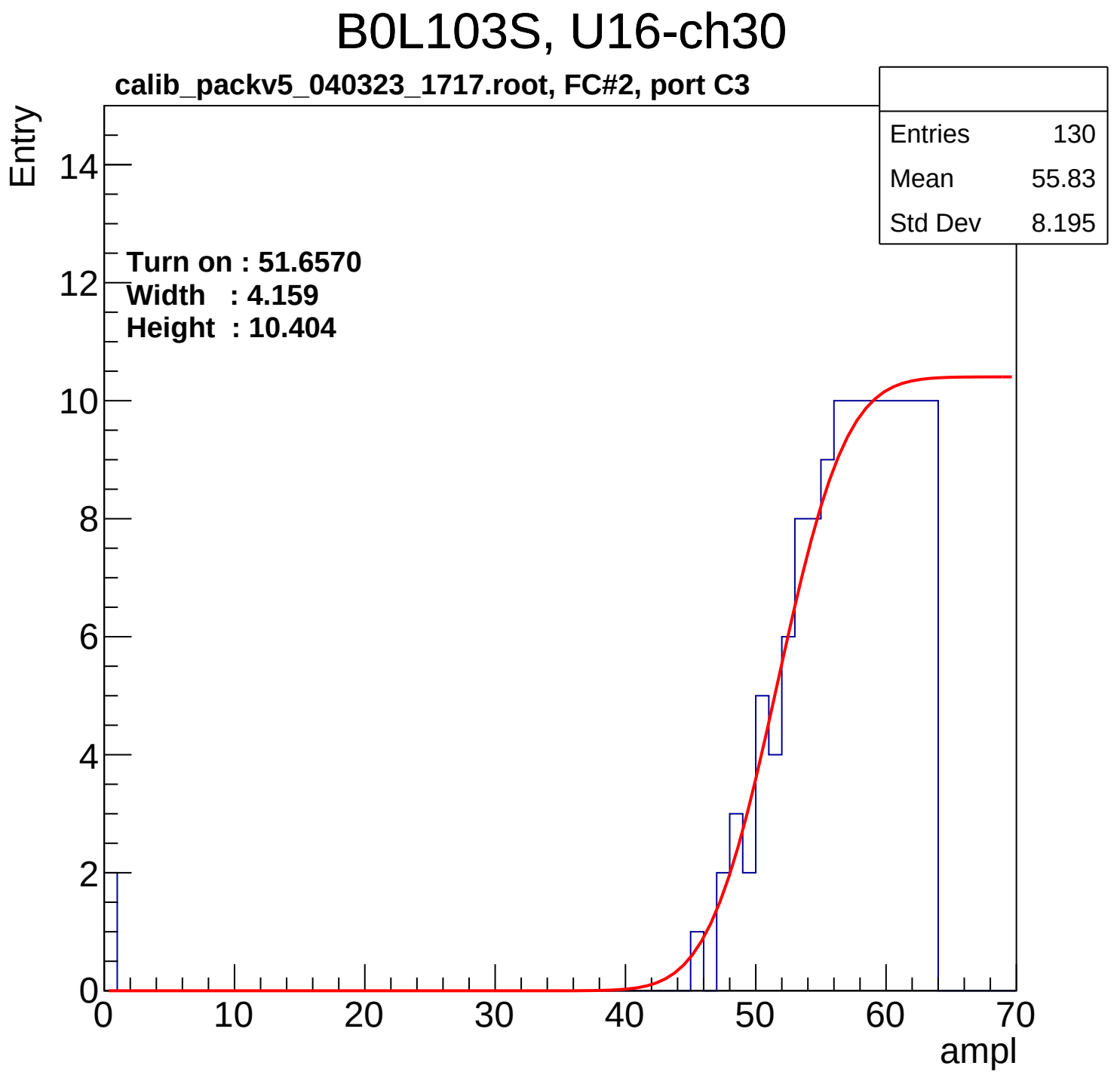
B0L103S, U16-ch30
calib_packv5_040323_1717.root, FC#2, port C3
Entries 130
Mean 55.83
Std Dev 8.195
Turn on : 51.6570
Width : 4.159
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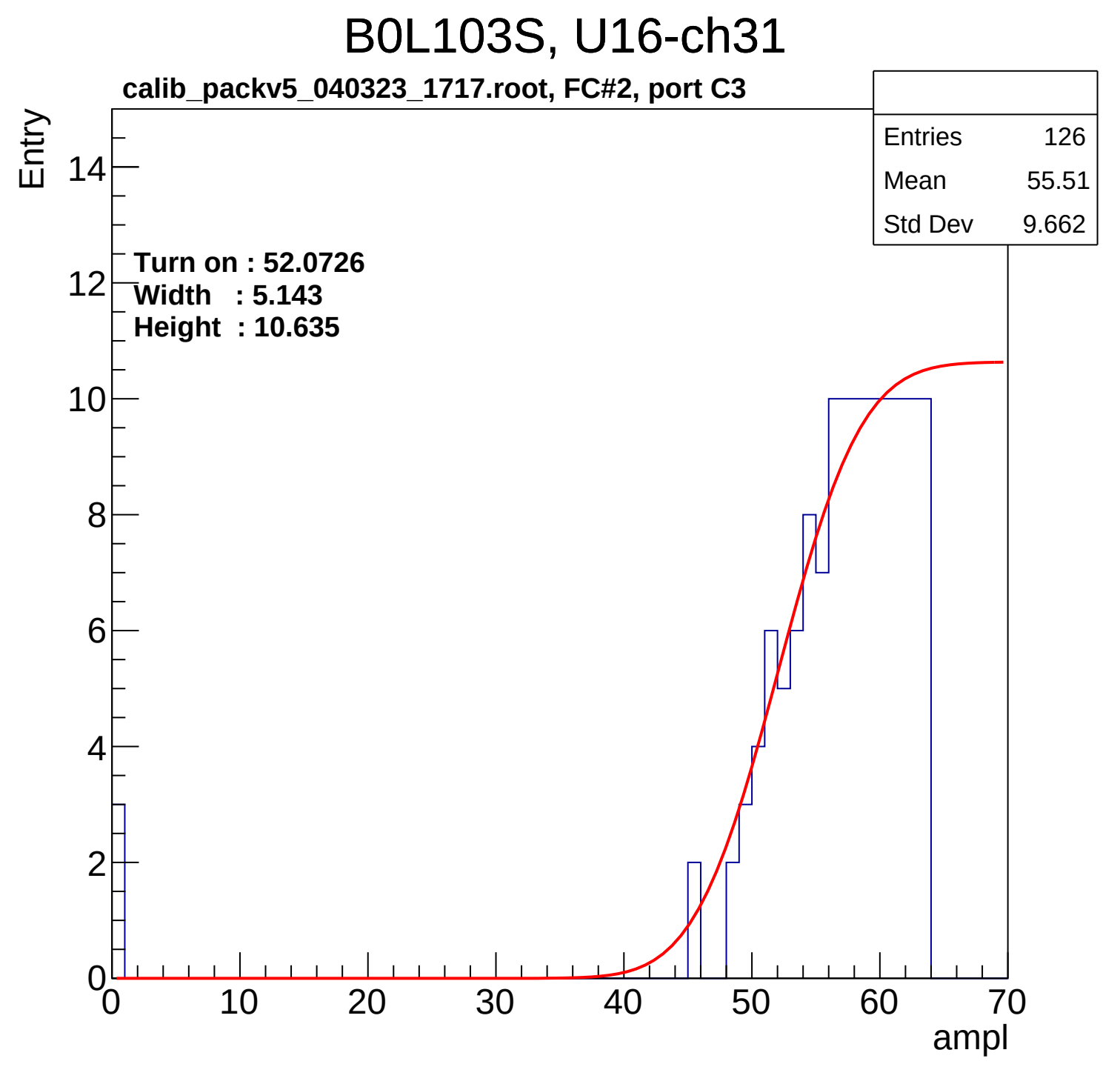
B0L103S, U16-ch31
calib_packv5_040323_1717.root, FC#2, port C3
Entries 126
Mean 55.51
Std Dev 9.662
Turn on : 52.0726
Width : 5.143
Height : 10.635
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ampl
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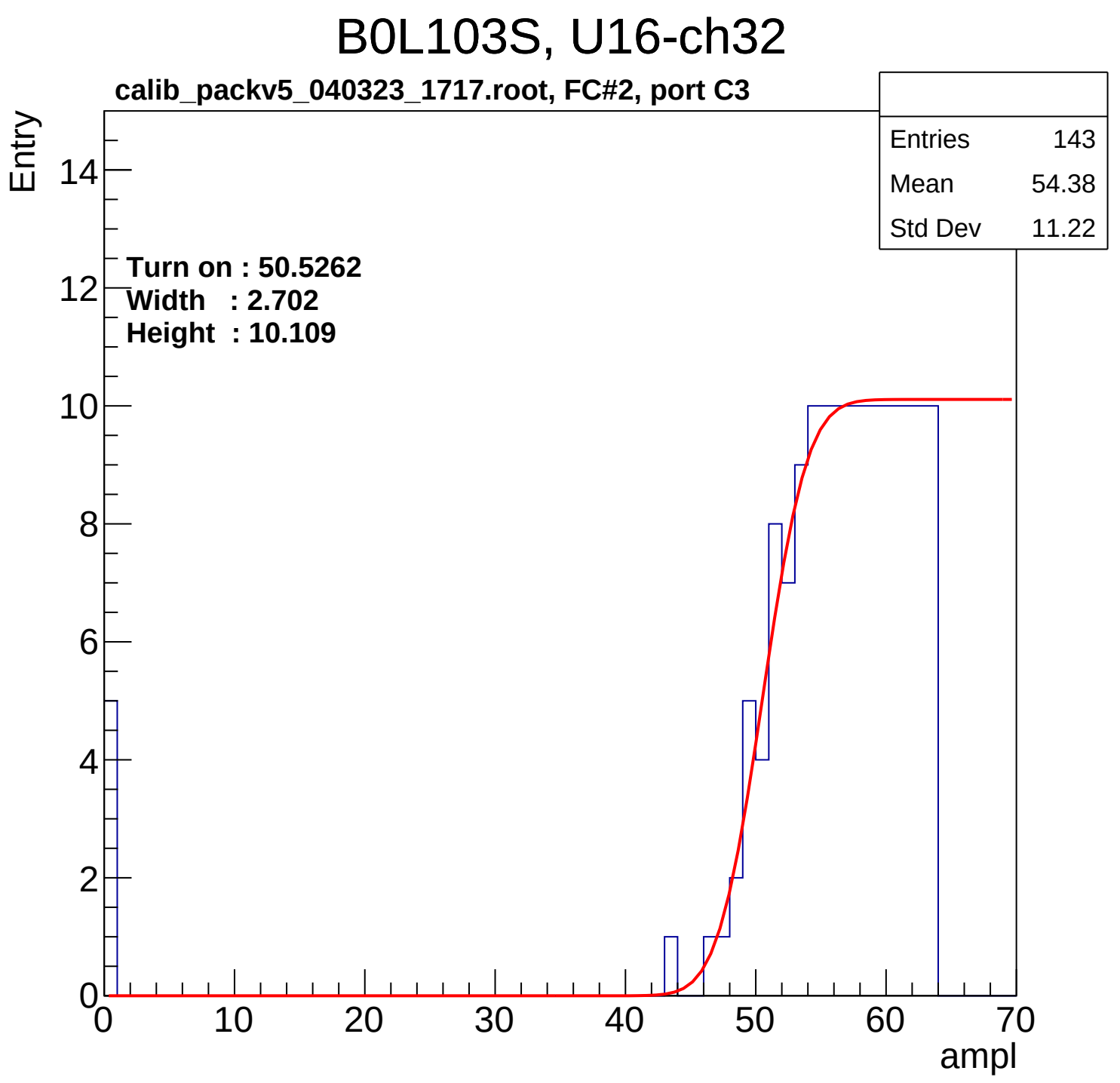
B0L103S, U16-ch32
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 54.38
Std Dev 11.22
Turn on : 50.5262
Width : 2.702
Height : 10.109
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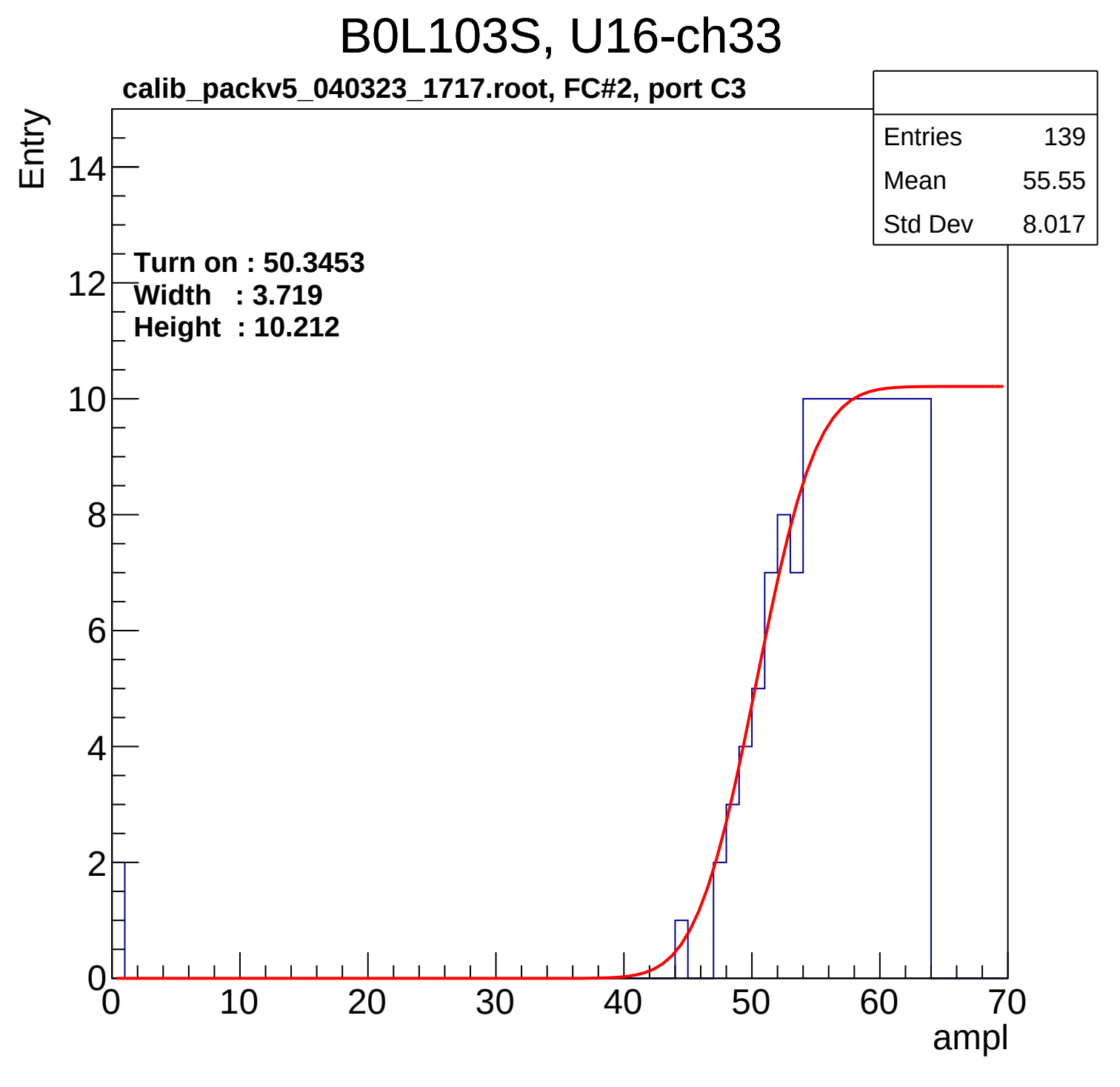
B0L103S, U16-ch33
calib_packv5_040323_1717.root, FC#2, port C3
Entries 139
Mean 55.55
Std Dev 8.017
Turn on : 50.3453
Width : 3.719
Height : 10.212
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ampl
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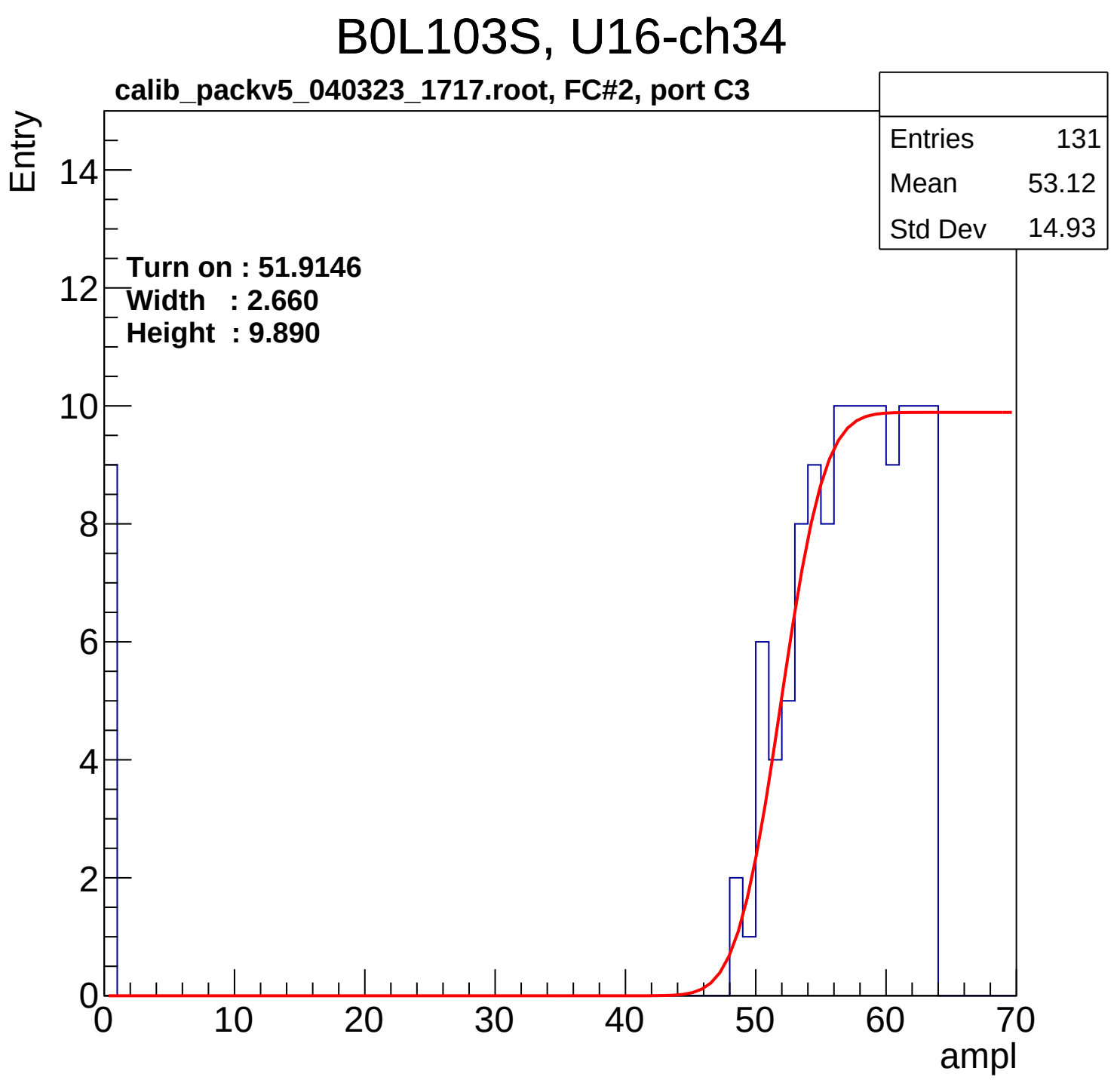
B0L103S, U16-ch34
calib_packv5_040323_1717.root, FC#2, port C3
Entries 131
Mean 53.12
Std Dev 14.93
Turn on : 51.9146
Width : 2.660
Height : 9.890
Entry
ampl
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6
8
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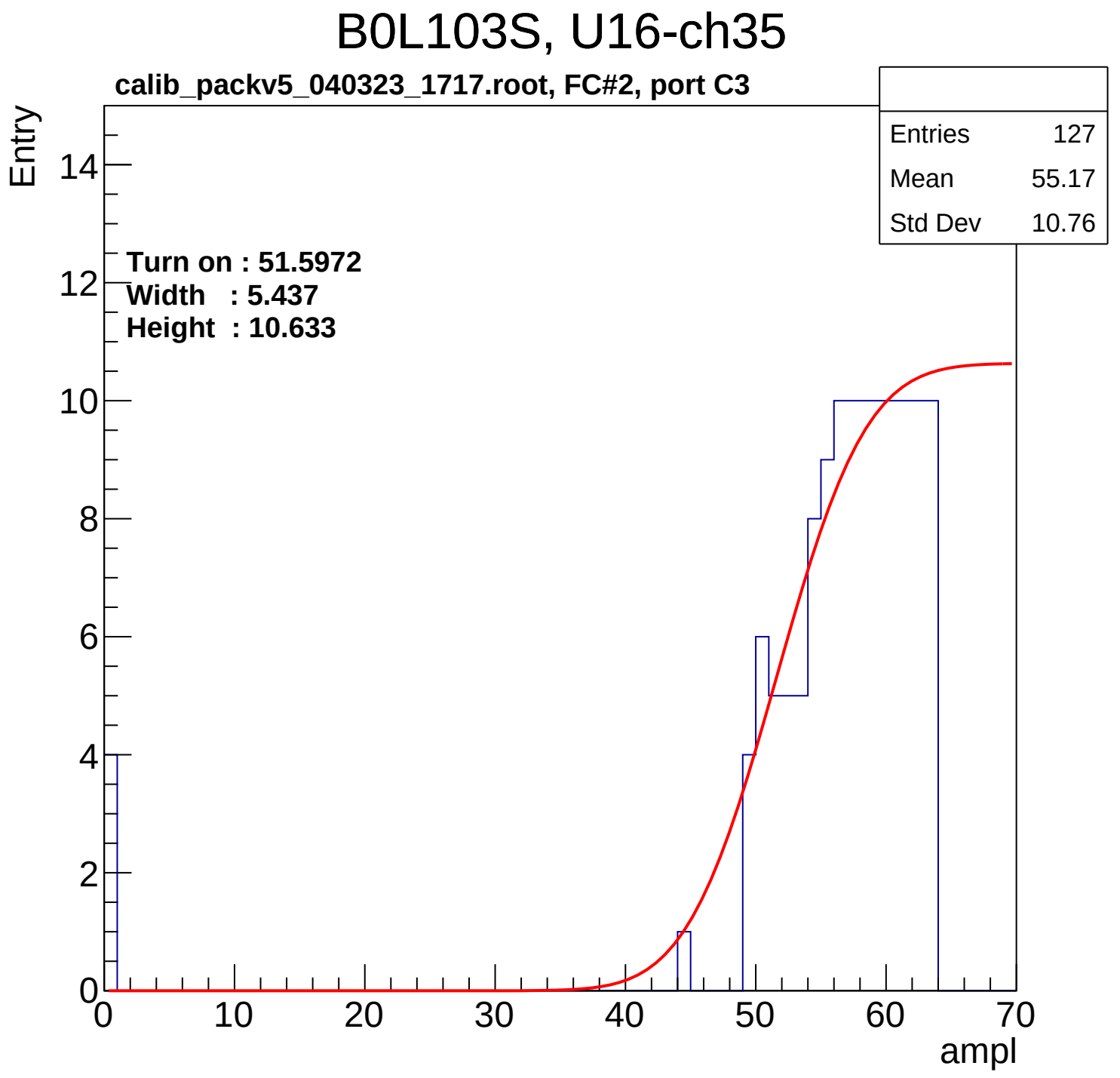
B0L103S, U16-ch35
calib_packv5_040323_1717.root, FC#2, port C3
Entries 127
Mean 55.17
Std Dev 10.76
Turn on : 51.5972
Width : 5.437
Height : 10.633
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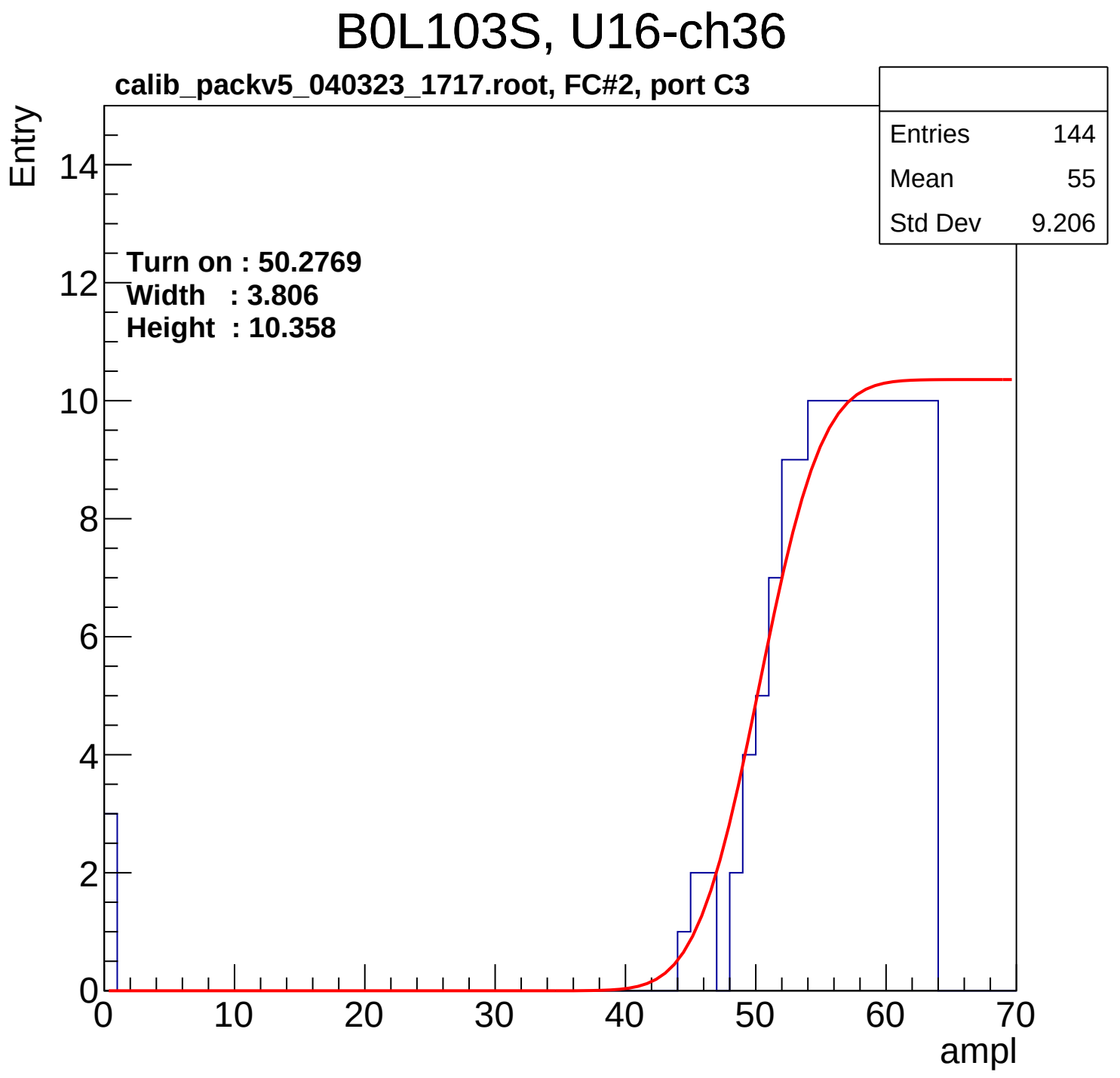
B0L103S, U16-ch36
calib_packv5_040323_1717.root, FC#2, port C3
Entries 144
Mean 55
Std Dev 9.206
Turn on : 50.2769
Width : 3.806
Height : 10.358
Entry
ampl
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6
8
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12
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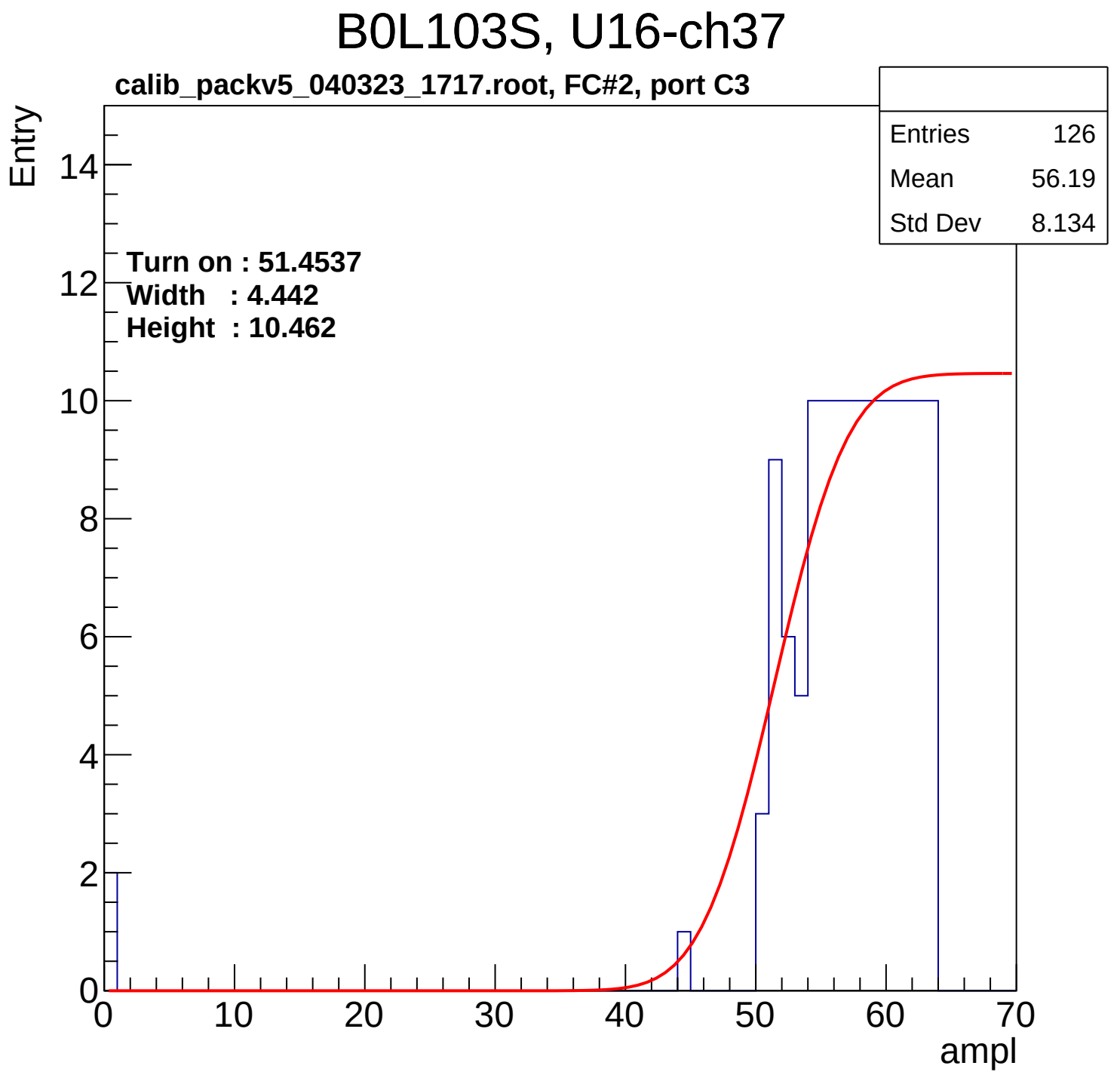
B0L103S, U16-ch37
calib_packv5_040323_1717.root, FC#2, port C3
Entries 126
Mean 56.19
Std Dev 8.134
Turn on : 51.4537
Width : 4.442
Height : 10.462
Entry
ampl
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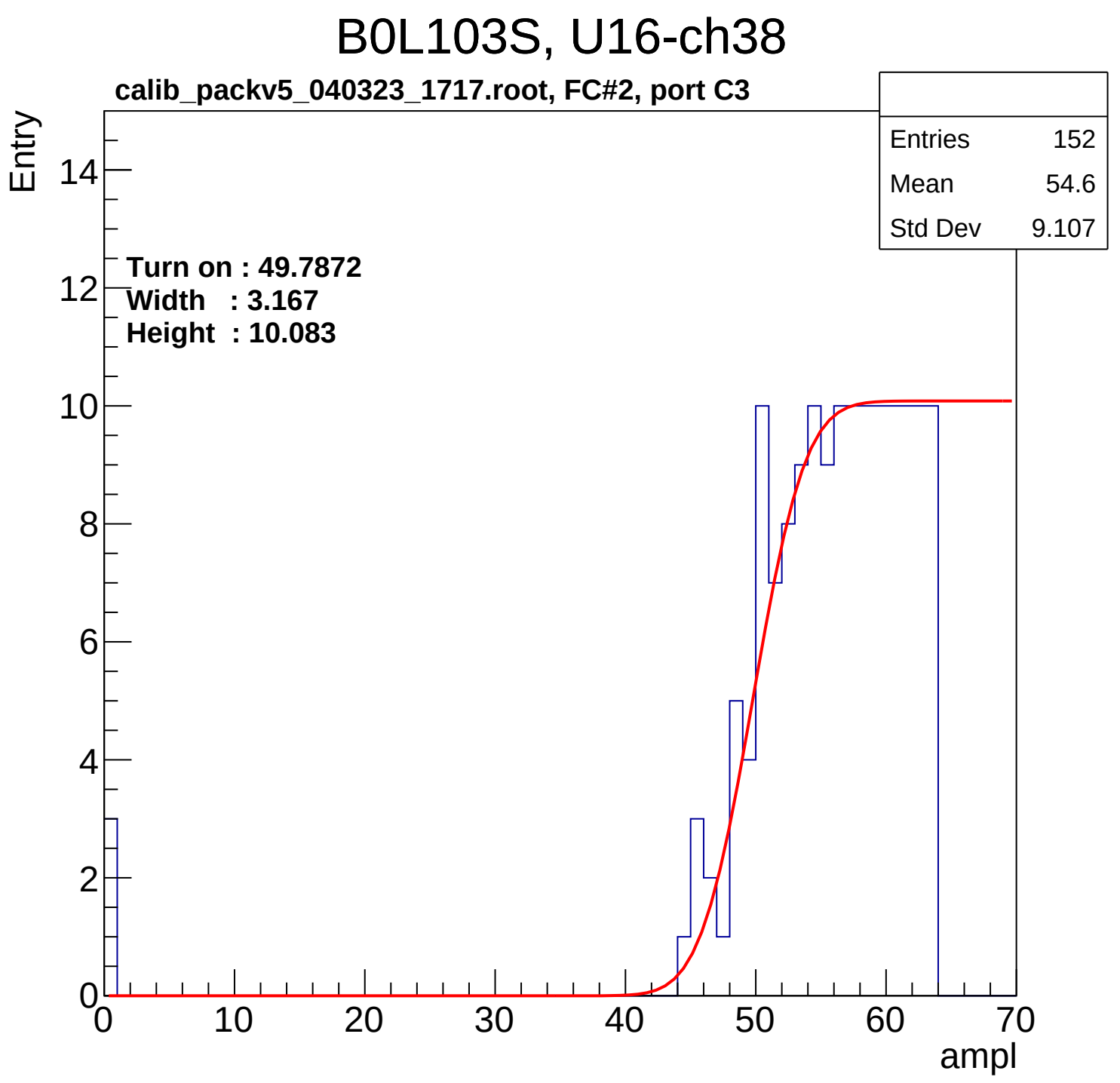
B0L103S, U16-ch38
calib_packv5_040323_1717.root, FC#2, port C3
Entries 152
Mean 54.6
Std Dev 9.107
Turn on : 49.7872
Width : 3.167
Height : 10.083
Entry
ampl
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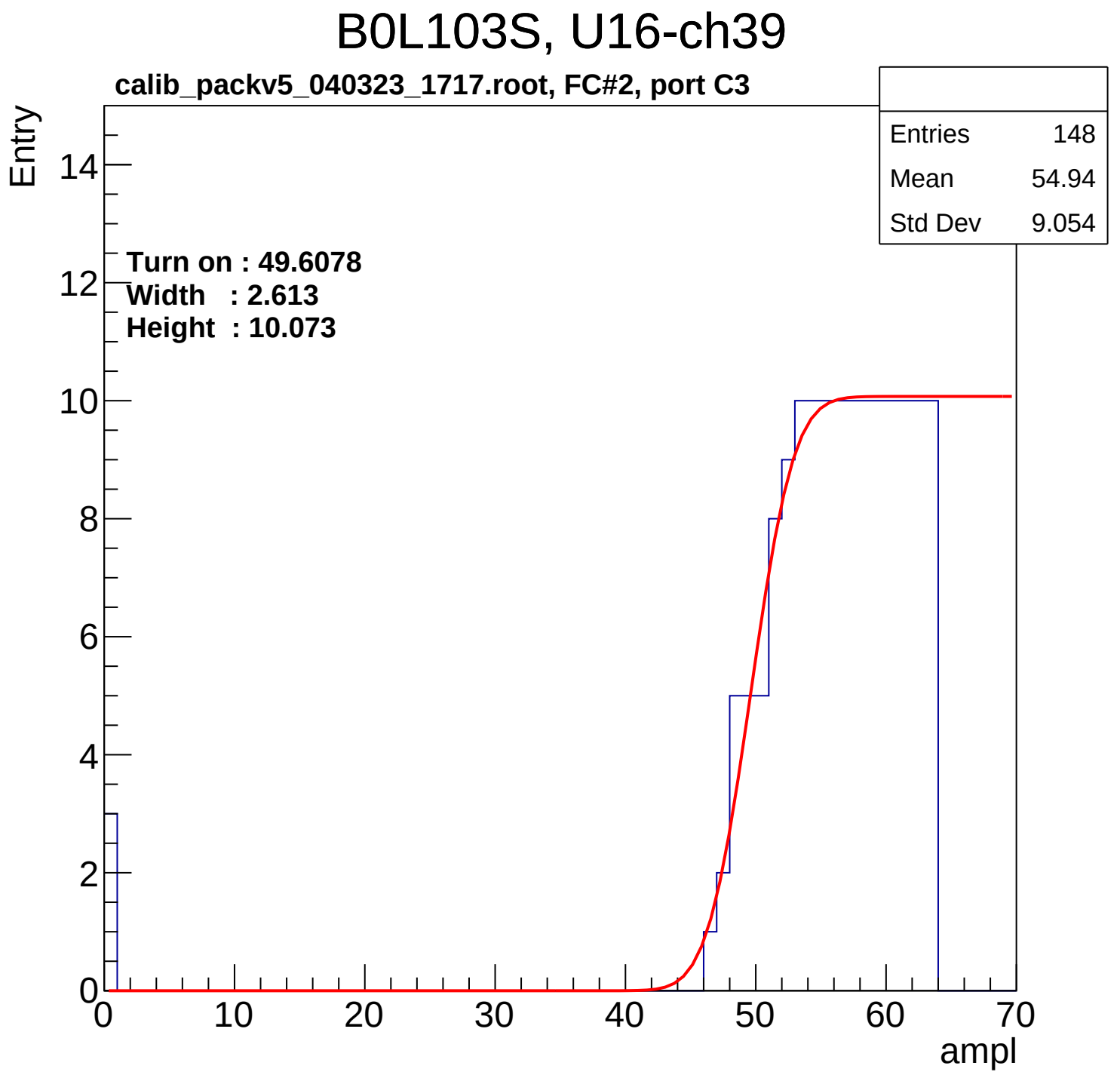
B0L103S, U16-ch39
calib_packv5_040323_1717.root, FC#2, port C3
Entries 148
Mean 54.94
Std Dev 9.054
Turn on : 49.6078
Width : 2.613
Height : 10.073
Entry
ampl
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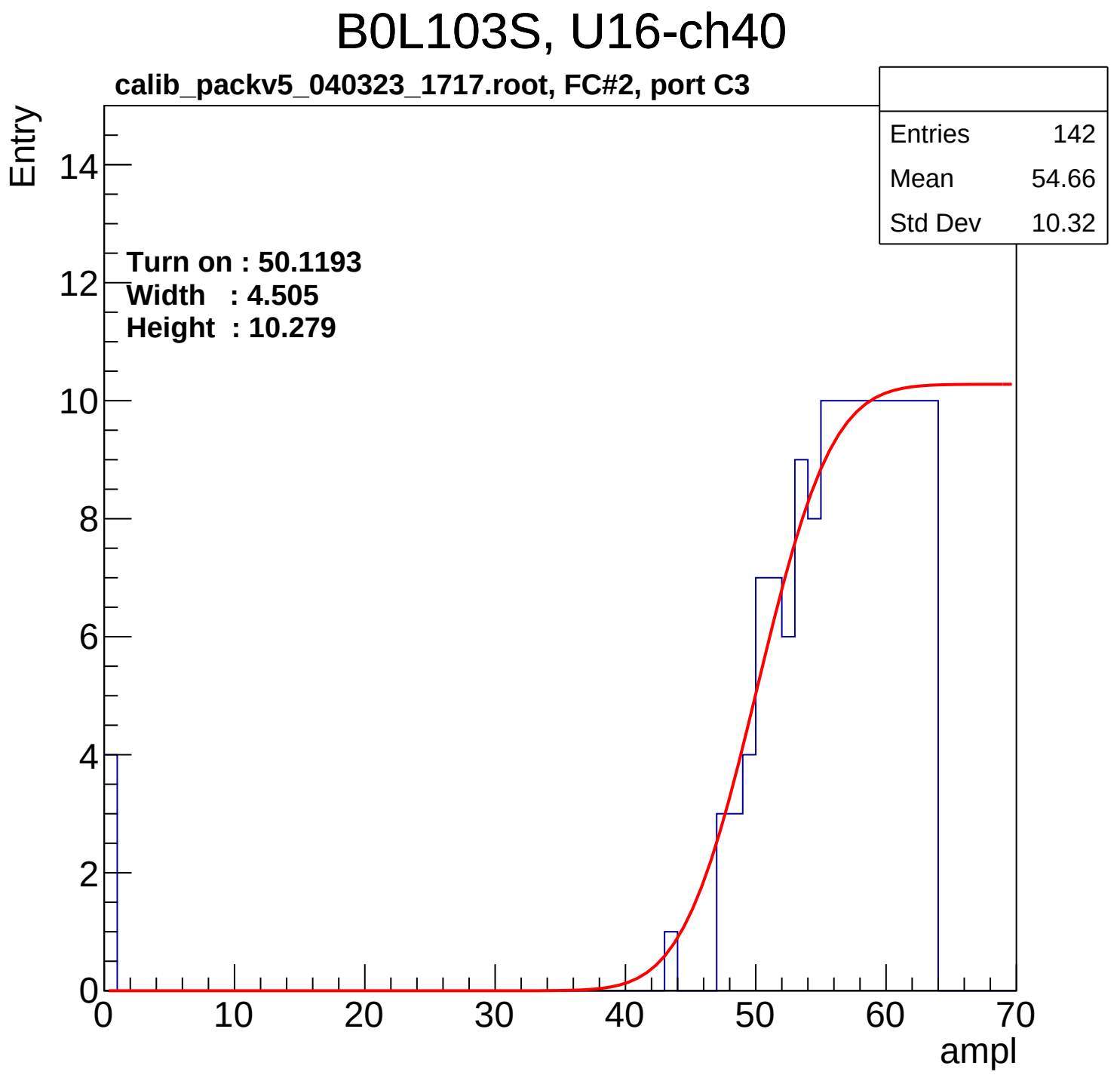
B0L103S, U16-ch40
calib_packv5_040323_1717.root, FC#2, port C3
Entries 142
Mean 54.66
Std Dev 10.32
Turn on : 50.1193
Width : 4.505
Height : 10.279
Entry
ampl
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4
6
8
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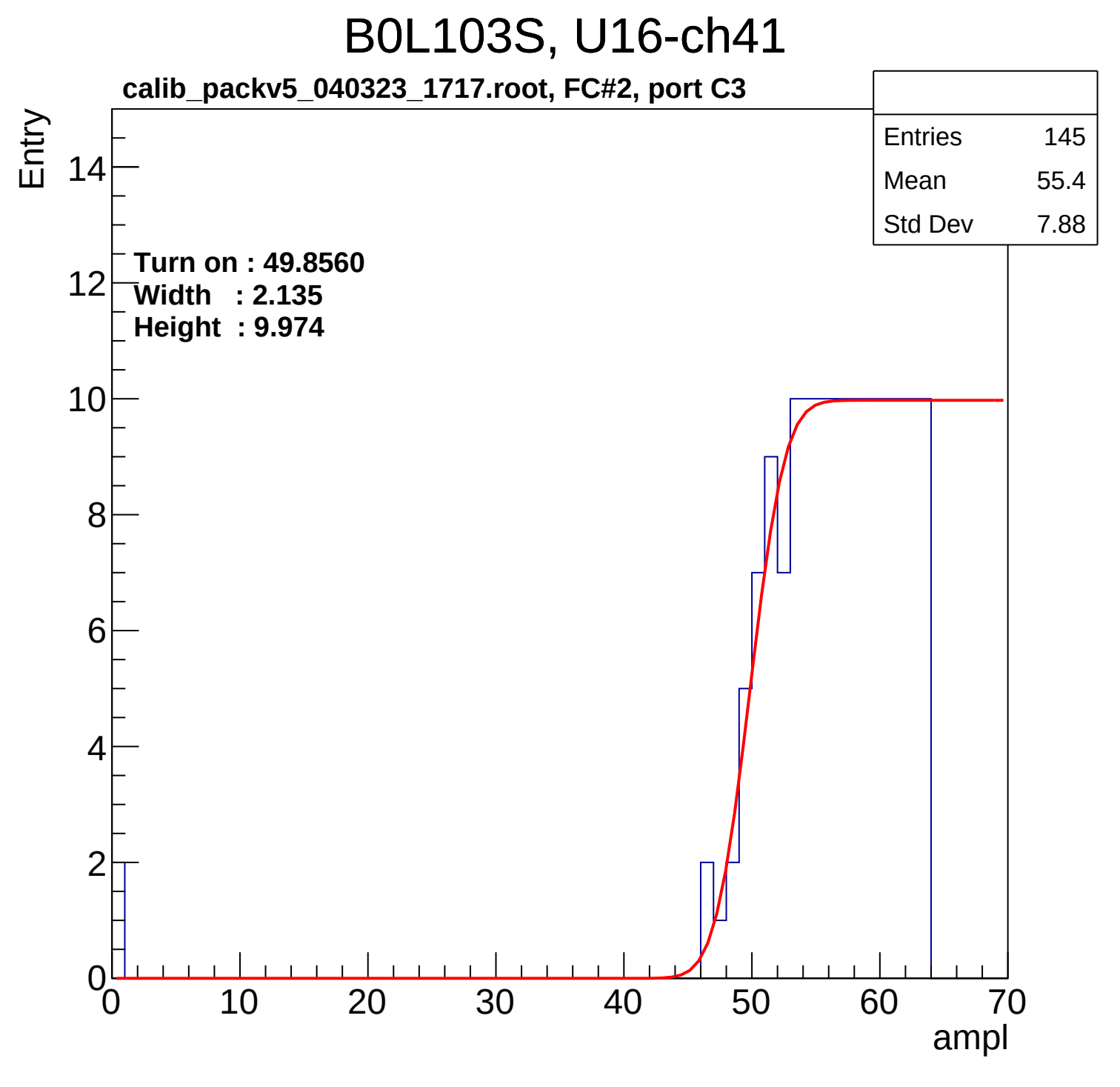
B0L103S, U16-ch41
calib_packv5_040323_1717.root, FC#2, port C3
Entries 145
Mean 55.4
Std Dev 7.88
Turn on : 49.8560
Width : 2.135
Height : 9.974
Entry
ampl
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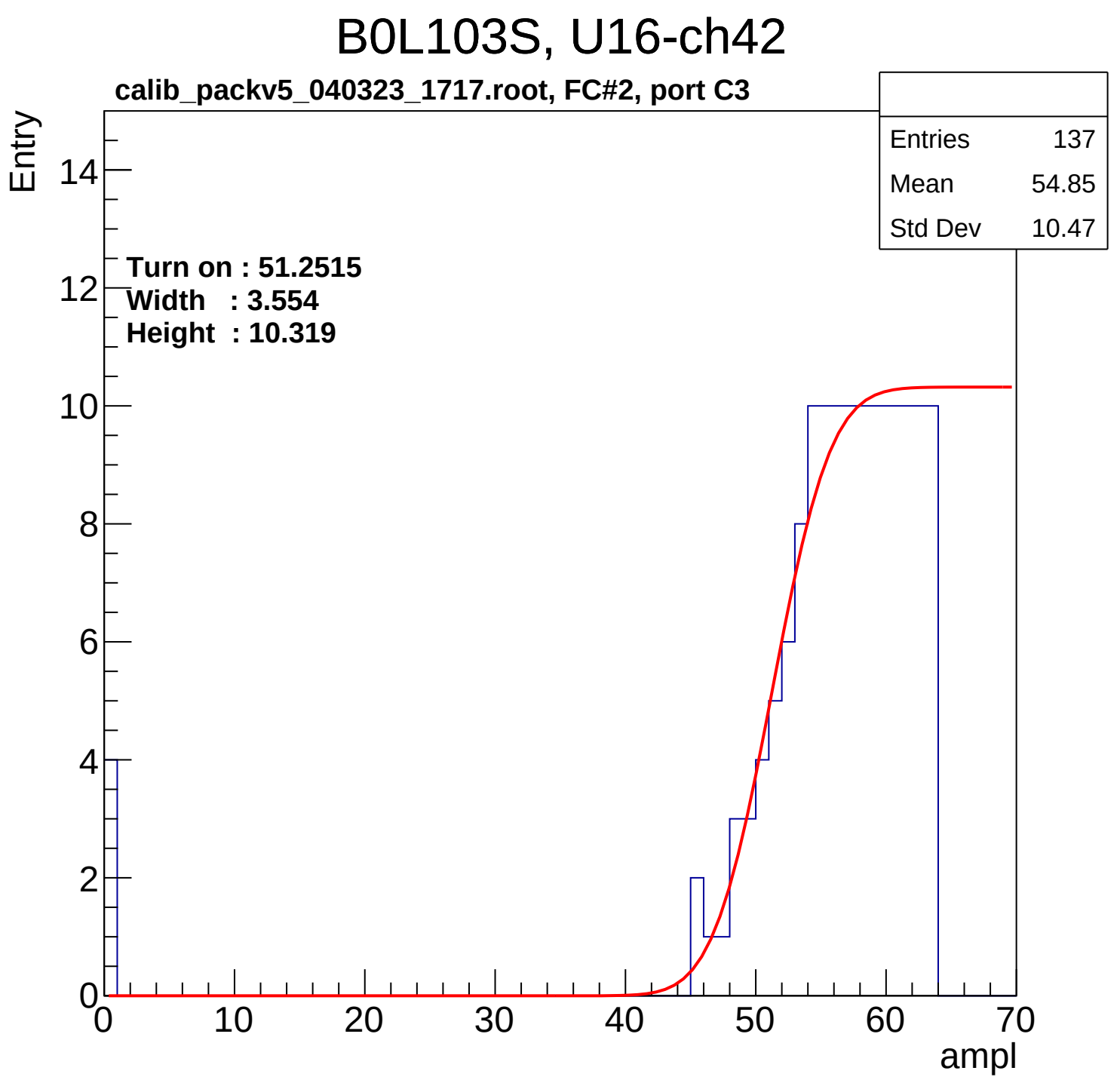
B0L103S, U16-ch42
calib_packv5_040323_1717.root, FC#2, port C3
Entries 137
Mean 54.85
Std Dev 10.47
Turn on : 51.2515
Width : 3.554
Height : 10.319
Entry
ampl
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8
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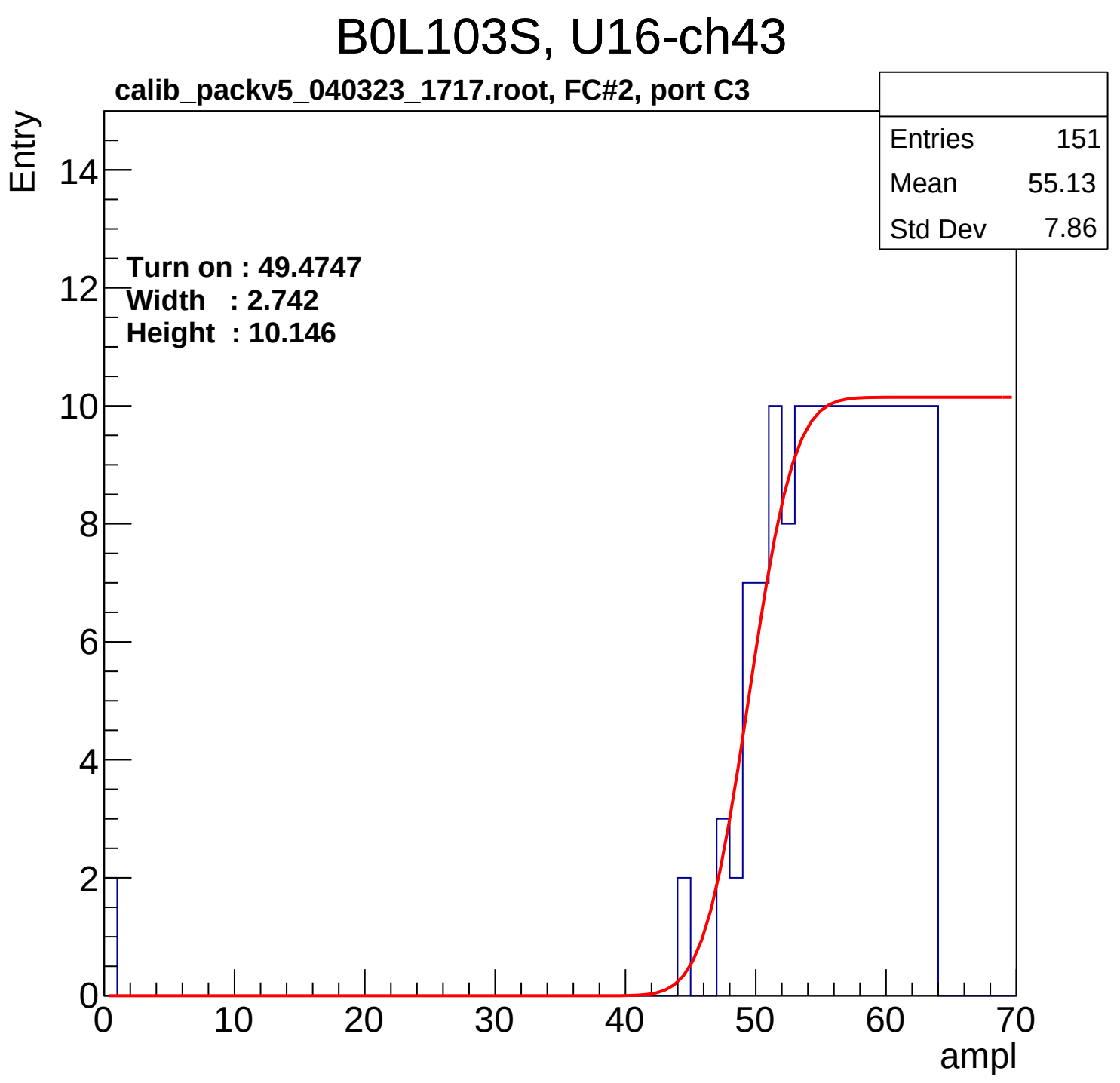
B0L103S, U16-ch43
calib_packv5_040323_1717.root, FC#2, port C3
Entries 151
Mean 55.13
Std Dev 7.86
Turn on : 49.4747
Width : 2.742
Height : 10.146
Entry
ampl
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6
8
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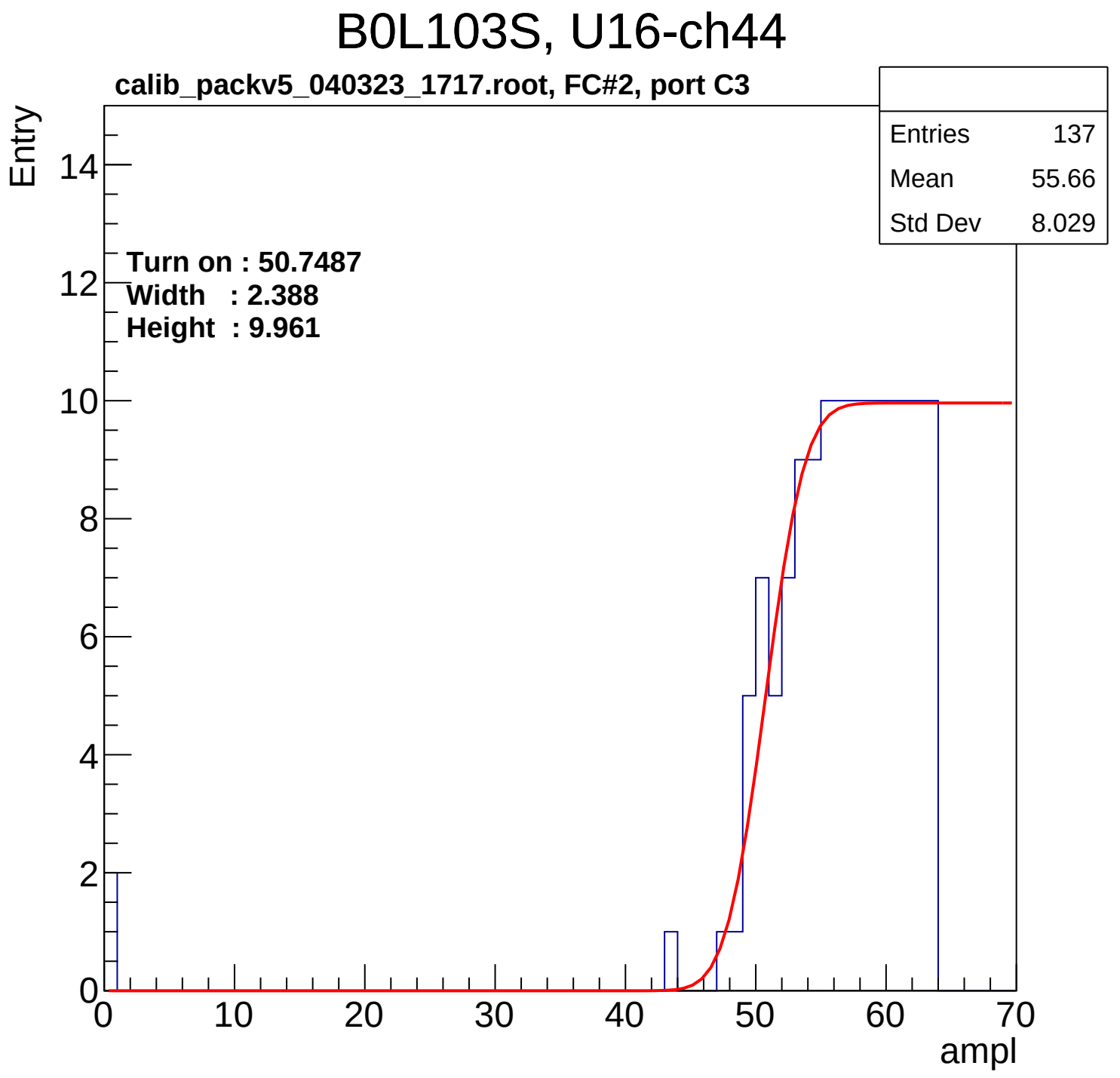
B0L103S, U16-ch44
calib_packv5_040323_1717.root, FC#2, port C3
Entries 137
Mean 55.66
Std Dev 8.029
Turn on : 50.7487
Width : 2.388
Height : 9.961
Entry
ampl
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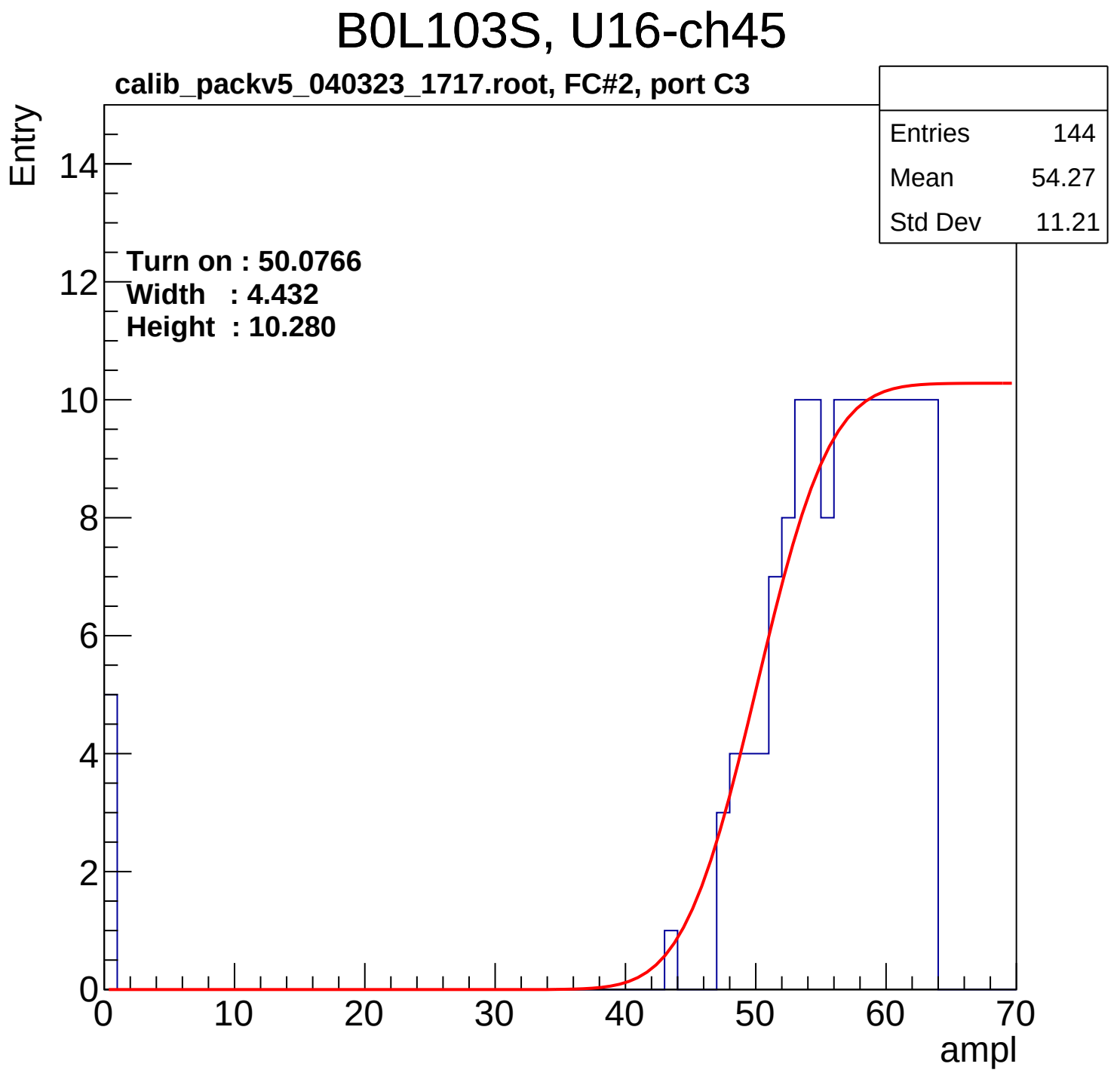
B0L103S, U16-ch45
calib_packv5_040323_1717.root, FC#2, port C3
Entries 144
Mean 54.27
Std Dev 11.21
Turn on : 50.0766
Width : 4.432
Height : 10.280
Entry
ampl
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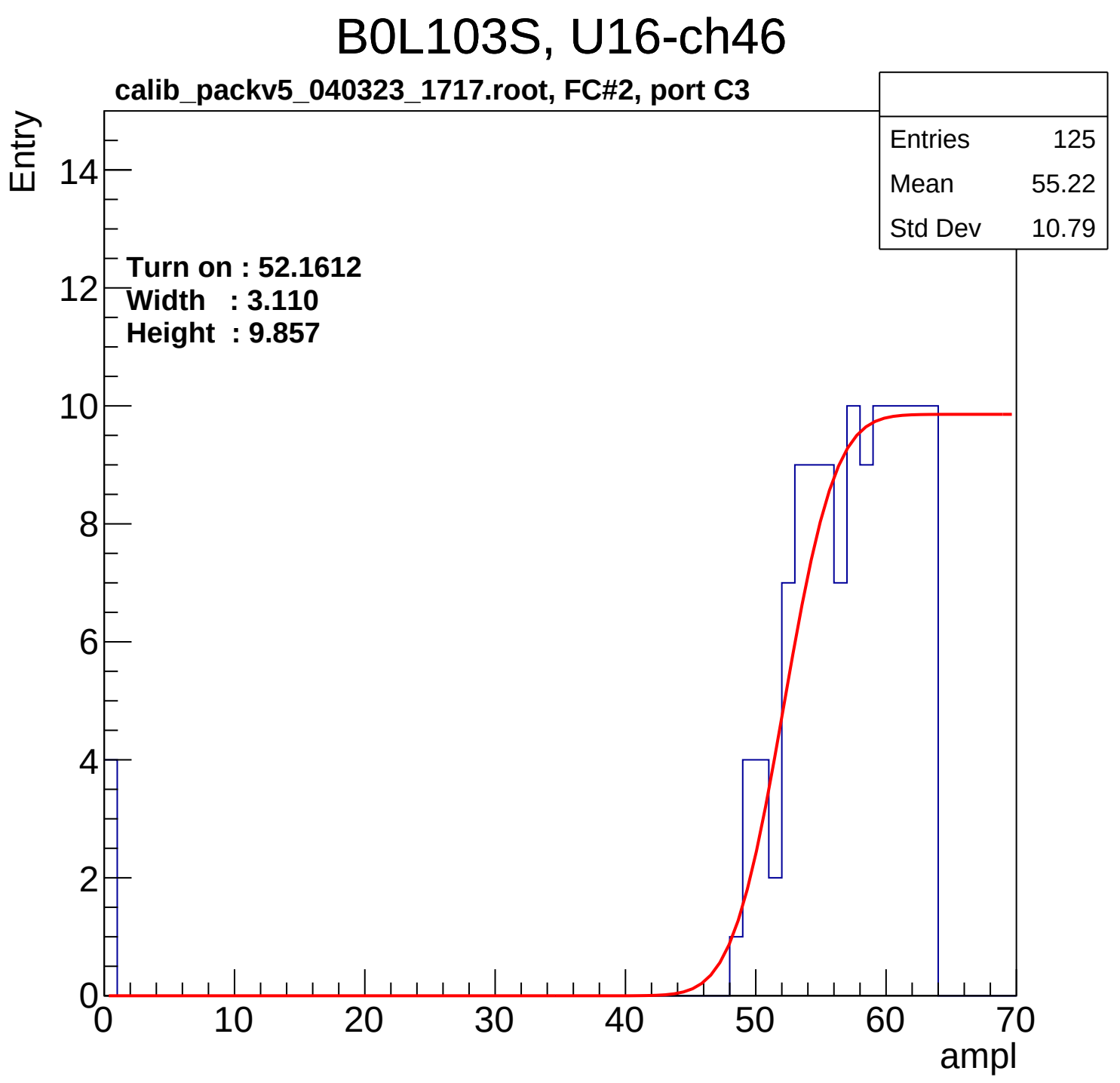
B0L103S, U16-ch46
calib_packv5_040323_1717.root, FC#2, port C3
Entries 125
Mean 55.22
Std Dev 10.79
Turn on : 52.1612
Width : 3.110
Height : 9.857
Entry
ampl
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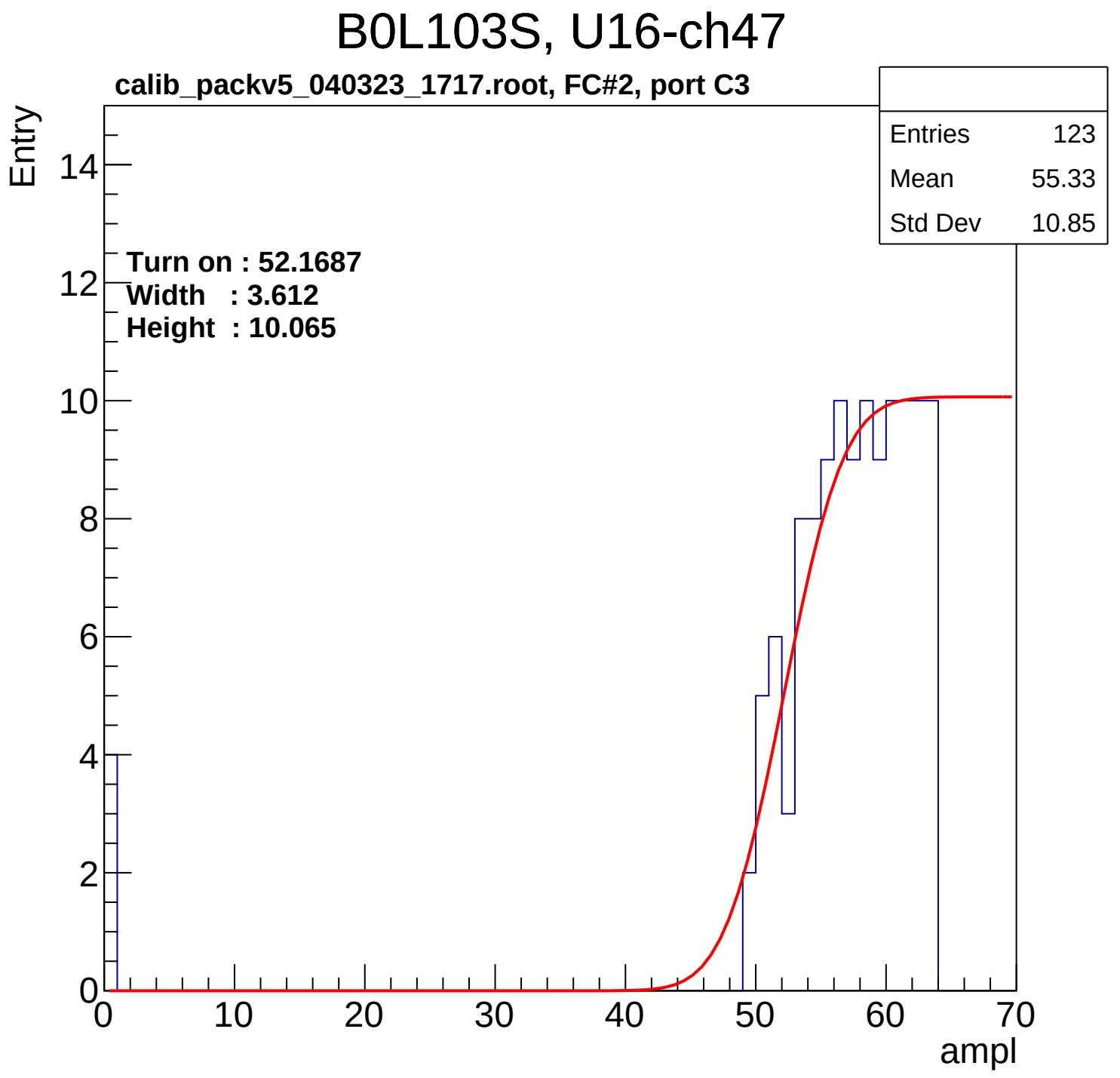
B0L103S, U16-ch47
calib_packv5_040323_1717.root, FC#2, port C3
Entries 123
Mean 55.33
Std Dev 10.85
Turn on : 52.1687
Width : 3.612
Height : 10.065
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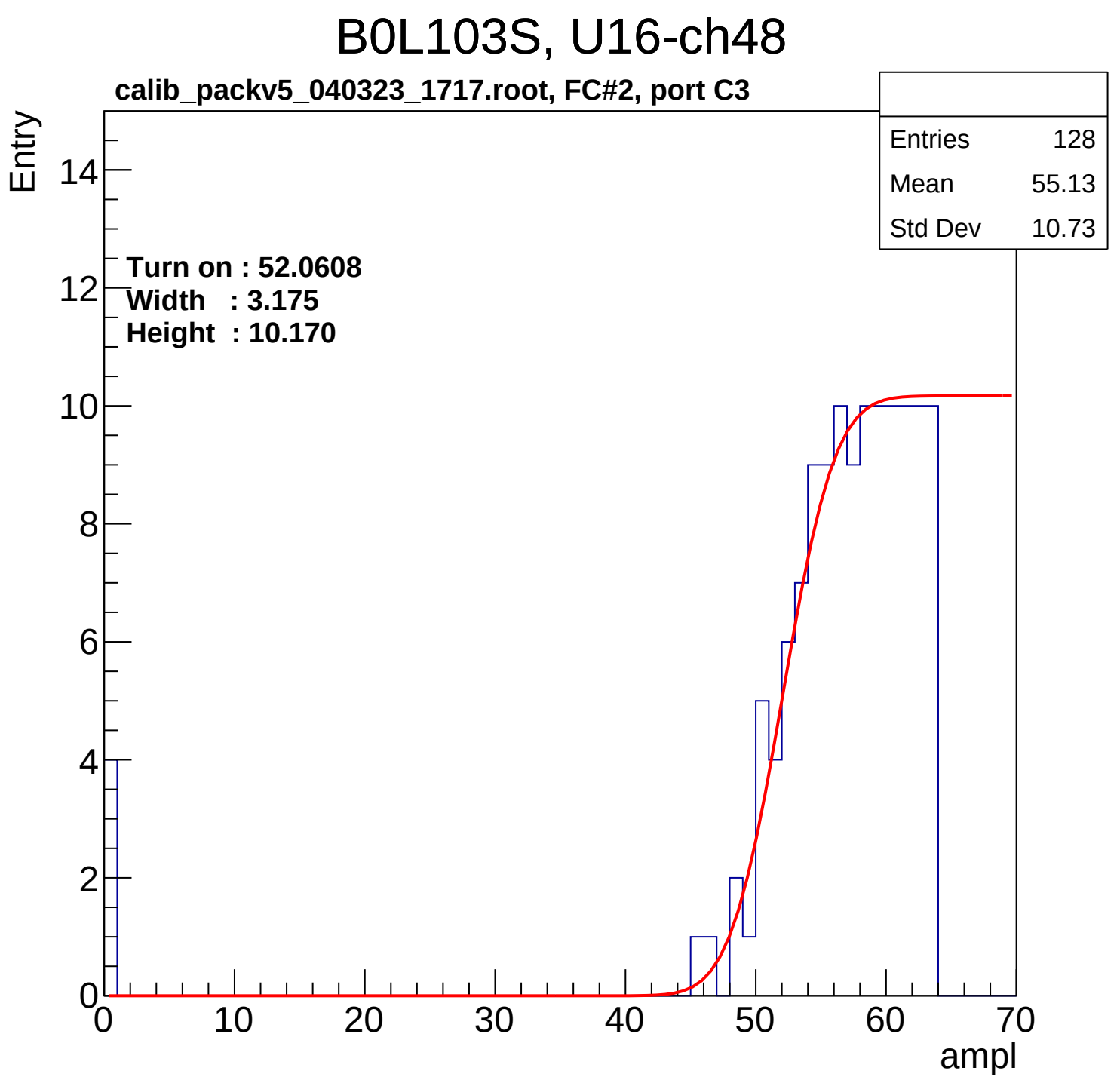
B0L103S, U16-ch48
calib_packv5_040323_1717.root, FC#2, port C3
Entries 128
Mean 55.13
Std Dev 10.73
Turn on : 52.0608
Width : 3.175
Height : 10.170
Entry
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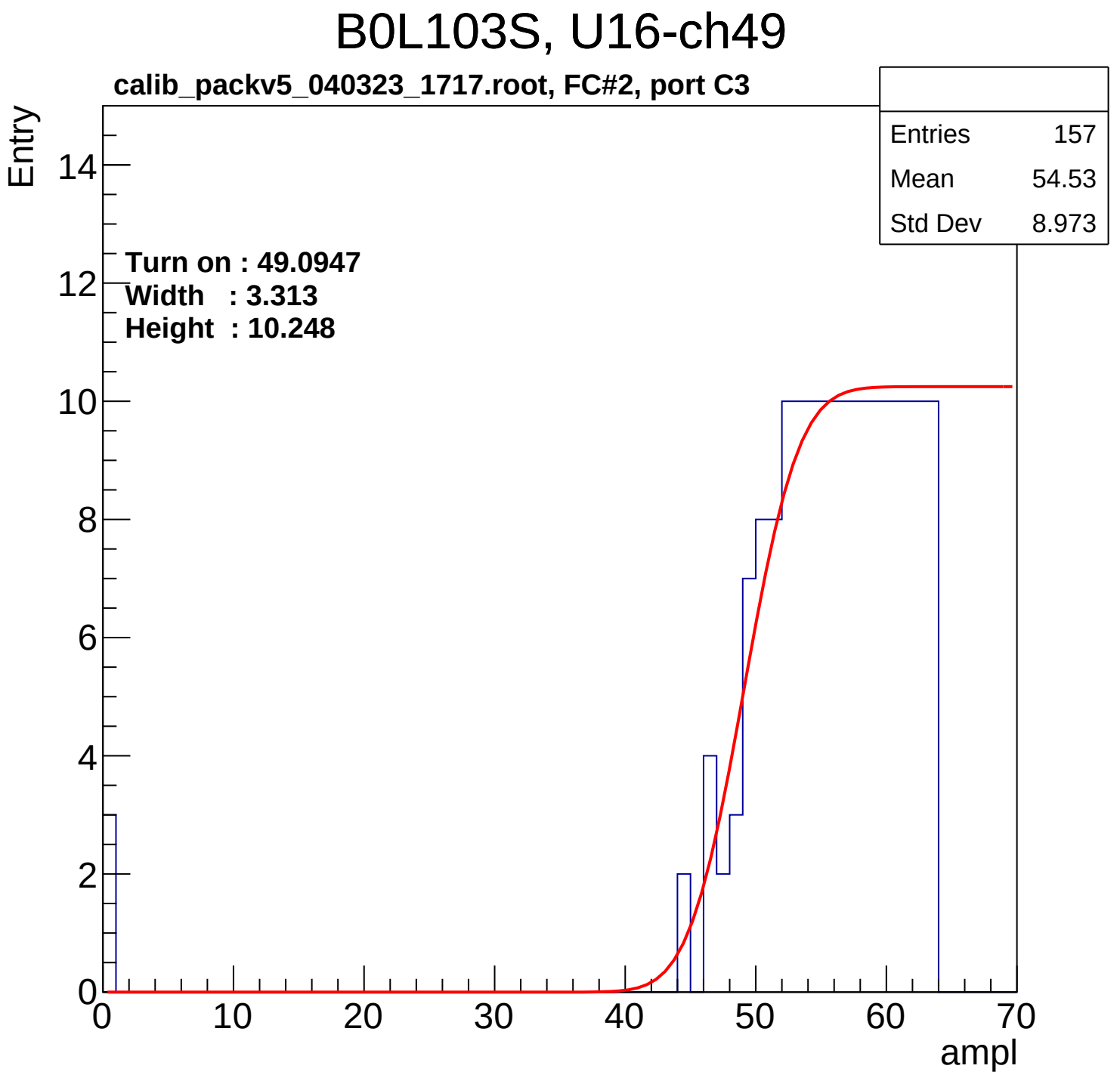
B0L103S, U16-ch49
calib_packv5_040323_1717.root, FC#2, port C3
Entries 157
Mean 54.53
Std Dev 8.973
Turn on : 49.0947
Width : 3.313
Height : 10.248
Entry
ampl
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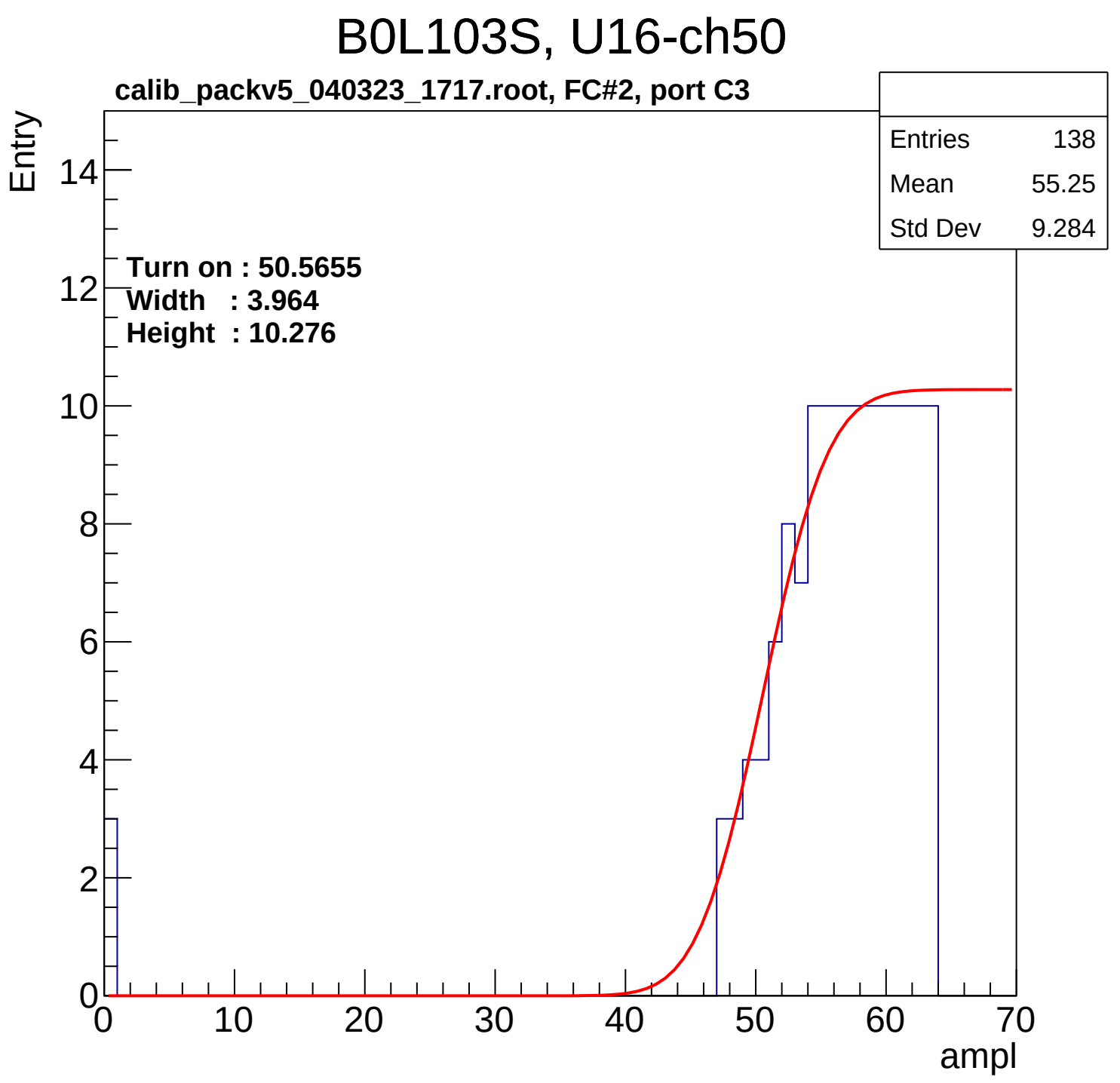
B0L103S, U16-ch50
calib_packv5_040323_1717.root, FC#2, port C3
Entries 138
Mean 55.25
Std Dev 9.284
Turn on : 50.5655
Width : 3.964
Height : 10.276
Entry
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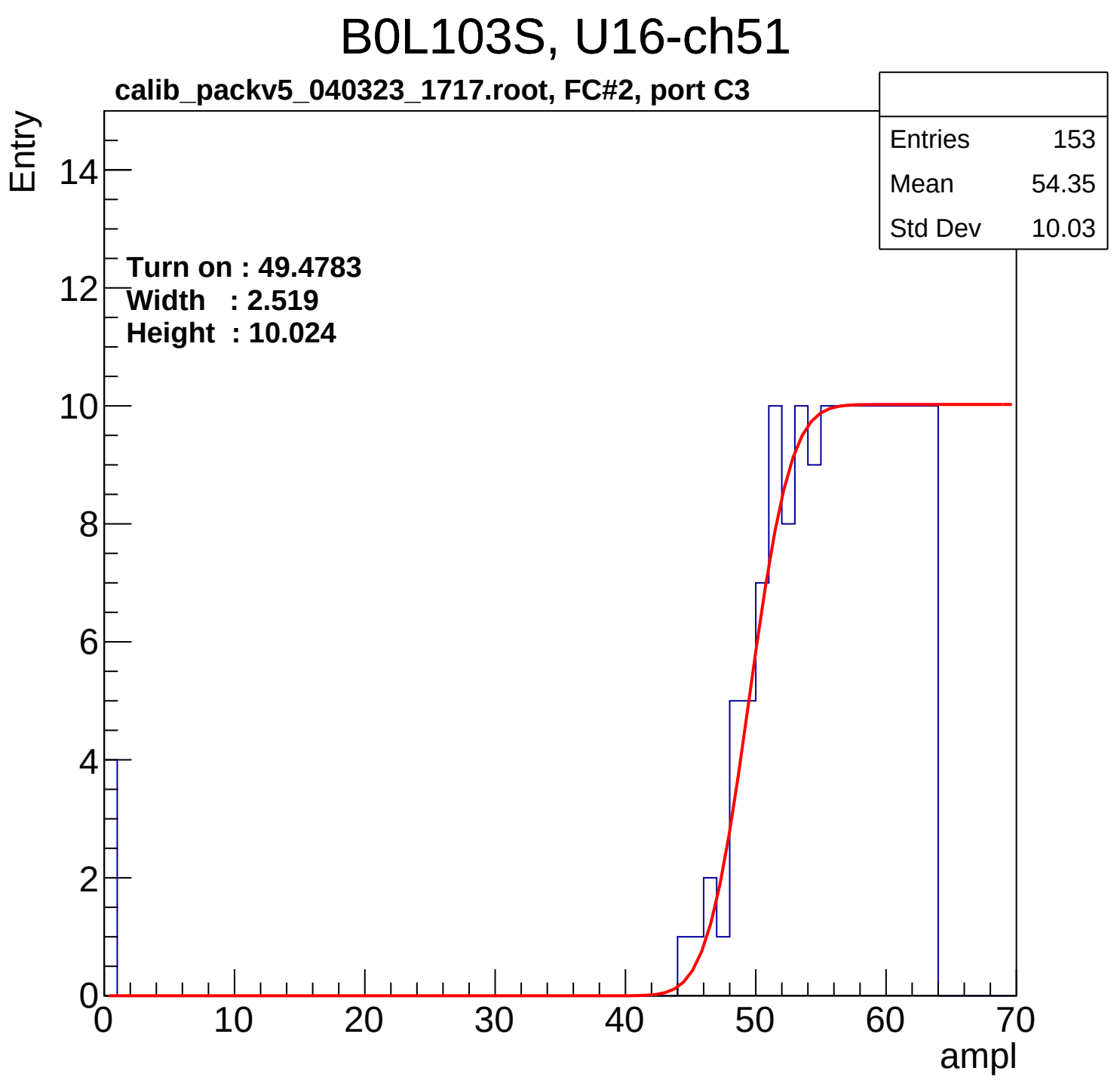
B0L103S, U16-ch51
calib_packv5_040323_1717.root, FC#2, port C3
Entries 153
Mean 54.35
Std Dev 10.03
Turn on : 49.4783
Width : 2.519
Height : 10.024
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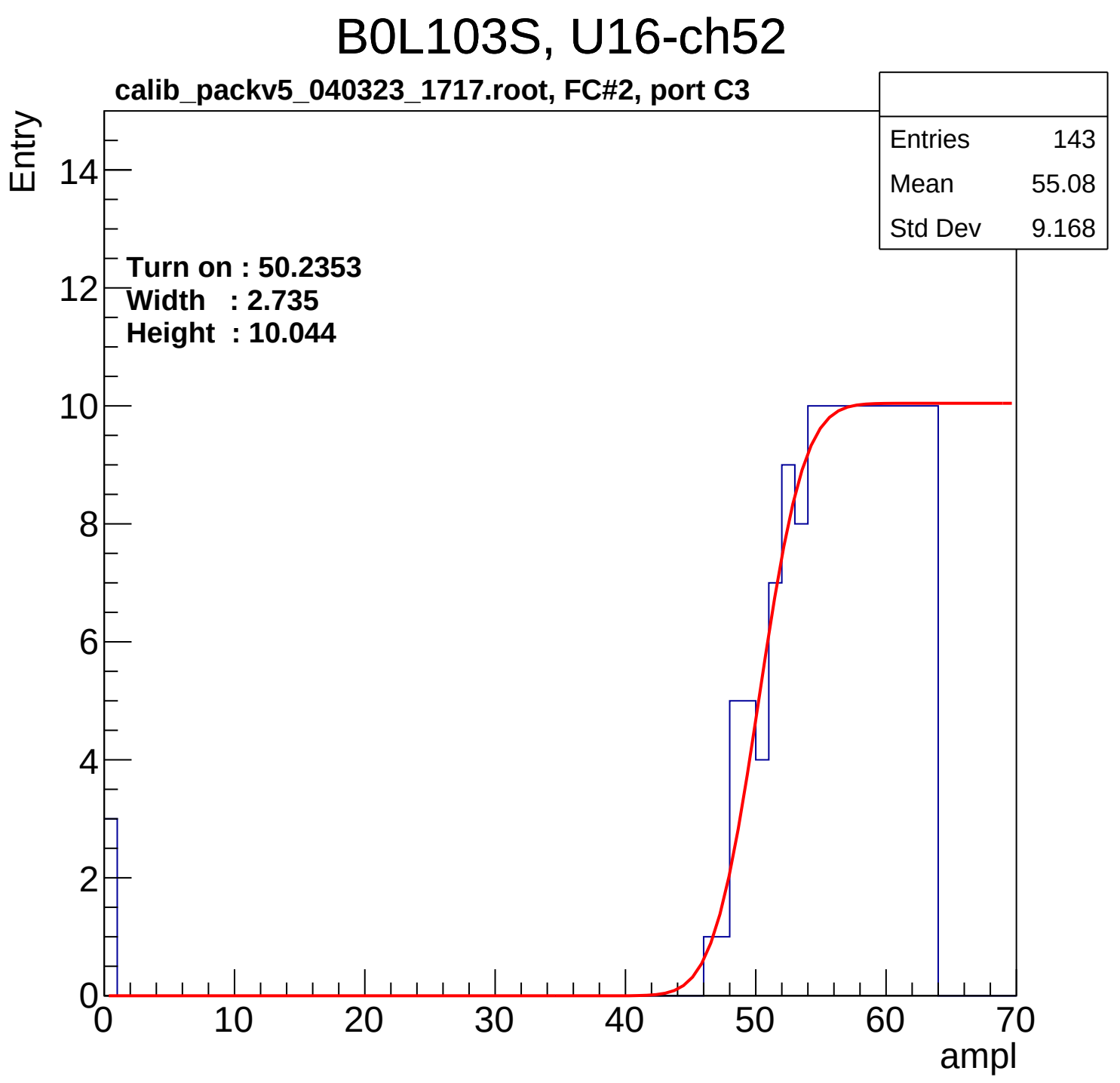
B0L103S, U16-ch52
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 55.08
Std Dev 9.168
Turn on : 50.2353
Width : 2.735
Height : 10.044
Entry
ampl
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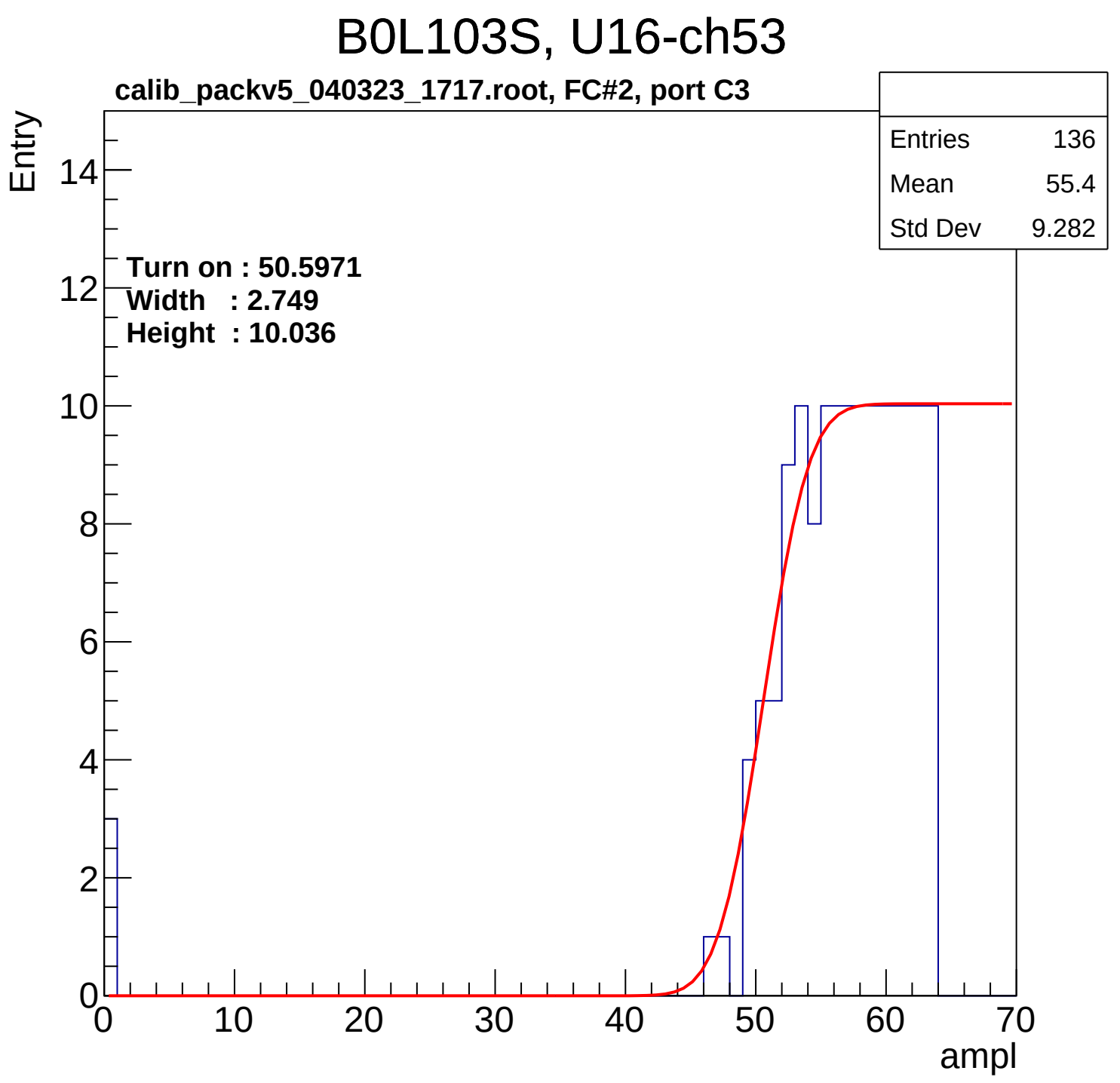
B0L103S, U16-ch53
calib_packv5_040323_1717.root, FC#2, port C3
Entries 136
Mean 55.4
Std Dev 9.282
Turn on : 50.5971
Width : 2.749
Height : 10.036
Entry
ampl
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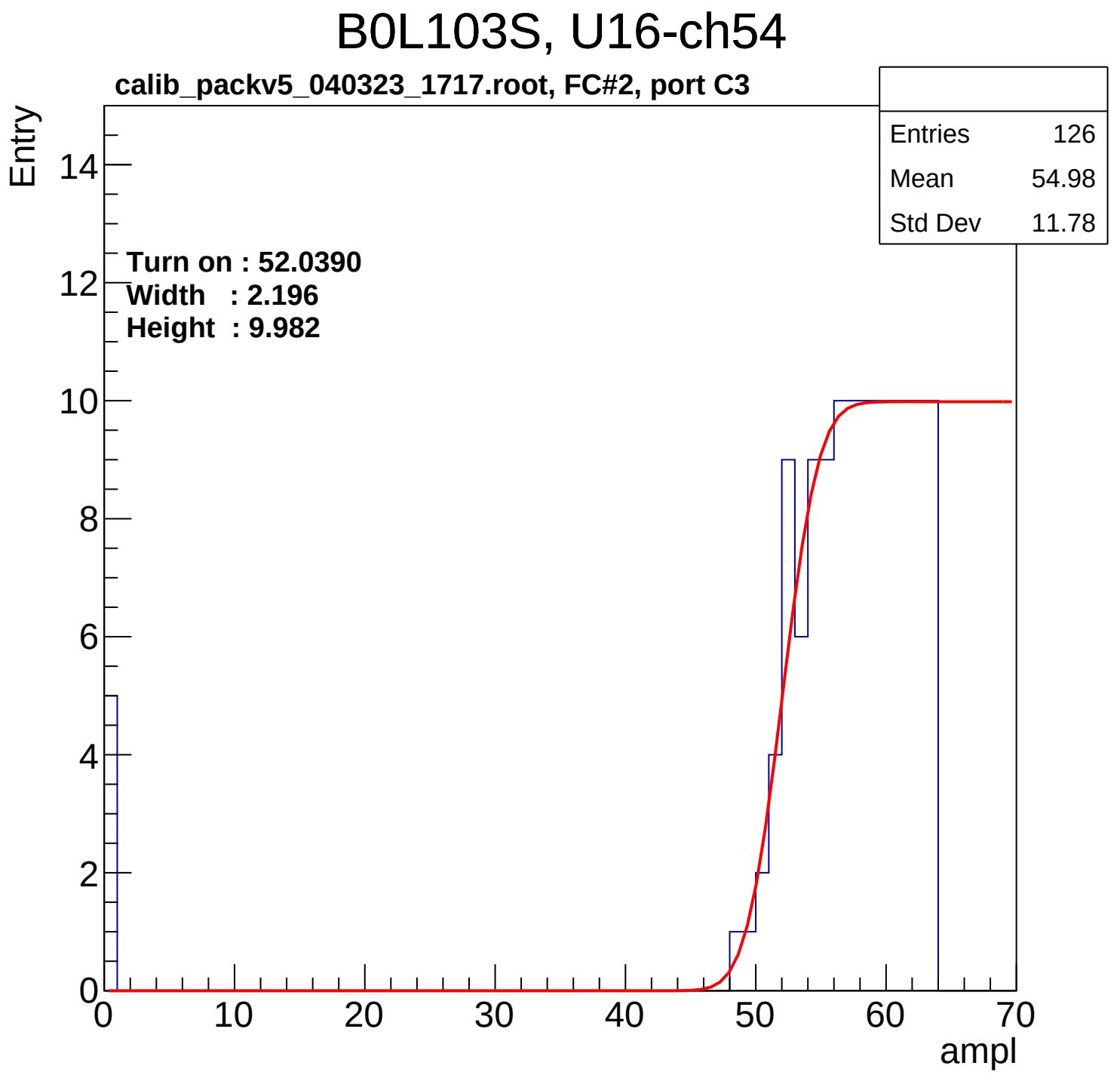
B0L103S, U16-ch54
calib_packv5_040323_1717.root, FC#2, port C3
Entries 126
Mean 54.98
Std Dev 11.78
Turn on : 52.0390
Width : 2.196
Height : 9.982
Entry
ampl
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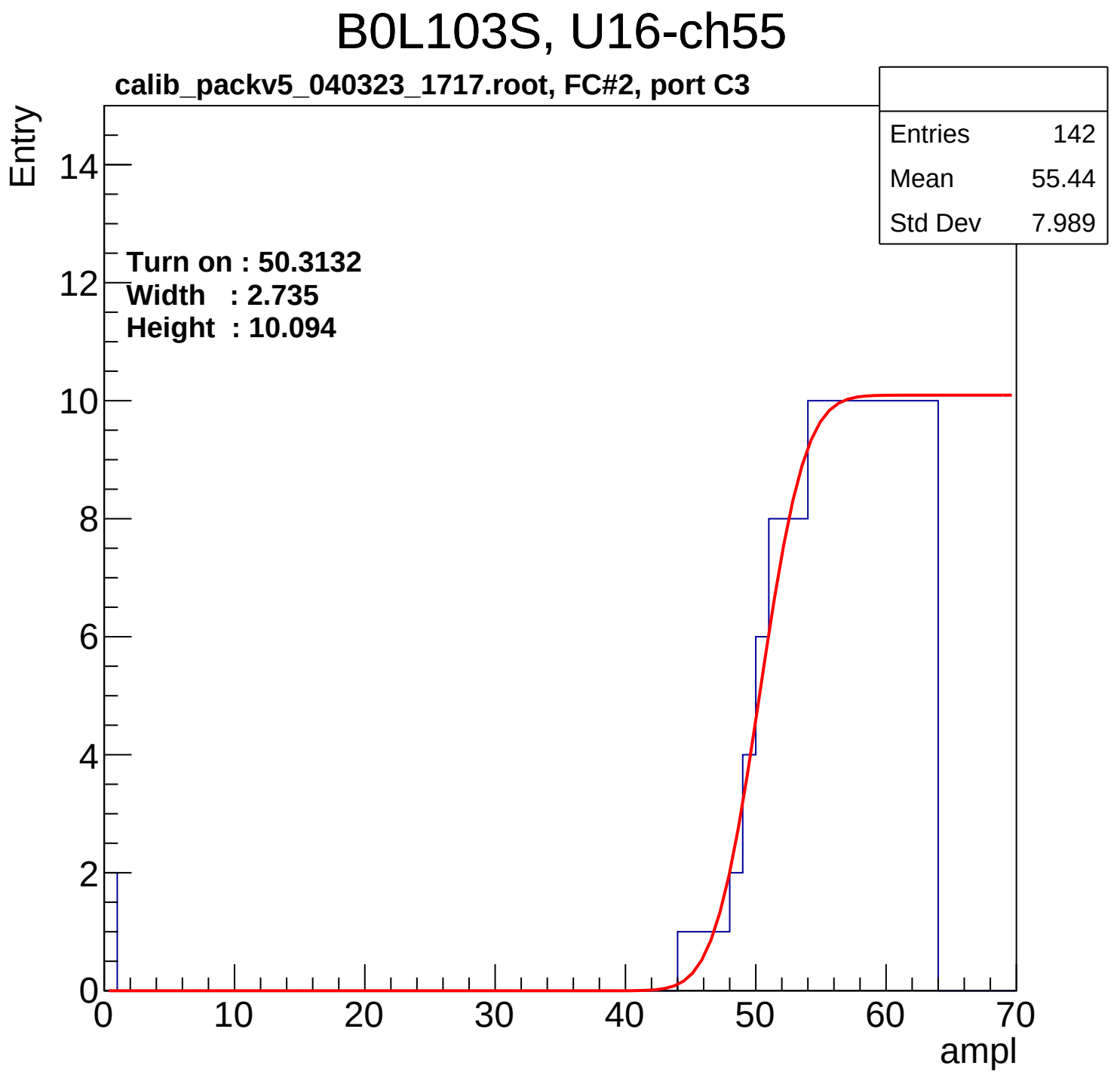
B0L103S, U16-ch55
calib_packv5_040323_1717.root, FC#2, port C3
Entries 142
Mean 55.44
Std Dev 7.989
Turn on : 50.3132
Width : 2.735
Height : 10.094
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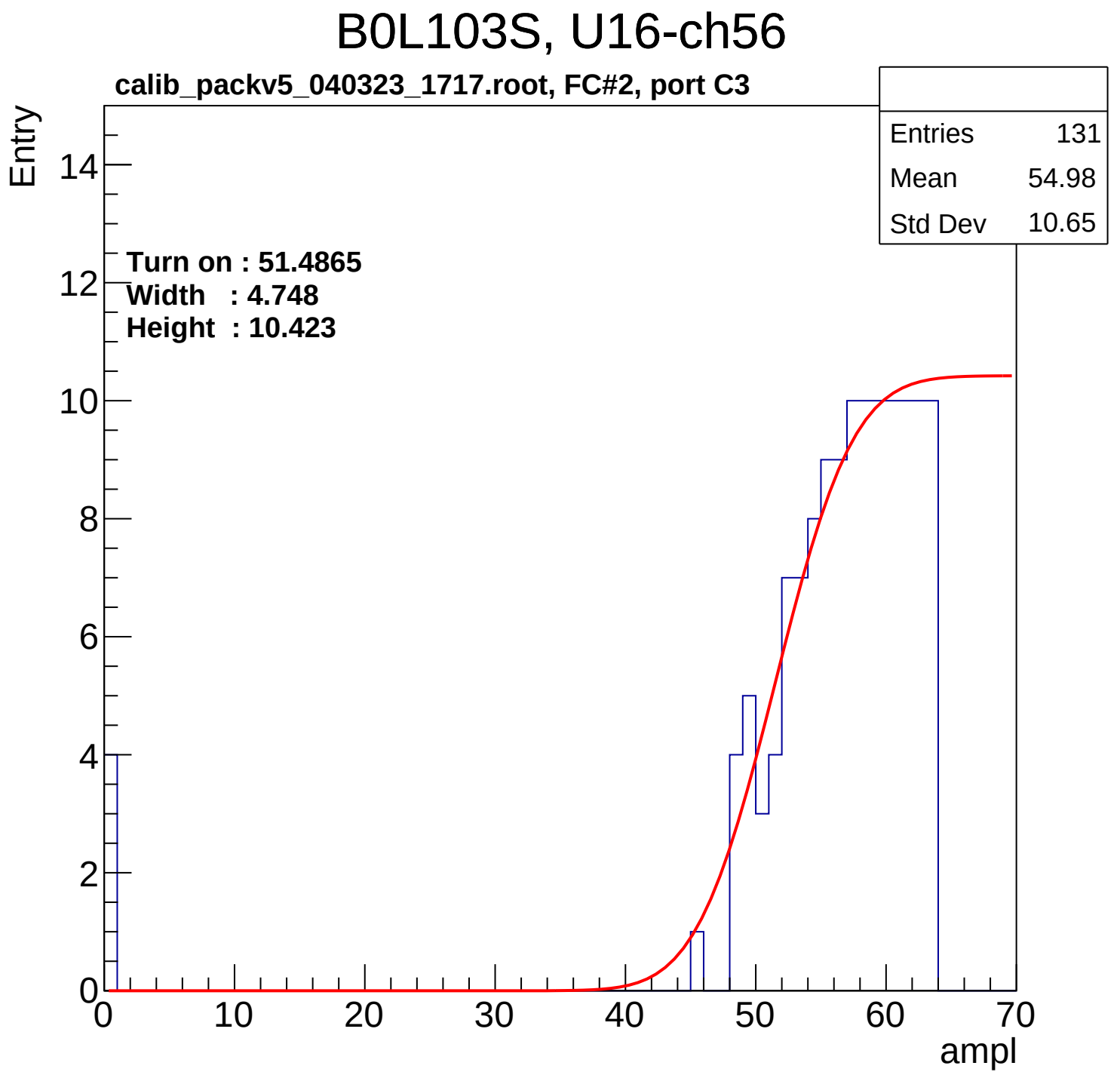
B0L103S, U16-ch56
calib_packv5_040323_1717.root, FC#2, port C3
Entries 131
Mean 54.98
Std Dev 10.65
Turn on : 51.4865
Width : 4.748
Height : 10.423
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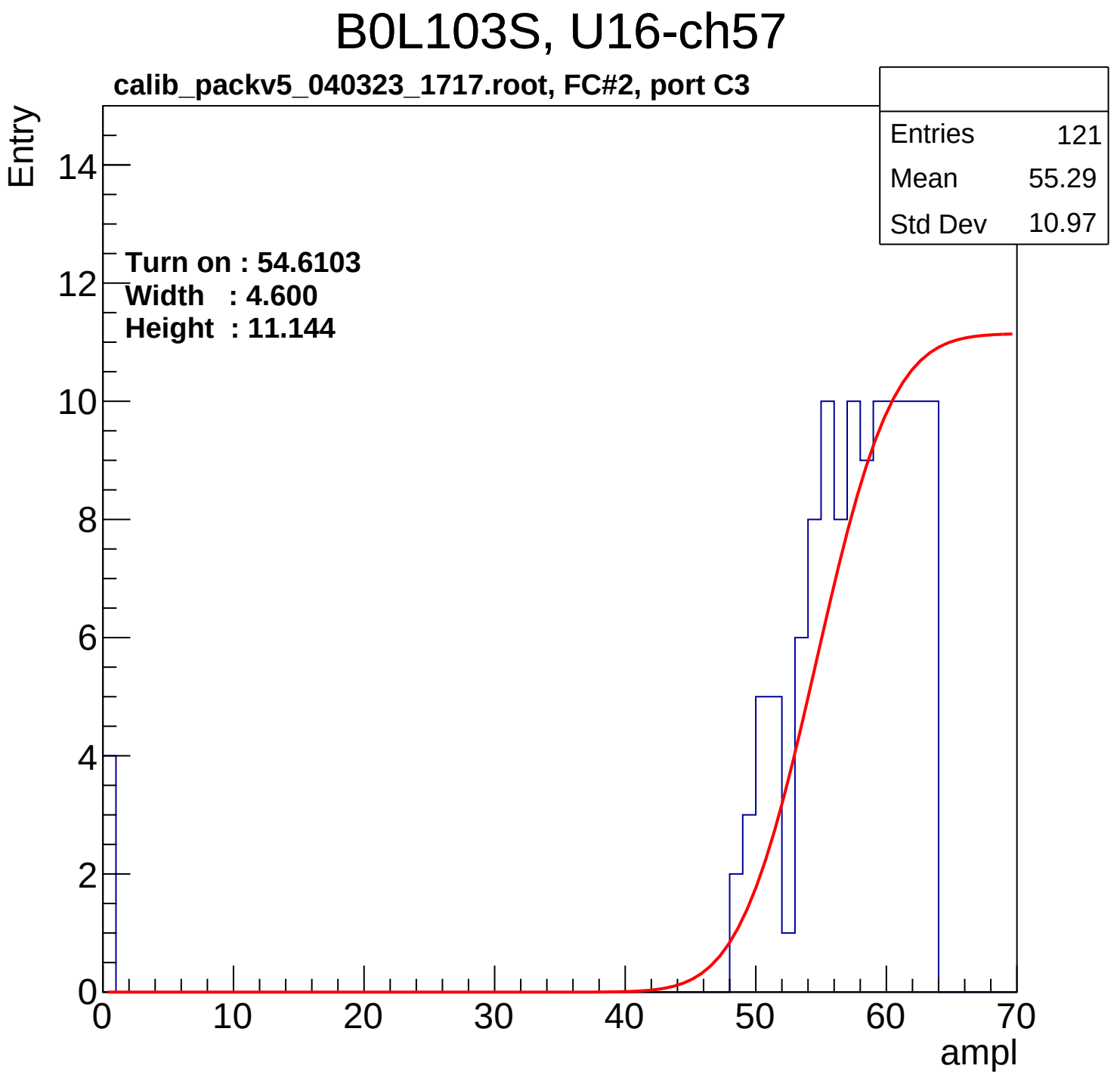
B0L103S, U16-ch57
calib_packv5_040323_1717.root, FC#2, port C3
Entries 121
Mean 55.29
Std Dev 10.97
Turn on : 54.6103
Width : 4.600
Height : 11.144
Entry
ampl
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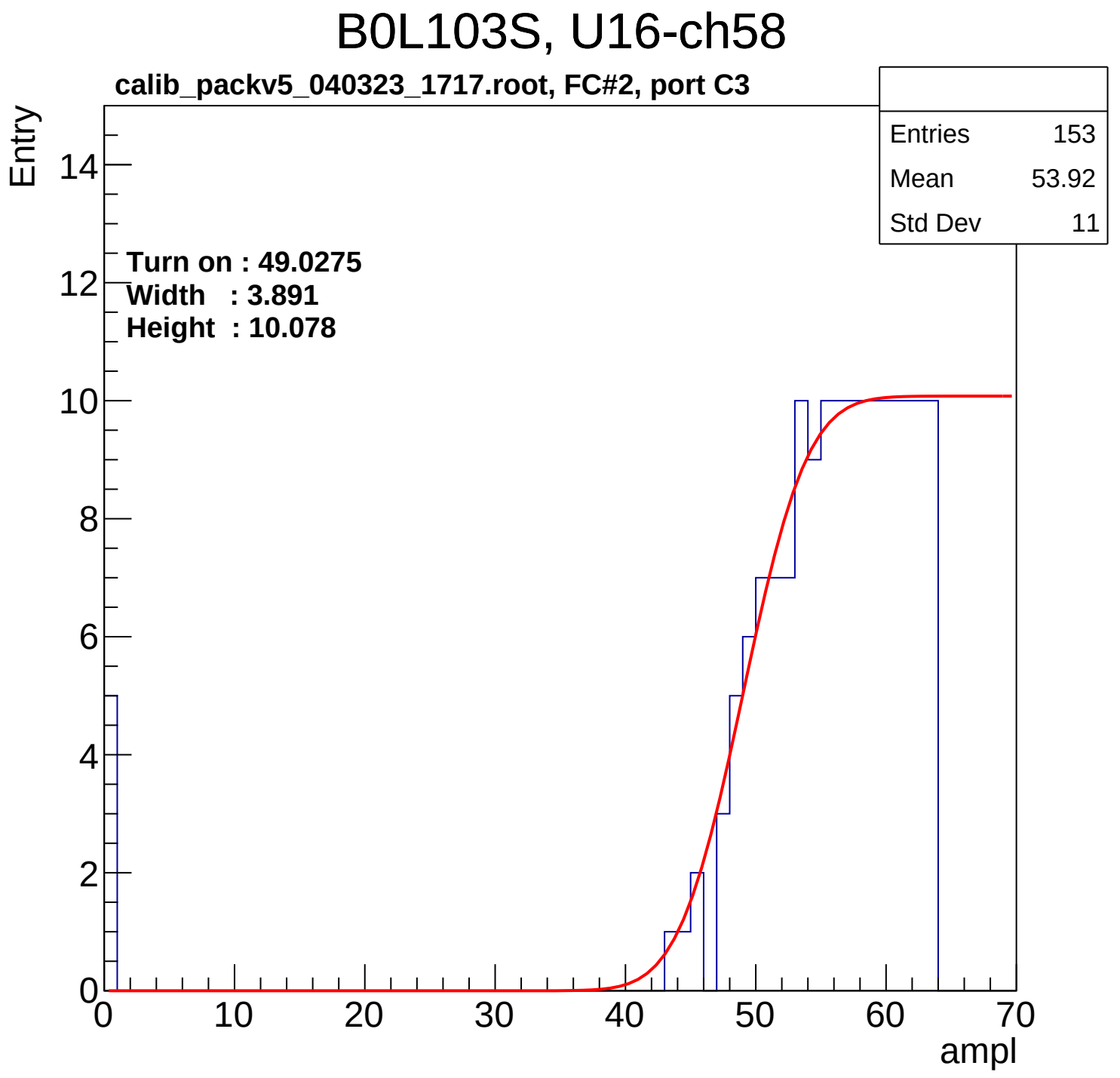
B0L103S, U16-ch58
calib_packv5_040323_1717.root, FC#2, port C3
Entries 153
Mean 53.92
Std Dev 11
Turn on : 49.0275
Width : 3.891
Height : 10.078
Entry
ampl
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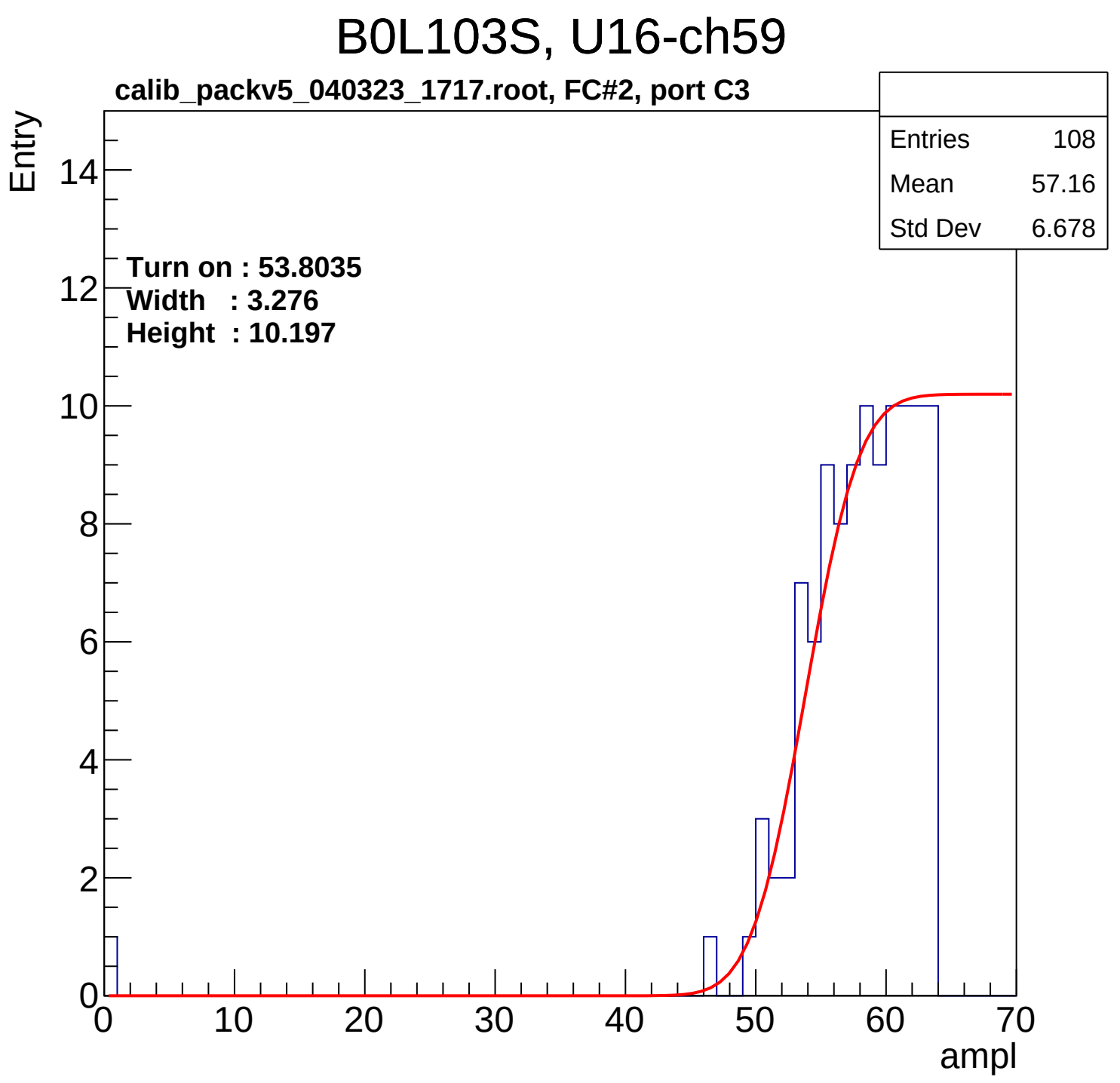
B0L103S, U16-ch59
calib_packv5_040323_1717.root, FC#2, port C3
Entries 108
Mean 57.16
Std Dev 6.678
Turn on : 53.8035
Width : 3.276
Height : 10.197
Entry
ampl
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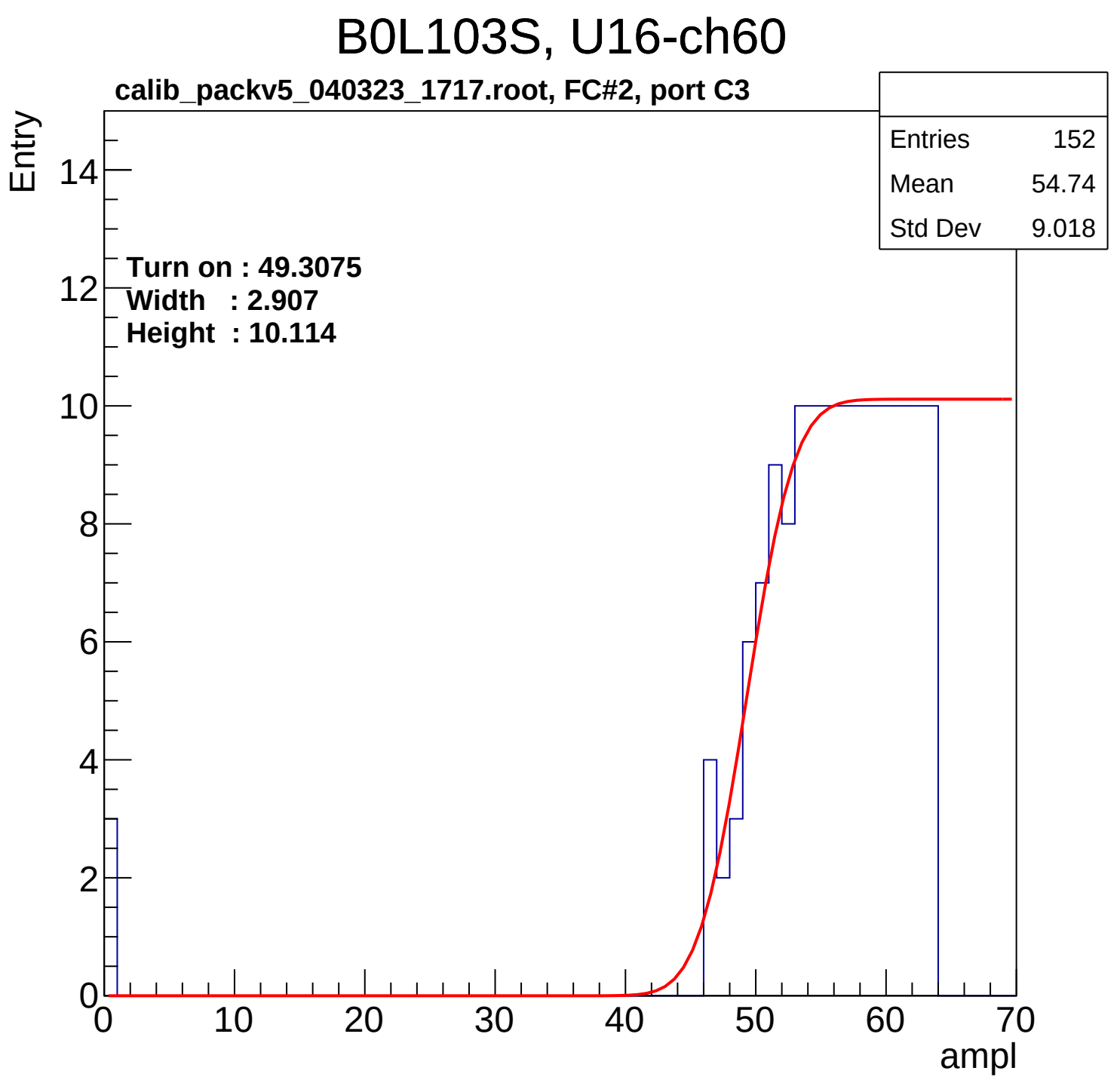
B0L103S, U16-ch60
calib_packv5_040323_1717.root, FC#2, port C3
Entries 152
Mean 54.74
Std Dev 9.018
Turn on : 49.3075
Width : 2.907
Height : 10.114
Entry
ampl
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4
6
8
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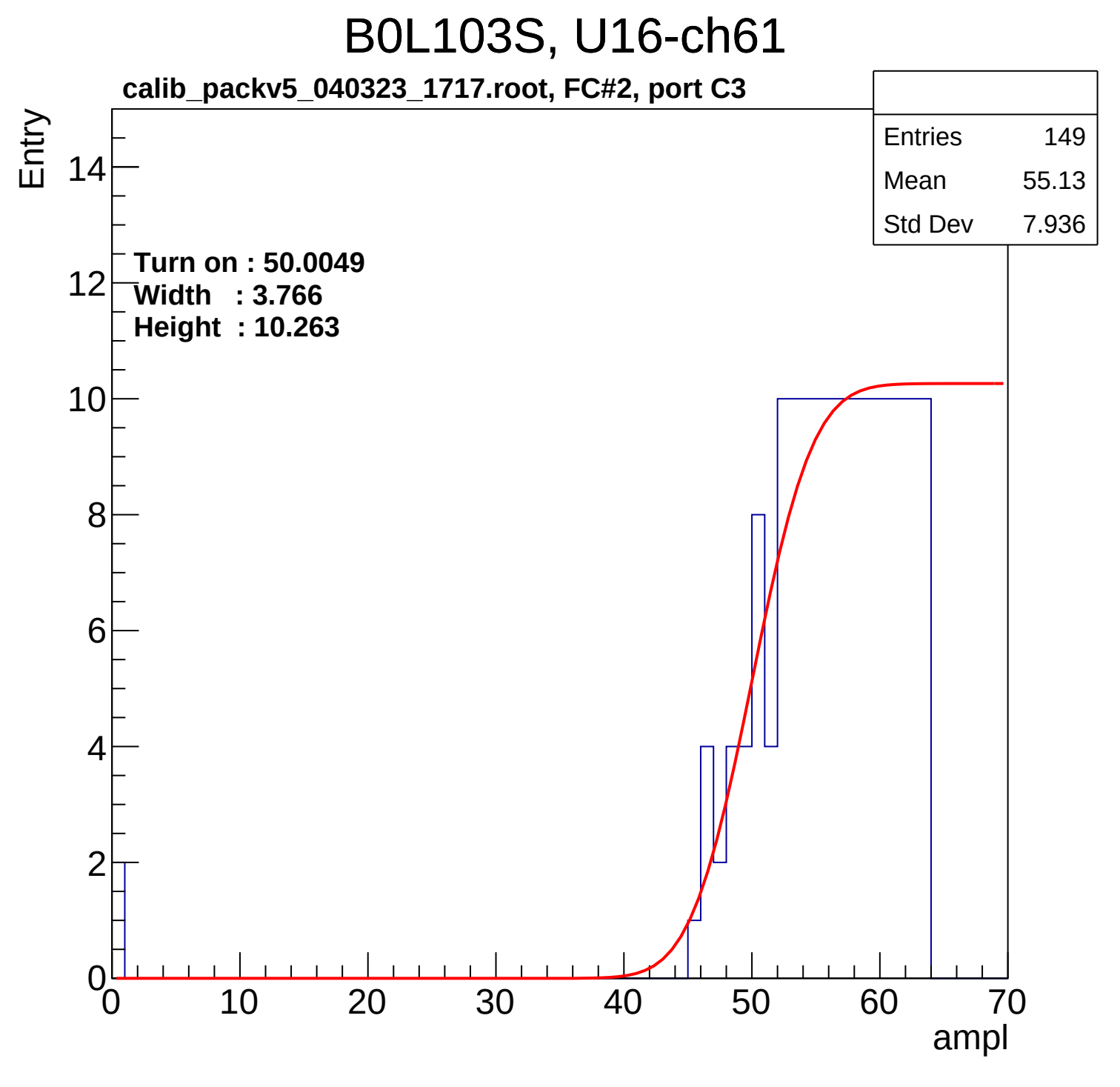
B0L103S, U16-ch61
calib_packv5_040323_1717.root, FC#2, port C3
Entries 149
Mean 55.13
Std Dev 7.936
Turn on : 50.0049
Width : 3.766
Height : 10.263
Entry
ampl
0
2
4
6
8
10
12
14
0
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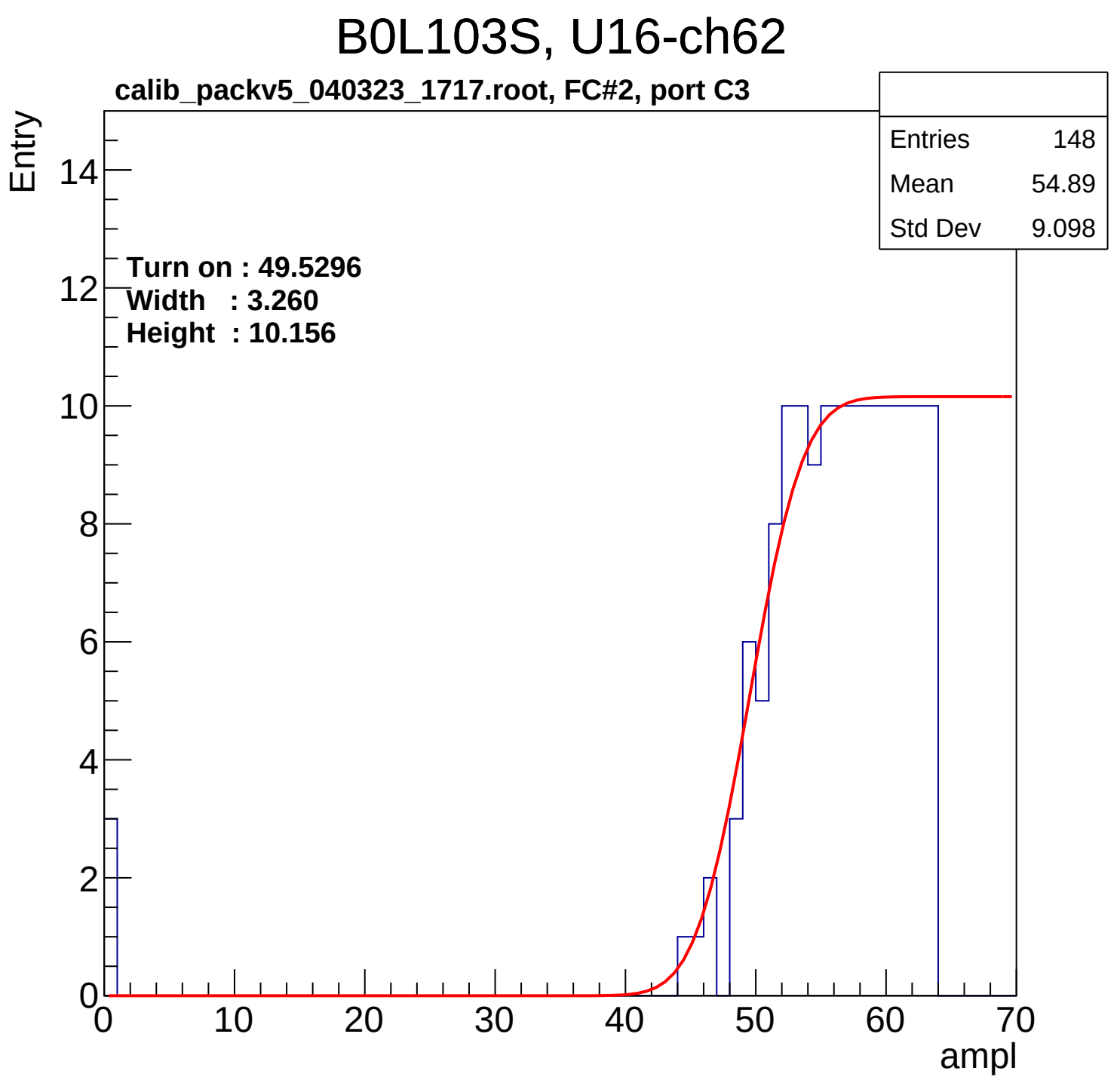
B0L103S, U16-ch62
calib_packv5_040323_1717.root, FC#2, port C3
Entries 148
Mean 54.89
Std Dev 9.098
Turn on : 49.5296
Width : 3.260
Height : 10.156
Entry
ampl
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2
4
6
8
10
12
14
0
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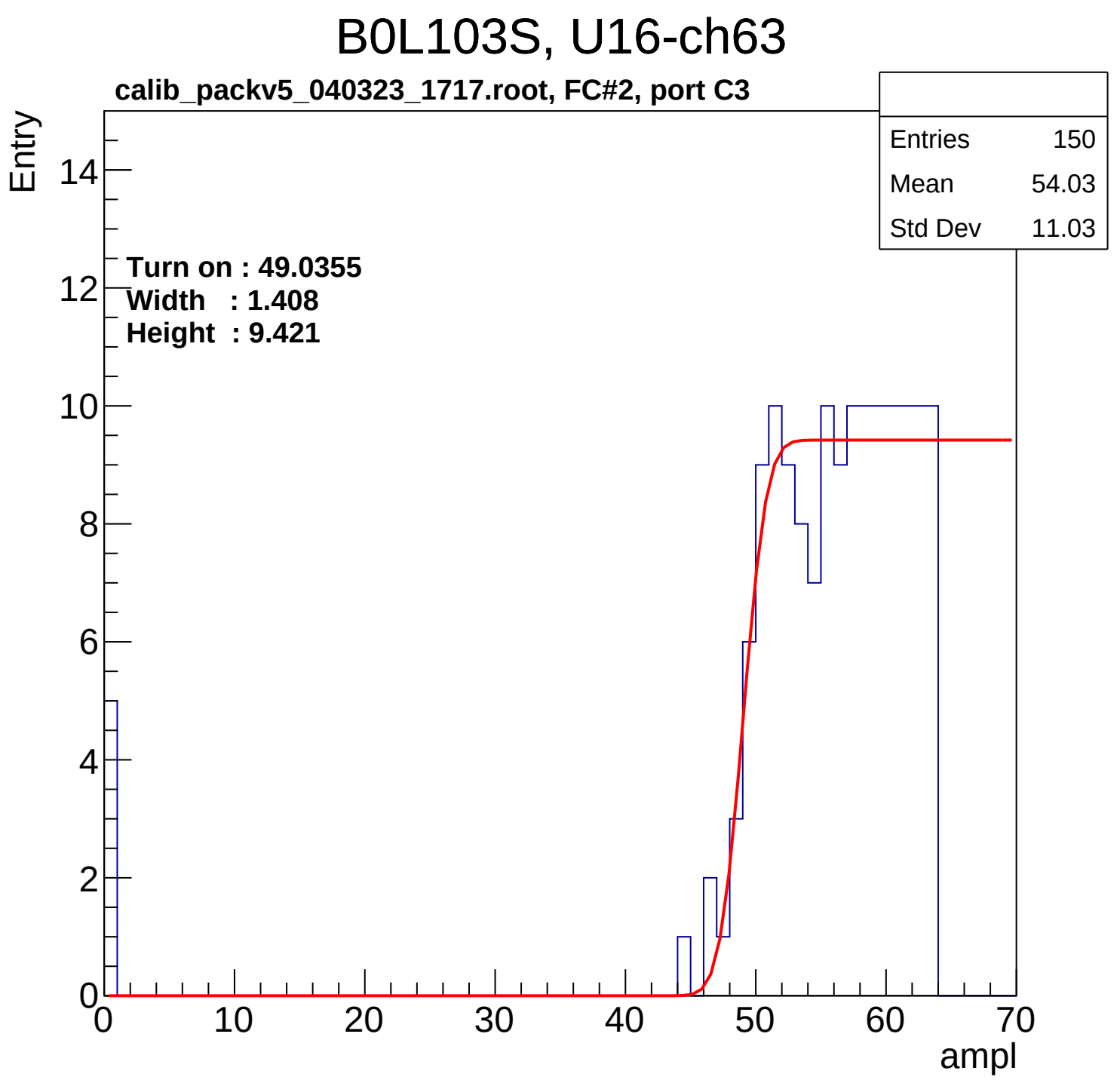
B0L103S, U16-ch63
calib_packv5_040323_1717.root, FC#2, port C3
Entries 150
Mean 54.03
Std Dev 11.03
Turn on : 49.0355
Width : 1.408
Height : 9.421
Entry
ampl
0
2
4
6
8
10
12
14
0
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40
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60
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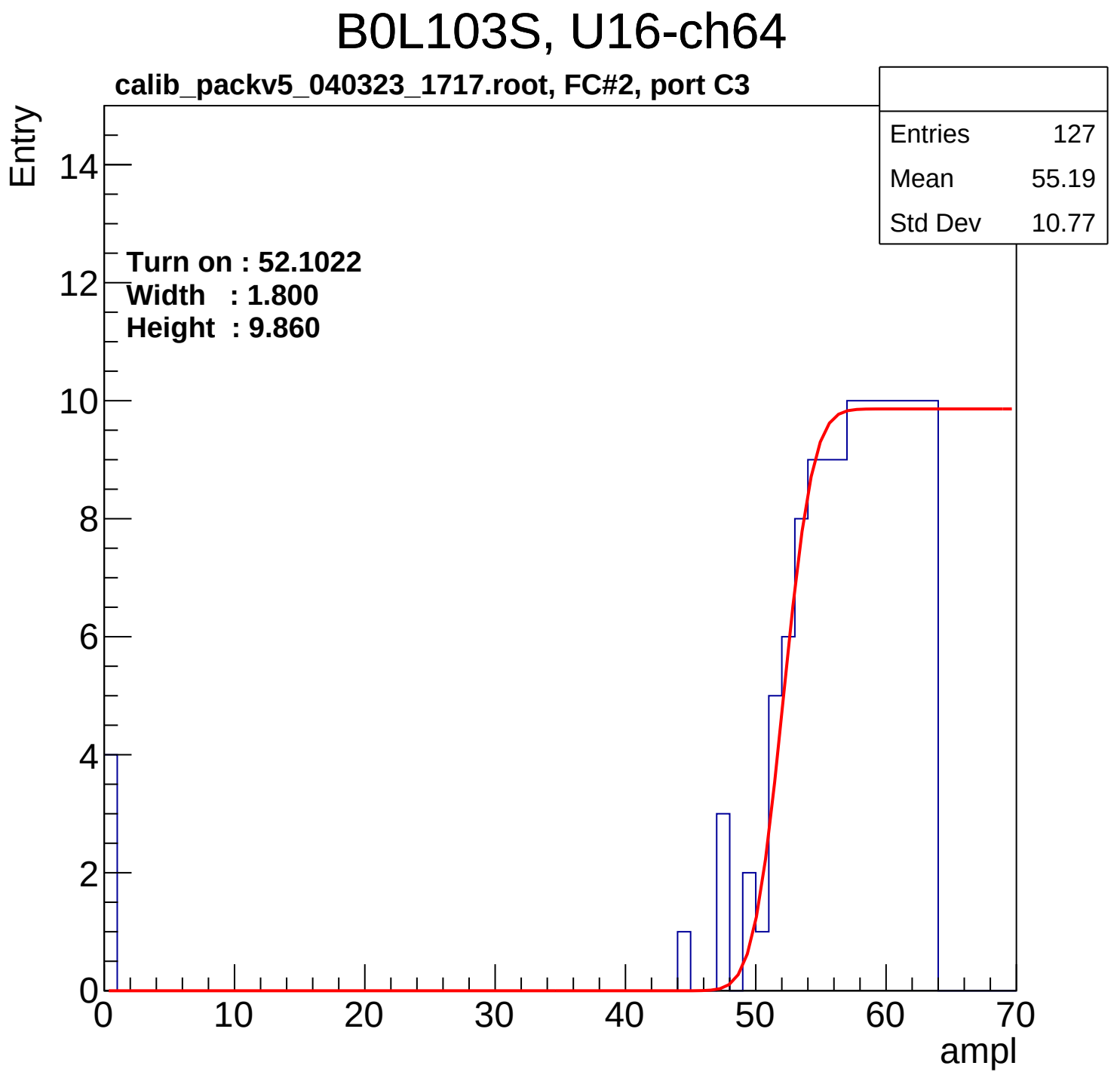
B0L103S, U16-ch64
calib_packv5_040323_1717.root, FC#2, port C3
Entries 127
Mean 55.19
Std Dev 10.77
Turn on : 52.1022
Width : 1.800
Height : 9.860
Entry
ampl
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4
6
8
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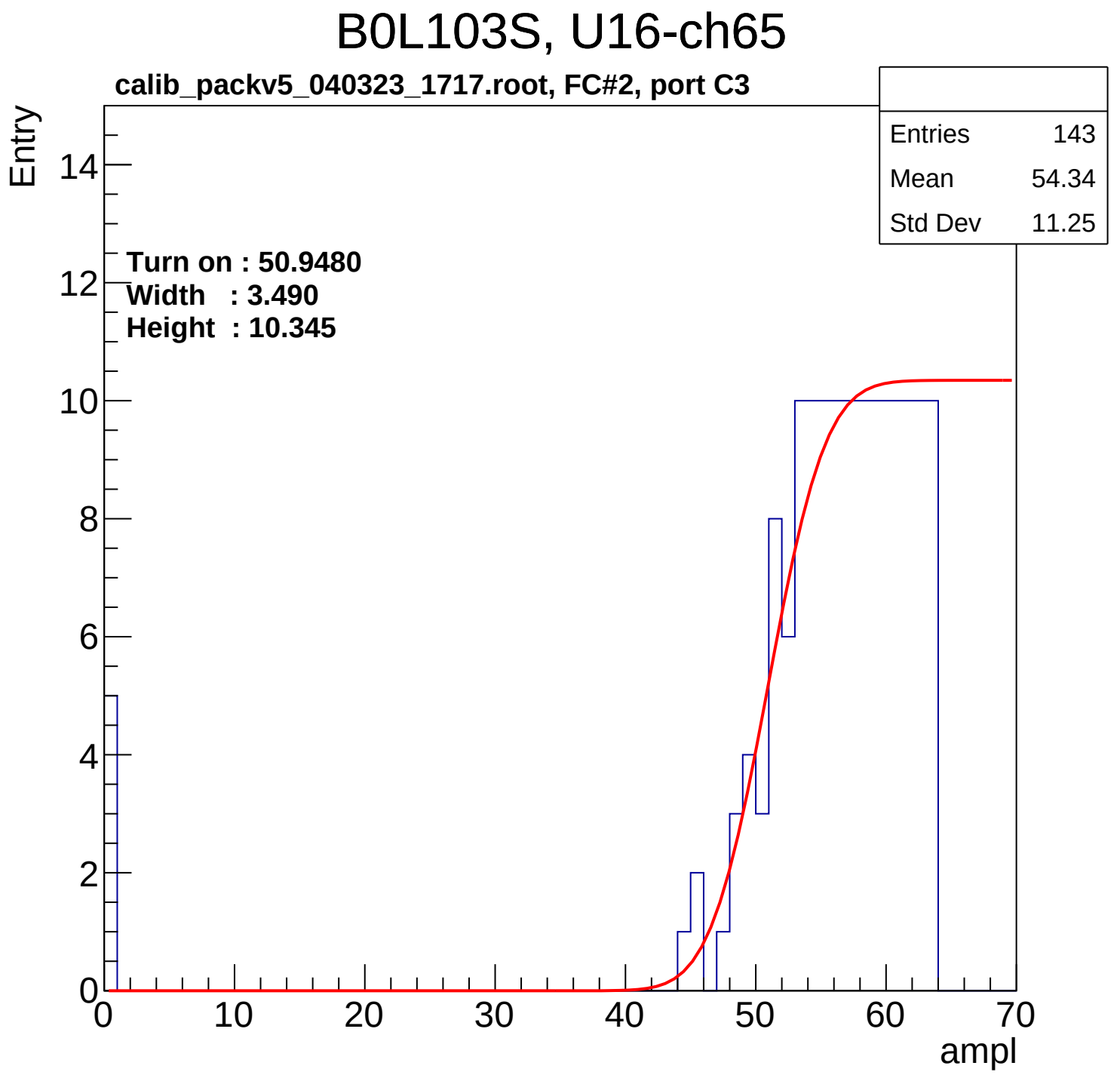
B0L103S, U16-ch65
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 54.34
Std Dev 11.25
Turn on : 50.9480
Width : 3.490
Height : 10.345
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
50
60
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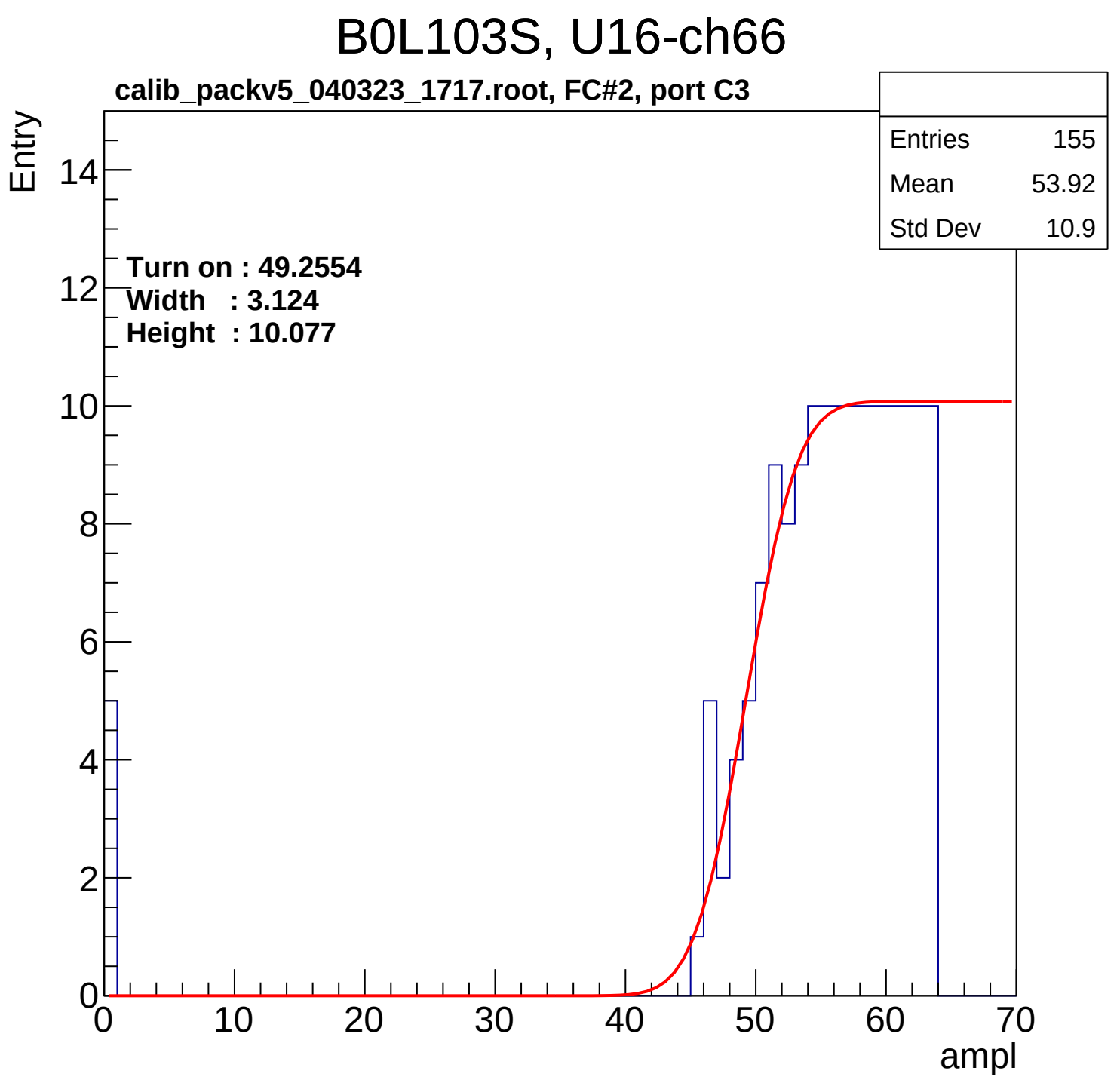
B0L103S, U16-ch66
calib_packv5_040323_1717.root, FC#2, port C3
Entries 155
Mean 53.92
Std Dev 10.9
Turn on : 49.2554
Width : 3.124
Height : 10.077
Entry
ampl
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4
6
8
10
12
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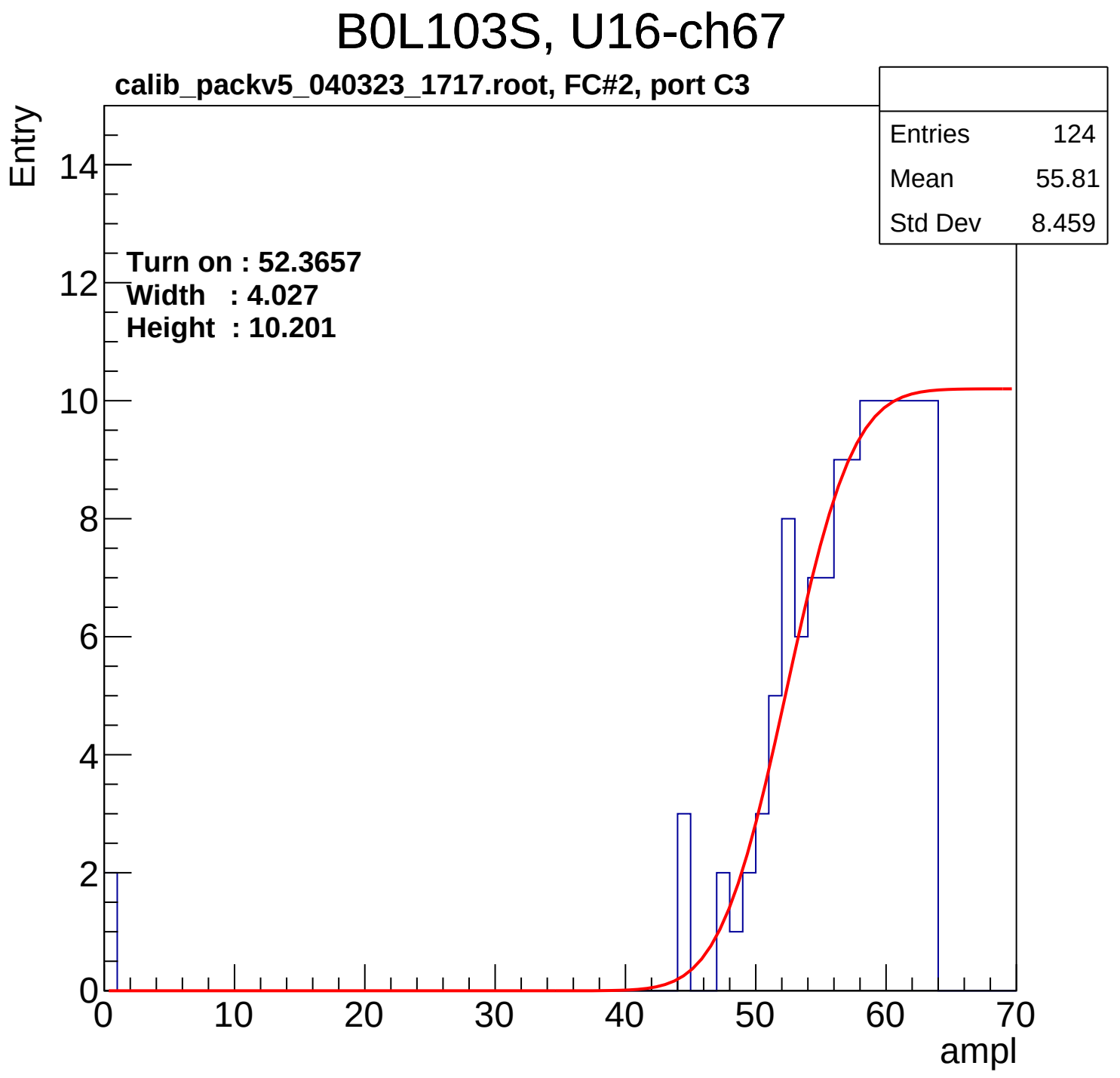
B0L103S, U16-ch67
calib_packv5_040323_1717.root, FC#2, port C3
Entries 124
Mean 55.81
Std Dev 8.459
Turn on : 52.3657
Width : 4.027
Height : 10.201
Entry
ampl
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2
4
6
8
10
12
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60
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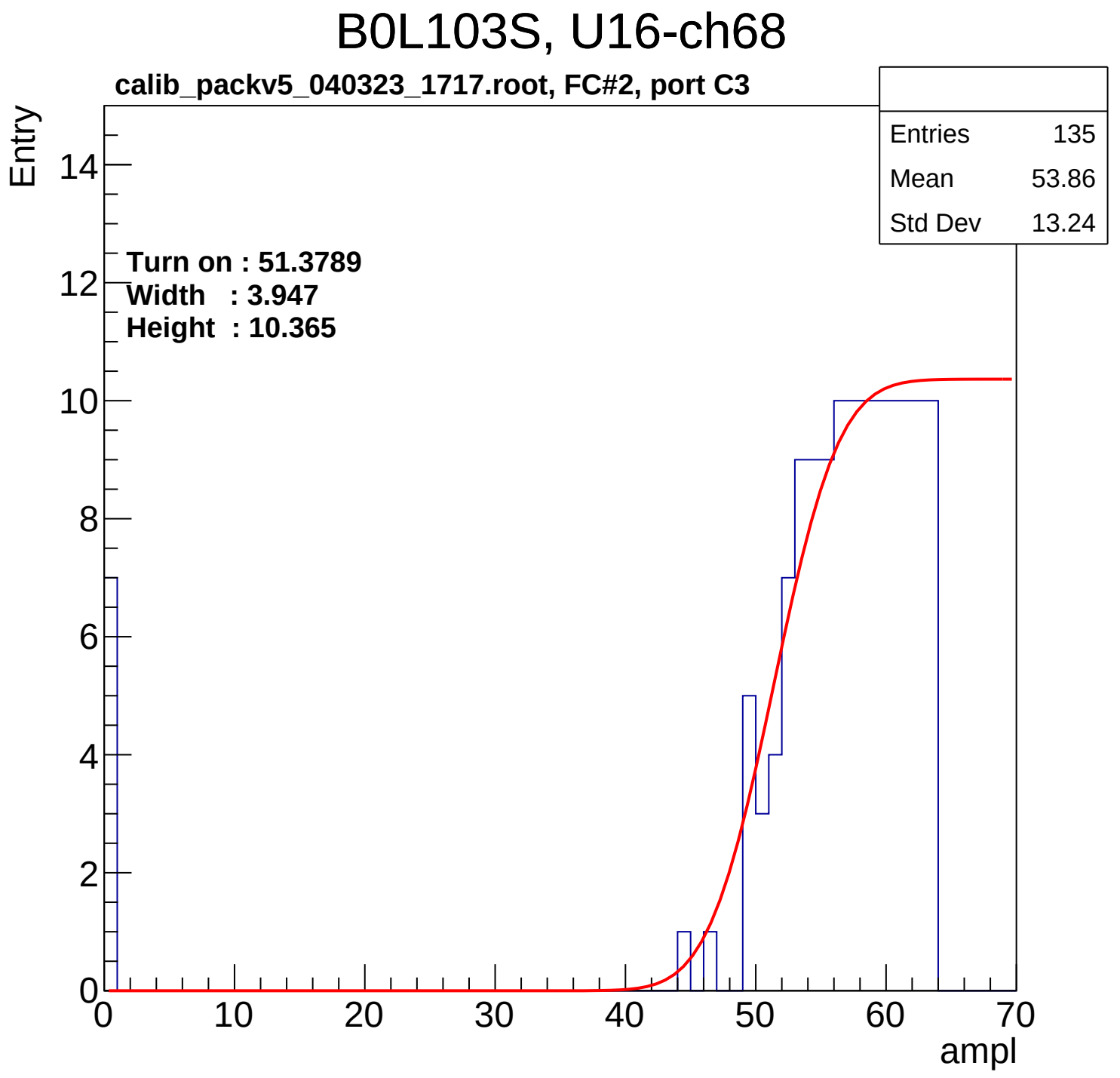
B0L103S, U16-ch68
calib_packv5_040323_1717.root, FC#2, port C3
Entries 135
Mean 53.86
Std Dev 13.24
Turn on : 51.3789
Width : 3.947
Height : 10.365
Entry
ampl
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6
8
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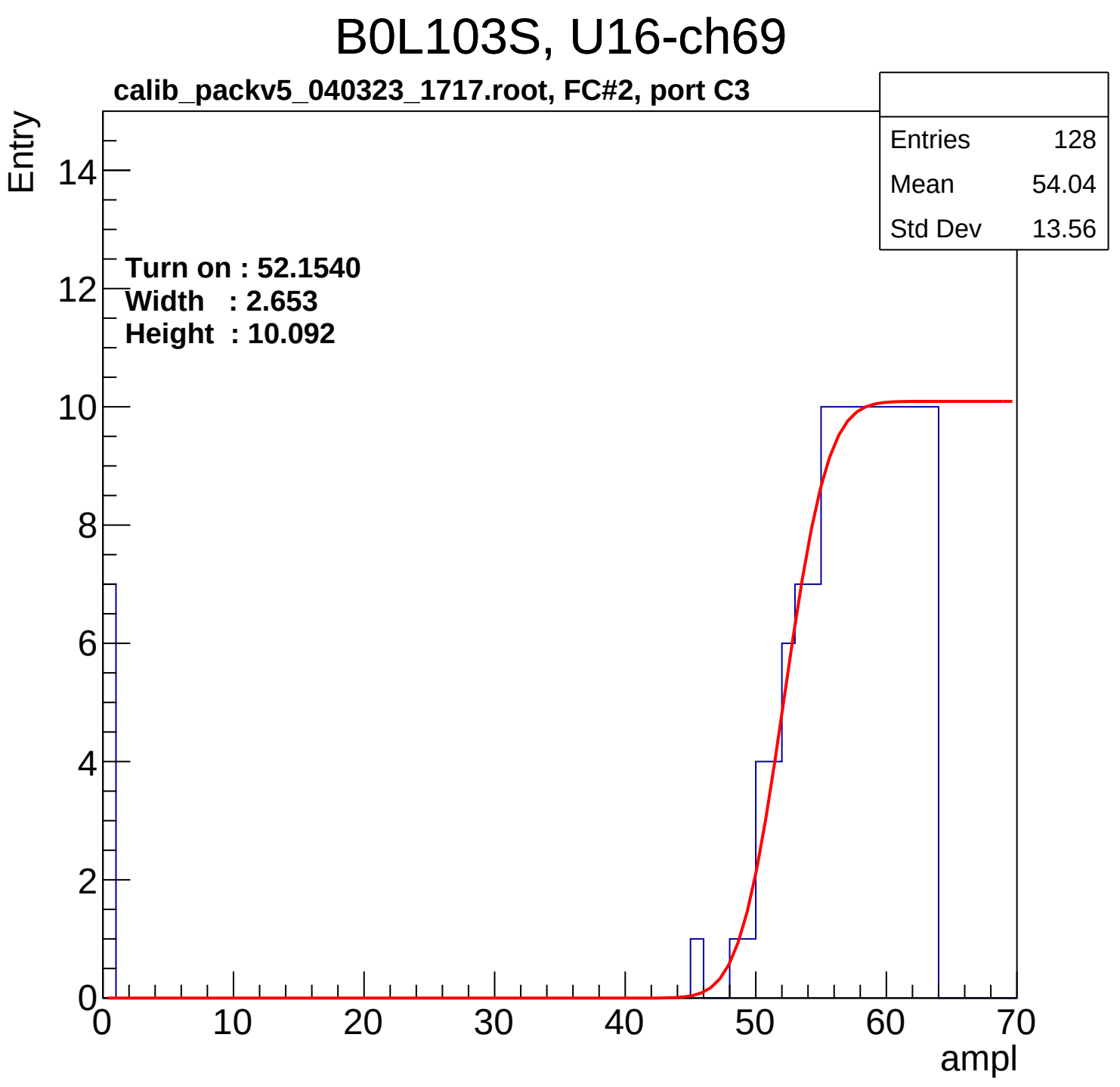
B0L103S, U16-ch69
calib_packv5_040323_1717.root, FC#2, port C3
Entries 128
Mean 54.04
Std Dev 13.56
Turn on : 52.1540
Width : 2.653
Height : 10.092
Entry
ampl
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4
6
8
10
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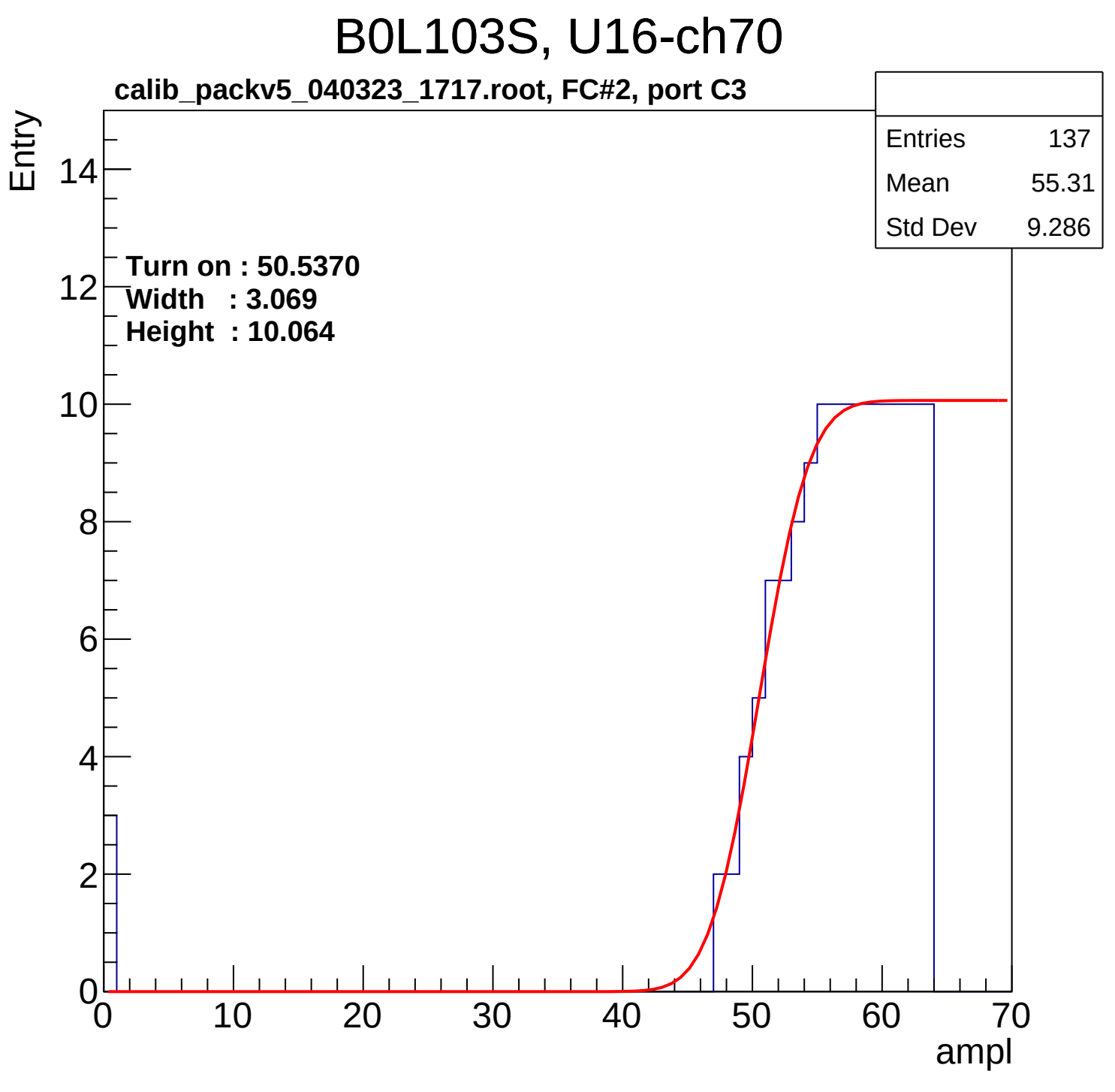
B0L103S, U16-ch70
calib_packv5_040323_1717.root, FC#2, port C3
Entries 137
Mean 55.31
Std Dev 9.286
Turn on : 50.5370
Width : 3.069
Height : 10.064
Entry
ampl
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6
8
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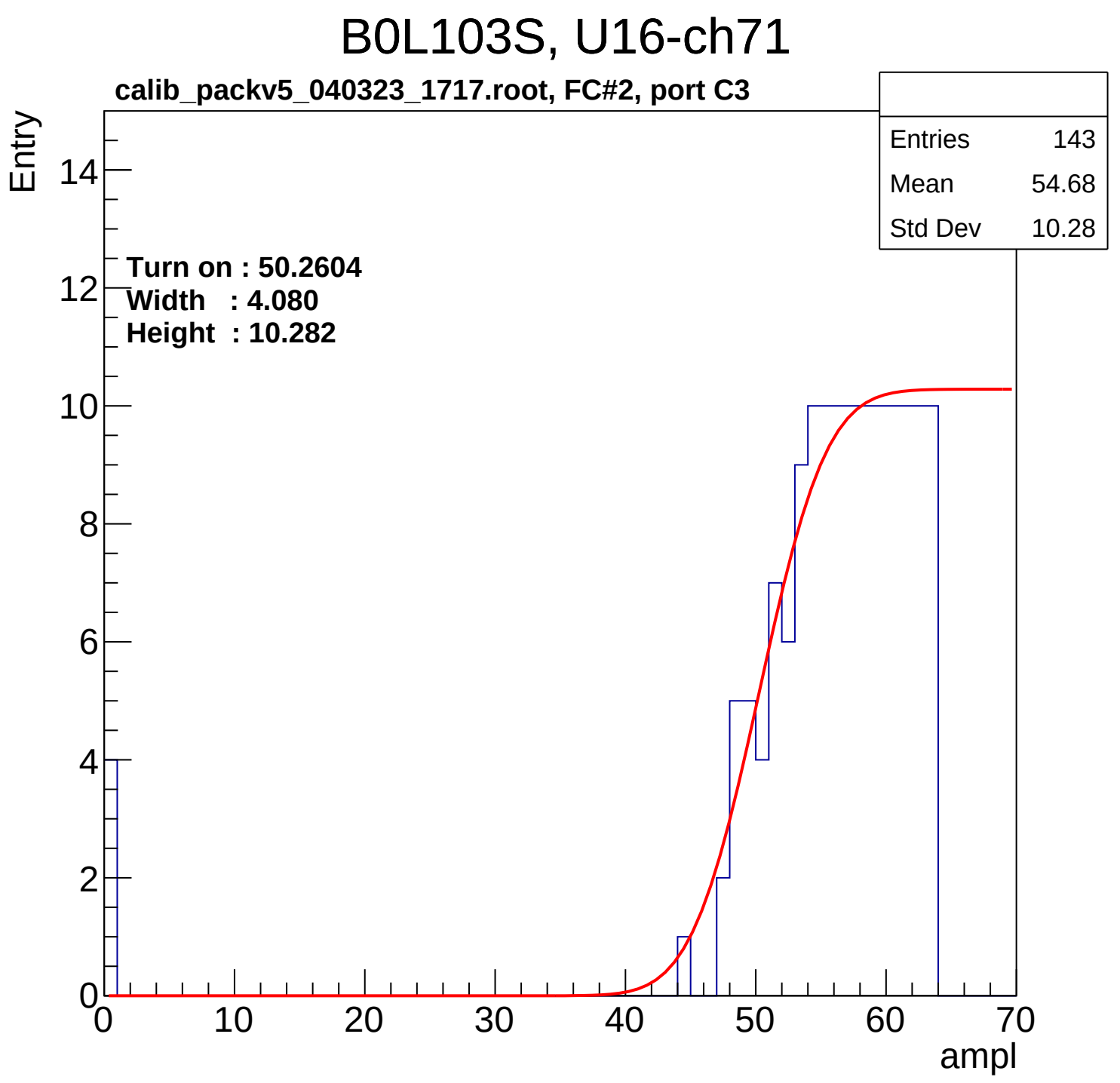
B0L103S, U16-ch71
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 54.68
Std Dev 10.28
Turn on : 50.2604
Width : 4.080
Height : 10.282
Entry
ampl
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6
8
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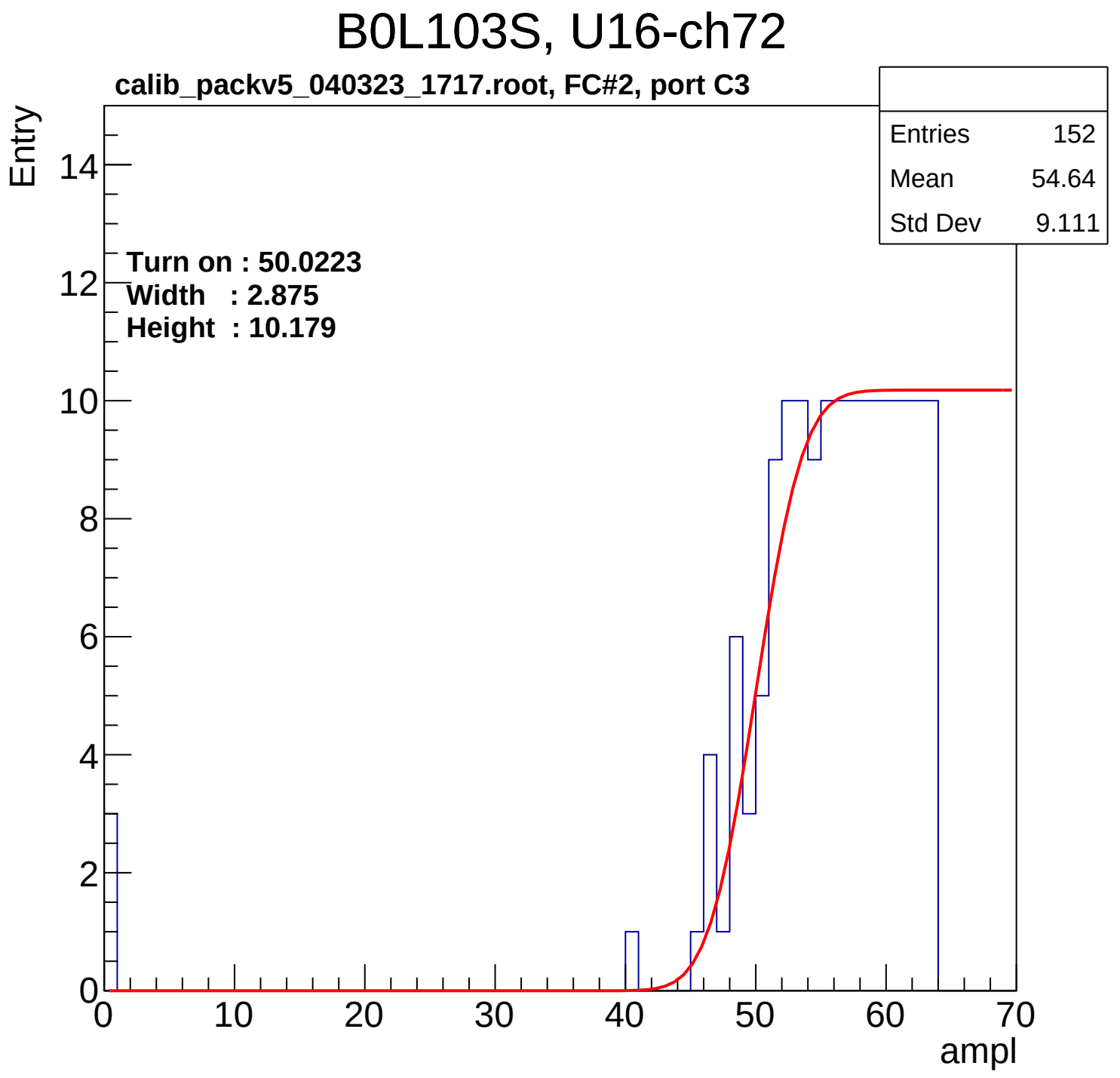
B0L103S, U16-ch72
calib_packv5_040323_1717.root, FC#2, port C3
Entries 152
Mean 54.64
Std Dev 9.111
Turn on : 50.0223
Width : 2.875
Height : 10.179
Entry
ampl
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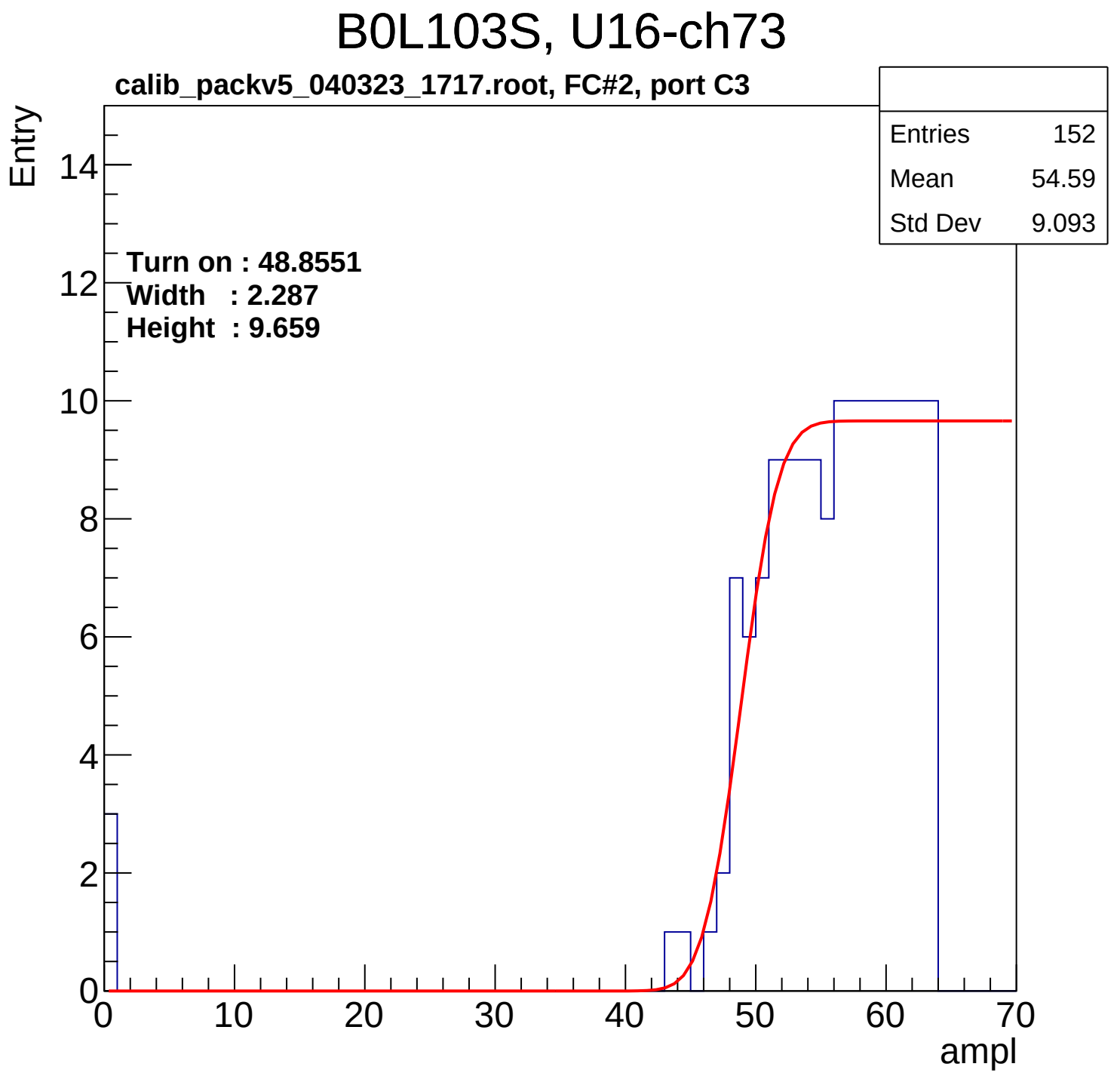
B0L103S, U16-ch73
calib_packv5_040323_1717.root, FC#2, port C3
Entries 152
Mean 54.59
Std Dev 9.093
Turn on : 48.8551
Width : 2.287
Height : 9.659
Entry
ampl
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10
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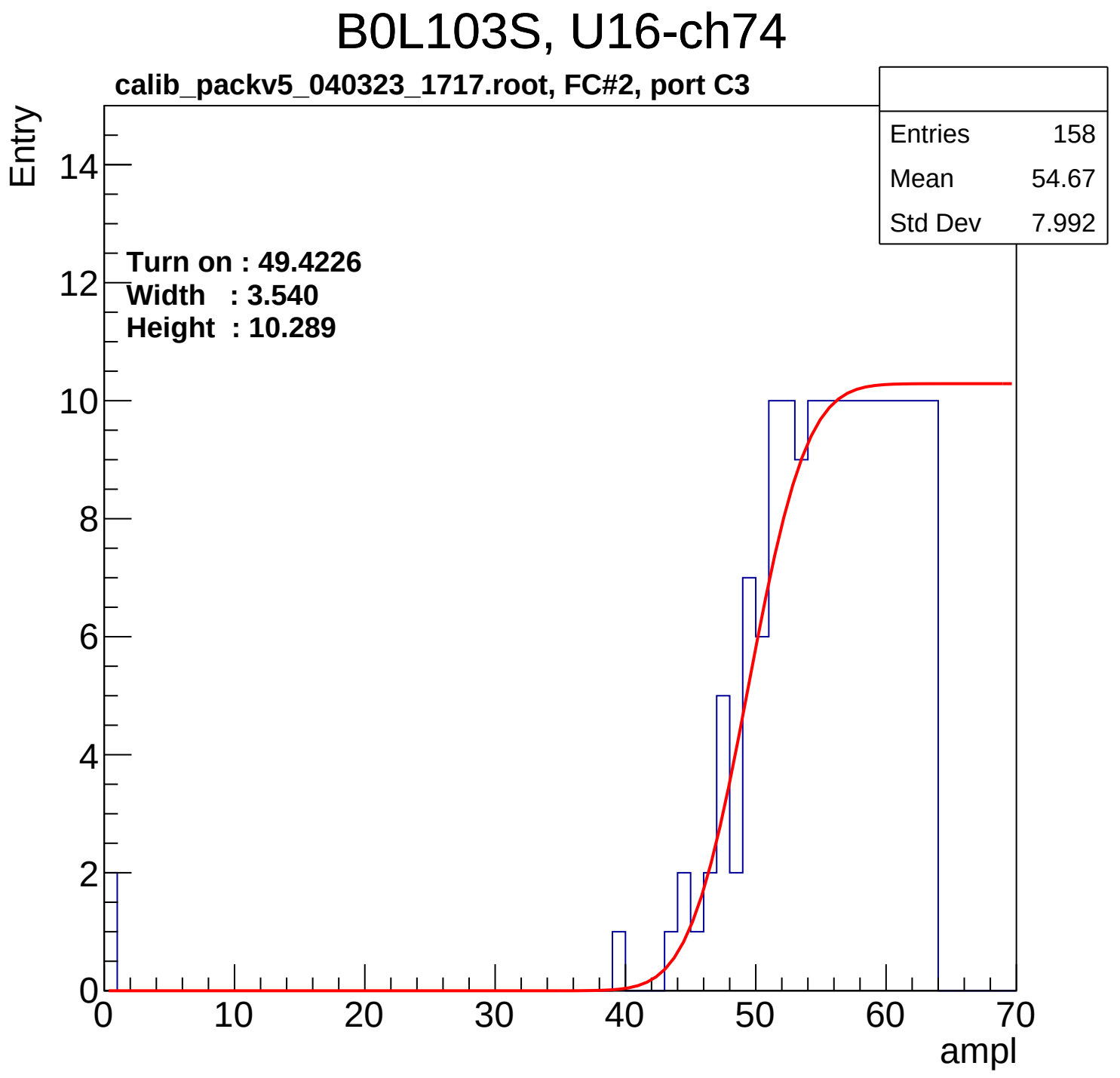
B0L103S, U16-ch74
calib_packv5_040323_1717.root, FC#2, port C3
Entries 158
Mean 54.67
Std Dev 7.992
Turn on : 49.4226
Width : 3.540
Height : 10.289
Entry
ampl
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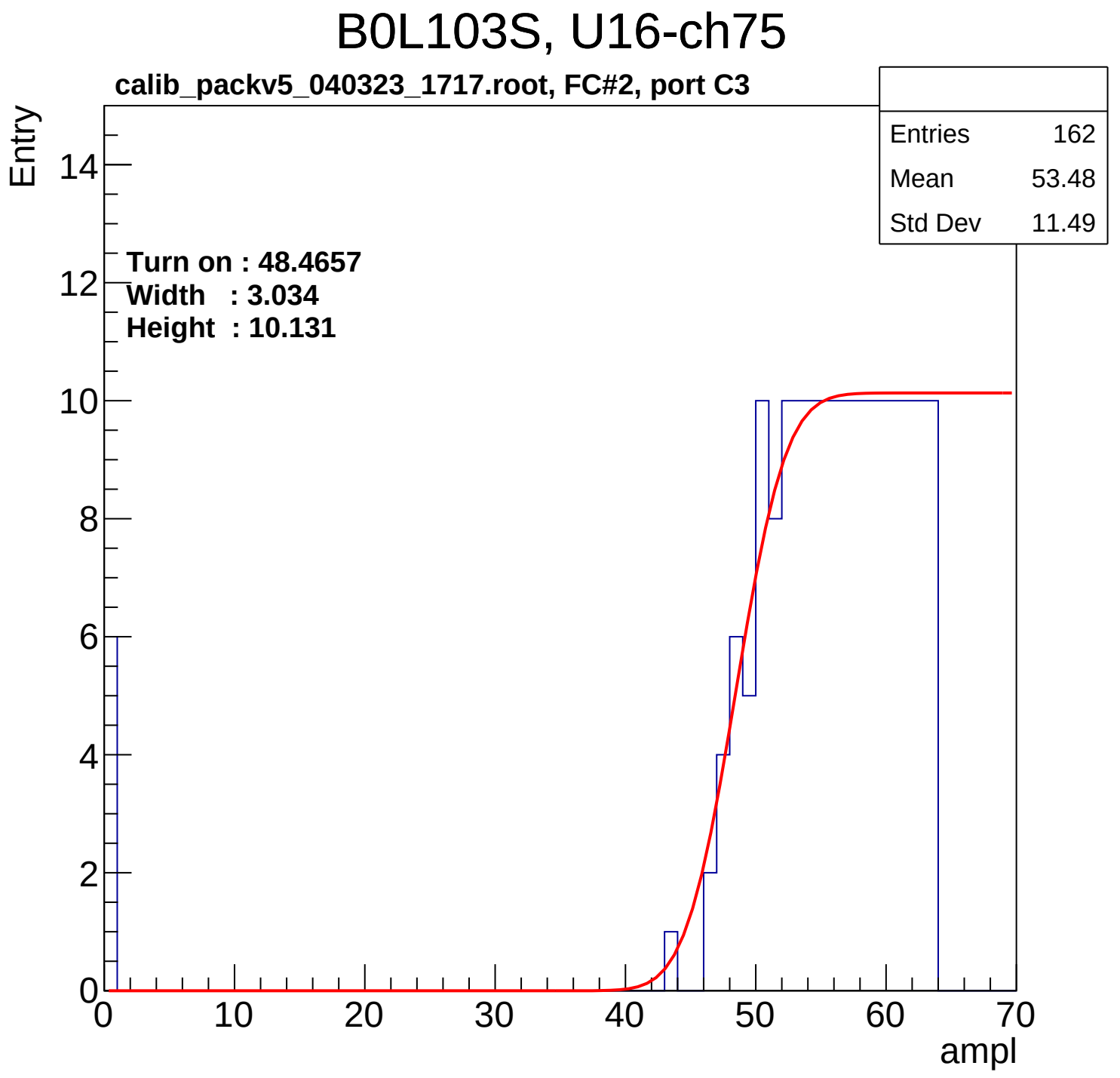
B0L103S, U16-ch75
calib_packv5_040323_1717.root, FC#2, port C3
Entries 162
Mean 53.48
Std Dev 11.49
Turn on : 48.4657
Width : 3.034
Height : 10.131
Entry
ampl
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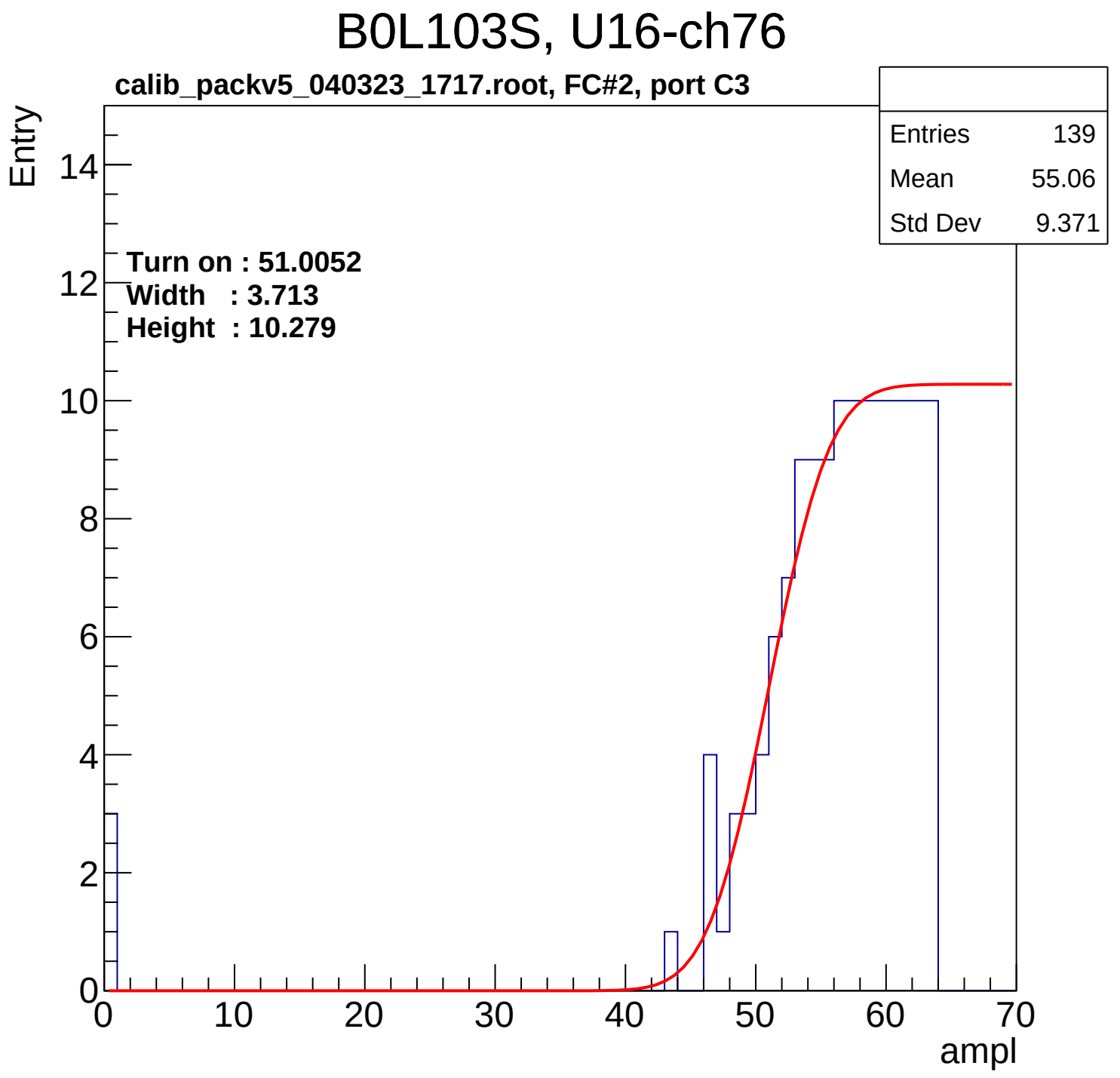
B0L103S, U16-ch76
calib_packv5_040323_1717.root, FC#2, port C3
Entries 139
Mean 55.06
Std Dev 9.371
Turn on : 51.0052
Width : 3.713
Height : 10.279
Entry
ampl
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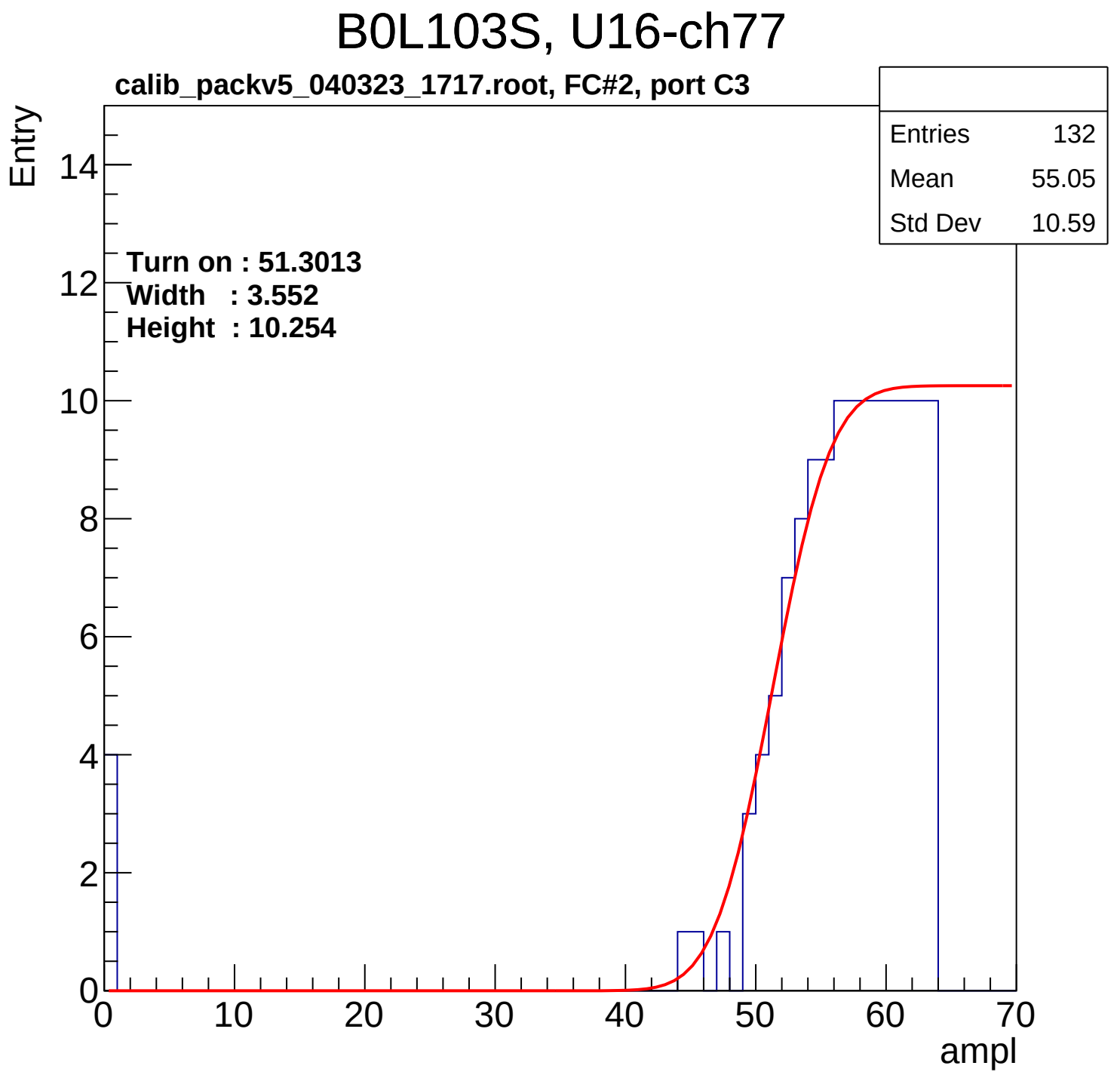
B0L103S, U16-ch77
calib_packv5_040323_1717.root, FC#2, port C3
Entries 132
Mean 55.05
Std Dev 10.59
Turn on : 51.3013
Width : 3.552
Height : 10.254
Entry
ampl
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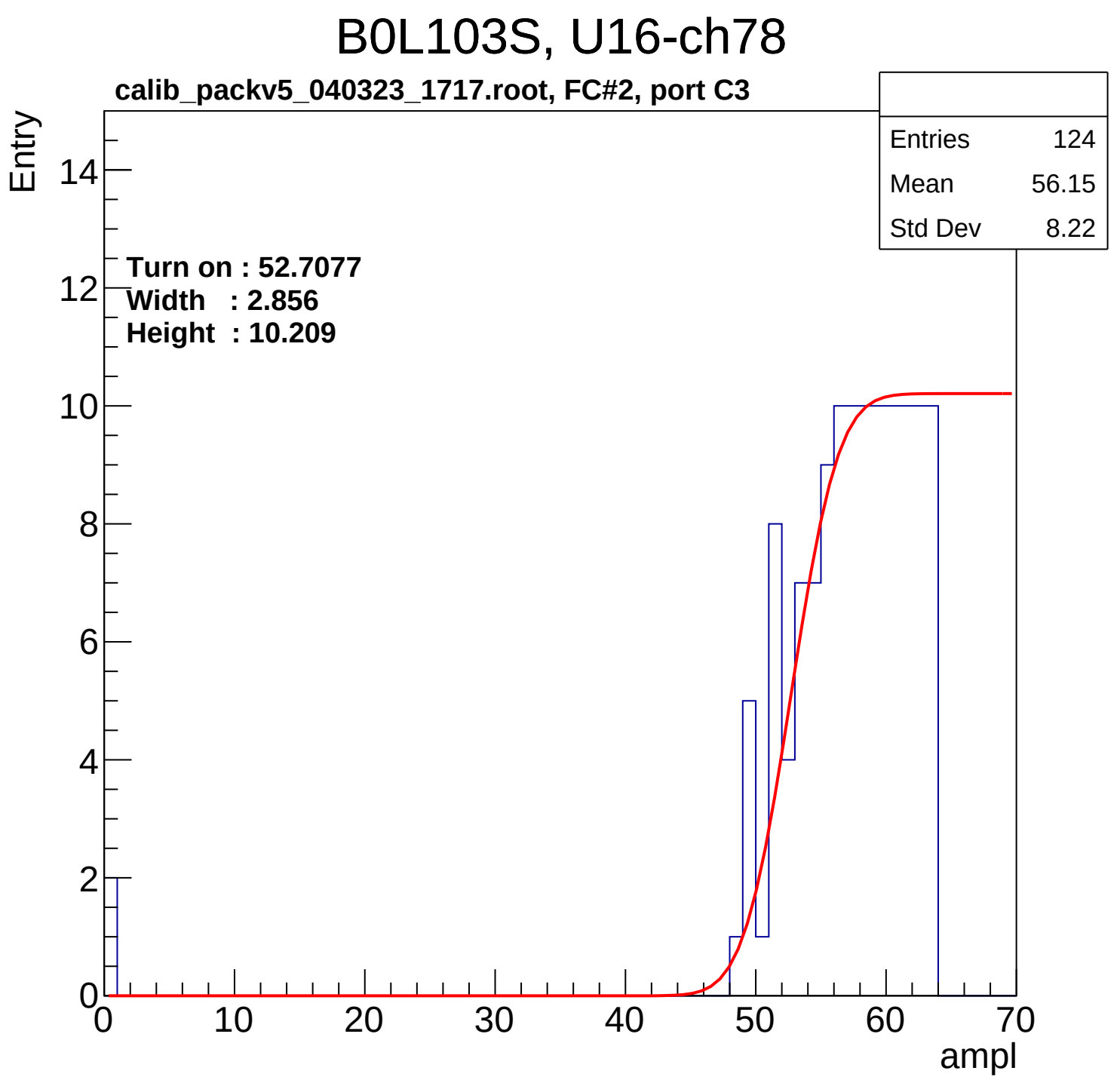
B0L103S, U16-ch78
calib_packv5_040323_1717.root, FC#2, port C3
Entries 124
Mean 56.15
Std Dev 8.22
Turn on : 52.7077
Width : 2.856
Height : 10.209
Entry
ampl
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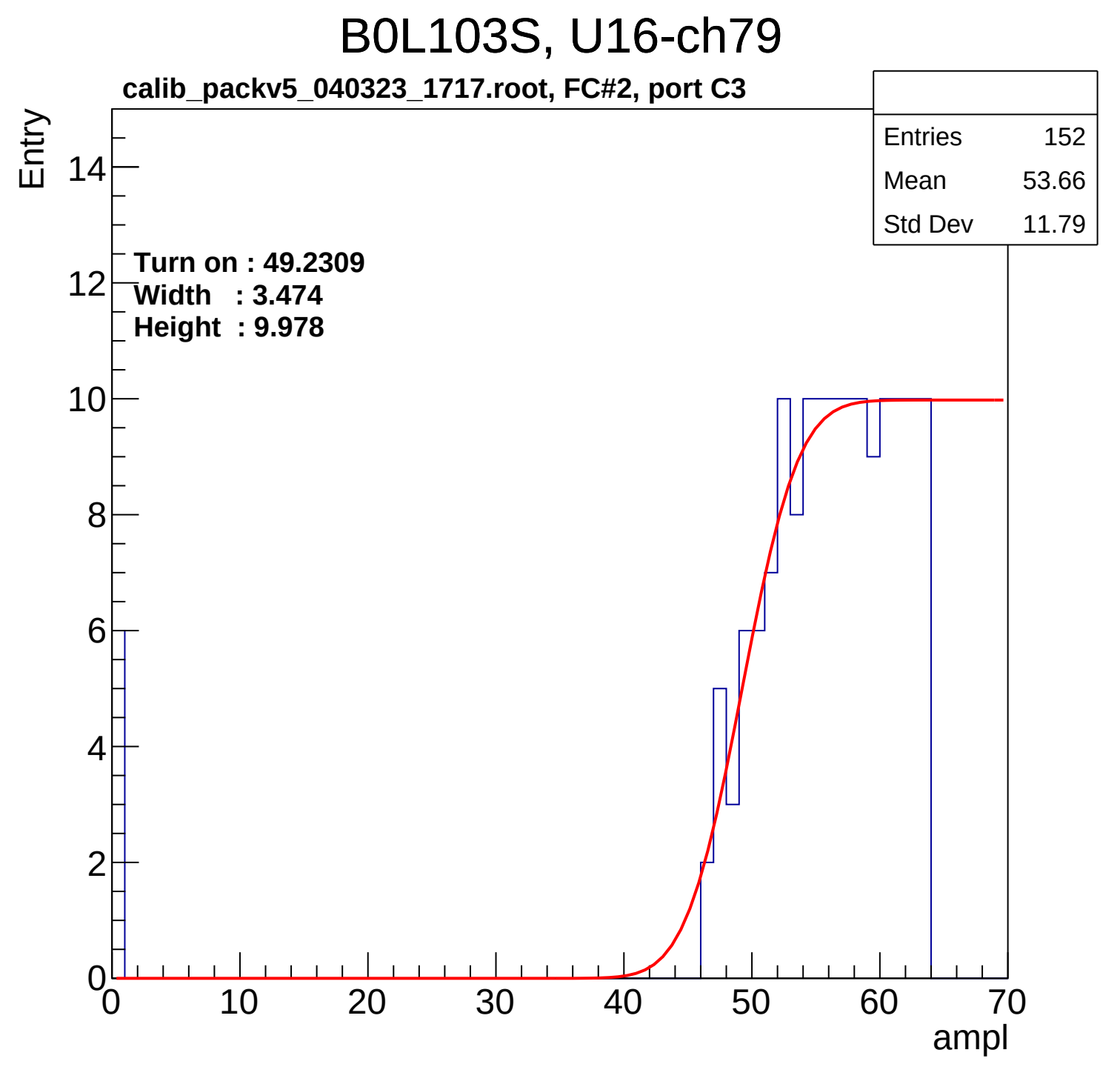
B0L103S, U16-ch79
calib_packv5_040323_1717.root, FC#2, port C3
Entries 152
Mean 53.66
Std Dev 11.79
Turn on : 49.2309
Width : 3.474
Height : 9.978
Entry
ampl
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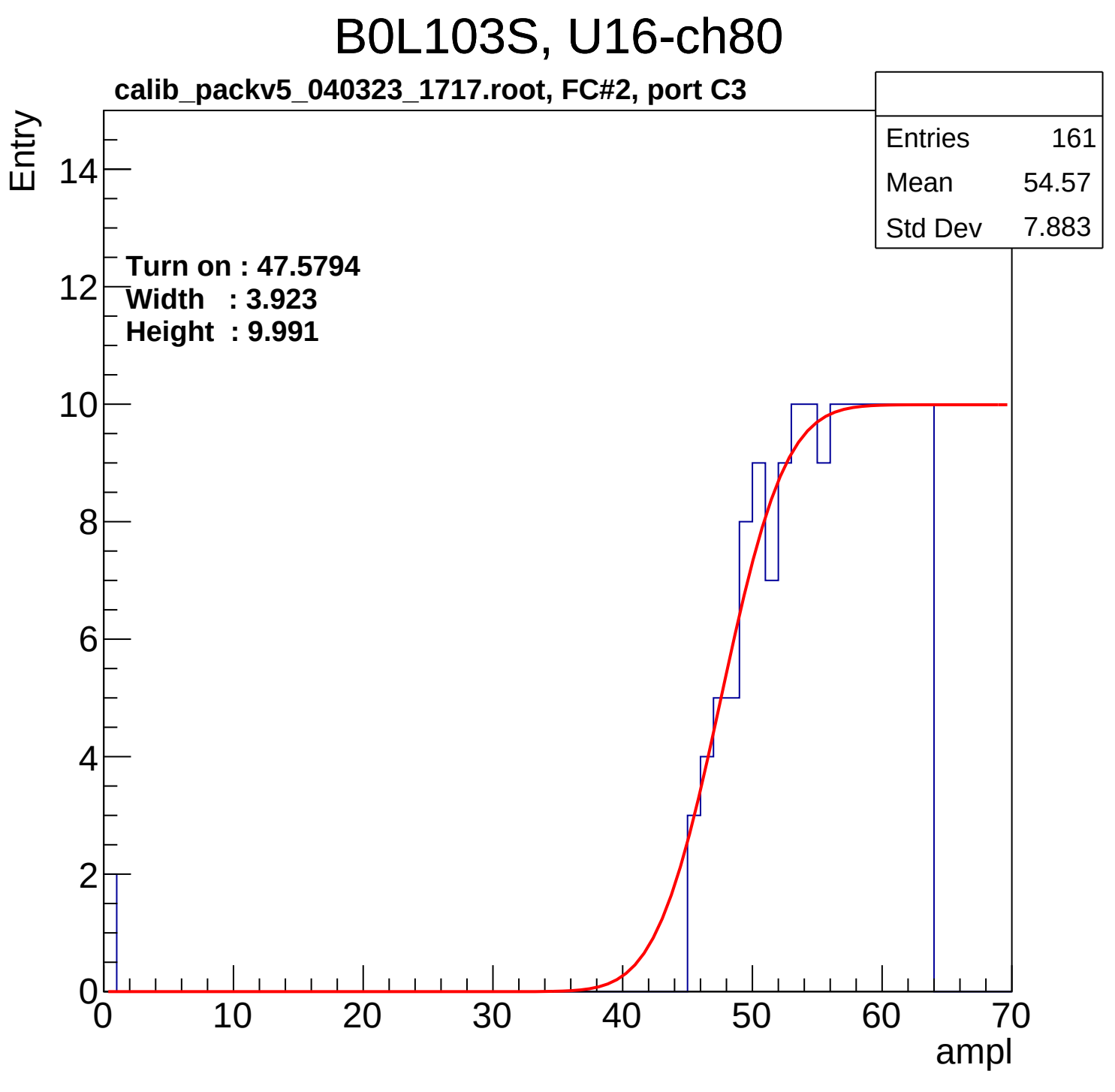
B0L103S, U16-ch80
calib_packv5_040323_1717.root, FC#2, port C3
Entries 161
Mean 54.57
Std Dev 7.883
Turn on : 47.5794
Width : 3.923
Height : 9.991
Entry
ampl
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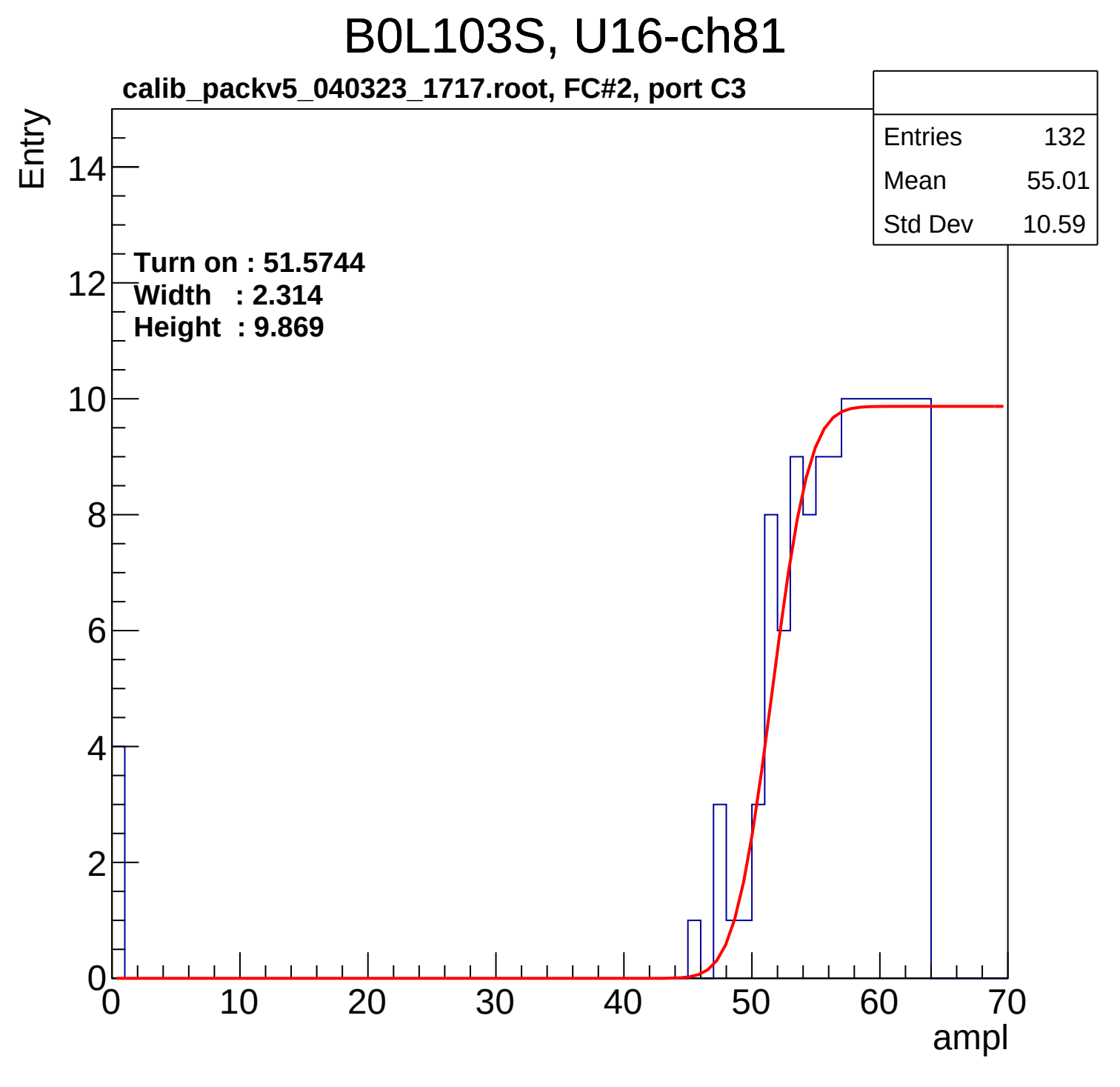
B0L103S, U16-ch81
calib_packv5_040323_1717.root, FC#2, port C3
Entries 132
Mean 55.01
Std Dev 10.59
Turn on : 51.5744
Width : 2.314
Height : 9.869
Entry
ampl
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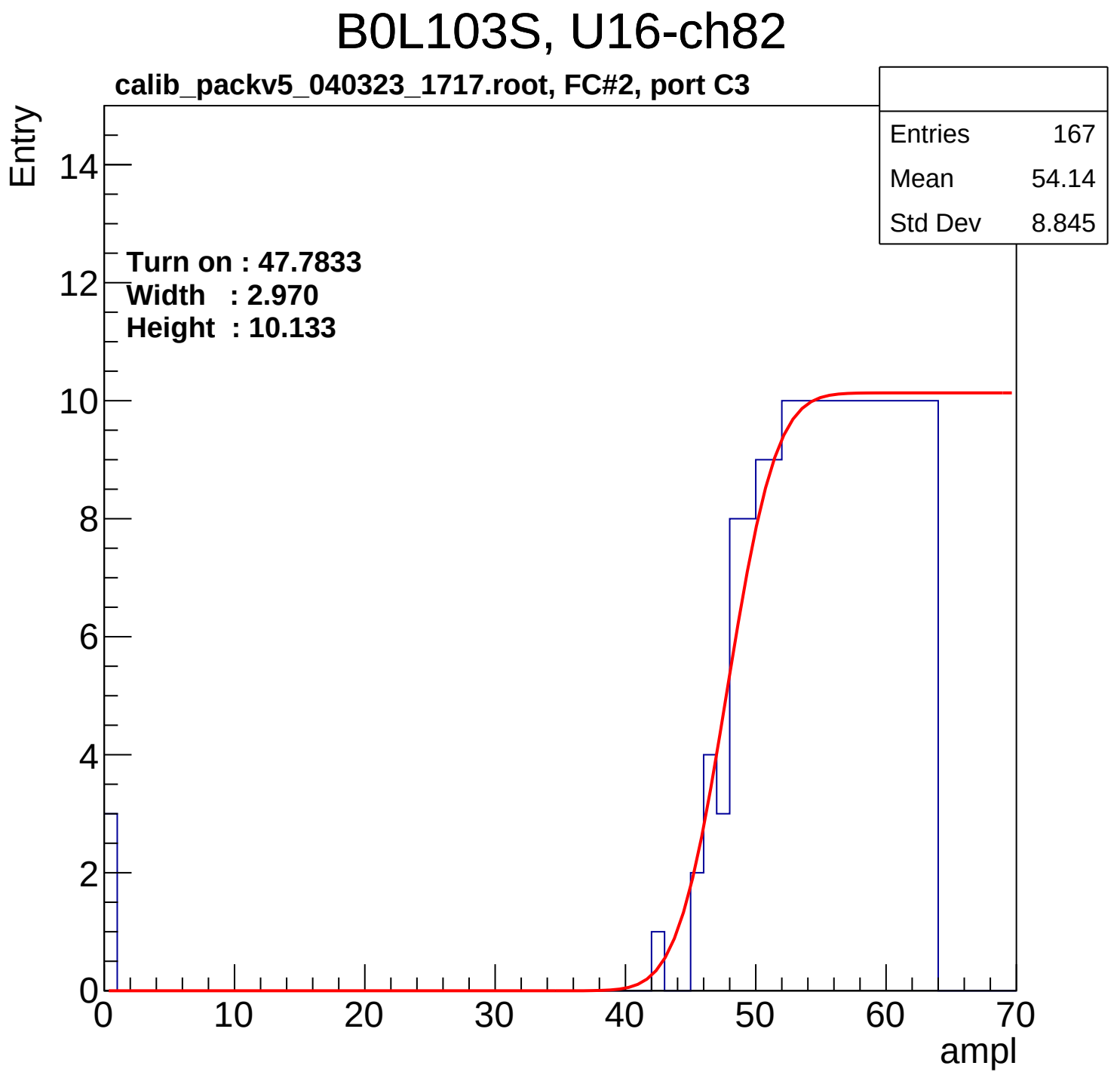
B0L103S, U16-ch82
calib_packv5_040323_1717.root, FC#2, port C3
Entries 167
Mean 54.14
Std Dev 8.845
Turn on : 47.7833
Width : 2.970
Height : 10.133
Entry
ampl
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6
8
10
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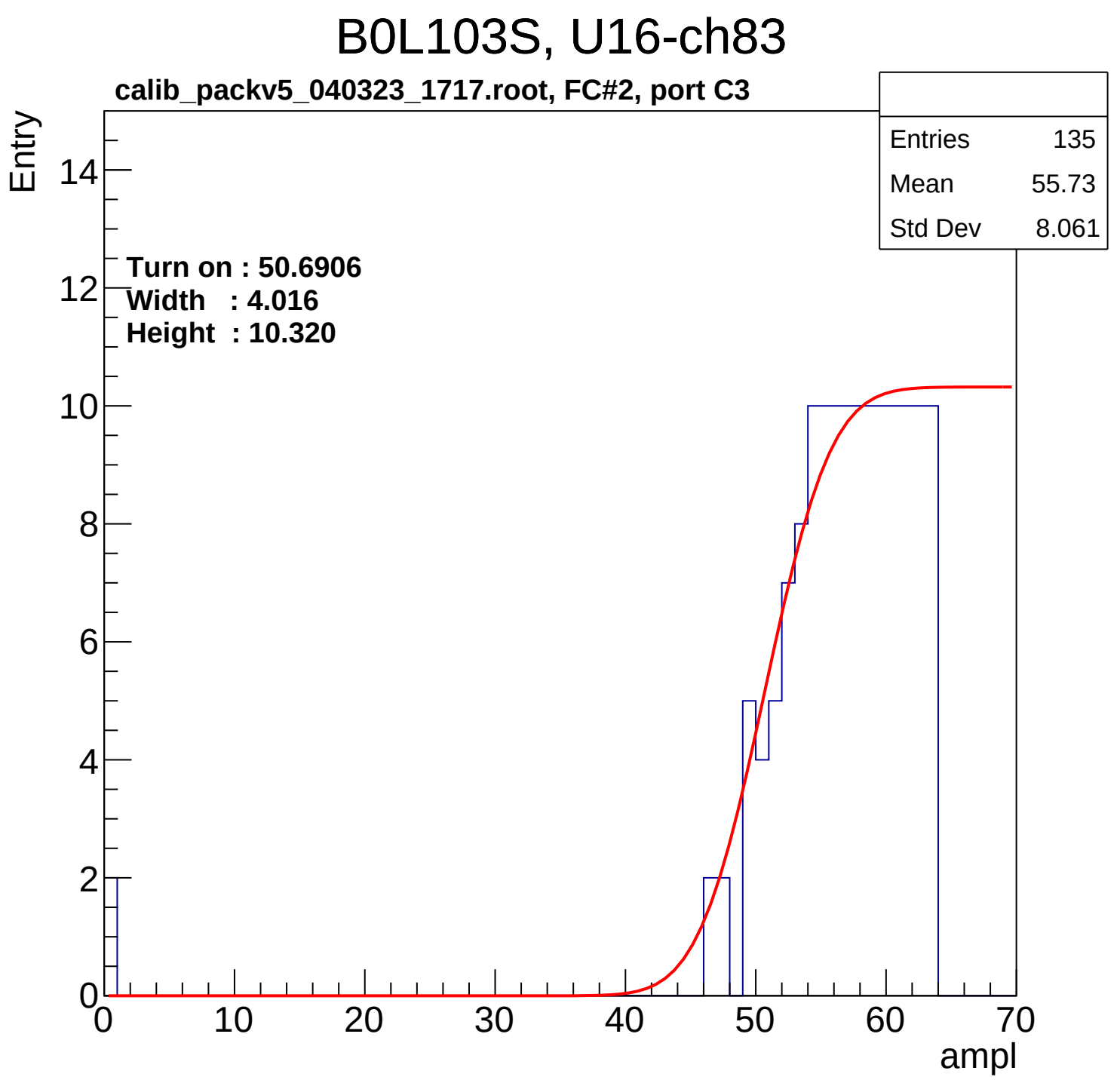
B0L103S, U16-ch83
calib_packv5_040323_1717.root, FC#2, port C3
Entries 135
Mean 55.73
Std Dev 8.061
Turn on : 50.6906
Width : 4.016
Height : 10.320
Entry
ampl
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6
8
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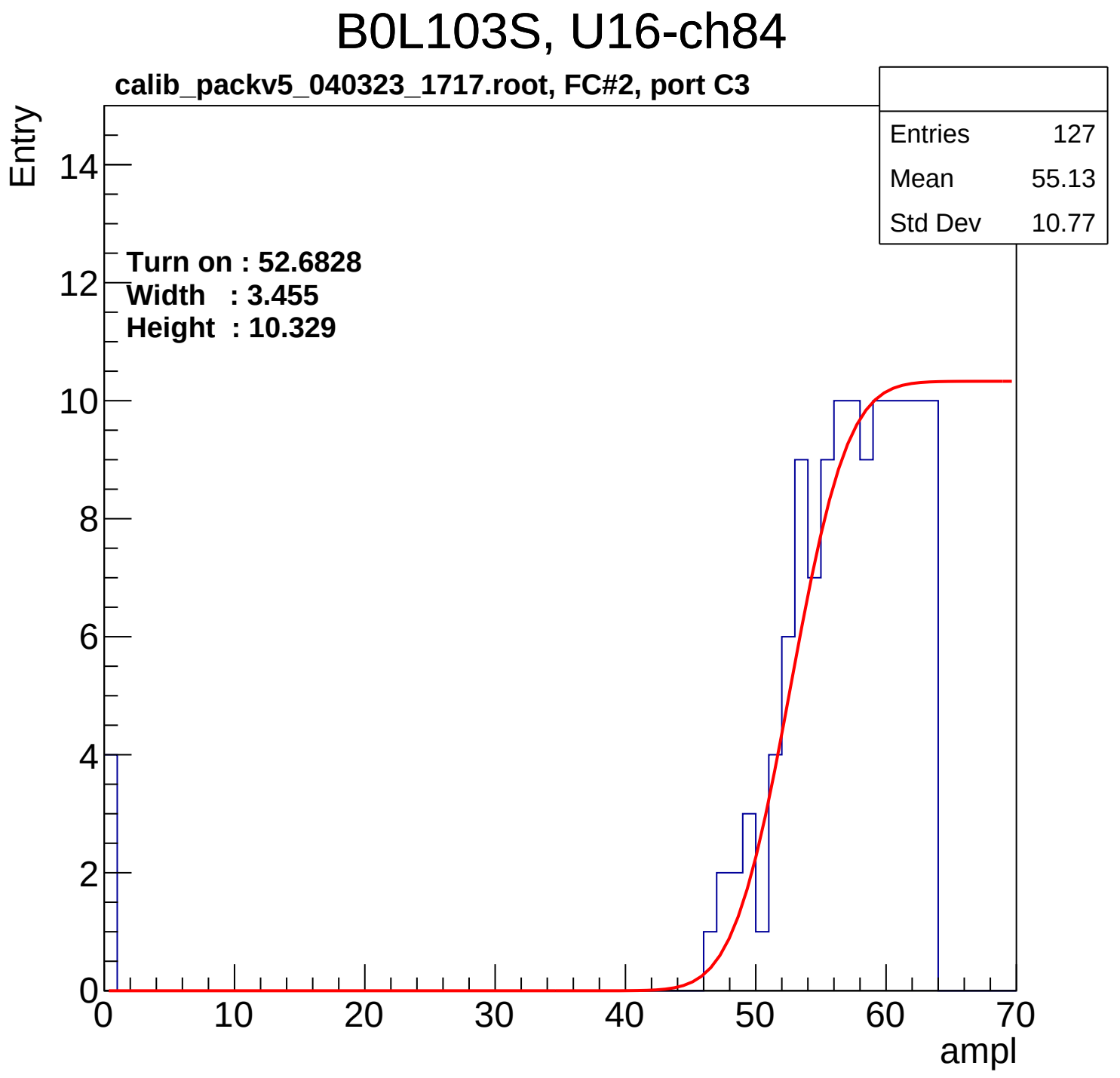
B0L103S, U16-ch84
calib_packv5_040323_1717.root, FC#2, port C3
Entries 127
Mean 55.13
Std Dev 10.77
Turn on : 52.6828
Width : 3.455
Height : 10.329
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ampl
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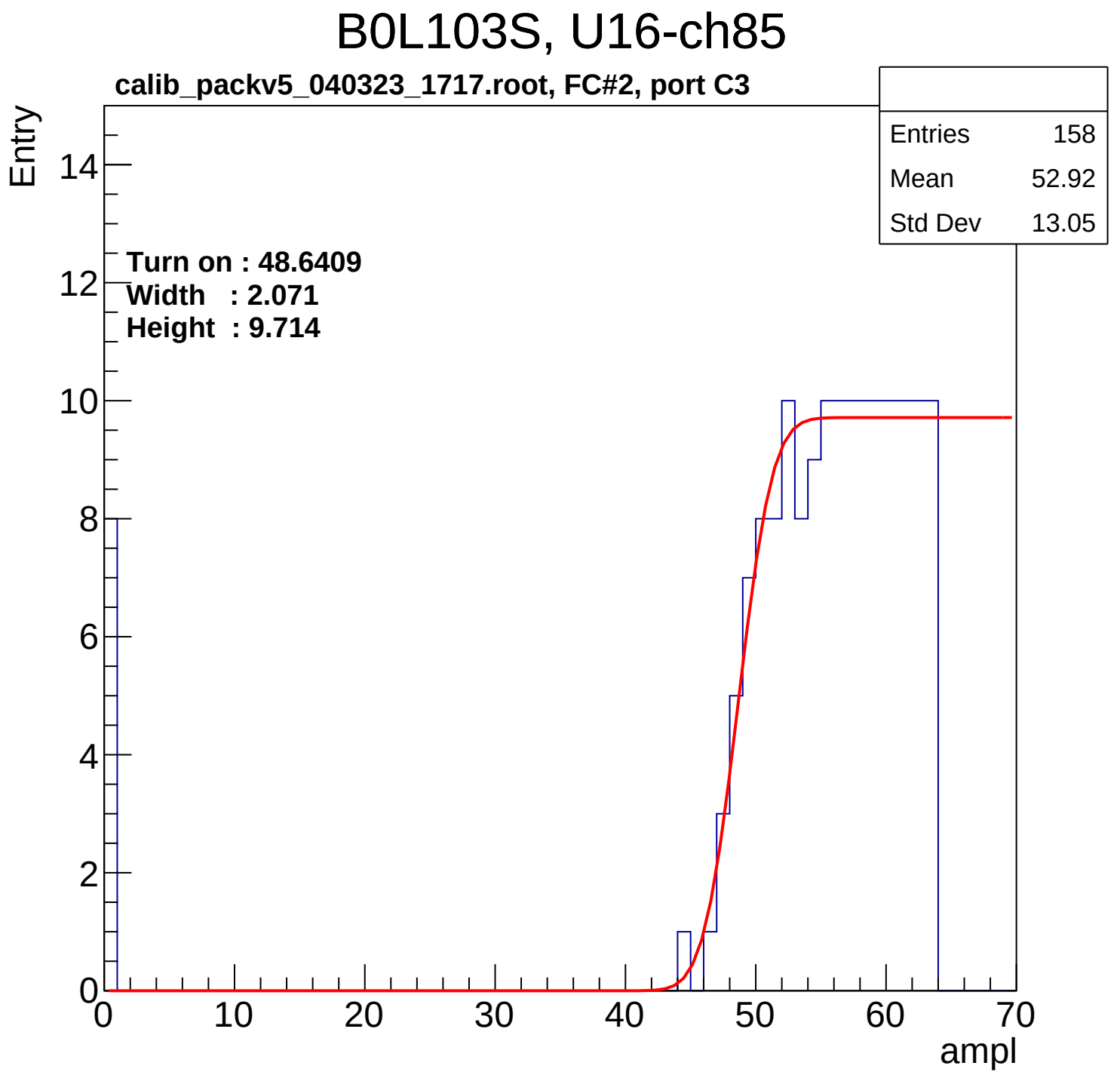
B0L103S, U16-ch85
calib_packv5_040323_1717.root, FC#2, port C3
Entries 158
Mean 52.92
Std Dev 13.05
Turn on : 48.6409
Width : 2.071
Height : 9.714
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ampl
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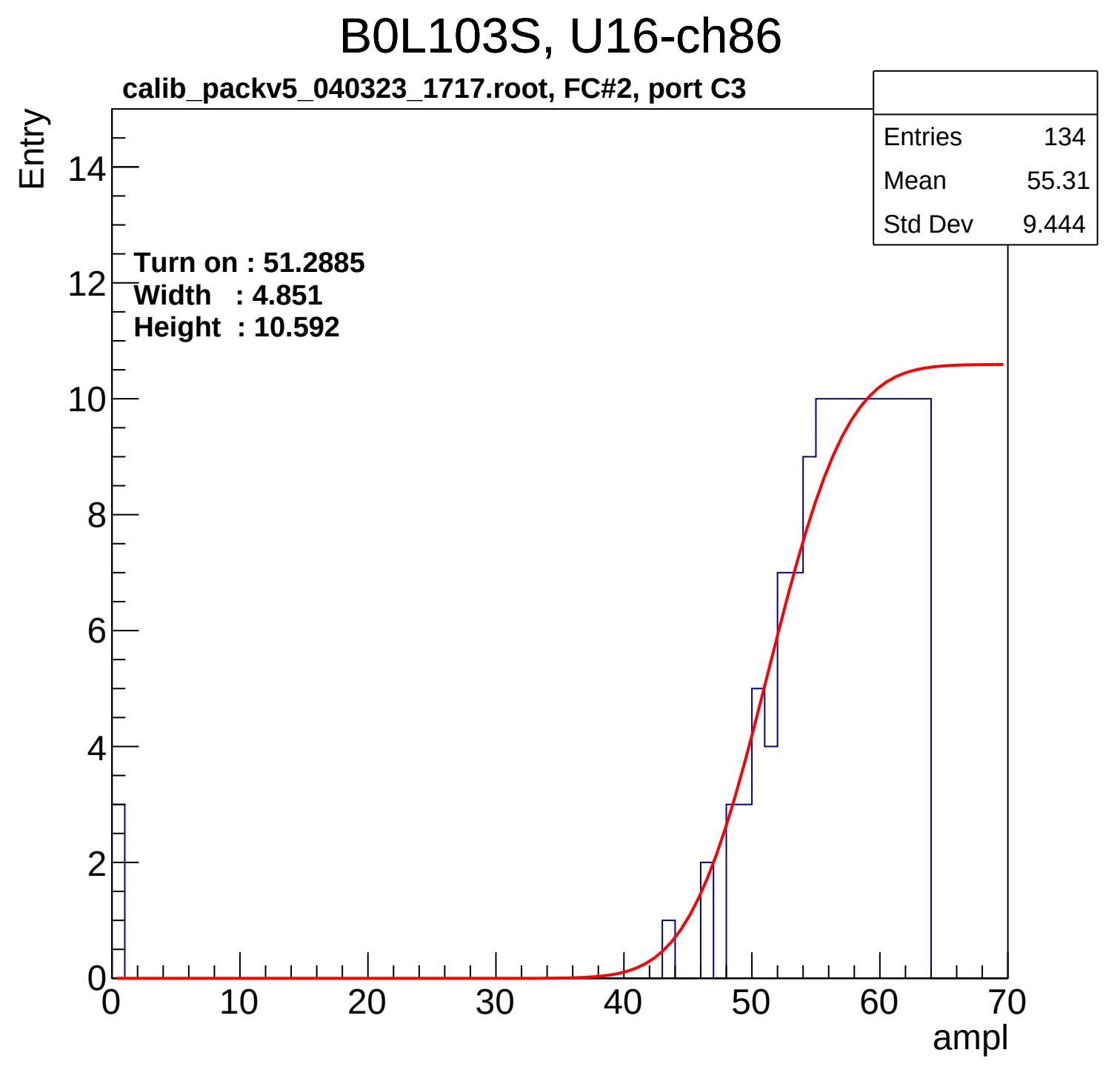
B0L103S, U16-ch86
calib_packv5_040323_1717.root, FC#2, port C3
Entries 134
Mean 55.31
Std Dev 9.444
Turn on : 51.2885
Width : 4.851
Height : 10.592
Entry
ampl
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4
6
8
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12
14
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10
20
30
40
50
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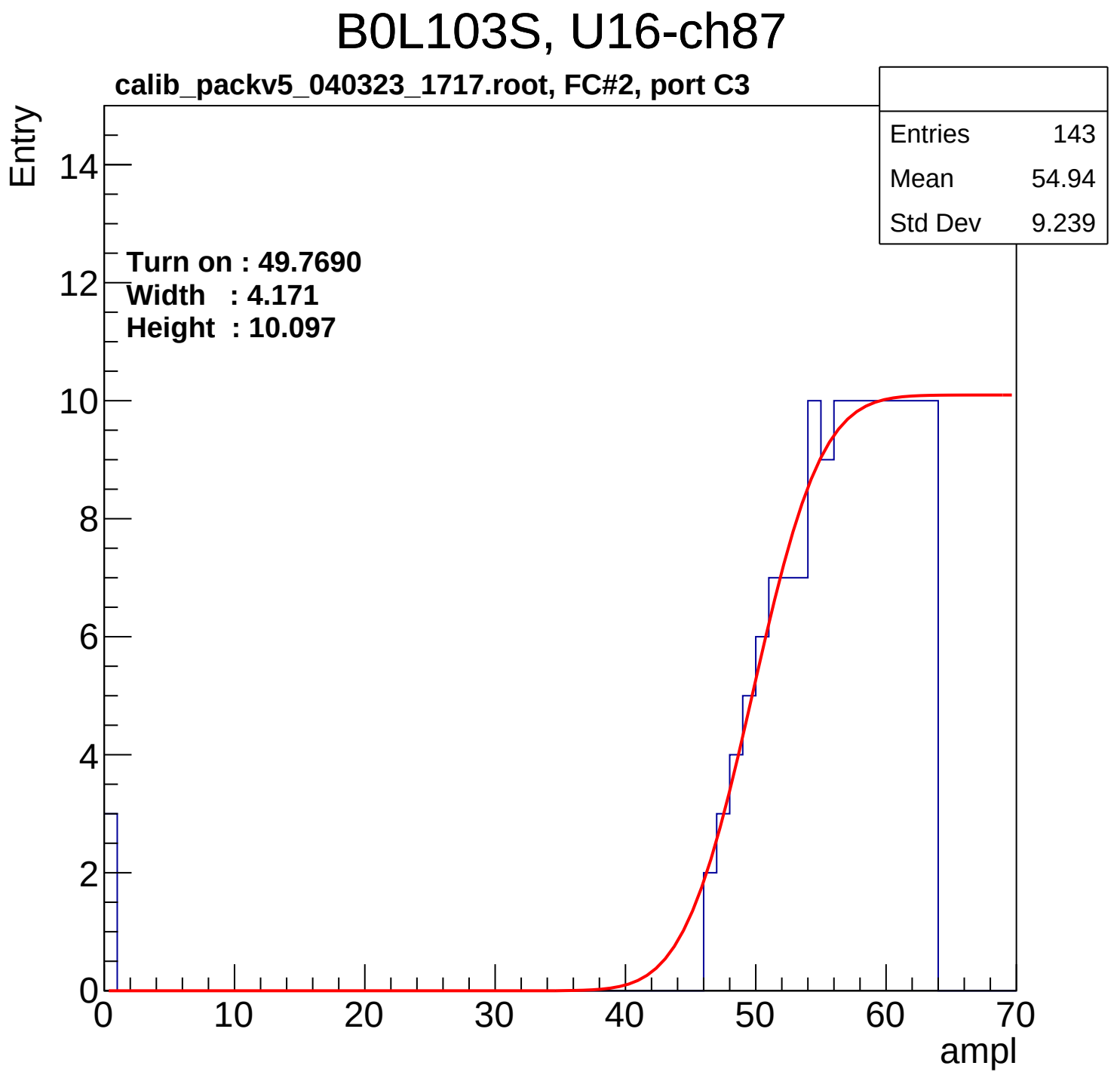
B0L103S, U16-ch87
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 54.94
Std Dev 9.239
Turn on : 49.7690
Width : 4.171
Height : 10.097
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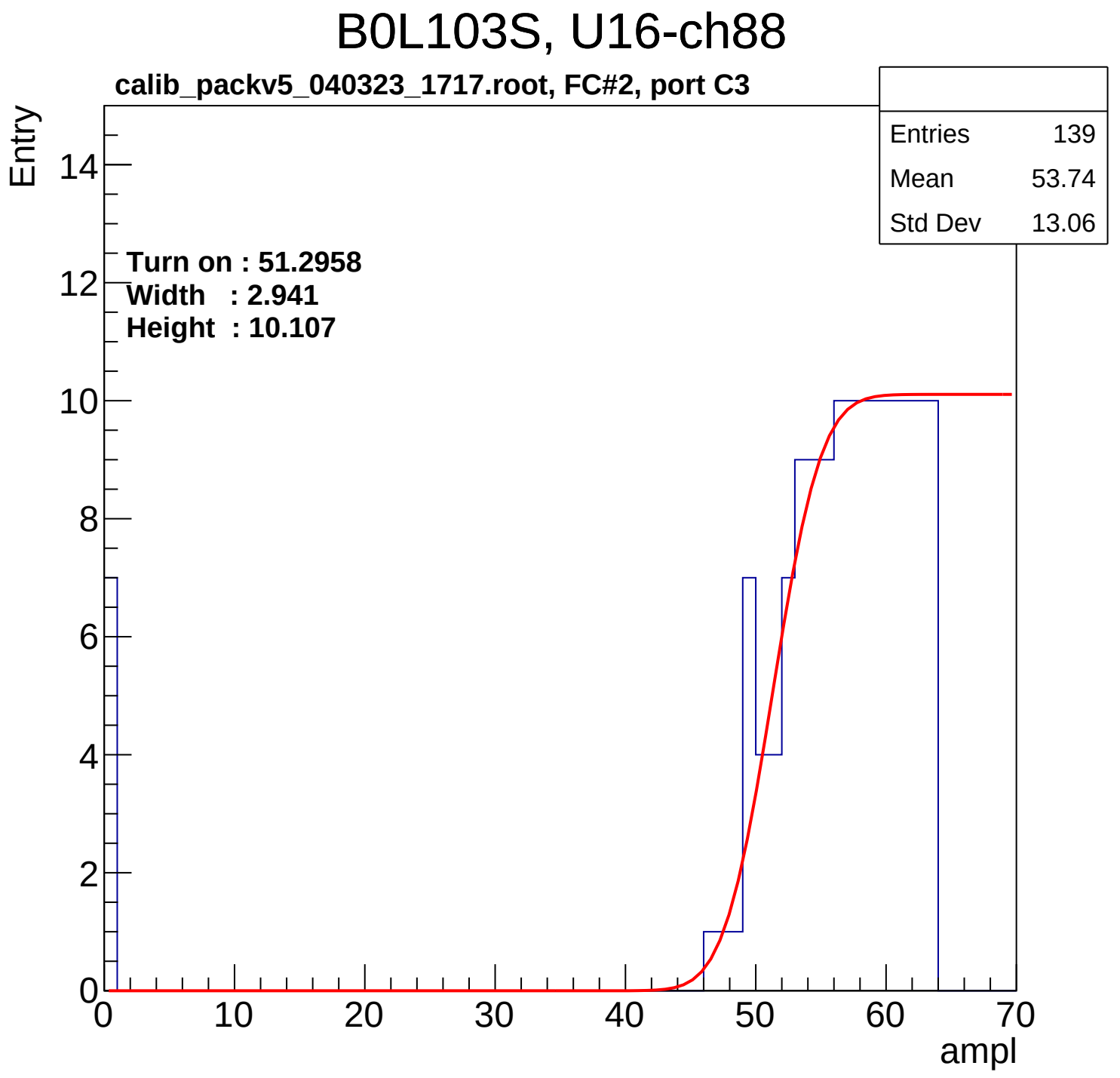
B0L103S, U16-ch88
calib_packv5_040323_1717.root, FC#2, port C3
Entries 139
Mean 53.74
Std Dev 13.06
Turn on : 51.2958
Width : 2.941
Height : 10.107
Entry
ampl
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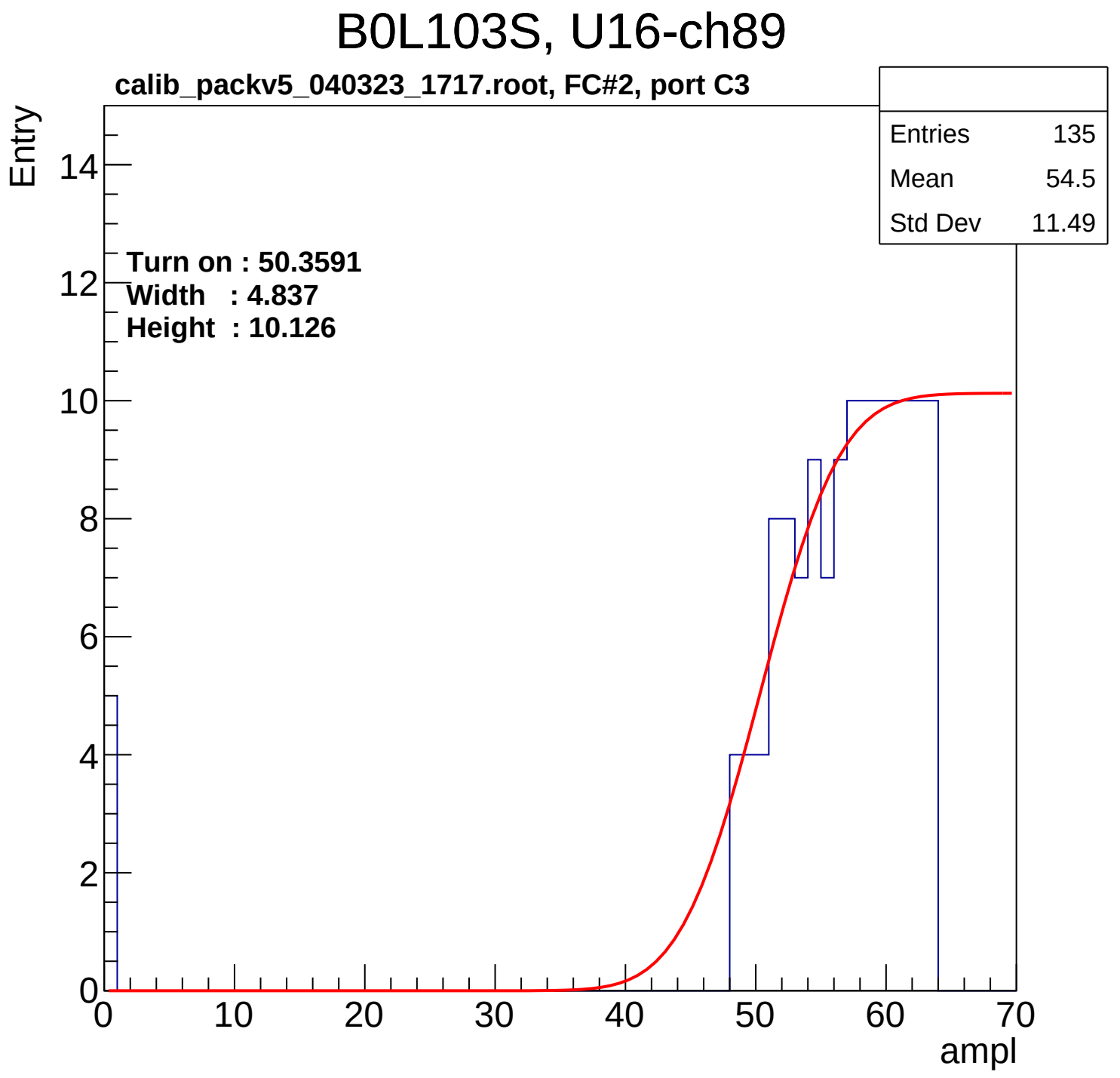
B0L103S, U16-ch89
calib_packv5_040323_1717.root, FC#2, port C3
Entries 135
Mean 54.5
Std Dev 11.49
Turn on : 50.3591
Width : 4.837
Height : 10.126
Entry
ampl
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4
6
8
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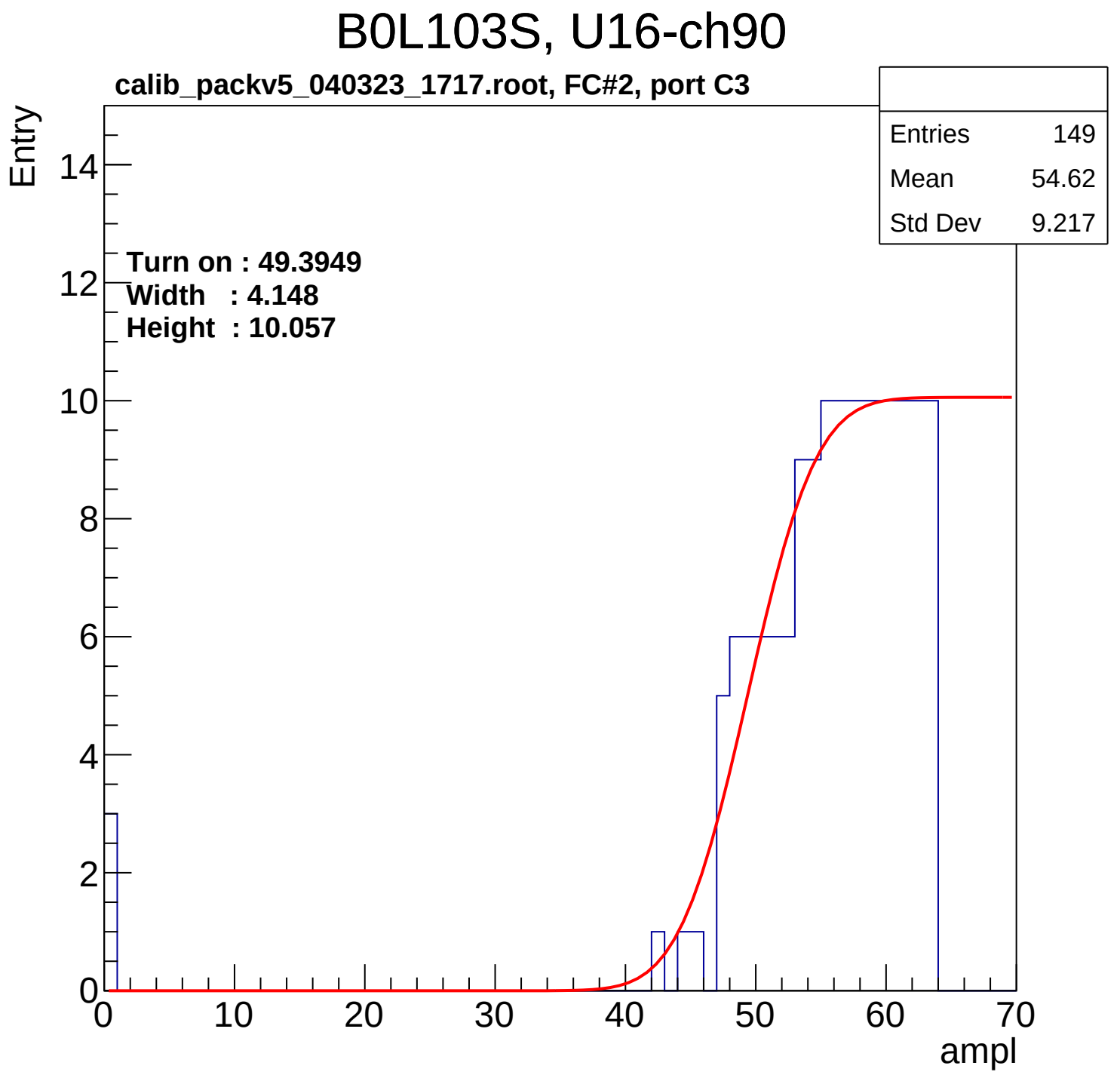
B0L103S, U16-ch90
calib_packv5_040323_1717.root, FC#2, port C3
Entries 149
Mean 54.62
Std Dev 9.217
Turn on : 49.3949
Width : 4.148
Height : 10.057
Entry
ampl
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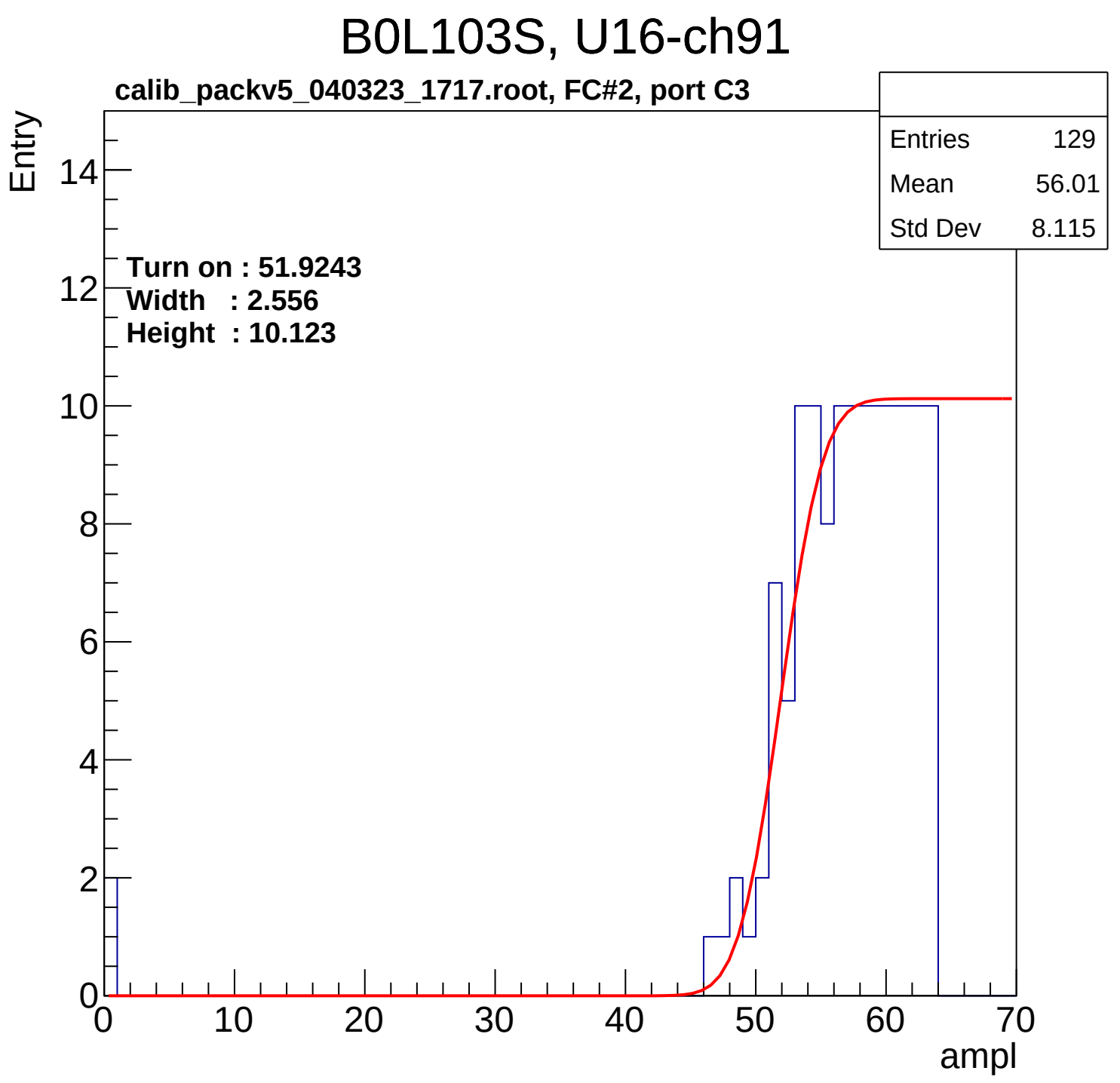
B0L103S, U16-ch91
calib_packv5_040323_1717.root, FC#2, port C3
Entries 129
Mean 56.01
Std Dev 8.115
Turn on : 51.9243
Width : 2.556
Height : 10.123
Entry
ampl
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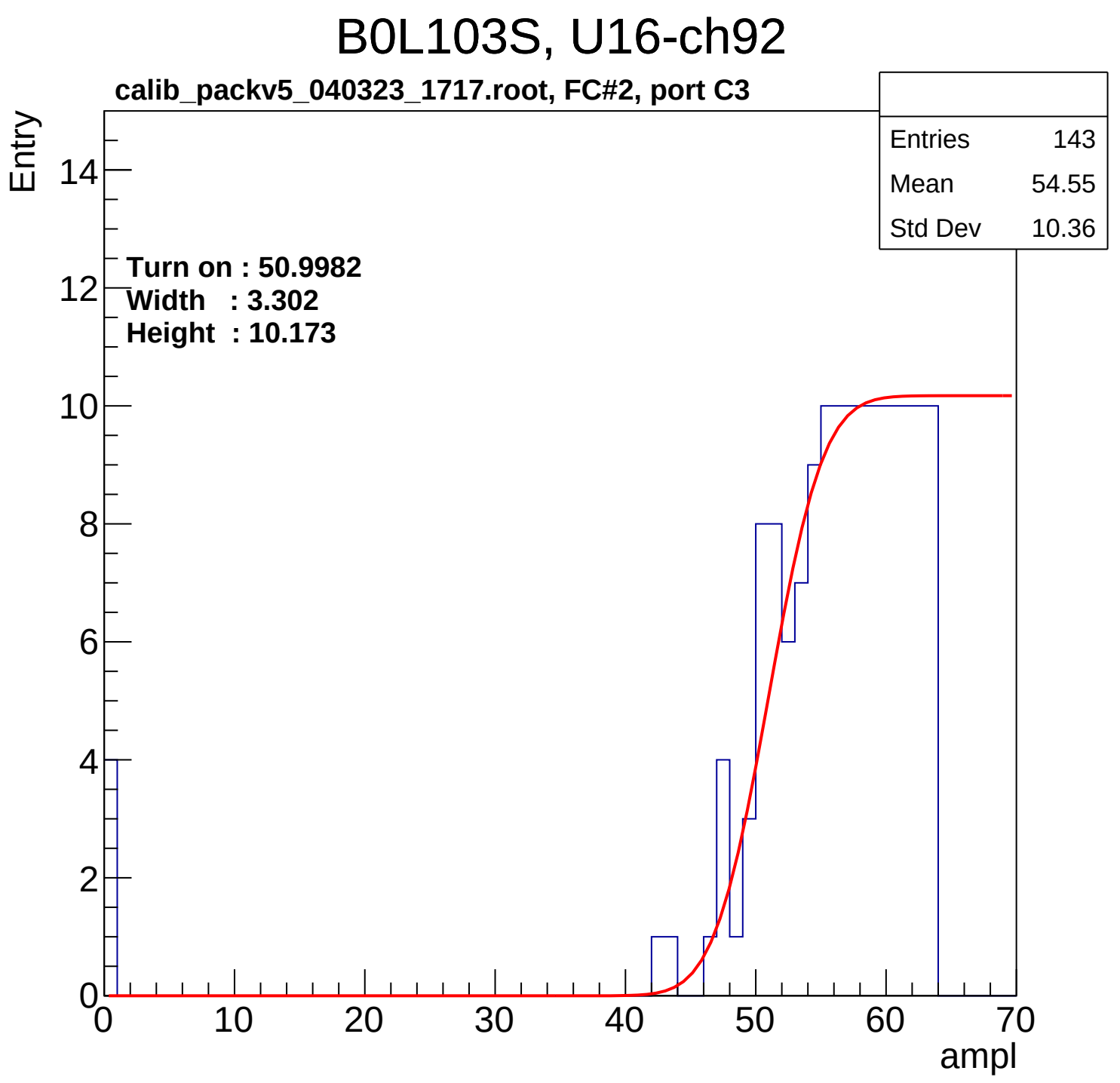
B0L103S, U16-ch92
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 54.55
Std Dev 10.36
Turn on : 50.9982
Width : 3.302
Height : 10.173
Entry
ampl
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2
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6
8
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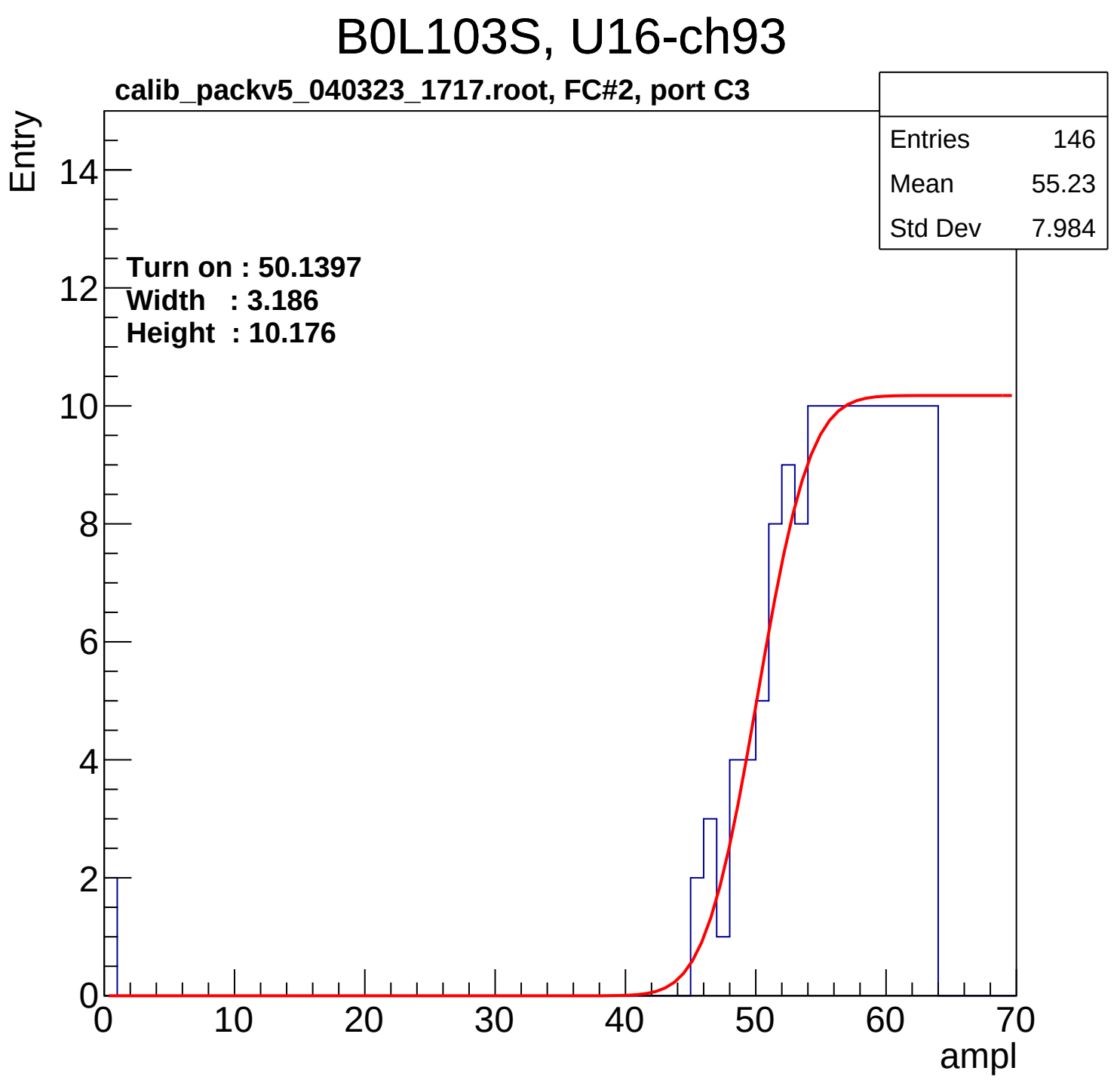
B0L103S, U16-ch93
calib_packv5_040323_1717.root, FC#2, port C3
Entries 146
Mean 55.23
Std Dev 7.984
Turn on : 50.1397
Width : 3.186
Height : 10.176
Entry
ampl
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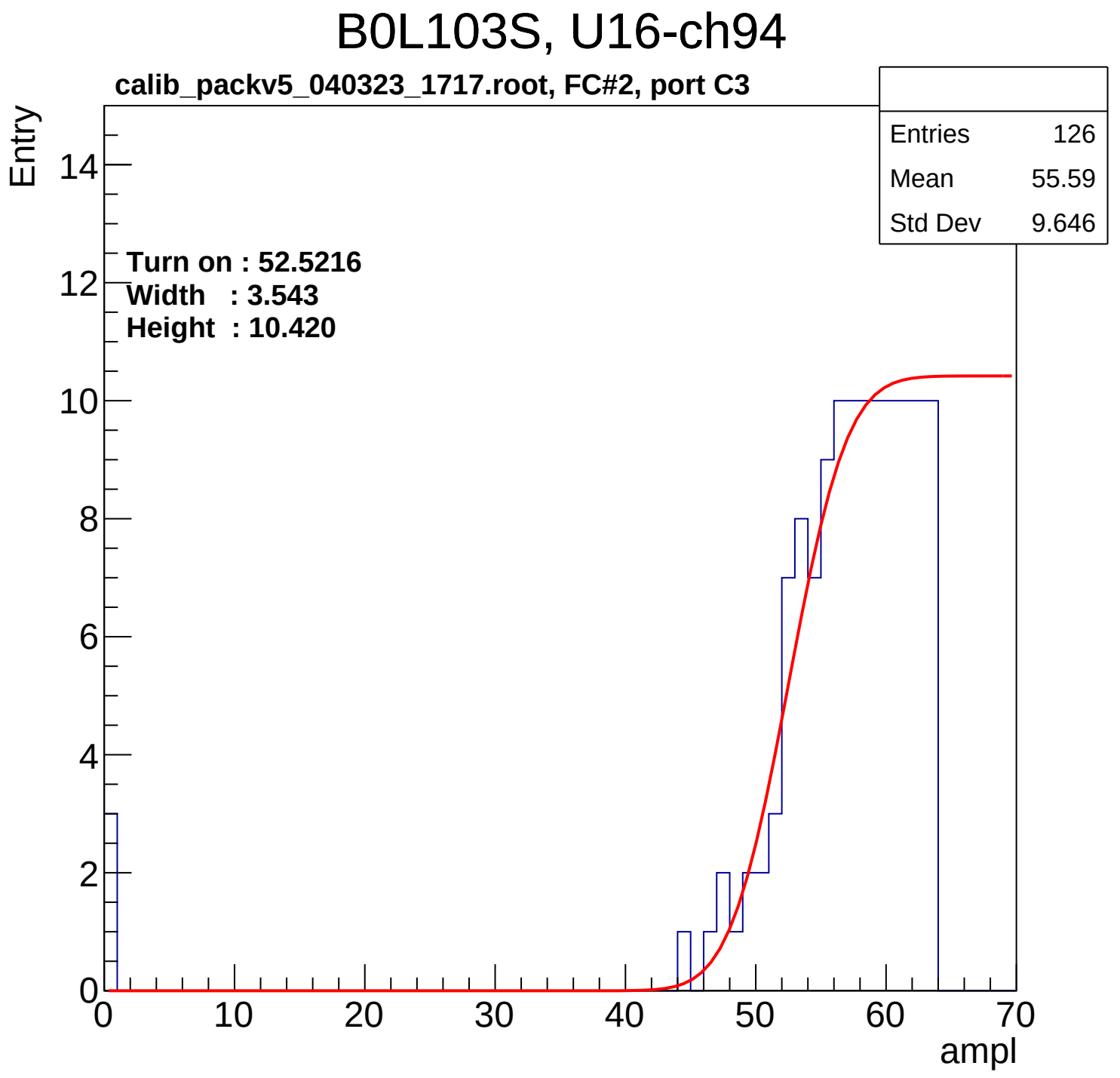
B0L103S, U16-ch94
calib_packv5_040323_1717.root, FC#2, port C3
Entries 126
Mean 55.59
Std Dev 9.646
Turn on : 52.5216
Width : 3.543
Height : 10.420
Entry
ampl
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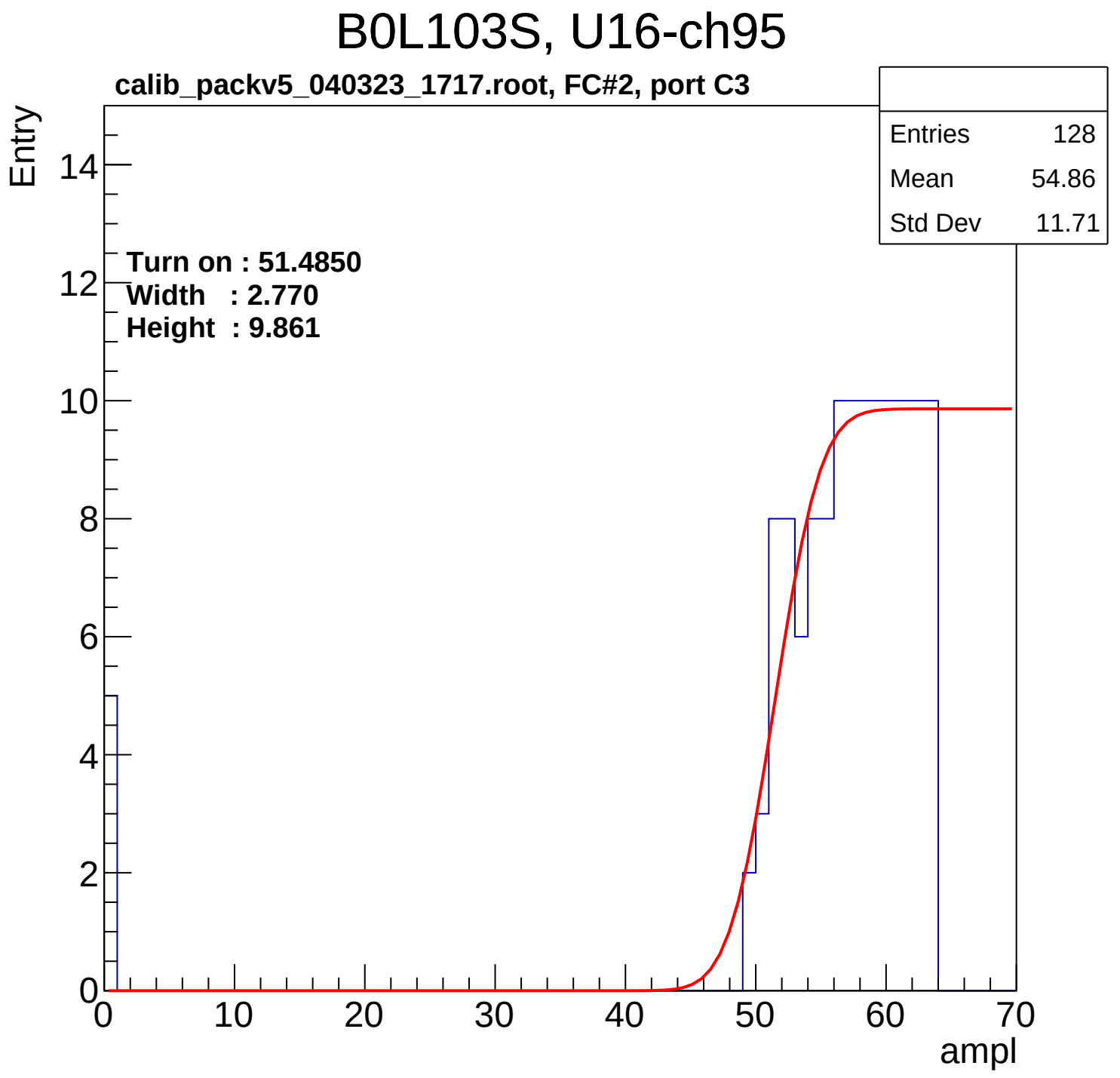
B0L103S, U16-ch95
calib_packv5_040323_1717.root, FC#2, port C3
Entries 128
Mean 54.86
Std Dev 11.71
Turn on : 51.4850
Width : 2.770
Height : 9.861
Entry
ampl
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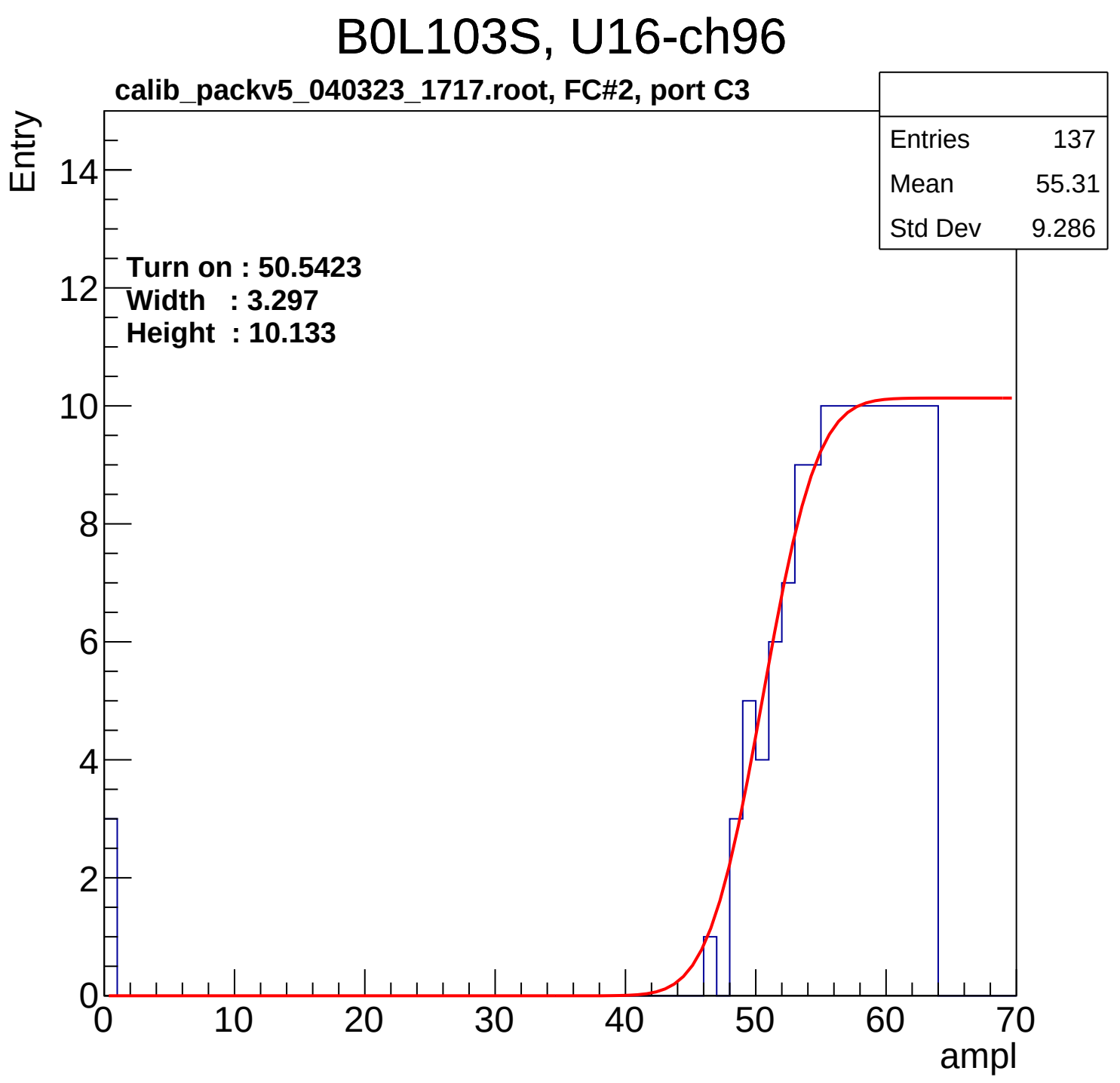
B0L103S, U16-ch96
calib_packv5_040323_1717.root, FC#2, port C3
Entries 137
Mean 55.31
Std Dev 9.286
Turn on : 50.5423
Width : 3.297
Height : 10.133
Entry
ampl
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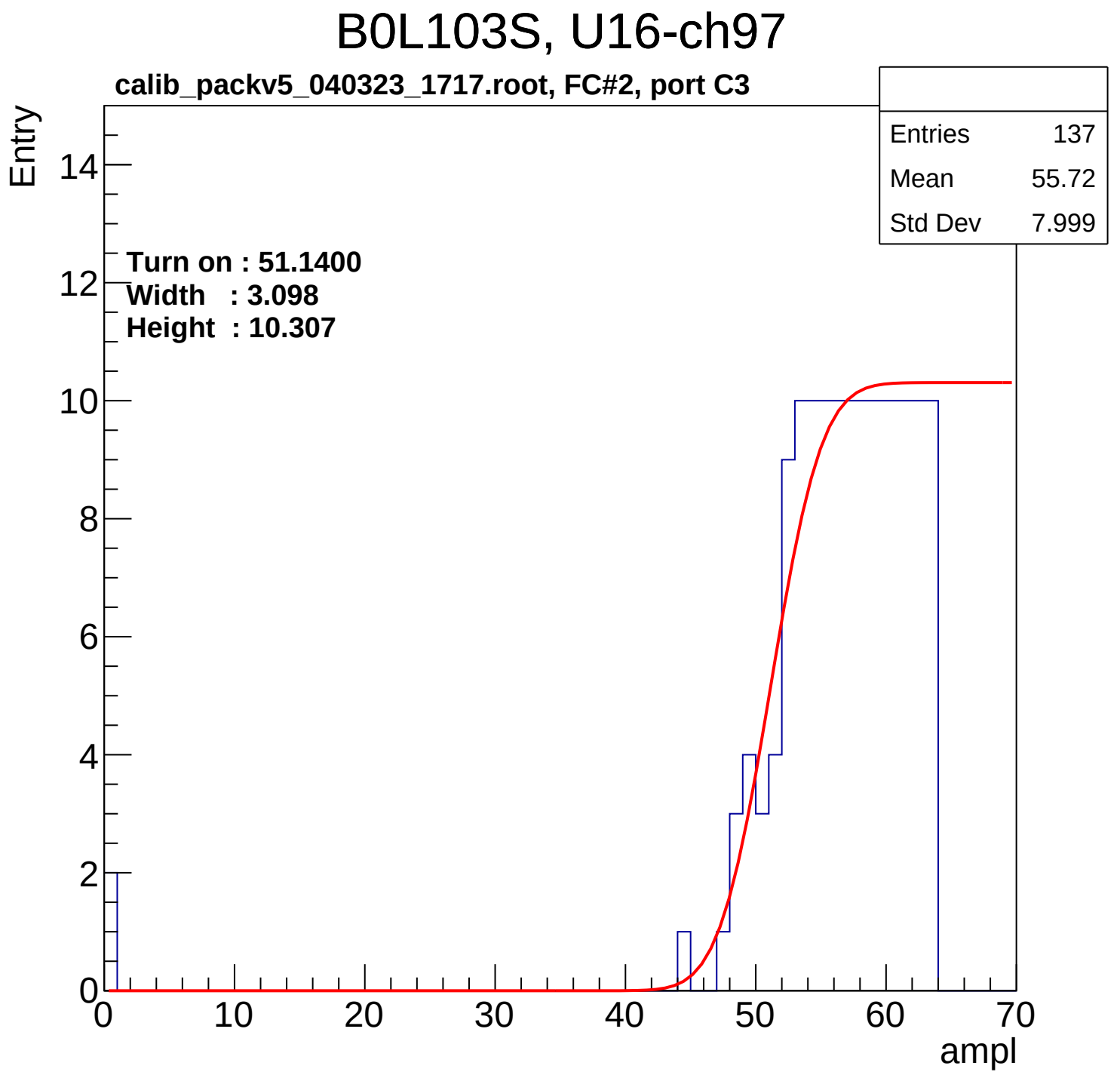
B0L103S, U16-ch97
calib_packv5_040323_1717.root, FC#2, port C3
Entries 137
Mean 55.72
Std Dev 7.999
Turn on : 51.1400
Width : 3.098
Height : 10.307
Entry
ampl
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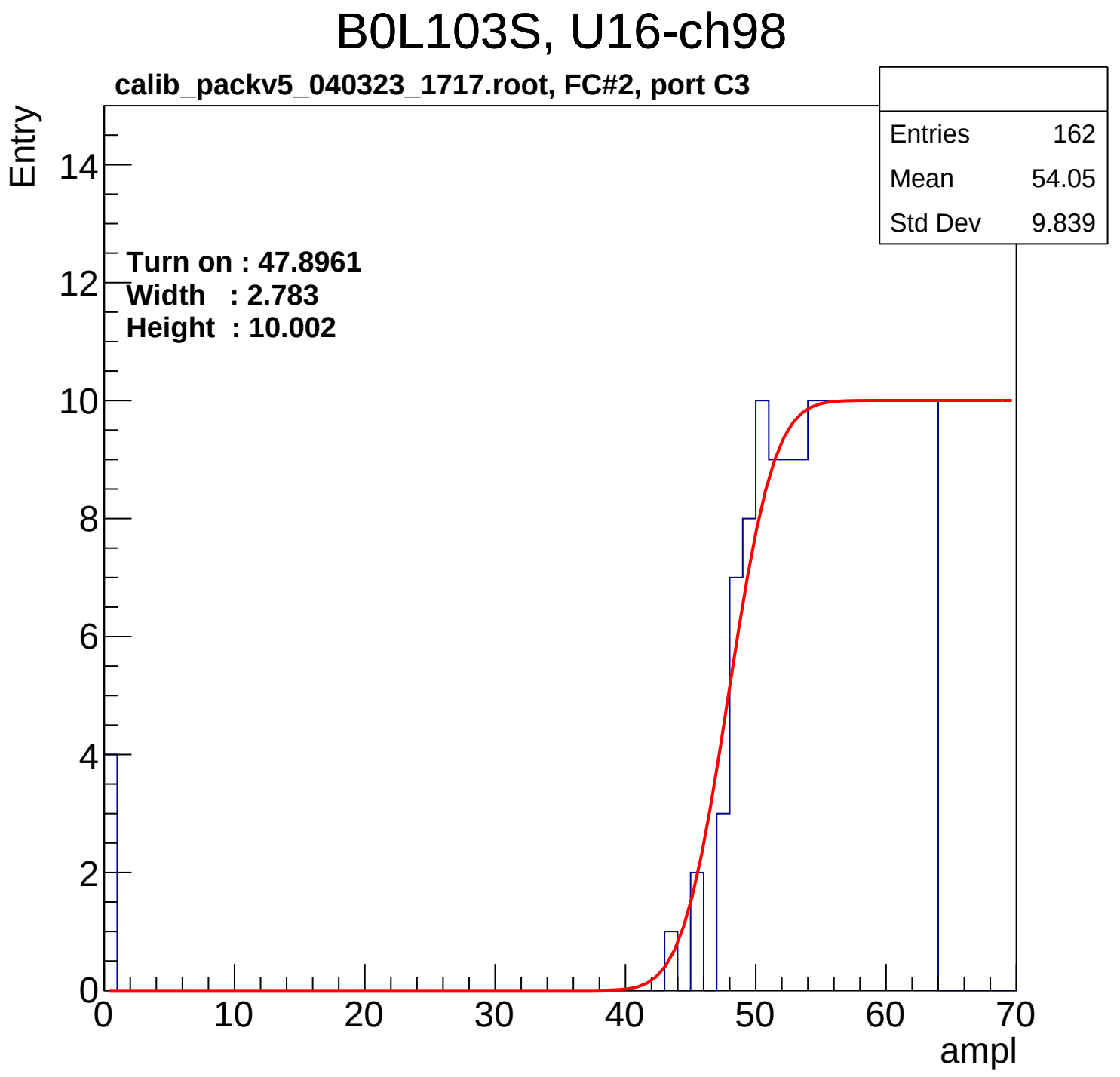
B0L103S, U16-ch98
calib_packv5_040323_1717.root, FC#2, port C3
Entries 162
Mean 54.05
Std Dev 9.839
Turn on : 47.8961
Width : 2.783
Height : 10.002
Entry
ampl
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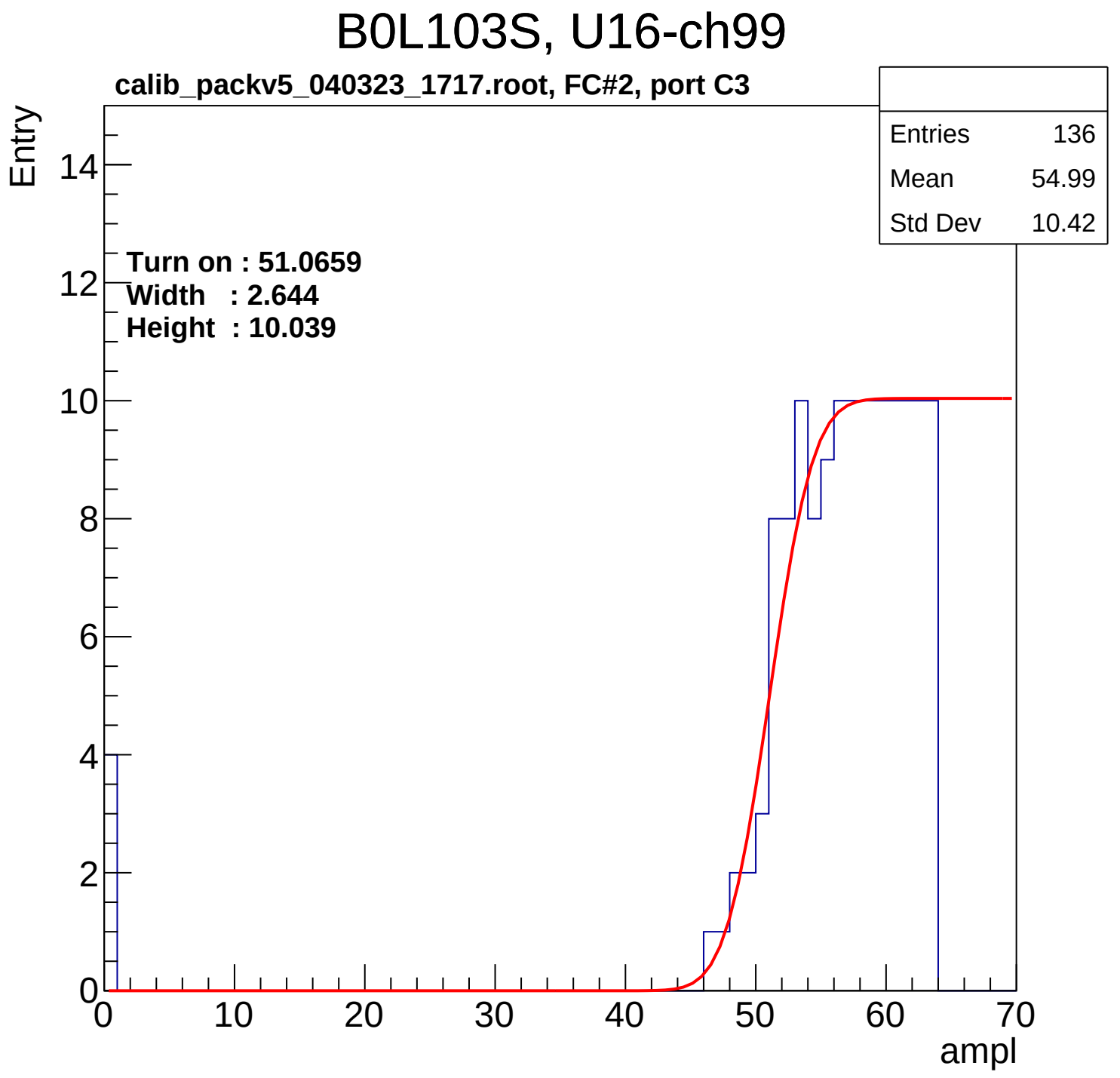
B0L103S, U16-ch99
calib_packv5_040323_1717.root, FC#2, port C3
Entries 136
Mean 54.99
Std Dev 10.42
Turn on : 51.0659
Width : 2.644
Height : 10.039
Entry
ampl
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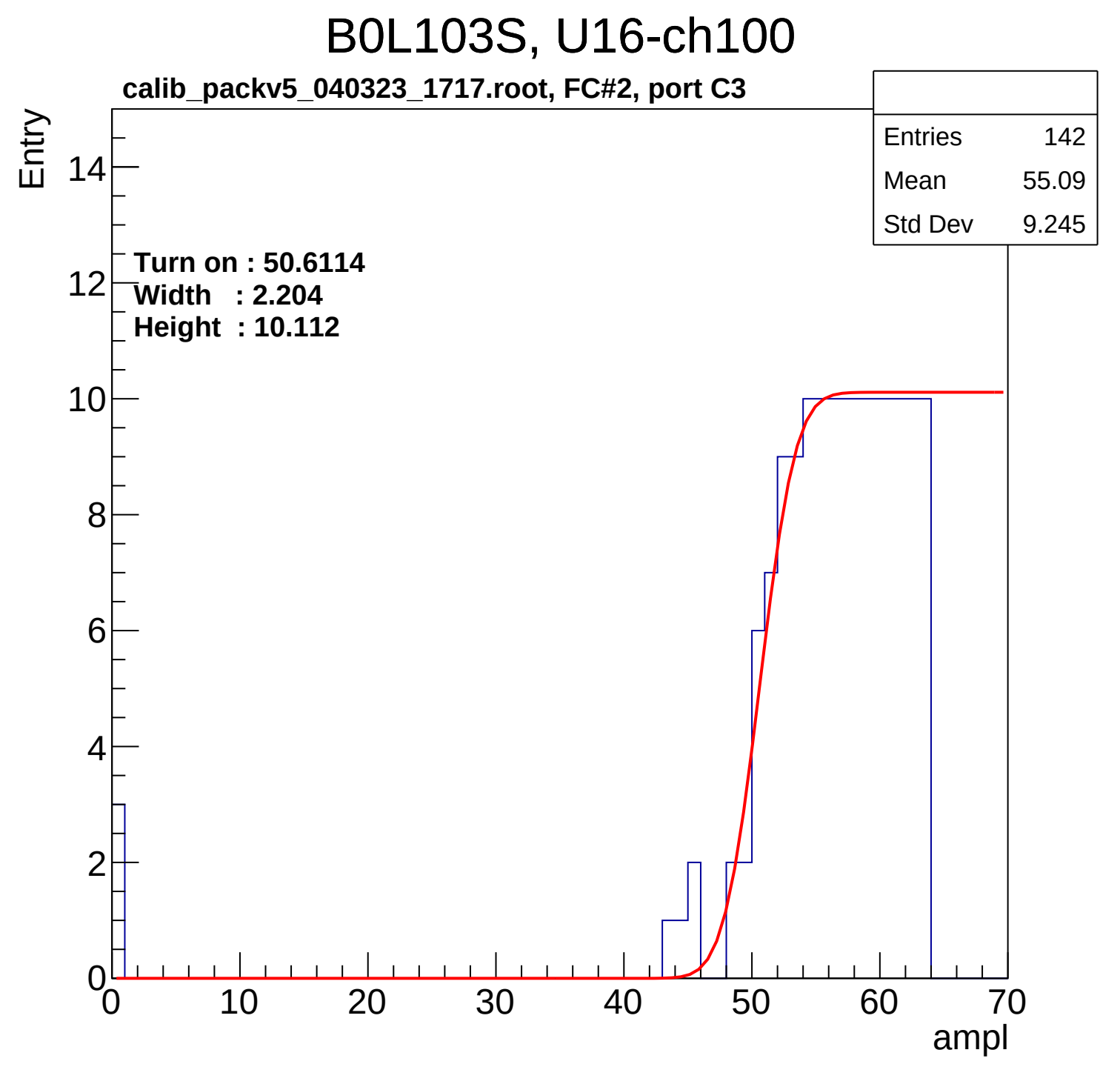
B0L103S, U16-ch100
calib_packv5_040323_1717.root, FC#2, port C3
Entries 142
Mean 55.09
Std Dev 9.245
Turn on : 50.6114
Width : 2.204
Height : 10.112
Entry
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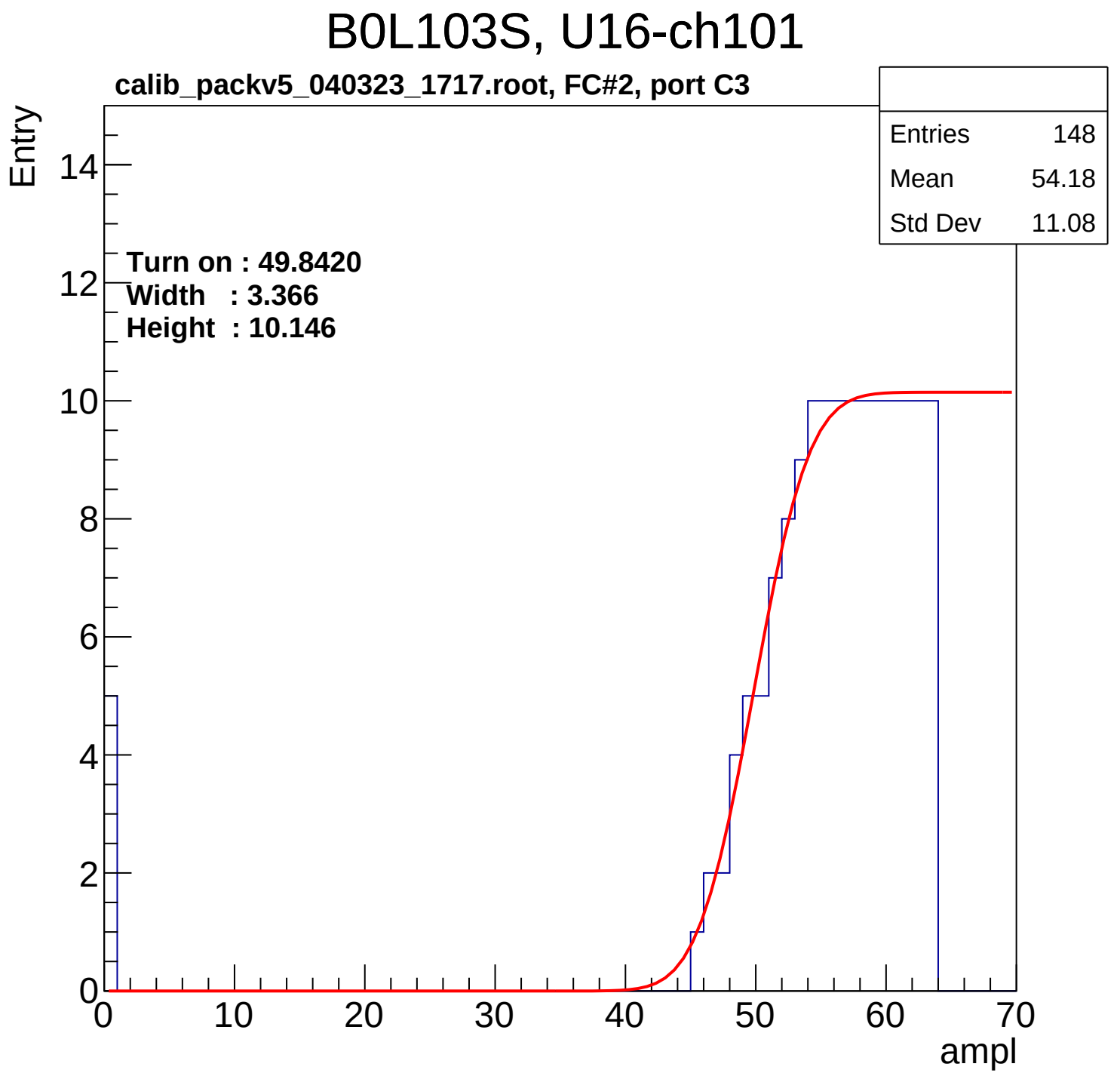
B0L103S, U16-ch101
calib_packv5_040323_1717.root, FC#2, port C3
Entries 148
Mean 54.18
Std Dev 11.08
Turn on : 49.8420
Width : 3.366
Height : 10.146
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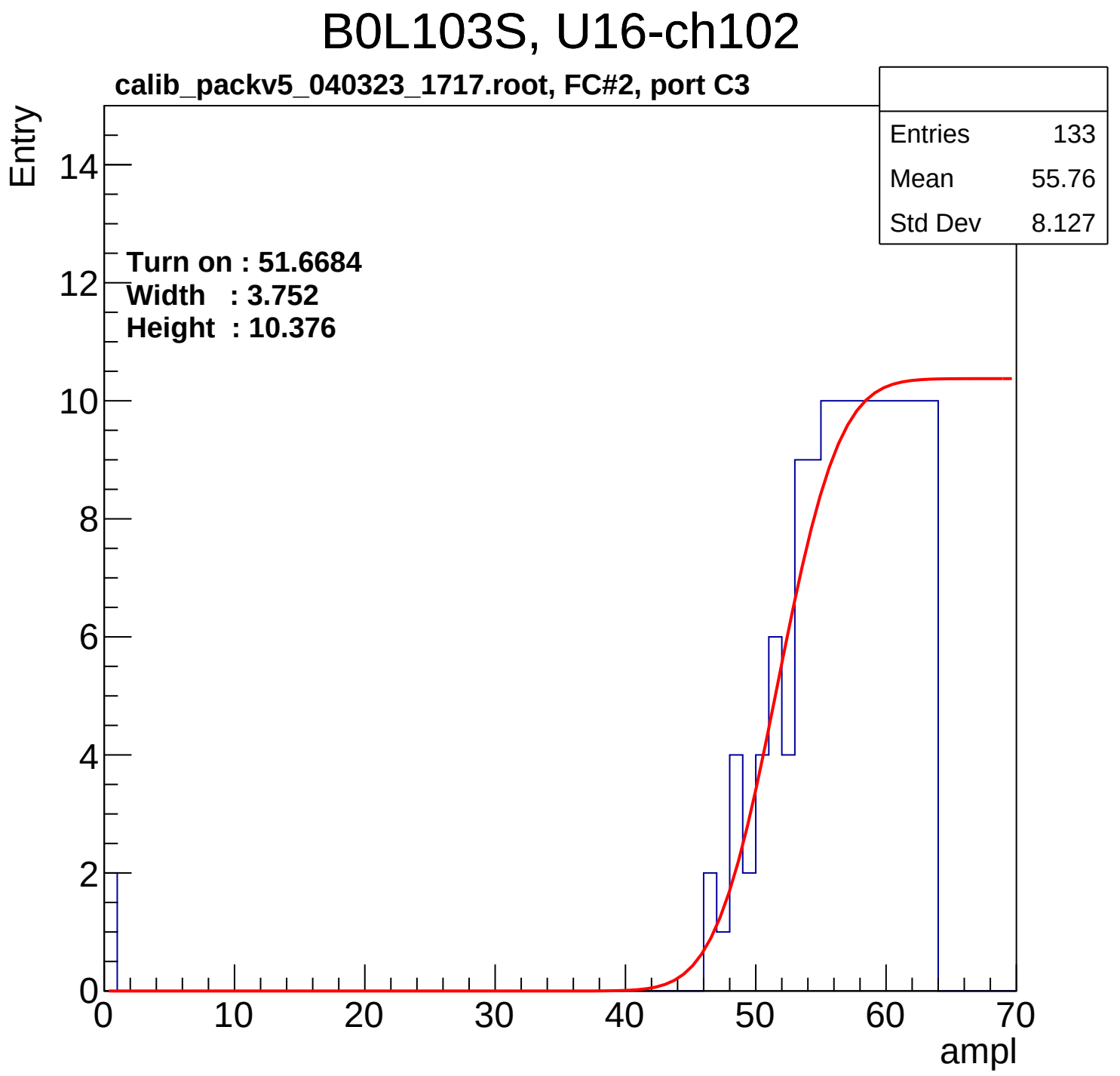
B0L103S, U16-ch102
calib_packv5_040323_1717.root, FC#2, port C3
Entries 133
Mean 55.76
Std Dev 8.127
Turn on : 51.6684
Width : 3.752
Height : 10.376
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ampl
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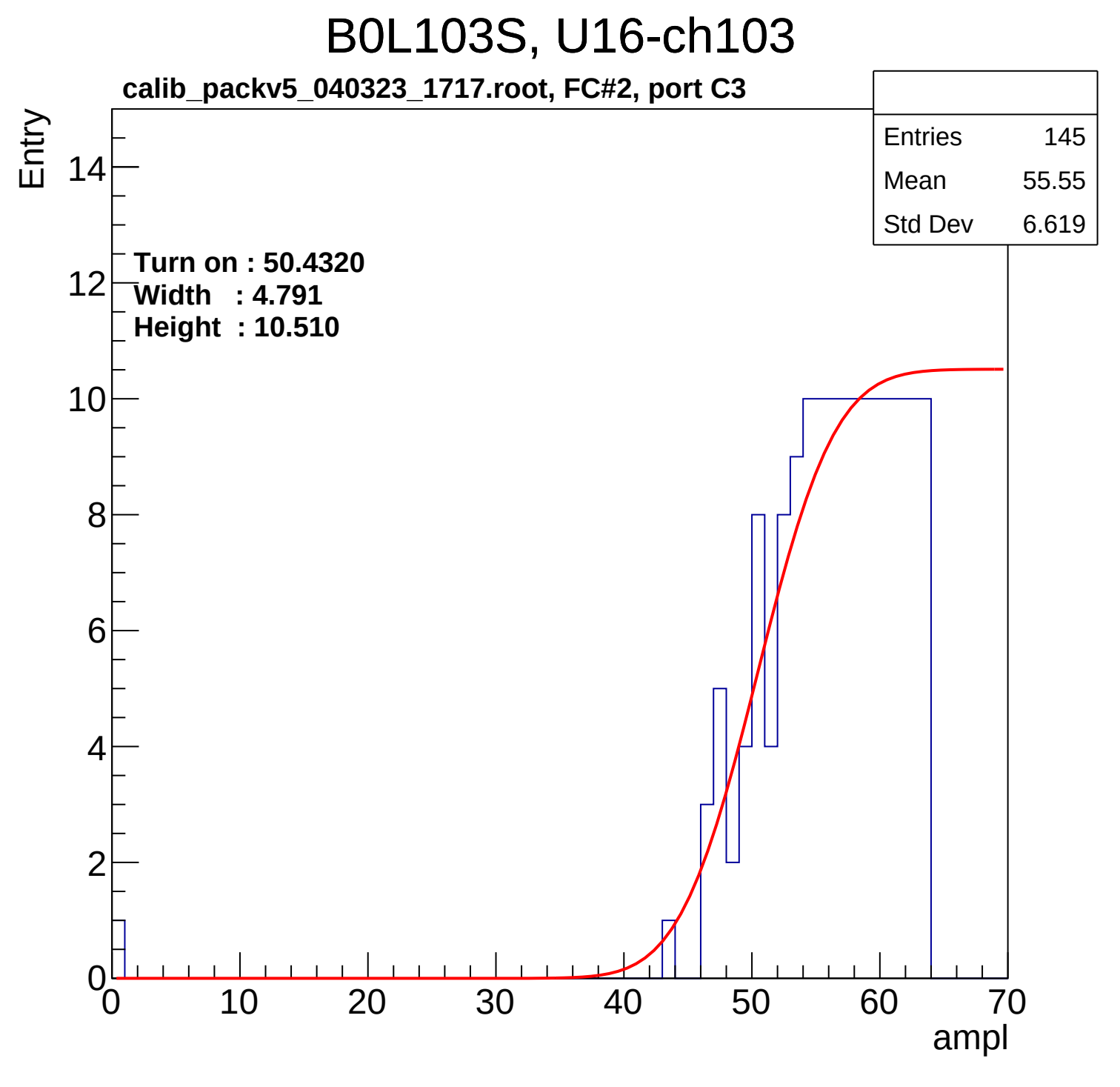
B0L103S, U16-ch103
calib_packv5_040323_1717.root, FC#2, port C3
Entries 145
Mean 55.55
Std Dev 6.619
Turn on : 50.4320
Width : 4.791
Height : 10.510
Entry
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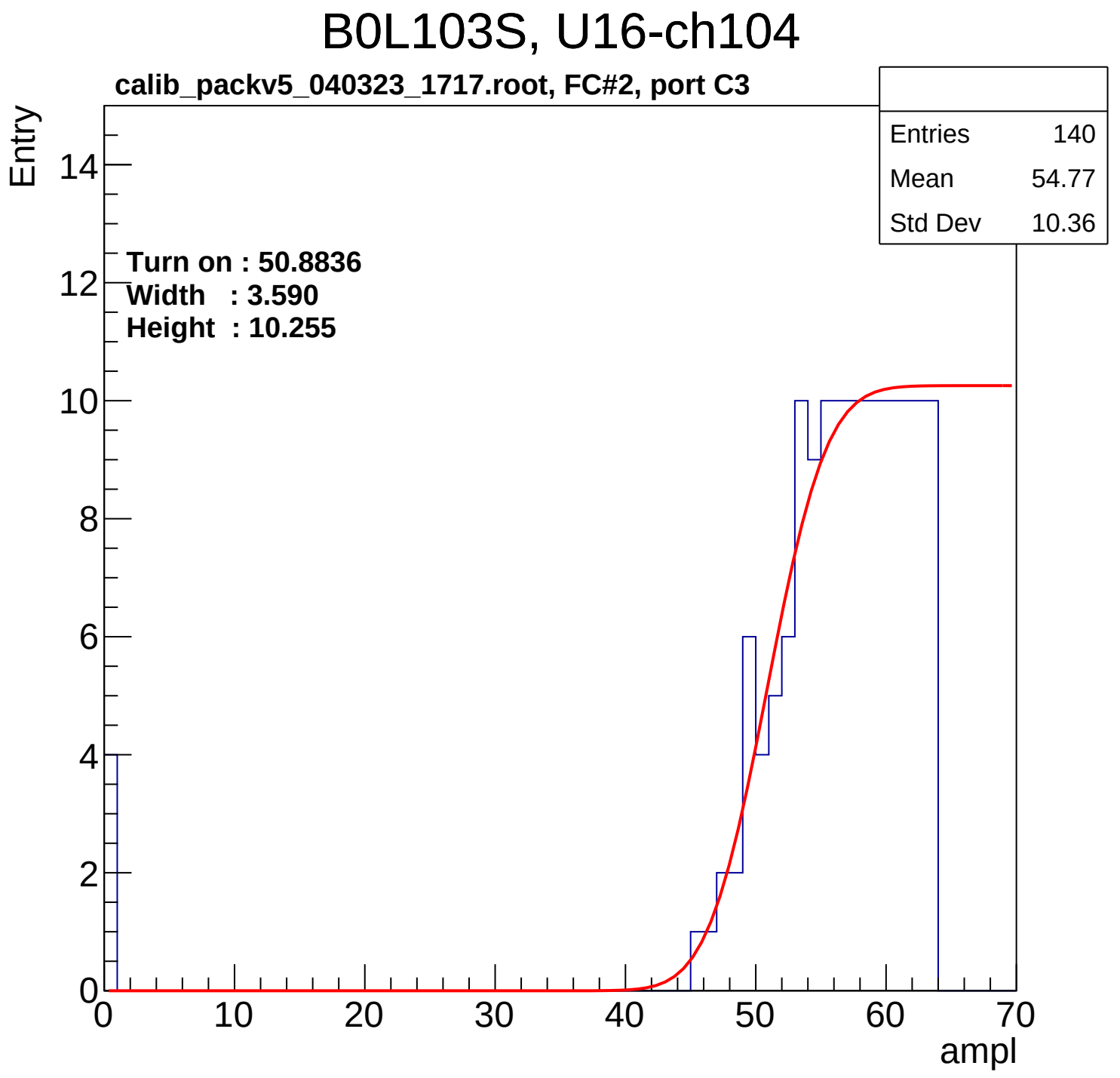
B0L103S, U16-ch104
calib_packv5_040323_1717.root, FC#2, port C3
Entries 140
Mean 54.77
Std Dev 10.36
Turn on : 50.8836
Width : 3.590
Height : 10.255
Entry
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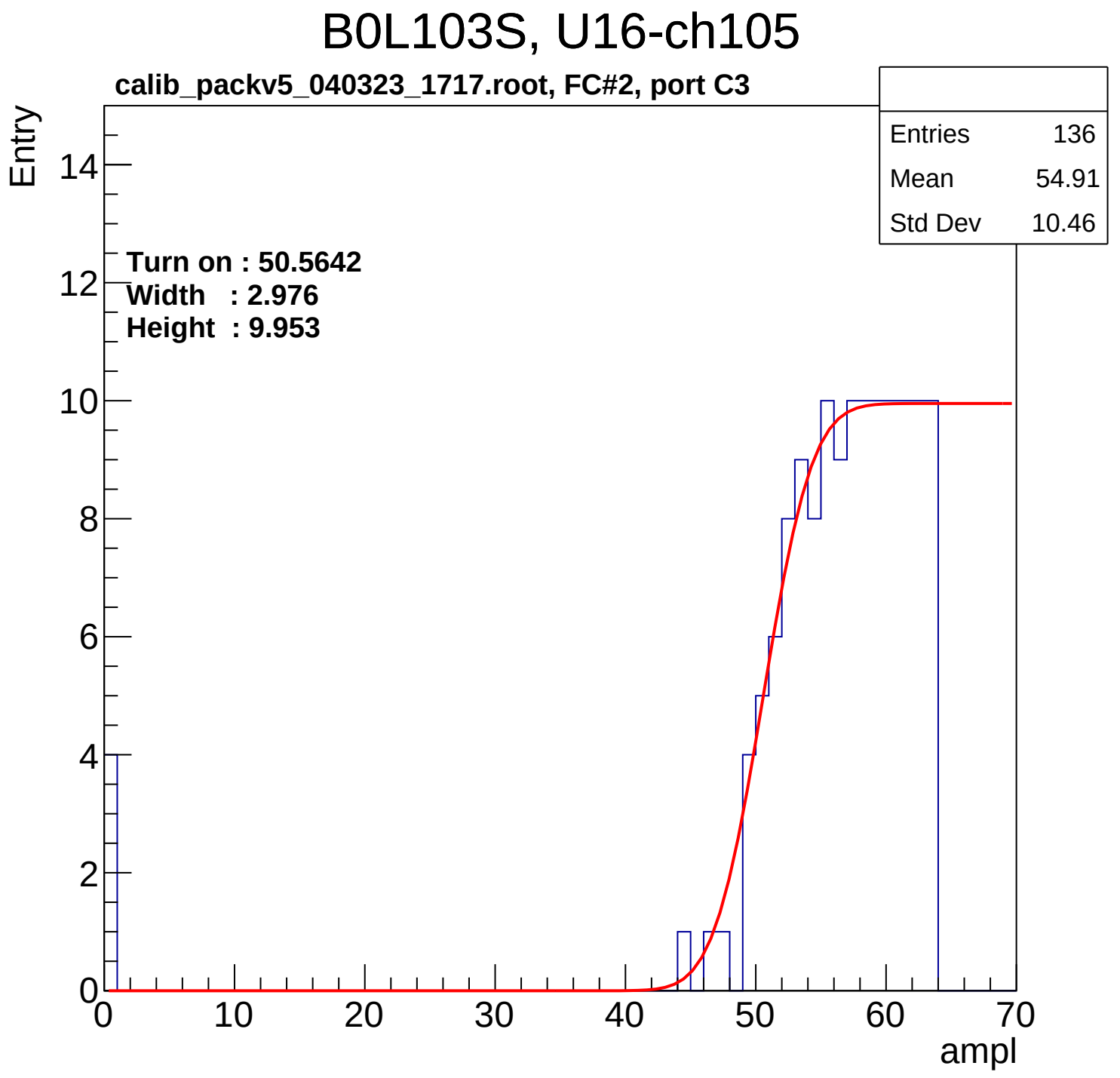
B0L103S, U16-ch105
calib_packv5_040323_1717.root, FC#2, port C3
Entries 136
Mean 54.91
Std Dev 10.46
Turn on : 50.5642
Width : 2.976
Height : 9.953
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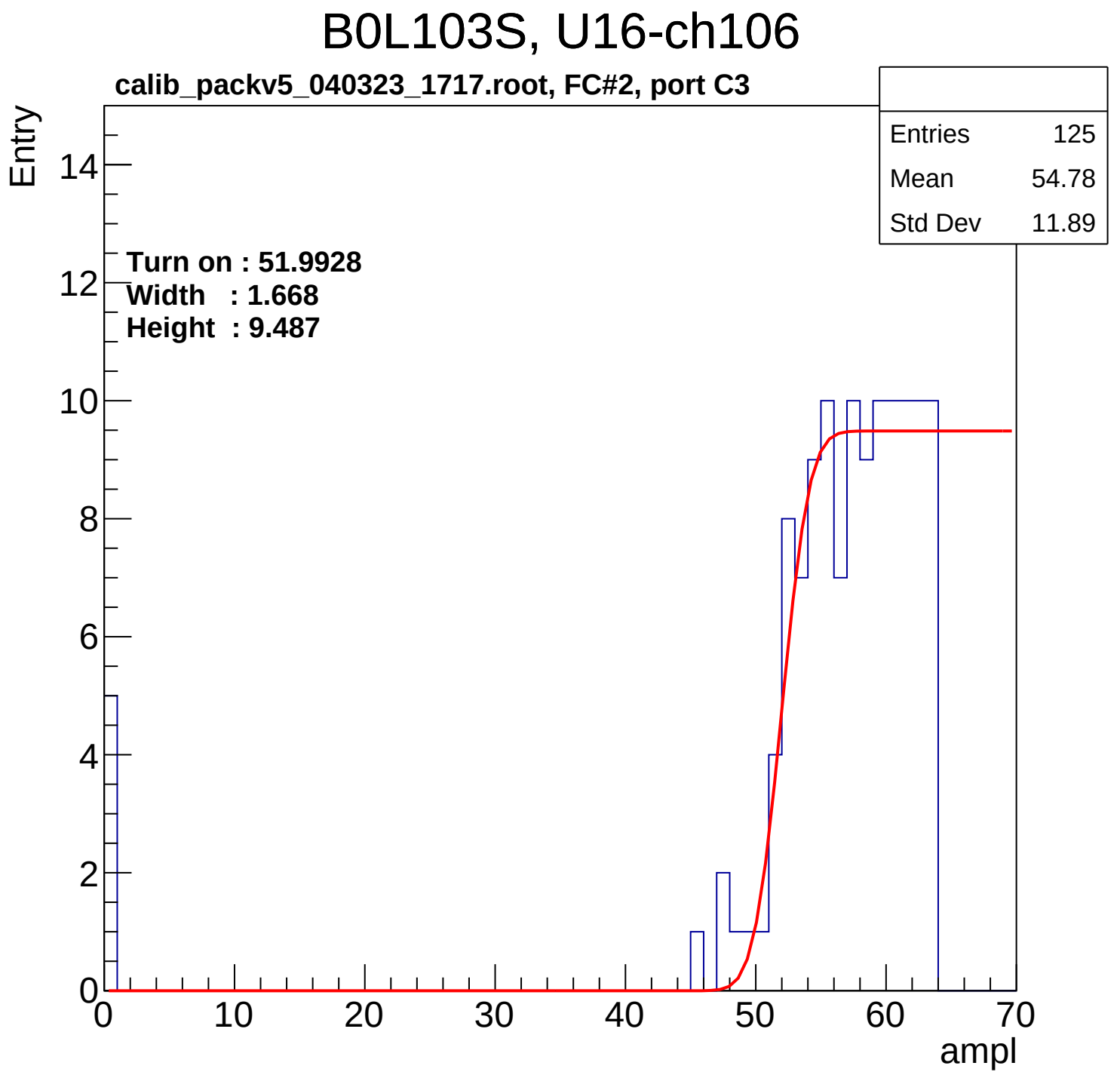
B0L103S, U16-ch106
calib_packv5_040323_1717.root, FC#2, port C3
Entries 125
Mean 54.78
Std Dev 11.89
Turn on : 51.9928
Width : 1.668
Height : 9.487
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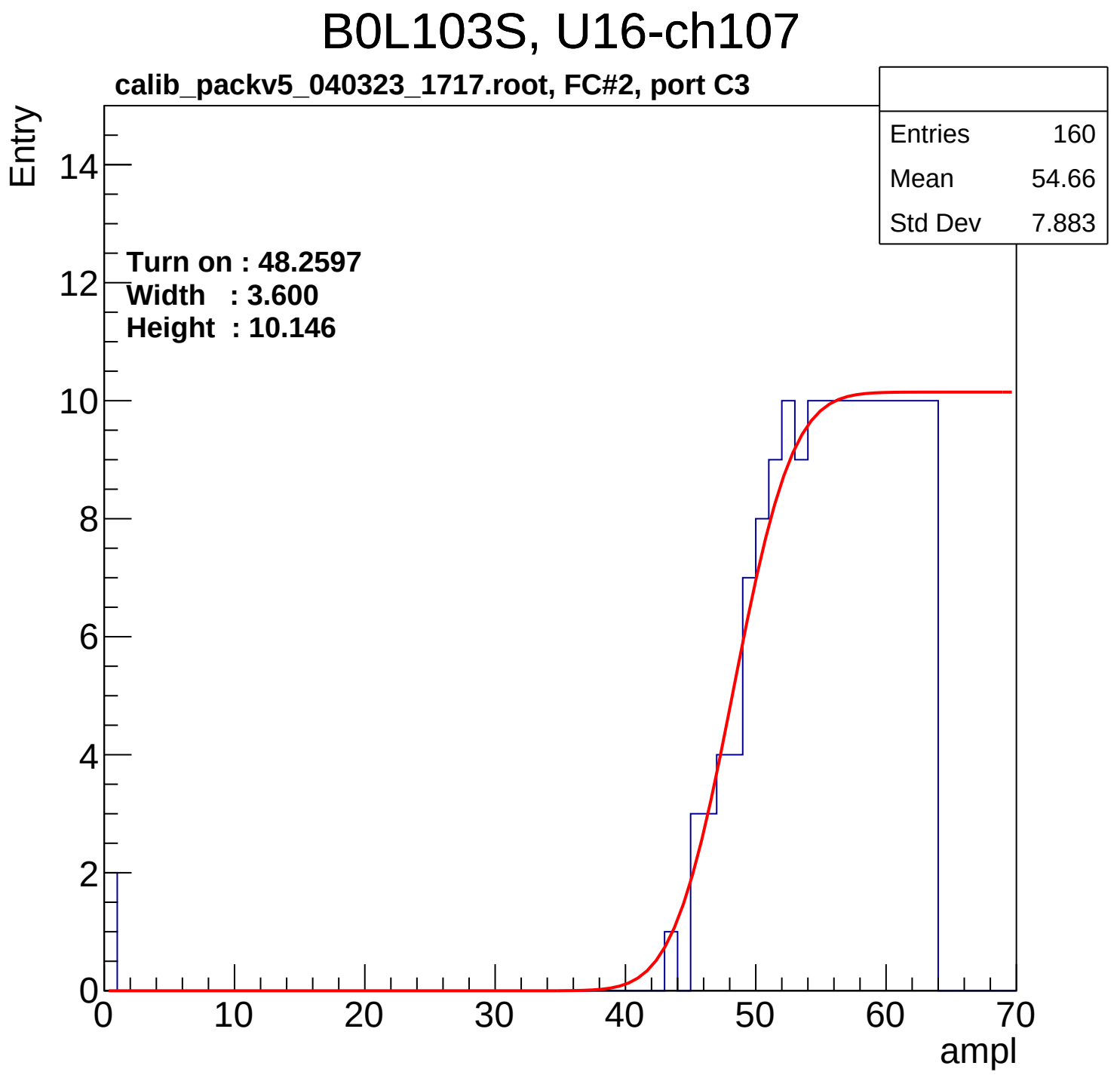
B0L103S, U16-ch107
calib_packv5_040323_1717.root, FC#2, port C3
Entries 160
Mean 54.66
Std Dev 7.883
Turn on : 48.2597
Width : 3.600
Height : 10.146
Entry
ampl
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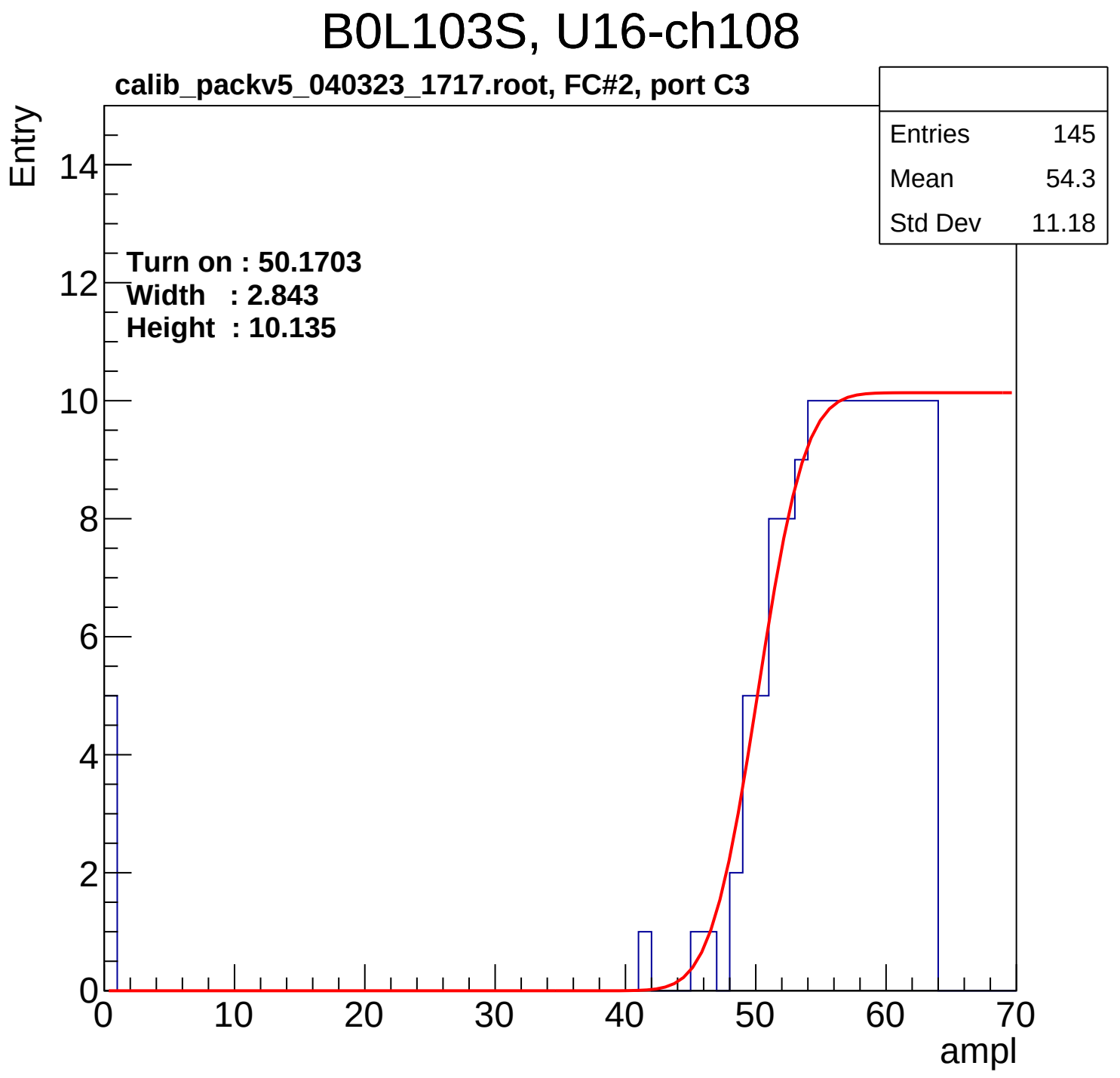
B0L103S, U16-ch108
calib_packv5_040323_1717.root, FC#2, port C3
Entries 145
Mean 54.3
Std Dev 11.18
Turn on : 50.1703
Width : 2.843
Height : 10.135
Entry
ampl
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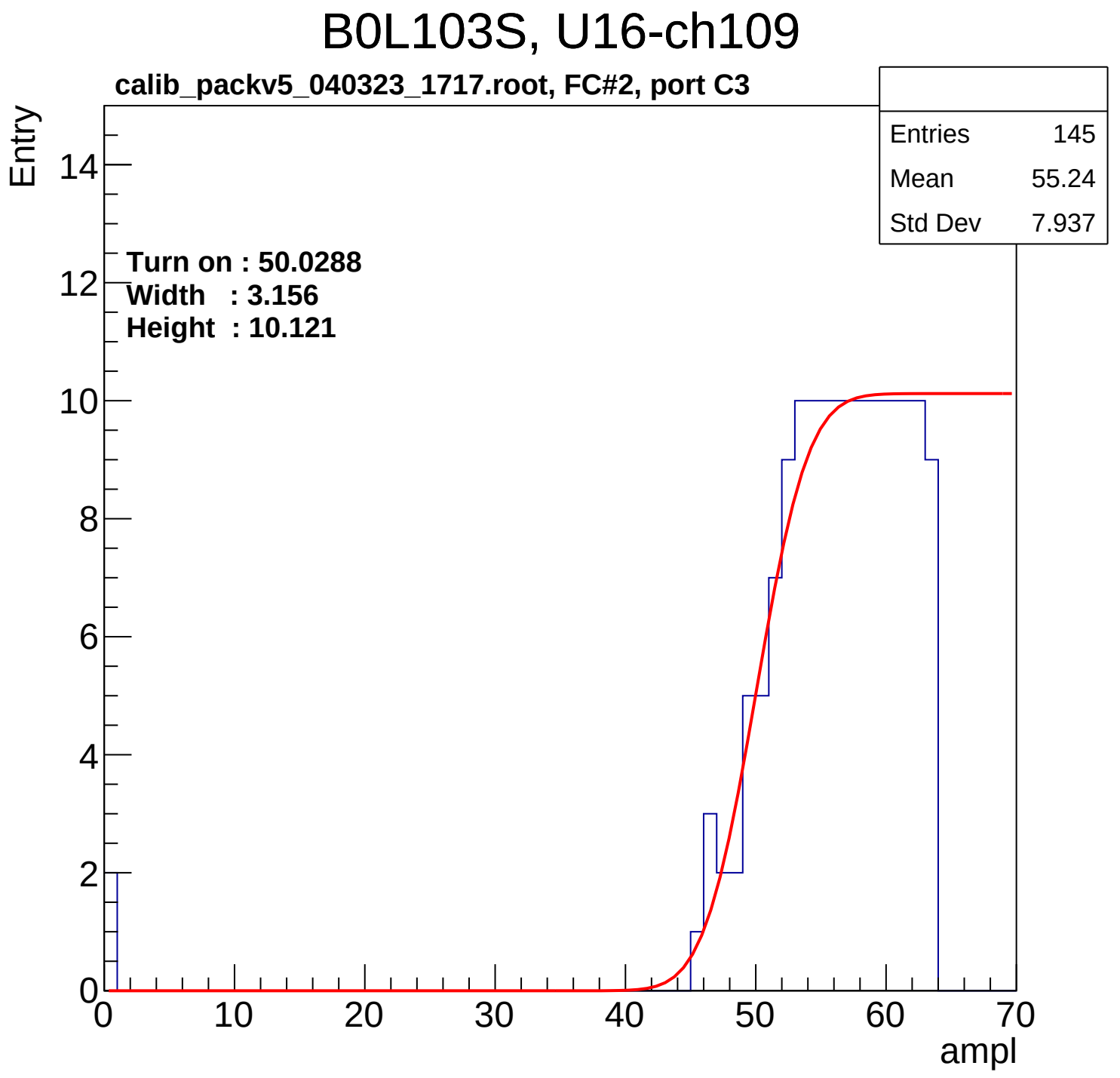
B0L103S, U16-ch109
calib_packv5_040323_1717.root, FC#2, port C3
Entries 145
Mean 55.24
Std Dev 7.937
Turn on : 50.0288
Width : 3.156
Height : 10.121
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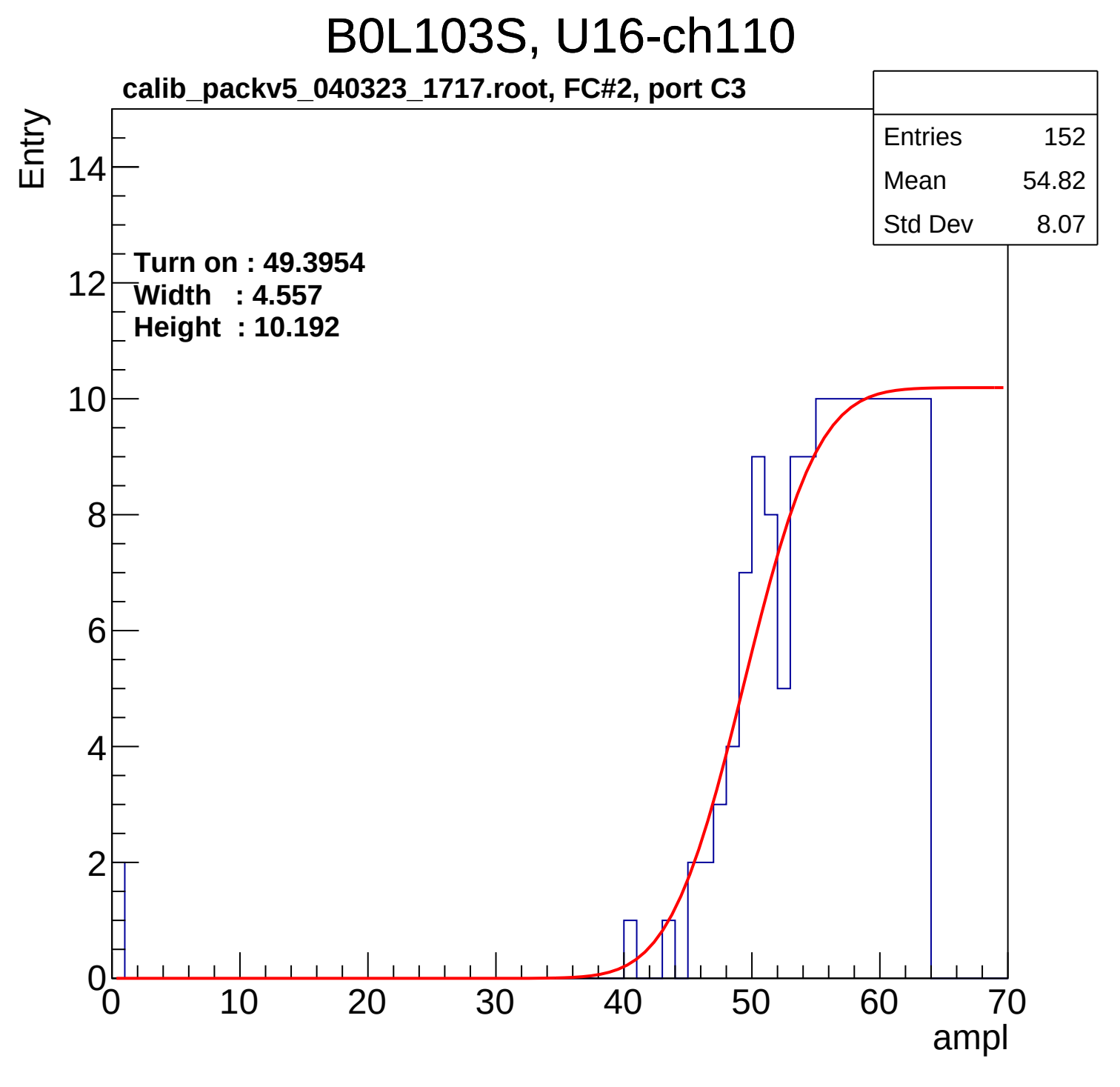
B0L103S, U16-ch110
calib_packv5_040323_1717.root, FC#2, port C3
Entries 152
Mean 54.82
Std Dev 8.07
Turn on : 49.3954
Width : 4.557
Height : 10.192
Entry
ampl
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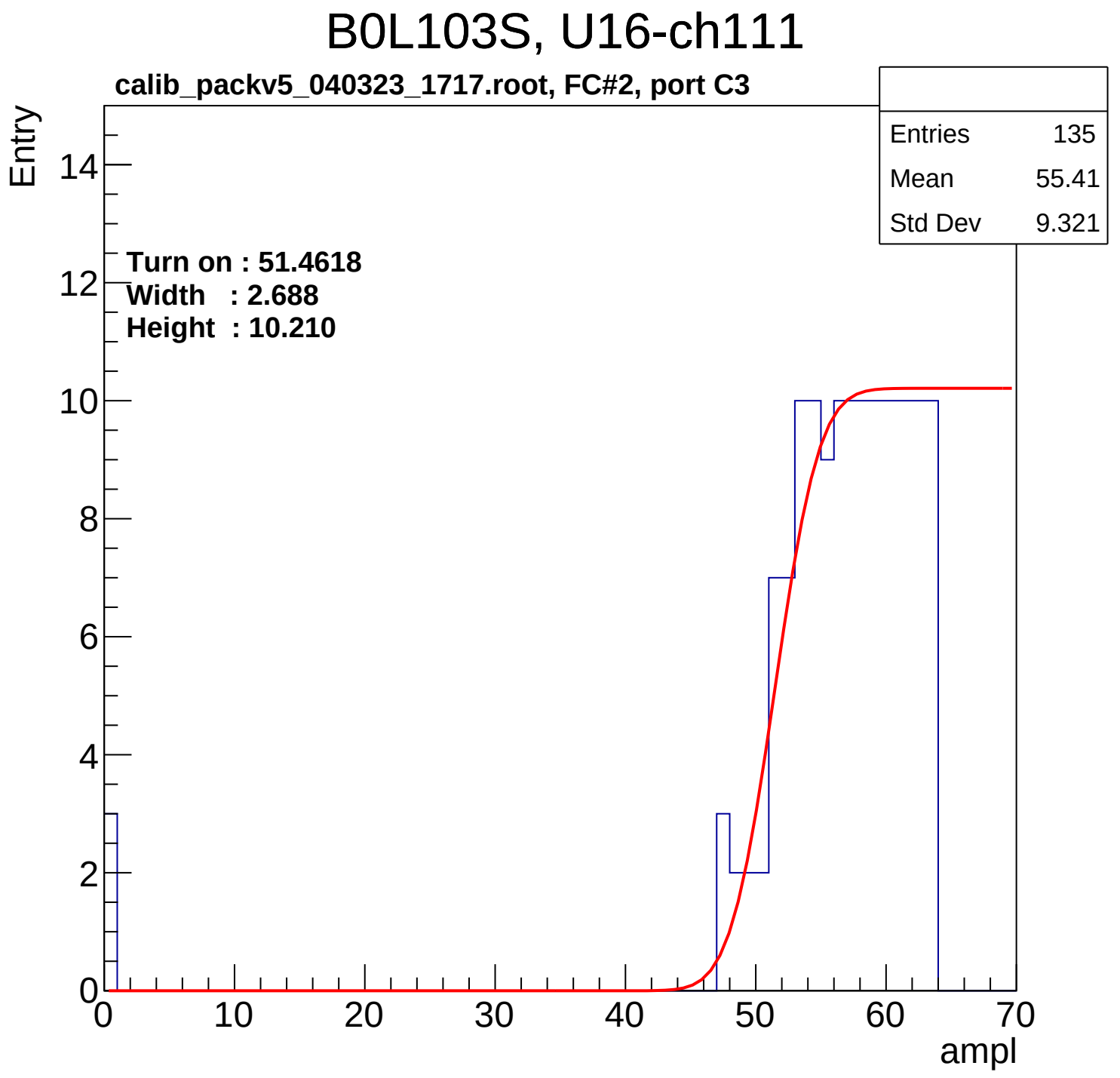
B0L103S, U16-ch111
calib_packv5_040323_1717.root, FC#2, port C3
Entries 135
Mean 55.41
Std Dev 9.321
Turn on : 51.4618
Width : 2.688
Height : 10.210
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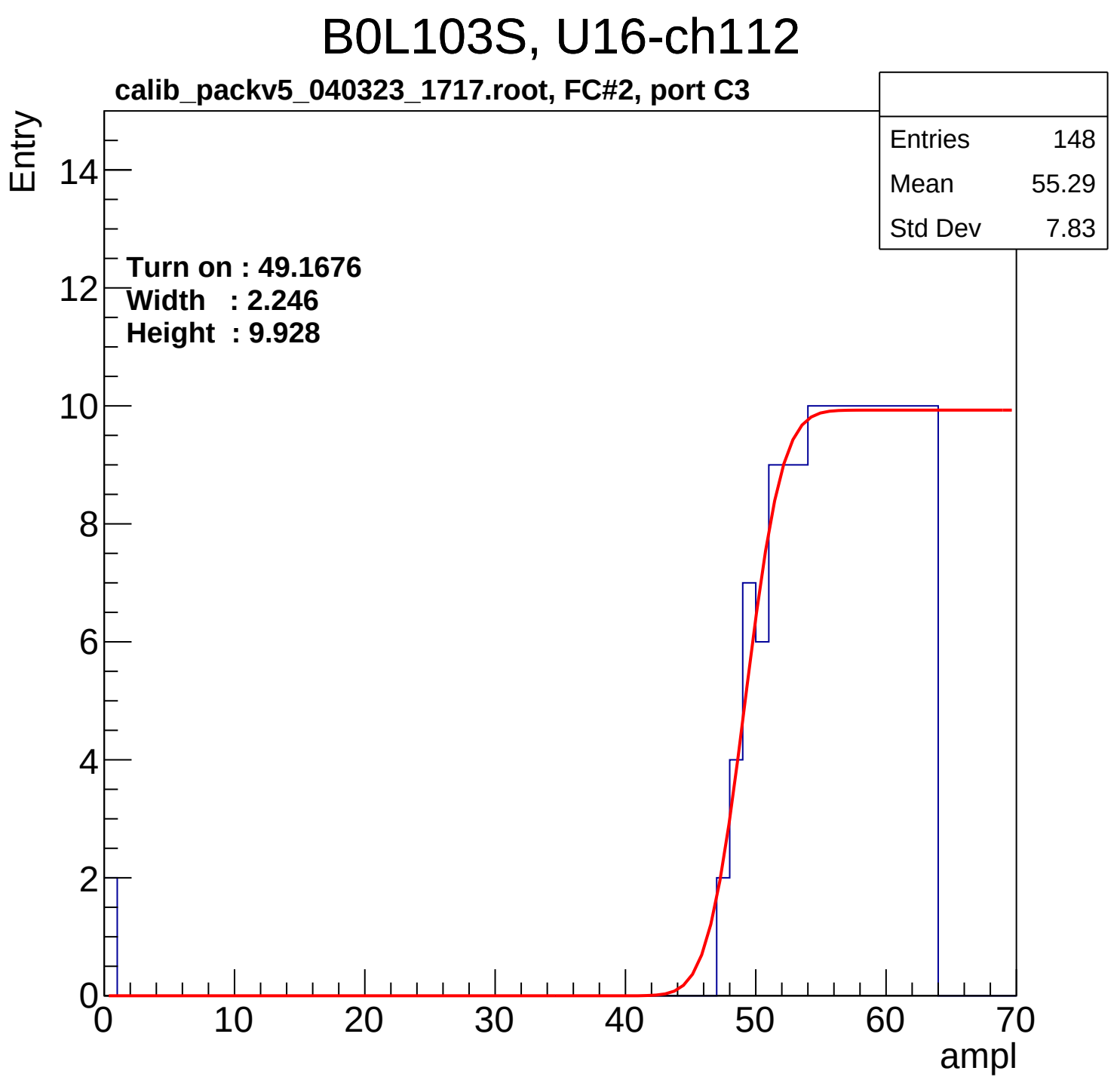
B0L103S, U16-ch112
calib_packv5_040323_1717.root, FC#2, port C3
Entries 148
Mean 55.29
Std Dev 7.83
Turn on : 49.1676
Width : 2.246
Height : 9.928
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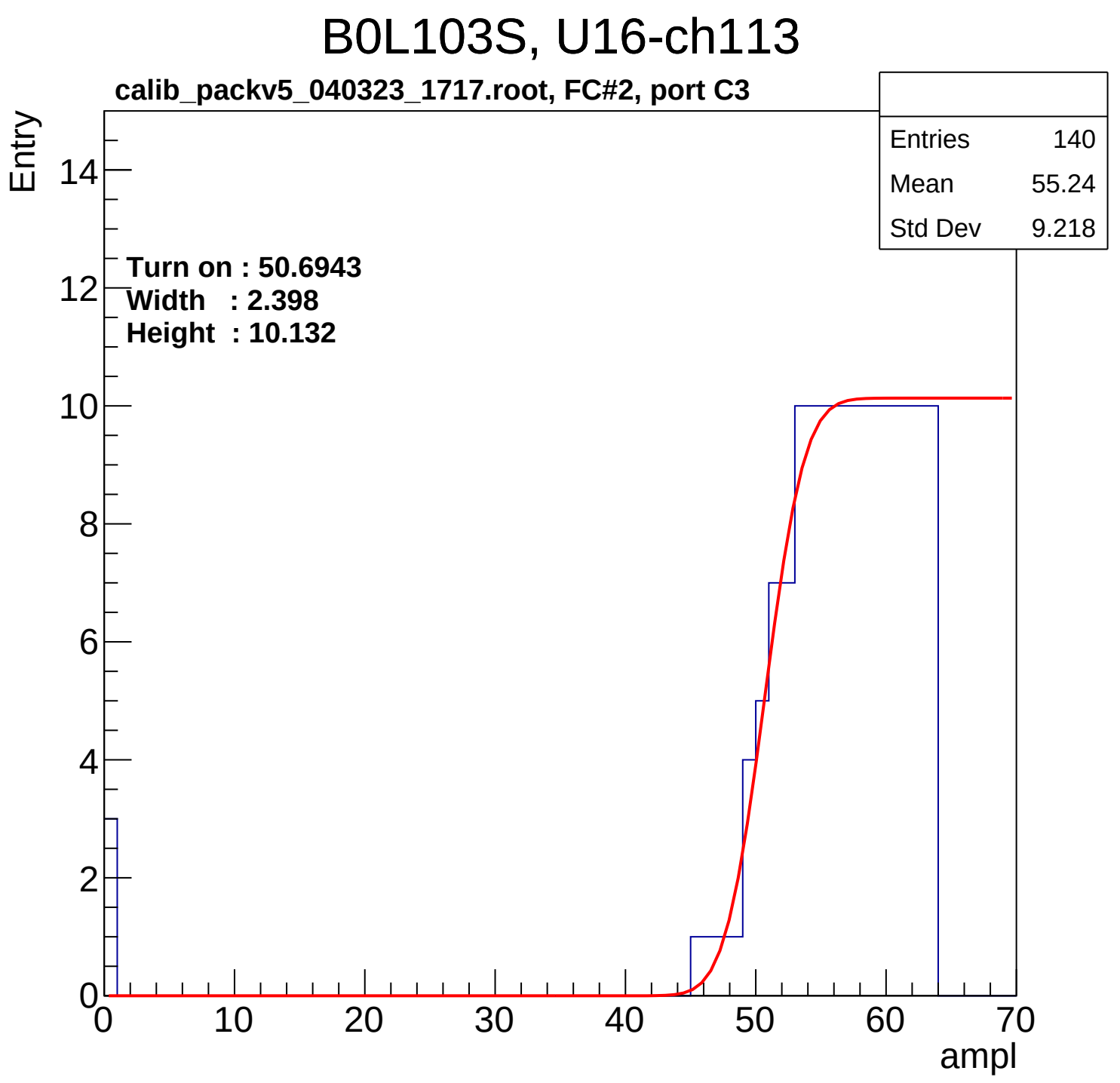
B0L103S, U16-ch113
calib_packv5_040323_1717.root, FC#2, port C3
Entries 140
Mean 55.24
Std Dev 9.218
Turn on : 50.6943
Width : 2.398
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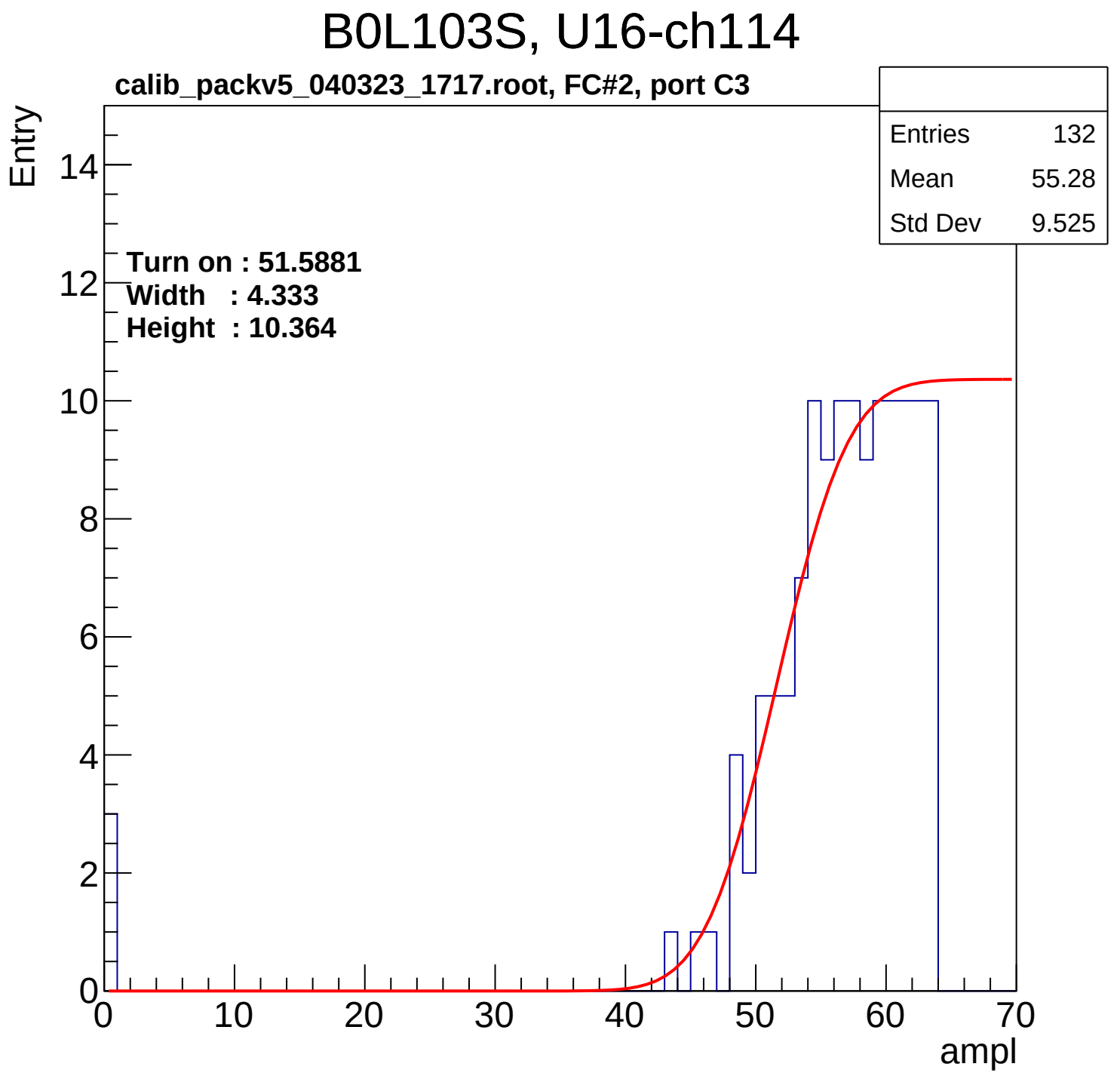
B0L103S, U16-ch114
calib_packv5_040323_1717.root, FC#2, port C3
Entries 132
Mean 55.28
Std Dev 9.525
Turn on : 51.5881
Width : 4.333
Height : 10.364
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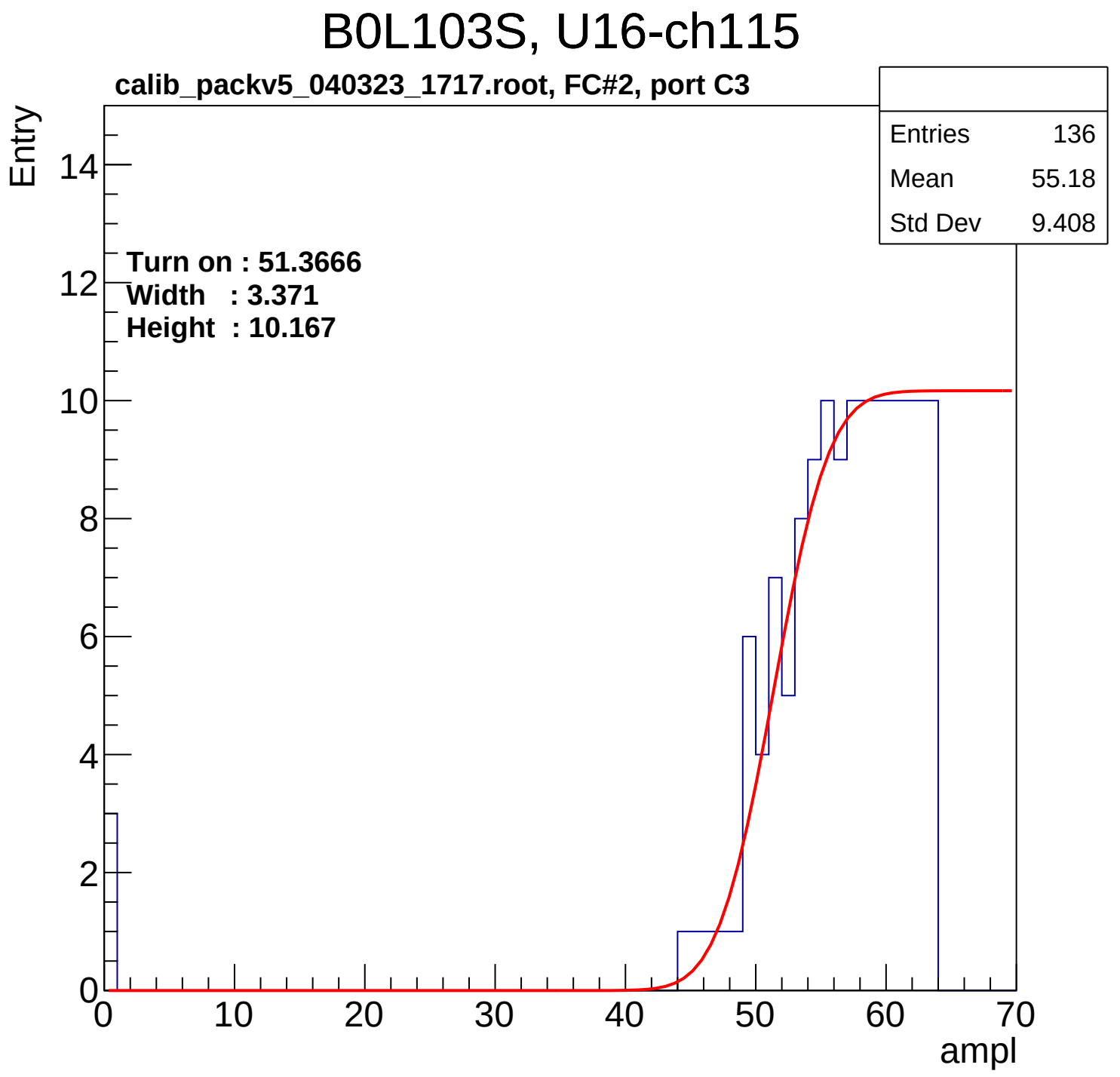
B0L103S, U16-ch115
calib_packv5_040323_1717.root, FC#2, port C3
Entries 136
Mean 55.18
Std Dev 9.408
Turn on : 51.3666
Width : 3.371
Height : 10.167
Entry
ampl
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4
6
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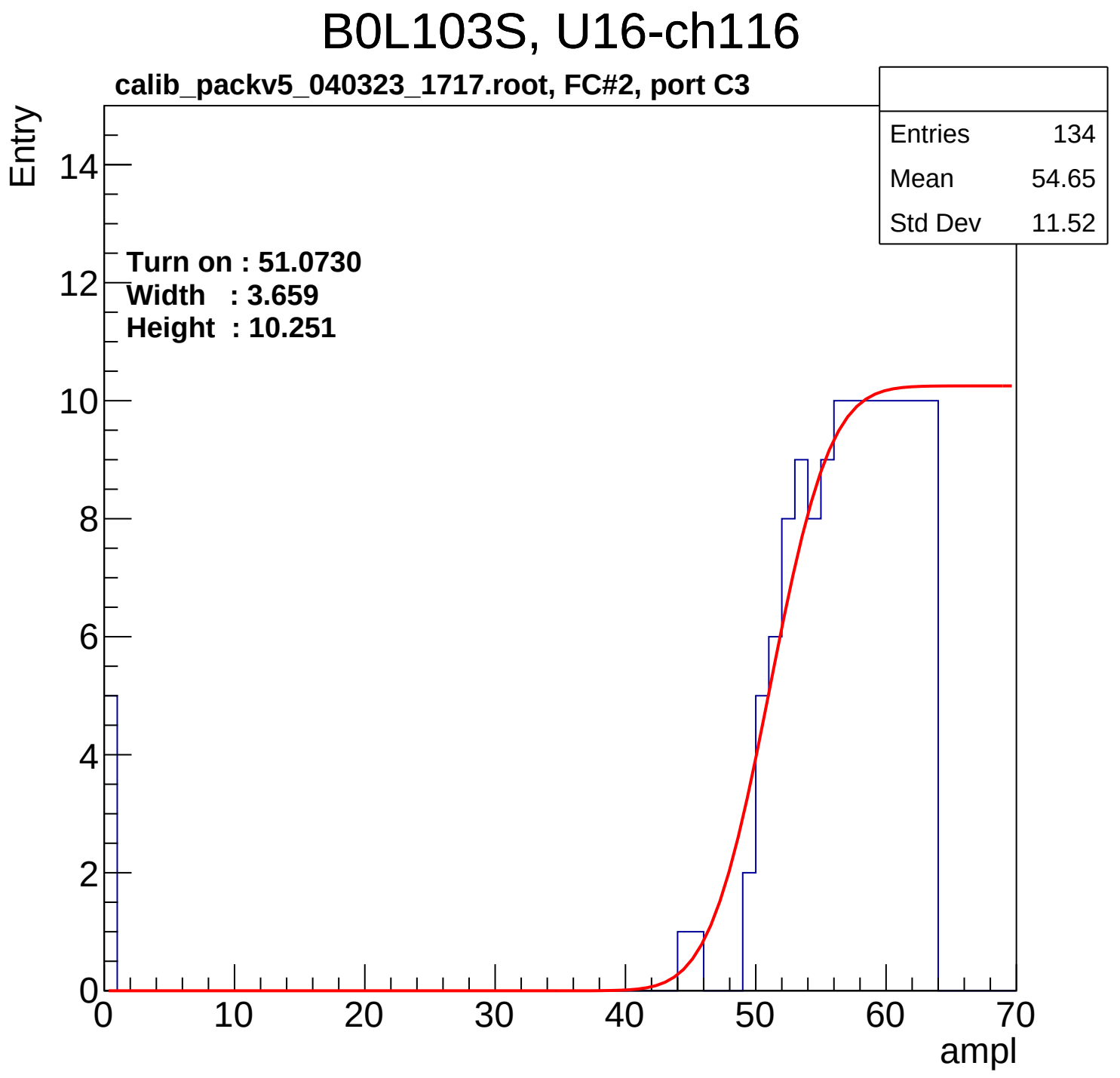
B0L103S, U16-ch116
calib_packv5_040323_1717.root, FC#2, port C3
Entries 134
Mean 54.65
Std Dev 11.52
Turn on : 51.0730
Width : 3.659
Height : 10.251
Entry
ampl
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4
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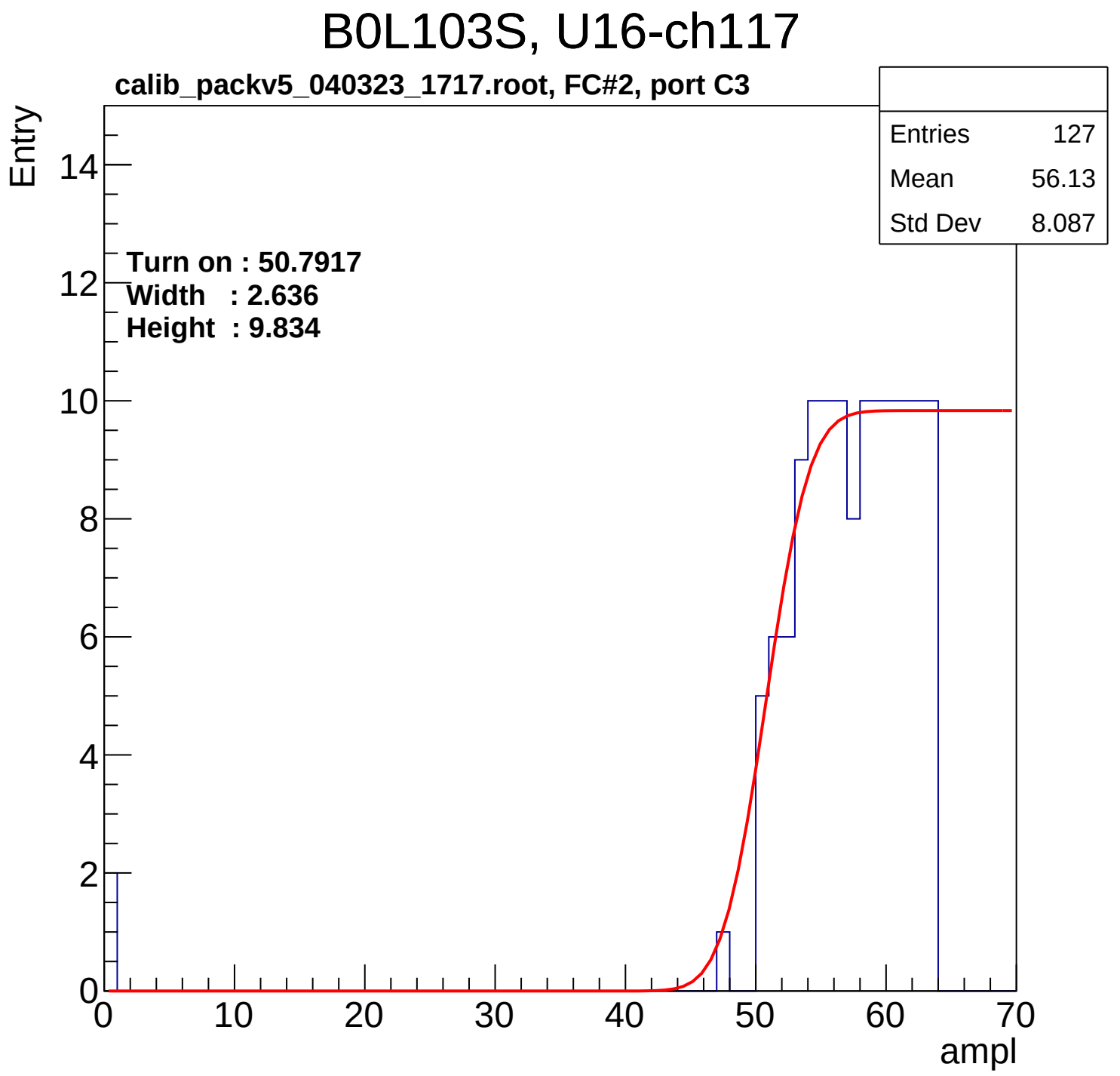
B0L103S, U16-ch117
calib_packv5_040323_1717.root, FC#2, port C3
Entries 127
Mean 56.13
Std Dev 8.087
Turn on : 50.7917
Width : 2.636
Height : 9.834
Entry
ampl
0
2
4
6
8
10
12
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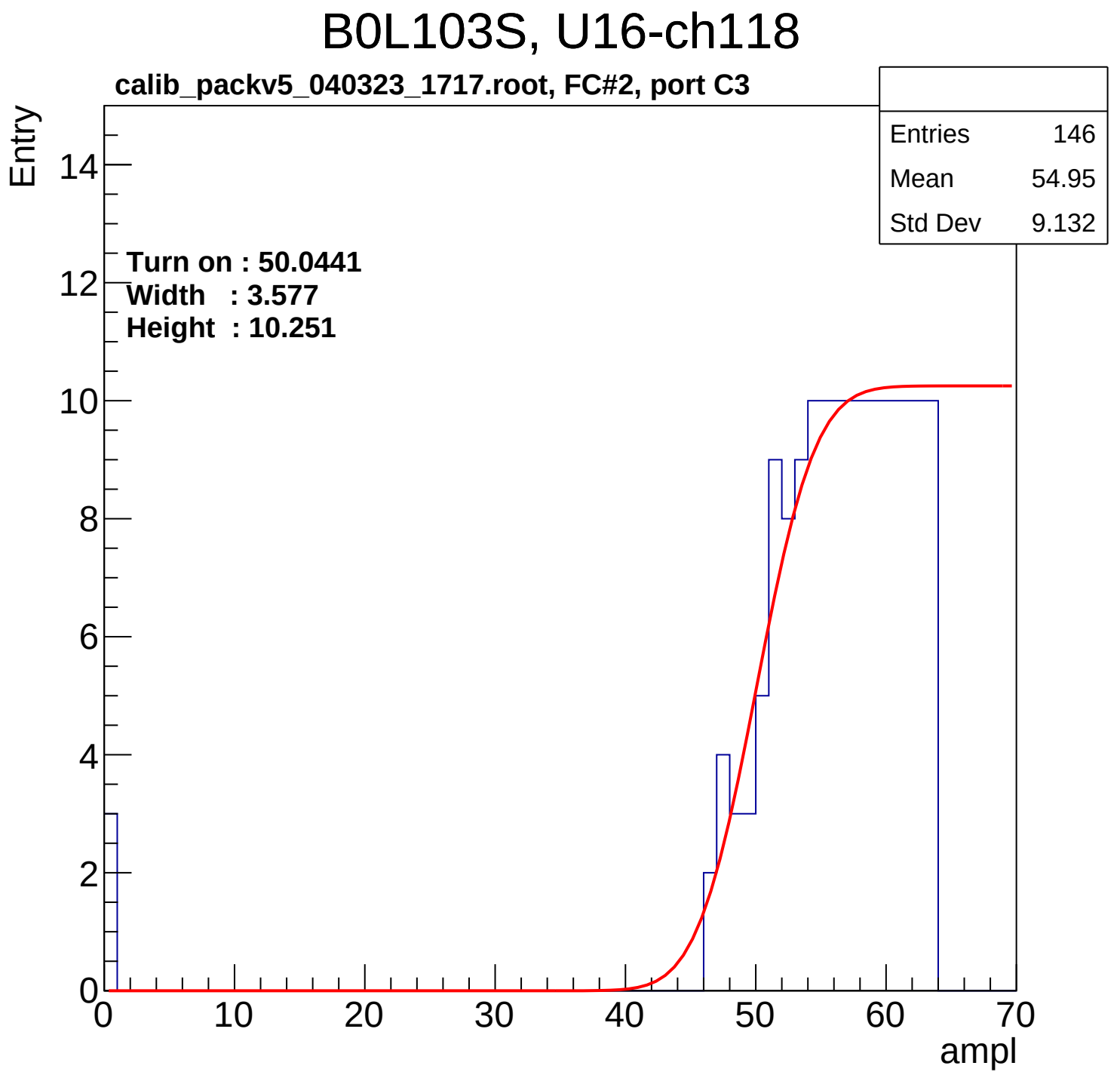
B0L103S, U16-ch118
calib_packv5_040323_1717.root, FC#2, port C3
Entries 146
Mean 54.95
Std Dev 9.132
Turn on : 50.0441
Width : 3.577
Height : 10.251
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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40
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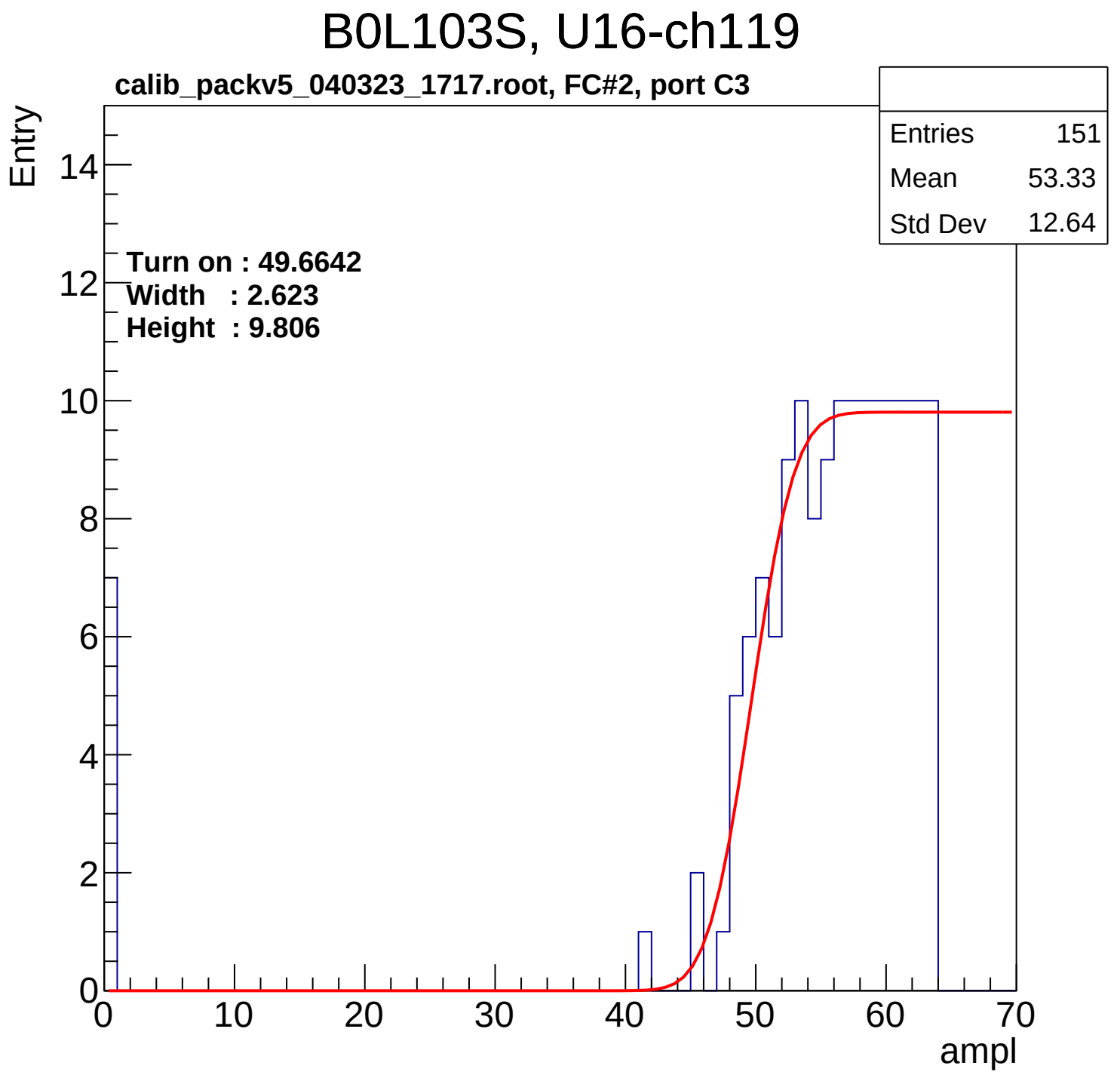
B0L103S, U16-ch119
calib_packv5_040323_1717.root, FC#2, port C3
Entries 151
Mean 53.33
Std Dev 12.64
Turn on : 49.6642
Width : 2.623
Height : 9.806
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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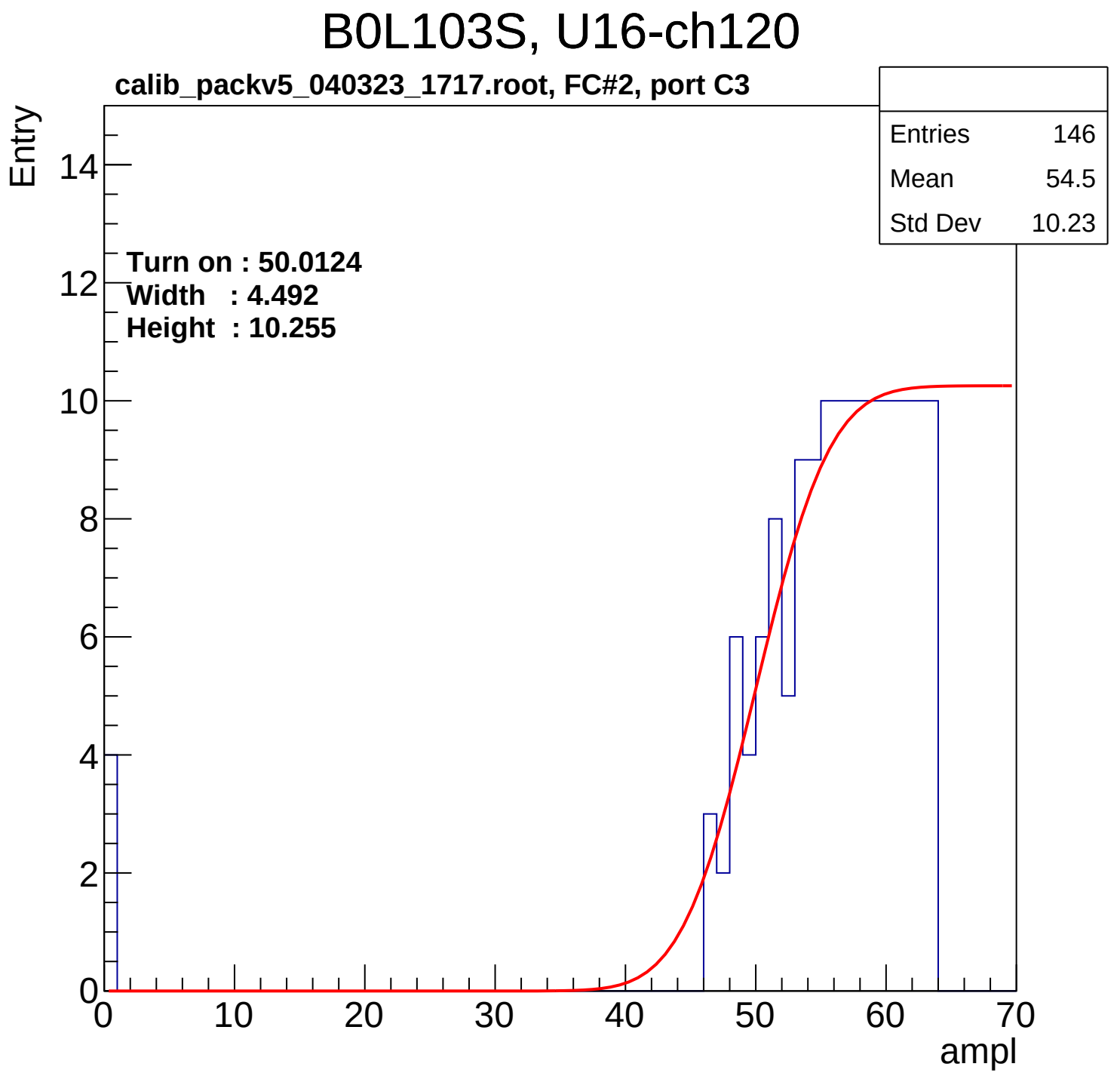
B0L103S, U16-ch120
calib_packv5_040323_1717.root, FC#2, port C3
Entries 146
Mean 54.5
Std Dev 10.23
Turn on : 50.0124
Width : 4.492
Height : 10.255
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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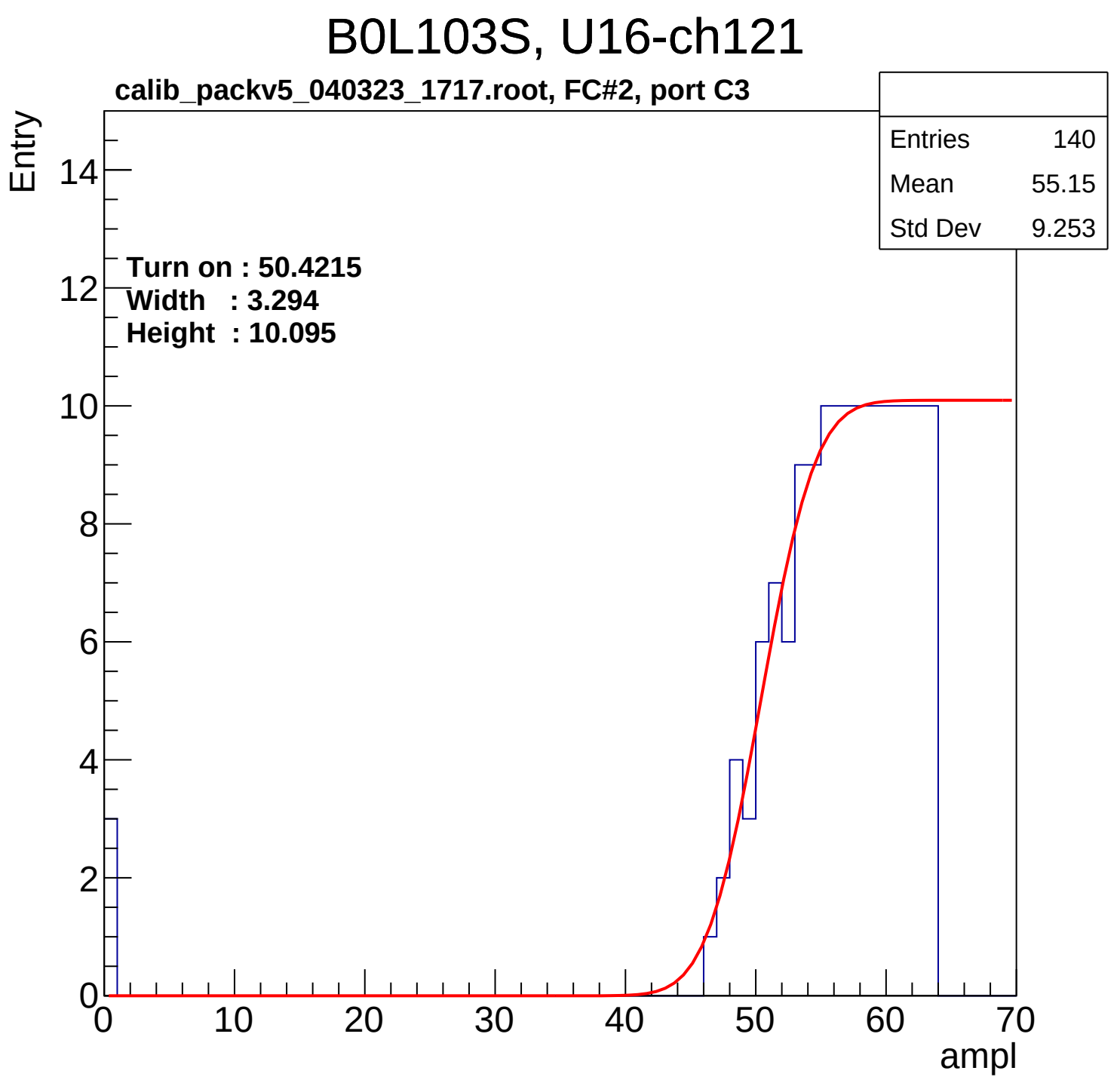
B0L103S, U16-ch121
calib_packv5_040323_1717.root, FC#2, port C3
Entries 140
Mean 55.15
Std Dev 9.253
Turn on : 50.4215
Width : 3.294
Height : 10.095
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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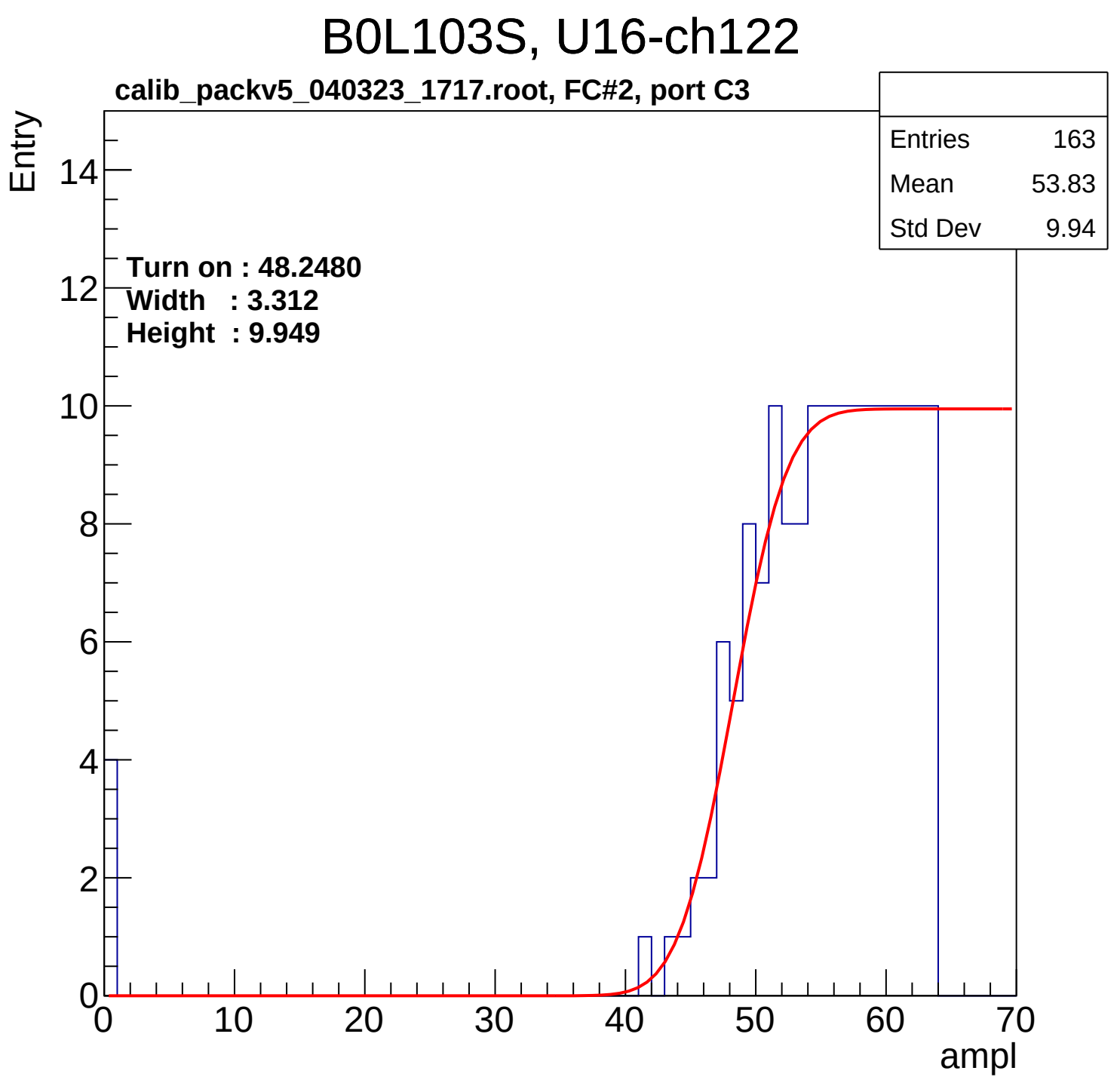
B0L103S, U16-ch122
calib_packv5_040323_1717.root, FC#2, port C3
Entries 163
Mean 53.83
Std Dev 9.94
Turn on : 48.2480
Width : 3.312
Height : 9.949
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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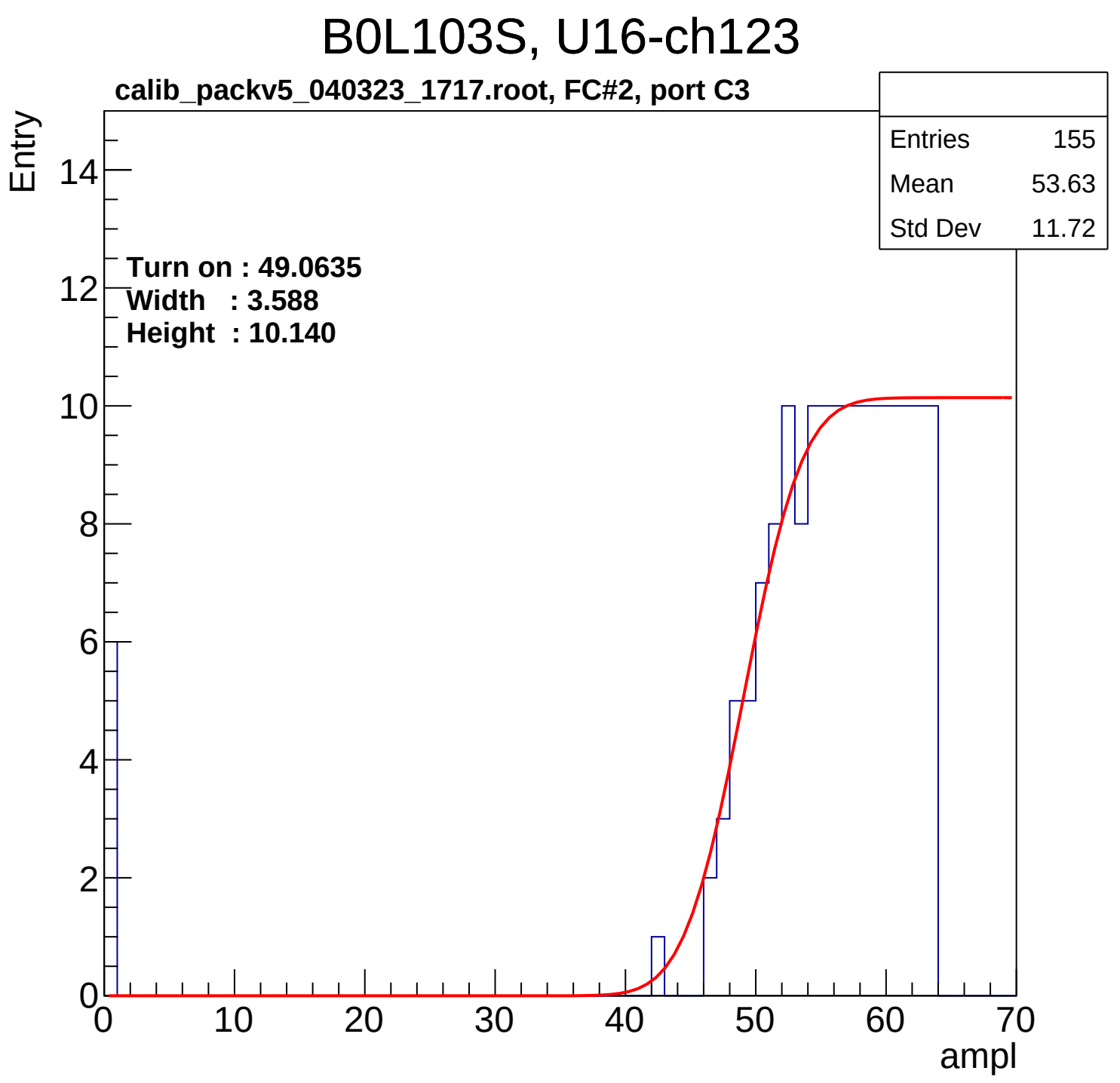
B0L103S, U16-ch123
calib_packv5_040323_1717.root, FC#2, port C3
Entries 155
Mean 53.63
Std Dev 11.72
Turn on : 49.0635
Width : 3.588
Height : 10.140
Entry
ampl
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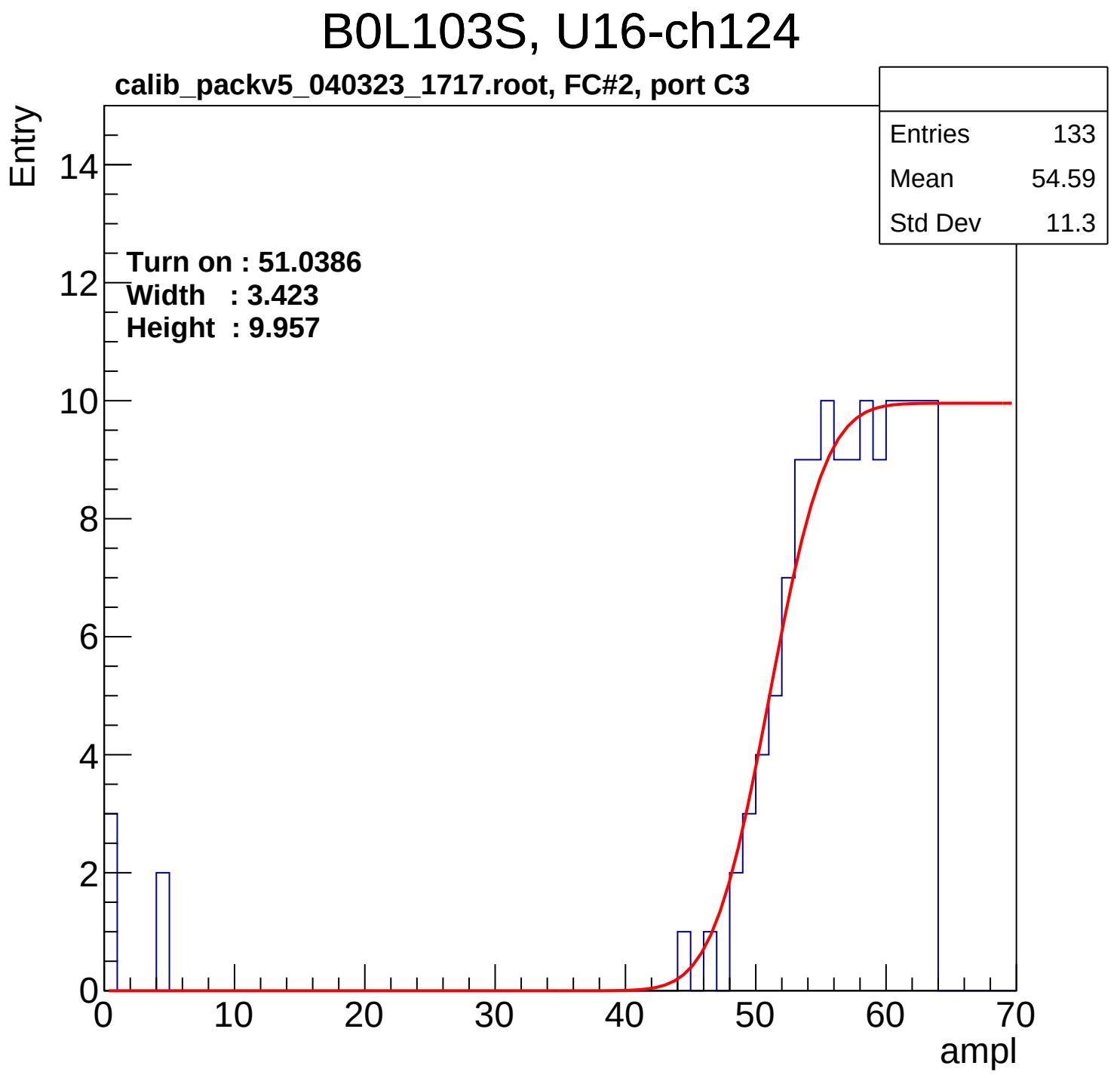
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L103S, U16-ch124
calib_packv5_040323_1717.root, FC#2, port C3
Entries 133
Mean 54.59
Std Dev 11.3
Turn on : 51.0386
Width : 3.423
Height : 9.957
Entry
ampl
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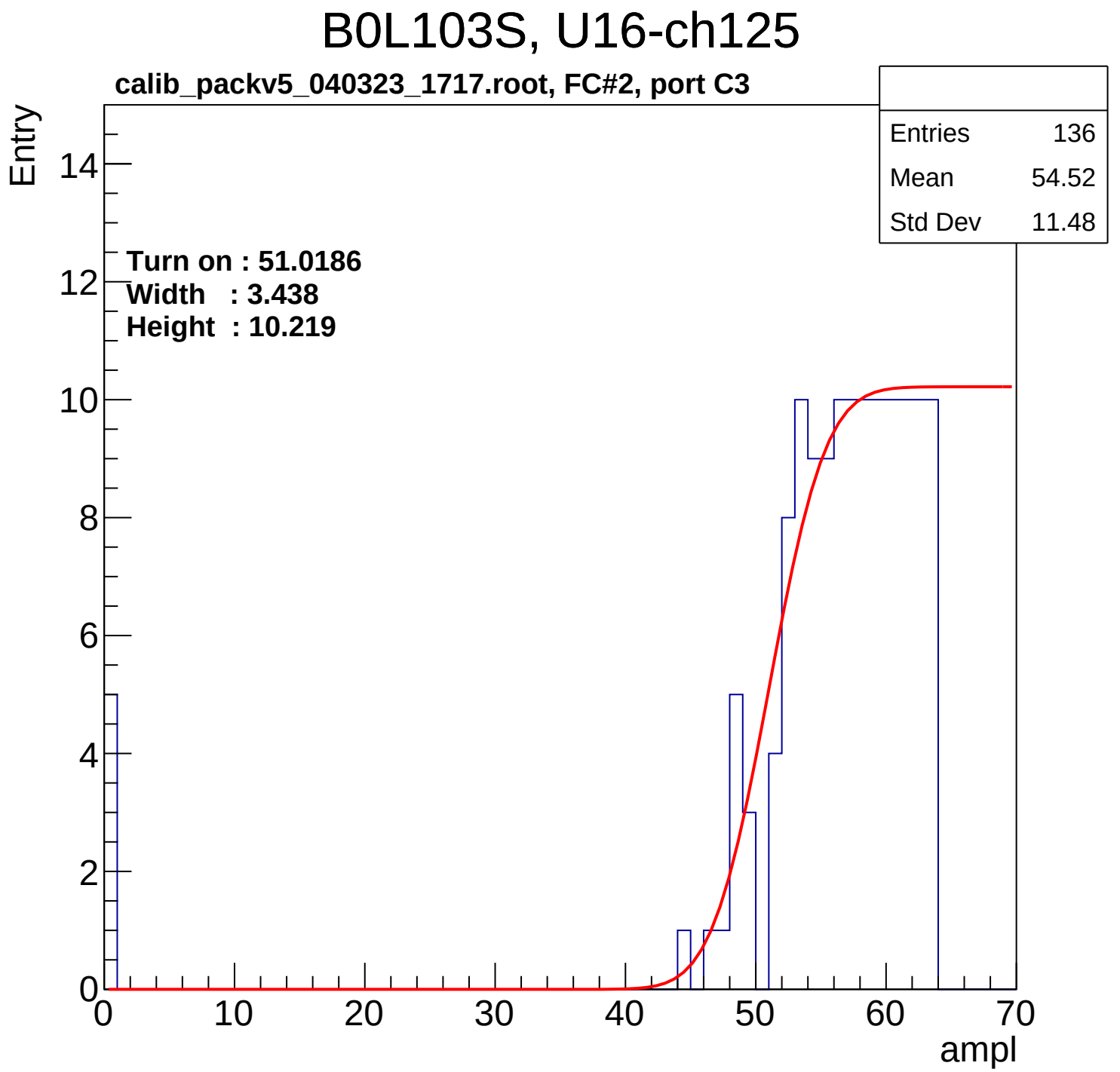
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L103S, U16-ch125
calib_packv5_040323_1717.root, FC#2, port C3
Entries 136
Mean 54.52
Std Dev 11.48
Turn on : 51.0186
Width : 3.438
Height : 10.219
Entry
ampl
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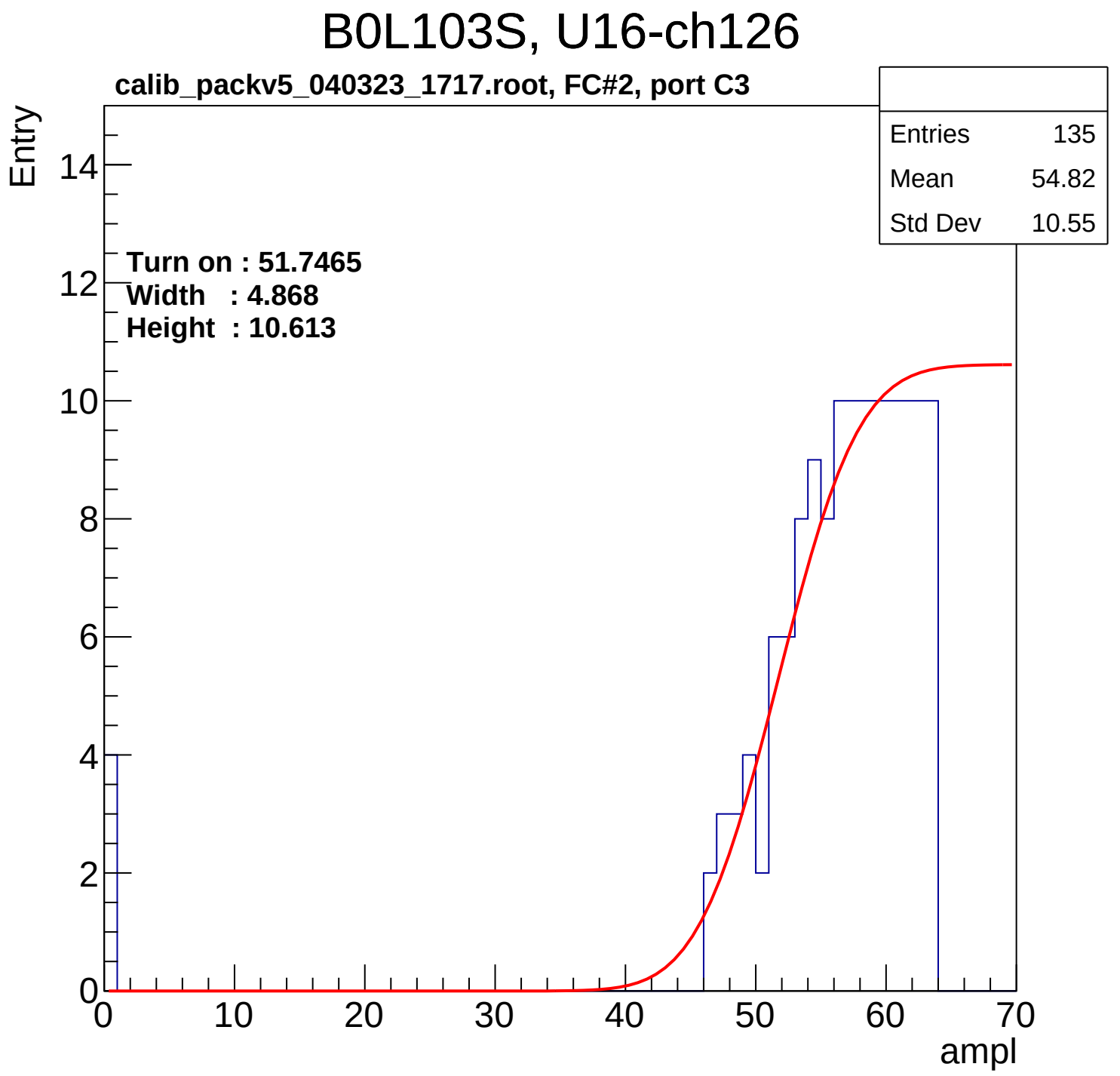
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L103S, U16-ch126
calib_packv5_040323_1717.root, FC#2, port C3
Entries 135
Mean 54.82
Std Dev 10.55
Turn on : 51.7465
Width : 4.868
Height : 10.613
Entry
ampl
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2
4
6
8
10
12
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0
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20
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40
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60
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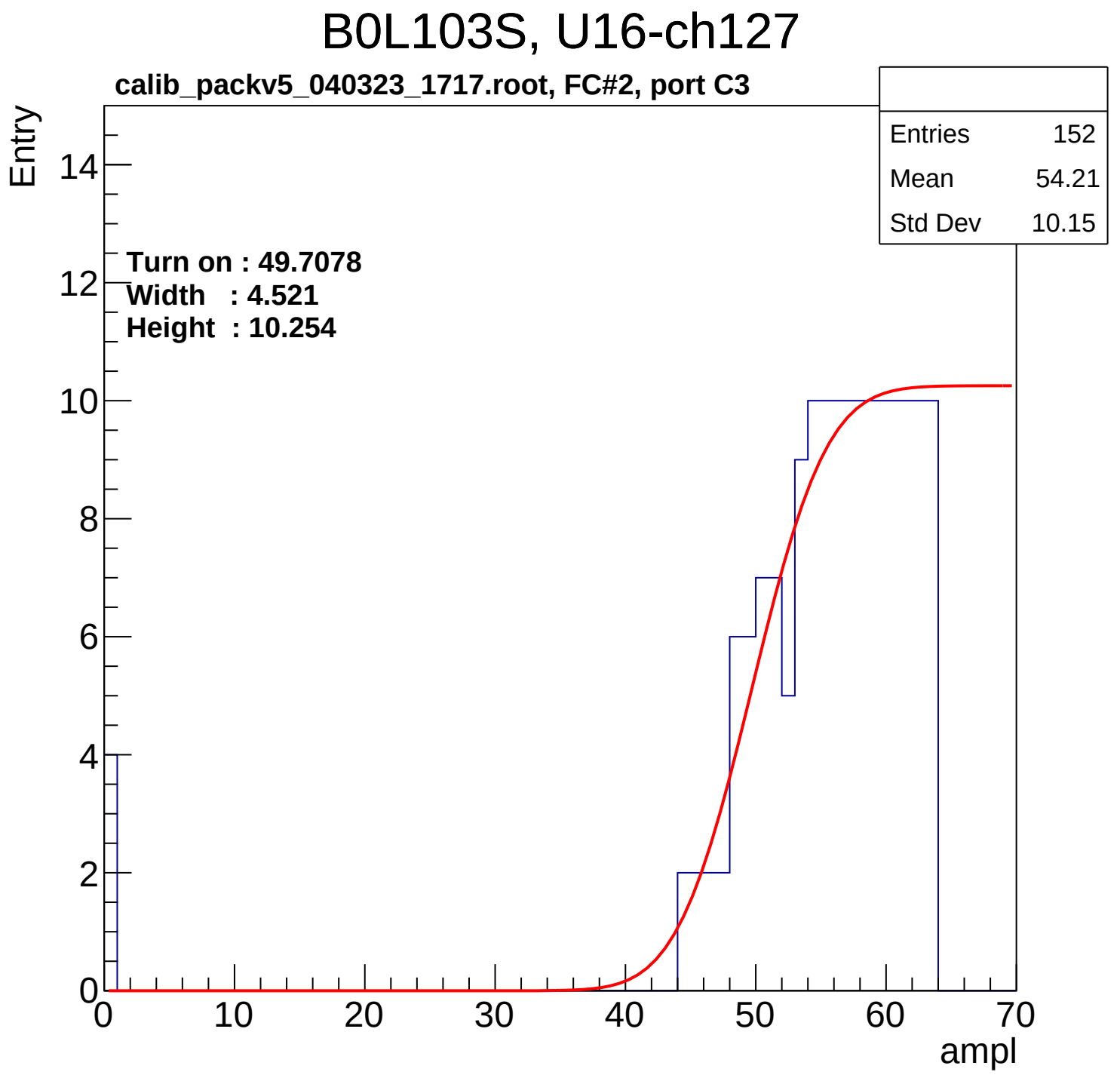
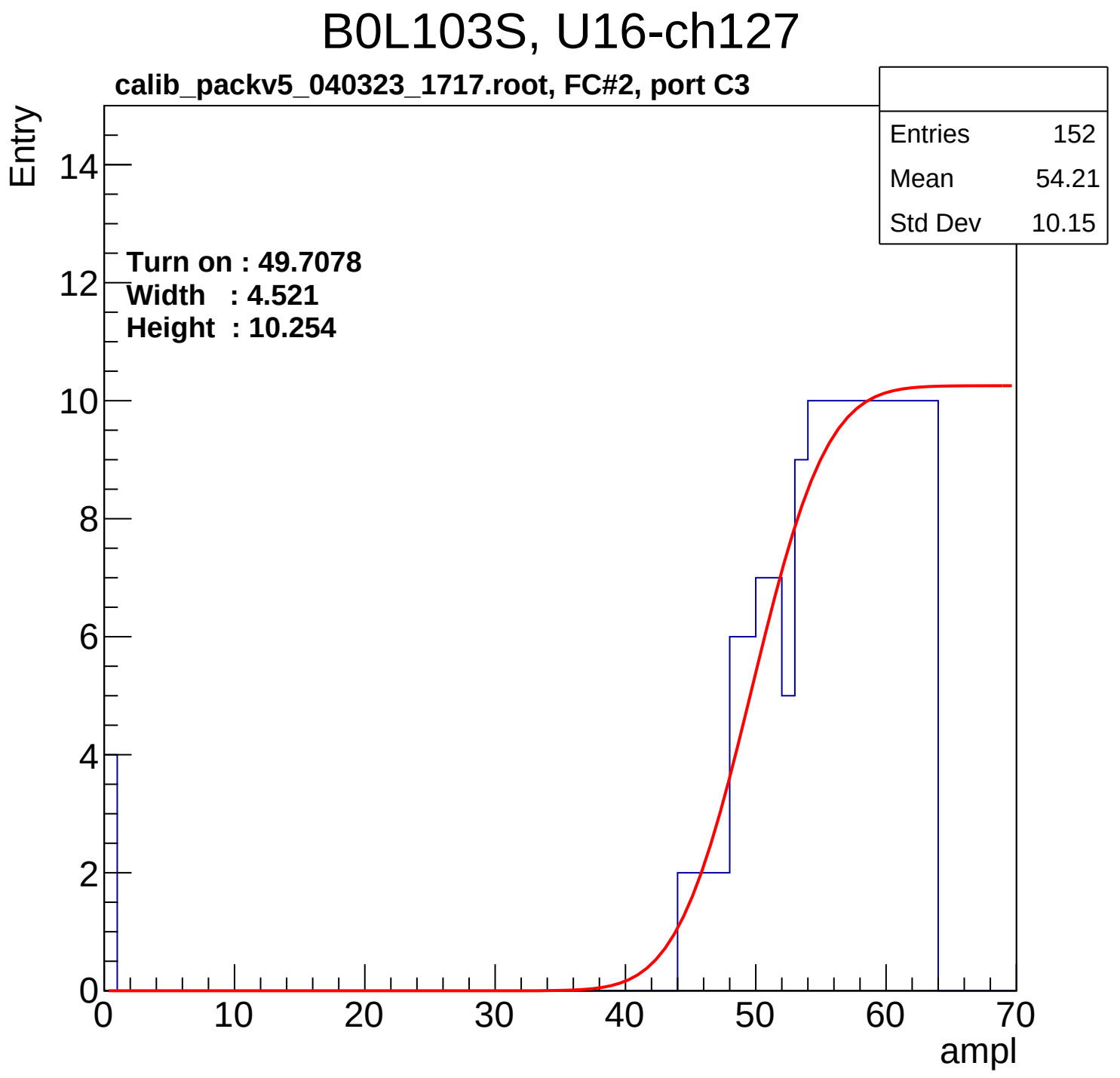

B0L103S, U16-ch127
calib_packv5_040323_1717.root, FC#2, port C3
Entries 152
Mean 54.21
Std Dev 10.15
Turn on : 49.7078
Width : 4.521
Height : 10.254
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L103S, U16-ch127
calib_packv5_040323_1717.root, FC#2, port C3
Entries 152
Mean 54.21
Std Dev 10.15
Turn on : 49.7078
Width : 4.521
Height : 10.254
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70