



# B0L001S, U5-ch0, adc0

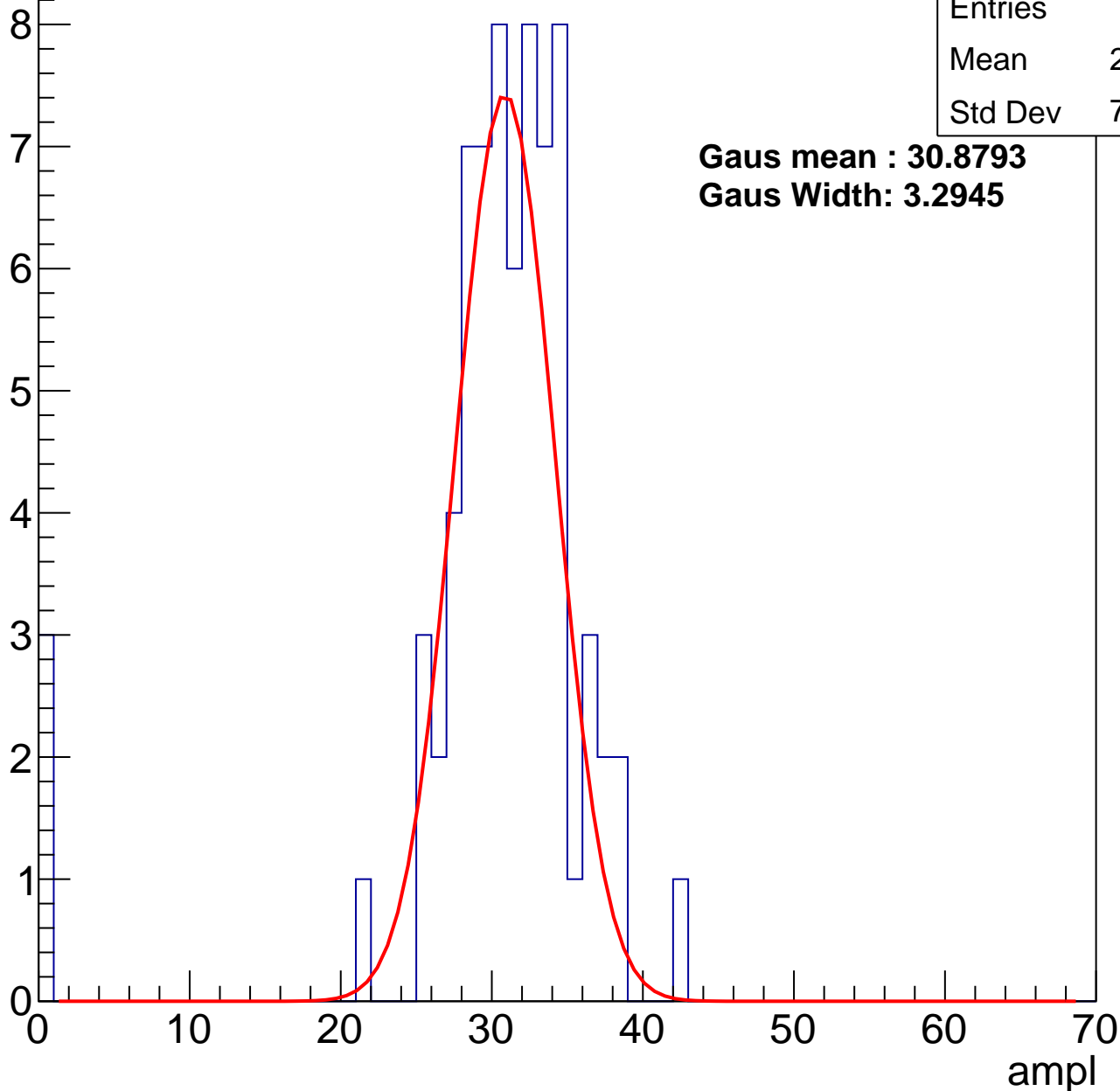
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	29.79
Std Dev	7.108

**Gaus mean : 30.8793**

**Gaus Width: 3.2945**

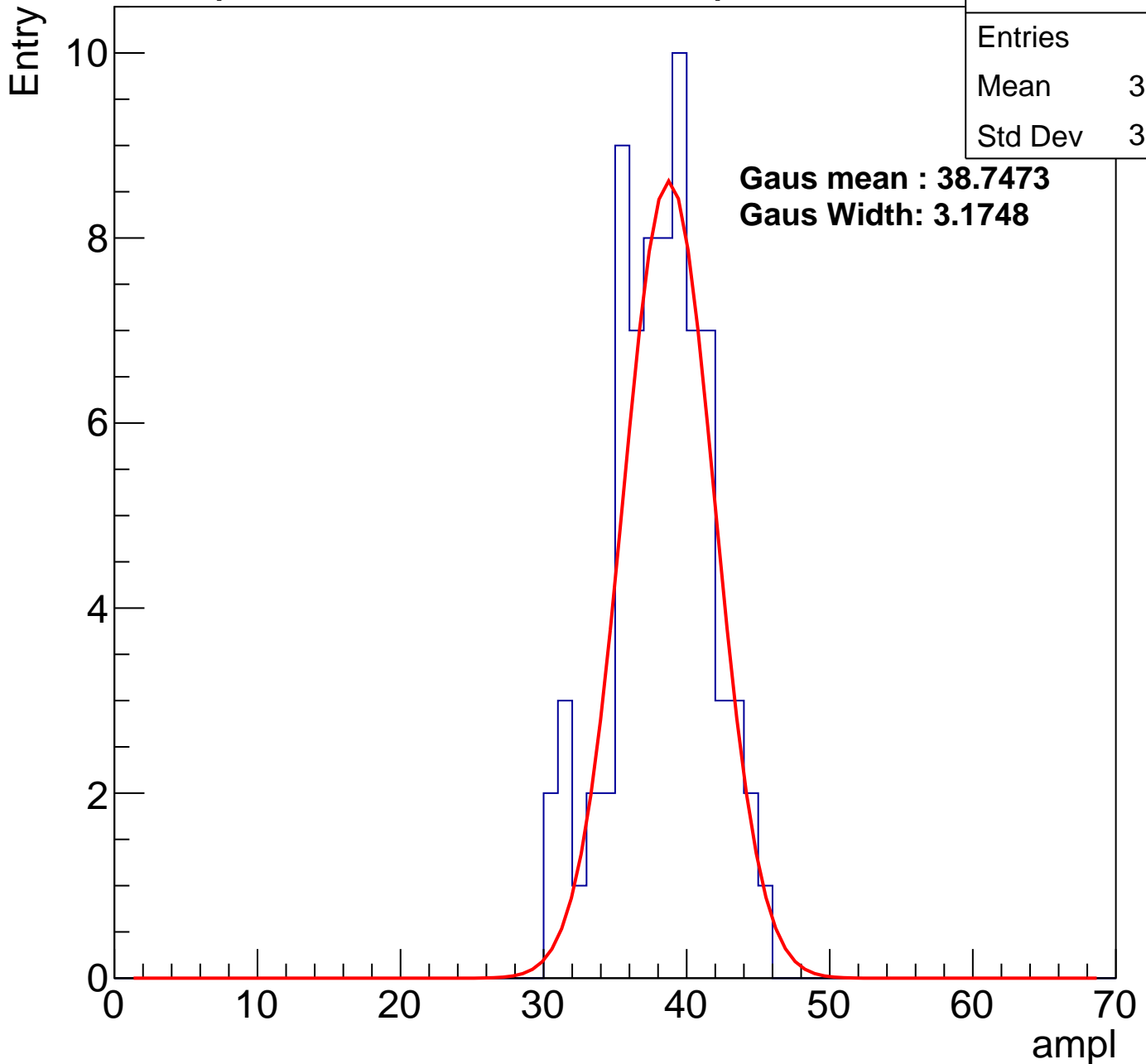


# B0L001S, U5-ch0, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	75
Mean	37.75
Std Dev	3.367

**Gaus mean : 38.7473**  
**Gaus Width: 3.1748**



# B0L001S, U5-ch0, adc2

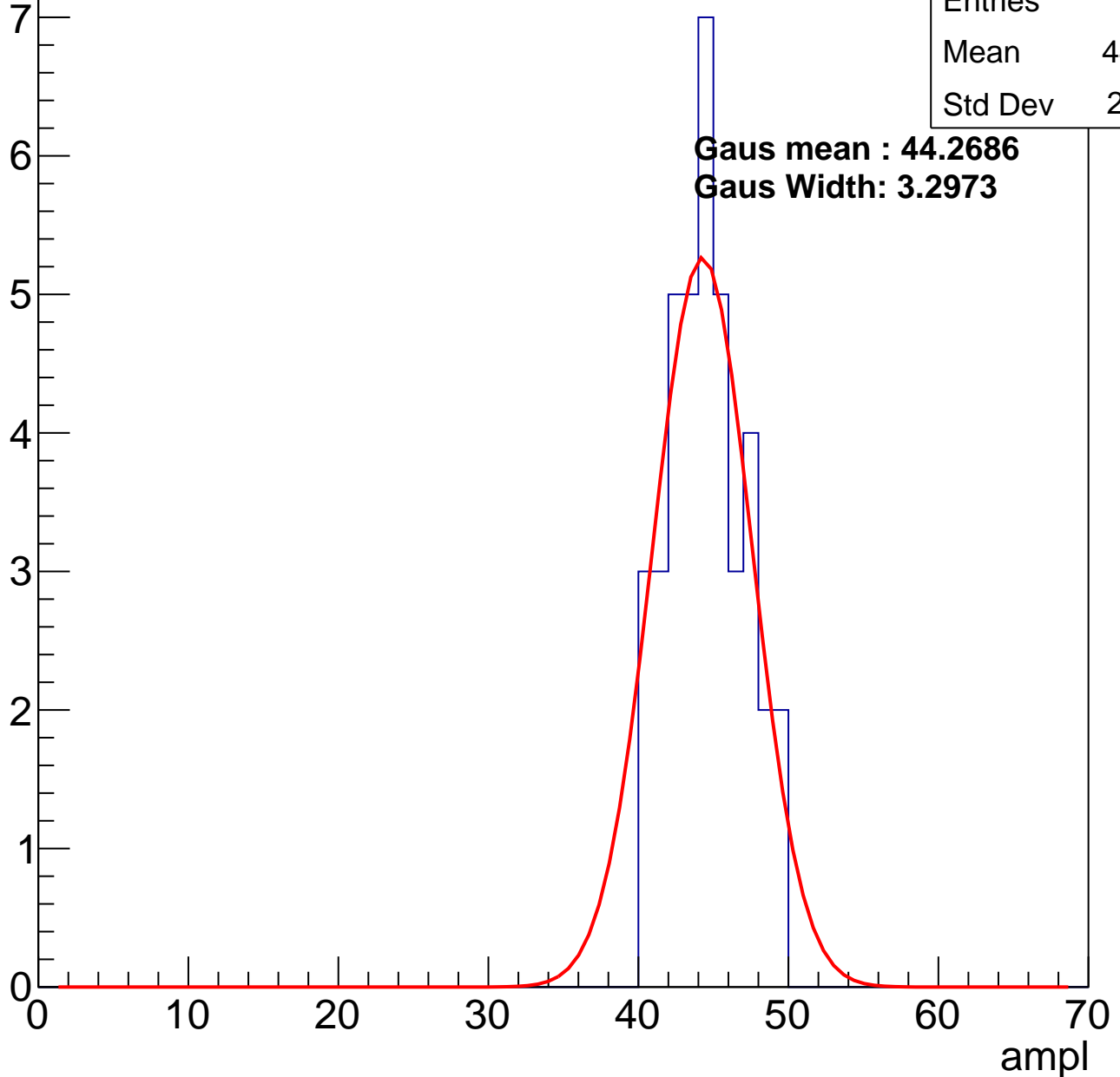
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	39
Mean	44.13
Std Dev	2.451

**Gaus mean : 44.2686**

**Gaus Width: 3.2973**

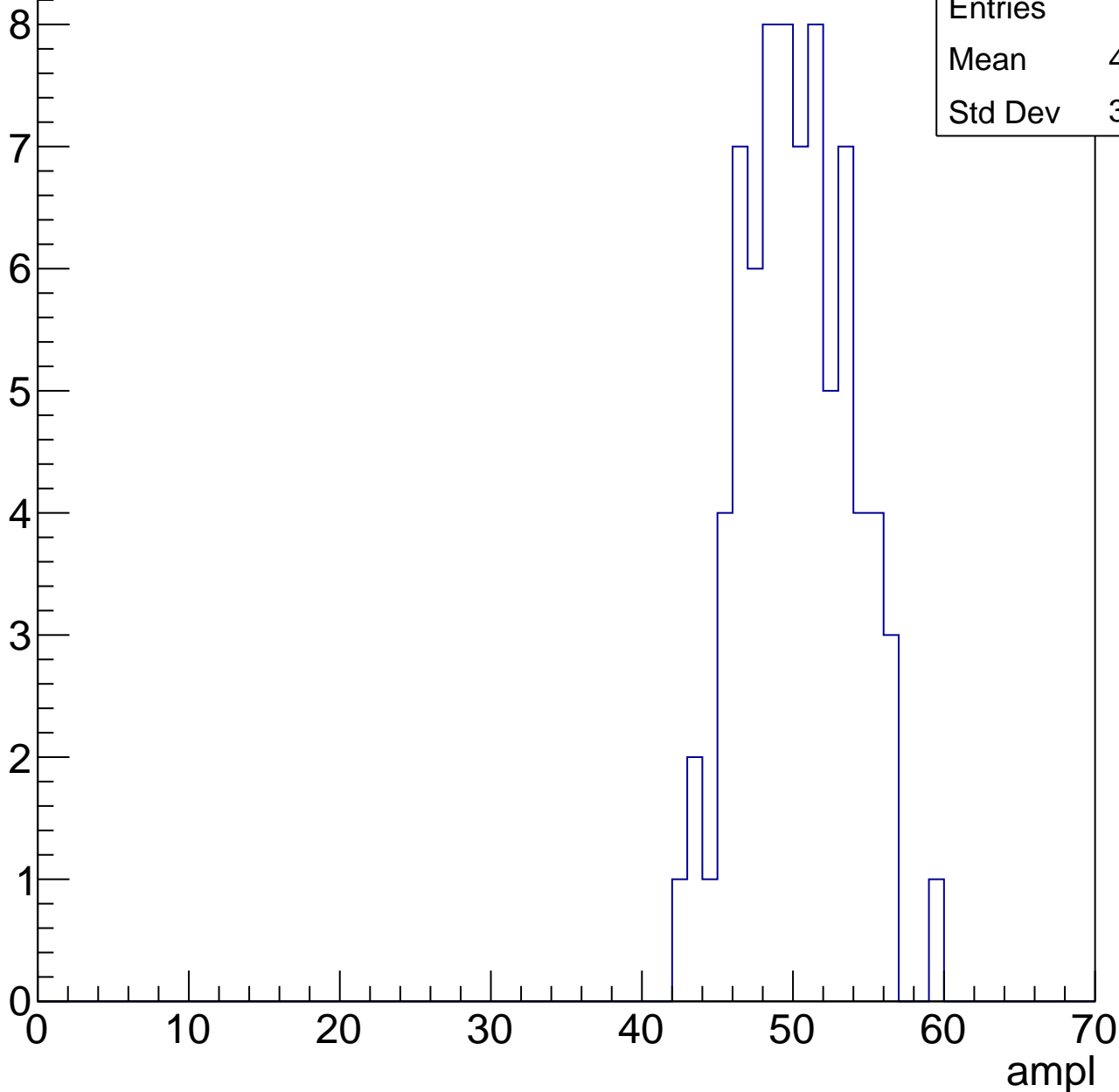


# B0L001S, U5-ch0, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	76
Mean	49.79
Std Dev	3.526



# B0L001S, U5-ch0, adc4

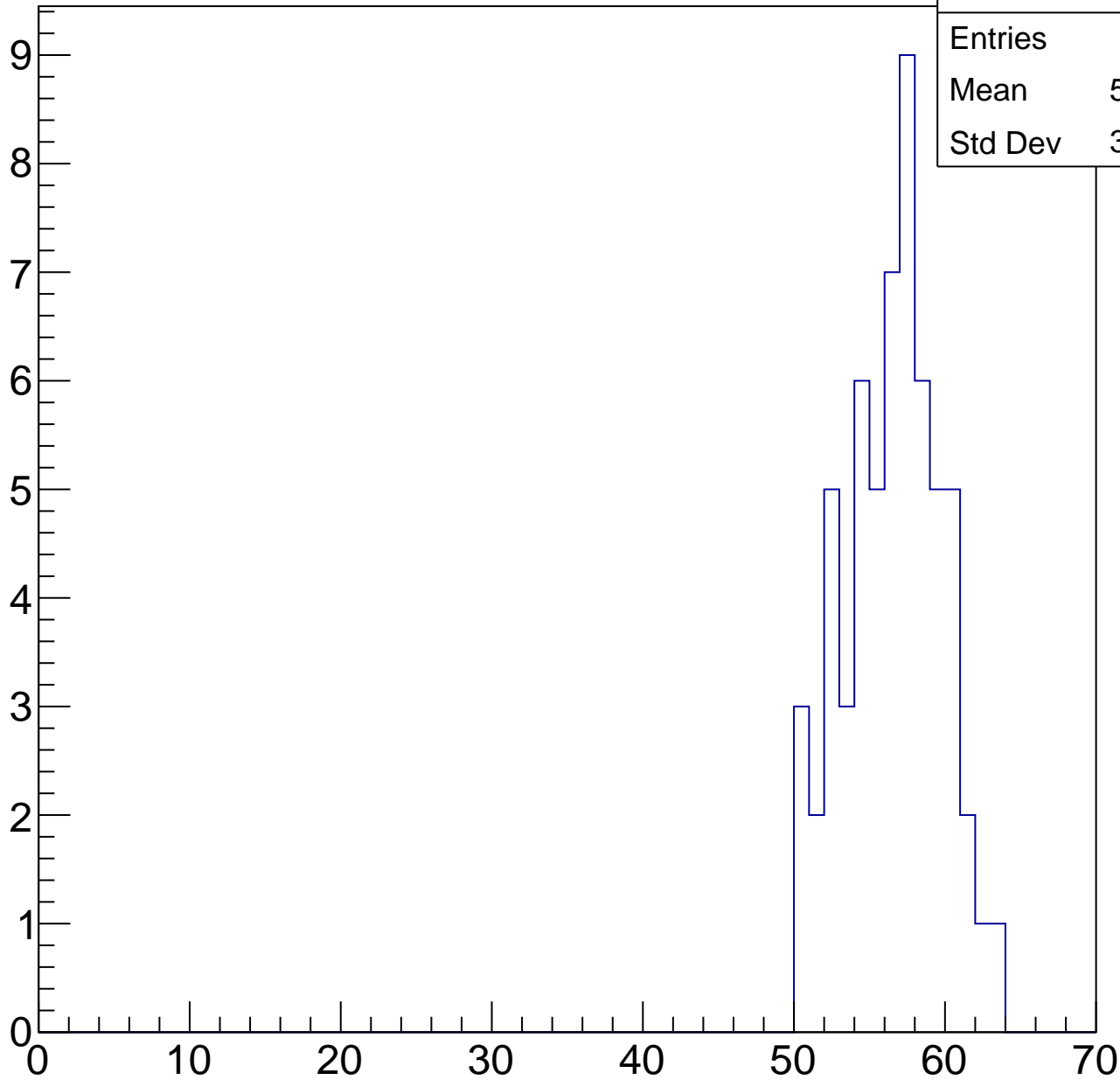
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	60
Mean	56.08
Std Dev	3.127

ampl

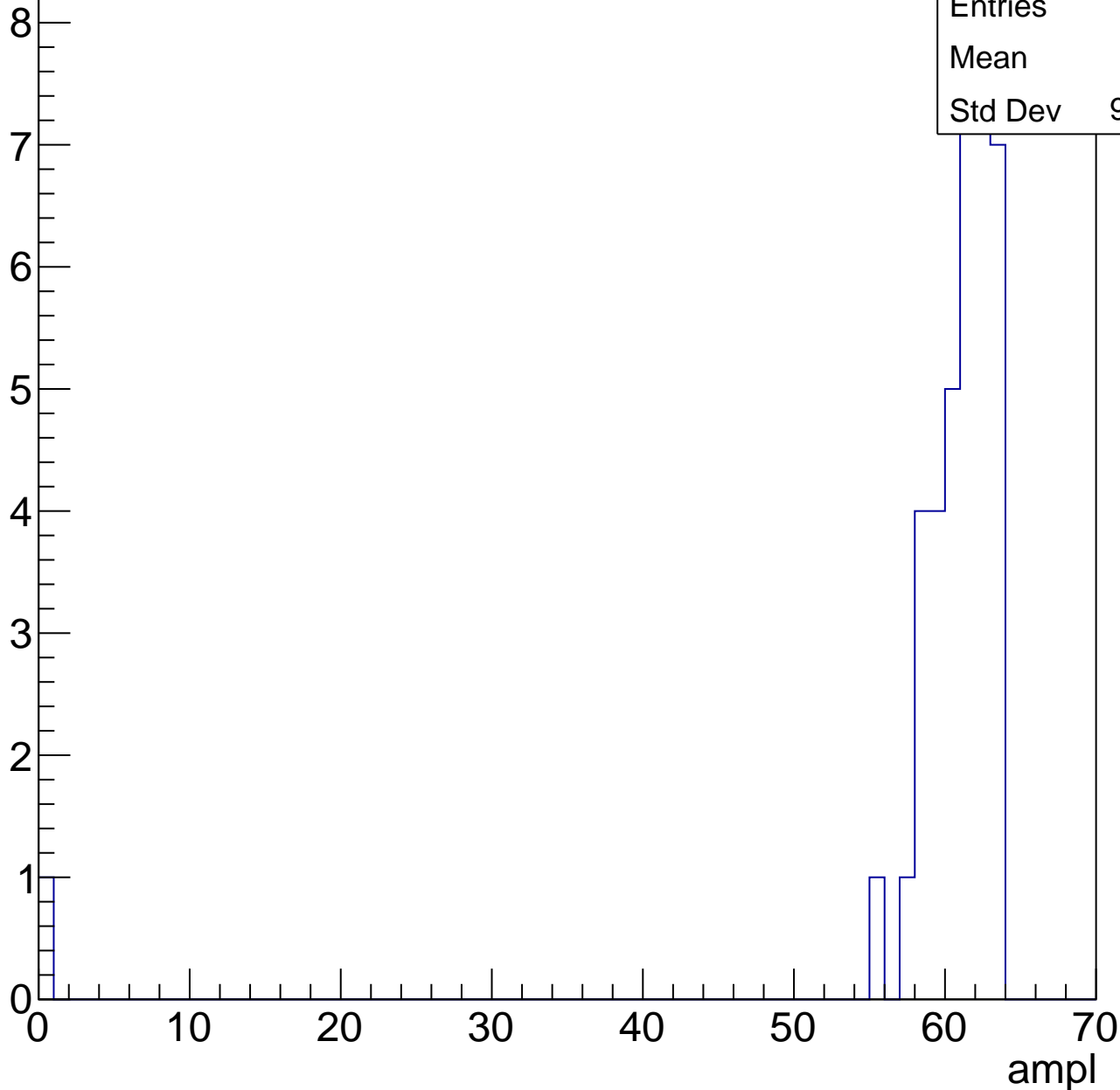


# B0L001S, U5-ch0, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	39
Mean	59.1
Std Dev	9.774



# B0L001S, U5-ch0, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch0, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch1, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	79
Mean	27.89
Std Dev	6.473

**Gaus mean : 29.5618**

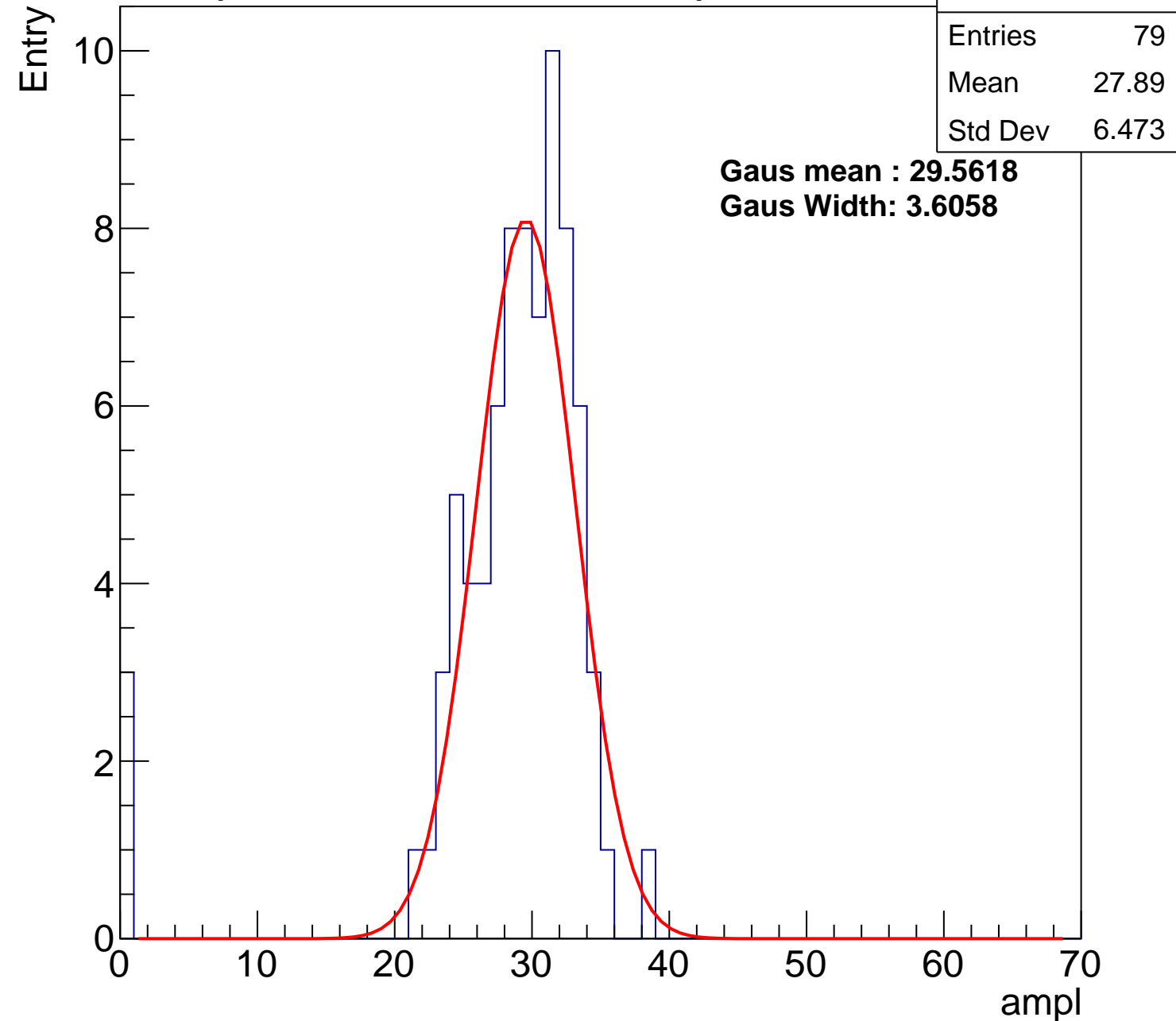
**Gaus Width: 3.6058**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



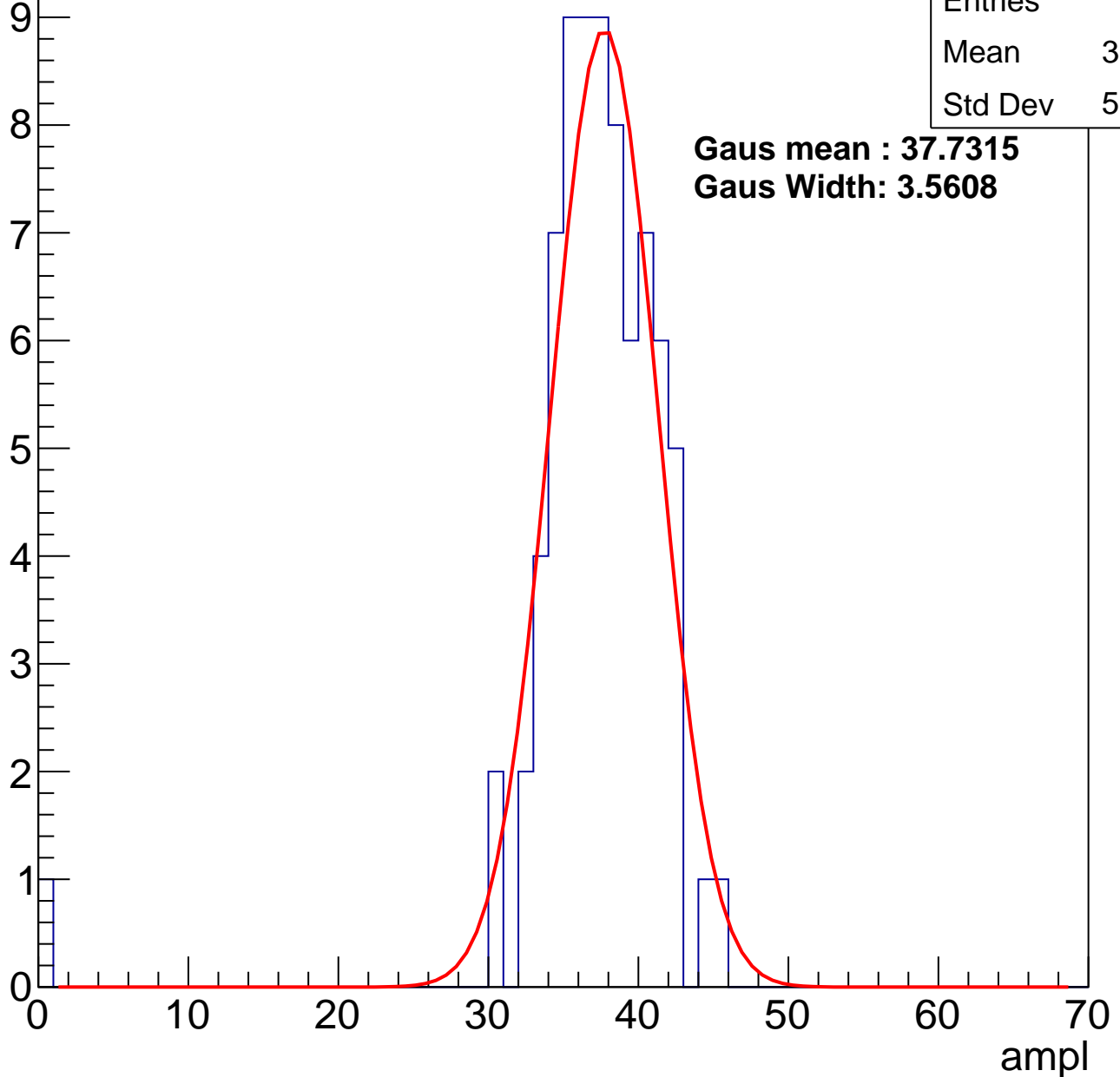
# B0L001S, U5-ch1, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	77
Mean	36.74
Std Dev	5.238

**Gaus mean : 37.7315**  
**Gaus Width: 3.5608**



# B0L001S, U5-ch1, adc2

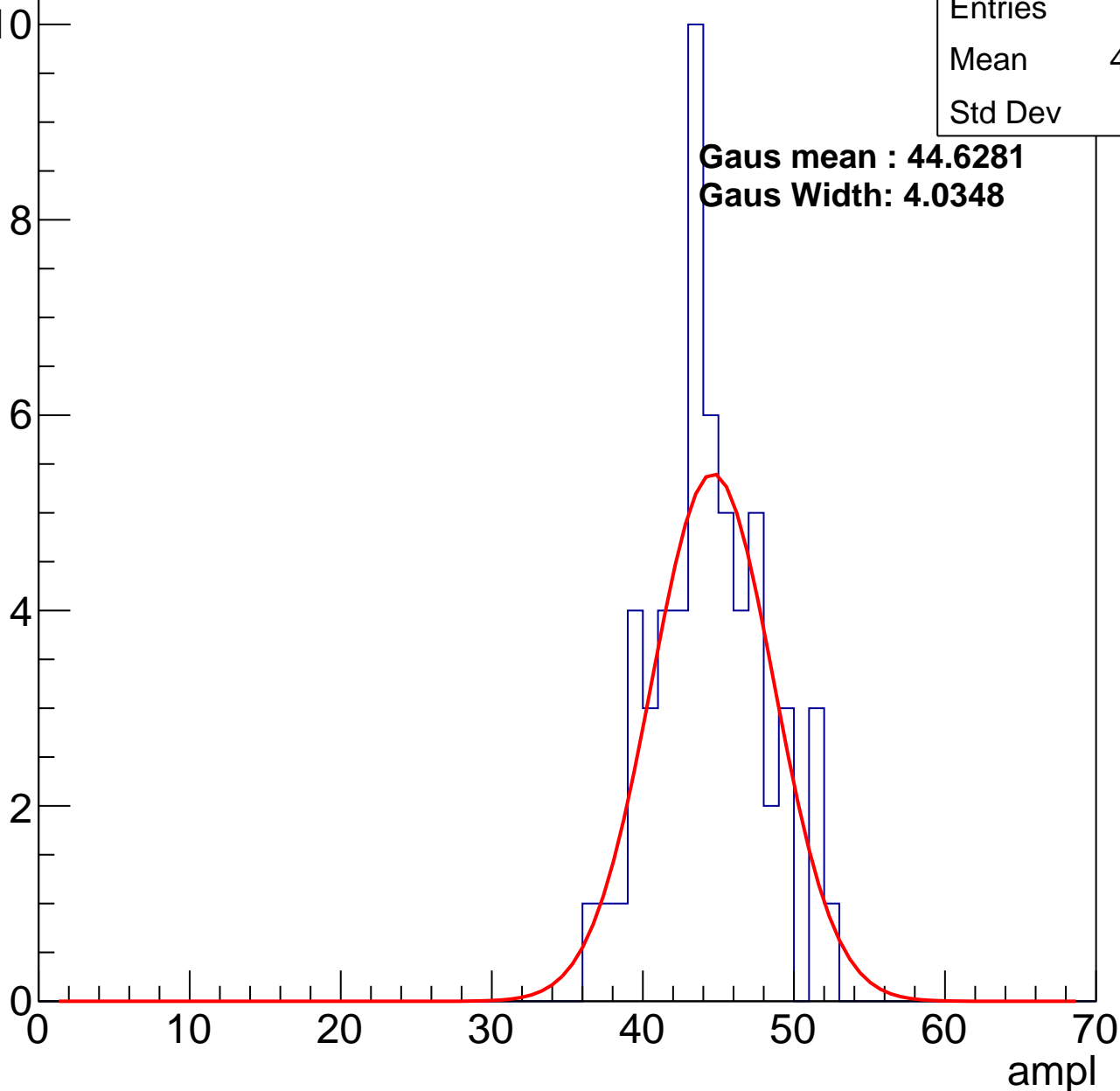
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	43.95
Std Dev	3.61

**Gaus mean : 44.6281**

**Gaus Width: 4.0348**

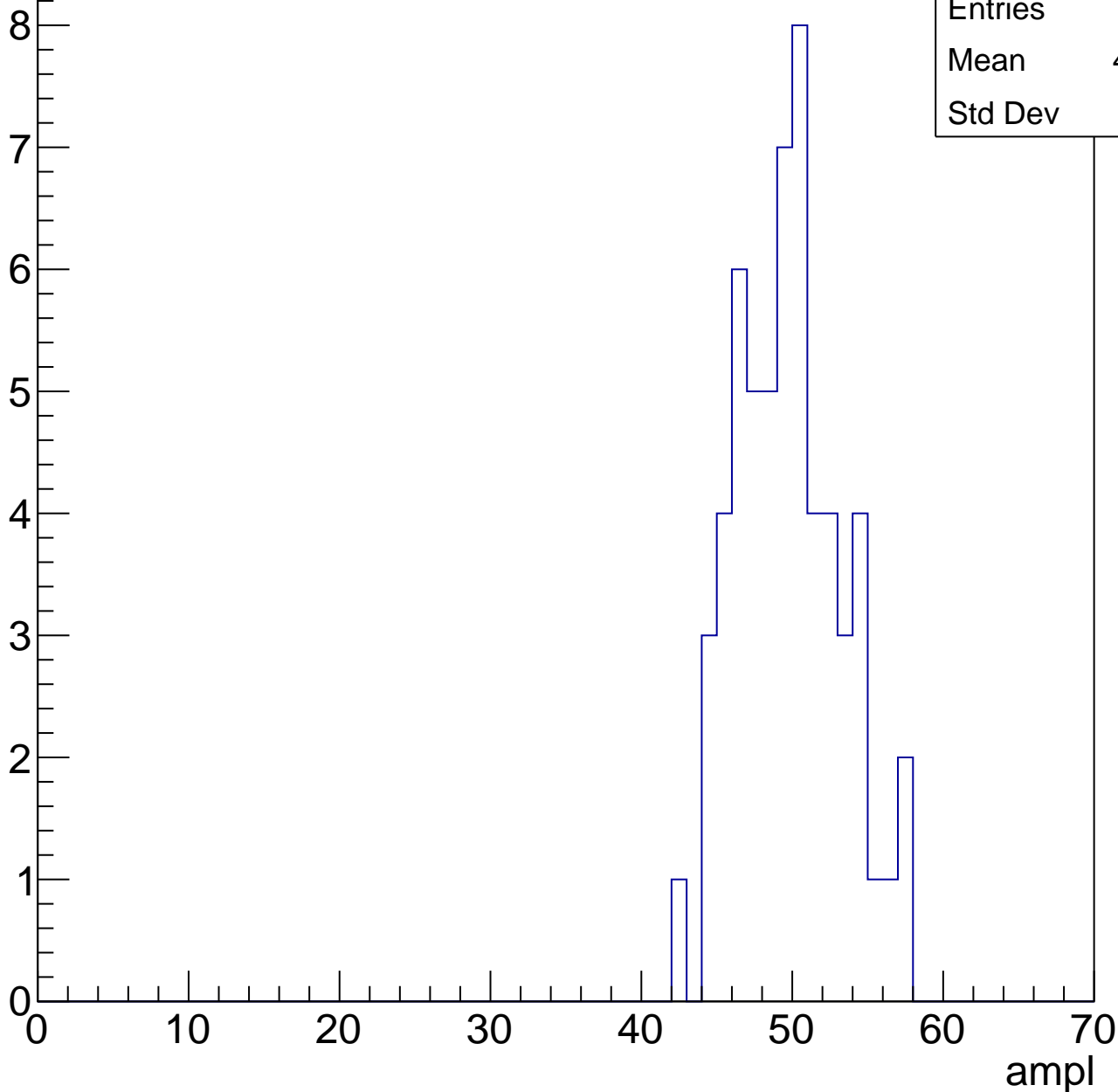


# B0L001S, U5-ch1, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	49.31
Std Dev	3.43

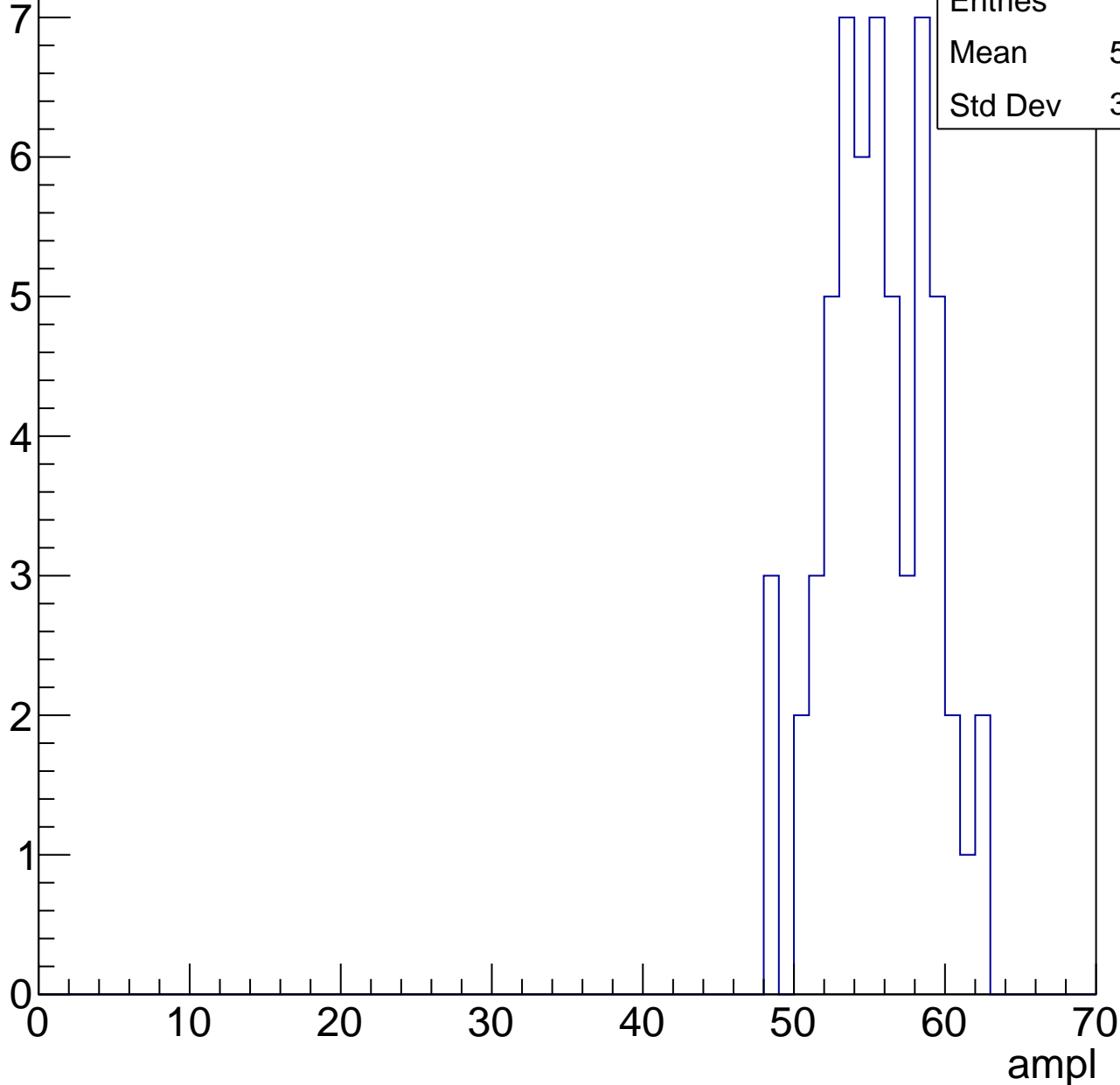


# B0L001S, U5-ch1, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	55.07
Std Dev	3.393

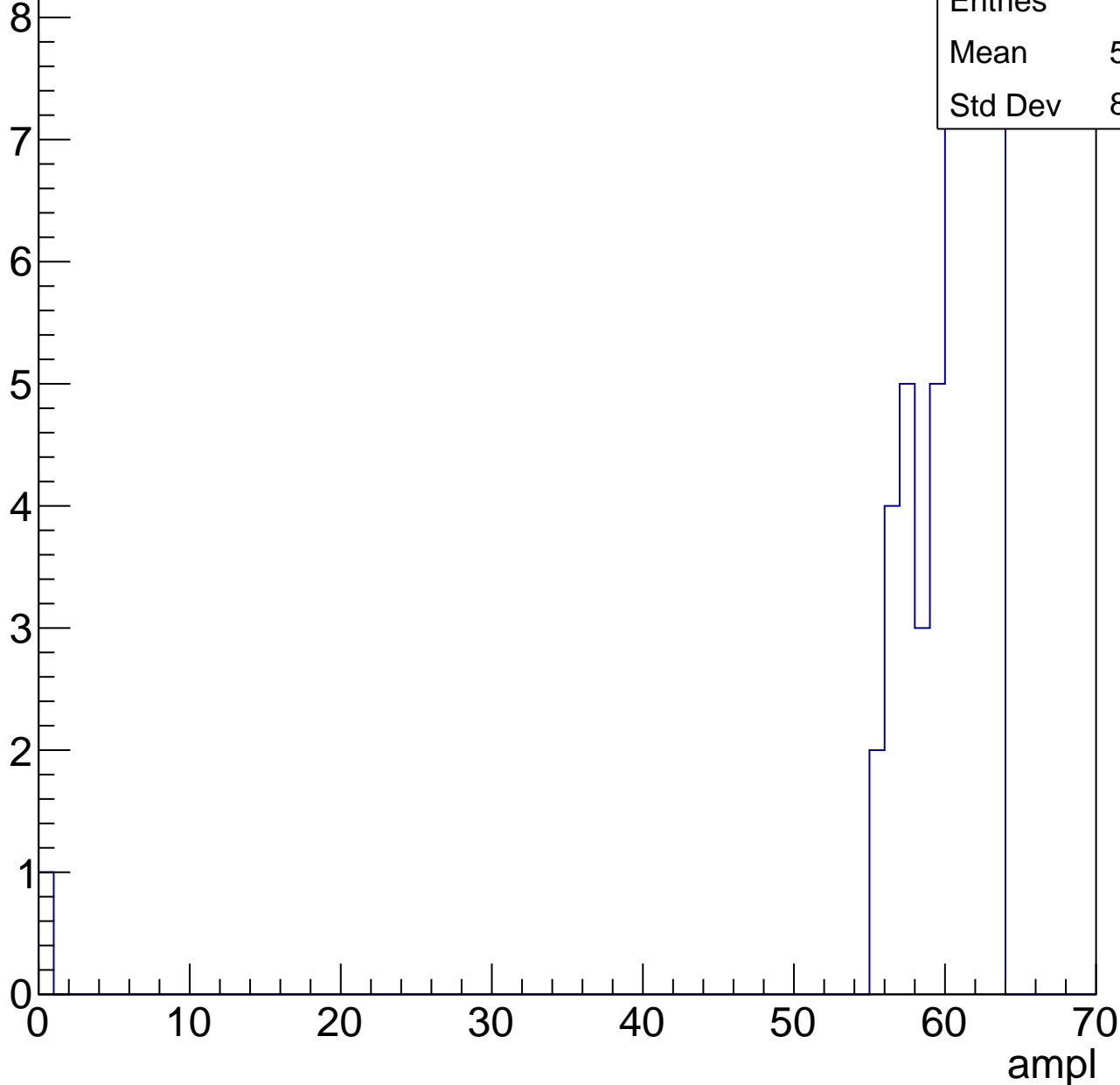


# B0L001S, U5-ch1, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	58.77
Std Dev	8.559



# B0L001S, U5-ch1, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch1, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch2, adc0

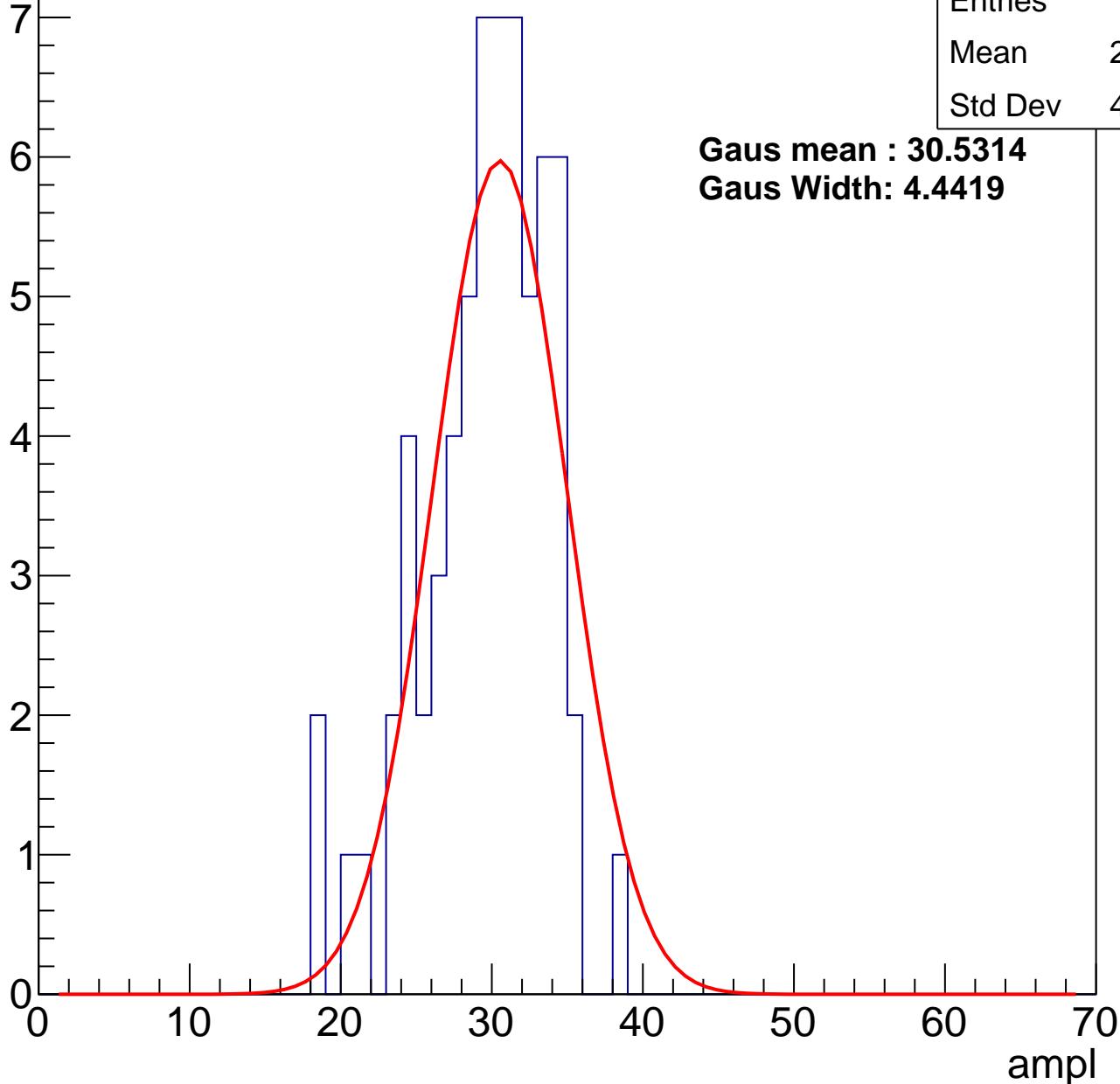
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	29.15
Std Dev	4.144

**Gaus mean : 30.5314**

**Gaus Width: 4.4419**



# B0L001S, U5-ch2, adc1

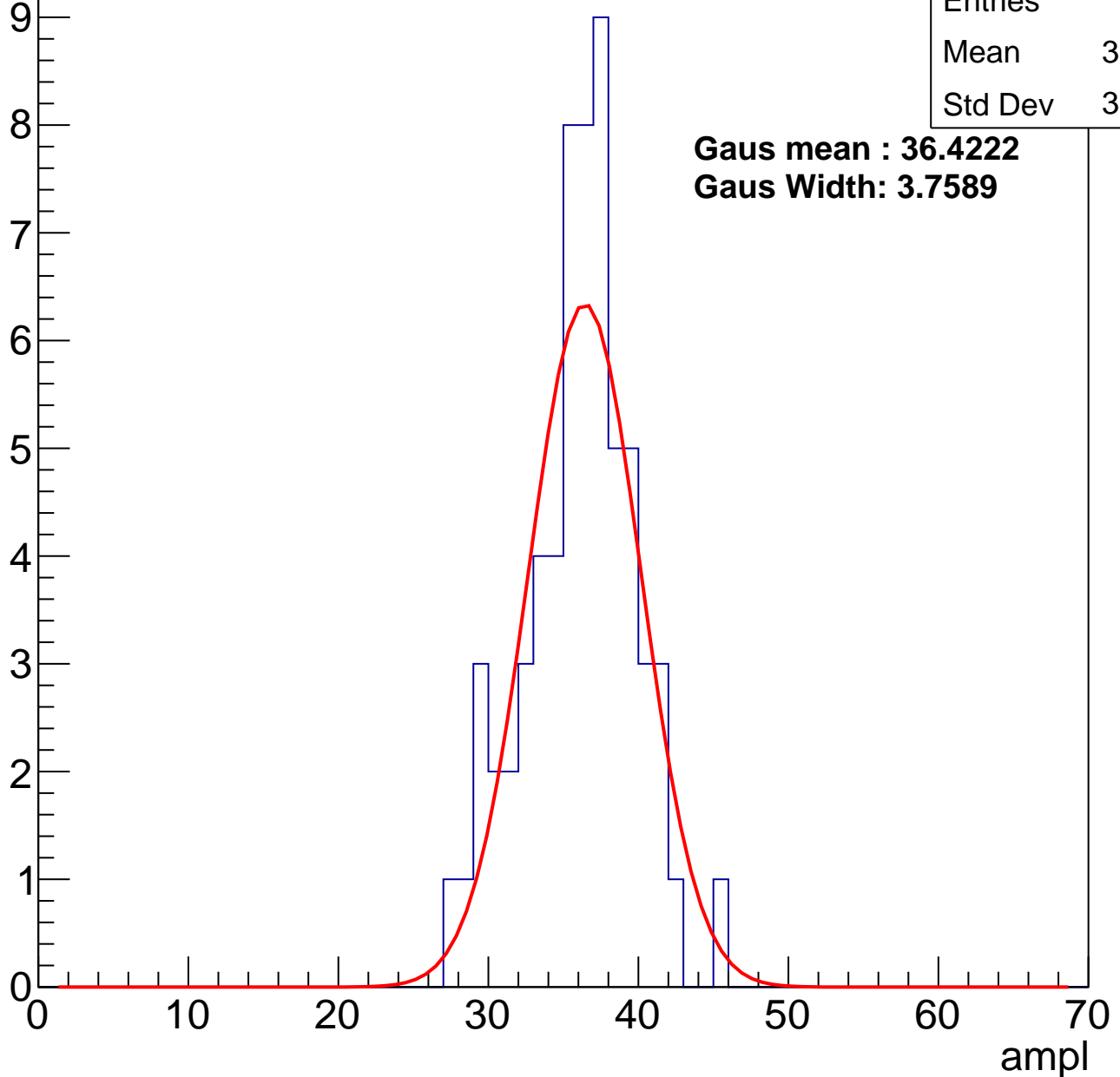
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	35.62
Std Dev	3.623

**Gaus mean : 36.4222**

**Gaus Width: 3.7589**



# B0L001S, U5-ch2, adc2

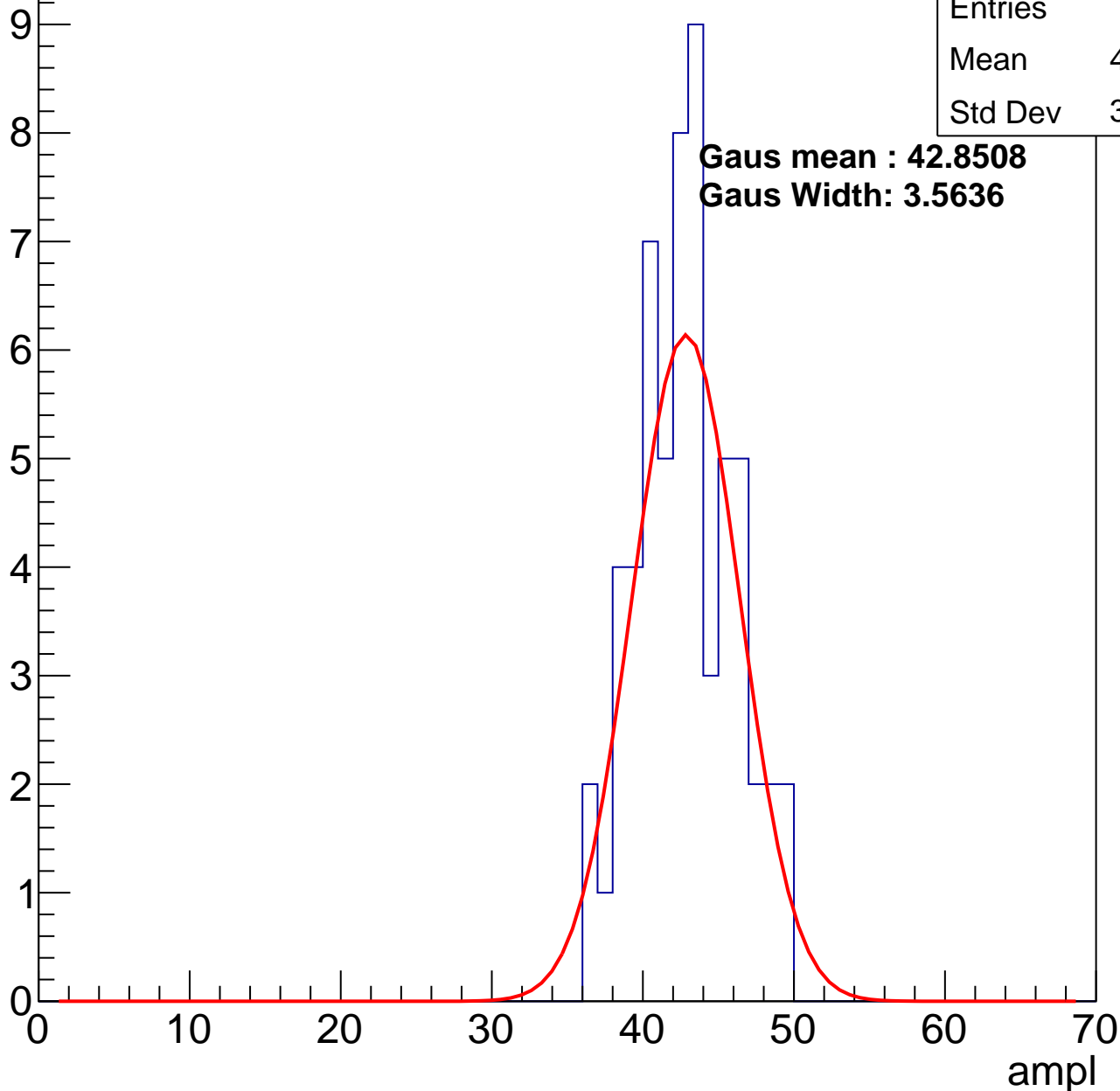
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	42.37
Std Dev	3.156

**Gaus mean : 42.8508**

**Gaus Width: 3.5636**

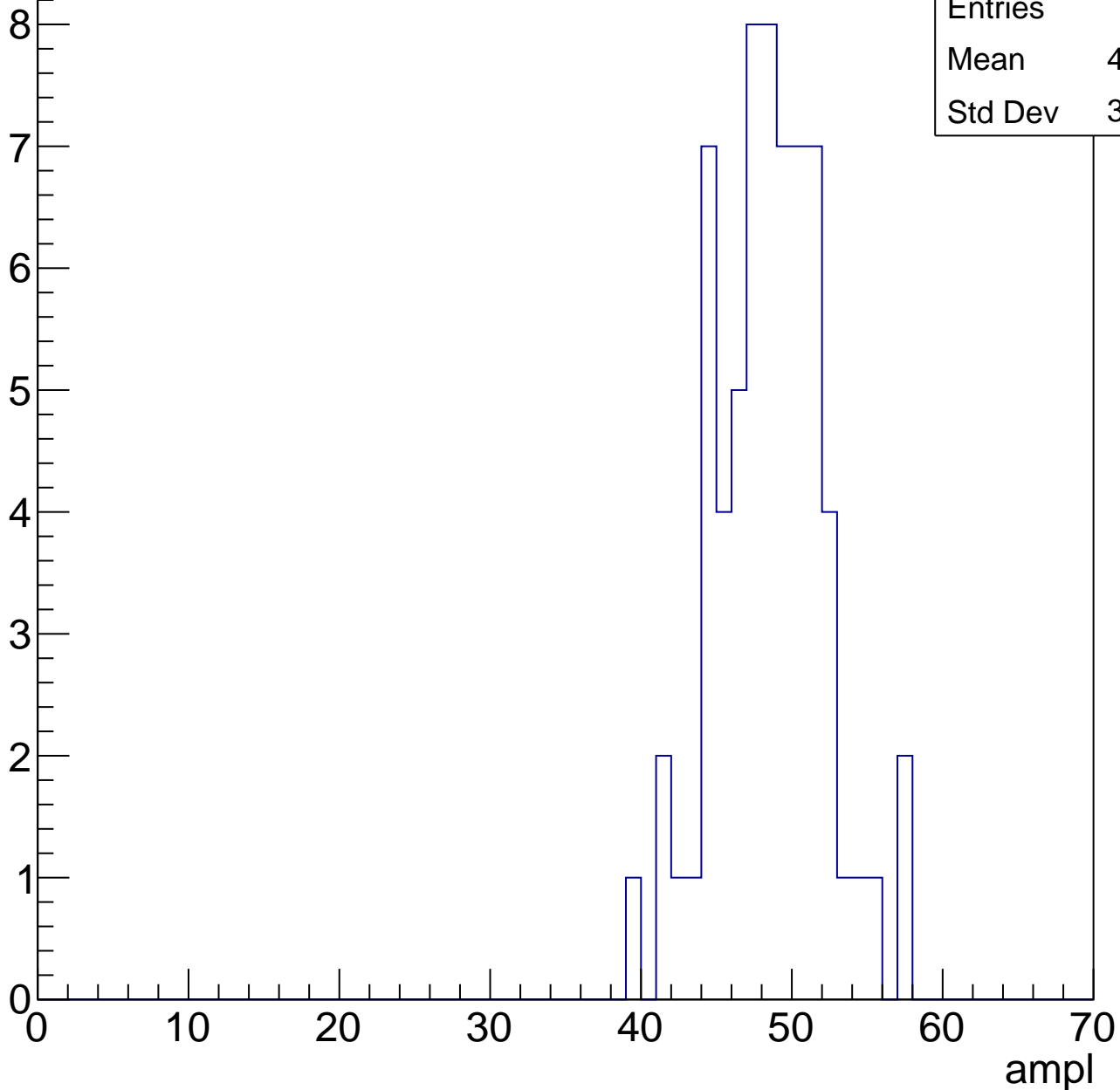


# B0L001S, U5-ch2, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

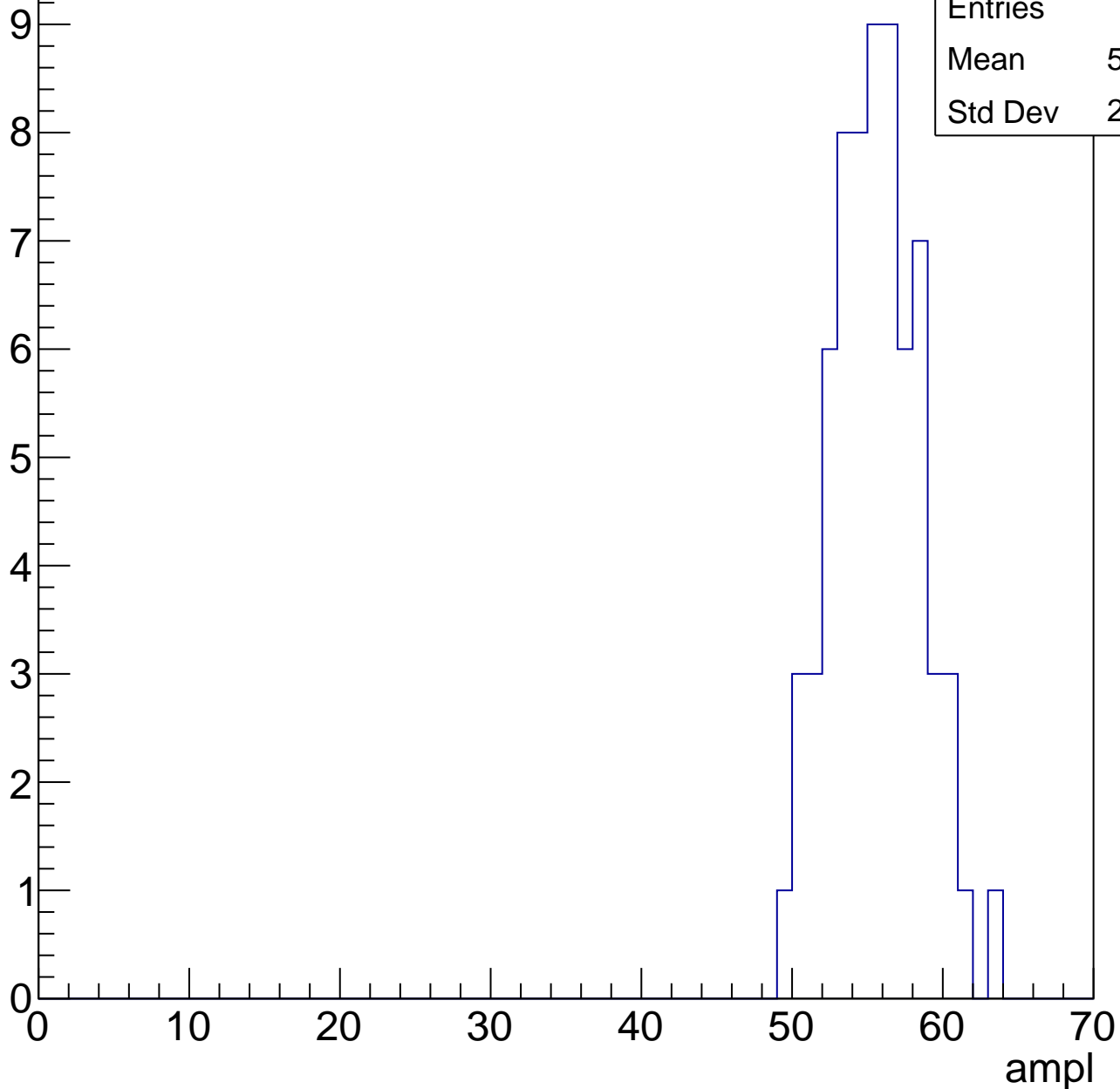
Entries	67
Mean	48.03
Std Dev	3.562



# B0L001S, U5-ch2, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

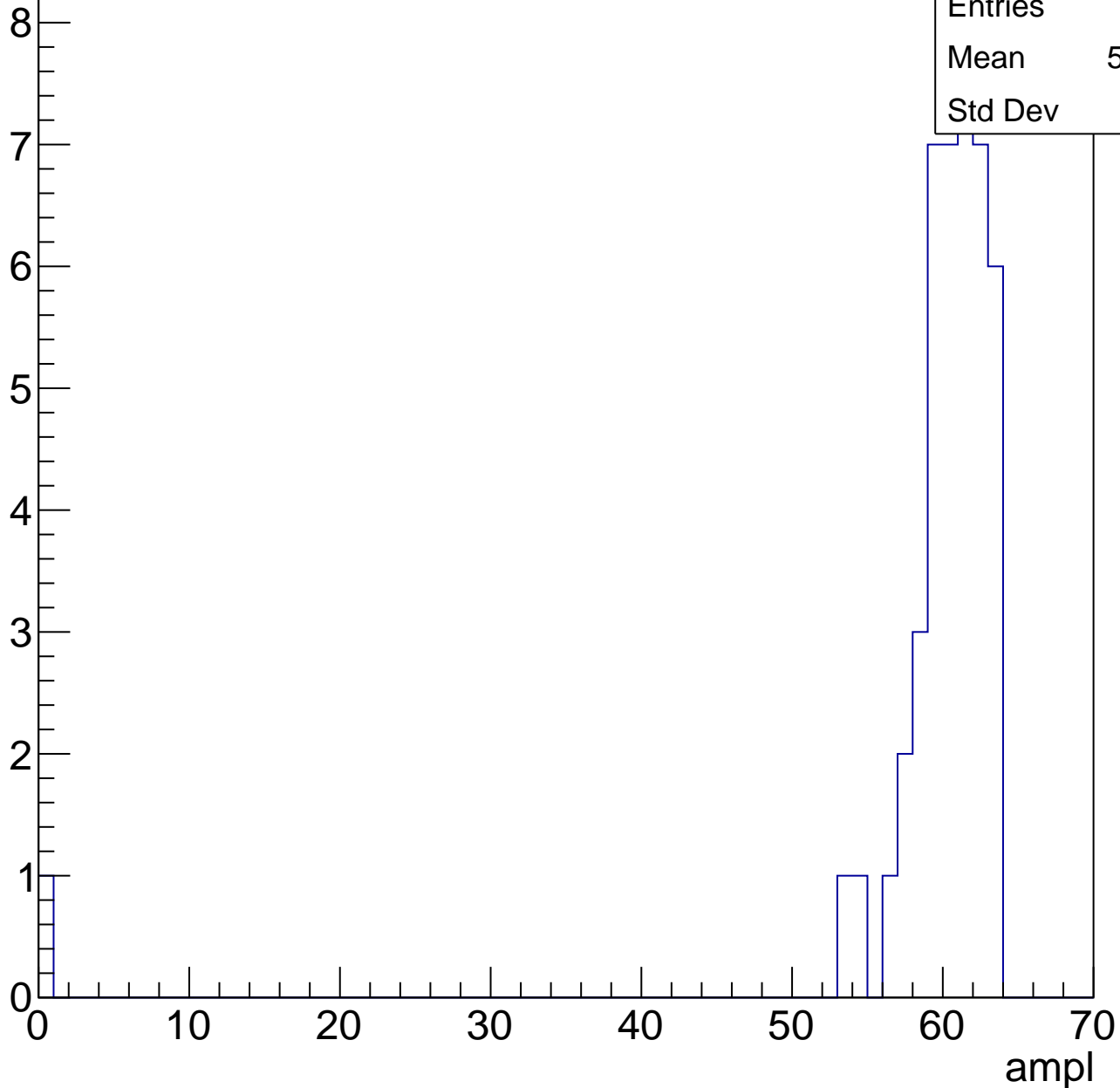


Entries	68
Mean	55.12
Std Dev	2.898

# B0L001S, U5-ch2, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch2, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch2, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch3, adc0

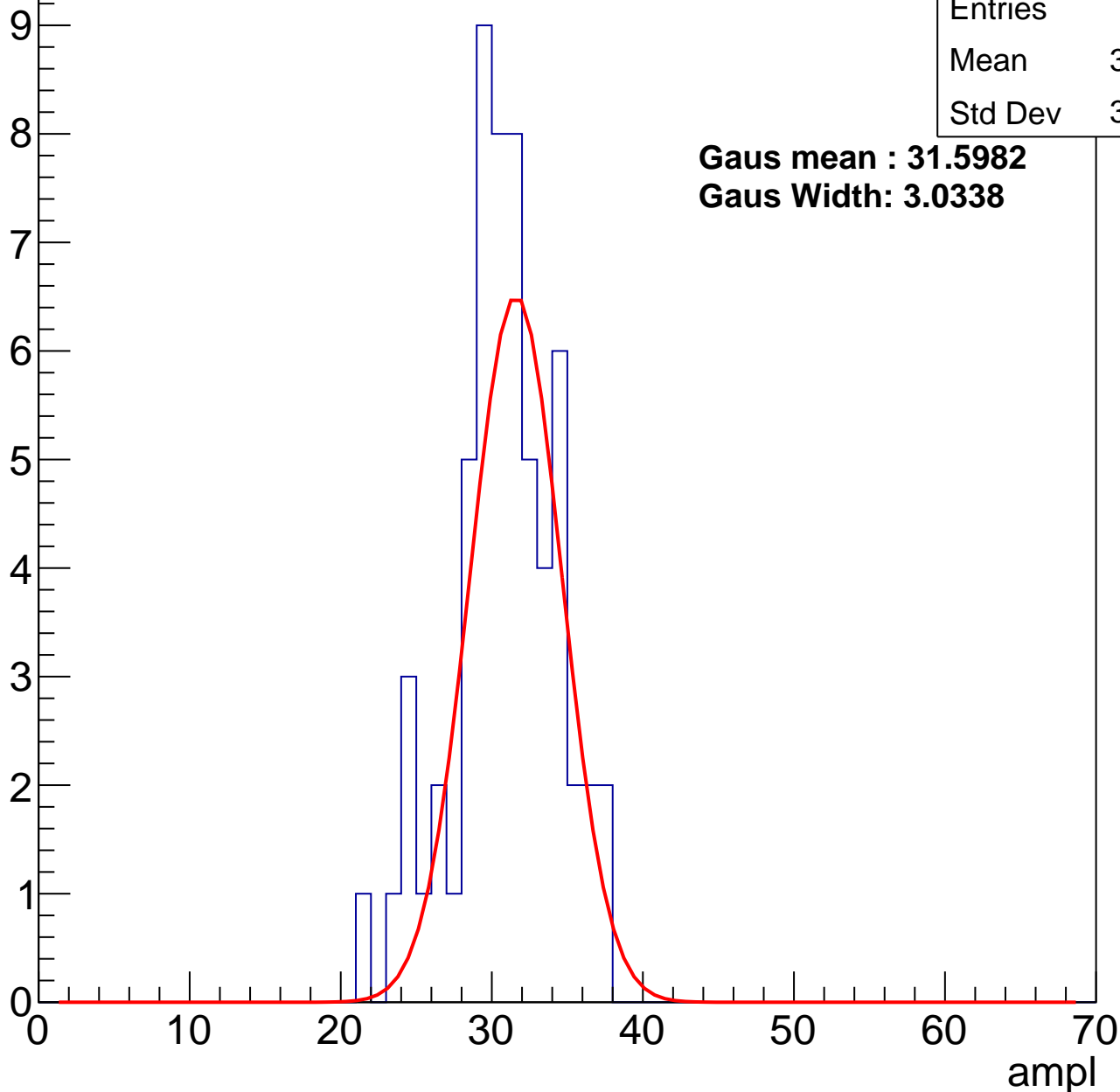
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	30.35
Std Dev	3.429

**Gaus mean : 31.5982**

**Gaus Width: 3.0338**



# B0L001S, U5-ch3, adc1

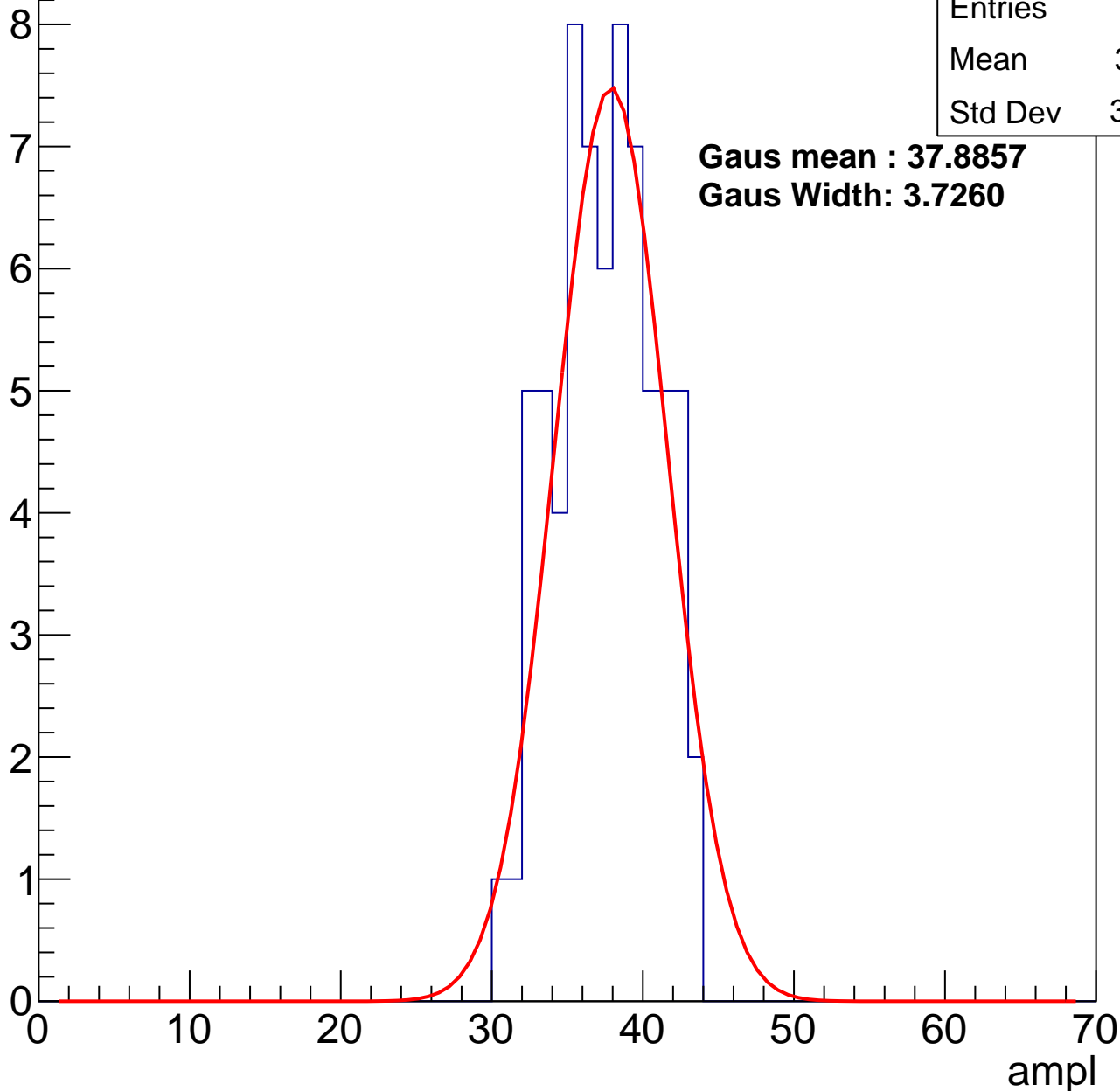
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	37.01
Std Dev	3.237

**Gaus mean : 37.8857**

**Gaus Width: 3.7260**



# B0L001S, U5-ch3, adc2

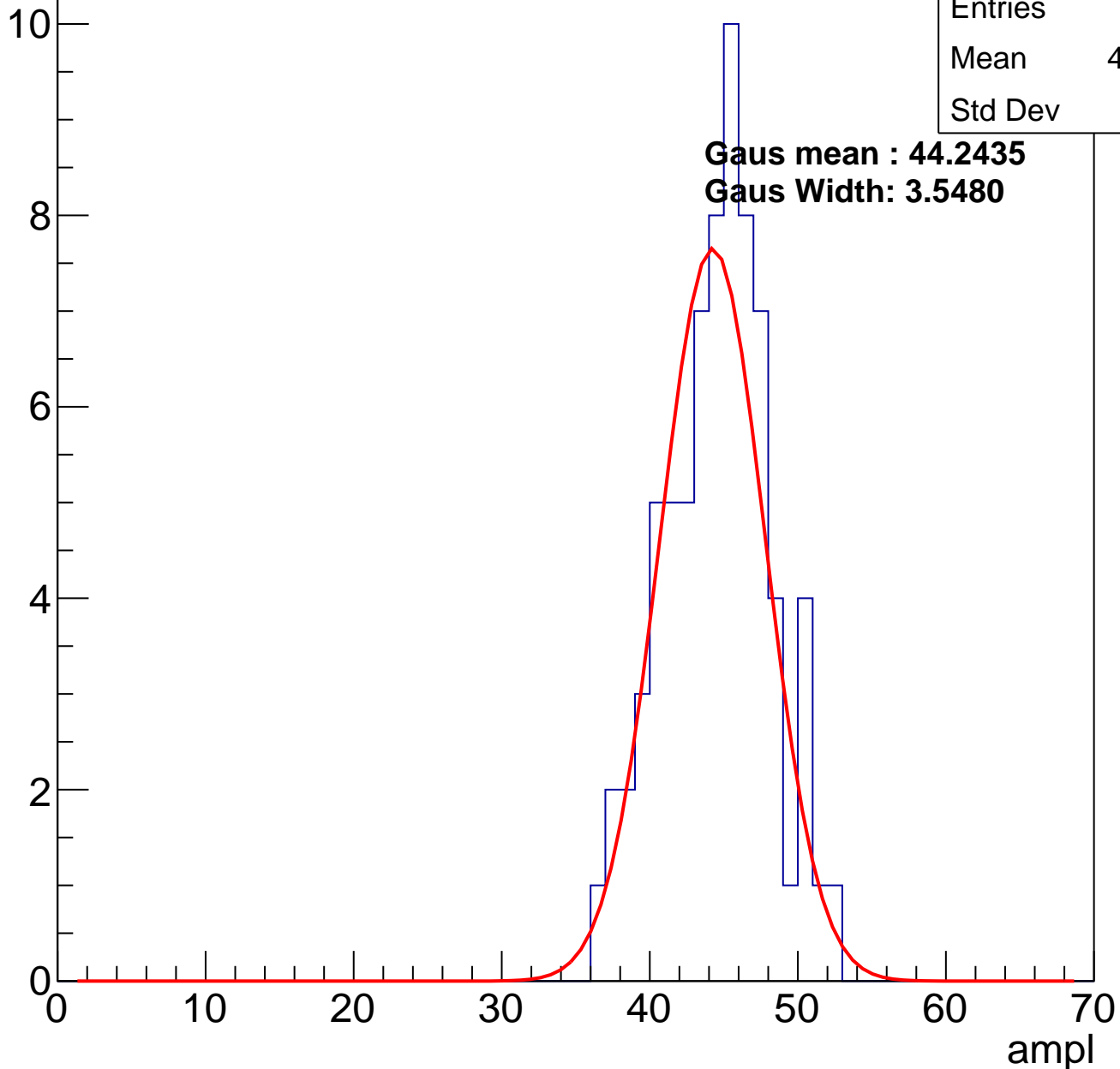
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	74
Mean	44.08
Std Dev	3.51

**Gaus mean : 44.2435**

**Gaus Width: 3.5480**

Entry

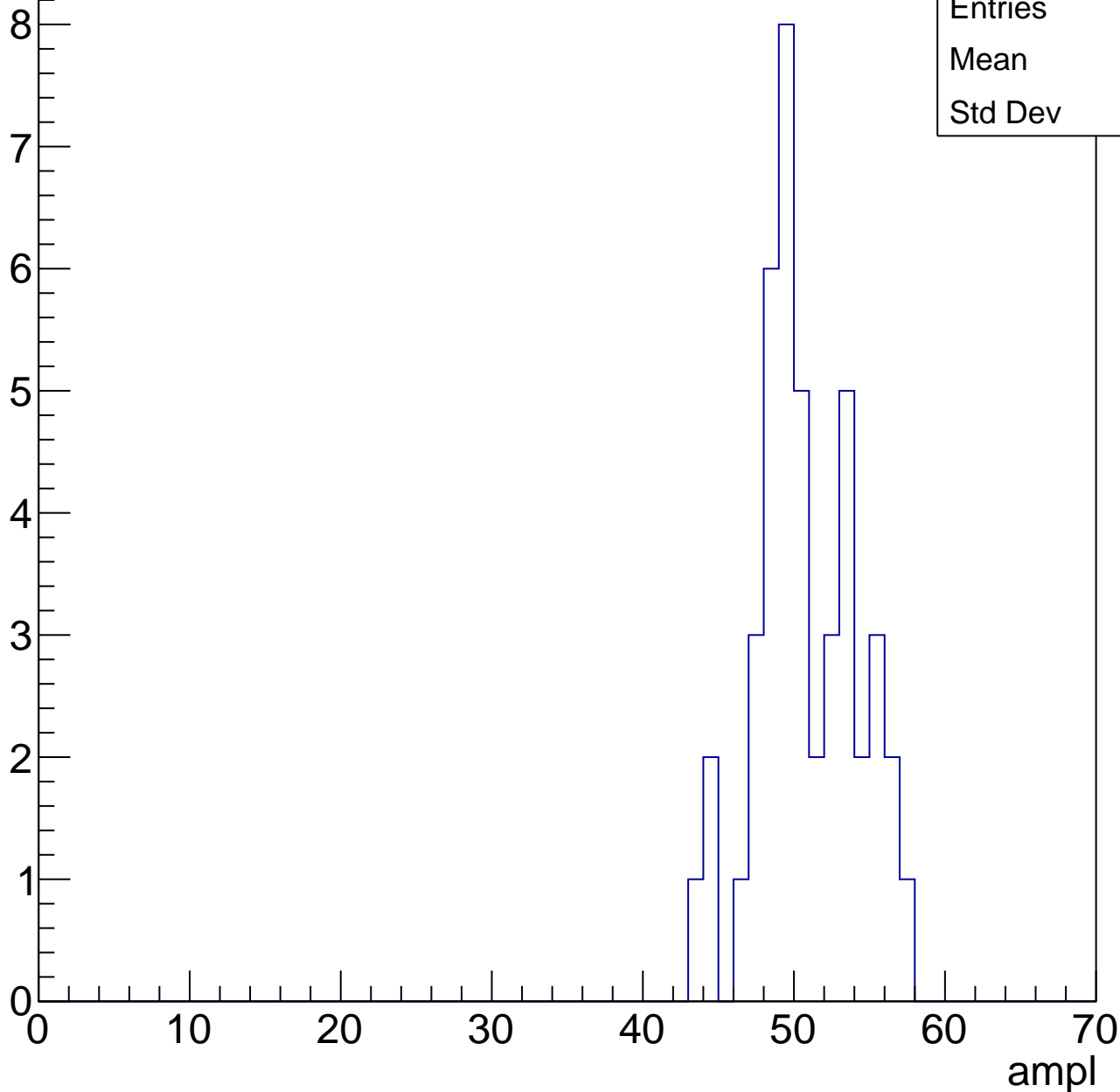


# B0L001S, U5-ch3, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	44
Mean	50.3
Std Dev	3.3

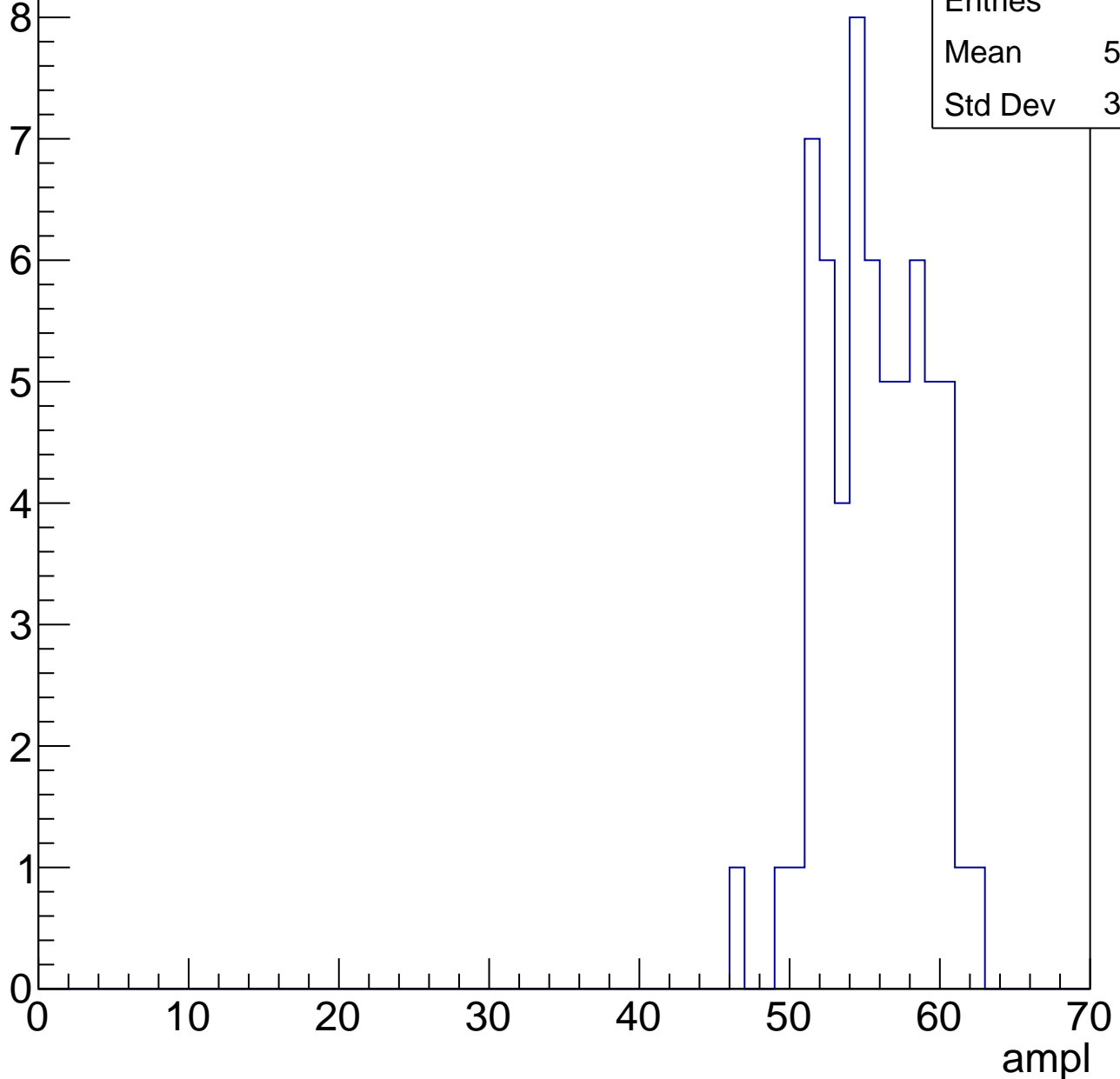


# B0L001S, U5-ch3, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

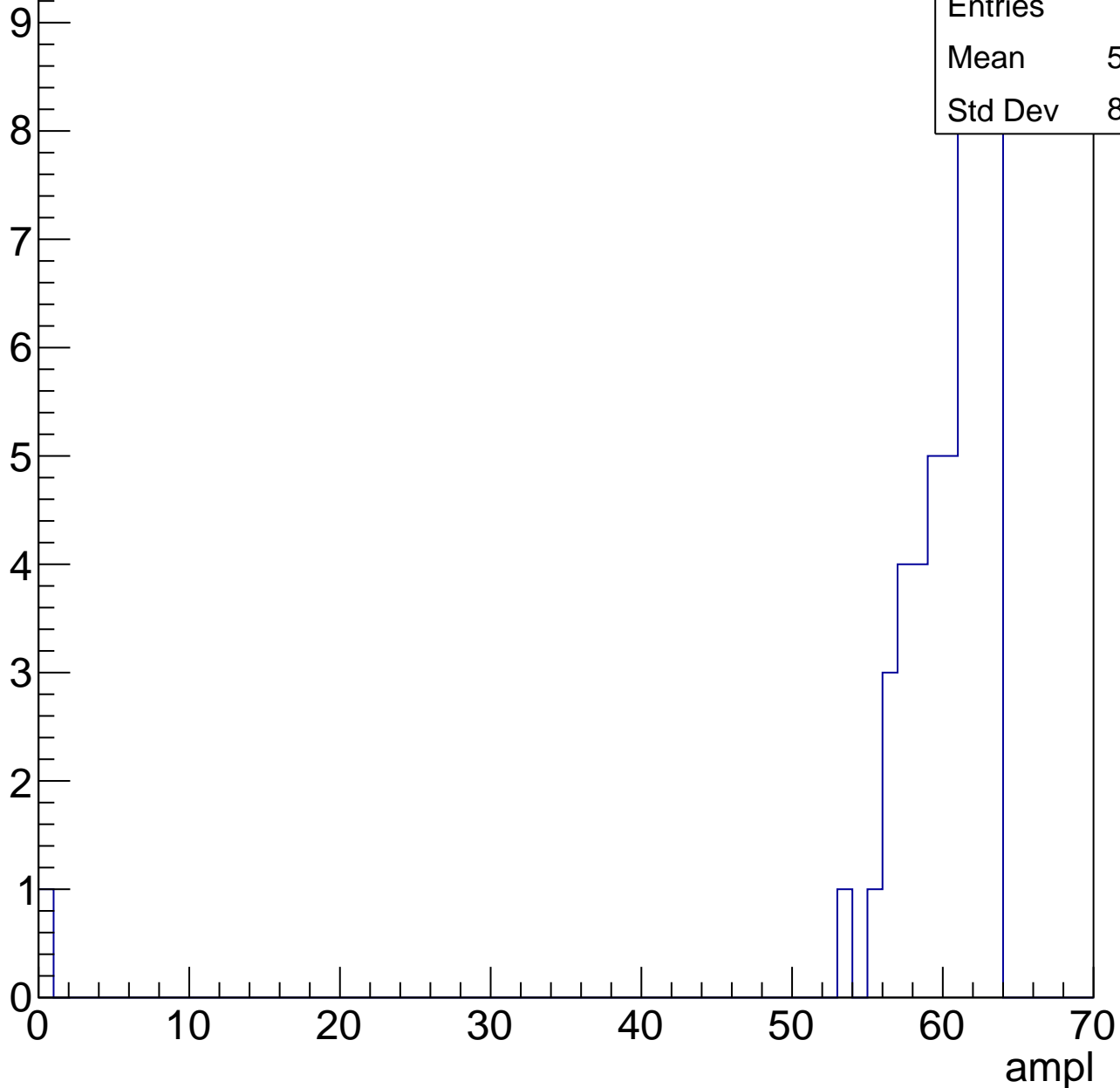
Entries	62
Mean	55.15
Std Dev	3.359



# B0L001S, U5-ch3, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch3, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch3, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U5-ch4, adc0

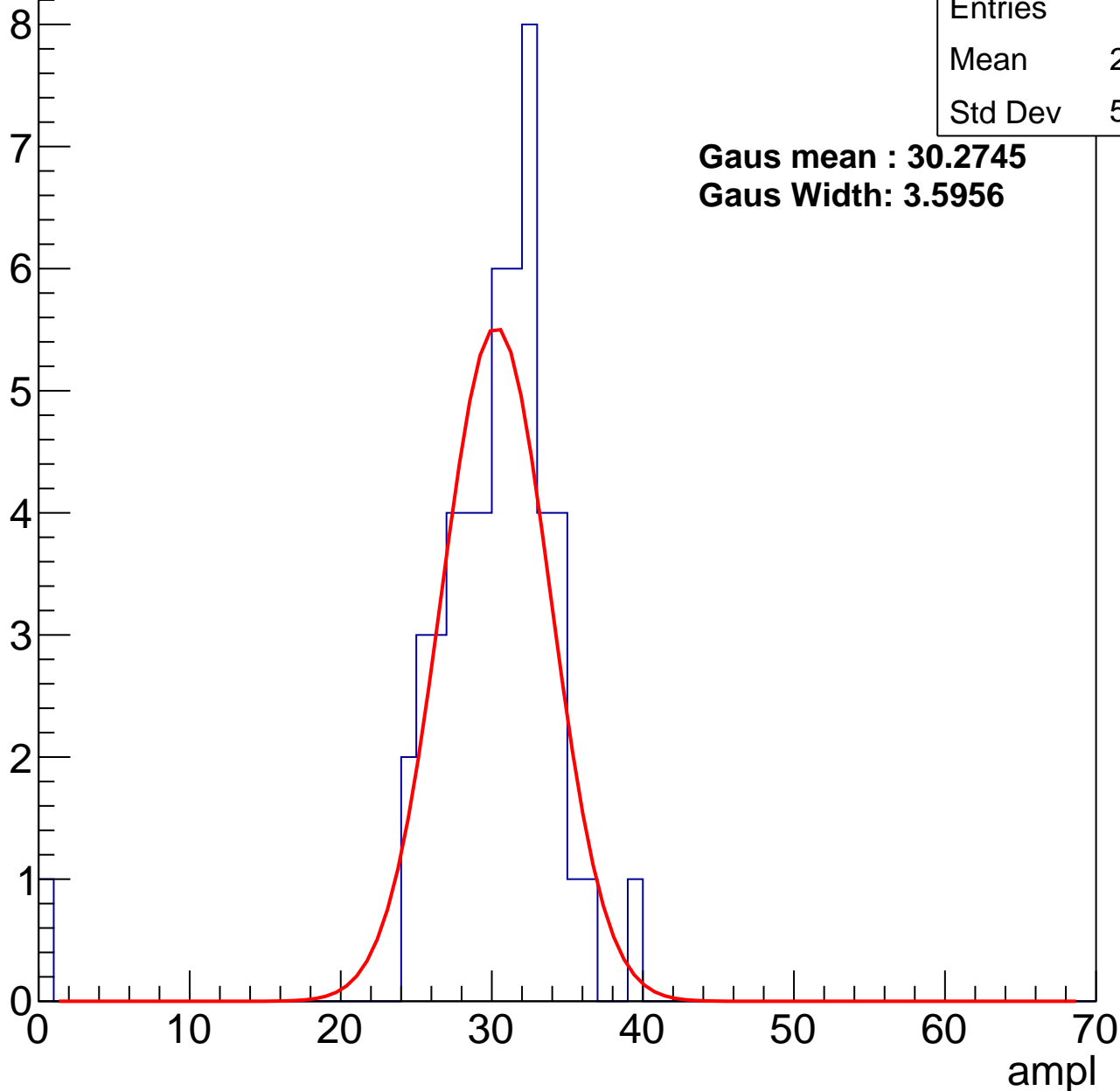
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	29.56
Std Dev	5.227

**Gaus mean : 30.2745**

**Gaus Width: 3.5956**



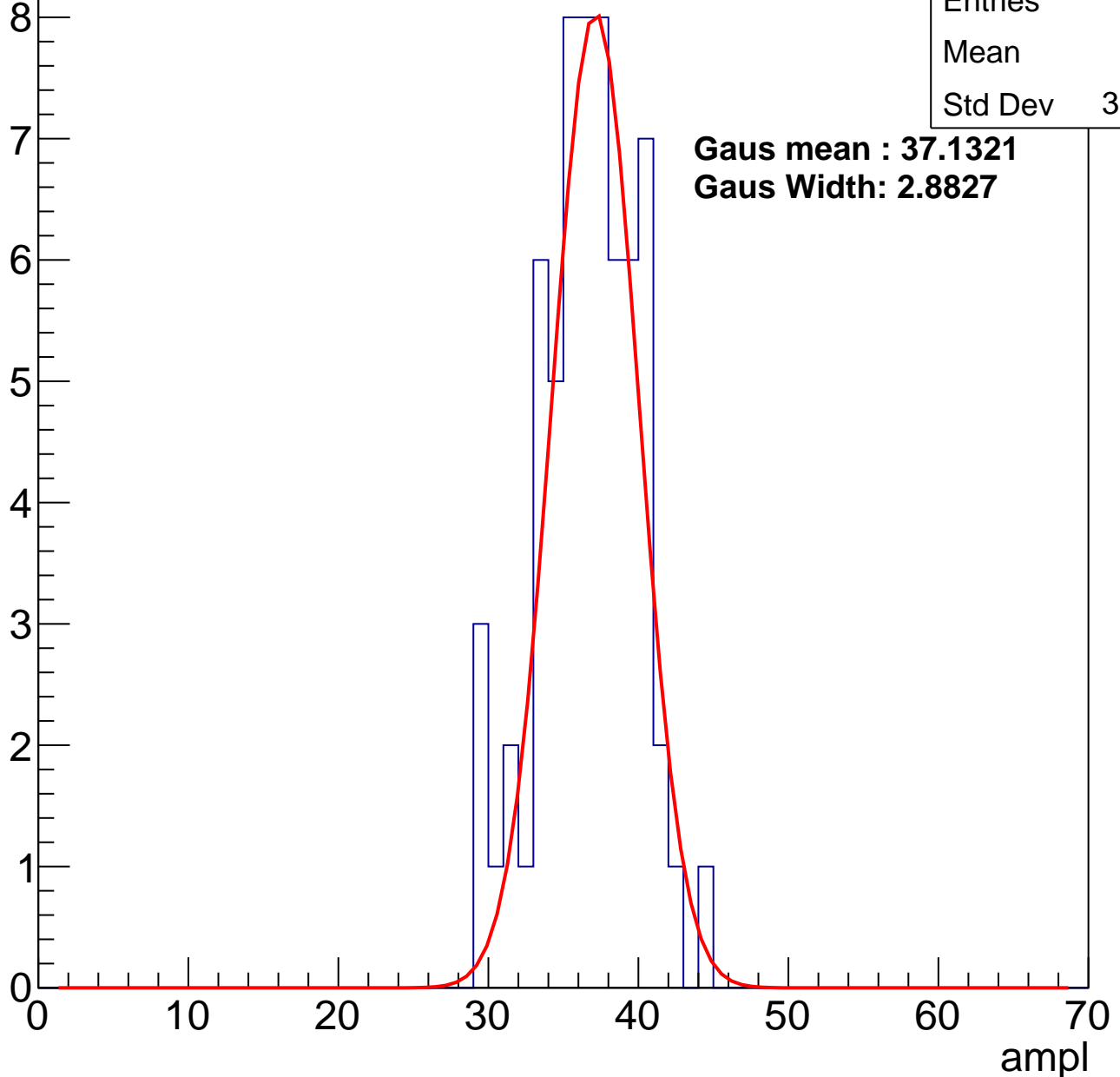
# B0L001S, U5-ch4, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	36.2
Std Dev	3.226

**Gaus mean : 37.1321**  
**Gaus Width: 2.8827**



# B0L001S, U5-ch4, adc2

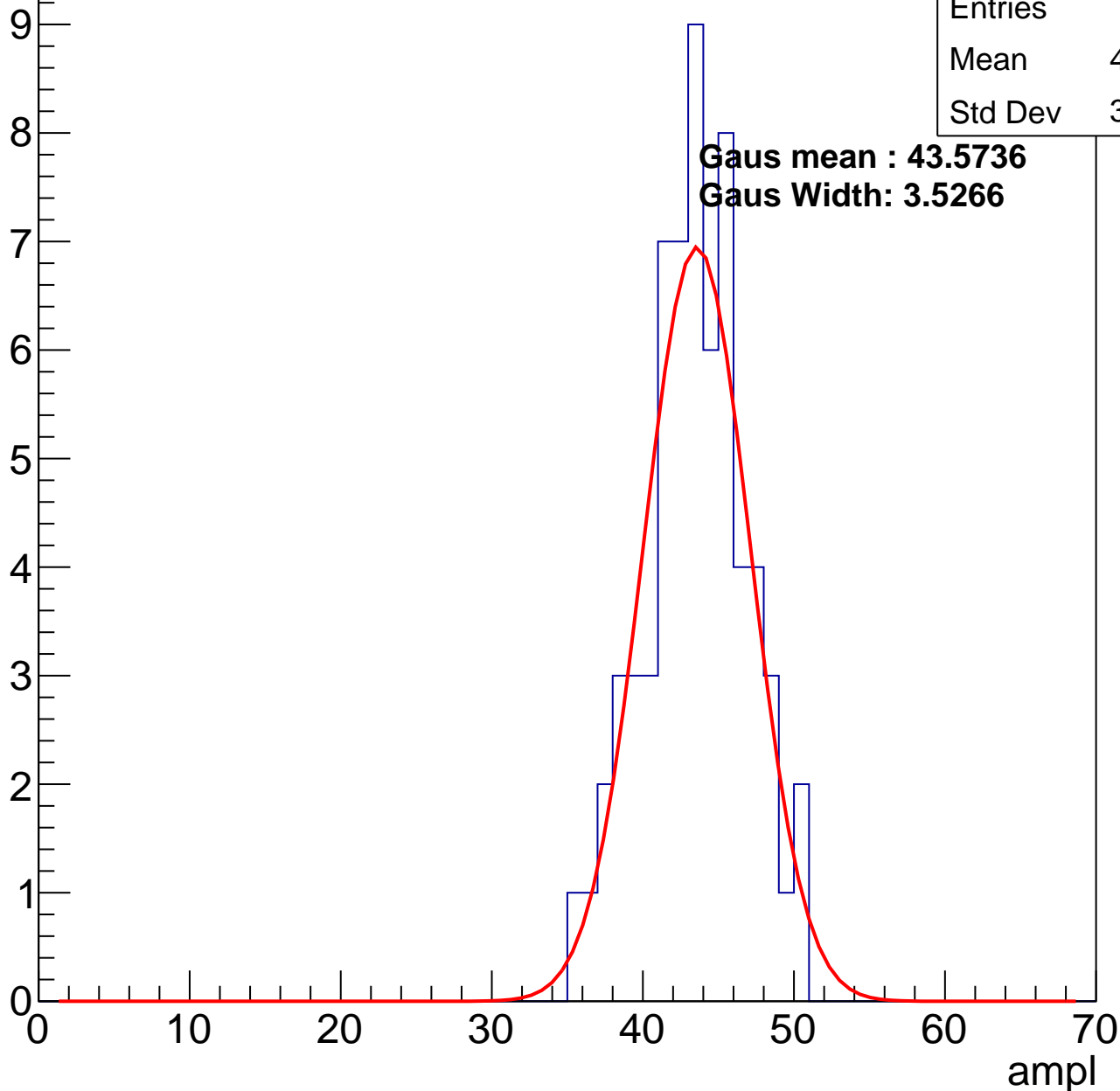
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	43.02
Std Dev	3.347

**Gaus mean : 43.5736**

**Gaus Width: 3.5266**

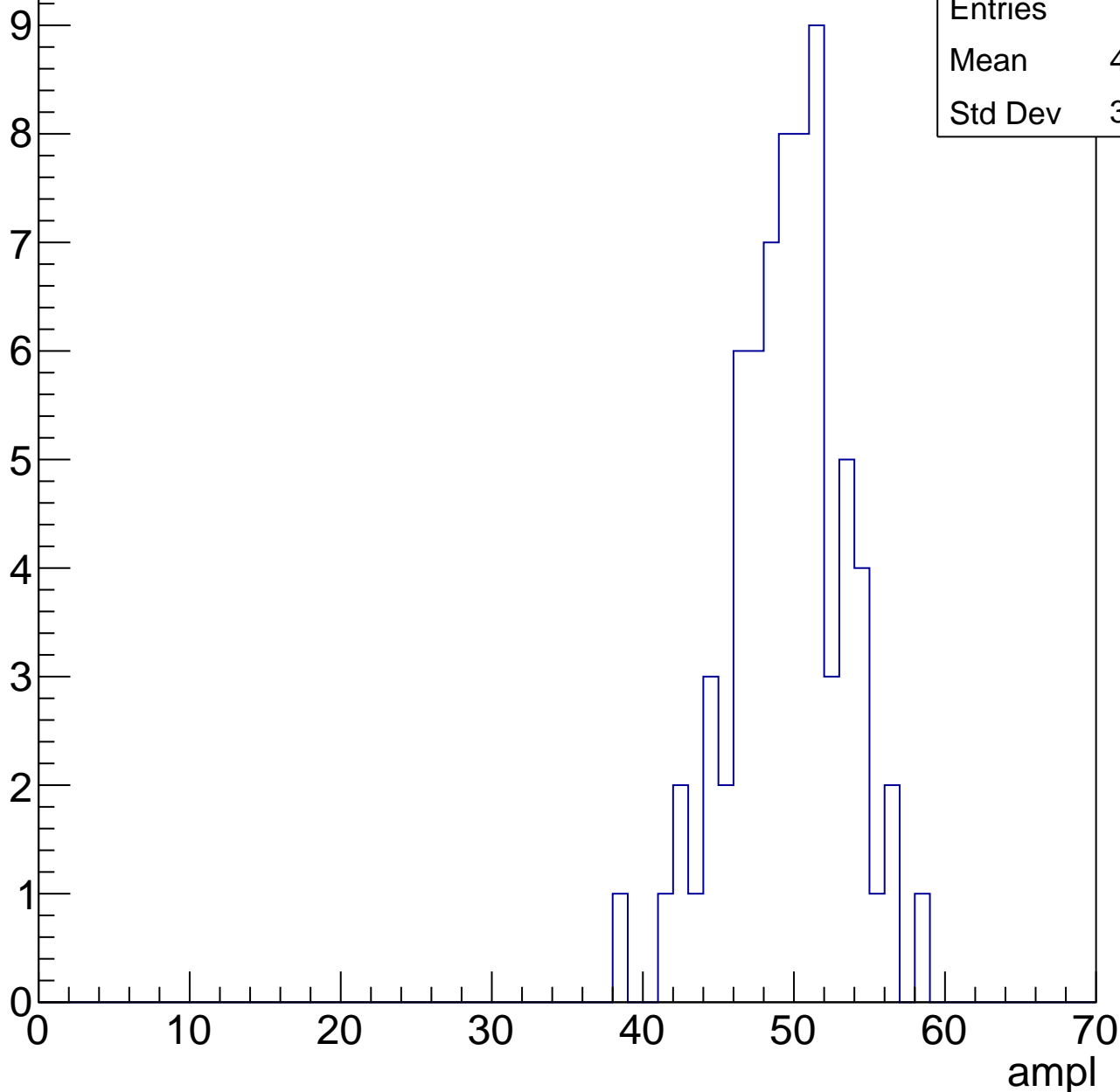


# B0L001S, U5-ch4, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

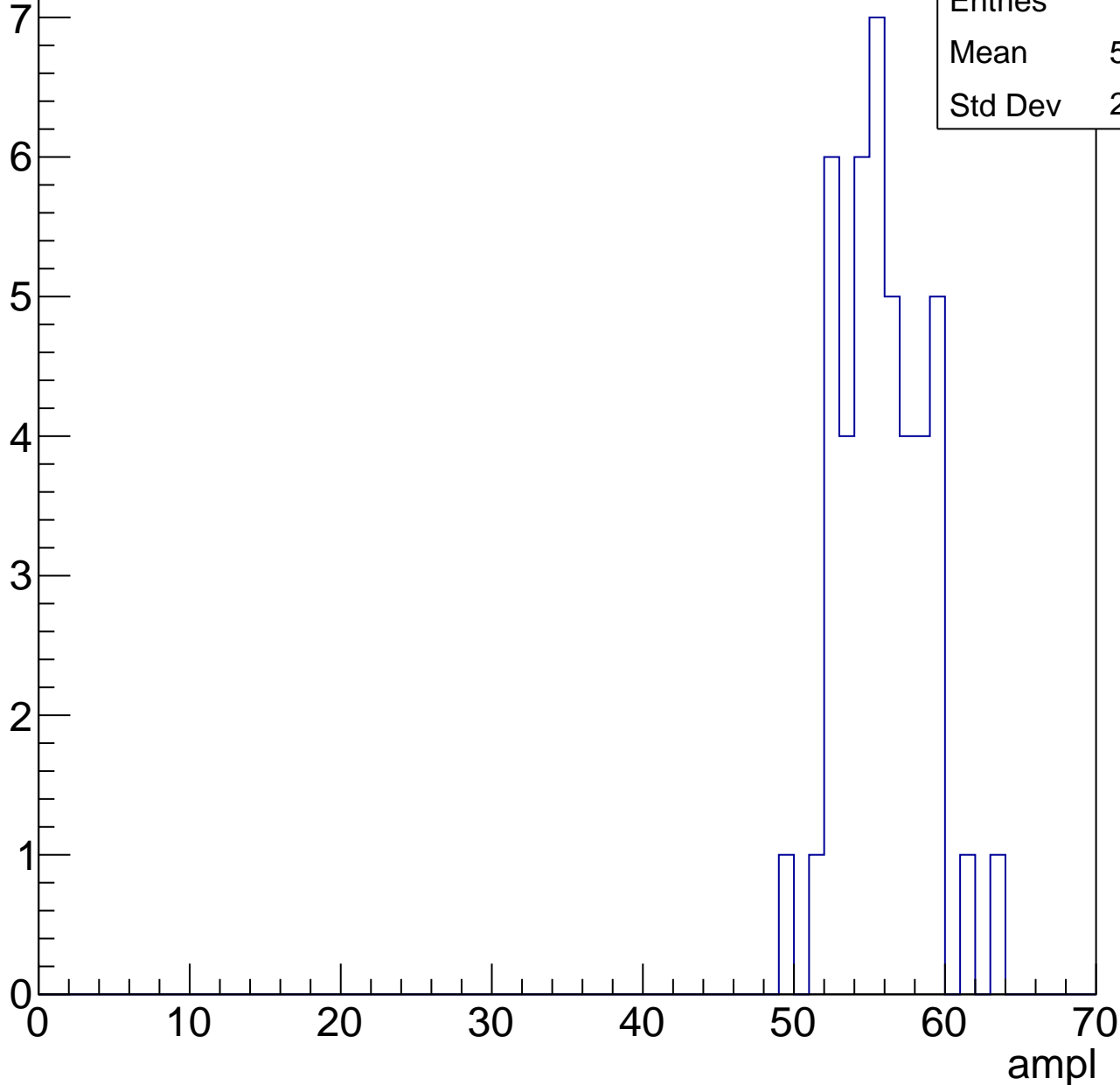
Entries	70
Mean	49.07
Std Dev	3.735



# B0L001S, U5-ch4, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

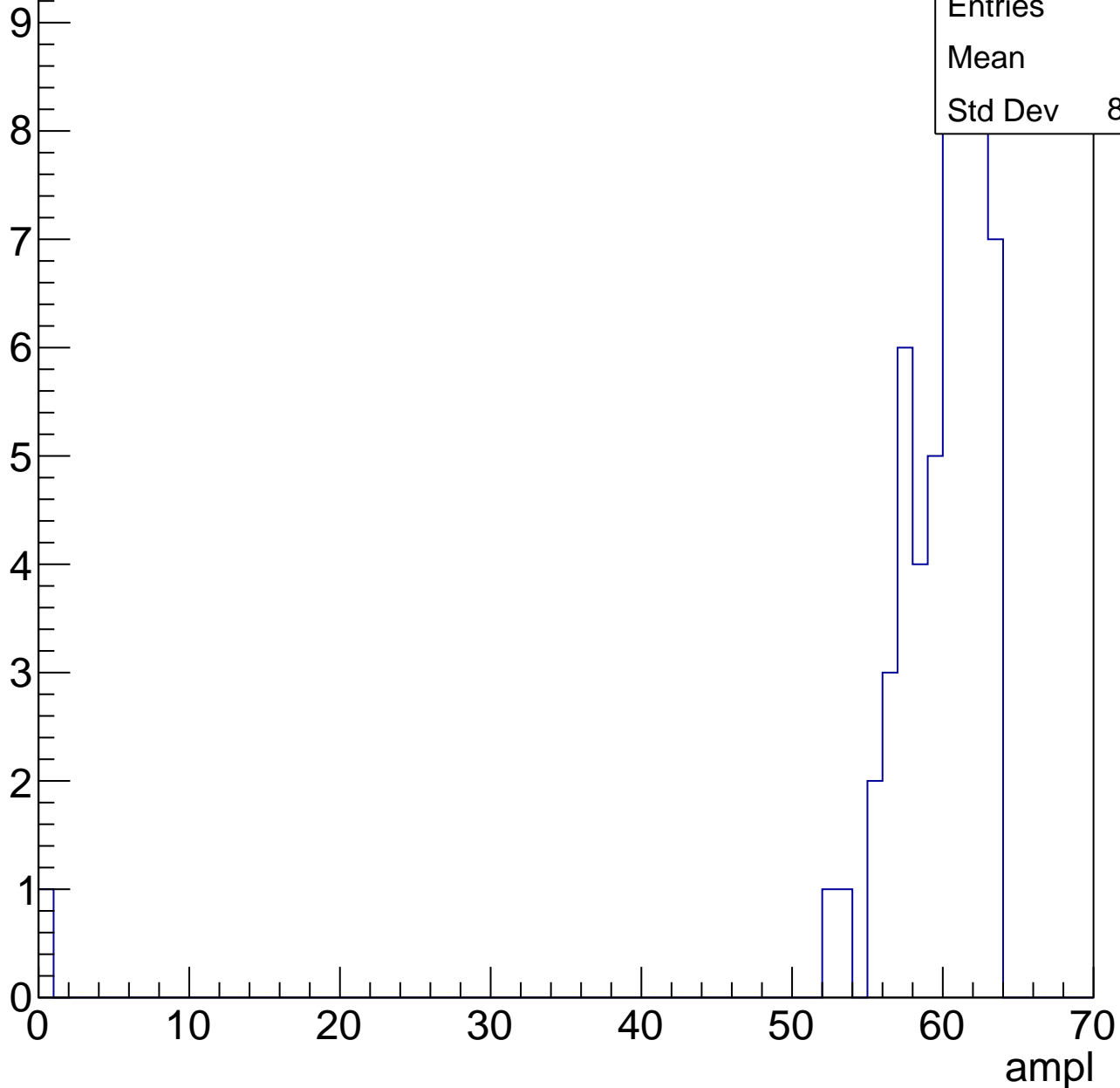
Entry



# B0L001S, U5-ch4, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

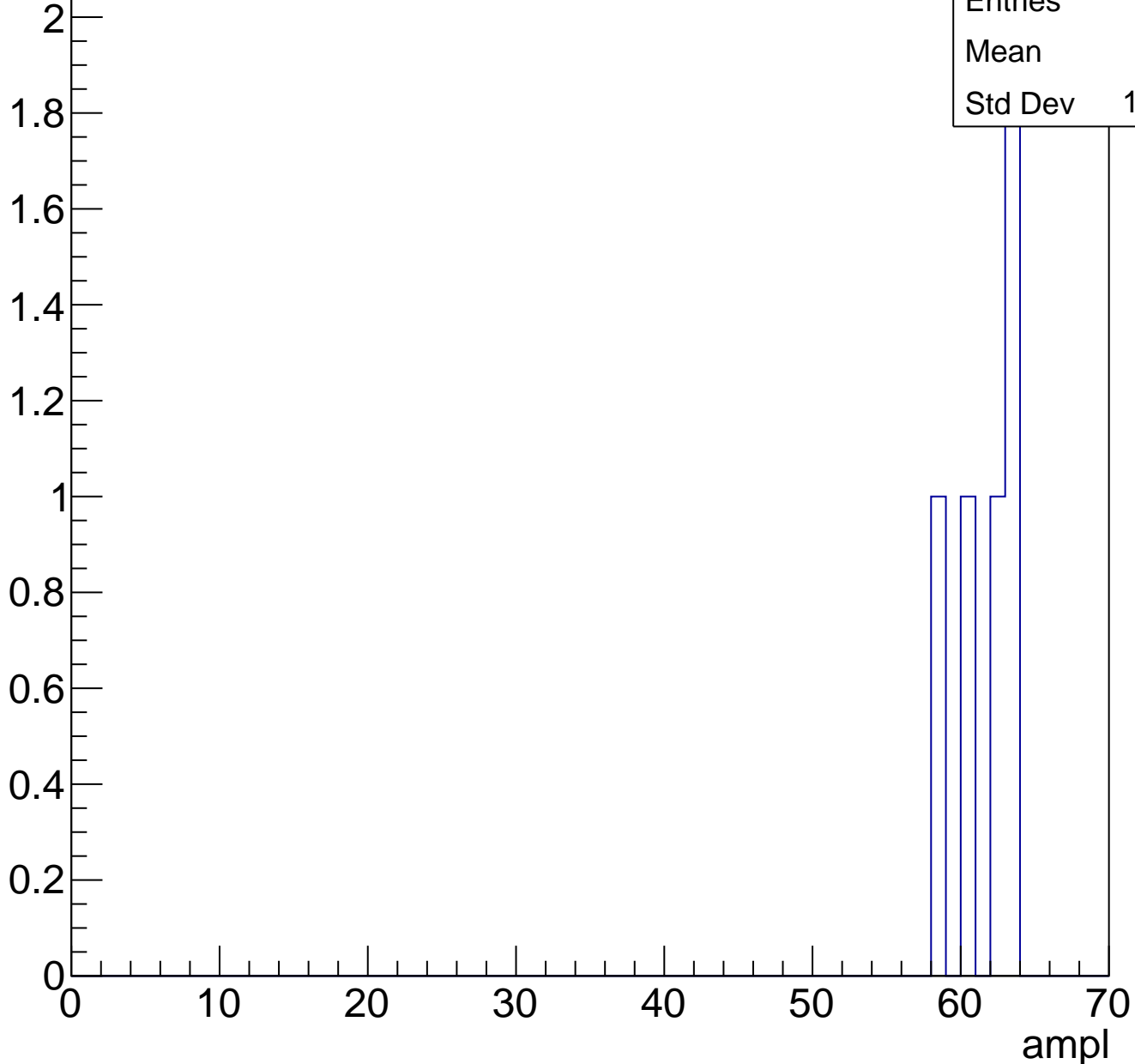
Entry



# B0L001S, U5-ch4, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch4, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch5, adc0

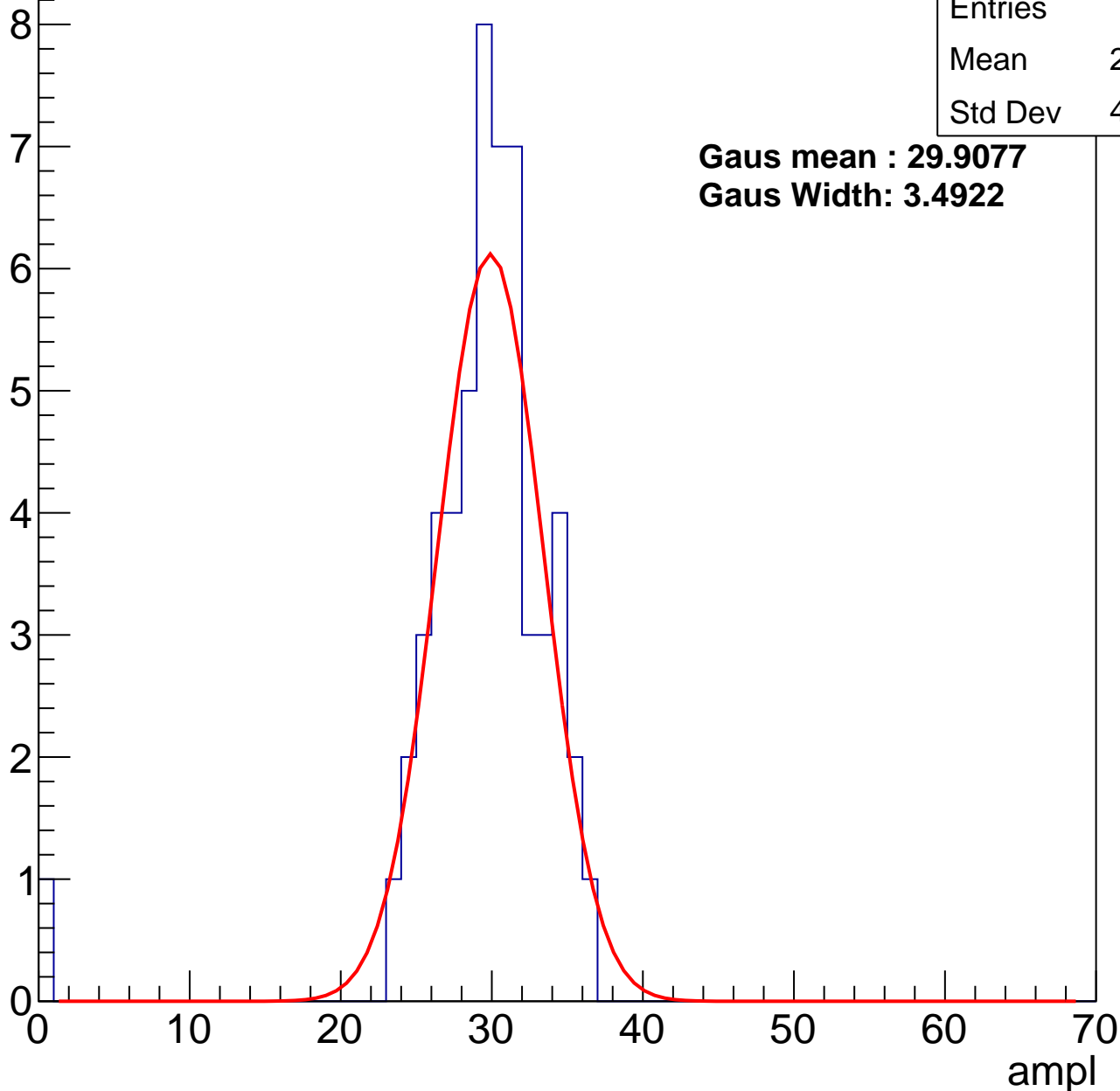
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	28.98
Std Dev	4.978

**Gaus mean : 29.9077**

**Gaus Width: 3.4922**



# B0L001S, U5-ch5, adc1

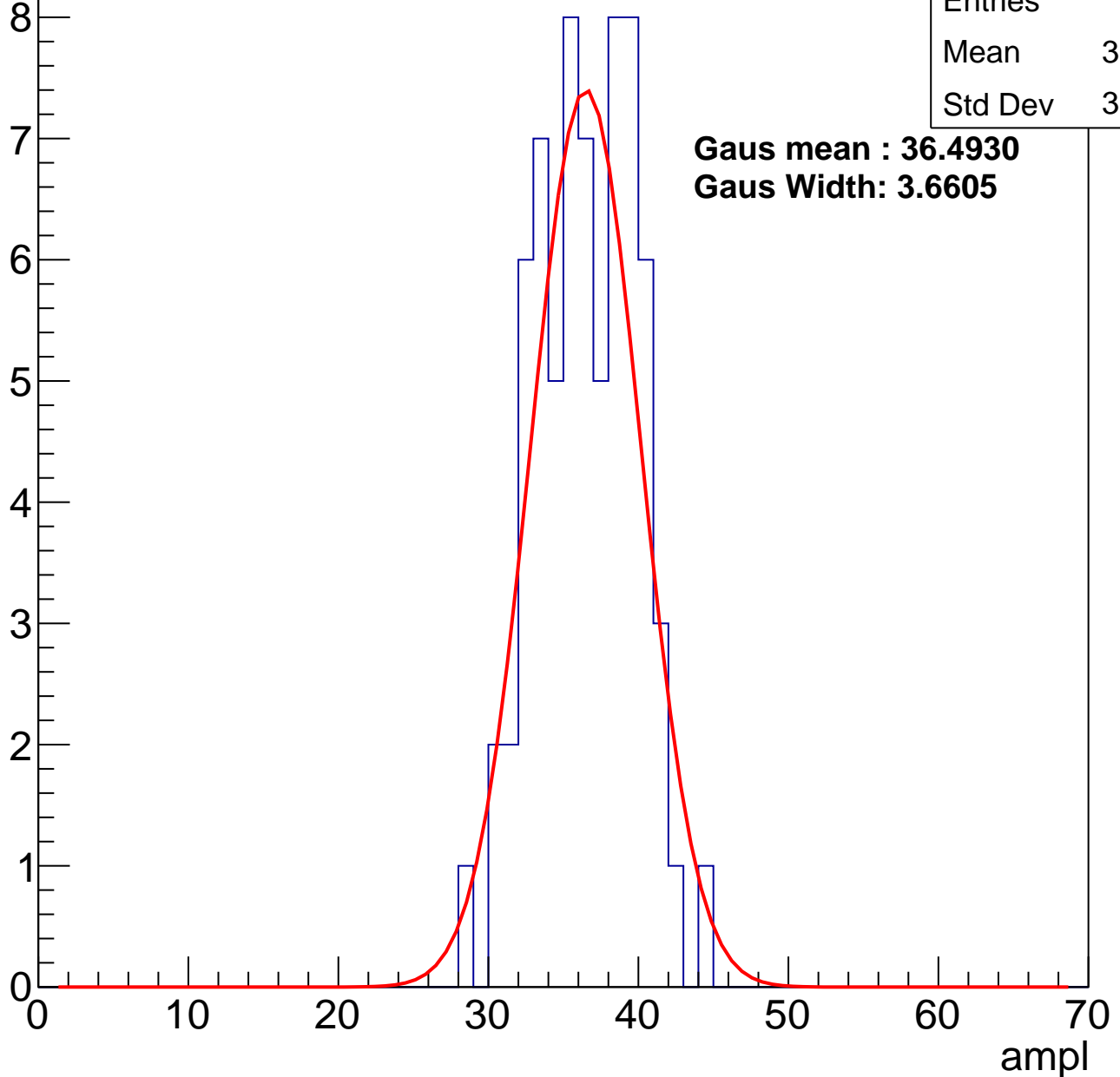
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	36.07
Std Dev	3.279

**Gaus mean : 36.4930**

**Gaus Width: 3.6605**



# B0L001S, U5-ch5, adc2

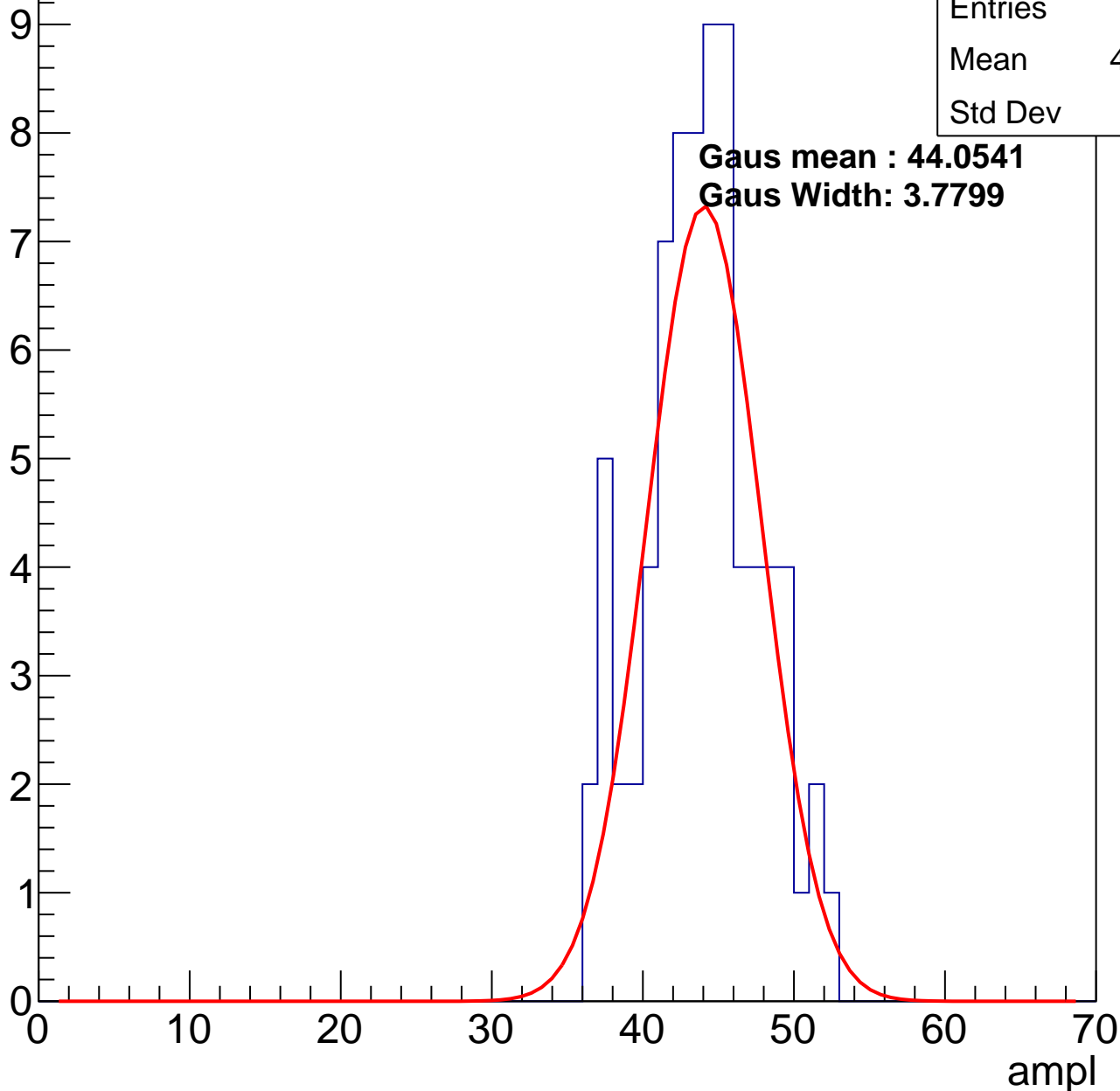
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	76
Mean	43.46
Std Dev	3.74

**Gaus mean : 44.0541**

**Gaus Width: 3.7799**

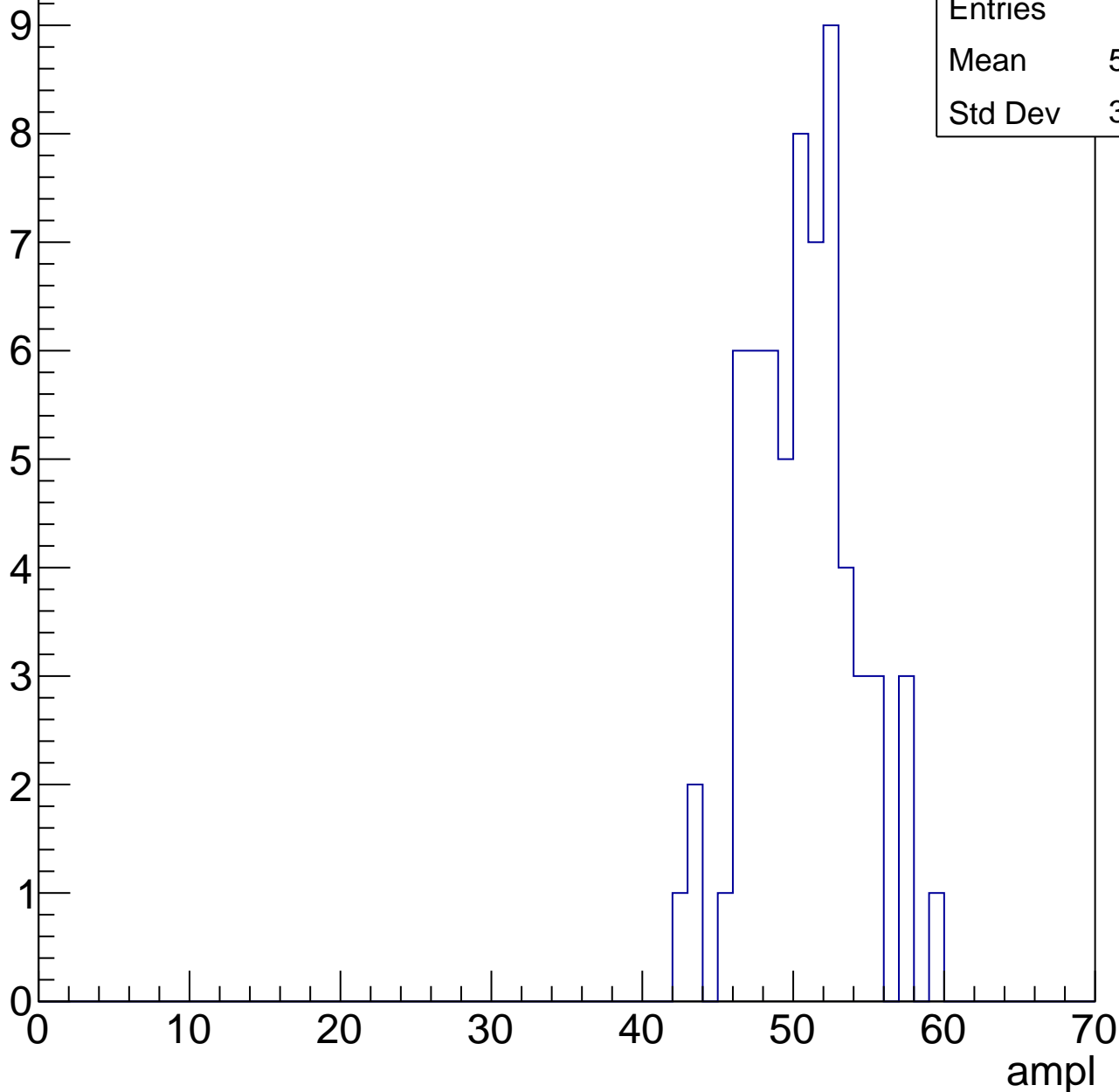


# B0L001S, U5-ch5, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

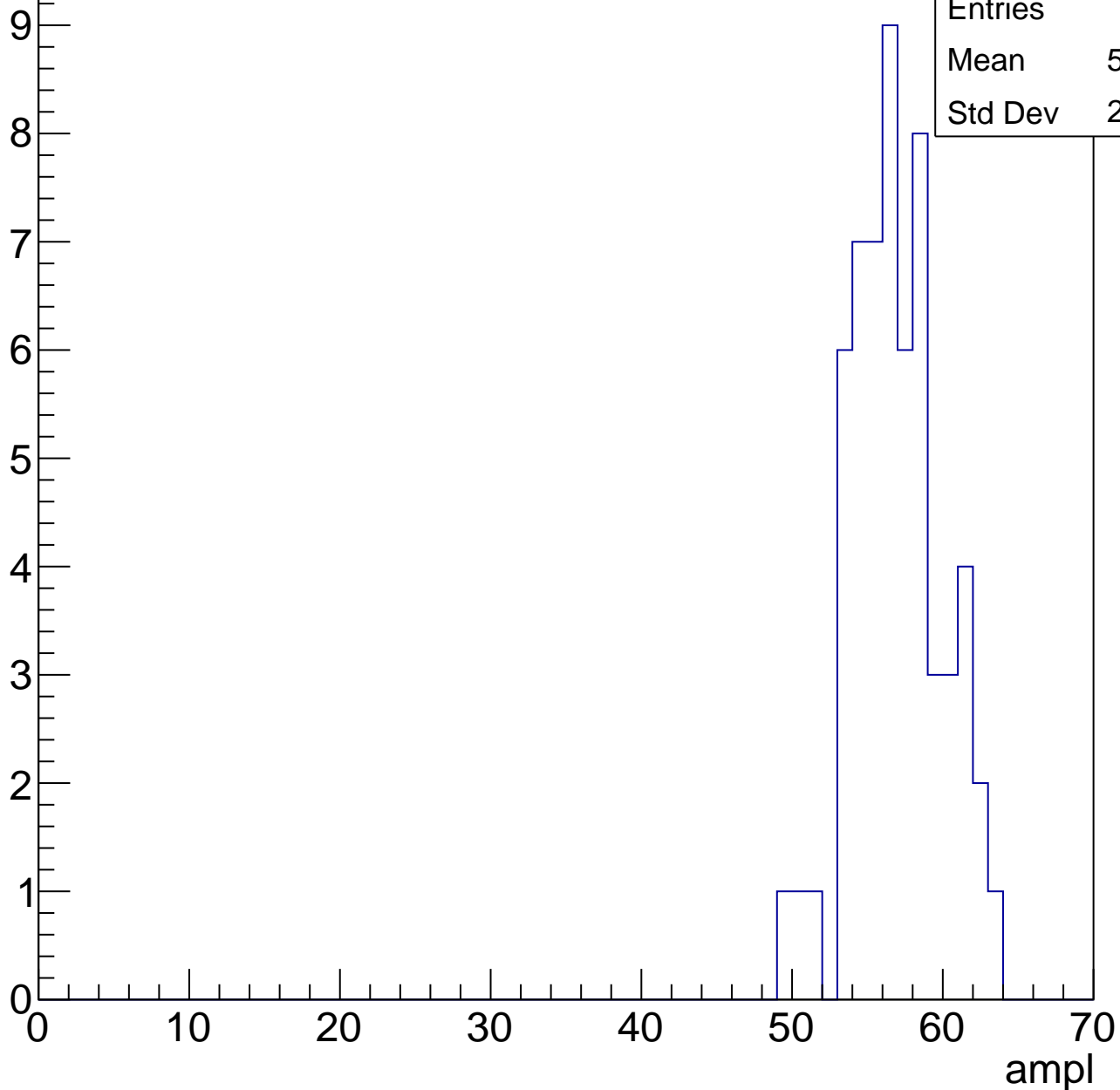
Entries	65
Mean	50.12
Std Dev	3.497



# B0L001S, U5-ch5, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



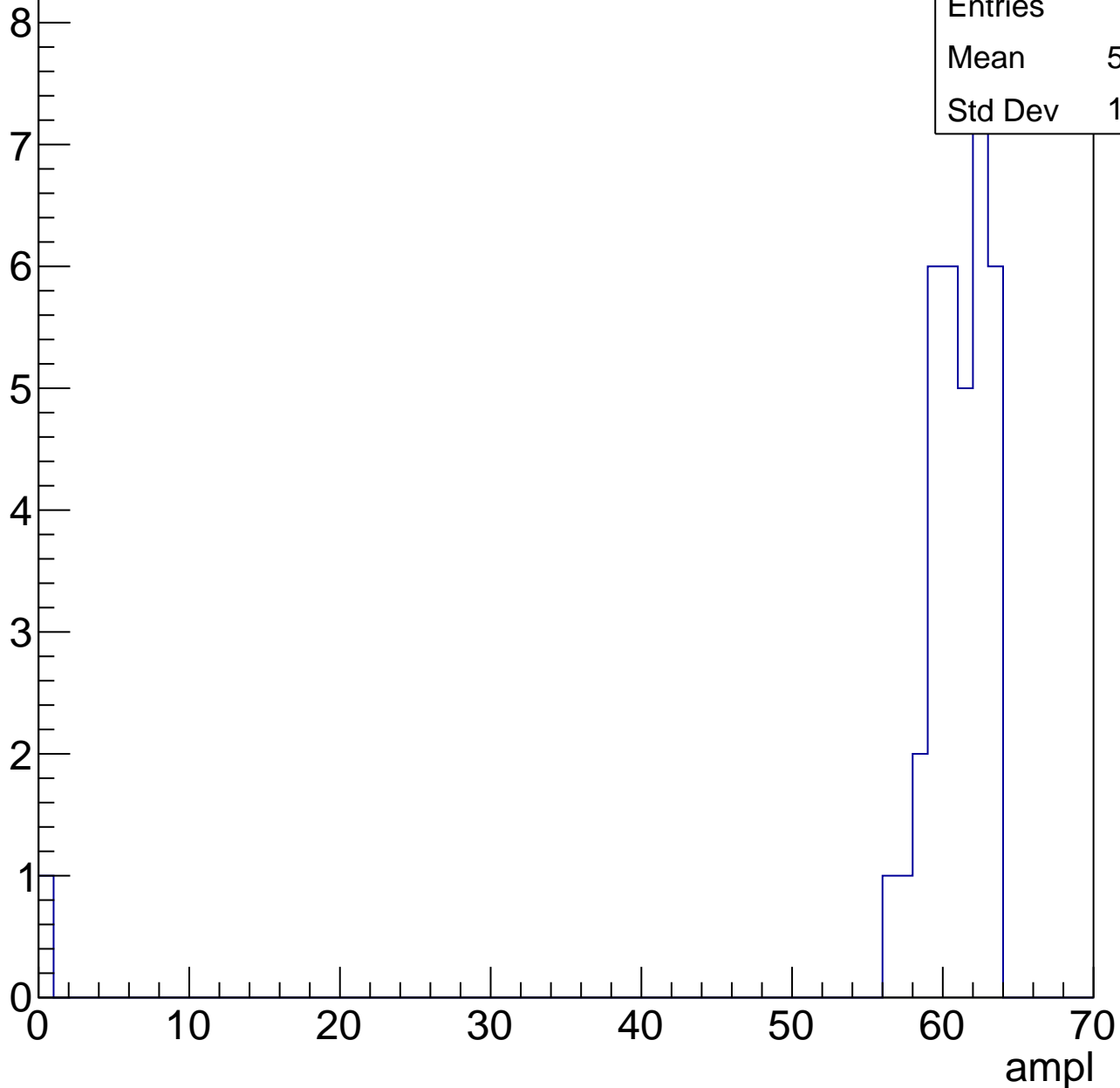
Entries	59
Mean	56.42
Std Dev	2.976

# B0L001S, U5-ch5, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	36
Mean	58.94
Std Dev	10.12



# B0L001S, U5-ch5, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

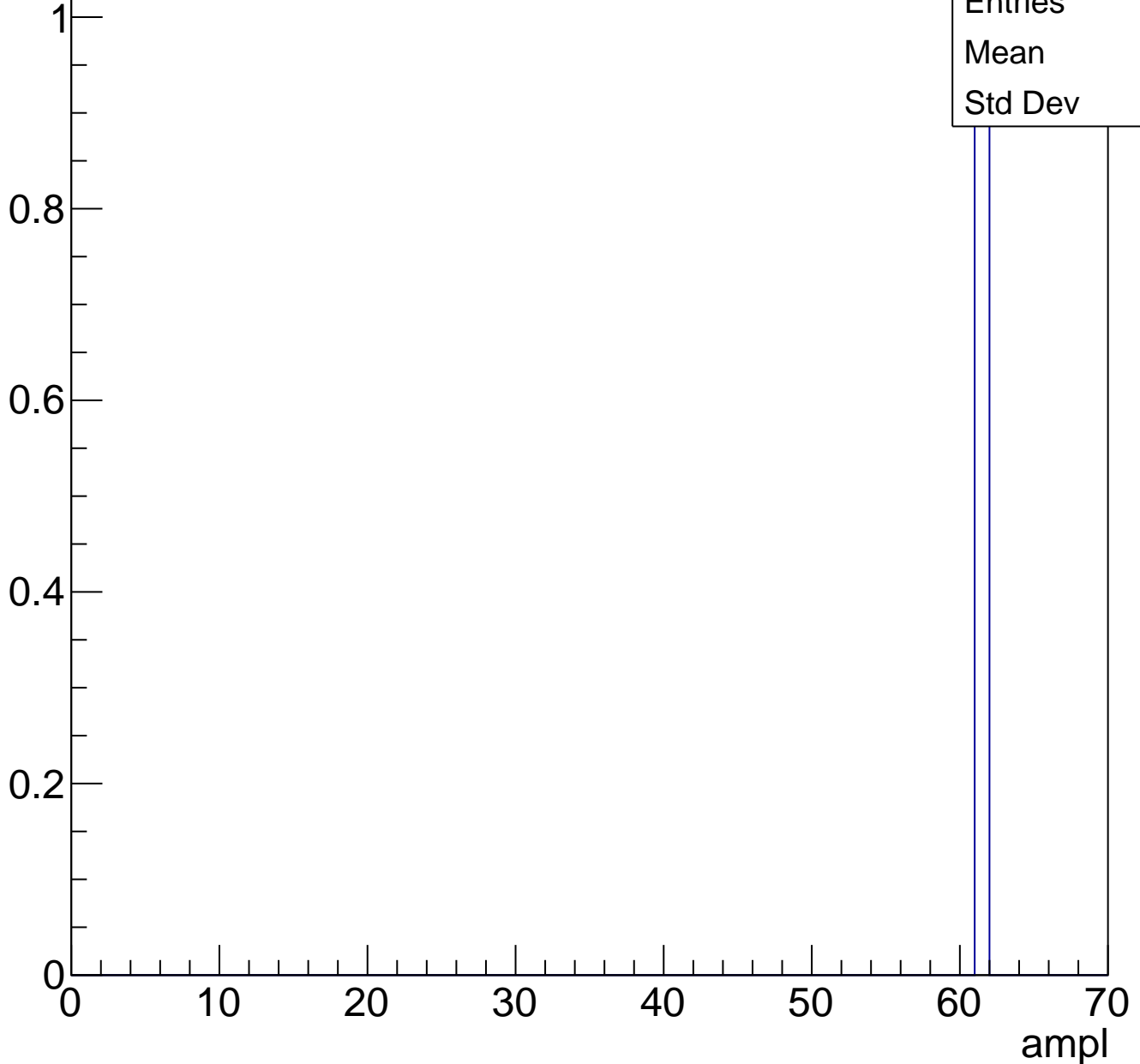




# B0L001S, U5-ch5, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch6, adc0

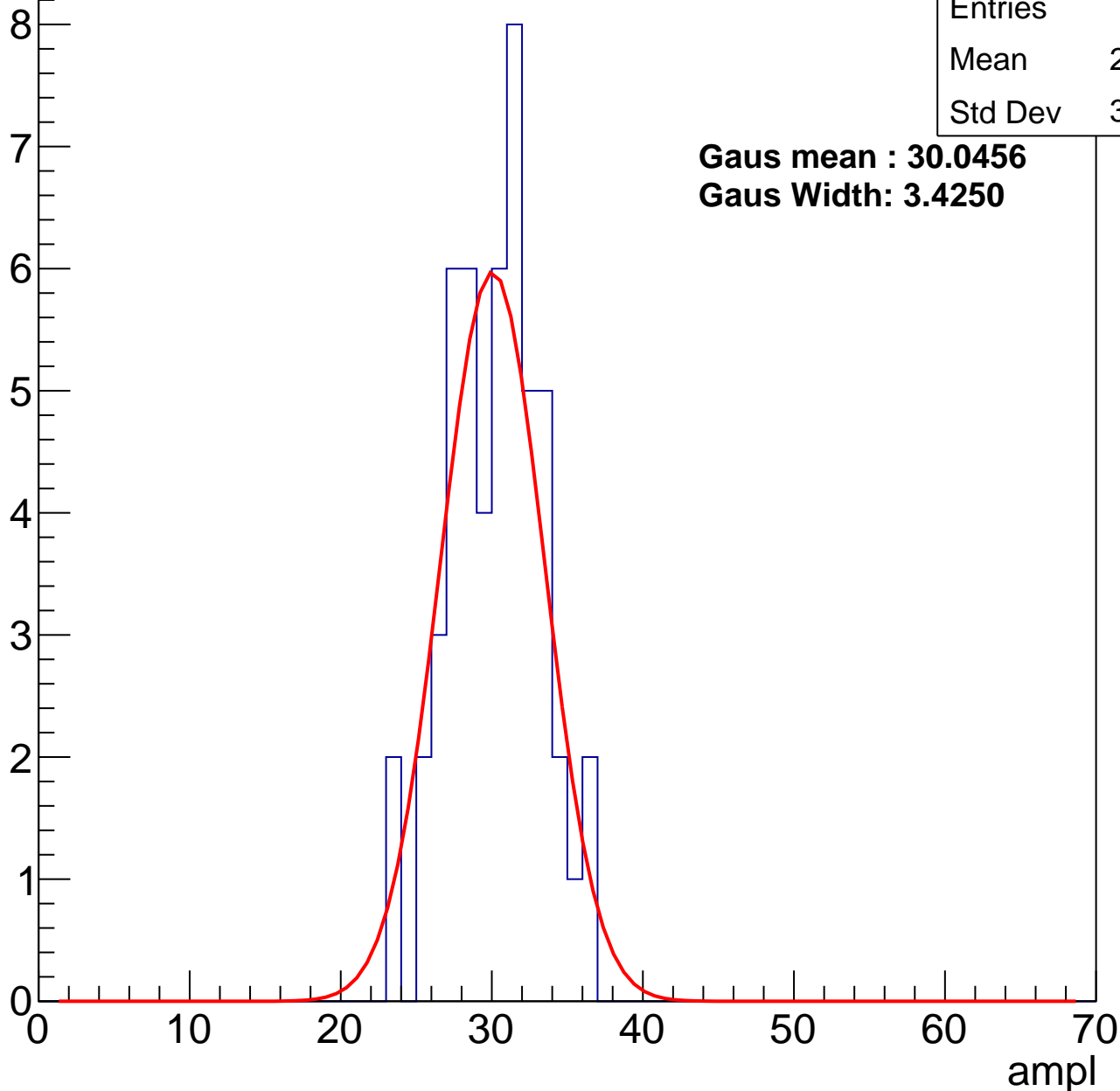
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	29.77
Std Dev	3.029

**Gaus mean : 30.0456**

**Gaus Width: 3.4250**



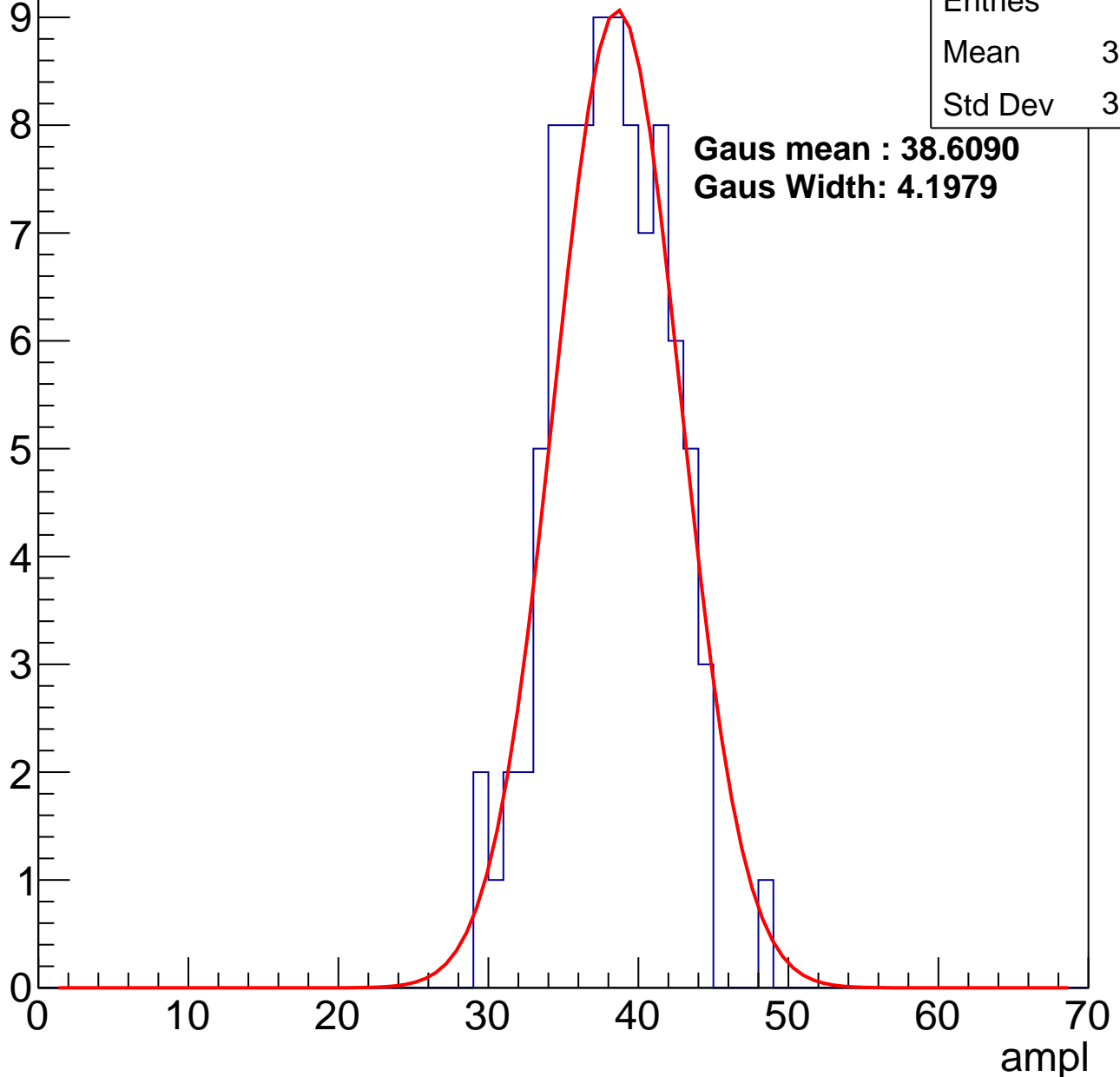
# B0L001S, U5-ch6, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	92
Mean	37.62
Std Dev	3.738

**Gaus mean : 38.6090**  
**Gaus Width: 4.1979**



# B0L001S, U5-ch6, adc2

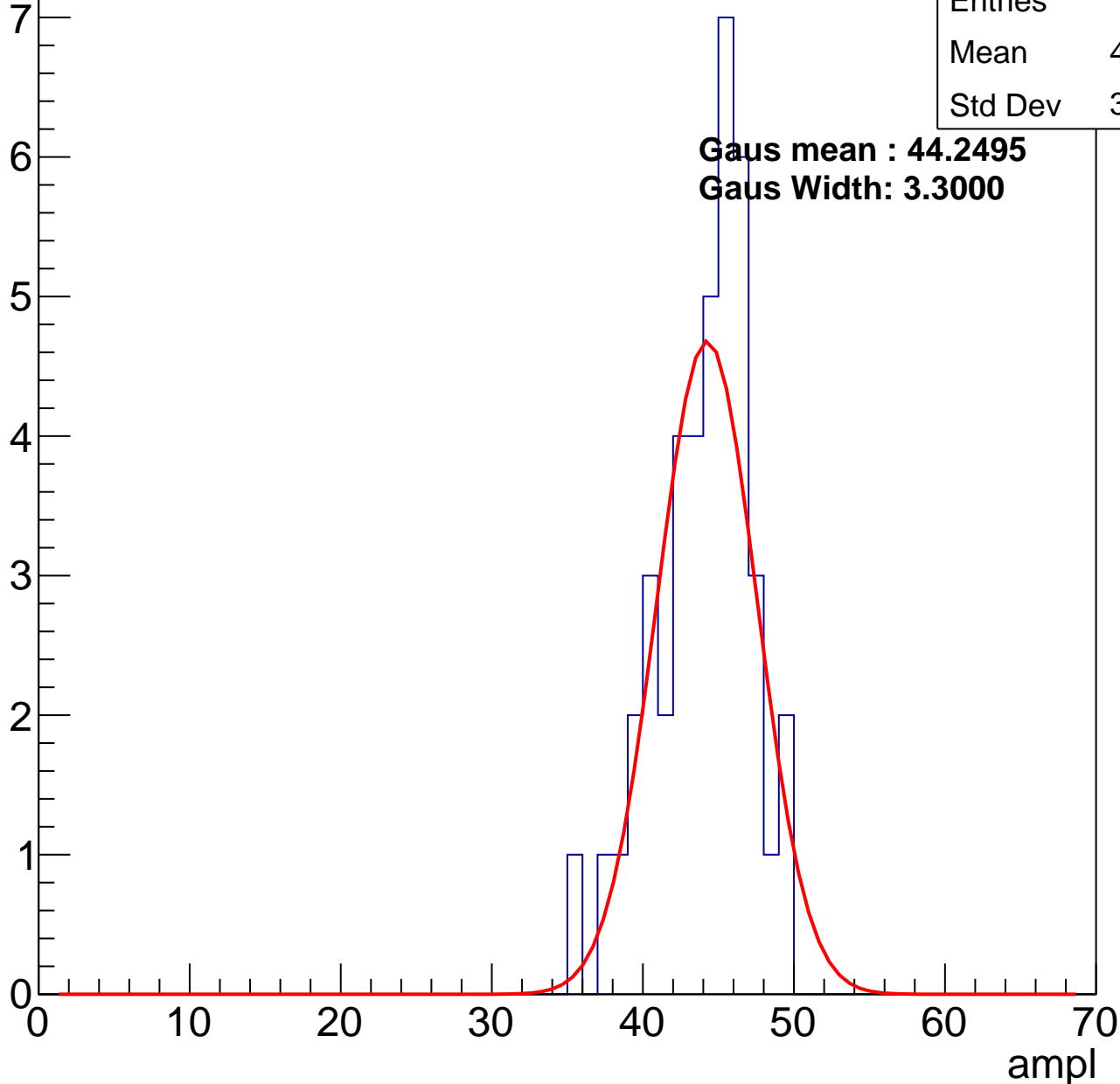
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	42
Mean	43.52
Std Dev	3.149

**Gaus mean : 44.2495**

**Gaus Width: 3.3000**

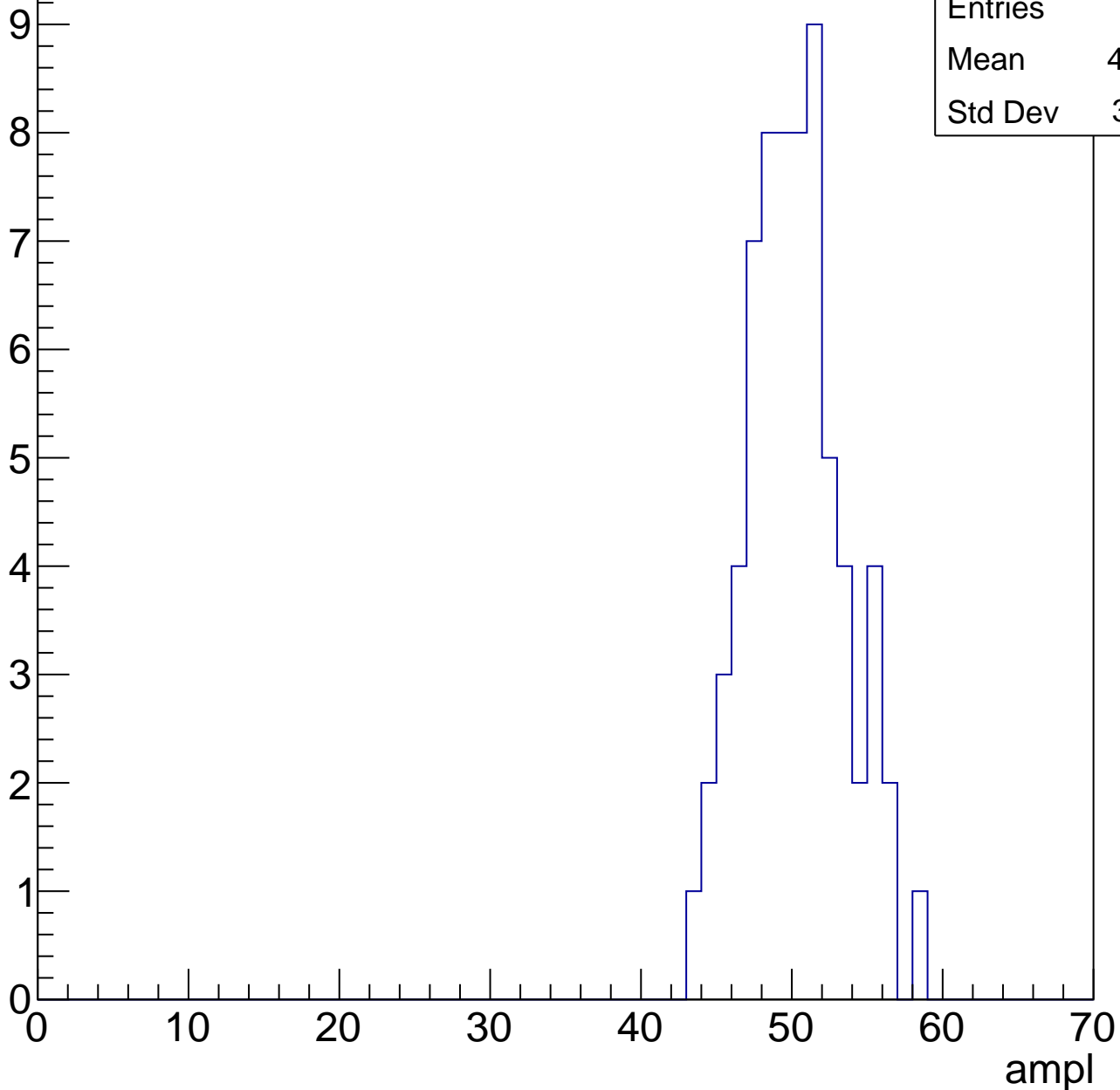


# B0L001S, U5-ch6, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	49.76
Std Dev	3.191

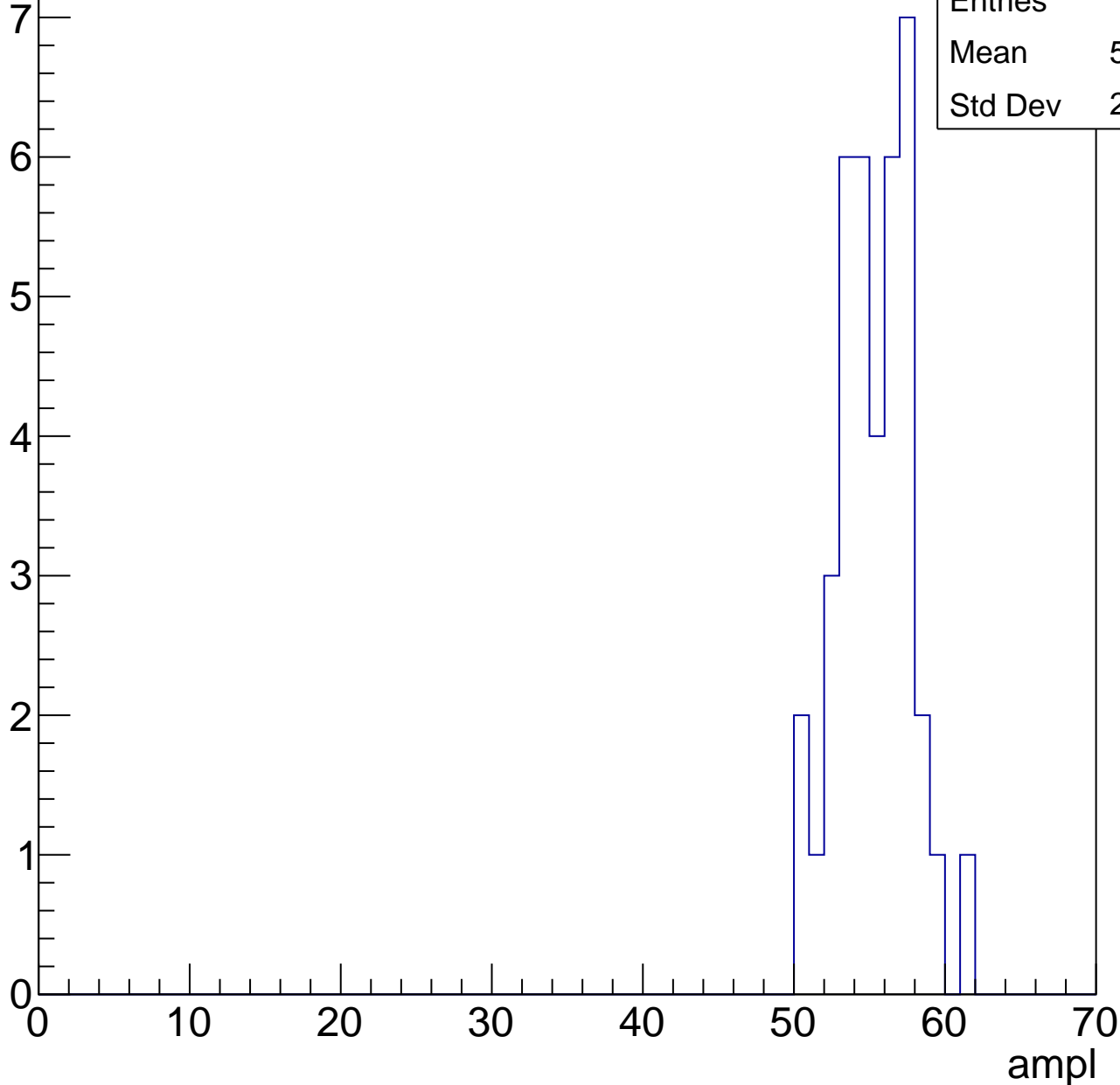


# B0L001S, U5-ch6, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

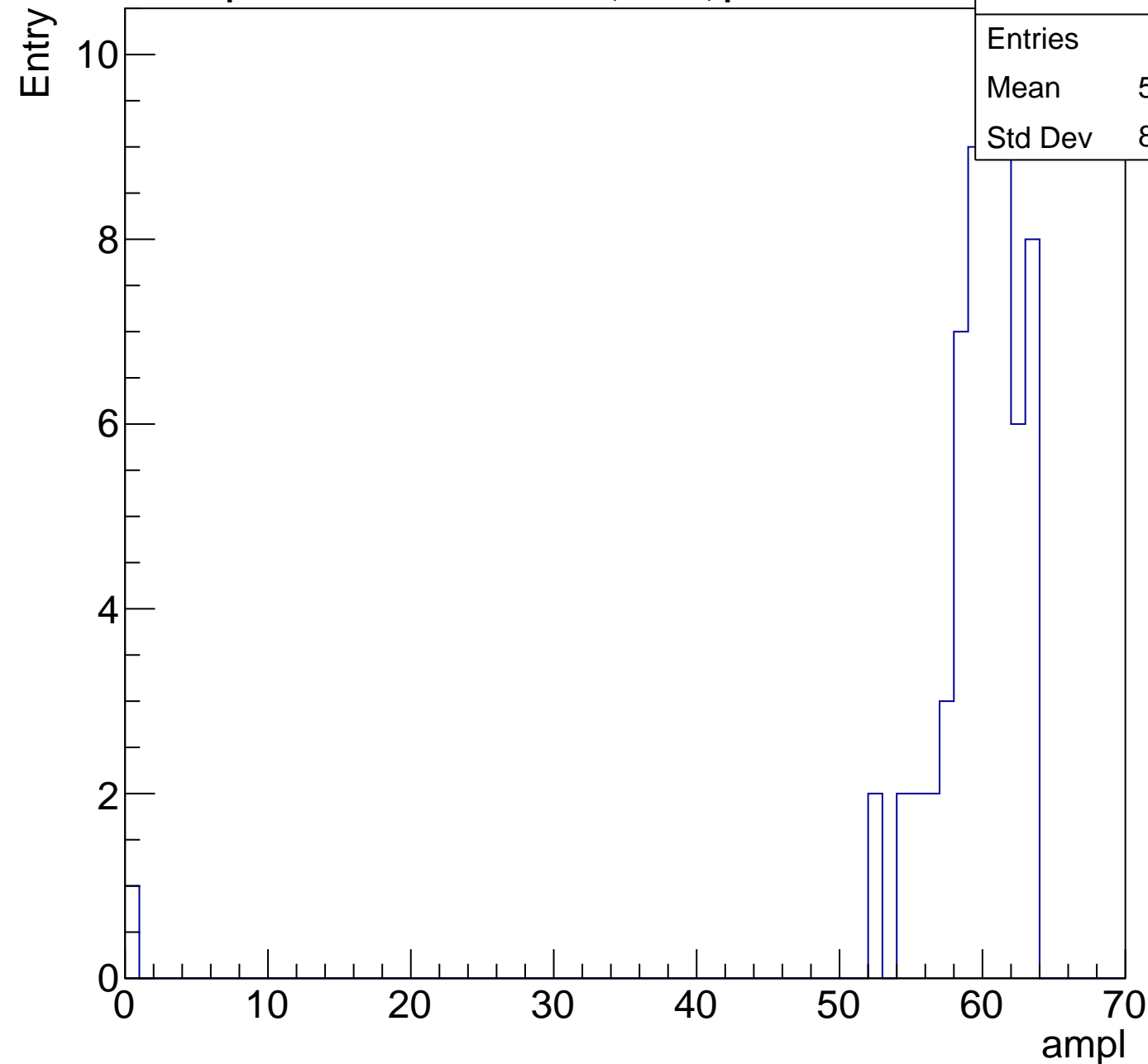
Entries	39
Mean	54.87
Std Dev	2.409



# B0L001S, U5-ch6, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

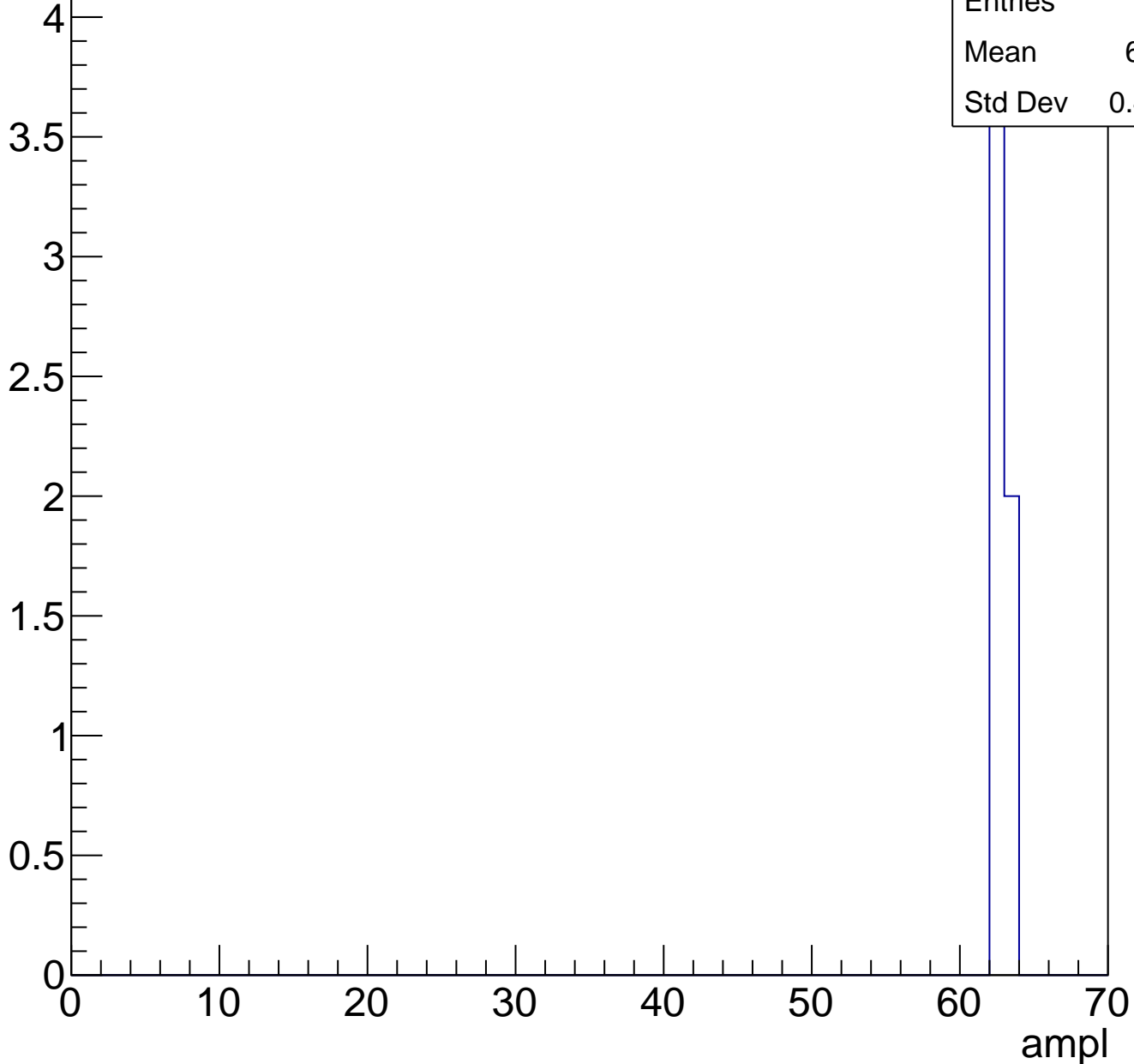
Entries	61
Mean	58.48
Std Dev	8.005



# B0L001S, U5-ch6, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch6, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch7, adc0

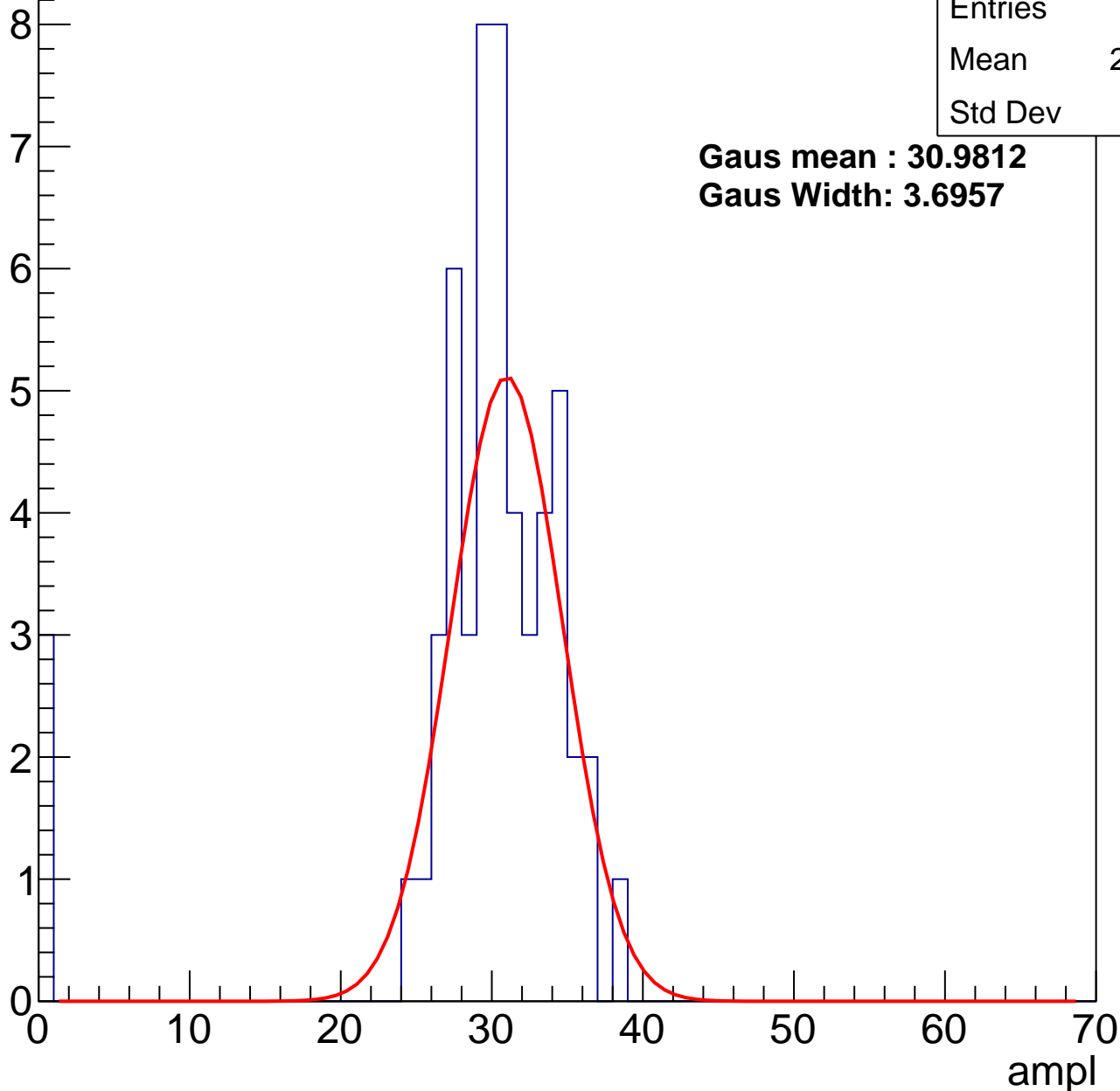
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	28.65
Std Dev	7.58

**Gaus mean : 30.9812**

**Gaus Width: 3.6957**



# B0L001S, U5-ch7, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	77
Mean	36.06
Std Dev	5.669

**Gaus mean : 36.6999**

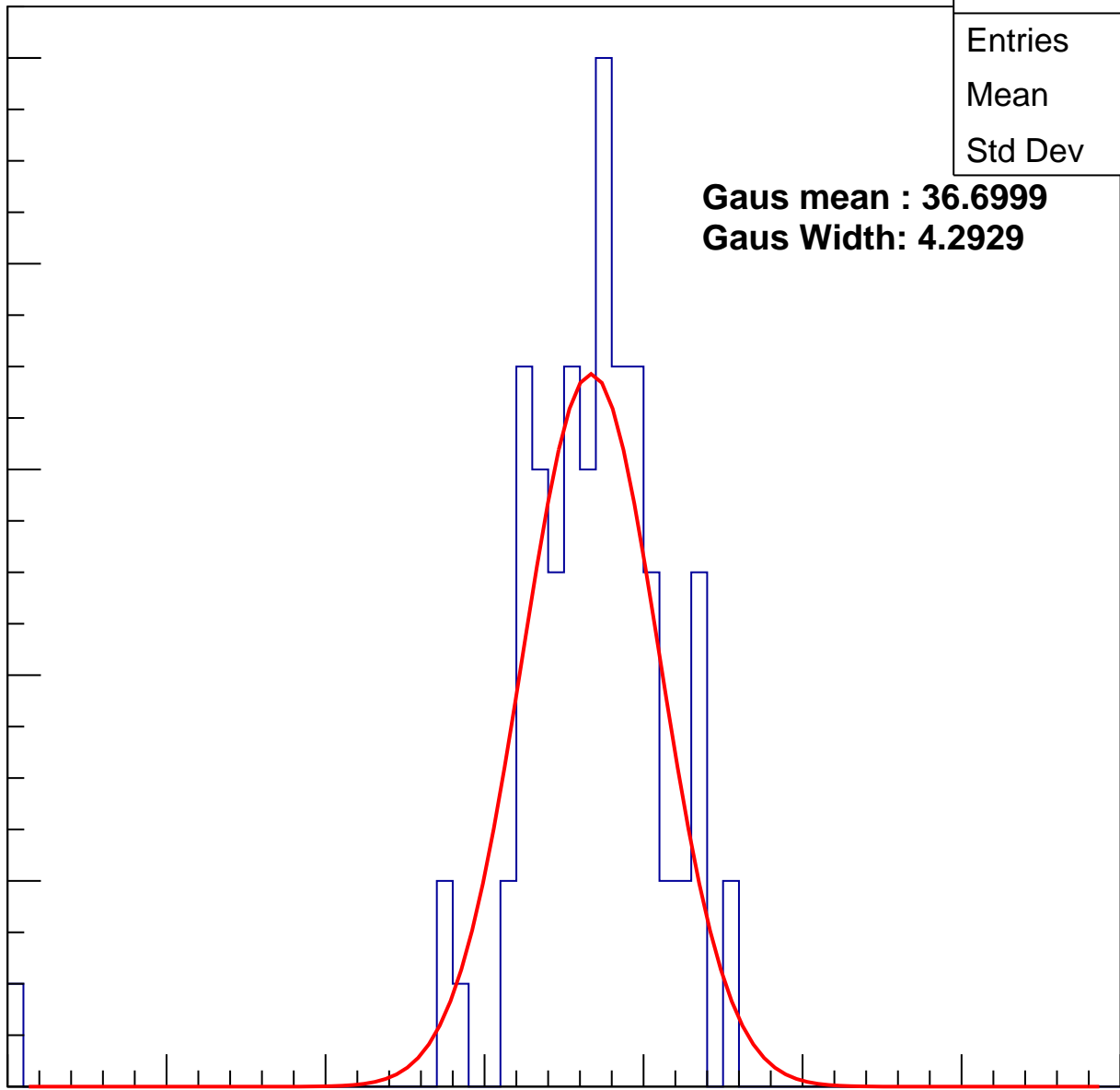
**Gaus Width: 4.2929**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U5-ch7, adc2

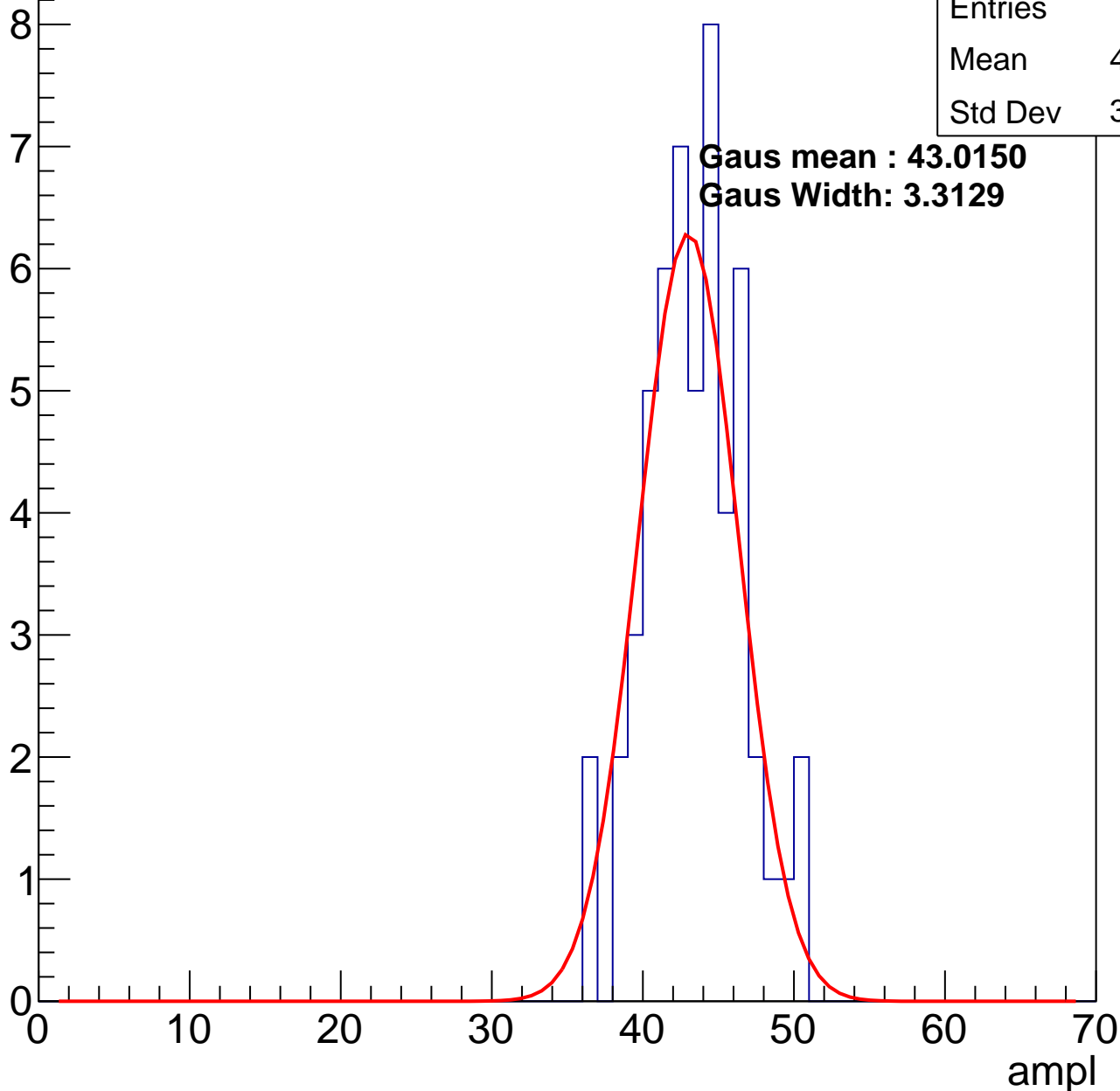
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	42.94
Std Dev	3.165

**Gaus mean : 43.0150**

**Gaus Width: 3.3129**

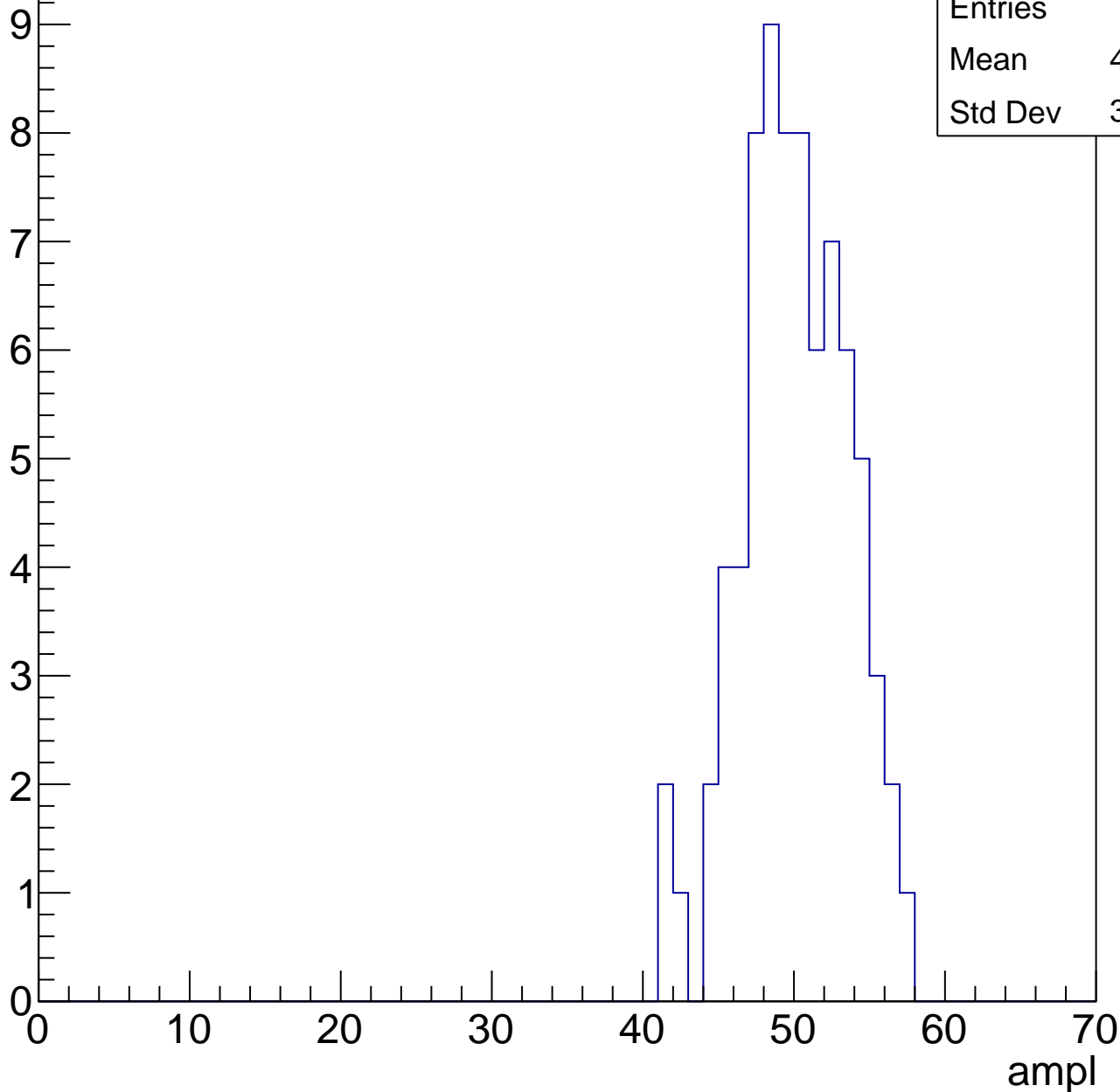


# B0L001S, U5-ch7, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	76
Mean	49.58
Std Dev	3.495

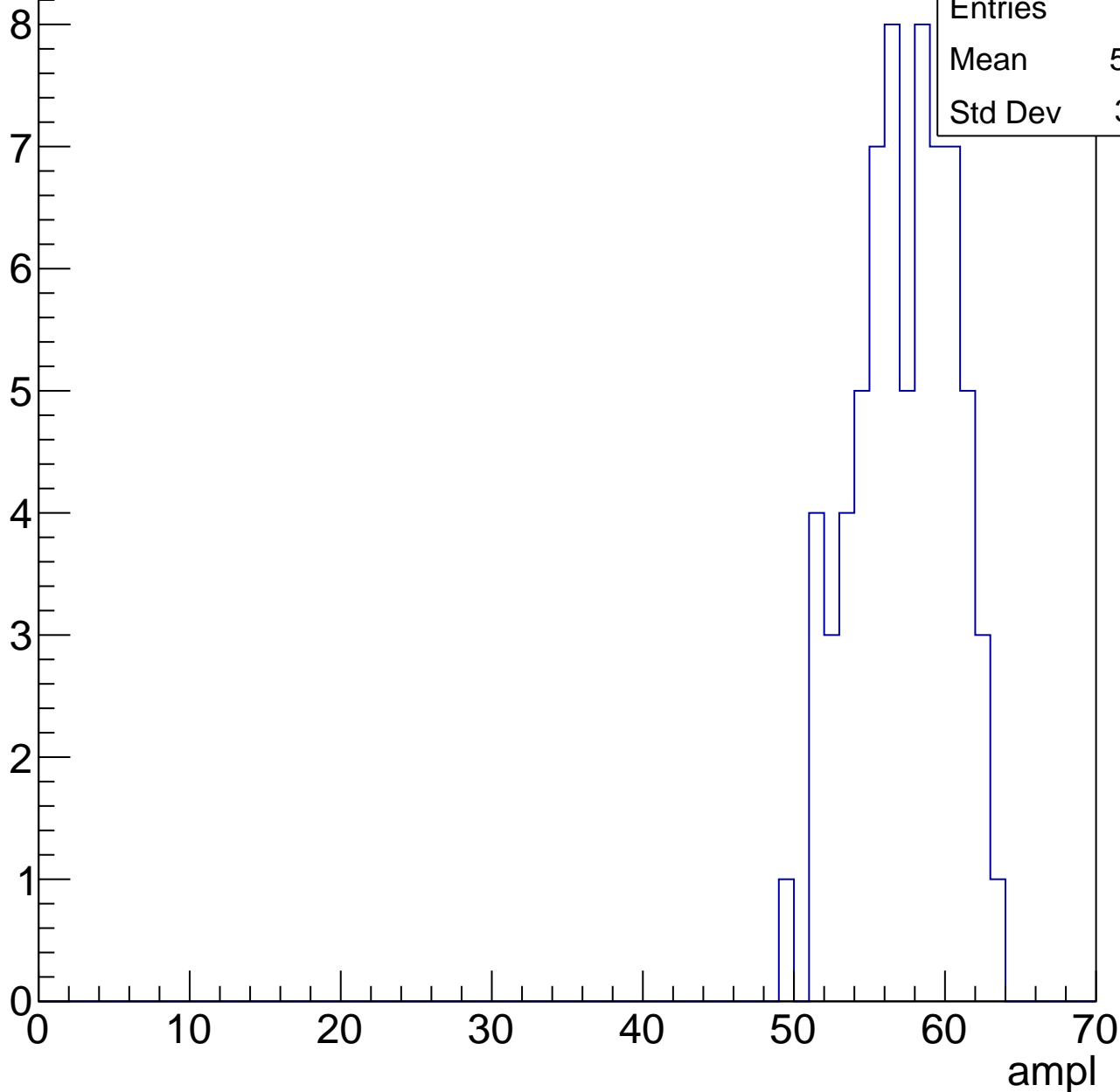


# B0L001S, U5-ch7, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	56.76
Std Dev	3.241

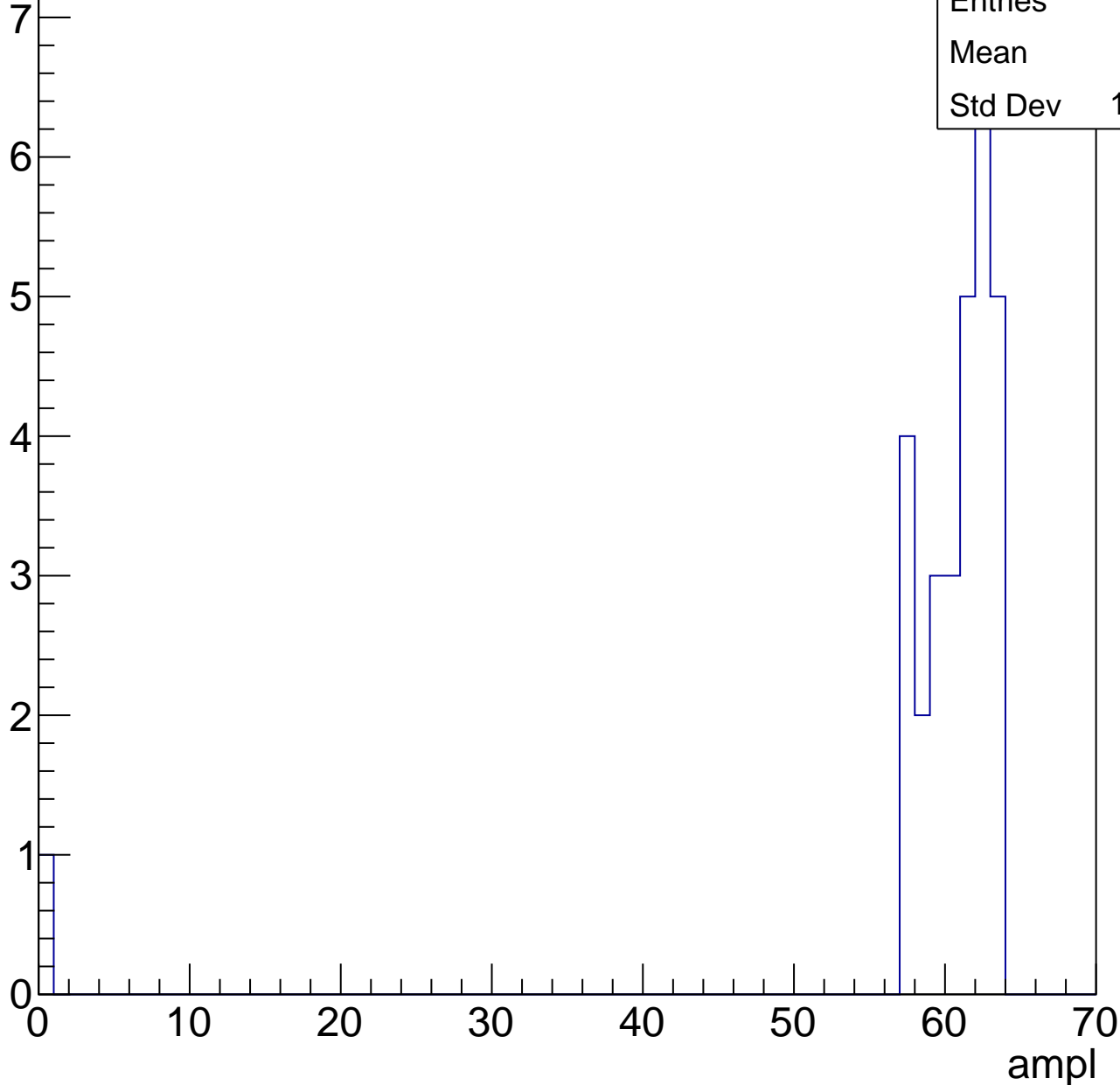


# B0L001S, U5-ch7, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

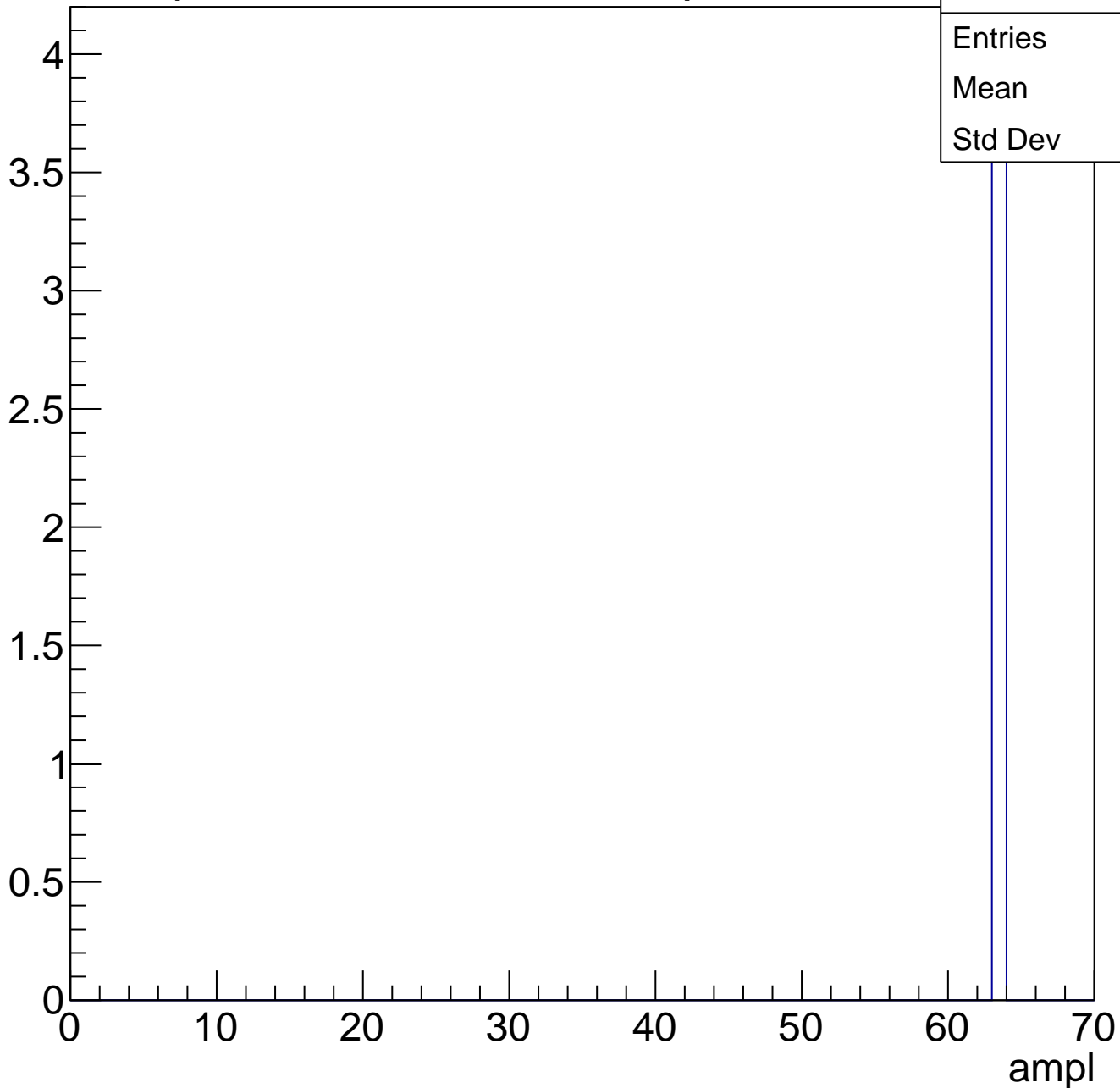
Entries	30
Mean	58.5
Std Dev	11.04



# B0L001S, U5-ch7, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch7, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	22
Std Dev	0

ampl

# B0L001S, U5-ch8, adc0

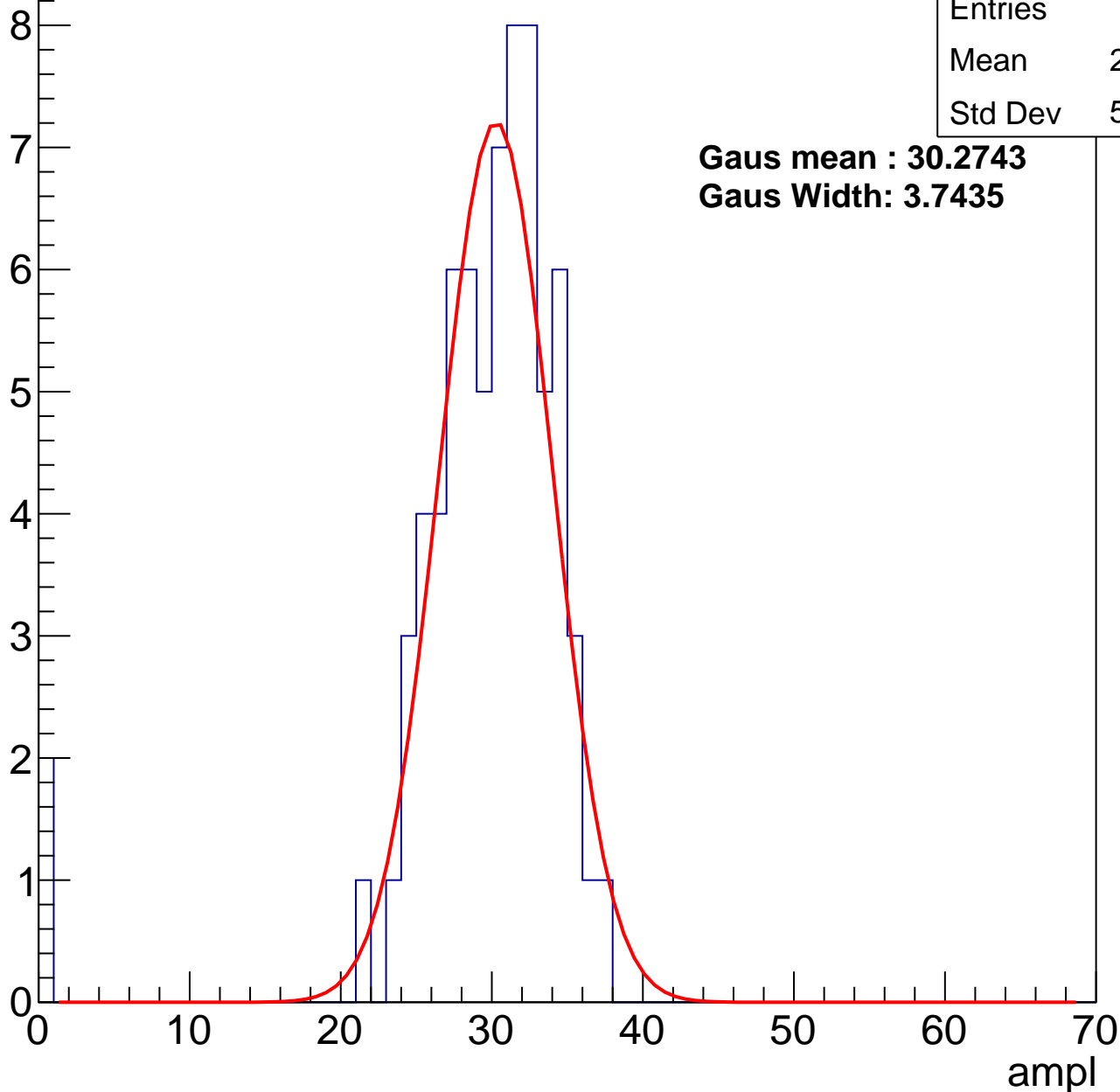
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	28.96
Std Dev	5.992

**Gaus mean : 30.2743**

**Gaus Width: 3.7435**



# B0L001S, U5-ch8, adc1

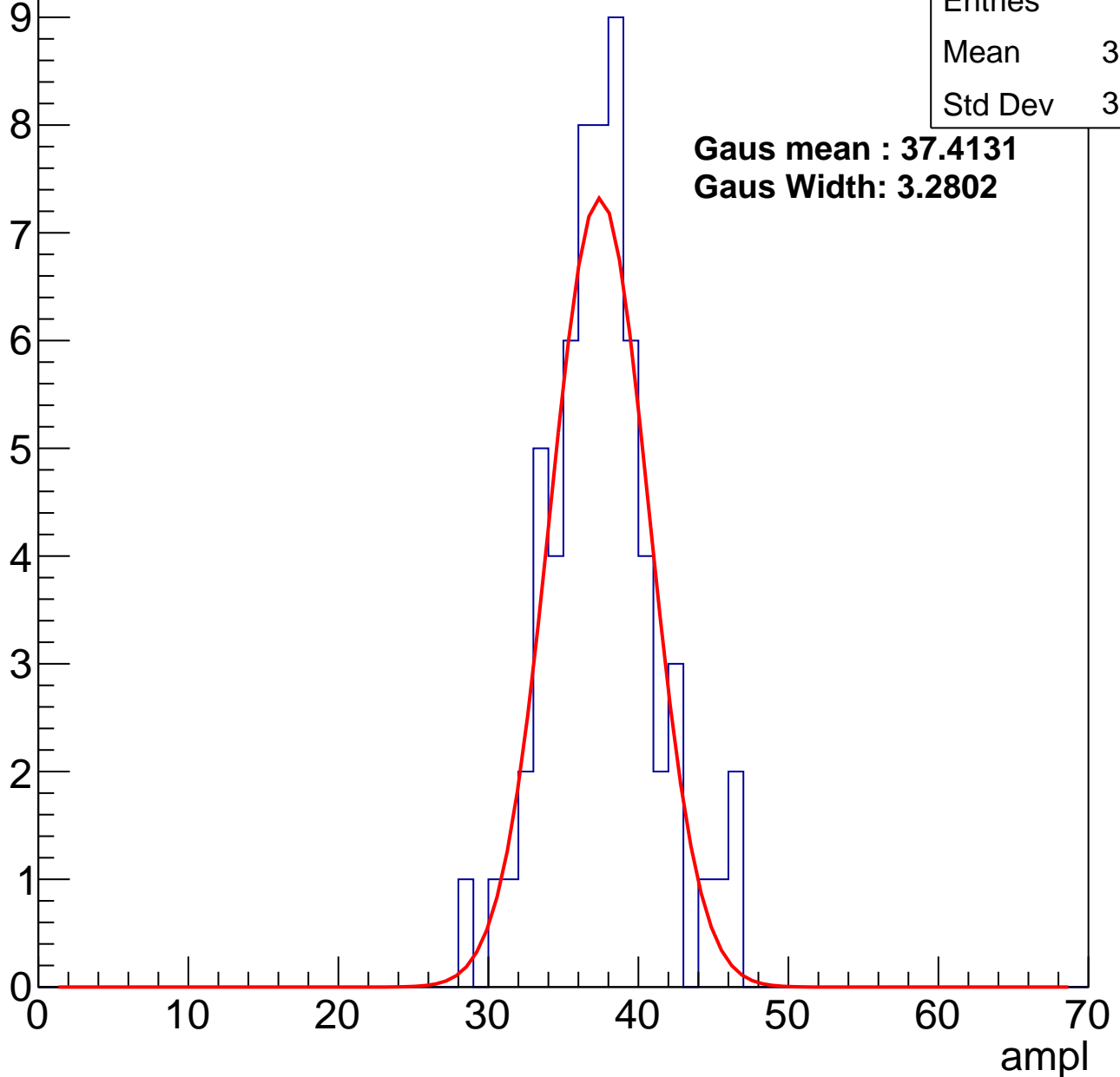
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	37.08
Std Dev	3.568

**Gaus mean : 37.4131**

**Gaus Width: 3.2802**



# B0L001S, U5-ch8, adc2

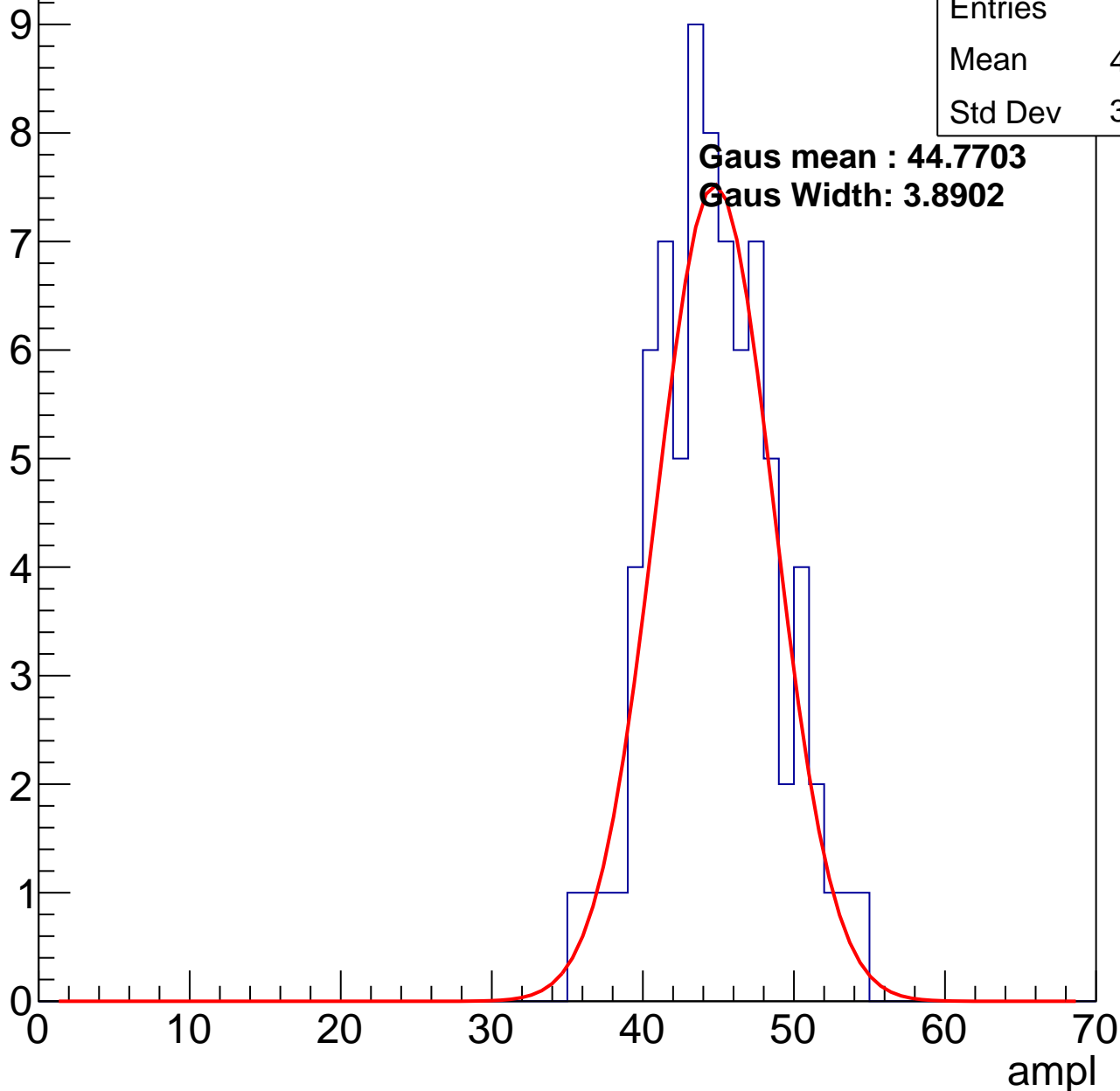
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	79
Mean	44.27
Std Dev	3.935

**Gaus mean : 44.7703**

**Gaus Width: 3.8902**

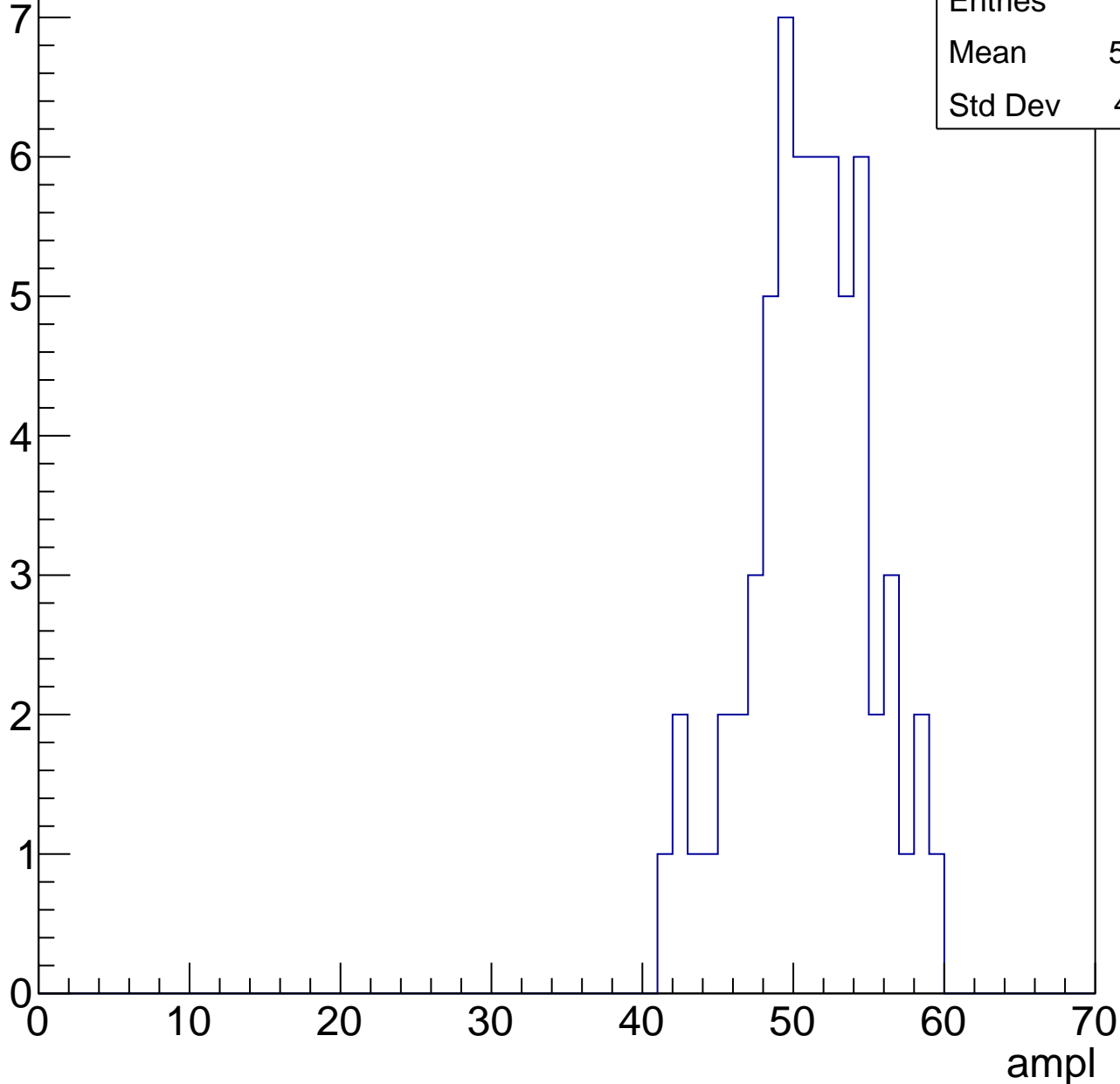


# B0L001S, U5-ch8, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

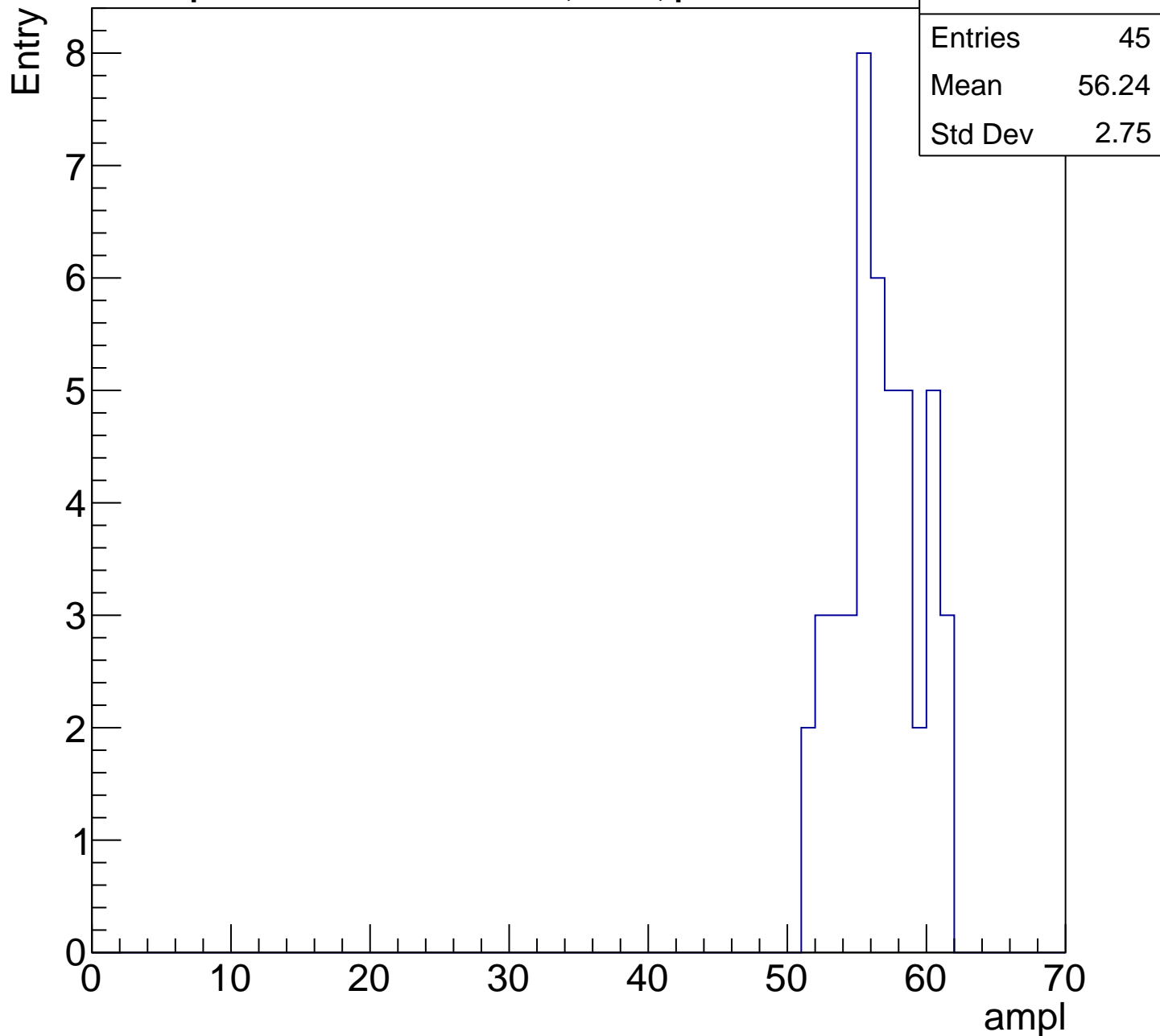
Entry

Entries	62
Mean	50.56
Std Dev	4.011



# B0L001S, U5-ch8, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U5-ch8, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	44
Mean	60.09
Std Dev	2.835

Entry

10

8

6

4

2

0

0

10

20

30

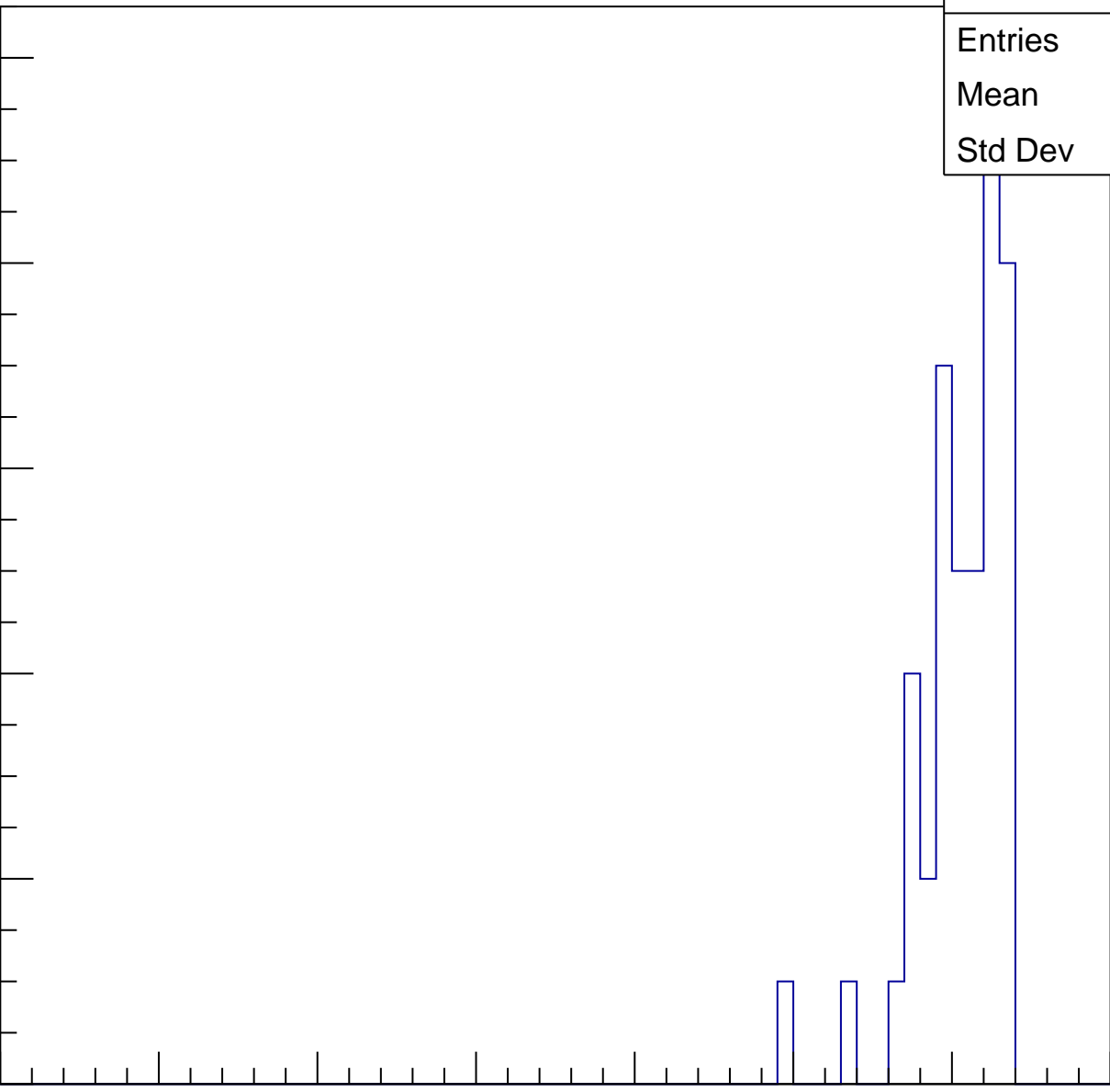
40

50

60

ampl

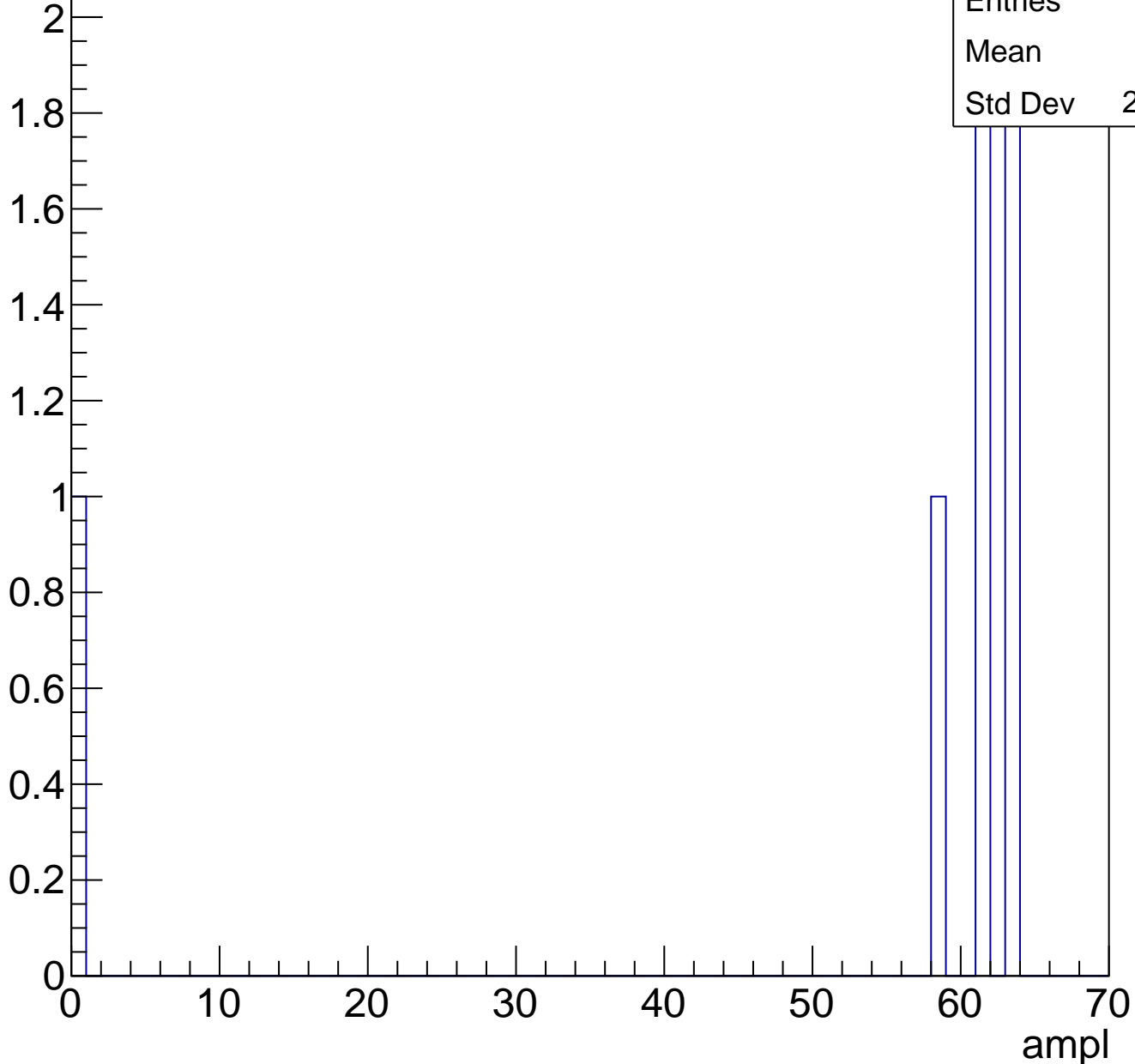
70



# B0L001S, U5-ch8, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch8, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U5-ch9, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	75
Mean	30.05
Std Dev	3.874

**Gaus mean : 30.2675**

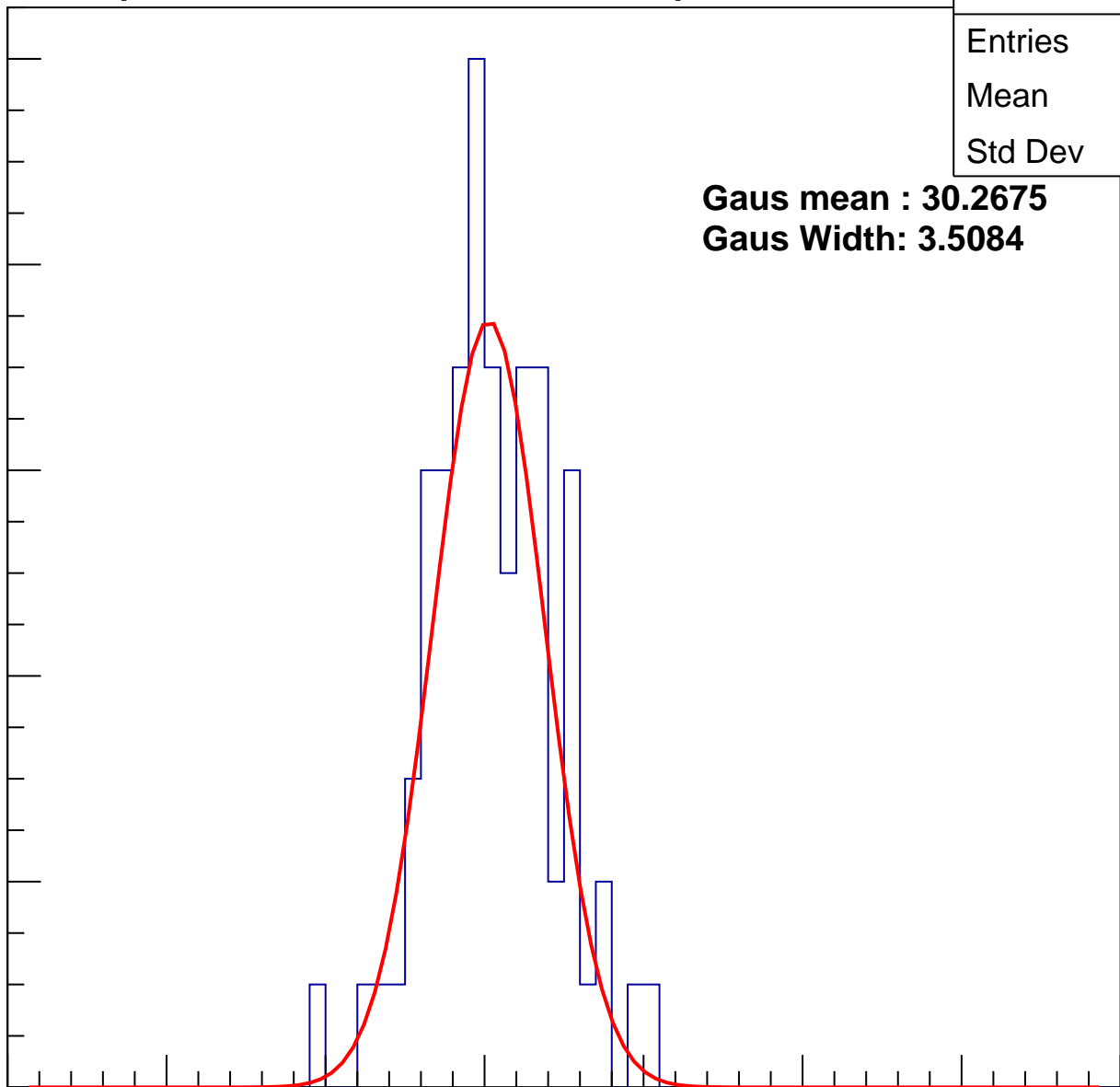
**Gaus Width: 3.5084**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U5-ch9, adc1

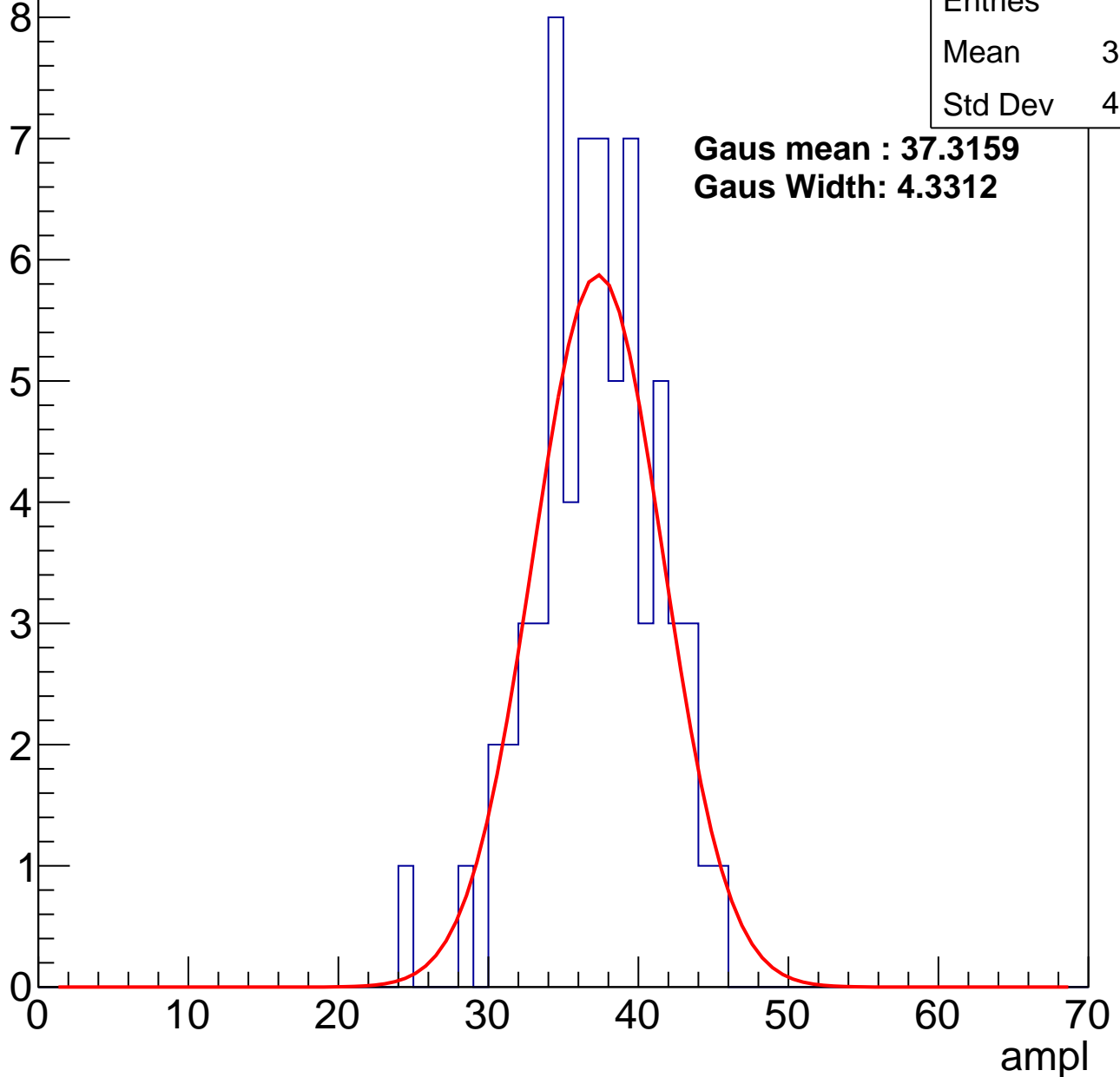
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	36.73
Std Dev	4.025

**Gaus mean : 37.3159**

**Gaus Width: 4.3312**



# B0L001S, U5-ch9, adc2

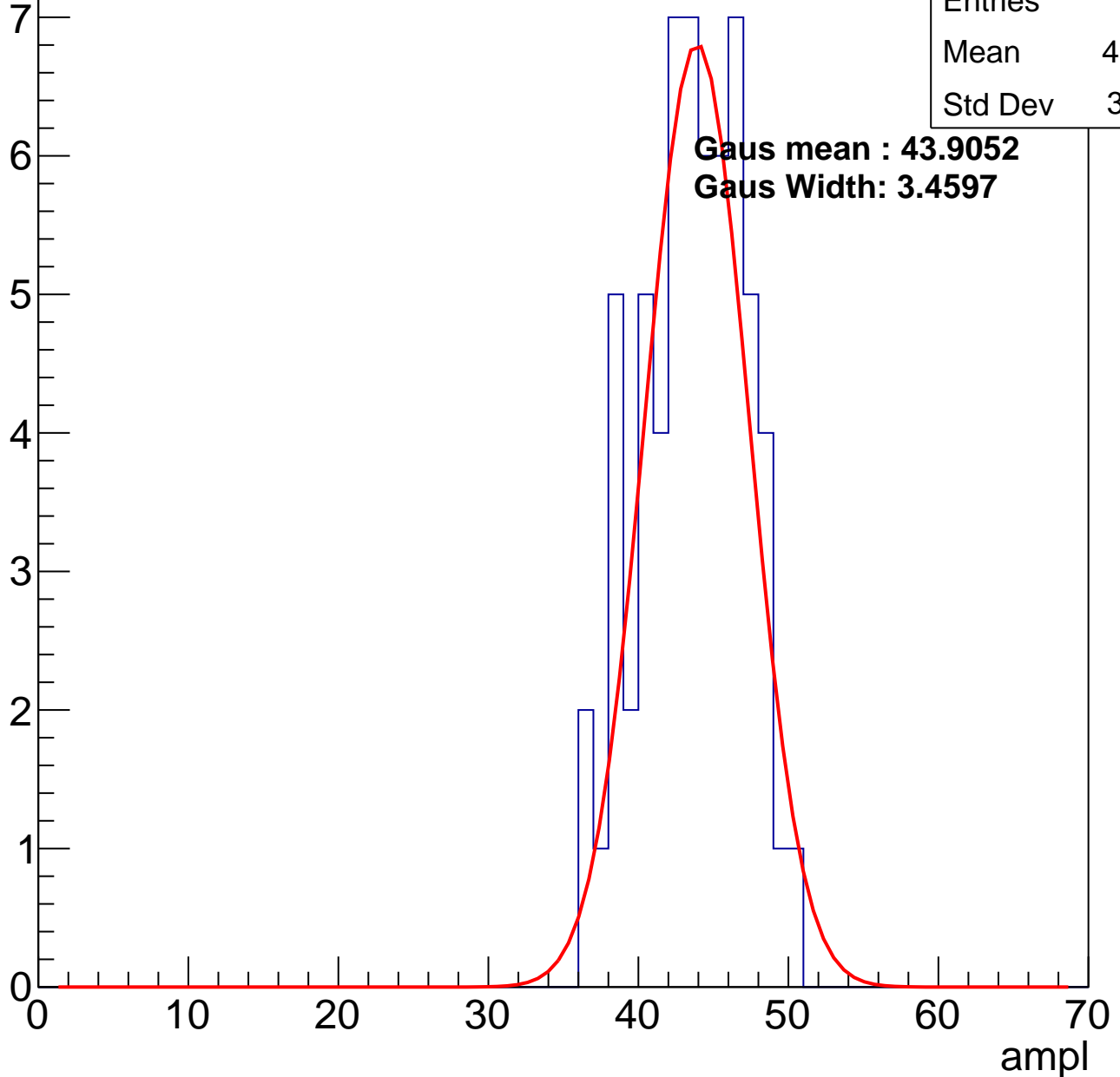
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	43.14
Std Dev	3.371

**Gaus mean : 43.9052**

**Gaus Width: 3.4597**

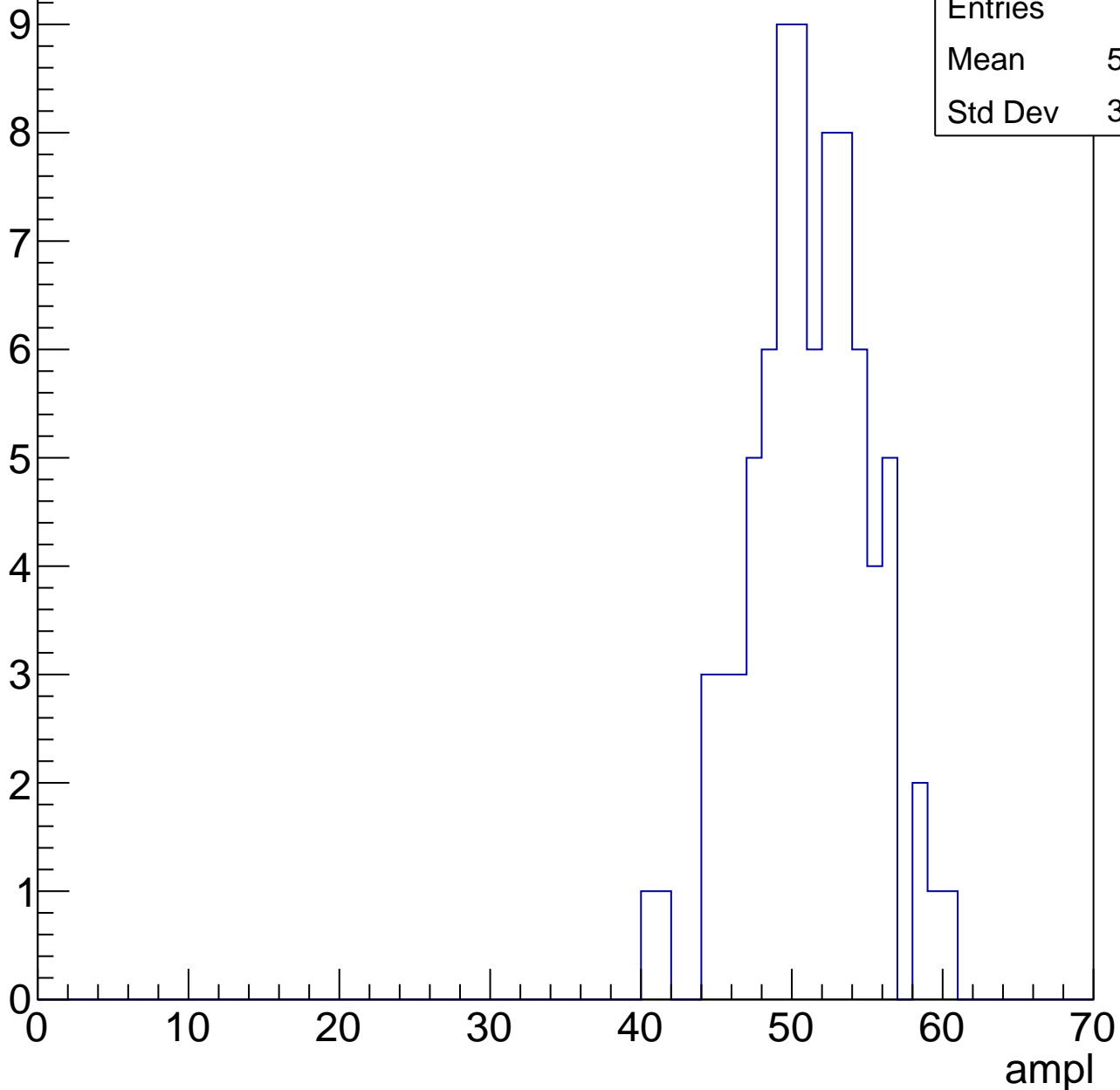


# B0L001S, U5-ch9, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	81
Mean	50.68
Std Dev	3.925

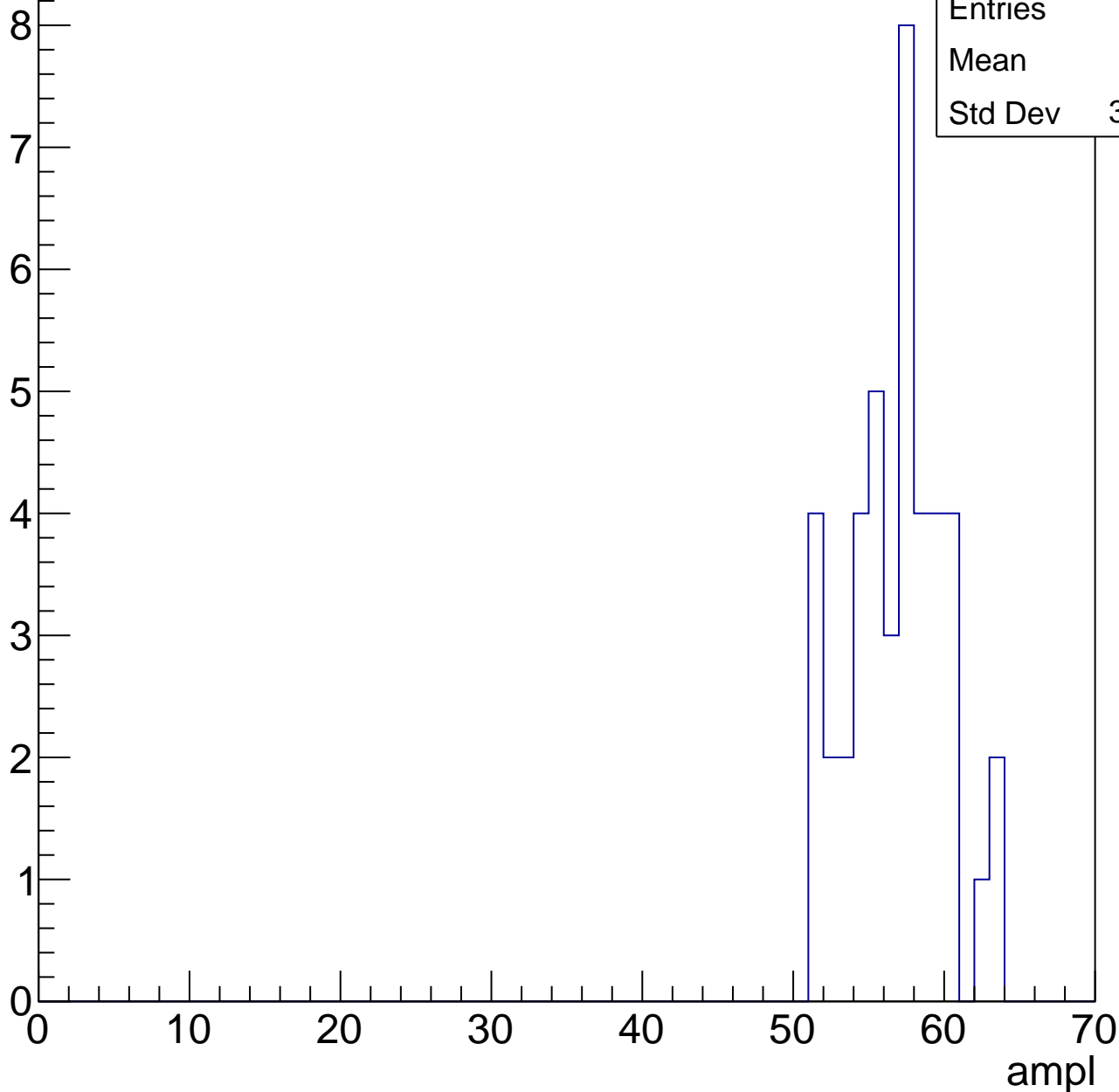


# B0L001S, U5-ch9, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	43
Mean	56.4
Std Dev	3.134



# B0L001S, U5-ch9, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

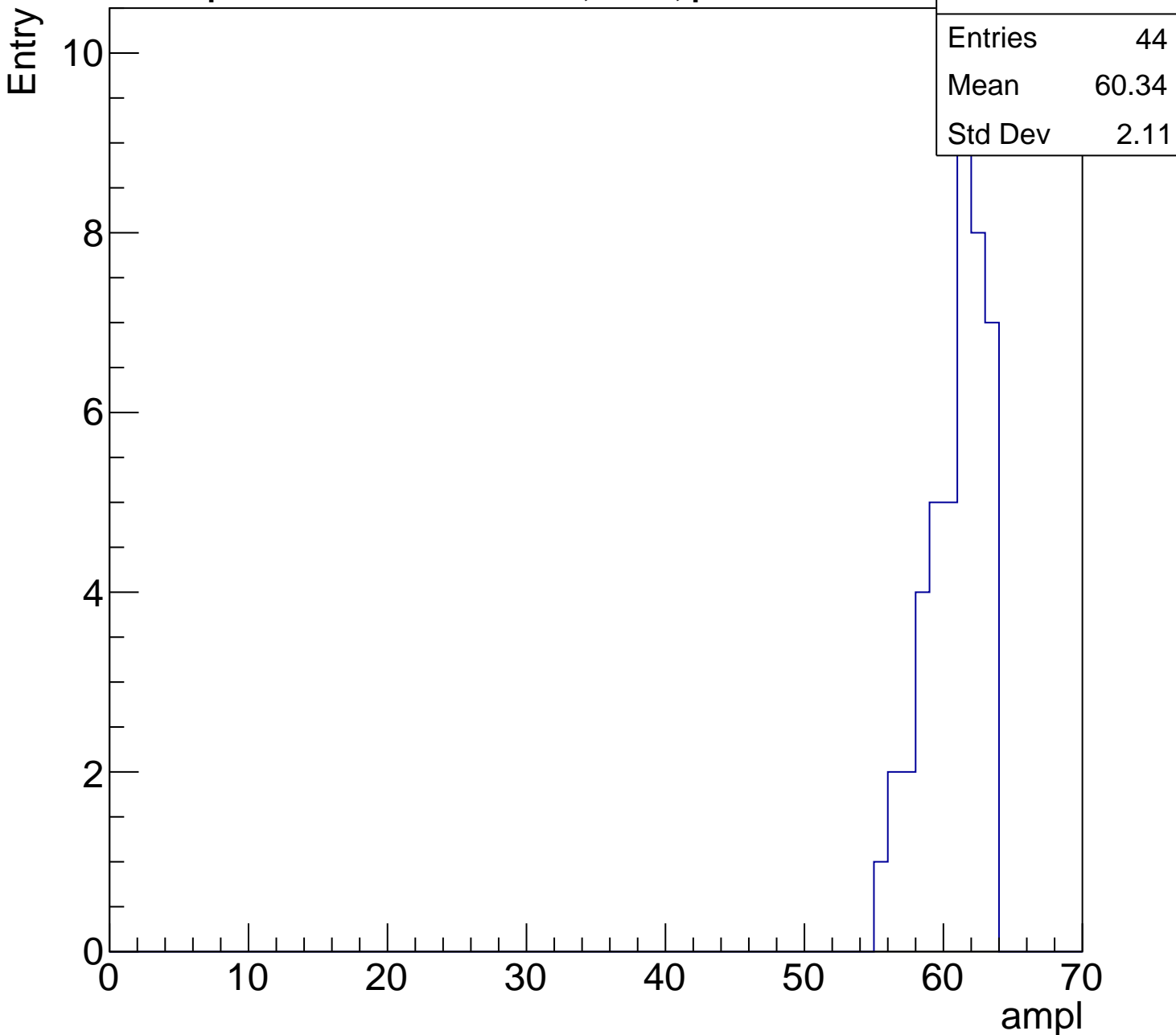
Entries	44
Mean	60.34
Std Dev	2.11

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

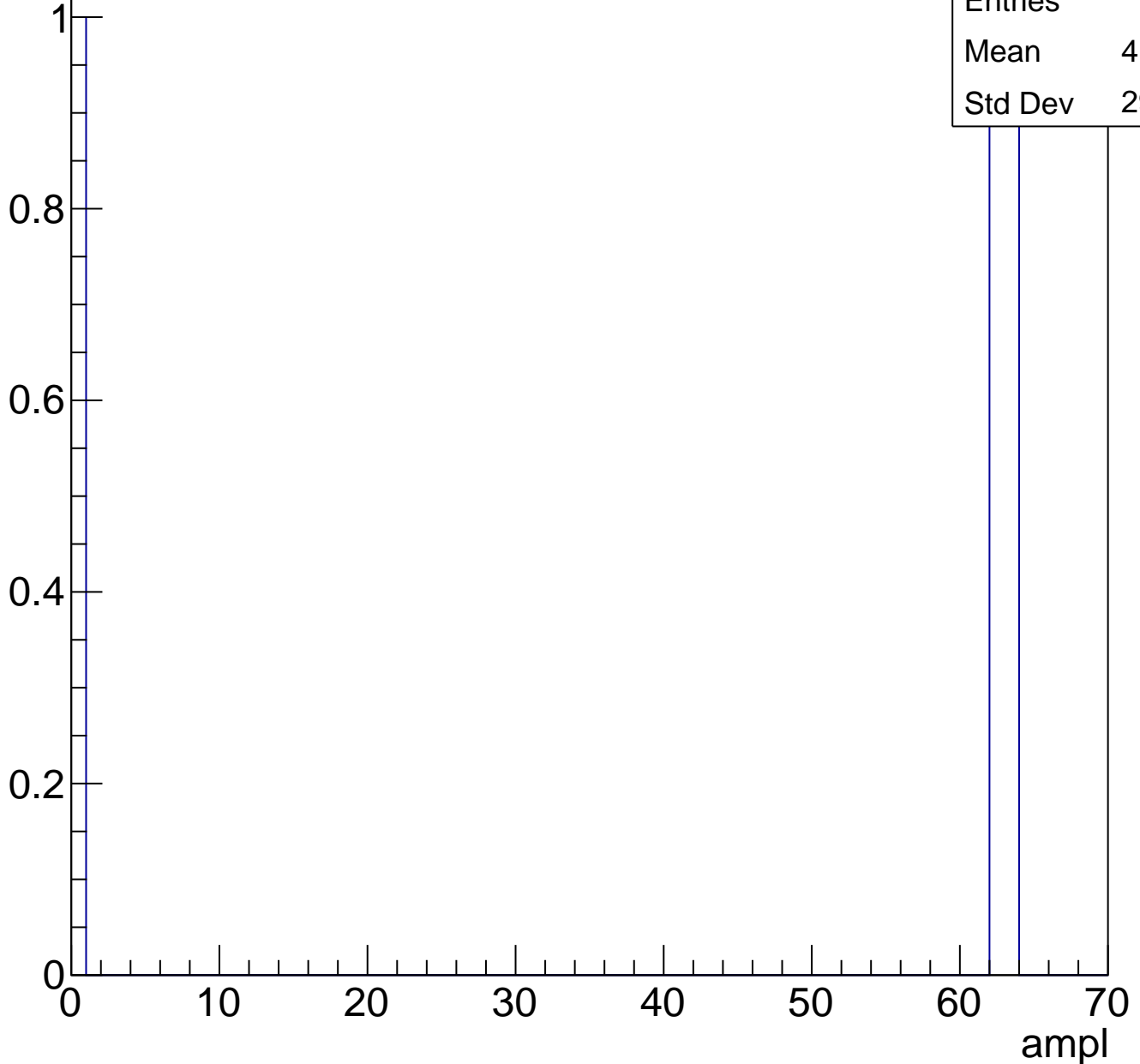
ampl



# B0L001S, U5-ch9, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

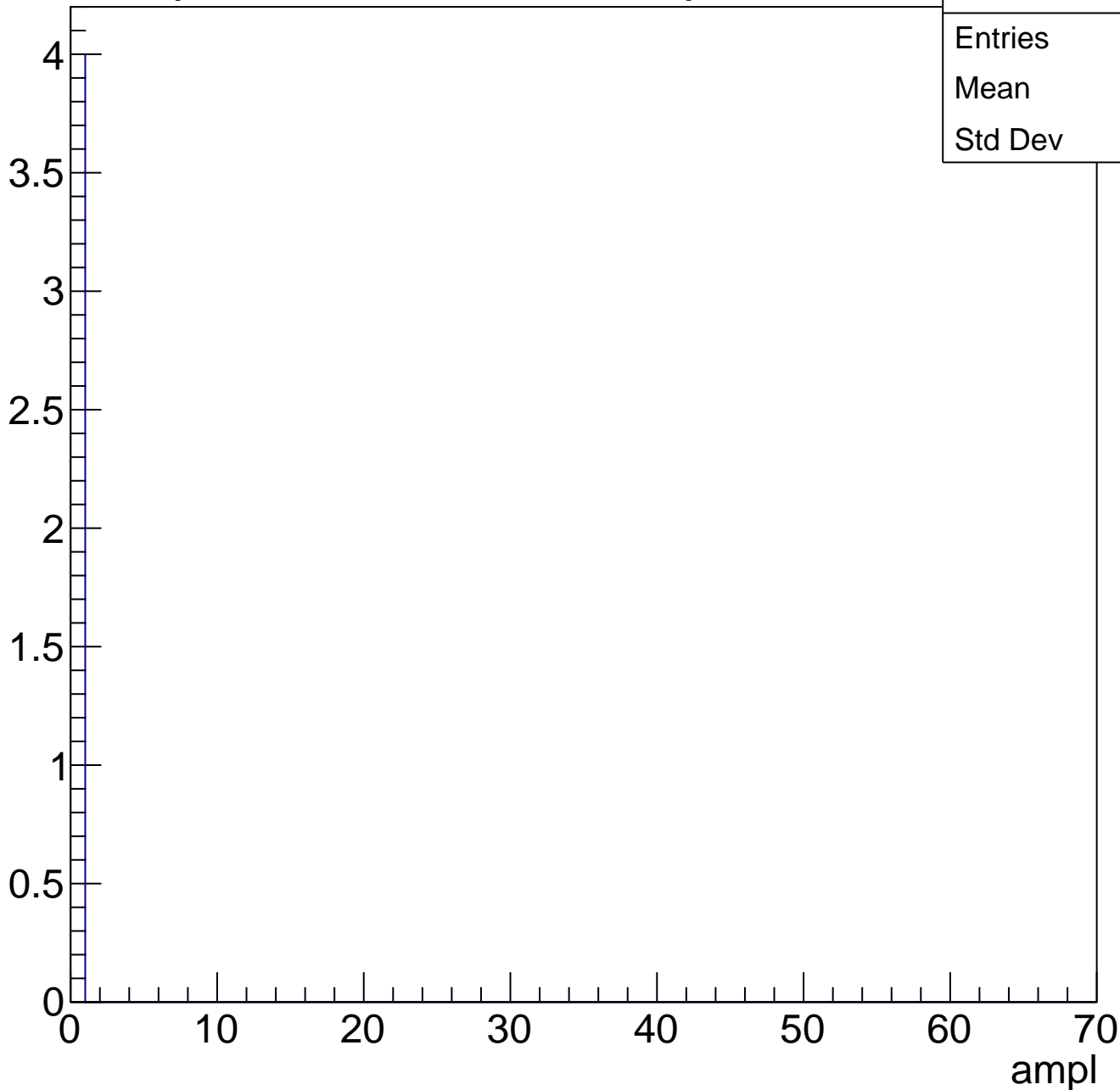




# B0L001S, U5-ch9, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	4
Mean	0
Std Dev	0

# B0L001S, U5-ch10, adc0

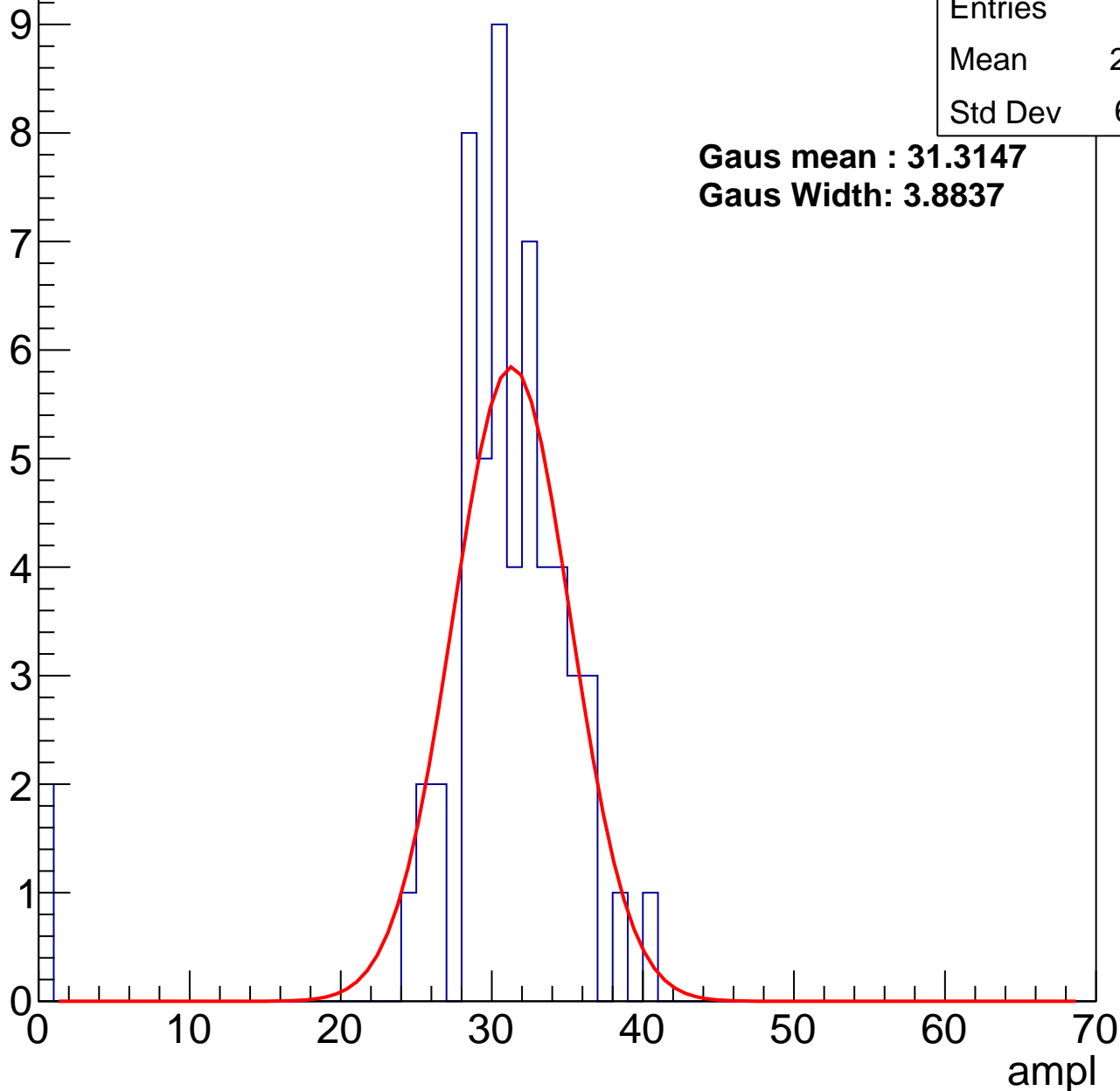
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	29.86
Std Dev	6.591

**Gaus mean : 31.3147**

**Gaus Width: 3.8837**



# B0L001S, U5-ch10, adc1

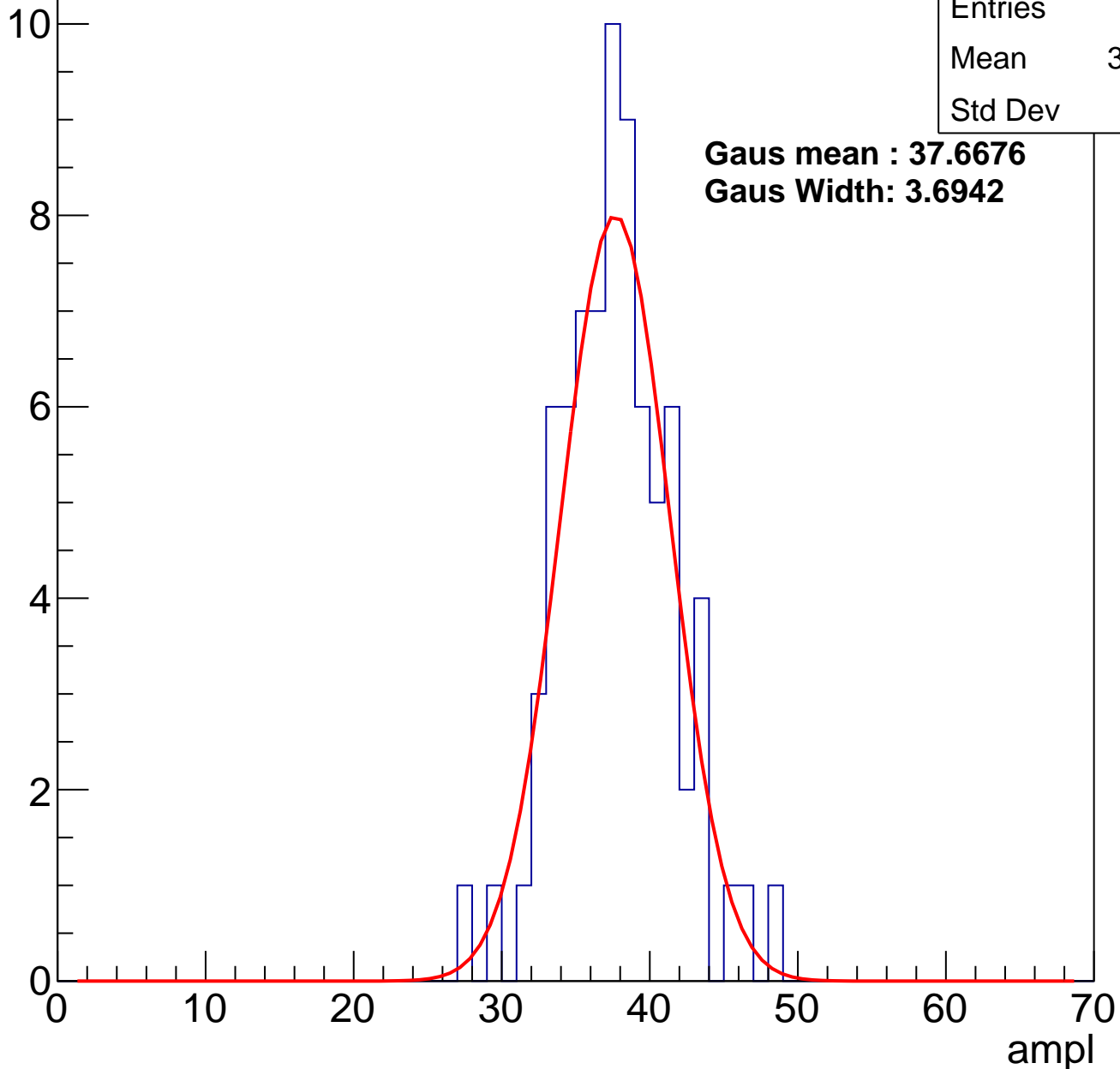
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	77
Mean	37.26
Std Dev	3.76

**Gaus mean : 37.6676**

**Gaus Width: 3.6942**

Entry



# B0L001S, U5-ch10, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

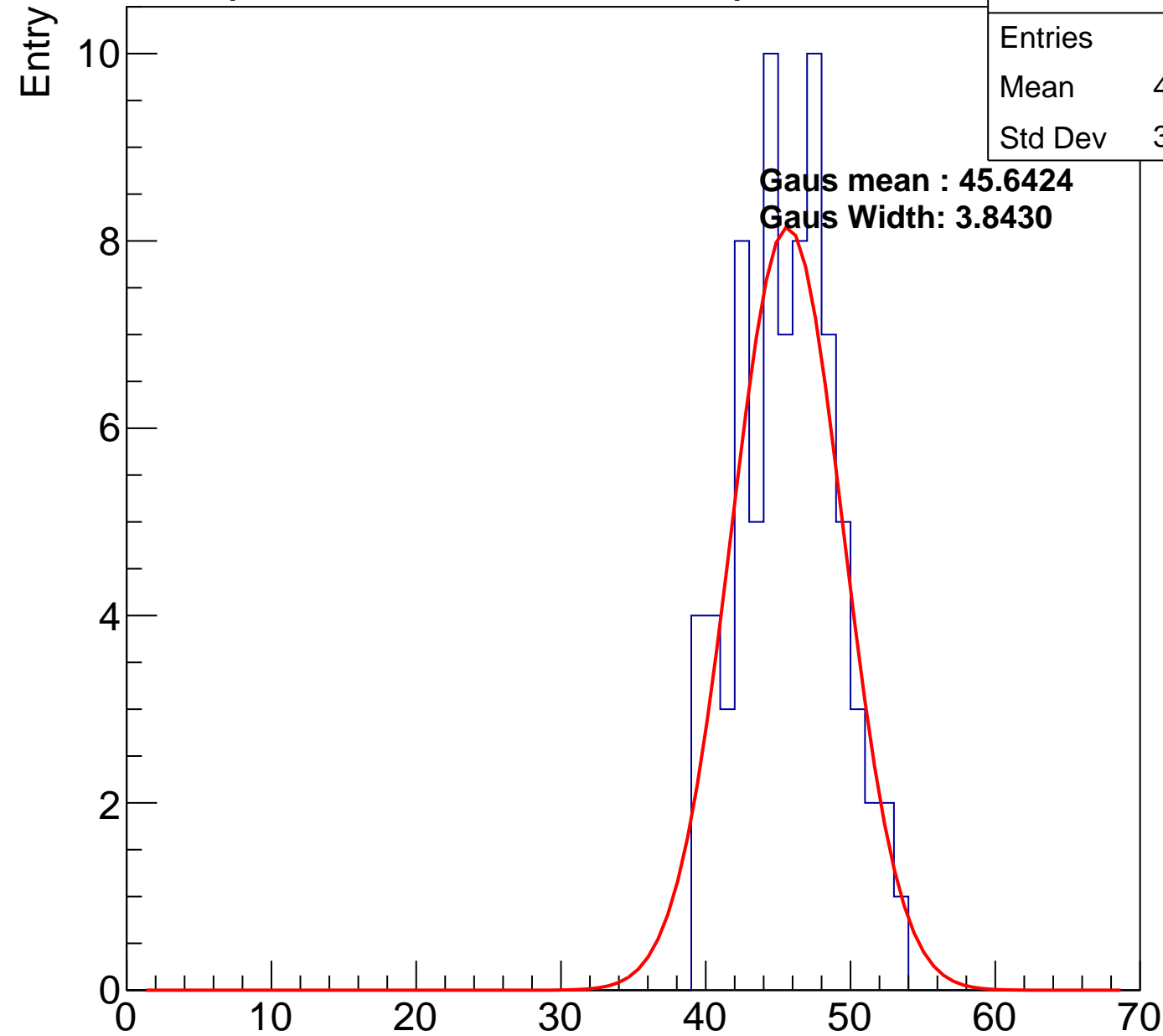
Entries	79
Mean	45.23
Std Dev	3.356

**Gaus mean : 45.6424**

**Gaus Width: 3.8430**

10  
8  
6  
4  
2  
0

ampl

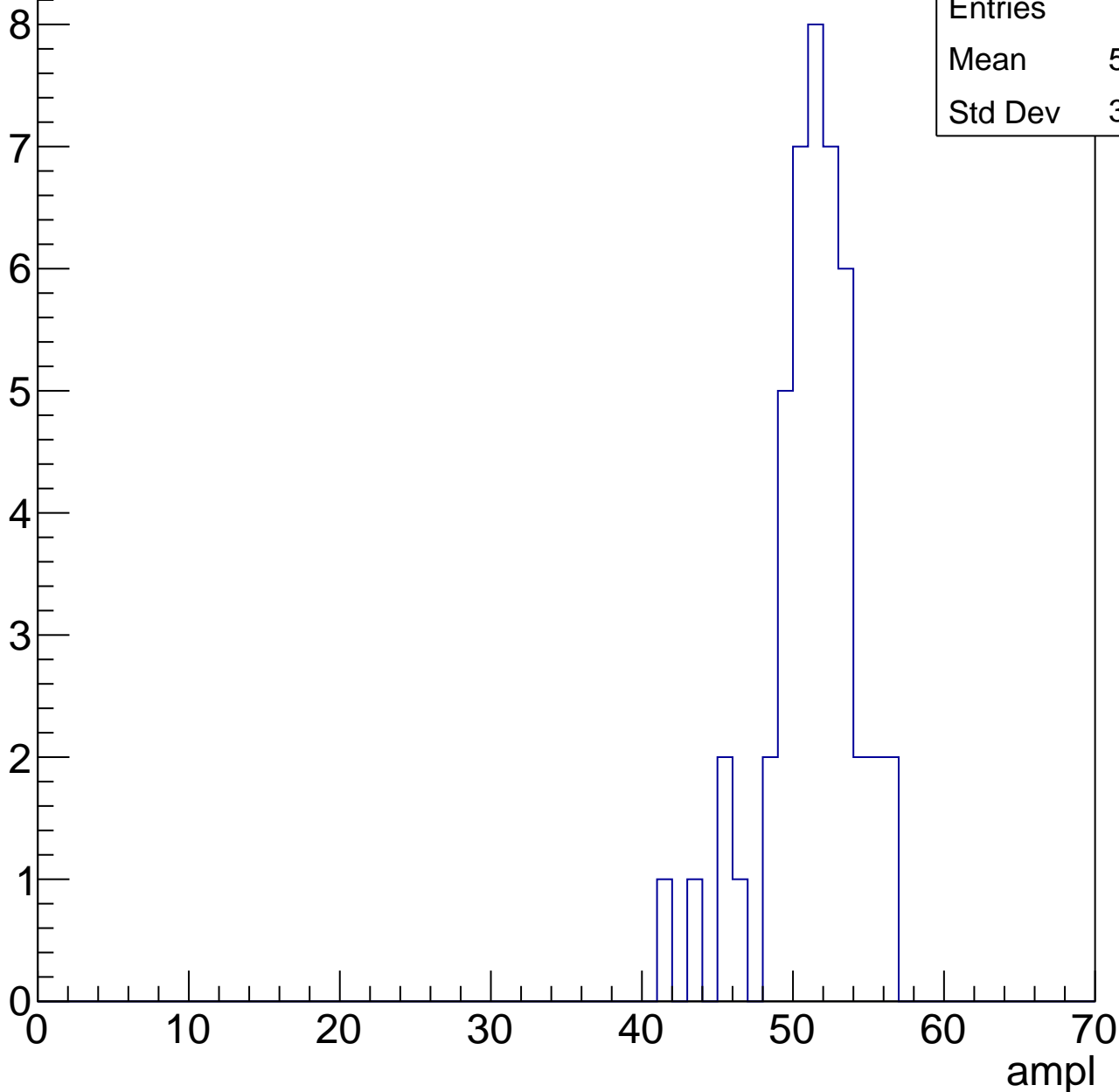


# B0L001S, U5-ch10, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	46
Mean	50.67
Std Dev	3.065

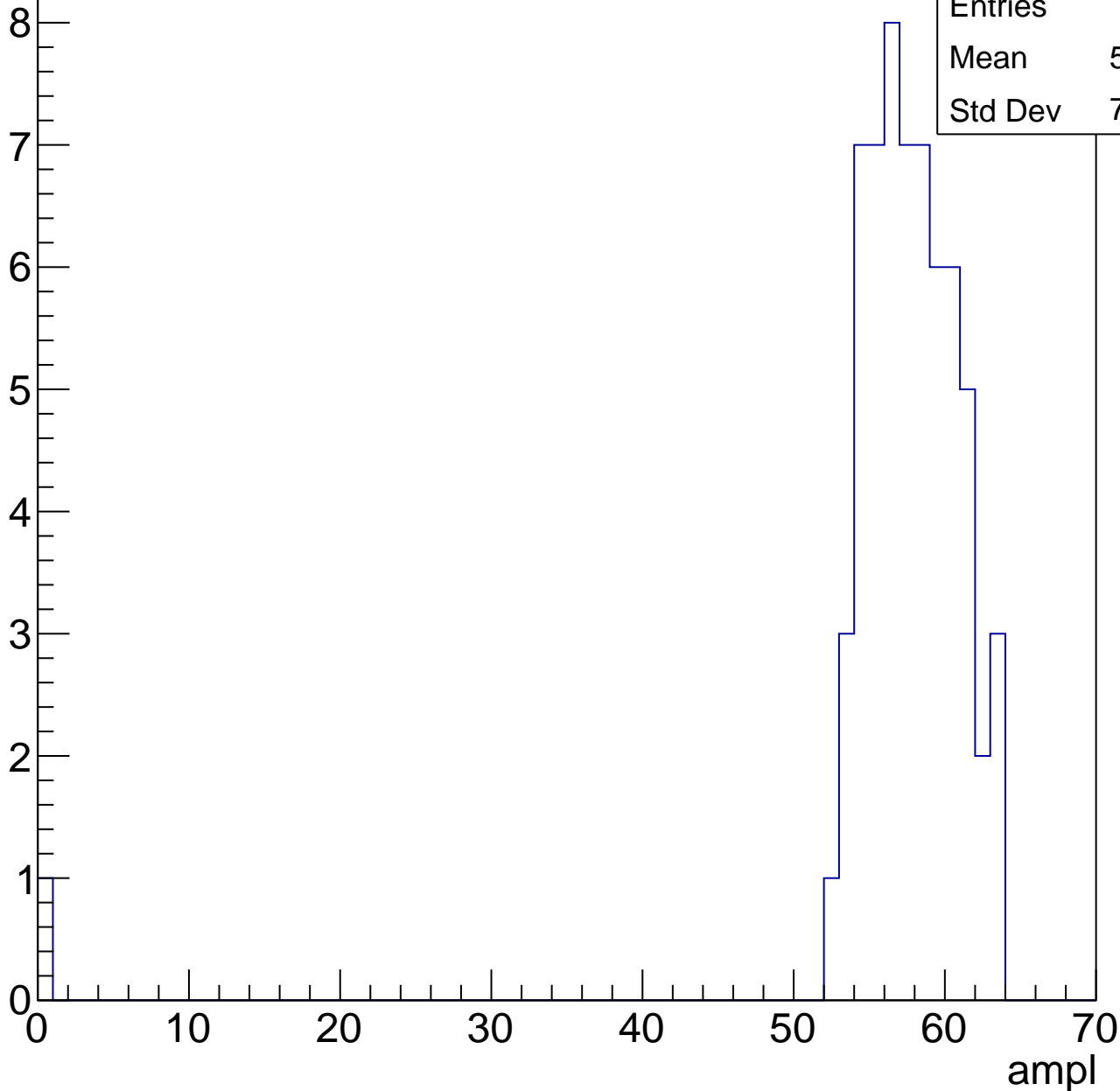


# B0L001S, U5-ch10, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	56.49
Std Dev	7.692

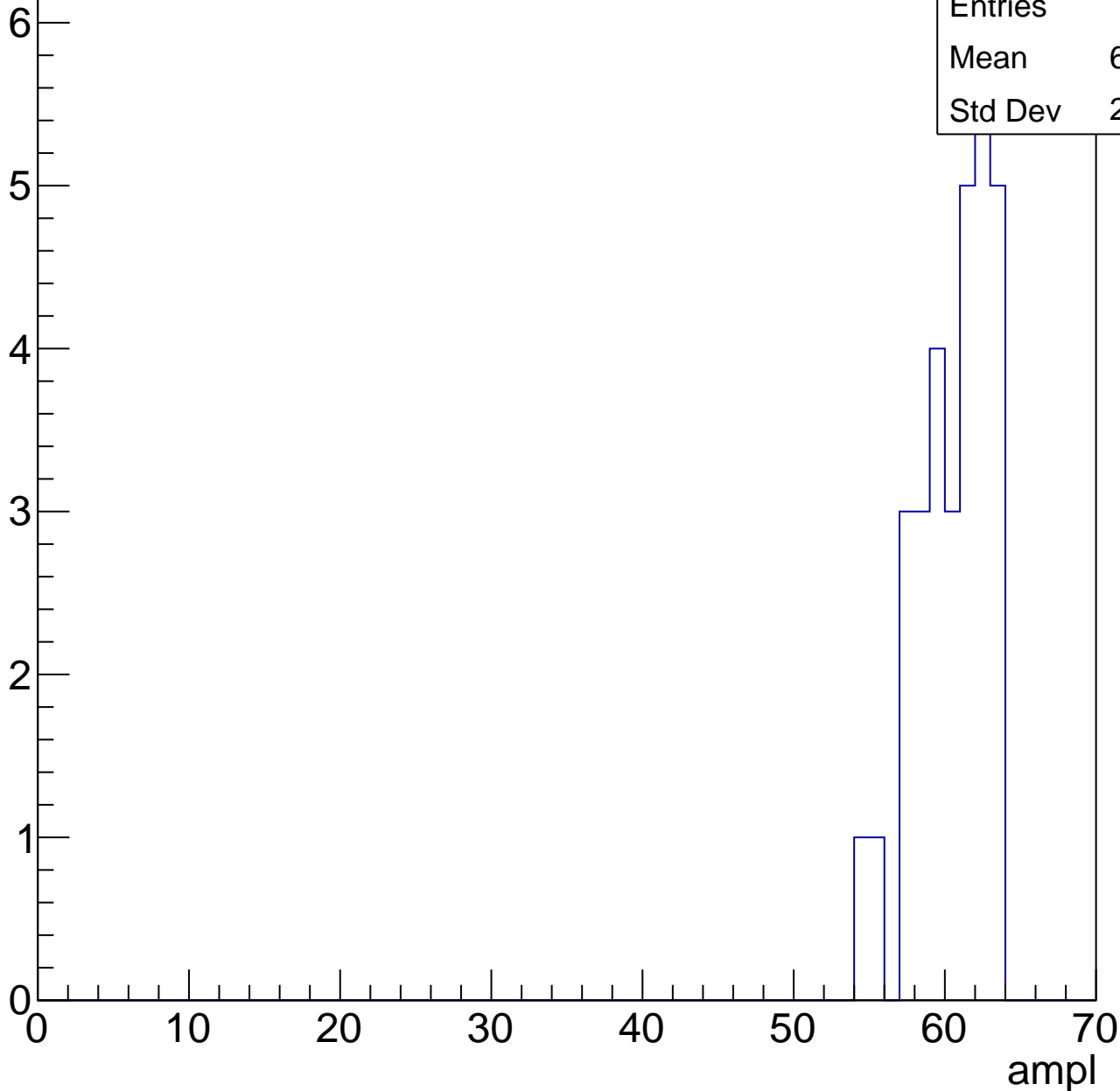


# B0L001S, U5-ch10, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	31
Mean	60.06
Std Dev	2.395



# B0L001S, U5-ch10, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch10, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L001S, U5-ch11, adc0

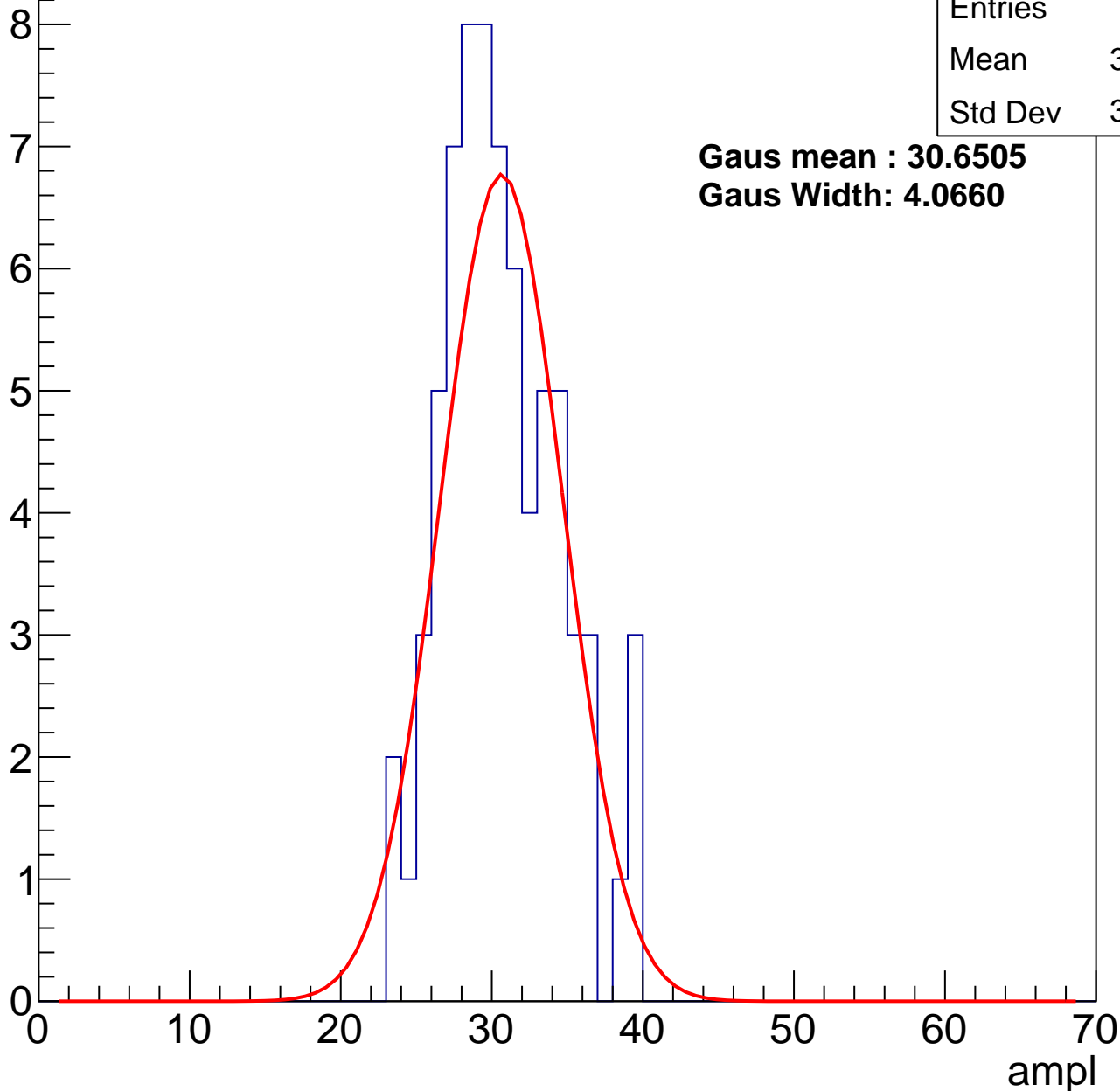
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	30.24
Std Dev	3.799

**Gaus mean : 30.6505**

**Gaus Width: 4.0660**



# B0L001S, U5-ch11, adc1

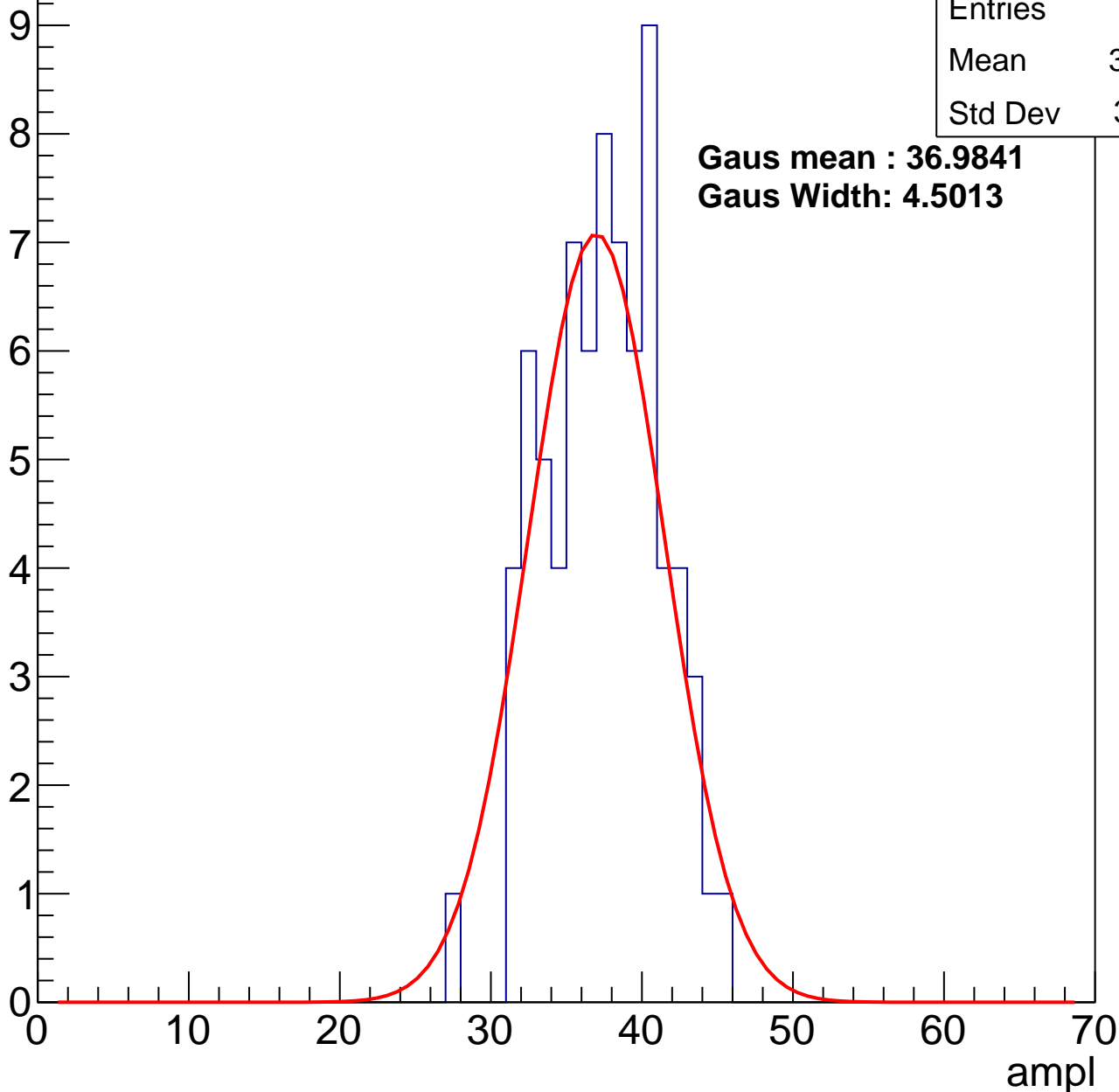
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	76
Mean	36.99
Std Dev	3.701

**Gaus mean : 36.9841**

**Gaus Width: 4.5013**

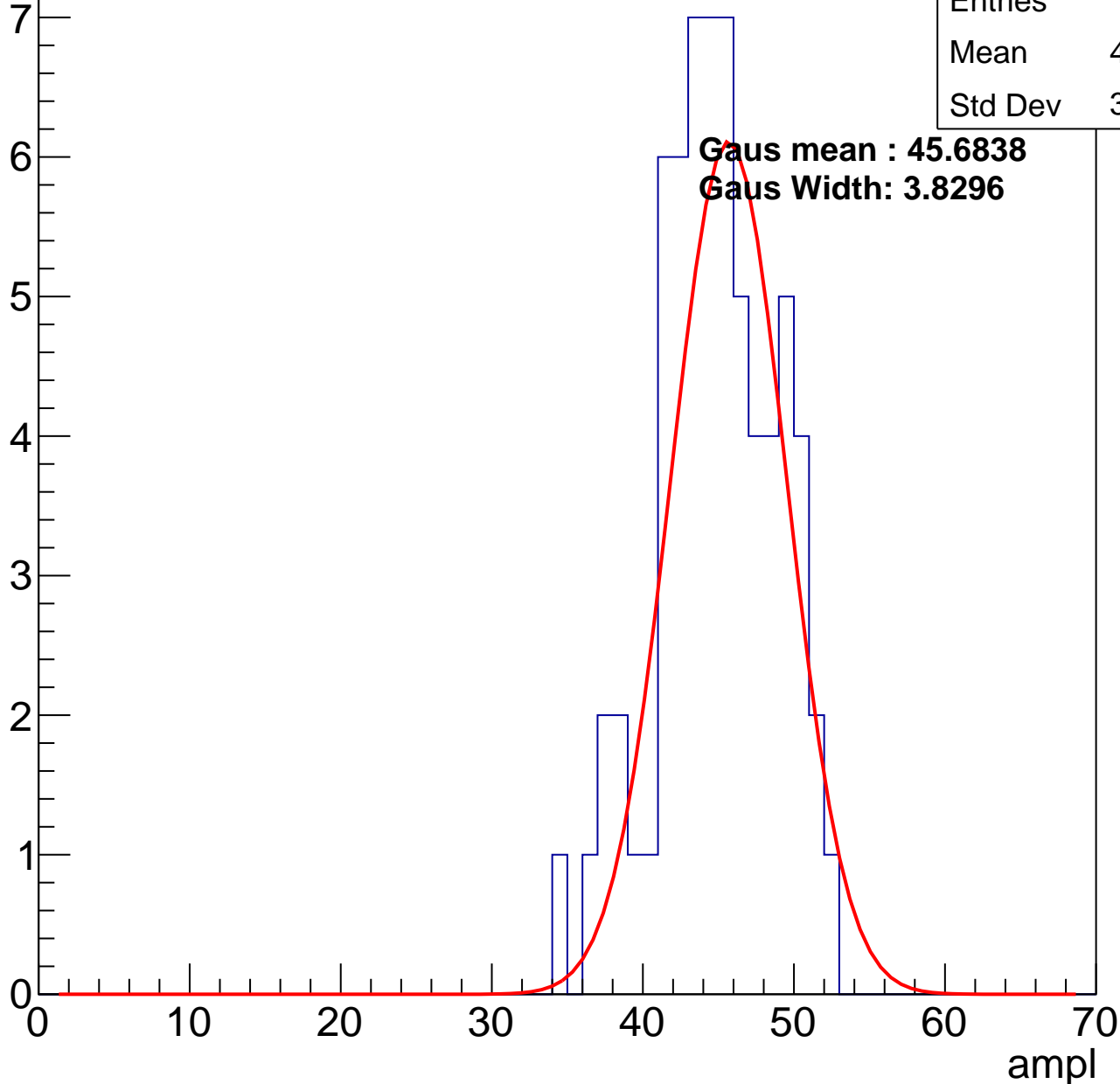


# B0L001S, U5-ch11, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	44.39
Std Dev	3.908

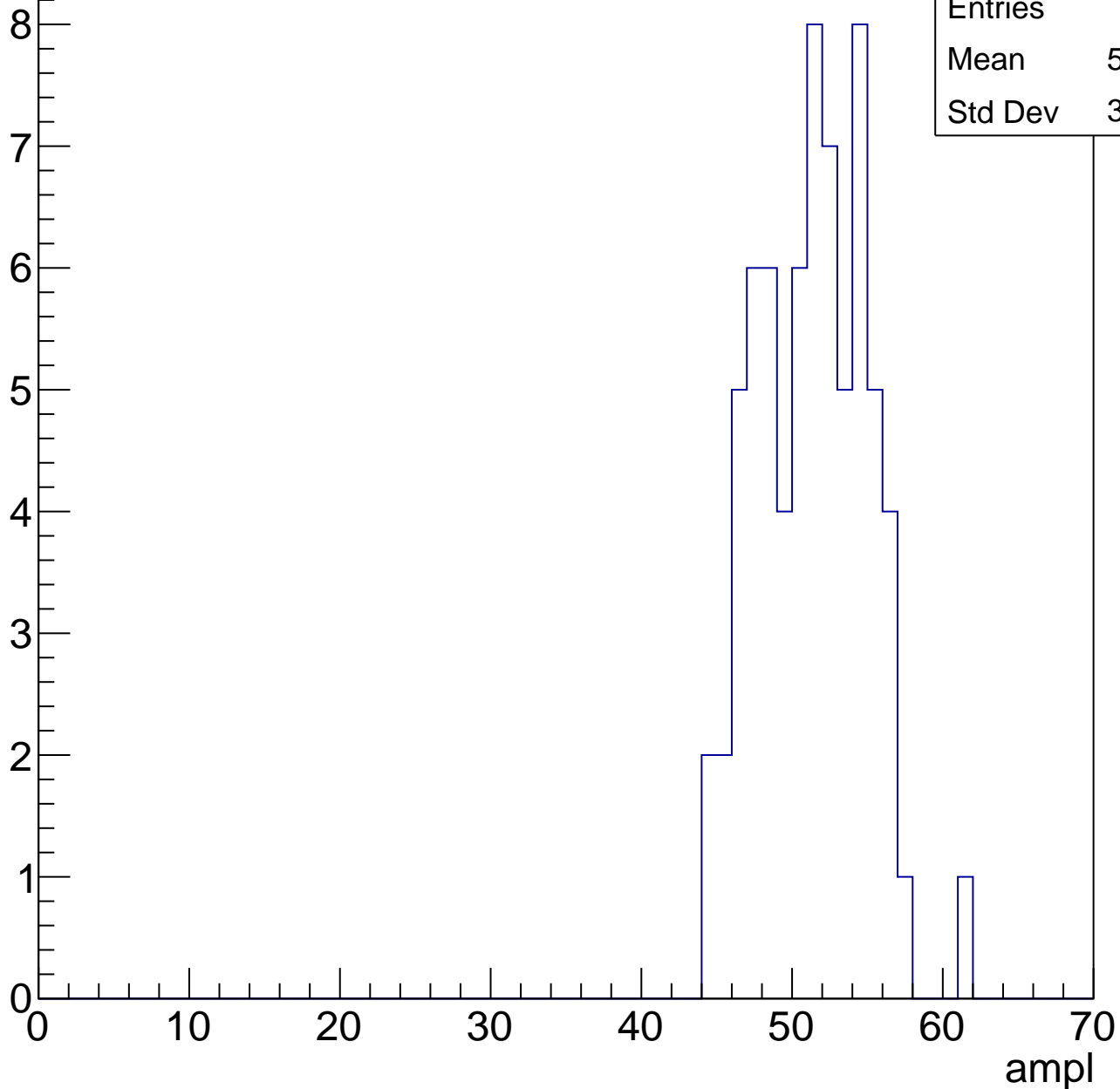


# B0L001S, U5-ch11, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	50.86
Std Dev	3.547



# B0L001S, U5-ch11, adc4

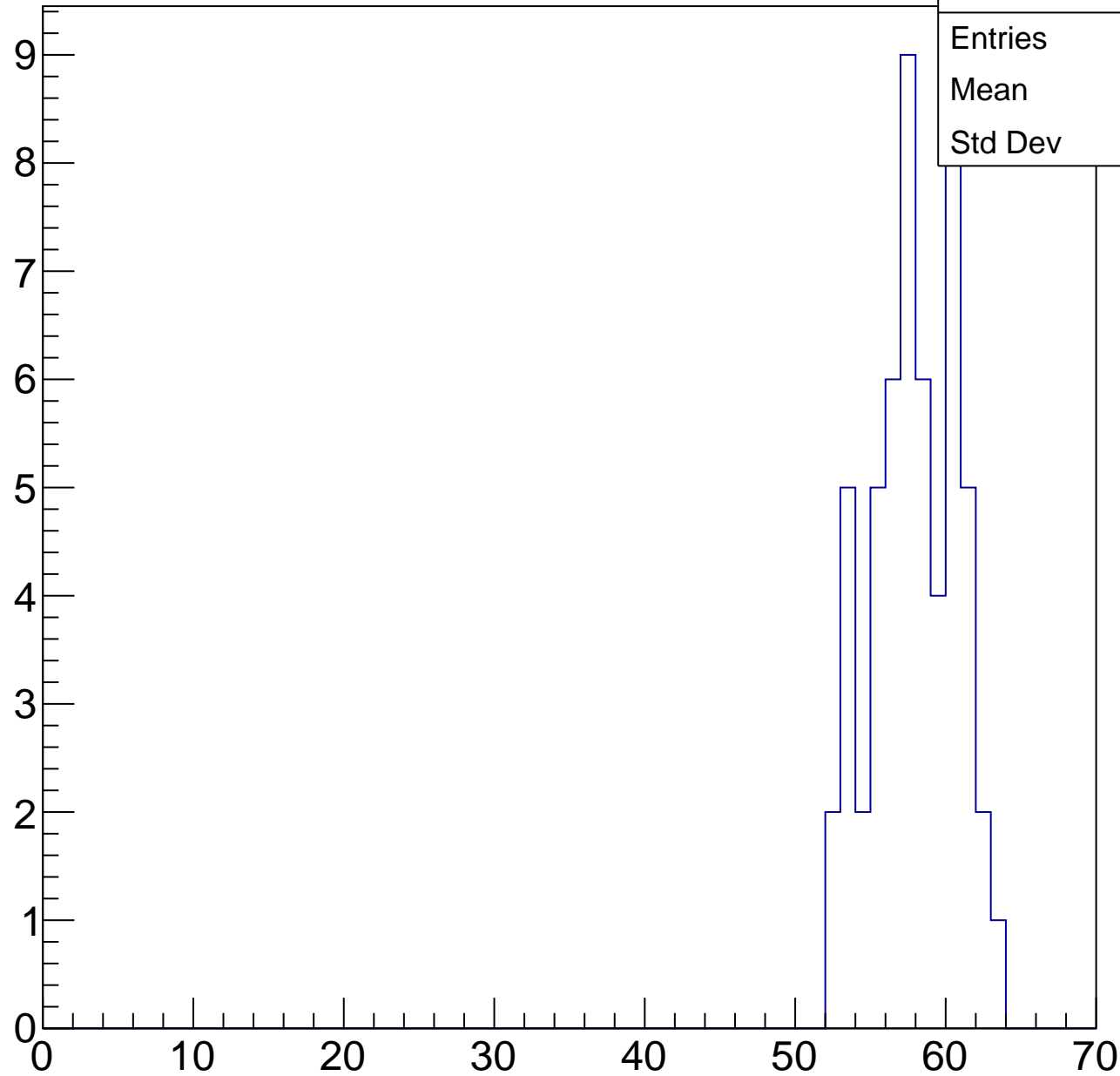
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	55
Mean	57.4
Std Dev	2.78

ampl

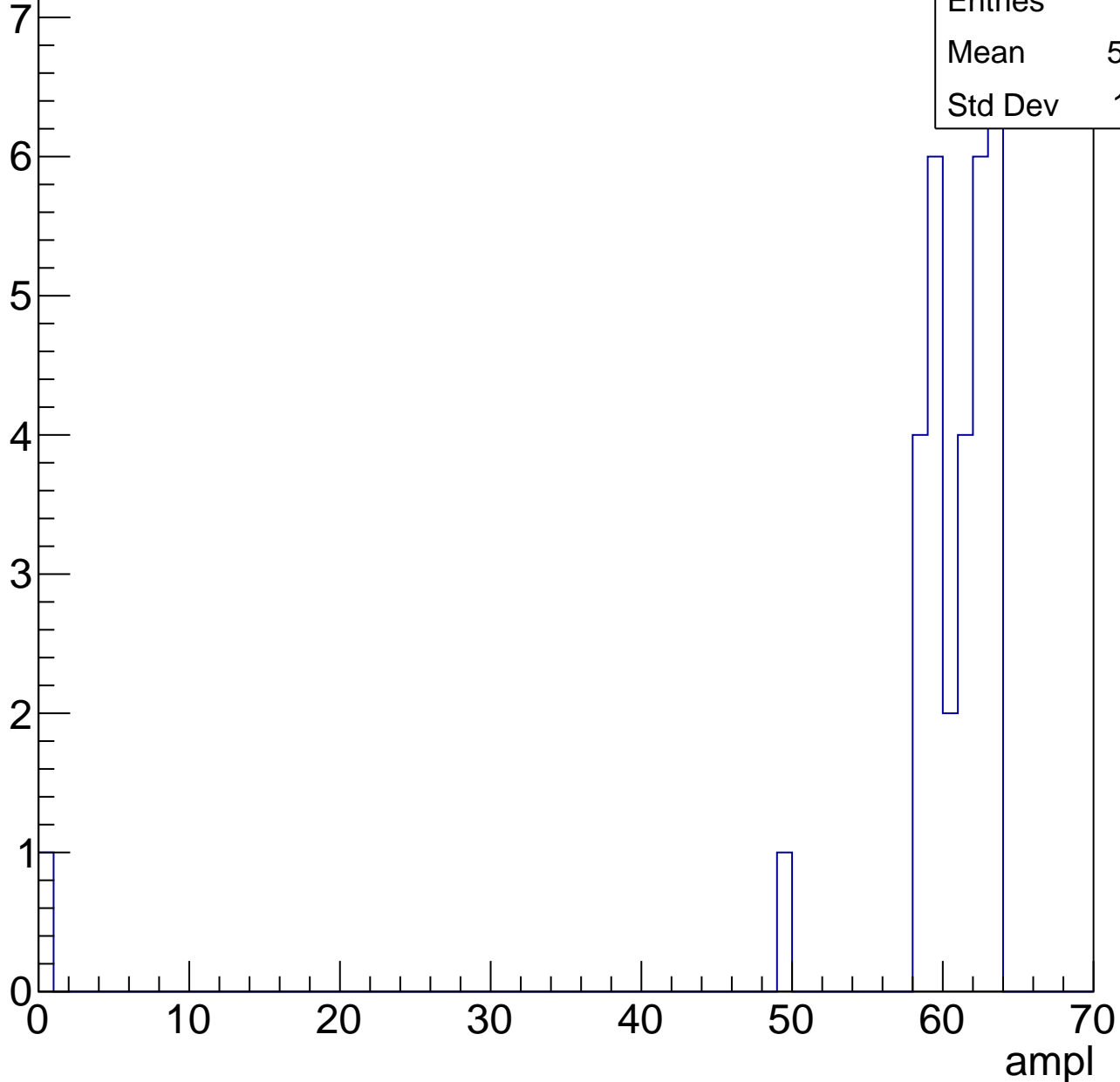


# B0L001S, U5-ch11, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	31
Mean	58.45
Std Dev	11.01



# B0L001S, U5-ch11, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch11, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch12, adc0

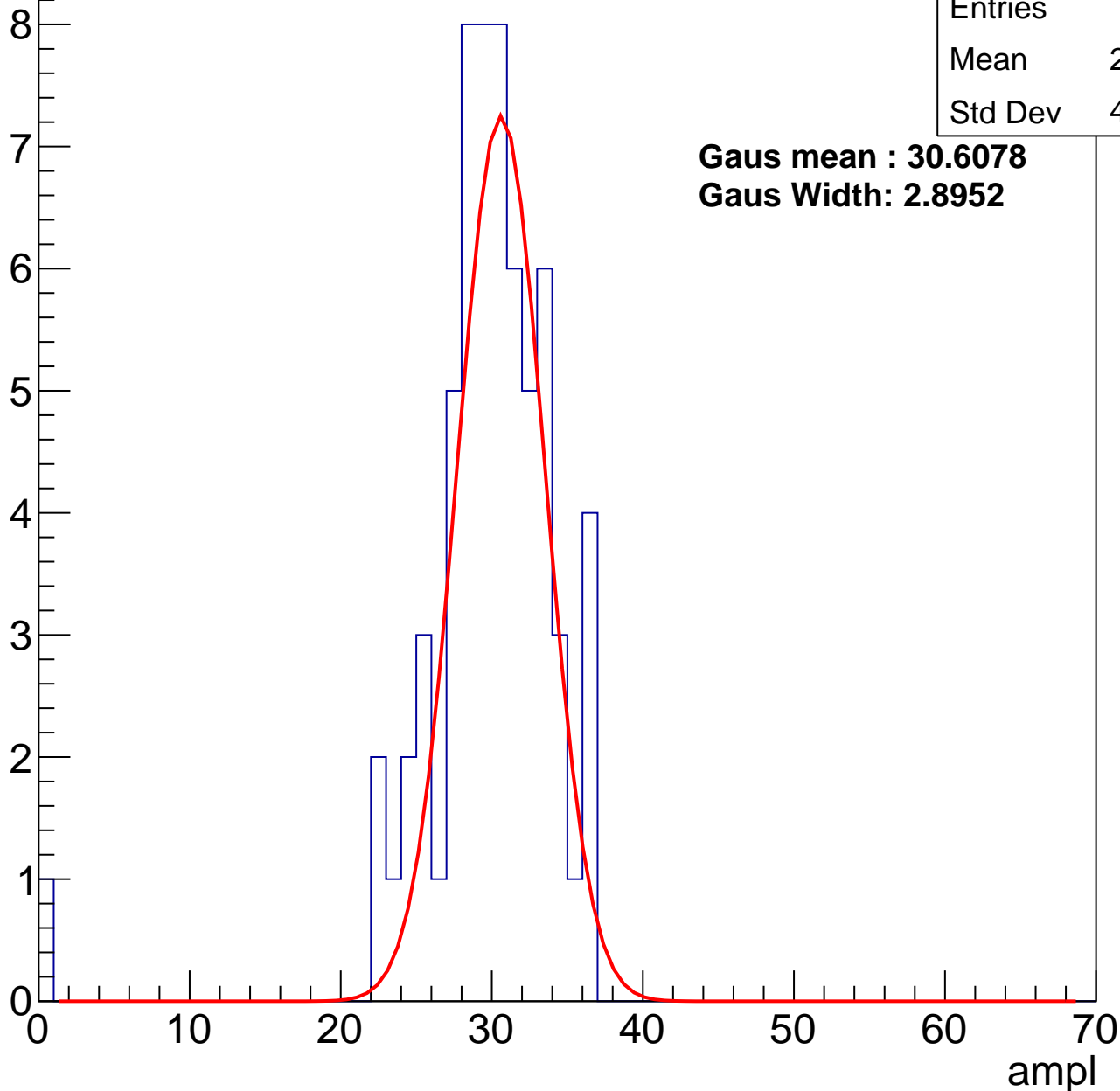
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	29.25
Std Dev	4.978

**Gaus mean : 30.6078**

**Gaus Width: 2.8952**



# B0L001S, U5-ch12, adc1

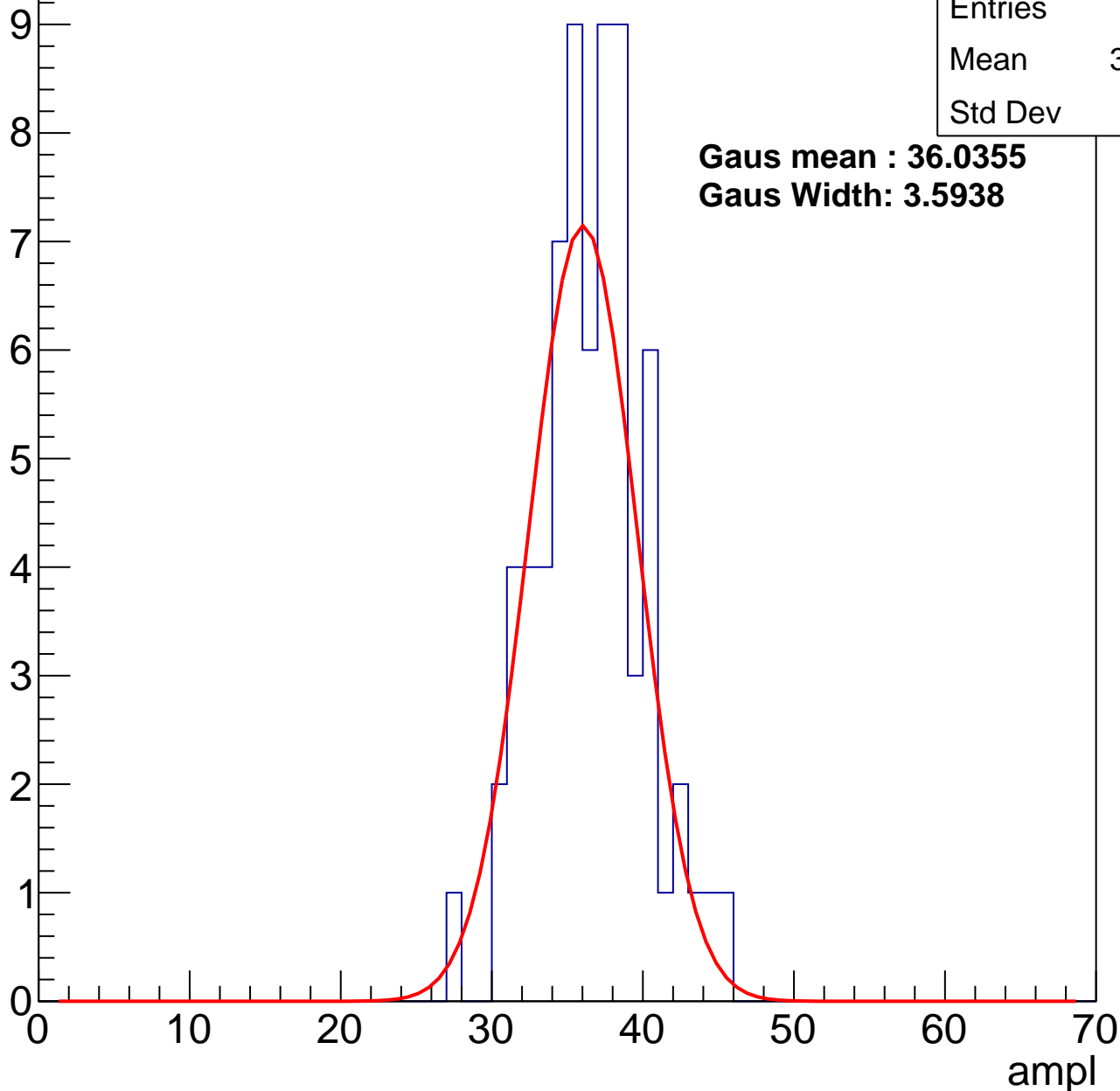
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	36.13
Std Dev	3.48

**Gaus mean : 36.0355**

**Gaus Width: 3.5938**



# B0L001S, U5-ch12, adc2

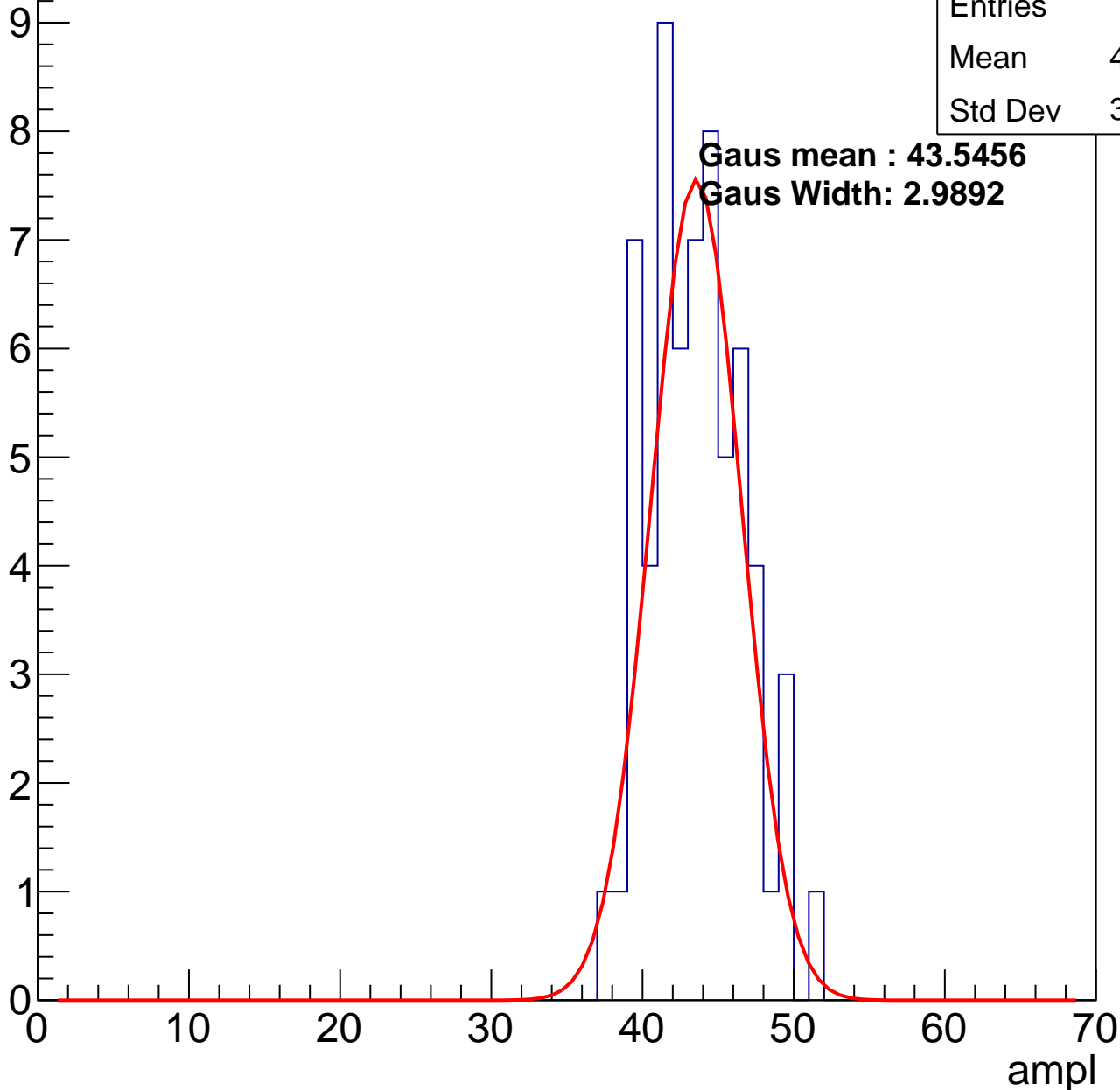
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	43.13
Std Dev	3.068

**Gaus mean : 43.5456**

**Gaus Width: 2.9892**

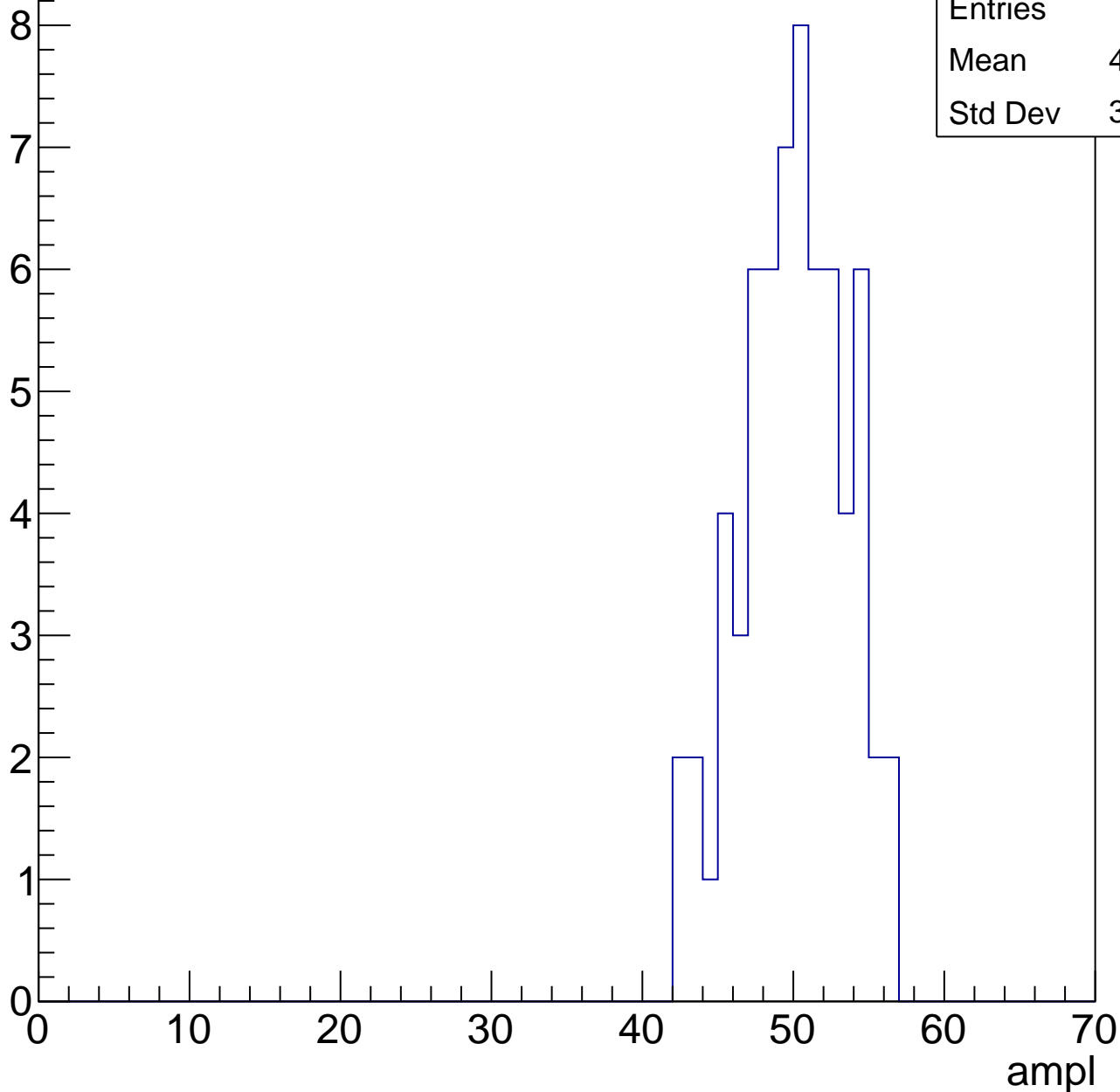


# B0L001S, U5-ch12, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	49.55
Std Dev	3.433

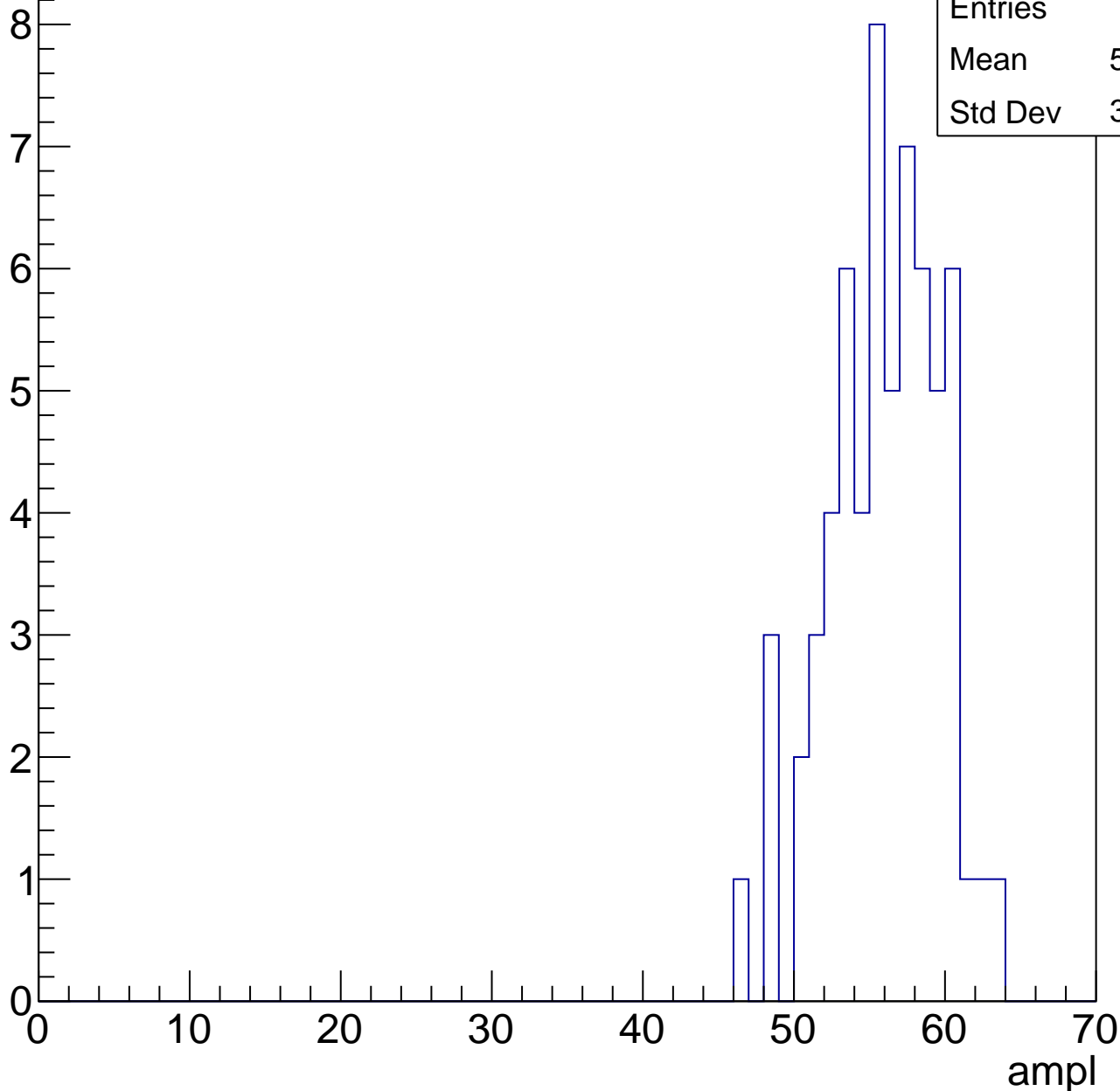


# B0L001S, U5-ch12, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	55.44
Std Dev	3.659

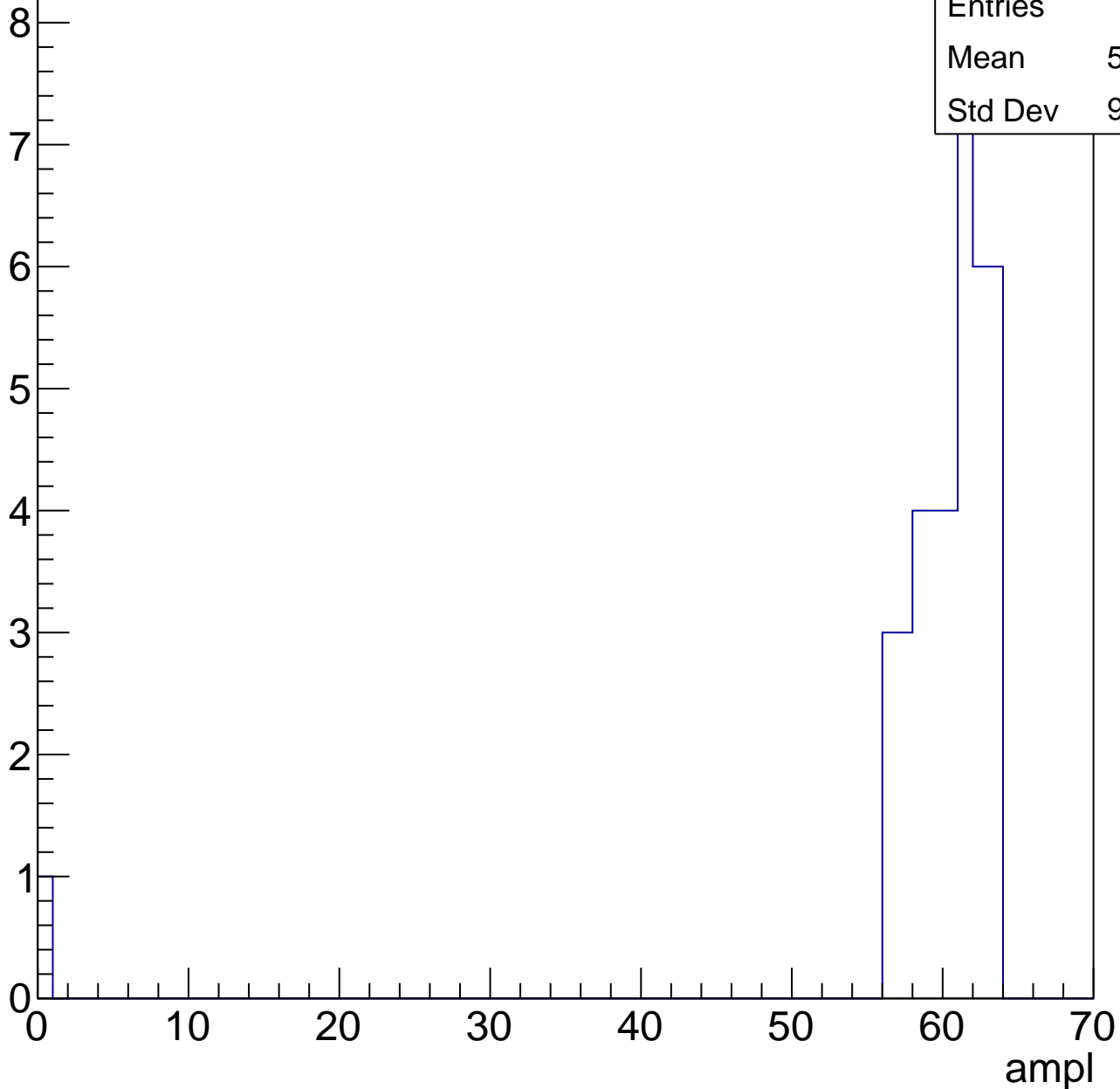


# B0L001S, U5-ch12, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

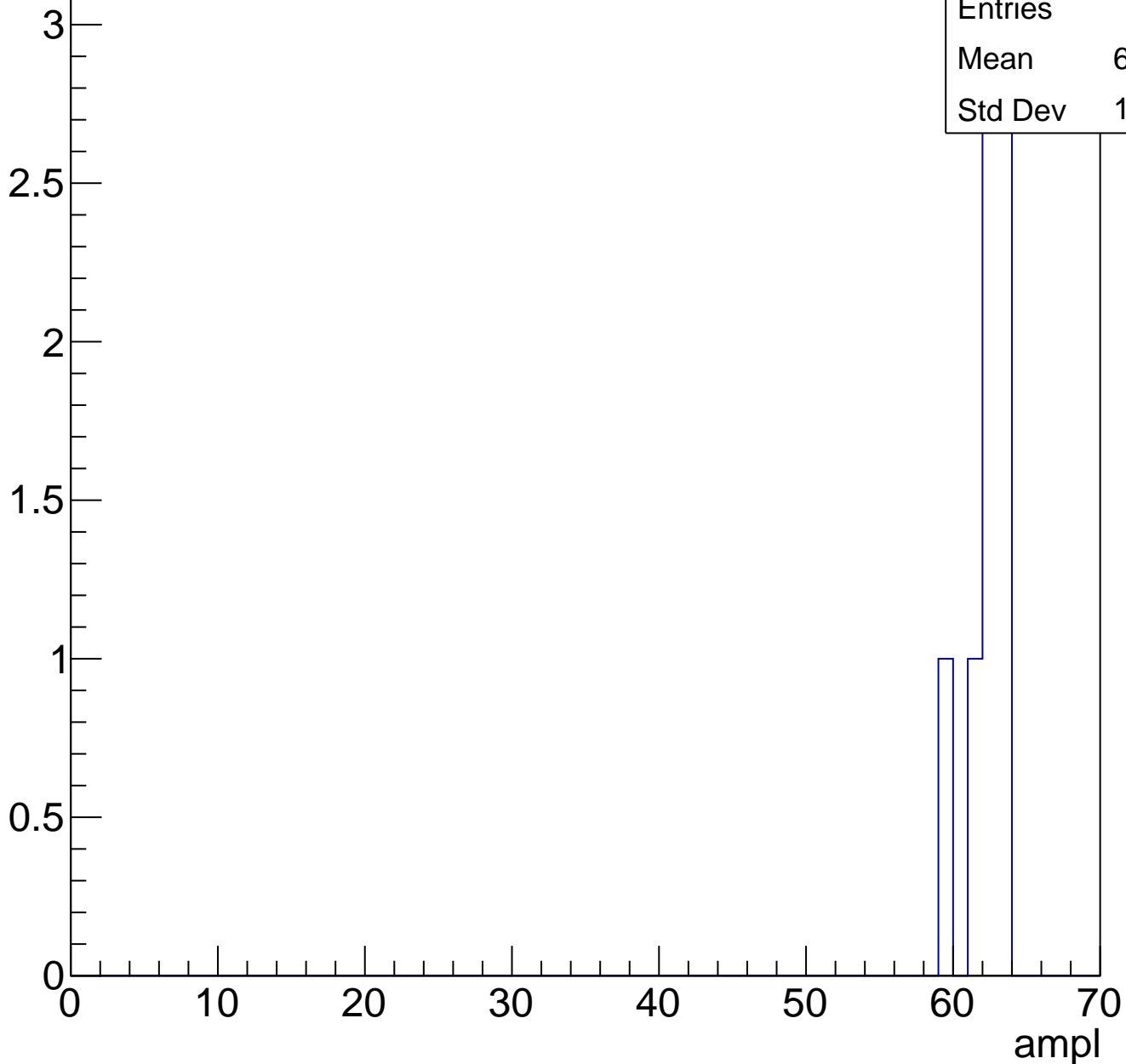
Entries	39
Mean	58.59
Std Dev	9.745



# B0L001S, U5-ch12, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch12, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch13, adc0

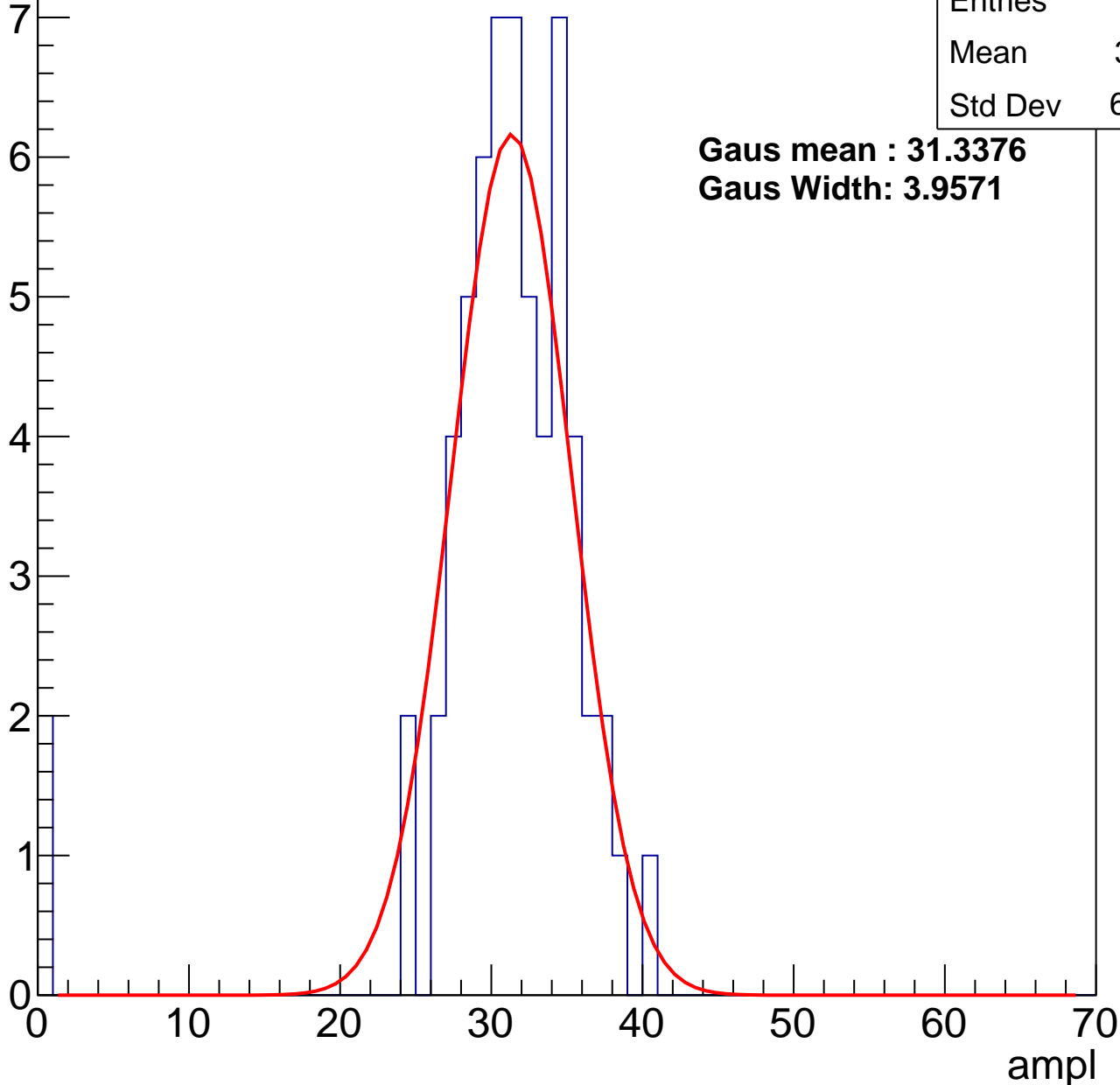
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	30.21
Std Dev	6.494

**Gaus mean : 31.3376**

**Gaus Width: 3.9571**



# B0L001S, U5-ch13, adc1

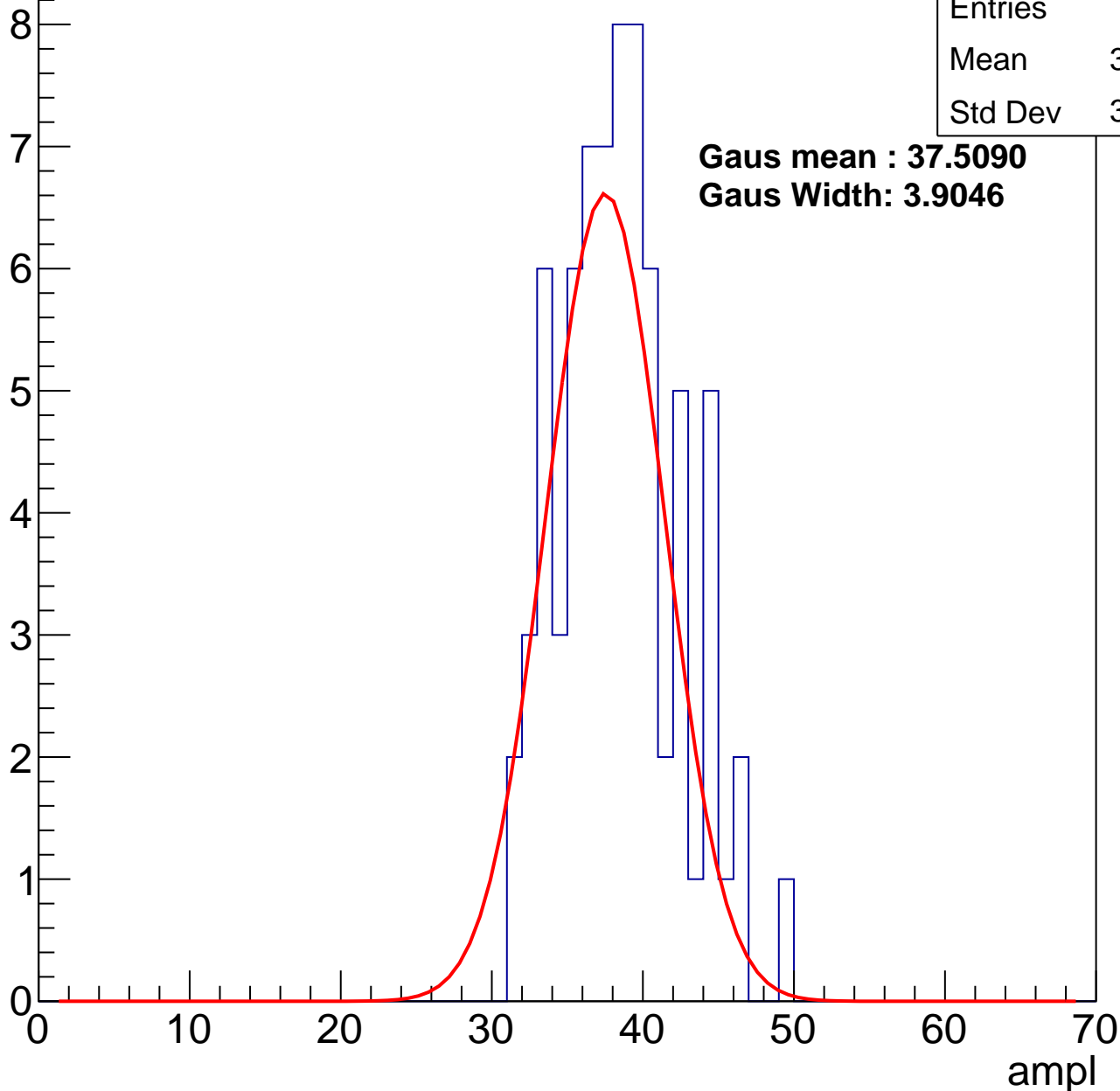
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	38.03
Std Dev	3.927

**Gaus mean : 37.5090**

**Gaus Width: 3.9046**



# B0L001S, U5-ch13, adc2

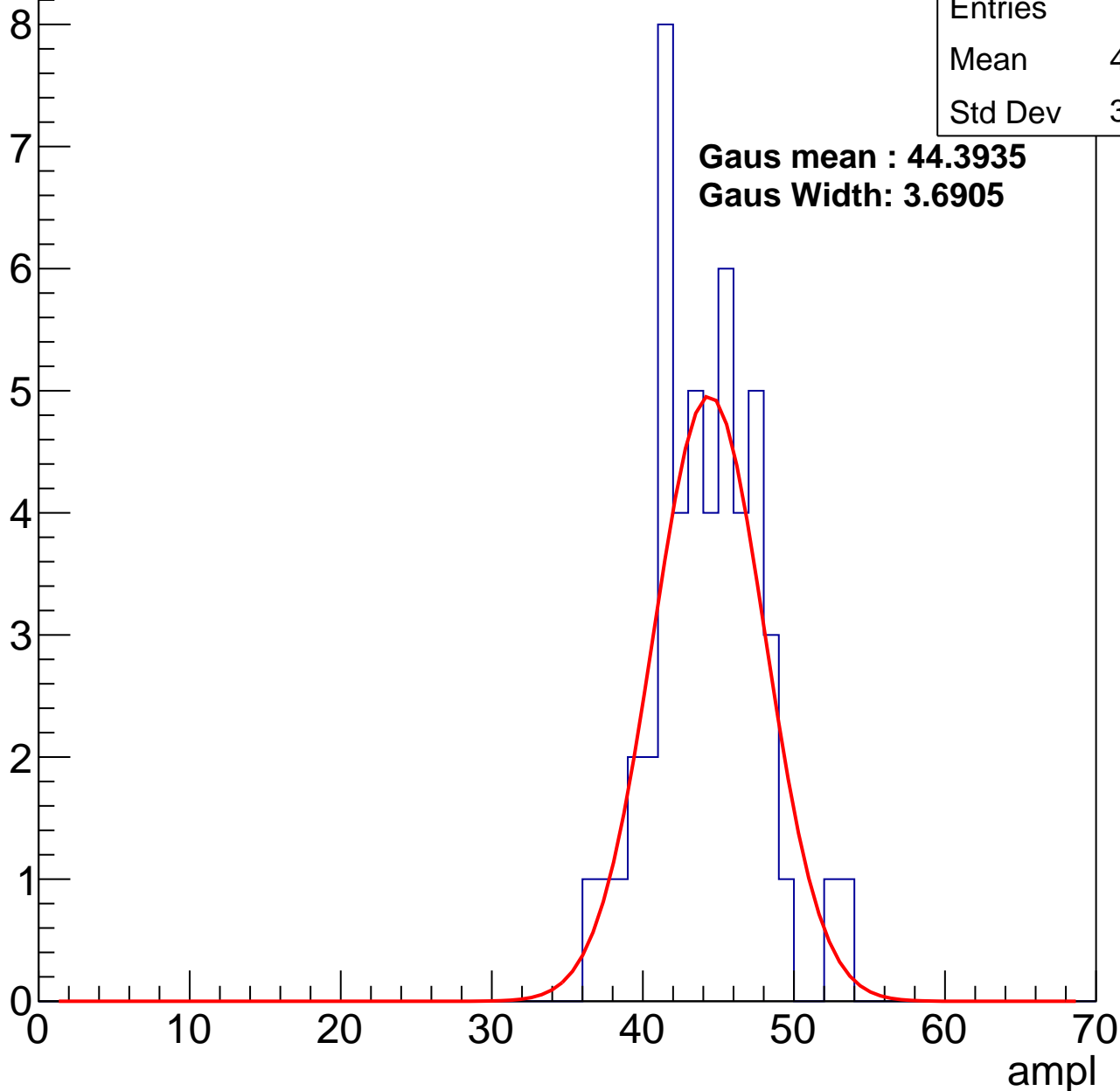
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	49
Mean	43.73
Std Dev	3.515

**Gaus mean : 44.3935**

**Gaus Width: 3.6905**

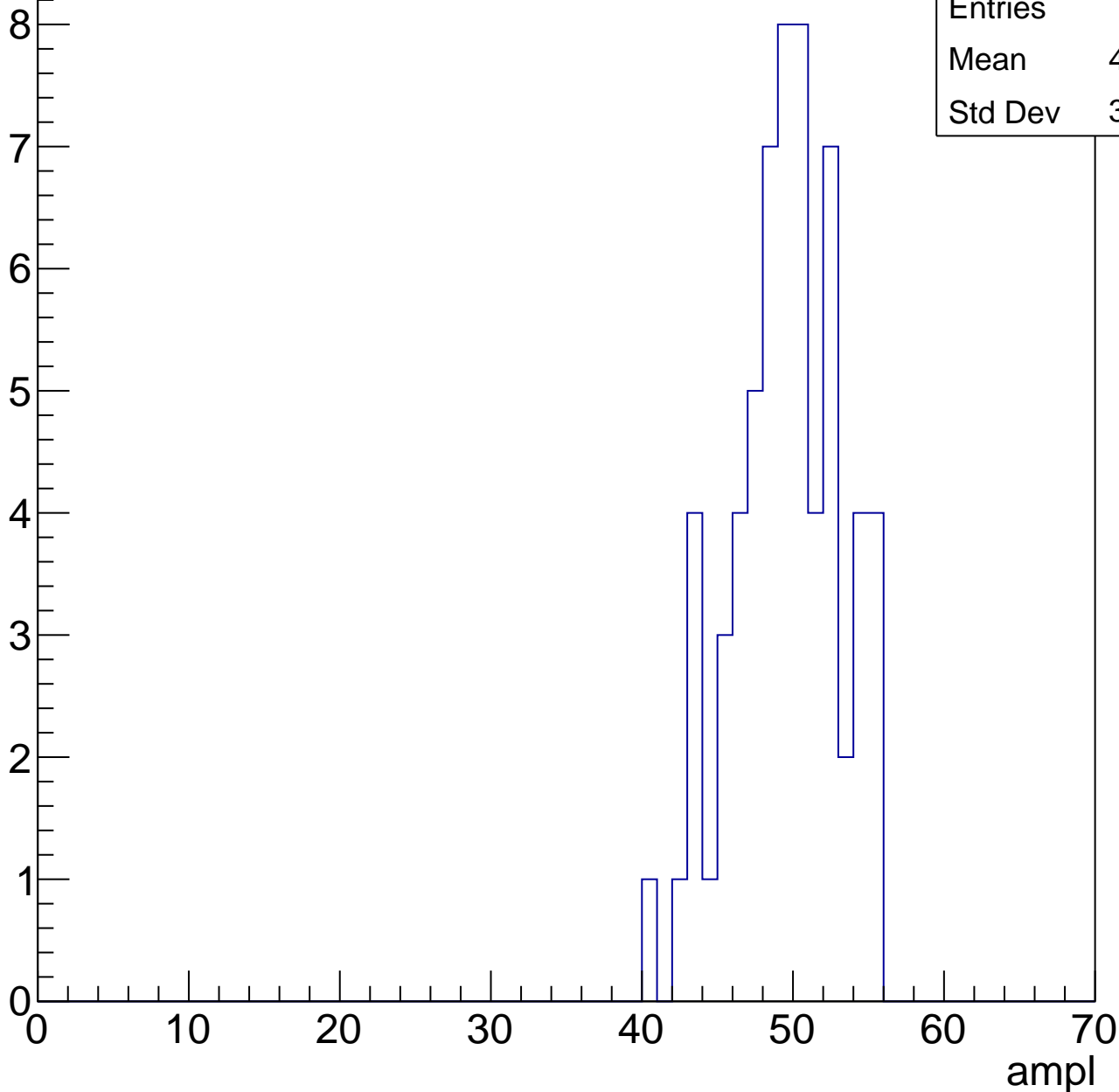


# B0L001S, U5-ch13, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	49.05
Std Dev	3.503



# B0L001S, U5-ch13, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	64
Mean	55.81
Std Dev	3.127

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

ampl

0

2

4

6

8

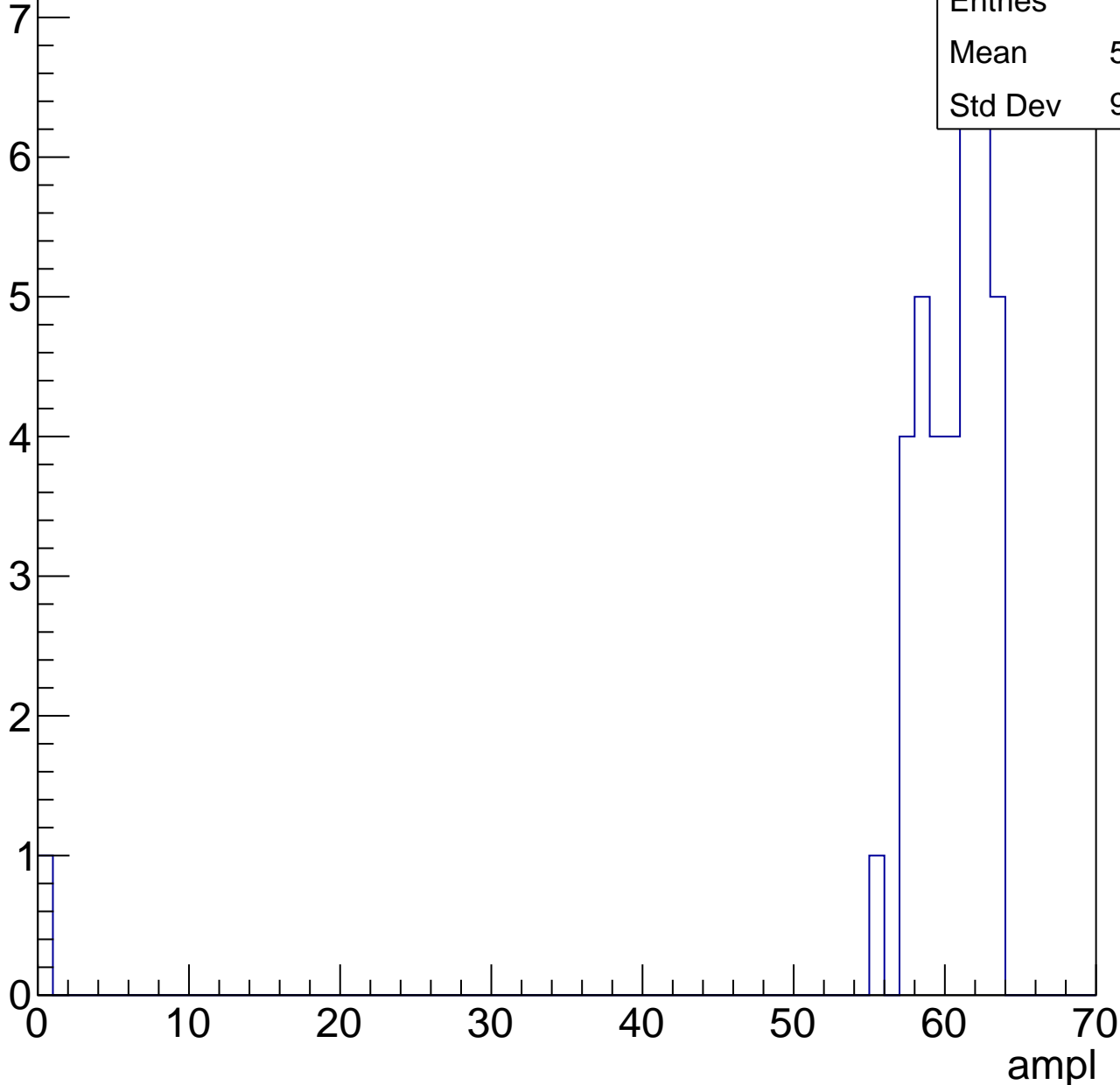
10

# B0L001S, U5-ch13, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	38
Mean	58.55
Std Dev	9.848

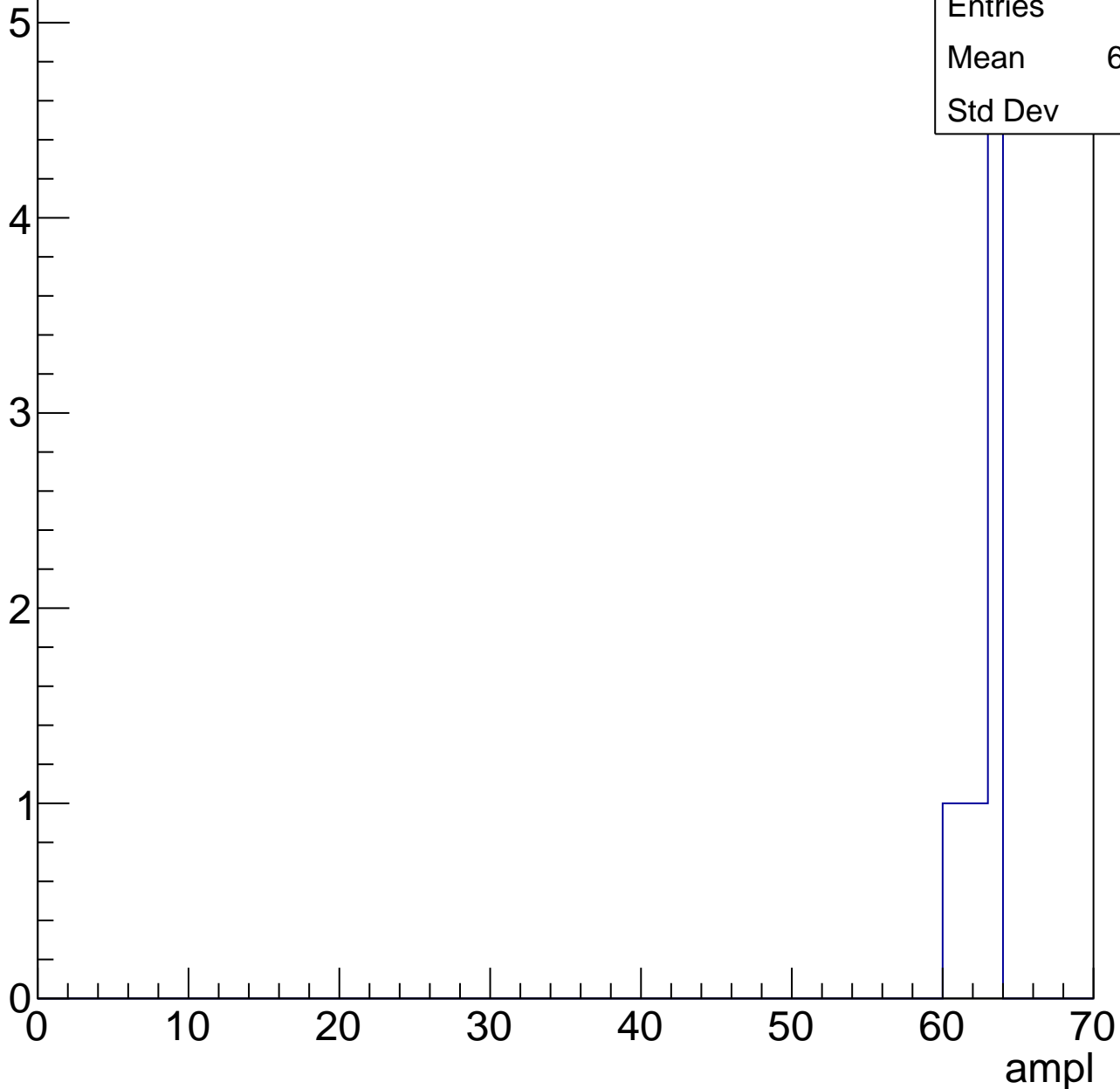


# B0L001S, U5-ch13, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	8
Mean	62.25
Std Dev	1.09





# B0L001S, U5-ch13, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U5-ch14, adc0

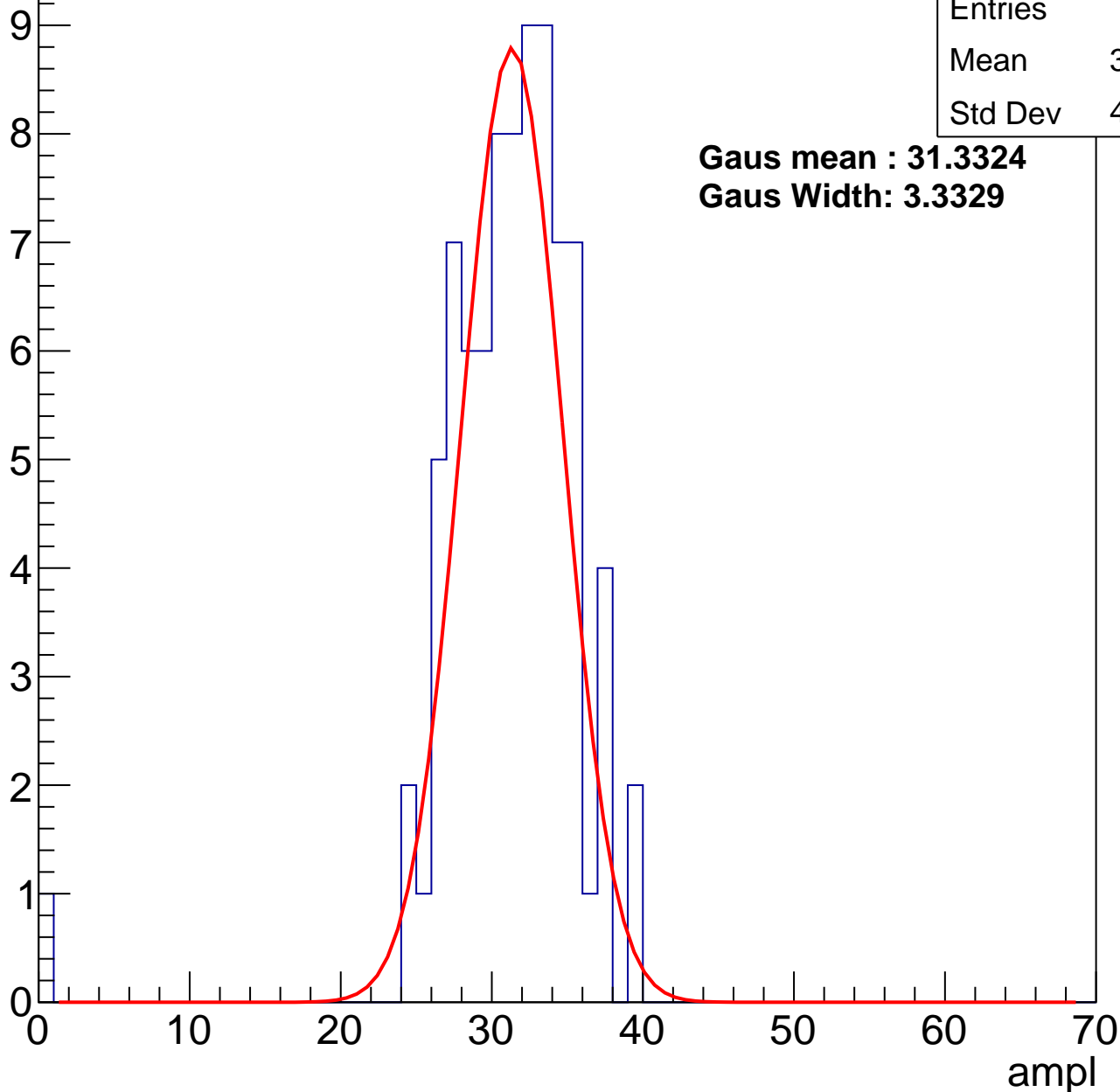
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	83
Mean	30.75
Std Dev	4.822

**Gaus mean : 31.3324**

**Gaus Width: 3.3329**



# B0L001S, U5-ch14, adc1

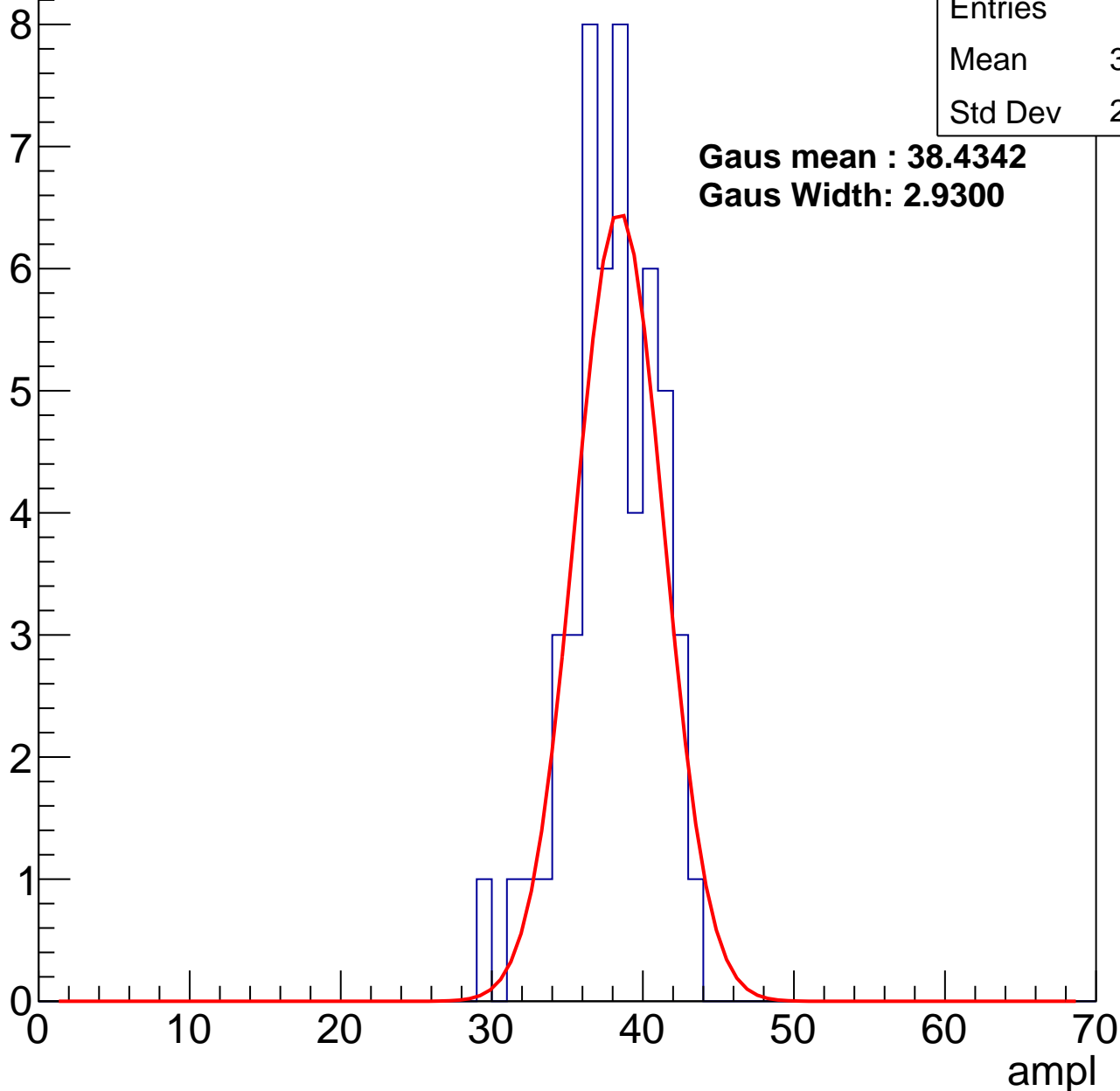
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	51
Mean	37.57
Std Dev	2.939

**Gaus mean : 38.4342**

**Gaus Width: 2.9300**



# B0L001S, U5-ch14, adc2

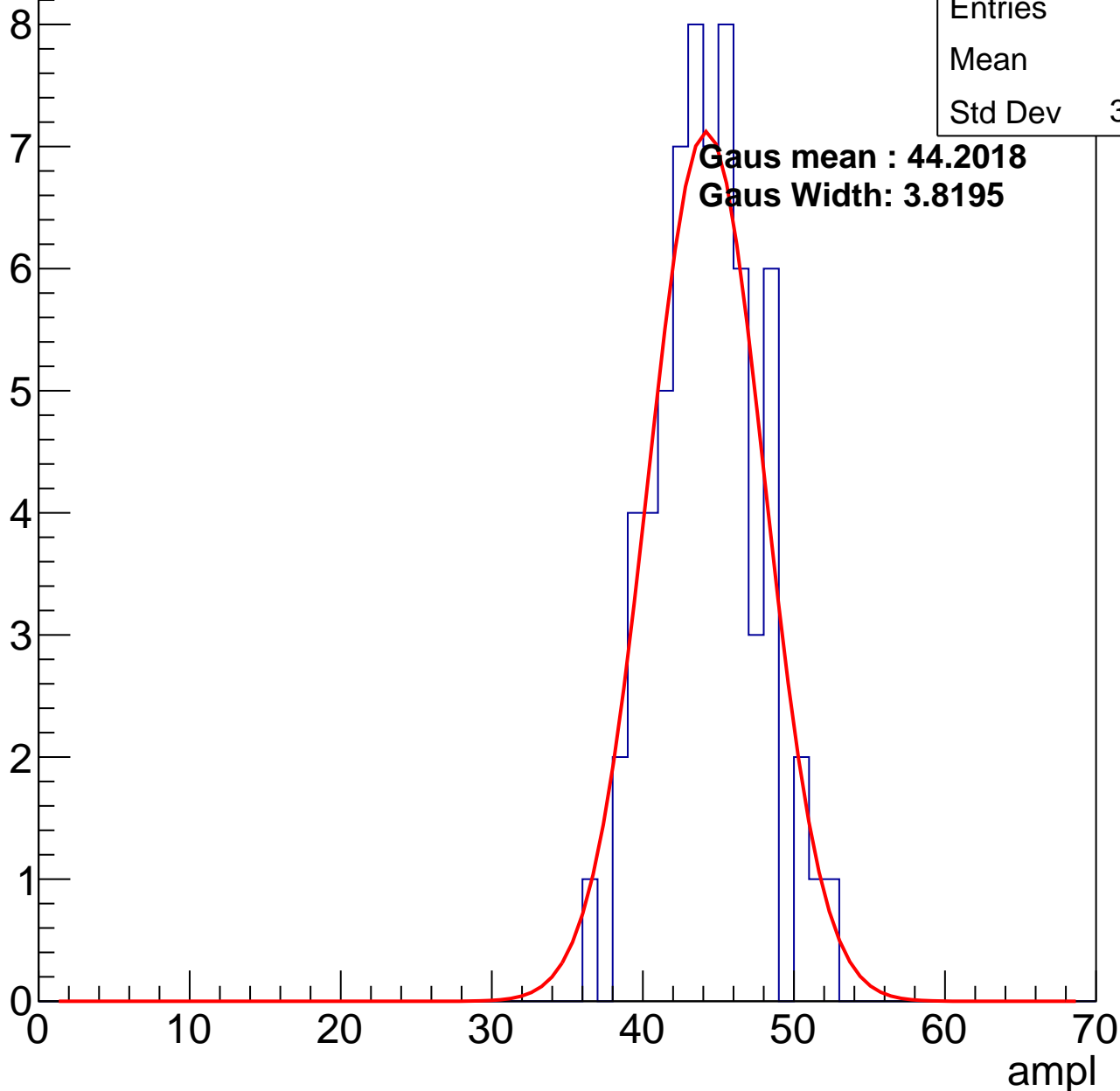
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	43.8
Std Dev	3.325

**Gaus mean : 44.2018**

**Gaus Width: 3.8195**



# B0L001S, U5-ch14, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

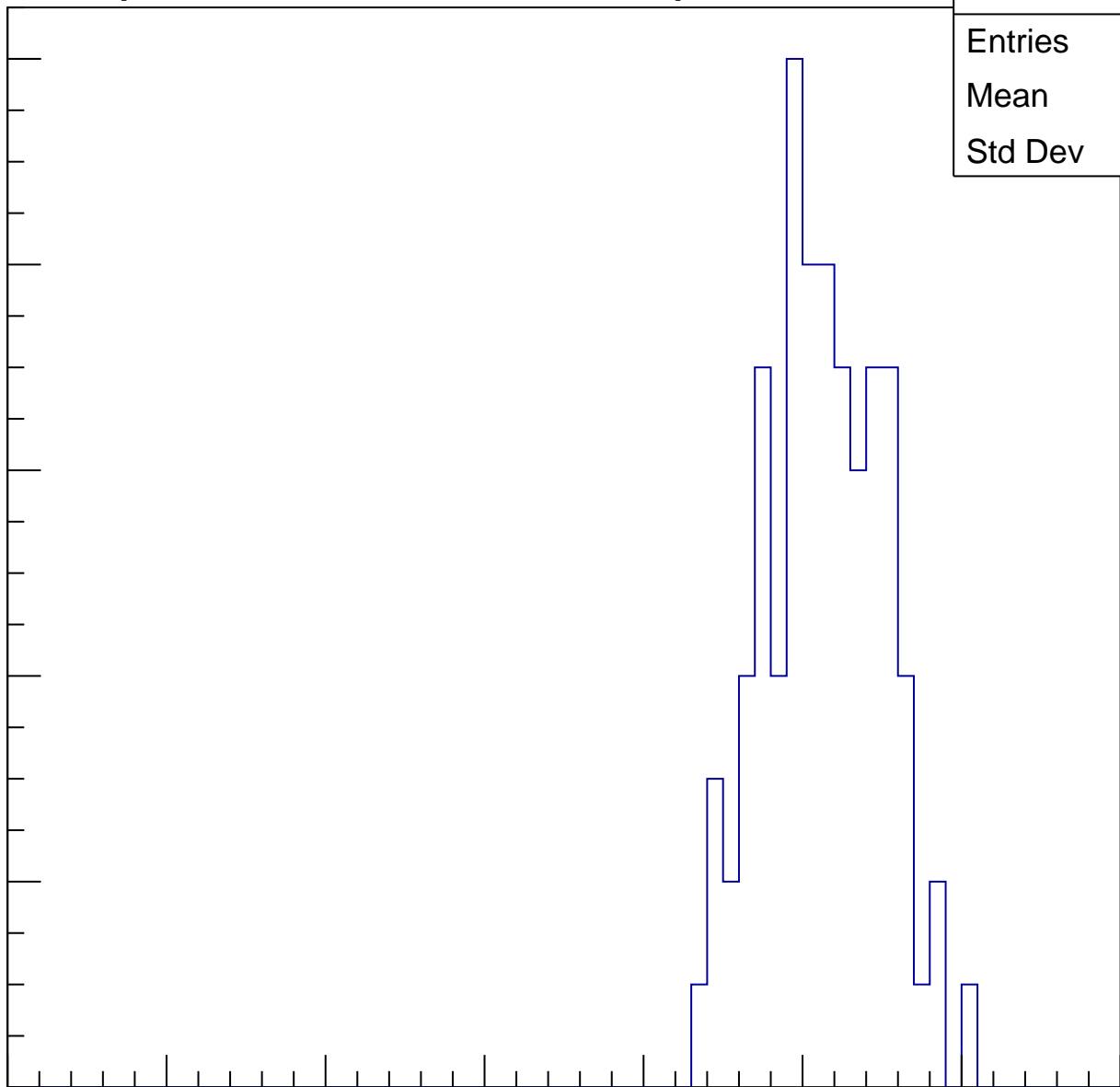
Entries	82
Mean	50.85
Std Dev	3.66

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

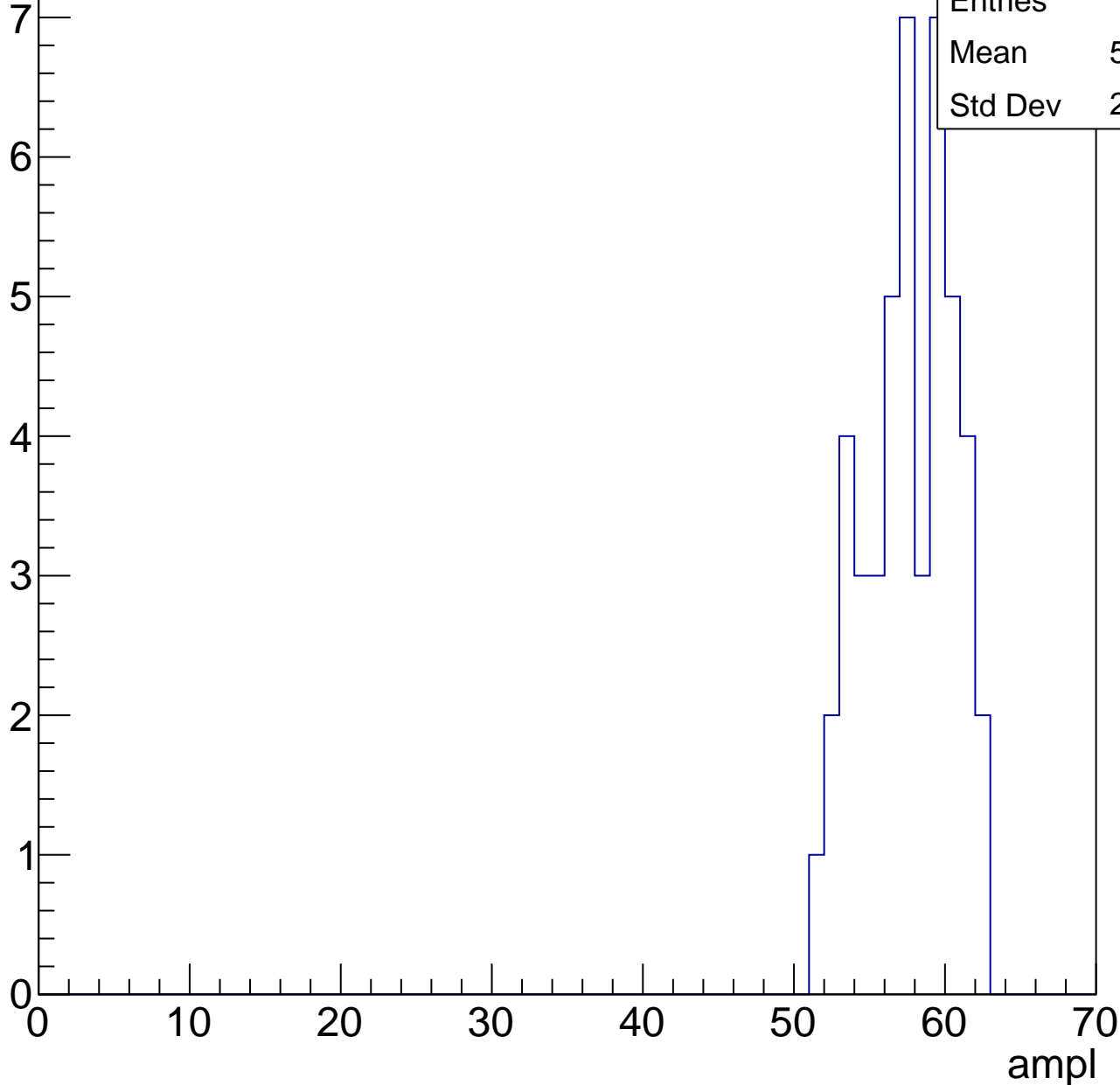
ampl



# B0L001S, U5-ch14, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch14, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

10

Entries 37

Mean 60.73

Std Dev 2.101

8

6

4

2

0

0

10

20

30

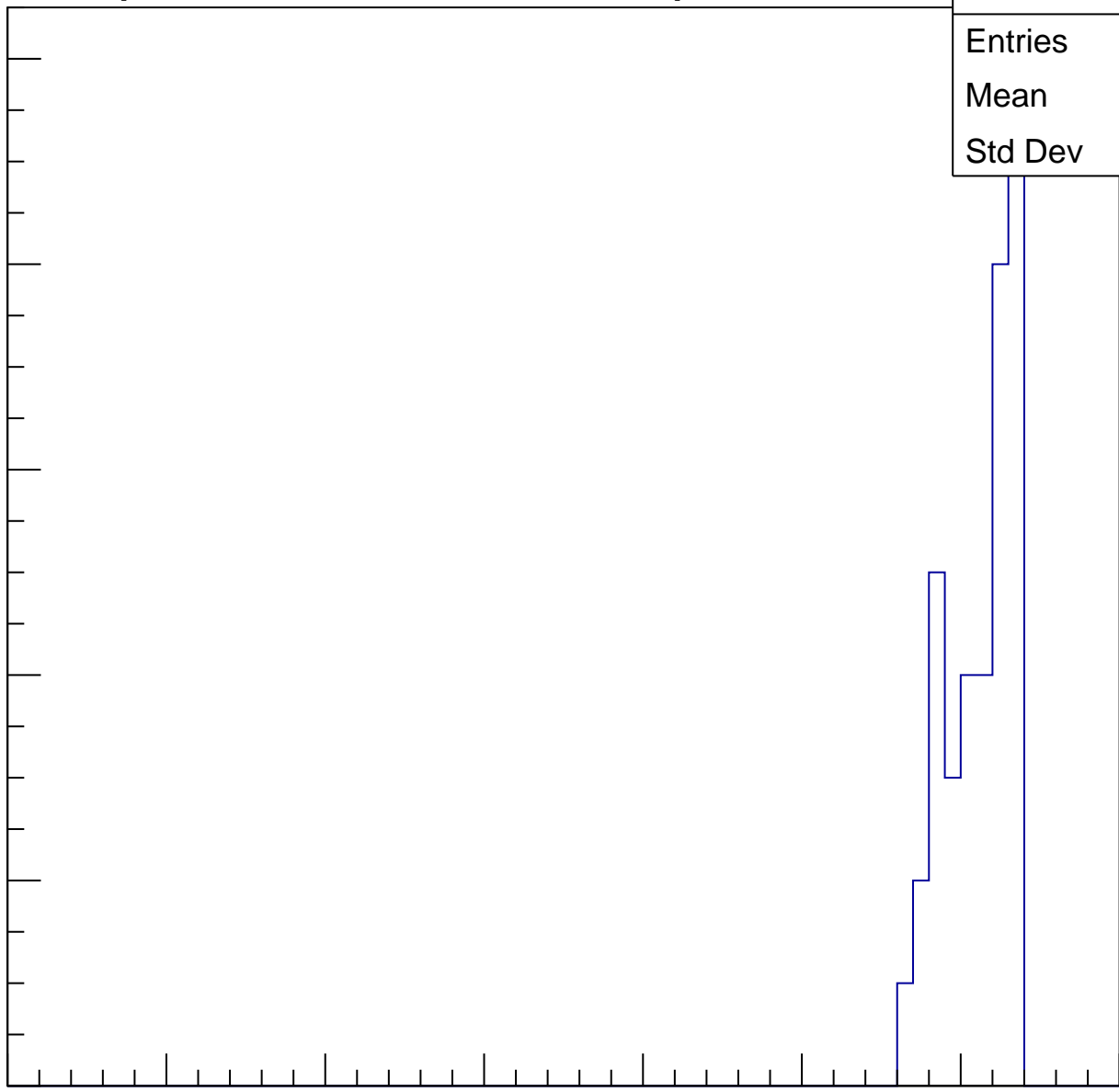
40

50

60

70

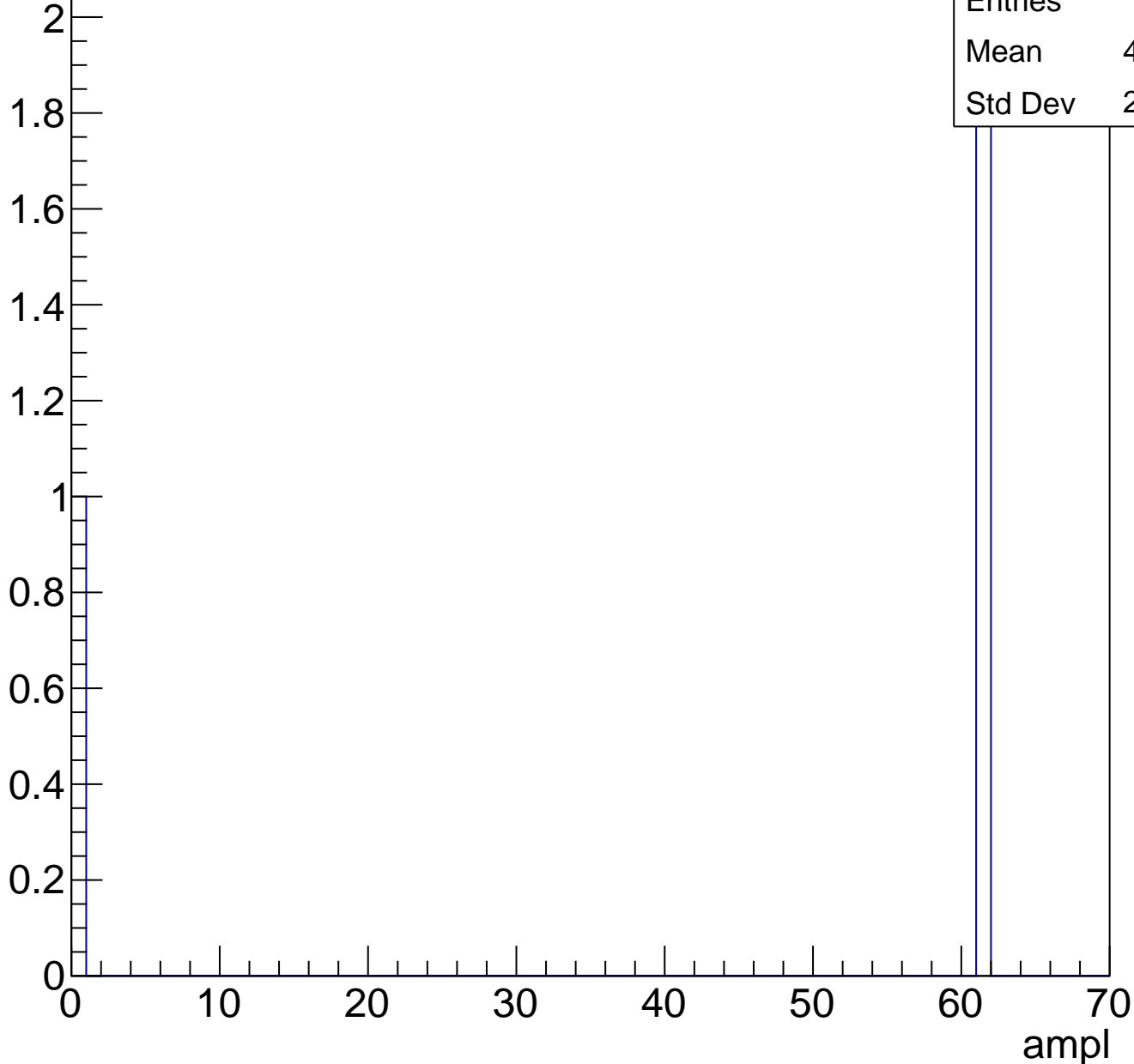
ampl



# B0L001S, U5-ch14, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

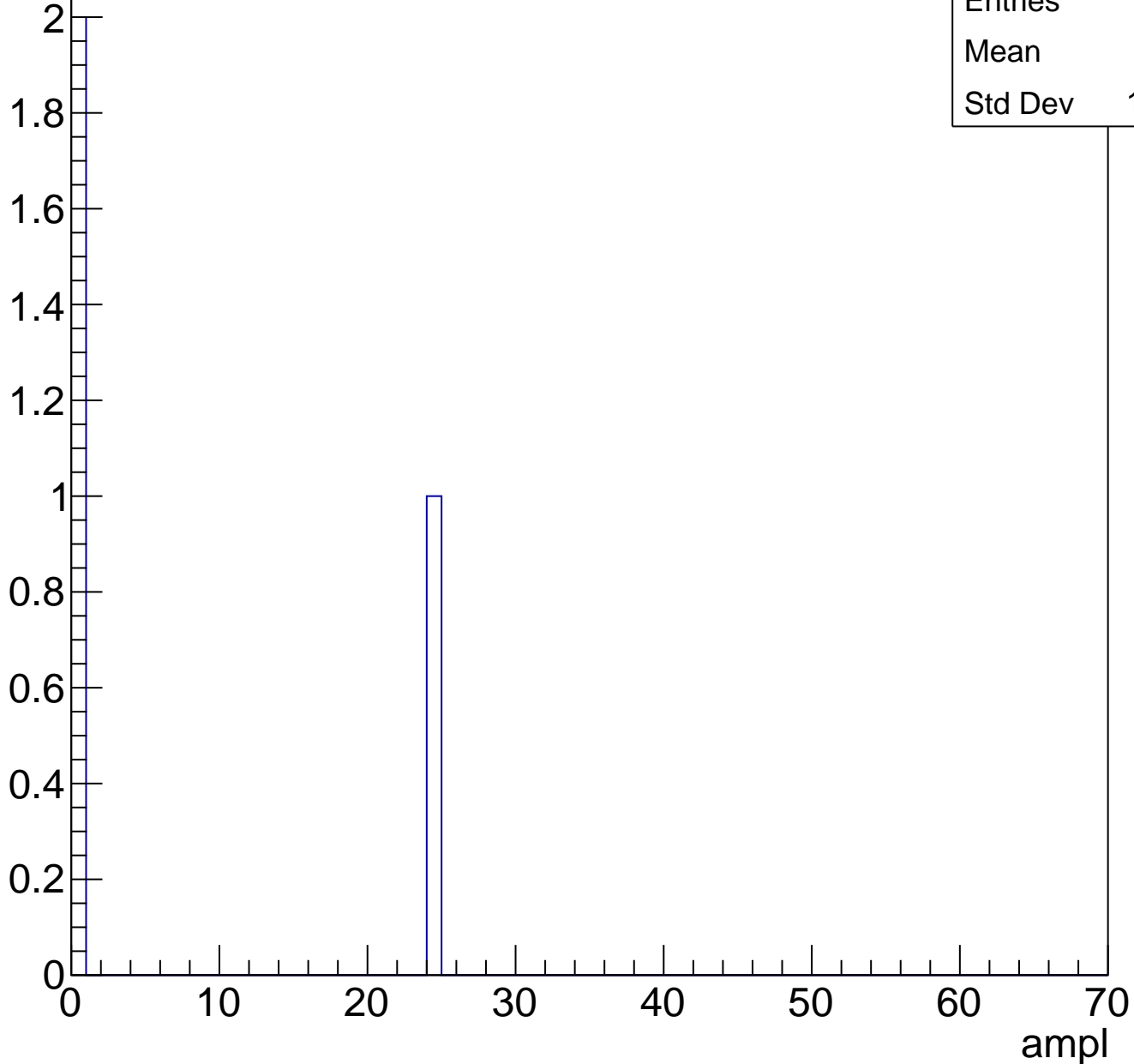




# B0L001S, U5-ch14, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch15, adc0

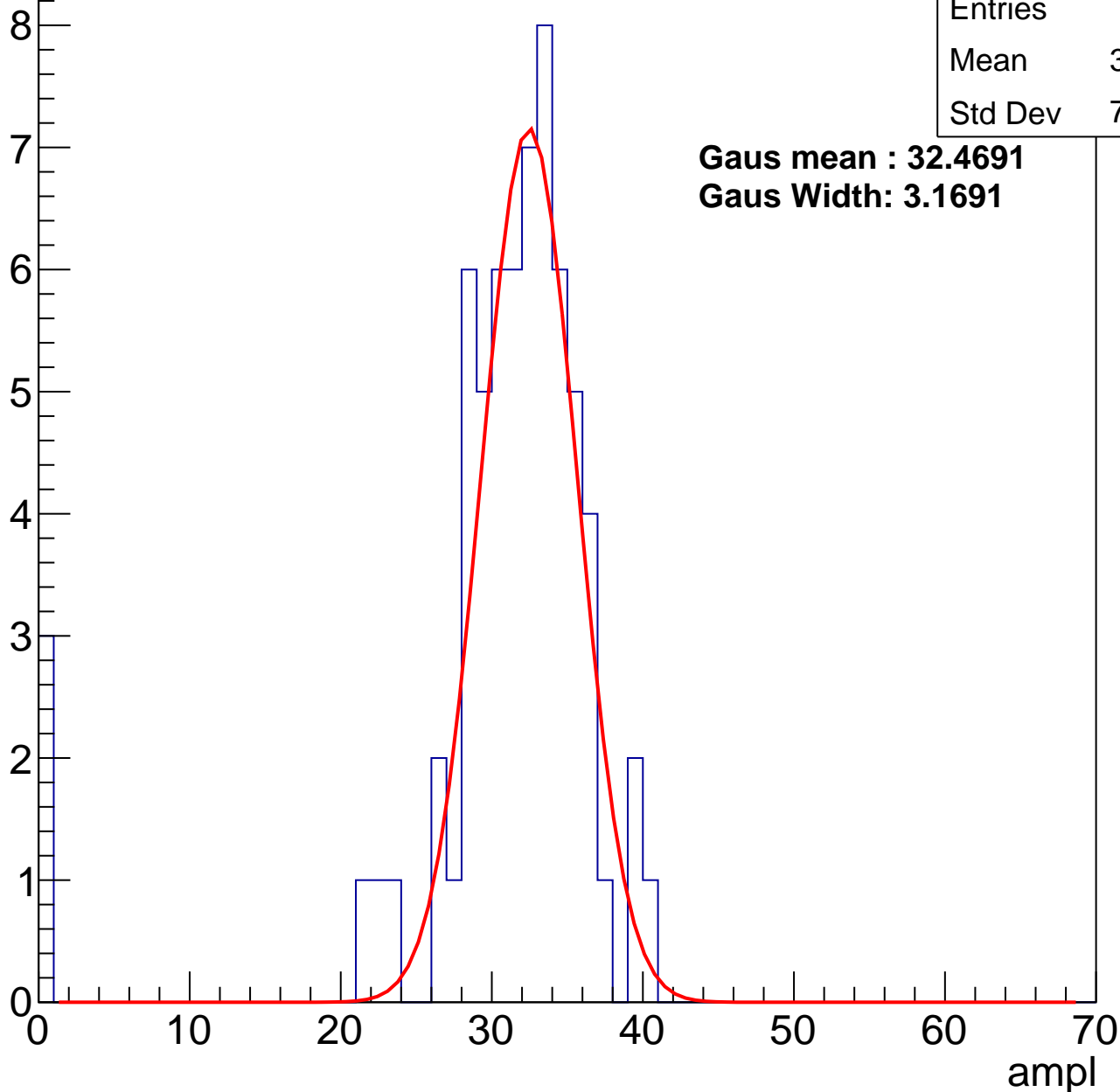
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	30.15
Std Dev	7.532

**Gaus mean : 32.4691**

**Gaus Width: 3.1691**



# B0L001S, U5-ch15, adc1

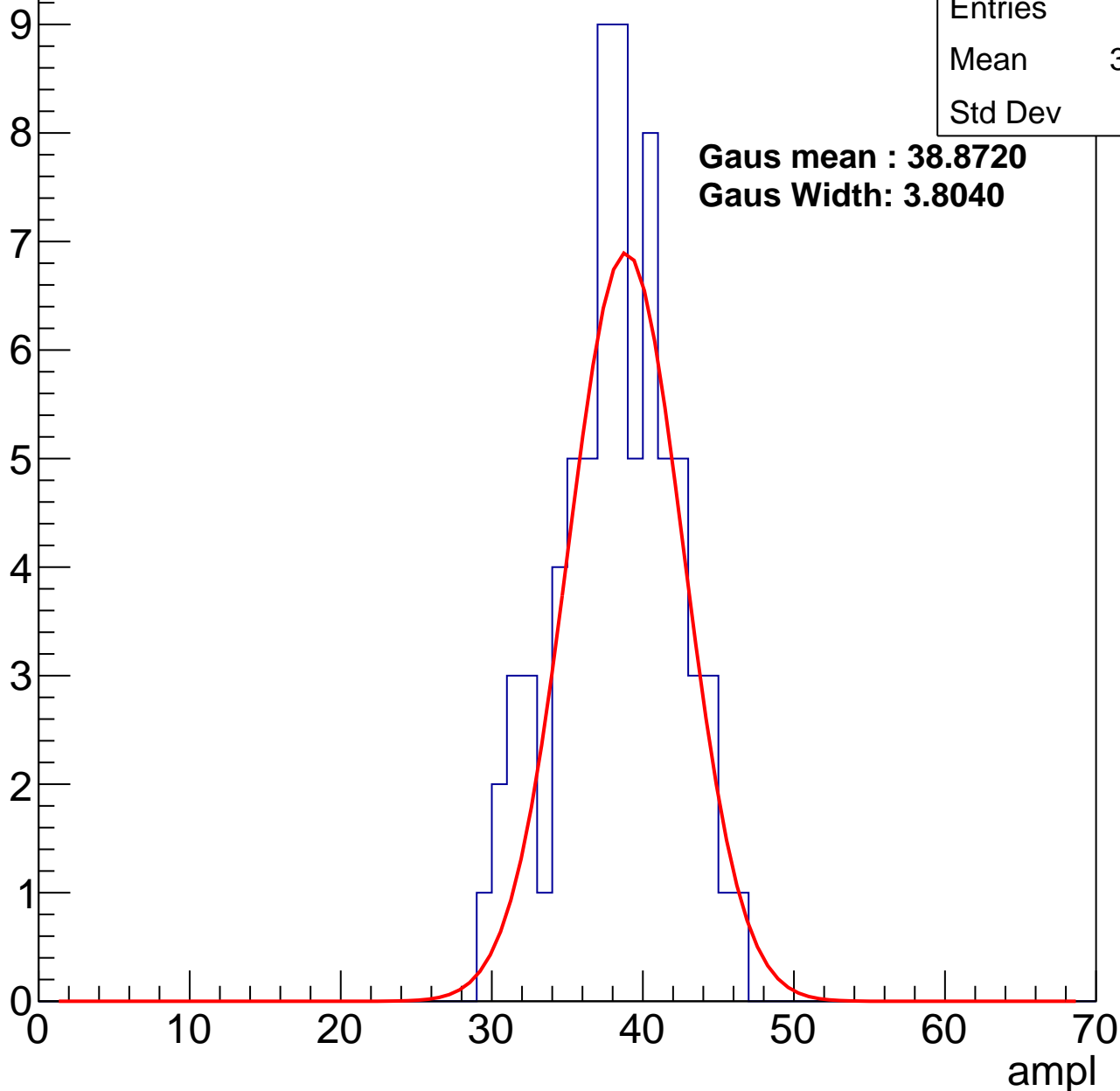
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	37.79
Std Dev	3.85

**Gaus mean : 38.8720**

**Gaus Width: 3.8040**



# B0L001S, U5-ch15, adc2

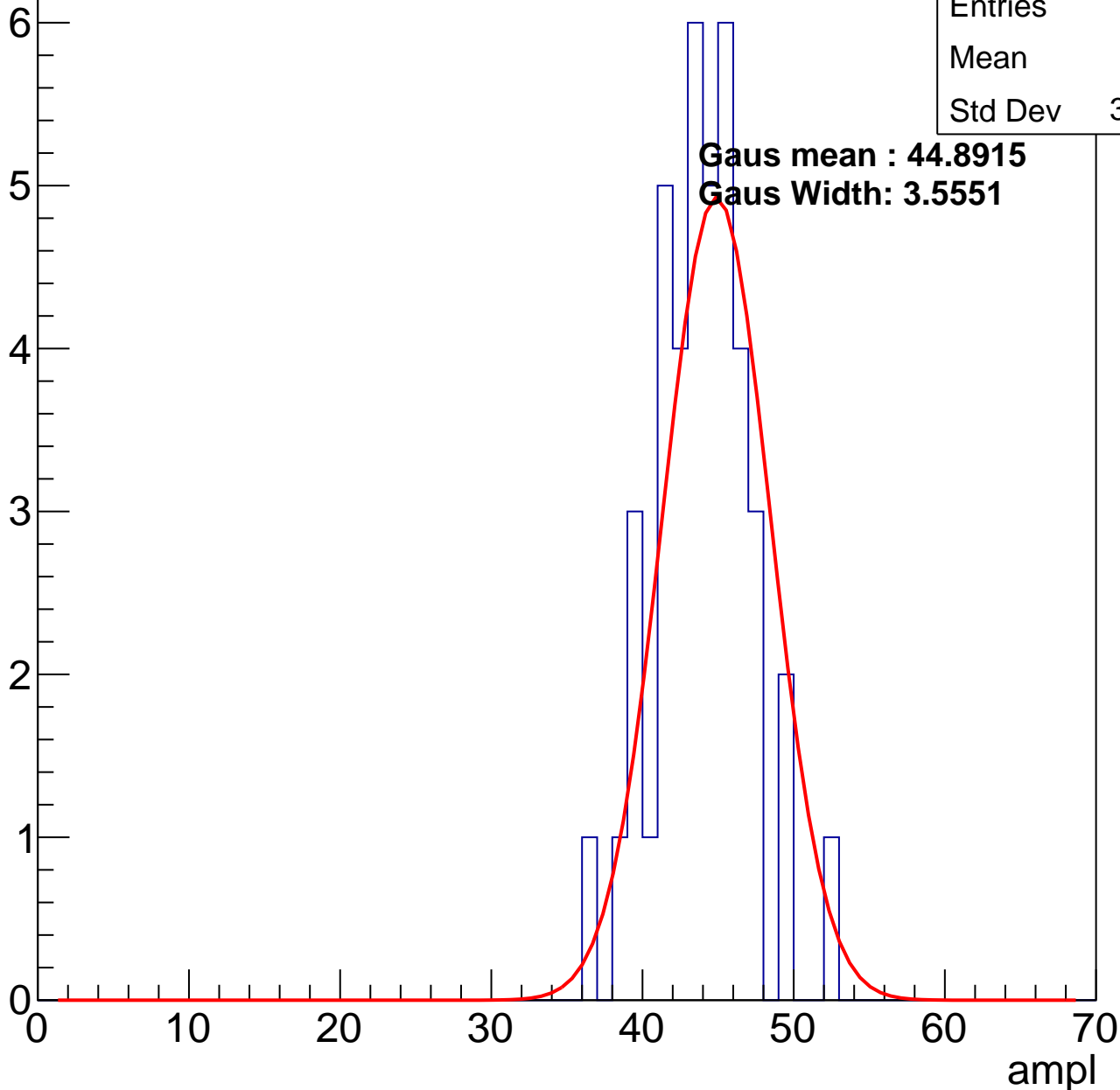
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	42
Mean	43.5
Std Dev	3.126

**Gaus mean : 44.8915**

**Gaus Width: 3.5551**

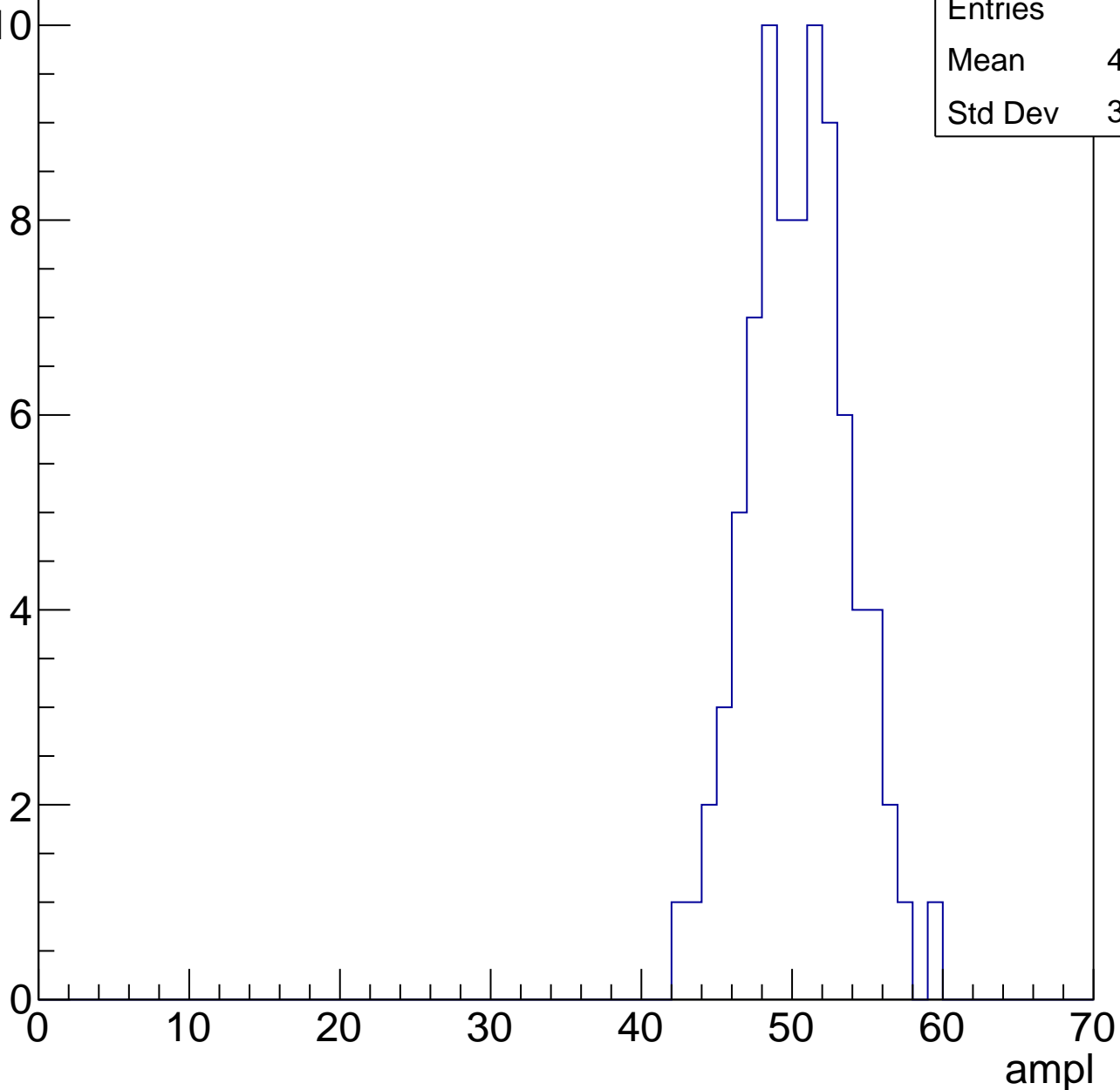


# B0L001S, U5-ch15, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

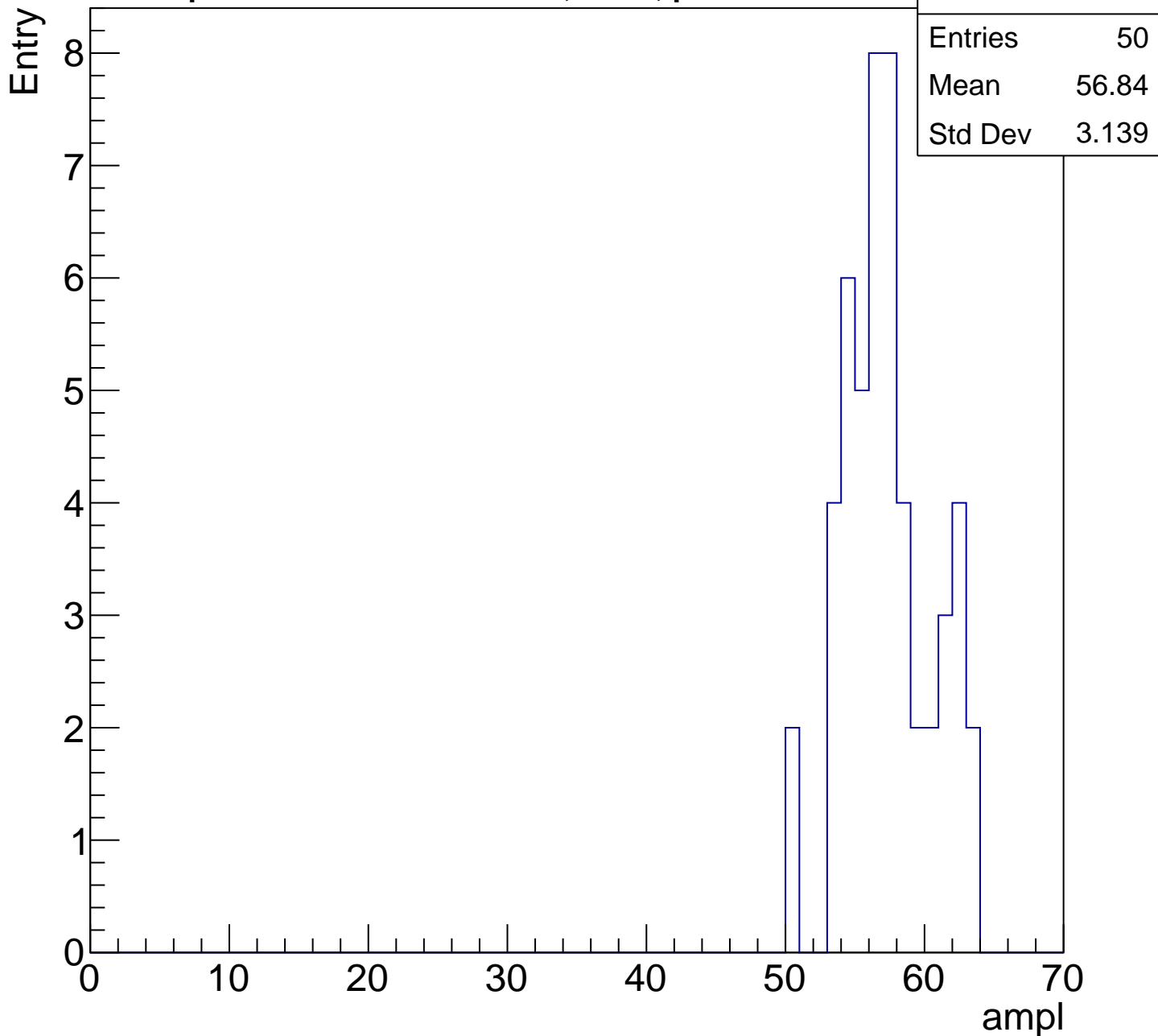
Entry

Entries	82
Mean	49.99
Std Dev	3.344



# B0L001S, U5-ch15, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

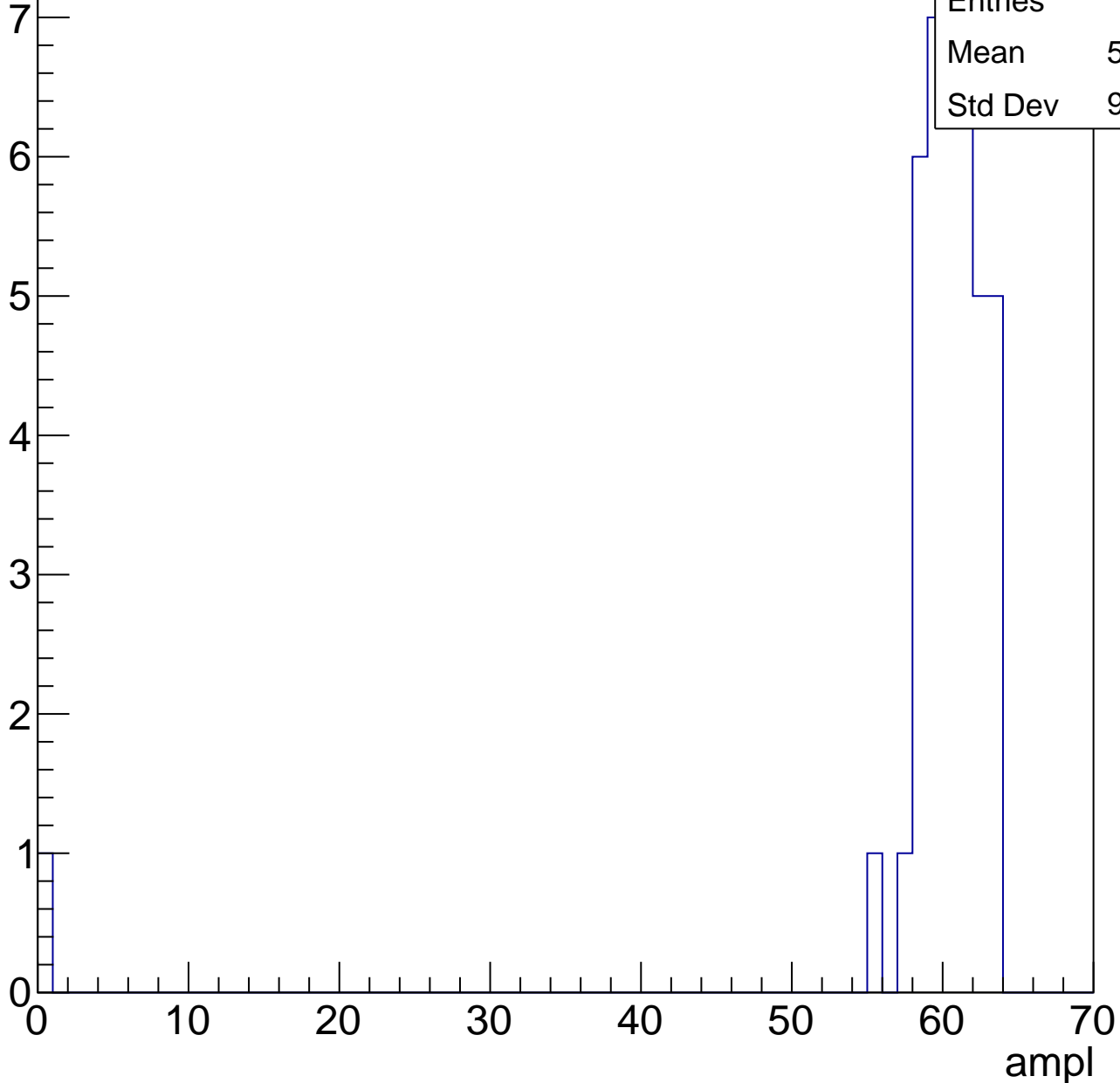


# B0L001S, U5-ch15, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	40
Mean	58.62
Std Dev	9.567



# B0L001S, U5-ch15, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch15, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L001S, U5-ch16, adc0

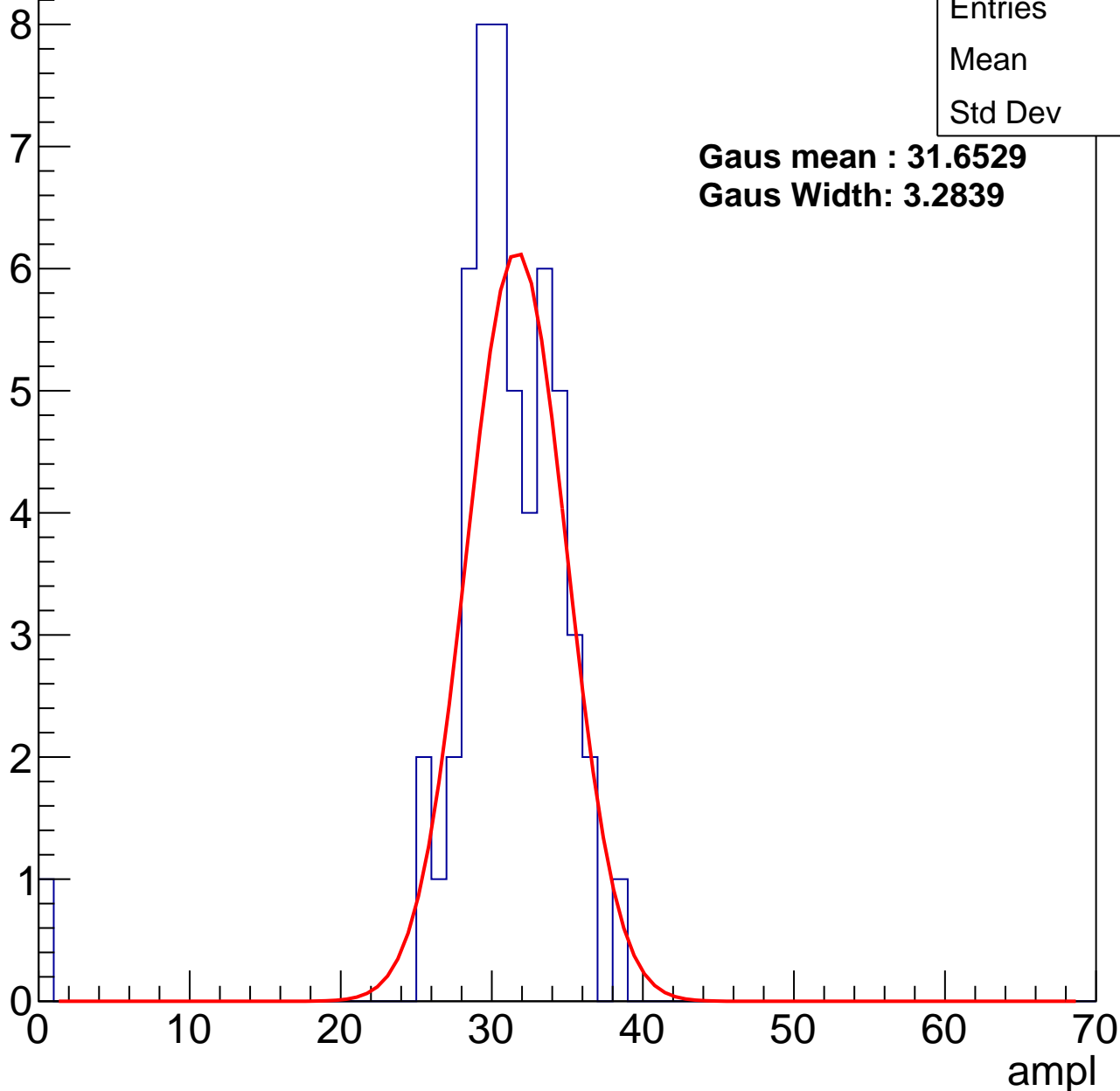
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	30.3
Std Dev	5.05

**Gaus mean : 31.6529**

**Gaus Width: 3.2839**



# B0L001S, U5-ch16, adc1

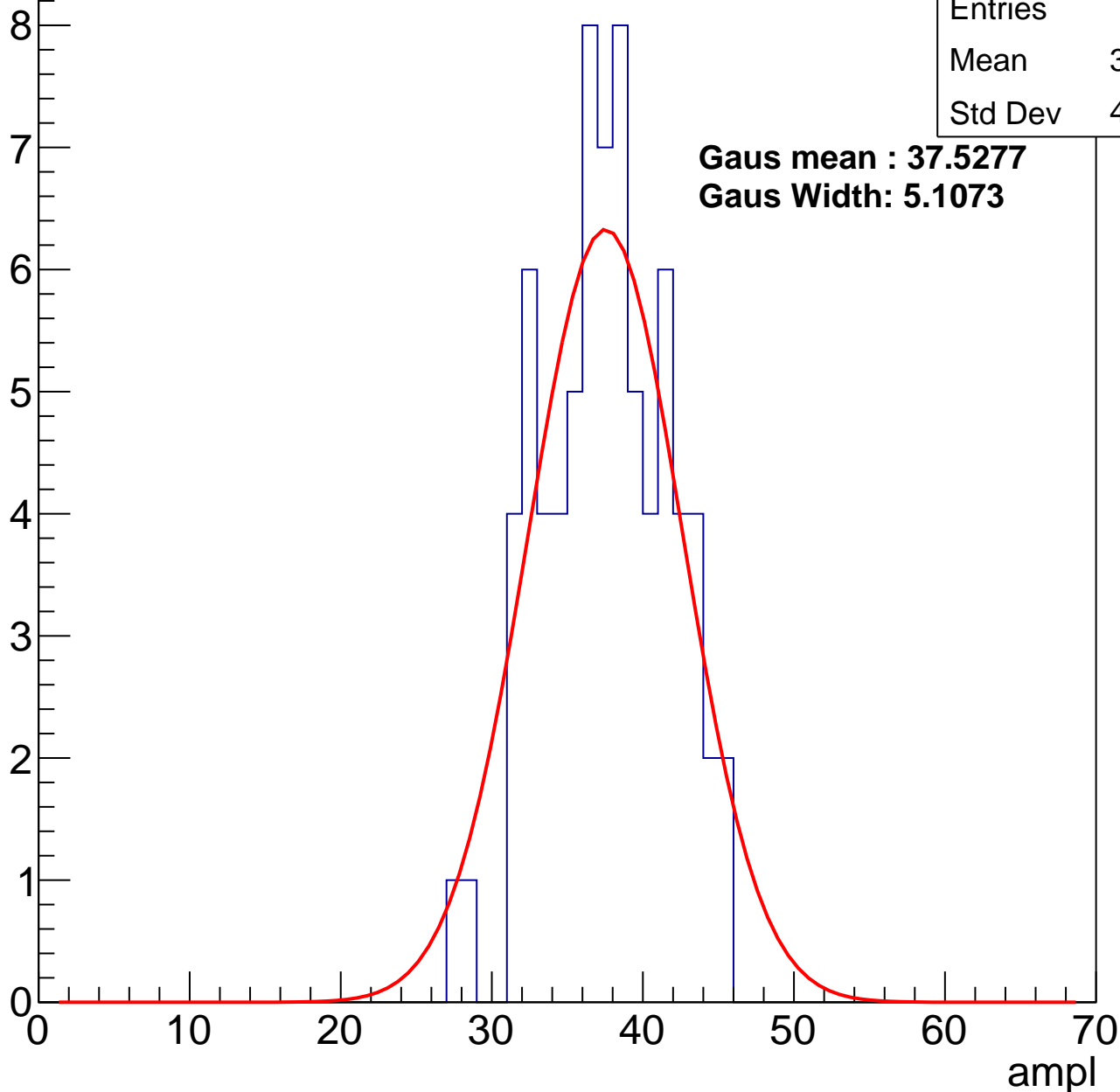
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	75
Mean	37.12
Std Dev	4.053

**Gaus mean : 37.5277**

**Gaus Width: 5.1073**



# B0L001S, U5-ch16, adc2

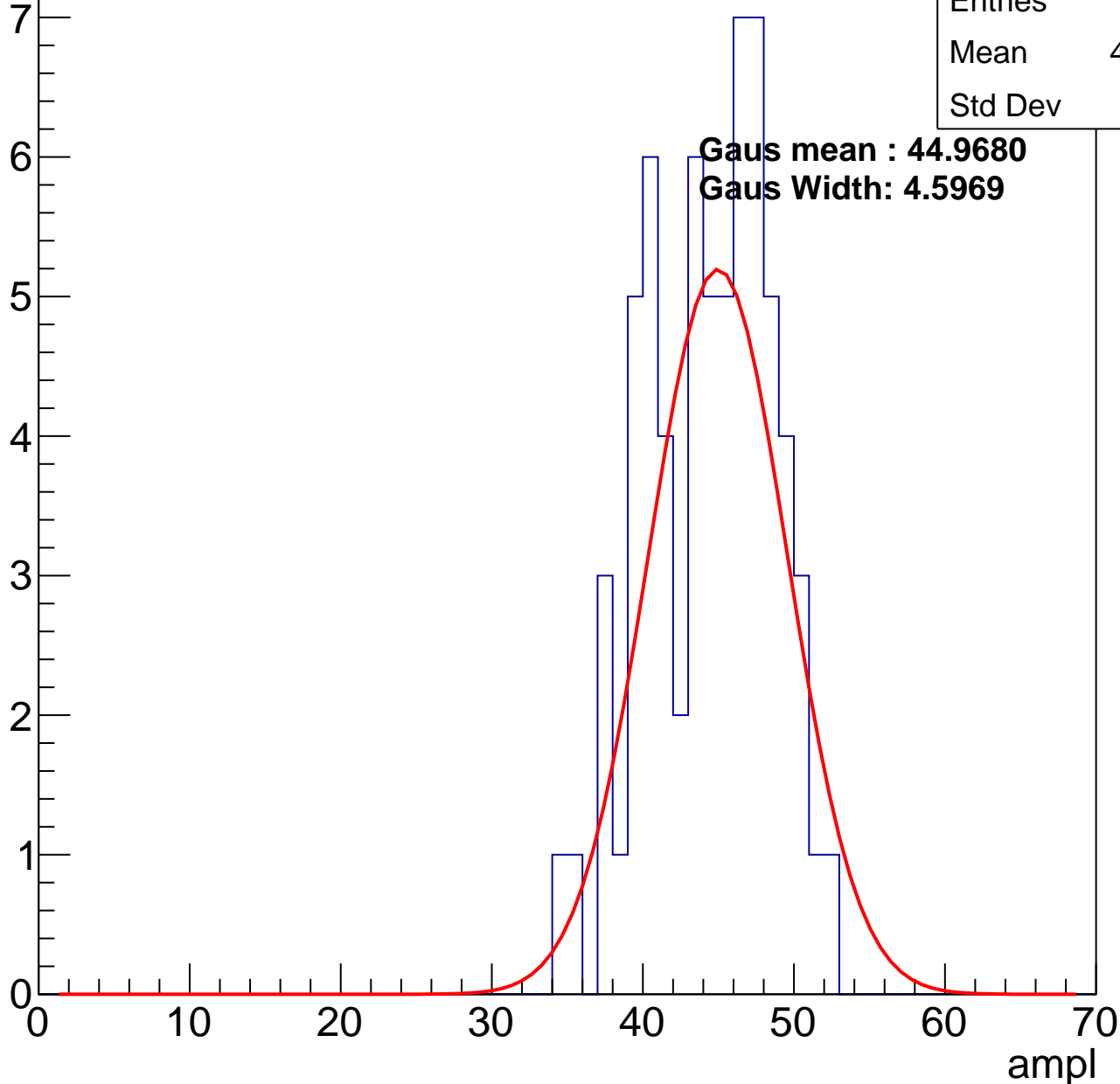
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	43.94
Std Dev	4.11

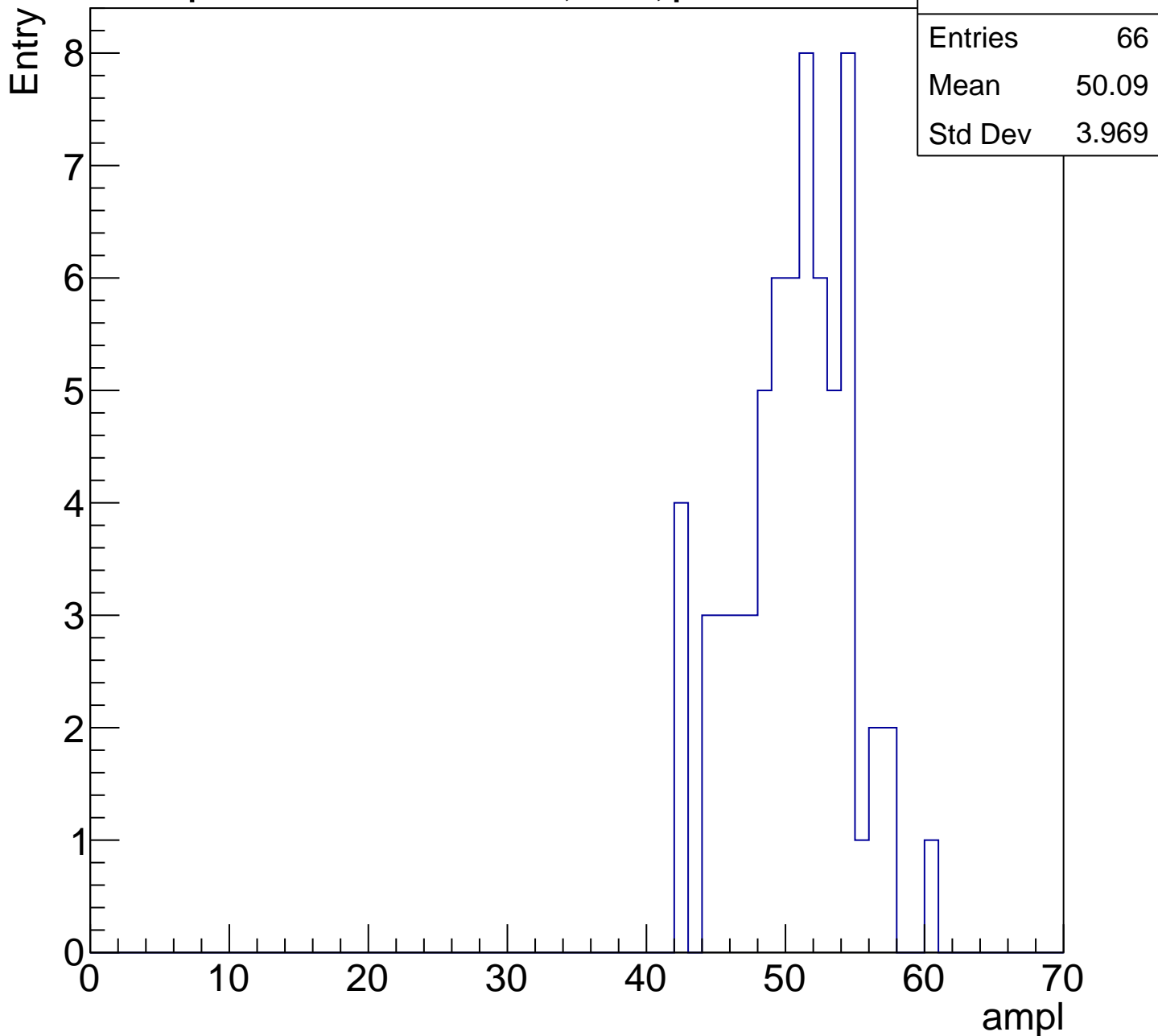
**Gaus mean : 44.9680**

**Gaus Width: 4.5969**



# B0L001S, U5-ch16, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

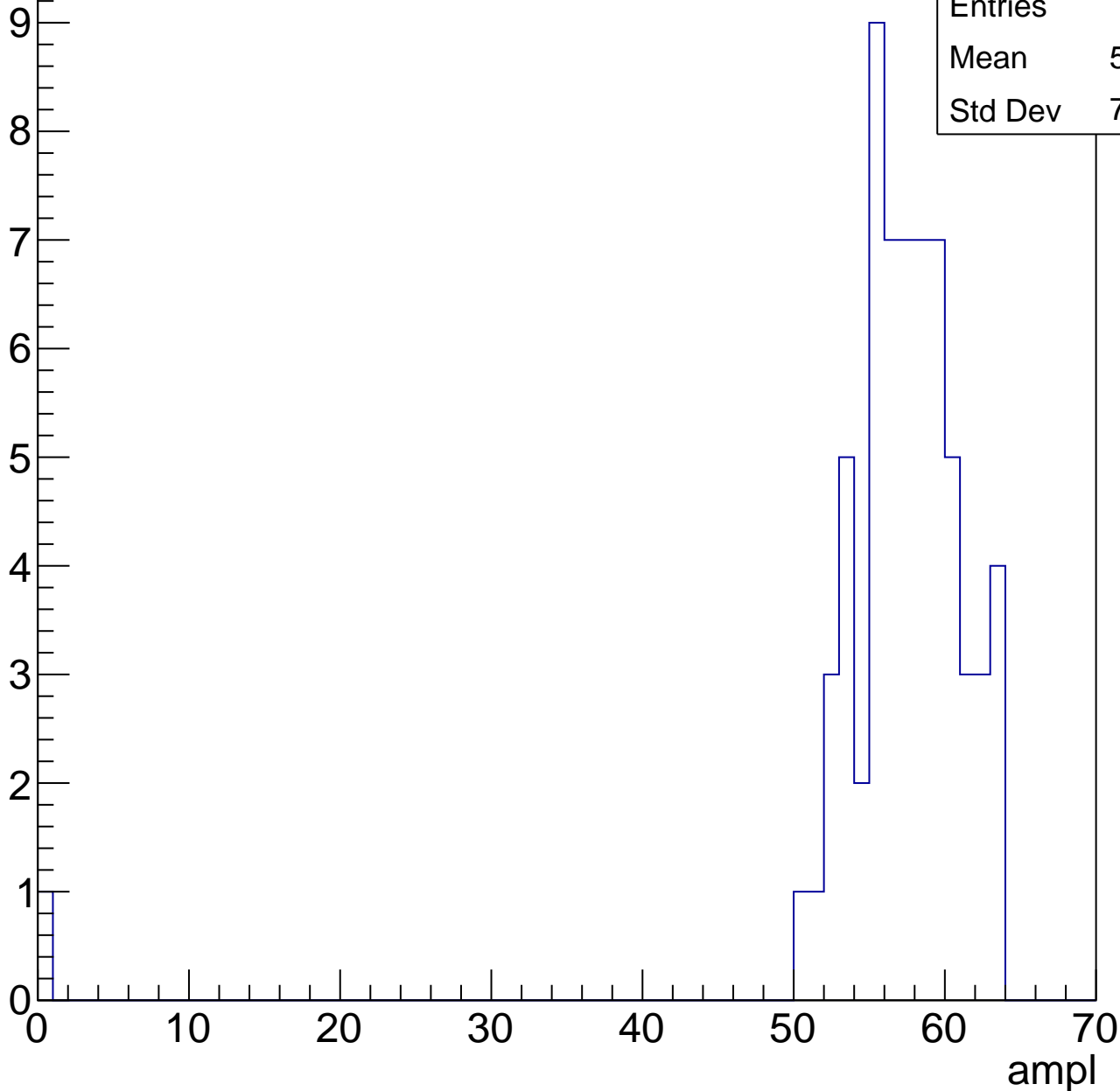


# B0L001S, U5-ch16, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	56.25
Std Dev	7.706

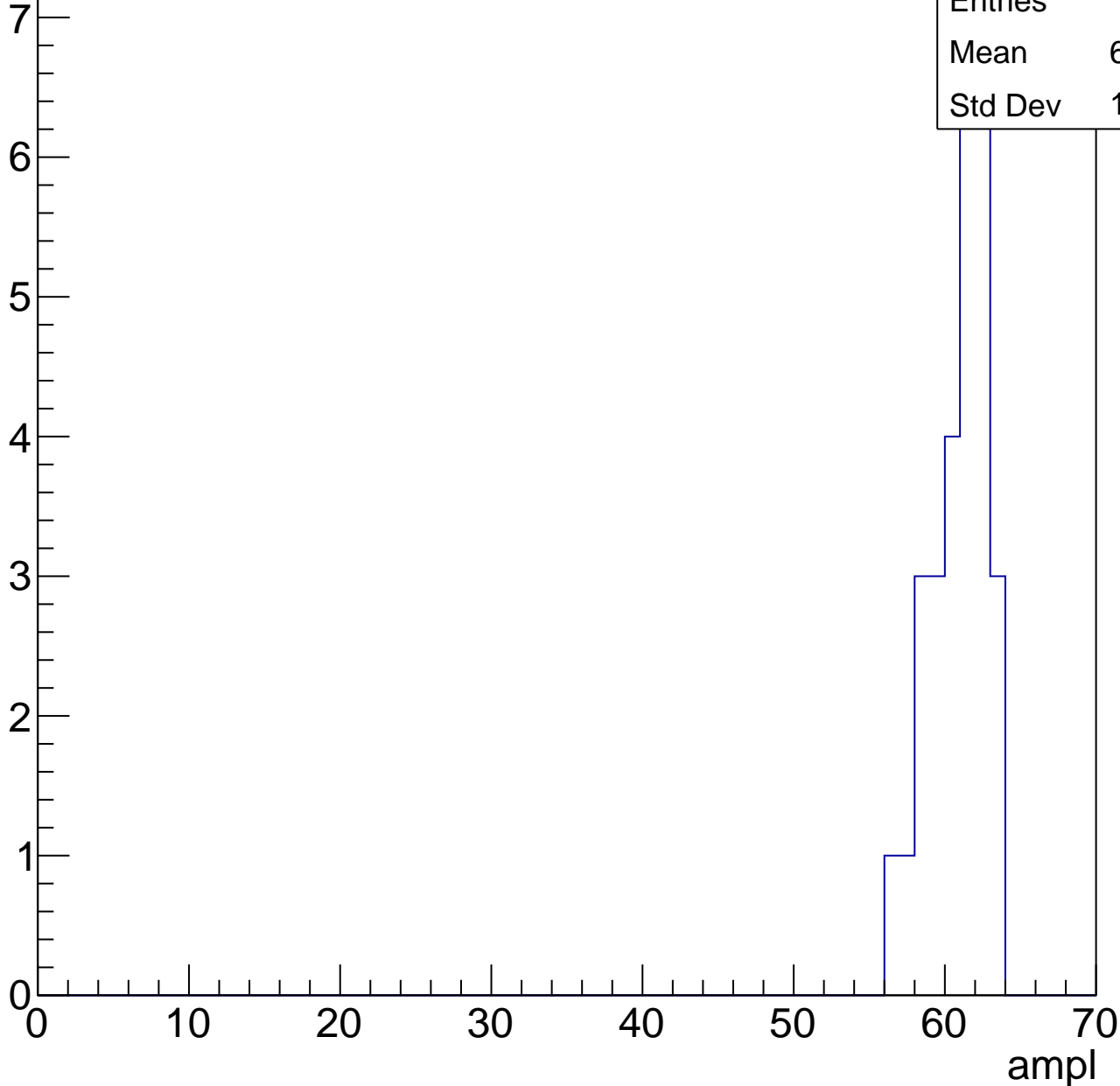


# B0L001S, U5-ch16, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

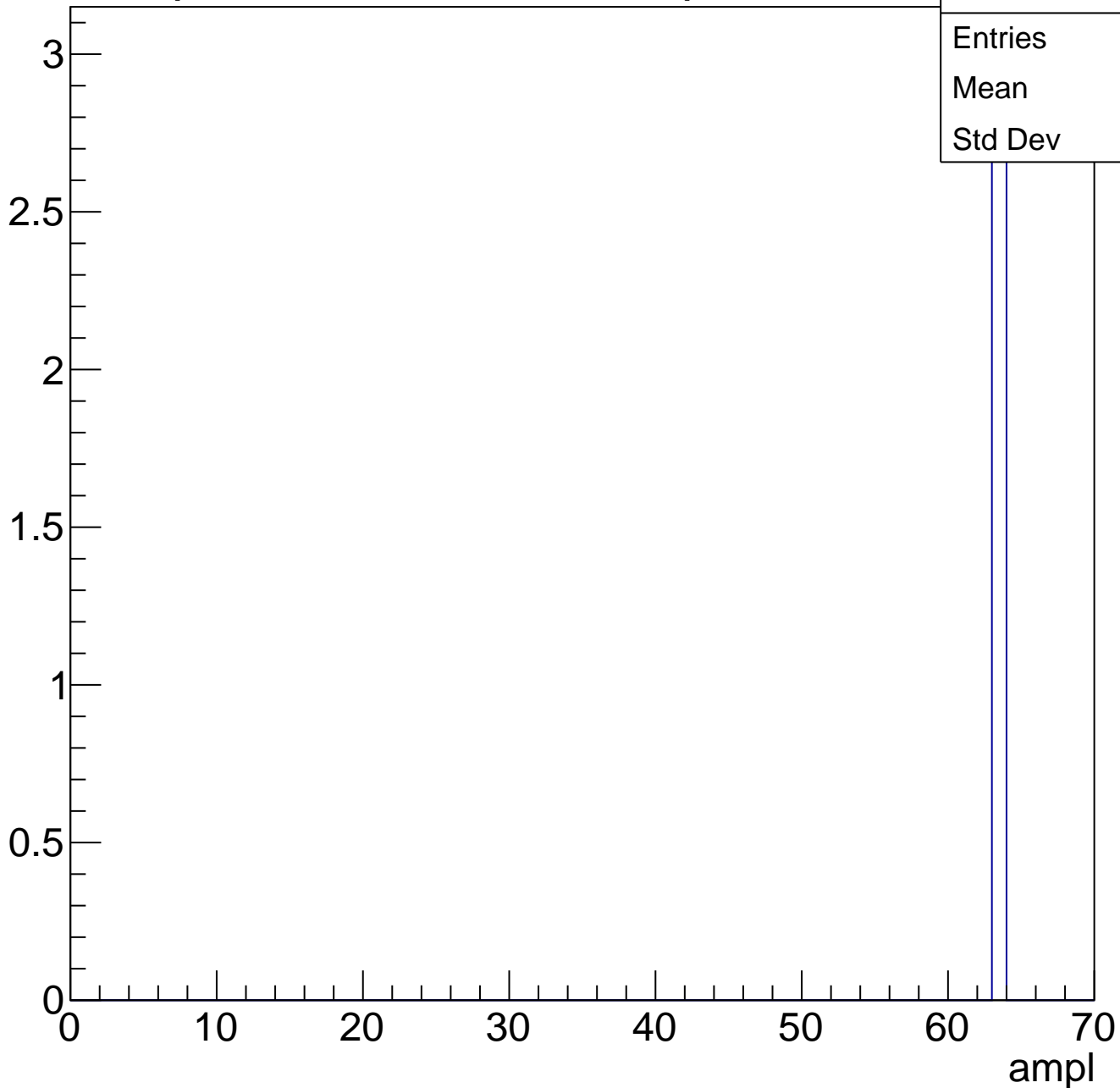
Entries	29
Mean	60.48
Std Dev	1.812



# B0L001S, U5-ch16, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch16, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch17, adc0

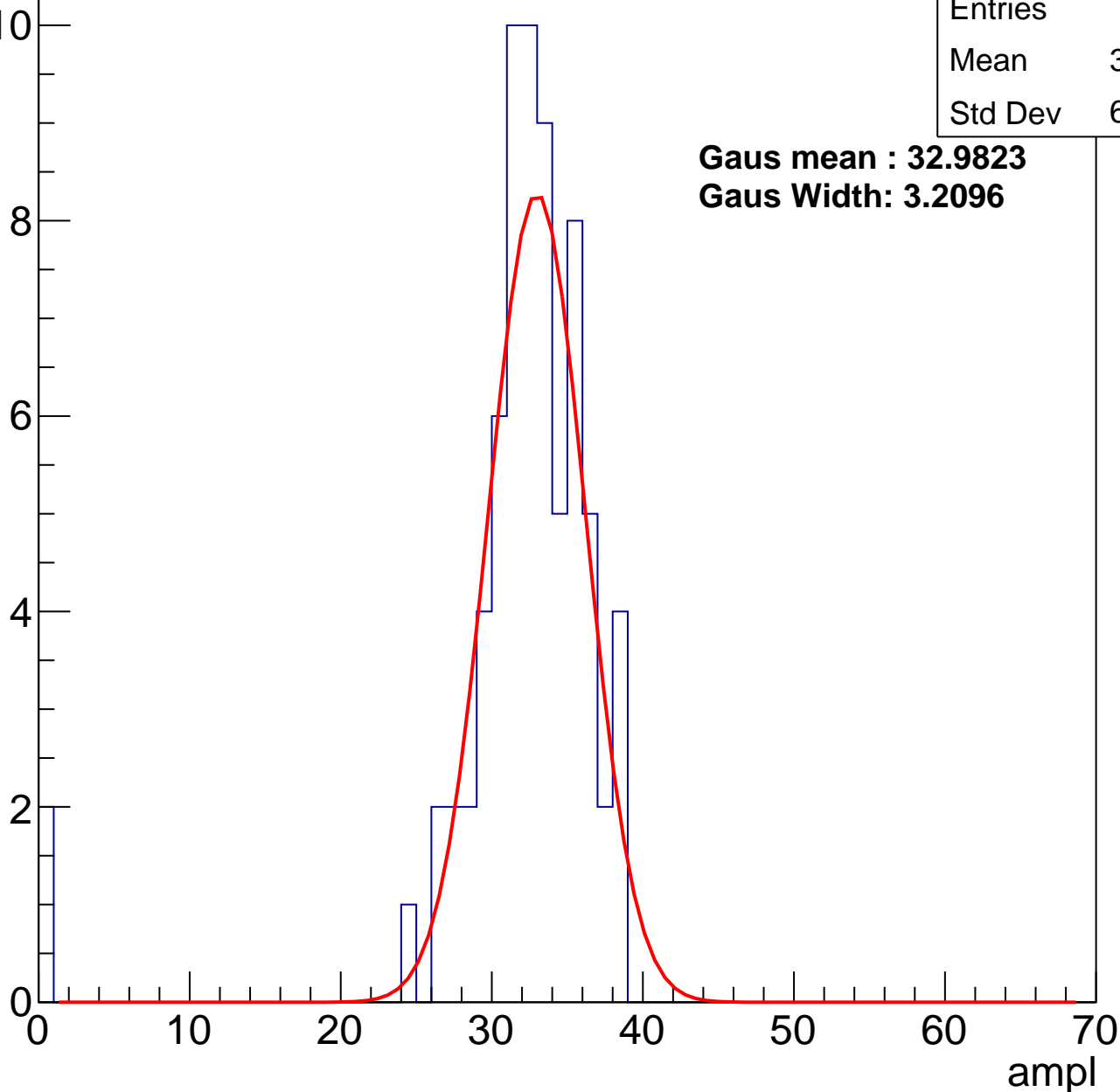
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	31.46
Std Dev	6.112

**Gaus mean : 32.9823**

**Gaus Width: 3.2096**



# B0L001S, U5-ch17, adc1

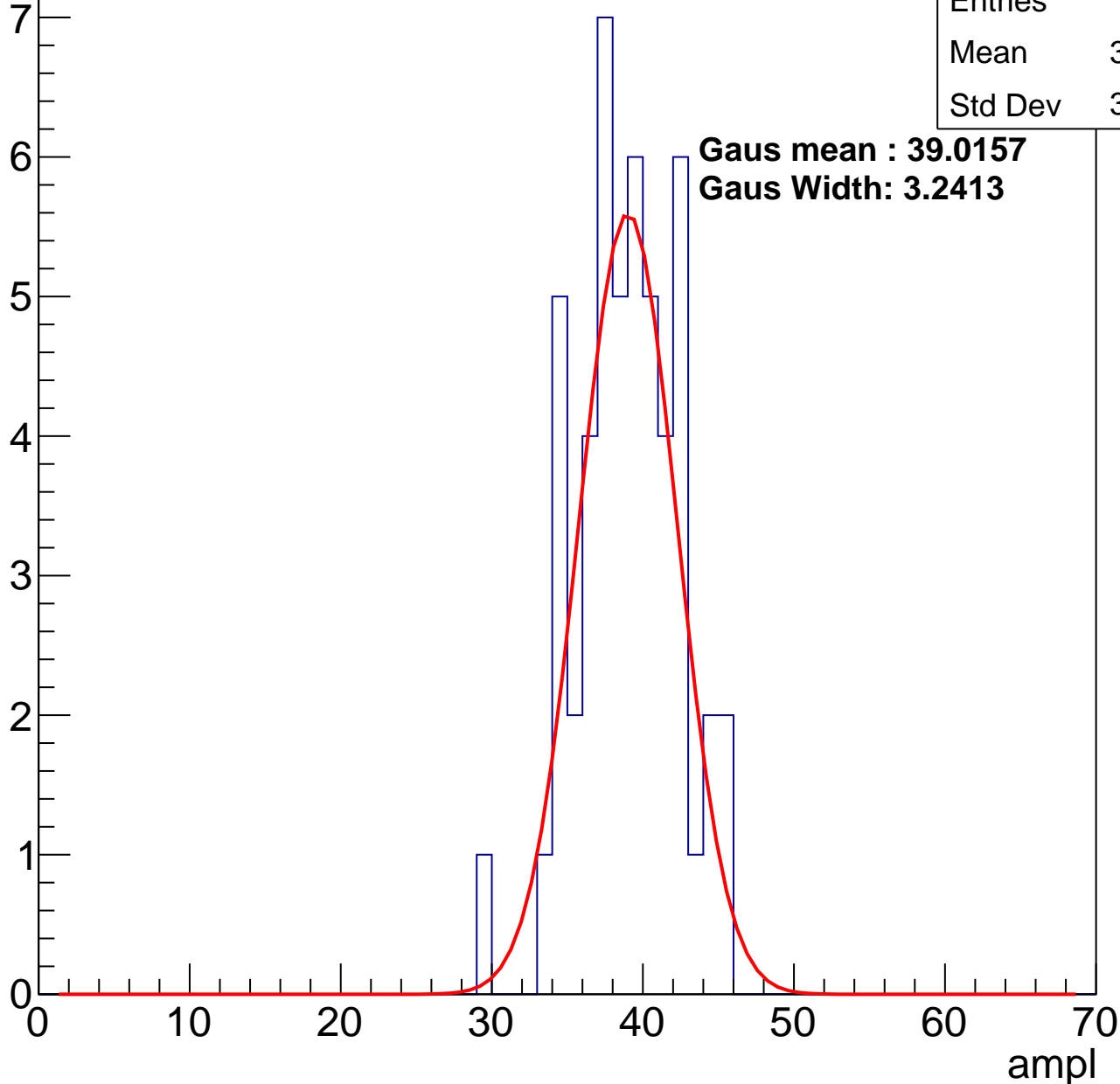
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	51
Mean	38.55
Std Dev	3.327

**Gaus mean : 39.0157**

**Gaus Width: 3.2413**



# B0L001S, U5-ch17, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	70
Mean	43.97
Std Dev	3.304

**Gaus mean : 44.5832**

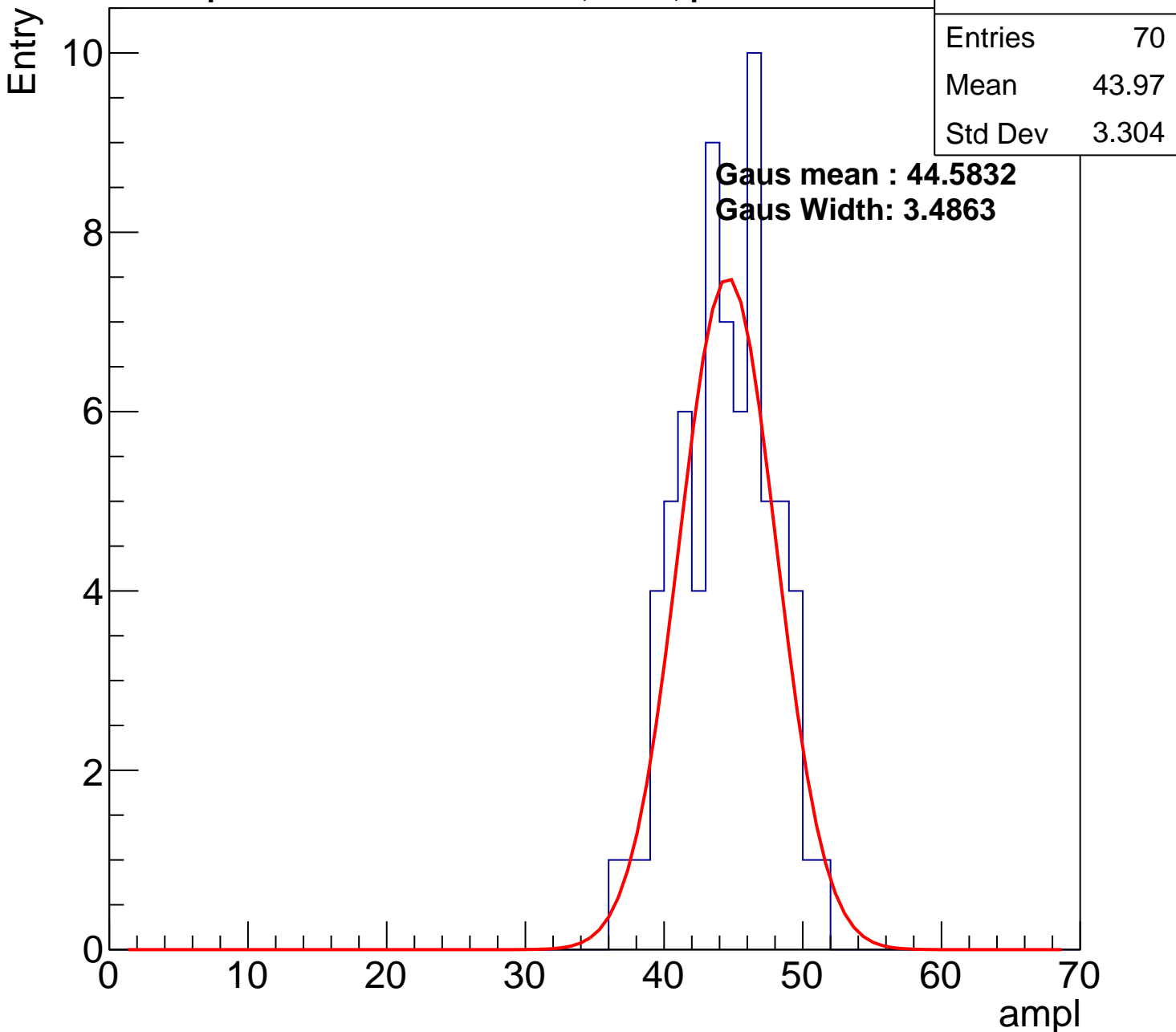
**Gaus Width: 3.4863**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

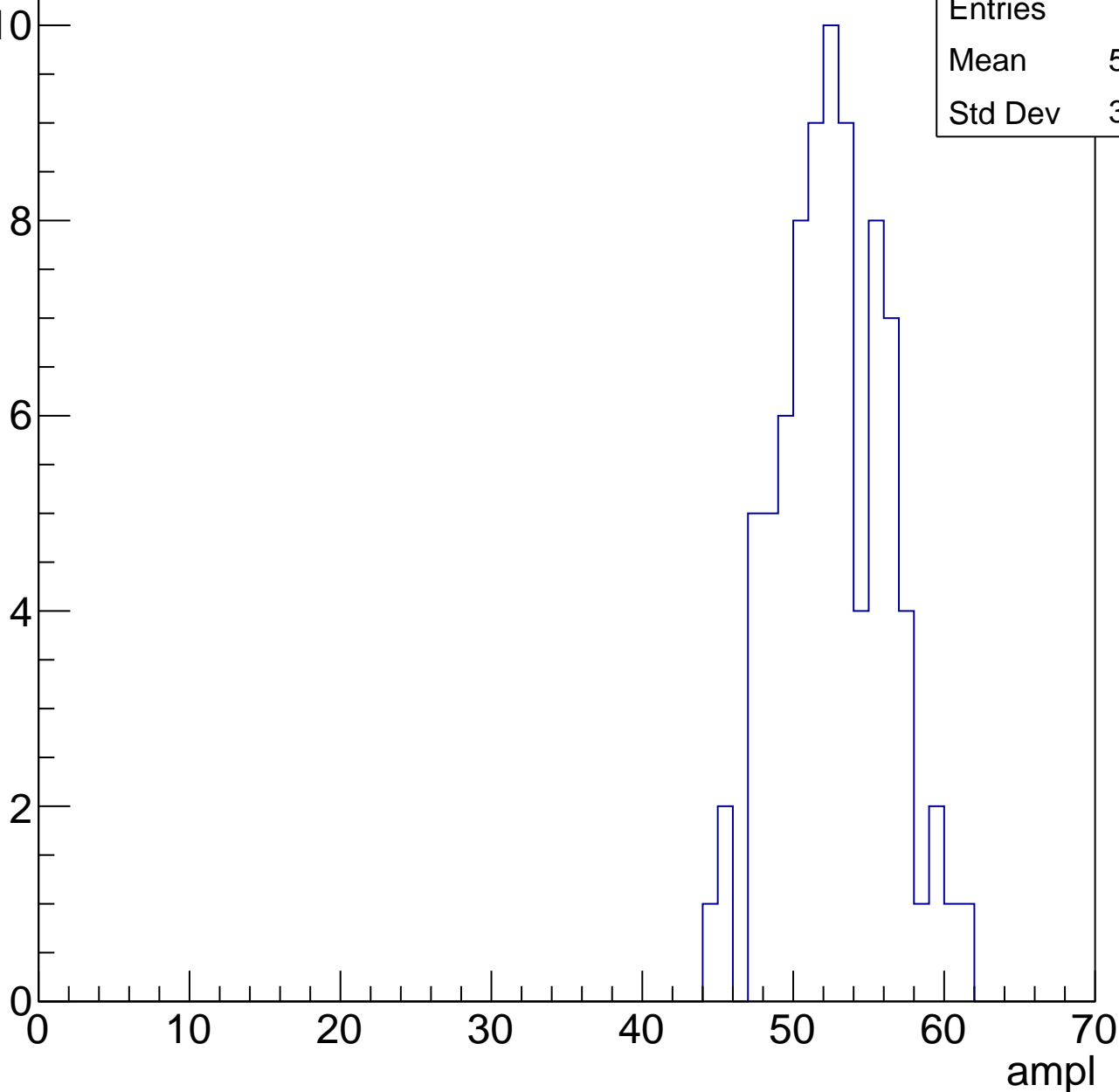


# B0L001S, U5-ch17, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	83
Mean	52.19
Std Dev	3.552

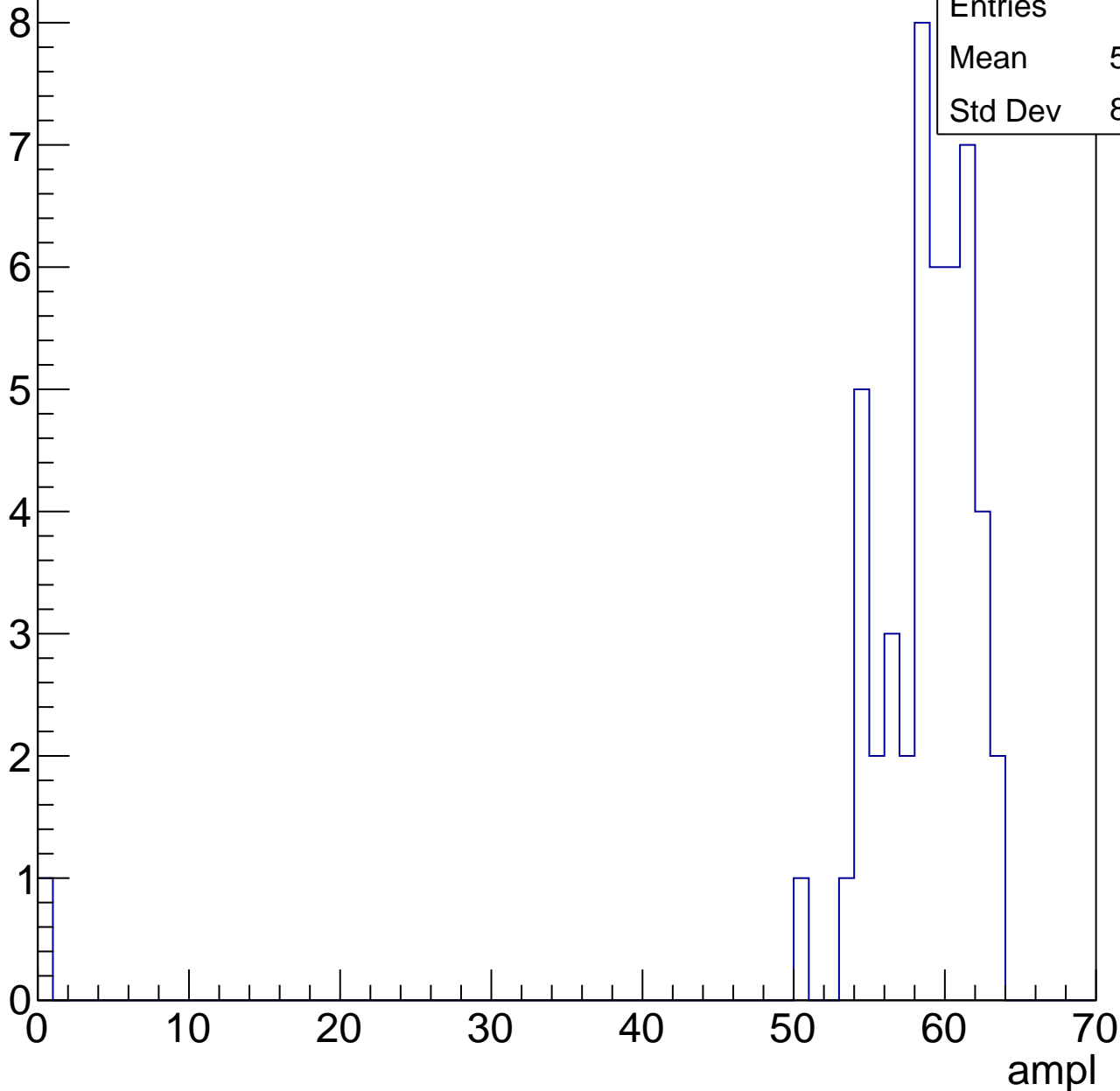


# B0L001S, U5-ch17, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	48
Mean	57.17
Std Dev	8.825

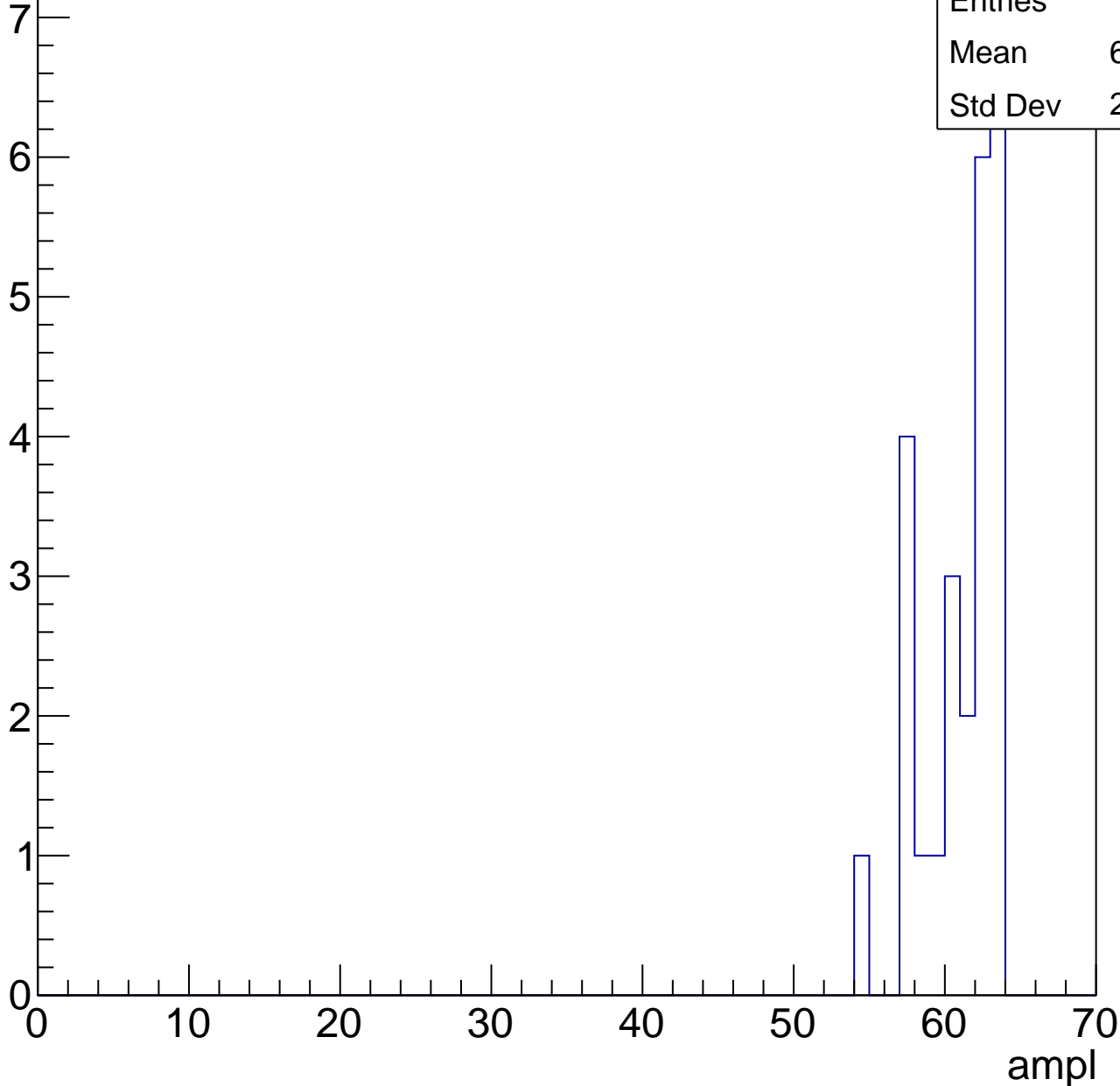


# B0L001S, U5-ch17, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	25
Mean	60.56
Std Dev	2.515



# B0L001S, U5-ch17, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch17, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch18, adc0

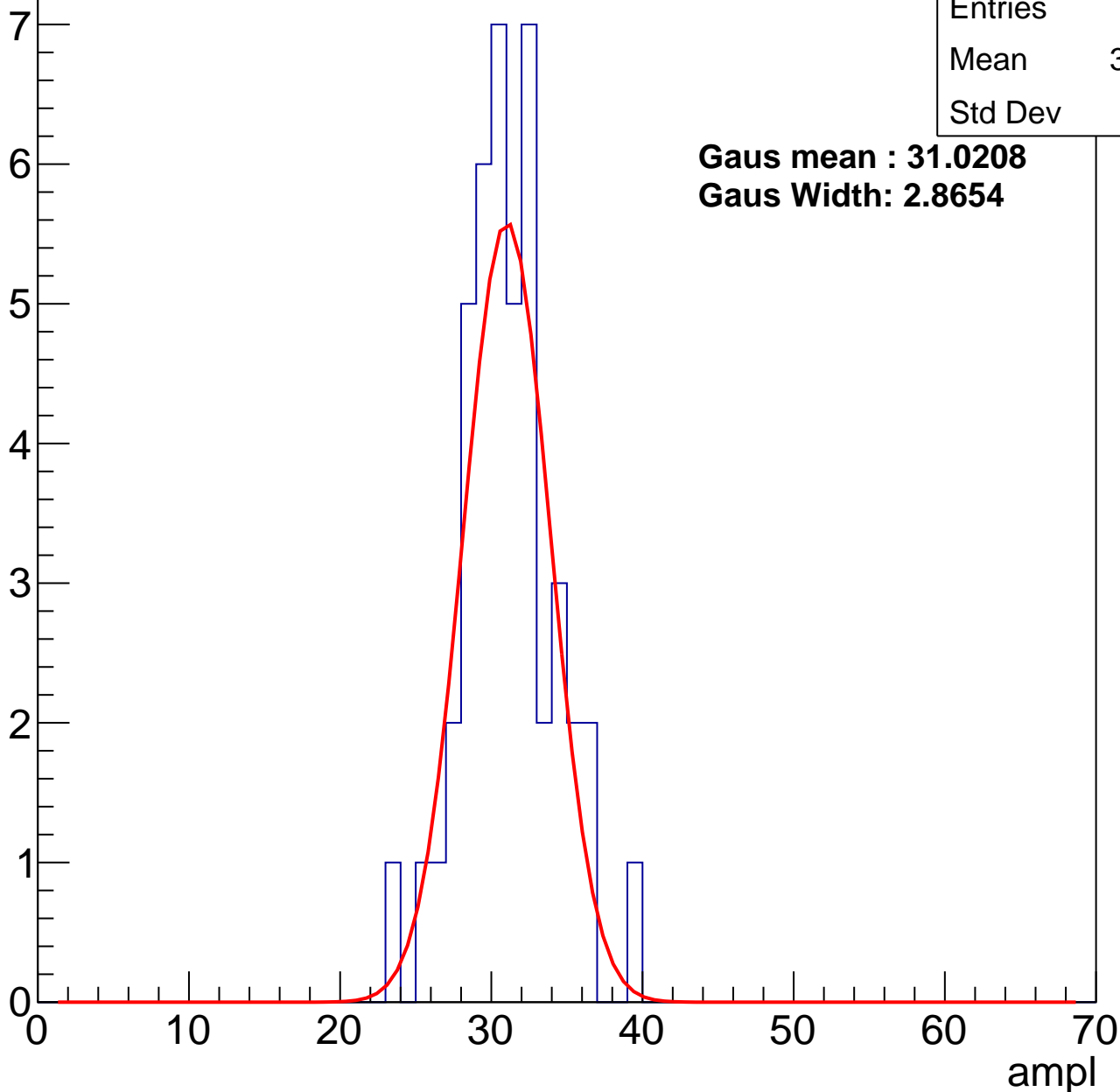
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	45
Mean	30.67
Std Dev	3.04

**Gaus mean : 31.0208**

**Gaus Width: 2.8654**



# B0L001S, U5-ch18, adc1

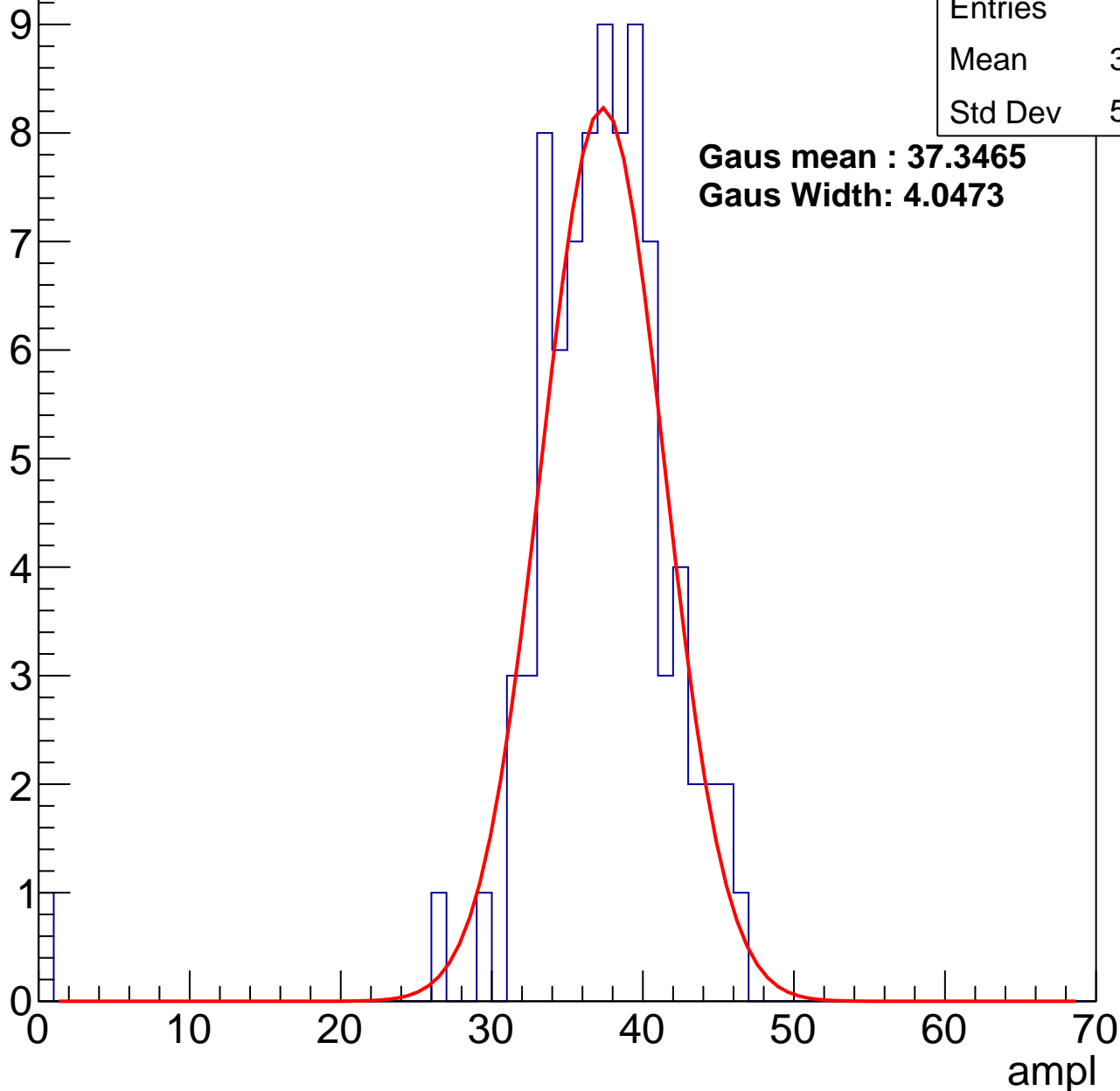
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	85
Mean	36.64
Std Dev	5.507

**Gaus mean : 37.3465**

**Gaus Width: 4.0473**

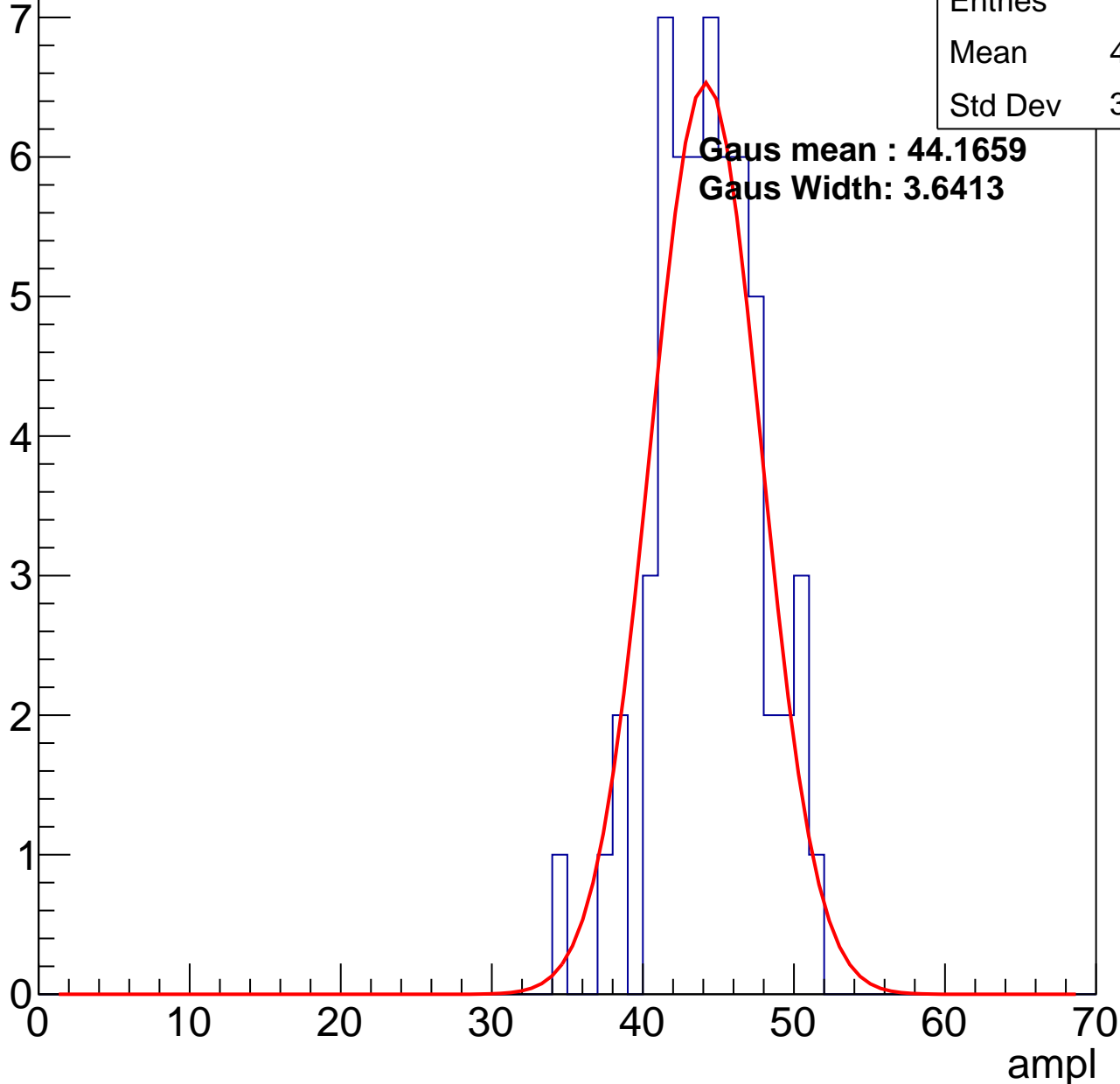


# B0L001S, U5-ch18, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

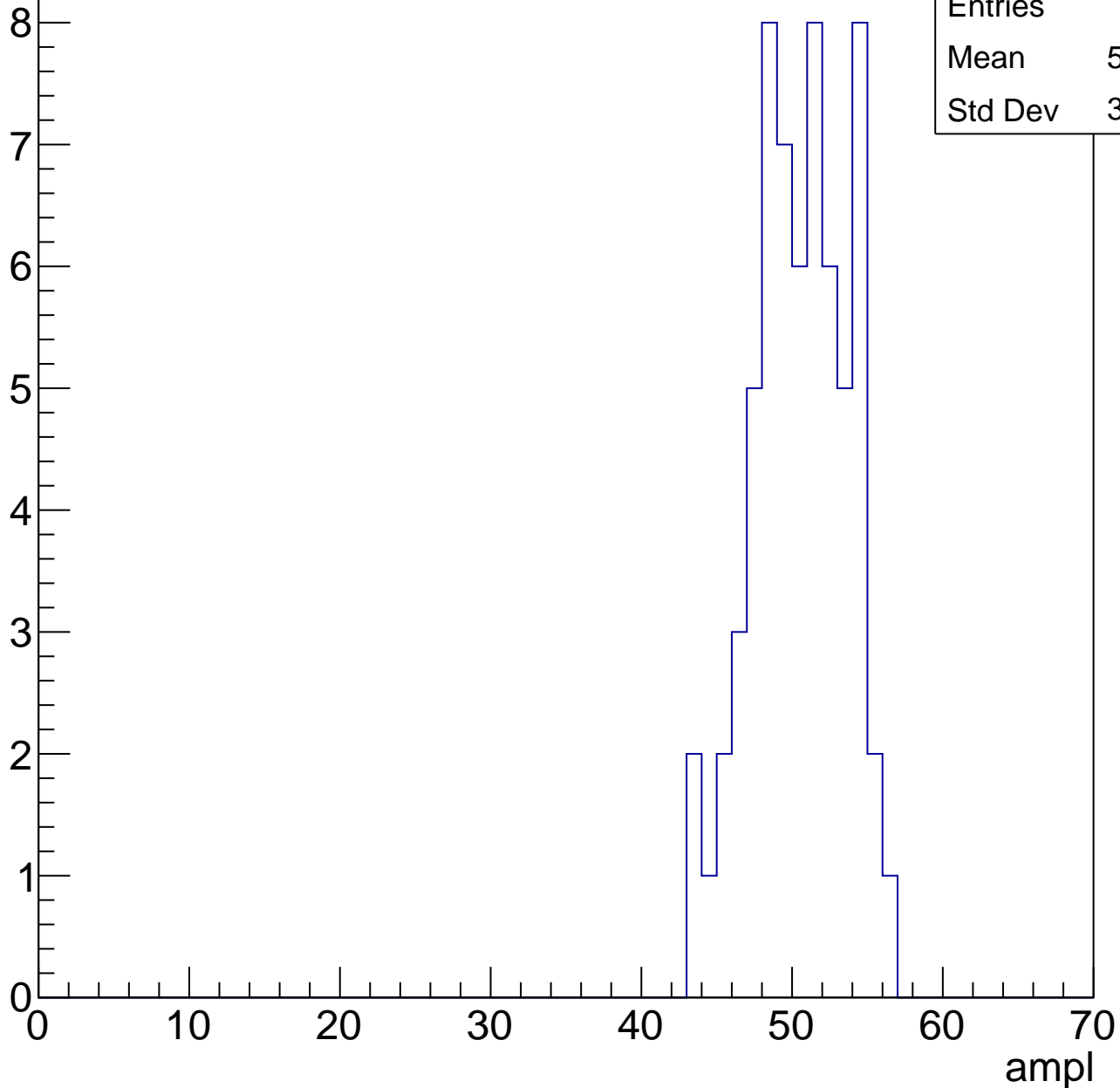
Entries	58
Mean	43.93
Std Dev	3.413



# B0L001S, U5-ch18, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



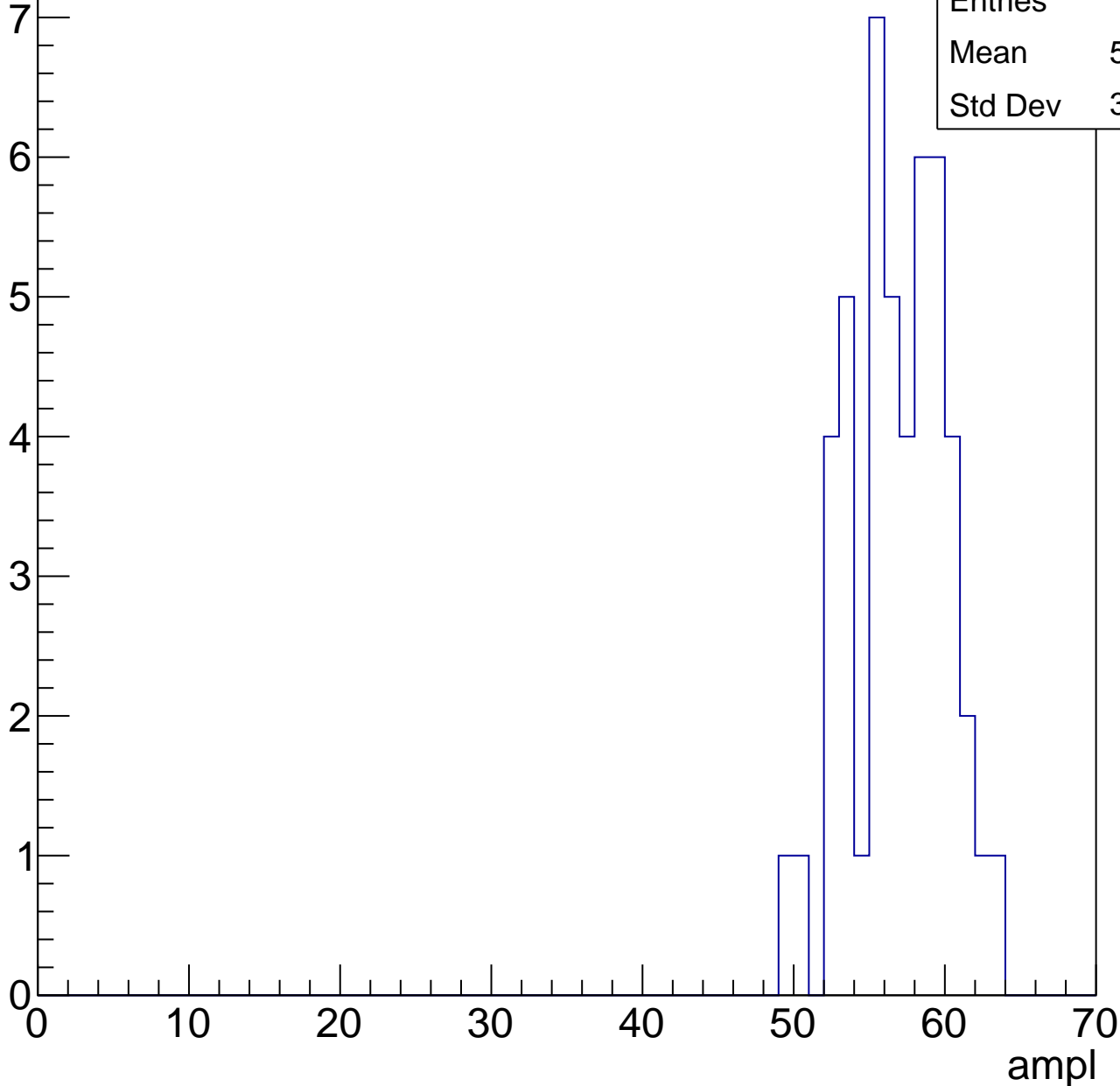
Entries	64
Mean	50.05
Std Dev	3.079

# B0L001S, U5-ch18, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	48
Mean	56.42
Std Dev	3.155

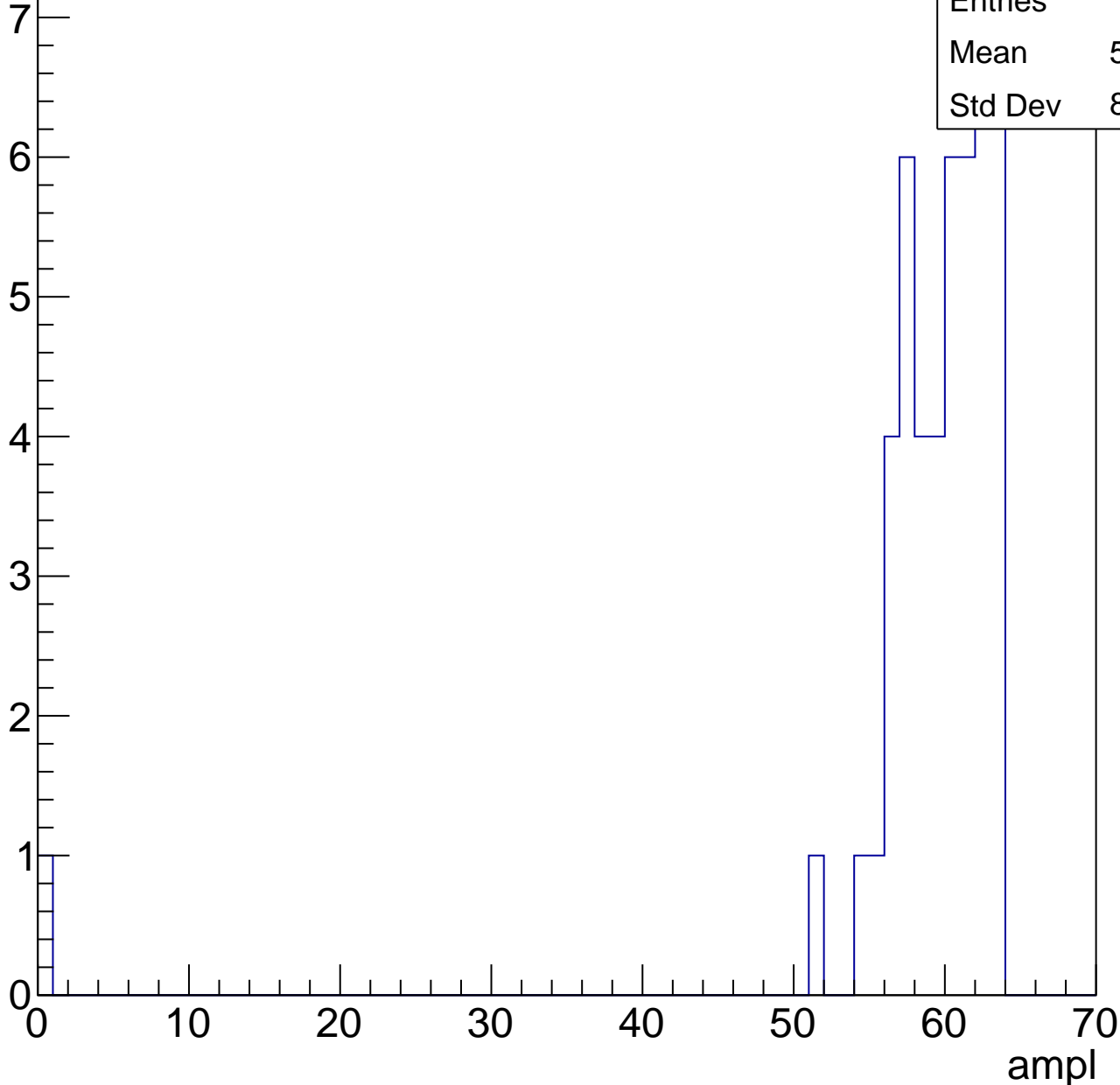


# B0L001S, U5-ch18, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	48
Mean	58.23
Std Dev	8.929



# B0L001S, U5-ch18, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	62
Std Dev	0.8165

ampl



# B0L001S, U5-ch18, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	3
Mean	0
Std Dev	0

# B0L001S, U5-ch19, adc0

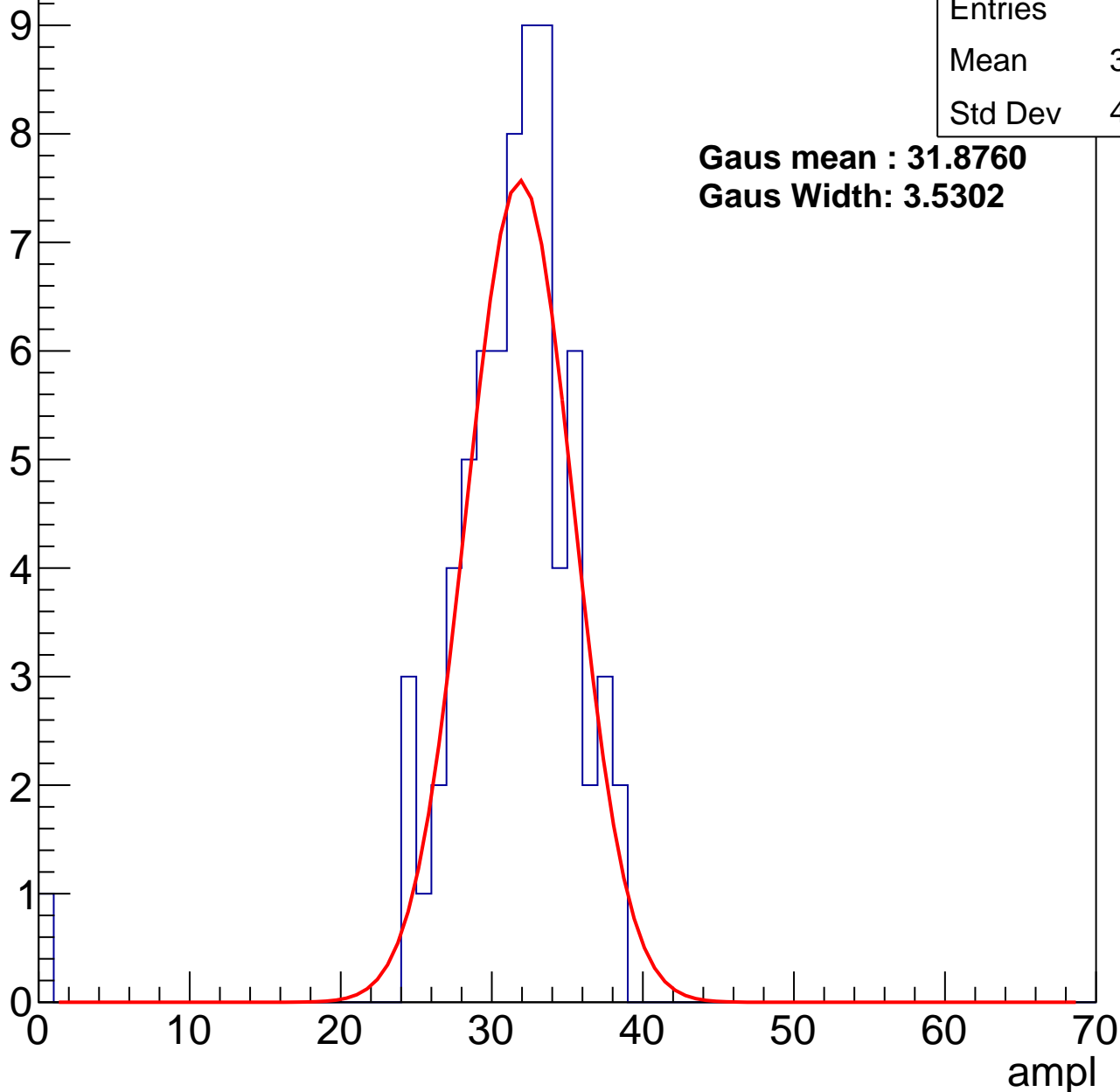
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	30.83
Std Dev	4.984

**Gaus mean : 31.8760**

**Gaus Width: 3.5302**



# B0L001S, U5-ch19, adc1

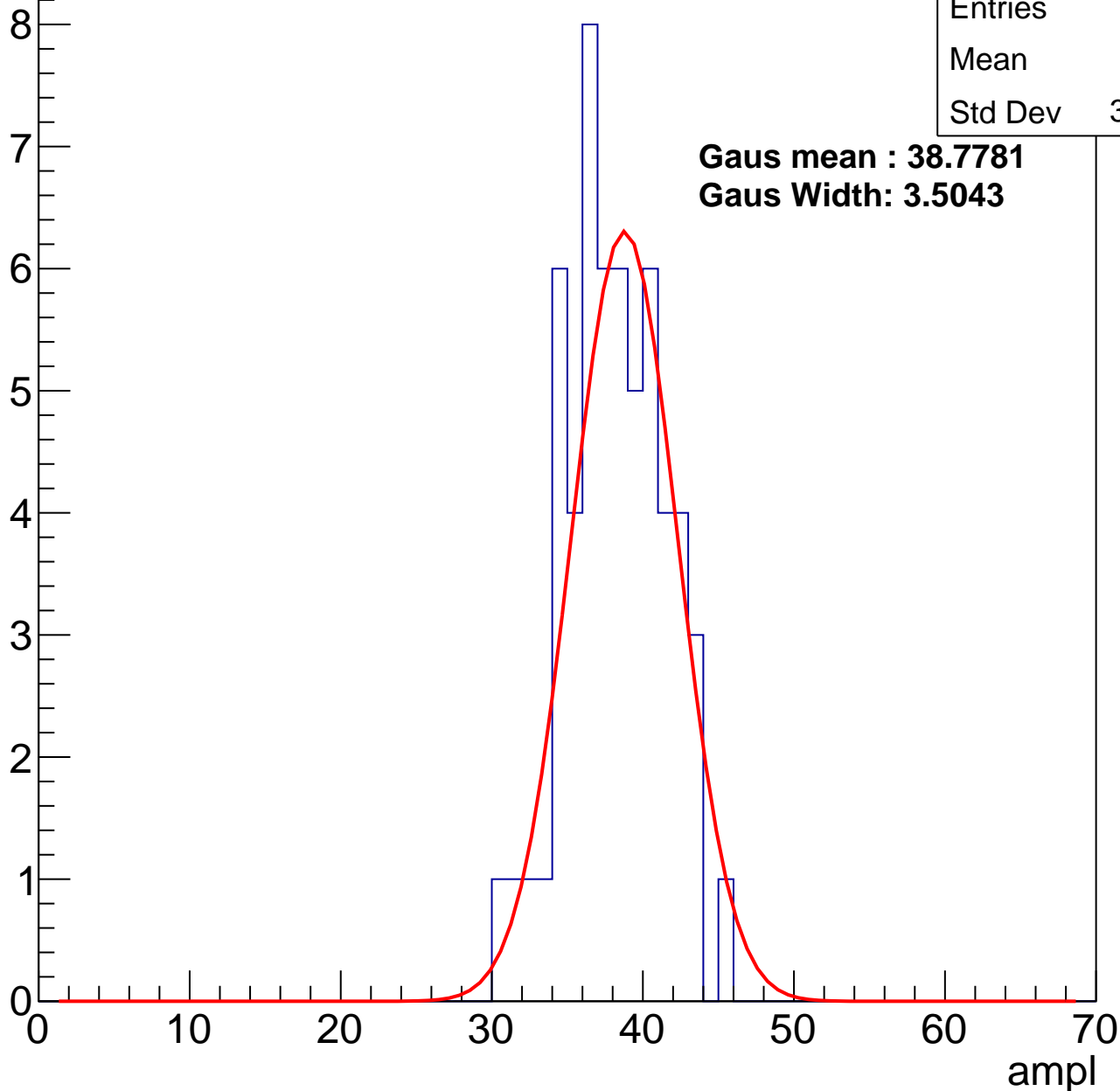
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	37.7
Std Dev	3.223

**Gaus mean : 38.7781**

**Gaus Width: 3.5043**



# B0L001S, U5-ch19, adc2

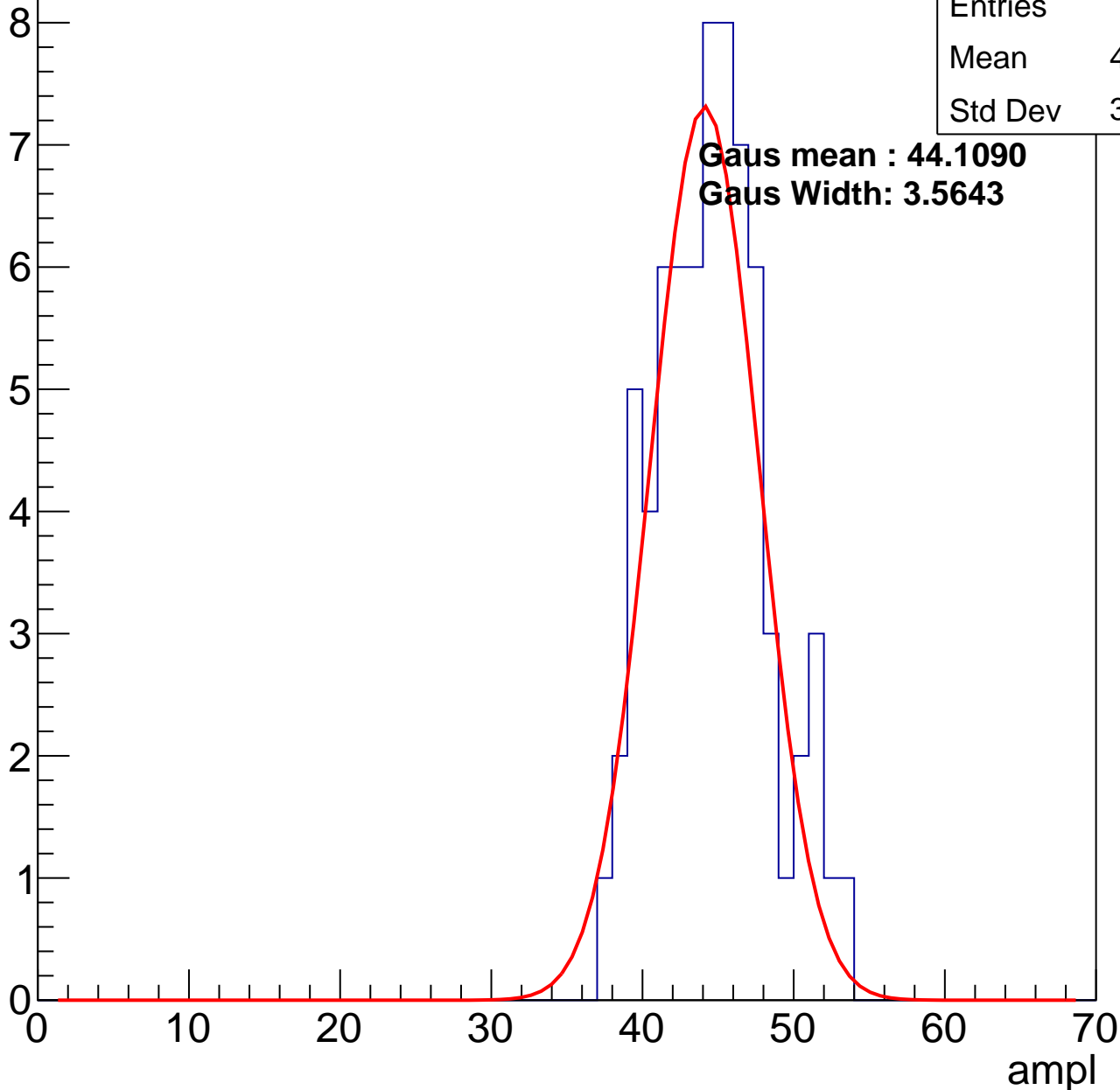
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	44.16
Std Dev	3.624

**Gaus mean : 44.1090**

**Gaus Width: 3.5643**

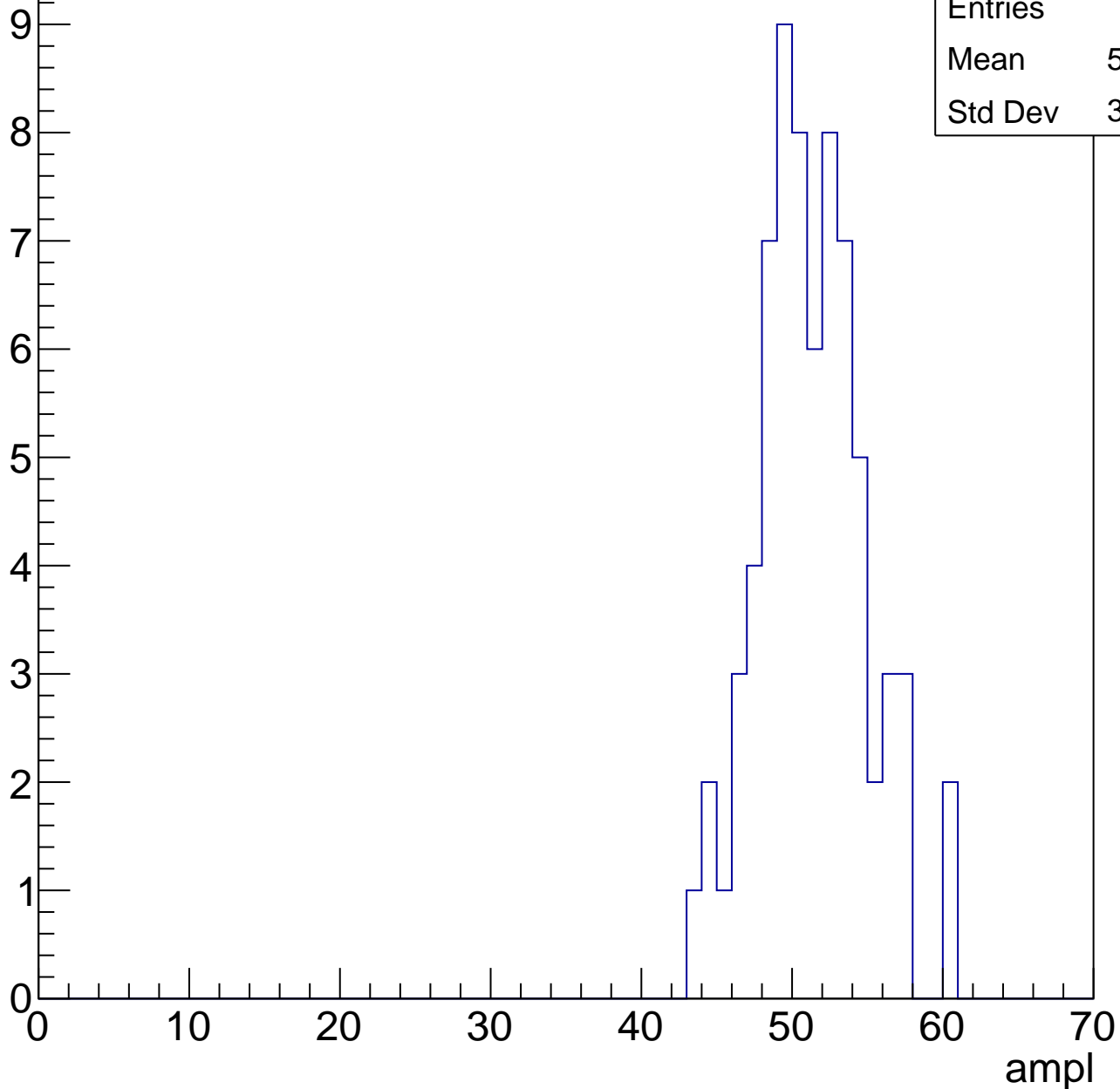


# B0L001S, U5-ch19, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

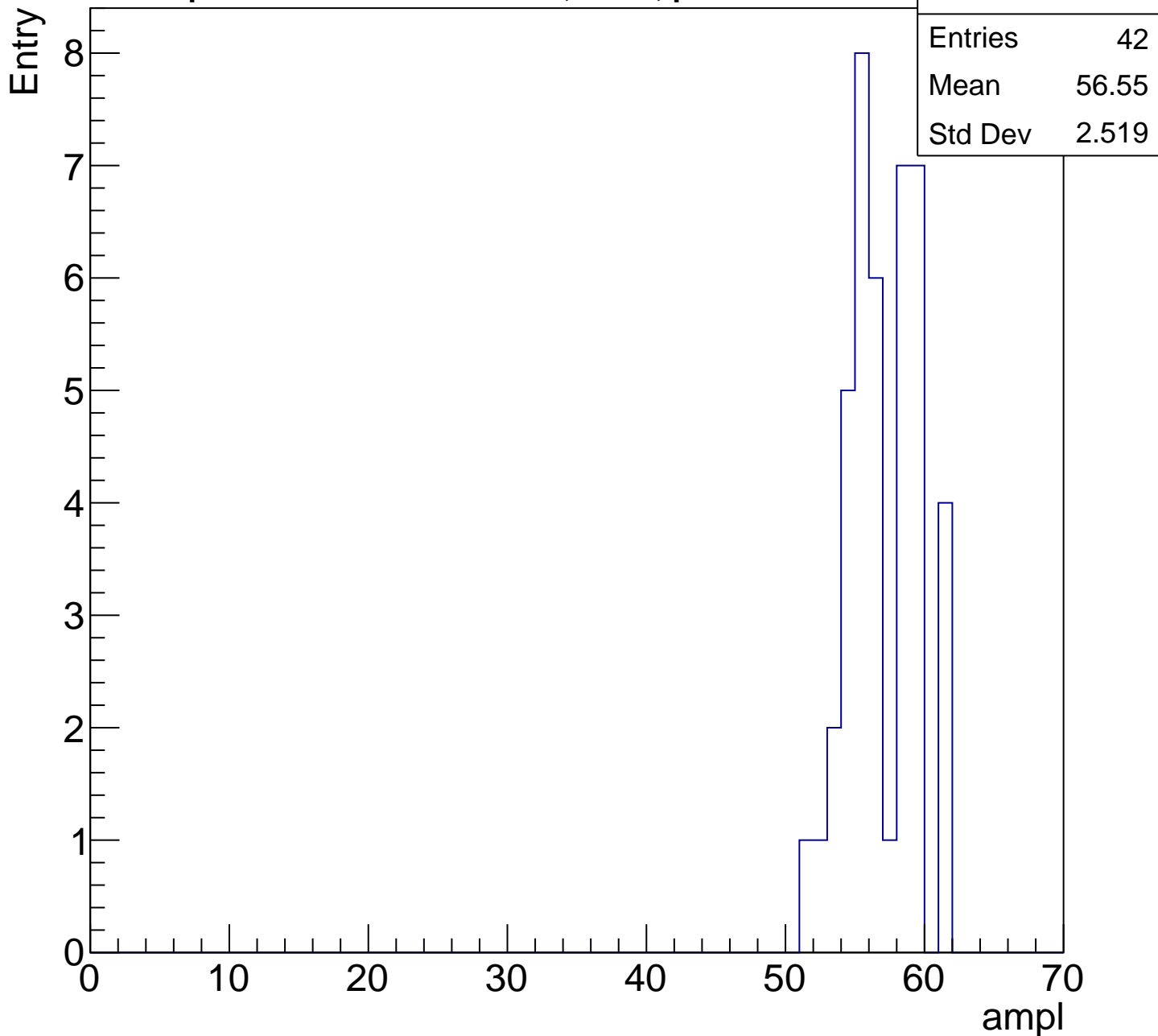
Entry

Entries	71
Mean	50.86
Std Dev	3.562



# B0L001S, U5-ch19, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

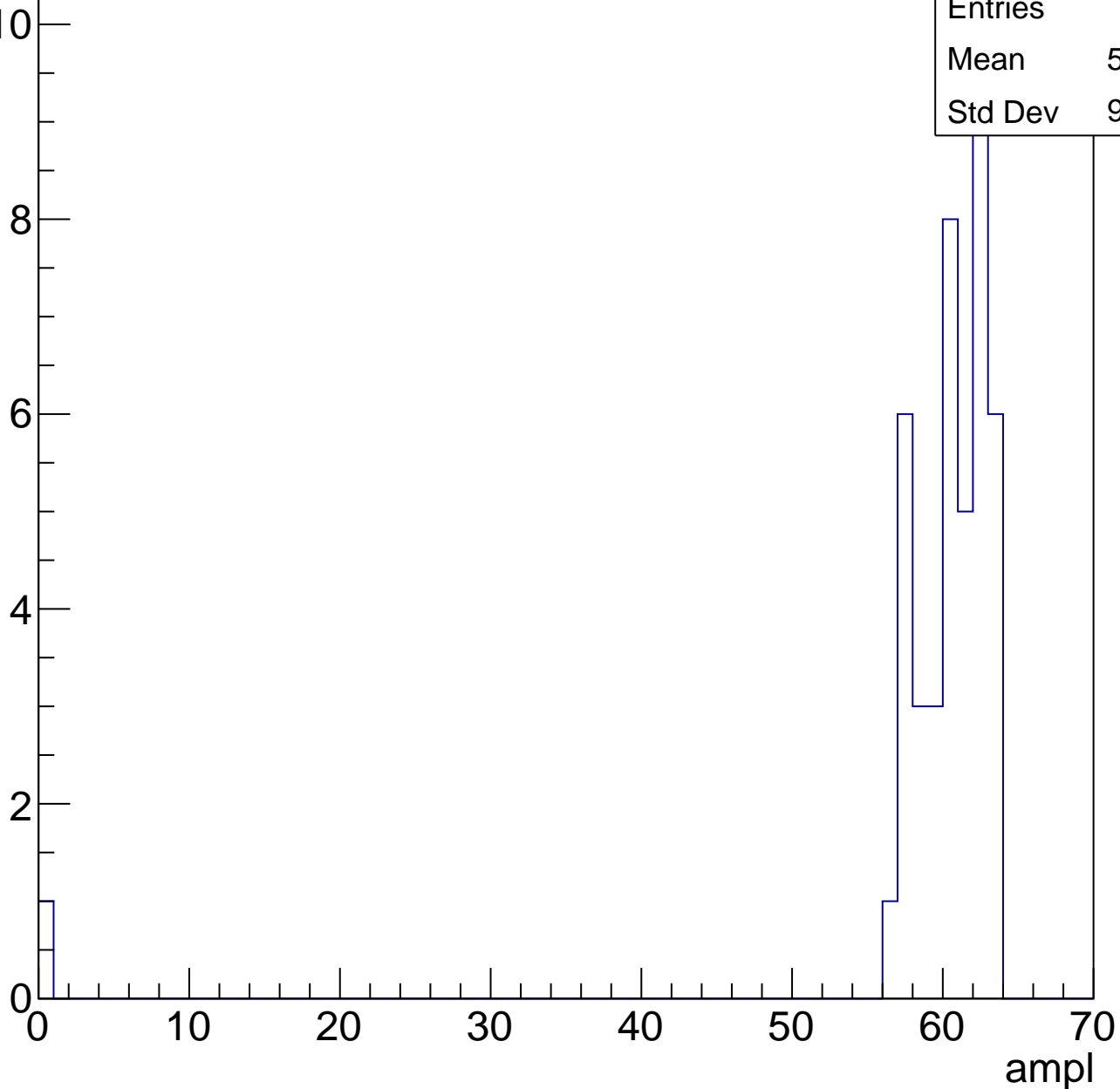


# B0L001S, U5-ch19, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

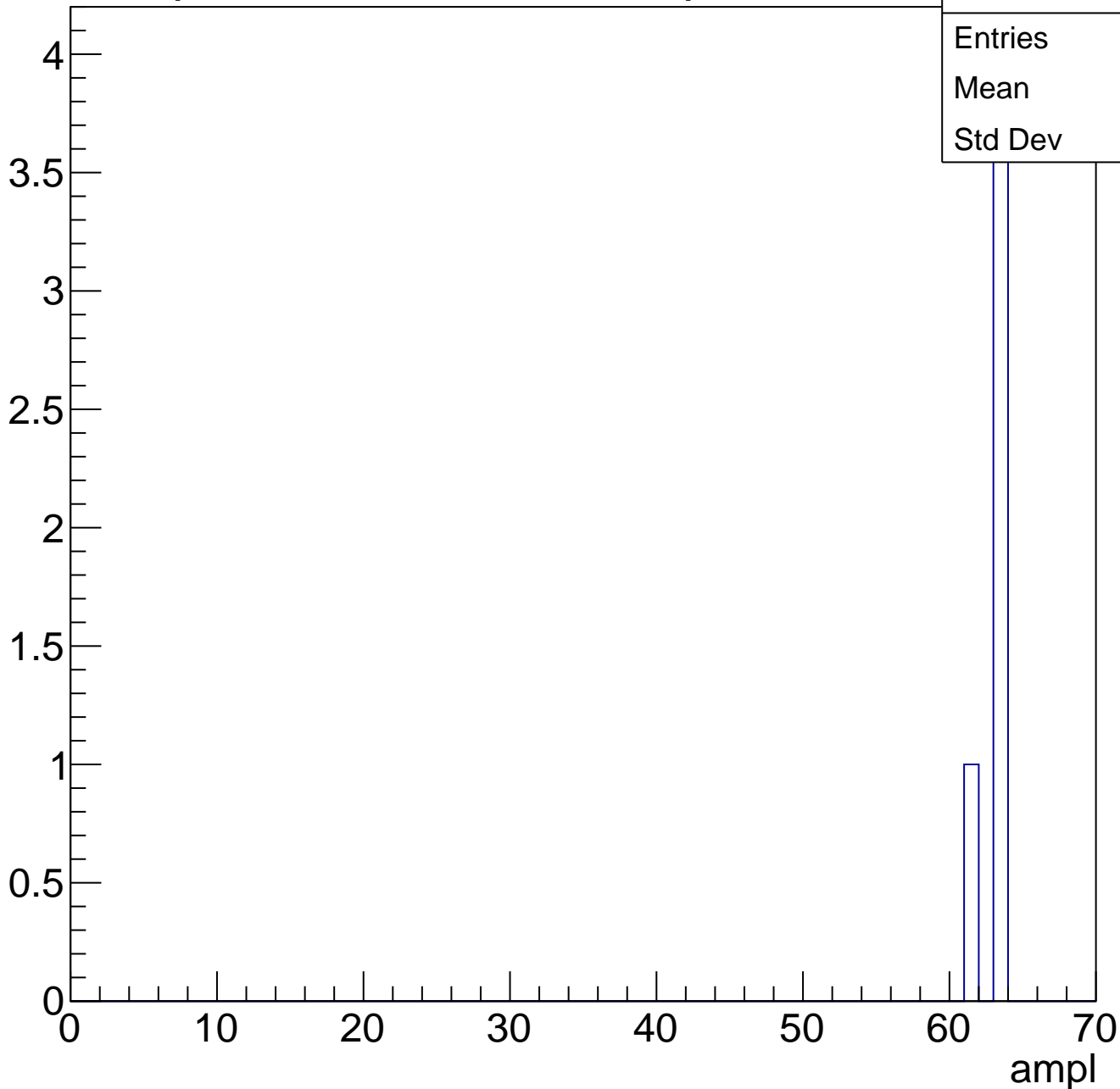
Entries	43
Mean	58.88
Std Dev	9.314



# B0L001S, U5-ch19, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch19, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U5-ch20, adc0

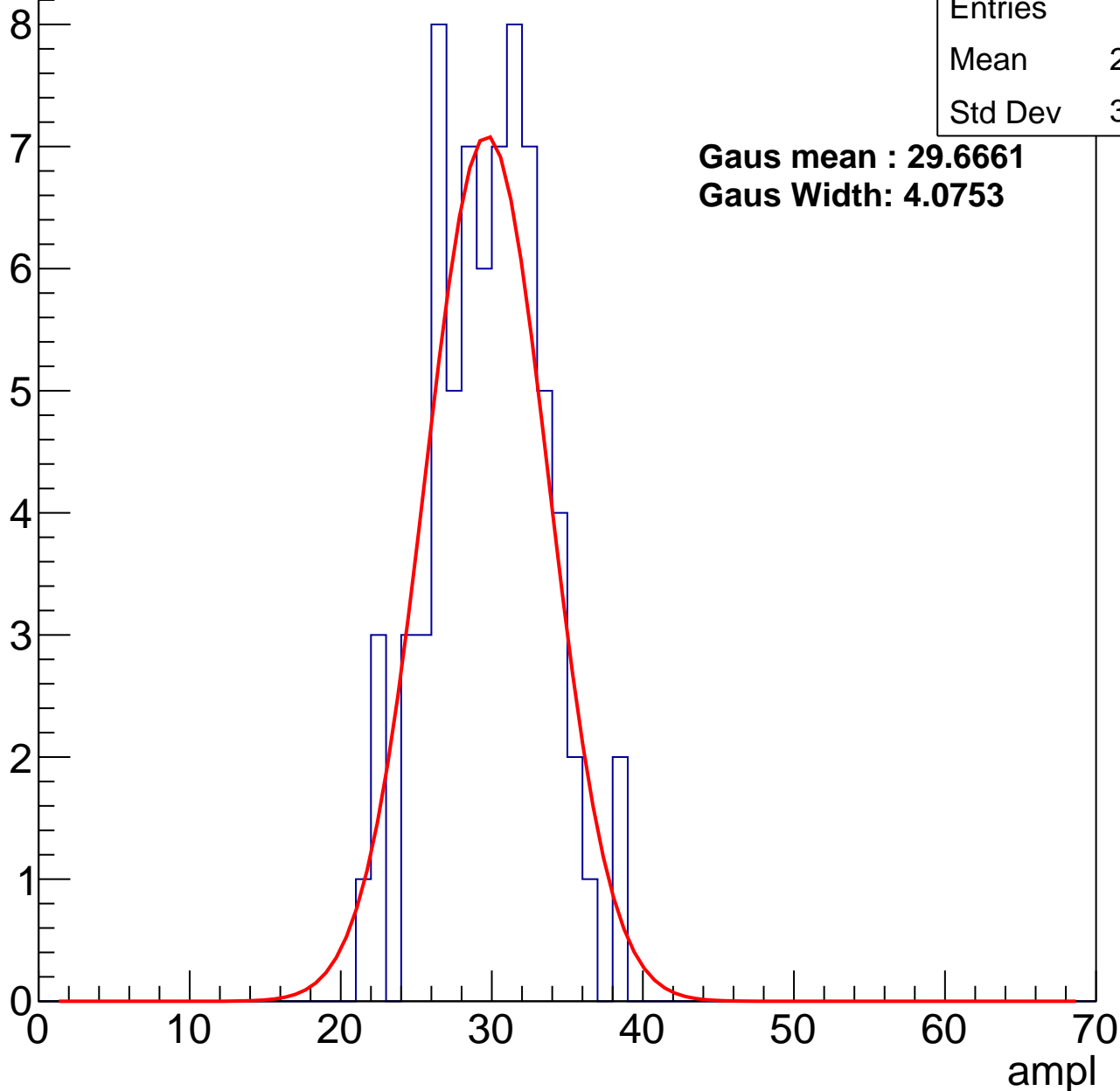
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	29.33
Std Dev	3.708

**Gaus mean : 29.6661**

**Gaus Width: 4.0753**



# B0L001S, U5-ch20, adc1

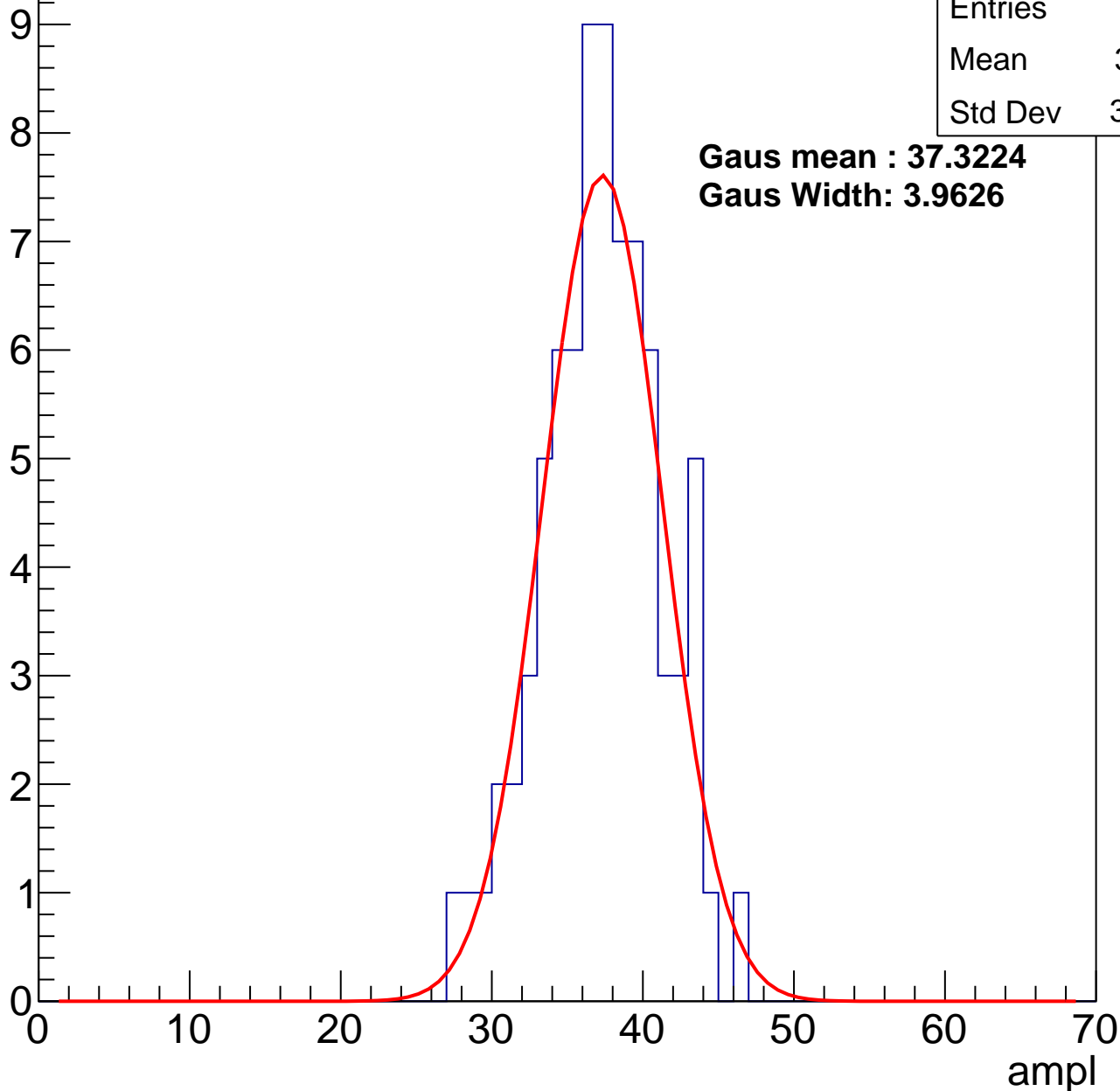
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	78
Mean	36.81
Std Dev	3.883

**Gaus mean : 37.3224**

**Gaus Width: 3.9626**



# B0L001S, U5-ch20, adc2

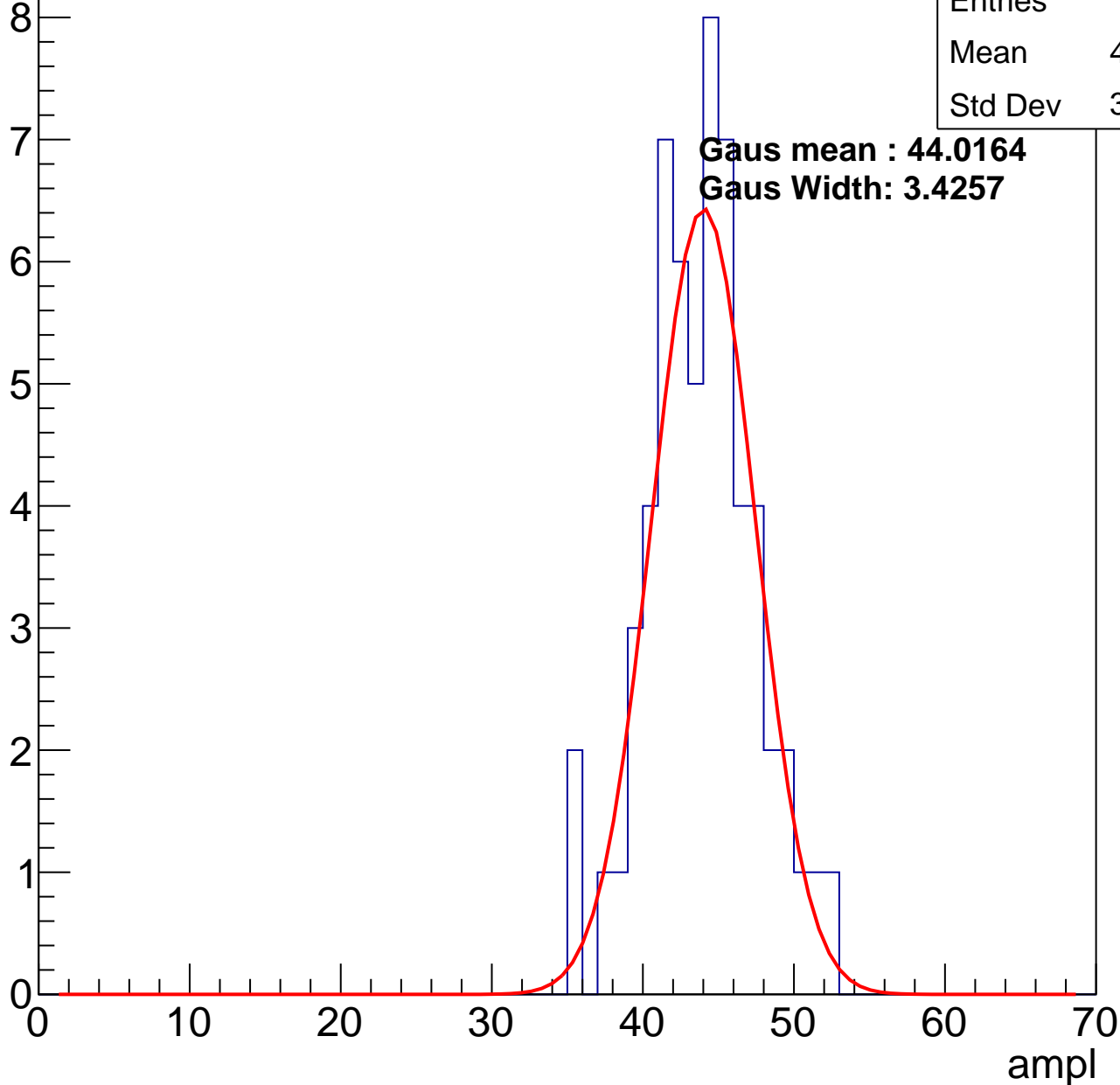
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	43.42
Std Dev	3.562

**Gaus mean : 44.0164**

**Gaus Width: 3.4257**

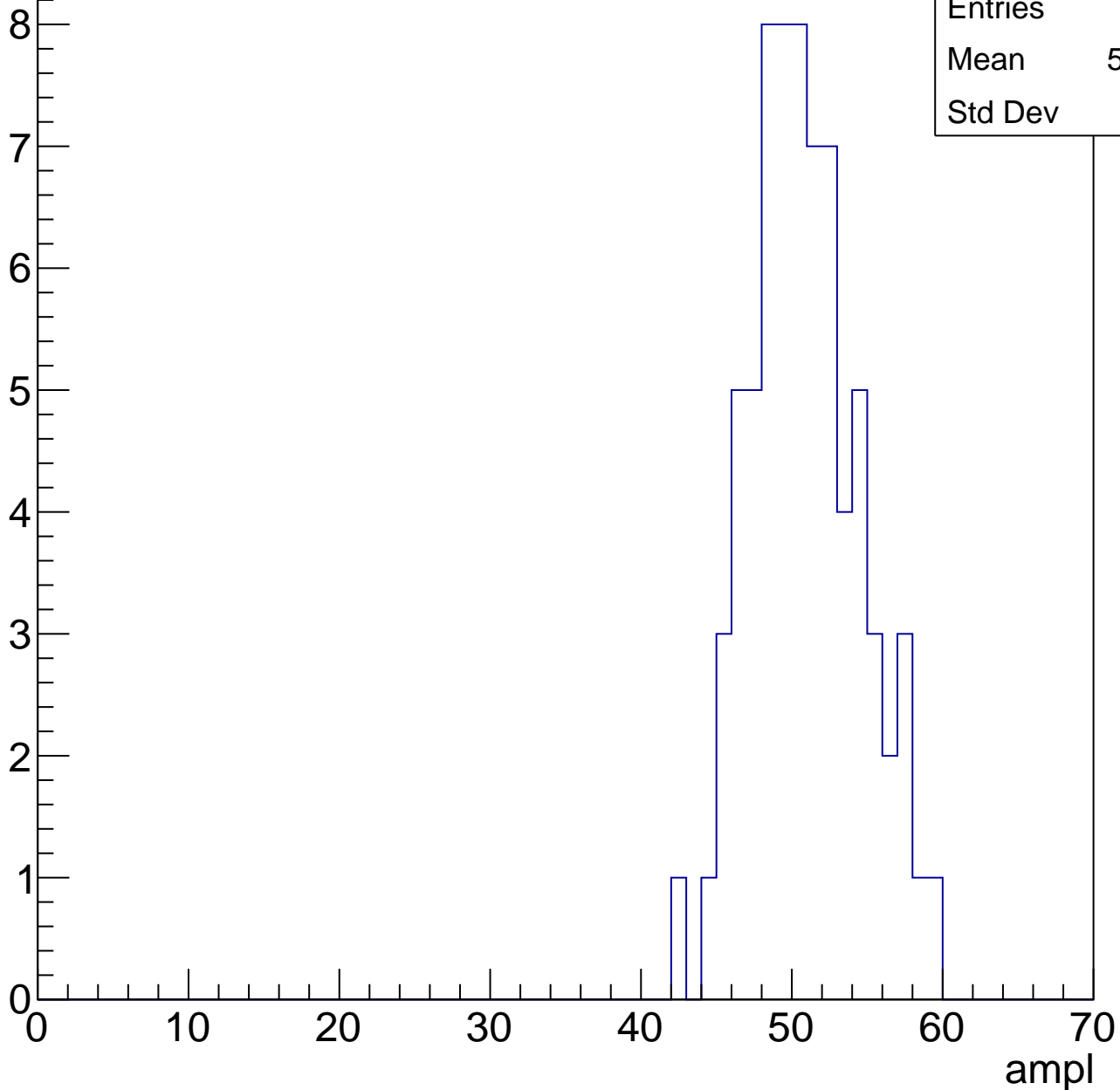


# B0L001S, U5-ch20, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

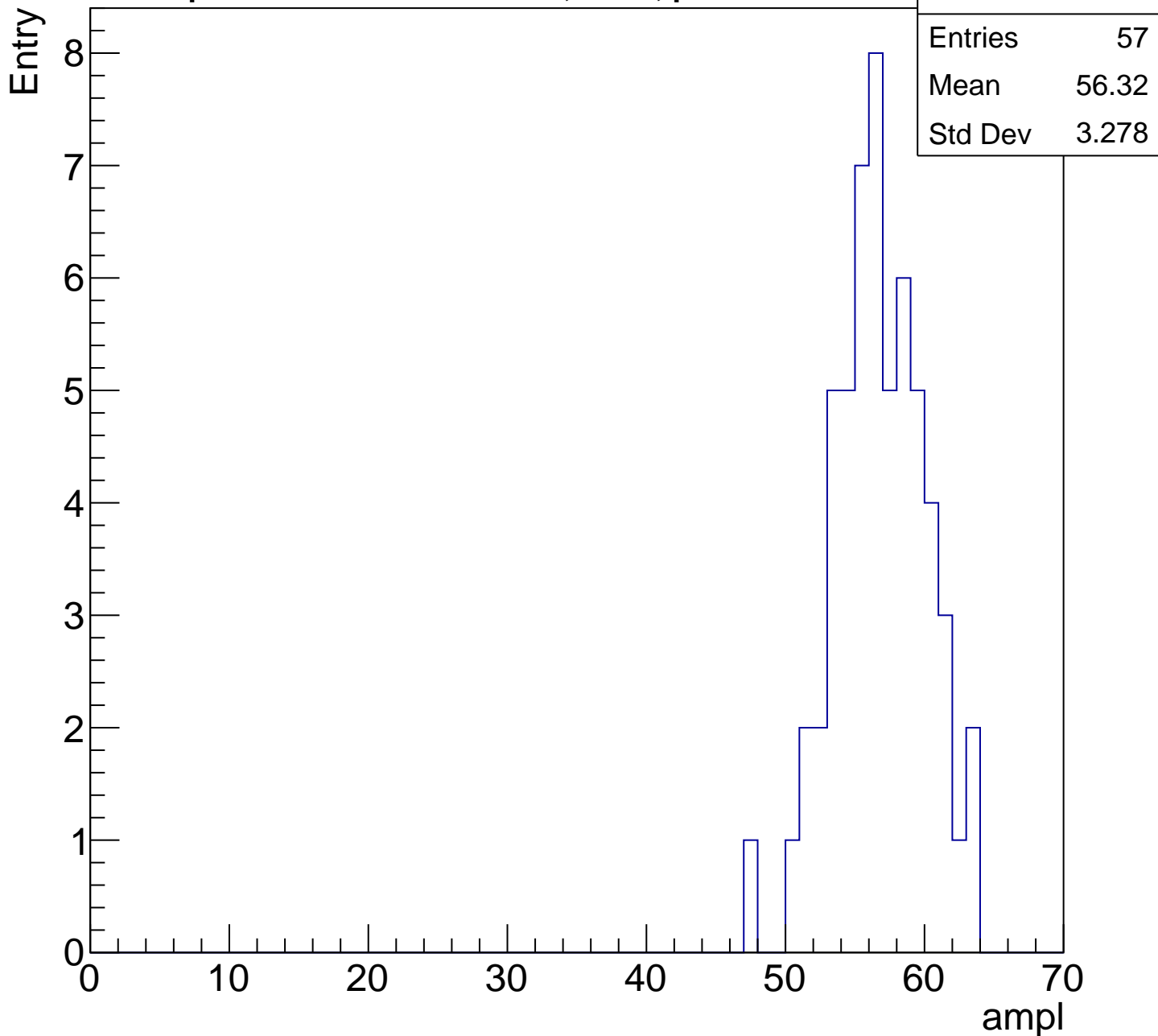
Entry

Entries	72
Mean	50.42
Std Dev	3.57



# B0L001S, U5-ch20, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

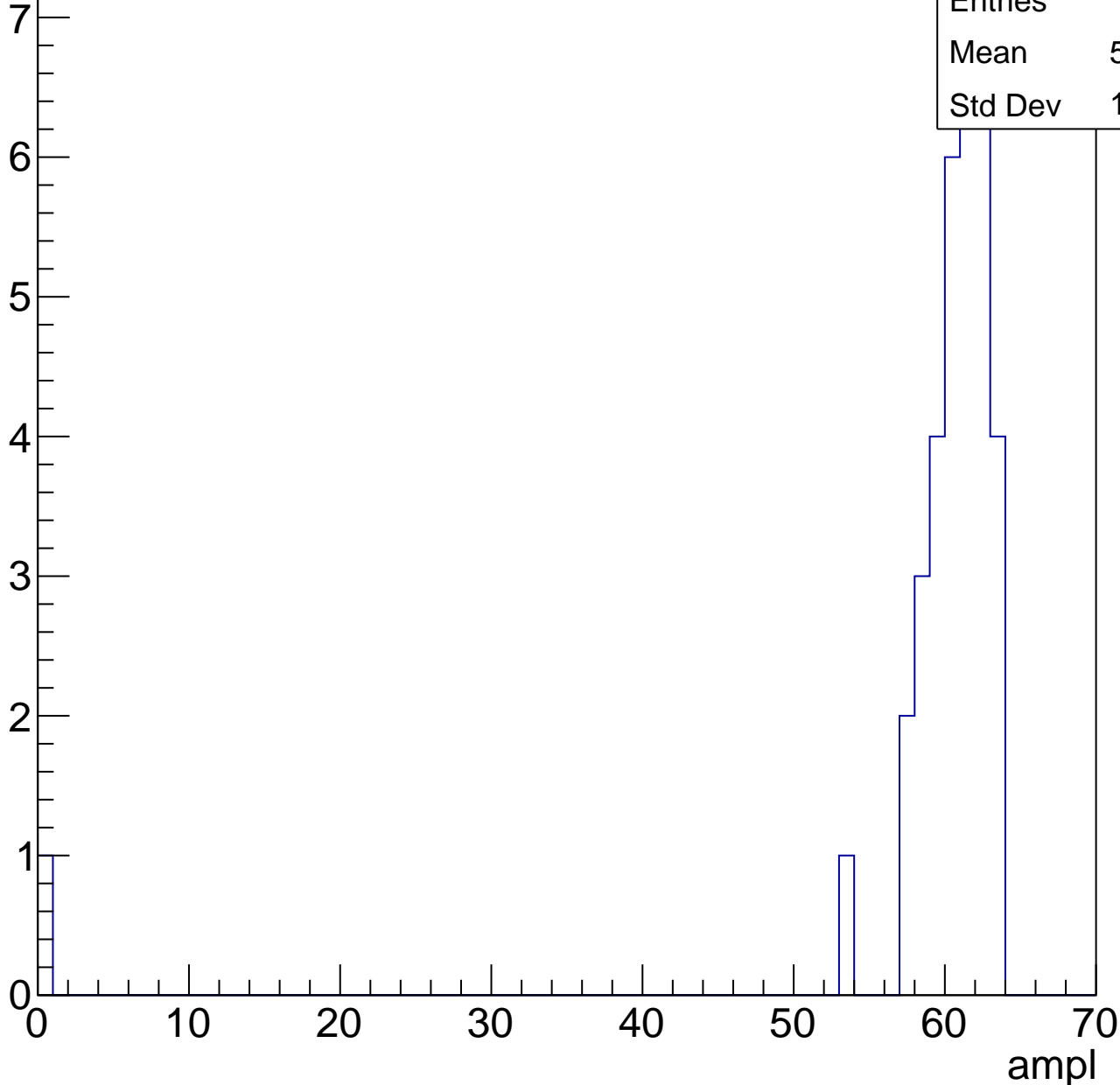


# B0L001S, U5-ch20, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

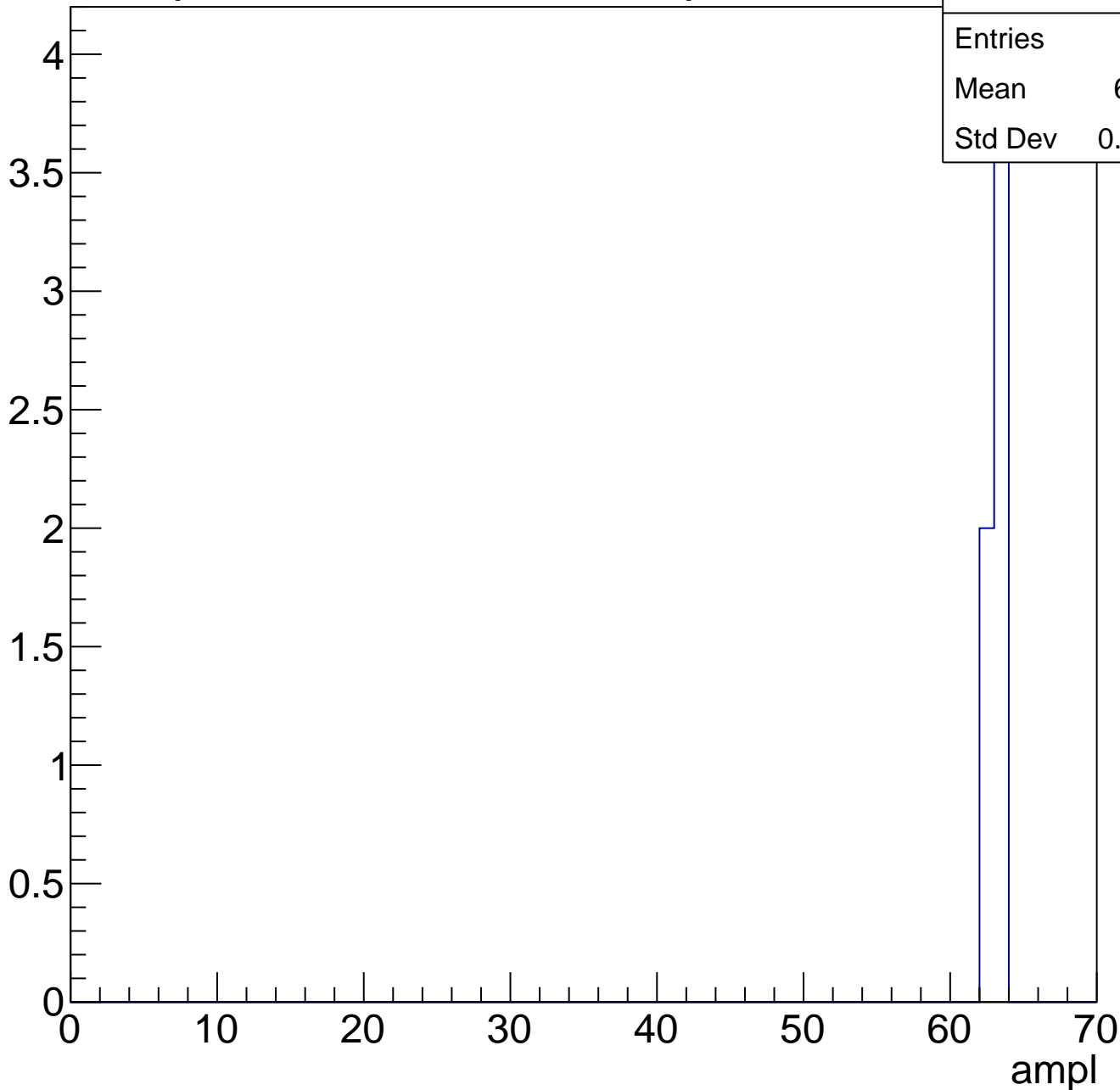
Entries	35
Mean	58.57
Std Dev	10.26



# B0L001S, U5-ch20, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch20, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch21, adc0

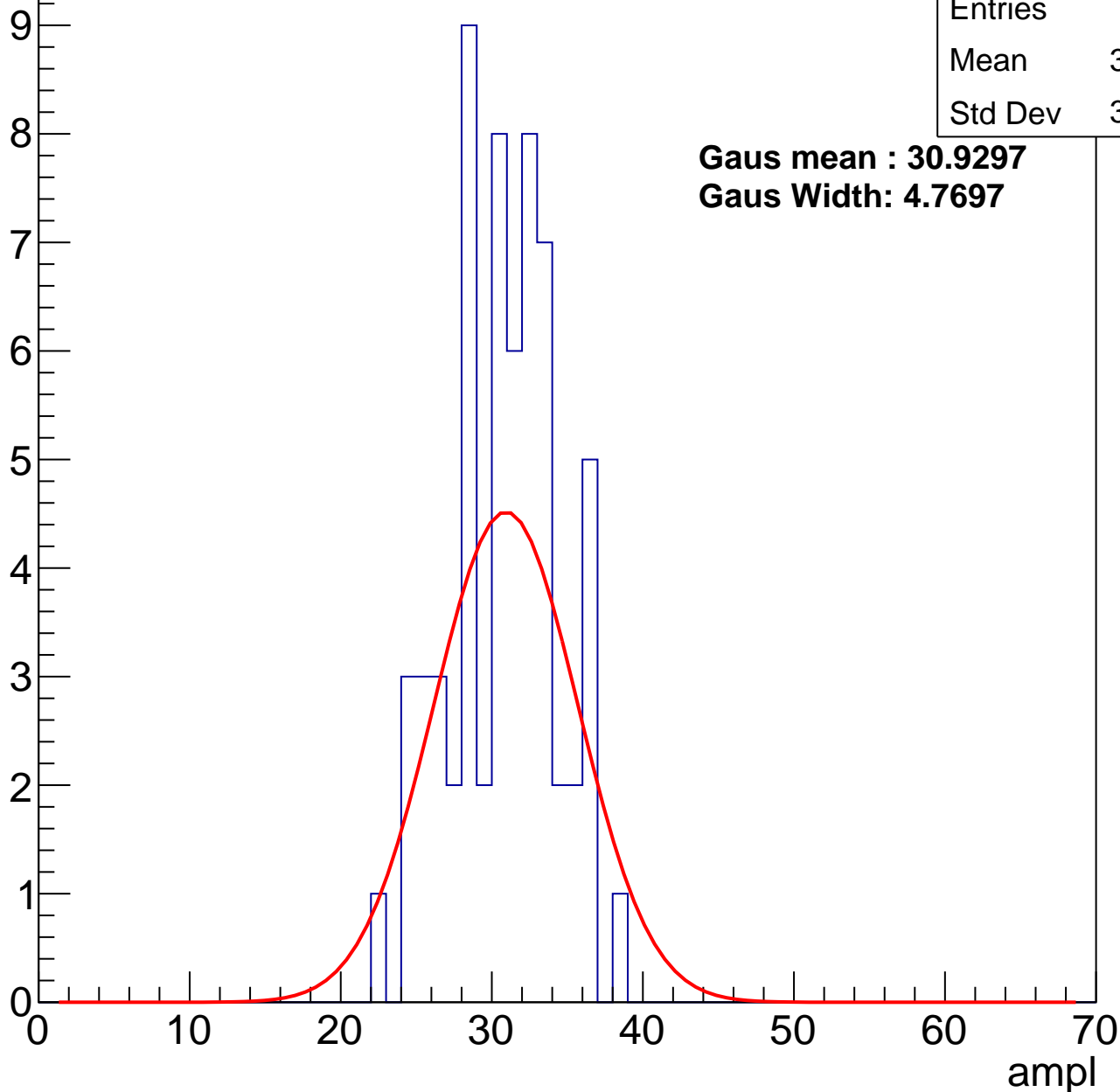
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	30.32
Std Dev	3.528

**Gaus mean : 30.9297**

**Gaus Width: 4.7697**



# B0L001S, U5-ch21, adc1

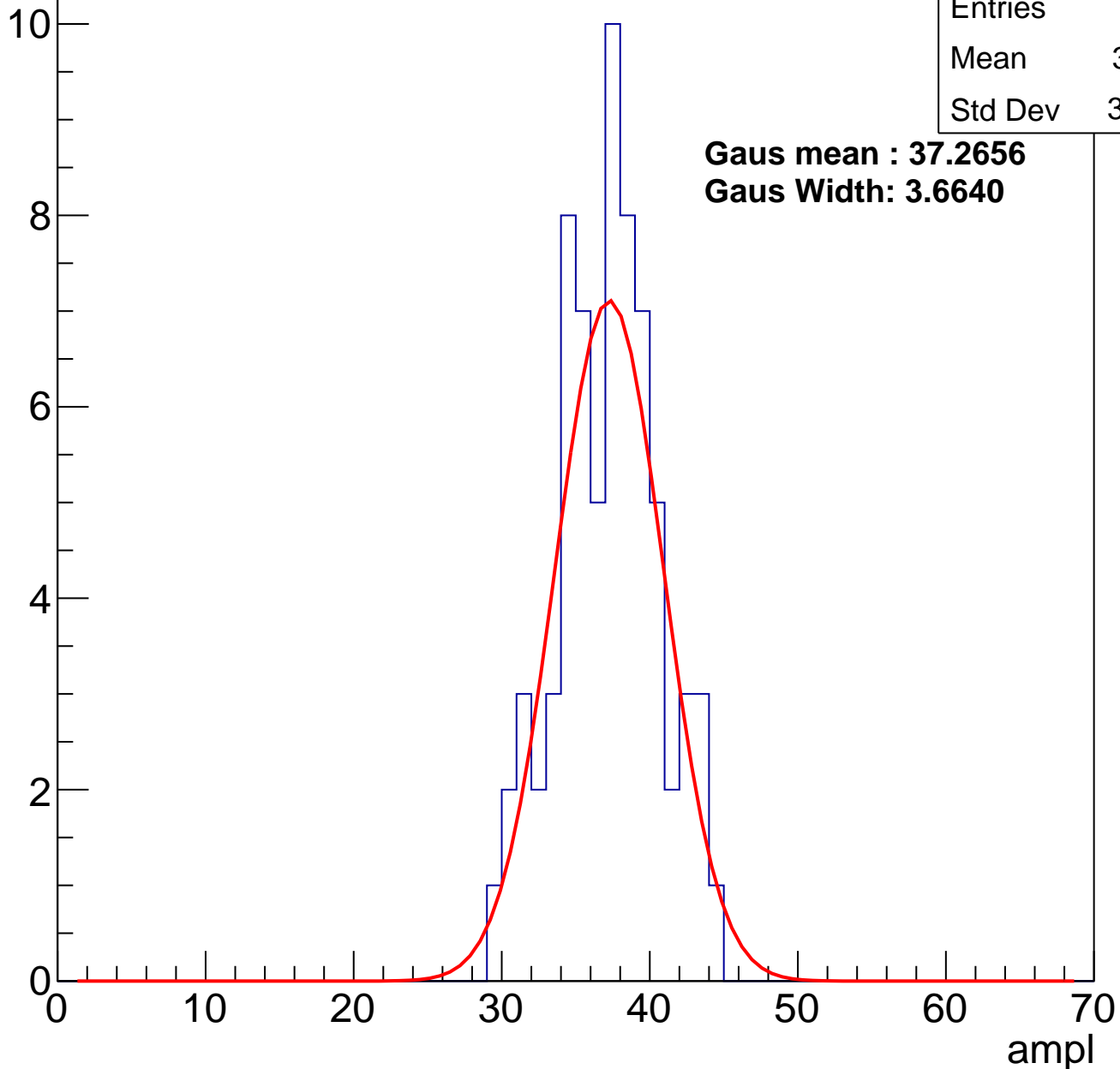
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	70
Mean	36.71
Std Dev	3.406

**Gaus mean : 37.2656**

**Gaus Width: 3.6640**

Entry



# B0L001S, U5-ch21, adc2

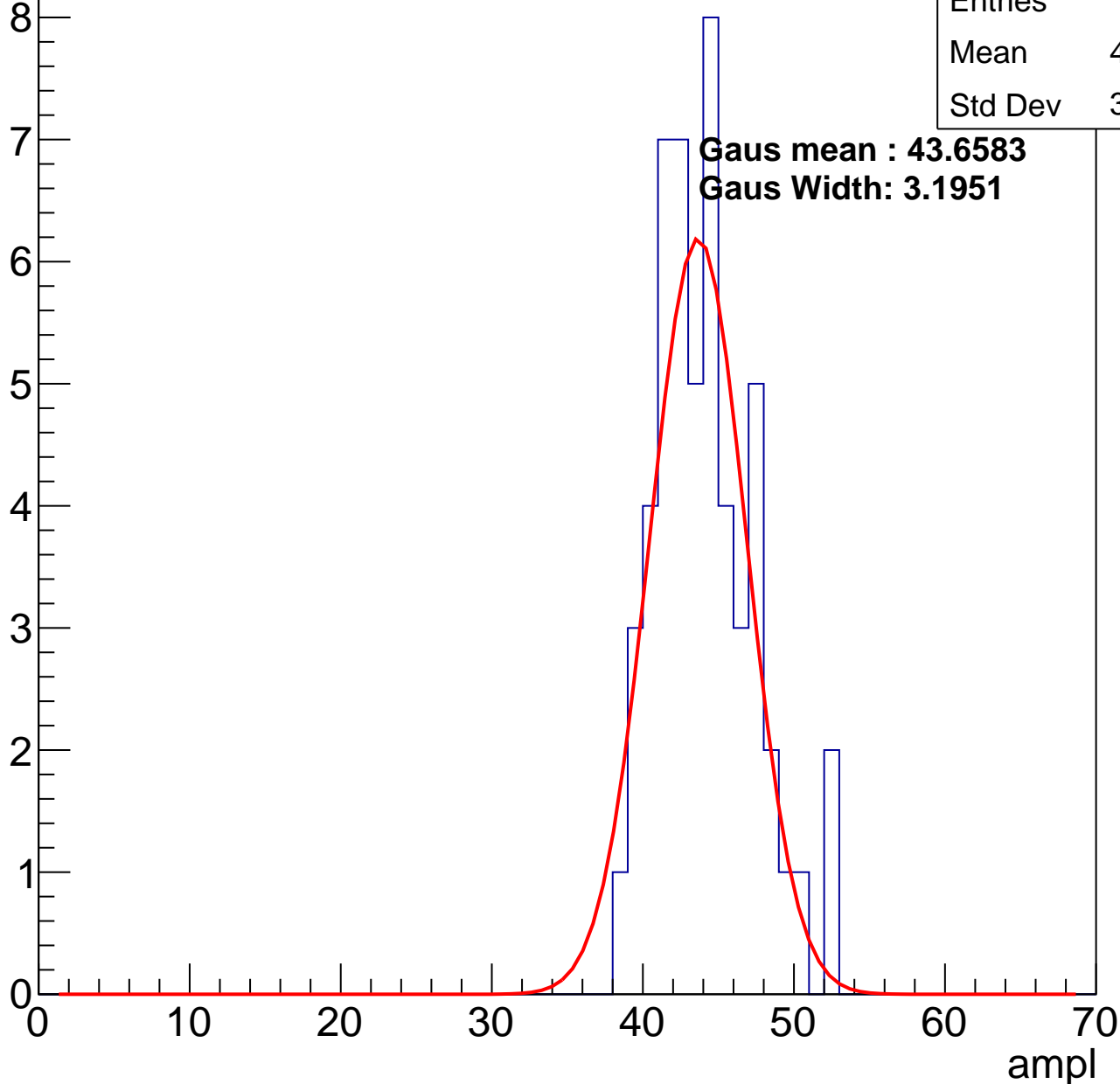
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	43.68
Std Dev	3.214

**Gaus mean : 43.6583**

**Gaus Width: 3.1951**



# B0L001S, U5-ch21, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

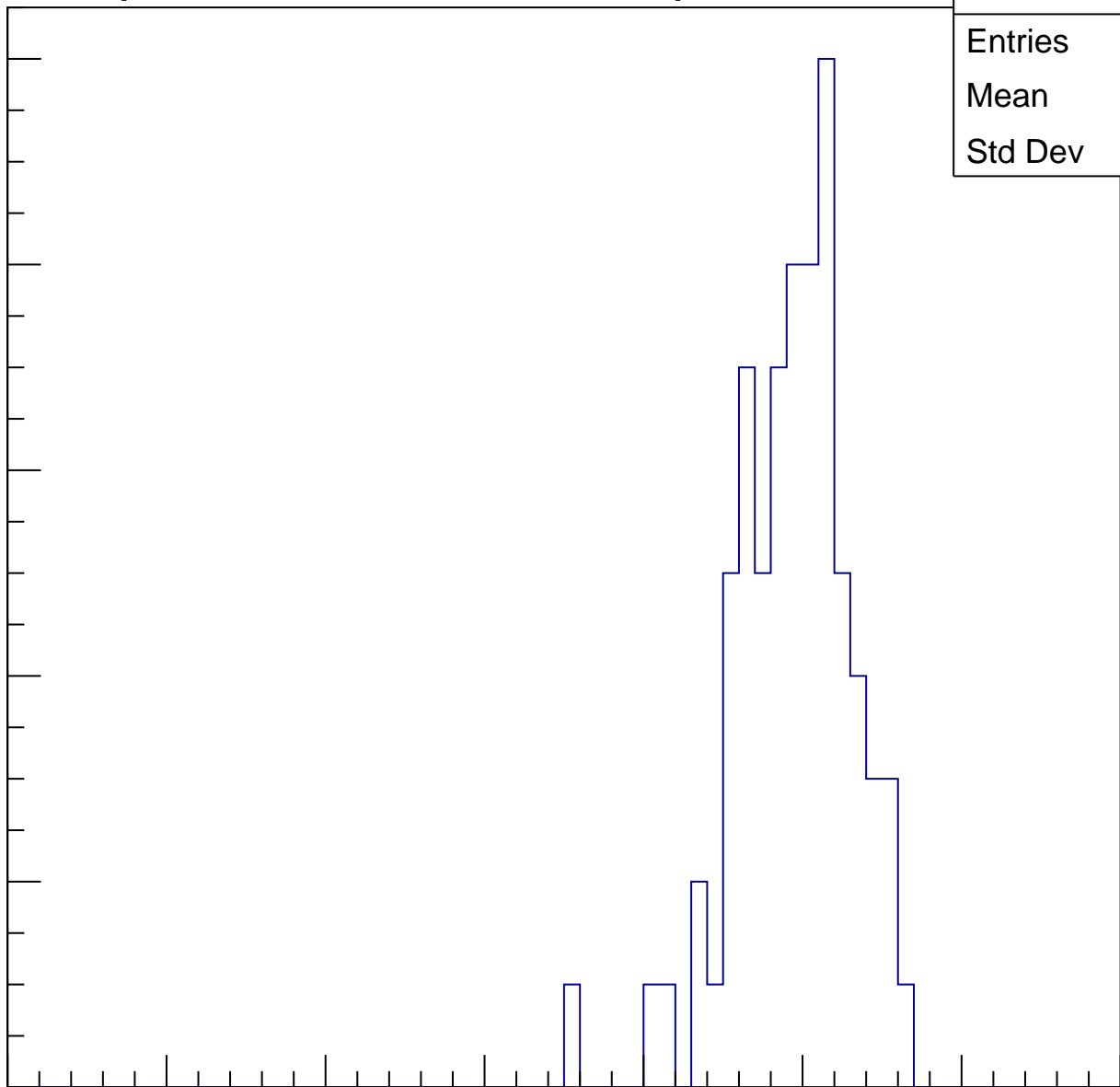
Entries	72
Mean	48.9
Std Dev	3.72

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B0L001S, U5-ch21, adc4

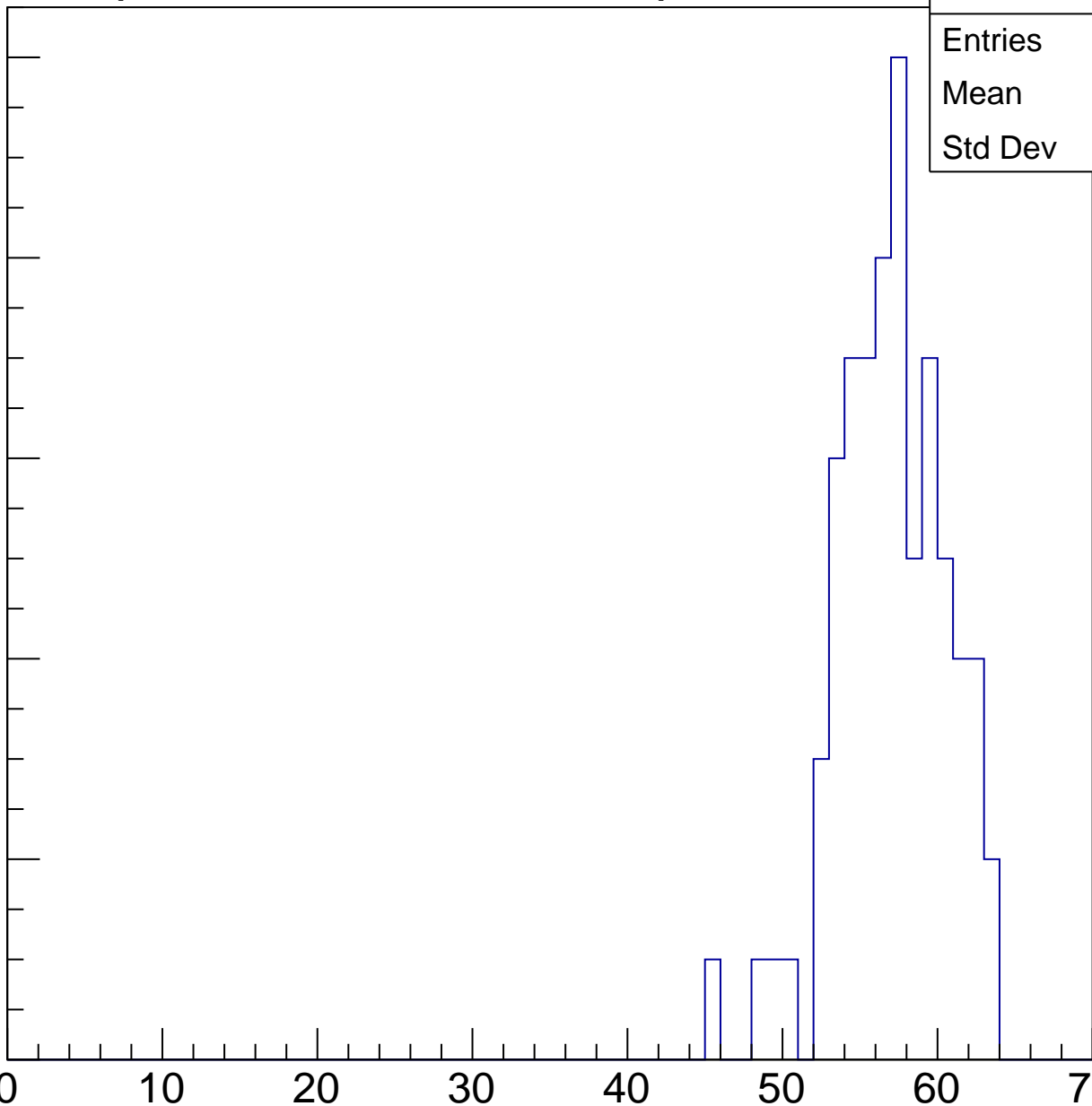
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

10  
8  
6  
4  
2  
0

Entries	72
Mean	56.5
Std Dev	3.543

ampl

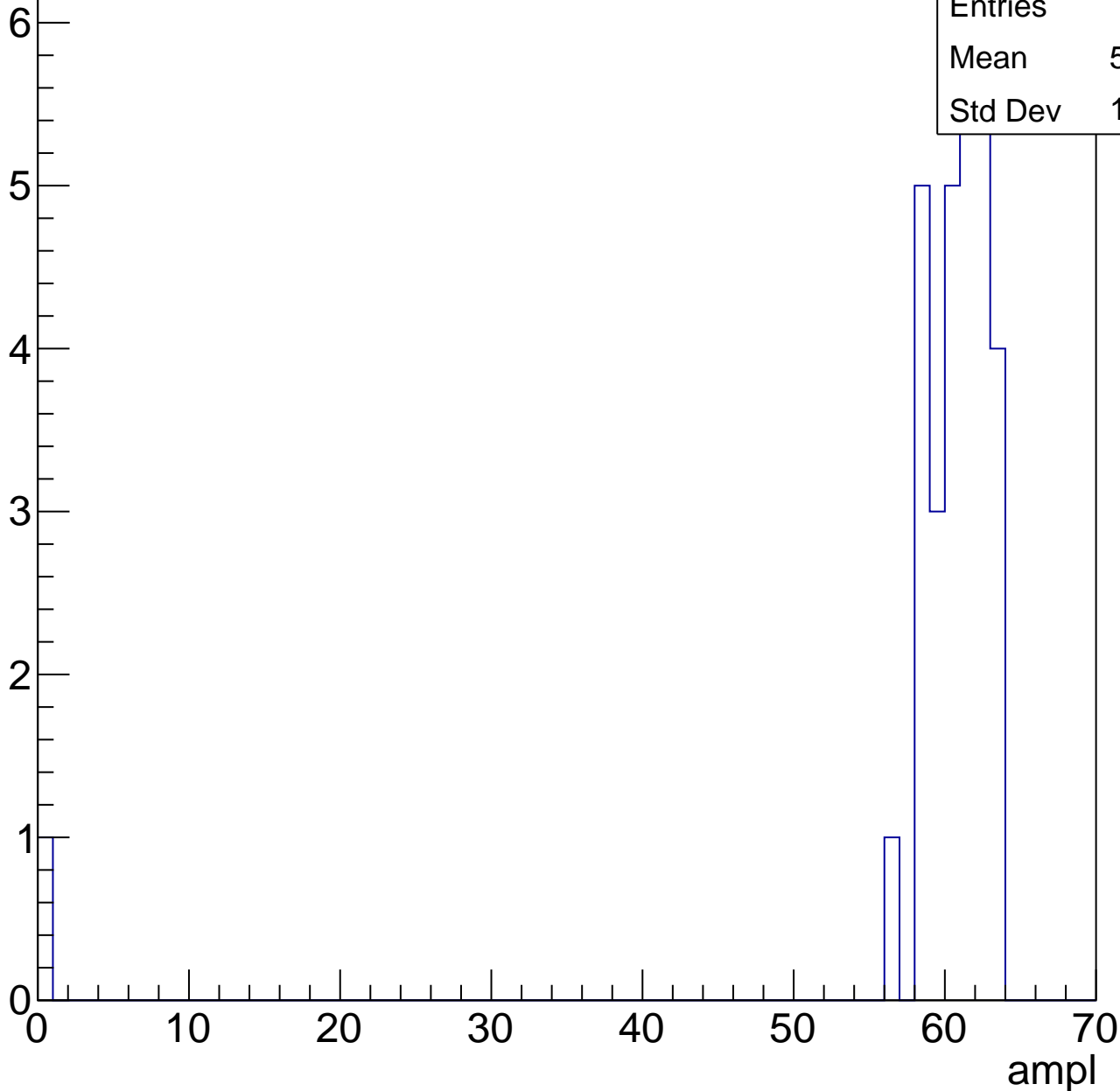


# B0L001S, U5-ch21, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

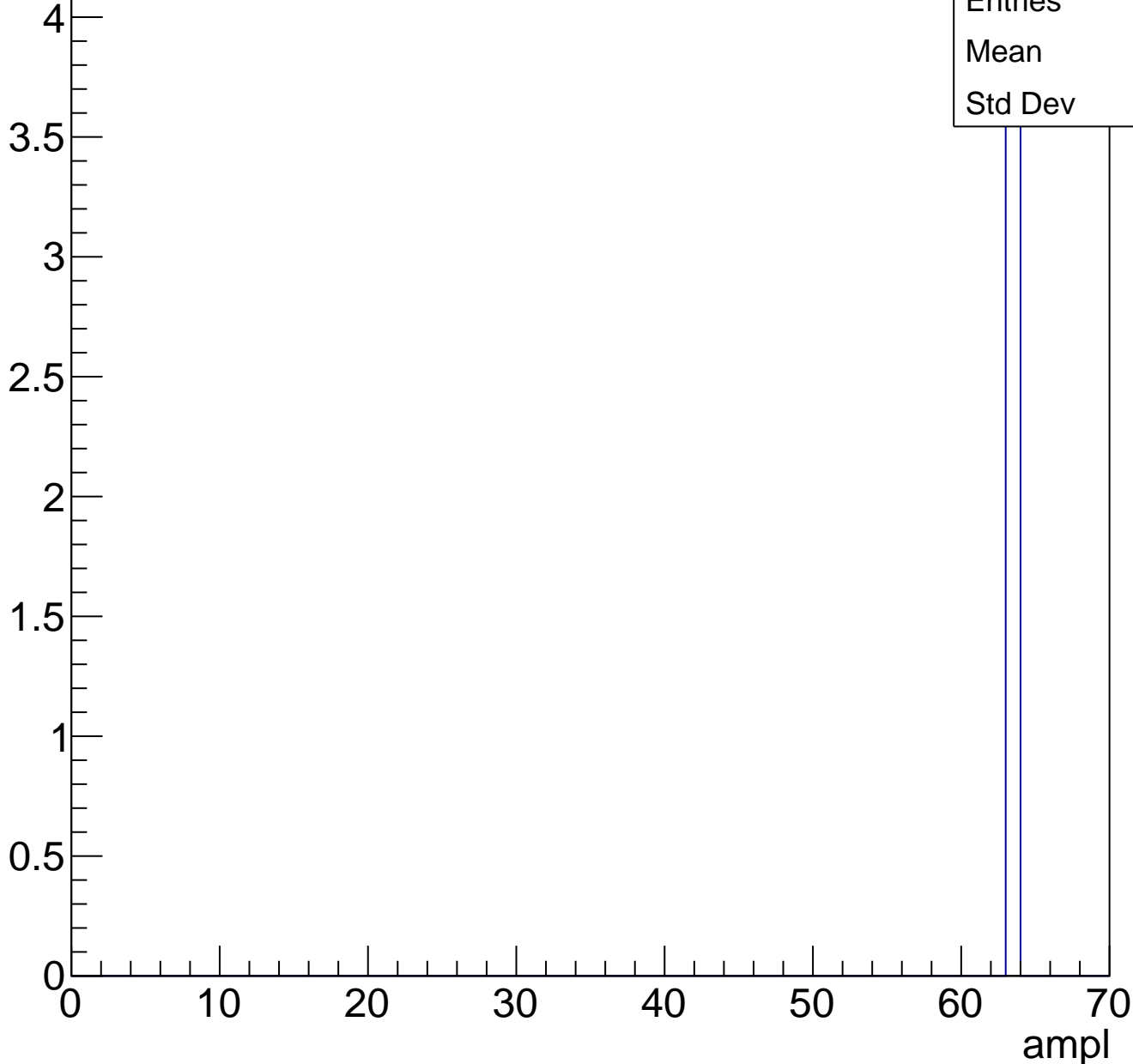
Entries	31
Mean	58.48
Std Dev	10.83



# B0L001S, U5-ch21, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch21, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U5-ch22, adc0

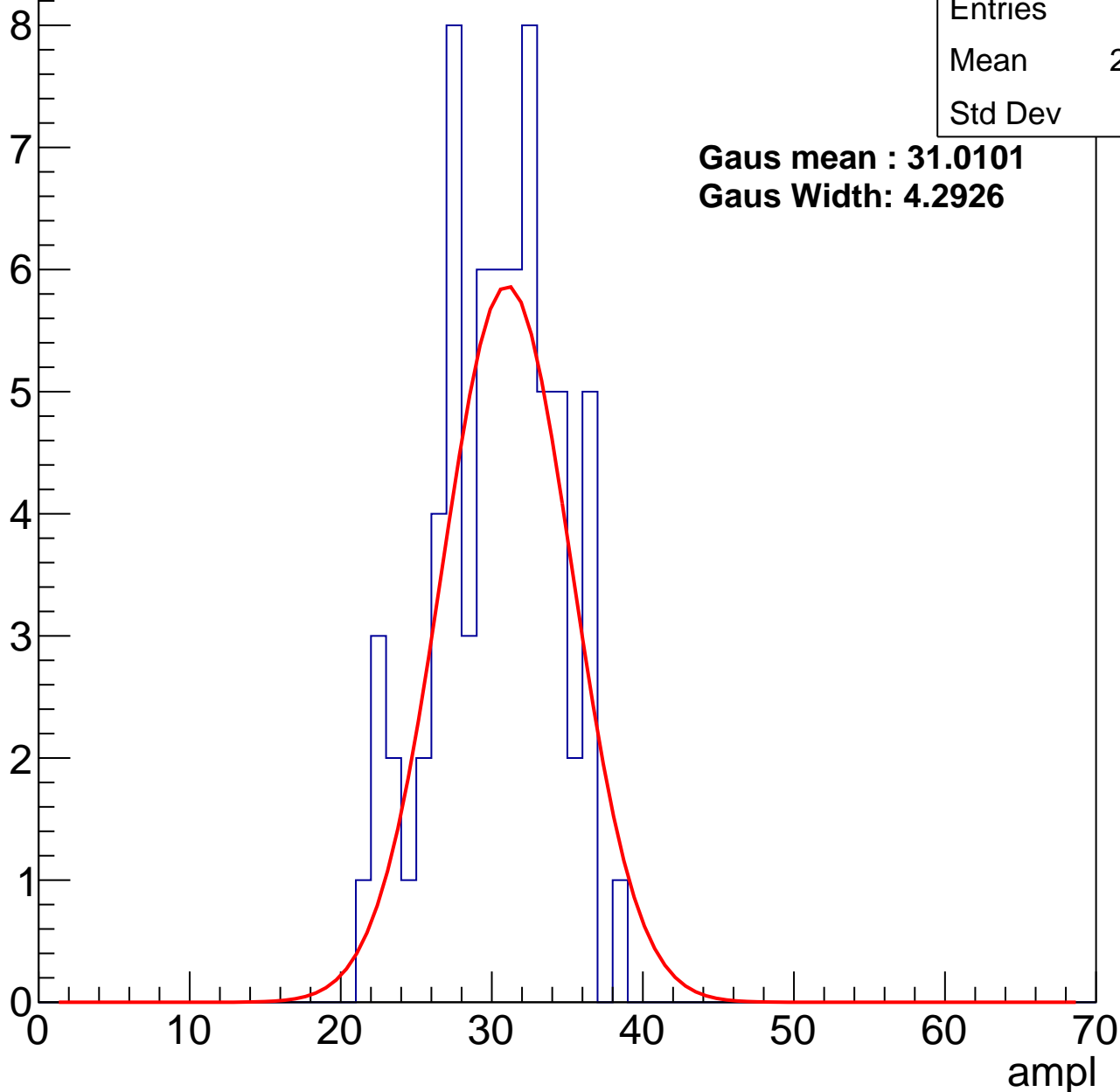
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	29.85
Std Dev	3.96

**Gaus mean : 31.0101**

**Gaus Width: 4.2926**



# B0L001S, U5-ch22, adc1

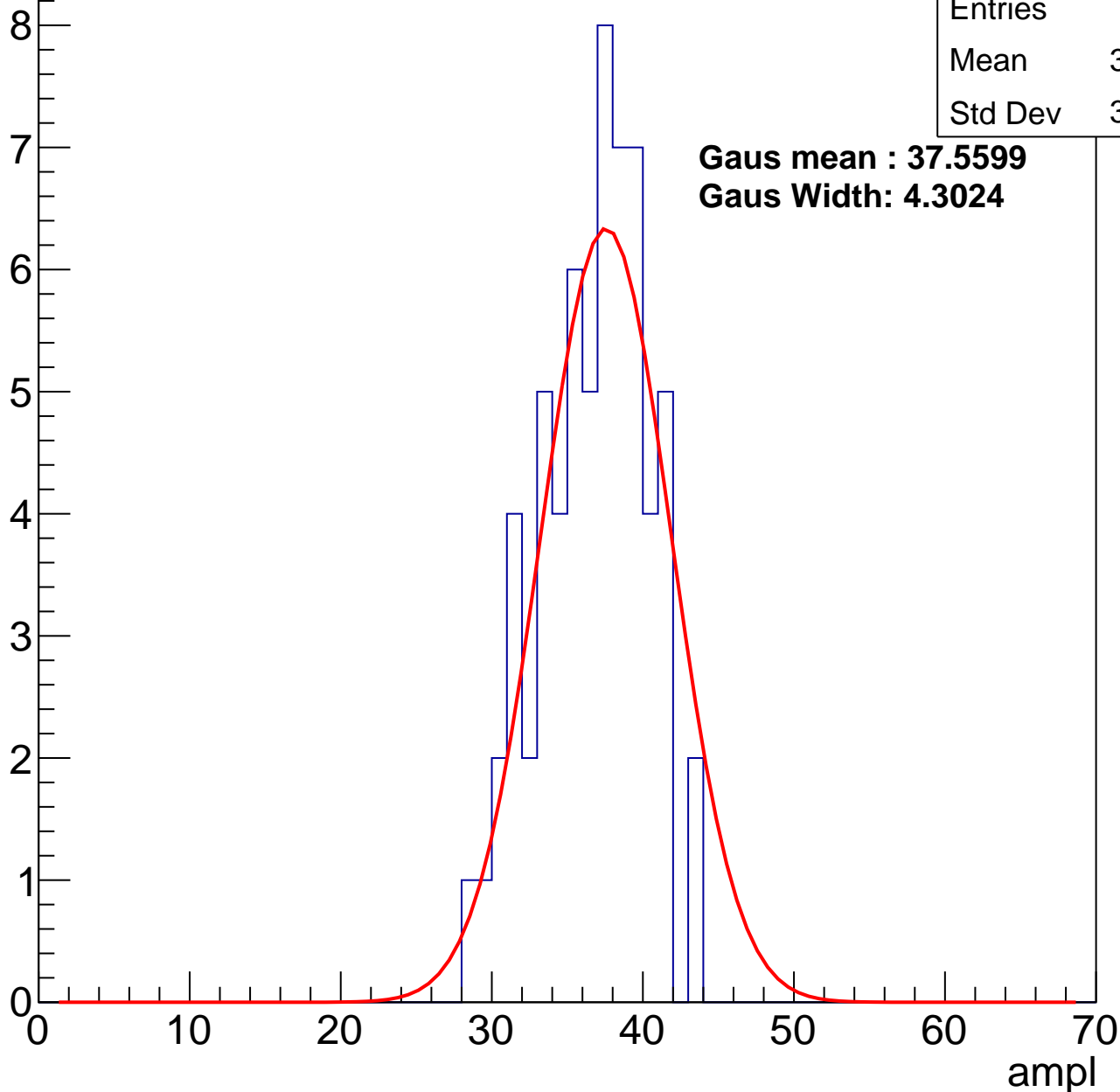
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	36.22
Std Dev	3.489

**Gaus mean : 37.5599**

**Gaus Width: 4.3024**



# B0L001S, U5-ch22, adc2

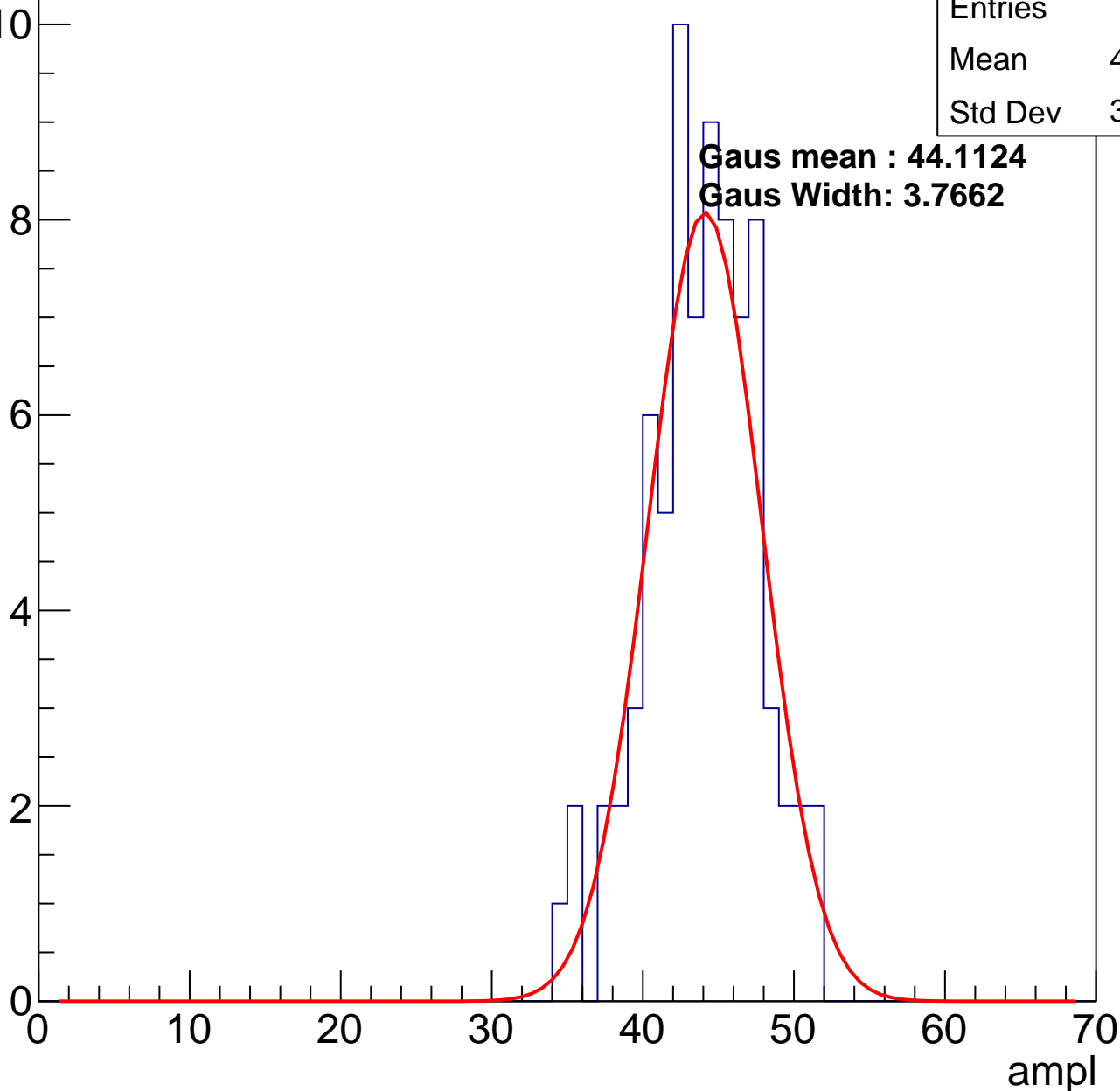
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	79
Mean	43.48
Std Dev	3.645

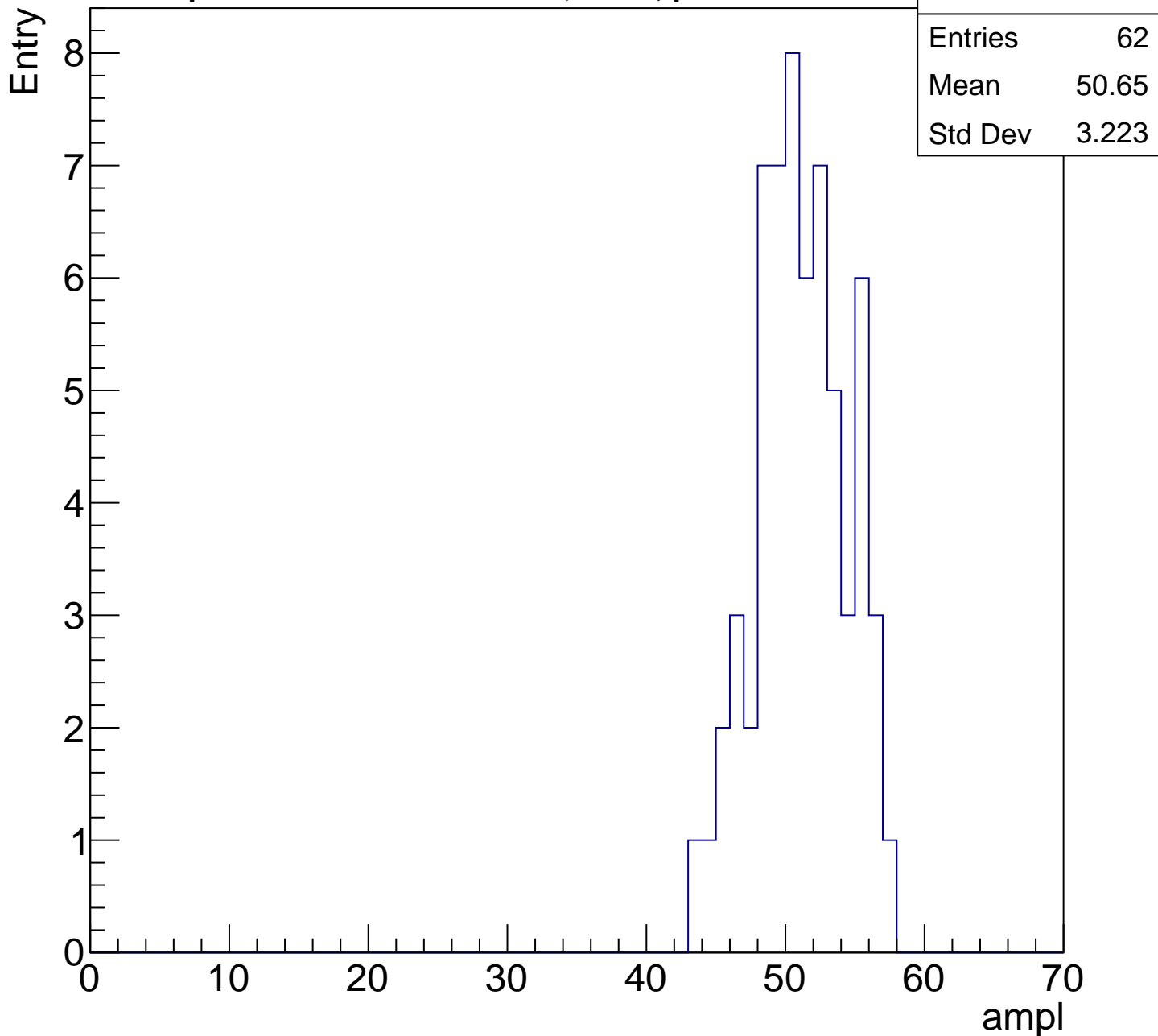
**Gaus mean : 44.1124**

**Gaus Width: 3.7662**



# B0L001S, U5-ch22, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

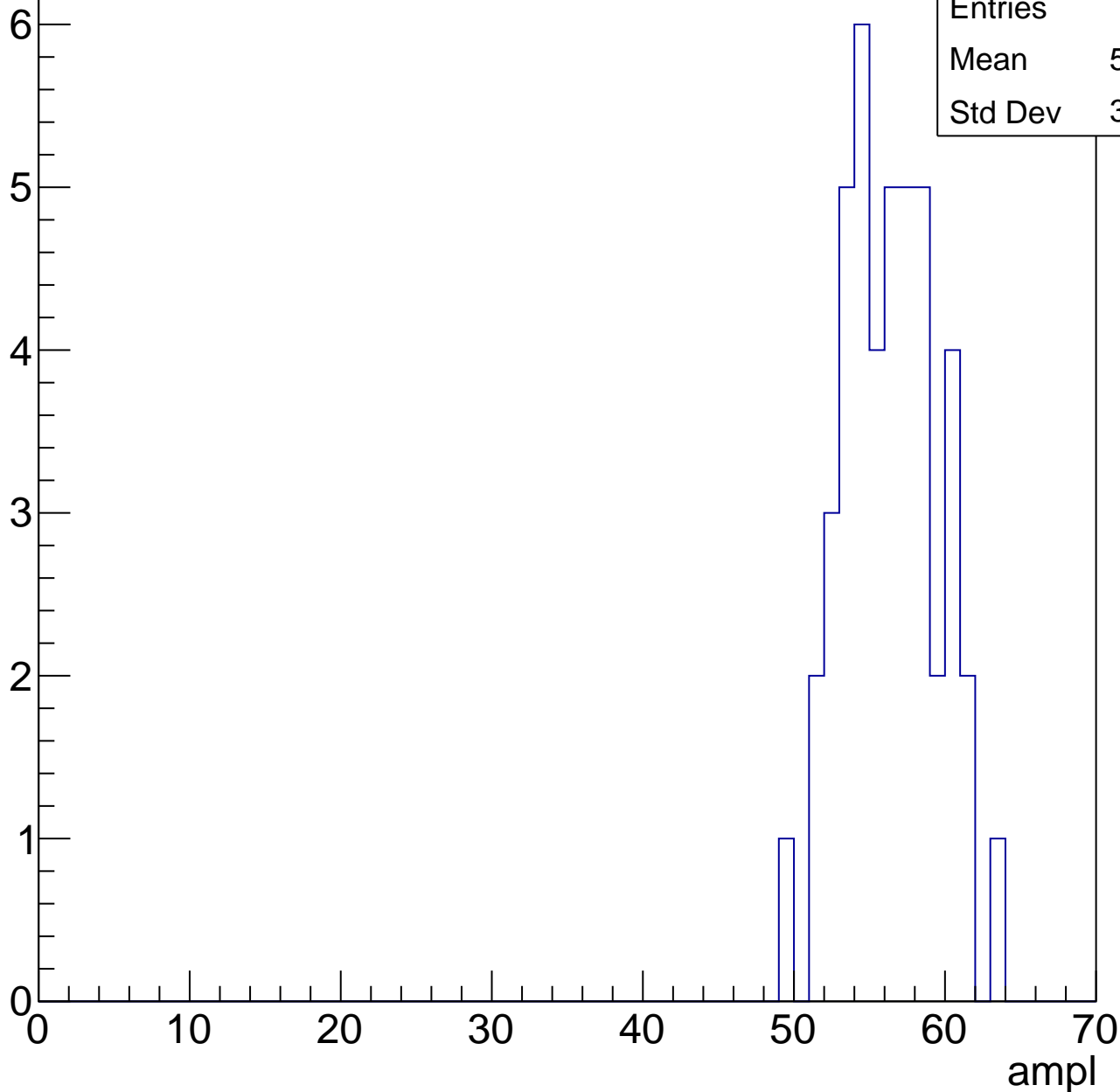


# B0L001S, U5-ch22, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	45
Mean	55.87
Std Dev	3.074



# B0L001S, U5-ch22, adc5

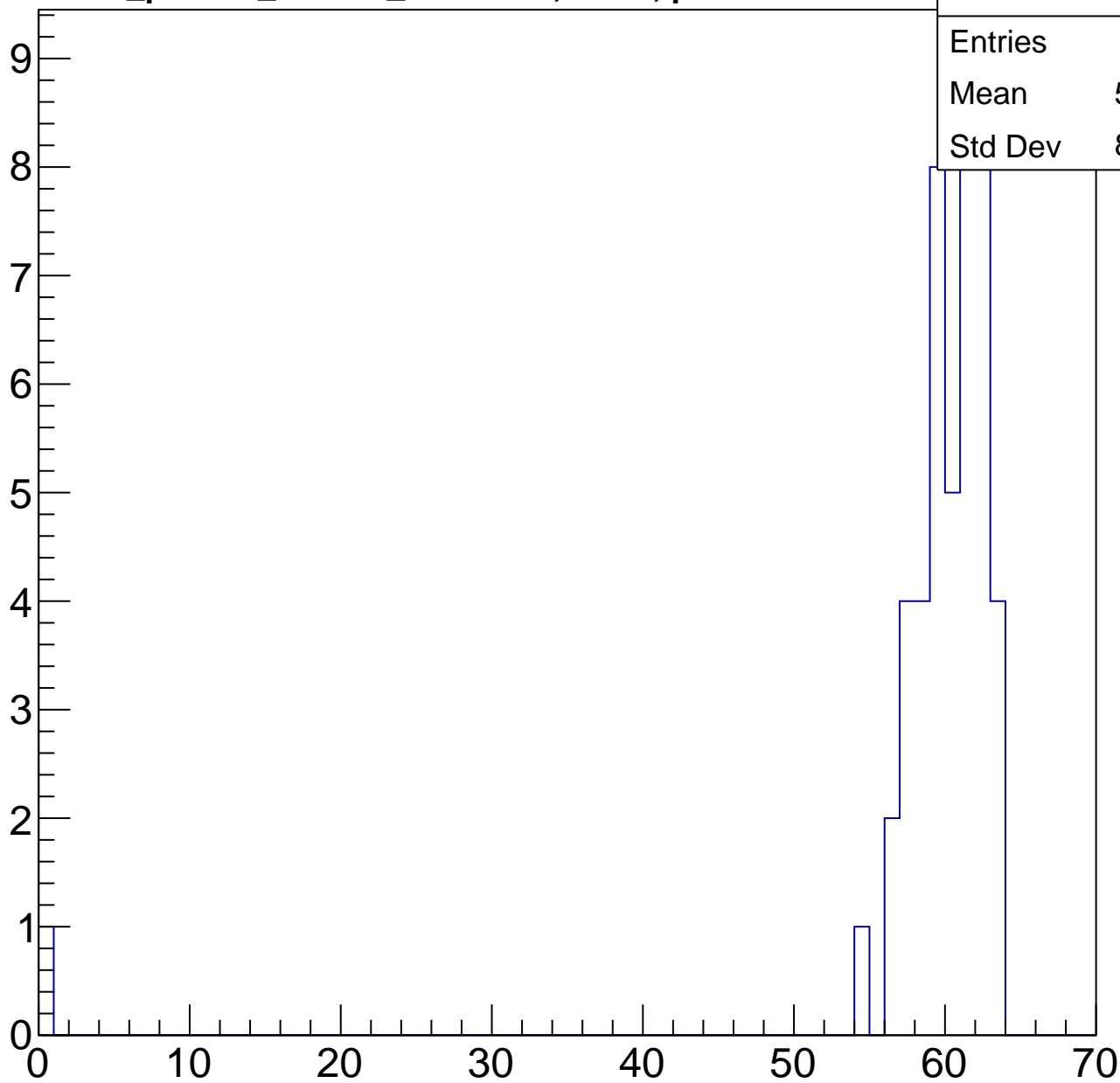
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	46
Mean	58.61
Std Dev	8.991

ampl

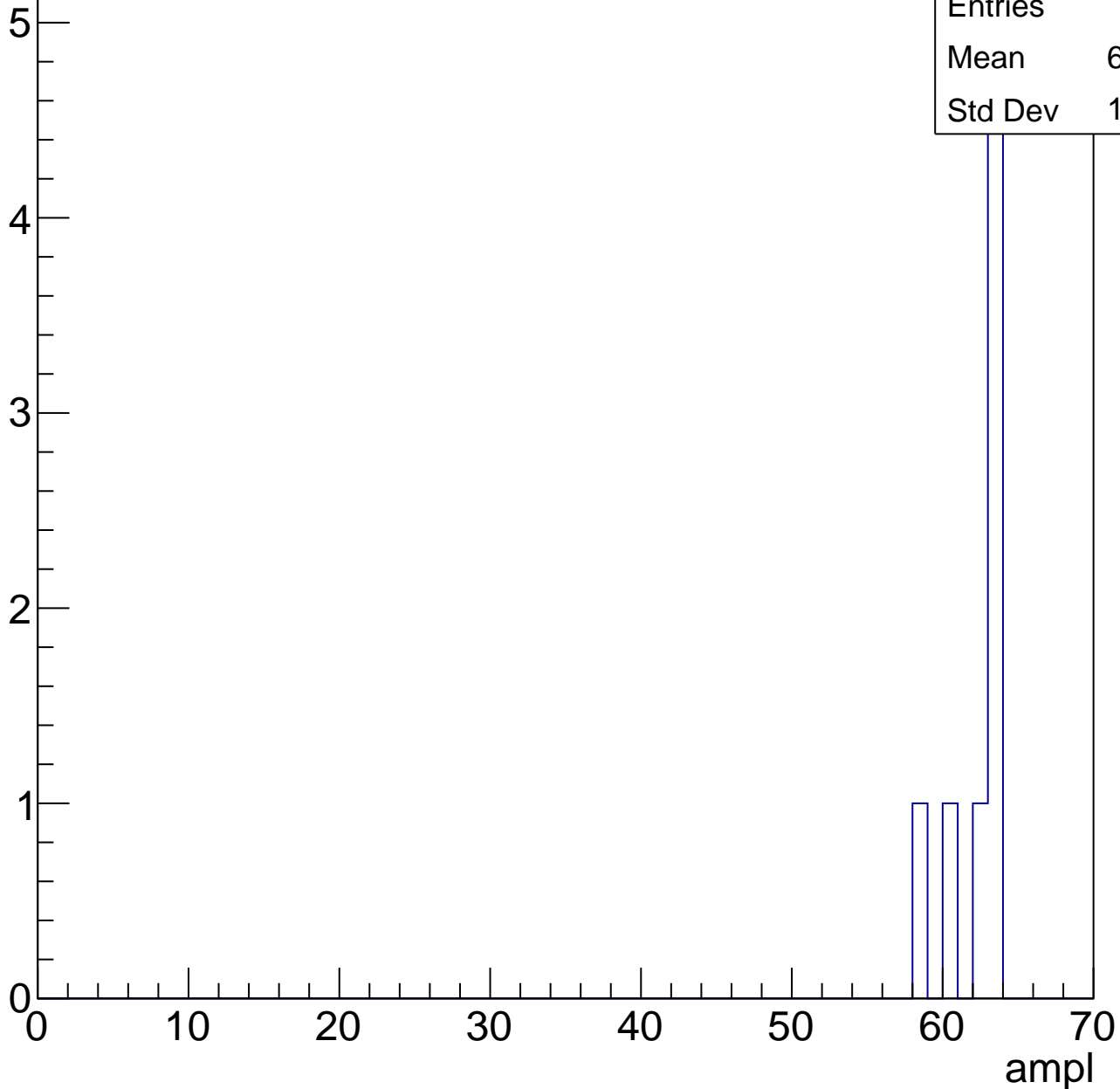


# B0L001S, U5-ch22, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	8
Mean	61.88
Std Dev	1.763





# B0L001S, U5-ch22, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch23, adc0

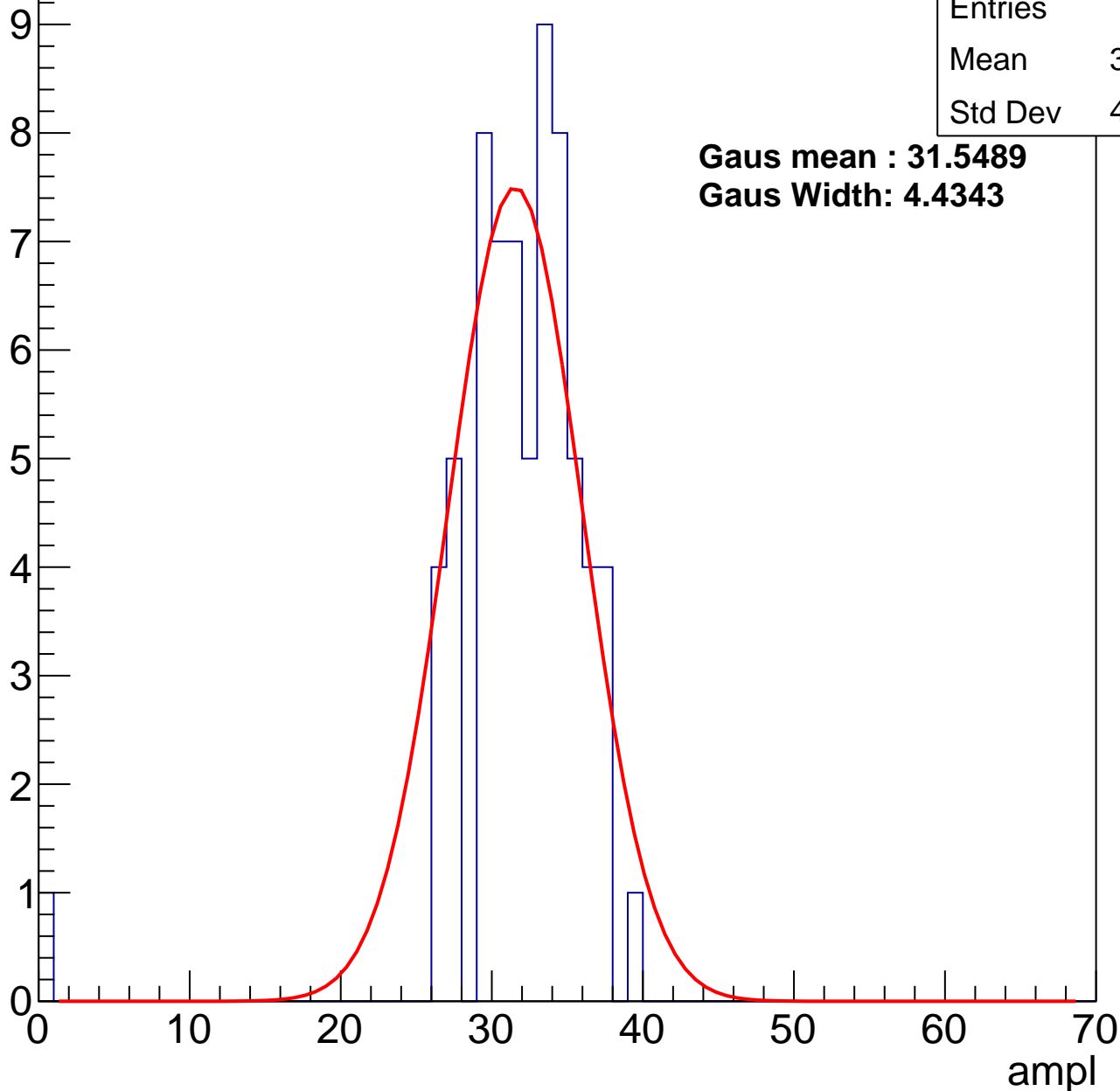
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	31.37
Std Dev	4.958

**Gaus mean : 31.5489**

**Gaus Width: 4.4343**



# B0L001S, U5-ch23, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	55
Mean	38.84
Std Dev	3.985

**Gaus mean : 39.1106**

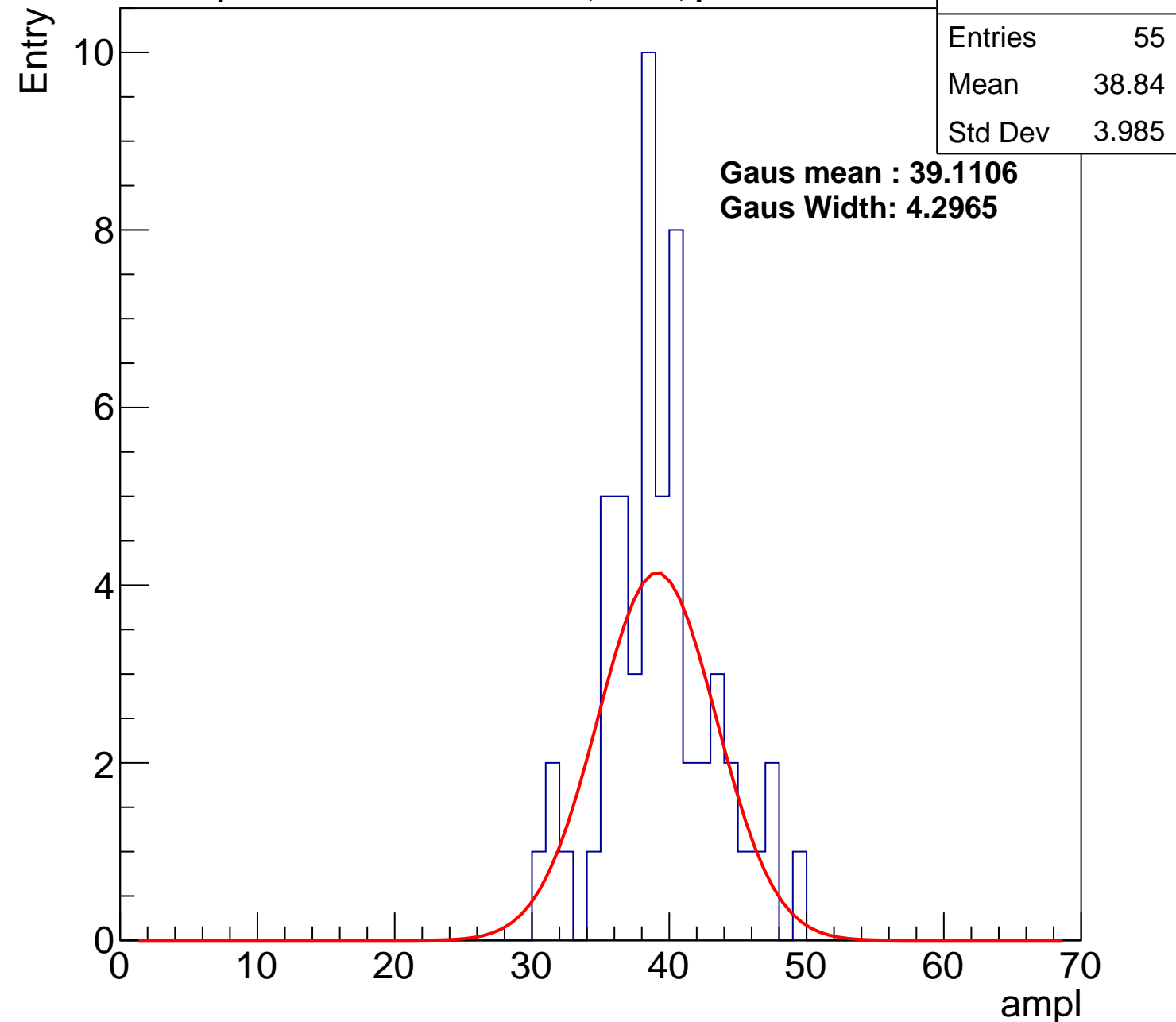
**Gaus Width: 4.2965**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U5-ch23, adc2

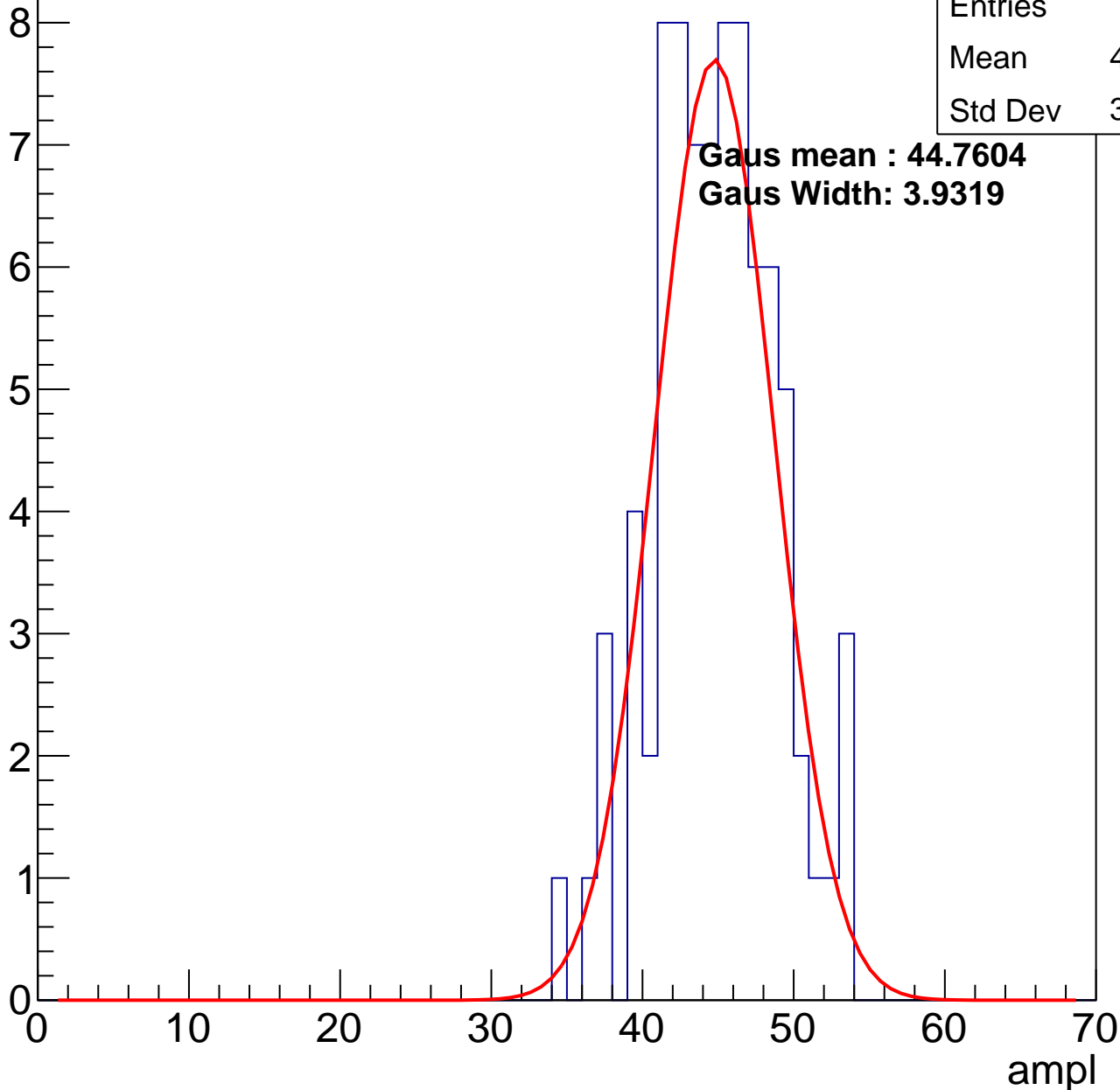
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	81
Mean	44.38
Std Dev	3.983

**Gaus mean : 44.7604**

**Gaus Width: 3.9319**

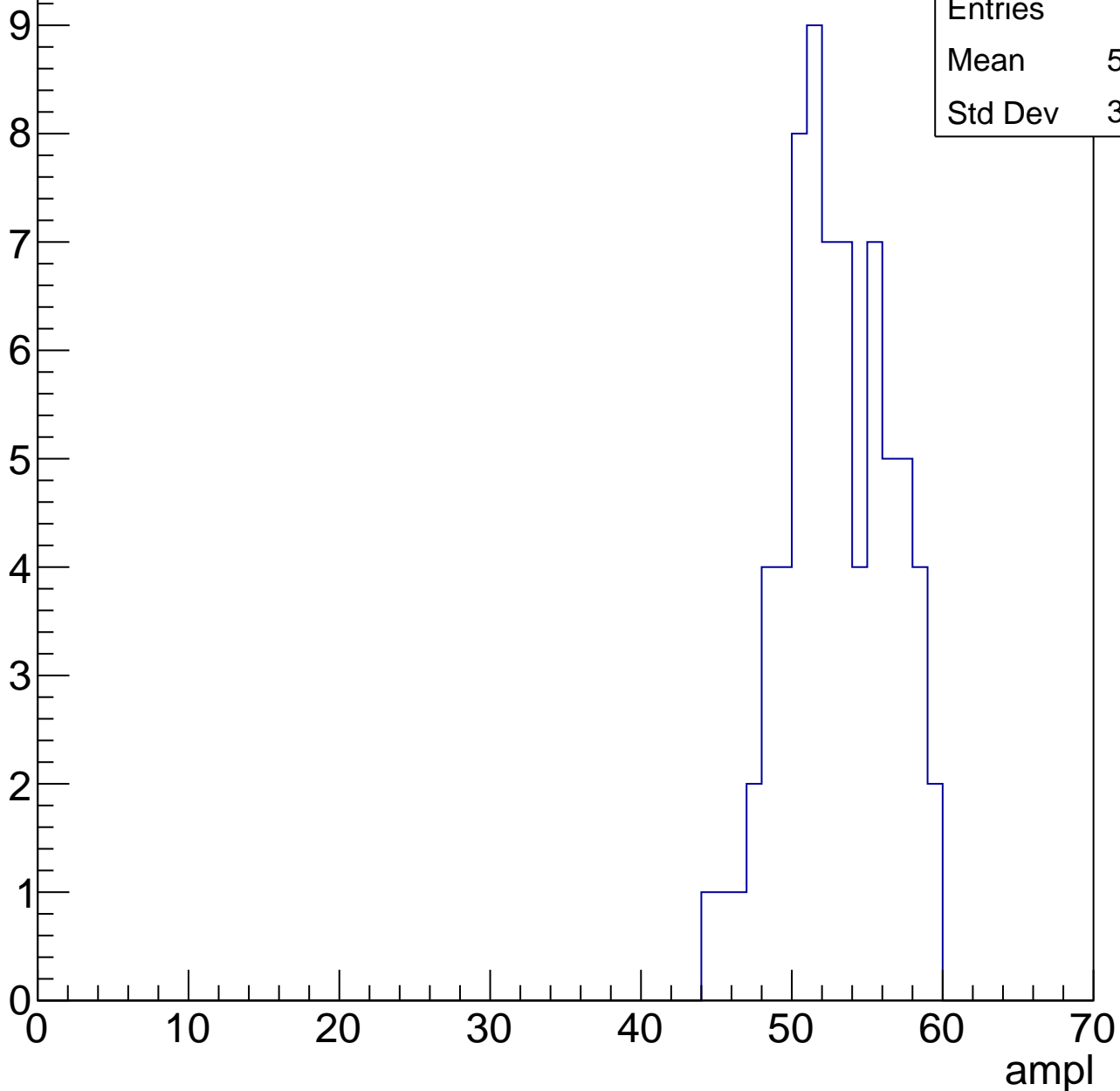


# B0L001S, U5-ch23, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	52.49
Std Dev	3.472

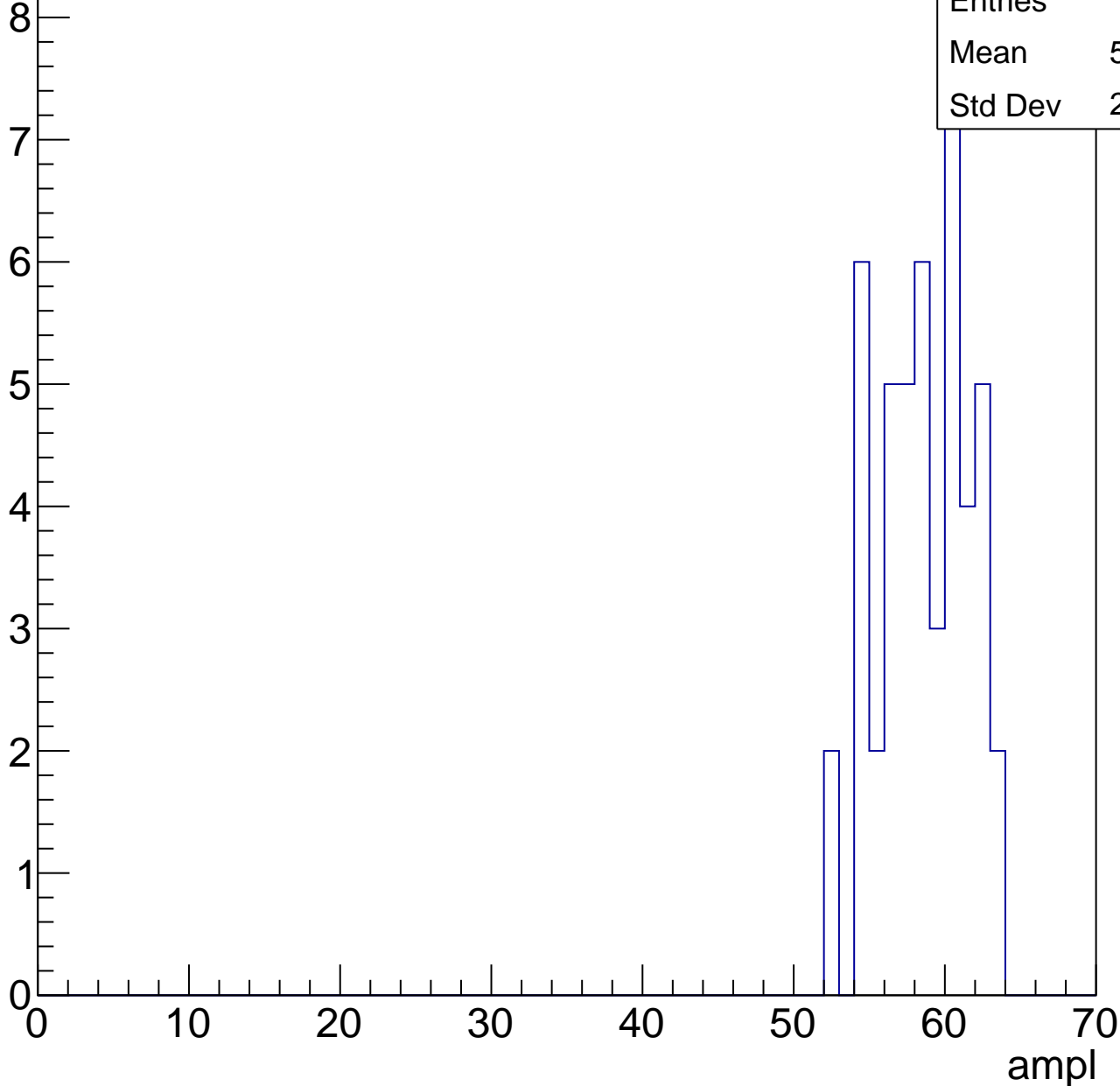


# B0L001S, U5-ch23, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	48
Mean	58.08
Std Dev	2.929

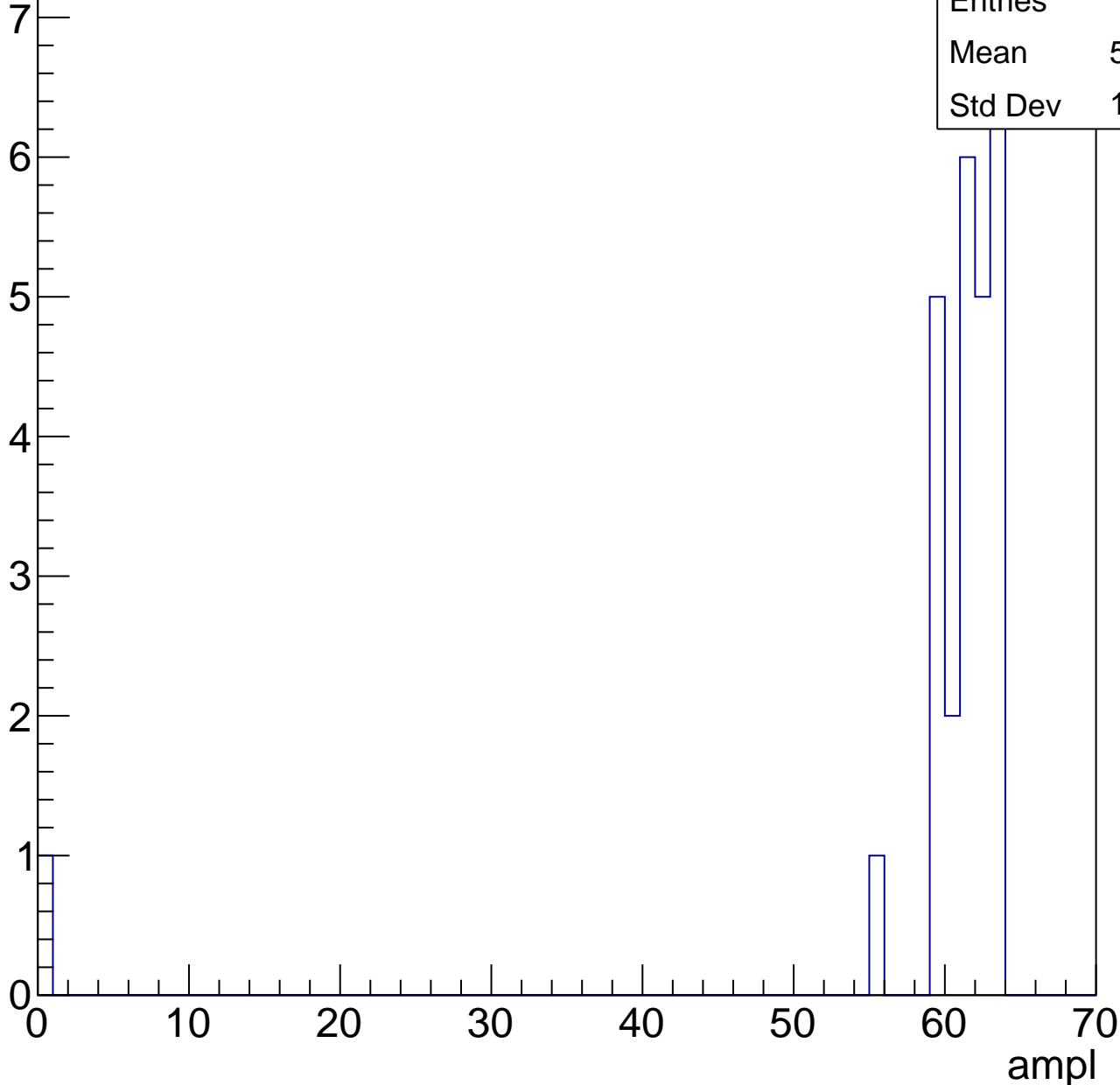


# B0L001S, U5-ch23, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	27
Mean	58.78
Std Dev	11.67



# B0L001S, U5-ch23, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch23, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U5-ch24, adc0

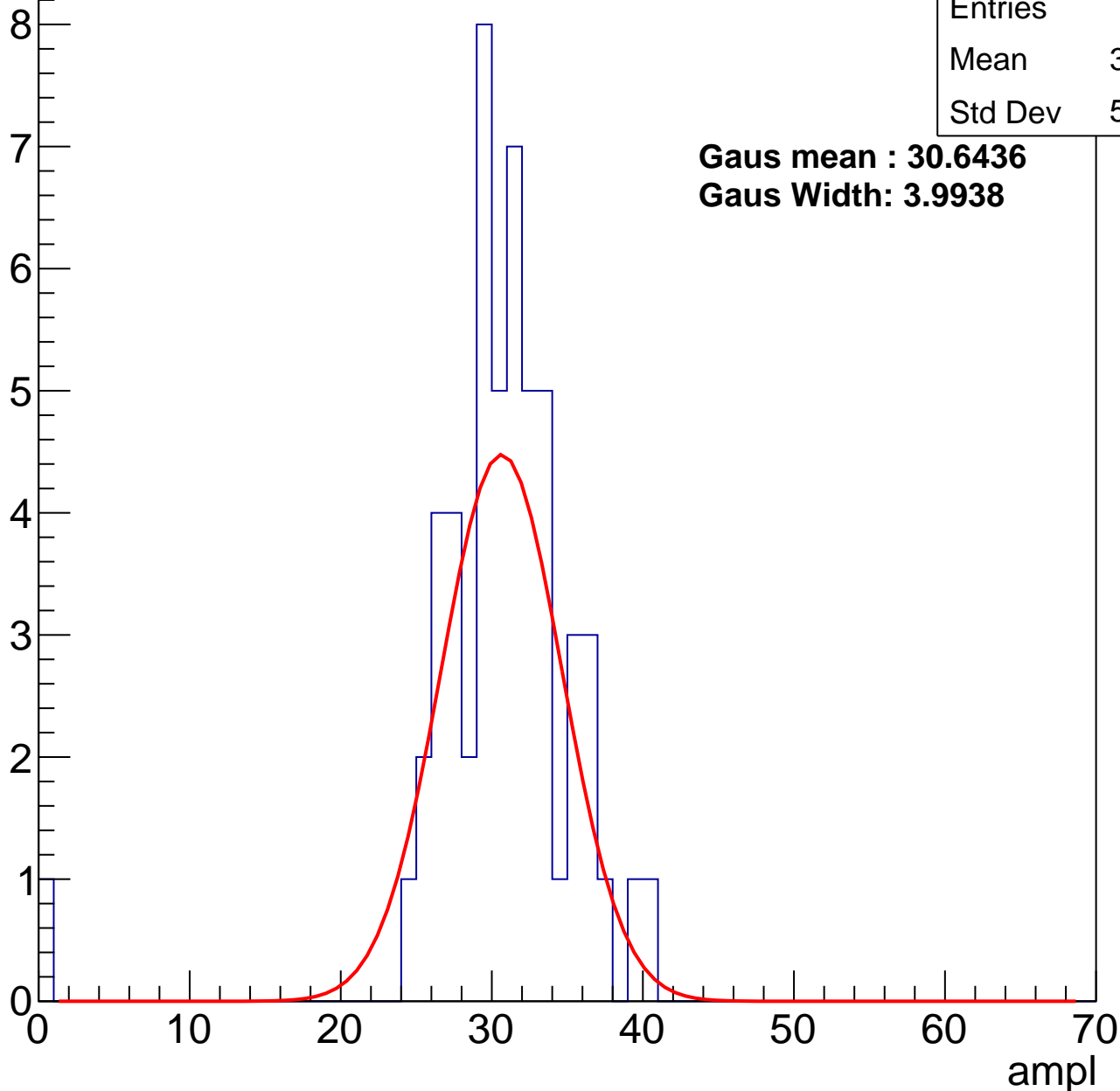
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	30.17
Std Dev	5.446

**Gaus mean : 30.6436**

**Gaus Width: 3.9938**



# B0L001S, U5-ch24, adc1

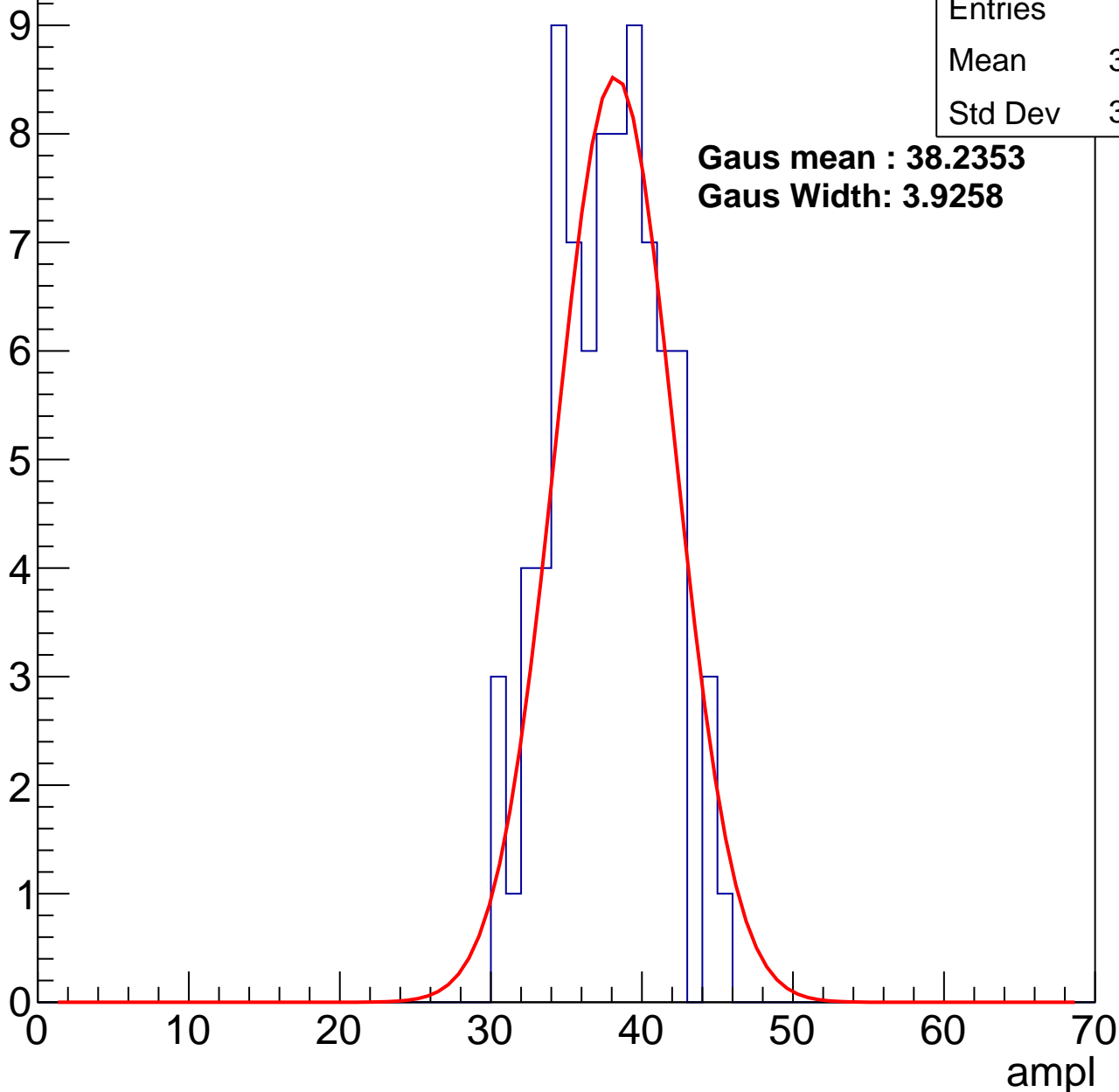
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	82
Mean	37.24
Std Dev	3.529

**Gaus mean : 38.2353**

**Gaus Width: 3.9258**



# B0L001S, U5-ch24, adc2

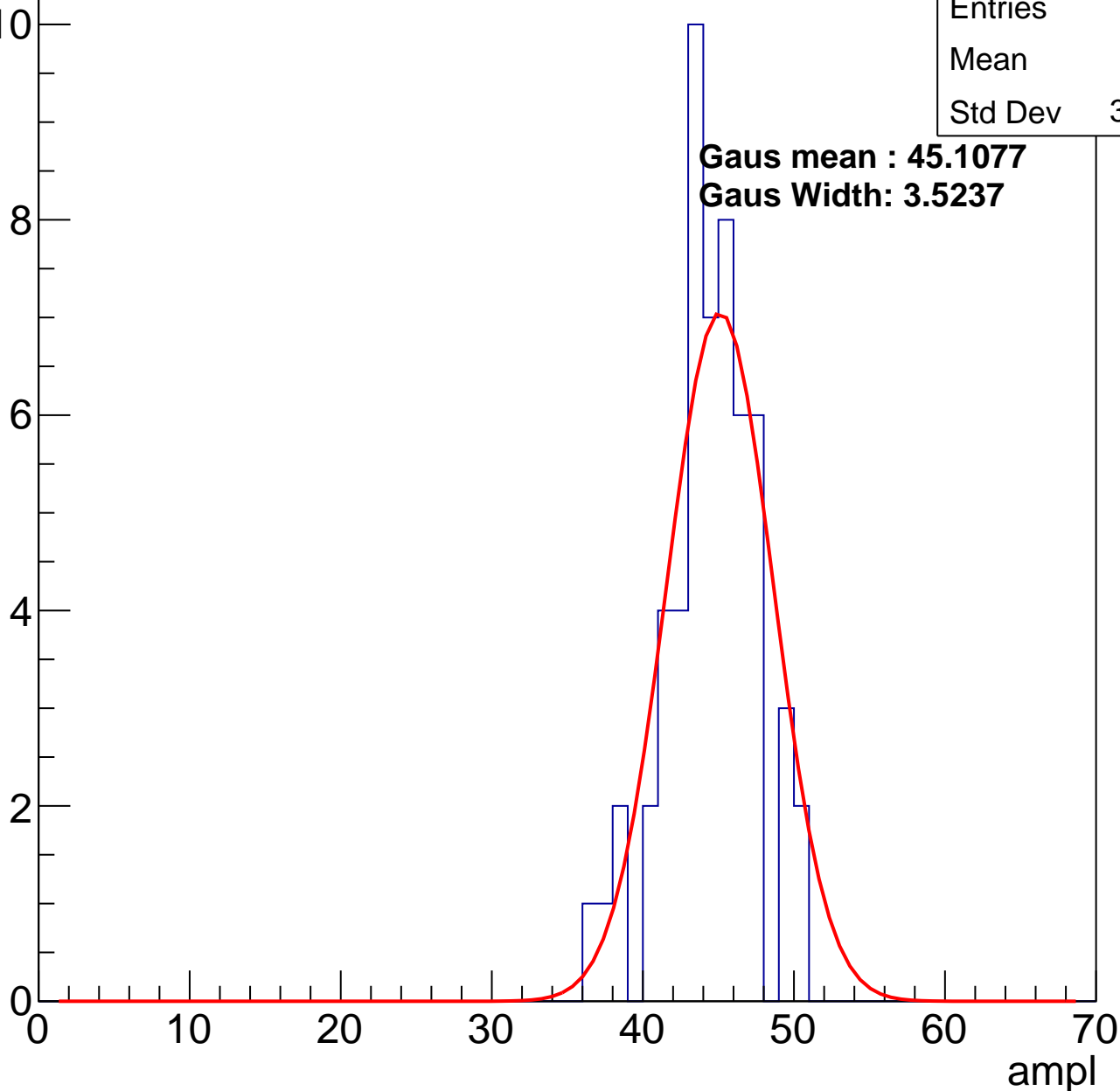
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	44
Std Dev	3.024

**Gaus mean : 45.1077**

**Gaus Width: 3.5237**

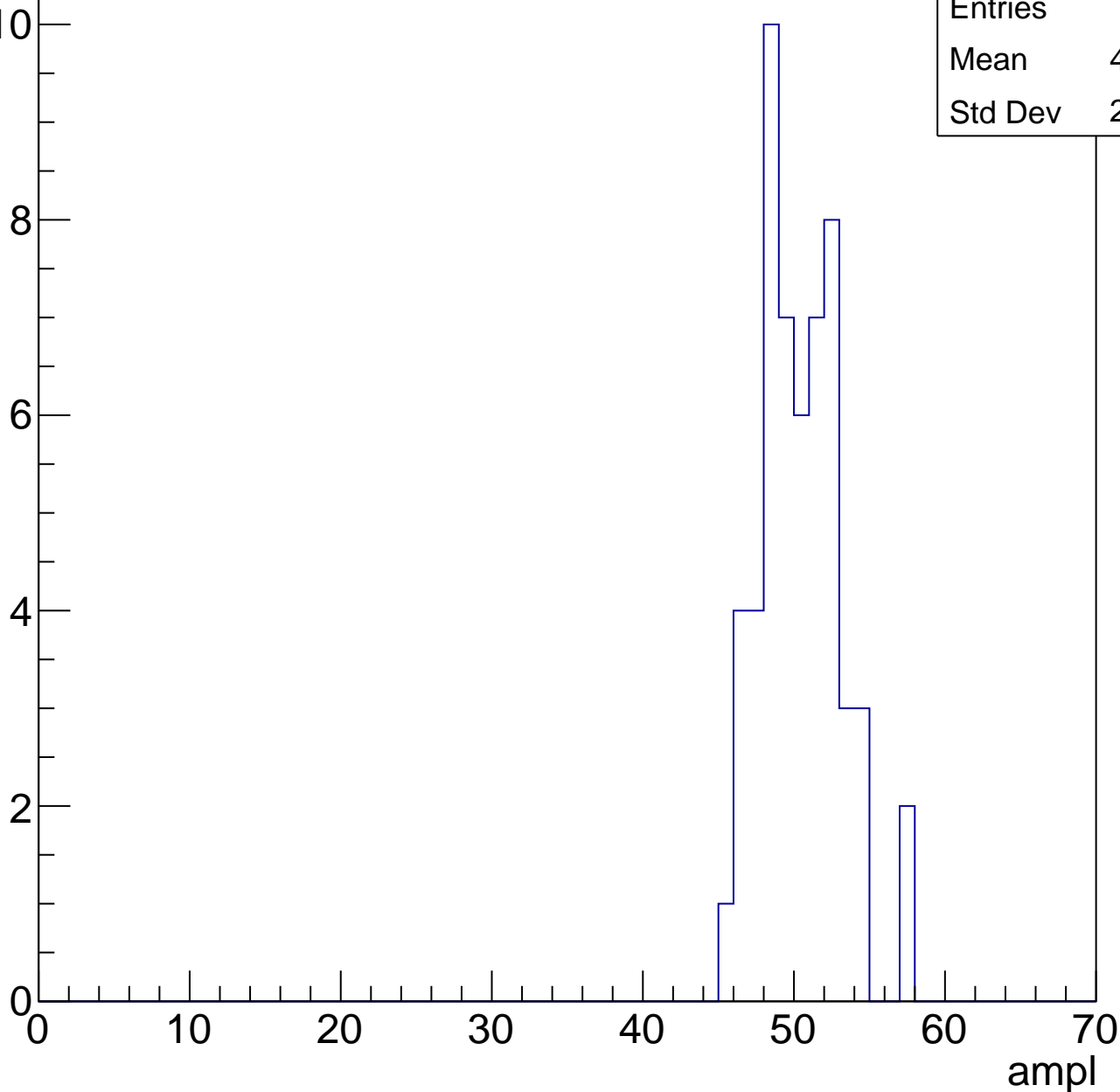


# B0L001S, U5-ch24, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	49.96
Std Dev	2.642

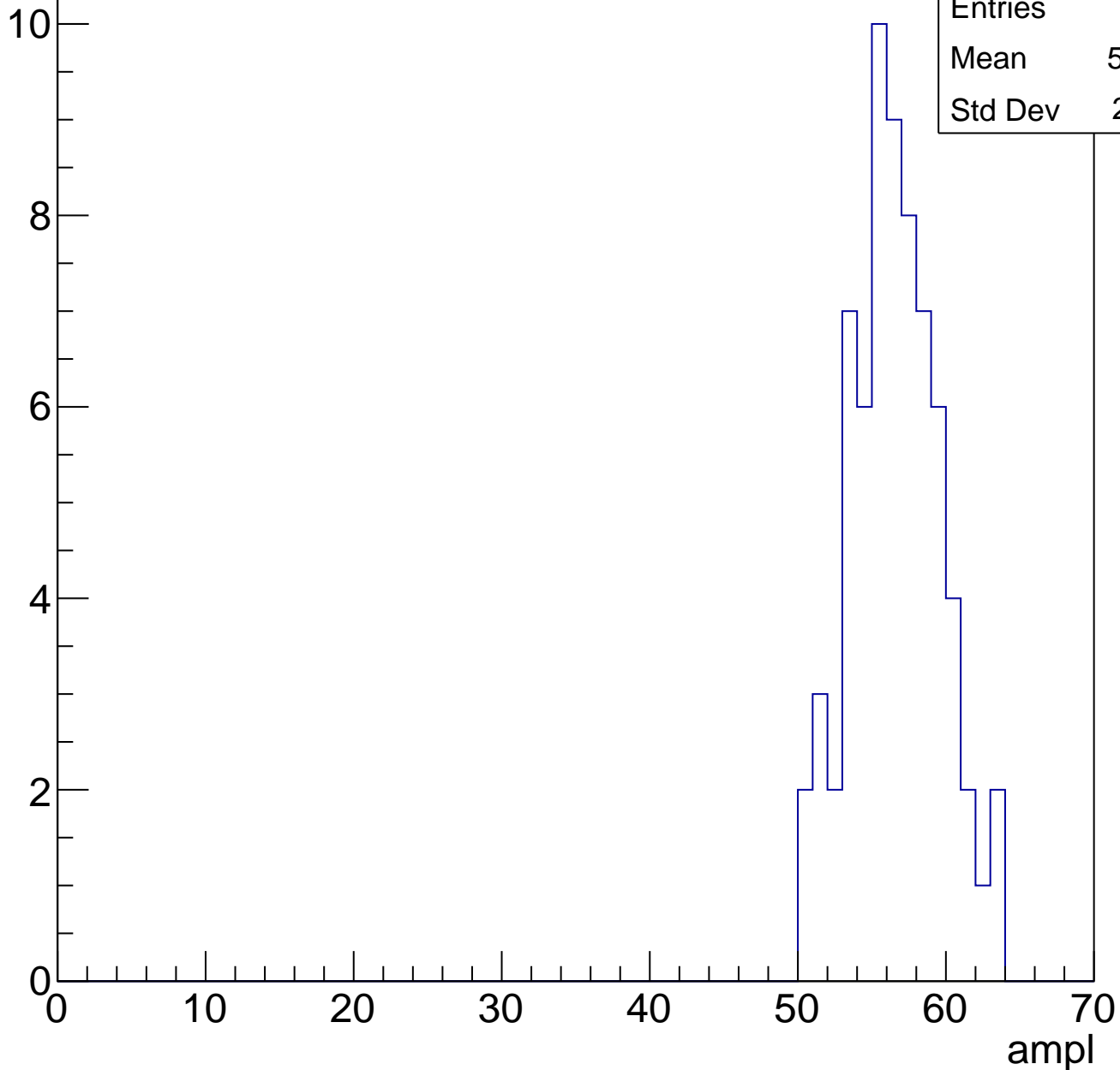


# B0L001S, U5-ch24, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	69
Mean	56.12
Std Dev	2.981

Entry

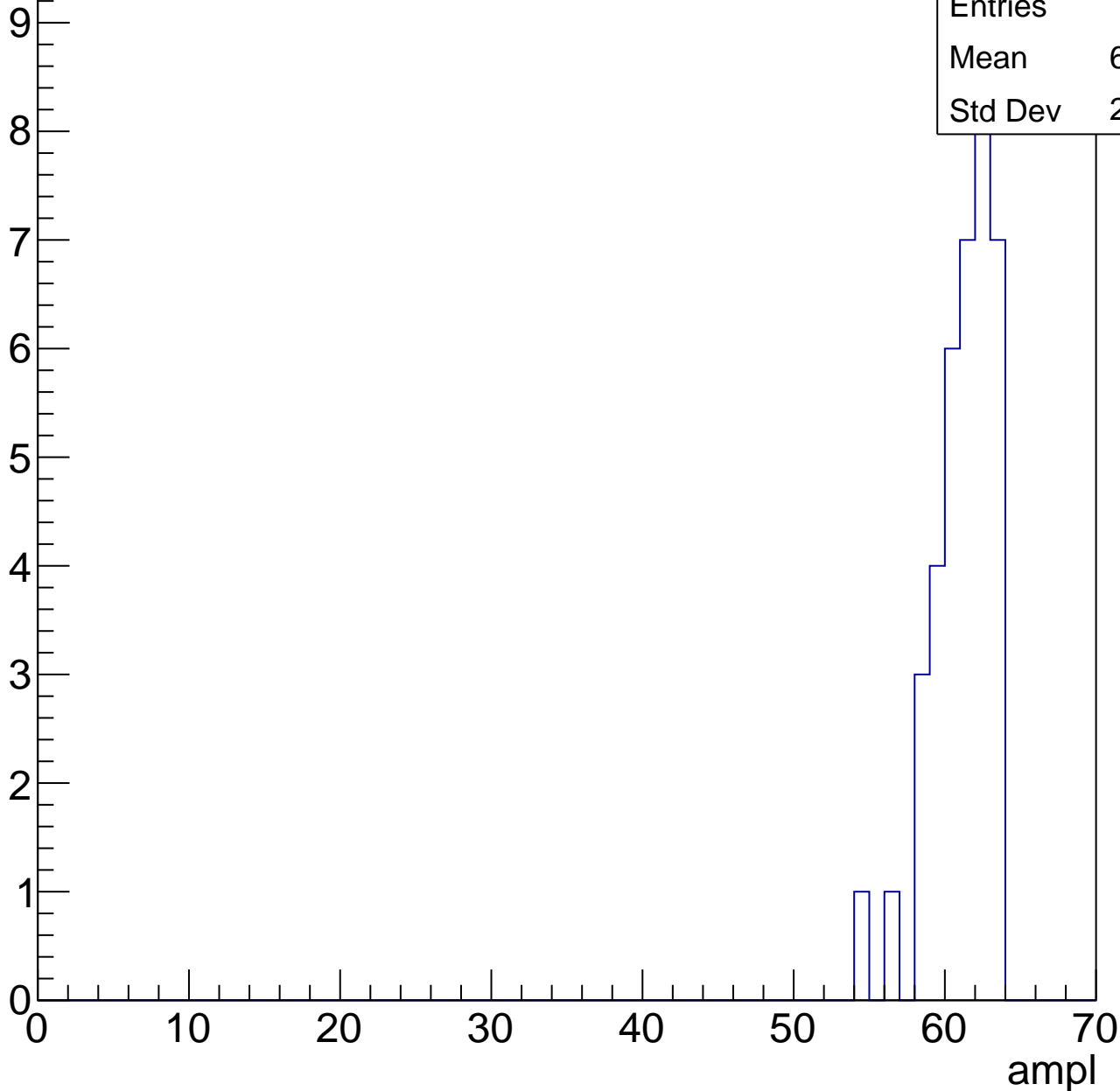


# B0L001S, U5-ch24, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

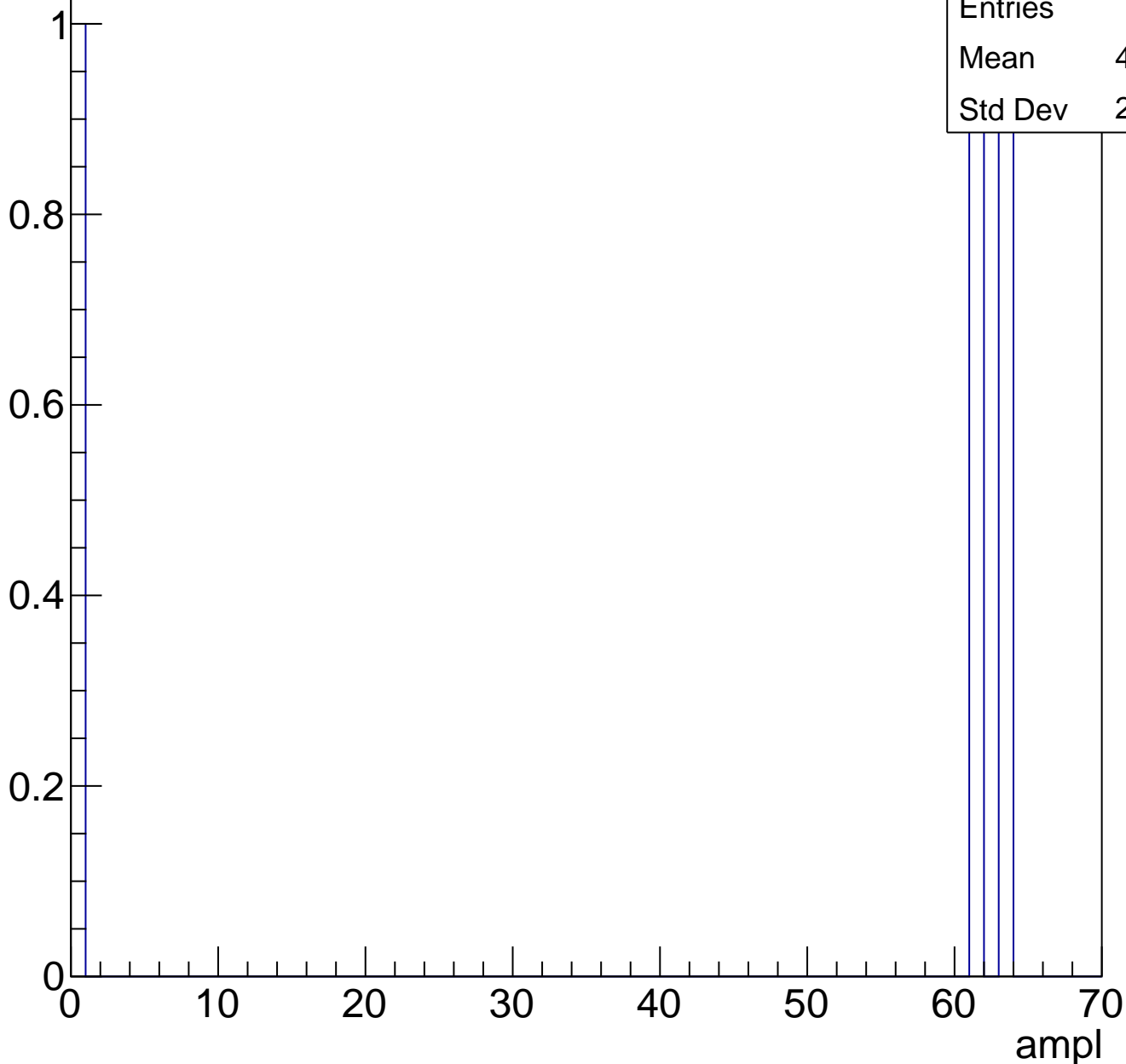
Entries	38
Mean	60.68
Std Dev	2.028



# B0L001S, U5-ch24, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch24, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch25, adc0

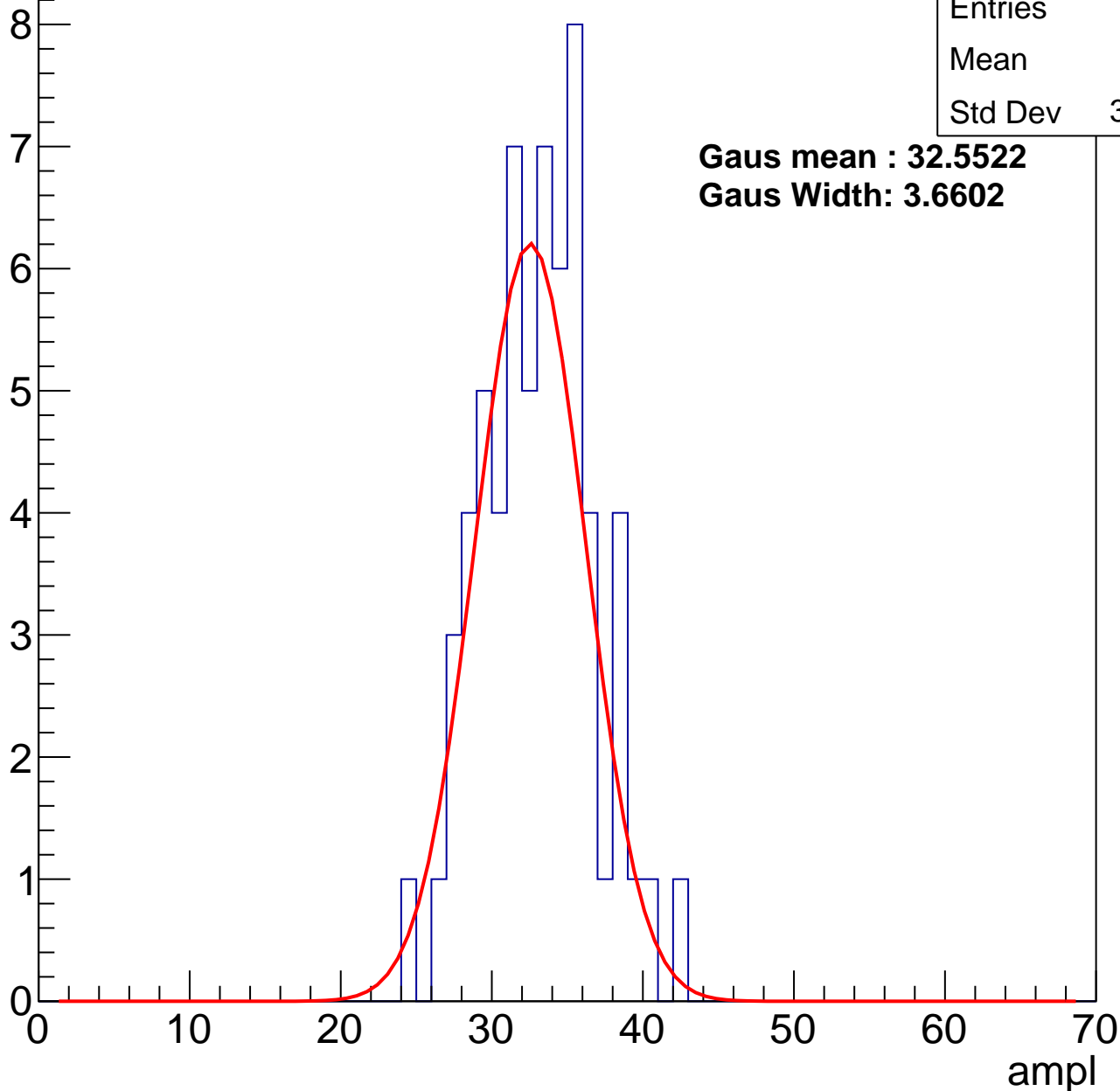
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	32.6
Std Dev	3.636

**Gaus mean : 32.5522**

**Gaus Width: 3.6602**



# B0L001S, U5-ch25, adc1

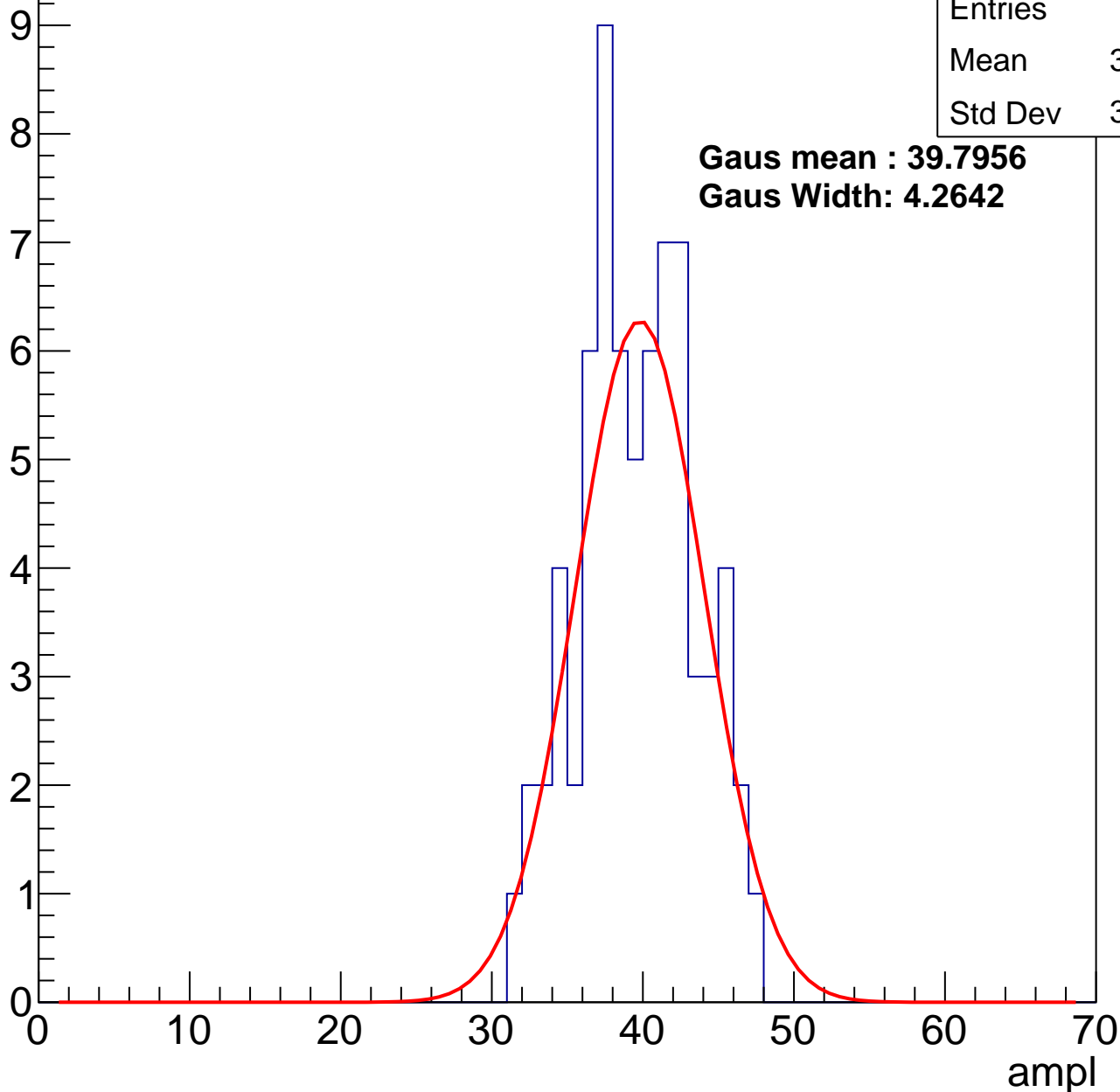
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	39.14
Std Dev	3.754

**Gaus mean : 39.7956**

**Gaus Width: 4.2642**



# B0L001S, U5-ch25, adc2

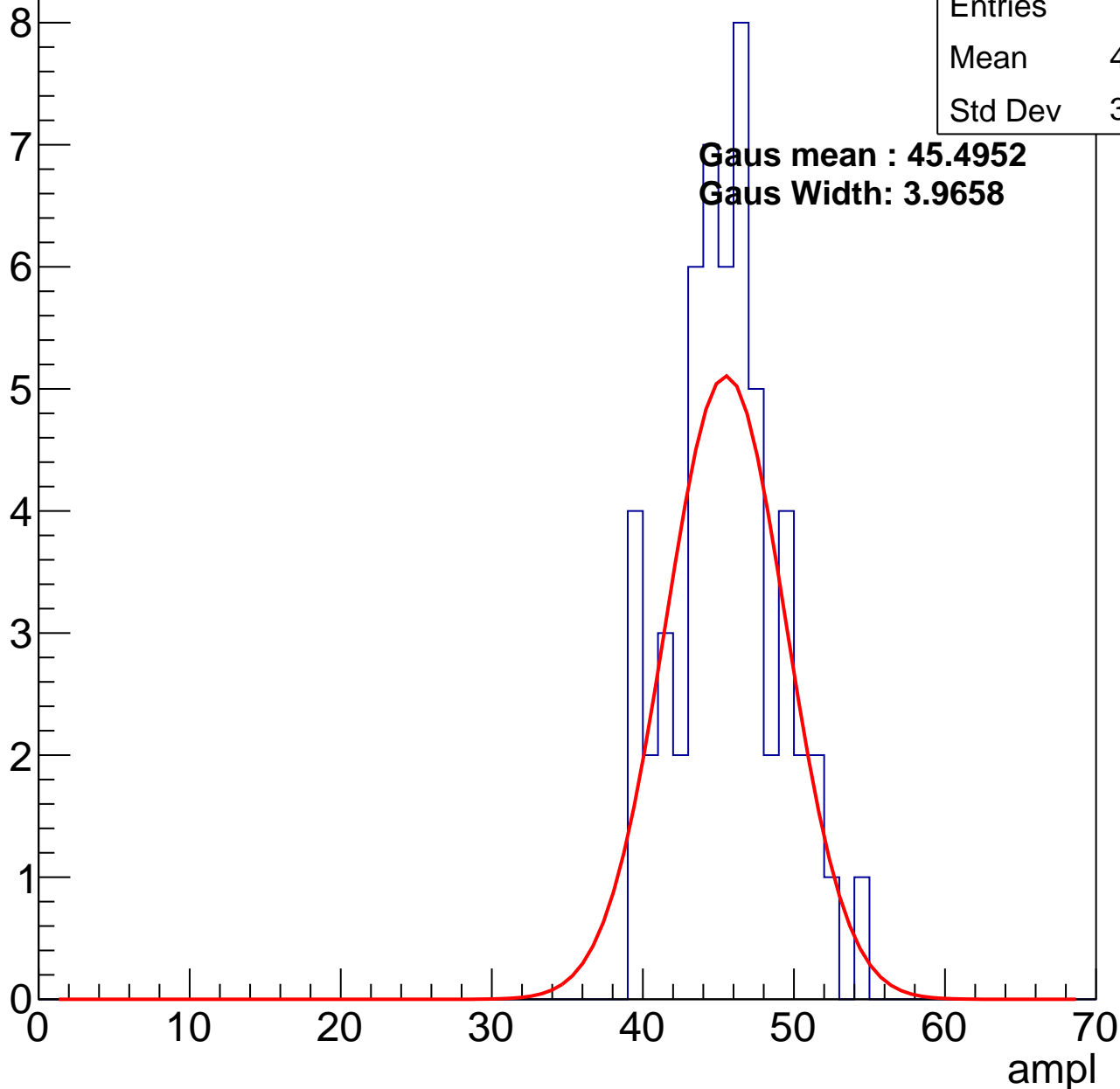
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	45.13
Std Dev	3.443

**Gaus mean : 45.4952**

**Gaus Width: 3.9658**

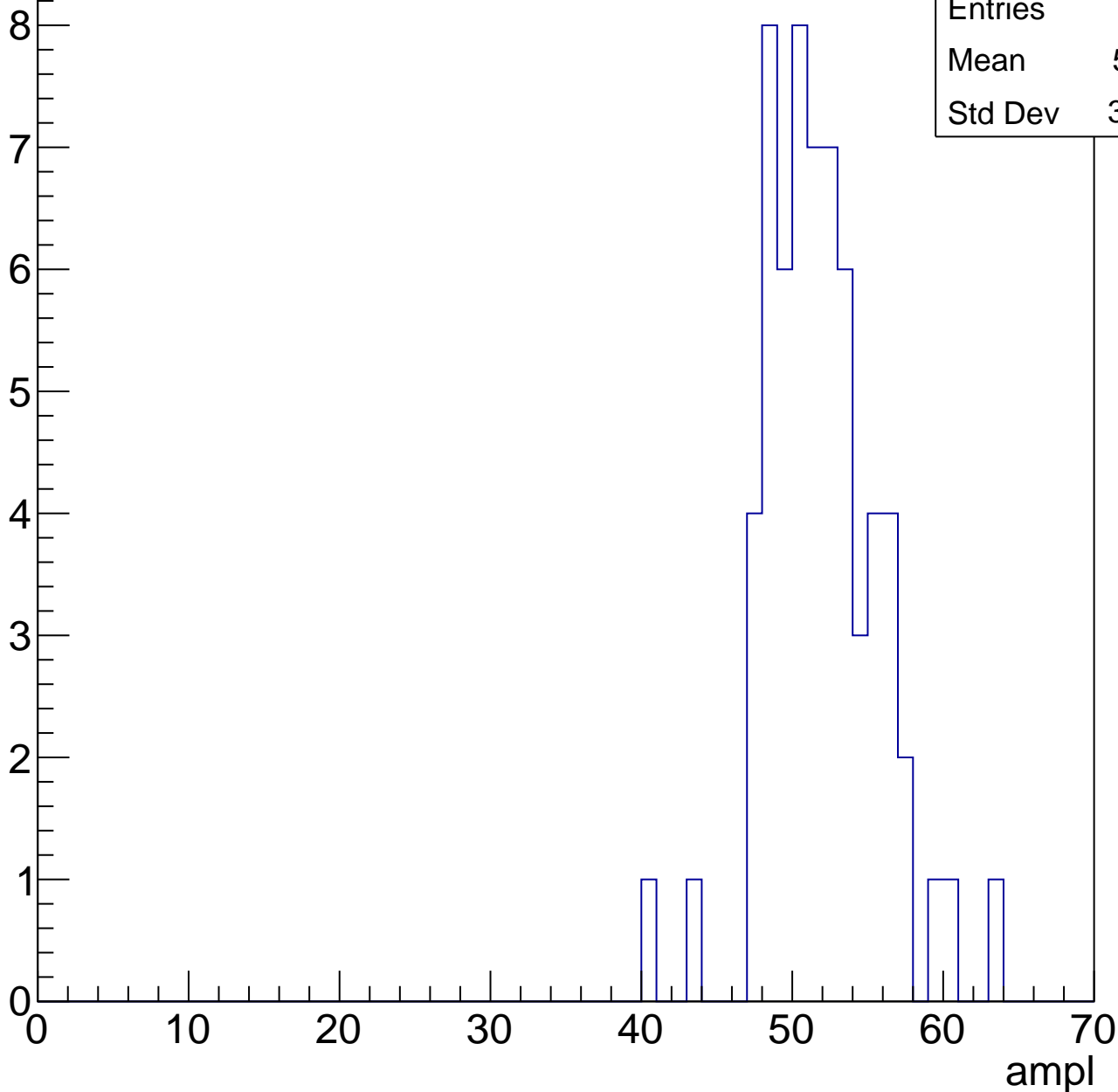


# B0L001S, U5-ch25, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

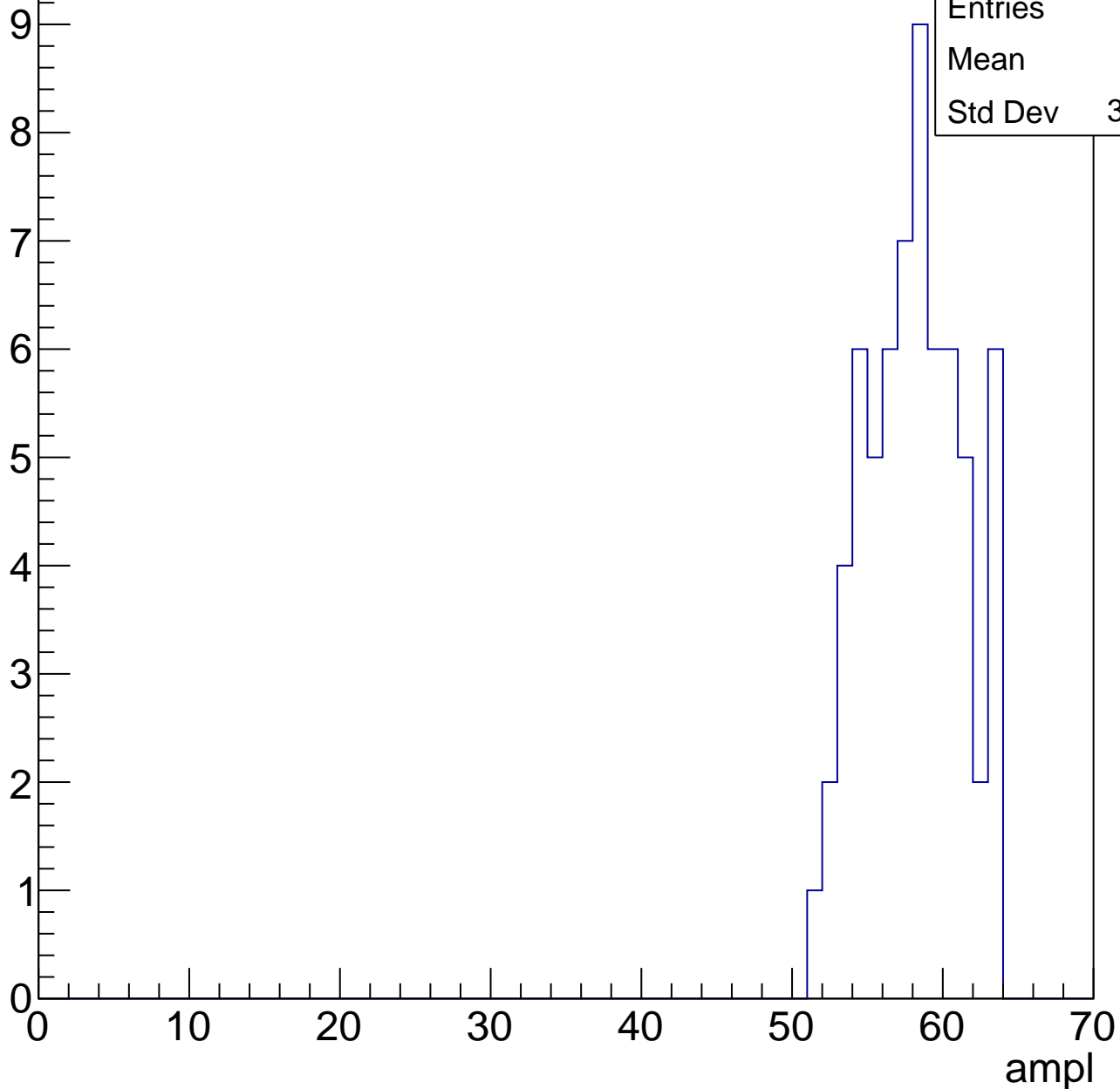
Entries	64
Mean	51.41
Std Dev	3.803



# B0L001S, U5-ch25, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

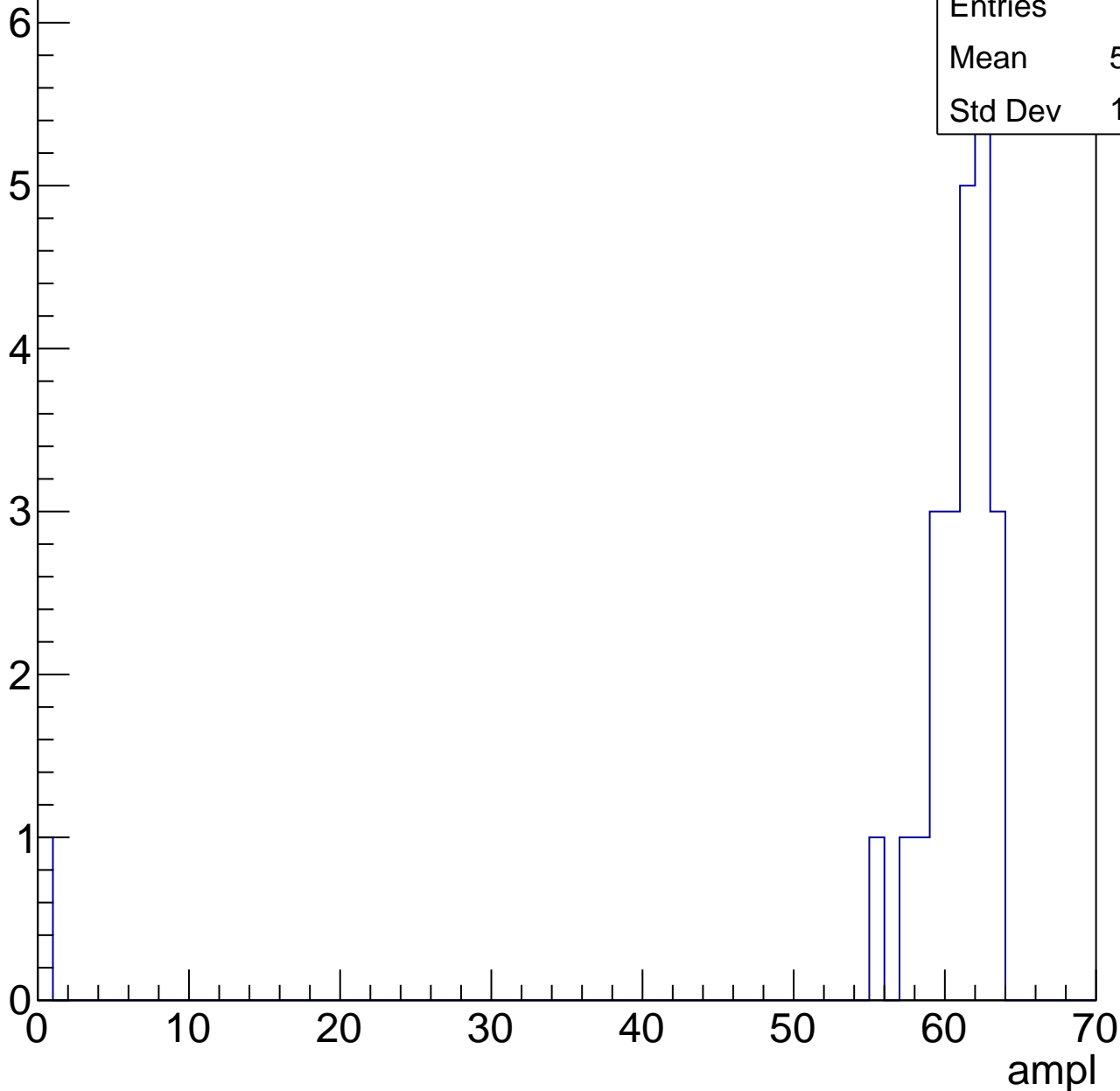


# B0L001S, U5-ch25, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	24
Mean	58.04
Std Dev	12.26



# B0L001S, U5-ch25, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch25, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U5-ch26, adc0

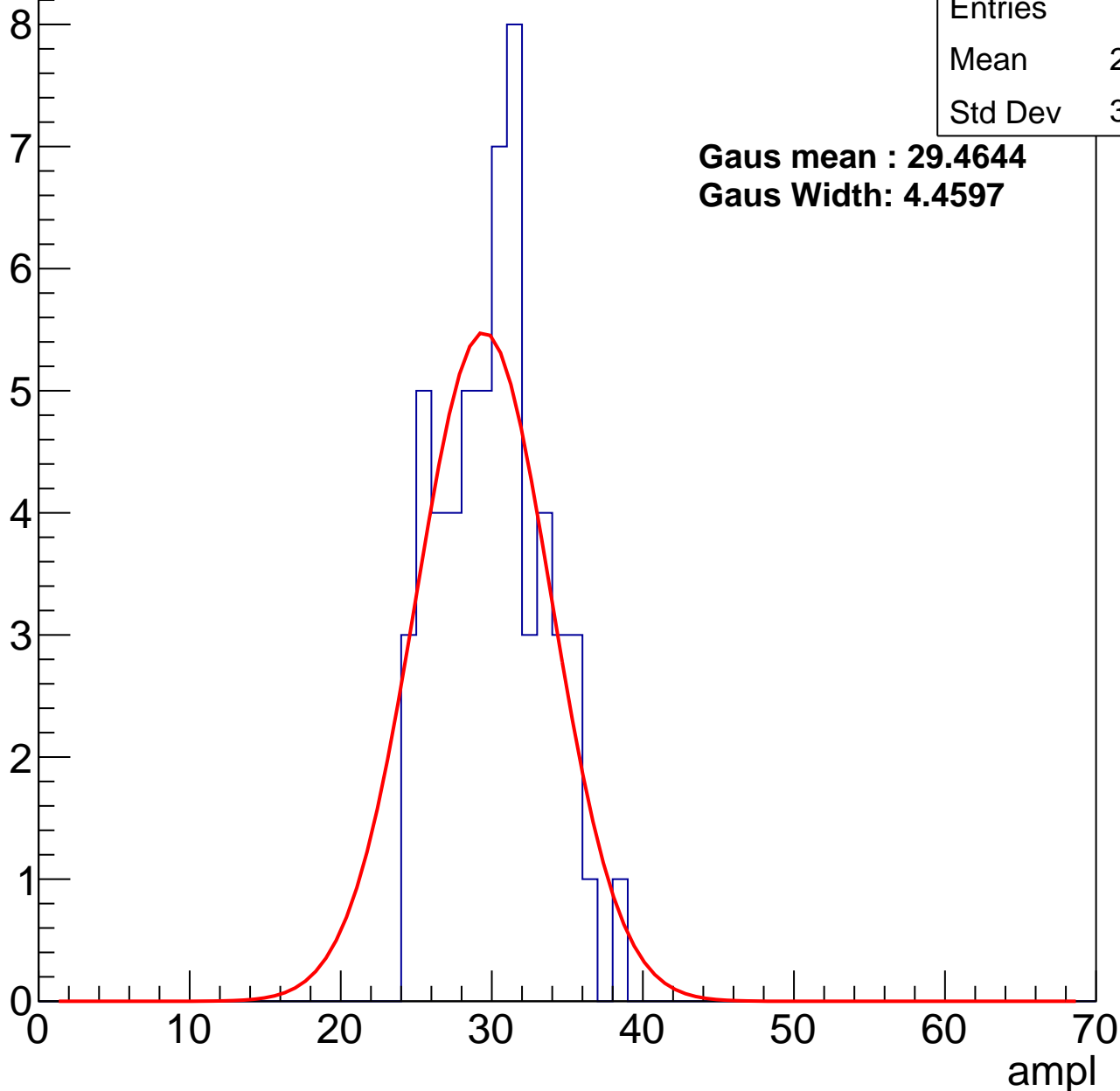
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	29.66
Std Dev	3.356

**Gaus mean : 29.4644**

**Gaus Width: 4.4597**



# B0L001S, U5-ch26, adc1

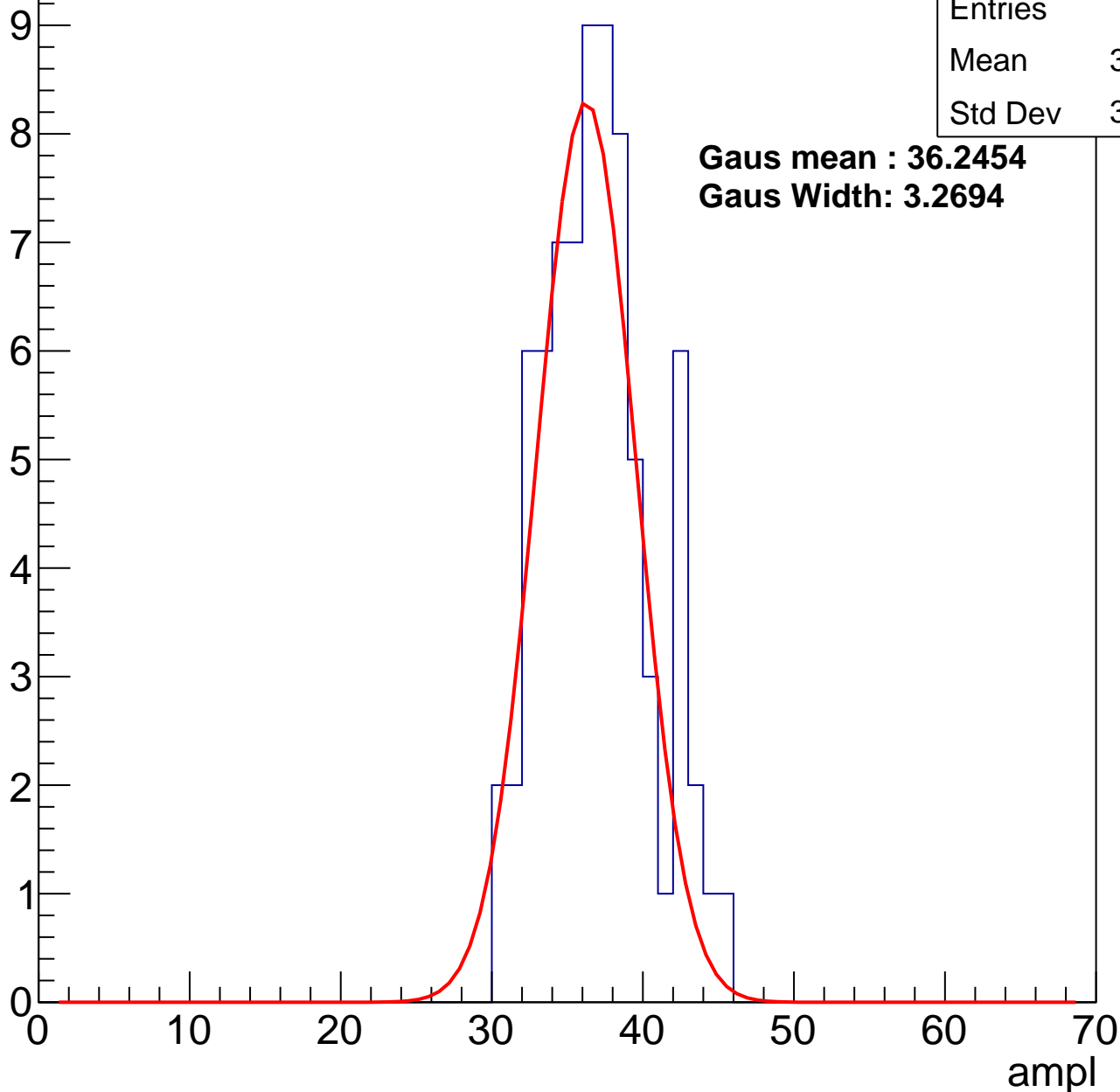
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	75
Mean	36.52
Std Dev	3.473

**Gaus mean : 36.2454**

**Gaus Width: 3.2694**



# B0L001S, U5-ch26, adc2

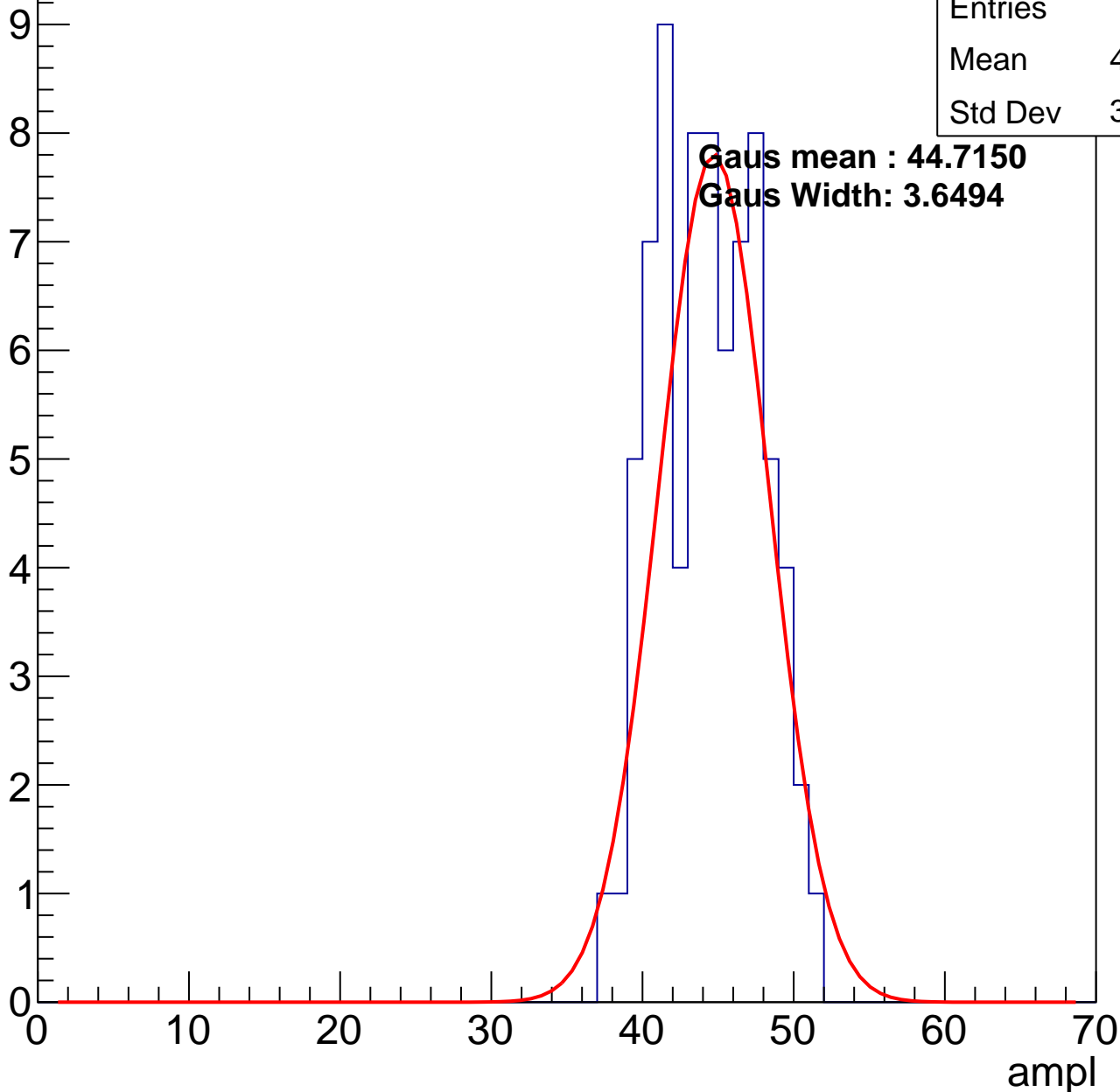
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	76
Mean	43.92
Std Dev	3.312

**Gaus mean : 44.7150**

**Gaus Width: 3.6494**

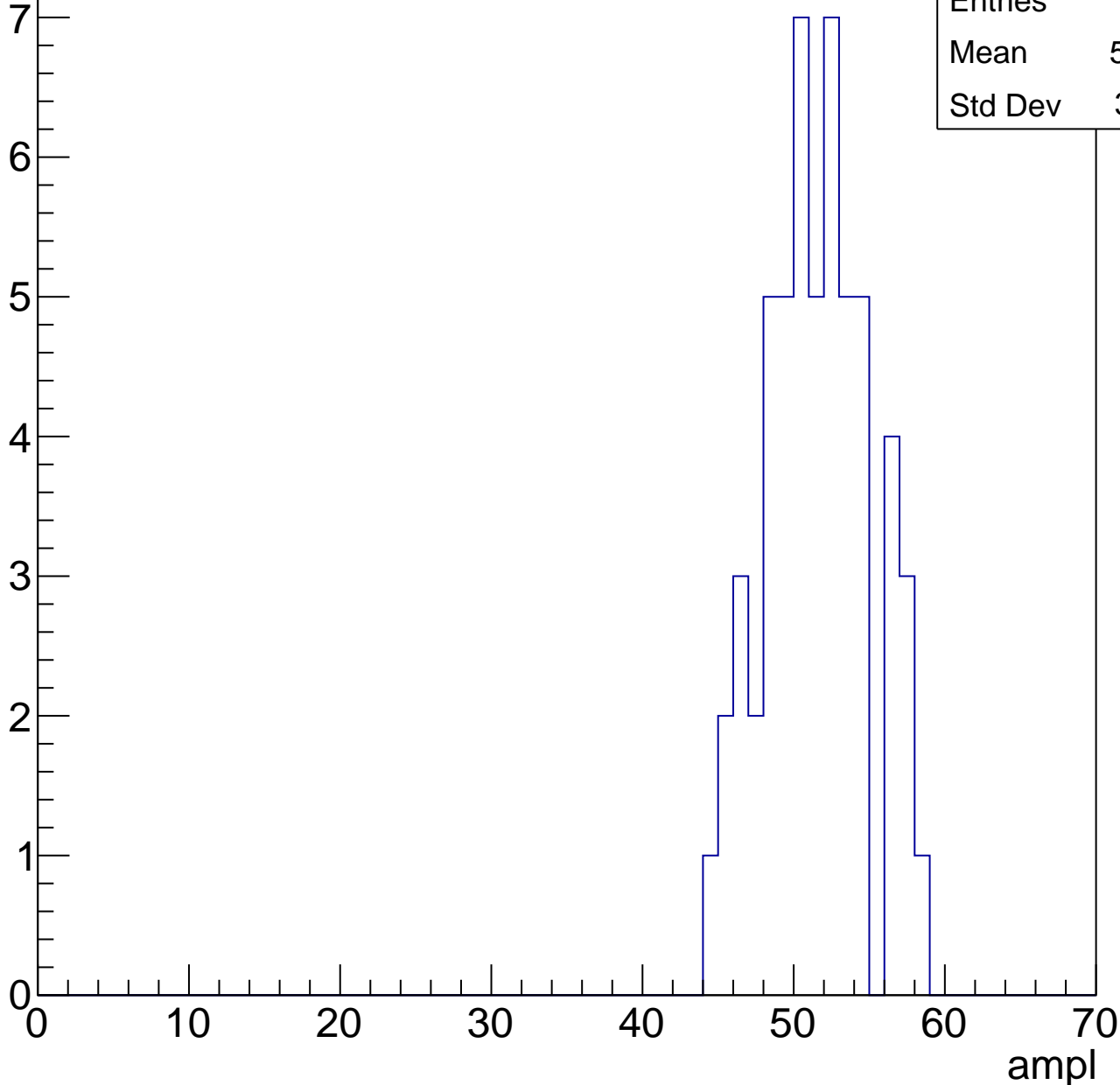


# B0L001S, U5-ch26, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	51.05
Std Dev	3.381

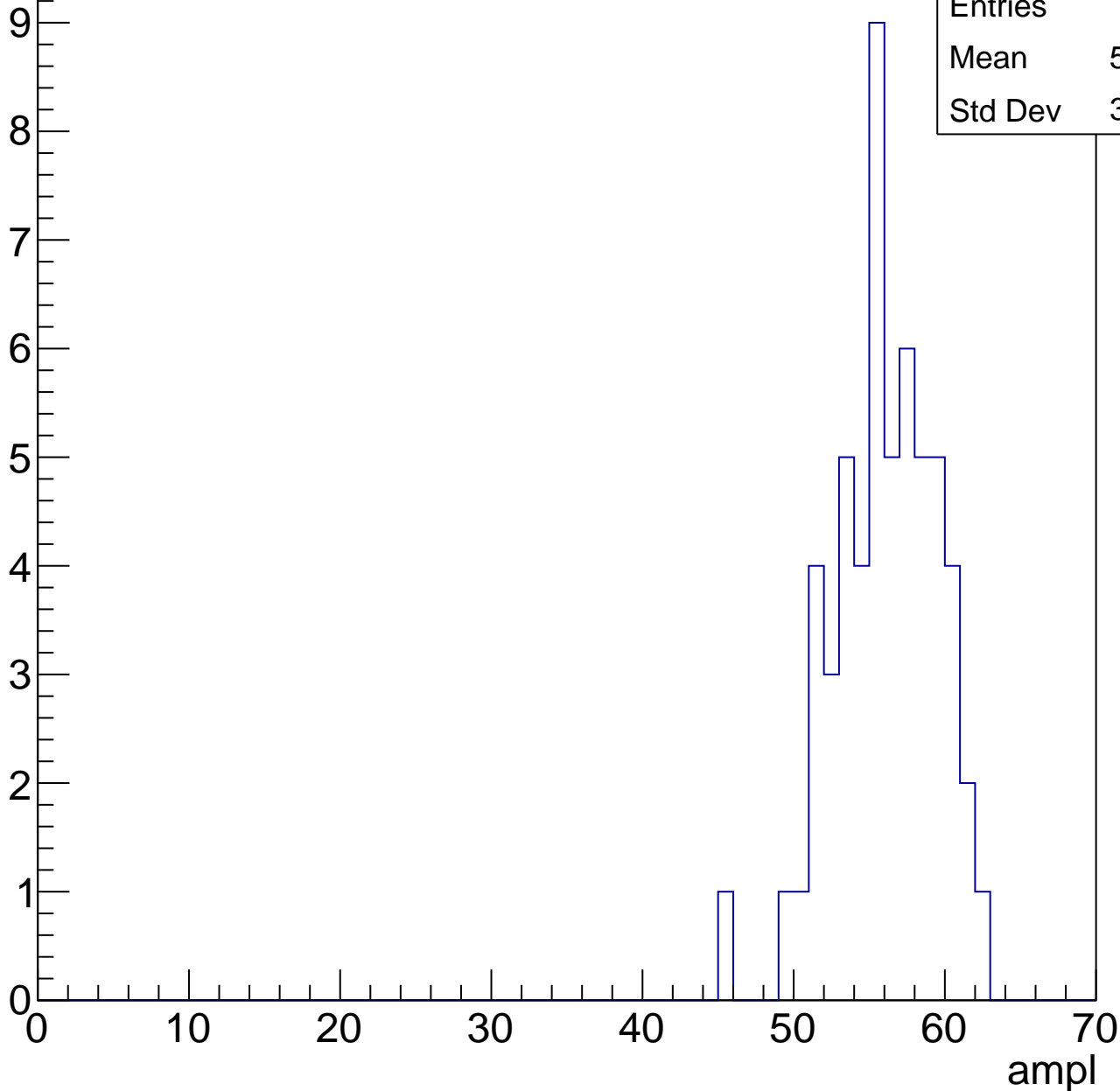


# B0L001S, U5-ch26, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	55.55
Std Dev	3.364

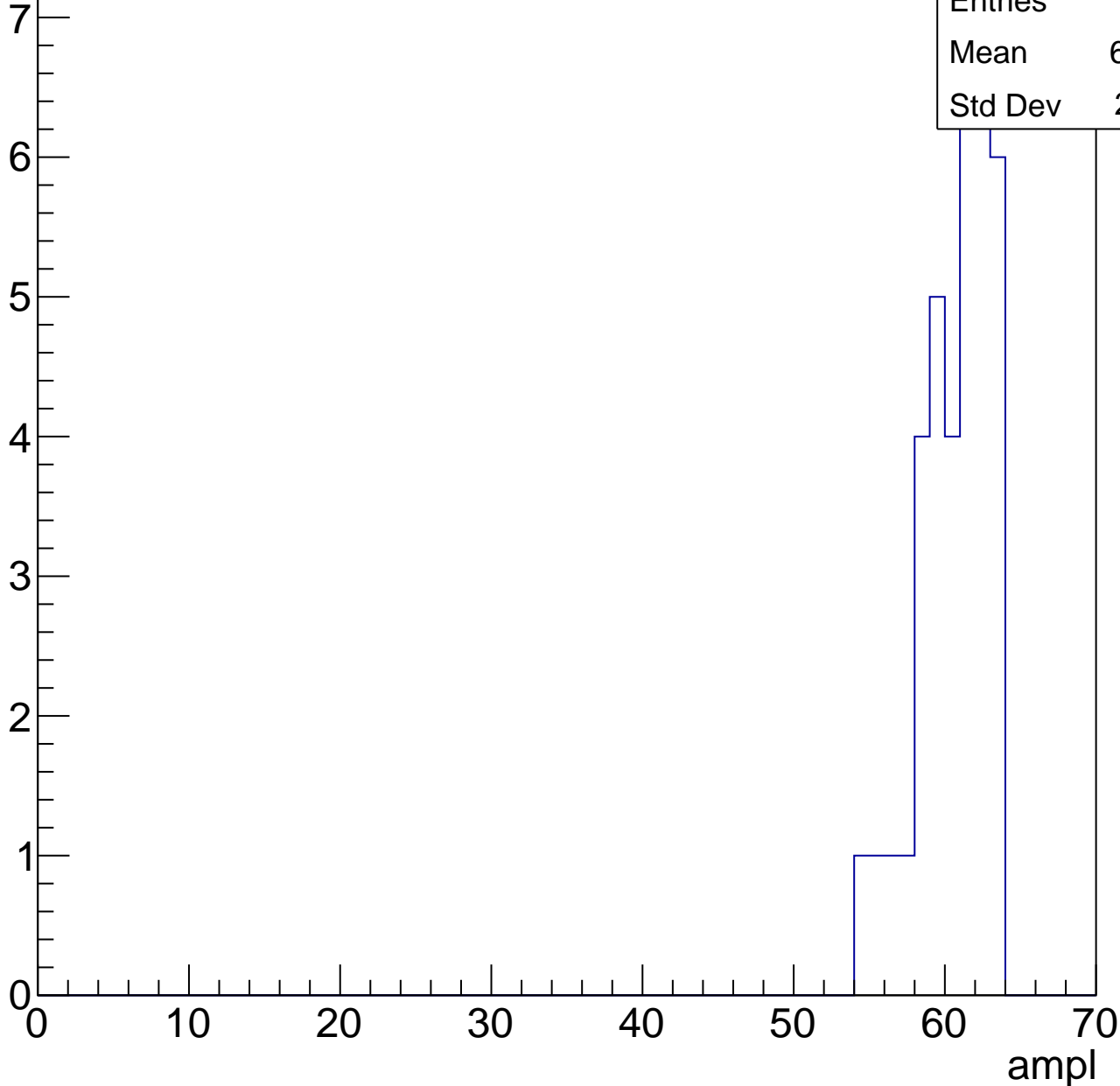


# B0L001S, U5-ch26, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

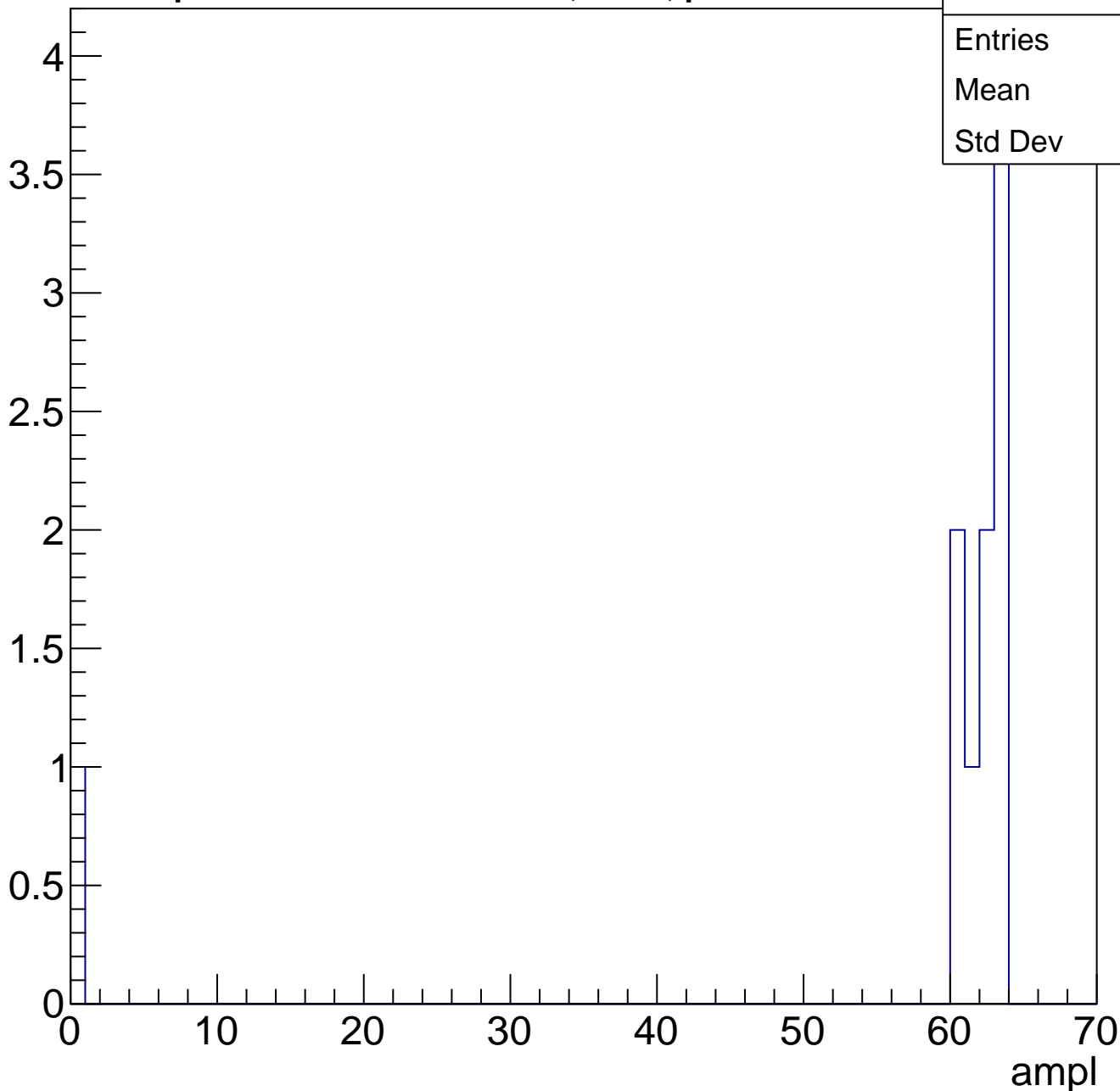
Entries	37
Mean	60.22
Std Dev	2.291



# B0L001S, U5-ch26, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch26, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U5-ch27, adc0

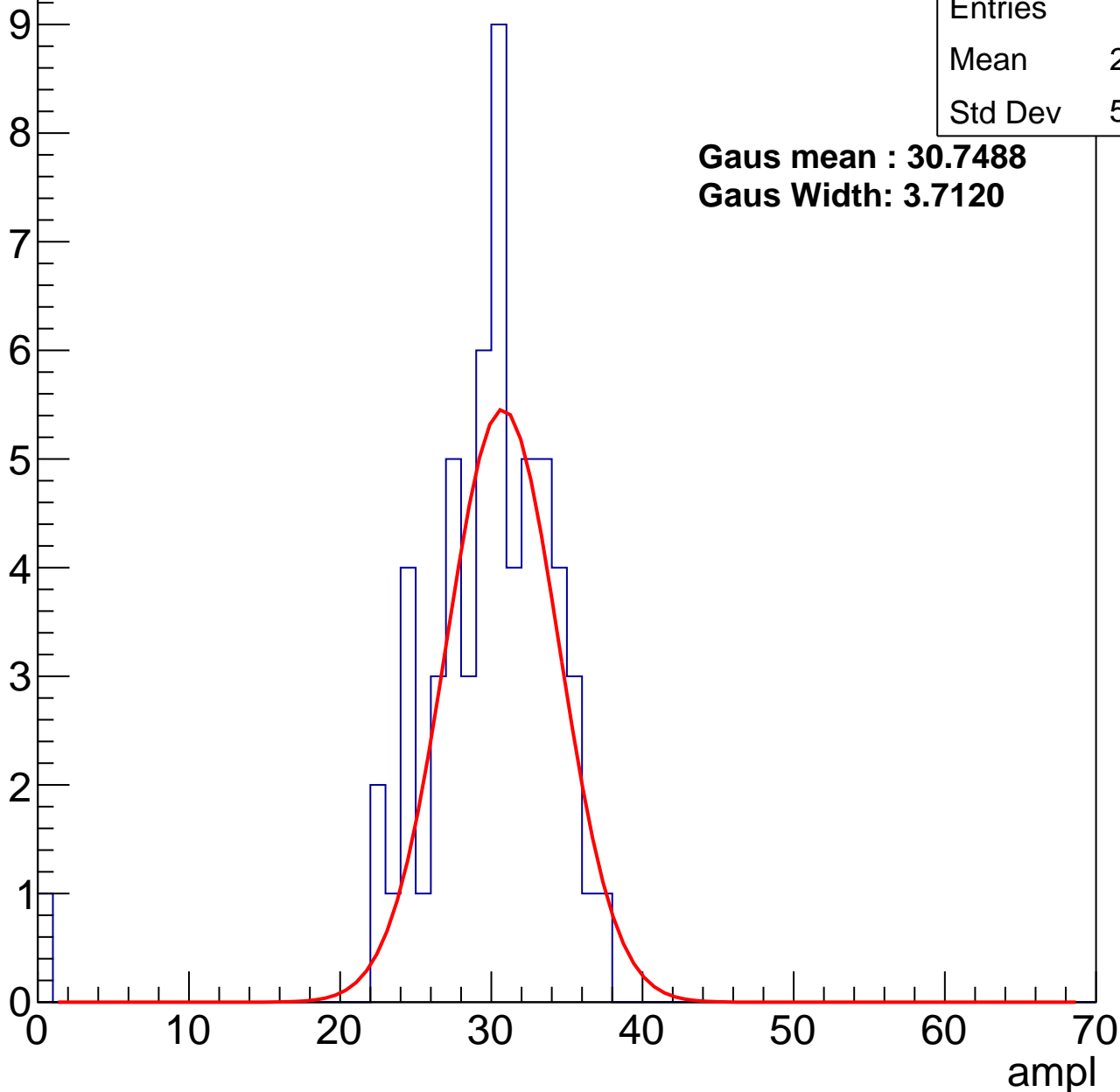
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	29.17
Std Dev	5.269

**Gaus mean : 30.7488**

**Gaus Width: 3.7120**



# B0L001S, U5-ch27, adc1

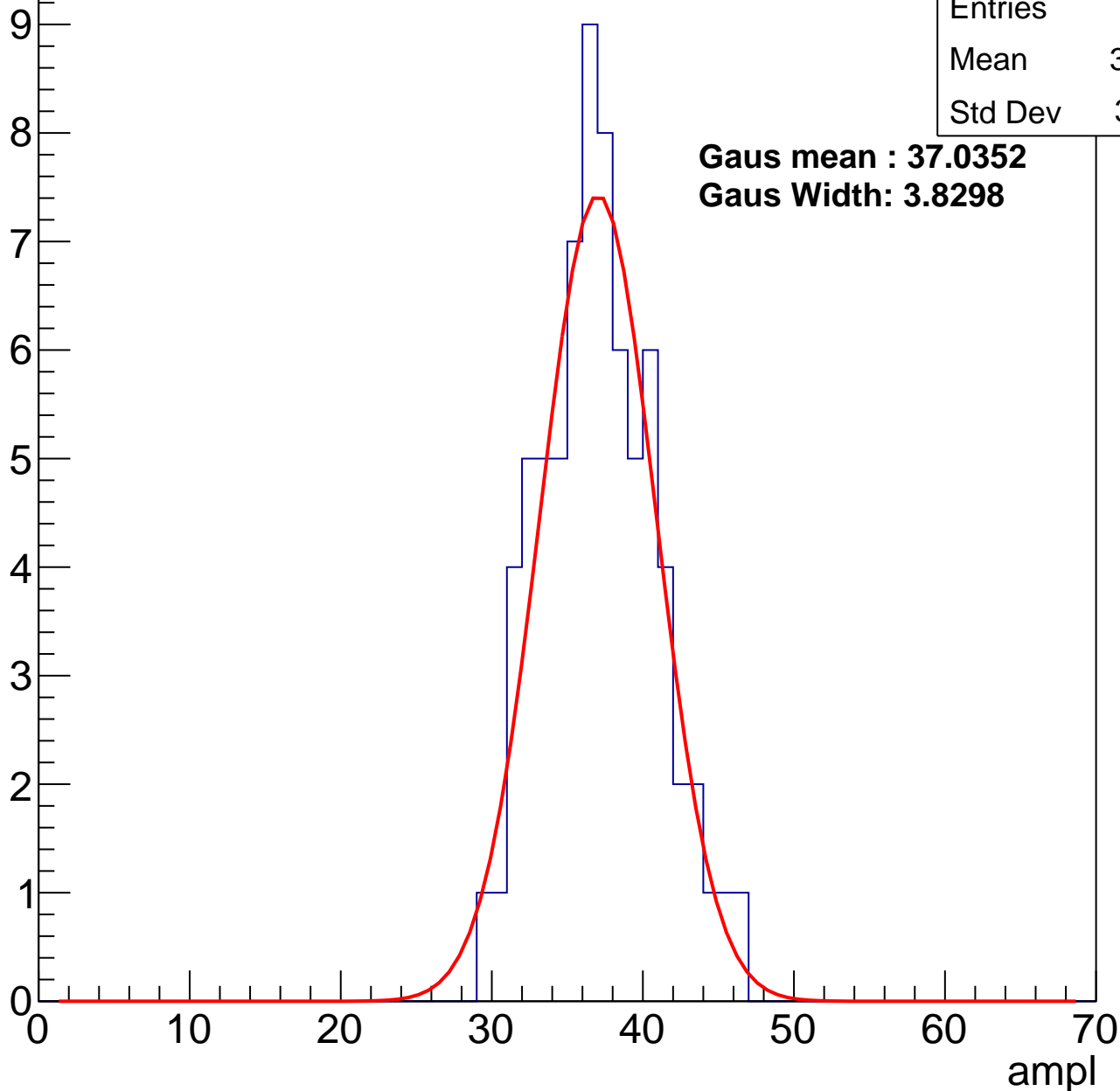
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	36.64
Std Dev	3.691

**Gaus mean : 37.0352**

**Gaus Width: 3.8298**



# B0L001S, U5-ch27, adc2

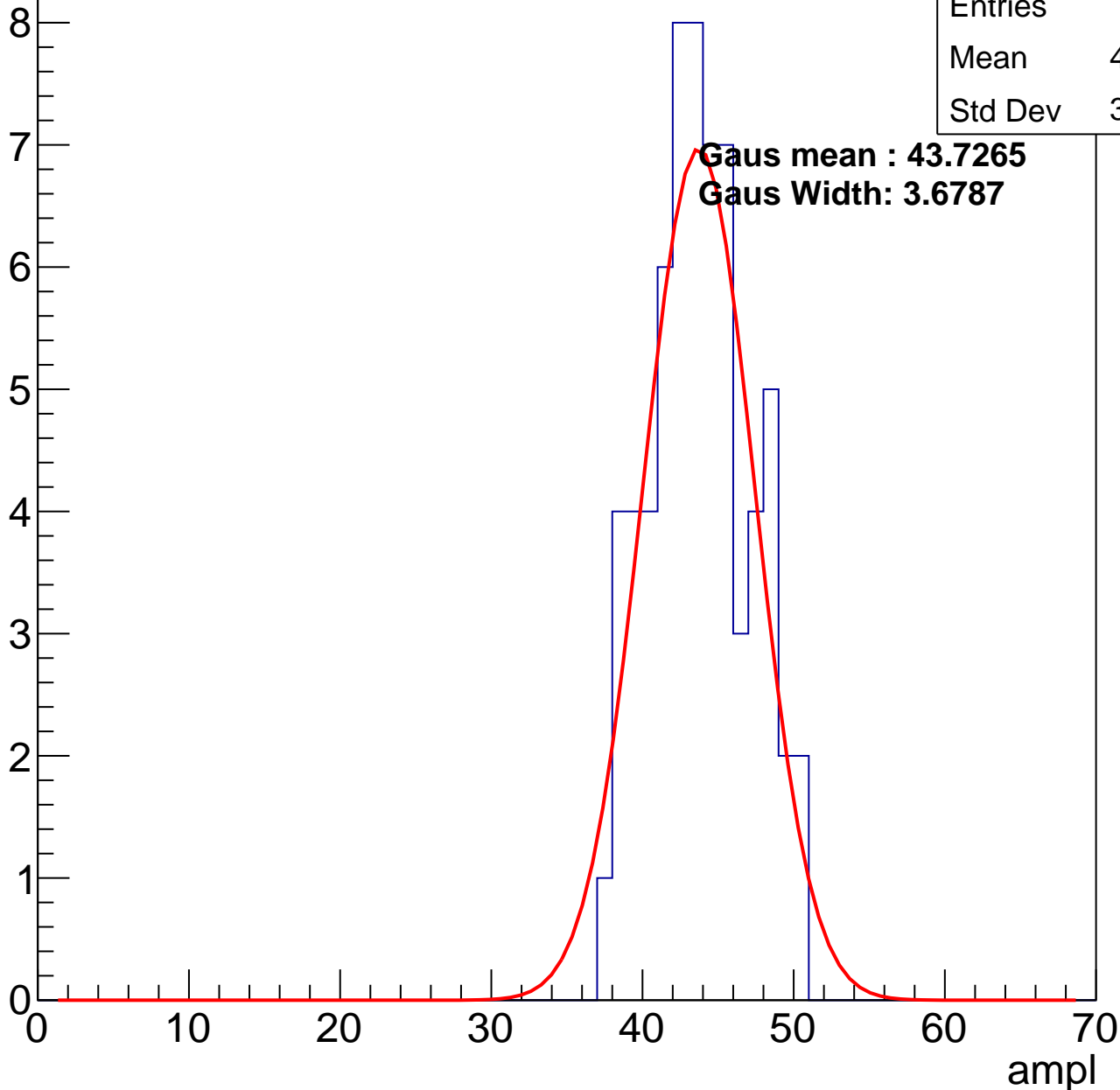
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	43.35
Std Dev	3.236

**Gaus mean : 43.7265**

**Gaus Width: 3.6787**

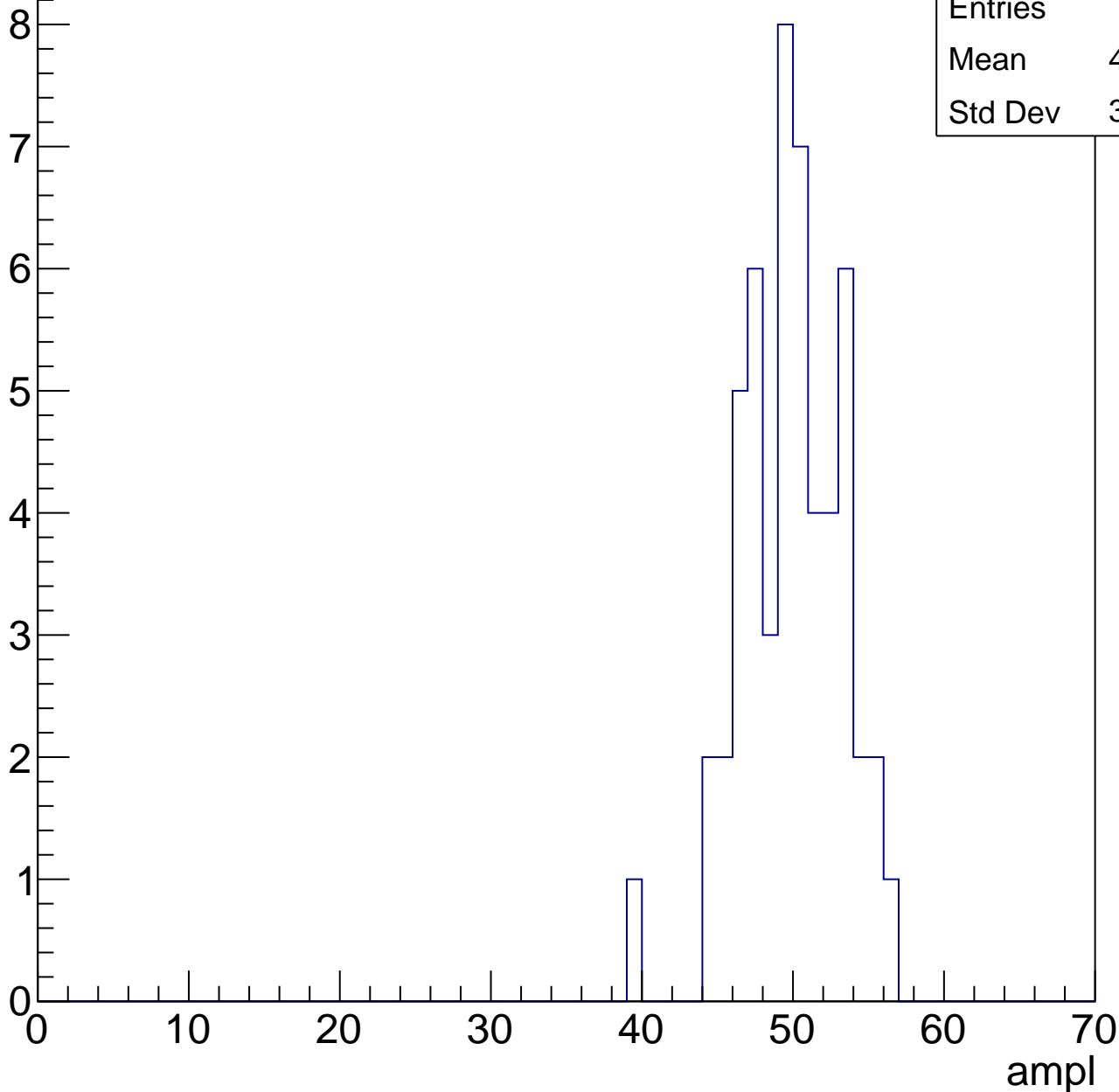


# B0L001S, U5-ch27, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	49.42
Std Dev	3.282

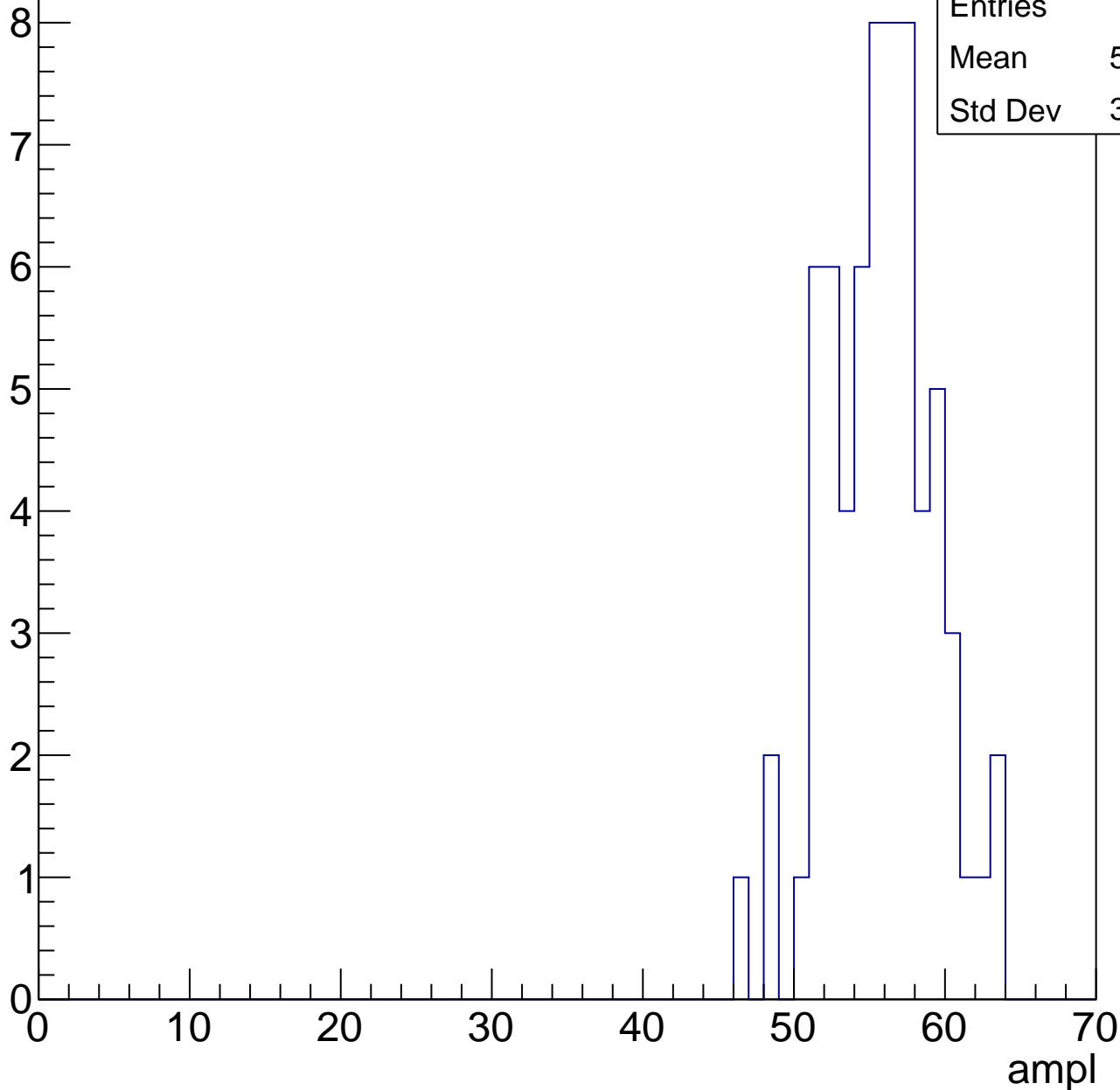


# B0L001S, U5-ch27, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	55.24
Std Dev	3.516

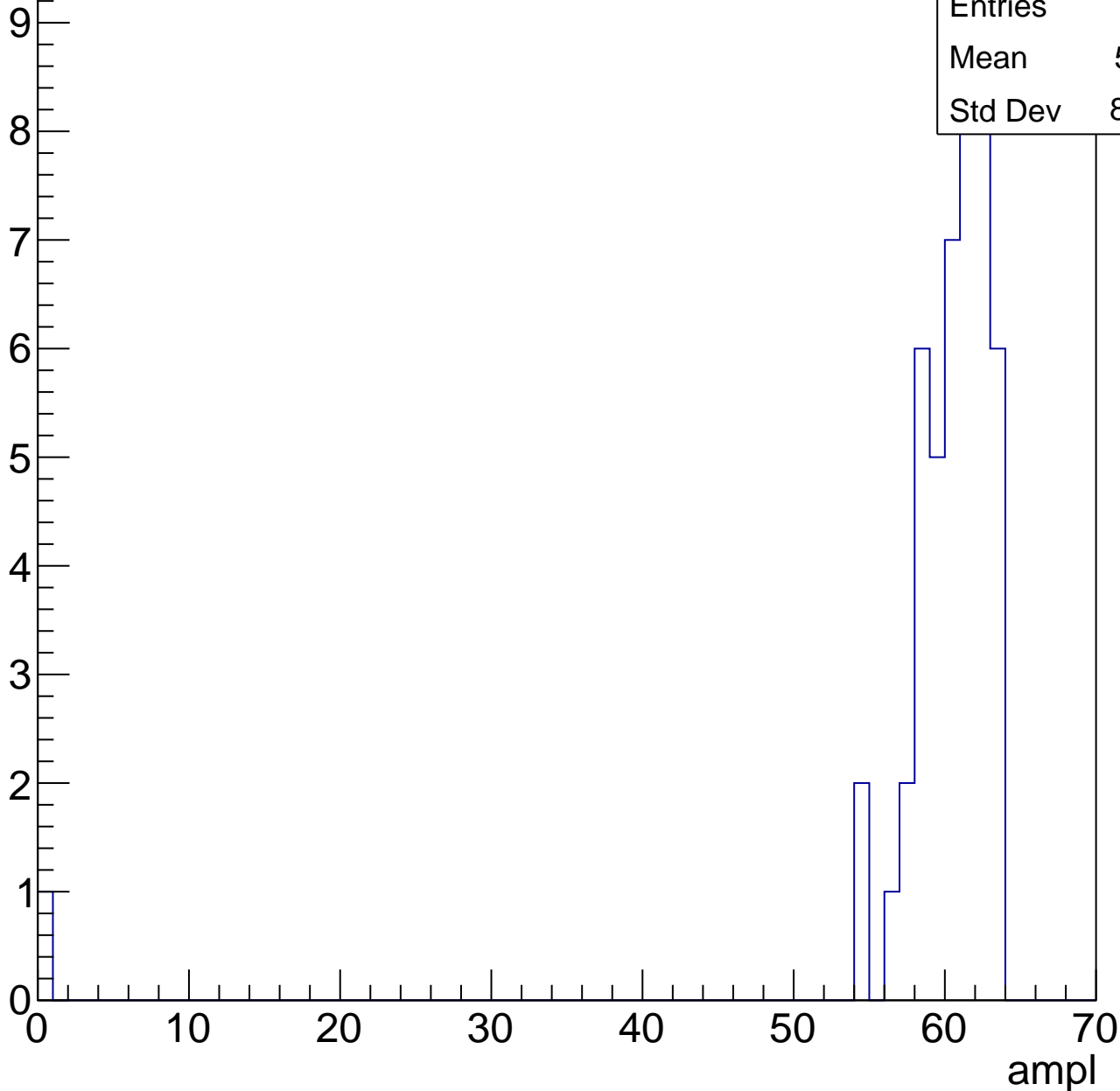


# B0L001S, U5-ch27, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	47
Mean	58.81
Std Dev	8.948



# B0L001S, U5-ch27, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.67
Std Dev	0.4714

ampl

0 10 20 30 40 50 60 70



# B0L001S, U5-ch27, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch28, adc0

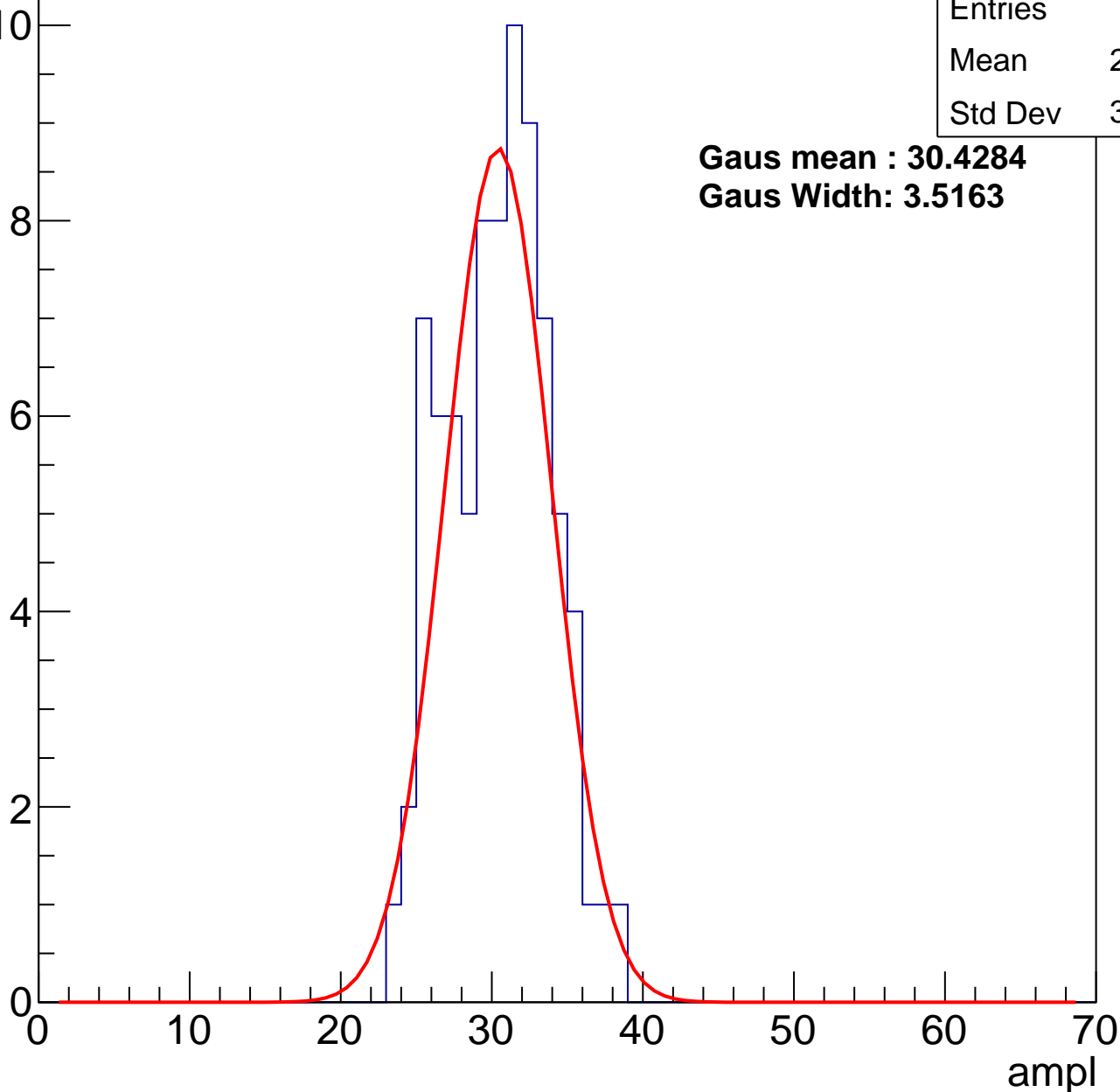
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	81
Mean	29.95
Std Dev	3.355

**Gaus mean : 30.4284**

**Gaus Width: 3.5163**



# B0L001S, U5-ch28, adc1

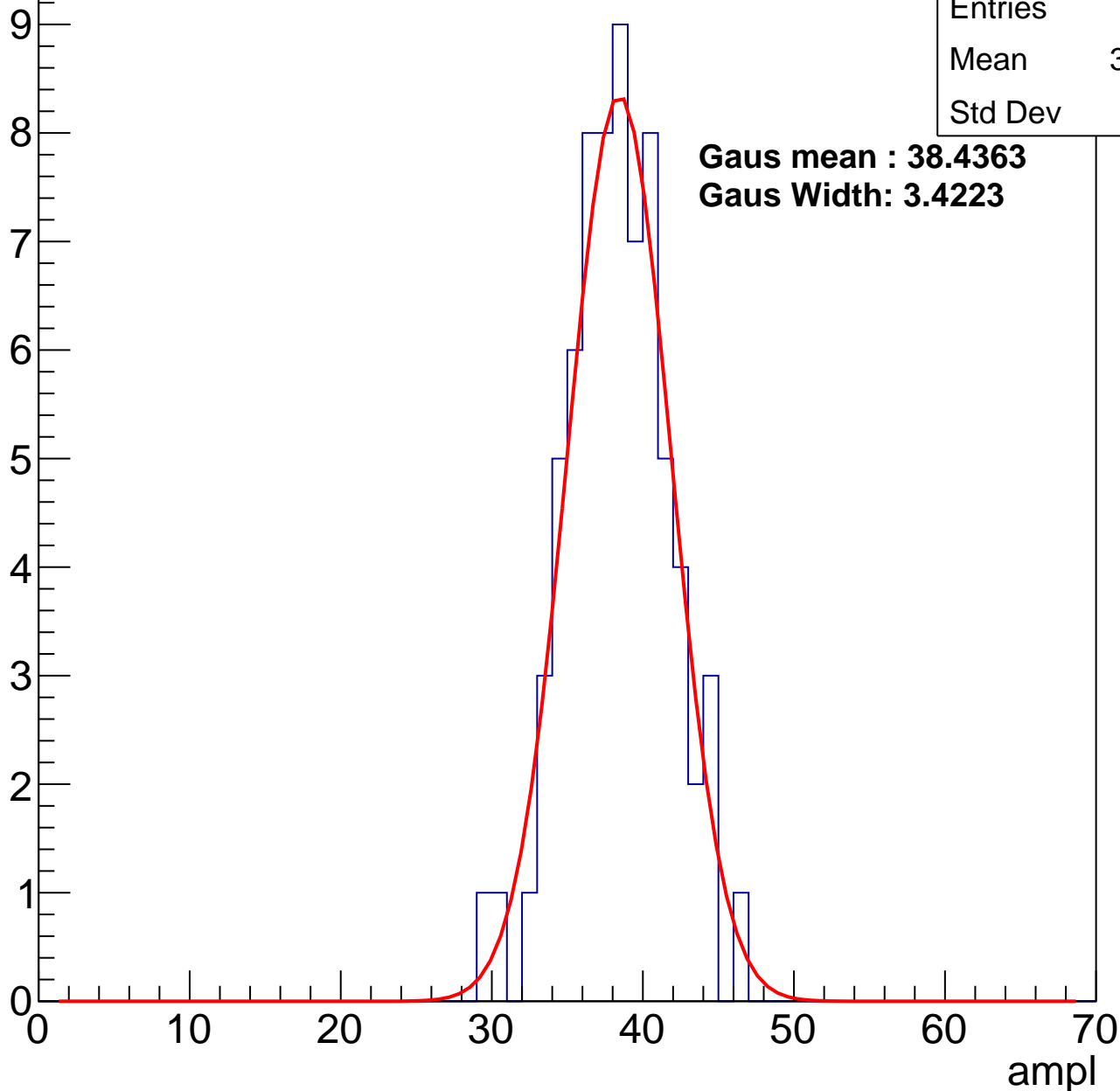
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	37.86
Std Dev	3.33

**Gaus mean : 38.4363**

**Gaus Width: 3.4223**

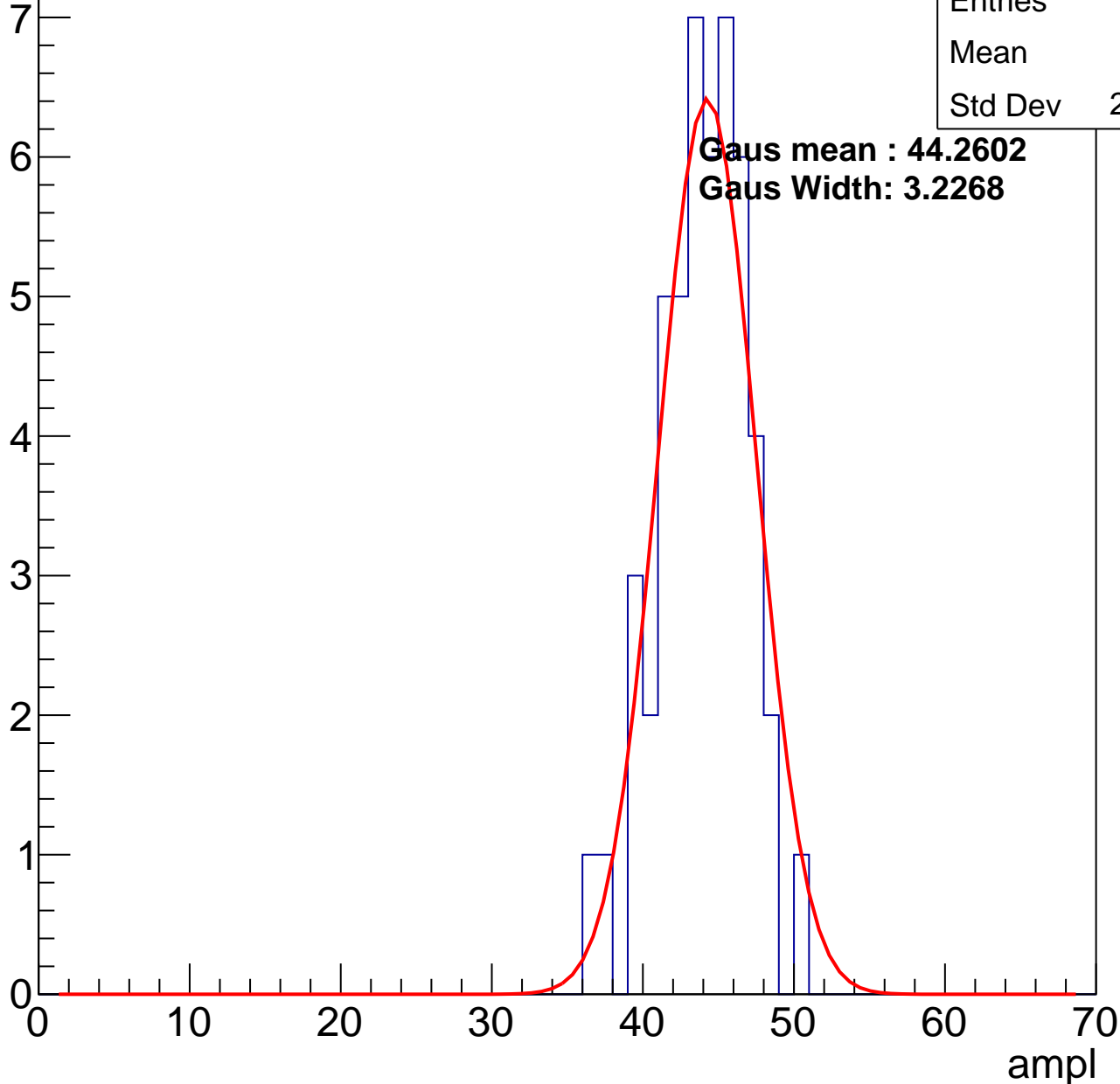


# B0L001S, U5-ch28, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	50
Mean	43.5
Std Dev	2.879

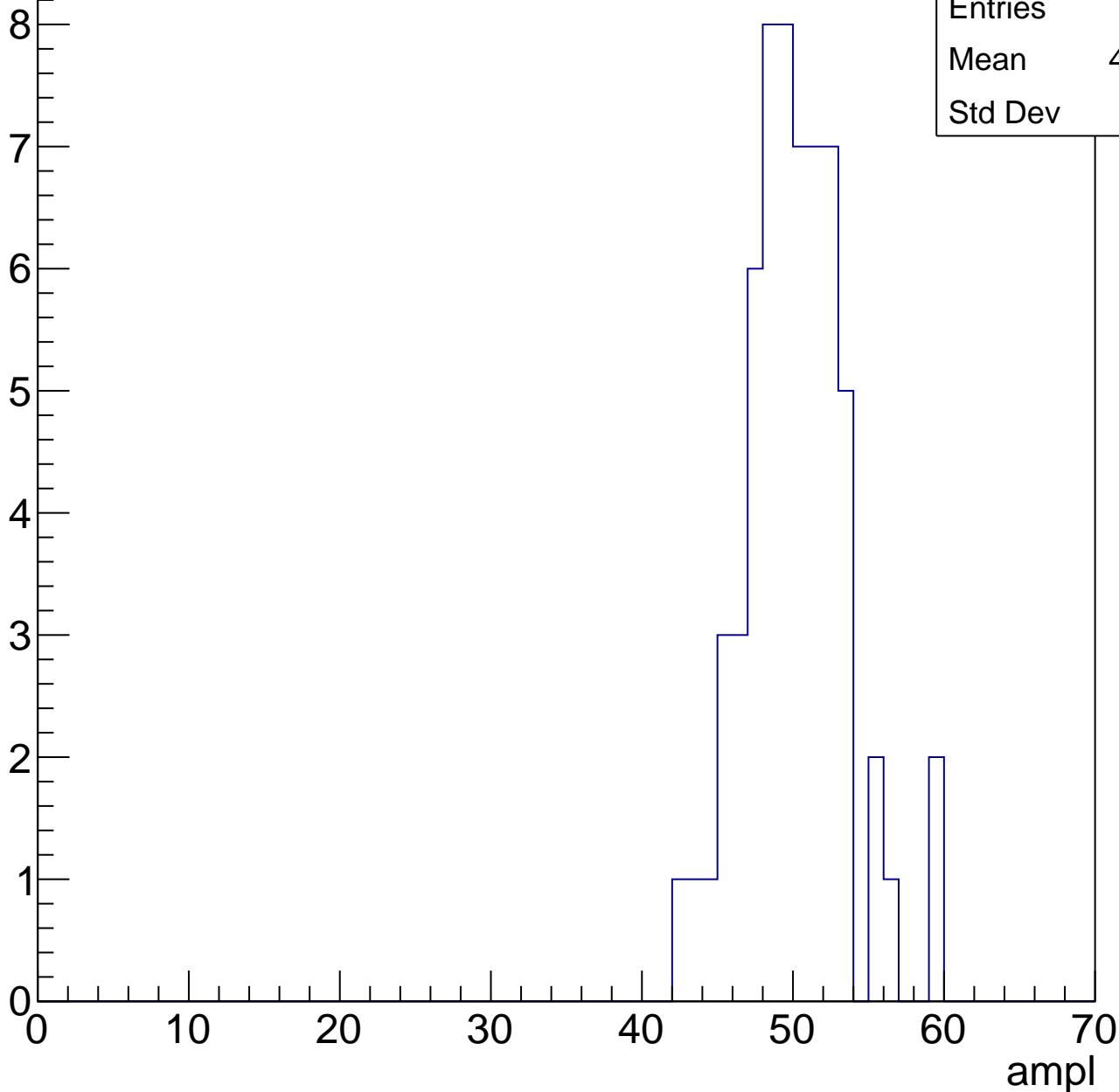


# B0L001S, U5-ch28, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	49.68
Std Dev	3.33

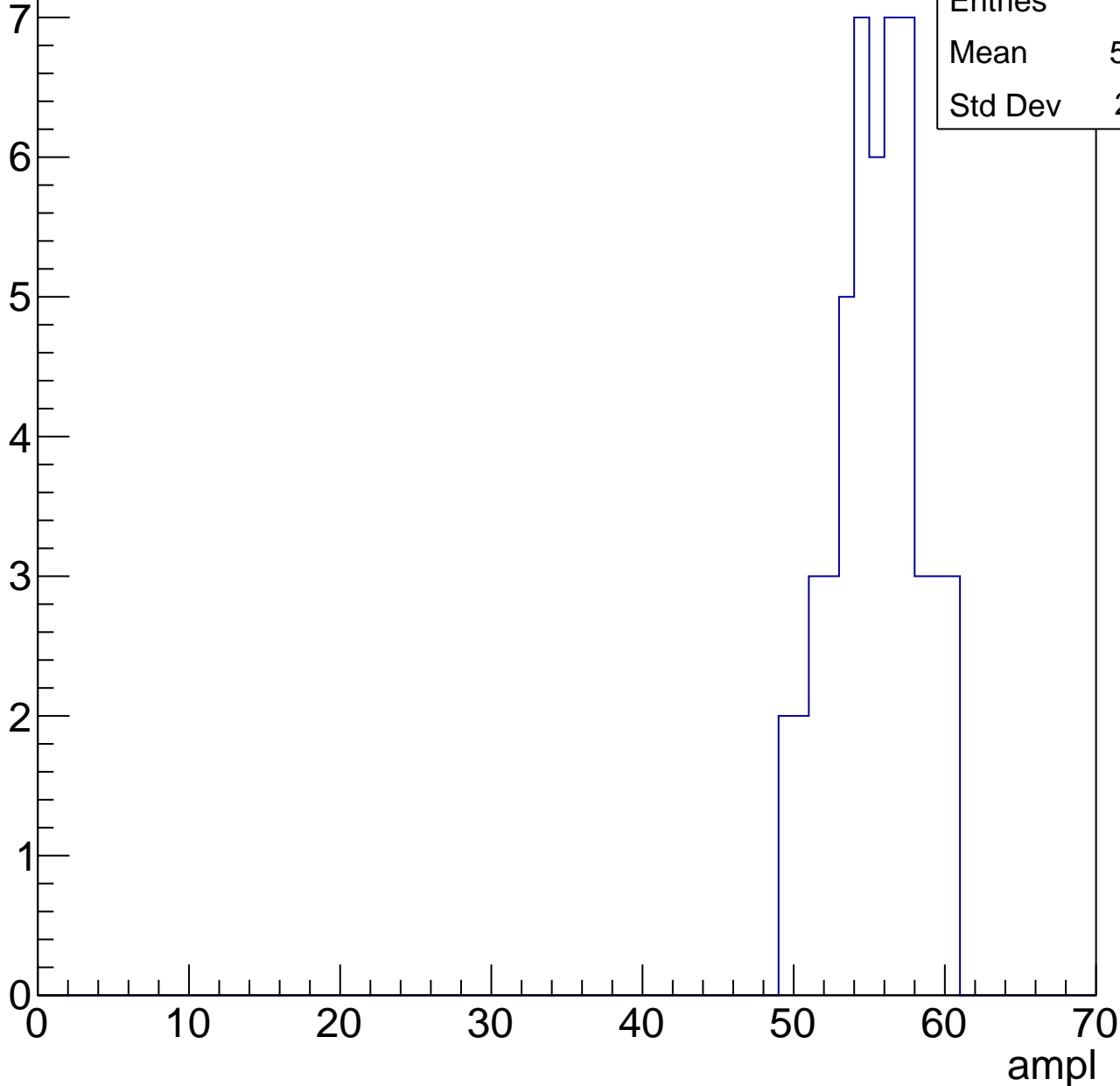


# B0L001S, U5-ch28, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	51
Mean	54.94
Std Dev	2.831



# B0L001S, U5-ch28, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

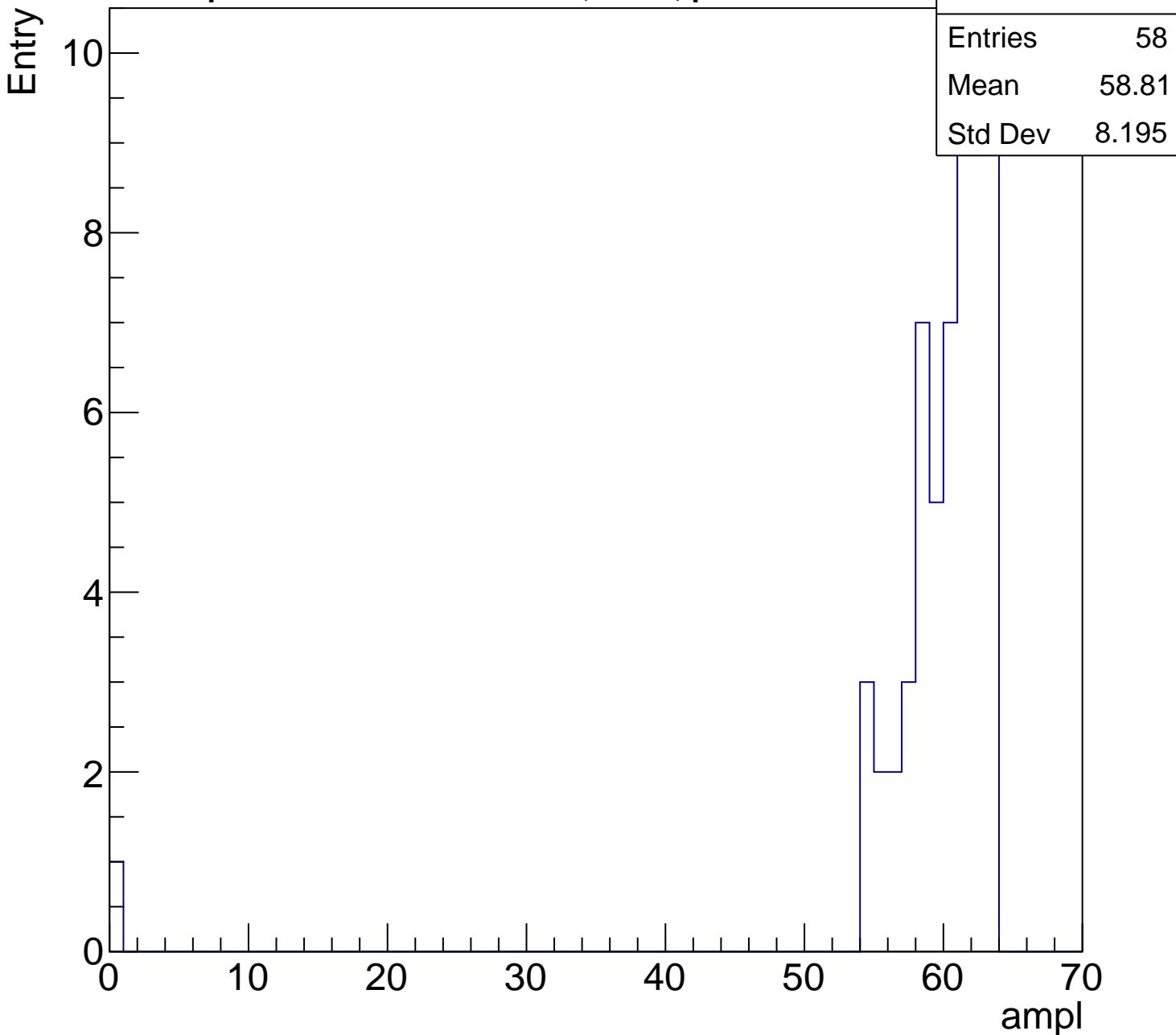
Entries	58
Mean	58.81
Std Dev	8.195

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B0L001S, U5-ch28, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch28, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U5-ch29, adc0

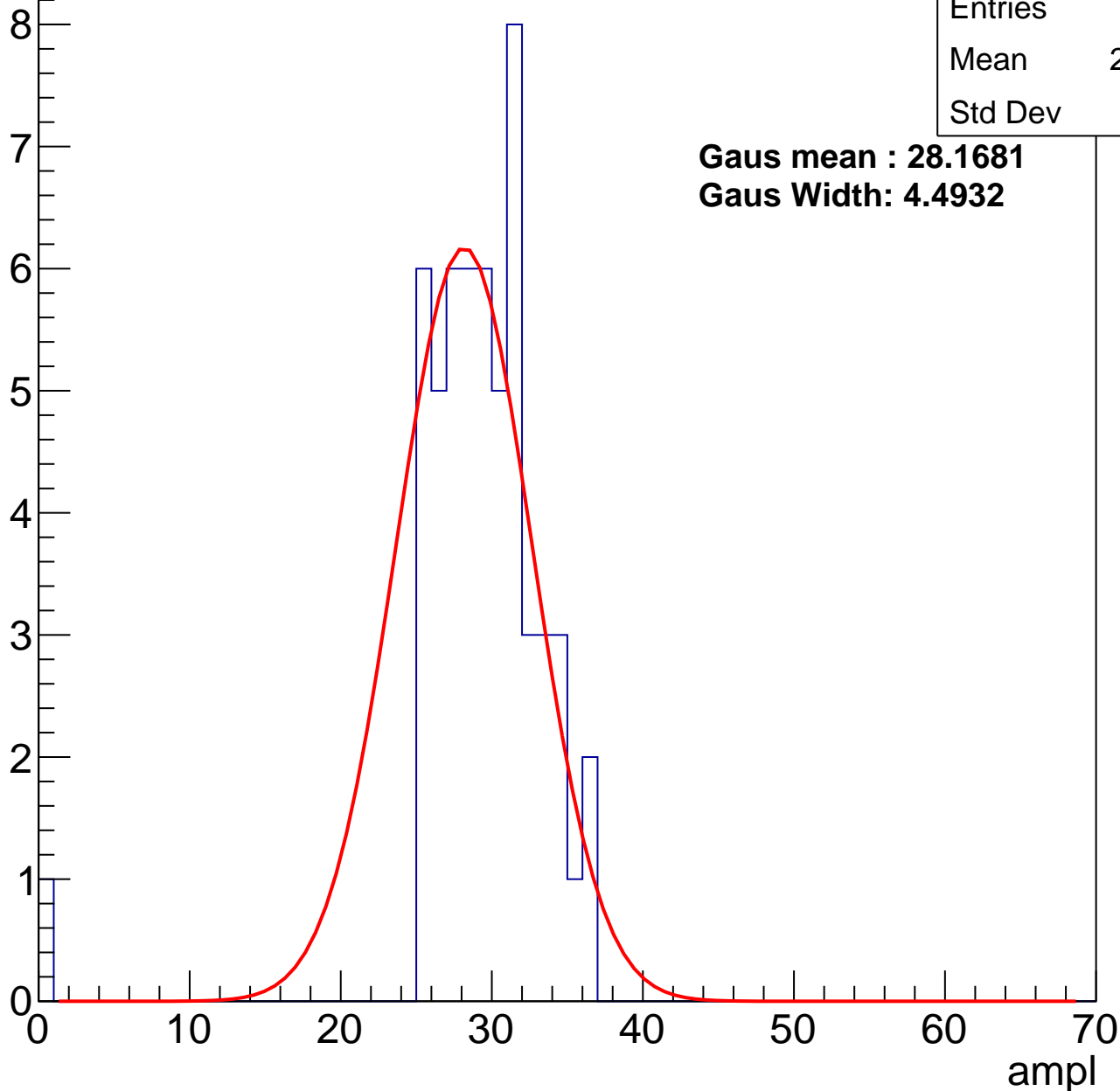
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	28.84
Std Dev	4.92

**Gaus mean : 28.1681**

**Gaus Width: 4.4932**



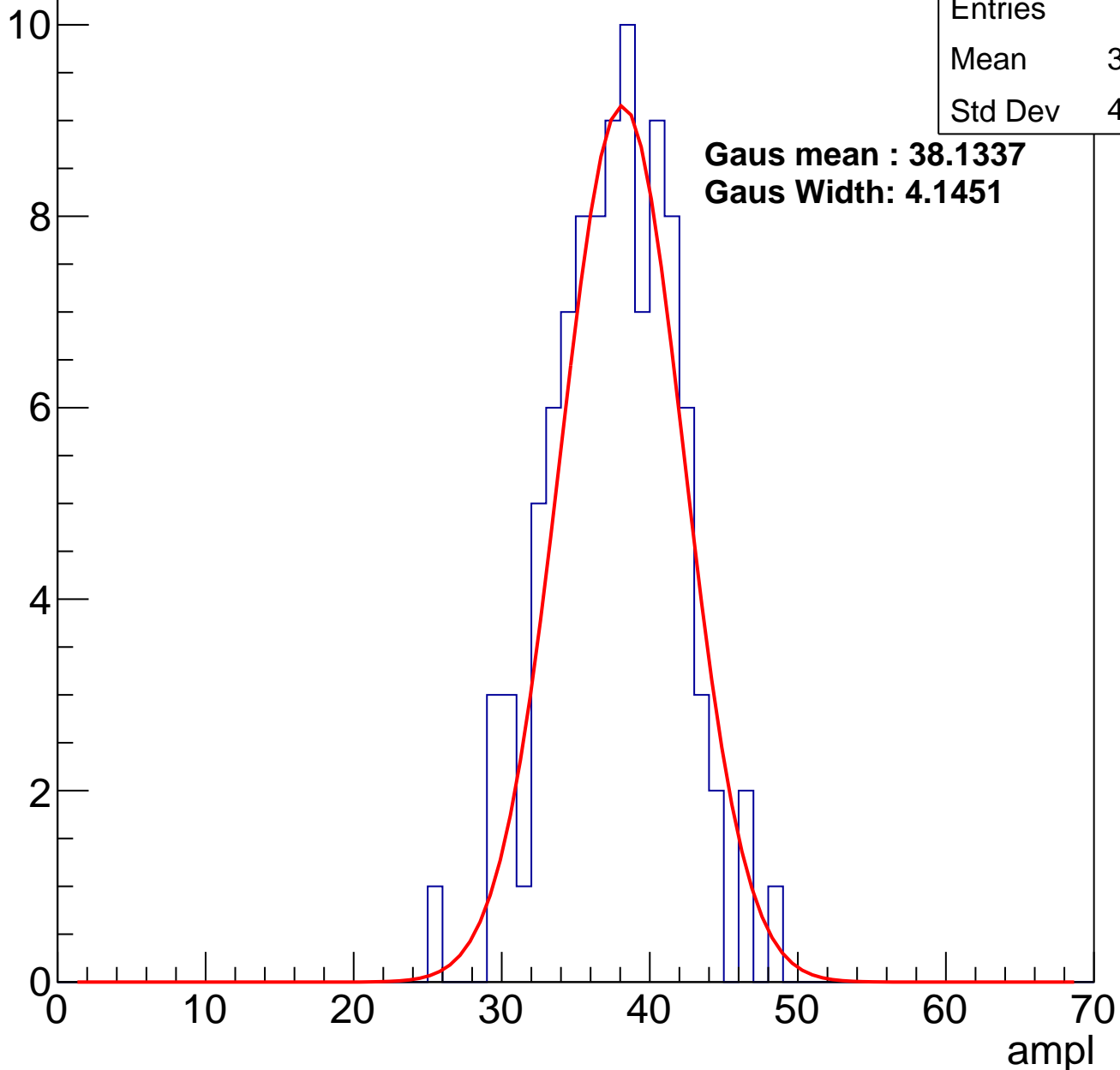
# B0L001S, U5-ch29, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	99
Mean	37.17
Std Dev	4.176

**Gaus mean : 38.1337**  
**Gaus Width: 4.1451**

Entry



# B0L001S, U5-ch29, adc2

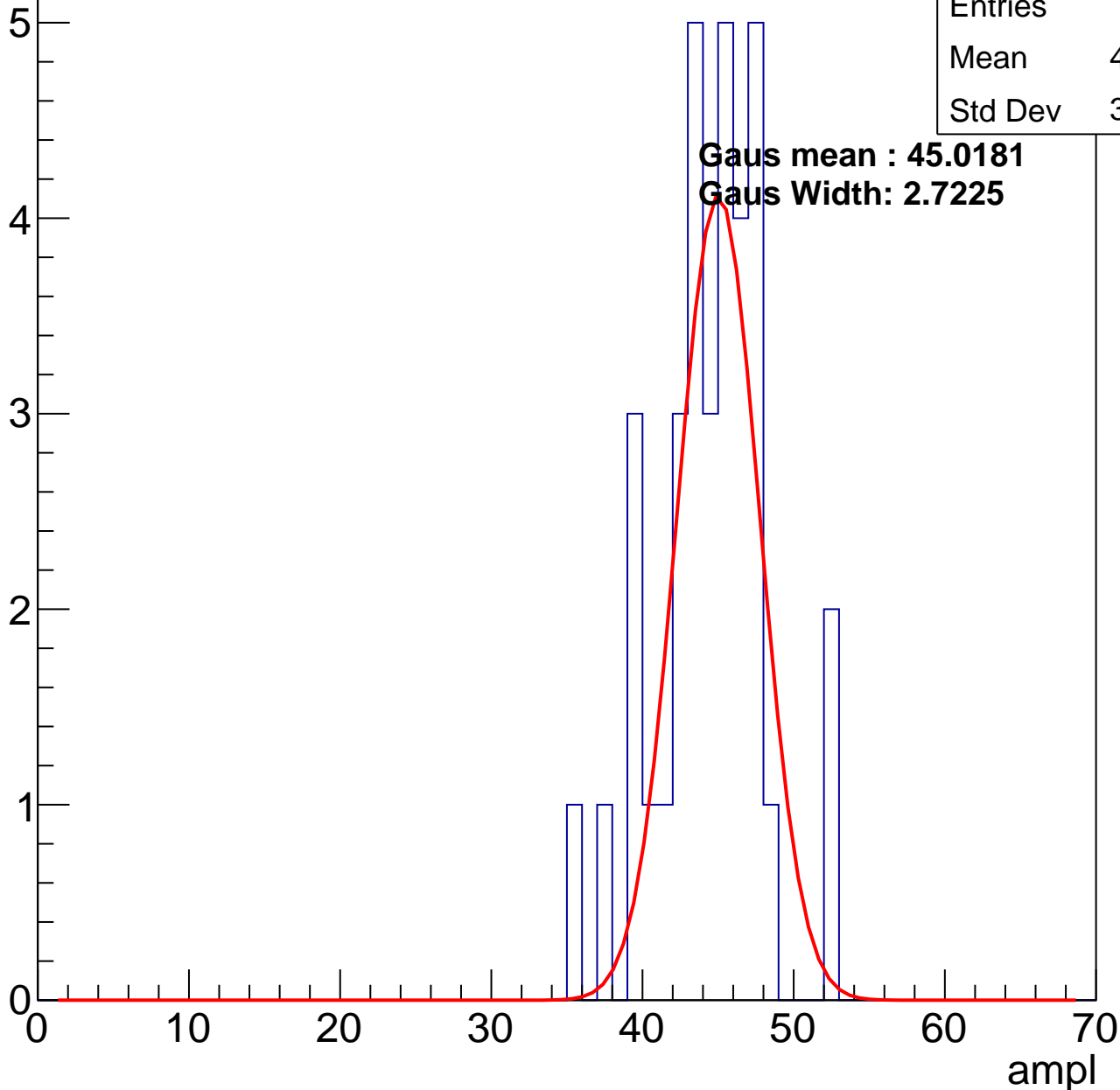
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	35
Mean	43.97
Std Dev	3.613

**Gaus mean : 45.0181**

**Gaus Width: 2.7225**

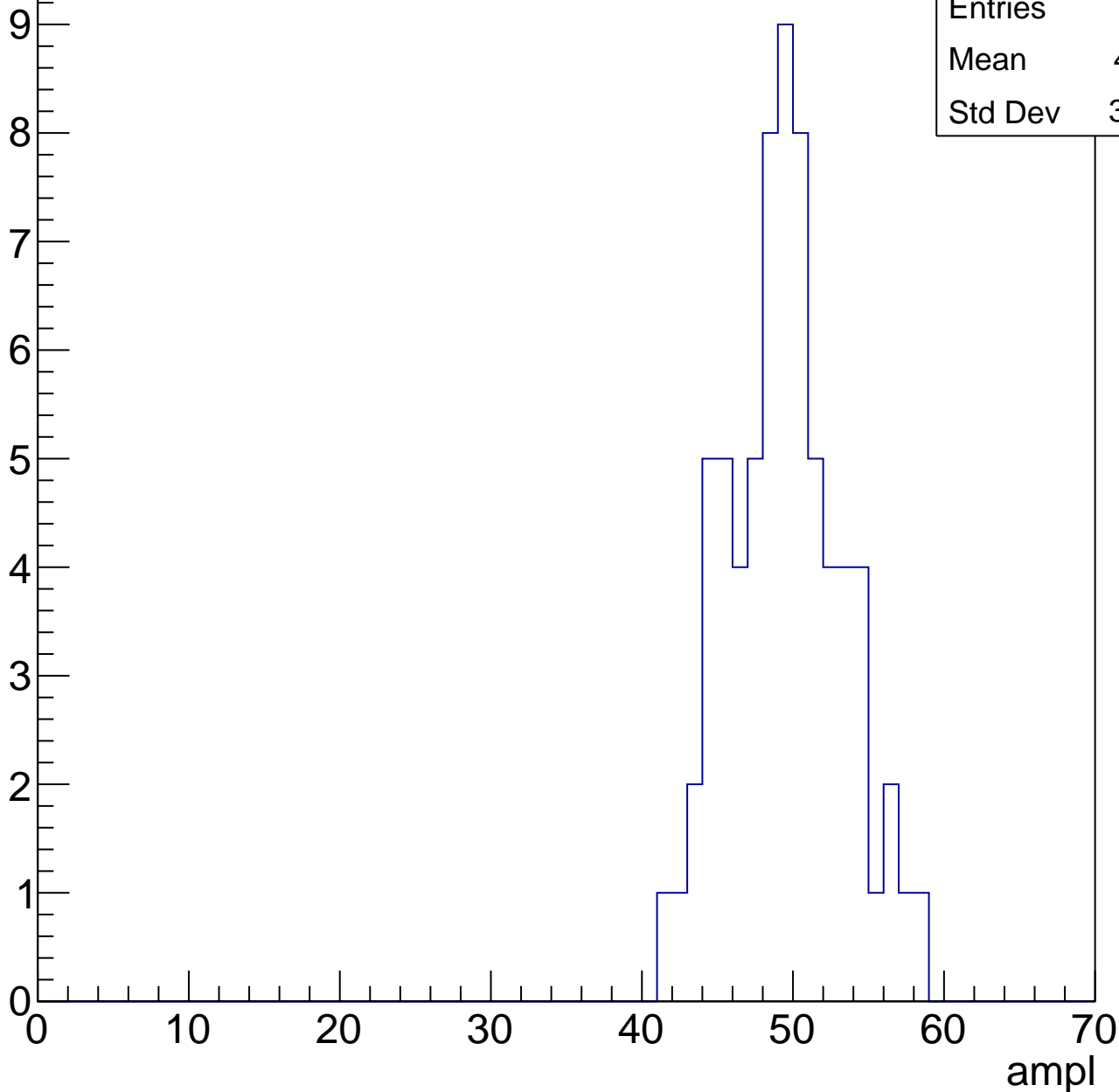


# B0L001S, U5-ch29, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	49.01
Std Dev	3.705



# B0L001S, U5-ch29, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

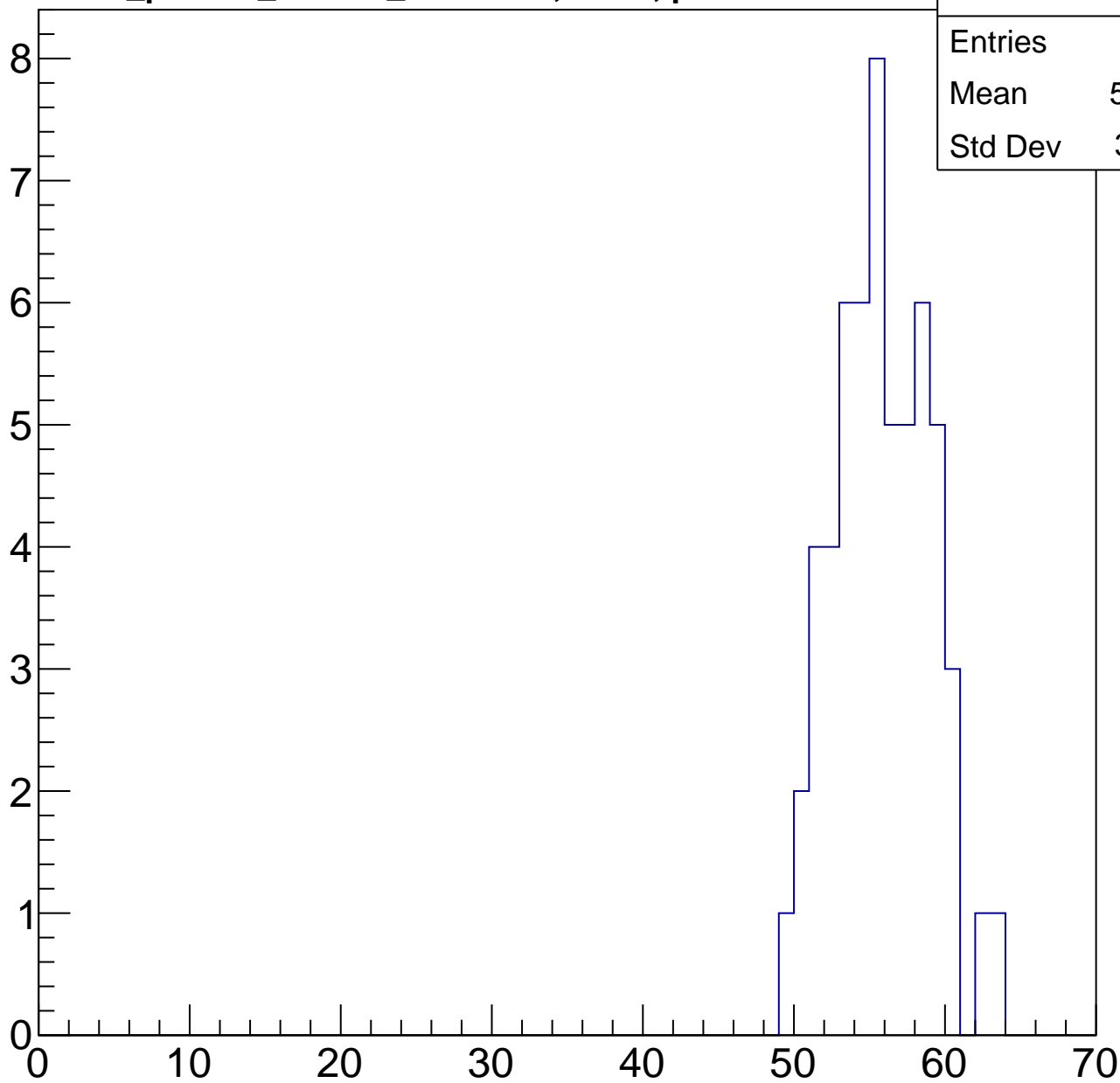
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	57
Mean	55.37
Std Dev	3.121

ampl

0 10 20 30 40 50 60 70

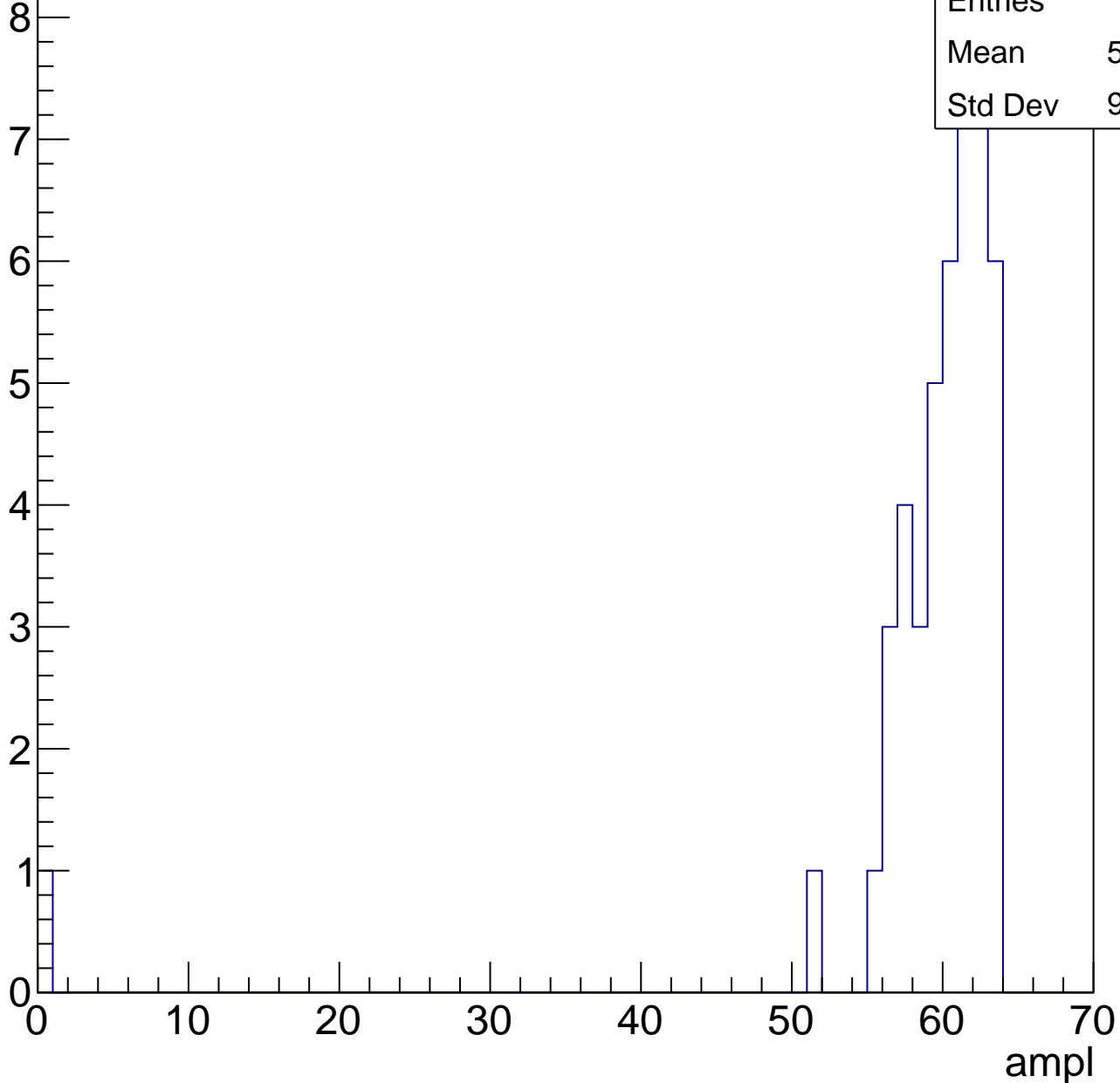


# B0L001S, U5-ch29, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	46
Mean	58.54
Std Dev	9.093



# B0L001S, U5-ch29, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

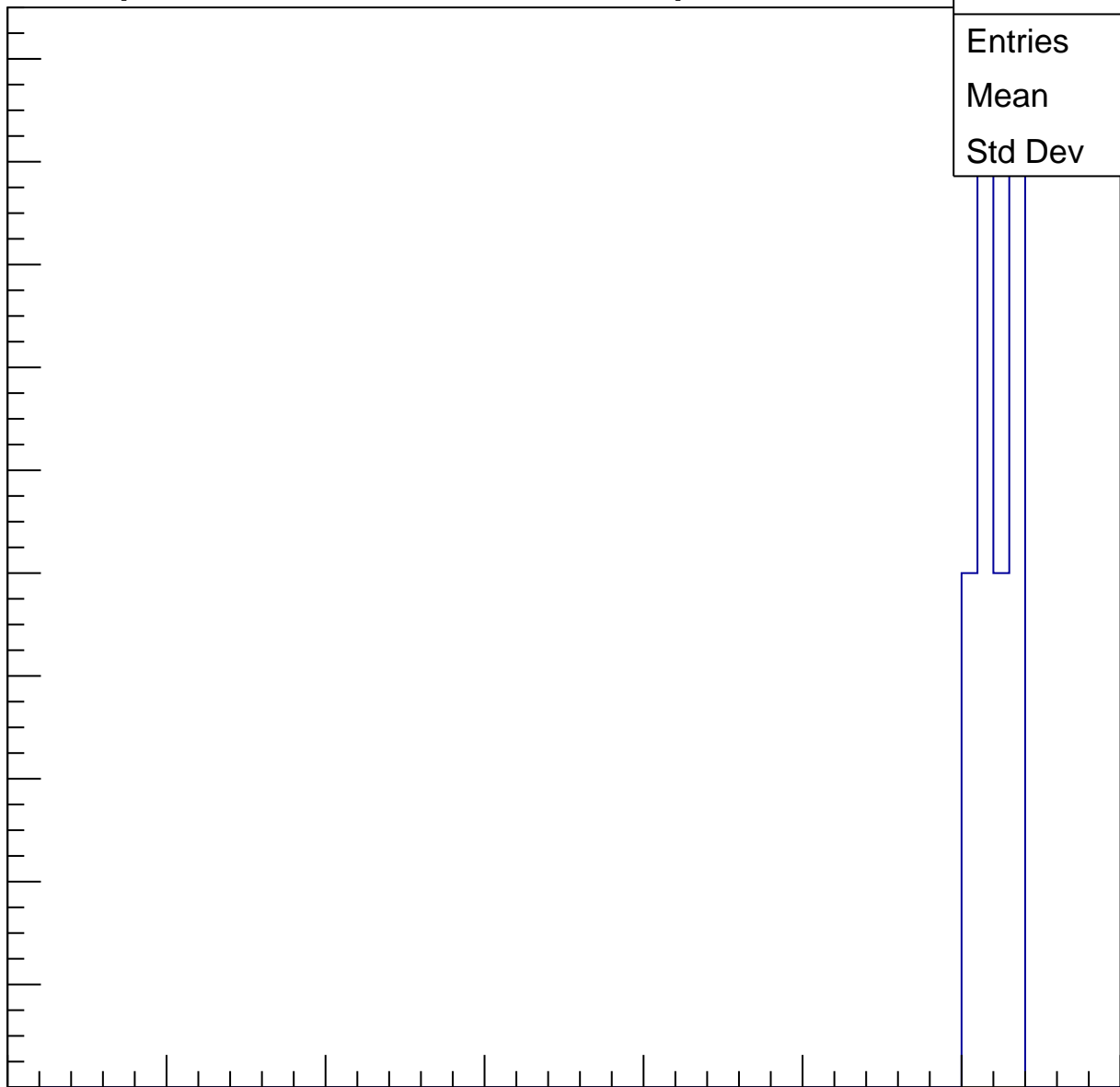
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	61.67
Std Dev	1.106

0 10 20 30 40 50 60 70

ampl





# B0L001S, U5-ch29, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	63
Std Dev	0

ampl

# B0L001S, U5-ch30, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	84
Mean	29.44
Std Dev	6.348

**Gaus mean : 30.6369**

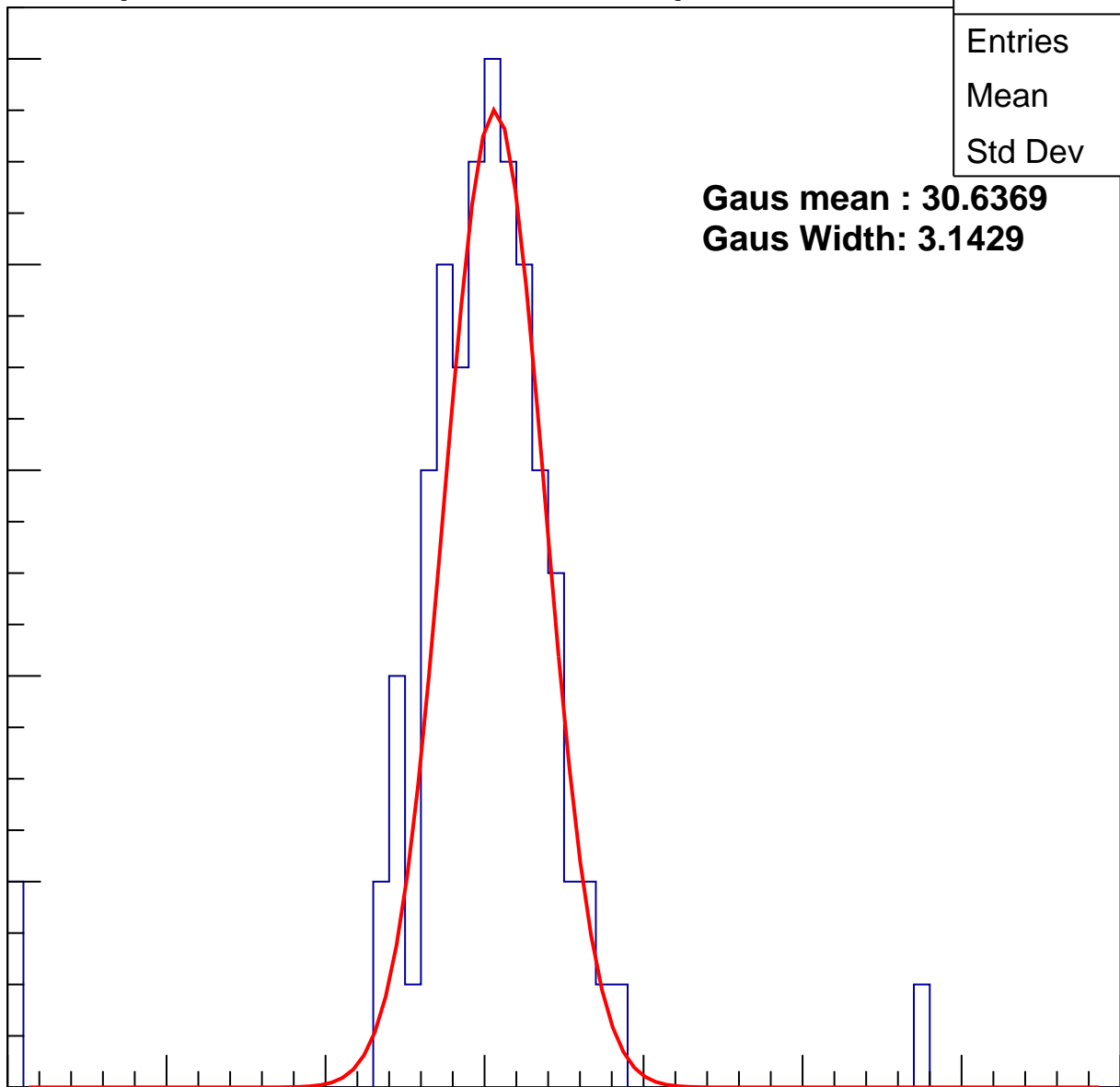
**Gaus Width: 3.1429**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U5-ch30, adc1

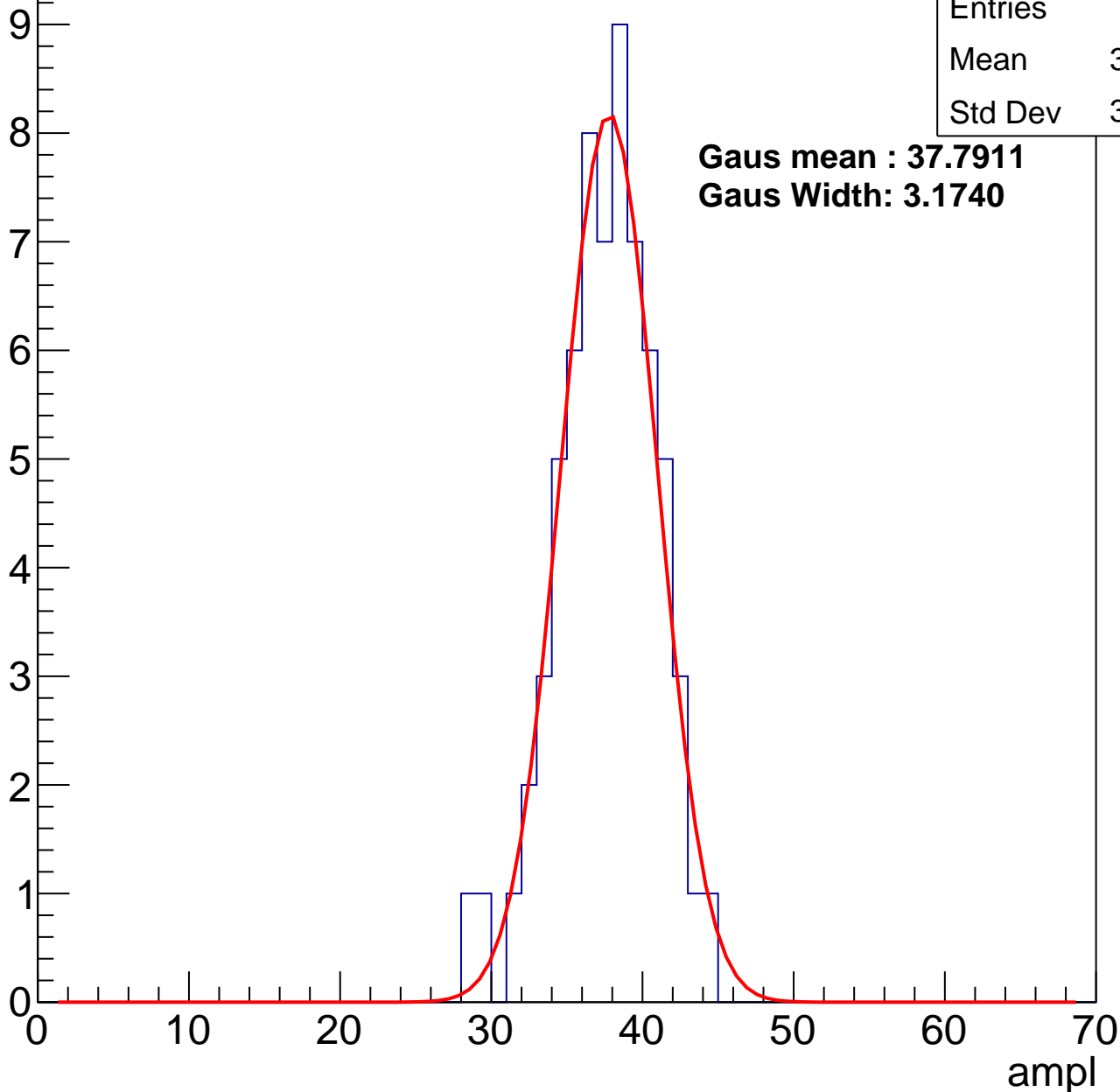
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	37.14
Std Dev	3.223

**Gaus mean : 37.7911**

**Gaus Width: 3.1740**



# B0L001S, U5-ch30, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	76
Mean	43.95
Std Dev	3.677

**Gaus mean : 44.5199**

**Gaus Width: 4.0509**

10

8

6

4

2

0

0

10

20

30

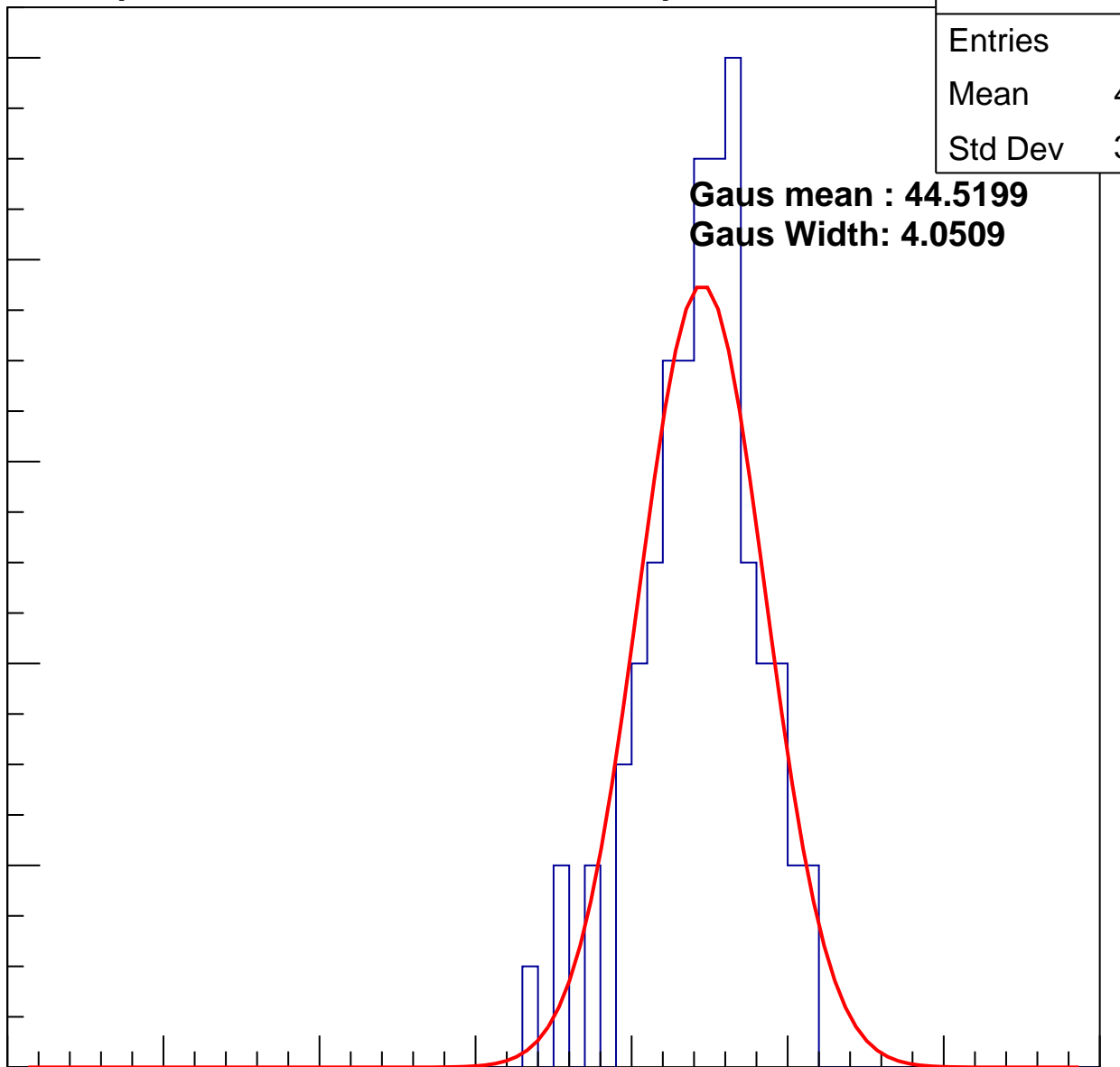
40

50

60

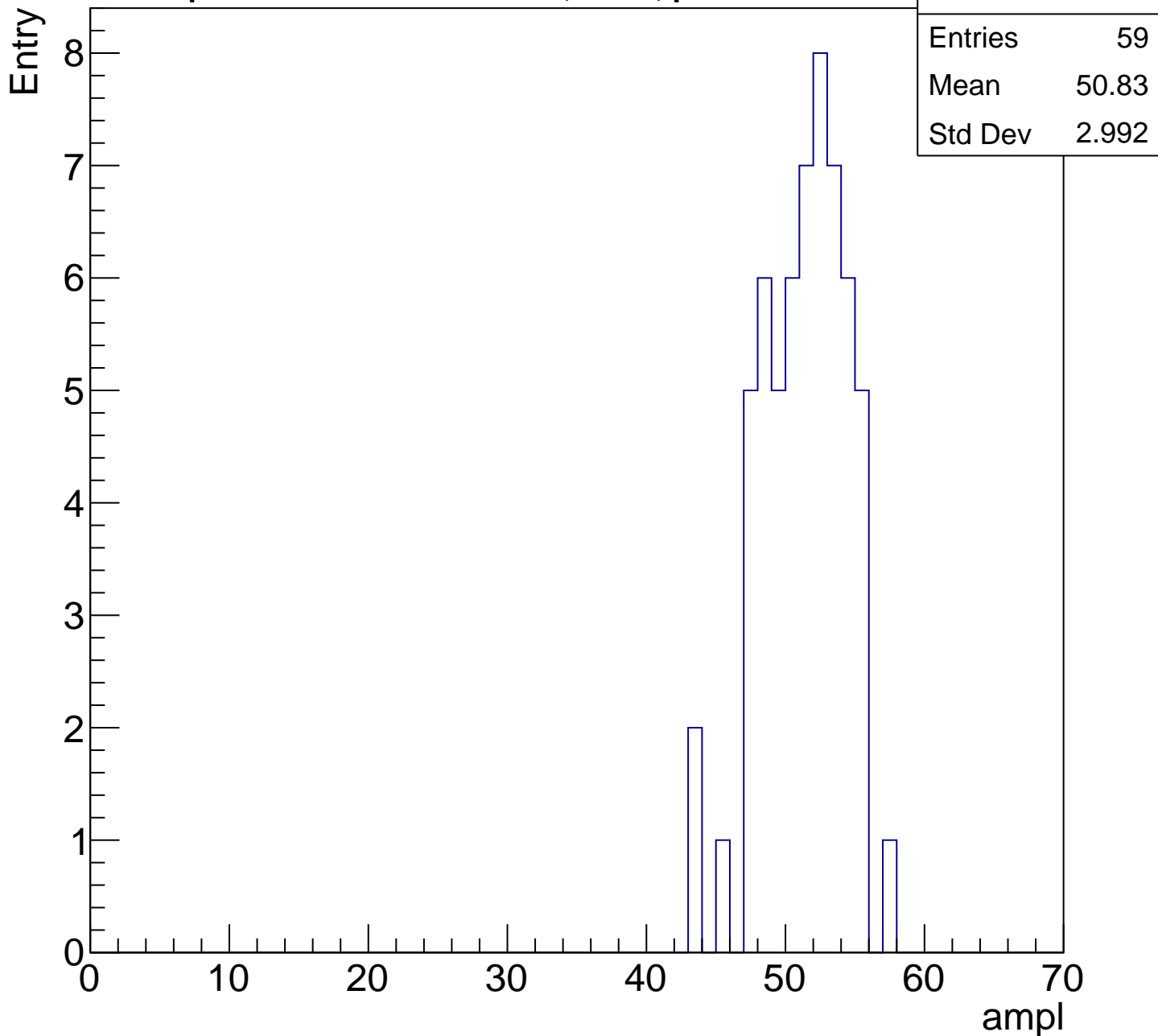
70

ampl



# B0L001S, U5-ch30, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

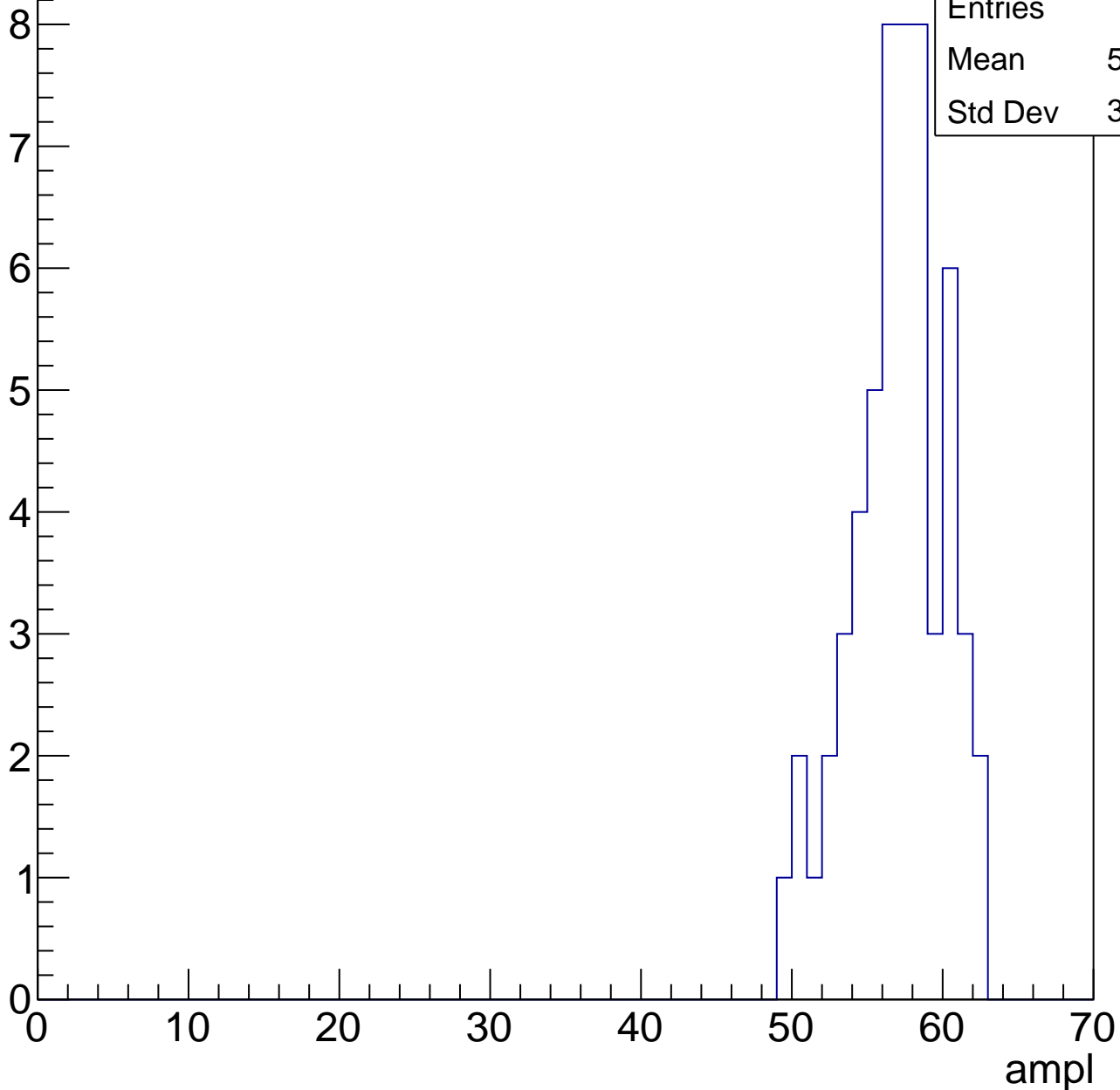


# B0L001S, U5-ch30, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	56.54
Std Dev	3.047

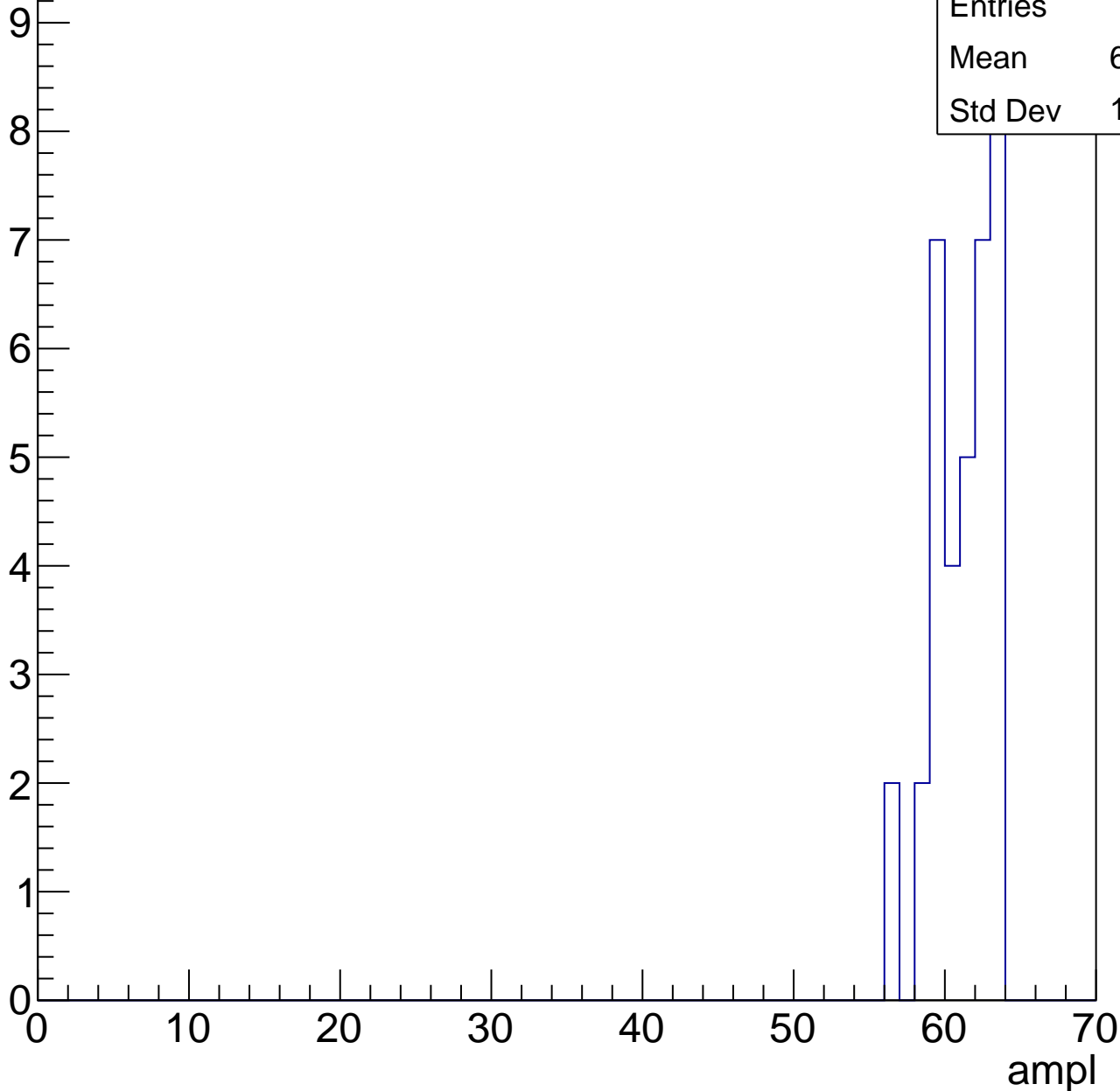


# B0L001S, U5-ch30, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

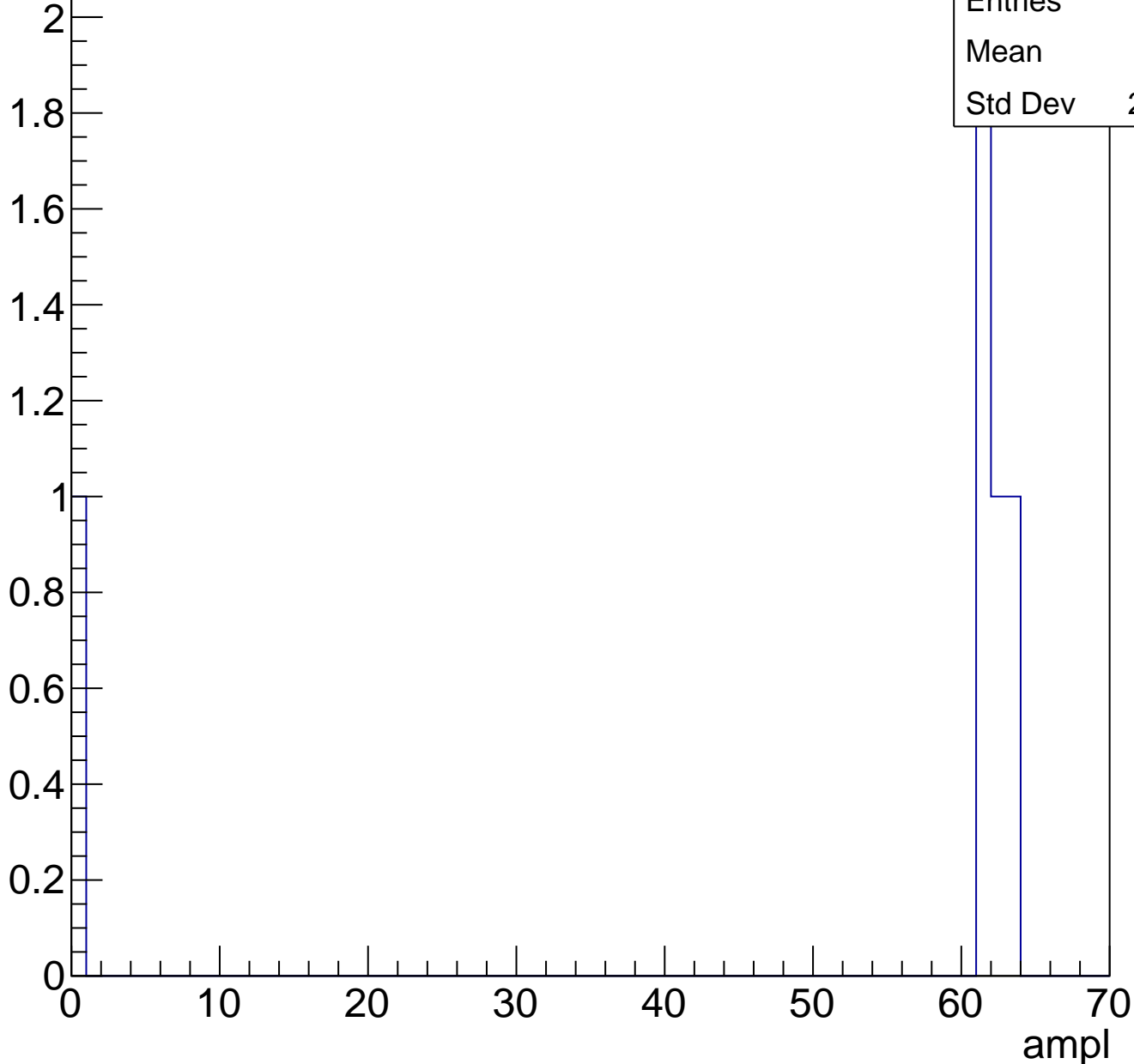
Entries	36
Mean	60.75
Std Dev	1.977



# B0L001S, U5-ch30, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch30, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U5-ch31, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	84
Mean	29.23
Std Dev	6.066

**Gaus mean : 30.5097**

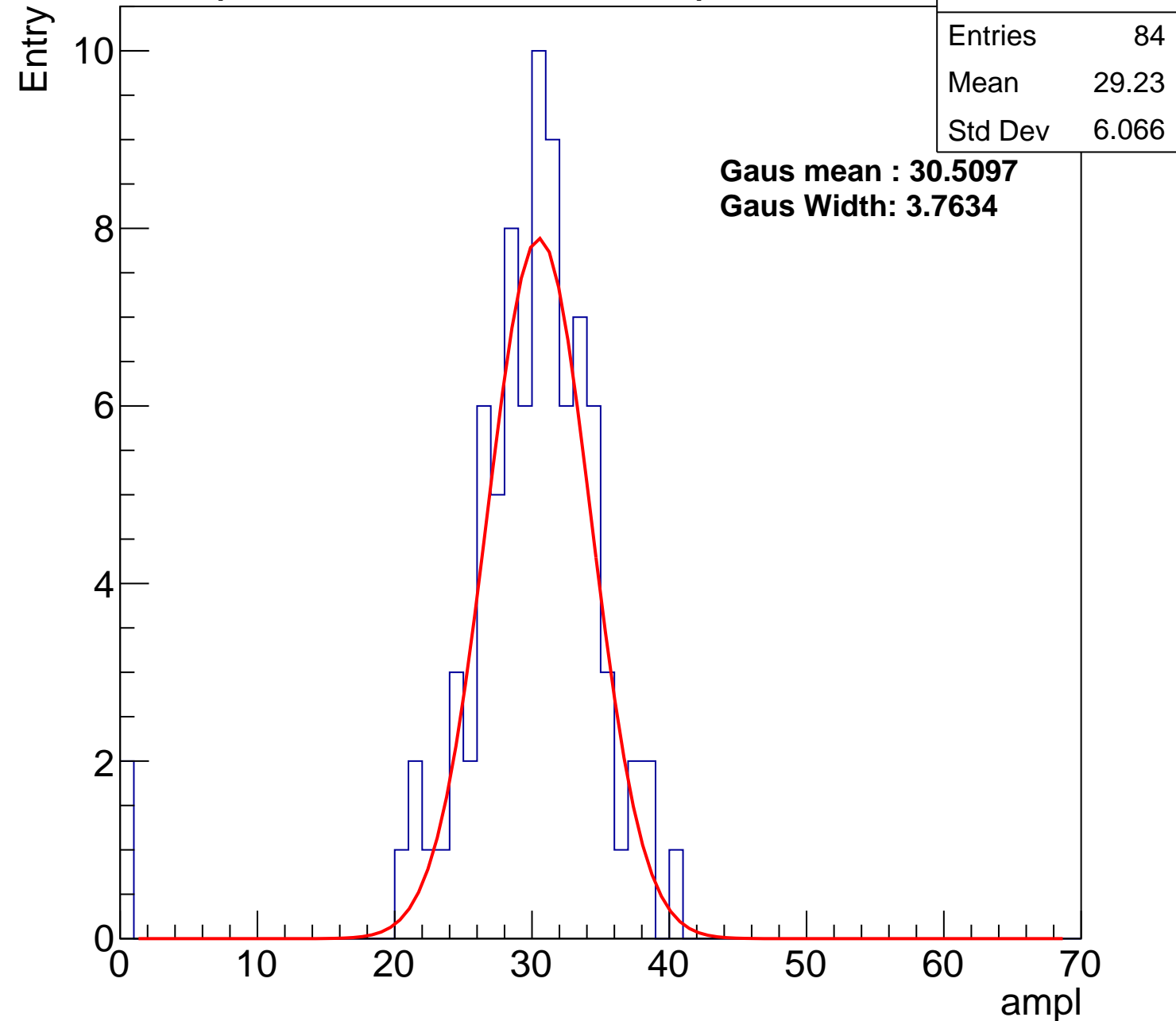
**Gaus Width: 3.7634**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U5-ch31, adc1

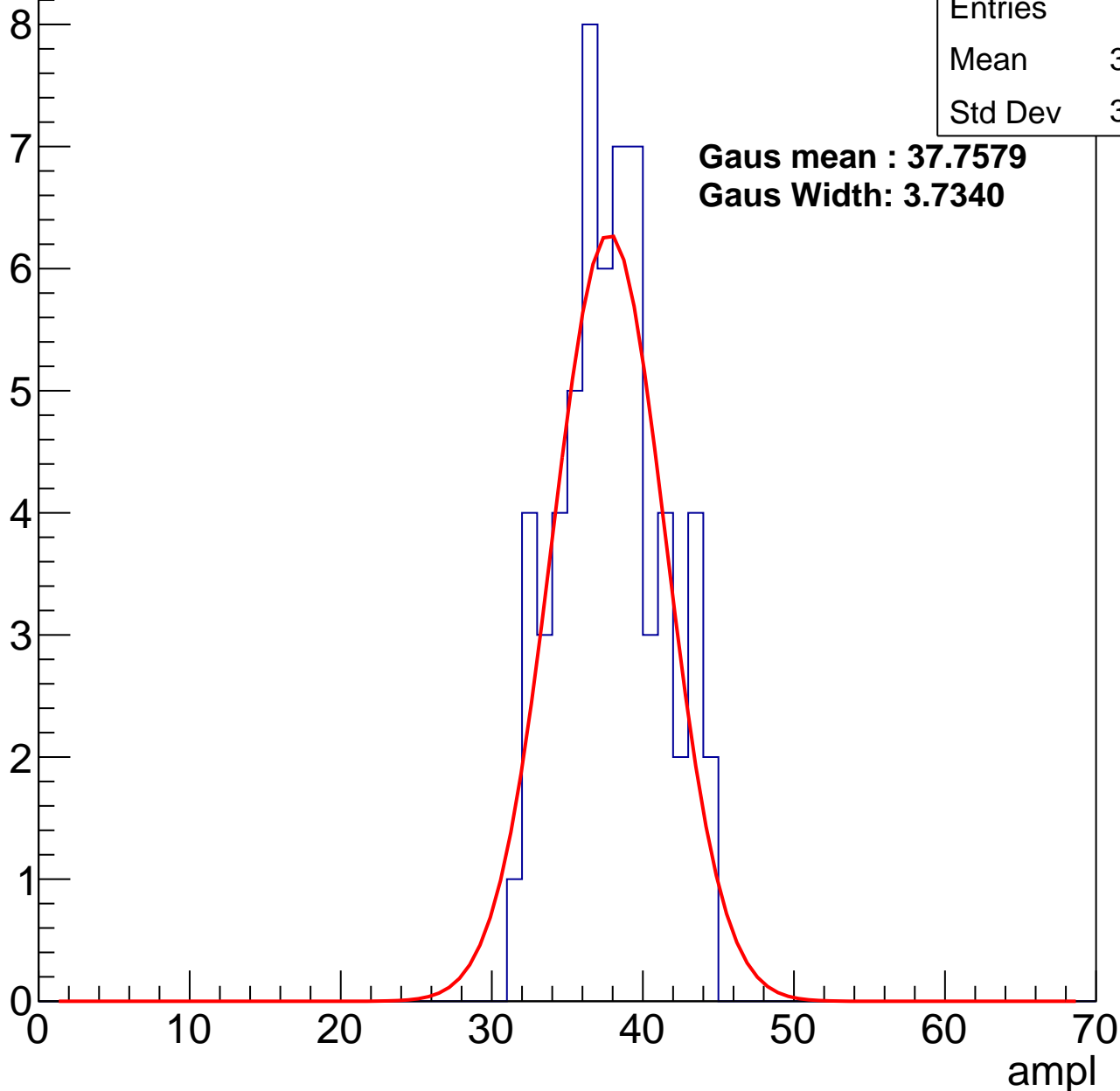
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	37.43
Std Dev	3.303

**Gaus mean : 37.7579**

**Gaus Width: 3.7340**



# B0L001S, U5-ch31, adc2

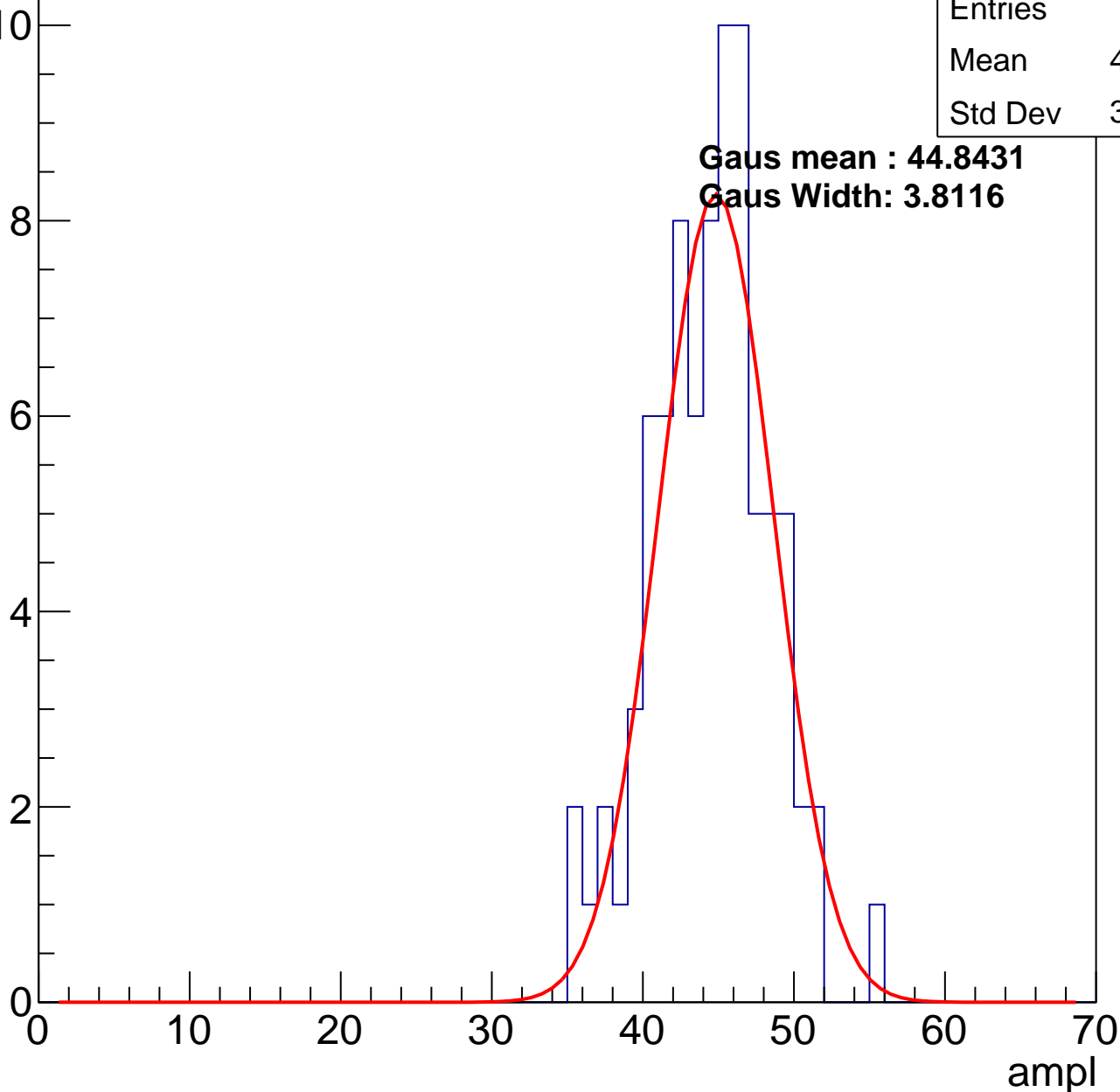
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	83
Mean	44.02
Std Dev	3.824

**Gaus mean : 44.8431**

**Gaus Width: 3.8116**

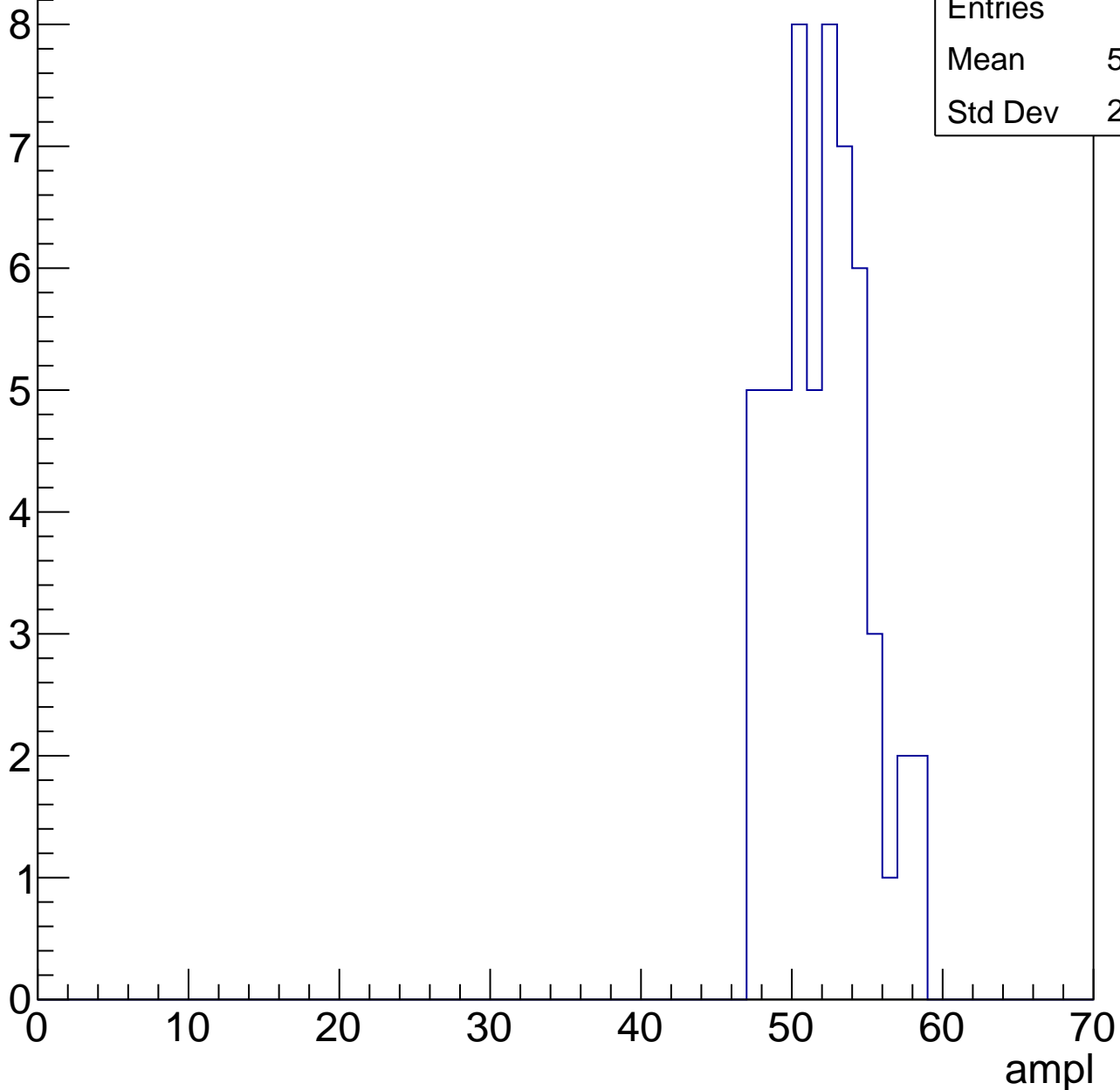


# B0L001S, U5-ch31, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

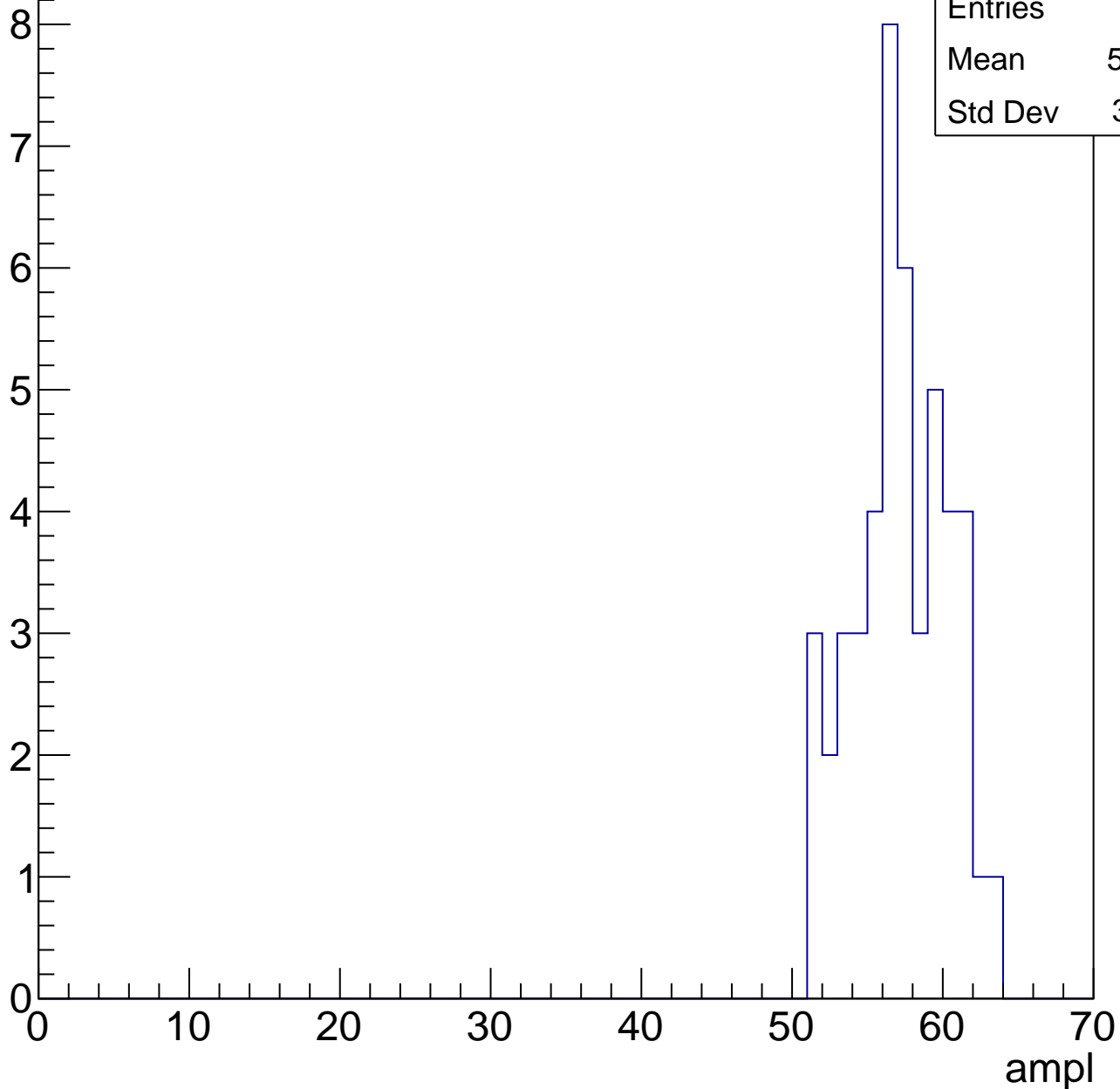
Entries	57
Mean	51.53
Std Dev	2.872



# B0L001S, U5-ch31, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



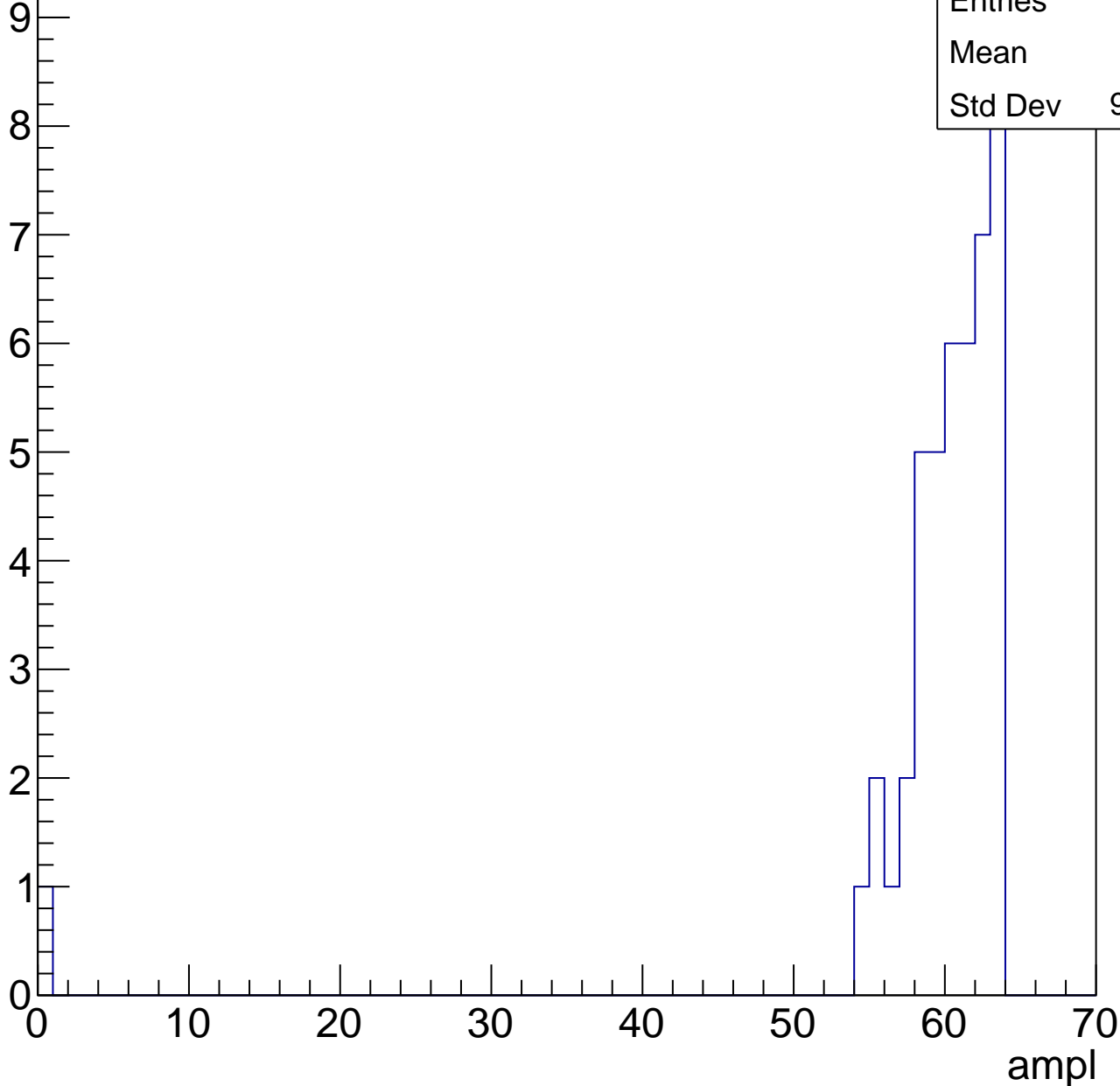
Entries	47
Mean	56.72
Std Dev	3.051

# B0L001S, U5-ch31, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	45
Mean	58.8
Std Dev	9.184



# B0L001S, U5-ch31, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch31, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U5-ch32, adc0

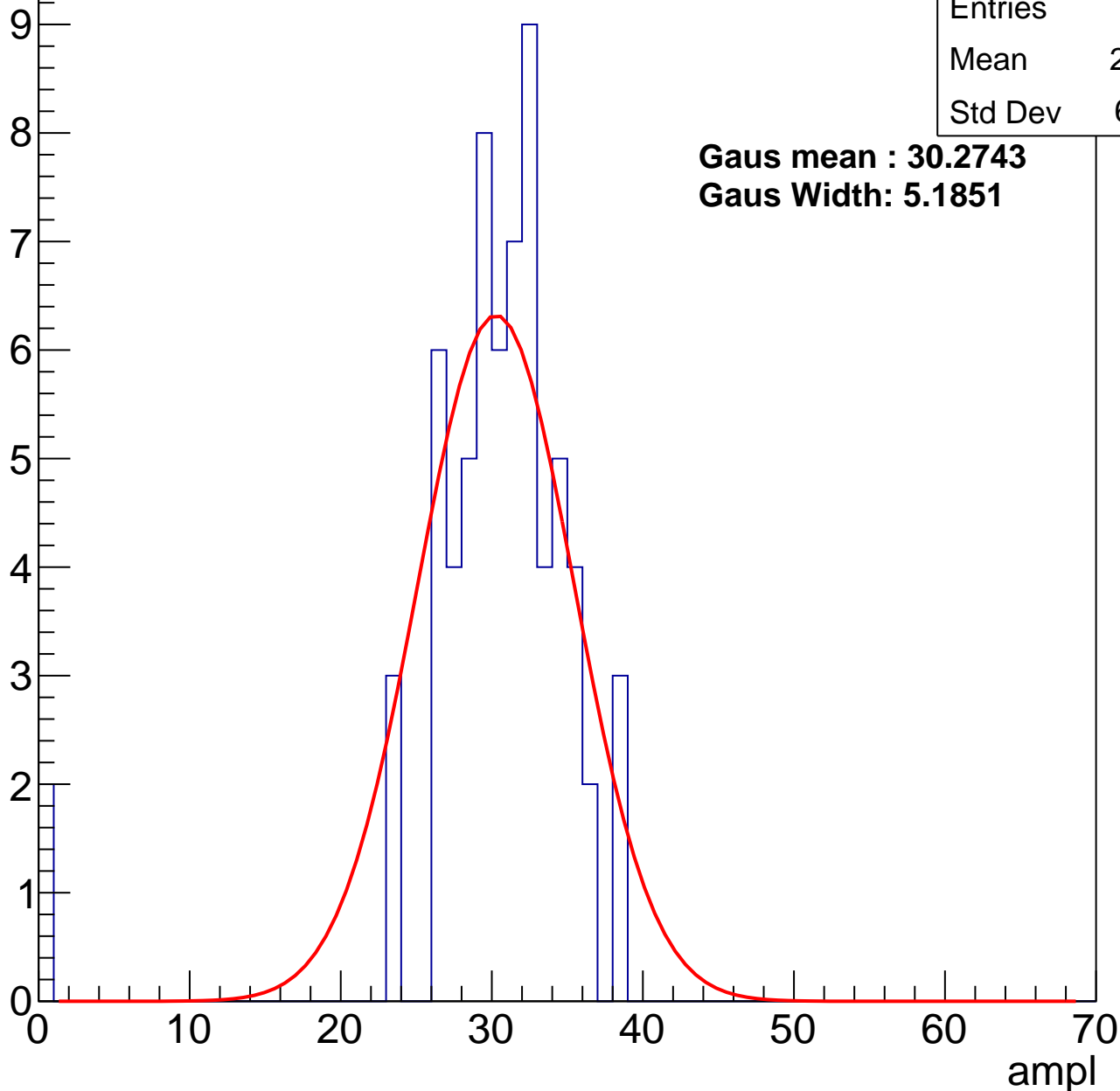
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	29.68
Std Dev	6.211

**Gaus mean : 30.2743**

**Gaus Width: 5.1851**



# B0L001S, U5-ch32, adc1

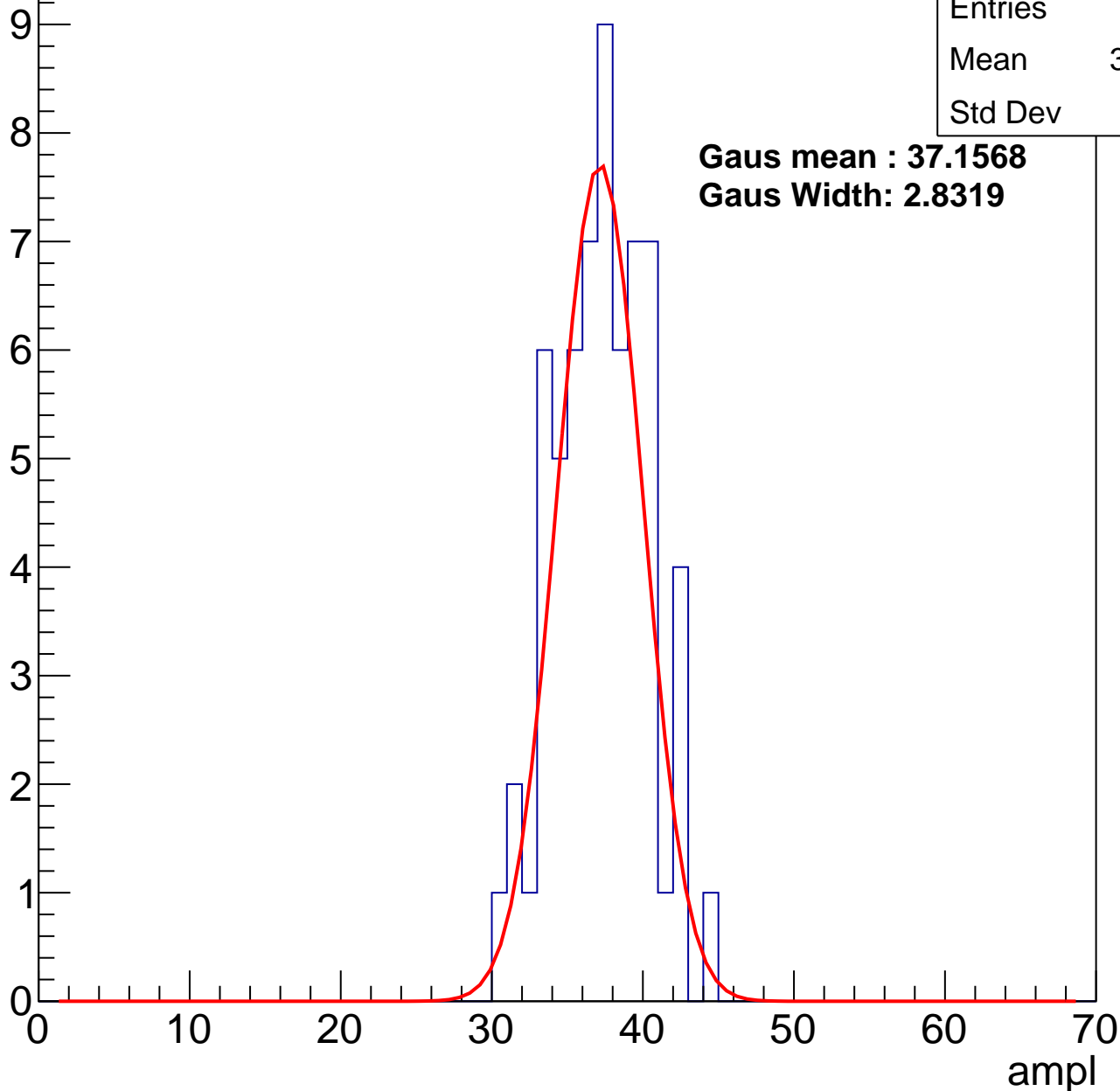
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	36.84
Std Dev	3.03

**Gaus mean : 37.1568**

**Gaus Width: 2.8319**



# B0L001S, U5-ch32, adc2

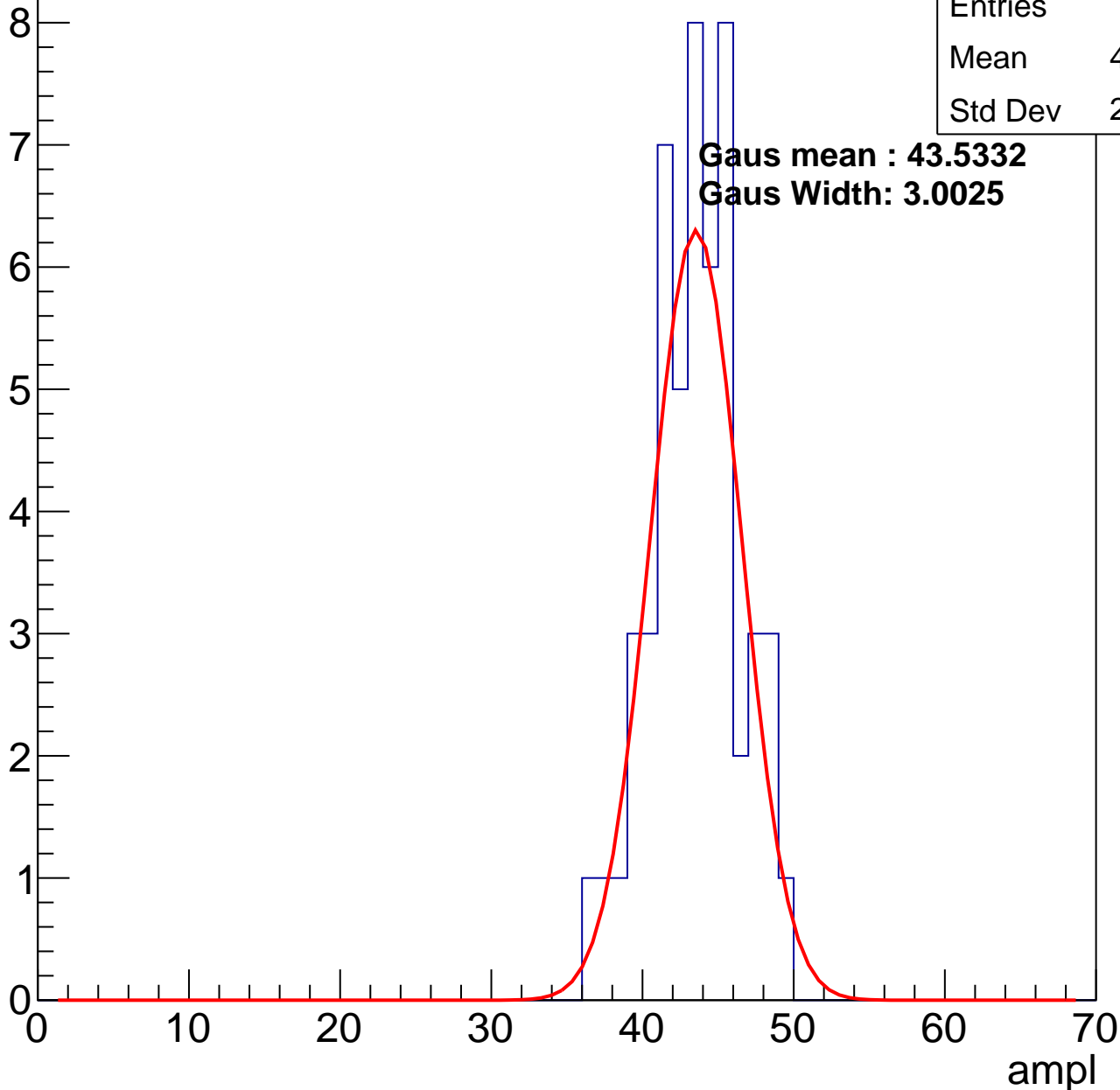
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	43.06
Std Dev	2.885

**Gaus mean : 43.5332**

**Gaus Width: 3.0025**

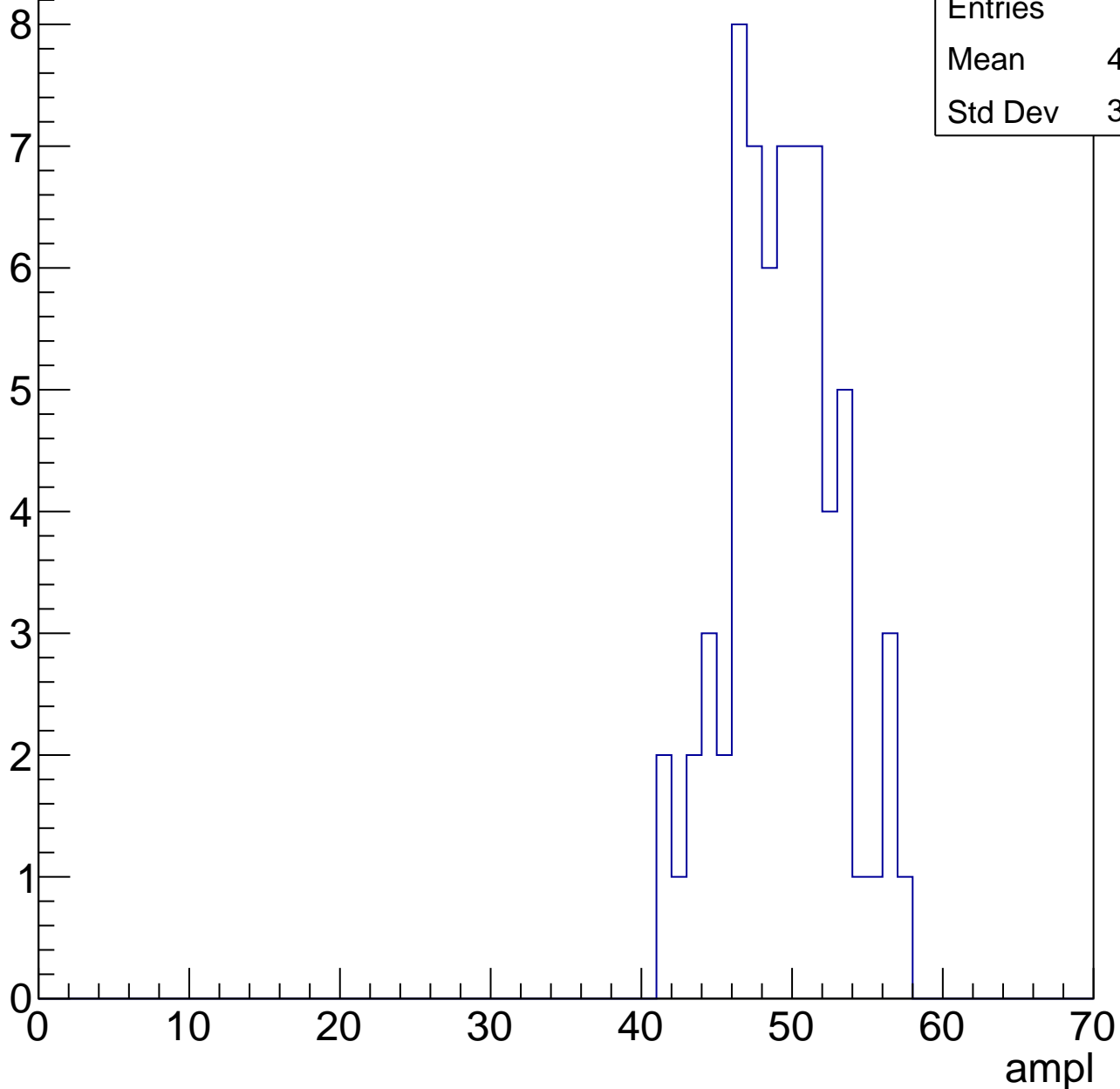


# B0L001S, U5-ch32, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

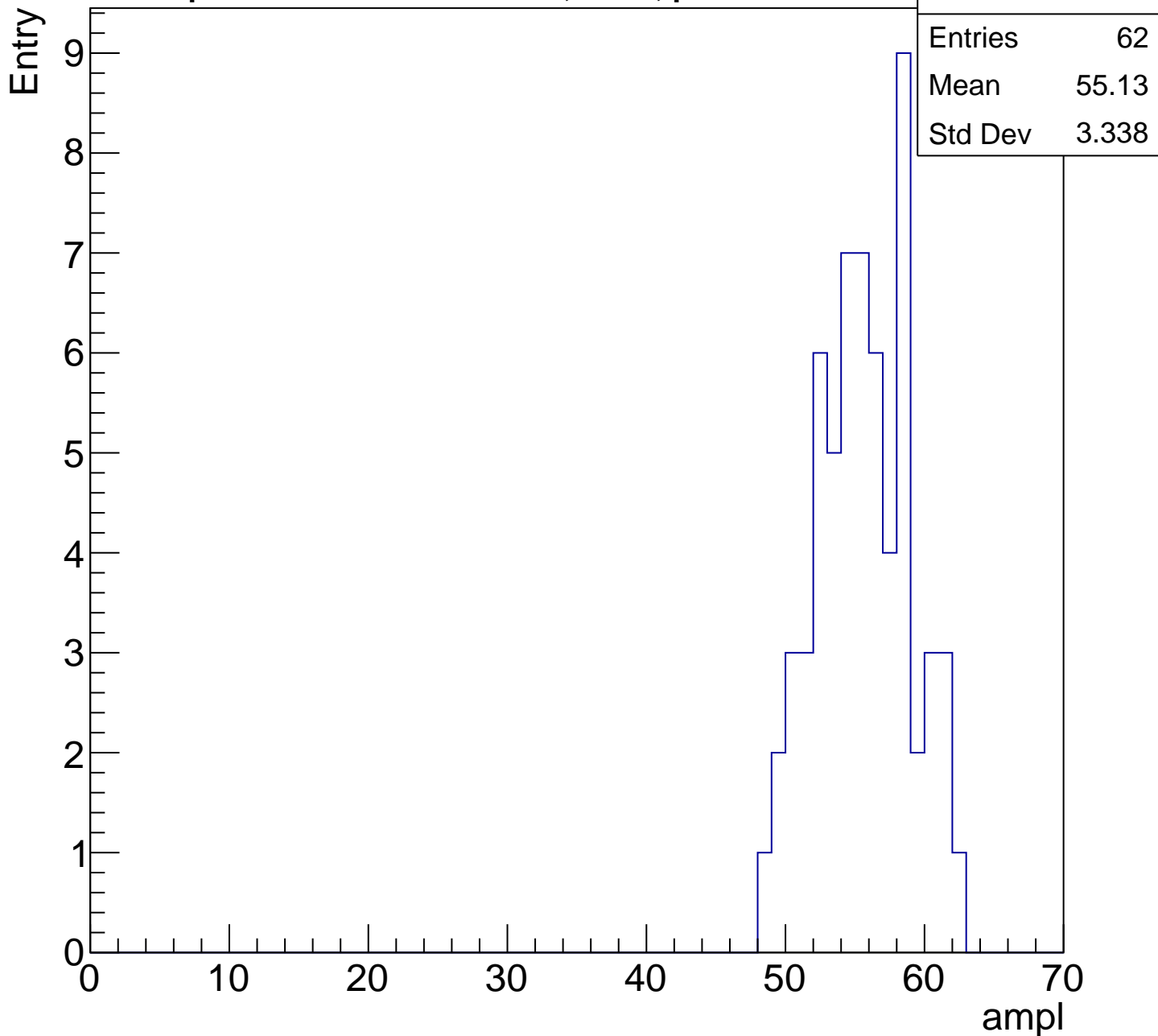
Entry

Entries	67
Mean	48.87
Std Dev	3.632



# B0L001S, U5-ch32, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U5-ch32, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

10

Entries 52

Mean 58.88

Std Dev 8.615

8

6

4

2

0

0

10

20

30

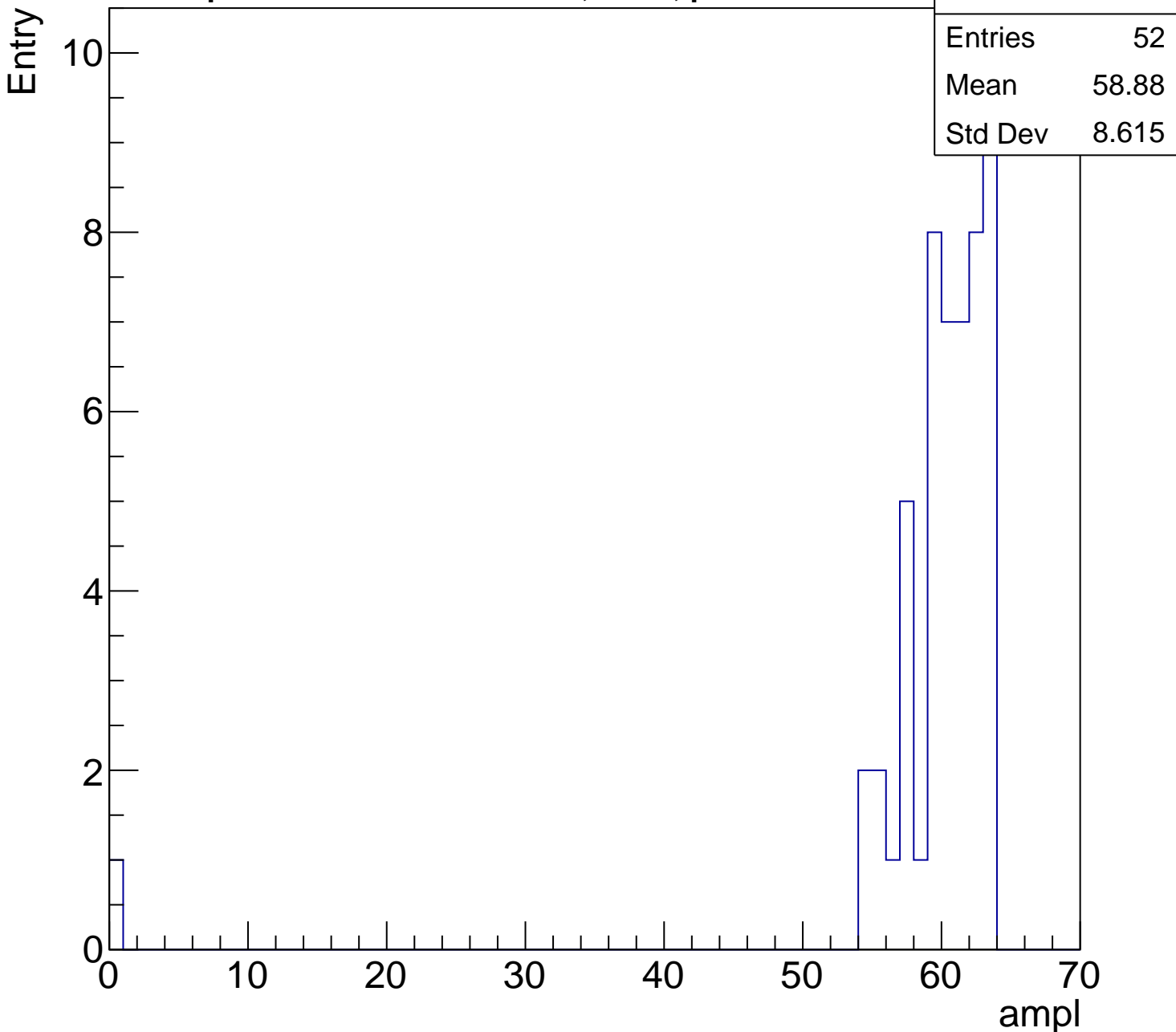
40

50

60

ampl

70



# B0L001S, U5-ch32, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch32, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

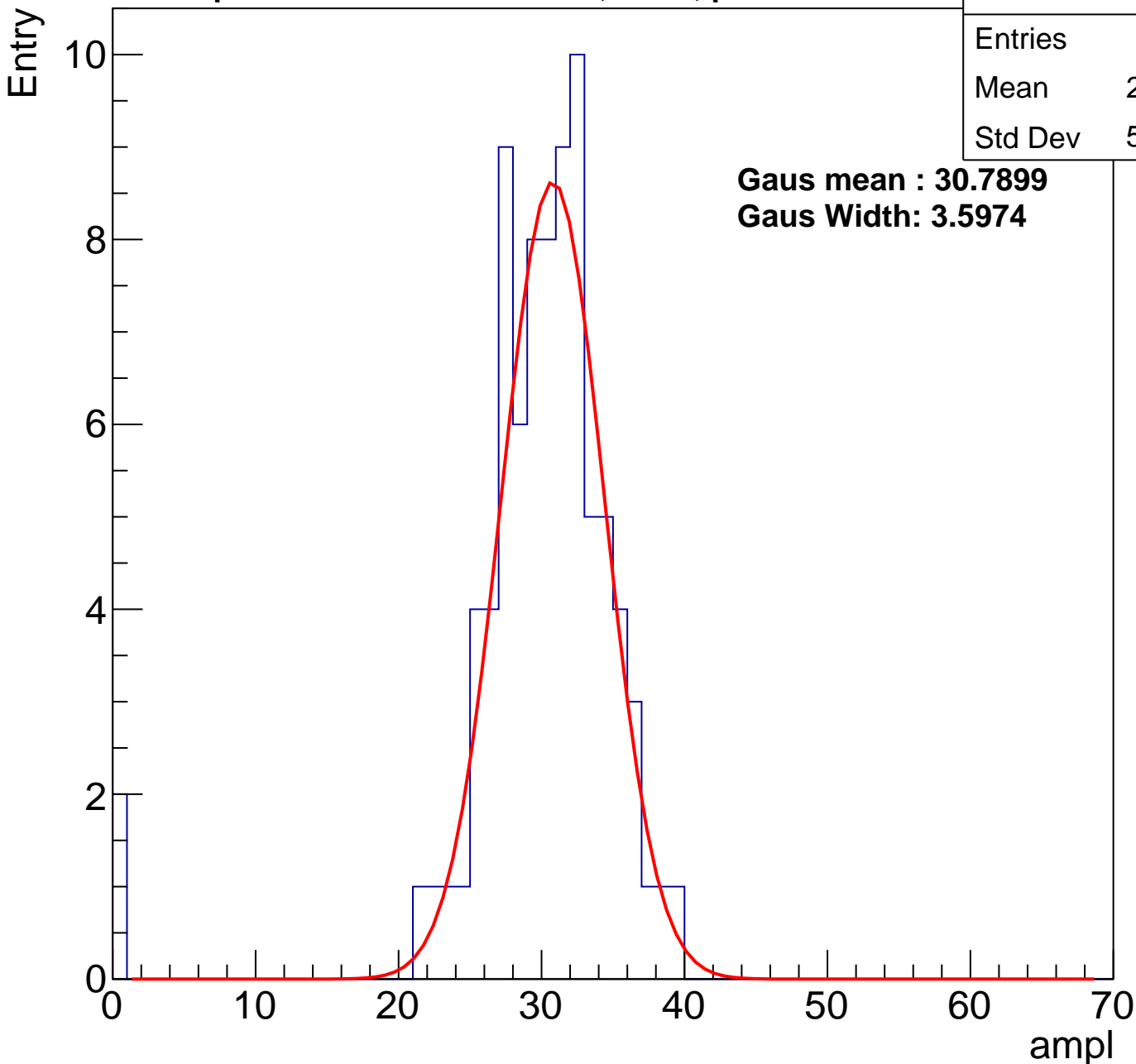
# B0L001S, U5-ch33, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	84
Mean	29.44
Std Dev	5.832

**Gaus mean : 30.7899**

**Gaus Width: 3.5974**



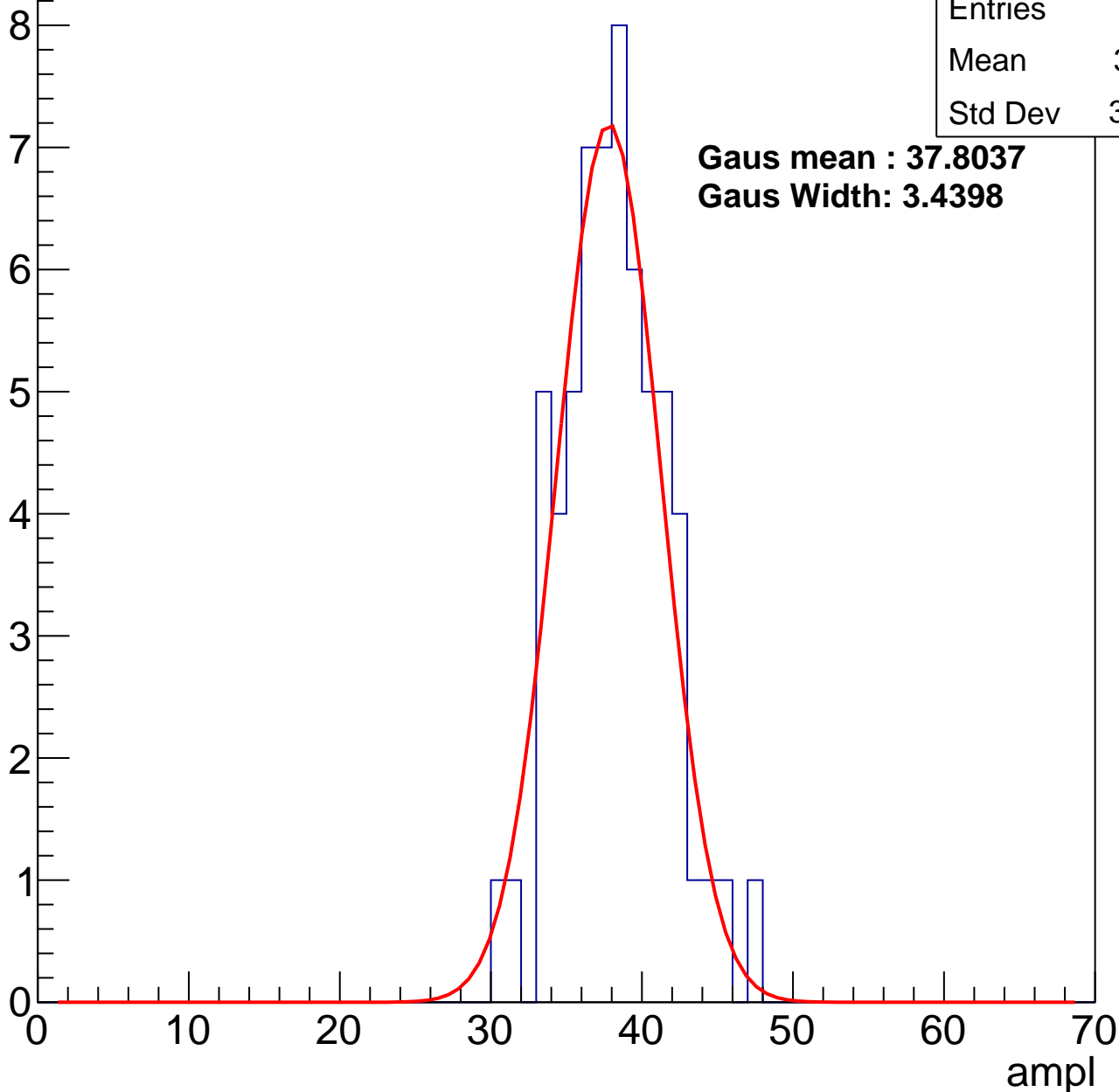
# B0L001S, U5-ch33, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	37.71
Std Dev	3.367

**Gaus mean : 37.8037**  
**Gaus Width: 3.4398**



# B0L001S, U5-ch33, adc2

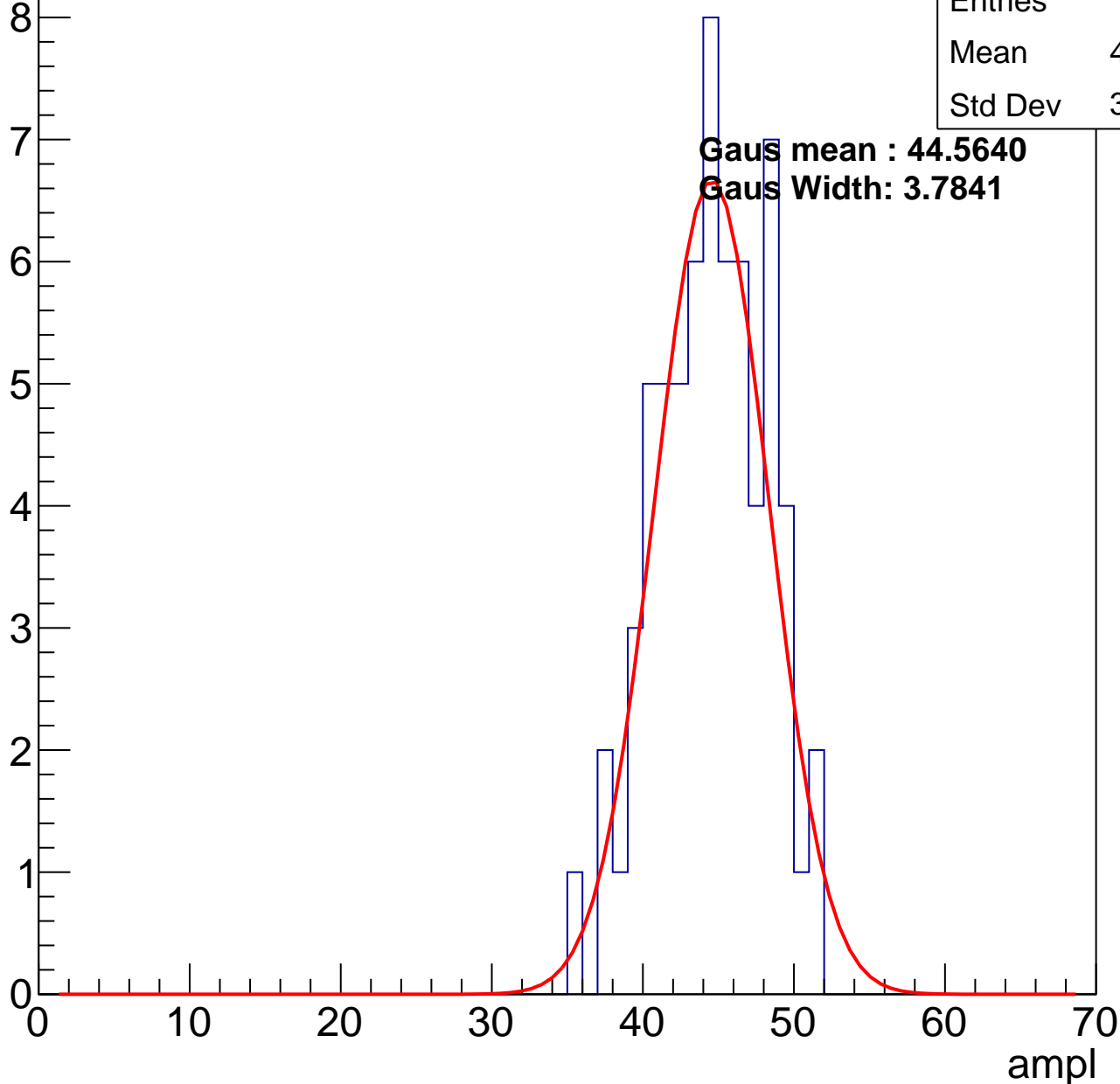
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	44.05
Std Dev	3.595

Gaus mean : 44.5640

Gaus Width: 3.7841

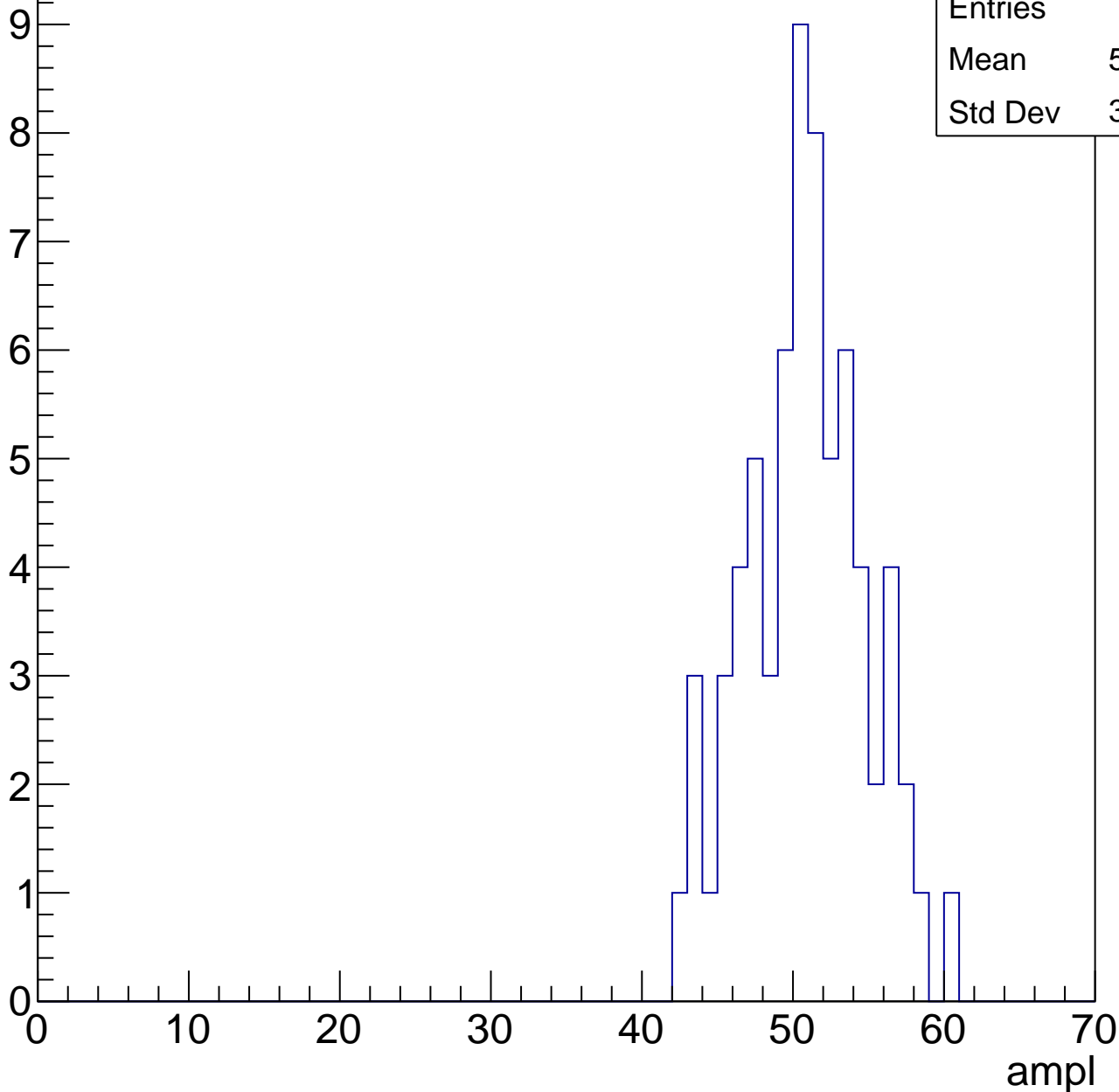


# B0L001S, U5-ch33, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

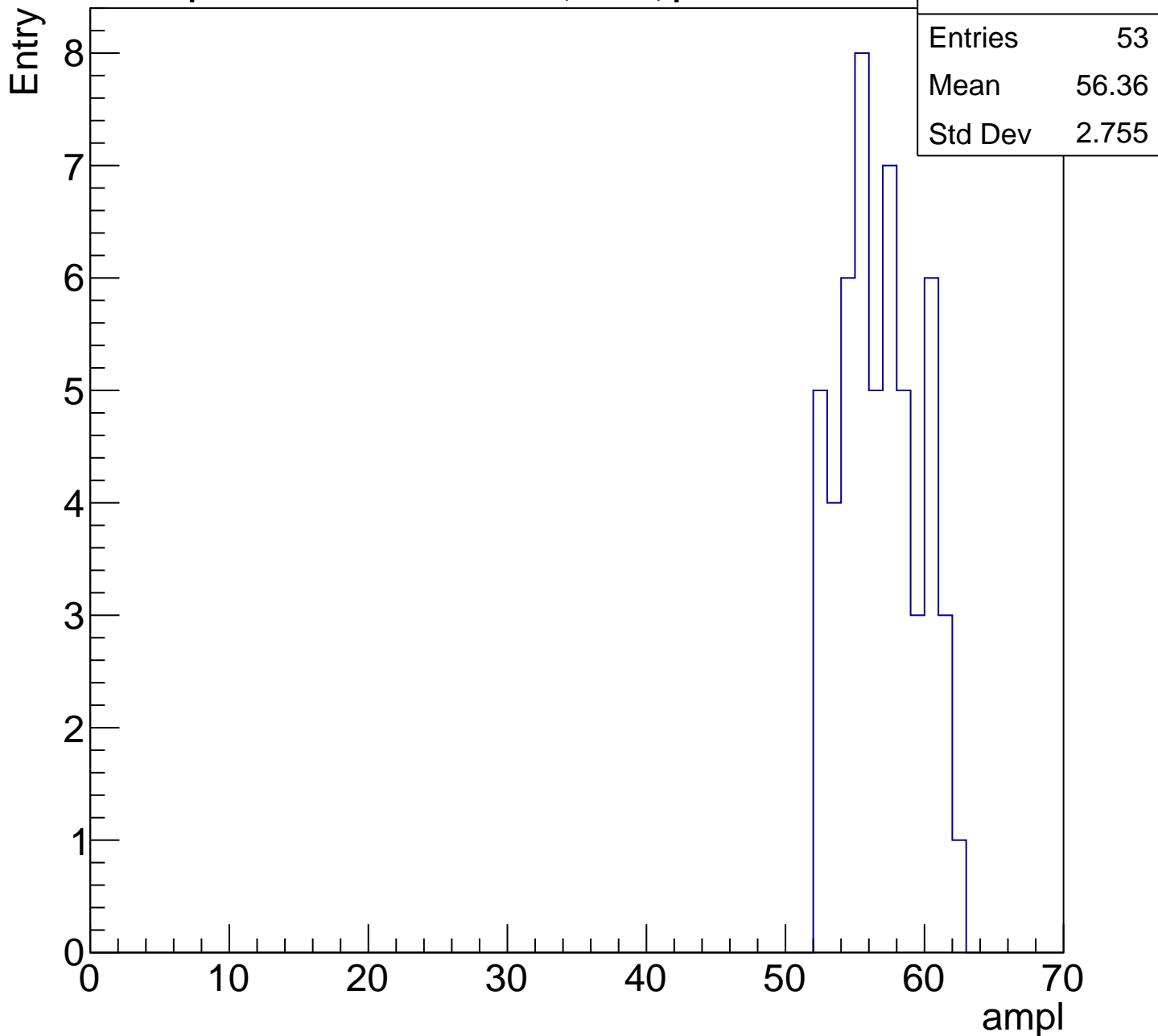
Entry

Entries	68
Mean	50.37
Std Dev	3.914



# B0L001S, U5-ch33, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U5-ch33, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

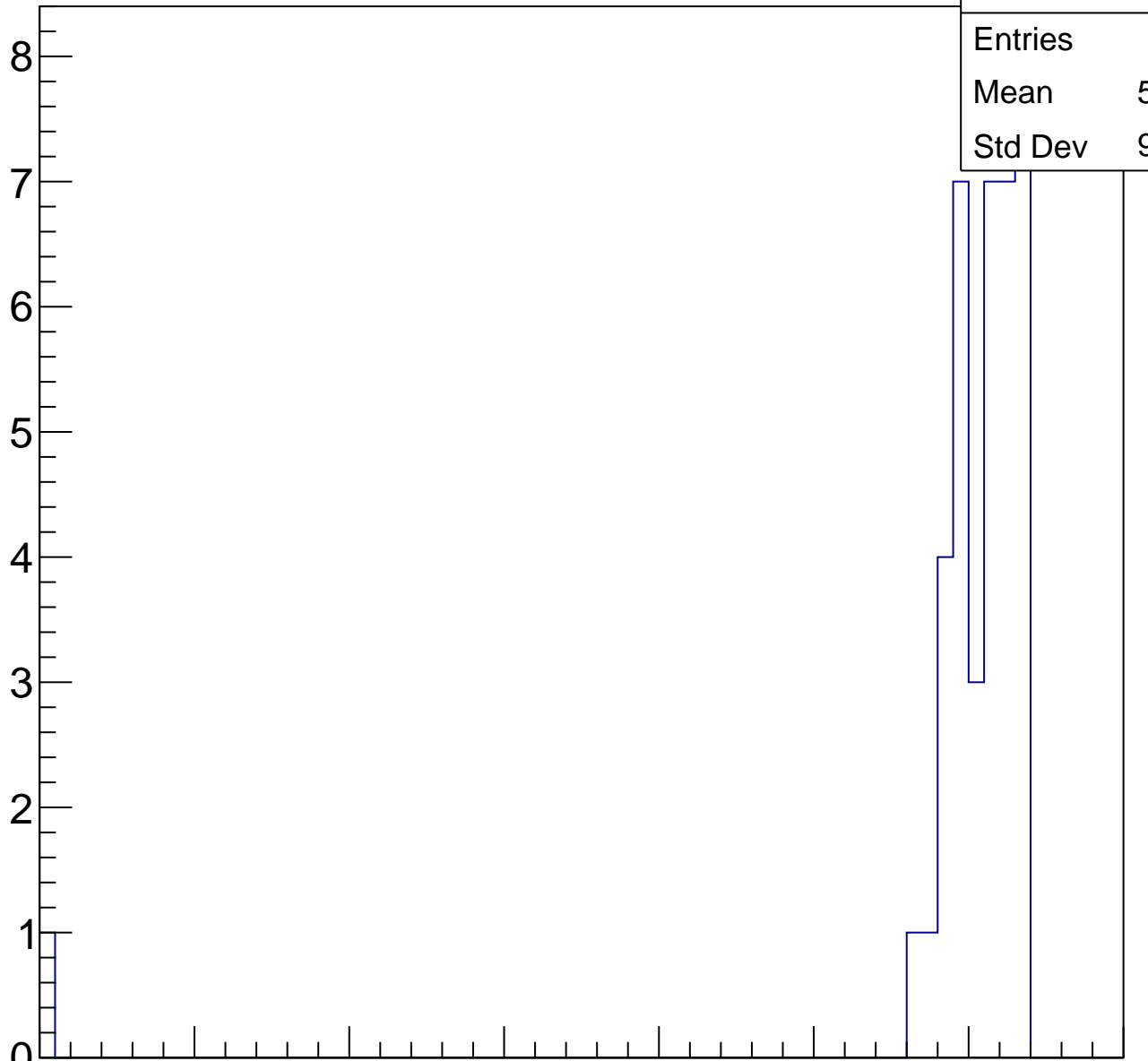
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	39
Mean	59.05
Std Dev	9.766

ampl

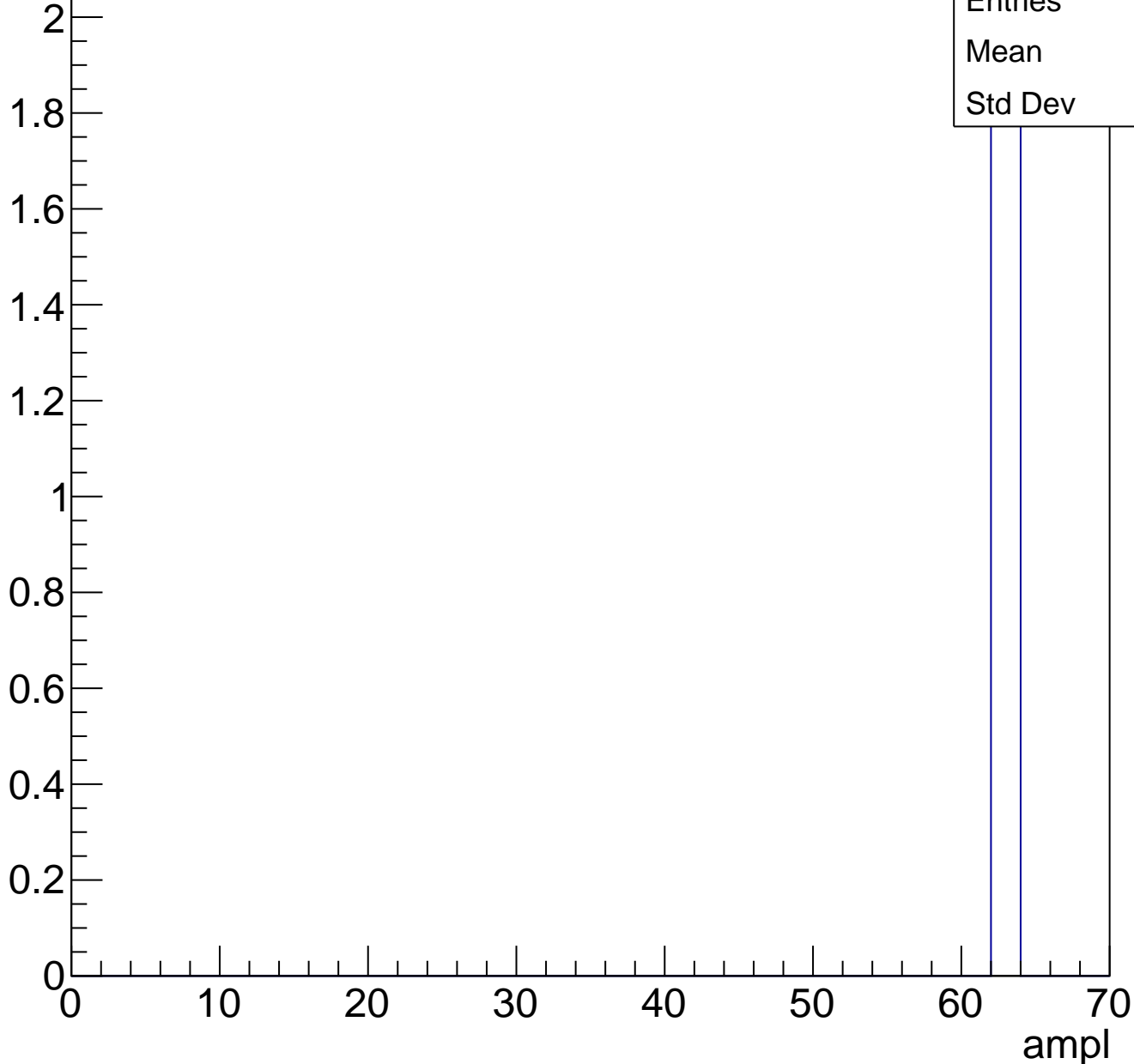
0 10 20 30 40 50 60 70



# B0L001S, U5-ch33, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch33, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U5-ch34, adc0

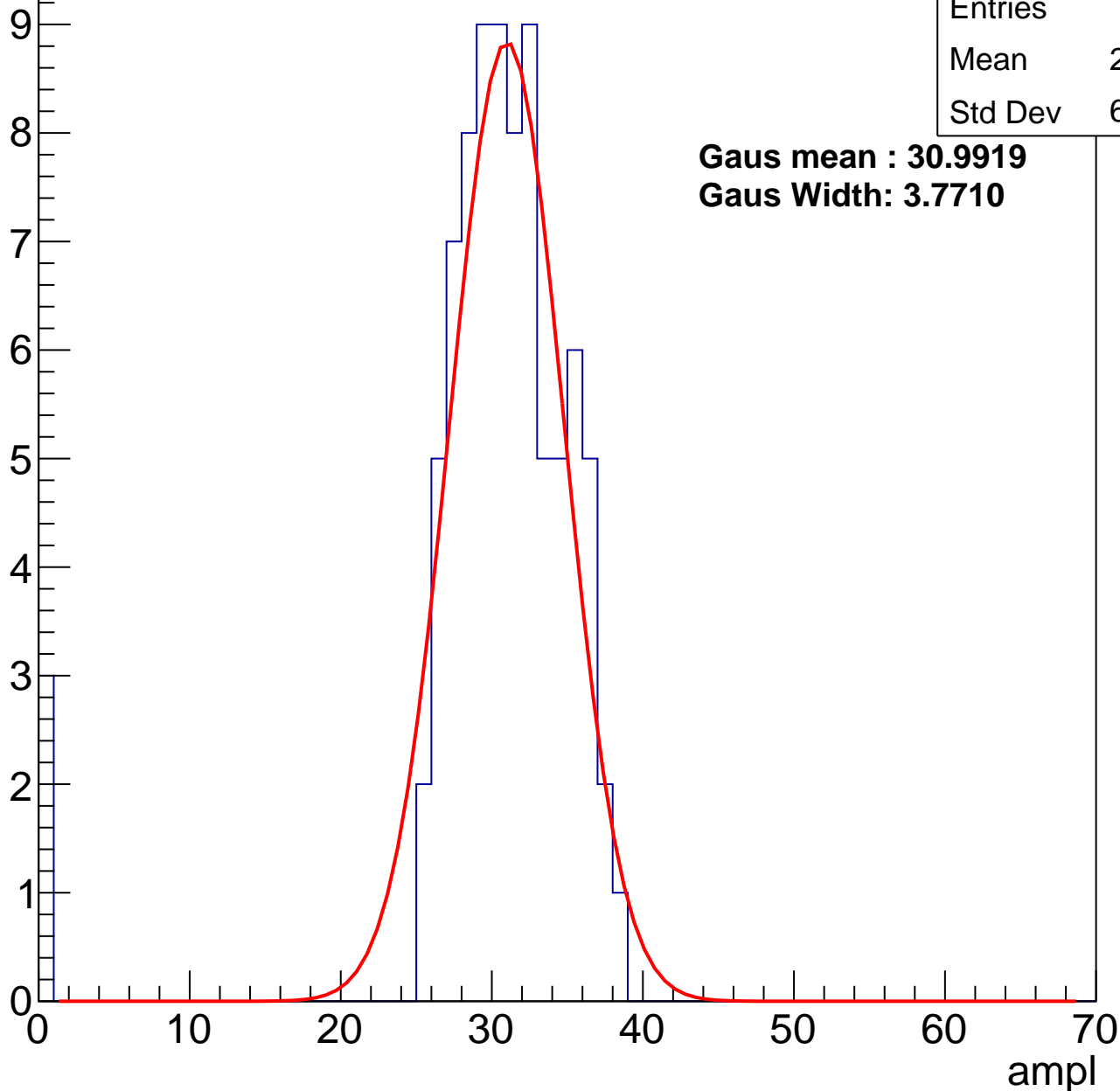
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	84
Mean	29.73
Std Dev	6.536

**Gaus mean : 30.9919**

**Gaus Width: 3.7710**



# B0L001S, U5-ch34, adc1

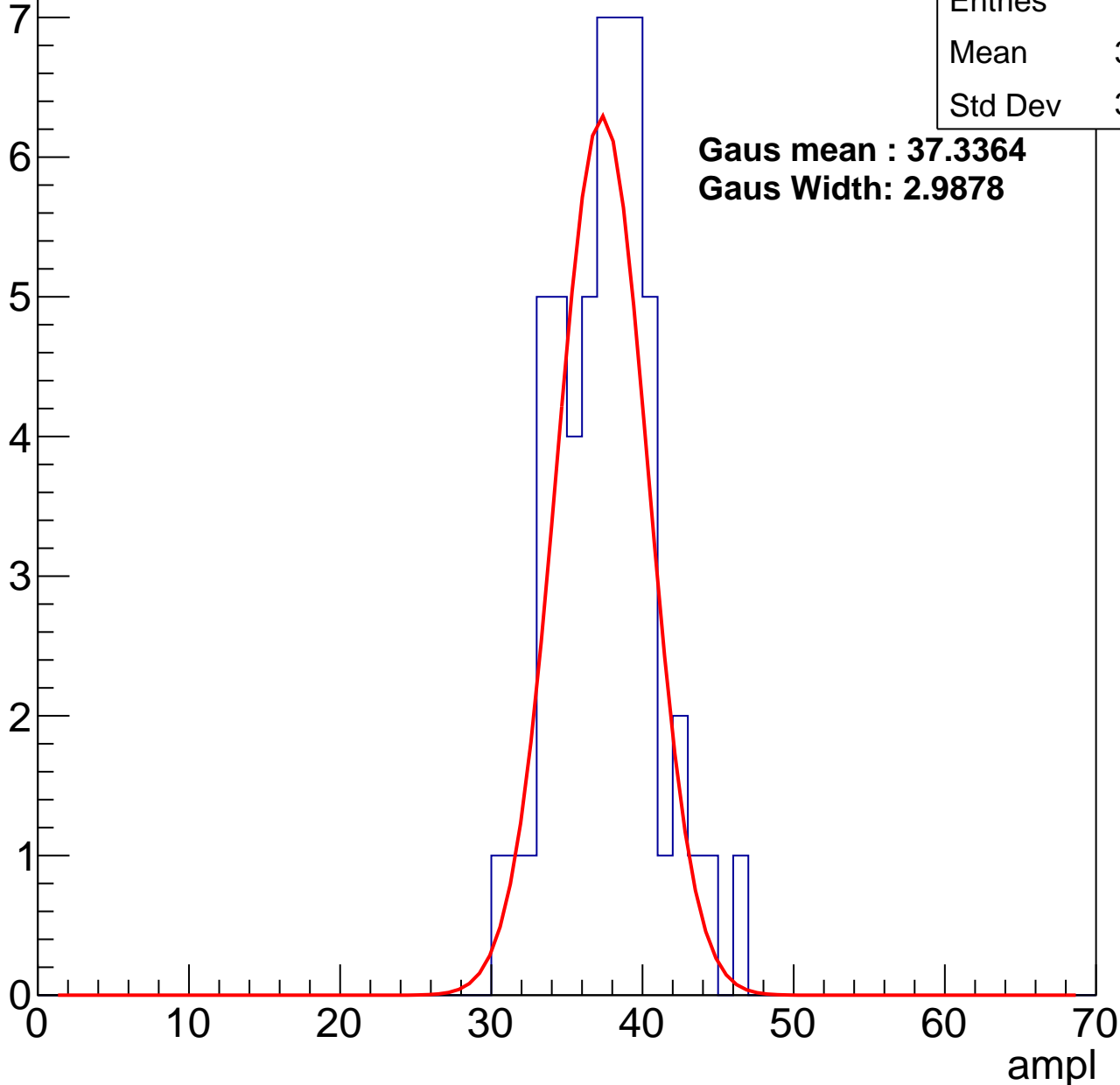
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	37.11
Std Dev	3.241

**Gaus mean : 37.3364**

**Gaus Width: 2.9878**



# B0L001S, U5-ch34, adc2

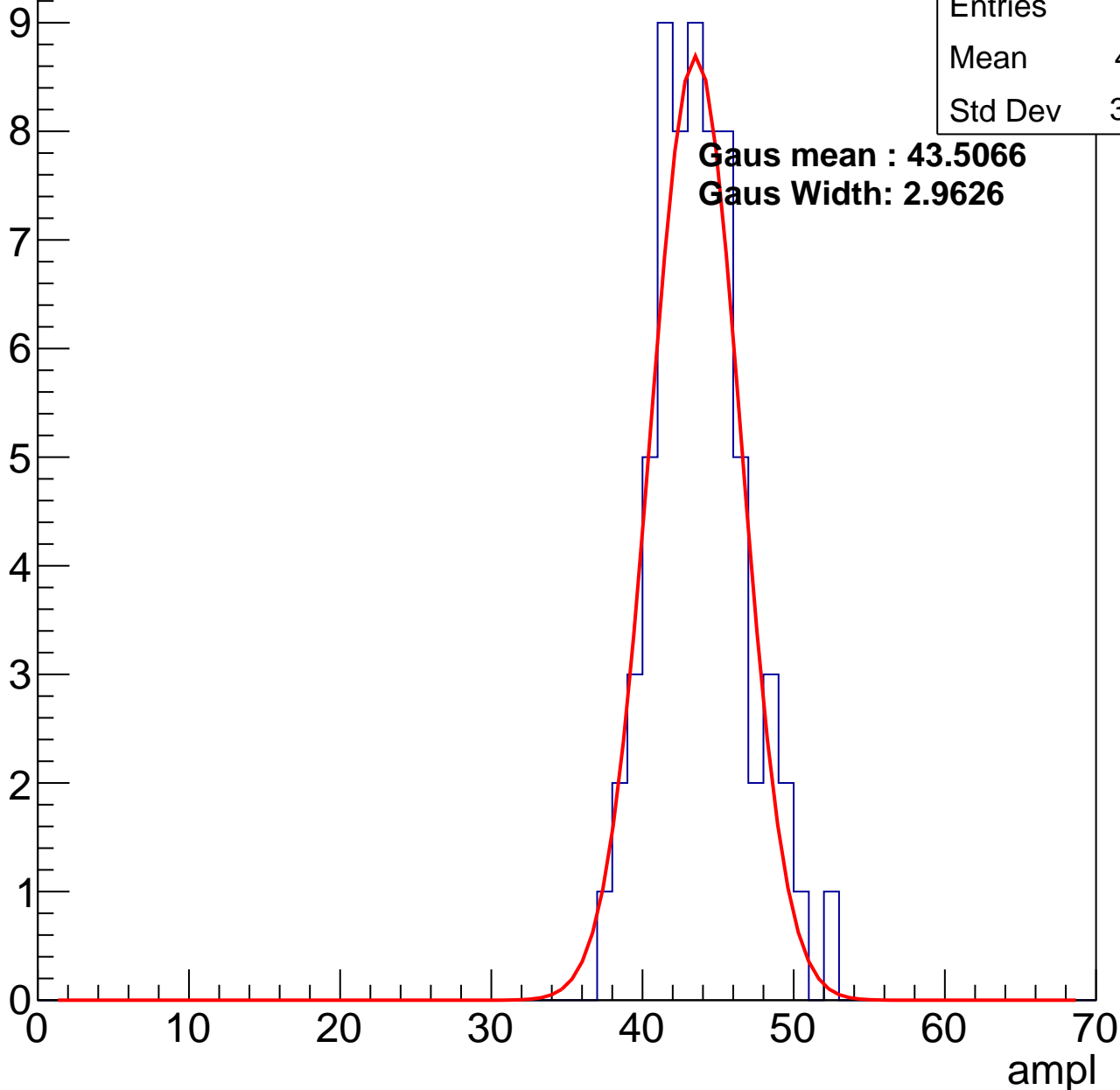
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	43.31
Std Dev	3.018

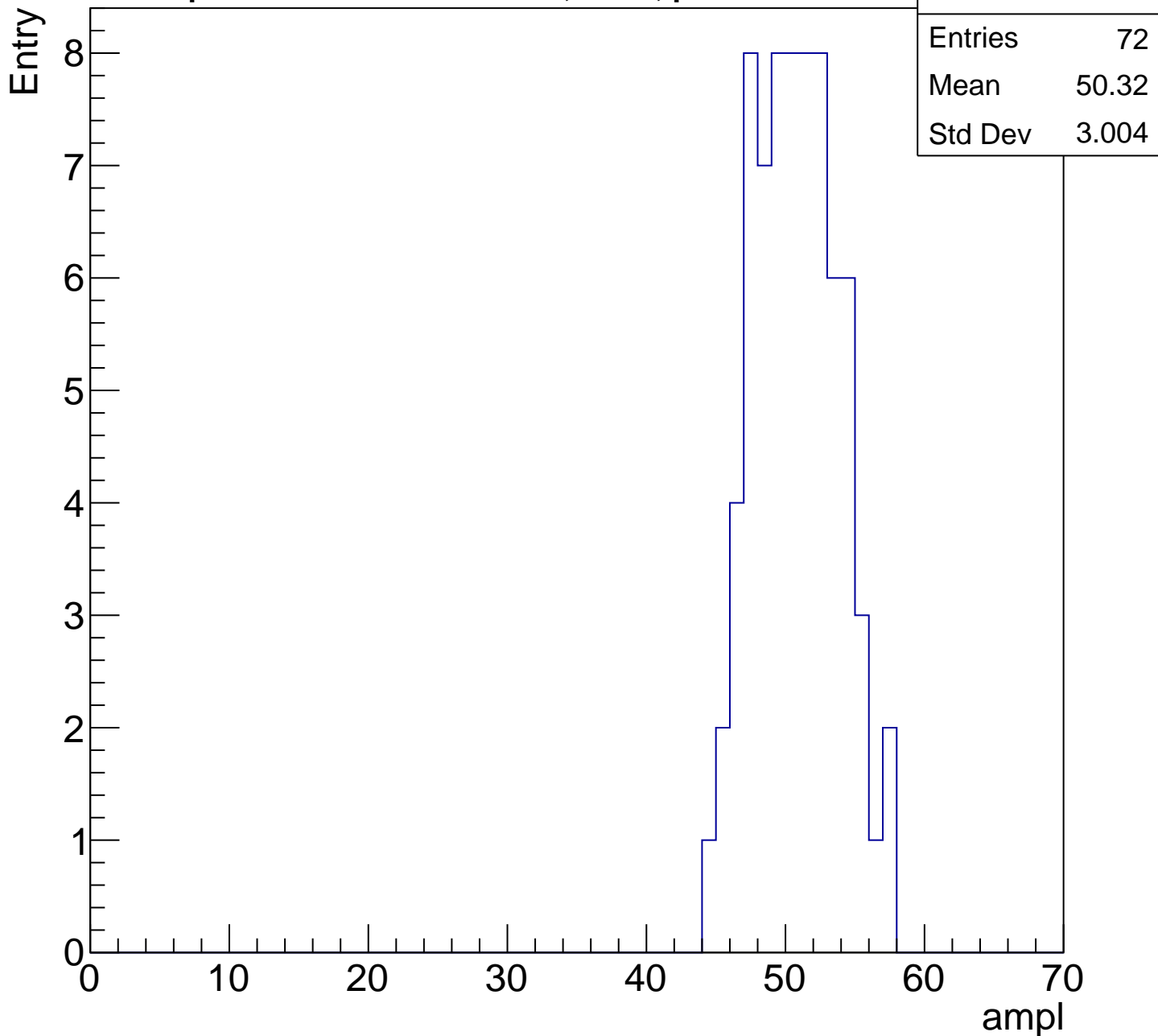
**Gaus mean : 43.5066**

**Gaus Width: 2.9626**



# B0L001S, U5-ch34, adc3

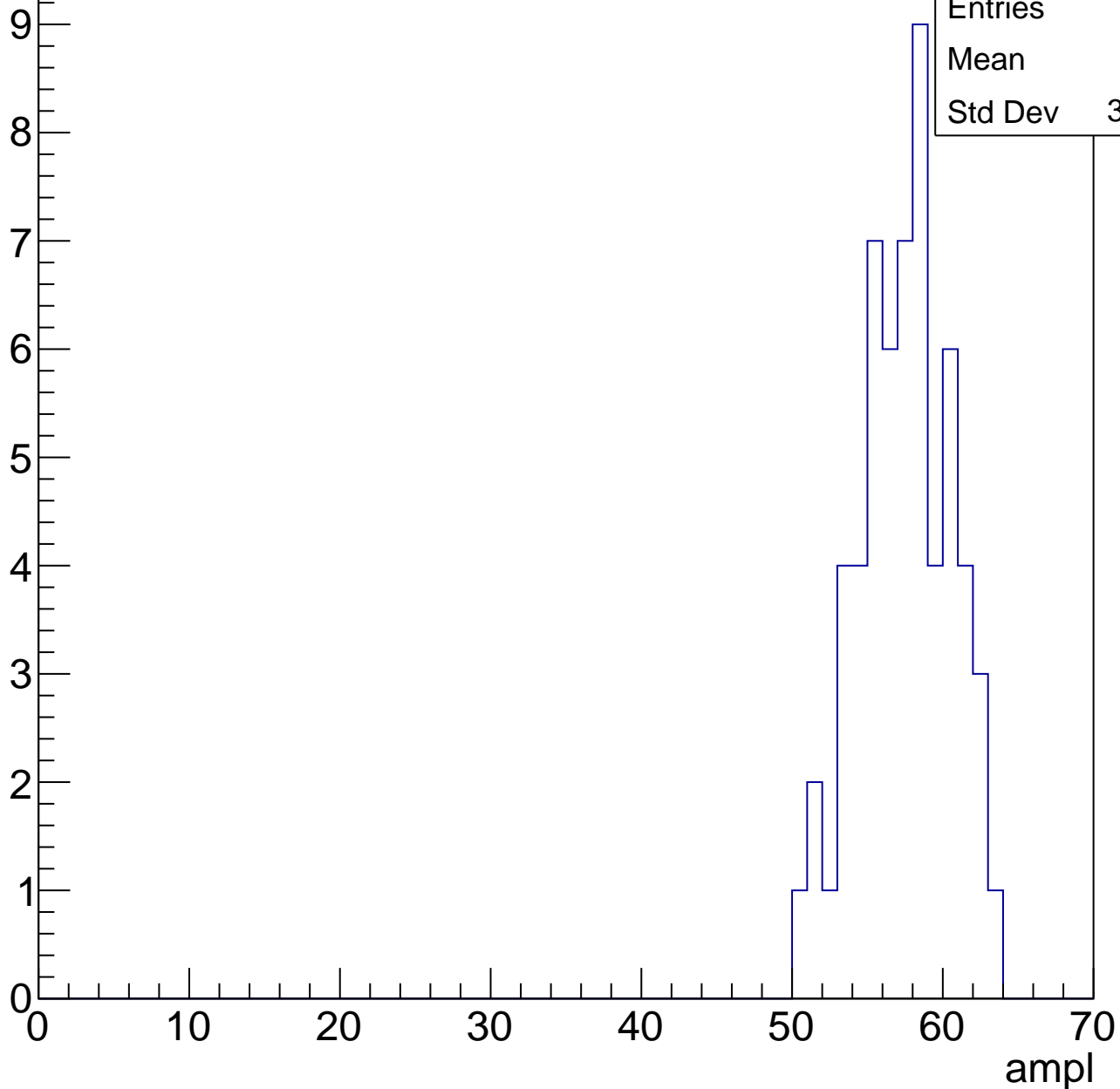
calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U5-ch34, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

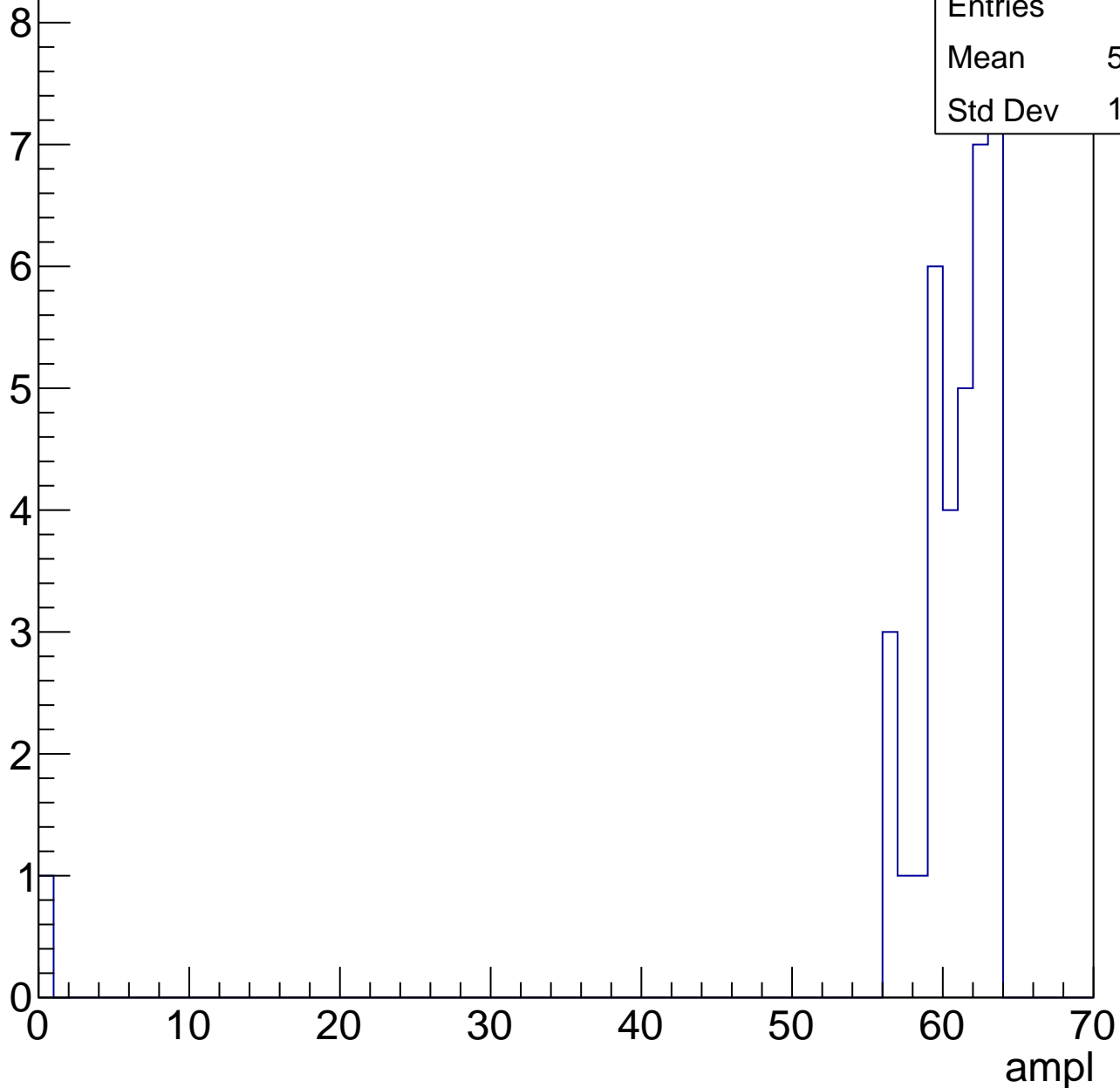


# B0L001S, U5-ch34, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

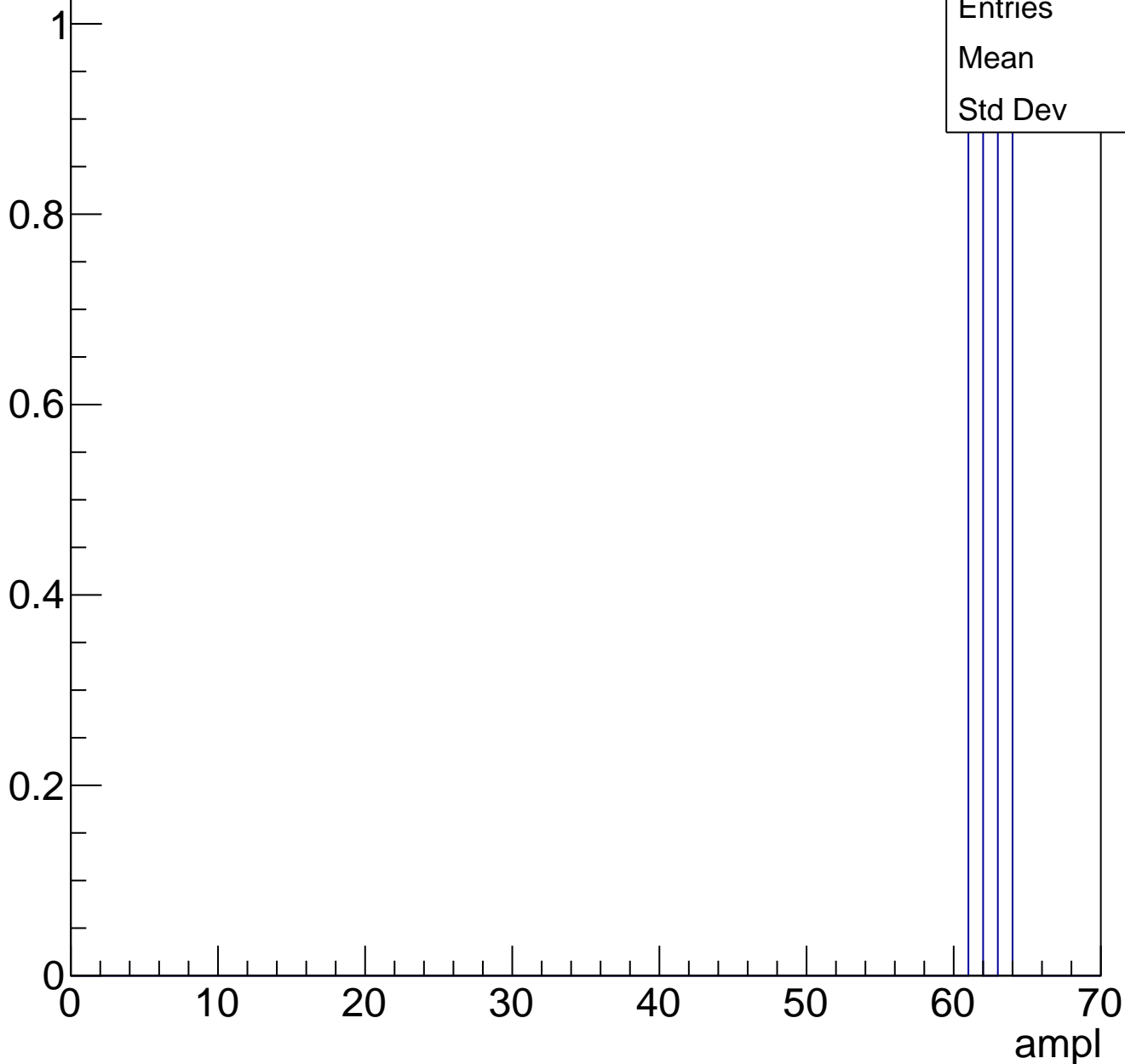
Entries	36
Mean	58.89
Std Dev	10.18



# B0L001S, U5-ch34, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch34, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L001S, U5-ch35, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	80
Mean	31.18
Std Dev	5.019

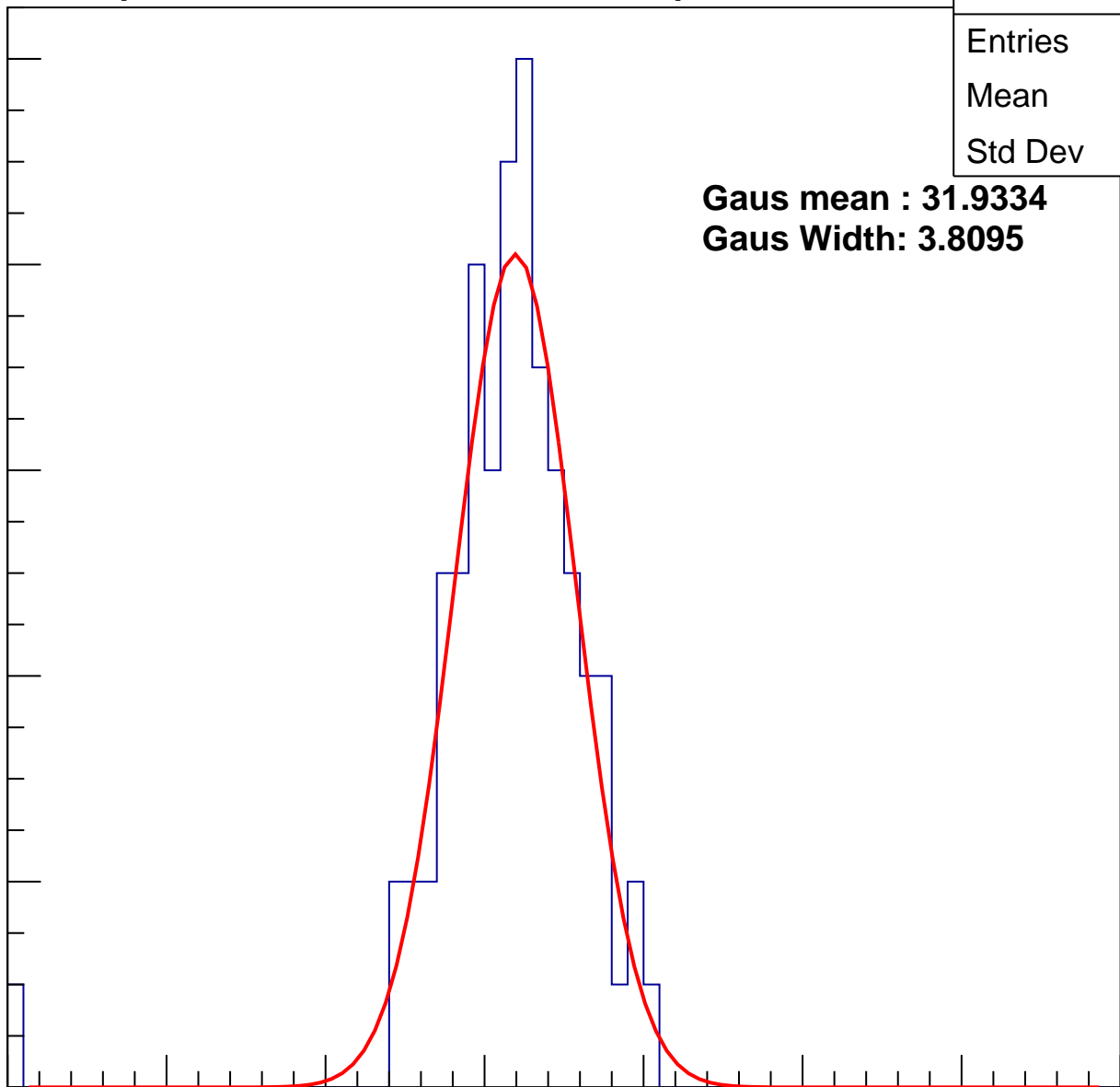
**Gaus mean : 31.9334**

**Gaus Width: 3.8095**

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U5-ch35, adc1

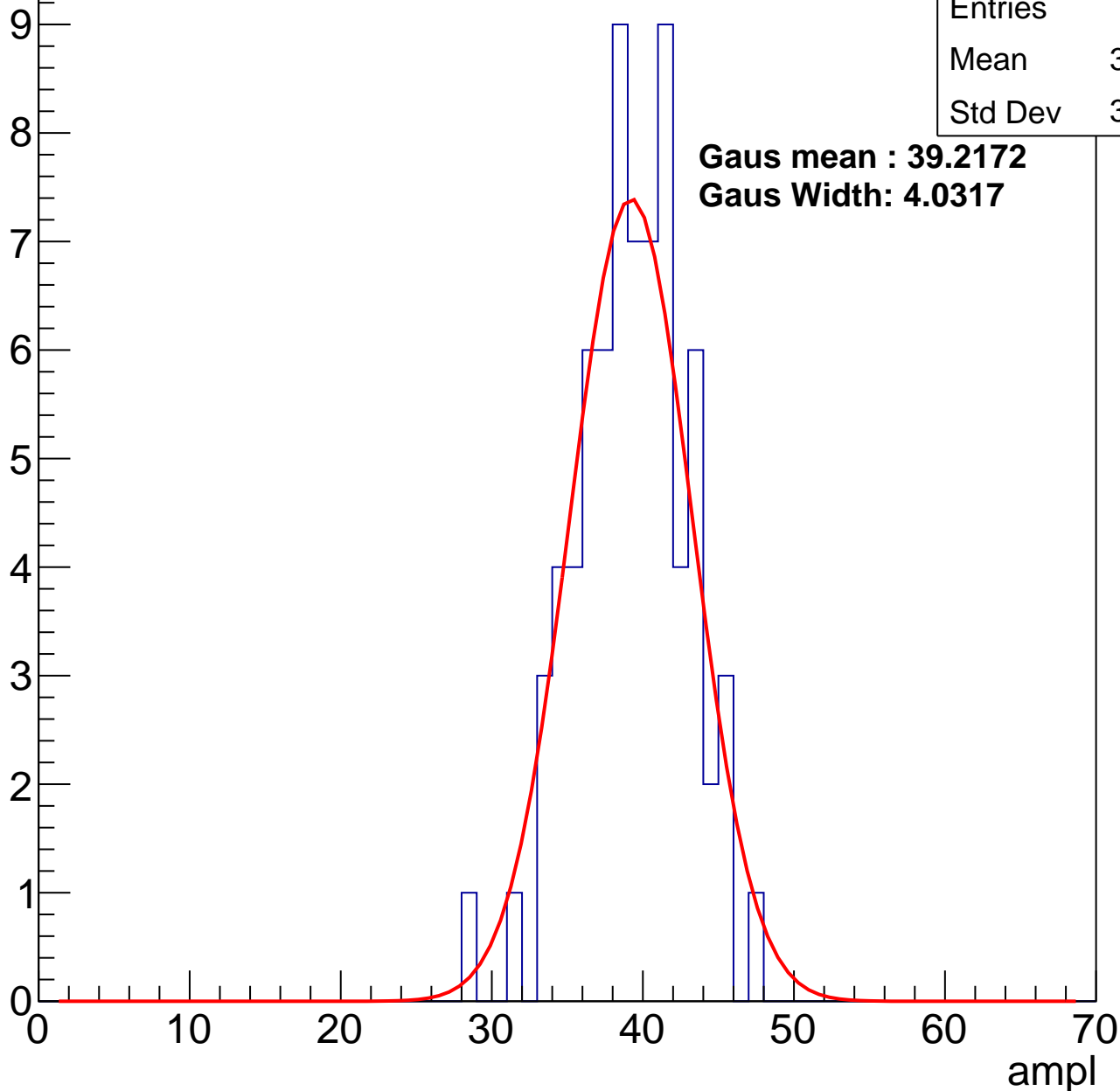
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	38.79
Std Dev	3.584

**Gaus mean : 39.2172**

**Gaus Width: 4.0317**



# B0L001S, U5-ch35, adc2

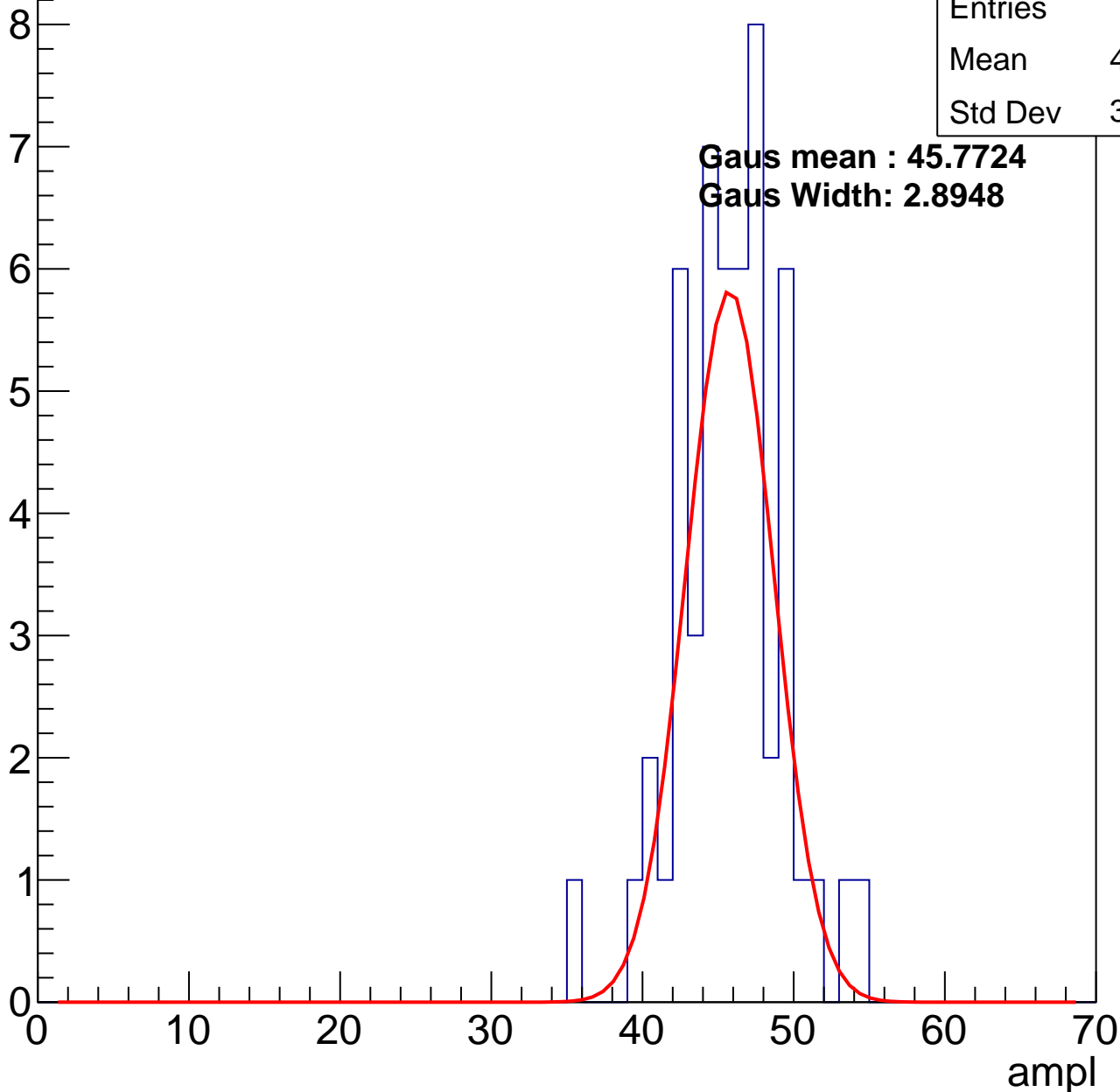
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	45.36
Std Dev	3.437

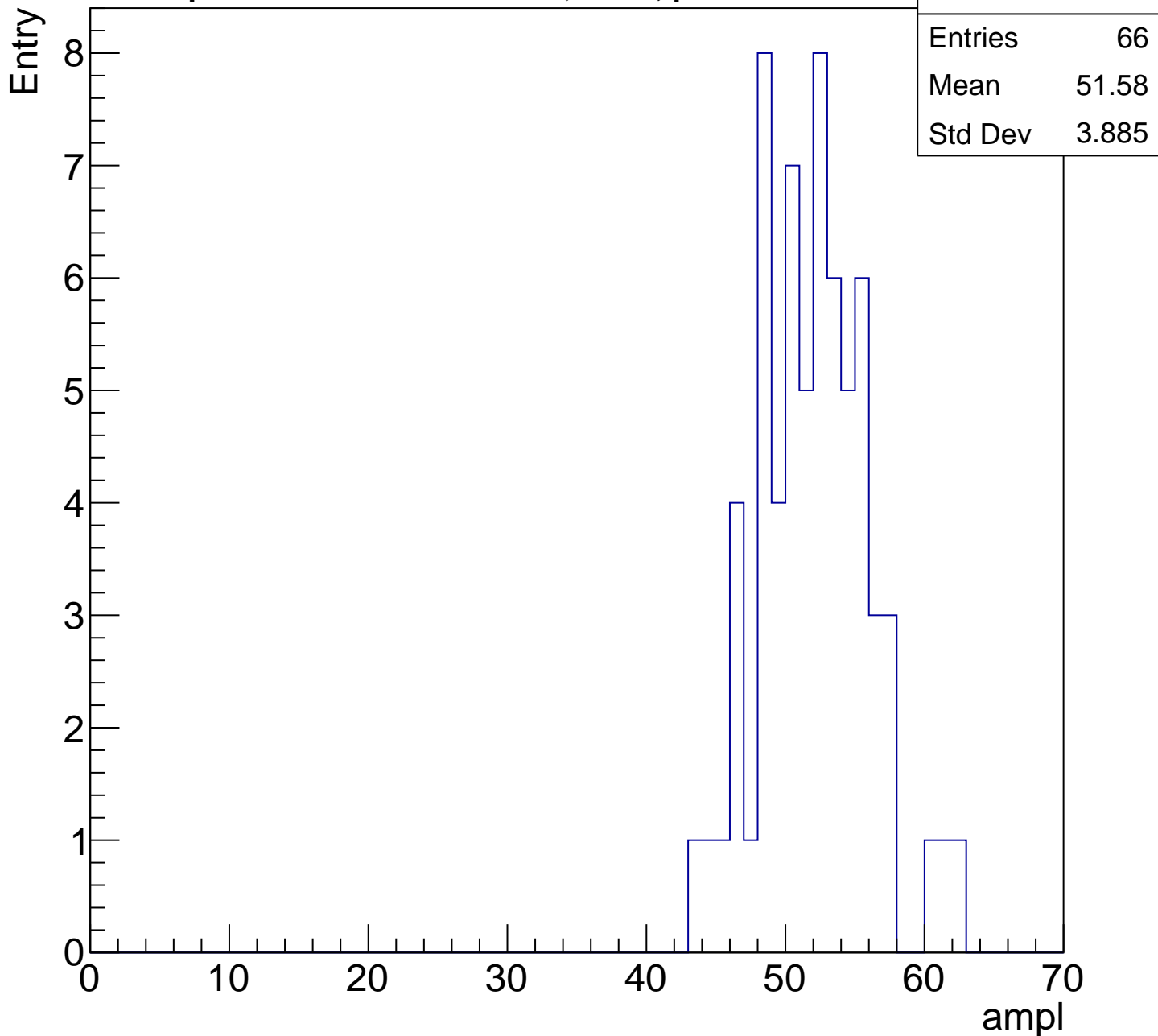
**Gaus mean : 45.7724**

**Gaus Width: 2.8948**



# B0L001S, U5-ch35, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

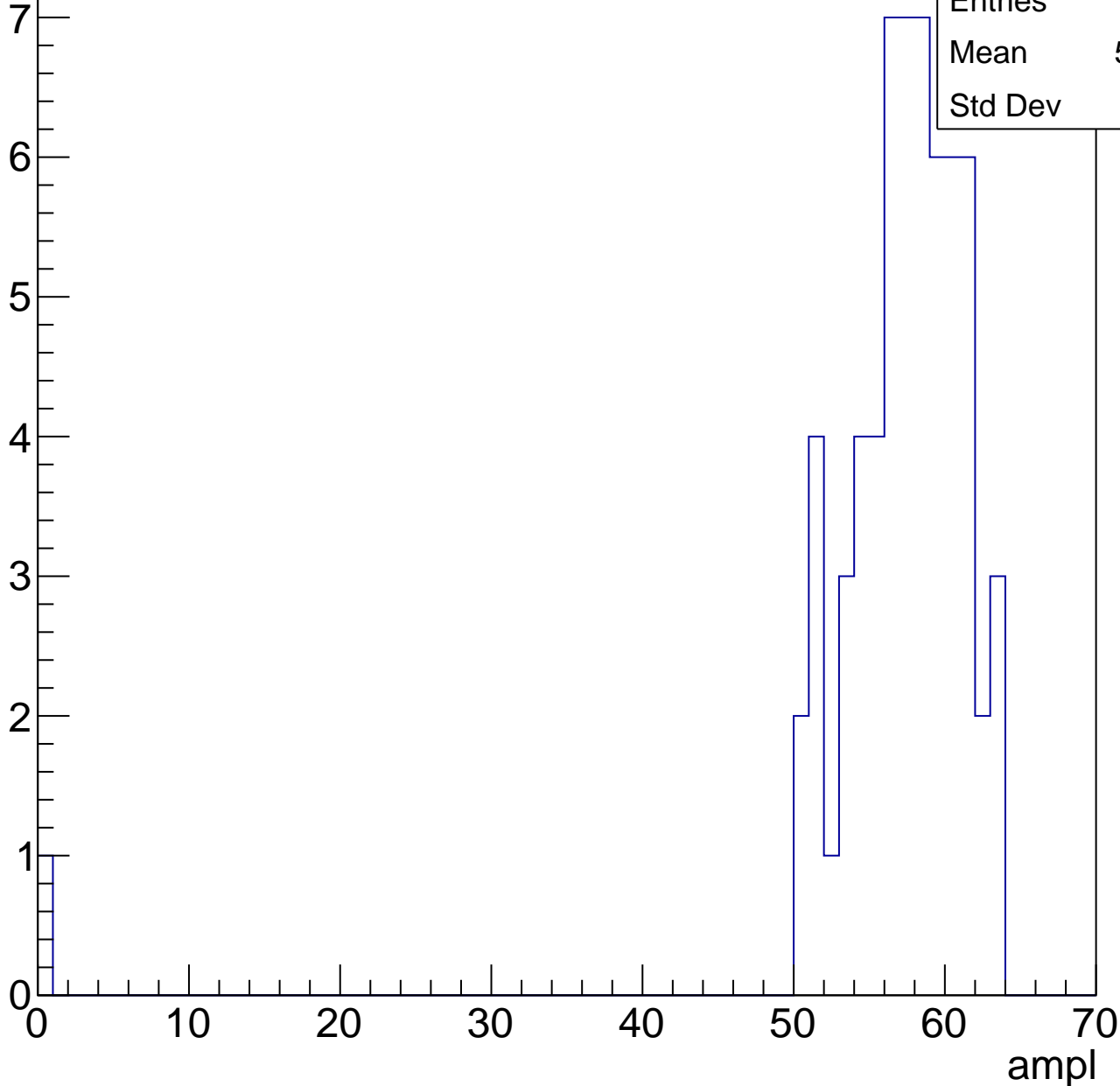


# B0L001S, U5-ch35, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	56.21
Std Dev	7.89

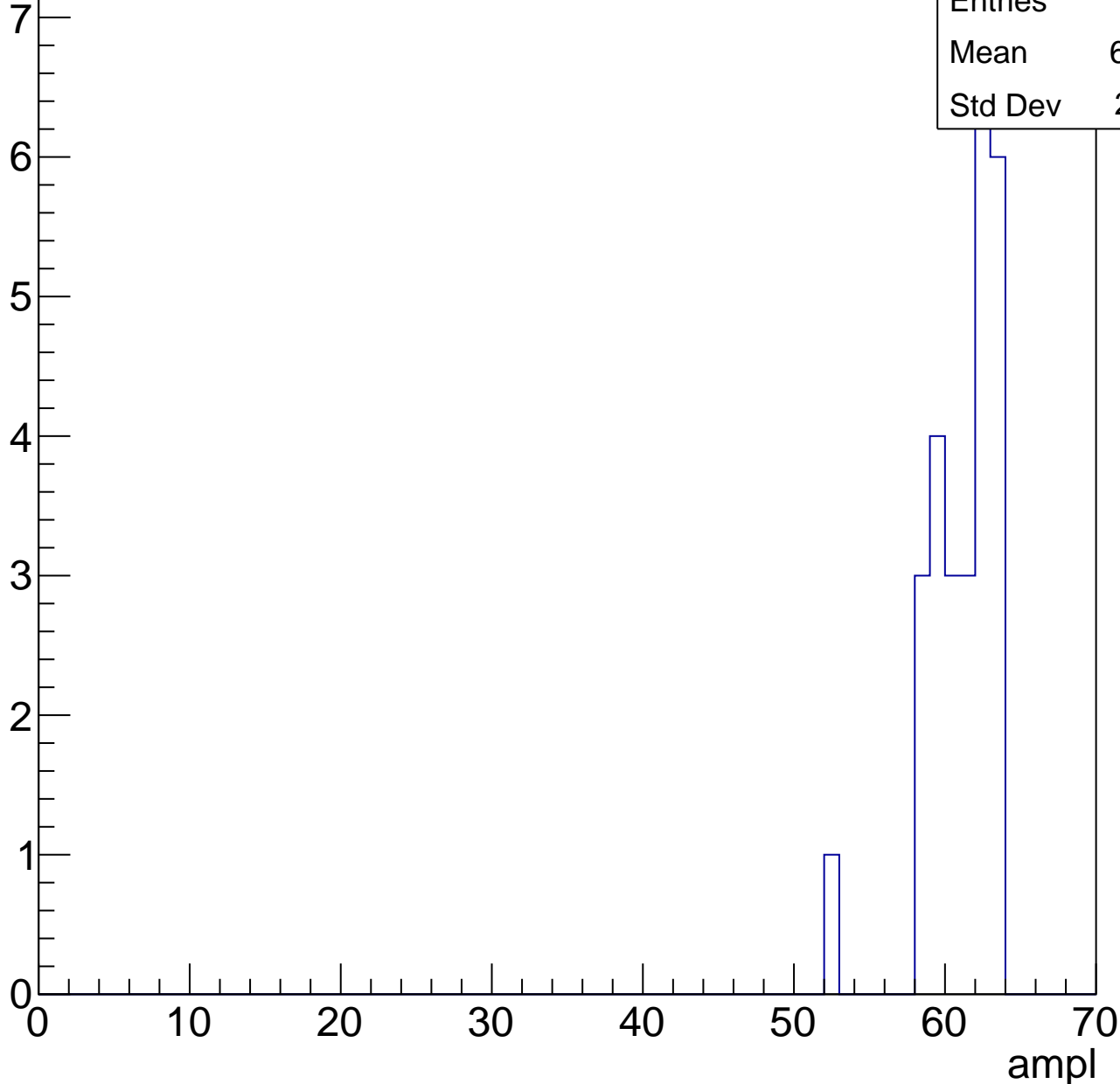


# B0L001S, U5-ch35, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	27
Mean	60.63
Std Dev	2.391



# B0L001S, U5-ch35, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch35, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U5-ch36, adc0

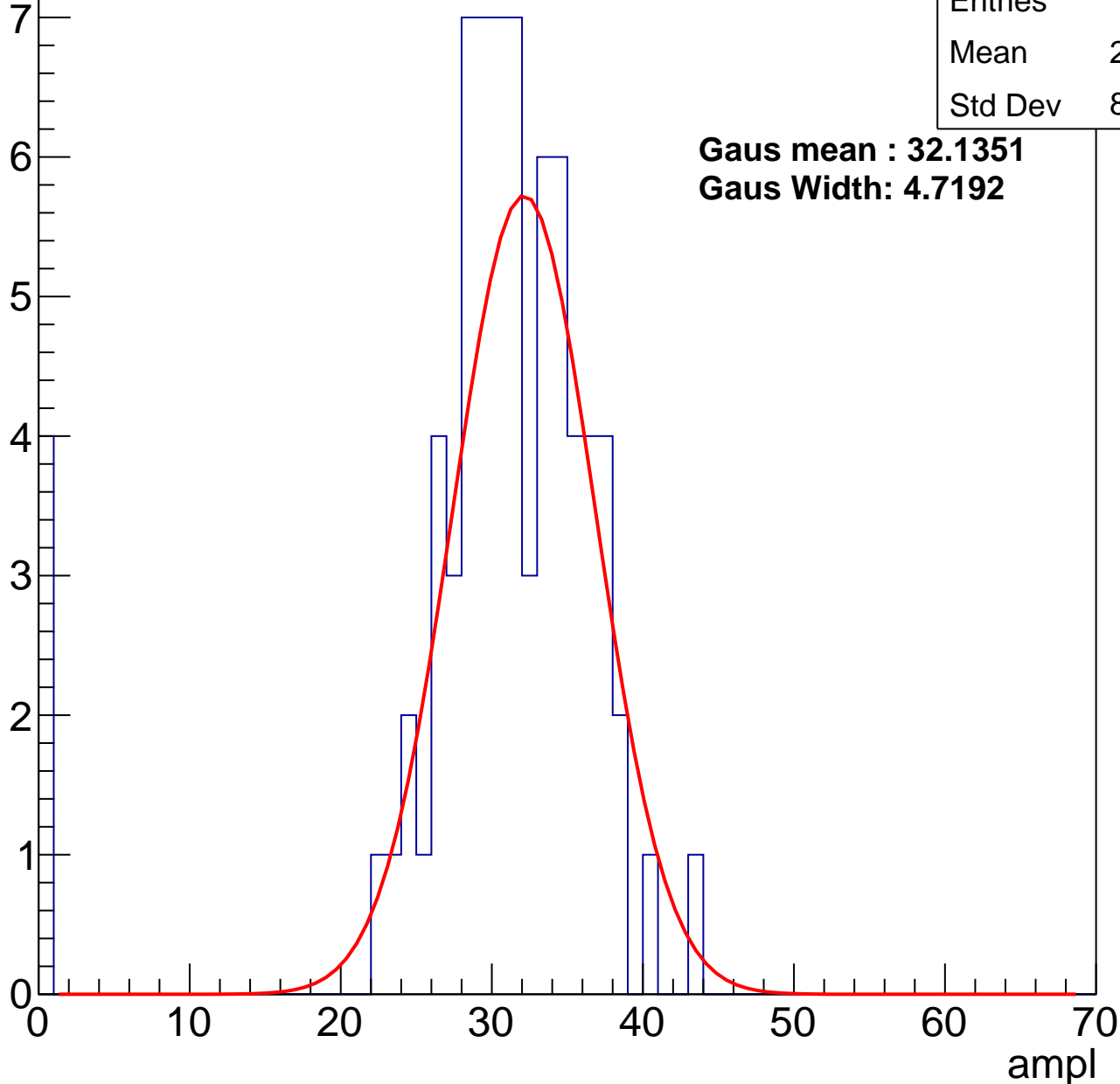
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	75
Mean	29.57
Std Dev	8.106

**Gaus mean : 32.1351**

**Gaus Width: 4.7192**



# B0L001S, U5-ch36, adc1

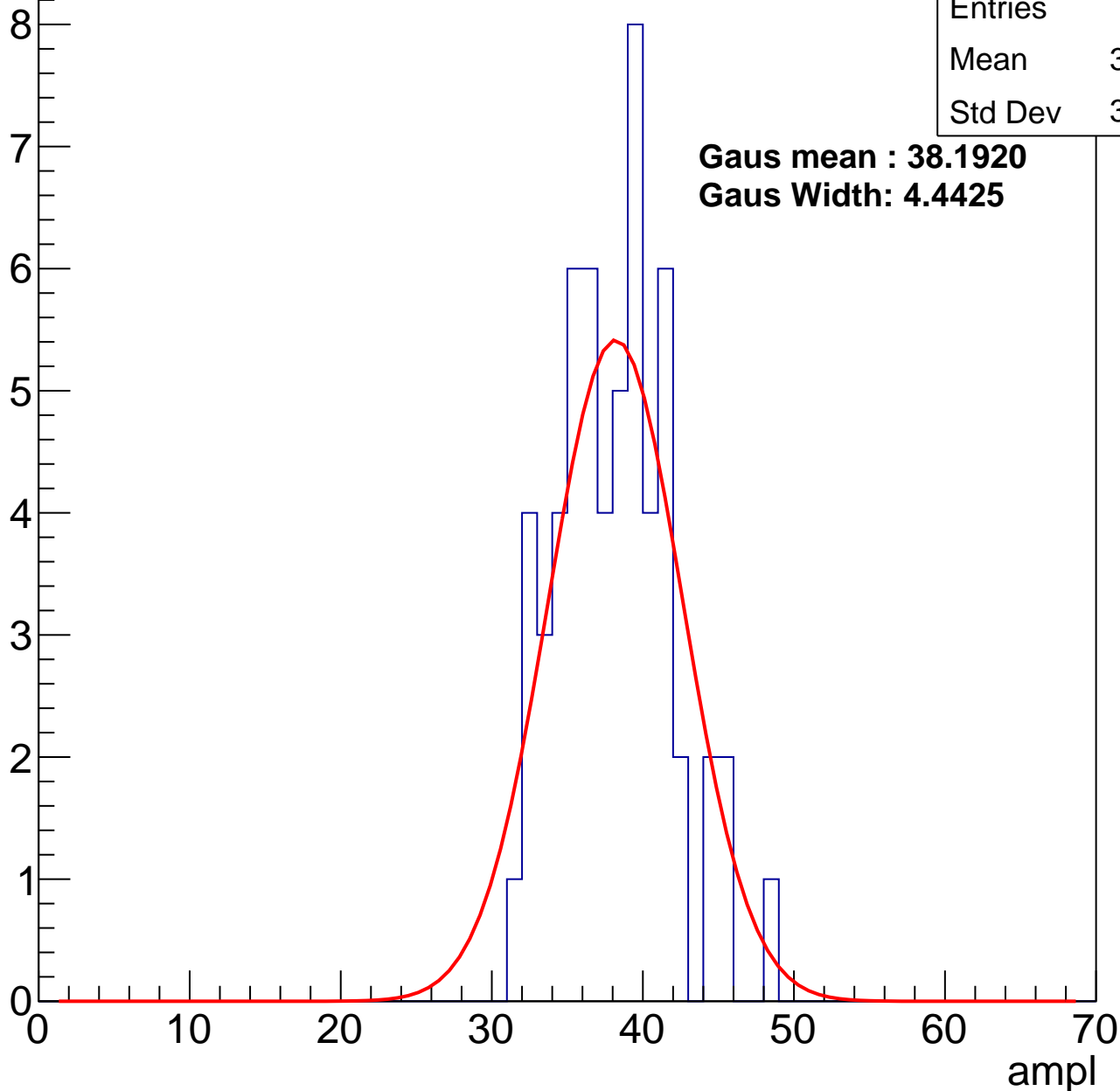
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	37.69
Std Dev	3.687

**Gaus mean : 38.1920**

**Gaus Width: 4.4425**



# B0L001S, U5-ch36, adc2

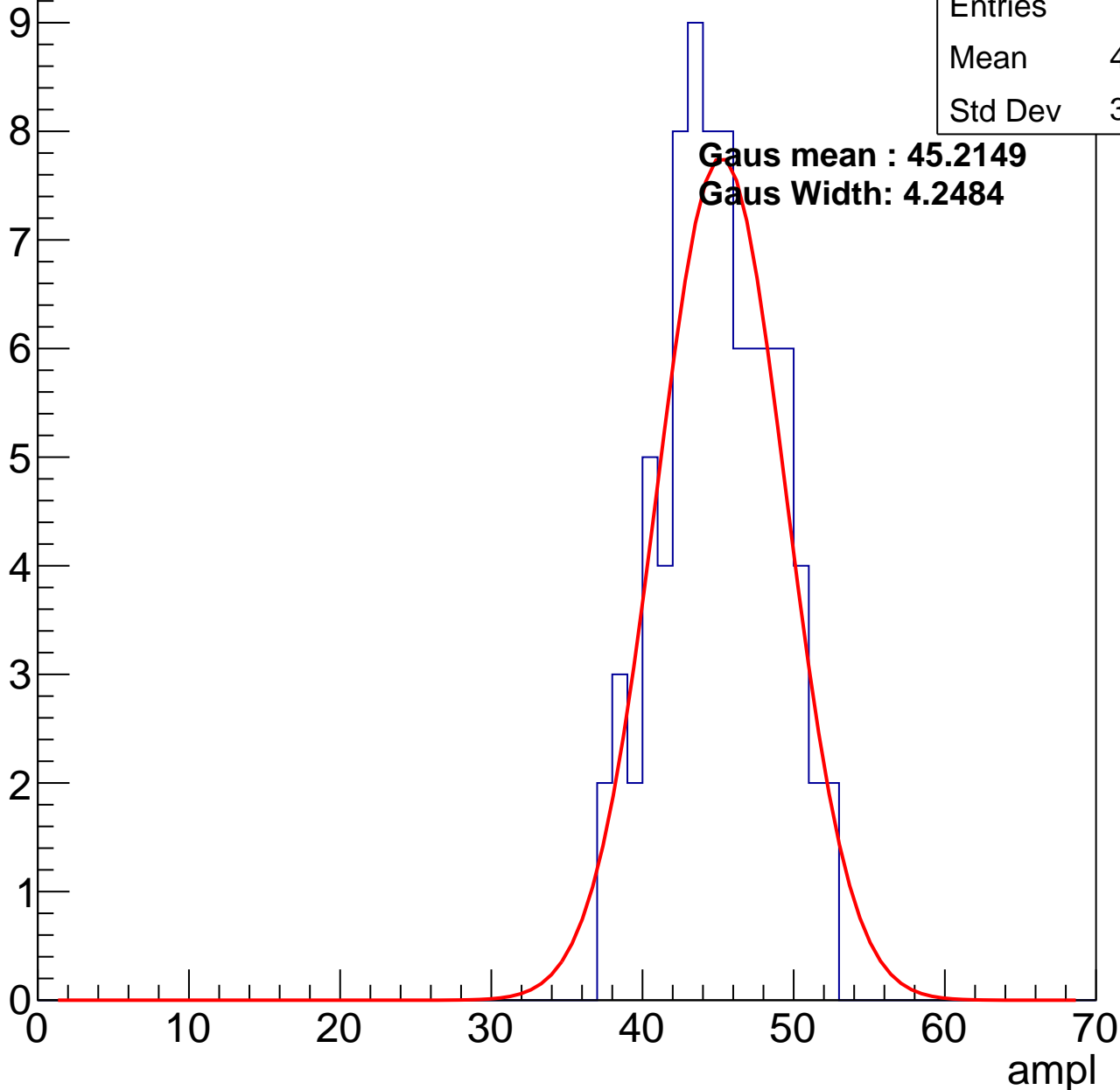
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	81
Mean	44.58
Std Dev	3.665

**Gaus mean : 45.2149**

**Gaus Width: 4.2484**

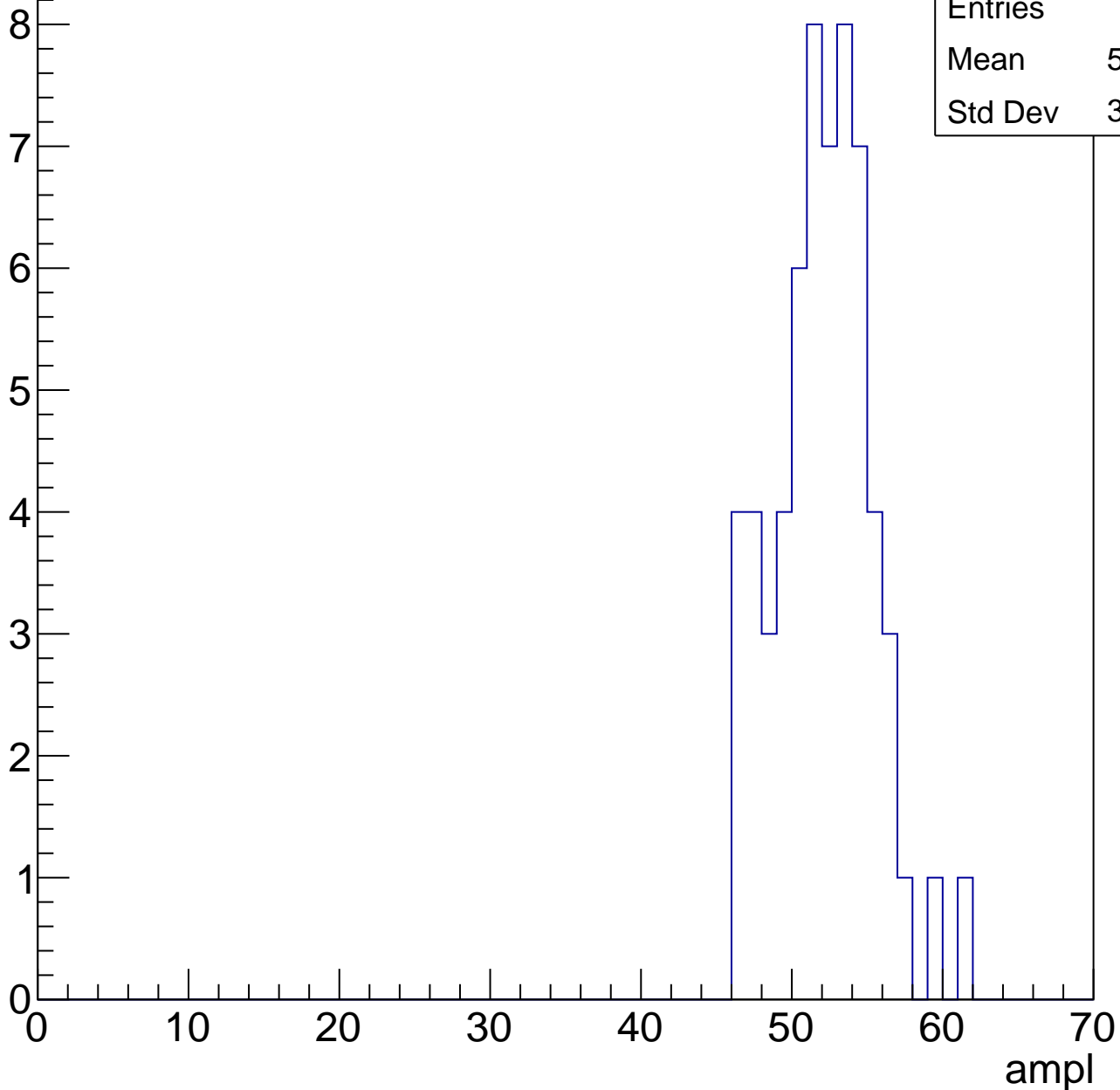


# B0L001S, U5-ch36, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	51.66
Std Dev	3.208

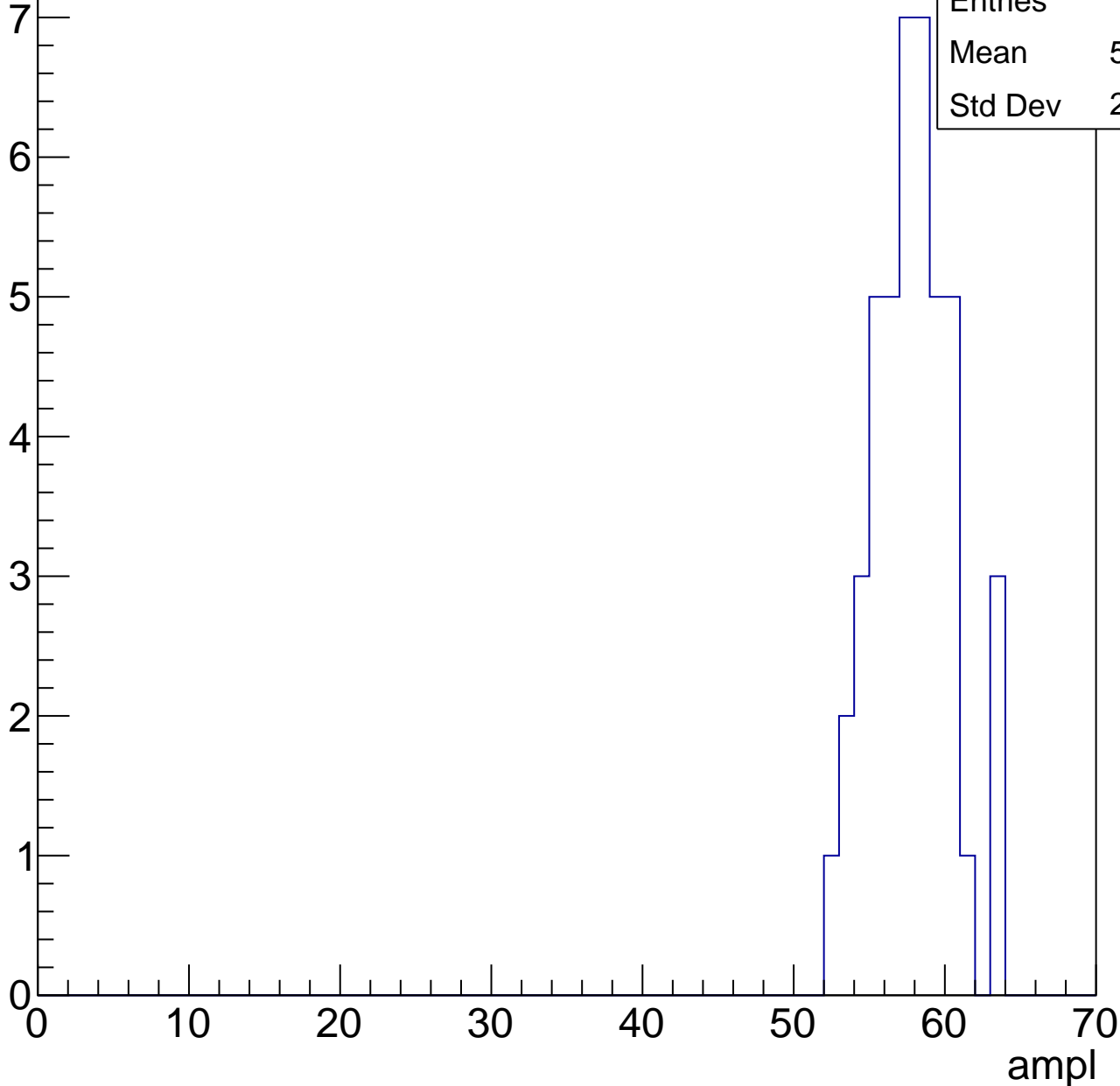


# B0L001S, U5-ch36, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	44
Mean	57.39
Std Dev	2.604

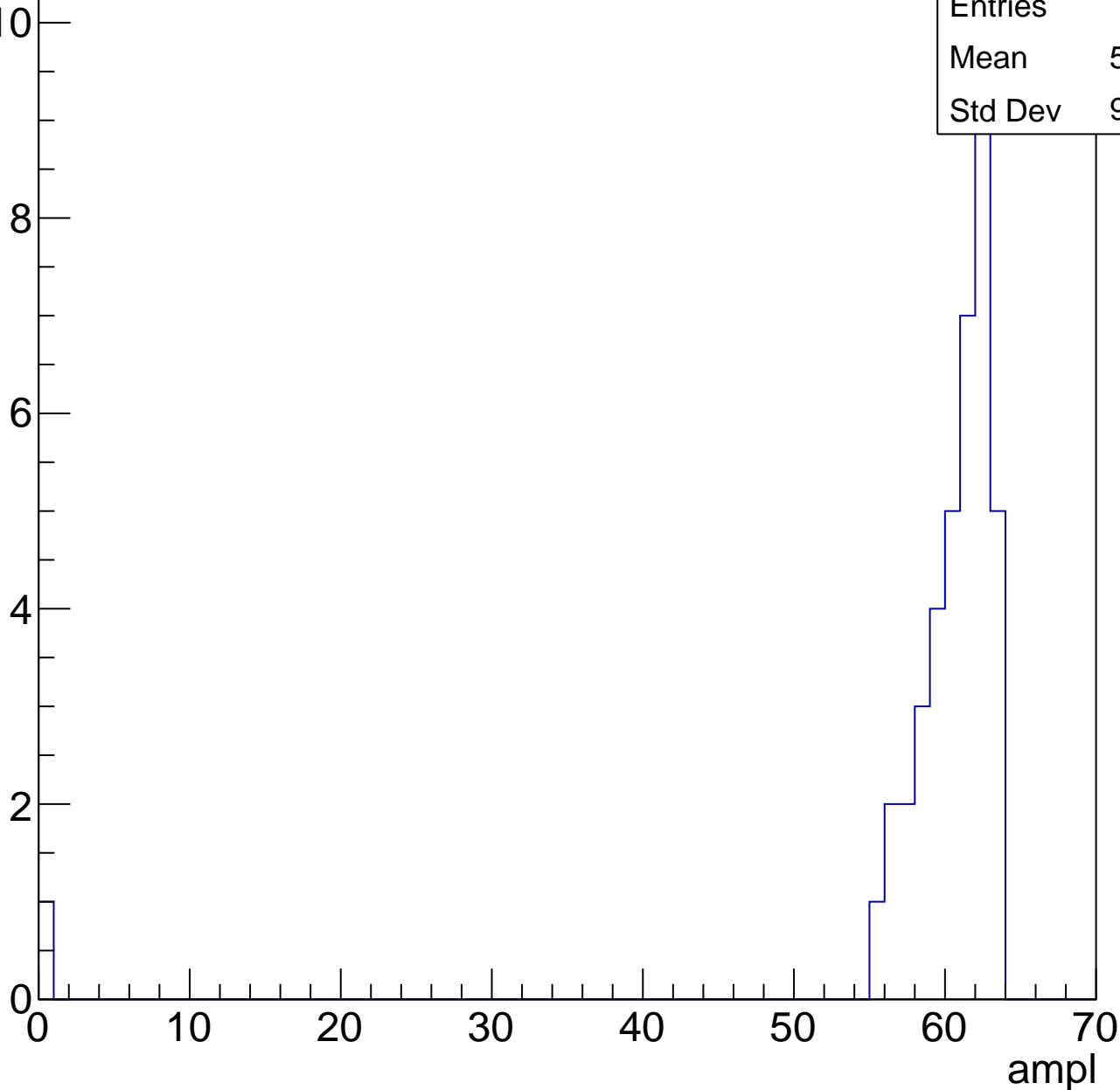


# B0L001S, U5-ch36, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	40
Mean	58.83
Std Dev	9.654



# B0L001S, U5-ch36, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

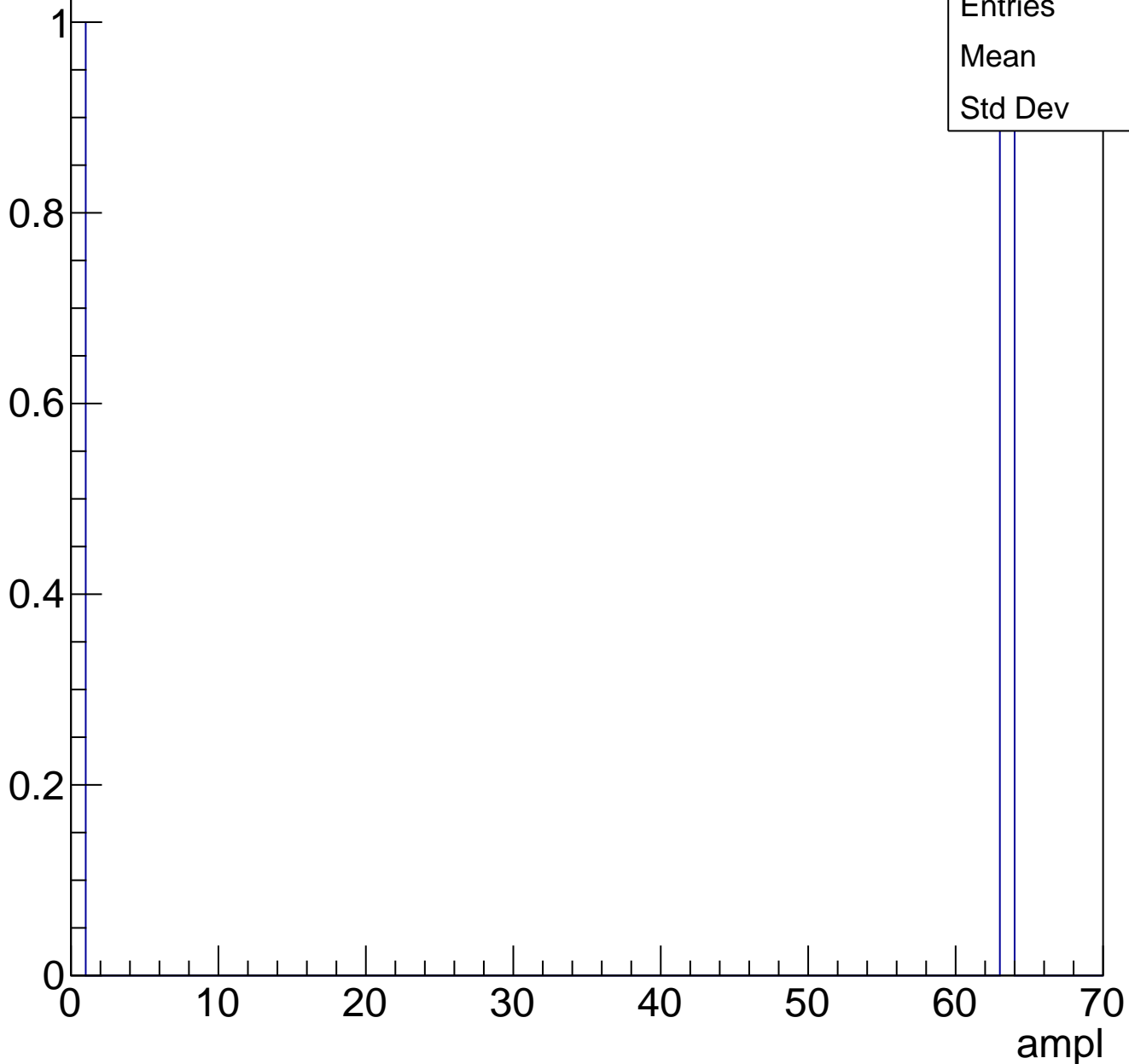




# B0L001S, U5-ch36, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch37, adc0

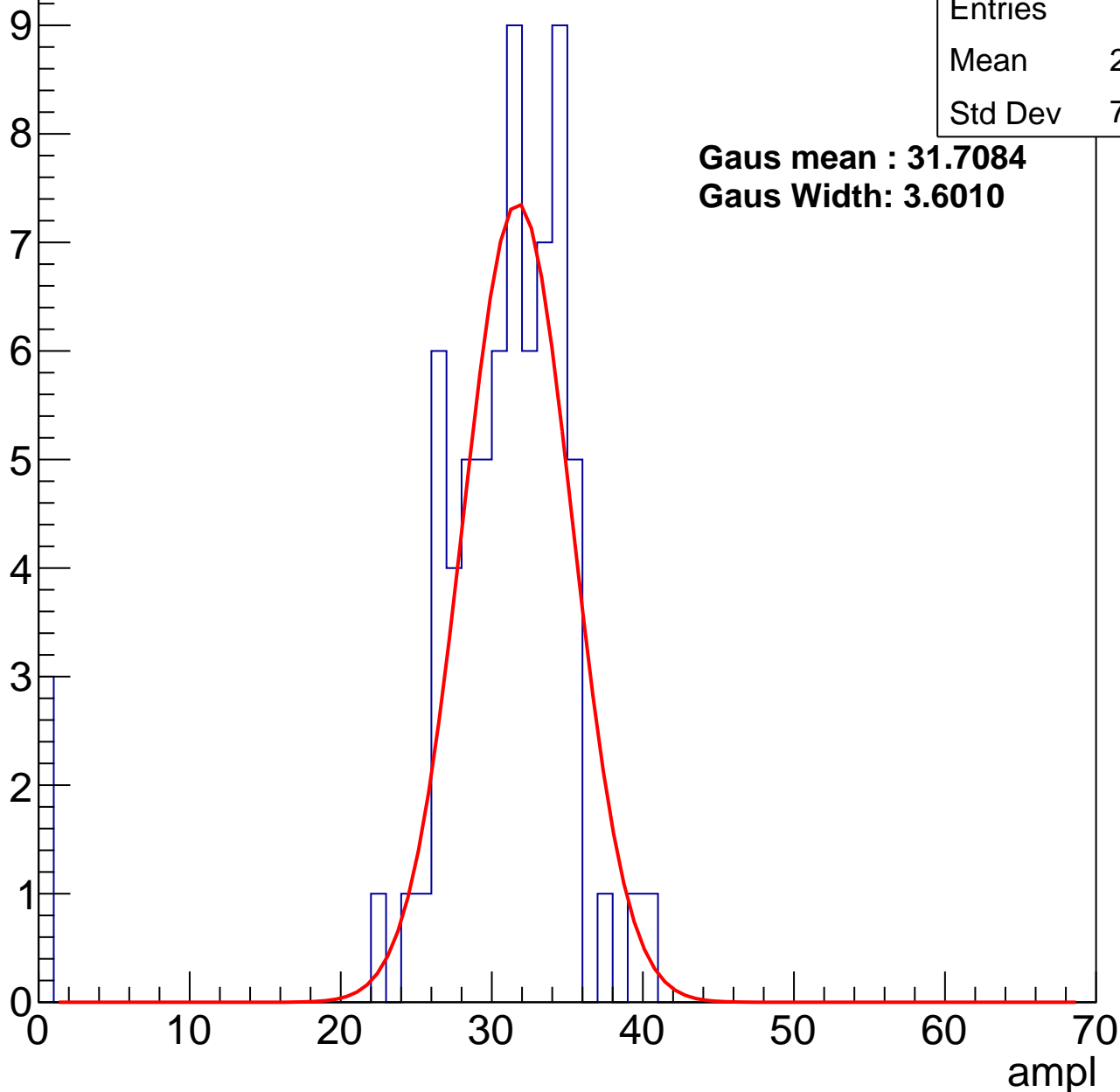
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	29.56
Std Dev	7.084

**Gaus mean : 31.7084**

**Gaus Width: 3.6010**



# B0L001S, U5-ch37, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	61
Mean	37.72
Std Dev	3.219

**Gaus mean : 38.5259**

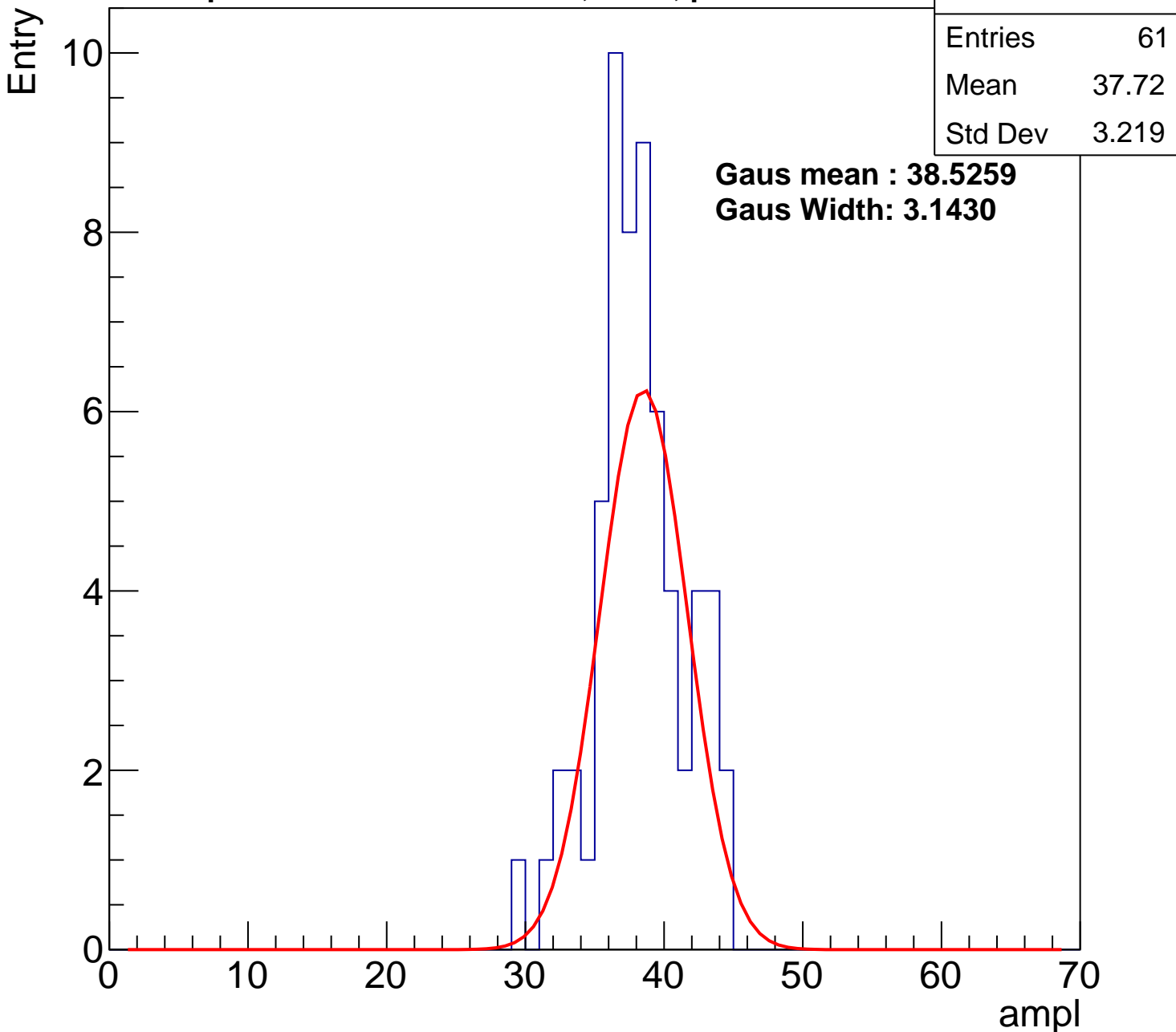
**Gaus Width: 3.1430**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U5-ch37, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	80
Mean	44.74
Std Dev	3.622

**Gaus mean : 45.2333**

**Gaus Width: 3.8804**

Entry

10

8

6

4

2

0

0

10

20

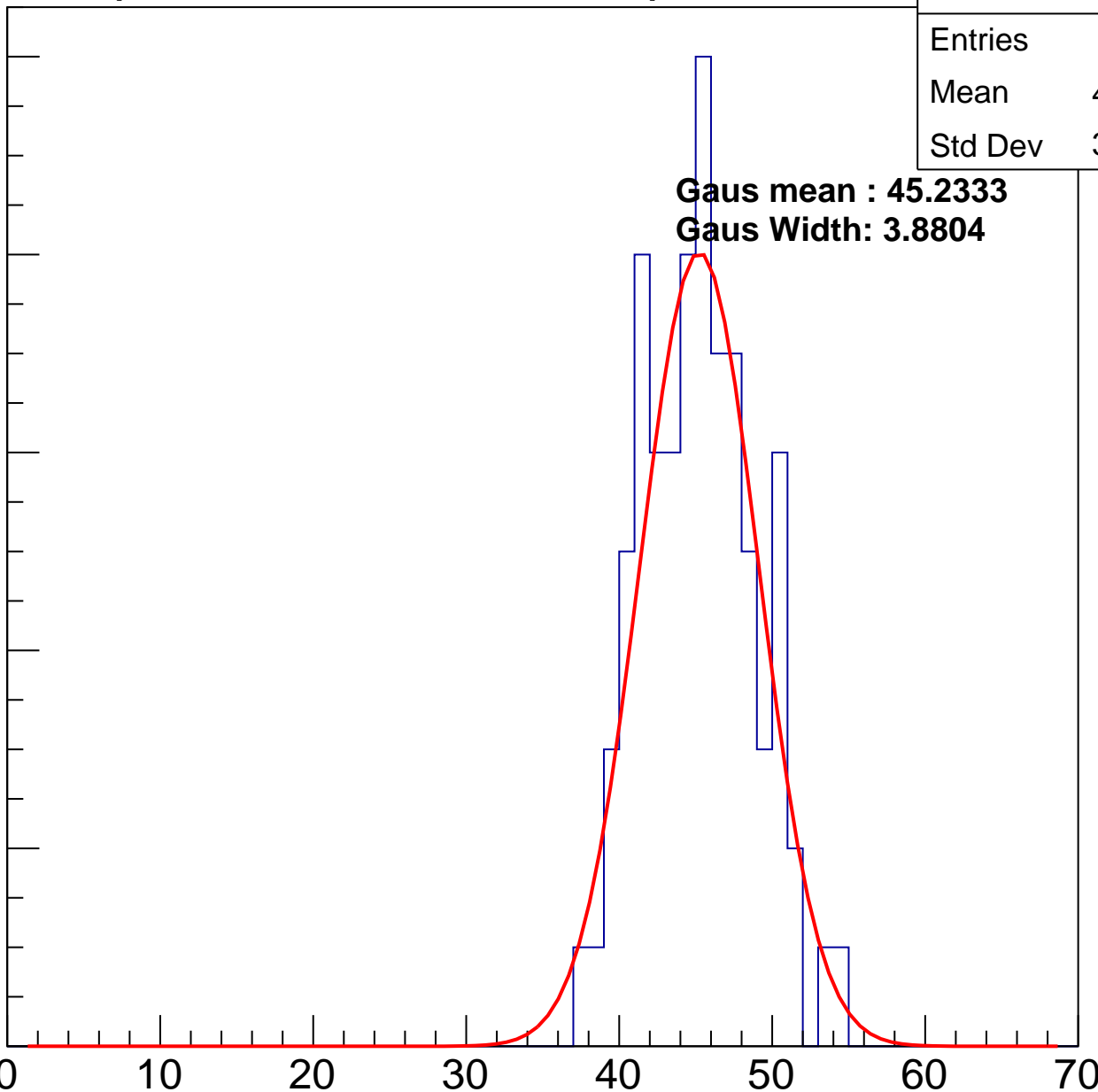
30

40

50

60

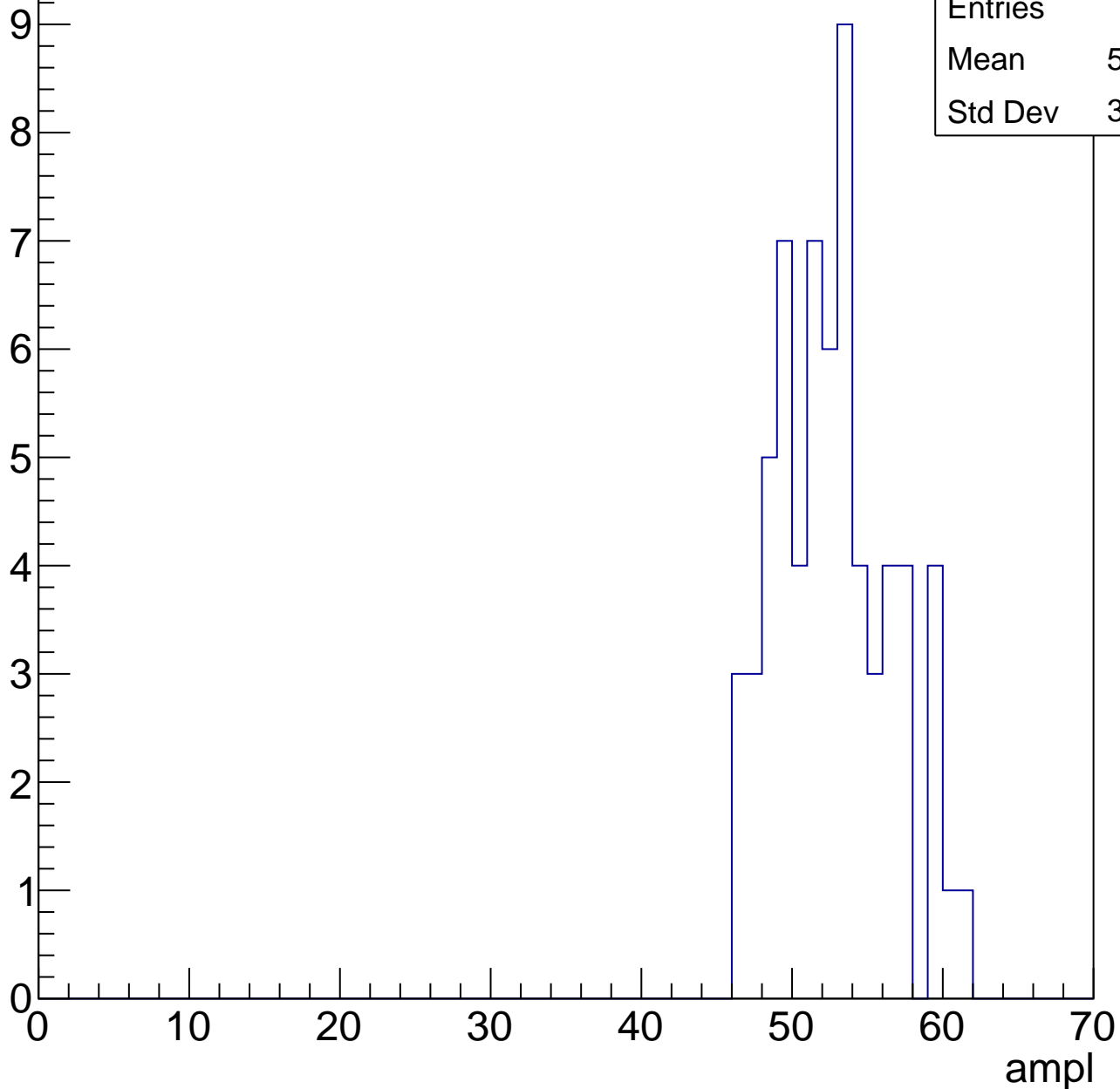
ampl



# B0L001S, U5-ch37, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



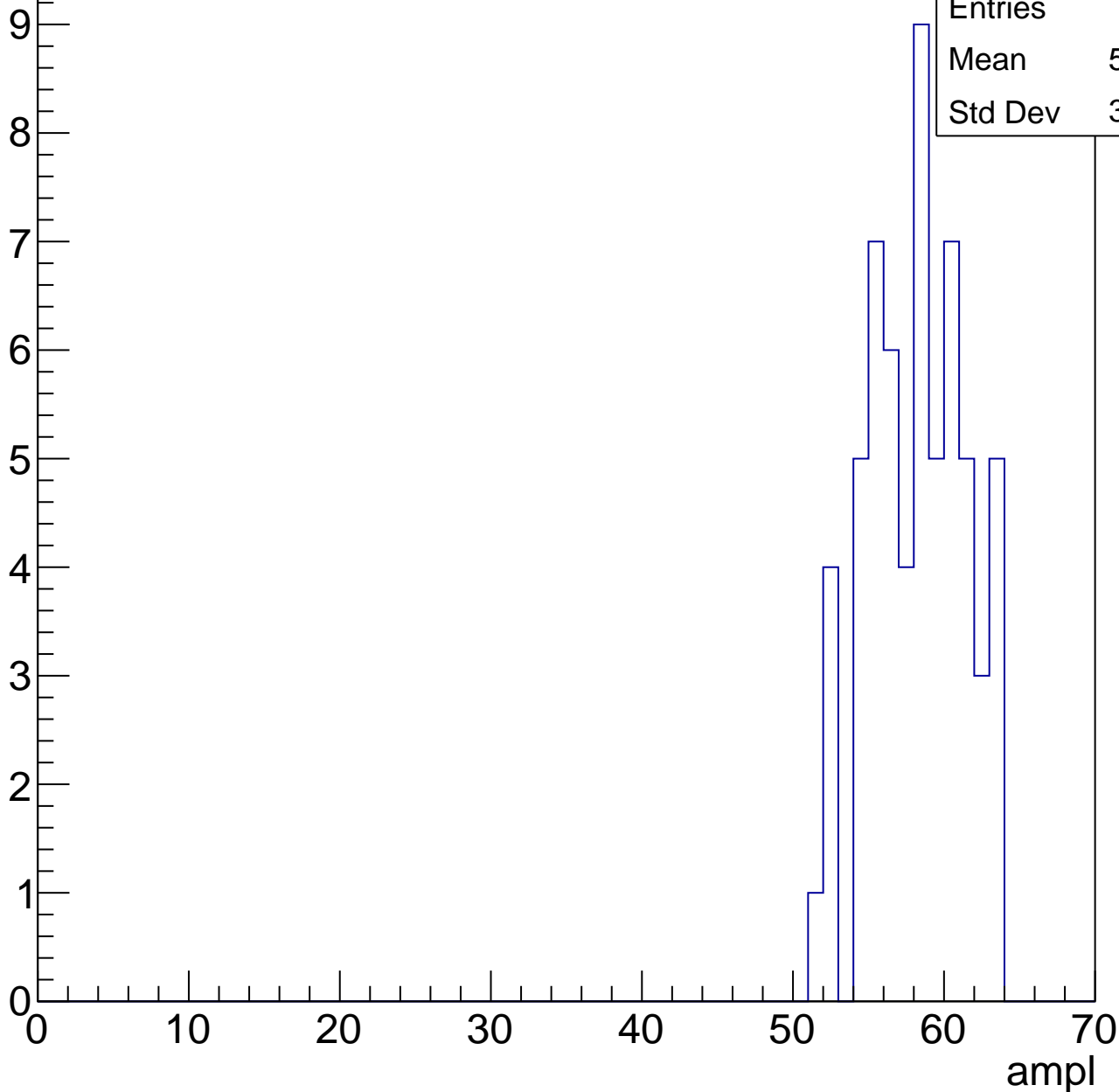
Entries	65
Mean	52.28
Std Dev	3.723

# B0L001S, U5-ch37, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	57.72
Std Dev	3.163

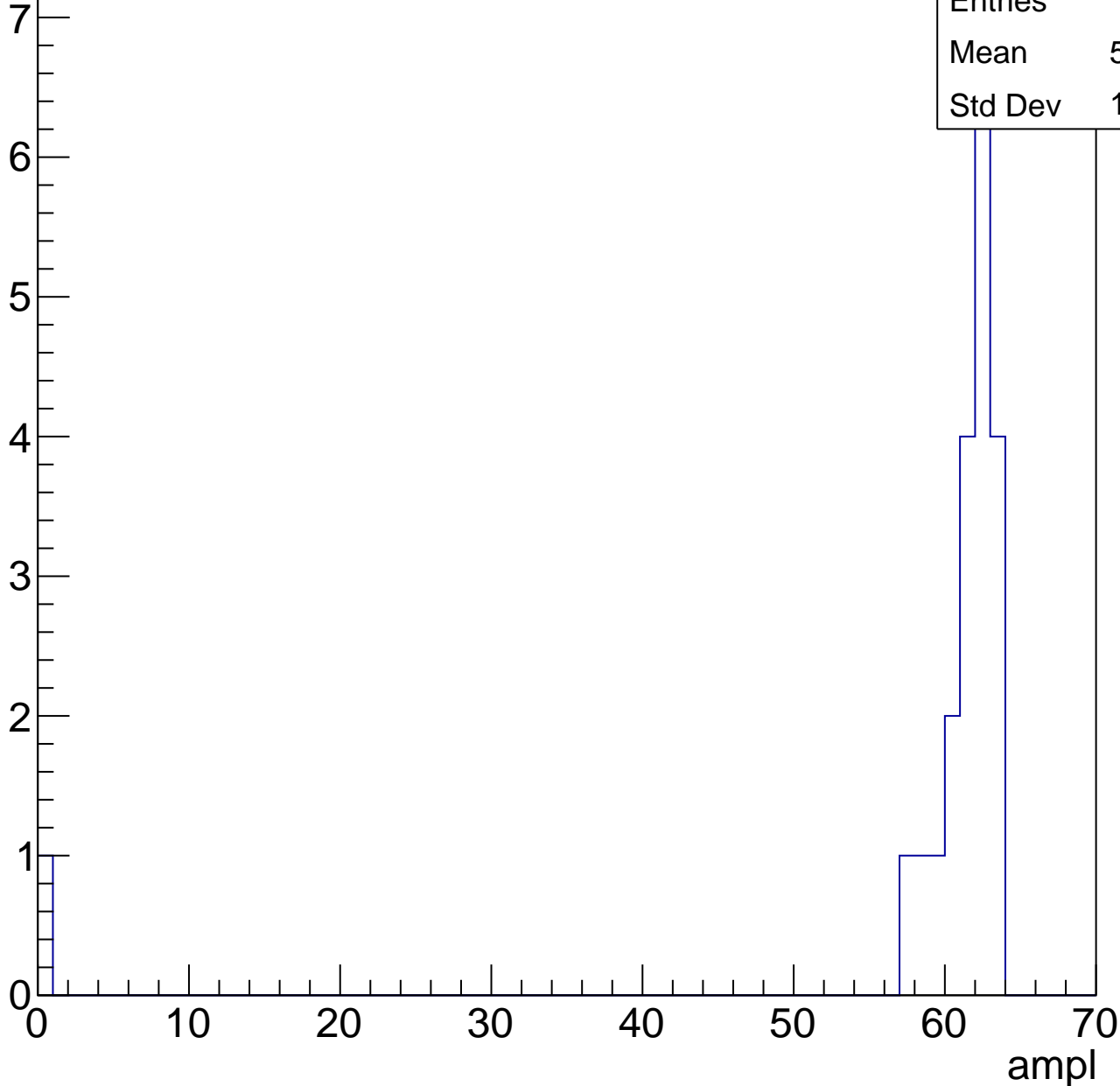


# B0L001S, U5-ch37, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

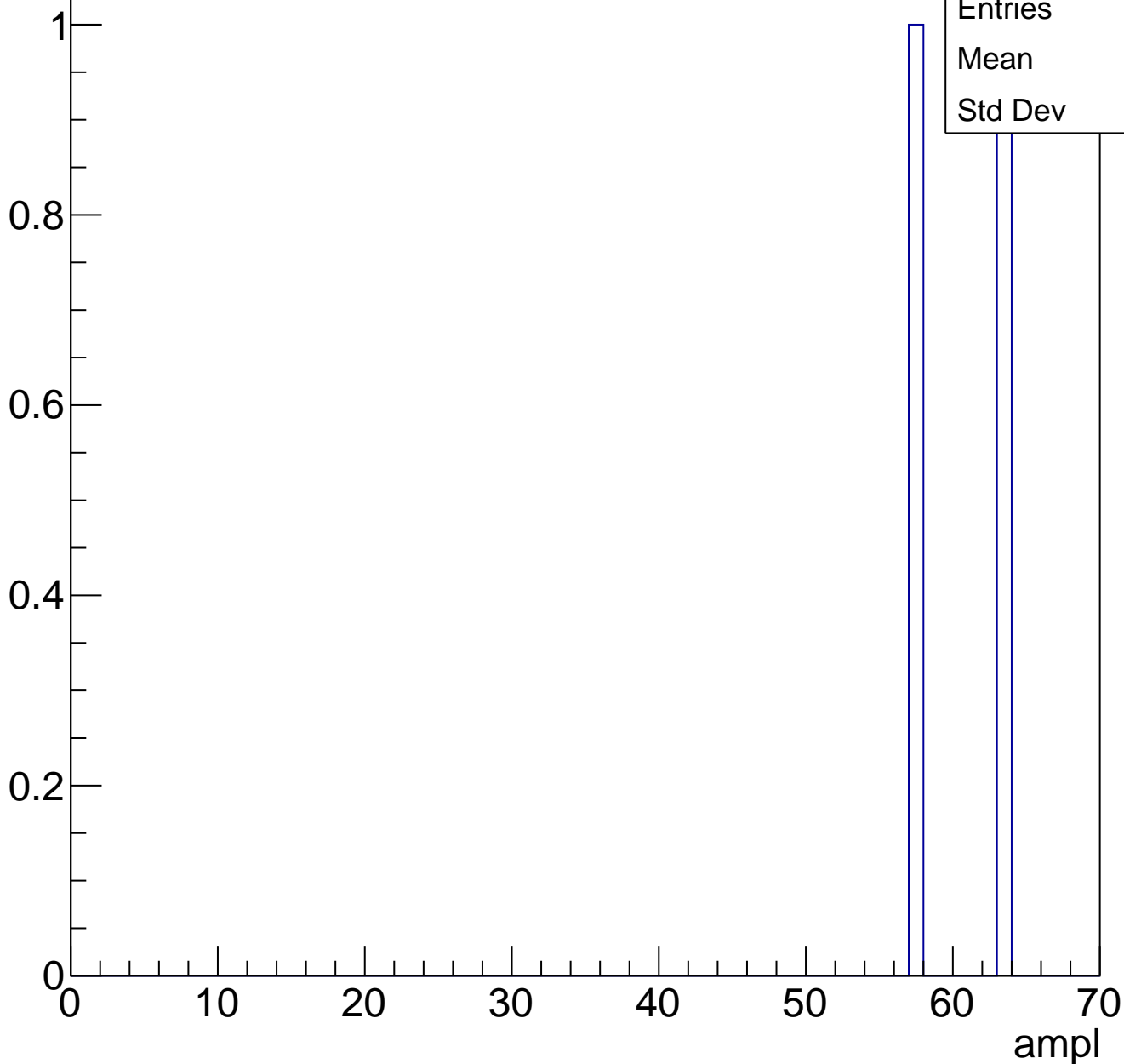
Entries	21
Mean	58.29
Std Dev	13.13



# B0L001S, U5-ch37, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch37, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch38, adc0

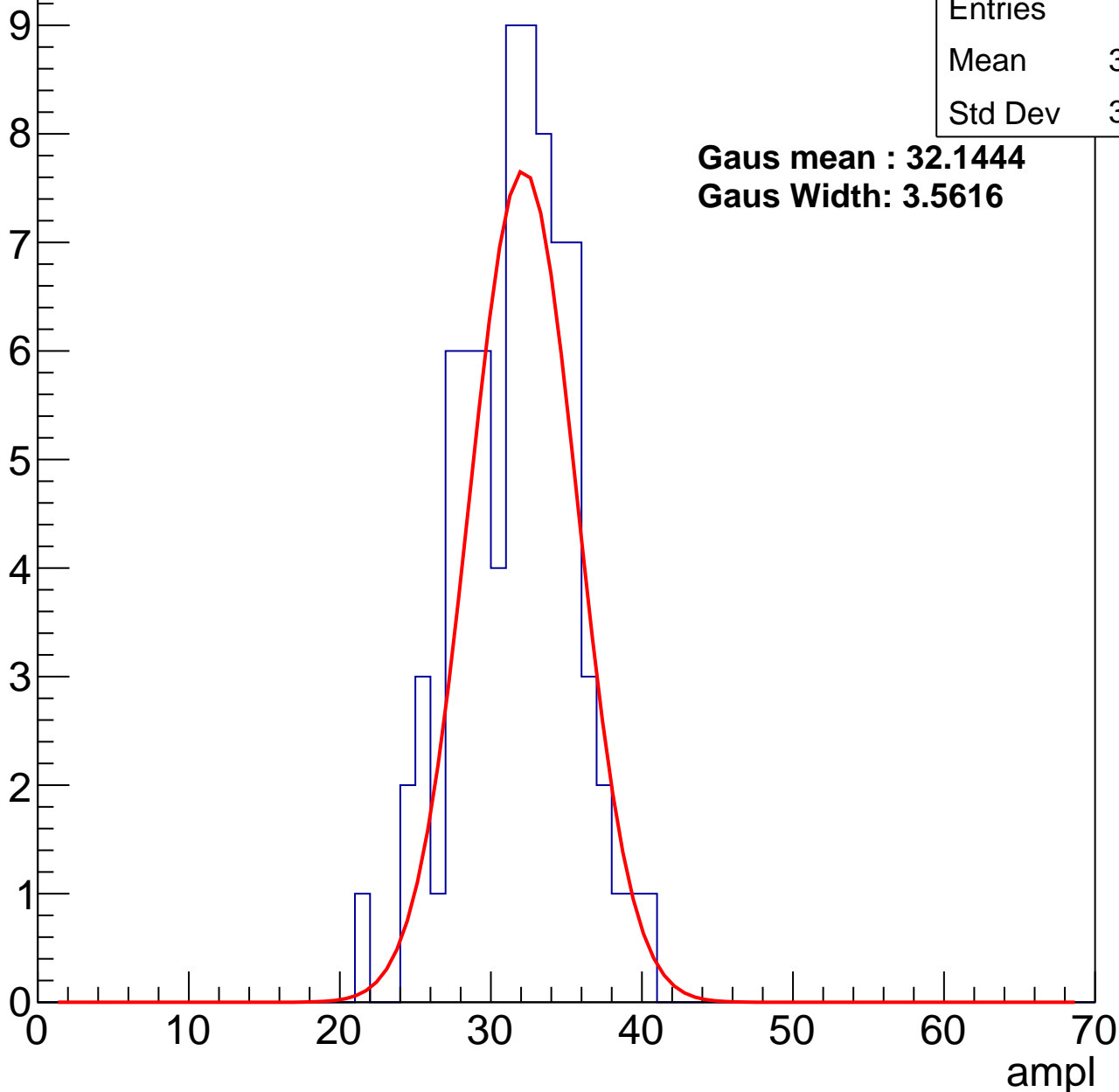
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	77
Mean	31.26
Std Dev	3.712

**Gaus mean : 32.1444**

**Gaus Width: 3.5616**



# B0L001S, U5-ch38, adc1

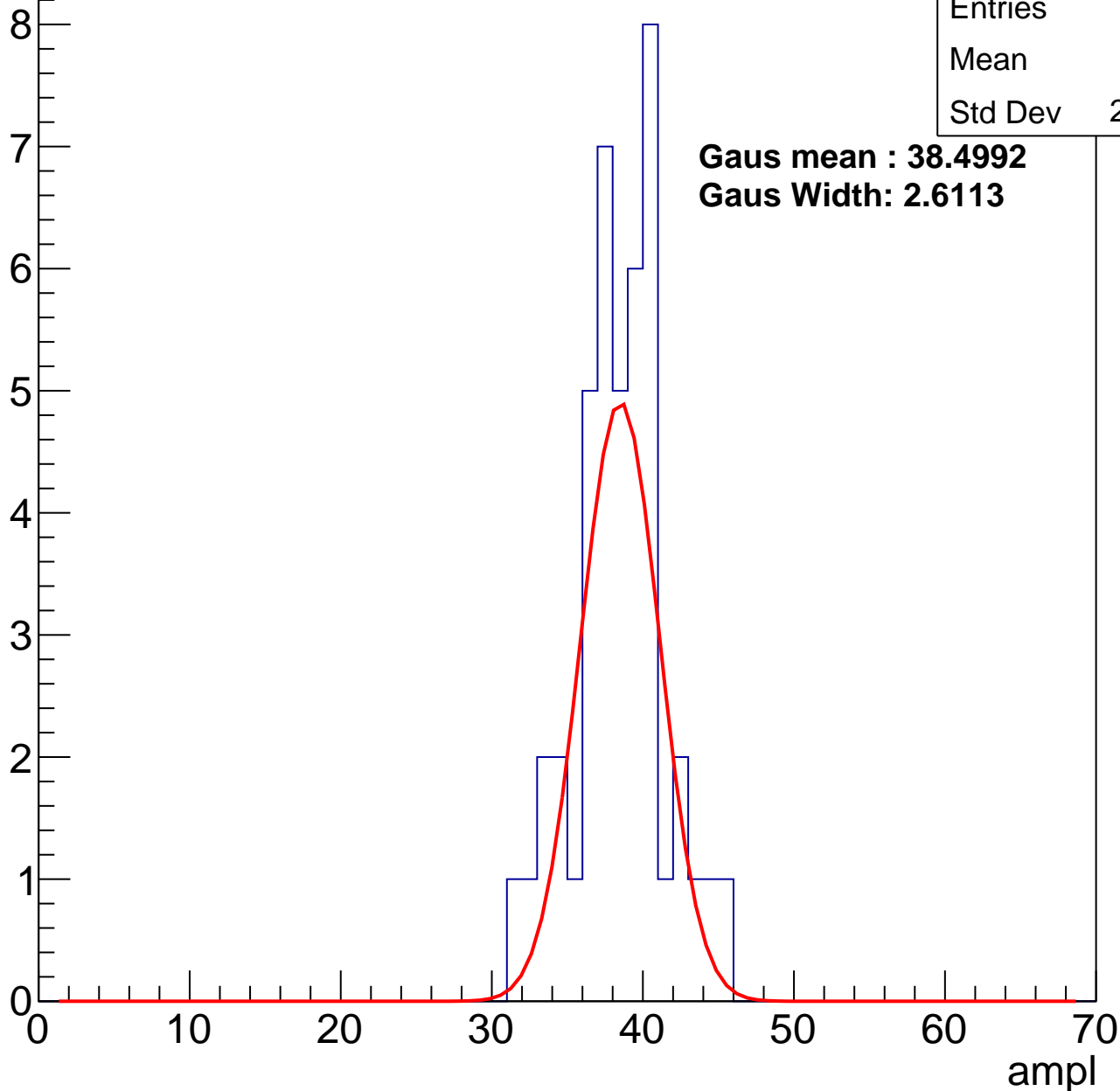
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	44
Mean	38
Std Dev	2.985

**Gaus mean : 38.4992**

**Gaus Width: 2.6113**



# B0L001S, U5-ch38, adc2

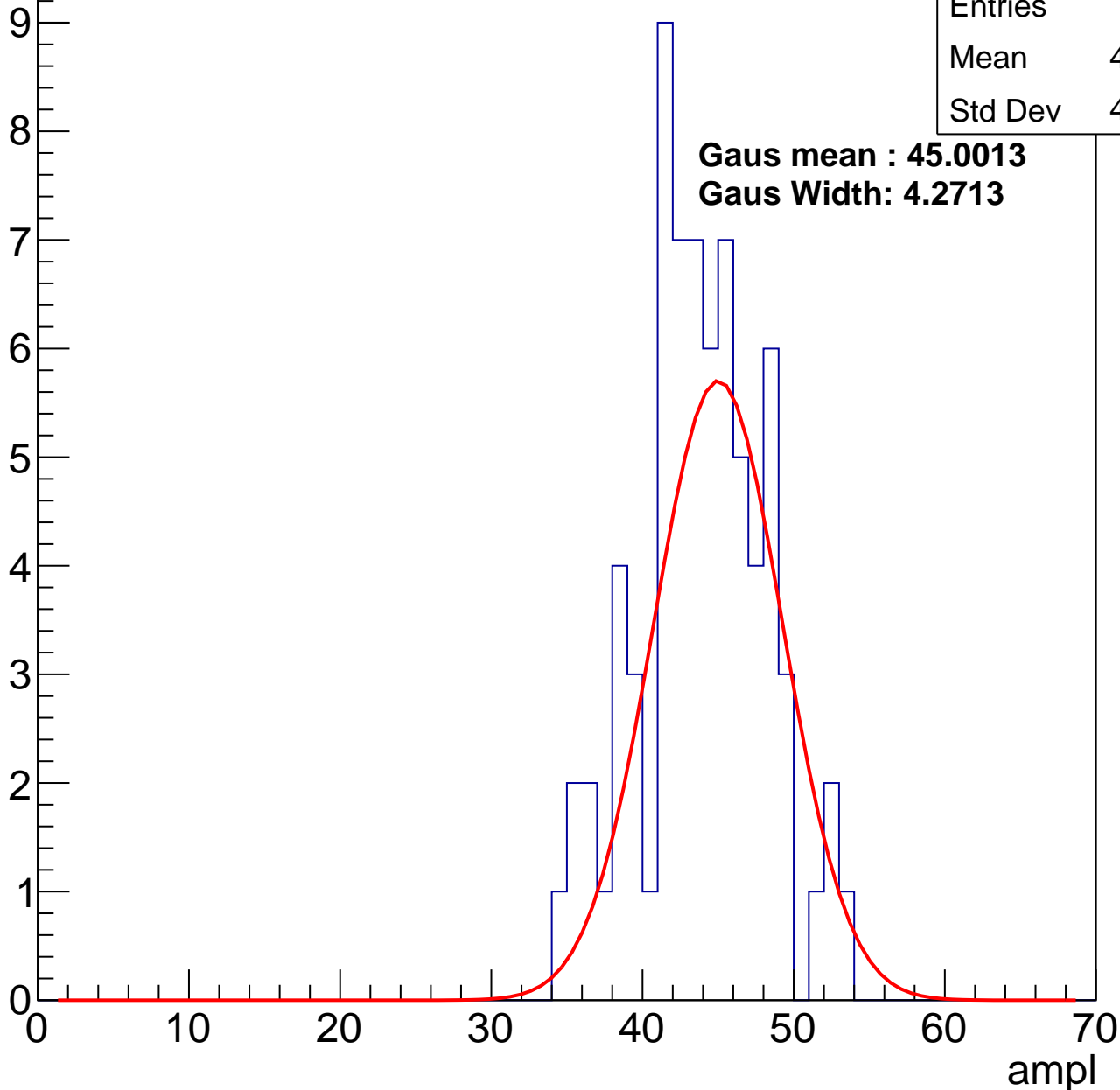
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	43.42
Std Dev	4.179

**Gaus mean : 45.0013**

**Gaus Width: 4.2713**

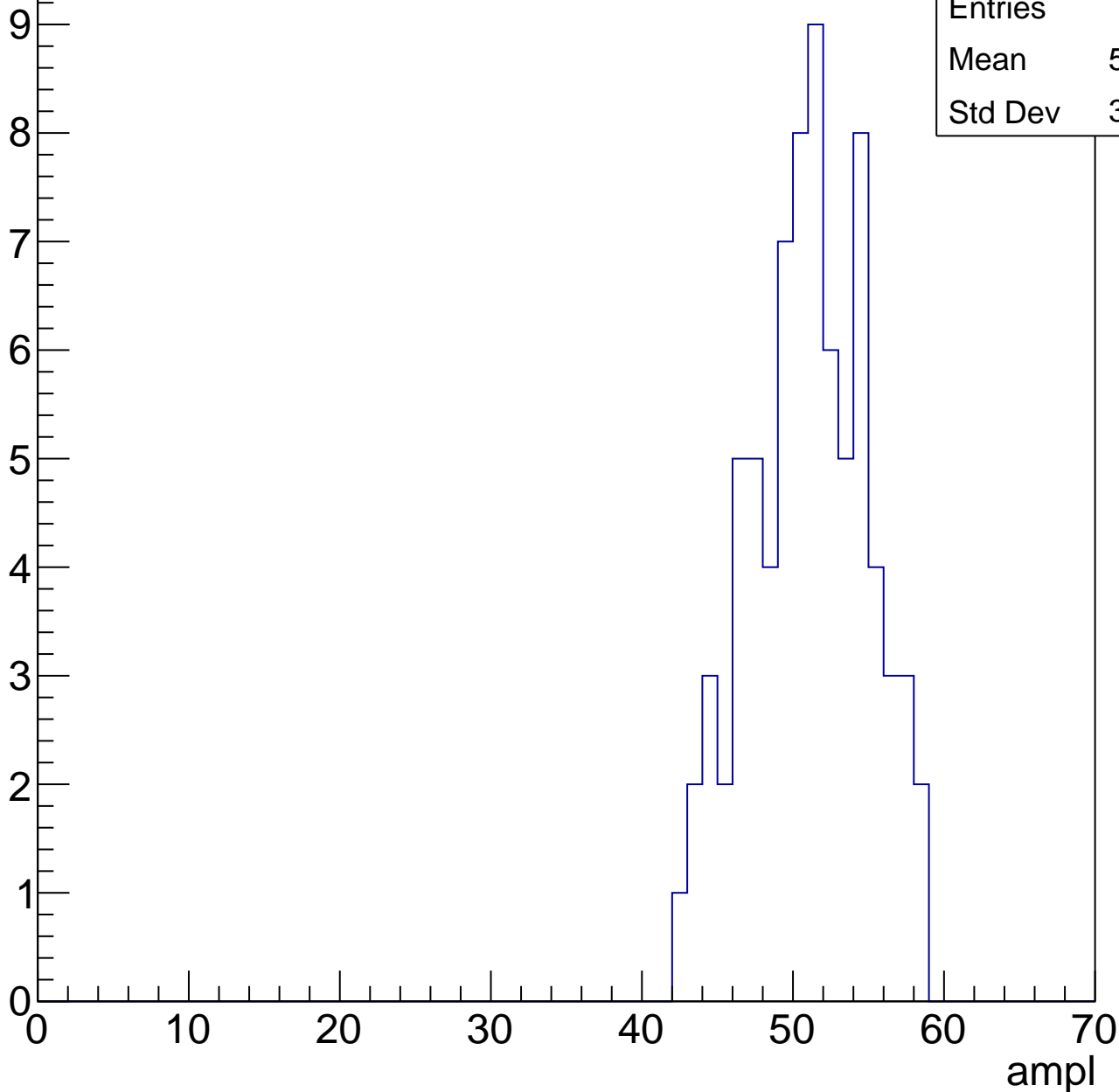


# B0L001S, U5-ch38, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	77
Mean	50.56
Std Dev	3.836

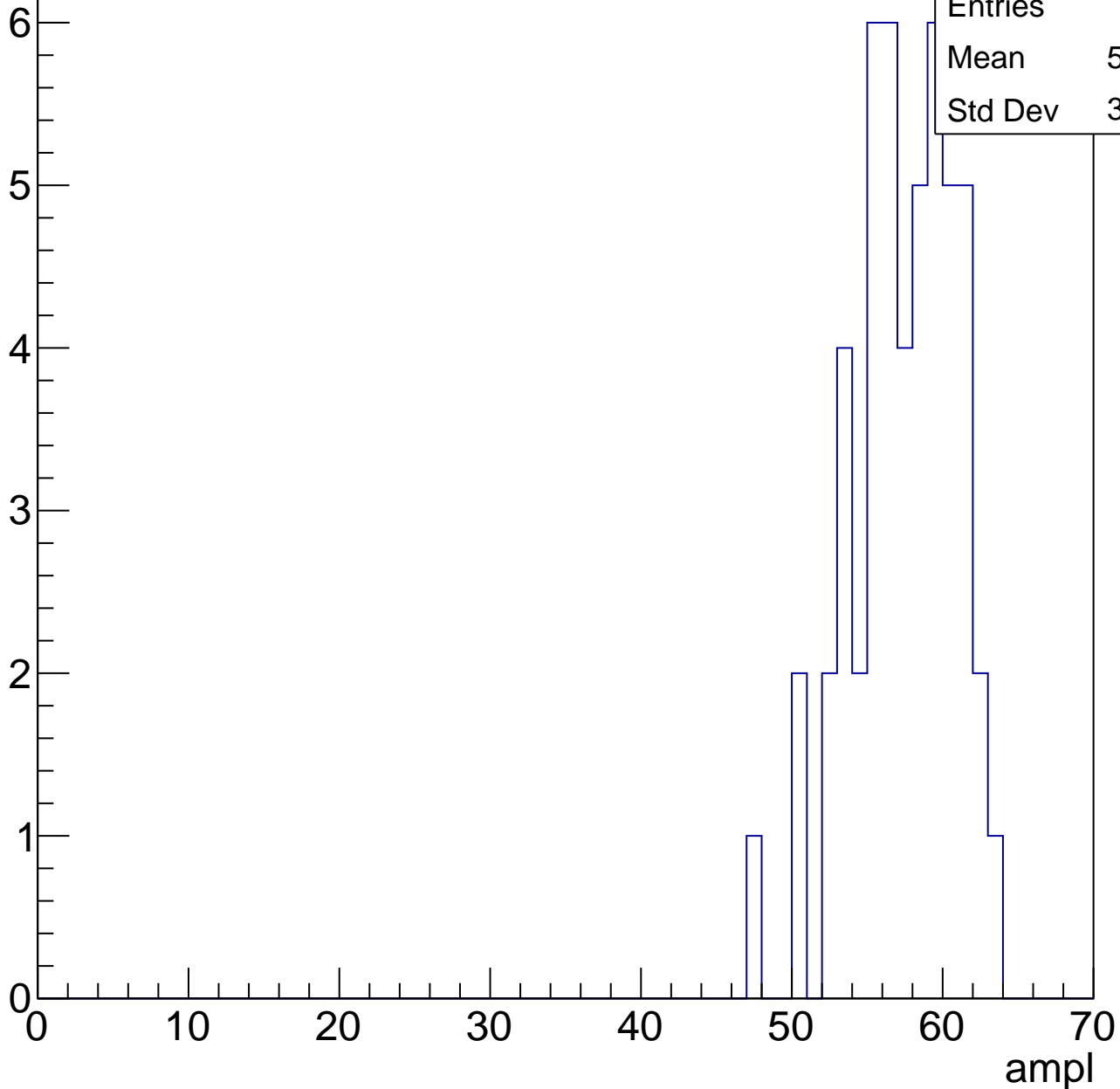


# B0L001S, U5-ch38, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	51
Mean	56.88
Std Dev	3.428

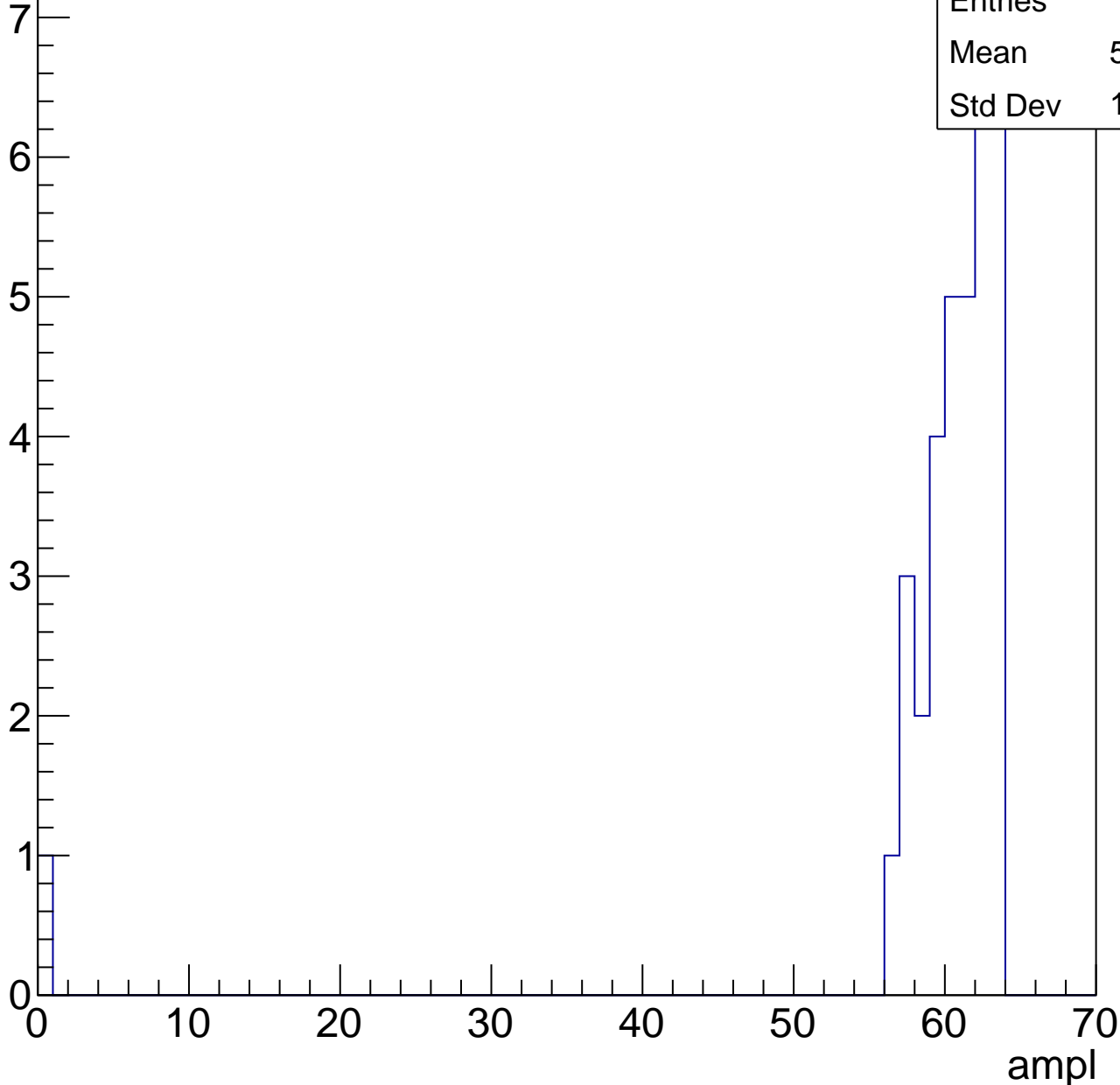


# B0L001S, U5-ch38, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	35
Mean	58.83
Std Dev	10.29



# B0L001S, U5-ch38, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch38, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L001S, U5-ch39, adc0

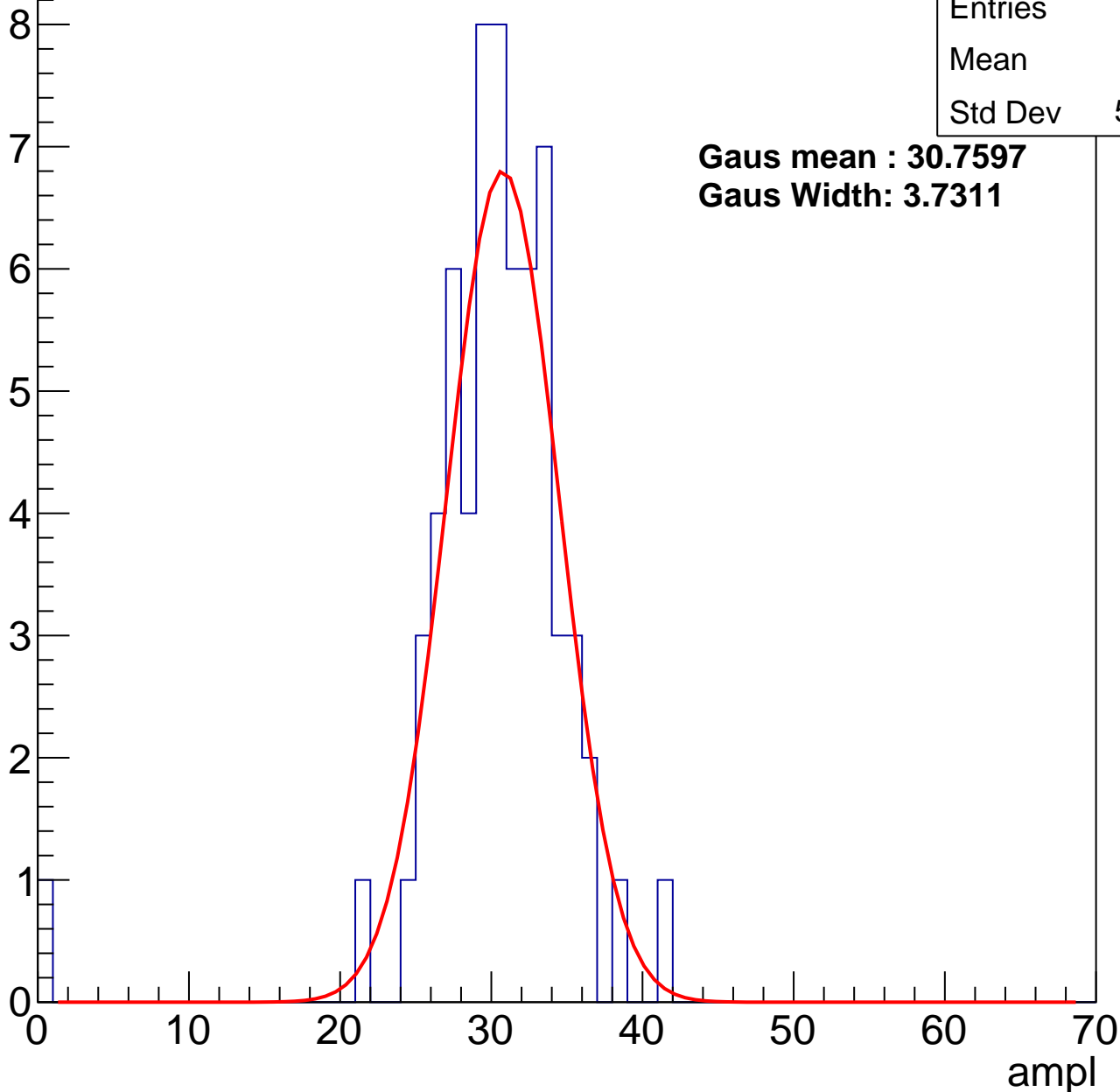
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	29.8
Std Dev	5.121

**Gaus mean : 30.7597**

**Gaus Width: 3.7311**



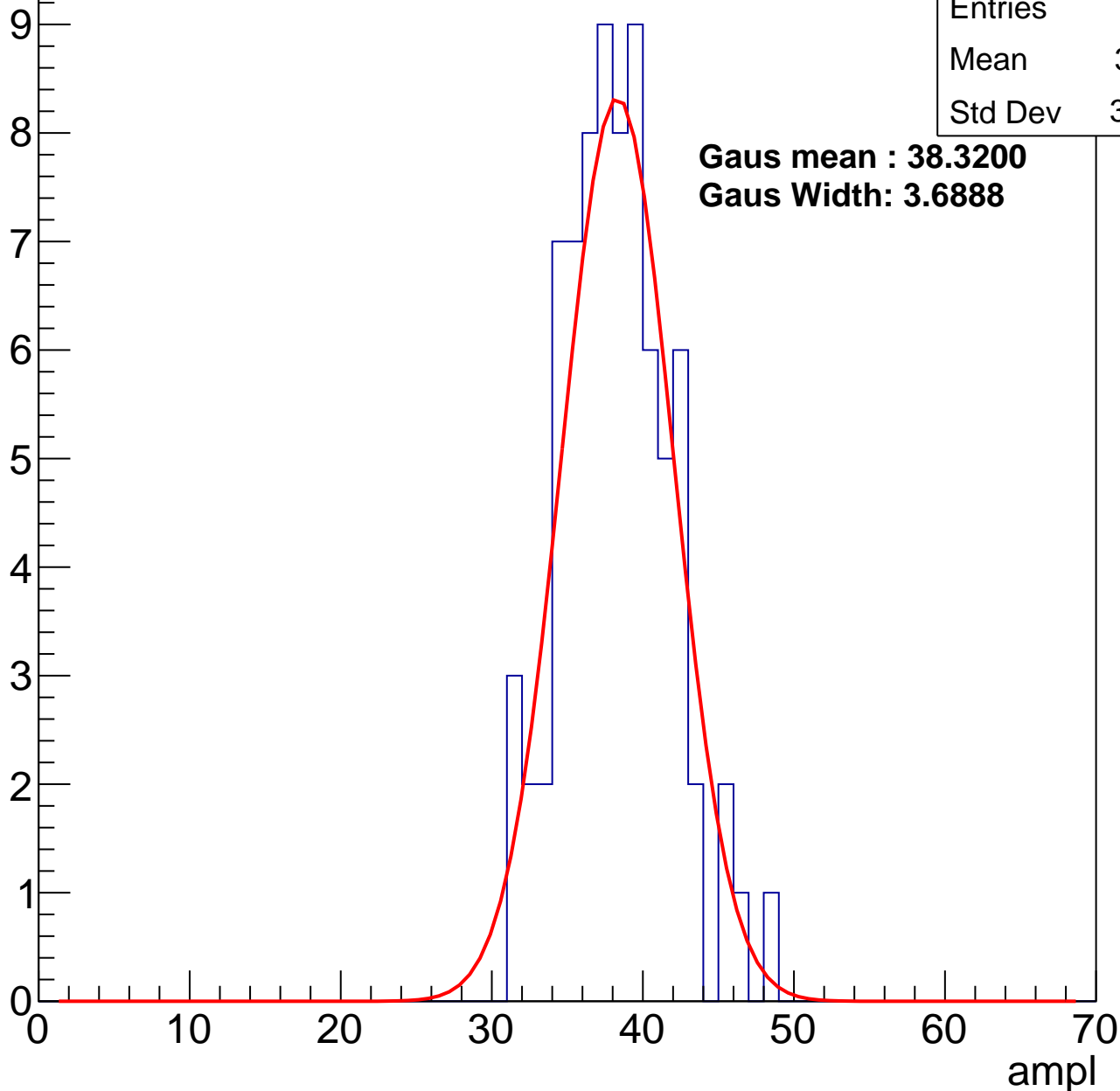
# B0L001S, U5-ch39, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	78
Mean	37.81
Std Dev	3.523

**Gaus mean : 38.3200**  
**Gaus Width: 3.6888**



# B0L001S, U5-ch39, adc2

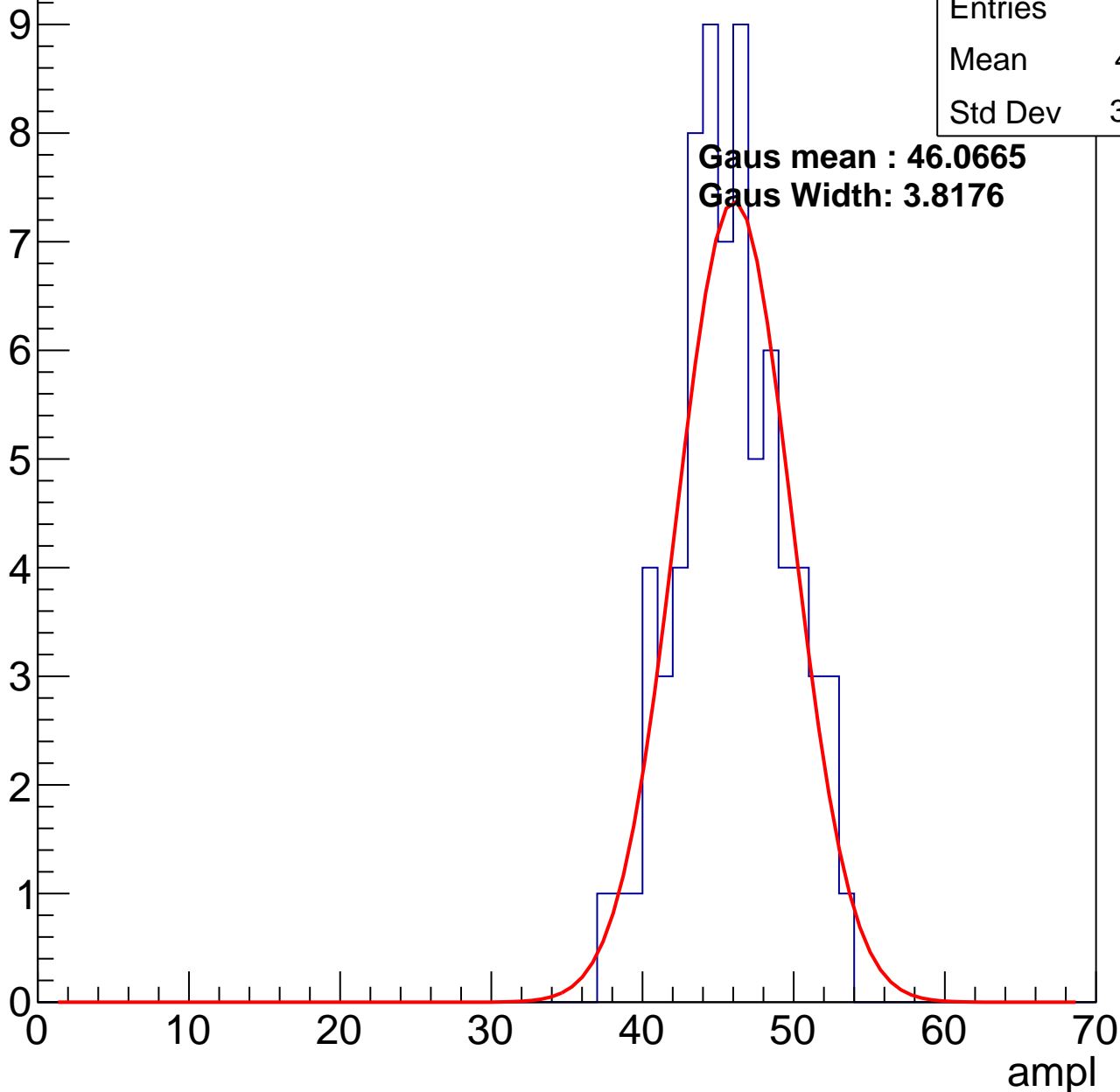
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	45.41
Std Dev	3.565

**Gaus mean : 46.0665**

**Gaus Width: 3.8176**

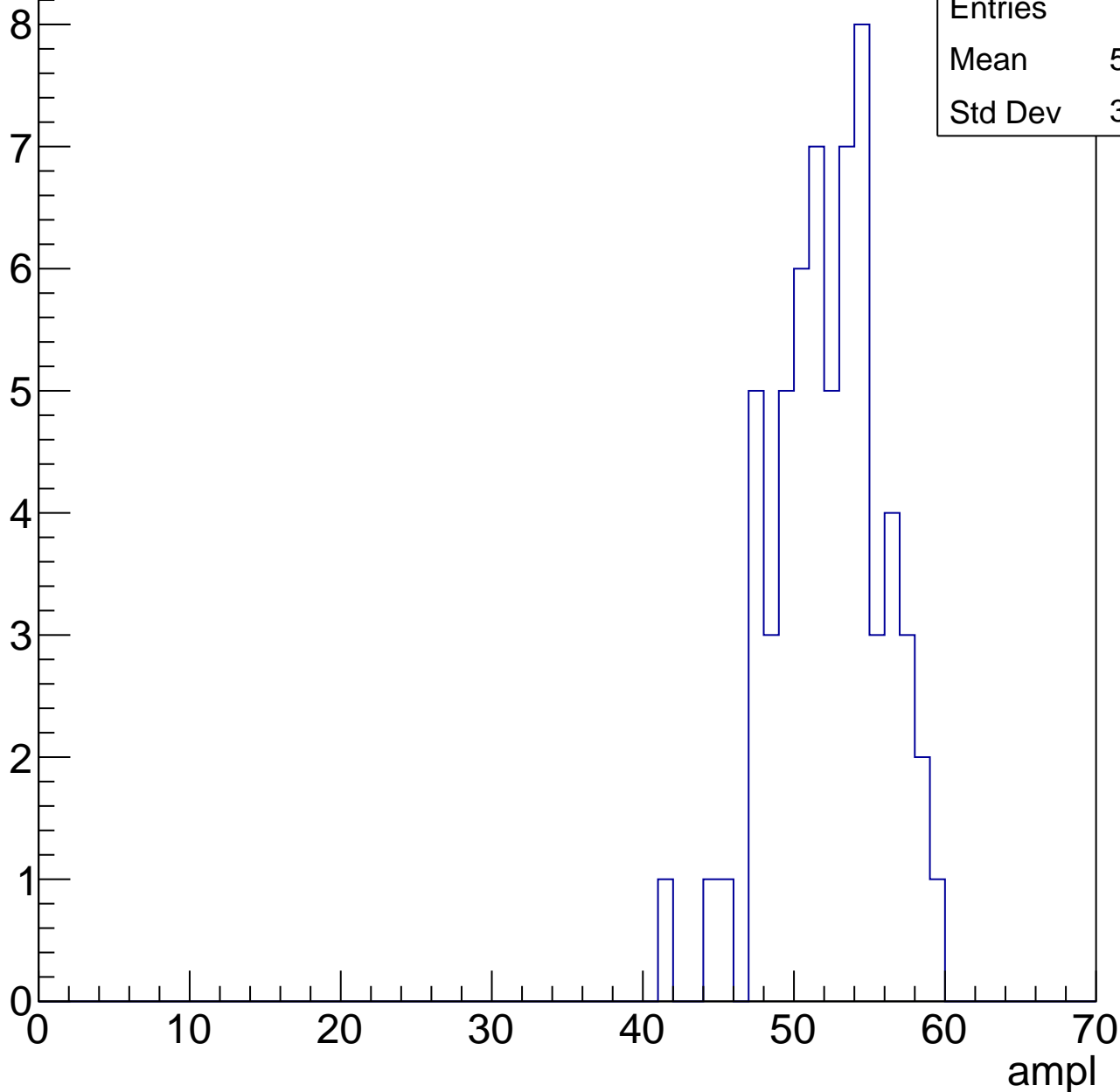


# B0L001S, U5-ch39, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	51.76
Std Dev	3.604



# B0L001S, U5-ch39, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

7

6

5

4

3

2

1

0

Entries 45

Mean 56.96

Std Dev 2.836

0

10

20

30

40

50

60

70

ampl

0

1

2

3

4

5

6

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12

13

14

15

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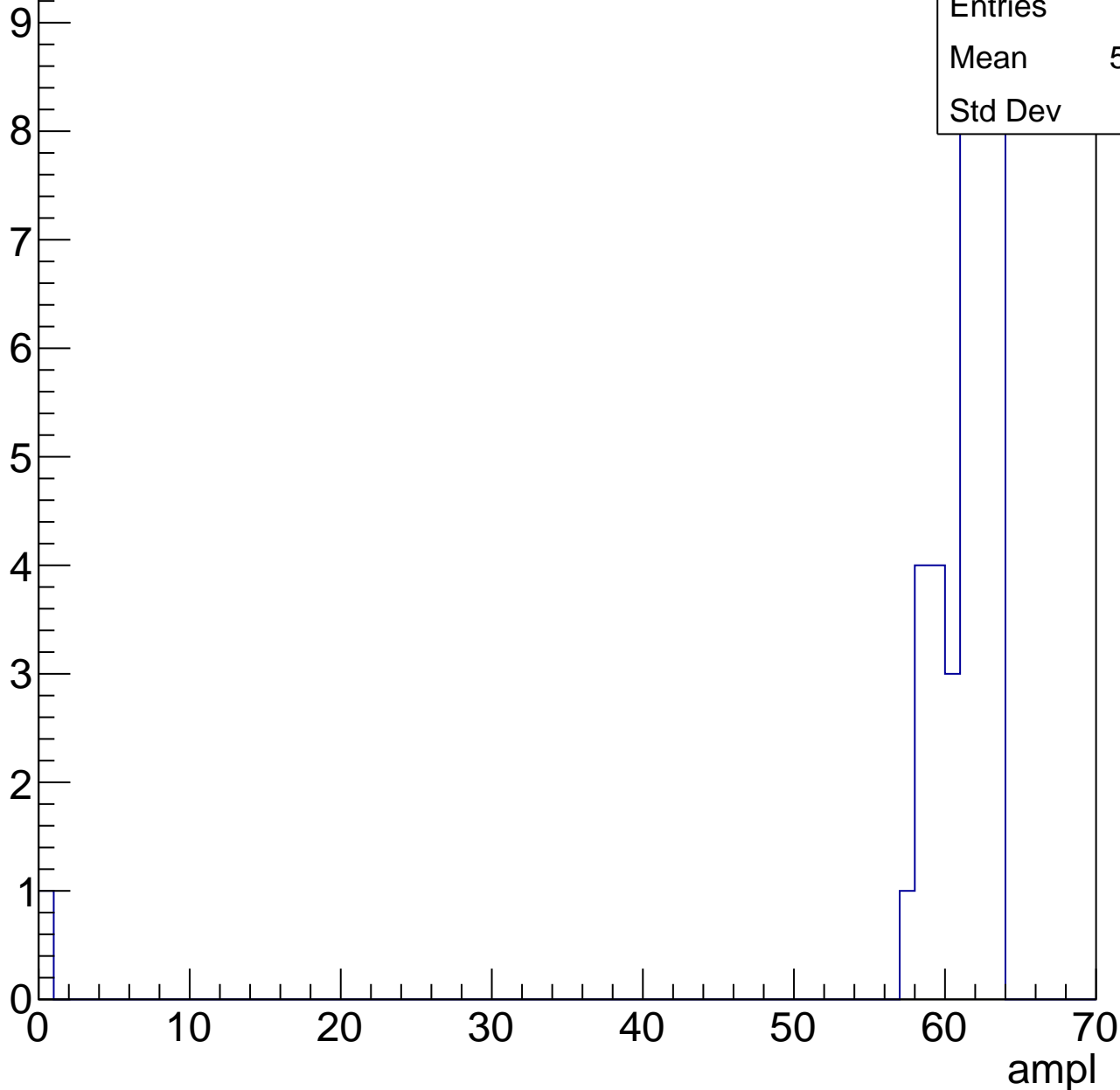
323

# B0L001S, U5-ch39, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	38
Mean	59.32
Std Dev	9.9



# B0L001S, U5-ch39, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch39, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U5-ch40, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	70
Mean	29.13
Std Dev	4.96

**Gaus mean : 30.3955**

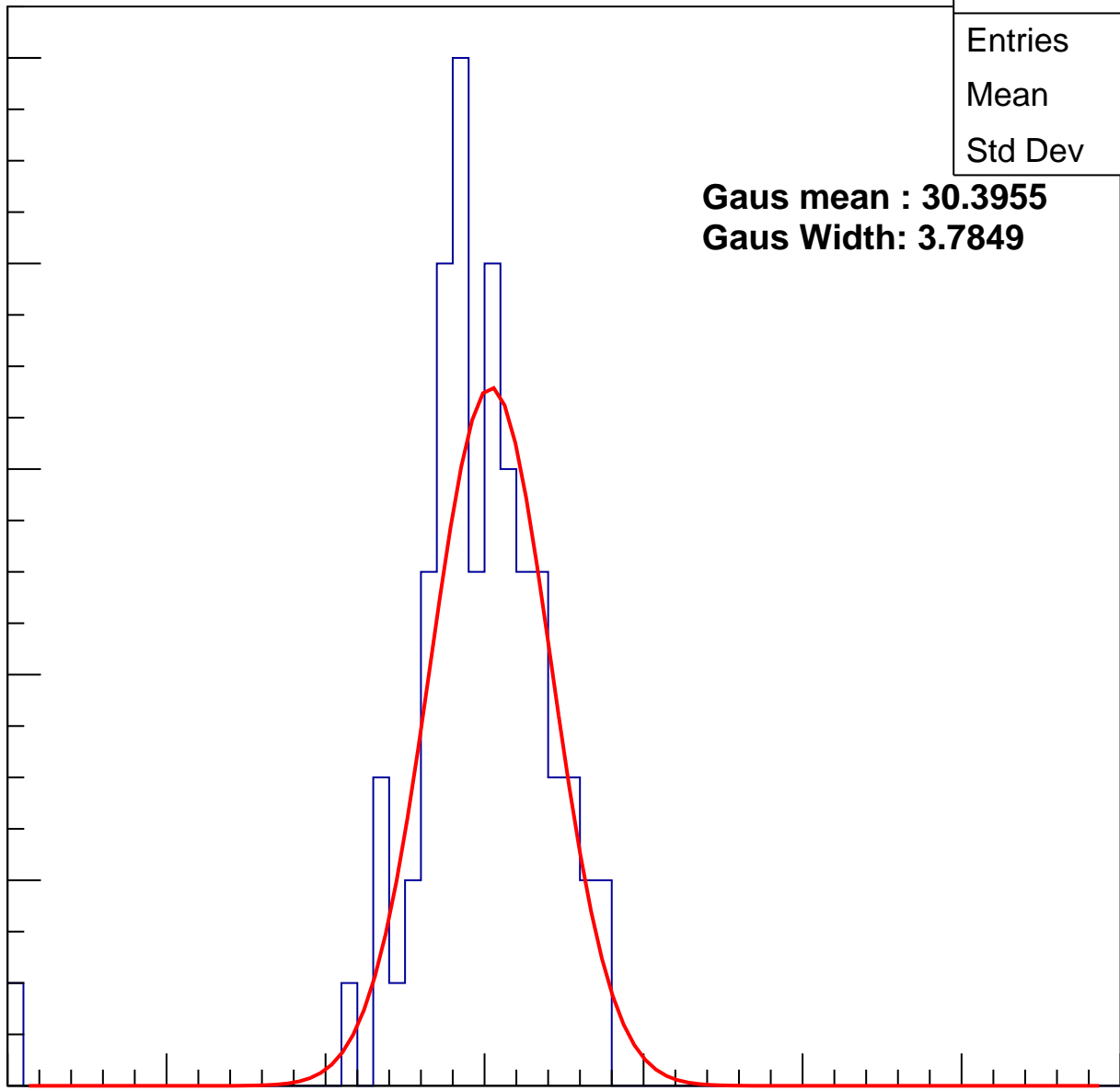
**Gaus Width: 3.7849**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U5-ch40, adc1

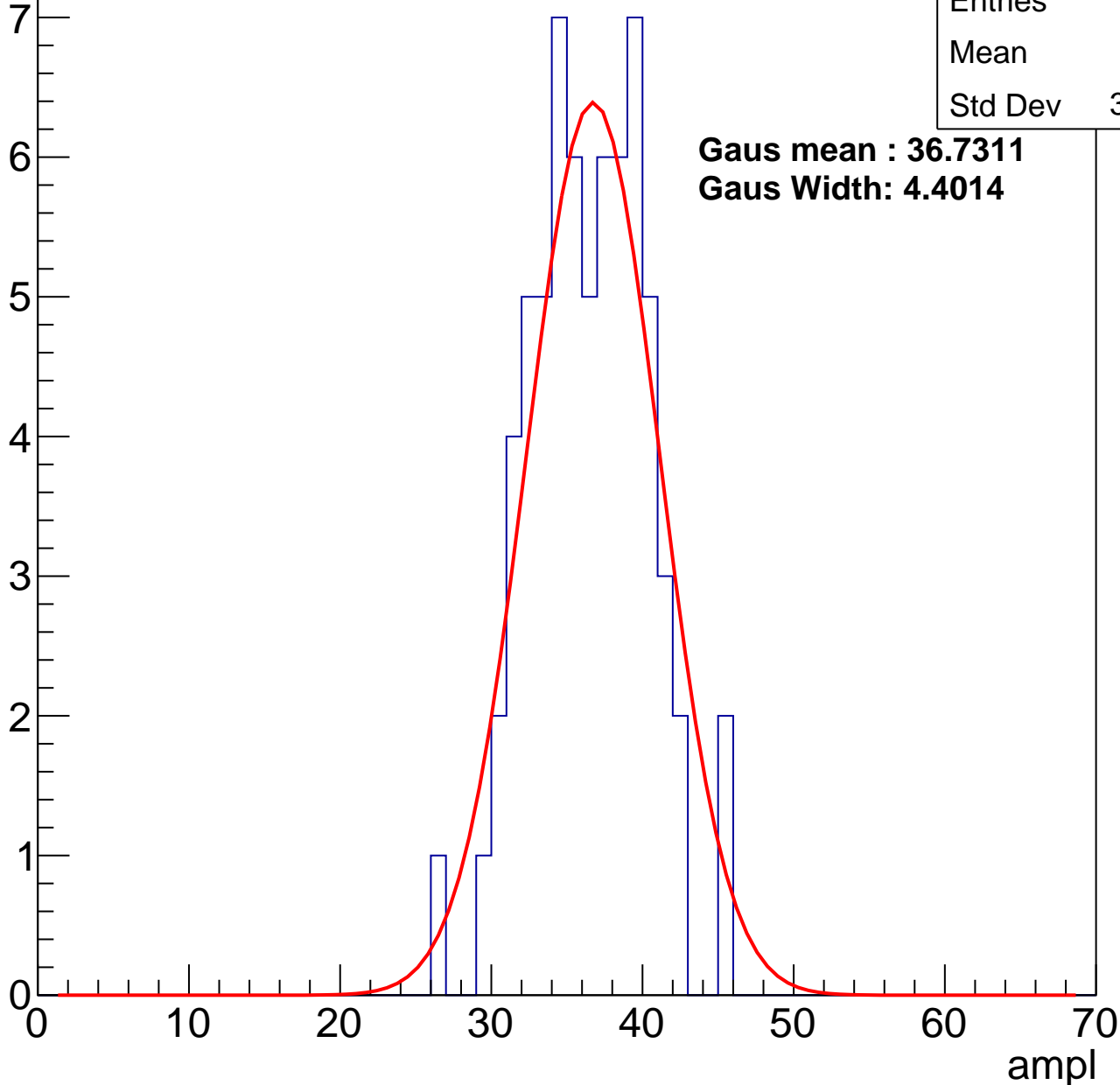
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	36
Std Dev	3.789

**Gaus mean : 36.7311**

**Gaus Width: 4.4014**



# B0L001S, U5-ch40, adc2

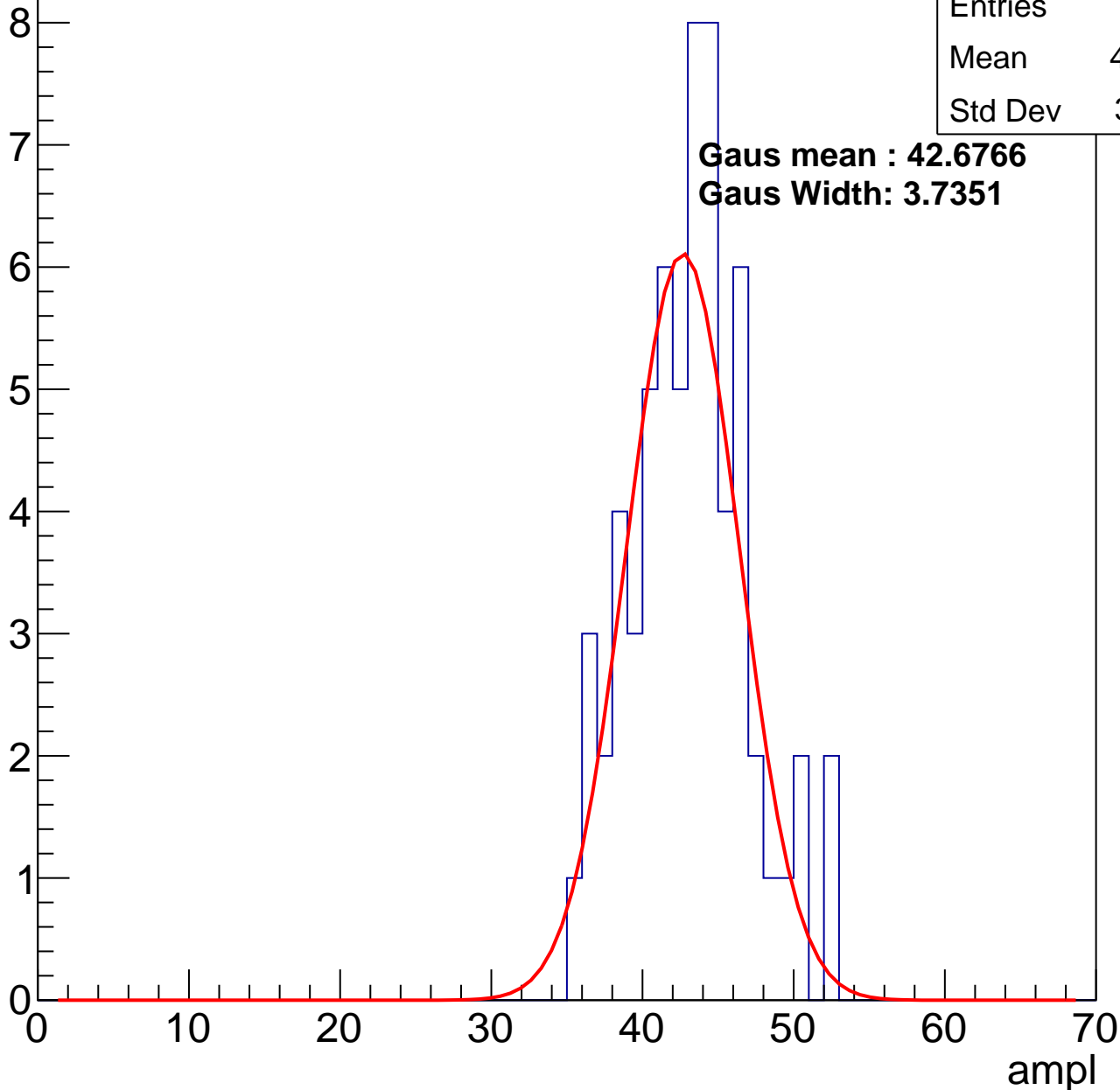
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	42.68
Std Dev	3.841

**Gaus mean : 42.6766**

**Gaus Width: 3.7351**

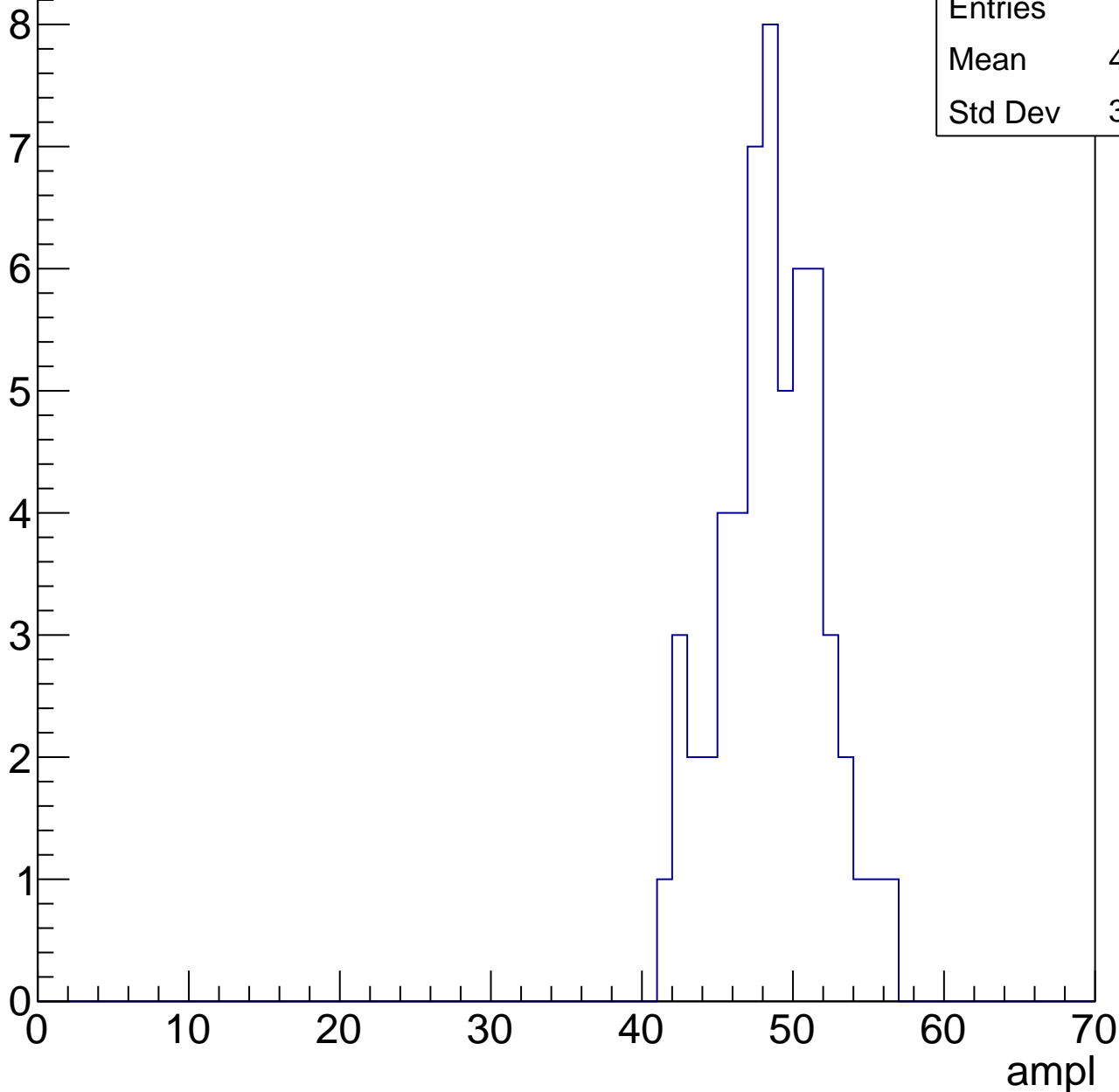


# B0L001S, U5-ch40, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

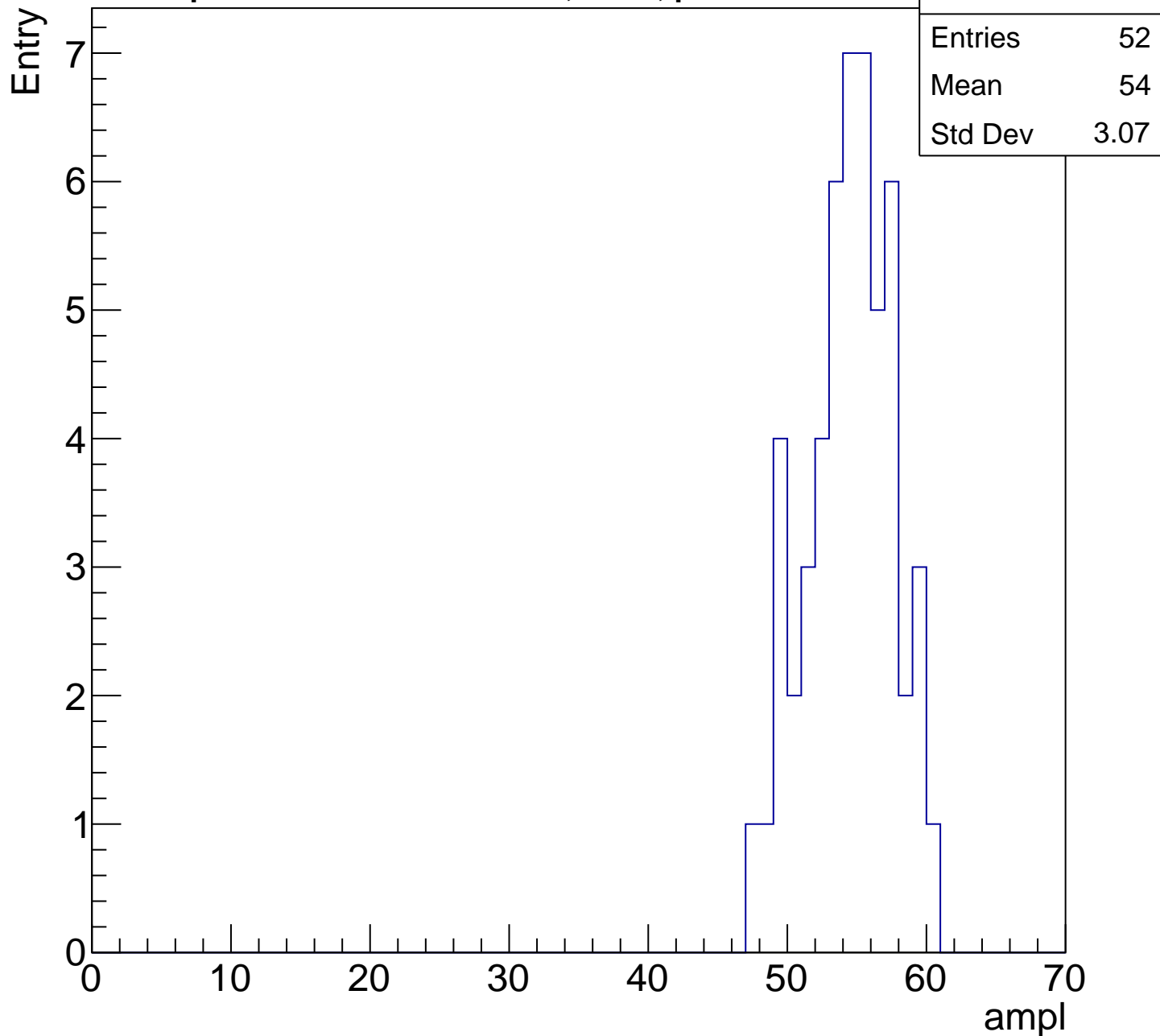
Entry

Entries	56
Mean	48.14
Std Dev	3.346



# B0L001S, U5-ch40, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

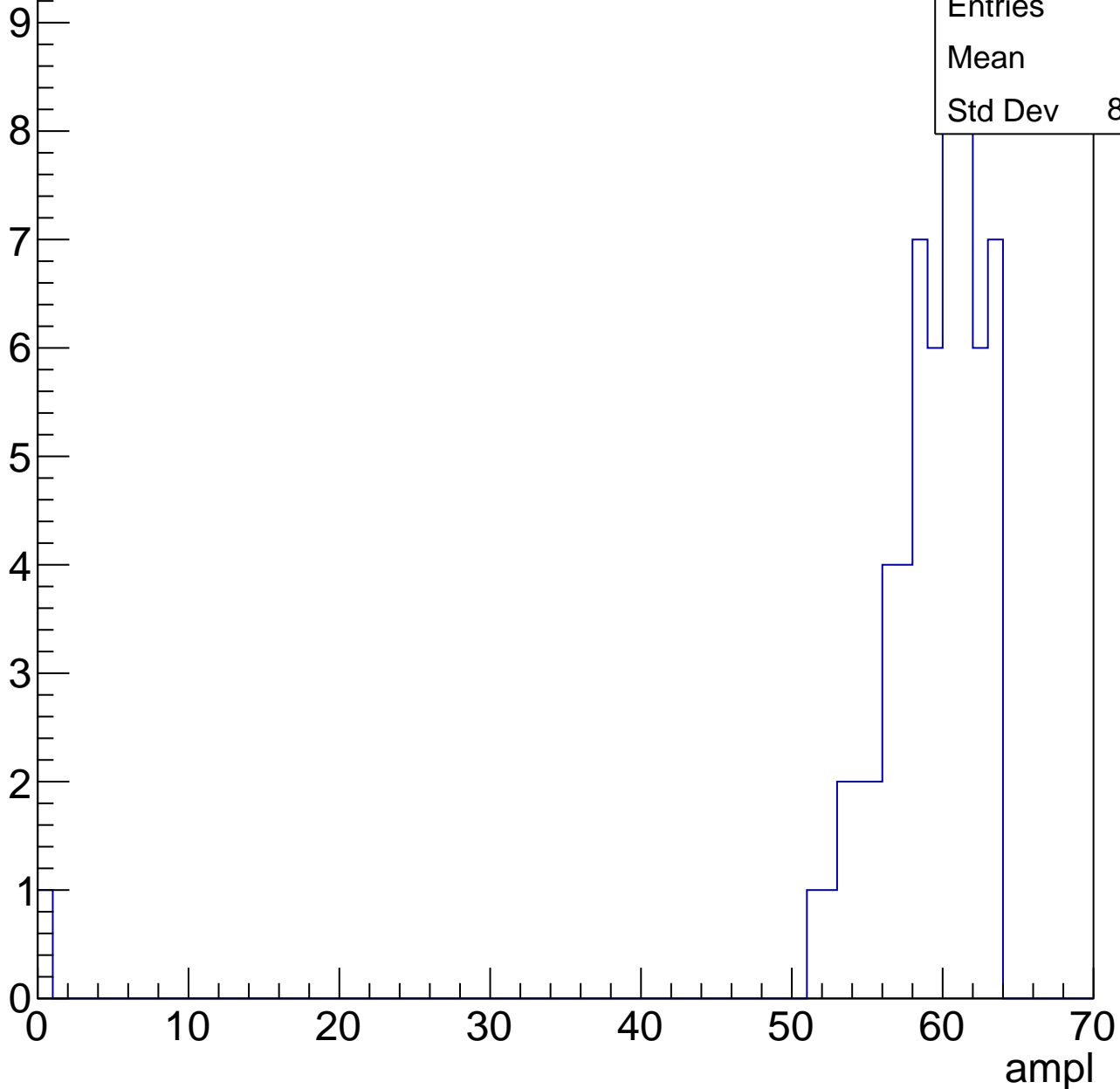


# B0L001S, U5-ch40, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

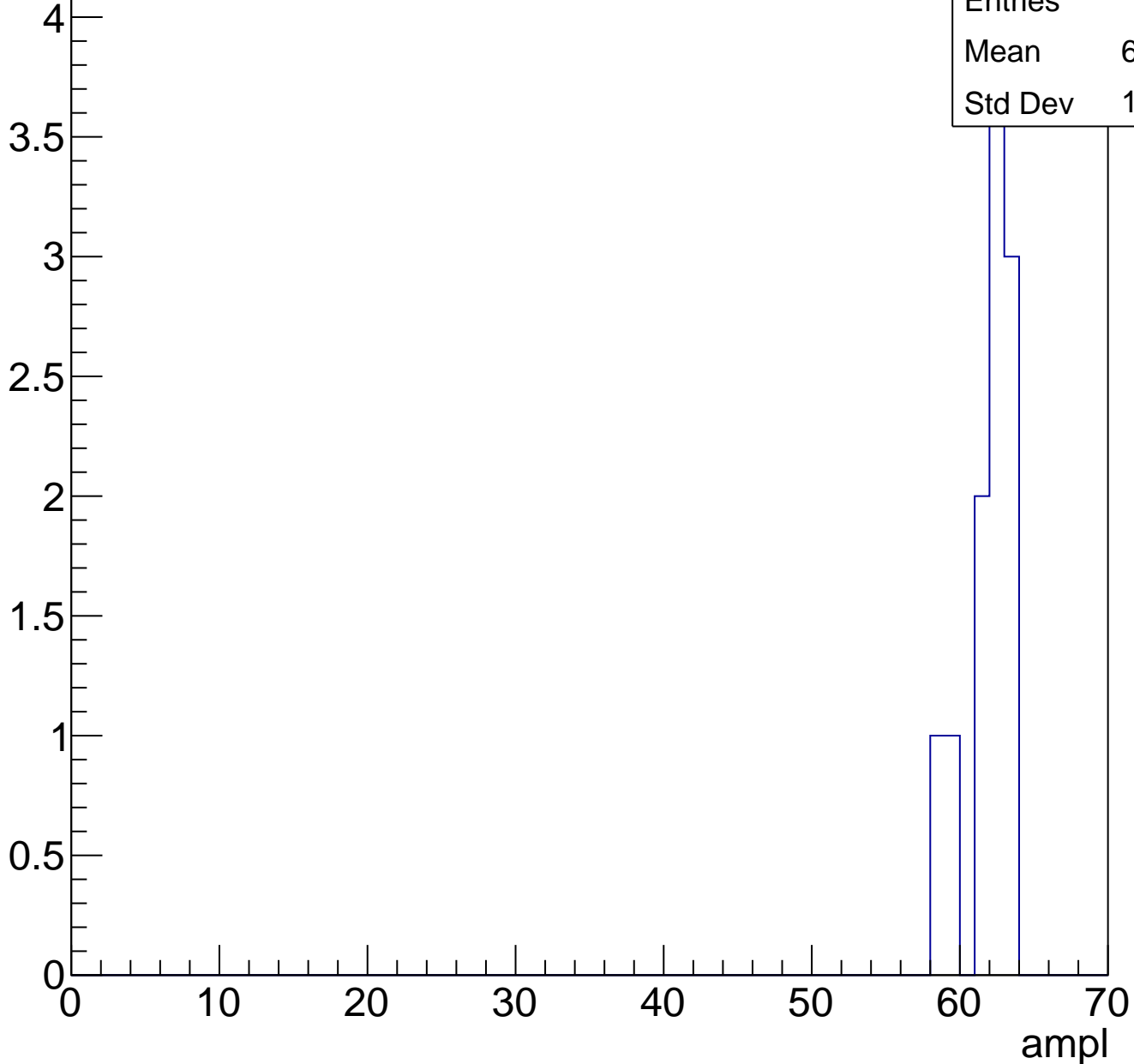
Entries	60
Mean	58
Std Dev	8.118



# B0L001S, U5-ch40, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch40, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch41, adc0

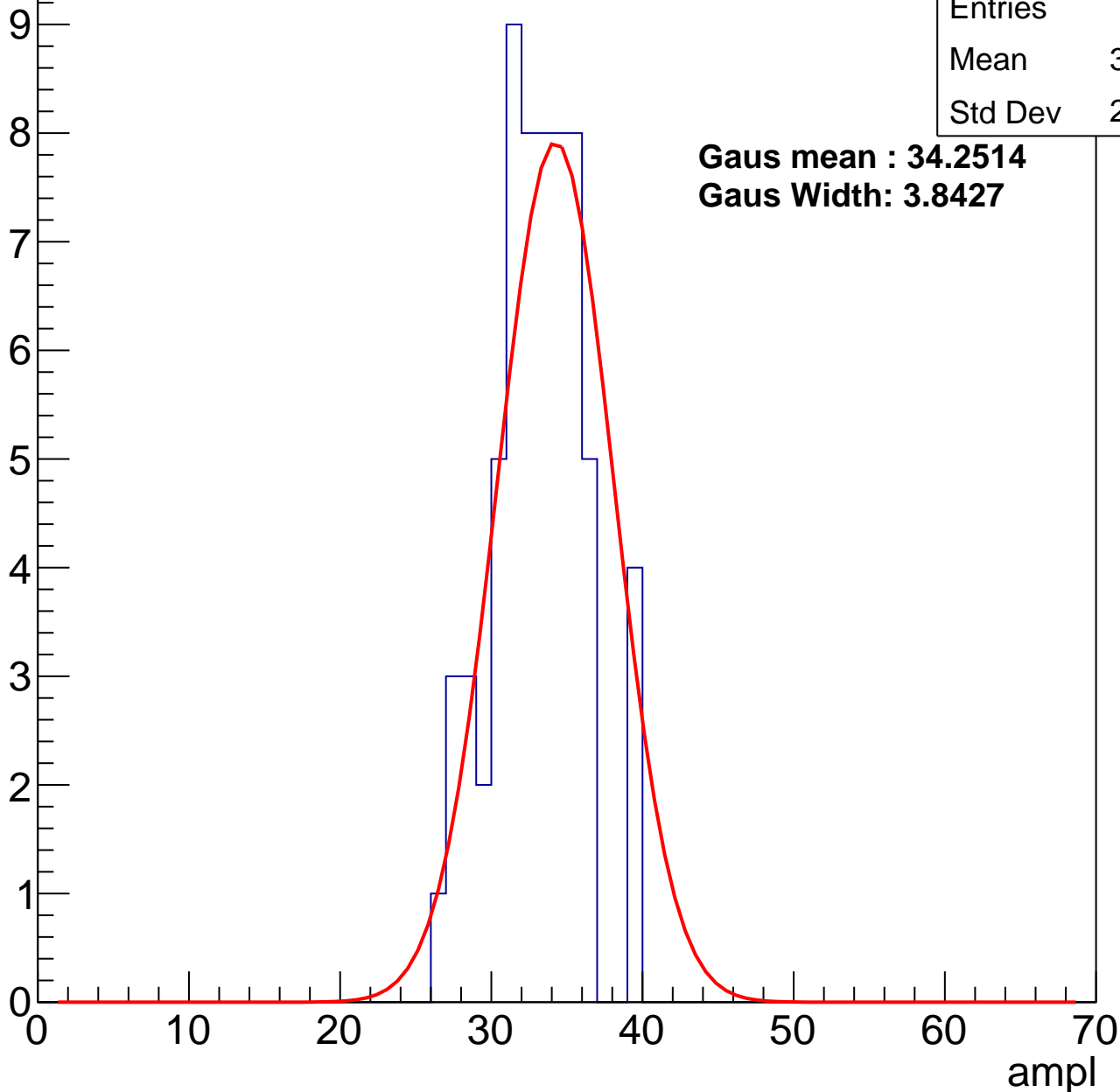
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	32.59
Std Dev	2.988

**Gaus mean : 34.2514**

**Gaus Width: 3.8427**



# B0L001S, U5-ch41, adc1

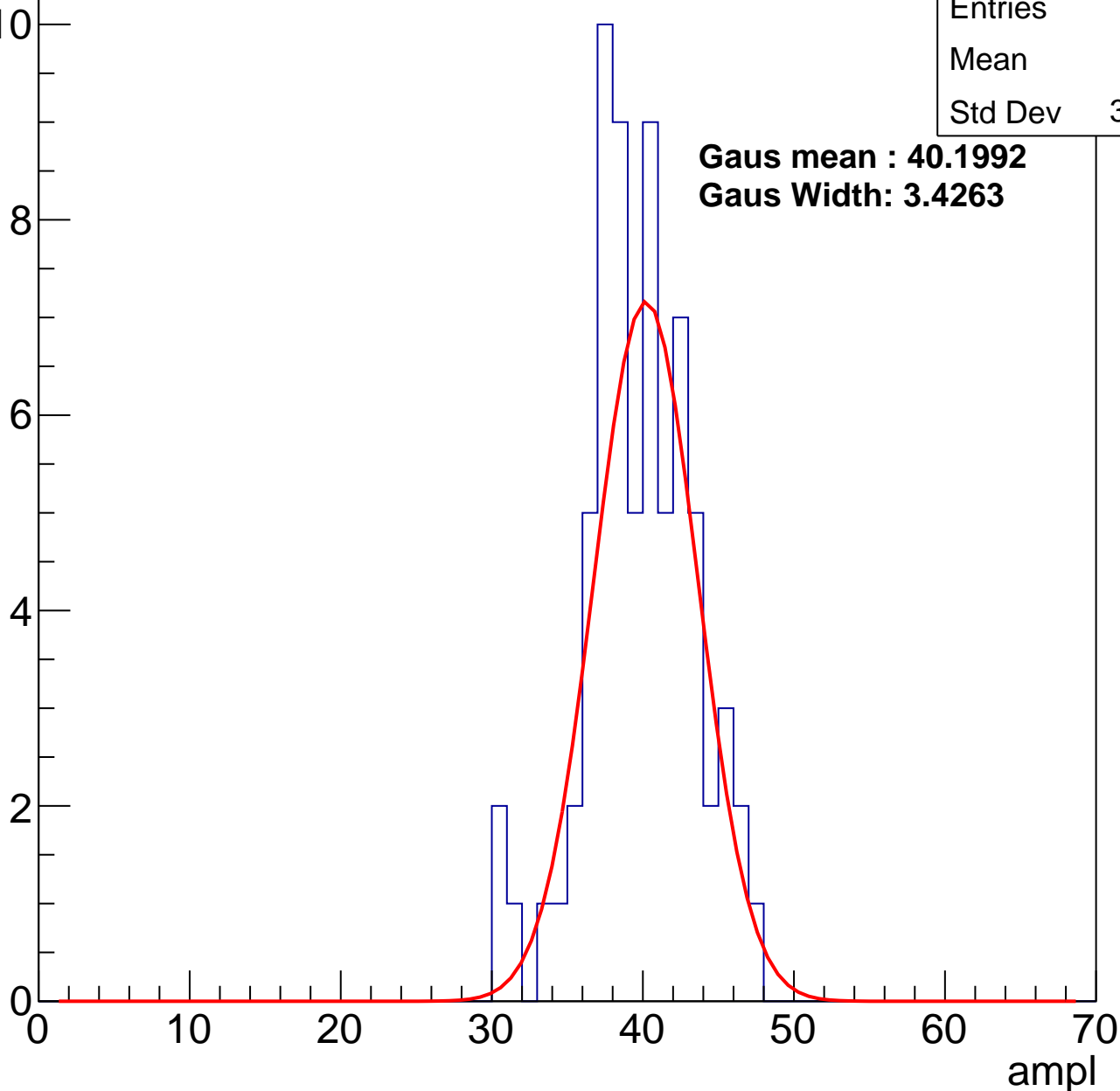
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	39.3
Std Dev	3.583

**Gaus mean : 40.1992**

**Gaus Width: 3.4263**



# B0L001S, U5-ch41, adc2

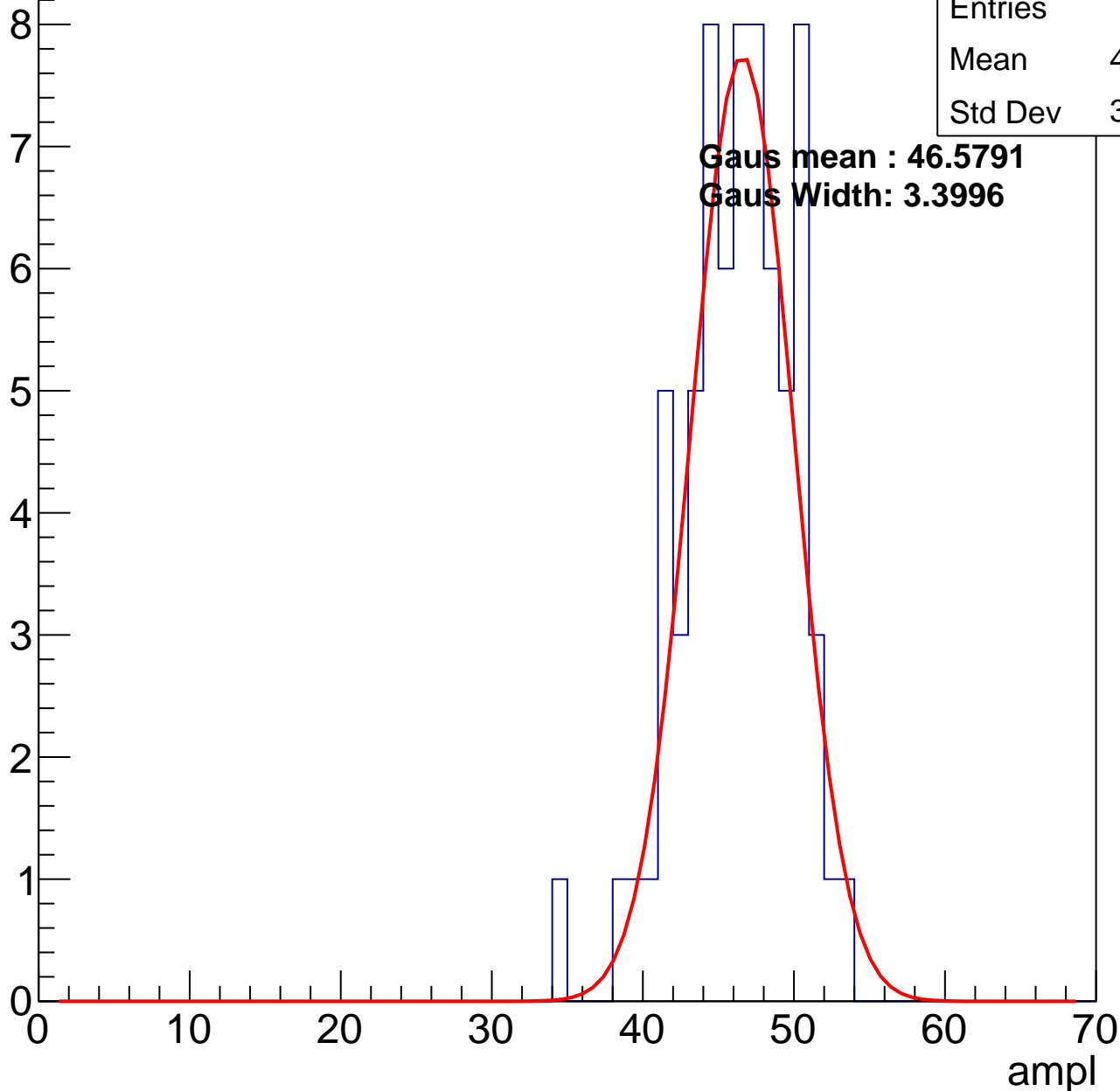
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	45.83
Std Dev	3.584

**Gaus mean : 46.5791**

**Gaus Width: 3.3996**

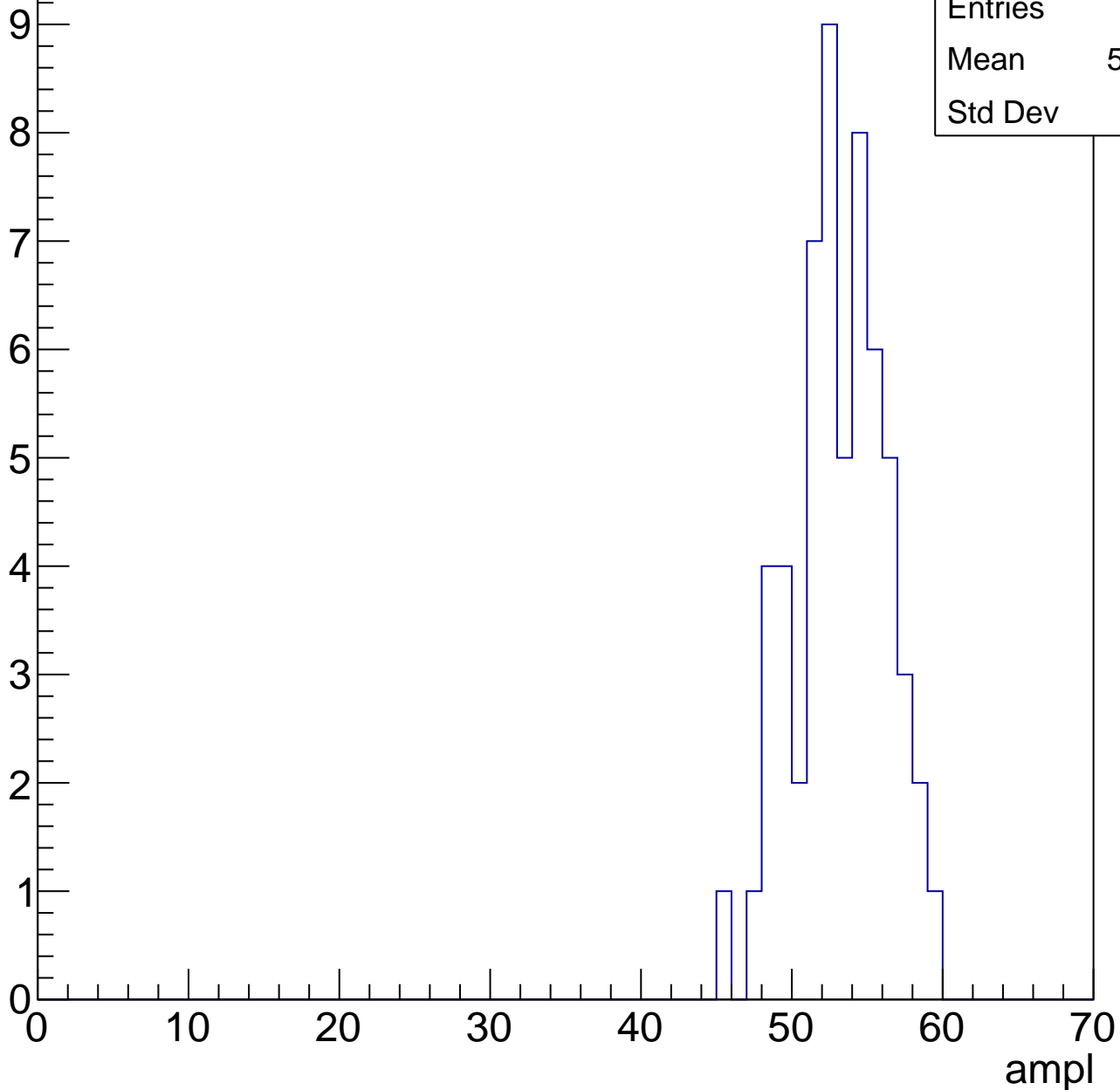


# B0L001S, U5-ch41, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	52.72
Std Dev	3.01

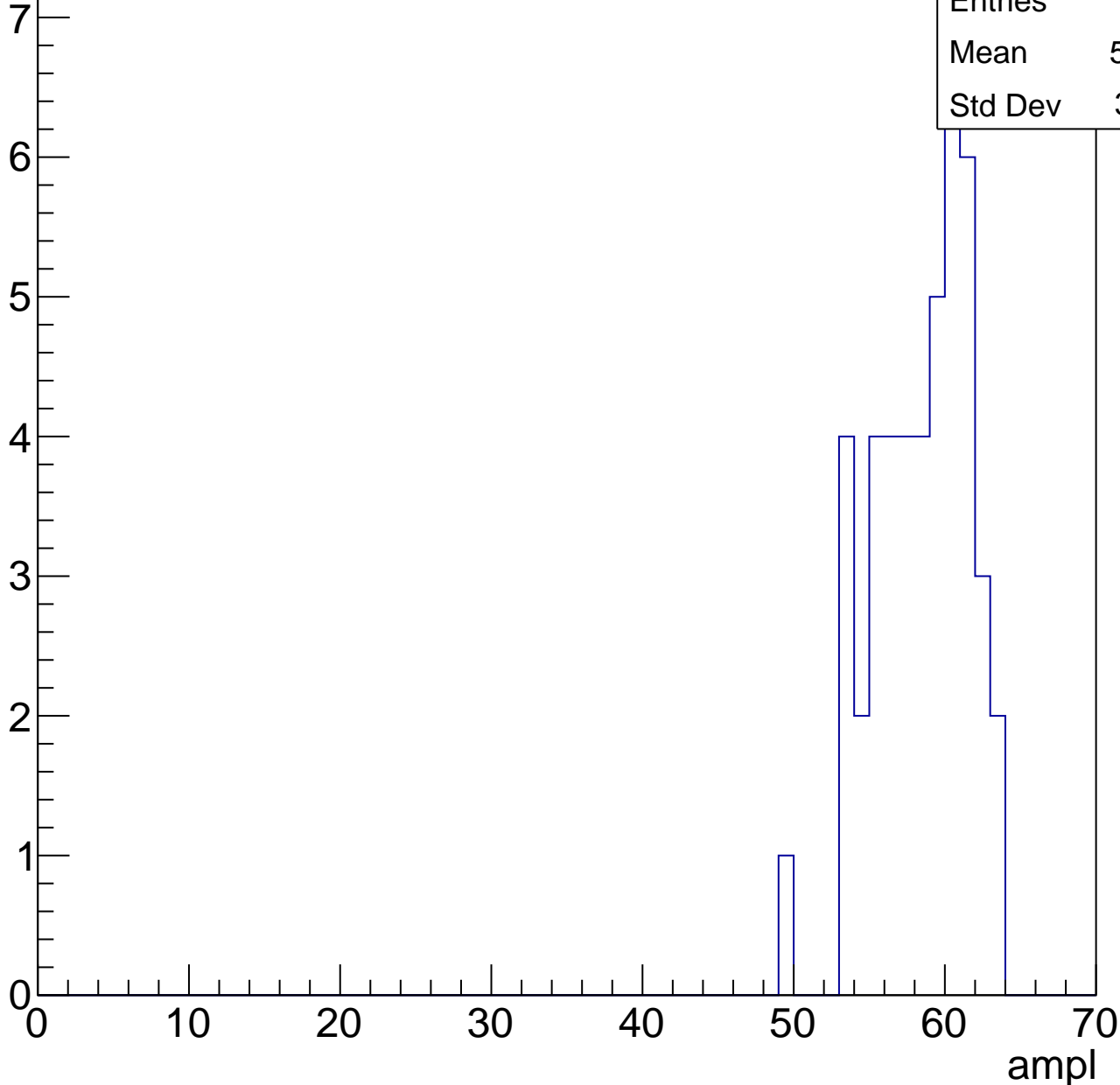


# B0L001S, U5-ch41, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	46
Mean	57.96
Std Dev	3.141

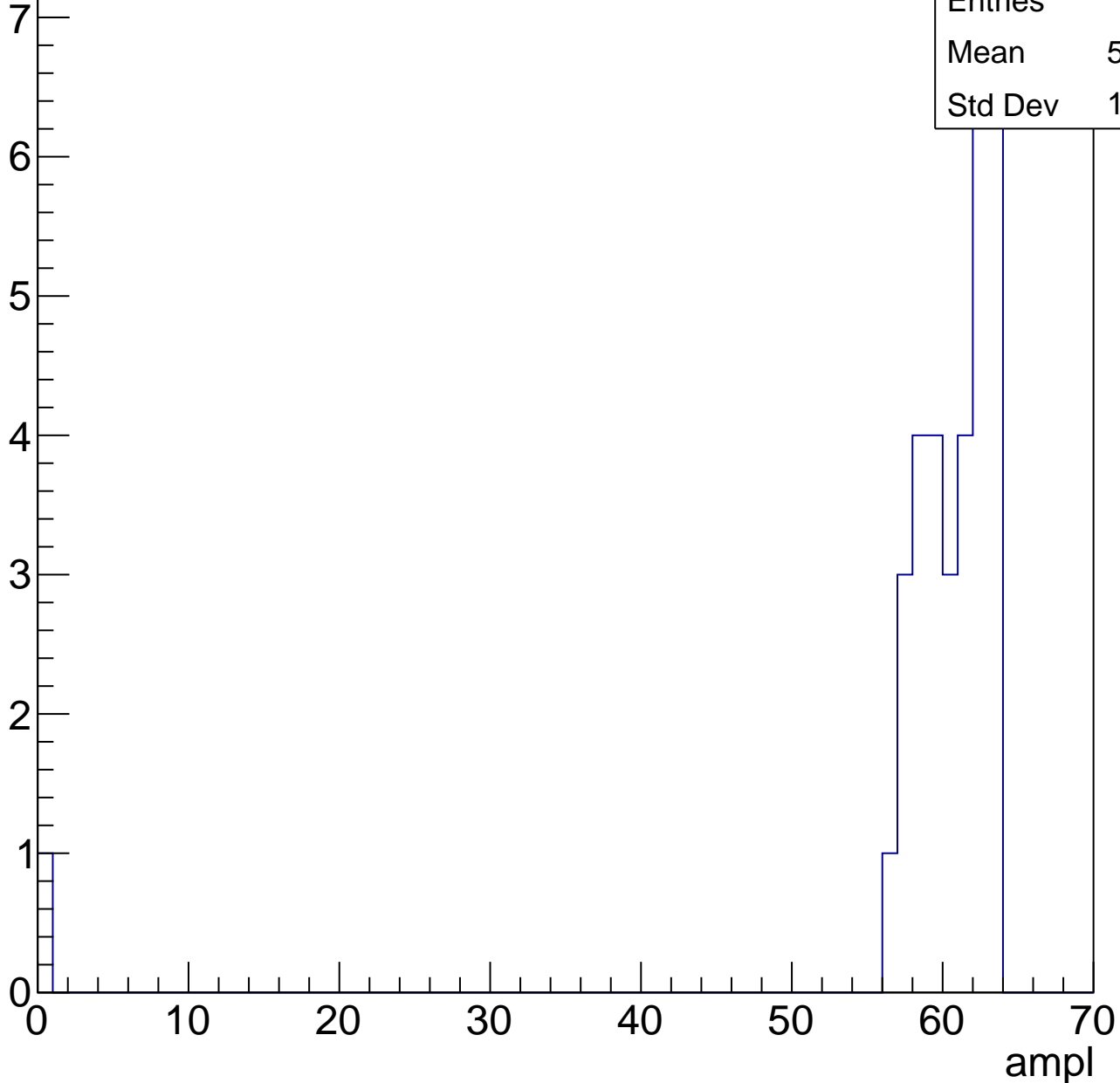


# B0L001S, U5-ch41, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	34
Mean	58.65
Std Dev	10.43



# B0L001S, U5-ch41, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

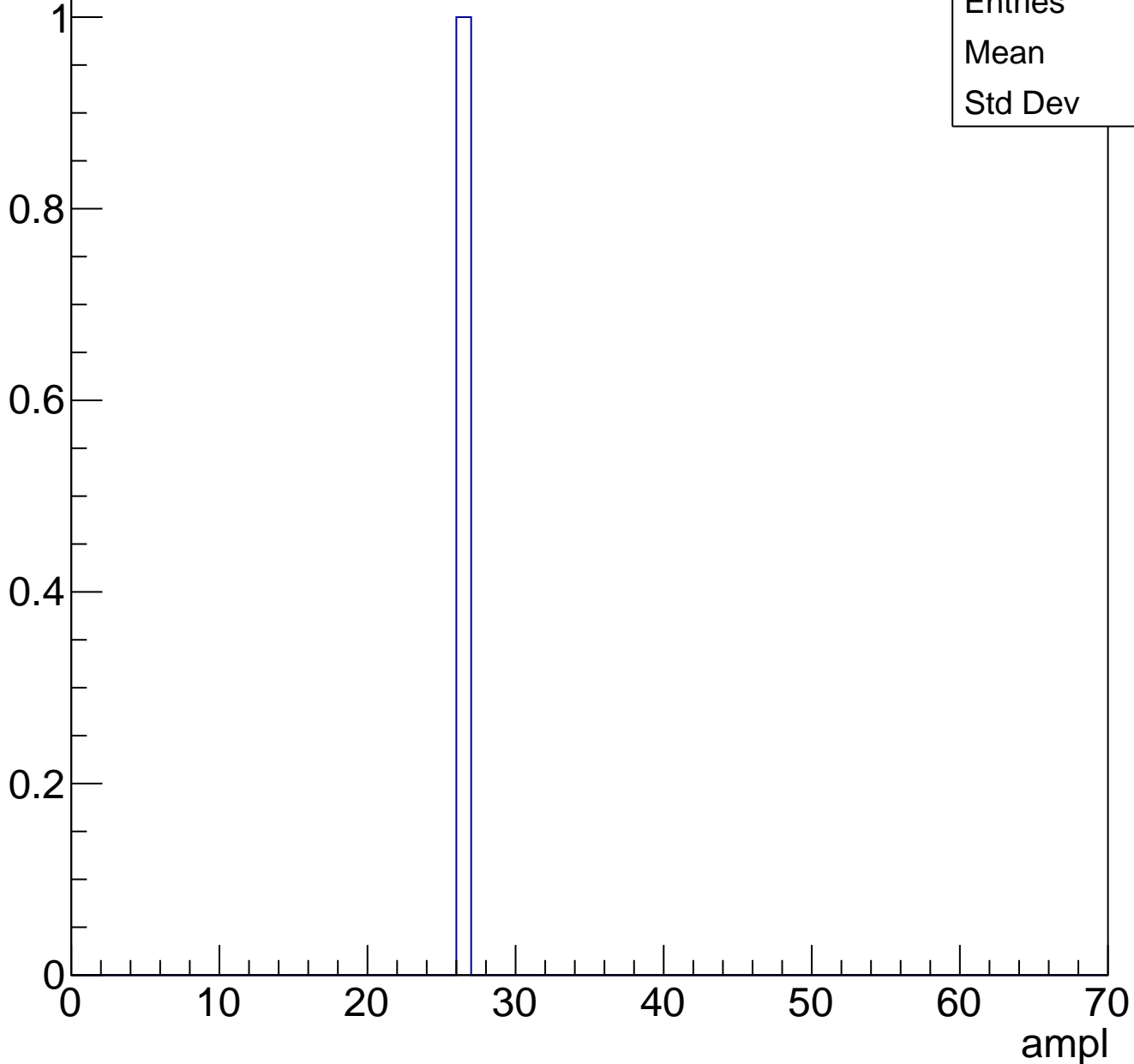




# B0L001S, U5-ch41, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	26
Std Dev	0

# B0L001S, U5-ch42, adc0

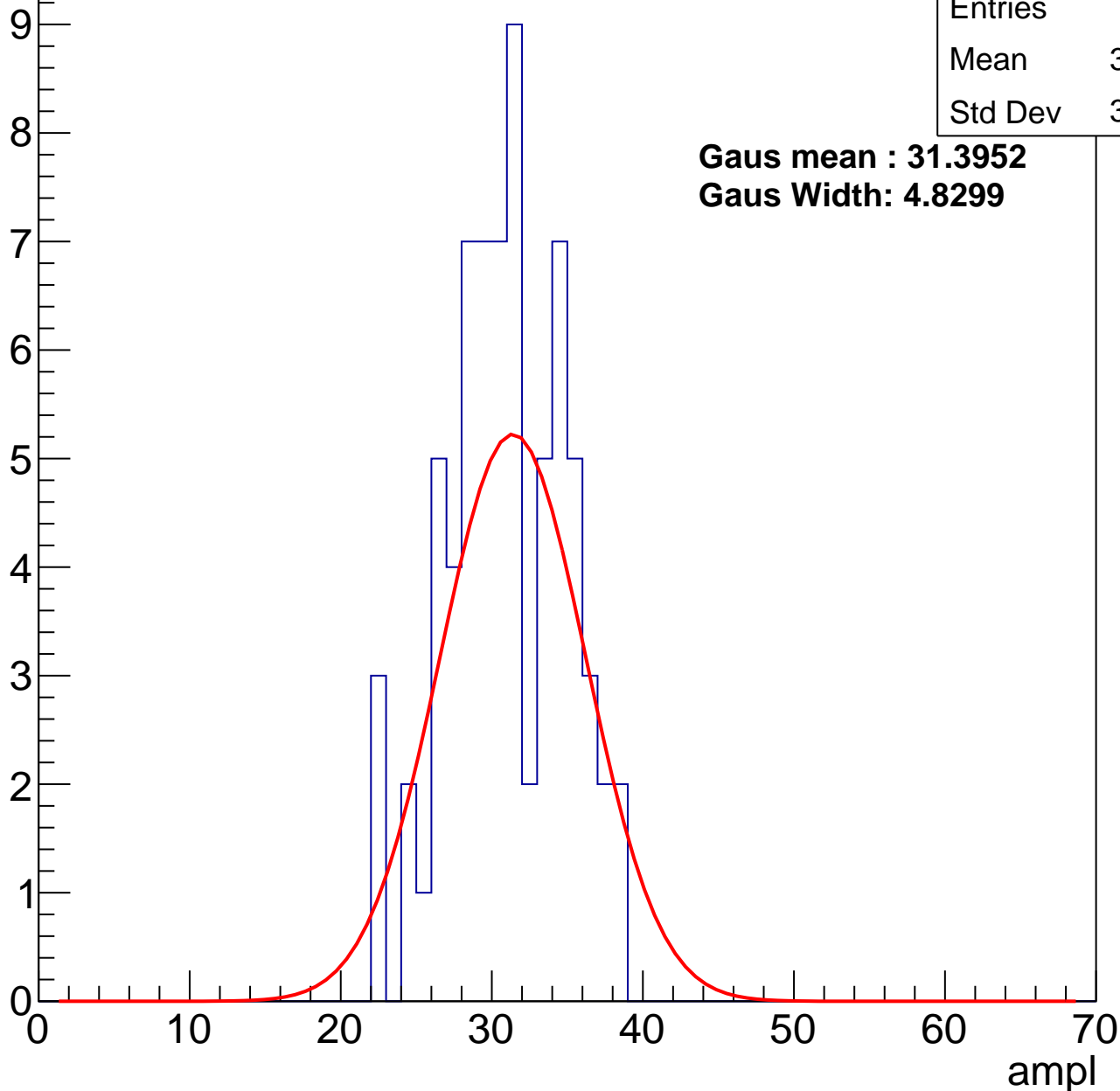
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	30.49
Std Dev	3.856

**Gaus mean : 31.3952**

**Gaus Width: 4.8299**



# B0L001S, U5-ch42, adc1

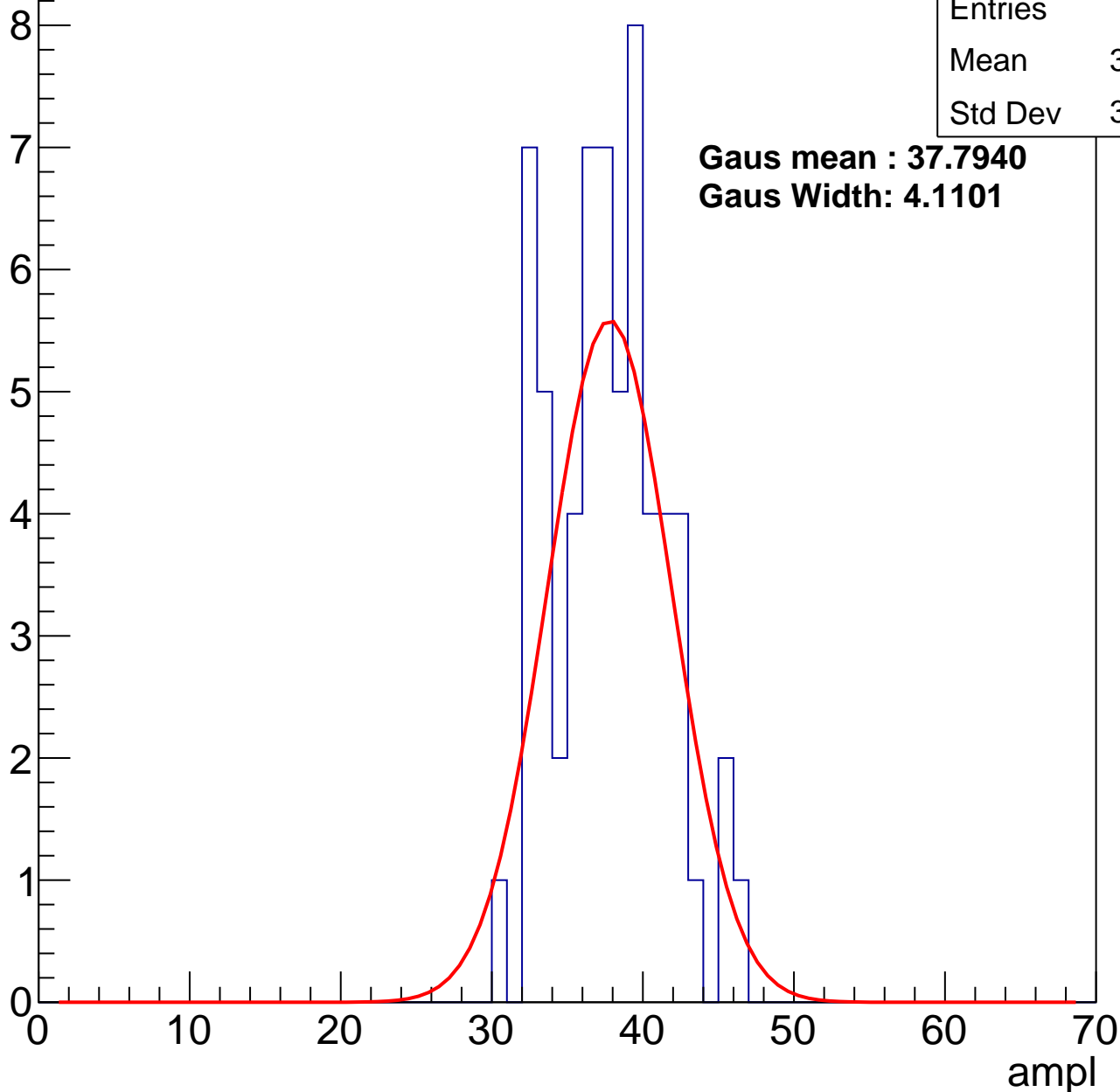
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	37.27
Std Dev	3.642

**Gaus mean : 37.7940**

**Gaus Width: 4.1101**



# B0L001S, U5-ch42, adc2

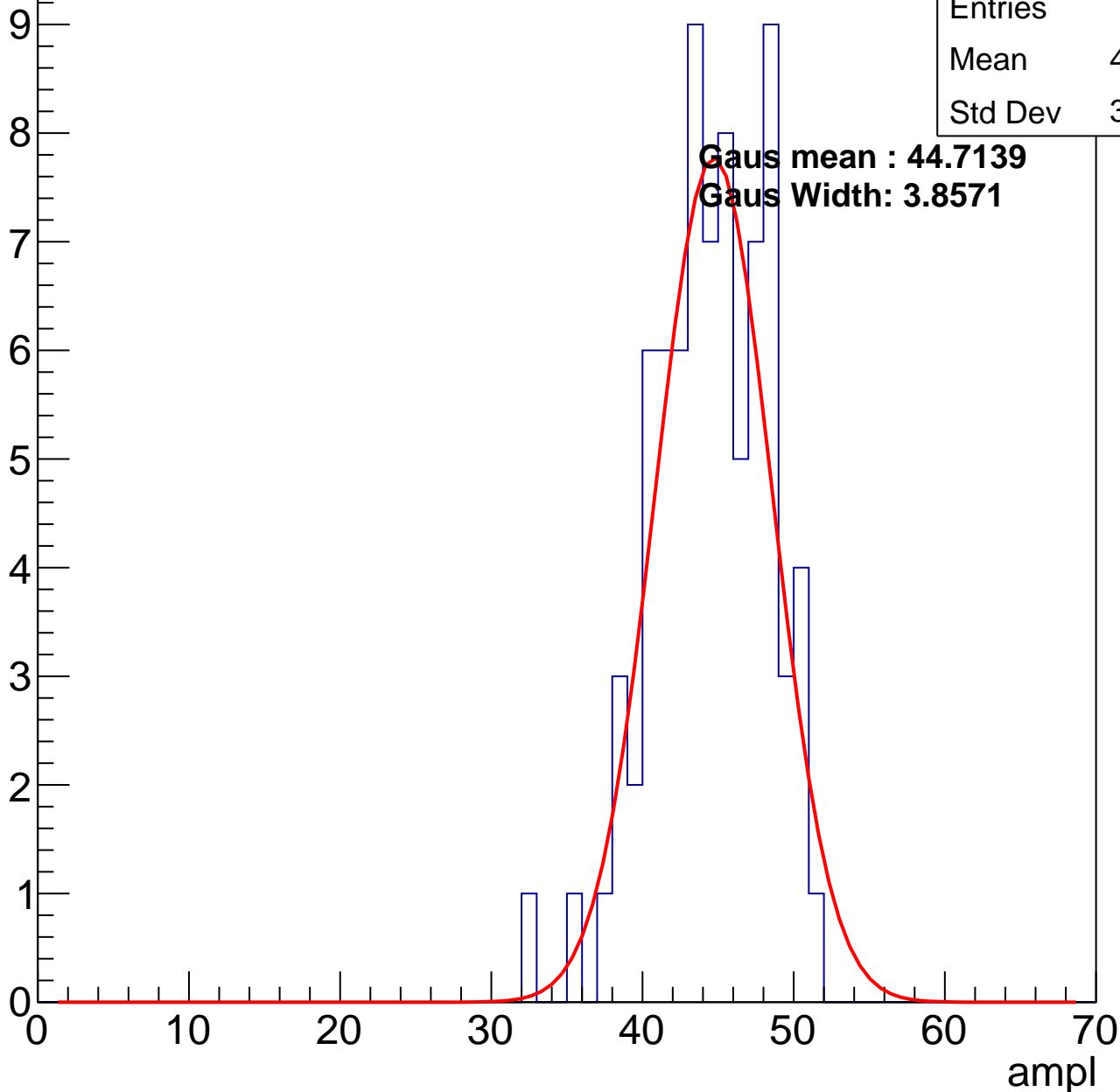
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	79
Mean	44.03
Std Dev	3.762

**Gaus mean : 44.7139**

**Gaus Width: 3.8571**

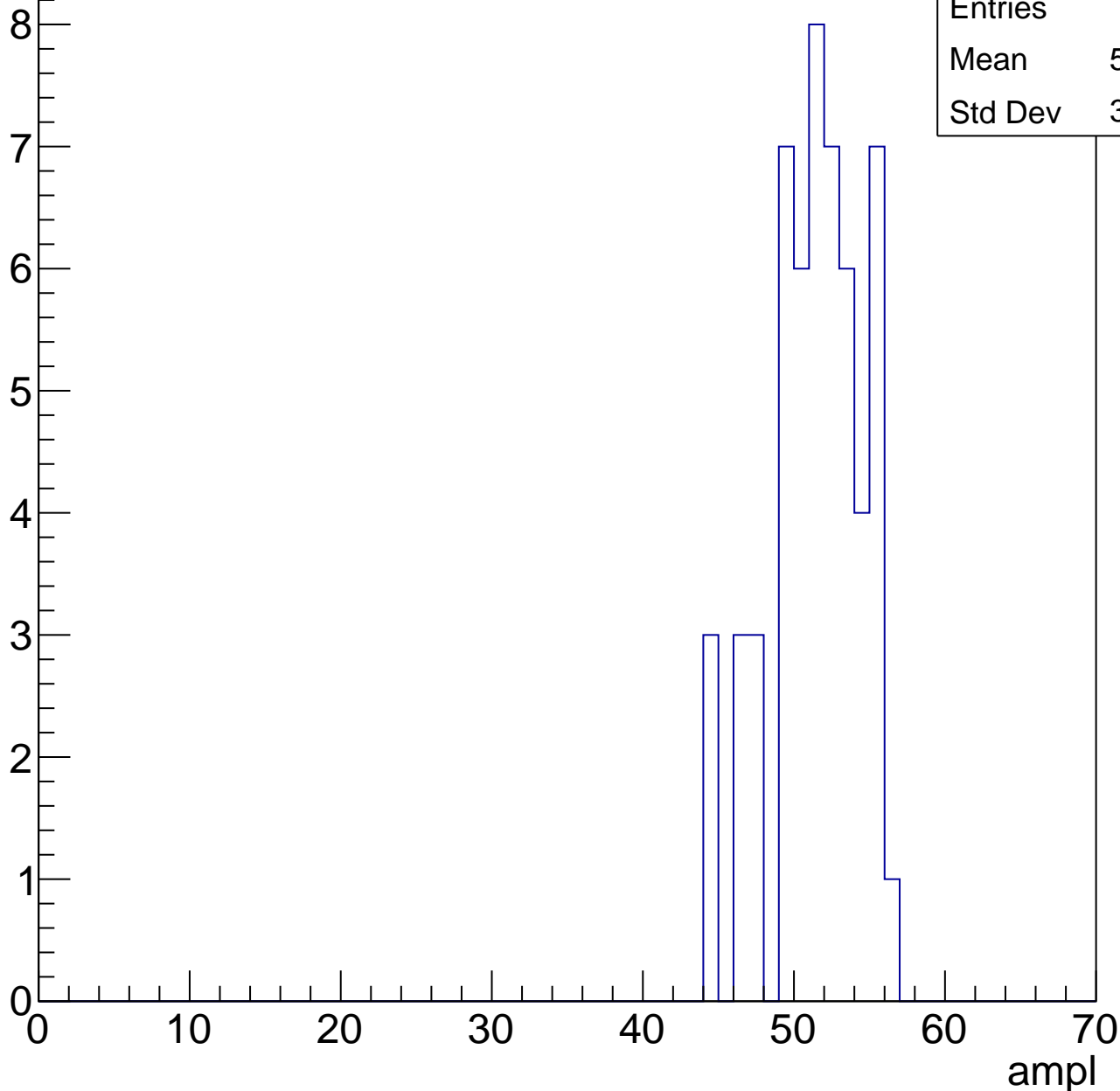


# B0L001S, U5-ch42, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	50.93
Std Dev	3.038

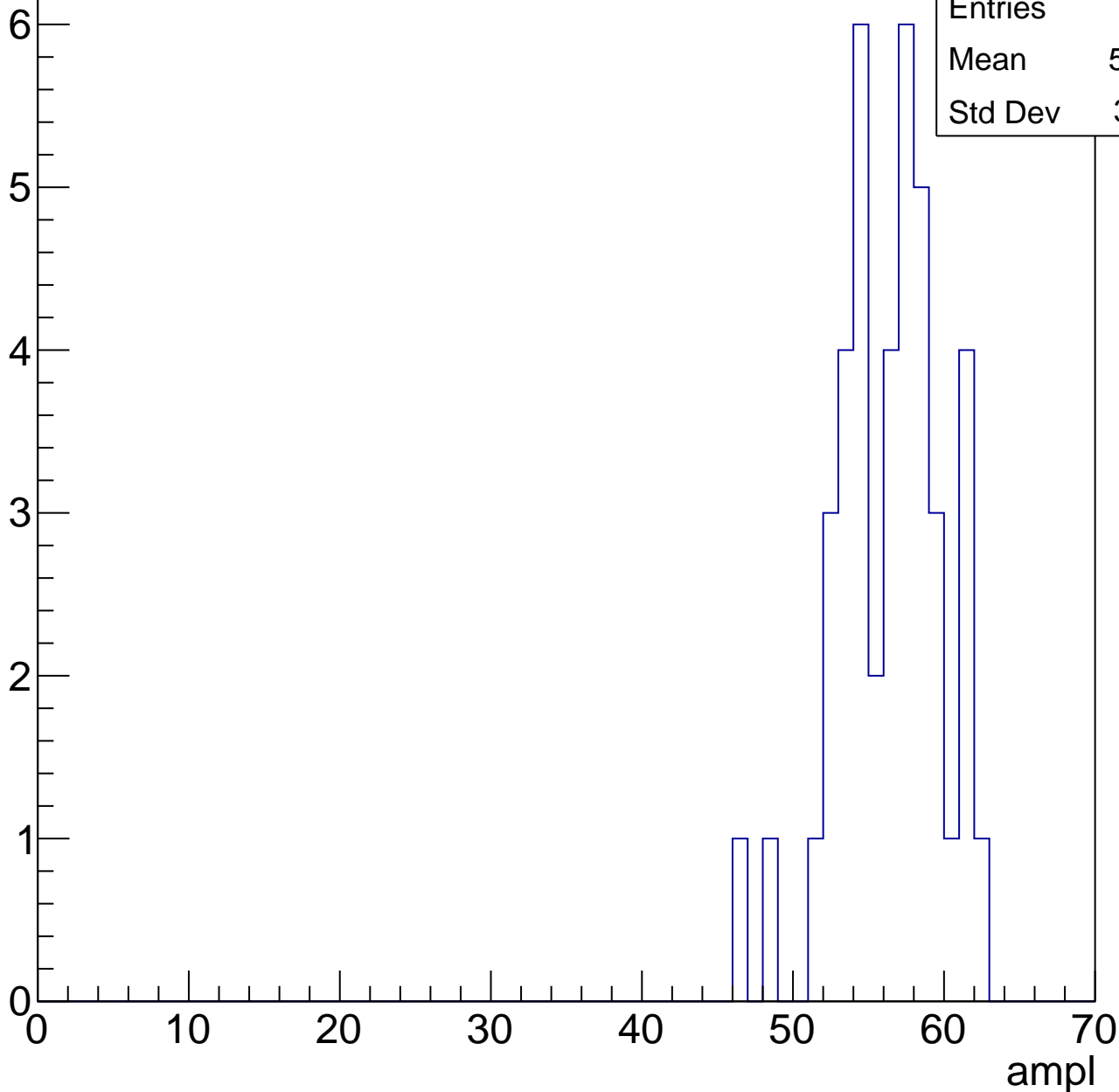


# B0L001S, U5-ch42, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	42
Mean	55.86
Std Dev	3.461



# B0L001S, U5-ch42, adc5

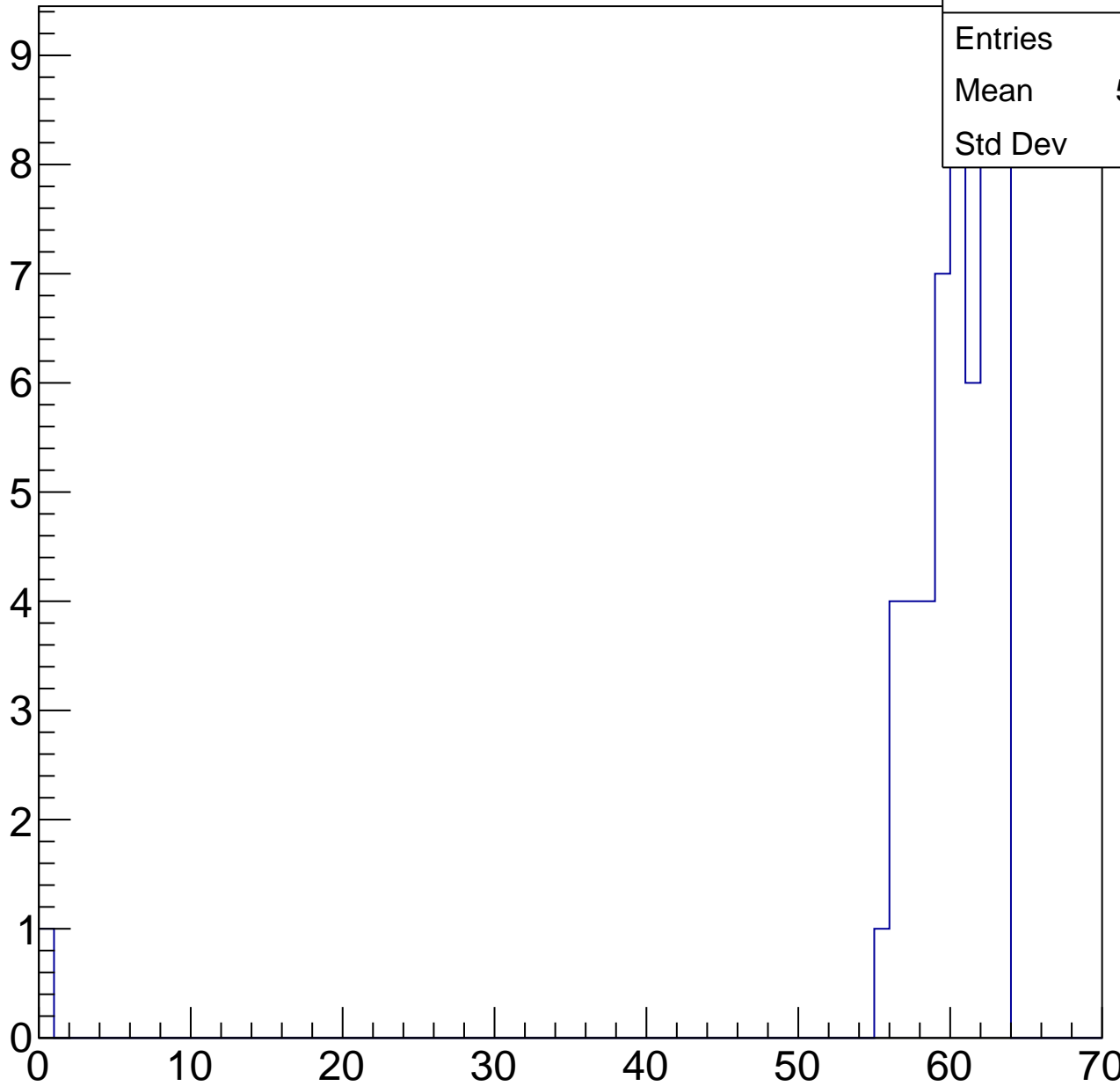
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	54
Mean	58.94
Std Dev	8.401

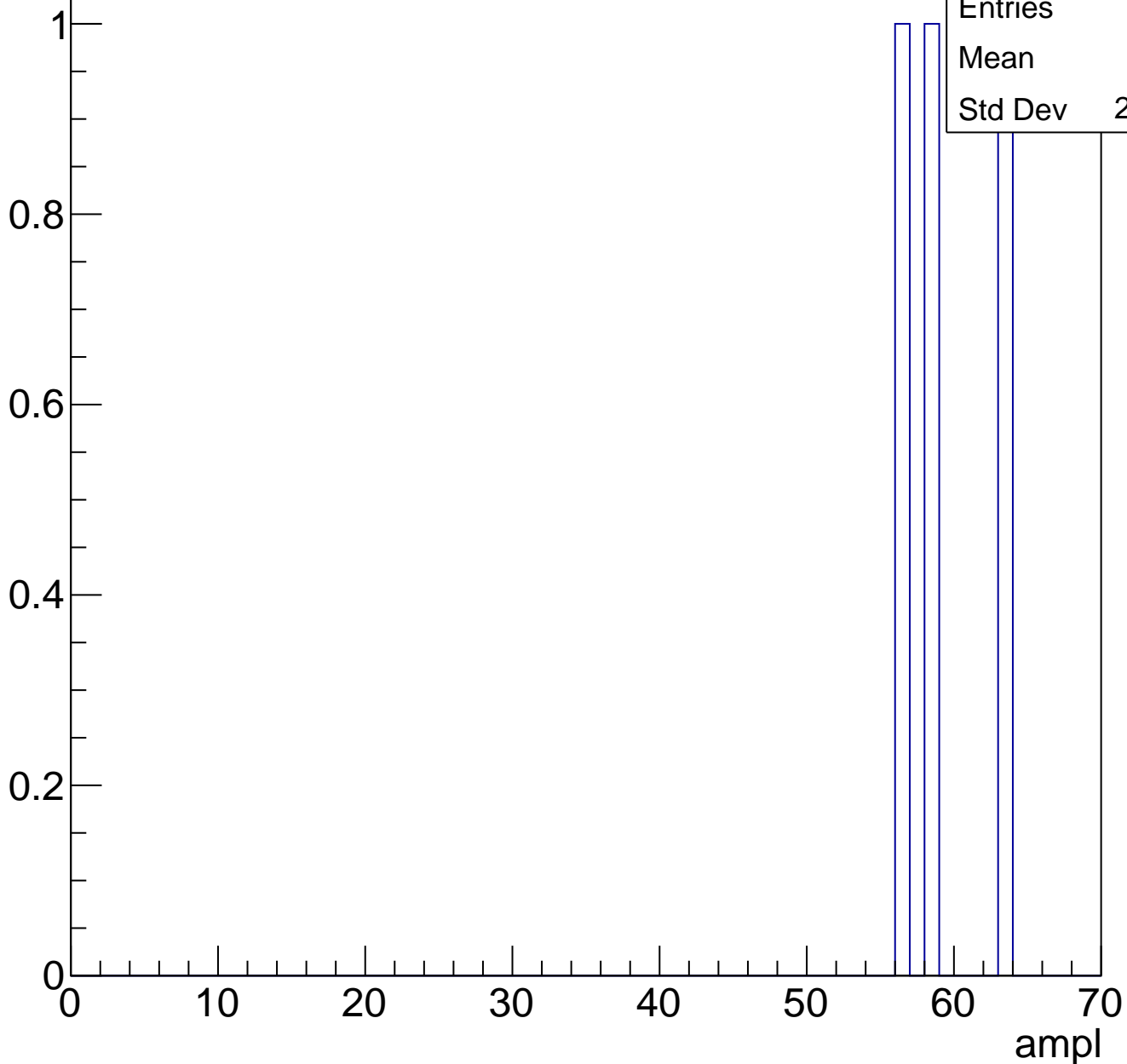
ampl



# B0L001S, U5-ch42, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch42, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch43, adc0

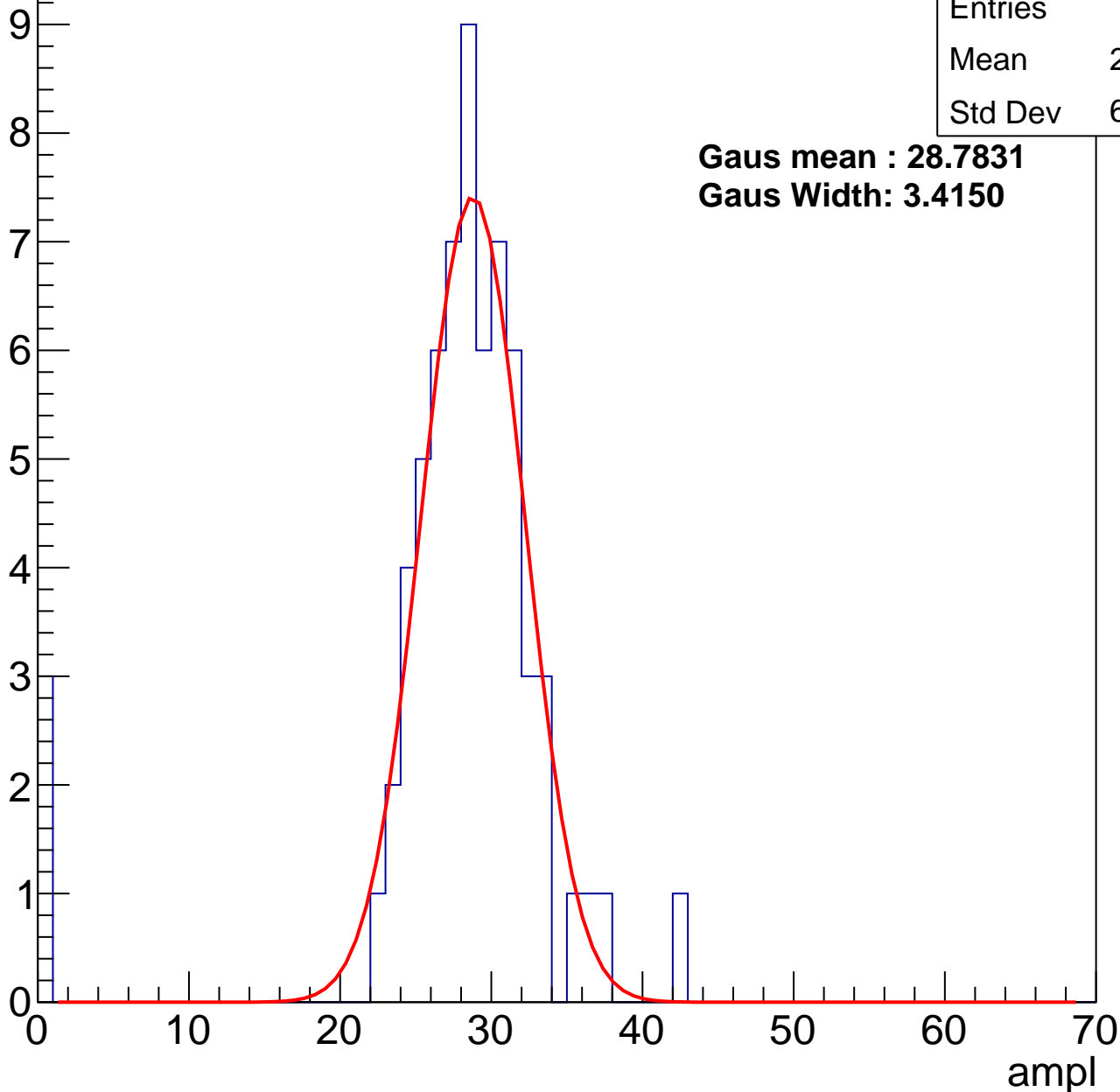
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	27.29
Std Dev	6.904

**Gaus mean : 28.7831**

**Gaus Width: 3.4150**



# B0L001S, U5-ch43, adc1

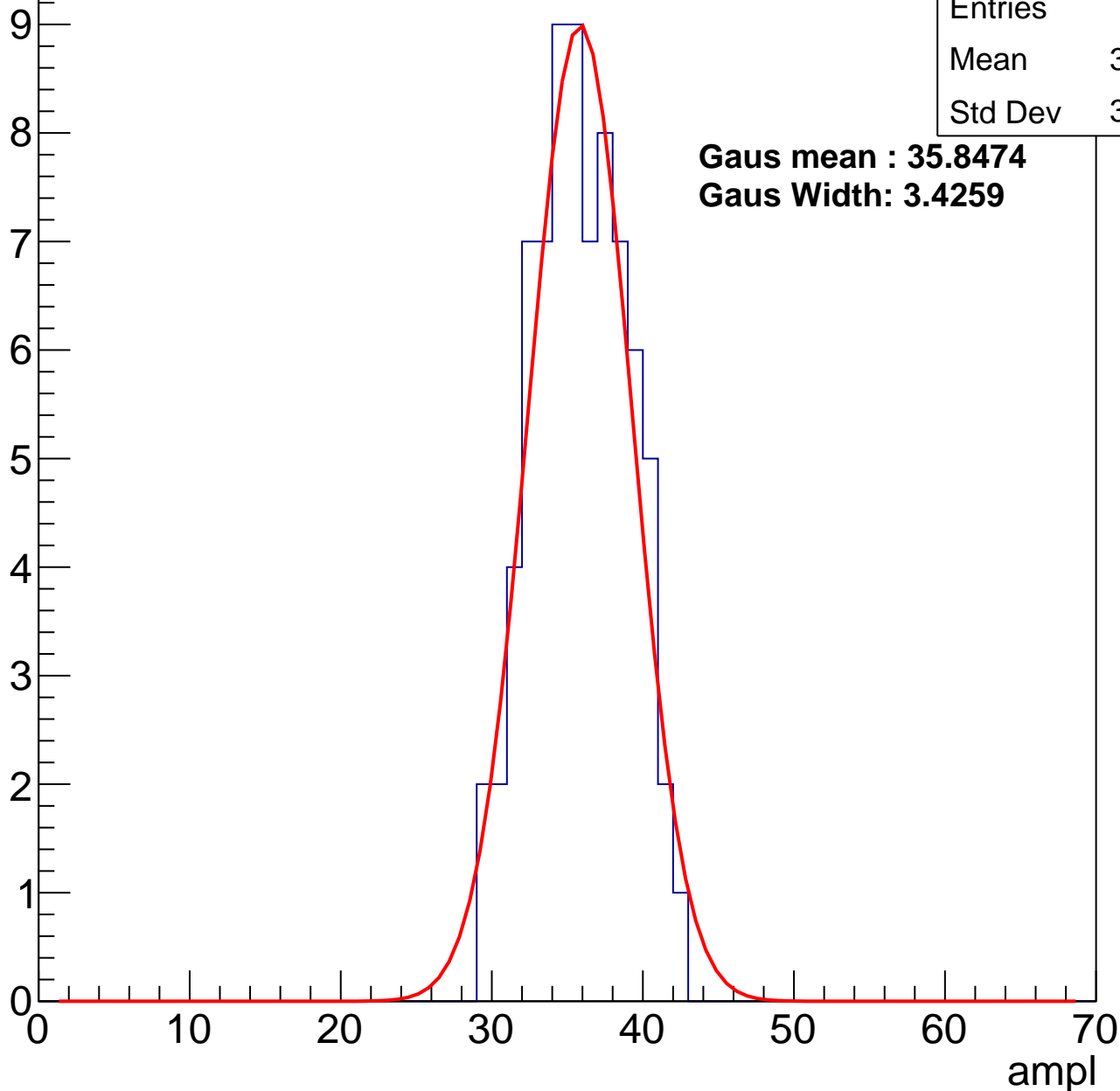
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	76
Mean	35.39
Std Dev	3.074

**Gaus mean : 35.8474**

**Gaus Width: 3.4259**



# B0L001S, U5-ch43, adc2

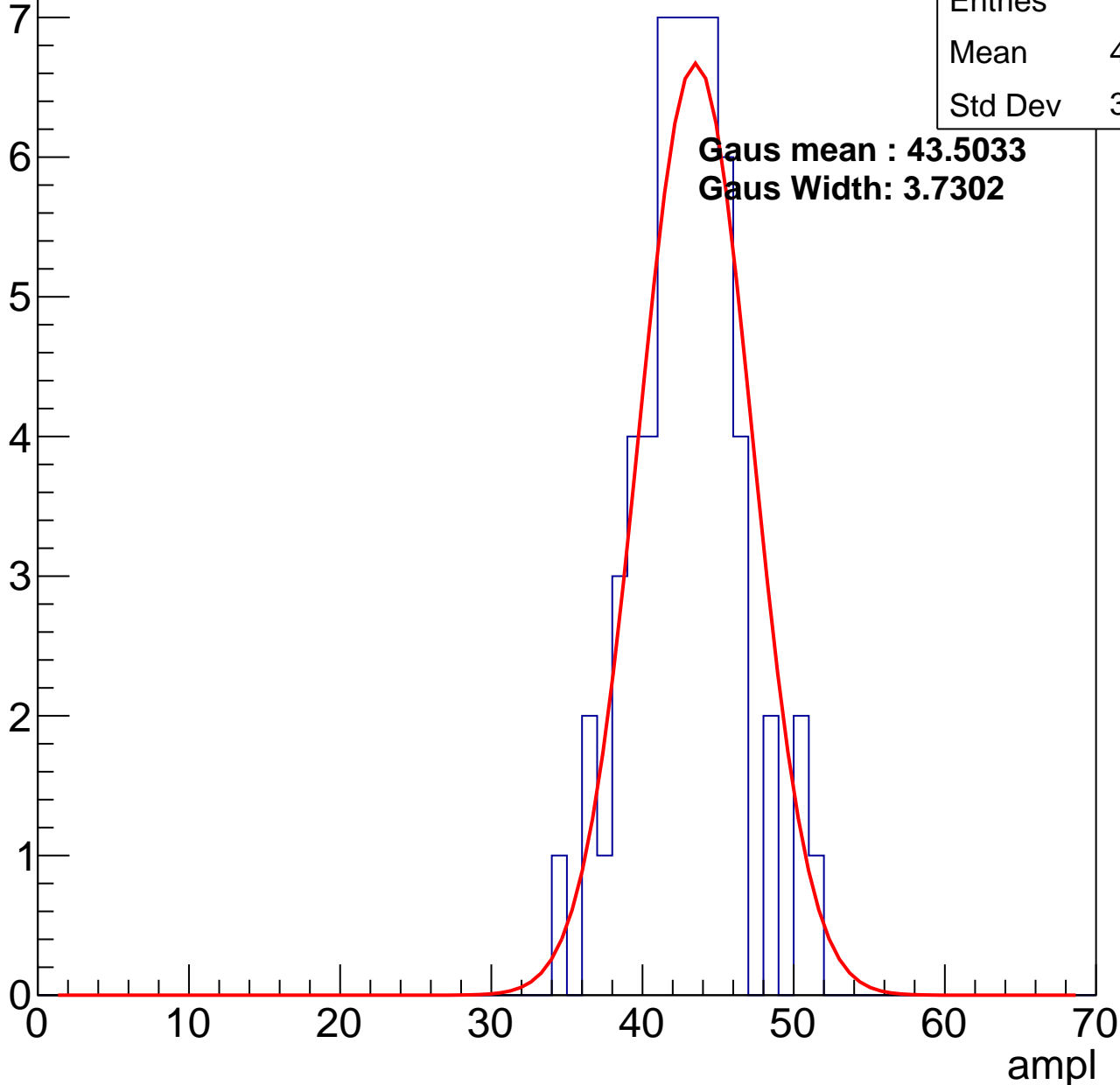
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	42.48
Std Dev	3.445

**Gaus mean : 43.5033**

**Gaus Width: 3.7302**

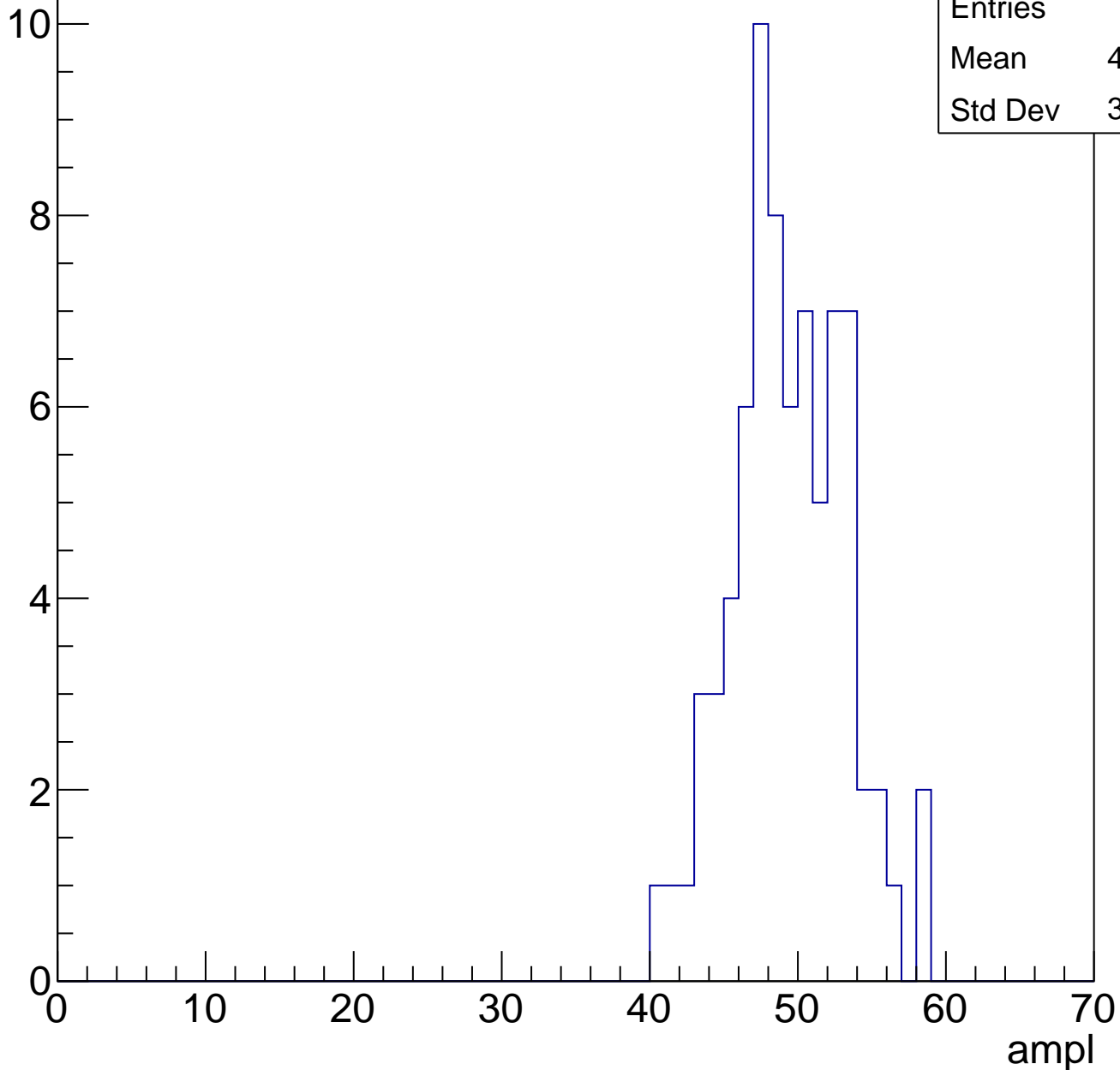


# B0L001S, U5-ch43, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	76
Mean	48.92
Std Dev	3.765

Entry

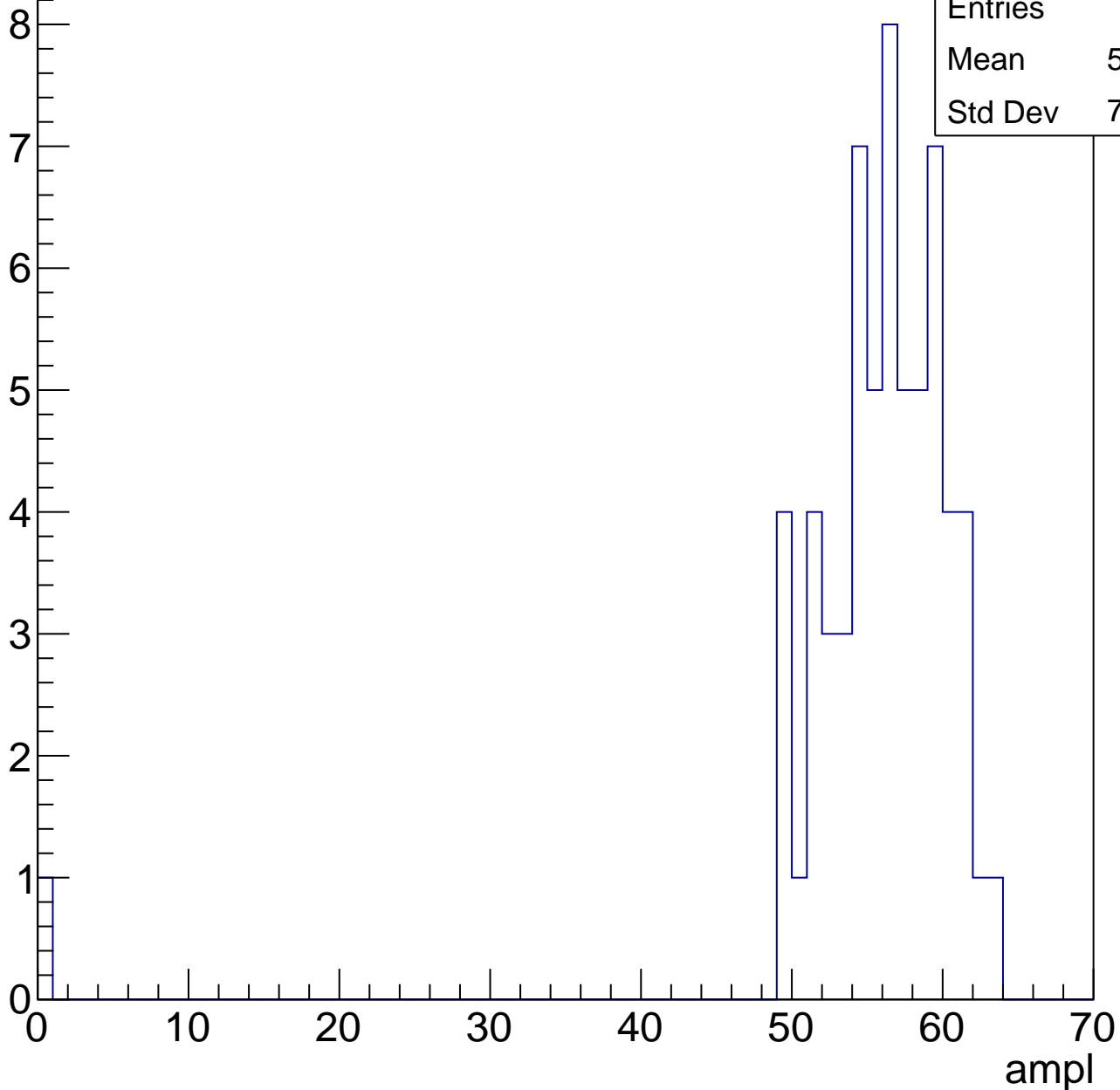


# B0L001S, U5-ch43, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	54.97
Std Dev	7.813

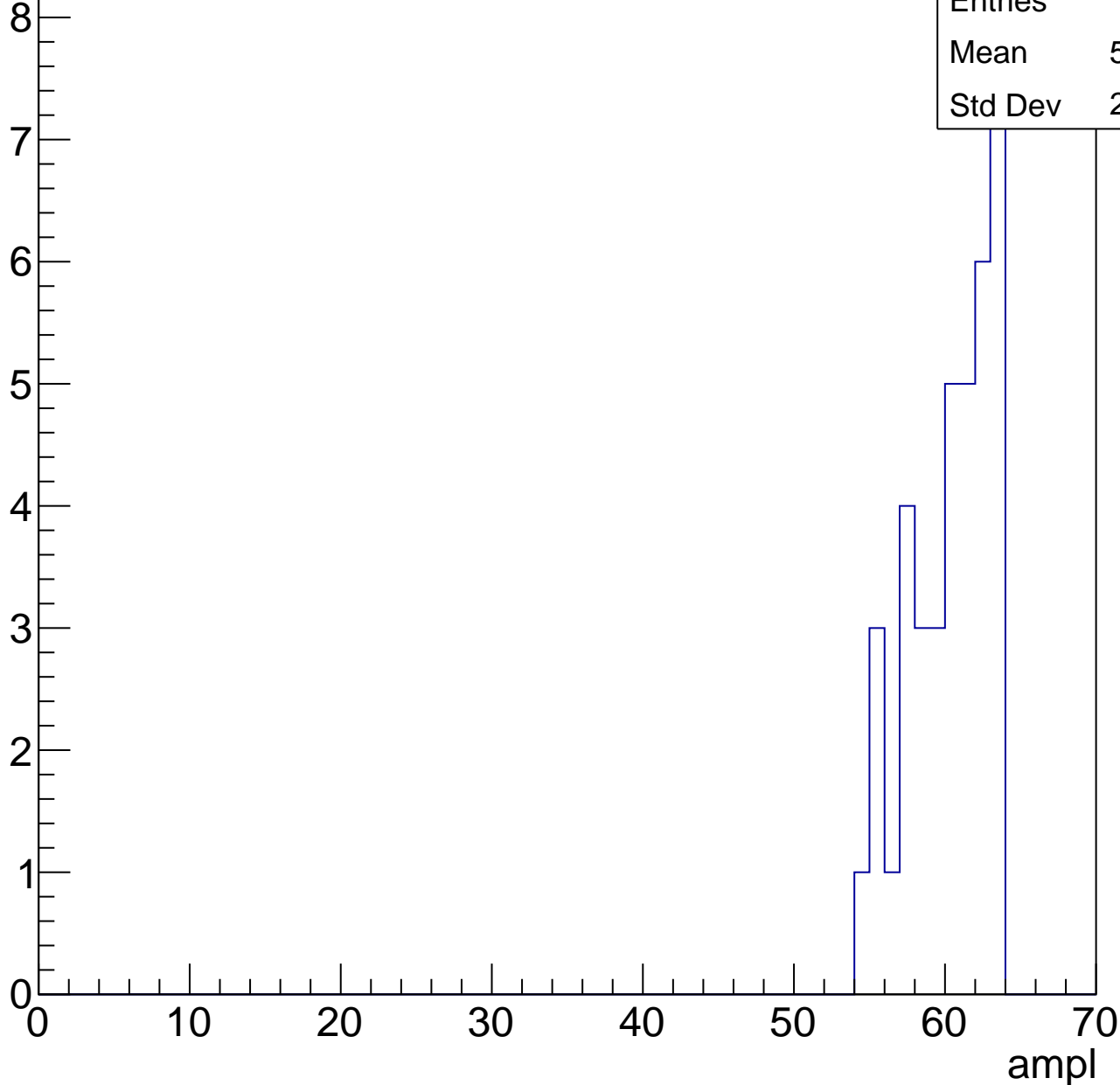


# B0L001S, U5-ch43, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

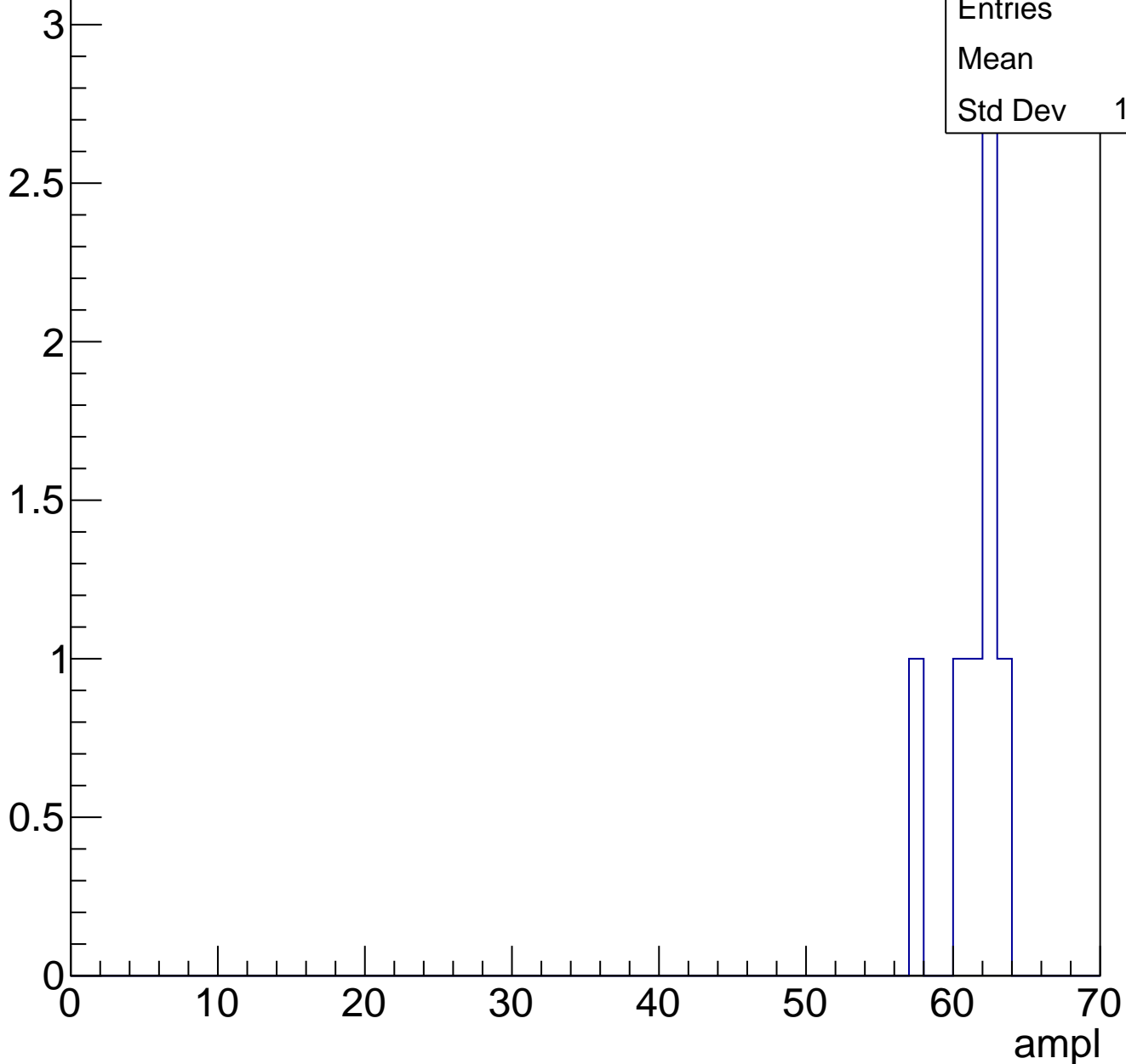
Entries	39
Mean	59.87
Std Dev	2.672



# B0L001S, U5-ch43, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch43, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U5-ch44, adc0

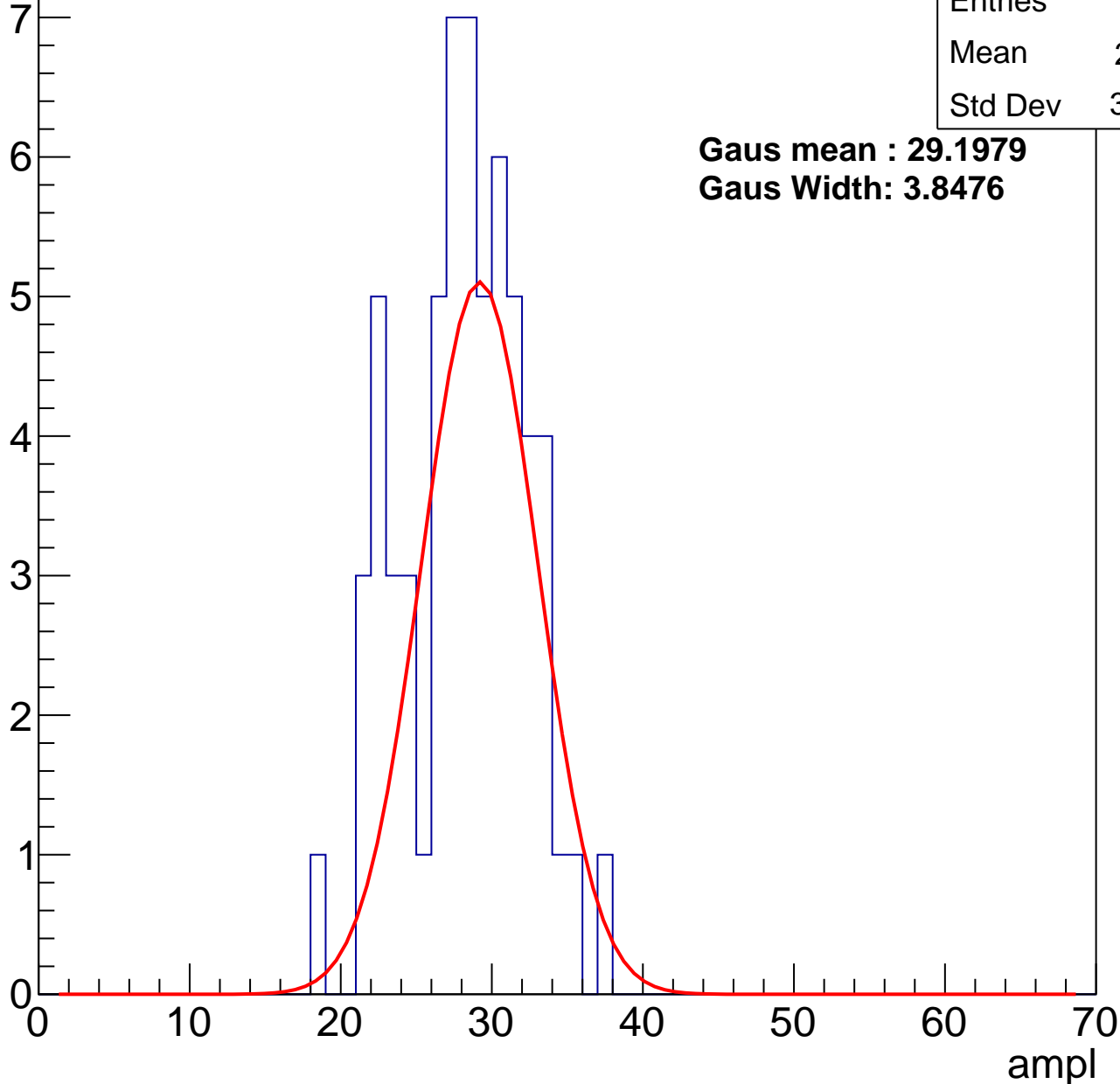
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	27.71
Std Dev	3.985

**Gaus mean : 29.1779**

**Gaus Width: 3.8476**



# B0L001S, U5-ch44, adc1

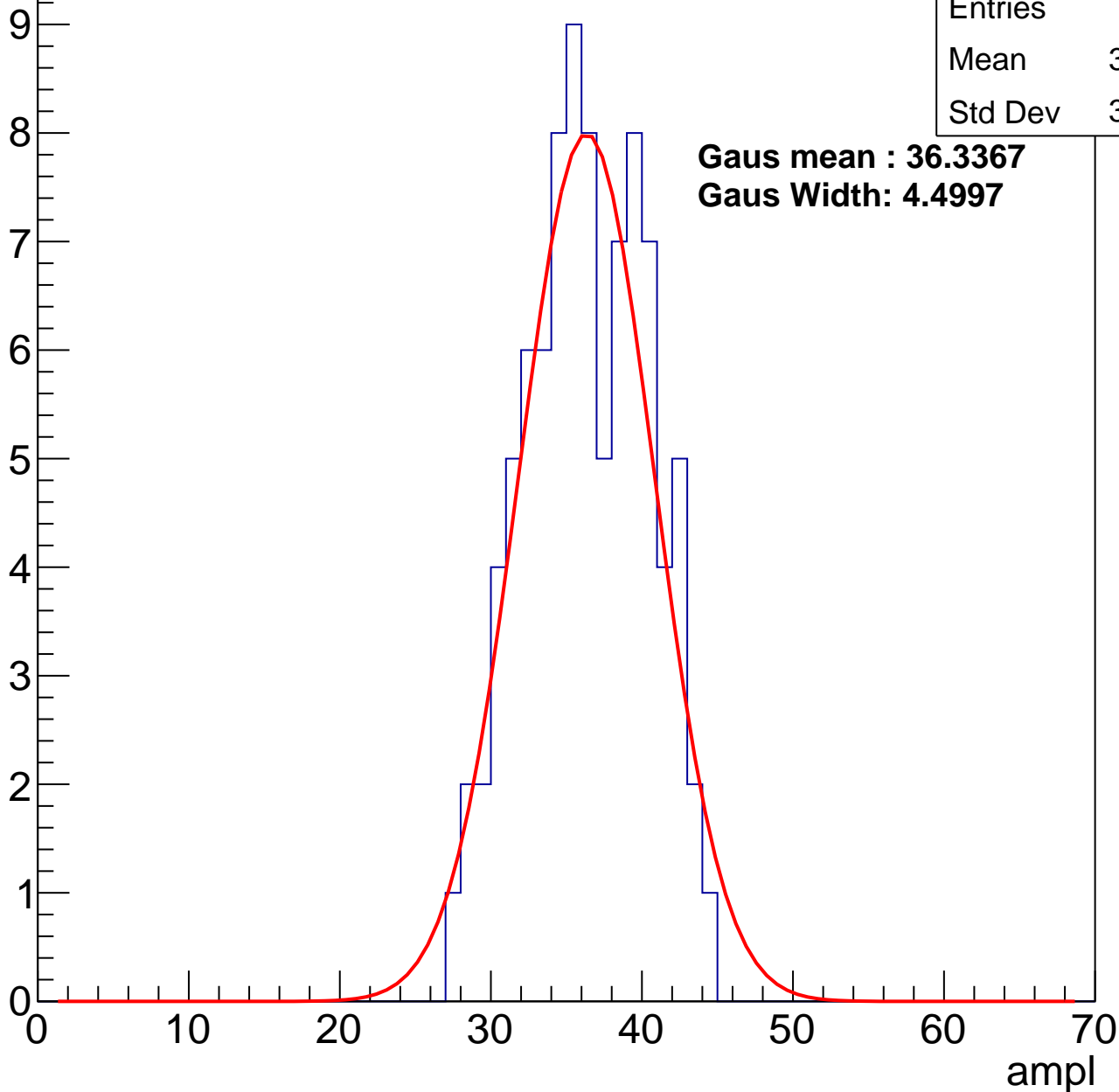
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	90
Mean	35.87
Std Dev	3.978

**Gaus mean : 36.3367**

**Gaus Width: 4.4997**



# B0L001S, U5-ch44, adc2

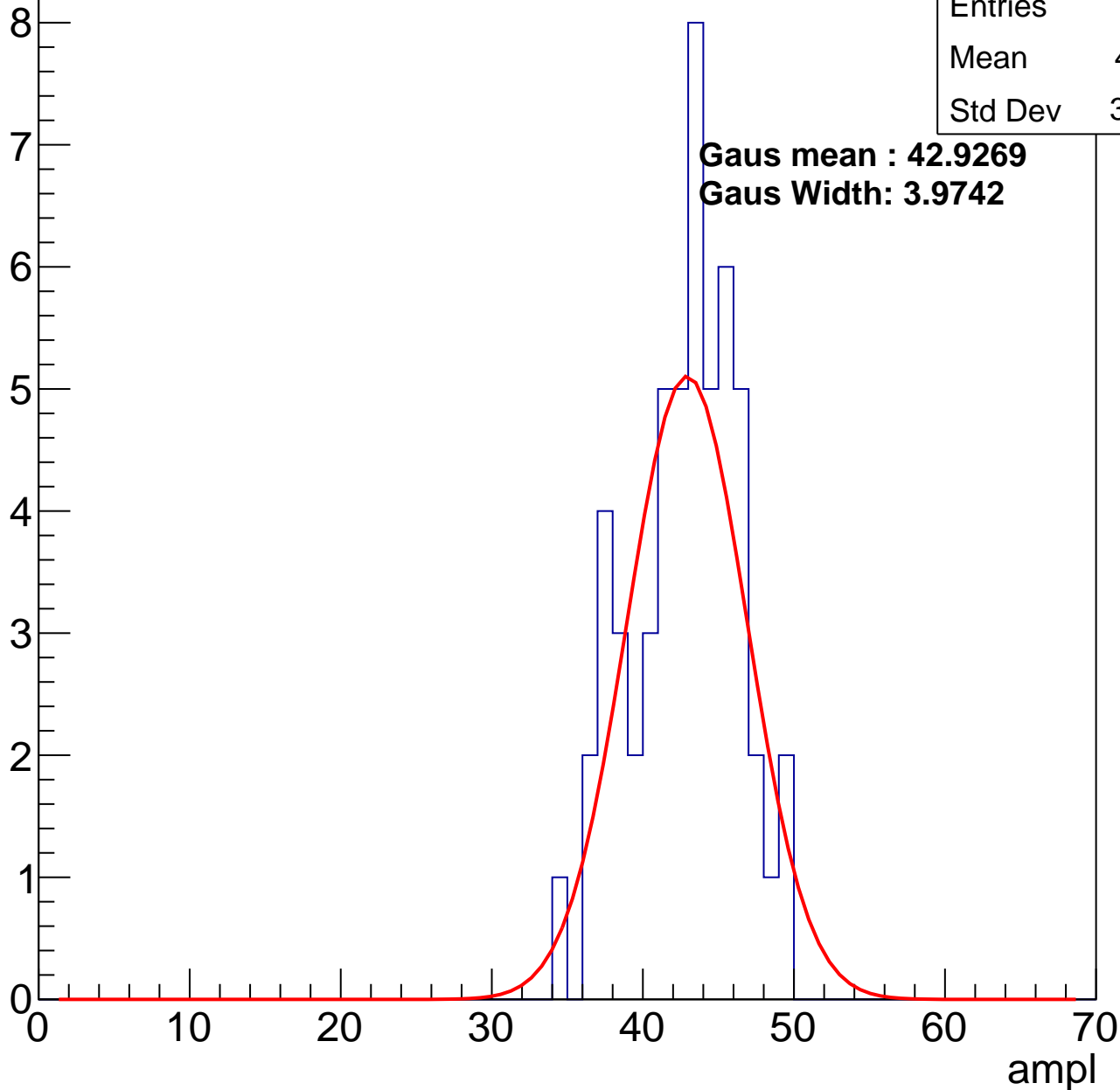
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	42.31
Std Dev	3.495

**Gaus mean : 42.9269**

**Gaus Width: 3.9742**

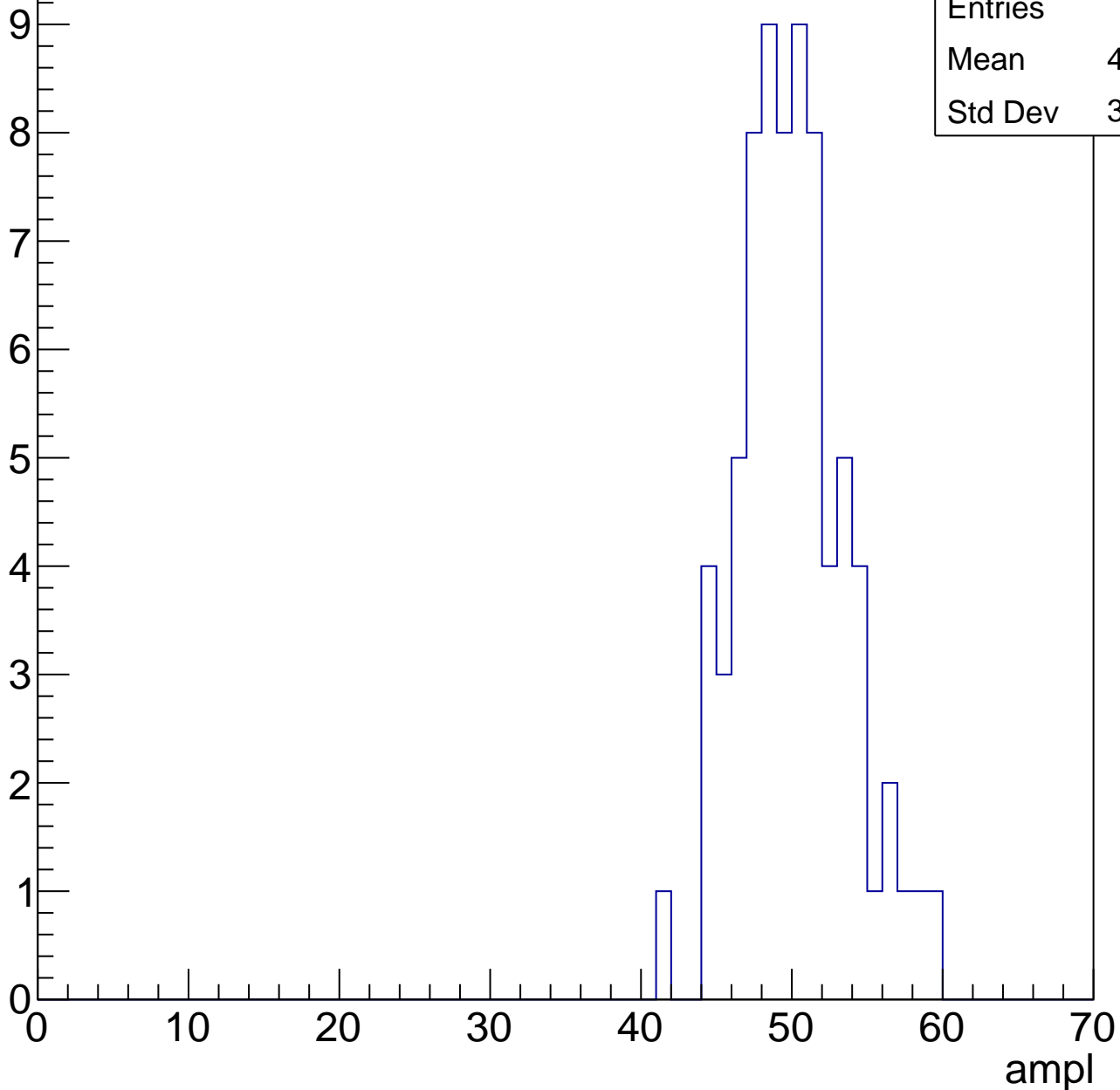


# B0L001S, U5-ch44, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	49.59
Std Dev	3.503



# B0L001S, U5-ch44, adc4

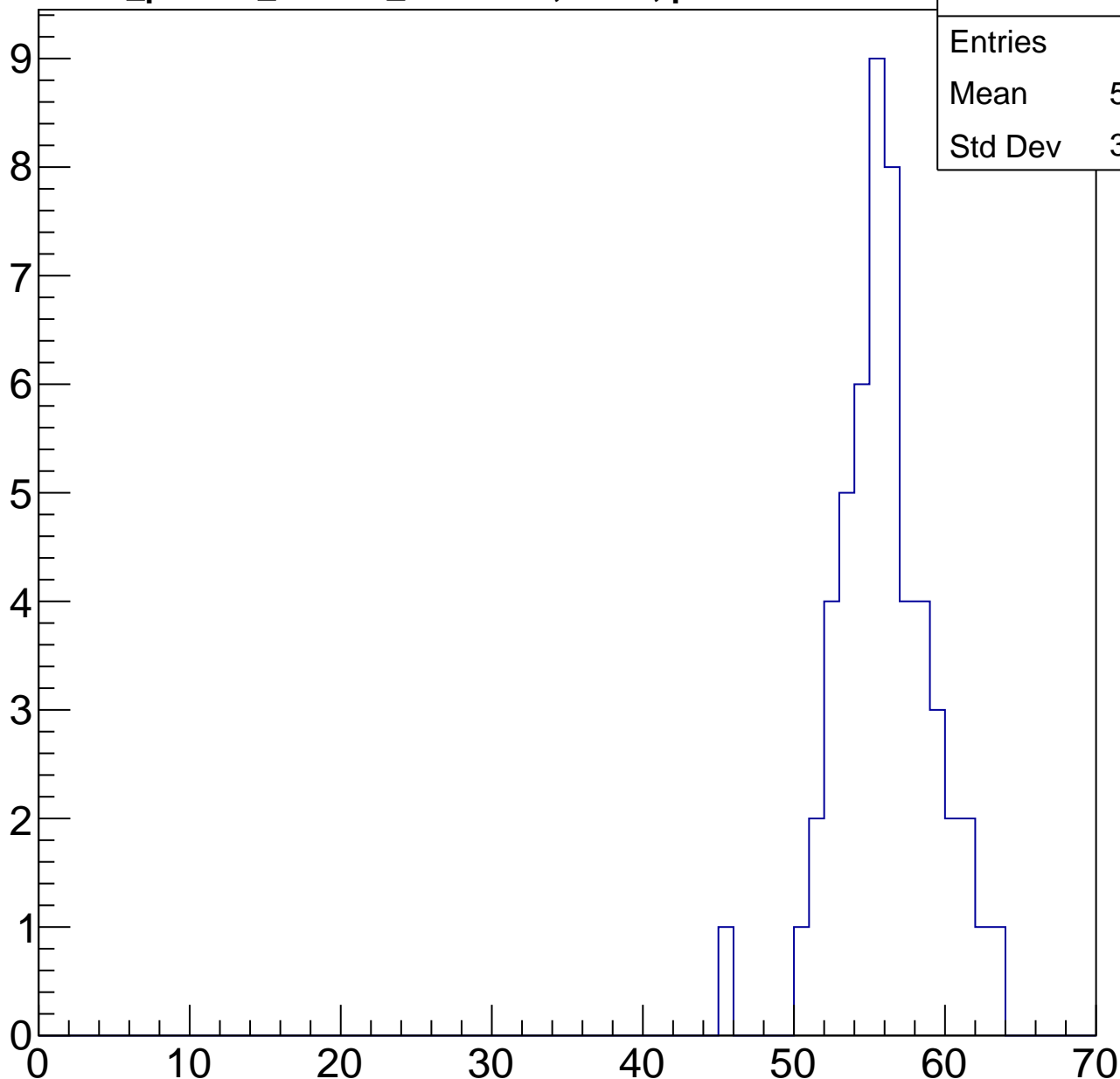
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	53
Mean	55.49
Std Dev	3.219

ampl

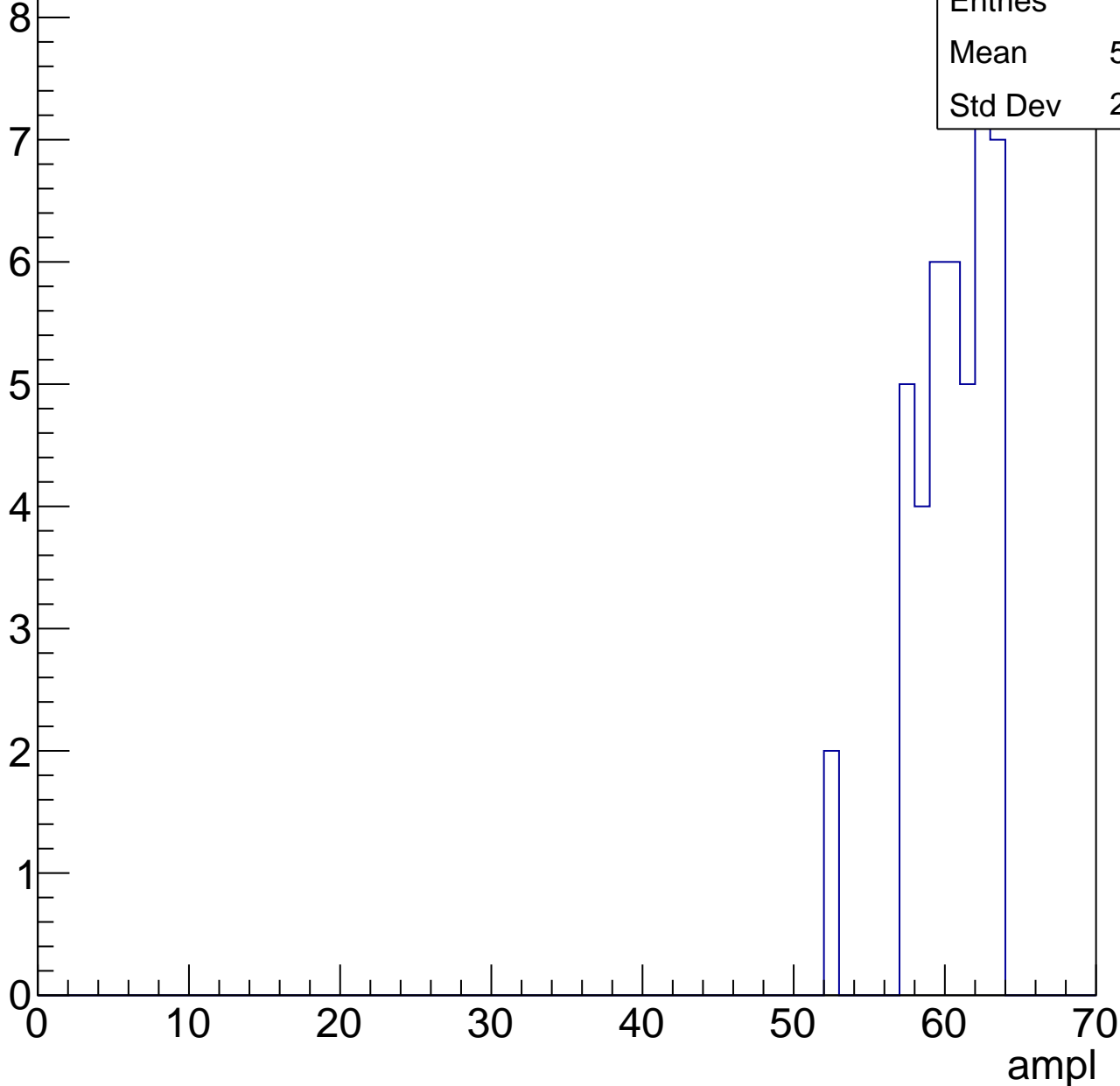


# B0L001S, U5-ch44, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

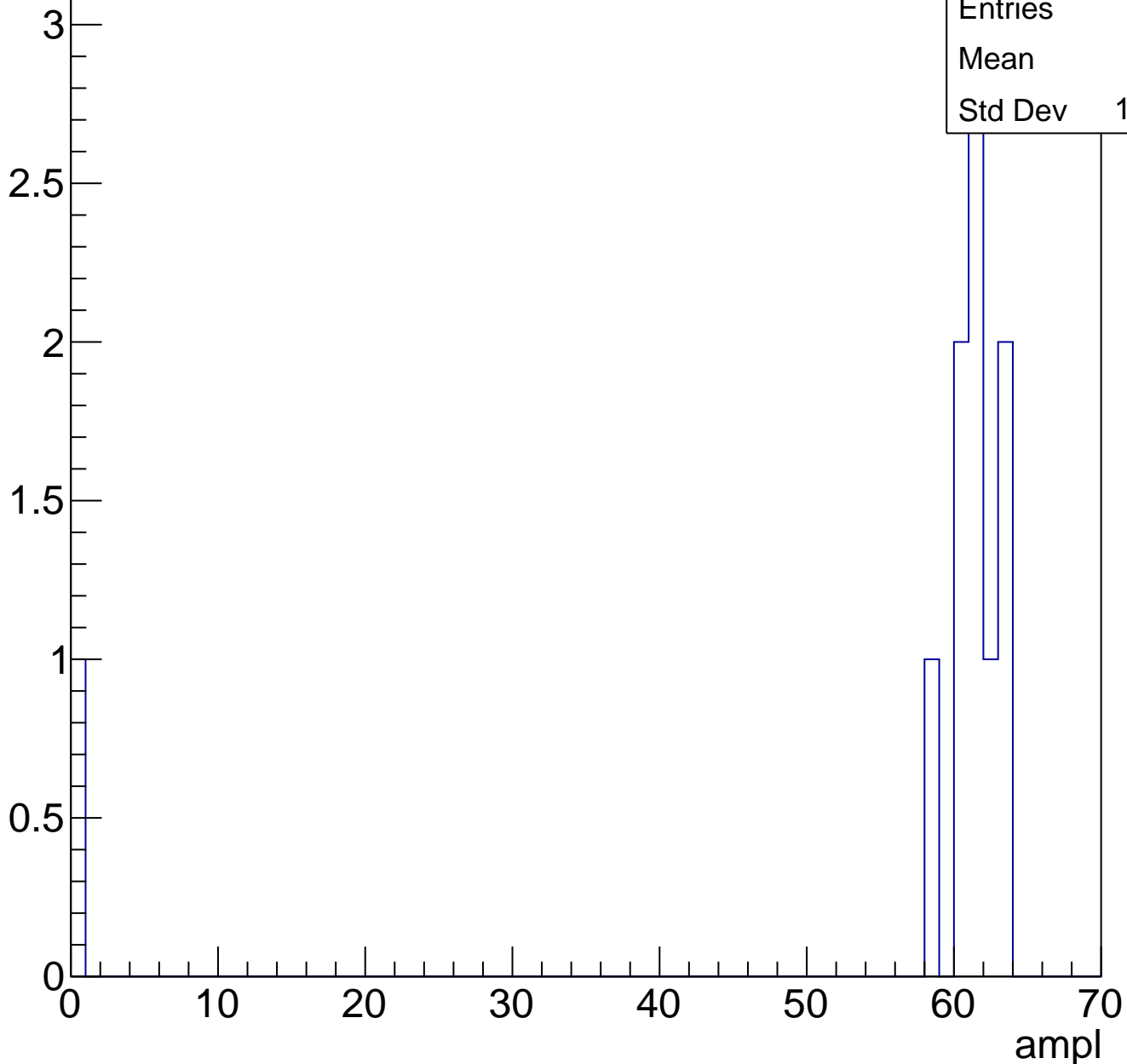
Entries	43
Mean	59.93
Std Dev	2.618



# B0L001S, U5-ch44, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch44, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U5-ch45, adc0

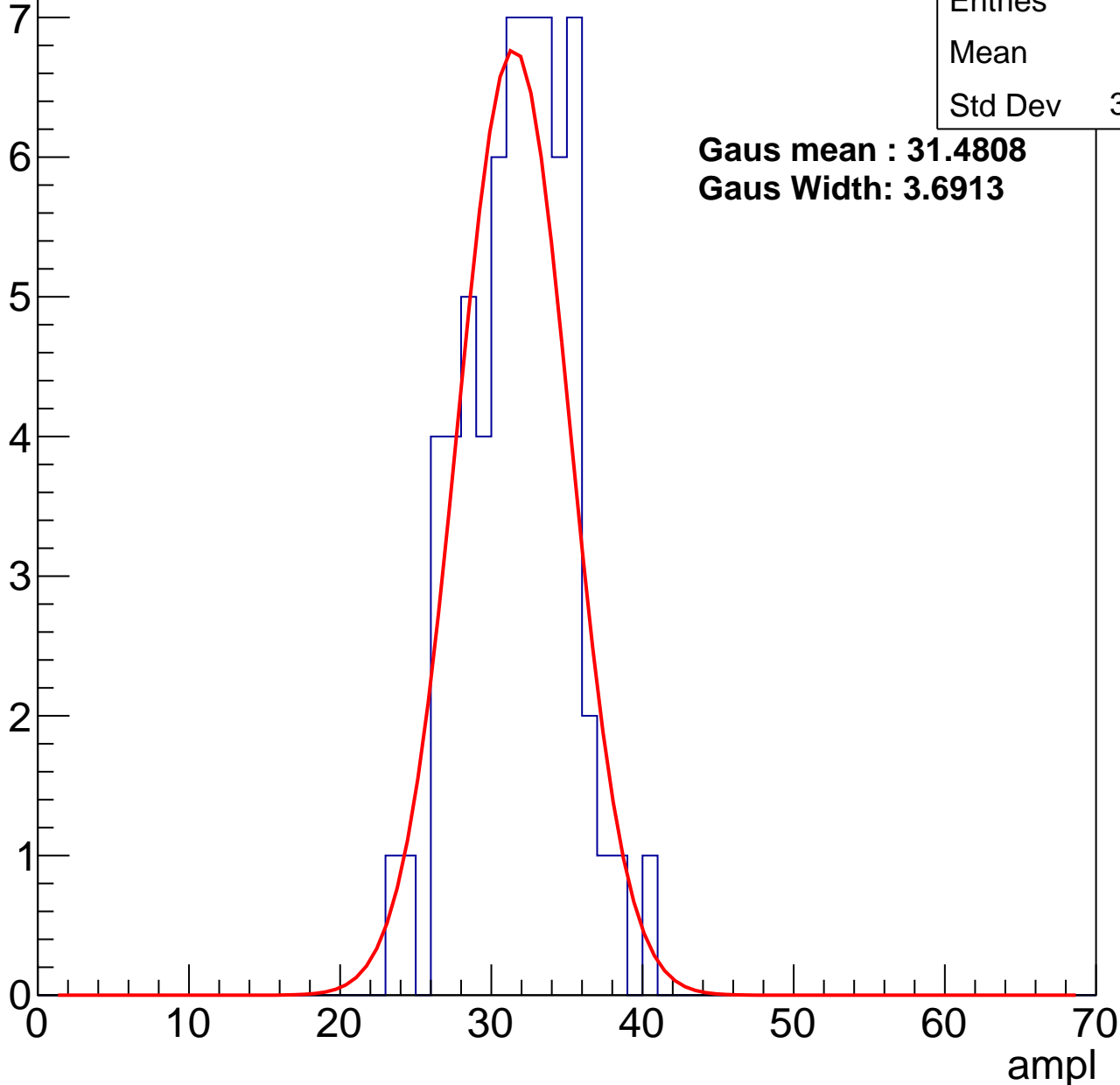
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	31.3
Std Dev	3.435

**Gaus mean : 31.4808**

**Gaus Width: 3.6913**



# B0L001S, U5-ch45, adc1

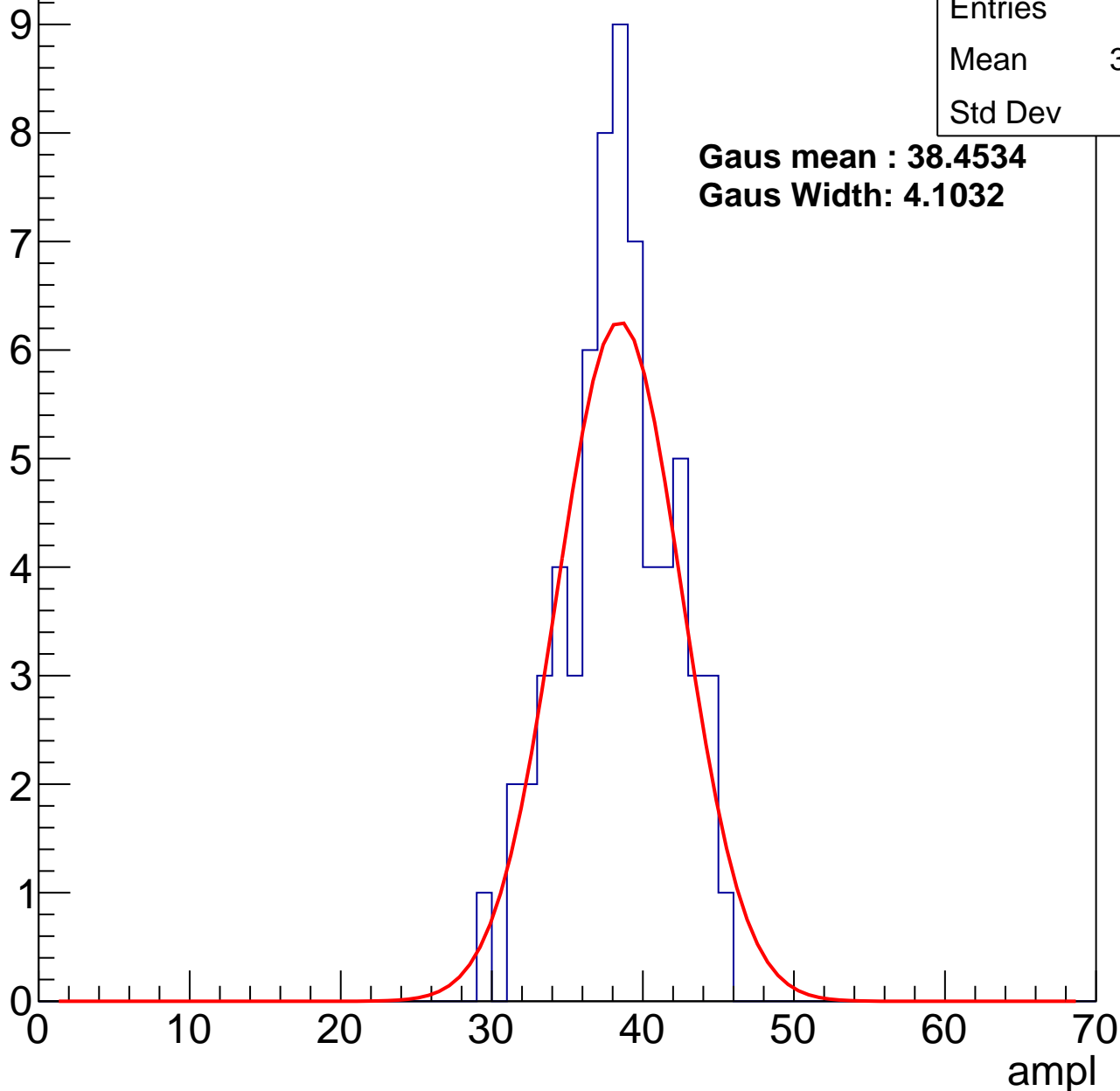
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	37.88
Std Dev	3.55

**Gaus mean : 38.4534**

**Gaus Width: 4.1032**



# B0L001S, U5-ch45, adc2

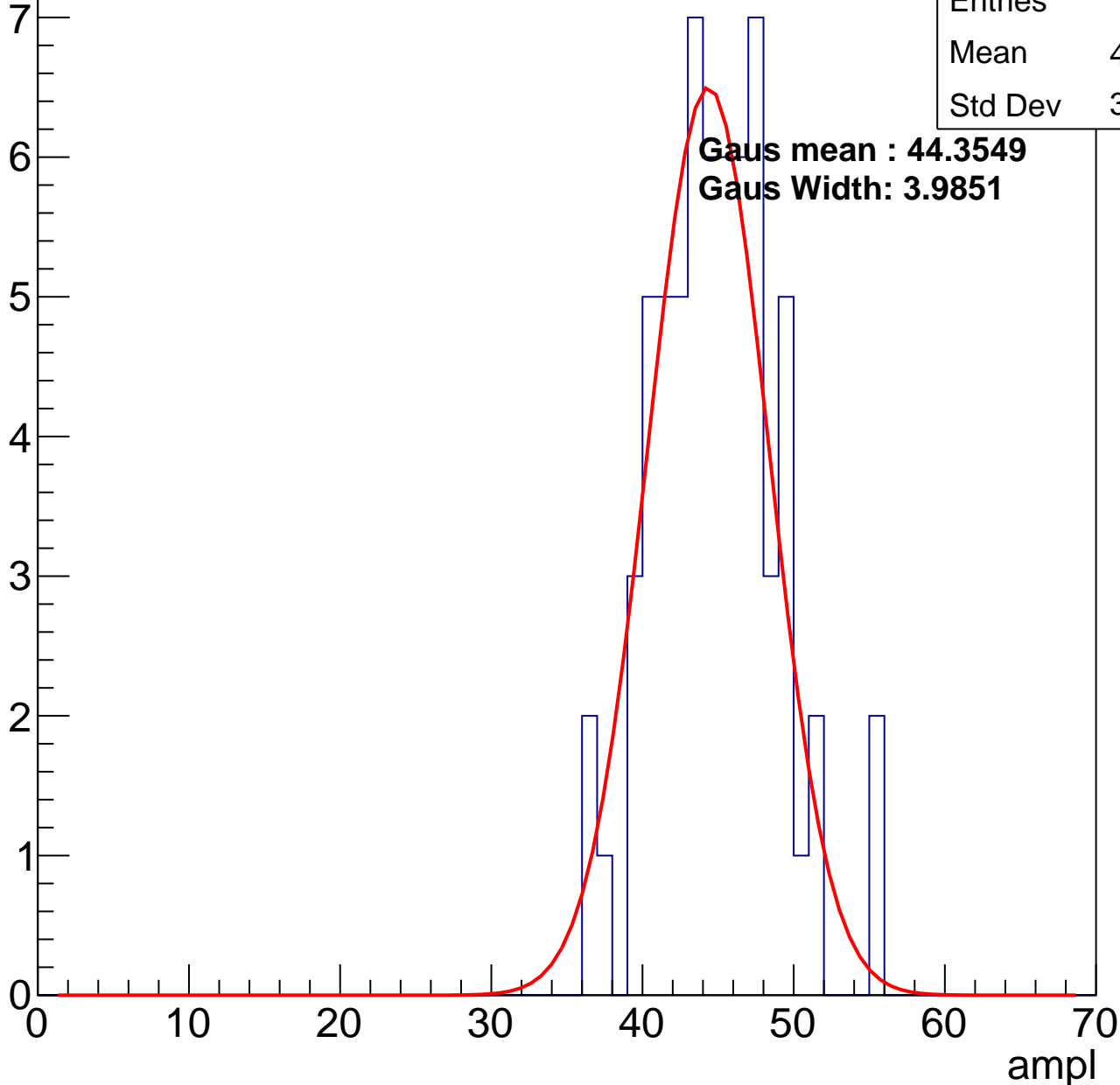
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	44.42
Std Dev	3.958

**Gaus mean : 44.3549**

**Gaus Width: 3.9851**

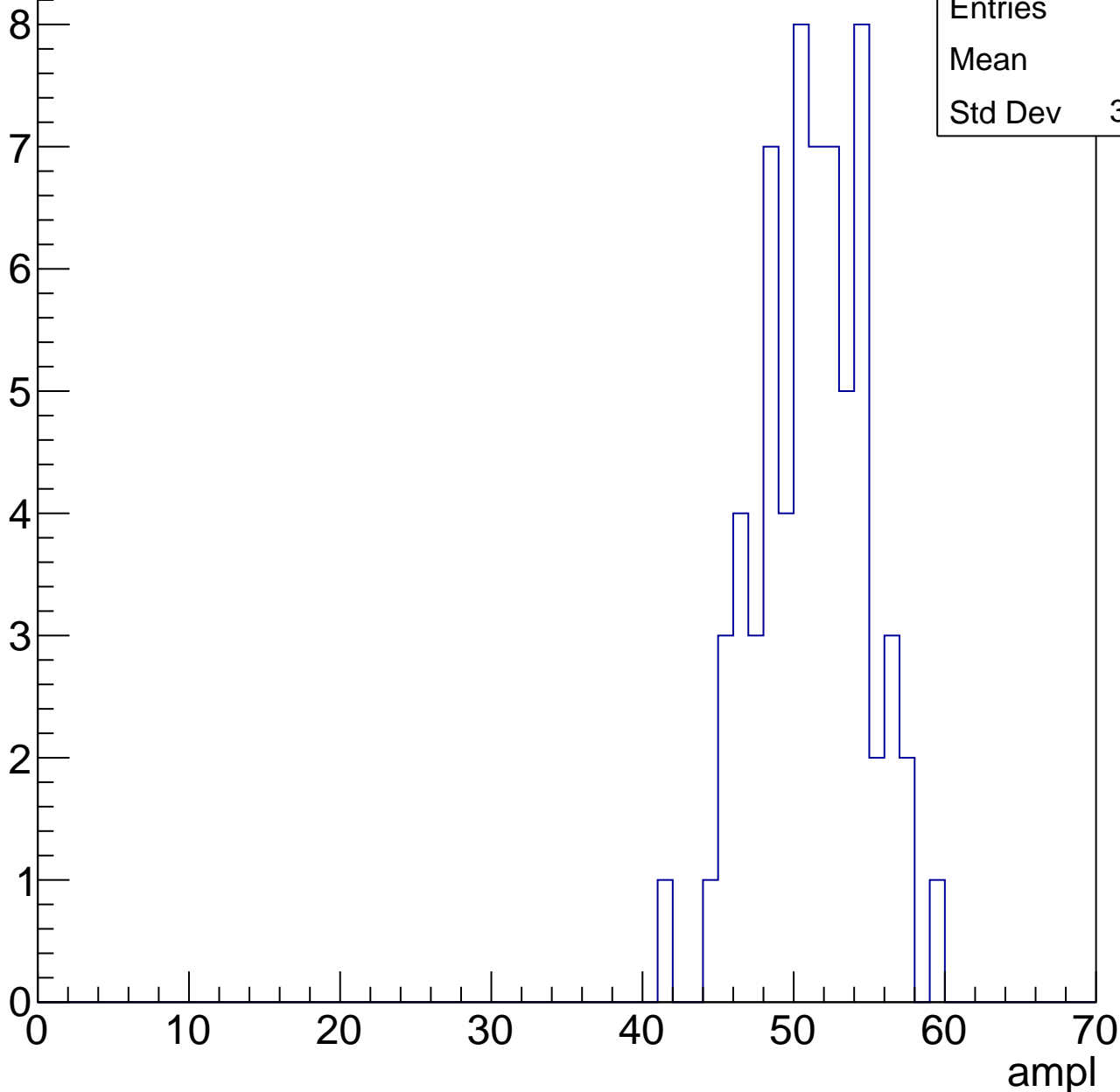


# B0L001S, U5-ch45, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

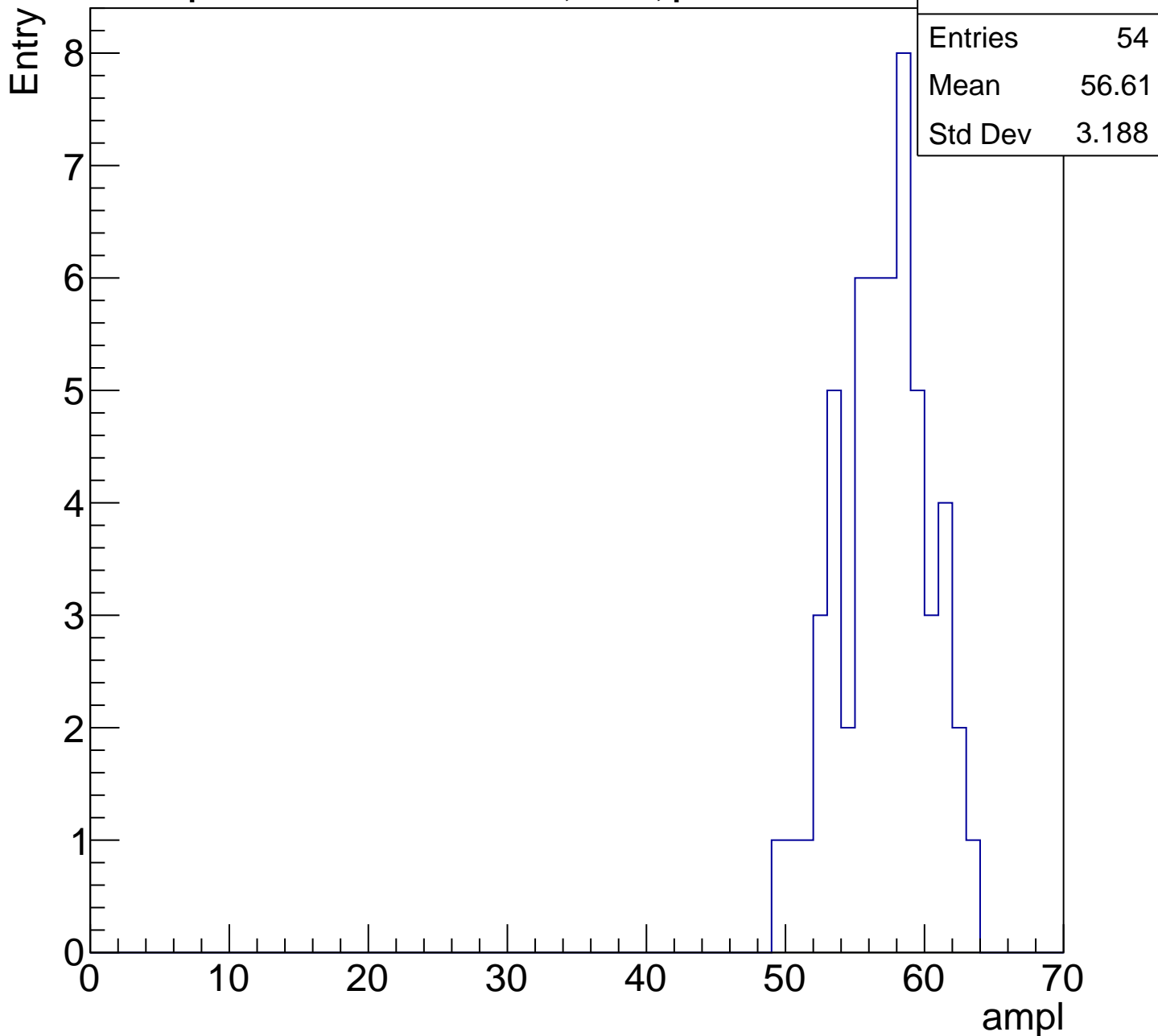
Entry

Entries	66
Mean	50.7
Std Dev	3.542



# B0L001S, U5-ch45, adc4

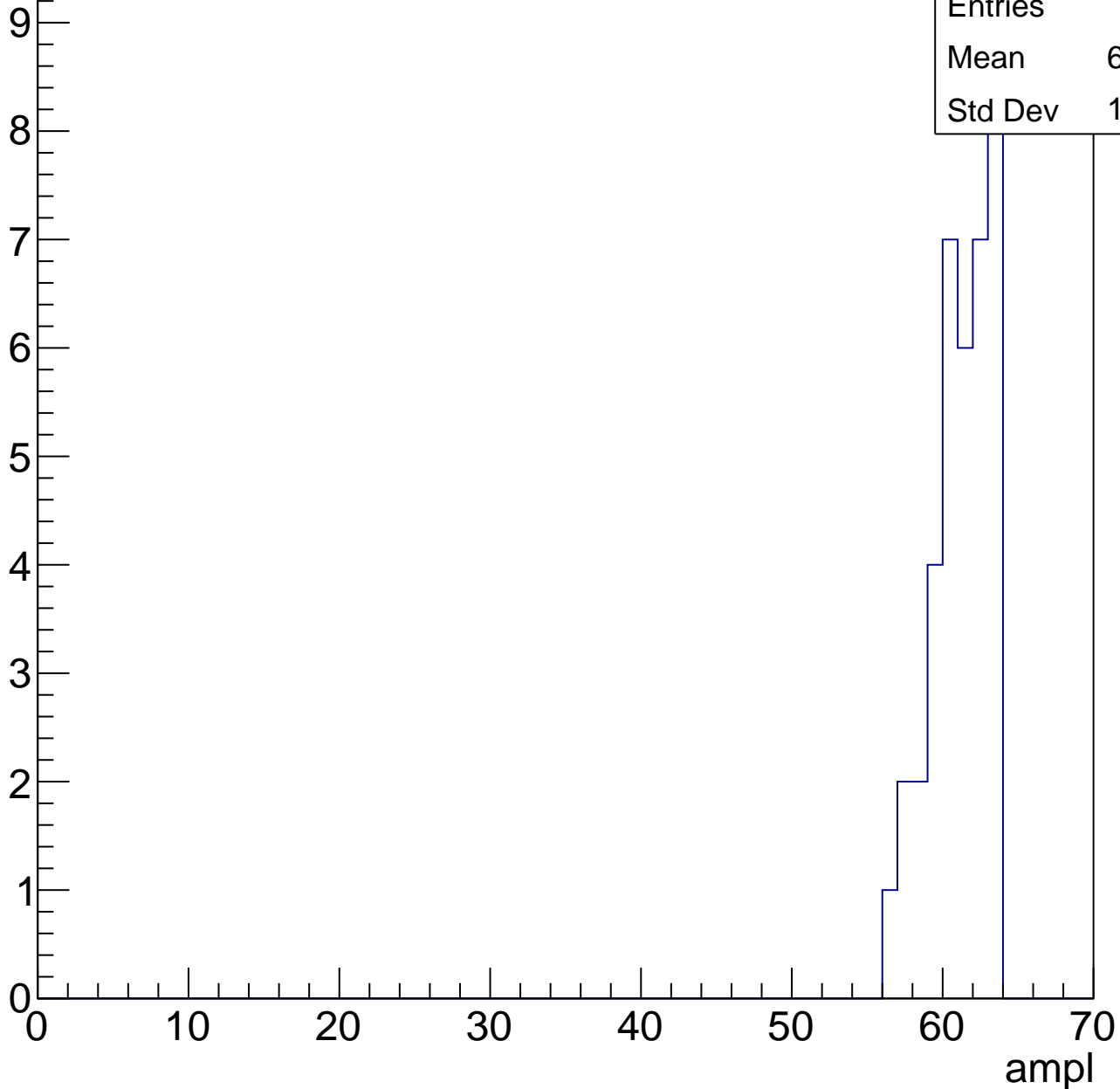
calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U5-ch45, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

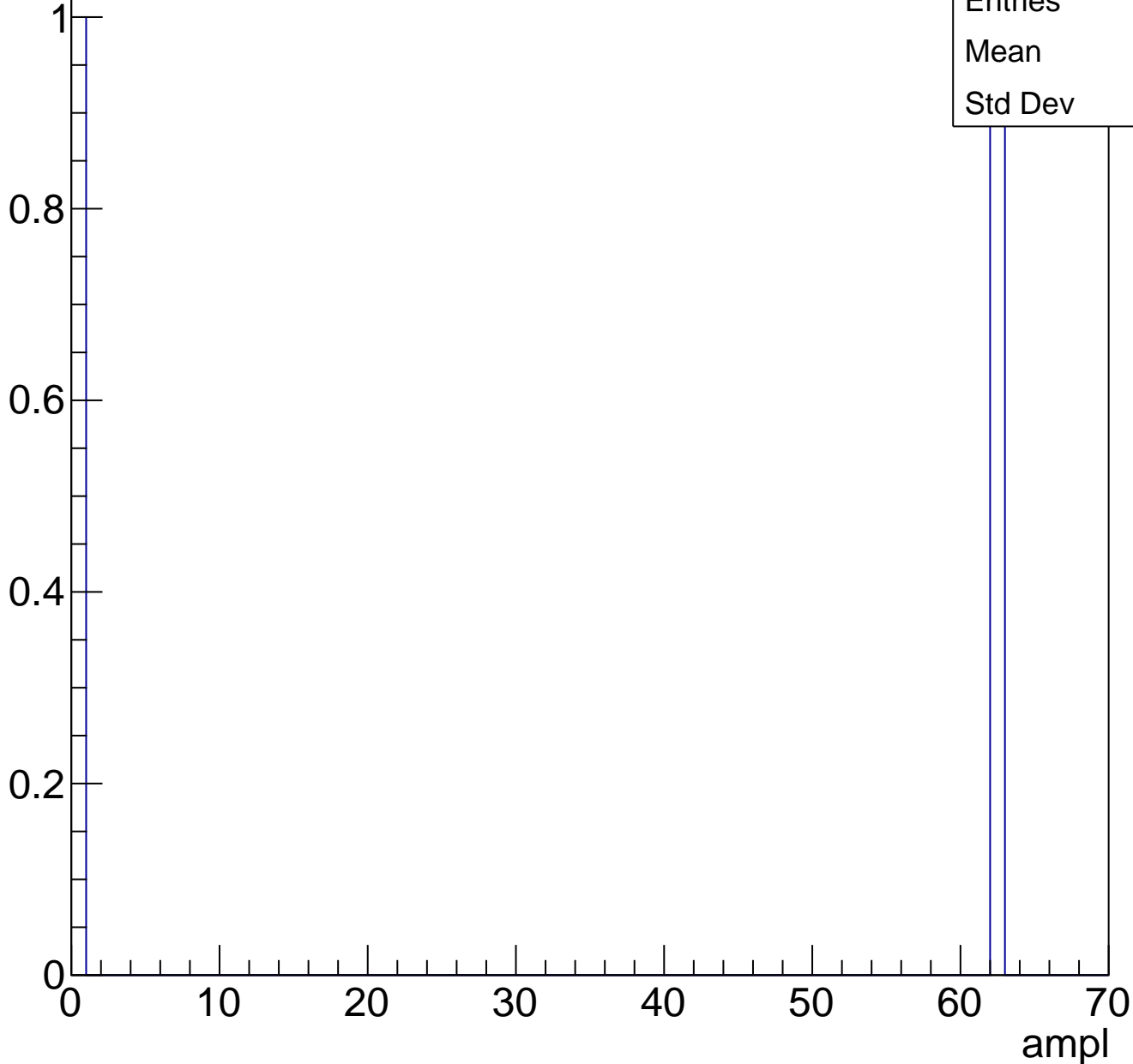
Entry



# B0L001S, U5-ch45, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch45, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch46, adc0

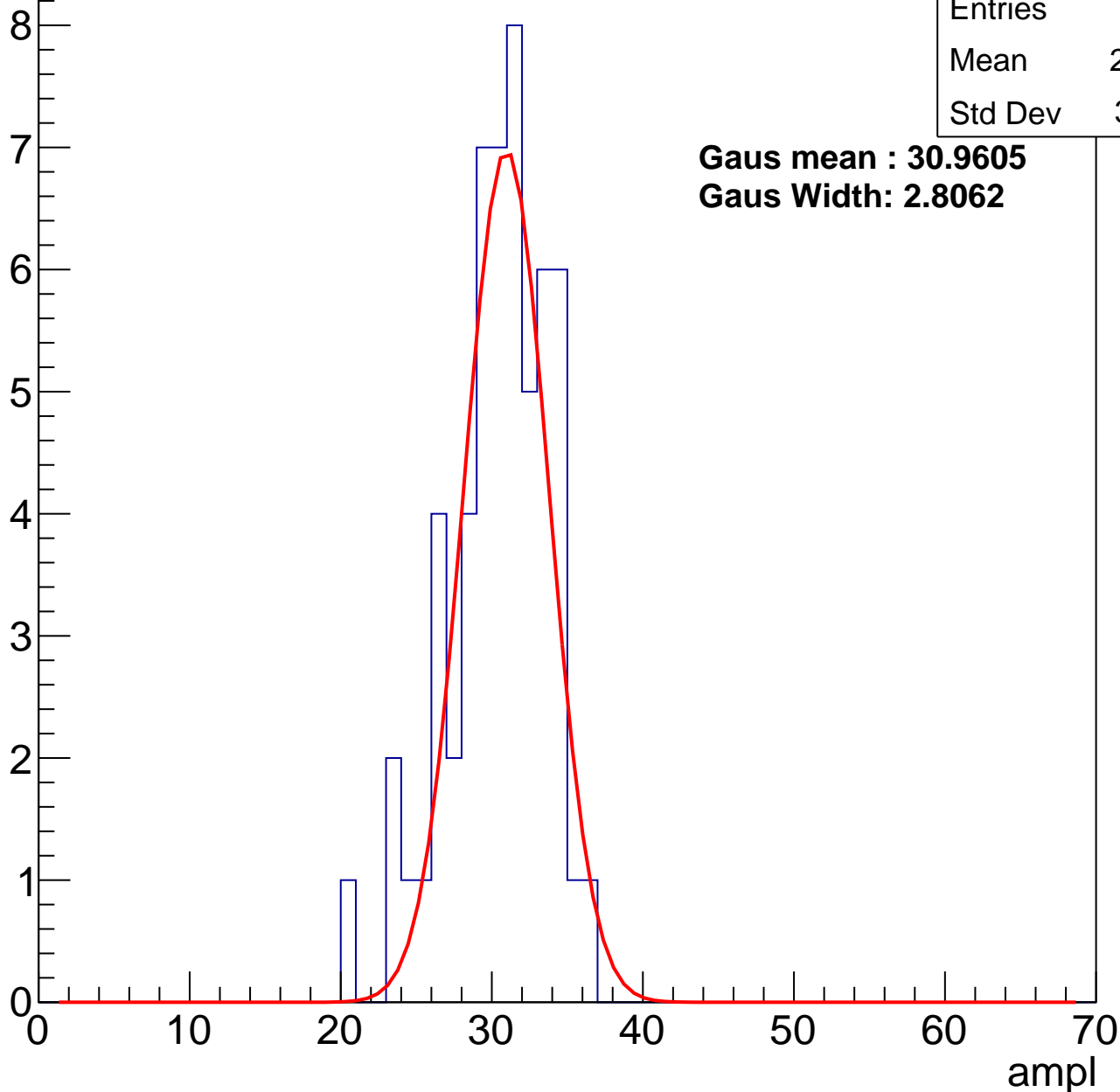
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	29.98
Std Dev	3.281

**Gaus mean : 30.9605**

**Gaus Width: 2.8062**



# B0L001S, U5-ch46, adc1

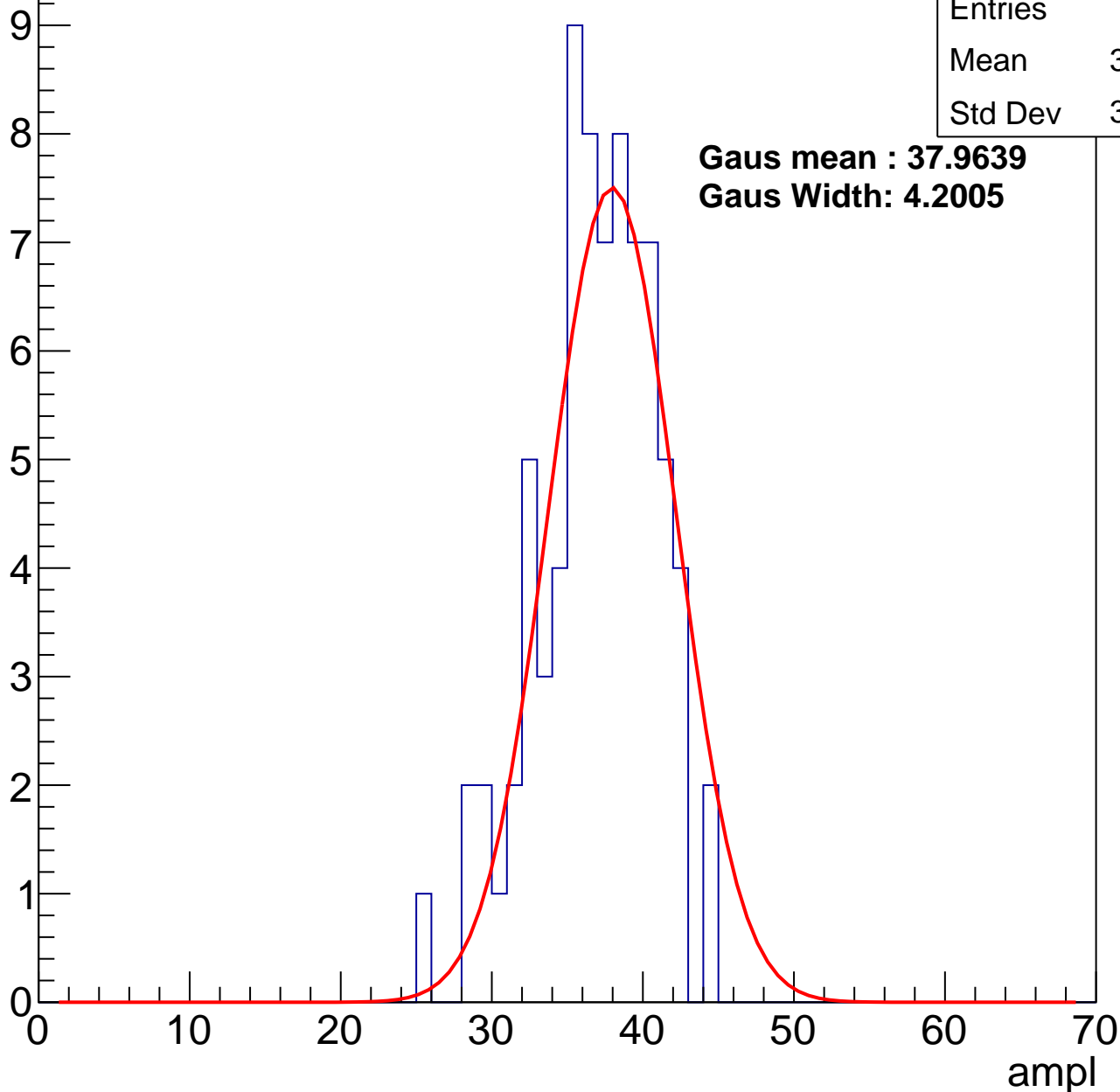
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	77
Mean	36.44
Std Dev	3.883

**Gaus mean : 37.9639**

**Gaus Width: 4.2005**



# B0L001S, U5-ch46, adc2

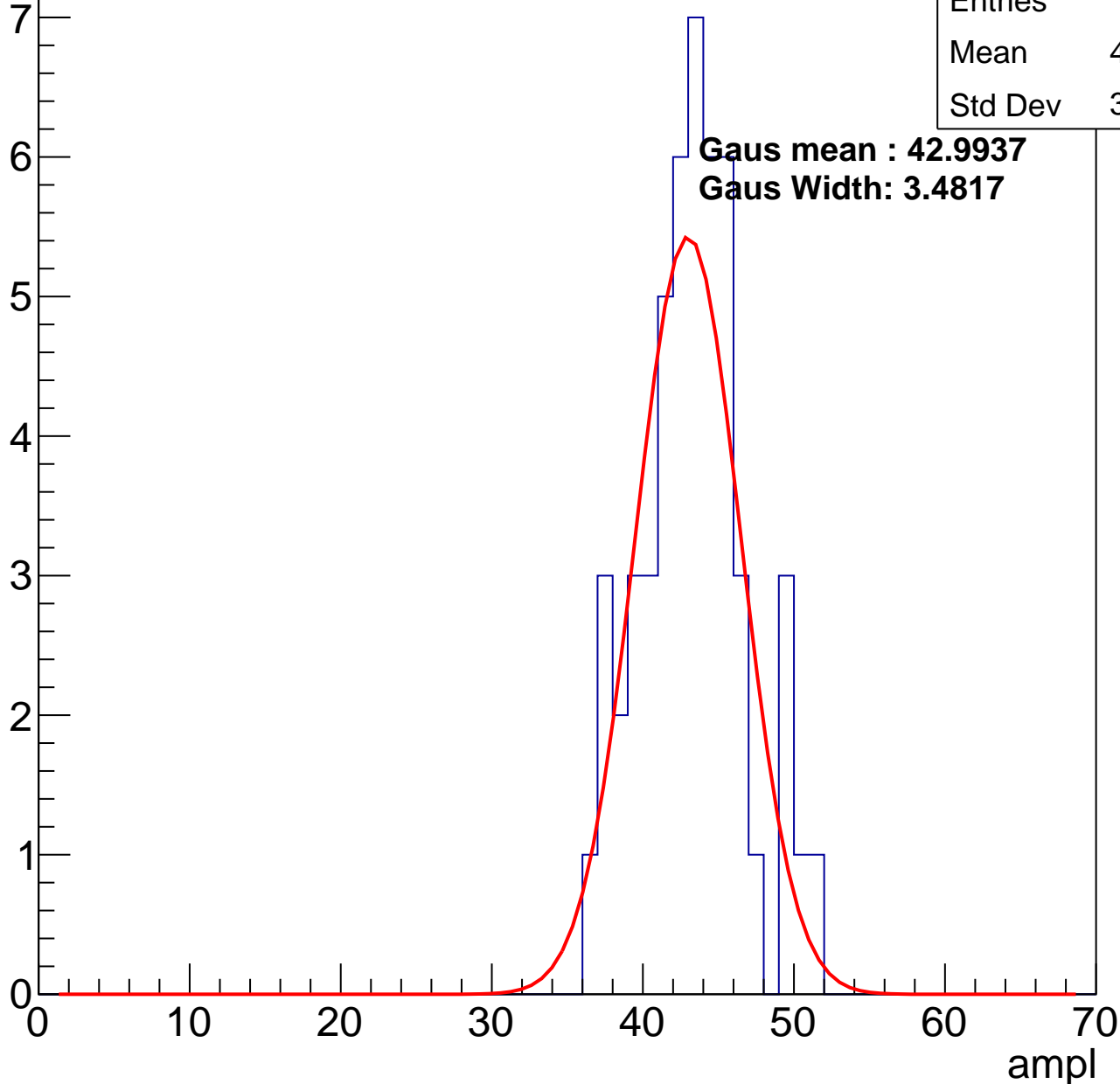
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	51
Mean	42.84
Std Dev	3.432

**Gaus mean : 42.9937**

**Gaus Width: 3.4817**

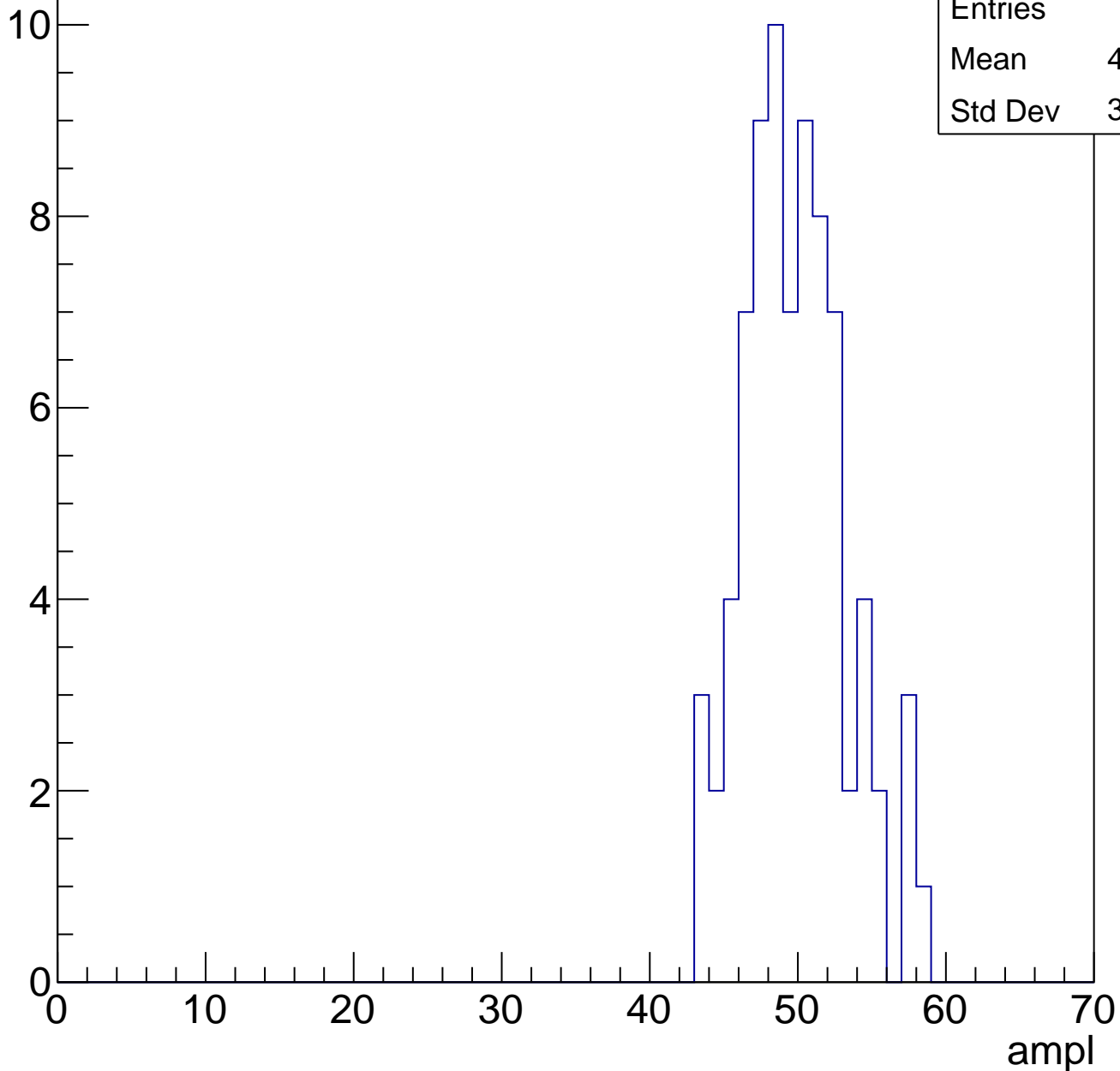


# B0L001S, U5-ch46, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

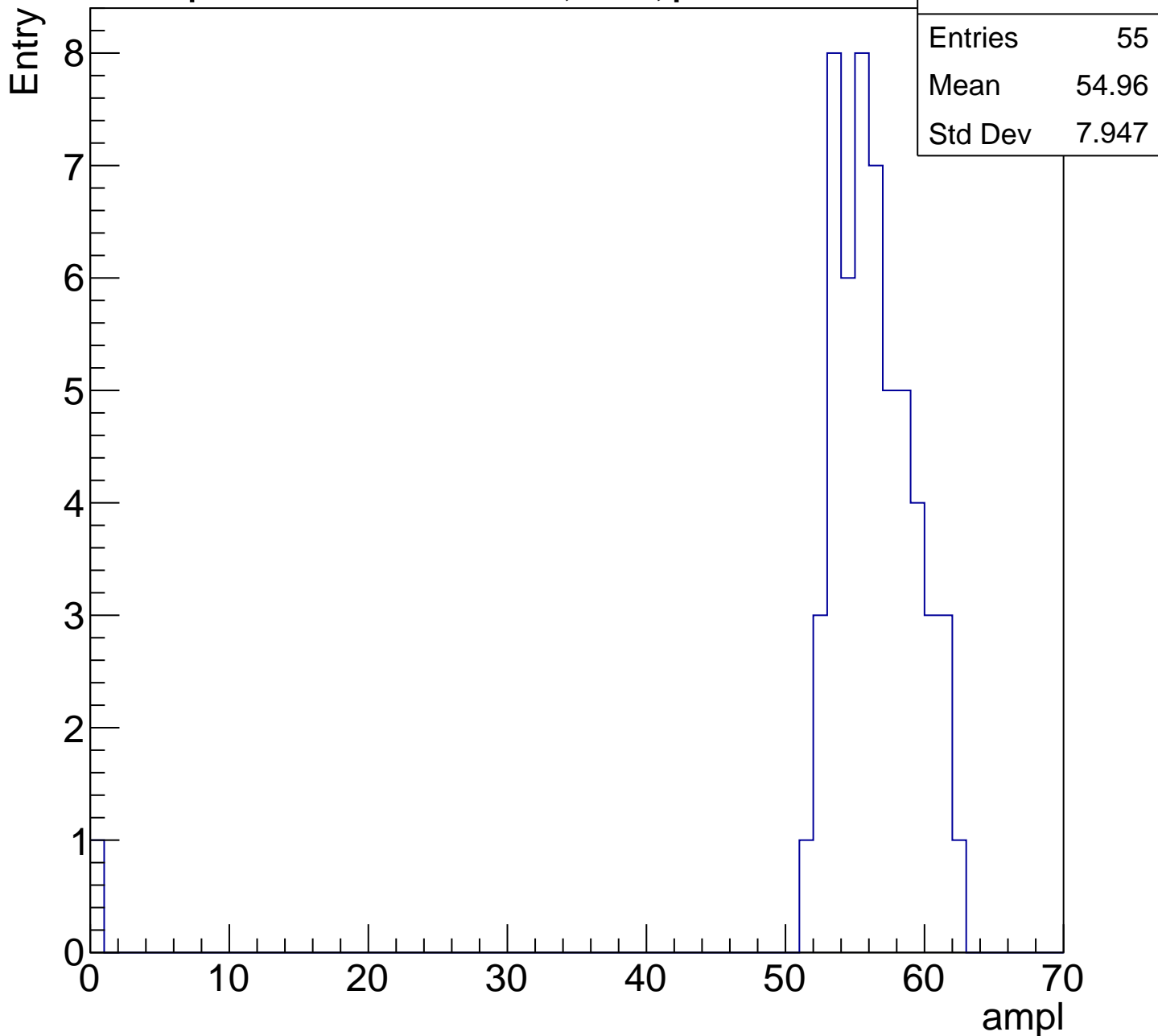
Entries	78
Mean	49.33
Std Dev	3.403

Entry



# B0L001S, U5-ch46, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

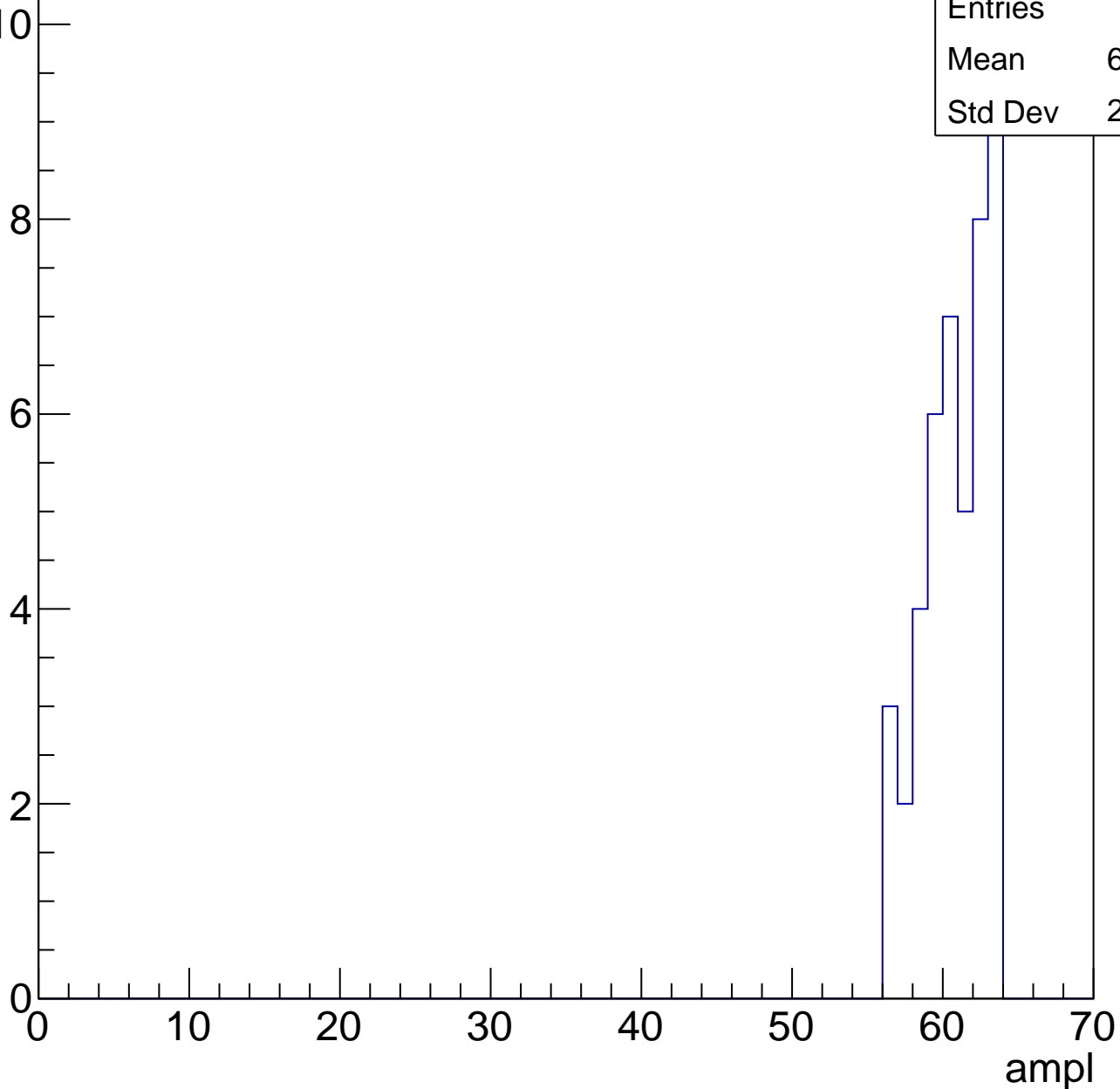


# B0L001S, U5-ch46, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

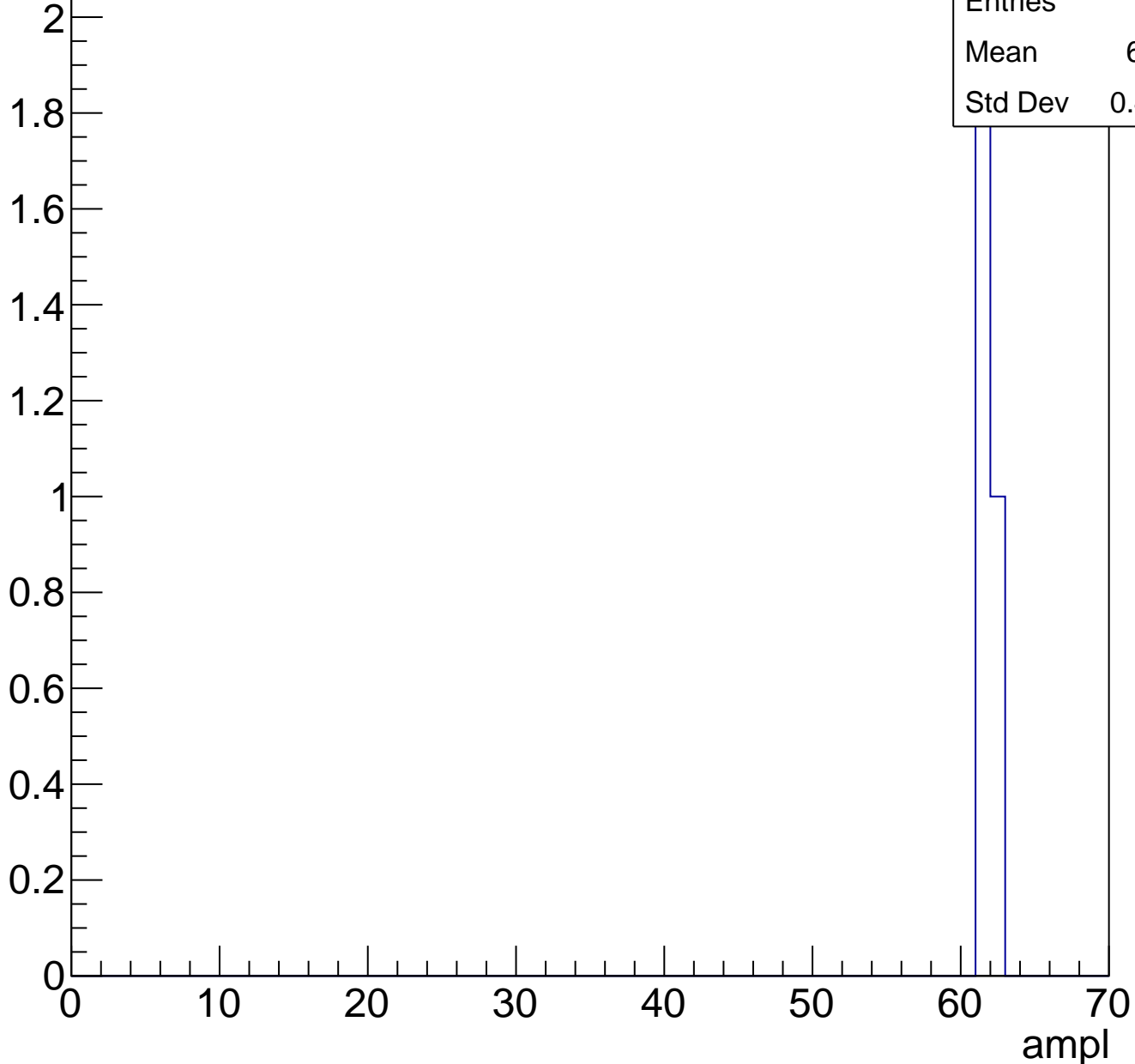
Entries	45
Mean	60.42
Std Dev	2.145



# B0L001S, U5-ch46, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch46, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch47, adc0

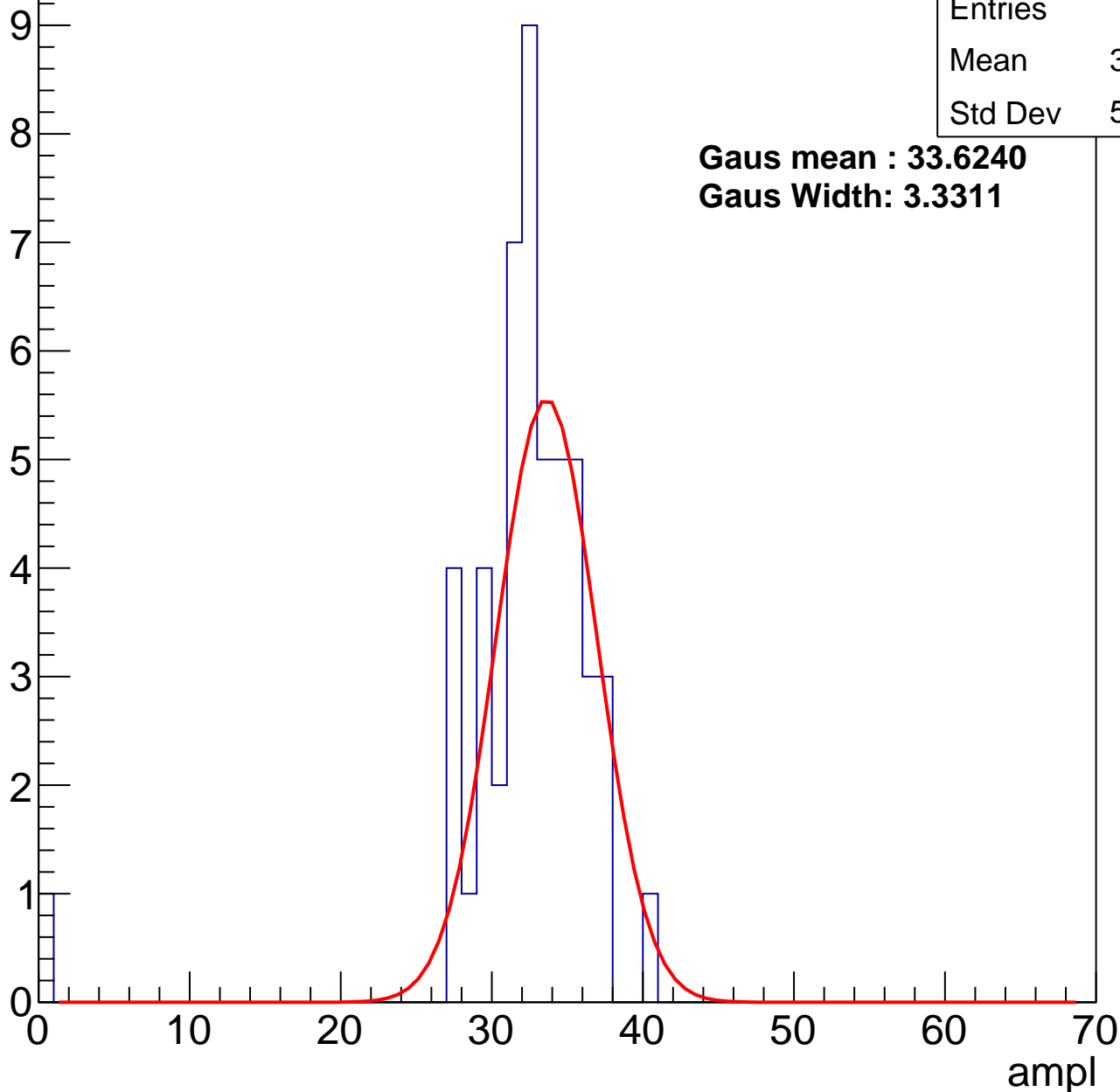
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	50
Mean	31.72
Std Dev	5.374

**Gaus mean : 33.6240**

**Gaus Width: 3.3311**



# B0L001S, U5-ch47, adc1

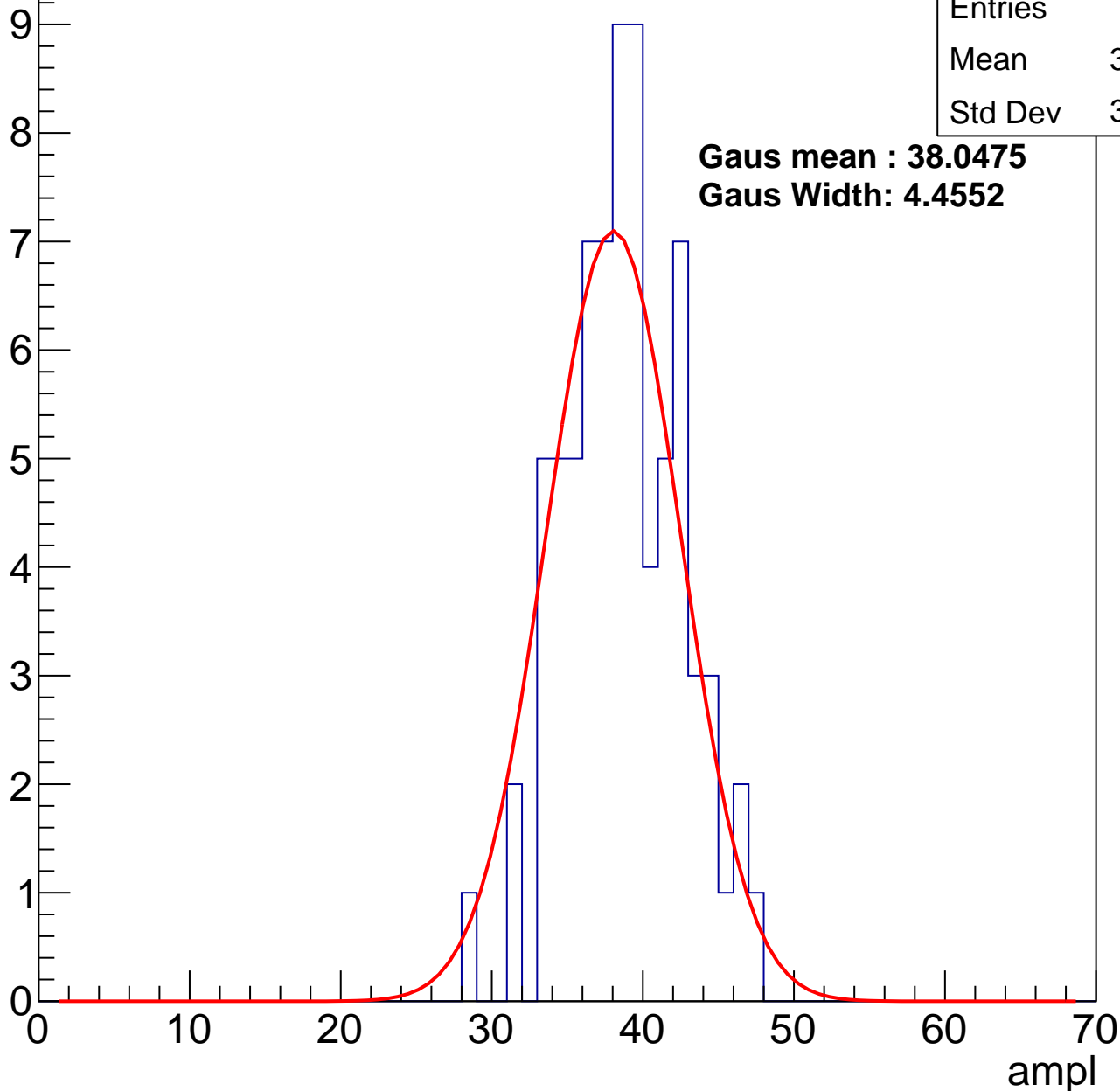
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	76
Mean	38.26
Std Dev	3.806

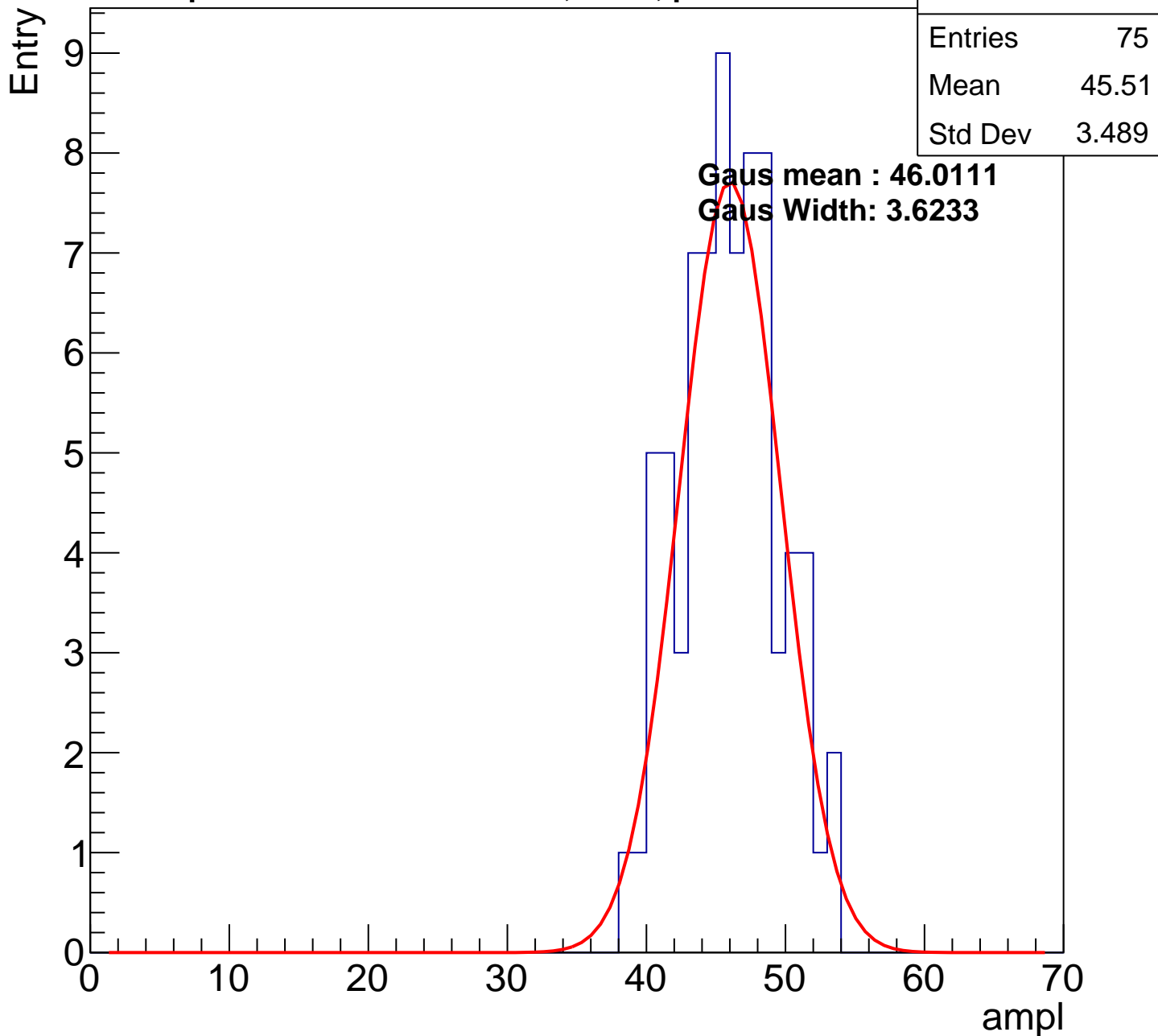
**Gaus mean : 38.0475**

**Gaus Width: 4.4552**



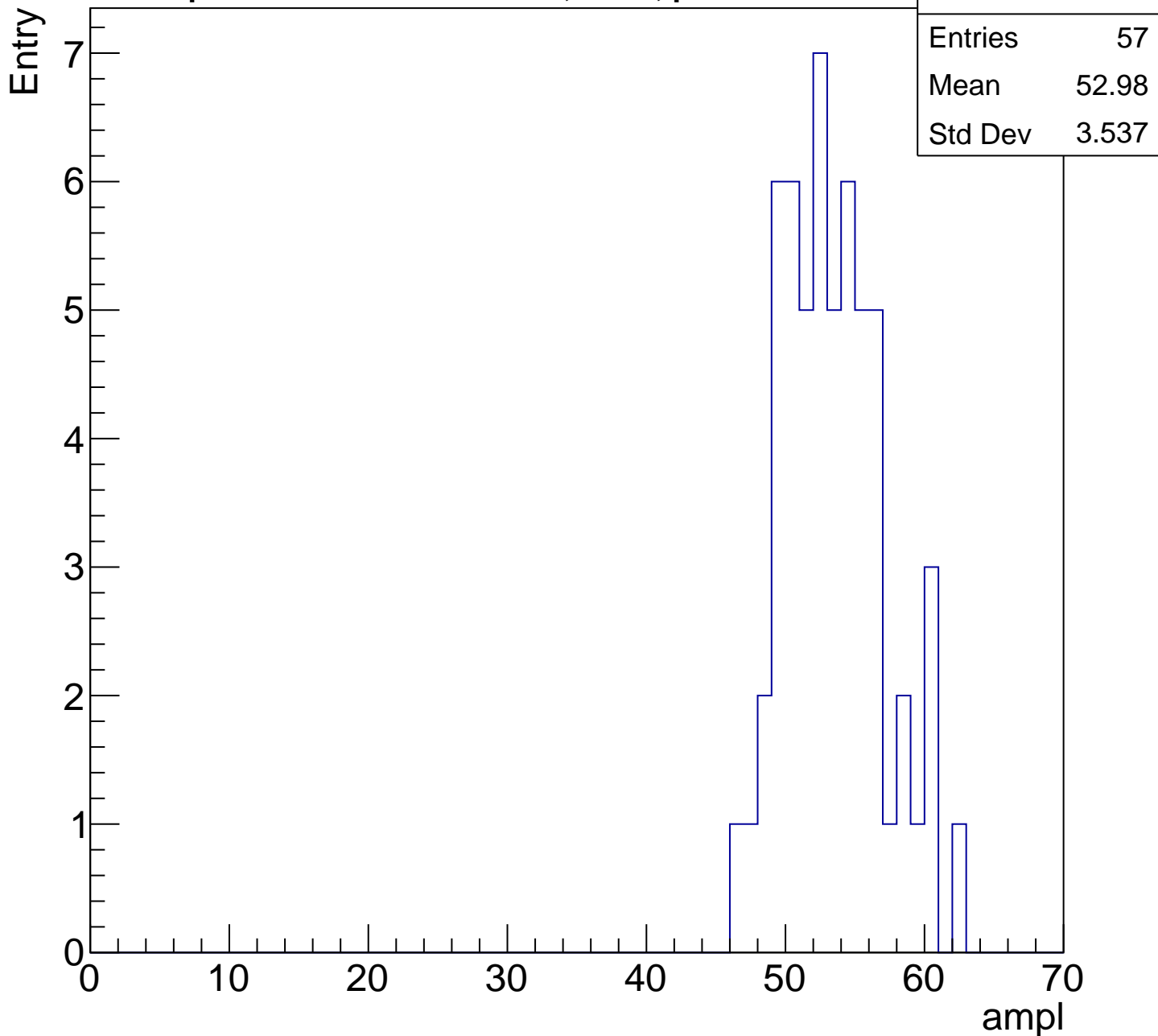
# B0L001S, U5-ch47, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U5-ch47, adc3

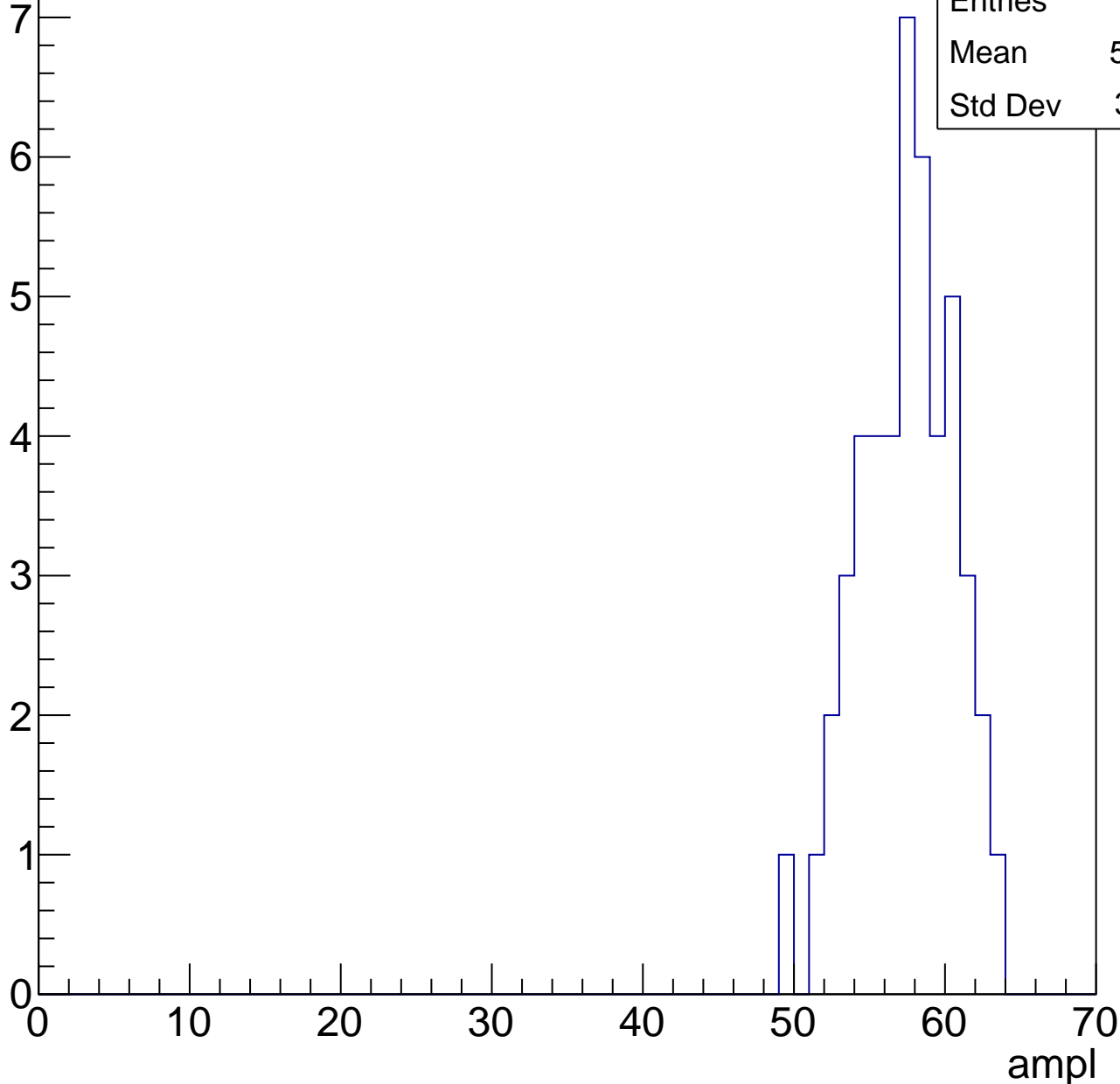
calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U5-ch47, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

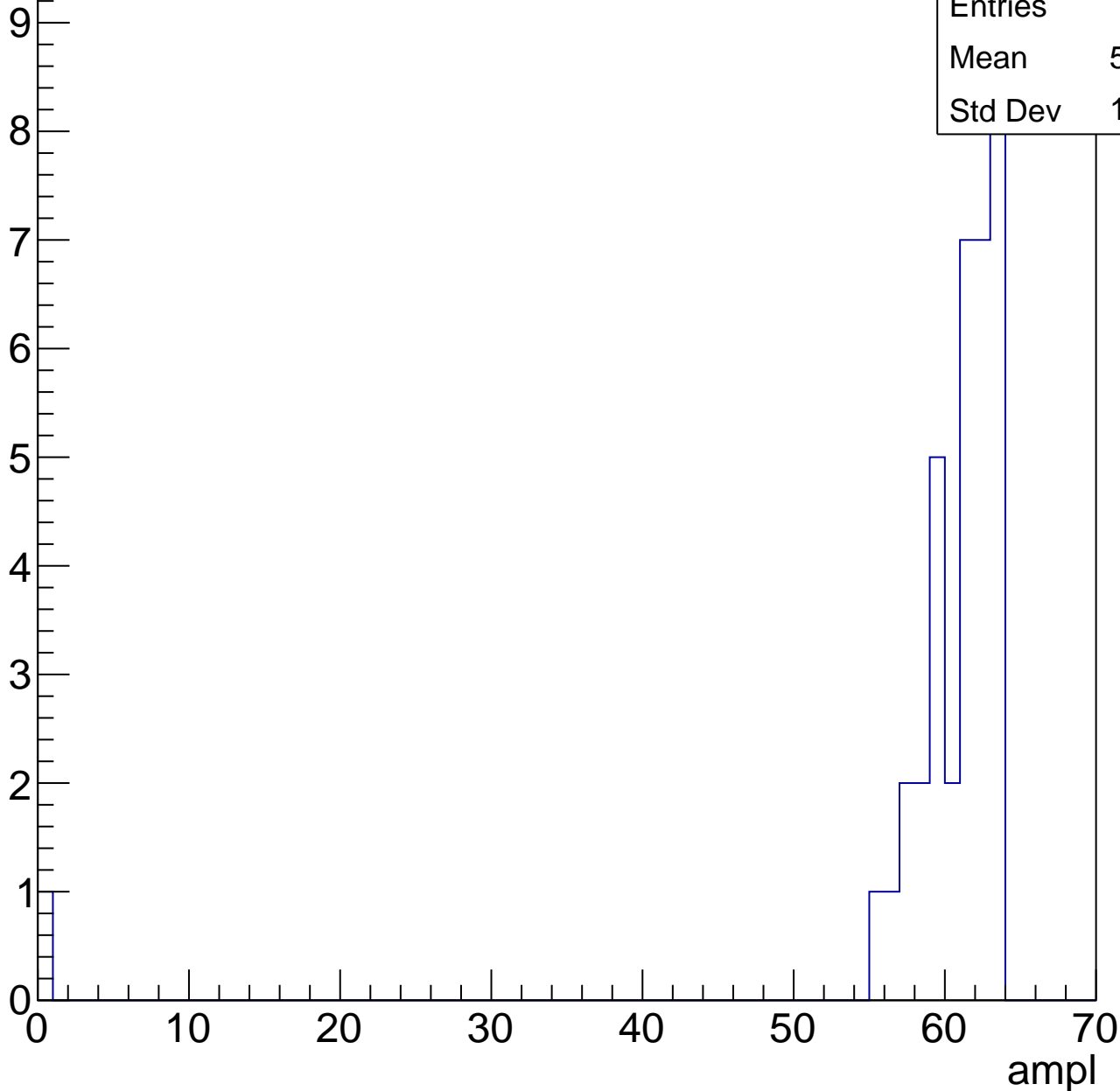


# B0L001S, U5-ch47, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	37
Mean	59.03
Std Dev	10.07



# B0L001S, U5-ch47, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U5-ch47, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch48, adc0

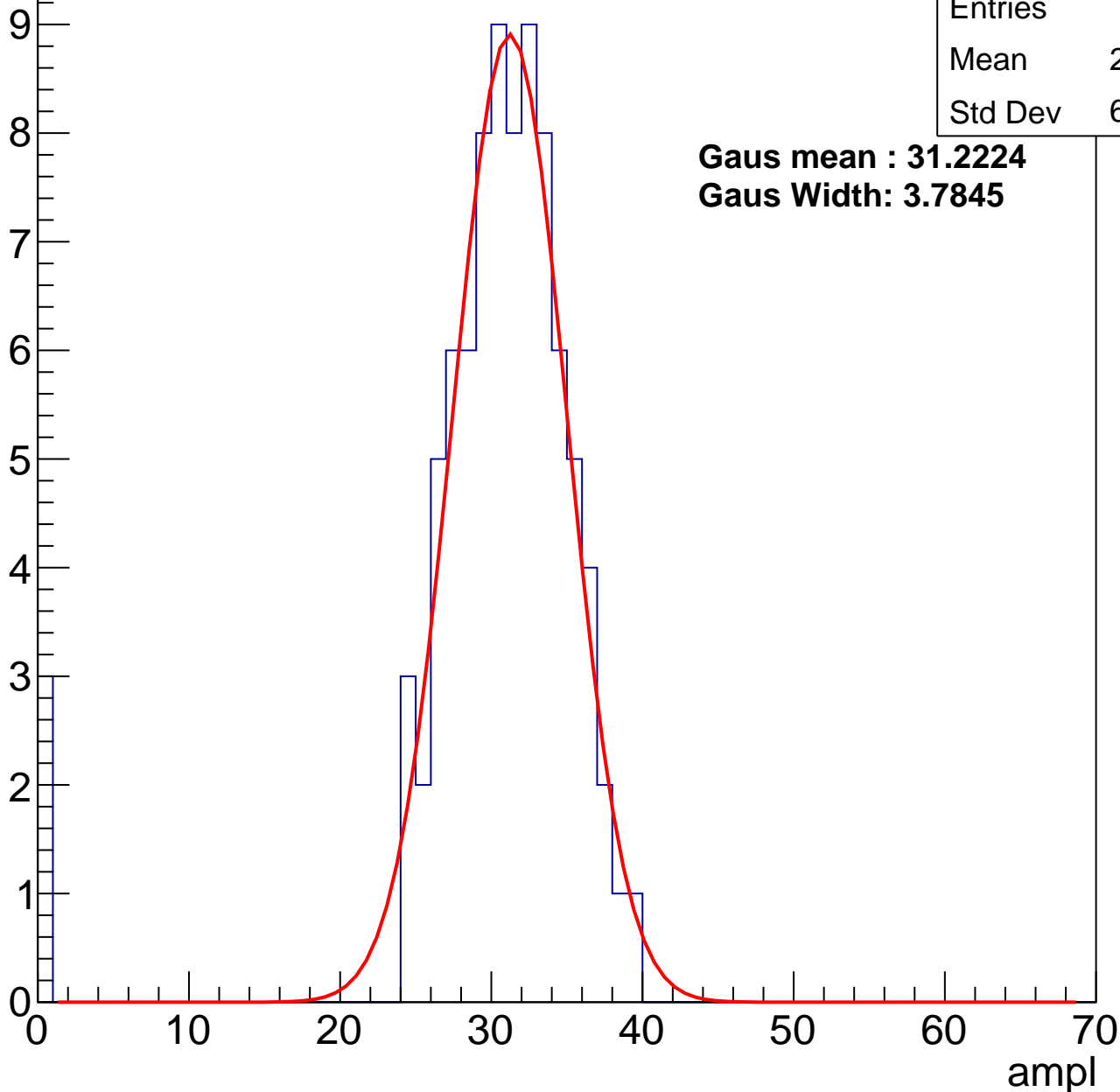
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	86
Mean	29.74
Std Dev	6.597

**Gaus mean : 31.2224**

**Gaus Width: 3.7845**



# B0L001S, U5-ch48, adc1

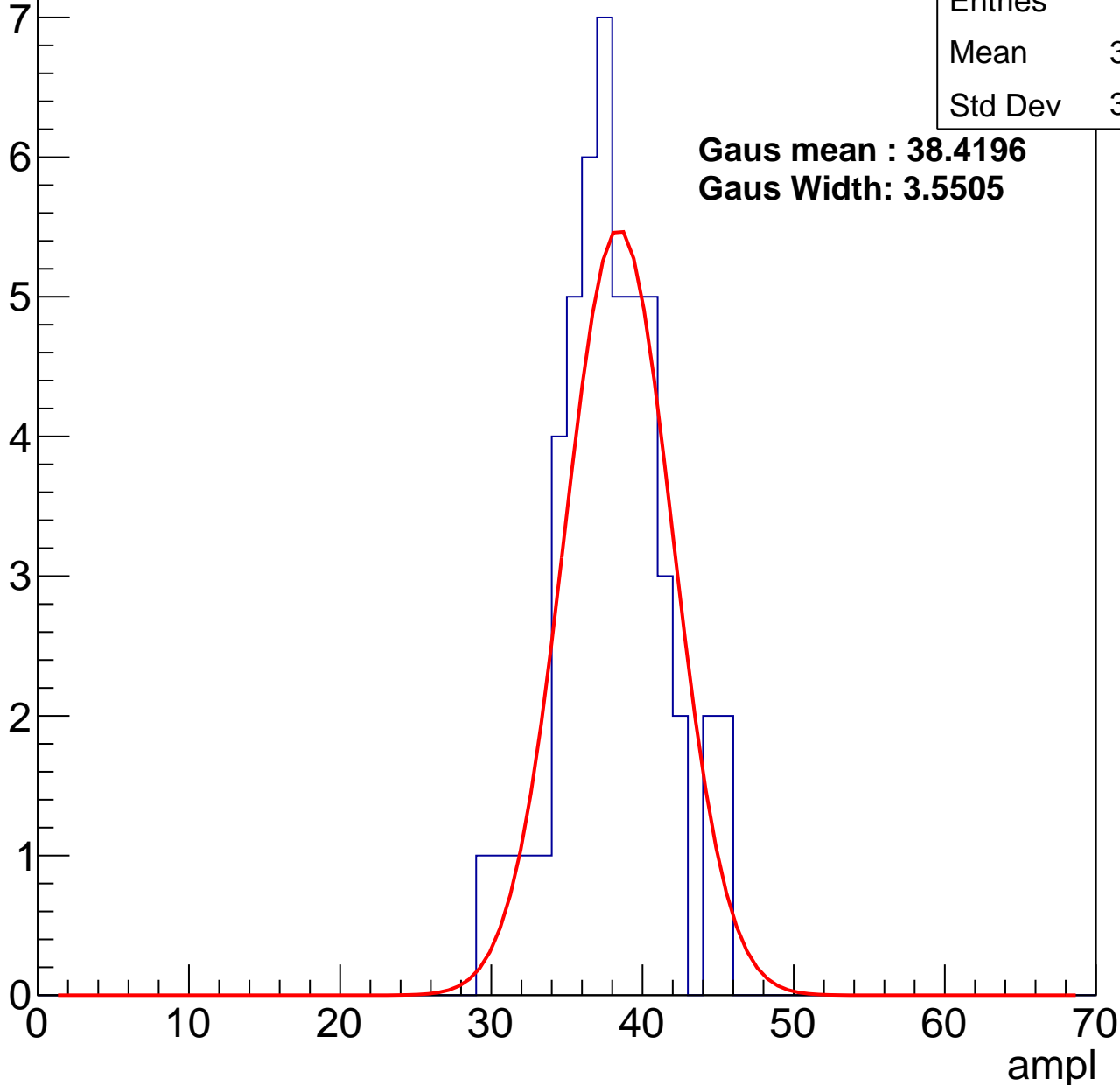
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	51
Mean	37.47
Std Dev	3.528

**Gaus mean : 38.4196**

**Gaus Width: 3.5505**



# B0L001S, U5-ch48, adc2

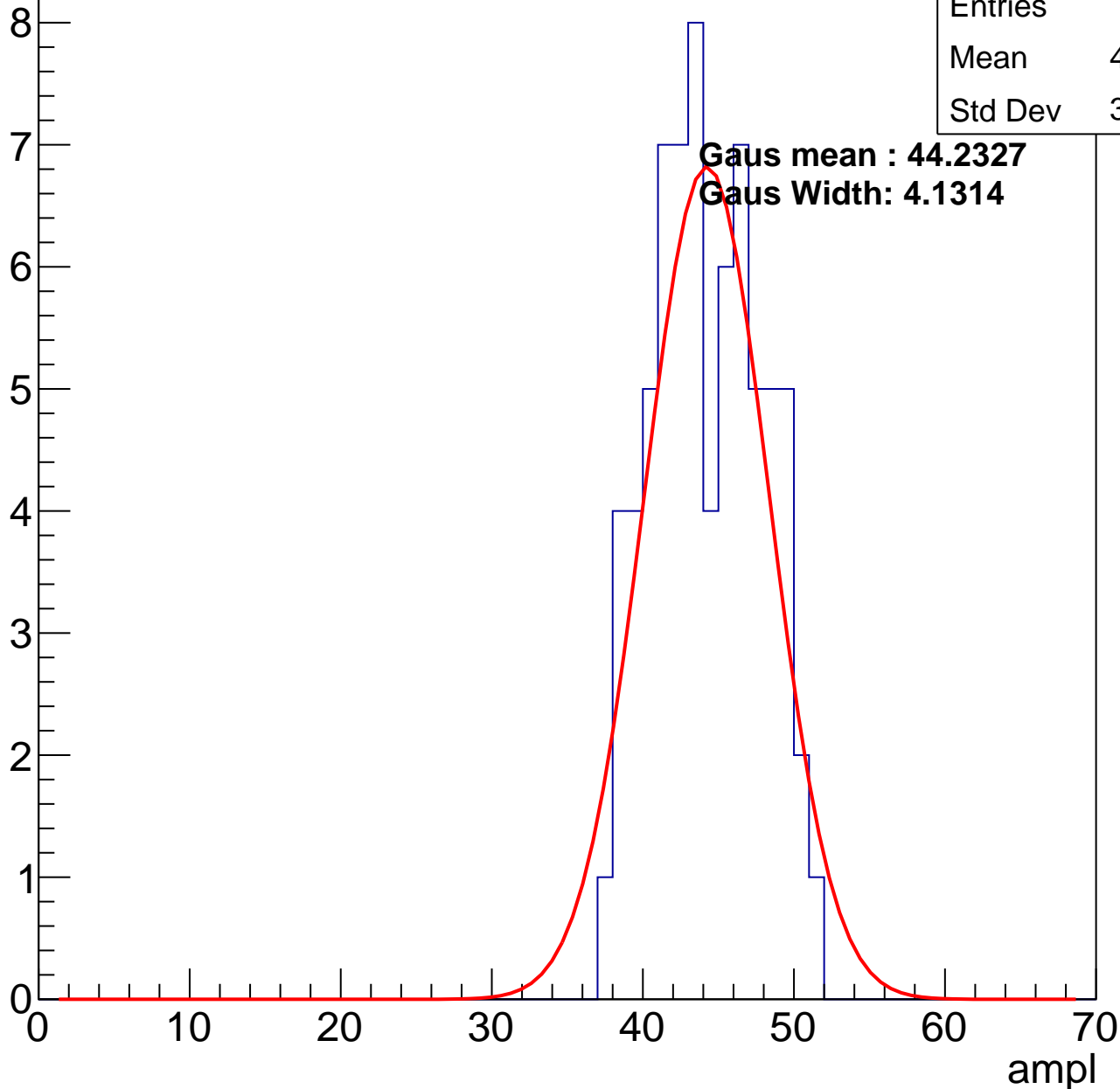
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	43.79
Std Dev	3.508

**Gaus mean : 44.2327**

**Gaus Width: 4.1314**

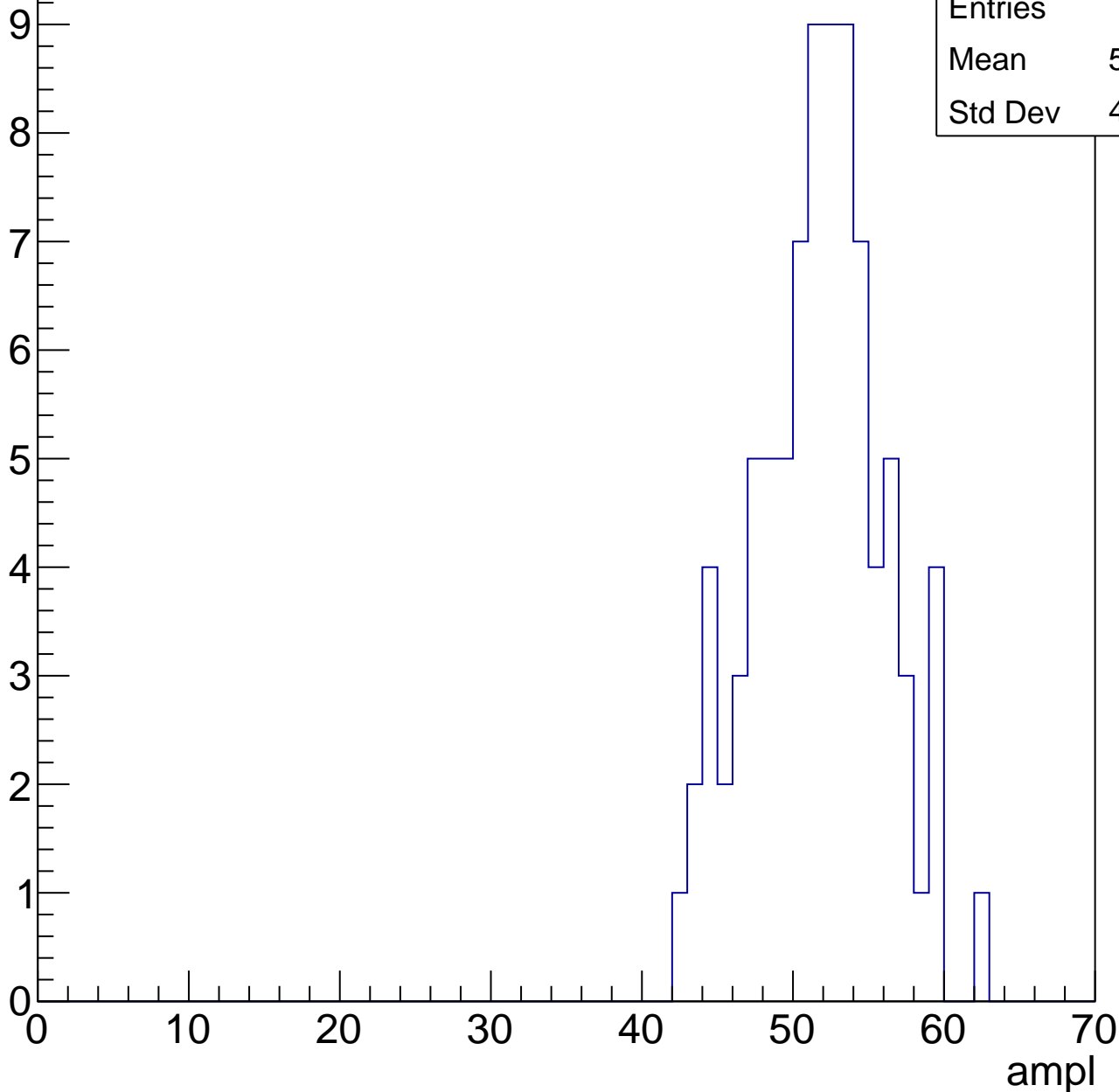


# B0L001S, U5-ch48, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	86
Mean	51.29
Std Dev	4.215

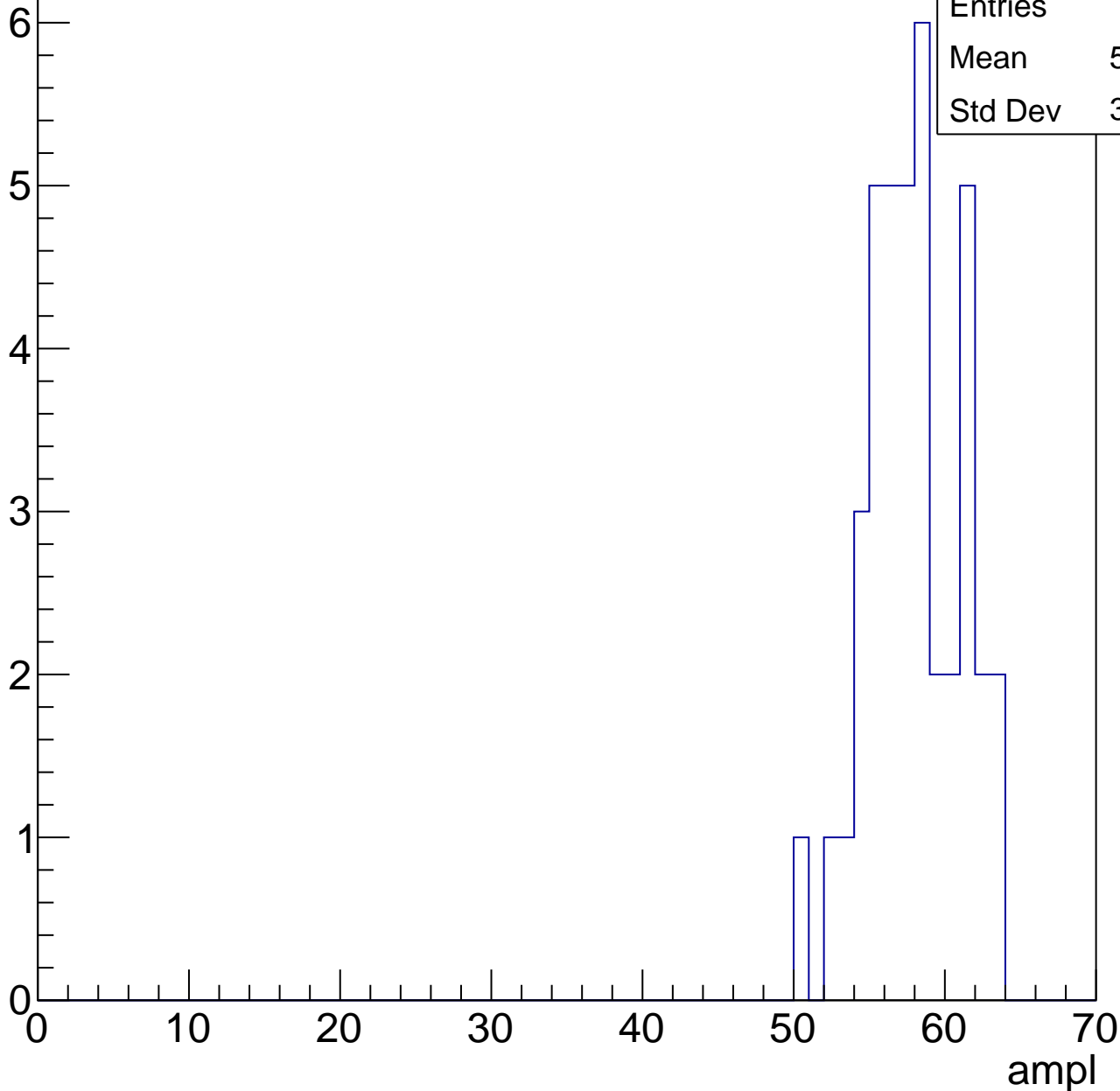


# B0L001S, U5-ch48, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	40
Mean	57.45
Std Dev	3.033



# B0L001S, U5-ch48, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

7

6

5

4

3

2

1

0

Entries	31
Mean	60.61
Std Dev	1.979

ampl

10

20

30

40

50

60

70

# B0L001S, U5-ch48, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	8
Mean	52.88
Std Dev	20.08

ampl

0 10 20 30 40 50 60 70



# B0L001S, U5-ch48, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U5-ch49, adc0

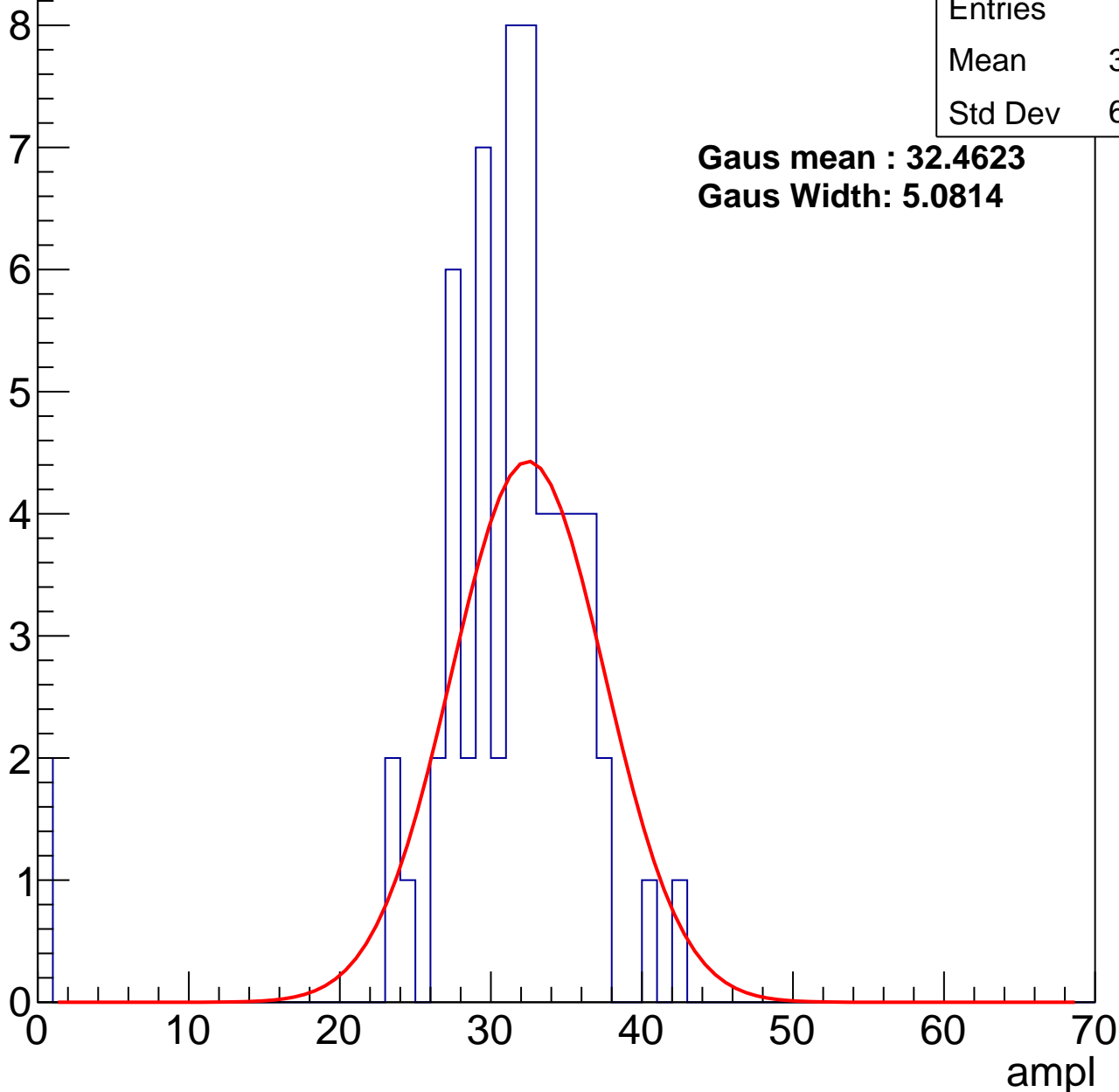
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	30.25
Std Dev	6.779

**Gaus mean : 32.4623**

**Gaus Width: 5.0814**



# B0L001S, U5-ch49, adc1

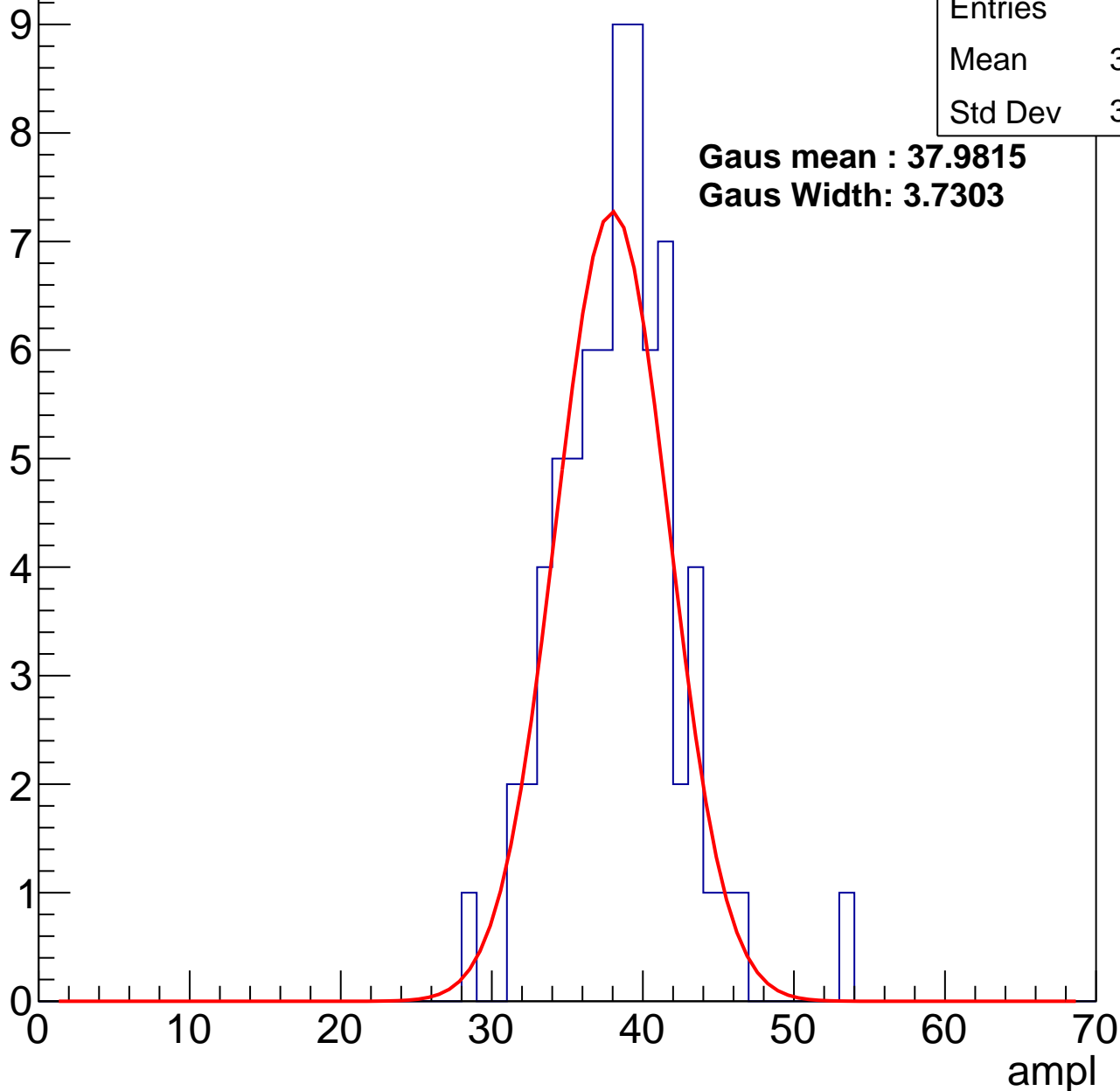
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	37.96
Std Dev	3.956

**Gaus mean : 37.9815**

**Gaus Width: 3.7303**



# B0L001S, U5-ch49, adc2

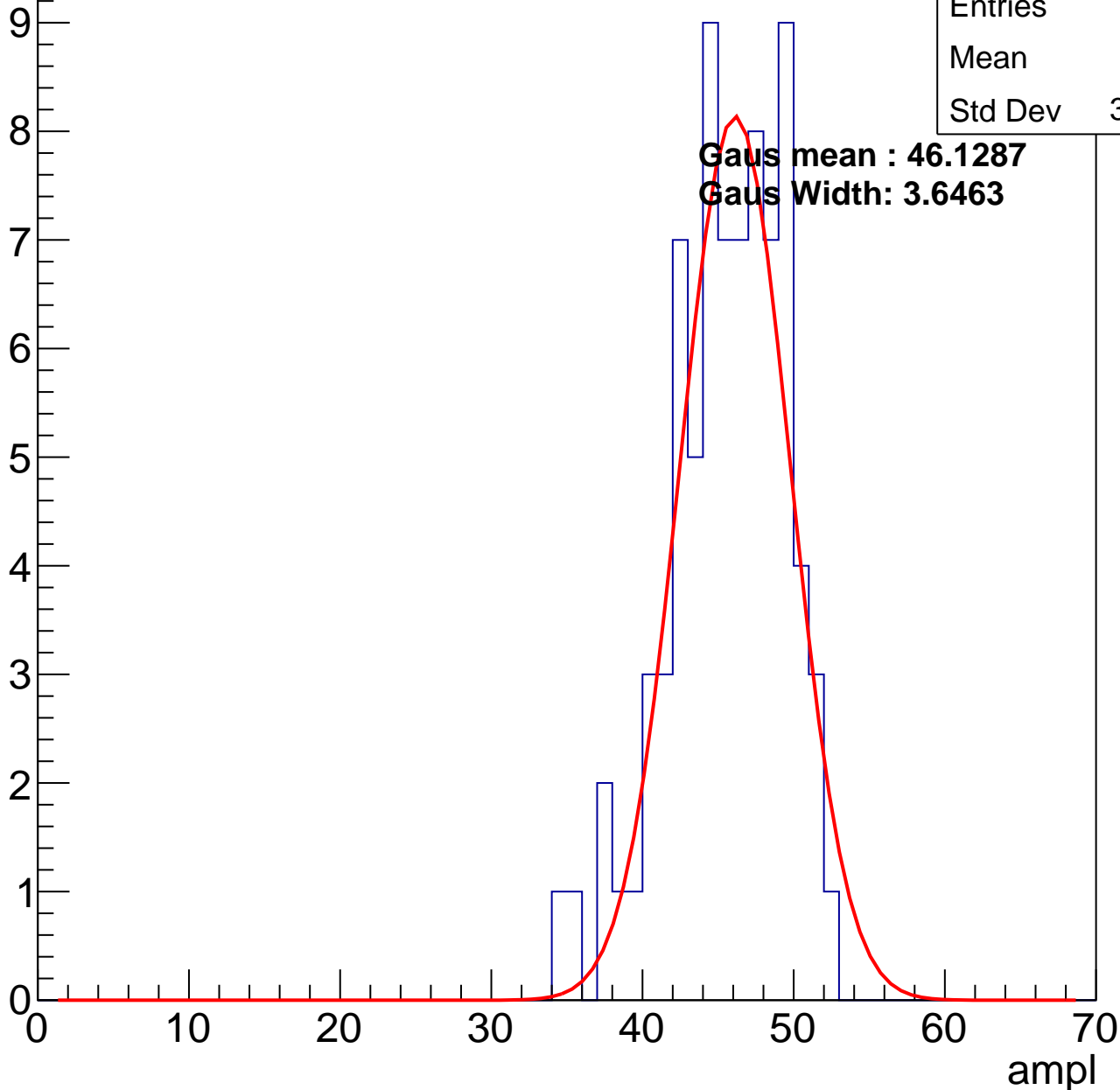
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	79
Mean	45.1
Std Dev	3.817

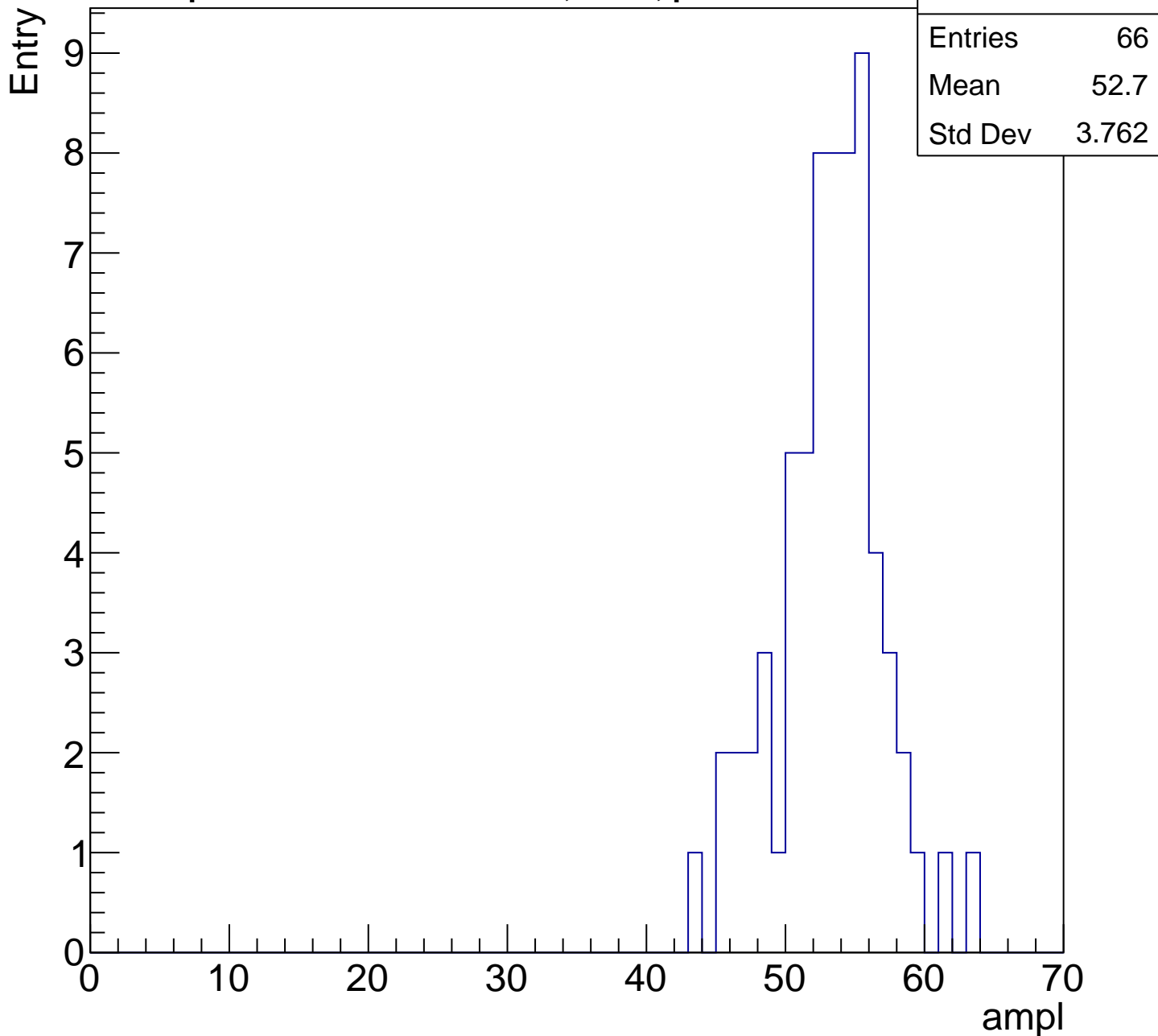
**Gaus mean : 46.1287**

**Gaus Width: 3.6463**



# B0L001S, U5-ch49, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

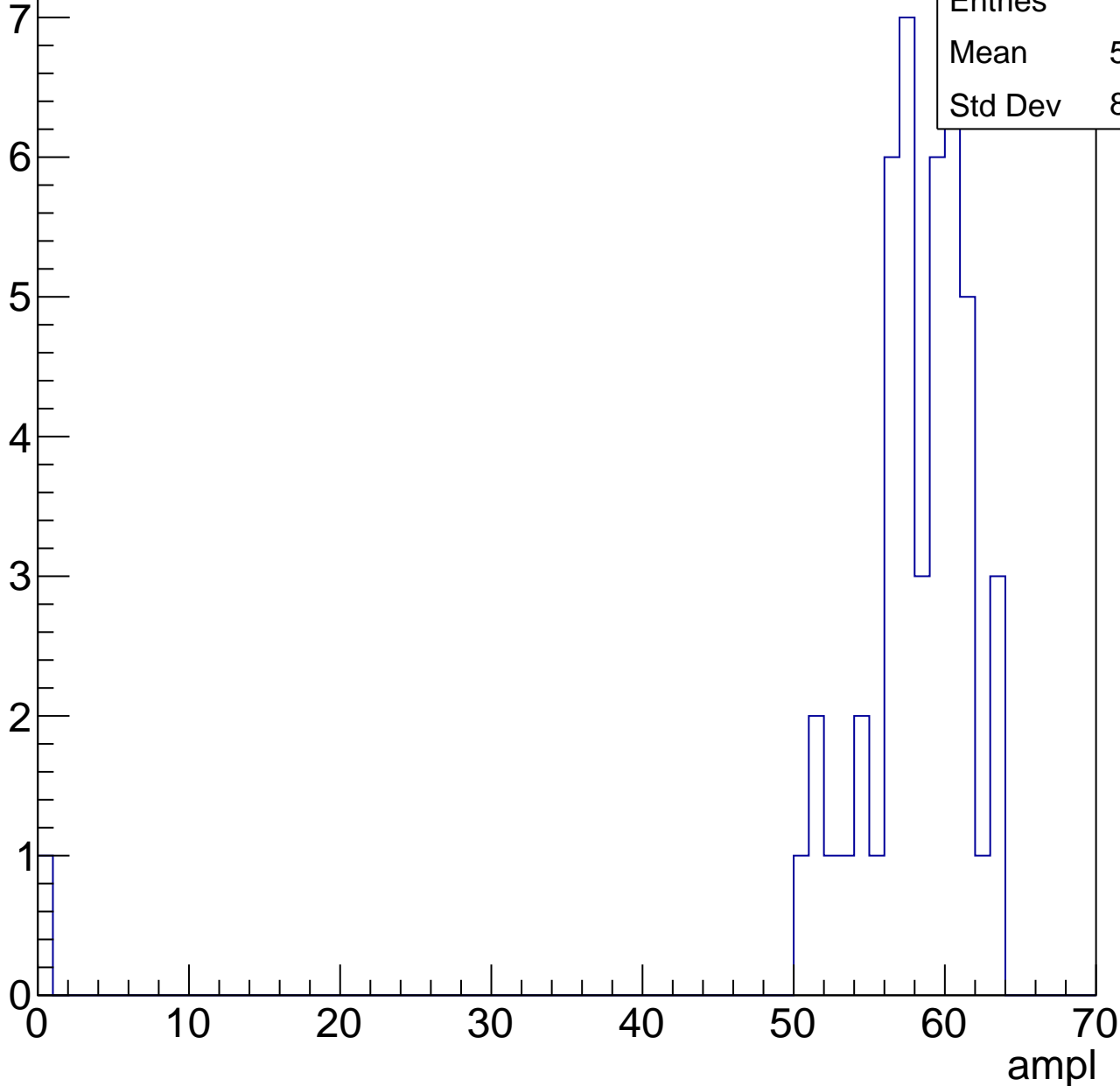


# B0L001S, U5-ch49, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	47
Mean	56.57
Std Dev	8.913

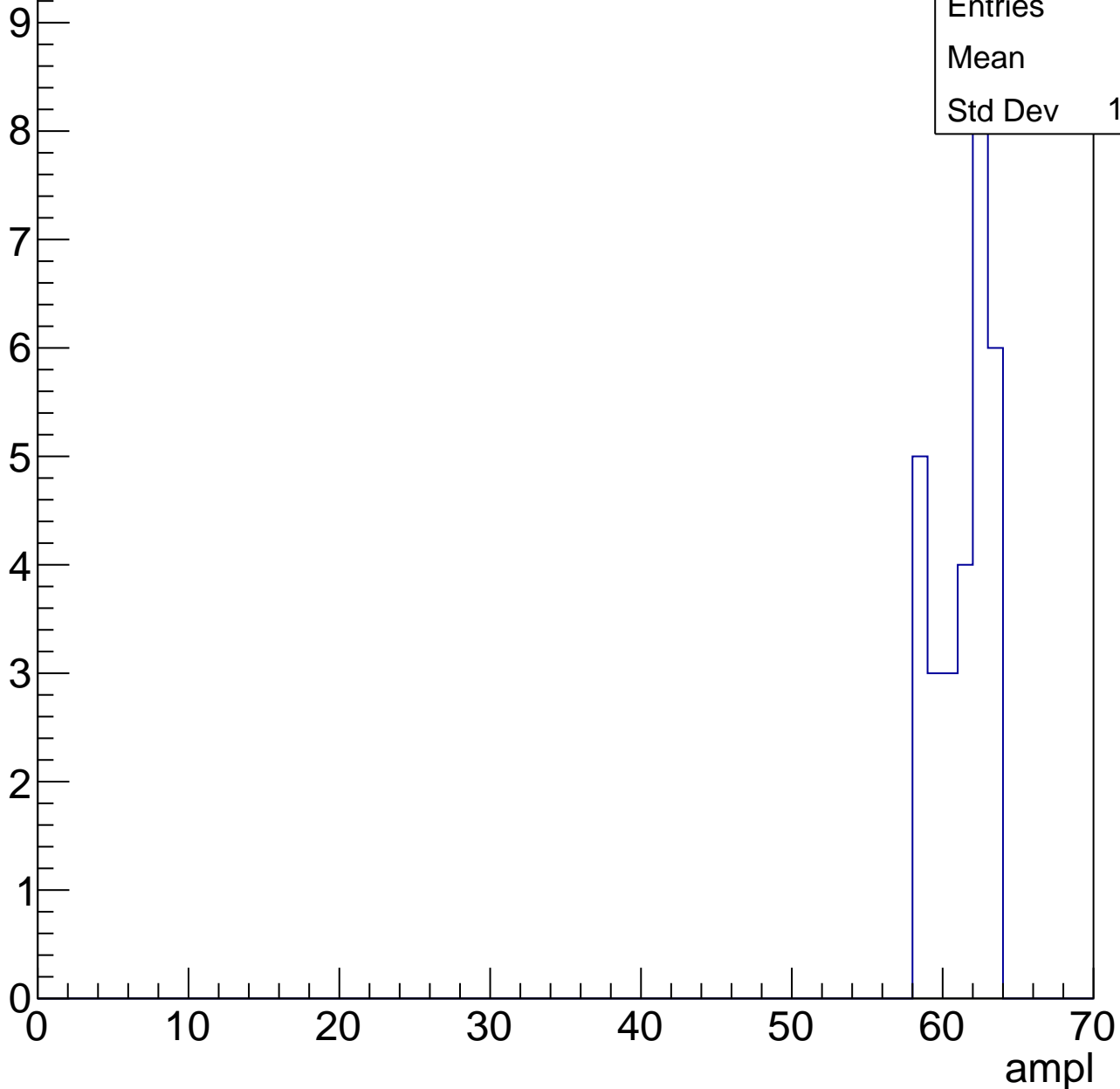


# B0L001S, U5-ch49, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	30
Mean	60.9
Std Dev	1.758



# B0L001S, U5-ch49, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U5-ch49, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U5-ch50, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	70
Mean	29.67
Std Dev	3.405

**Gaus mean : 30.0547**

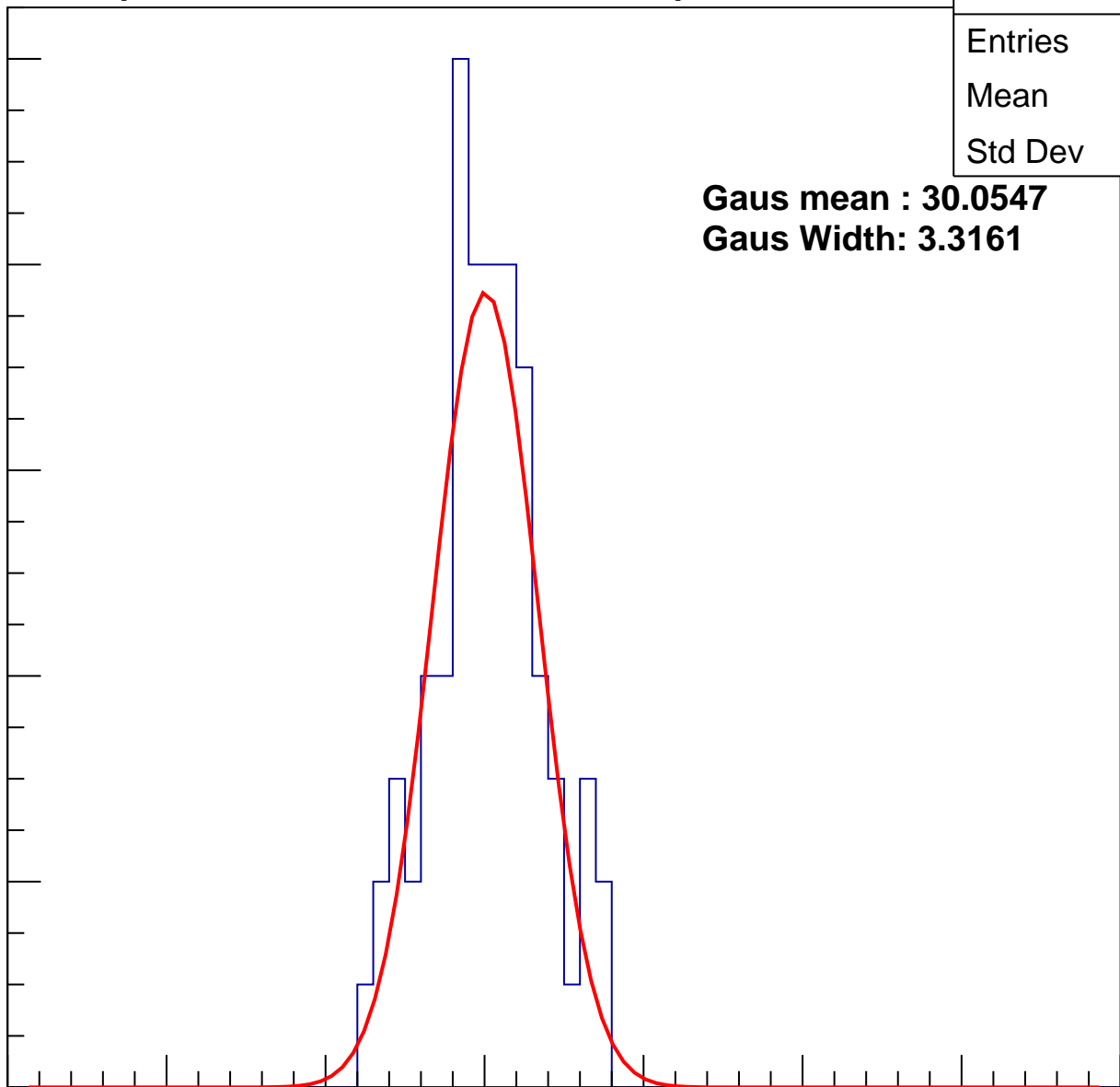
**Gaus Width: 3.3161**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U5-ch50, adc1

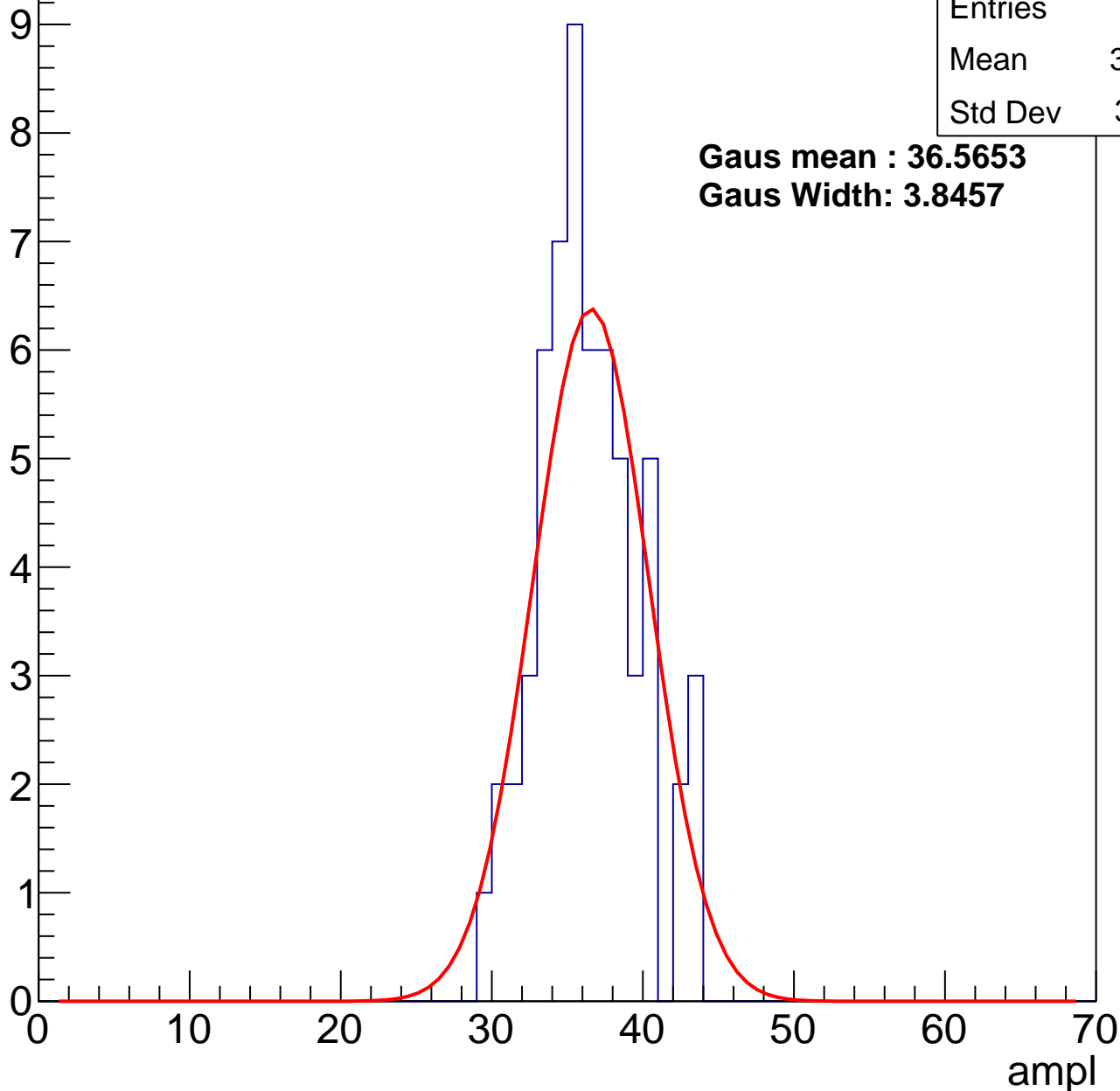
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	35.93
Std Dev	3.321

**Gaus mean : 36.5653**

**Gaus Width: 3.8457**



# B0L001S, U5-ch50, adc2

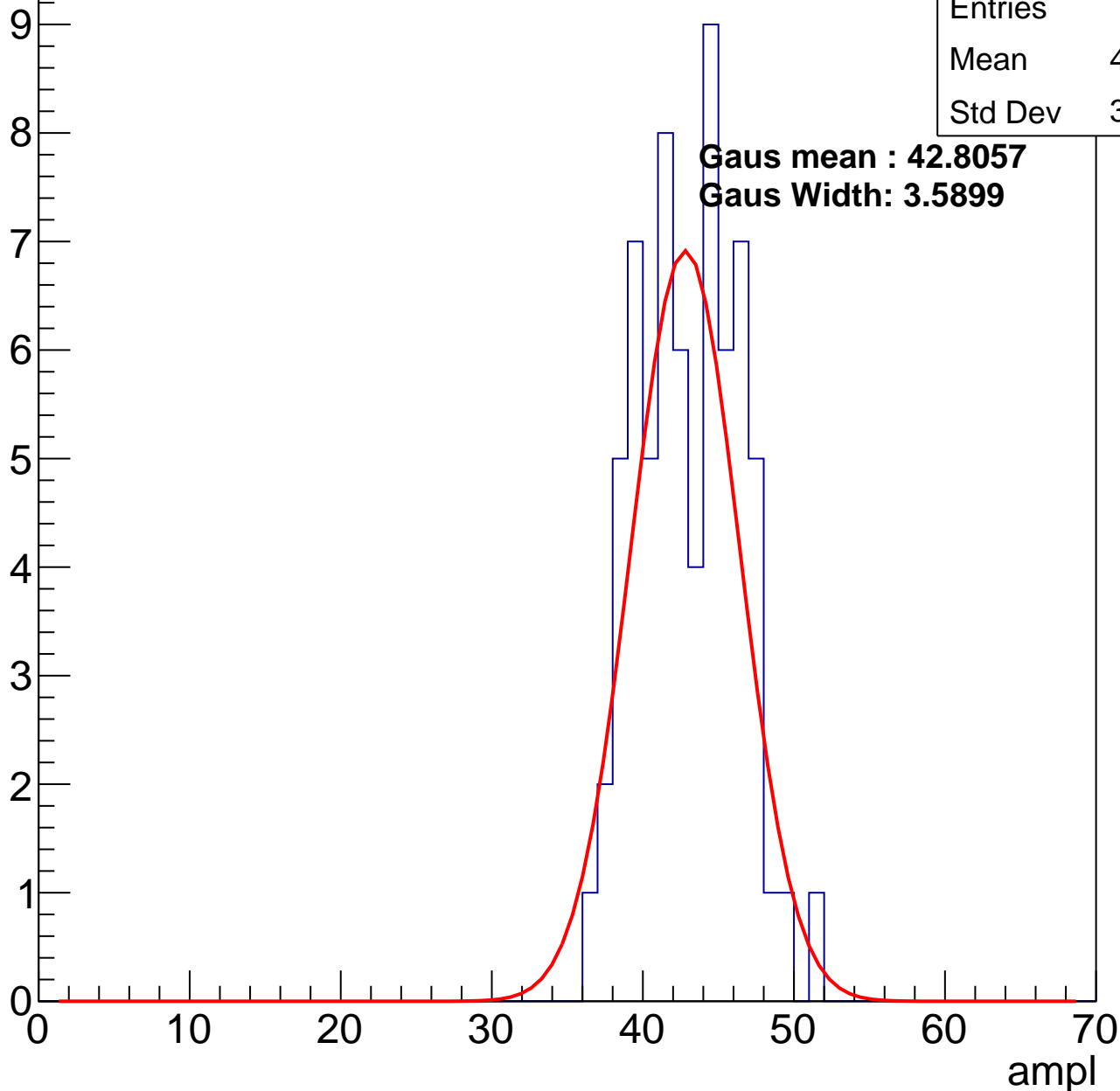
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	42.59
Std Dev	3.278

**Gaus mean : 42.8057**

**Gaus Width: 3.5899**



# B0L001S, U5-ch50, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	90
Mean	50.23
Std Dev	4.121

Entry

10

8

6

4

2

0

0

10

20

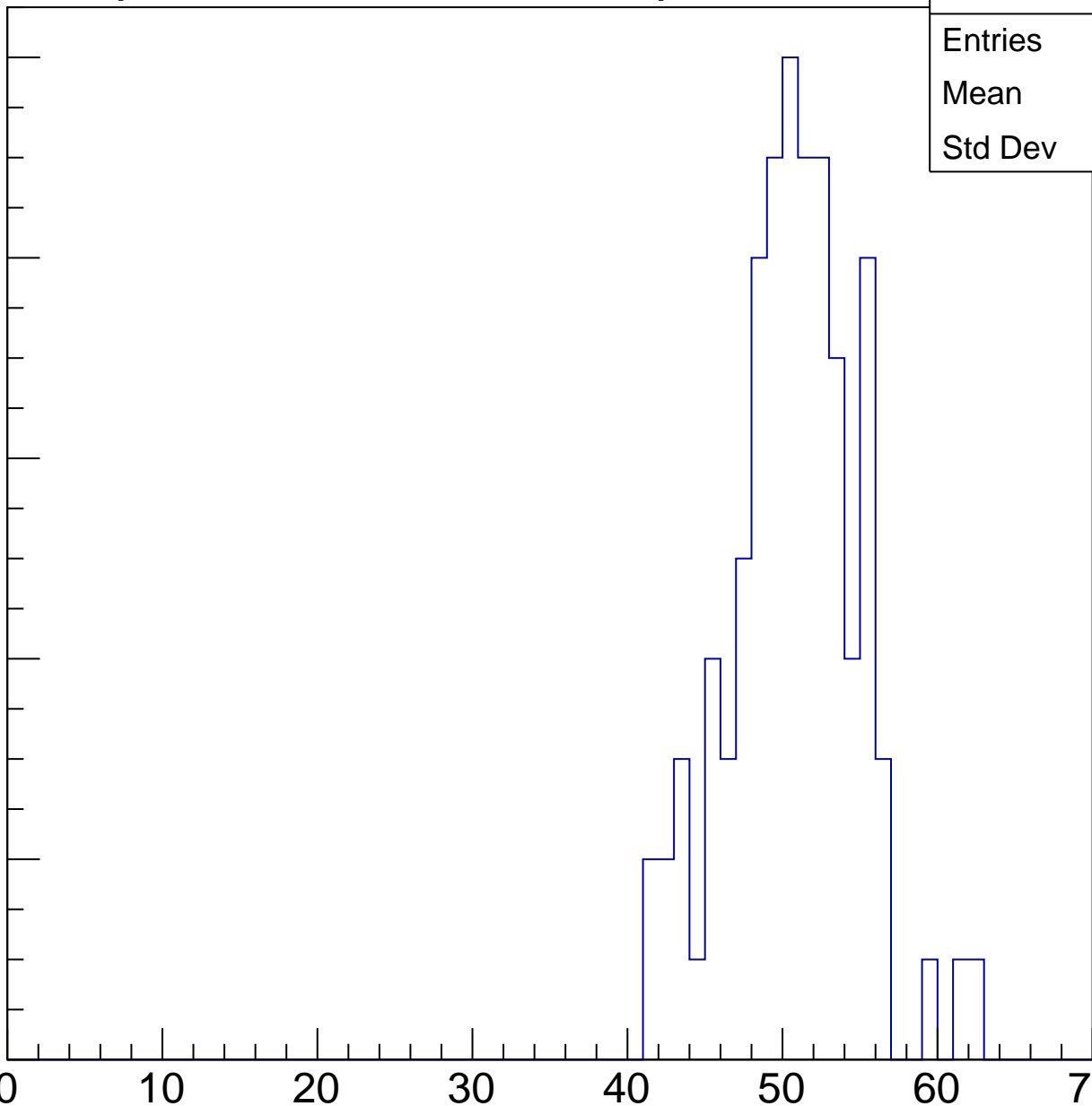
30

40

50

60

ampl

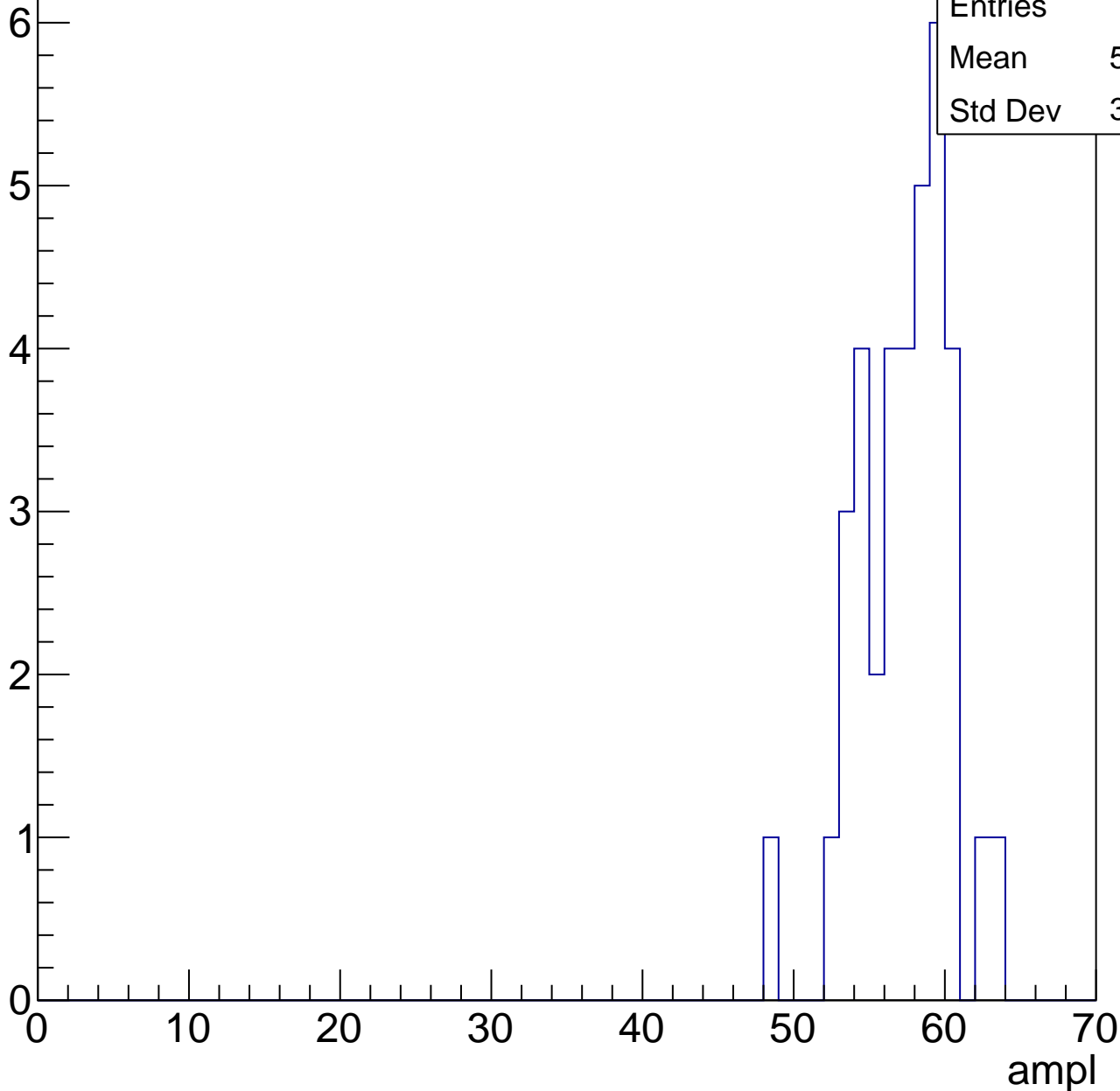


# B0L001S, U5-ch50, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

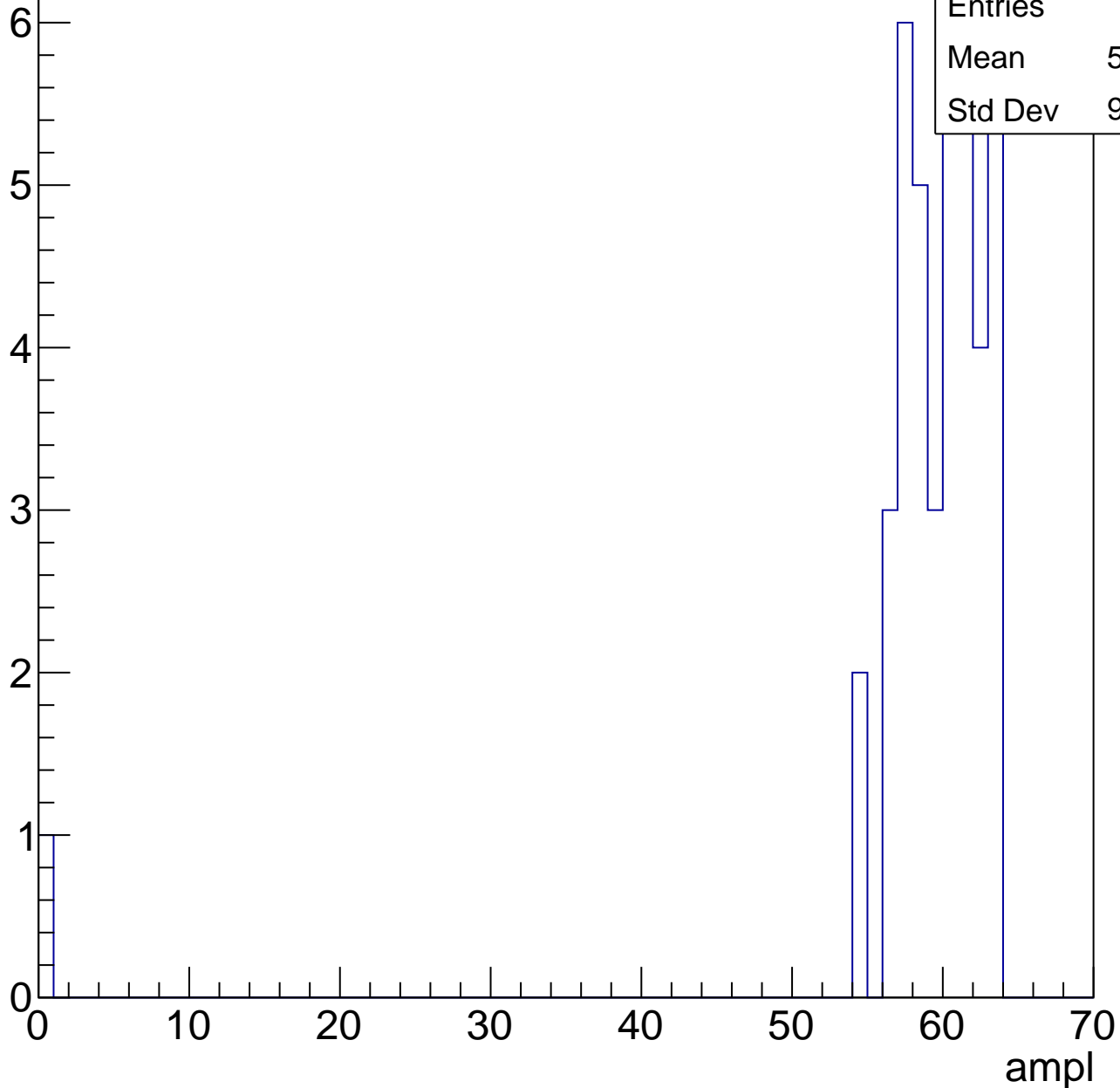
Entries	36
Mean	56.83
Std Dev	3.014



# B0L001S, U5-ch50, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

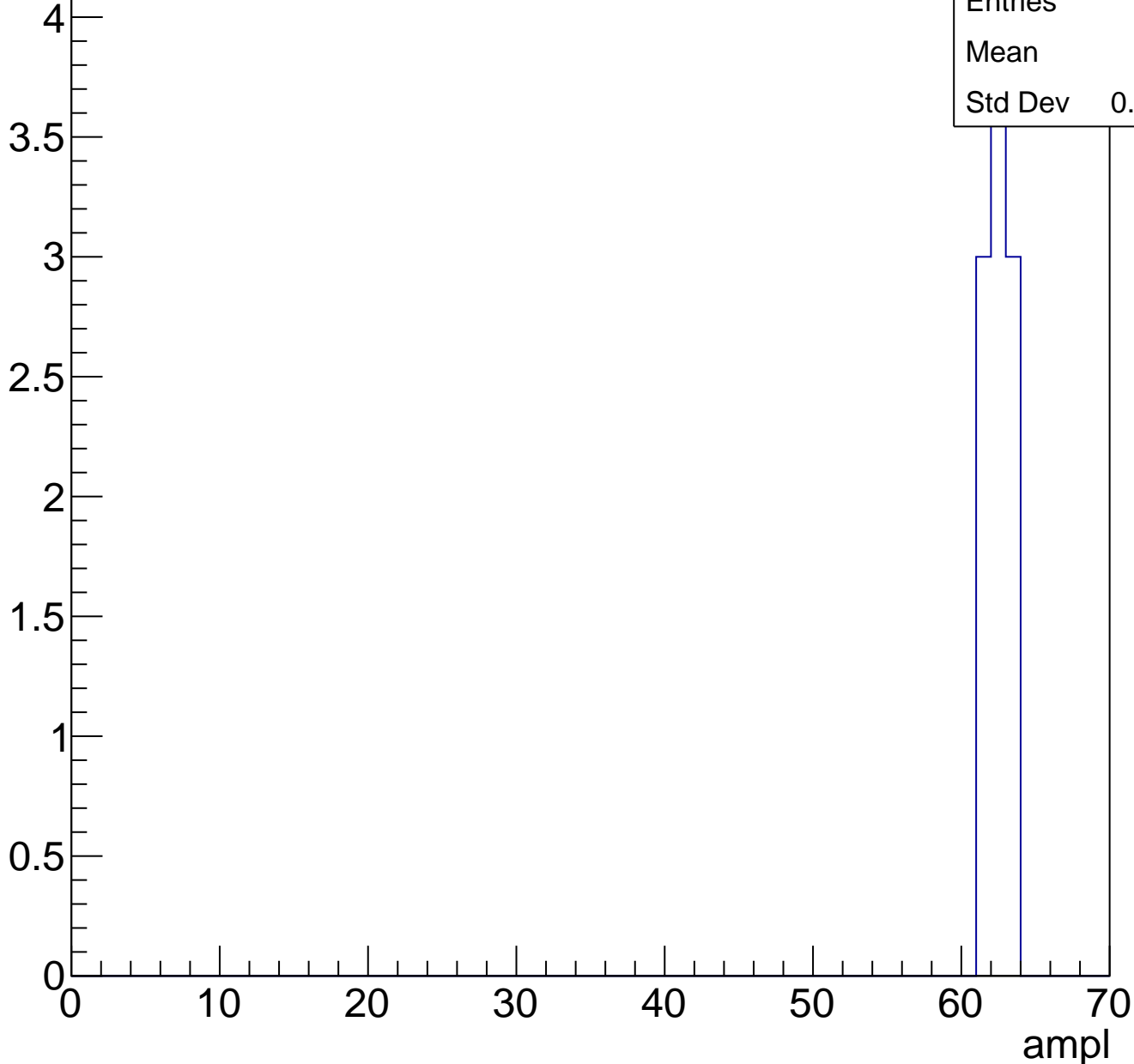
Entry



# B0L001S, U5-ch50, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch50, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L001S, U5-ch51, adc0

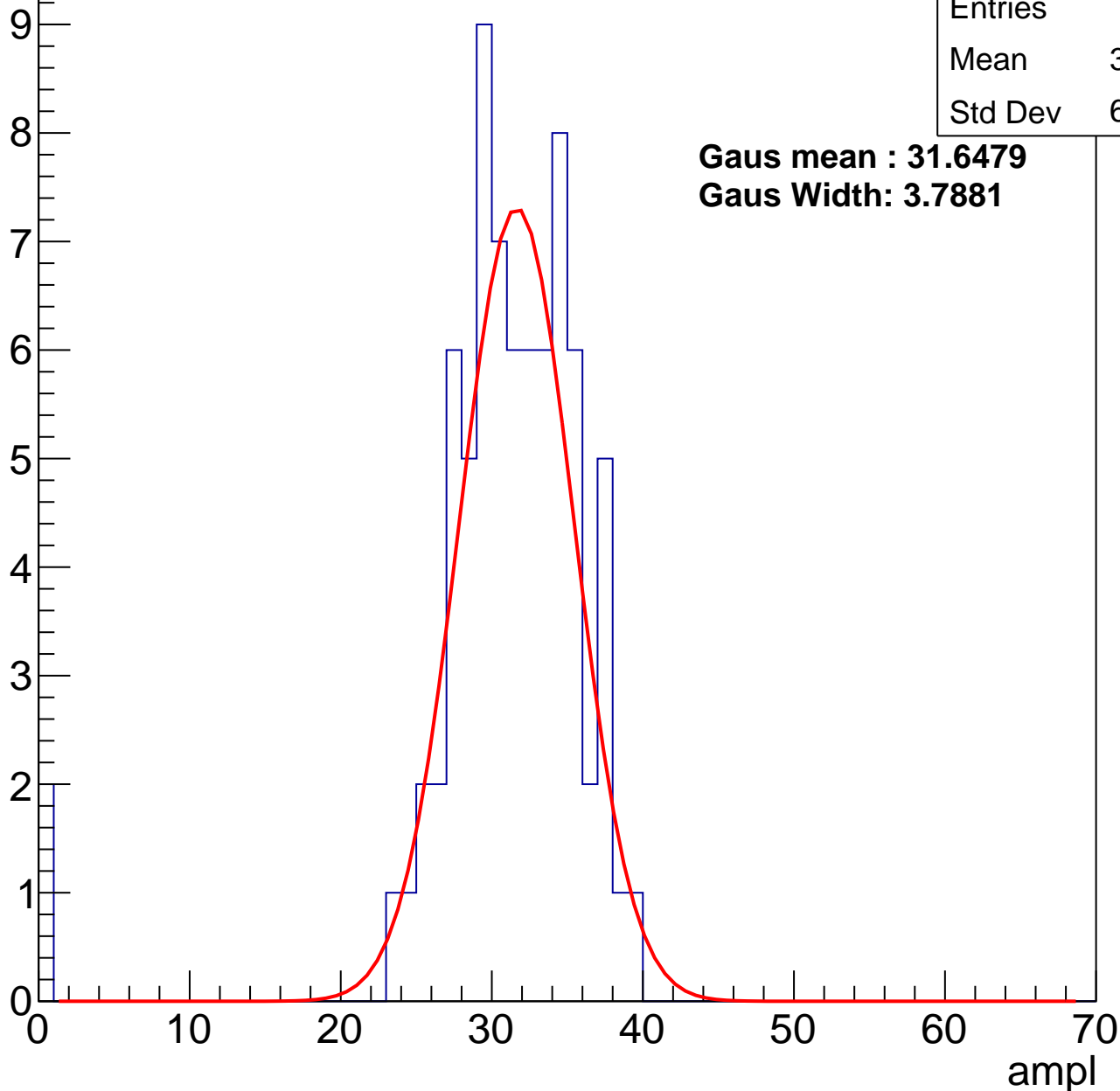
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	76
Mean	30.45
Std Dev	6.133

**Gaus mean : 31.6479**

**Gaus Width: 3.7881**



# B0L001S, U5-ch51, adc1

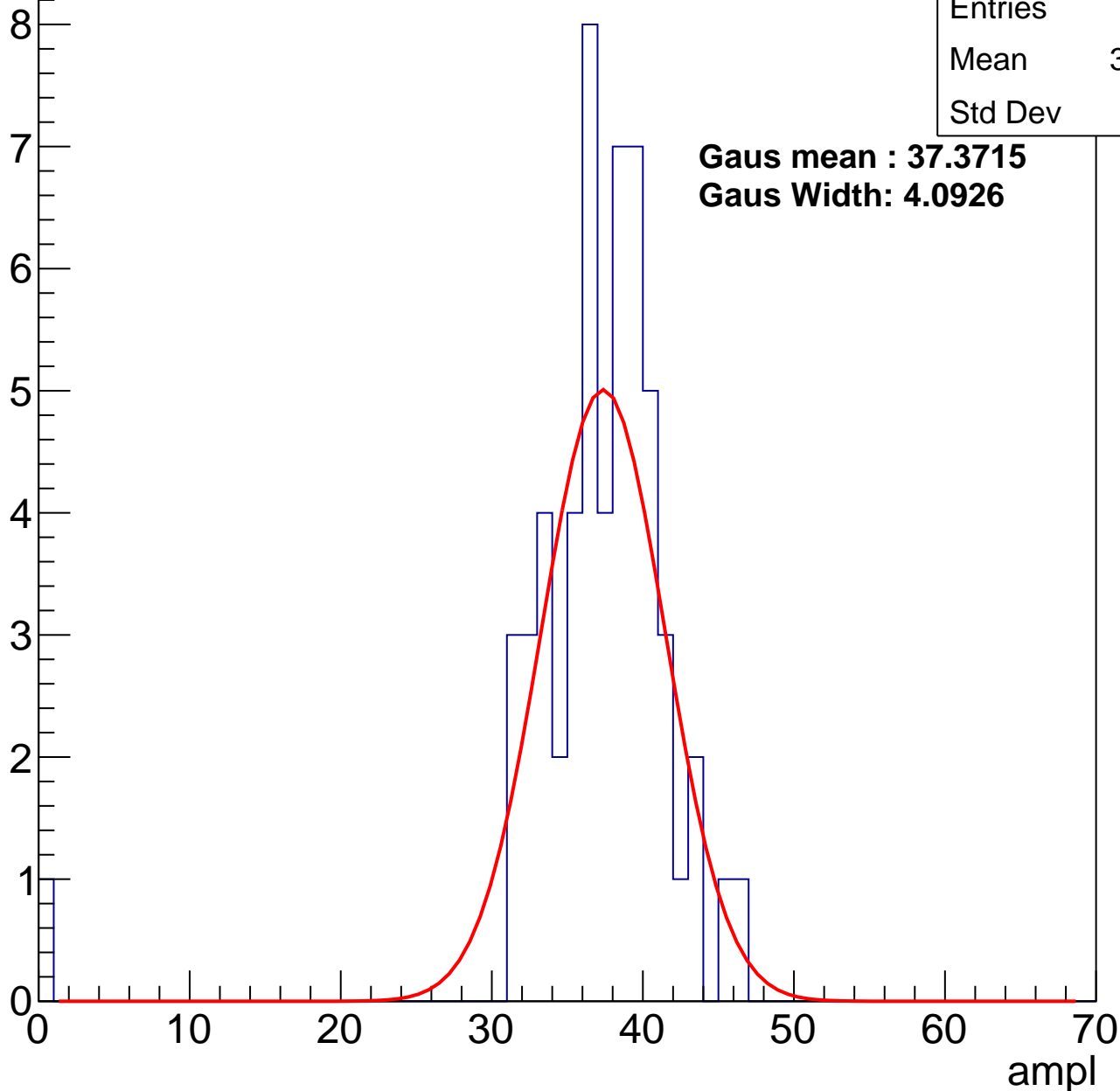
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	36.54
Std Dev	6

**Gaus mean : 37.3715**

**Gaus Width: 4.0926**



# B0L001S, U5-ch51, adc2

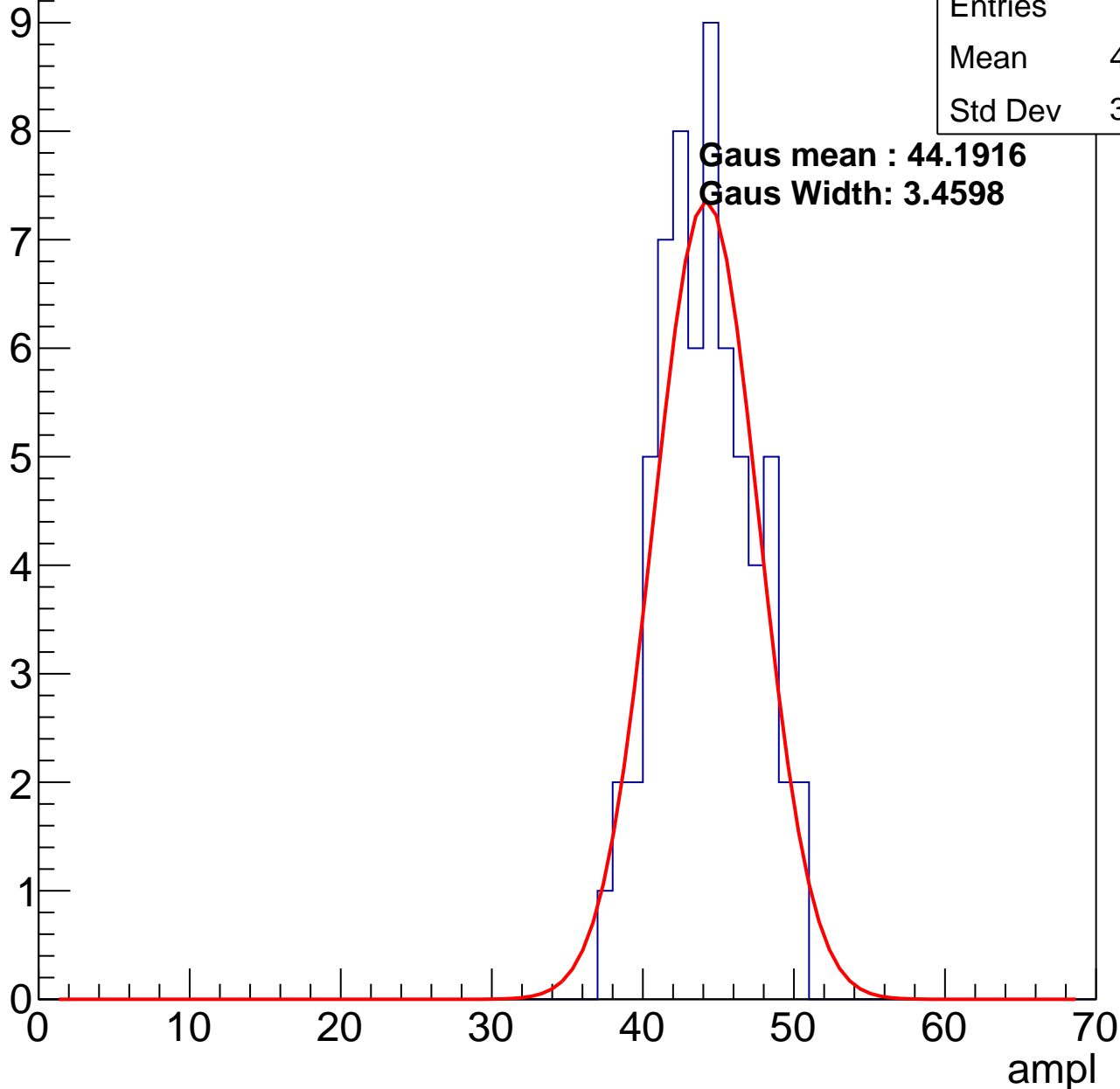
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	43.66
Std Dev	3.083

**Gaus mean : 44.1916**

**Gaus Width: 3.4598**

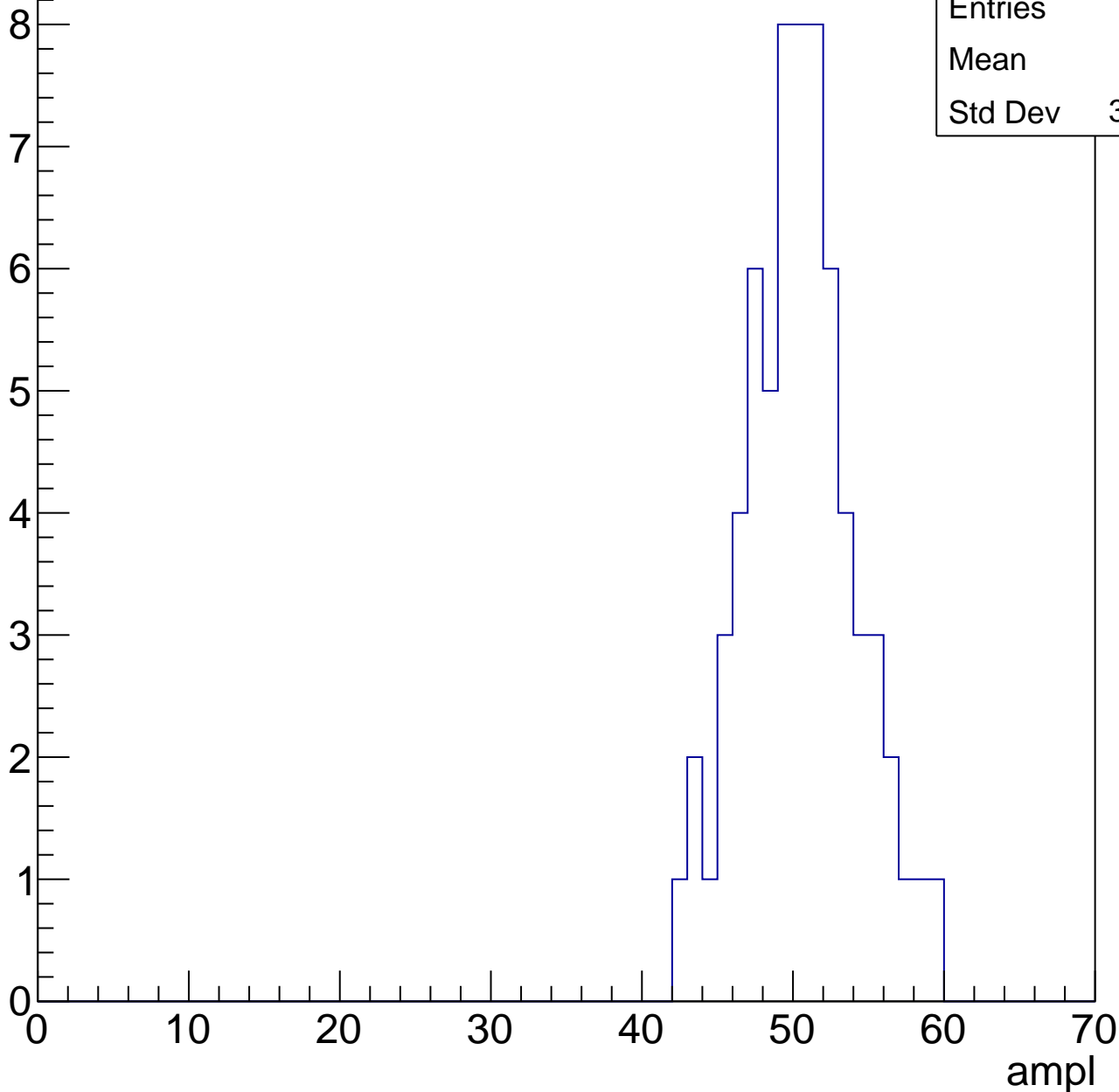


# B0L001S, U5-ch51, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

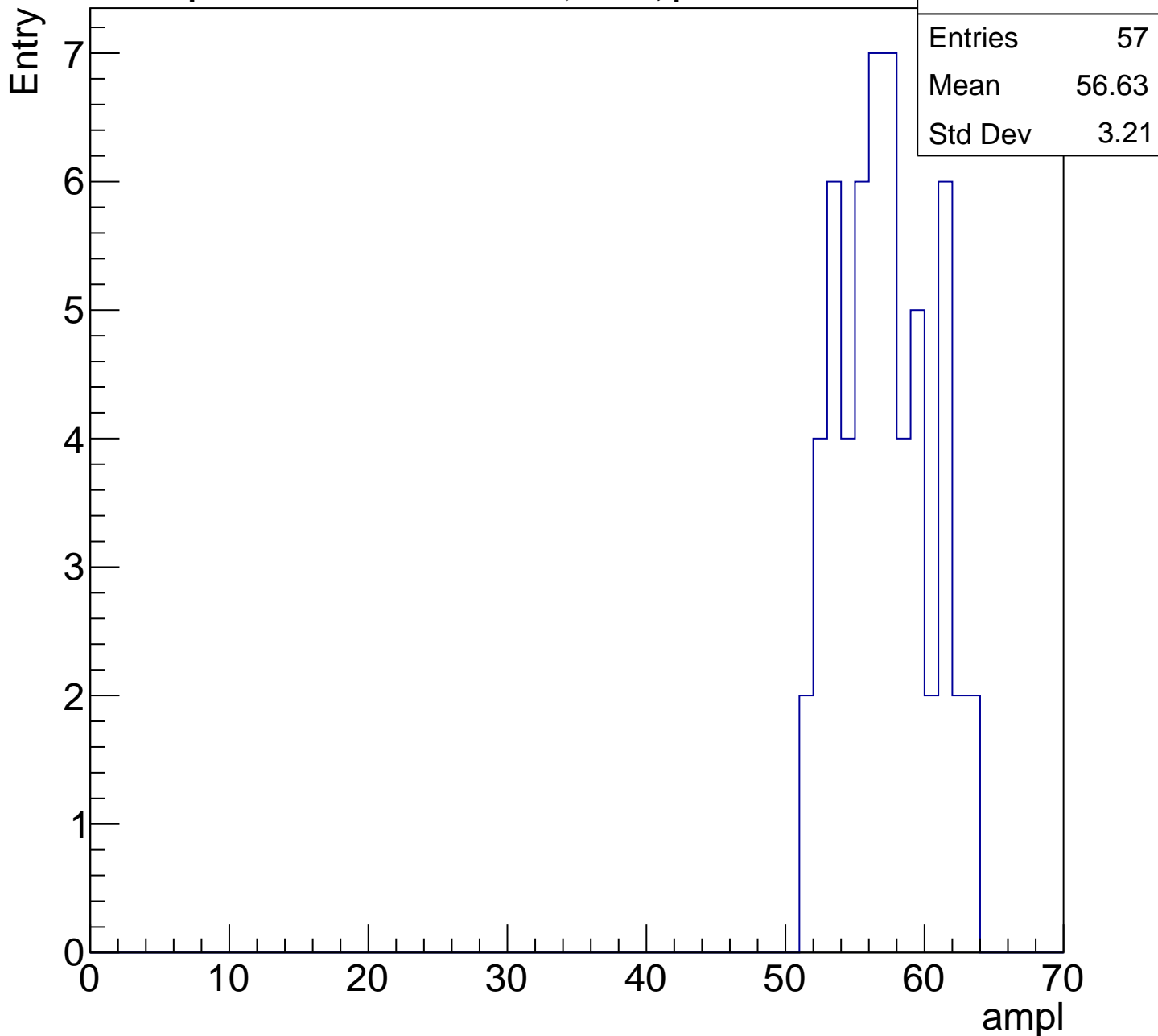
Entry

Entries	67
Mean	50
Std Dev	3.616



# B0L001S, U5-ch51, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

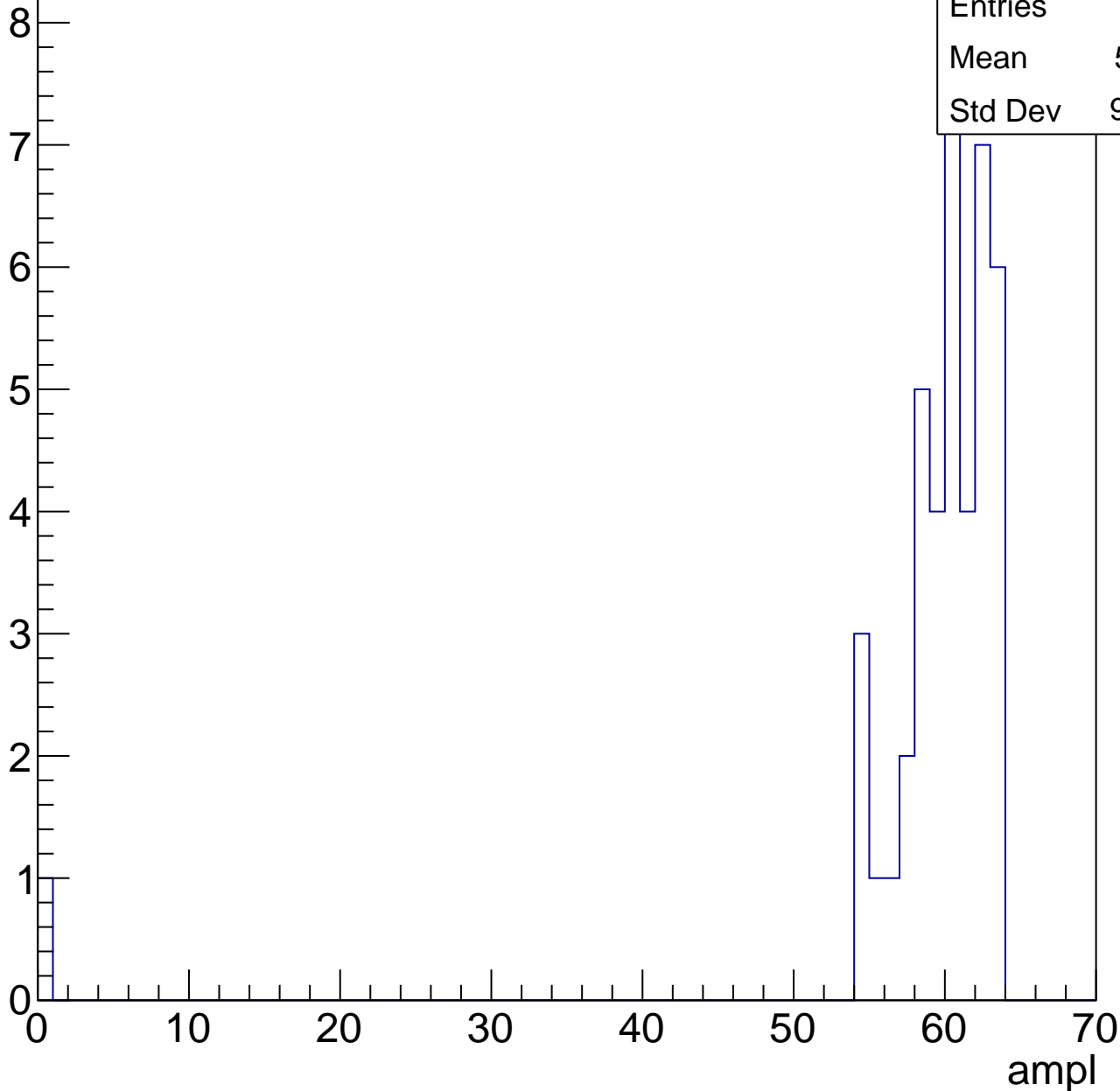


# B0L001S, U5-ch51, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	42
Mean	58.31
Std Dev	9.458



# B0L001S, U5-ch51, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	3
Mean	62.67
Std Dev	0.4714



# B0L001S, U5-ch51, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch52, adc0

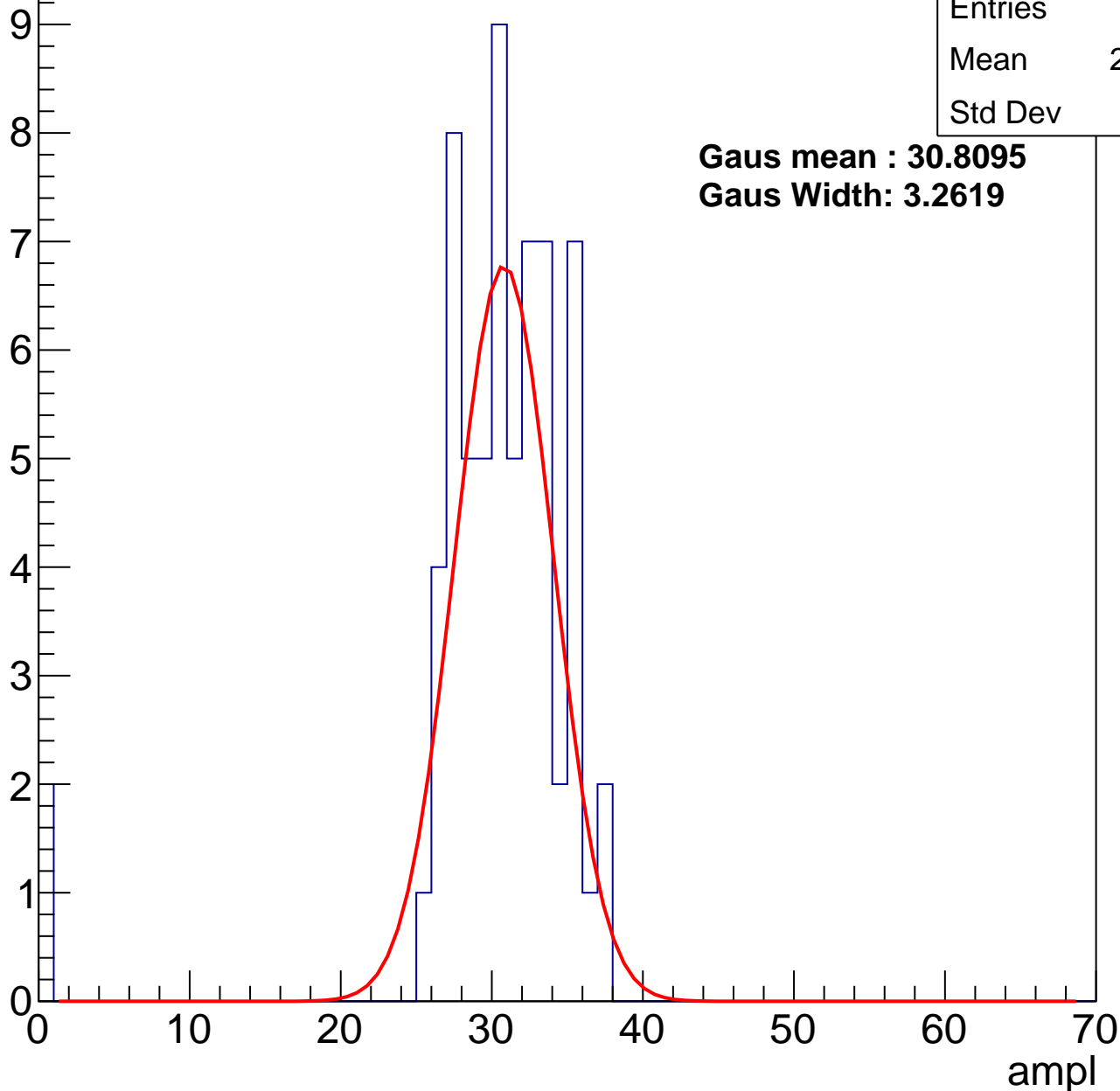
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	29.74
Std Dev	6.1

**Gaus mean : 30.8095**

**Gaus Width: 3.2619**



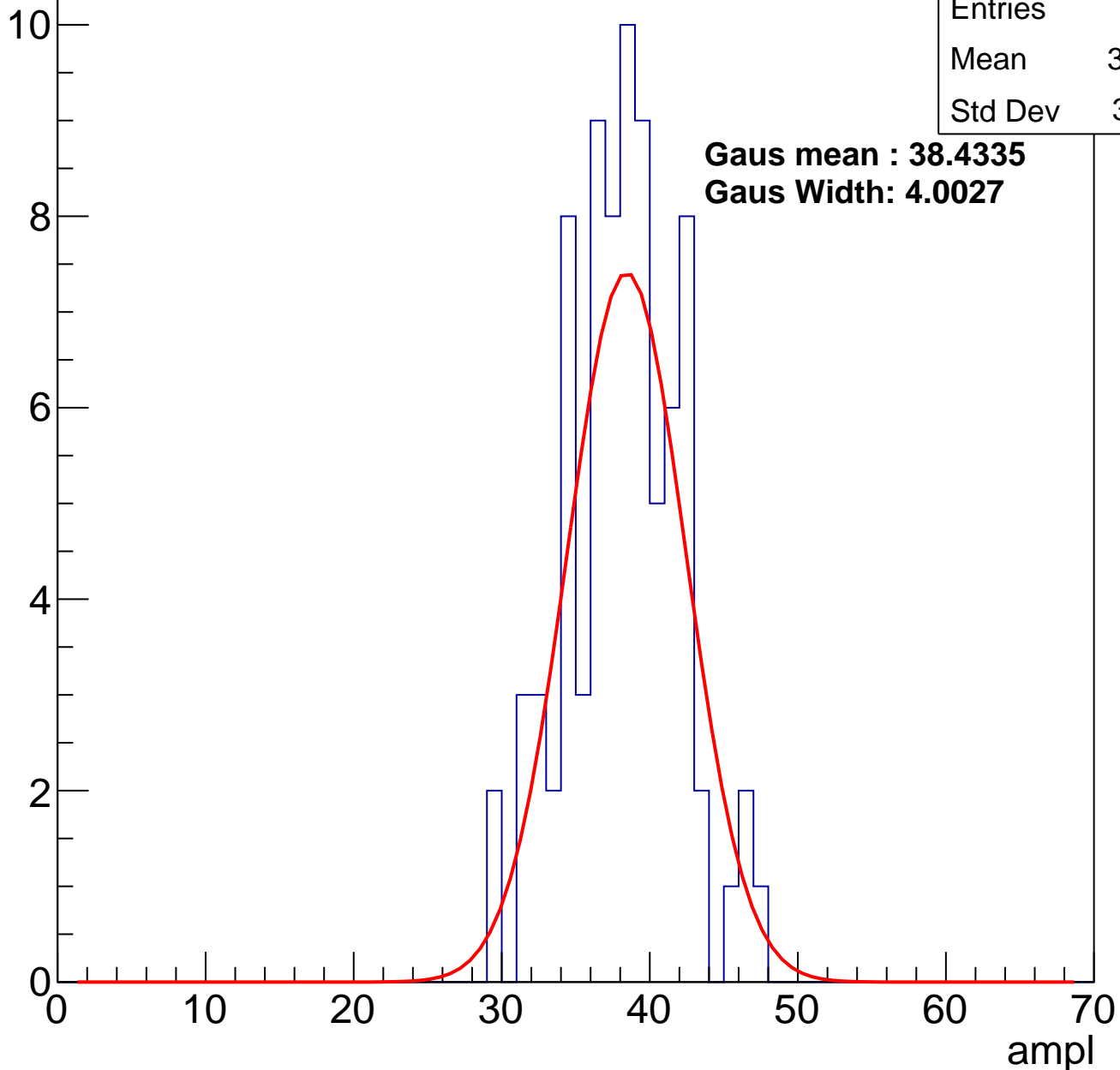
# B0L001S, U5-ch52, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	82
Mean	37.72
Std Dev	3.791

**Gaus mean : 38.4335**  
**Gaus Width: 4.0027**

Entry



# B0L001S, U5-ch52, adc2

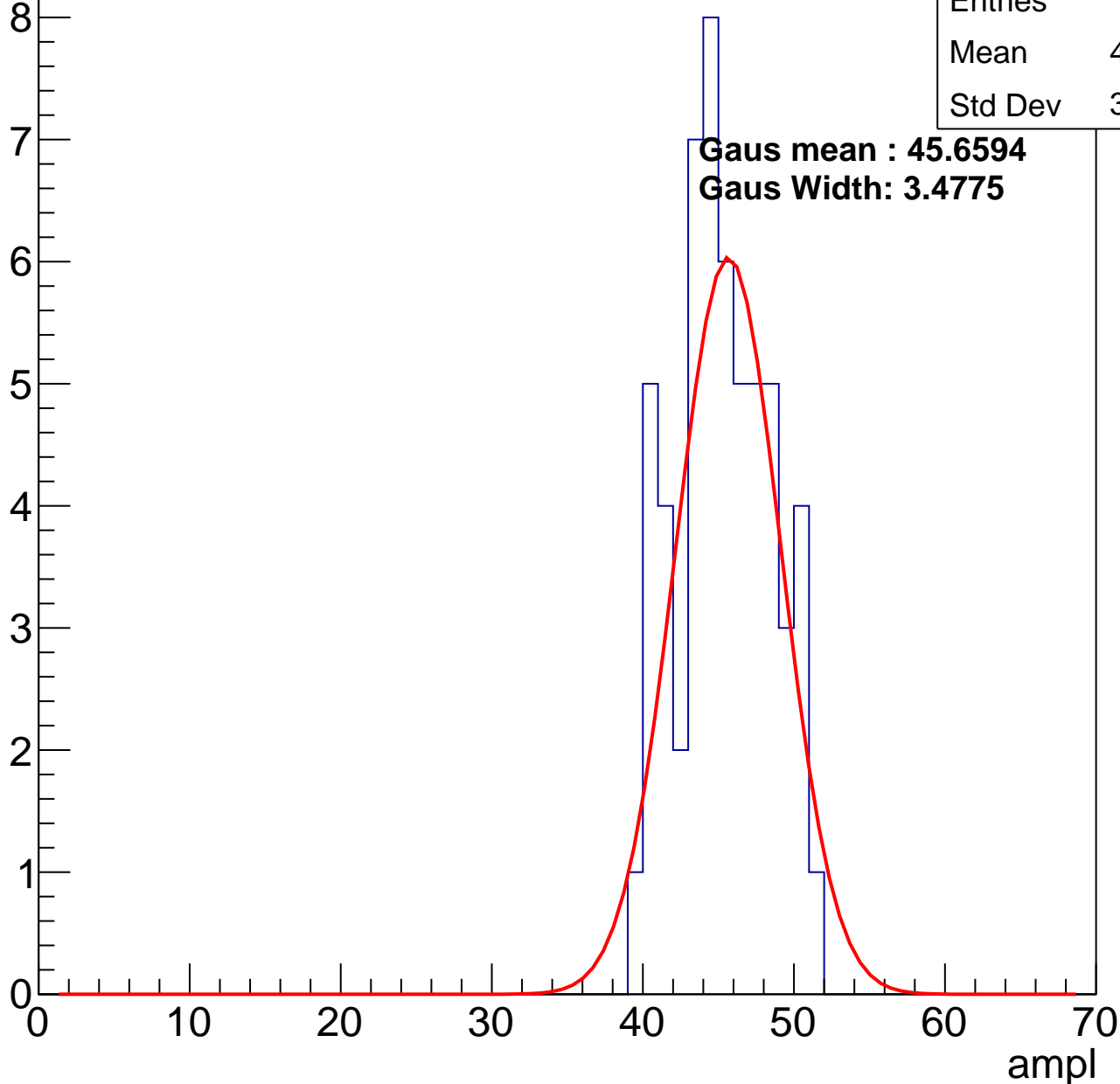
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	44.88
Std Dev	3.083

**Gaus mean : 45.6594**

**Gaus Width: 3.4775**

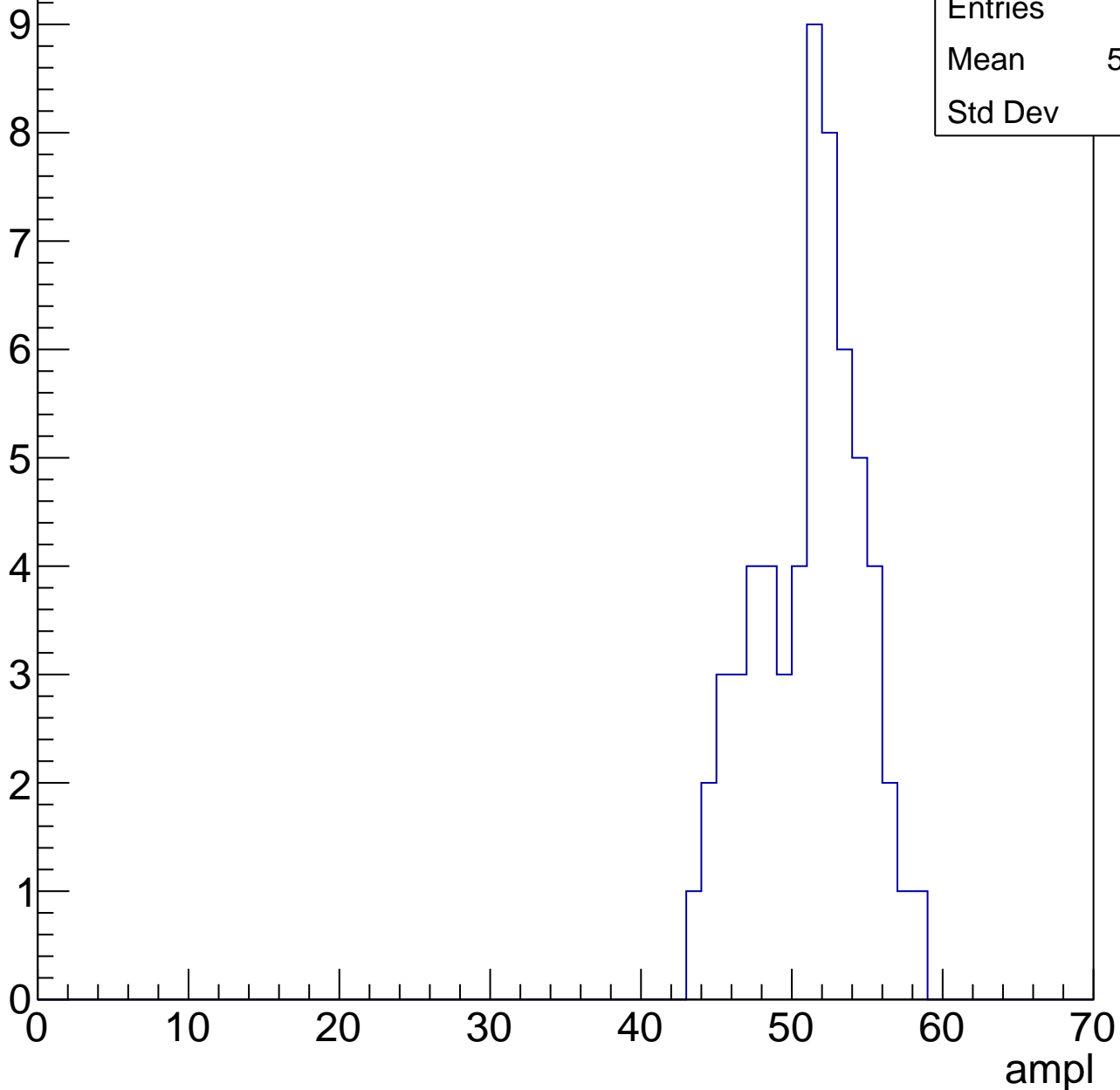


# B0L001S, U5-ch52, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	50.68
Std Dev	3.49

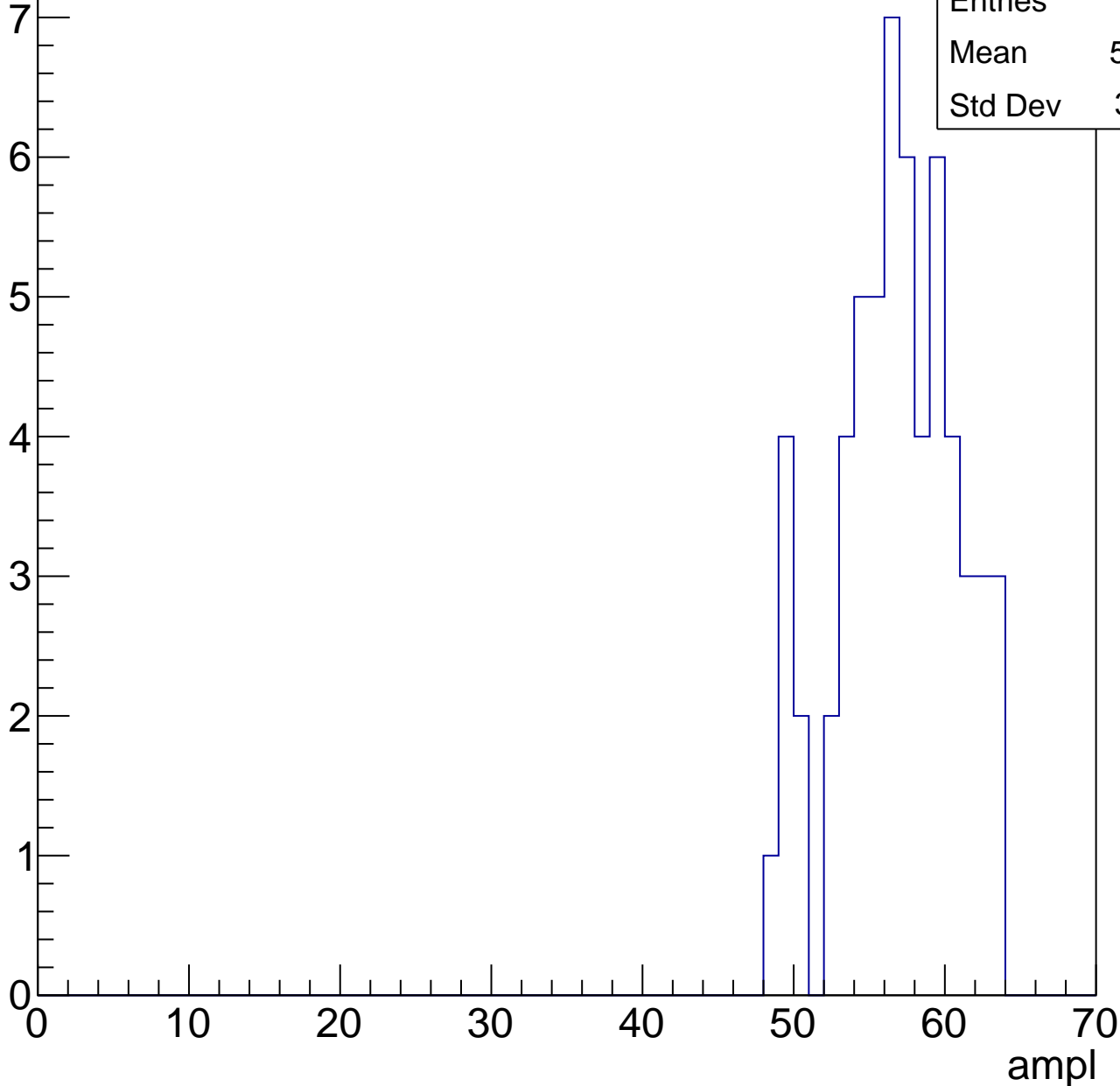


# B0L001S, U5-ch52, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	56.32
Std Dev	3.881

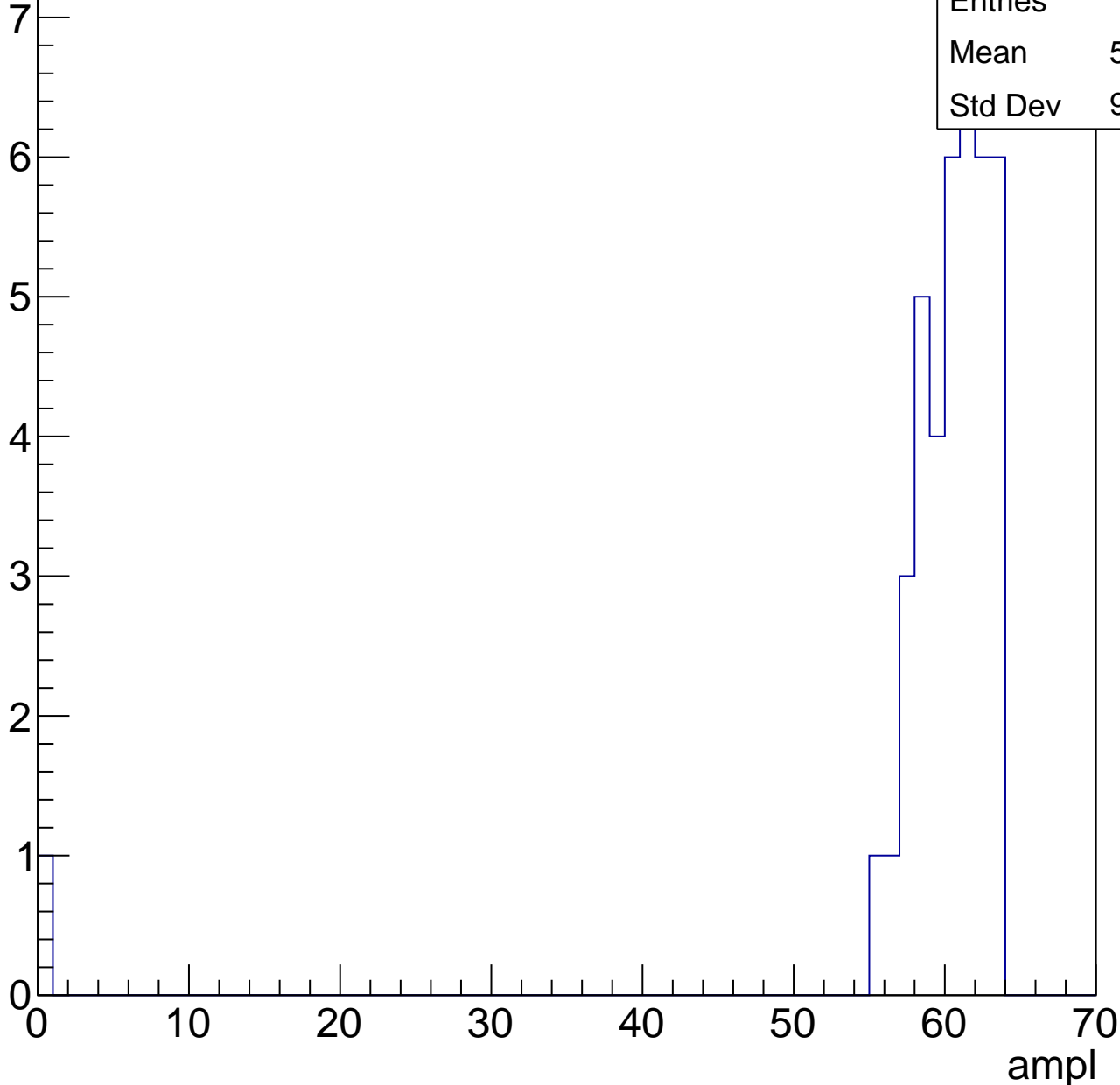


# B0L001S, U5-ch52, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	40
Mean	58.62
Std Dev	9.619



# B0L001S, U5-ch52, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch52, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch53, adc0

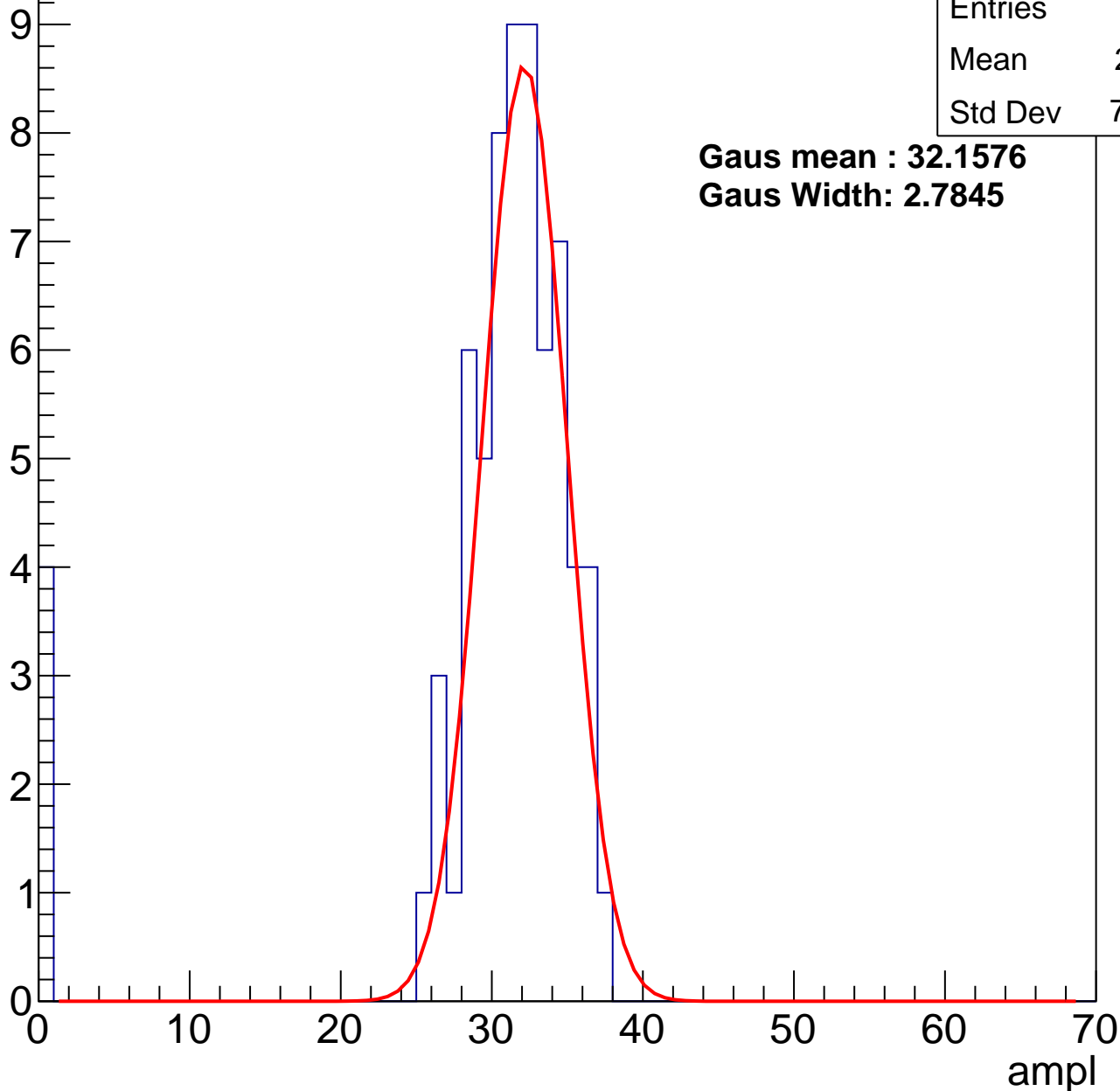
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	29.51
Std Dev	7.858

**Gaus mean : 32.1576**

**Gaus Width: 2.7845**



# B0L001S, U5-ch53, adc1

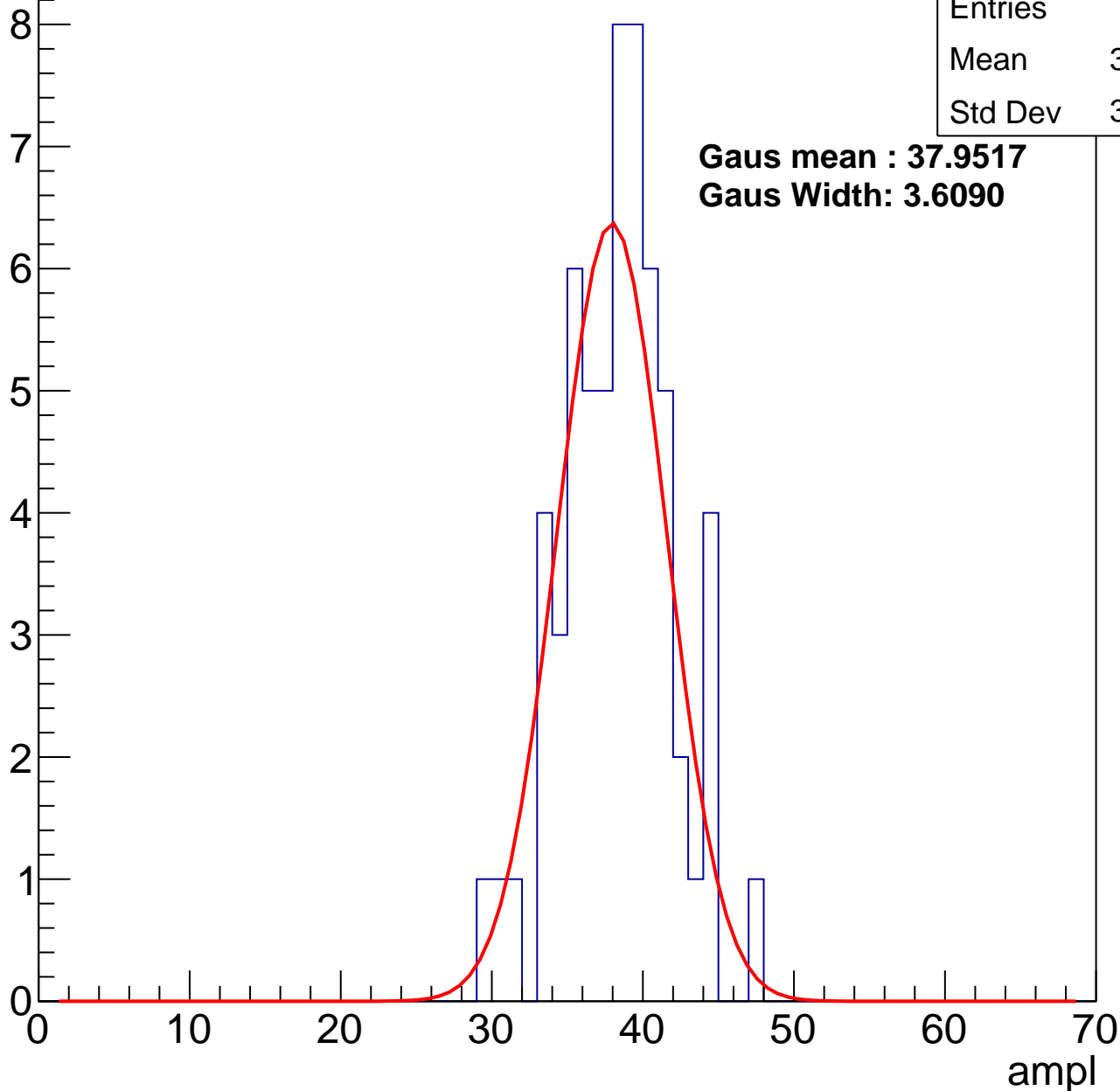
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	37.87
Std Dev	3.573

**Gaus mean : 37.9517**

**Gaus Width: 3.6090**



# B0L001S, U5-ch53, adc2

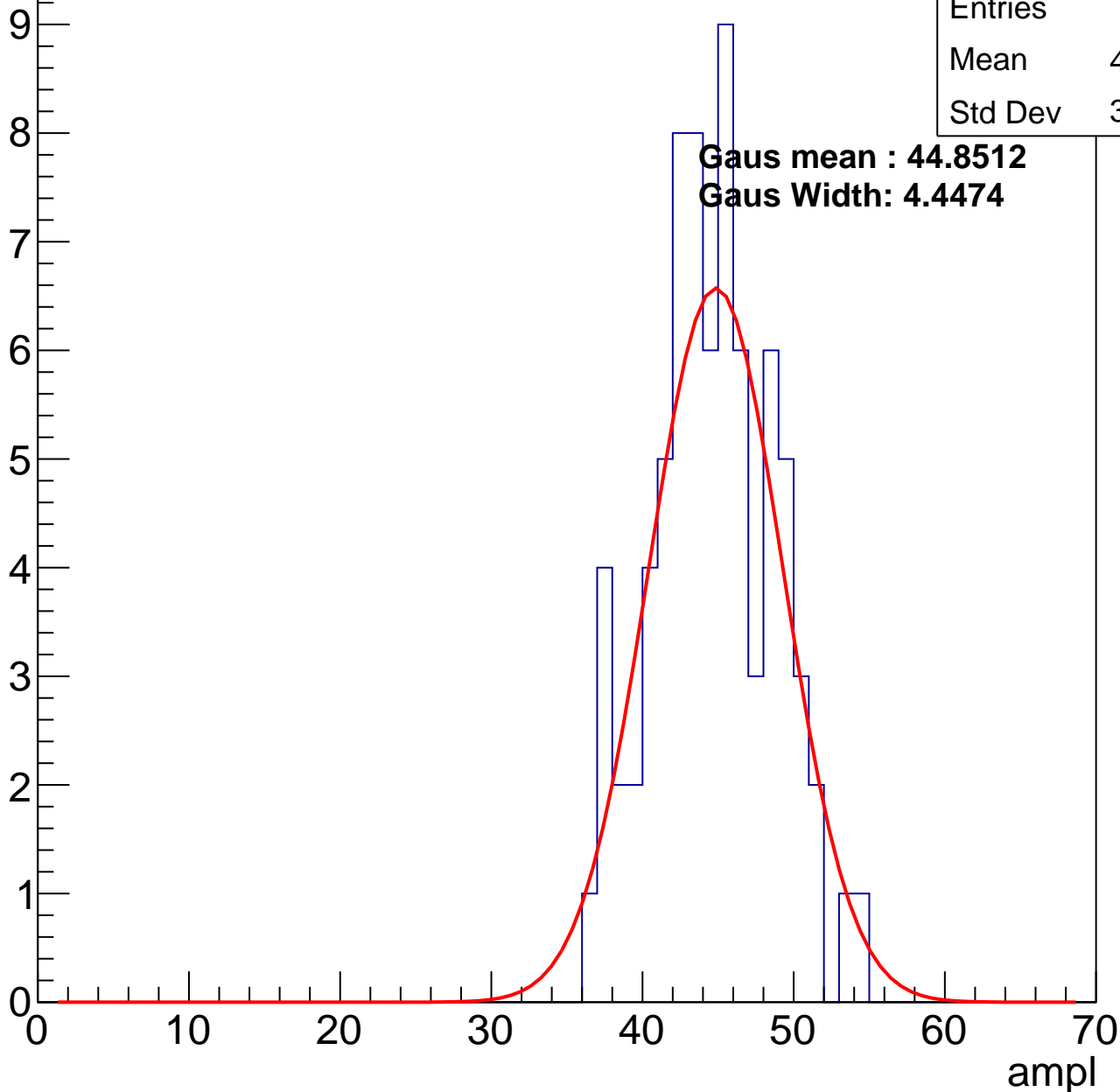
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	76
Mean	44.22
Std Dev	3.966

**Gaus mean : 44.8512**

**Gaus Width: 4.4474**

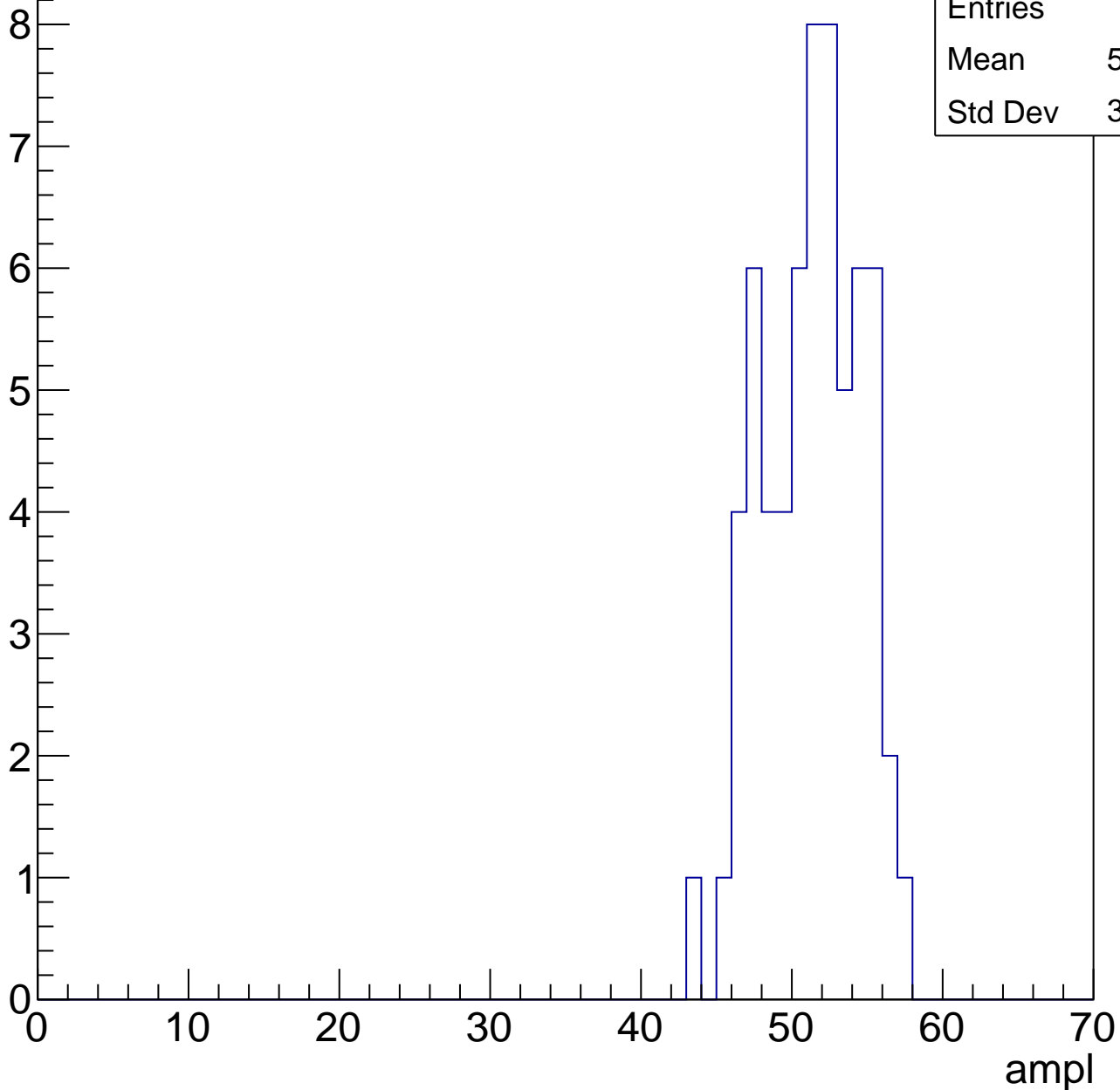


# B0L001S, U5-ch53, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	50.87
Std Dev	3.155

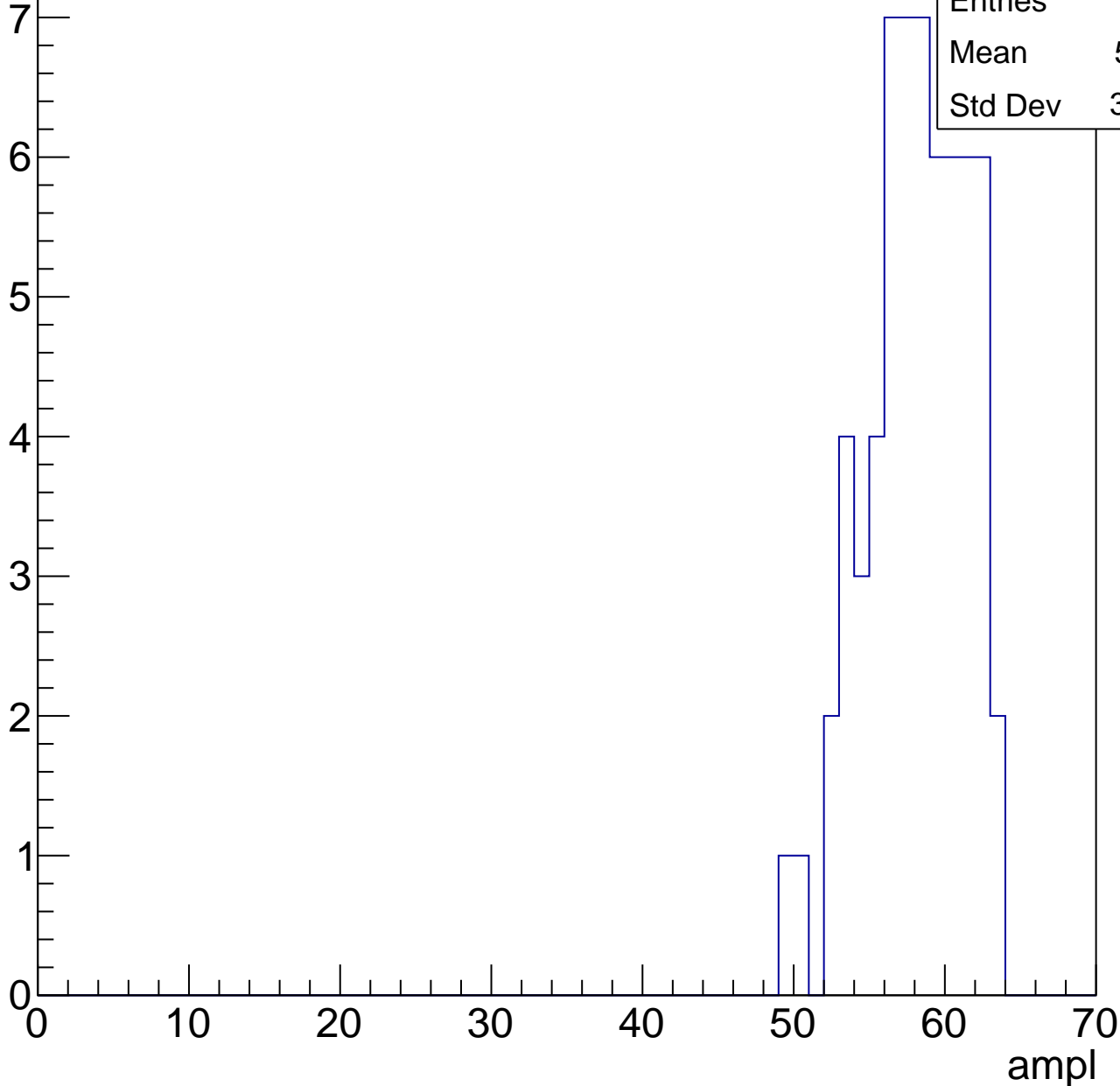


# B0L001S, U5-ch53, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	57.61
Std Dev	3.255

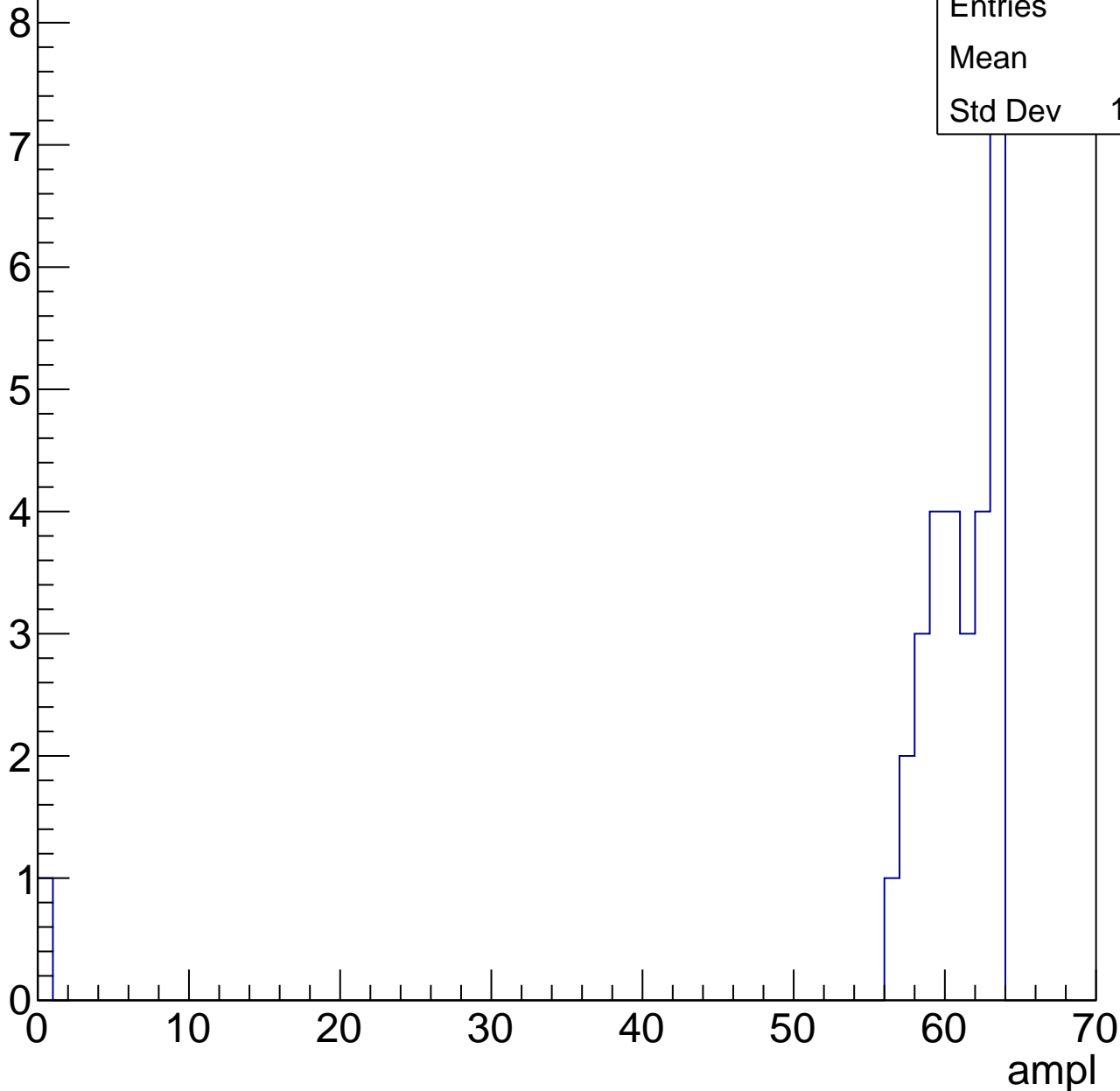


# B0L001S, U5-ch53, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	30
Mean	58.5
Std Dev	11.07



# B0L001S, U5-ch53, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch53, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U5-ch54, adc0

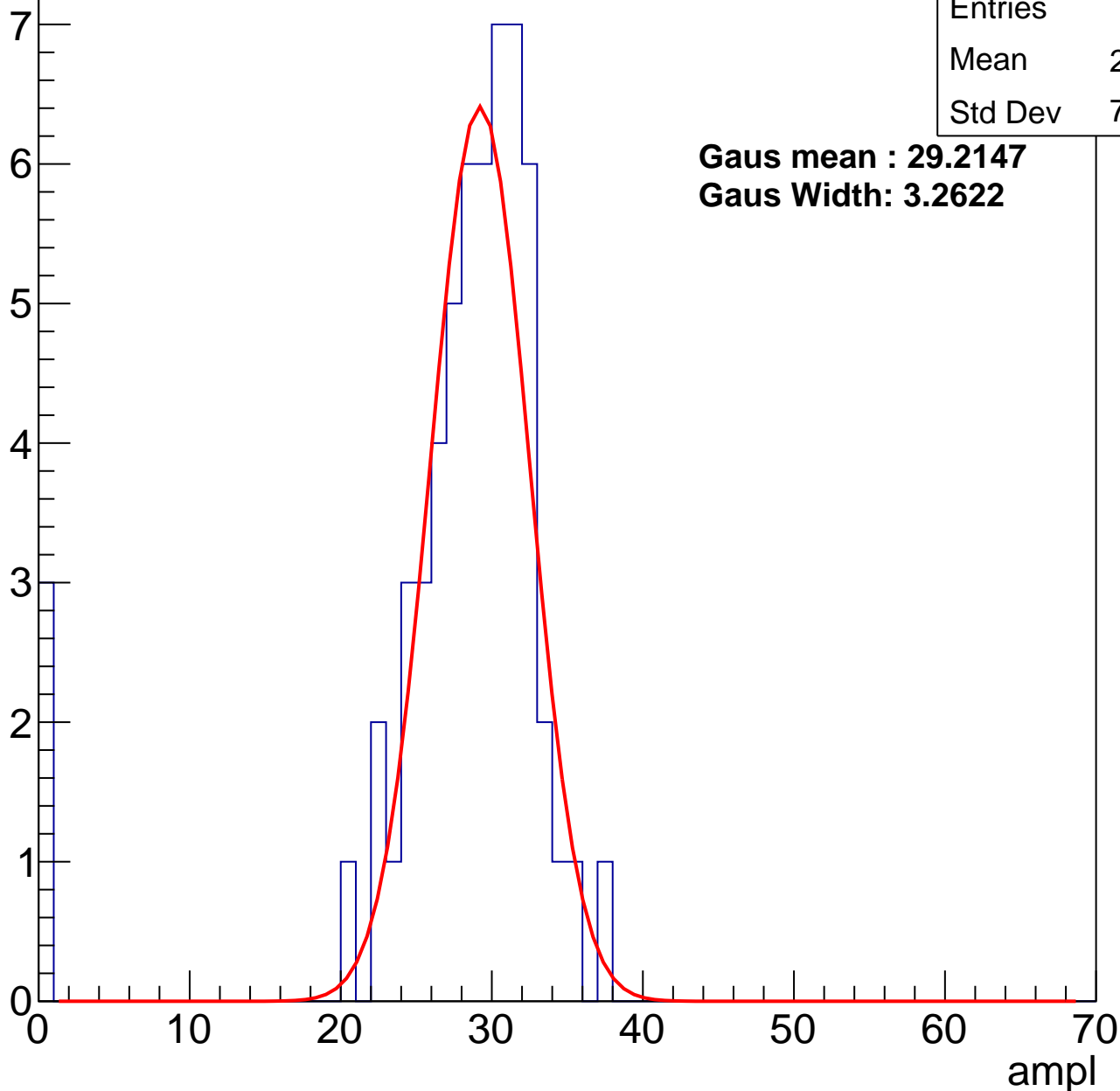
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	27.22
Std Dev	7.109

**Gaus mean : 29.2147**

**Gaus Width: 3.2622**



# B0L001S, U5-ch54, adc1

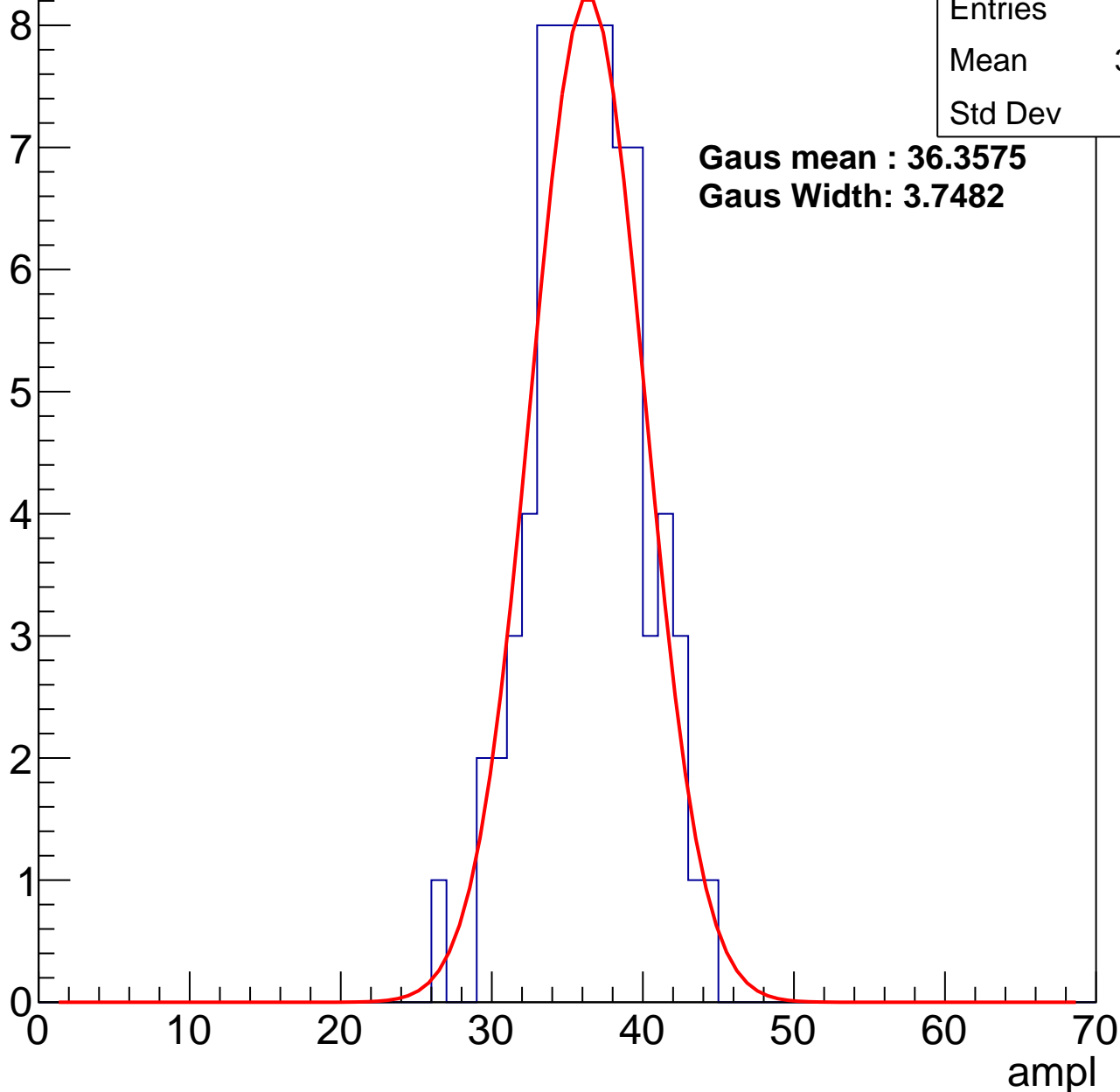
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	78
Mean	35.91
Std Dev	3.56

**Gaus mean : 36.3575**

**Gaus Width: 3.7482**



# B0L001S, U5-ch54, adc2

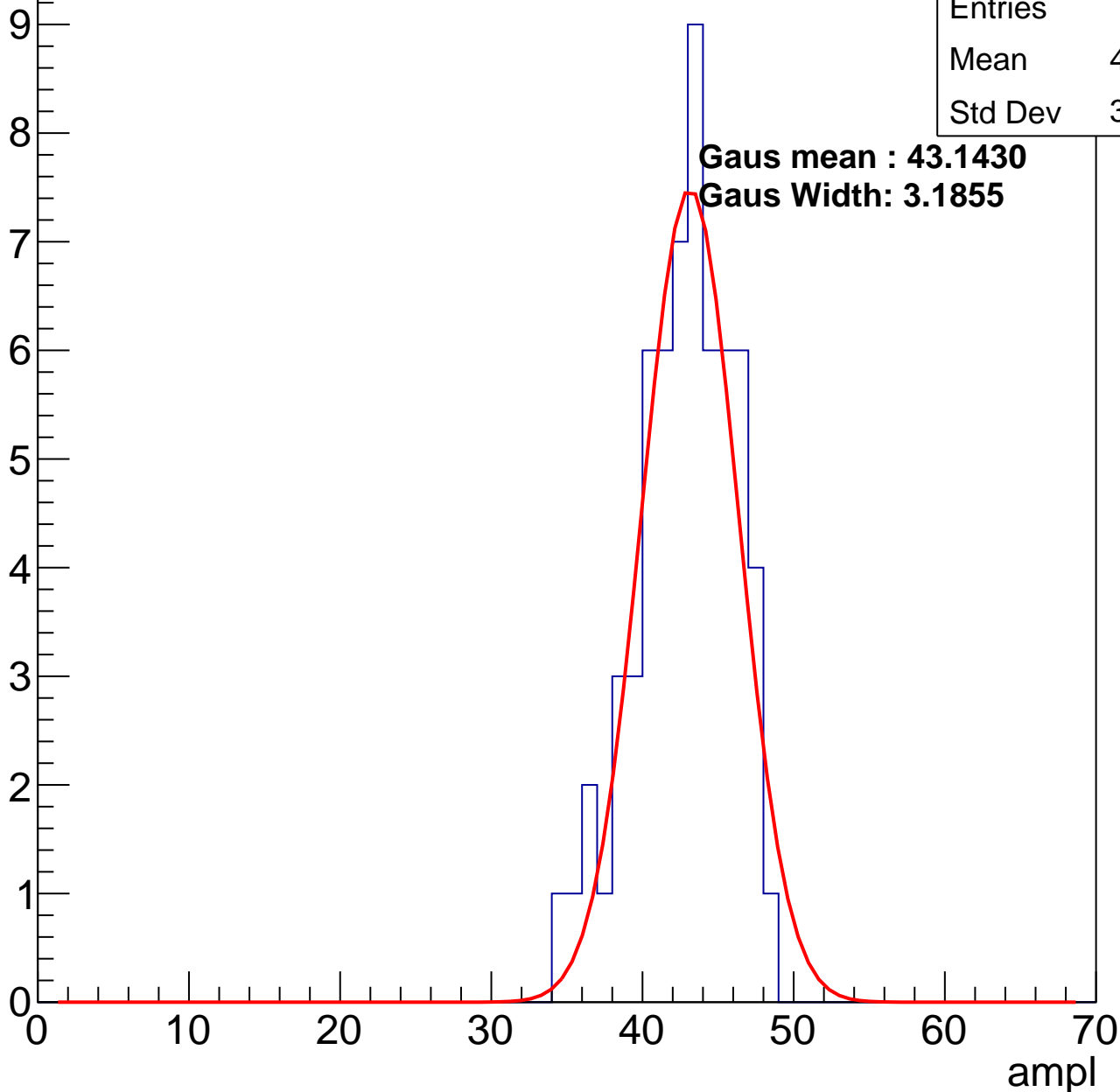
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	42.29
Std Dev	3.185

**Gaus mean : 43.1430**

**Gaus Width: 3.1855**

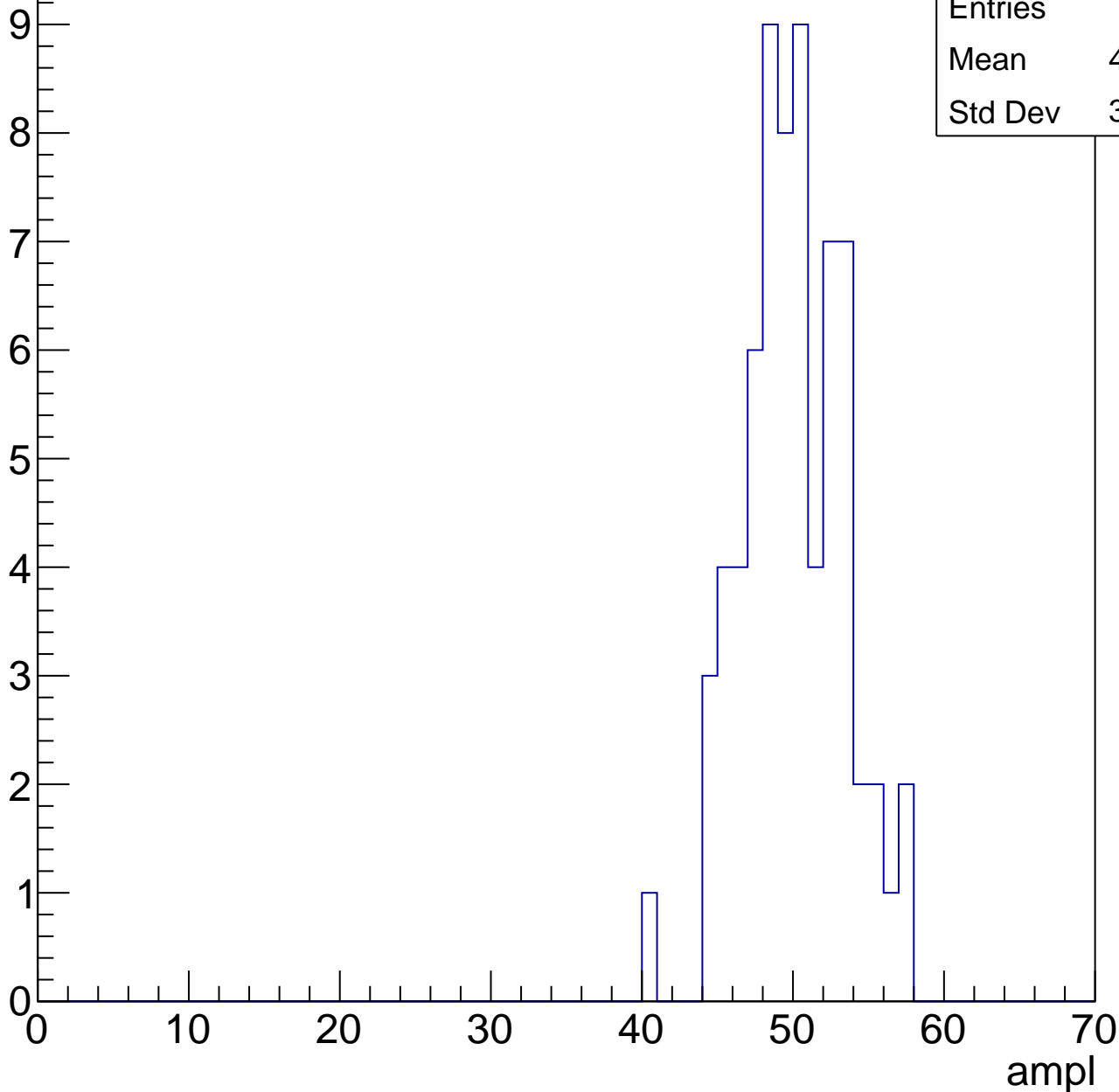


# B0L001S, U5-ch54, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	49.55
Std Dev	3.334

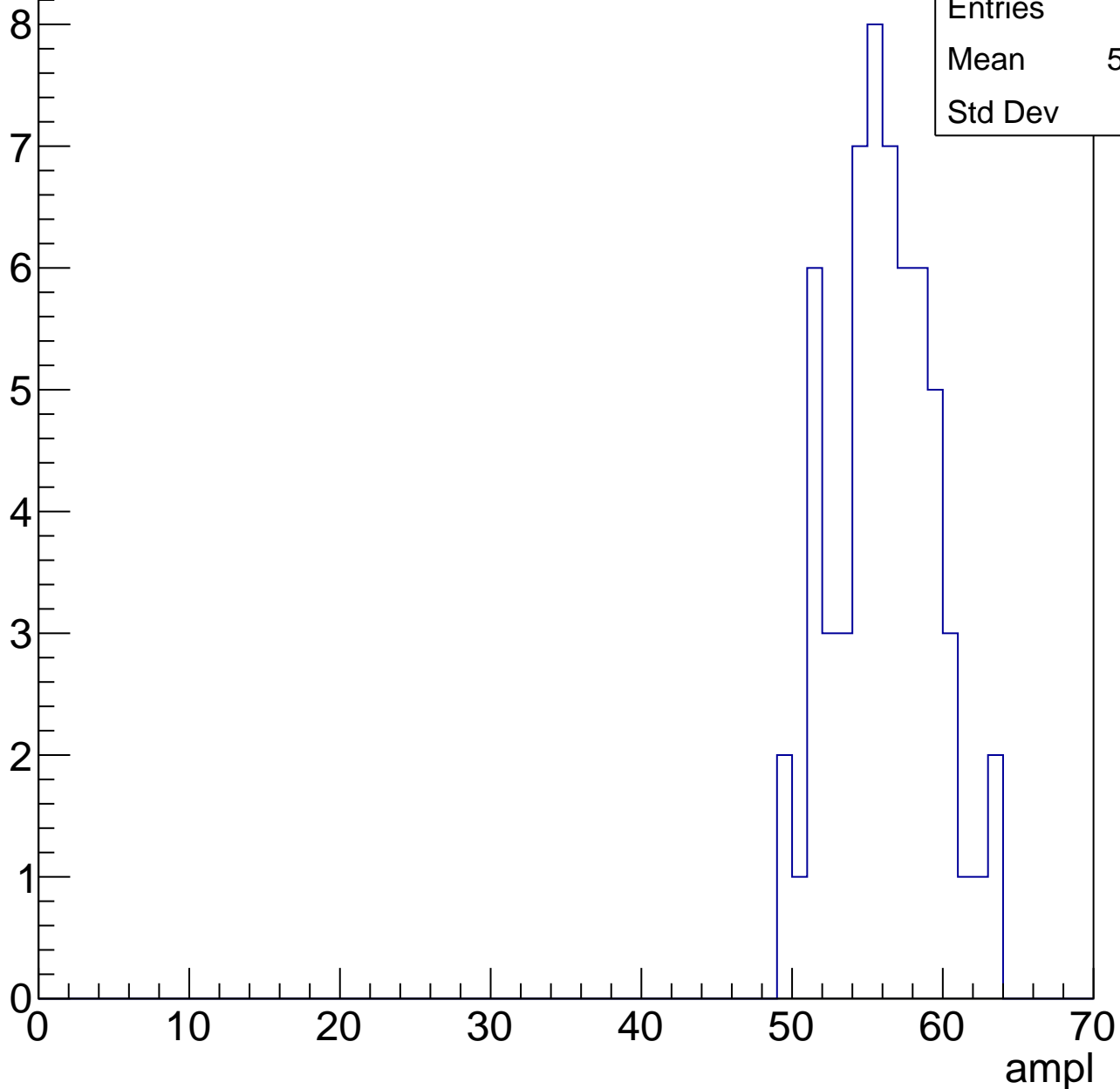


# B0L001S, U5-ch54, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	55.62
Std Dev	3.31

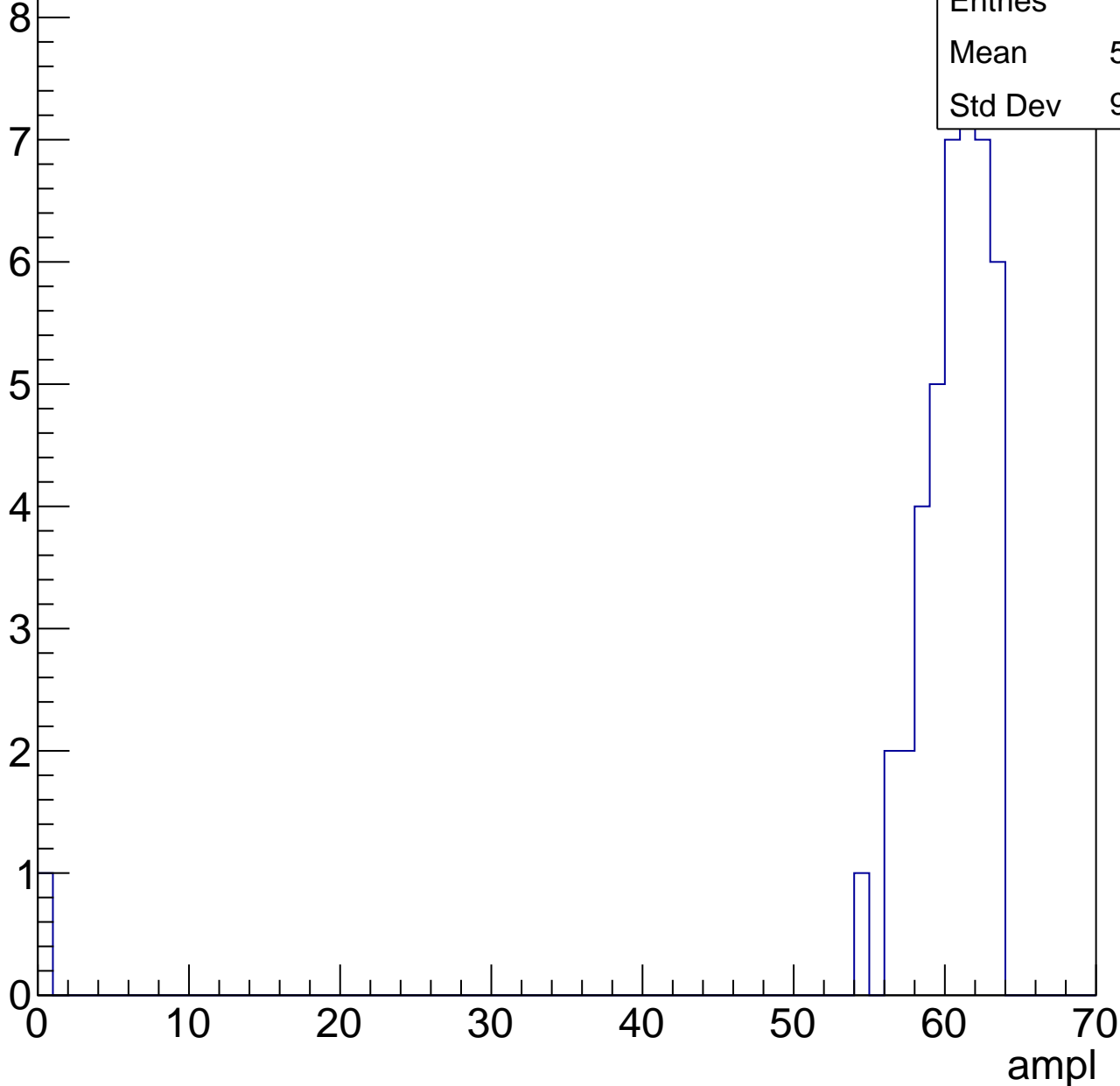


# B0L001S, U5-ch54, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	43
Mean	58.77
Std Dev	9.316



# B0L001S, U5-ch54, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch54, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L001S, U5-ch55, adc0

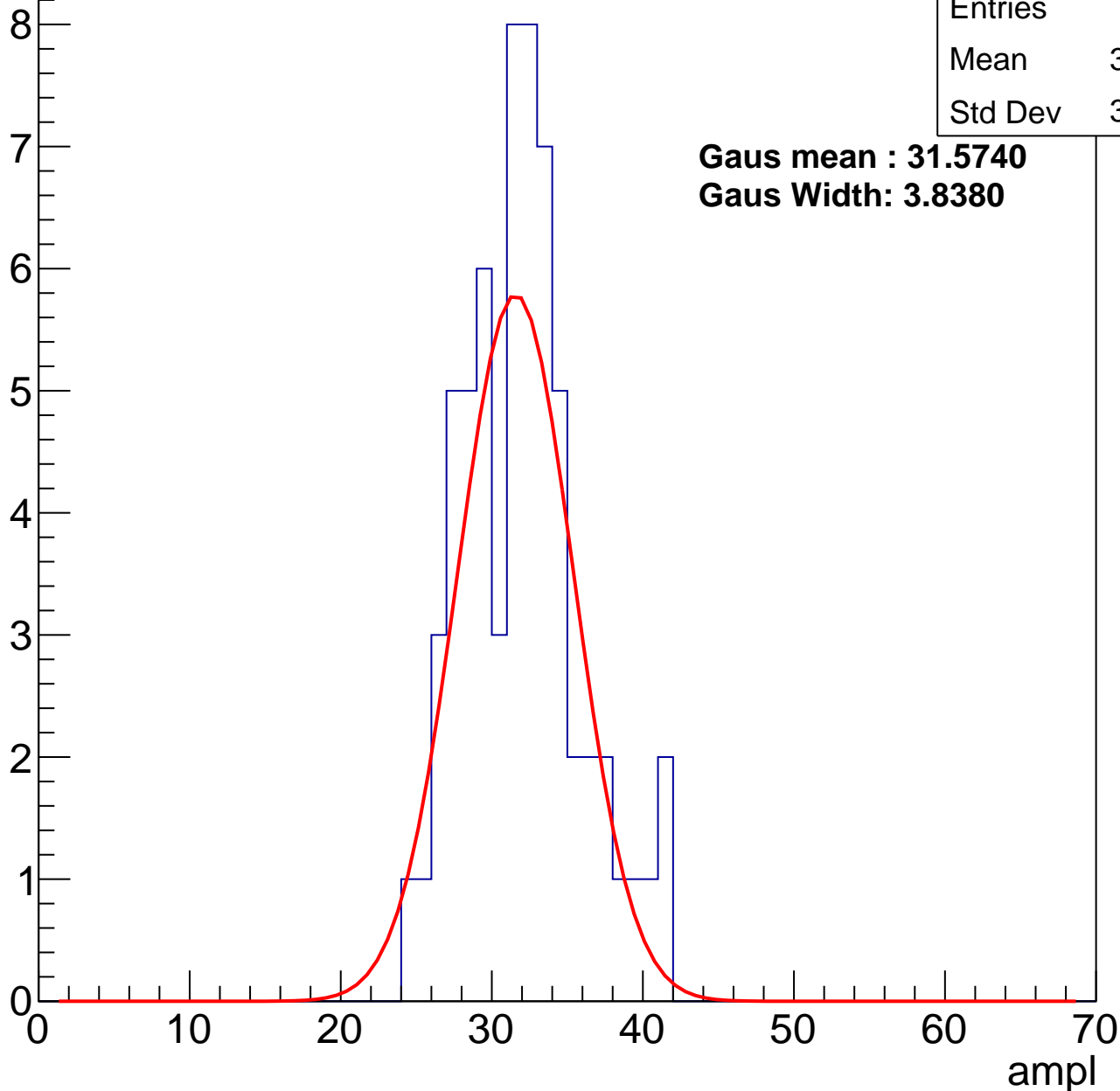
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	31.52
Std Dev	3.829

**Gaus mean : 31.5740**

**Gaus Width: 3.8380**



# B0L001S, U5-ch55, adc1

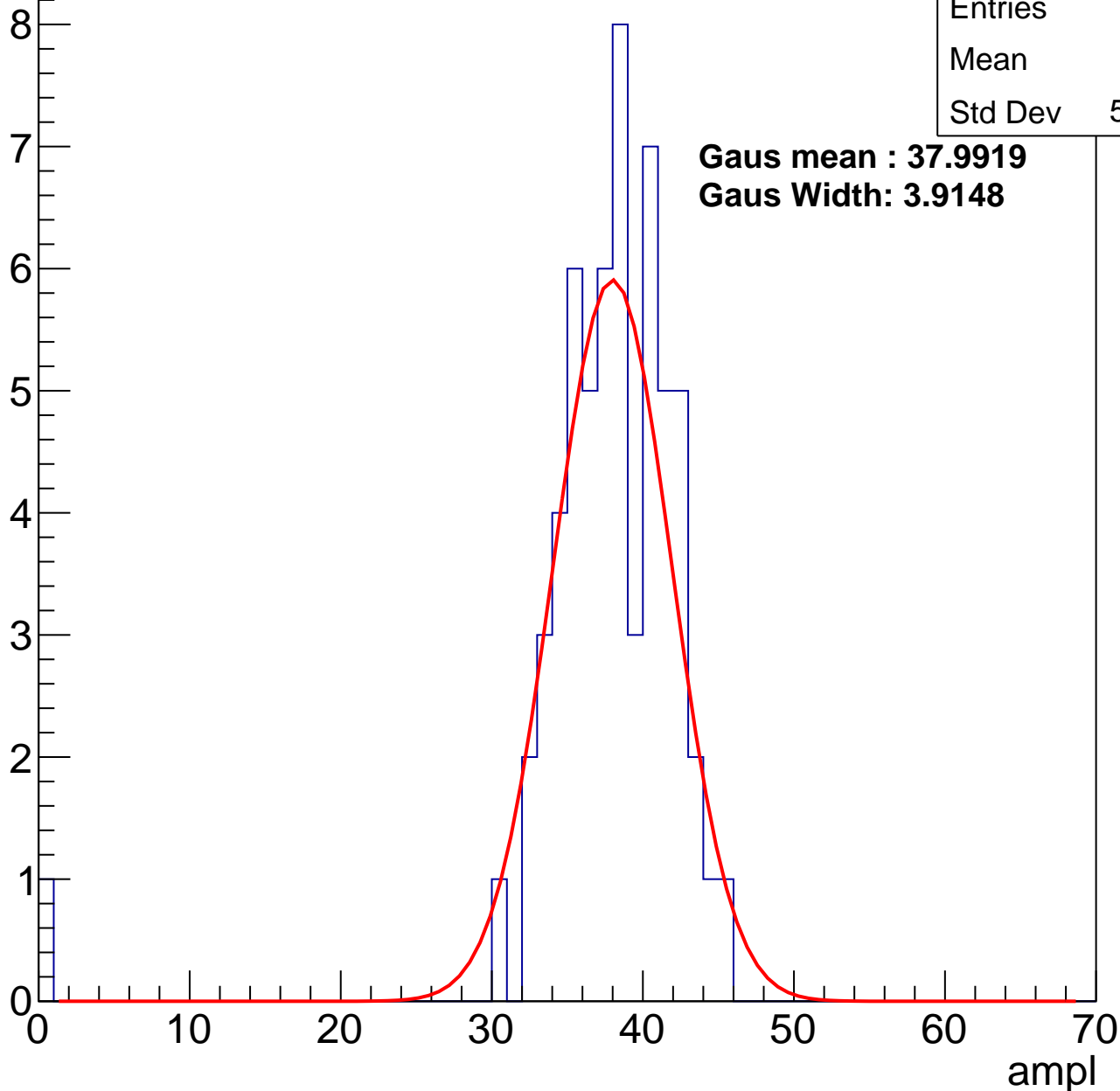
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	37.2
Std Dev	5.848

**Gaus mean : 37.9919**

**Gaus Width: 3.9148**



# B0L001S, U5-ch55, adc2

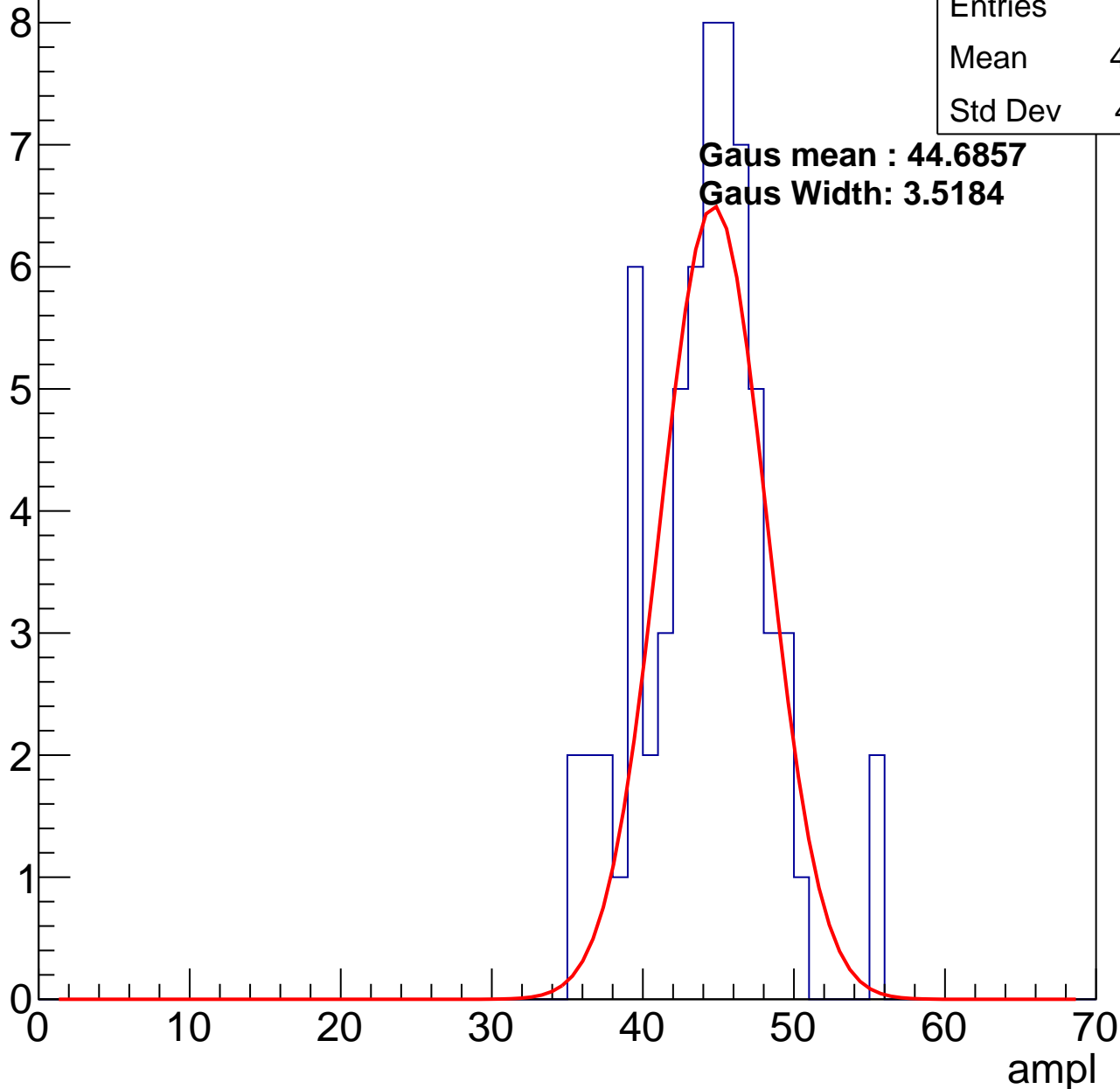
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	43.62
Std Dev	4.141

**Gaus mean : 44.6857**

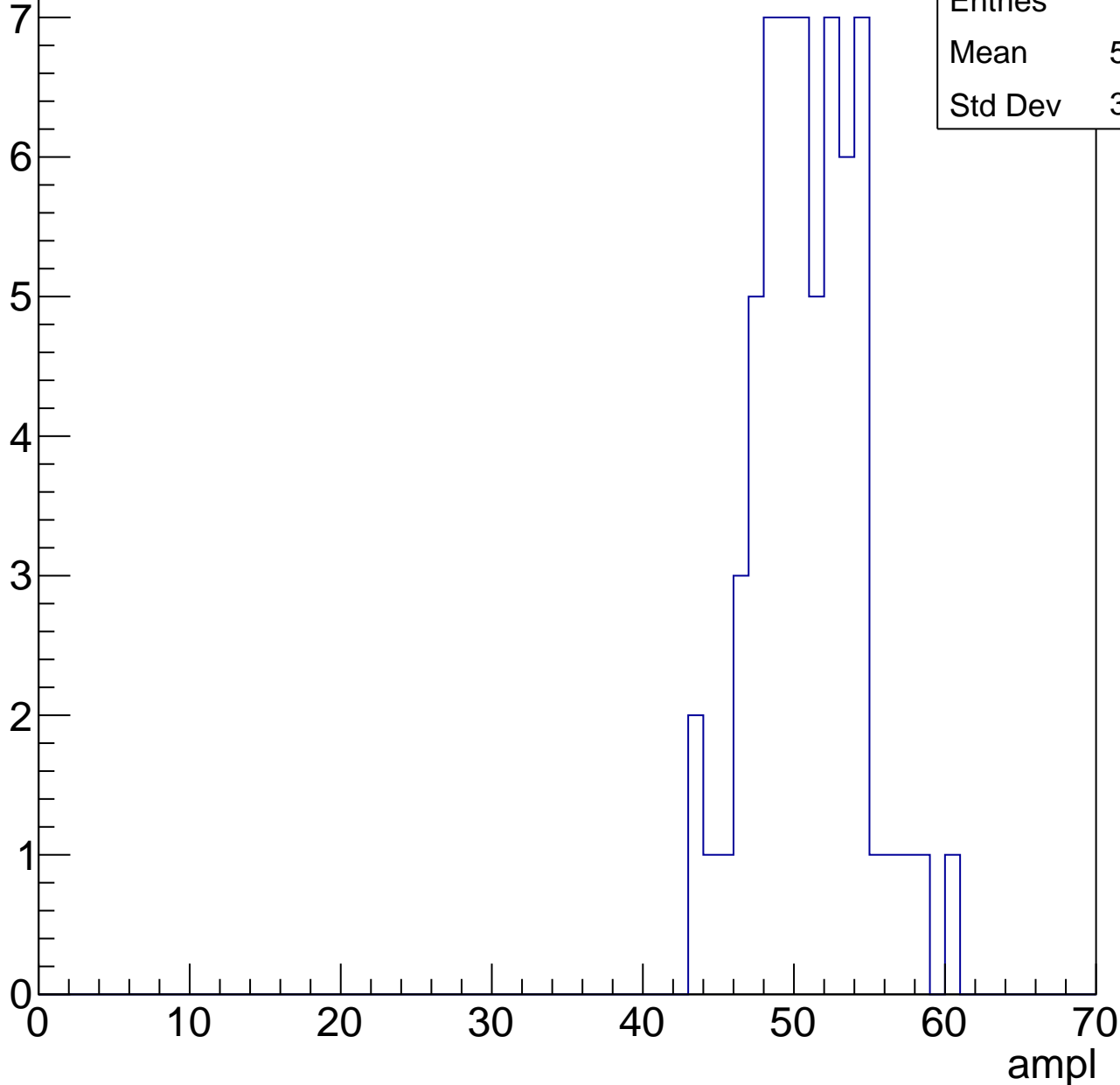
**Gaus Width: 3.5184**



# B0L001S, U5-ch55, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

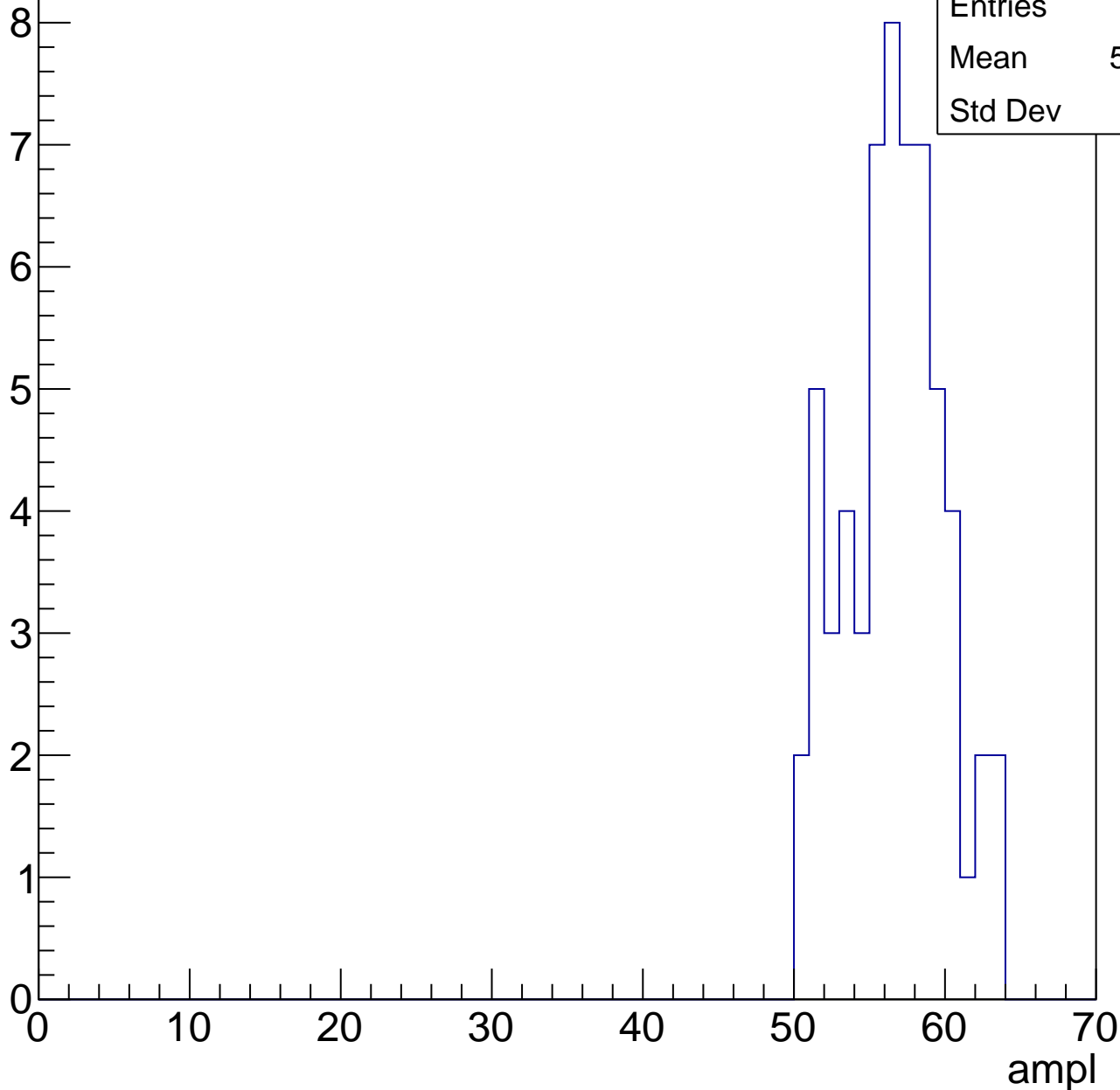


# B0L001S, U5-ch55, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	56.15
Std Dev	3.26



# B0L001S, U5-ch55, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

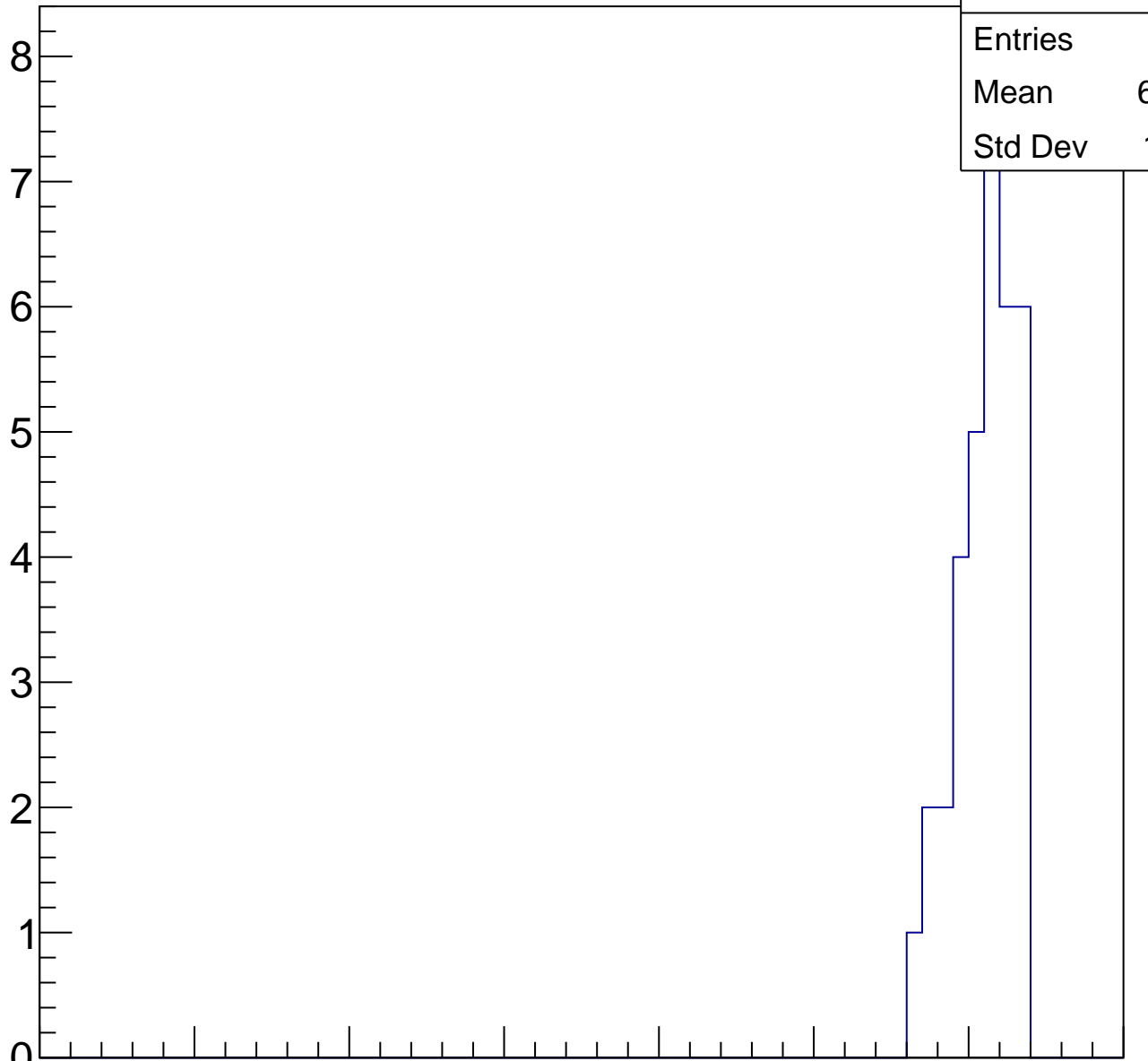
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	34
Mean	60.59
Std Dev	1.881

ampl

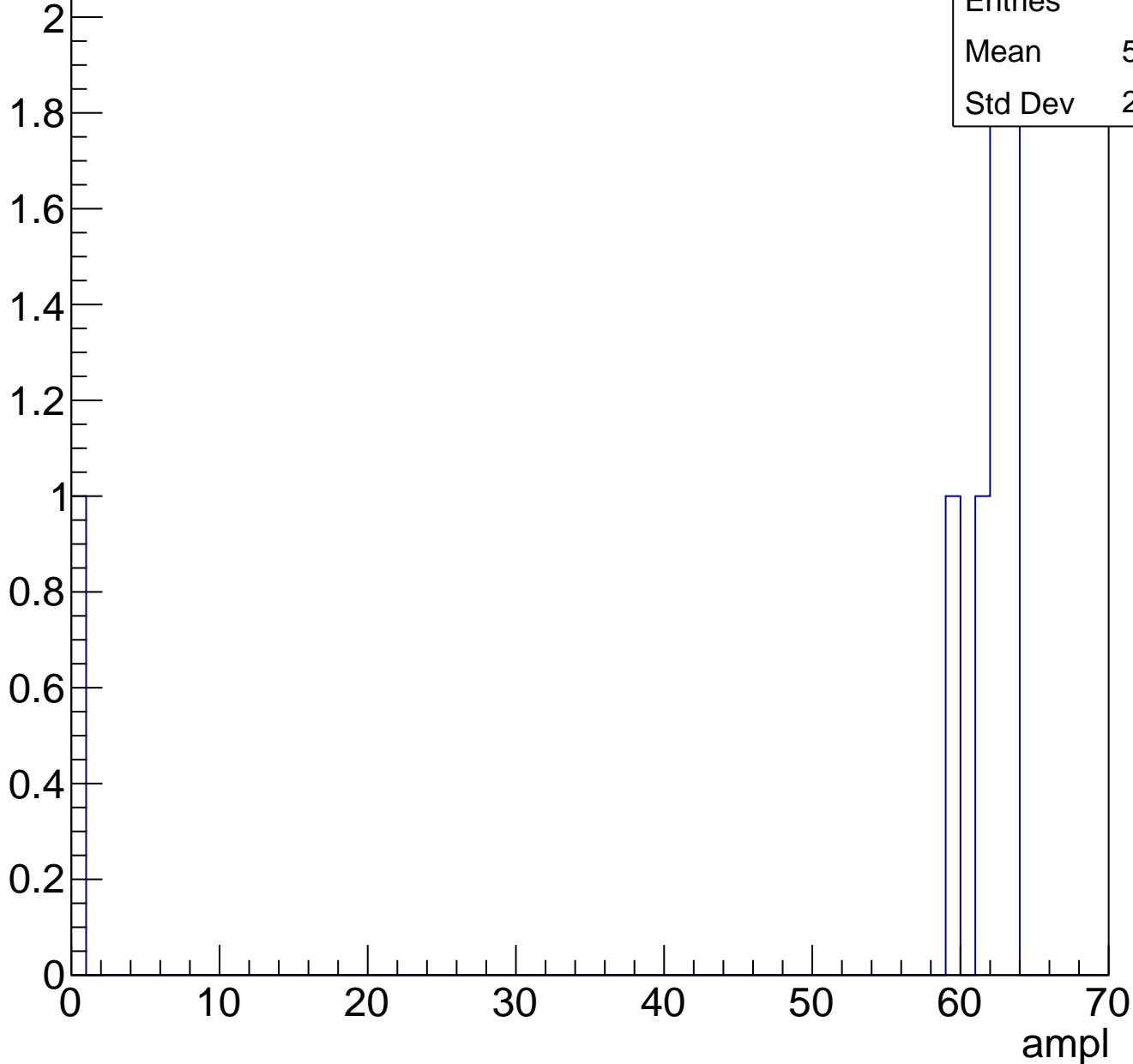
0 10 20 30 40 50 60 70



# B0L001S, U5-ch55, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch55, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U5-ch56, adc0

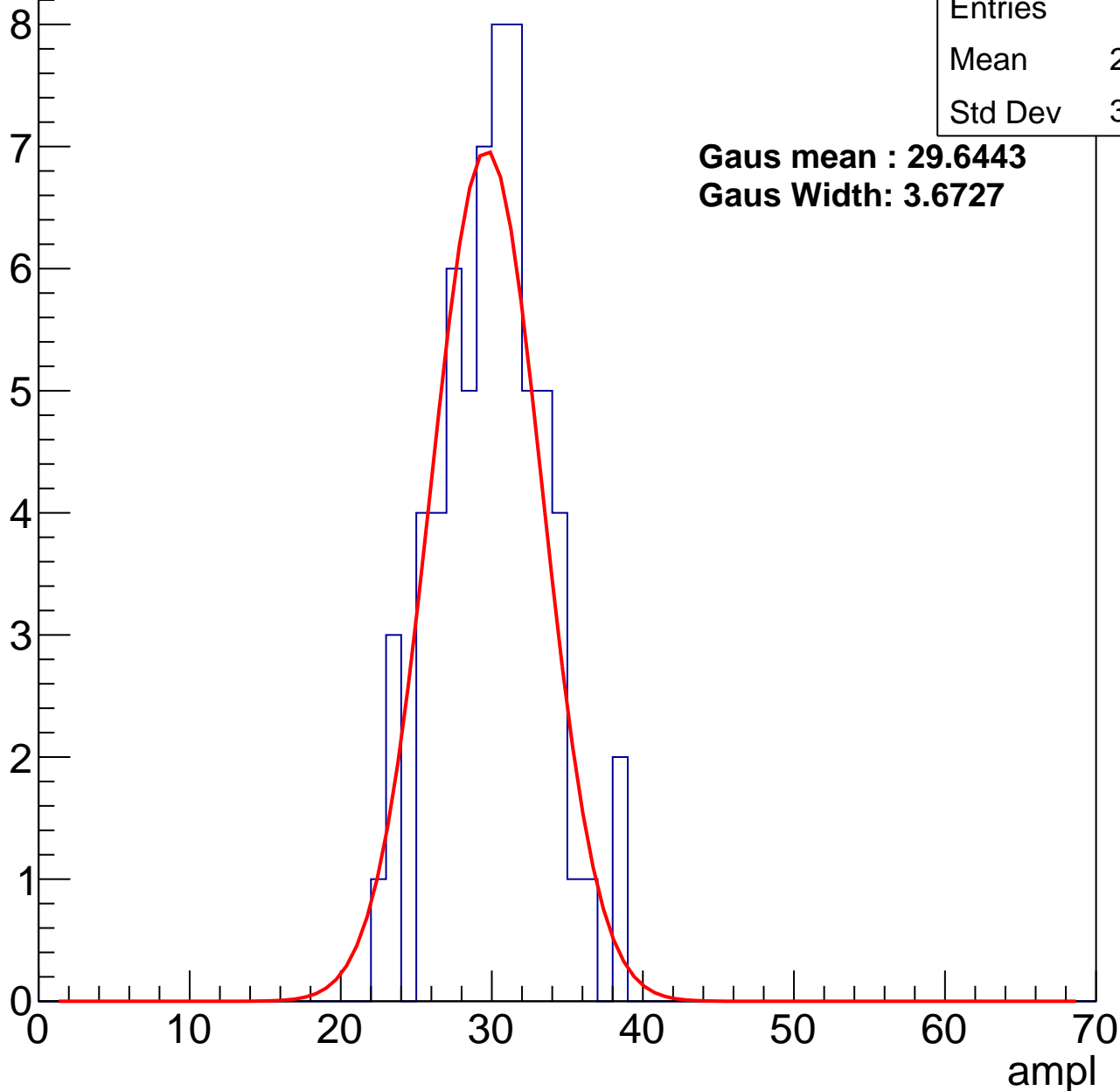
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	29.62
Std Dev	3.475

**Gaus mean : 29.6443**

**Gaus Width: 3.6727**



# B0L001S, U5-ch56, adc1

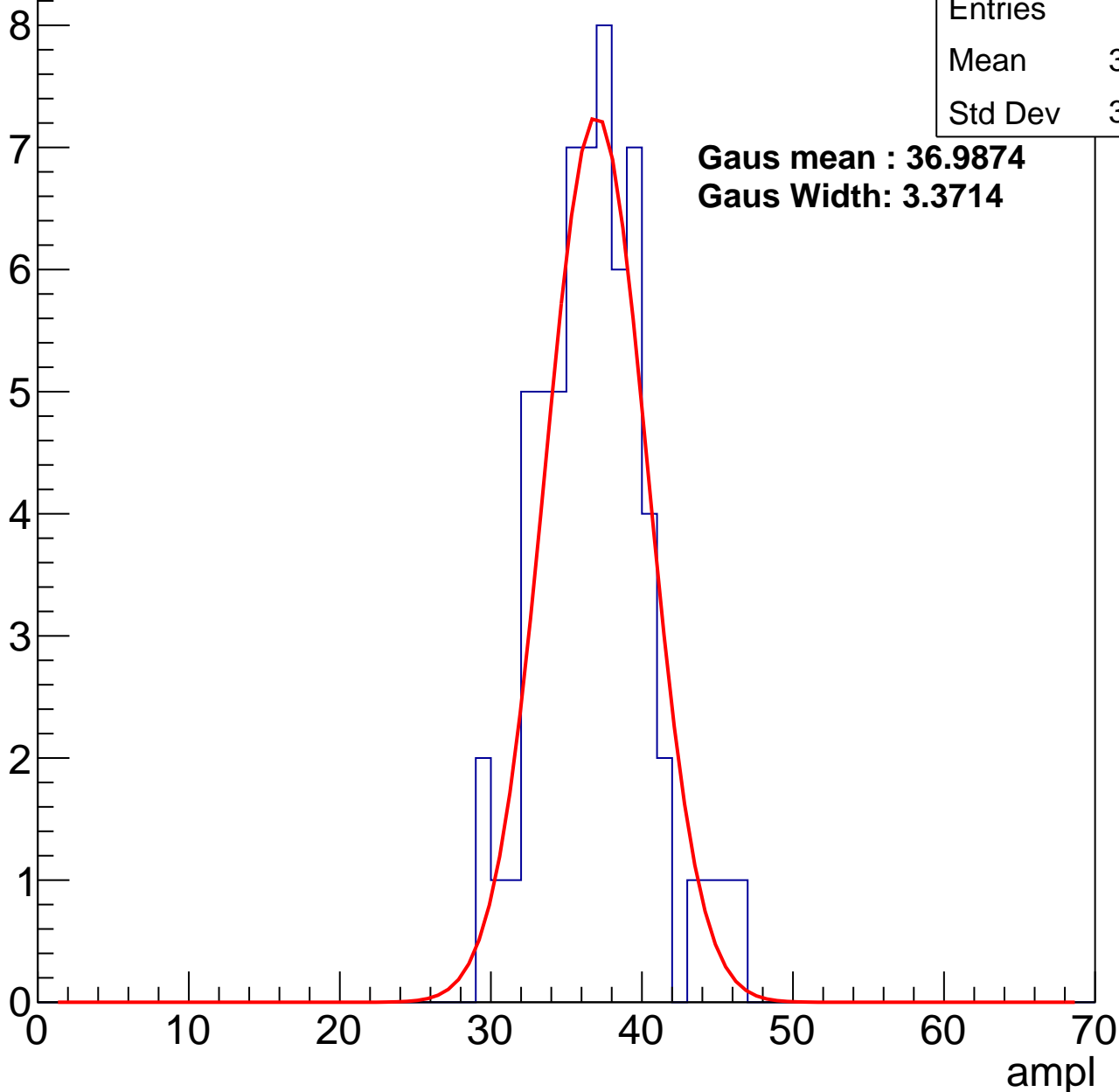
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	36.38
Std Dev	3.547

**Gaus mean : 36.9874**

**Gaus Width: 3.3714**

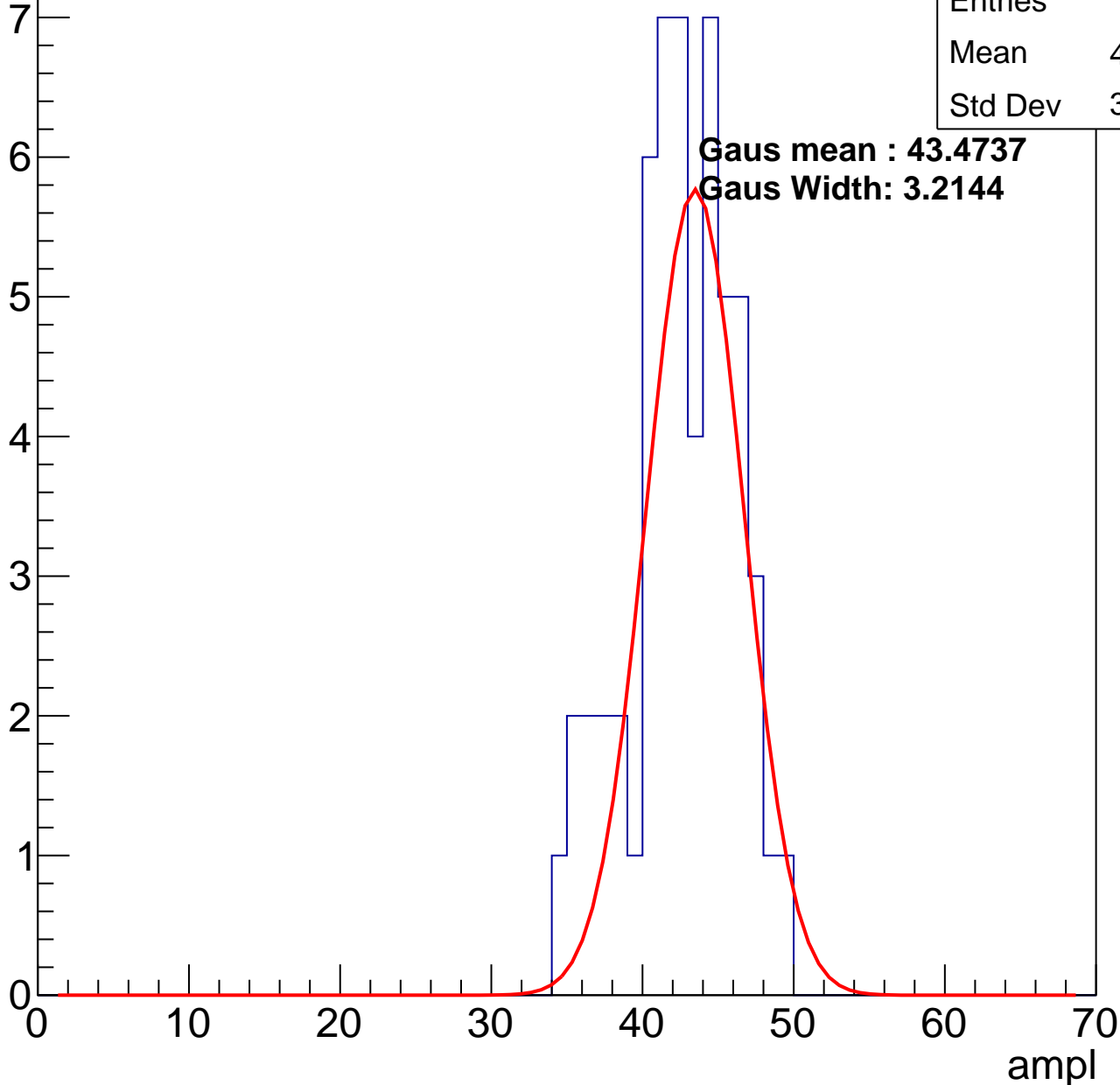


# B0L001S, U5-ch56, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	42.12
Std Dev	3.464

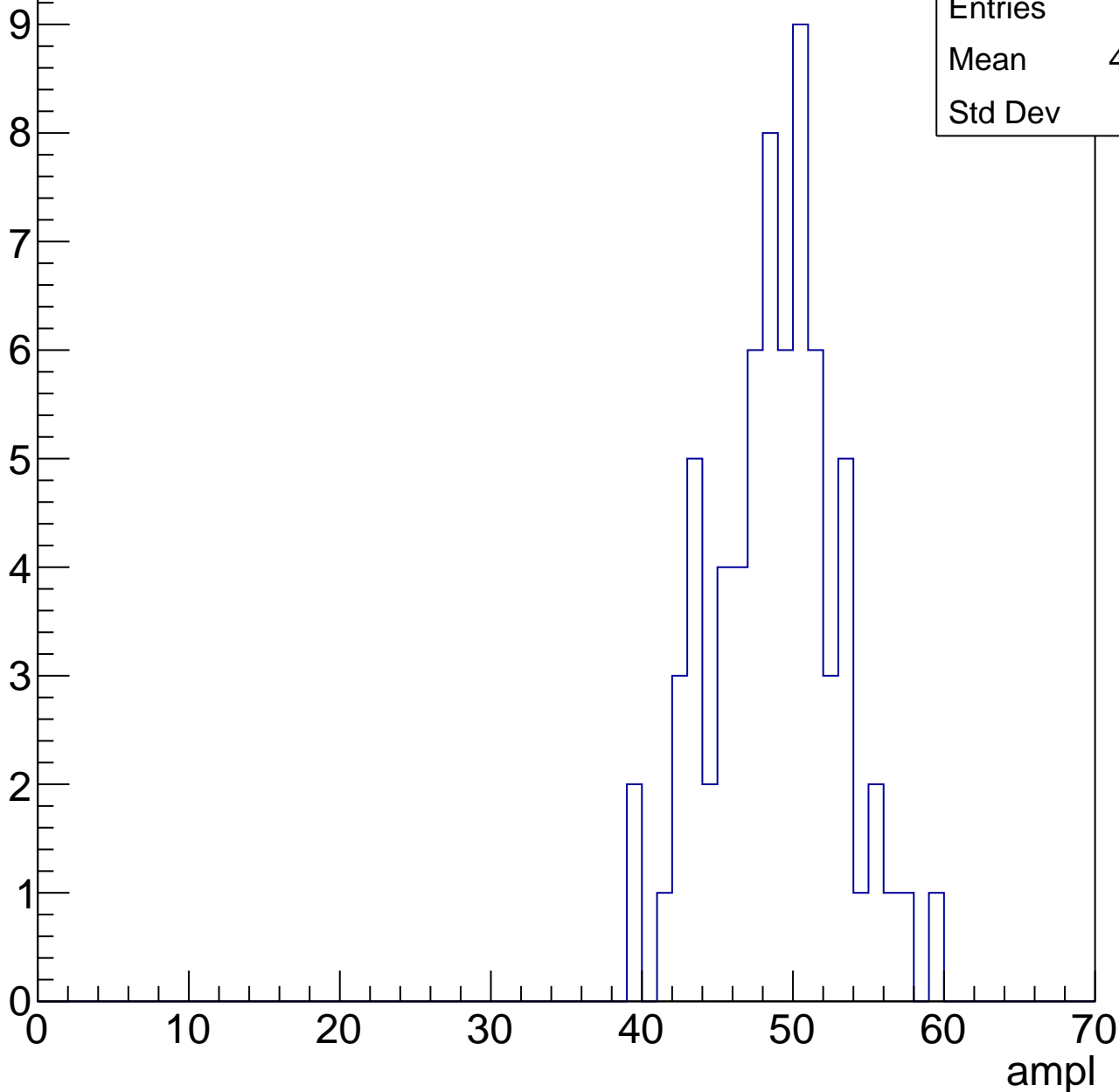


# B0L001S, U5-ch56, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	48.36
Std Dev	4.13

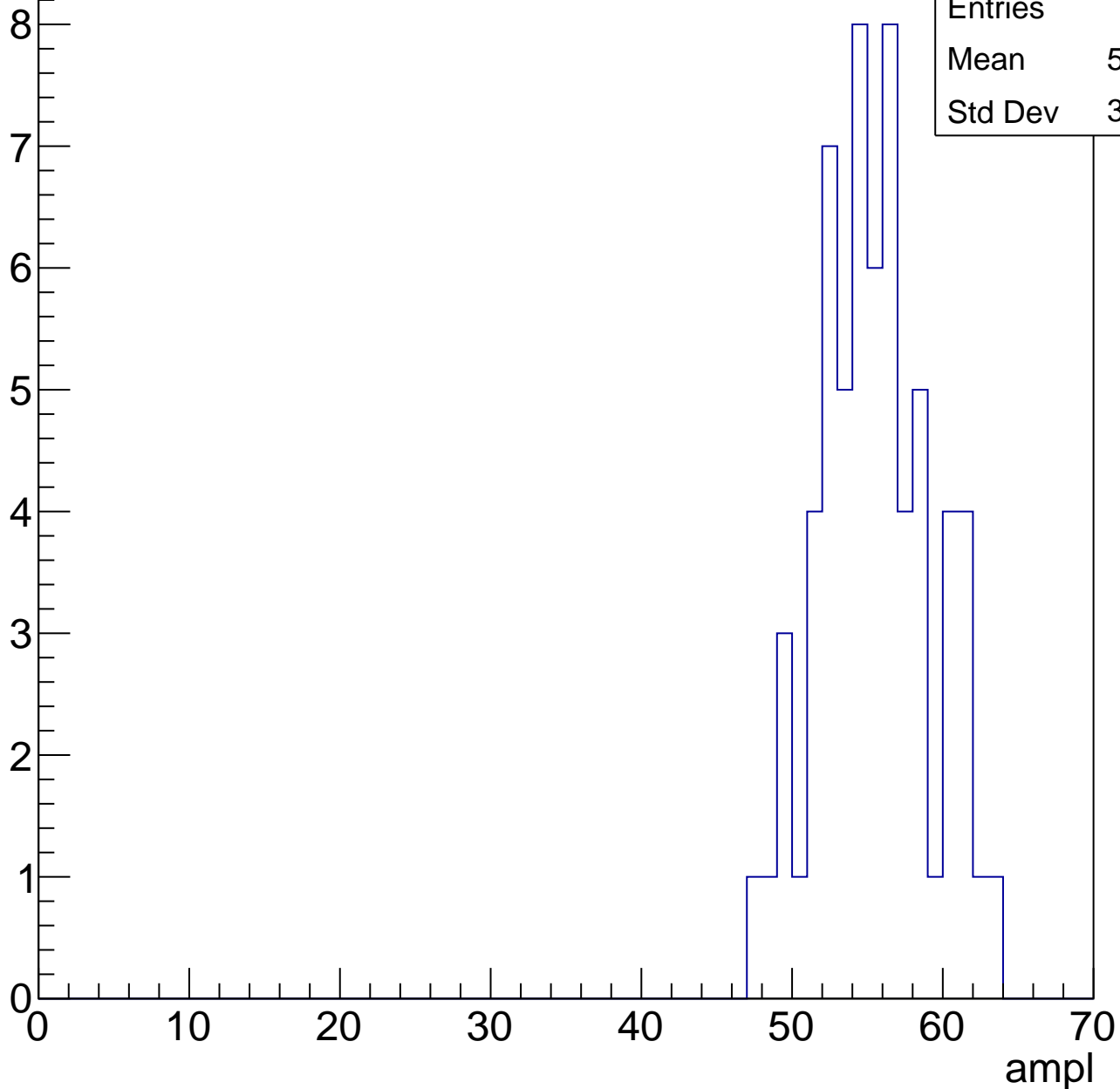


# B0L001S, U5-ch56, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	55.02
Std Dev	3.629

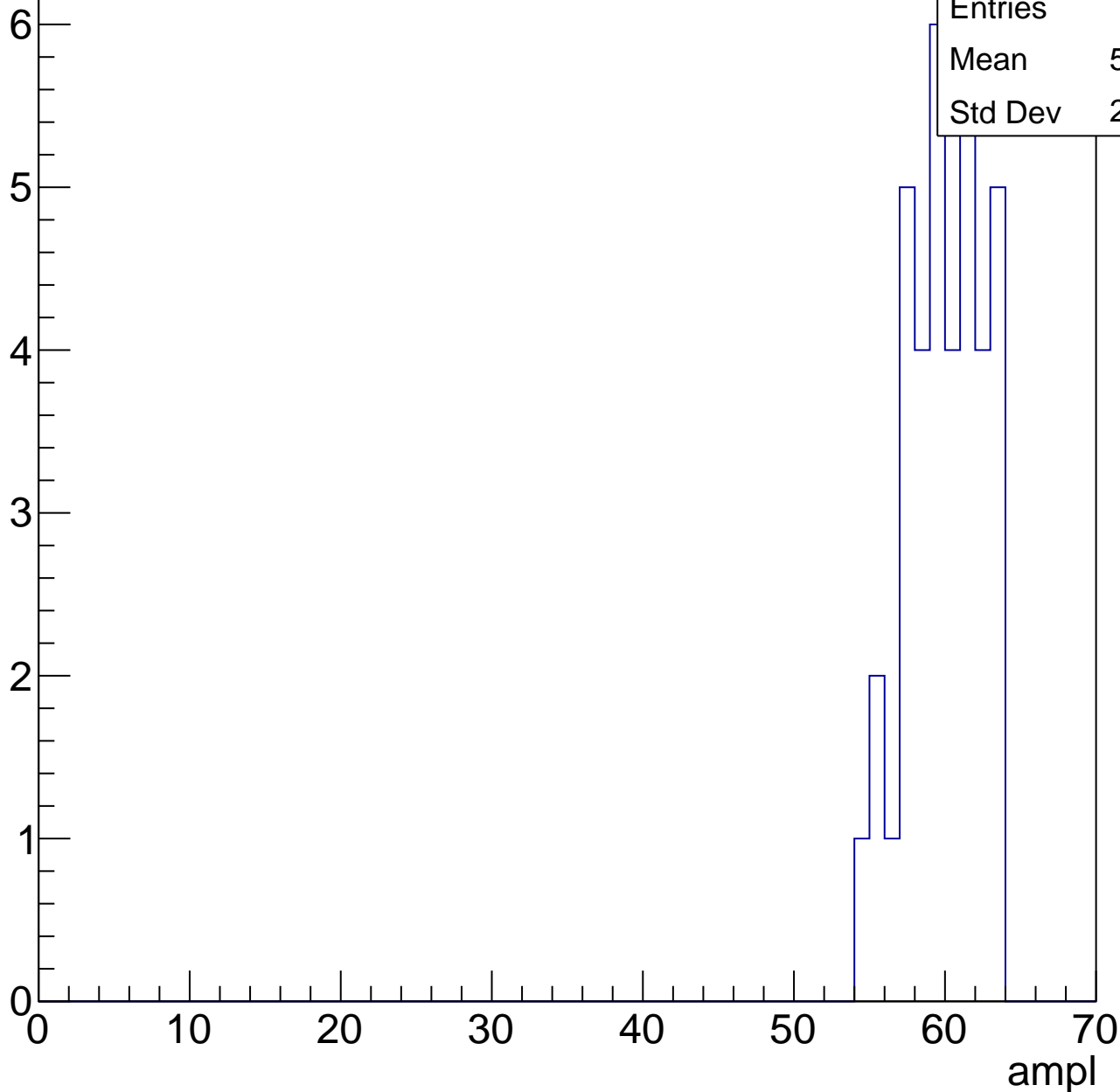


# B0L001S, U5-ch56, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	38
Mean	59.47
Std Dev	2.436

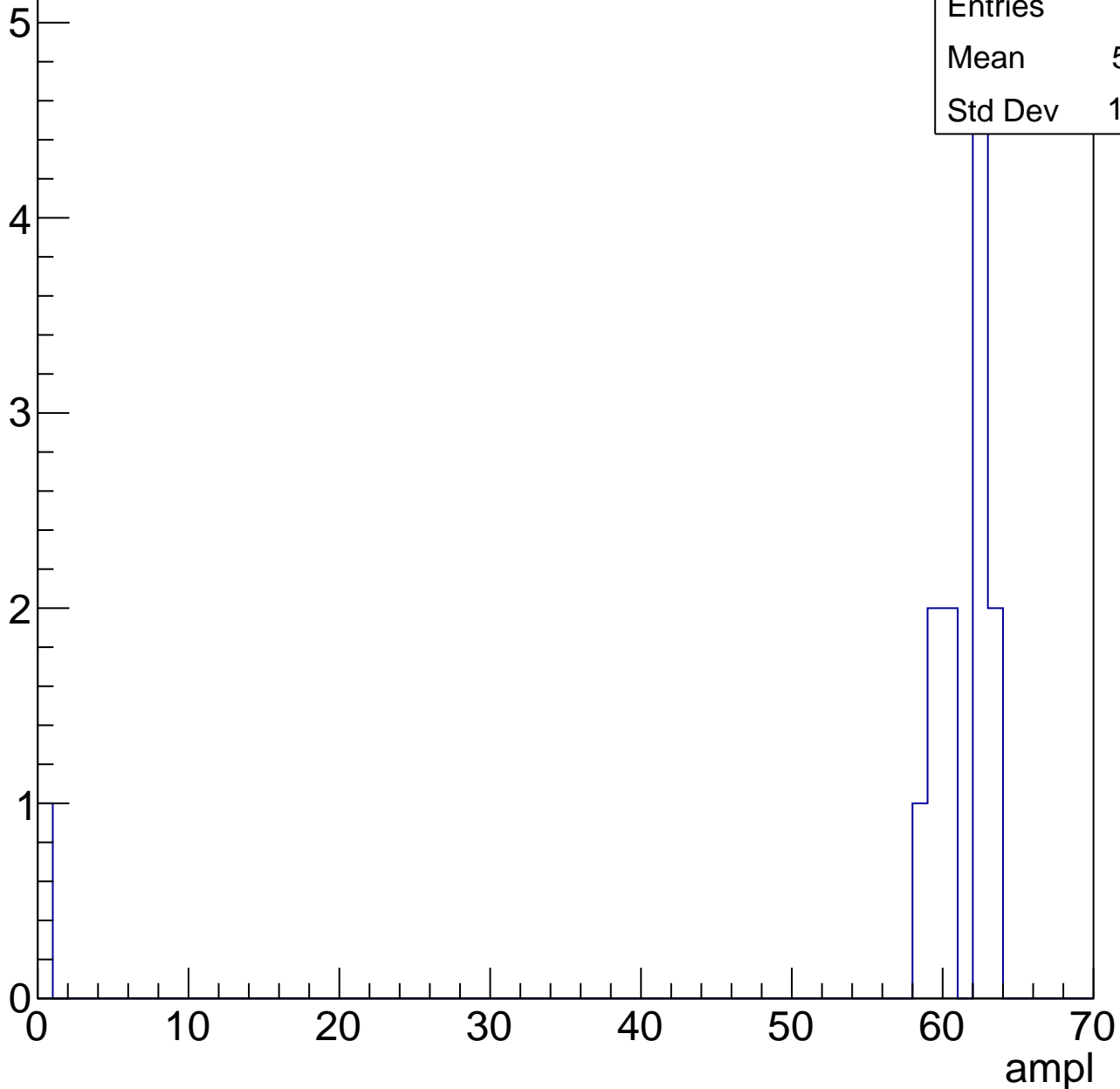


# B0L001S, U5-ch56, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	13
Mean	56.31
Std Dev	16.33





# B0L001S, U5-ch56, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch57, adc0

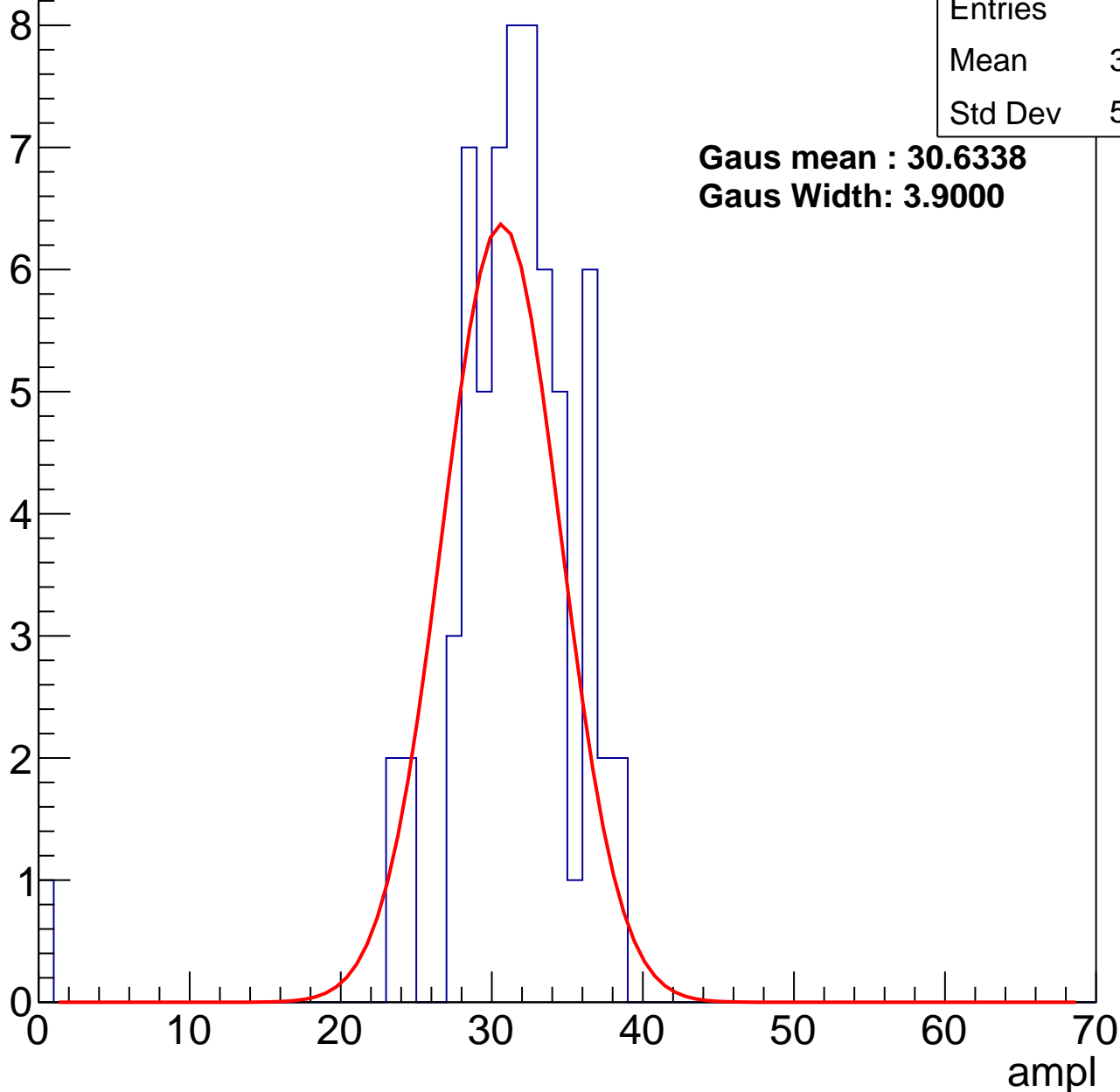
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	30.75
Std Dev	5.165

**Gaus mean : 30.6338**

**Gaus Width: 3.9000**



# B0L001S, U5-ch57, adc1

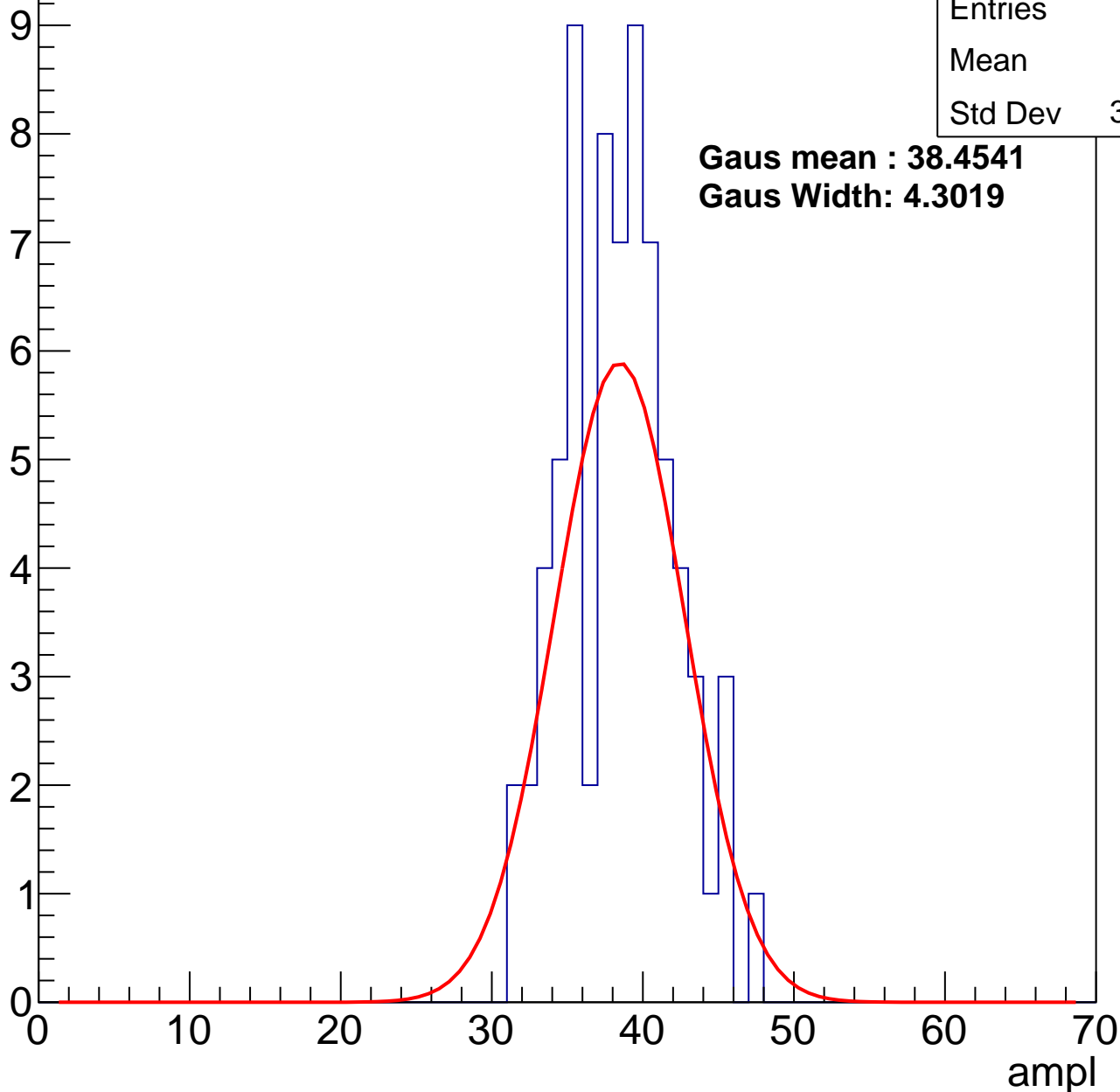
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	38
Std Dev	3.598

**Gaus mean : 38.4541**

**Gaus Width: 4.3019**



# B0L001S, U5-ch57, adc2

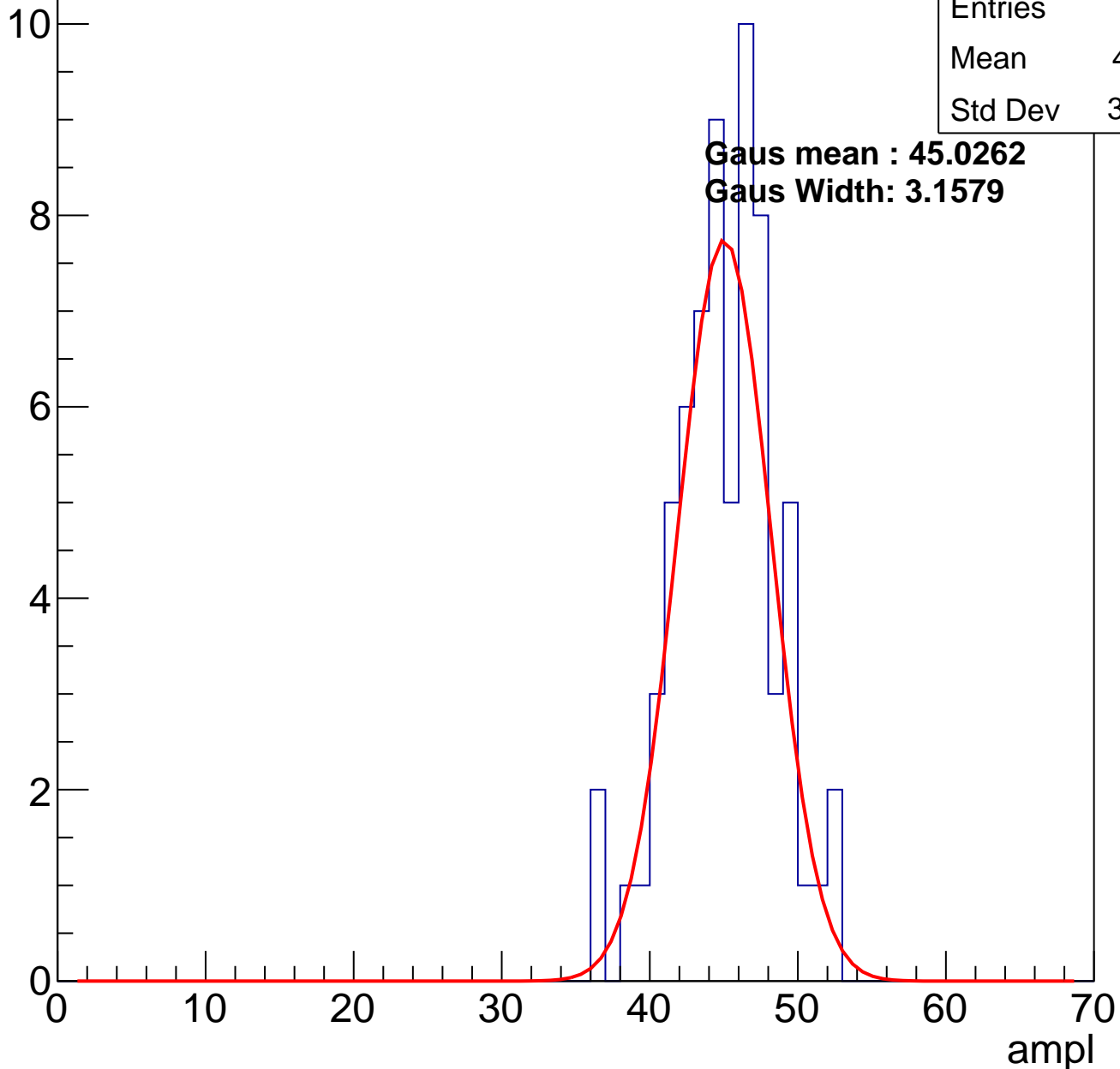
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	69
Mean	44.61
Std Dev	3.385

**Gaus mean : 45.0262**

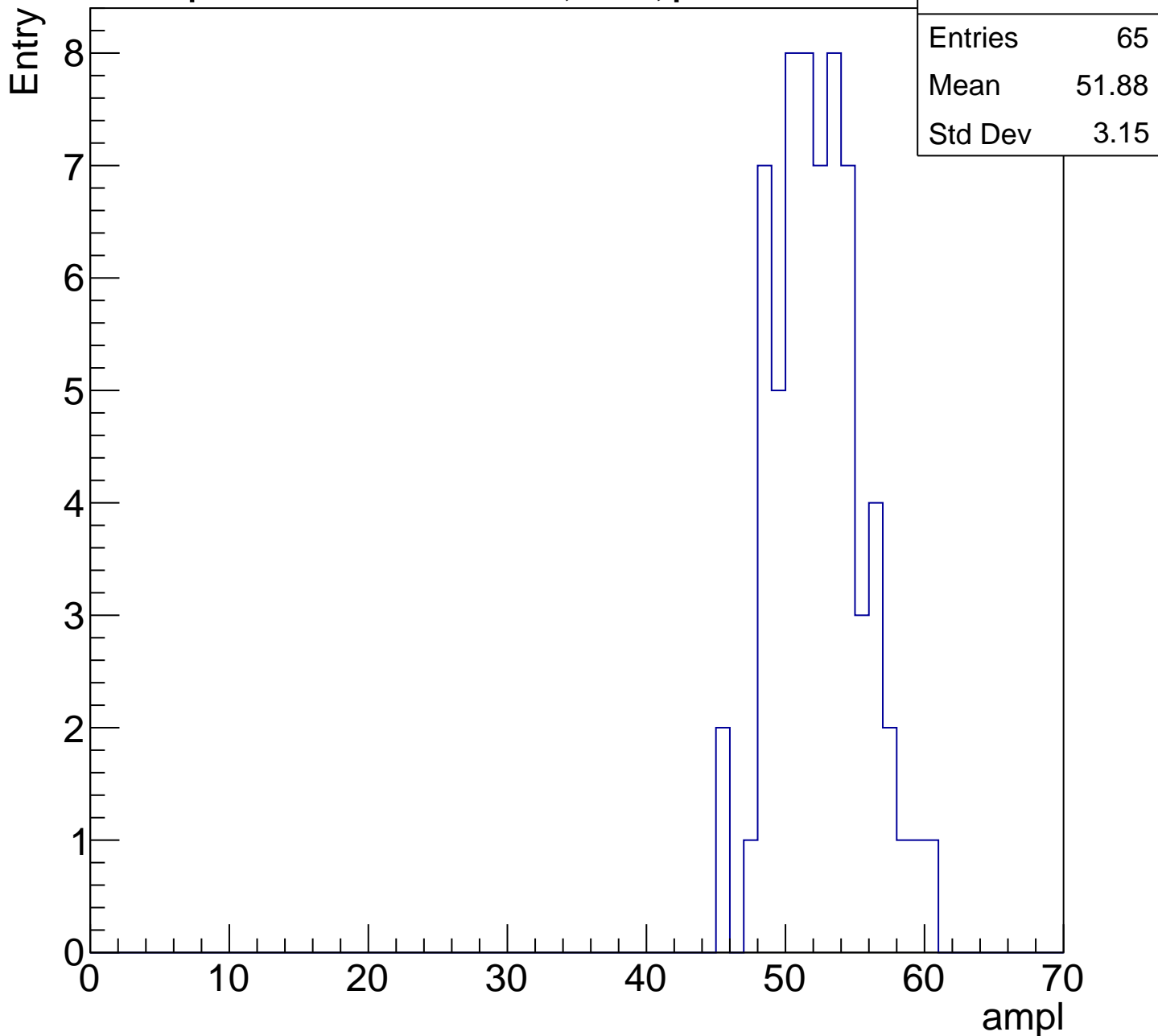
**Gaus Width: 3.1579**

Entry



# B0L001S, U5-ch57, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U5-ch57, adc4

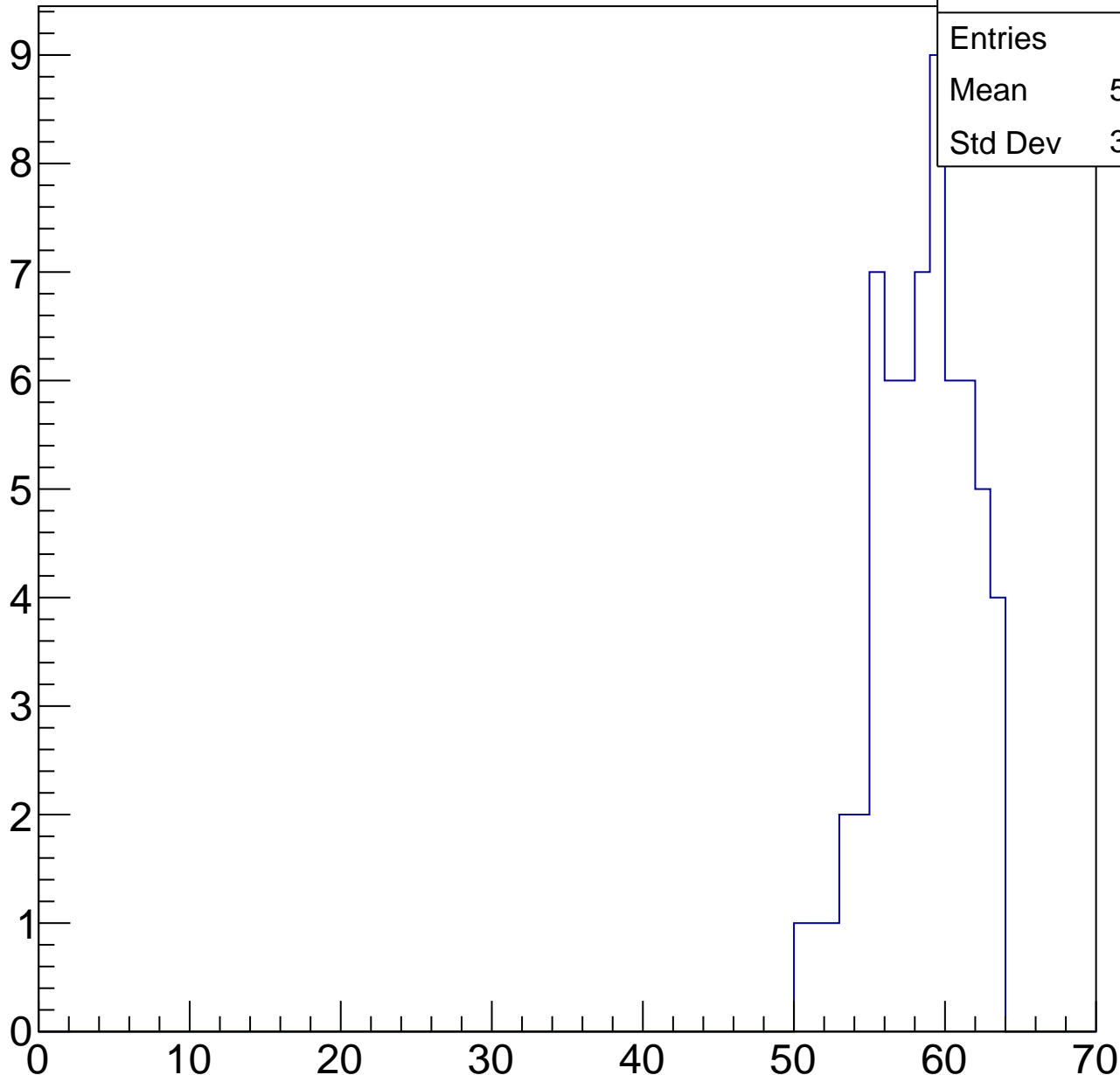
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	63
Mean	58.02
Std Dev	3.063

ampl

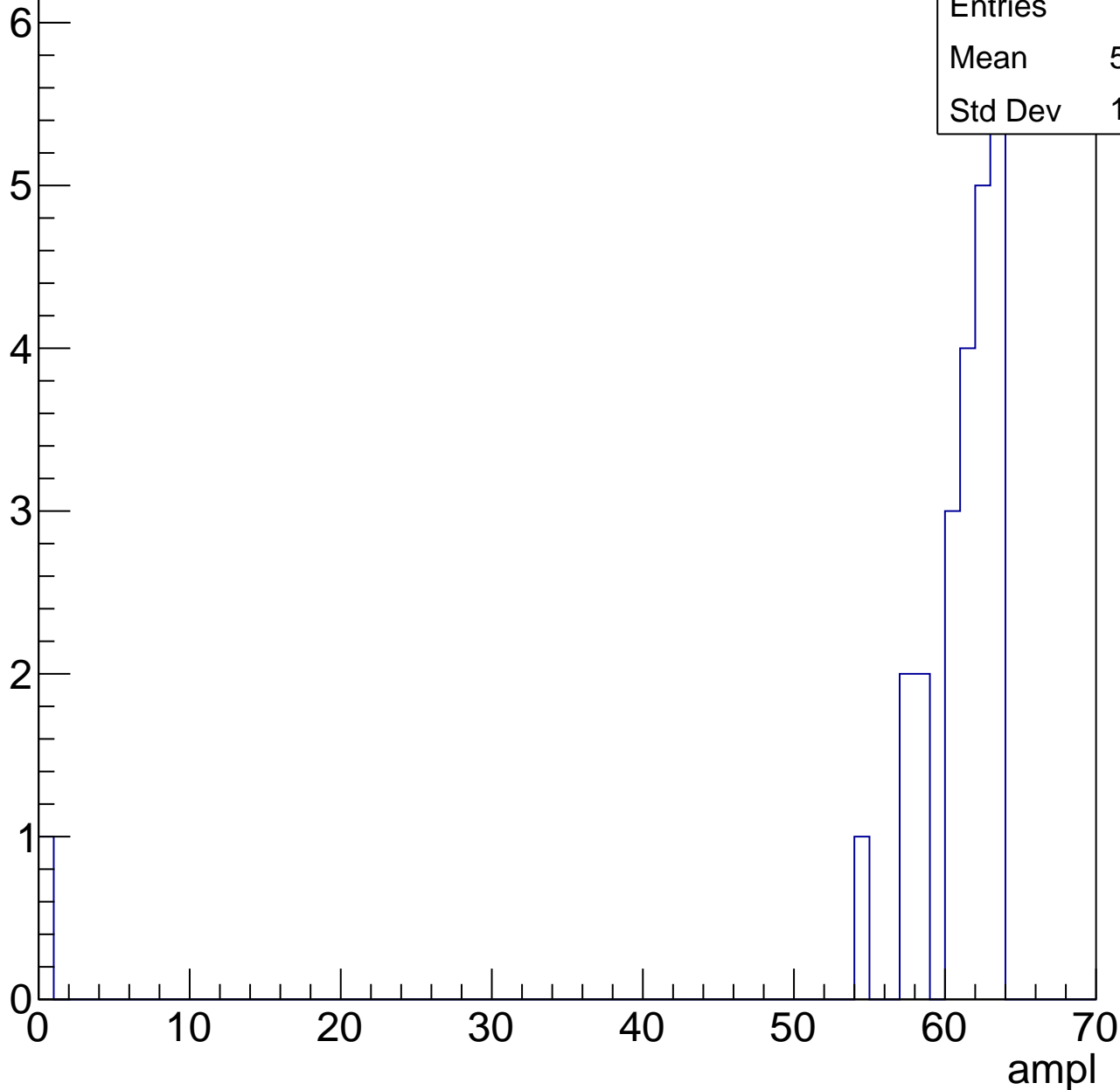


# B0L001S, U5-ch57, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	24
Mean	58.17
Std Dev	12.35



# B0L001S, U5-ch57, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U5-ch57, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch58, adc0

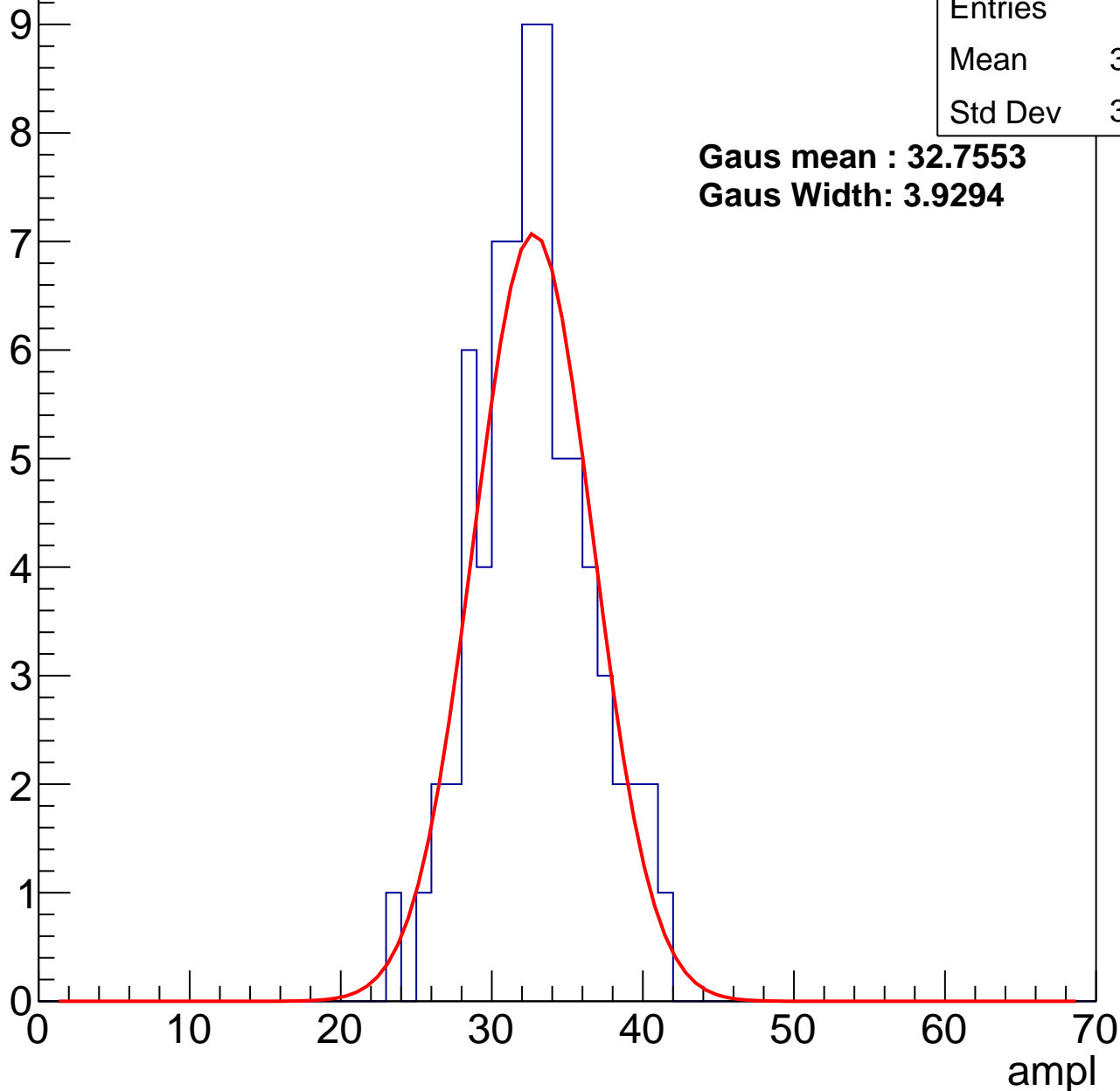
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	32.29
Std Dev	3.736

**Gaus mean : 32.7553**

**Gaus Width: 3.9294**



# B0L001S, U5-ch58, adc1

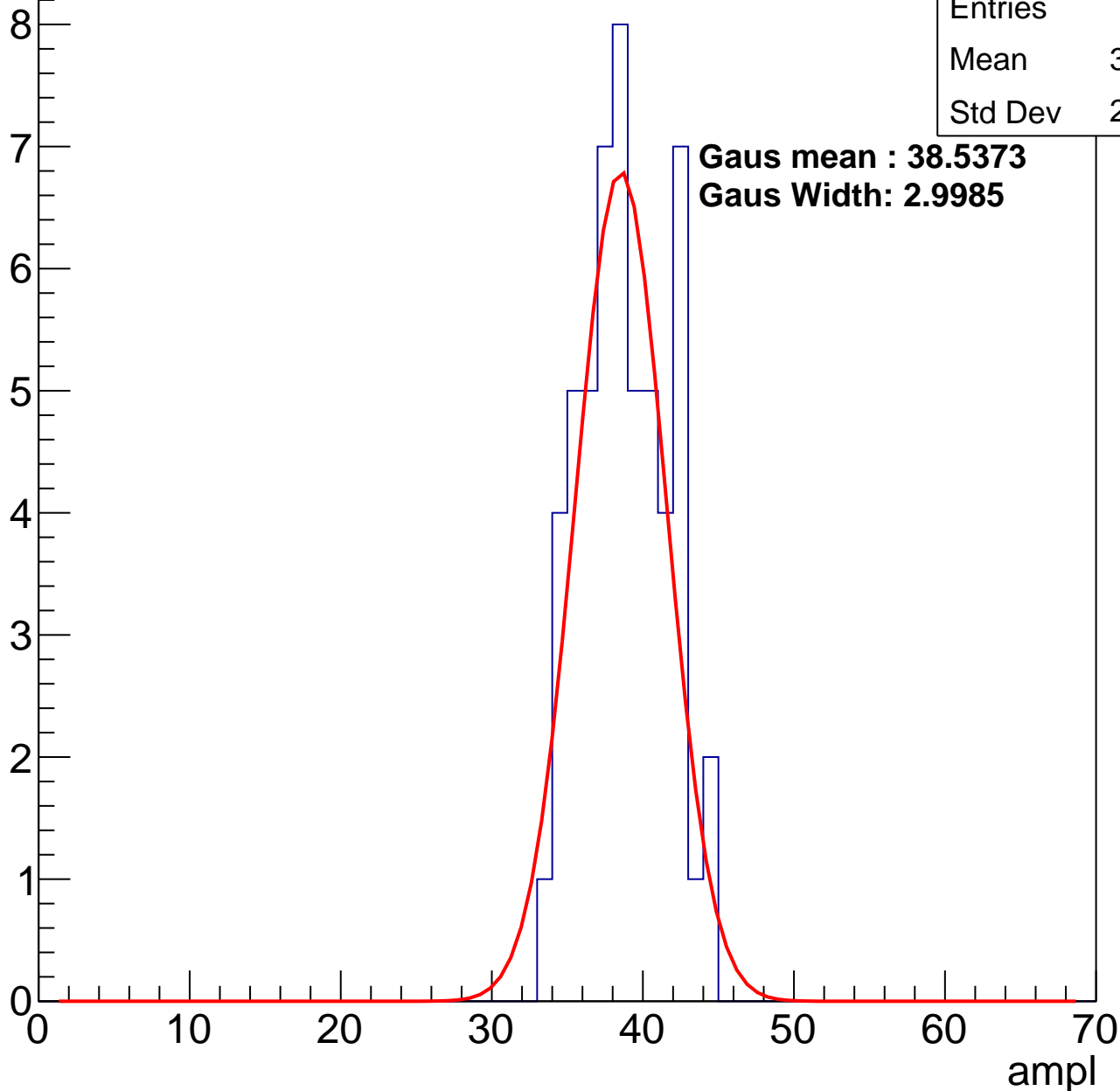
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	38.35
Std Dev	2.803

**Gaus mean : 38.5373**

**Gaus Width: 2.9985**



# B0L001S, U5-ch58, adc2

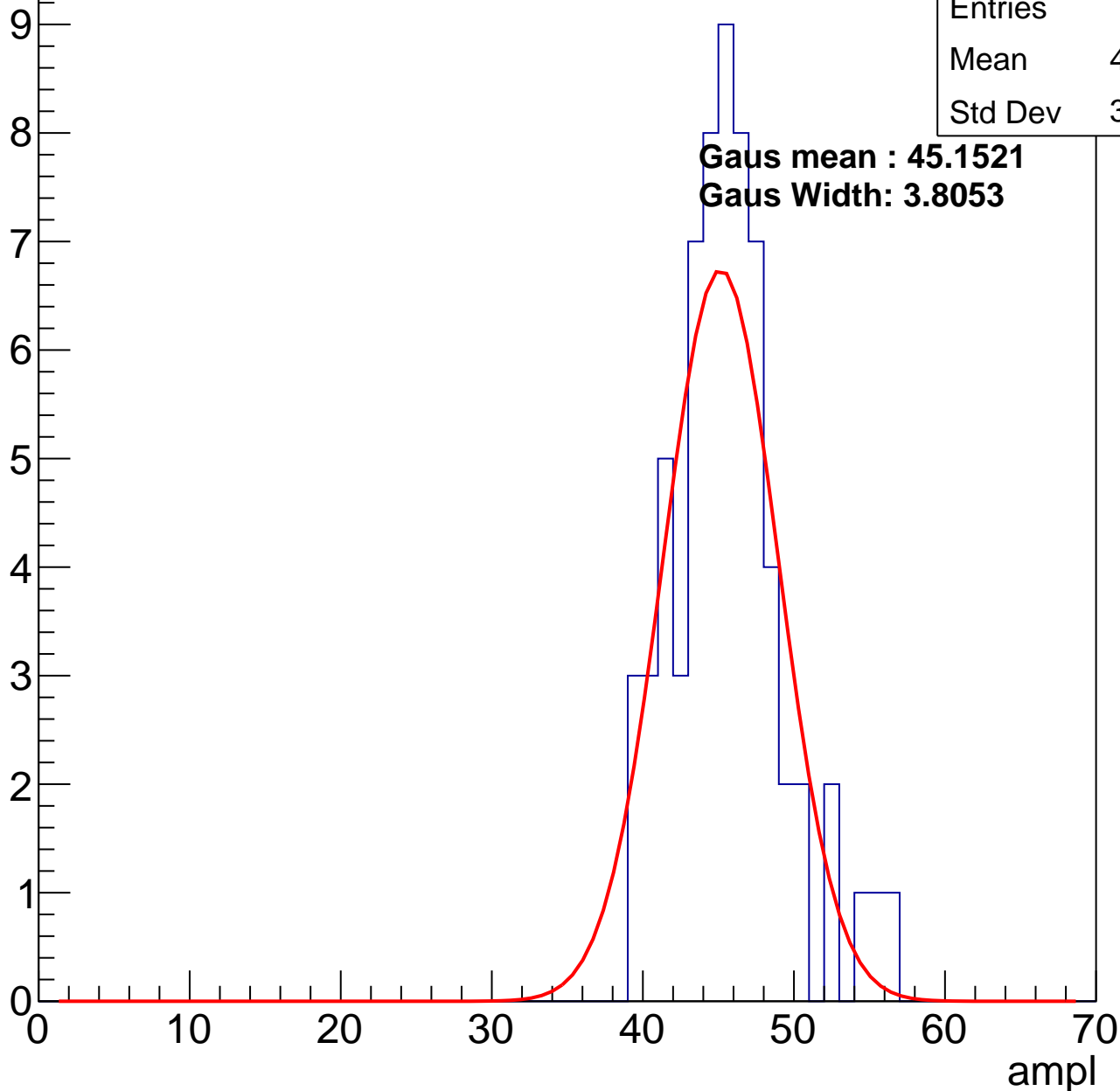
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	45.18
Std Dev	3.647

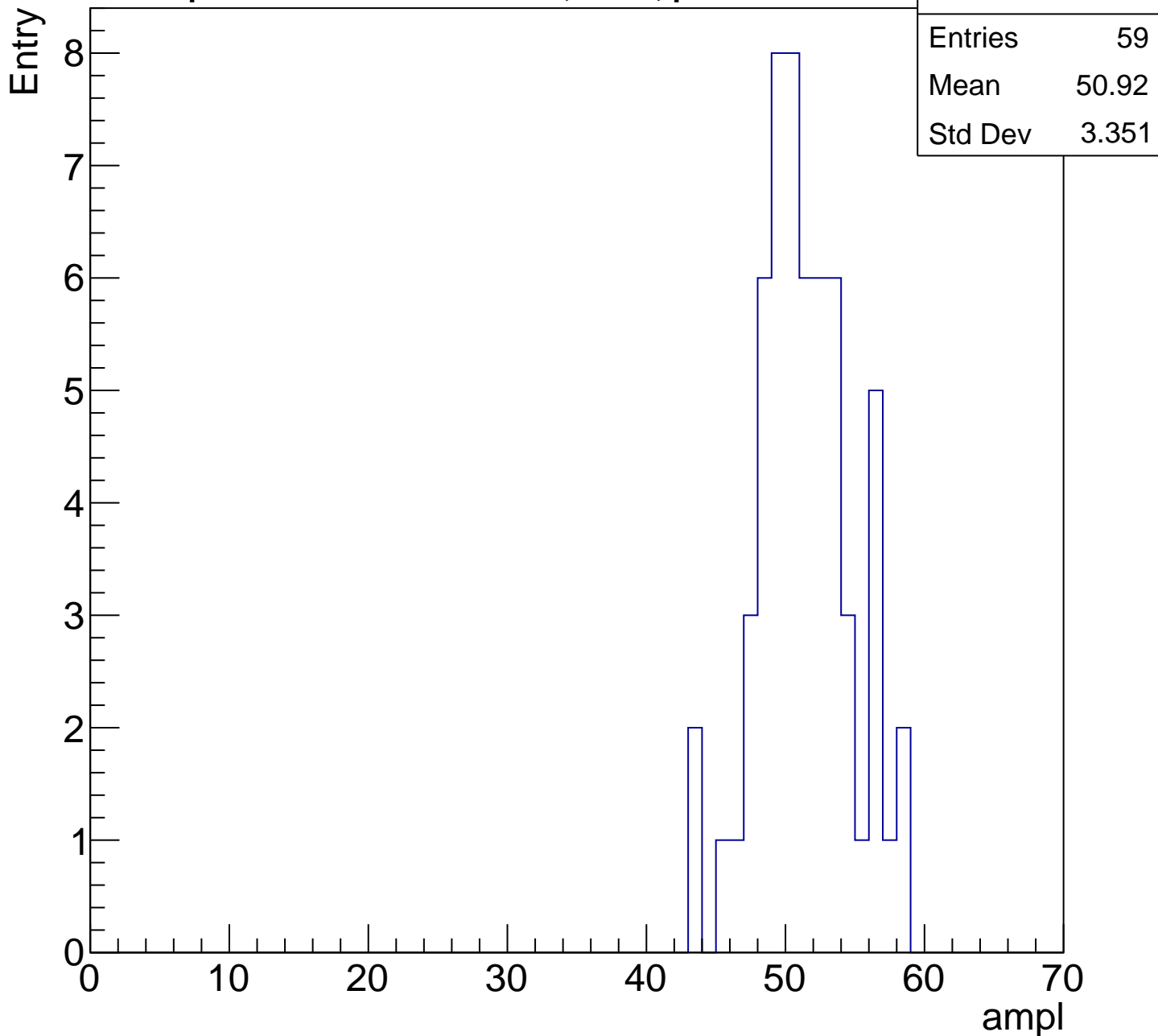
**Gaus mean : 45.1521**

**Gaus Width: 3.8053**



# B0L001S, U5-ch58, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

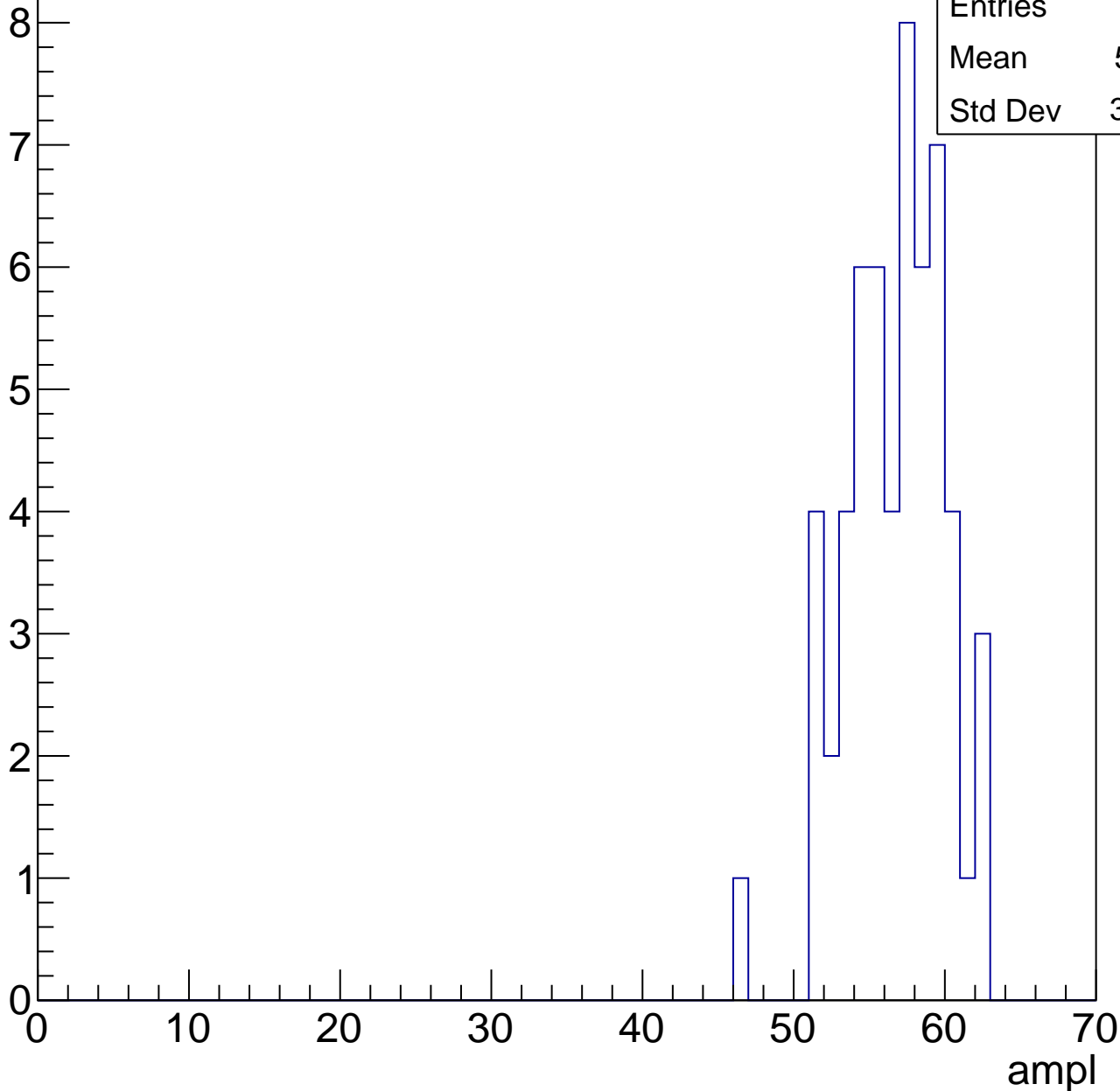


# B0L001S, U5-ch58, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	56.21
Std Dev	3.239

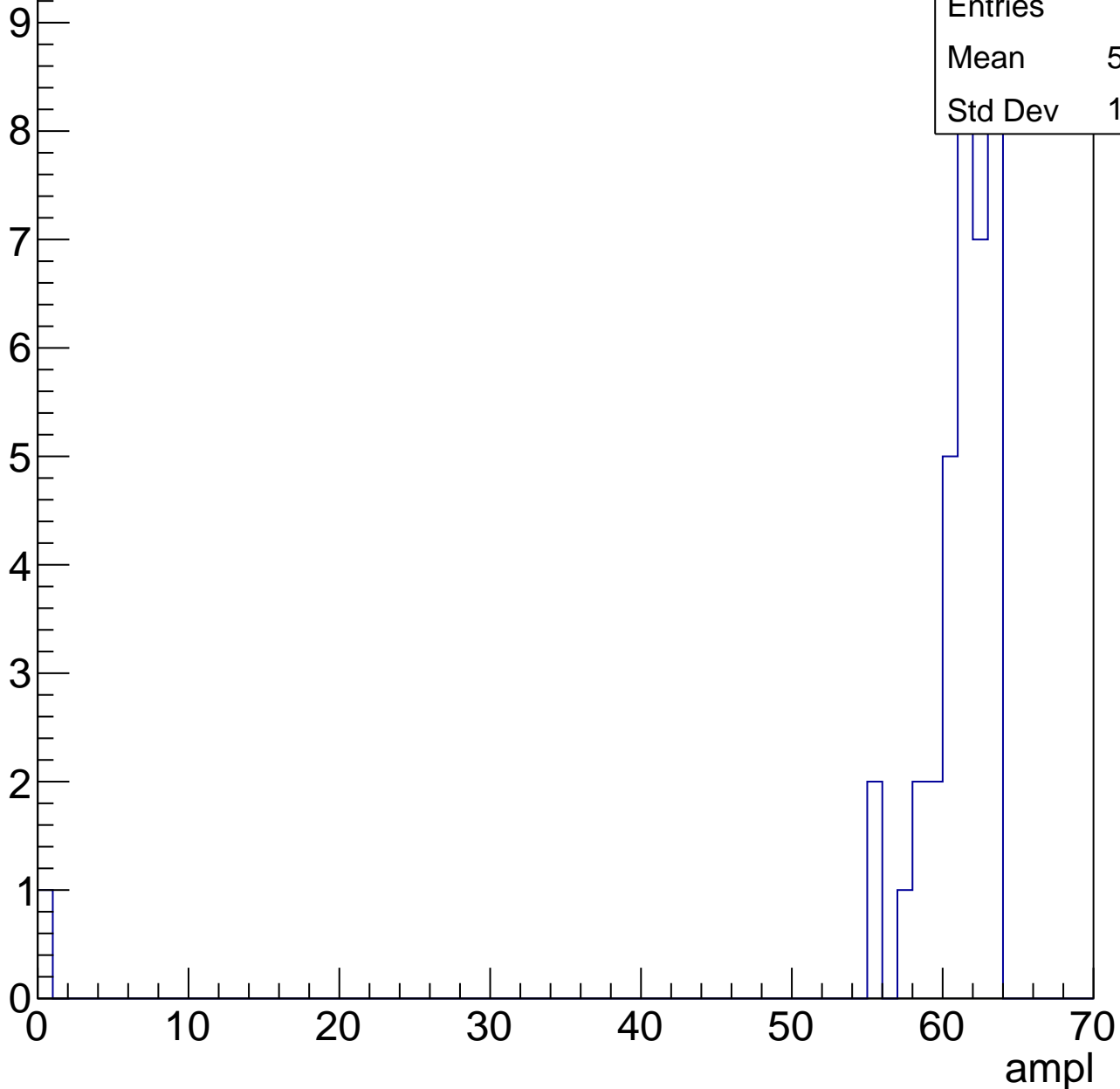


# B0L001S, U5-ch58, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

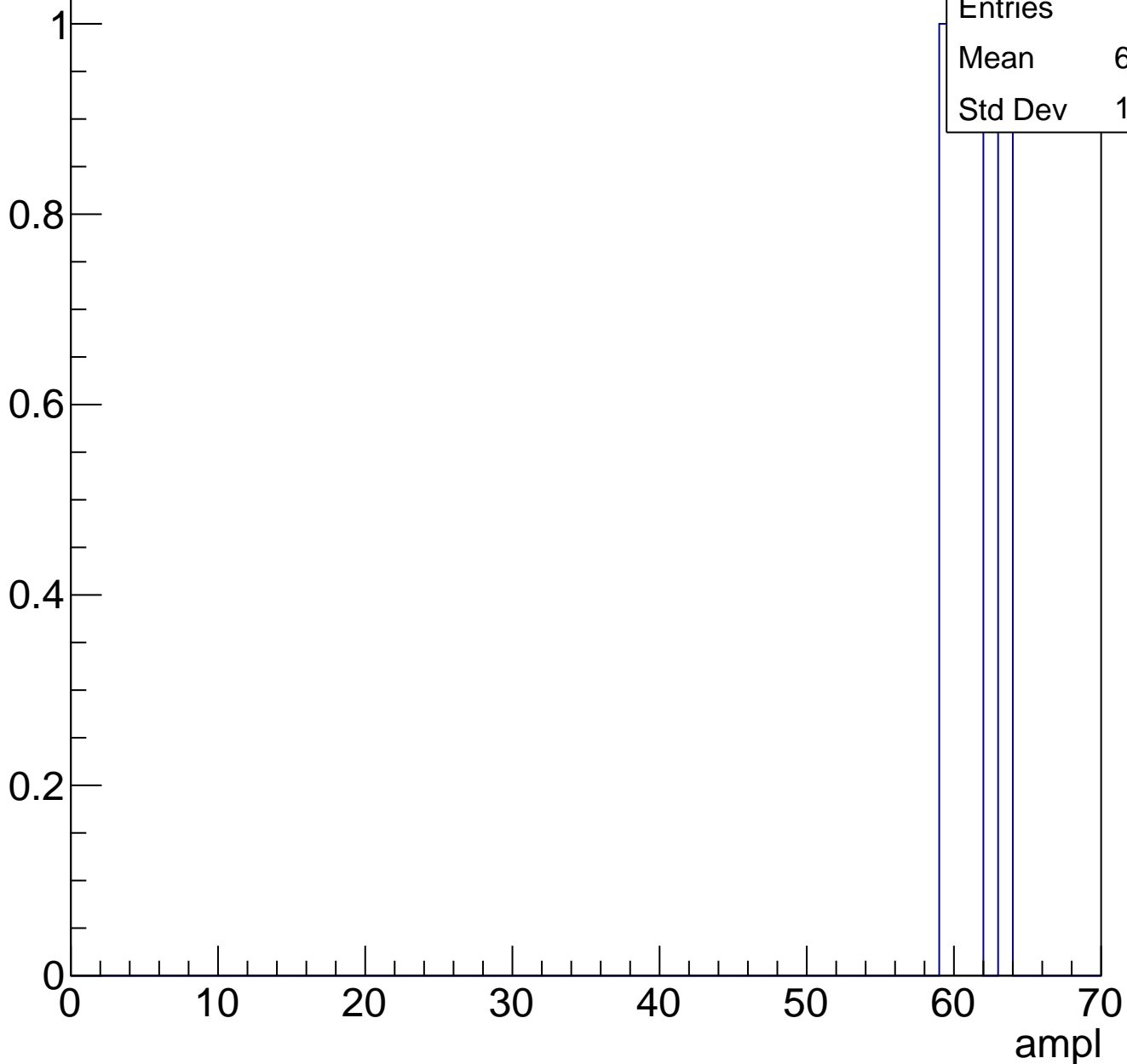
Entries	37
Mean	59.19
Std Dev	10.08



# B0L001S, U5-ch58, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch58, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U5-ch59, adc0

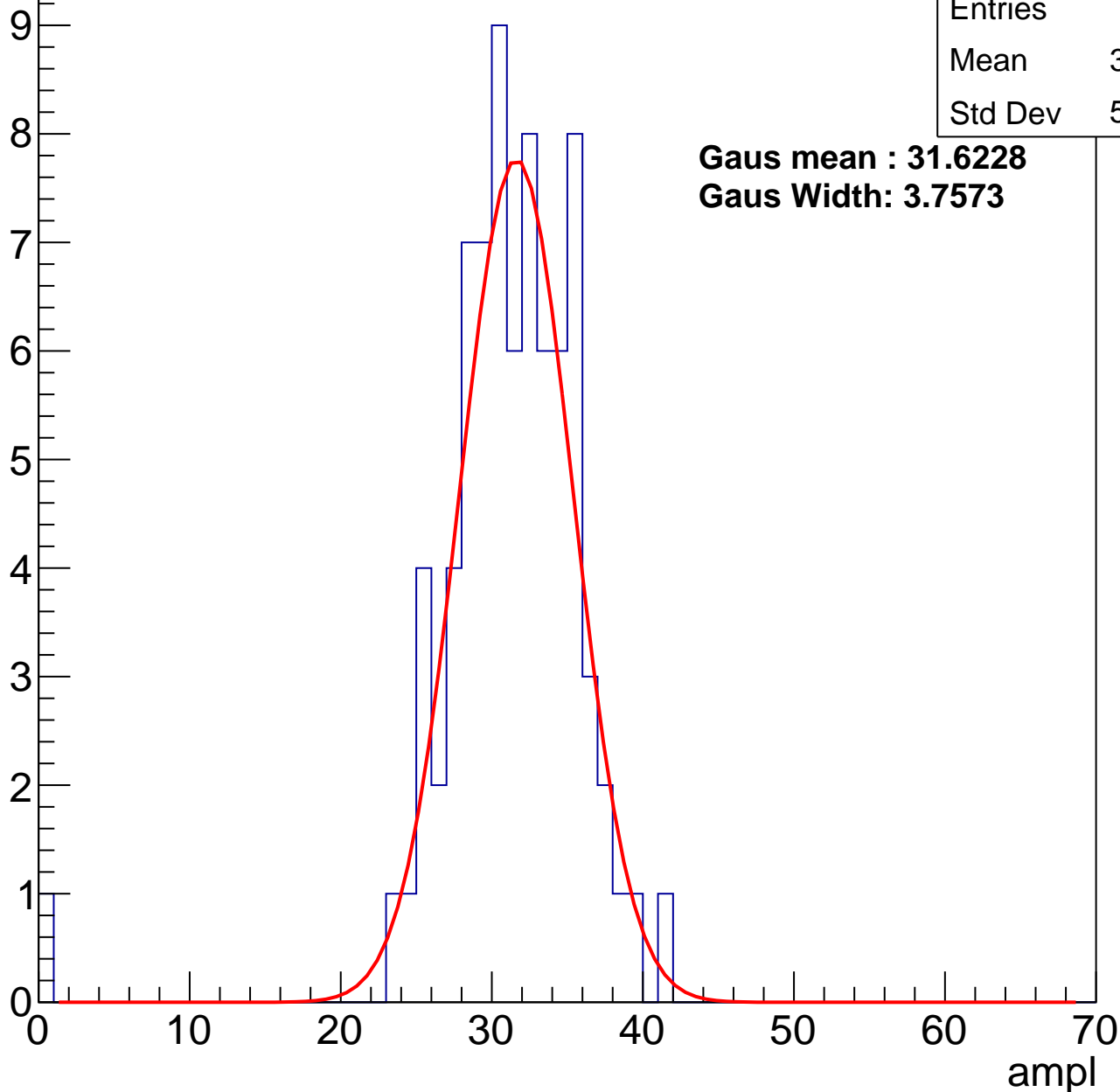
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	78
Mean	30.77
Std Dev	5.066

**Gaus mean : 31.6228**

**Gaus Width: 3.7573**



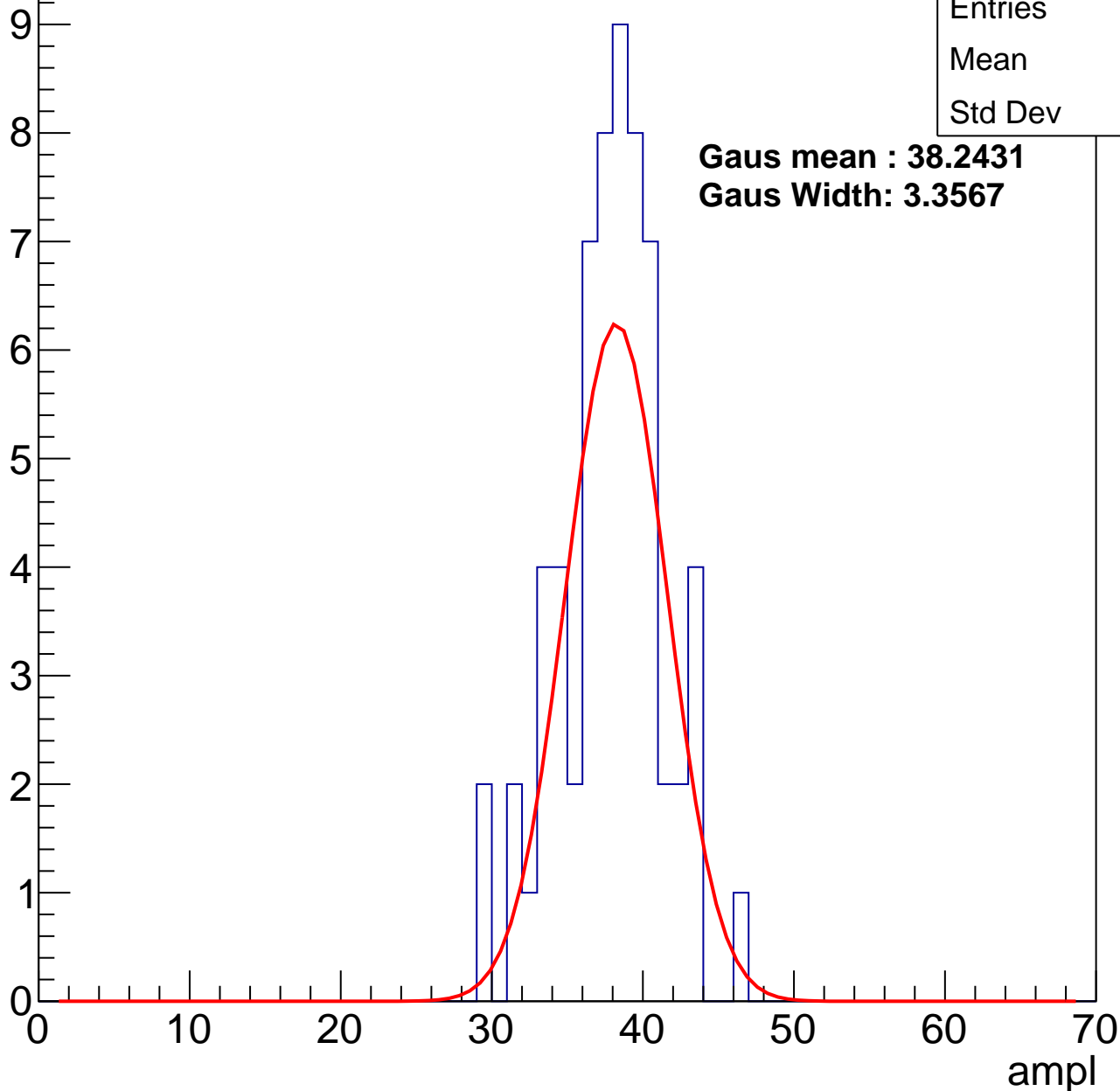
# B0L001S, U5-ch59, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	37.4
Std Dev	3.43

**Gaus mean : 38.2431**  
**Gaus Width: 3.3567**

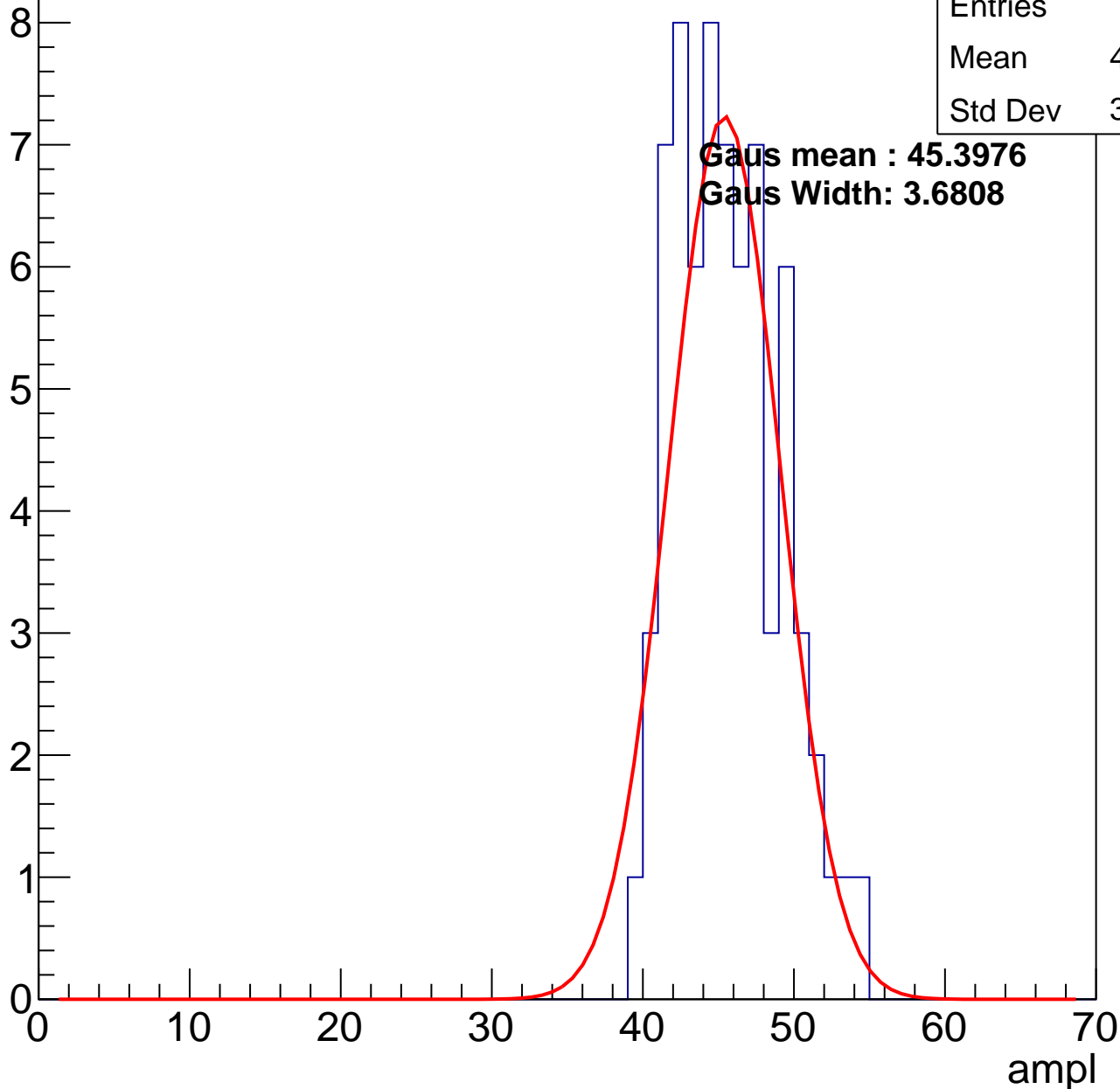


# B0L001S, U5-ch59, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	45.16
Std Dev	3.429

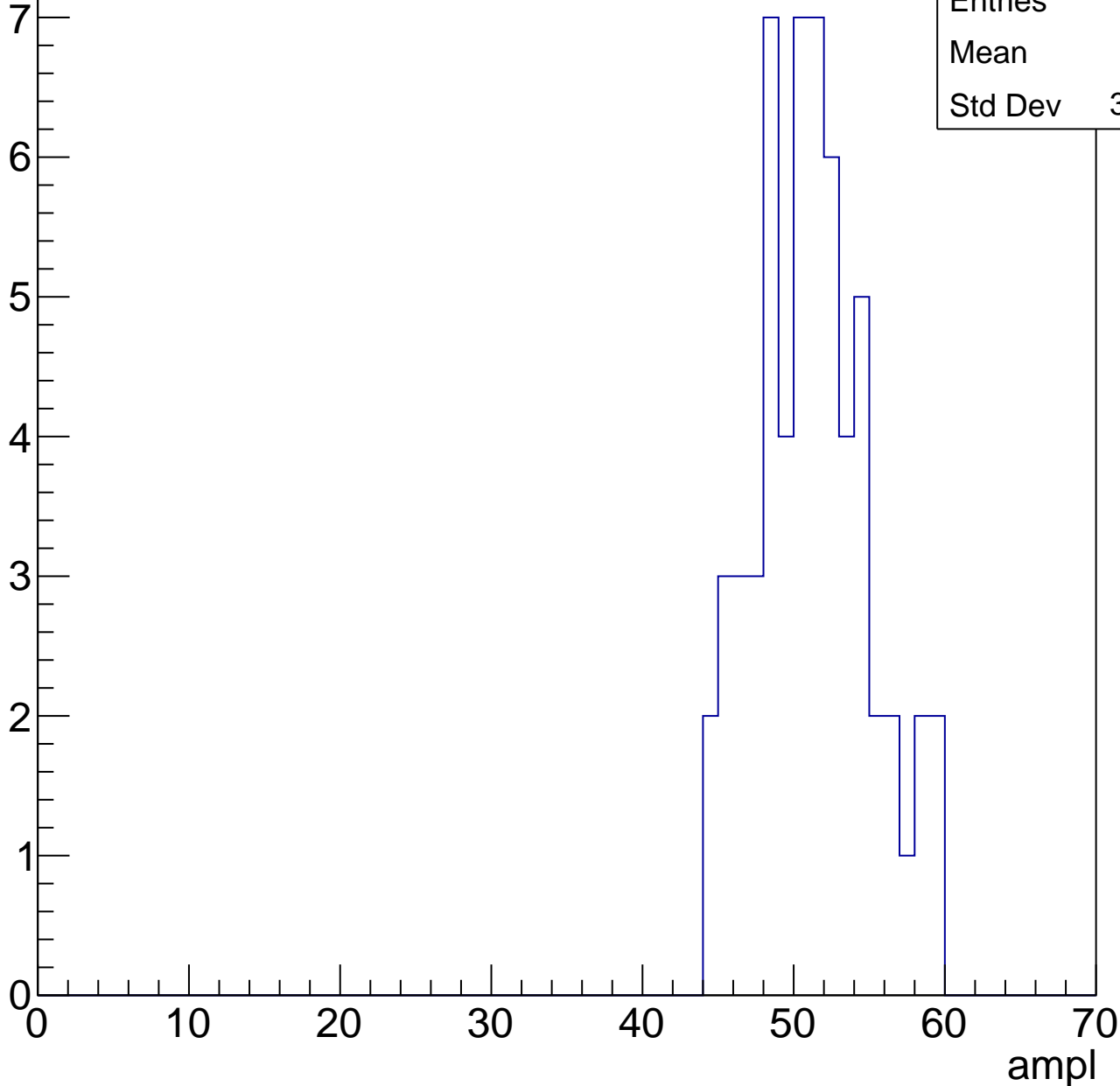


# B0L001S, U5-ch59, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

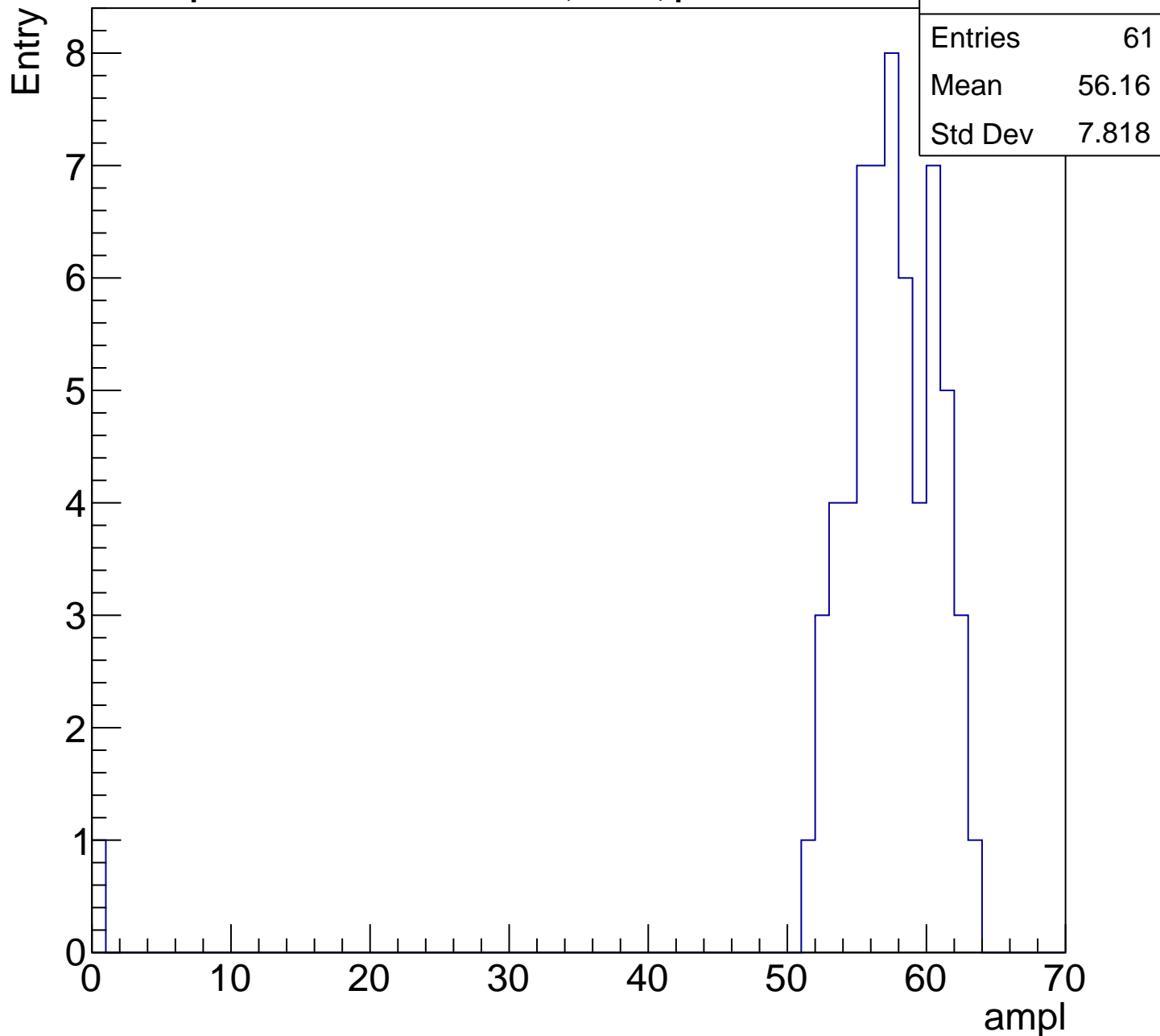
Entry

Entries	60
Mean	50.8
Std Dev	3.705



# B0L001S, U5-ch59, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

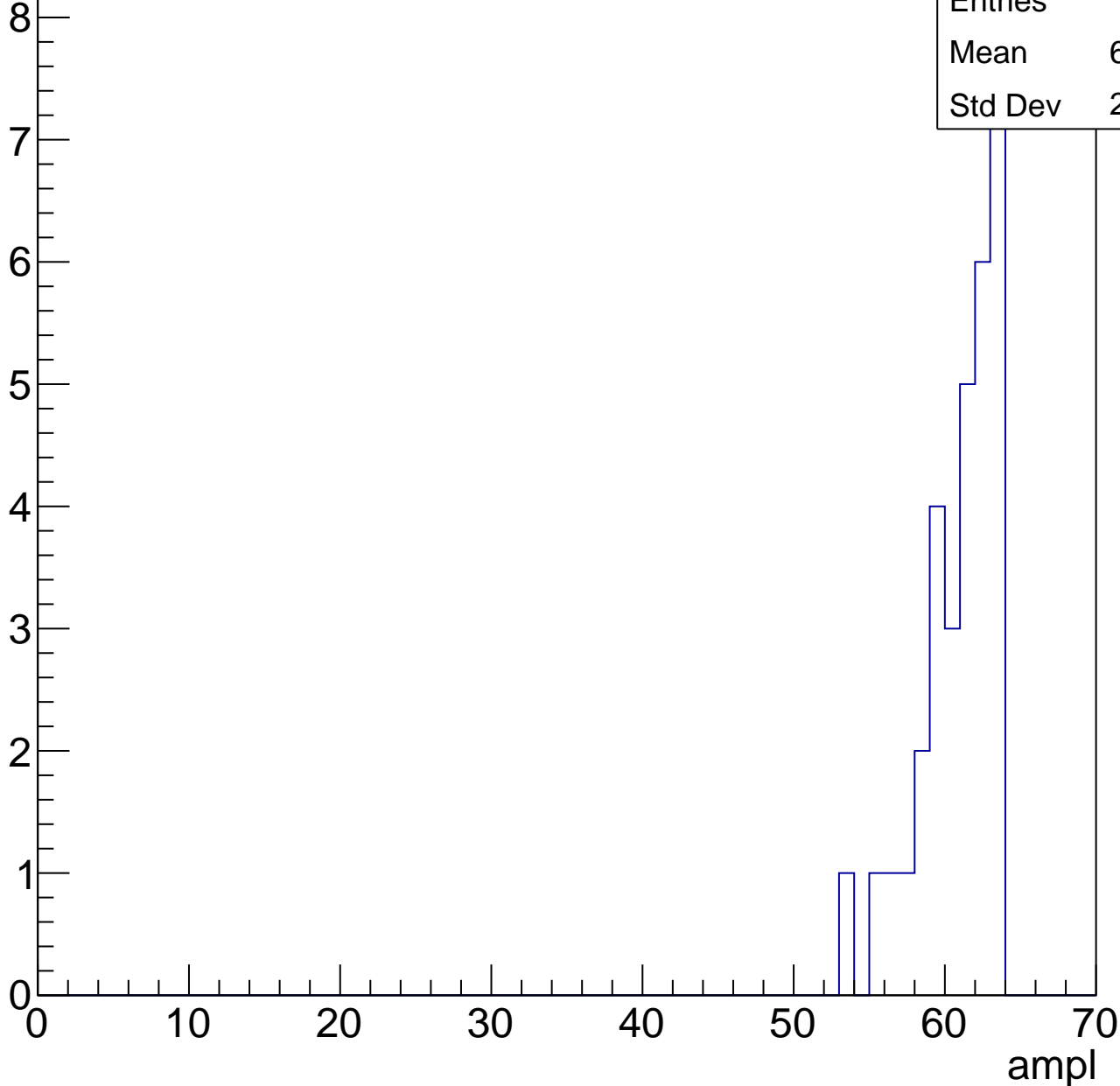


# B0L001S, U5-ch59, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	32
Mean	60.44
Std Dev	2.536



# B0L001S, U5-ch59, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch59, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U5-ch60, adc0

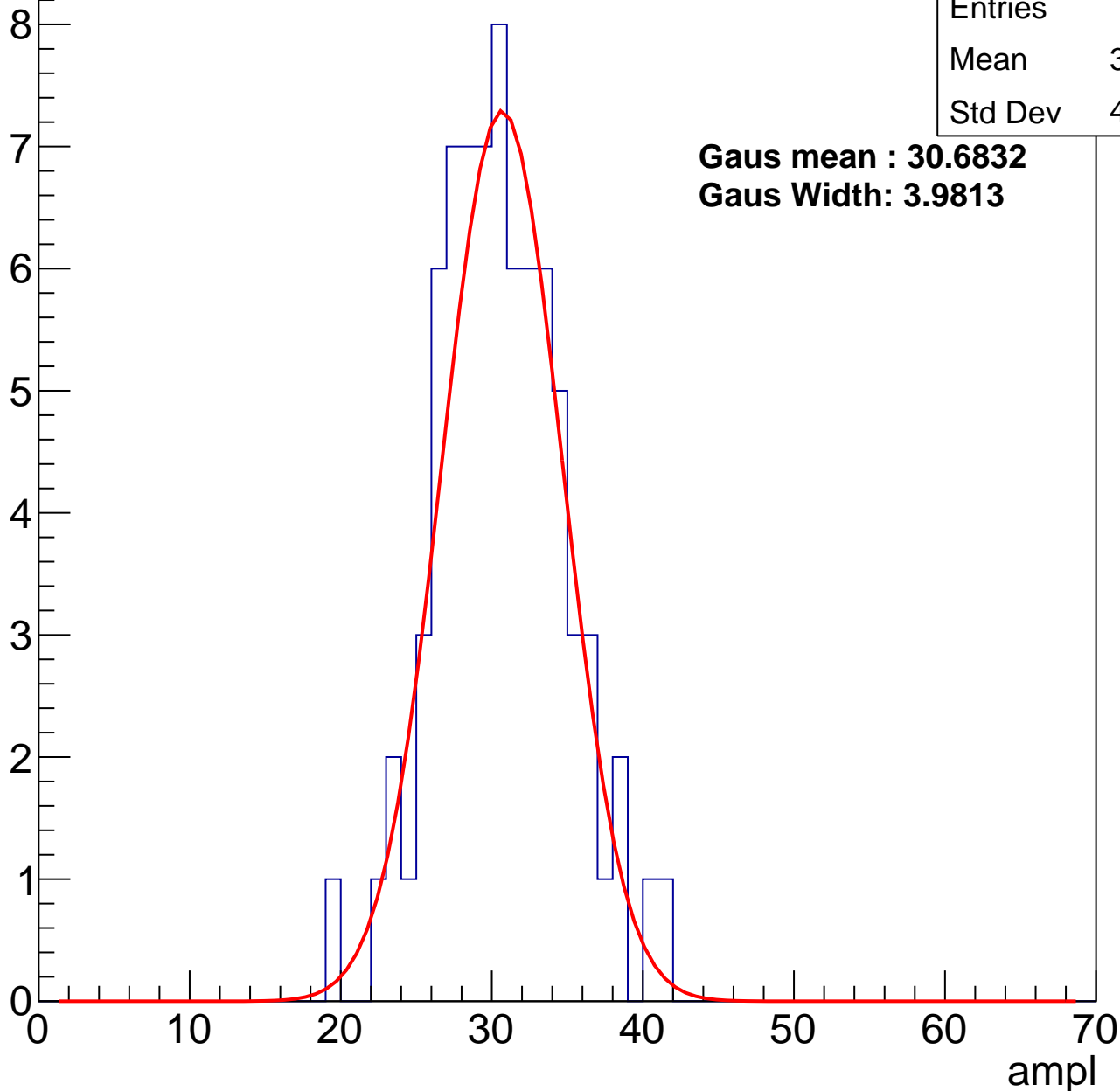
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	77
Mean	30.17
Std Dev	4.157

**Gaus mean : 30.6832**

**Gaus Width: 3.9813**



# B0L001S, U5-ch60, adc1

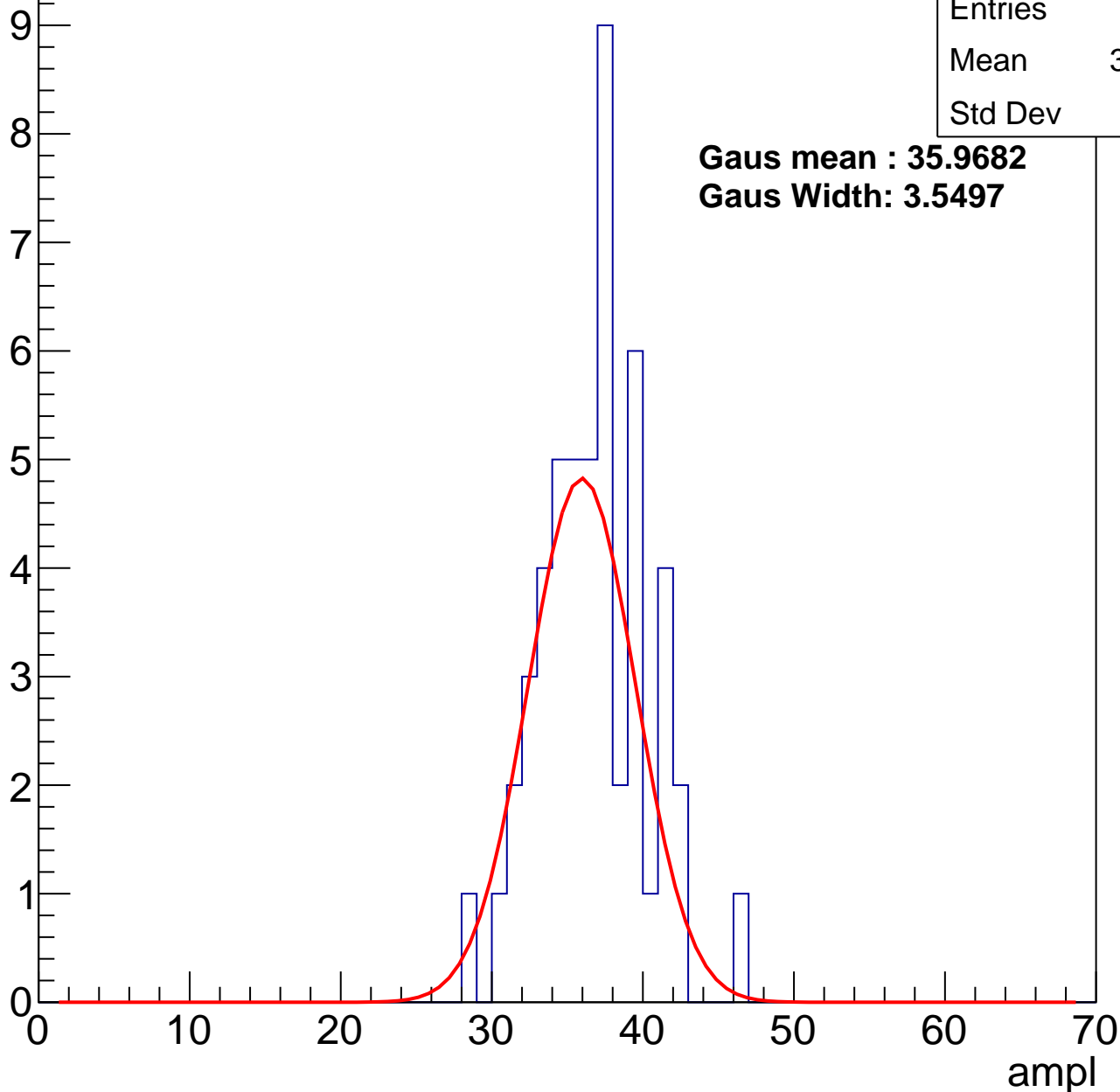
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	51
Mean	36.27
Std Dev	3.47

**Gaus mean : 35.9682**

**Gaus Width: 3.5497**



# B0L001S, U5-ch60, adc2

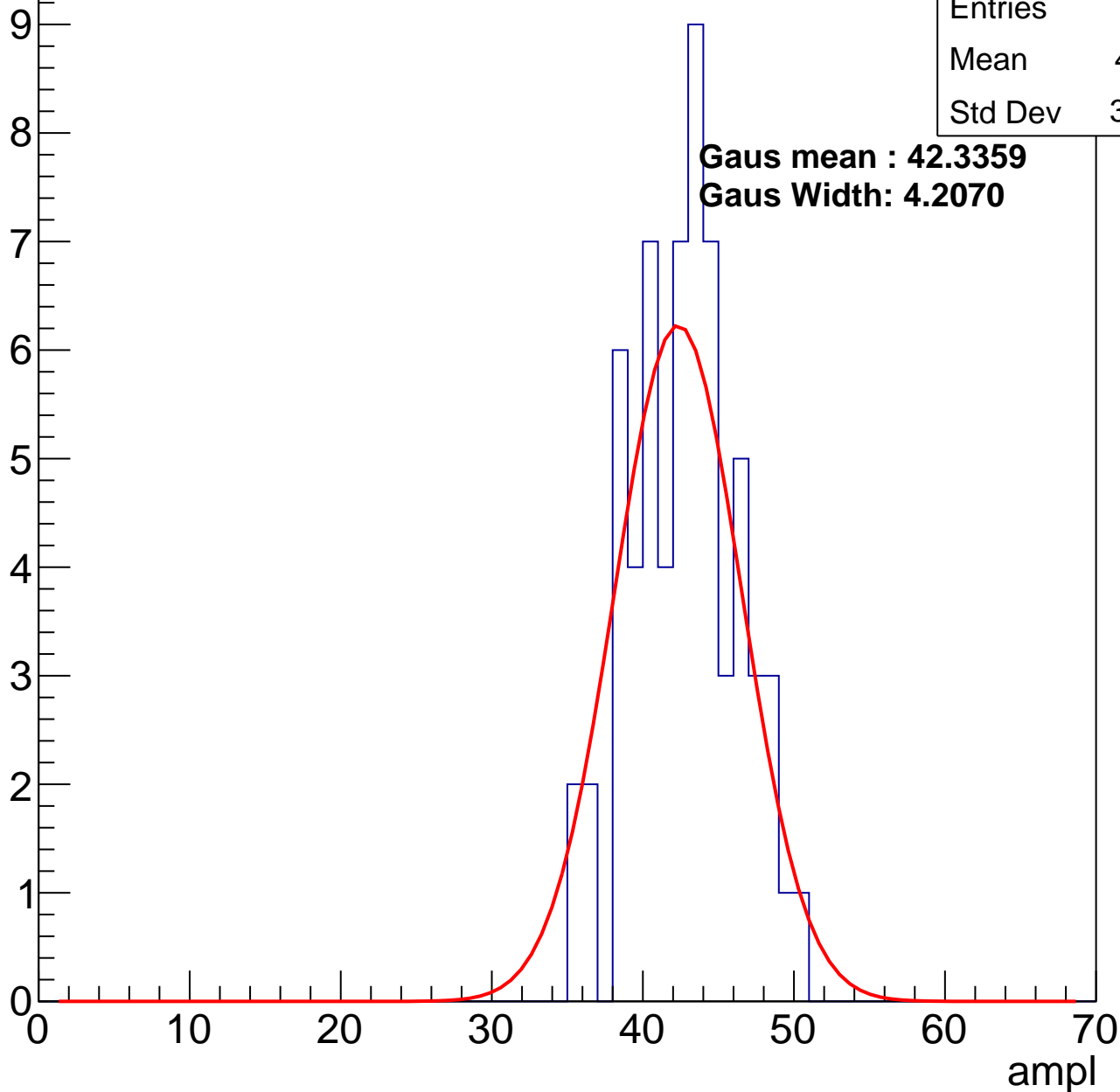
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	42.31
Std Dev	3.464

**Gaus mean : 42.3359**

**Gaus Width: 4.2070**

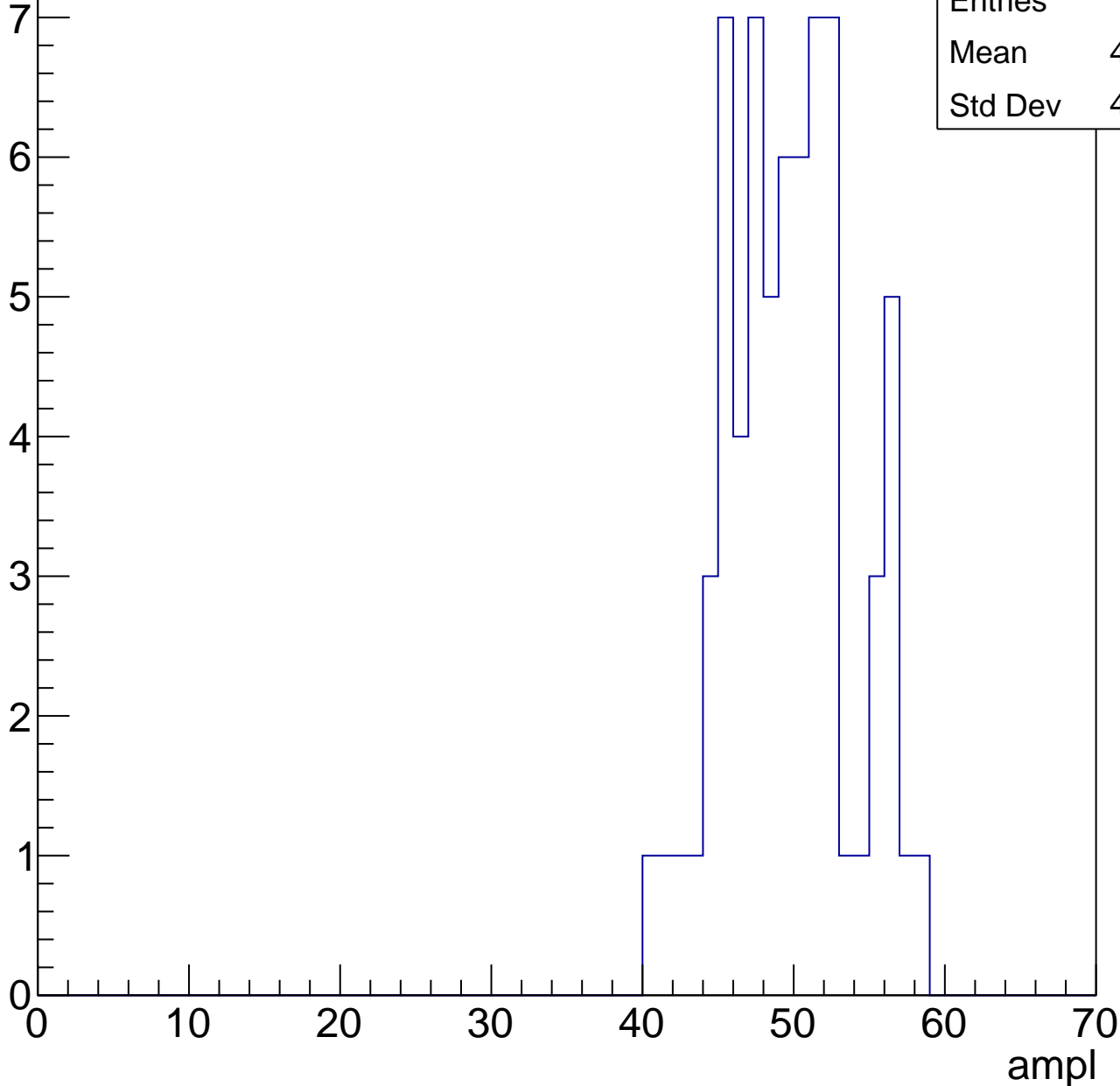


# B0L001S, U5-ch60, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	49.24
Std Dev	4.055

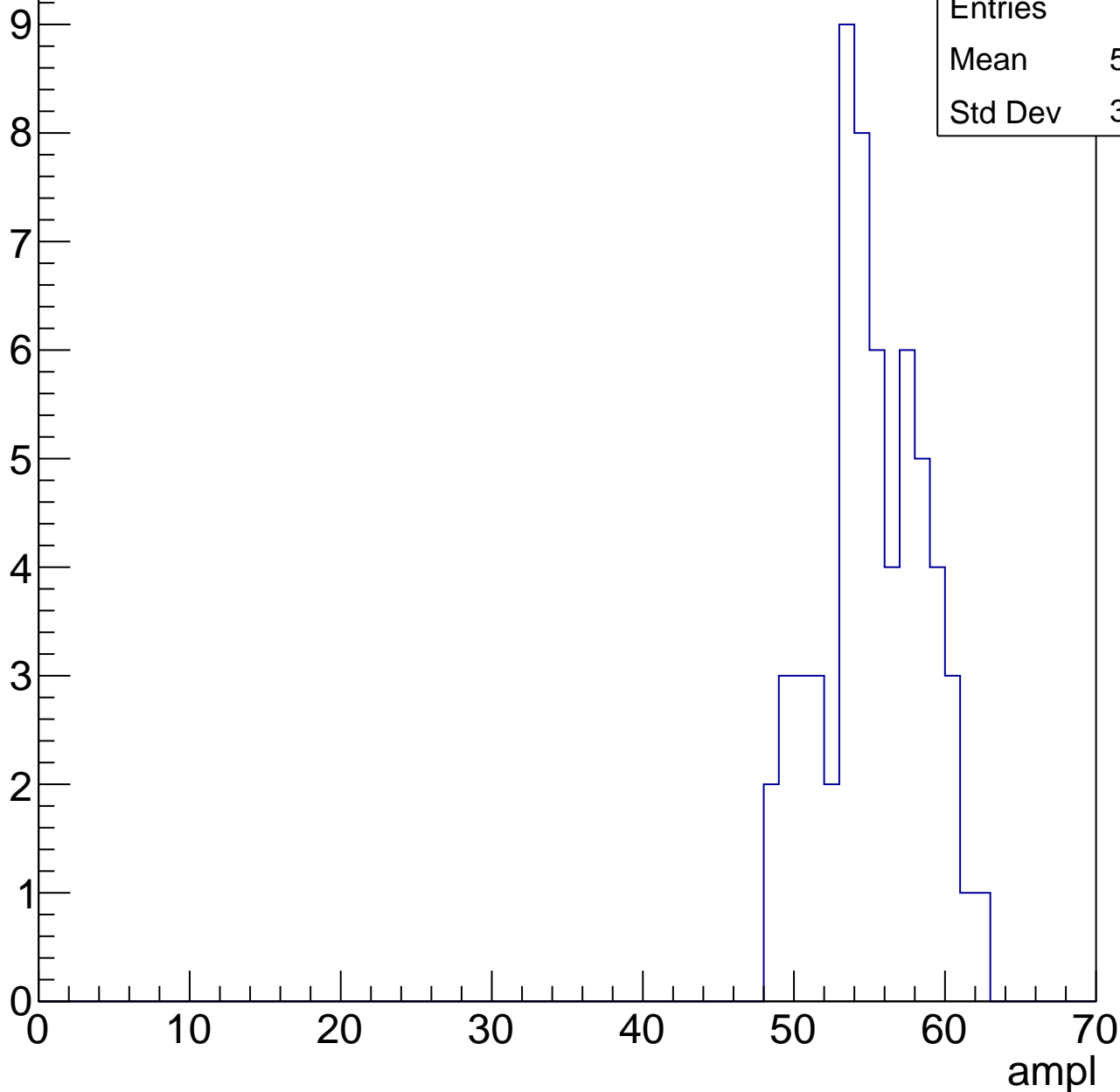


# B0L001S, U5-ch60, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	54.73
Std Dev	3.376

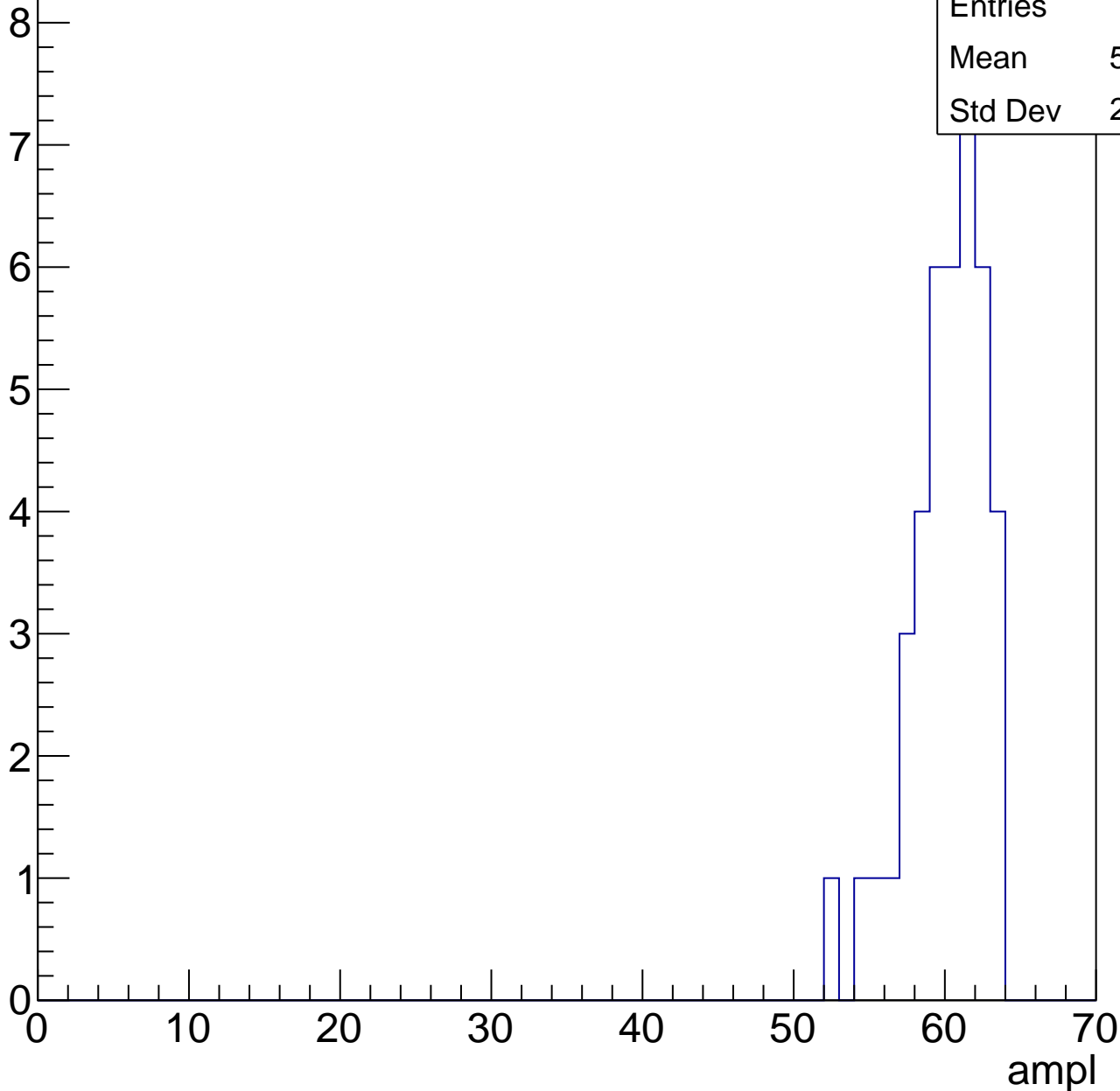


# B0L001S, U5-ch60, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	41
Mean	59.66
Std Dev	2.485

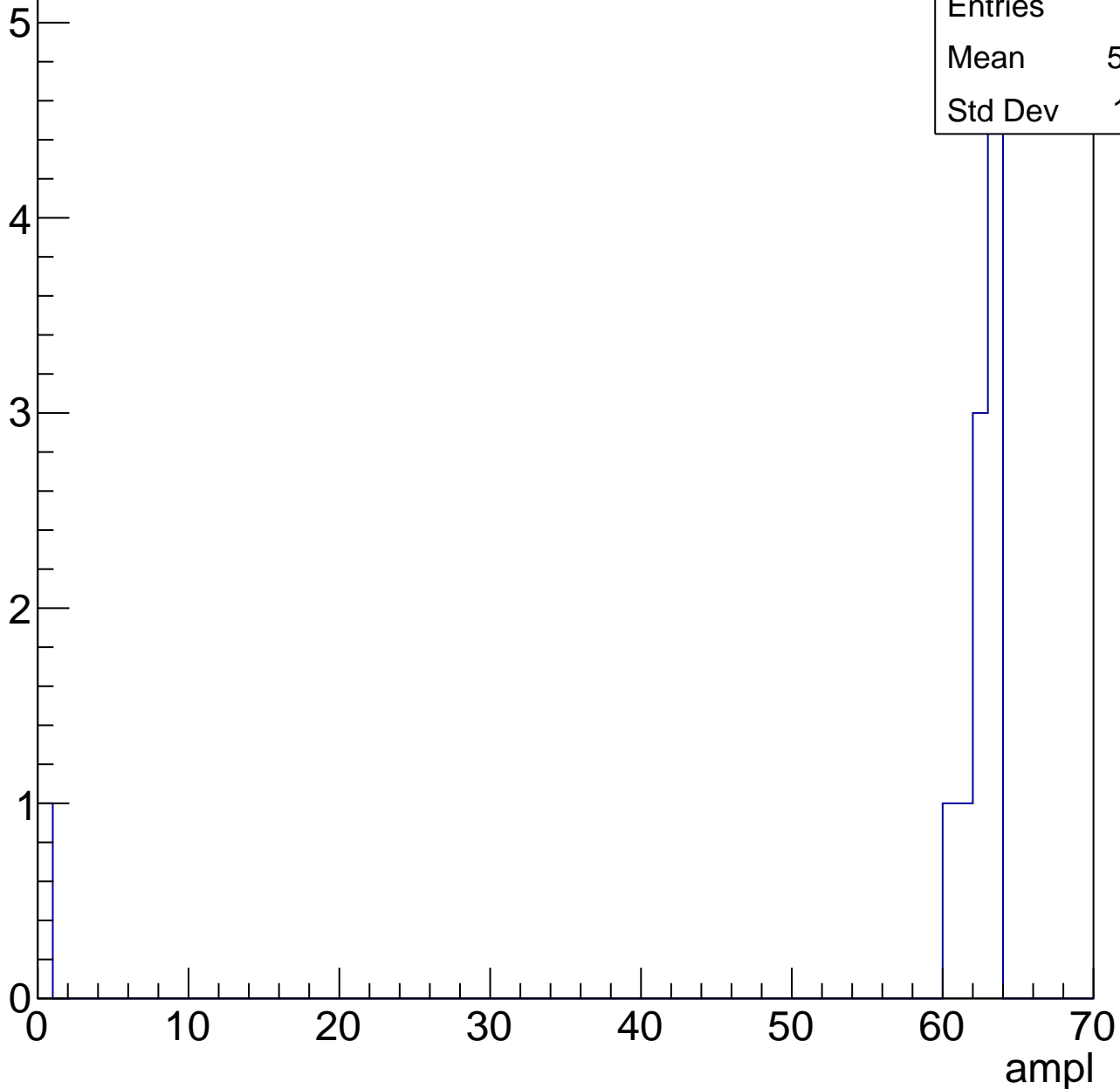


# B0L001S, U5-ch60, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	11
Mean	56.55
Std Dev	17.91





# B0L001S, U5-ch60, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch61, adc0

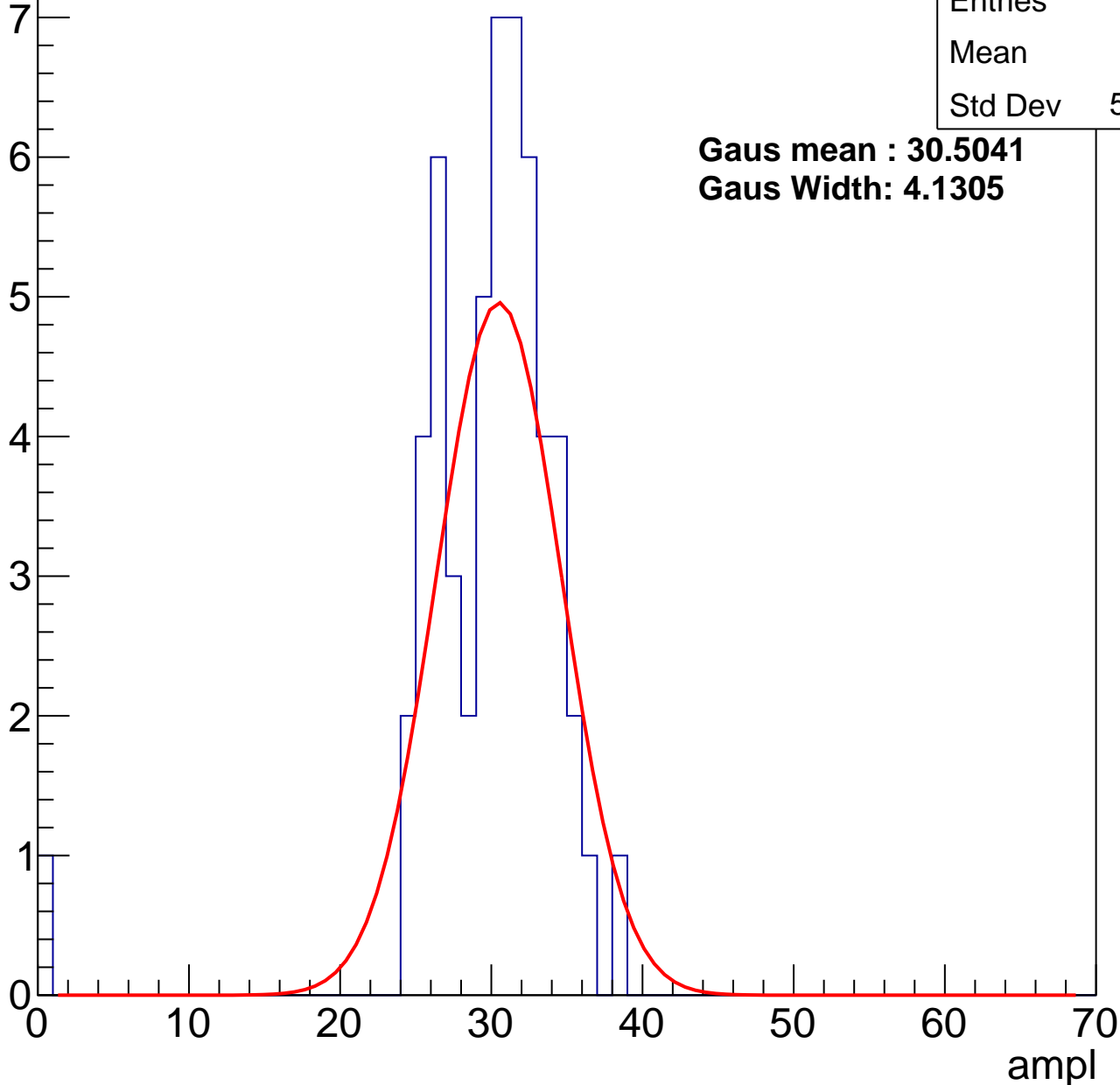
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	29.4
Std Dev	5.168

**Gaus mean : 30.5041**

**Gaus Width: 4.1305**



# B0L001S, U5-ch61, adc1

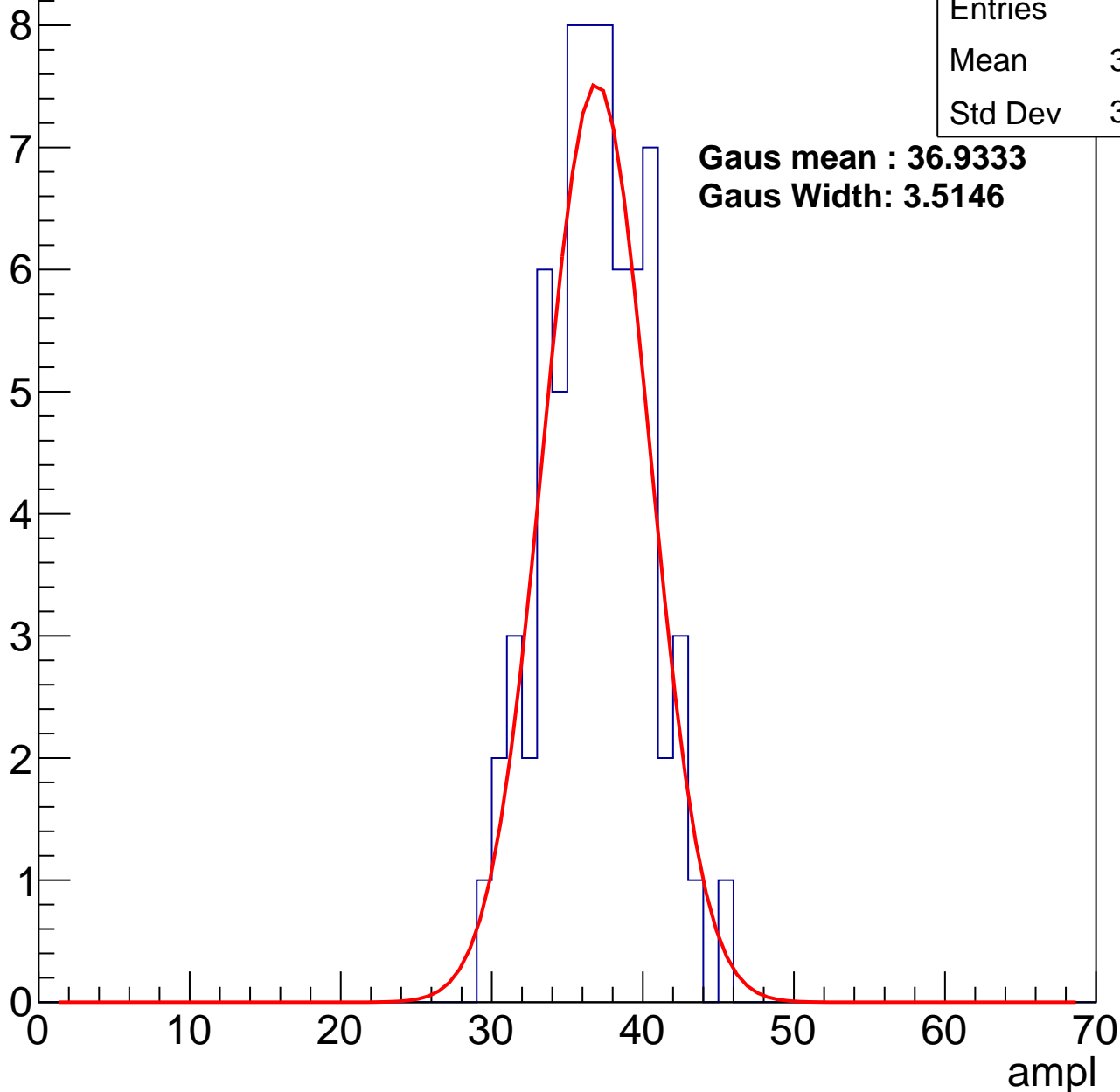
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	36.46
Std Dev	3.365

**Gaus mean : 36.9333**

**Gaus Width: 3.5146**



# B0L001S, U5-ch61, adc2

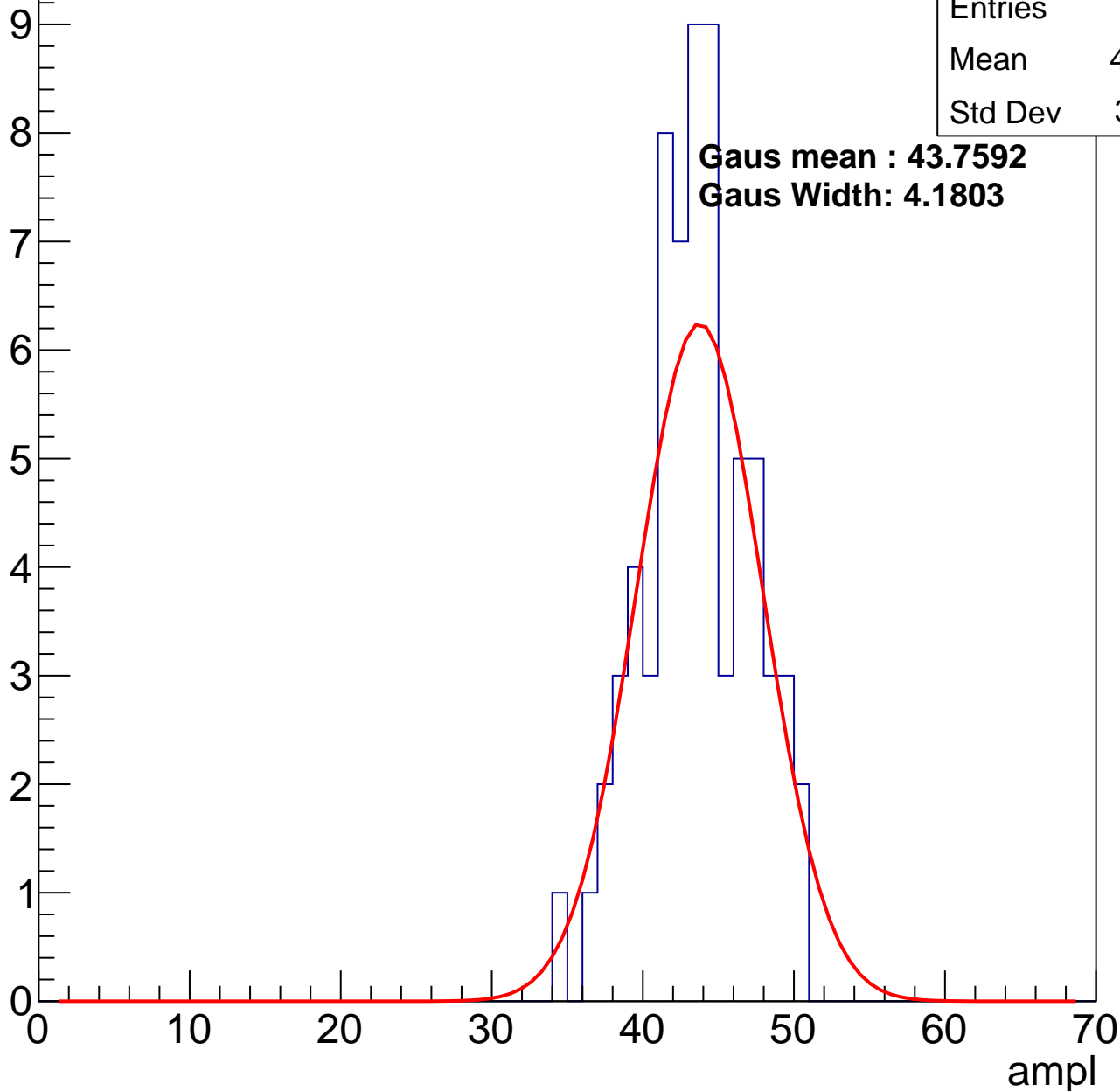
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	43.09
Std Dev	3.501

**Gaus mean : 43.7592**

**Gaus Width: 4.1803**

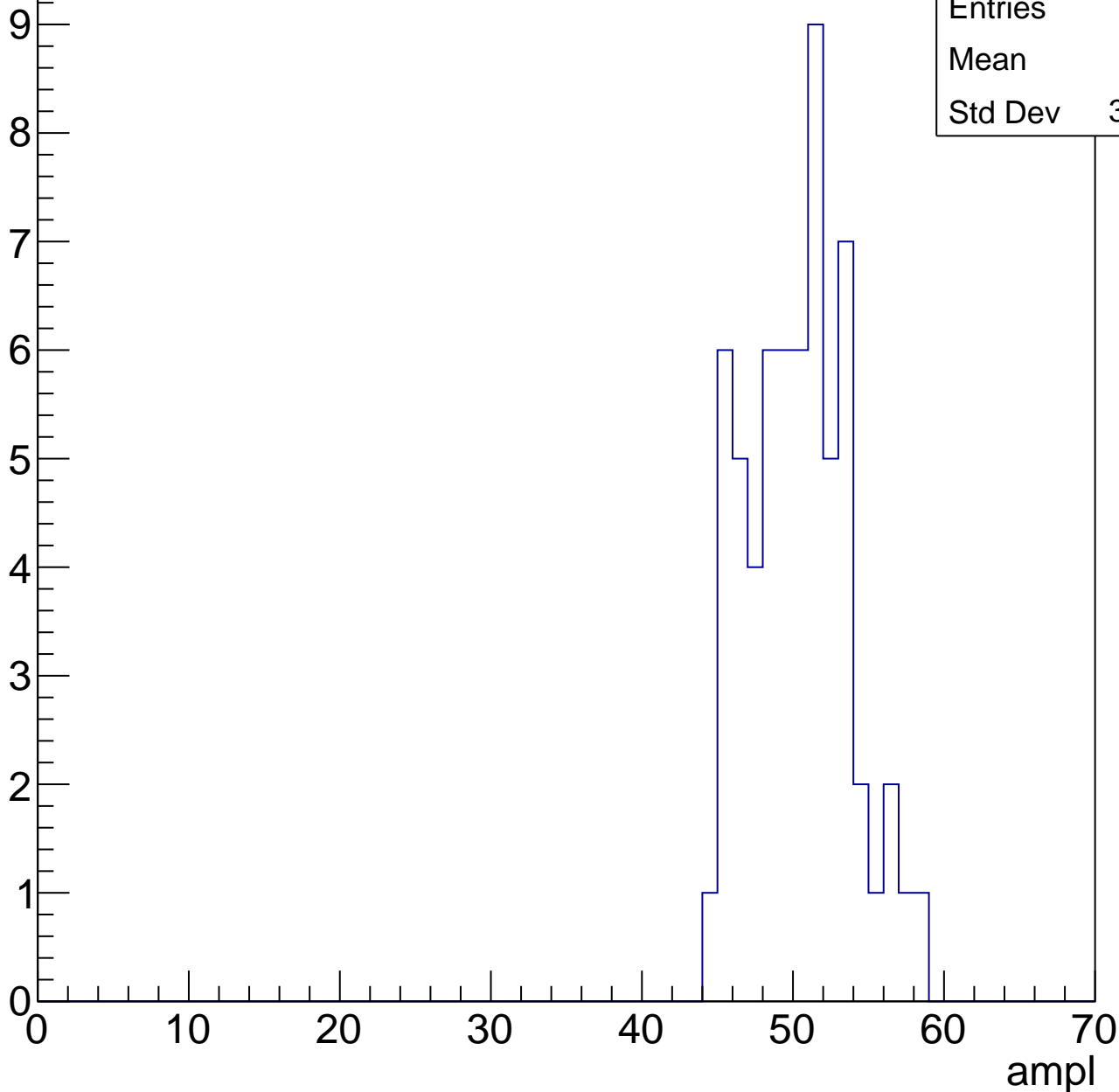


# B0L001S, U5-ch61, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

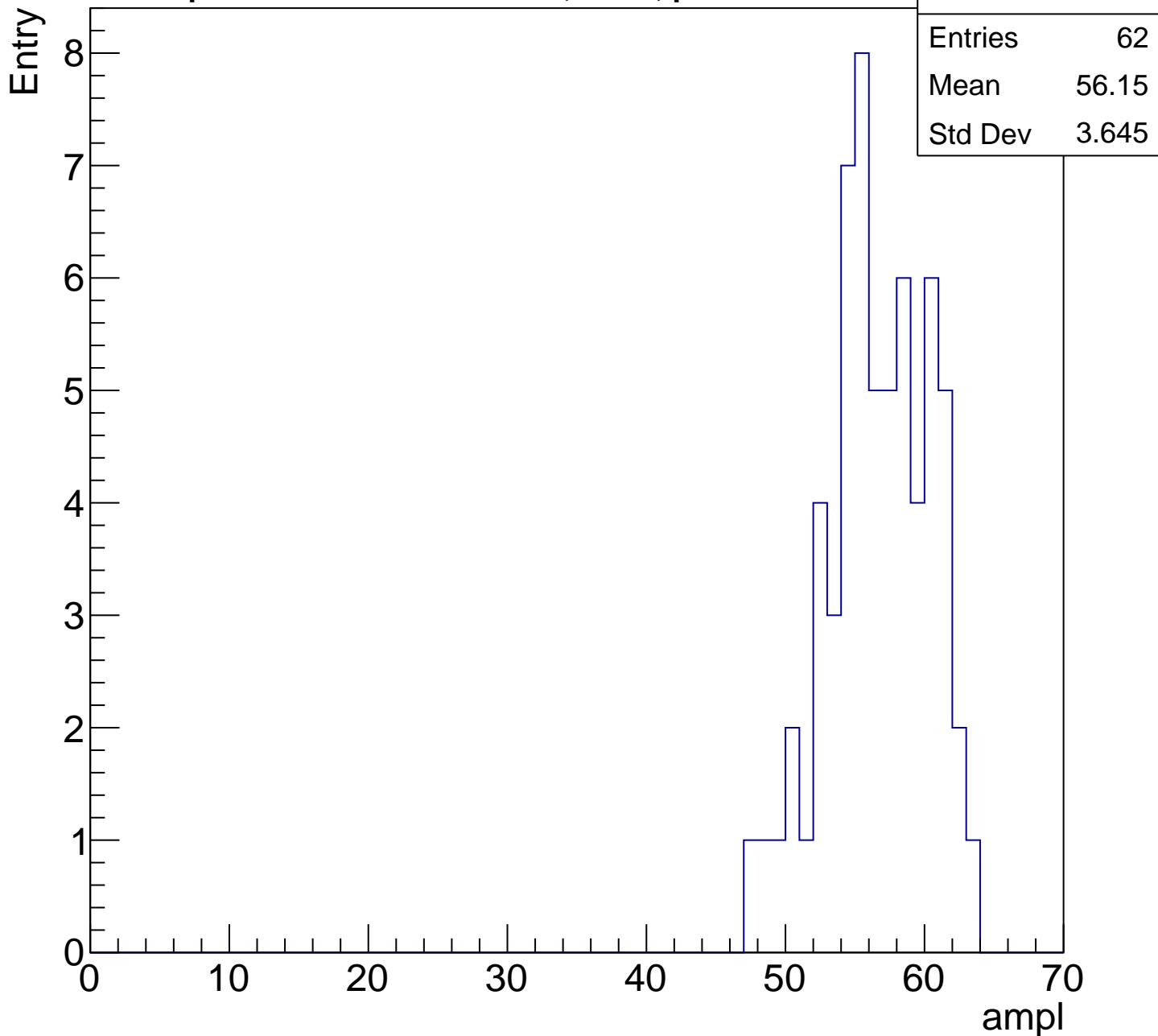
Entry

Entries	62
Mean	49.9
Std Dev	3.276



# B0L001S, U5-ch61, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

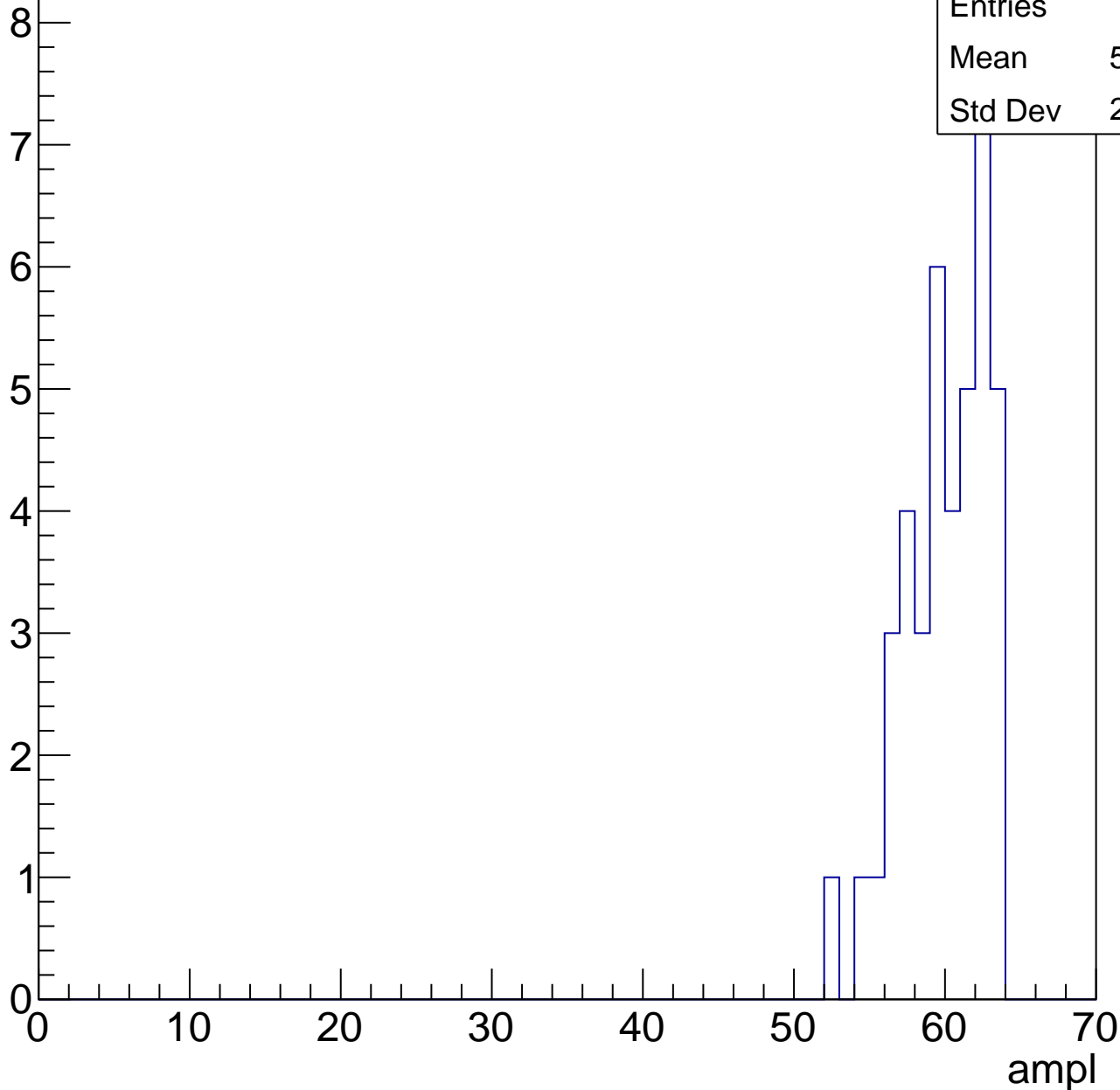


# B0L001S, U5-ch61, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

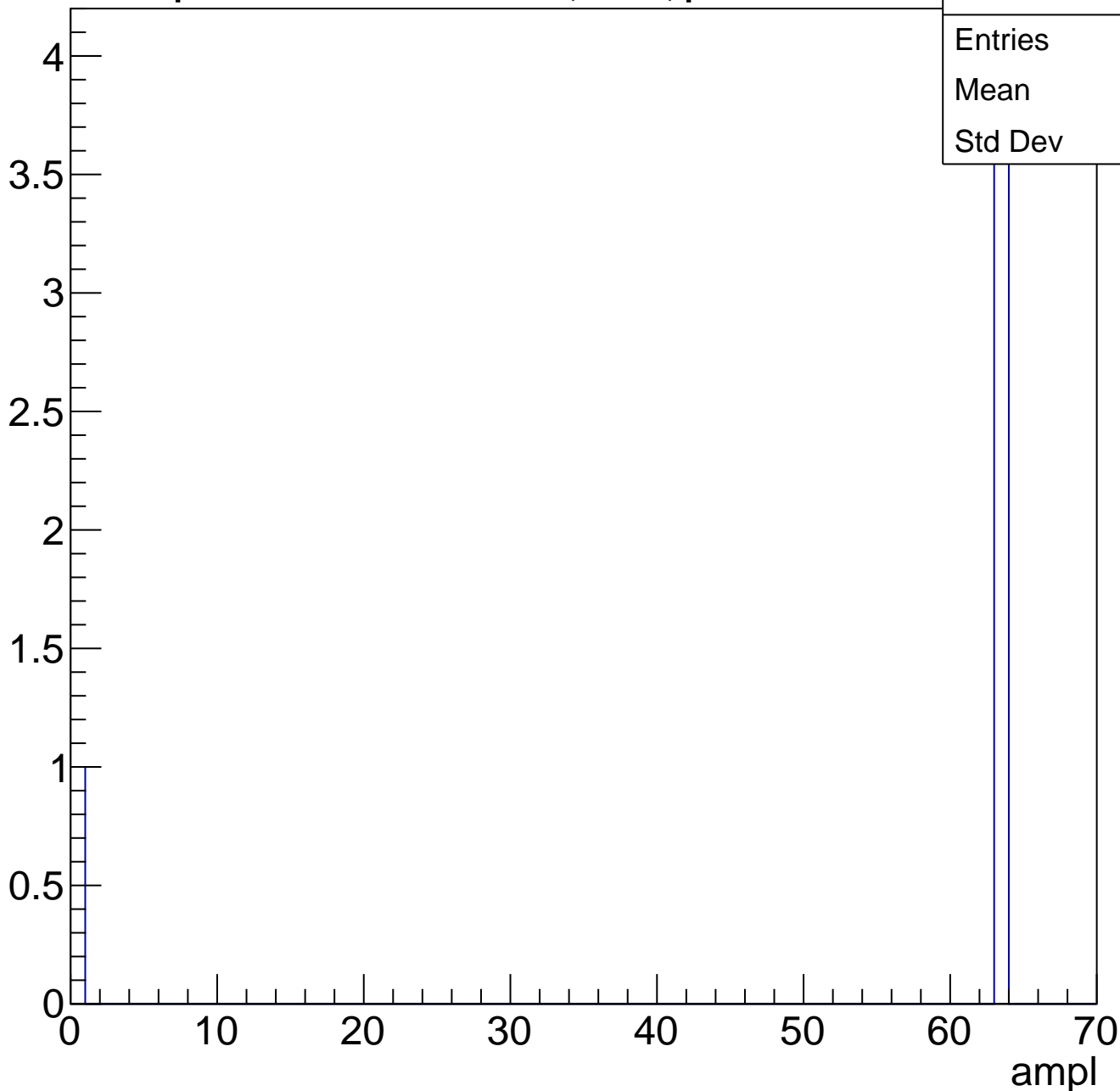
Entries	41
Mean	59.54
Std Dev	2.706



# B0L001S, U5-ch61, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch61, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch62, adc0

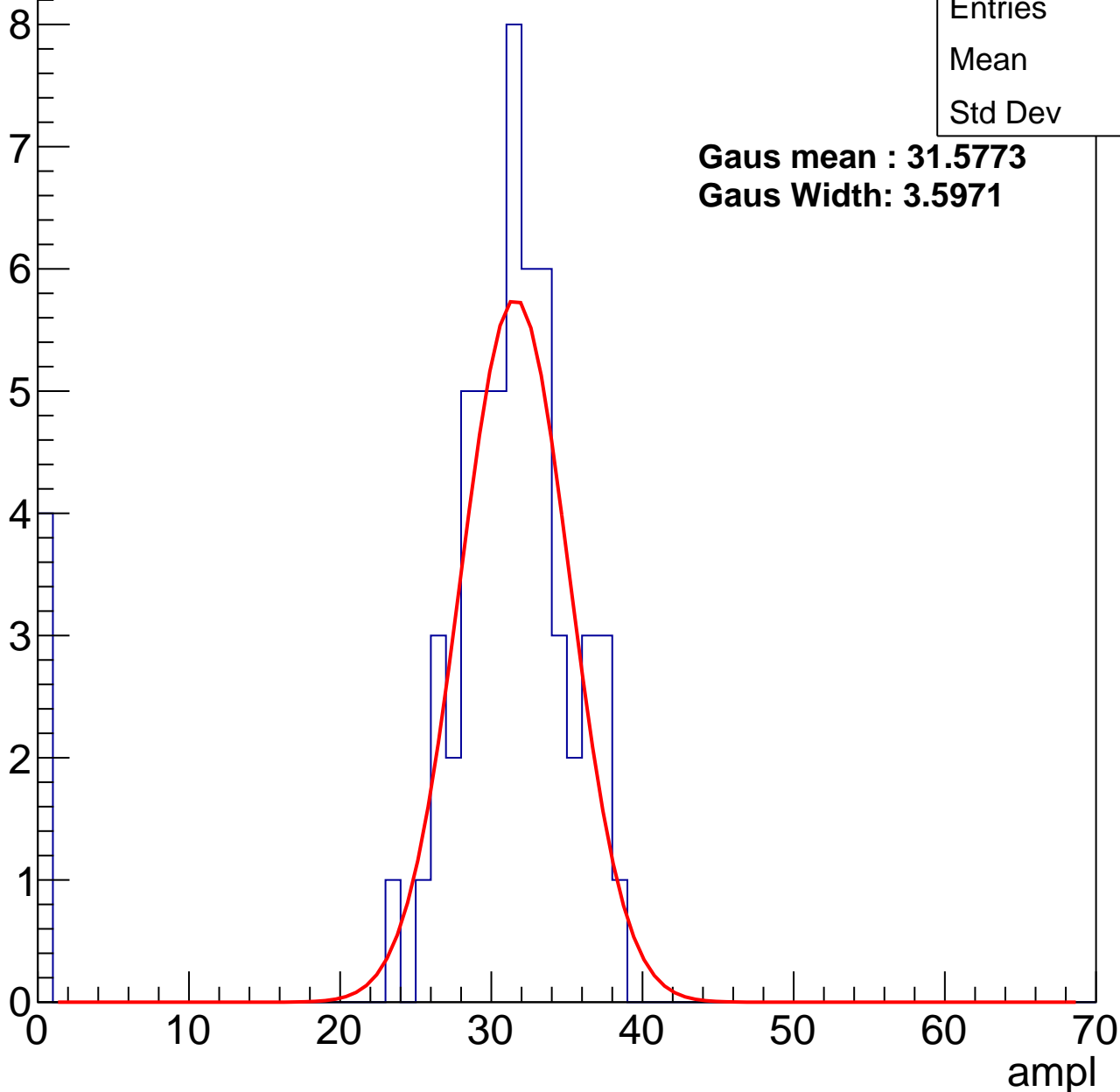
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	29
Std Dev	8.52

**Gaus mean : 31.5773**

**Gaus Width: 3.5971**



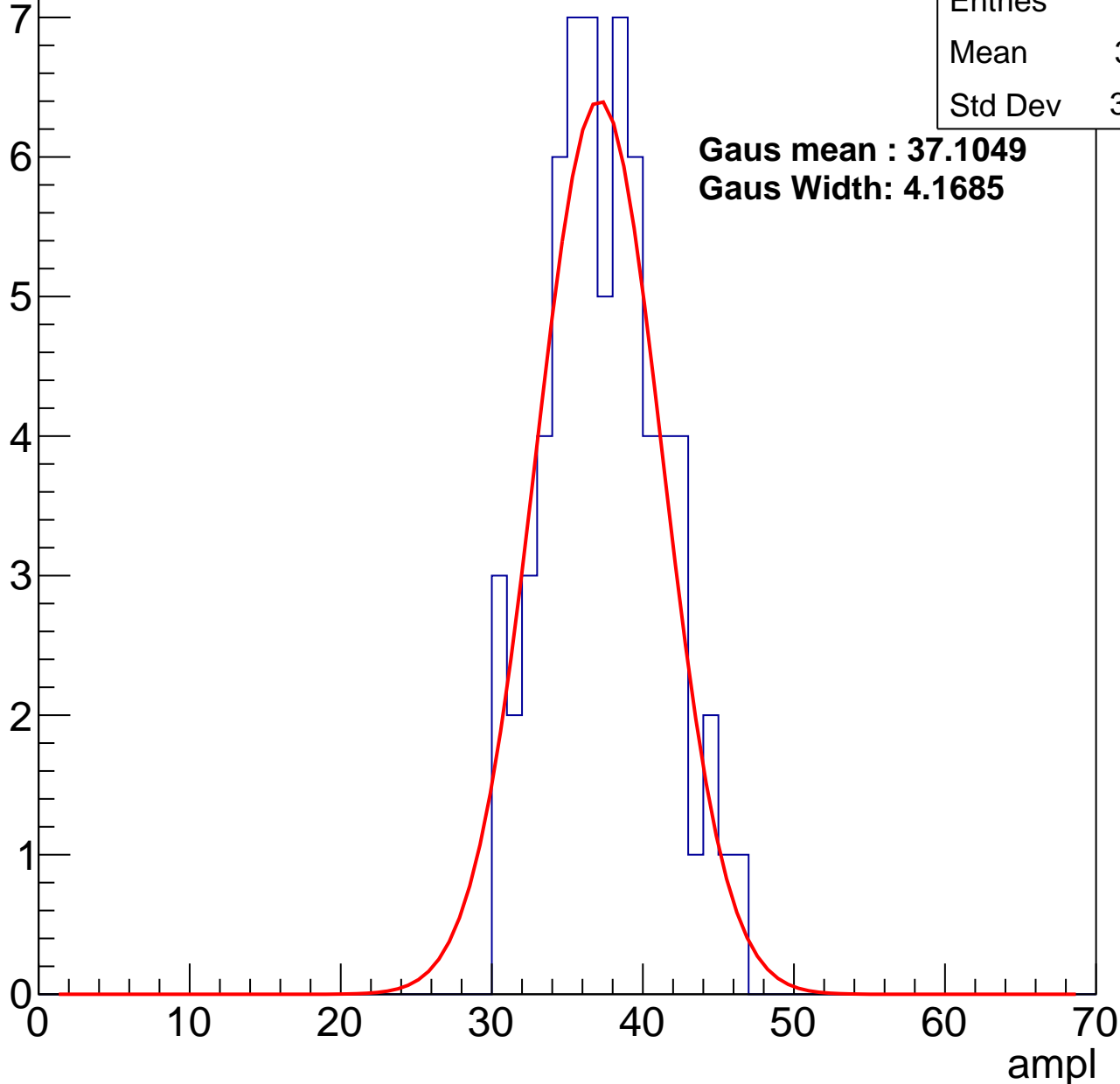
# B0L001S, U5-ch62, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	37.01
Std Dev	3.779

**Gaus mean : 37.1049**  
**Gaus Width: 4.1685**



# B0L001S, U5-ch62, adc2

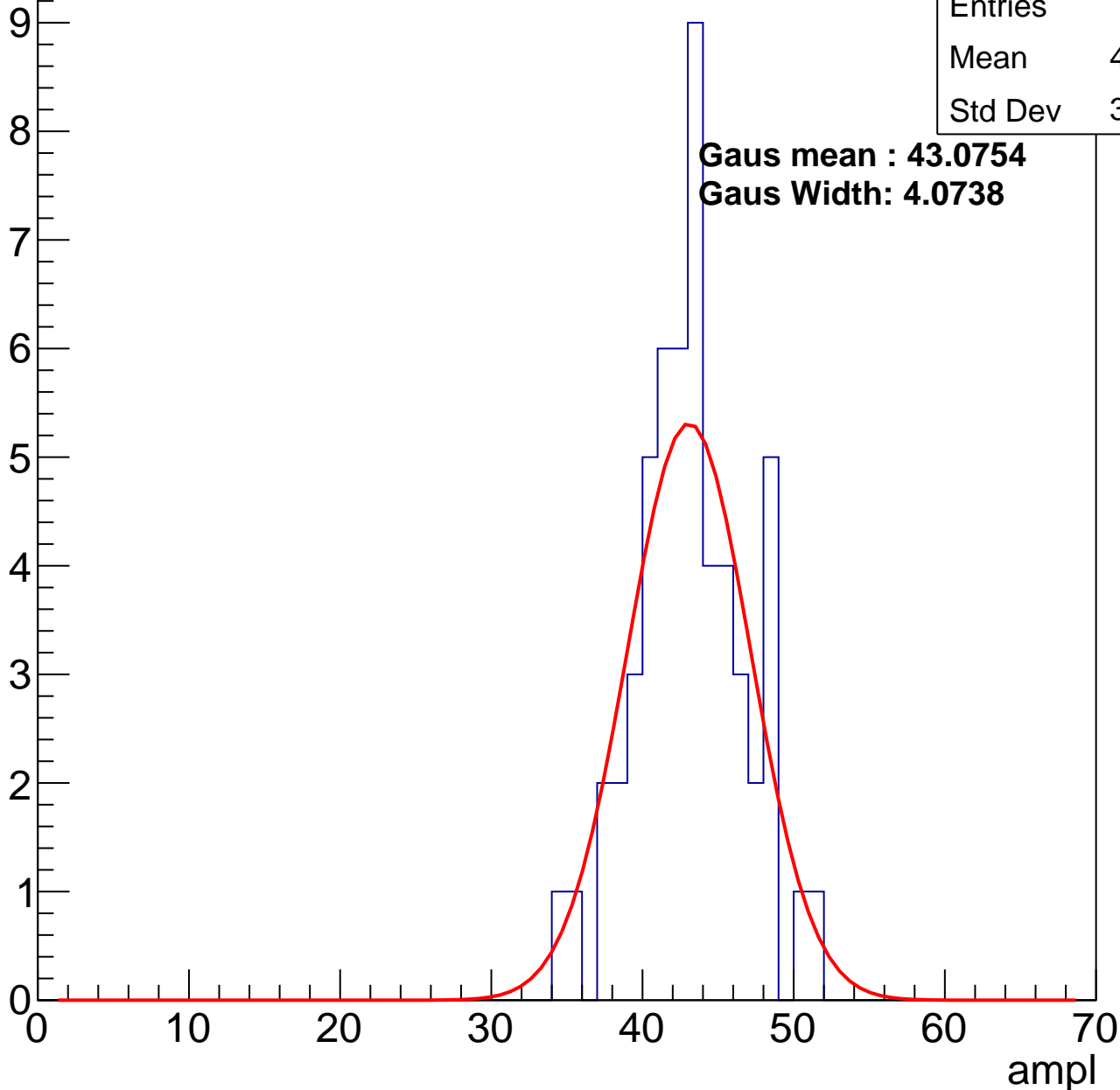
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	42.73
Std Dev	3.575

**Gaus mean : 43.0754**

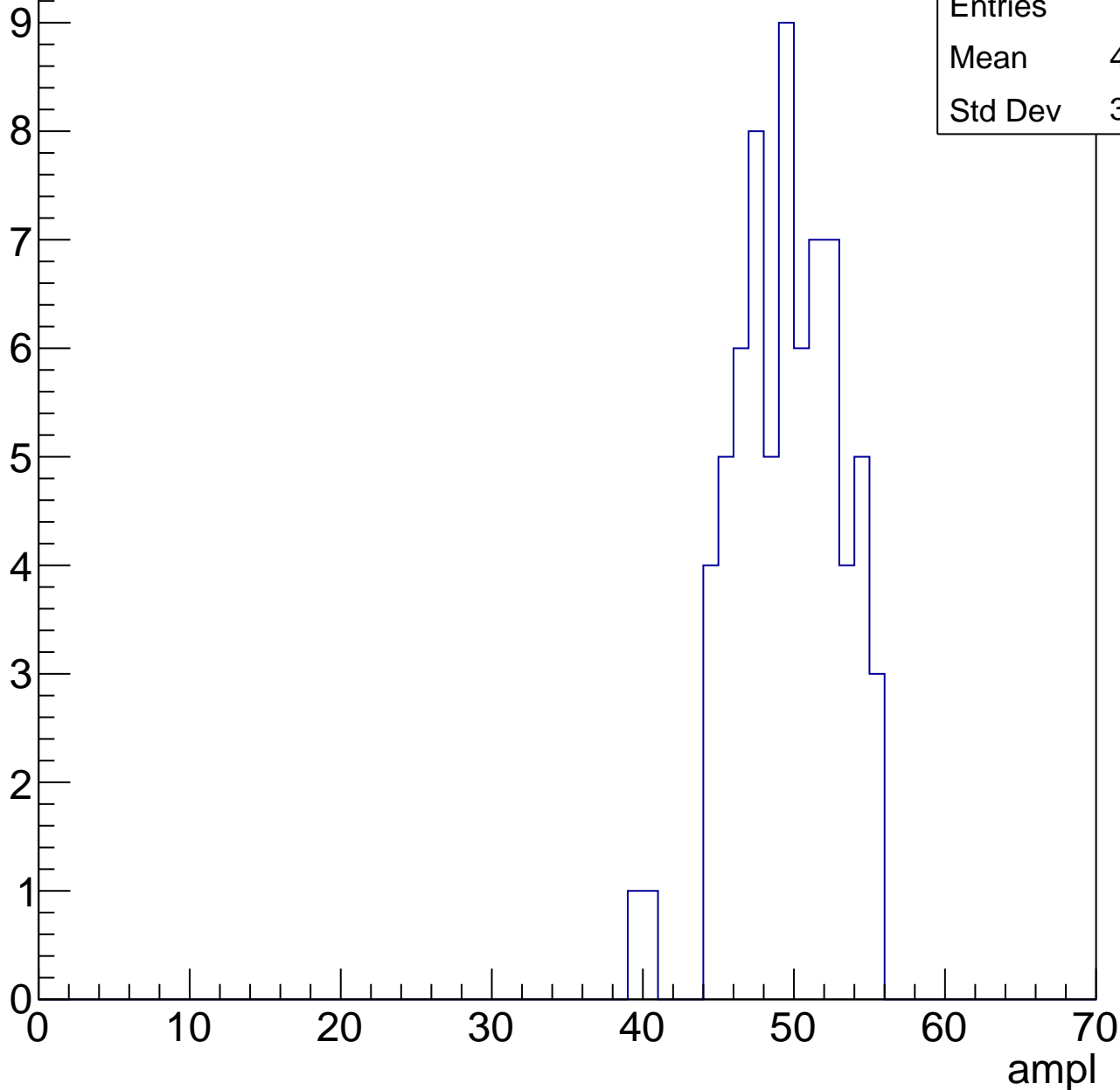
**Gaus Width: 4.0738**



# B0L001S, U5-ch62, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

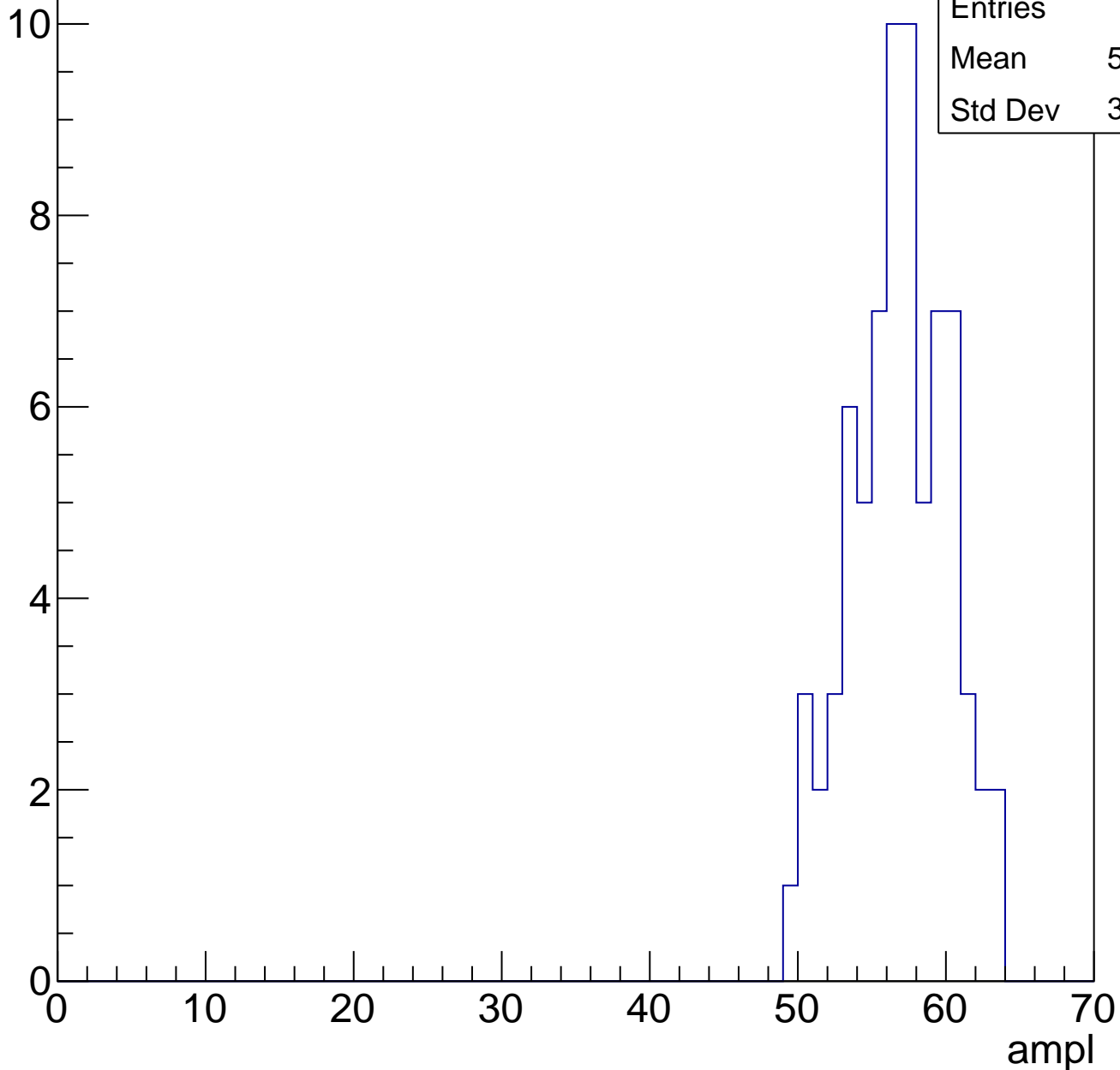


# B0L001S, U5-ch62, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	73
Mean	56.38
Std Dev	3.259

Entry

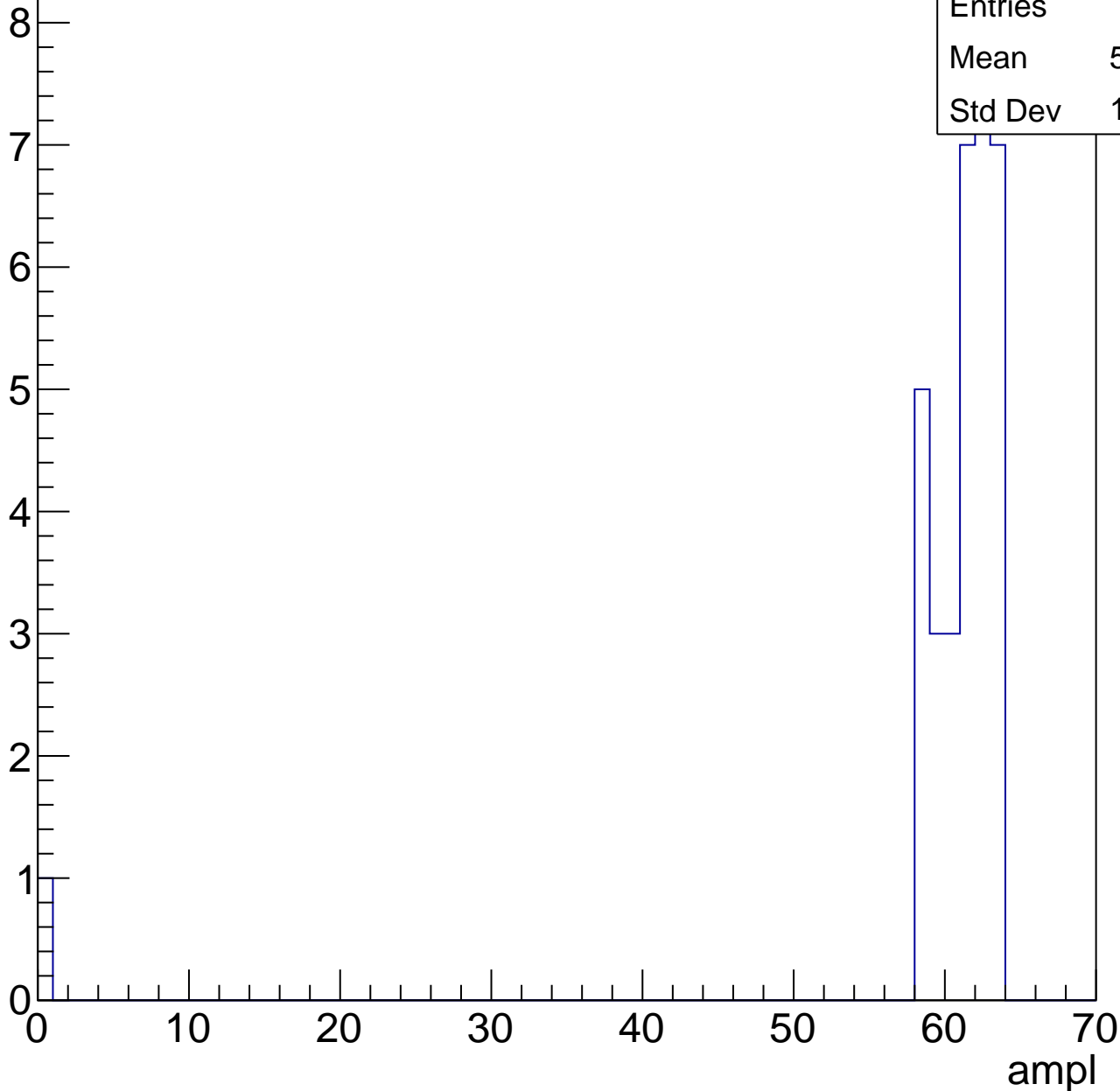


# B0L001S, U5-ch62, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	34
Mean	59.15
Std Dev	10.43



# B0L001S, U5-ch62, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch62, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch63, adc0

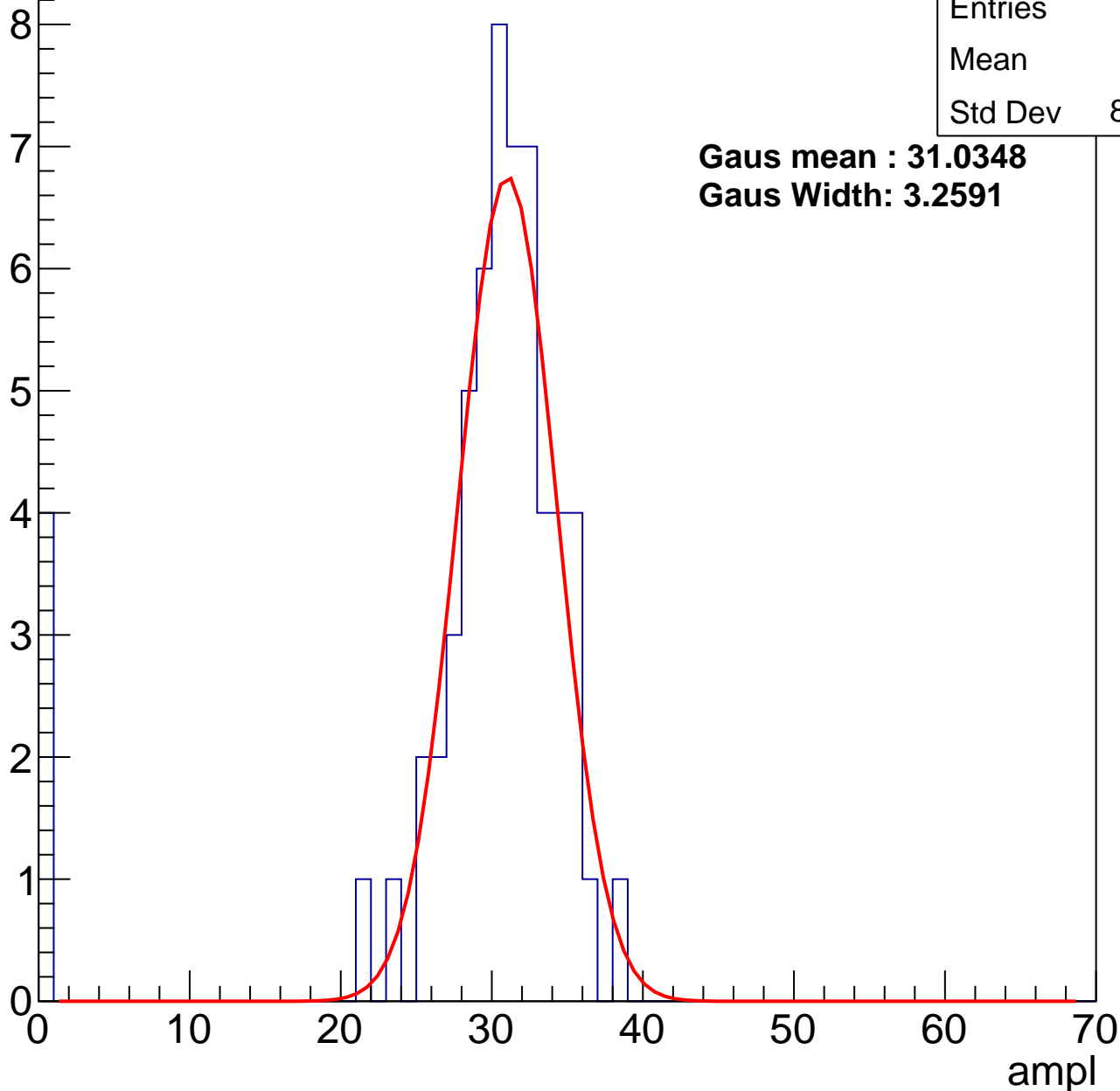
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	28.4
Std Dev	8.212

**Gaus mean : 31.0348**

**Gaus Width: 3.2591**



# B0L001S, U5-ch63, adc1

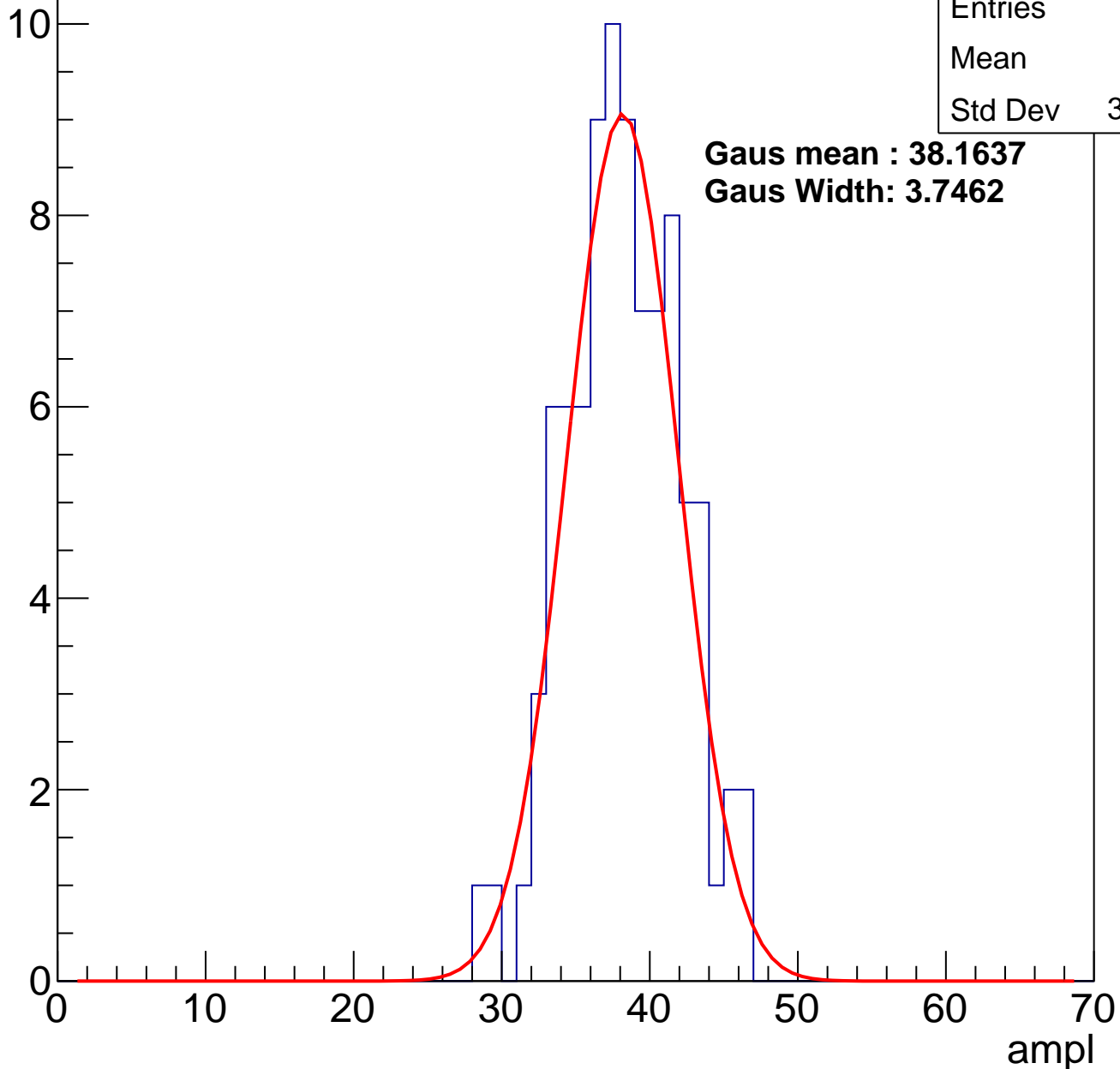
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	89
Mean	37.8
Std Dev	3.754

**Gaus mean : 38.1637**

**Gaus Width: 3.7462**

Entry



# B0L001S, U5-ch63, adc2

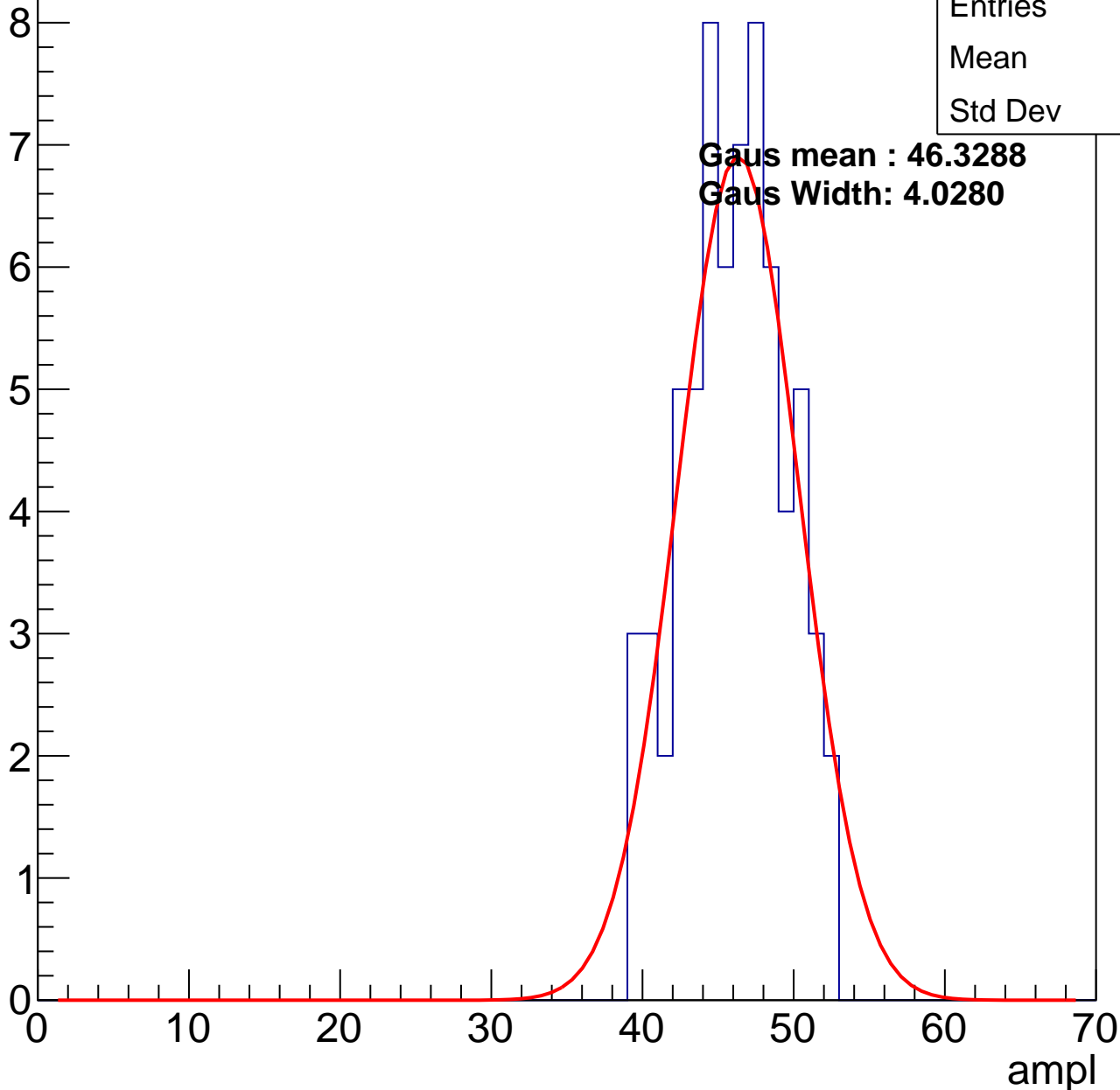
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	45.6
Std Dev	3.35

Gaus mean : 46.3288

Gaus Width: 4.0280

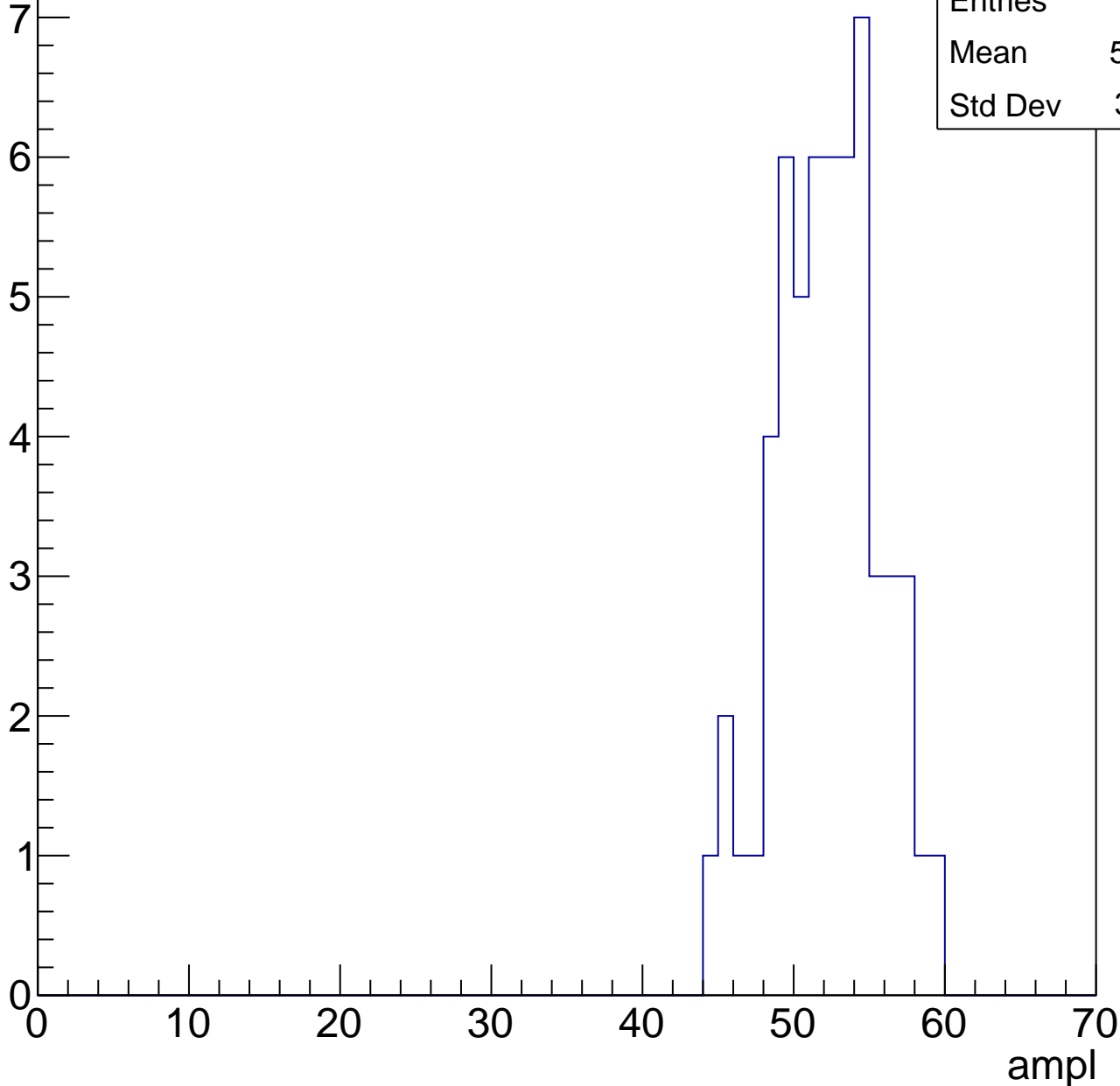


# B0L001S, U5-ch63, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	51.75
Std Dev	3.361

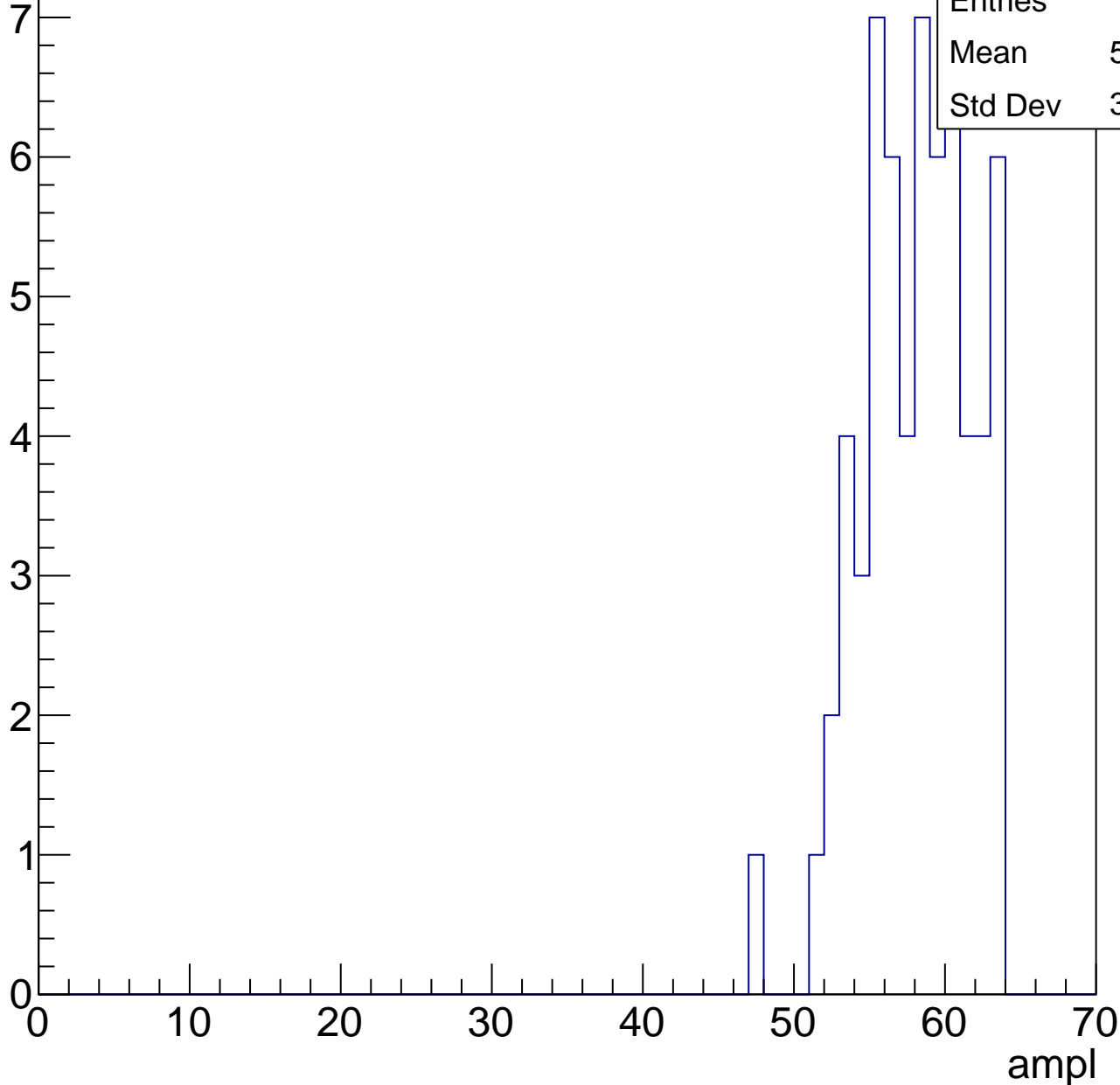


# B0L001S, U5-ch63, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	57.66
Std Dev	3.496

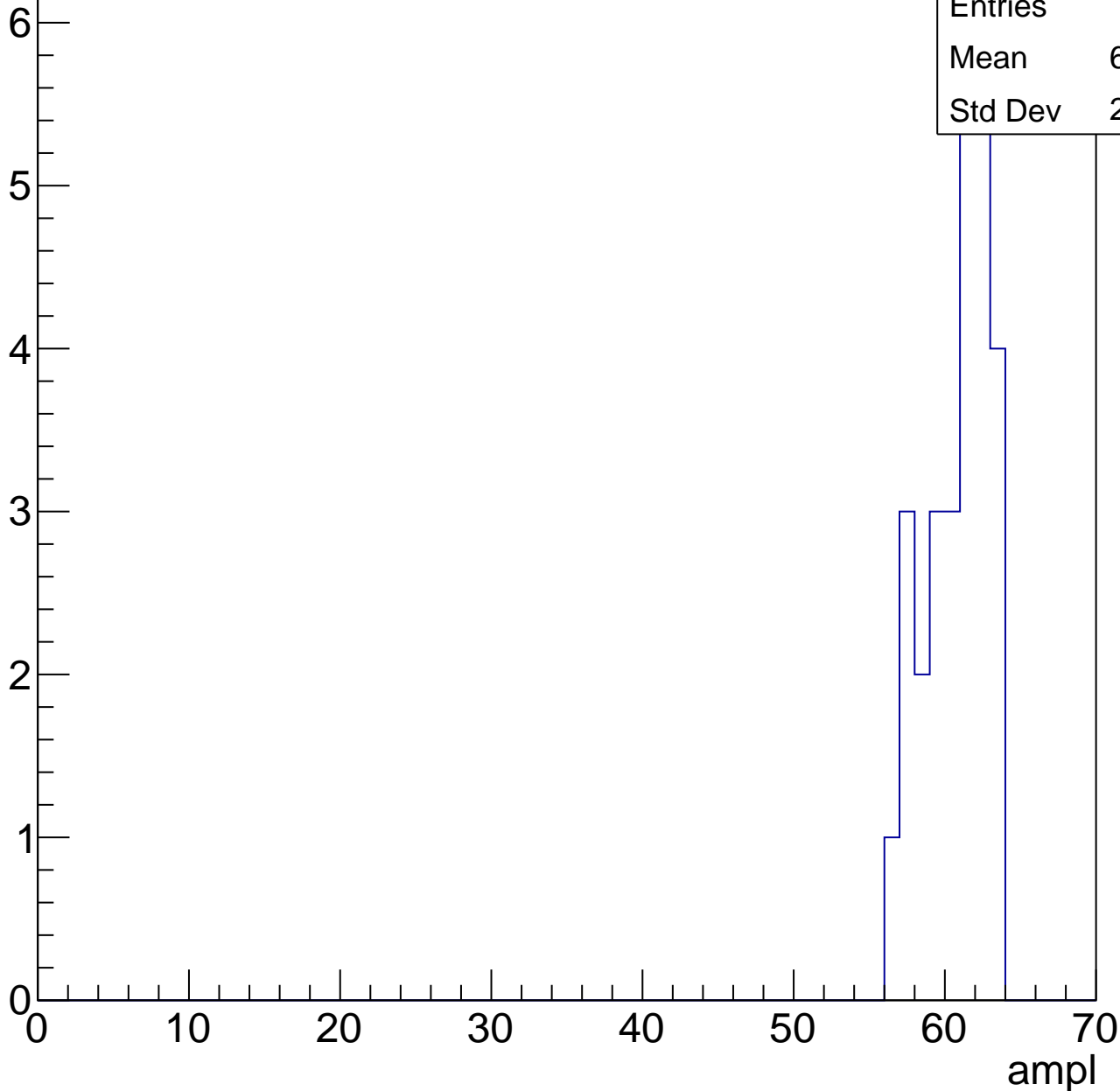


# B0L001S, U5-ch63, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	28
Mean	60.36
Std Dev	2.039



# B0L001S, U5-ch63, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0



# B0L001S, U5-ch63, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U5-ch64, adc0

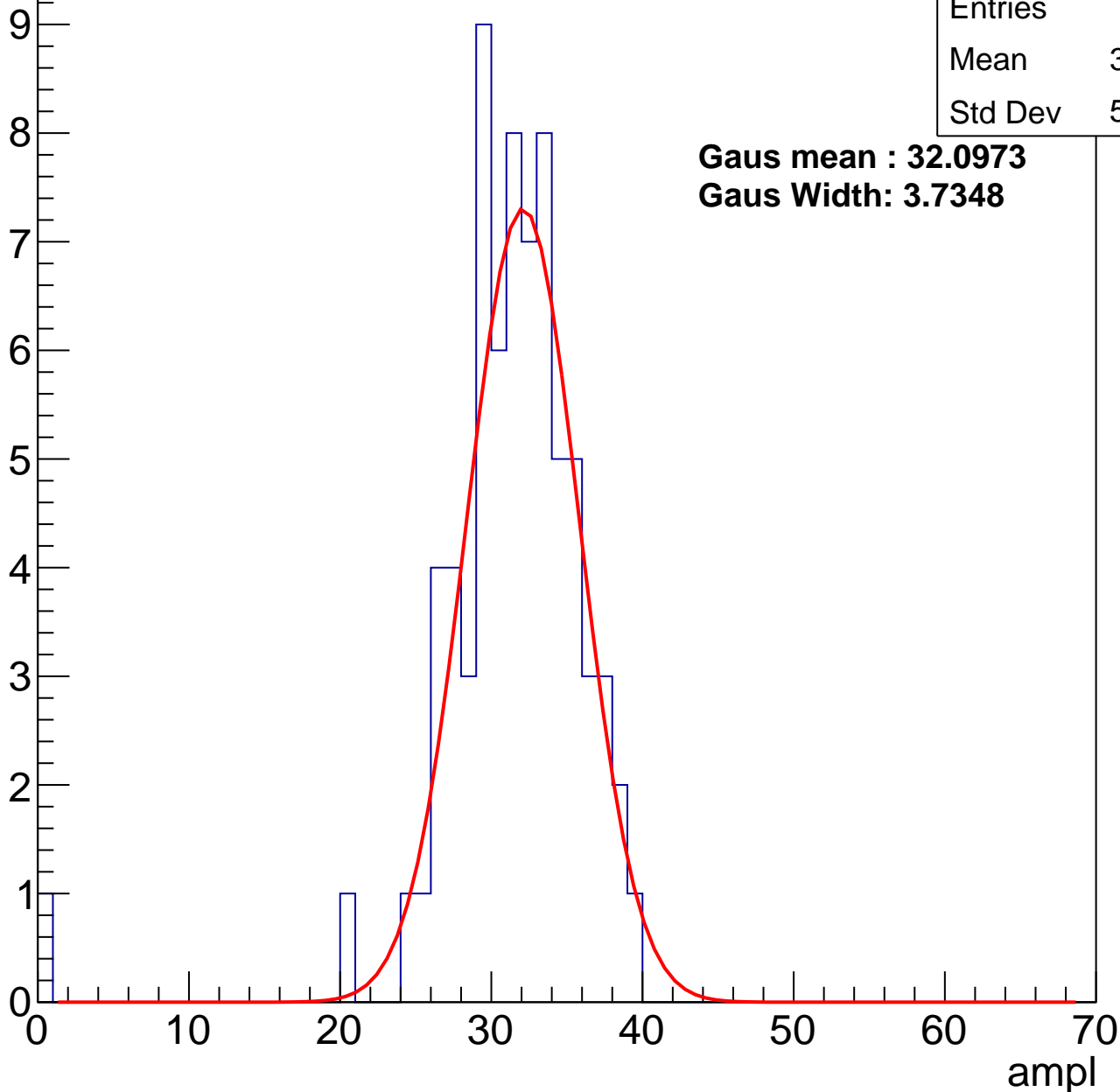
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	30.85
Std Dev	5.147

**Gaus mean : 32.0973**

**Gaus Width: 3.7348**



# B0L001S, U5-ch64, adc1

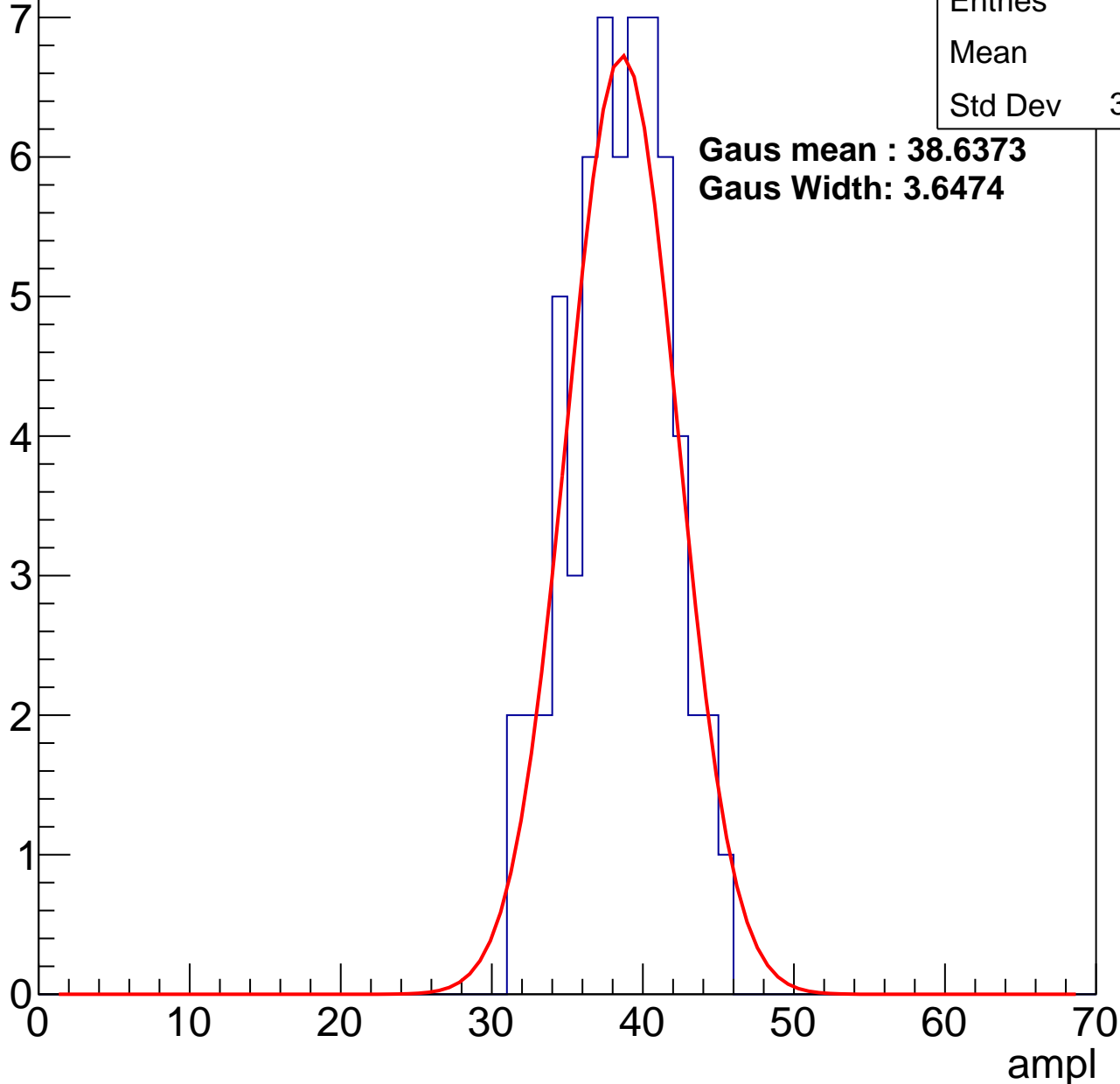
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	38
Std Dev	3.317

**Gaus mean : 38.6373**

**Gaus Width: 3.6474**



# B0L001S, U5-ch64, adc2

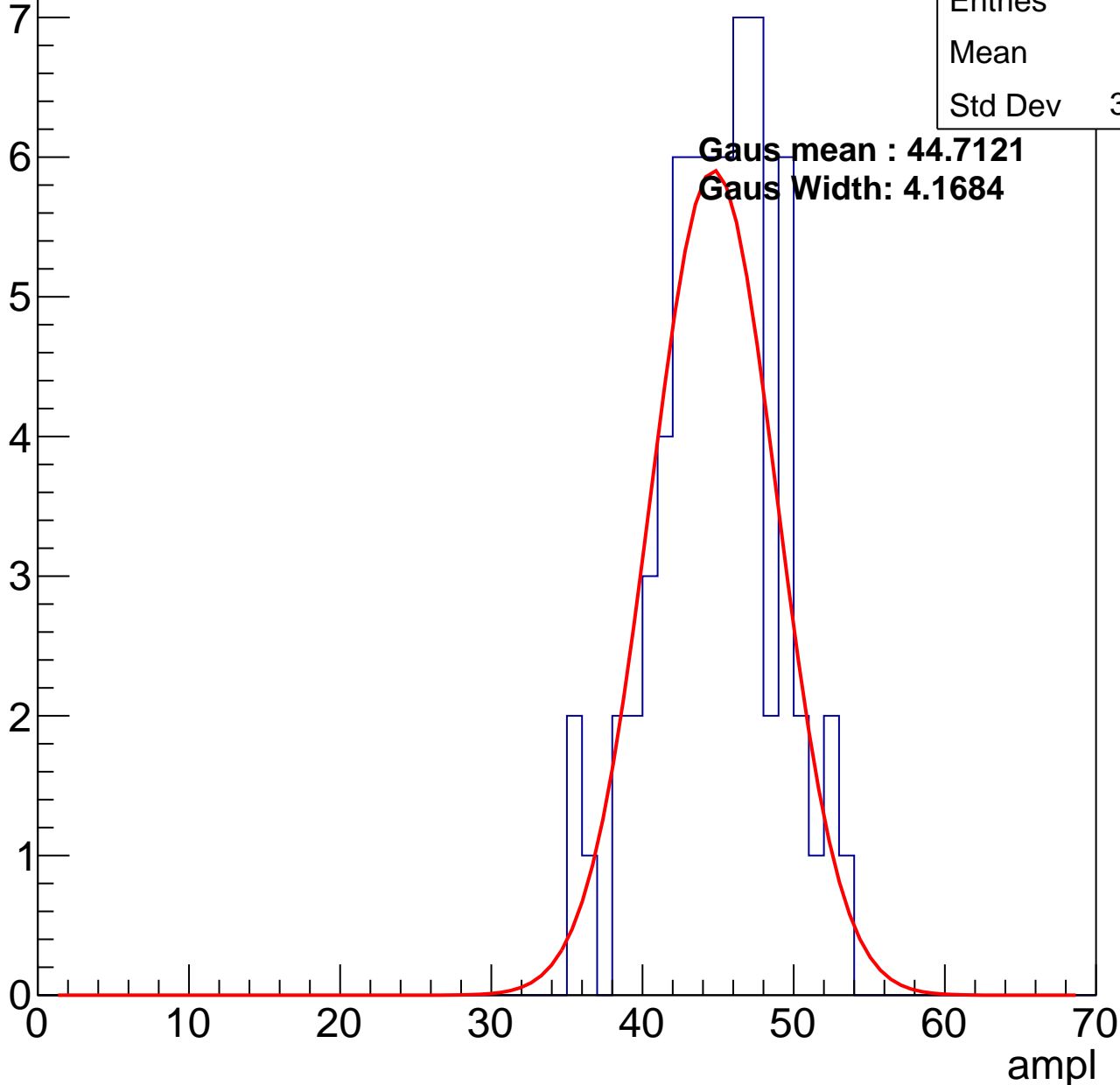
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	44.5
Std Dev	3.997

**Gaus mean : 44.7121**

**Gaus Width: 4.1684**

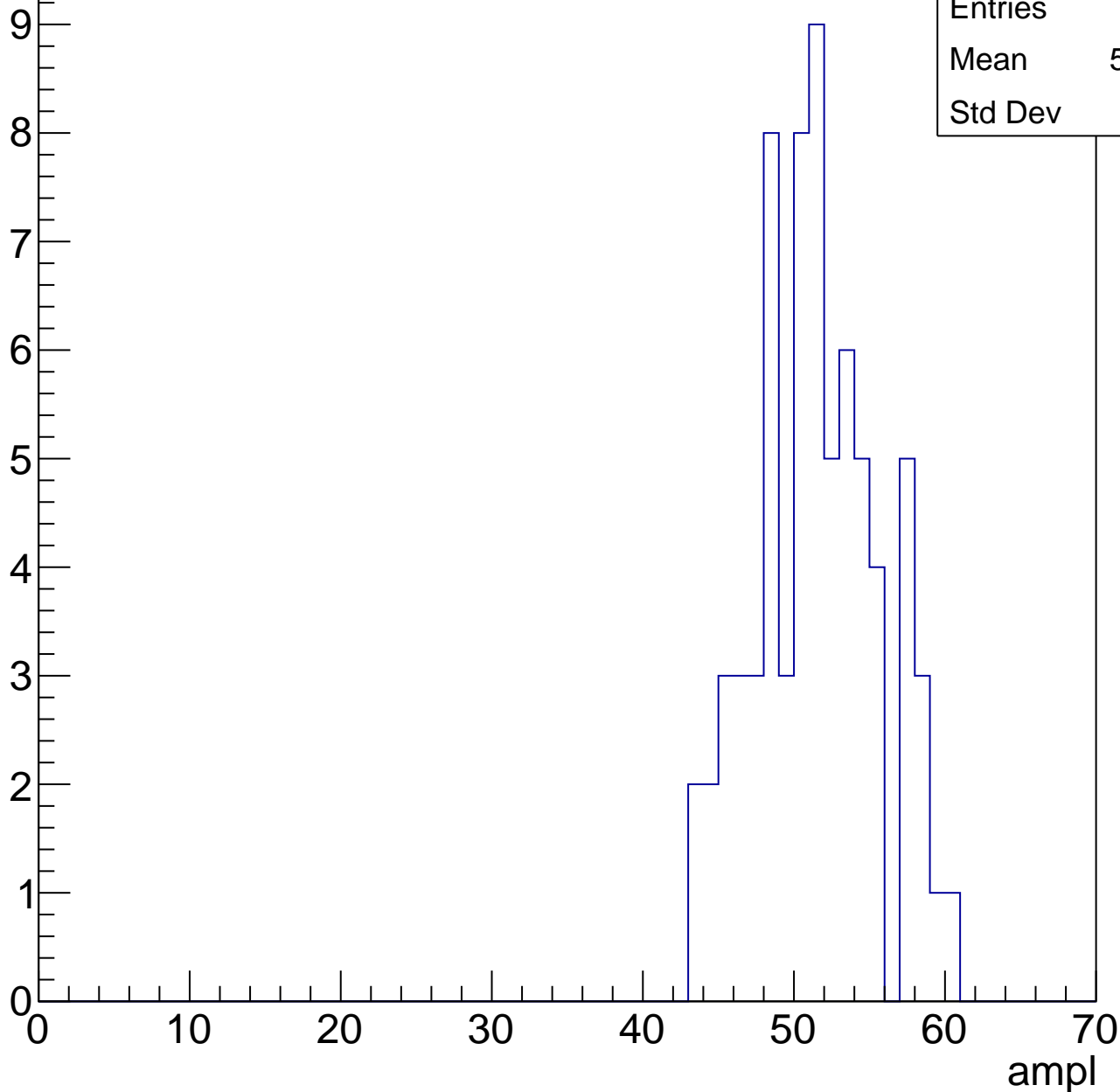


# B0L001S, U5-ch64, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	51.04
Std Dev	4.04

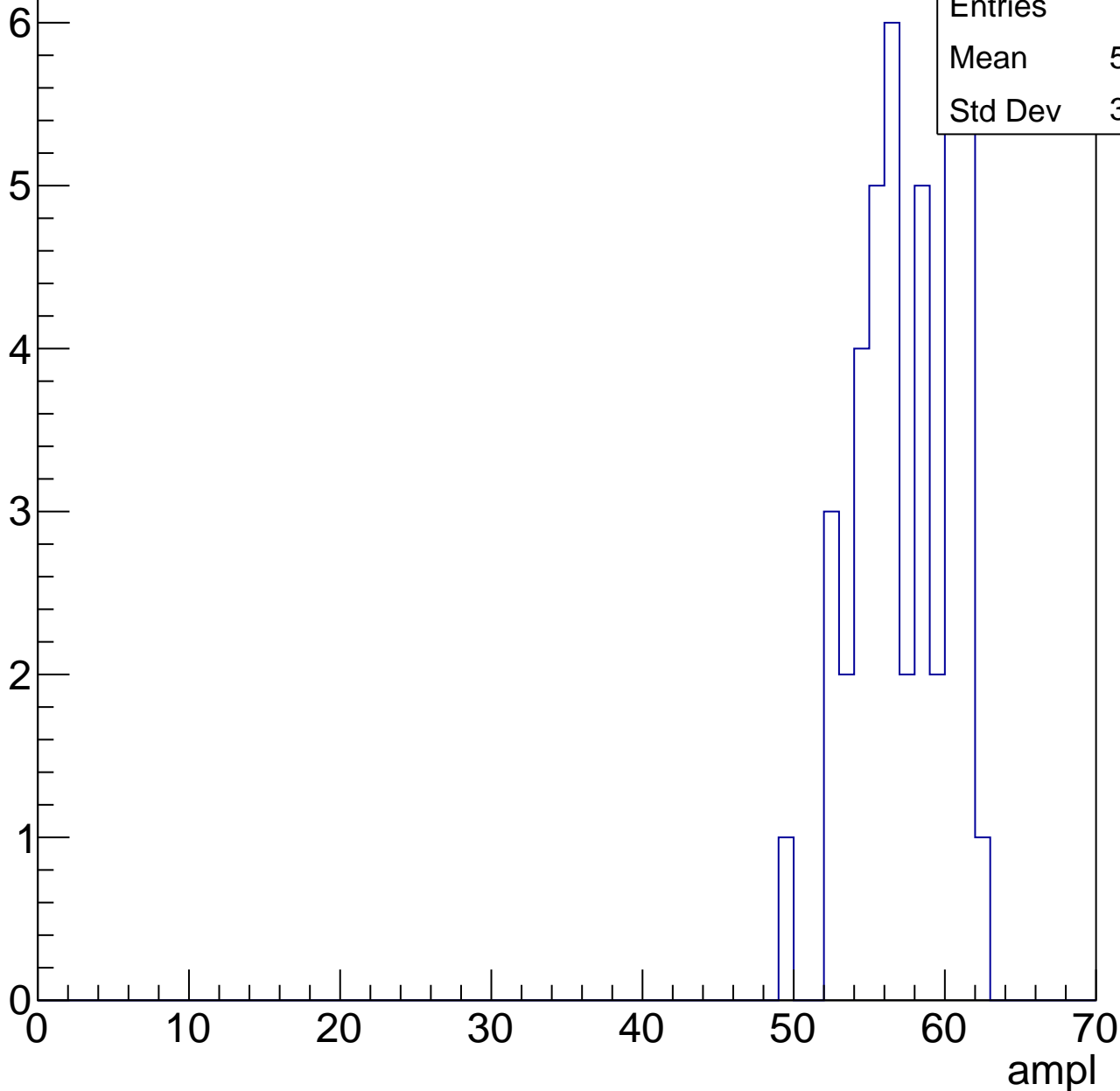


# B0L001S, U5-ch64, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	43
Mean	56.93
Std Dev	3.128

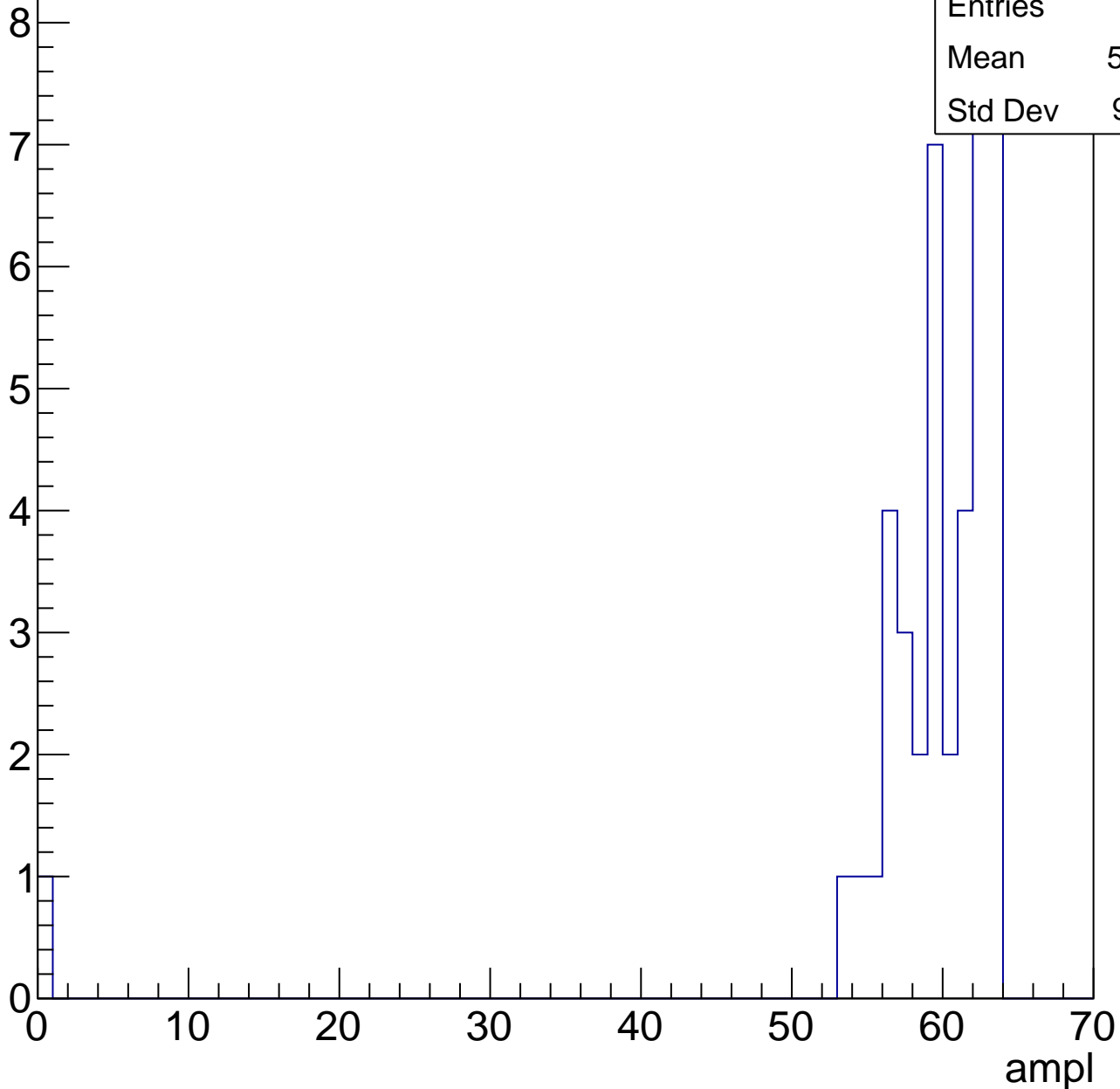


# B0L001S, U5-ch64, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

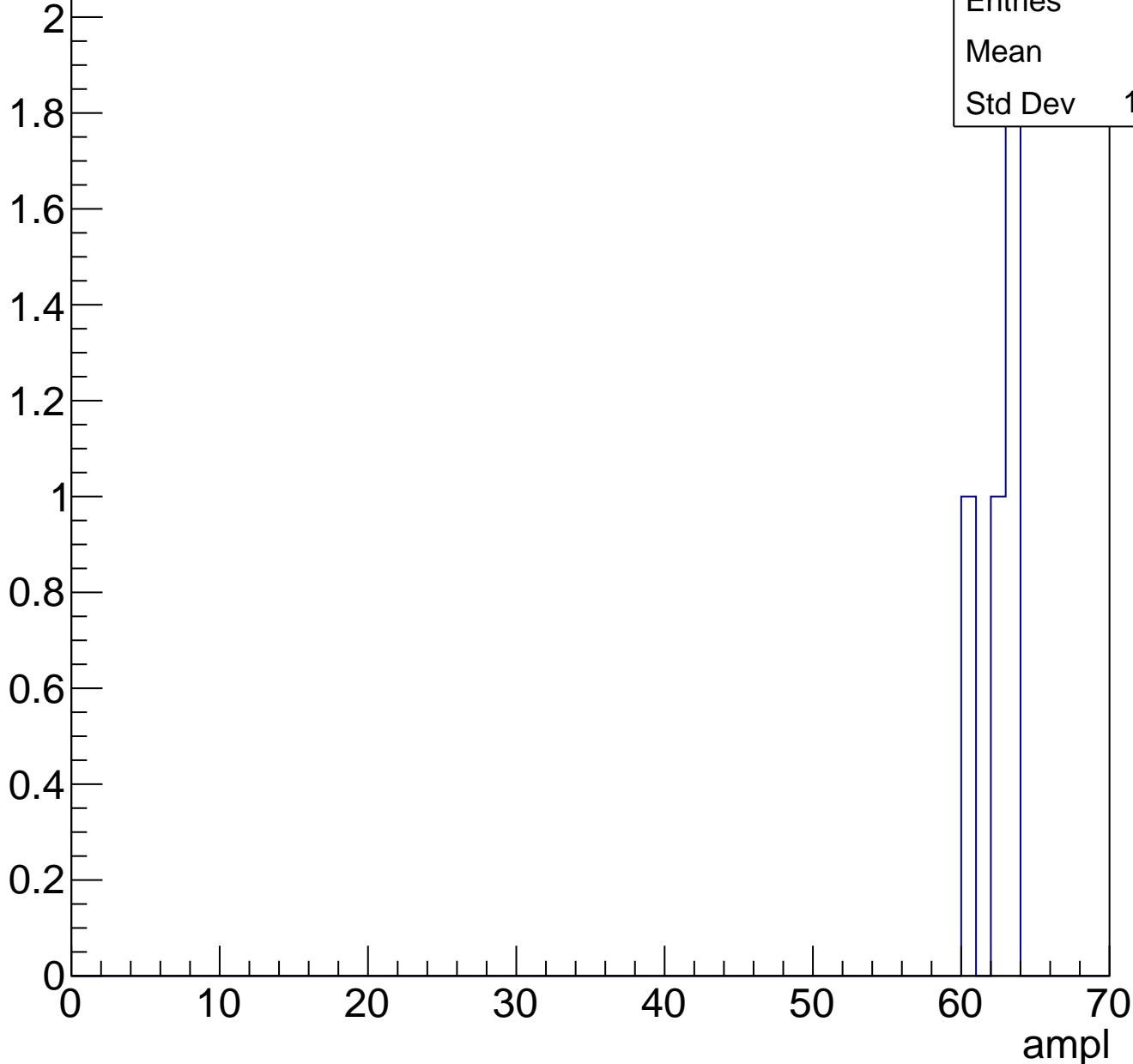
Entries	42
Mean	58.33
Std Dev	9.521



# B0L001S, U5-ch64, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch64, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch65, adc0

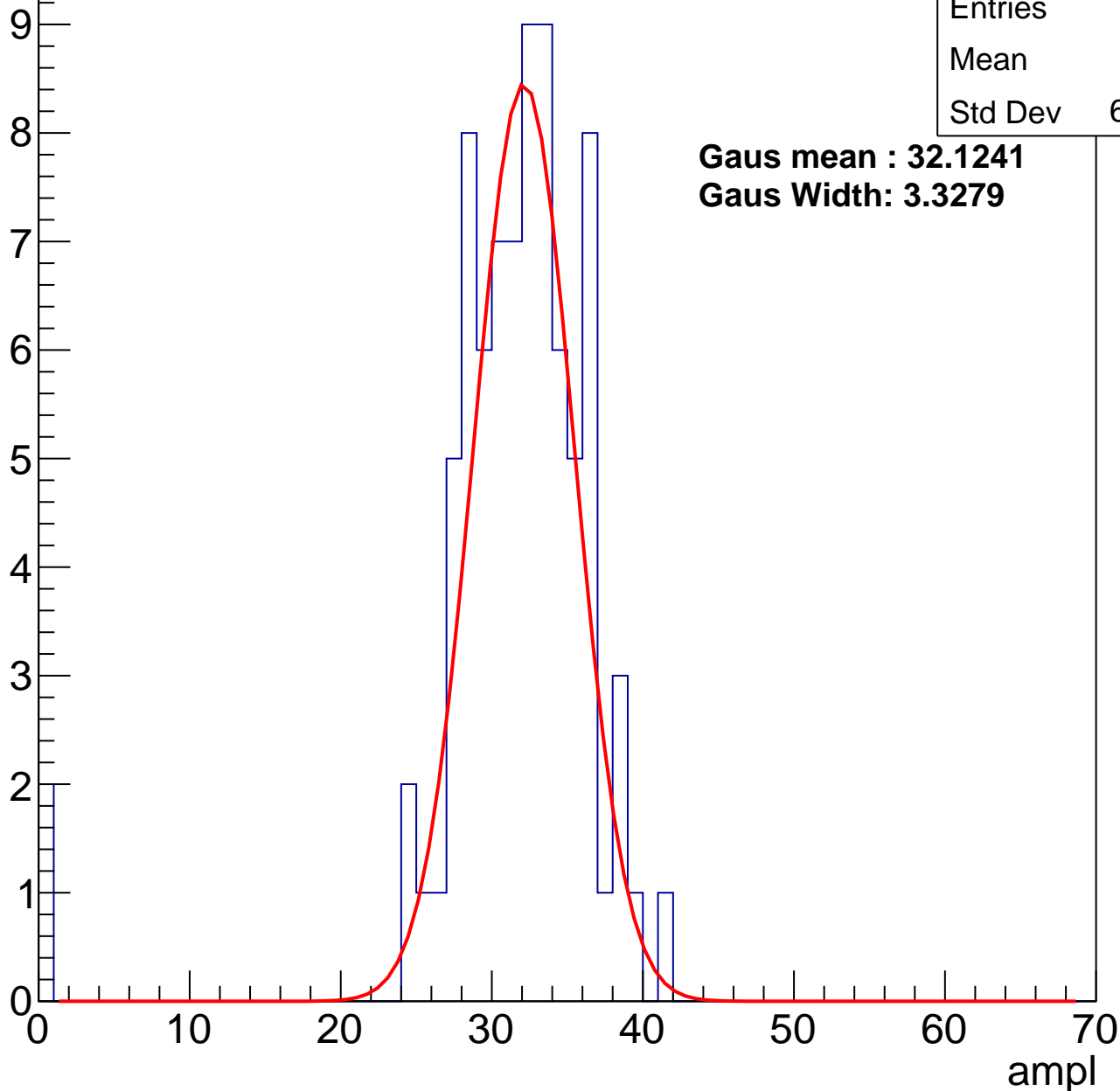
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	82
Mean	31
Std Dev	6.038

**Gaus mean : 32.1241**

**Gaus Width: 3.3279**



# B0L001S, U5-ch65, adc1

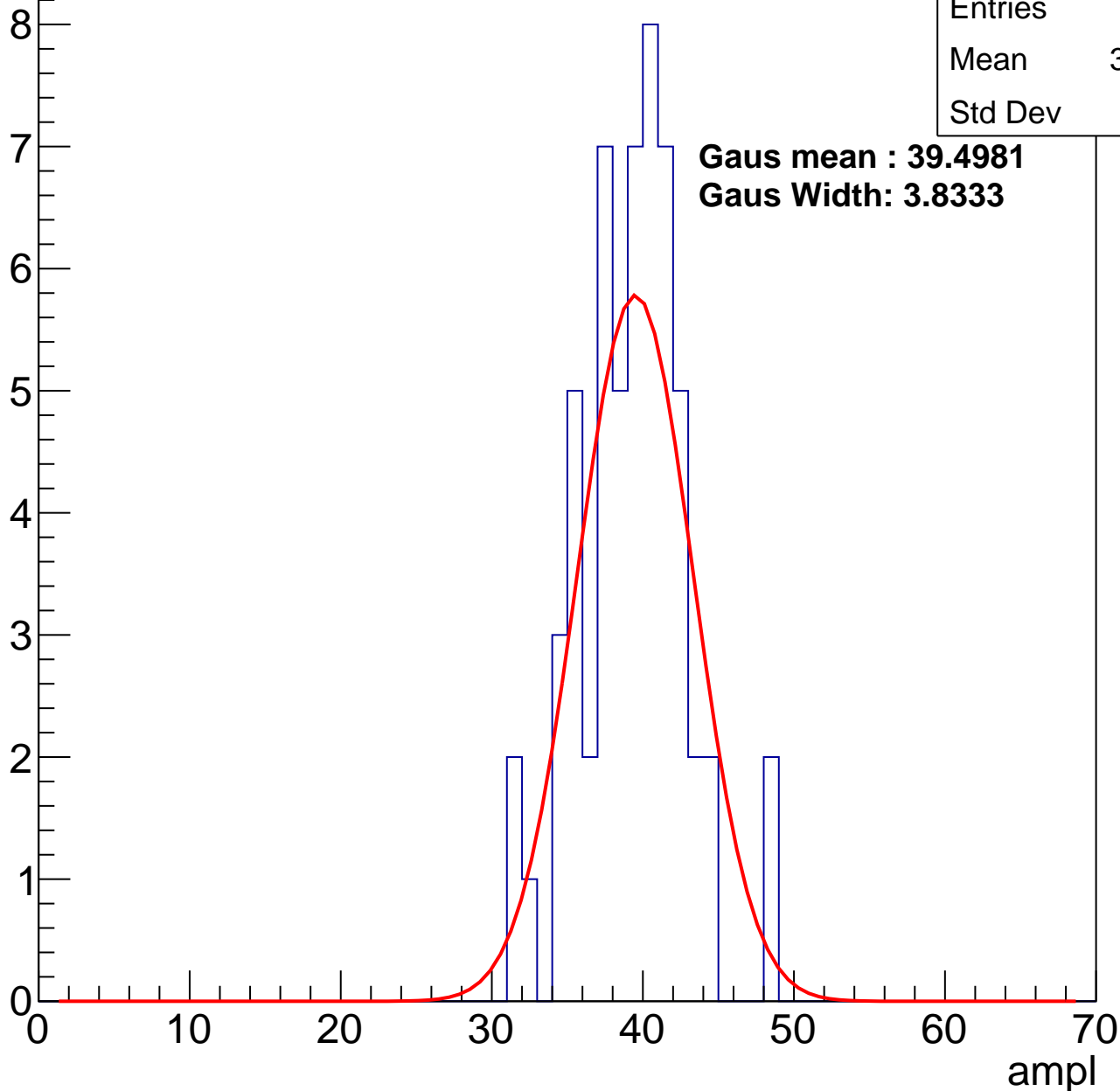
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	38.83
Std Dev	3.49

**Gaus mean : 39.4981**

**Gaus Width: 3.8333**



# B0L001S, U5-ch65, adc2

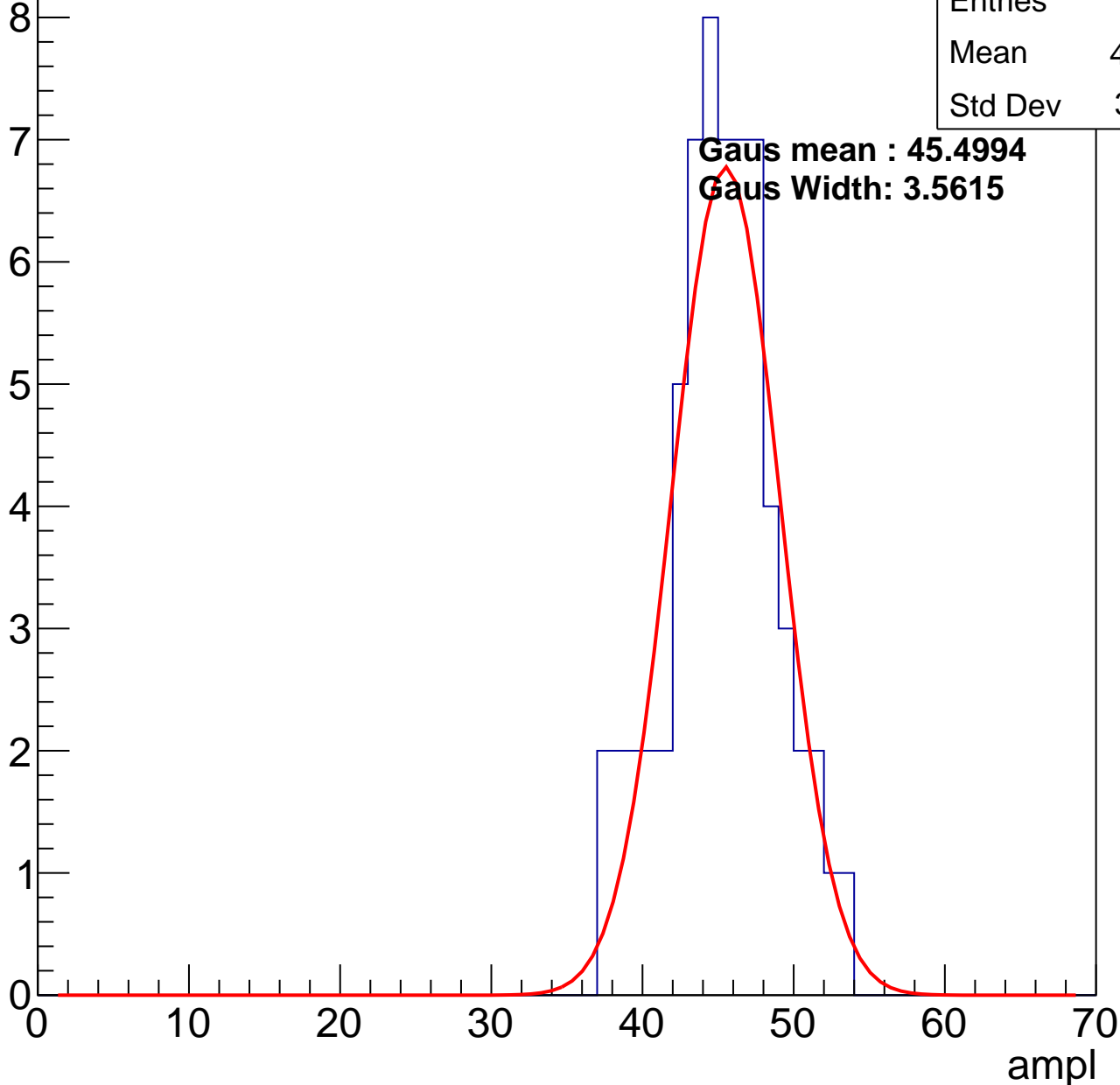
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	44.77
Std Dev	3.561

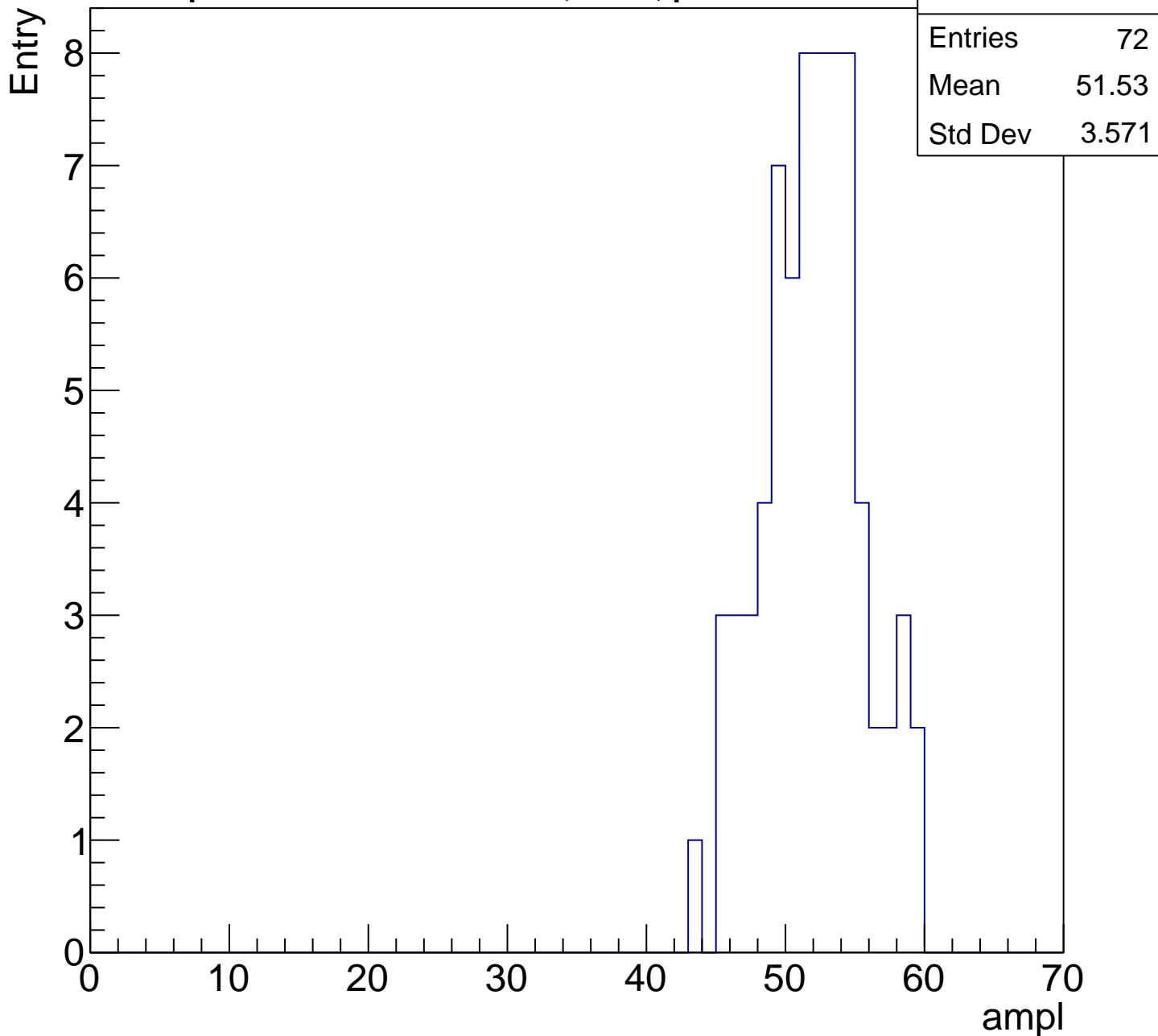
Gaus mean : 45.4994

Gaus Width: 3.5615



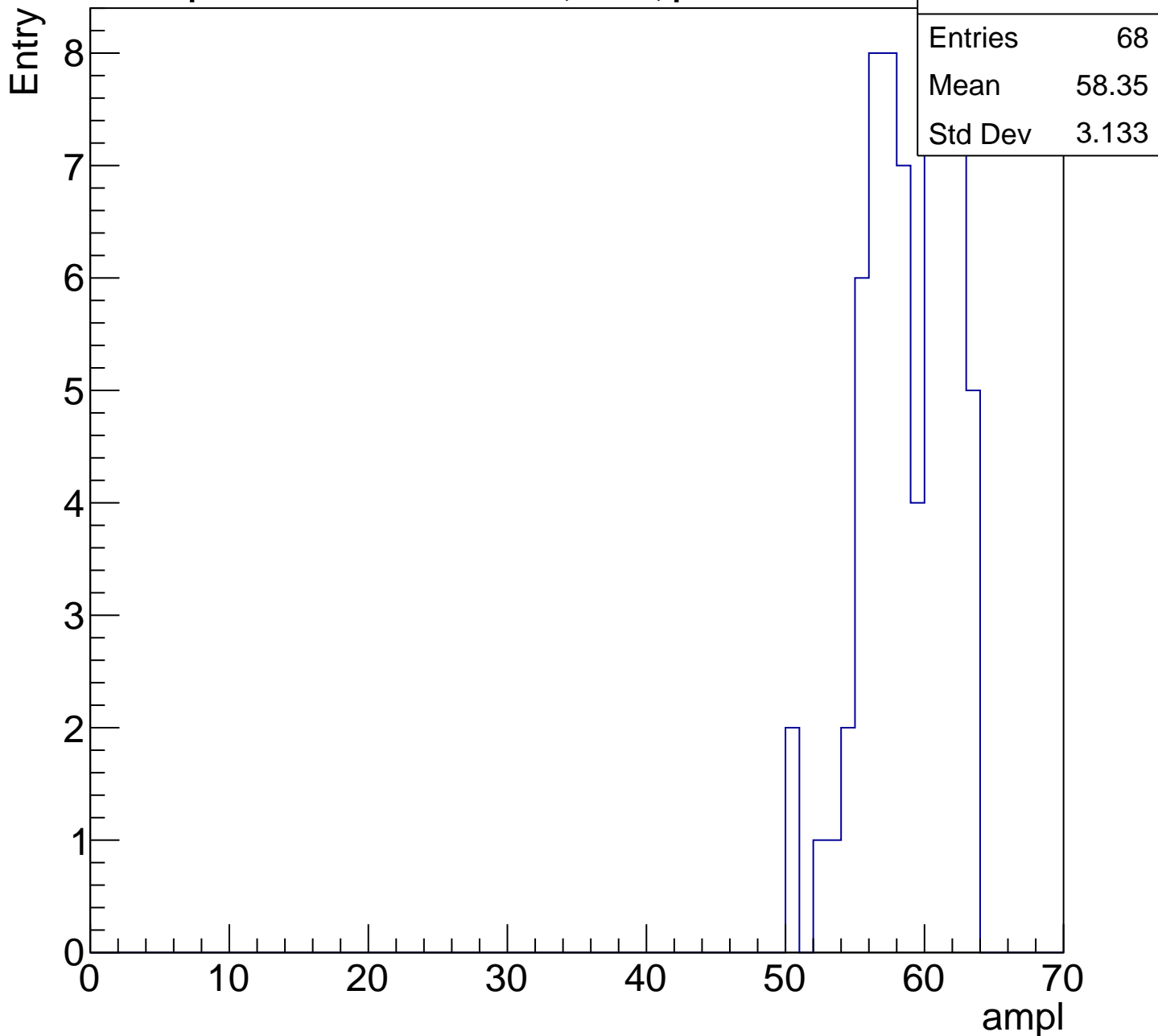
# B0L001S, U5-ch65, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U5-ch65, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

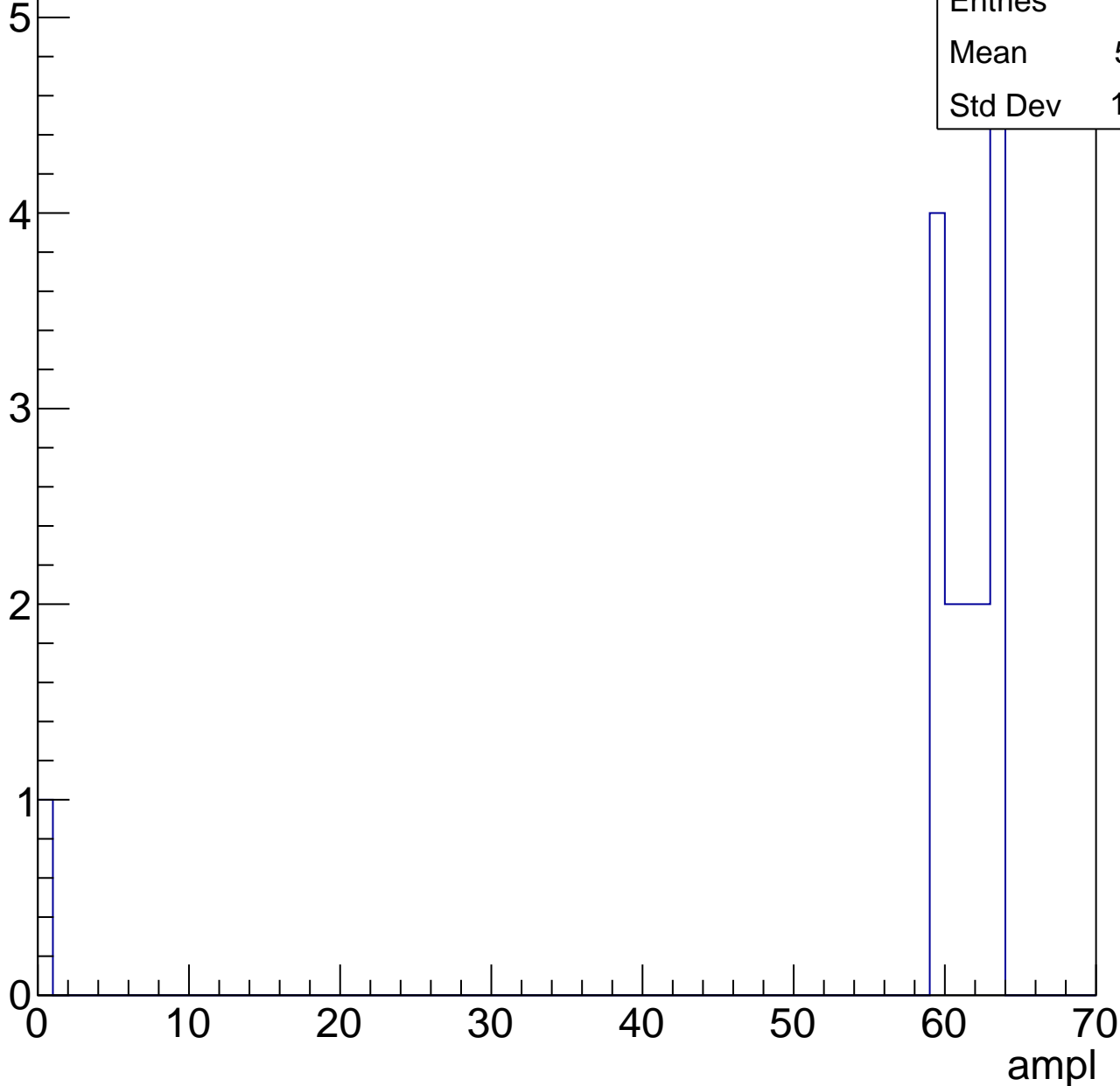


# B0L001S, U5-ch65, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	16
Mean	57.31
Std Dev	14.88



# B0L001S, U5-ch65, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U5-ch65, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L001S, U5-ch66, adc0

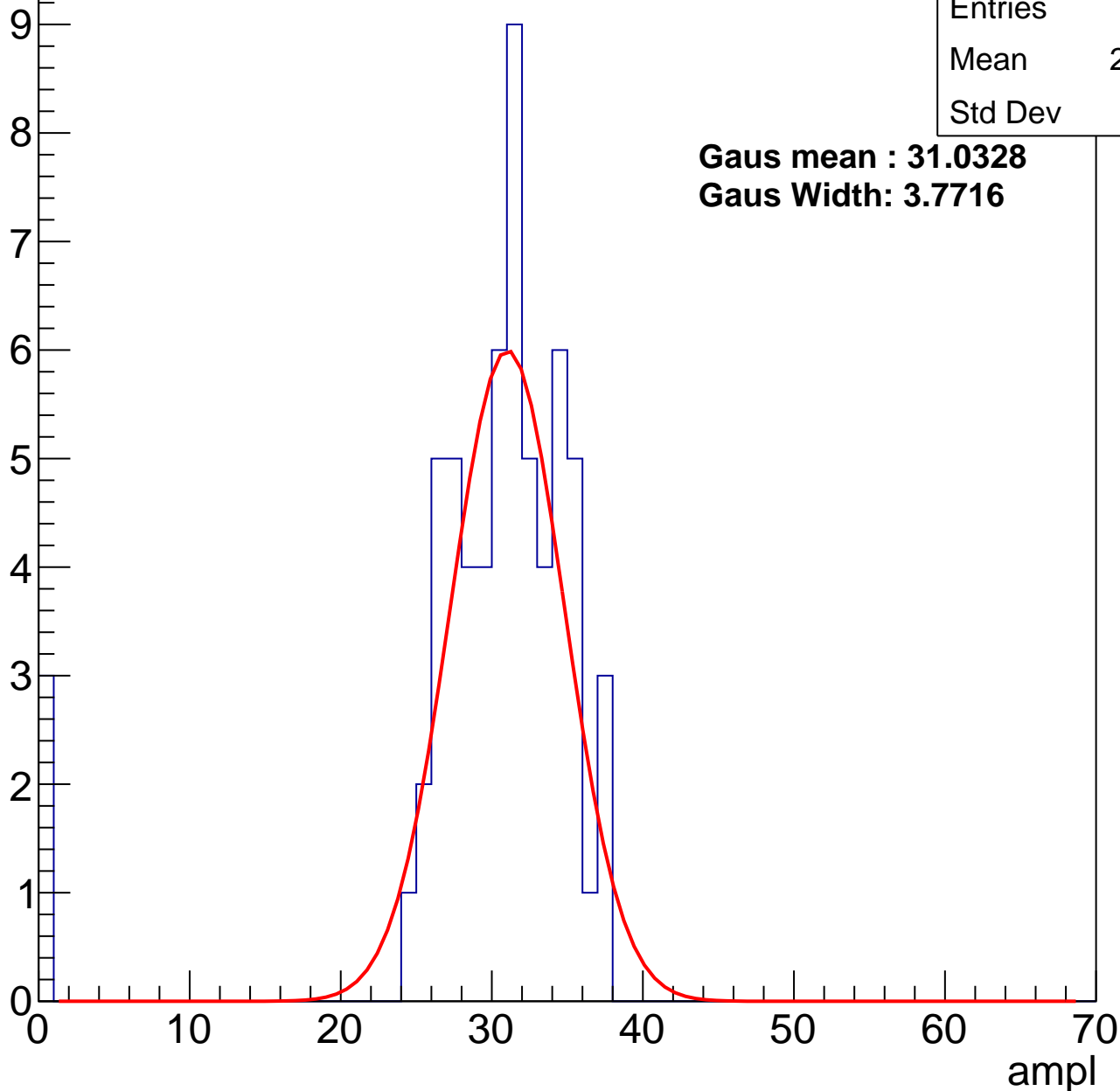
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	29.27
Std Dev	7.31

**Gaus mean : 31.0328**

**Gaus Width: 3.7716**



# B0L001S, U5-ch66, adc1

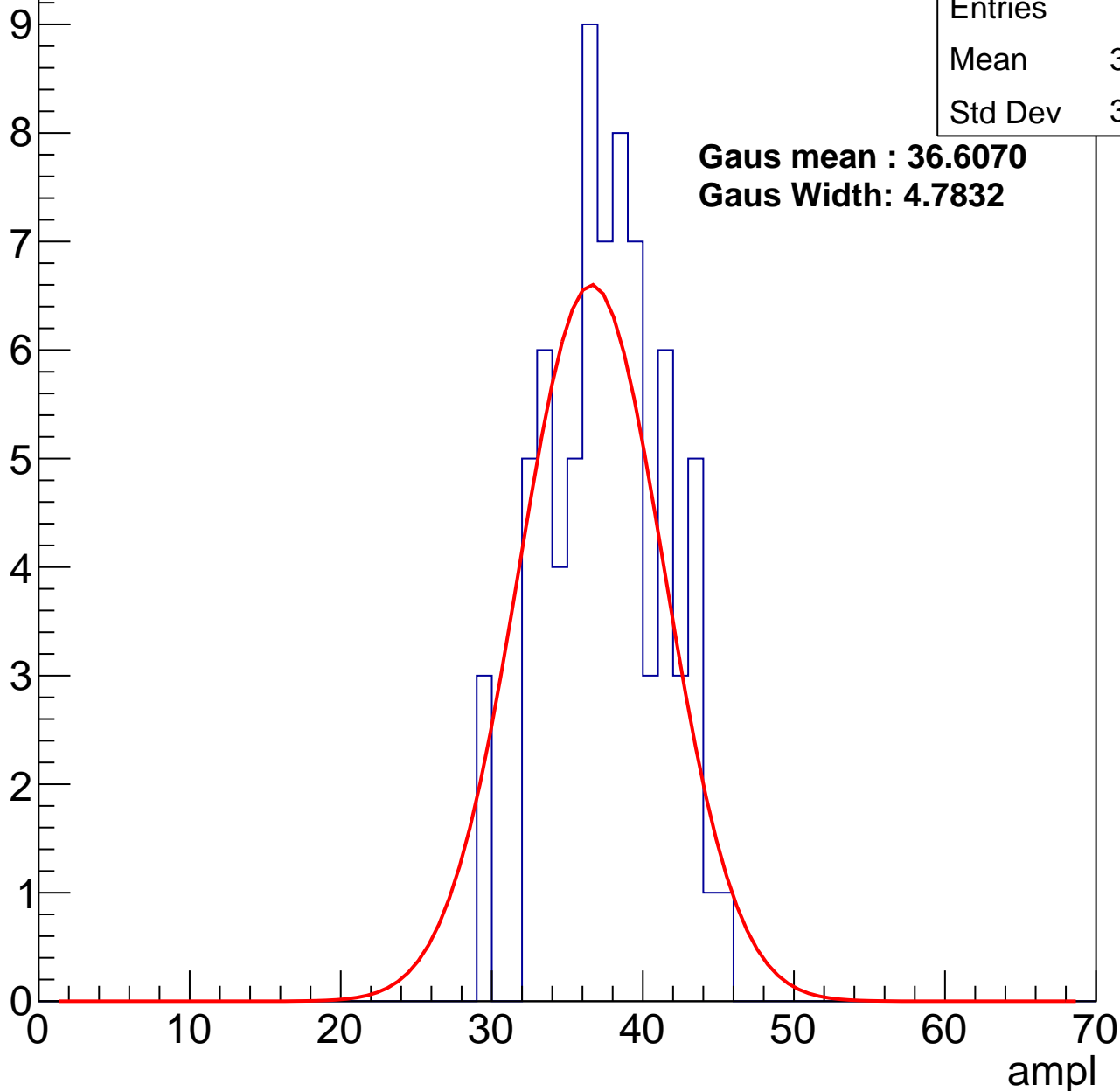
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	37.15
Std Dev	3.707

**Gaus mean : 36.6070**

**Gaus Width: 4.7832**



# B0L001S, U5-ch66, adc2

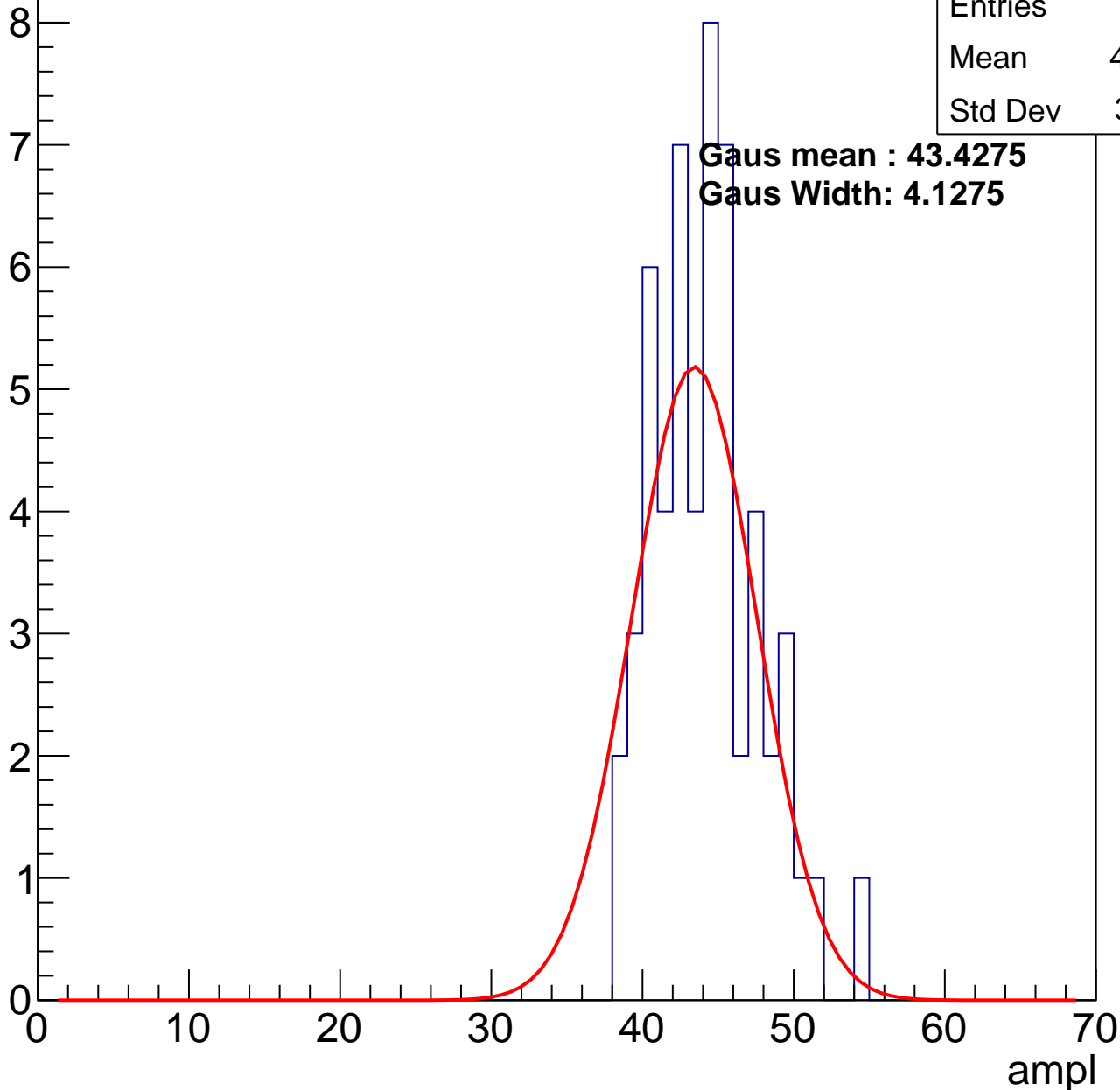
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	43.78
Std Dev	3.441

**Gaus mean : 43.4275**

**Gaus Width: 4.1275**

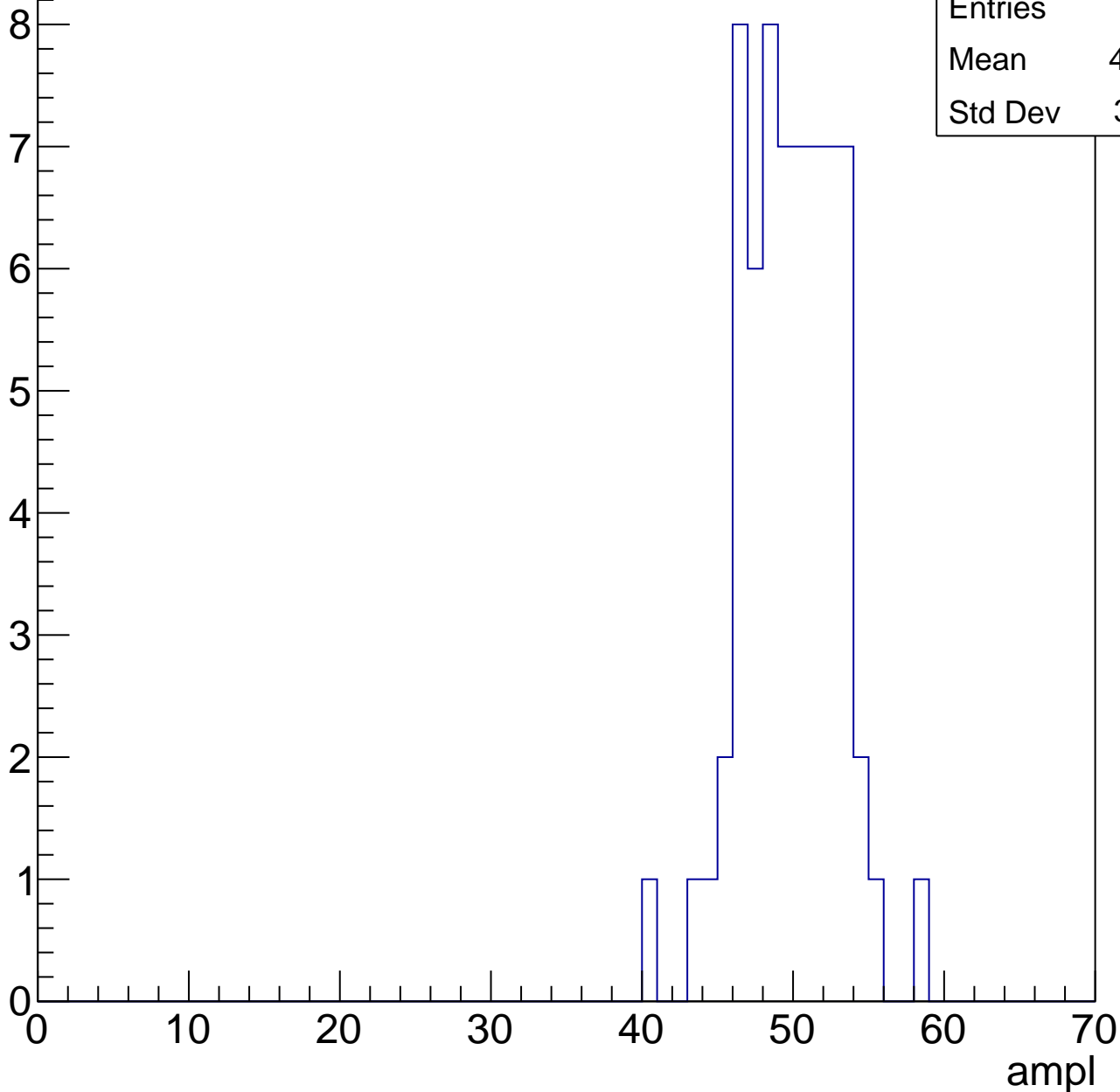


# B0L001S, U5-ch66, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	49.35
Std Dev	3.131

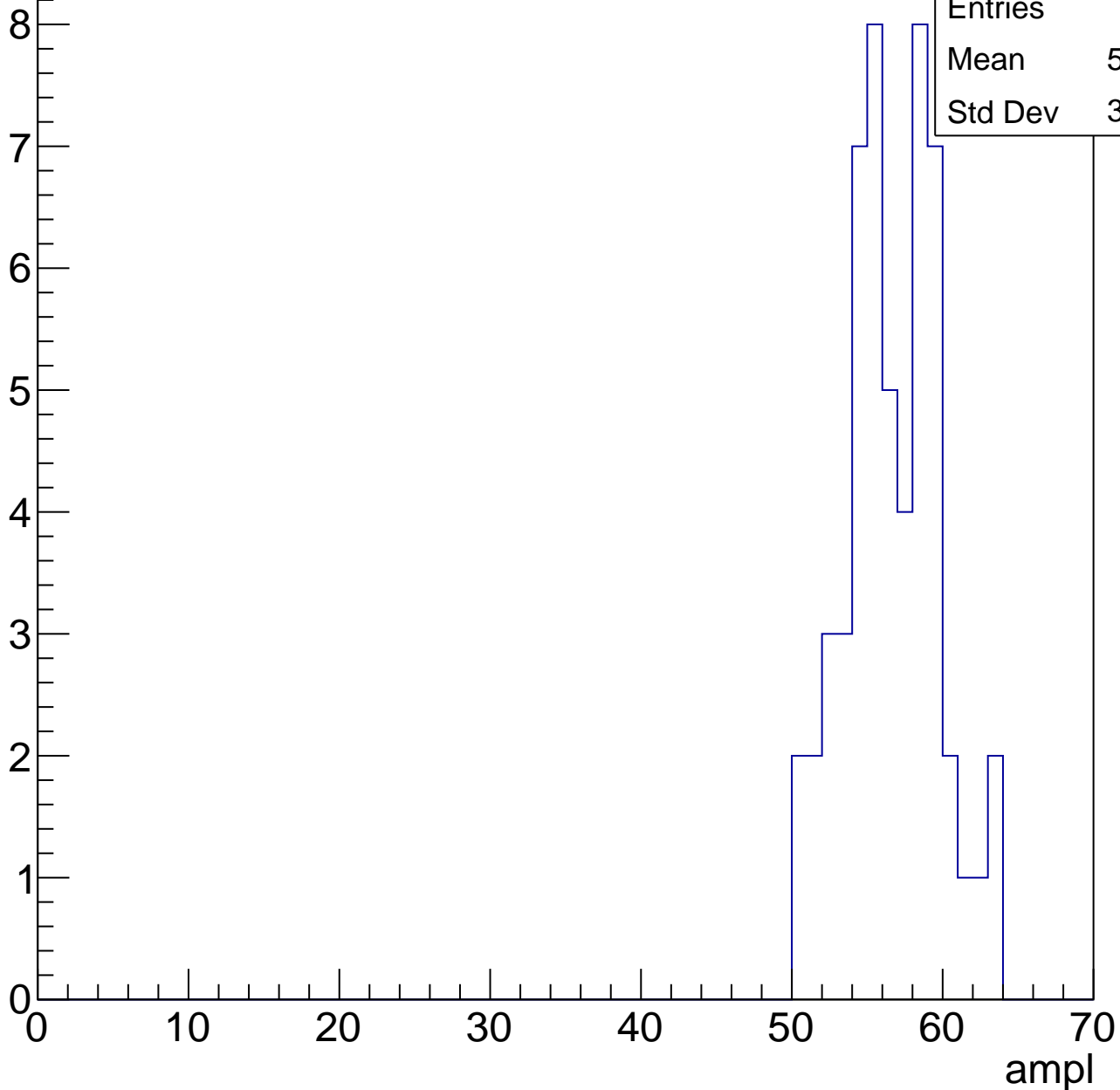


# B0L001S, U5-ch66, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	56.16
Std Dev	3.079



# B0L001S, U5-ch66, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	48
Mean	58.77
Std Dev	8.87

ampl

0 10 20 30 40 50 60 70

0

1

2

3

4

5

6

7

8

9

# B0L001S, U5-ch66, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	60.67
Std Dev	3.3

0 10 20 30 40 50 60 70

ampl

1



# B0L001S, U5-ch66, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U5-ch67, adc0

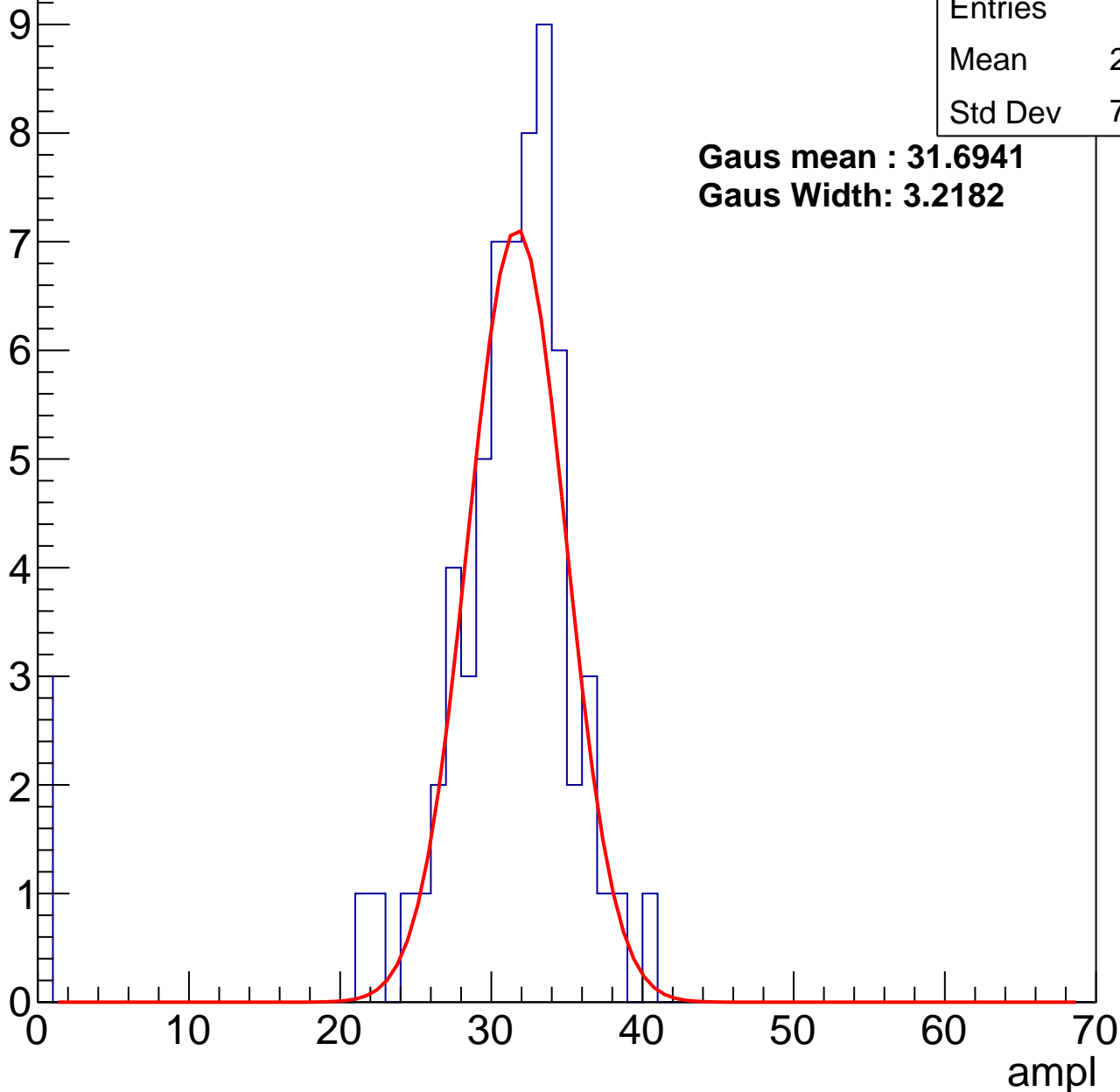
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	29.67
Std Dev	7.355

**Gaus mean : 31.6941**

**Gaus Width: 3.2182**



# B0L001S, U5-ch67, adc1

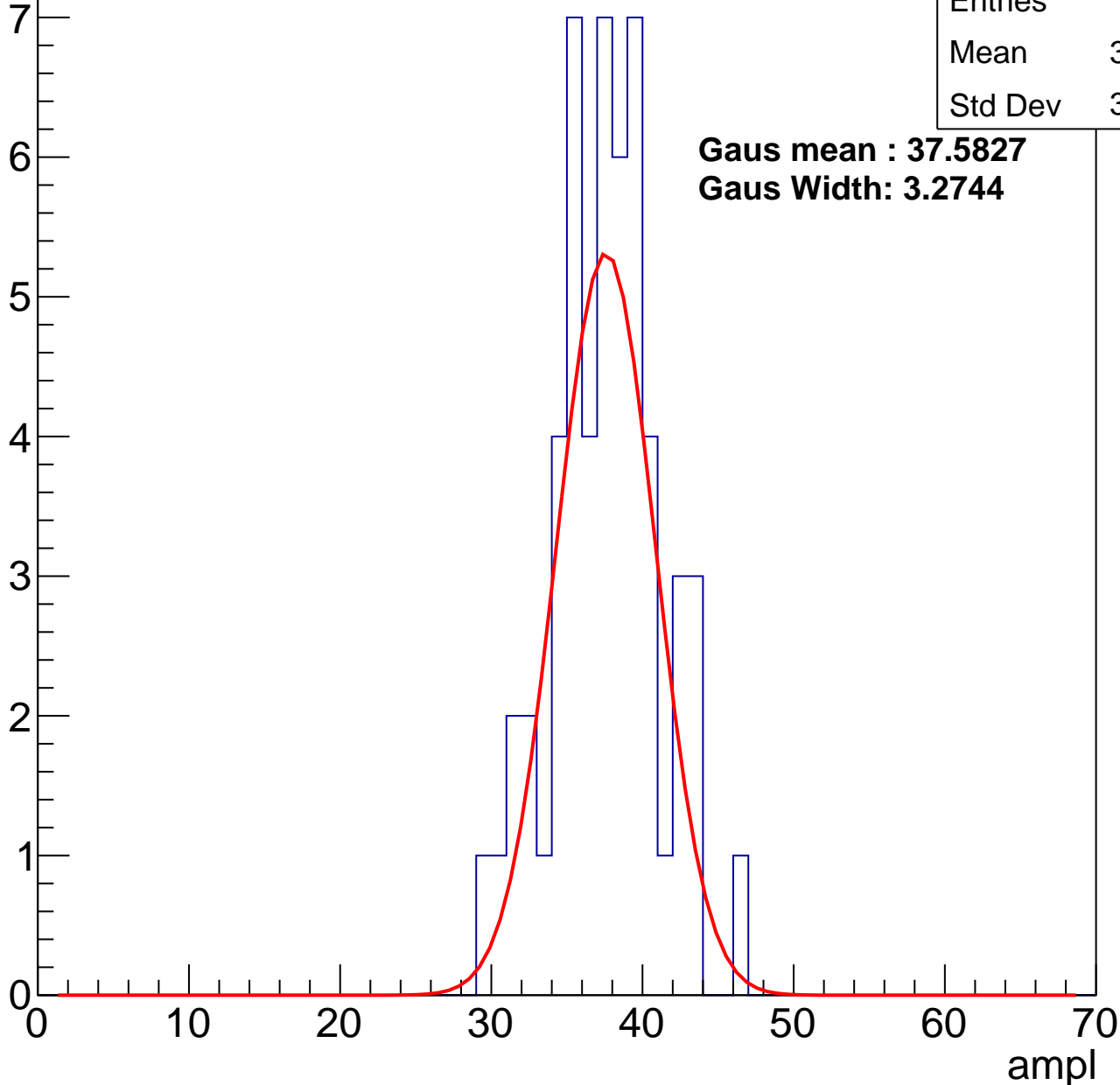
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	37.13
Std Dev	3.517

**Gaus mean : 37.5827**

**Gaus Width: 3.2744**



# B0L001S, U5-ch67, adc2

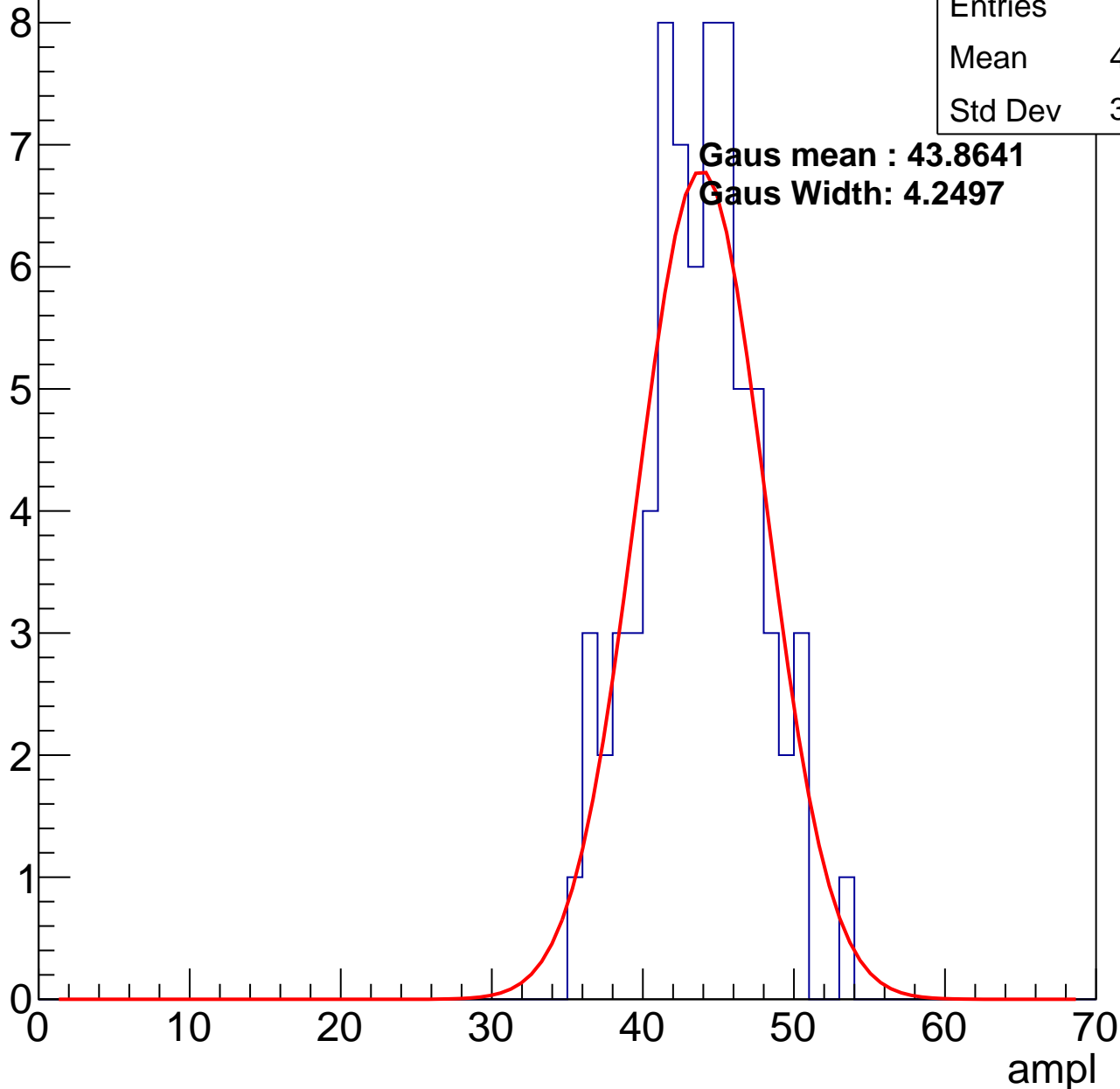
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	43.19
Std Dev	3.796

**Gaus mean : 43.8641**

**Gaus Width: 4.2497**

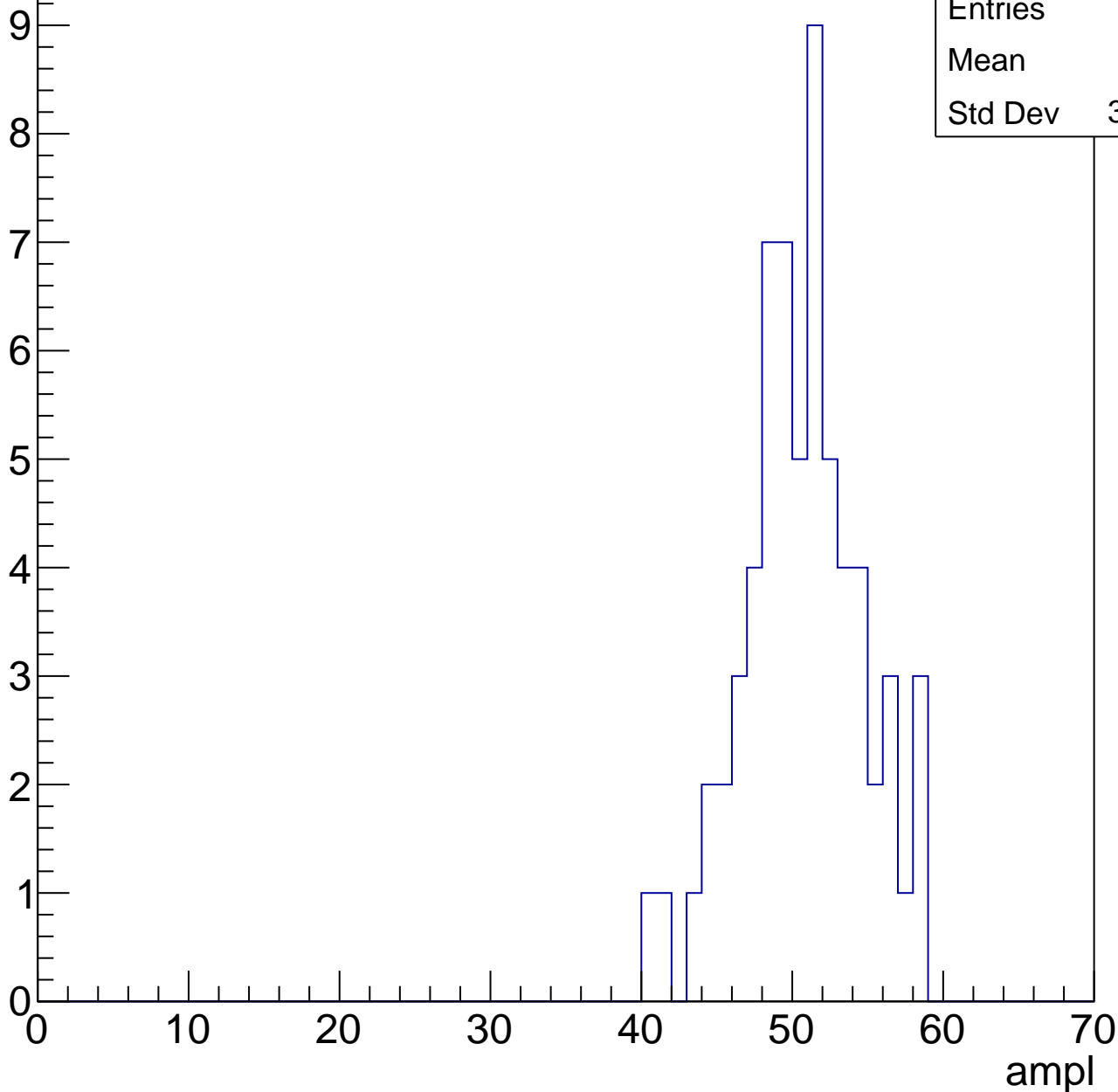


# B0L001S, U5-ch67, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	50.2
Std Dev	3.946

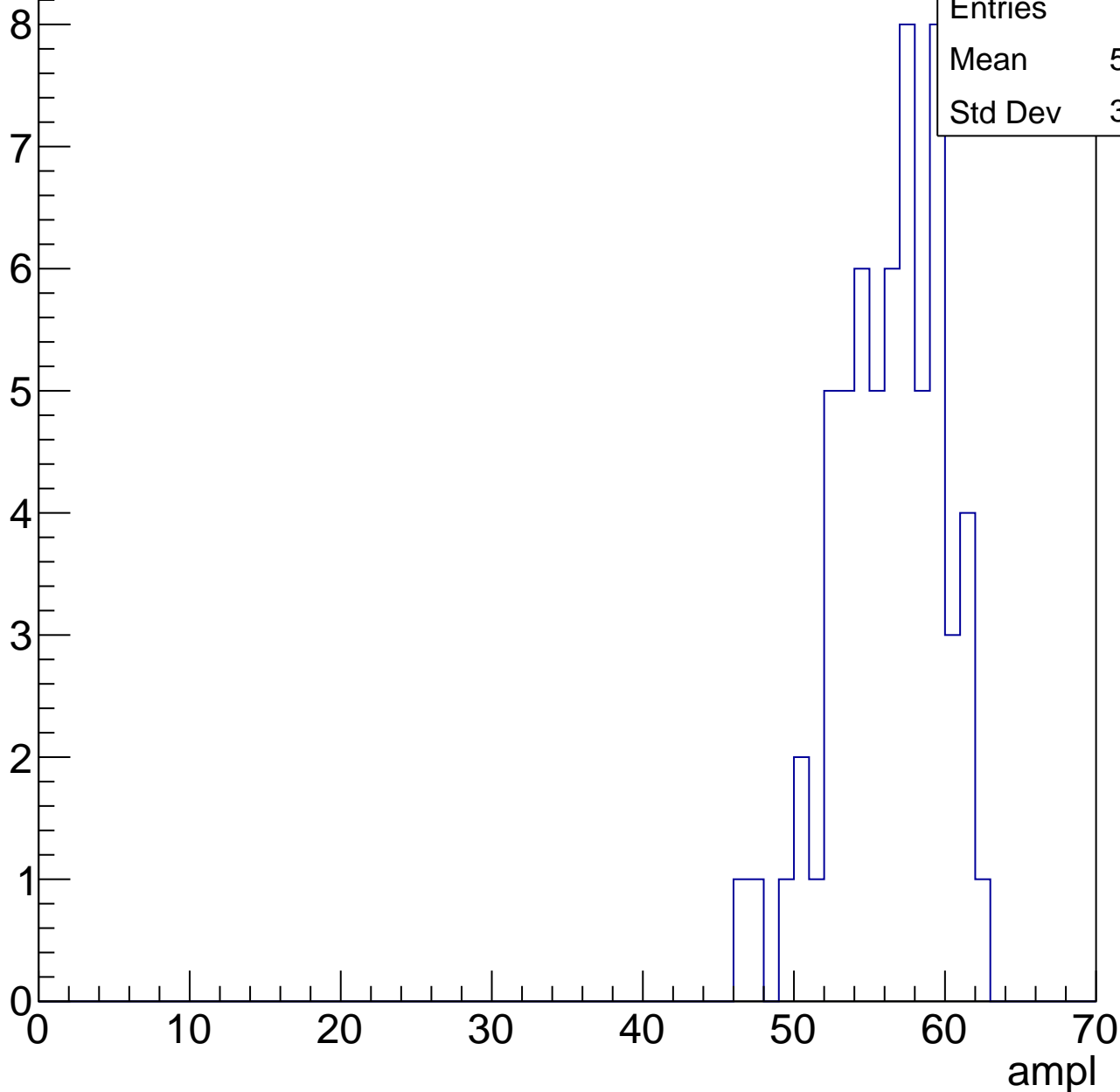


# B0L001S, U5-ch67, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	55.76
Std Dev	3.504

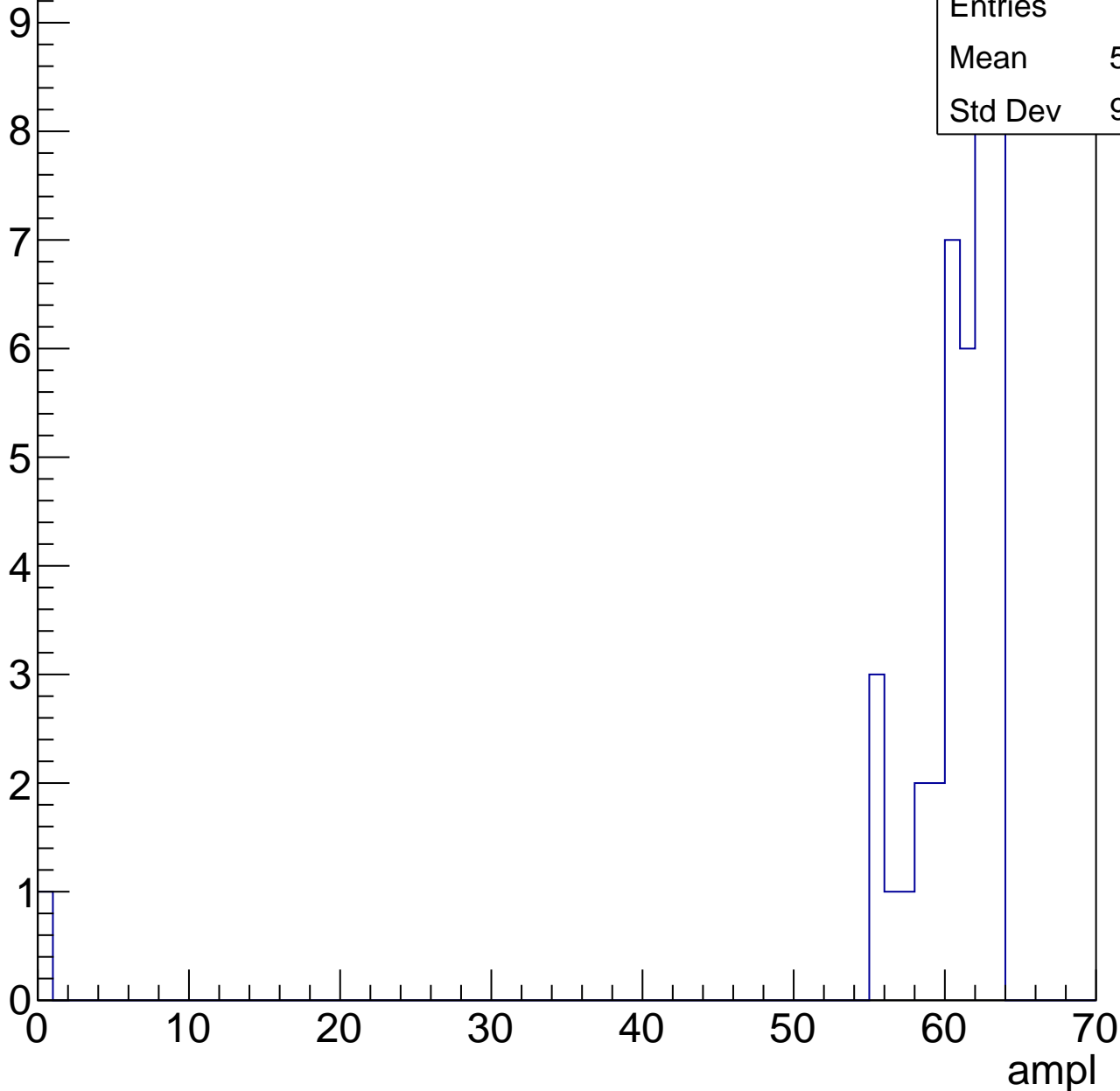


# B0L001S, U5-ch67, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	40
Mean	59.02
Std Dev	9.735



# B0L001S, U5-ch67, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch67, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch68, adc0

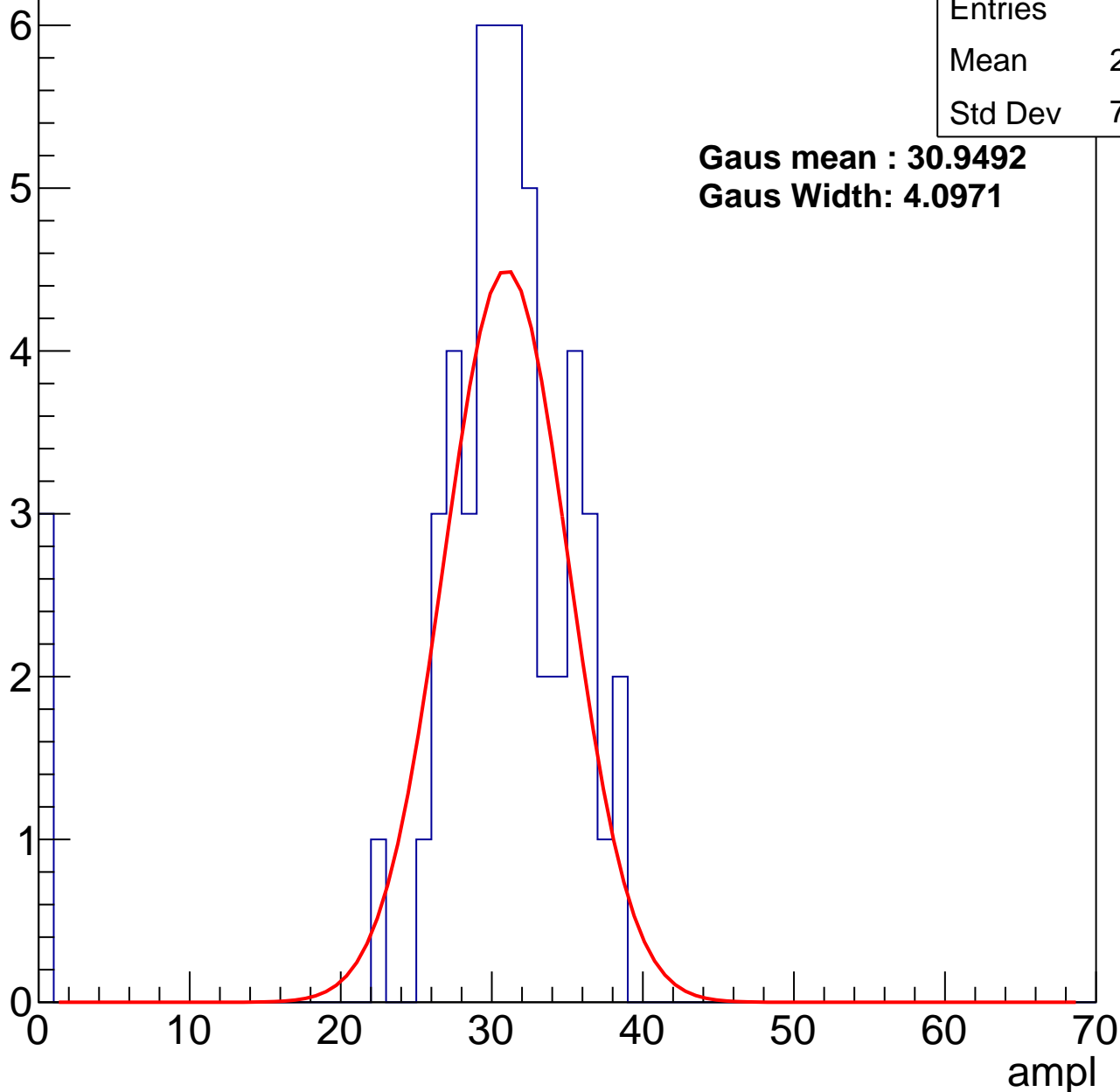
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	29.08
Std Dev	7.976

**Gaus mean : 30.9492**

**Gaus Width: 4.0971**



# B0L001S, U5-ch68, adc1

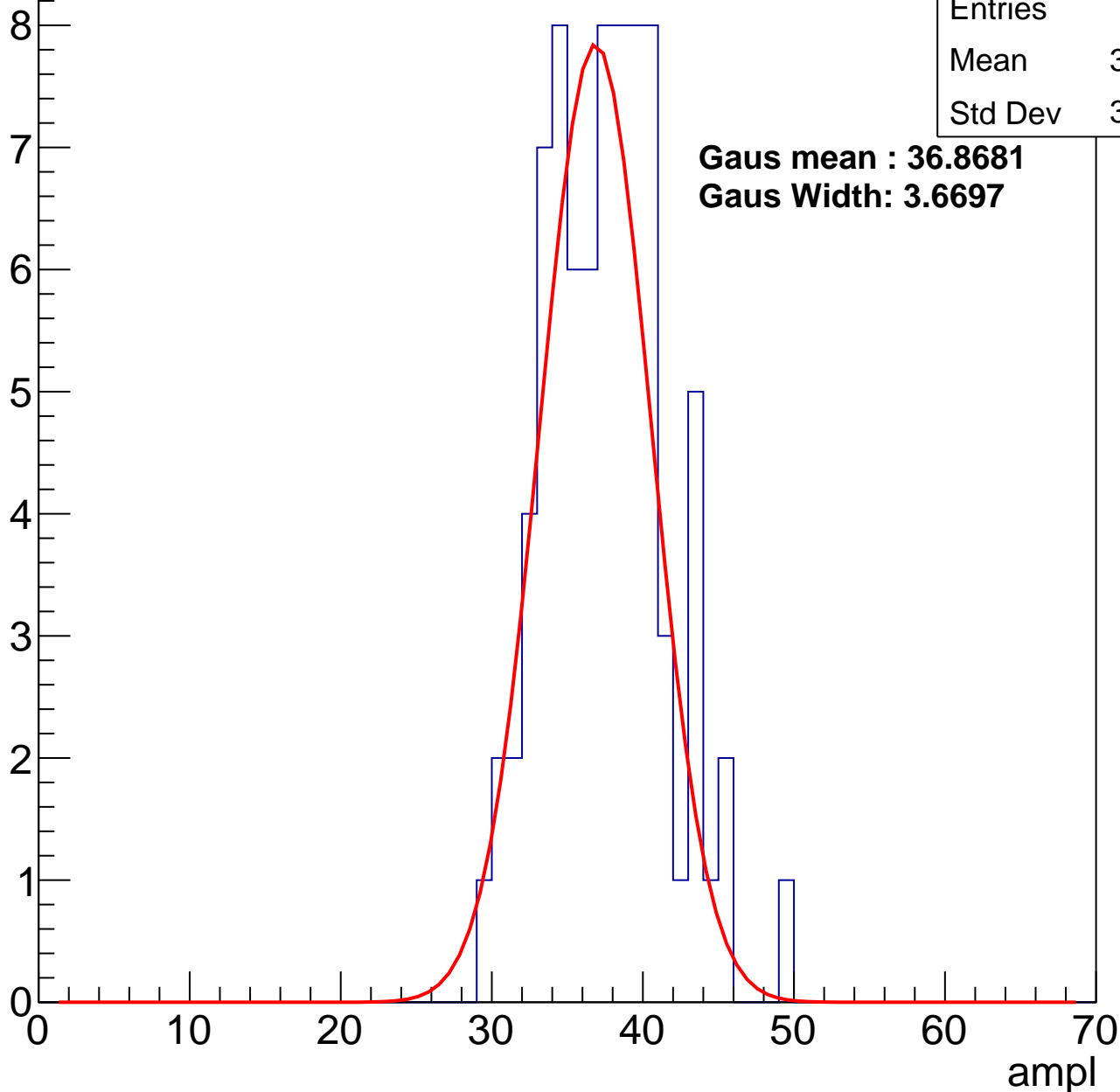
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	81
Mean	37.07
Std Dev	3.902

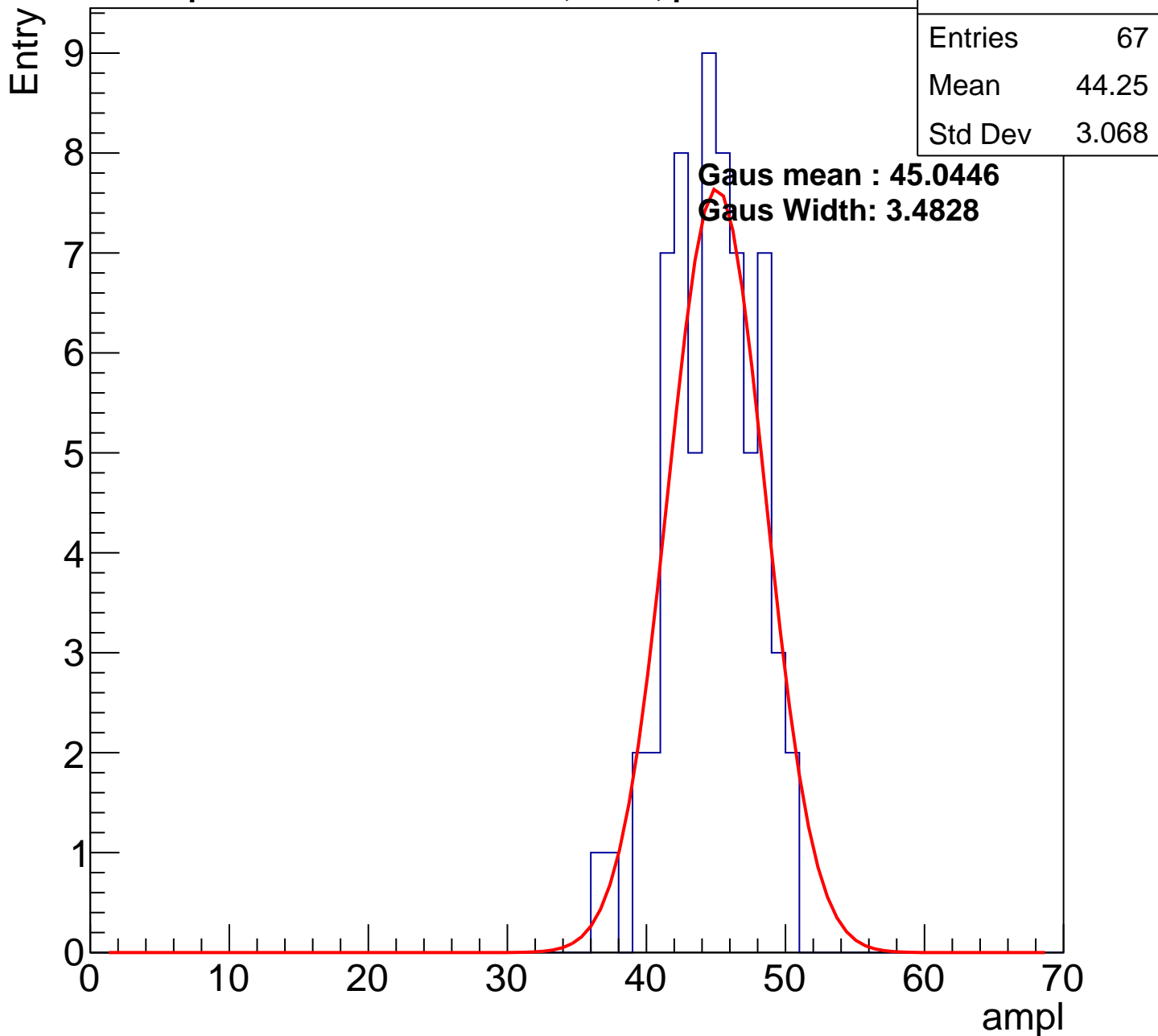
**Gaus mean : 36.8681**

**Gaus Width: 3.6697**



# B0L001S, U5-ch68, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

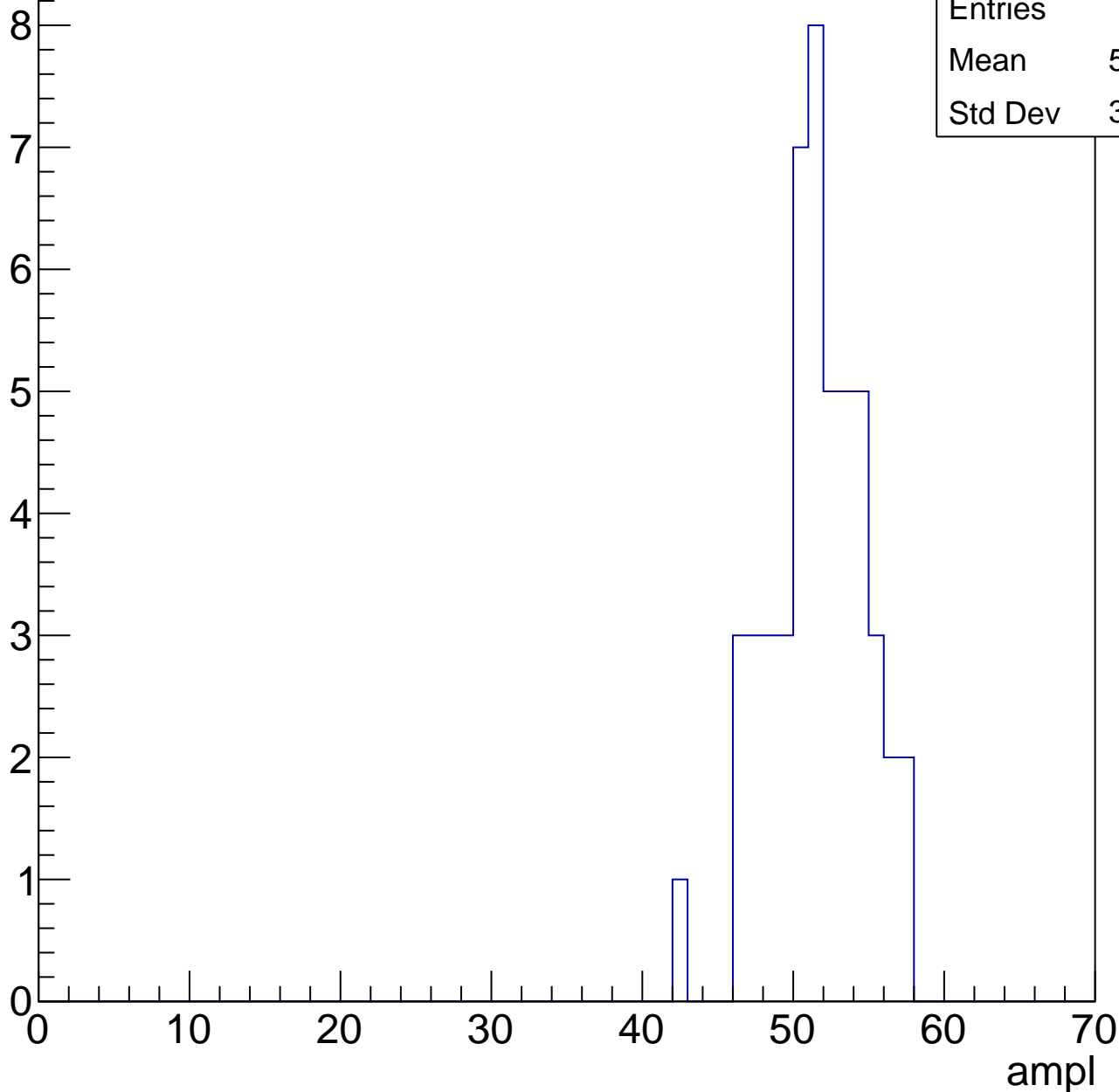


# B0L001S, U5-ch68, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	50
Mean	51.12
Std Dev	3.128

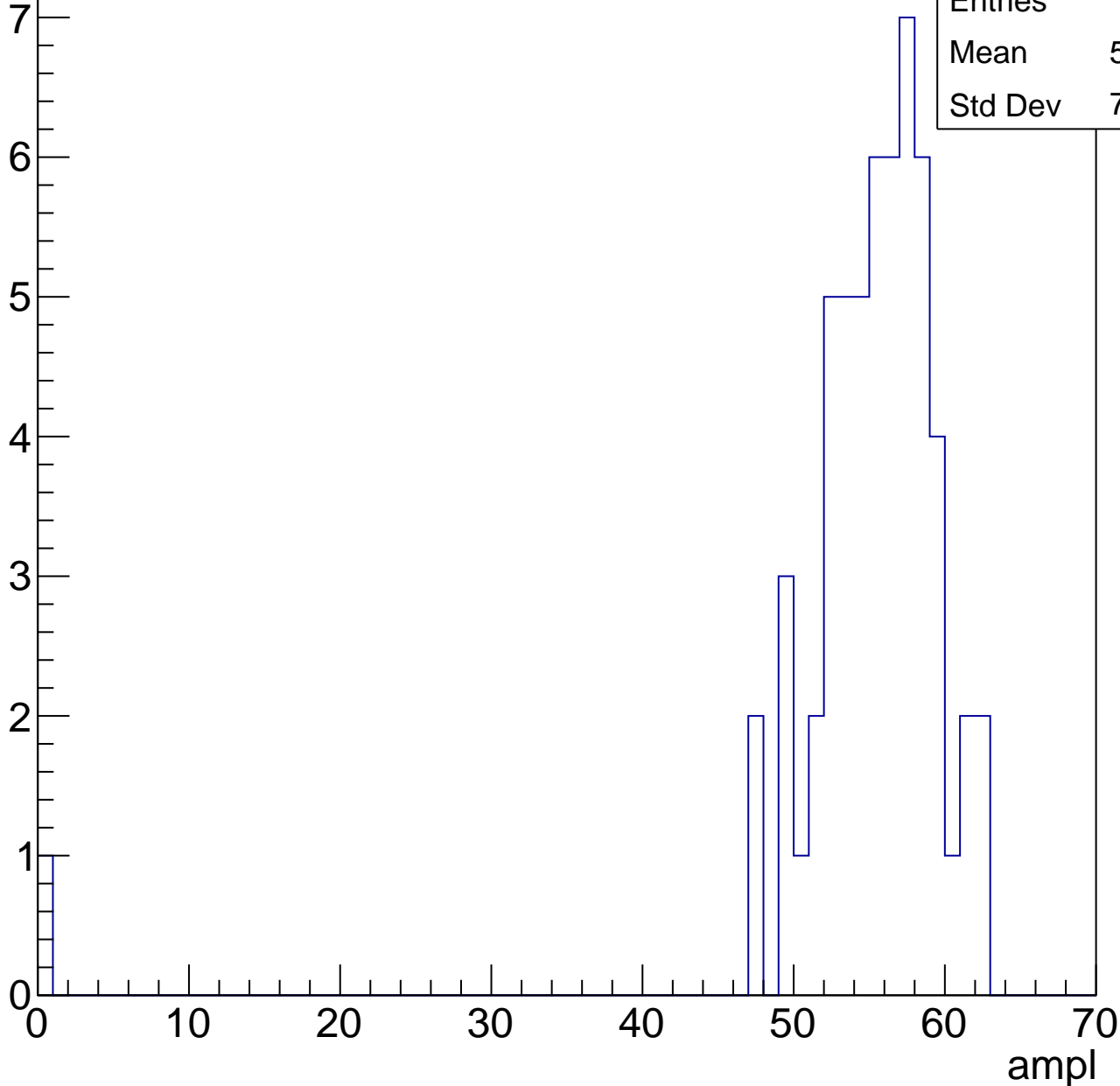


# B0L001S, U5-ch68, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

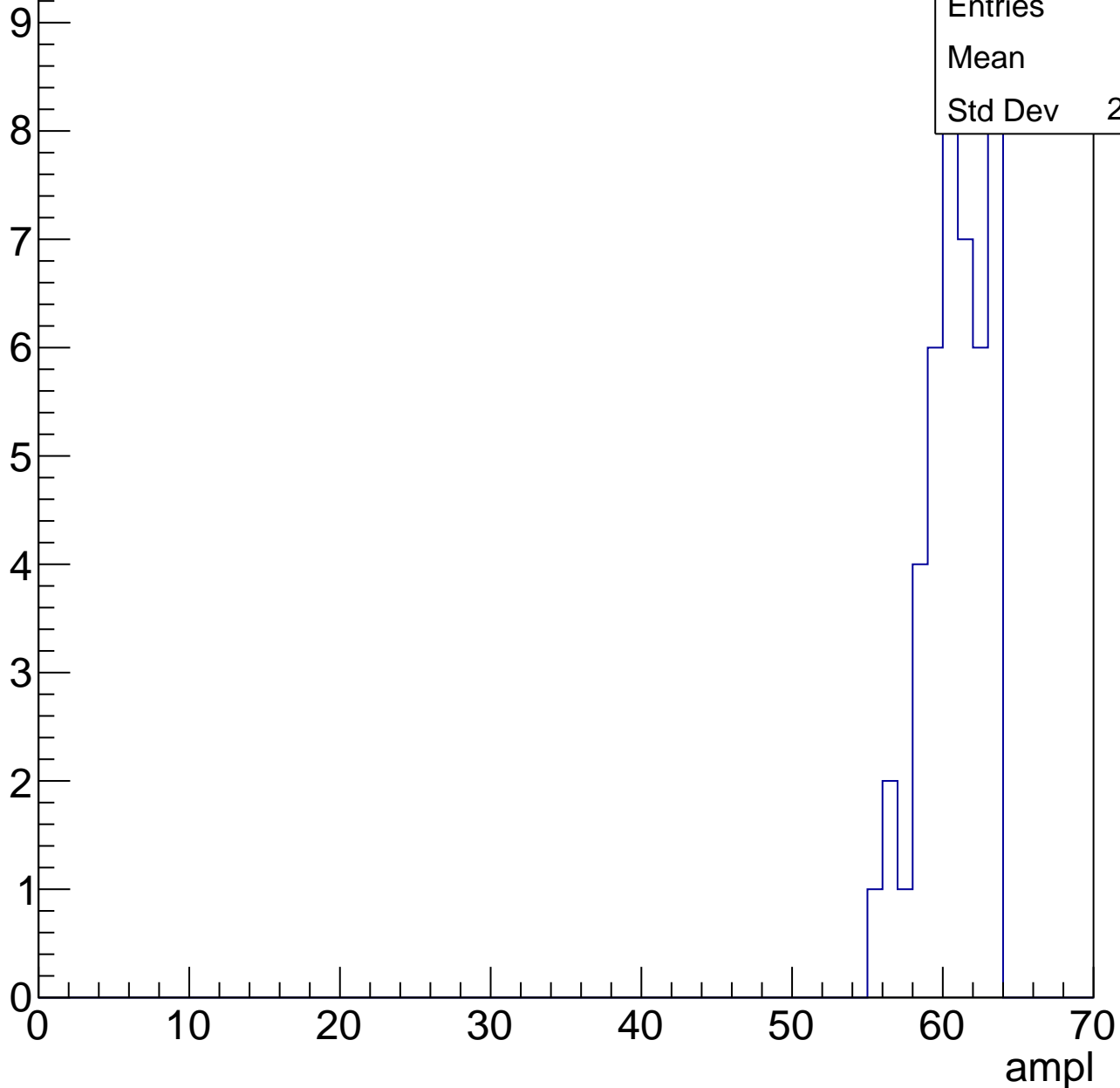
Entries	58
Mean	54.19
Std Dev	7.984



# B0L001S, U5-ch68, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch68, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	62.2
Std Dev	0.7483

ampl

0 10 20 30 40 50 60 70



# B0L001S, U5-ch68, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch69, adc0

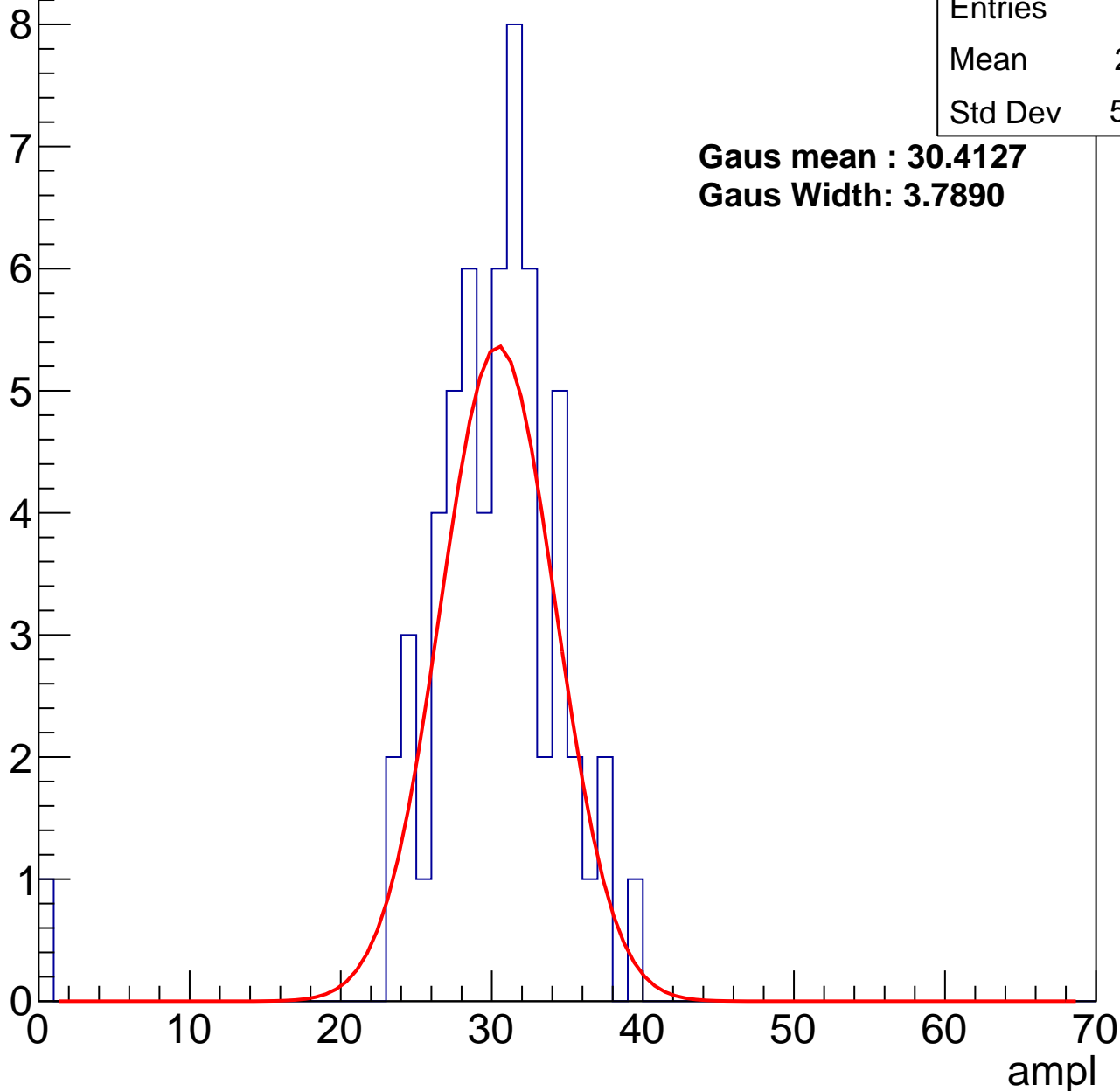
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	29.51
Std Dev	5.286

**Gaus mean : 30.4127**

**Gaus Width: 3.7890**



# B0L001S, U5-ch69, adc1

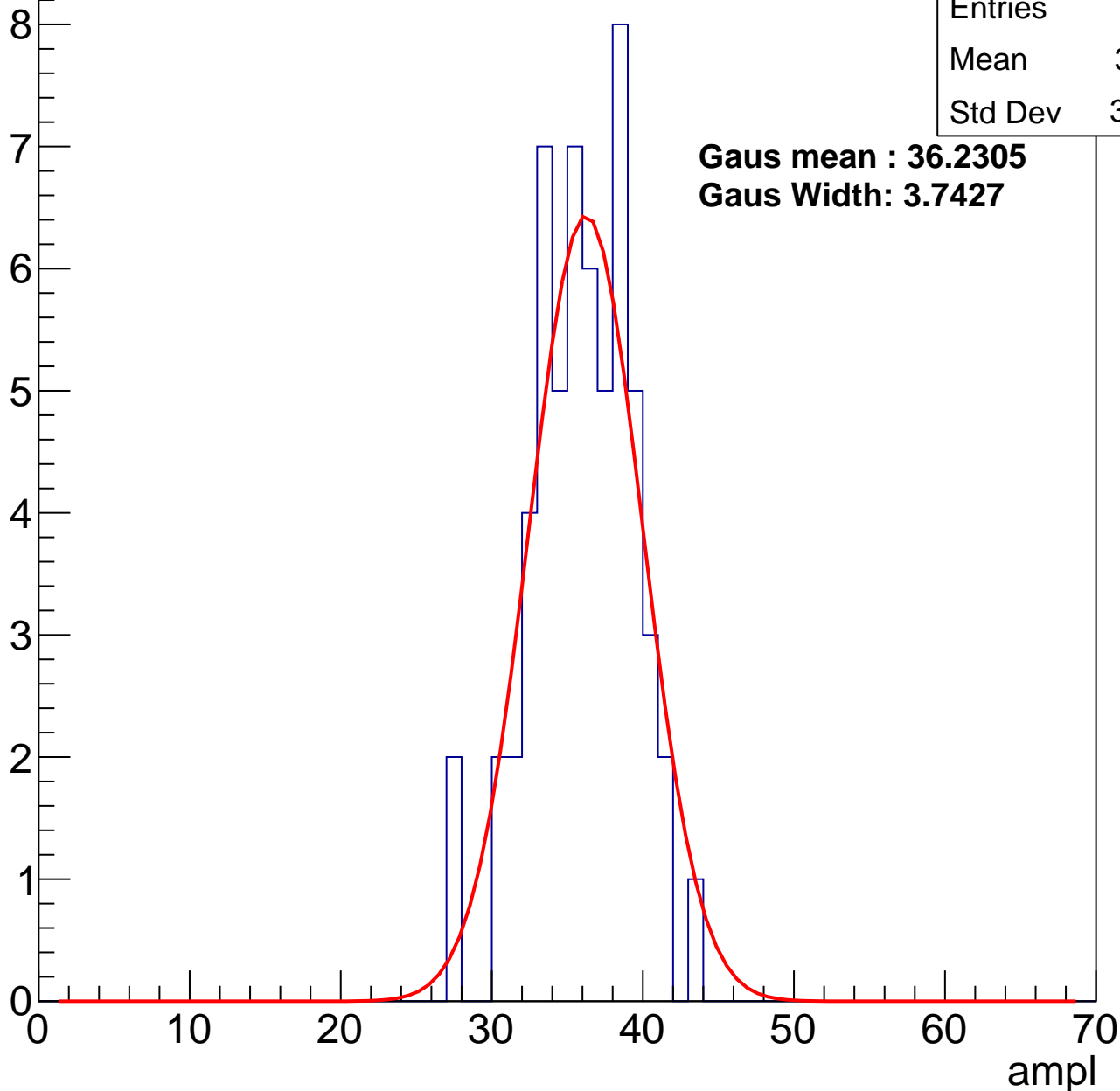
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	35.51
Std Dev	3.326

**Gaus mean : 36.2305**

**Gaus Width: 3.7427**



# B0L001S, U5-ch69, adc2

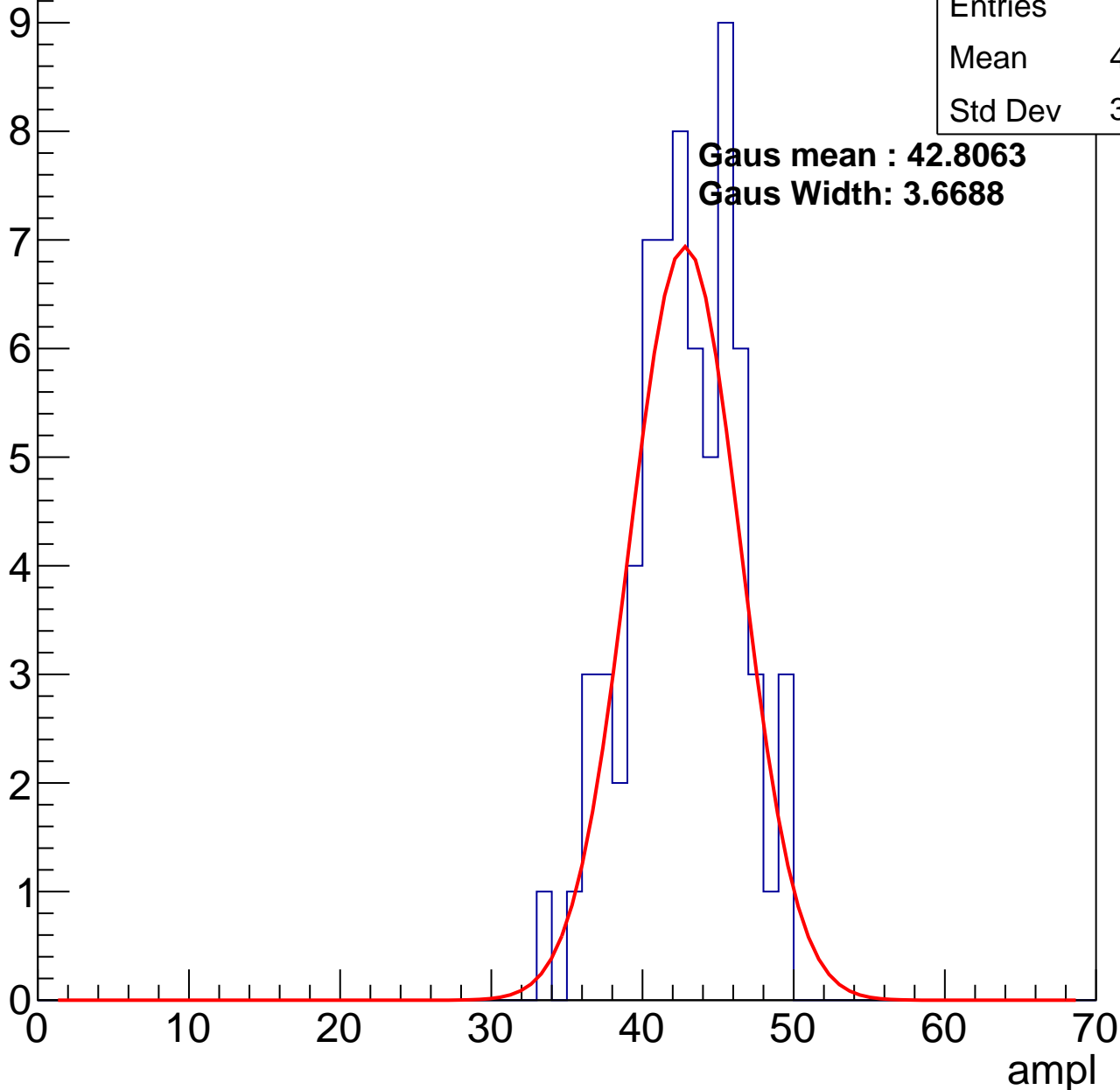
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	42.28
Std Dev	3.554

**Gaus mean : 42.8063**

**Gaus Width: 3.6688**

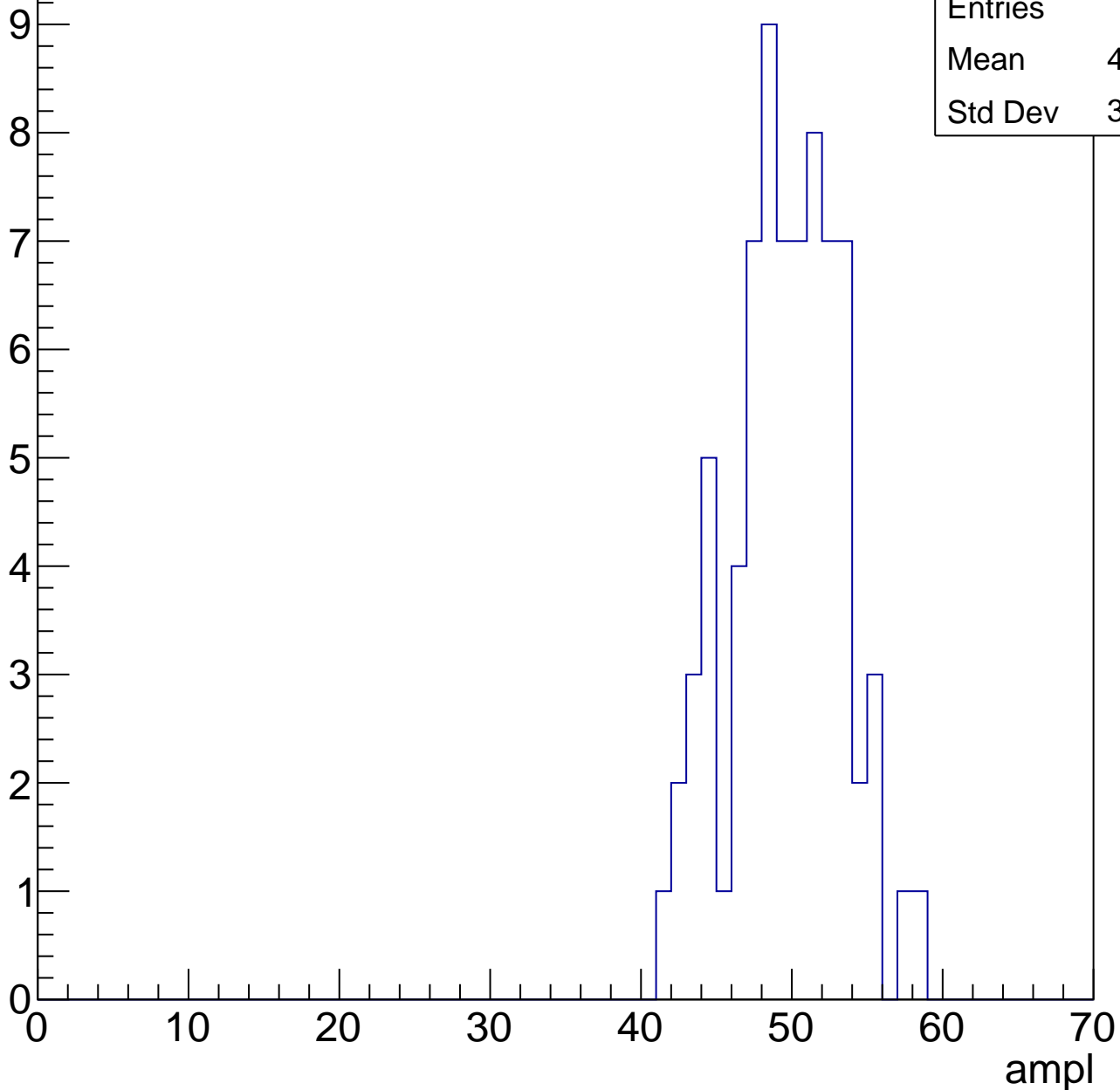


# B0L001S, U5-ch69, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	75
Mean	49.17
Std Dev	3.649

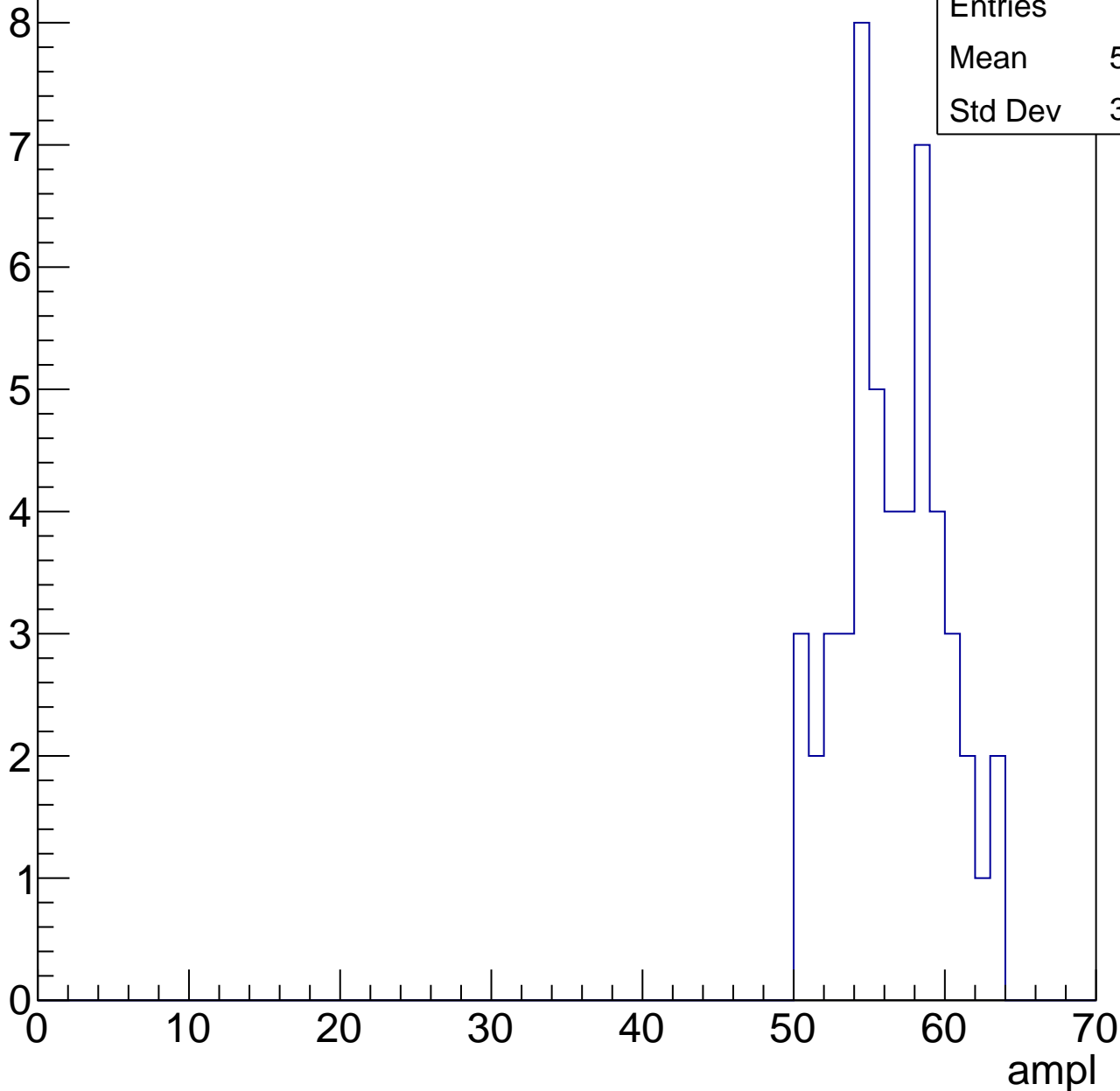


# B0L001S, U5-ch69, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	51
Mean	56.04
Std Dev	3.343

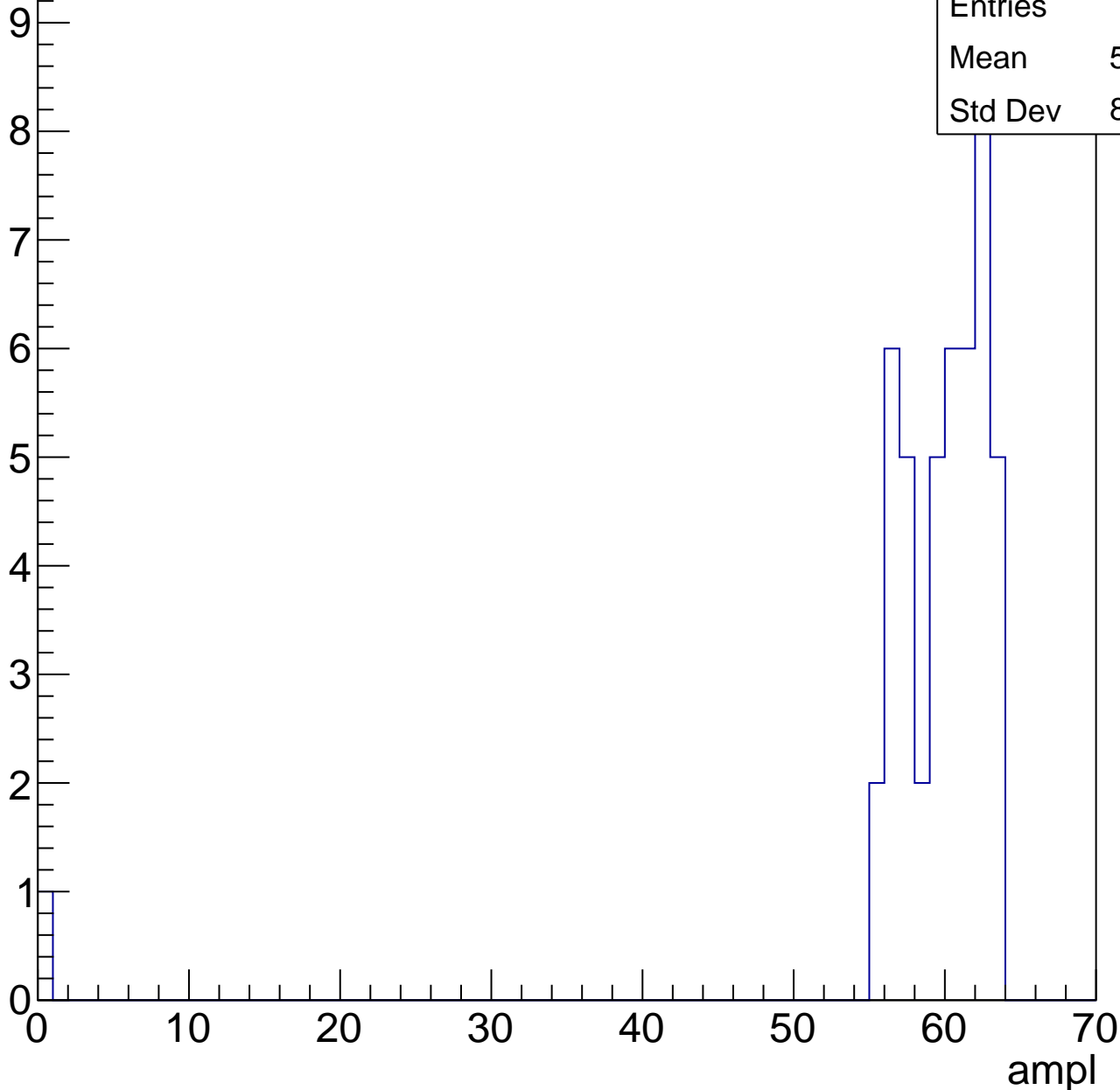


# B0L001S, U5-ch69, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

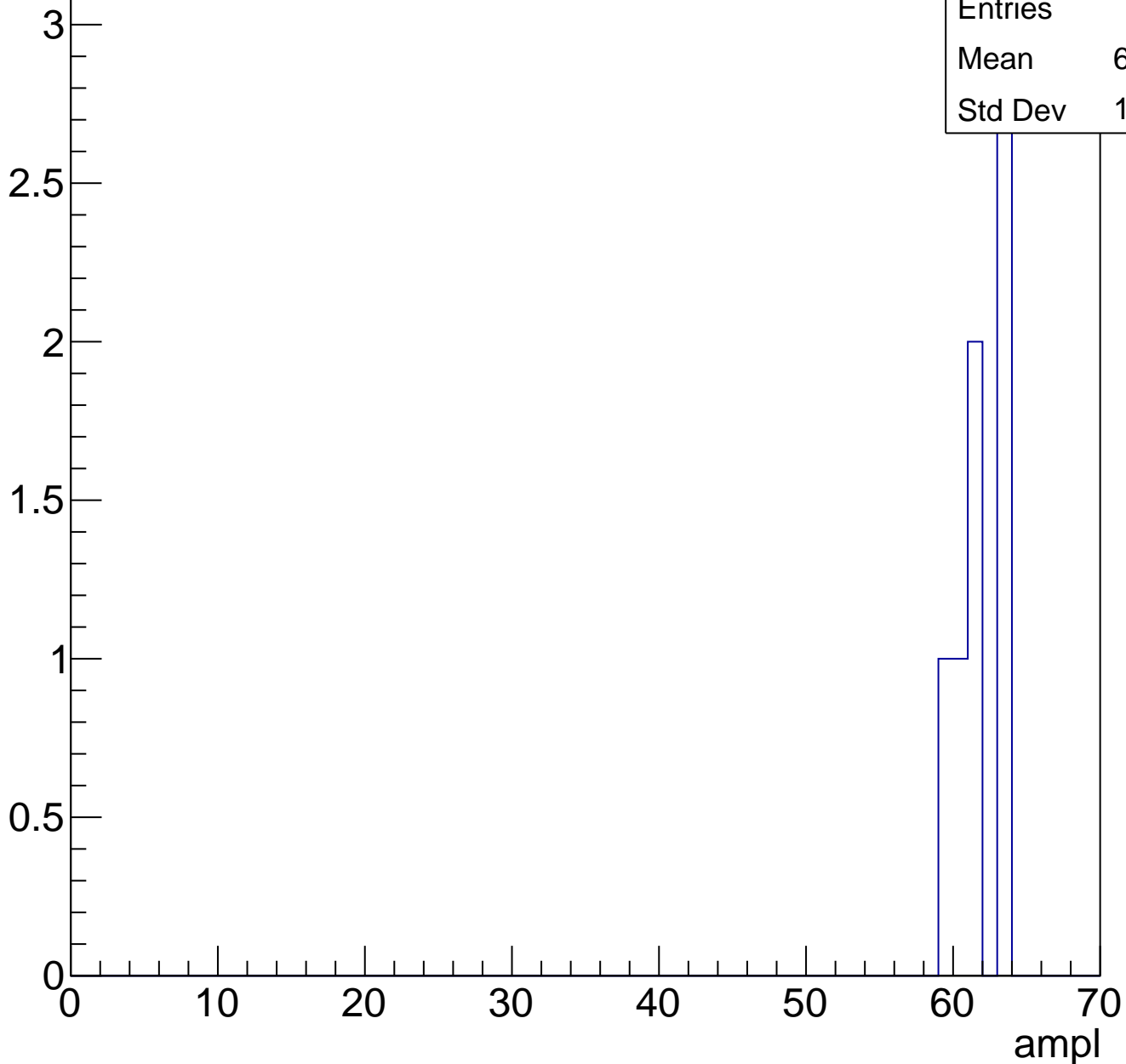
Entries	47
Mean	58.32
Std Dev	8.942



# B0L001S, U5-ch69, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch69, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	3
Mean	0
Std Dev	0

# B0L001S, U5-ch70, adc0

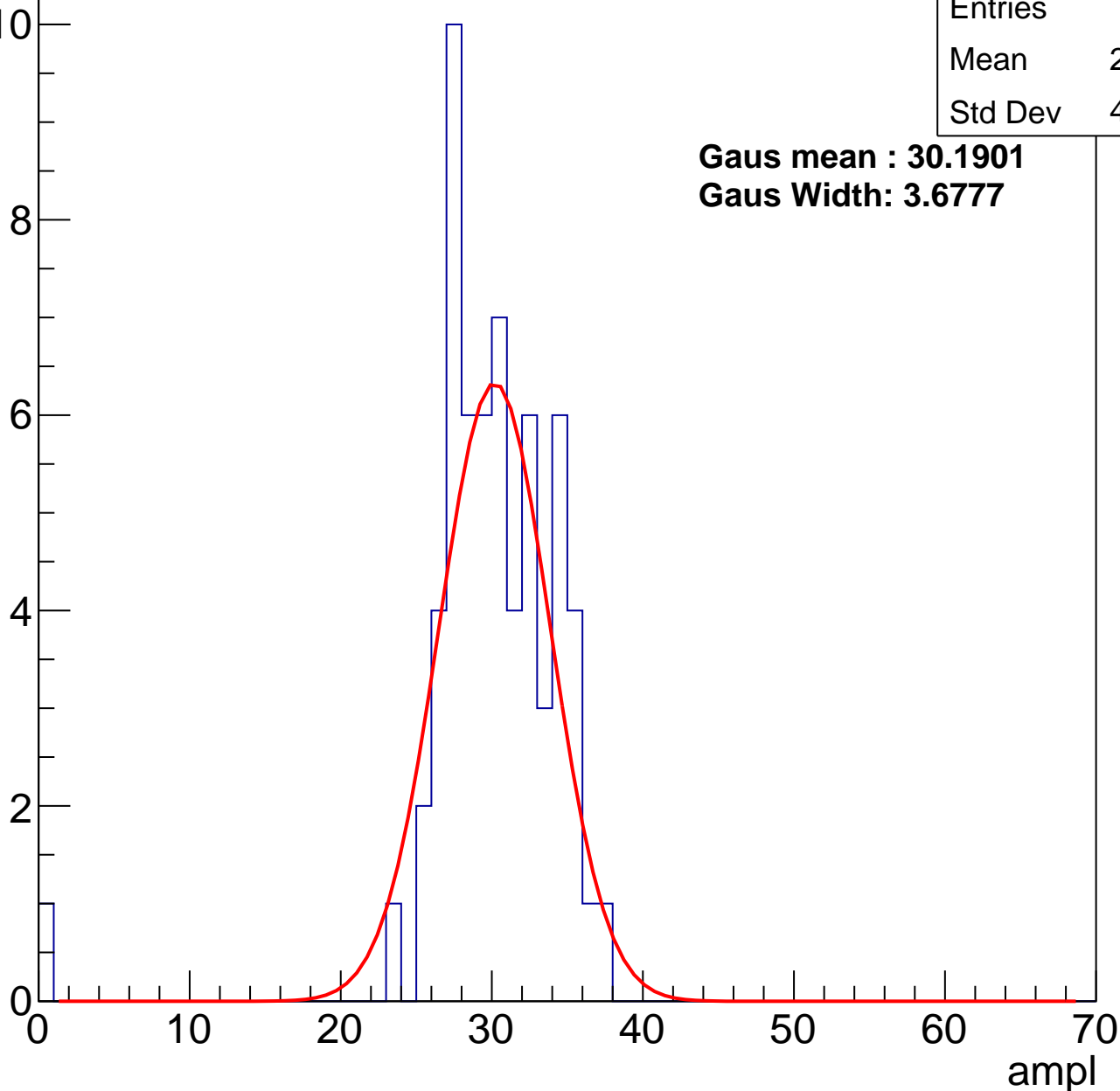
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	29.53
Std Dev	4.928

**Gaus mean : 30.1901**

**Gaus Width: 3.6777**



# B0L001S, U5-ch70, adc1

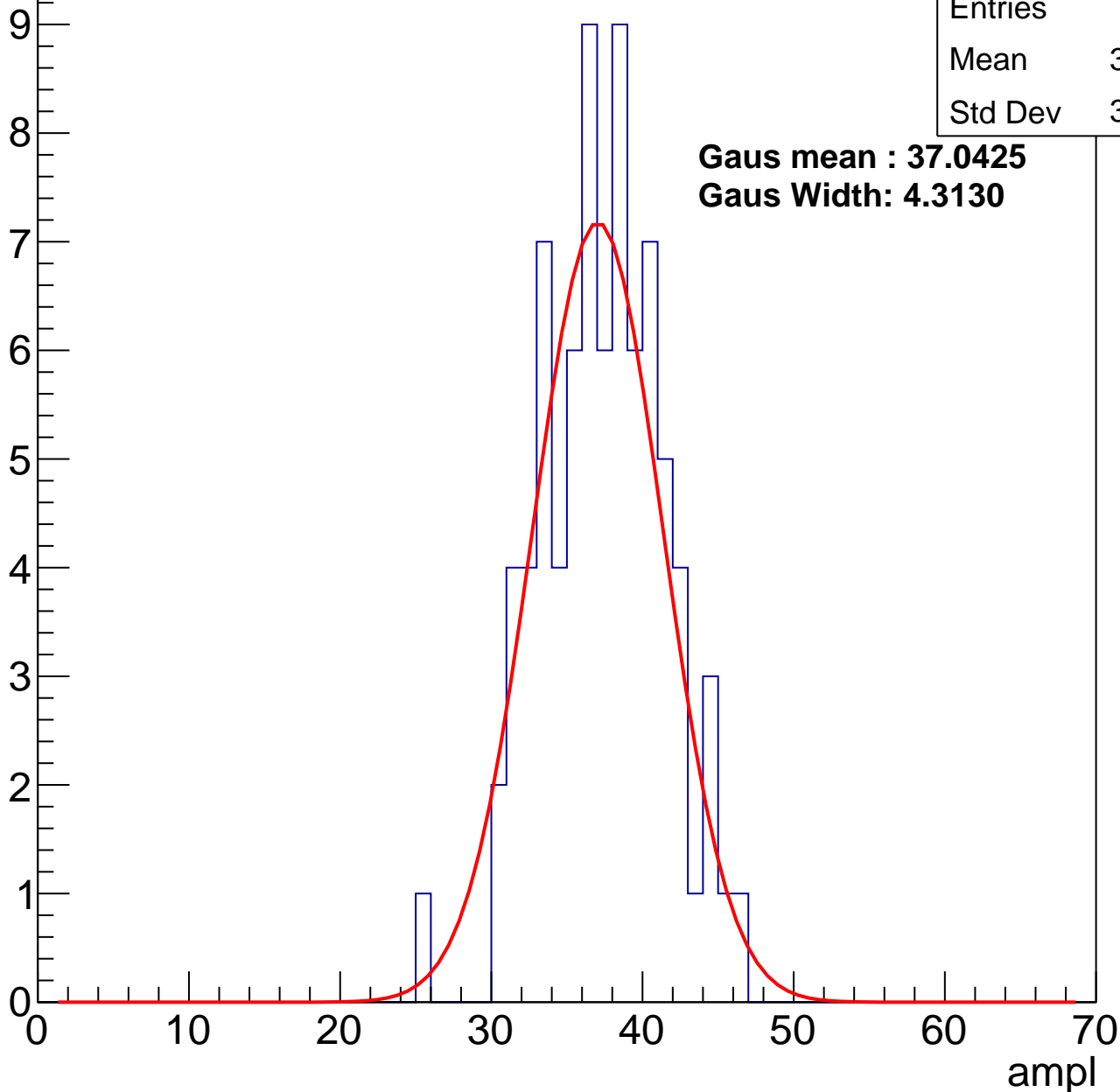
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	80
Mean	36.94
Std Dev	3.985

**Gaus mean : 37.0425**

**Gaus Width: 4.3130**



# B0L001S, U5-ch70, adc2

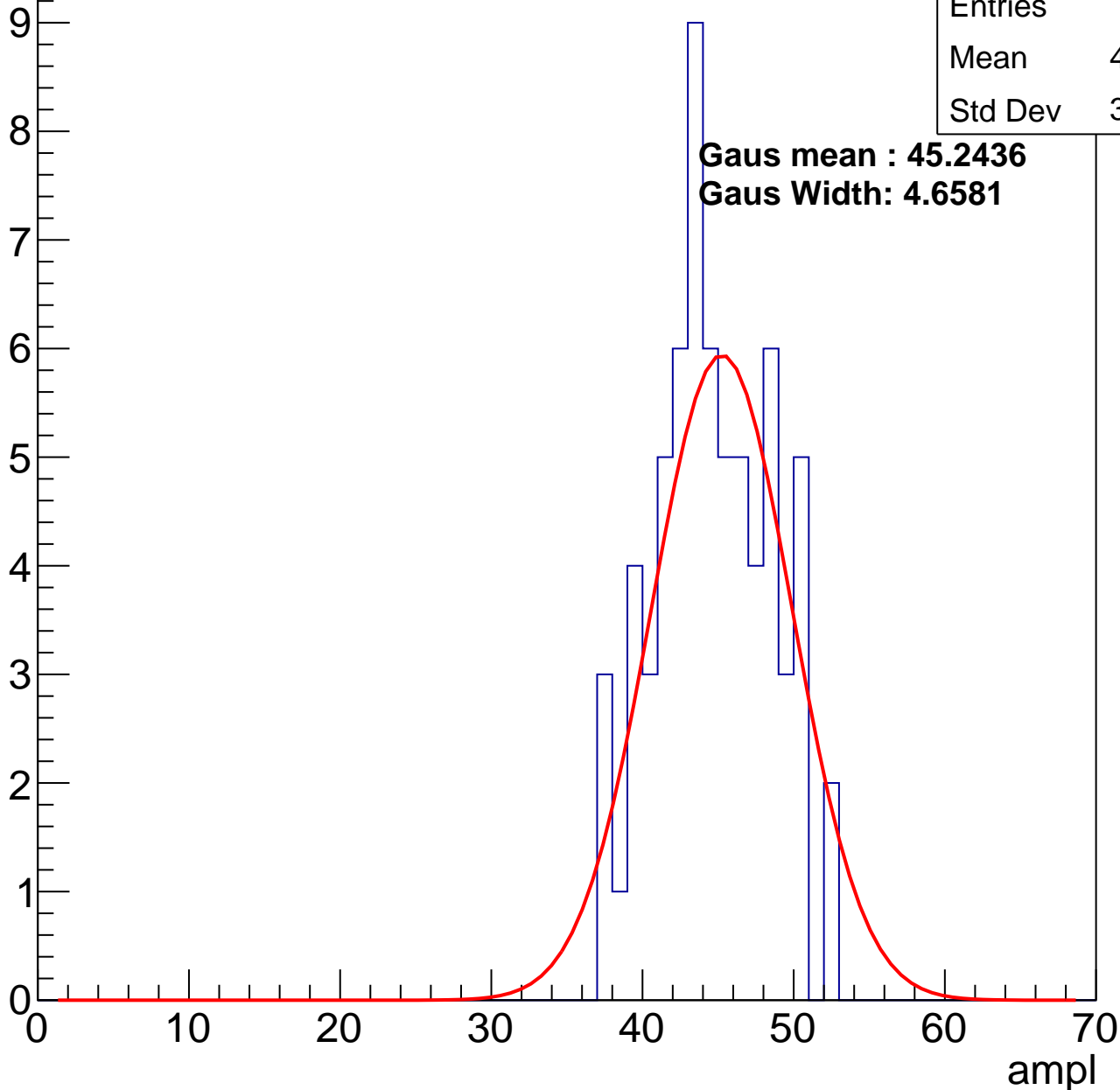
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	44.25
Std Dev	3.755

**Gaus mean : 45.2436**

**Gaus Width: 4.6581**

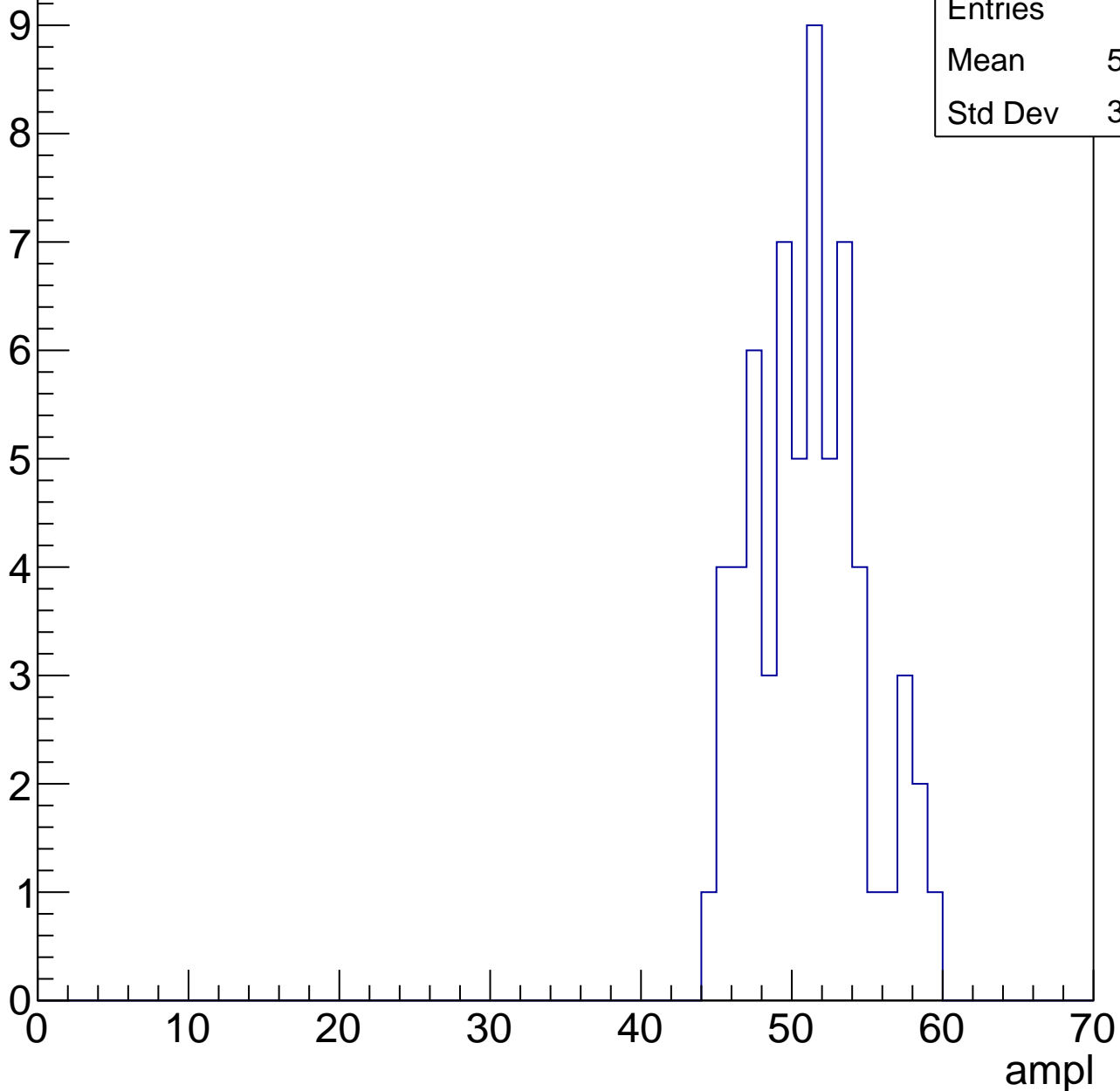


# B0L001S, U5-ch70, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	50.63
Std Dev	3.609

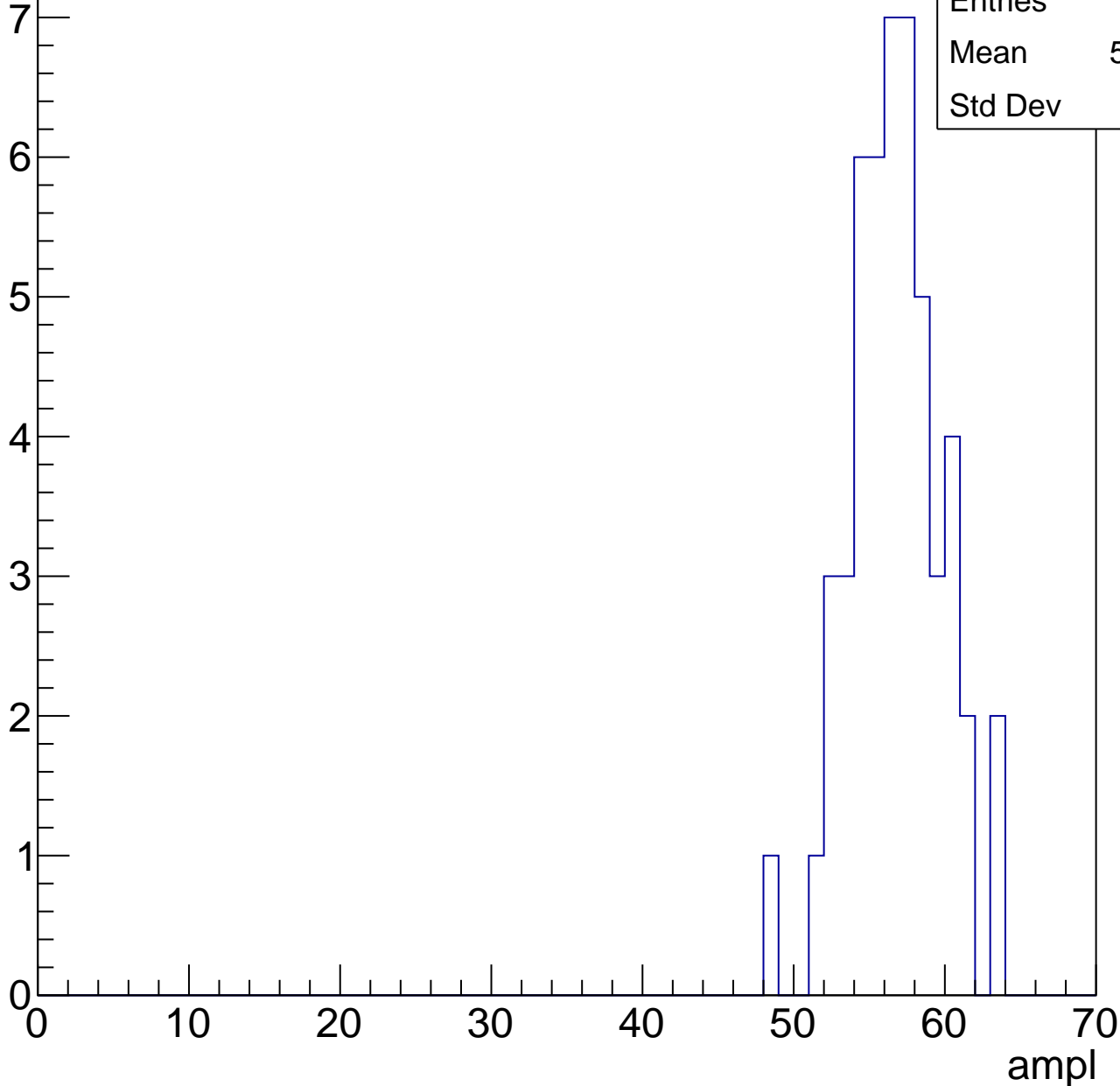


# B0L001S, U5-ch70, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	50
Mean	56.28
Std Dev	3.02

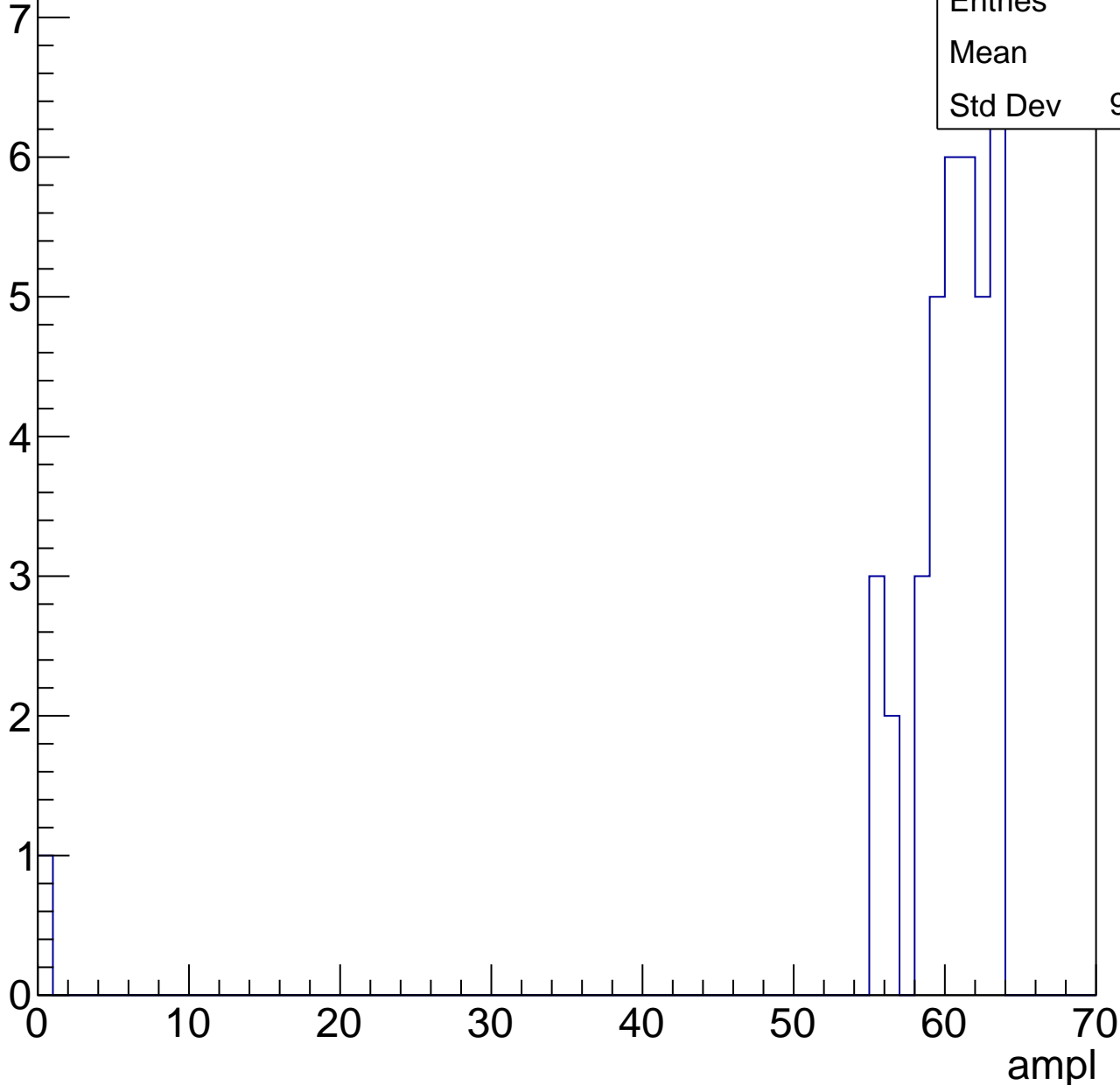


# B0L001S, U5-ch70, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	38
Mean	58.5
Std Dev	9.904

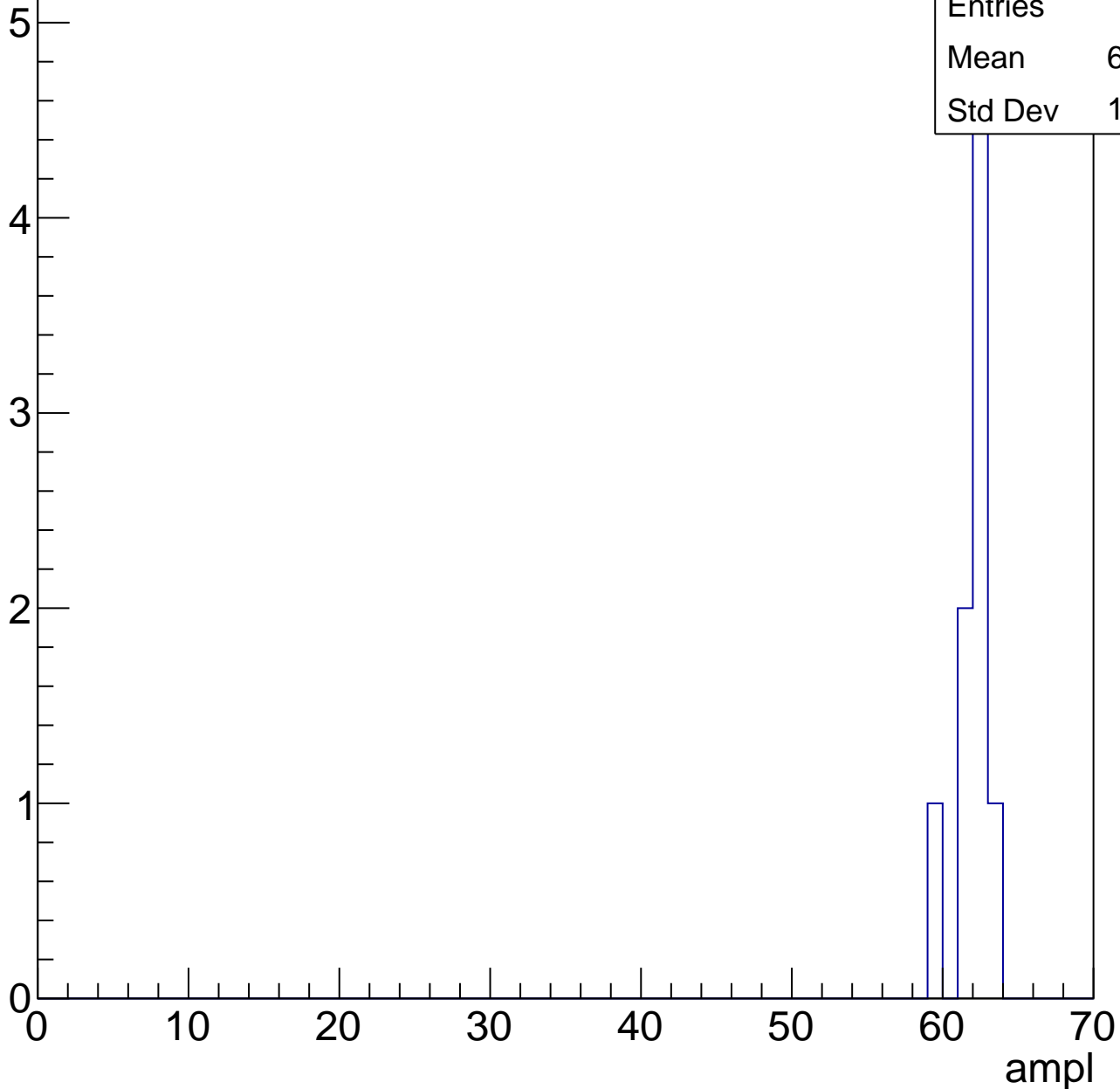


# B0L001S, U5-ch70, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	9
Mean	61.56
Std Dev	1.066





# B0L001S, U5-ch70, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch71, adc0

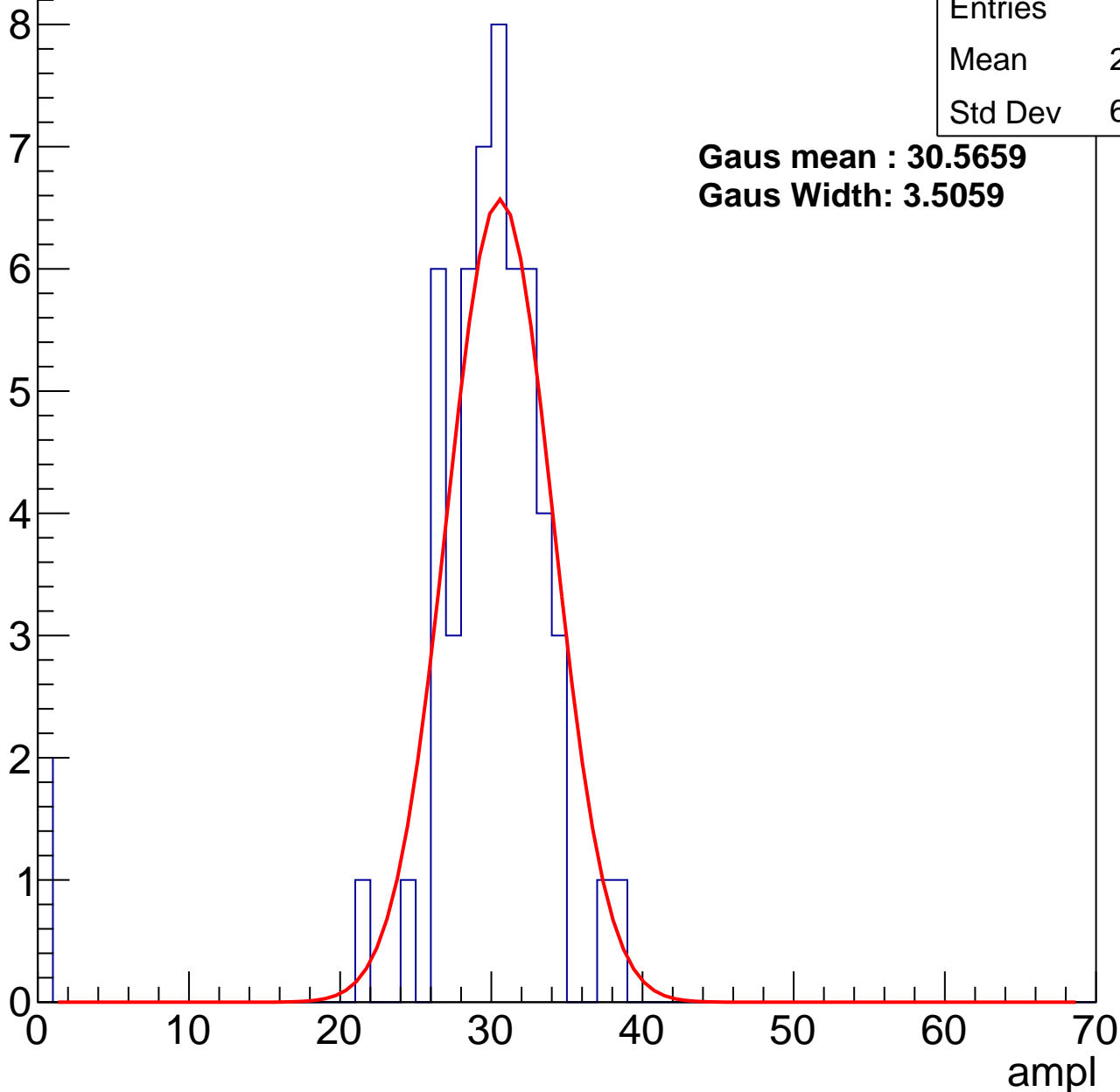
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	28.73
Std Dev	6.337

**Gaus mean : 30.5659**

**Gaus Width: 3.5059**



# B0L001S, U5-ch71, adc1

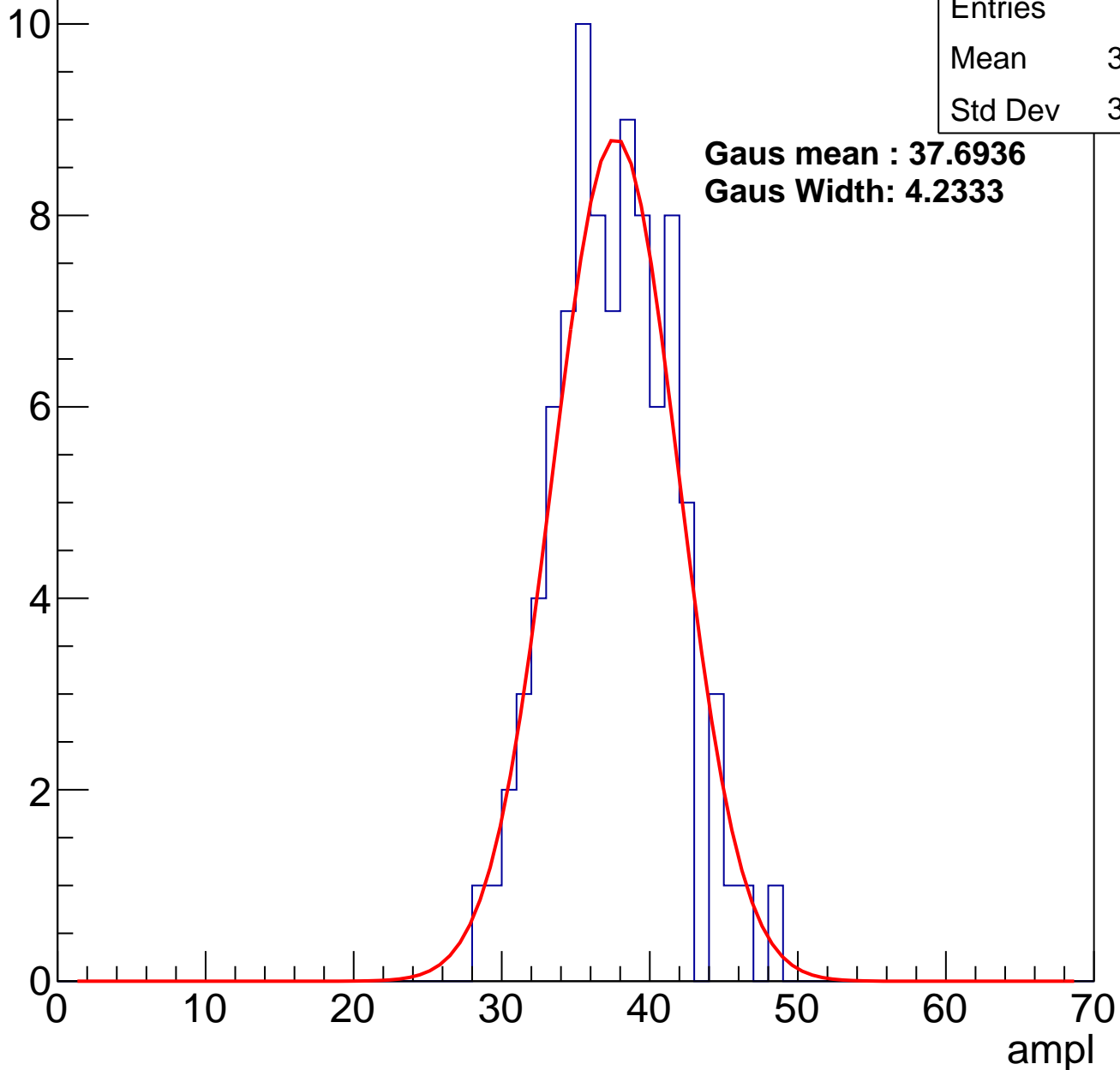
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	91
Mean	37.08
Std Dev	3.948

**Gaus mean : 37.6936**

**Gaus Width: 4.2333**

Entry



# B0L001S, U5-ch71, adc2

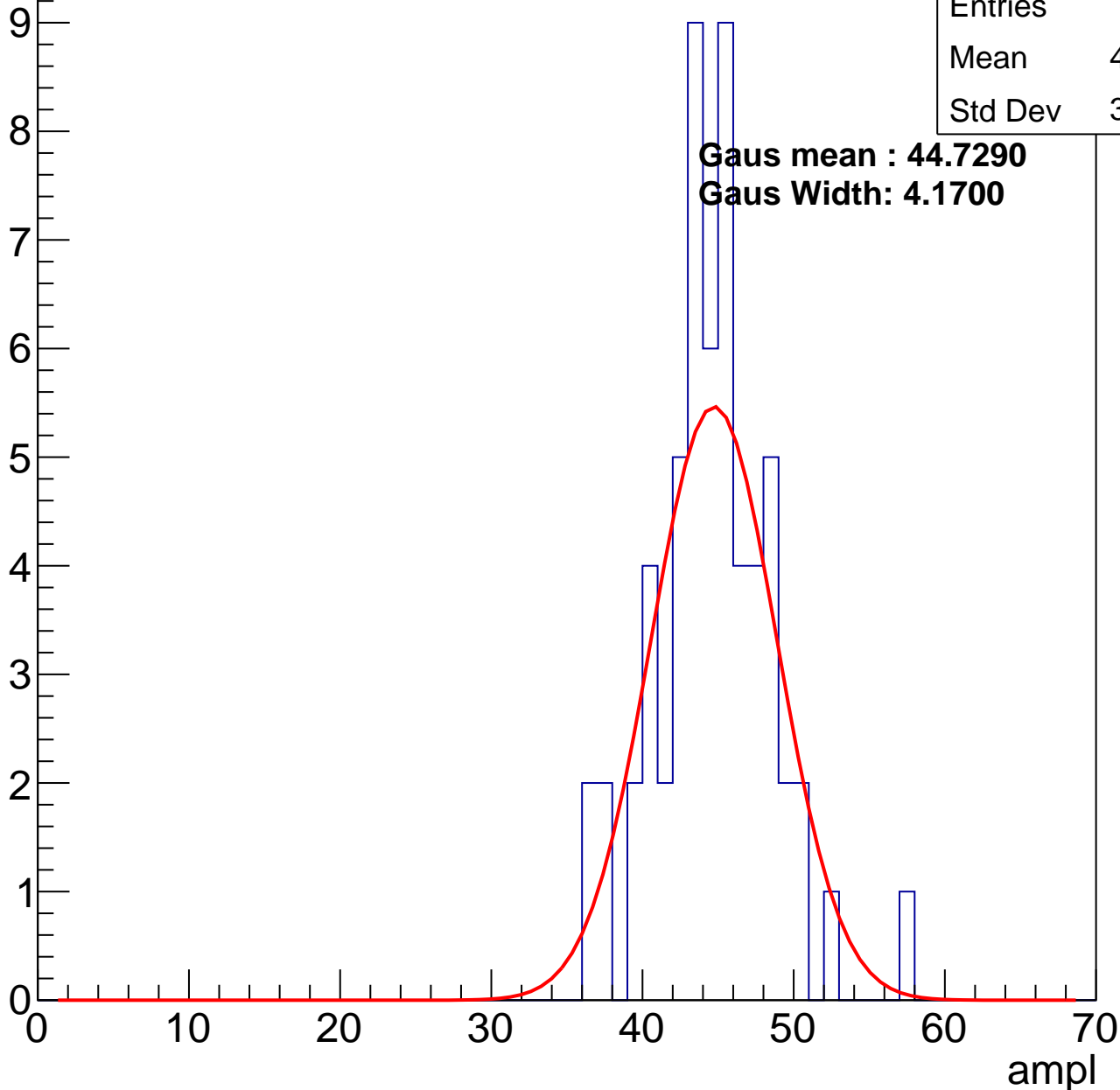
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	44.18
Std Dev	3.832

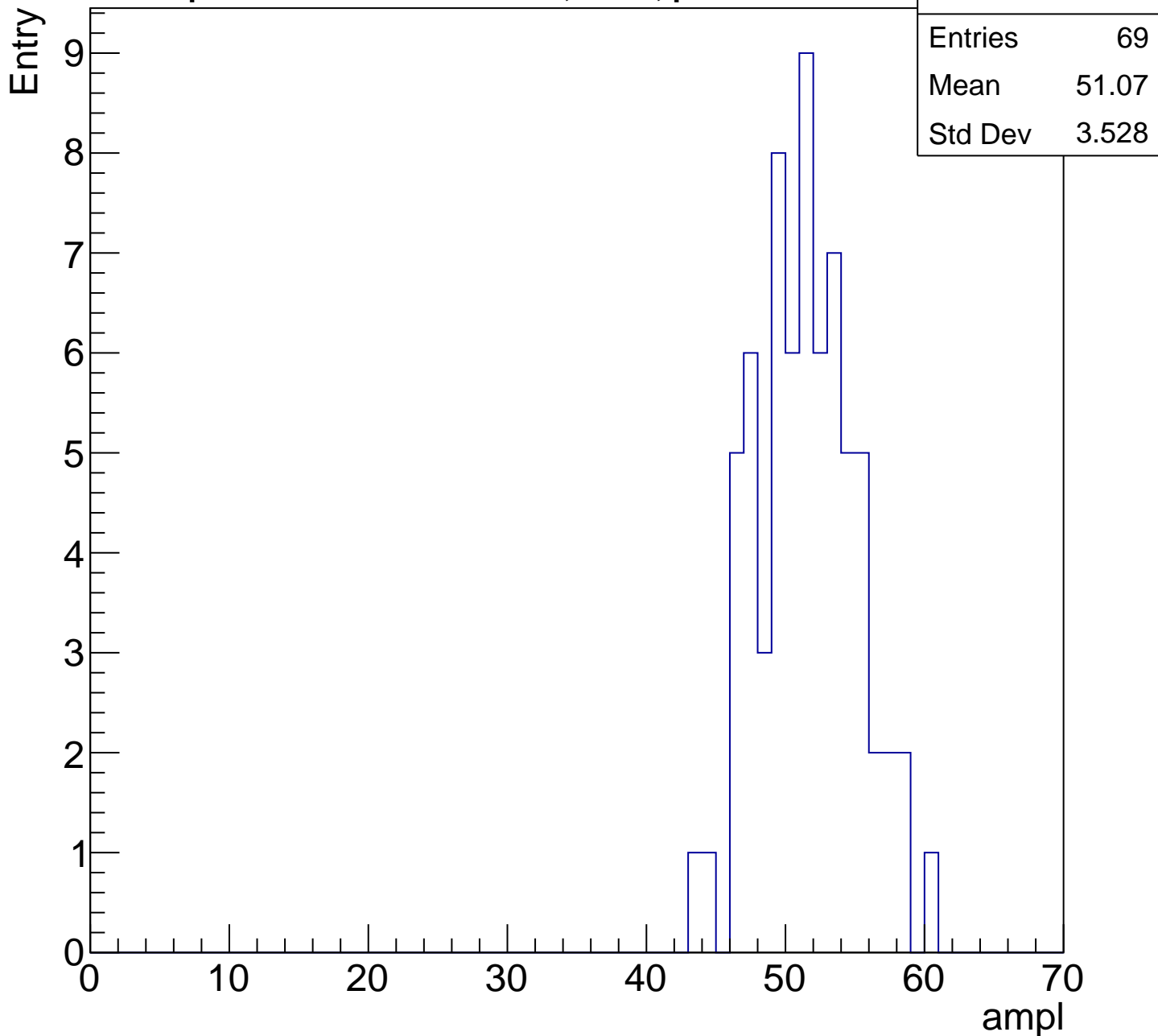
**Gaus mean : 44.7290**

**Gaus Width: 4.1700**



# B0L001S, U5-ch71, adc3

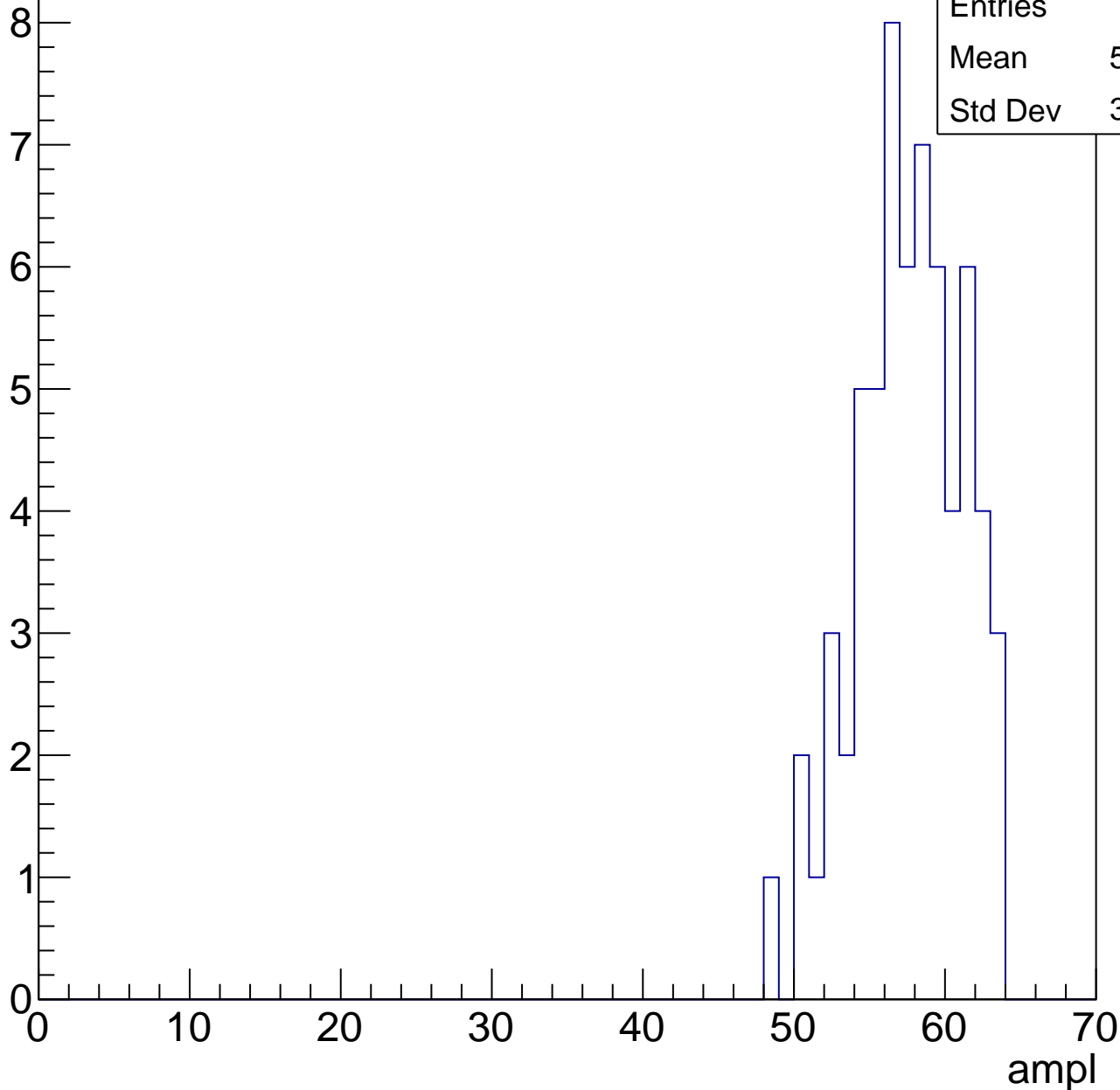
calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U5-ch71, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

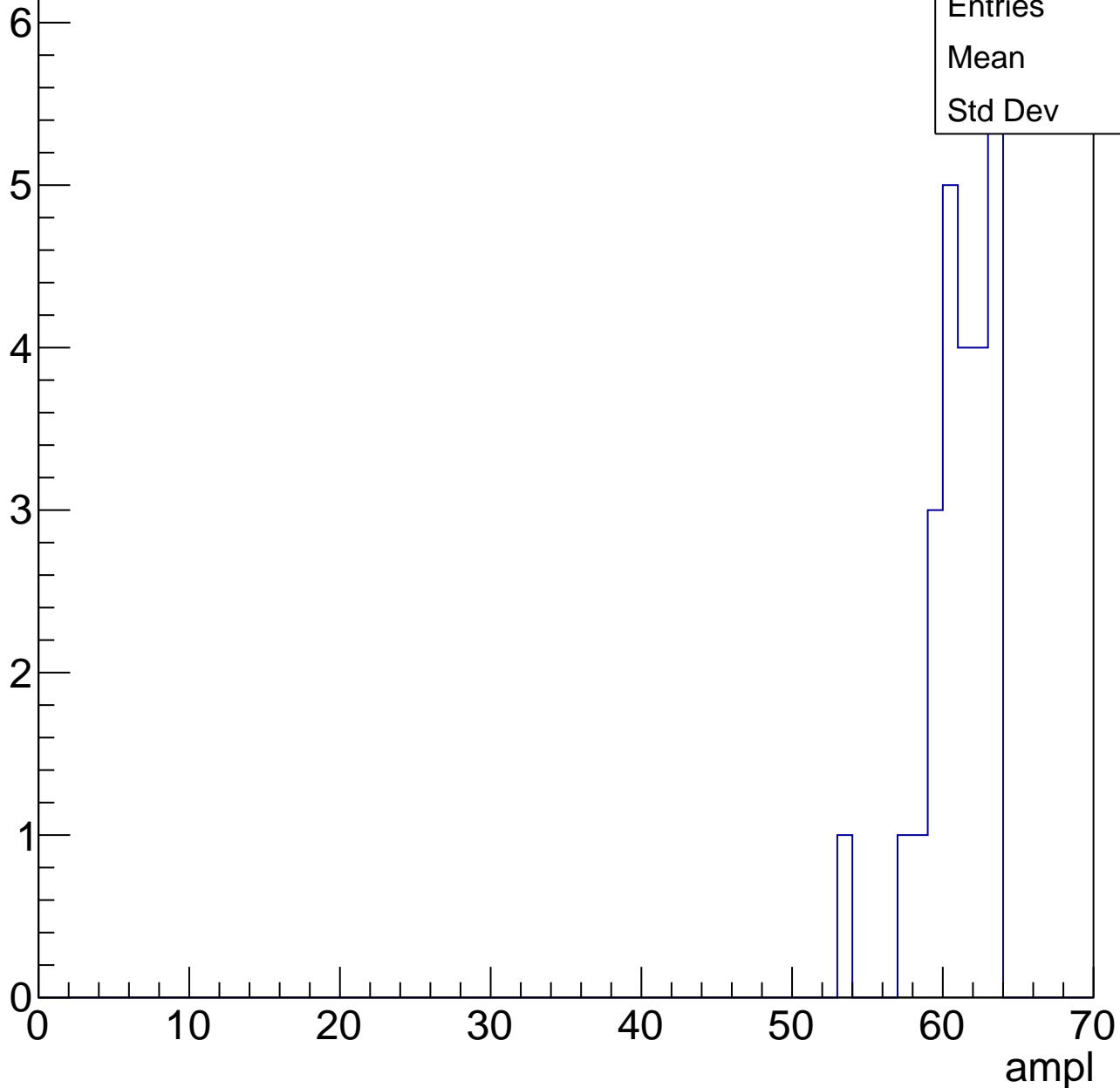


# B0L001S, U5-ch71, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

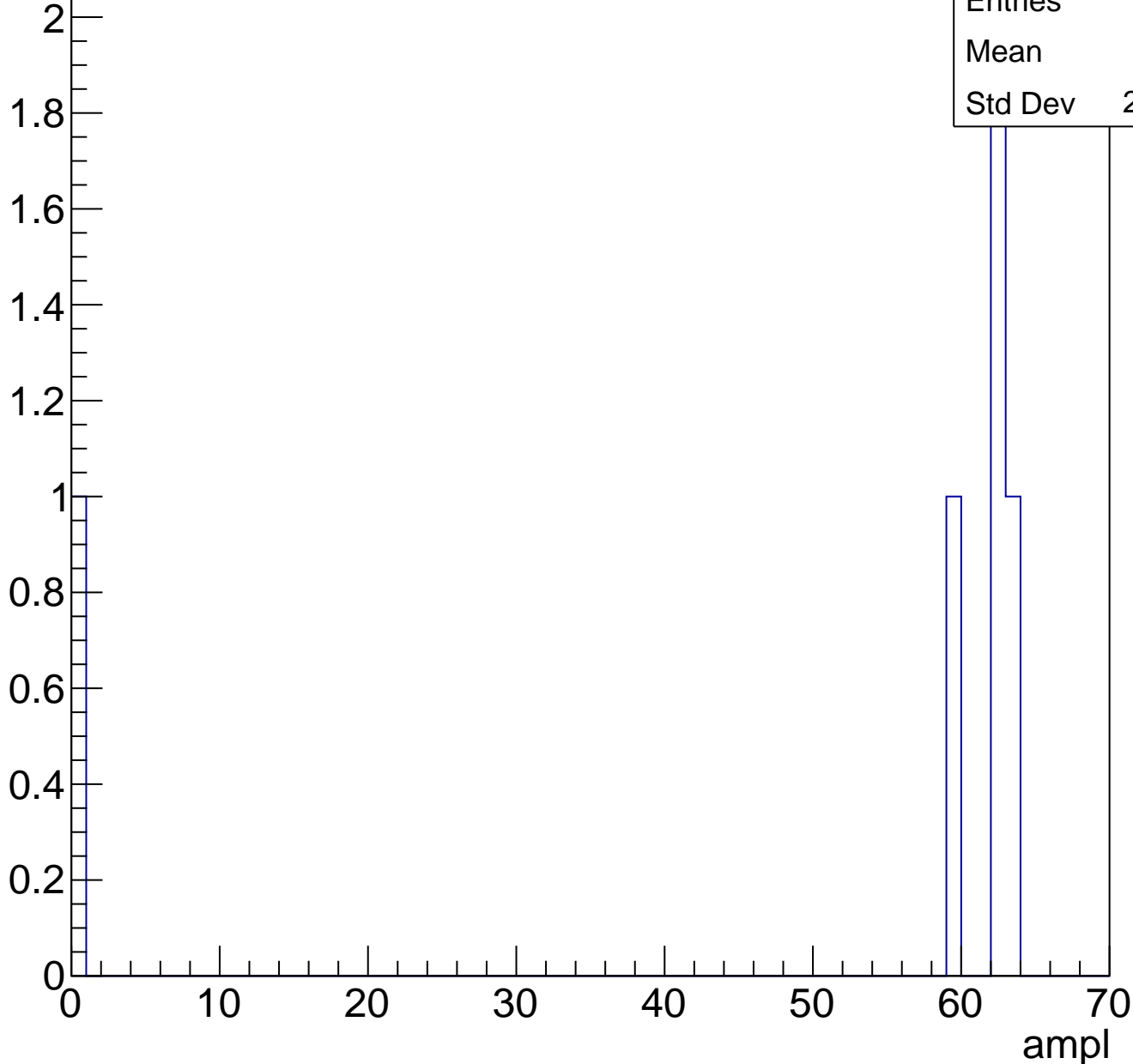
Entries	25
Mean	60.6
Std Dev	2.28



# B0L001S, U5-ch71, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch71, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L001S, U5-ch72, adc0

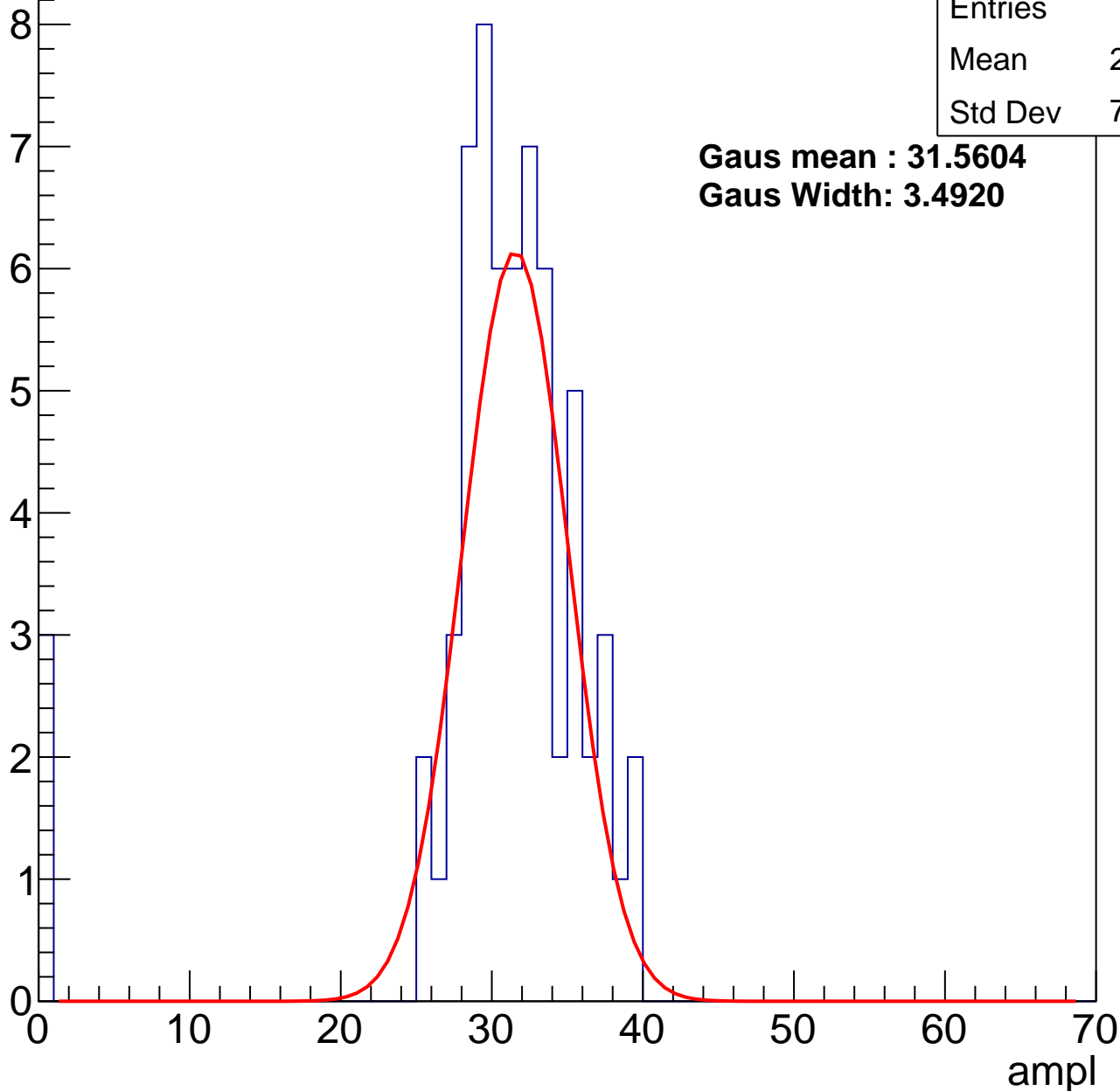
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	29.92
Std Dev	7.415

**Gaus mean : 31.5604**

**Gaus Width: 3.4920**



# B0L001S, U5-ch72, adc1

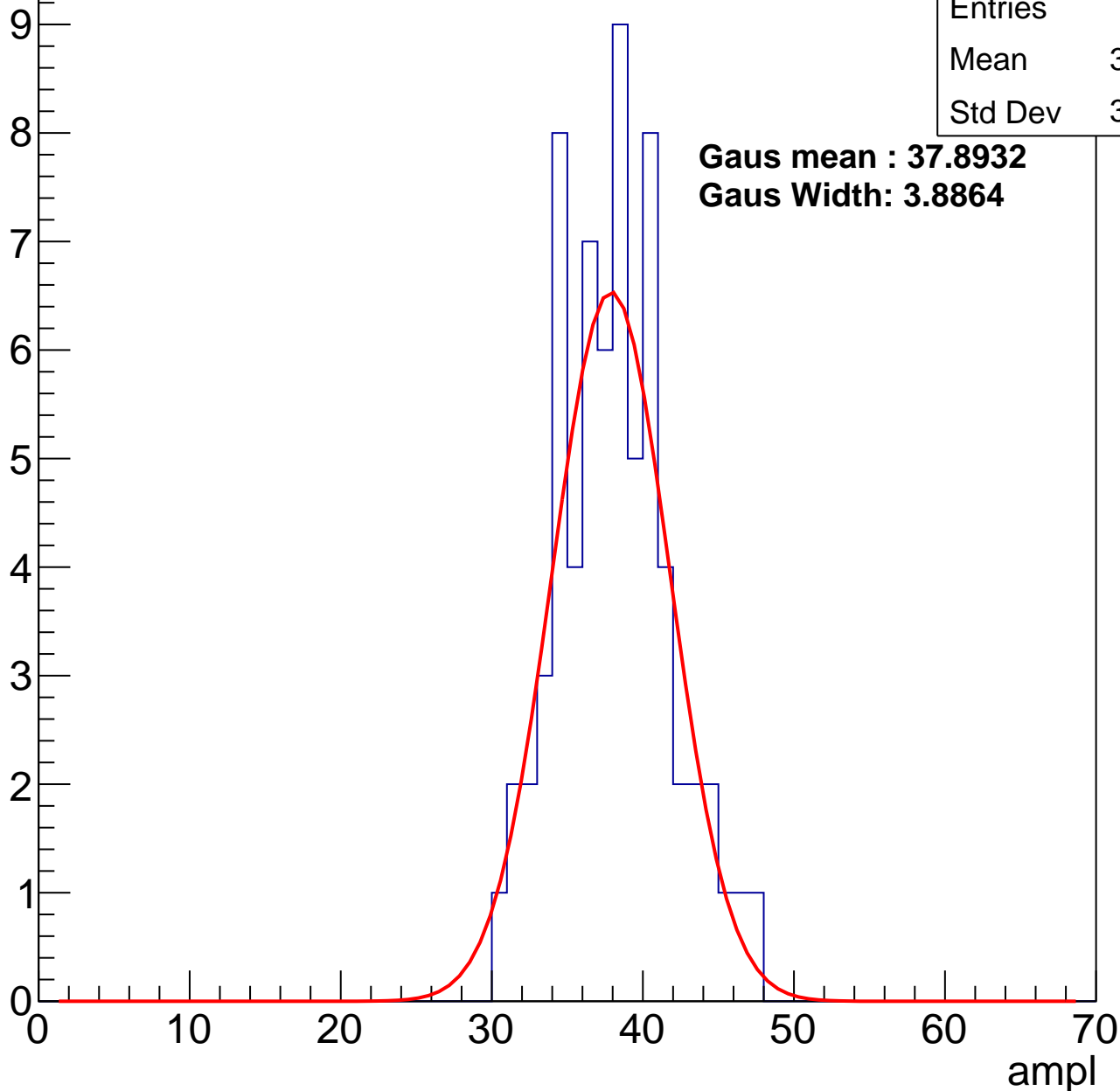
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	37.62
Std Dev	3.674

**Gaus mean : 37.8932**

**Gaus Width: 3.8864**



# B0L001S, U5-ch72, adc2

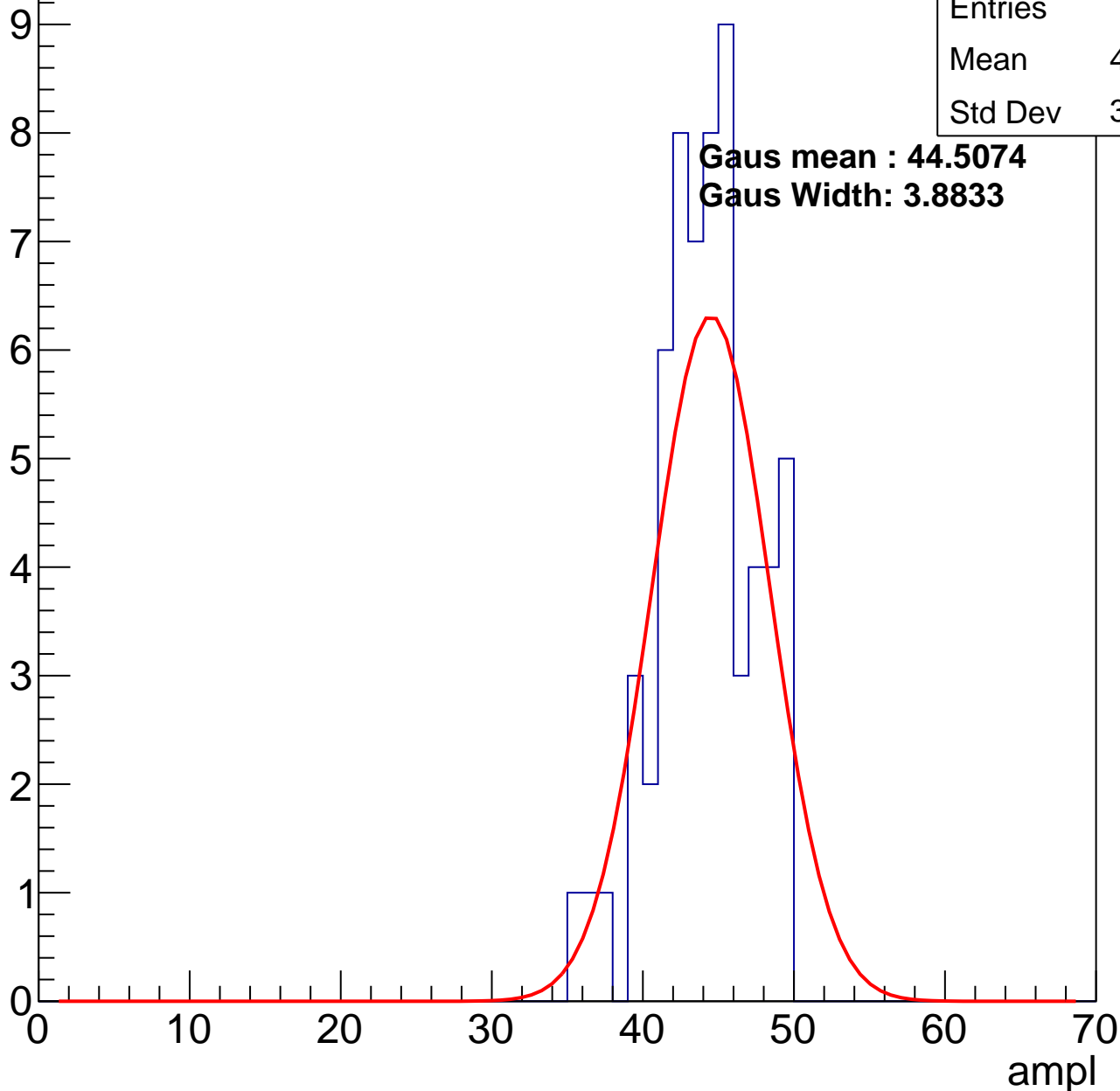
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	43.68
Std Dev	3.197

**Gaus mean : 44.5074**

**Gaus Width: 3.8833**

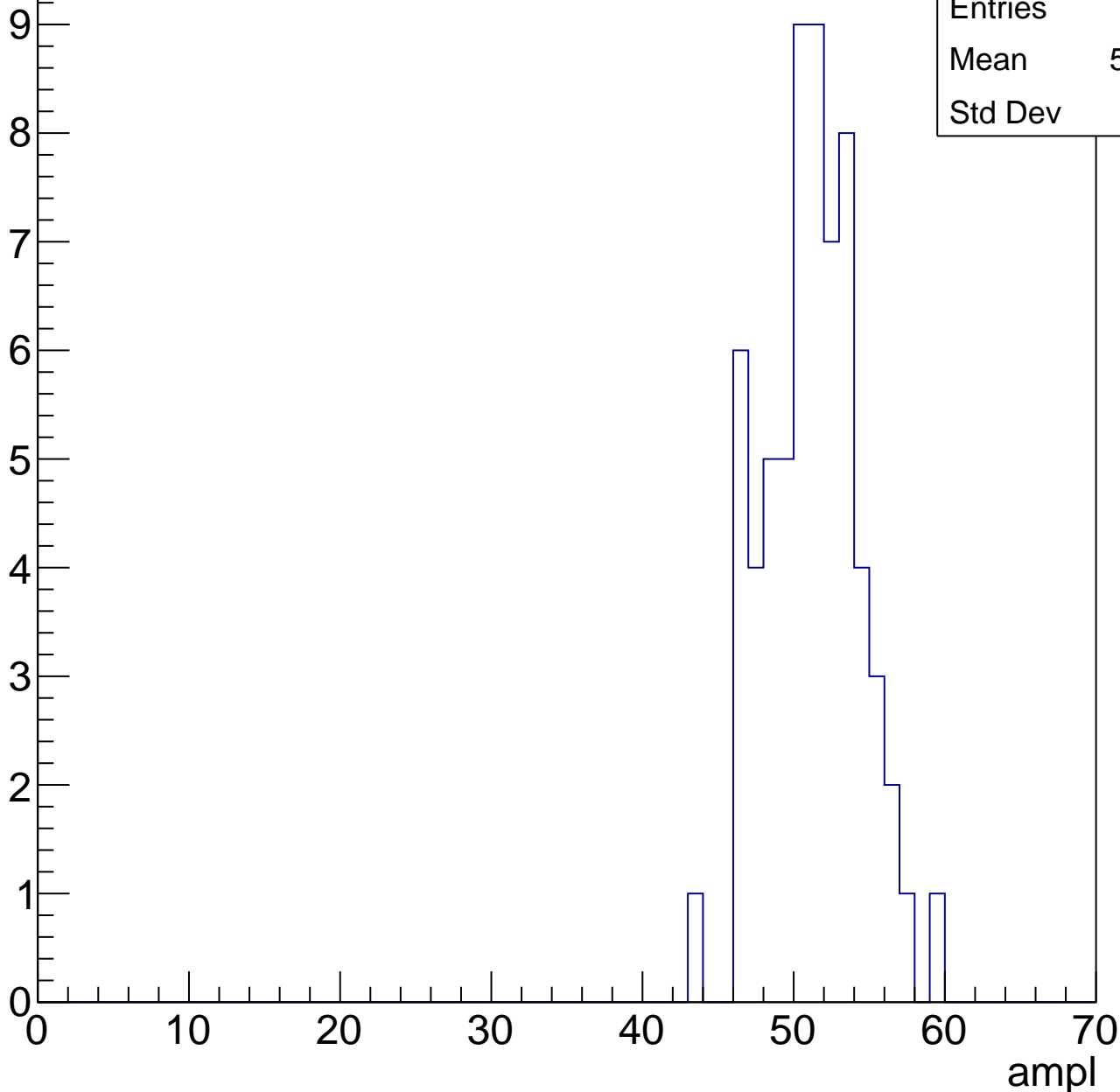


# B0L001S, U5-ch72, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	50.74
Std Dev	3.09

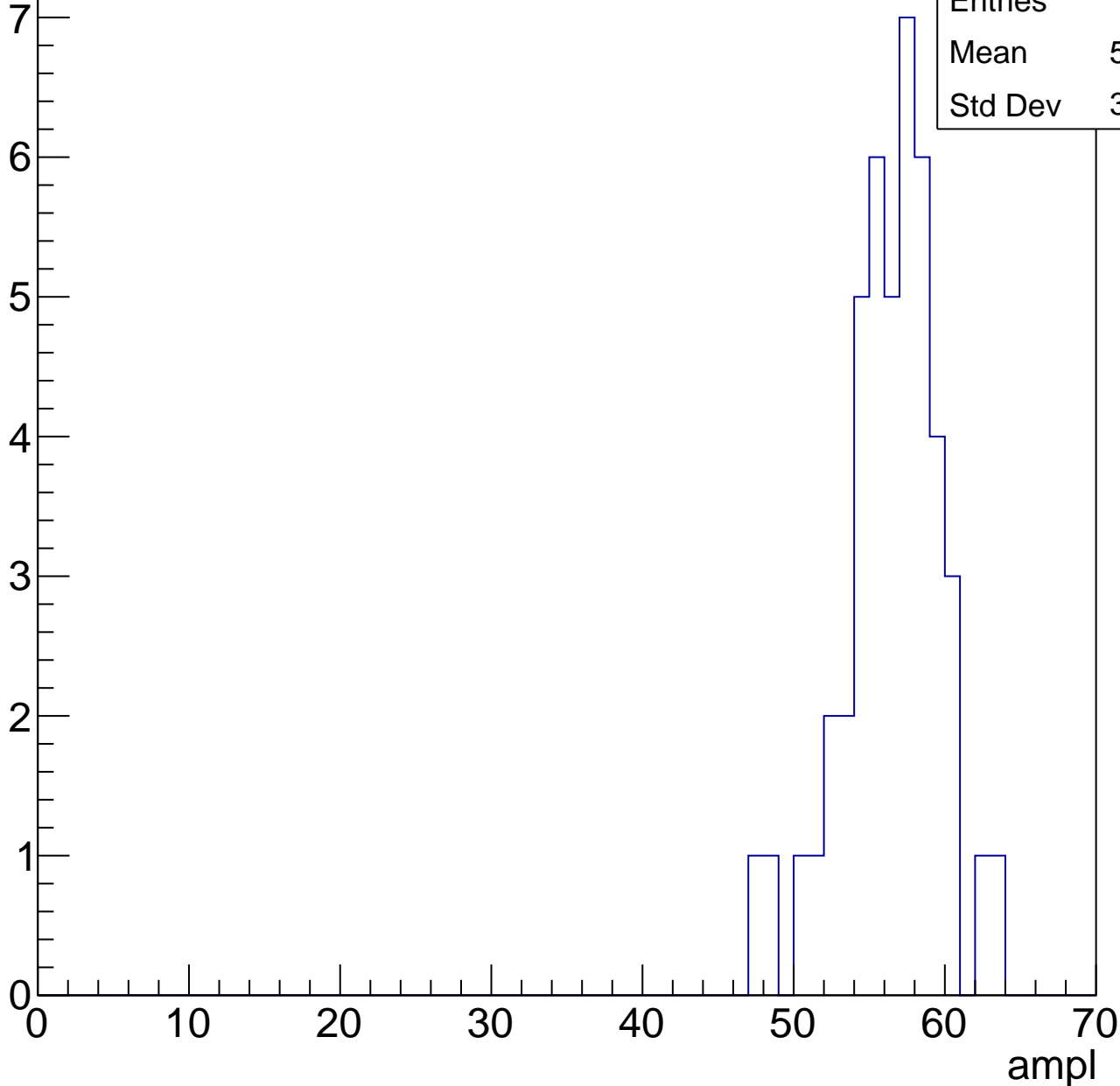


# B0L001S, U5-ch72, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	46
Mean	55.96
Std Dev	3.237

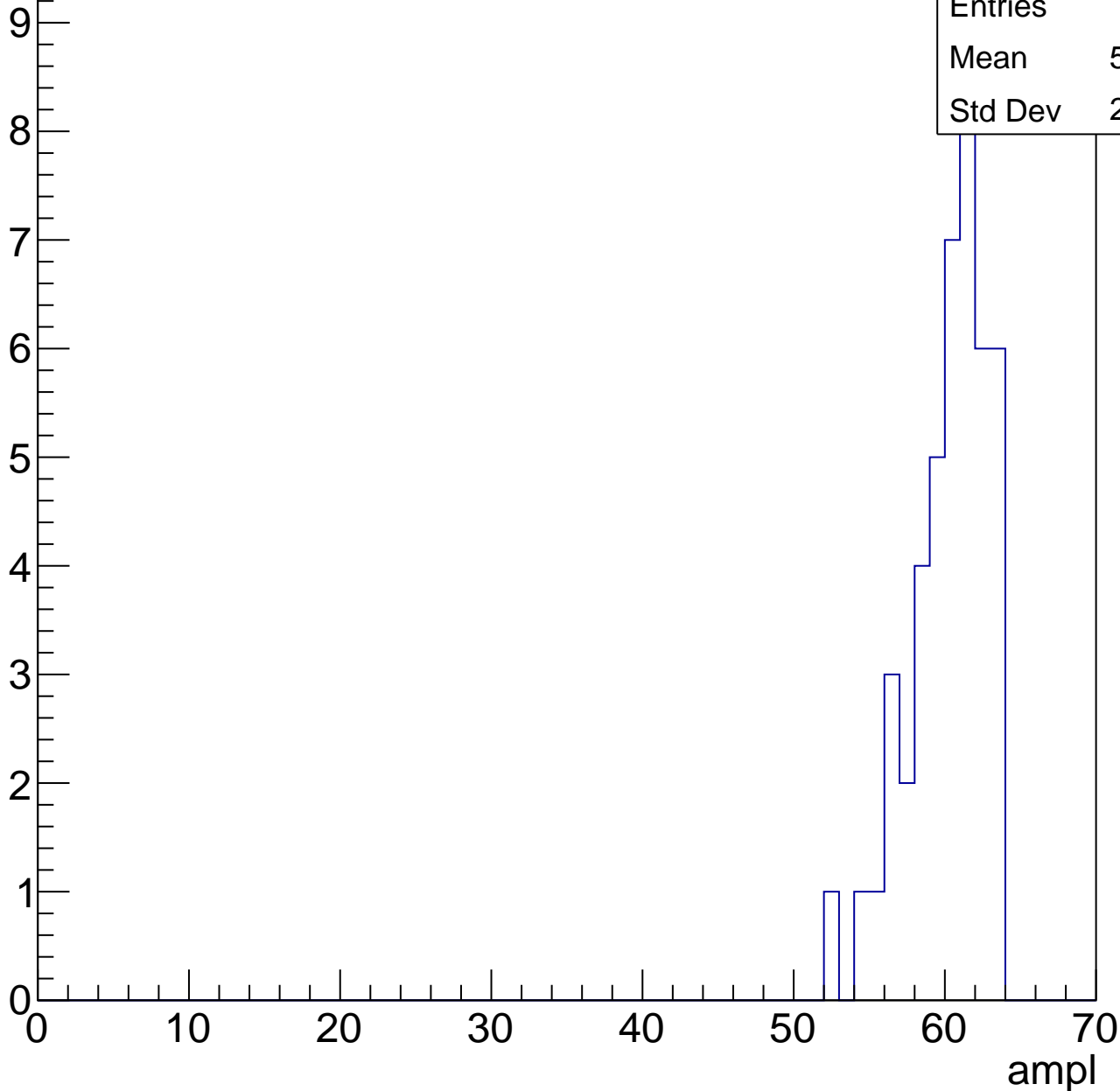


# B0L001S, U5-ch72, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

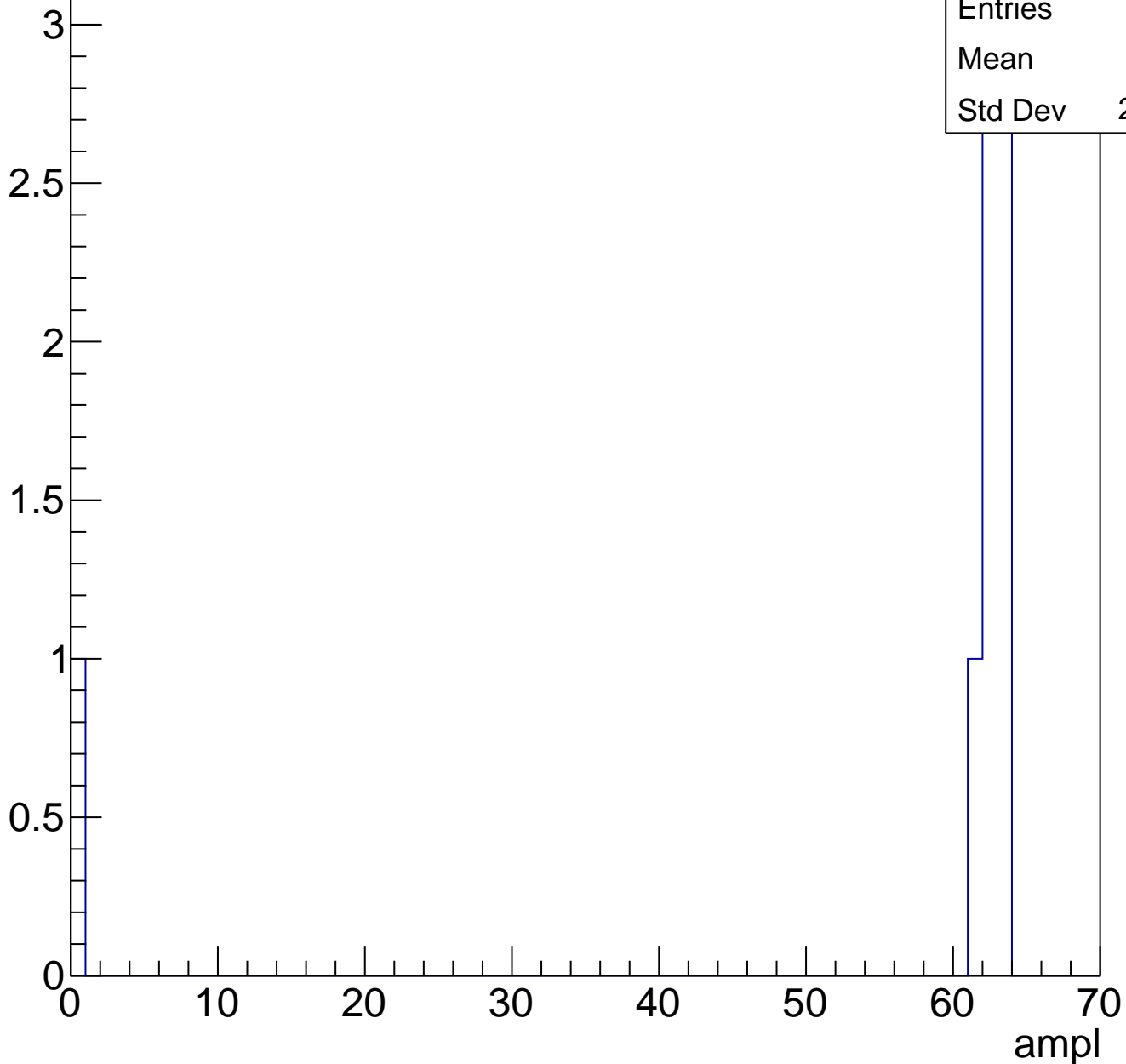
Entries	45
Mean	59.76
Std Dev	2.566



# B0L001S, U5-ch72, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	8
Mean	54.5
Std Dev	20.61



# B0L001S, U5-ch72, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch73, adc0

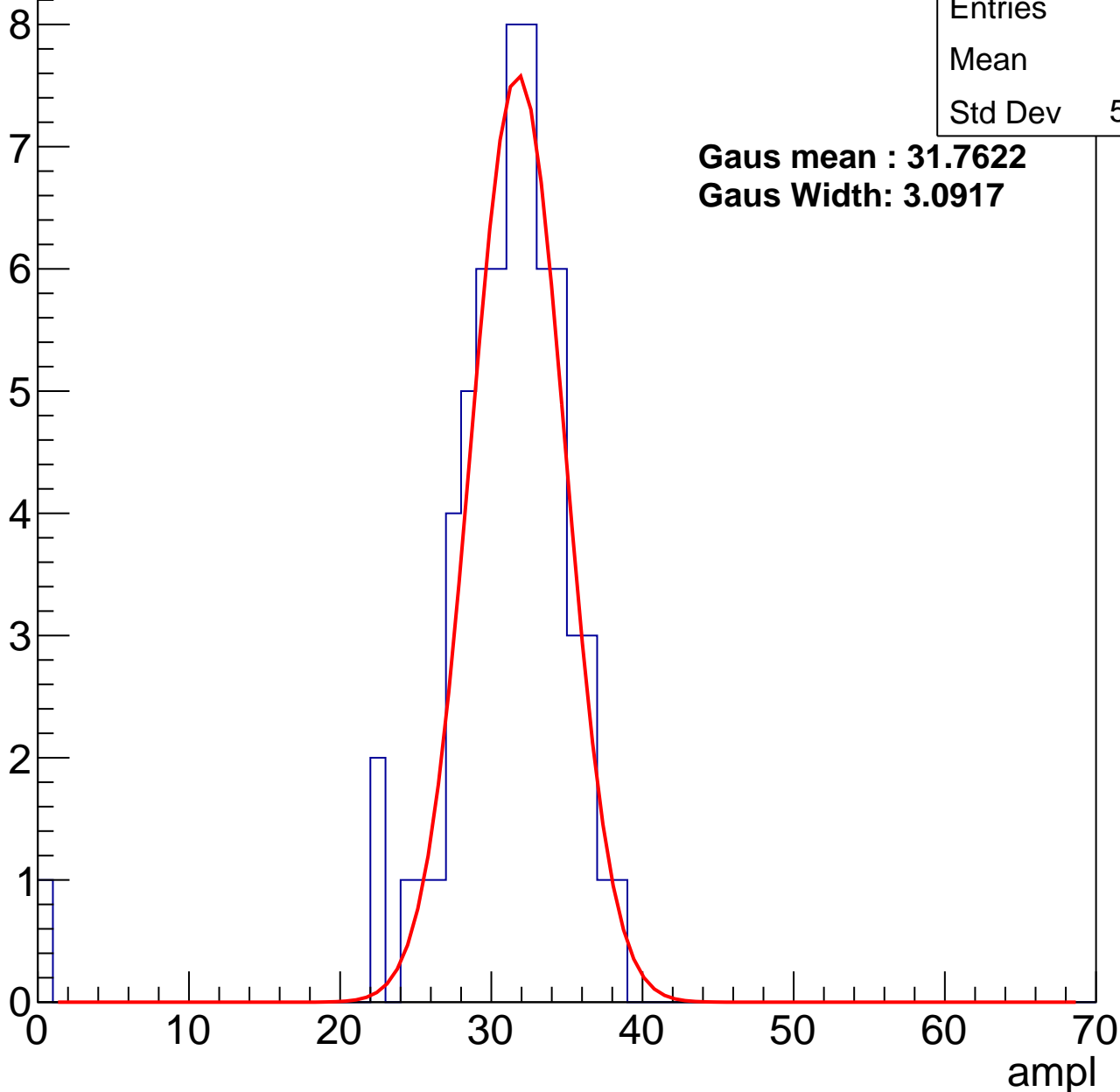
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	30.4
Std Dev	5.107

**Gaus mean : 31.7622**

**Gaus Width: 3.0917**



# B0L001S, U5-ch73, adc1

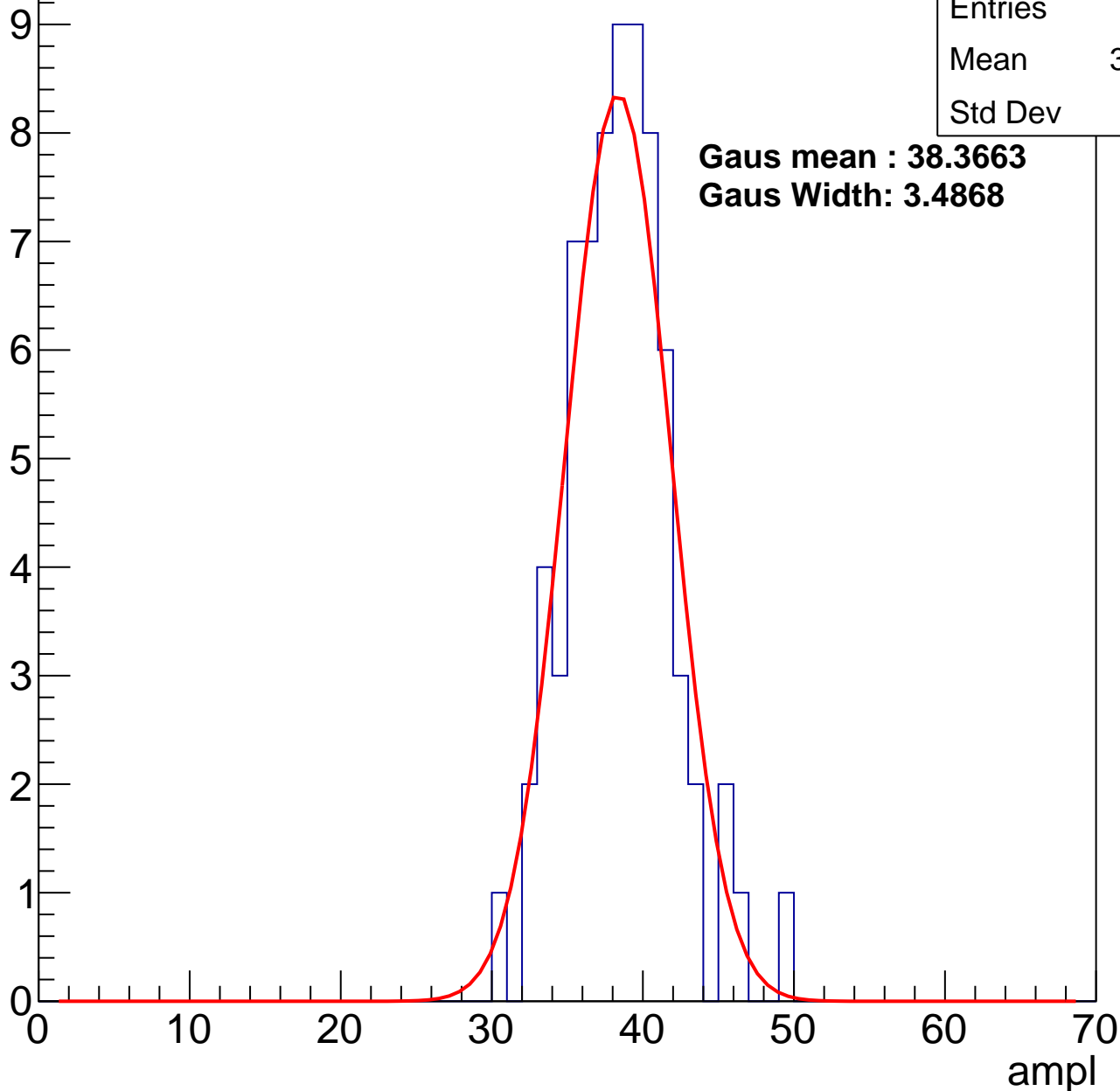
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	38.04
Std Dev	3.43

**Gaus mean : 38.3663**

**Gaus Width: 3.4868**



# B0L001S, U5-ch73, adc2

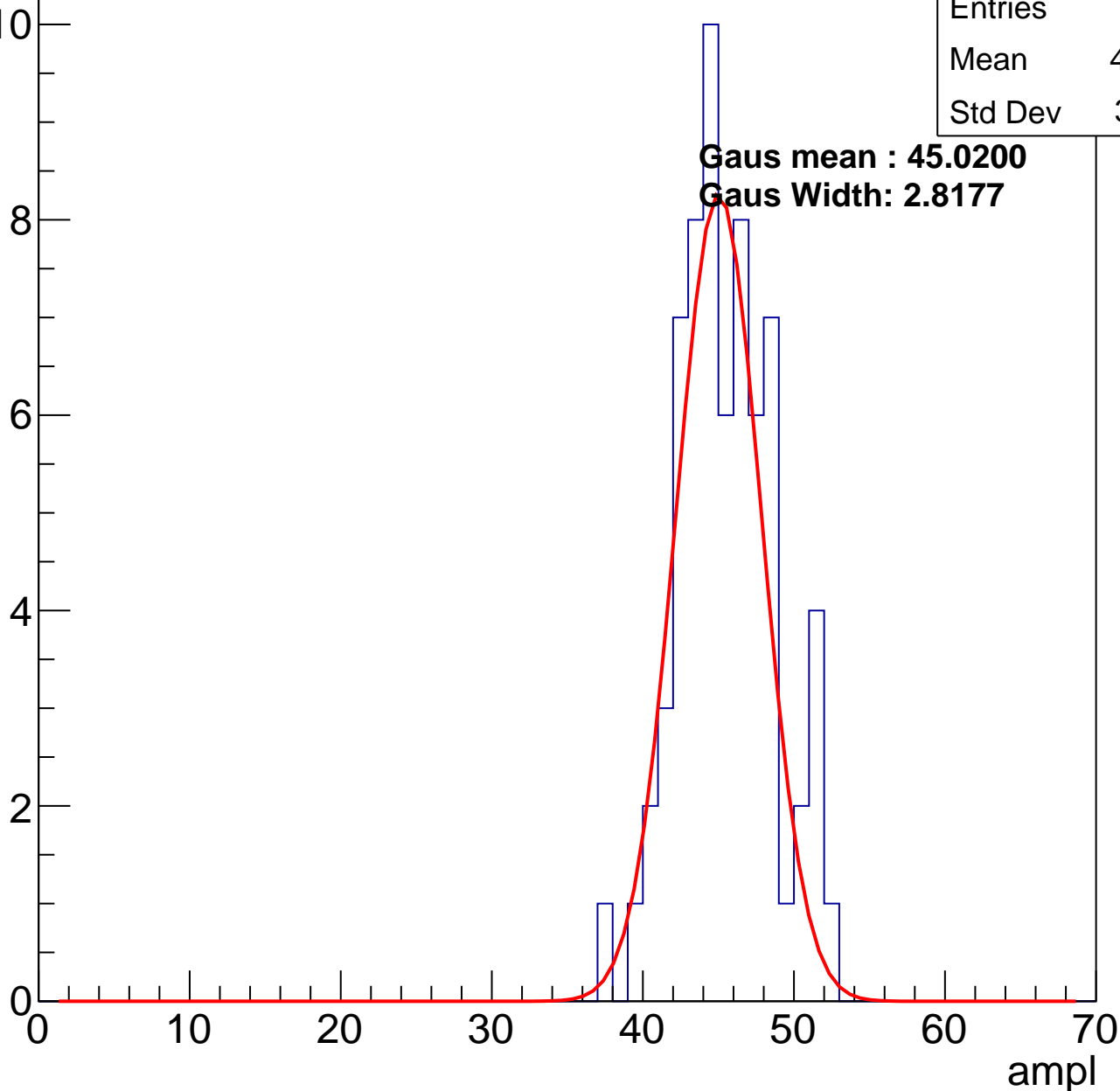
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	45.04
Std Dev	3.131

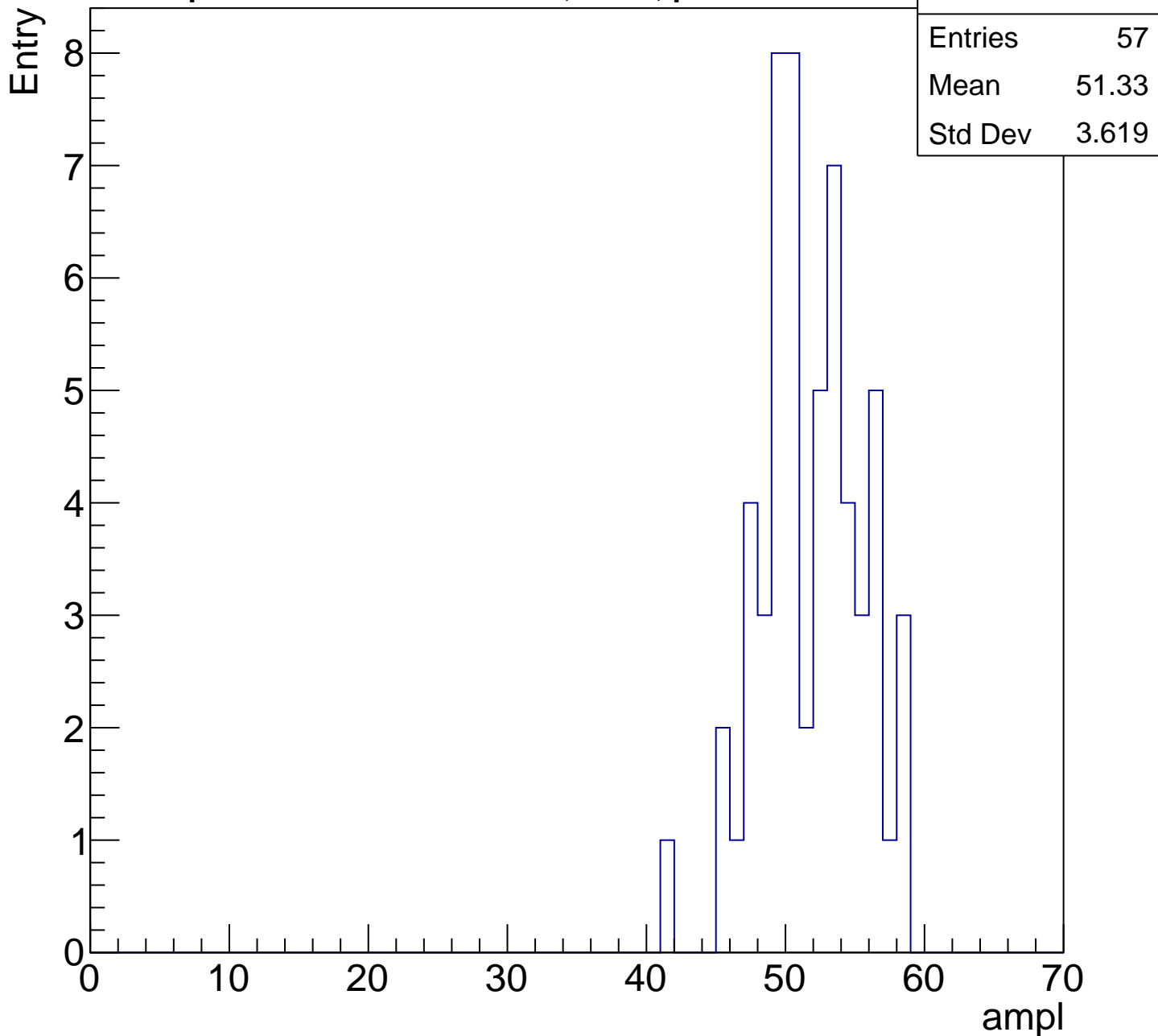
**Gaus mean : 45.0200**

**Gaus Width: 2.8177**



# B0L001S, U5-ch73, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

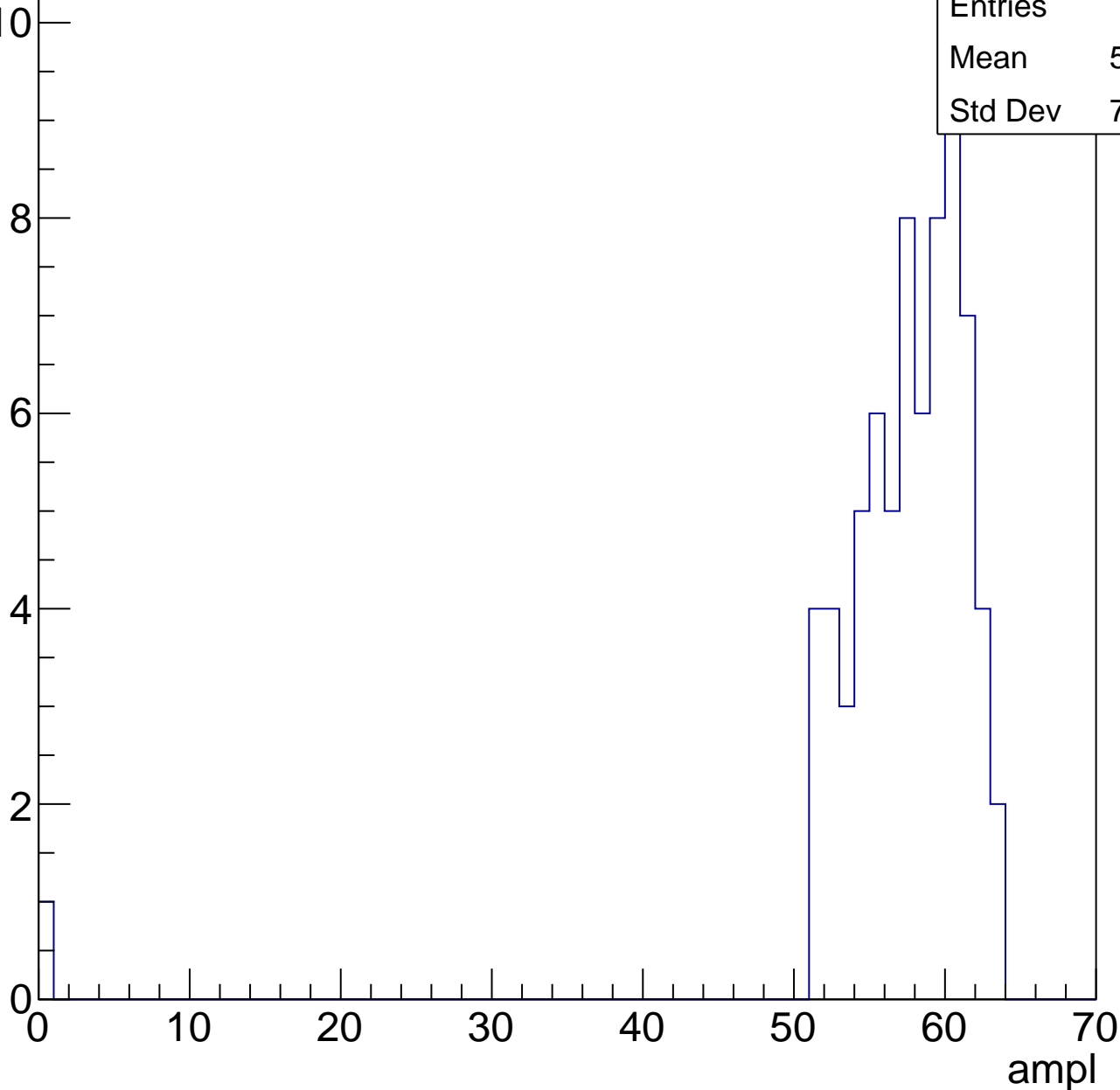


# B0L001S, U5-ch73, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	56.55
Std Dev	7.414

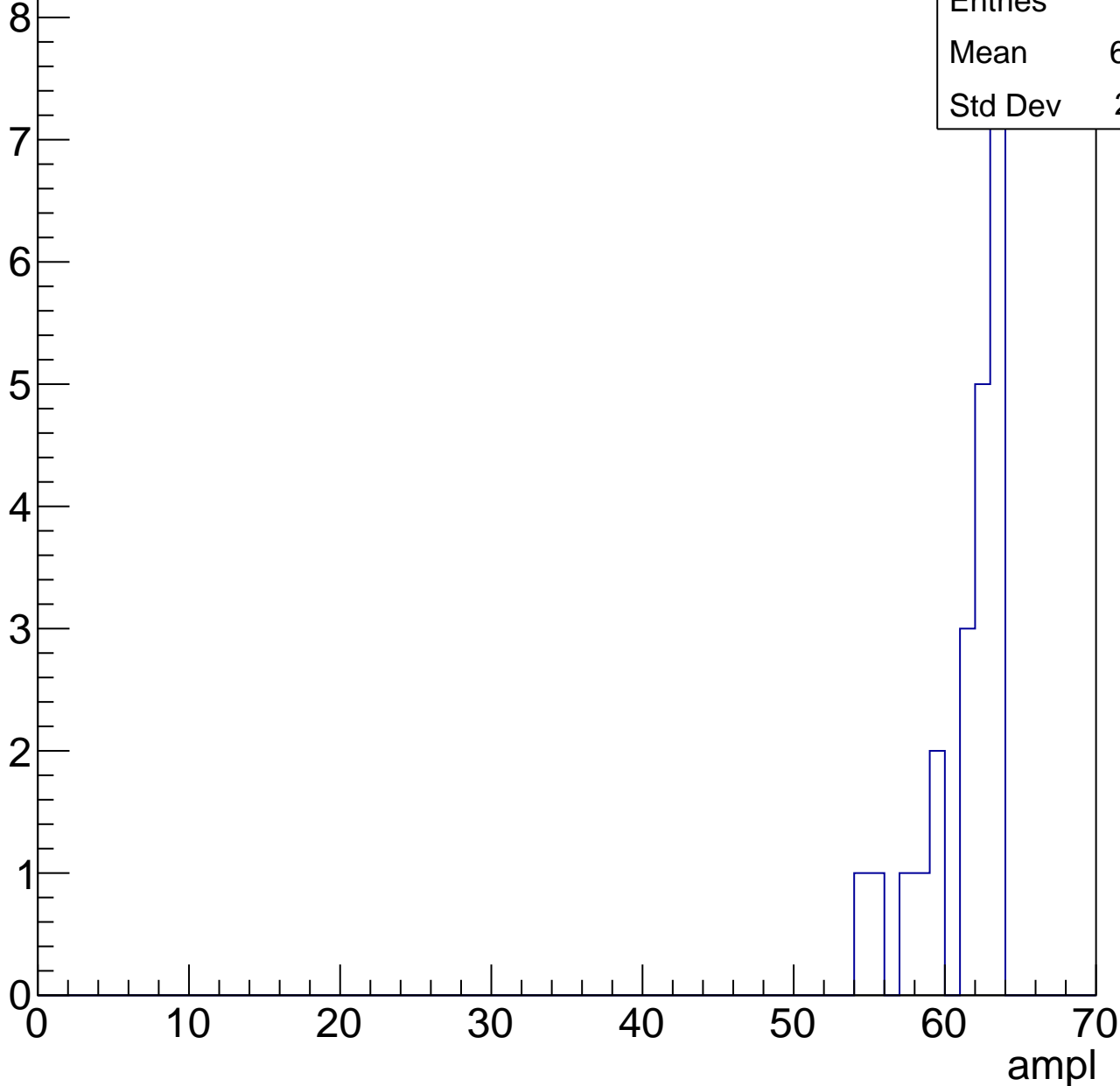


# B0L001S, U5-ch73, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	22
Mean	60.86
Std Dev	2.651



# B0L001S, U5-ch73, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch73, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch74, adc0

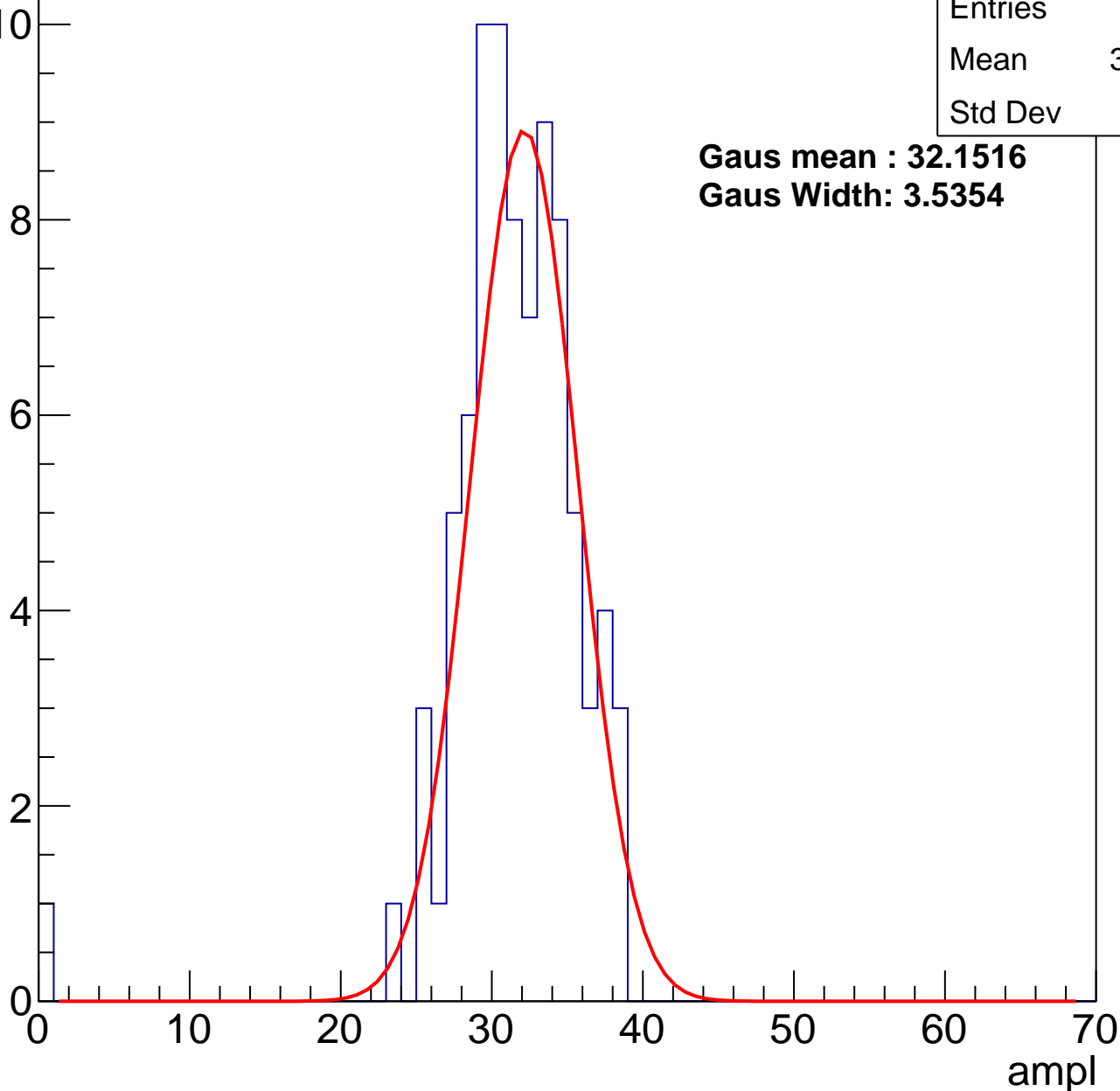
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	84
Mean	30.99
Std Dev	4.76

**Gaus mean : 32.1516**

**Gaus Width: 3.5354**



# B0L001S, U5-ch74, adc1

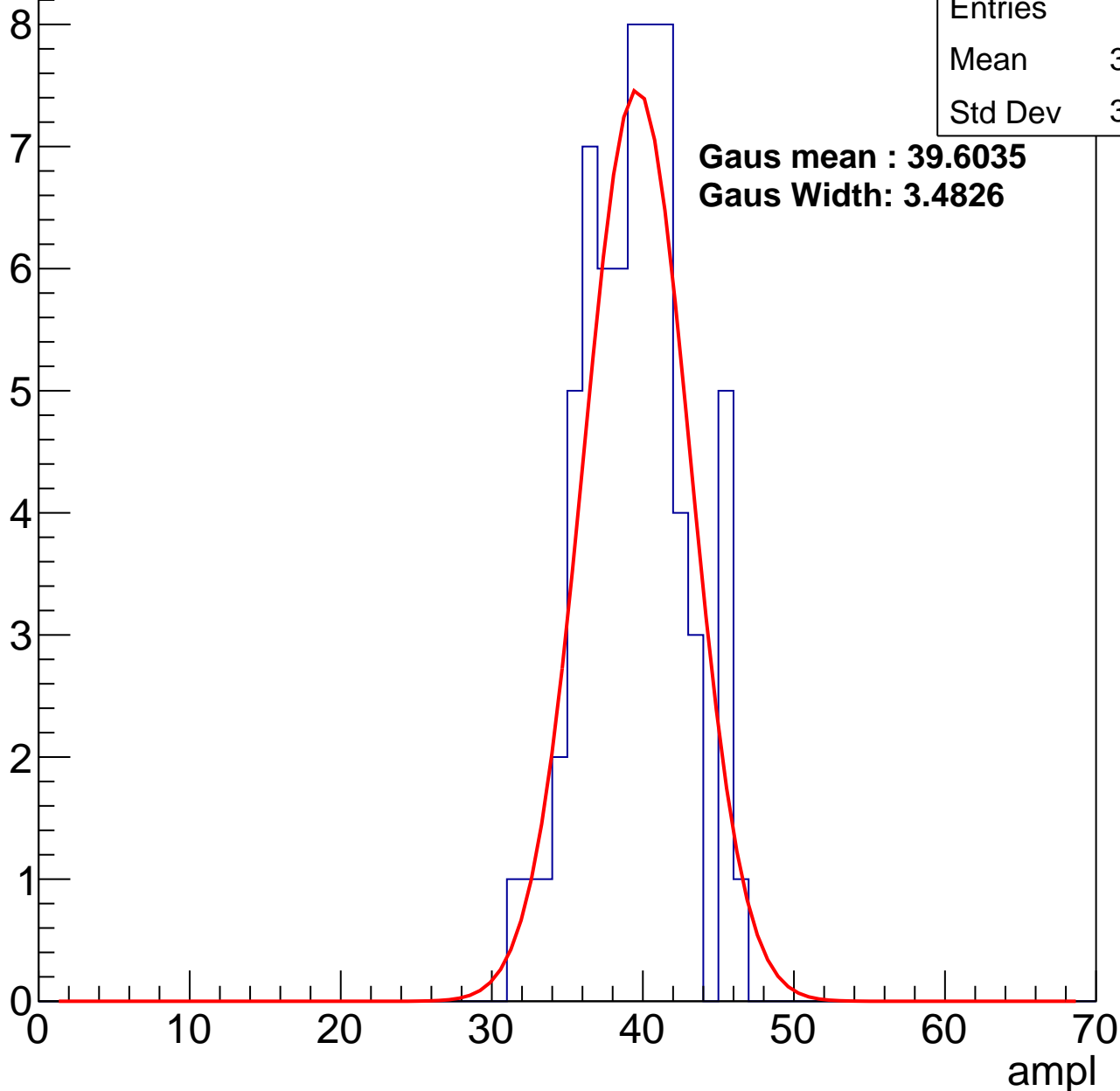
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	38.92
Std Dev	3.313

**Gaus mean : 39.6035**

**Gaus Width: 3.4826**



# B0L001S, U5-ch74, adc2

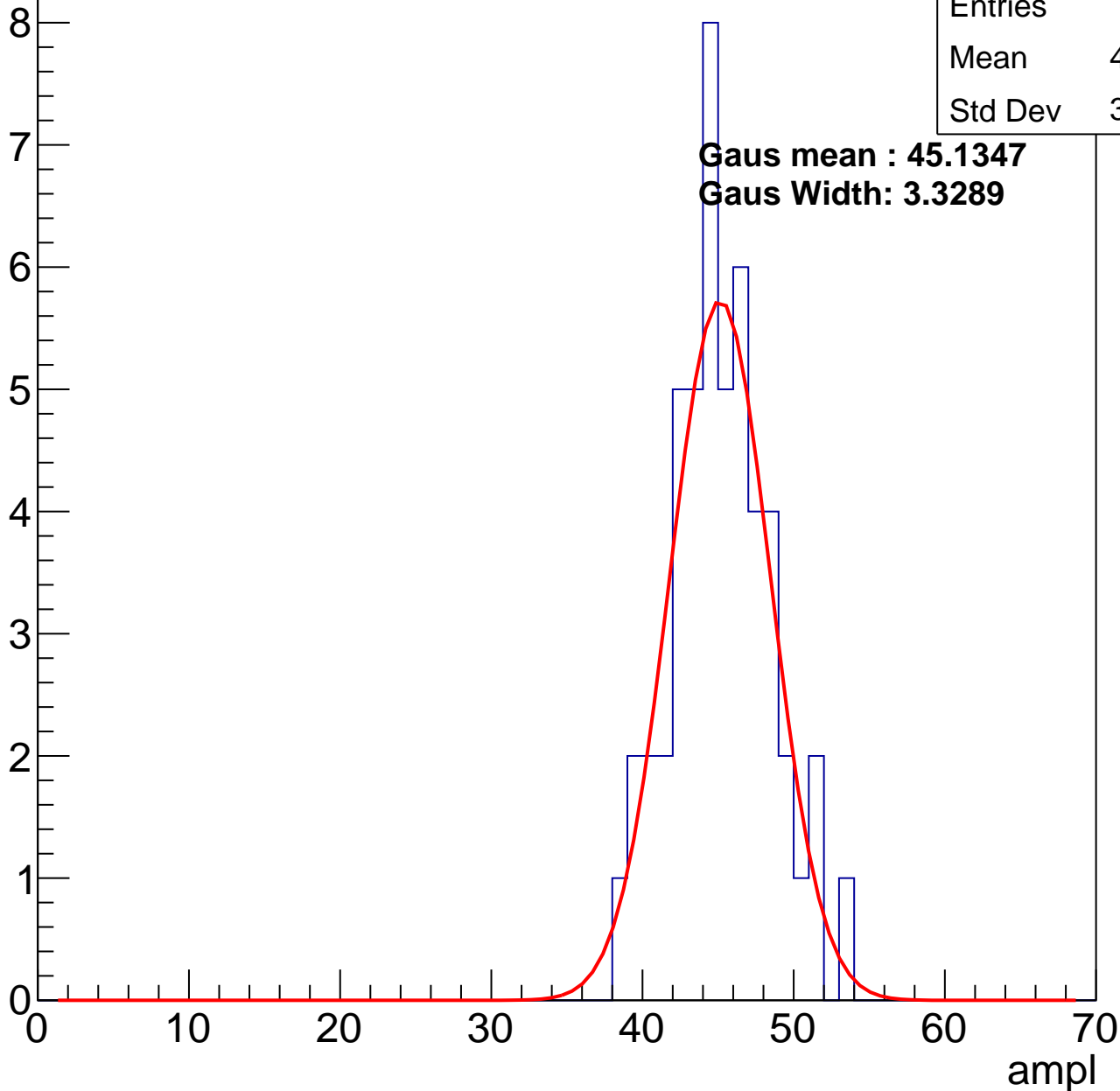
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	50
Mean	44.78
Std Dev	3.239

**Gaus mean : 45.1347**

**Gaus Width: 3.3289**

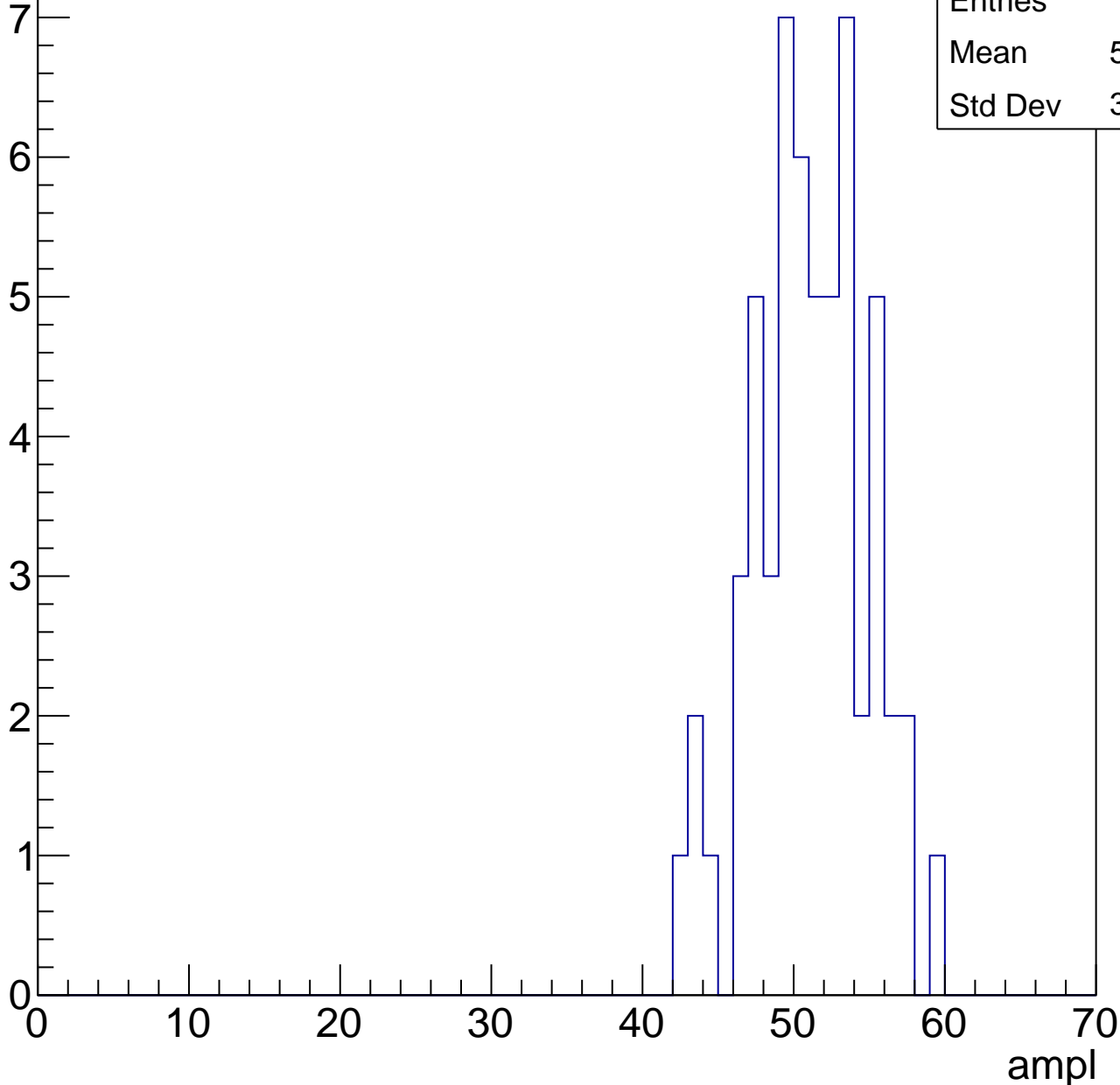


# B0L001S, U5-ch74, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	50.63
Std Dev	3.707



# B0L001S, U5-ch74, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

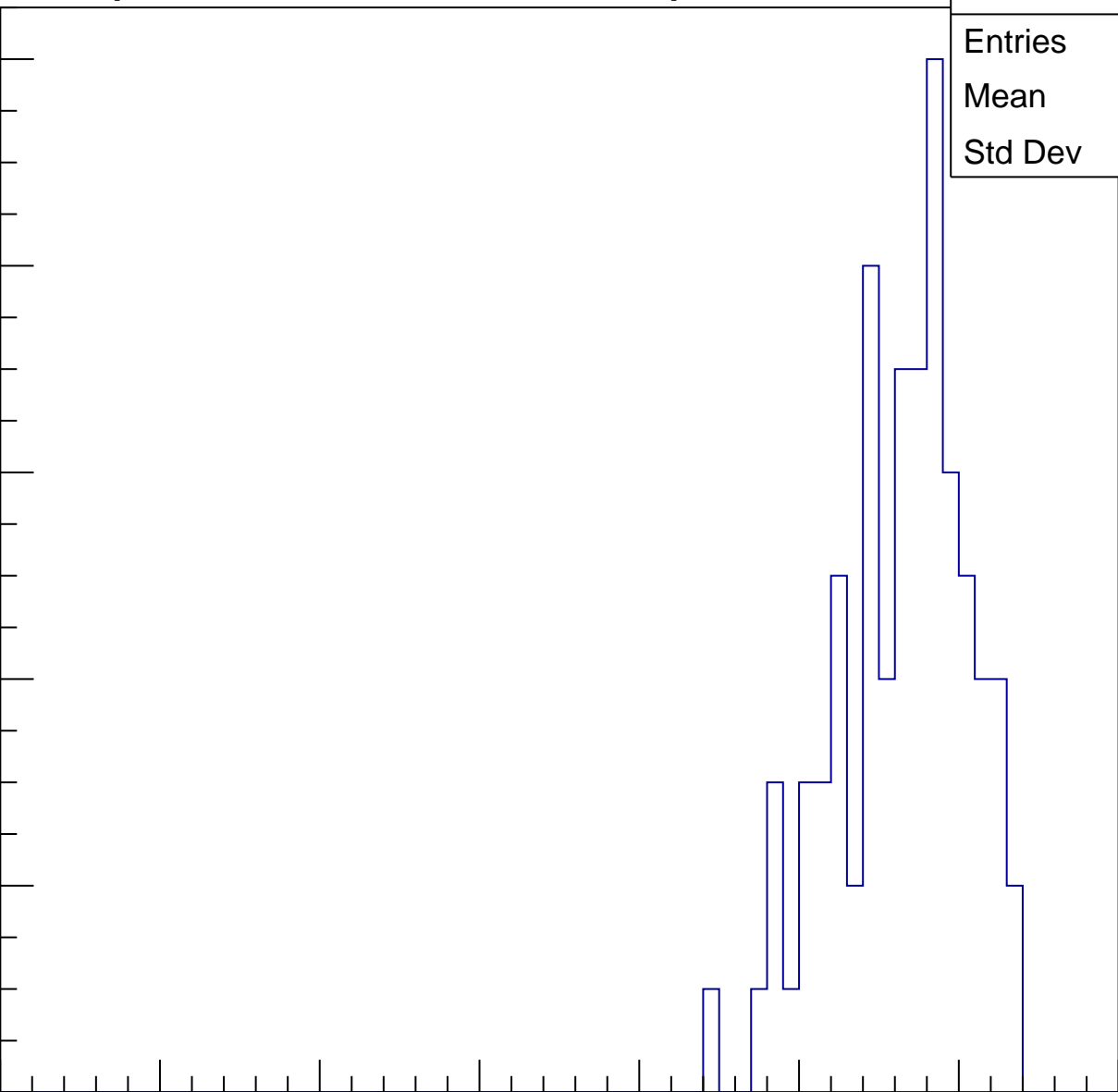
Entries	76
Mean	55.89
Std Dev	4.144

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

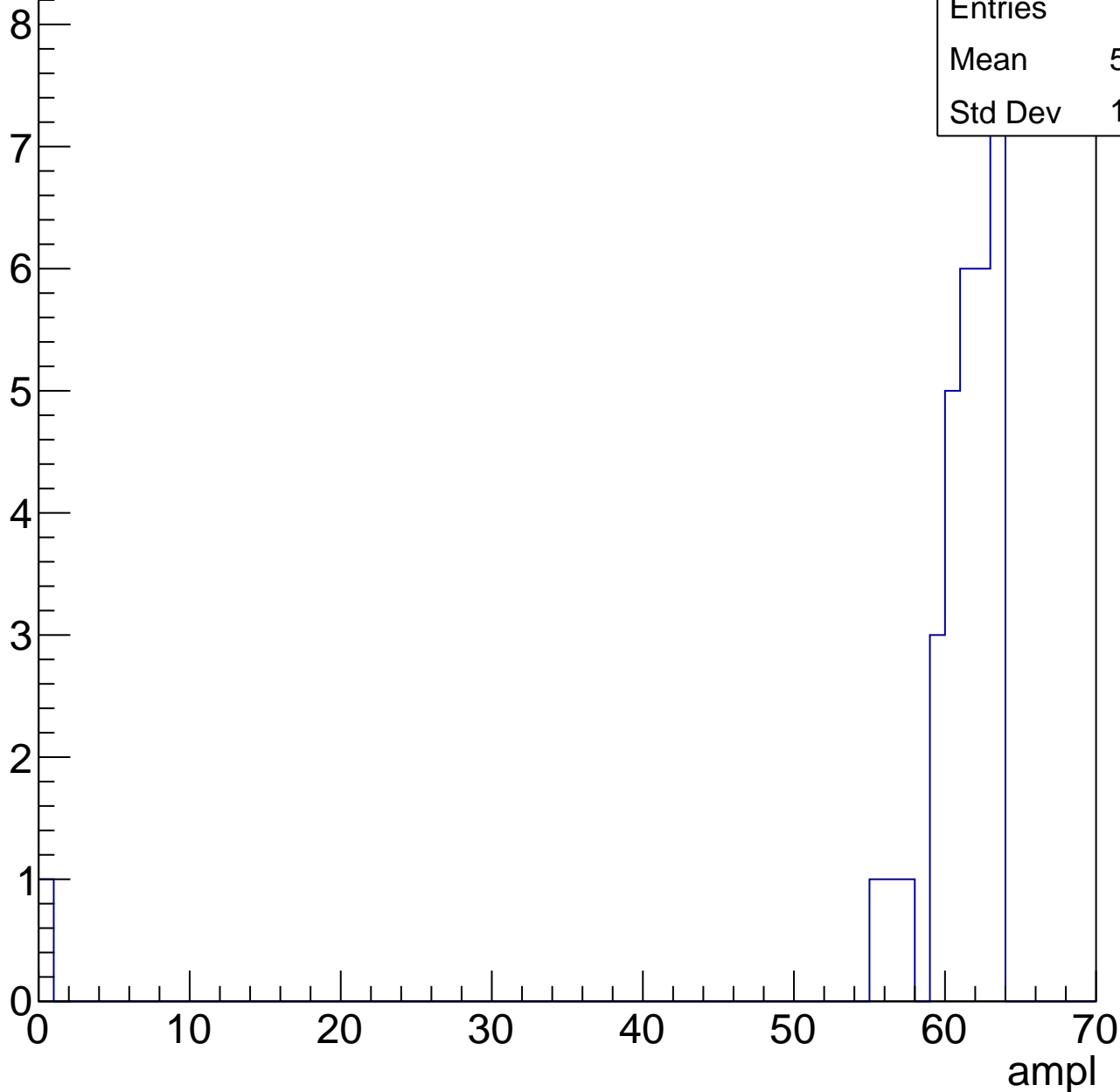


# B0L001S, U5-ch74, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	32
Mean	58.97
Std Dev	10.78



# B0L001S, U5-ch74, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch74, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch75, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	74
Mean	29.73
Std Dev	5.11

**Gaus mean : 31.1936**

**Gaus Width: 3.2531**

Entry

10  
8  
6  
4  
2  
0

ampl

0

10

20

30

40

50

60

70

0

2

4

6

8

10

# B0L001S, U5-ch75, adc1

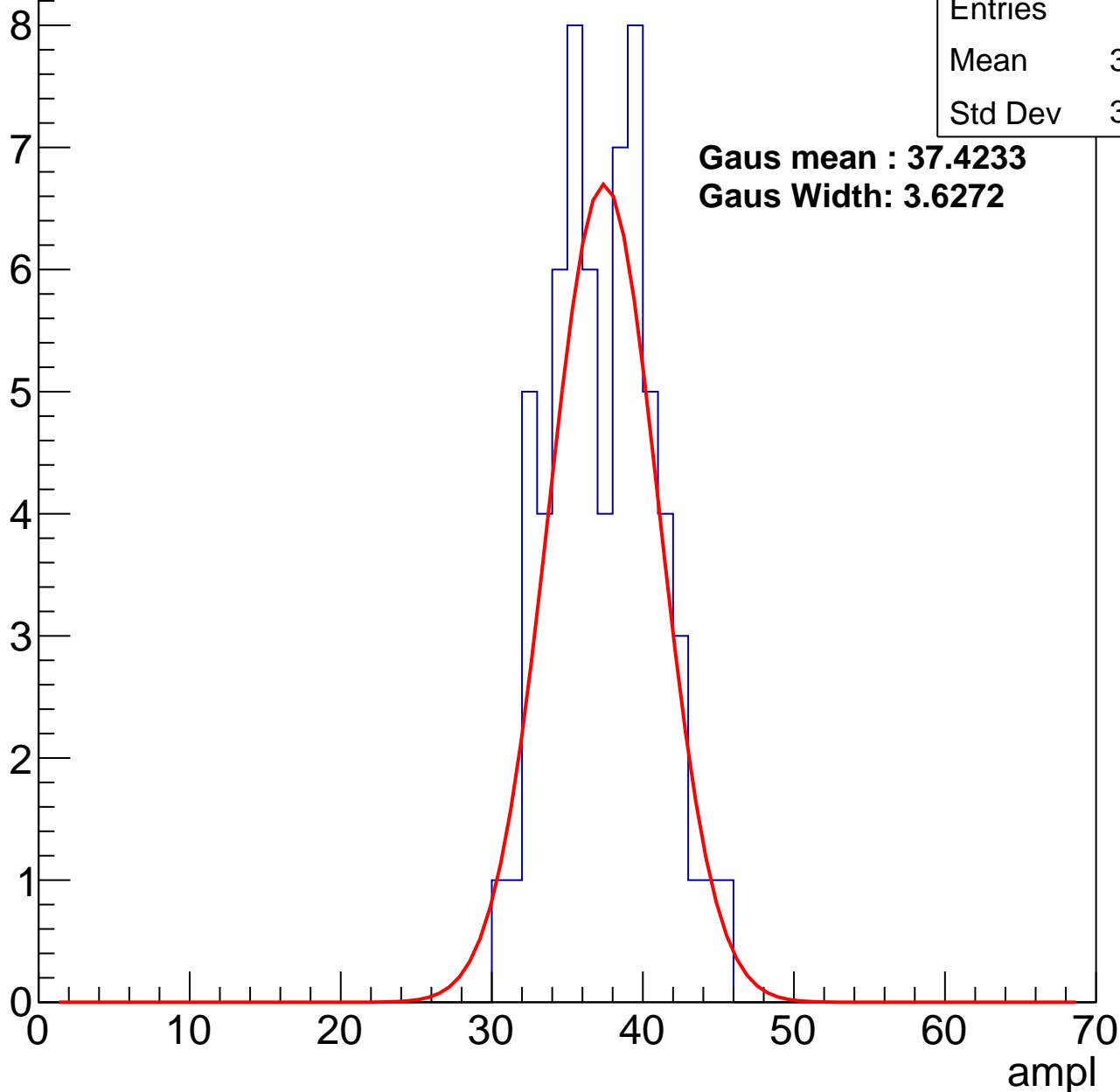
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	36.94
Std Dev	3.369

**Gaus mean : 37.4233**

**Gaus Width: 3.6272**



# B0L001S, U5-ch75, adc2

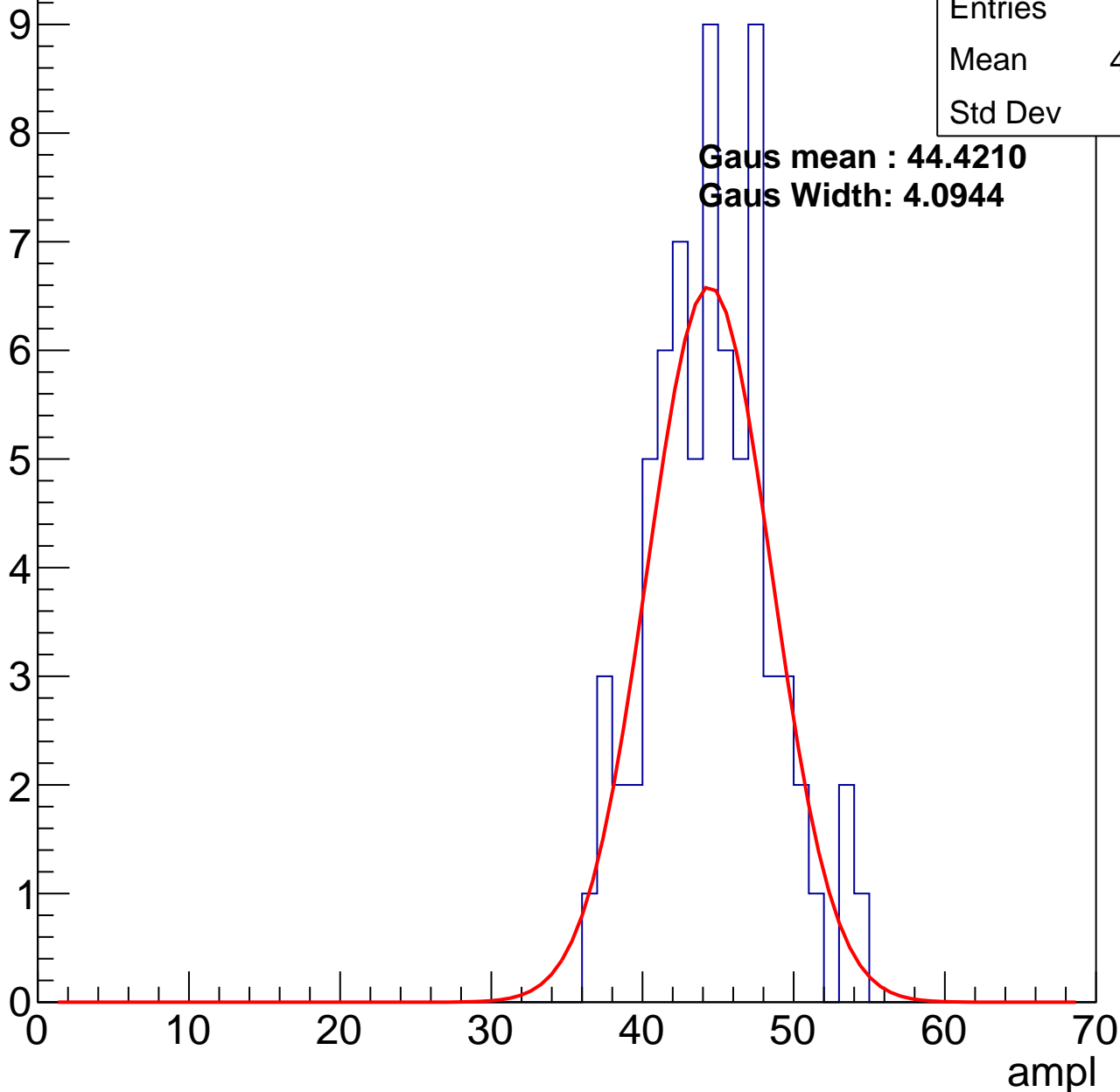
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	44.12
Std Dev	3.93

**Gaus mean : 44.4210**

**Gaus Width: 4.0944**

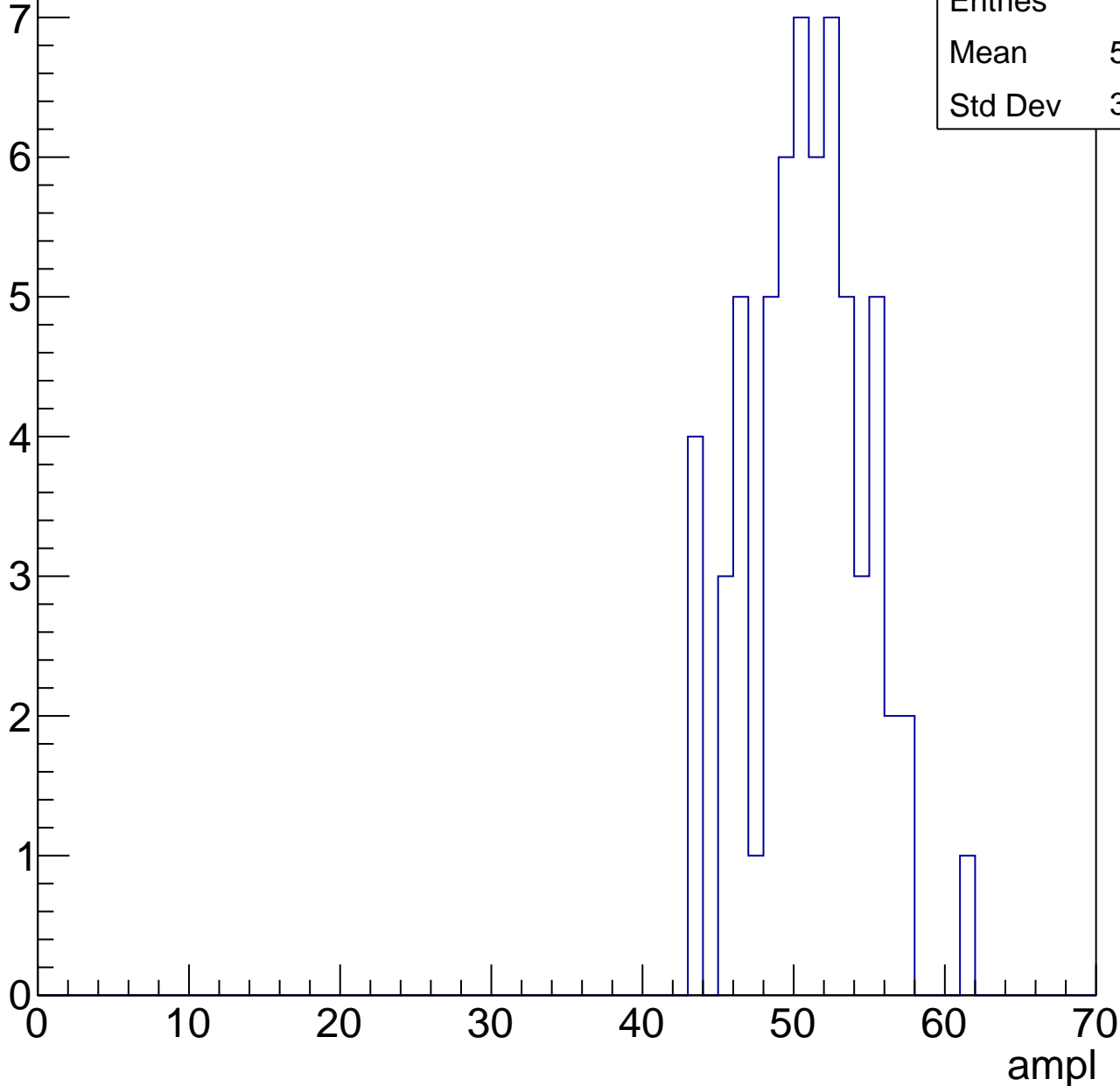


# B0L001S, U5-ch75, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

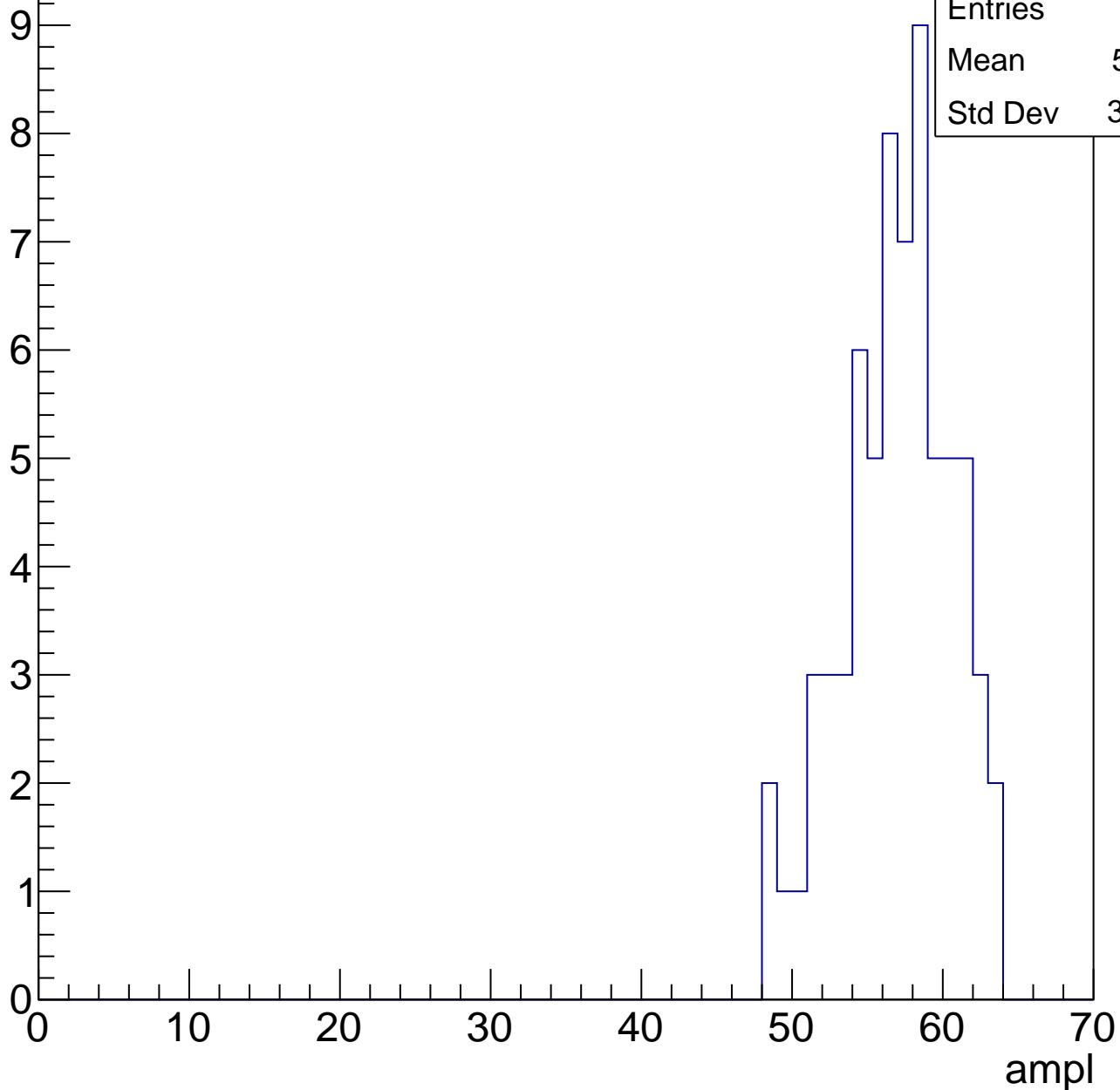
Entries	62
Mean	50.44
Std Dev	3.846



# B0L001S, U5-ch75, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



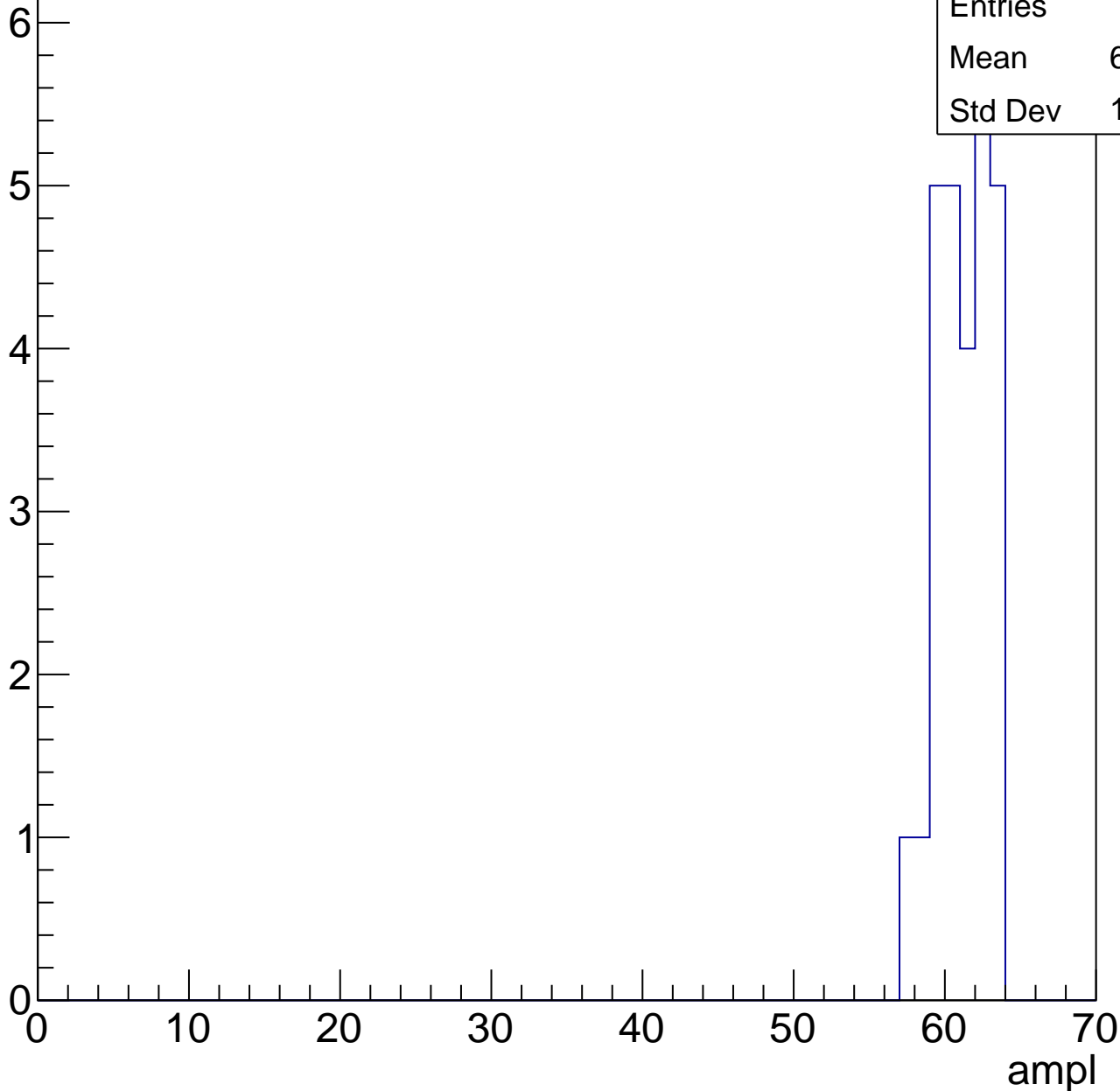
Entries	68
Mean	56.51
Std Dev	3.583

# B0L001S, U5-ch75, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	27
Mean	60.78
Std Dev	1.663



# B0L001S, U5-ch75, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch75, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U5-ch76, adc0

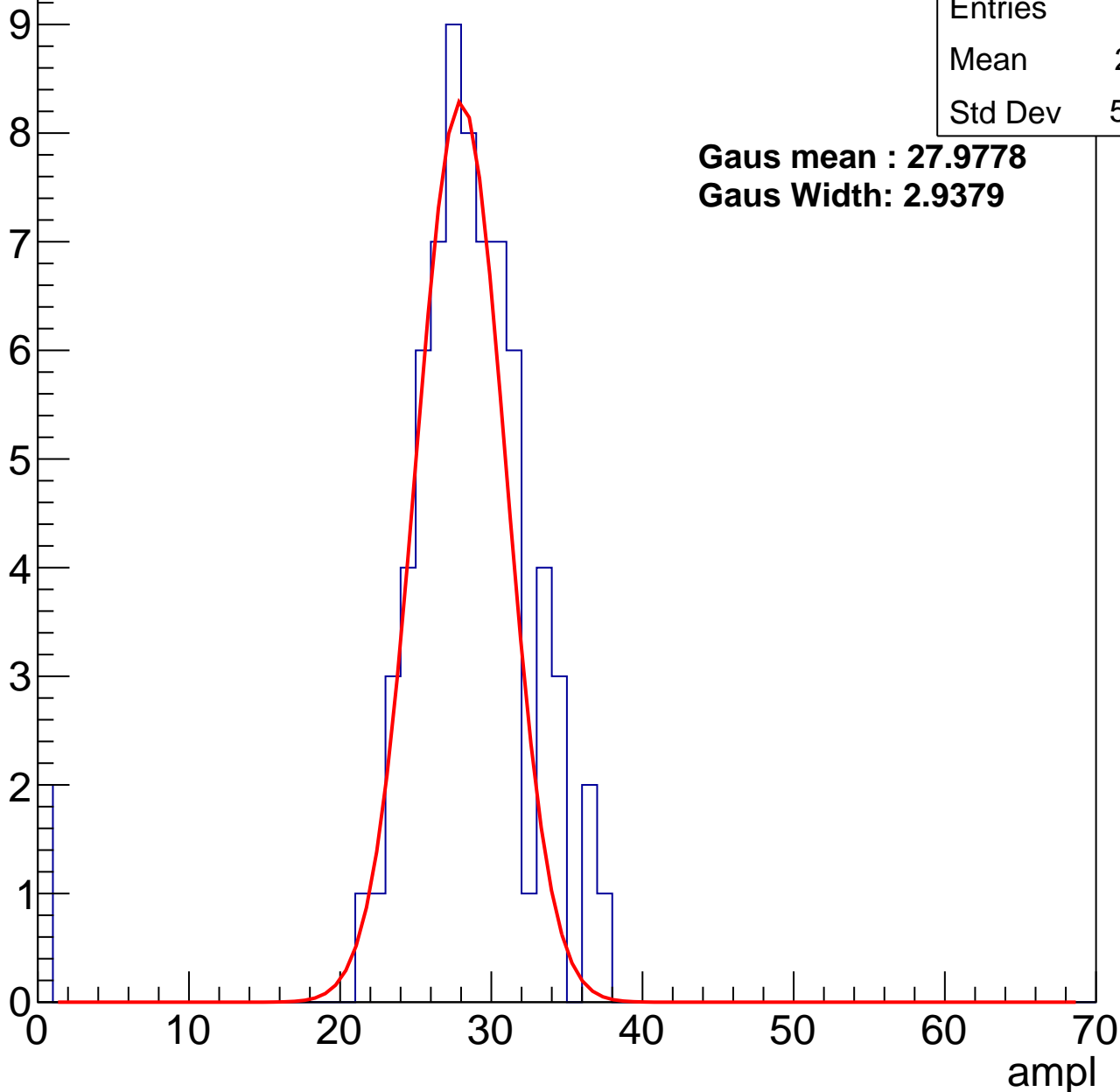
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	27.51
Std Dev	5.759

**Gaus mean : 27.9778**

**Gaus Width: 2.9379**



# B0L001S, U5-ch76, adc1

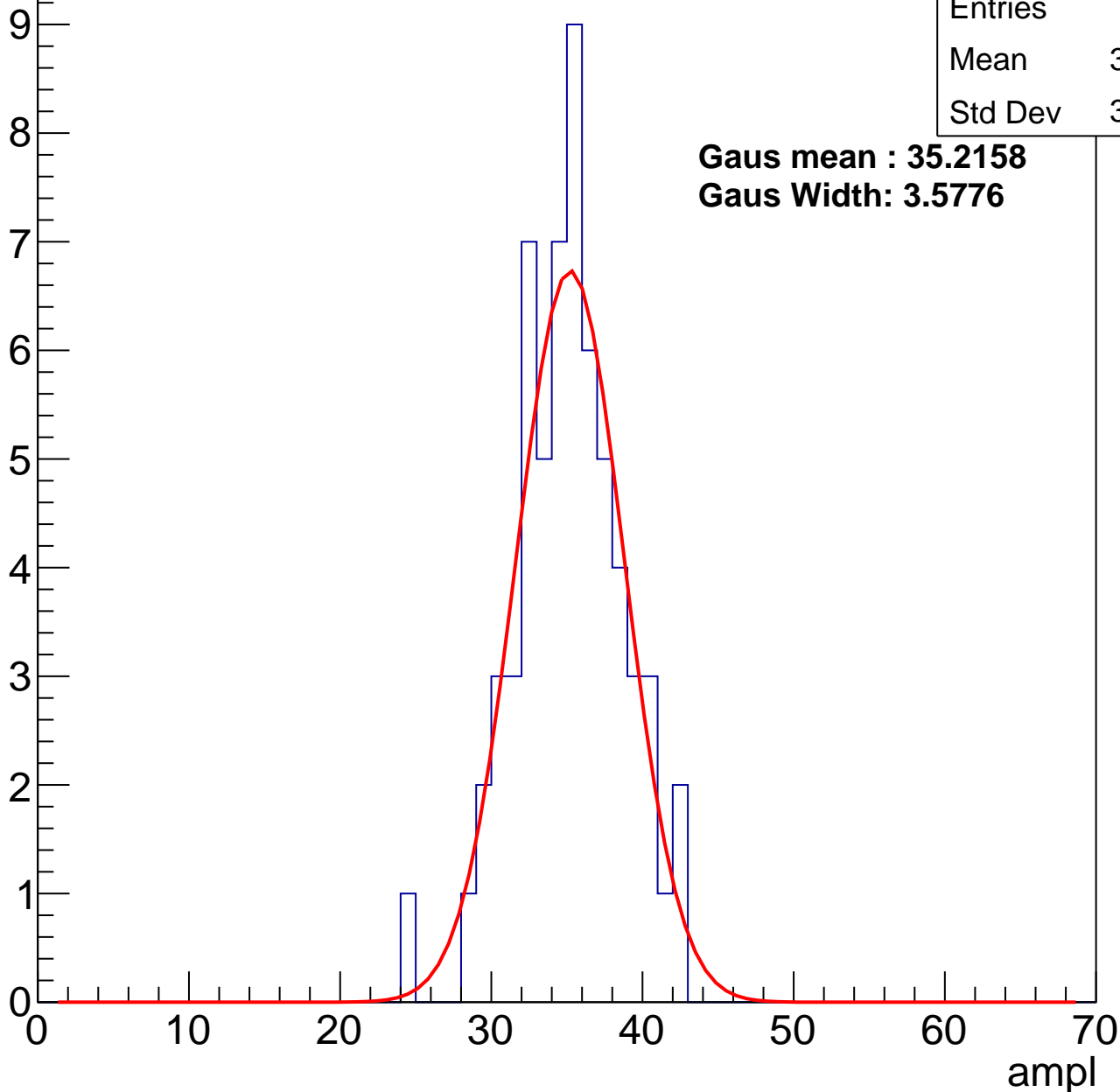
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	34.68
Std Dev	3.518

**Gaus mean : 35.2158**

**Gaus Width: 3.5776**



# B0L001S, U5-ch76, adc2

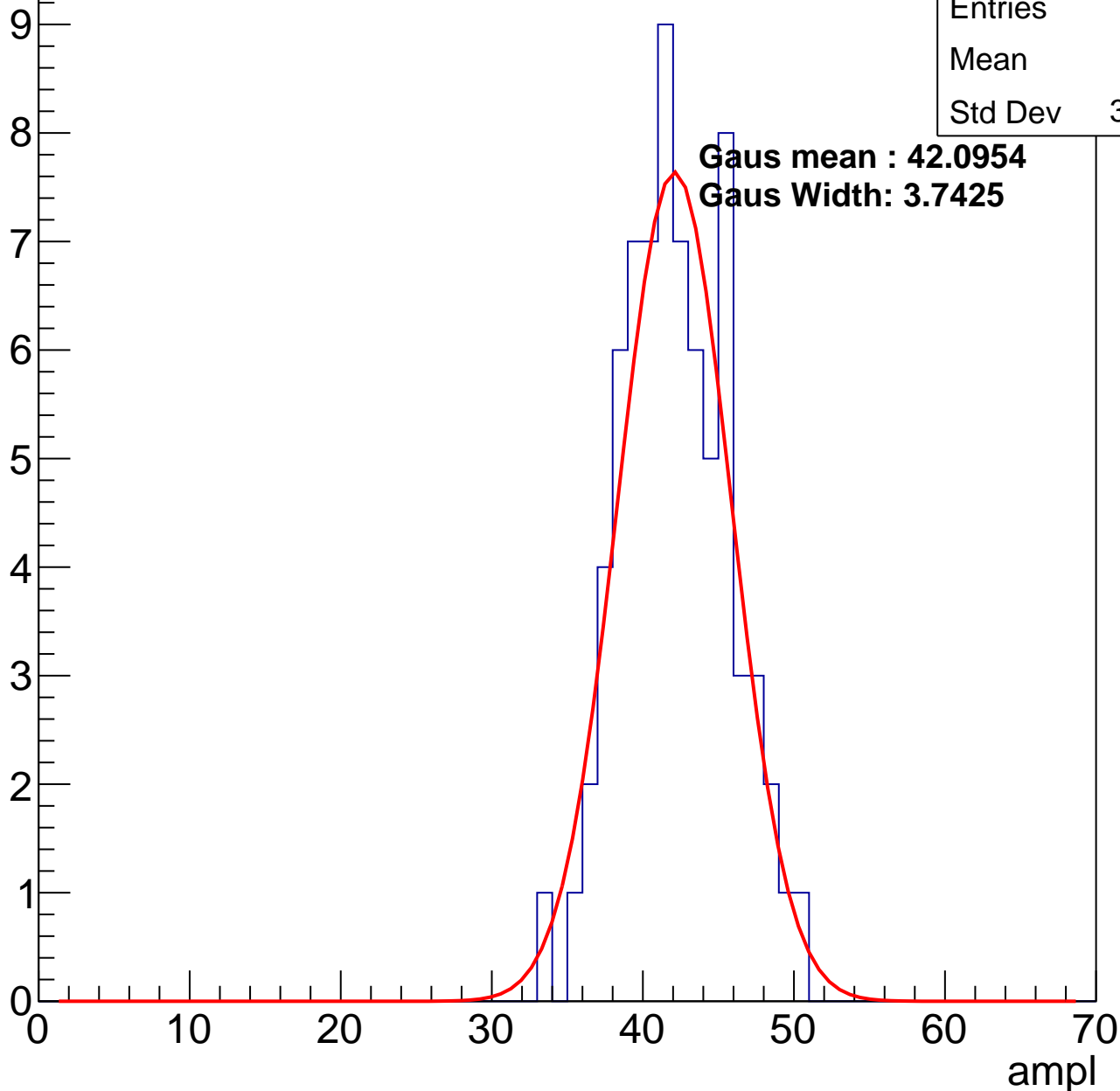
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	41.7
Std Dev	3.506

**Gaus mean : 42.0954**

**Gaus Width: 3.7425**

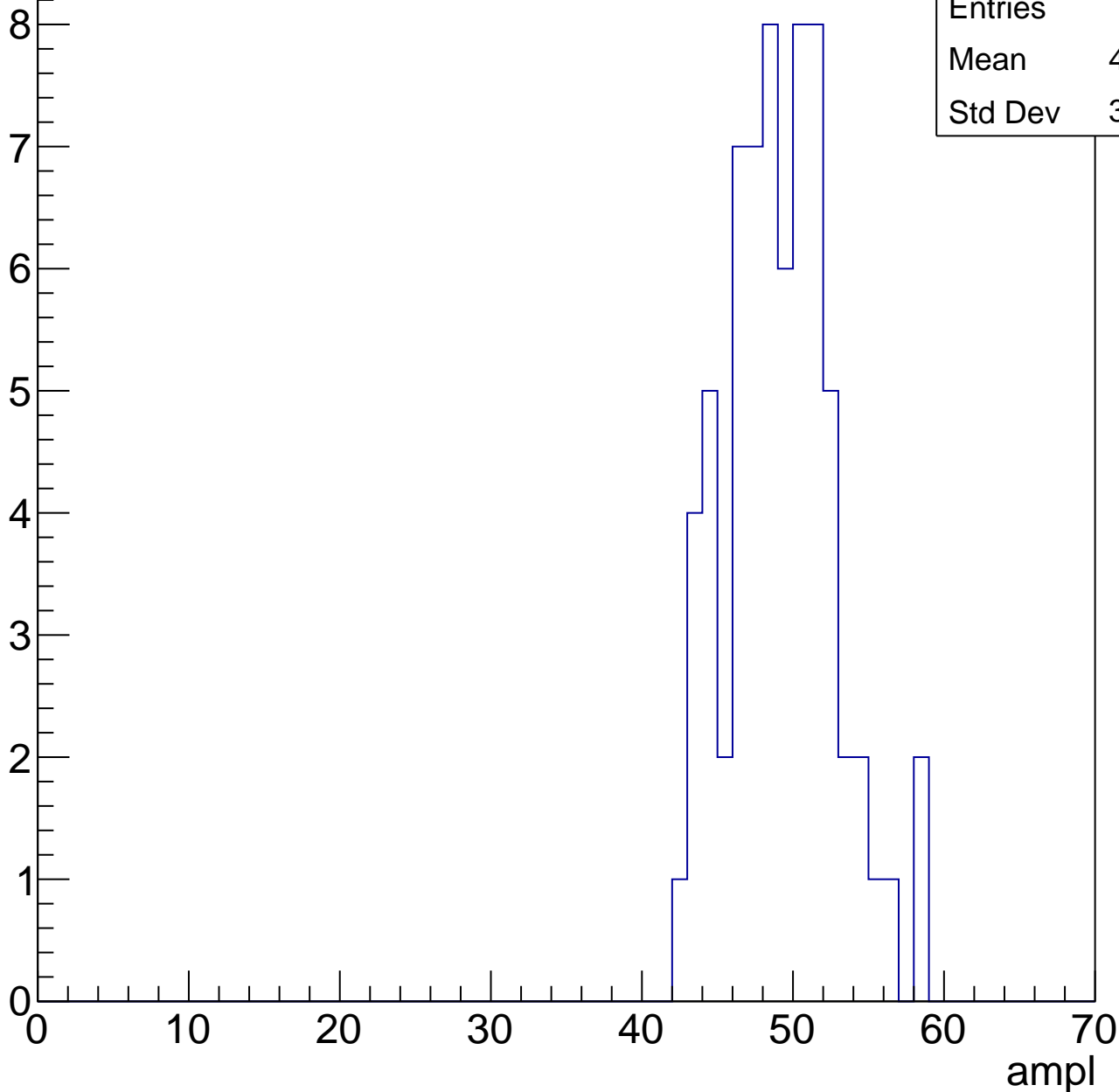


# B0L001S, U5-ch76, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	48.72
Std Dev	3.526

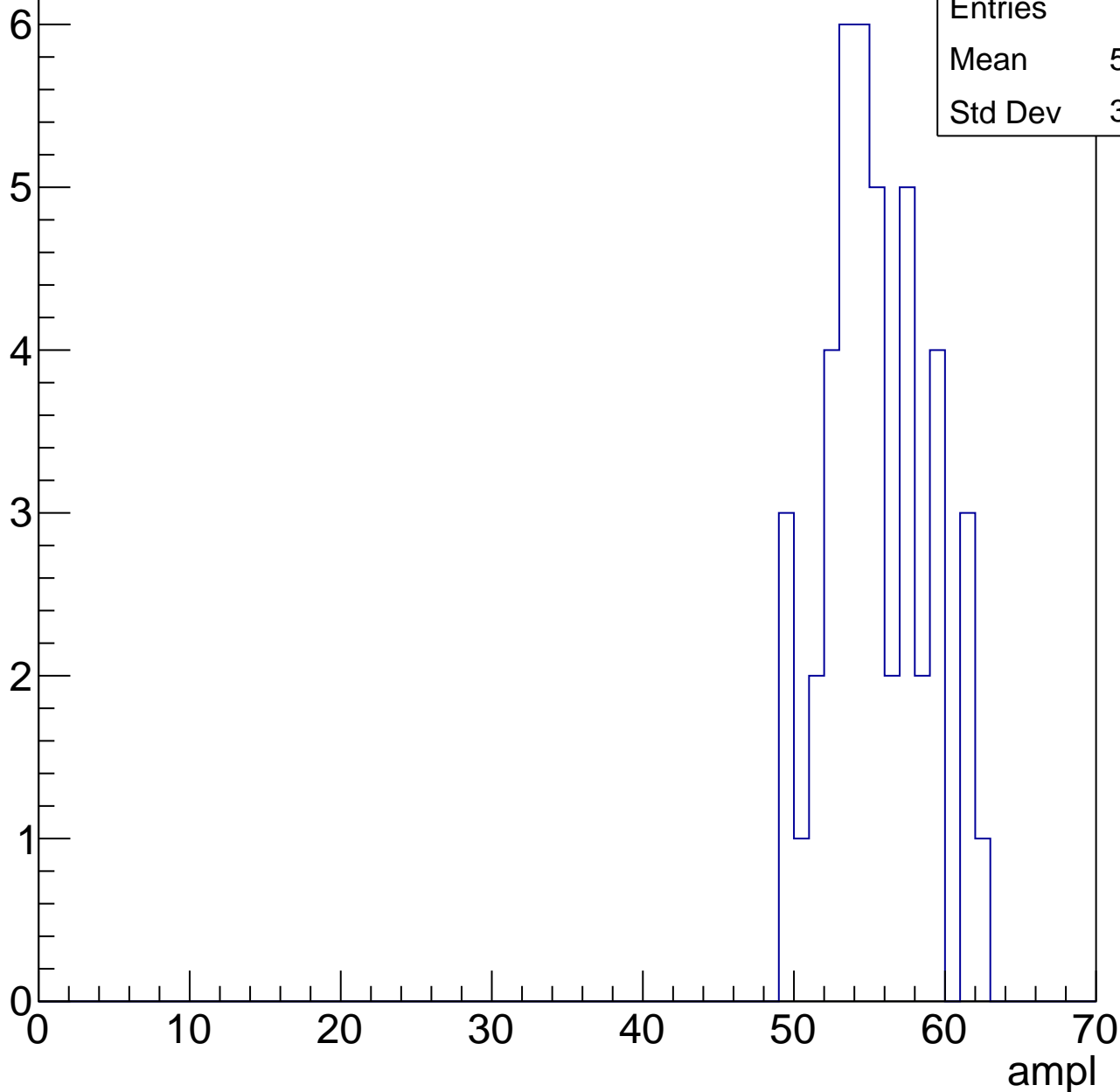


# B0L001S, U5-ch76, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

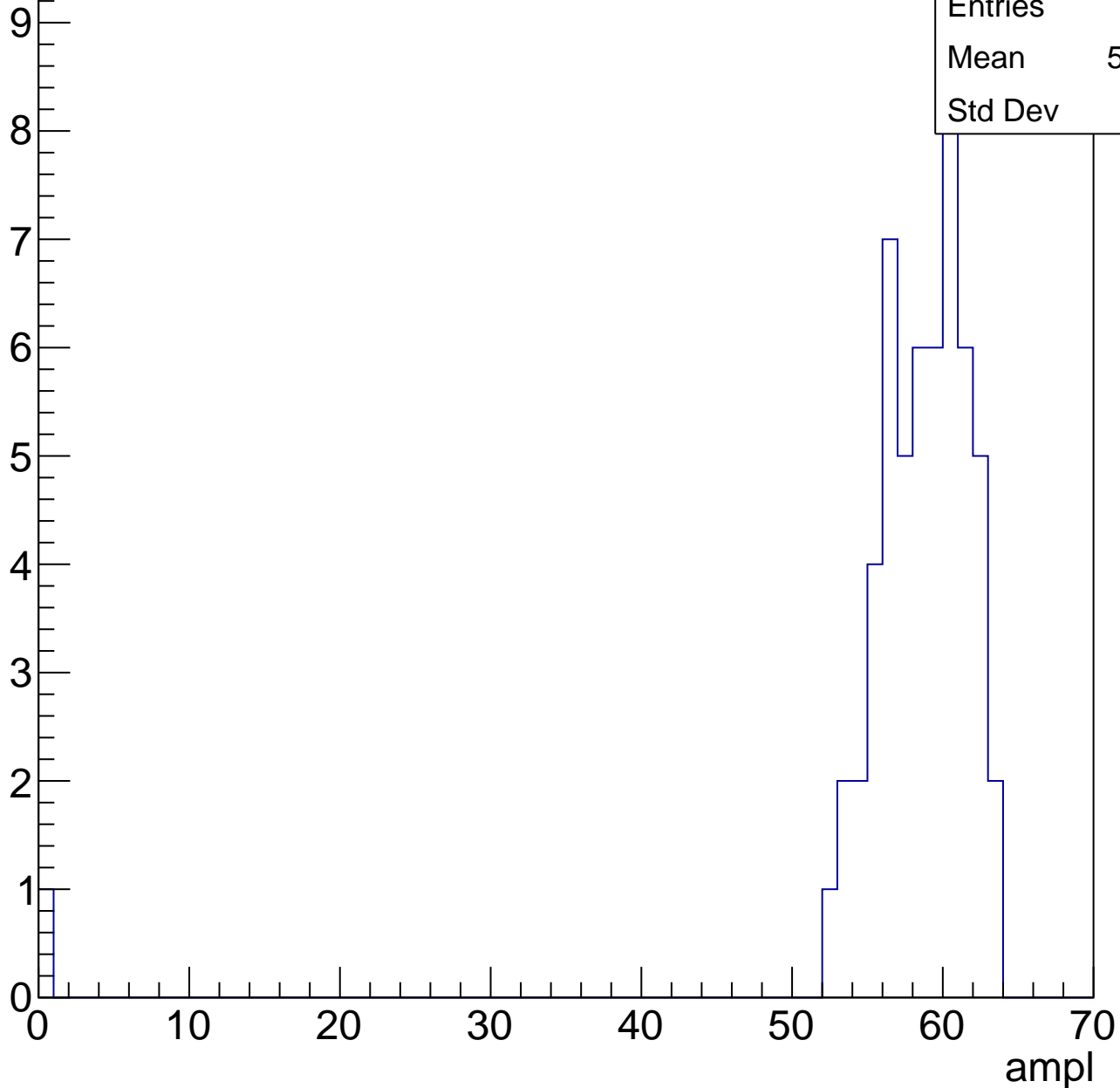
Entries	44
Mean	54.95
Std Dev	3.344



# B0L001S, U5-ch76, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

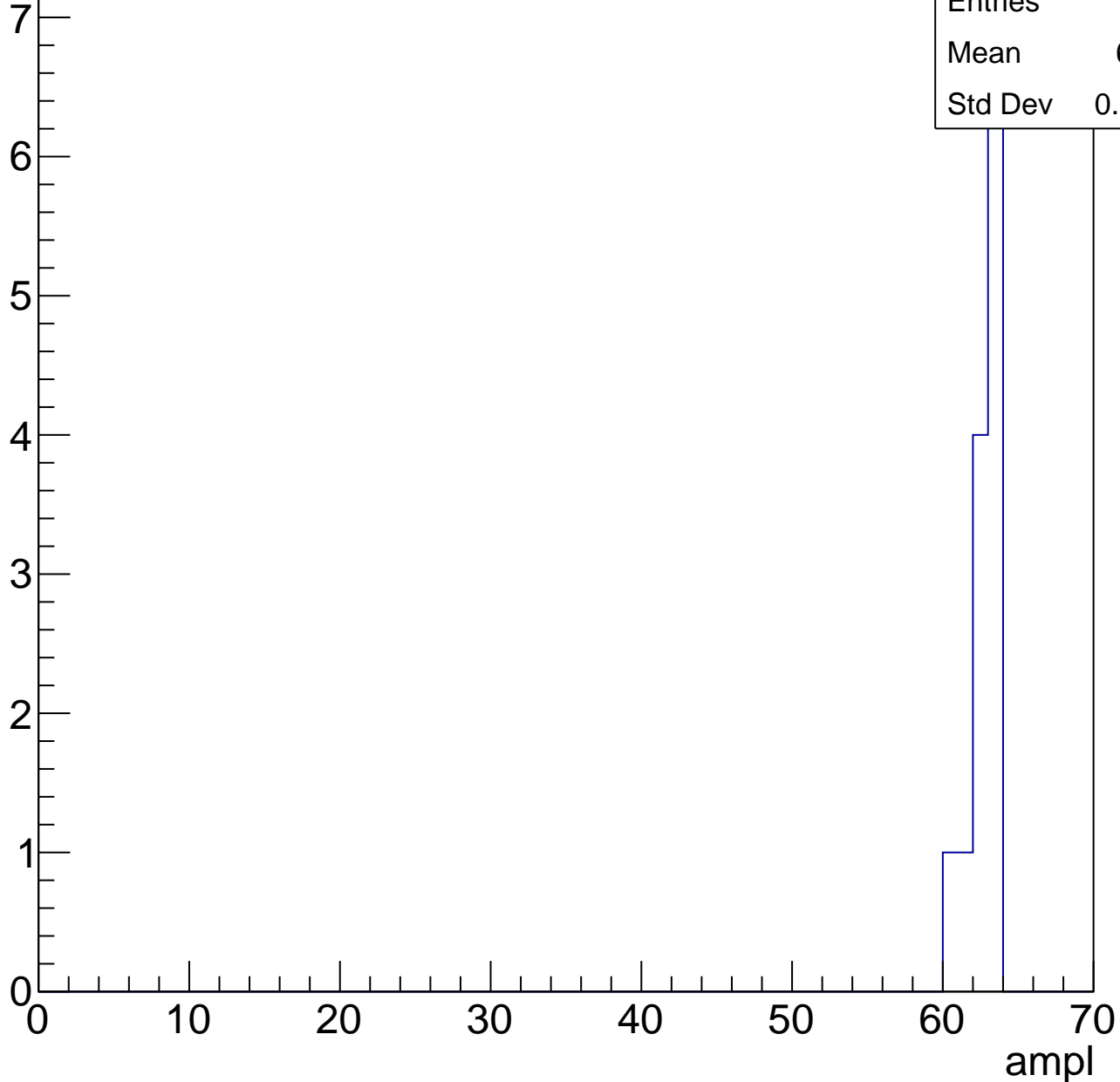
Entry



# B0L001S, U5-ch76, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	13
Mean	62.31
Std Dev	0.9102



# B0L001S, U5-ch76, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch77, adc0

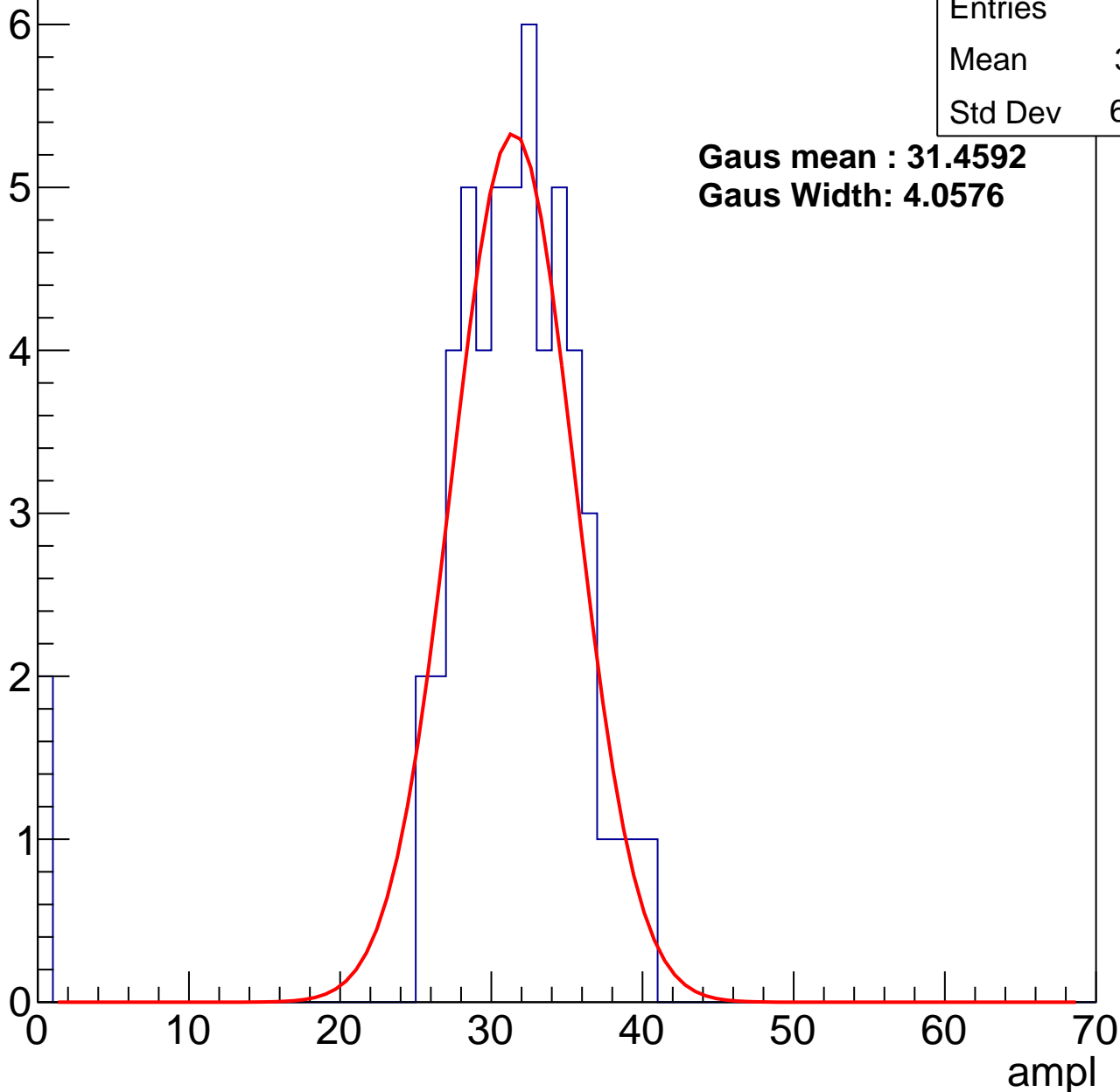
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	30.31
Std Dev	6.854

**Gaus mean : 31.4592**

**Gaus Width: 4.0576**



# B0L001S, U5-ch77, adc1

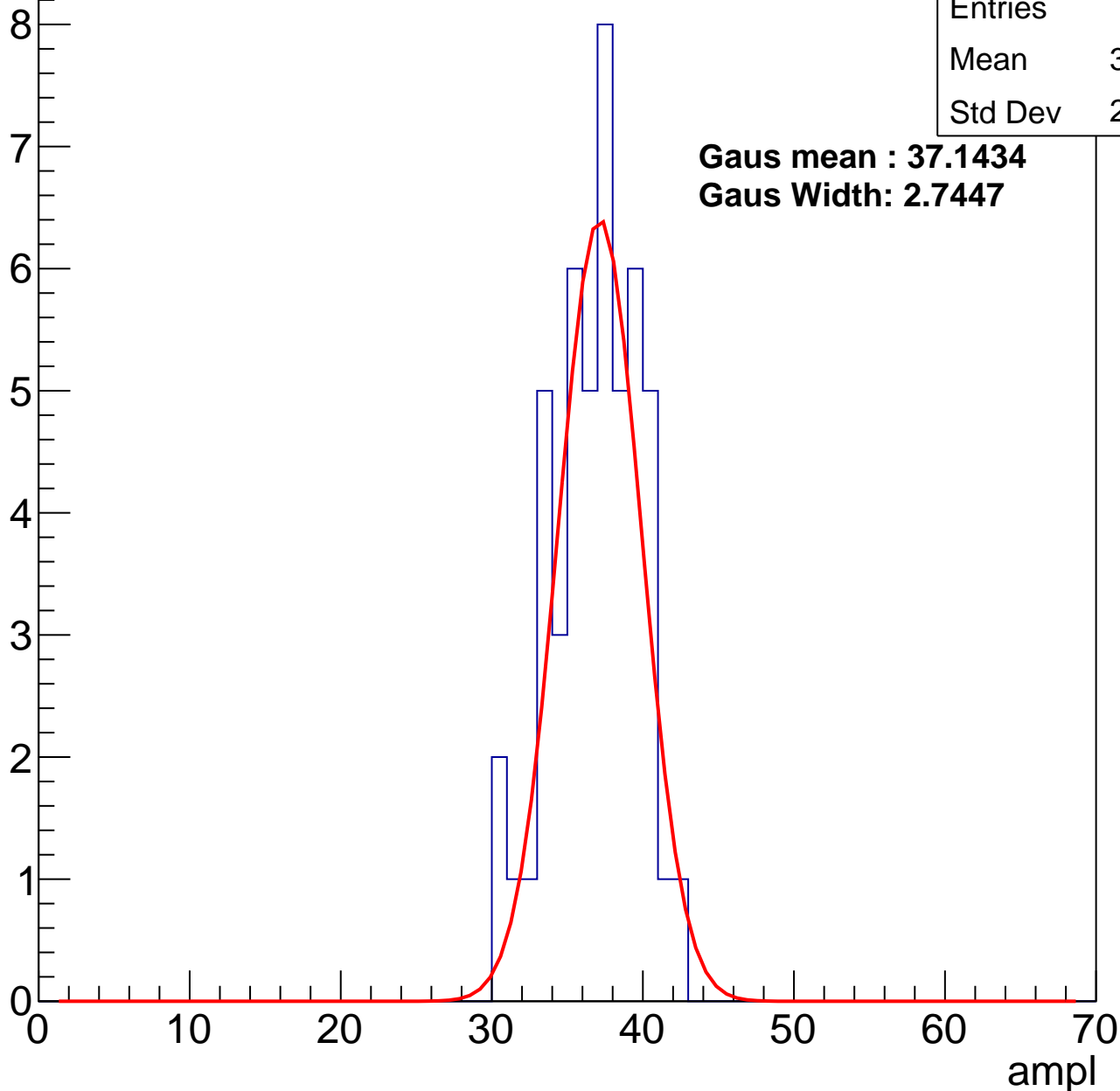
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	49
Mean	36.39
Std Dev	2.827

**Gaus mean : 37.1434**

**Gaus Width: 2.7447**



# B0L001S, U5-ch77, adc2

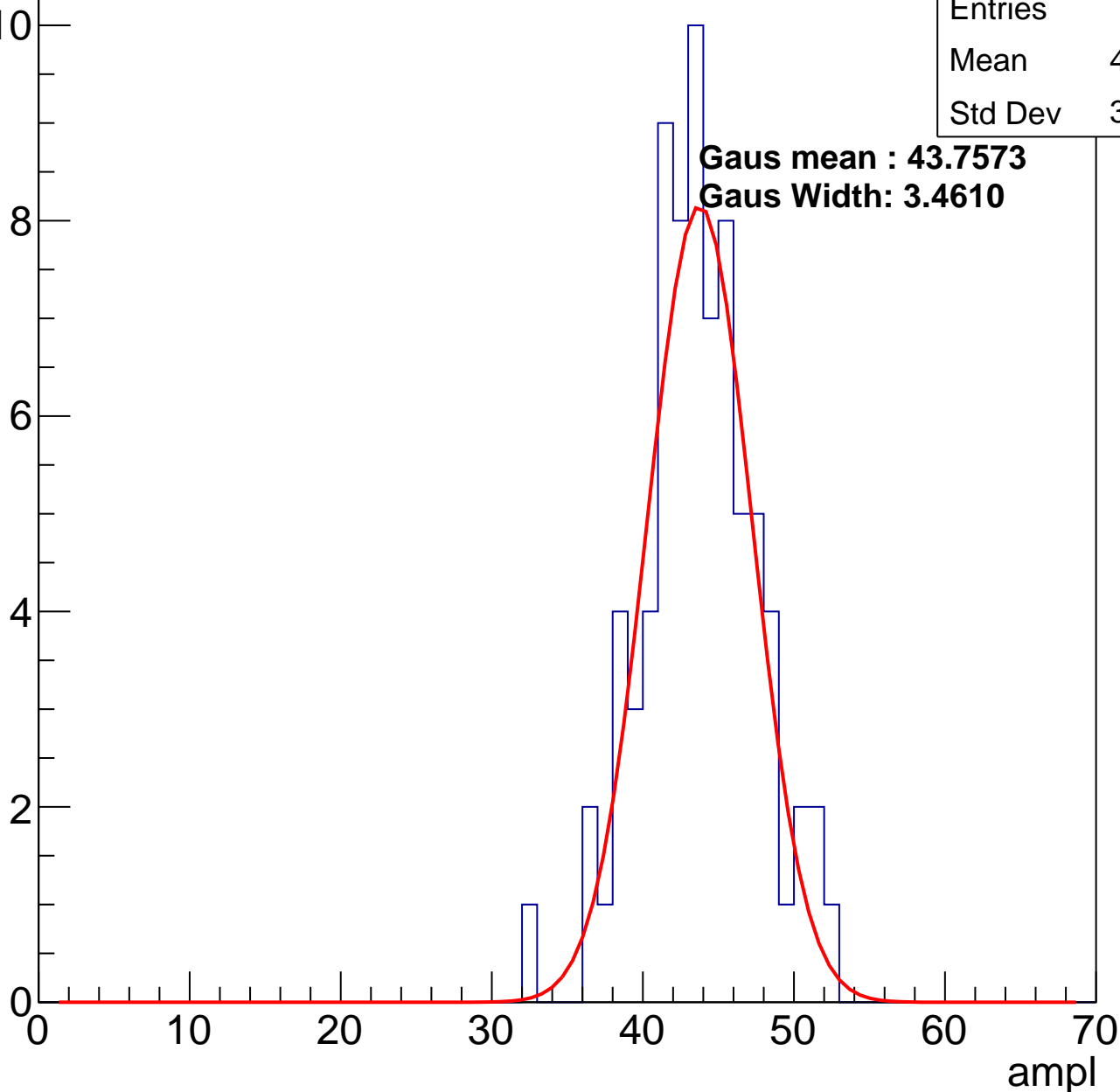
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	77
Mean	43.29
Std Dev	3.752

**Gaus mean : 43.7573**

**Gaus Width: 3.4610**

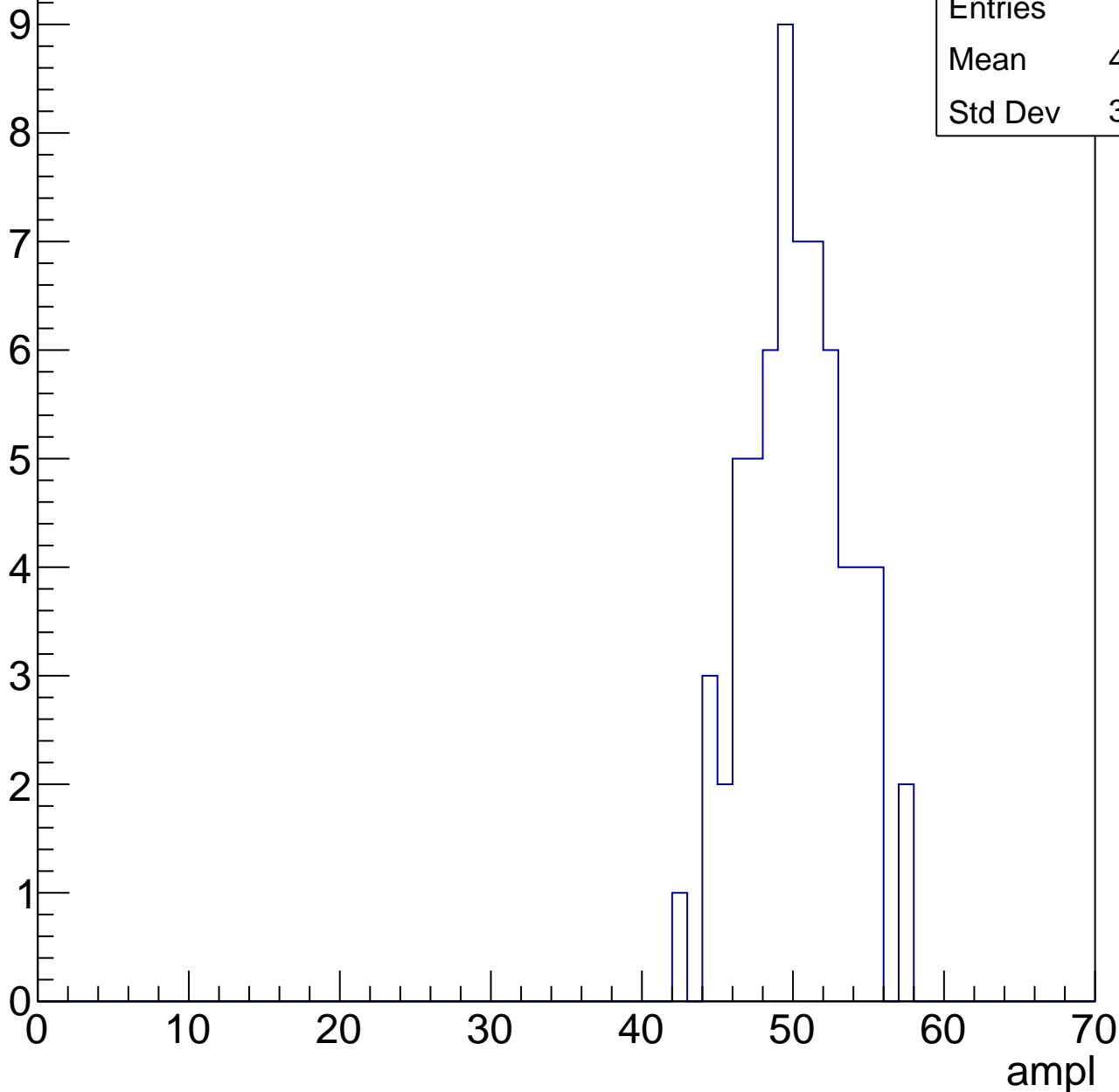


# B0L001S, U5-ch77, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	49.83
Std Dev	3.298

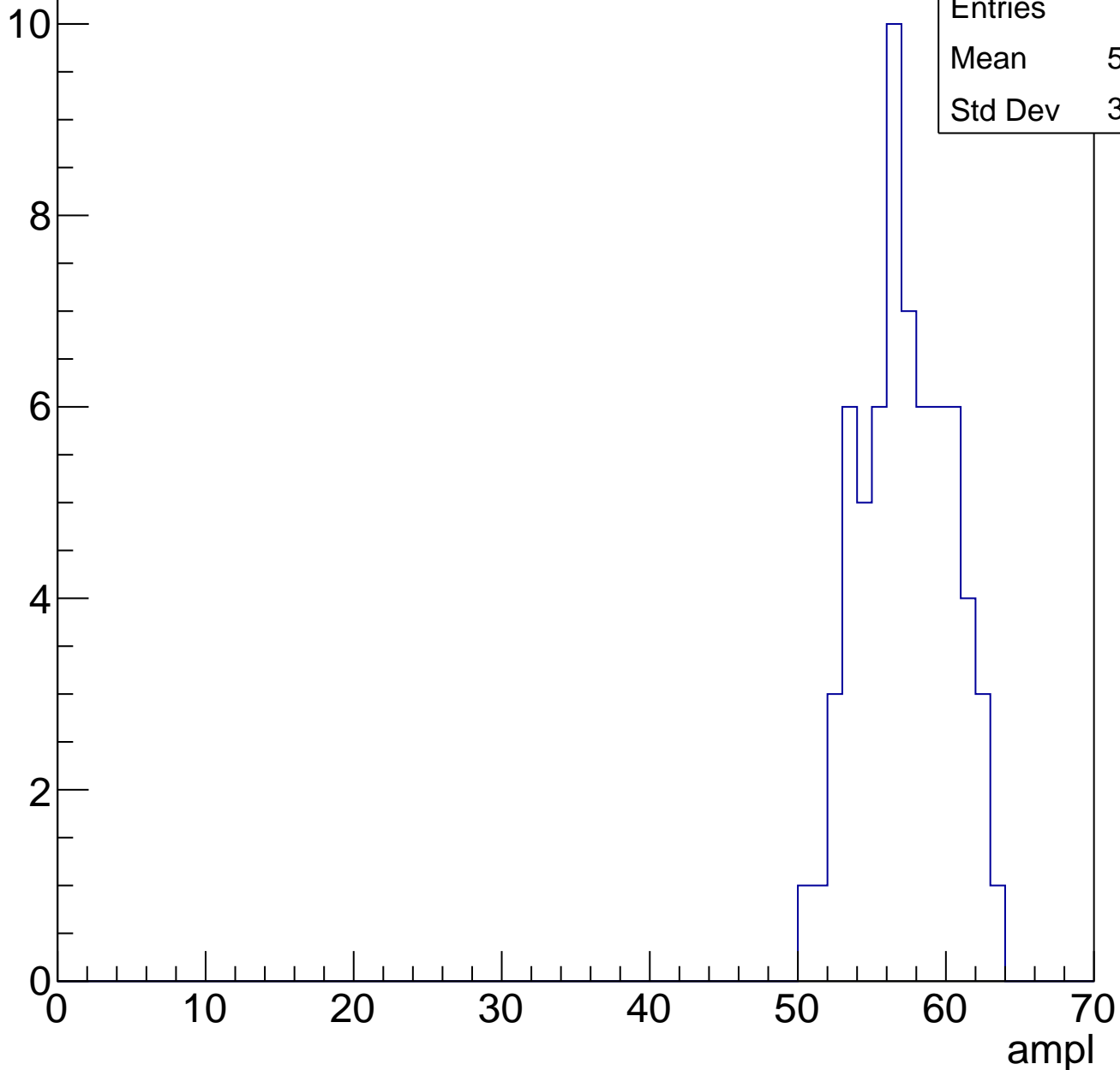


# B0L001S, U5-ch77, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	65
Mean	56.75
Std Dev	3.013

Entry

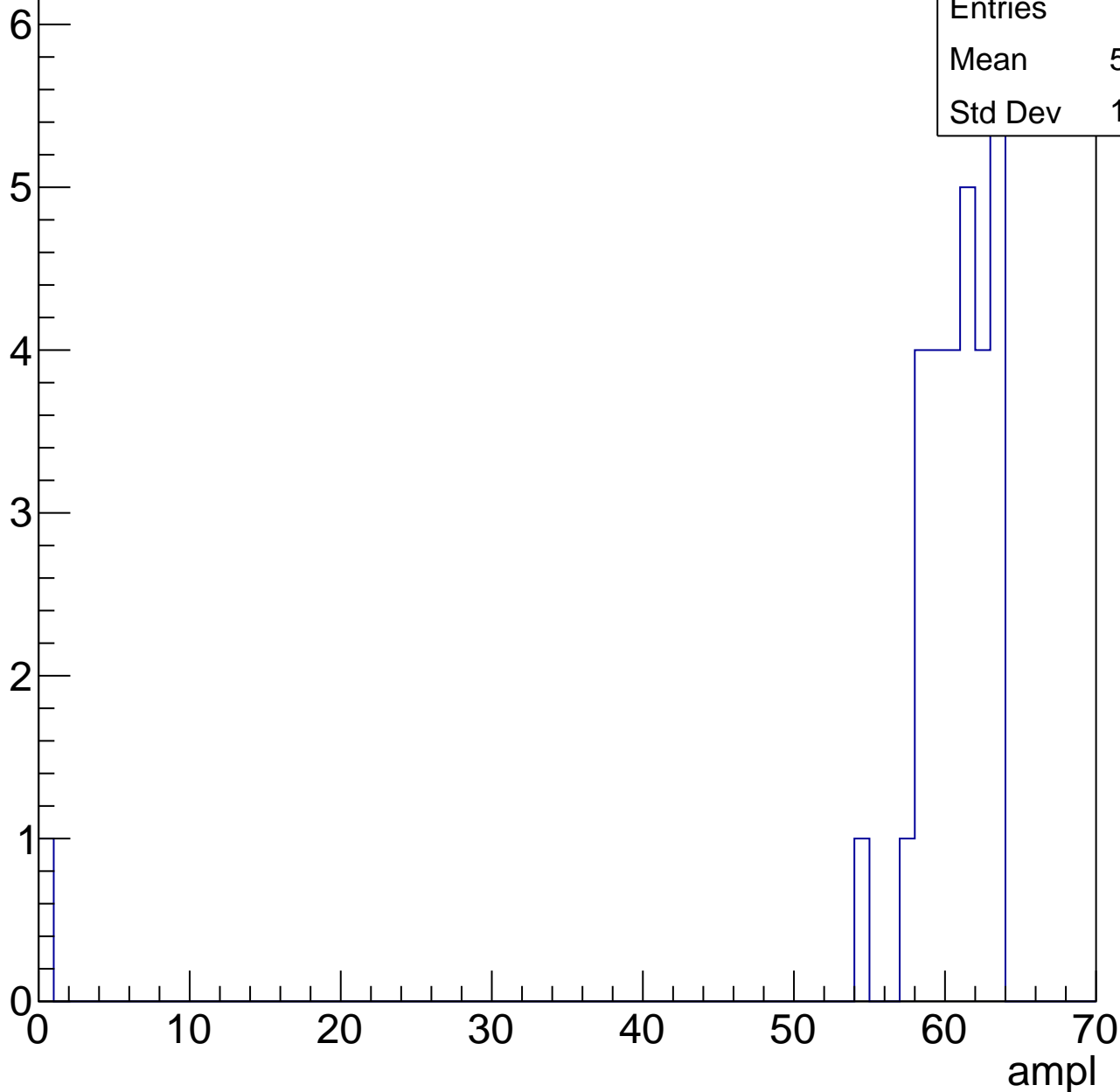


# B0L001S, U5-ch77, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

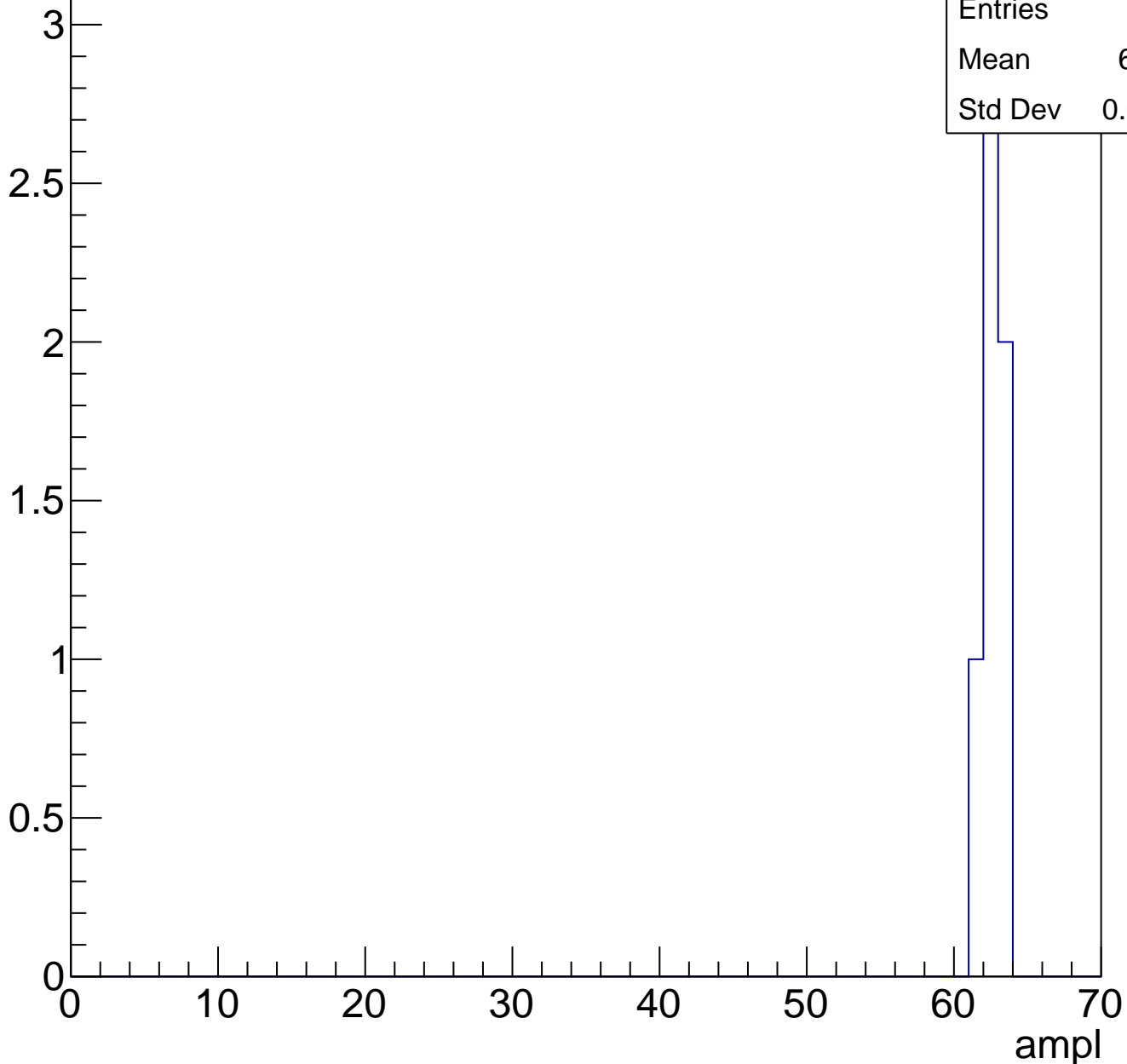
Entries	30
Mean	58.33
Std Dev	11.04



# B0L001S, U5-ch77, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch77, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch78, adc0

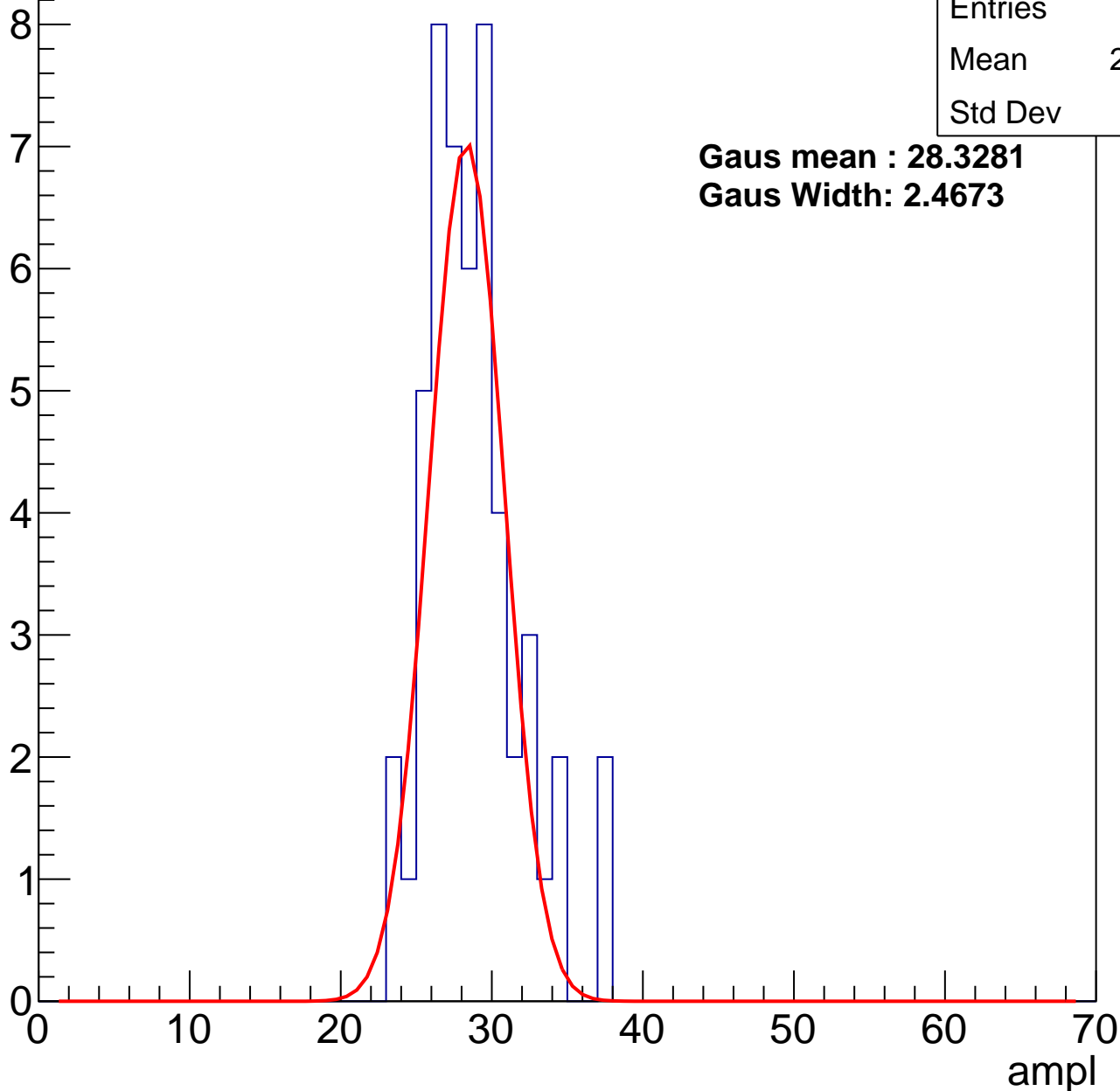
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	51
Mean	28.33
Std Dev	3.11

**Gaus mean : 28.3281**

**Gaus Width: 2.4673**



# B0L001S, U5-ch78, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	77
Mean	34.48
Std Dev	4.12

**Gaus mean : 34.7240**

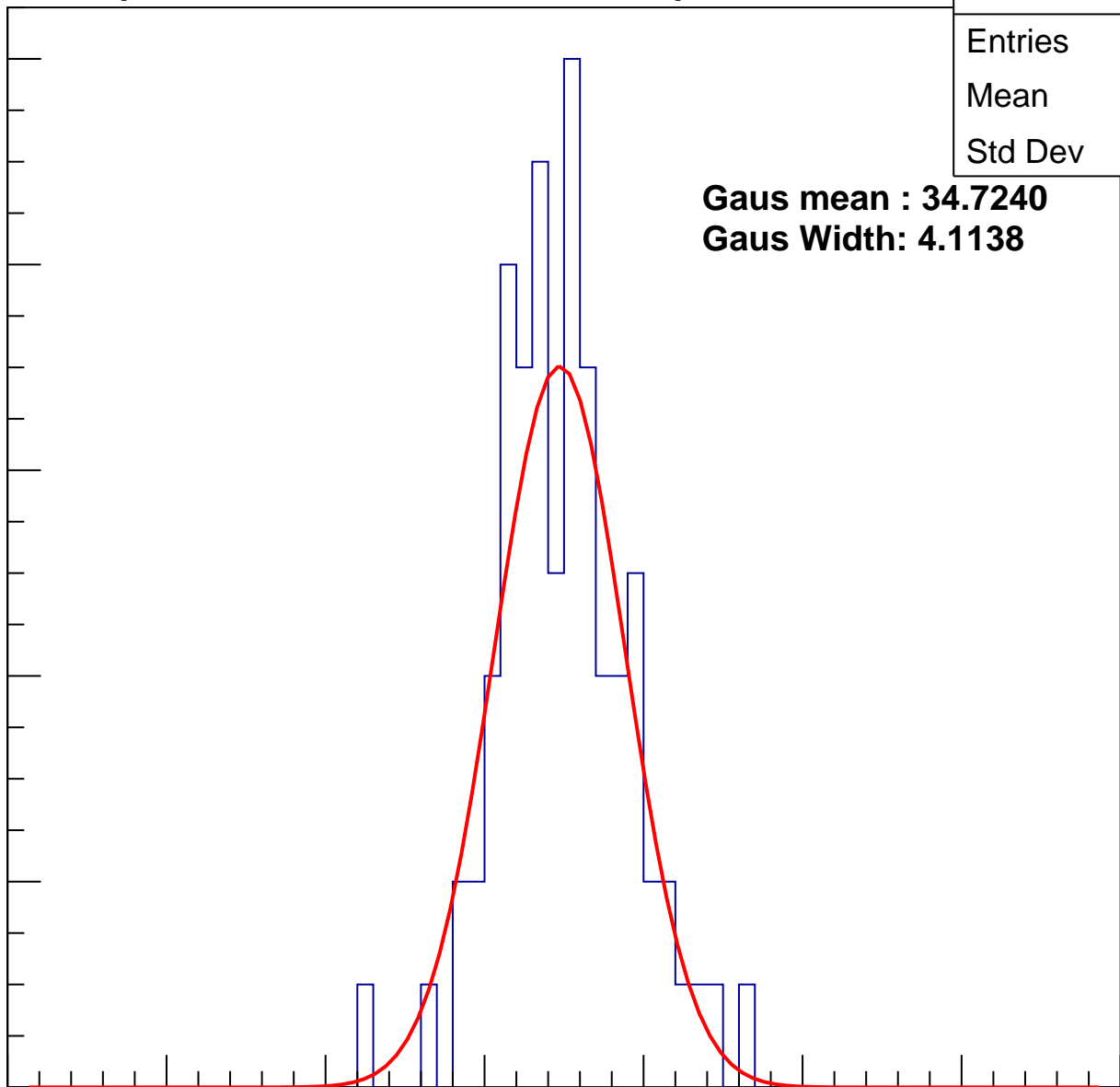
**Gaus Width: 4.1138**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U5-ch78, adc2

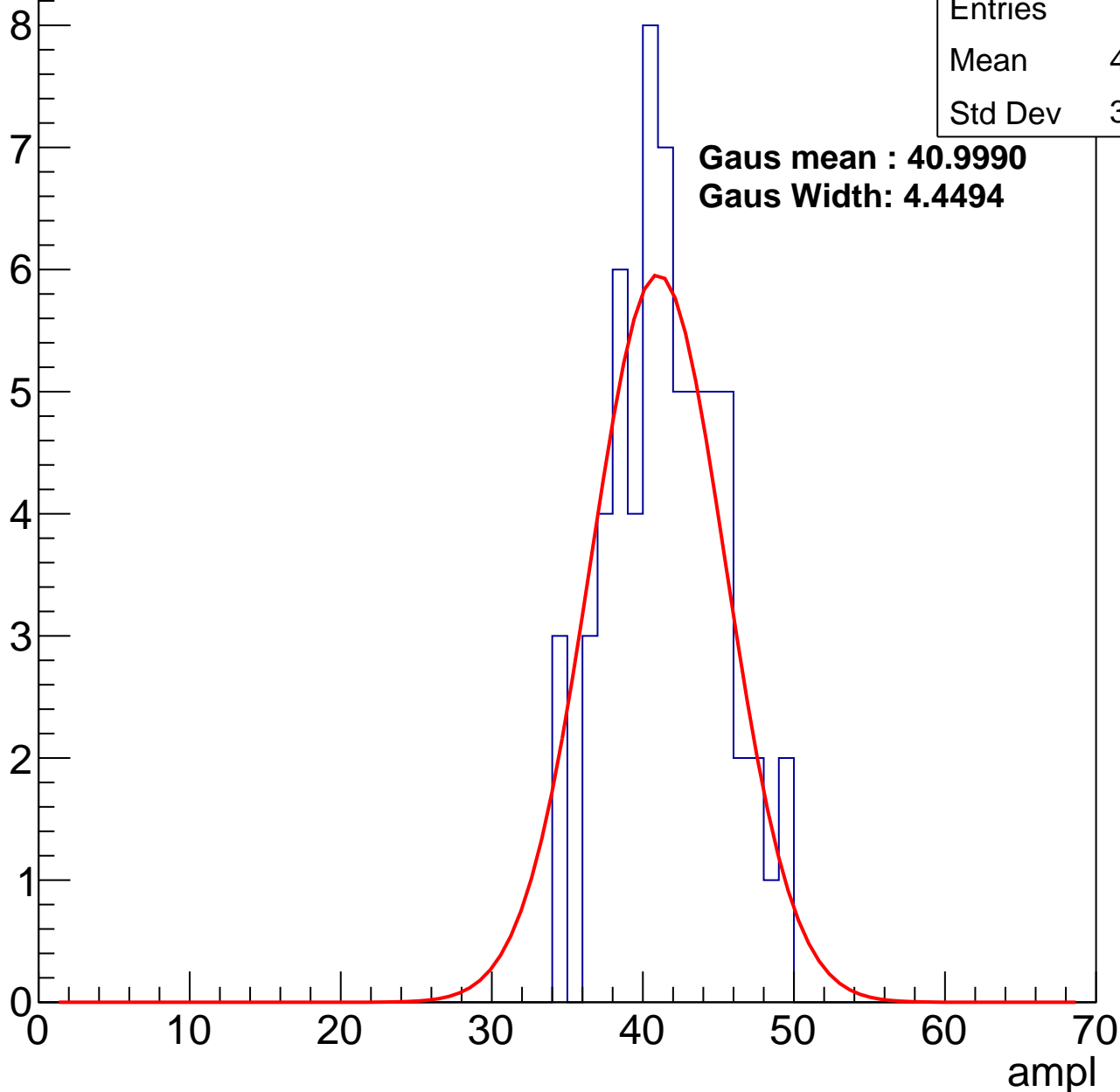
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	41.15
Std Dev	3.618

**Gaus mean : 40.9990**

**Gaus Width: 4.4494**

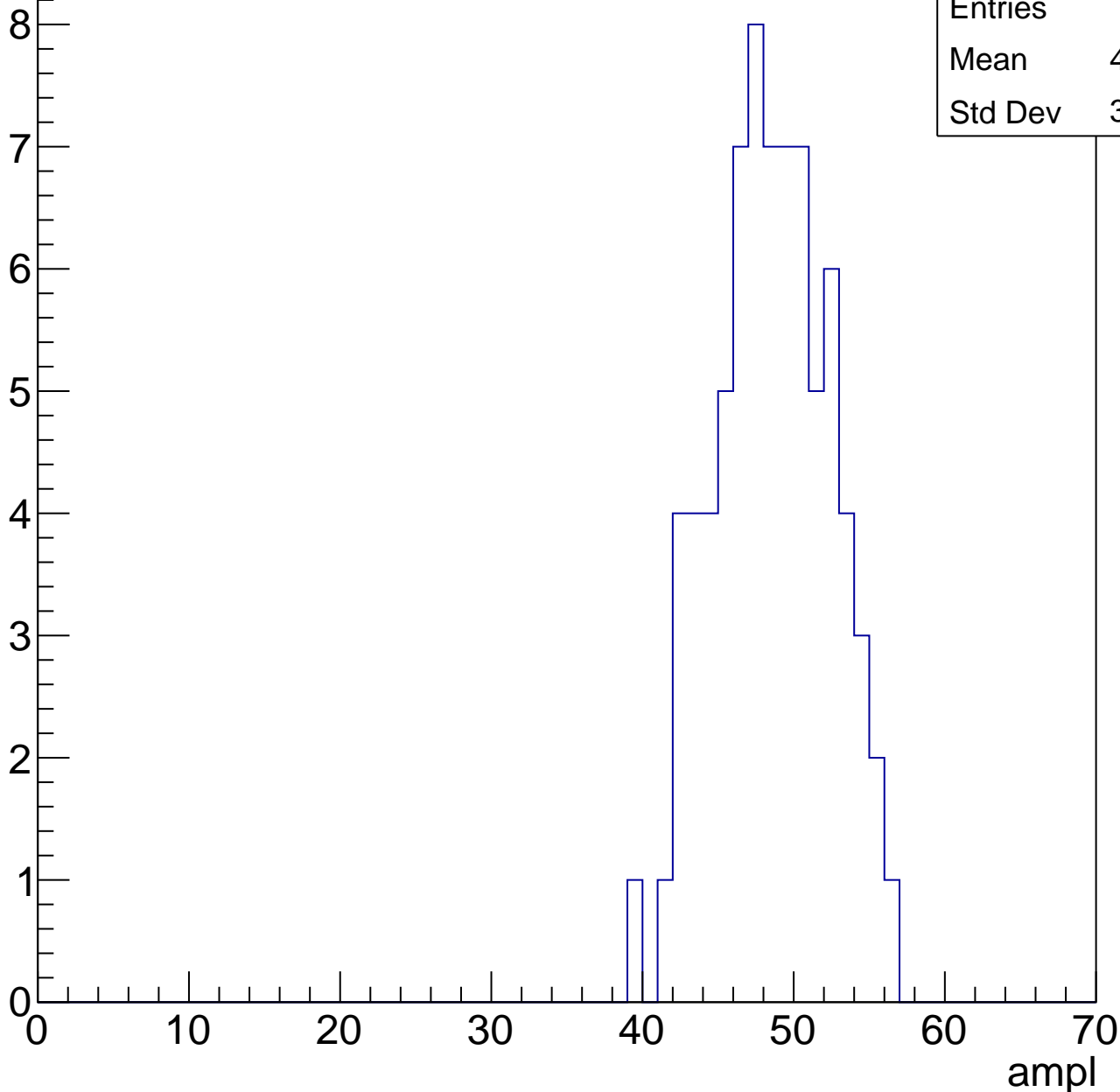


# B0L001S, U5-ch78, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	76
Mean	48.09
Std Dev	3.742

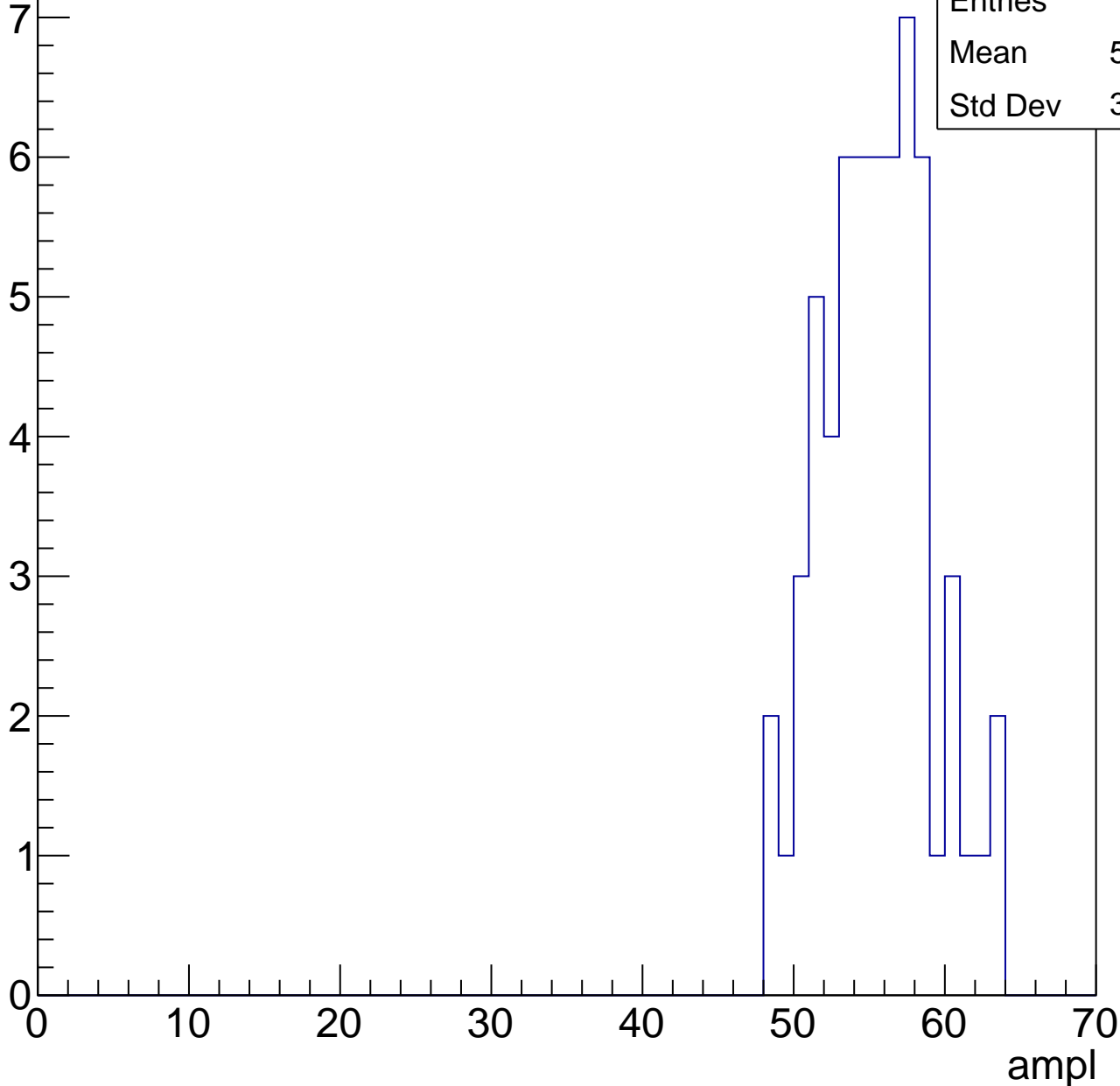


# B0L001S, U5-ch78, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

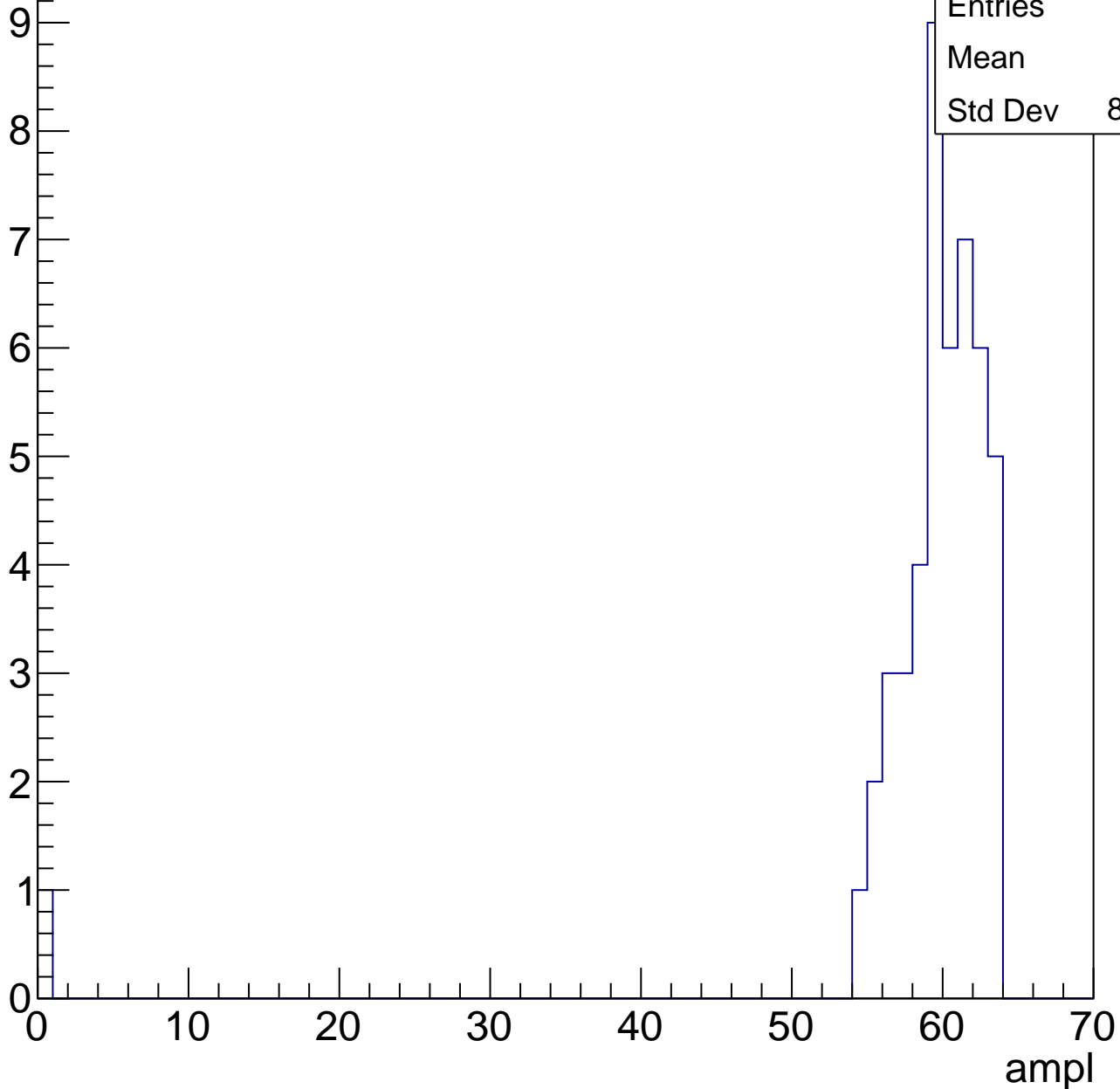
Entries	60
Mean	55.02
Std Dev	3.528



# B0L001S, U5-ch78, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

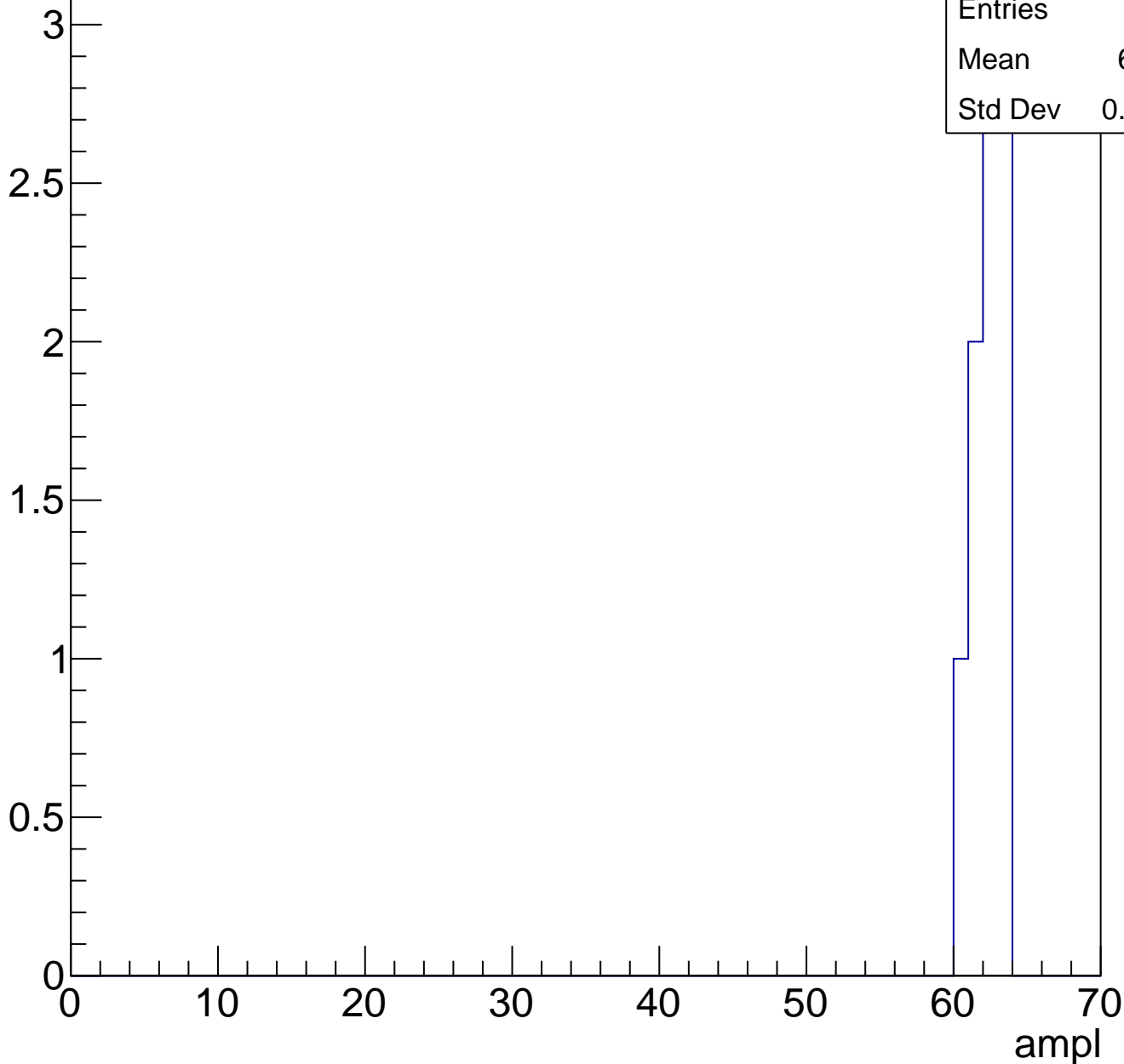
Entry



# B0L001S, U5-ch78, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch78, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch79, adc0

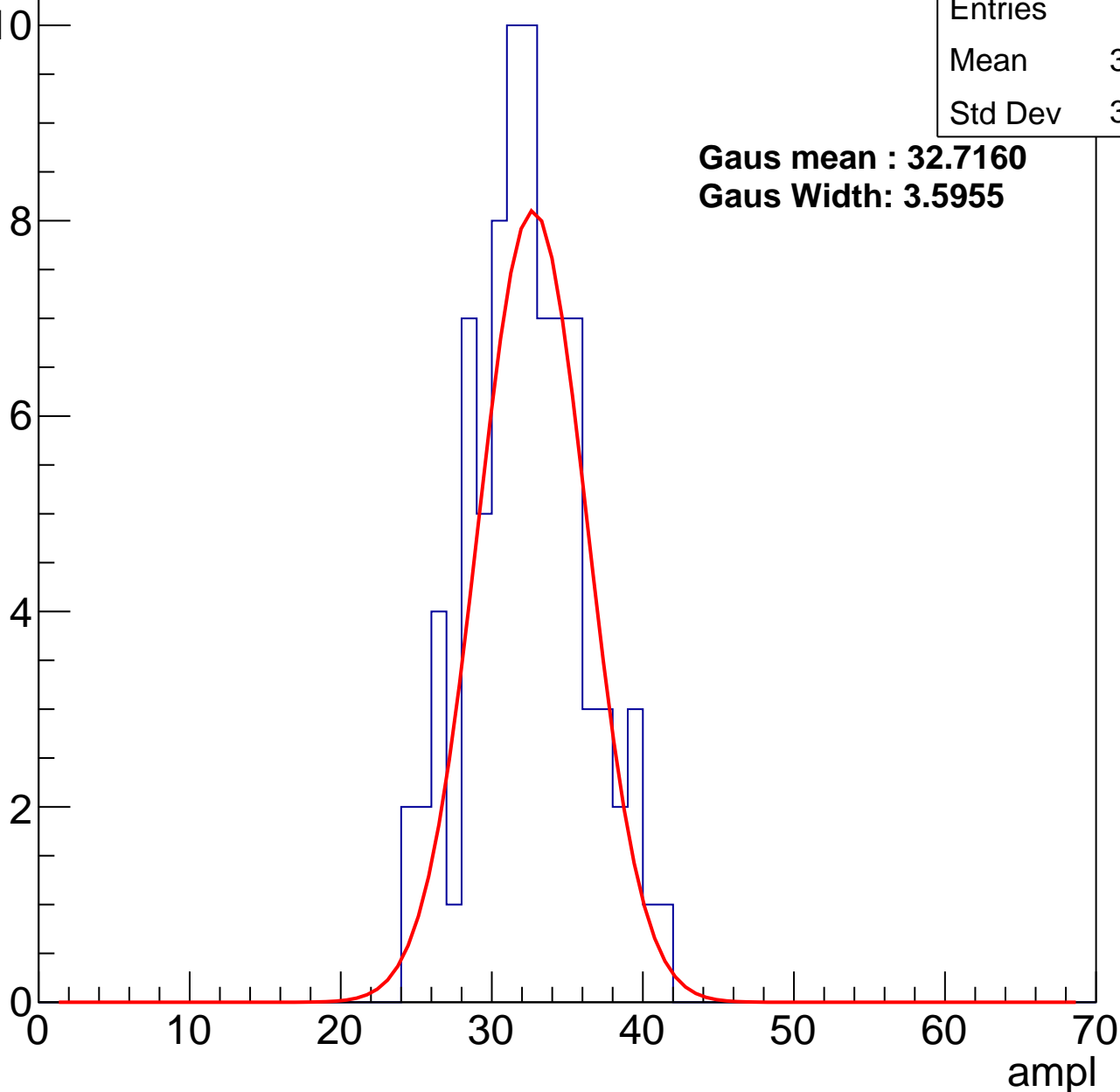
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	83
Mean	31.89
Std Dev	3.767

**Gaus mean : 32.7160**

**Gaus Width: 3.5955**



# B0L001S, U5-ch79, adc1

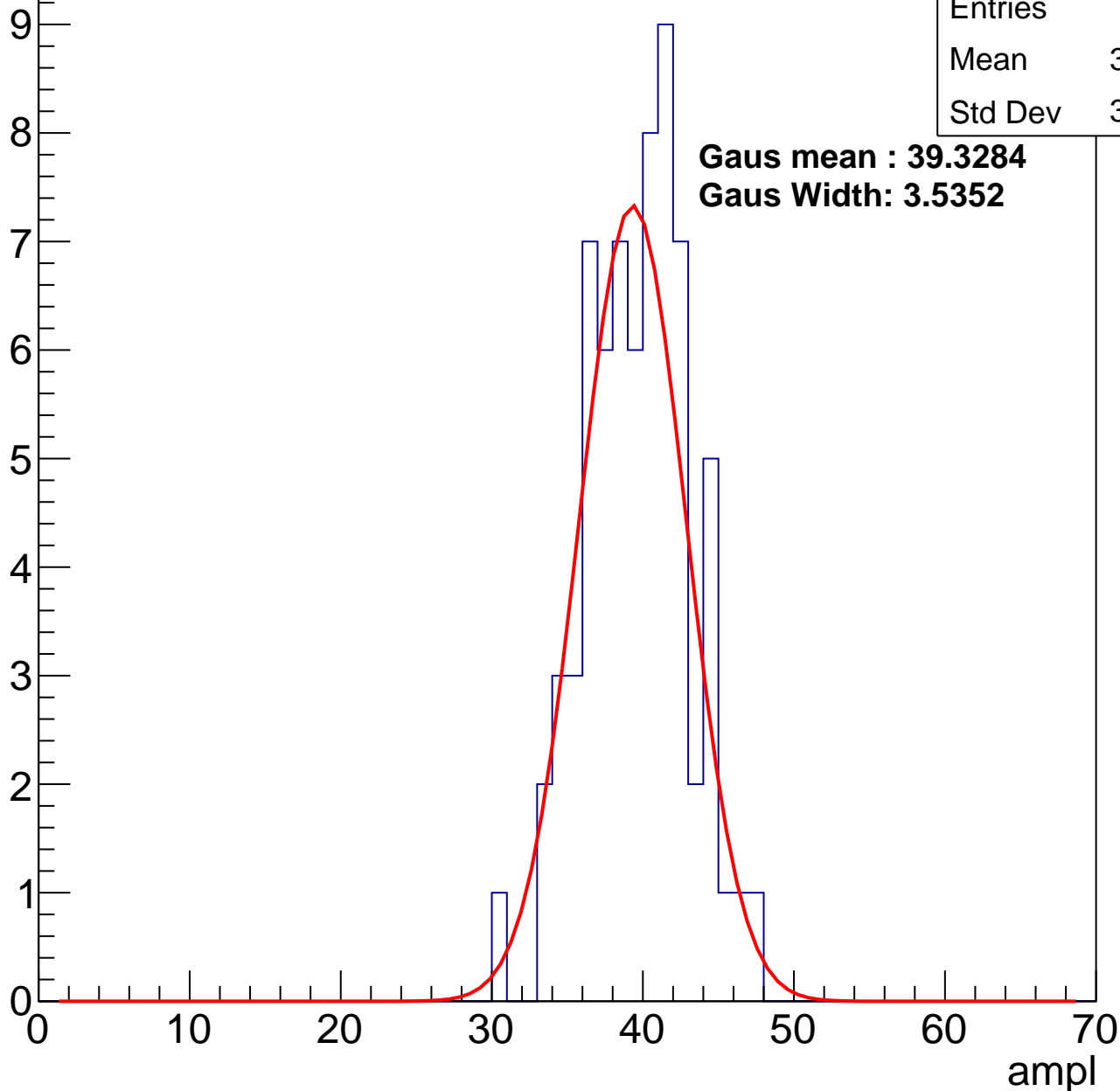
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	39.19
Std Dev	3.363

**Gaus mean : 39.3284**

**Gaus Width: 3.5352**



# B0L001S, U5-ch79, adc2

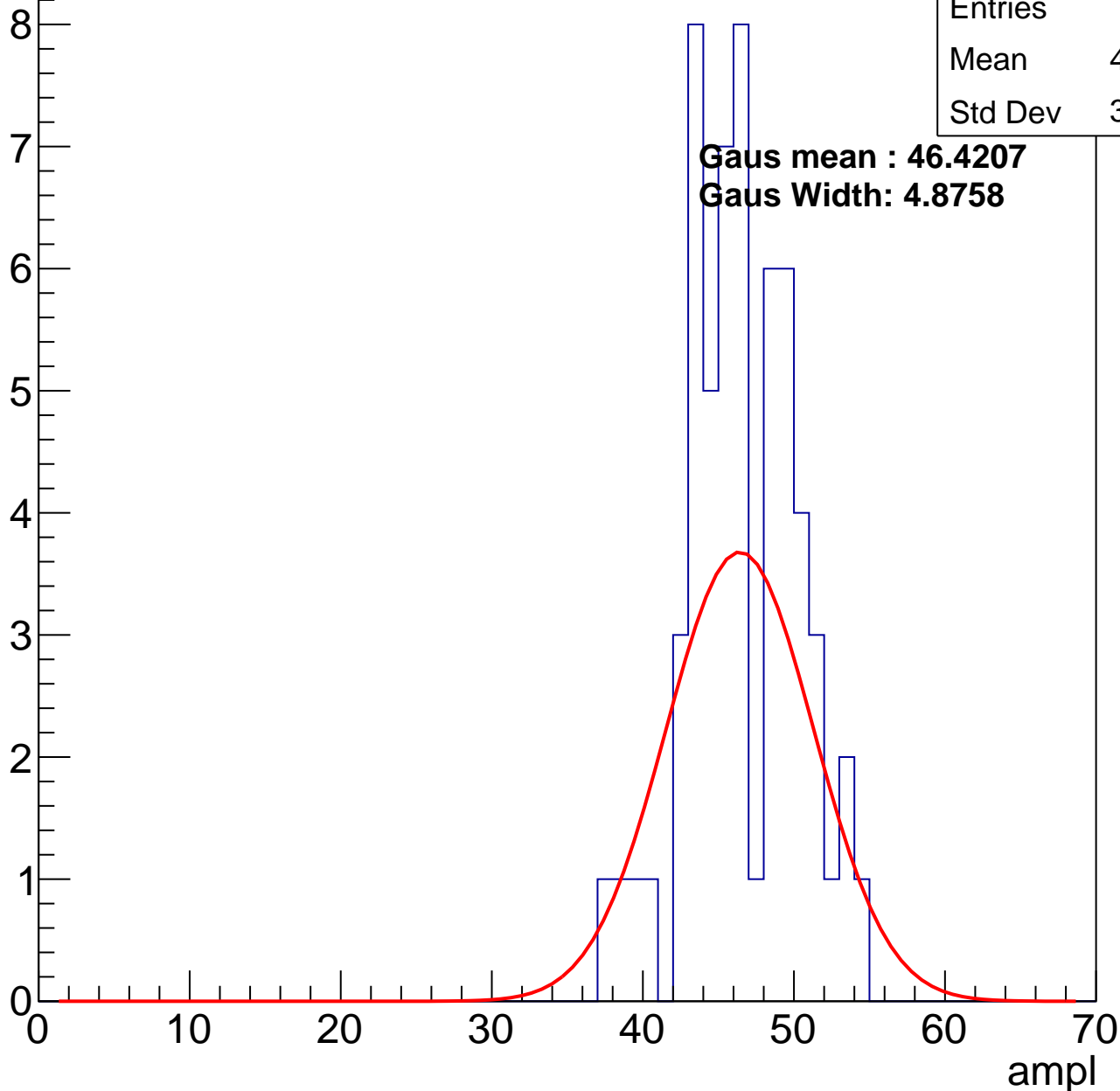
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	46.12
Std Dev	3.664

**Gaus mean : 46.4207**

**Gaus Width: 4.8758**

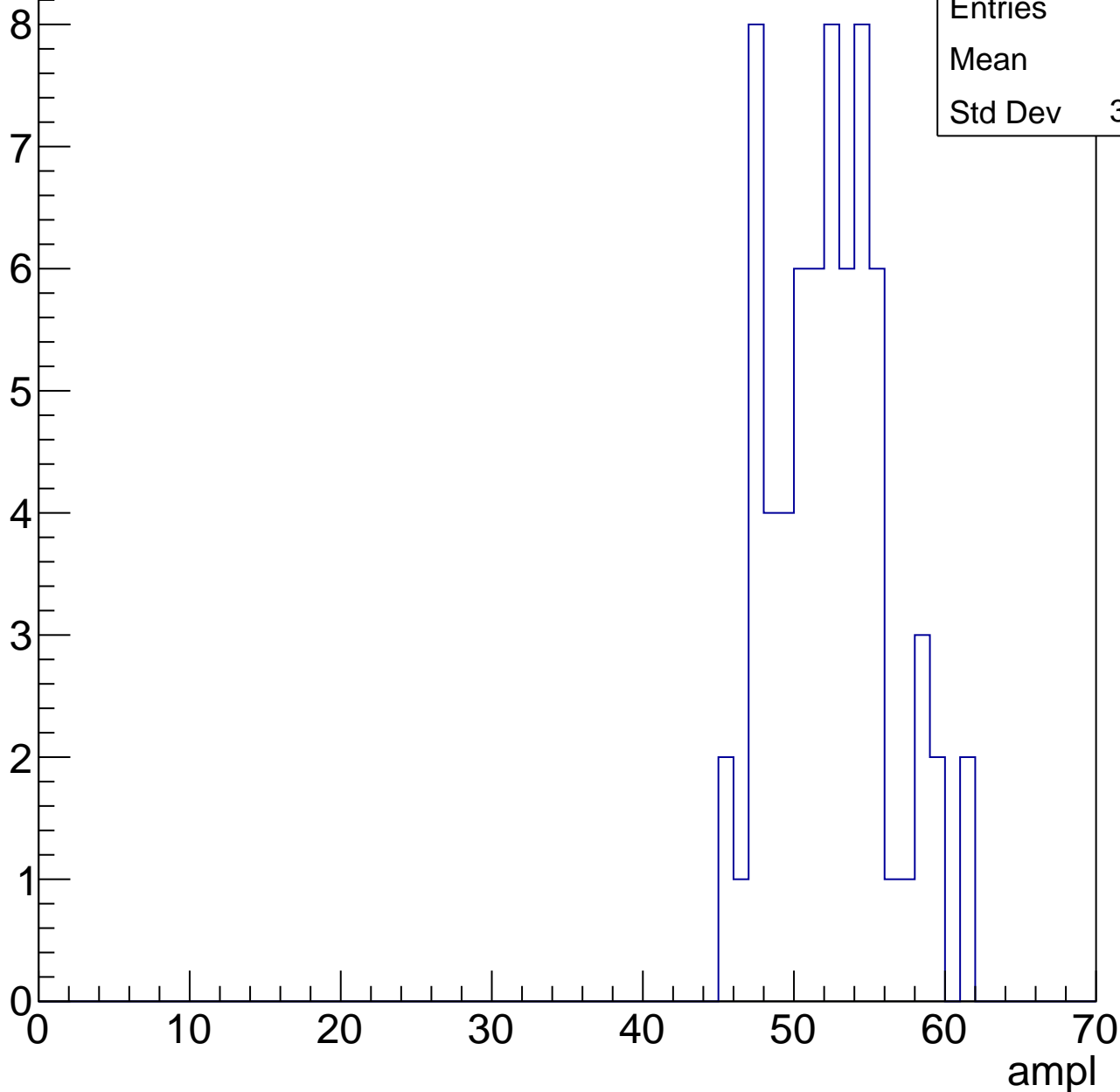


# B0L001S, U5-ch79, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	51.9
Std Dev	3.766

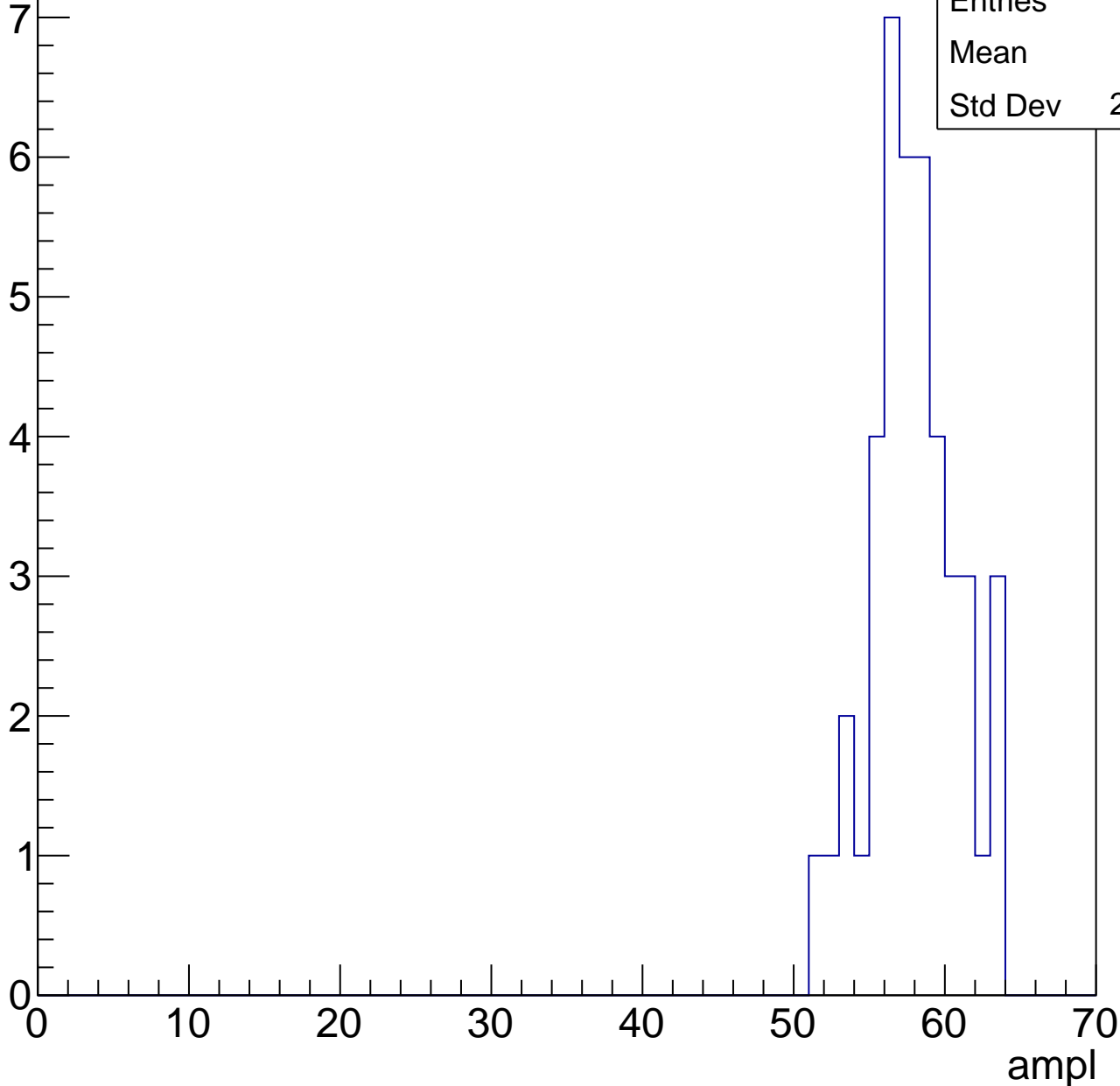


# B0L001S, U5-ch79, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	42
Mean	57.5
Std Dev	2.864

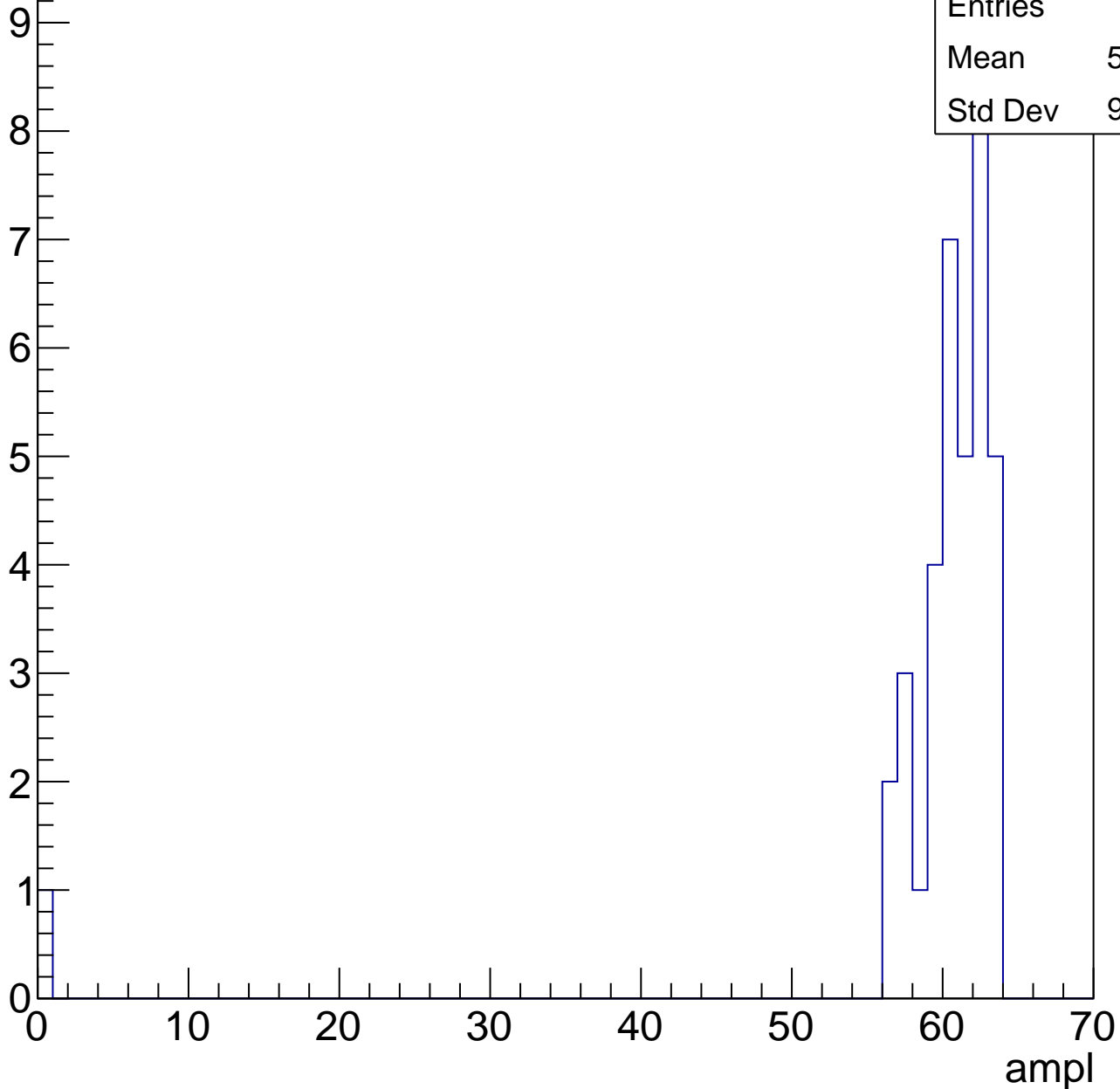


# B0L001S, U5-ch79, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	37
Mean	58.78
Std Dev	9.998



# B0L001S, U5-ch79, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

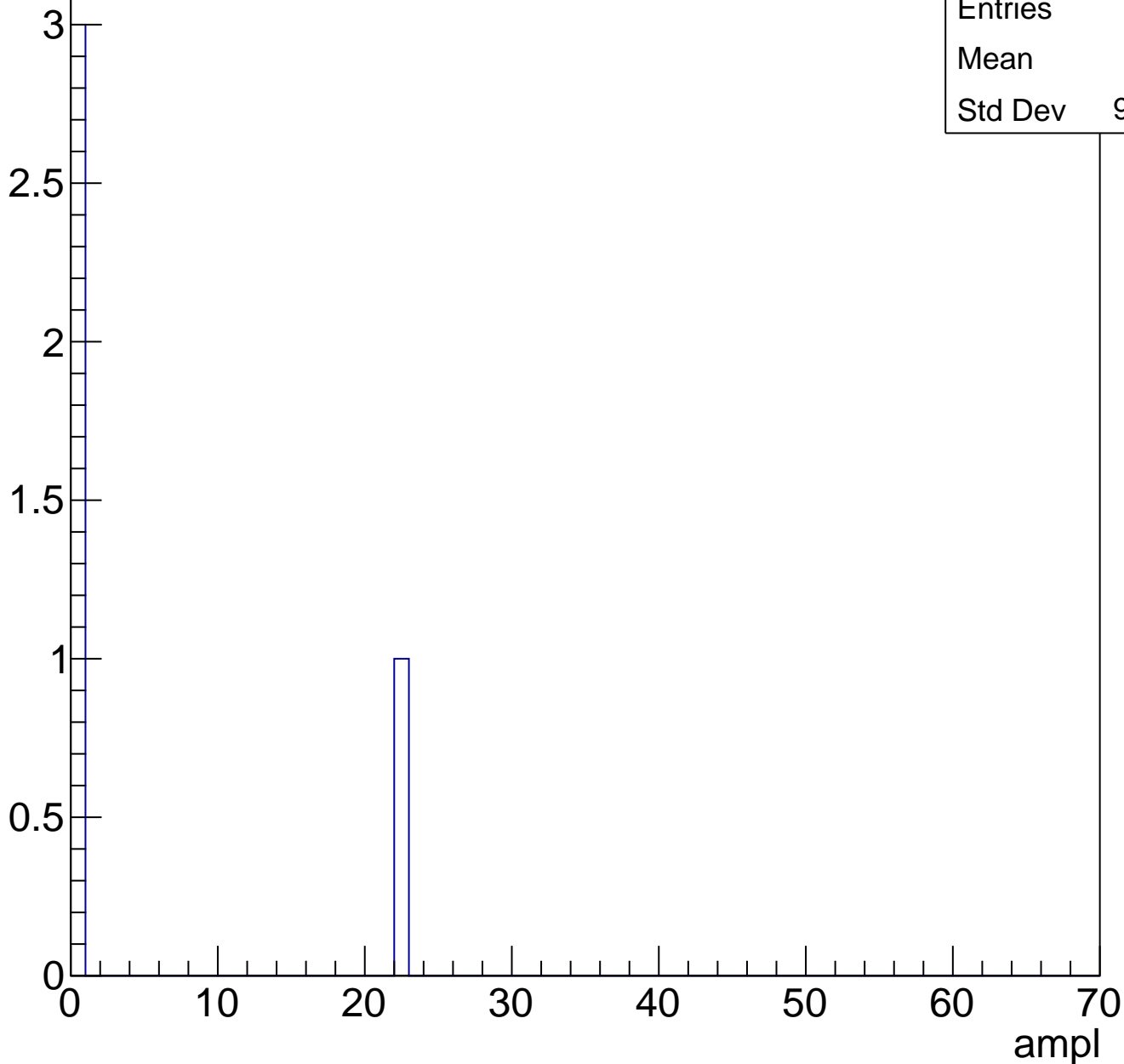




# B0L001S, U5-ch79, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch80, adc0

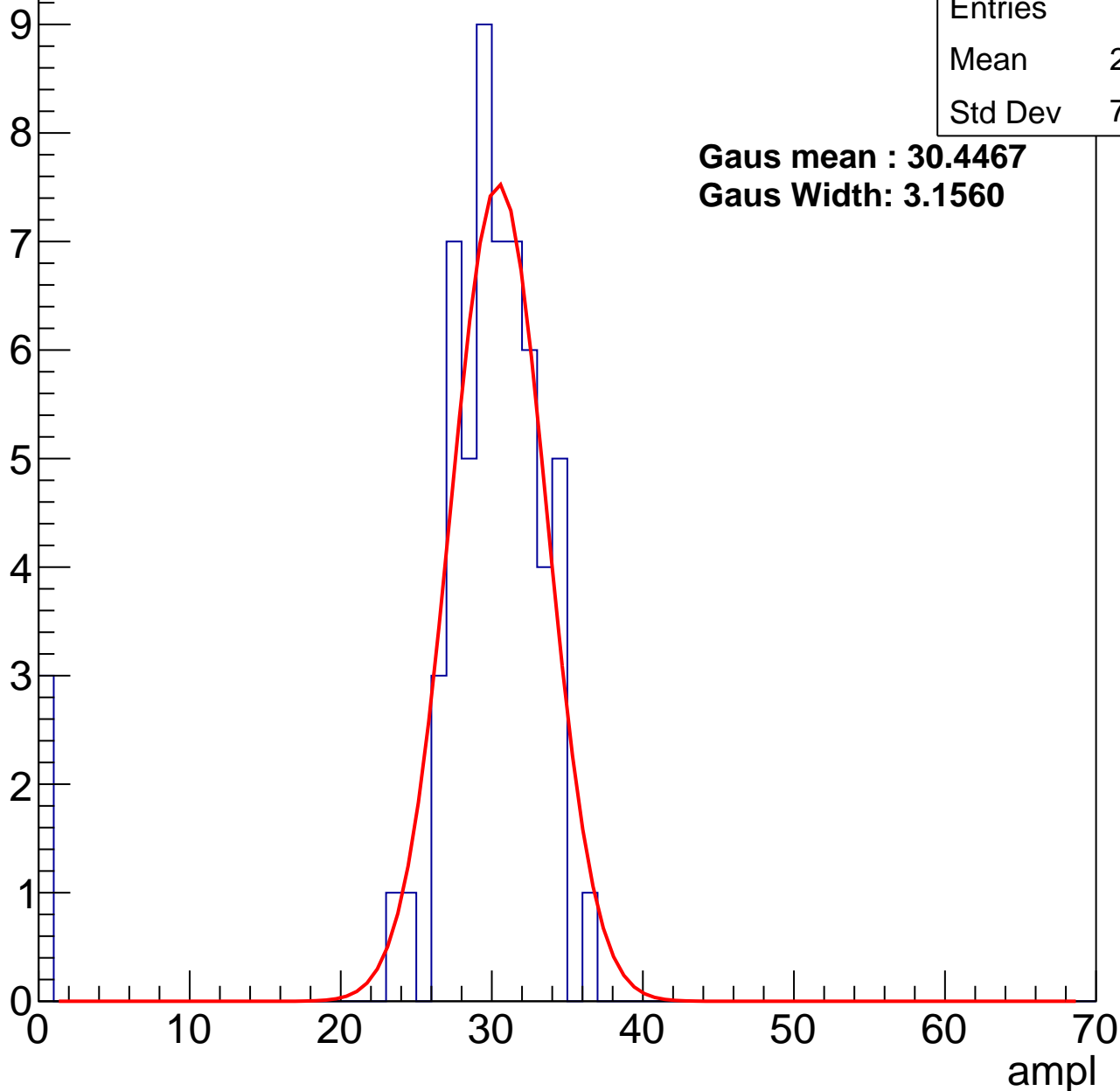
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	28.34
Std Dev	7.065

**Gaus mean : 30.4467**

**Gaus Width: 3.1560**



# B0L001S, U5-ch80, adc1

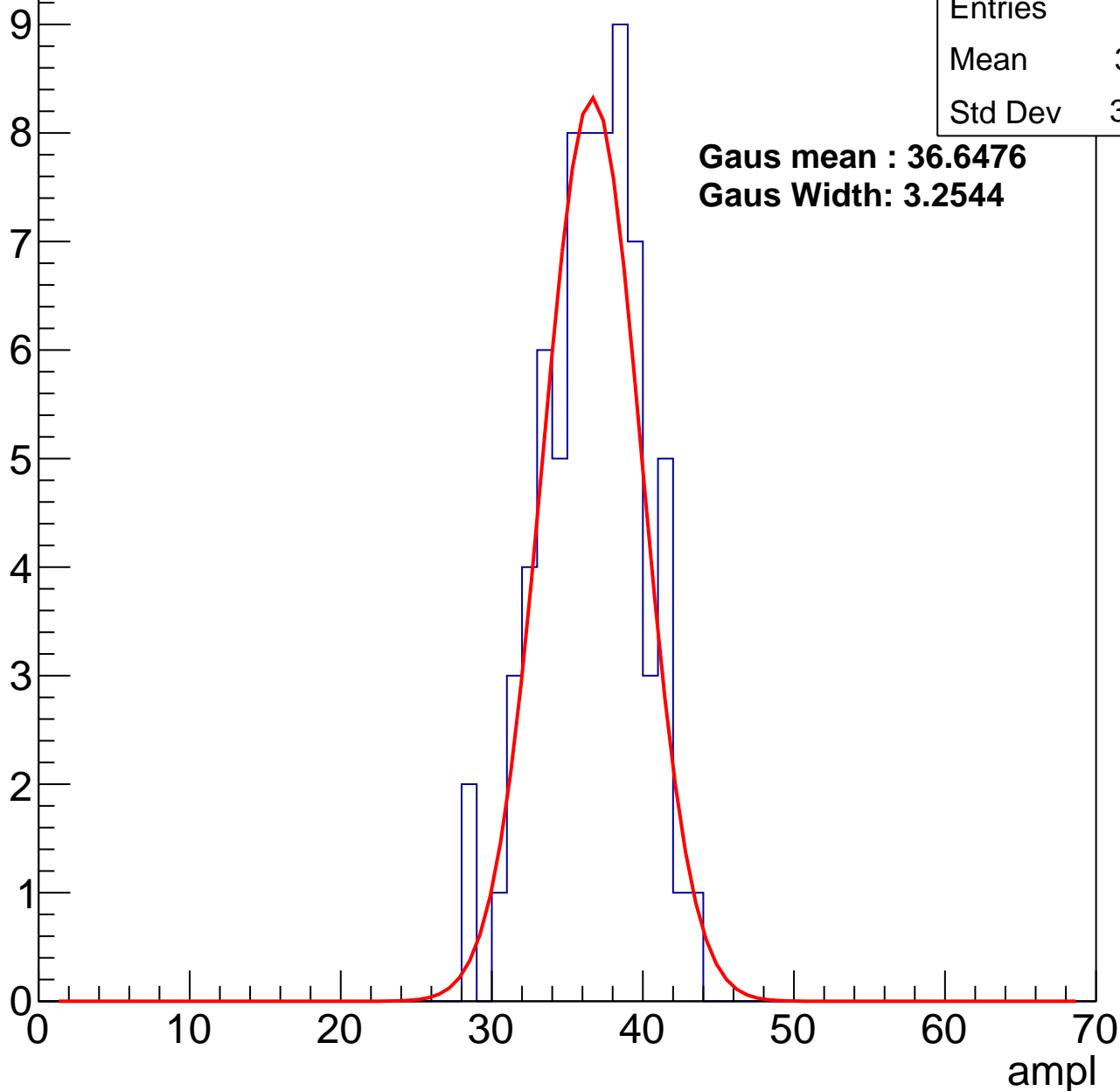
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	36.11
Std Dev	3.248

**Gaus mean : 36.6476**

**Gaus Width: 3.2544**



# B0L001S, U5-ch80, adc2

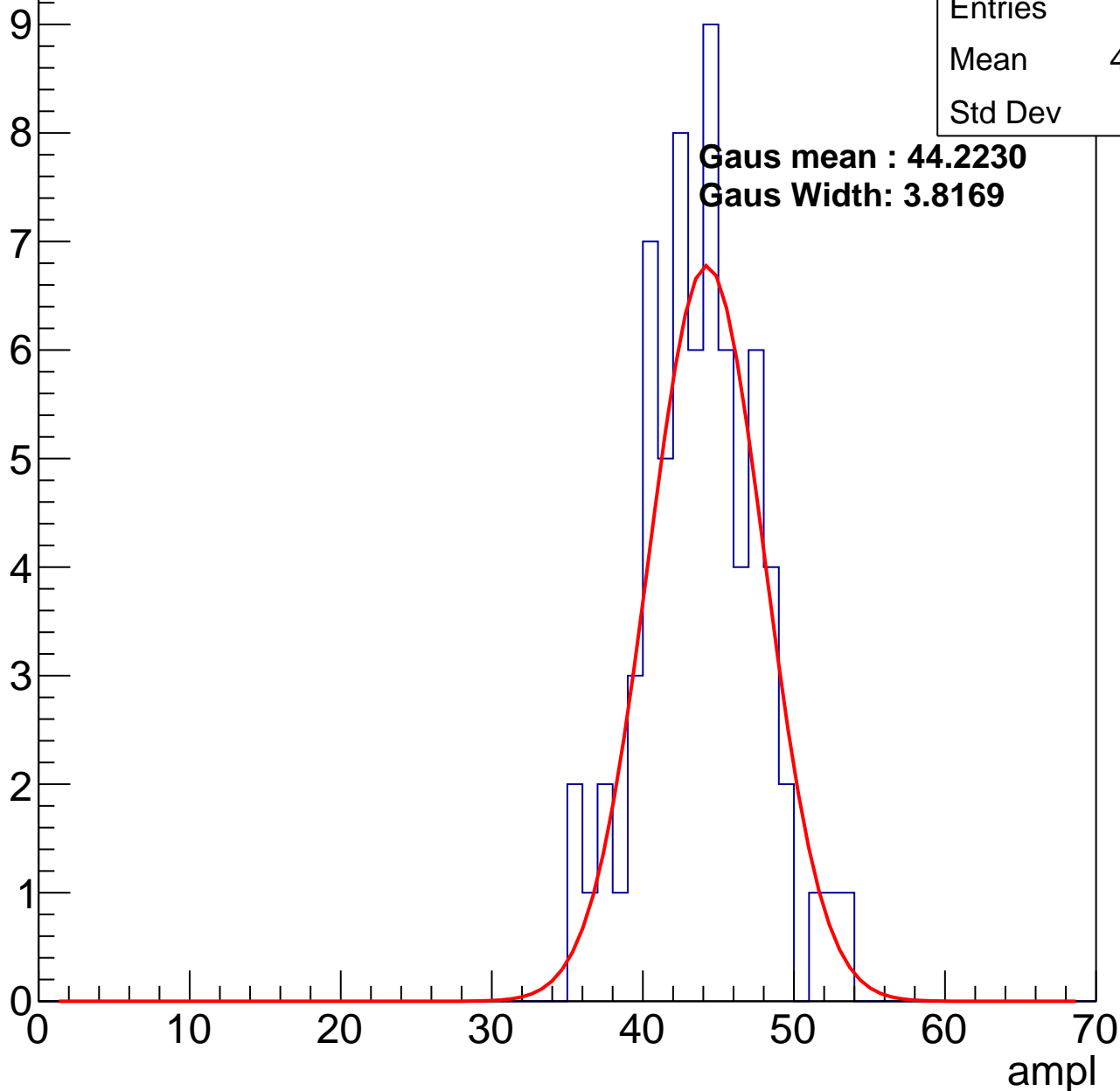
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	43.36
Std Dev	3.78

**Gaus mean : 44.2230**

**Gaus Width: 3.8169**

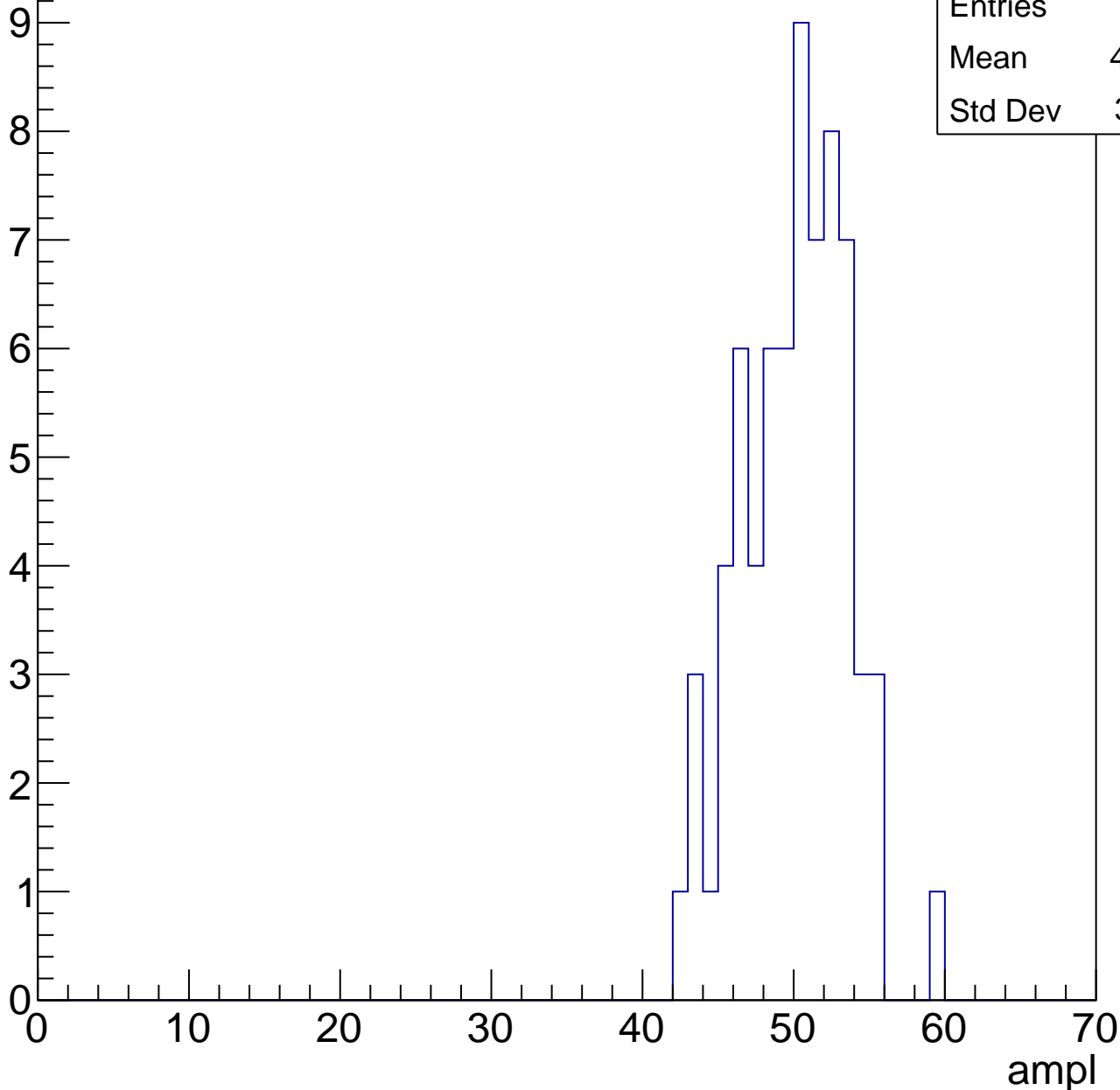


# B0L001S, U5-ch80, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	49.58
Std Dev	3.411

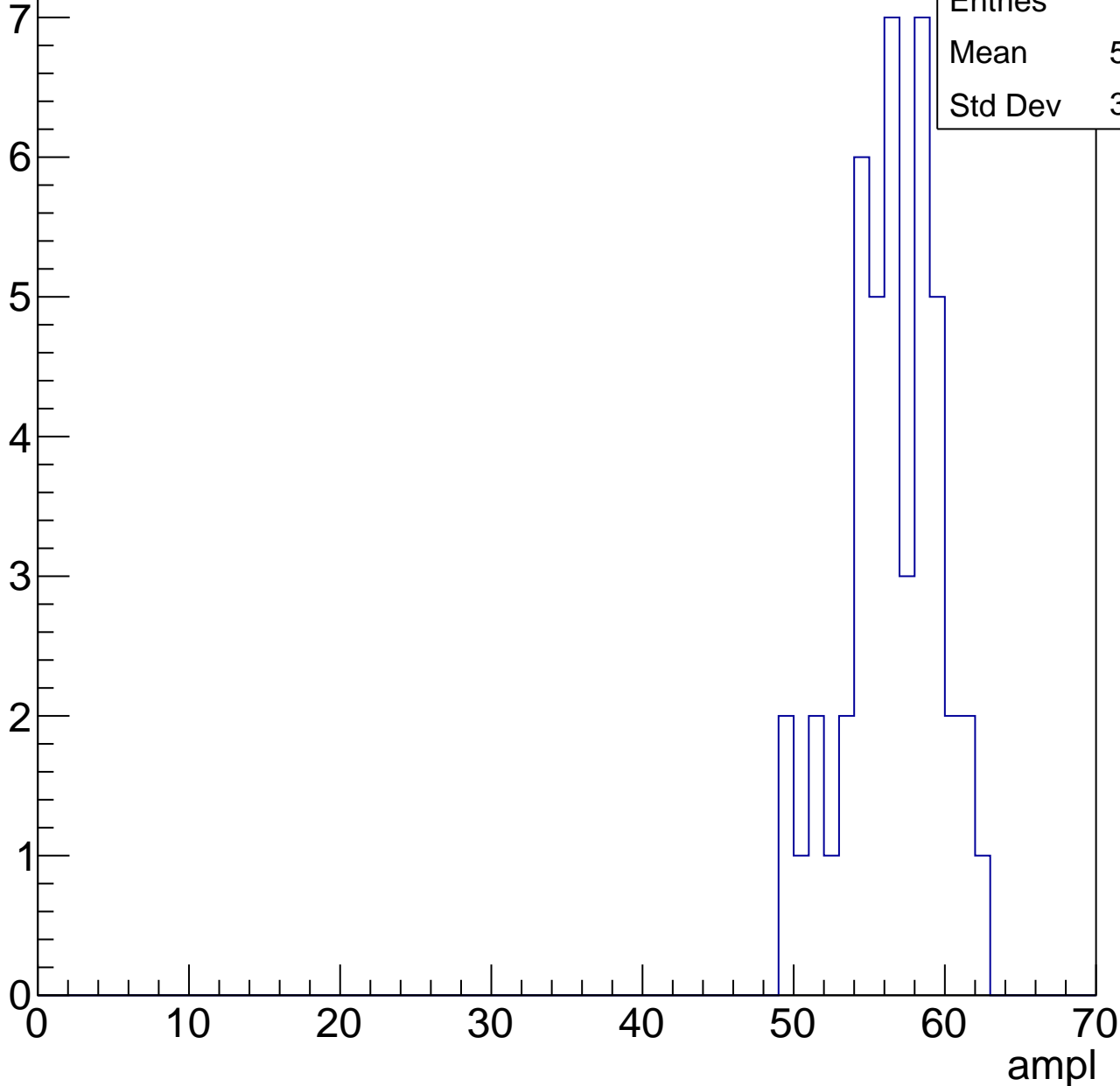


# B0L001S, U5-ch80, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	46
Mean	55.98
Std Dev	3.096

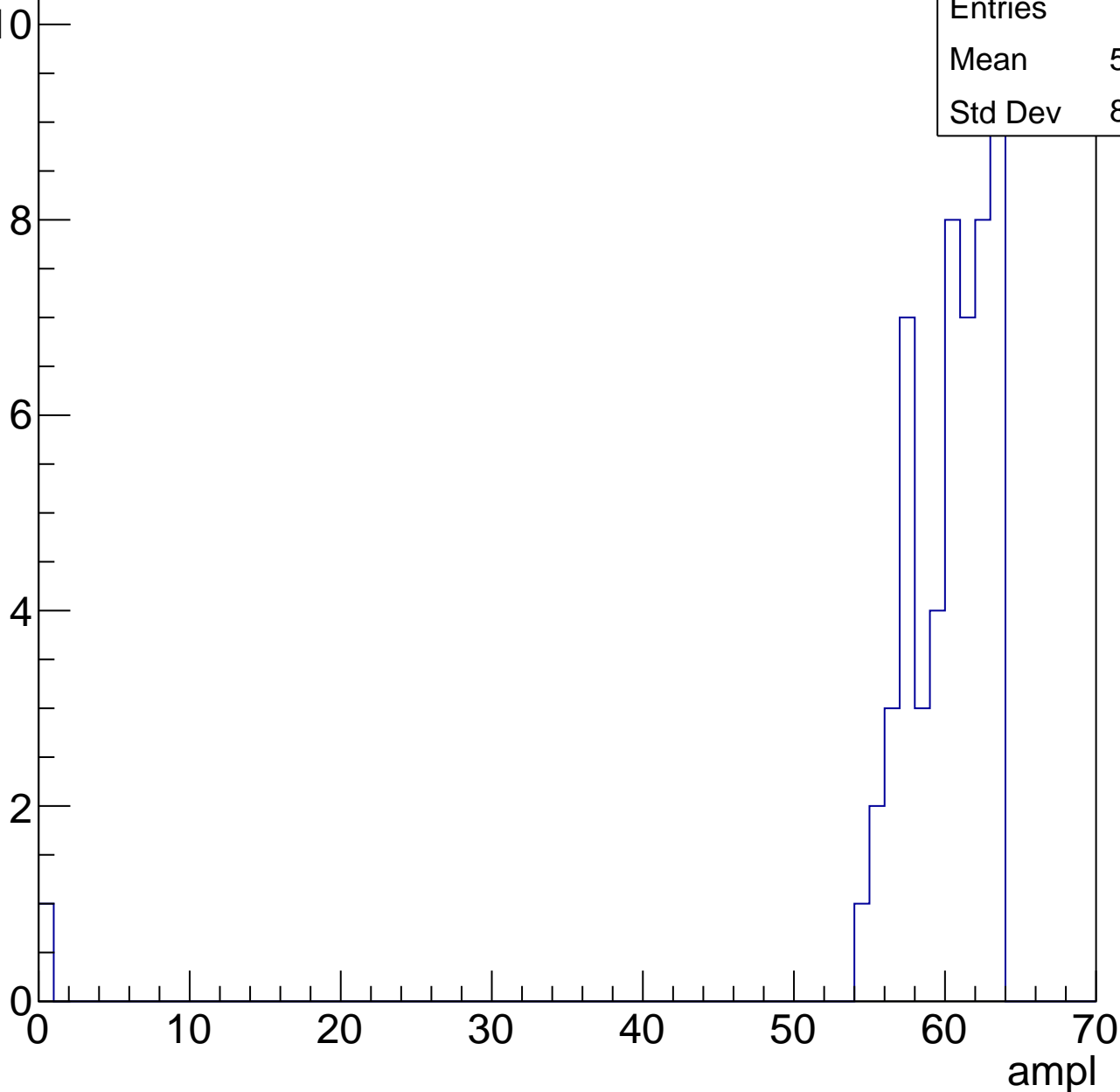


# B0L001S, U5-ch80, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

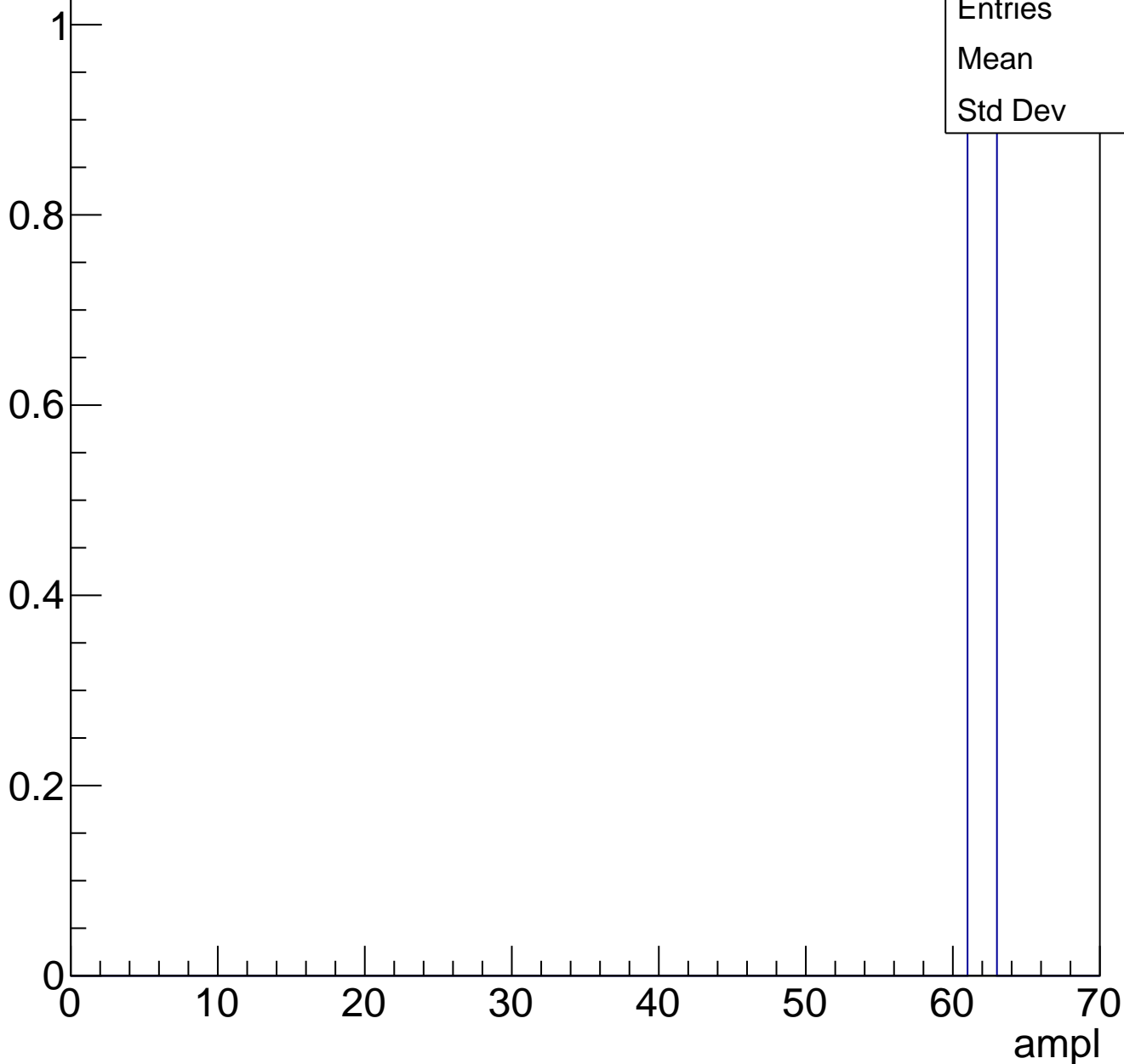
Entries	54
Mean	58.78
Std Dev	8.456



# B0L001S, U5-ch80, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch80, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U5-ch81, adc0

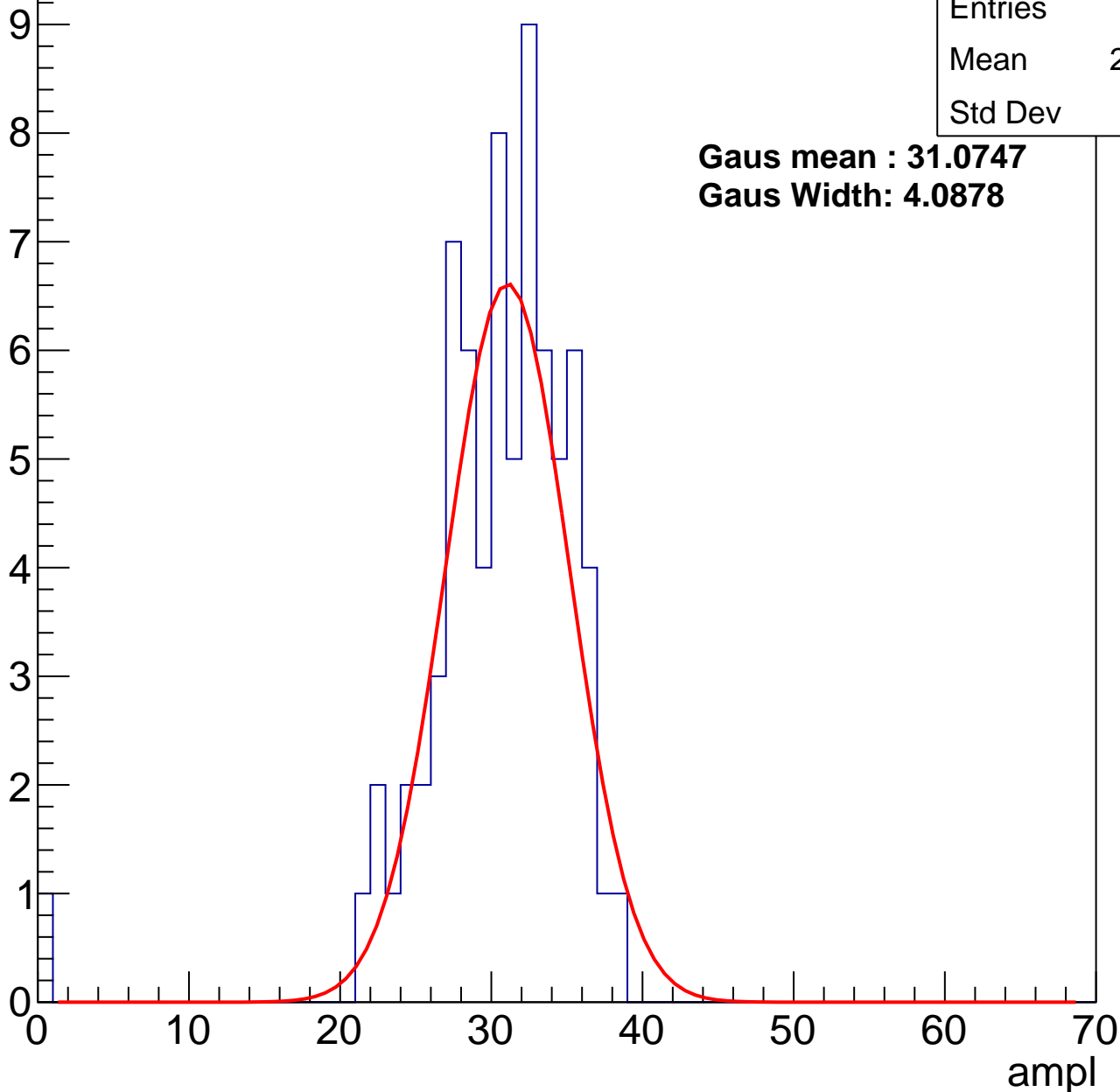
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	29.96
Std Dev	5.2

**Gaus mean : 31.0747**

**Gaus Width: 4.0878**



# B0L001S, U5-ch81, adc1

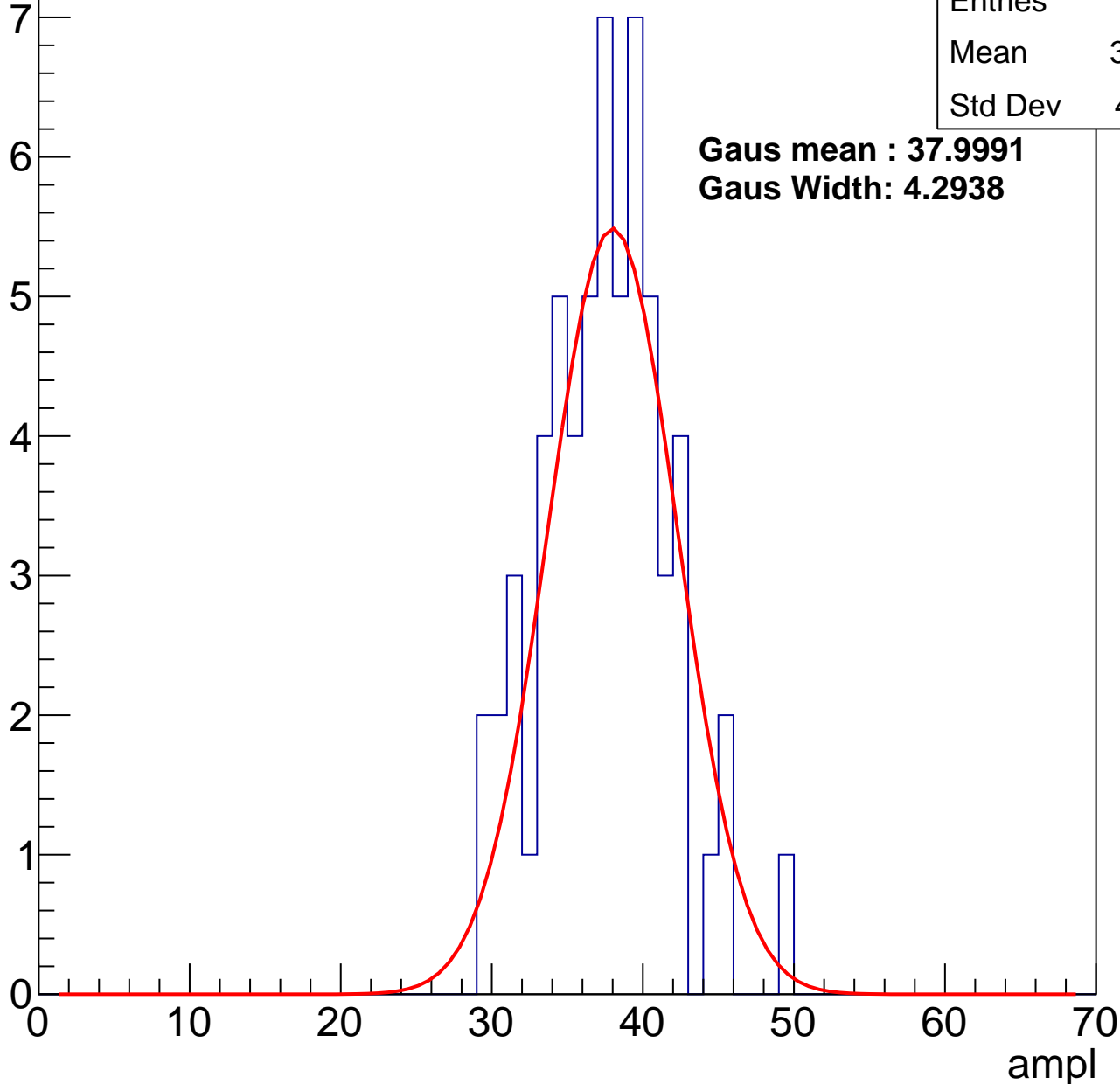
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	37.07
Std Dev	4.121

**Gaus mean : 37.9991**

**Gaus Width: 4.2938**



# B0L001S, U5-ch81, adc2

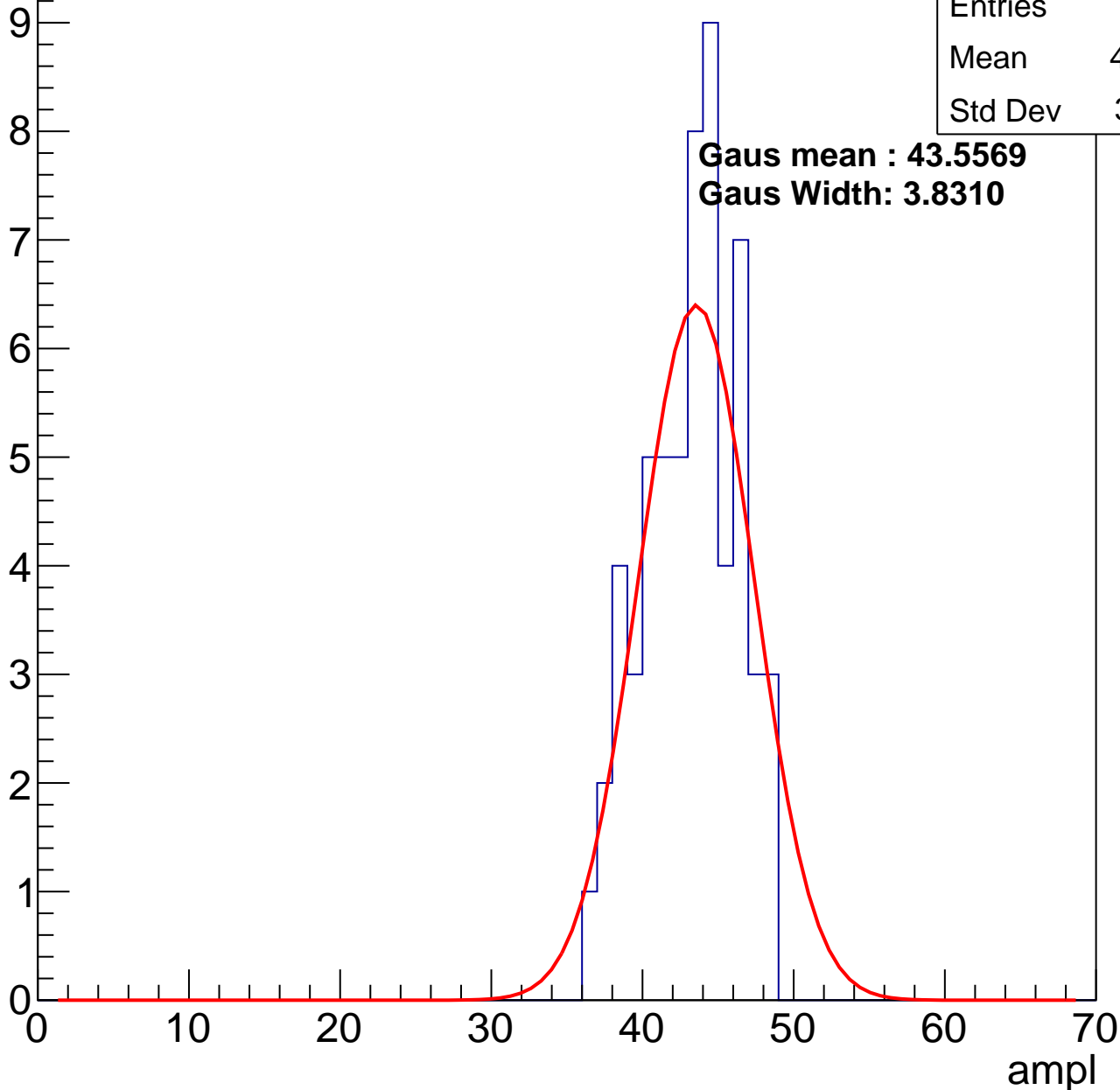
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	42.73
Std Dev	3.041

**Gaus mean : 43.5569**

**Gaus Width: 3.8310**

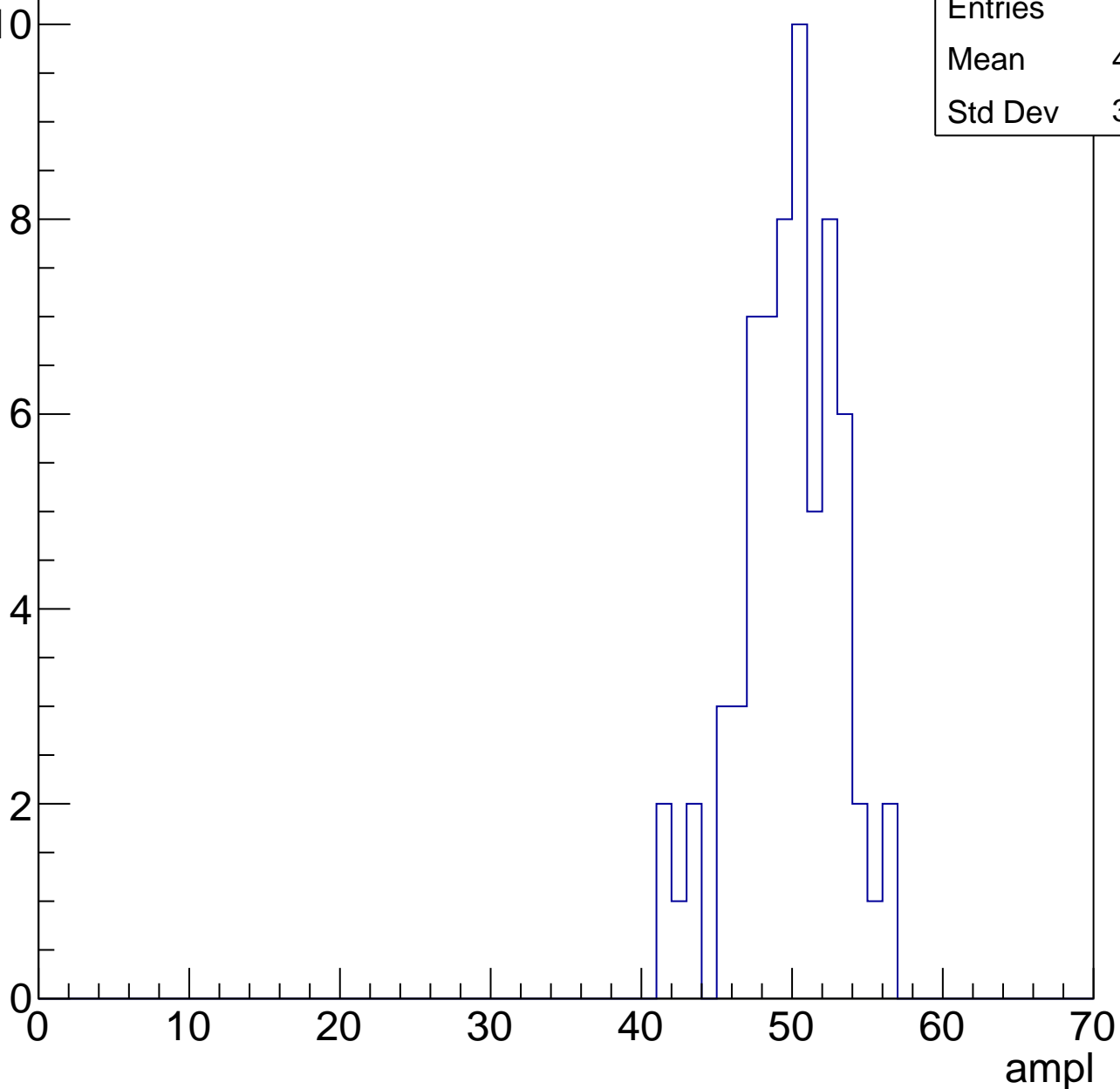


# B0L001S, U5-ch81, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

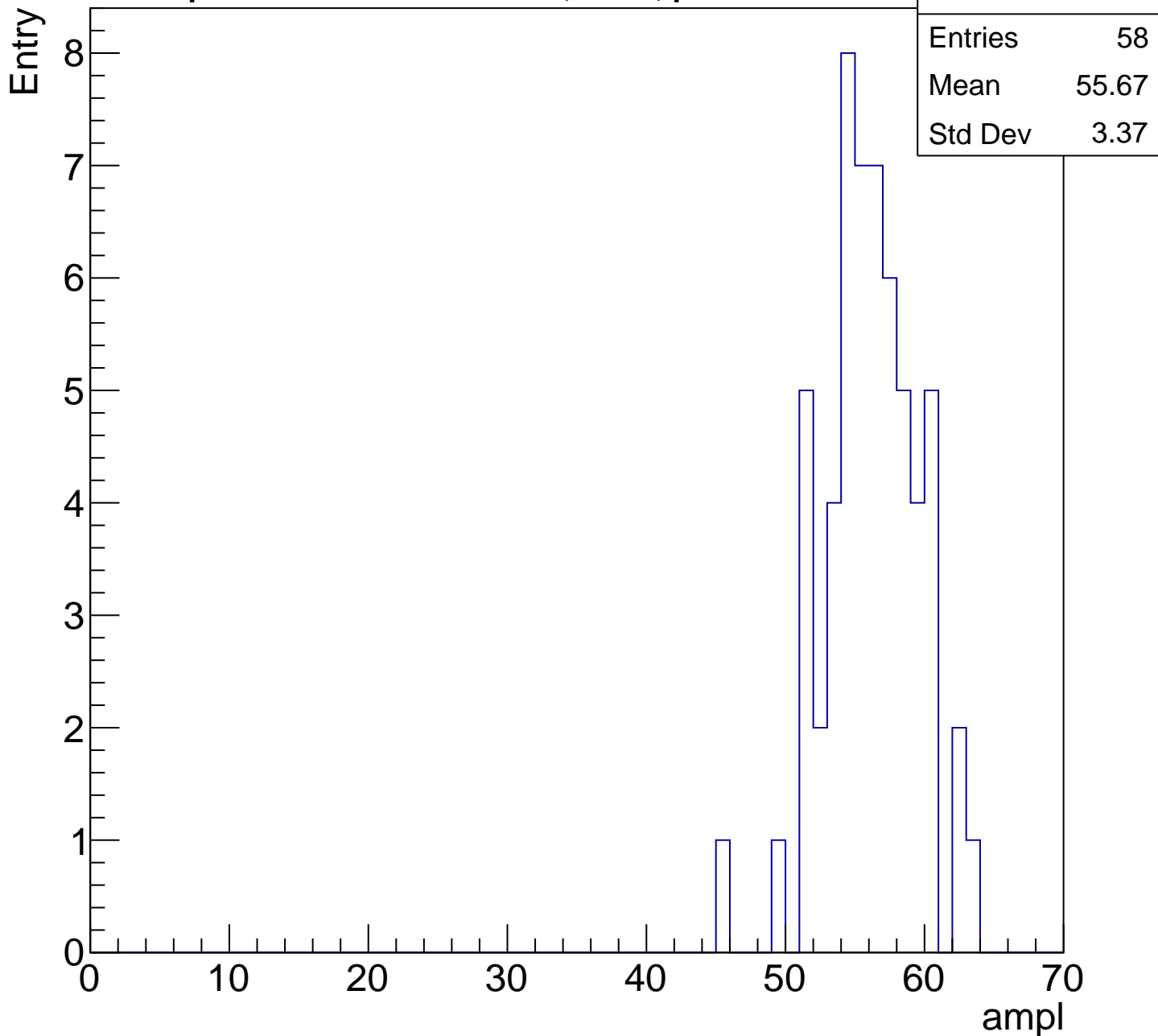
Entry

Entries	67
Mean	49.31
Std Dev	3.311



# B0L001S, U5-ch81, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

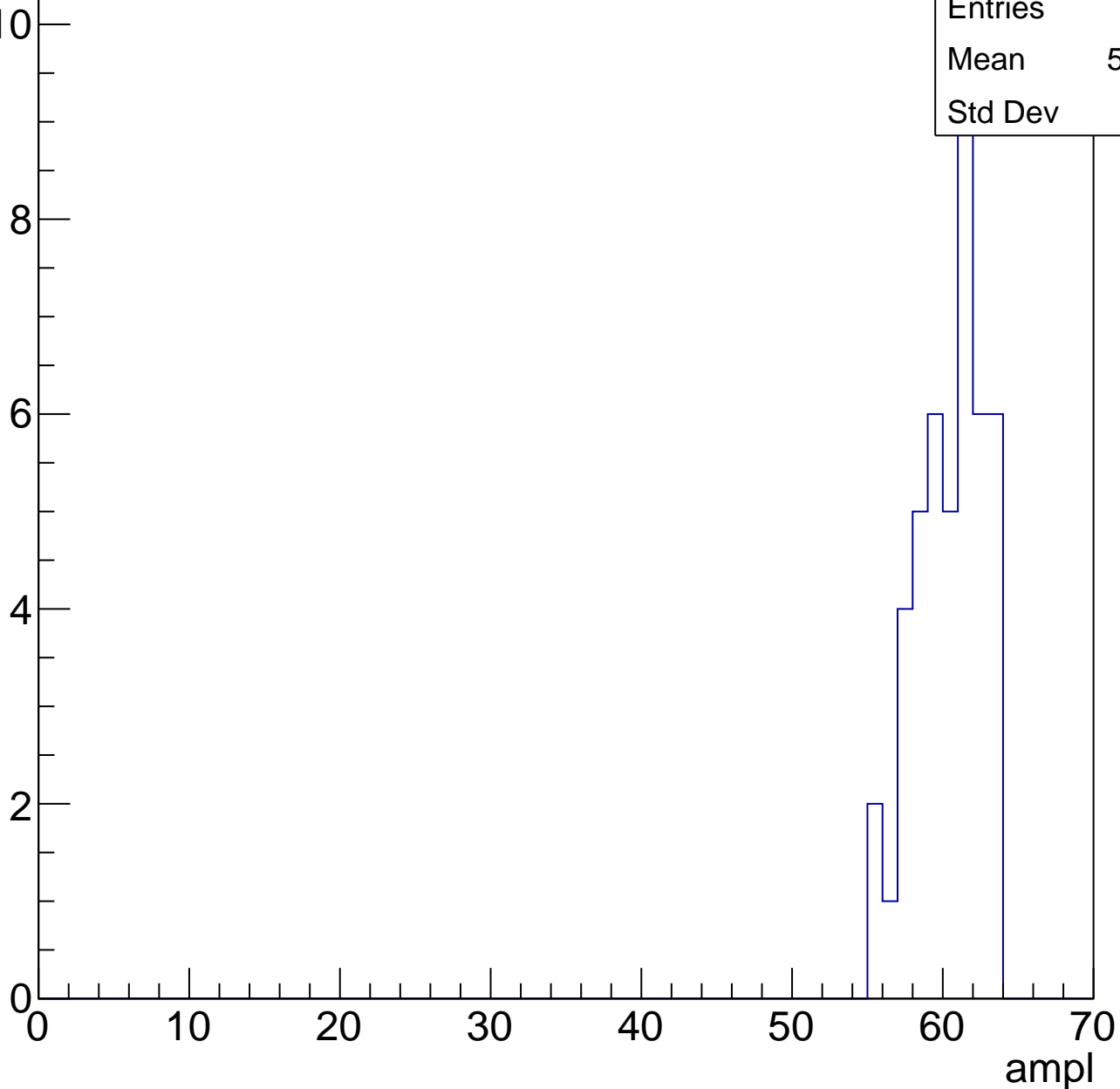


# B0L001S, U5-ch81, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

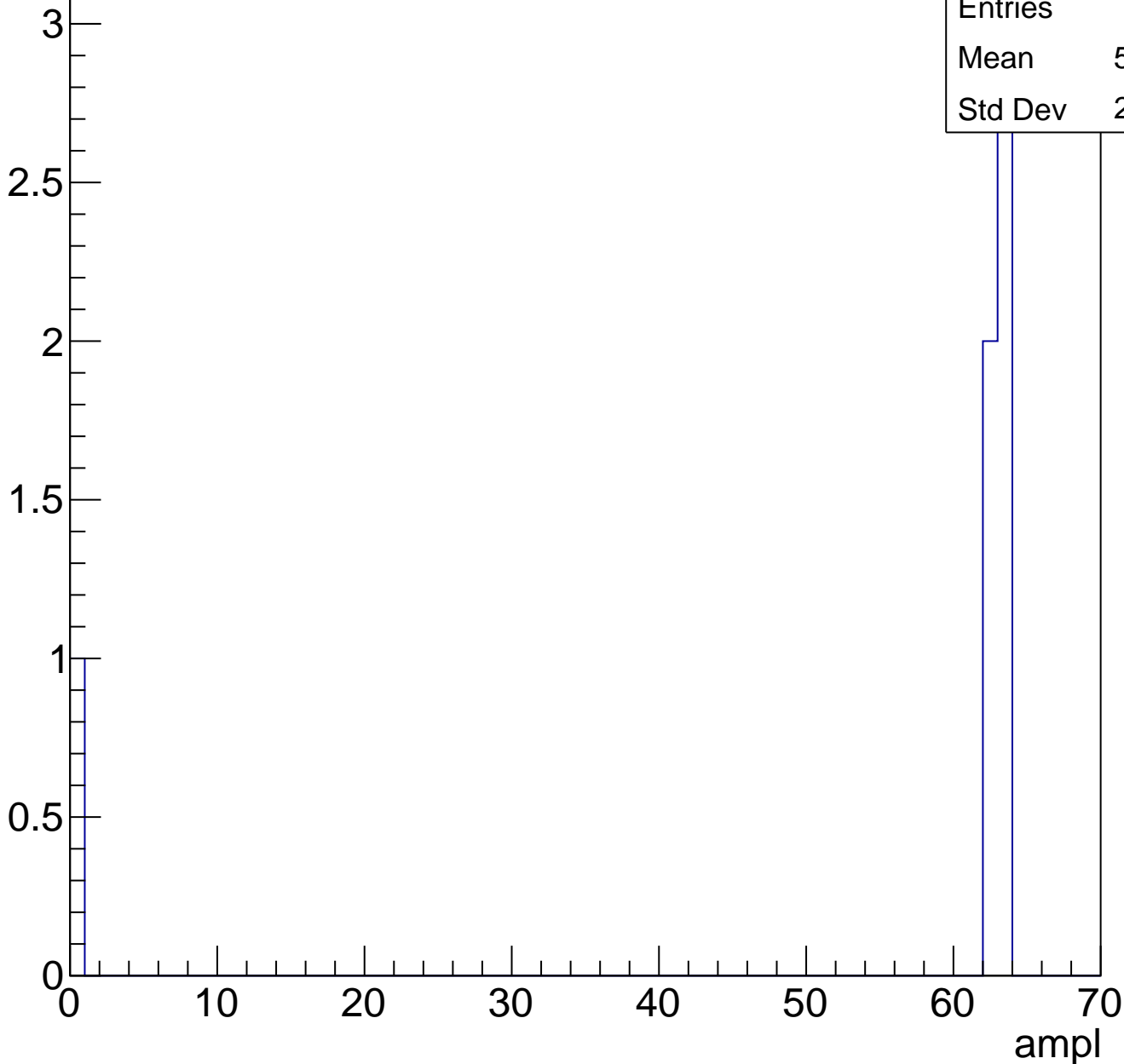
Entries	45
Mean	59.96
Std Dev	2.19



# B0L001S, U5-ch81, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch81, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch82, adc0

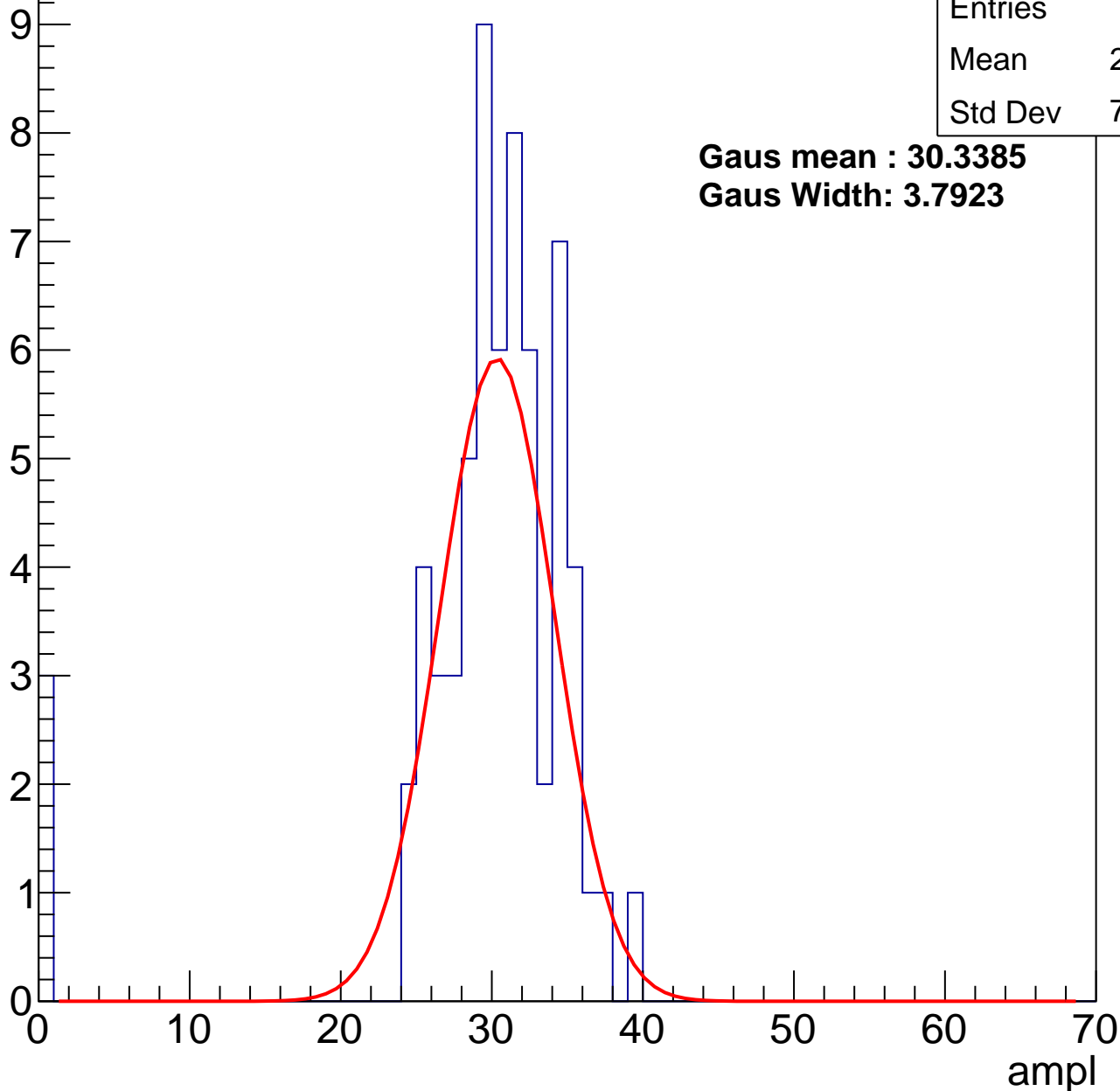
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	28.98
Std Dev	7.165

**Gaus mean : 30.3385**

**Gaus Width: 3.7923**



# B0L001S, U5-ch82, adc1

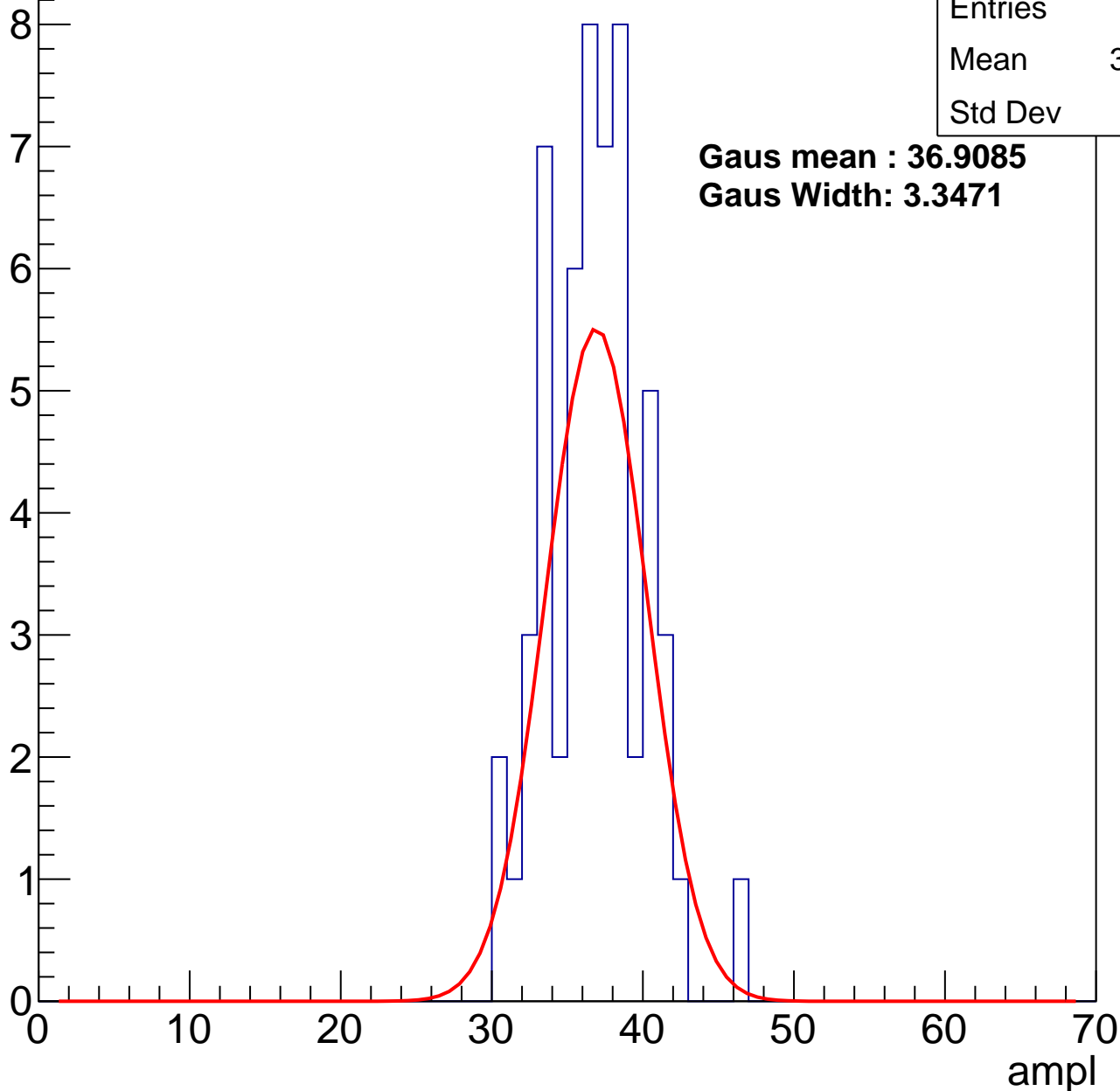
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	36.36
Std Dev	3.17

**Gaus mean : 36.9085**

**Gaus Width: 3.3471**



# B0L001S, U5-ch82, adc2

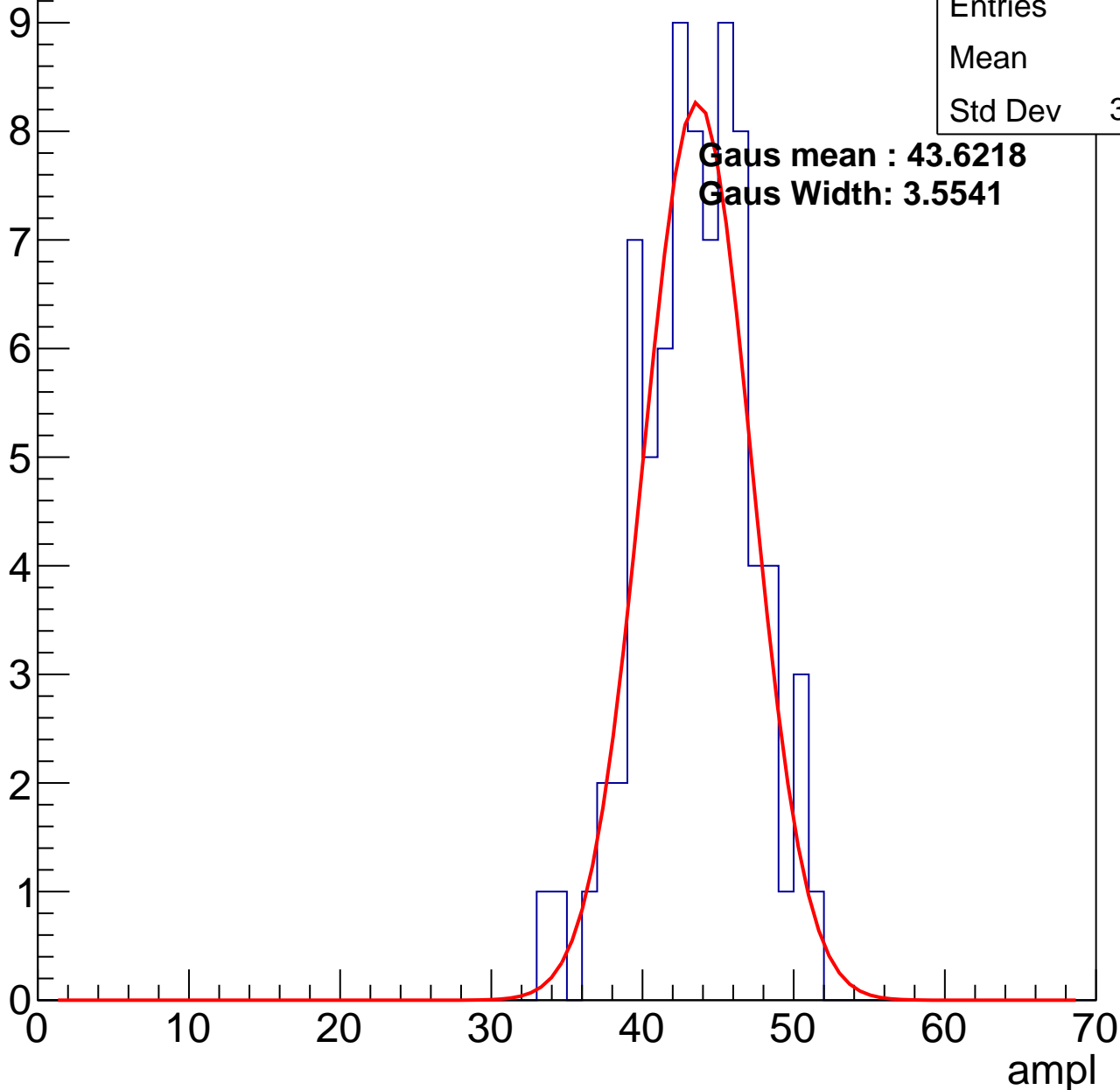
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	79
Mean	43.1
Std Dev	3.675

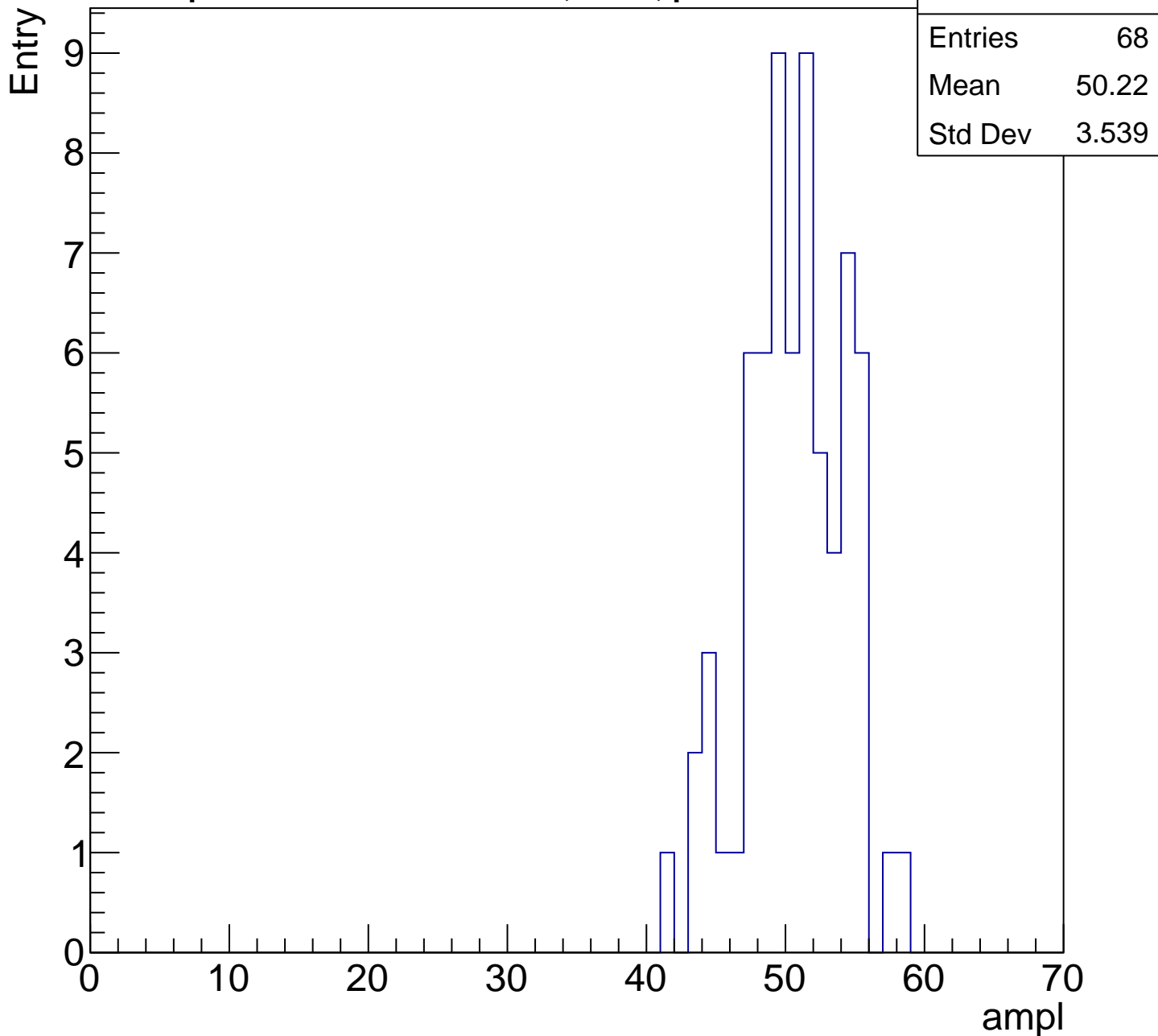
**Gaus mean : 43.6218**

**Gaus Width: 3.5541**



# B0L001S, U5-ch82, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

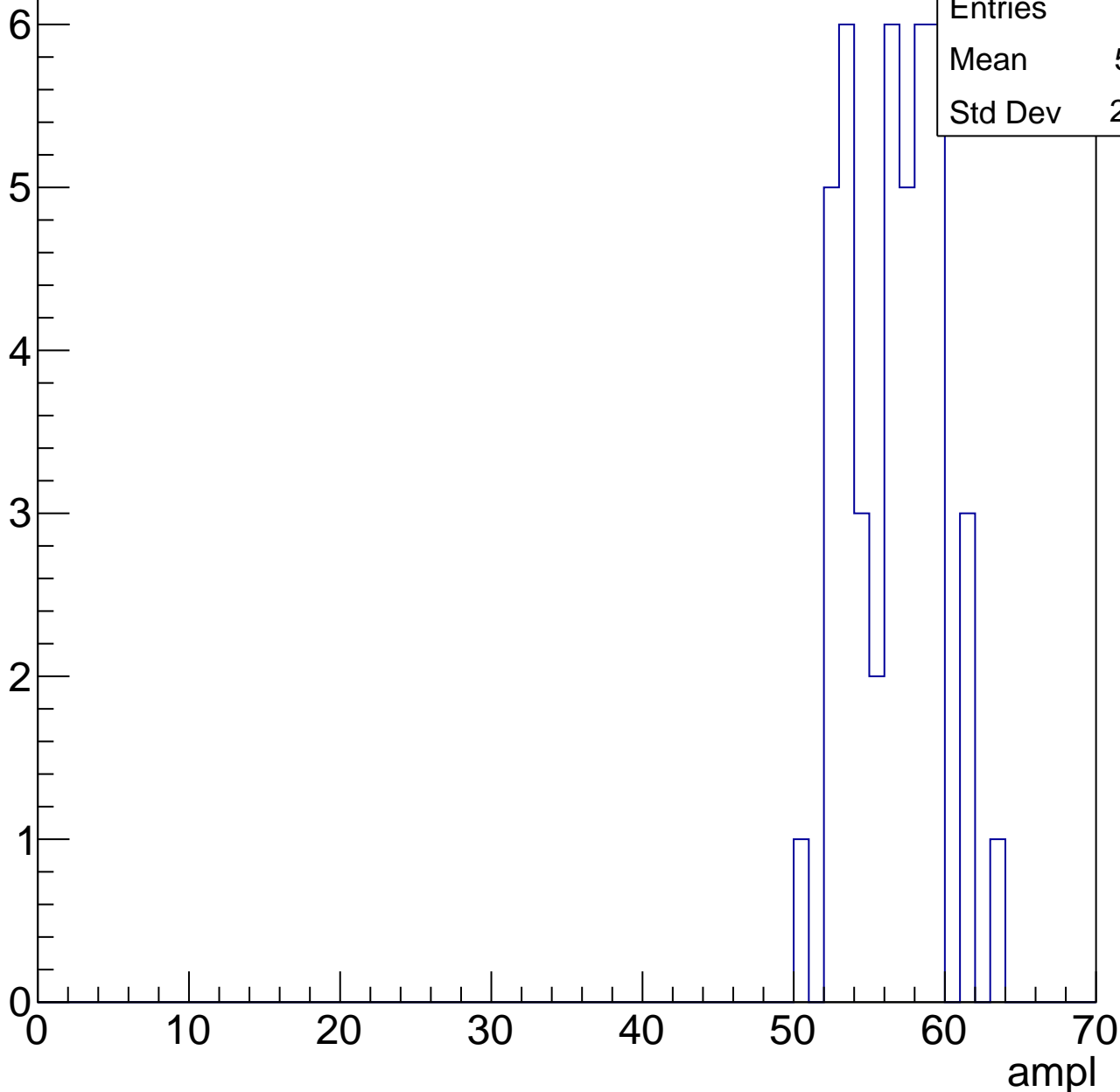


# B0L001S, U5-ch82, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	44
Mean	56.11
Std Dev	2.979

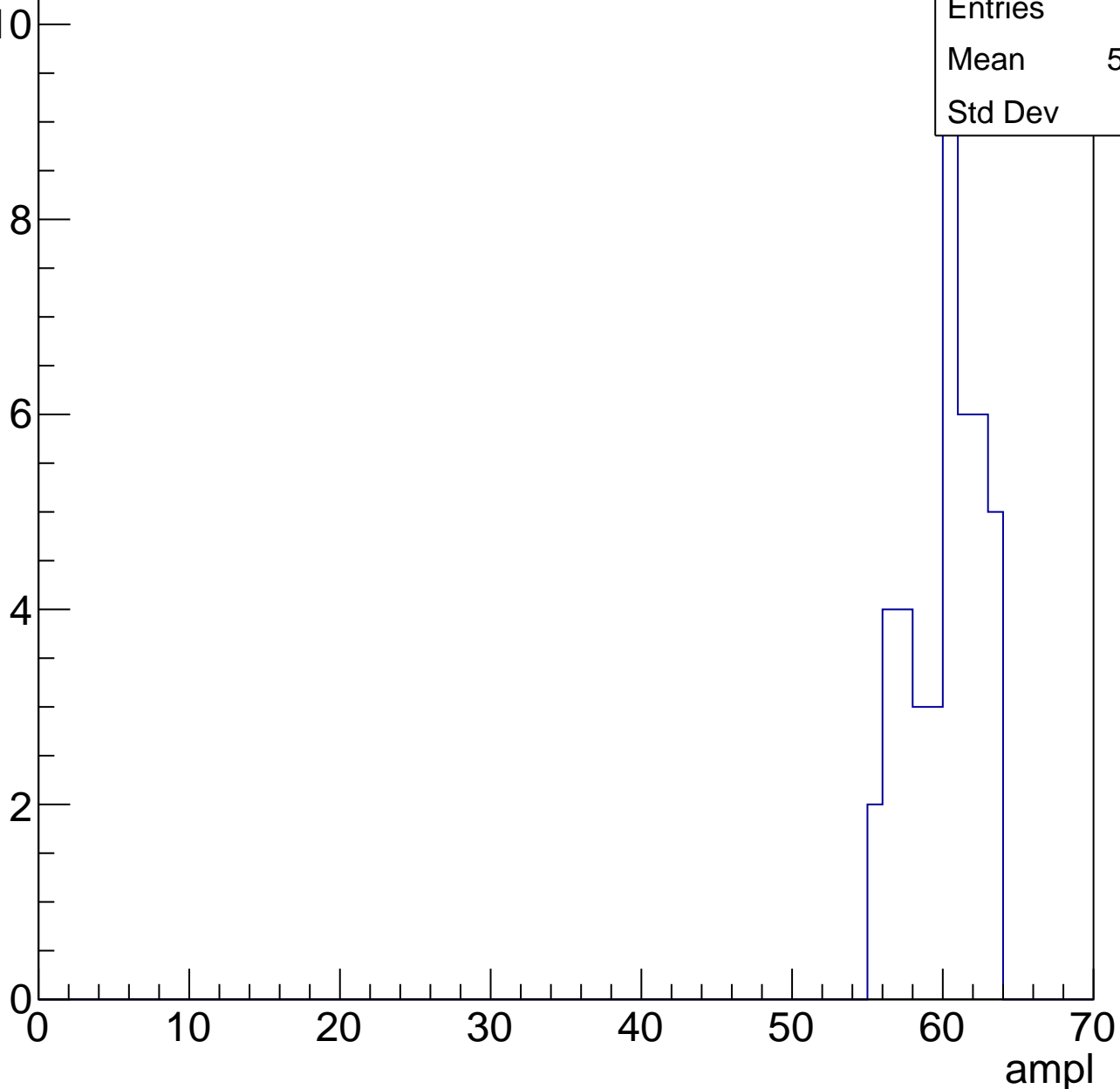


# B0L001S, U5-ch82, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

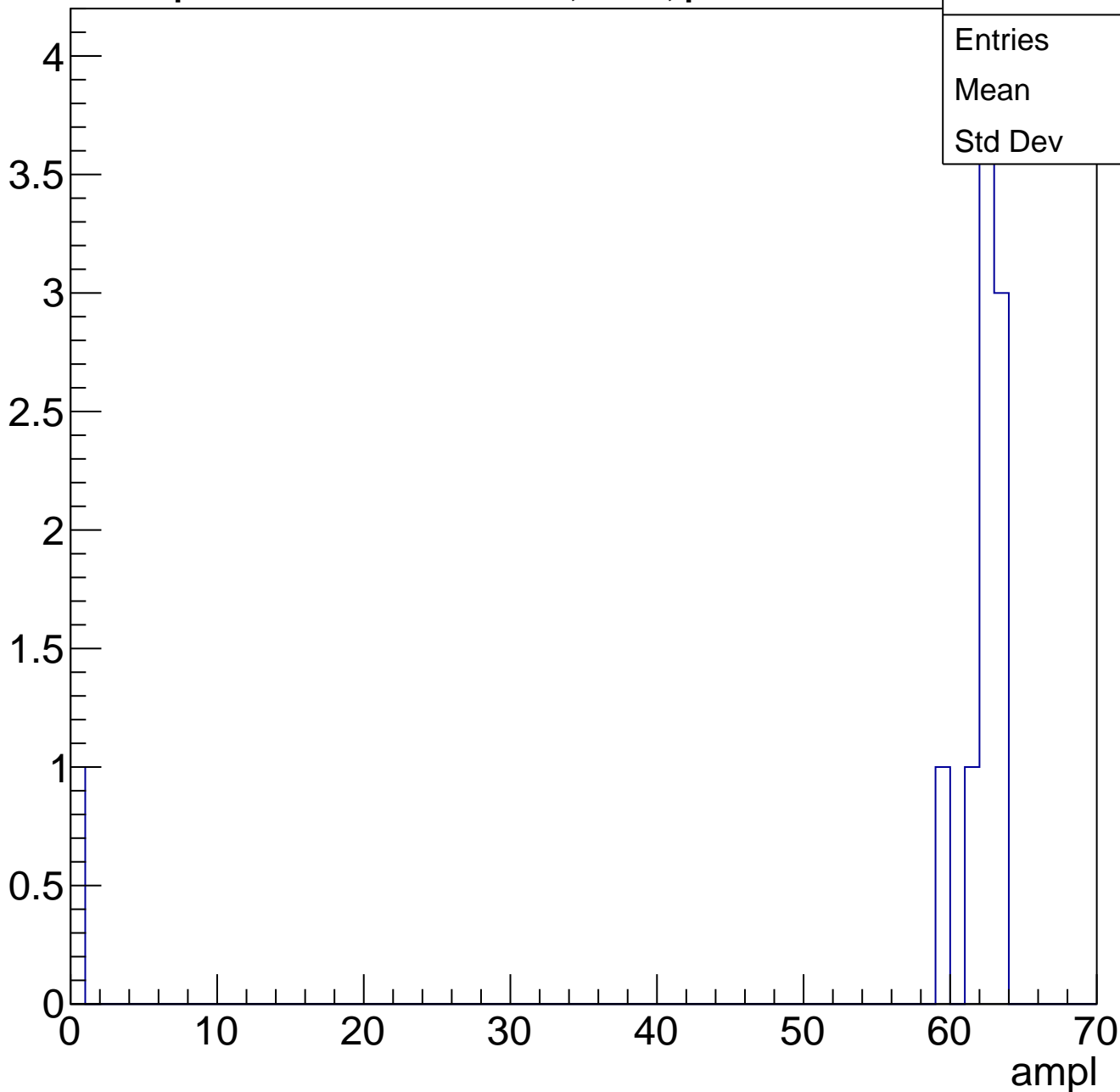
Entries	43
Mean	59.67
Std Dev	2.34



# B0L001S, U5-ch82, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	10
Mean	55.7
Std Dev	18.6



# B0L001S, U5-ch82, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch83, adc0

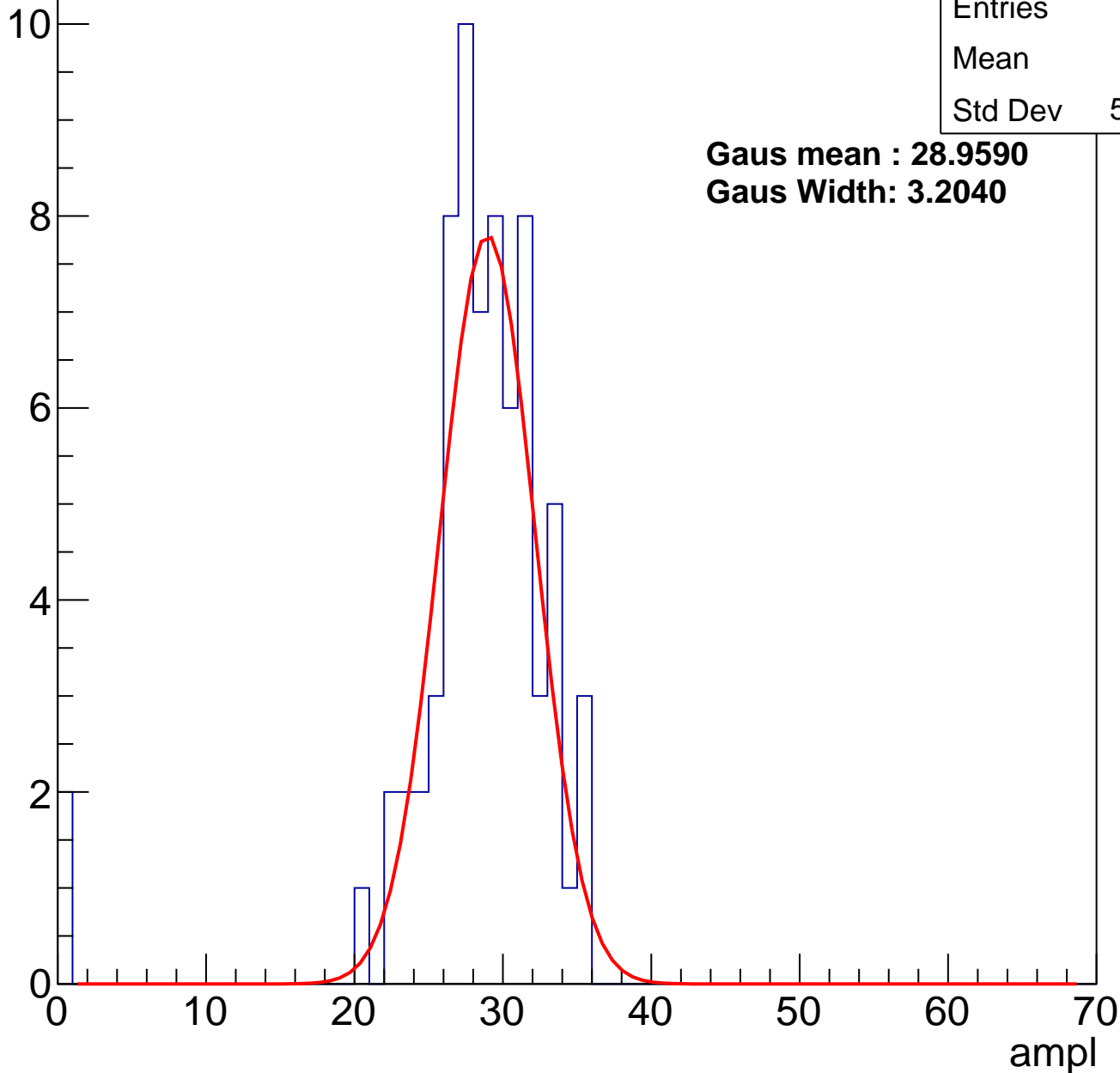
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	71
Mean	27.7
Std Dev	5.702

**Gaus mean : 28.9590**

**Gaus Width: 3.2040**

Entry



# B0L001S, U5-ch83, adc1

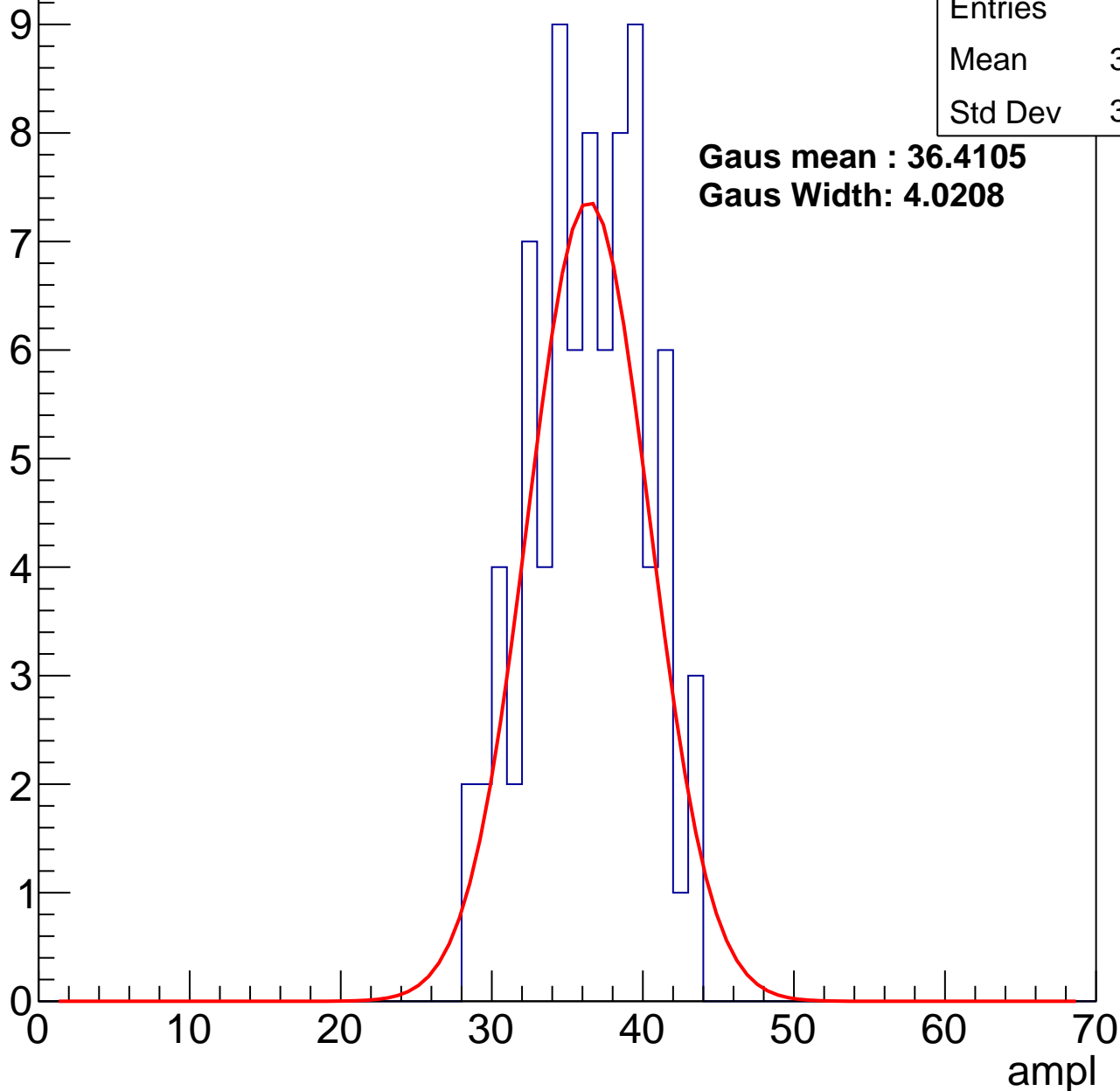
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	81
Mean	35.93
Std Dev	3.728

**Gaus mean : 36.4105**

**Gaus Width: 4.0208**



# B0L001S, U5-ch83, adc2

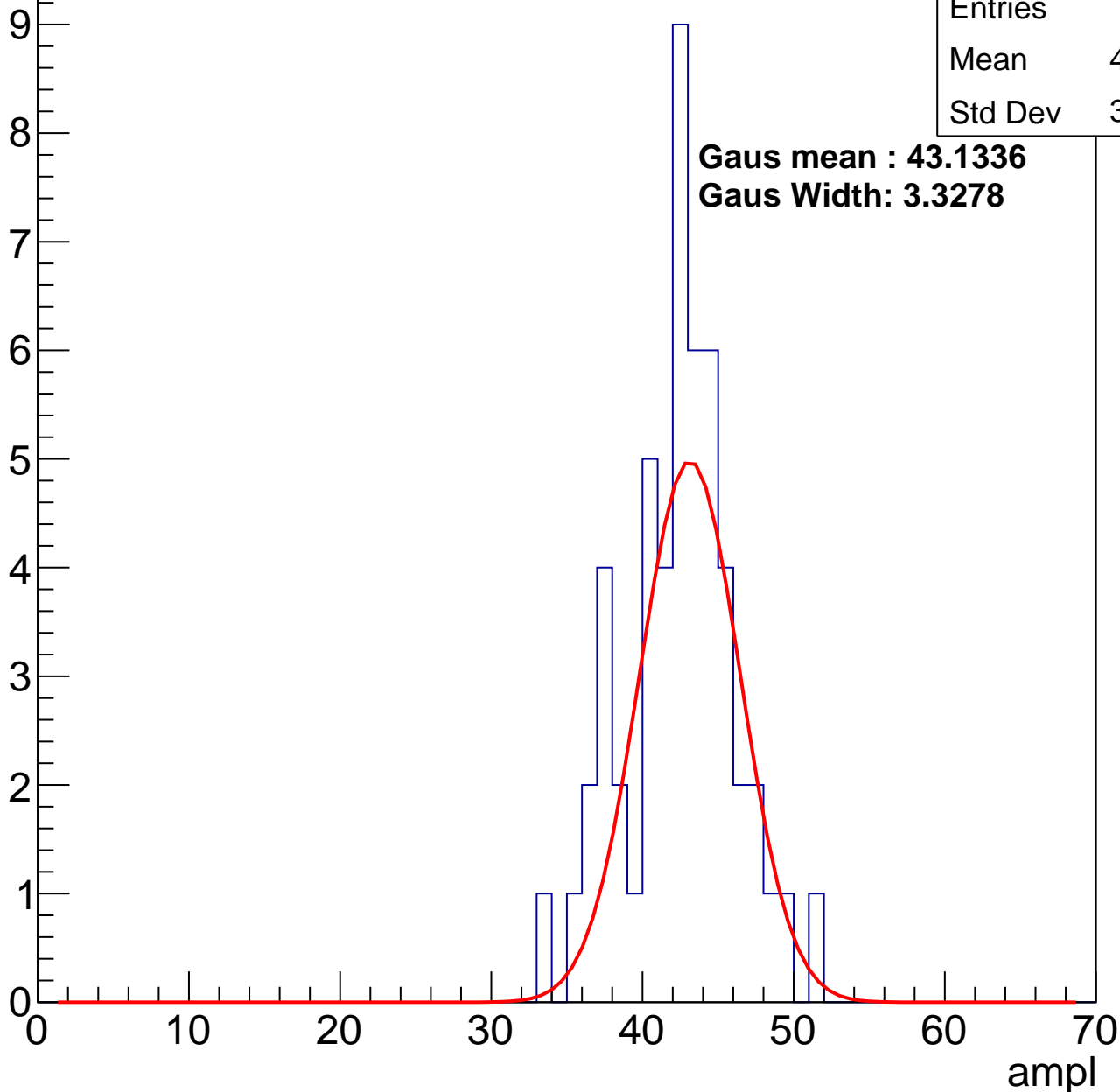
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	41.94
Std Dev	3.618

**Gaus mean : 43.1336**

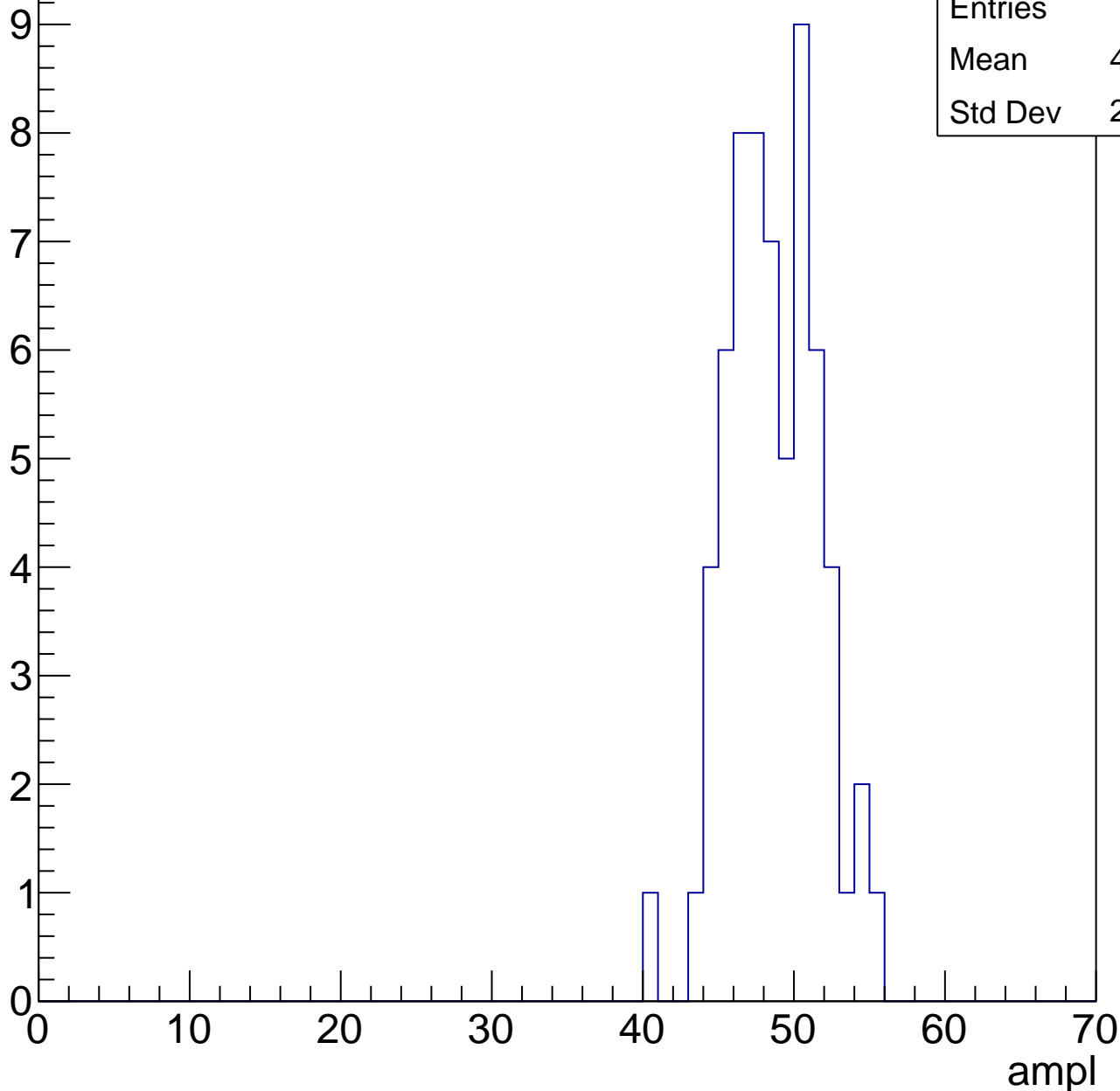
**Gaus Width: 3.3278**



# B0L001S, U5-ch83, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



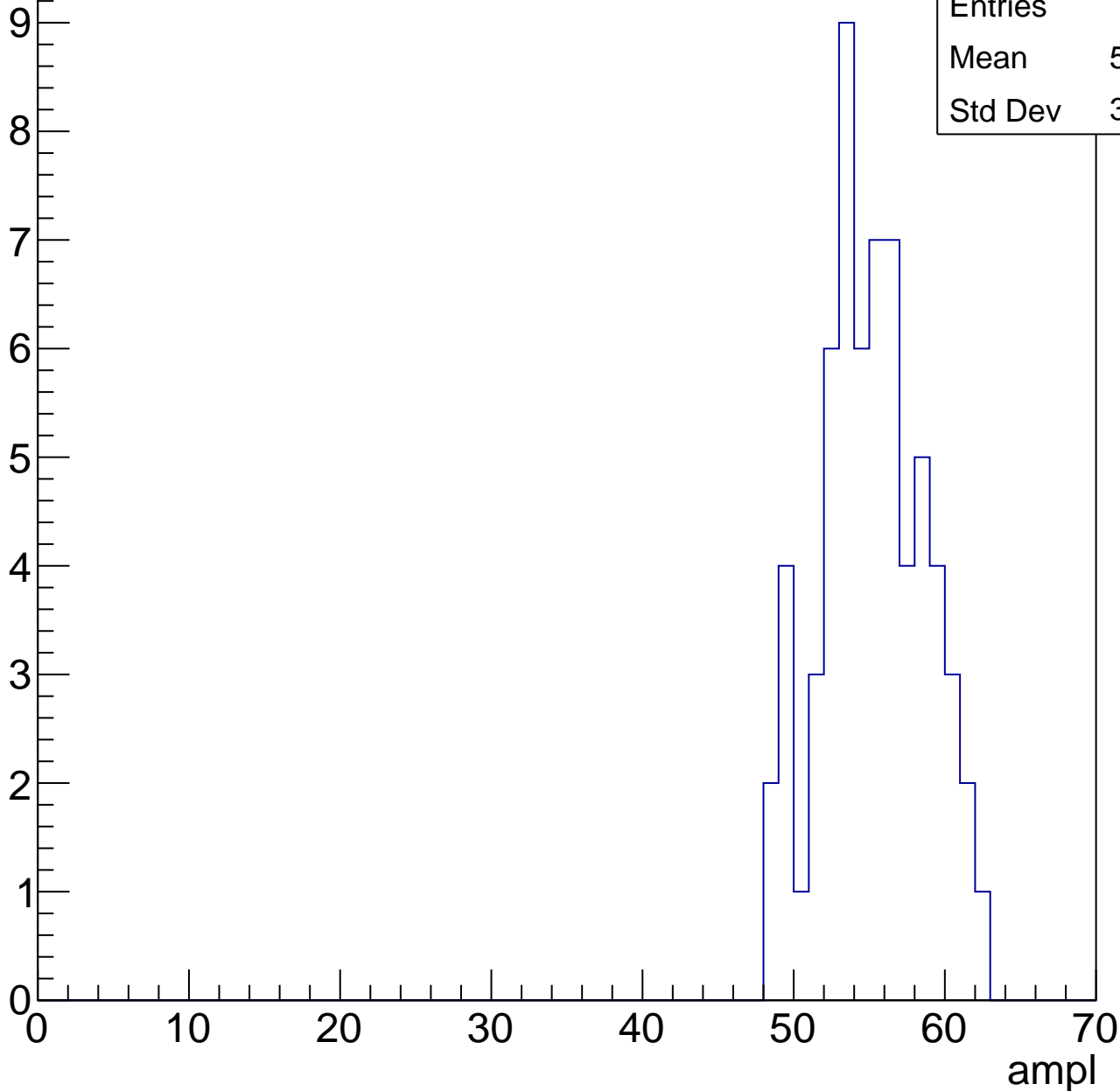
Entries	63
Mean	48.16
Std Dev	2.956

# B0L001S, U5-ch83, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	54.73
Std Dev	3.388



# B0L001S, U5-ch83, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

7

6

5

4

3

2

1

0

Entries	50
Mean	59.48
Std Dev	2.586

ampl

0

10

20

30

40

50

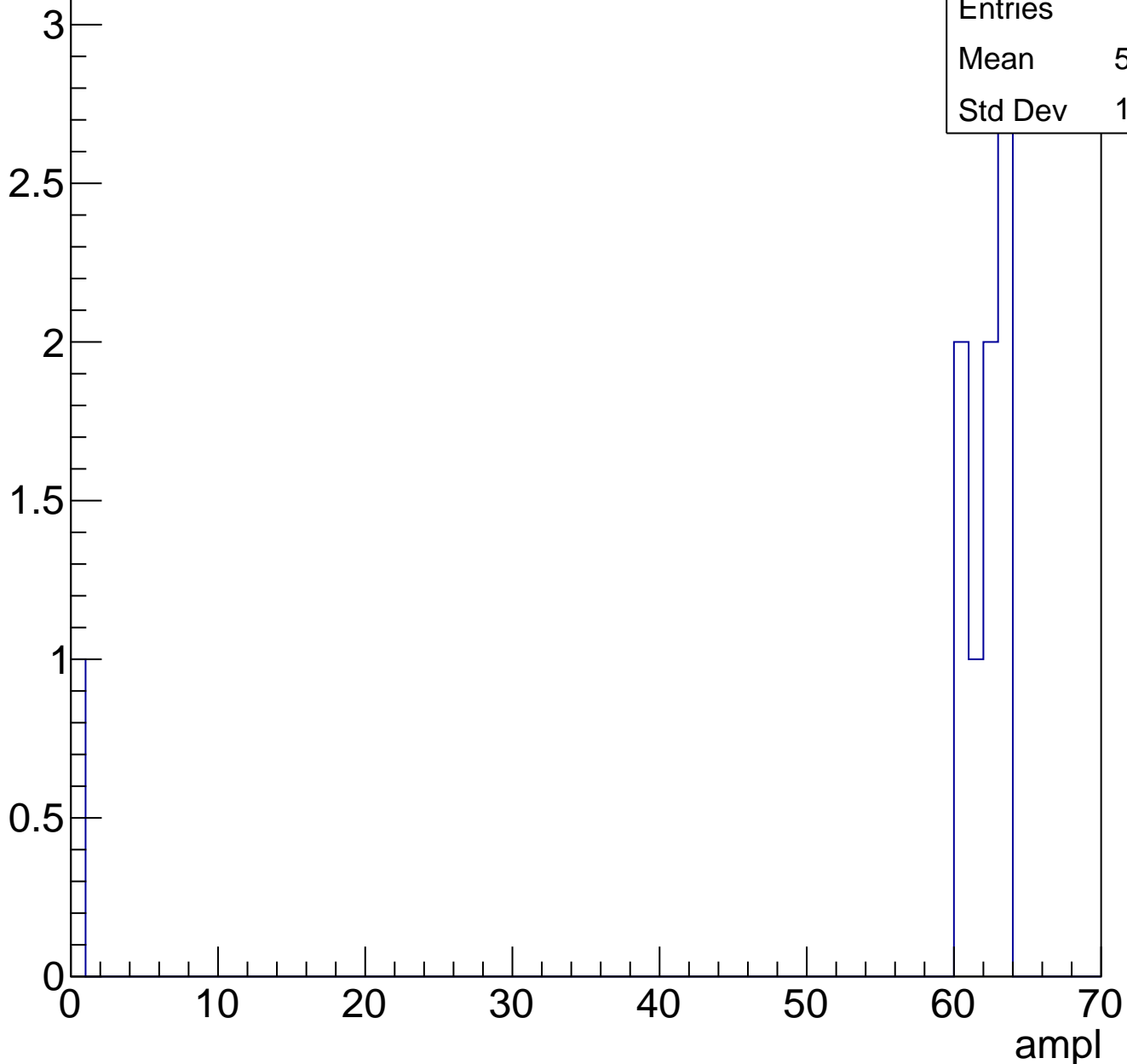
60

70

# B0L001S, U5-ch83, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	9
Mean	54.89
Std Dev	19.44



# B0L001S, U5-ch83, adc7

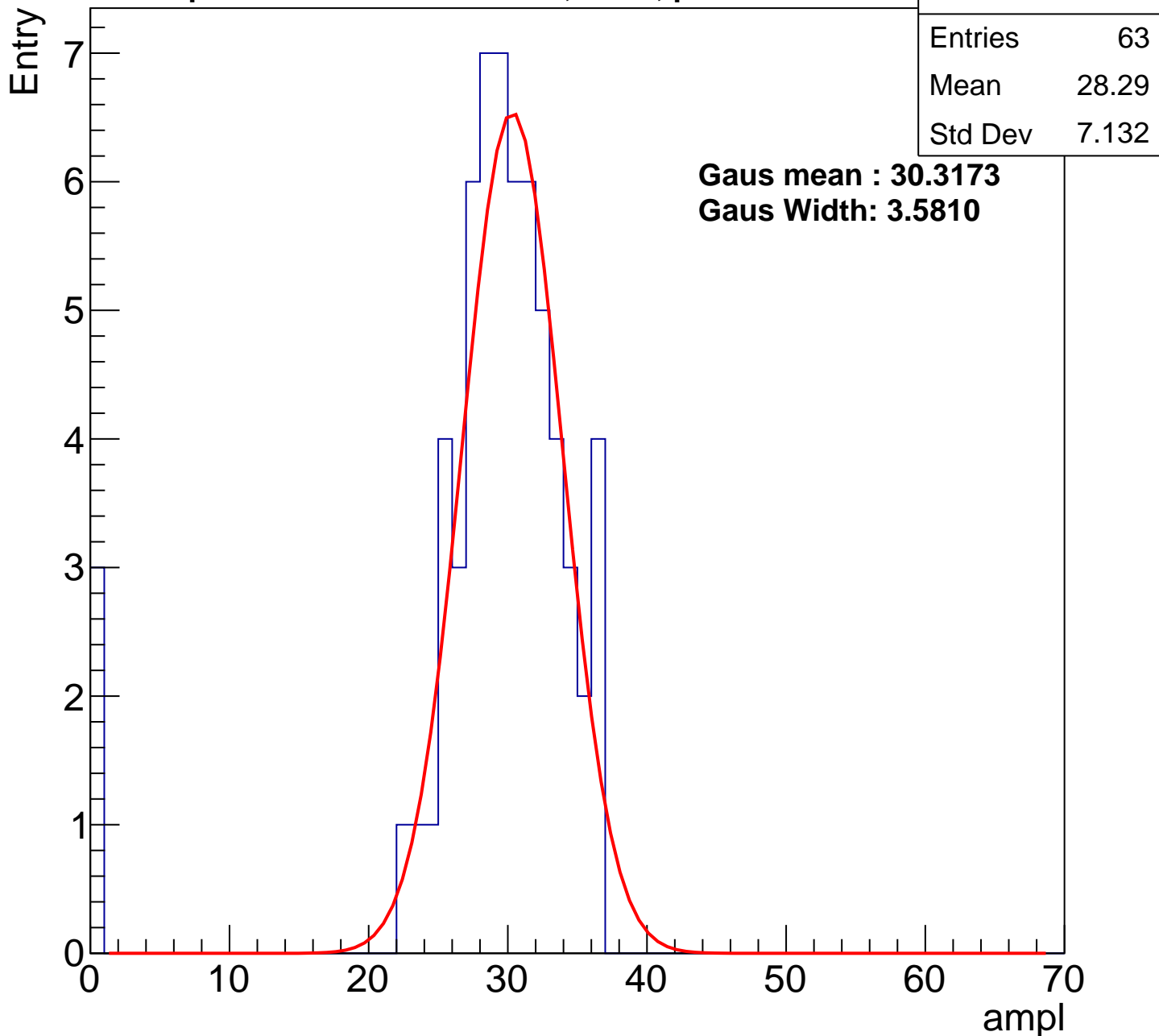
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch84, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U5-ch84, adc1

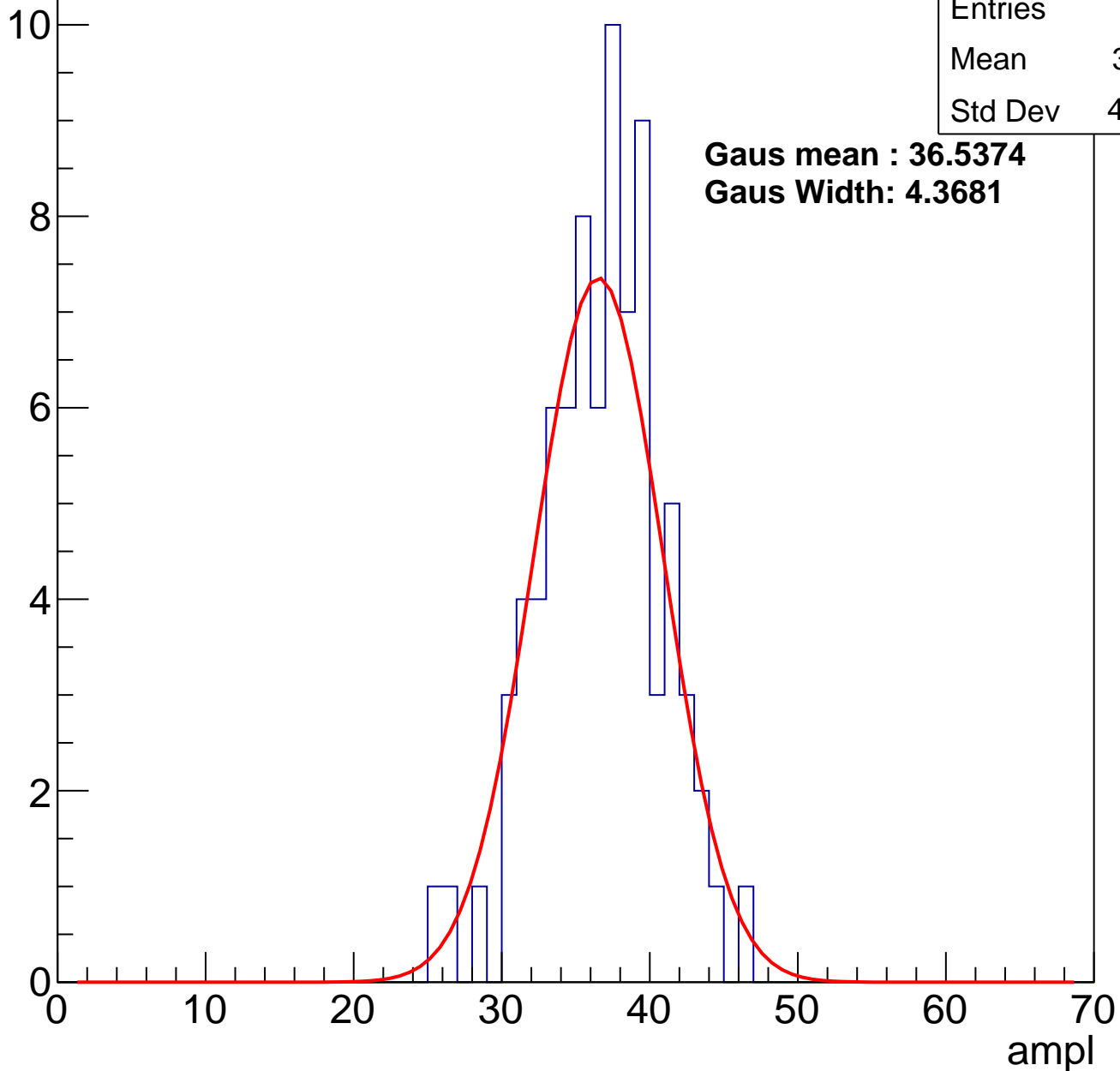
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	81
Mean	36.21
Std Dev	4.008

**Gaus mean : 36.5374**

**Gaus Width: 4.3681**

Entry



# B0L001S, U5-ch84, adc2

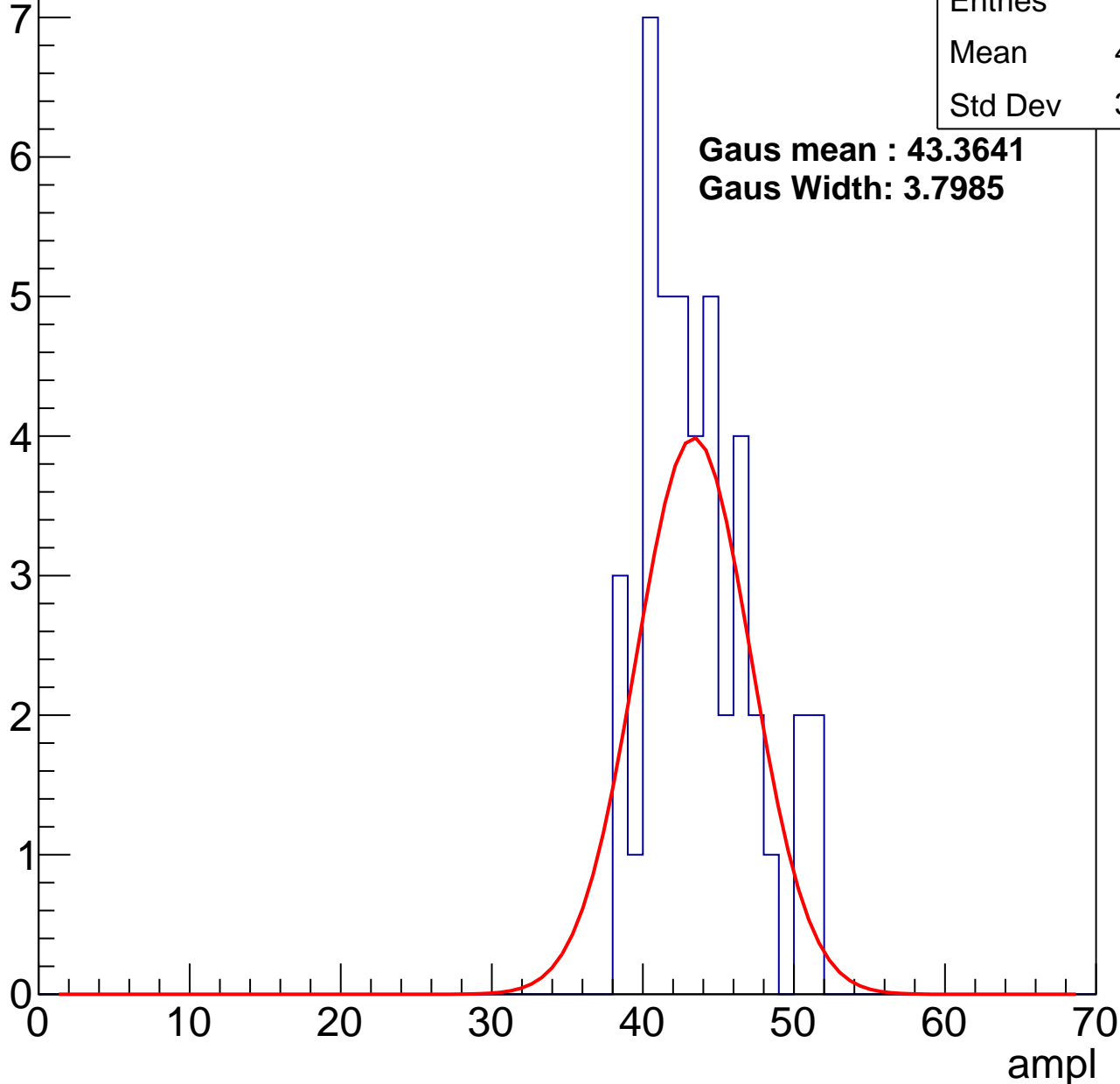
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	43
Mean	43.21
Std Dev	3.441

**Gaus mean : 43.3641**

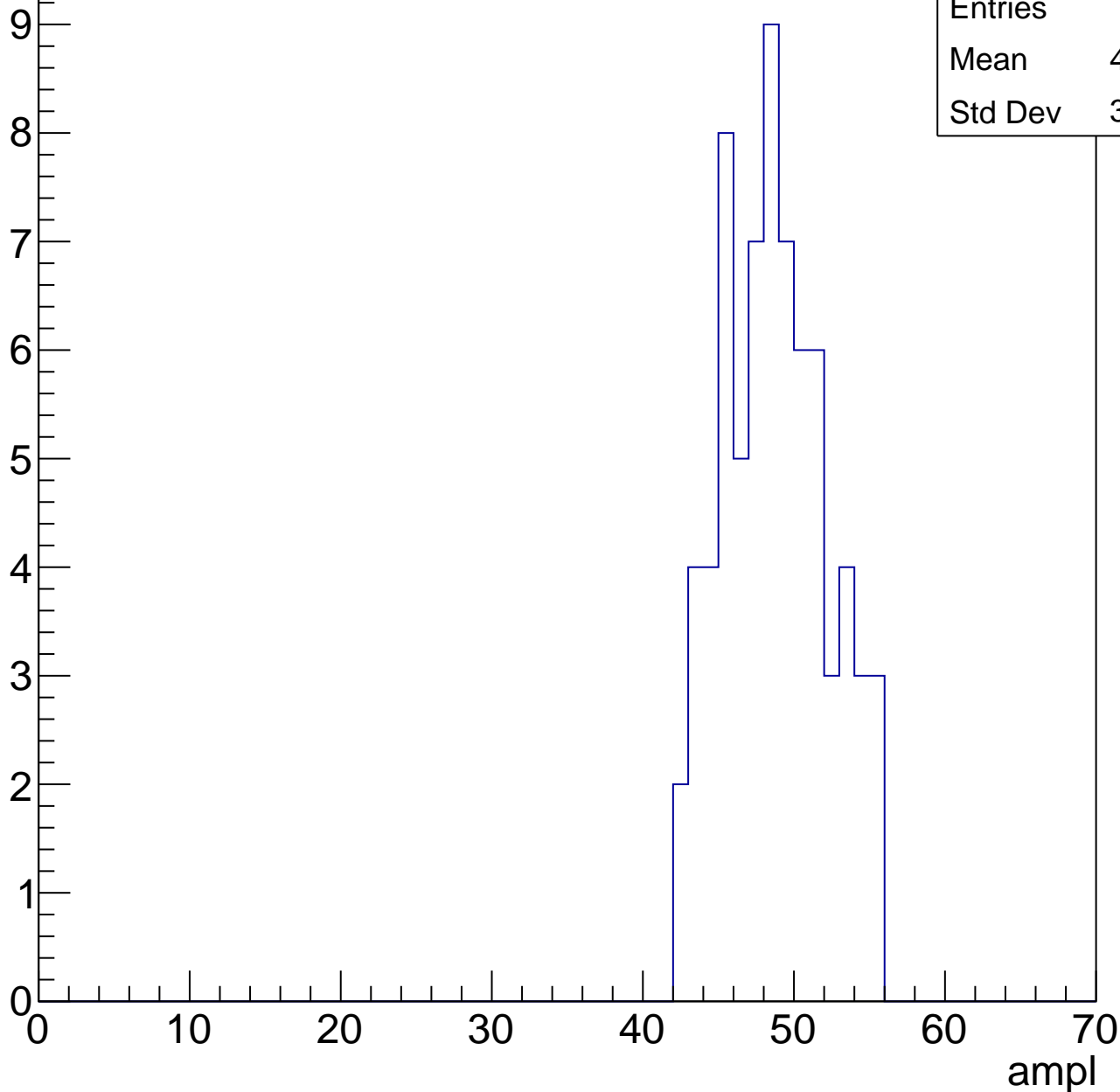
**Gaus Width: 3.7985**



# B0L001S, U5-ch84, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

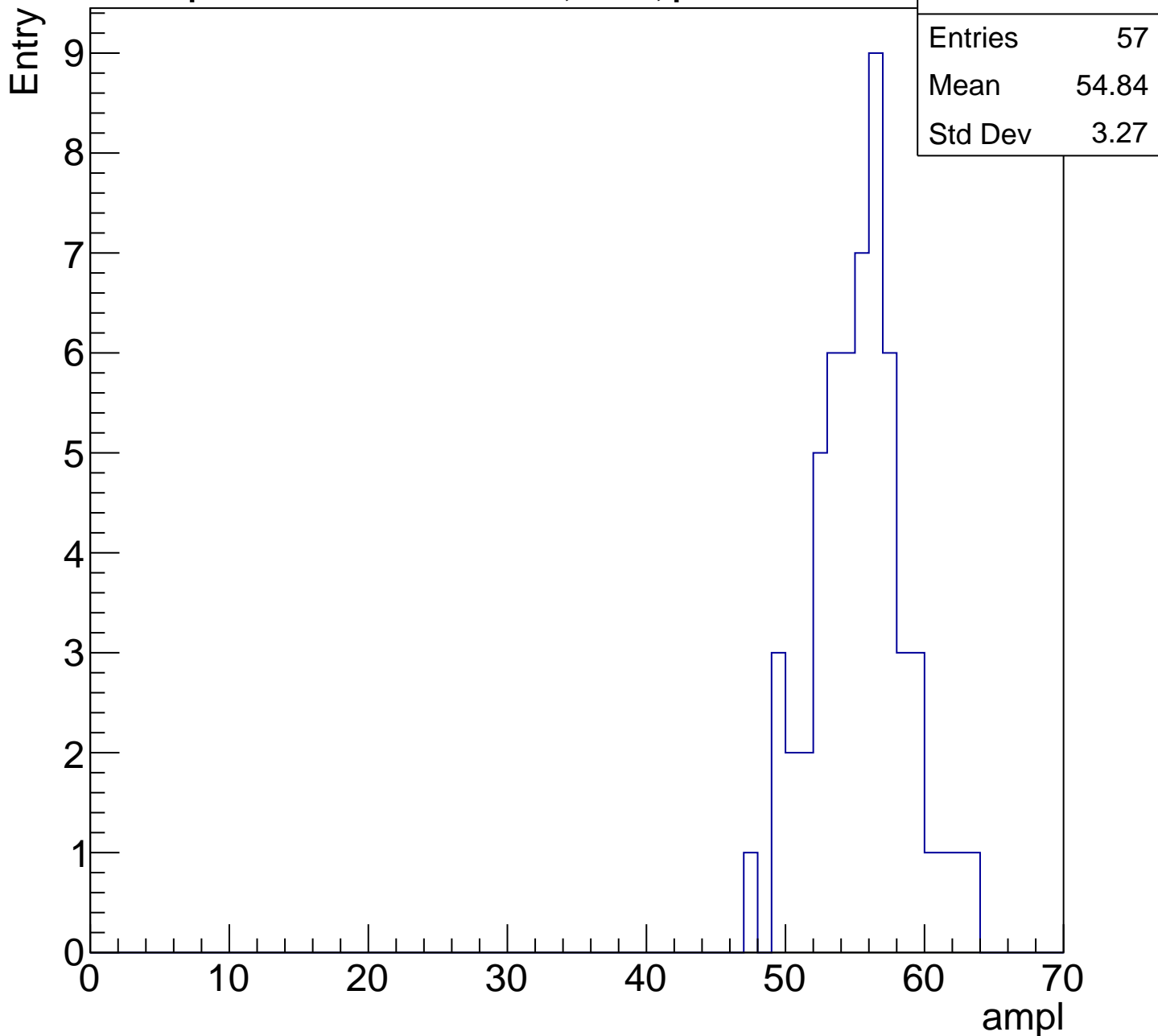
Entry



Entries	71
Mean	48.27
Std Dev	3.394

# B0L001S, U5-ch84, adc4

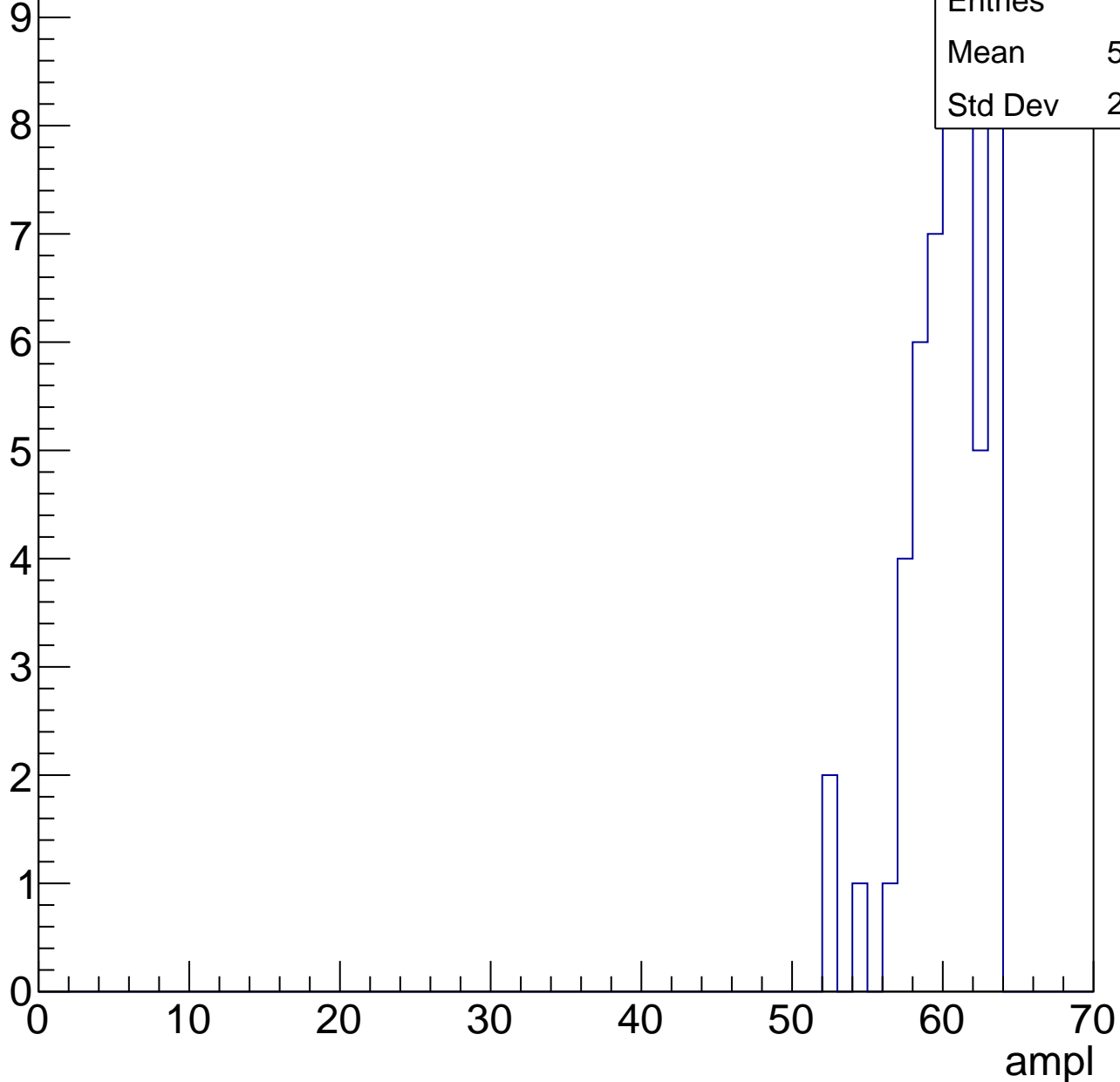
calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U5-ch84, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

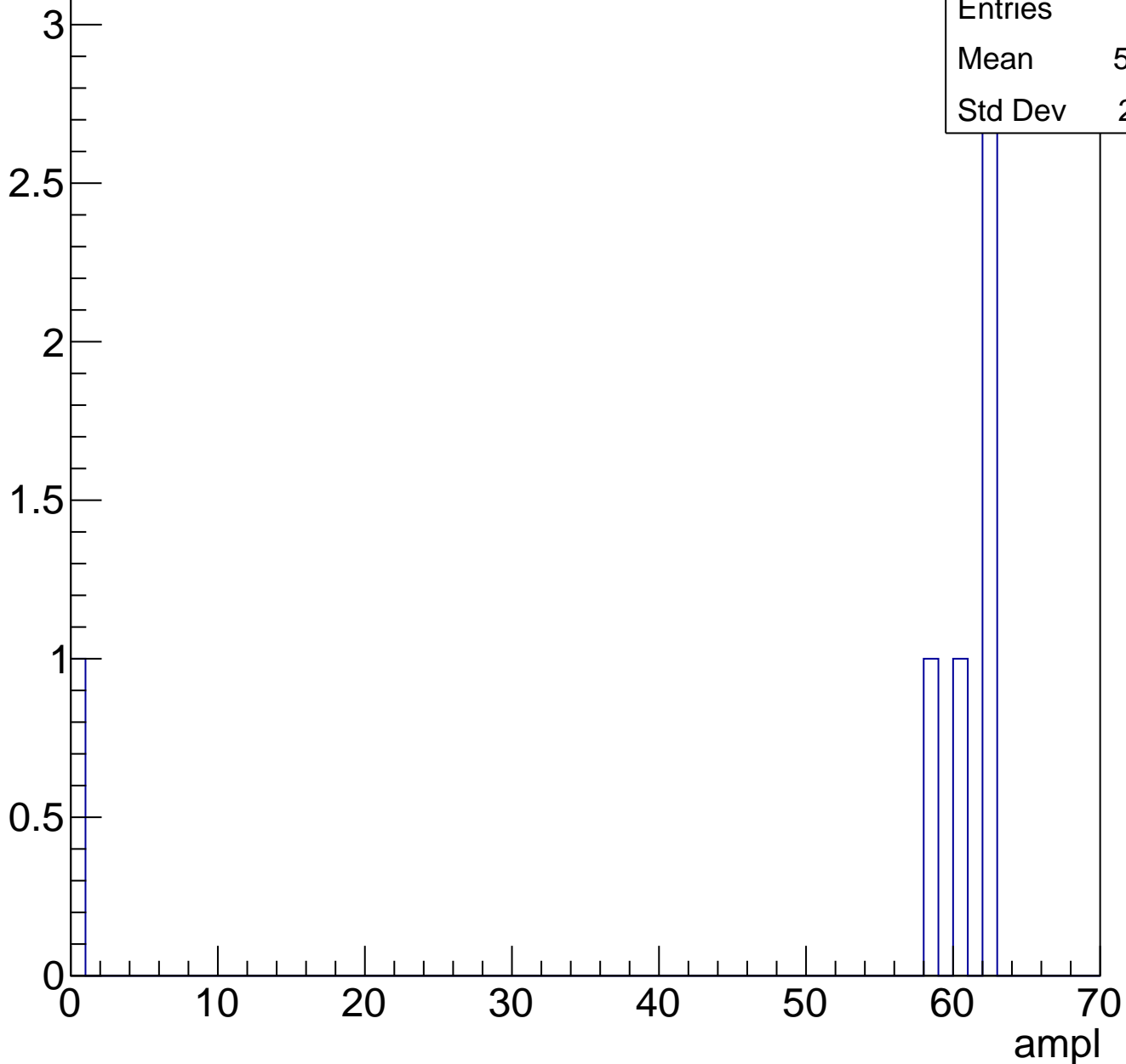
Entry



# B0L001S, U5-ch84, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

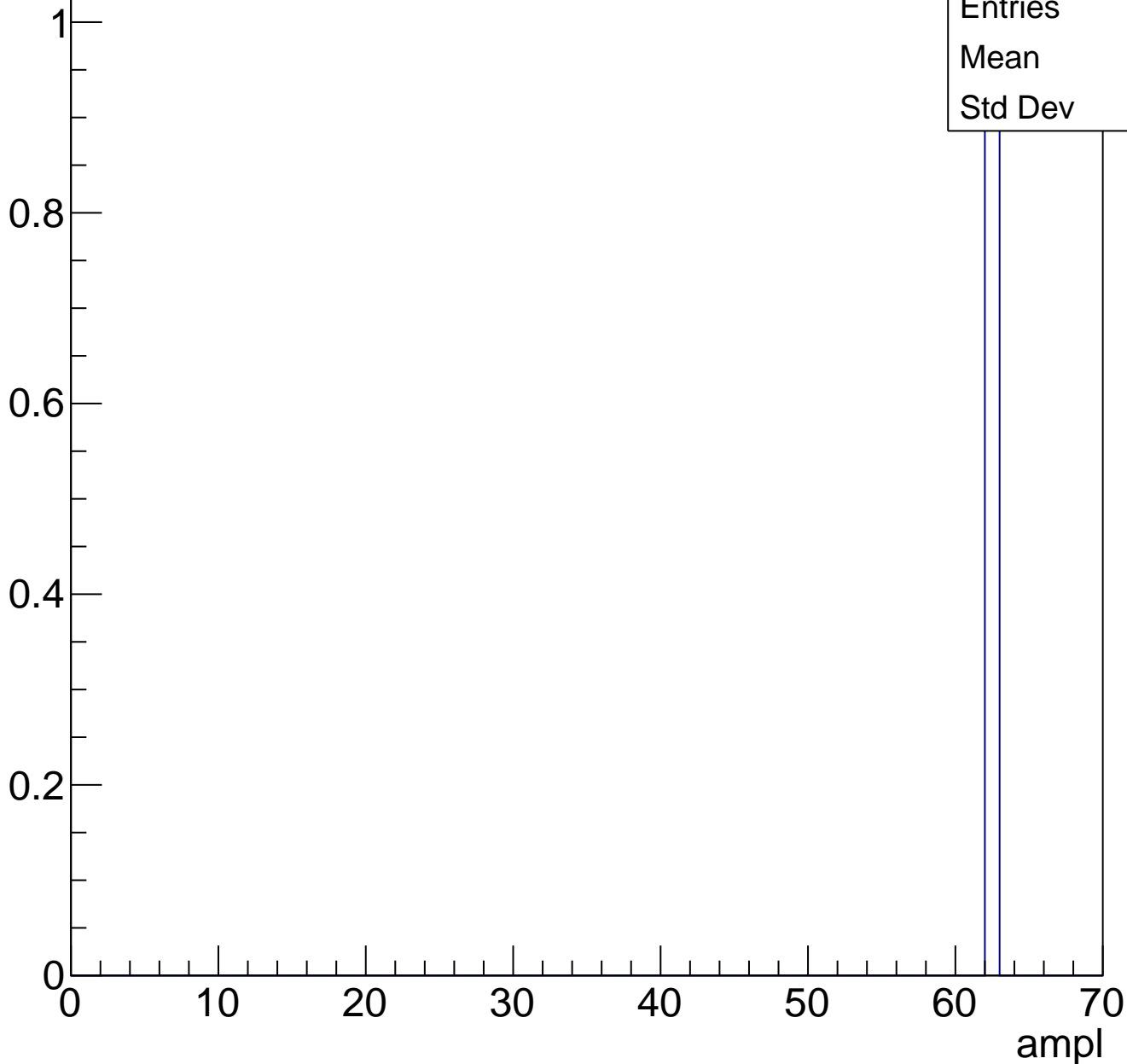




# B0L001S, U5-ch84, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch85, adc0

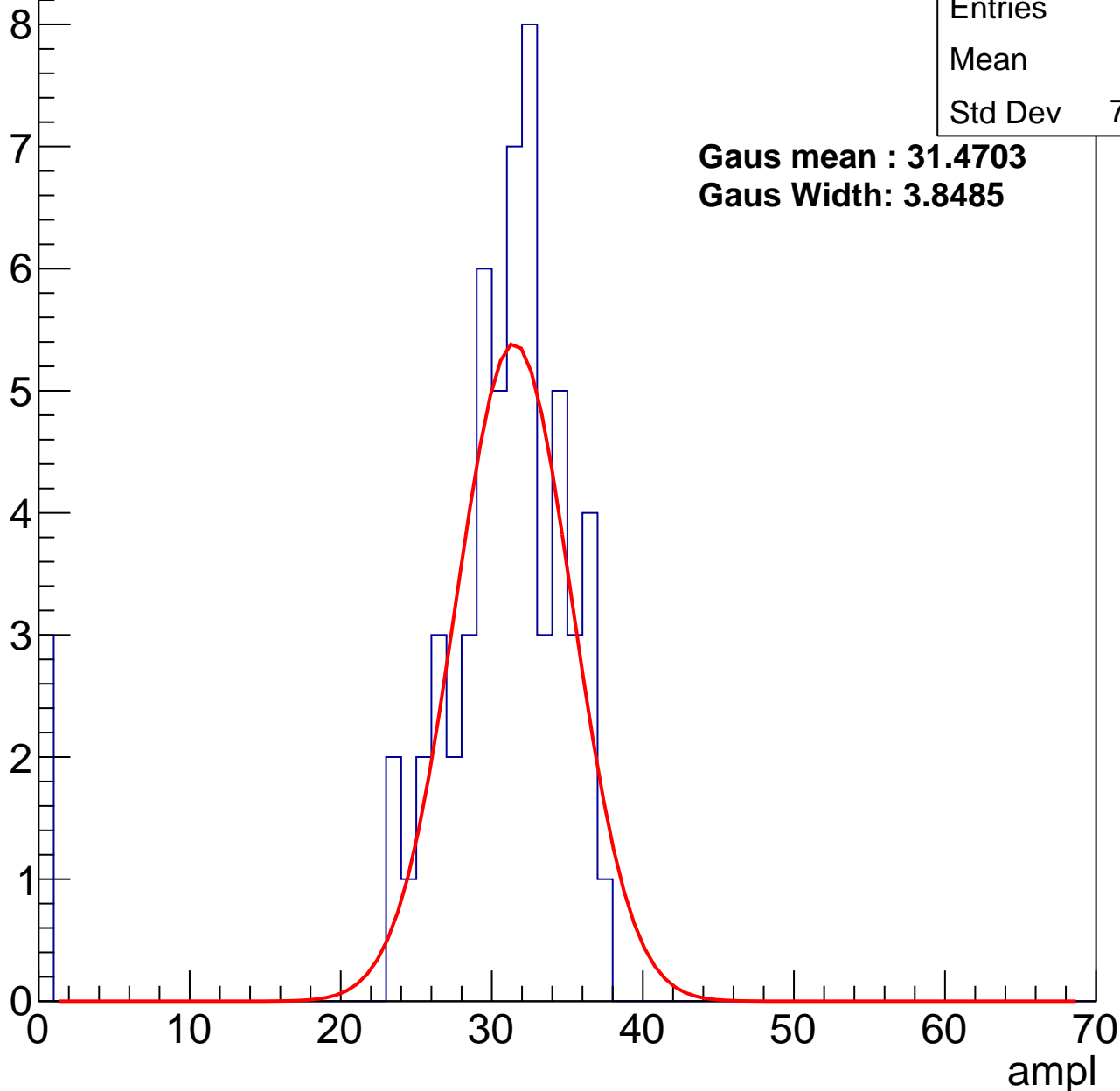
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	29.1
Std Dev	7.583

**Gaus mean : 31.4703**

**Gaus Width: 3.8485**



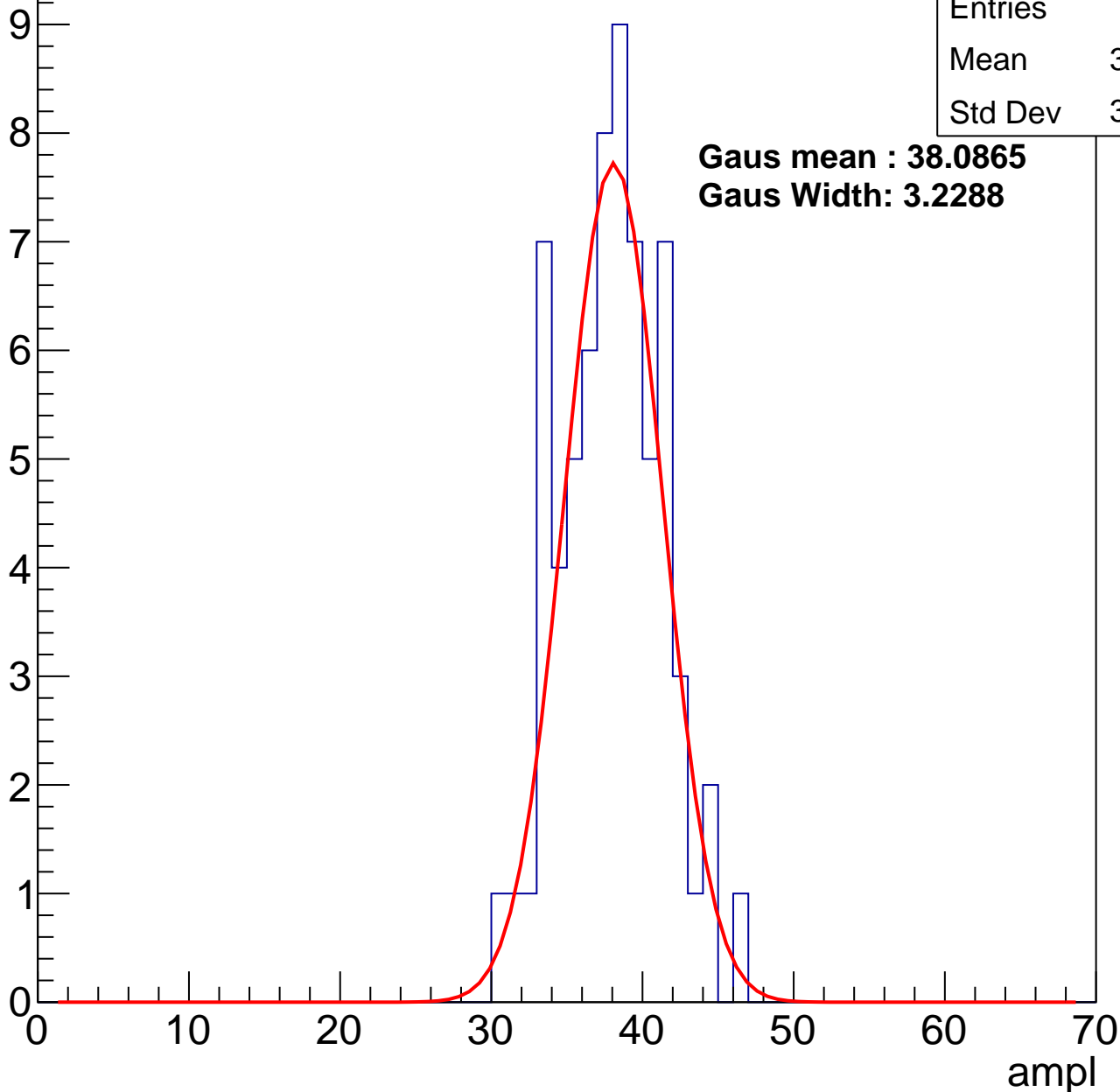
# B0L001S, U5-ch85, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	37.53
Std Dev	3.319

**Gaus mean : 38.0865**  
**Gaus Width: 3.2288**



# B0L001S, U5-ch85, adc2

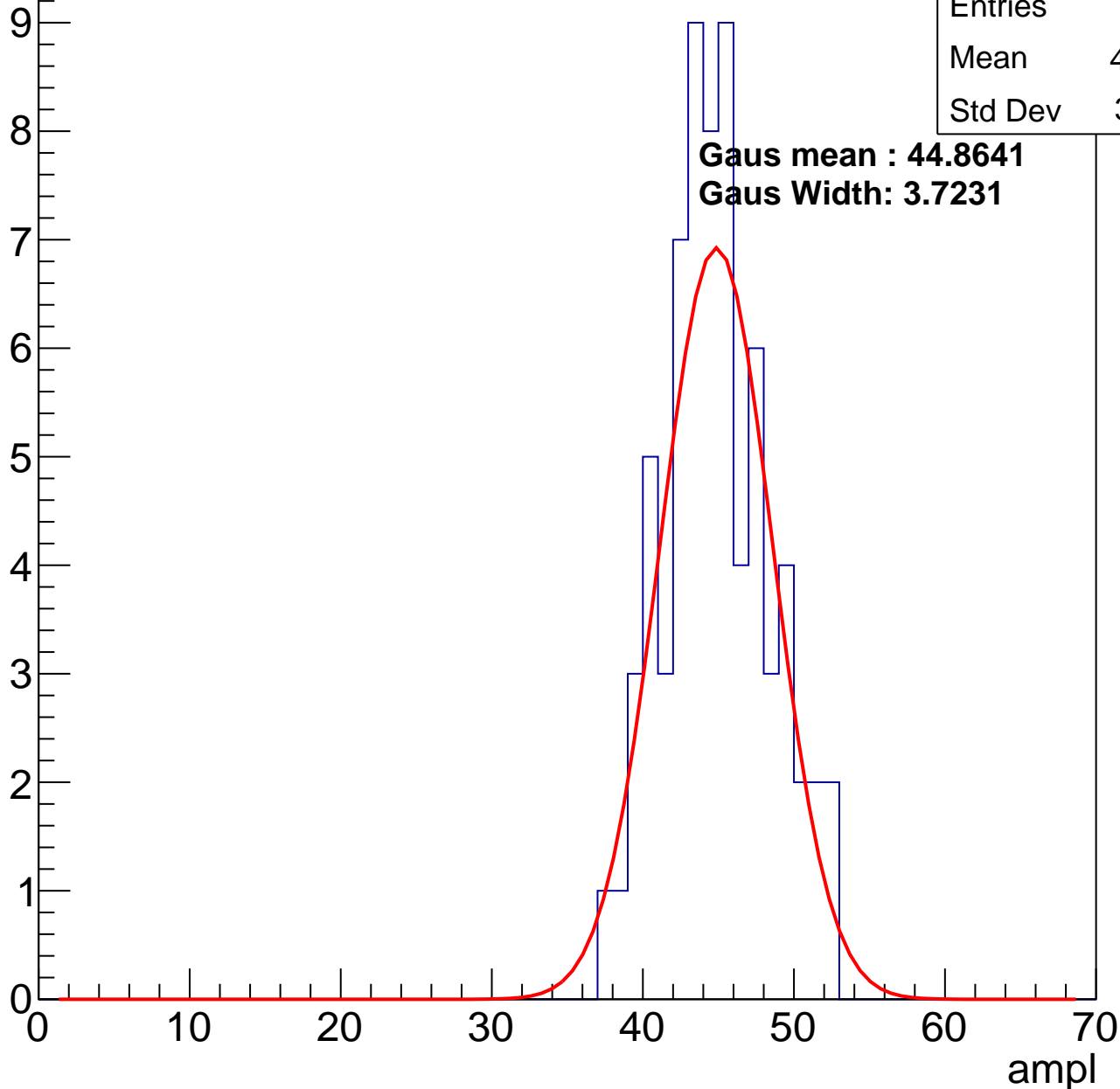
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	44.42
Std Dev	3.441

**Gaus mean : 44.8641**

**Gaus Width: 3.7231**

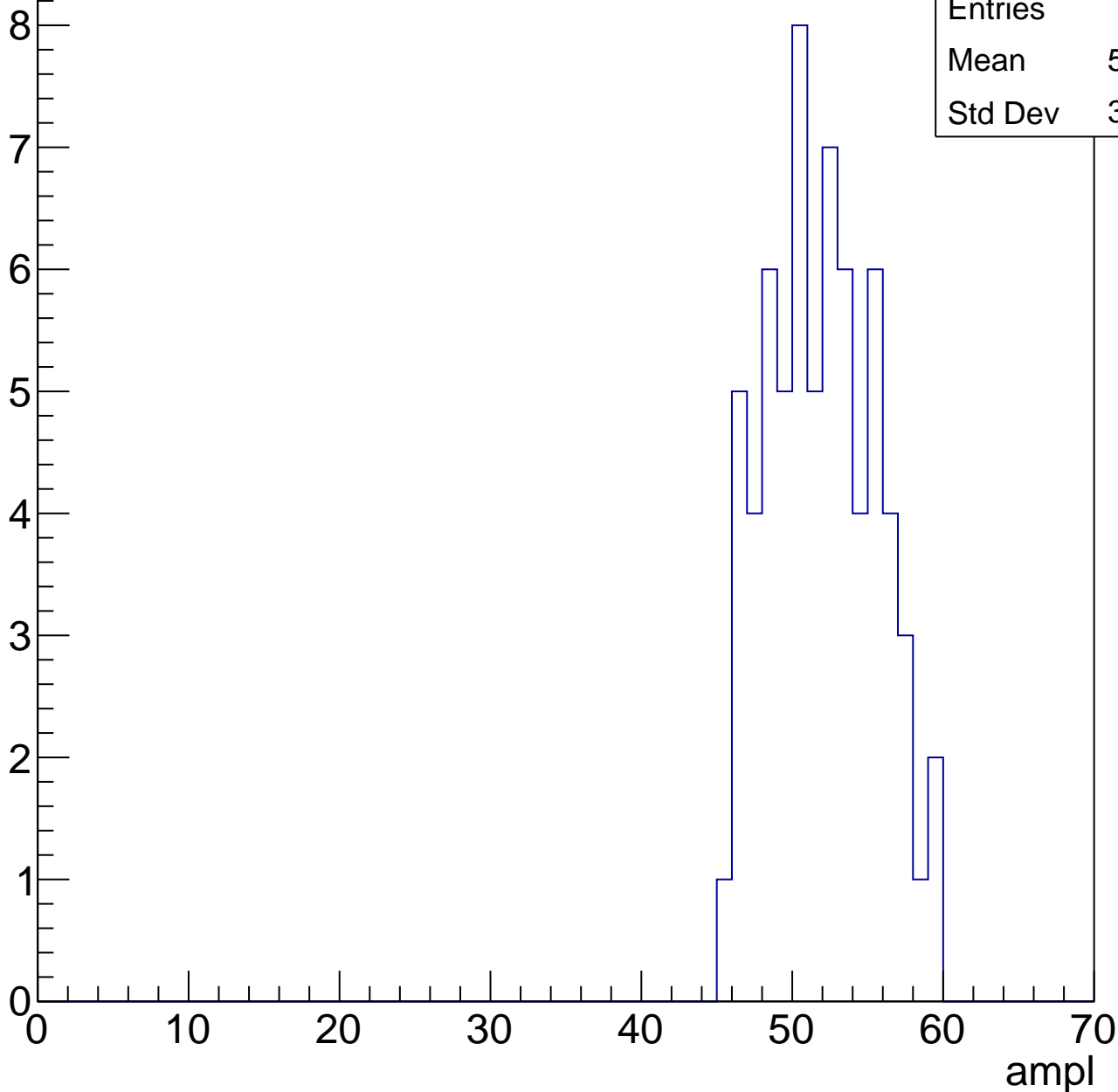


# B0L001S, U5-ch85, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	51.49
Std Dev	3.538

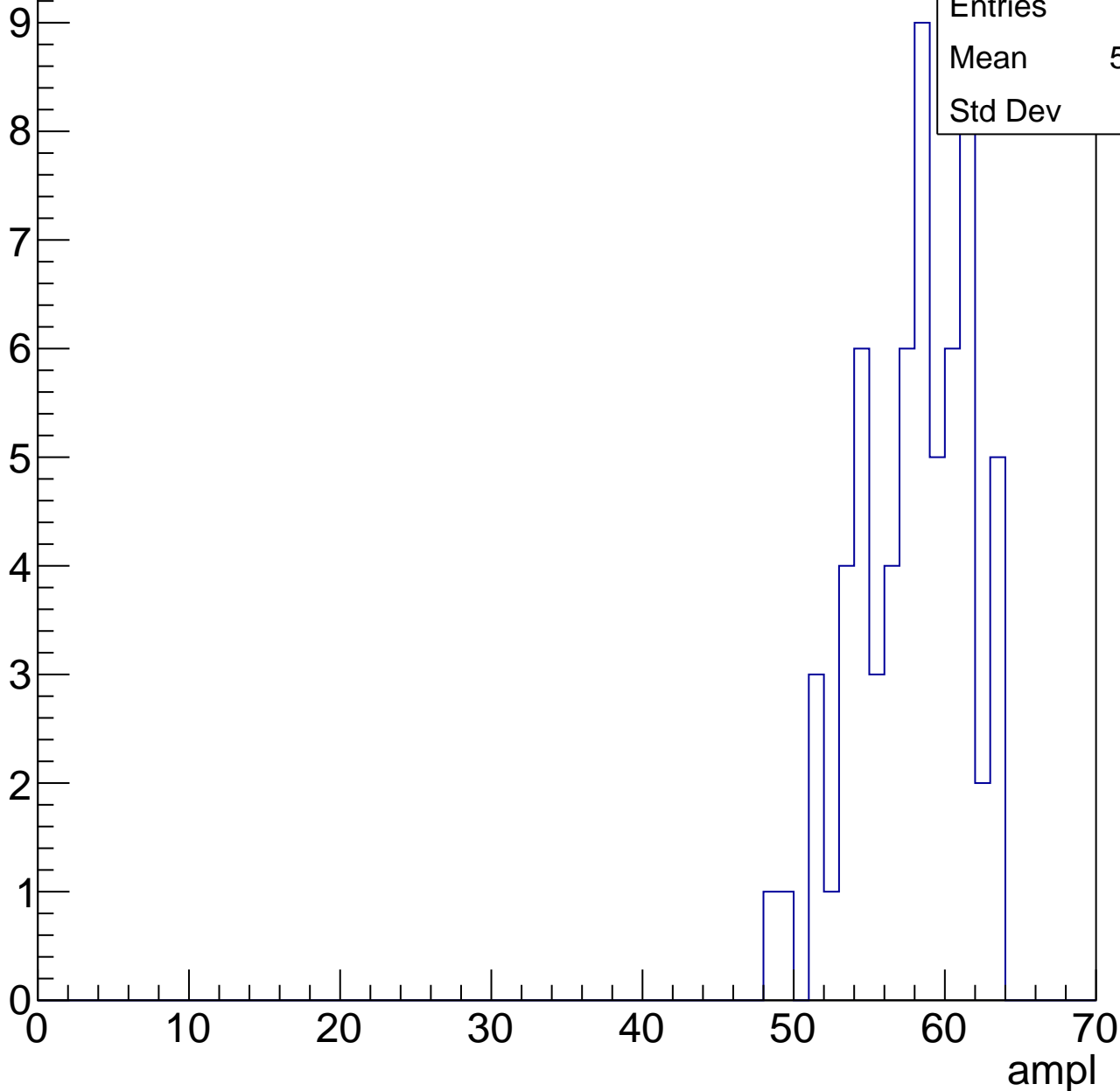


# B0L001S, U5-ch85, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	57.39
Std Dev	3.63

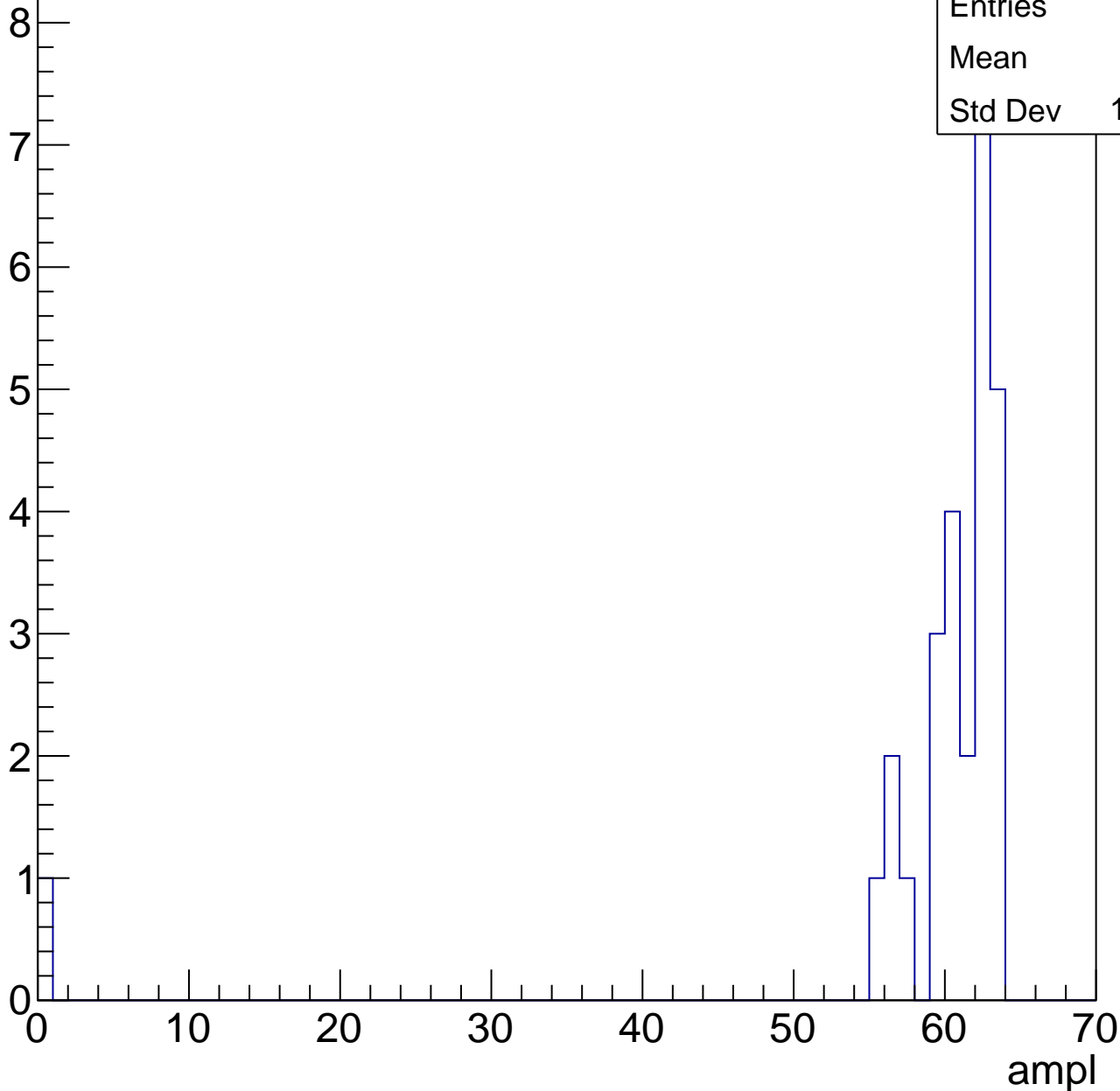


# B0L001S, U5-ch85, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	27
Mean	58.3
Std Dev	11.66



# B0L001S, U5-ch85, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U5-ch85, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch86, adc0

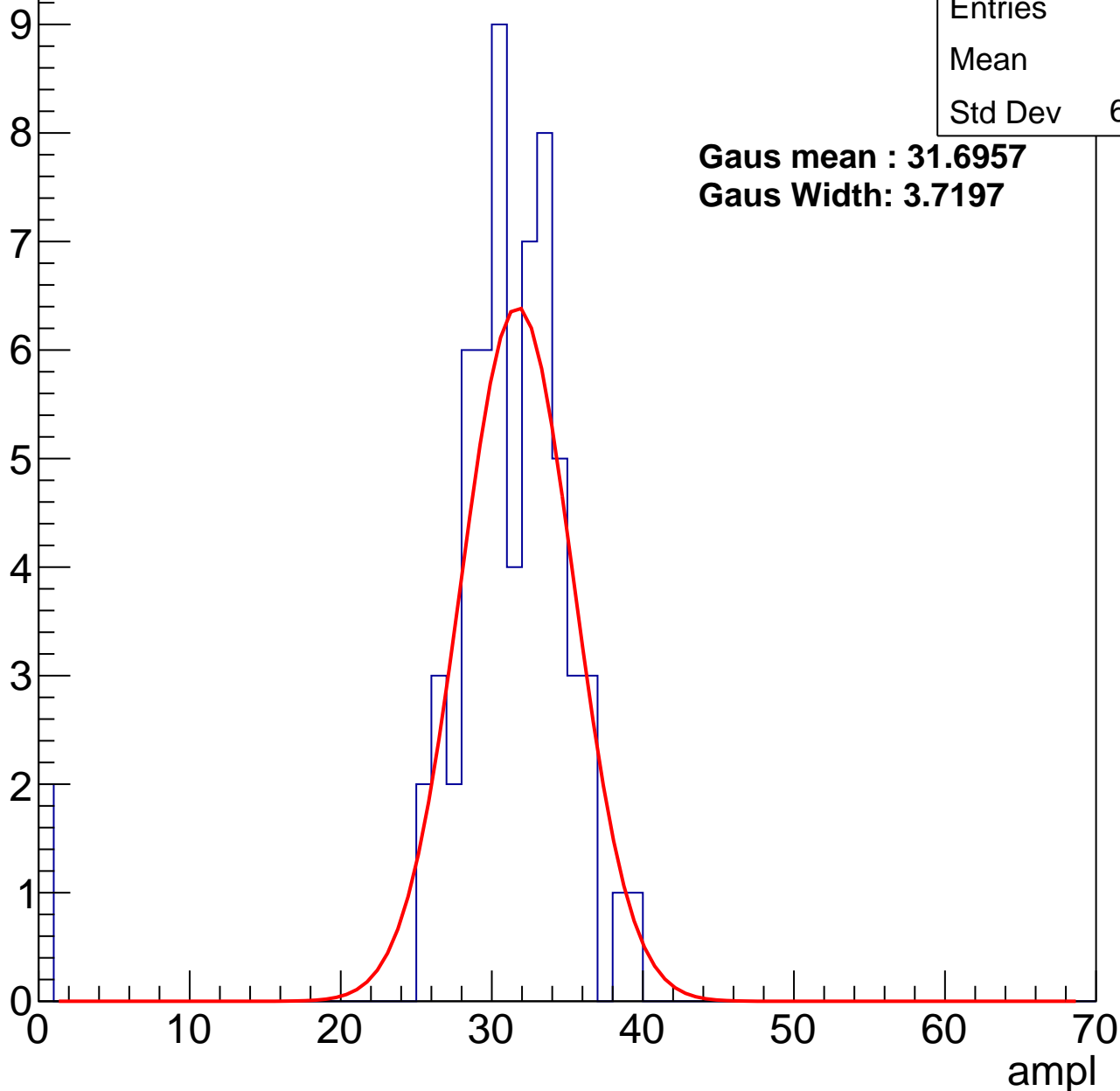
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	30.1
Std Dev	6.296

**Gaus mean : 31.6957**

**Gaus Width: 3.7197**



# B0L001S, U5-ch86, adc1

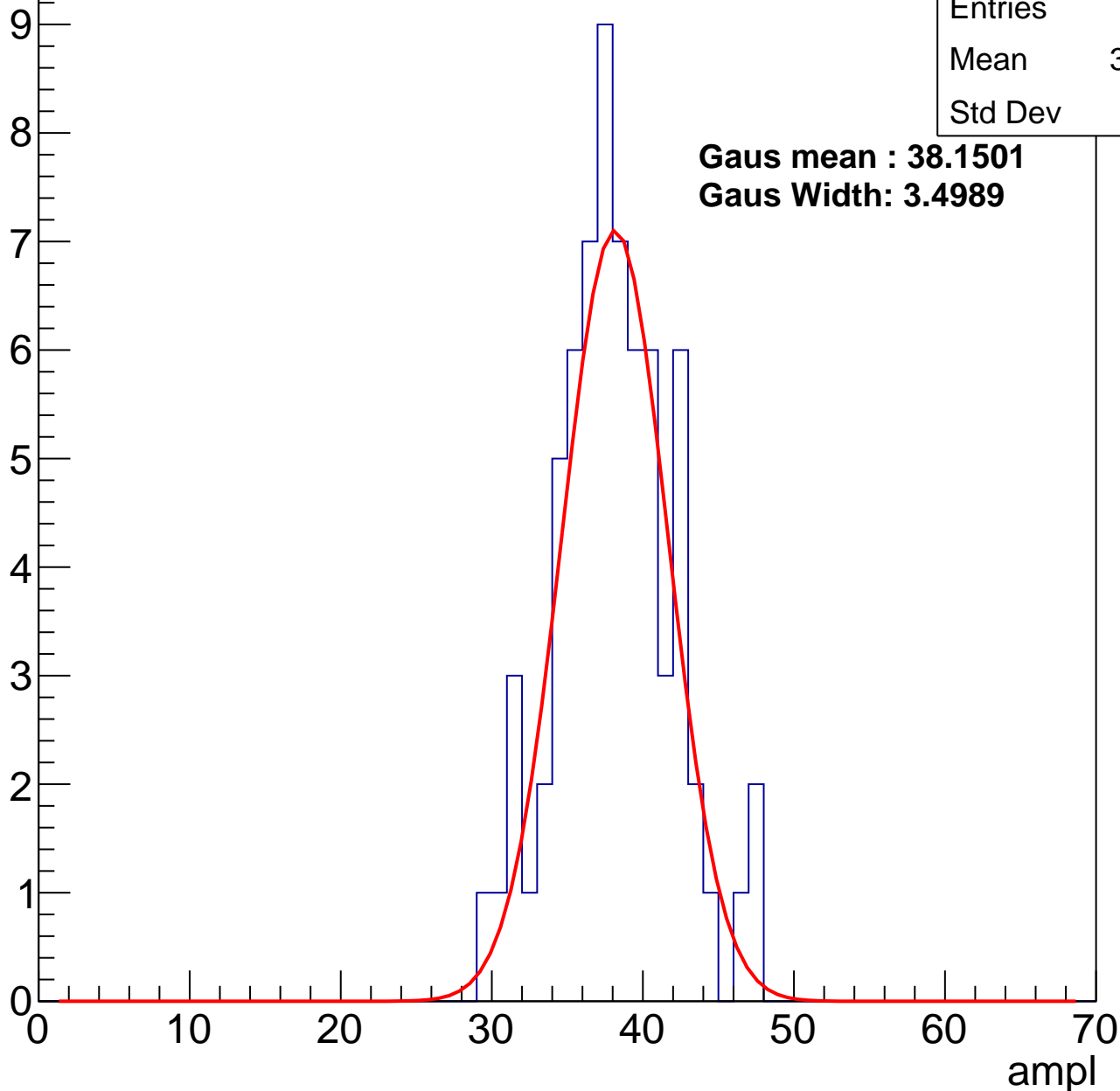
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	37.68
Std Dev	3.82

**Gaus mean : 38.1501**

**Gaus Width: 3.4989**



# B0L001S, U5-ch86, adc2

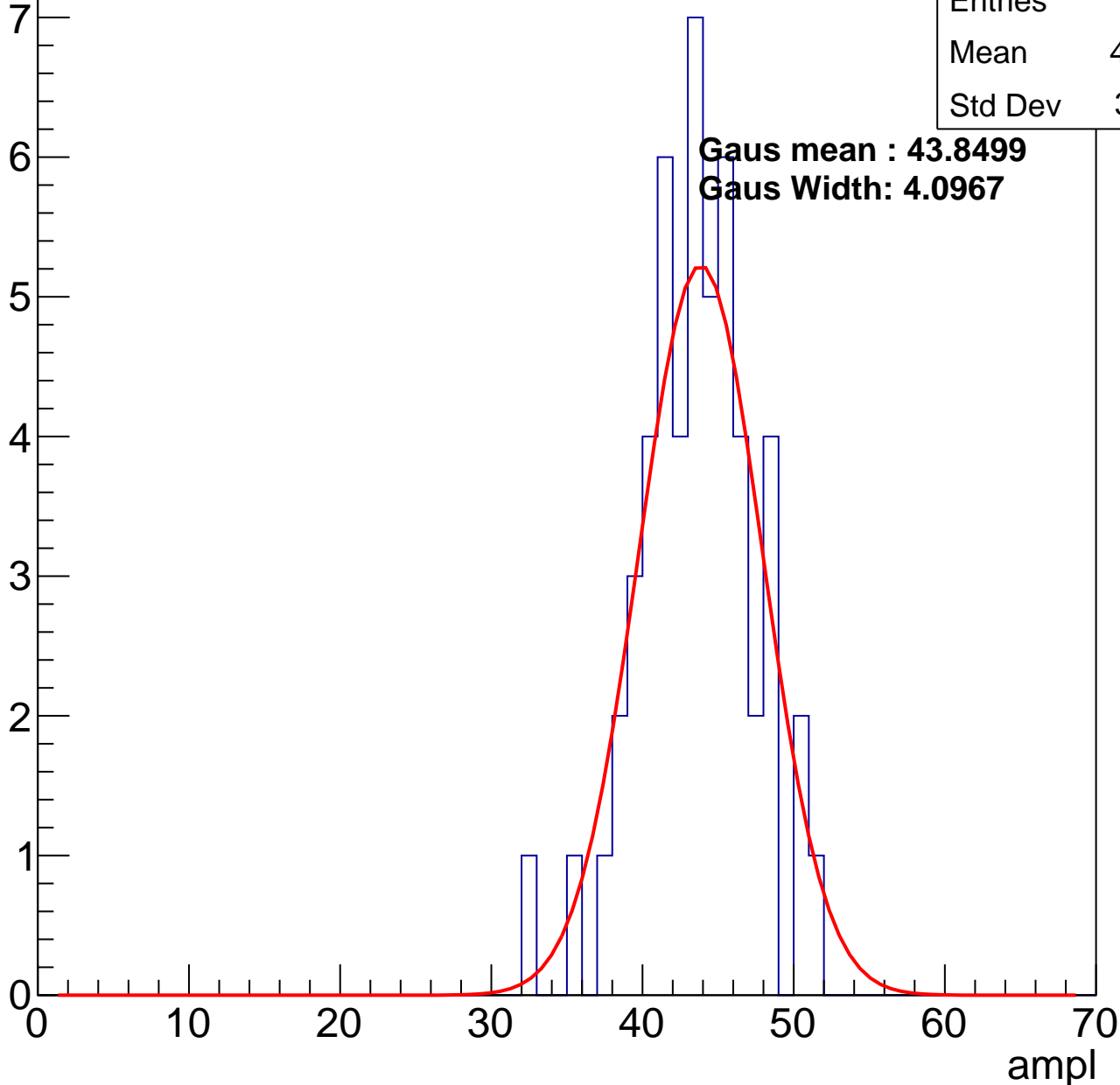
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	43.08
Std Dev	3.741

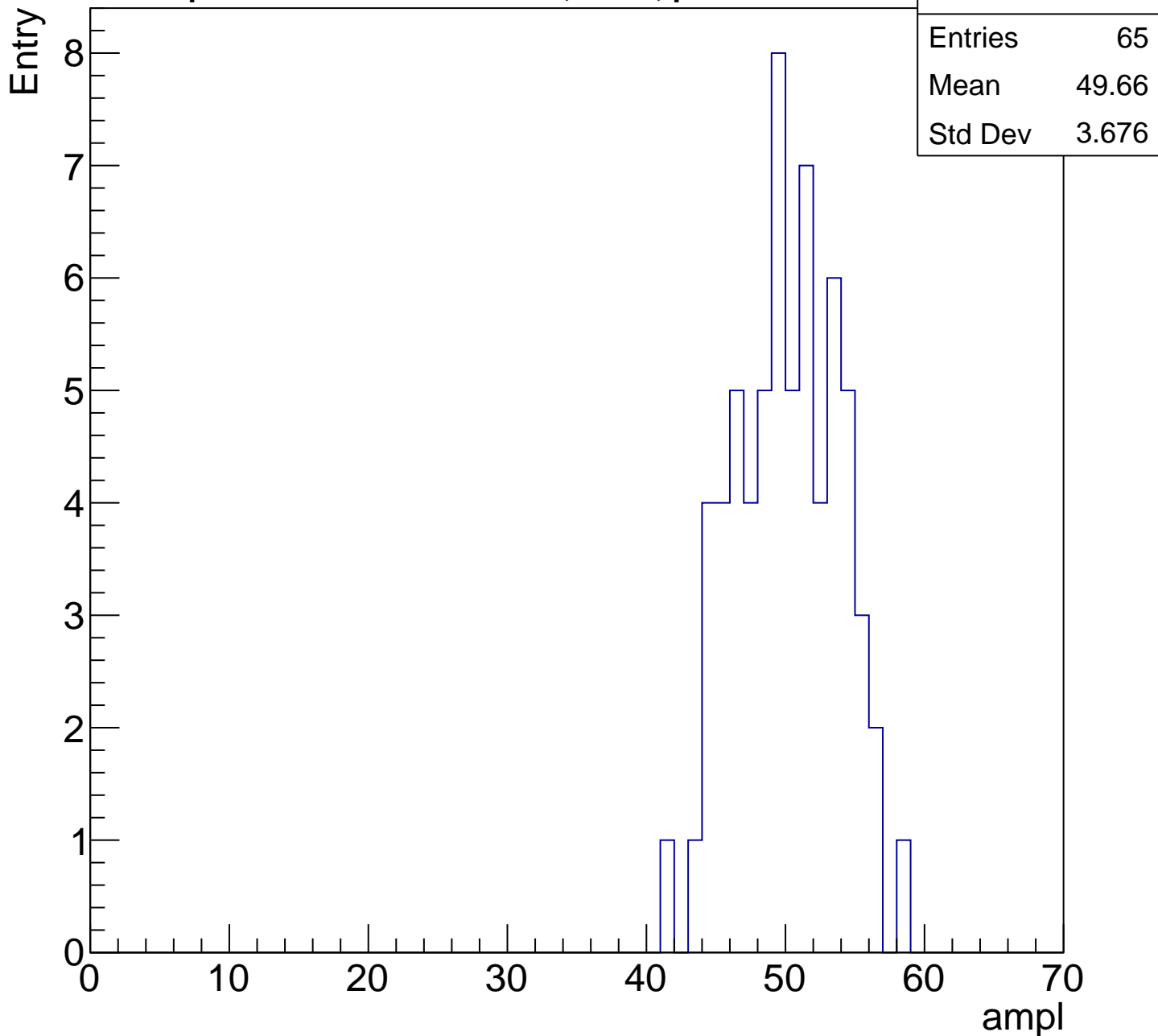
**Gaus mean : 43.8499**

**Gaus Width: 4.0967**



# B0L001S, U5-ch86, adc3

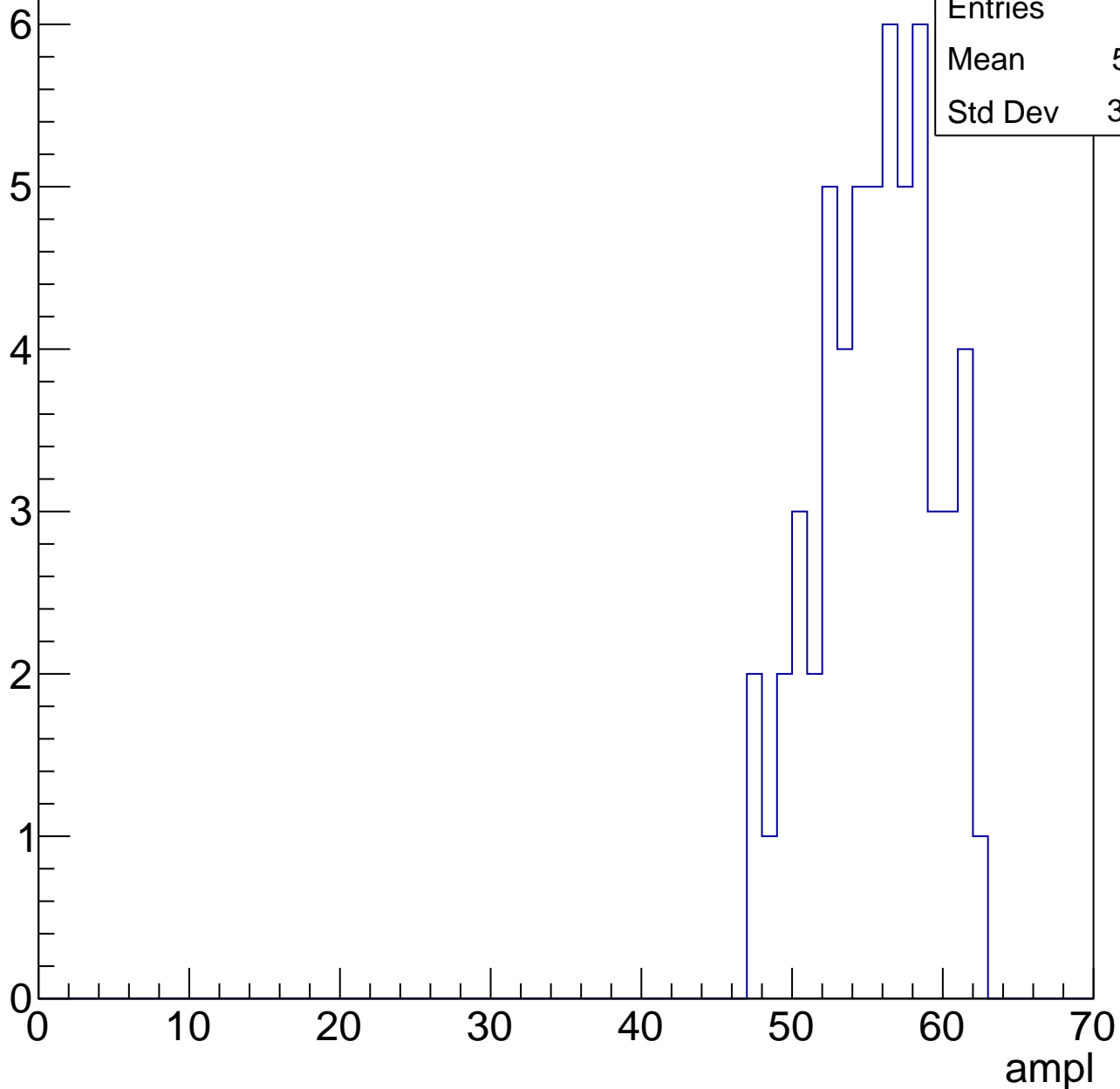
calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U5-ch86, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



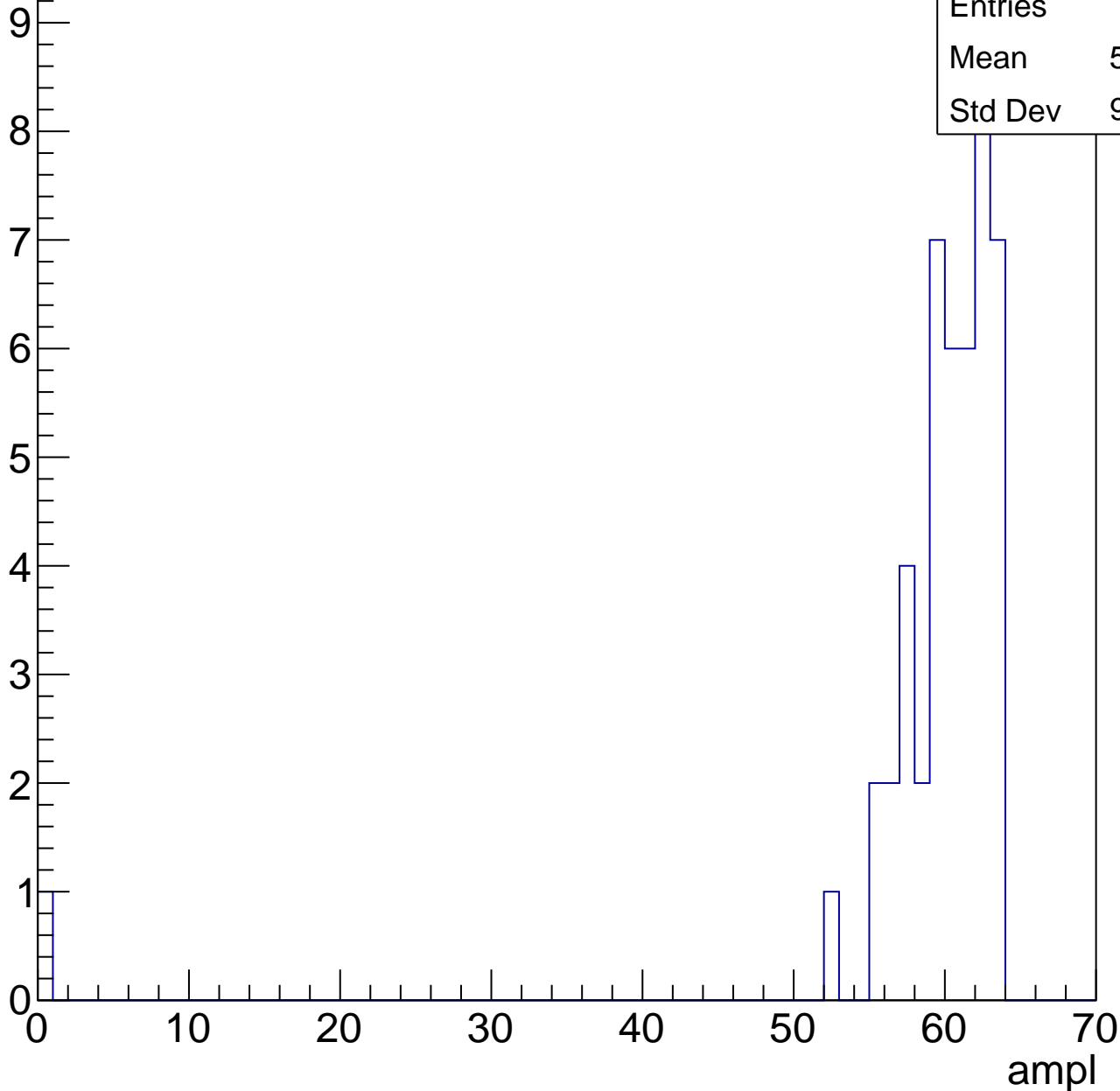
Entries	57
Mean	55.11
Std Dev	3.787

# B0L001S, U5-ch86, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

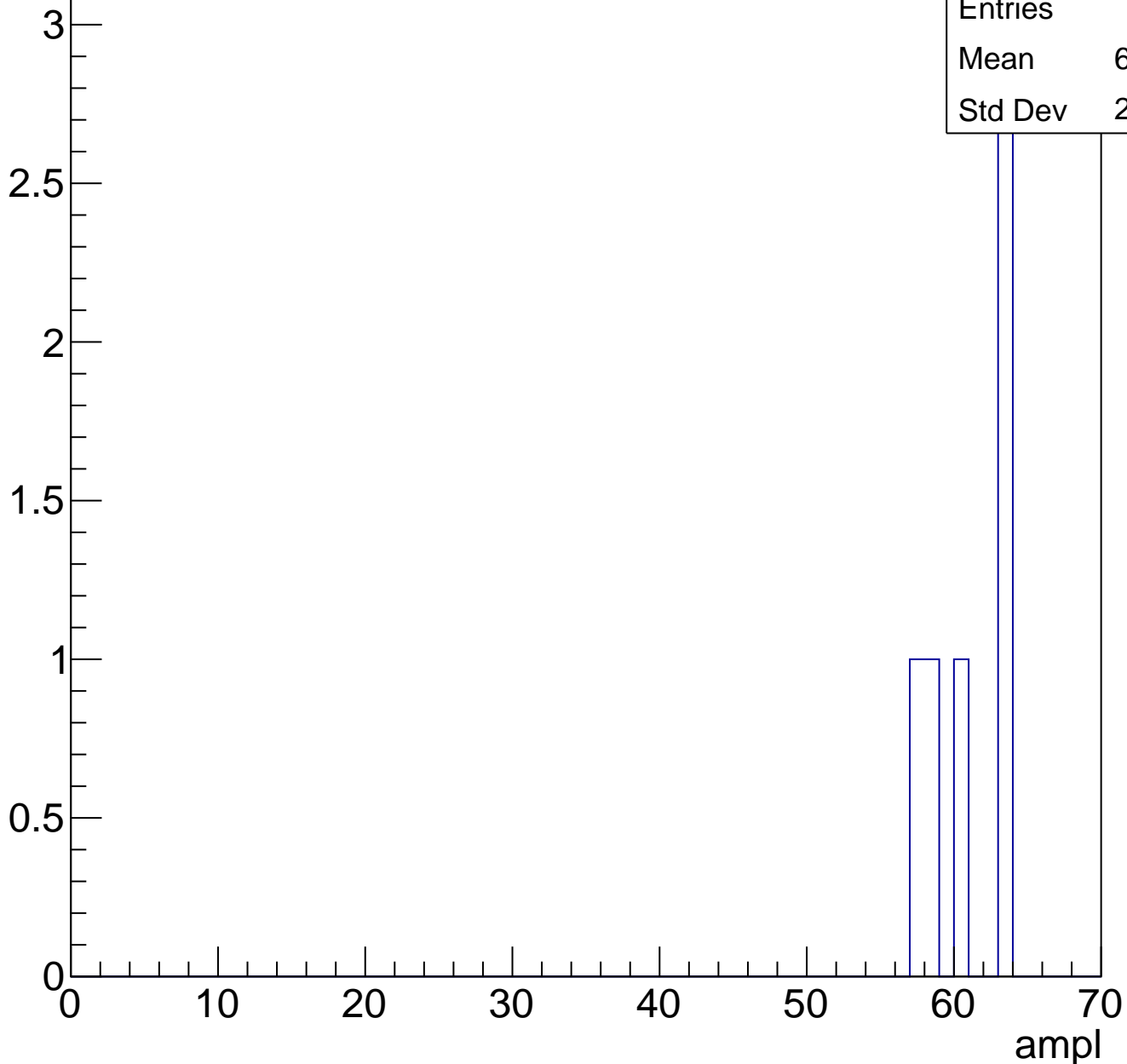
Entries	47
Mean	58.64
Std Dev	9.009



# B0L001S, U5-ch86, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	6
Mean	60.67
Std Dev	2.494



# B0L001S, U5-ch86, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U5-ch87, adc0

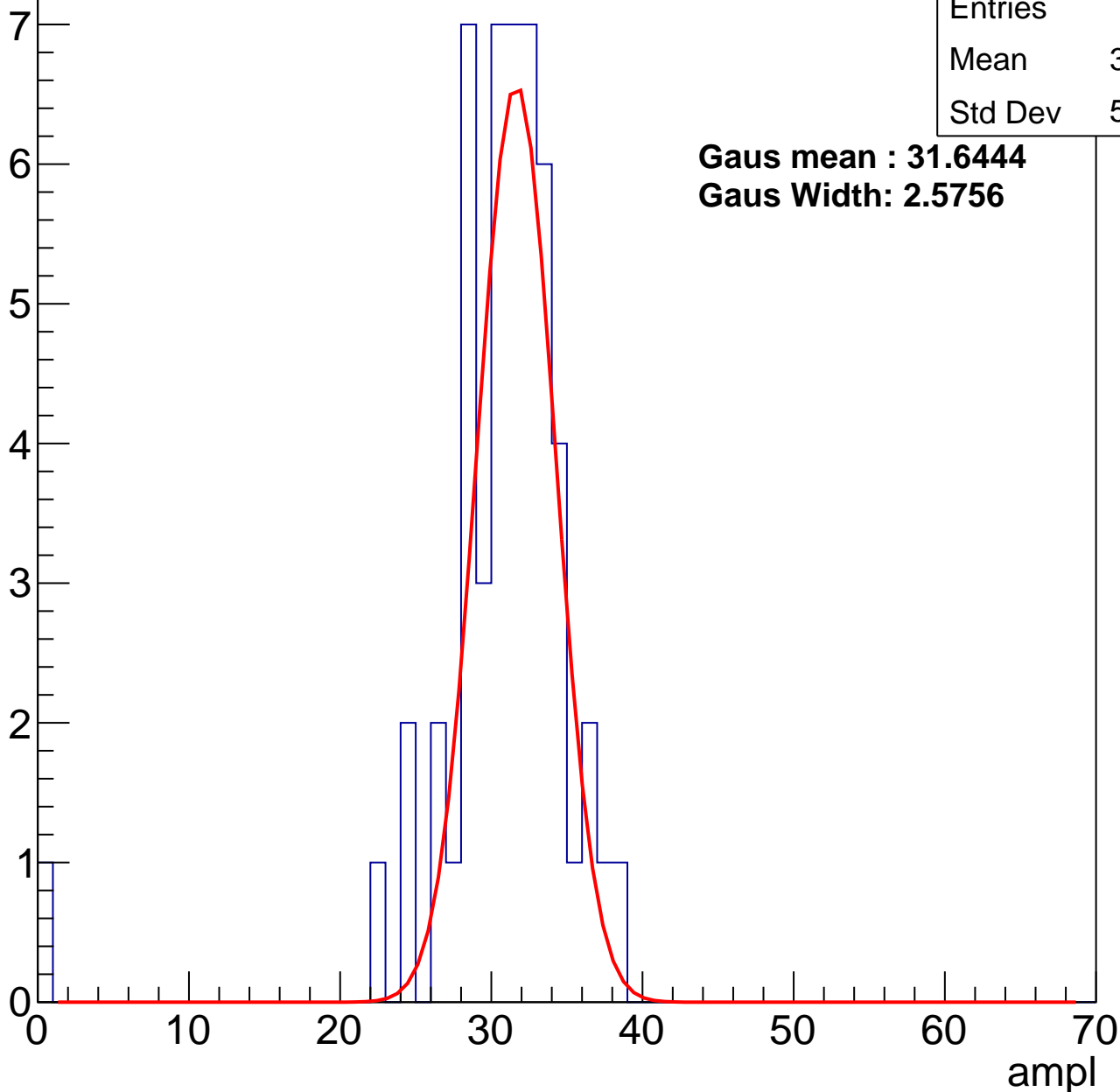
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	30.17
Std Dev	5.266

**Gaus mean : 31.6444**

**Gaus Width: 2.5756**



# B0L001S, U5-ch87, adc1

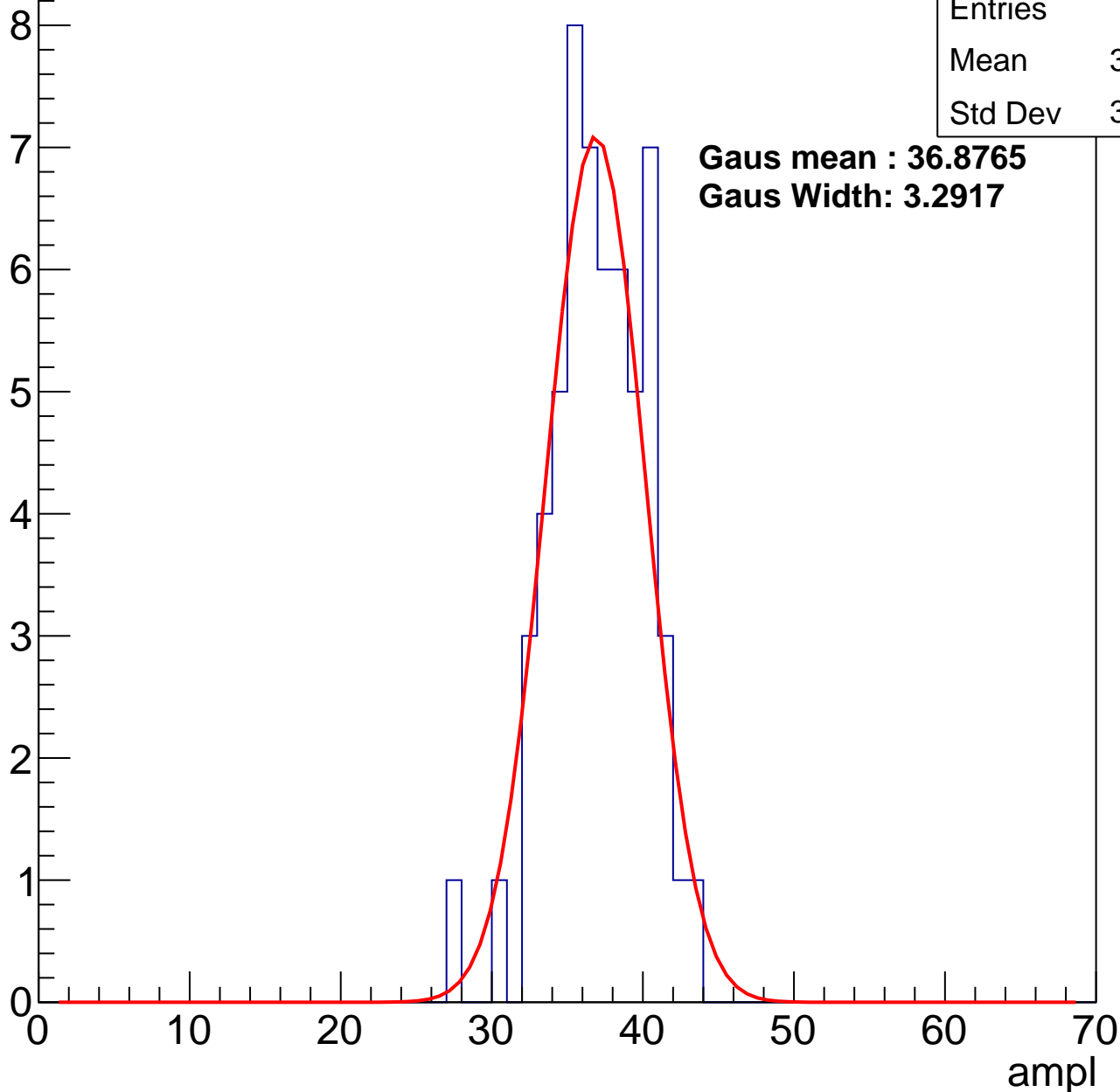
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	36.55
Std Dev	3.103

**Gaus mean : 36.8765**

**Gaus Width: 3.2917**



# B0L001S, U5-ch87, adc2

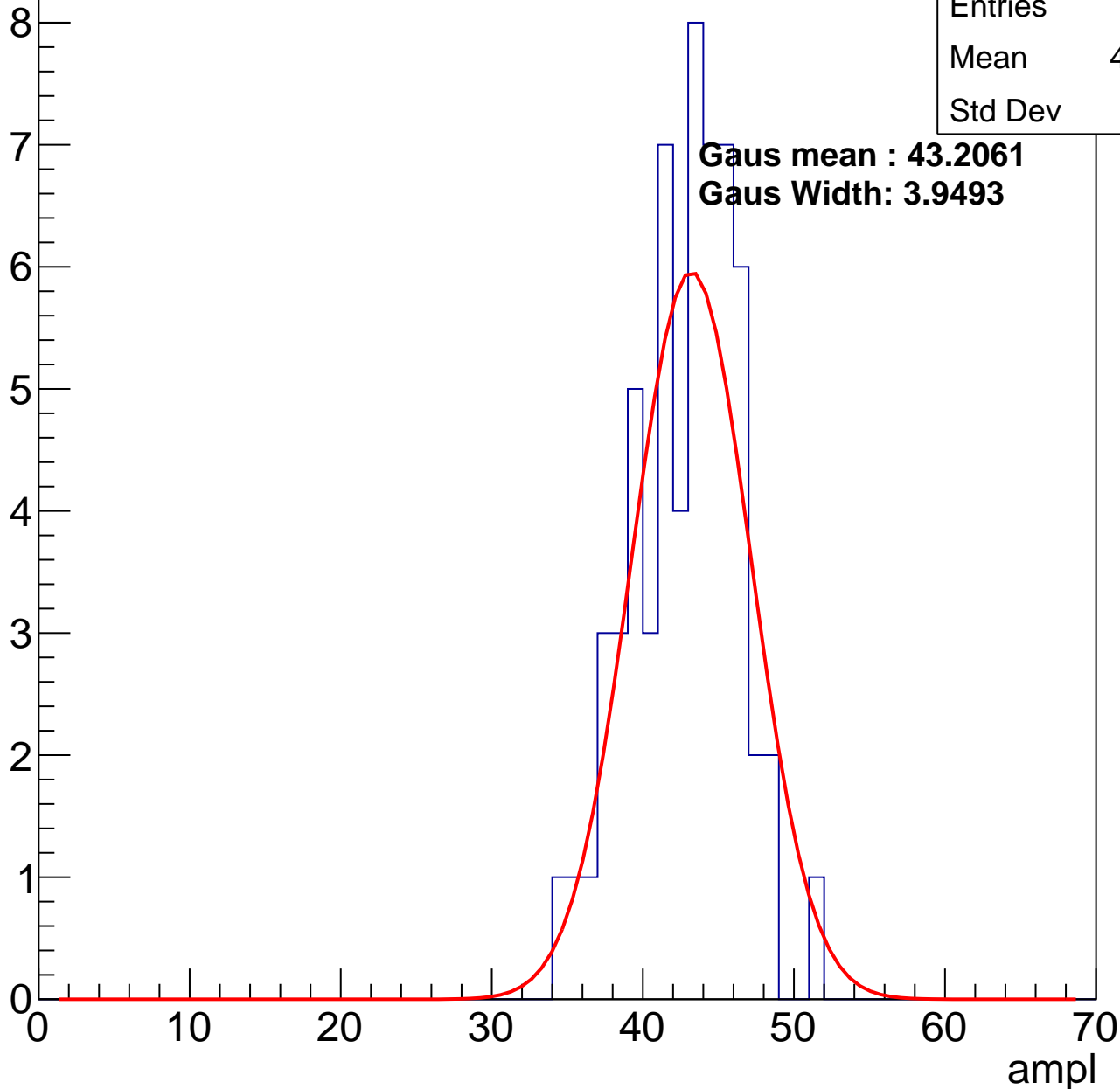
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	42.36
Std Dev	3.45

**Gaus mean : 43.2061**

**Gaus Width: 3.9493**

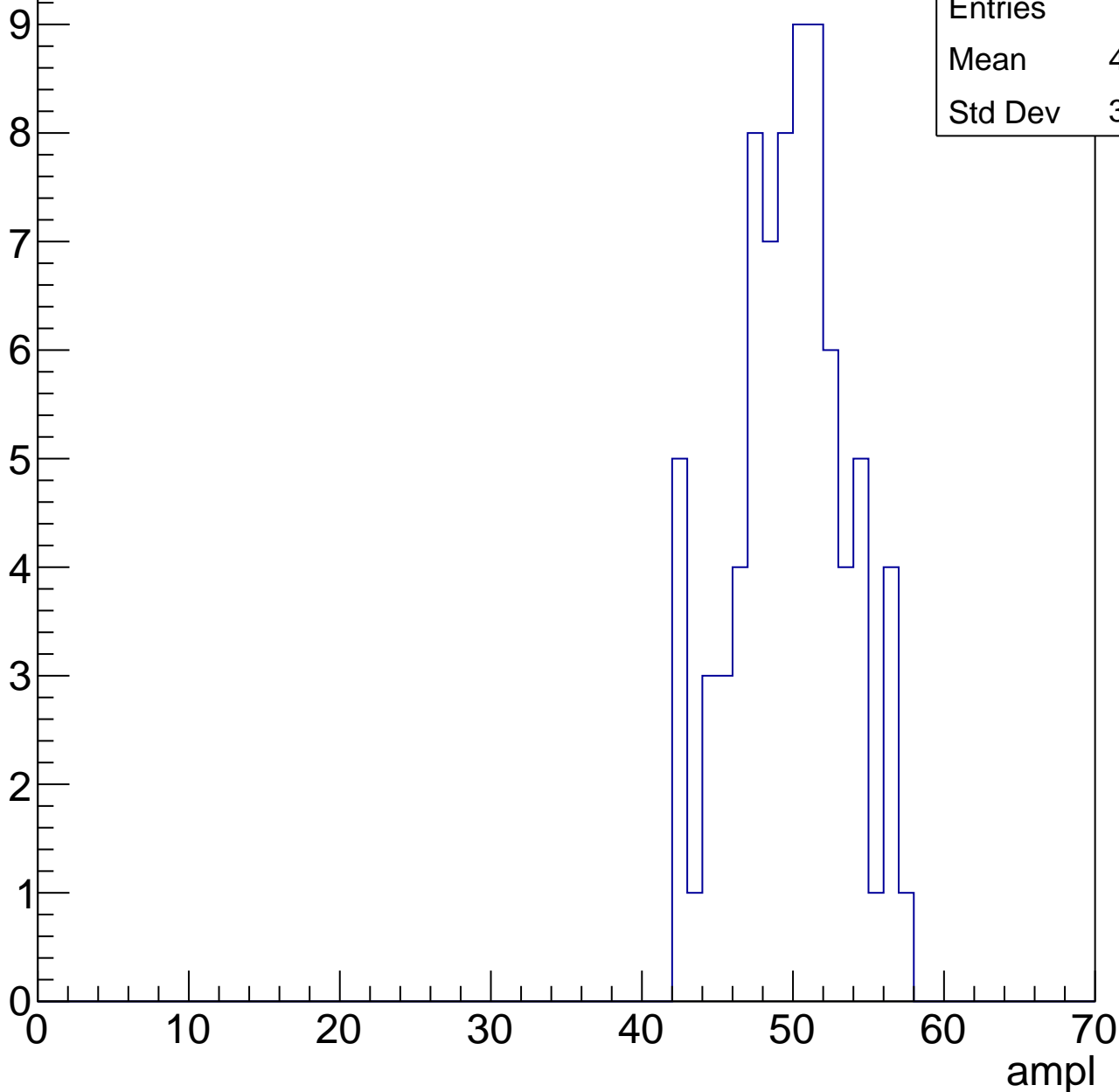


# B0L001S, U5-ch87, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	78
Mean	49.32
Std Dev	3.678

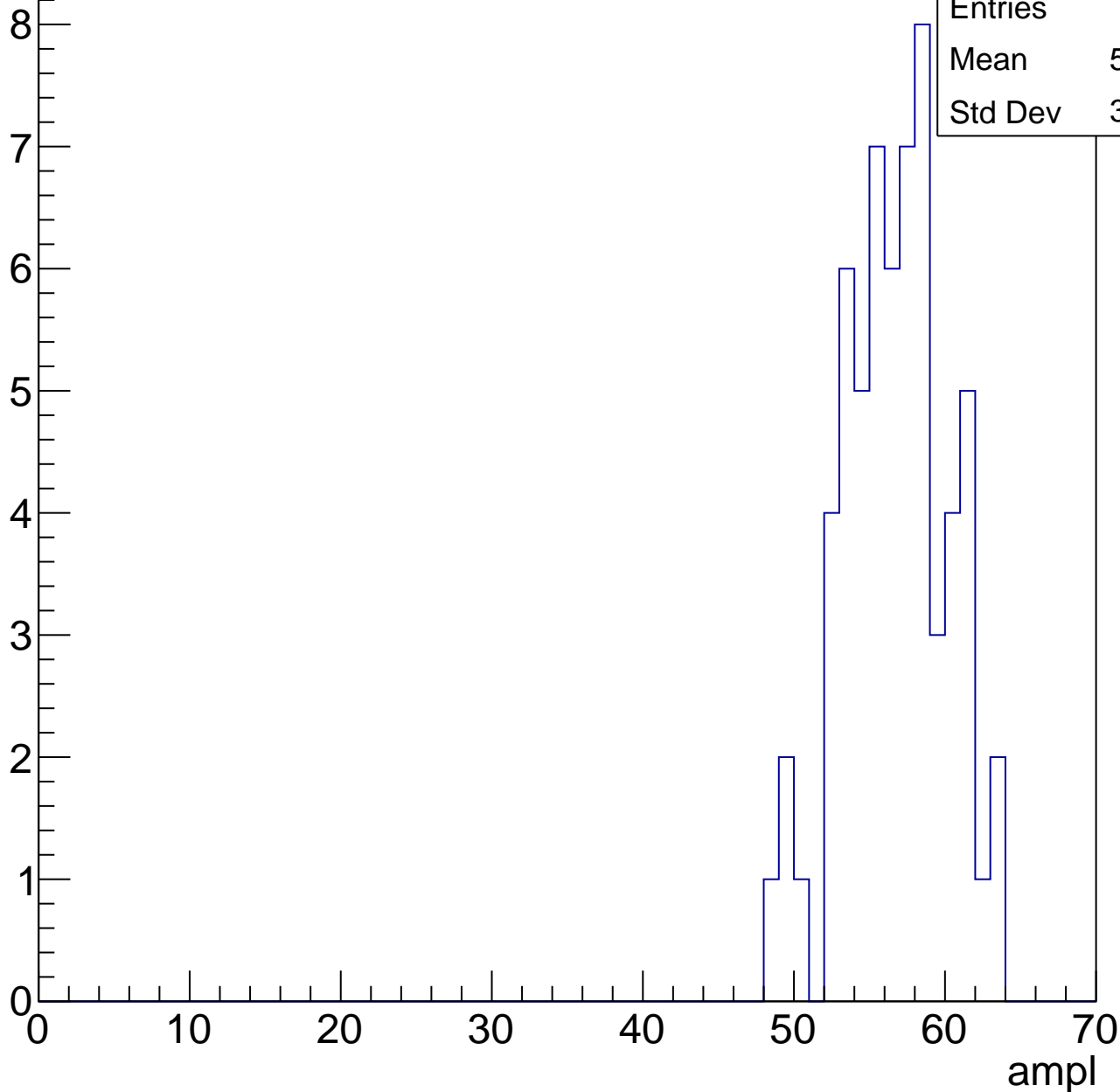


# B0L001S, U5-ch87, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	56.23
Std Dev	3.429

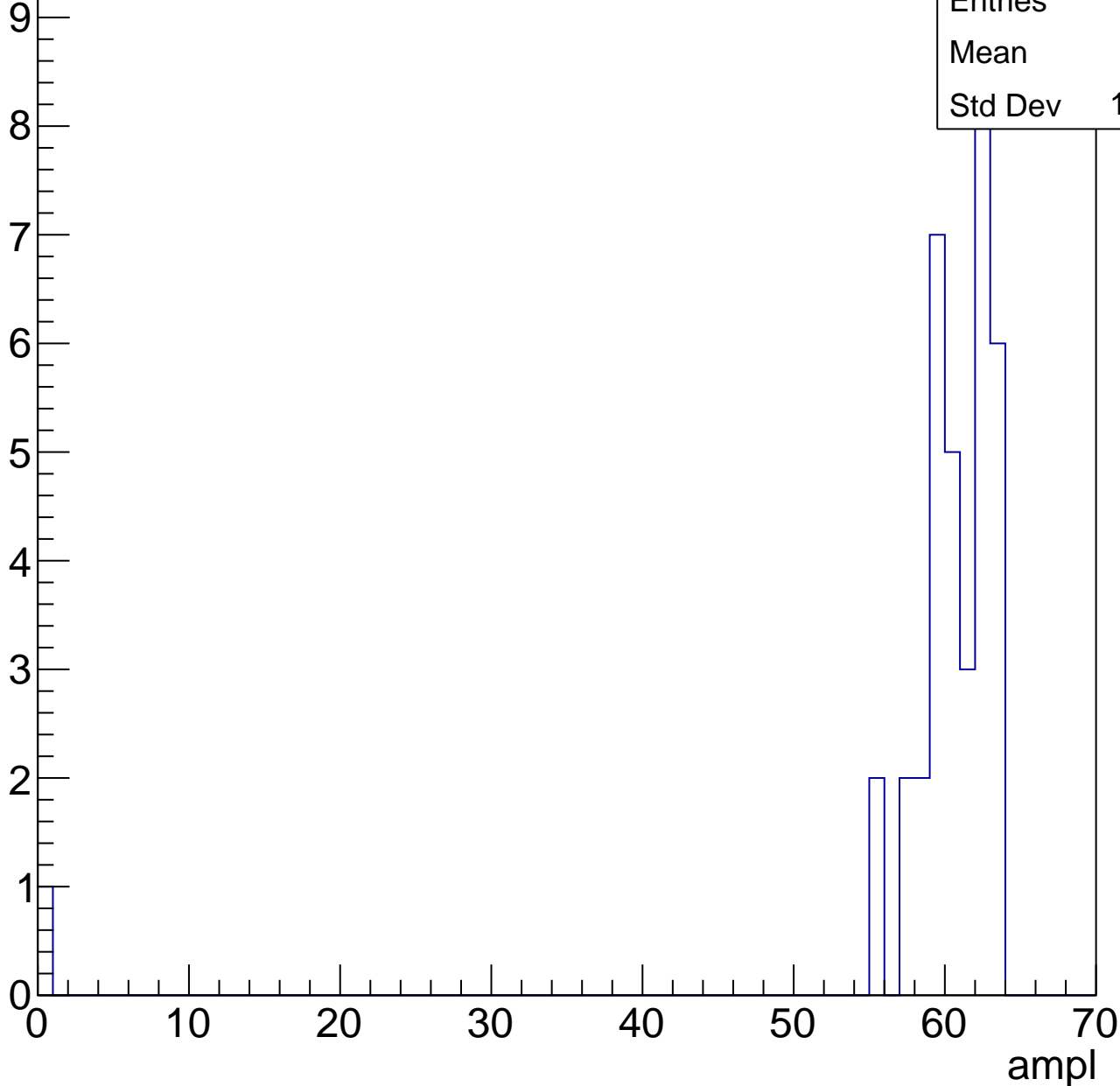


# B0L001S, U5-ch87, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	37
Mean	58.7
Std Dev	10.02



# B0L001S, U5-ch87, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	61.6
Std Dev	1.2

ampl

0 10 20 30 40 50 60 70



# B0L001S, U5-ch87, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch88, adc0

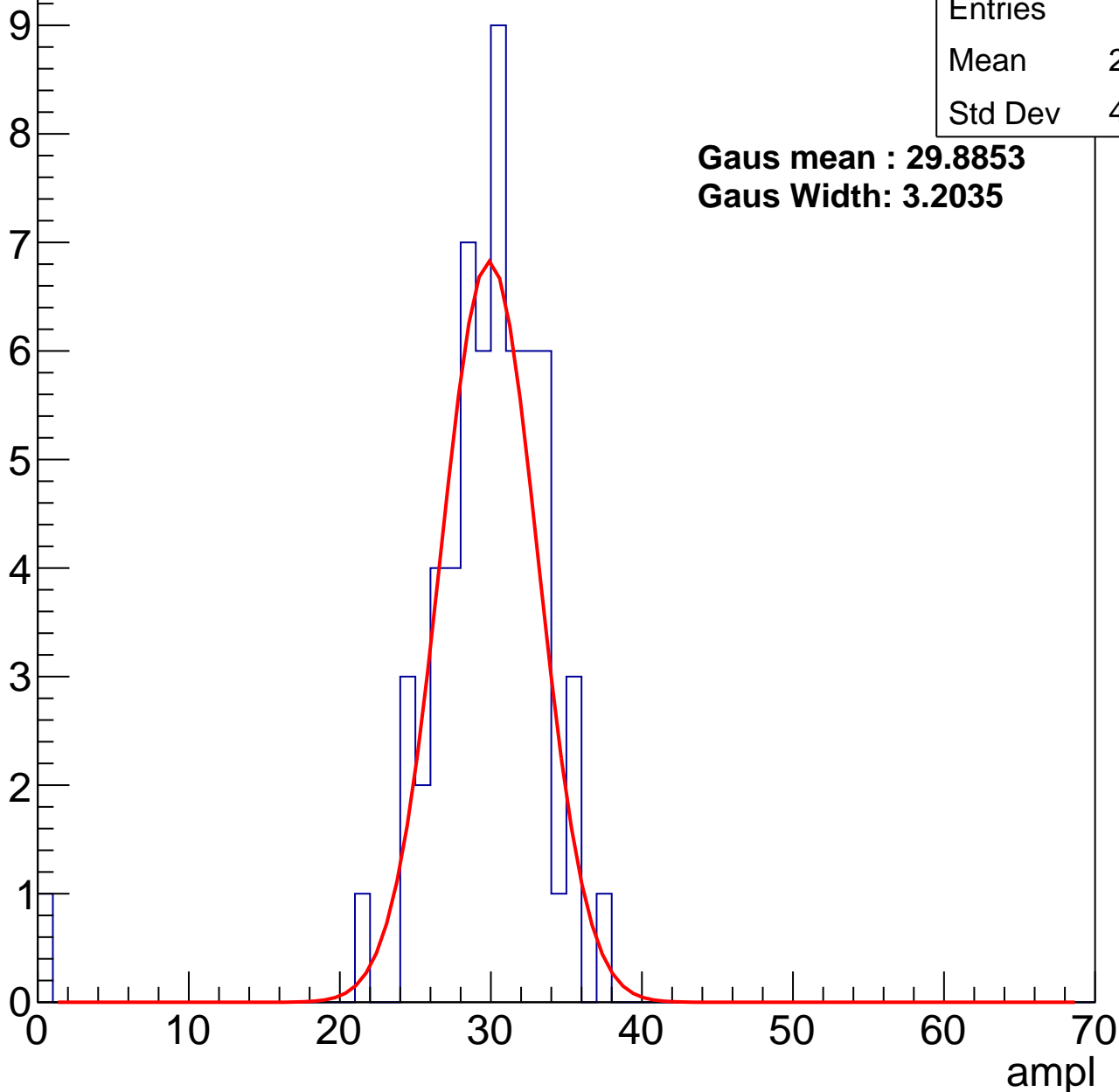
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	29.12
Std Dev	4.916

**Gaus mean : 29.8853**

**Gaus Width: 3.2035**



# B0L001S, U5-ch88, adc1

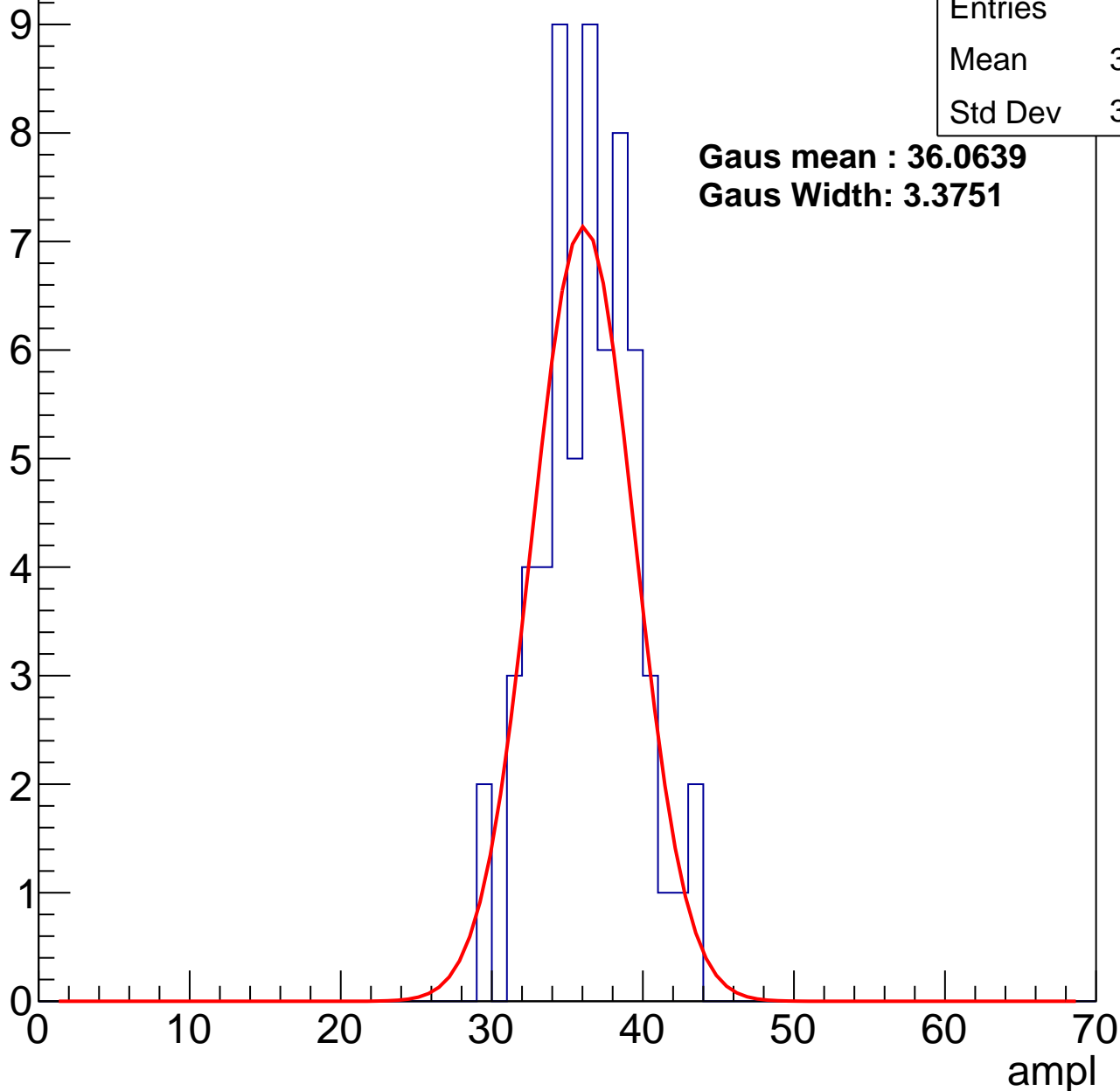
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	35.95
Std Dev	3.119

**Gaus mean : 36.0639**

**Gaus Width: 3.3751**



# B0L001S, U5-ch88, adc2

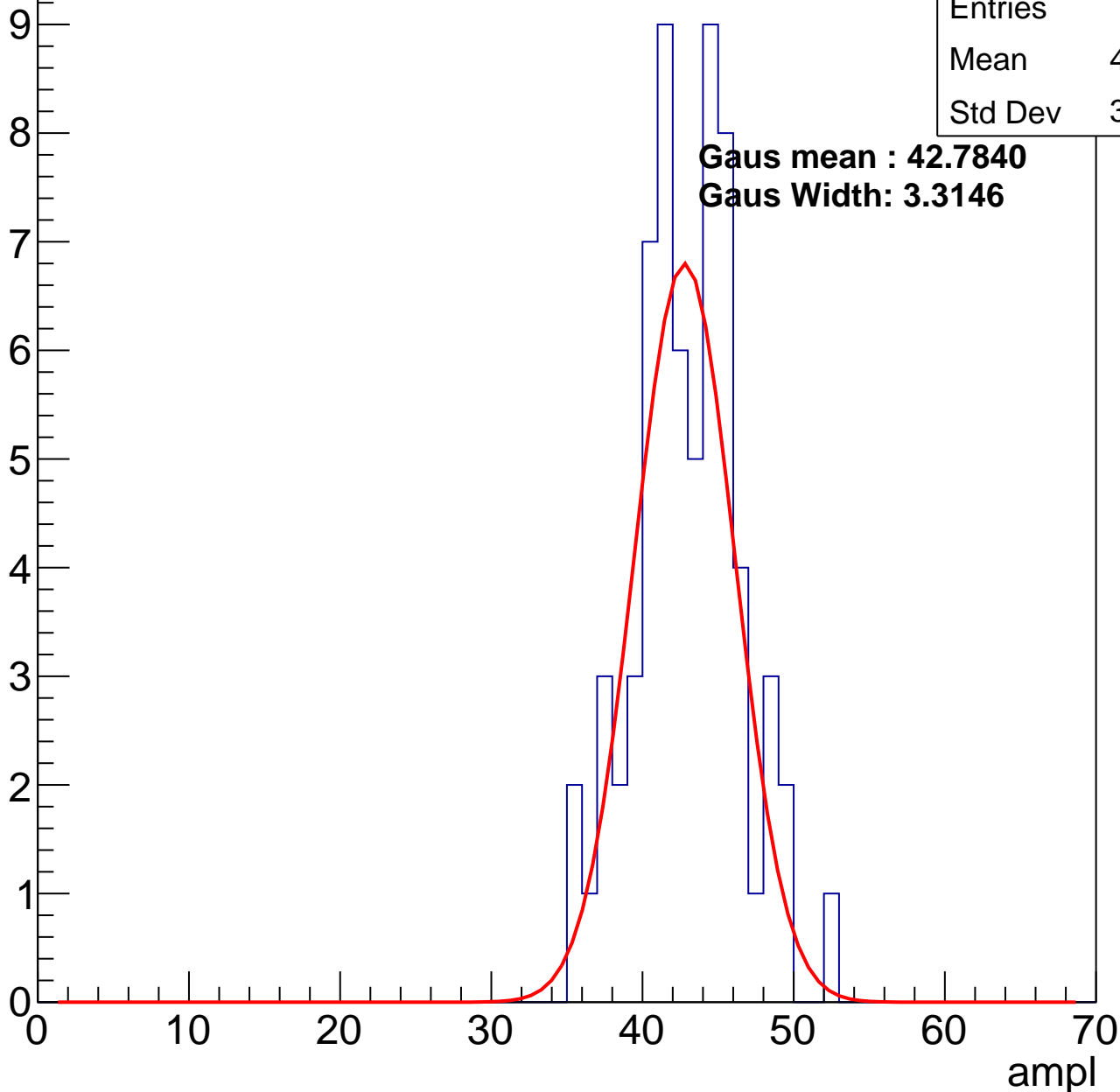
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	42.53
Std Dev	3.469

**Gaus mean : 42.7840**

**Gaus Width: 3.3146**

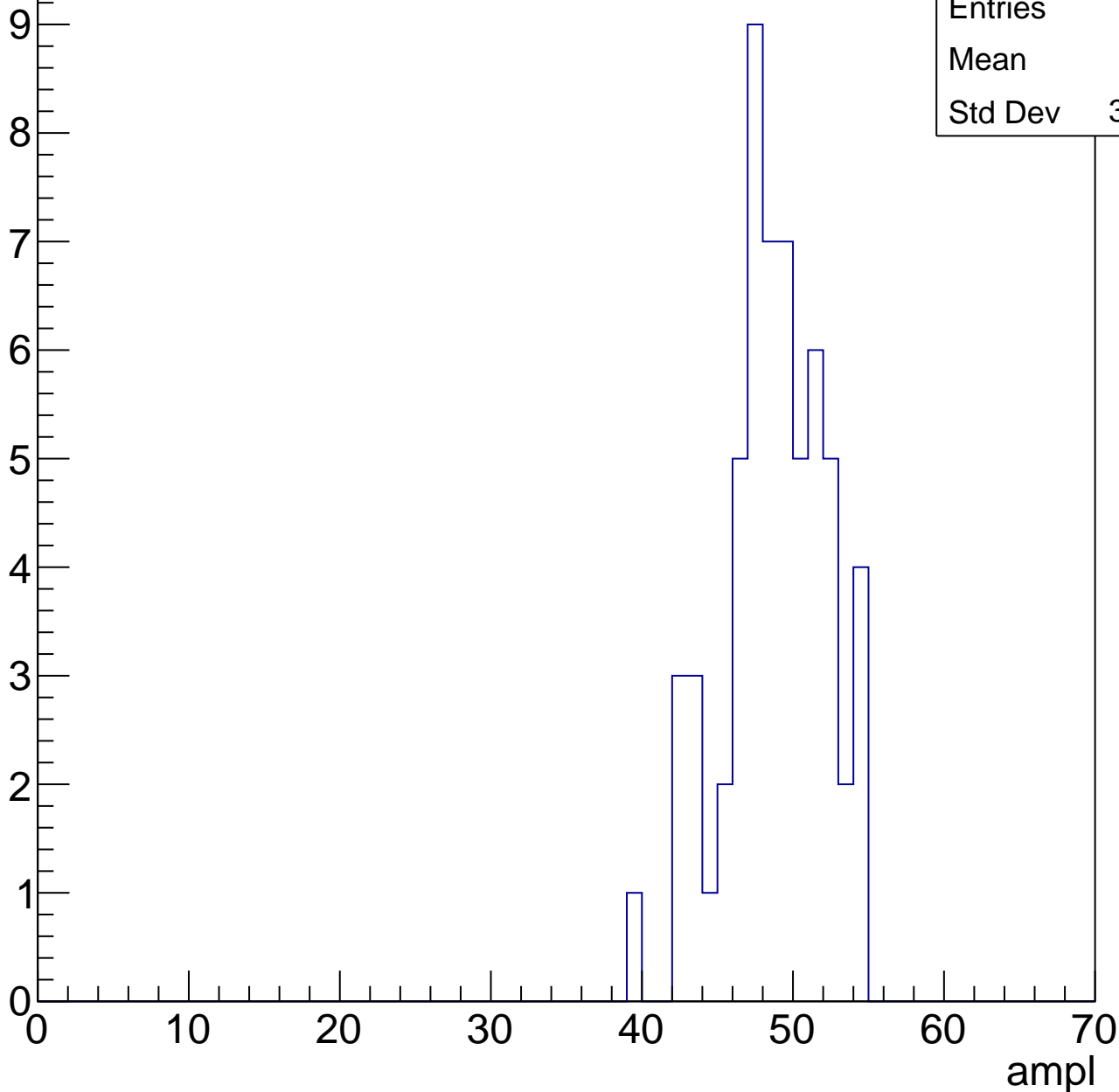


# B0L001S, U5-ch88, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	48.3
Std Dev	3.358



# B0L001S, U5-ch88, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

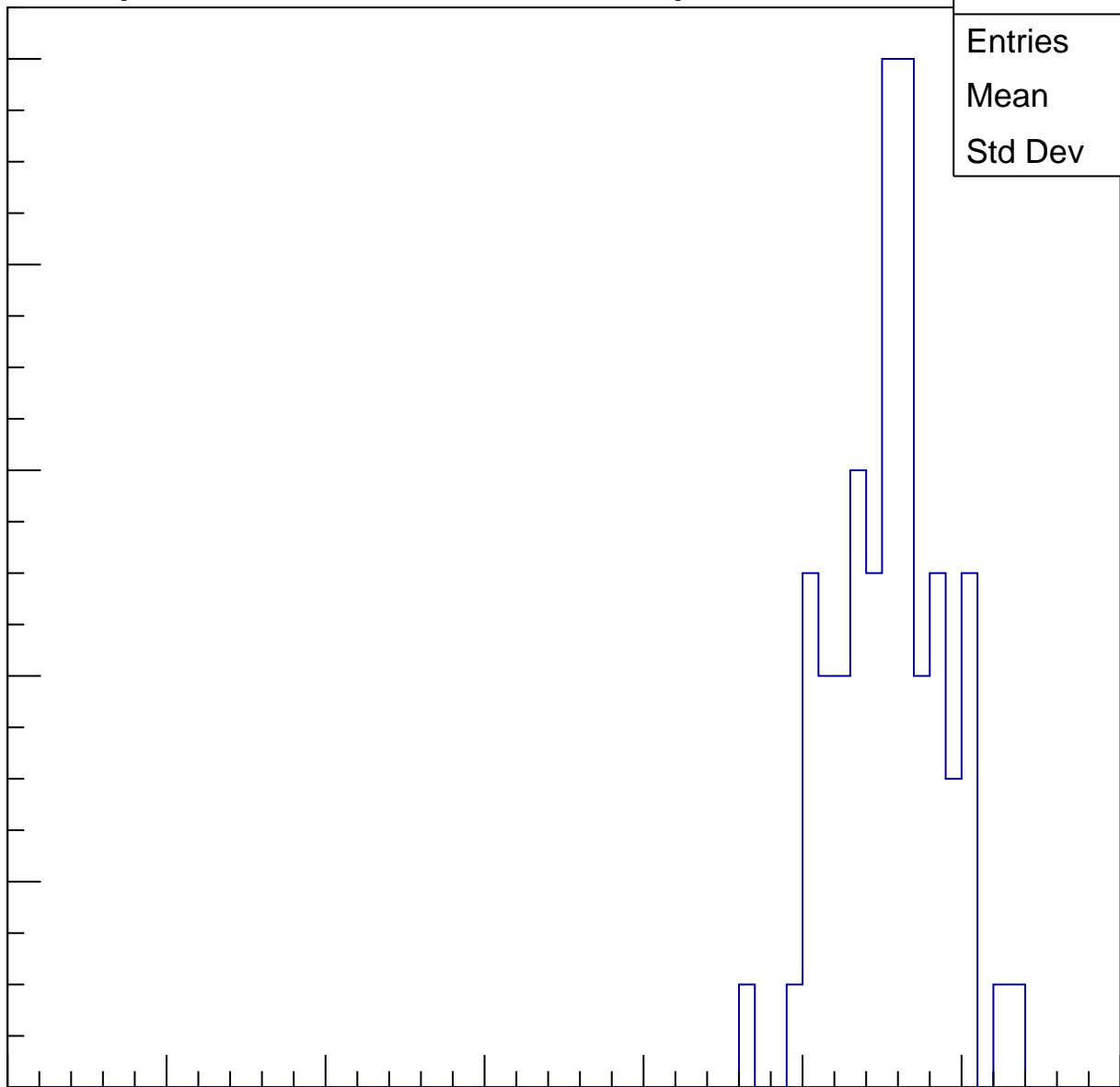
Entries	65
Mean	55
Std Dev	3.347

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

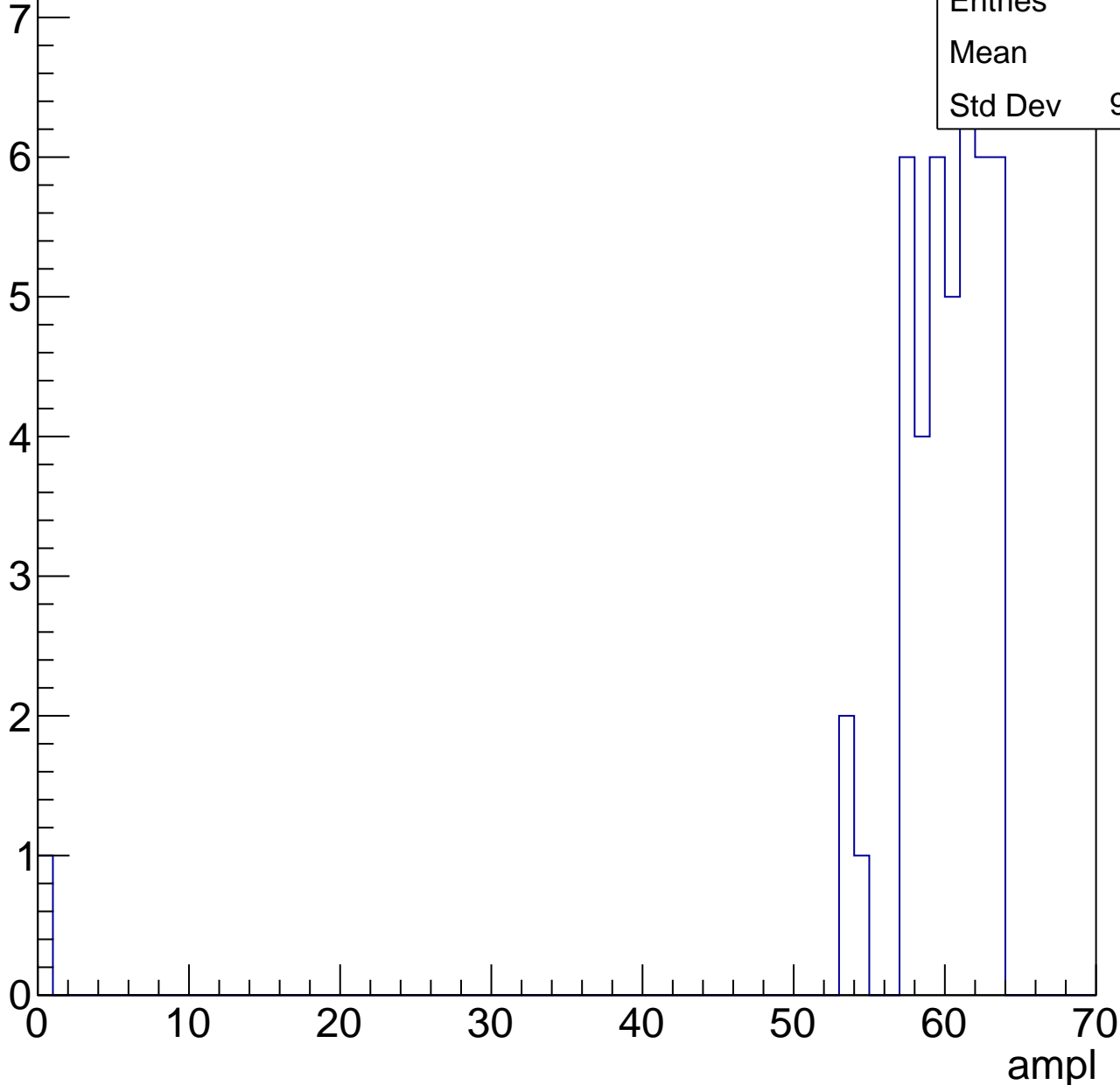


# B0L001S, U5-ch88, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

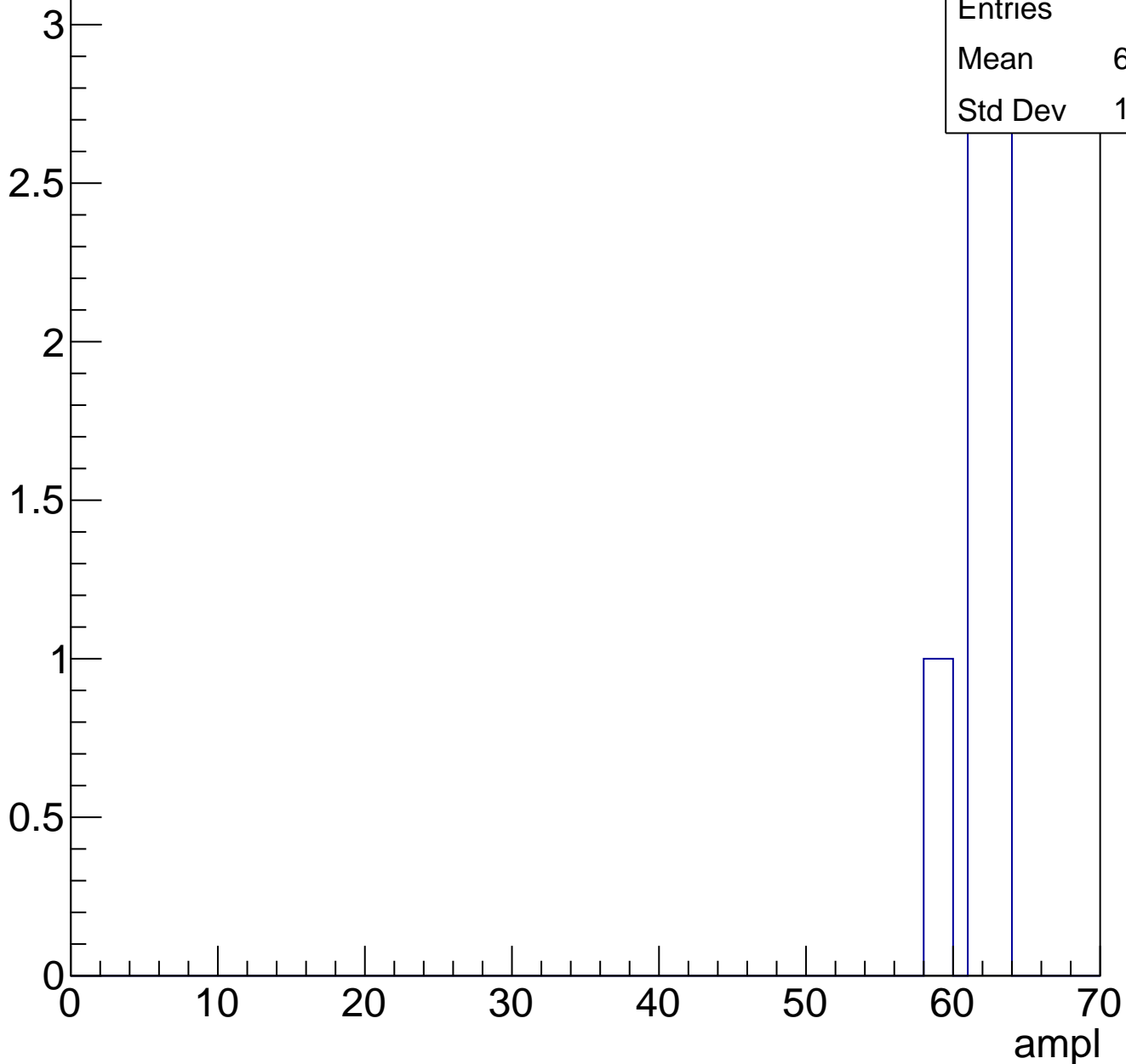
Entries	44
Mean	58.3
Std Dev	9.253



# B0L001S, U5-ch88, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch88, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L001S, U5-ch89, adc0

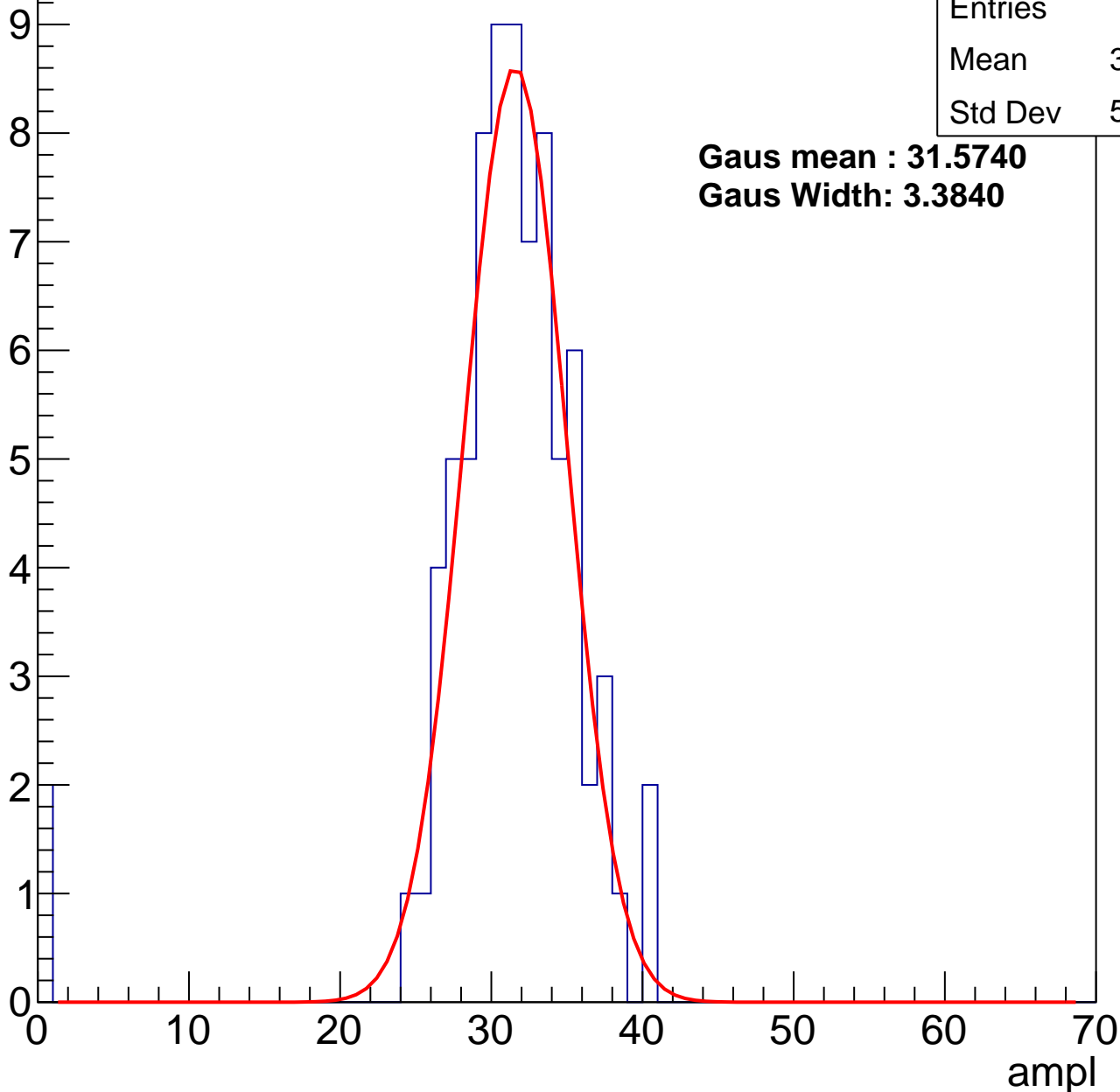
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	78
Mean	30.49
Std Dev	5.993

**Gaus mean : 31.5740**

**Gaus Width: 3.3840**



# B0L001S, U5-ch89, adc1

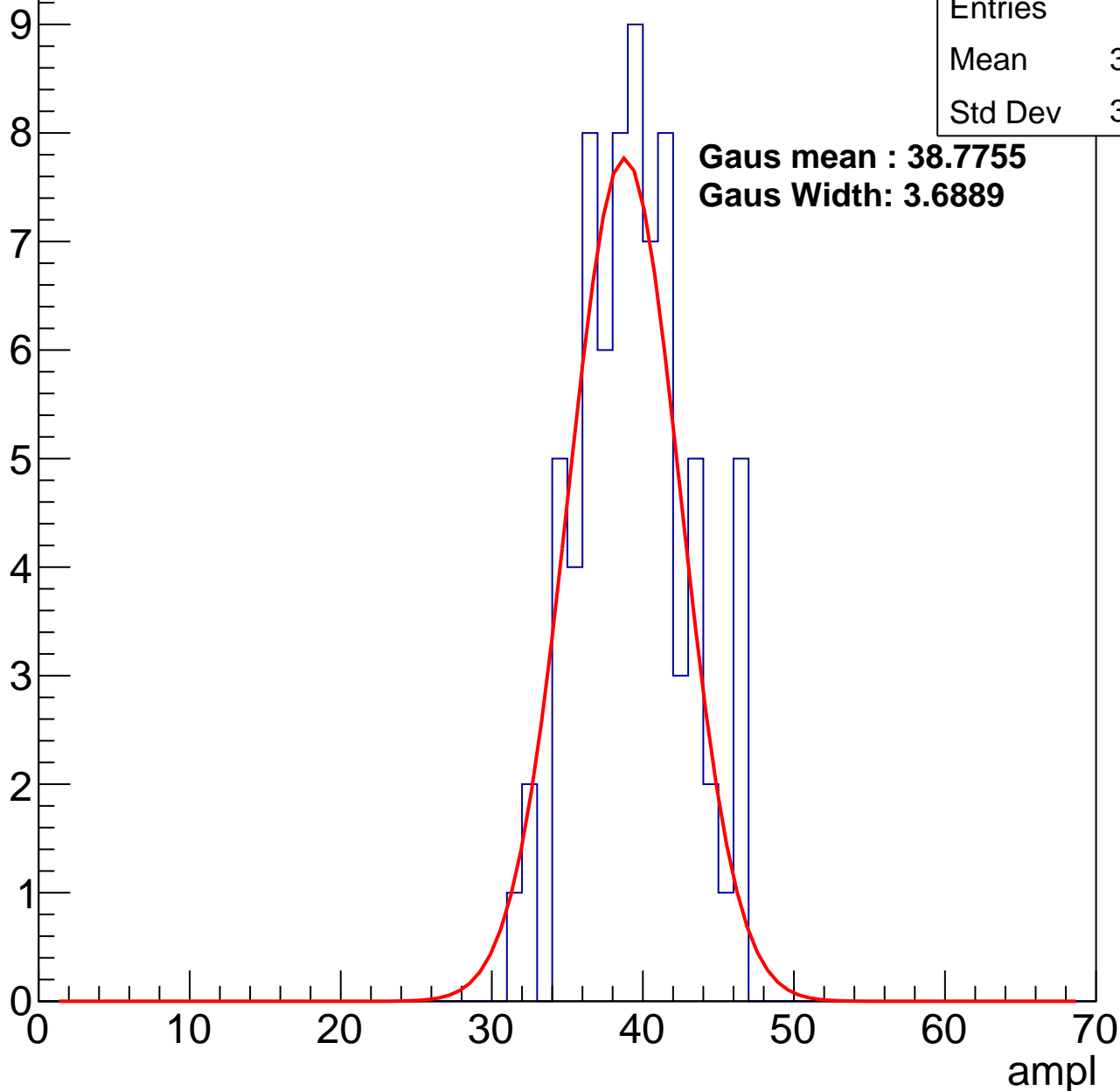
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	38.95
Std Dev	3.548

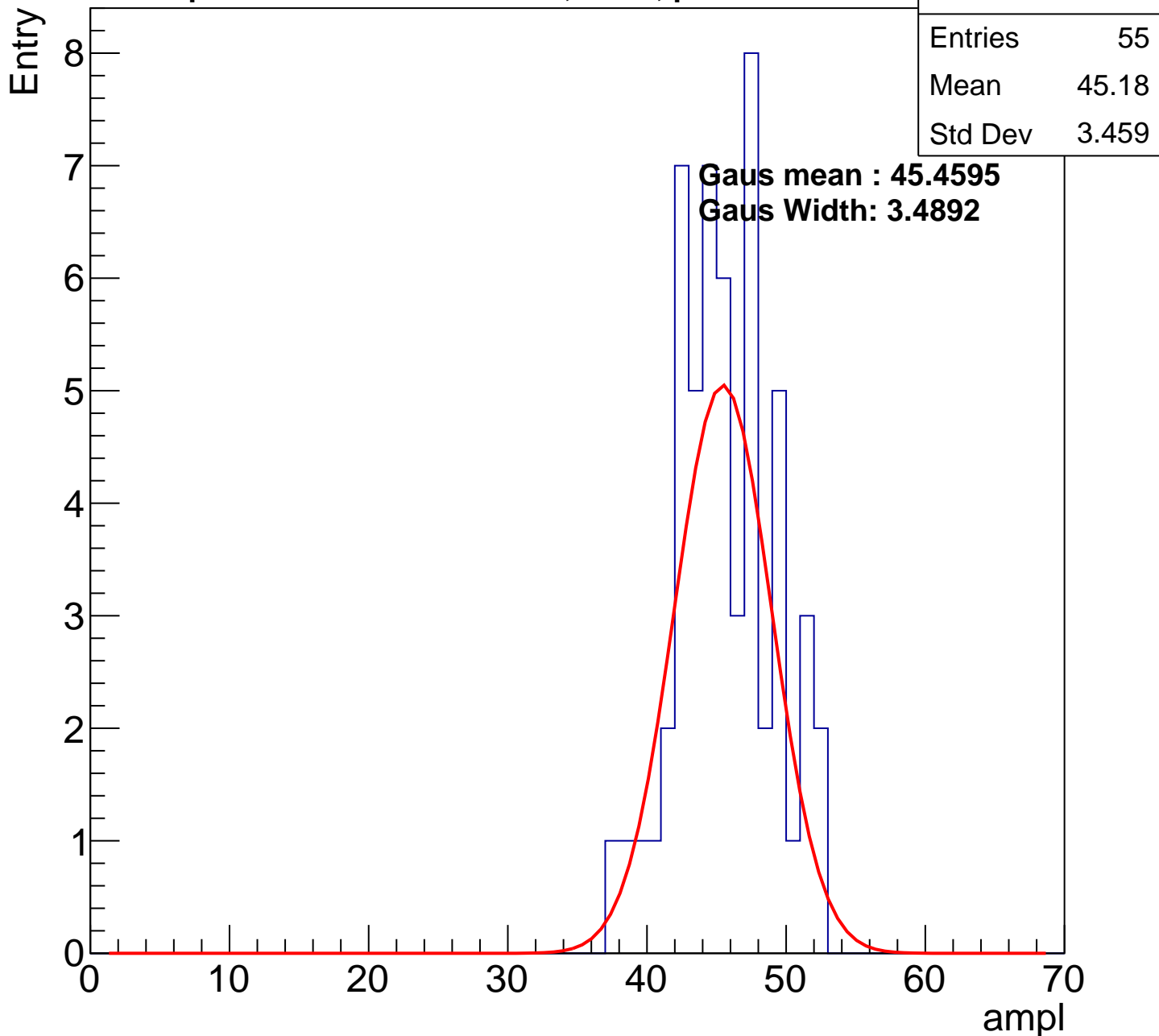
**Gaus mean : 38.7755**

**Gaus Width: 3.6889**



# B0L001S, U5-ch89, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

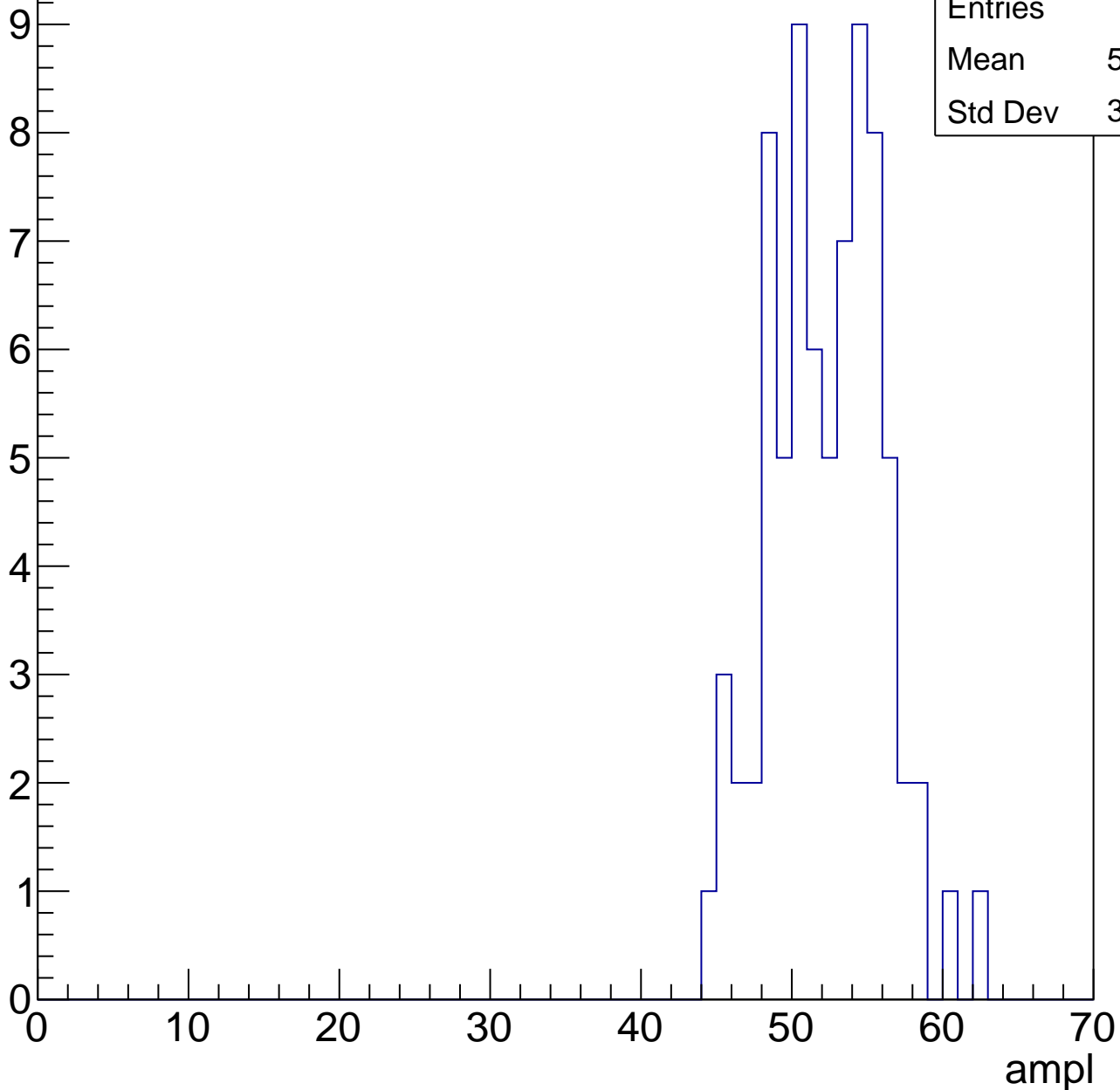


# B0L001S, U5-ch89, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	76
Mean	51.83
Std Dev	3.676

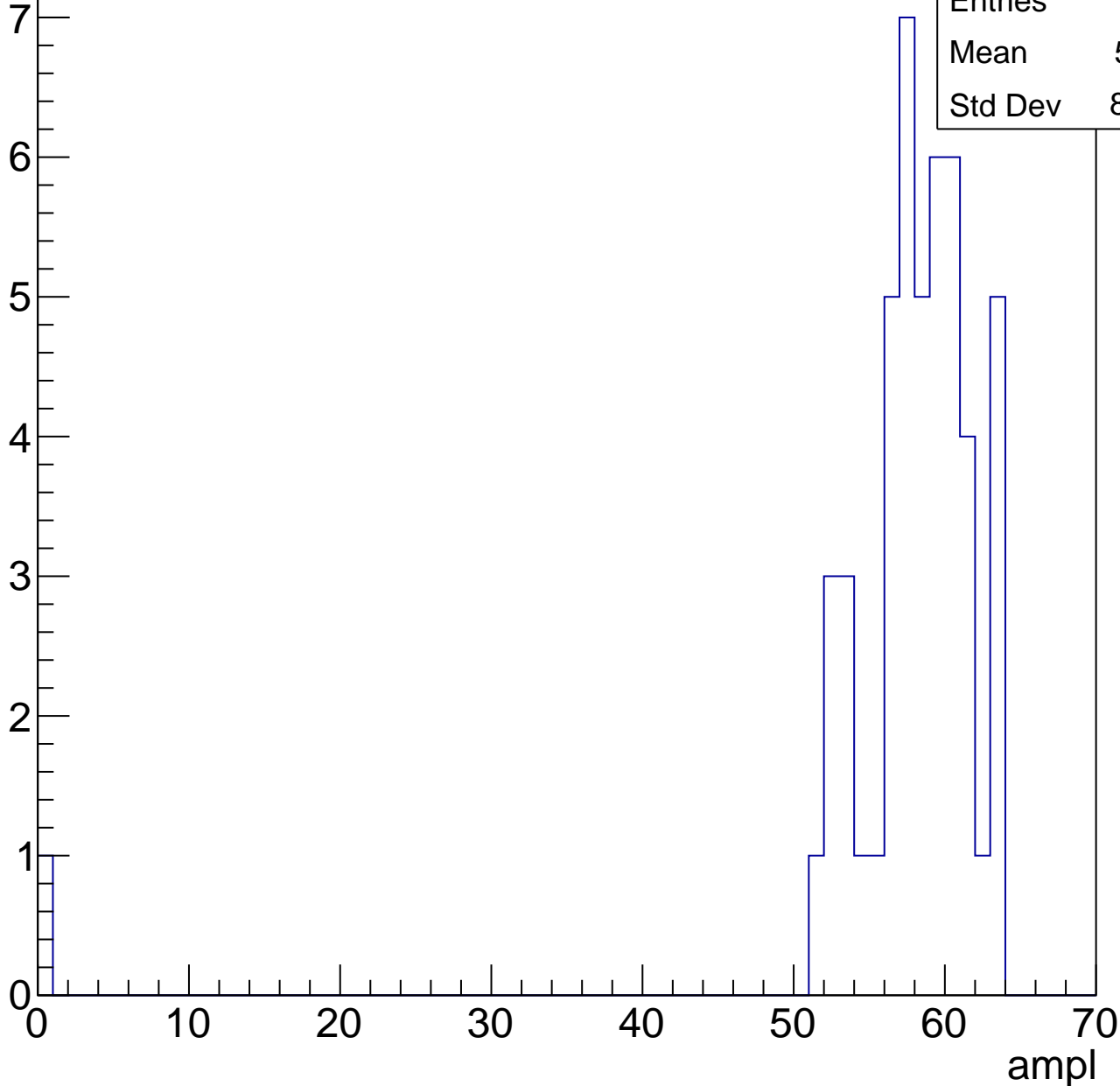


# B0L001S, U5-ch89, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	49
Mean	56.71
Std Dev	8.776

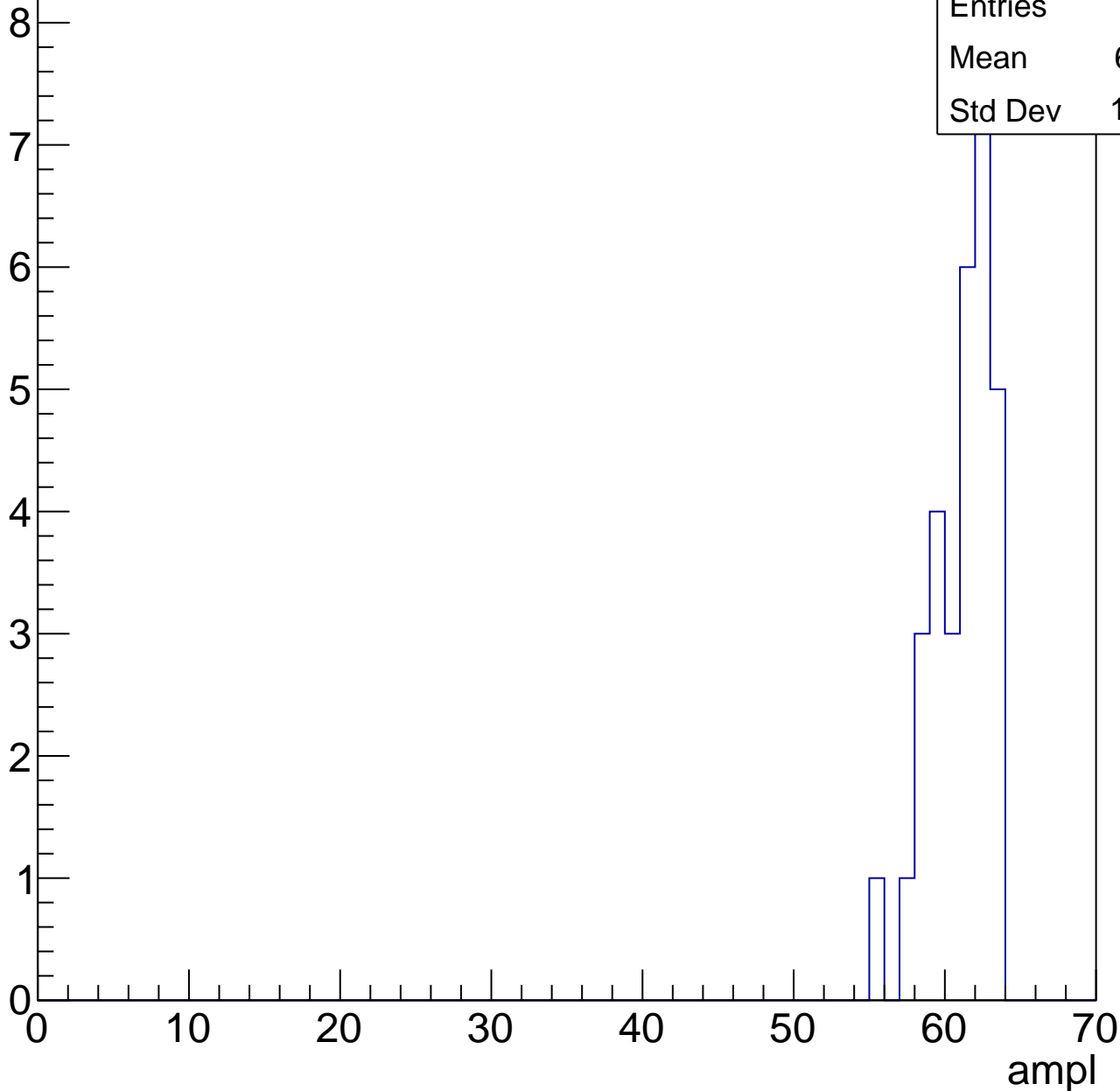


# B0L001S, U5-ch89, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	31
Mean	60.61
Std Dev	1.979



# B0L001S, U5-ch89, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch89, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch90, adc0

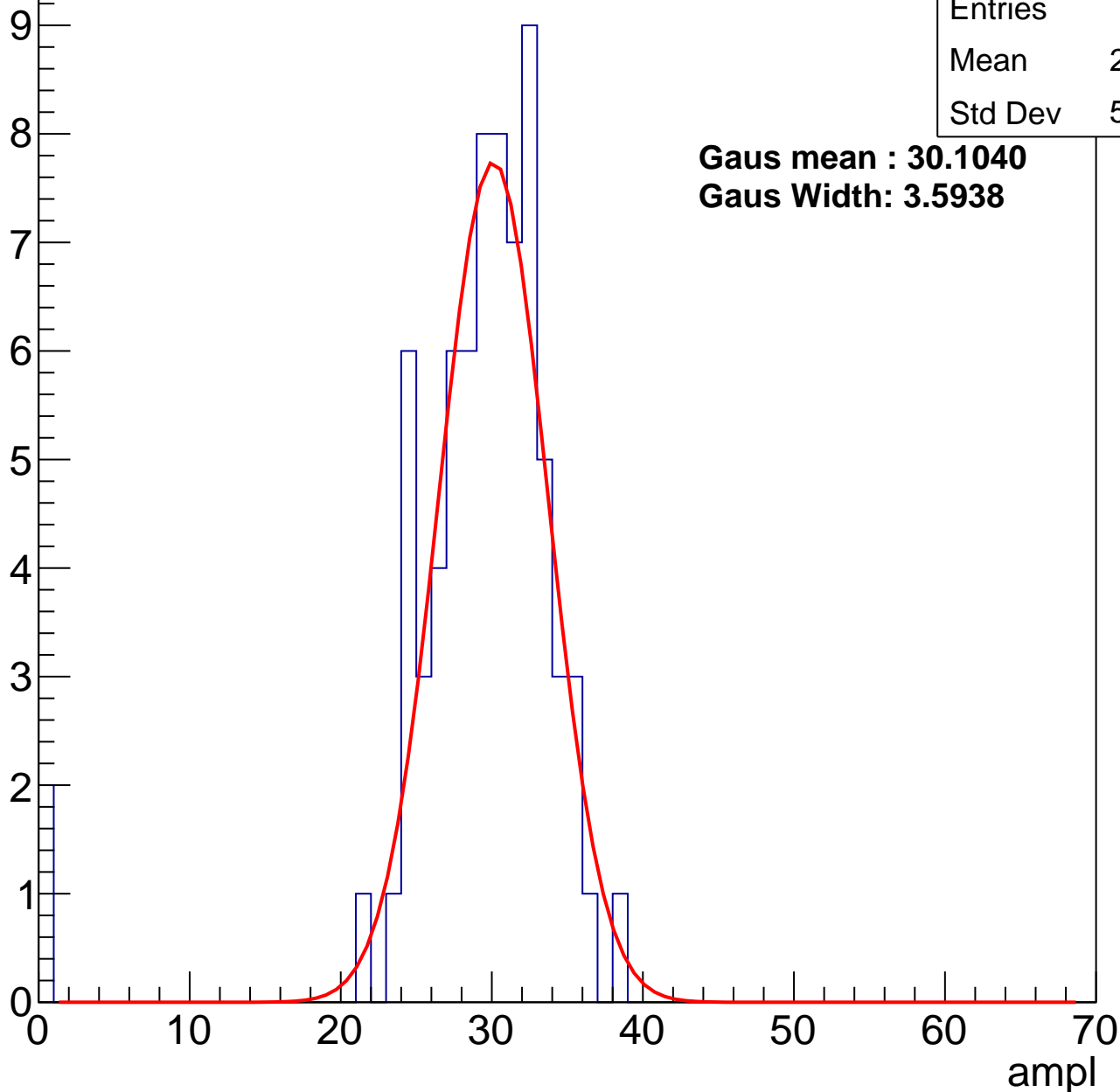
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	28.65
Std Dev	5.867

**Gaus mean : 30.1040**

**Gaus Width: 3.5938**



# B0L001S, U5-ch90, adc1

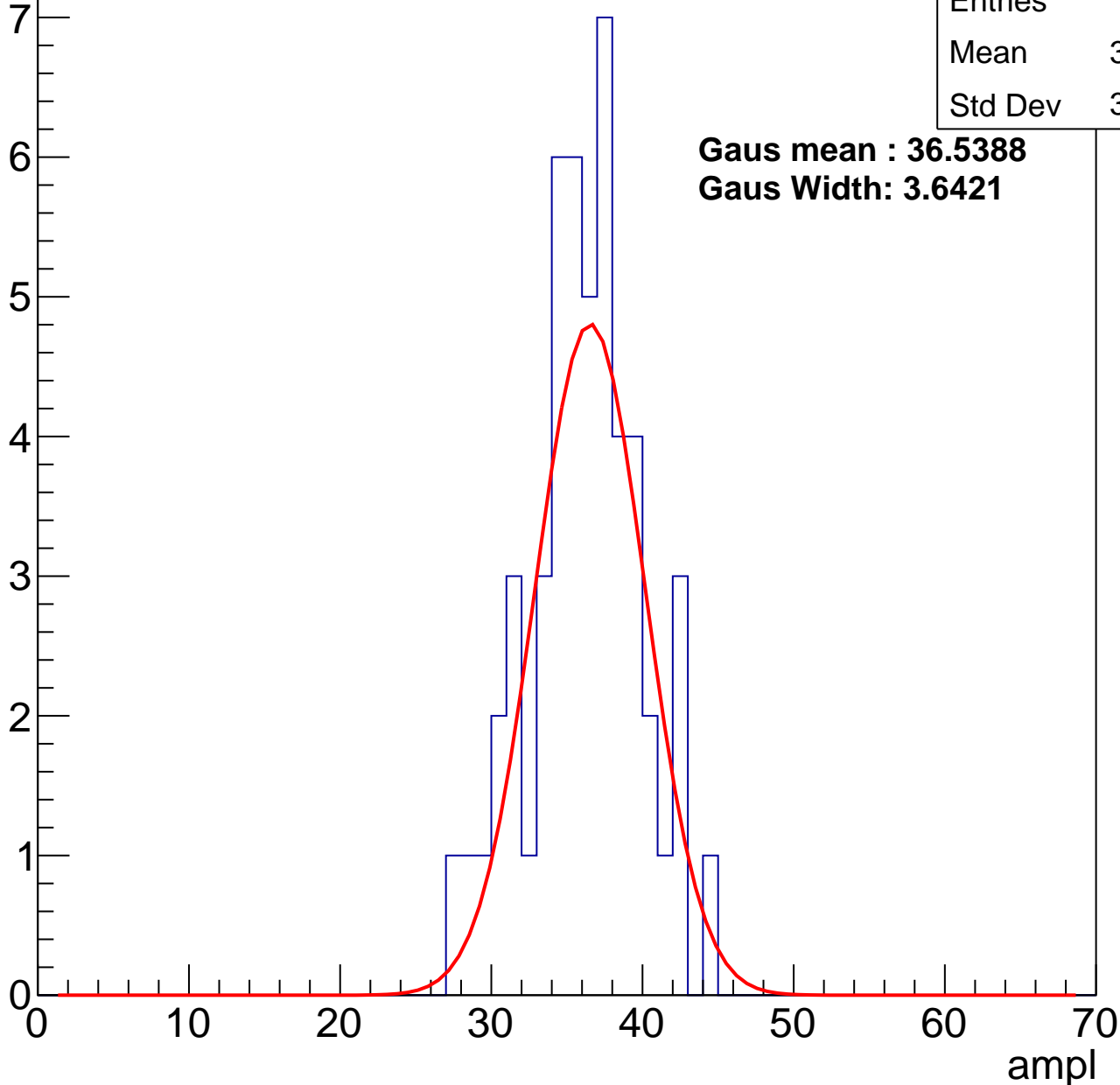
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	51
Mean	35.69
Std Dev	3.697

**Gaus mean : 36.5388**

**Gaus Width: 3.6421**



# B0L001S, U5-ch90, adc2

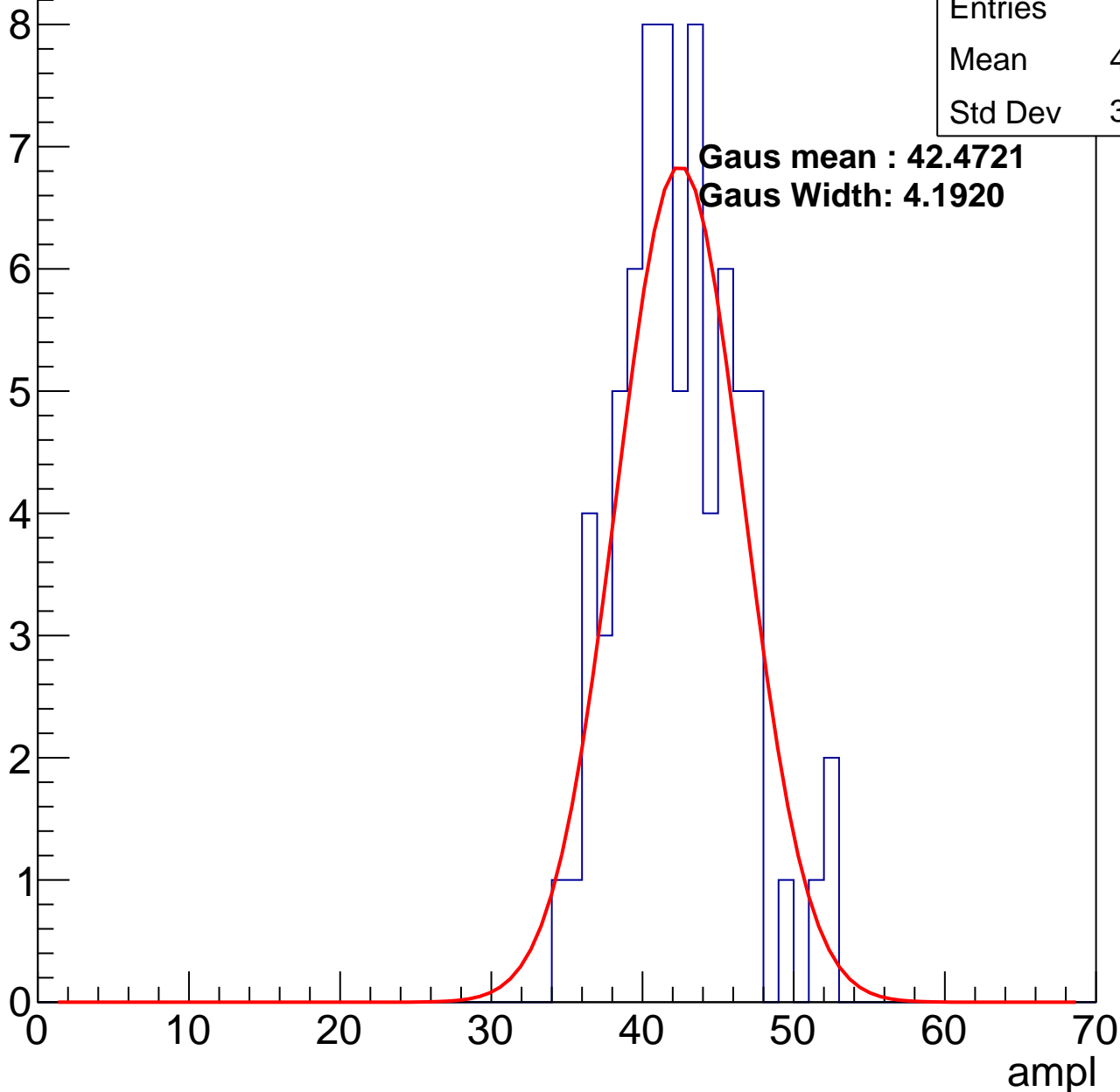
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	41.99
Std Dev	3.915

**Gaus mean : 42.4721**

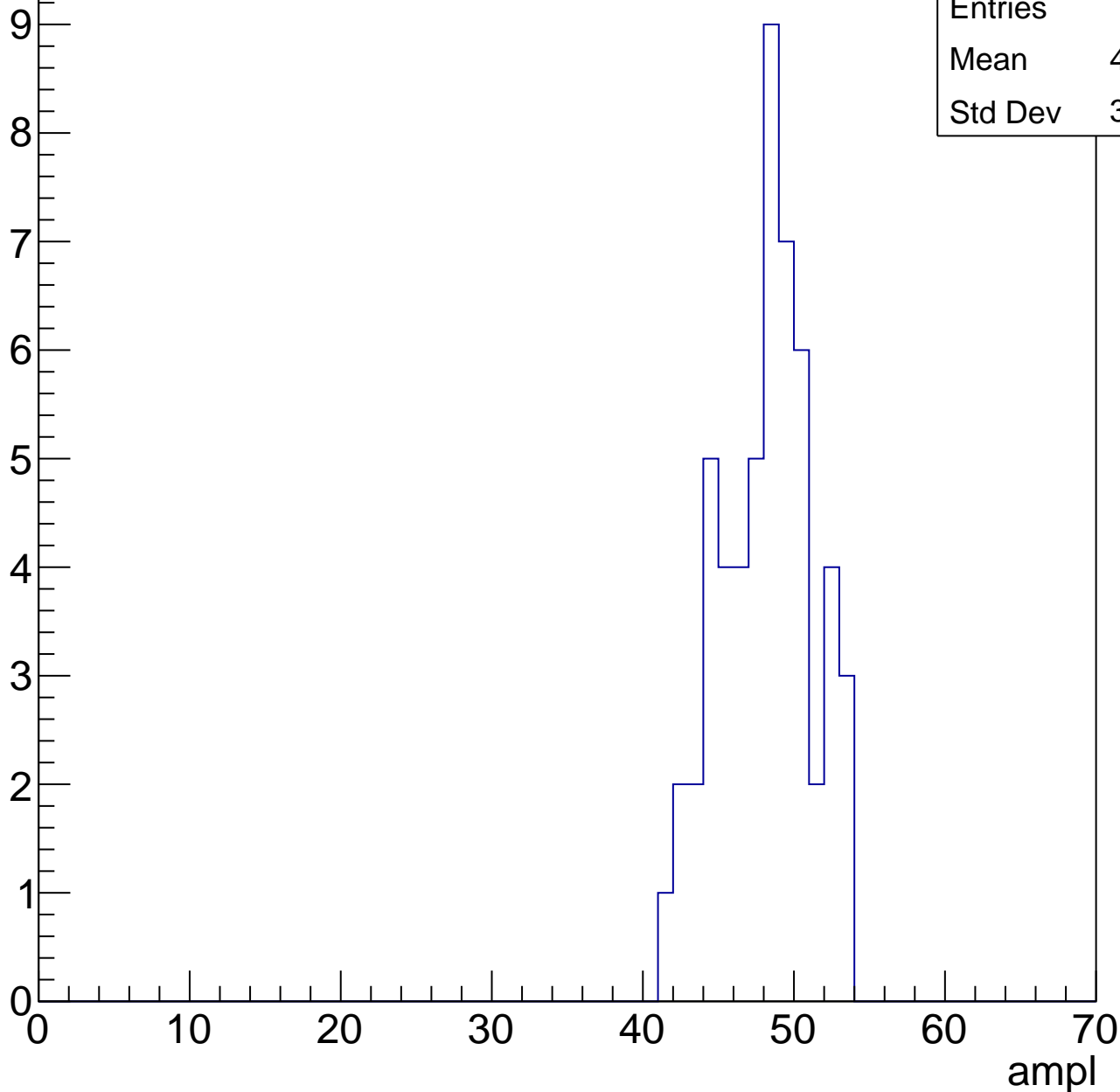
**Gaus Width: 4.1920**



# B0L001S, U5-ch90, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

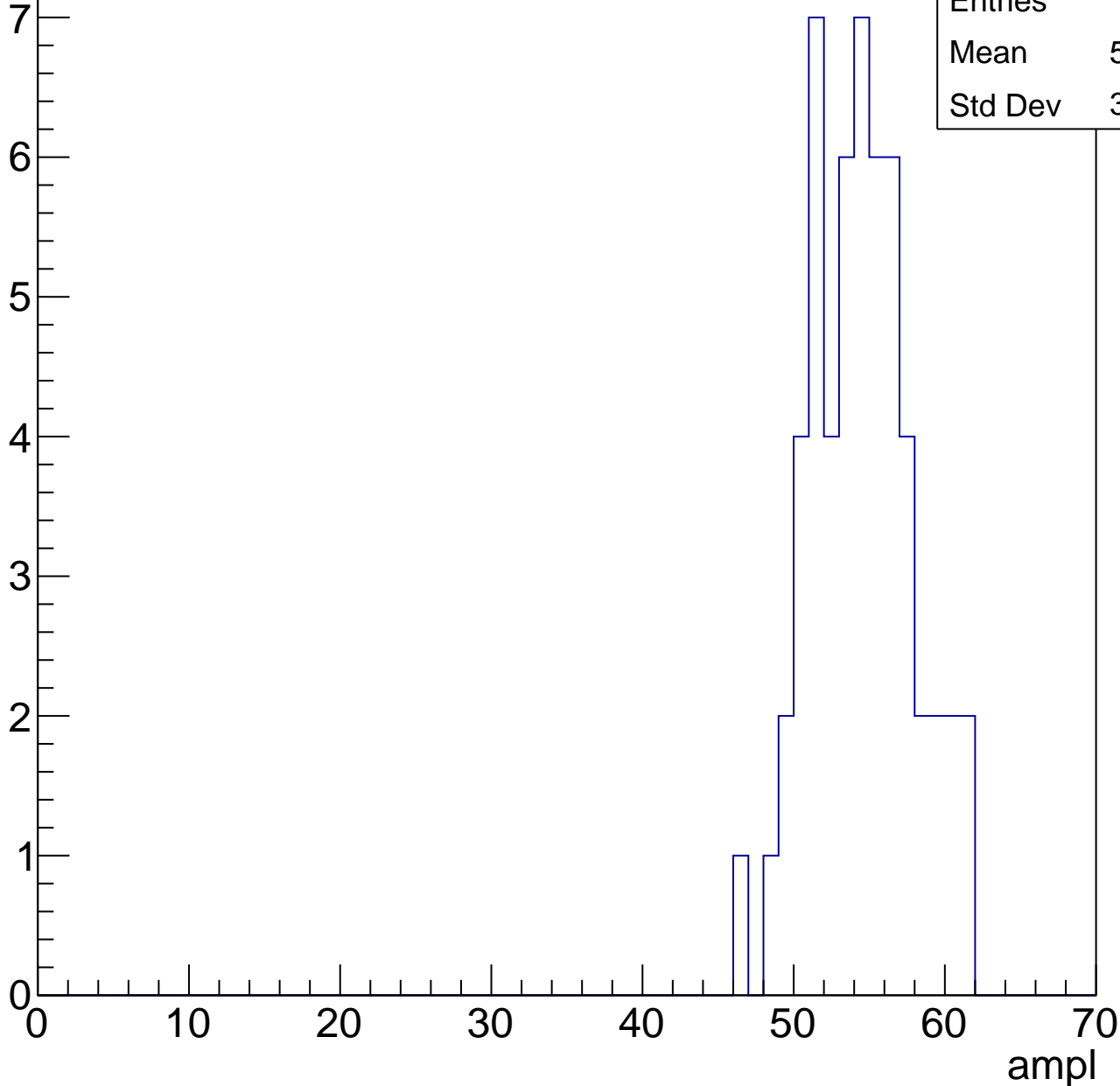


# B0L001S, U5-ch90, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	53.98
Std Dev	3.319



# B0L001S, U5-ch90, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

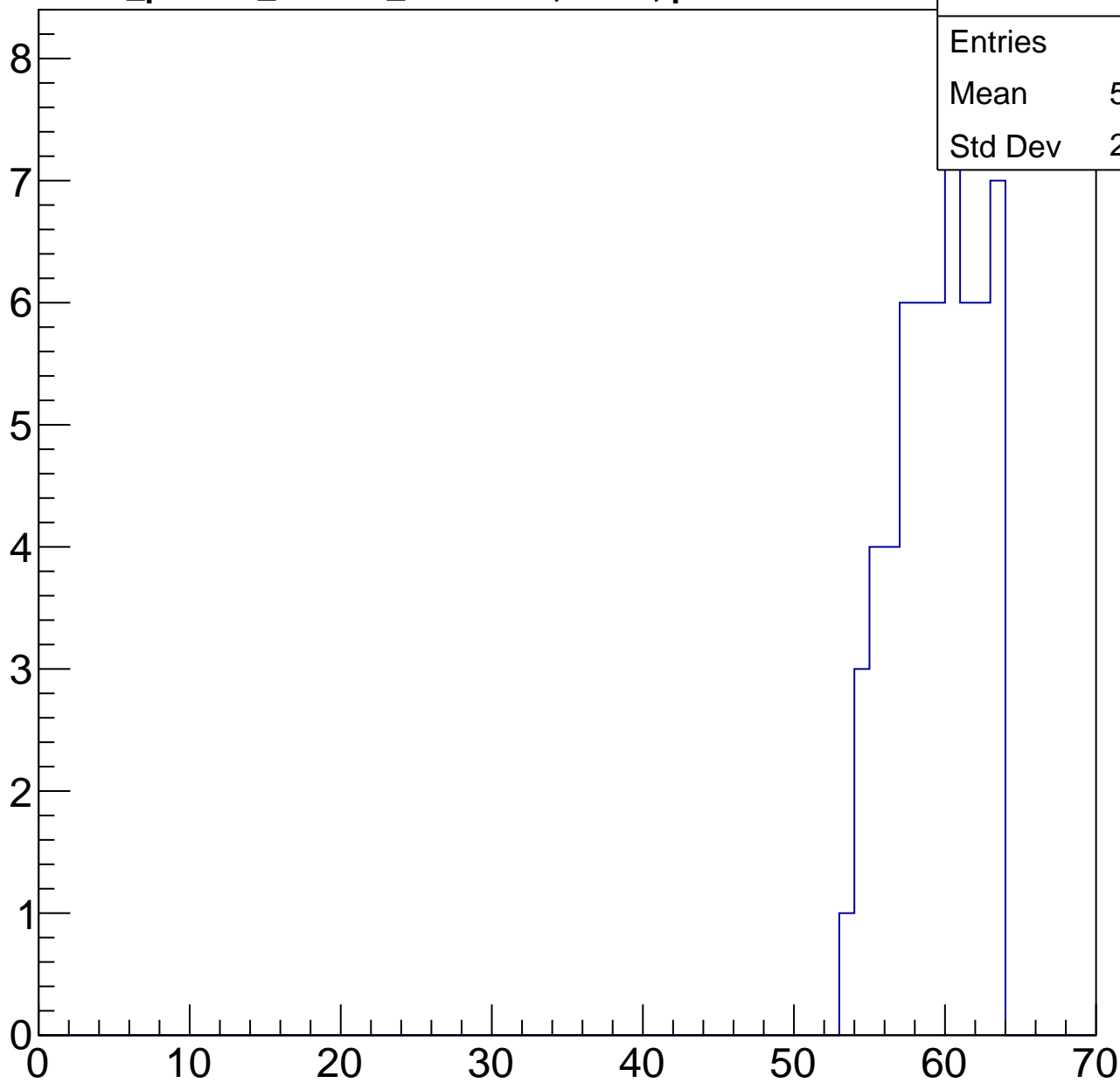
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	57
Mean	58.98
Std Dev	2.775

ampl

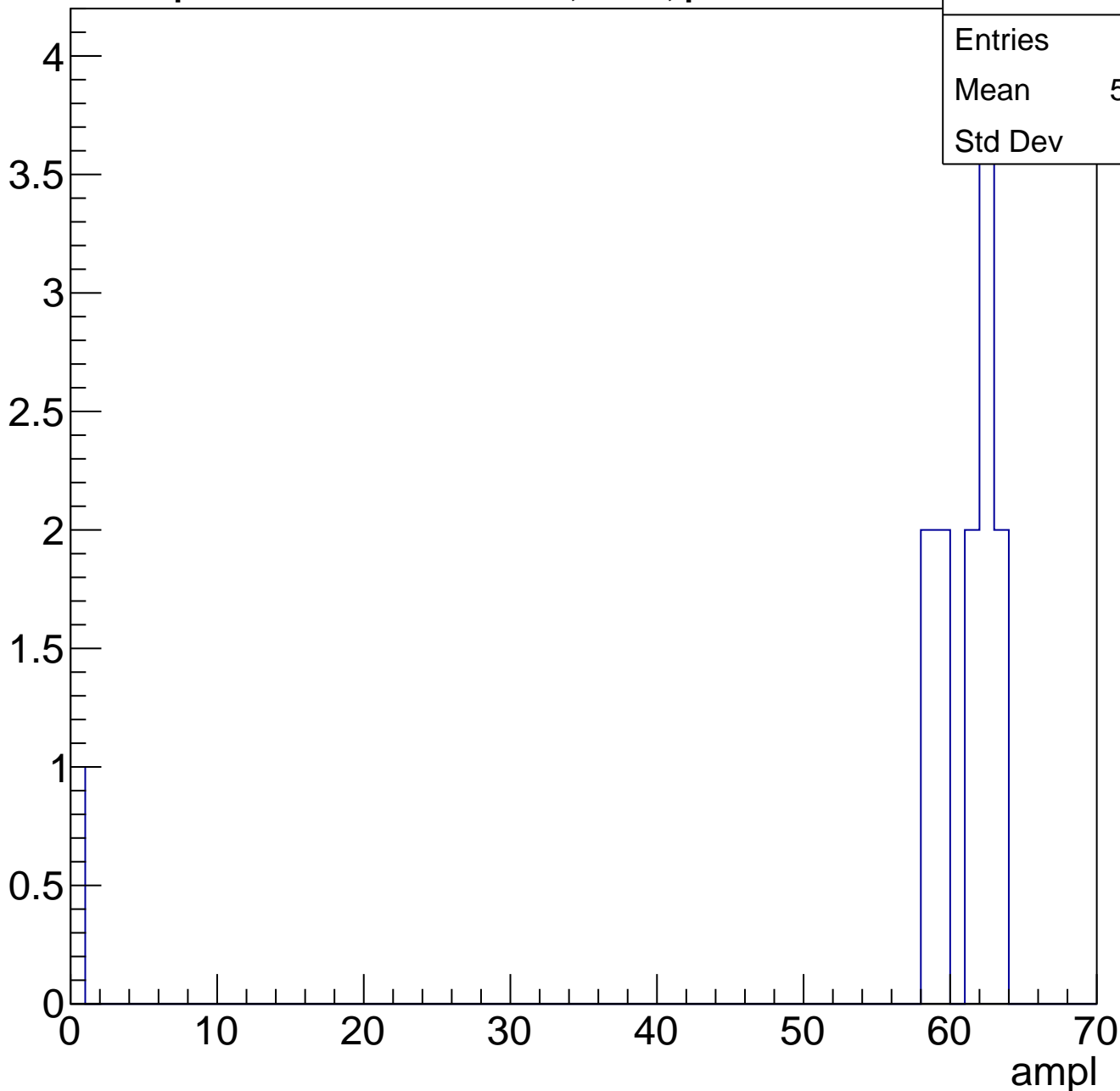
0 10 20 30 40 50 60 70



# B0L001S, U5-ch90, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

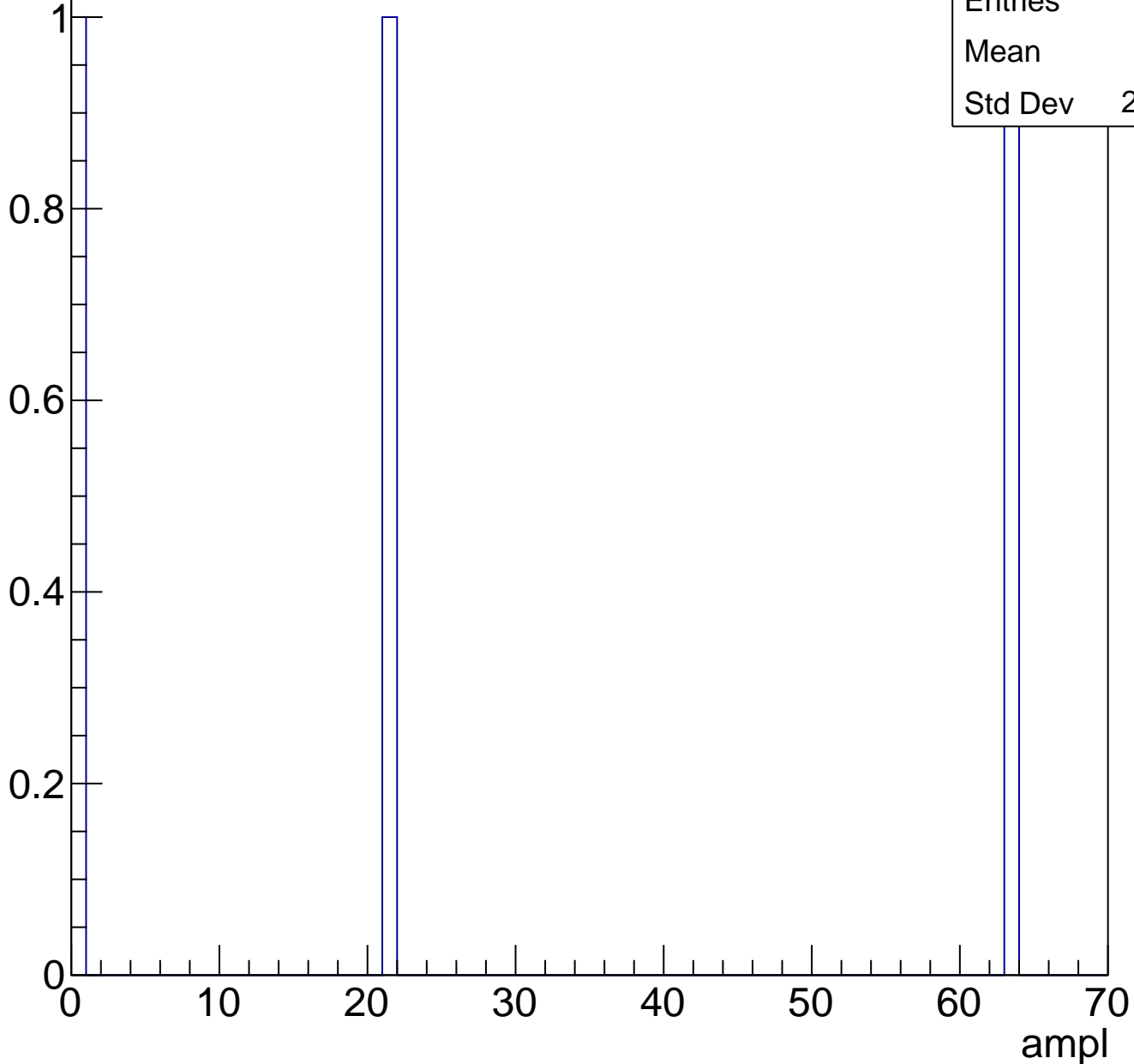




# B0L001S, U5-ch90, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	3
Mean	28
Std Dev	26.19

# B0L001S, U5-ch91, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	82
Mean	30.12
Std Dev	3.5

**Gaus mean : 30.7531**

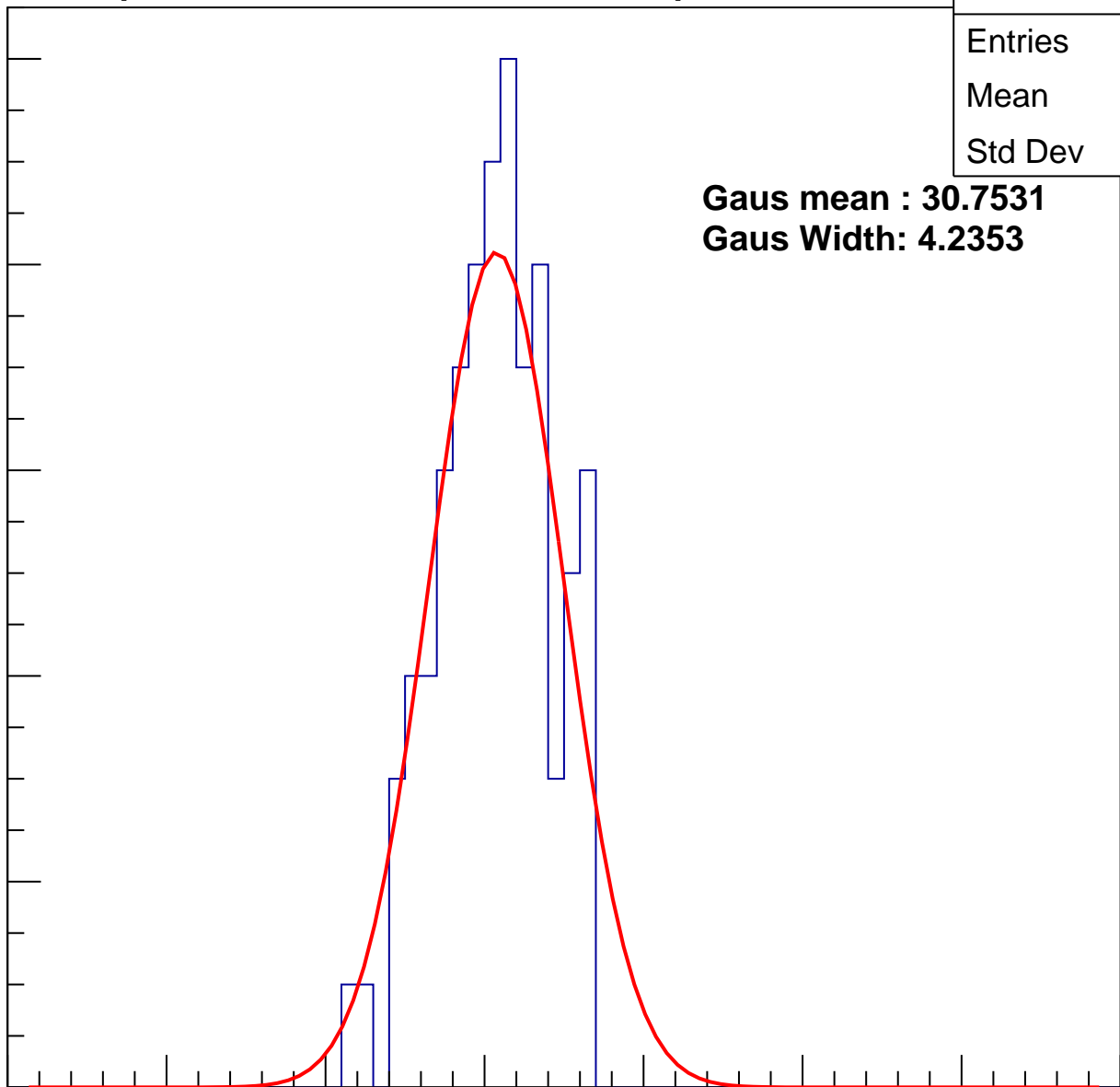
**Gaus Width: 4.2353**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B0L001S, U5-ch91, adc1

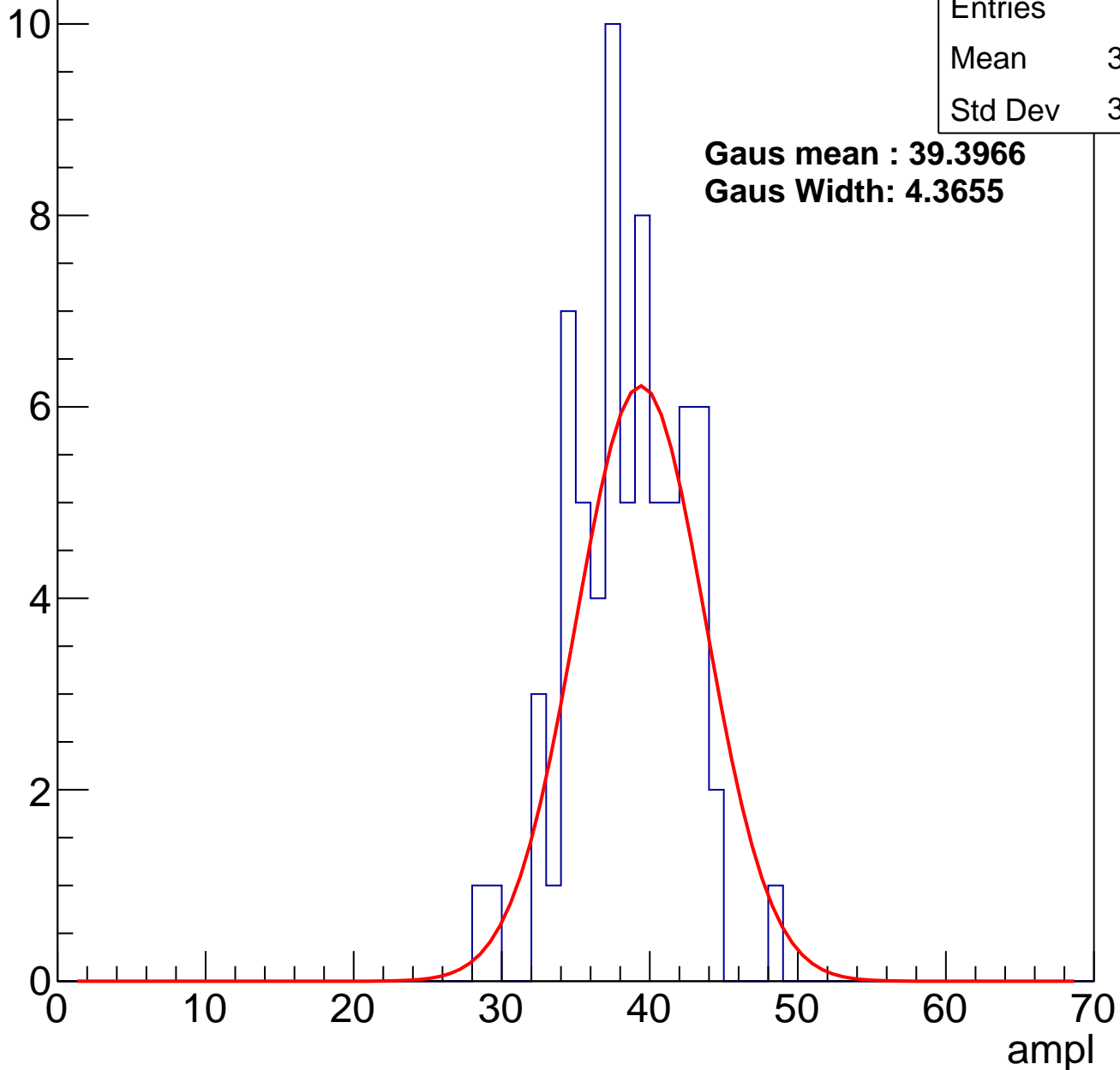
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	70
Mean	38.09
Std Dev	3.756

**Gaus mean : 39.3966**

**Gaus Width: 4.3655**

Entry



# B0L001S, U5-ch91, adc2

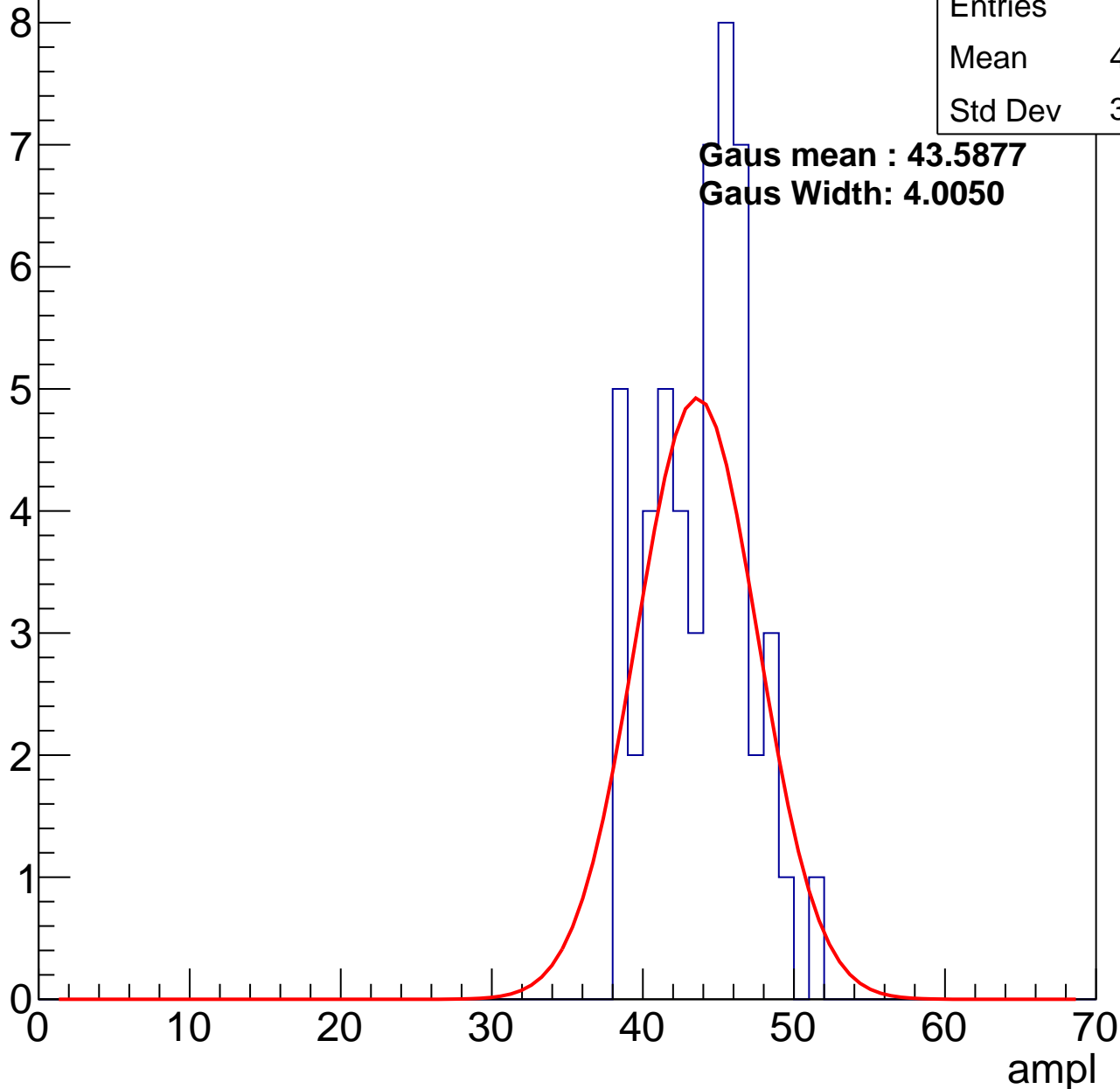
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	43.42
Std Dev	3.152

**Gaus mean : 43.5877**

**Gaus Width: 4.0050**

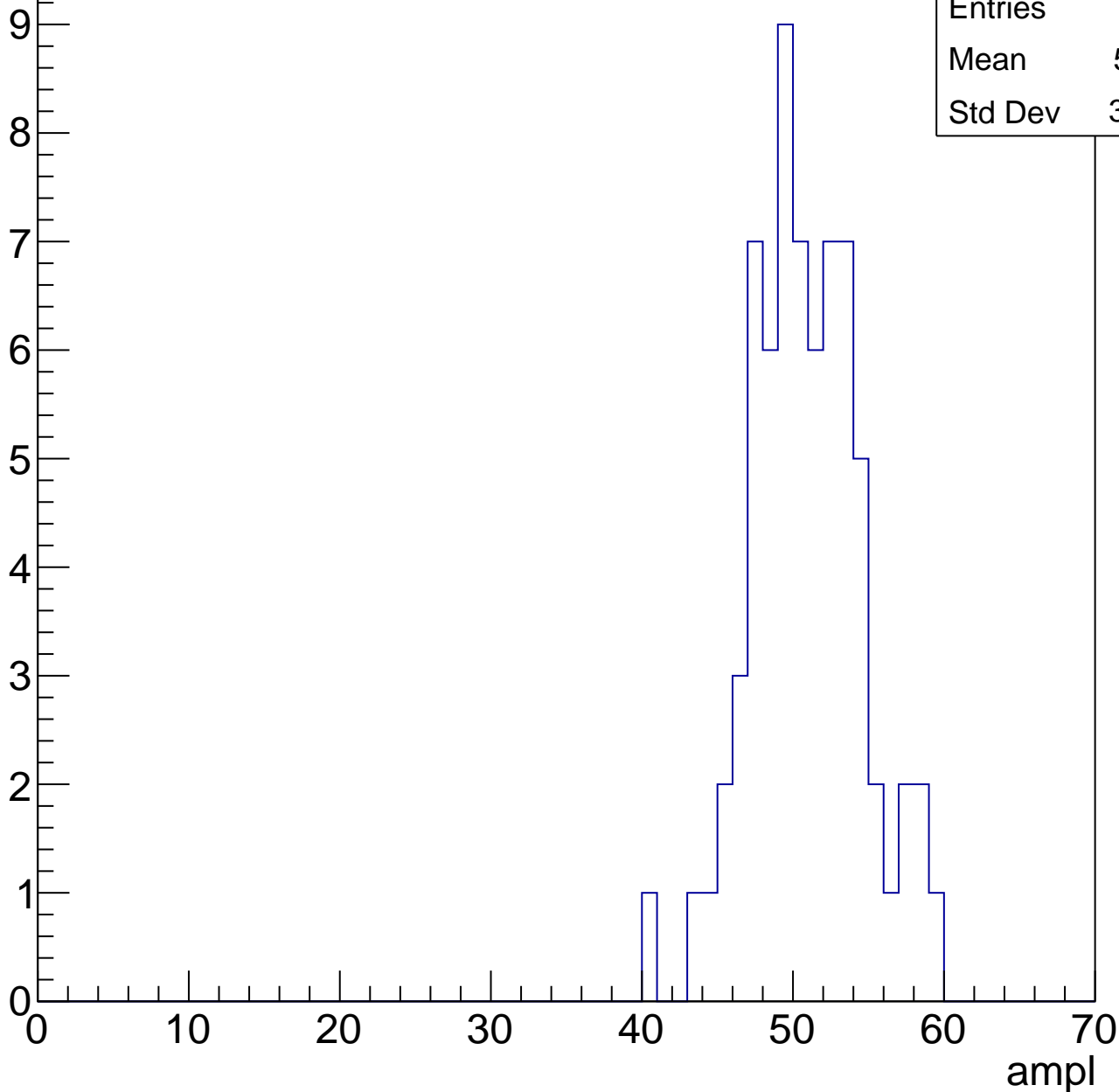


# B0L001S, U5-ch91, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	50.41
Std Dev	3.659

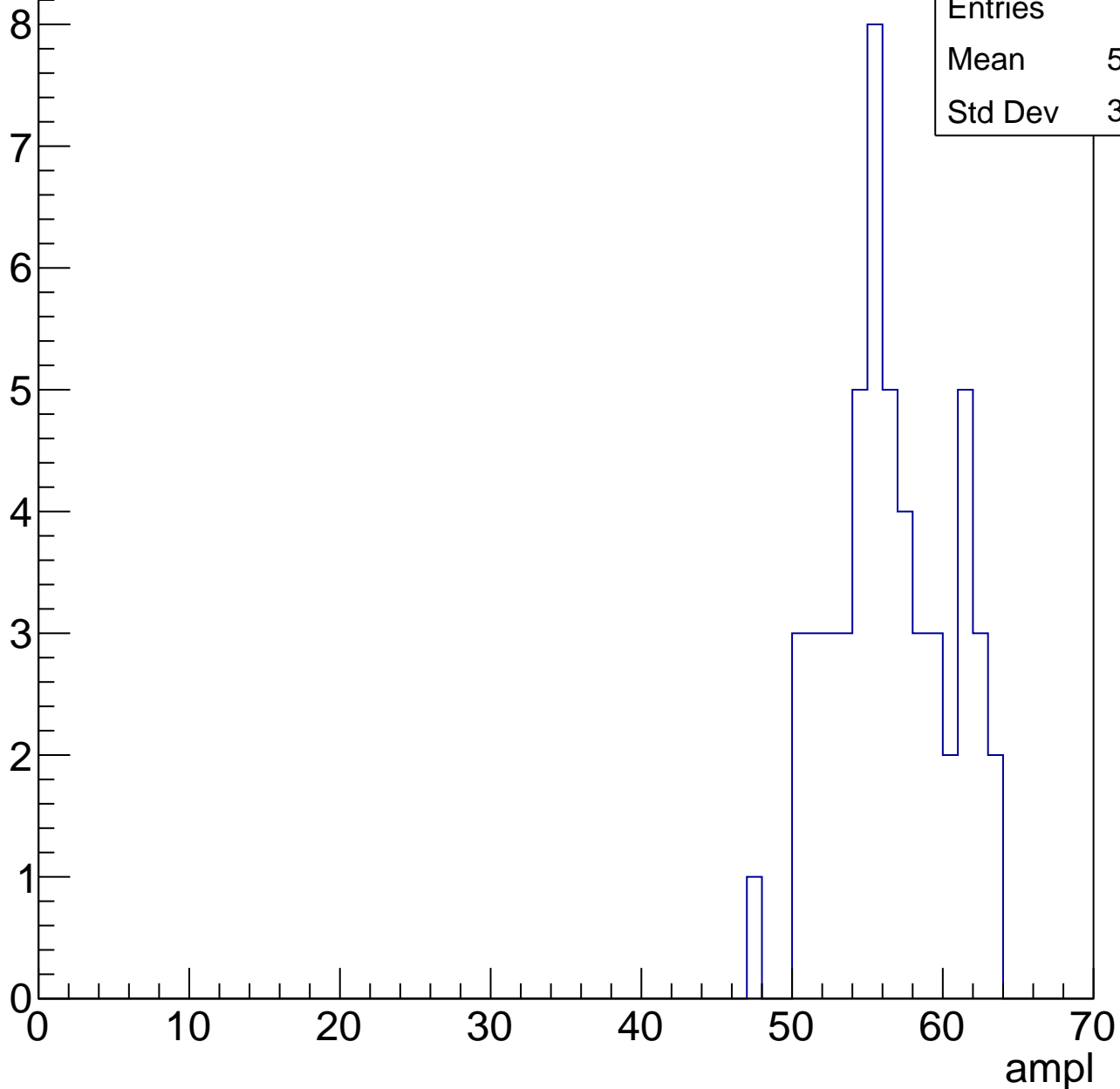


# B0L001S, U5-ch91, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	56.06
Std Dev	3.819



# B0L001S, U5-ch91, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

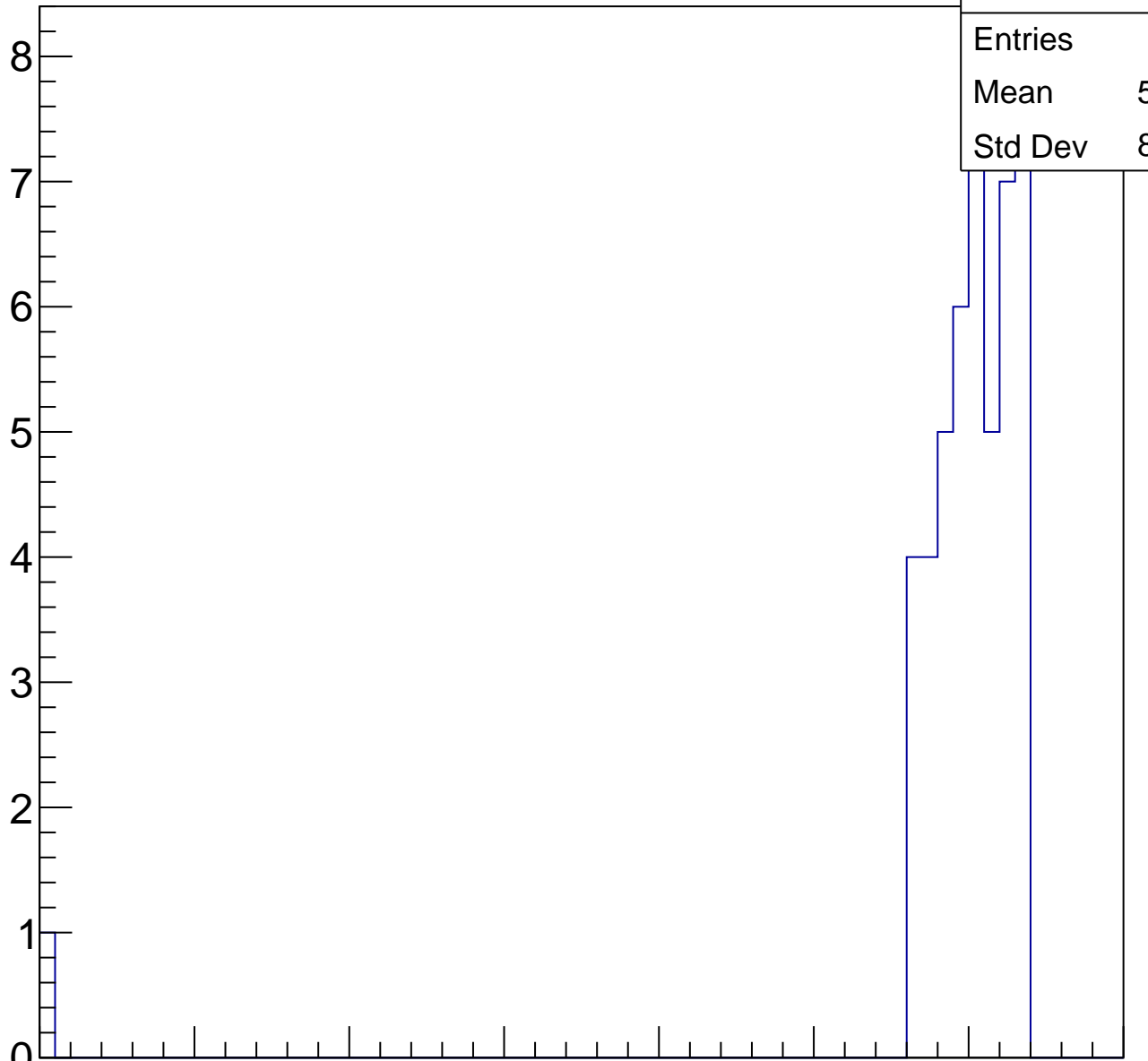
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	48
Mean	58.73
Std Dev	8.843

ampl

0 10 20 30 40 50 60 70



# B0L001S, U5-ch91, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U5-ch91, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U5-ch92, adc0

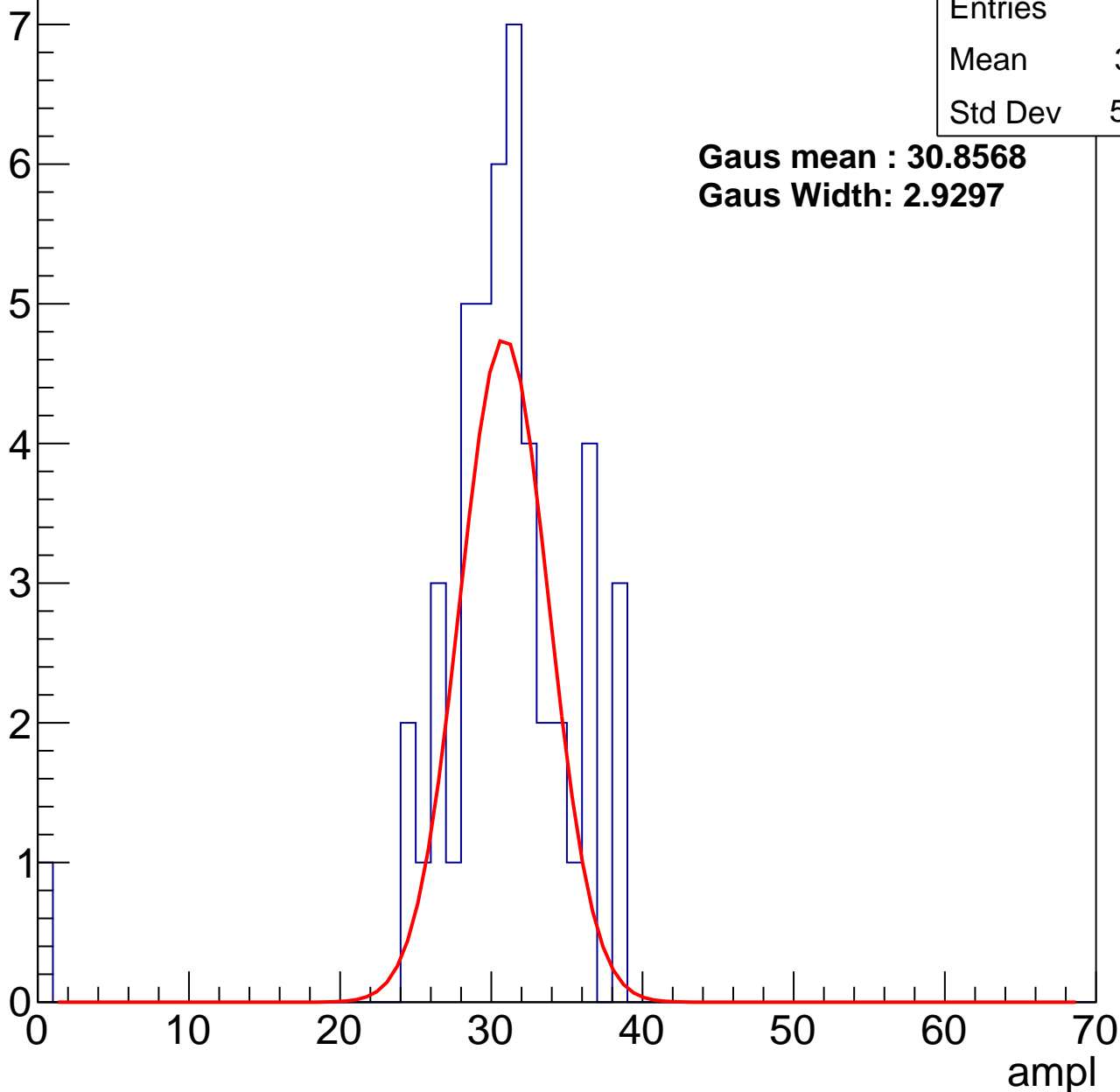
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	47
Mean	30.11
Std Dev	5.673

**Gaus mean : 30.8568**

**Gaus Width: 2.9297**



# B0L001S, U5-ch92, adc1

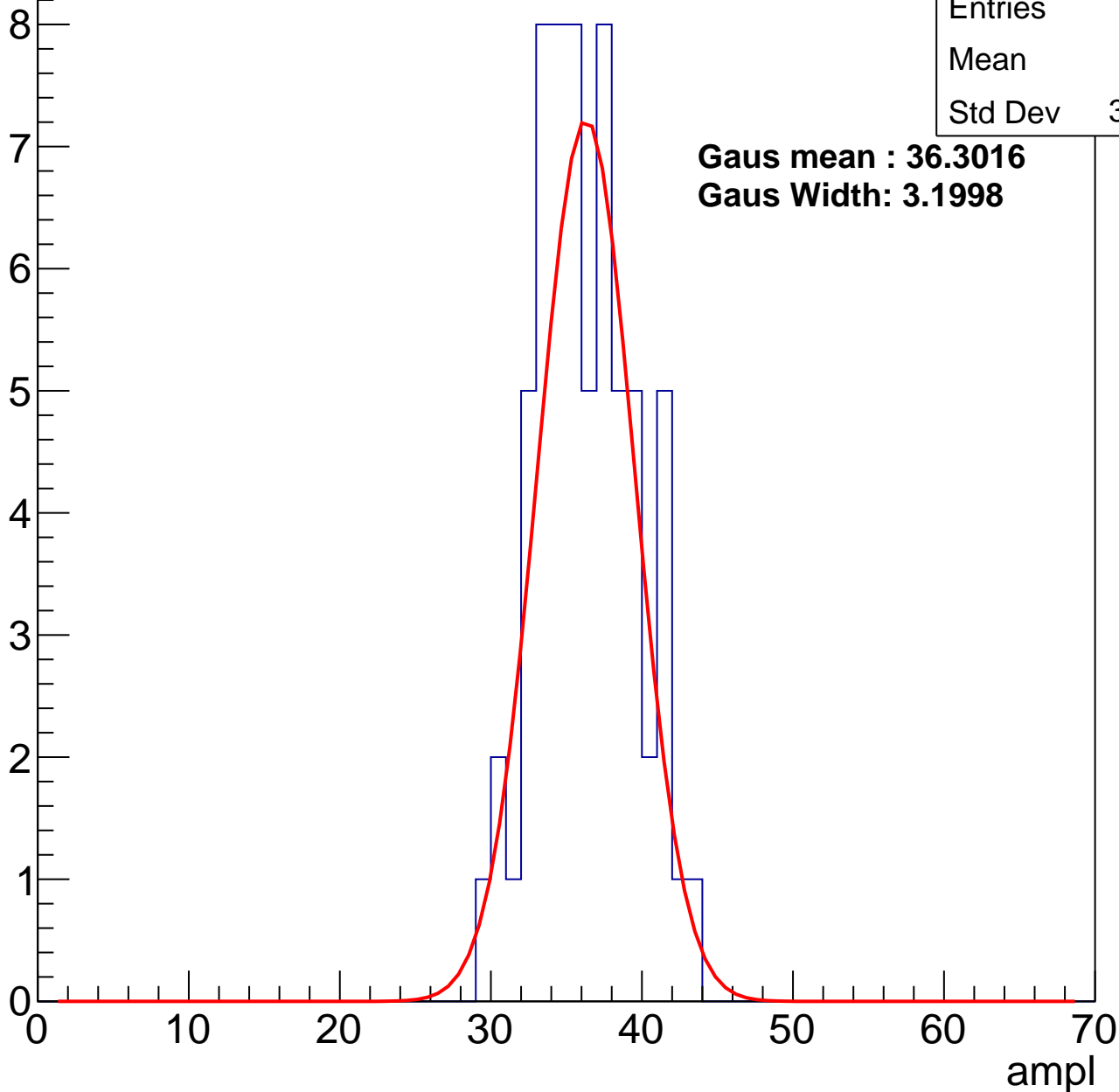
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	35.8
Std Dev	3.163

**Gaus mean : 36.3016**

**Gaus Width: 3.1998**



# B0L001S, U5-ch92, adc2

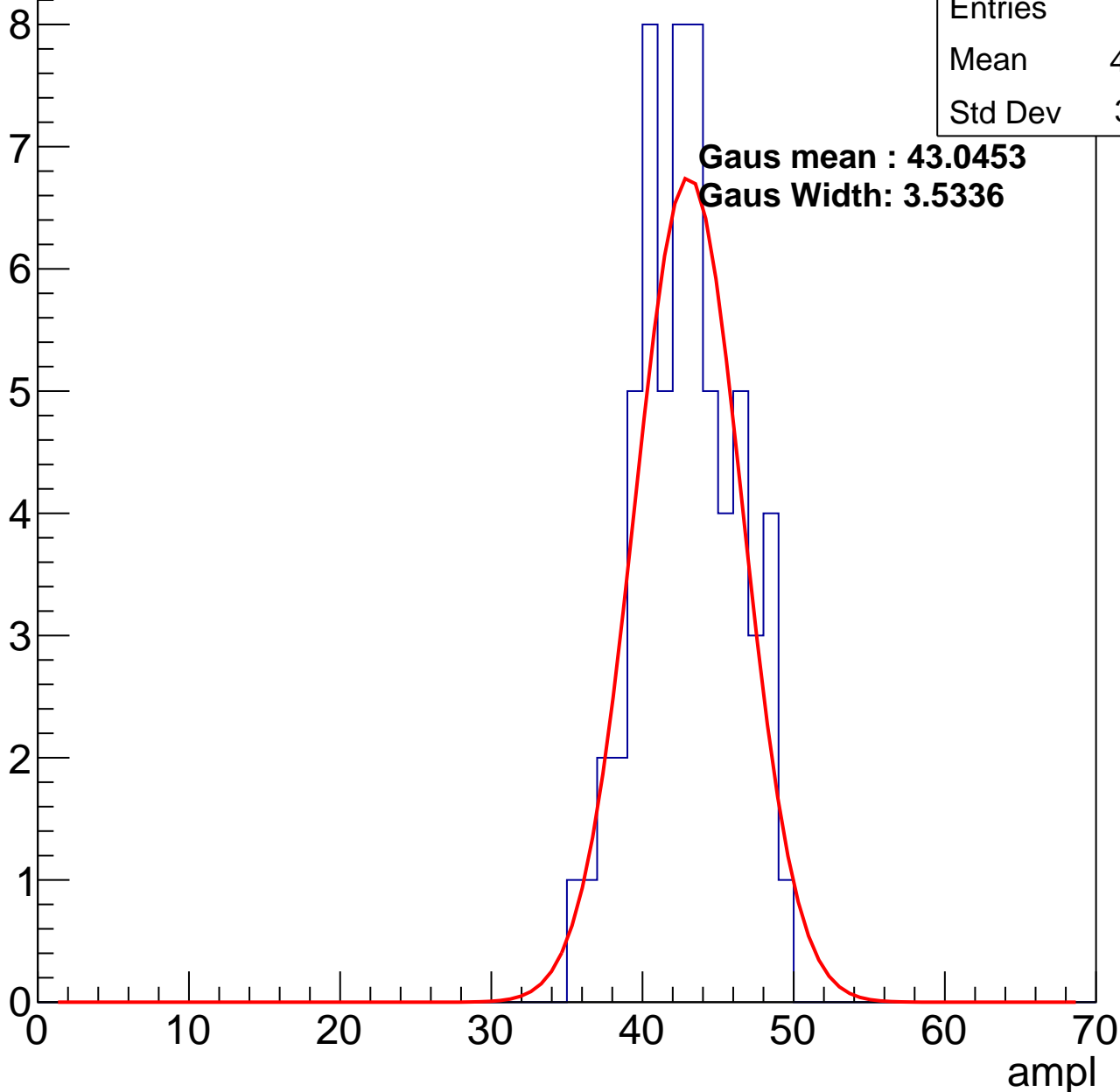
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	42.47
Std Dev	3.231

**Gaus mean : 43.0453**

**Gaus Width: 3.5336**

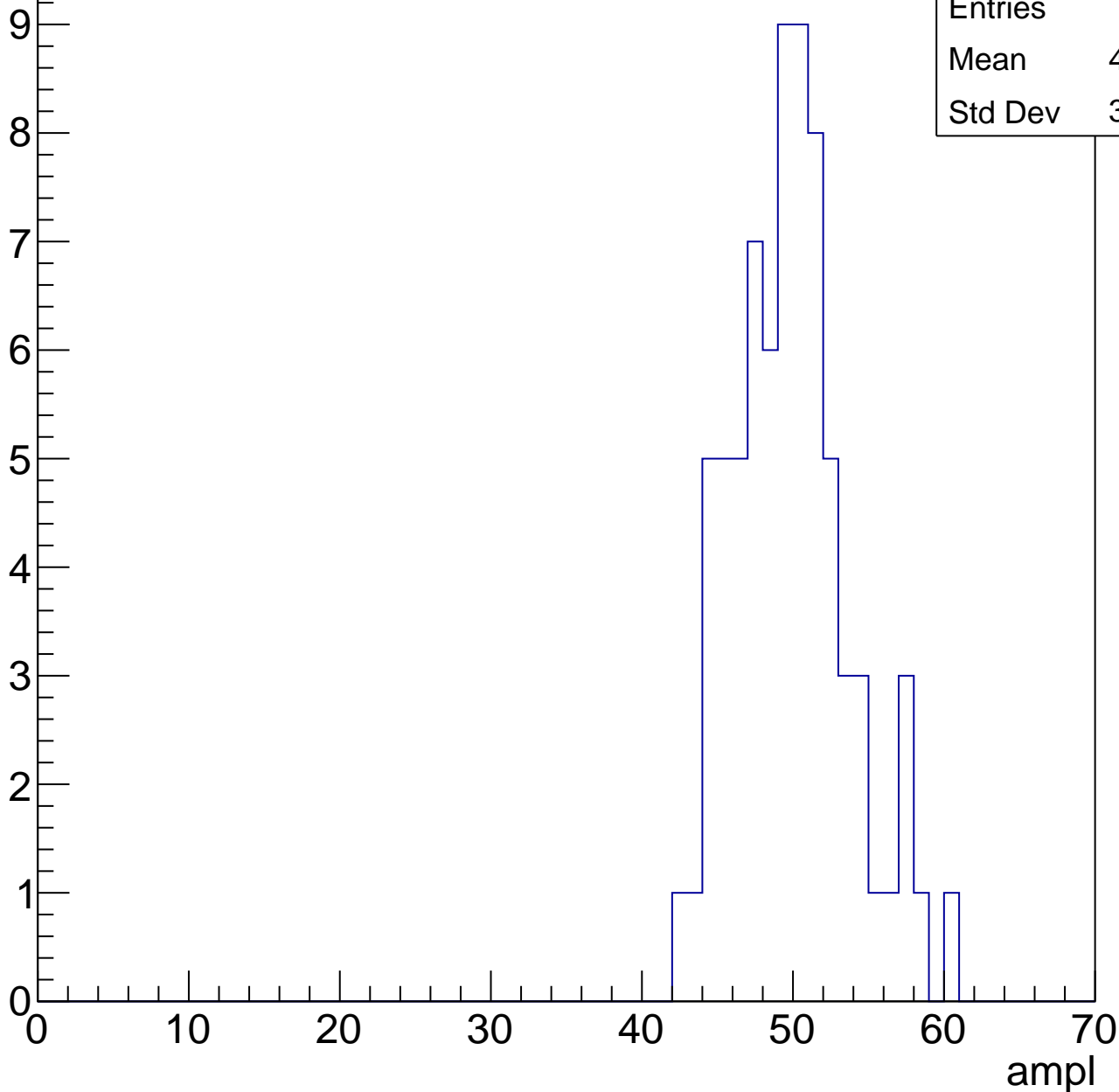


# B0L001S, U5-ch92, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	49.42
Std Dev	3.756

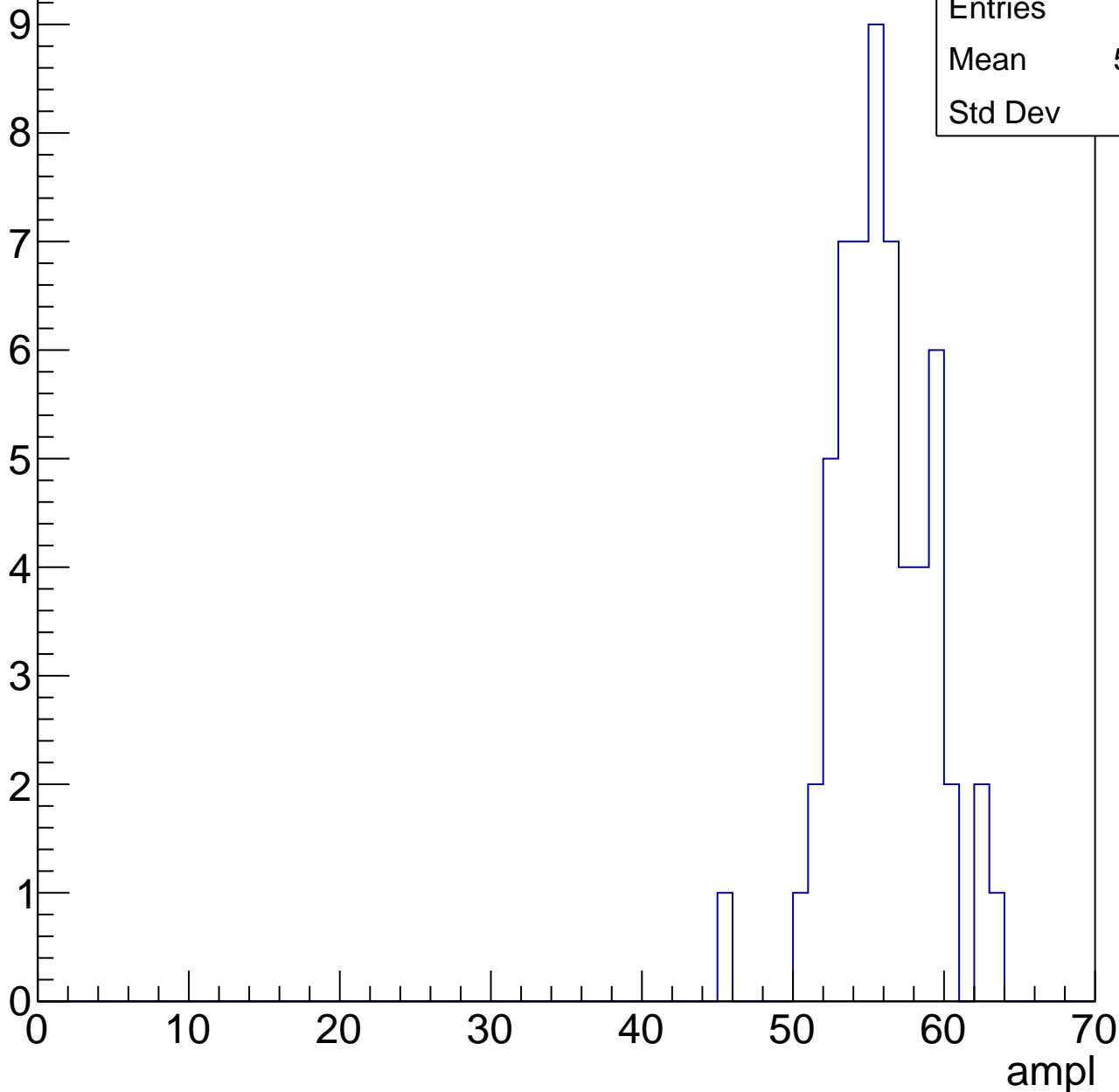


# B0L001S, U5-ch92, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	55.41
Std Dev	3.2



# B0L001S, U5-ch92, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

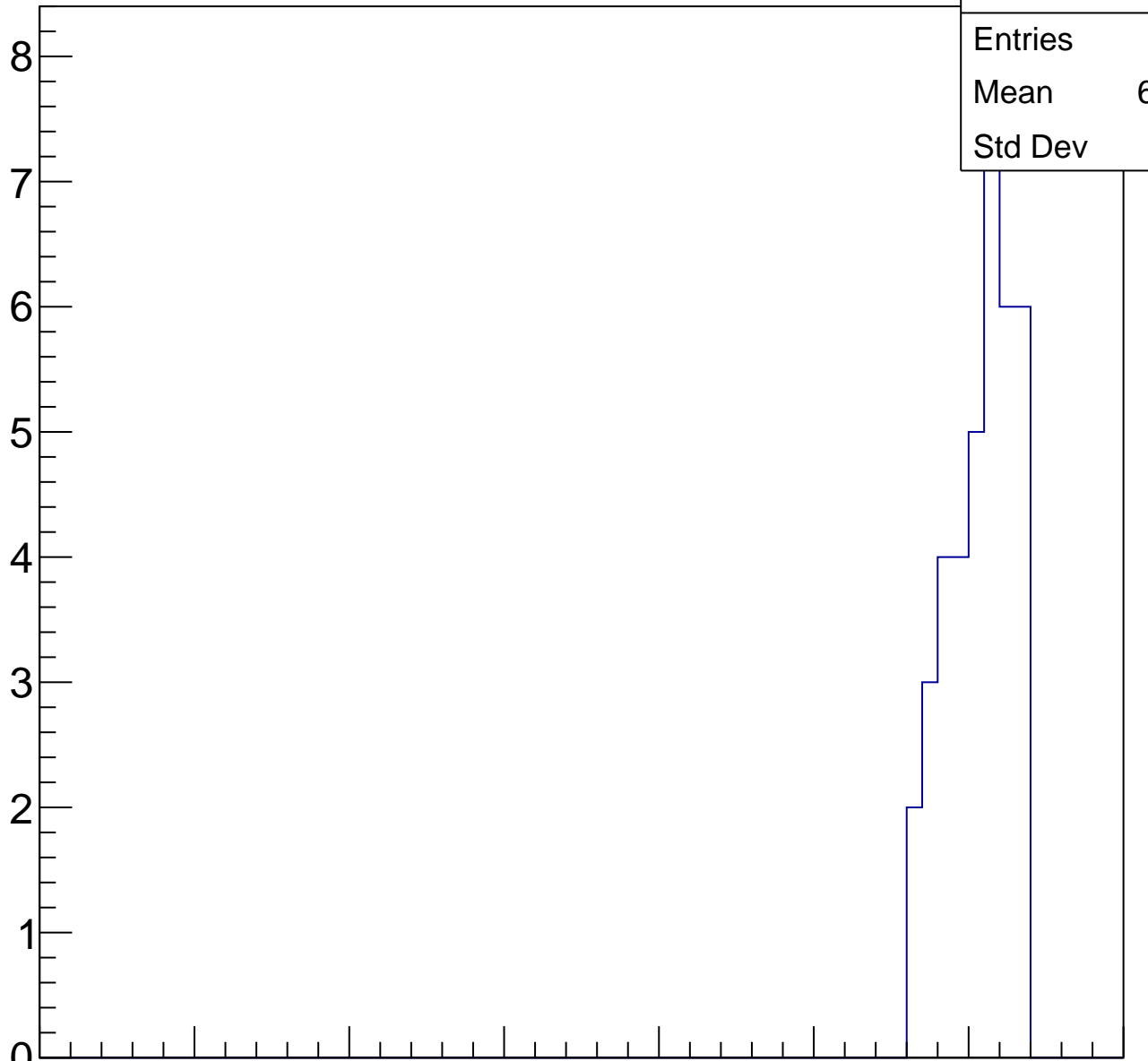
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	38
Mean	60.24
Std Dev	2.07

ampl

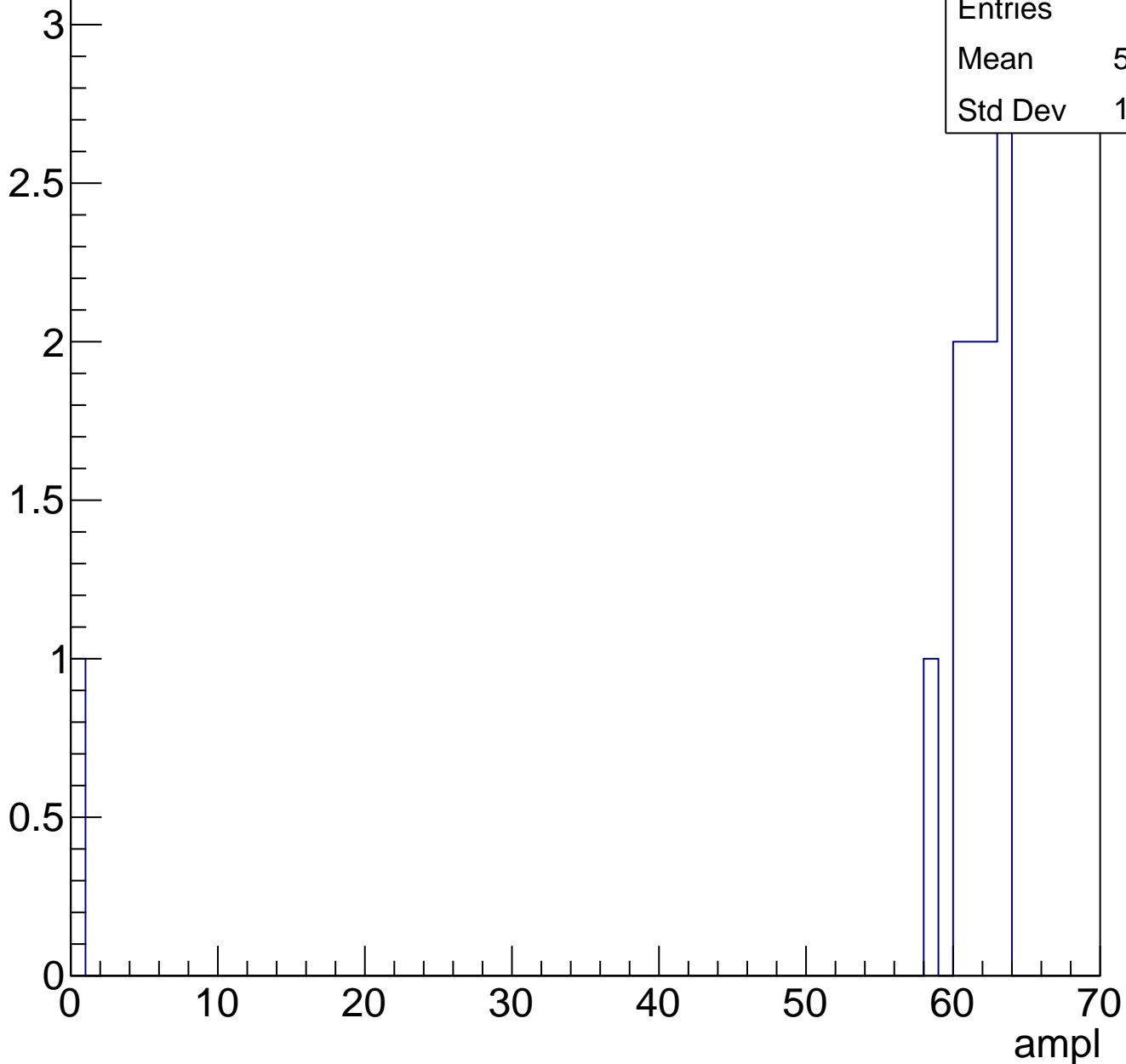
0 10 20 30 40 50 60 70



# B0L001S, U5-ch92, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch92, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch93, adc0

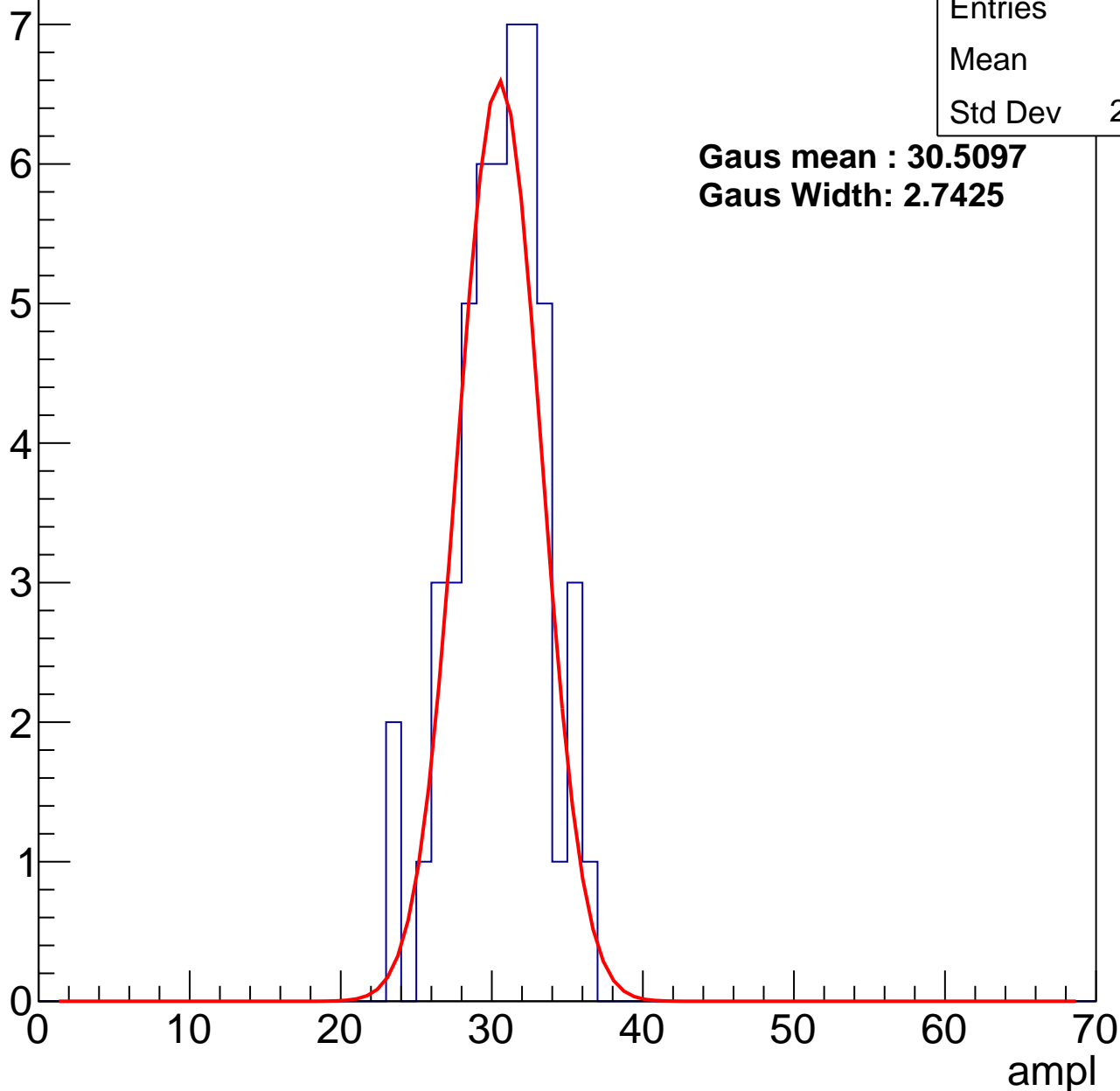
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	50
Mean	30.1
Std Dev	2.934

**Gaus mean : 30.5097**

**Gaus Width: 2.7425**



# B0L001S, U5-ch93, adc1

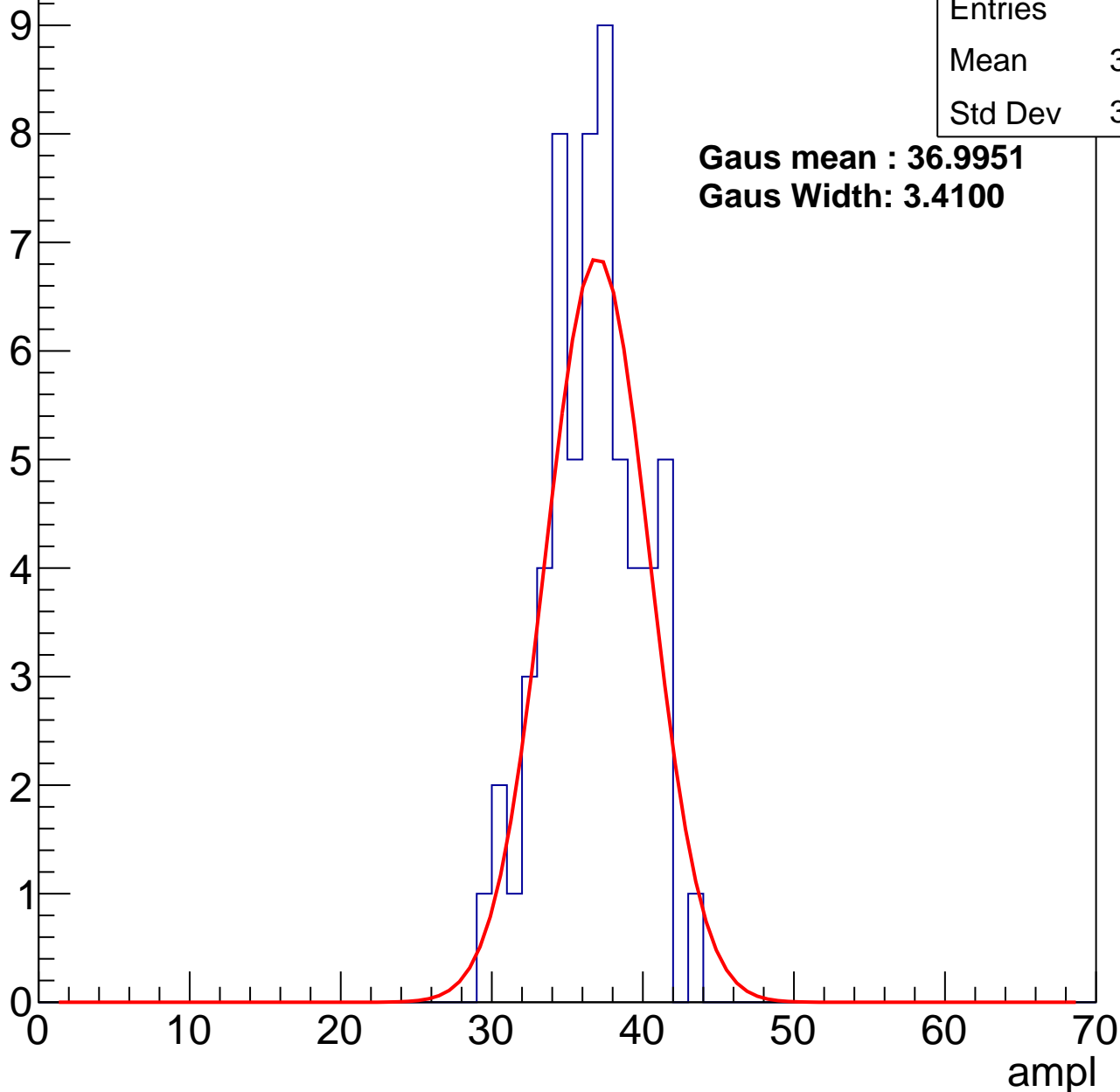
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	36.17
Std Dev	3.078

**Gaus mean : 36.9951**

**Gaus Width: 3.4100**



# B0L001S, U5-ch93, adc2

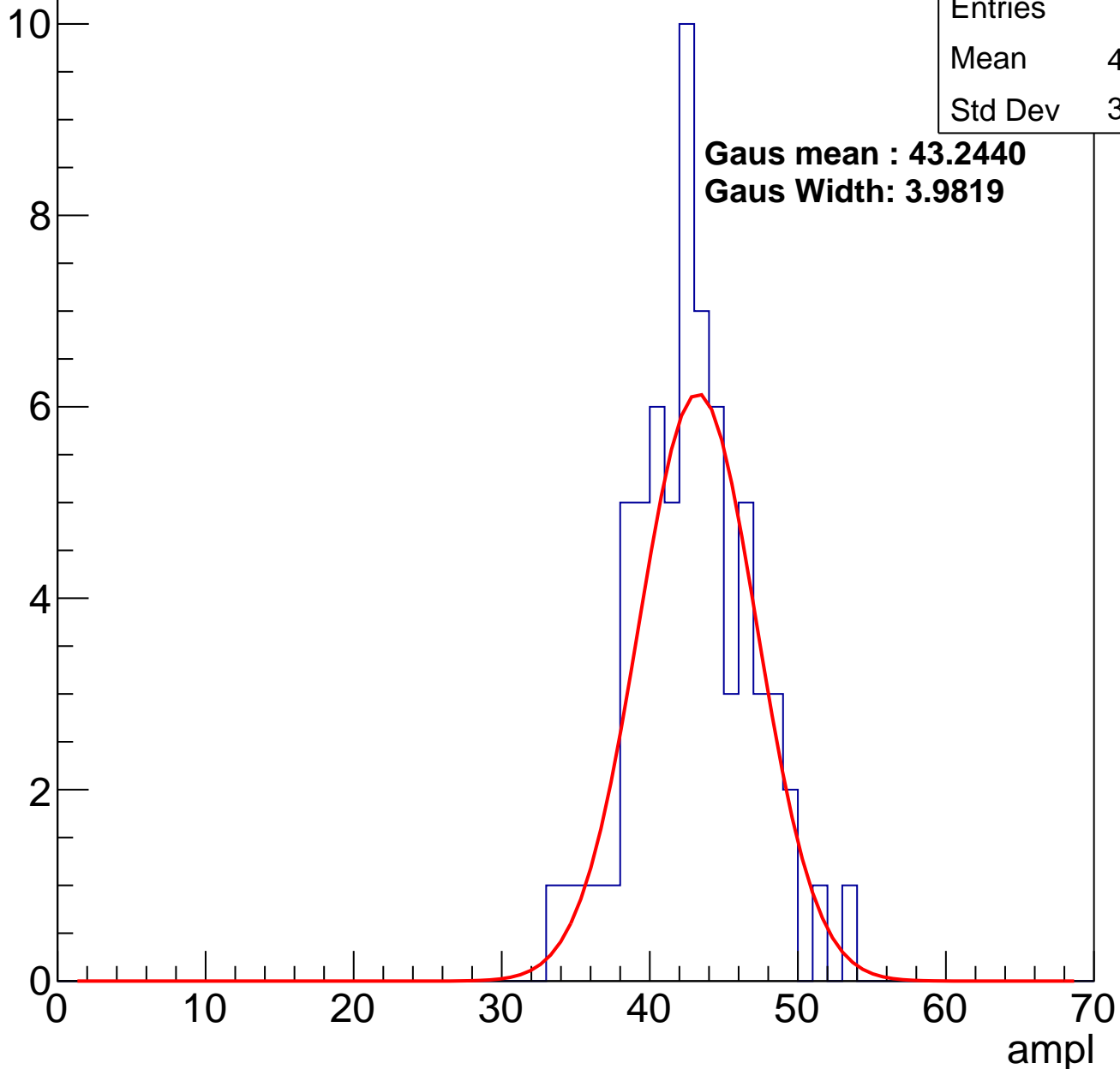
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	67
Mean	42.42
Std Dev	3.899

**Gaus mean : 43.2440**

**Gaus Width: 3.9819**

Entry

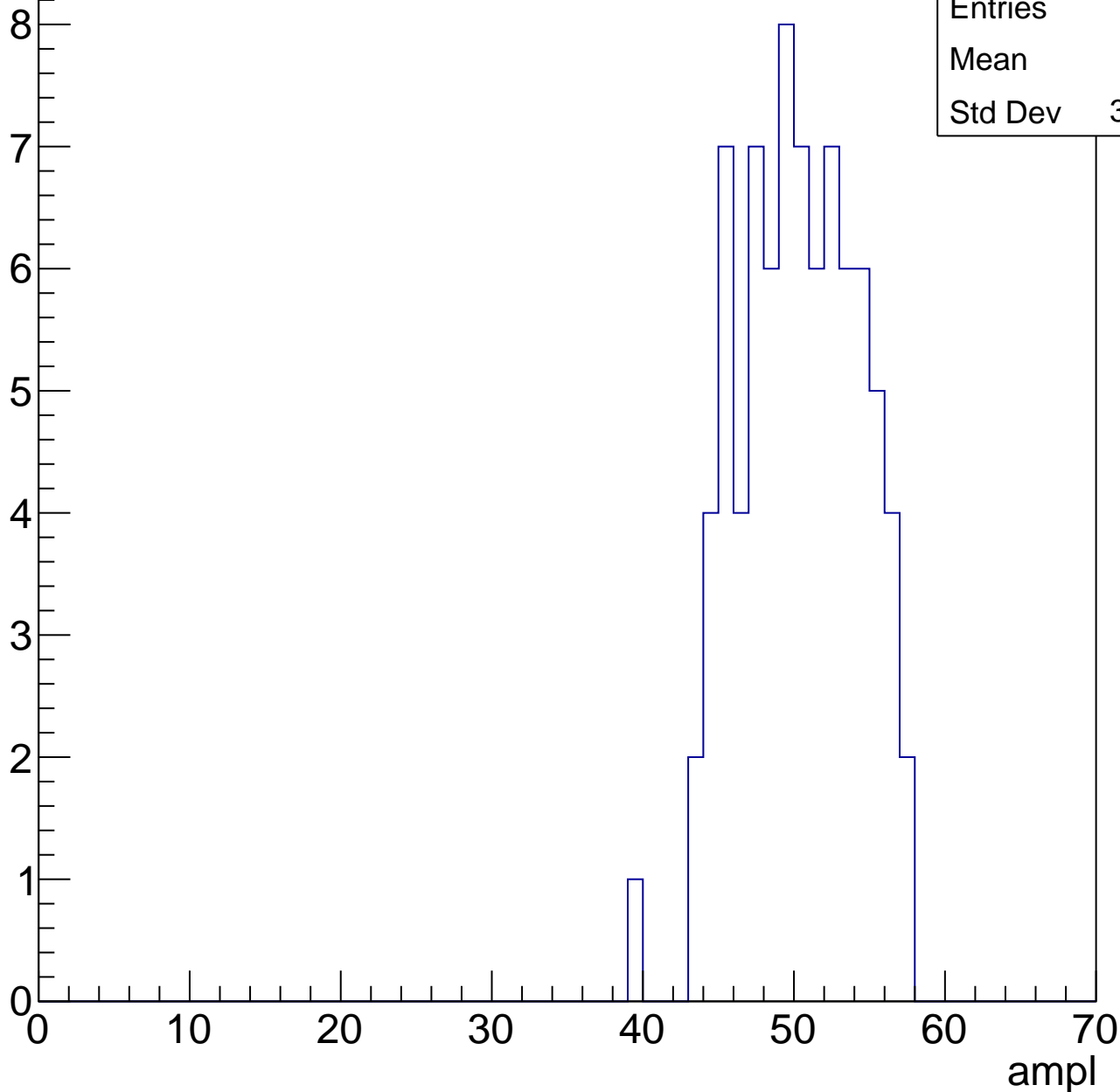


# B0L001S, U5-ch93, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	82
Mean	49.8
Std Dev	3.896

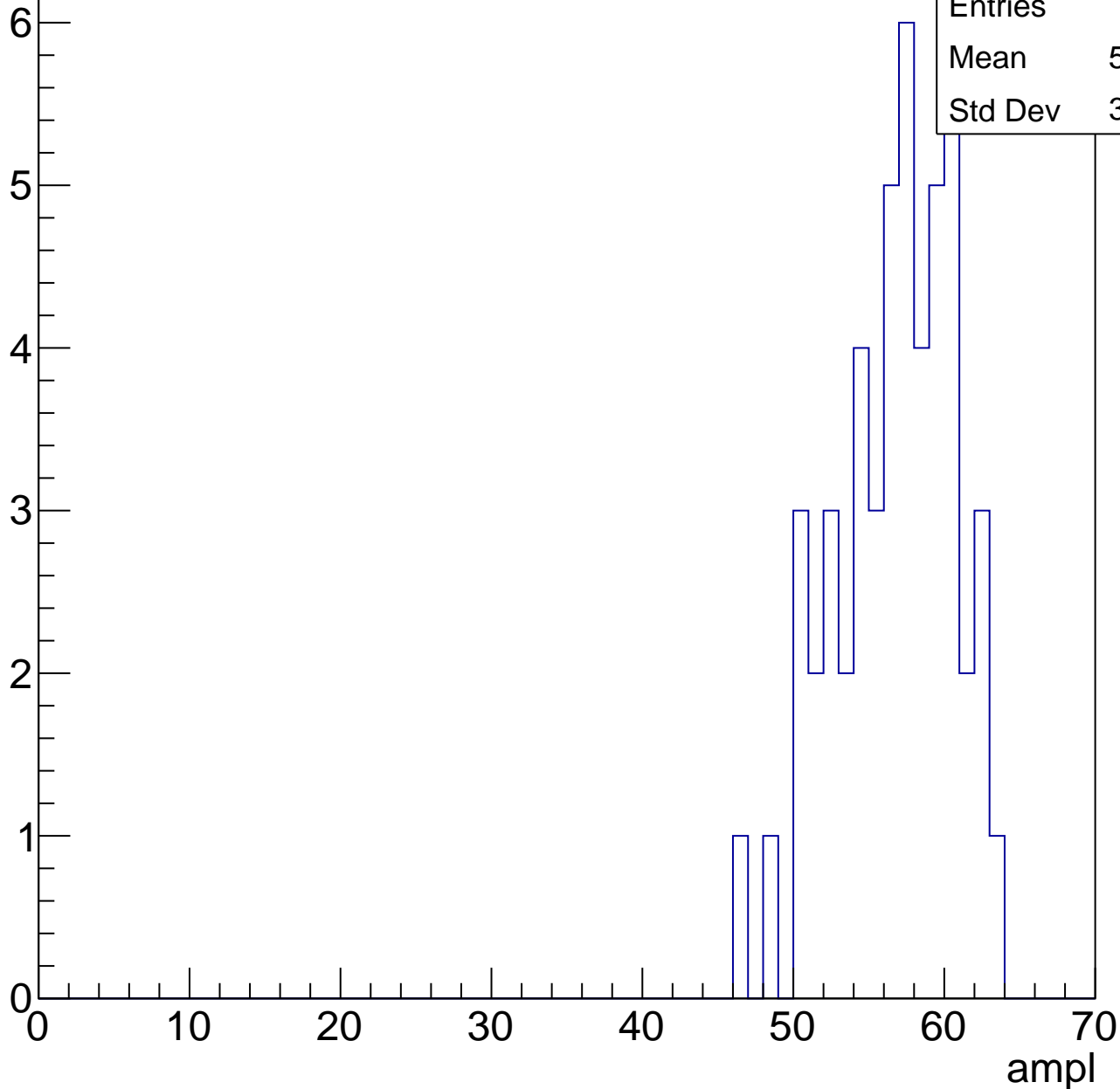


# B0L001S, U5-ch93, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	51
Mean	56.25
Std Dev	3.895

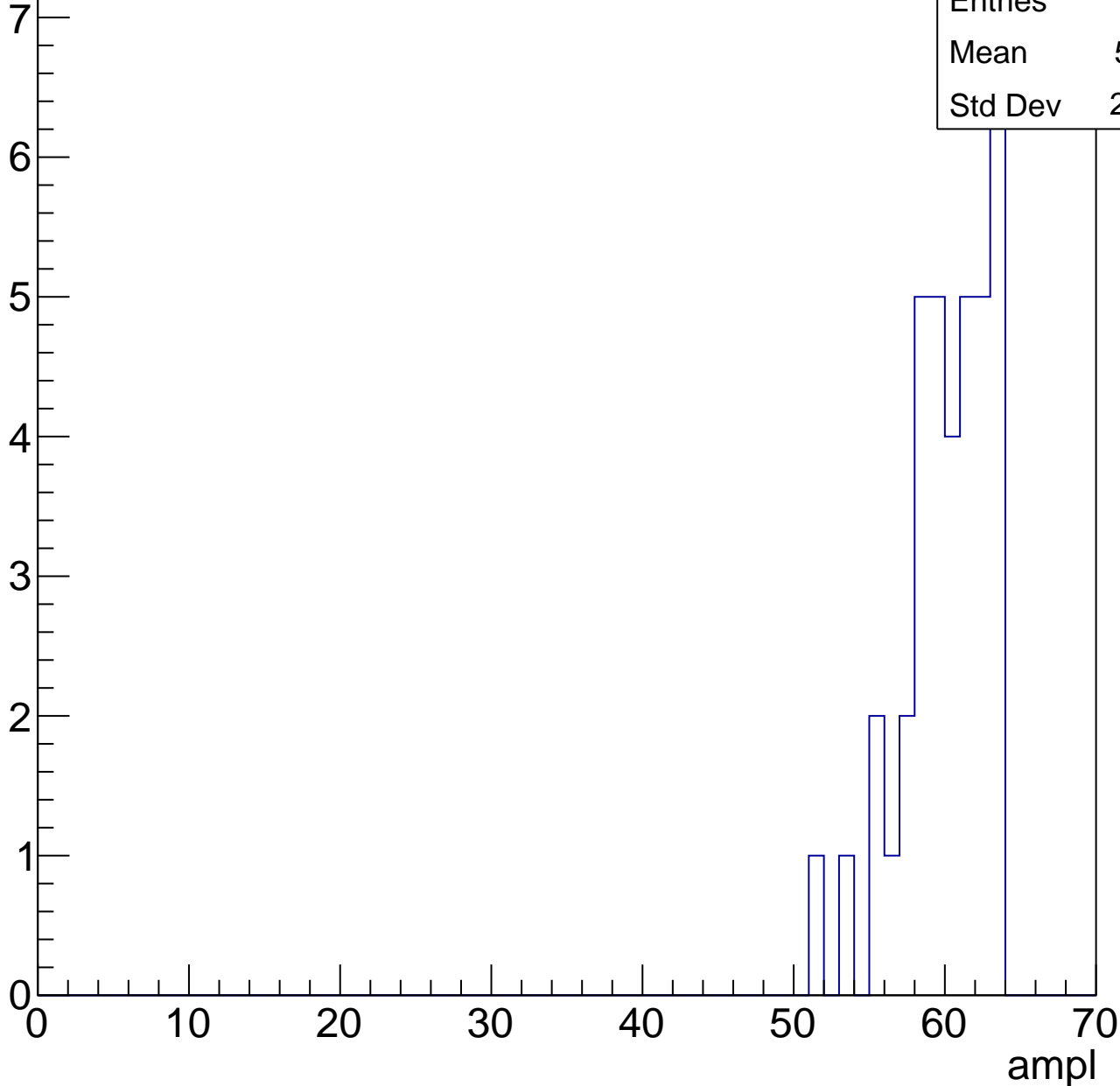


# B0L001S, U5-ch93, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

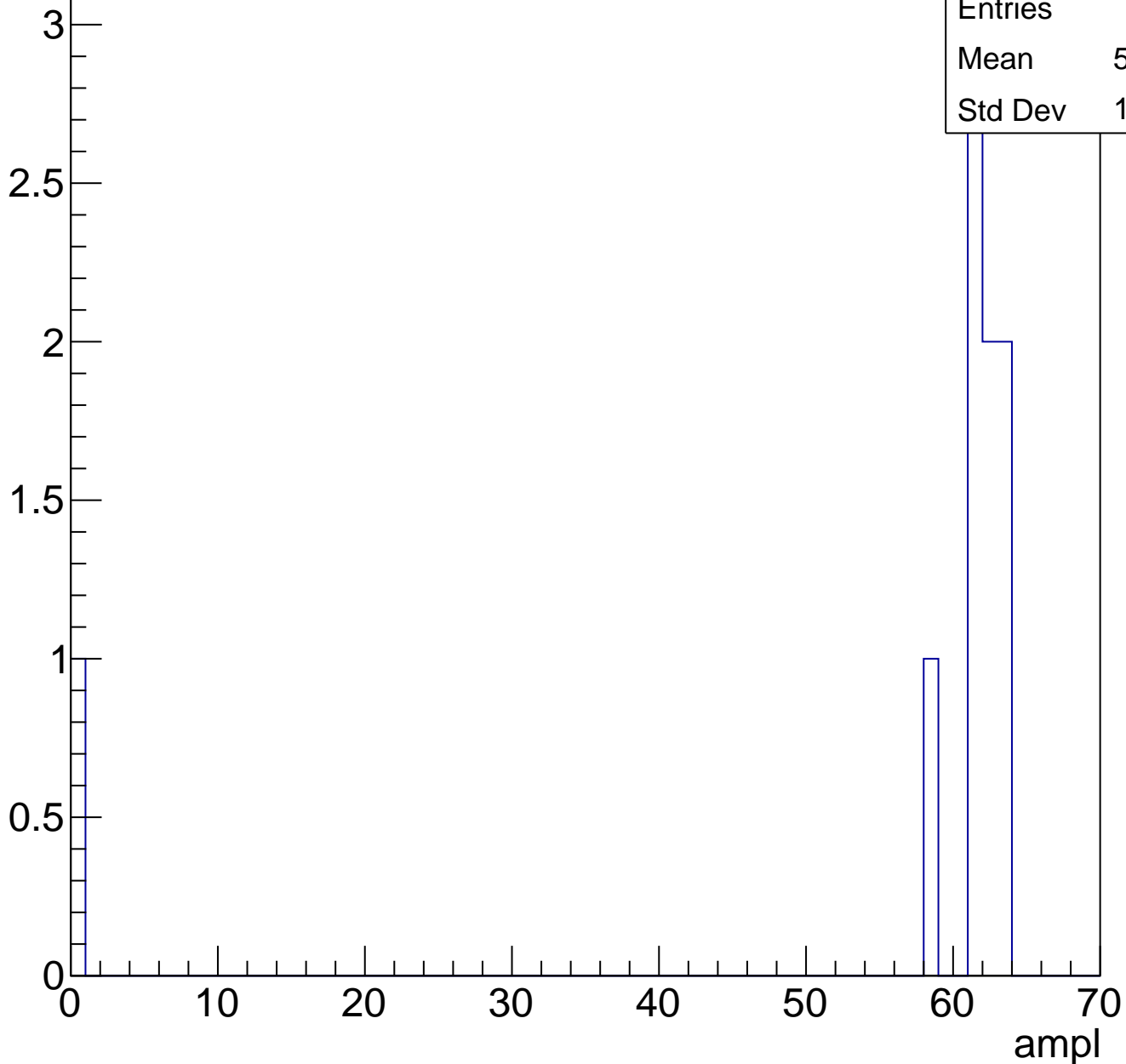
Entries	38
Mean	59.61
Std Dev	2.907



# B0L001S, U5-ch93, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch93, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L001S, U5-ch94, adc0

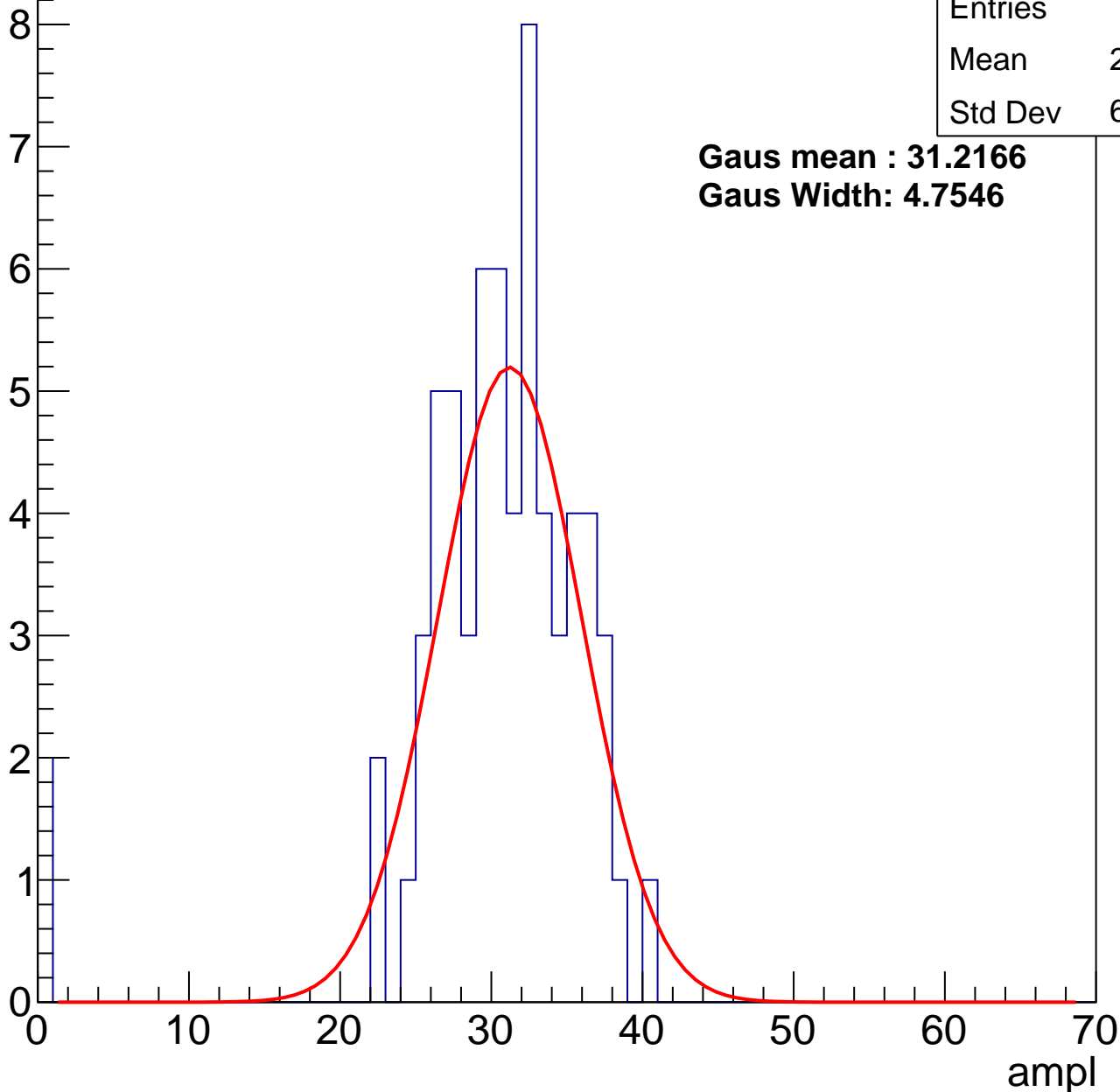
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	29.74
Std Dev	6.625

**Gaus mean : 31.2166**

**Gaus Width: 4.7546**



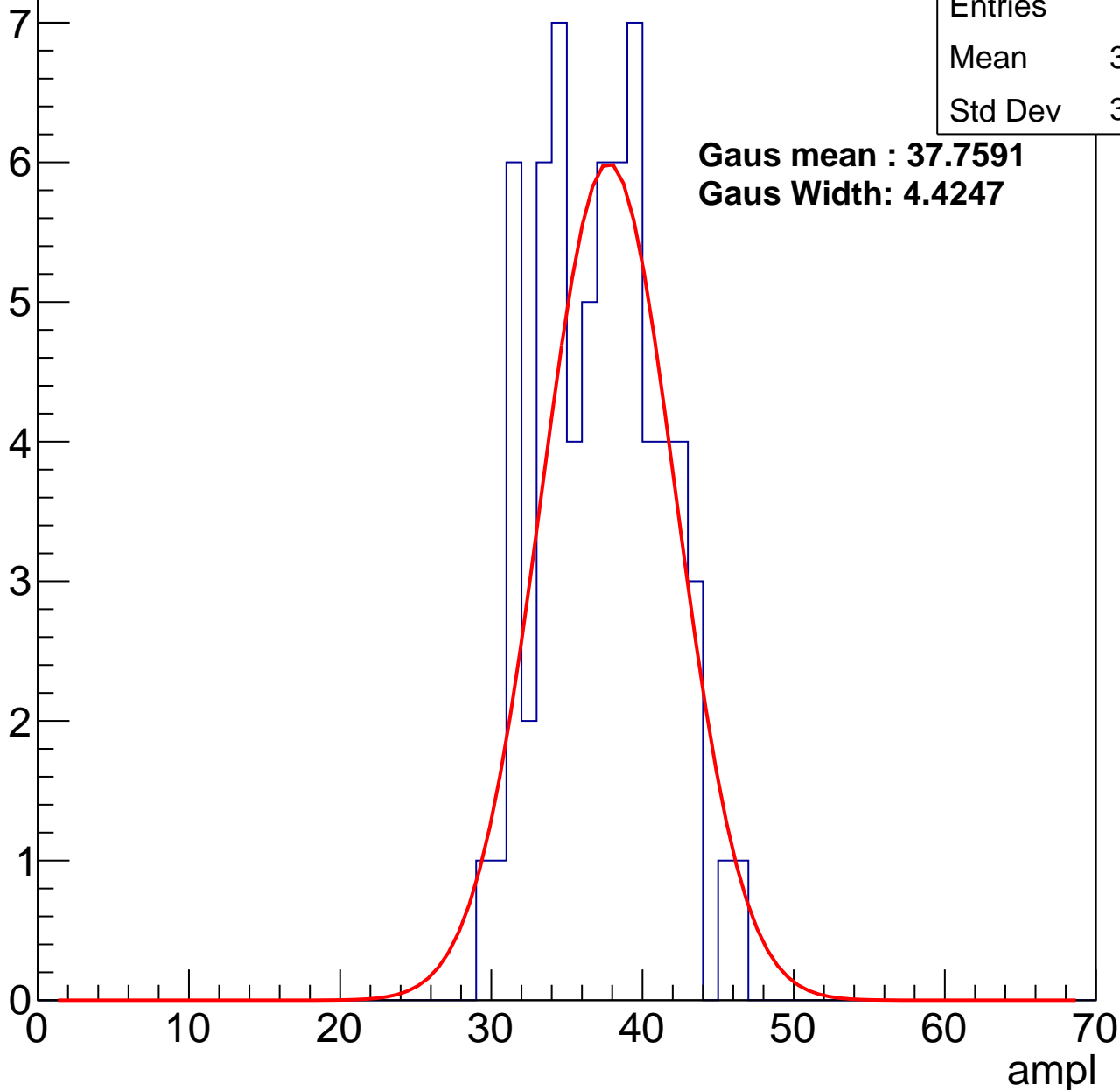
# B0L001S, U5-ch94, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	36.76
Std Dev	3.915

**Gaus mean : 37.7591**  
**Gaus Width: 4.4247**



# B0L001S, U5-ch94, adc2

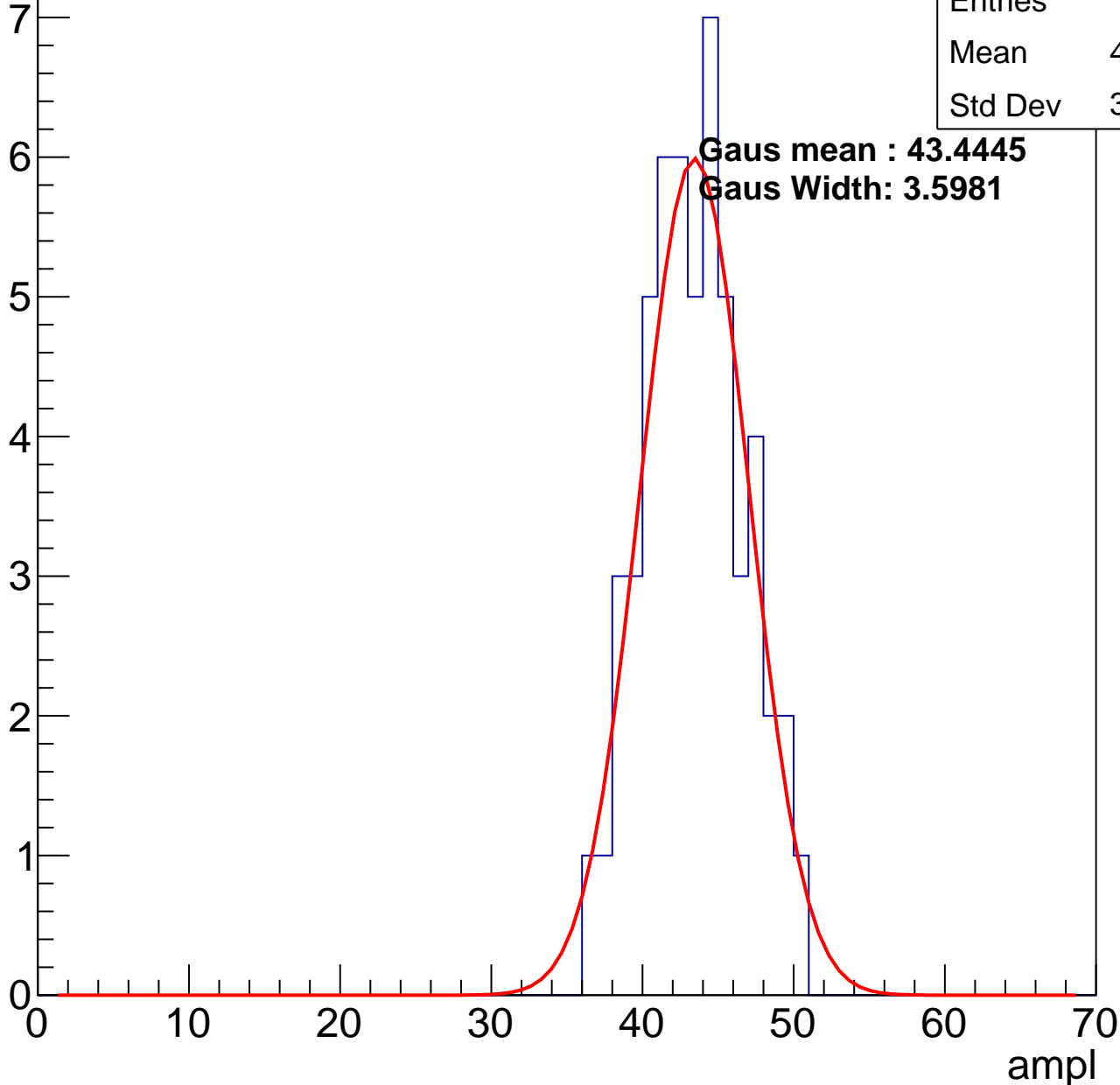
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	42.96
Std Dev	3.254

**Gaus mean : 43.4445**

**Gaus Width: 3.5981**

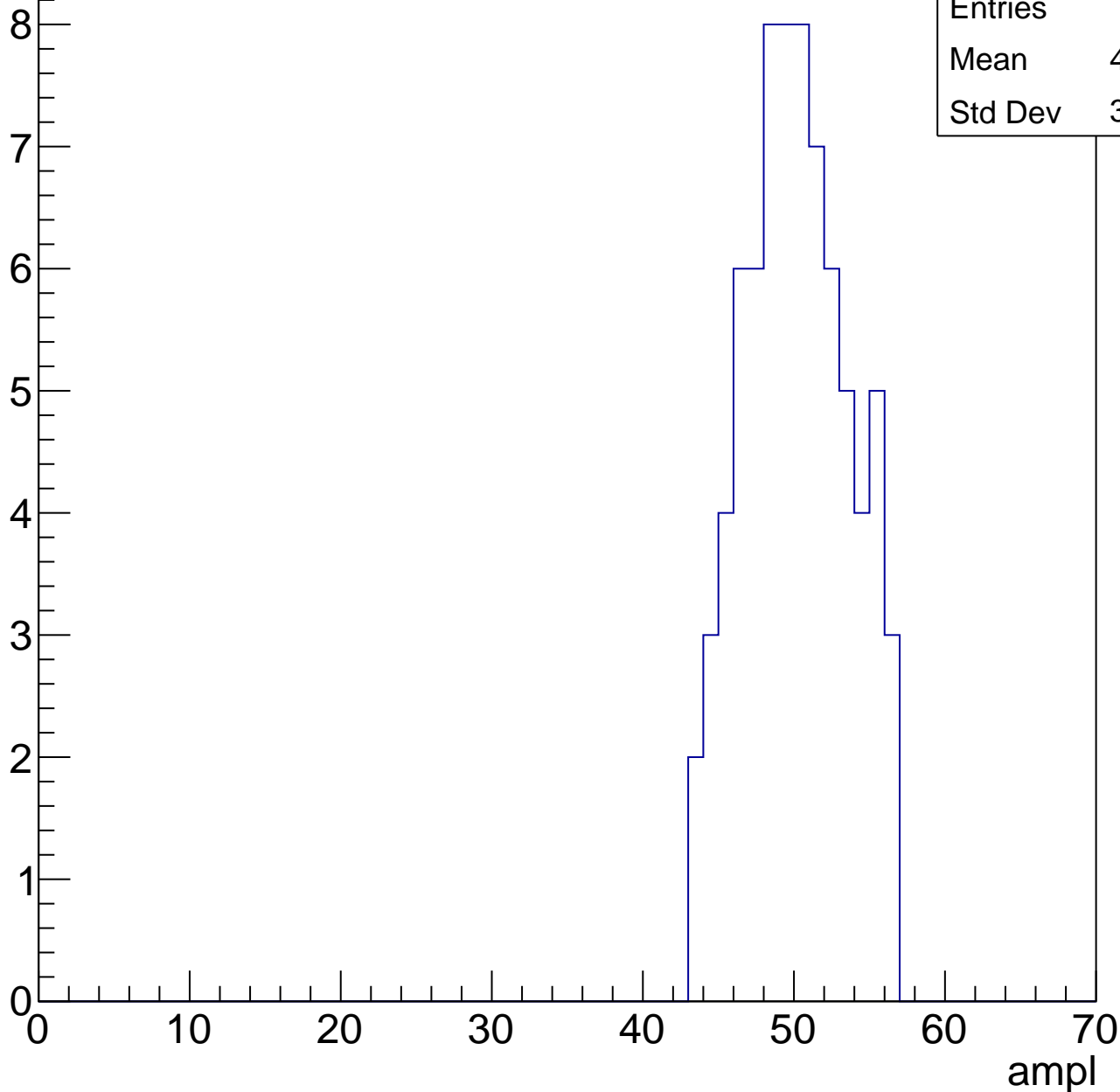


# B0L001S, U5-ch94, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	75
Mean	49.67
Std Dev	3.388

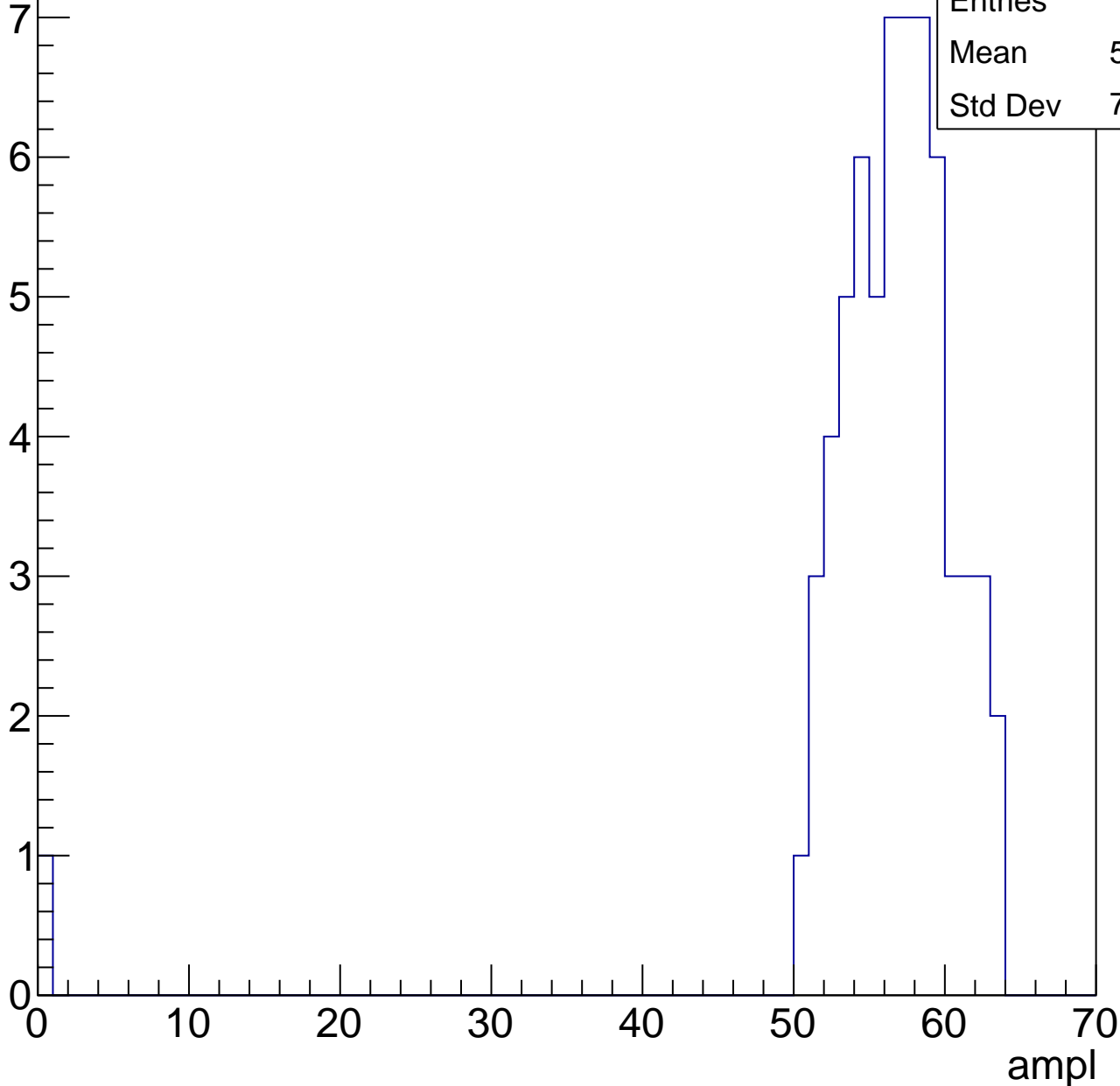


# B0L001S, U5-ch94, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	55.57
Std Dev	7.758



# B0L001S, U5-ch94, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

6

5

4

3

2

1

0

Entries	31
Mean	60.52
Std Dev	1.949

ampl

0

10

20

30

40

50

60

70

# B0L001S, U5-ch94, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries

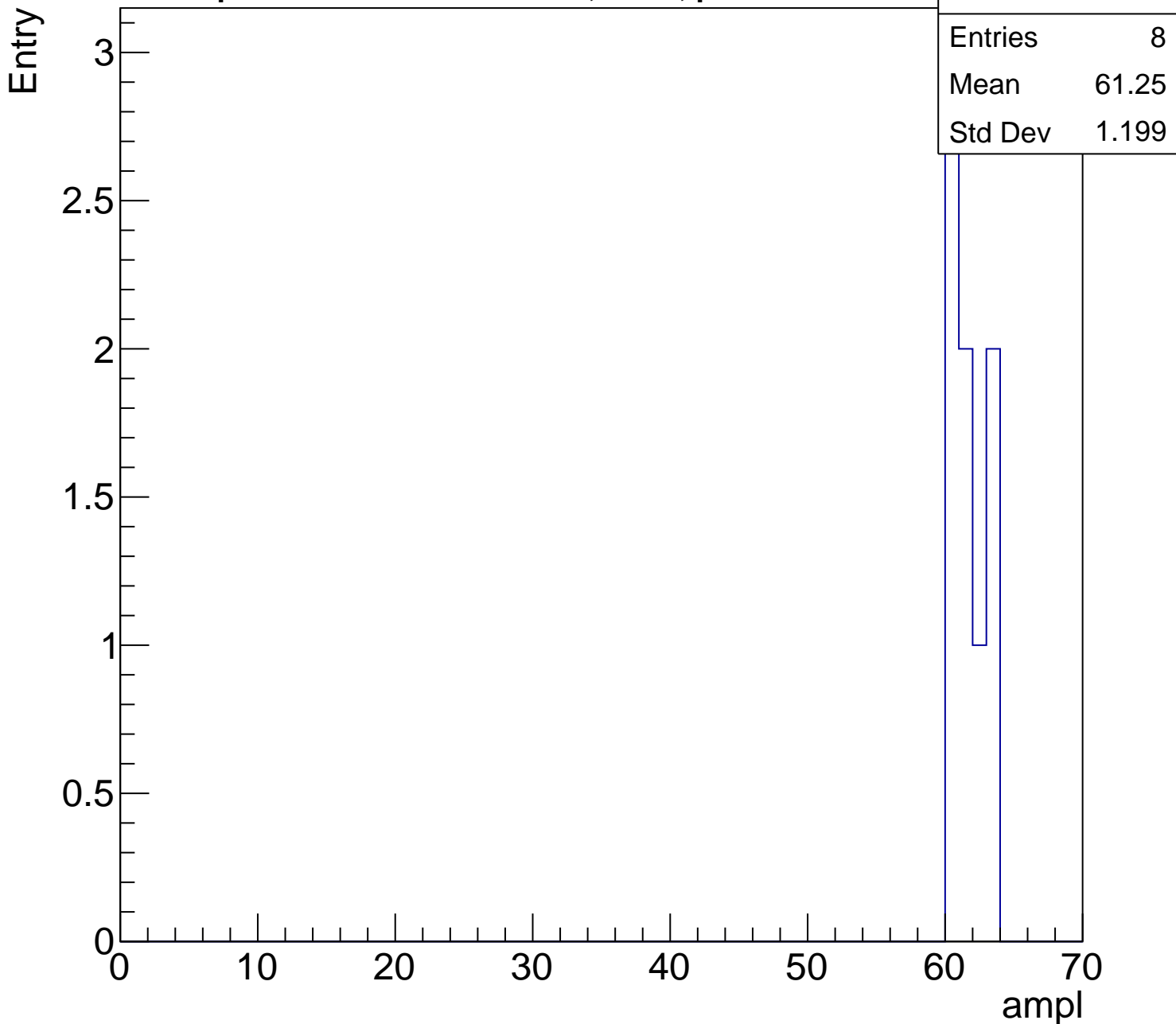
8

Mean

61.25

Std Dev

1.199





# B0L001S, U5-ch94, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U5-ch95, adc0

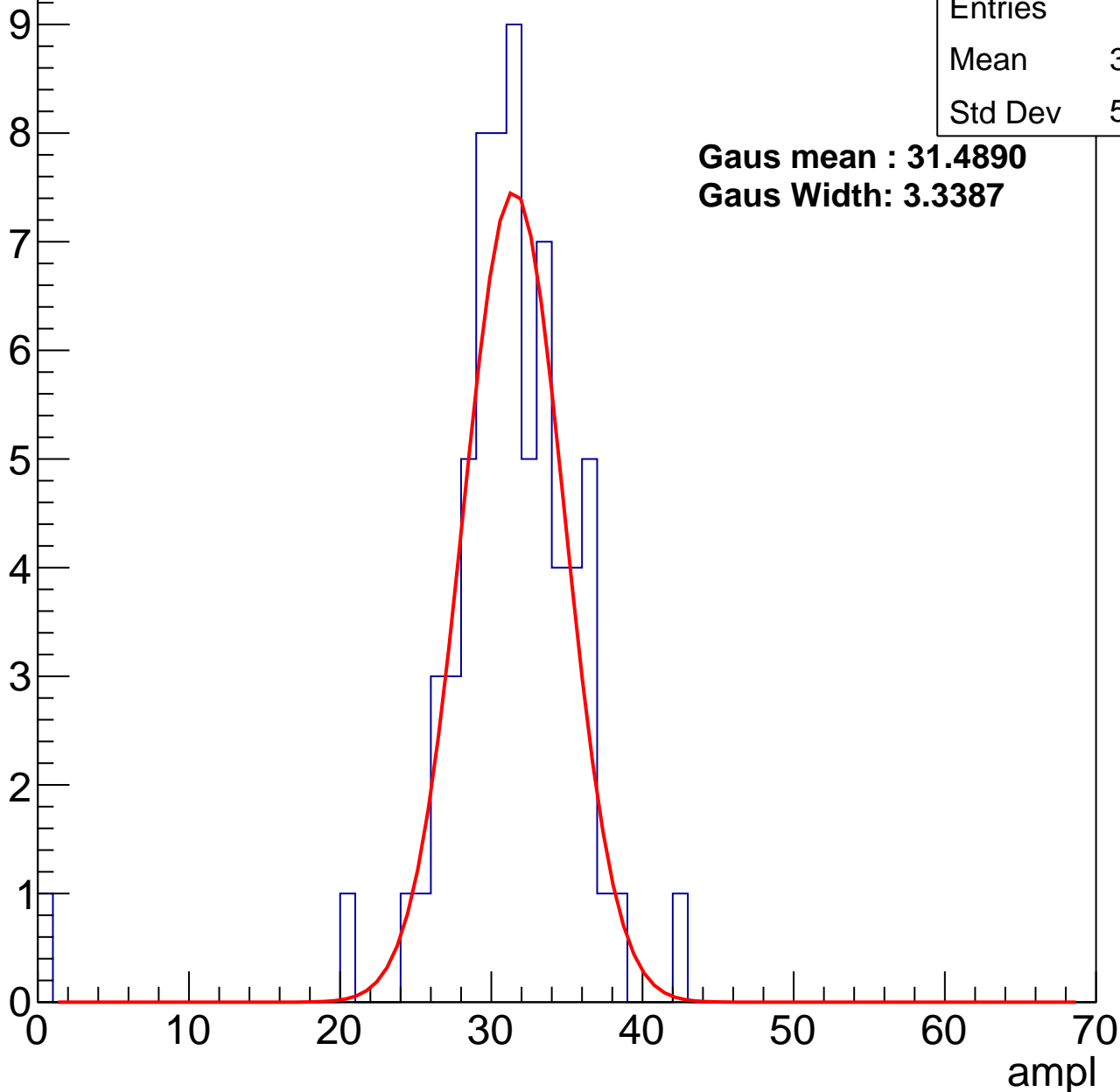
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	30.63
Std Dev	5.187

**Gaus mean : 31.4890**

**Gaus Width: 3.3387**



# B0L001S, U5-ch95, adc1

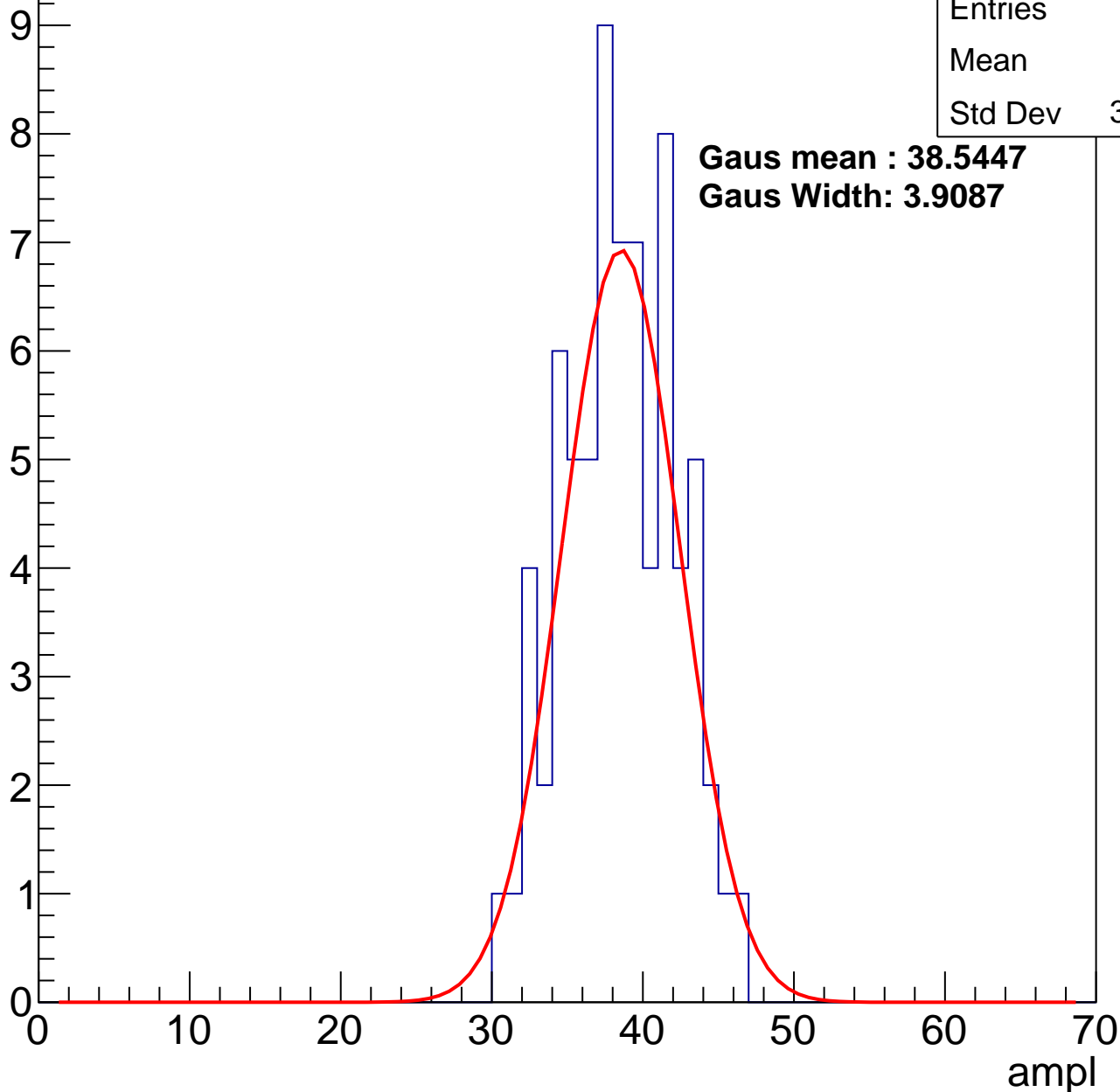
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	38
Std Dev	3.625

**Gaus mean : 38.5447**

**Gaus Width: 3.9087**



# B0L001S, U5-ch95, adc2

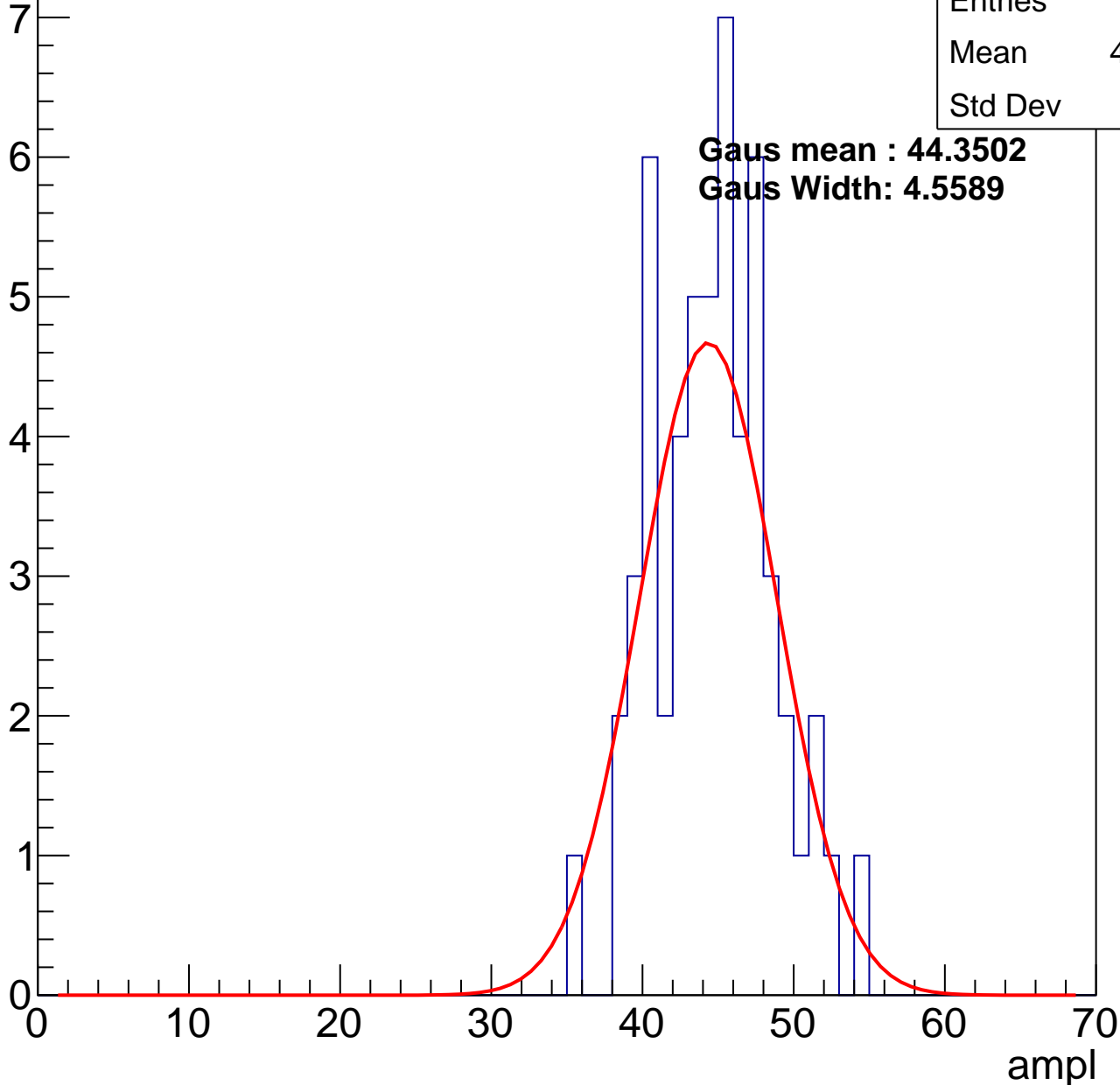
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	44.25
Std Dev	3.89

**Gaus mean : 44.3502**

**Gaus Width: 4.5589**

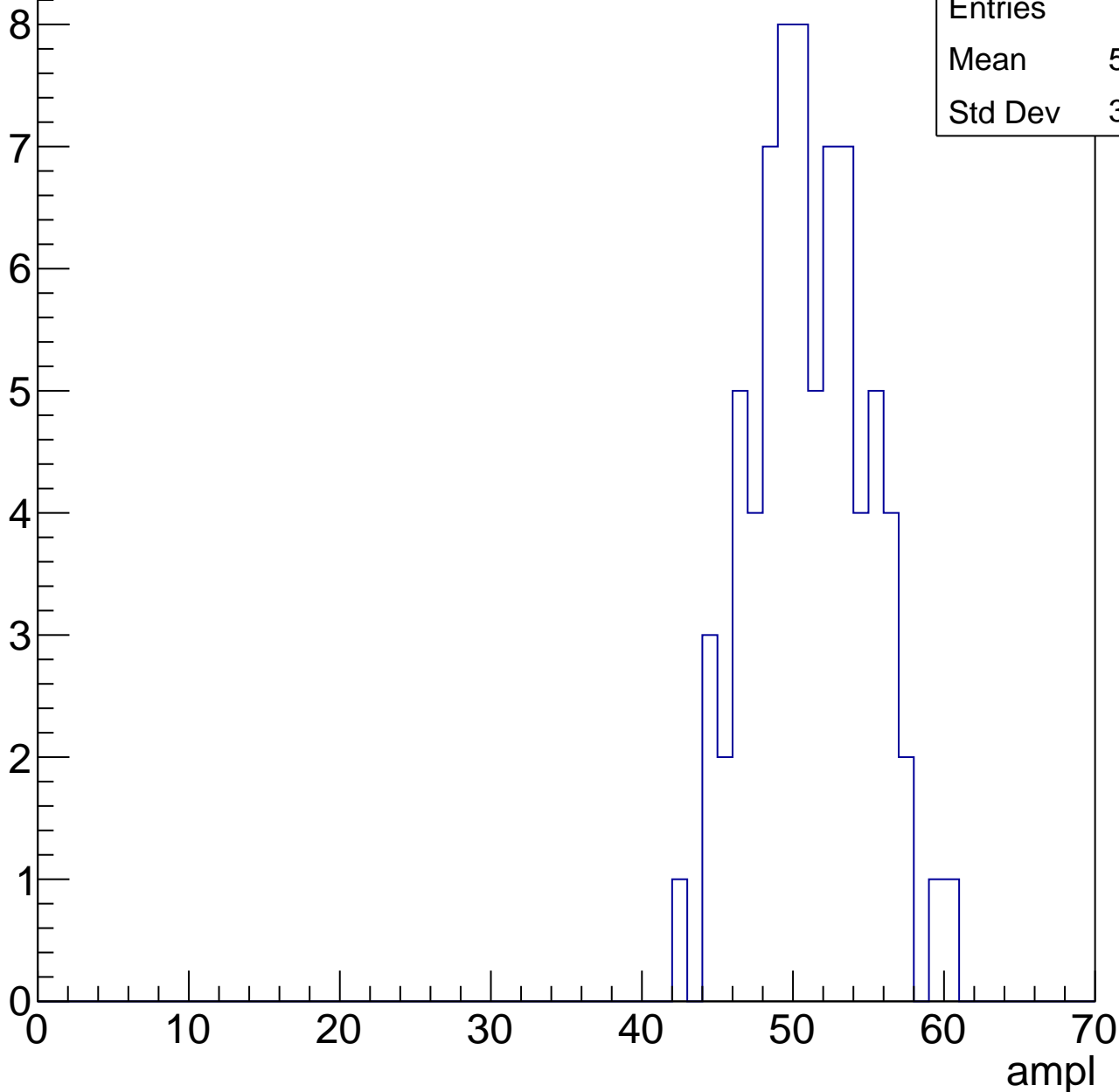


# B0L001S, U5-ch95, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	50.65
Std Dev	3.768

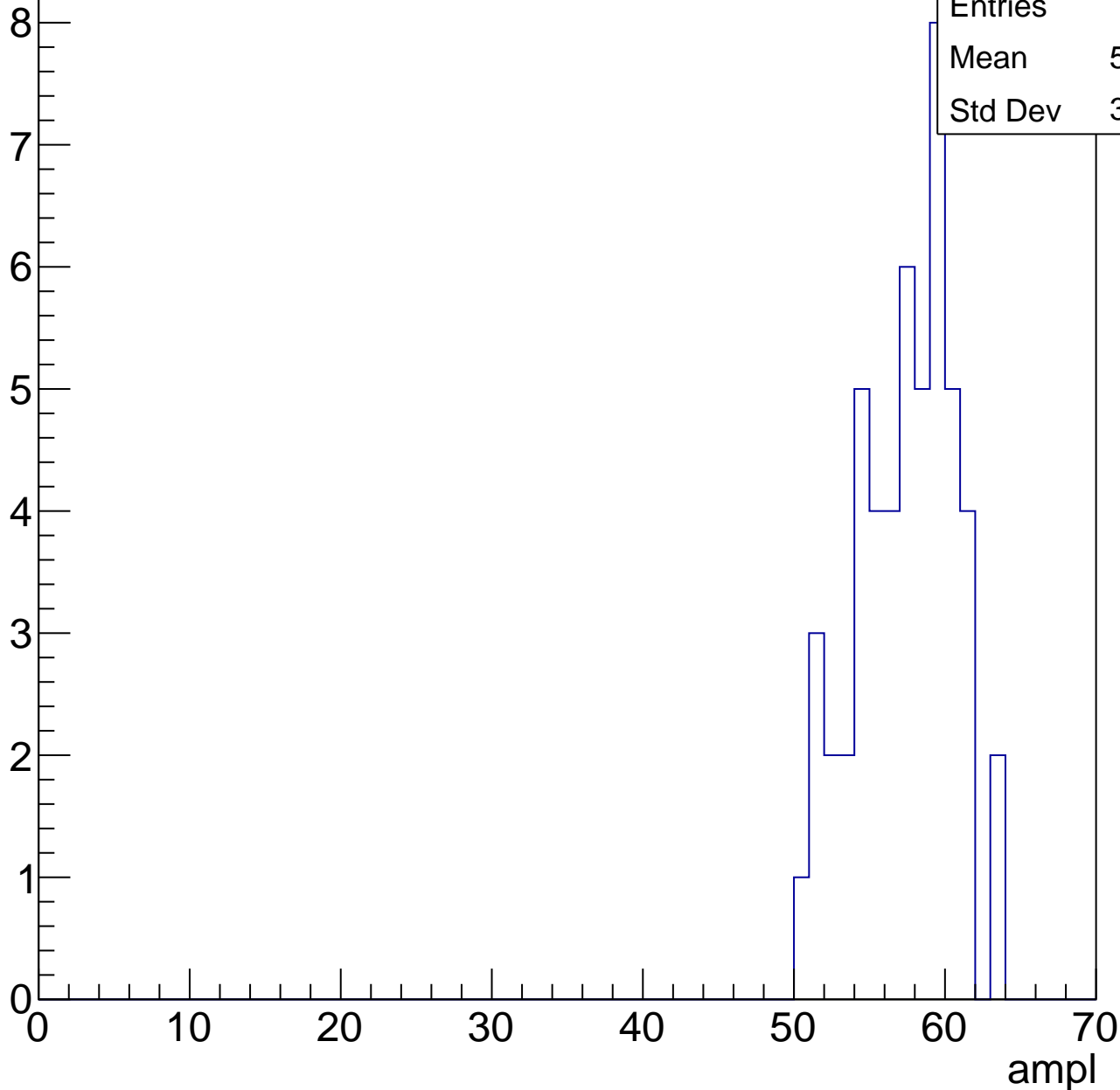


# B0L001S, U5-ch95, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	51
Mean	56.88
Std Dev	3.197

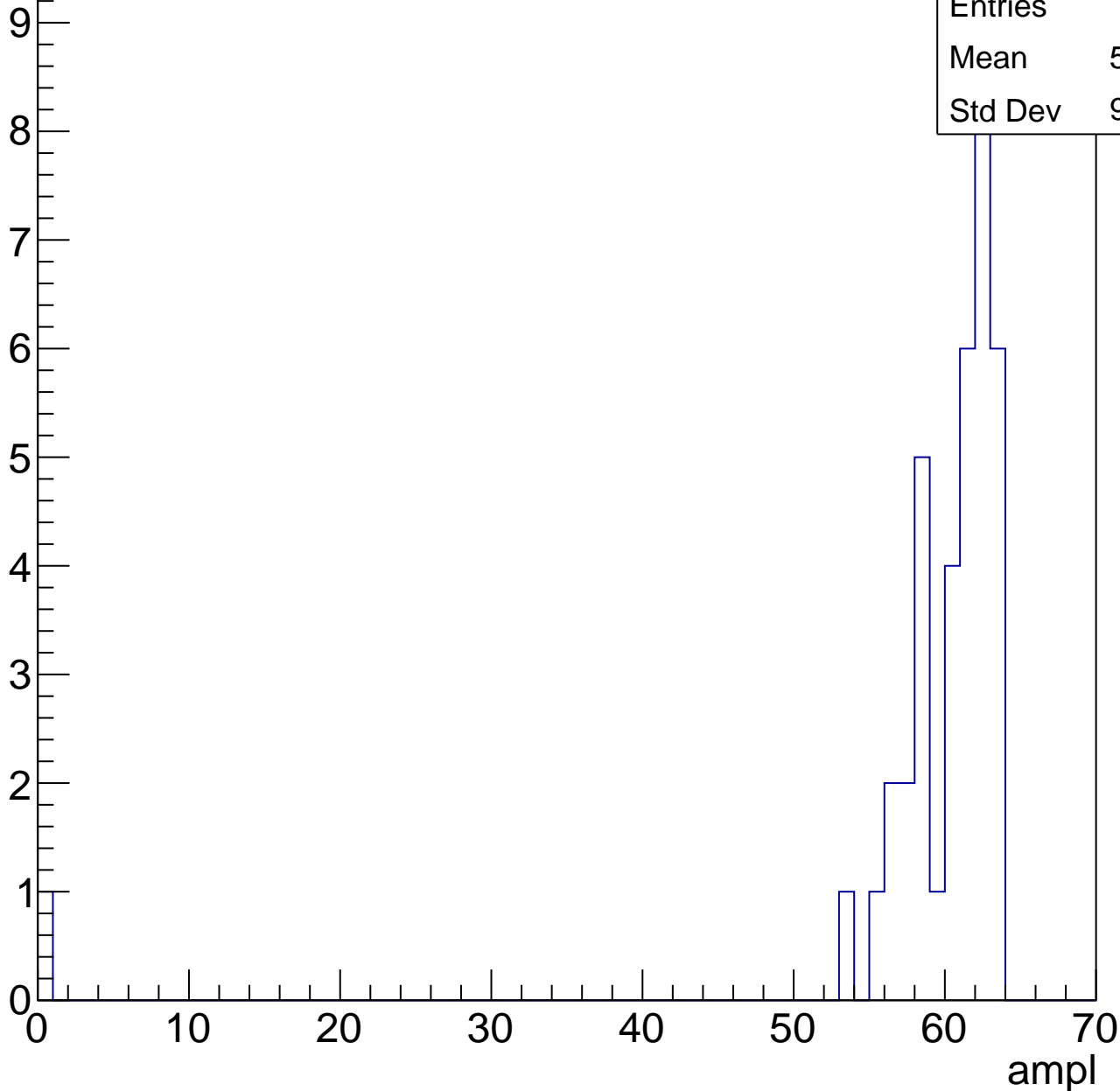


# B0L001S, U5-ch95, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	38
Mean	58.55
Std Dev	9.949



# B0L001S, U5-ch95, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch95, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U5-ch96, adc0

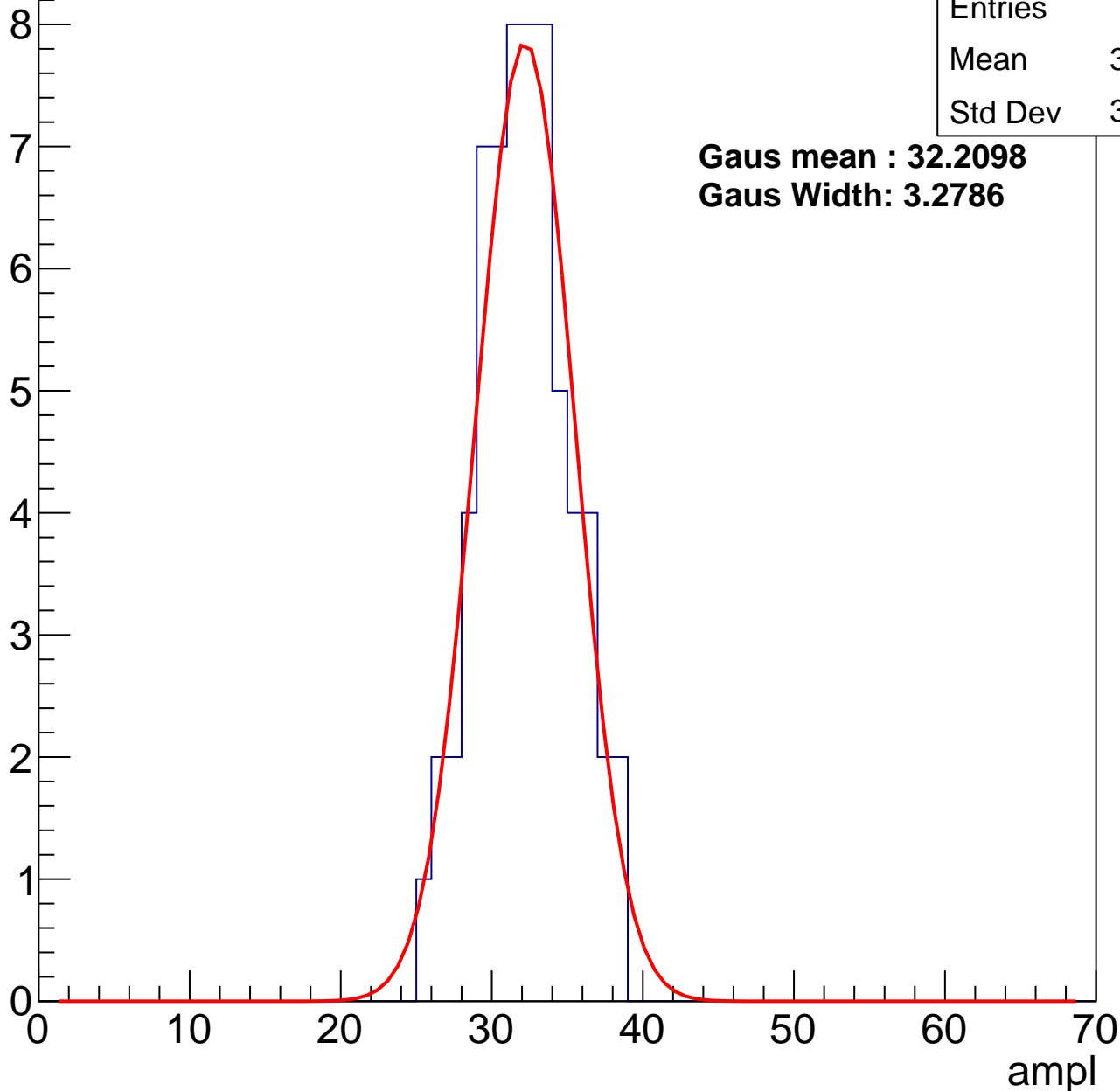
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	31.69
Std Dev	3.005

**Gaus mean : 32.2098**

**Gaus Width: 3.2786**



# B0L001S, U5-ch96, adc1

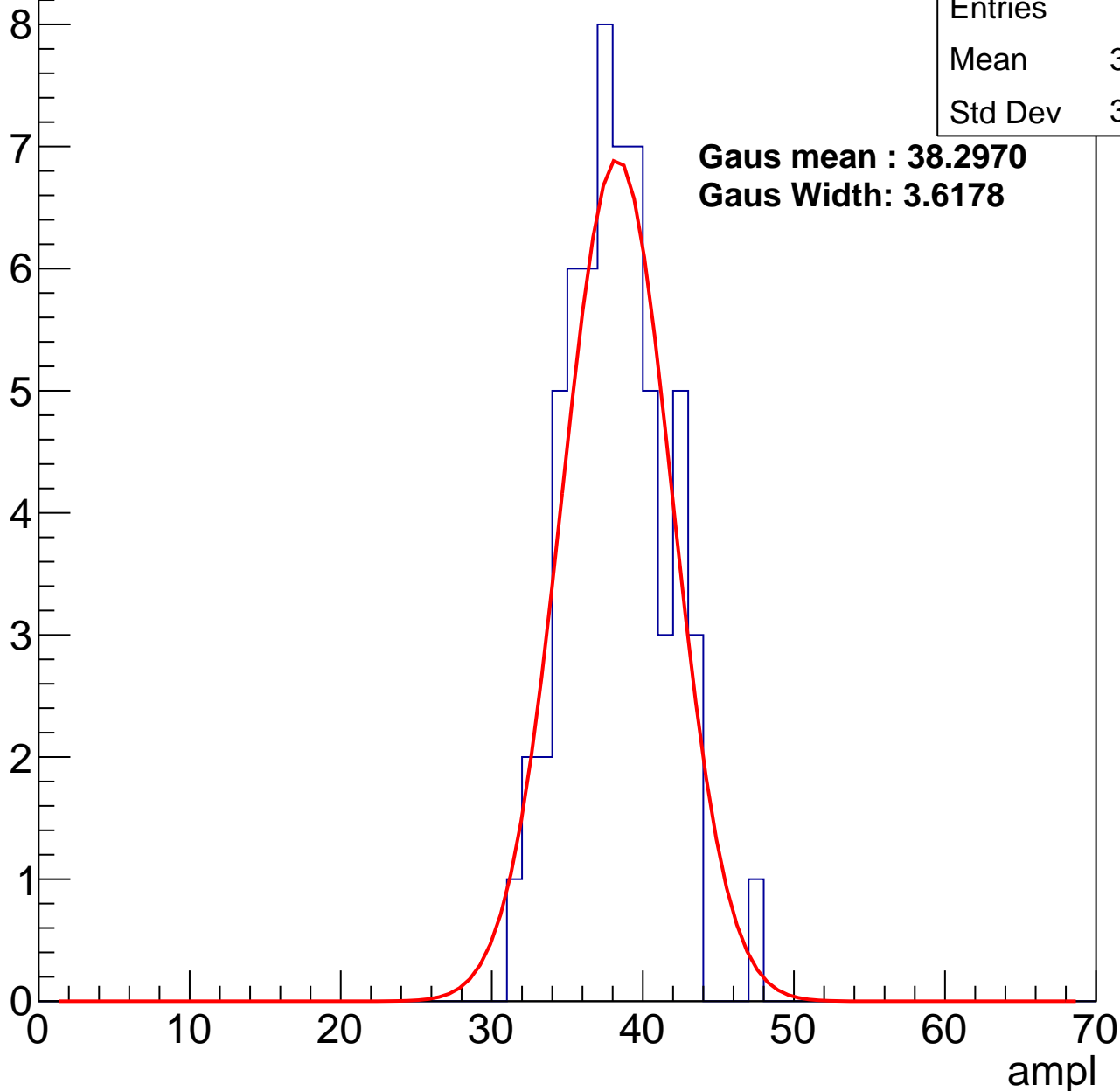
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	37.72
Std Dev	3.194

**Gaus mean : 38.2970**

**Gaus Width: 3.6178**



# B0L001S, U5-ch96, adc2

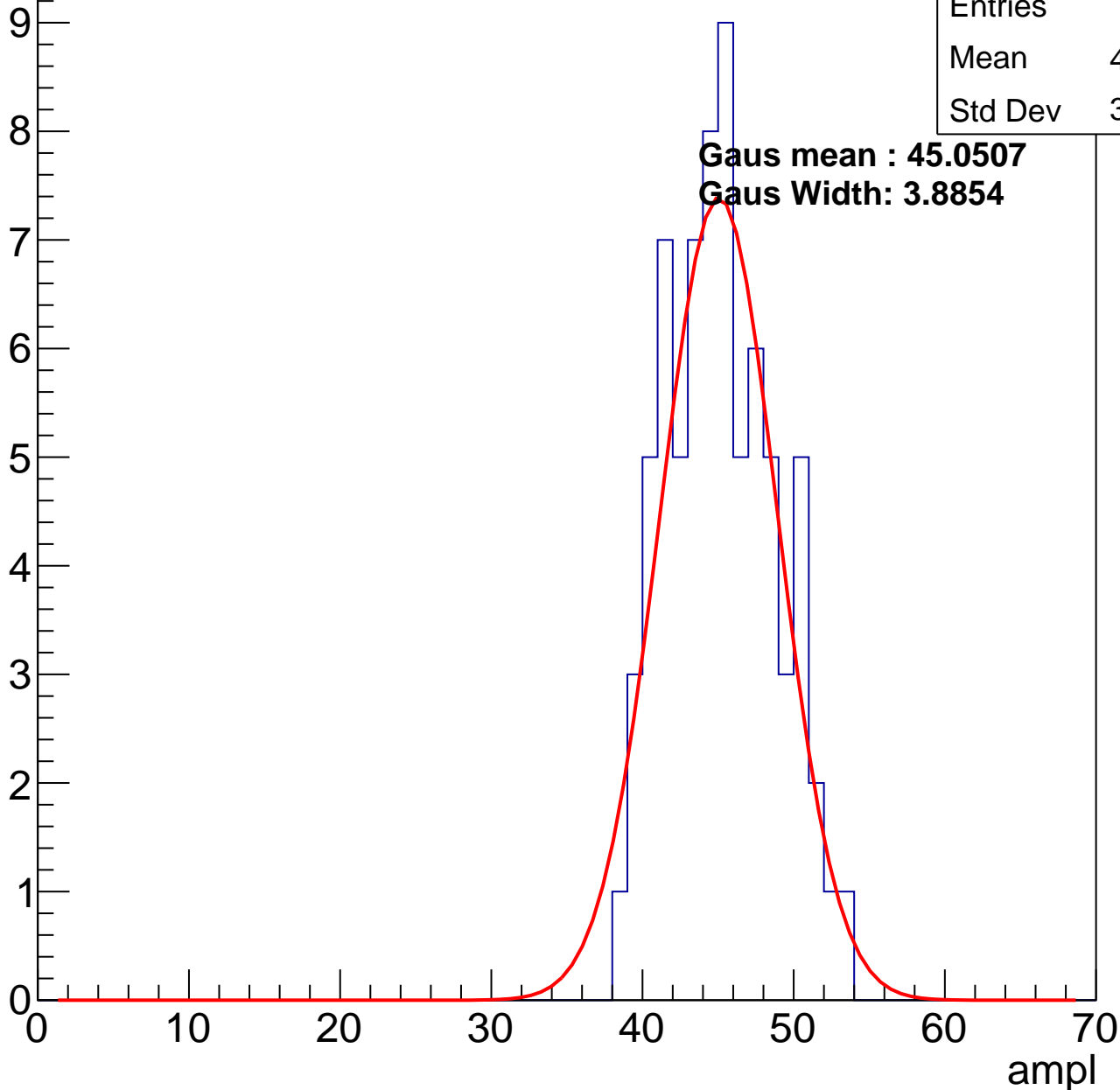
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	44.74
Std Dev	3.515

**Gaus mean : 45.0507**

**Gaus Width: 3.8854**

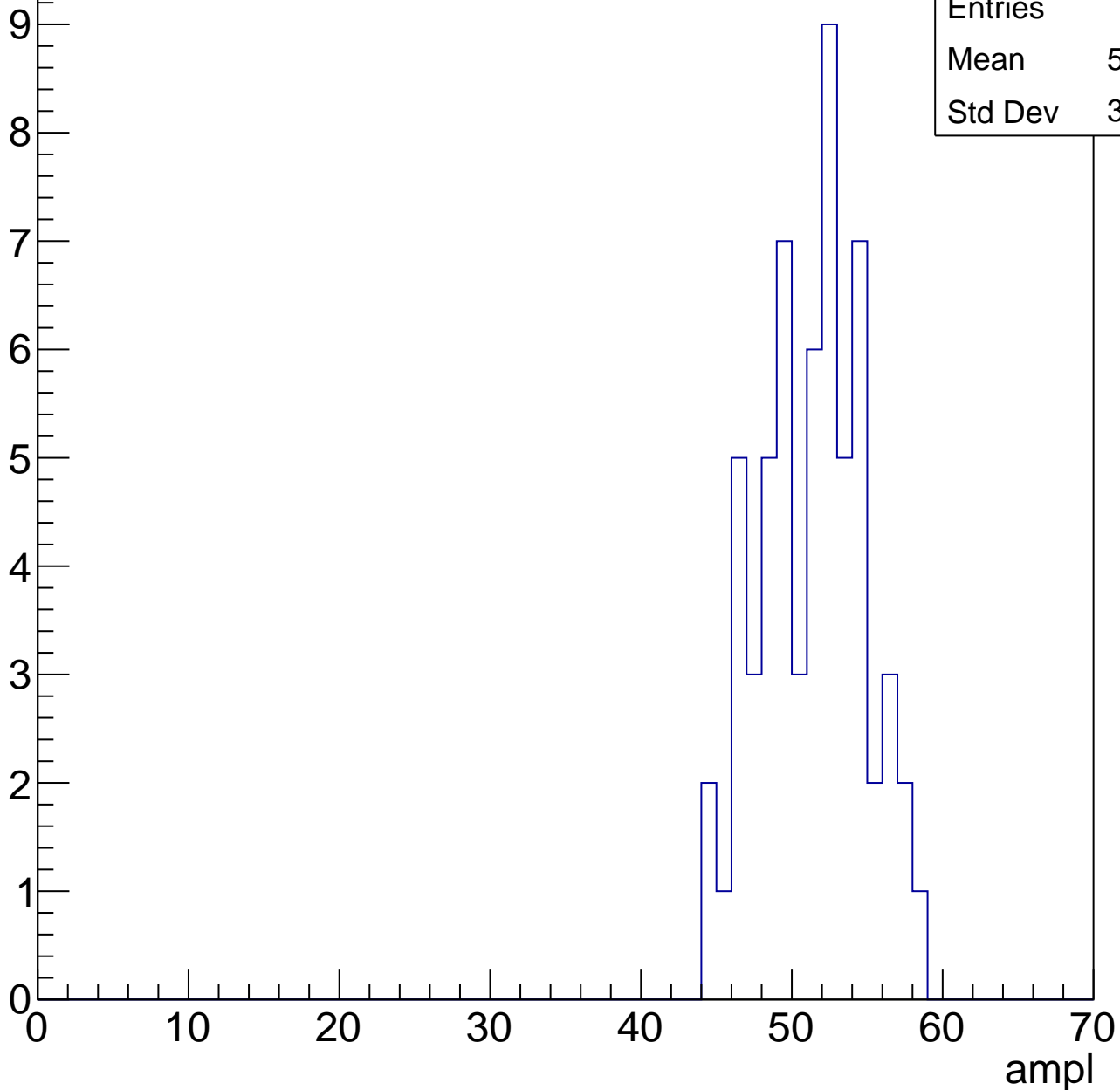


# B0L001S, U5-ch96, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

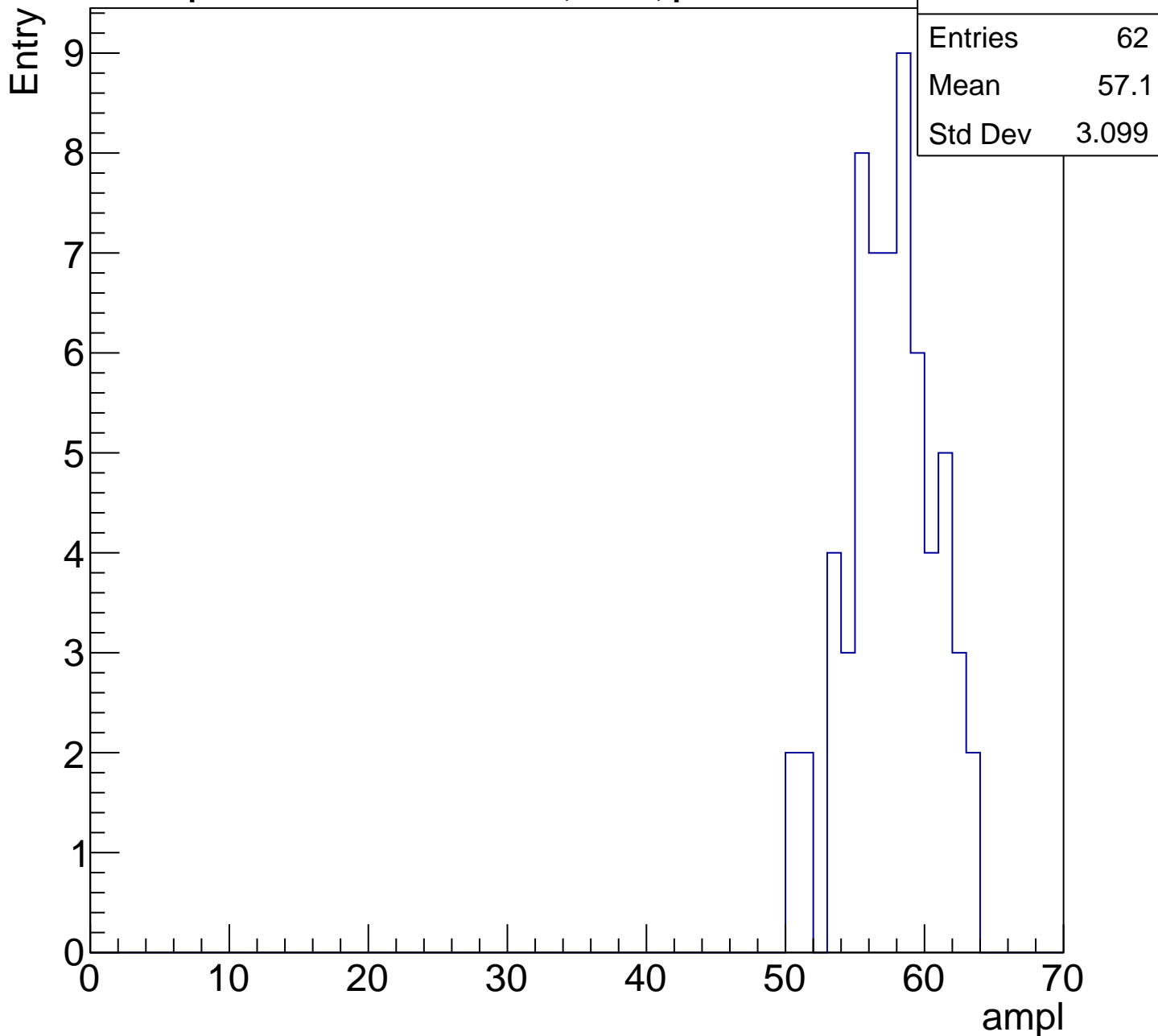
Entry

Entries	61
Mean	50.89
Std Dev	3.393



# B0L001S, U5-ch96, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

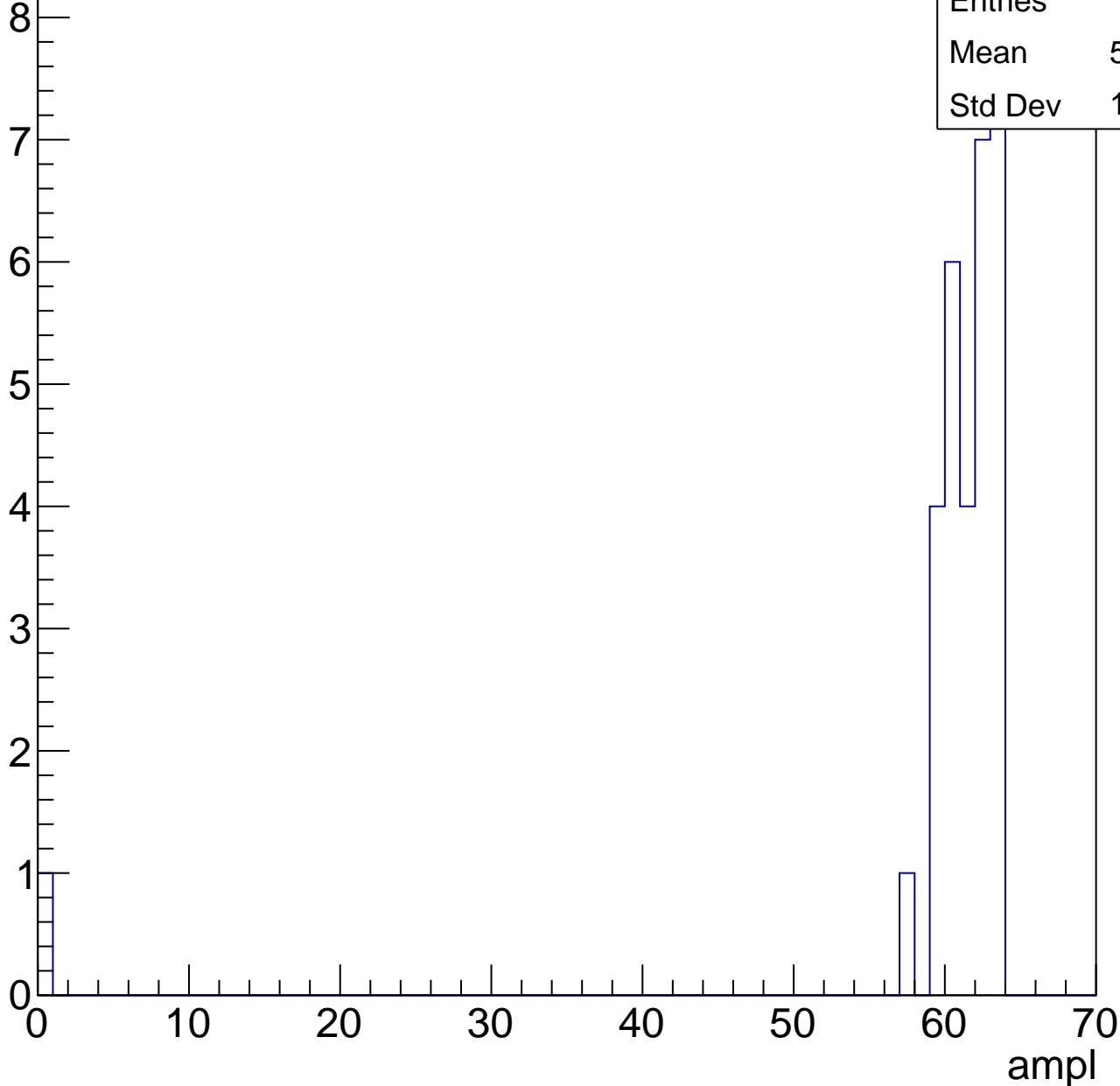


# B0L001S, U5-ch96, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	31
Mean	59.19
Std Dev	10.92



# B0L001S, U5-ch96, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch96, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U5-ch97, adc0

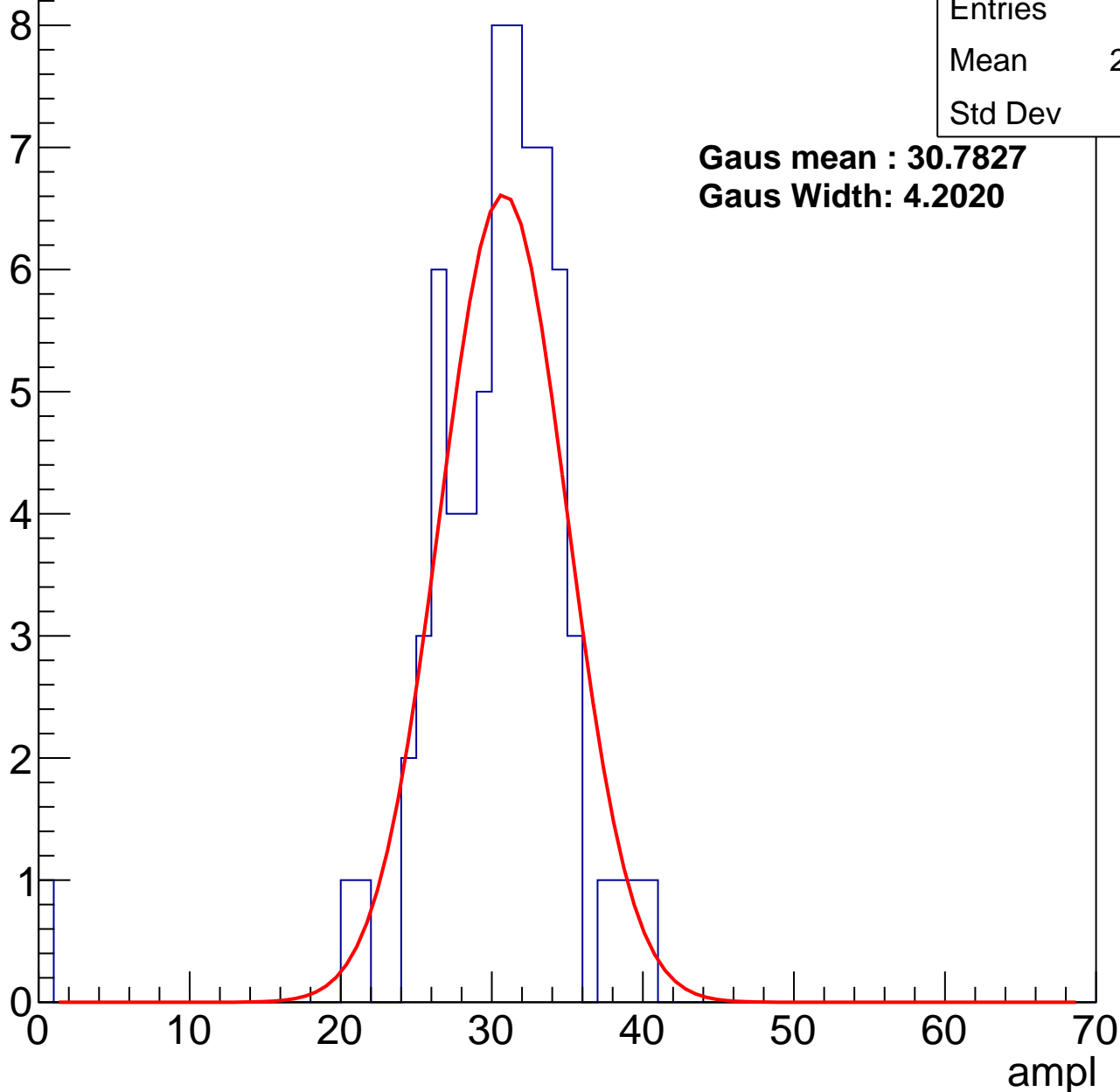
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	29.87
Std Dev	5.27

**Gaus mean : 30.7827**

**Gaus Width: 4.2020**



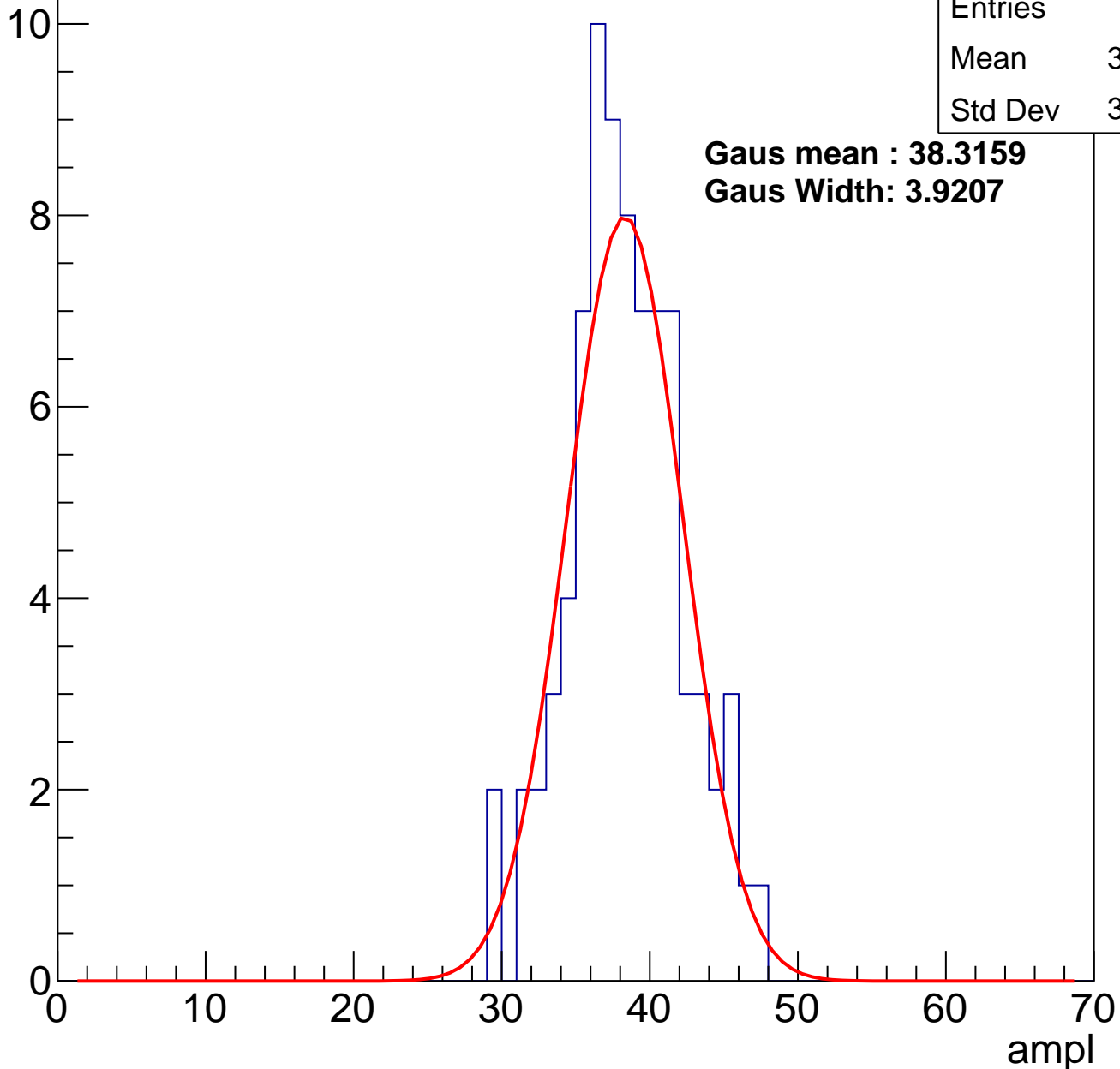
# B0L001S, U5-ch97, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	81
Mean	37.93
Std Dev	3.797

**Gaus mean : 38.3159**  
**Gaus Width: 3.9207**

Entry

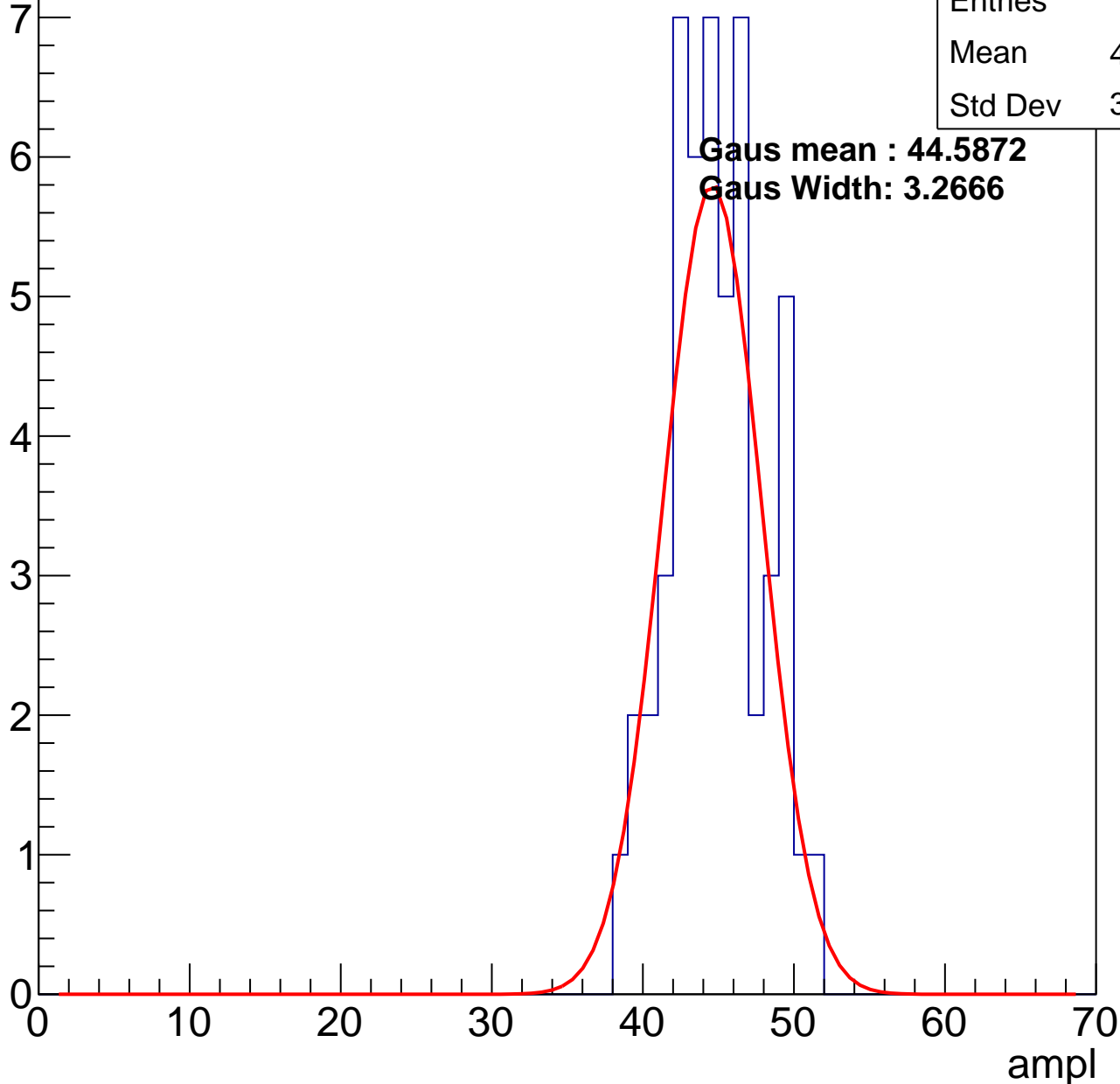


# B0L001S, U5-ch97, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	44.42
Std Dev	3.034

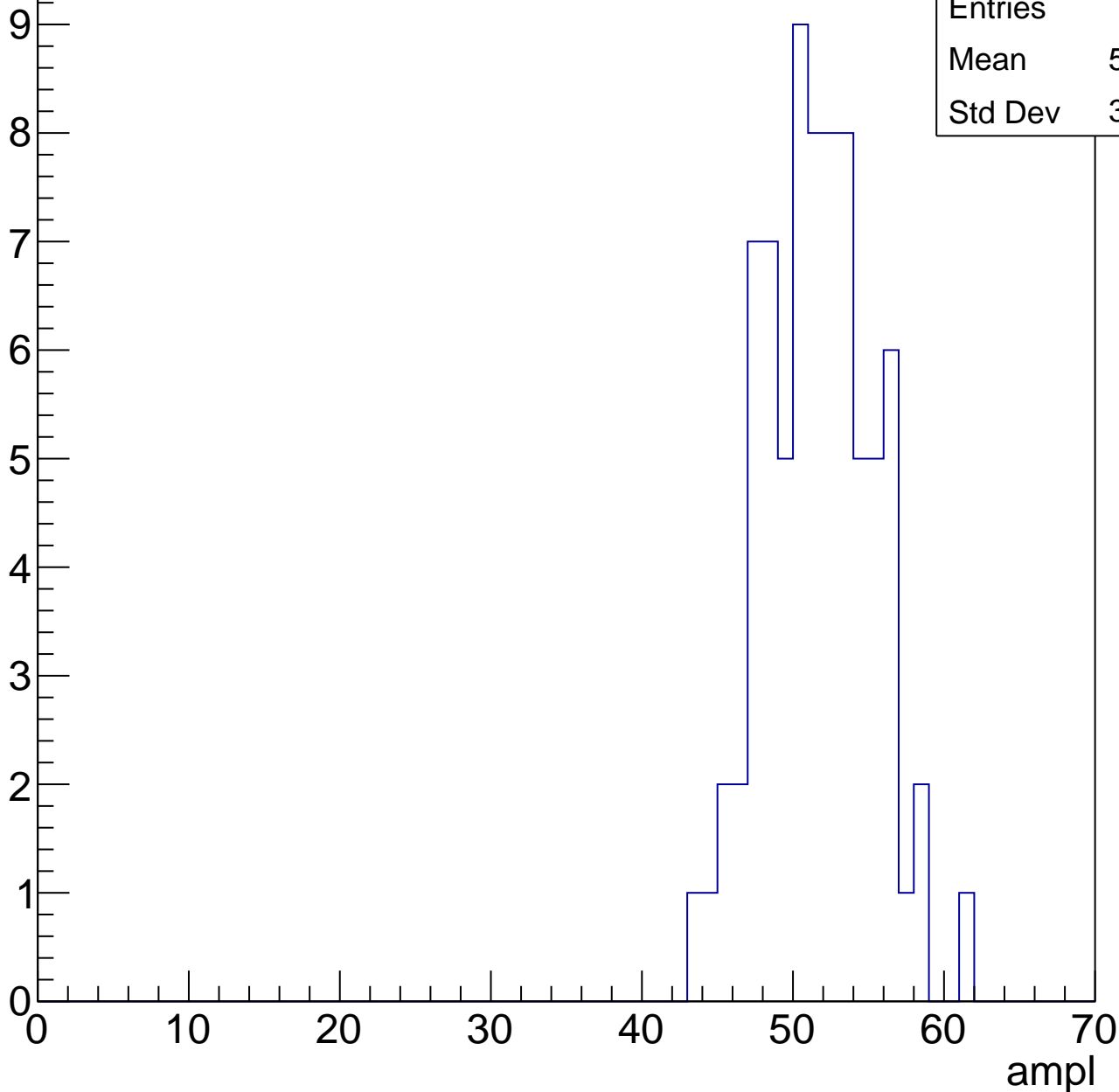


# B0L001S, U5-ch97, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

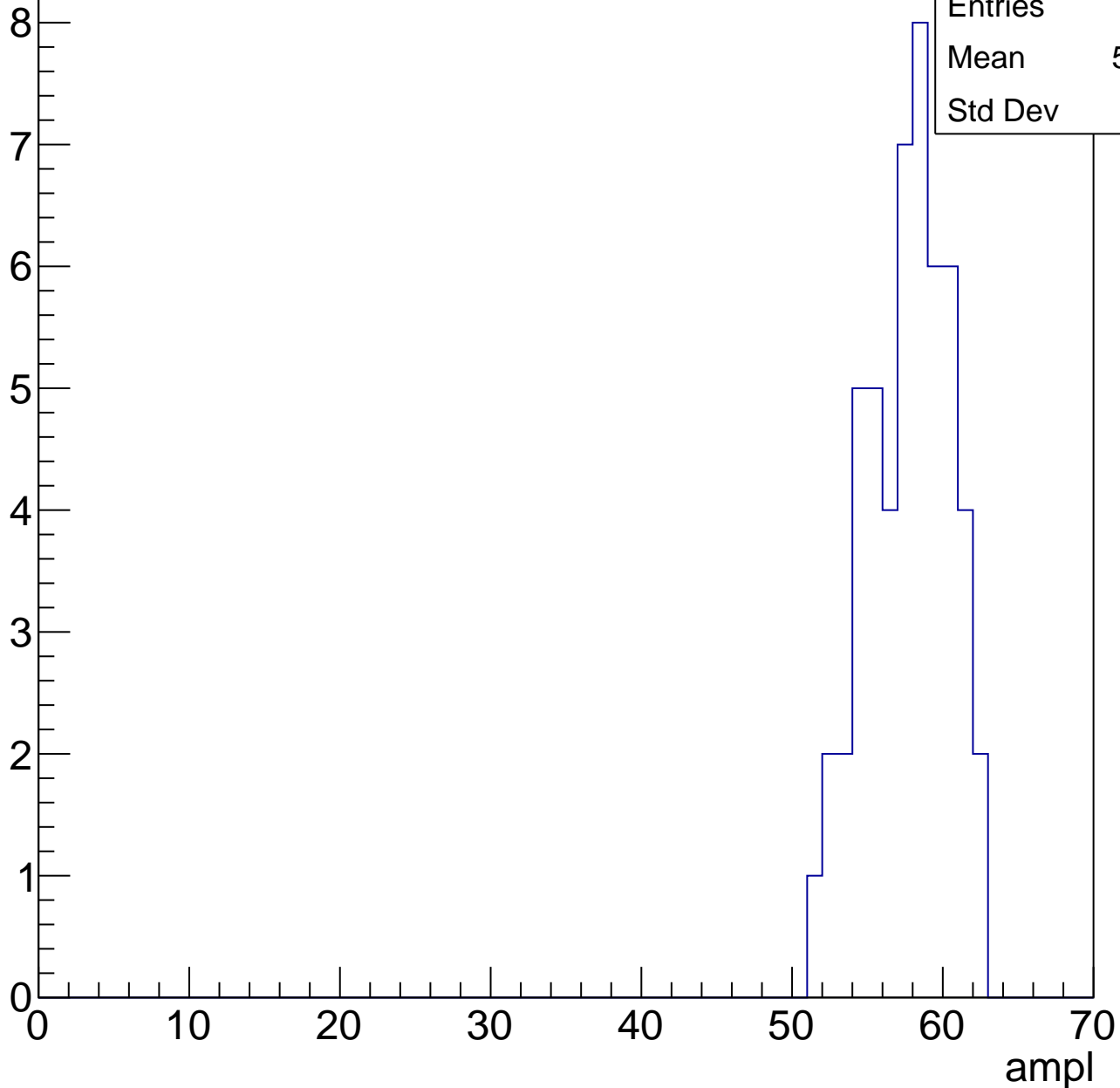
Entries	78
Mean	51.18
Std Dev	3.554



# B0L001S, U5-ch97, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



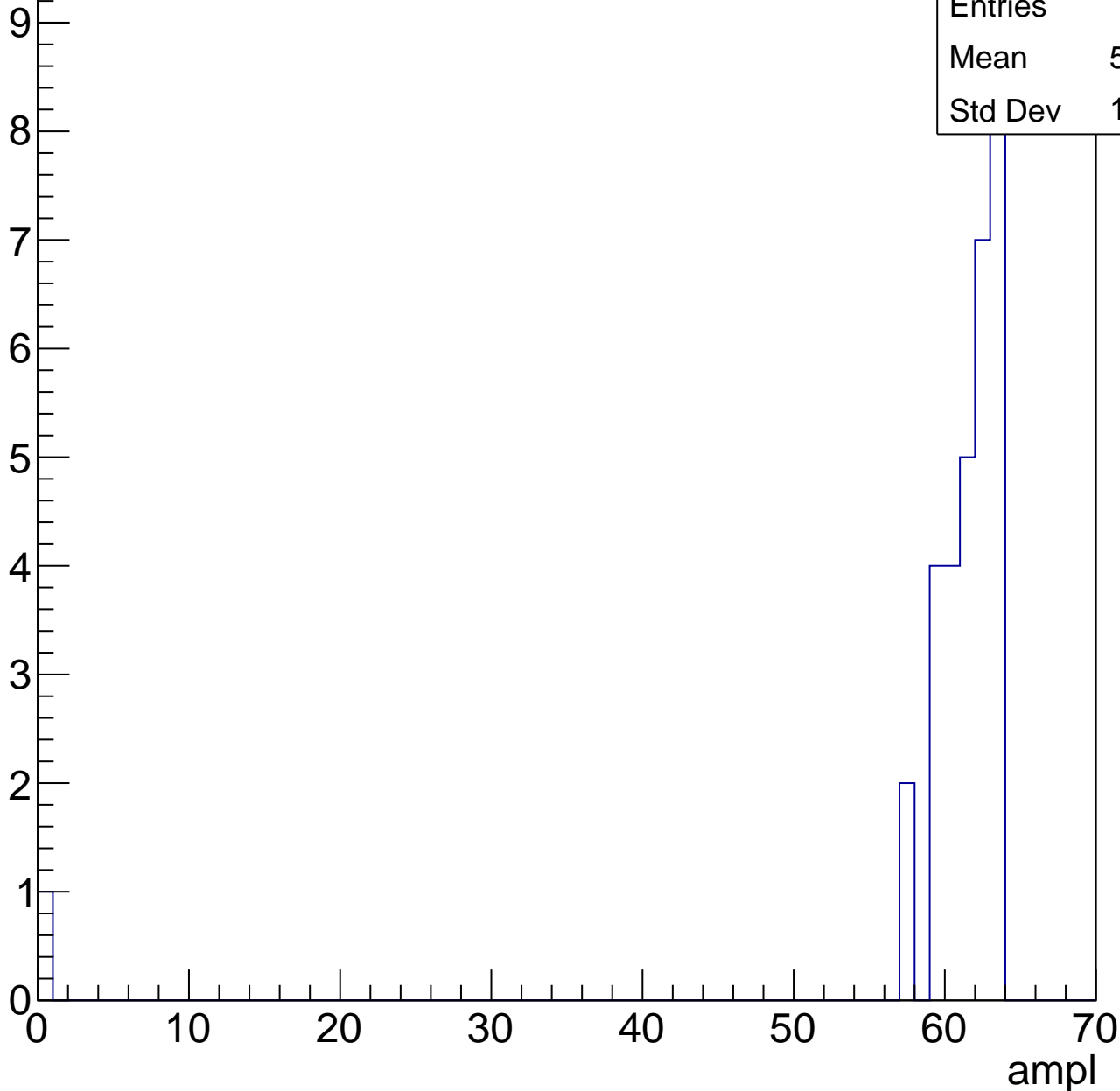
Entries	52
Mean	57.21
Std Dev	2.72

# B0L001S, U5-ch97, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	32
Mean	59.25
Std Dev	10.78



# B0L001S, U5-ch97, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch97, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U5-ch98, adc0

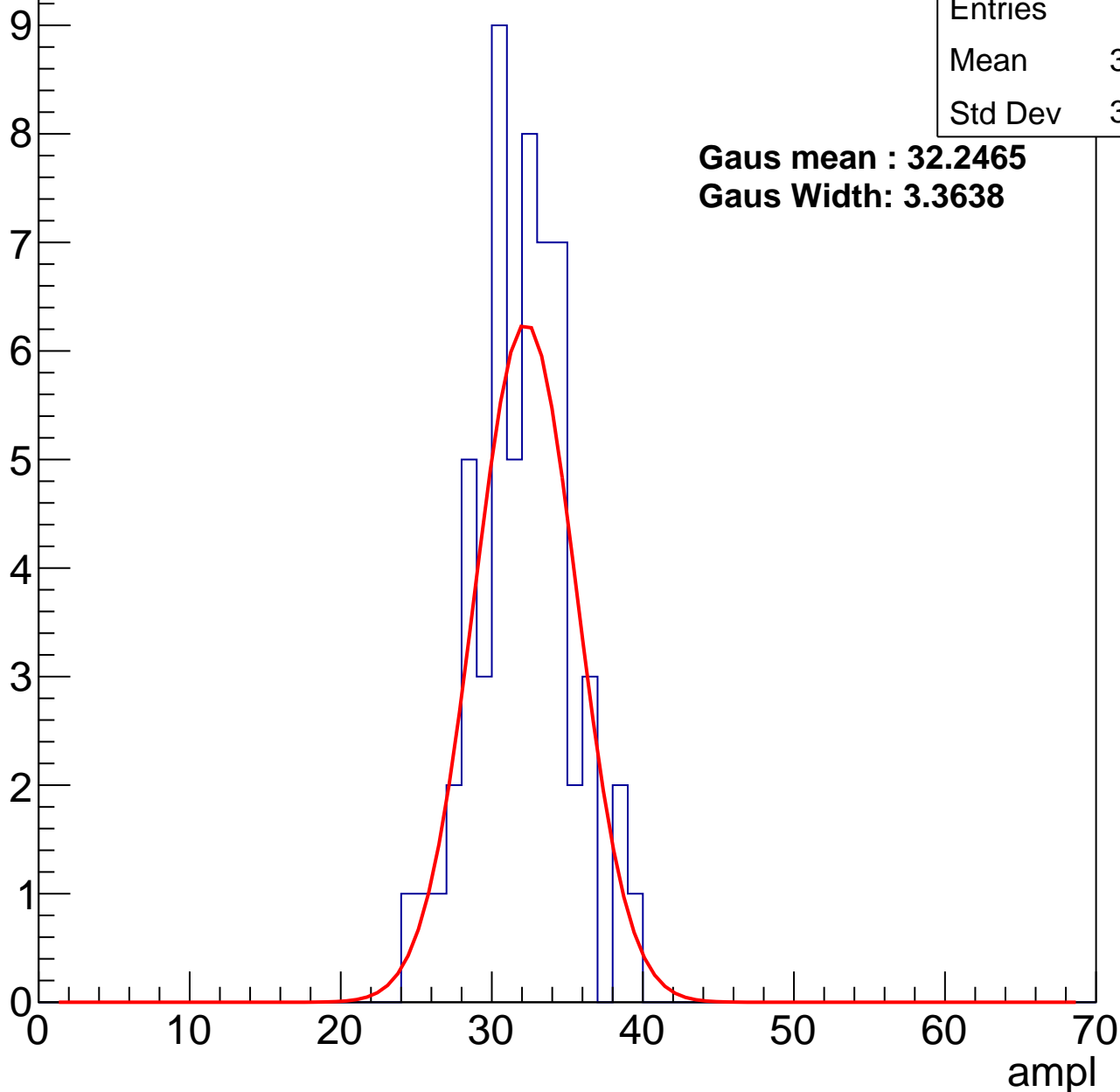
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	31.56
Std Dev	3.129

**Gaus mean : 32.2465**

**Gaus Width: 3.3638**



# B0L001S, U5-ch98, adc1

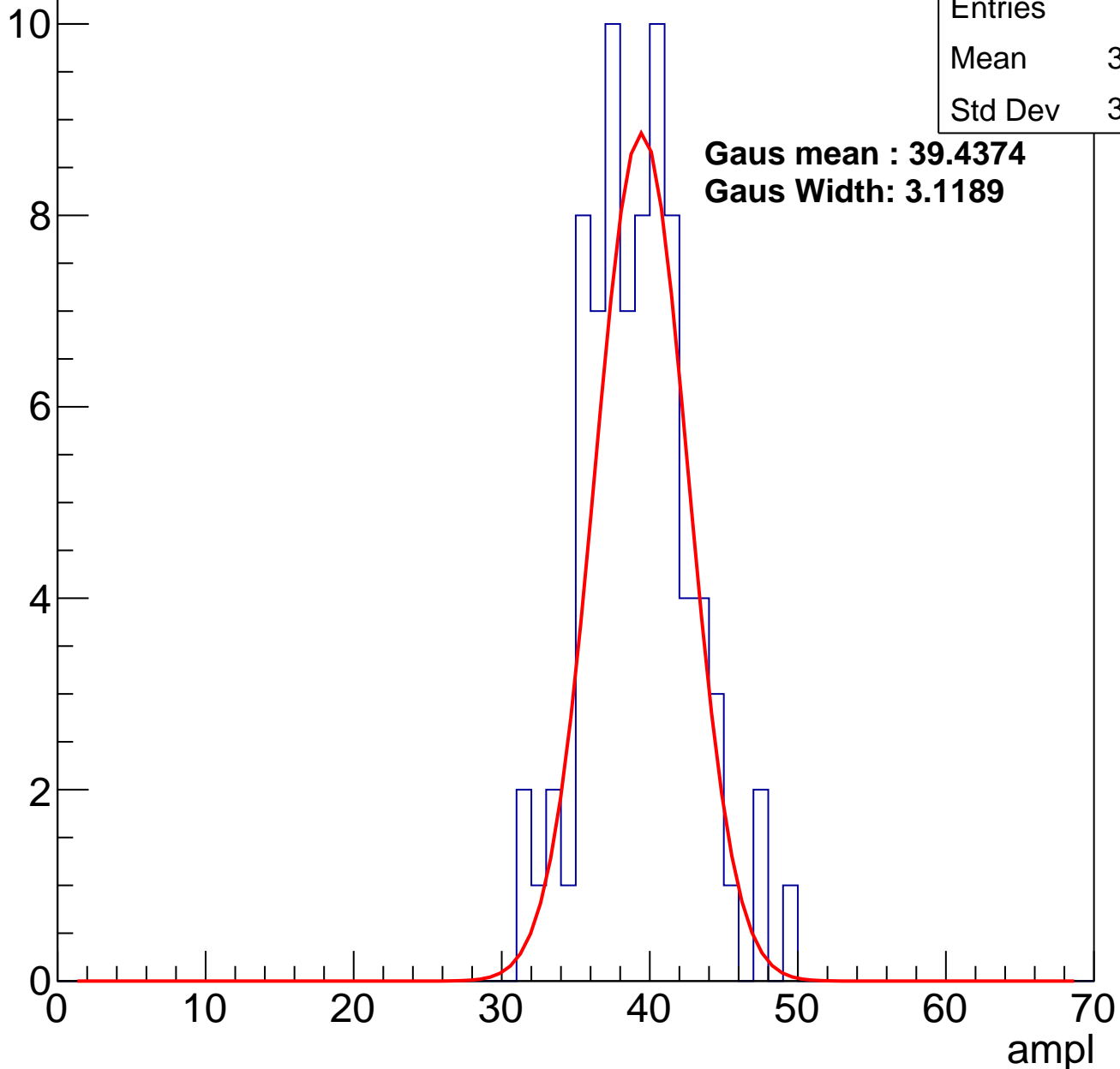
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	79
Mean	38.76
Std Dev	3.537

**Gaus mean : 39.4374**

**Gaus Width: 3.1189**

Entry



# B0L001S, U5-ch98, adc2

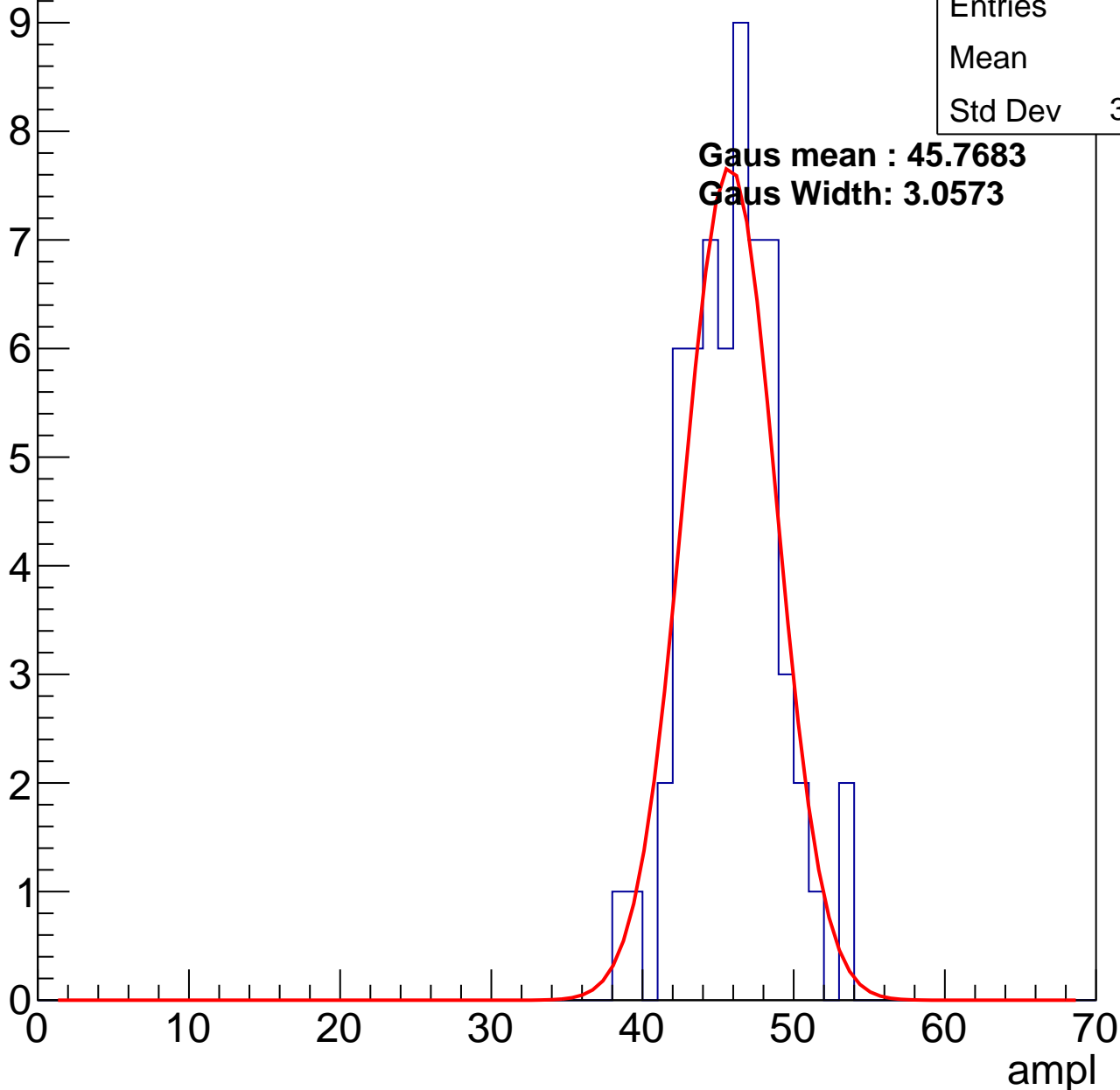
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	45.5
Std Dev	3.025

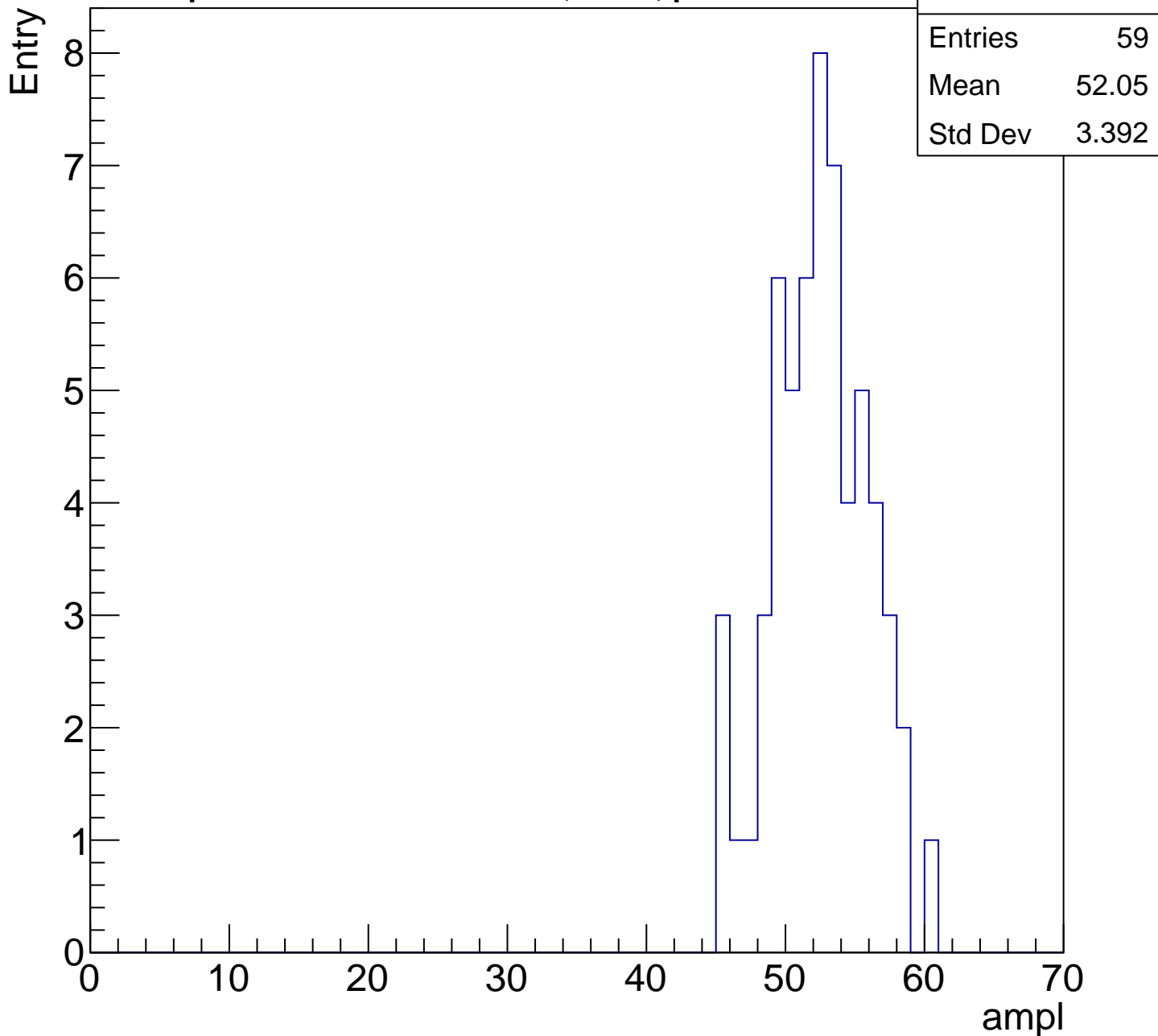
**Gaus mean : 45.7683**

**Gaus Width: 3.0573**



# B0L001S, U5-ch98, adc3

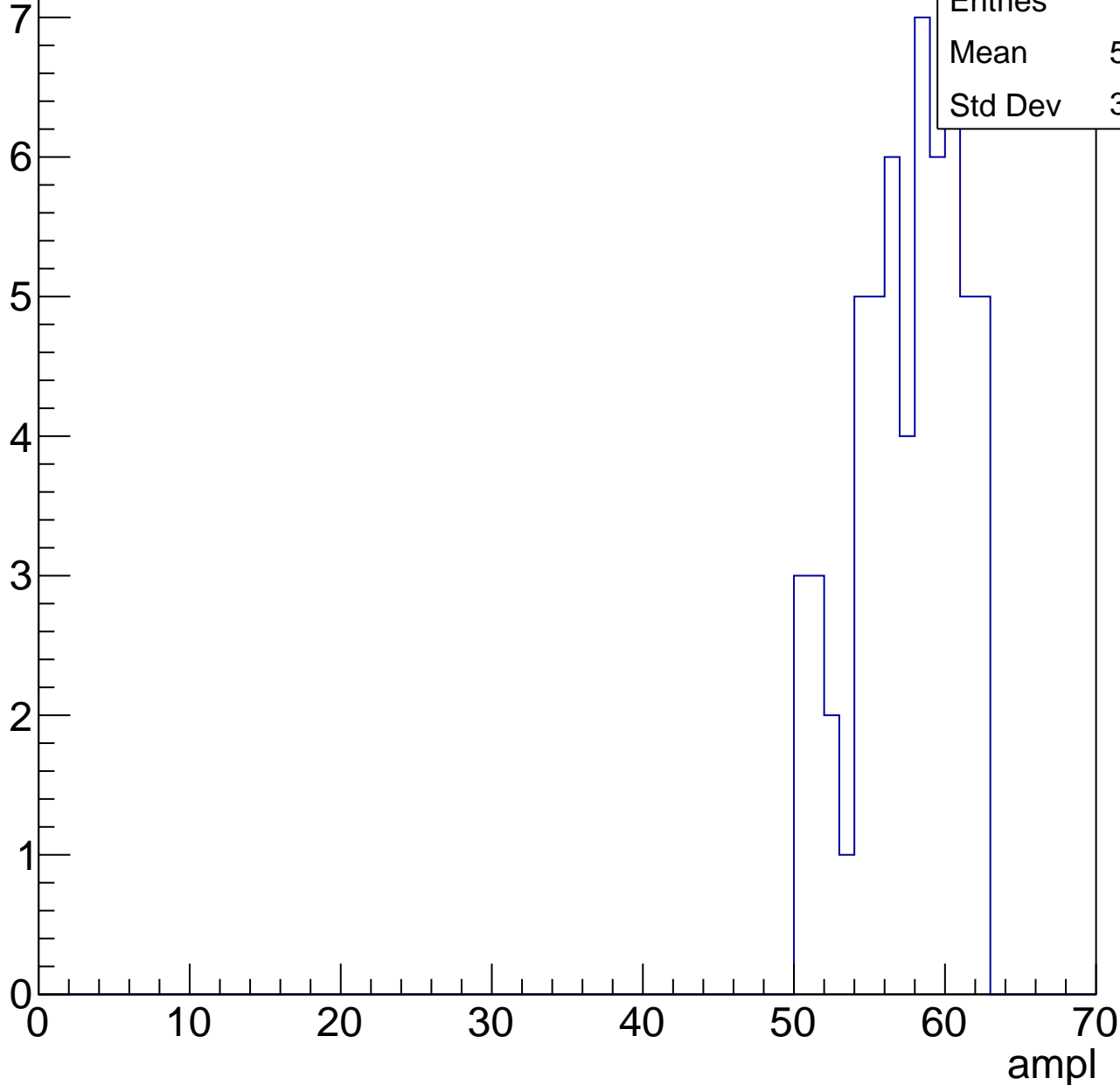
calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U5-ch98, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



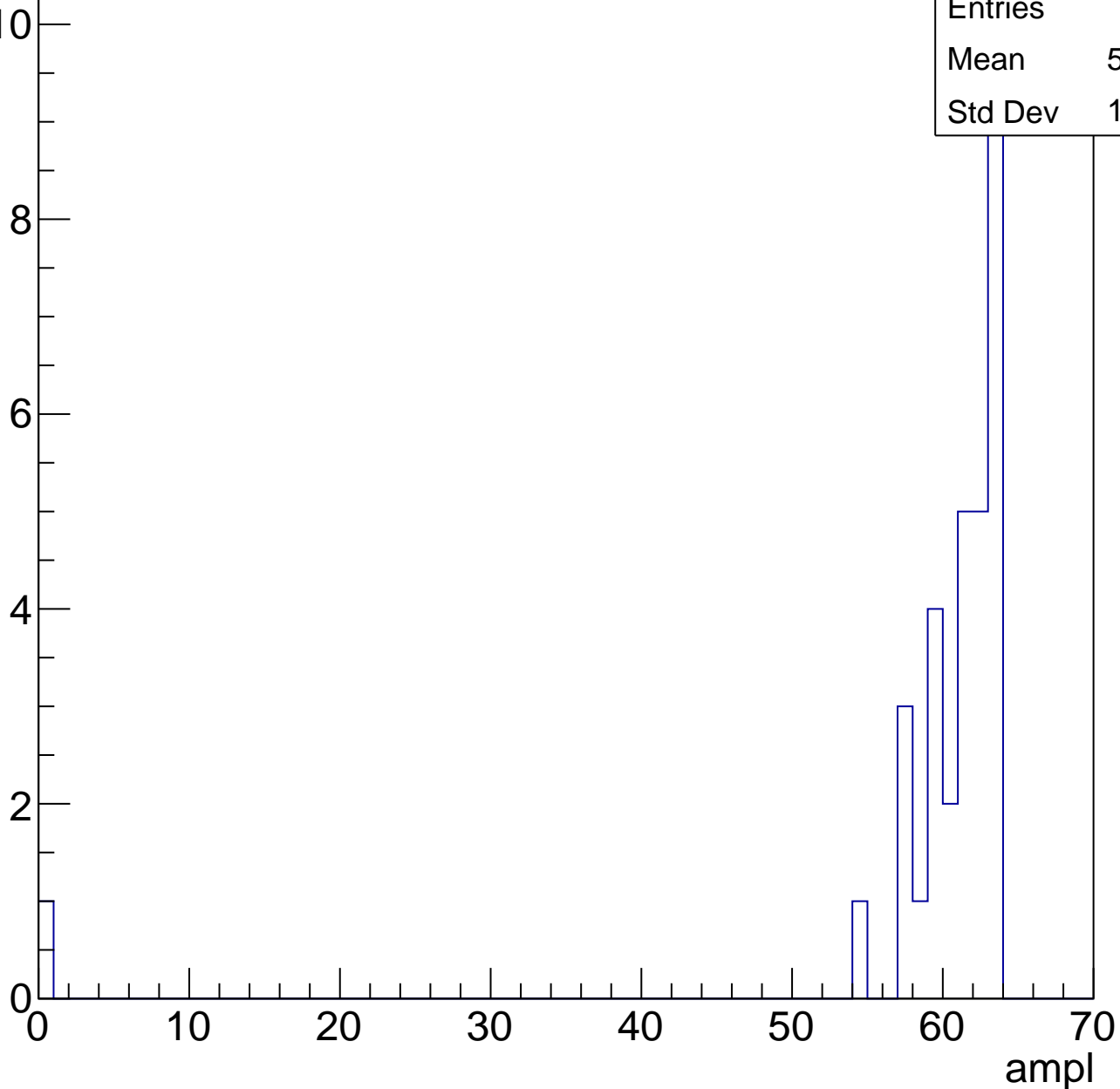
Entries	59
Mean	57.02
Std Dev	3.422

# B0L001S, U5-ch98, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	32
Mean	58.88
Std Dev	10.82



# B0L001S, U5-ch98, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U5-ch98, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U5-ch99, adc0

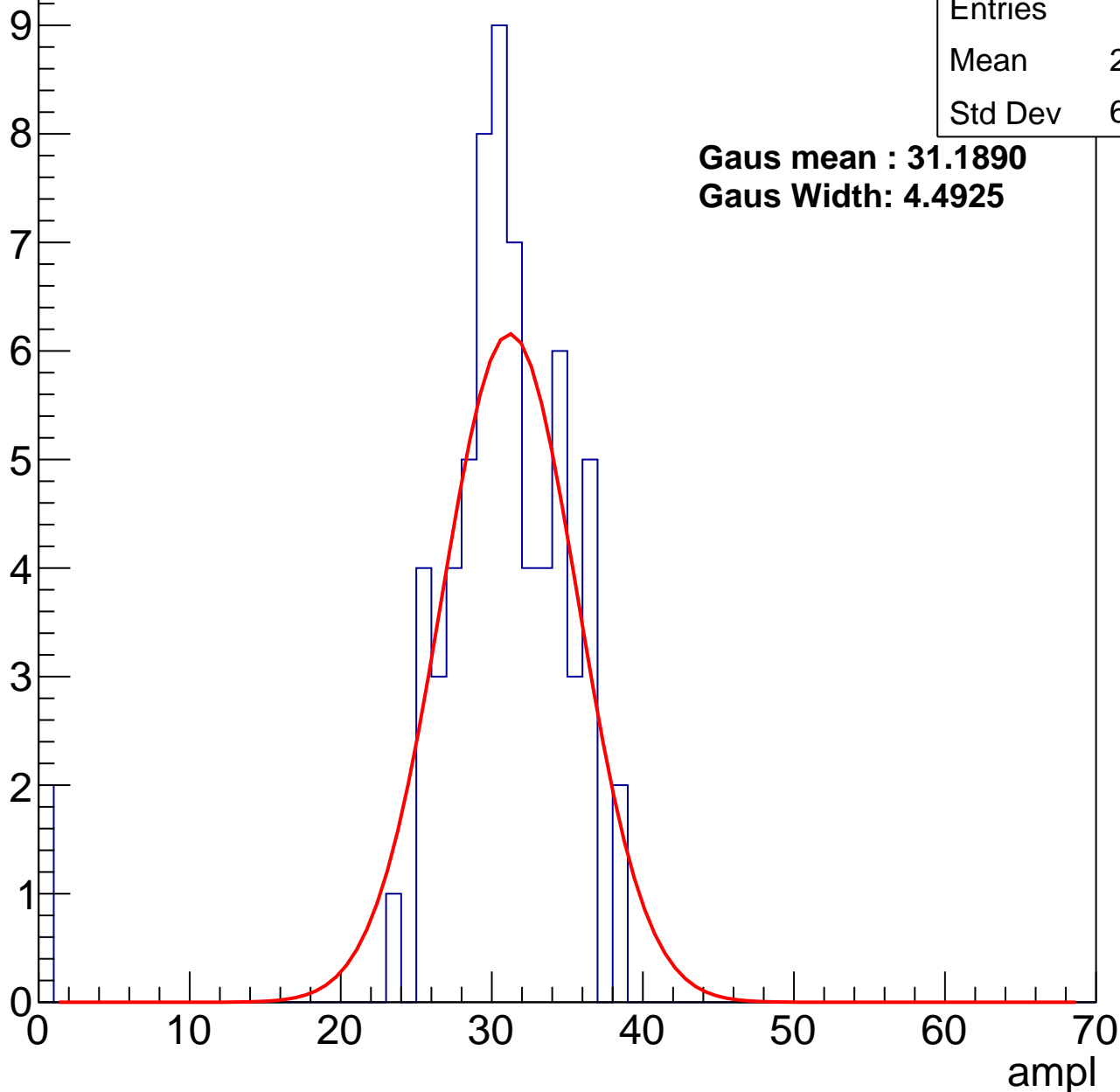
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	29.75
Std Dev	6.223

**Gaus mean : 31.1890**

**Gaus Width: 4.4925**



# B0L001S, U5-ch99, adc1

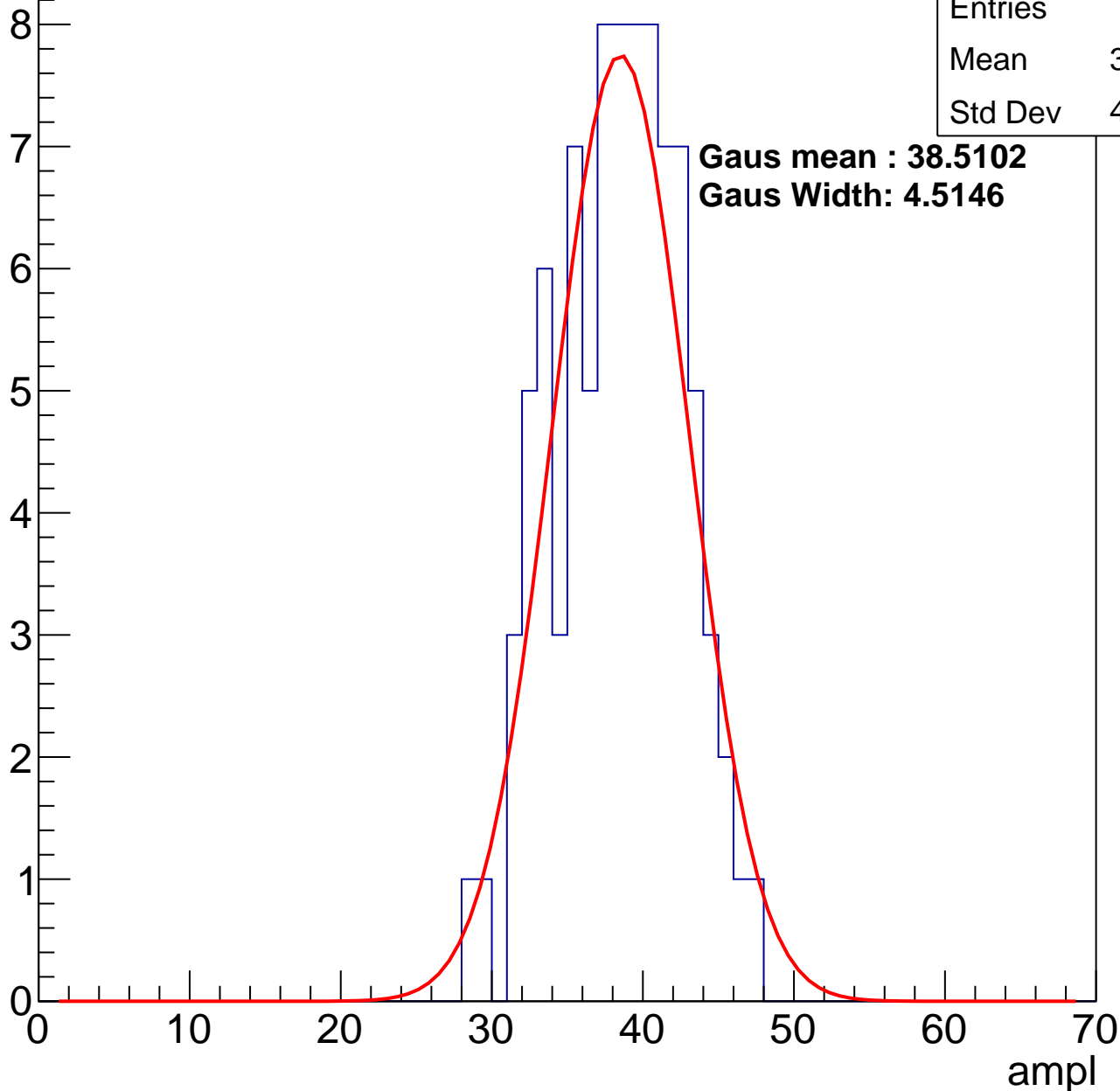
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	89
Mean	37.96
Std Dev	4.089

**Gaus mean : 38.5102**

**Gaus Width: 4.5146**



# B0L001S, U5-ch99, adc2

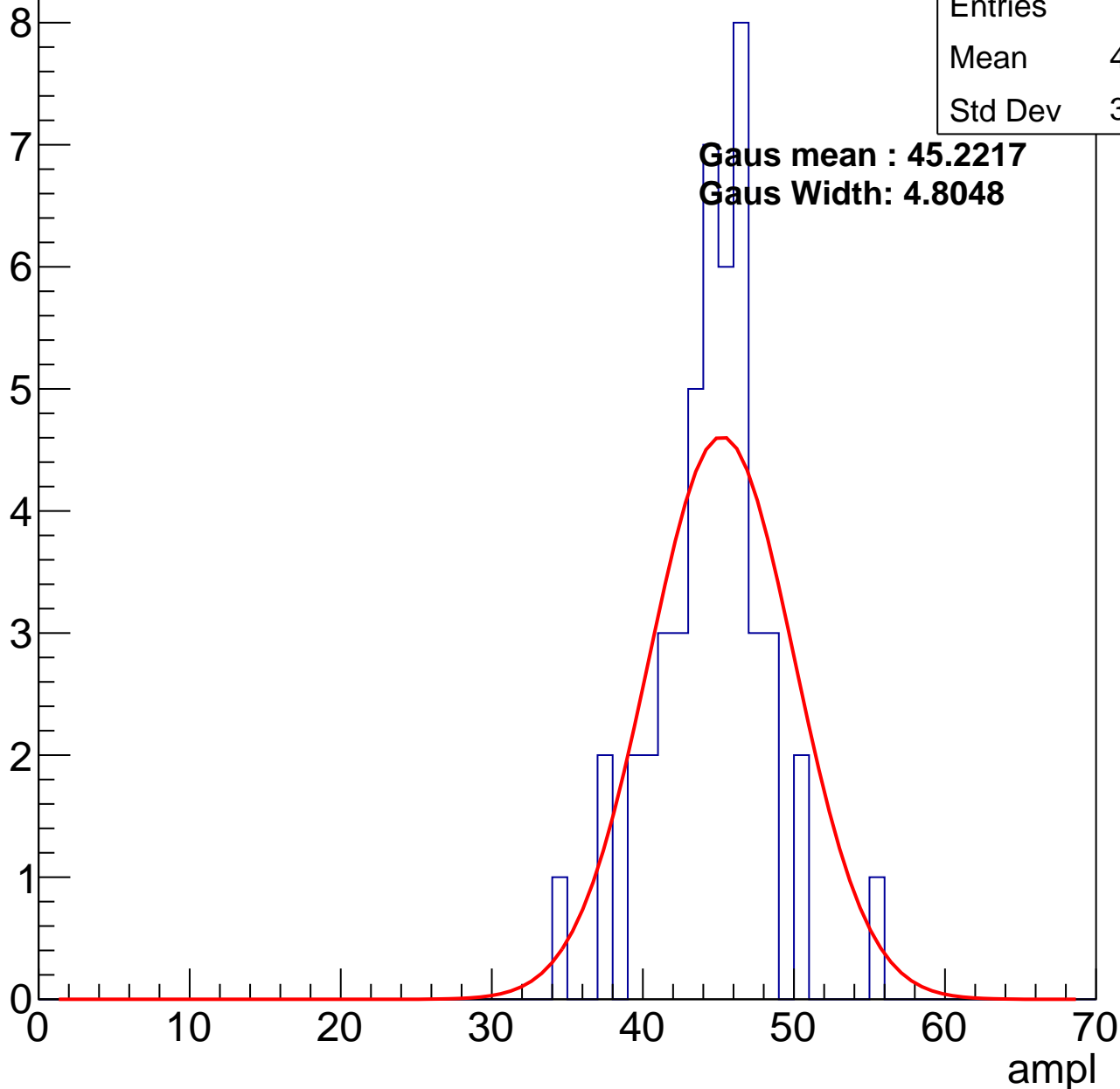
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	48
Mean	44.08
Std Dev	3.622

**Gaus mean : 45.2217**

**Gaus Width: 4.8048**



# B0L001S, U5-ch99, adc3

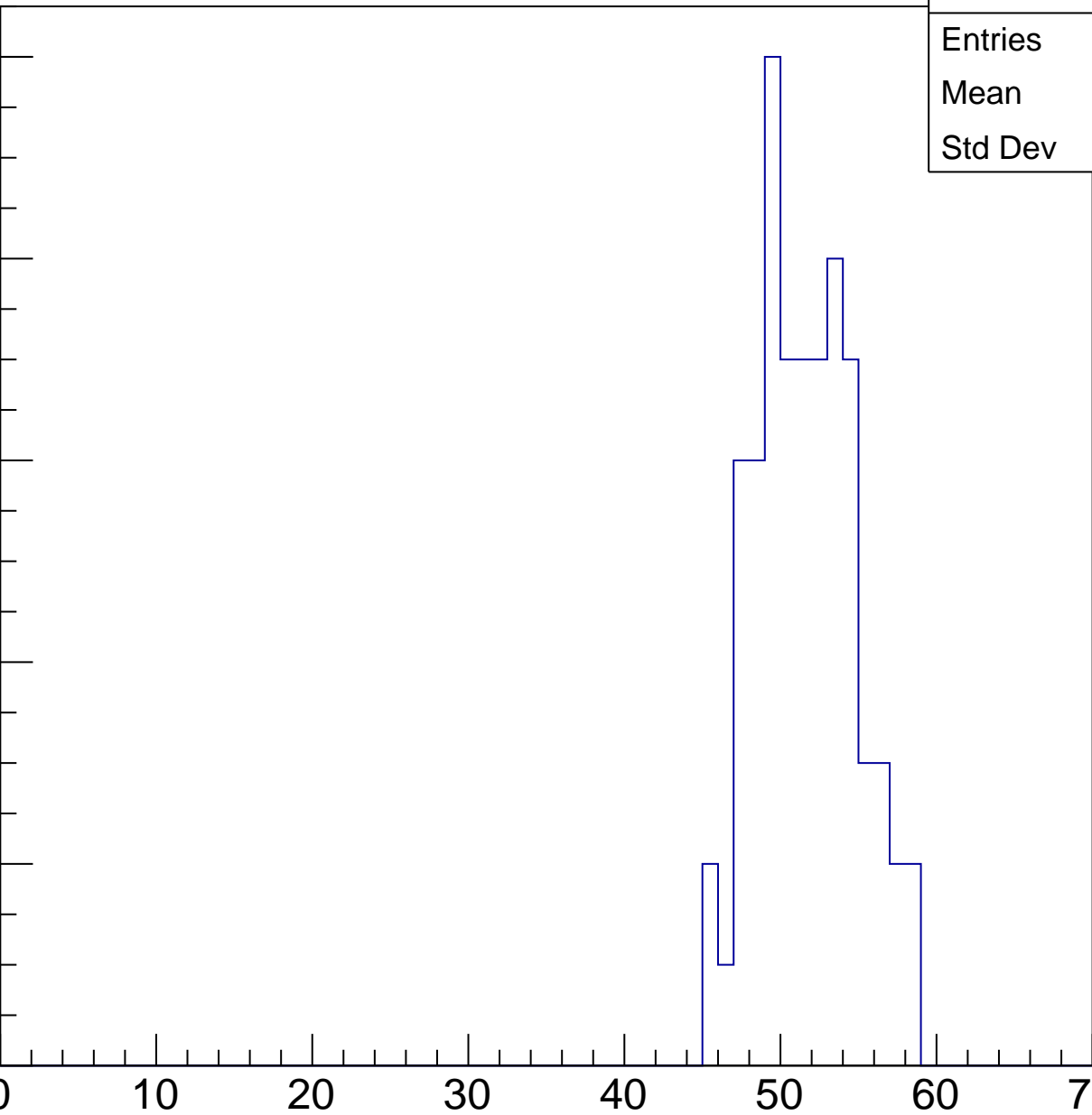
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	71
Mean	51.15
Std Dev	3.111

Entry

10  
8  
6  
4  
2  
0

ampl



# B0L001S, U5-ch99, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	59
Mean	56.93
Std Dev	3.399

Entry

10

8

6

4

2

0

0

10

20

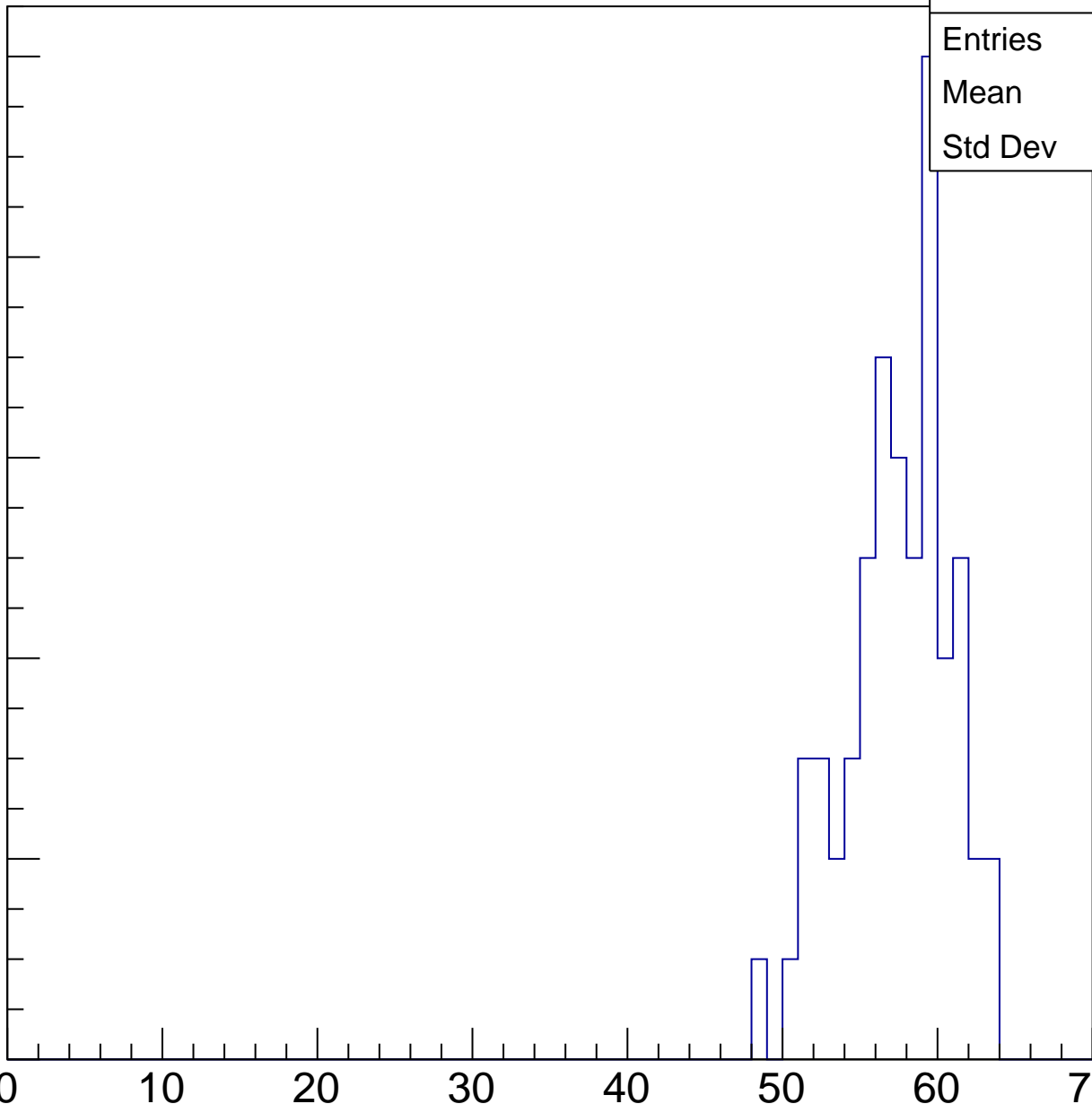
30

40

50

60

ampl

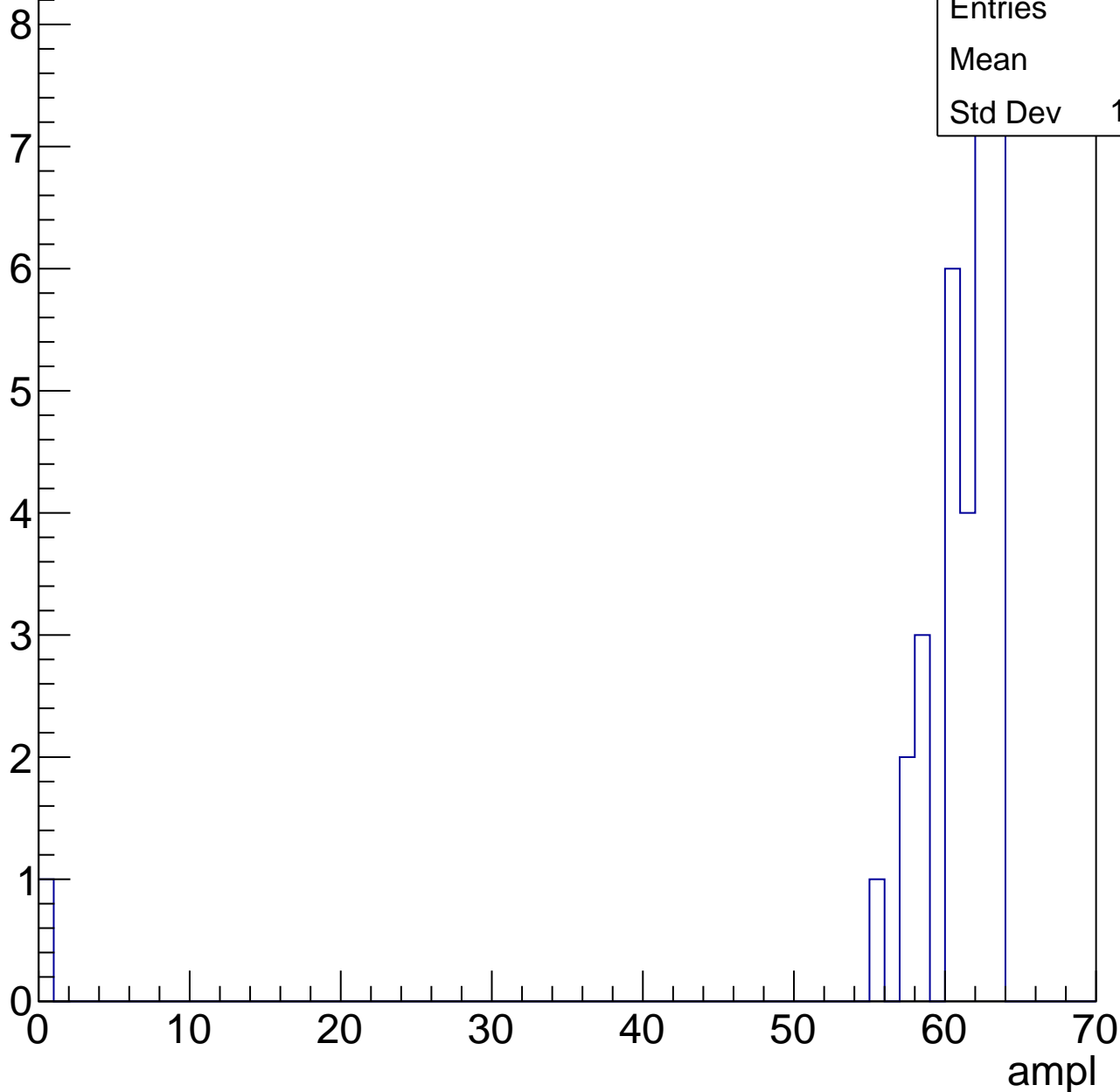


# B0L001S, U5-ch99, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

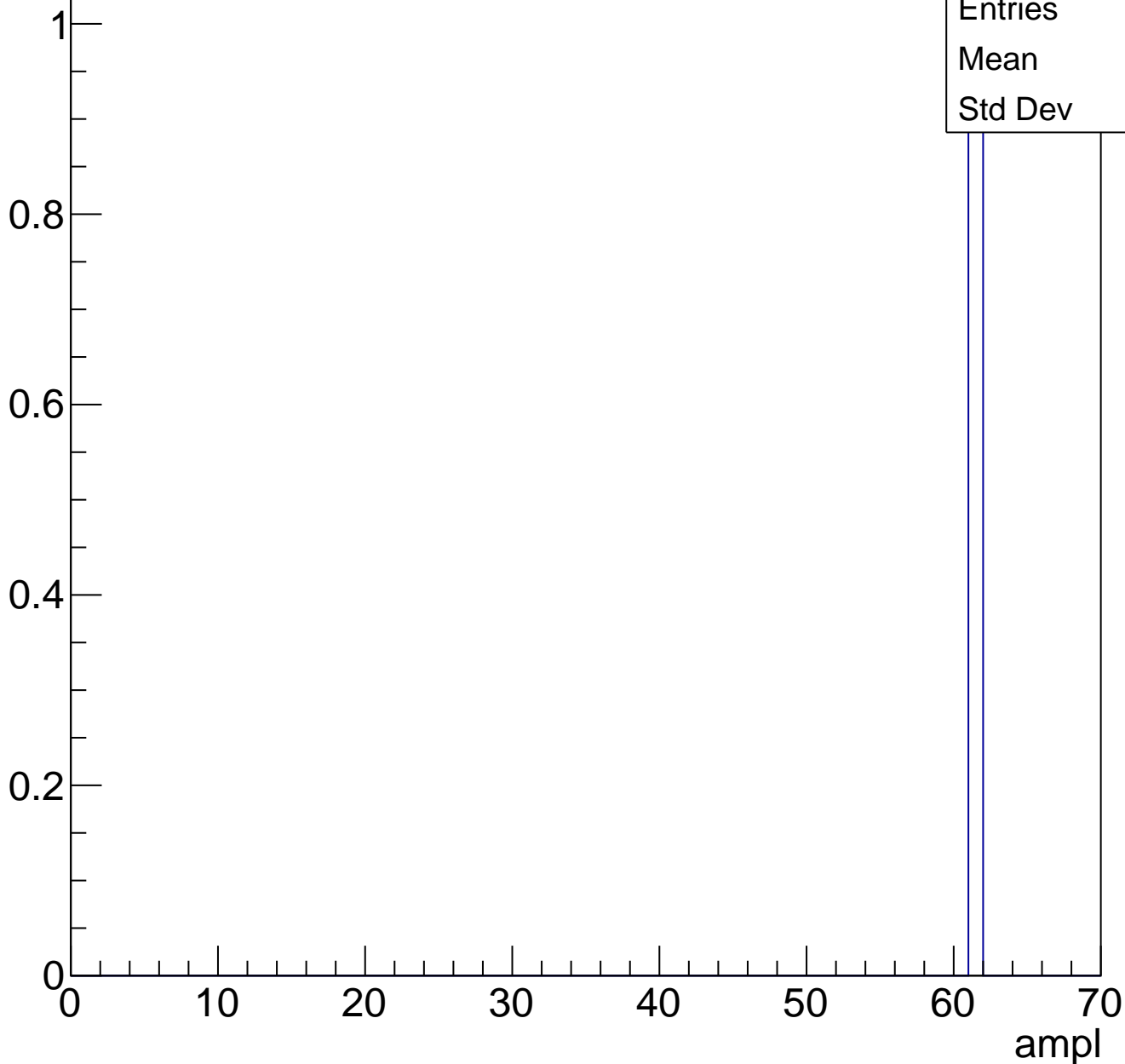
Entries	33
Mean	59
Std Dev	10.63



# B0L001S, U5-ch99, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch99, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U5-ch100, adc0

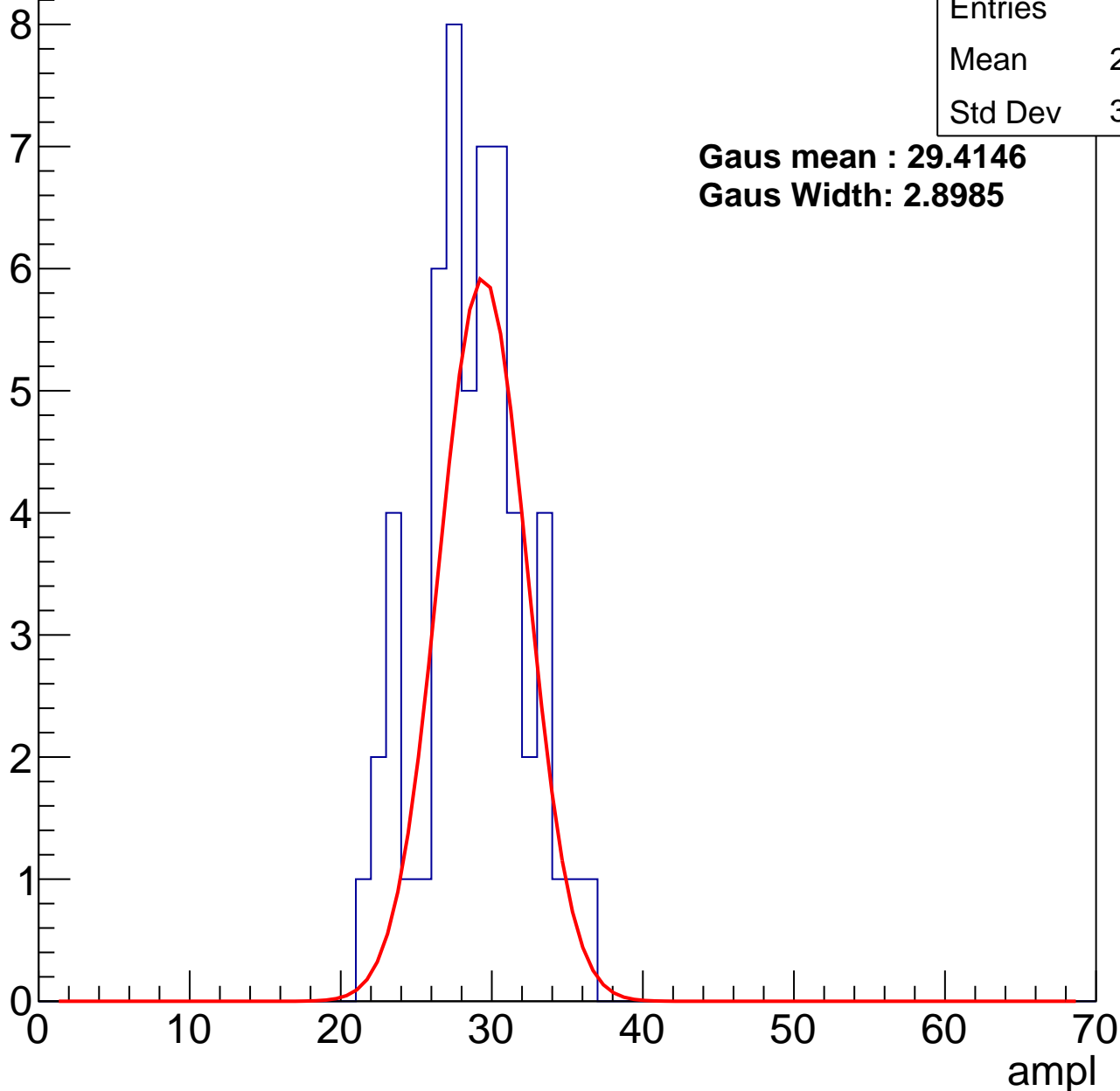
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	28.29
Std Dev	3.372

**Gaus mean : 29.4146**

**Gaus Width: 2.8985**



# B0L001S, U5-ch100, adc1

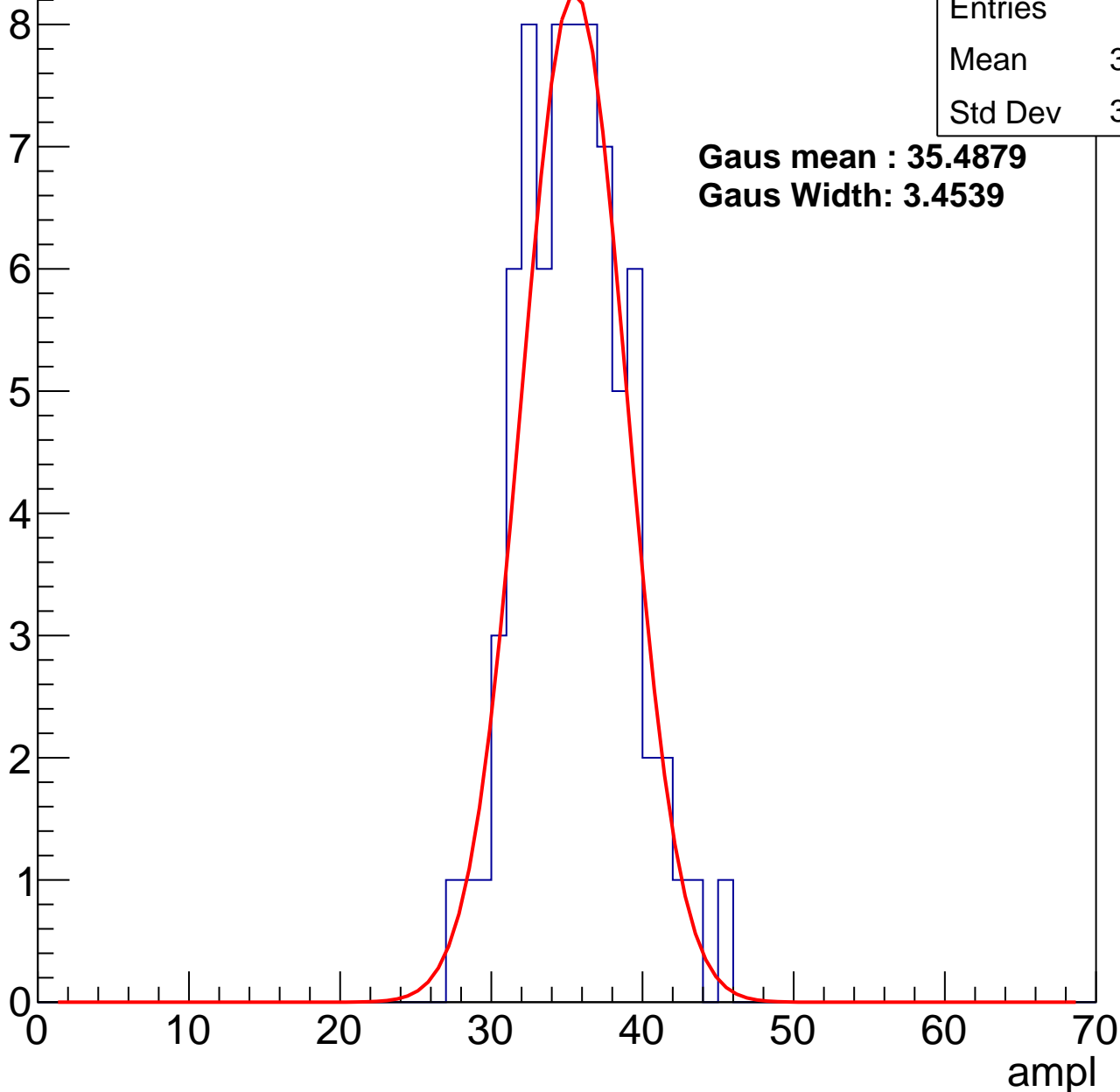
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	75
Mean	35.05
Std Dev	3.532

**Gaus mean : 35.4879**

**Gaus Width: 3.4539**



# B0L001S, U5-ch100, adc2

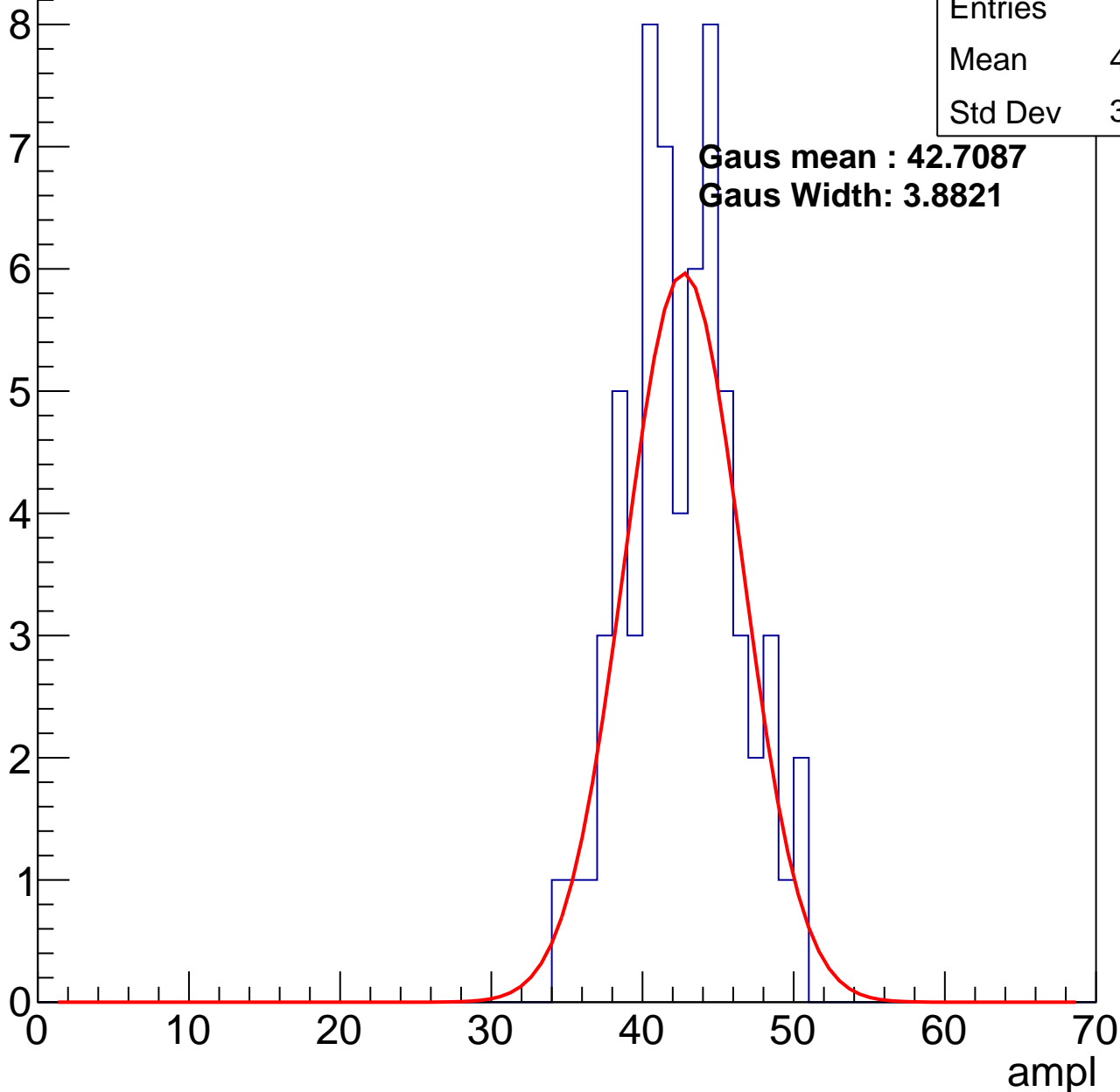
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	42.19
Std Dev	3.638

**Gaus mean : 42.7087**

**Gaus Width: 3.8821**

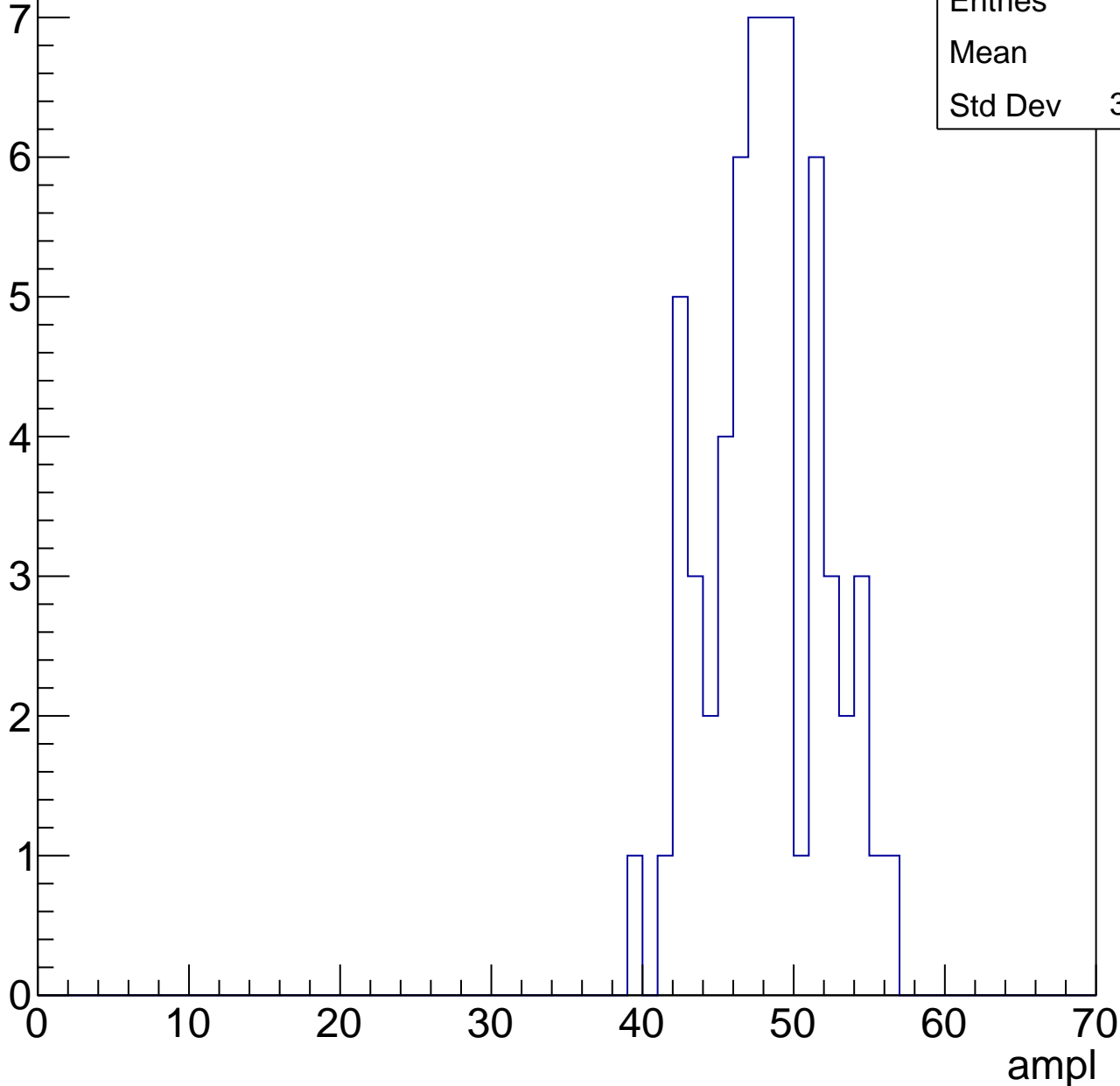


# B0L001S, U5-ch100, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	47.7
Std Dev	3.792

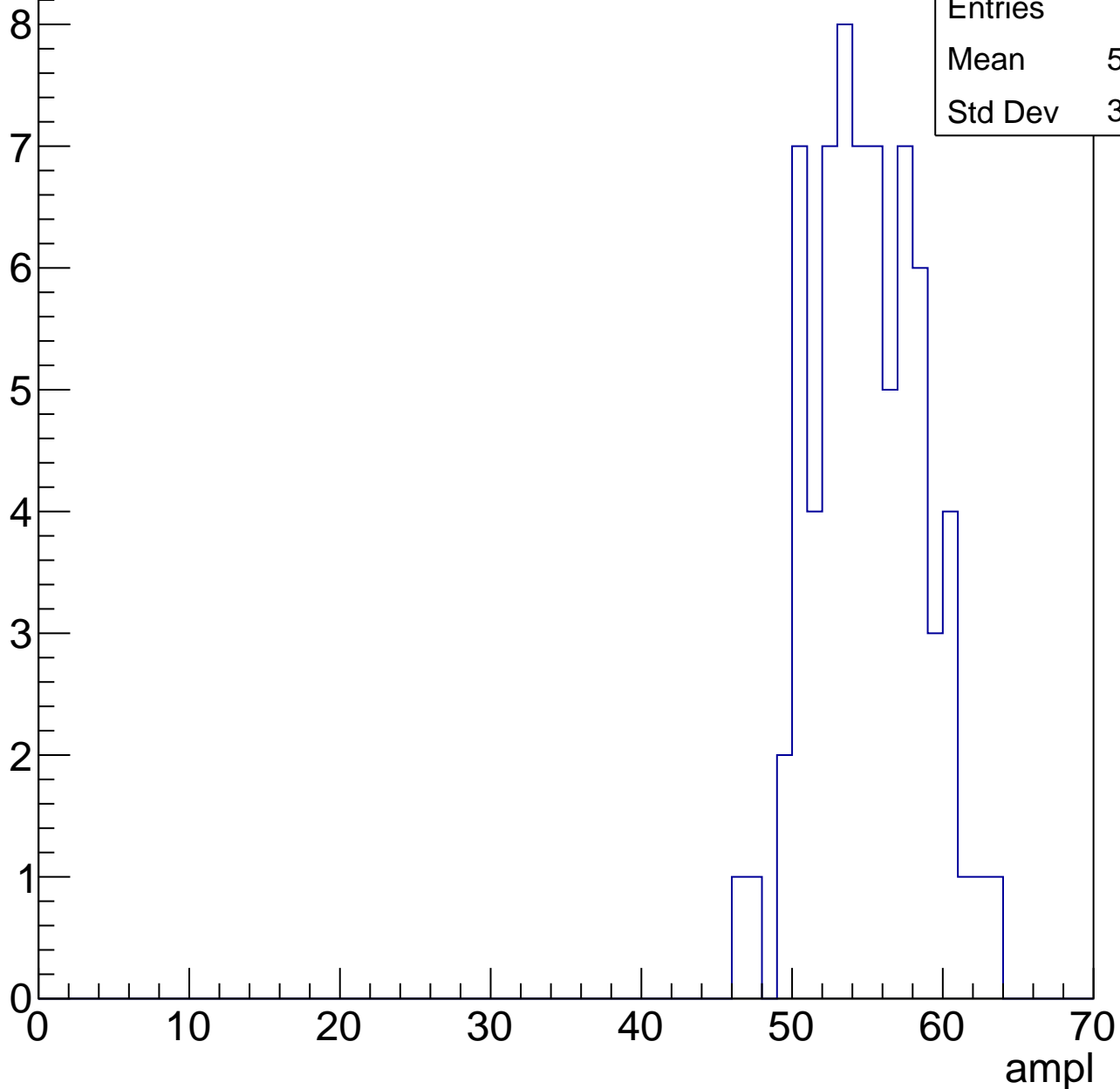


# B0L001S, U5-ch100, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	54.53
Std Dev	3.586



# B0L001S, U5-ch100, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

6

5

4

3

2

1

0

Entries	36
Mean	59.58
Std Dev	2.373

0

10

20

30

40

50

60

70

ampl

0

10

20

30

40

50

60

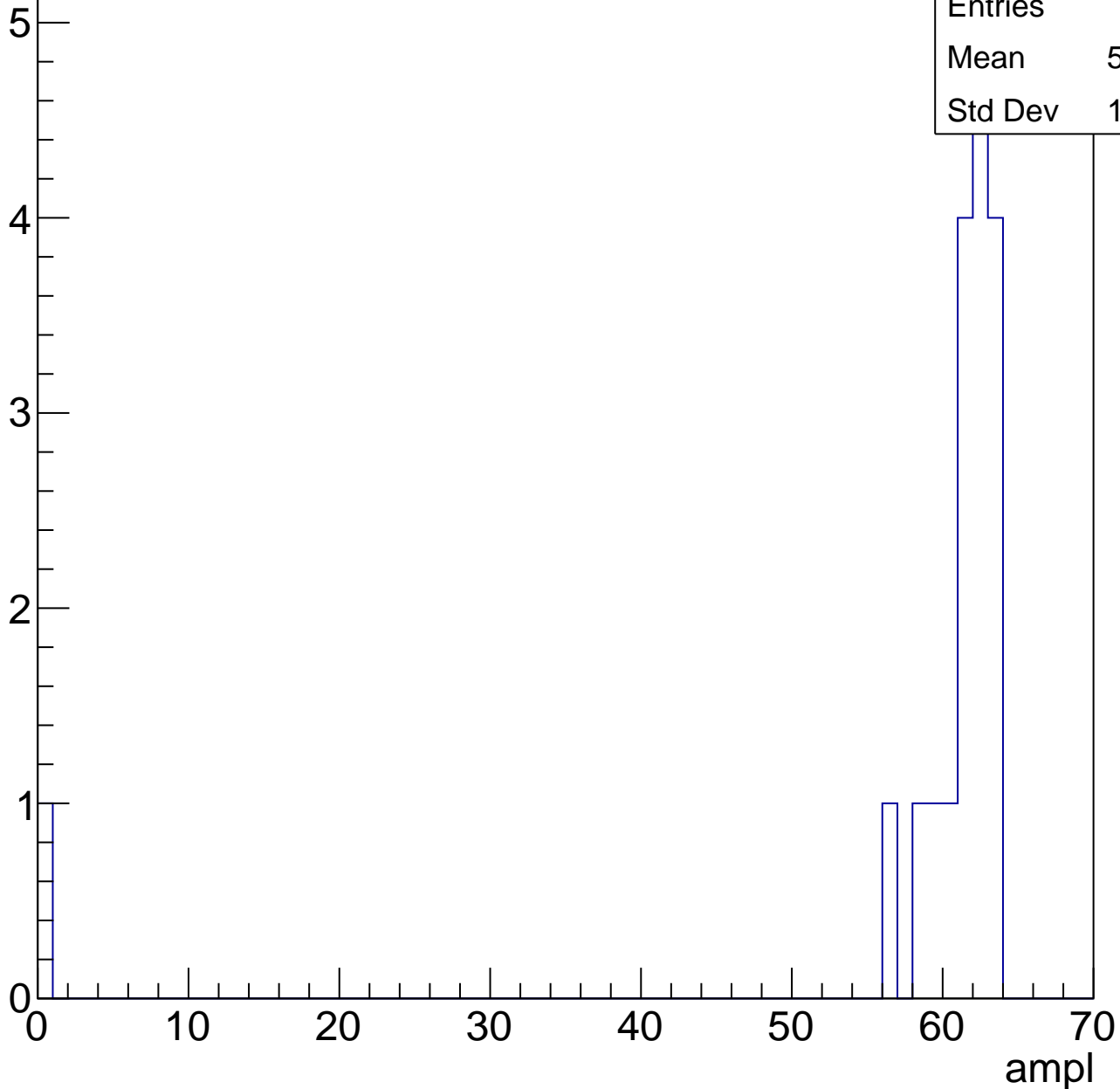
70

# B0L001S, U5-ch100, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	18
Mean	57.72
Std Dev	14.12

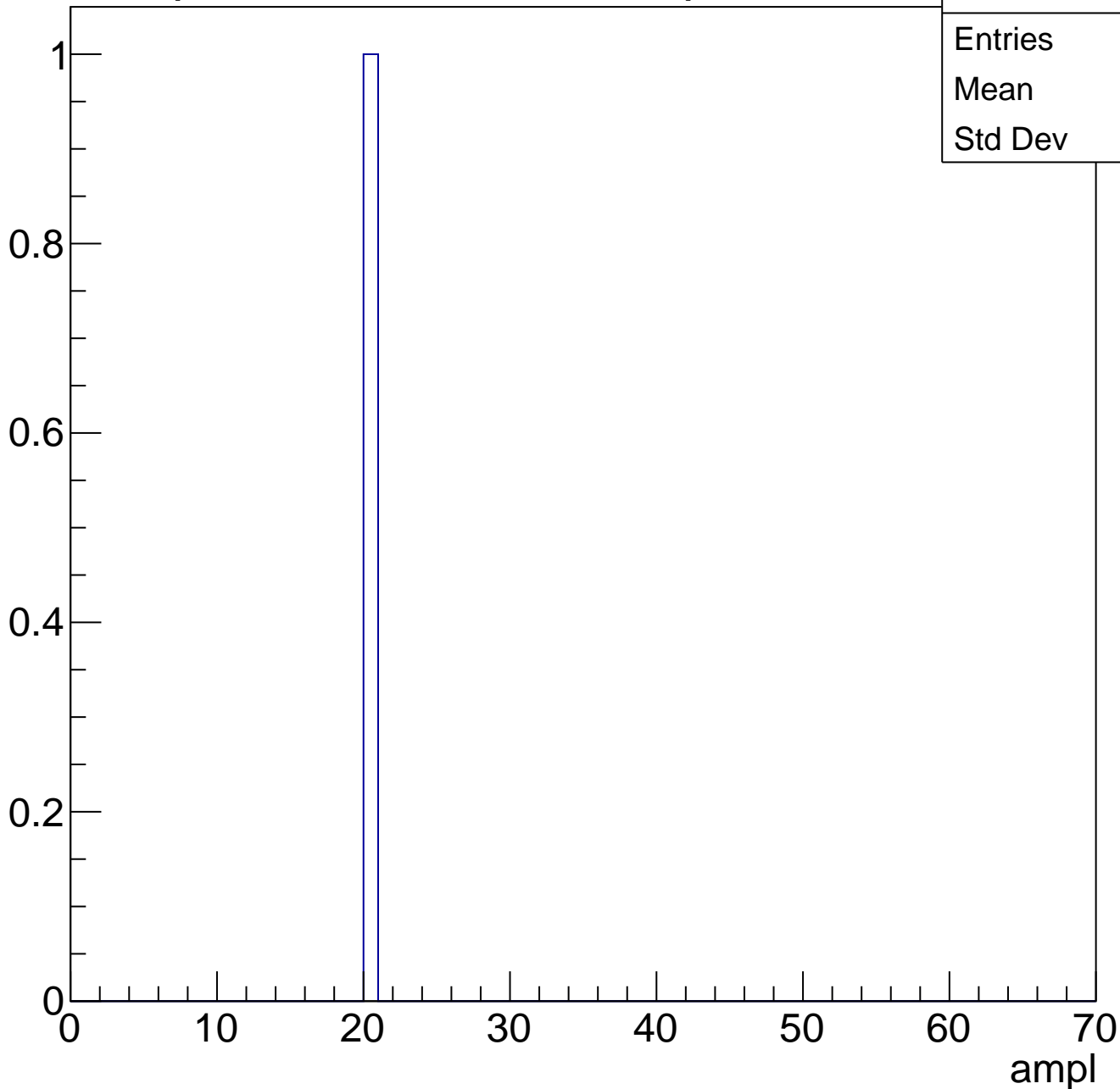




# B0L001S, U5-ch100, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	20
Std Dev	0

# B0L001S, U5-ch101, adc0

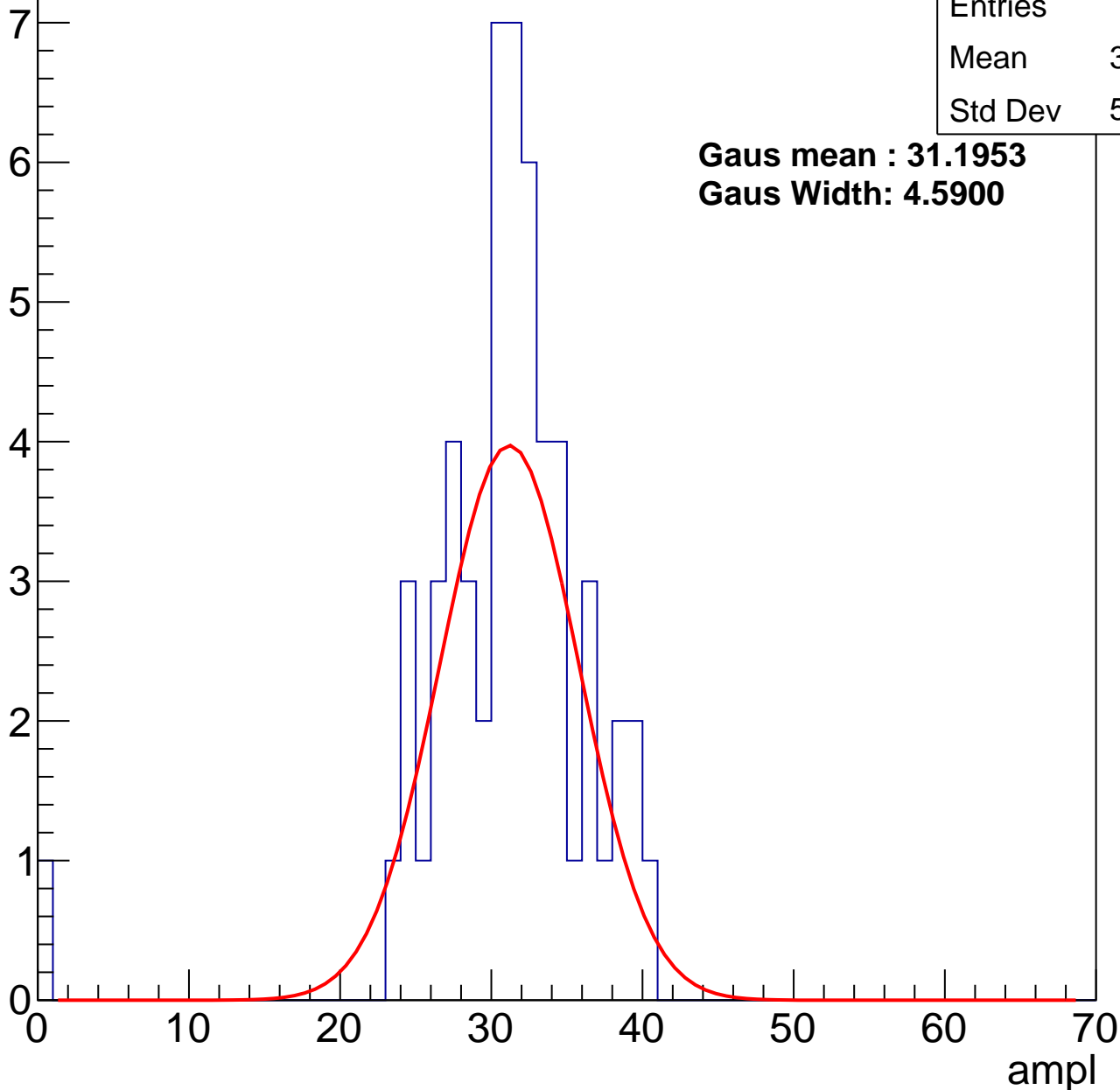
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	30.52
Std Dev	5.776

**Gaus mean : 31.1953**

**Gaus Width: 4.5900**



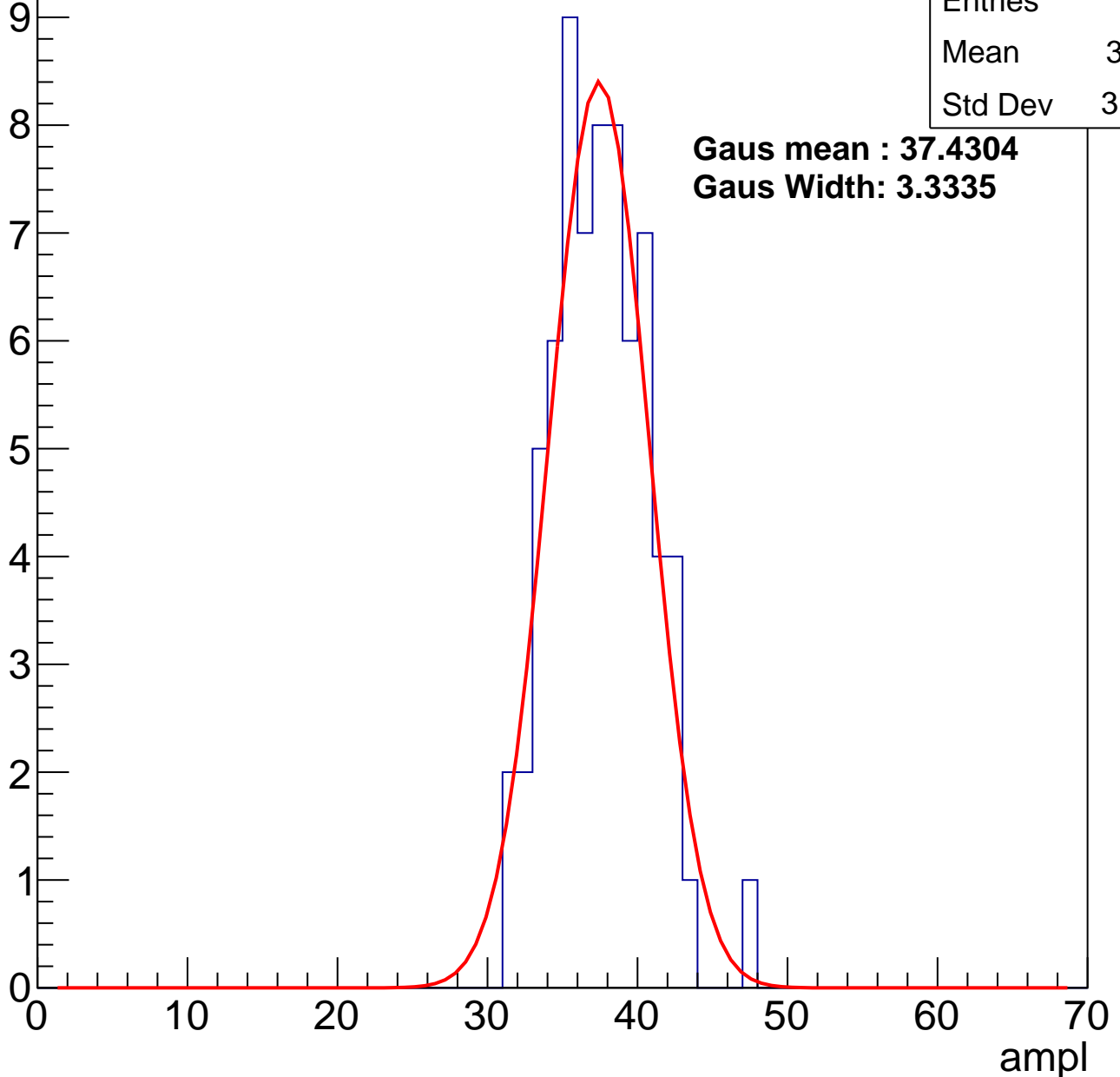
# B0L001S, U5-ch101, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	37.11
Std Dev	3.147

**Gaus mean : 37.4304**  
**Gaus Width: 3.3335**



# B0L001S, U5-ch101, adc2

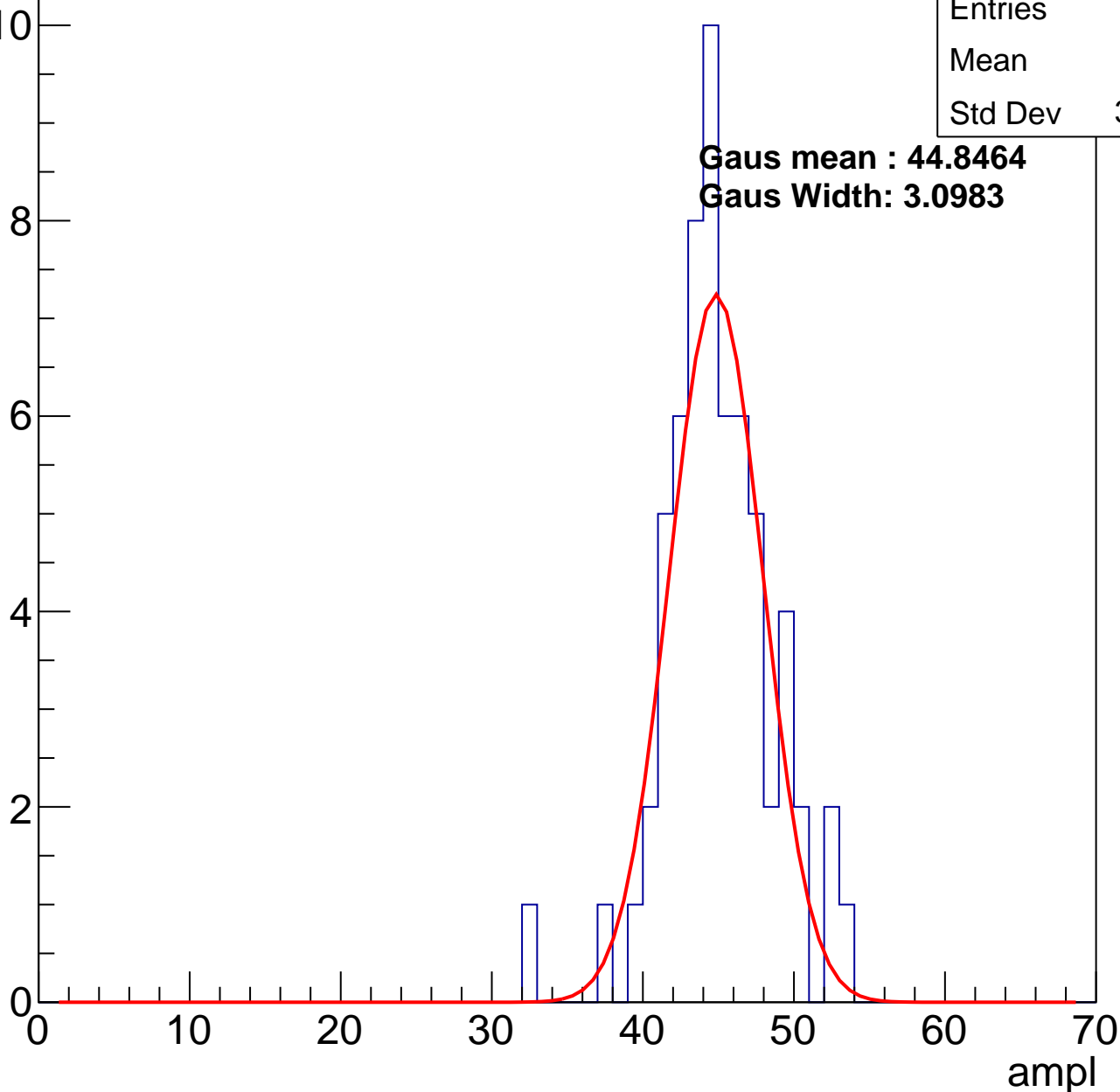
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	44.5
Std Dev	3.591

**Gaus mean : 44.8464**

**Gaus Width: 3.0983**



# B0L001S, U5-ch101, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

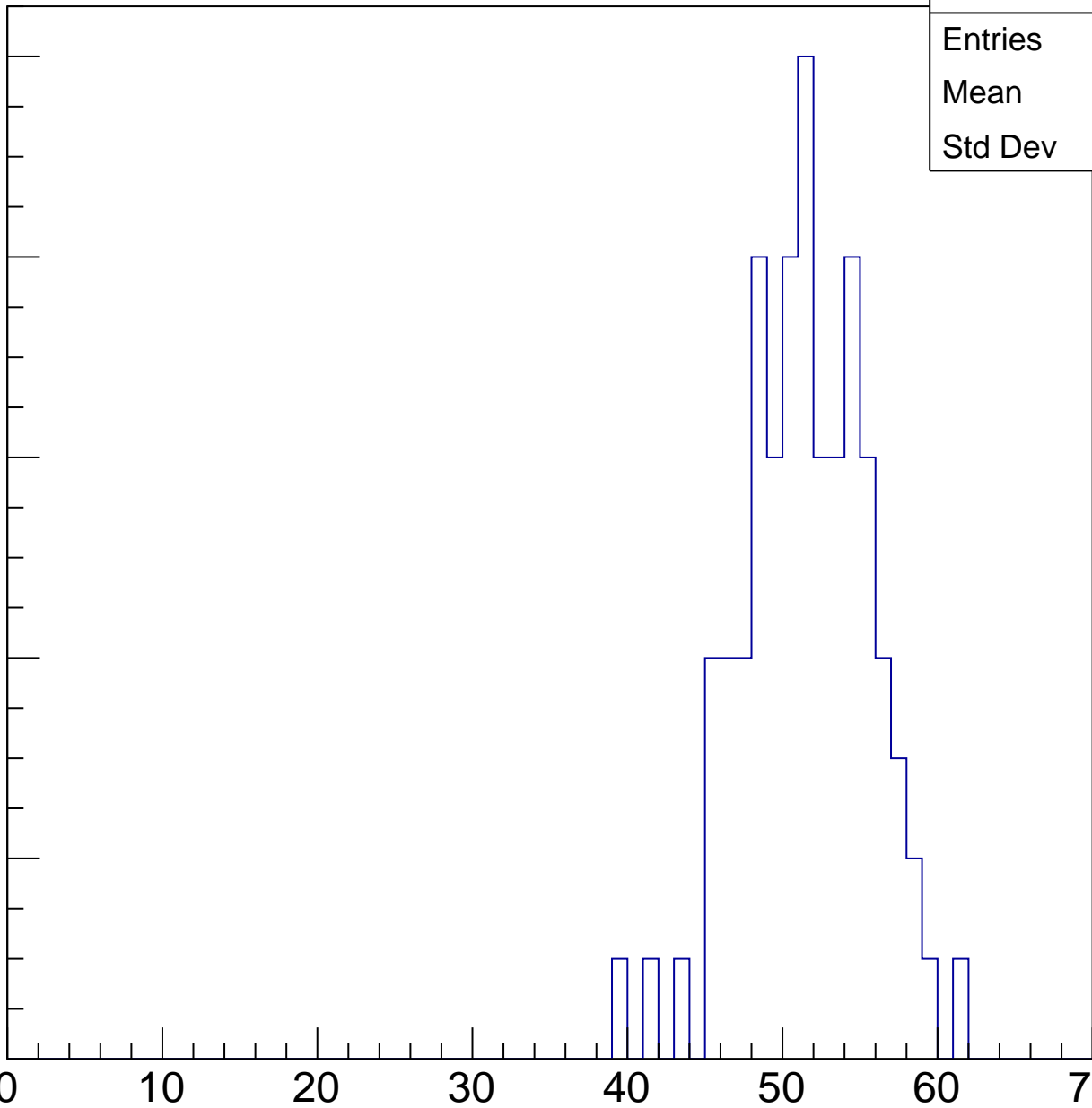
Entries	84
Mean	51.02
Std Dev	4.065

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

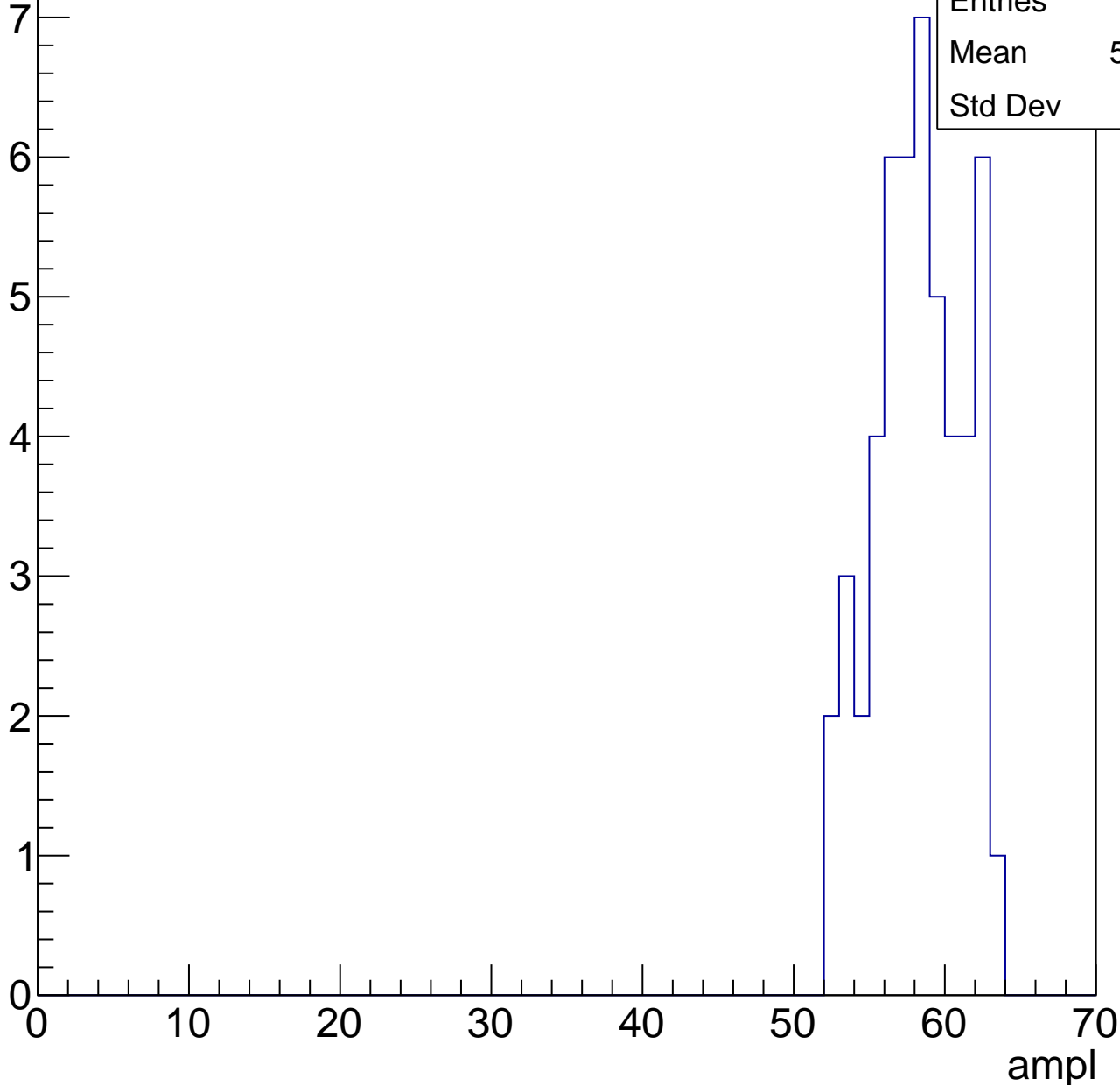


# B0L001S, U5-ch101, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	50
Mean	57.78
Std Dev	2.9

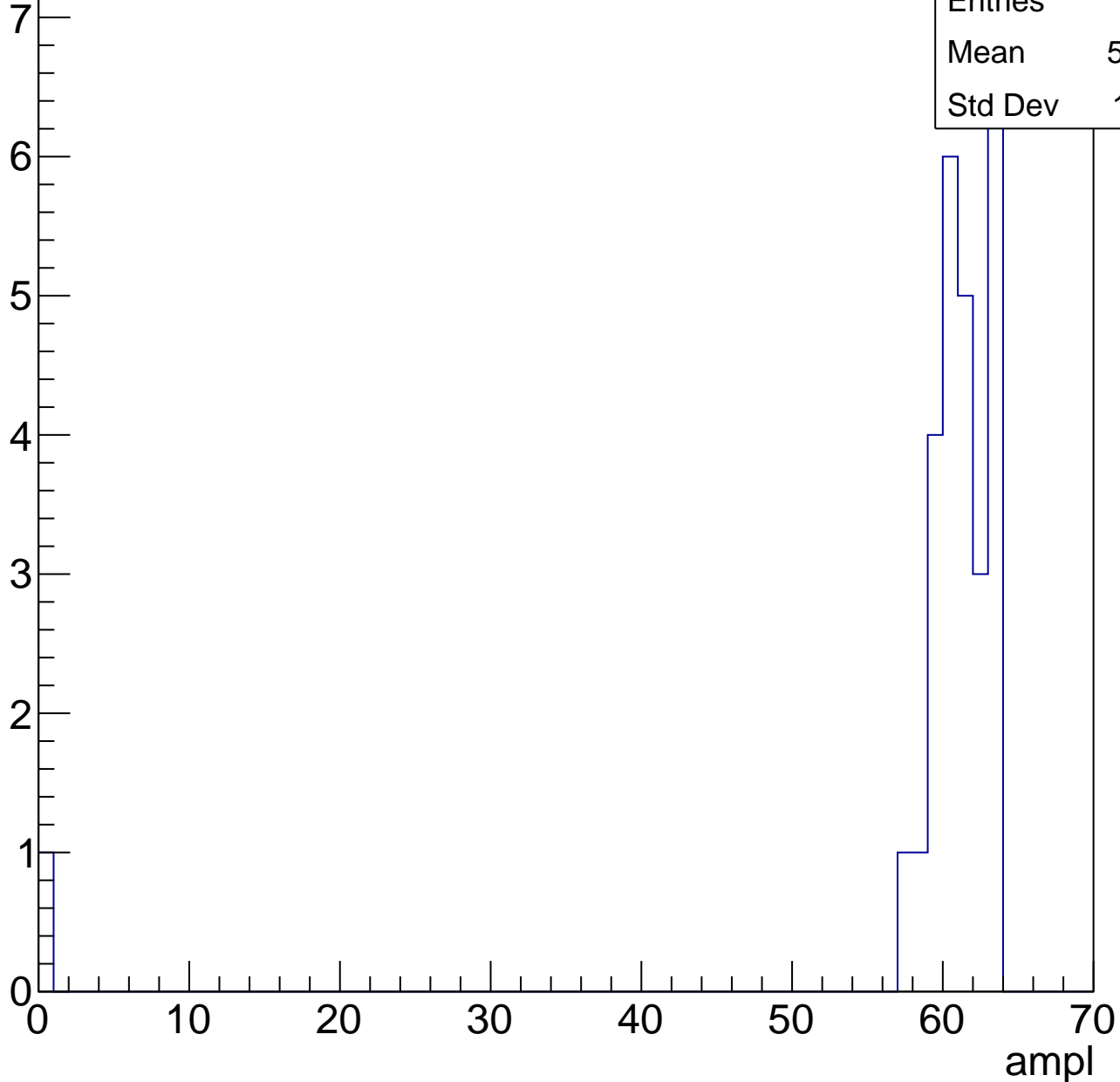


# B0L001S, U5-ch101, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	28
Mean	58.68
Std Dev	11.41



# B0L001S, U5-ch101, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.67
Std Dev	0.4714

ampl

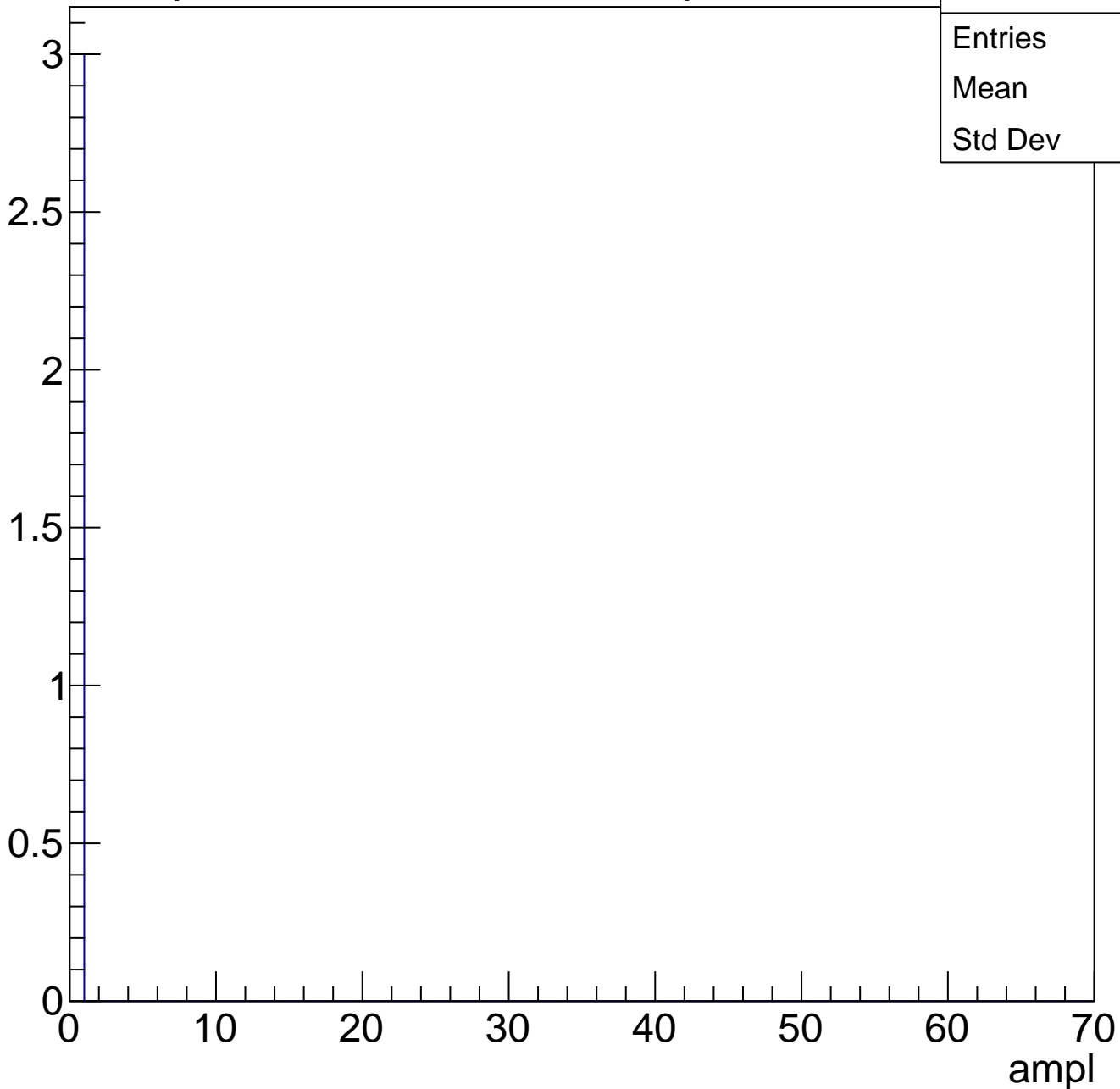
0 10 20 30 40 50 60 70



# B0L001S, U5-ch101, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	3
Mean	0
Std Dev	0

# B0L001S, U5-ch102, adc0

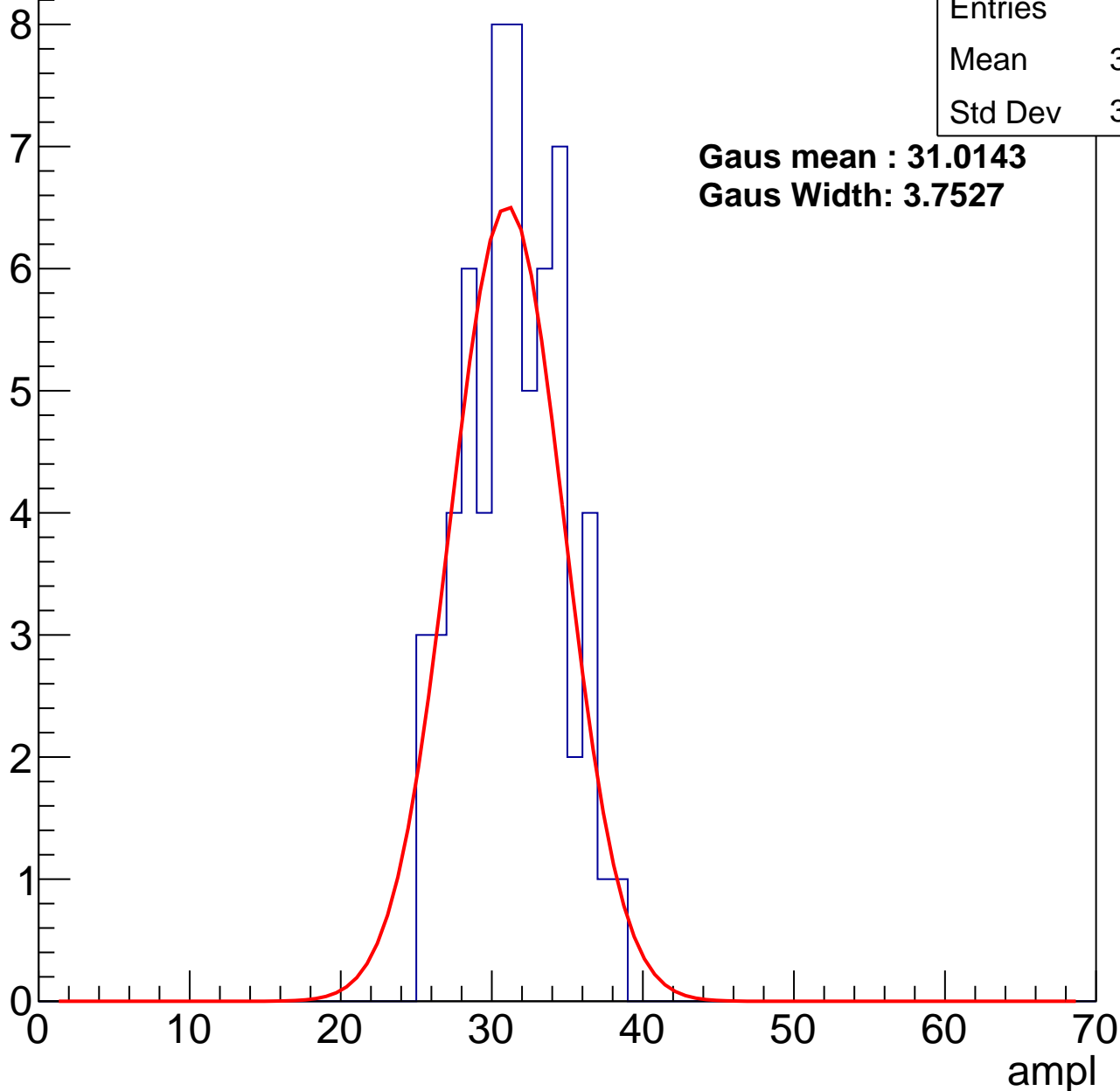
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	30.94
Std Dev	3.197

**Gaus mean : 31.0143**

**Gaus Width: 3.7527**



# B0L001S, U5-ch102, adc1

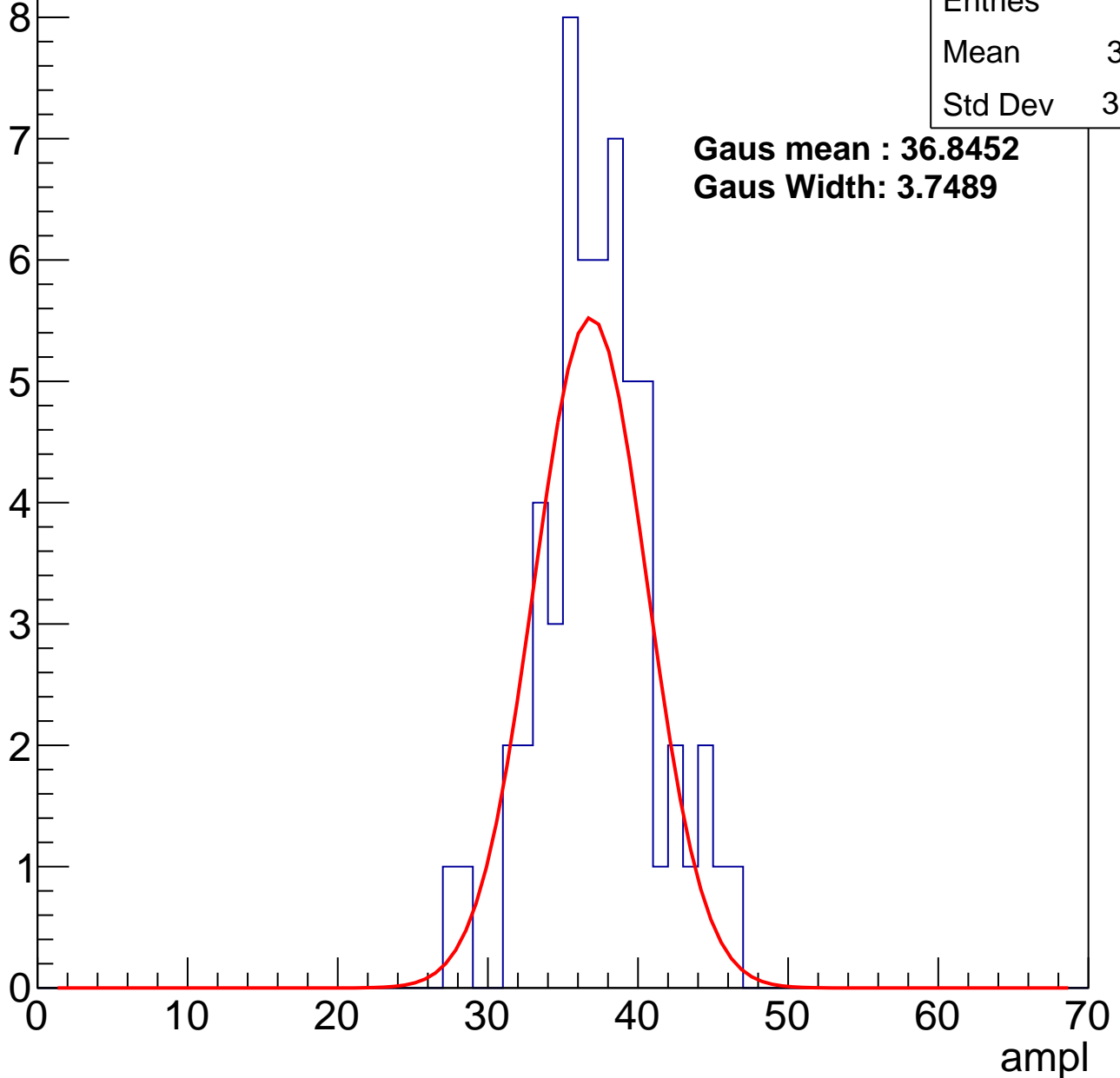
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	36.91
Std Dev	3.825

**Gaus mean : 36.8452**

**Gaus Width: 3.7489**



# B0L001S, U5-ch102, adc2

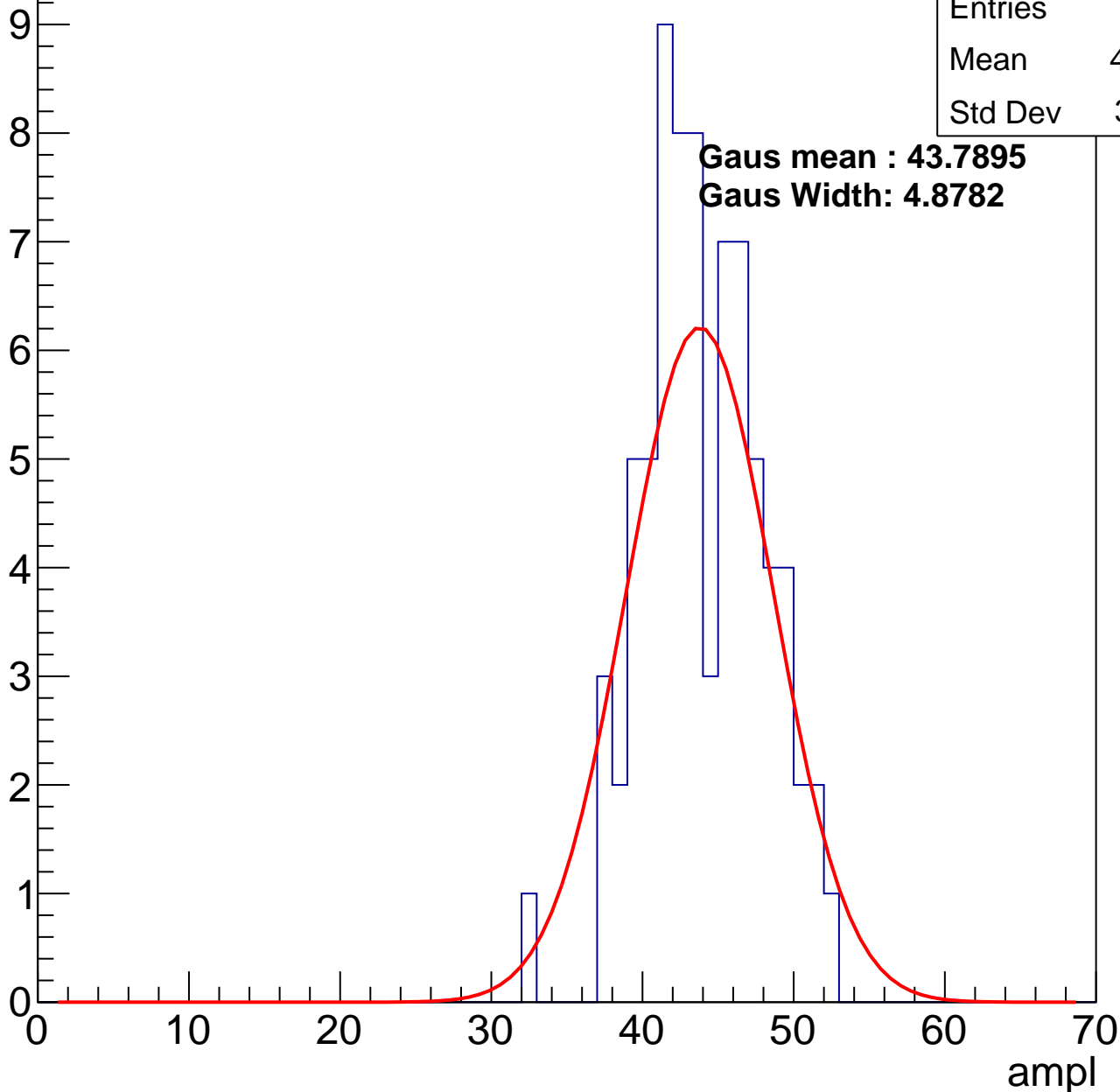
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	76
Mean	43.54
Std Dev	3.891

**Gaus mean : 43.7895**

**Gaus Width: 4.8782**

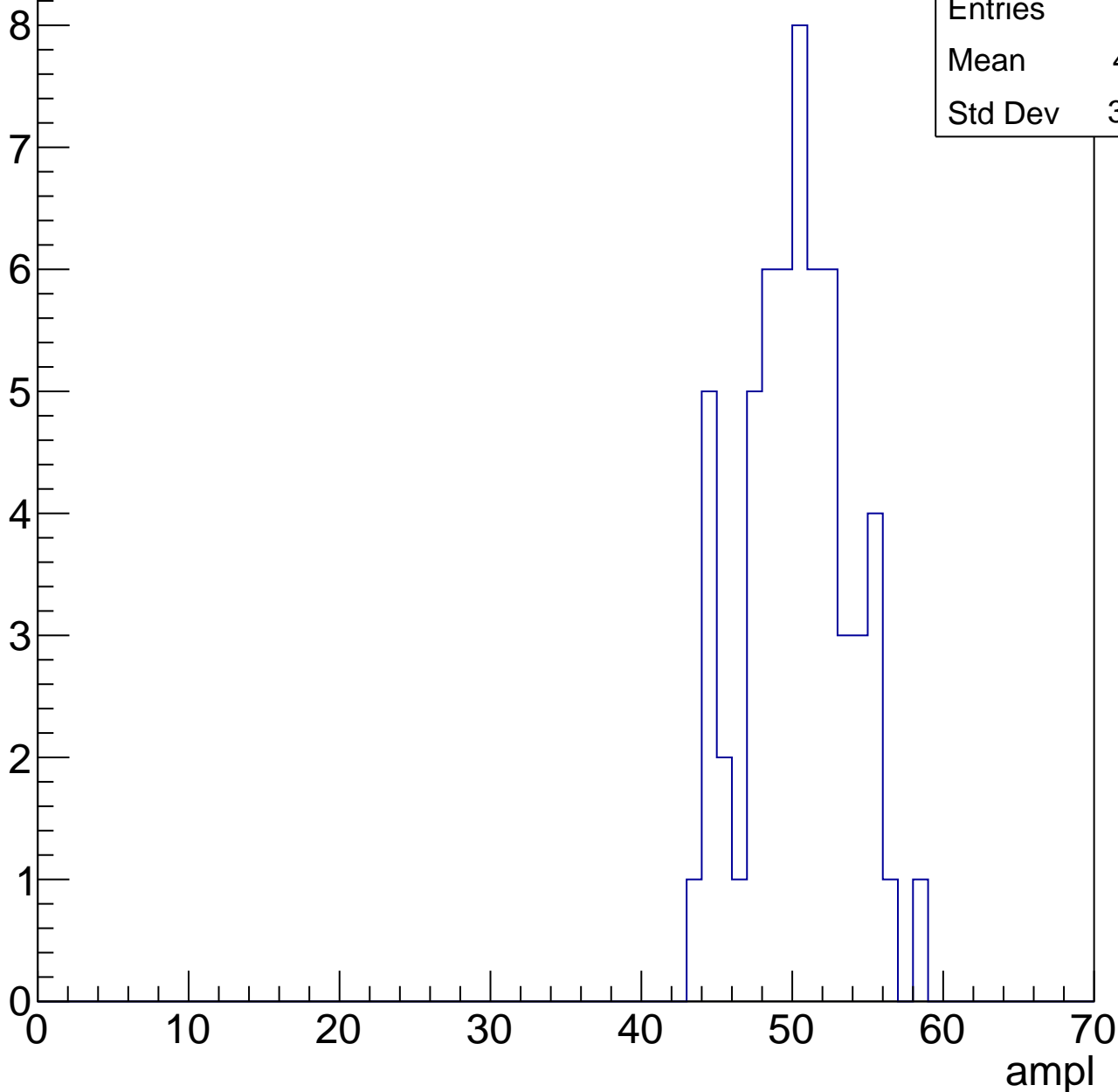


# B0L001S, U5-ch102, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	49.81
Std Dev	3.406

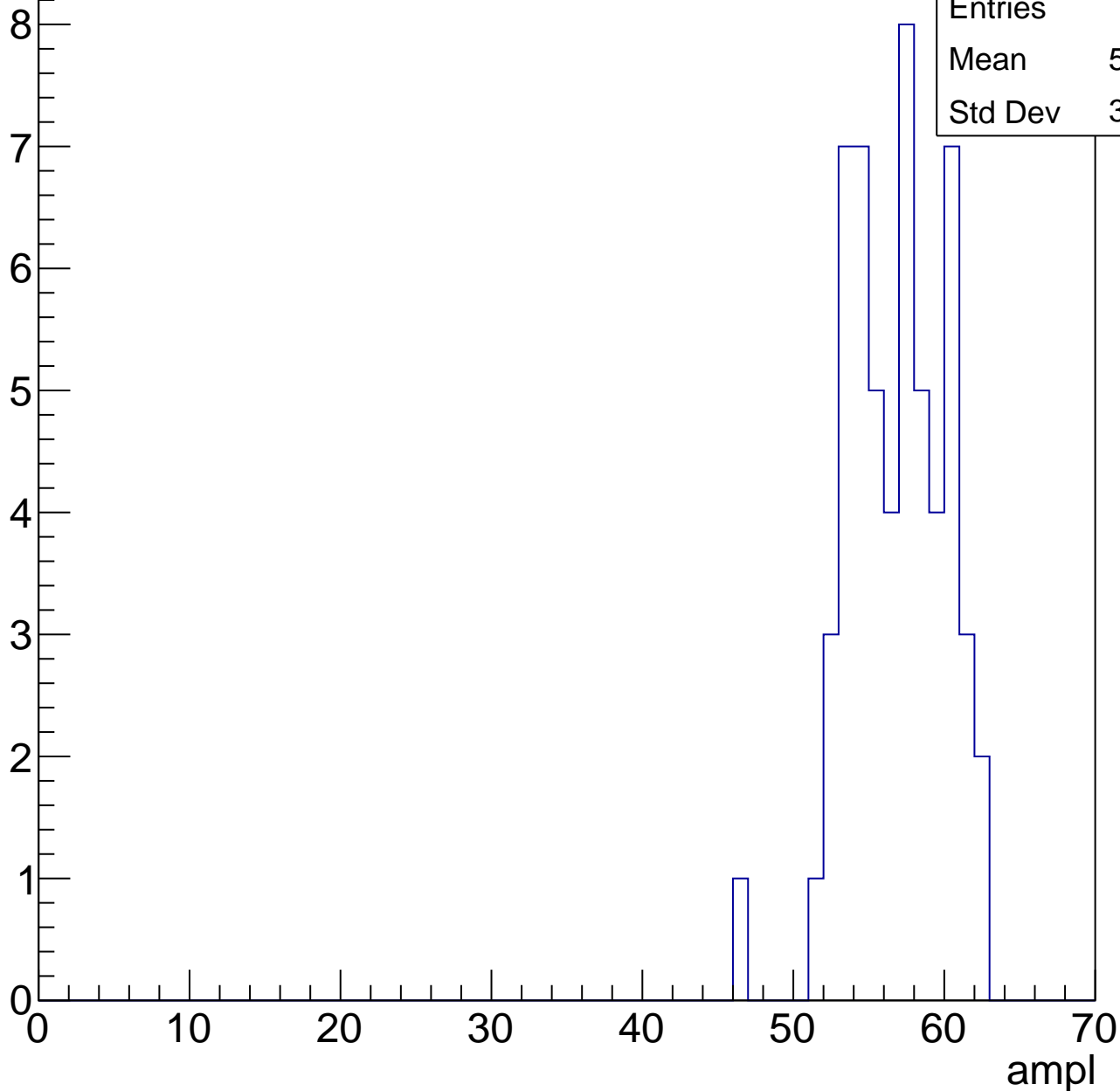


# B0L001S, U5-ch102, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	56.32
Std Dev	3.207

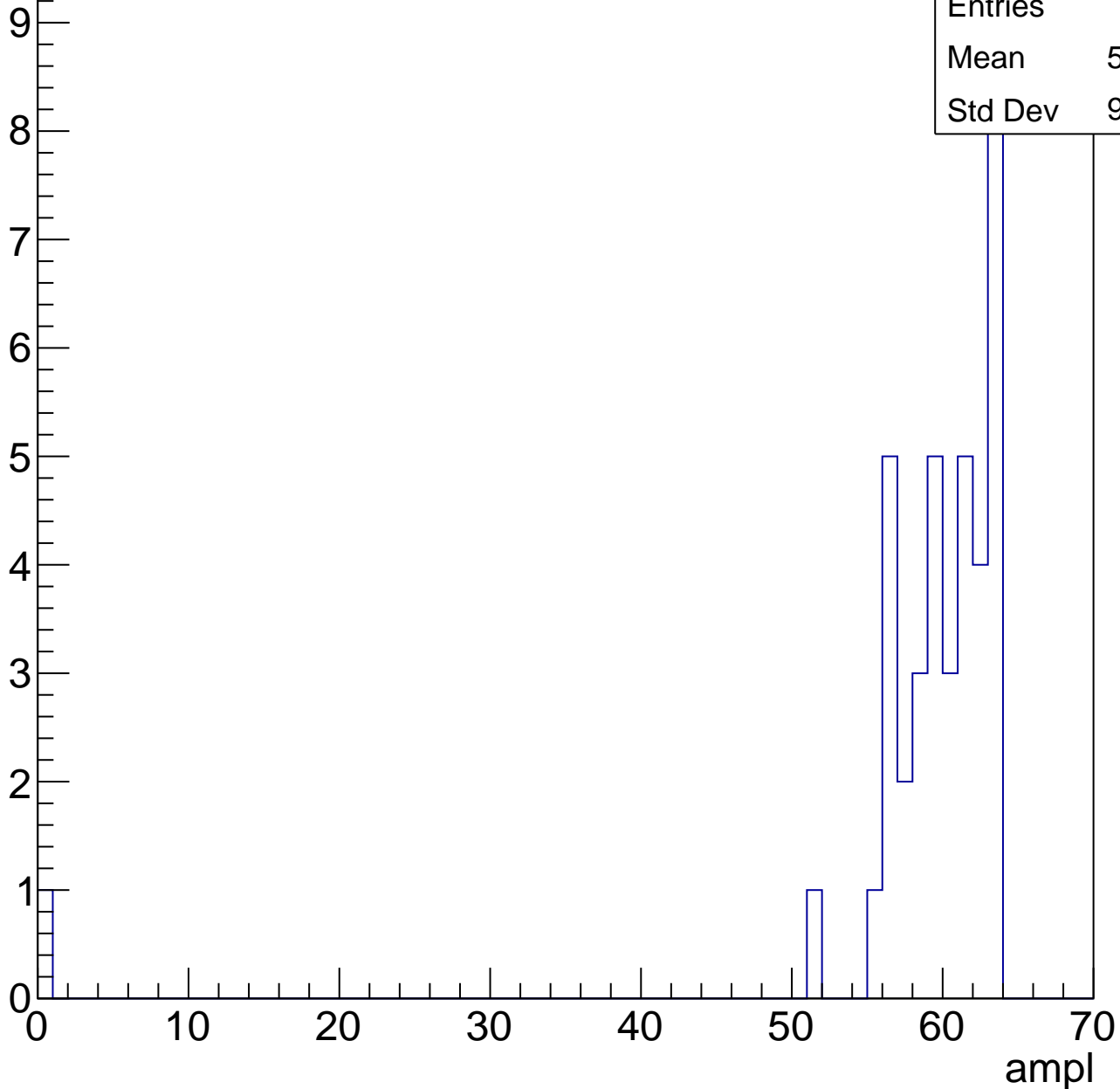


# B0L001S, U5-ch102, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

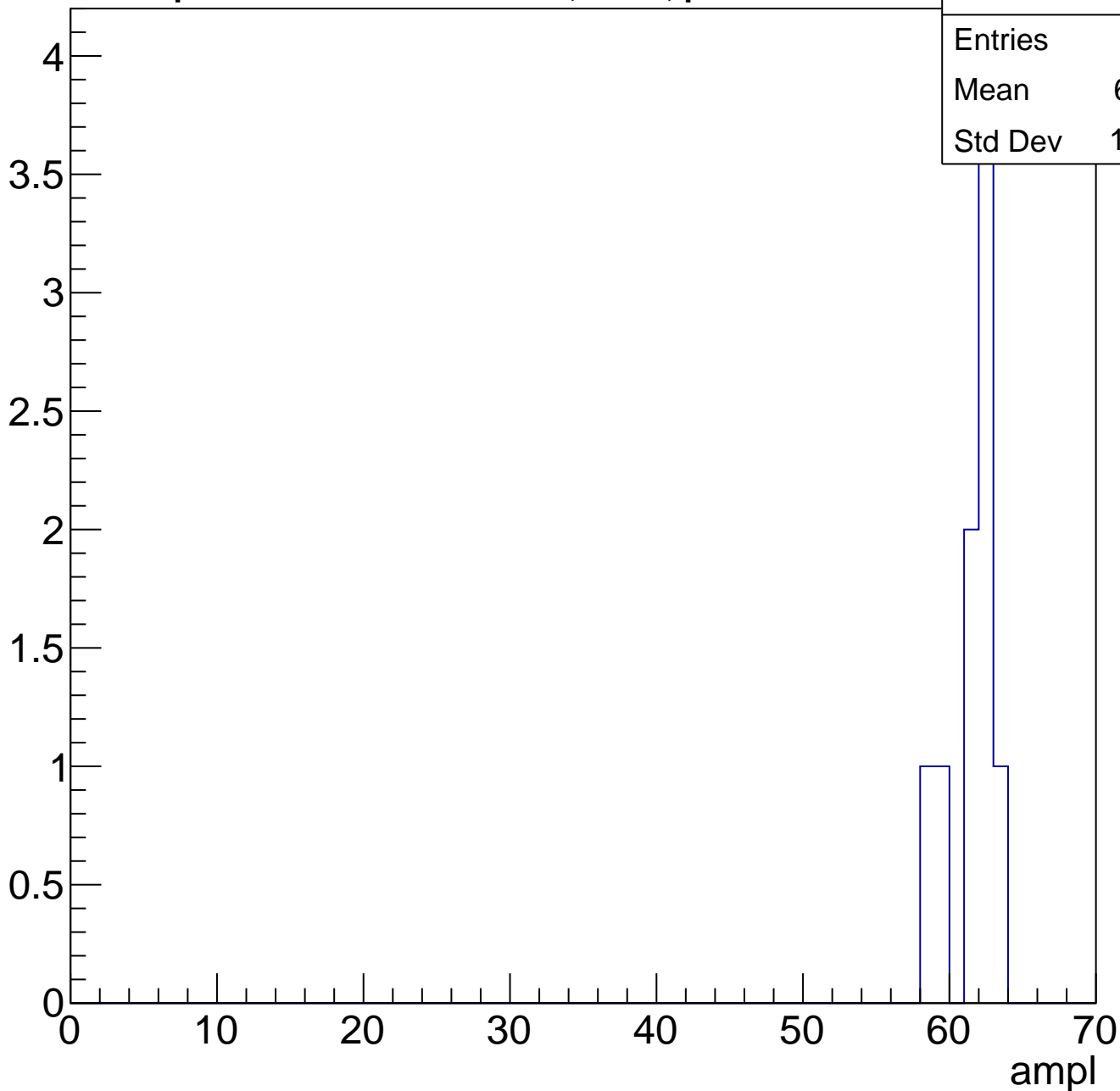
Entries	39
Mean	58.18
Std Dev	9.863



# B0L001S, U5-ch102, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch102, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	23
Std Dev	0

# B0L001S, U5-ch103, adc0

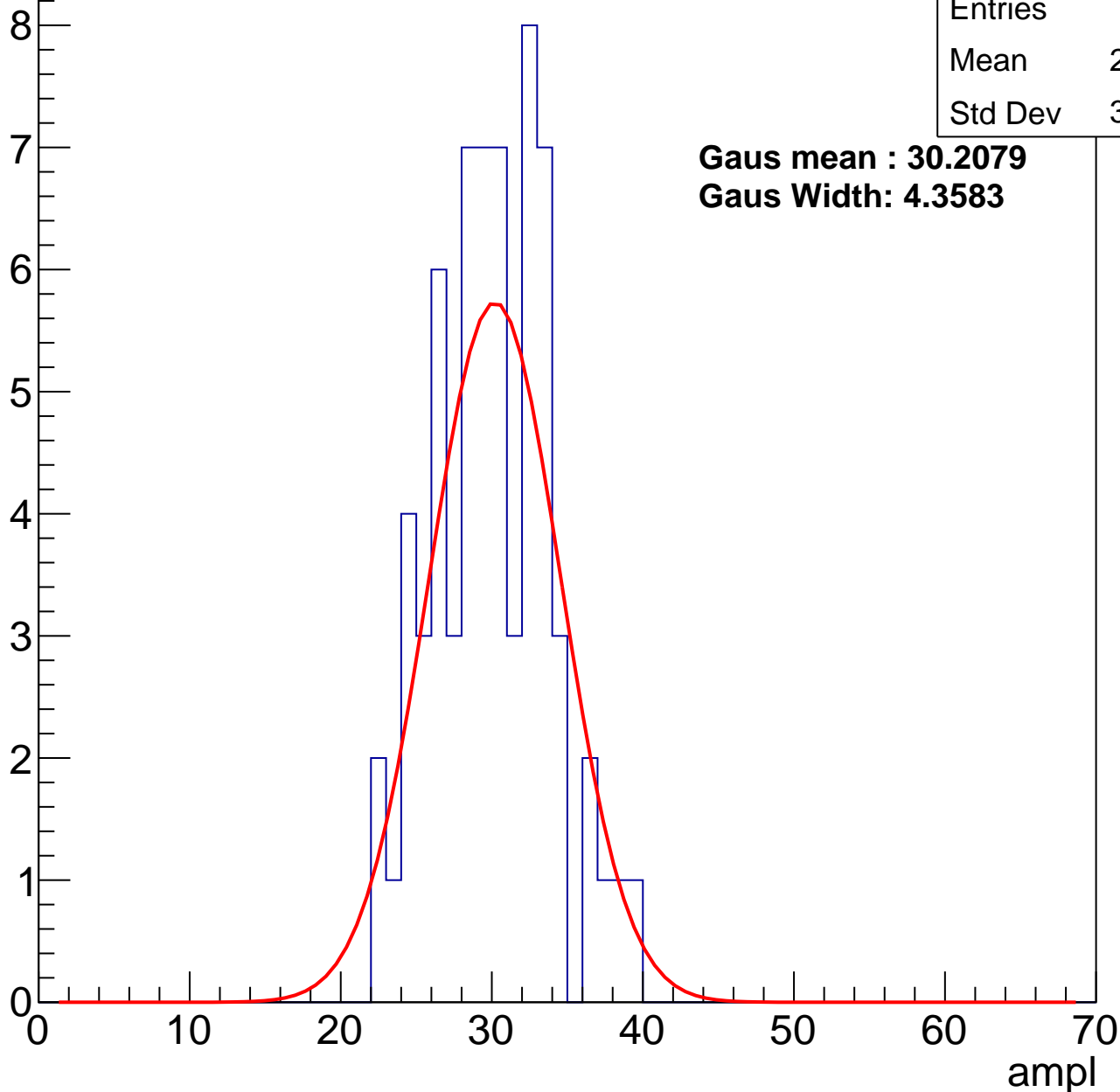
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	29.58
Std Dev	3.802

**Gaus mean : 30.2079**

**Gaus Width: 4.3583**



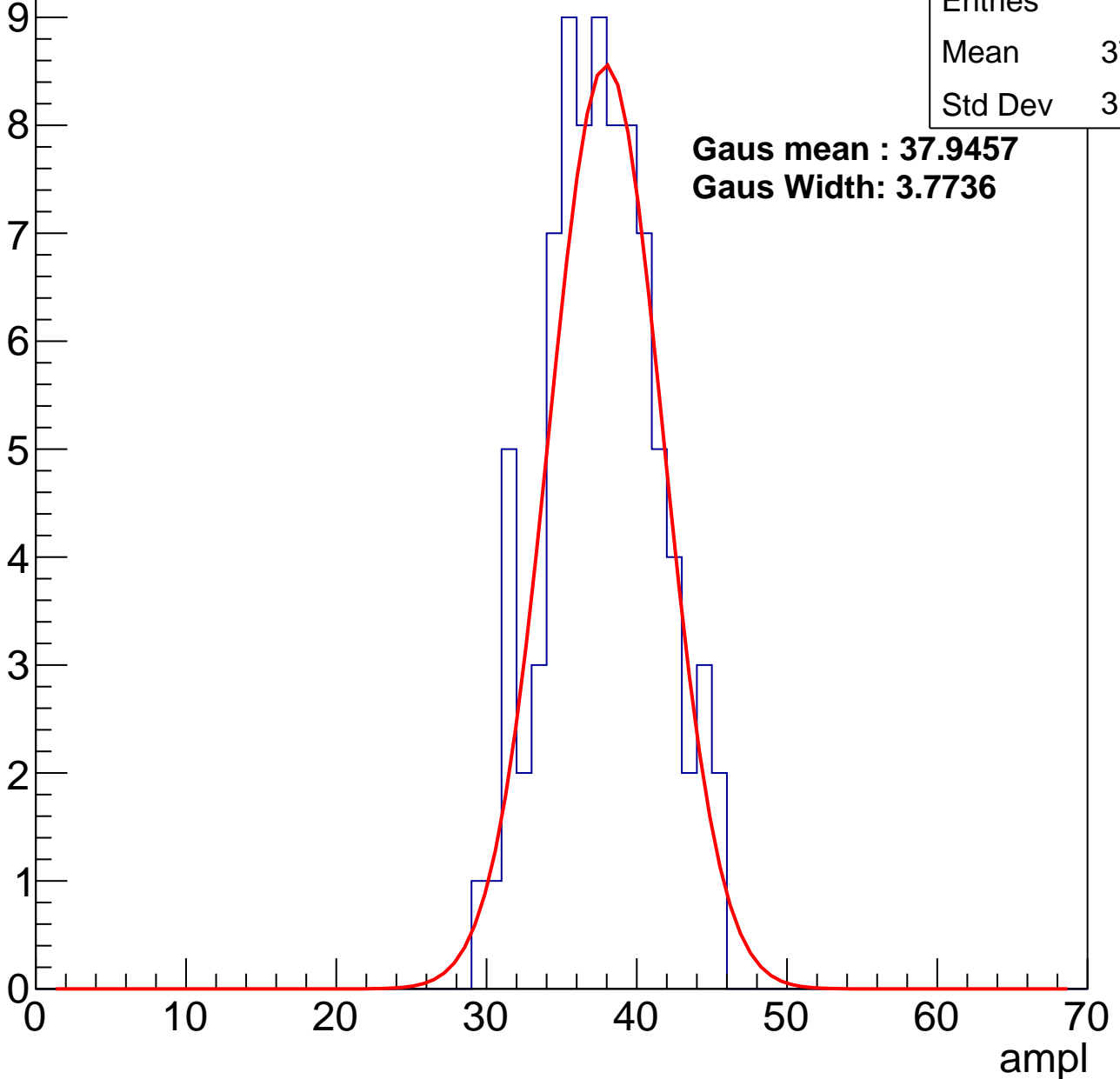
# B0L001S, U5-ch103, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	84
Mean	37.24
Std Dev	3.657

**Gaus mean : 37.9457**  
**Gaus Width: 3.7736**



# B0L001S, U5-ch103, adc2

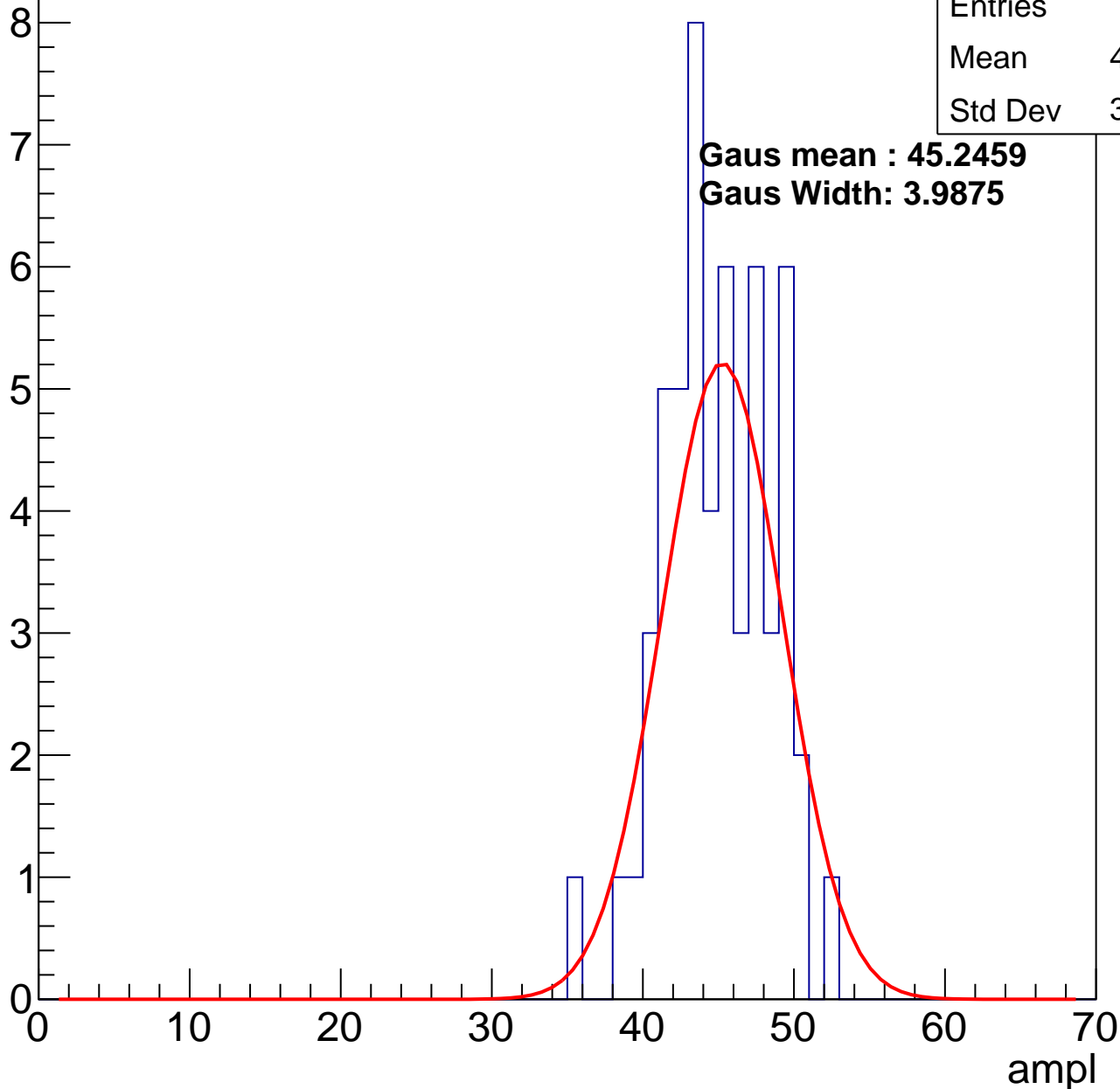
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	44.49
Std Dev	3.453

**Gaus mean : 45.2459**

**Gaus Width: 3.9875**

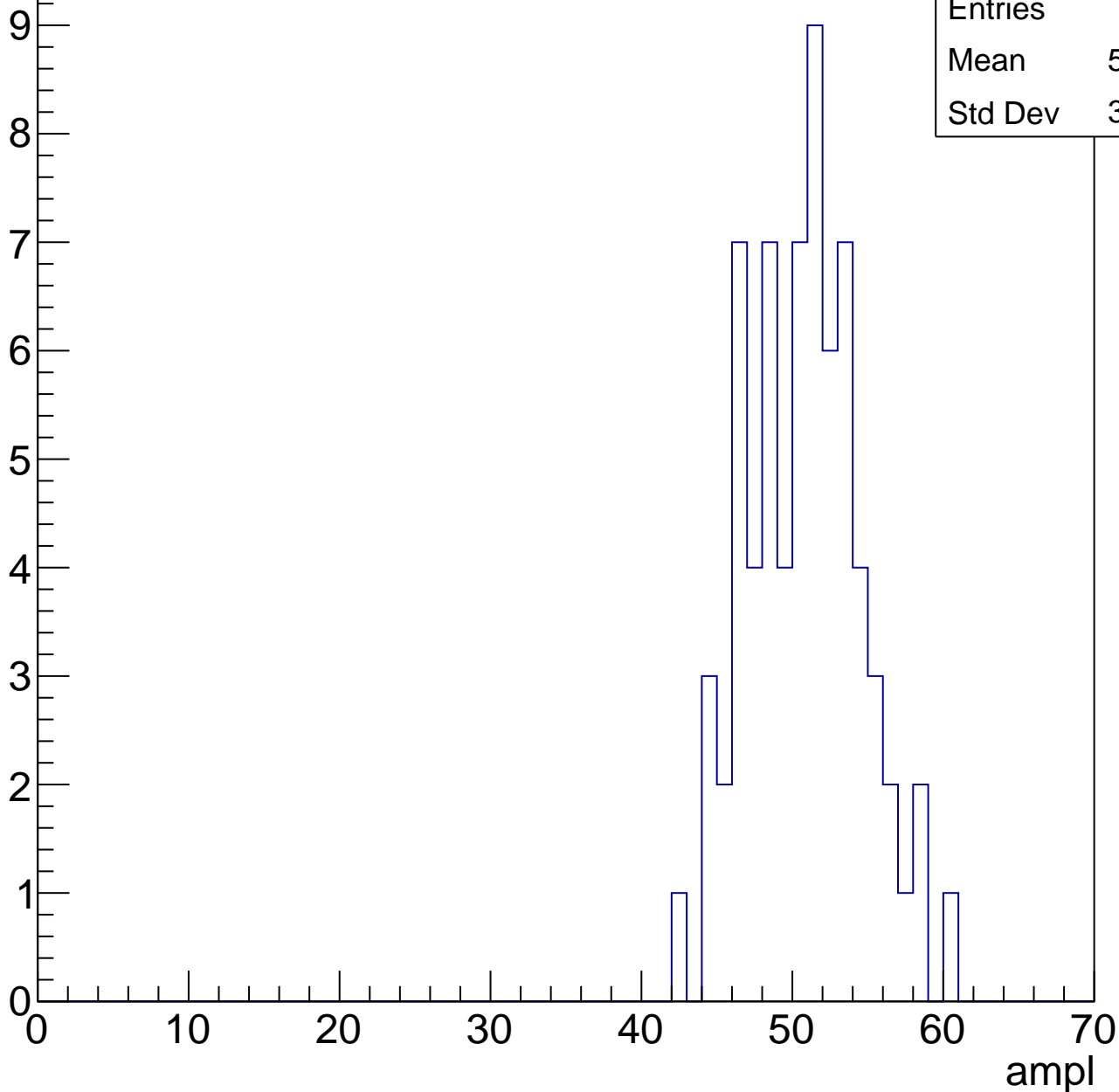


# B0L001S, U5-ch103, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	50.34
Std Dev	3.737

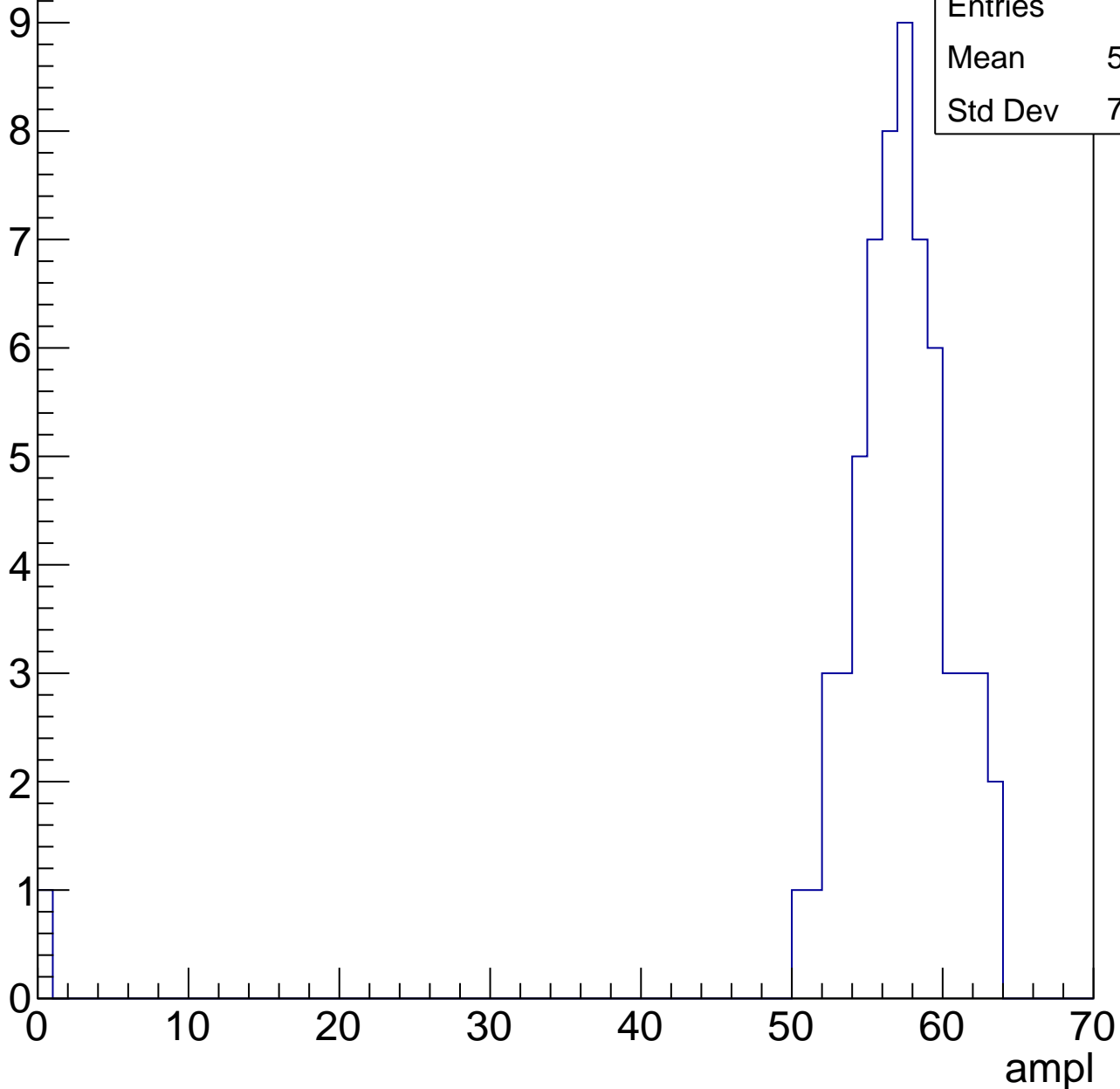


# B0L001S, U5-ch103, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	55.92
Std Dev	7.745

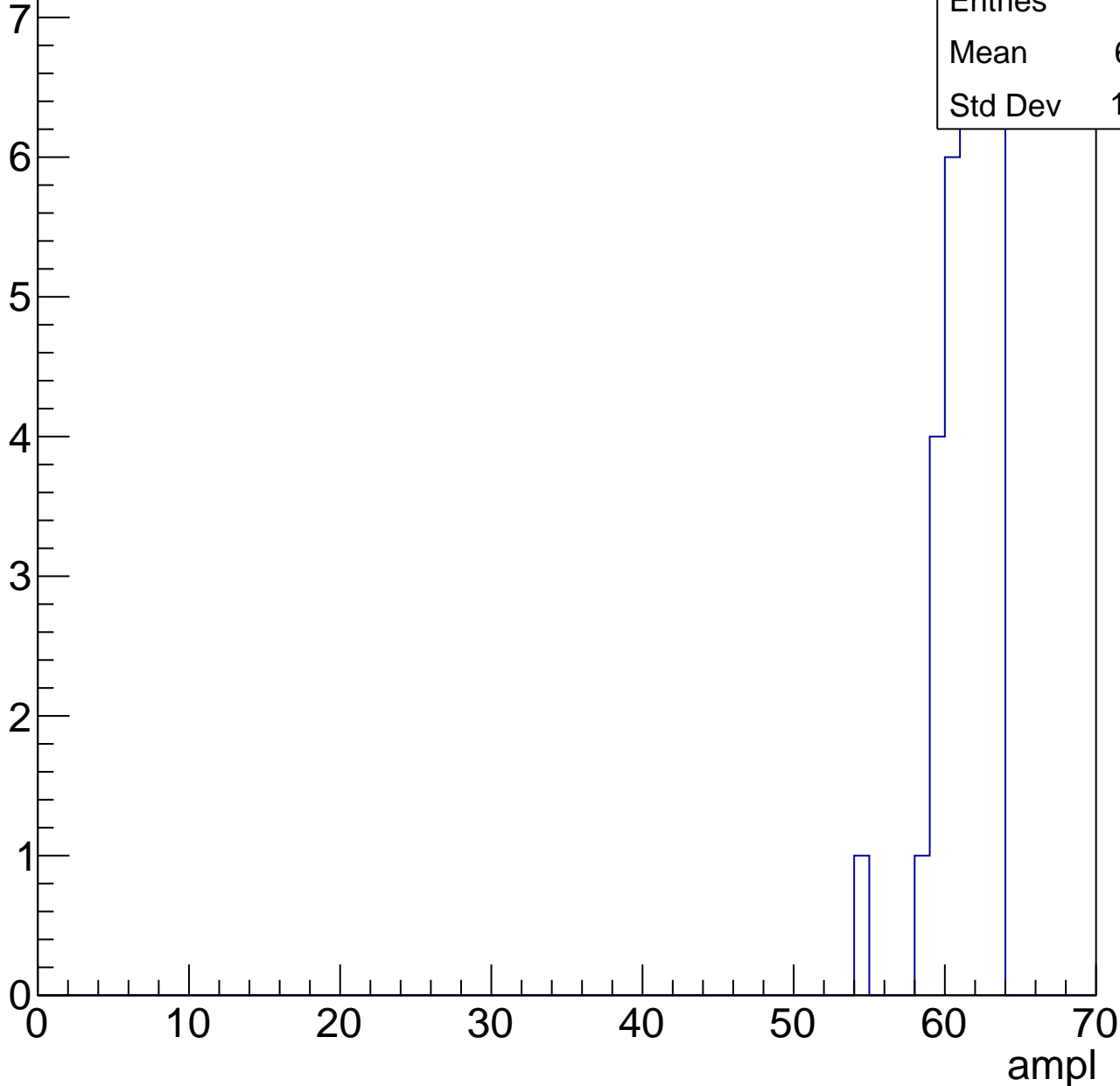


# B0L001S, U5-ch103, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	33
Mean	60.91
Std Dev	1.865



# B0L001S, U5-ch103, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch103, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U5-ch104, adc0

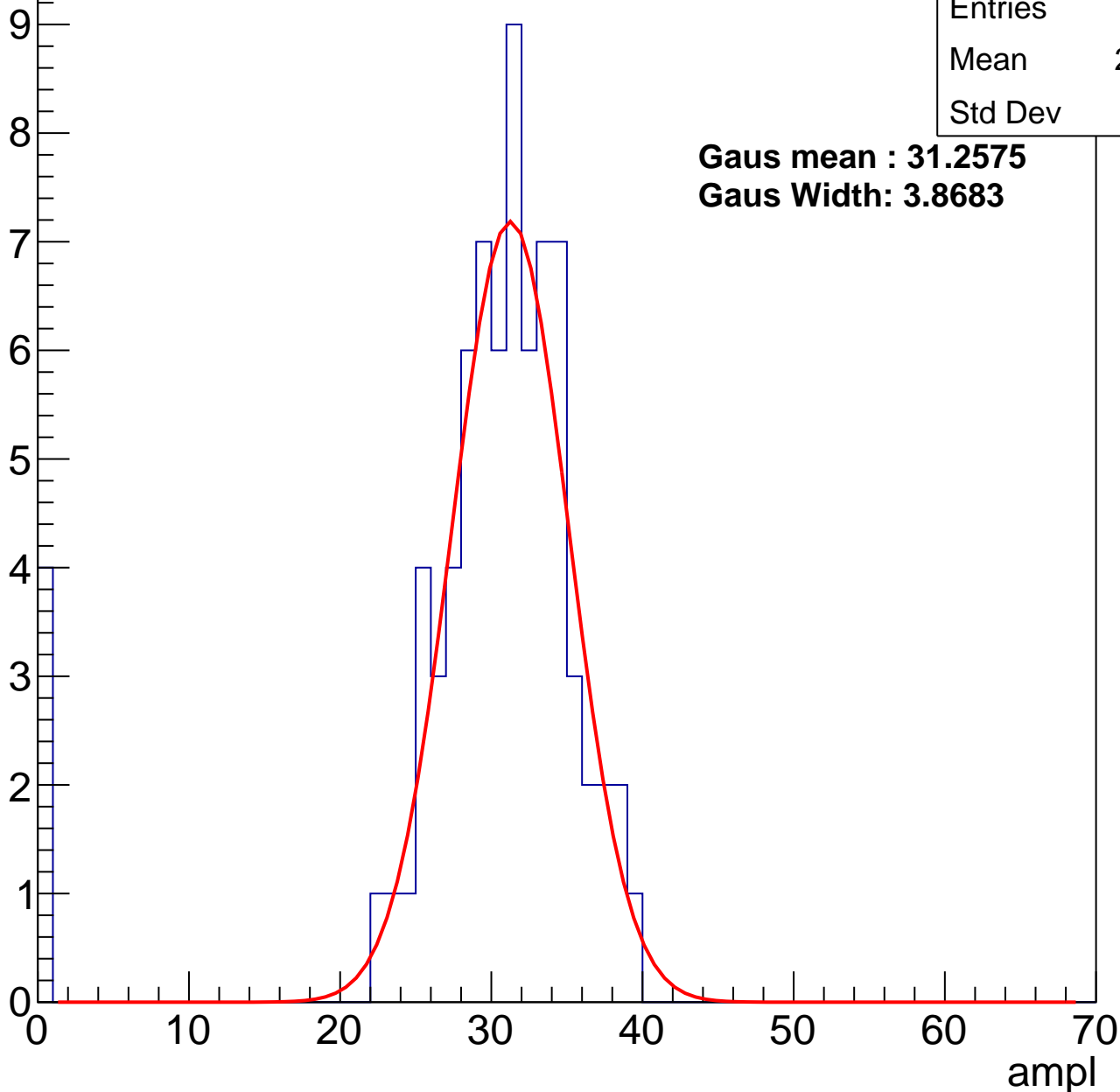
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	76
Mean	29.11
Std Dev	7.75

**Gaus mean : 31.2575**

**Gaus Width: 3.8683**



# B0L001S, U5-ch104, adc1

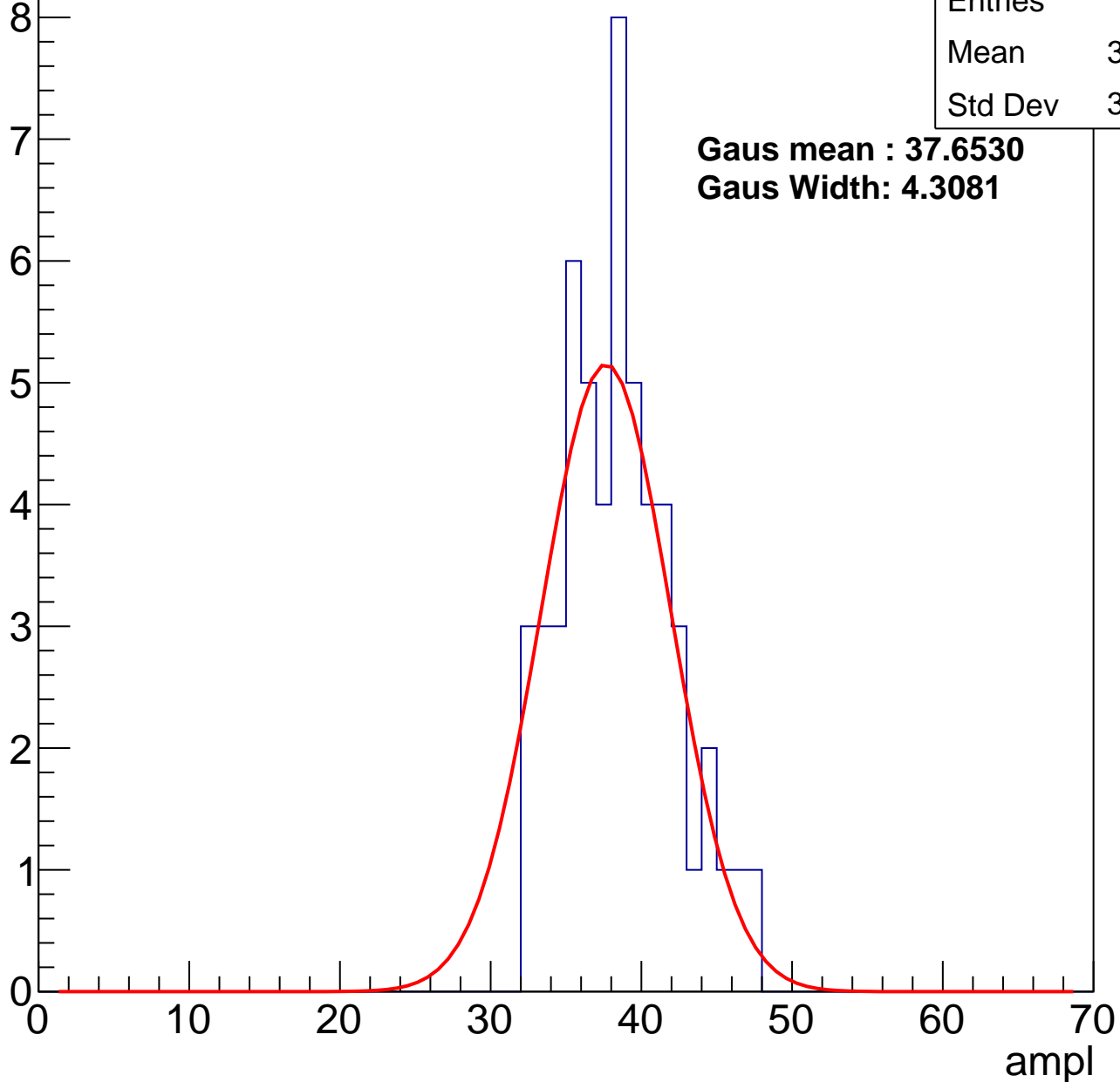
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	38.02
Std Dev	3.613

**Gaus mean : 37.6530**

**Gaus Width: 4.3081**



# B0L001S, U5-ch104, adc2

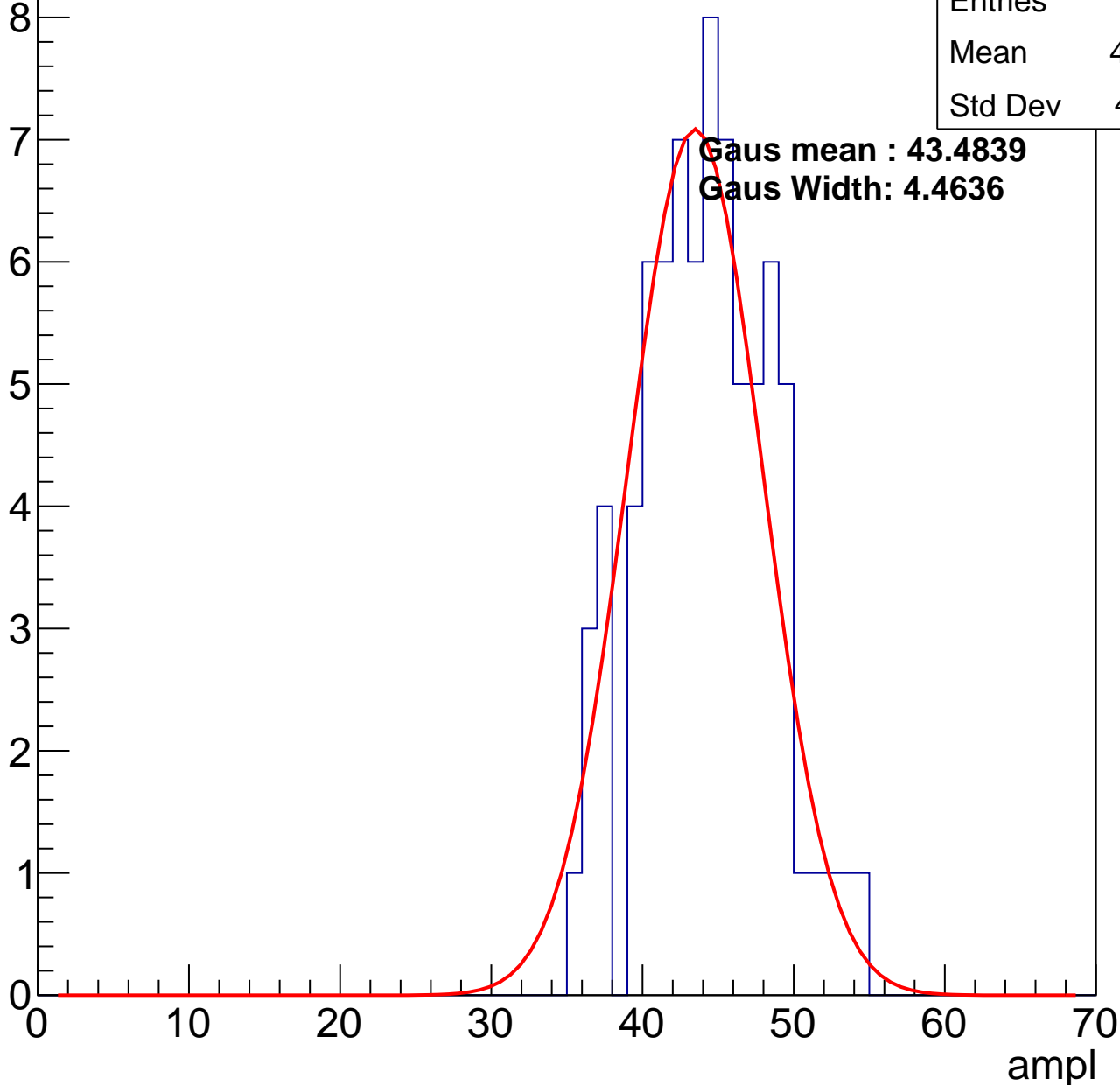
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	78
Mean	43.72
Std Dev	4.191

**Gaus mean : 43.4839**

**Gaus Width: 4.4636**

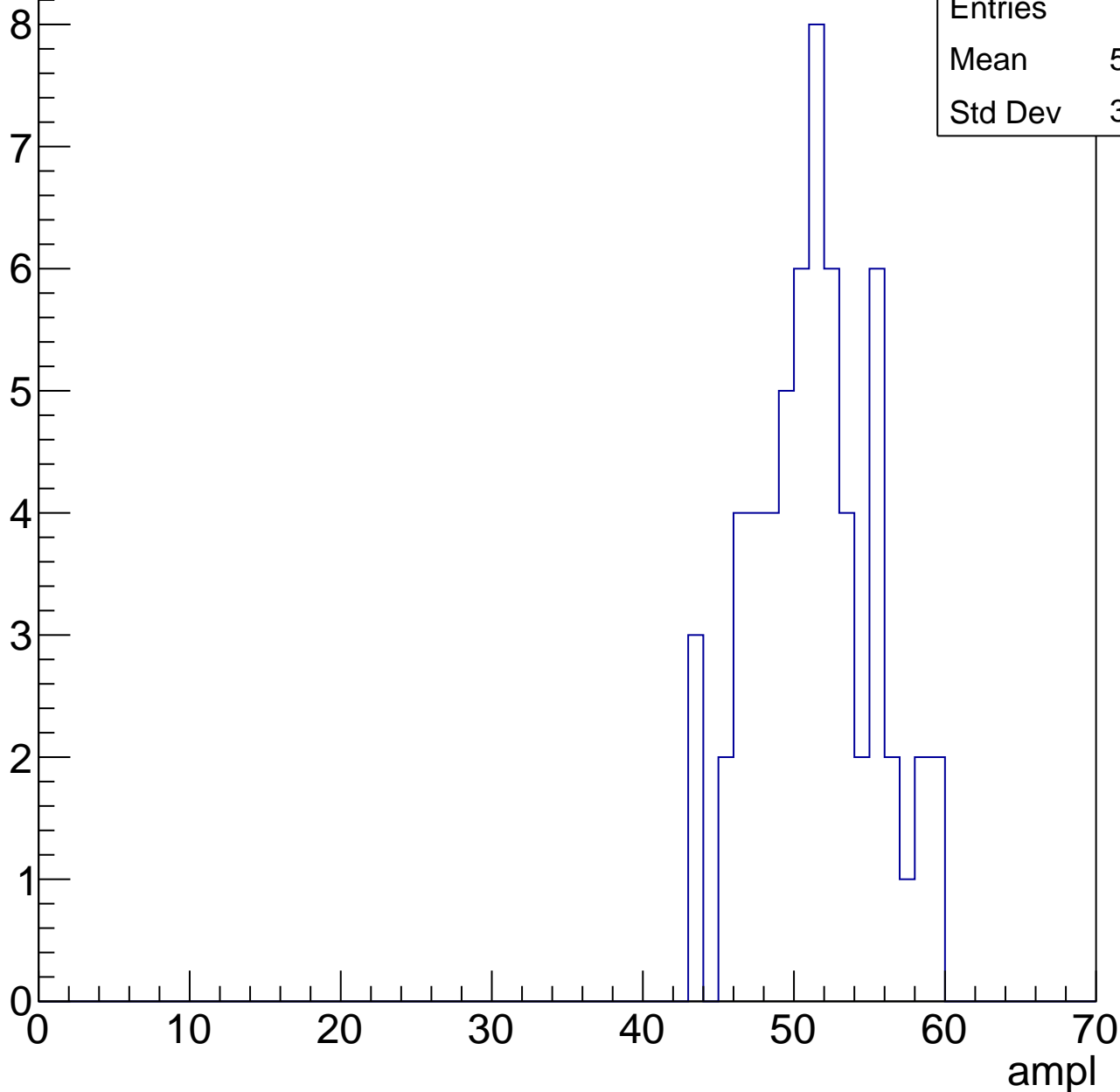


# B0L001S, U5-ch104, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

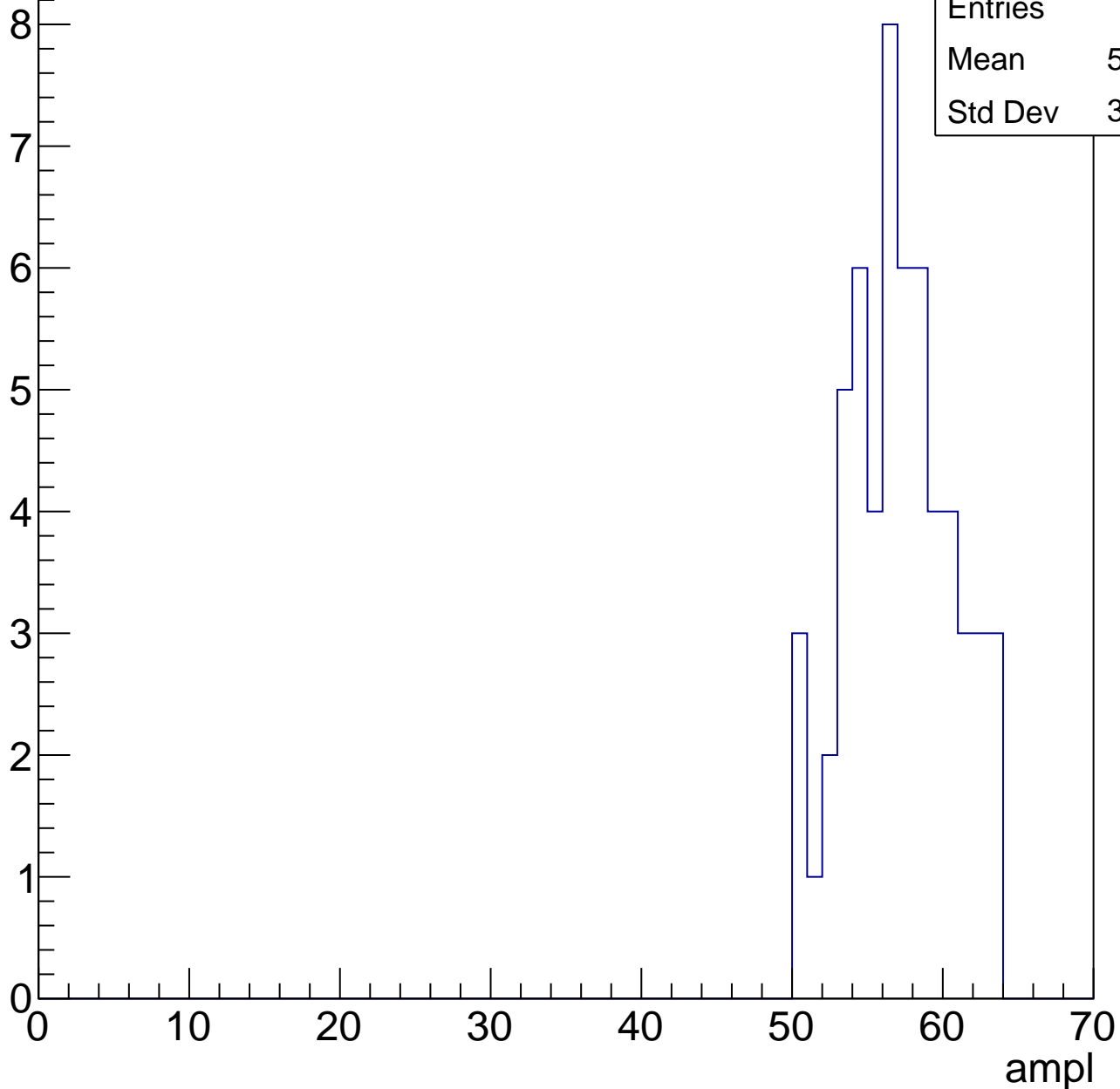
Entries	61
Mean	50.84
Std Dev	3.918



# B0L001S, U5-ch104, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

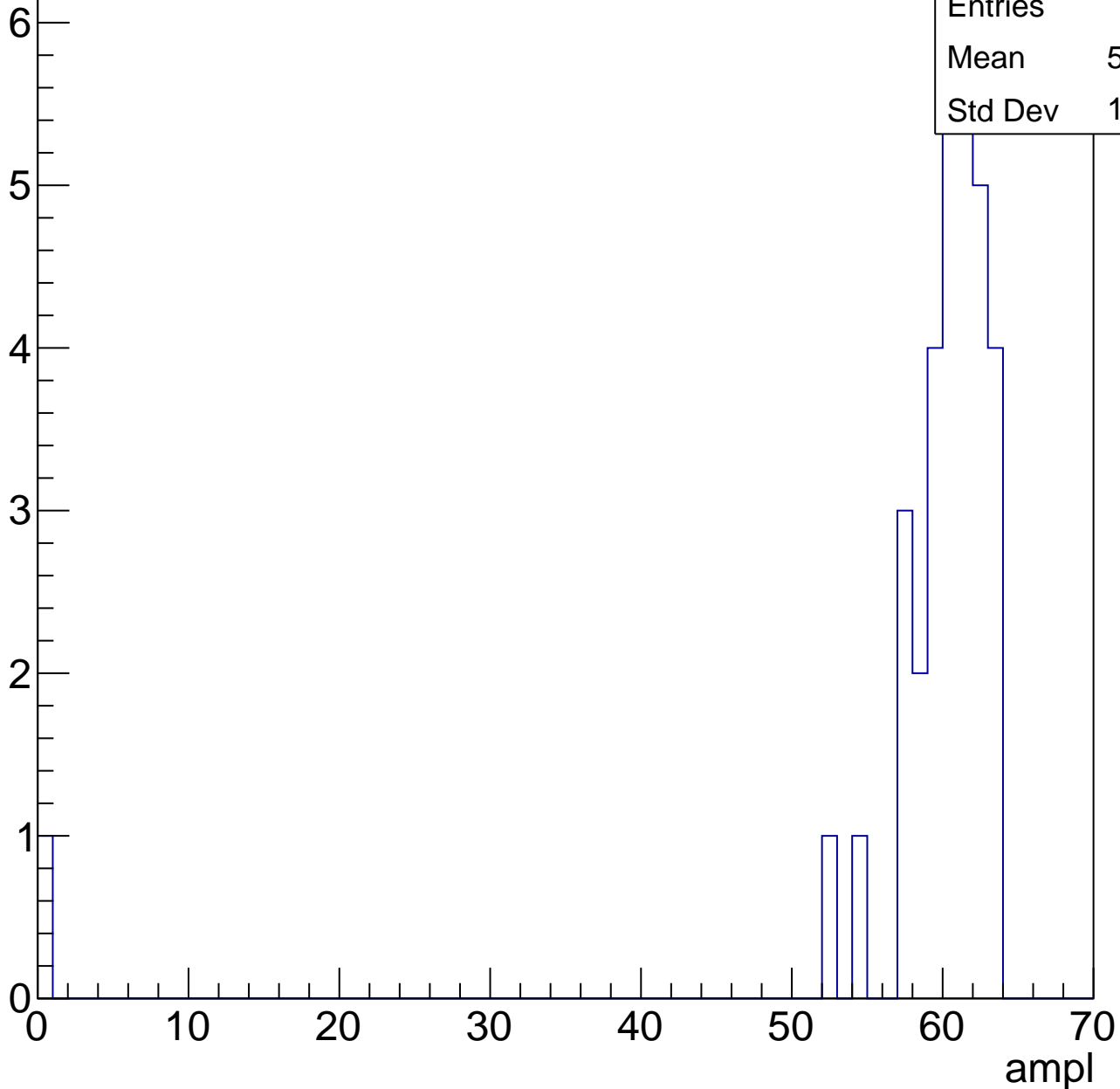


# B0L001S, U5-ch104, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	33
Mean	58.09
Std Dev	10.56



# B0L001S, U5-ch104, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	6
Mean	62.33
Std Dev	0.7454



# B0L001S, U5-ch104, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch105, adc0

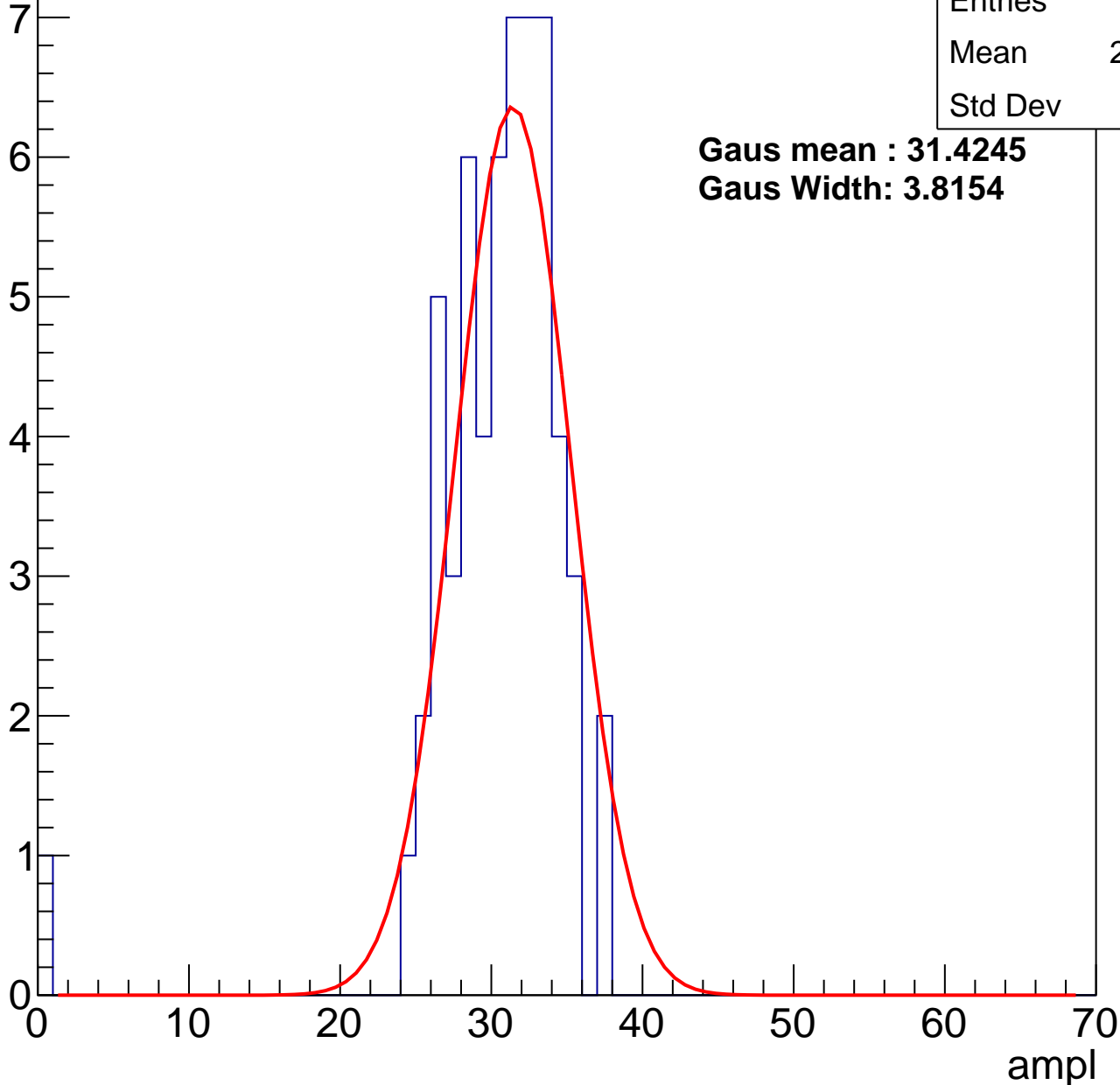
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	29.93
Std Dev	5.01

**Gaus mean : 31.4245**

**Gaus Width: 3.8154**



# B0L001S, U5-ch105, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	67
Mean	37.31
Std Dev	3.891

**Gaus mean : 37.3542**

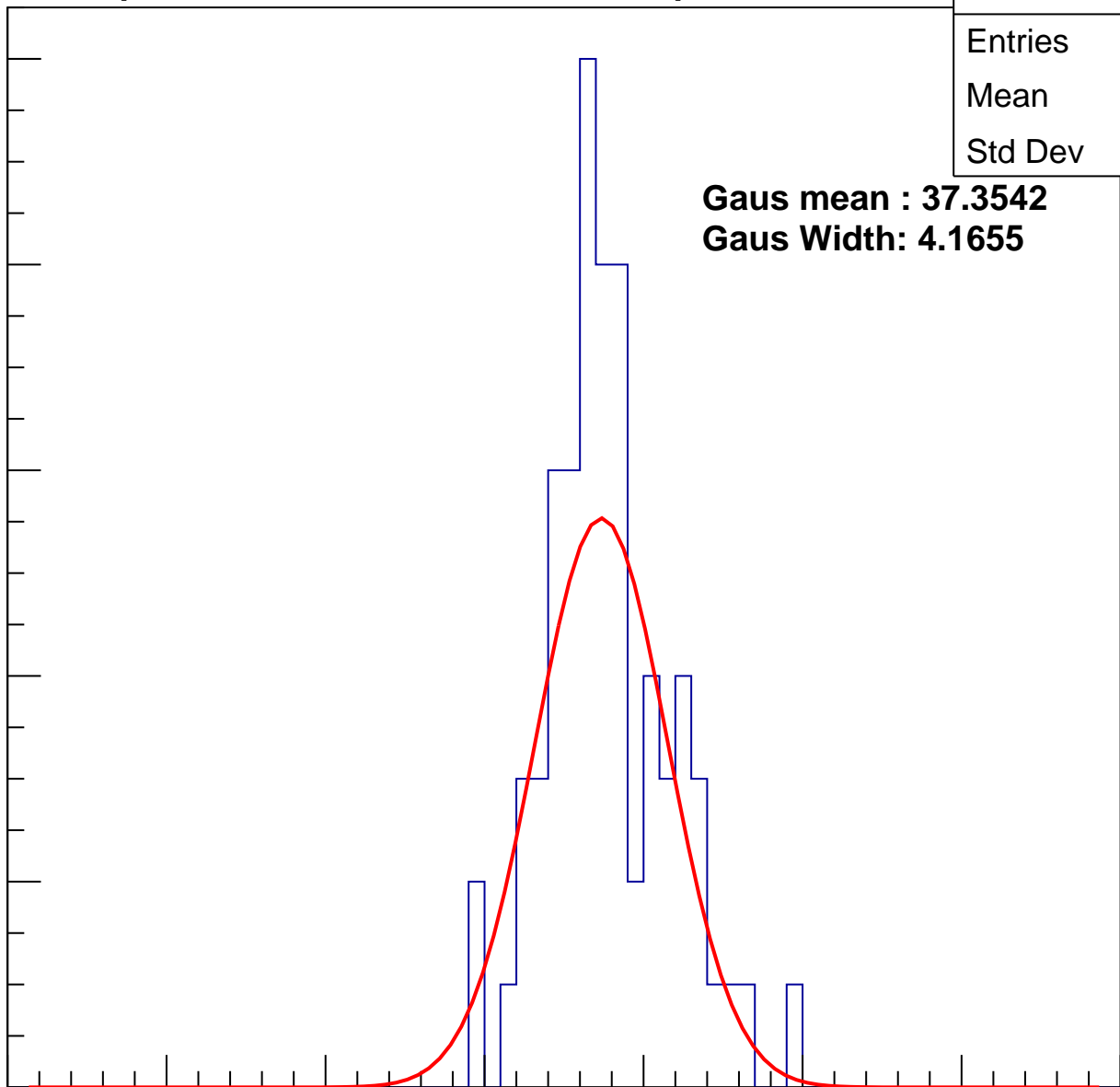
**Gaus Width: 4.1655**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B0L001S, U5-ch105, adc2

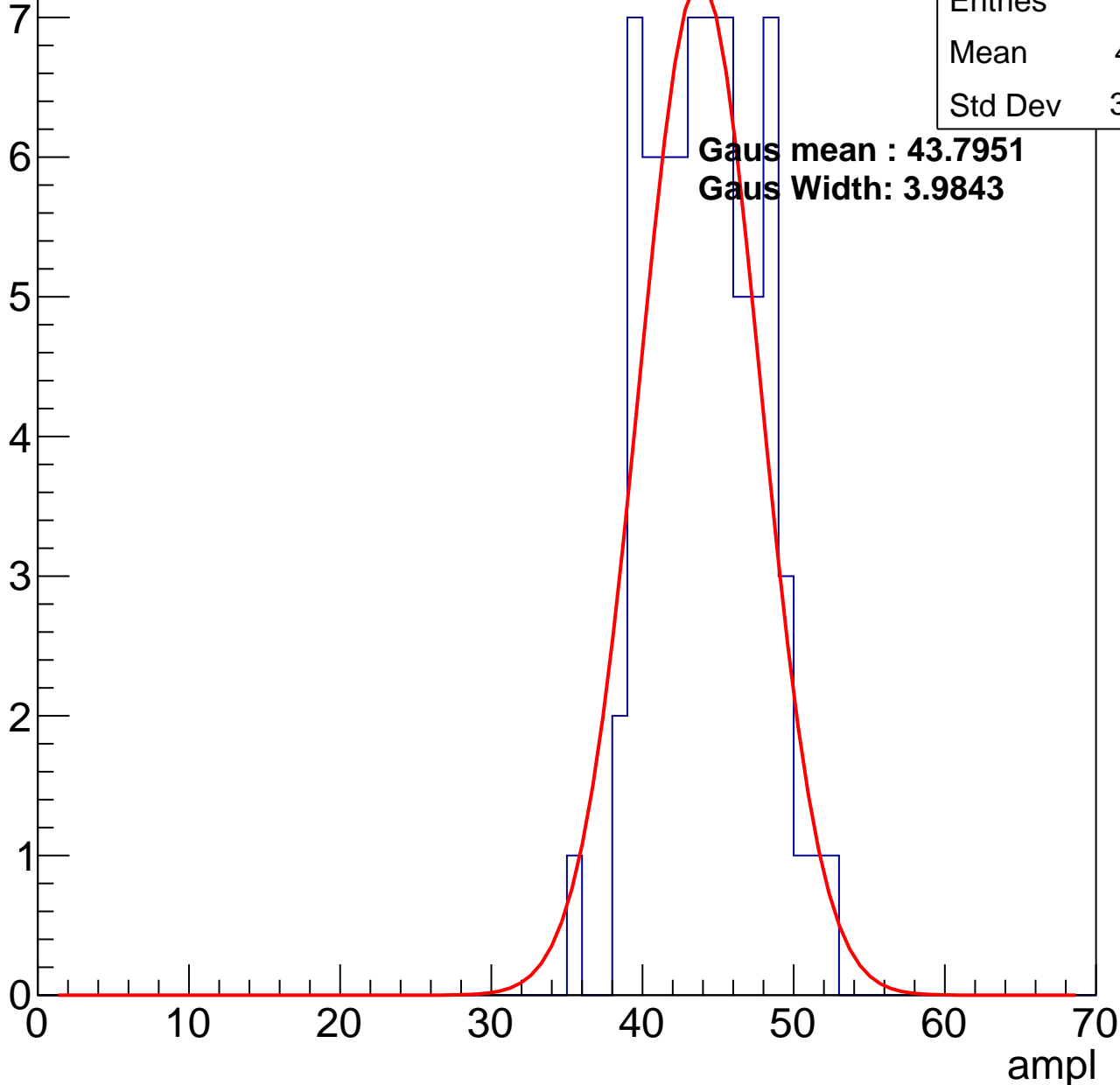
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	43.71
Std Dev	3.557

**Gaus mean : 43.7951**

**Gaus Width: 3.9843**

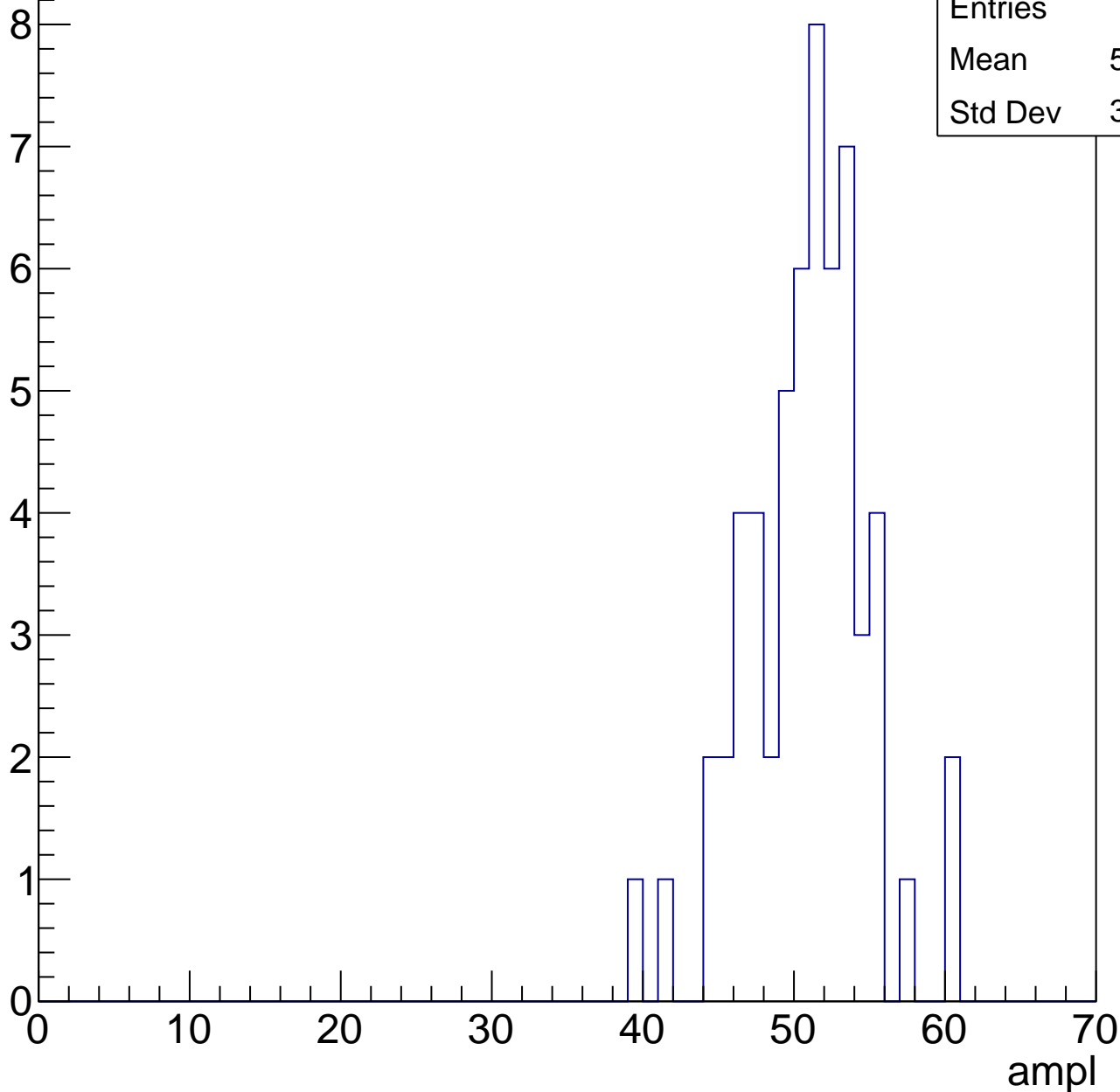


# B0L001S, U5-ch105, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

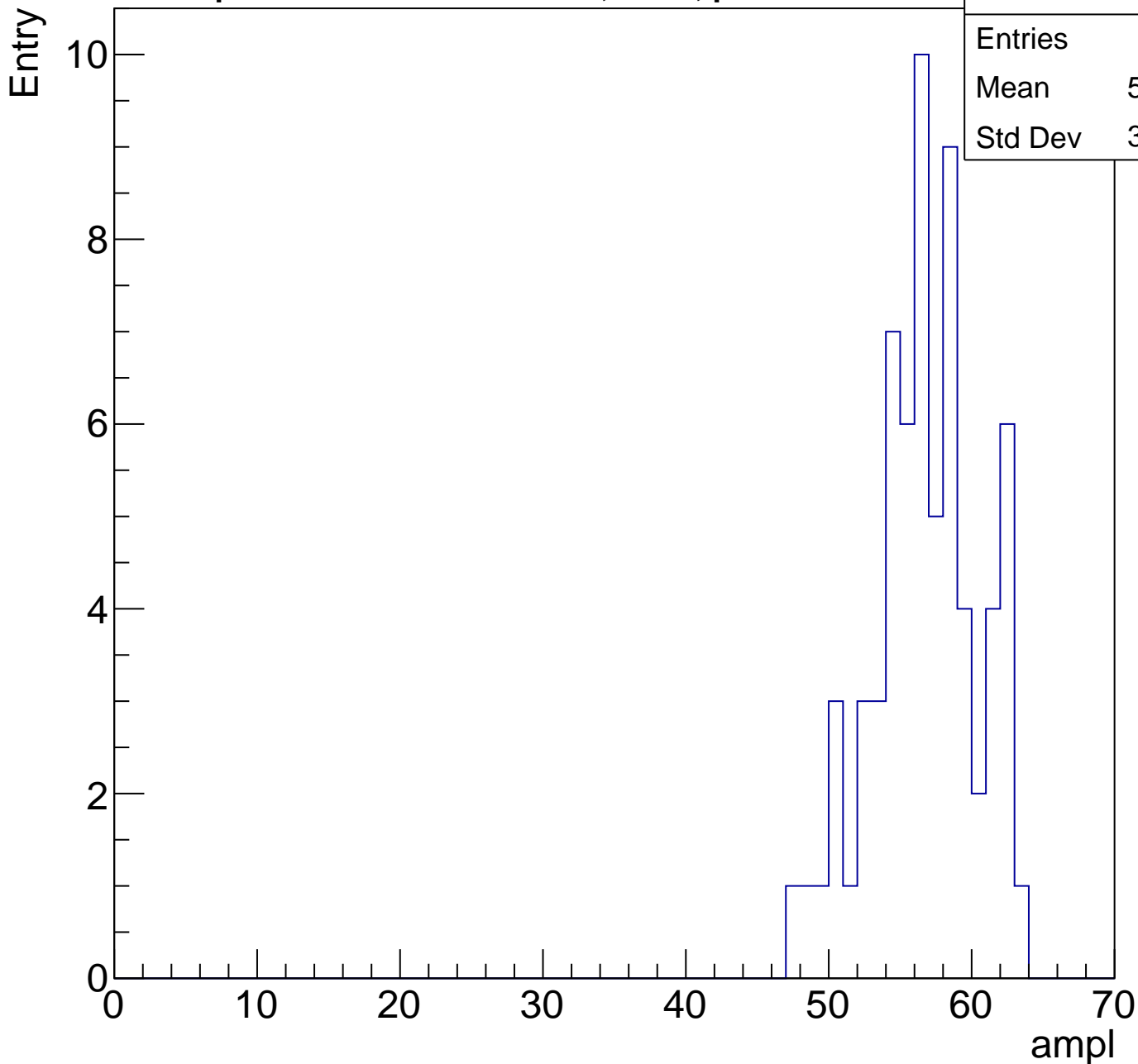
Entries	58
Mean	50.36
Std Dev	3.986



# B0L001S, U5-ch105, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

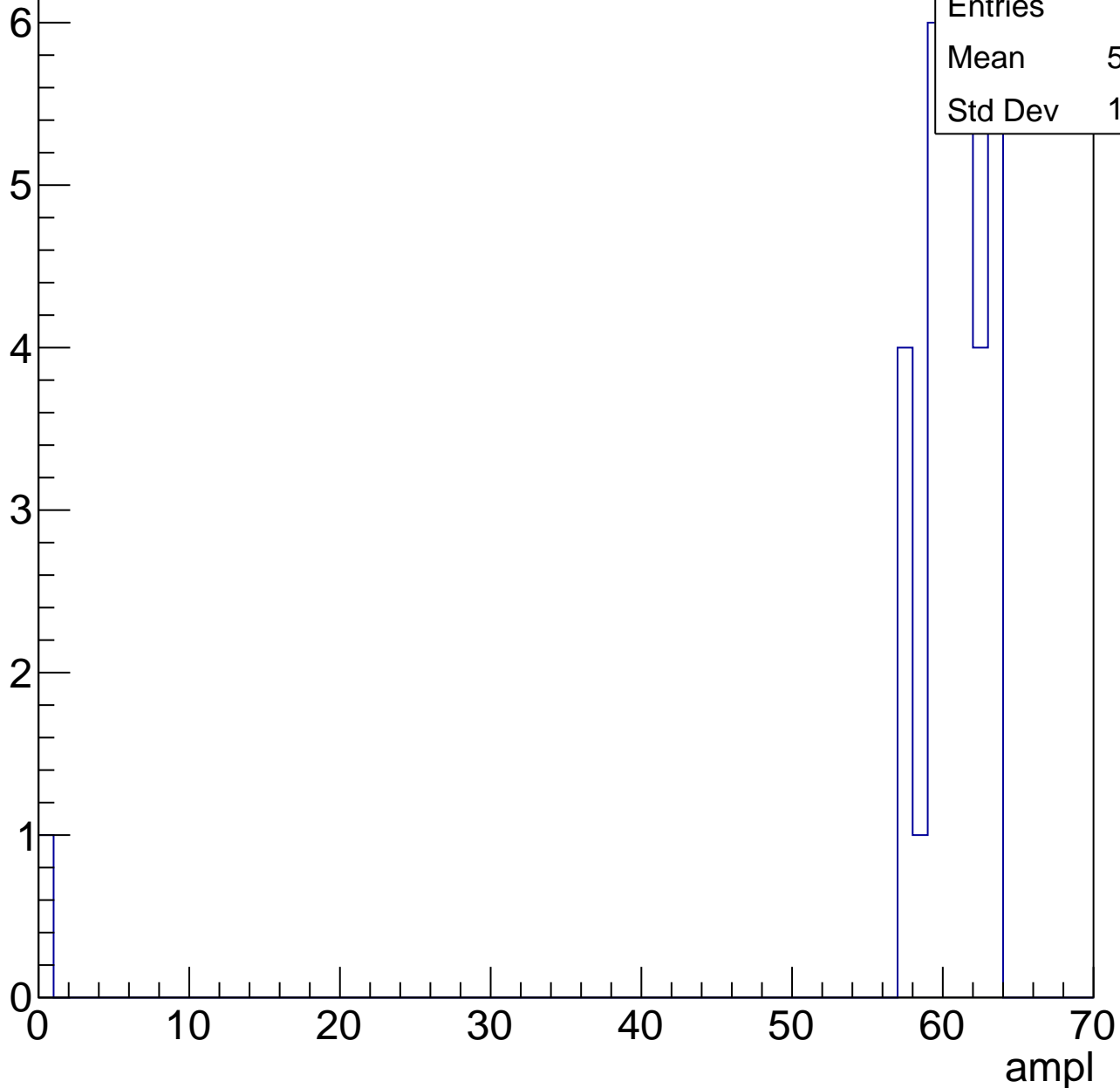
Entries	67
Mean	56.27
Std Dev	3.676



# B0L001S, U5-ch105, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch105, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch105, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch106, adc0

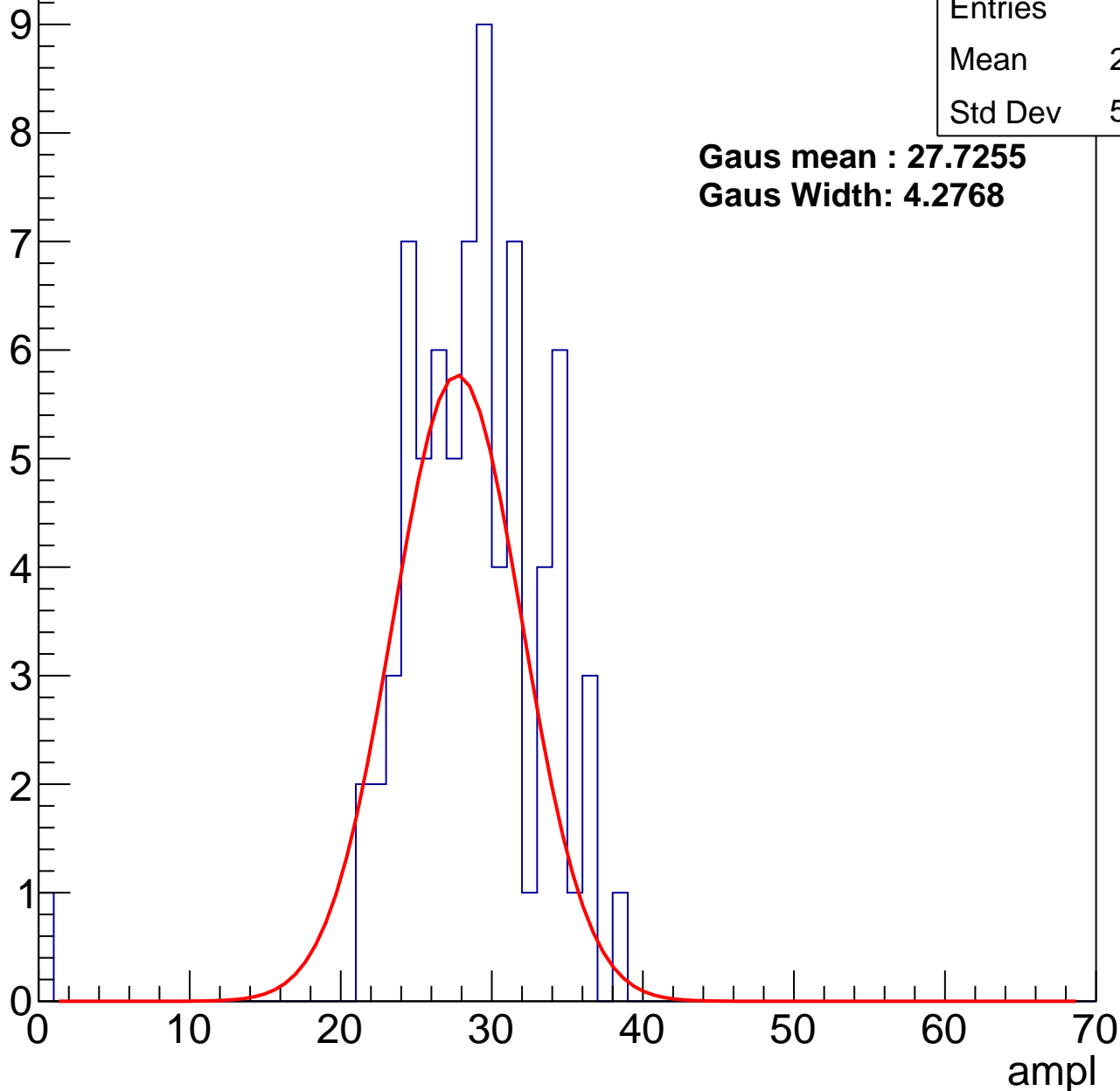
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	28.14
Std Dev	5.166

**Gaus mean : 27.7255**

**Gaus Width: 4.2768**



# B0L001S, U5-ch106, adc1

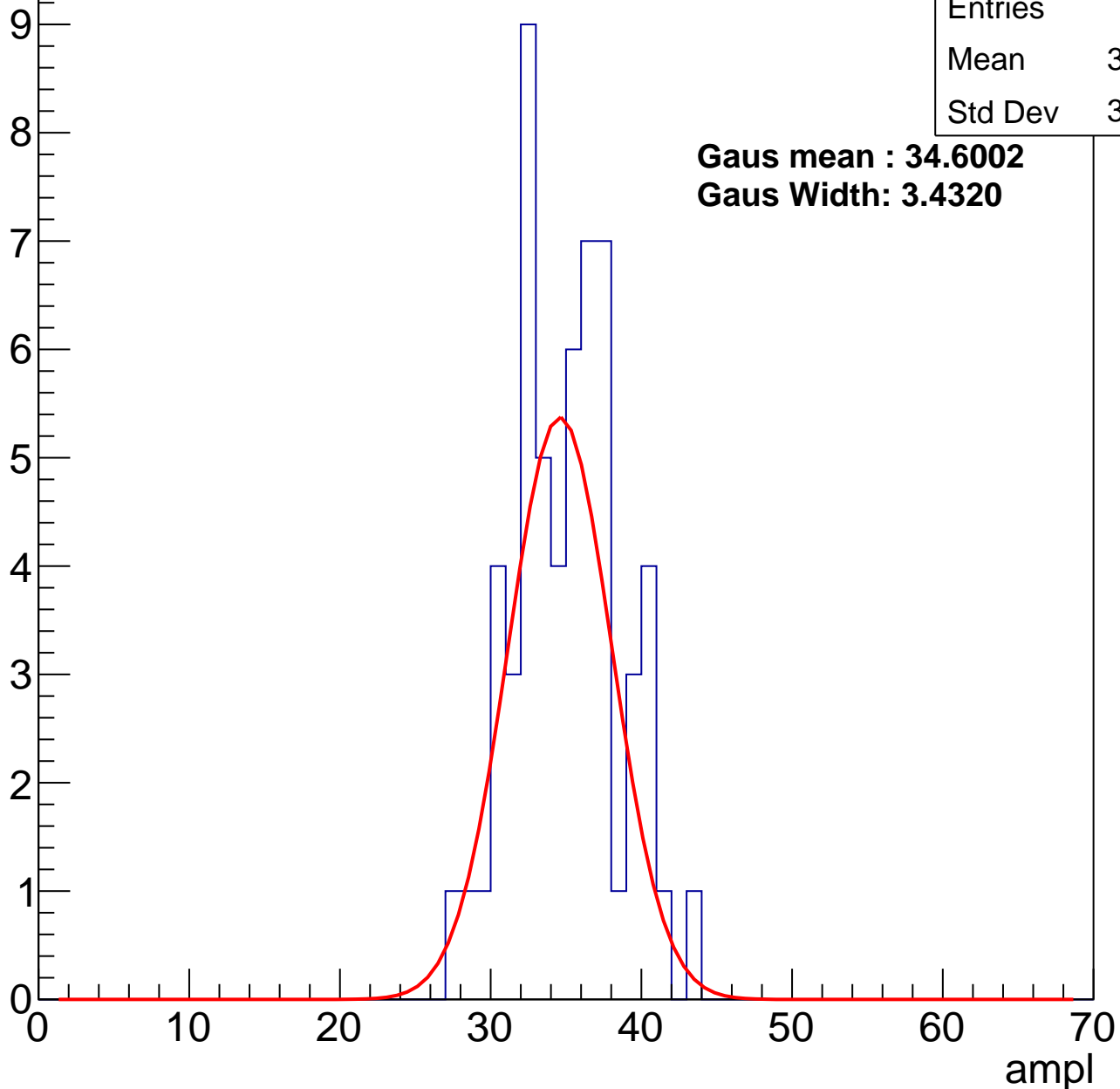
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	34.59
Std Dev	3.434

**Gaus mean : 34.6002**

**Gaus Width: 3.4320**



# B0L001S, U5-ch106, adc2

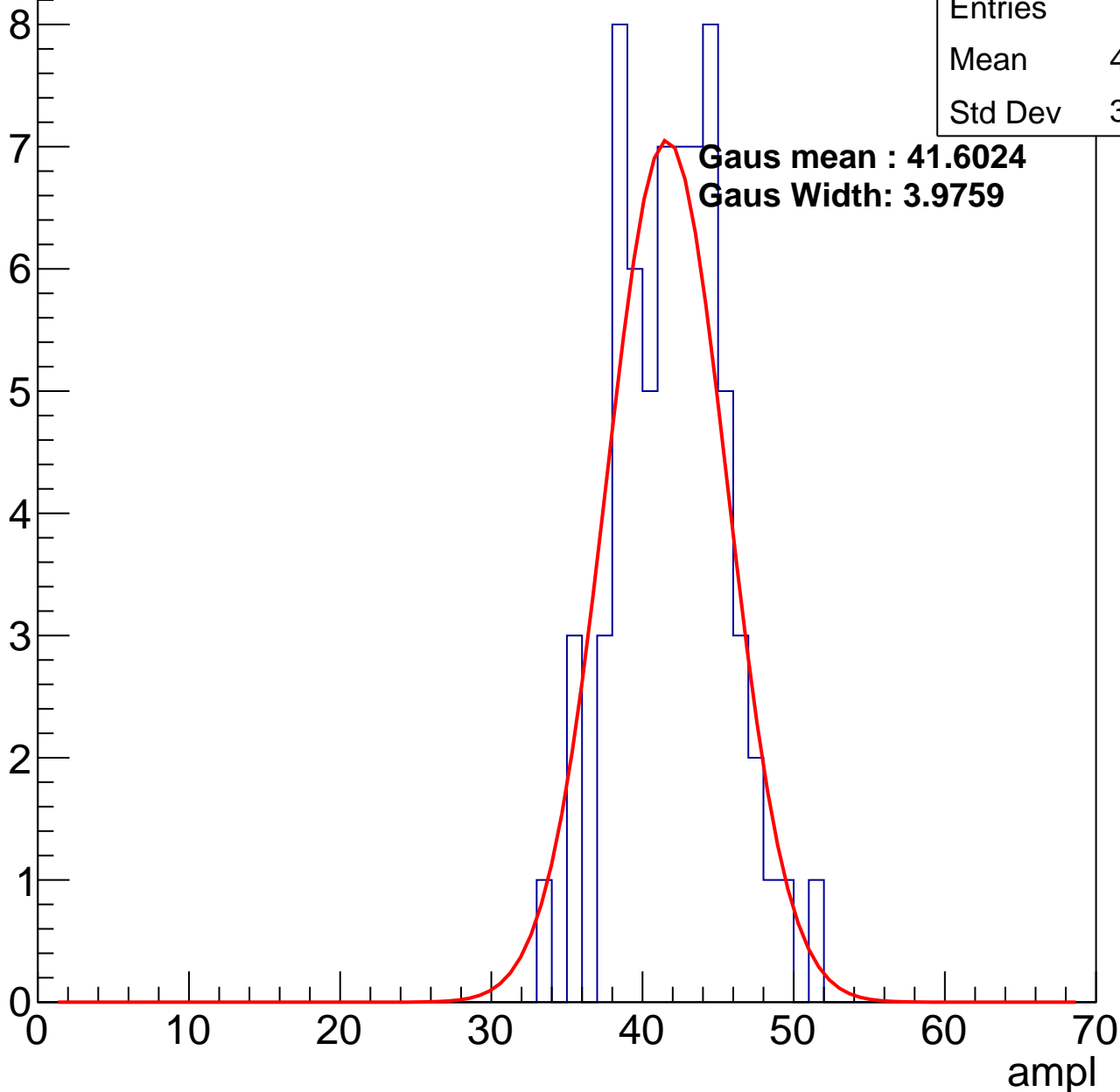
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	41.56
Std Dev	3.529

**Gaus mean : 41.6024**

**Gaus Width: 3.9759**

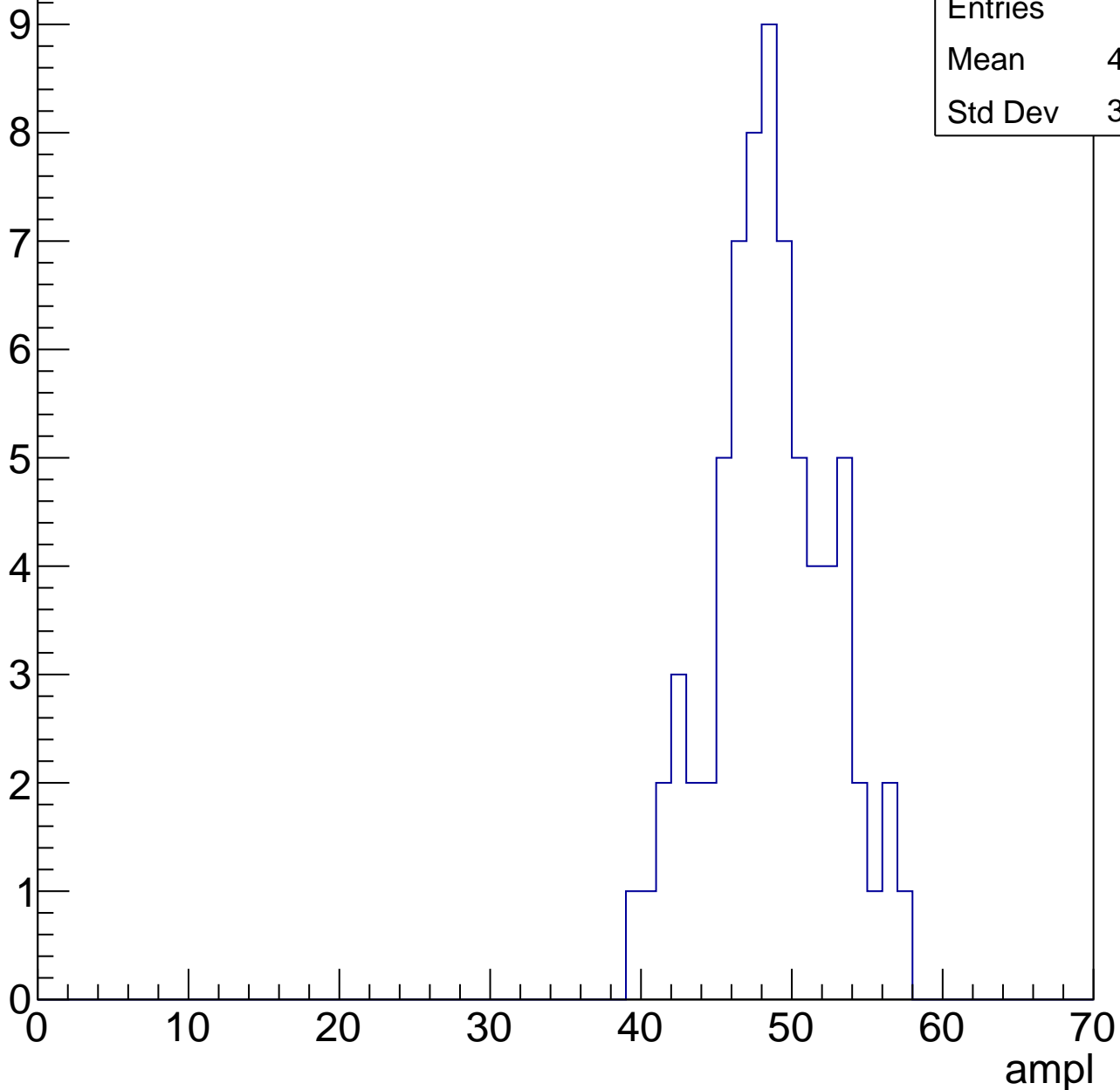


# B0L001S, U5-ch106, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

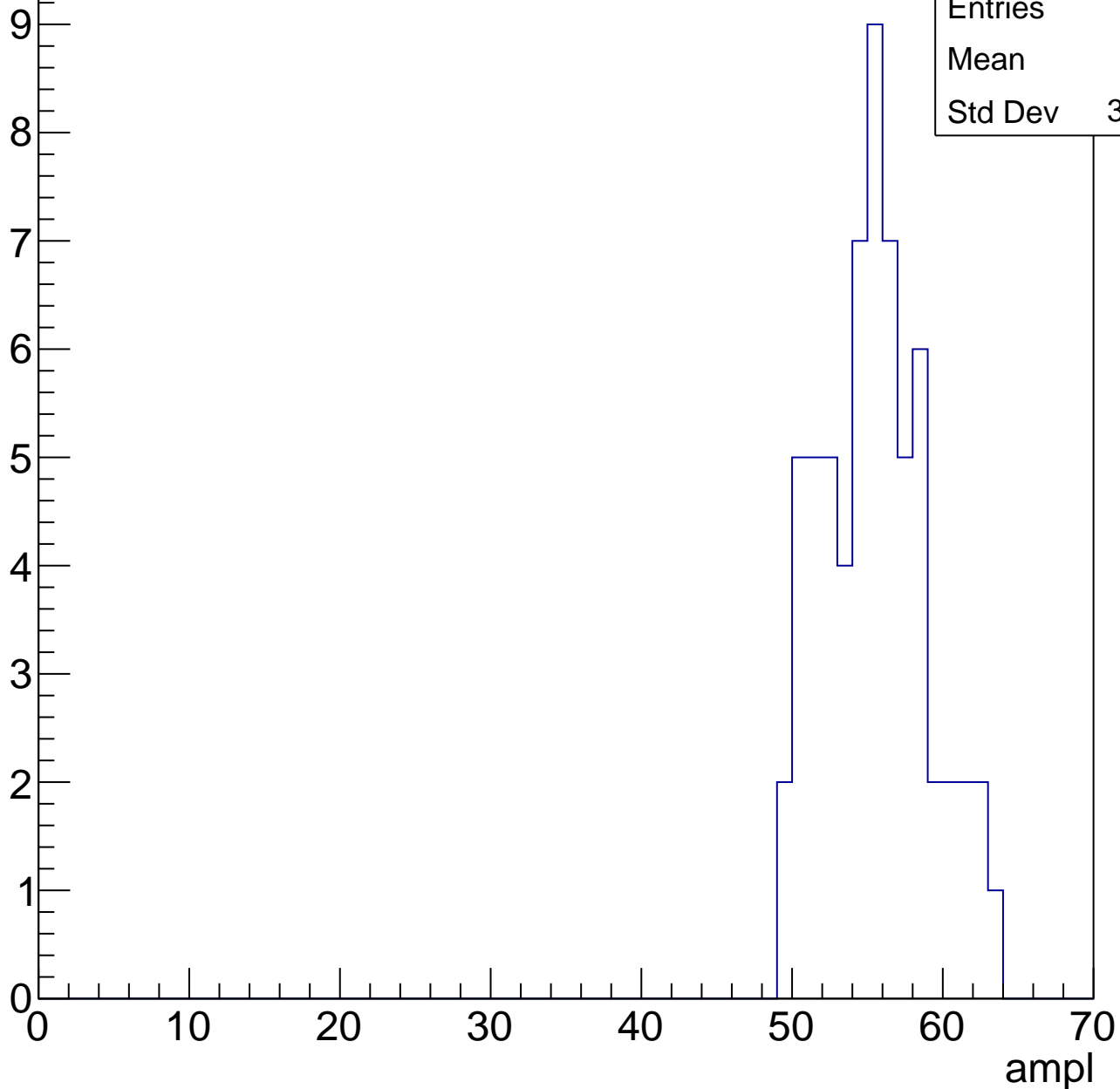
Entries	71
Mean	48.14
Std Dev	3.926



# B0L001S, U5-ch106, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

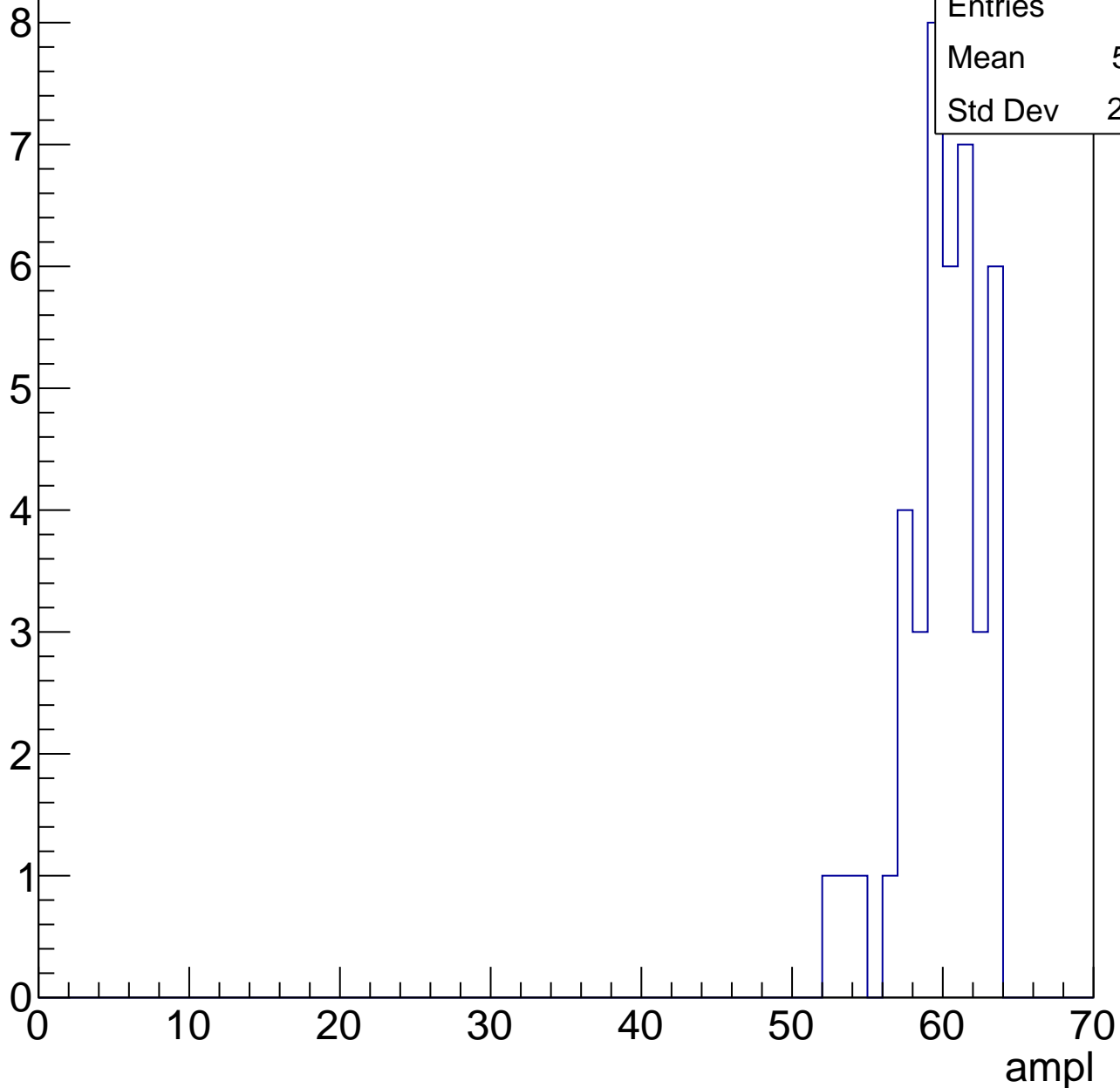


# B0L001S, U5-ch106, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	41
Mean	59.51
Std Dev	2.633

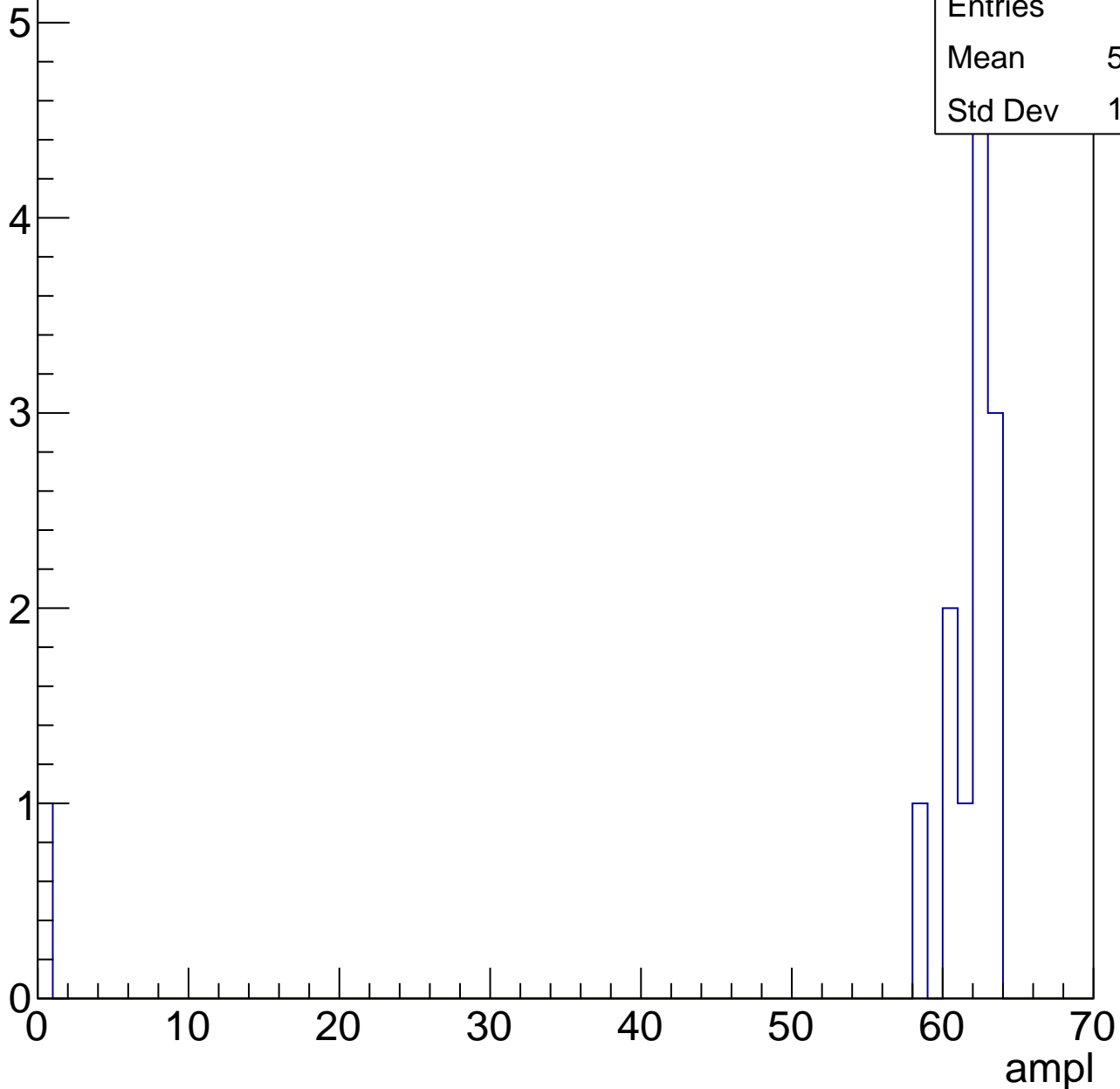


# B0L001S, U5-ch106, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	13
Mean	56.77
Std Dev	16.45





# B0L001S, U5-ch106, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

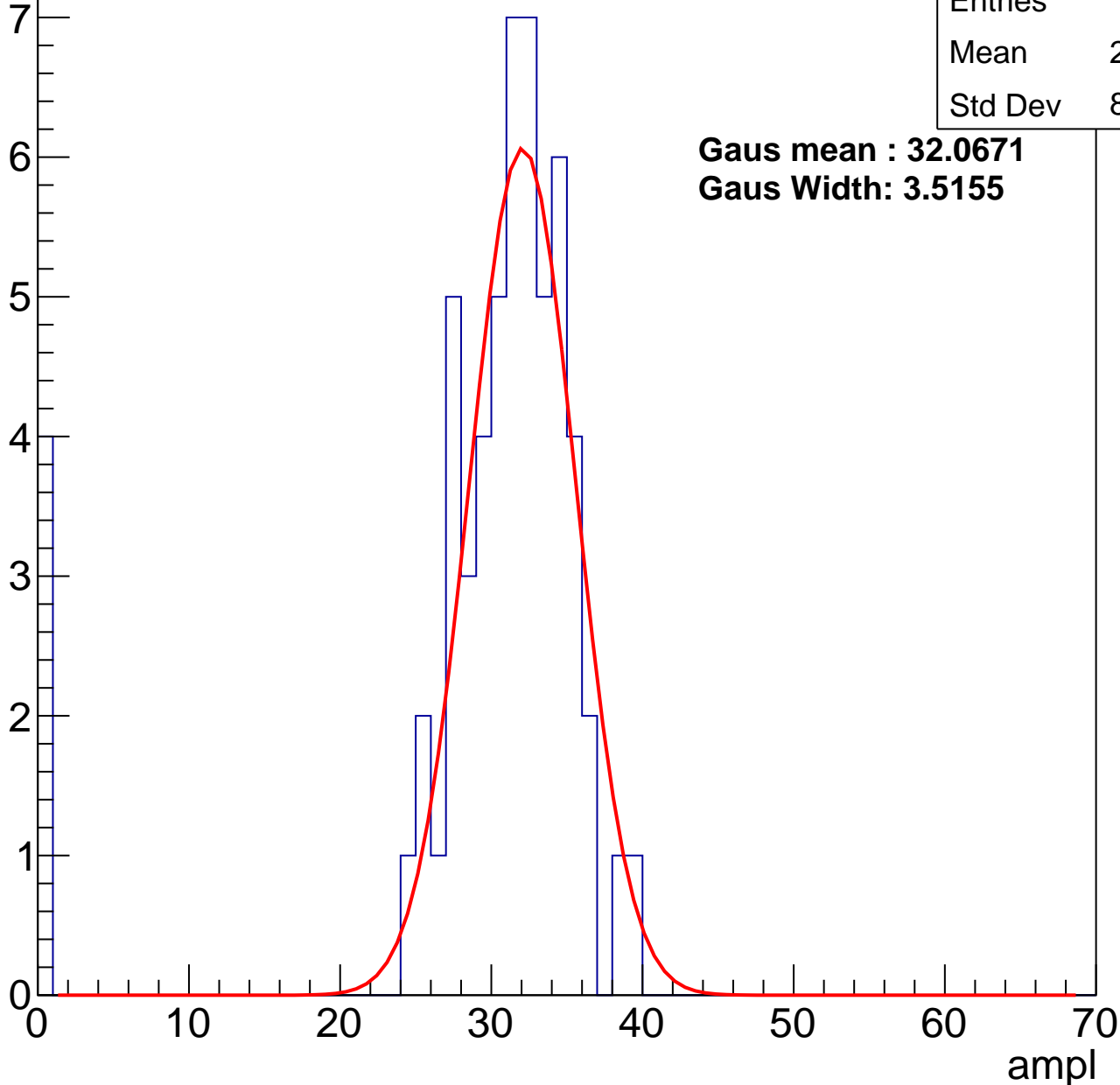
# B0L001S, U5-ch107, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	29.03
Std Dev	8.512

**Gaus mean : 32.0671**  
**Gaus Width: 3.5155**



# B0L001S, U5-ch107, adc1

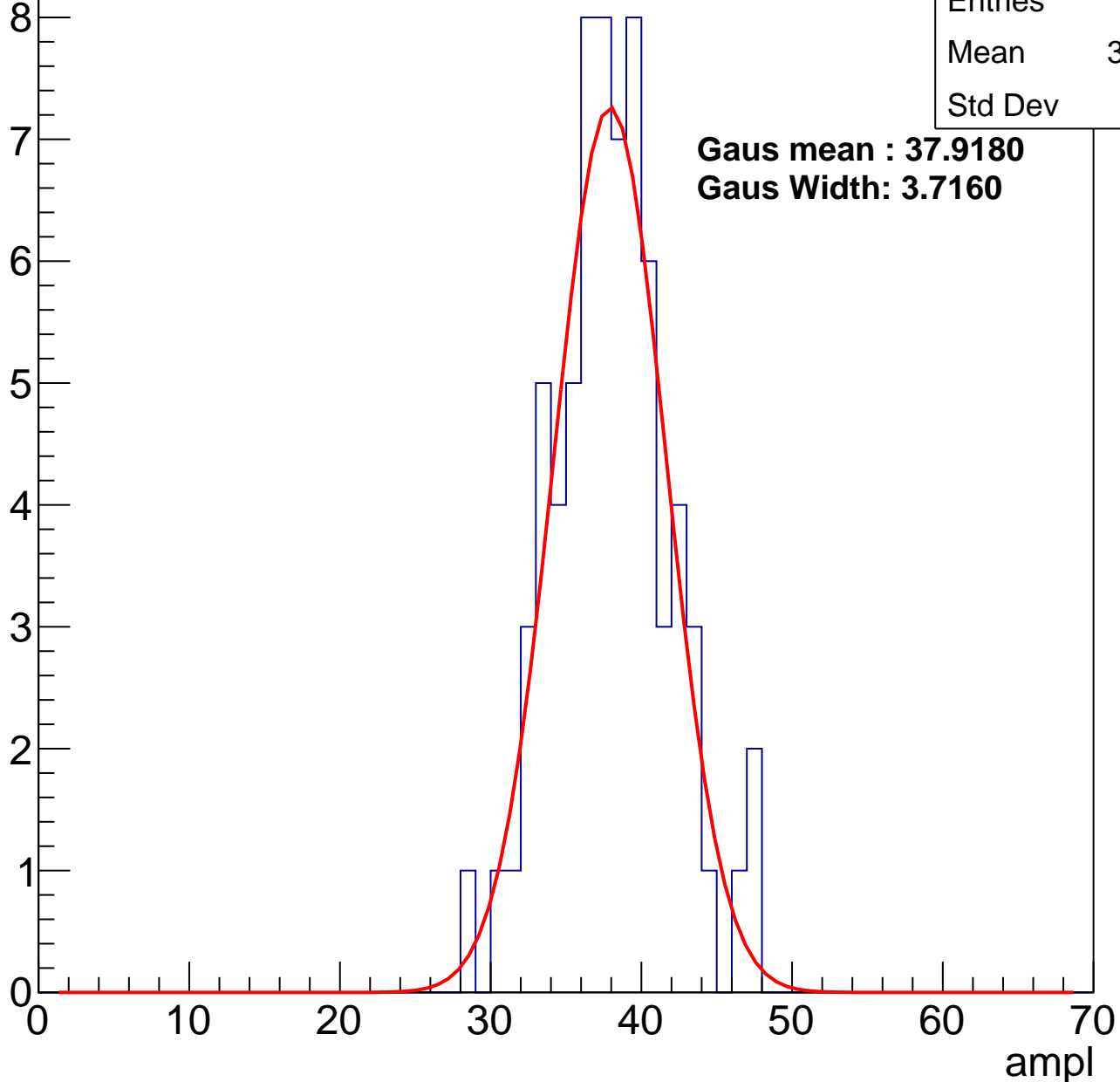
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	37.56
Std Dev	3.83

**Gaus mean : 37.9180**

**Gaus Width: 3.7160**

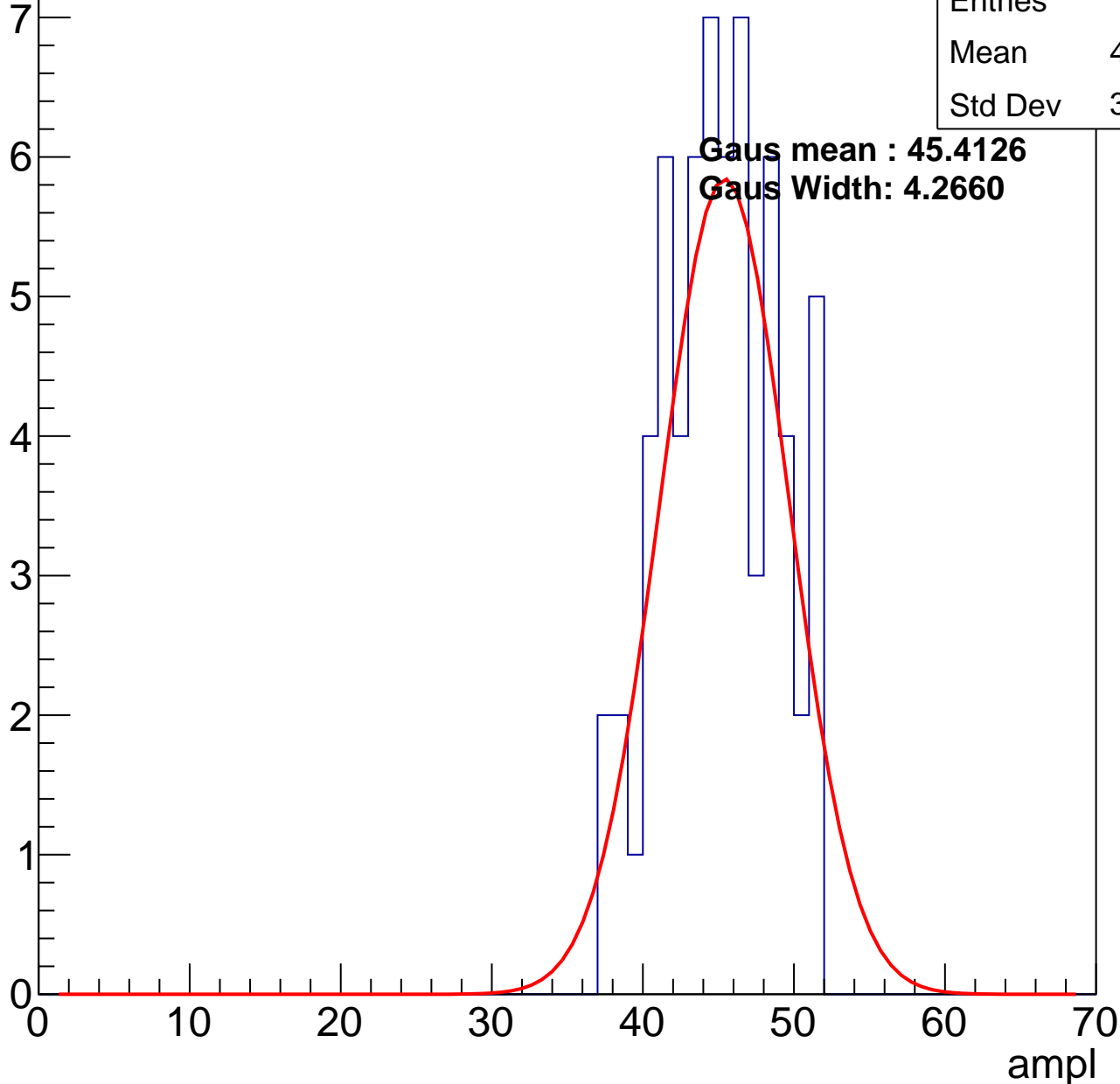


# B0L001S, U5-ch107, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	44.63
Std Dev	3.686

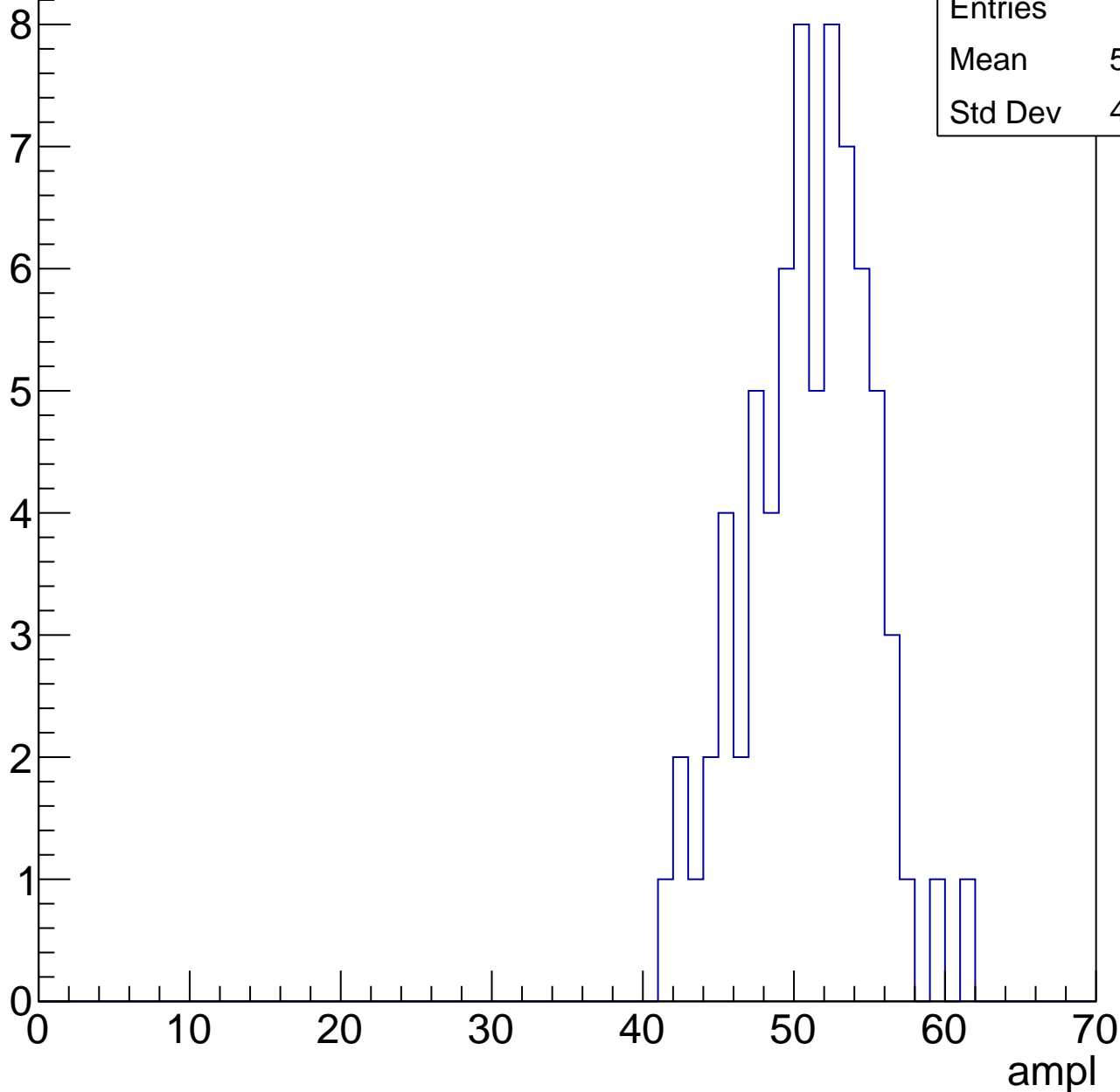


# B0L001S, U5-ch107, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	50.49
Std Dev	4.069

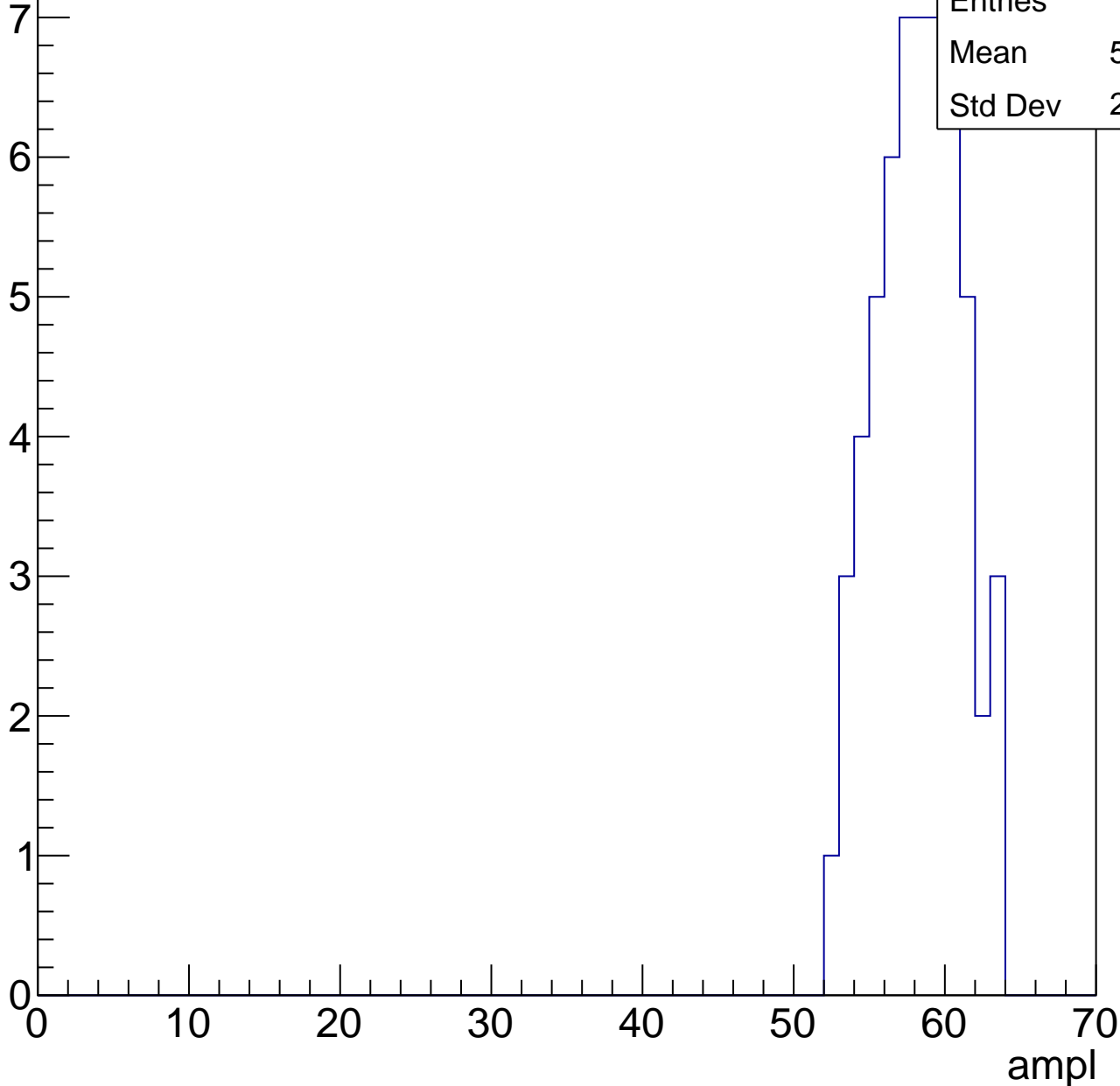


# B0L001S, U5-ch107, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	57.79
Std Dev	2.764

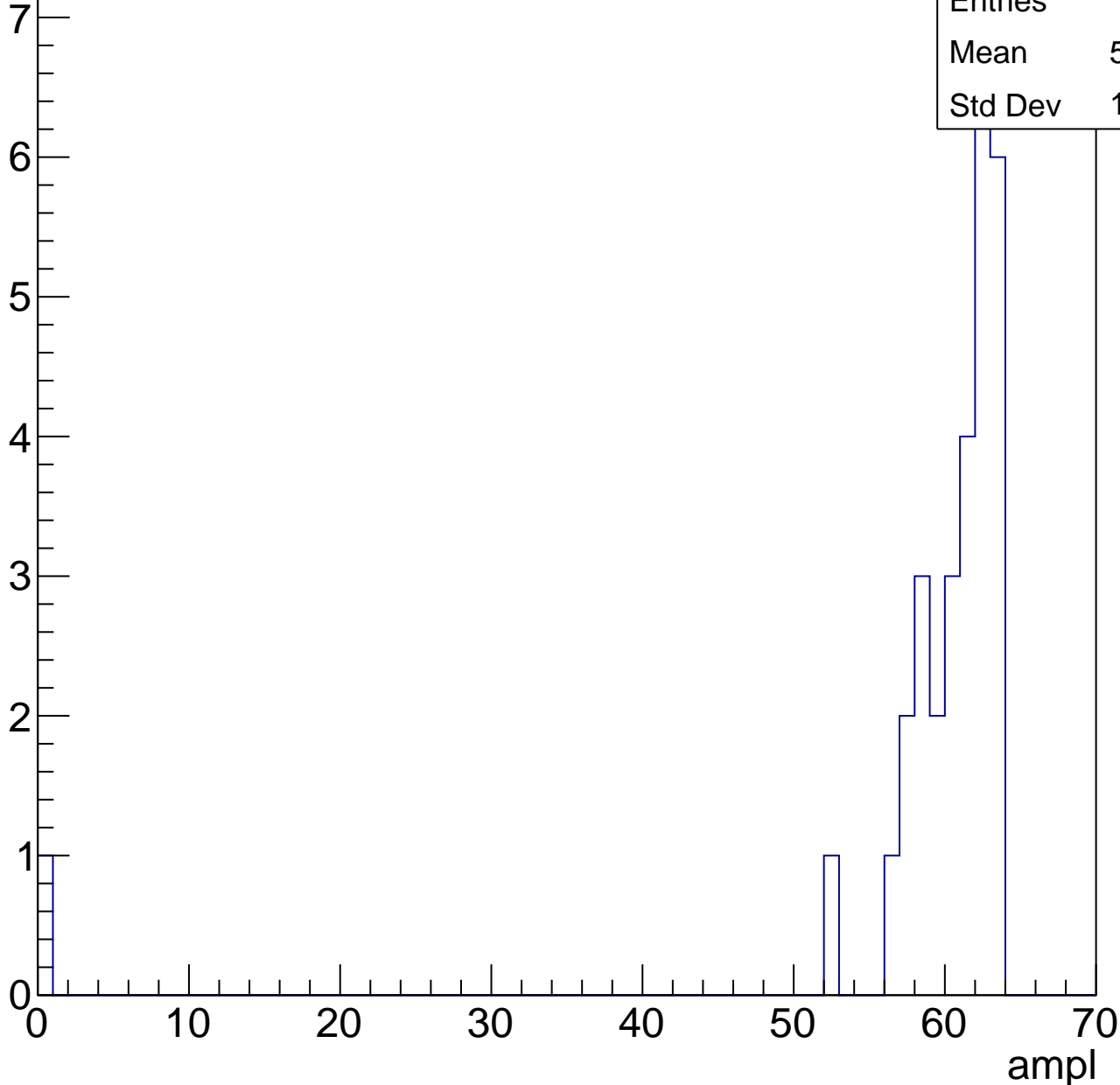


# B0L001S, U5-ch107, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	30
Mean	58.33
Std Dev	11.13



# B0L001S, U5-ch107, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch107, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch108, adc0

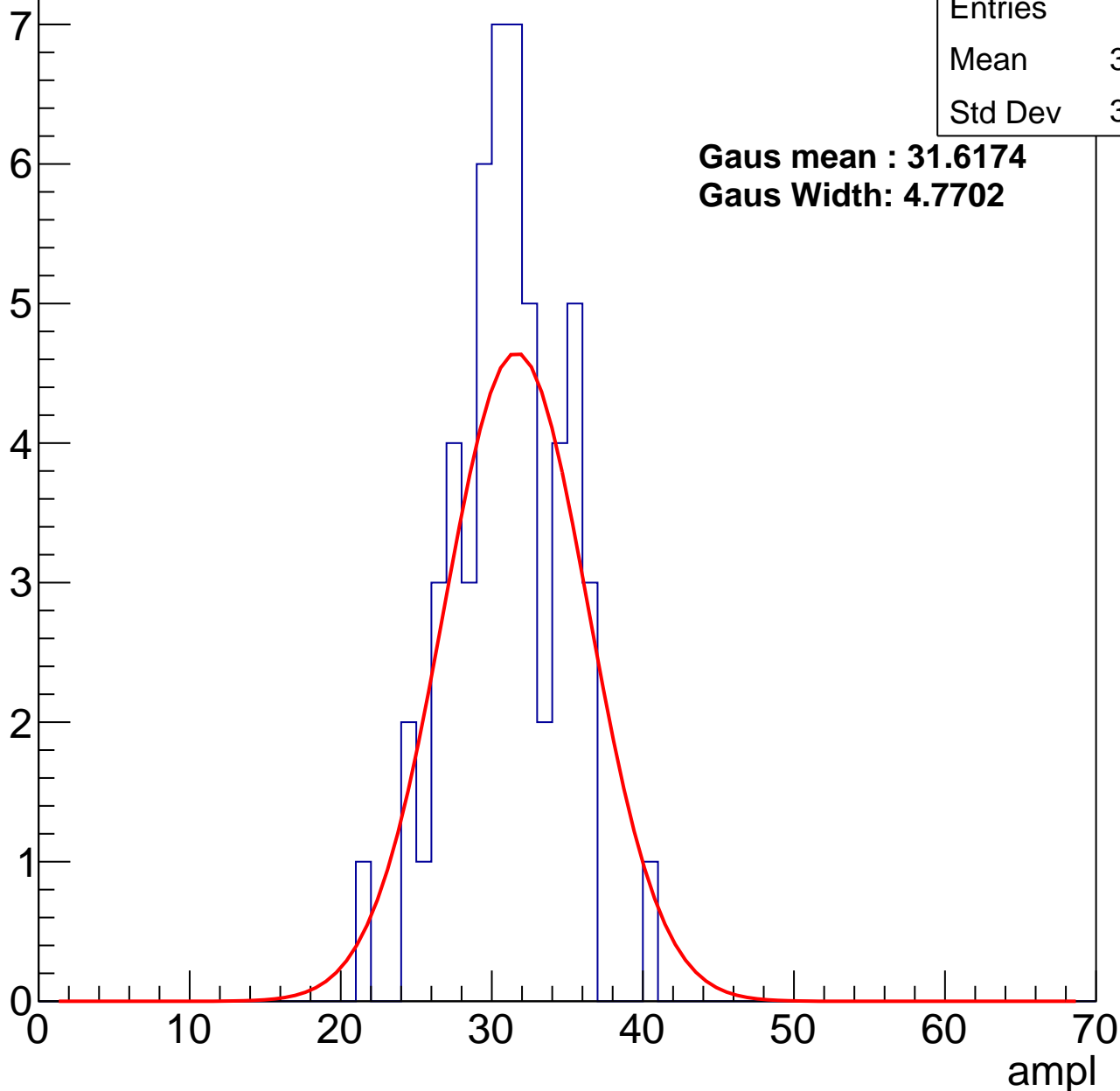
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	30.56
Std Dev	3.614

**Gaus mean : 31.6174**

**Gaus Width: 4.7702**



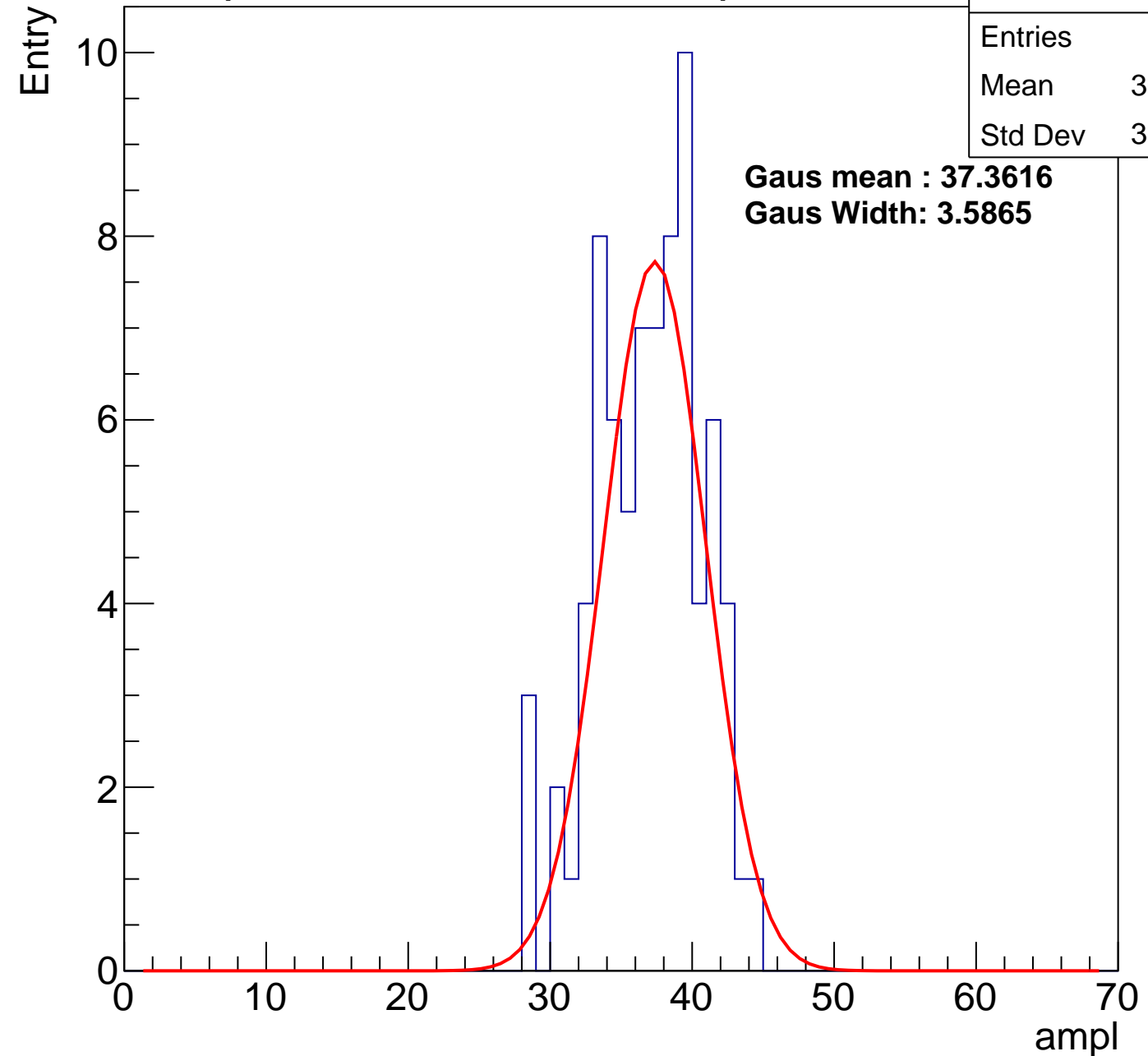
# B0L001S, U5-ch108, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	77
Mean	36.52
Std Dev	3.663

**Gaus mean : 37.3616**

**Gaus Width: 3.5865**



# B0L001S, U5-ch108, adc2

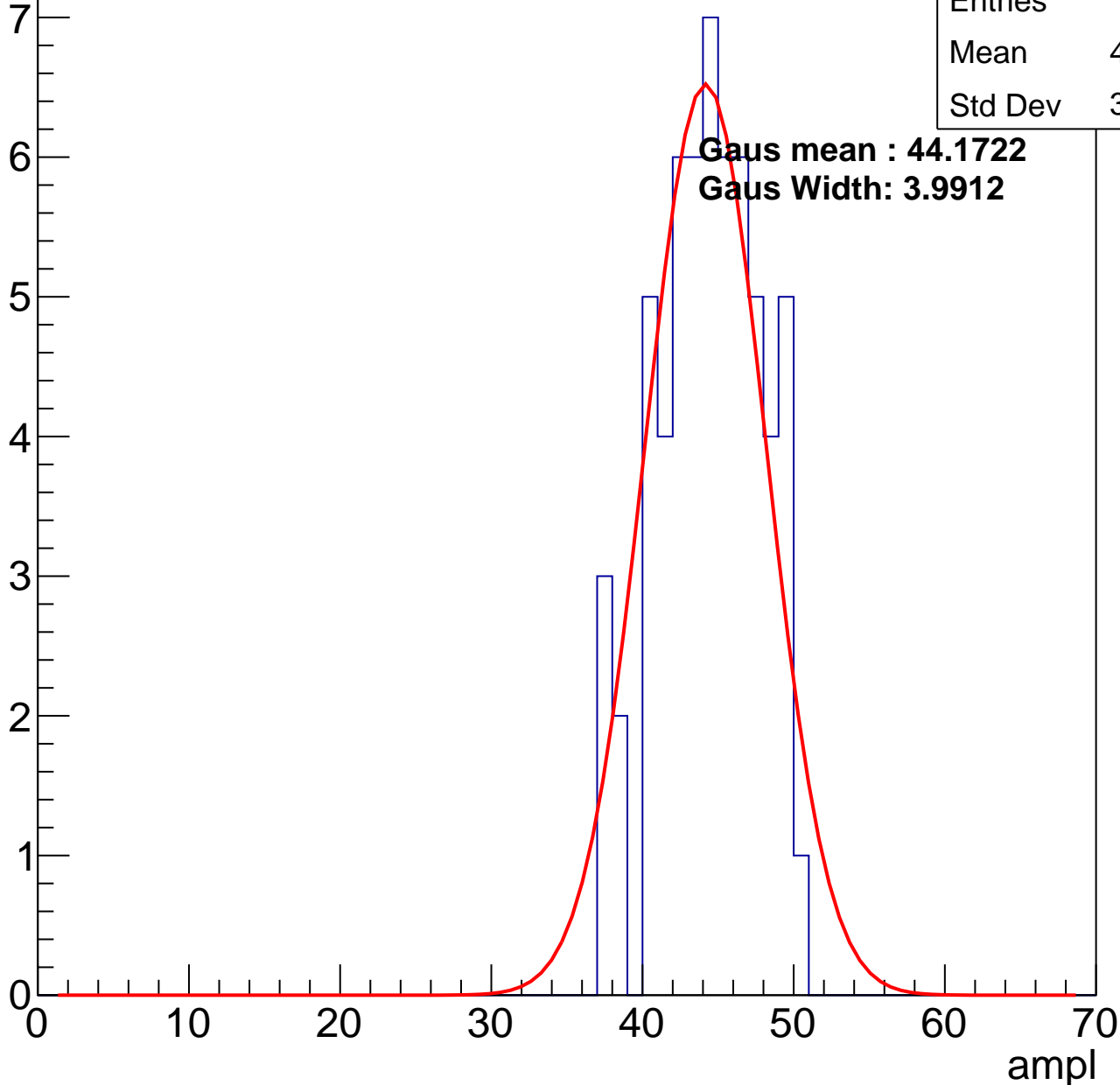
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	43.95
Std Dev	3.329

**Gaus mean : 44.1722**

**Gaus Width: 3.9912**

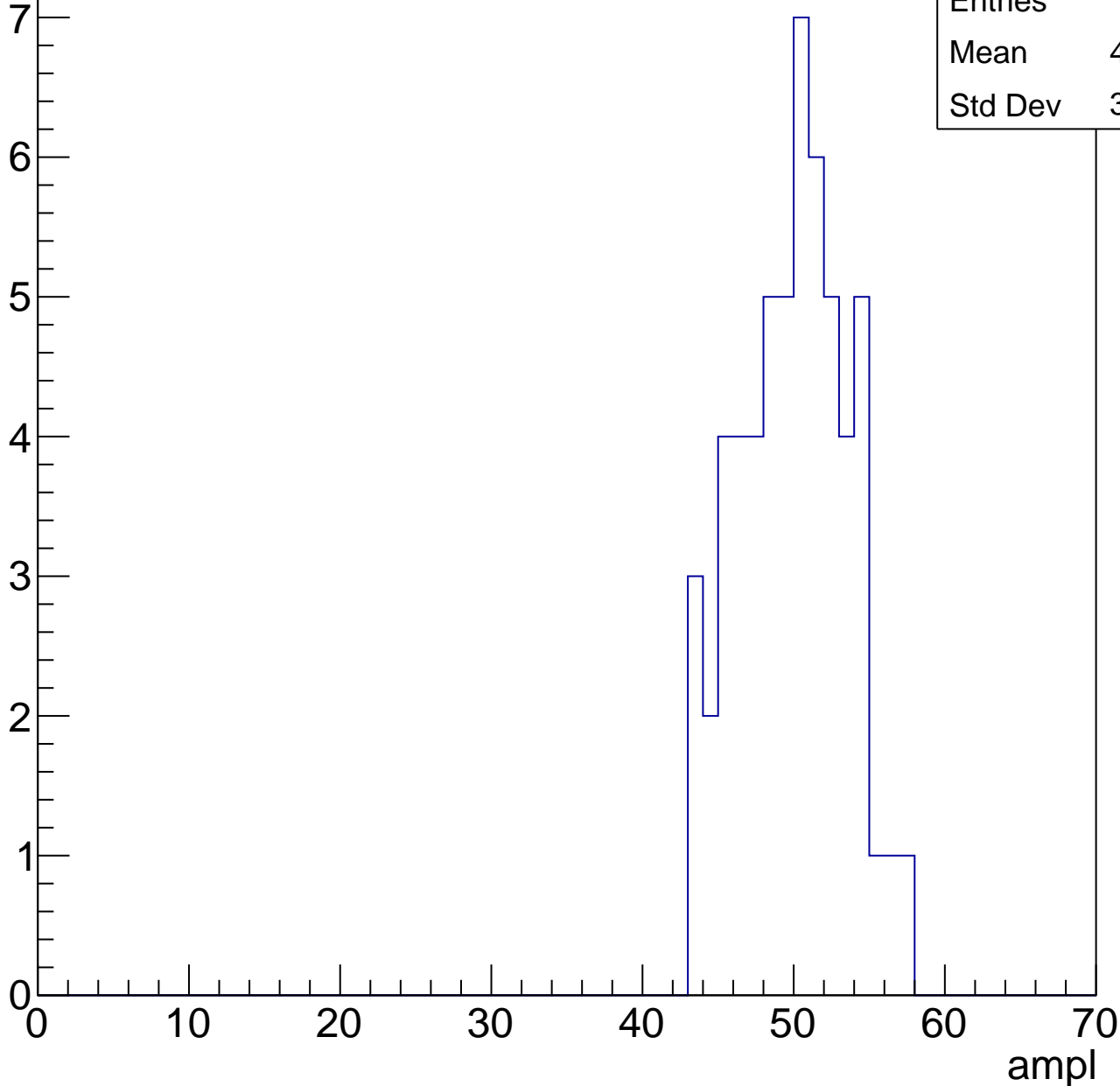


# B0L001S, U5-ch108, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	49.47
Std Dev	3.454

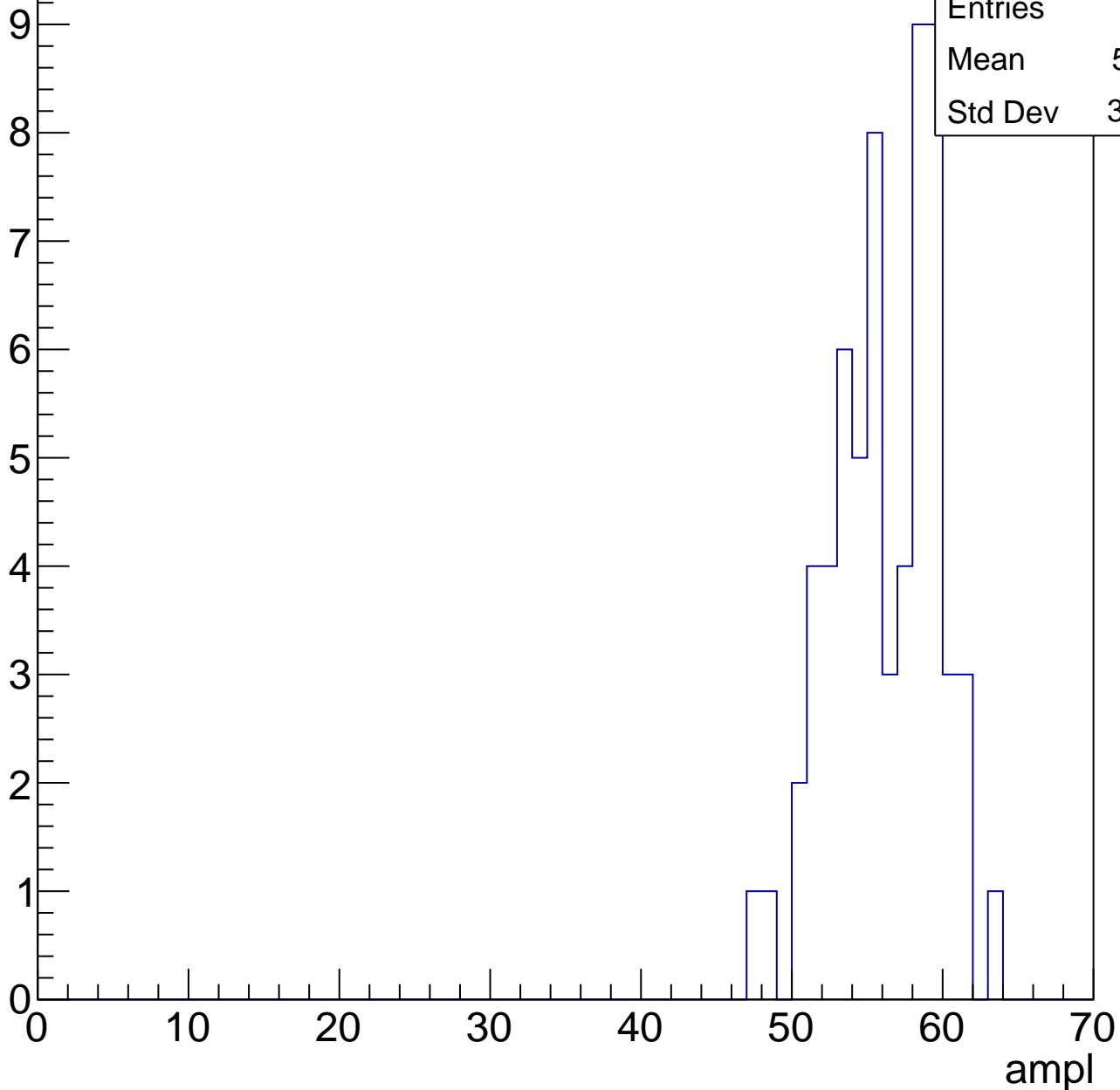


# B0L001S, U5-ch108, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	55.71
Std Dev	3.452

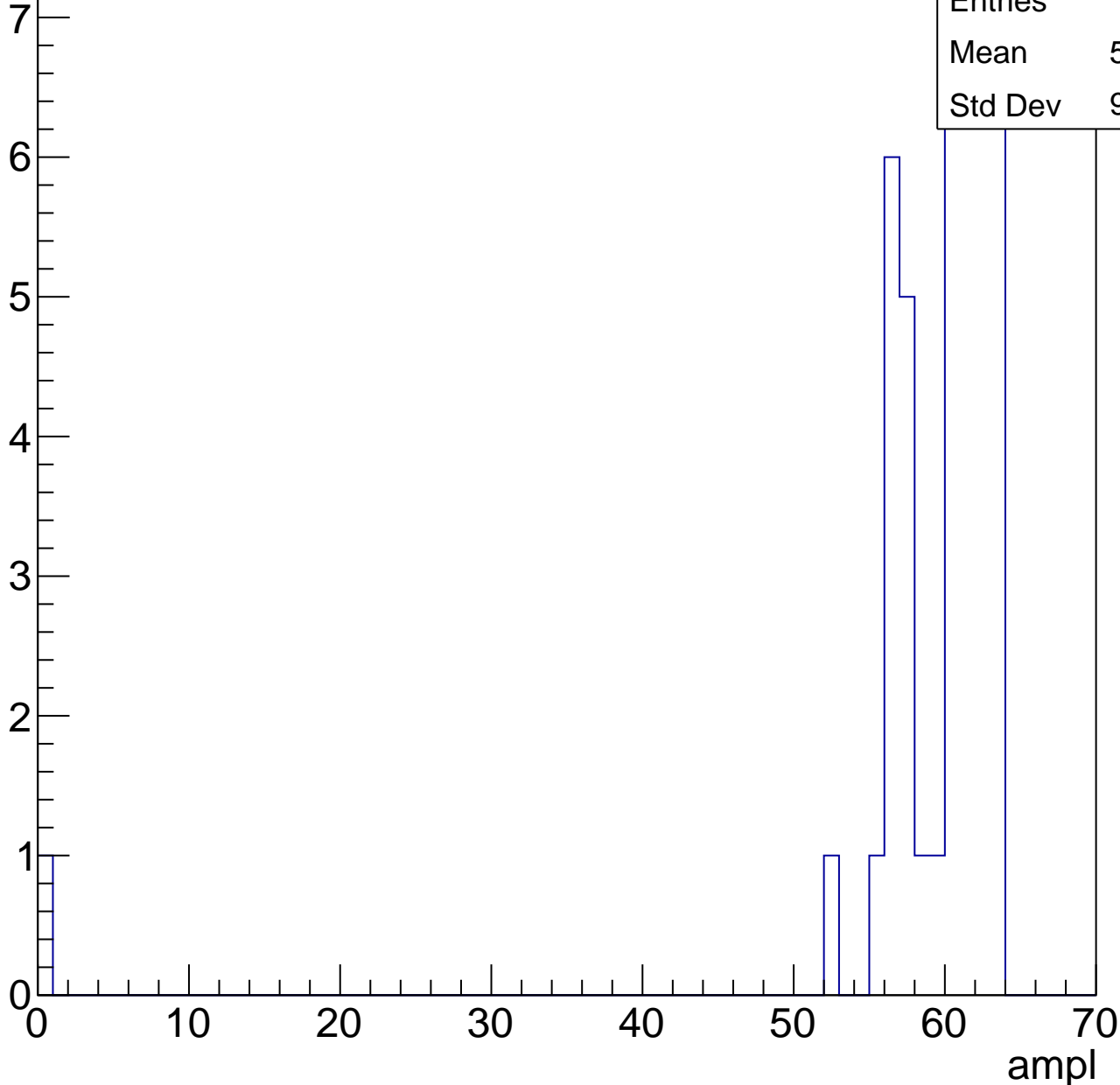


# B0L001S, U5-ch108, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	44
Mean	58.34
Std Dev	9.308



# B0L001S, U5-ch108, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch108, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L001S, U5-ch109, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	84
Mean	29.44
Std Dev	4.834

**Gaus mean : 30.3558**

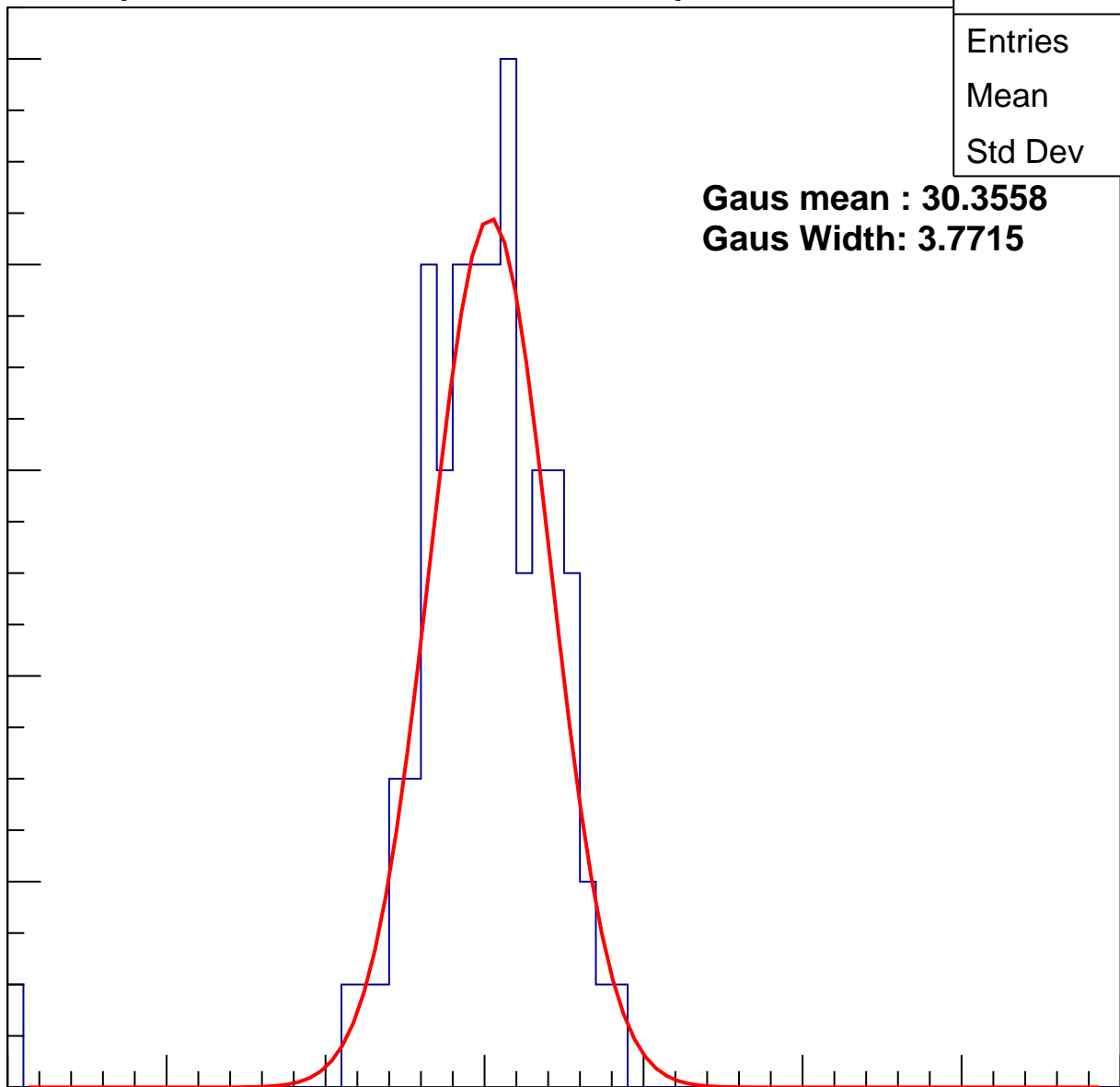
**Gaus Width: 3.7715**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



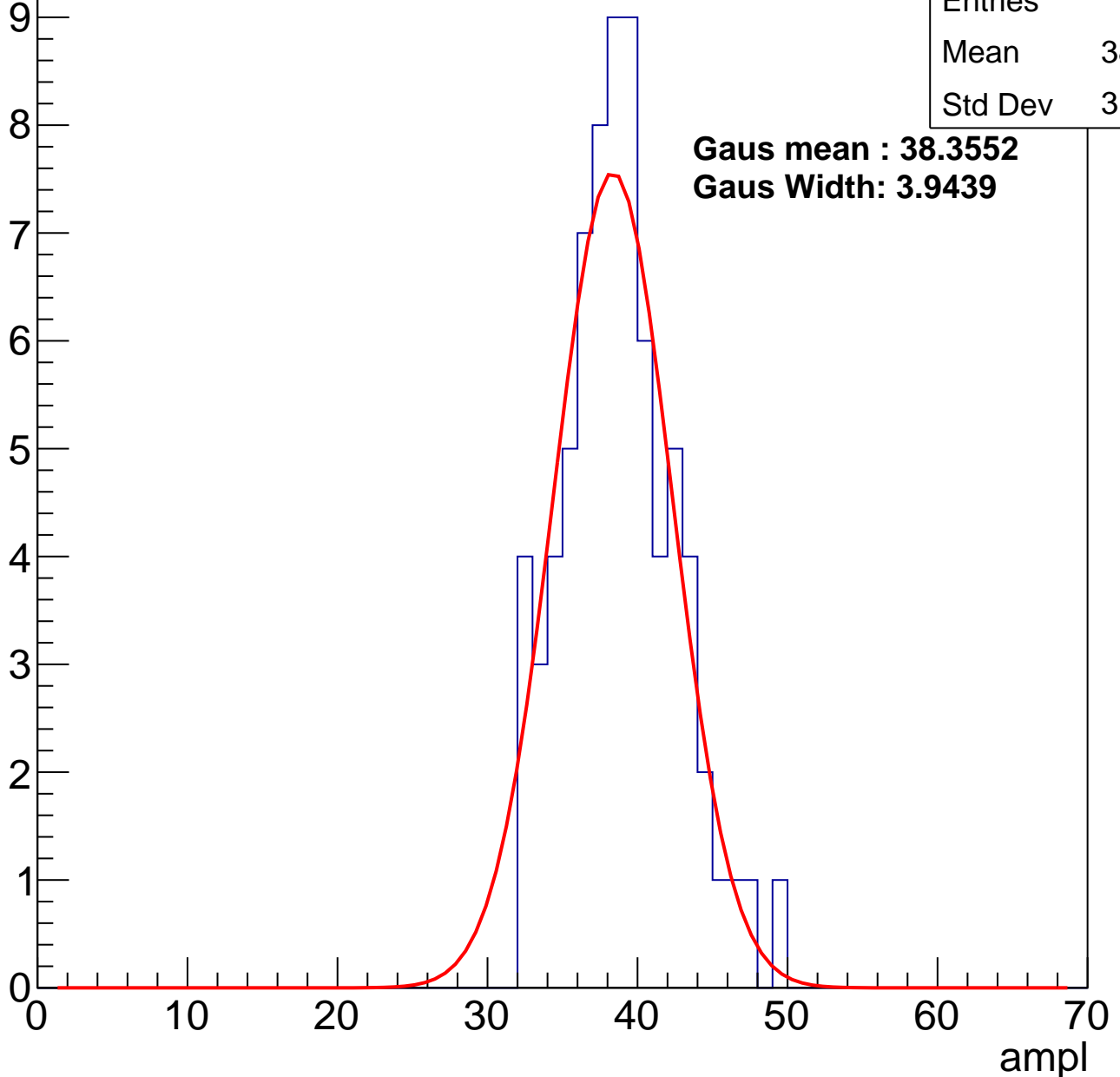
# B0L001S, U5-ch109, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	38.38
Std Dev	3.657

**Gaus mean : 38.3552**  
**Gaus Width: 3.9439**



# B0L001S, U5-ch109, adc2

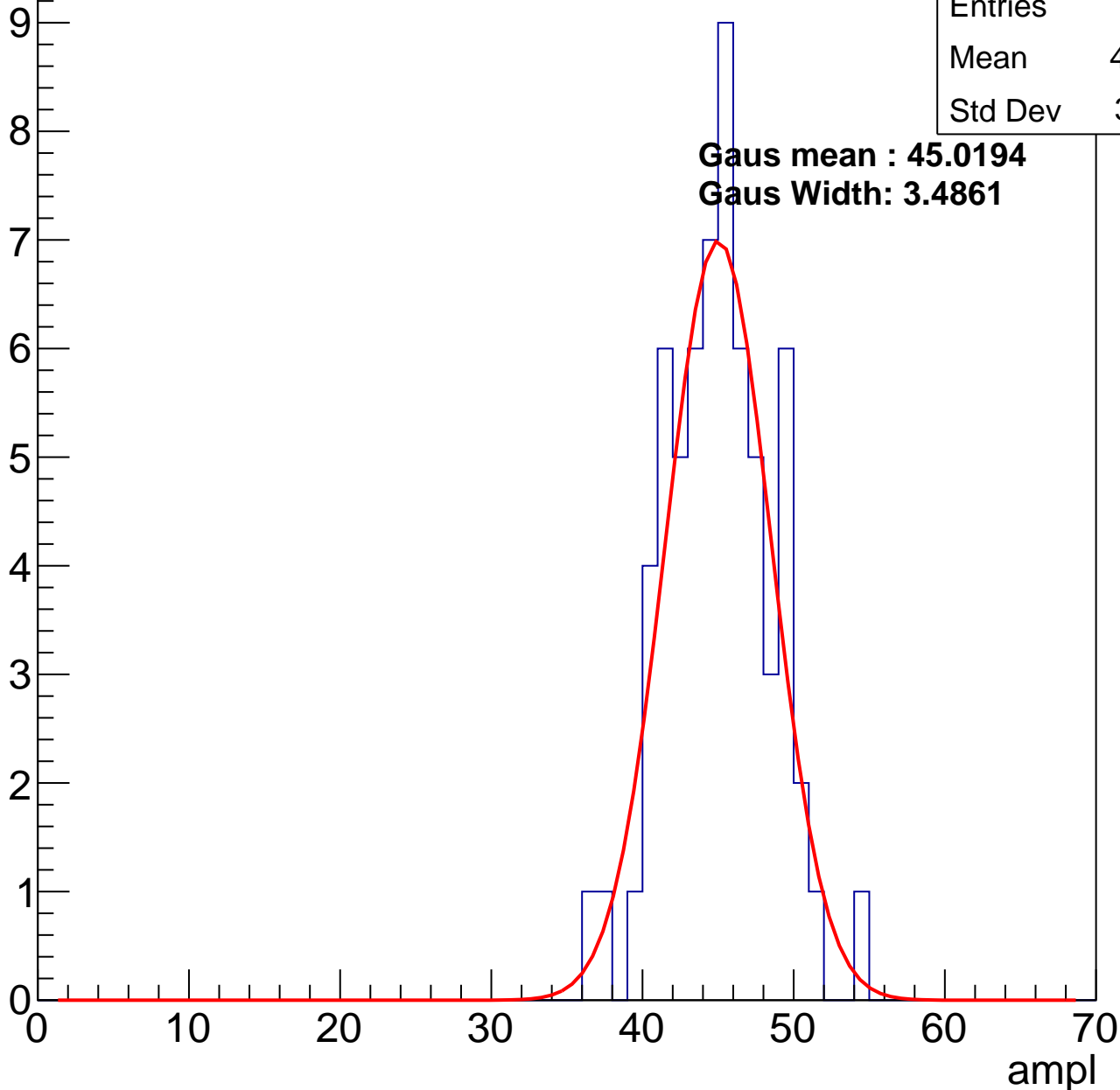
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	44.58
Std Dev	3.441

**Gaus mean : 45.0194**

**Gaus Width: 3.4861**

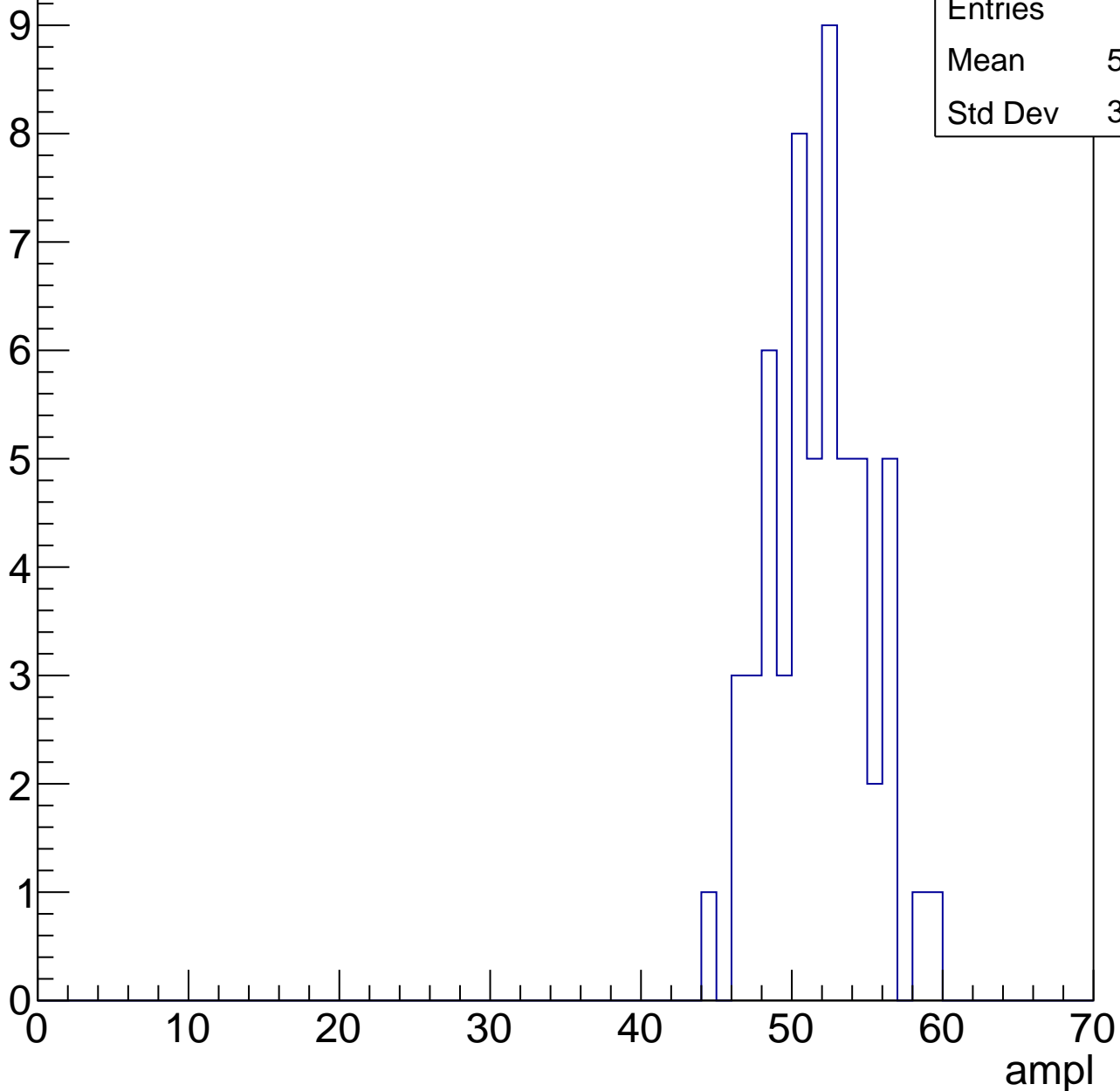


# B0L001S, U5-ch109, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	51.28
Std Dev	3.205

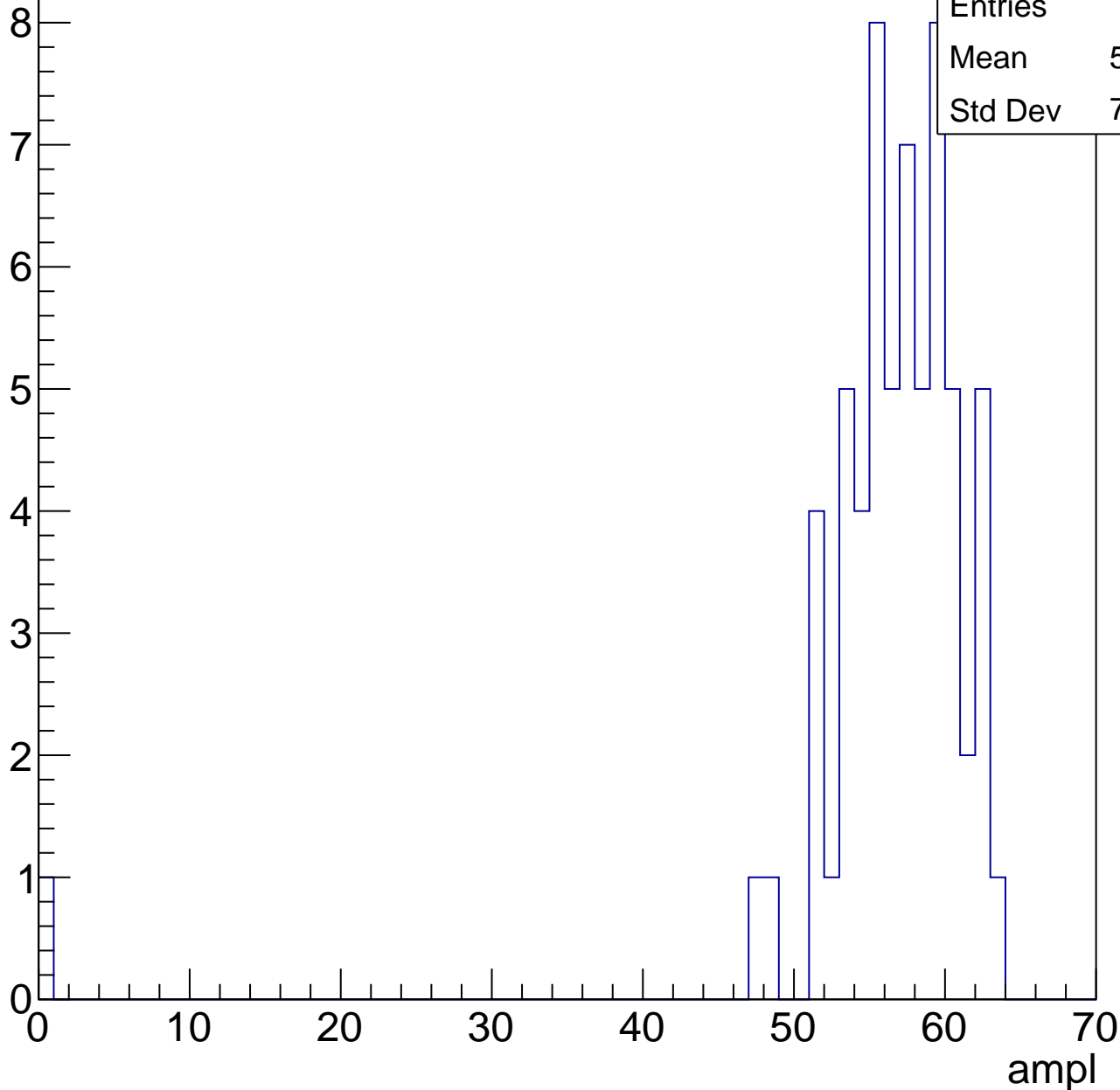


# B0L001S, U5-ch109, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	55.68
Std Dev	7.886

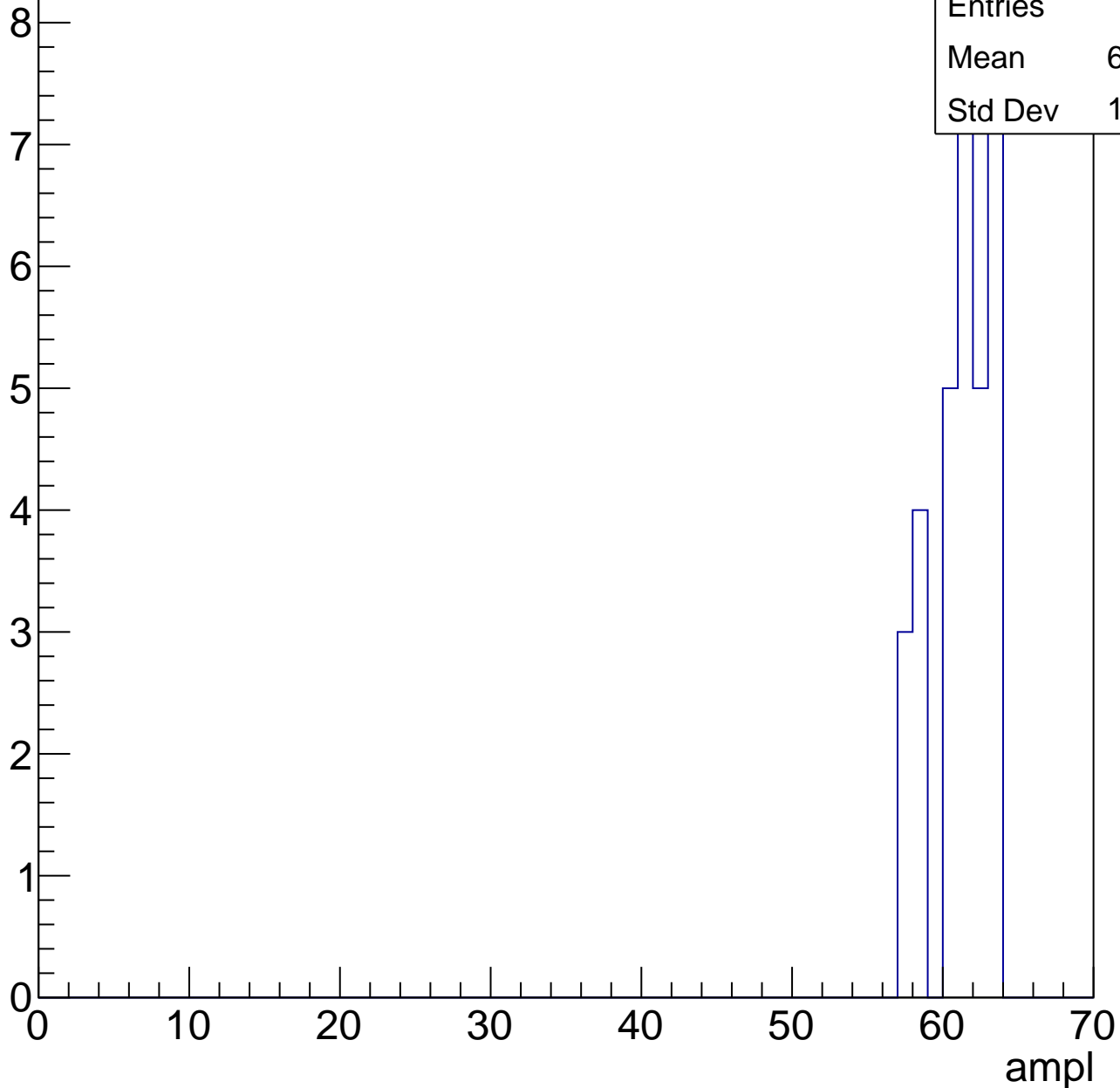


# B0L001S, U5-ch109, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

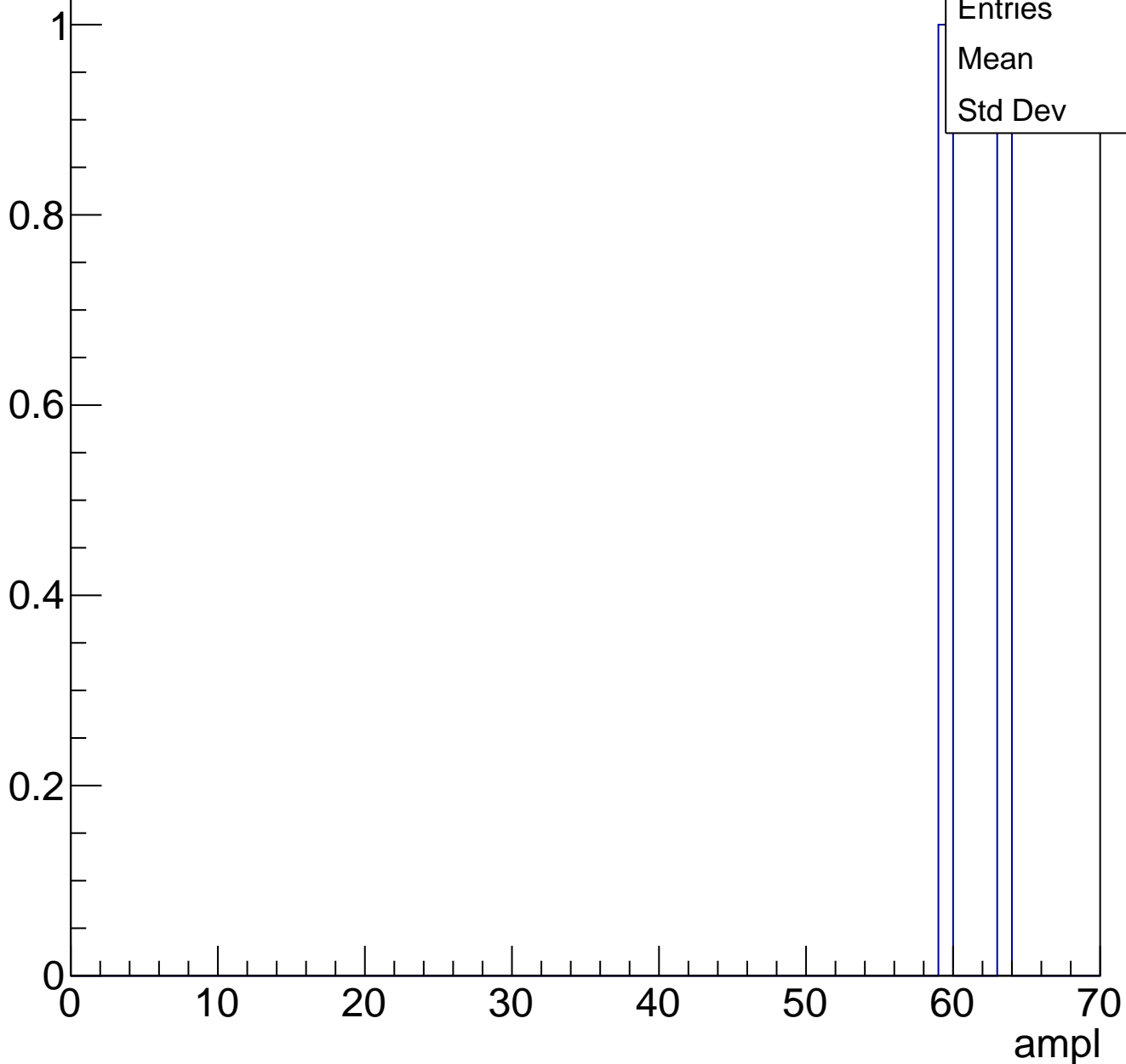
Entries	33
Mean	60.76
Std Dev	1.939



# B0L001S, U5-ch109, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch109, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch110, adc0

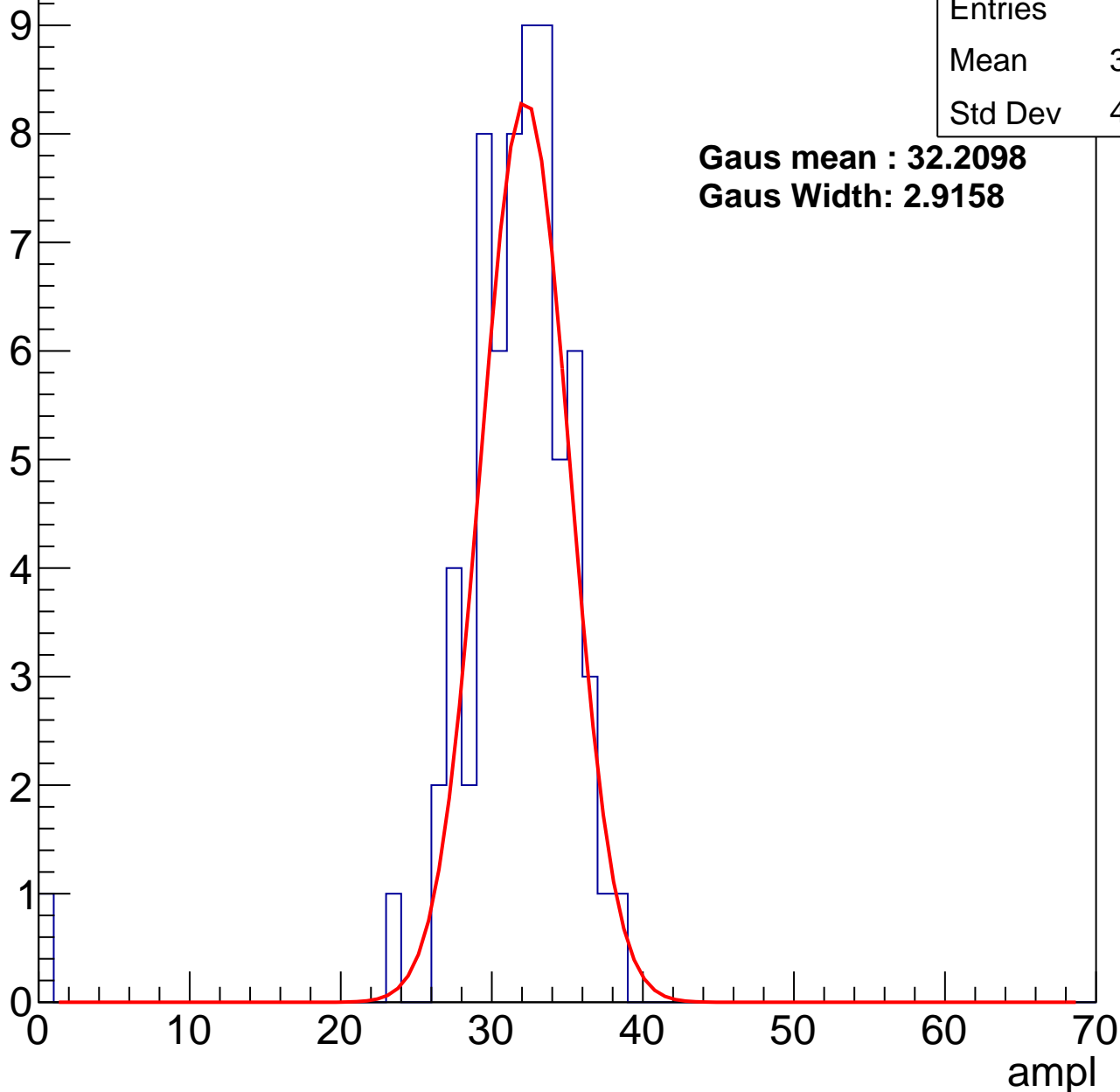
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	31.02
Std Dev	4.832

**Gaus mean : 32.2098**

**Gaus Width: 2.9158**



# B0L001S, U5-ch110, adc1

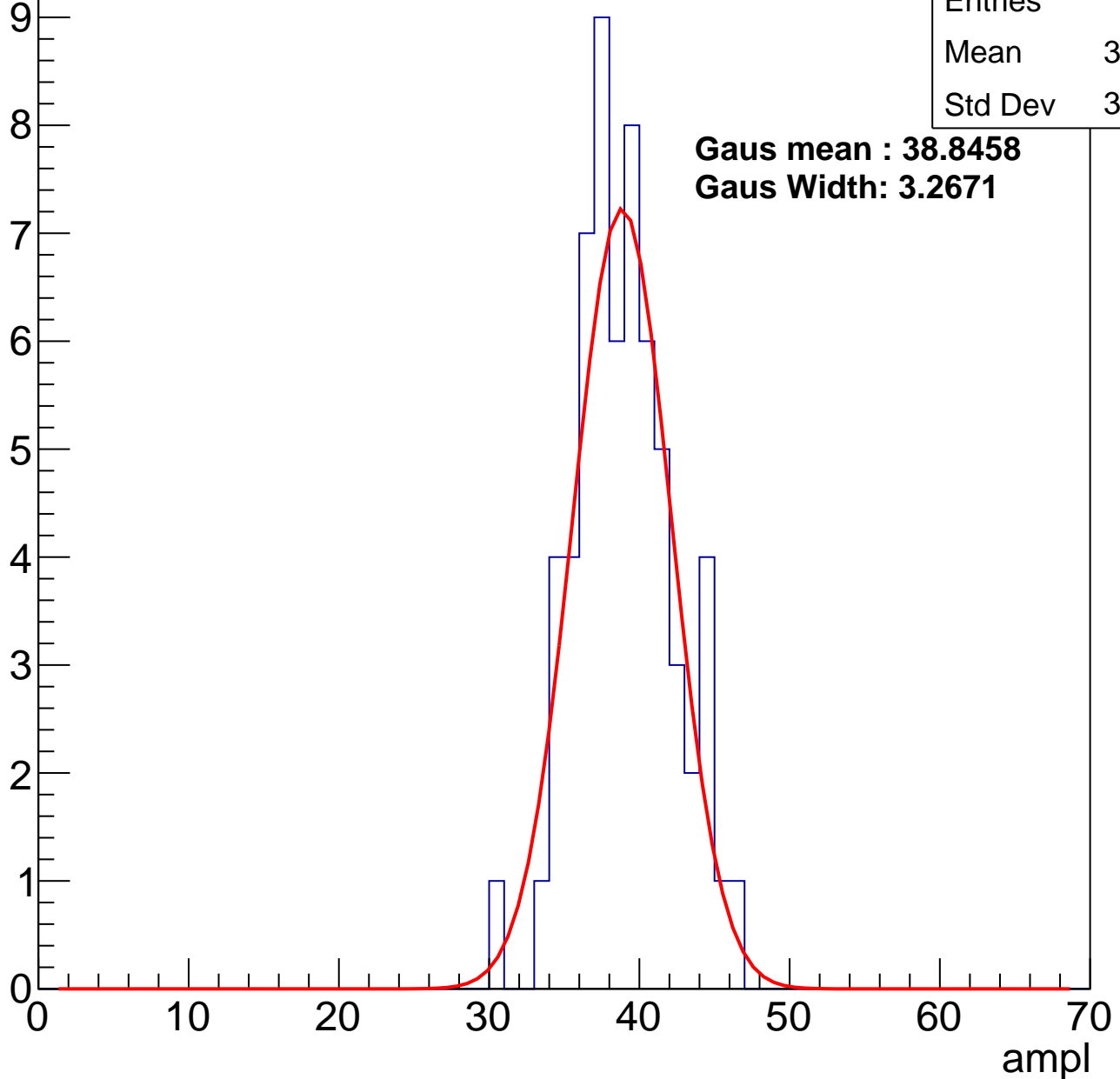
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	38.52
Std Dev	3.217

**Gaus mean : 38.8458**

**Gaus Width: 3.2671**

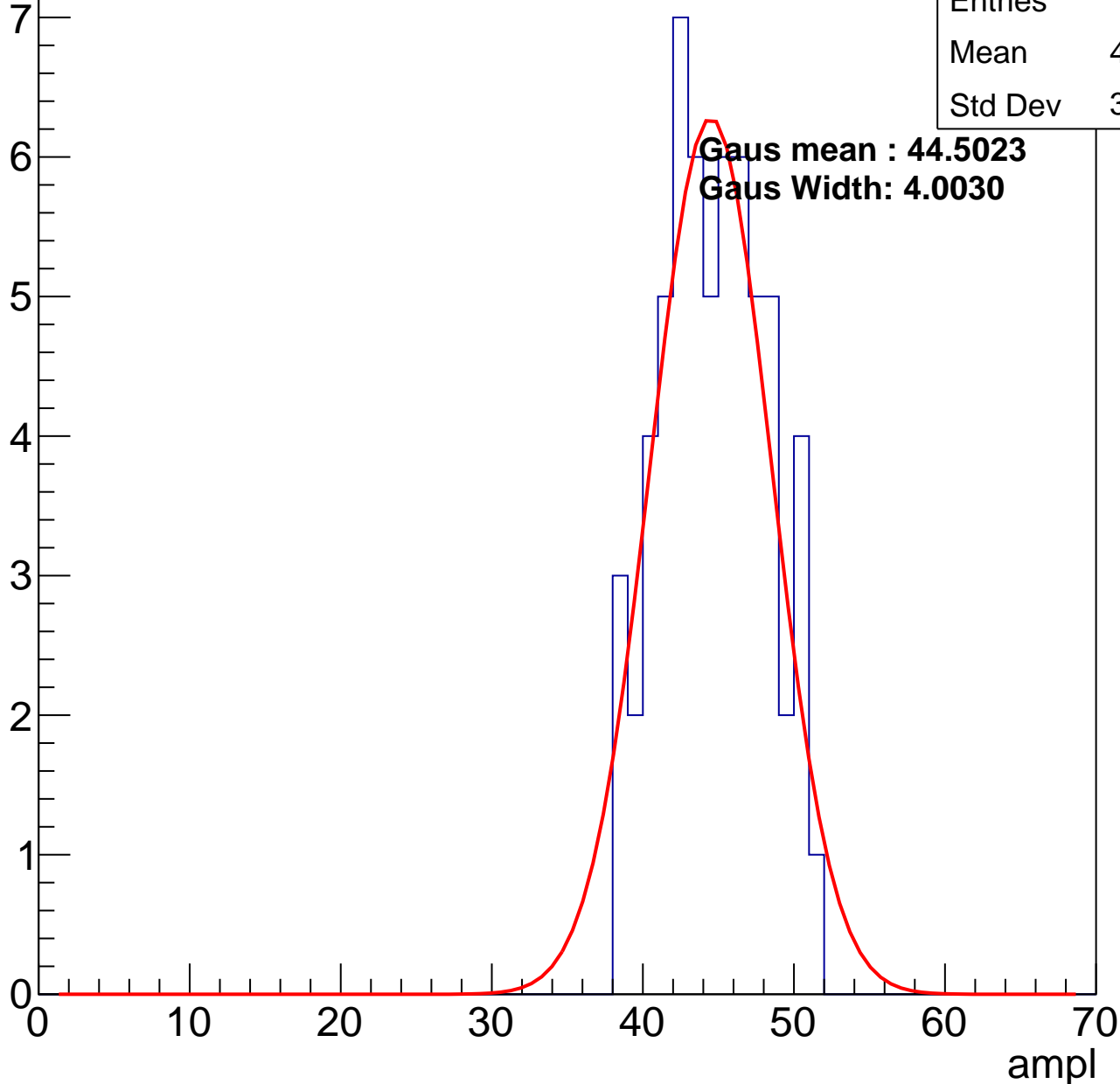


# B0L001S, U5-ch110, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	44.25
Std Dev	3.376

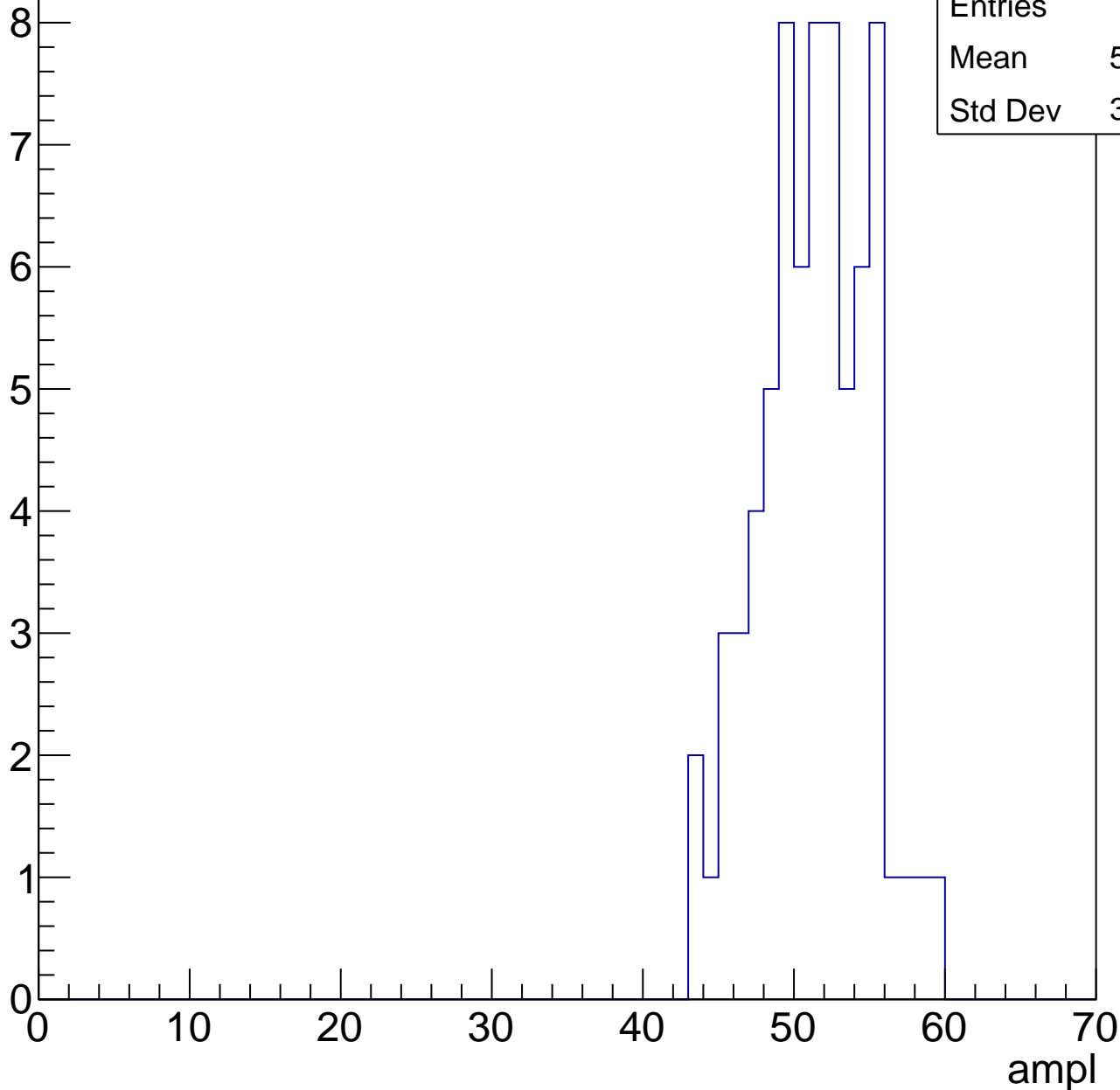


# B0L001S, U5-ch110, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	50.79
Std Dev	3.536

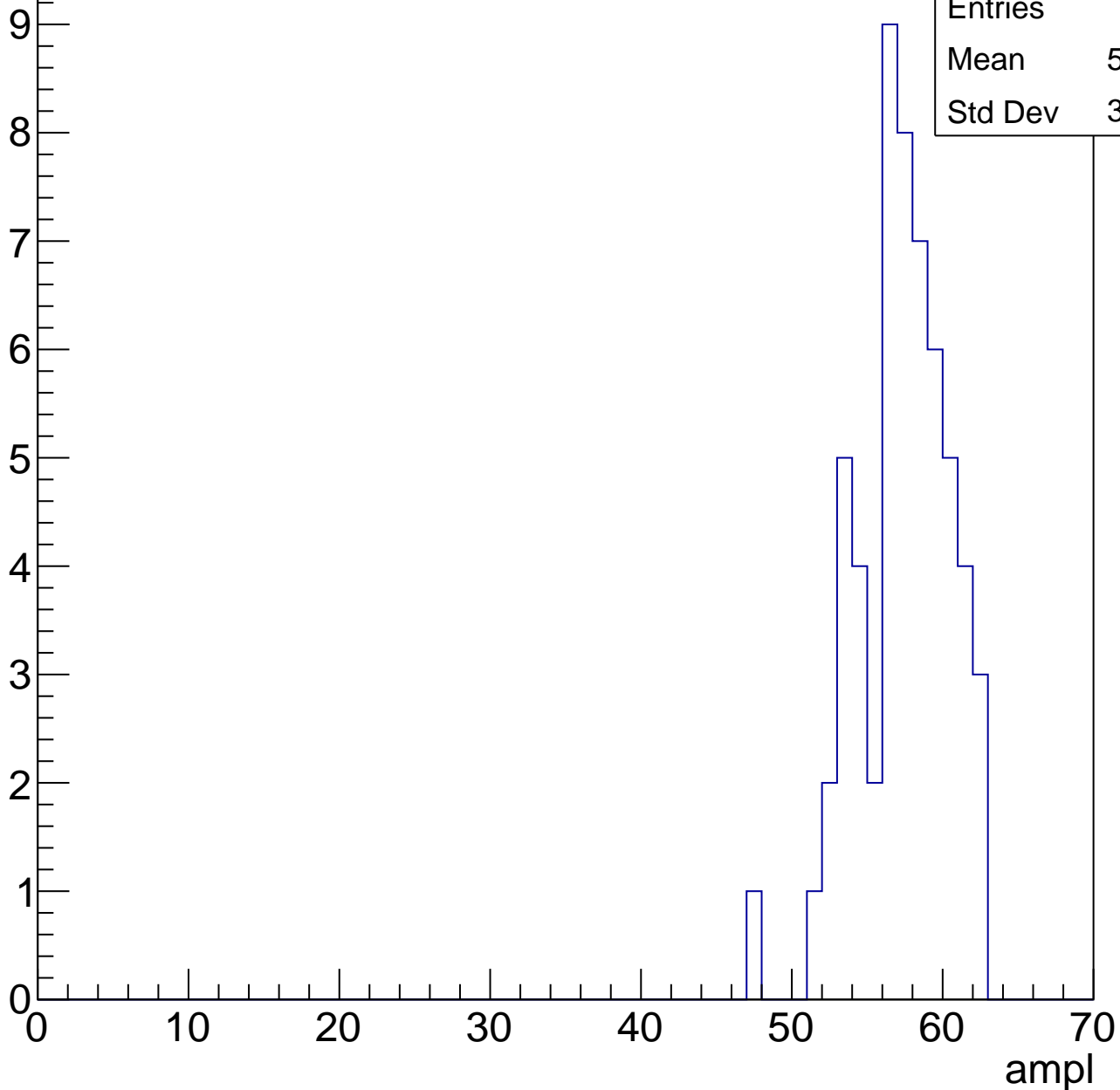


# B0L001S, U5-ch110, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	56.89
Std Dev	3.059

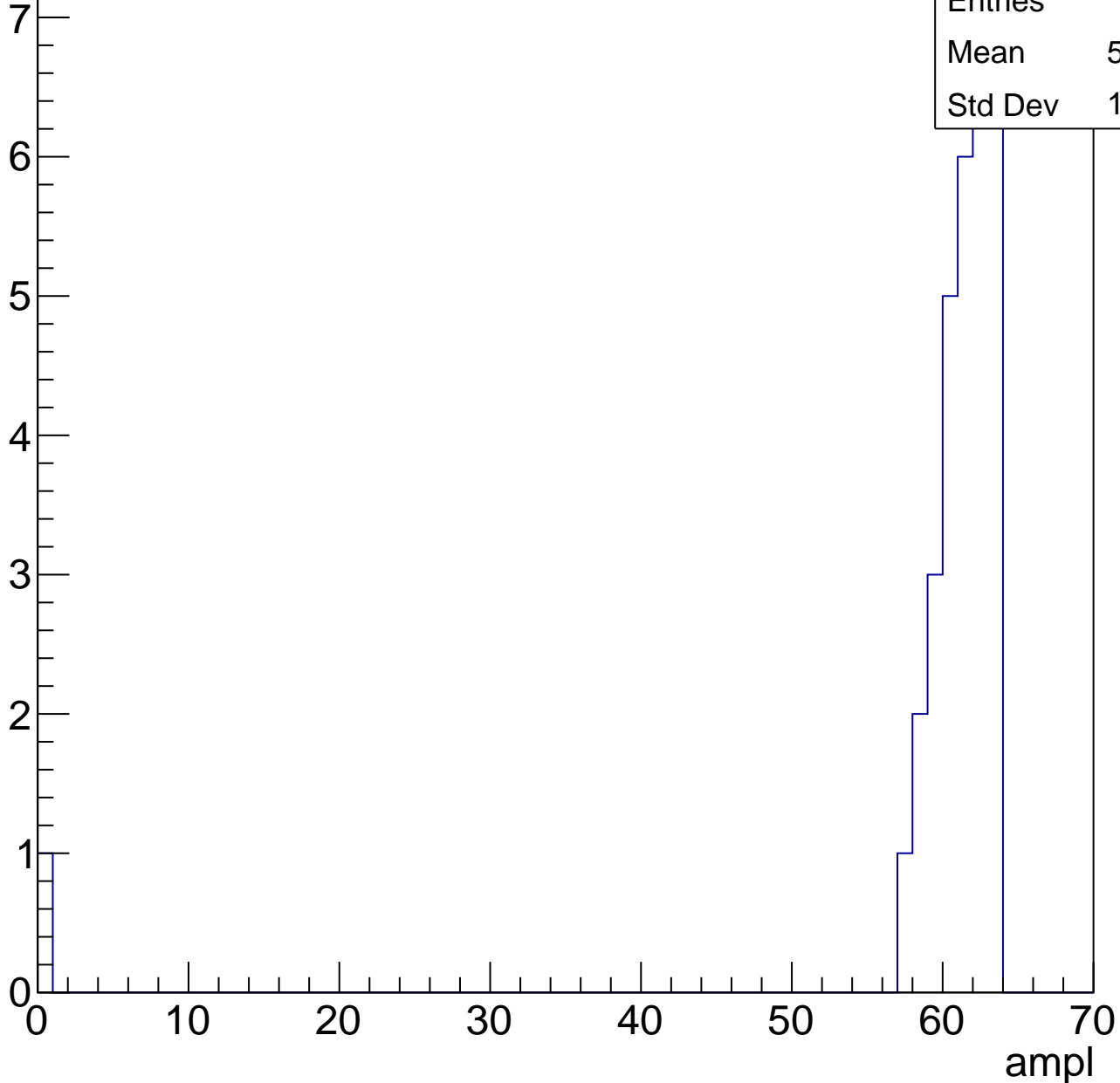


# B0L001S, U5-ch110, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	32
Mean	59.09
Std Dev	10.74



# B0L001S, U5-ch110, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch110, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch111, adc0

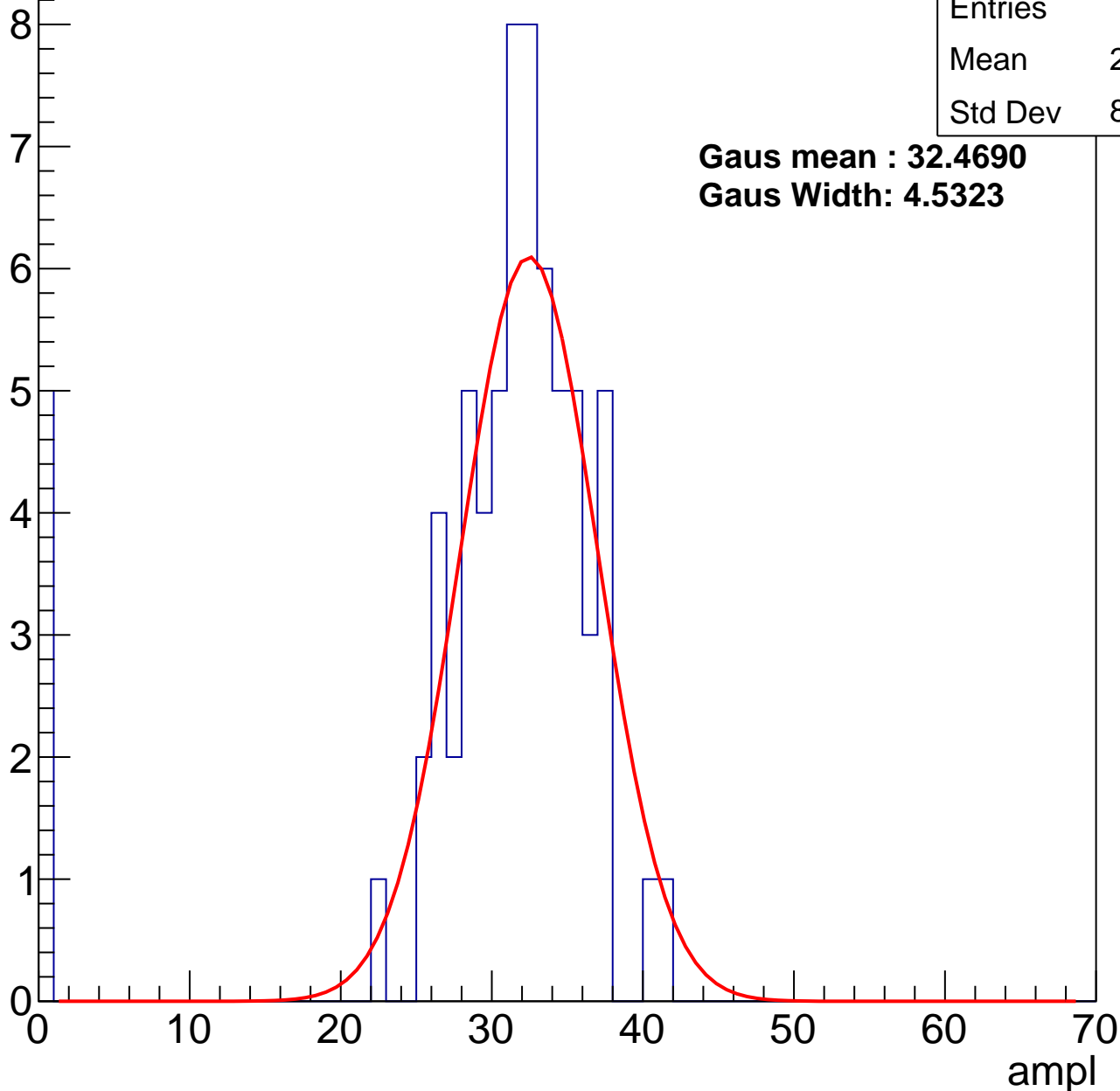
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	29.39
Std Dev	8.918

**Gaus mean : 32.4690**

**Gaus Width: 4.5323**



# B0L001S, U5-ch111, adc1

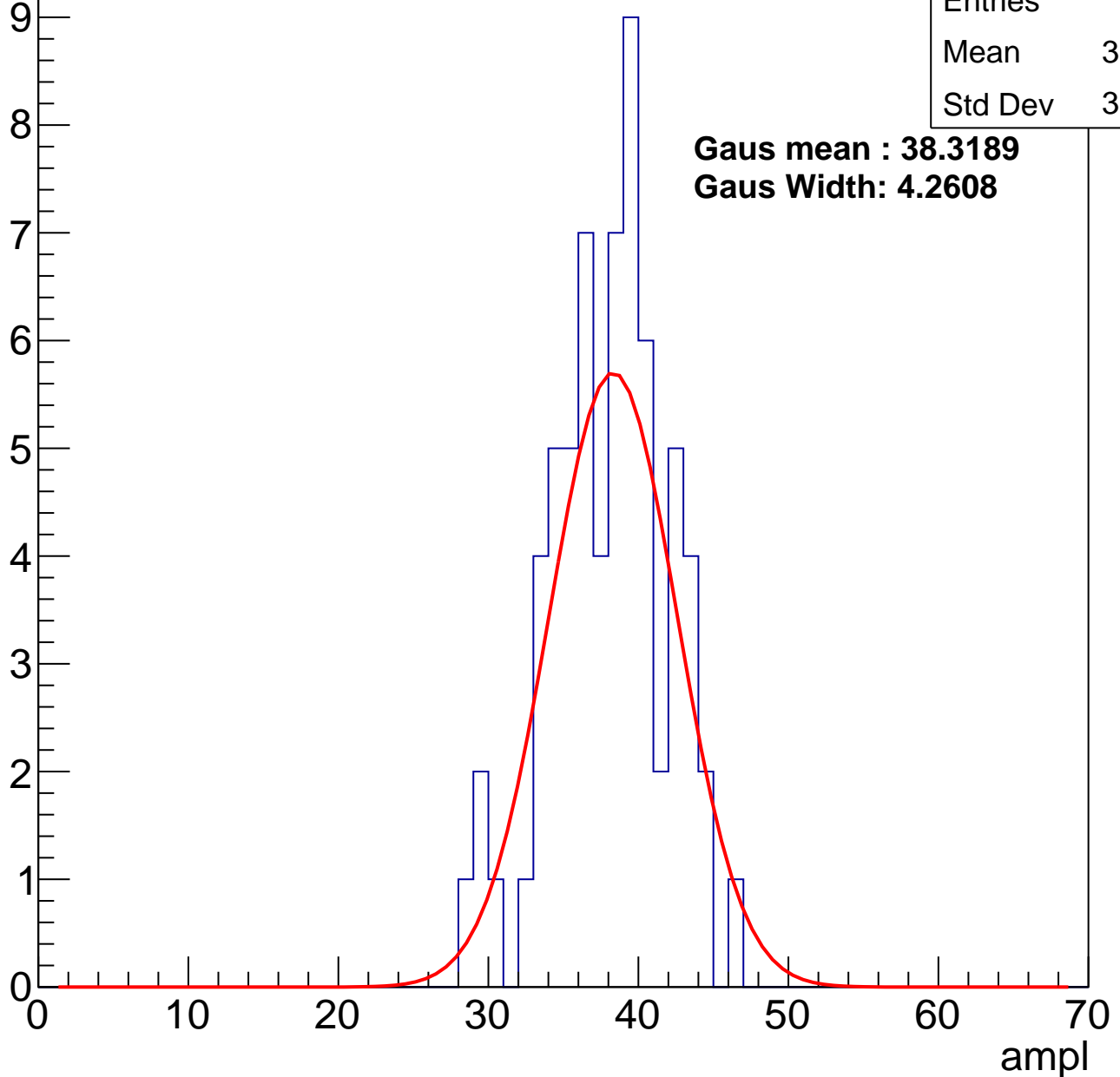
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	37.58
Std Dev	3.842

**Gaus mean : 38.3189**

**Gaus Width: 4.2608**

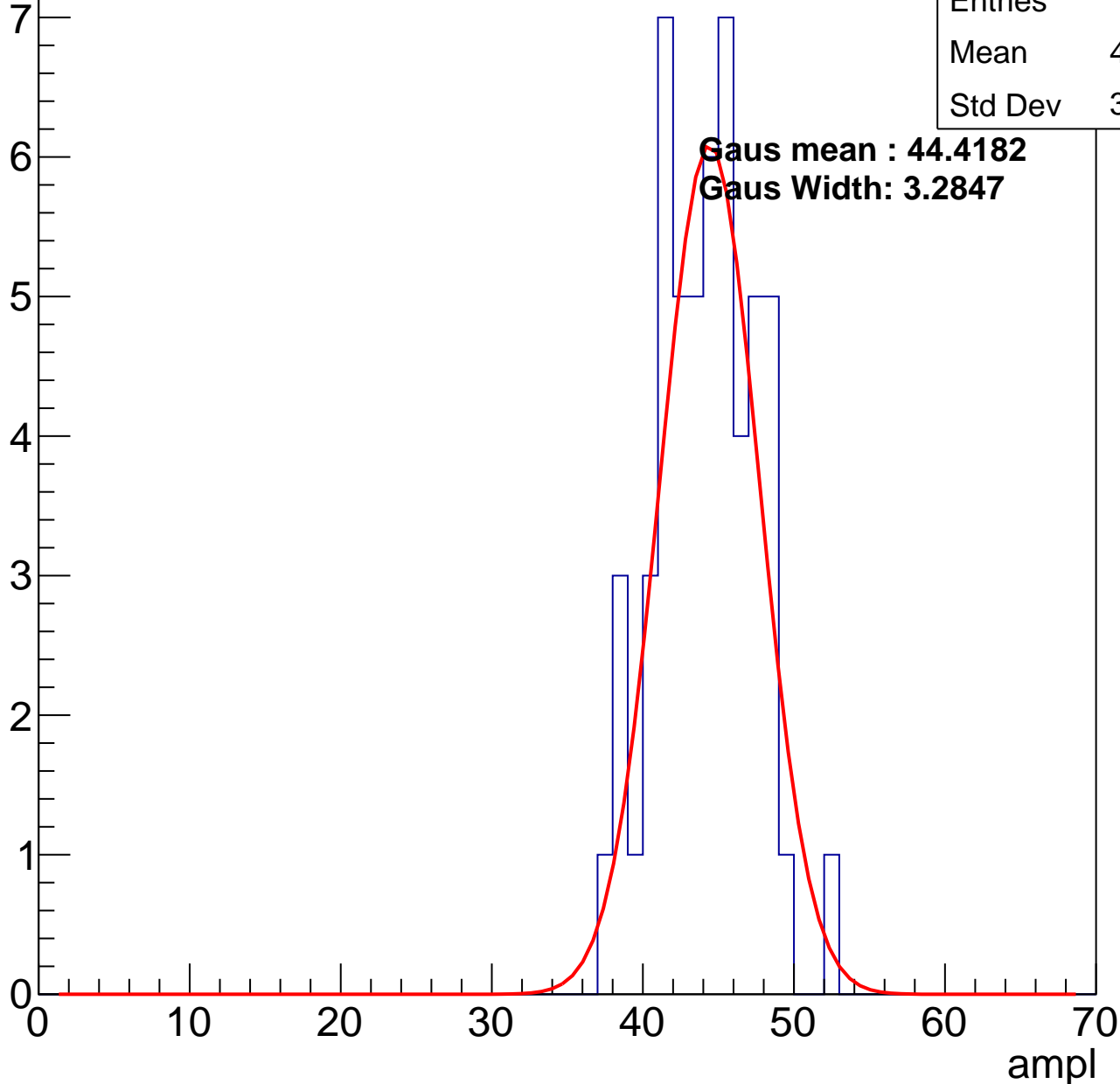


# B0L001S, U5-ch111, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

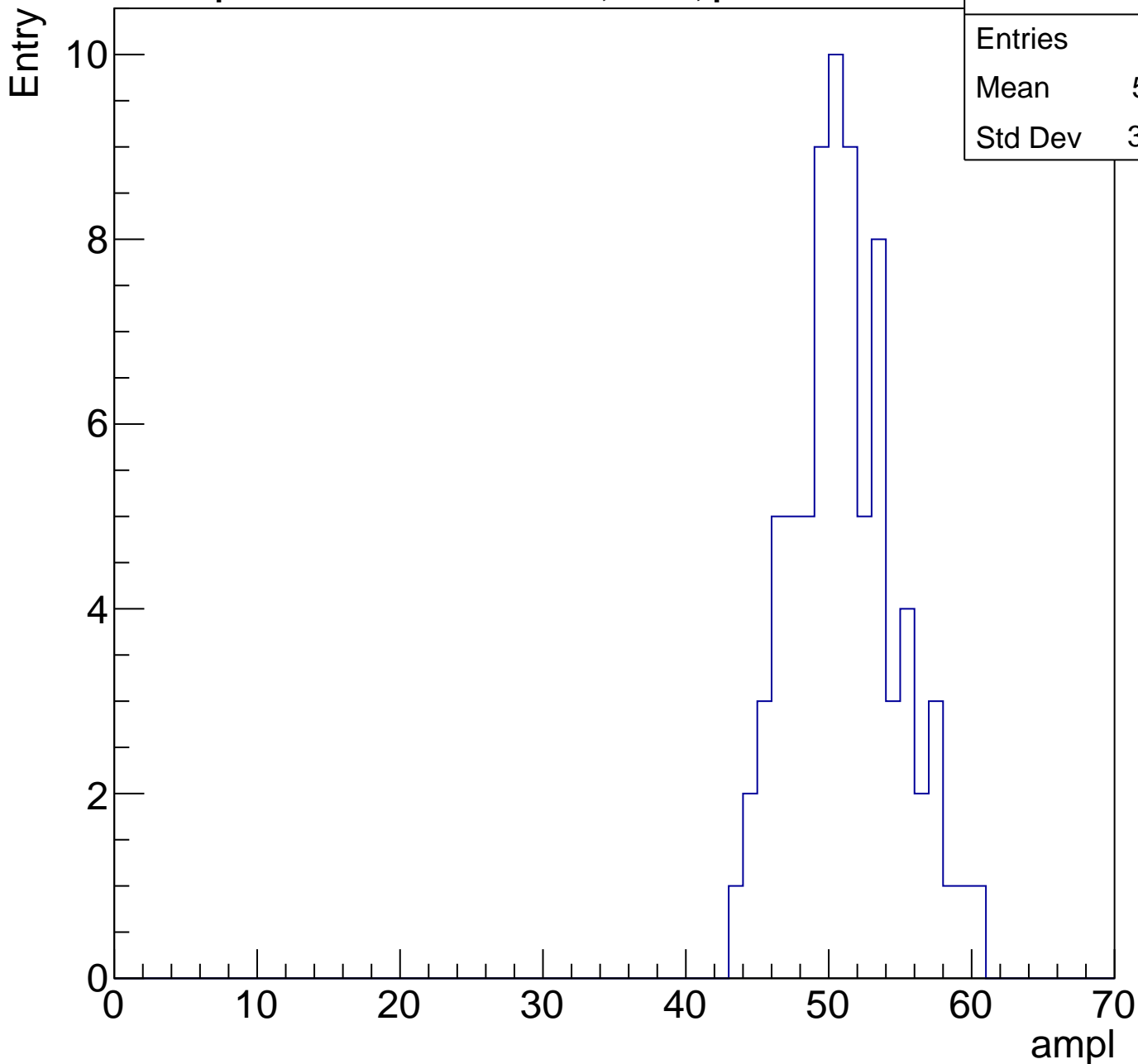
Entries	54
Mean	43.72
Std Dev	3.194



# B0L001S, U5-ch111, adc3

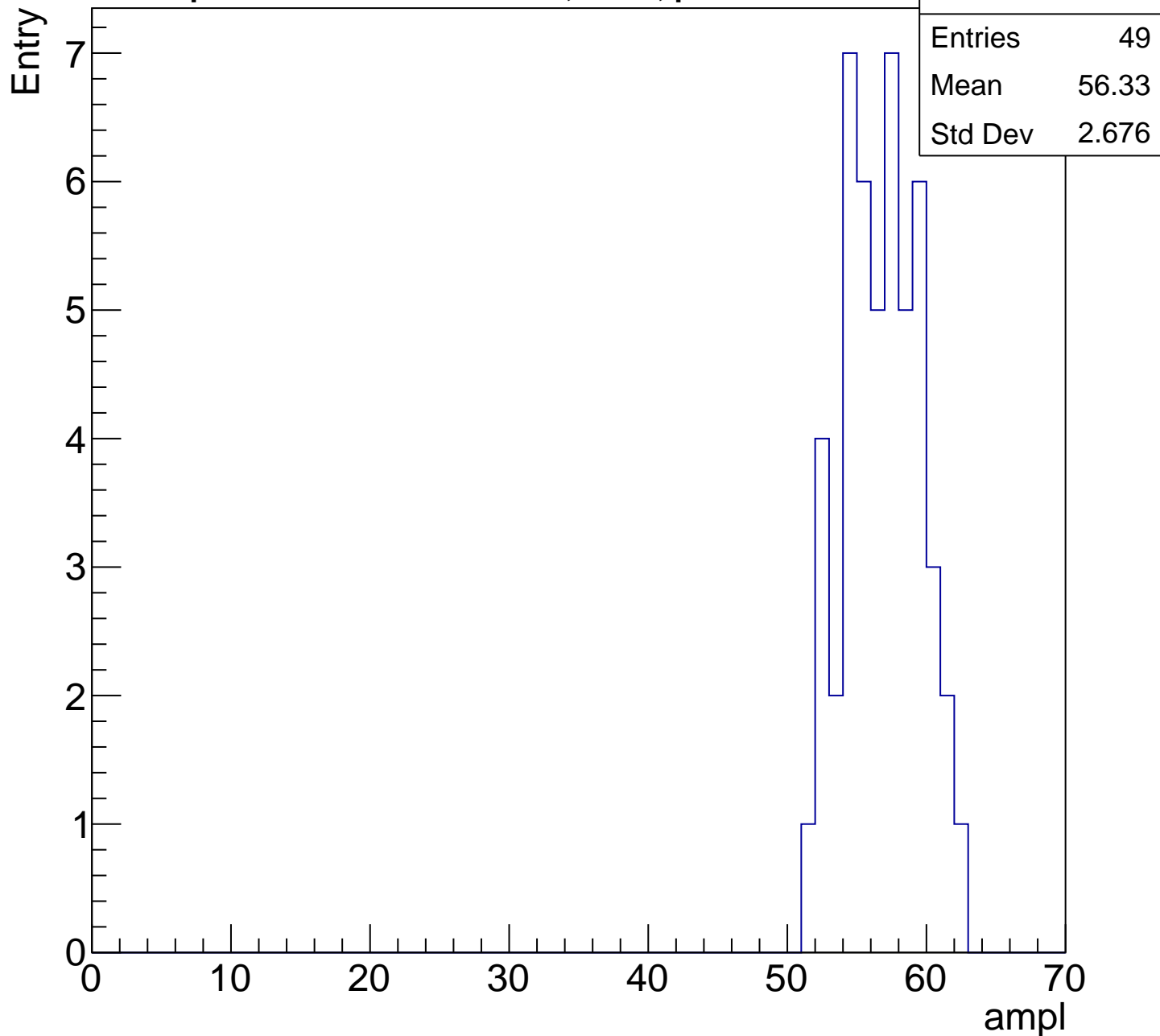
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	77
Mean	50.61
Std Dev	3.665



# B0L001S, U5-ch111, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

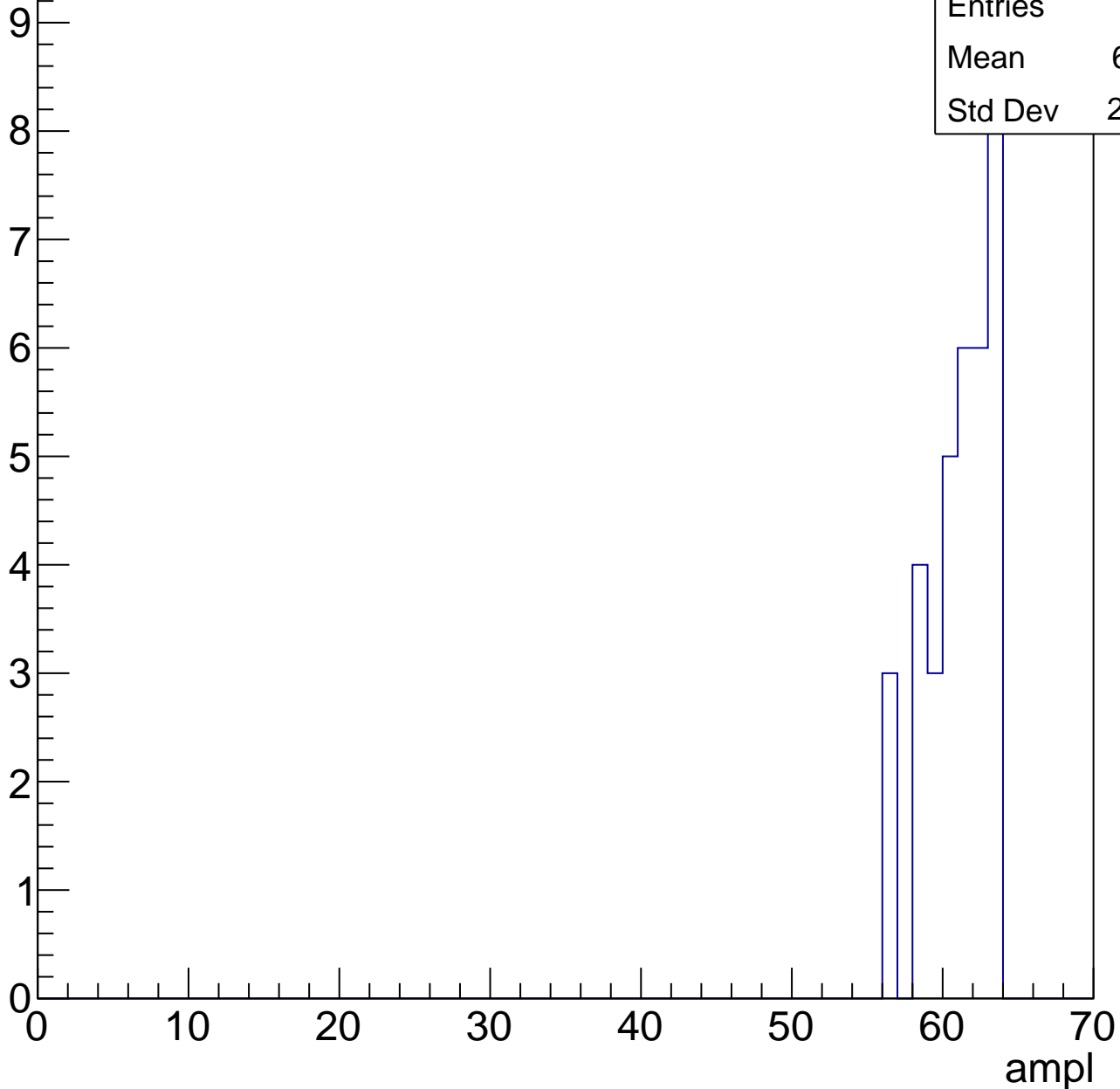


# B0L001S, U5-ch111, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

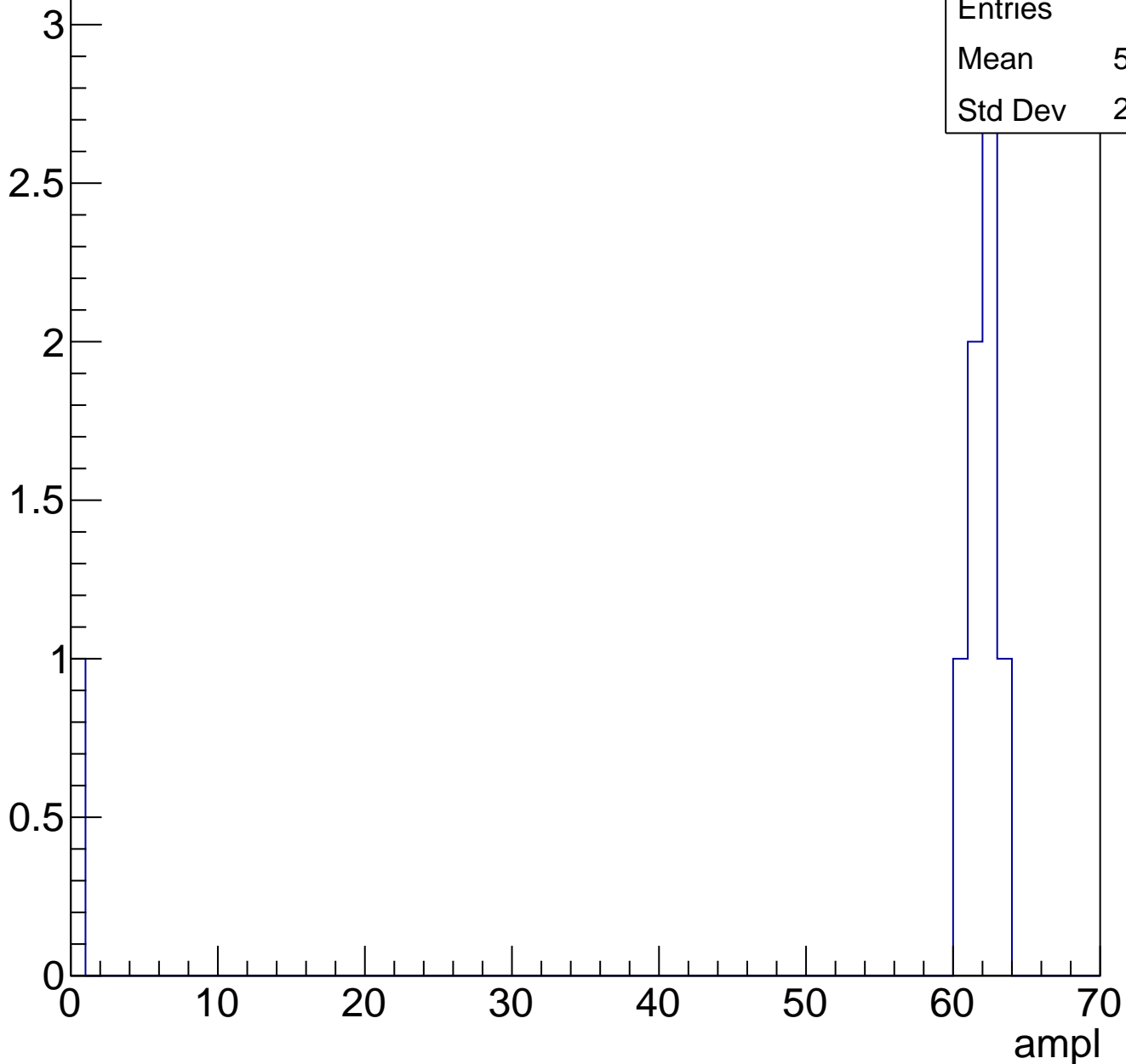
Entries	36
Mean	60.61
Std Dev	2.138



# B0L001S, U5-ch111, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch111, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch112, adc0

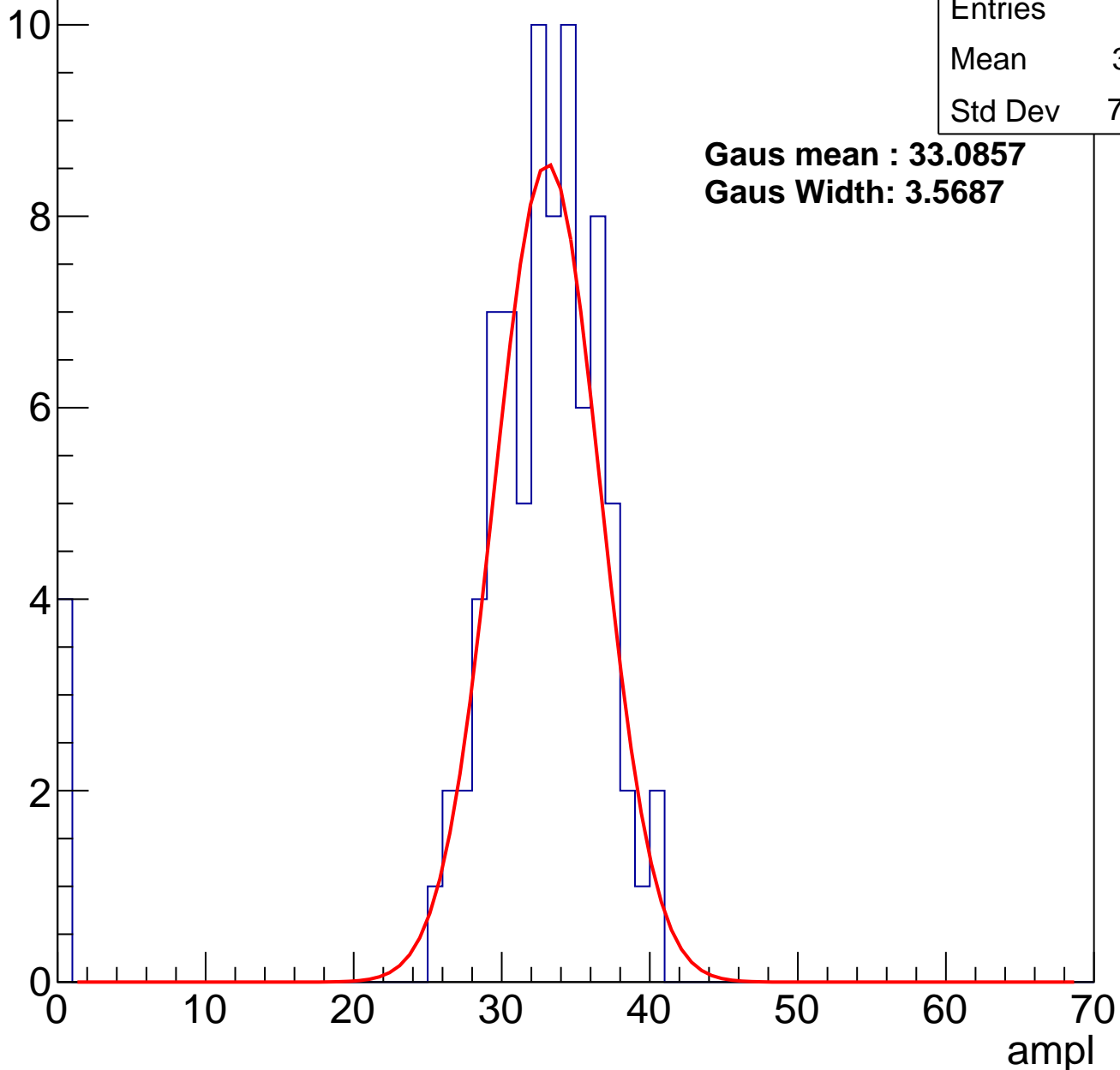
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	84
Mean	31.11
Std Dev	7.687

**Gaus mean : 33.0857**

**Gaus Width: 3.5687**

Entry



# B0L001S, U5-ch112, adc1

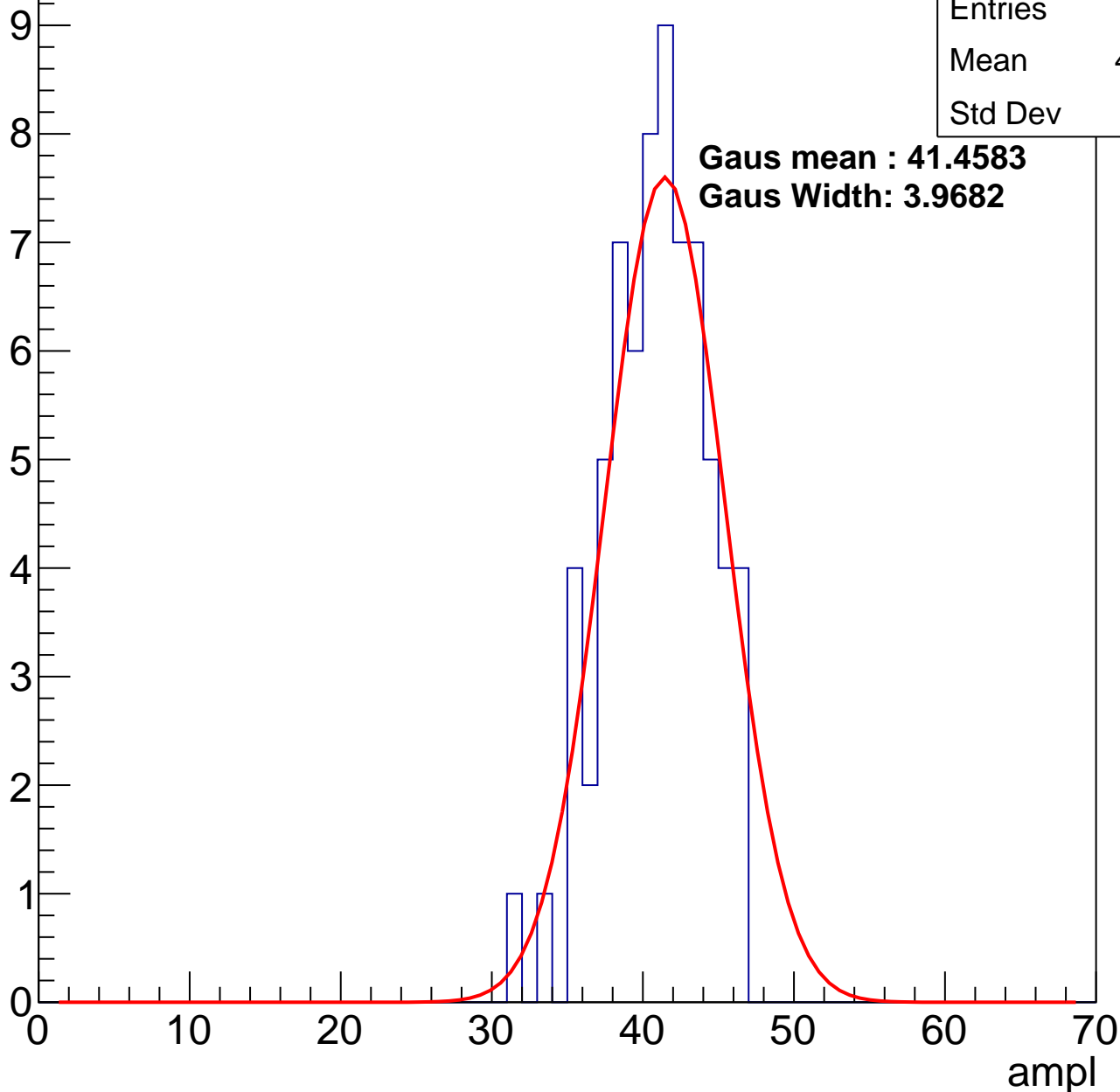
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	40.41
Std Dev	3.28

**Gaus mean : 41.4583**

**Gaus Width: 3.9682**



# B0L001S, U5-ch112, adc2

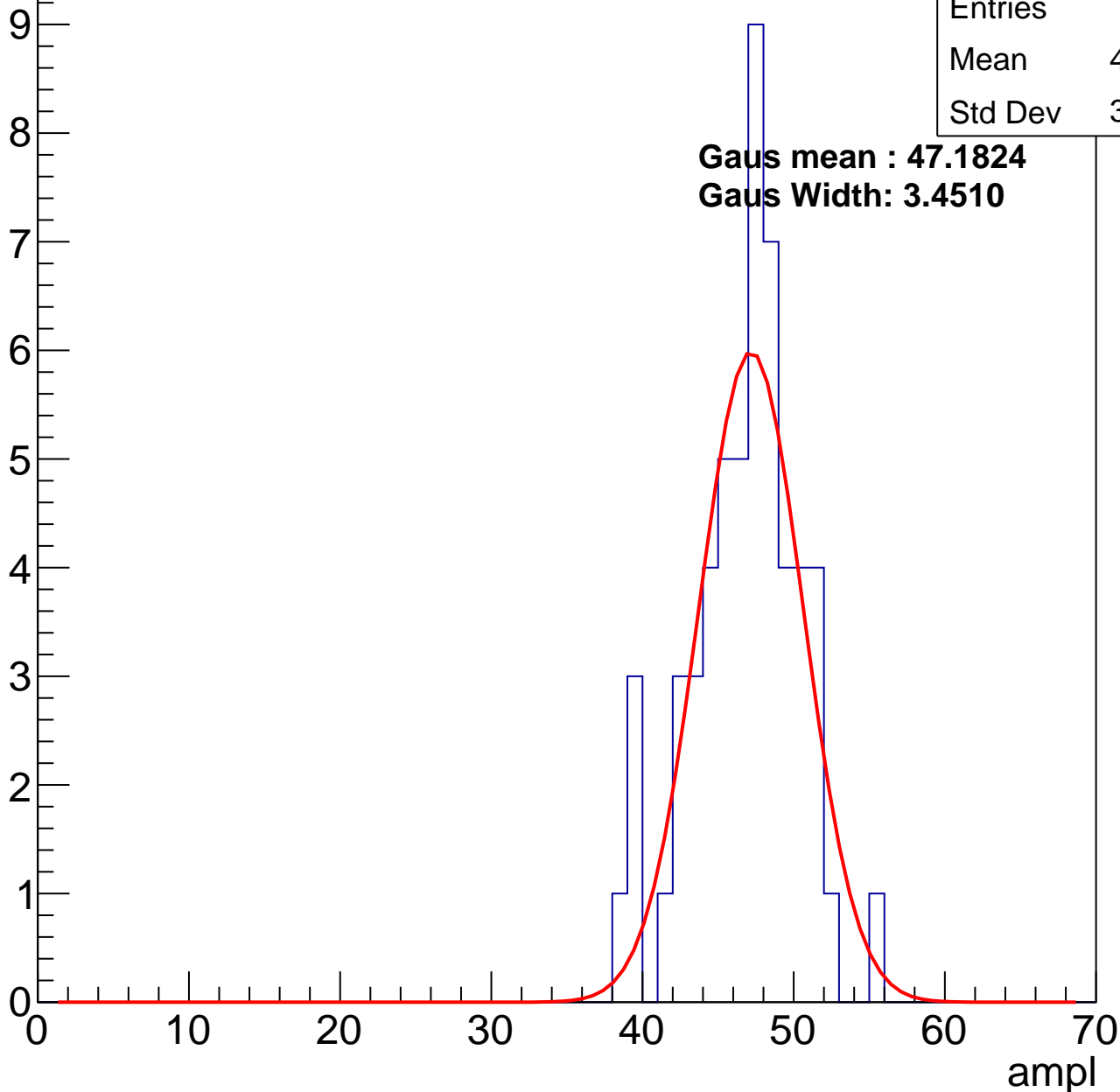
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	46.33
Std Dev	3.516

**Gaus mean : 47.1824**

**Gaus Width: 3.4510**

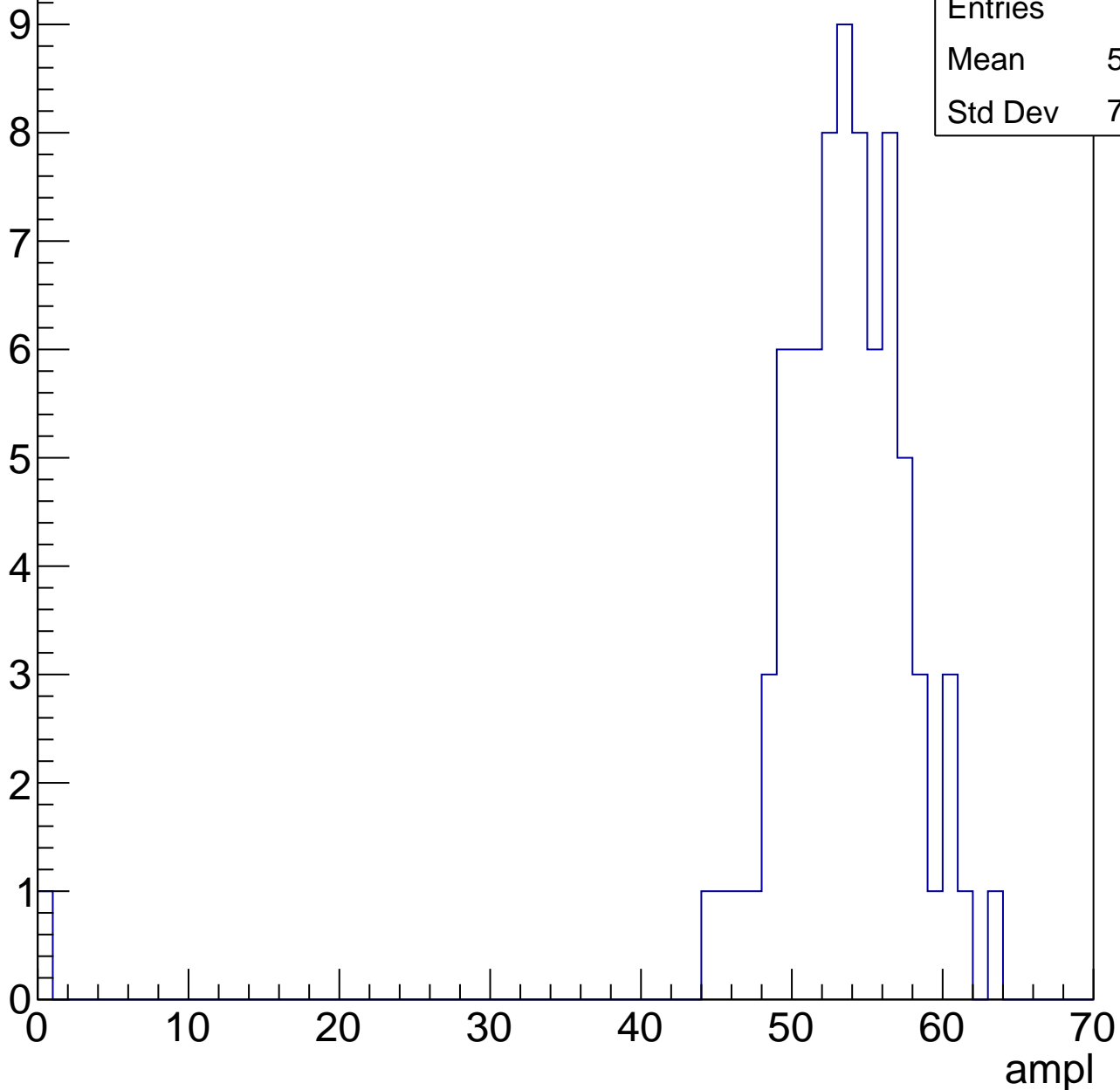


# B0L001S, U5-ch112, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

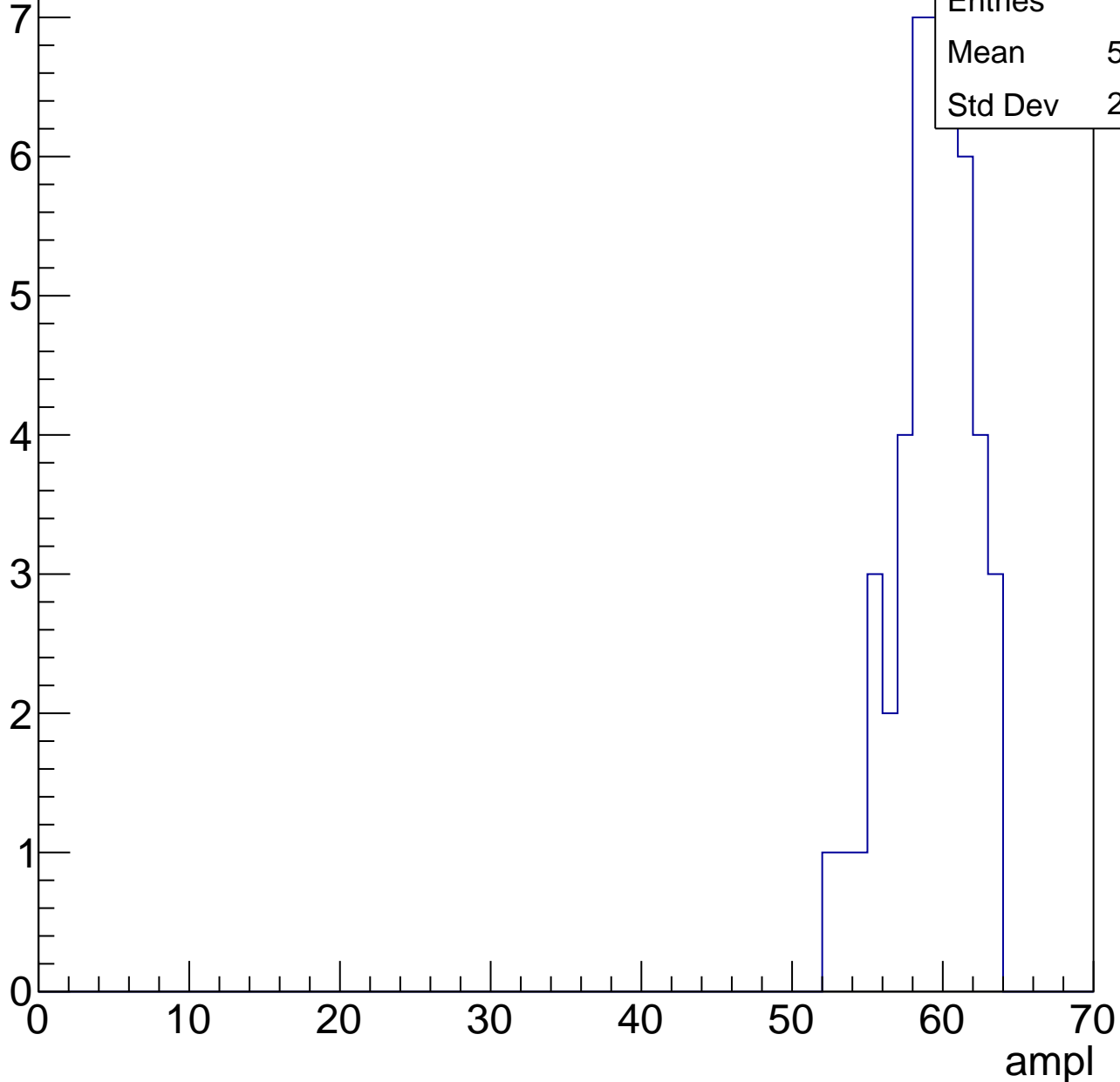
Entries	79
Mean	52.54
Std Dev	7.013



# B0L001S, U5-ch112, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

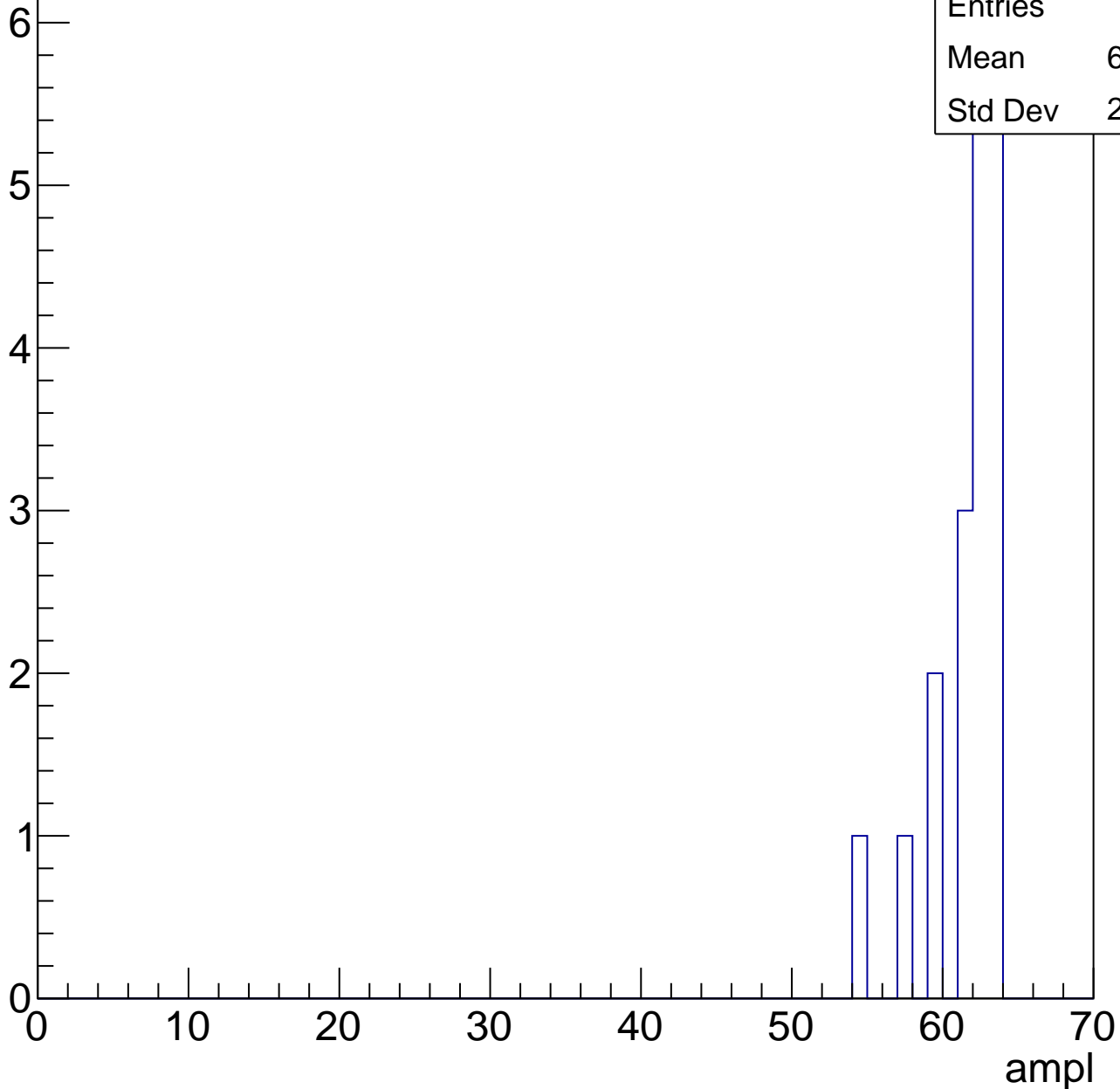


# B0L001S, U5-ch112, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	19
Mean	61.16
Std Dev	2.323



# B0L001S, U5-ch112, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U5-ch112, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	3
Mean	0
Std Dev	0

# B0L001S, U5-ch113, adc0

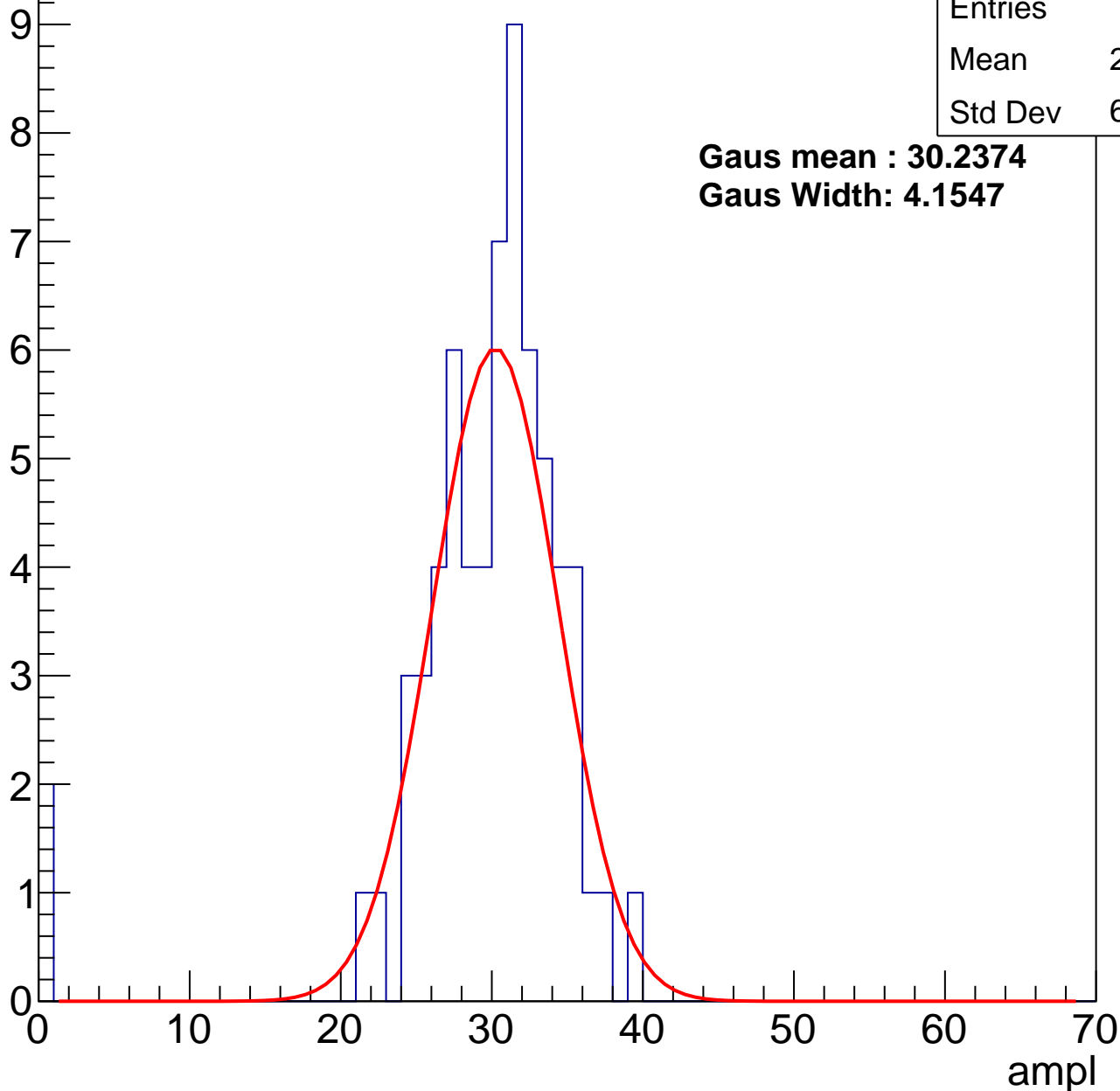
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	29.06
Std Dev	6.295

**Gaus mean : 30.2374**

**Gaus Width: 4.1547**



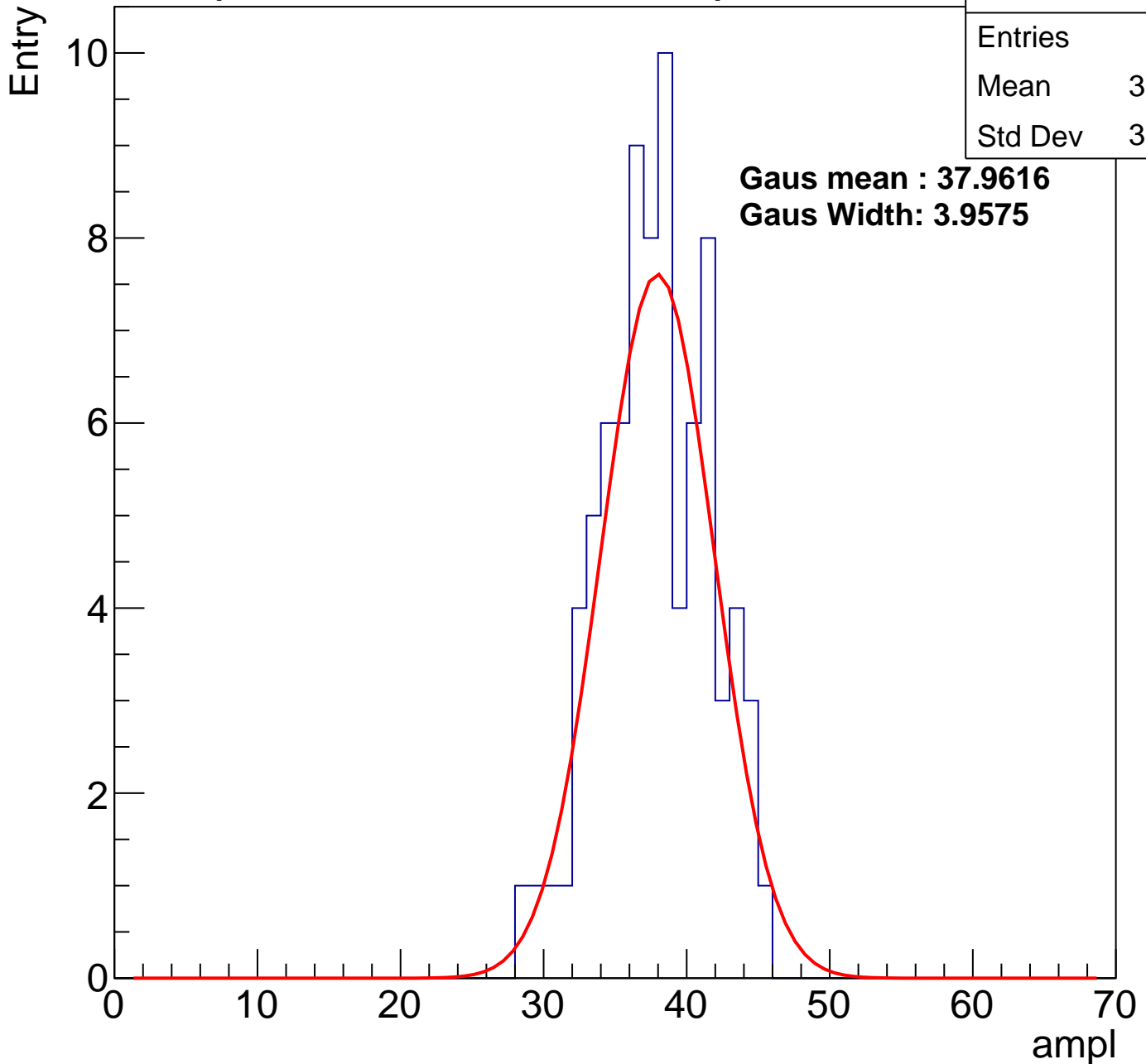
# B0L001S, U5-ch113, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	81
Mean	37.33
Std Dev	3.728

**Gaus mean : 37.9616**

**Gaus Width: 3.9575**



# B0L001S, U5-ch113, adc2

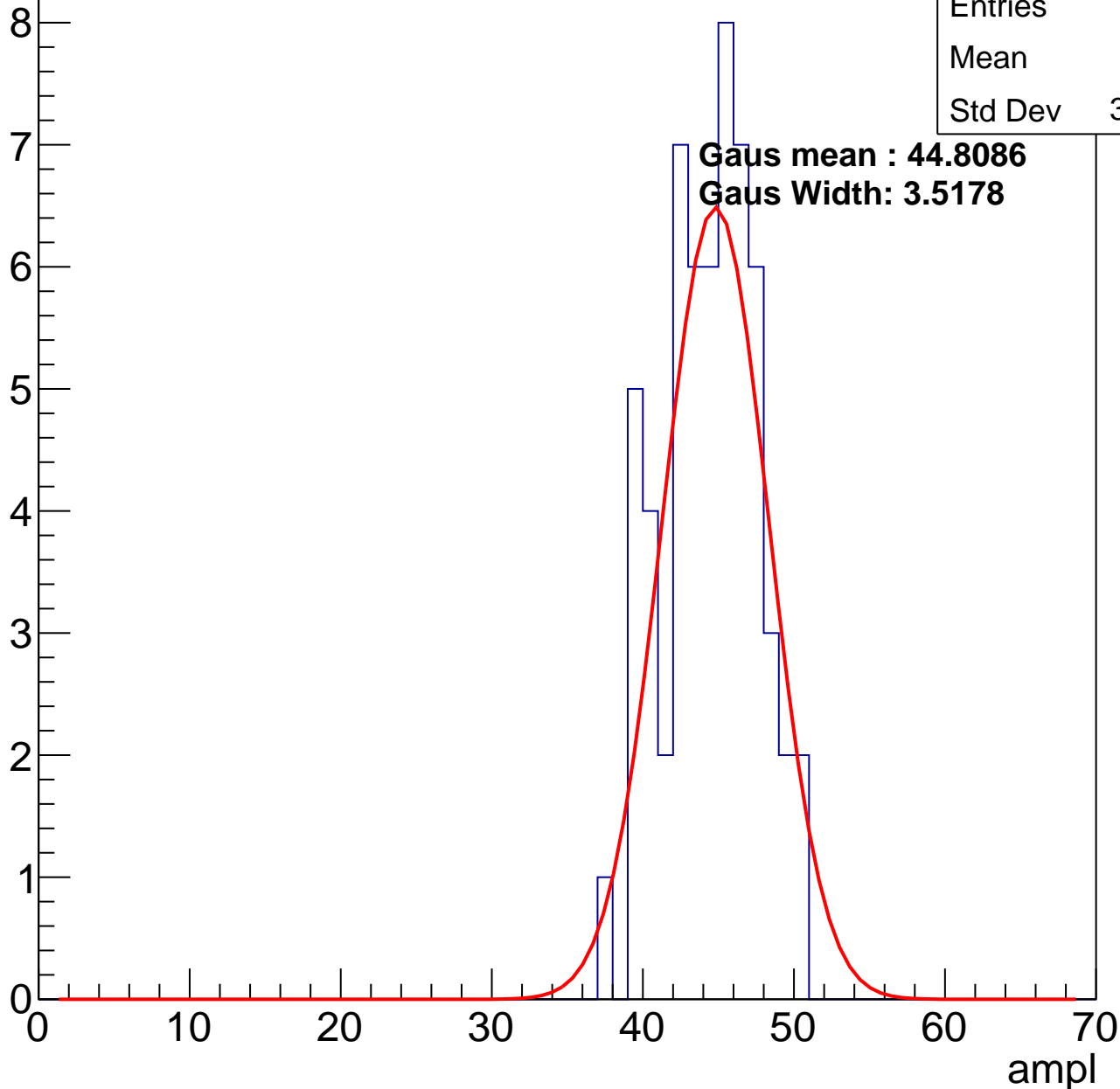
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	44
Std Dev	3.053

**Gaus mean : 44.8086**

**Gaus Width: 3.5178**



# B0L001S, U5-ch113, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	74
Mean	51.07
Std Dev	3.033

Entry

10

8

6

4

2

0

0

10

20

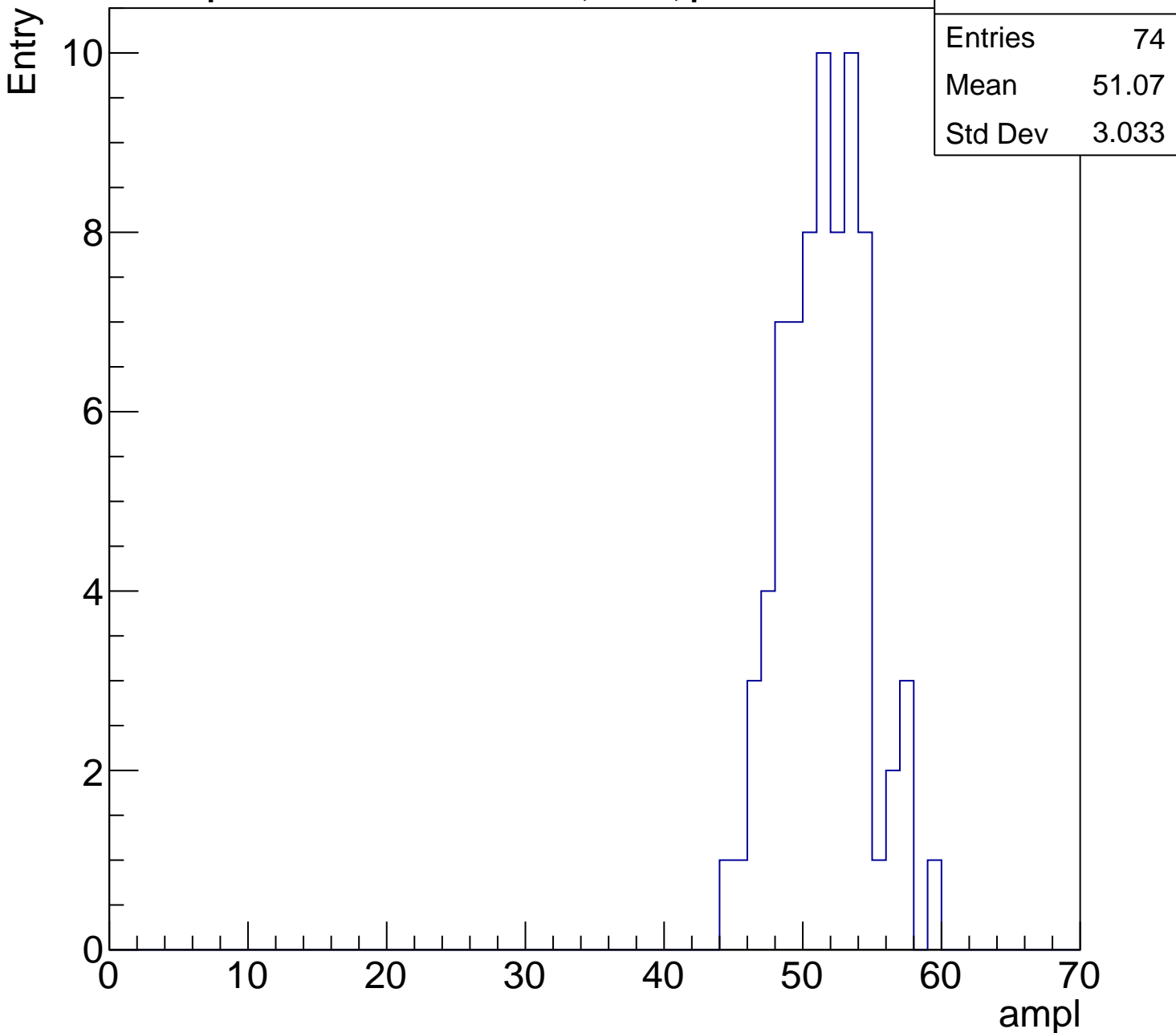
30

40

50

60

ampl

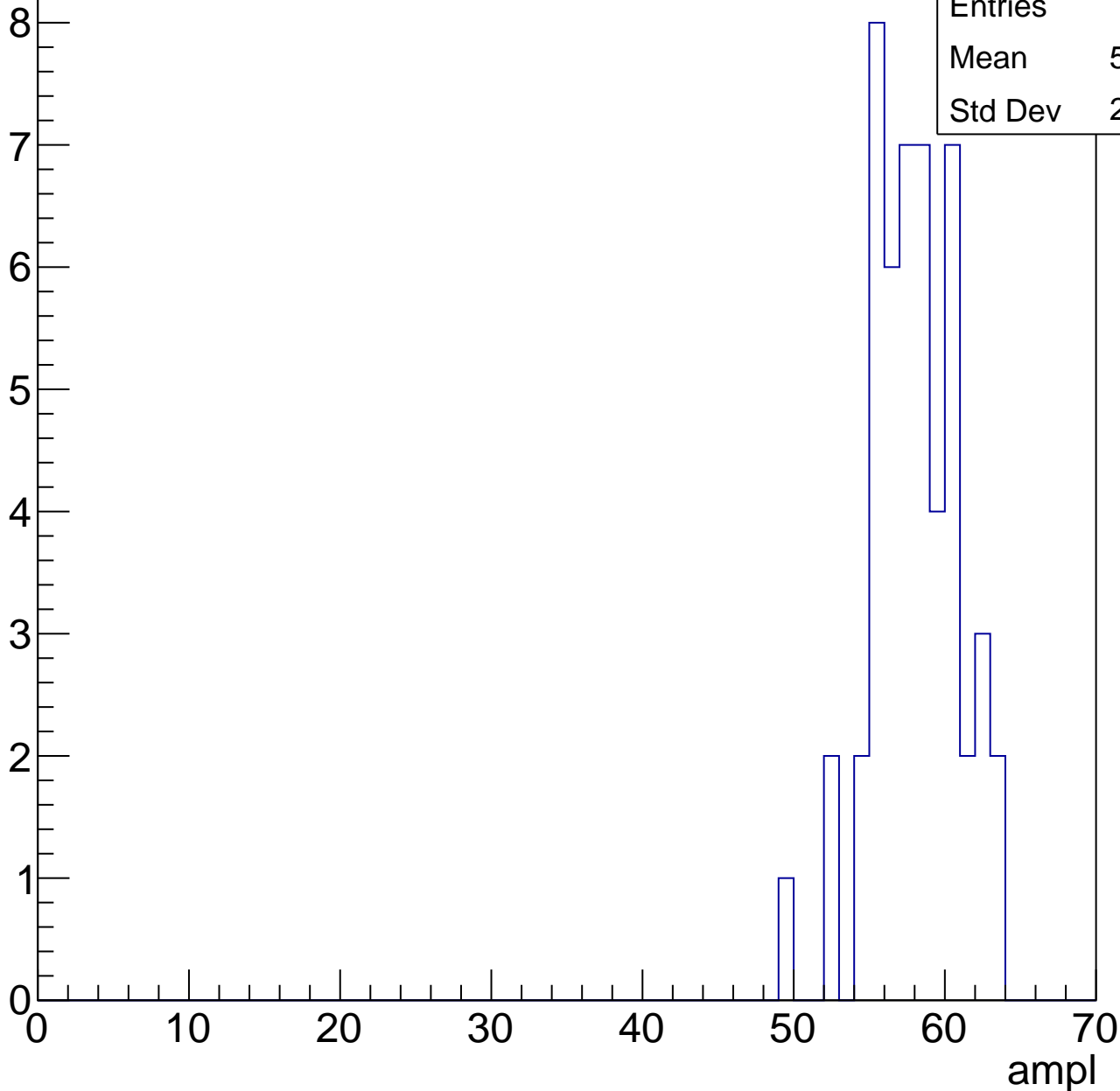


# B0L001S, U5-ch113, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	51
Mean	57.49
Std Dev	2.879

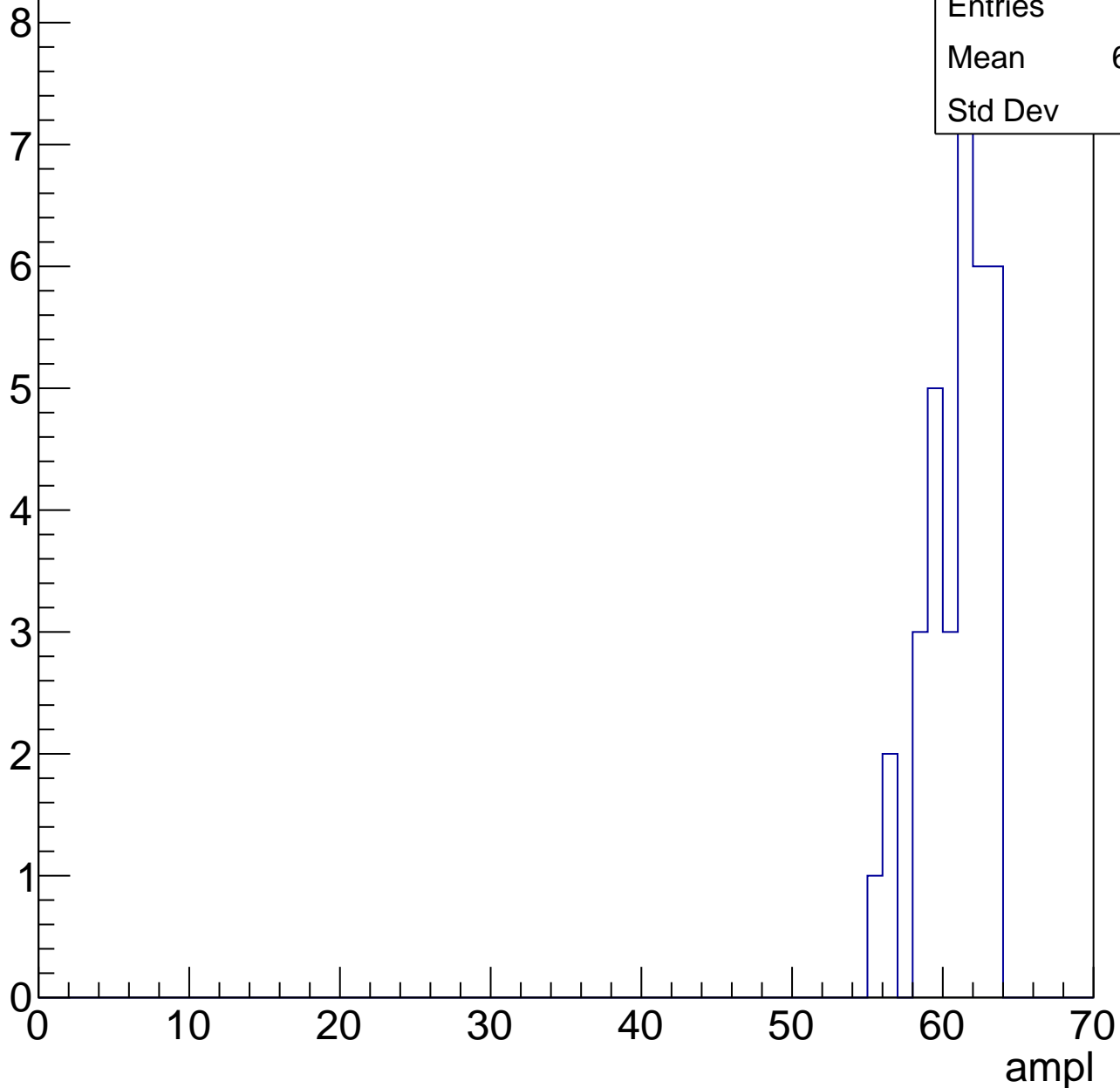


# B0L001S, U5-ch113, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	34
Mean	60.41
Std Dev	2.13



# B0L001S, U5-ch113, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch113, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch114, adc0

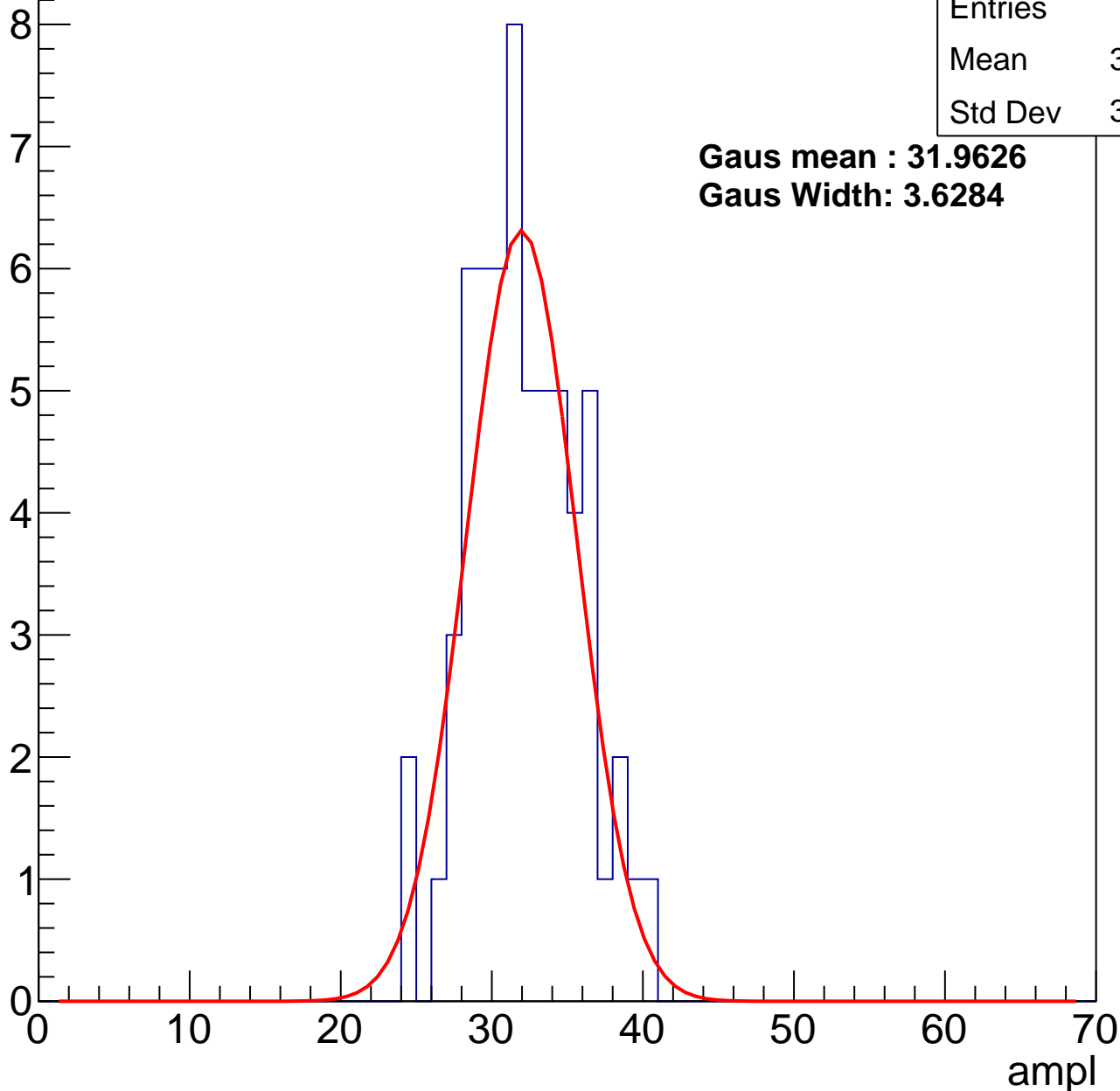
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	31.67
Std Dev	3.542

**Gaus mean : 31.9626**

**Gaus Width: 3.6284**



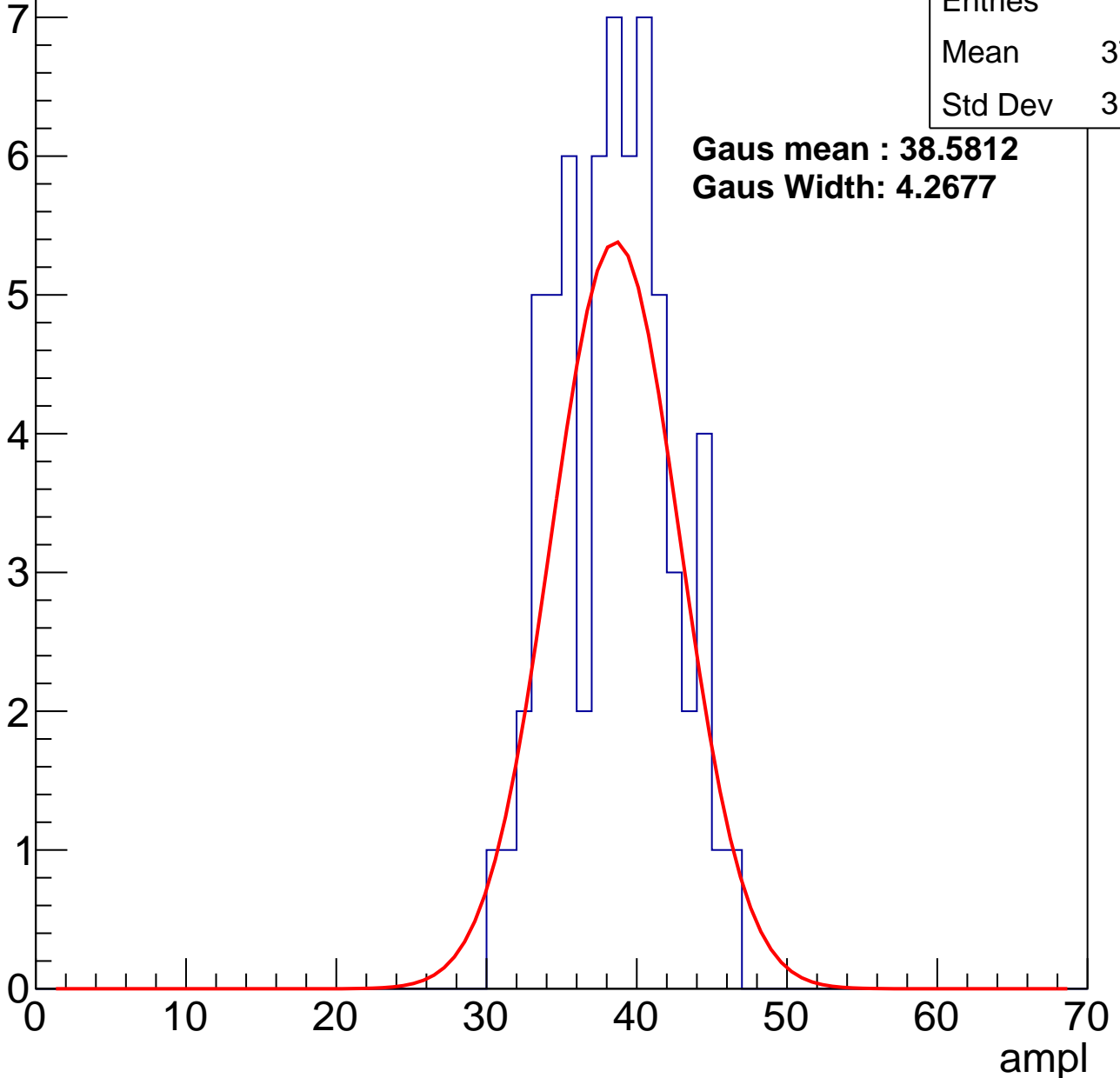
# B0L001S, U5-ch114, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	37.94
Std Dev	3.733

**Gaus mean : 38.5812**  
**Gaus Width: 4.2677**



# B0L001S, U5-ch114, adc2

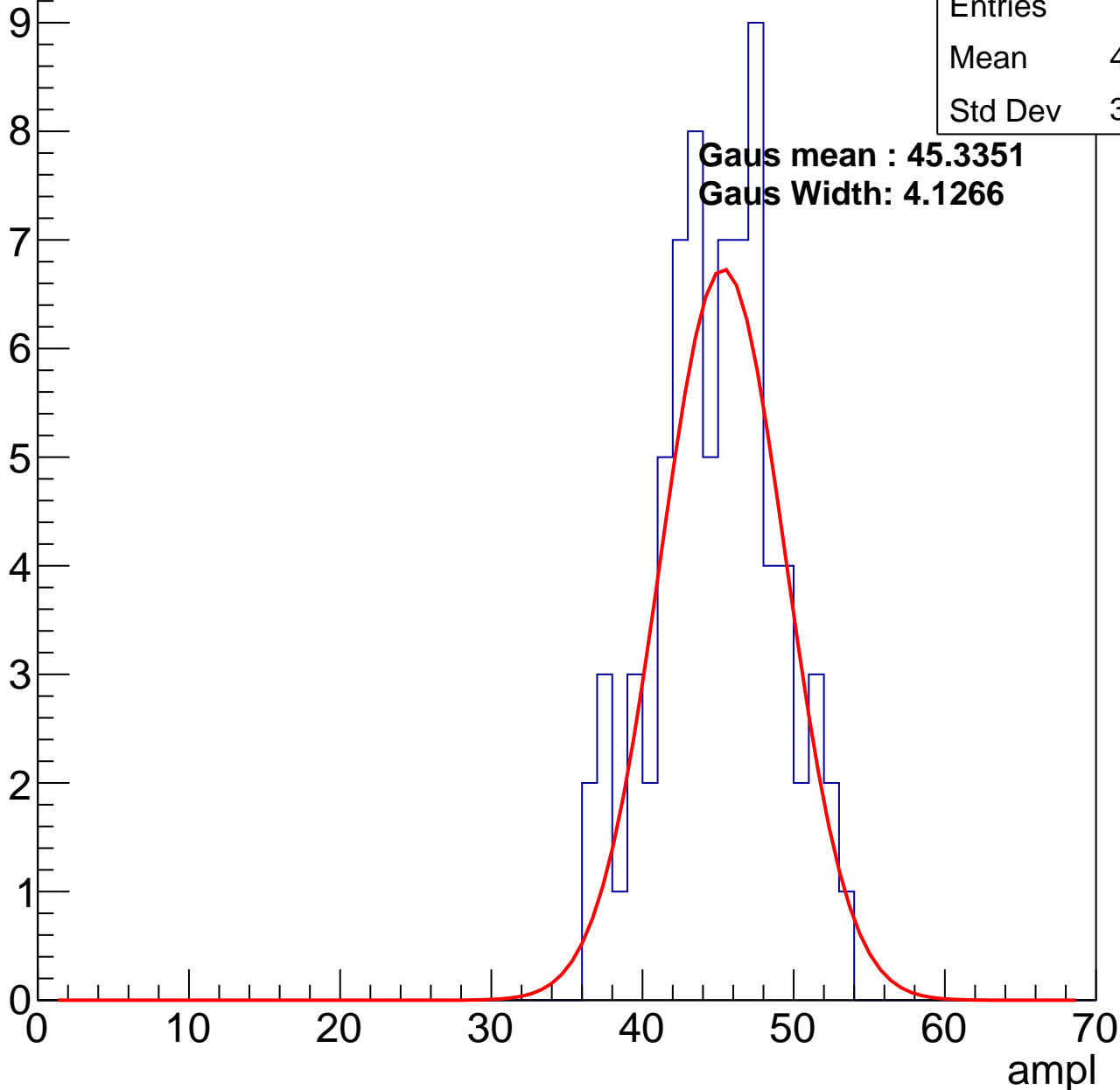
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	75
Mean	44.52
Std Dev	3.978

**Gaus mean : 45.3351**

**Gaus Width: 4.1266**

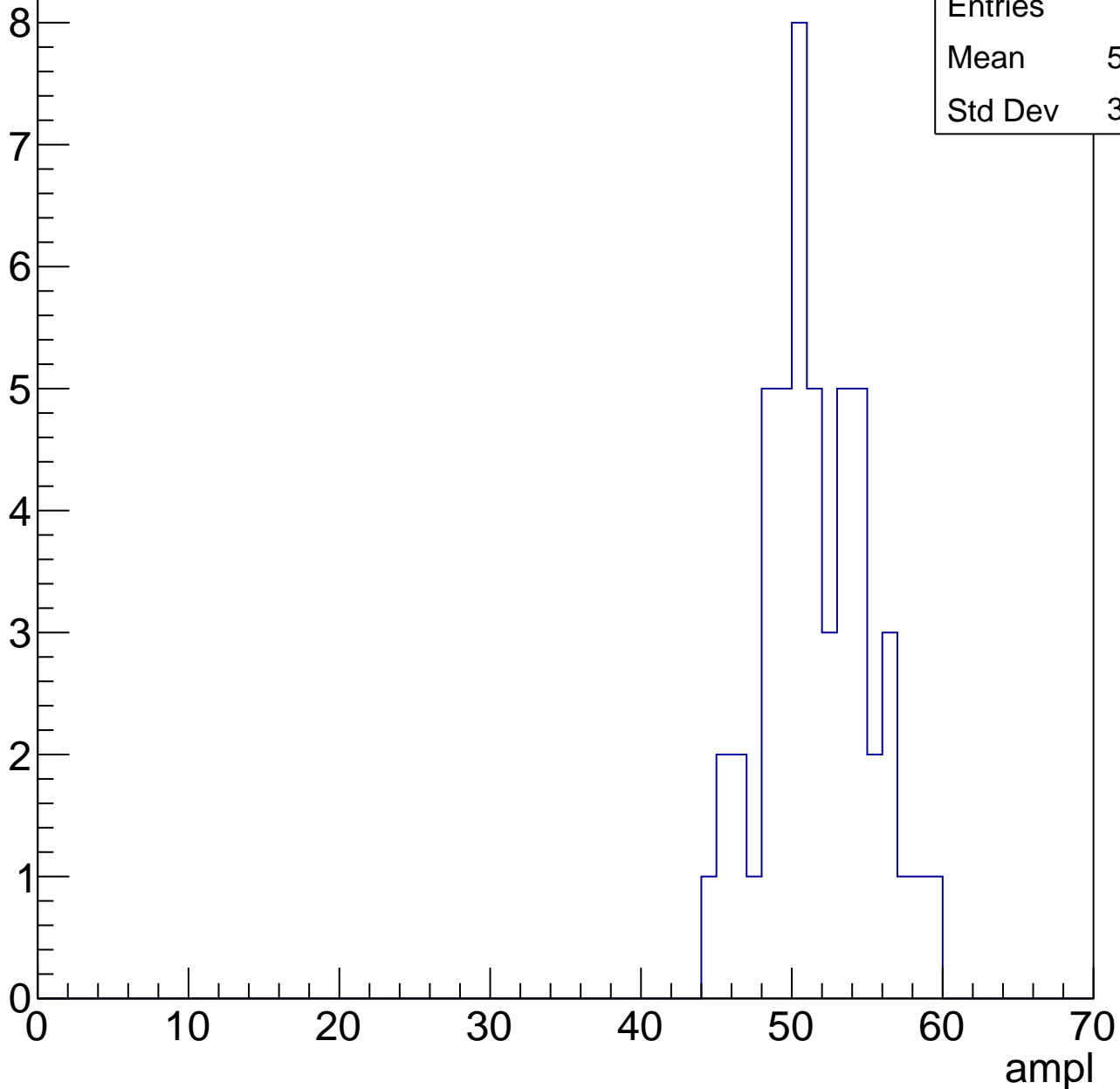


# B0L001S, U5-ch114, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	50
Mean	51.12
Std Dev	3.415

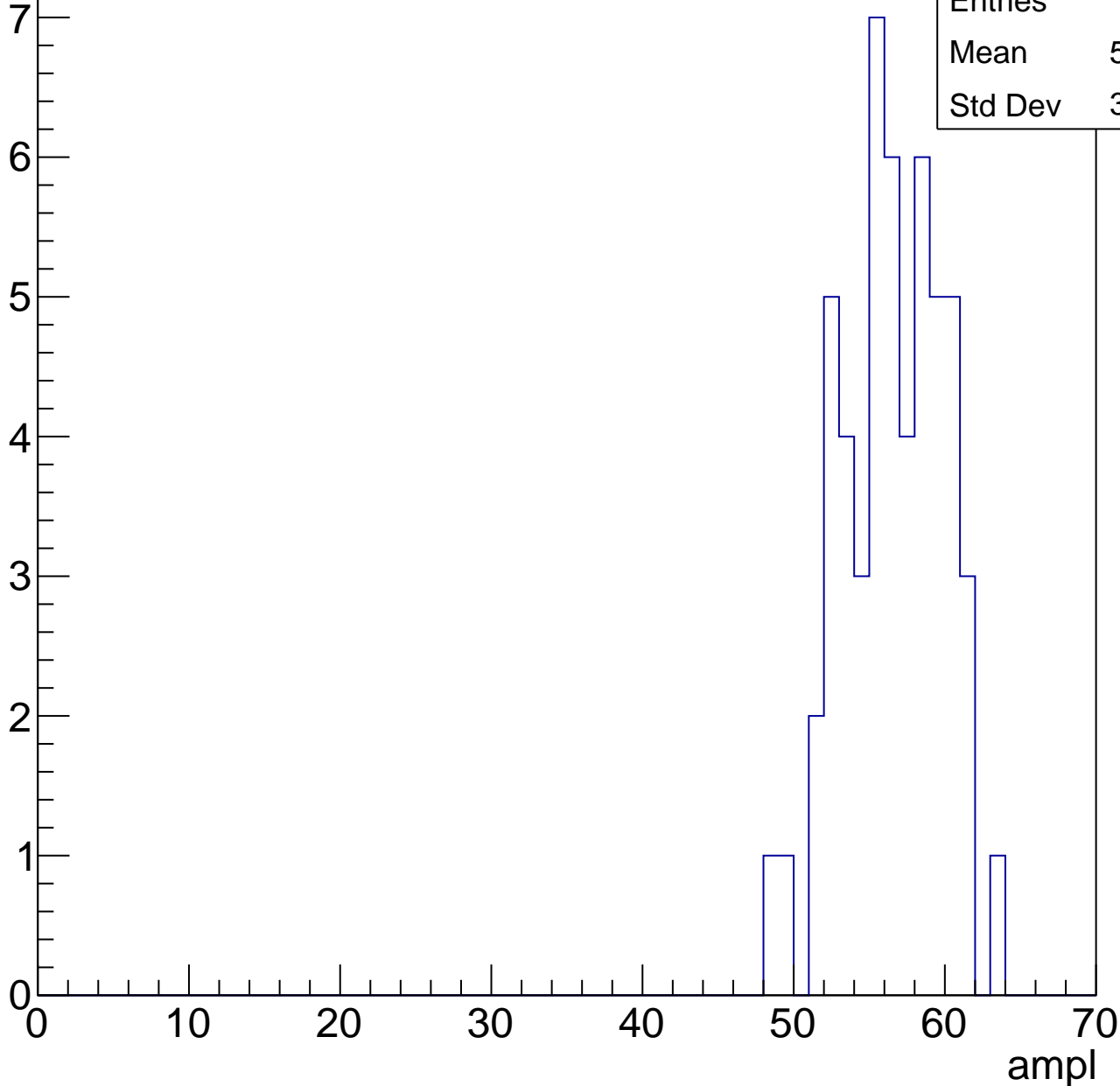


# B0L001S, U5-ch114, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

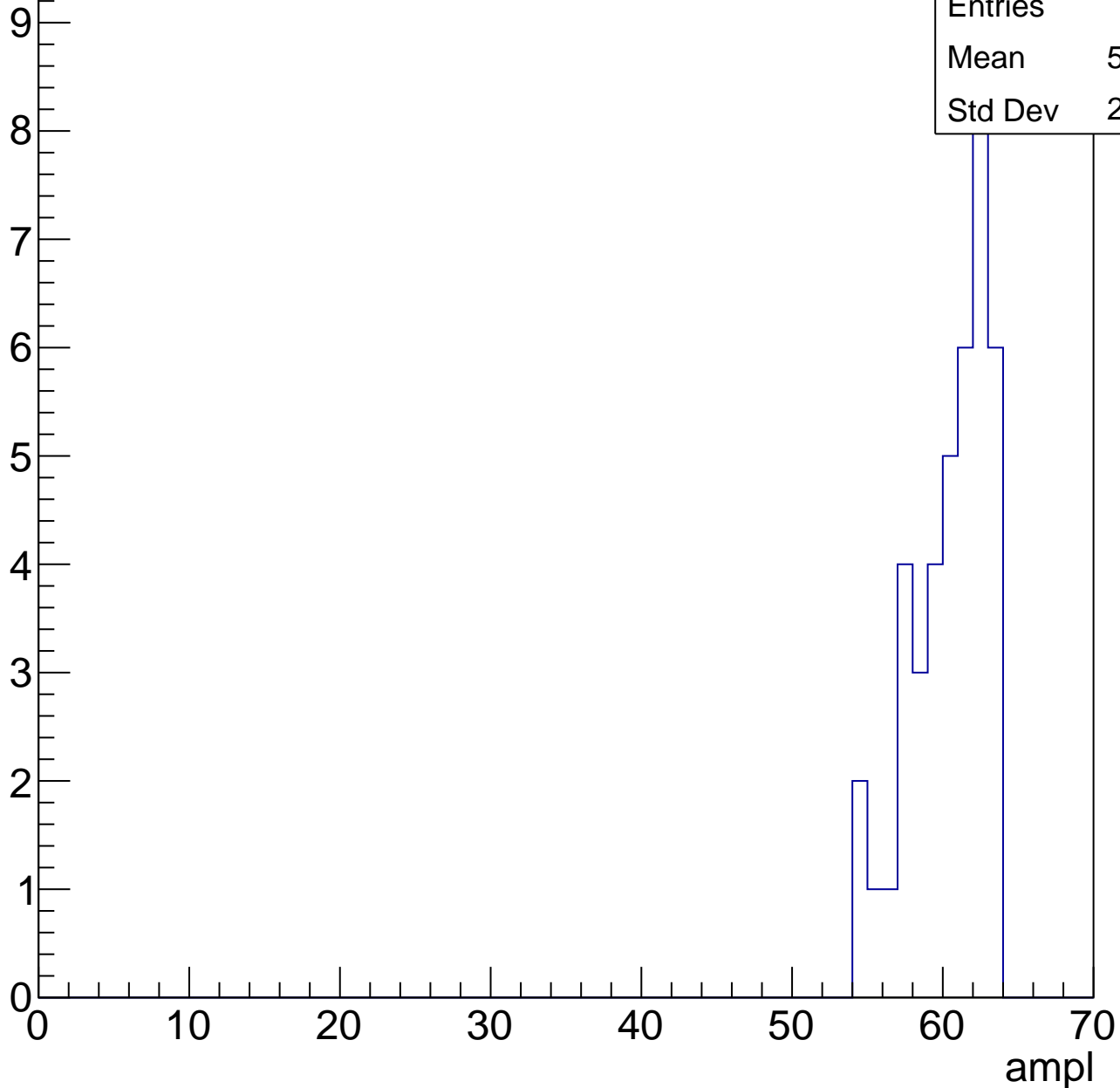
Entries	53
Mean	56.06
Std Dev	3.293



# B0L001S, U5-ch114, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

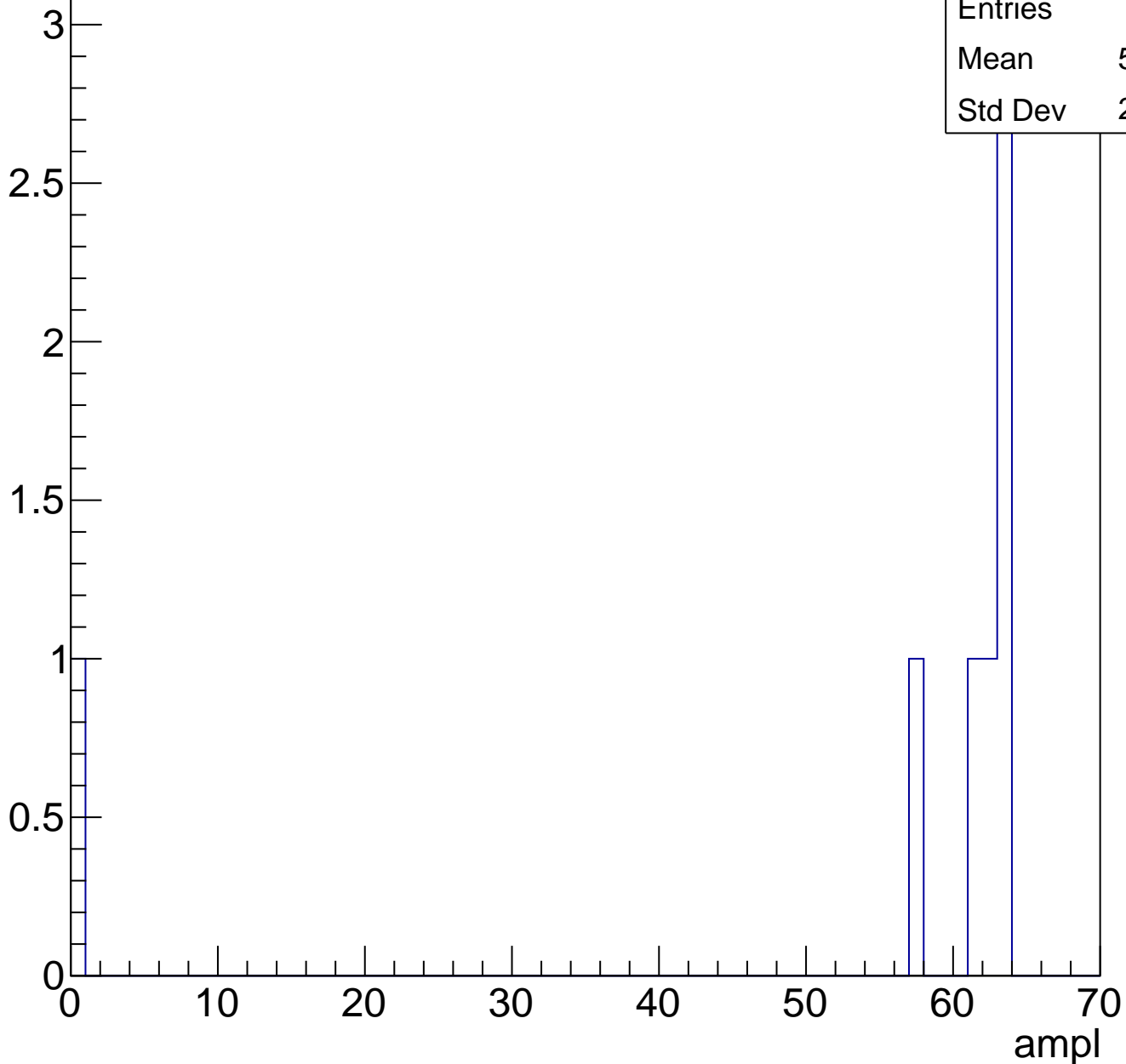
Entry



# B0L001S, U5-ch114, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch114, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U5-ch115, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	83
Mean	33.69
Std Dev	3.6

**Gaus mean : 33.6327**

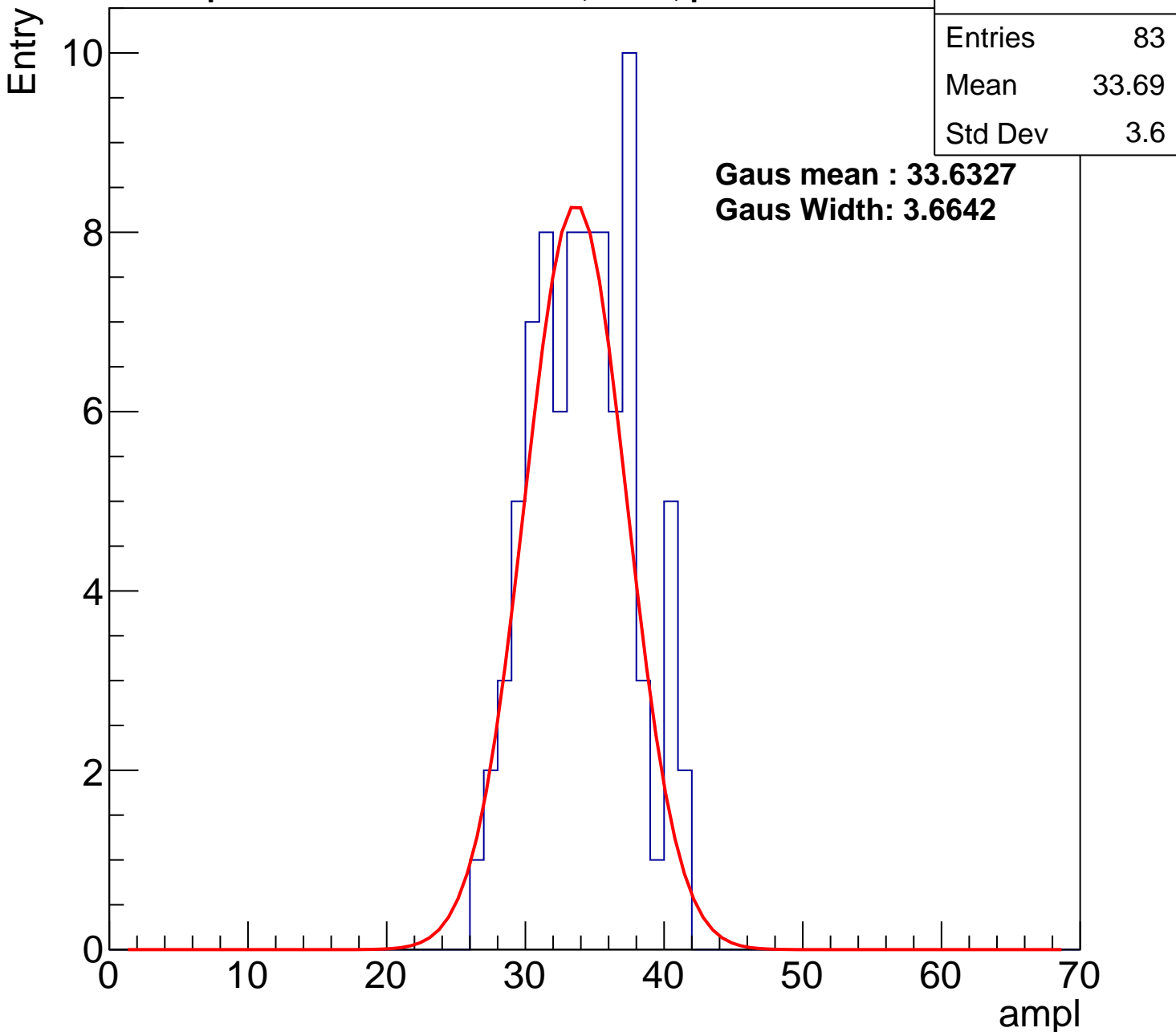
**Gaus Width: 3.6642**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U5-ch115, adc1

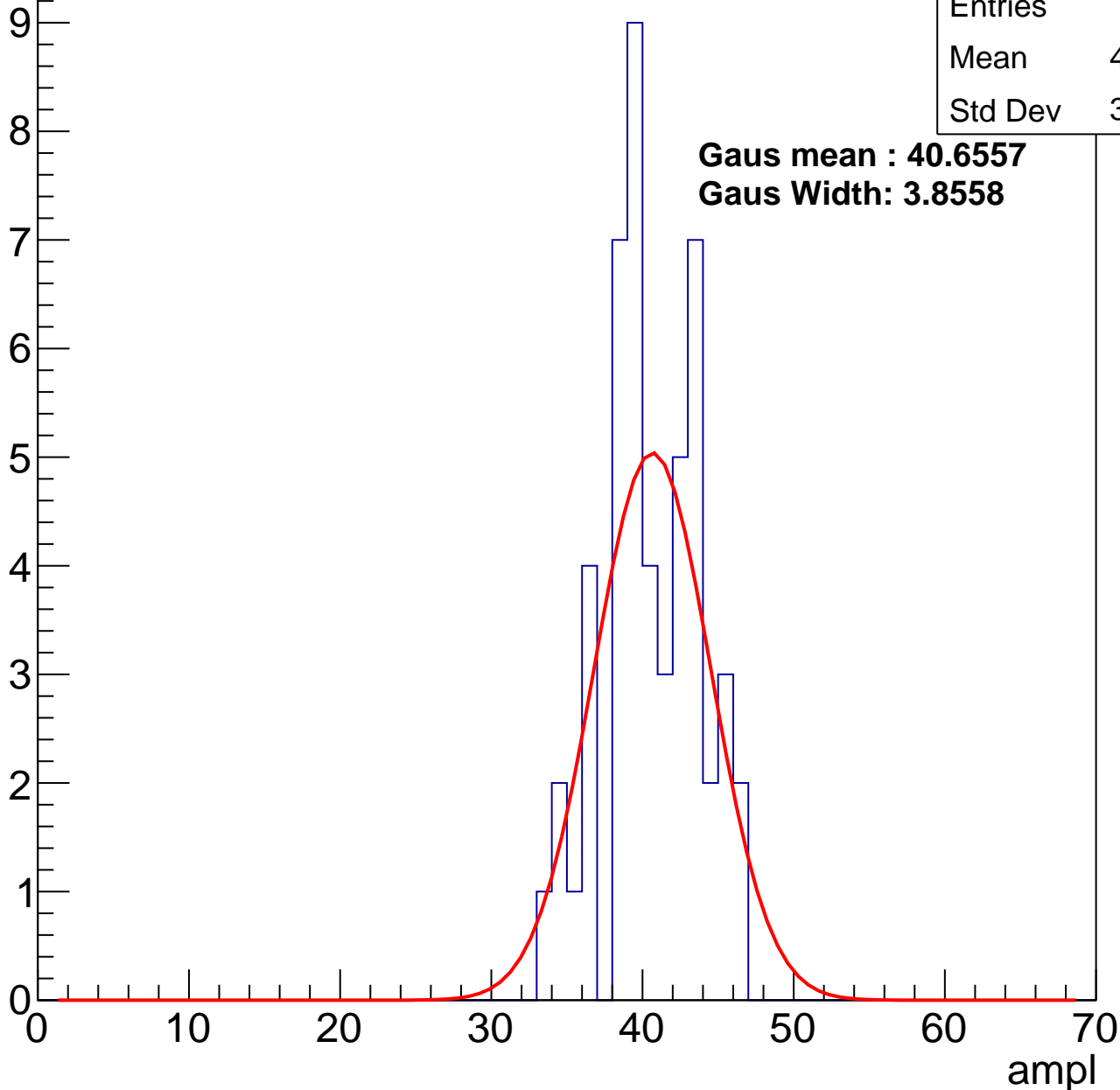
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	50
Mean	40.12
Std Dev	3.198

**Gaus mean : 40.6557**

**Gaus Width: 3.8558**



# B0L001S, U5-ch115, adc2

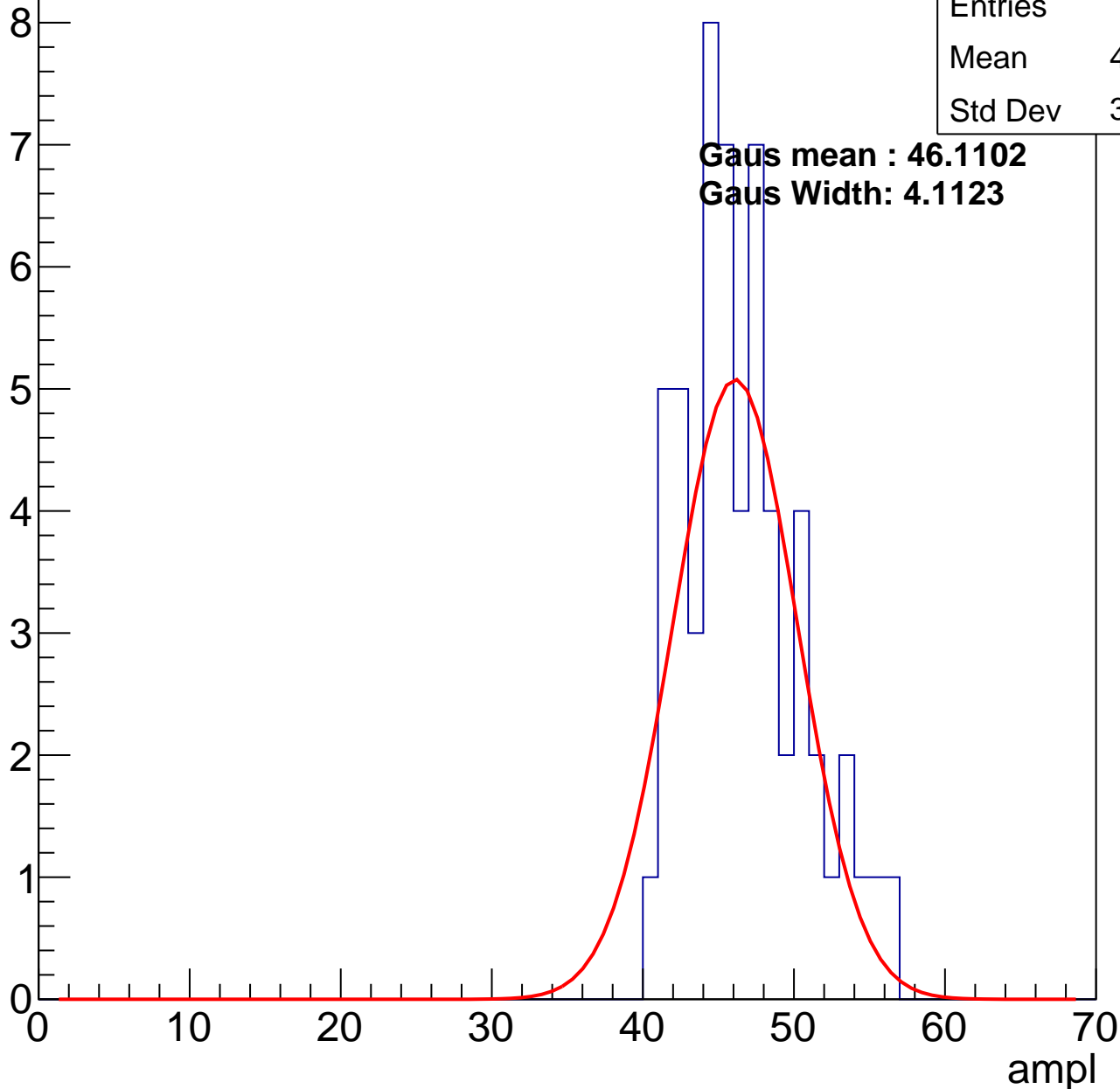
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	46.19
Std Dev	3.803

**Gaus mean : 46.1102**

**Gaus Width: 4.1123**

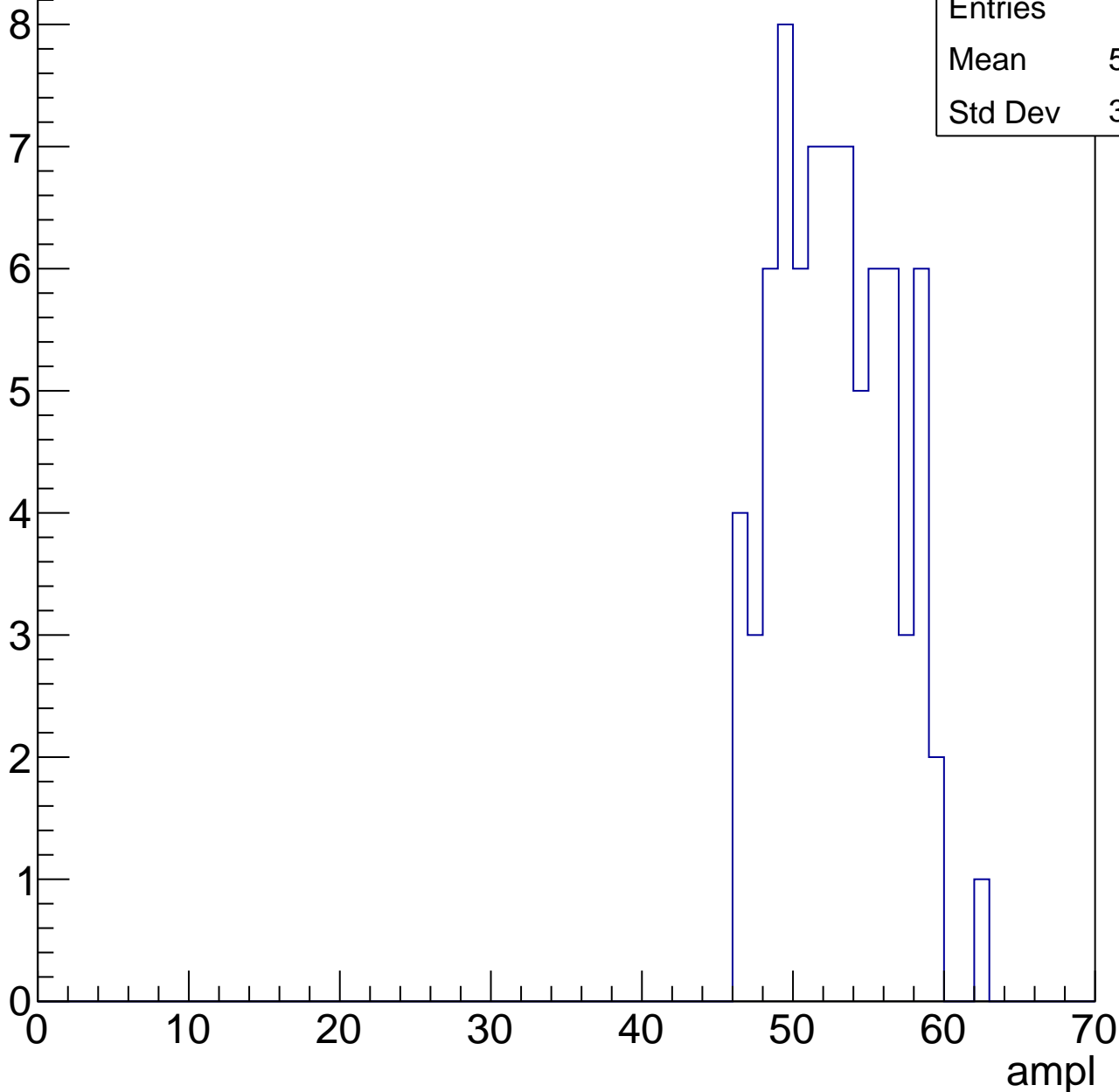


# B0L001S, U5-ch115, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

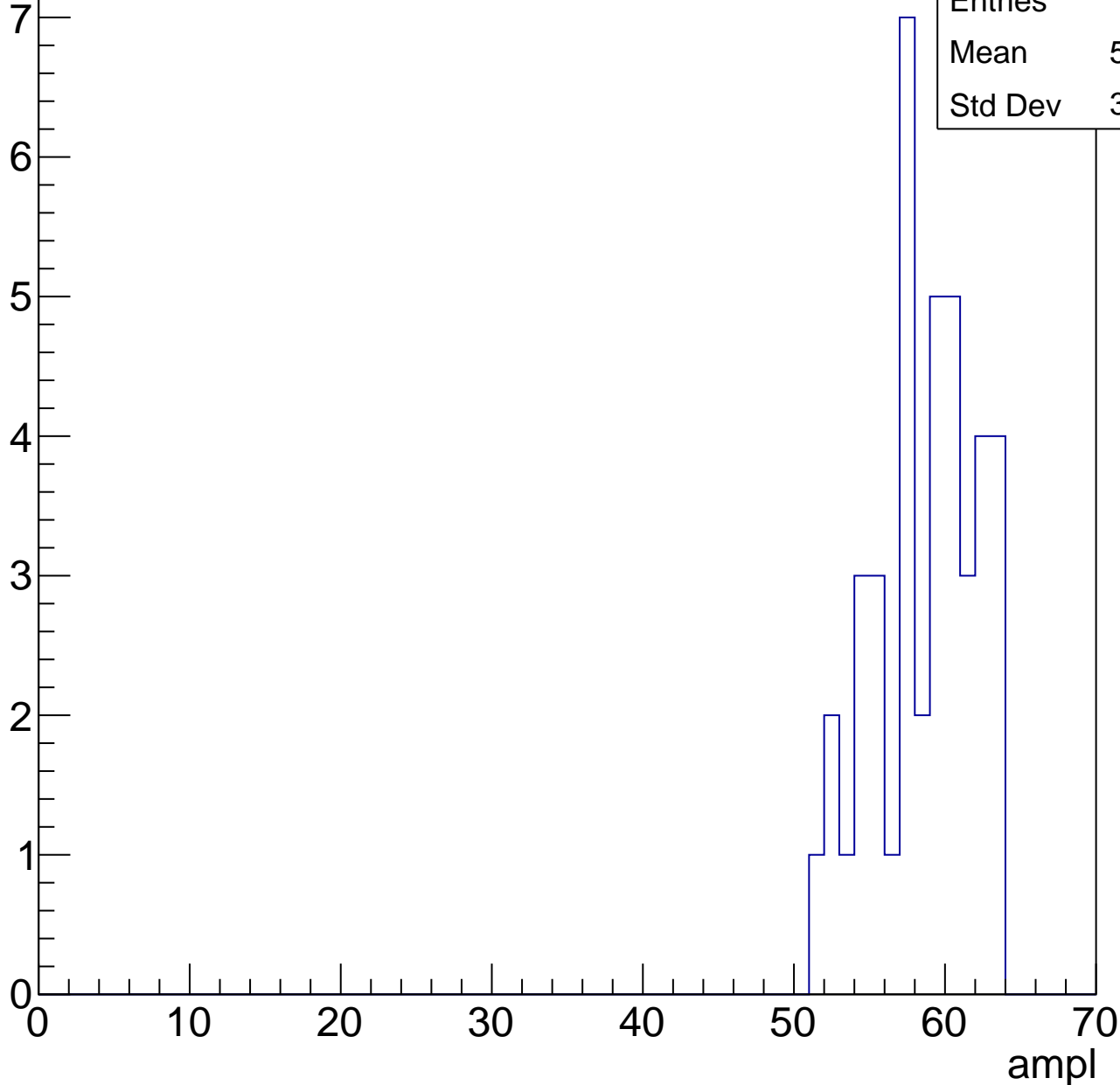
Entries	77
Mean	52.36
Std Dev	3.734



# B0L001S, U5-ch115, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



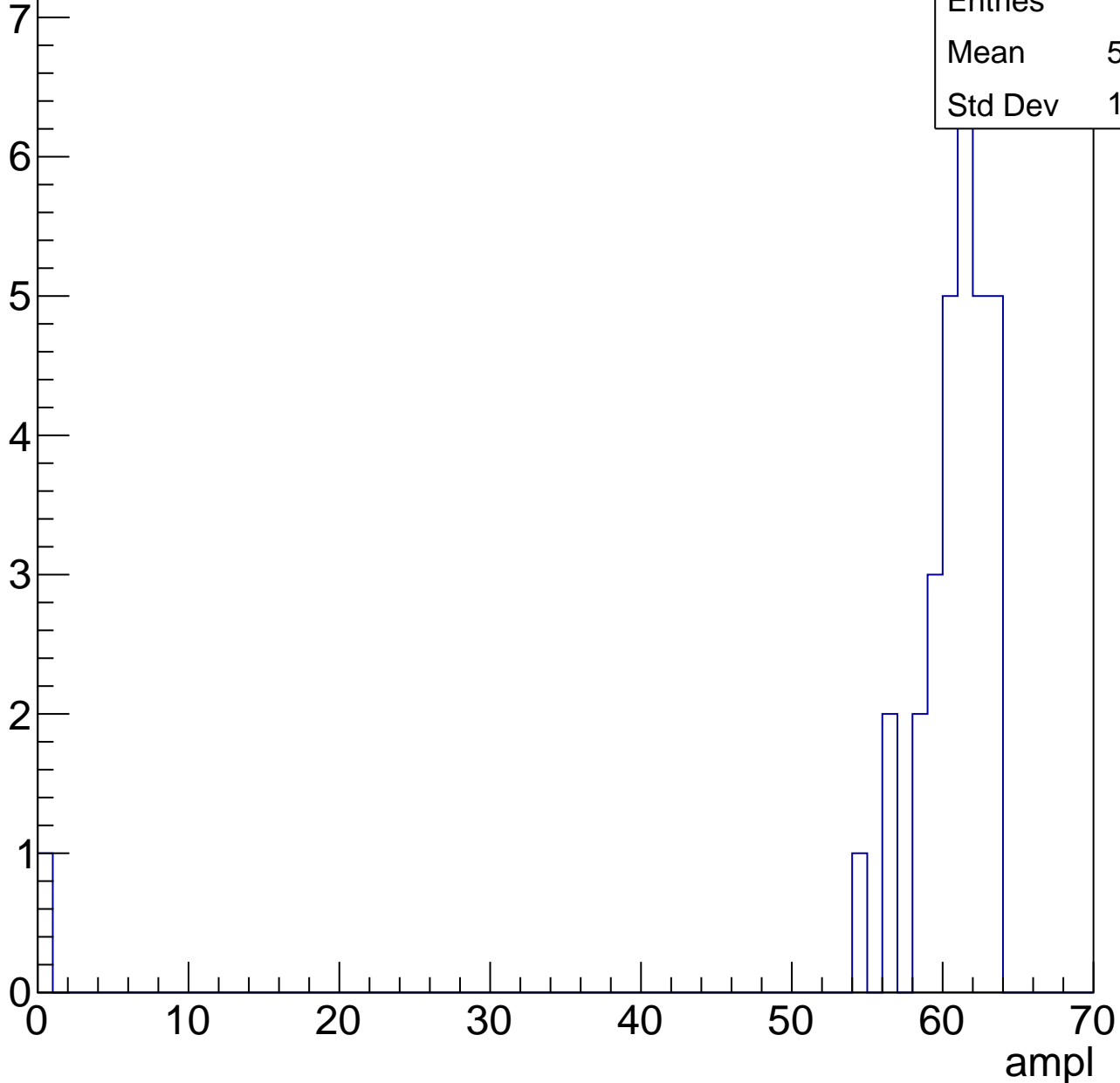
Entries	41
Mean	58.15
Std Dev	3.302

# B0L001S, U5-ch115, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	31
Mean	58.42
Std Dev	10.89



# B0L001S, U5-ch115, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch115, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U5-ch116, adc0

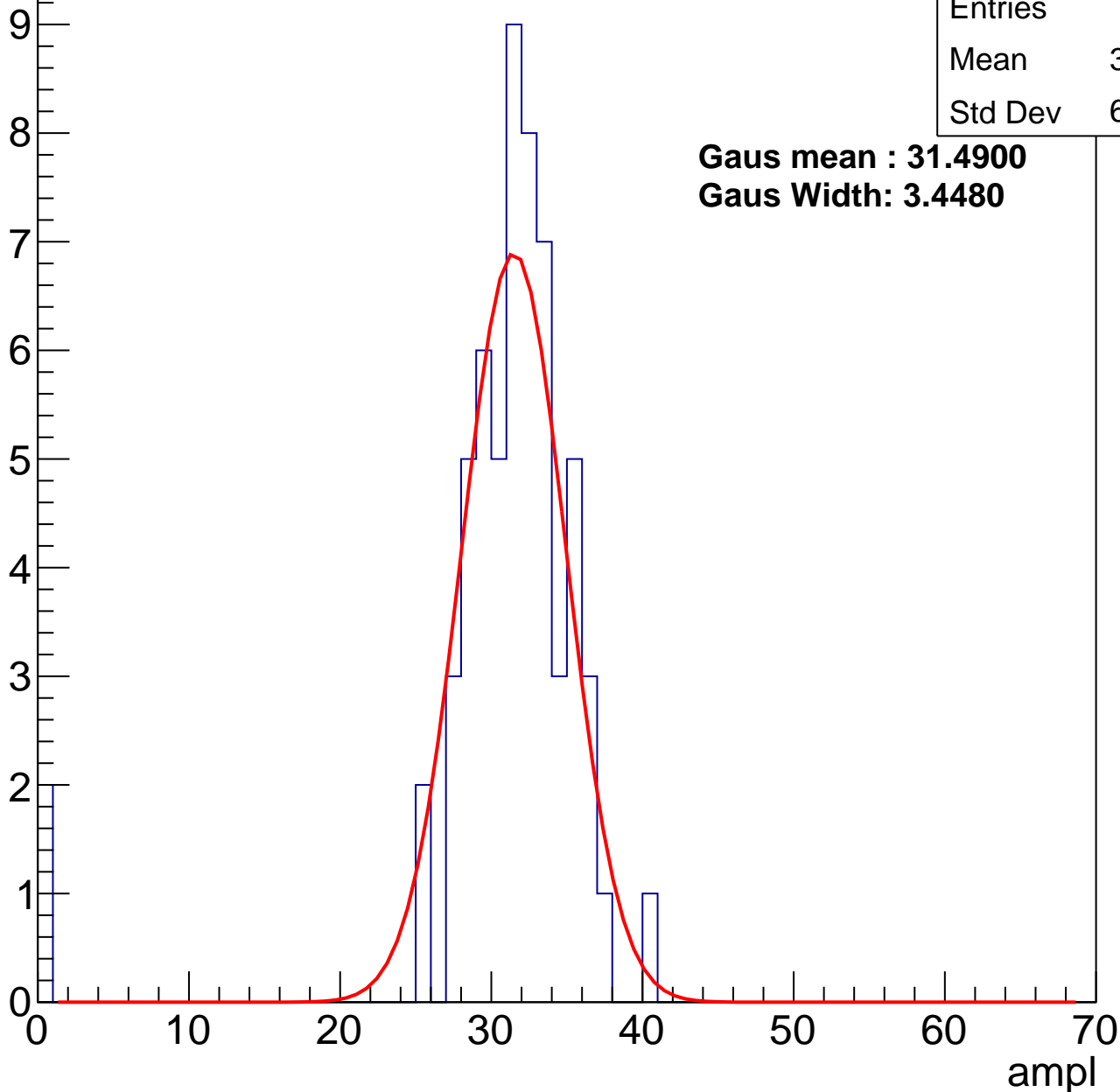
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	30.38
Std Dev	6.362

**Gaus mean : 31.4900**

**Gaus Width: 3.4480**



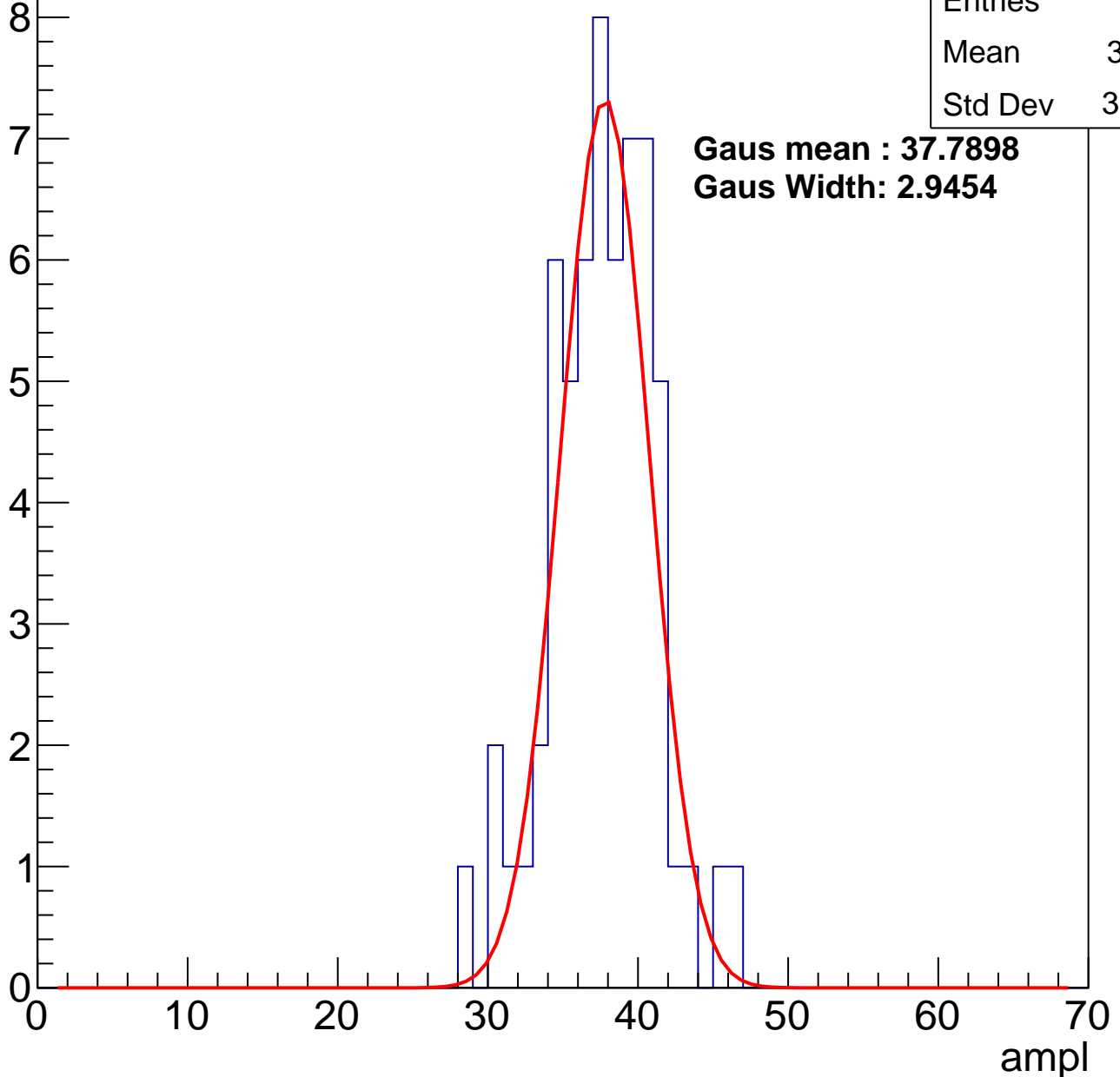
# B0L001S, U5-ch116, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	37.21
Std Dev	3.465

**Gaus mean : 37.7898**  
**Gaus Width: 2.9454**



# B0L001S, U5-ch116, adc2

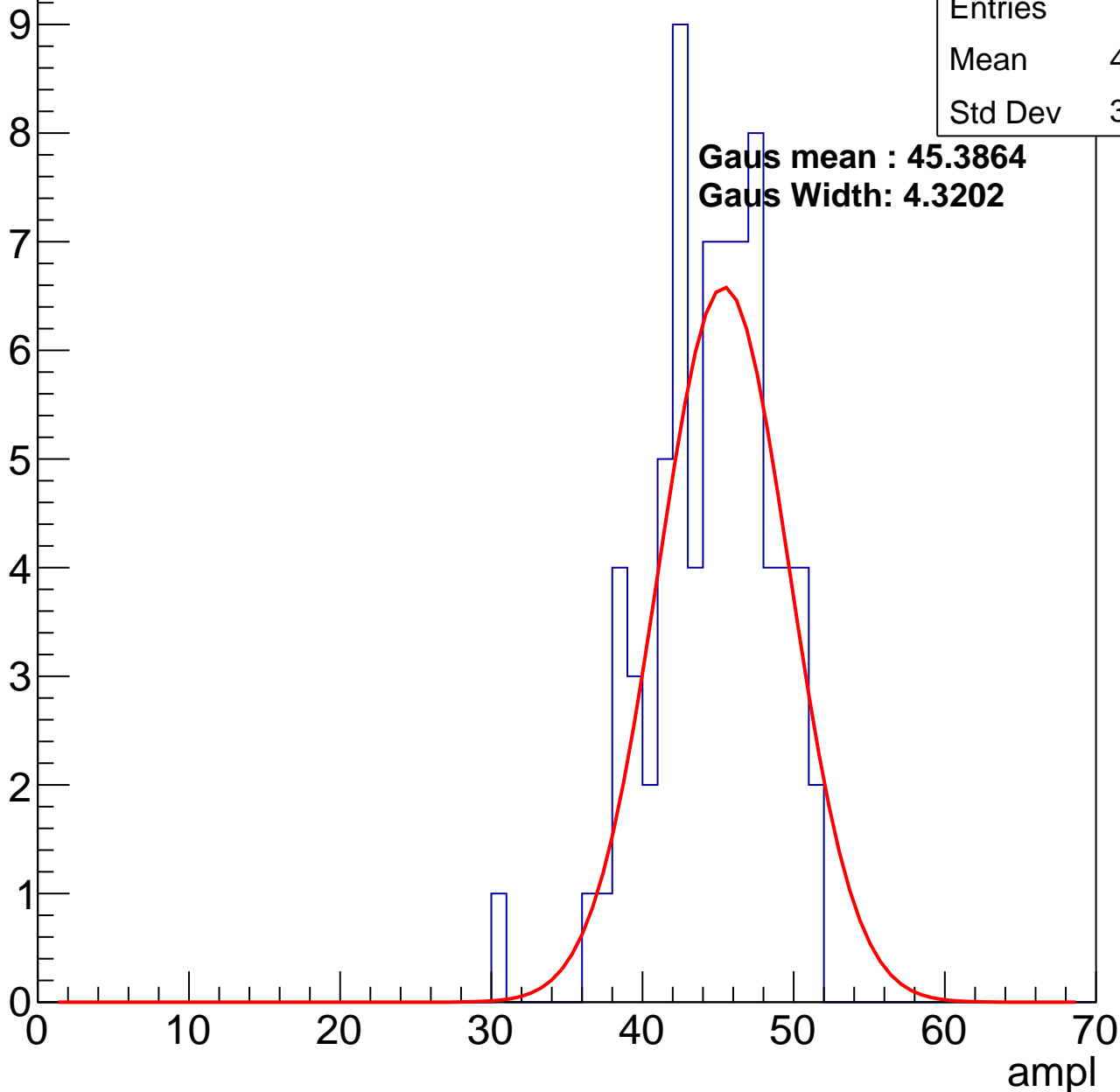
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	44.08
Std Dev	3.982

**Gaus mean : 45.3864**

**Gaus Width: 4.3202**

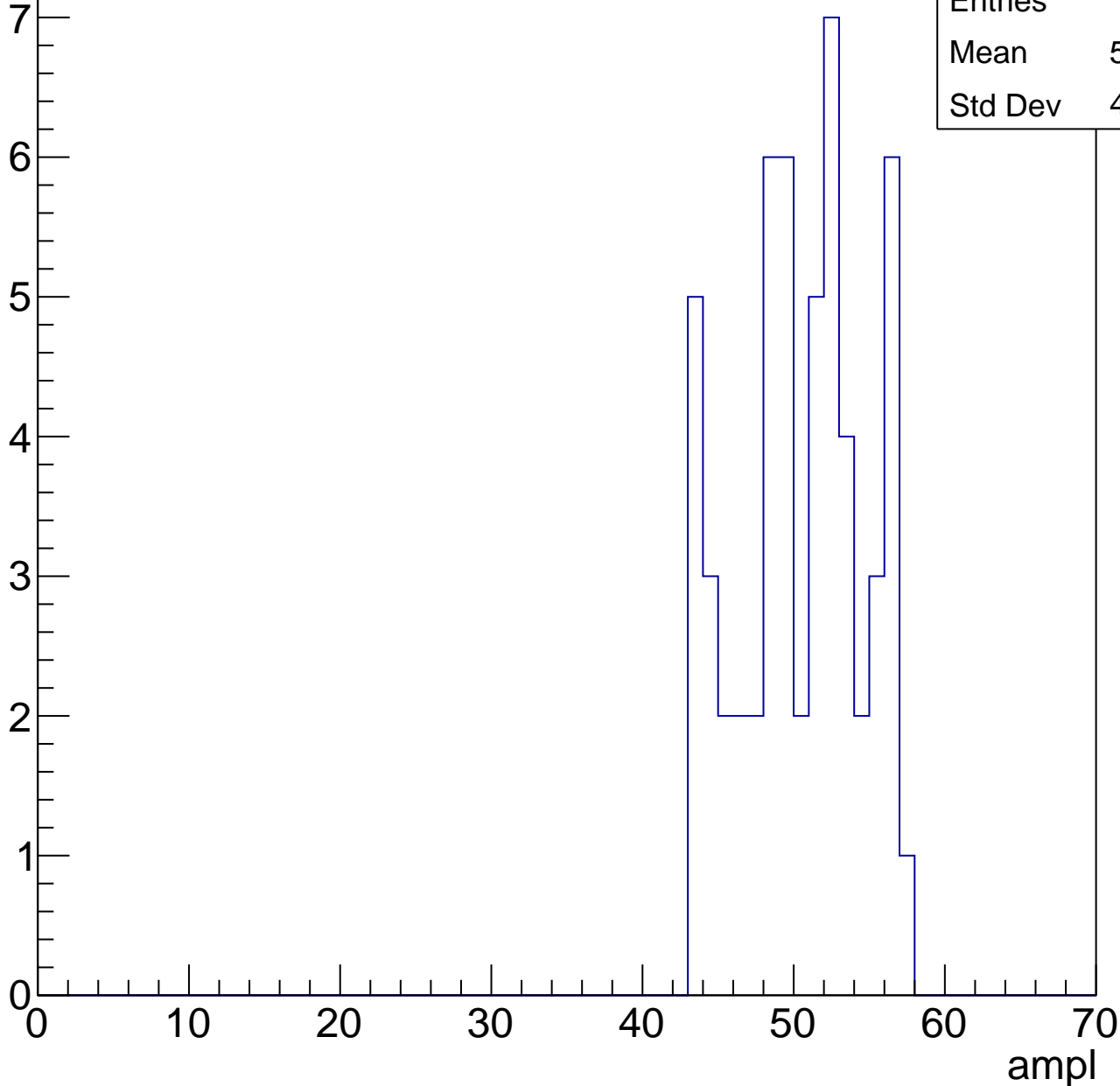


# B0L001S, U5-ch116, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	50.04
Std Dev	4.062

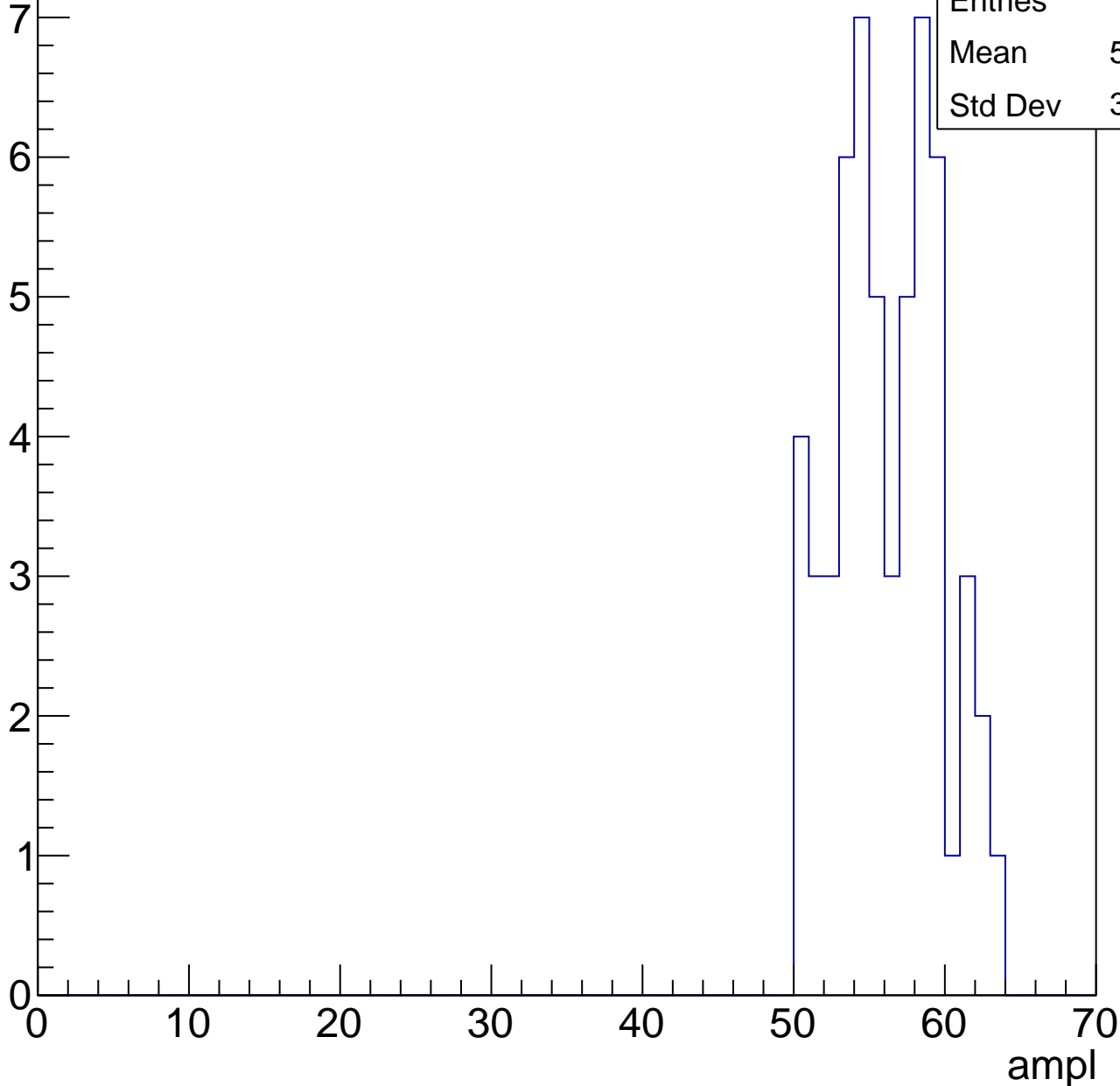


# B0L001S, U5-ch116, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

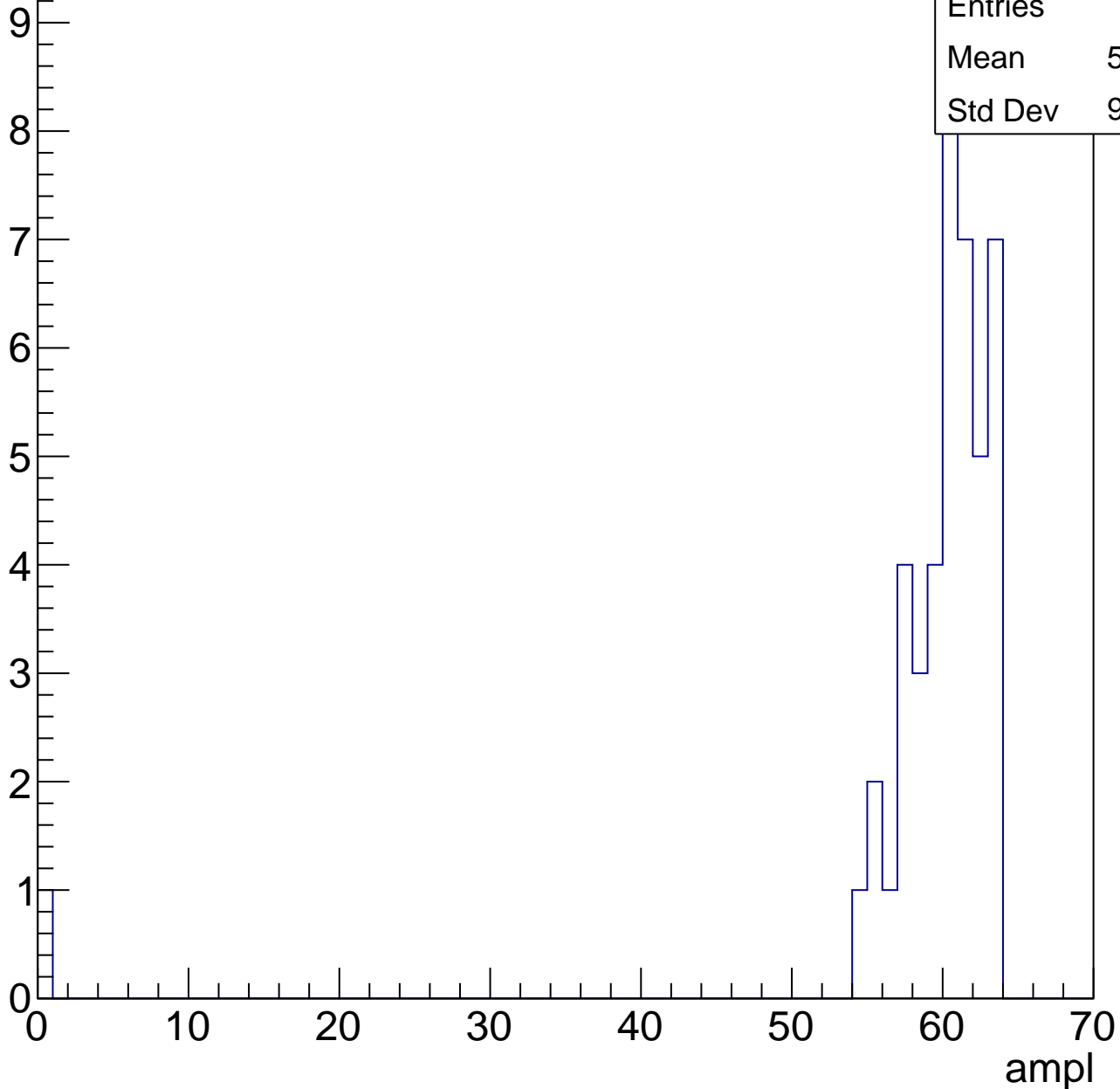
Entries	56
Mean	55.77
Std Dev	3.407



# B0L001S, U5-ch116, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch116, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch116, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch117, adc0

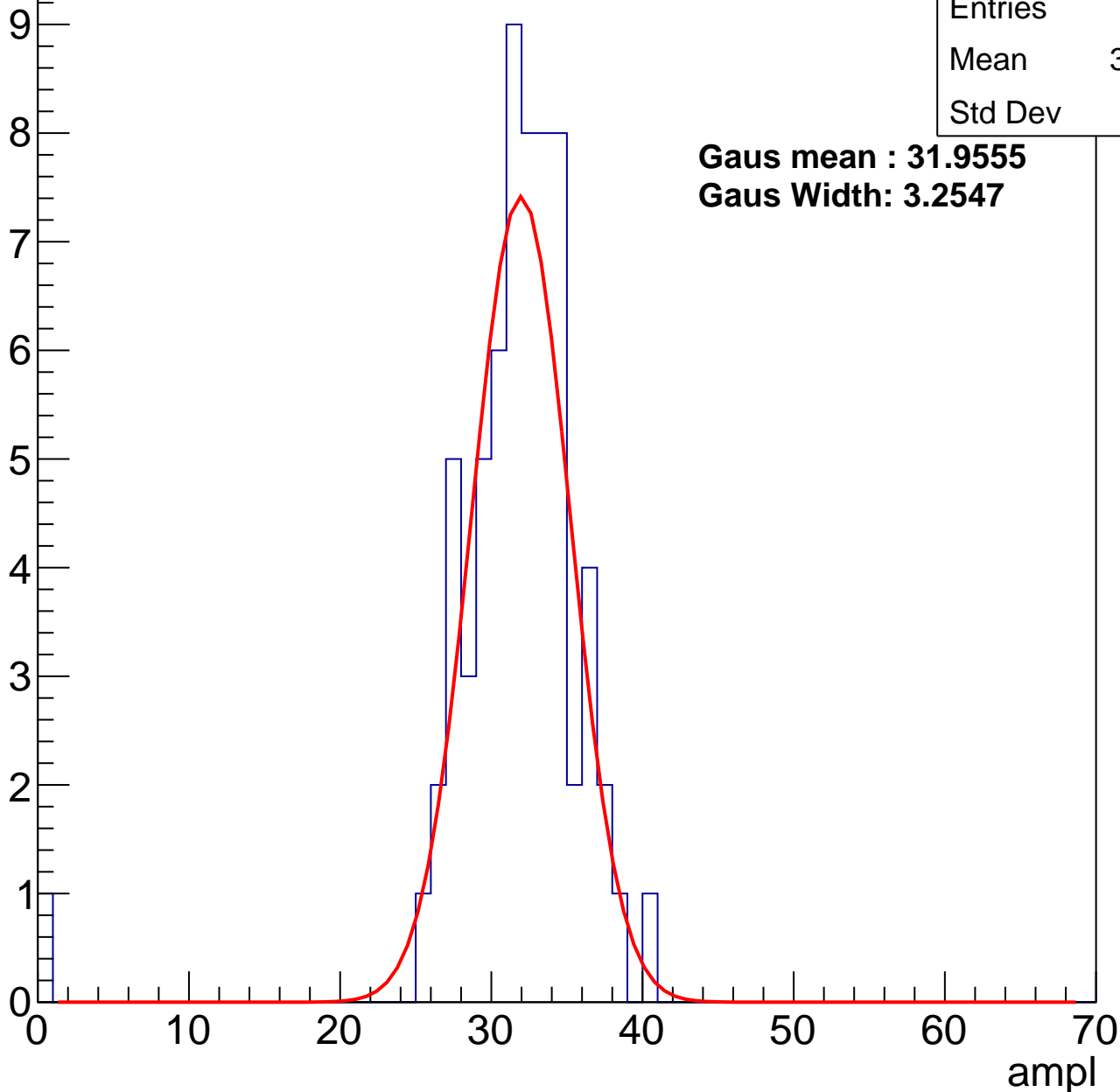
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	31.18
Std Dev	4.96

**Gaus mean : 31.9555**

**Gaus Width: 3.2547**



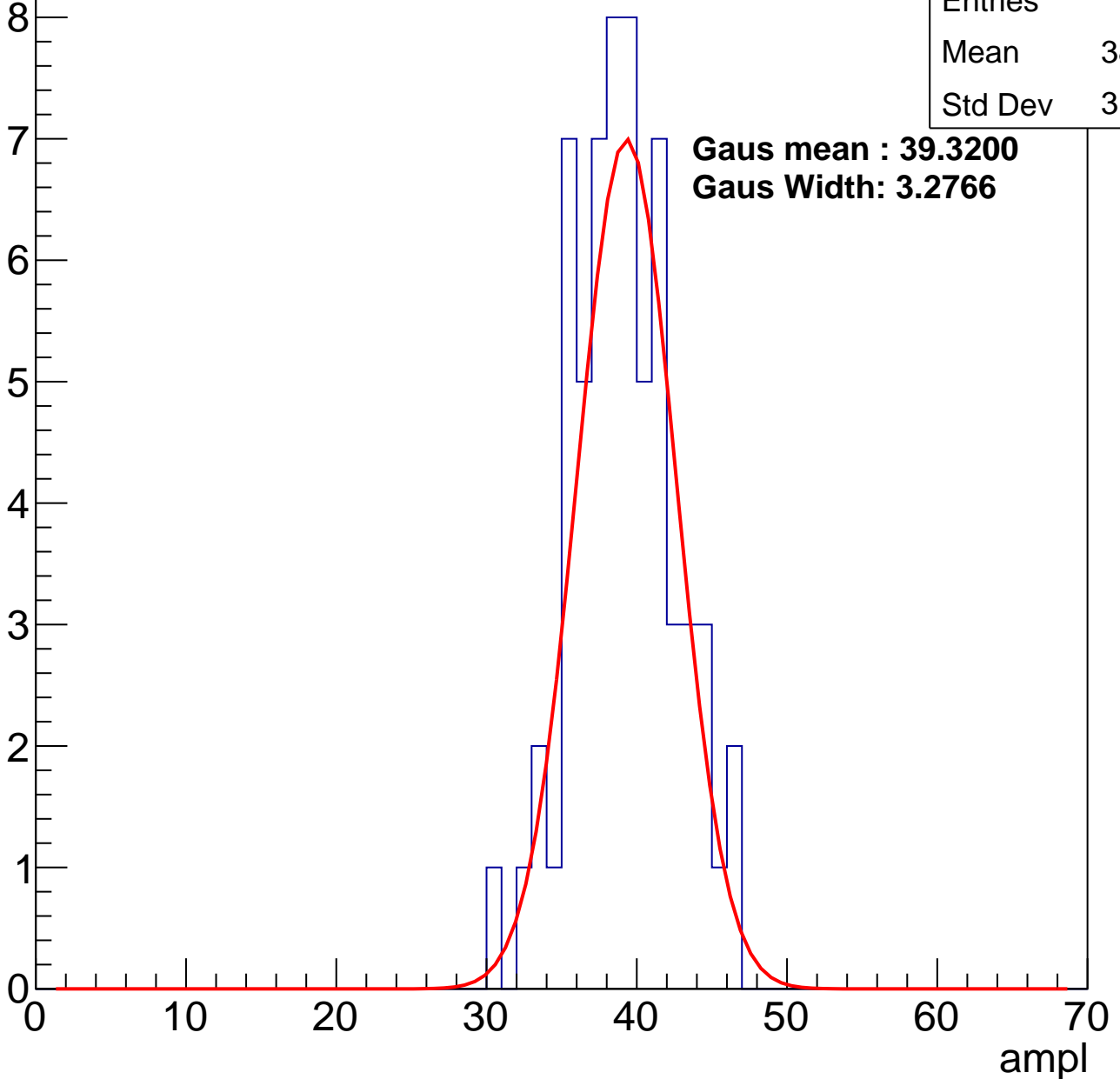
# B0L001S, U5-ch117, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	38.64
Std Dev	3.374

**Gaus mean : 39.3200**  
**Gaus Width: 3.2766**



# B0L001S, U5-ch117, adc2

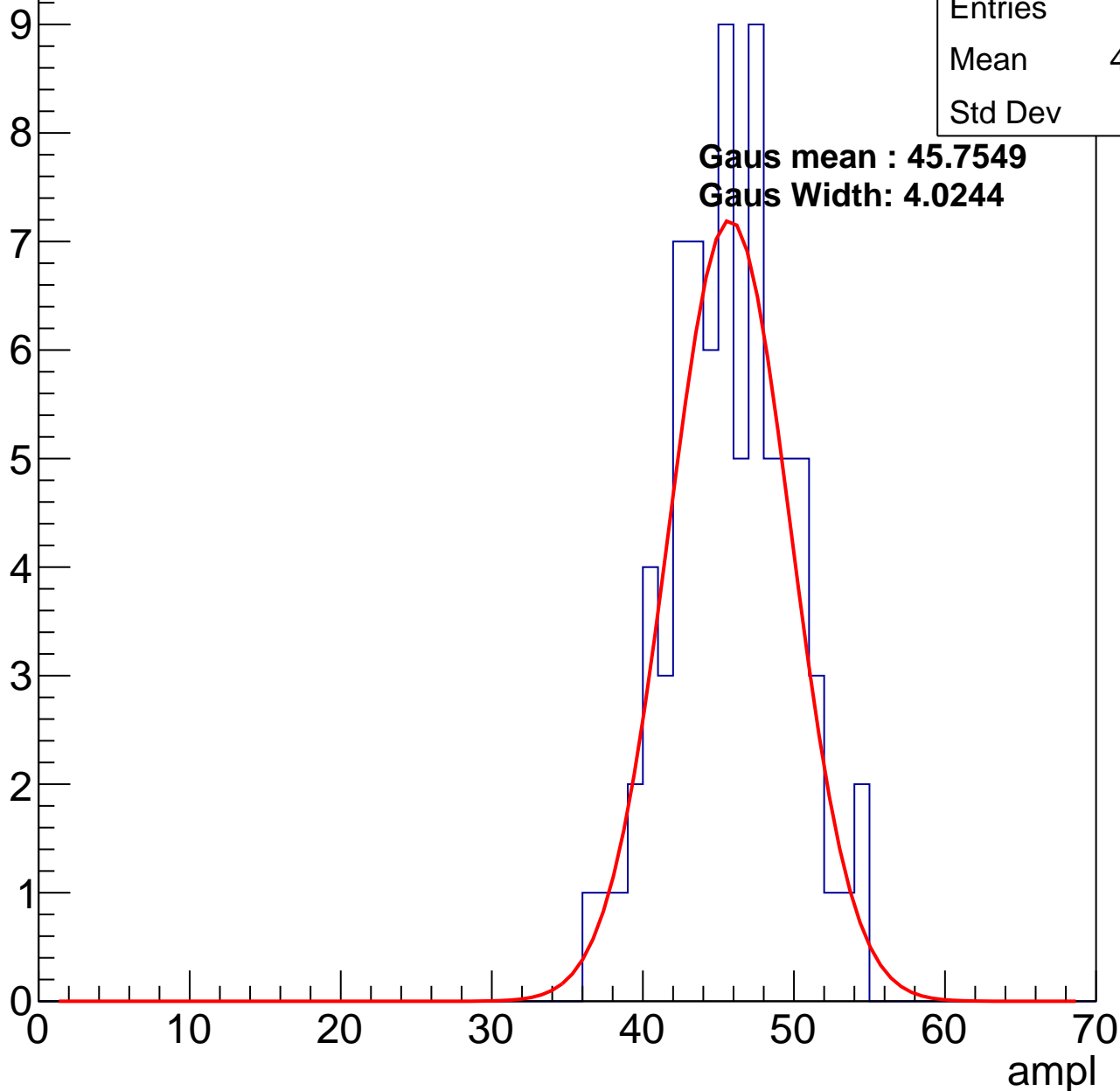
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	77
Mean	45.32
Std Dev	3.91

**Gaus mean : 45.7549**

**Gaus Width: 4.0244**

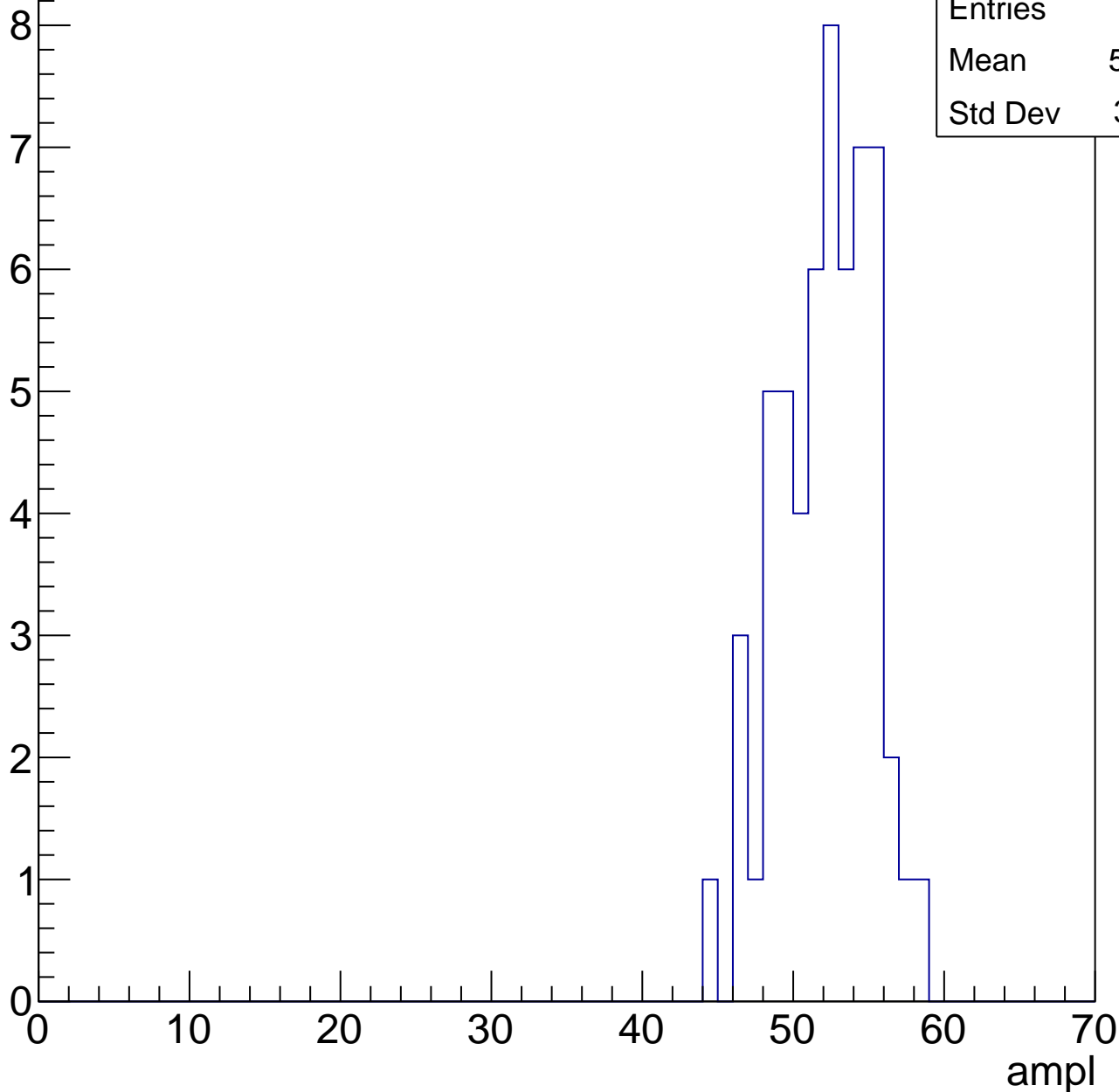


# B0L001S, U5-ch117, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	51.65
Std Dev	3.041

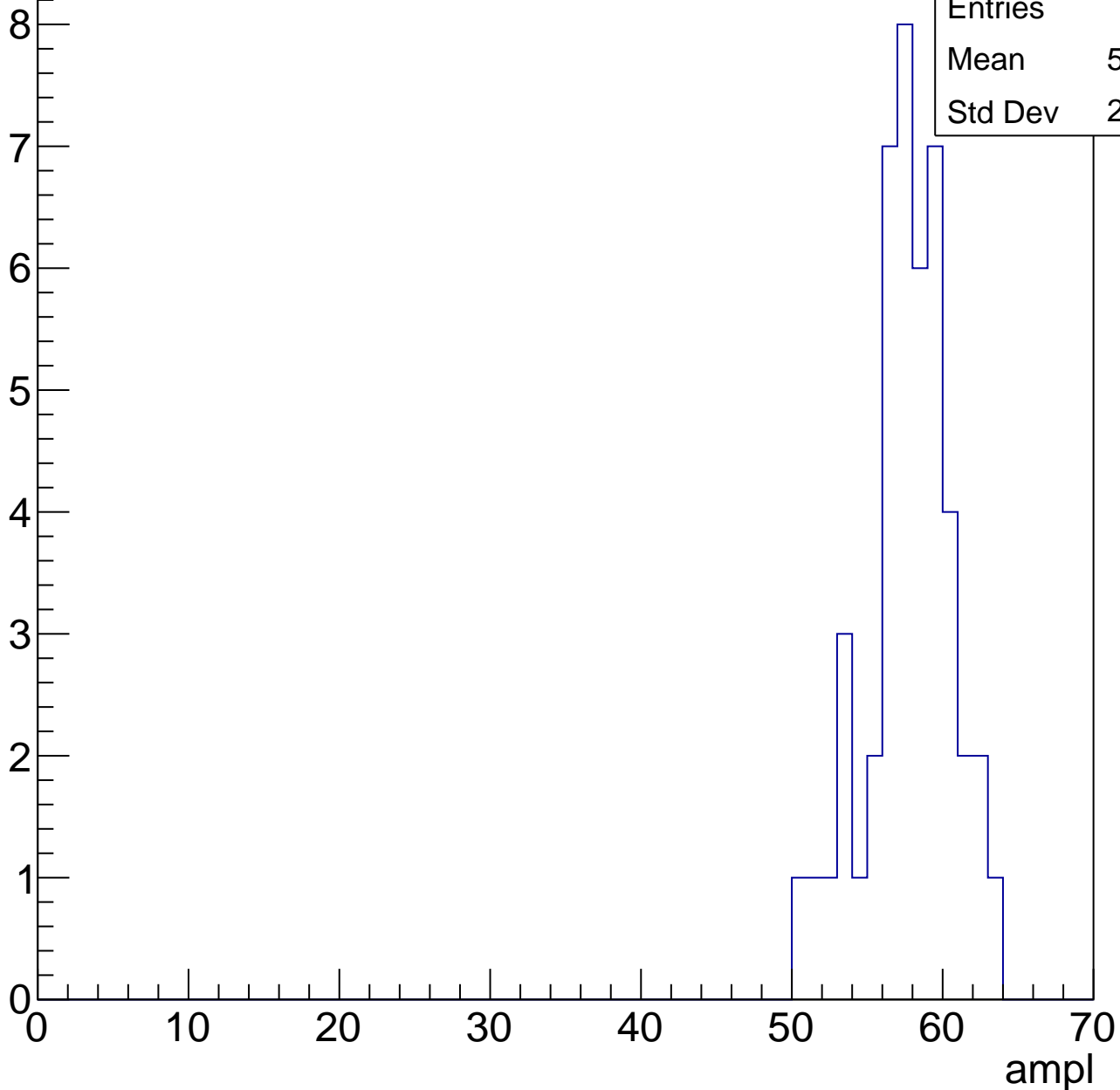


# B0L001S, U5-ch117, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	46
Mean	57.26
Std Dev	2.824

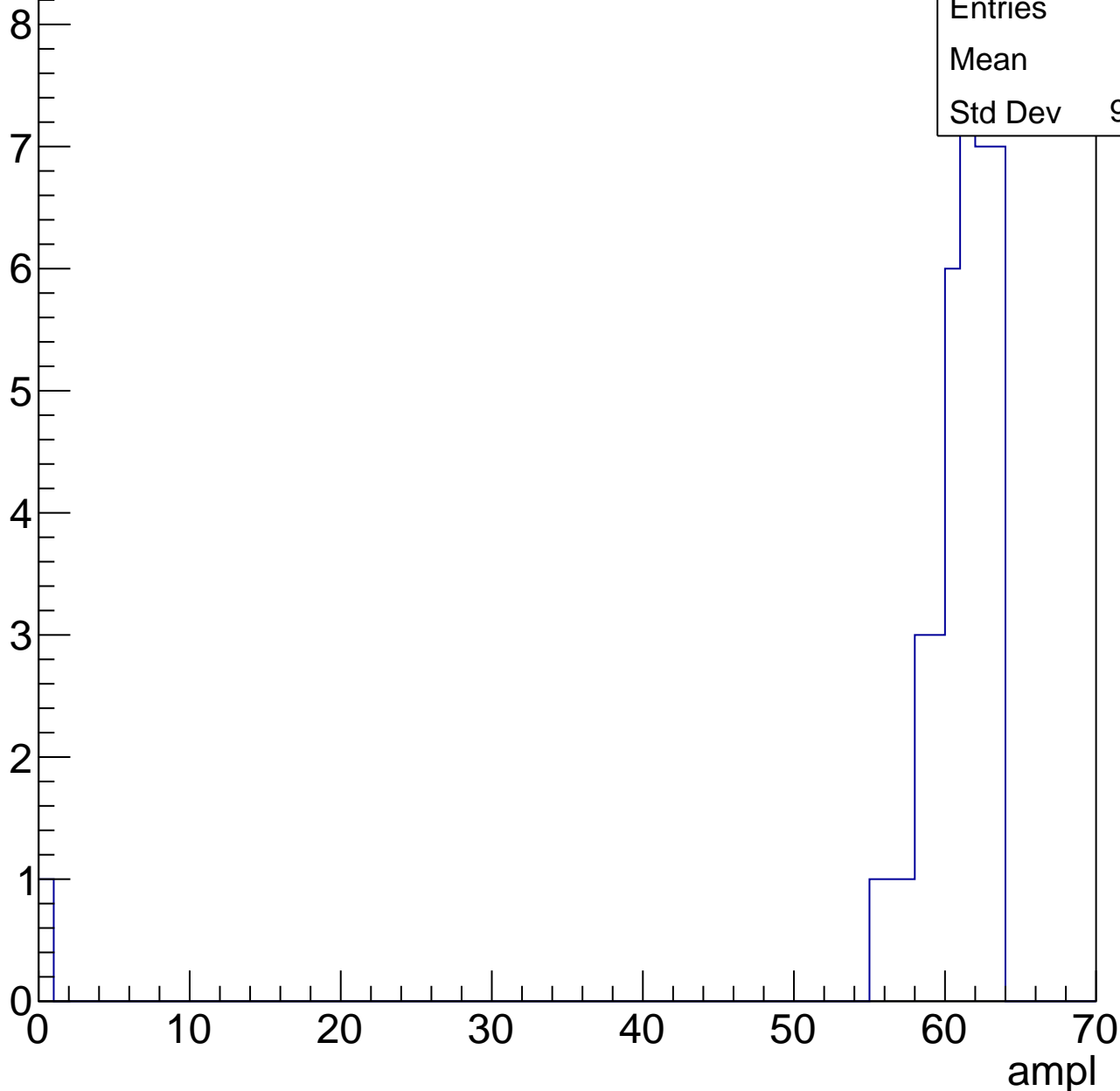


# B0L001S, U5-ch117, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	38
Mean	59
Std Dev	9.902



# B0L001S, U5-ch117, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.67
Std Dev	0.4714

ampl

0 10 20 30 40 50 60 70



# B0L001S, U5-ch117, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U5-ch118, adc0

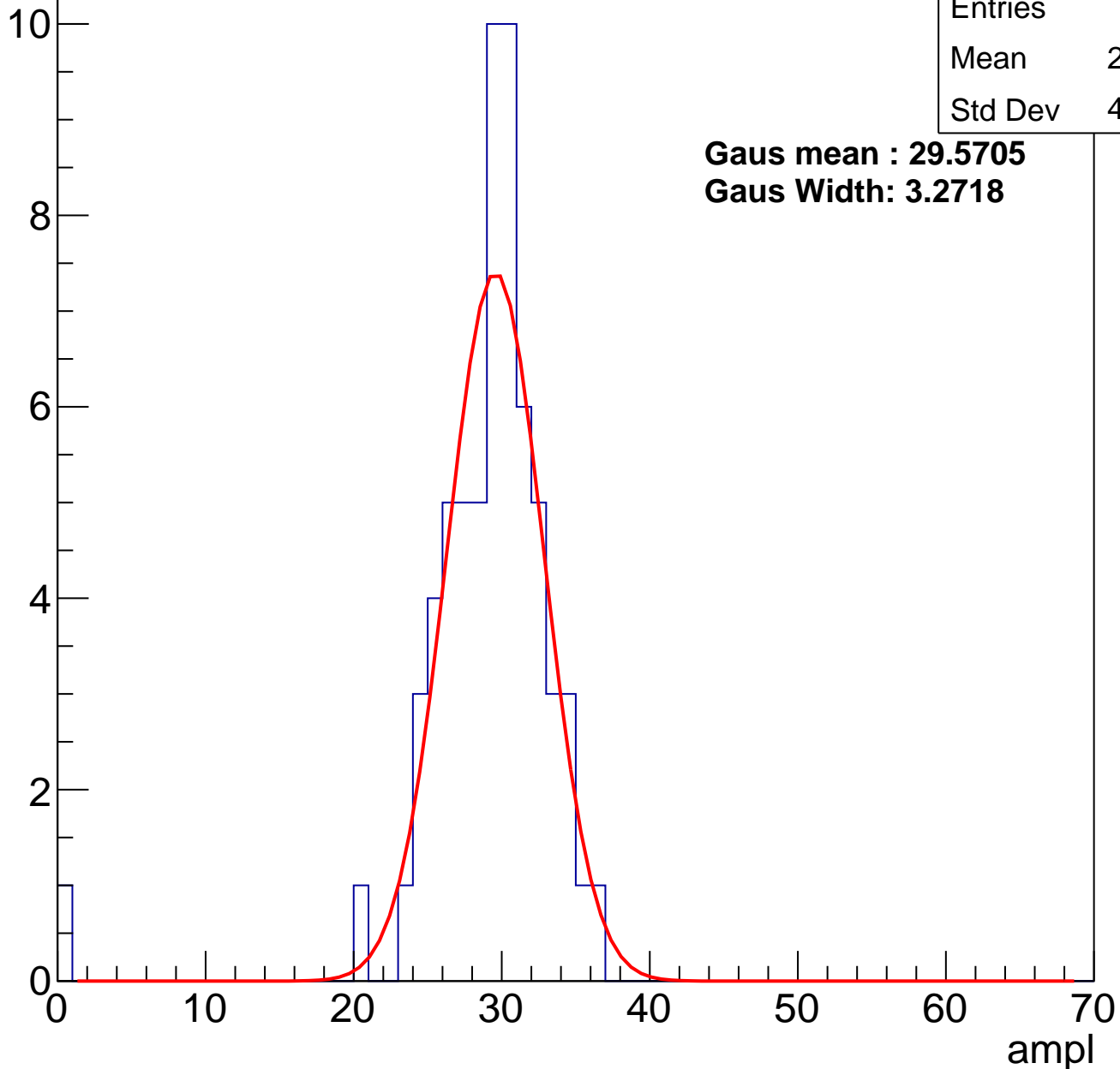
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	64
Mean	28.56
Std Dev	4.746

**Gaus mean : 29.5705**

**Gaus Width: 3.2718**

Entry



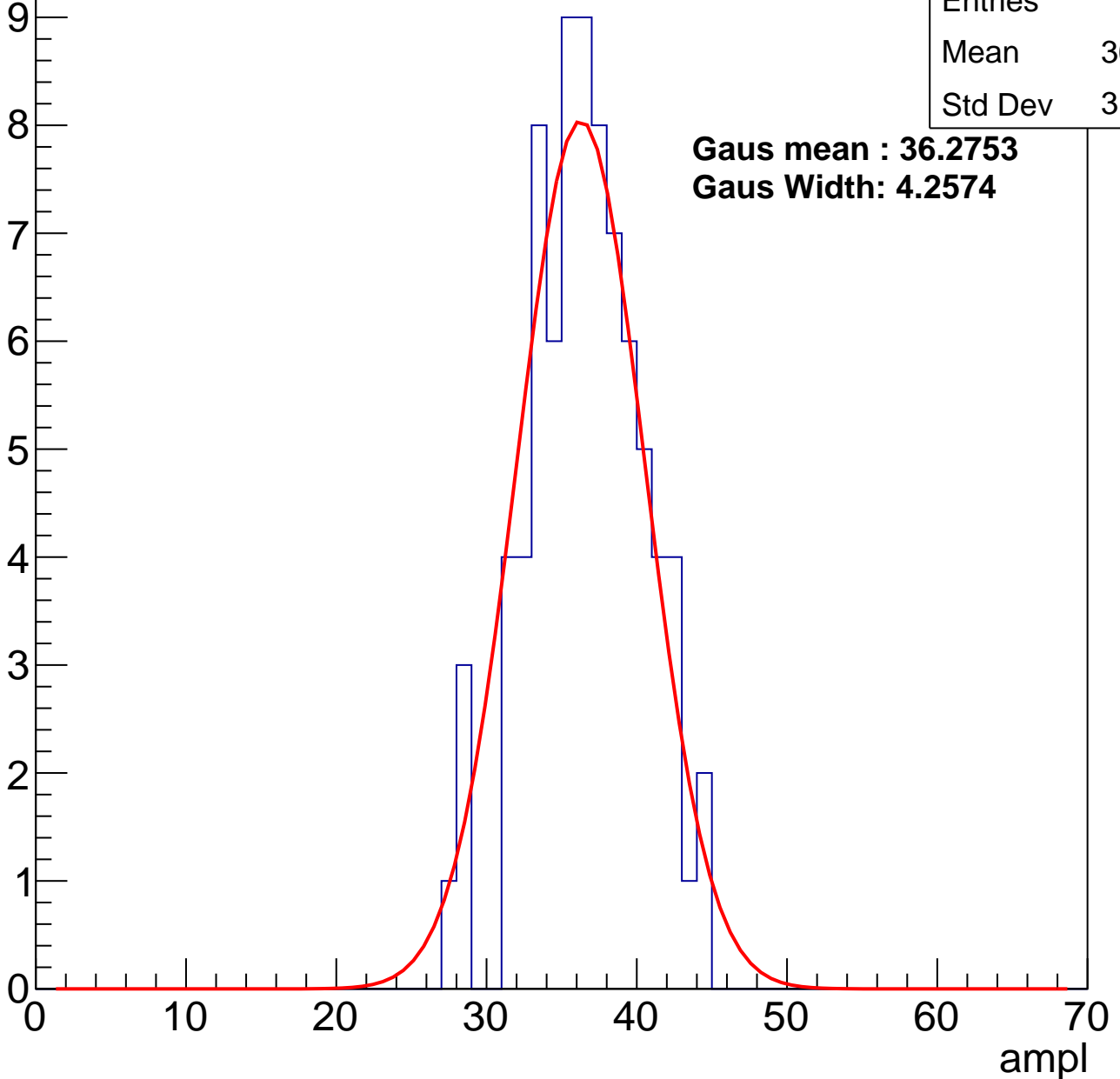
# B0L001S, U5-ch118, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	81
Mean	36.16
Std Dev	3.737

**Gaus mean : 36.2753**  
**Gaus Width: 4.2574**

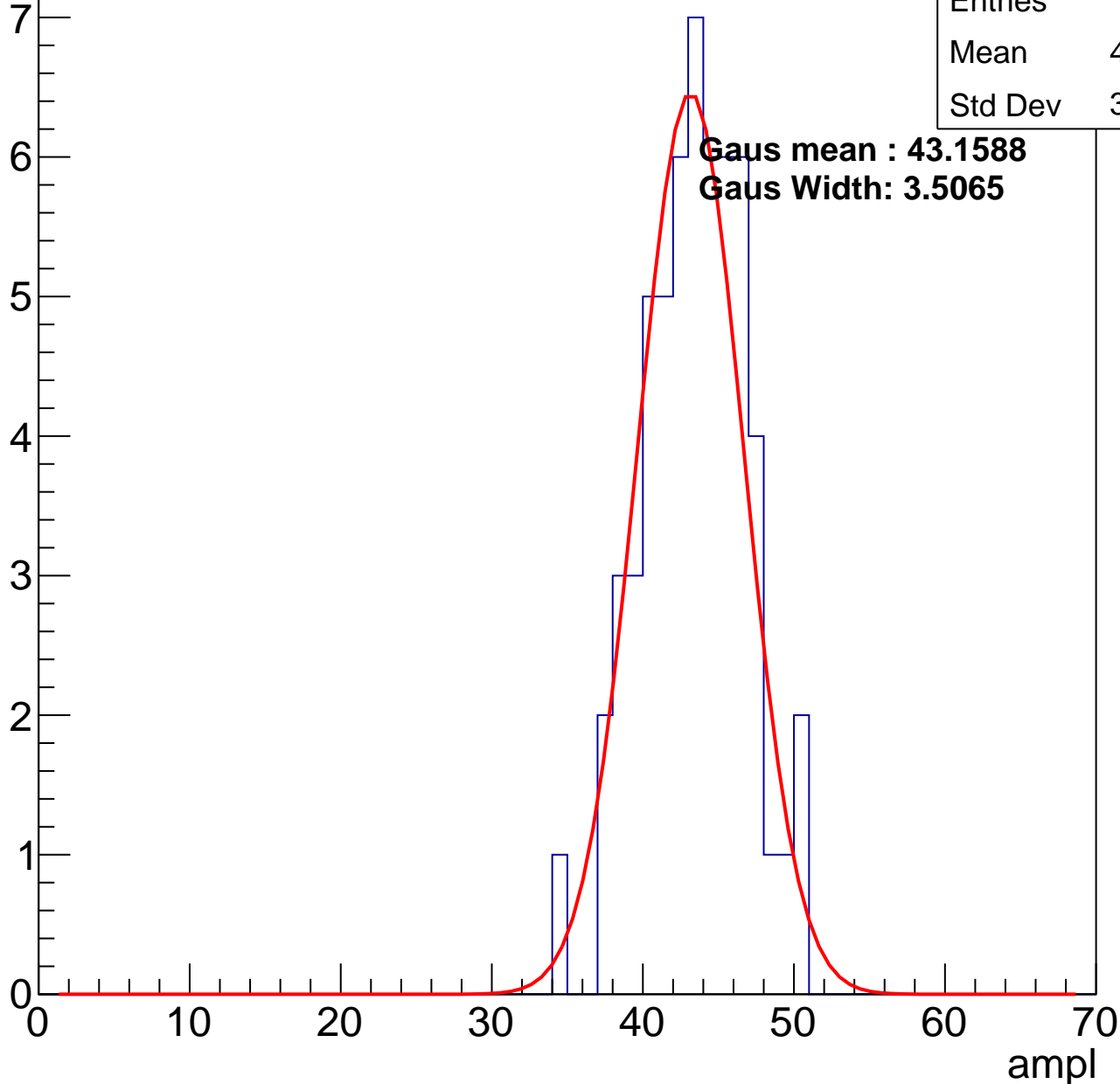


# B0L001S, U5-ch118, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	42.97
Std Dev	3.358

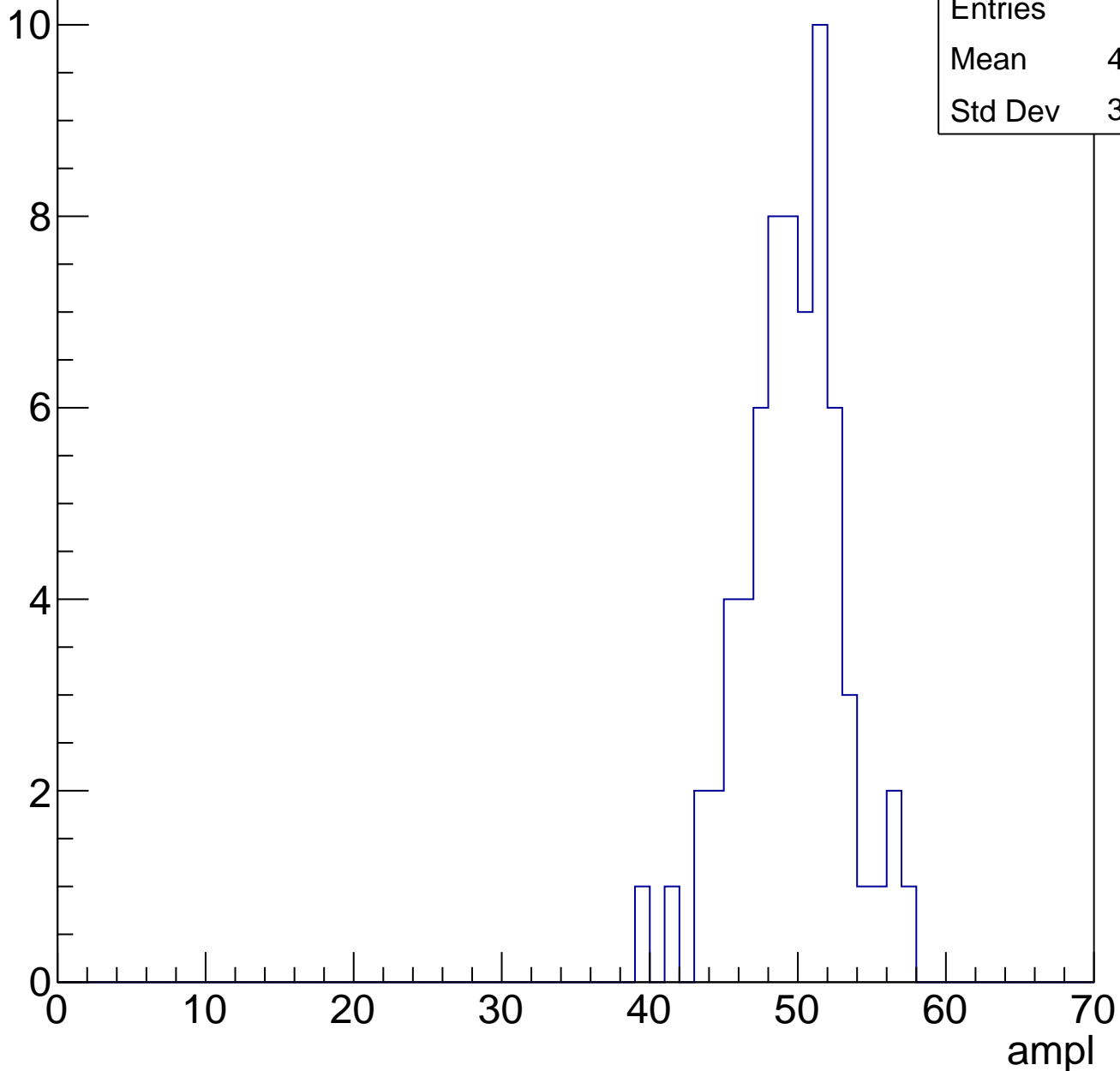


# B0L001S, U5-ch118, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	67
Mean	49.03
Std Dev	3.434

Entry

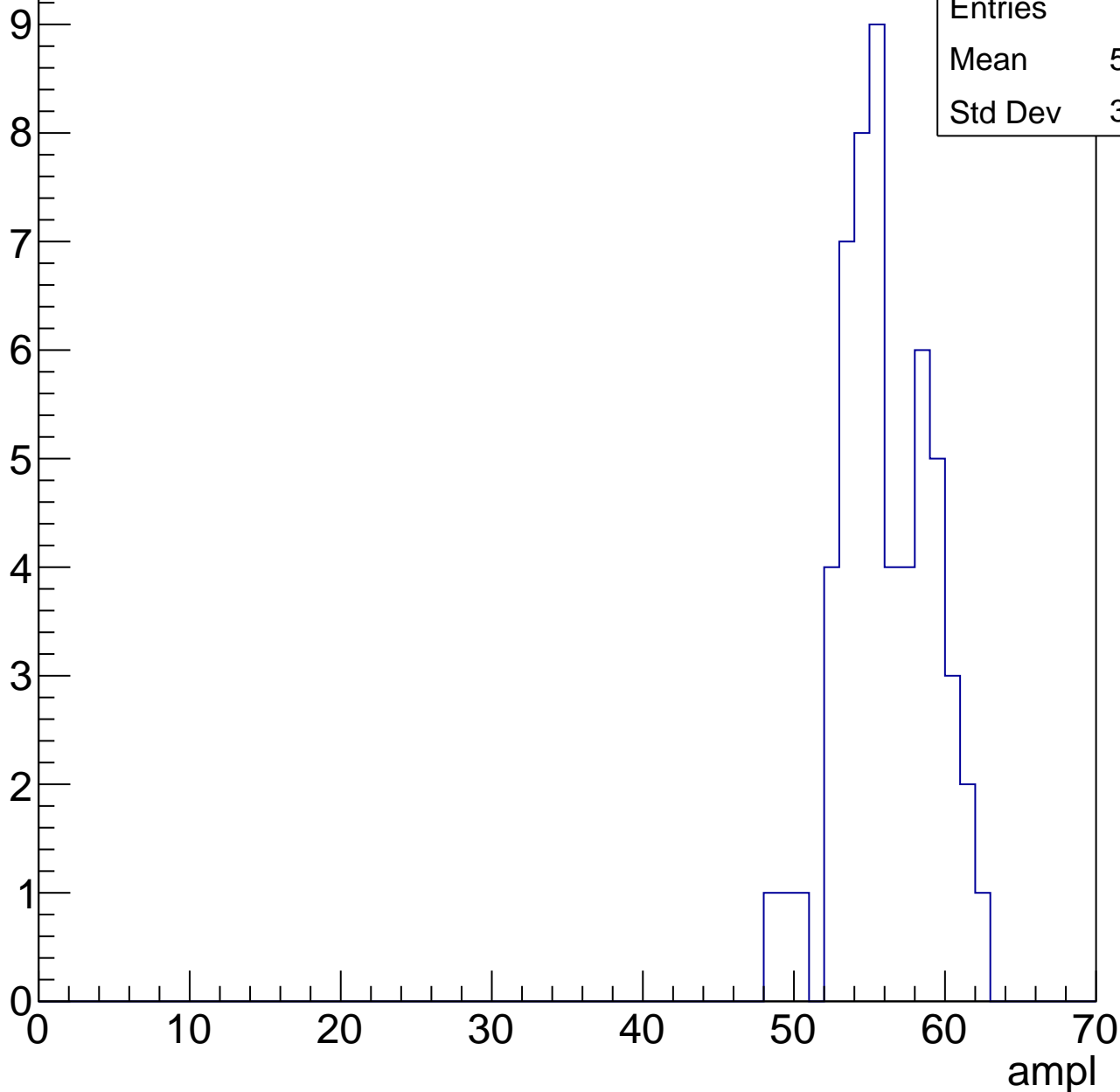


# B0L001S, U5-ch118, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	55.57
Std Dev	3.029

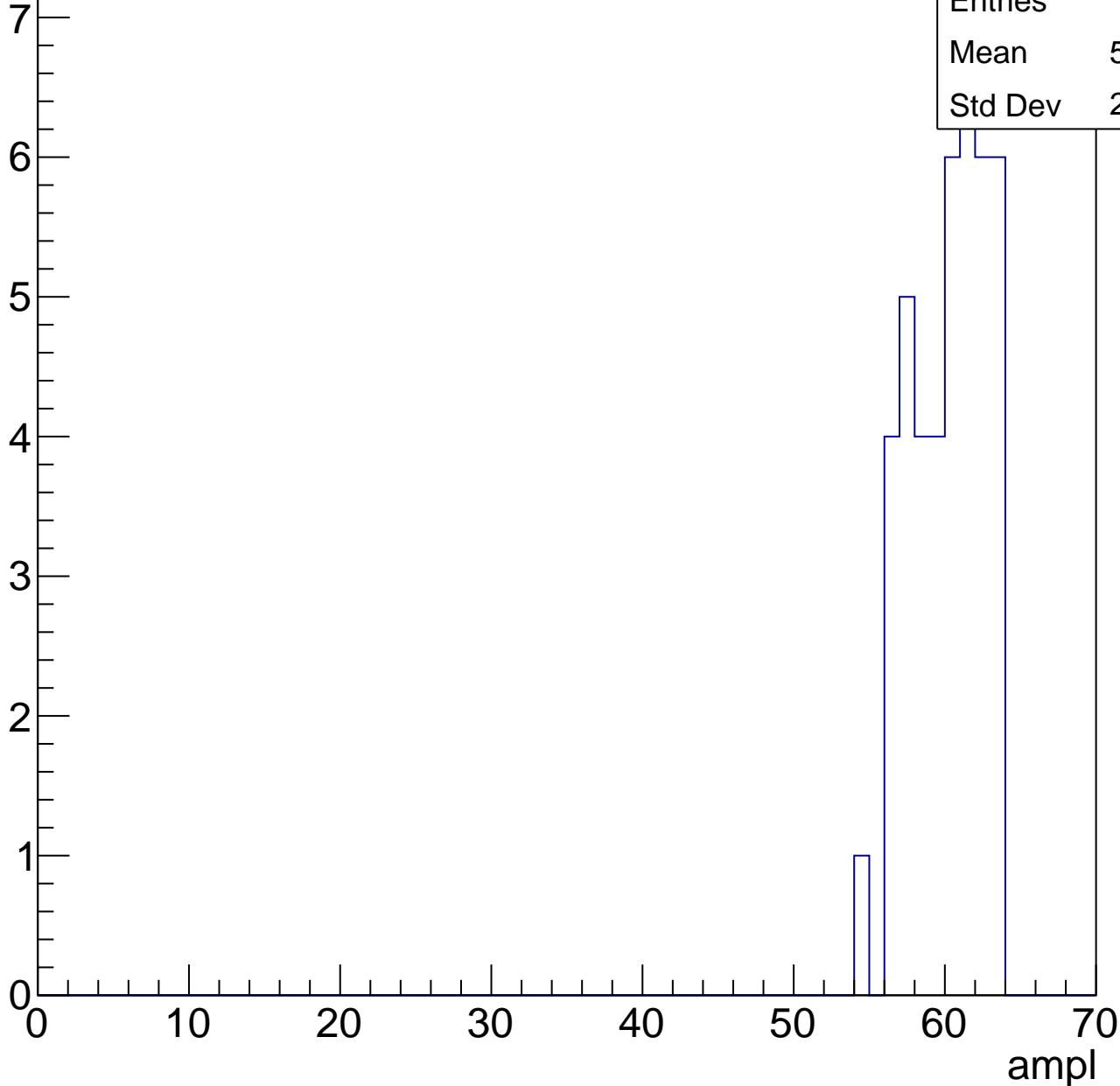


# B0L001S, U5-ch118, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

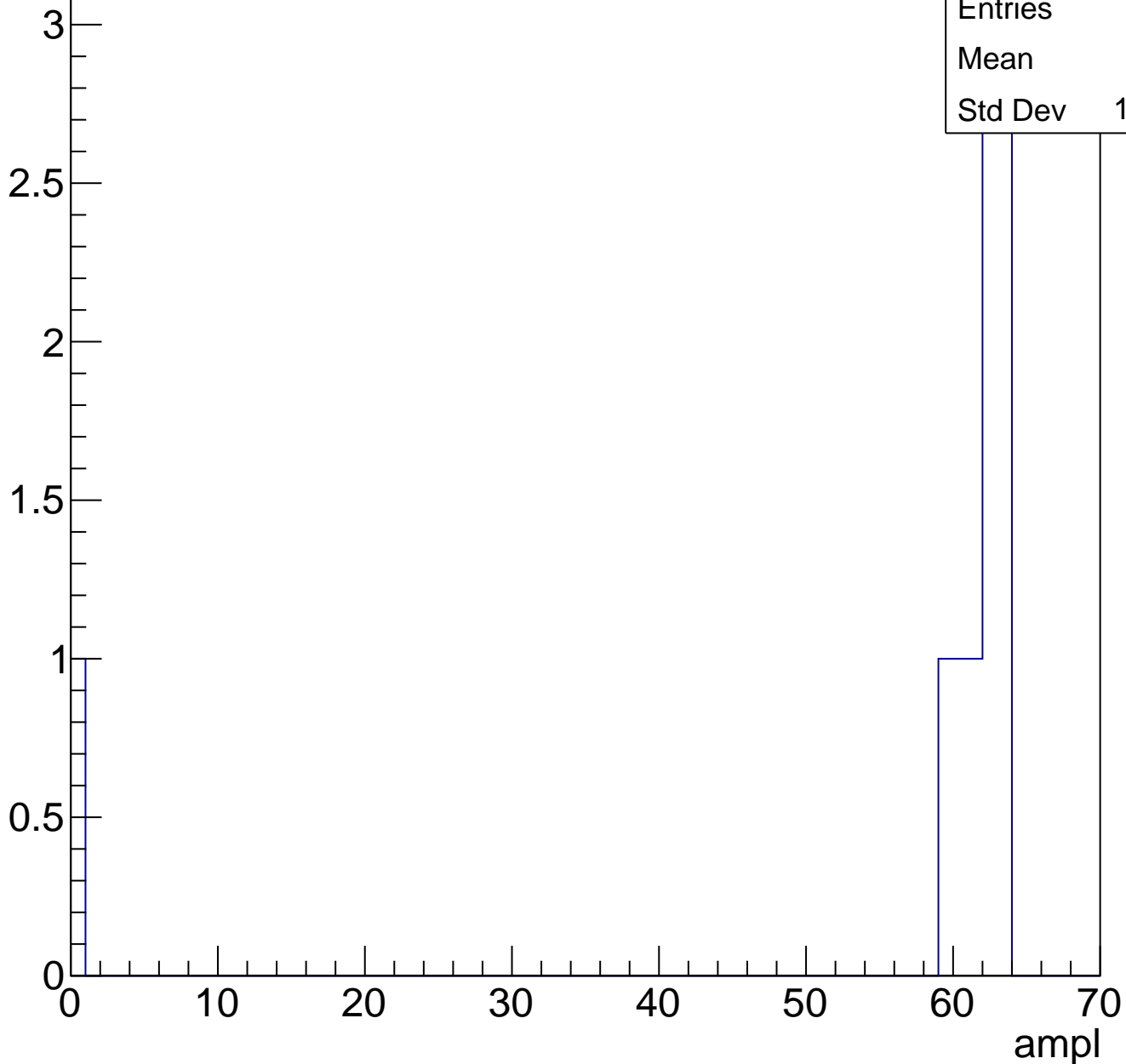
Entries	43
Mean	59.72
Std Dev	2.395



# B0L001S, U5-ch118, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch118, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch119, adc0

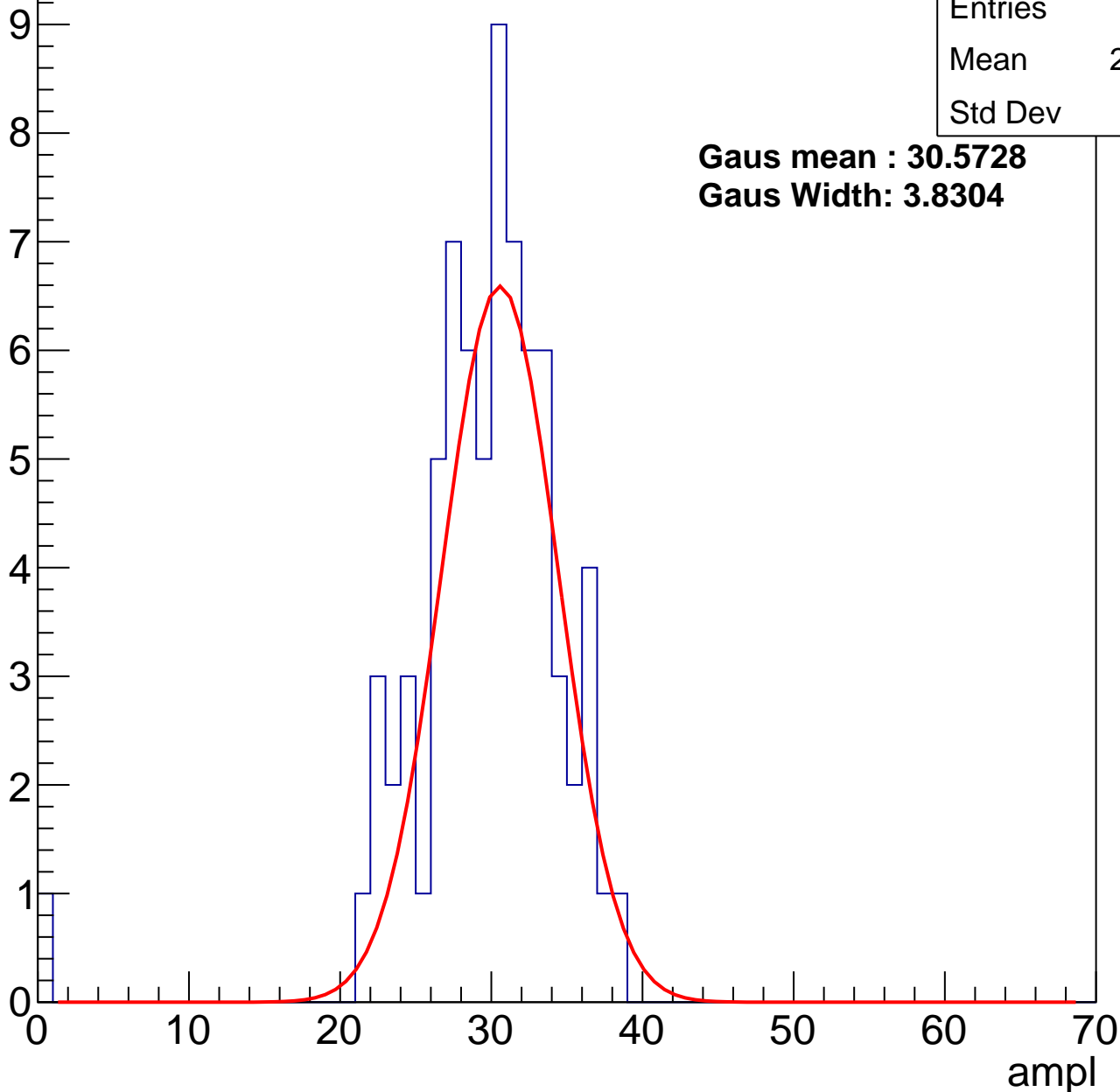
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	29.18
Std Dev	5.19

**Gaus mean : 30.5728**

**Gaus Width: 3.8304**



# B0L001S, U5-ch119, adc1

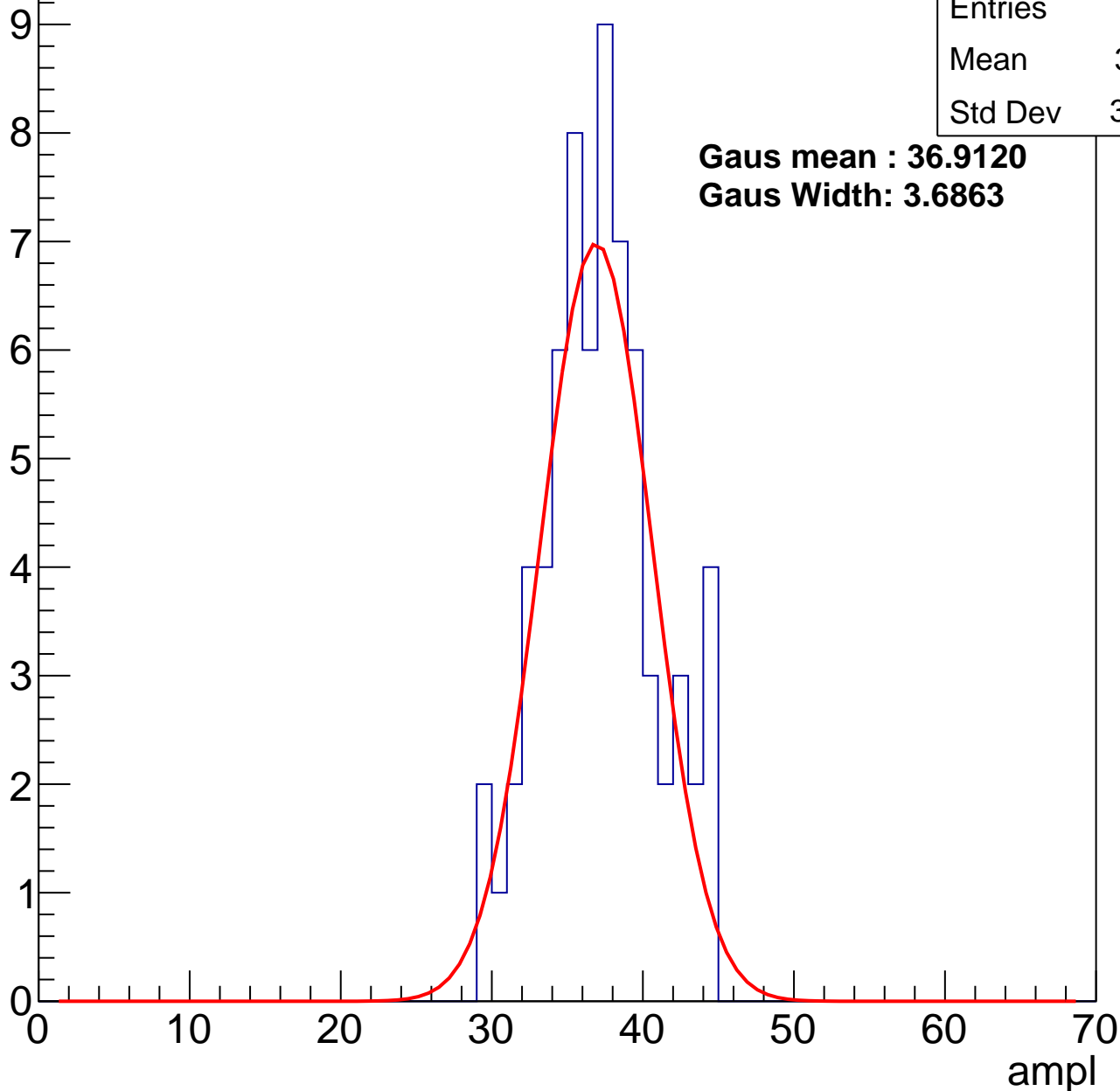
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	36.71
Std Dev	3.676

**Gaus mean : 36.9120**

**Gaus Width: 3.6863**



# B0L001S, U5-ch119, adc2

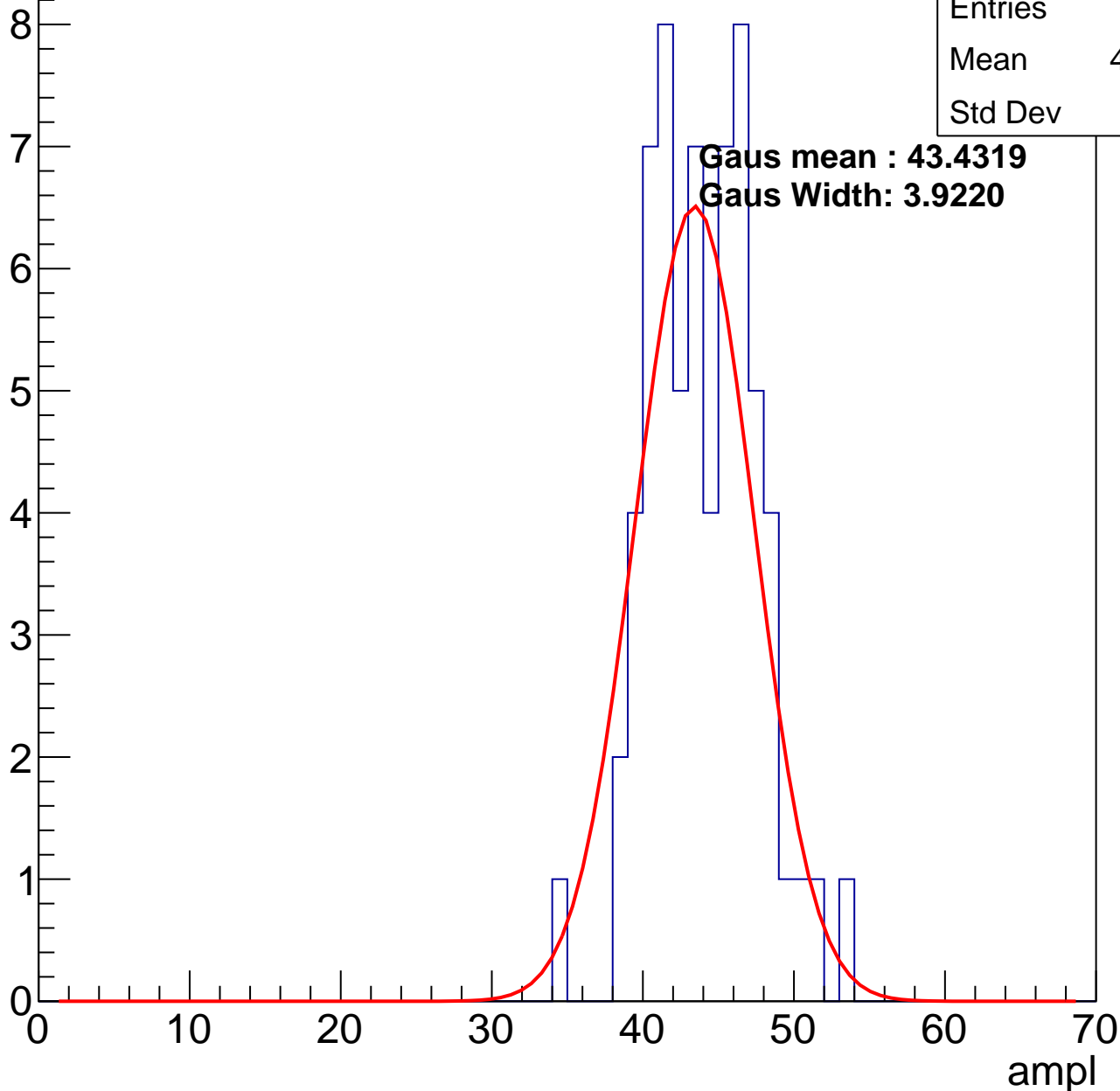
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	43.55
Std Dev	3.5

**Gaus mean : 43.4319**

**Gaus Width: 3.9220**

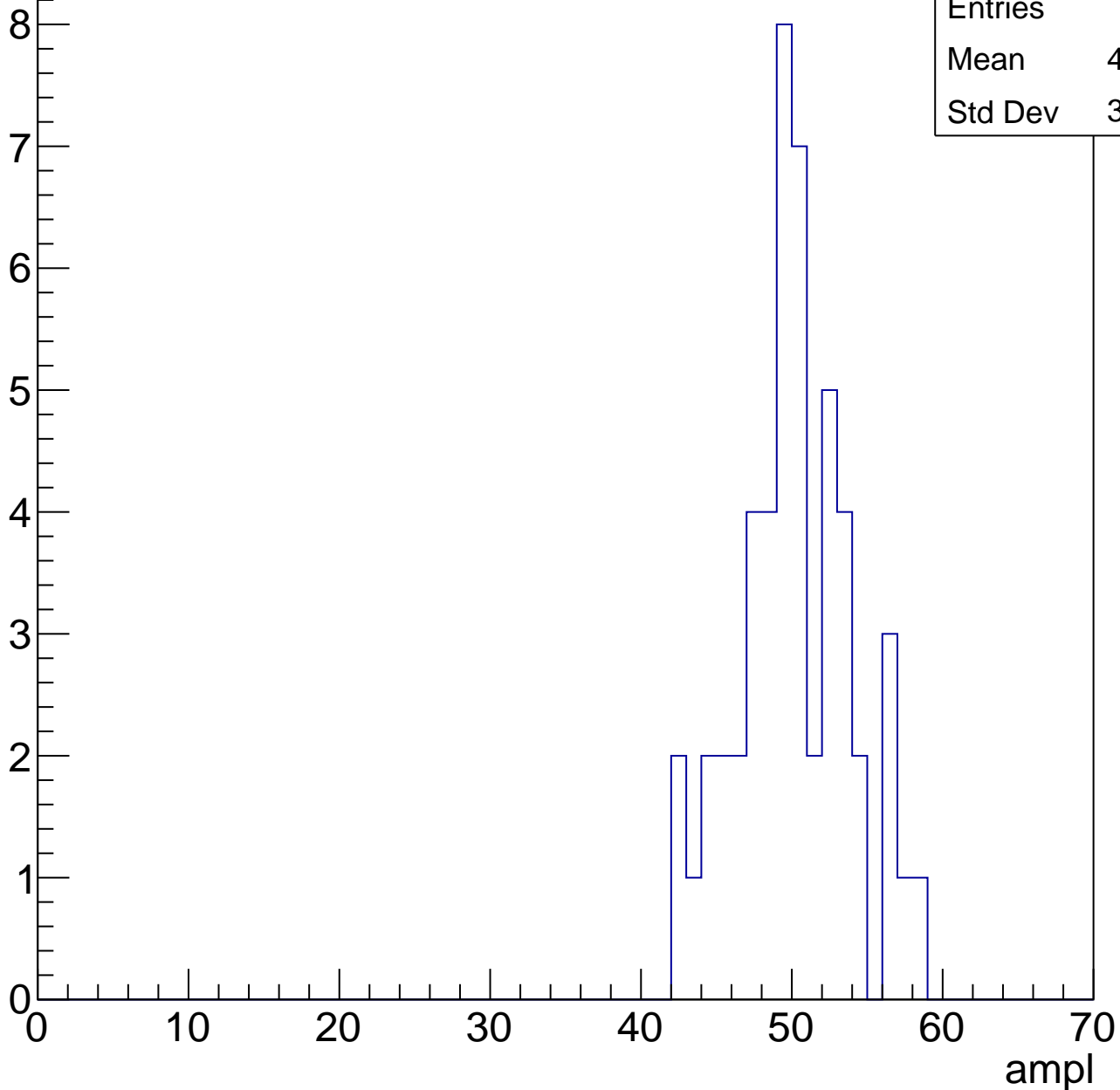


# B0L001S, U5-ch119, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	50
Mean	49.68
Std Dev	3.733

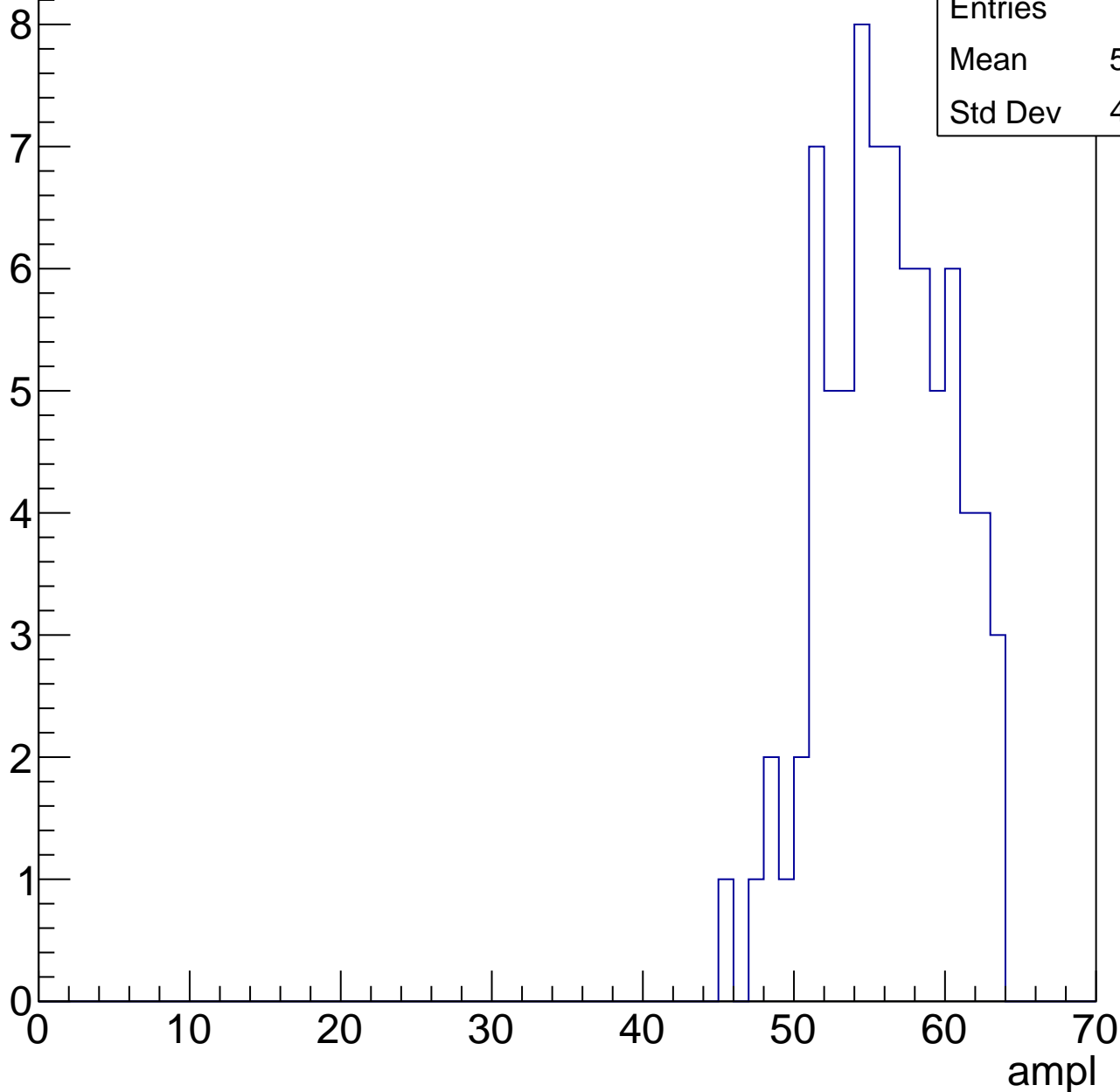


# B0L001S, U5-ch119, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	80
Mean	55.67
Std Dev	4.098

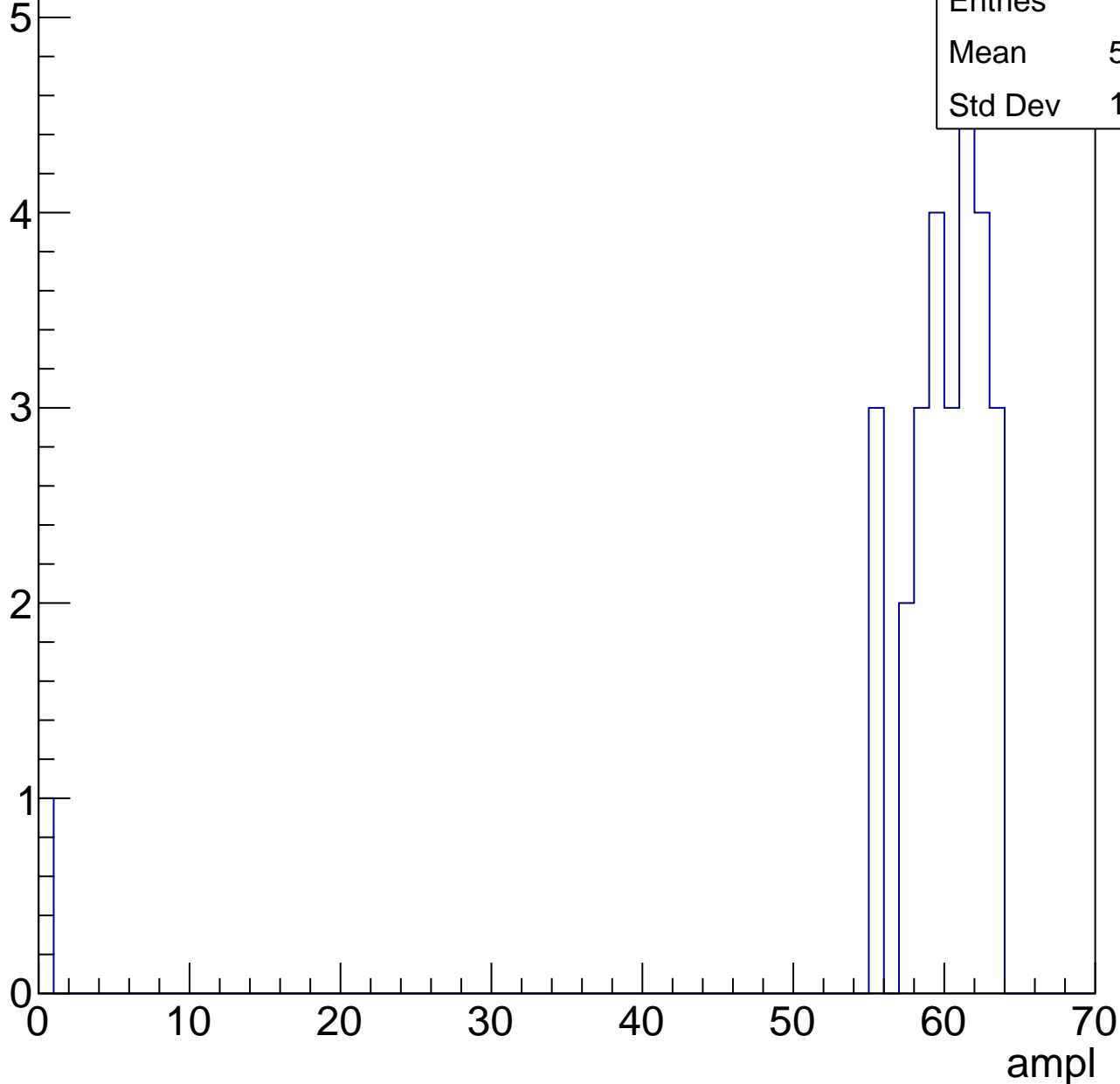


# B0L001S, U5-ch119, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	28
Mean	57.54
Std Dev	11.32



# B0L001S, U5-ch119, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

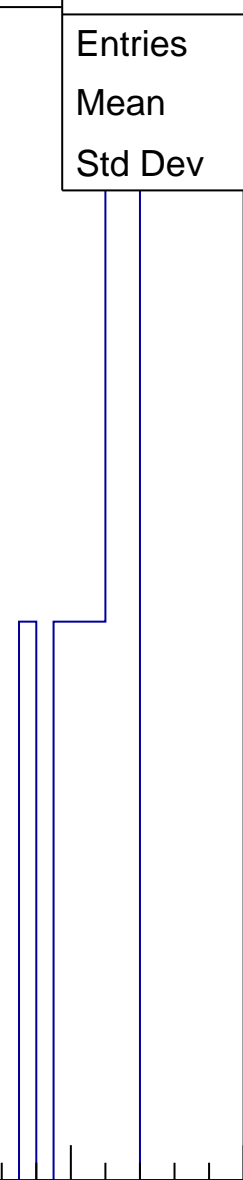
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	8
Mean	60.88
Std Dev	1.965

0 10 20 30 40 50 60 70

ampl





# B0L001S, U5-ch119, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch120, adc0

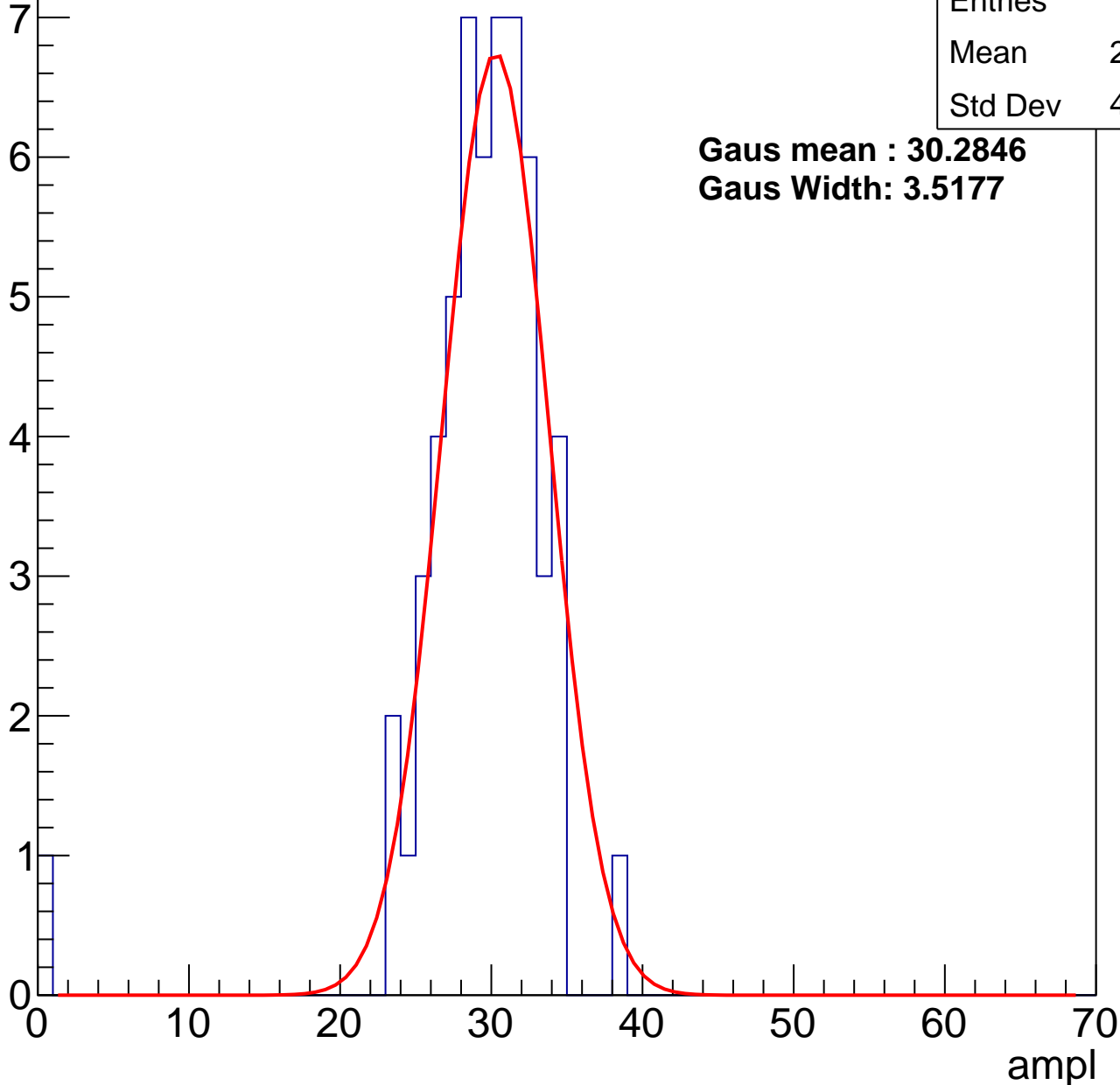
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	28.88
Std Dev	4.896

**Gaus mean : 30.2846**

**Gaus Width: 3.5177**



# B0L001S, U5-ch120, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	81
Mean	36.16
Std Dev	5.514

**Gaus mean : 37.2759**

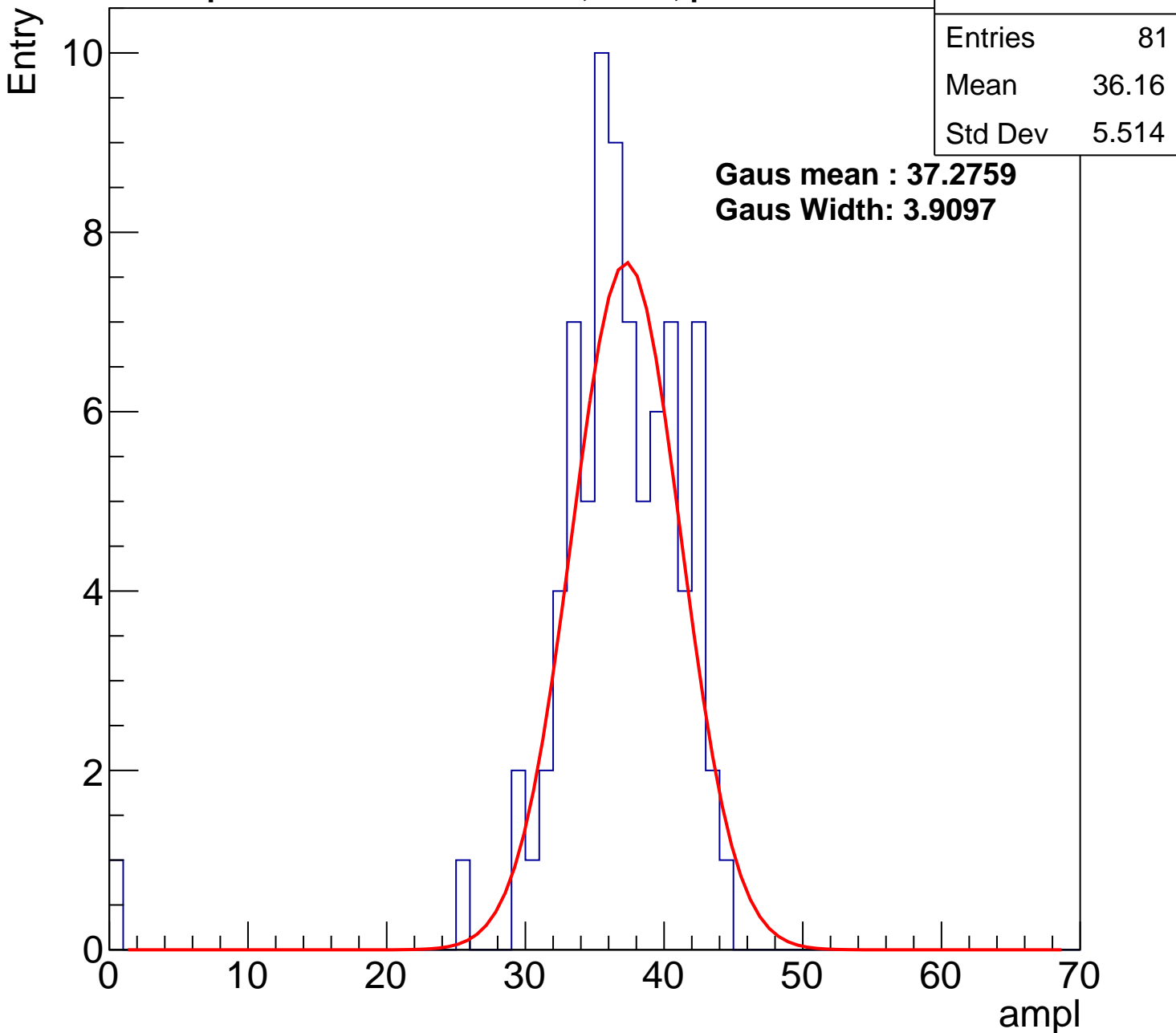
**Gaus Width: 3.9097**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U5-ch120, adc2

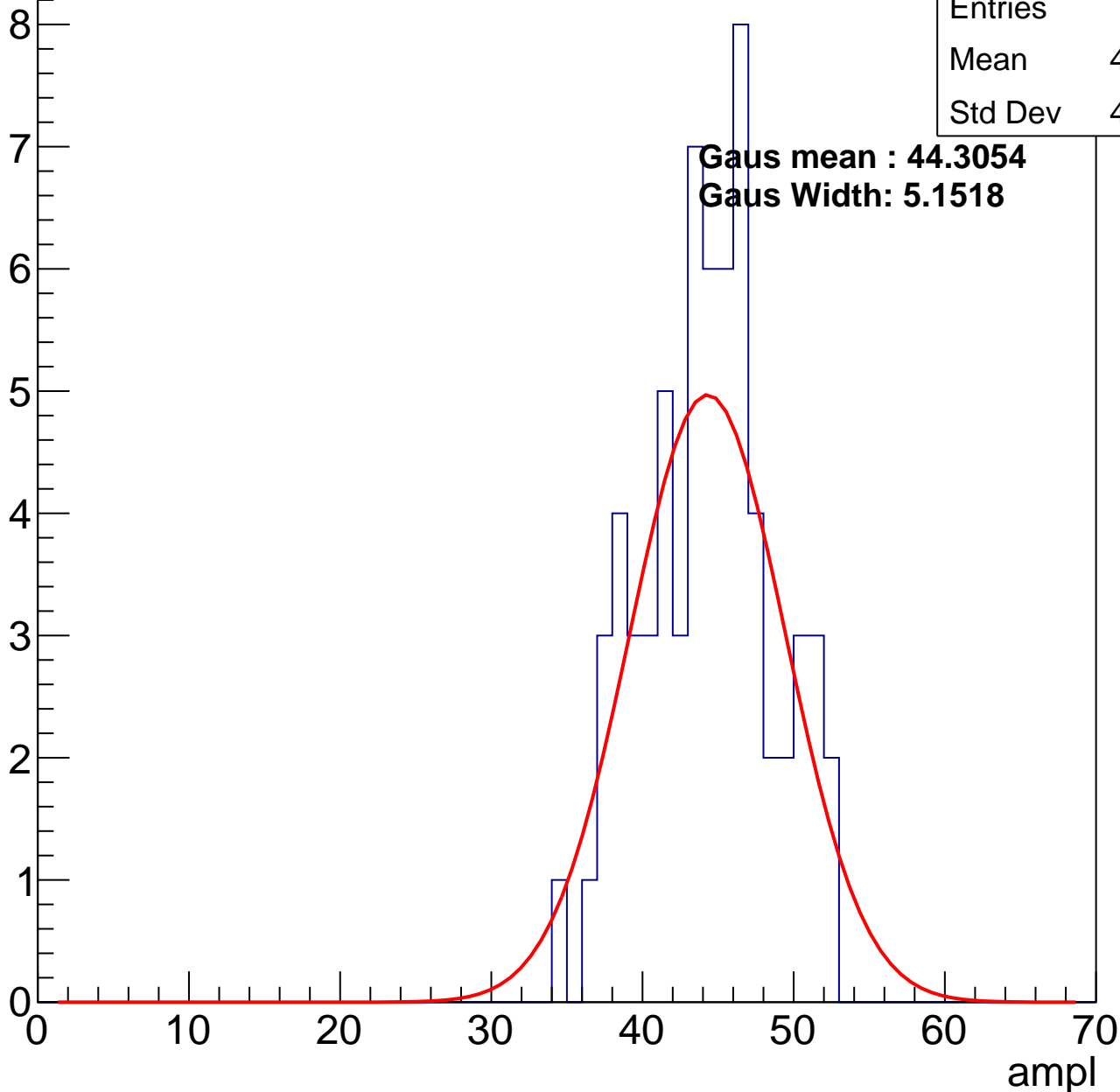
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	43.83
Std Dev	4.227

**Gaus mean : 44.3054**

**Gaus Width: 5.1518**

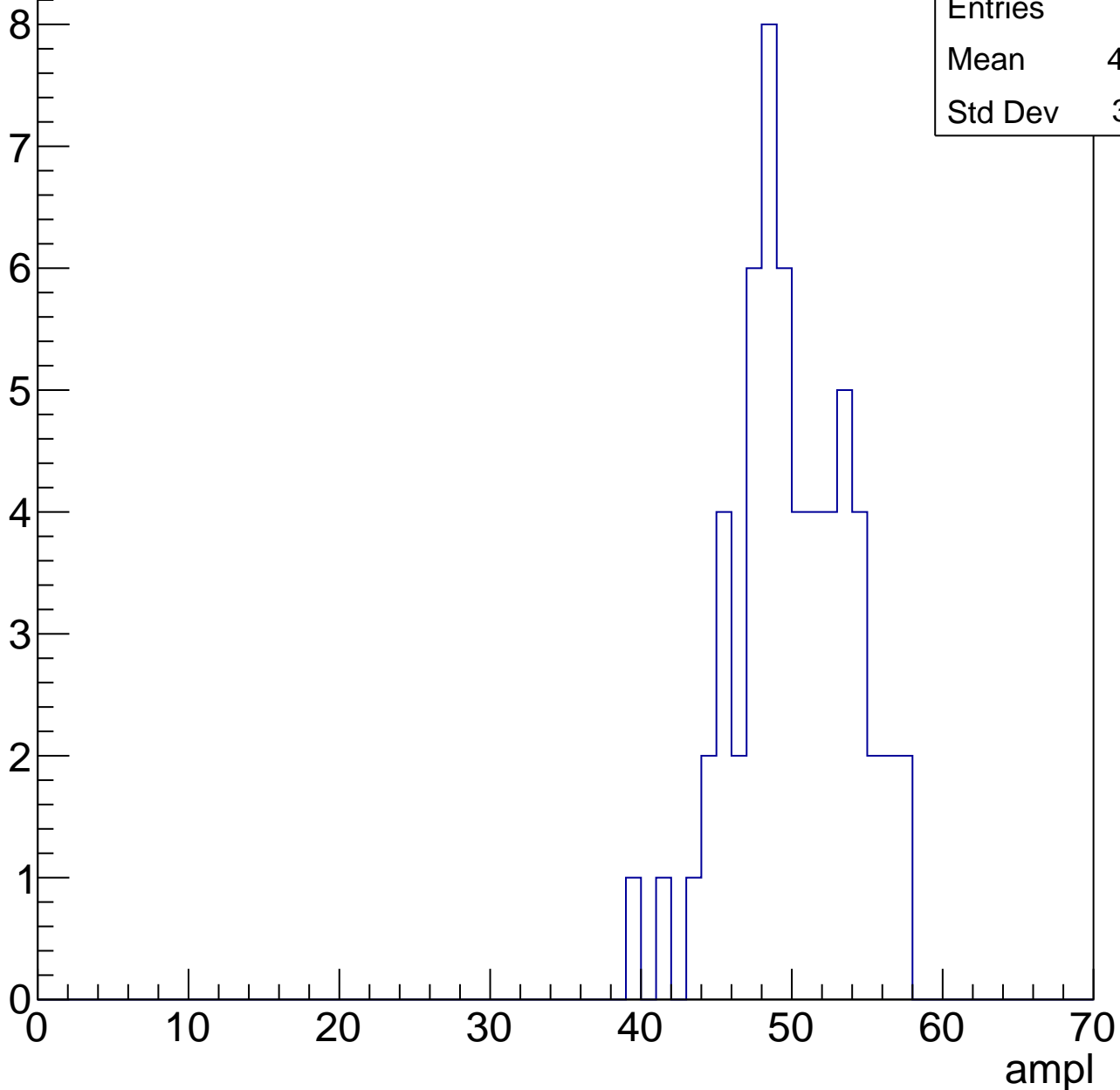


# B0L001S, U5-ch120, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	49.52
Std Dev	3.901

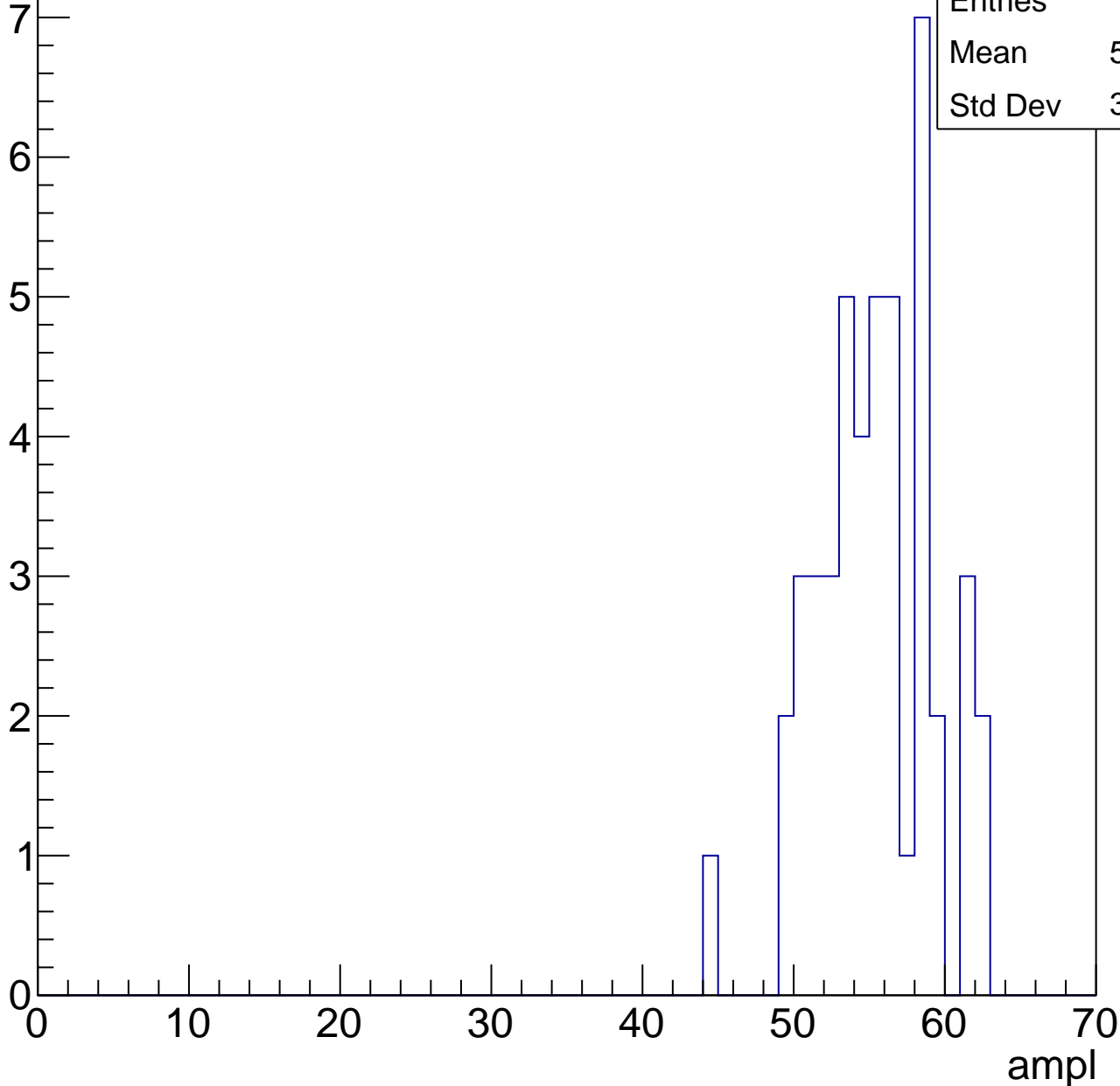


# B0L001S, U5-ch120, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	46
Mean	54.89
Std Dev	3.835

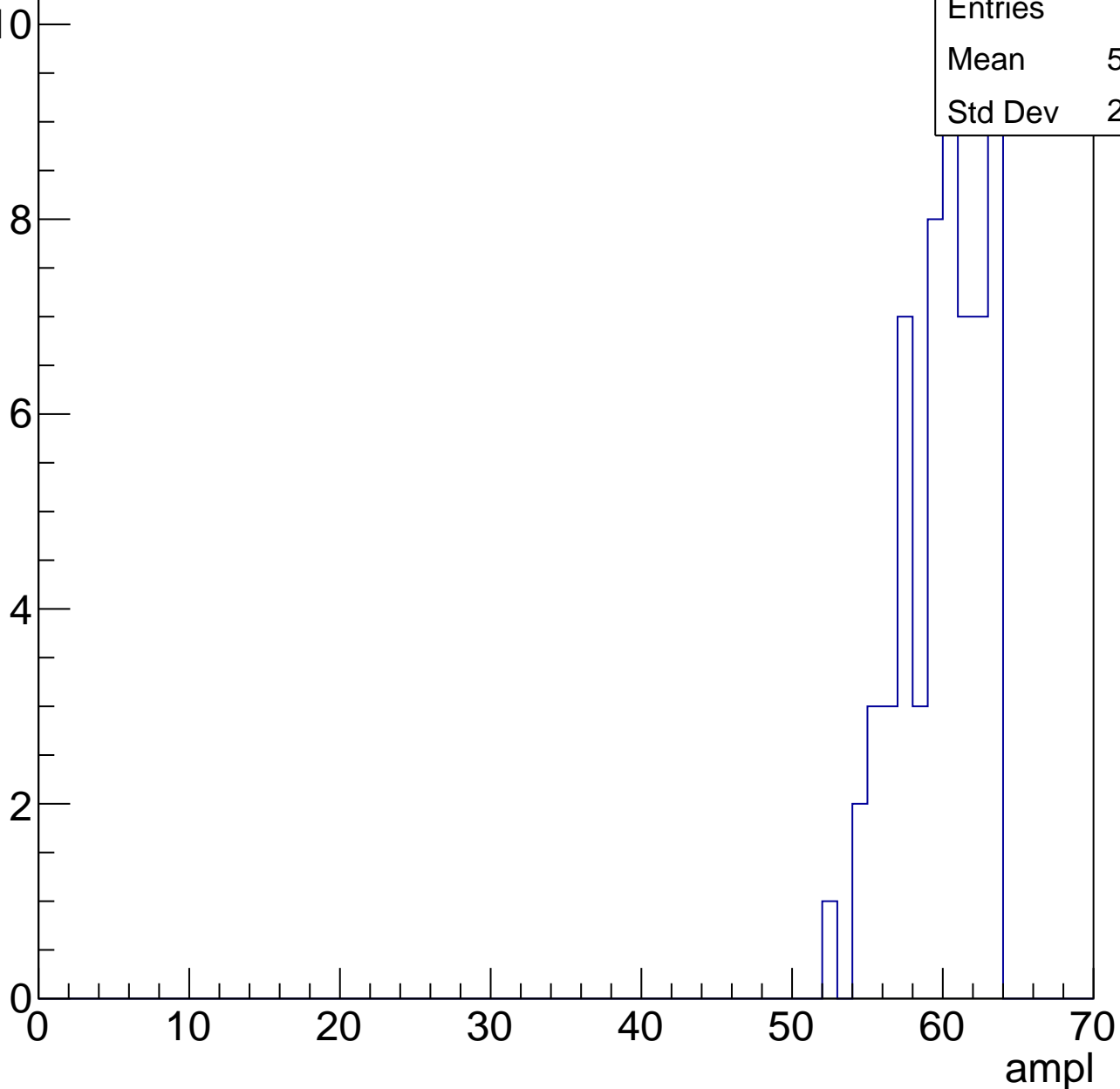


# B0L001S, U5-ch120, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

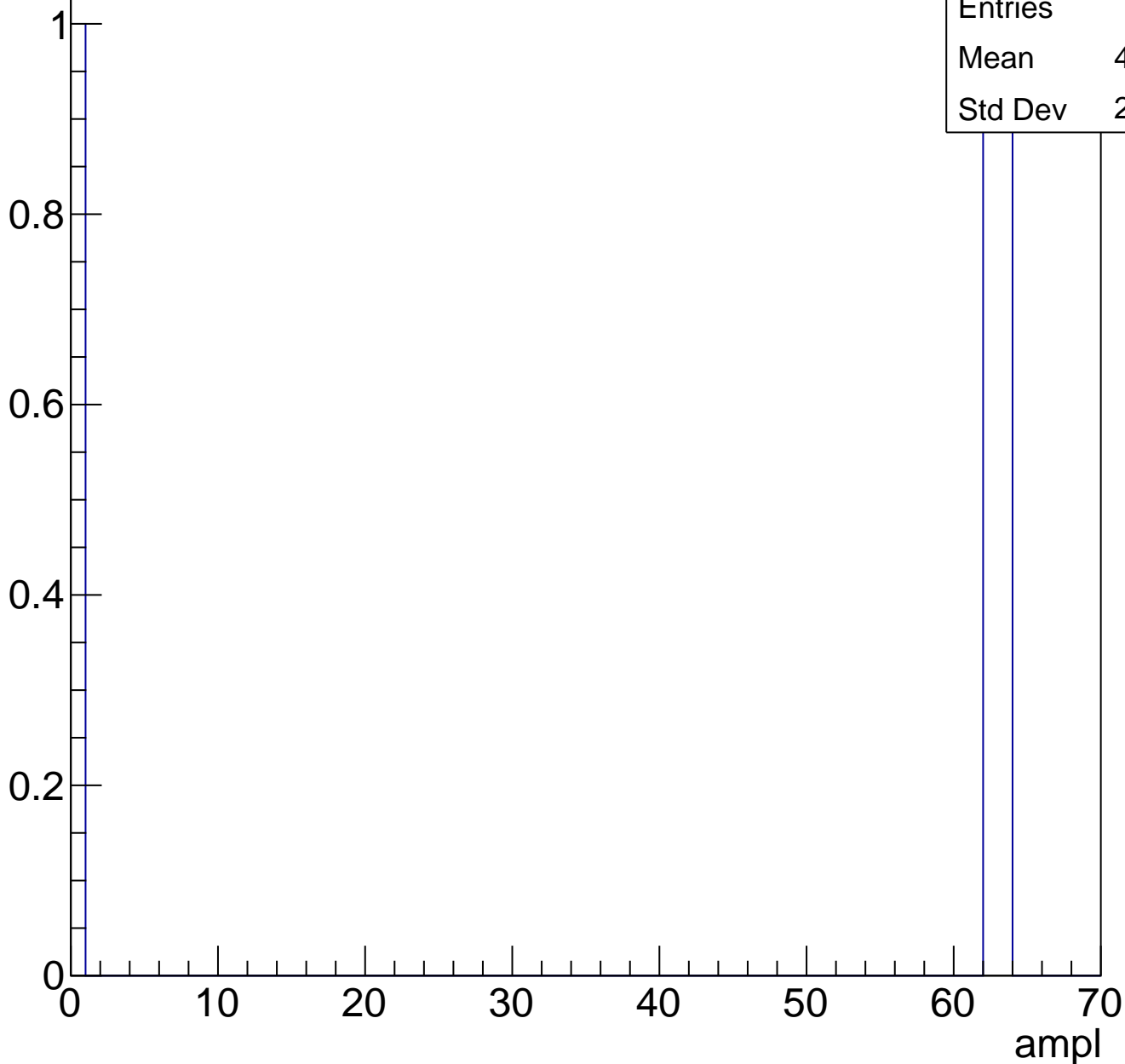
Entries	60
Mean	59.43
Std Dev	2.704



# B0L001S, U5-ch120, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch120, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch121, adc0

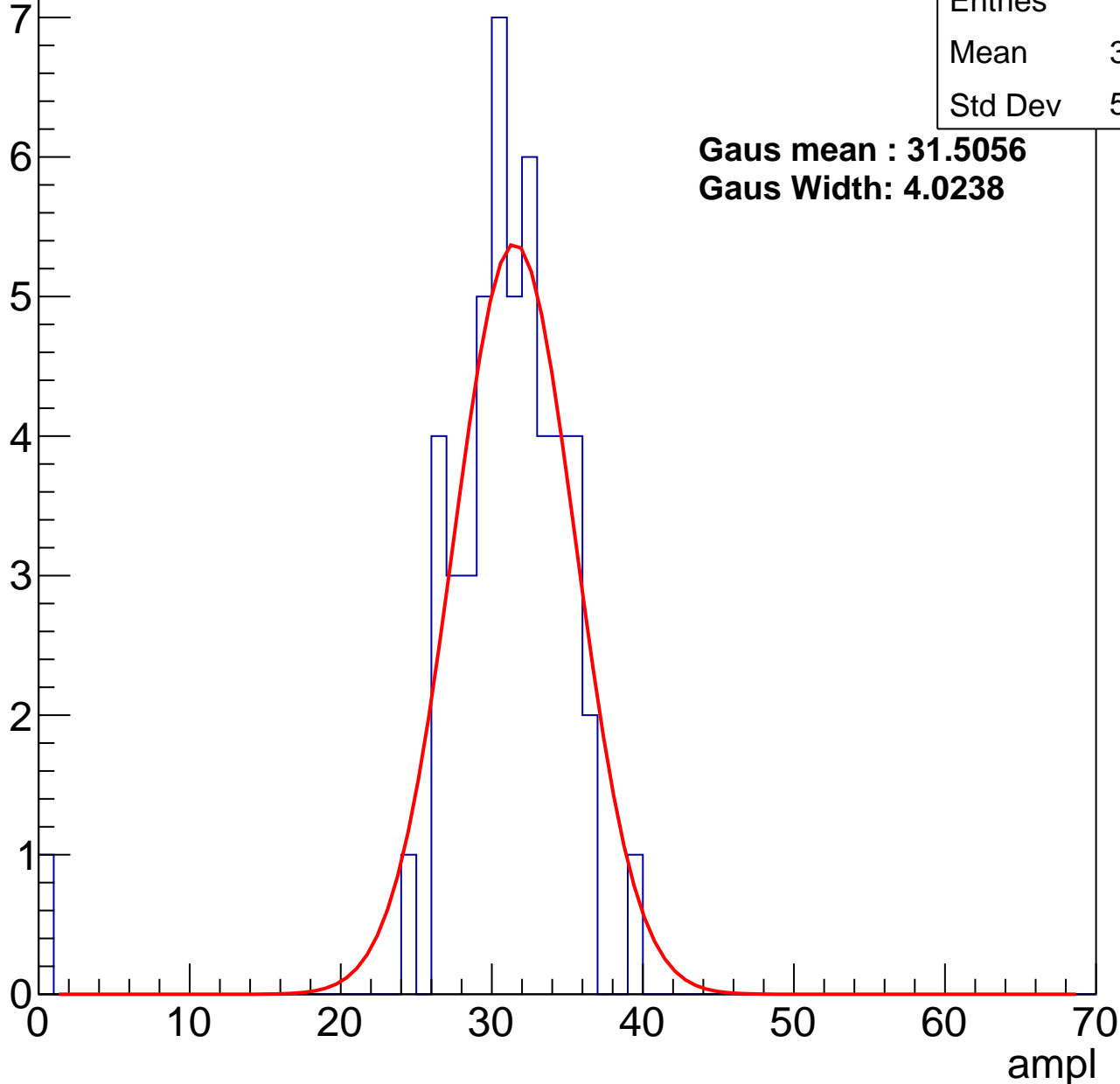
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	50
Mean	30.28
Std Dev	5.333

**Gaus mean : 31.5056**

**Gaus Width: 4.0238**



# B0L001S, U5-ch121, adc1

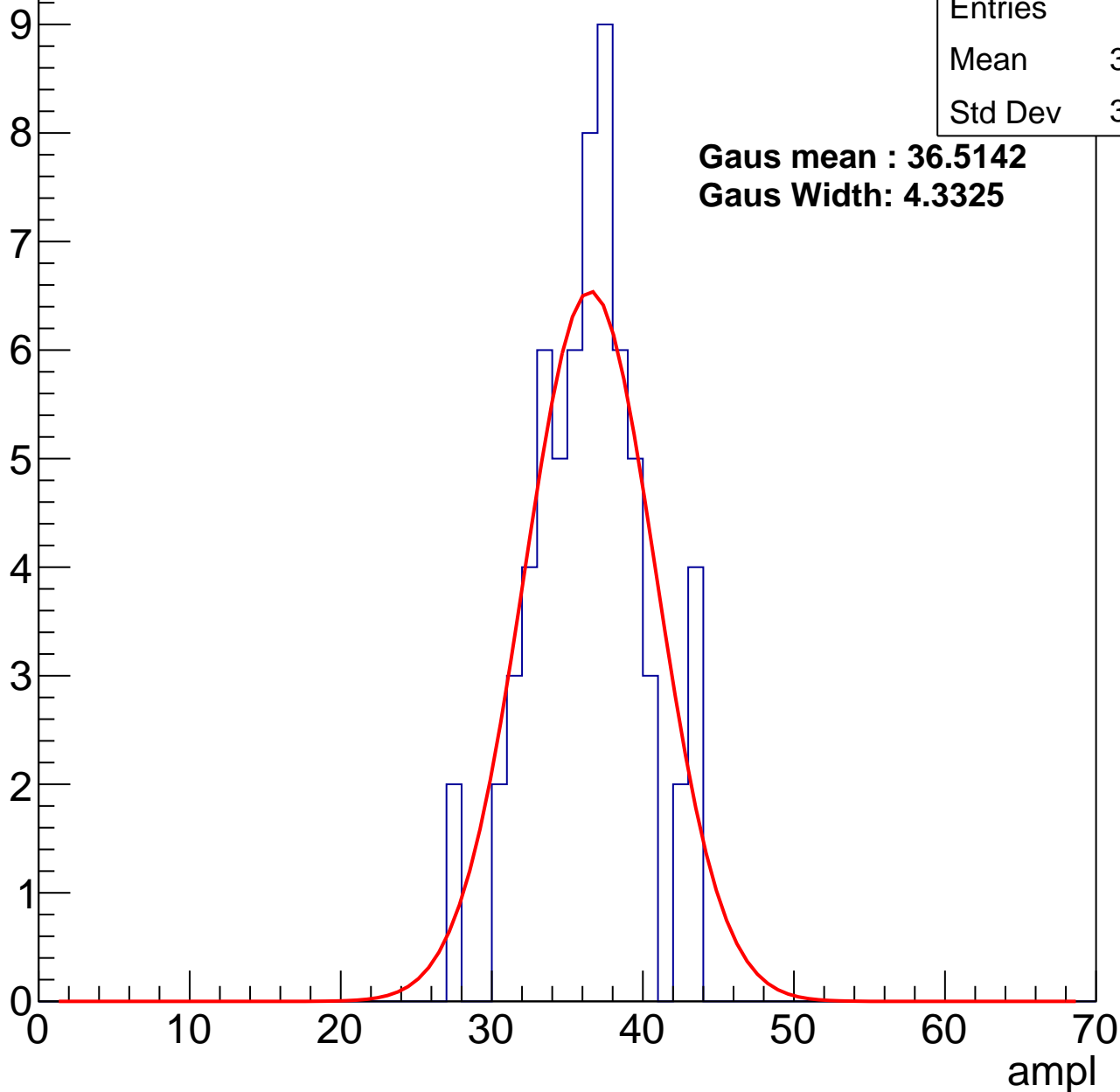
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	35.89
Std Dev	3.608

**Gaus mean : 36.5142**

**Gaus Width: 4.3325**



# B0L001S, U5-ch121, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	62
Mean	42.61
Std Dev	3.338

**Gaus mean : 43.2476**

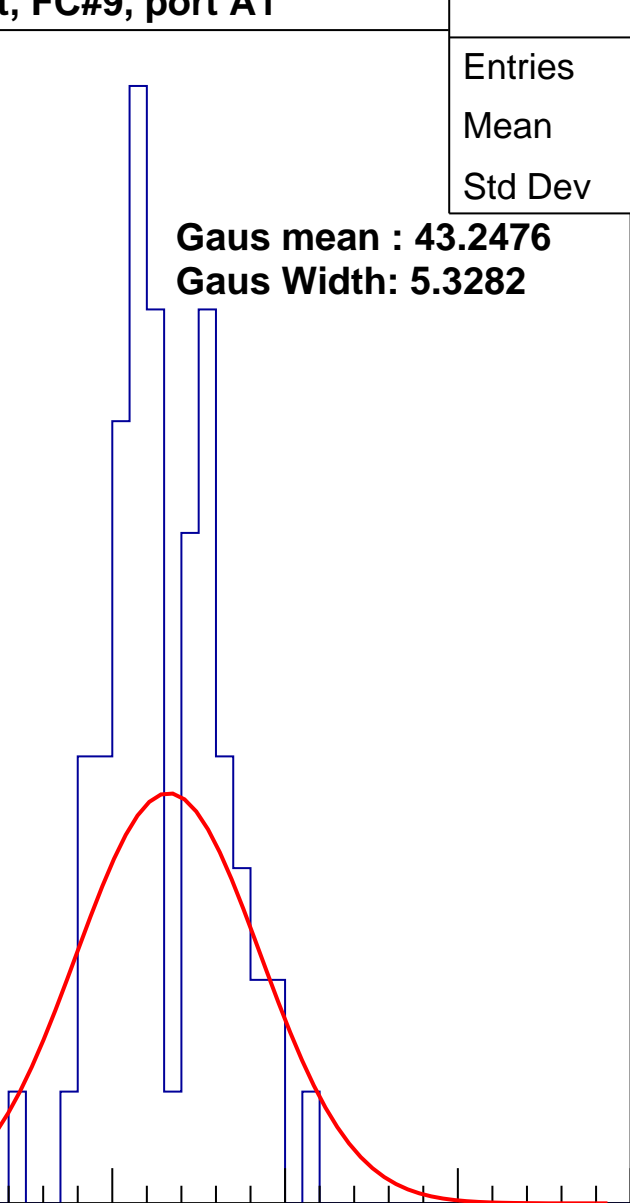
**Gaus Width: 5.3282**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

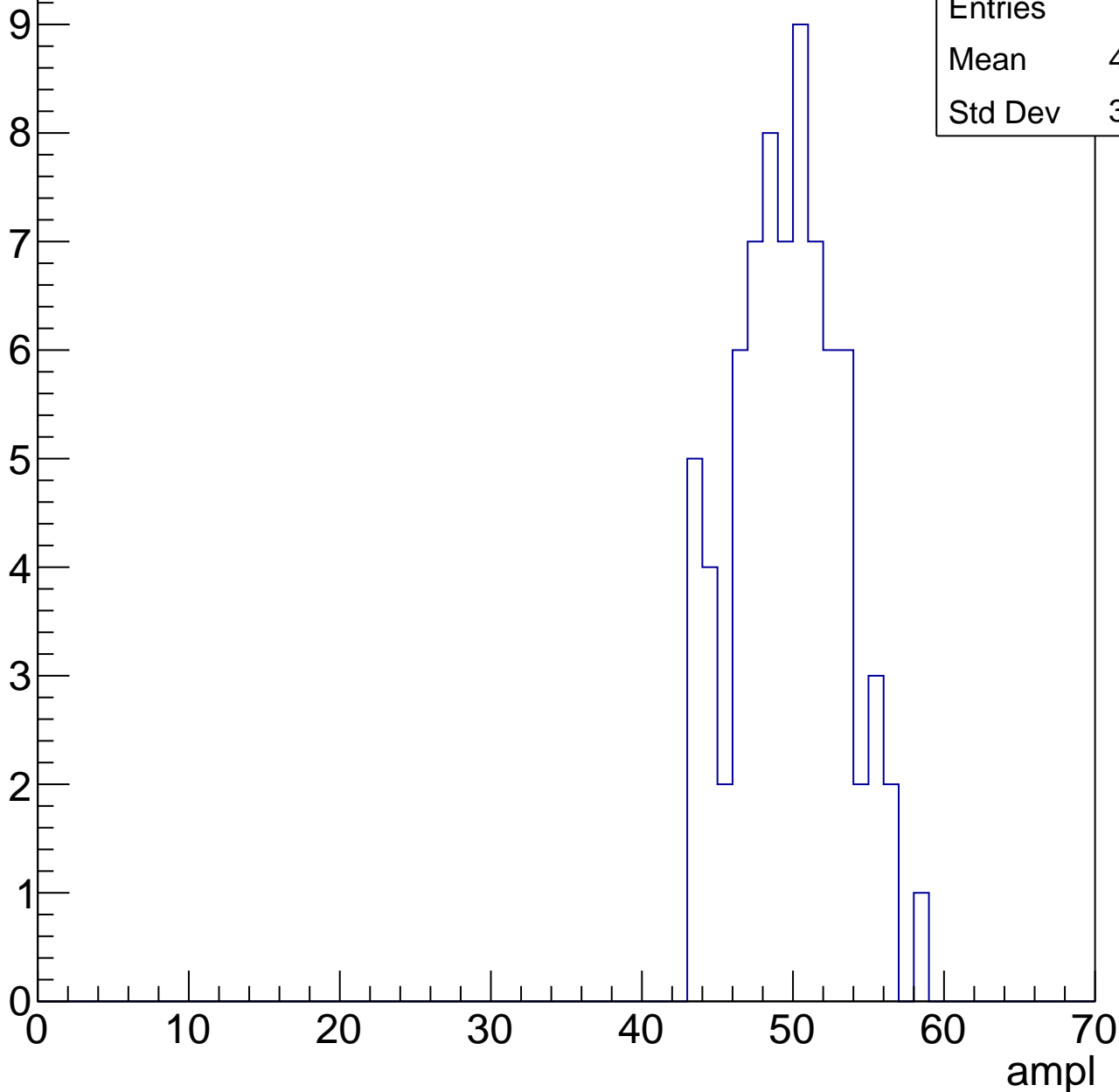


# B0L001S, U5-ch121, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	75
Mean	49.24
Std Dev	3.506

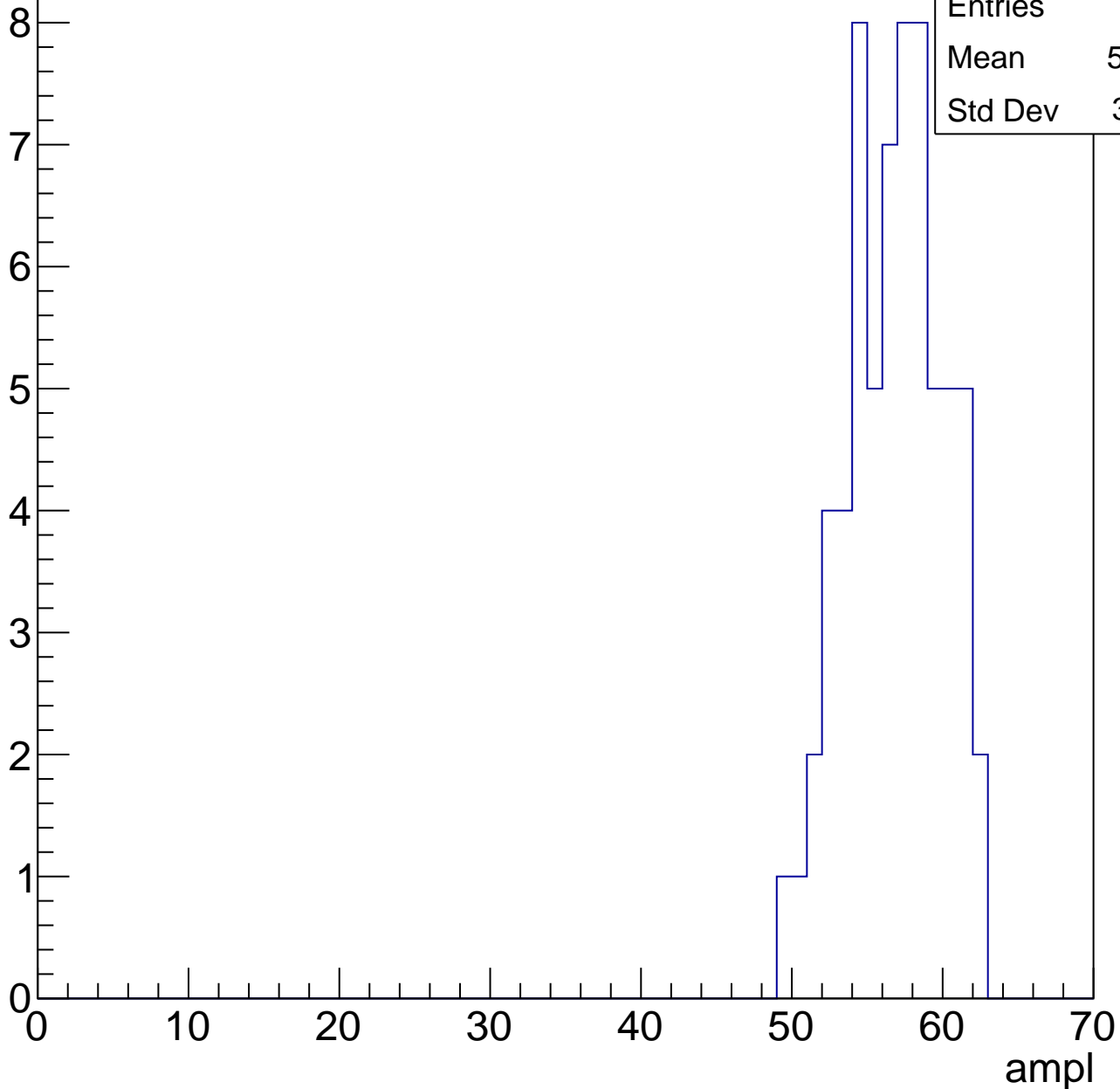


# B0L001S, U5-ch121, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

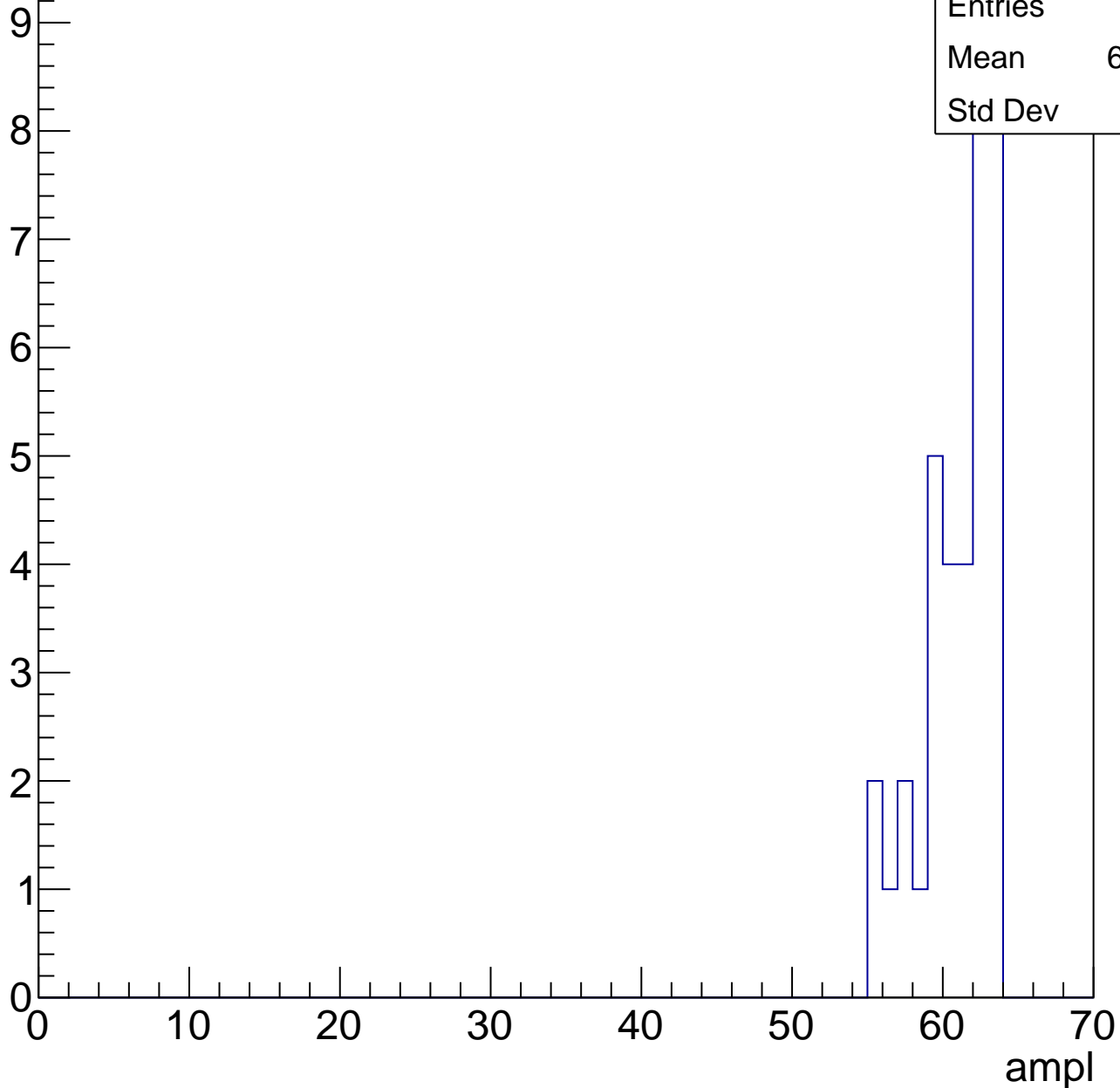
Entries	65
Mean	56.37
Std Dev	3.101



# B0L001S, U5-ch121, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

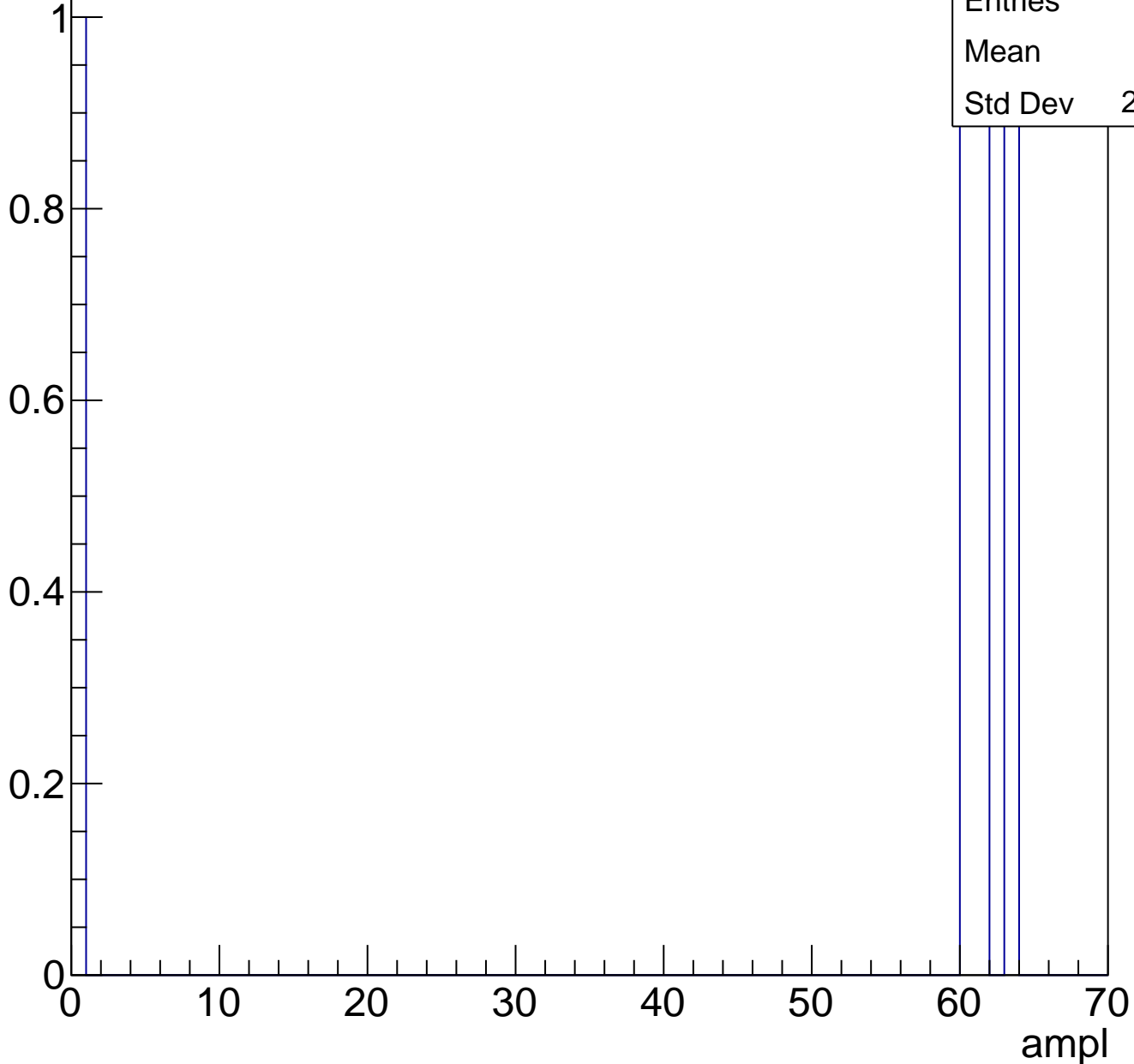


Entries	36
Mean	60.56
Std Dev	2.35

# B0L001S, U5-ch121, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch121, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch122, adc0

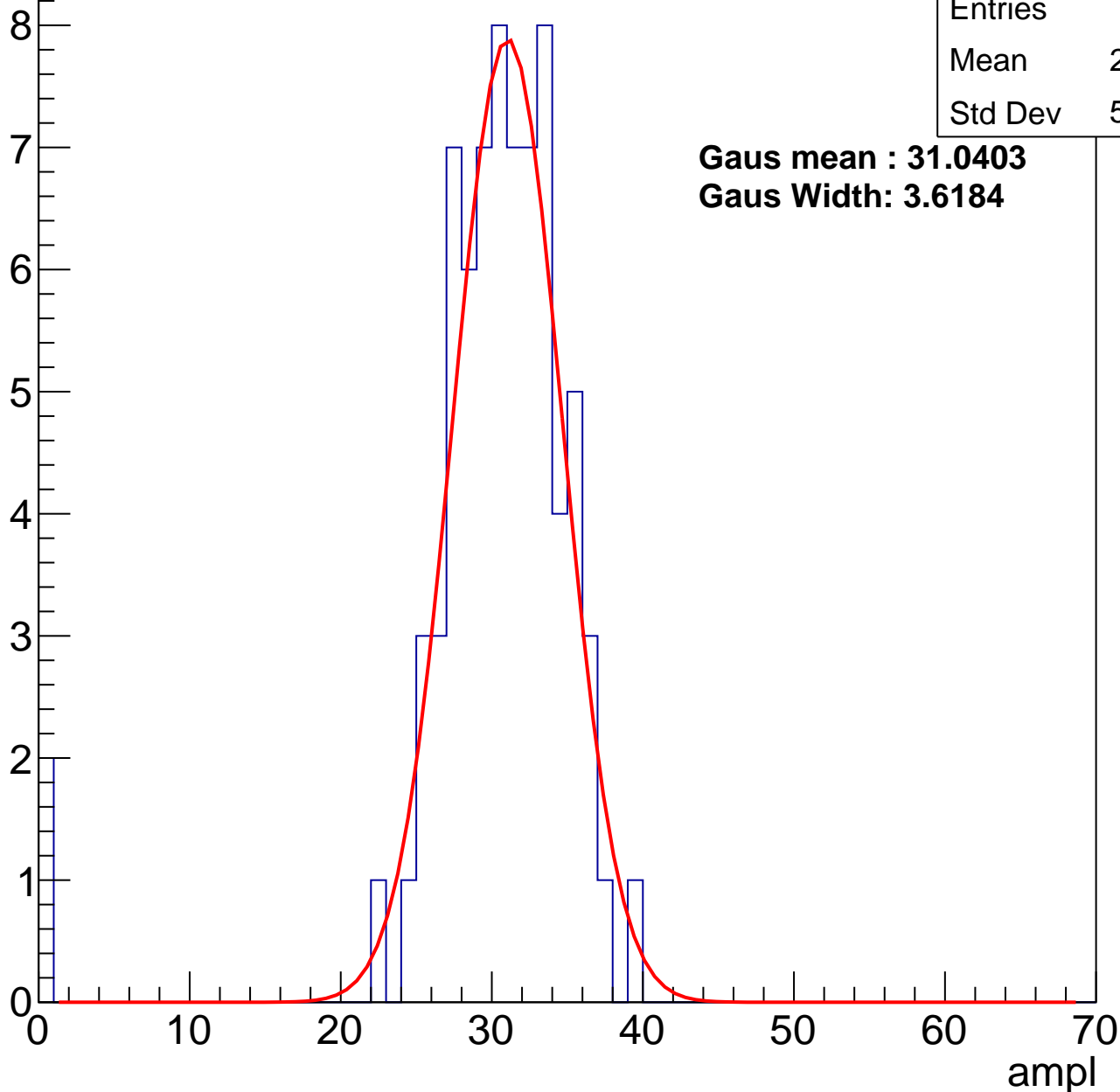
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	29.72
Std Dev	5.979

**Gaus mean : 31.0403**

**Gaus Width: 3.6184**



# B0L001S, U5-ch122, adc1

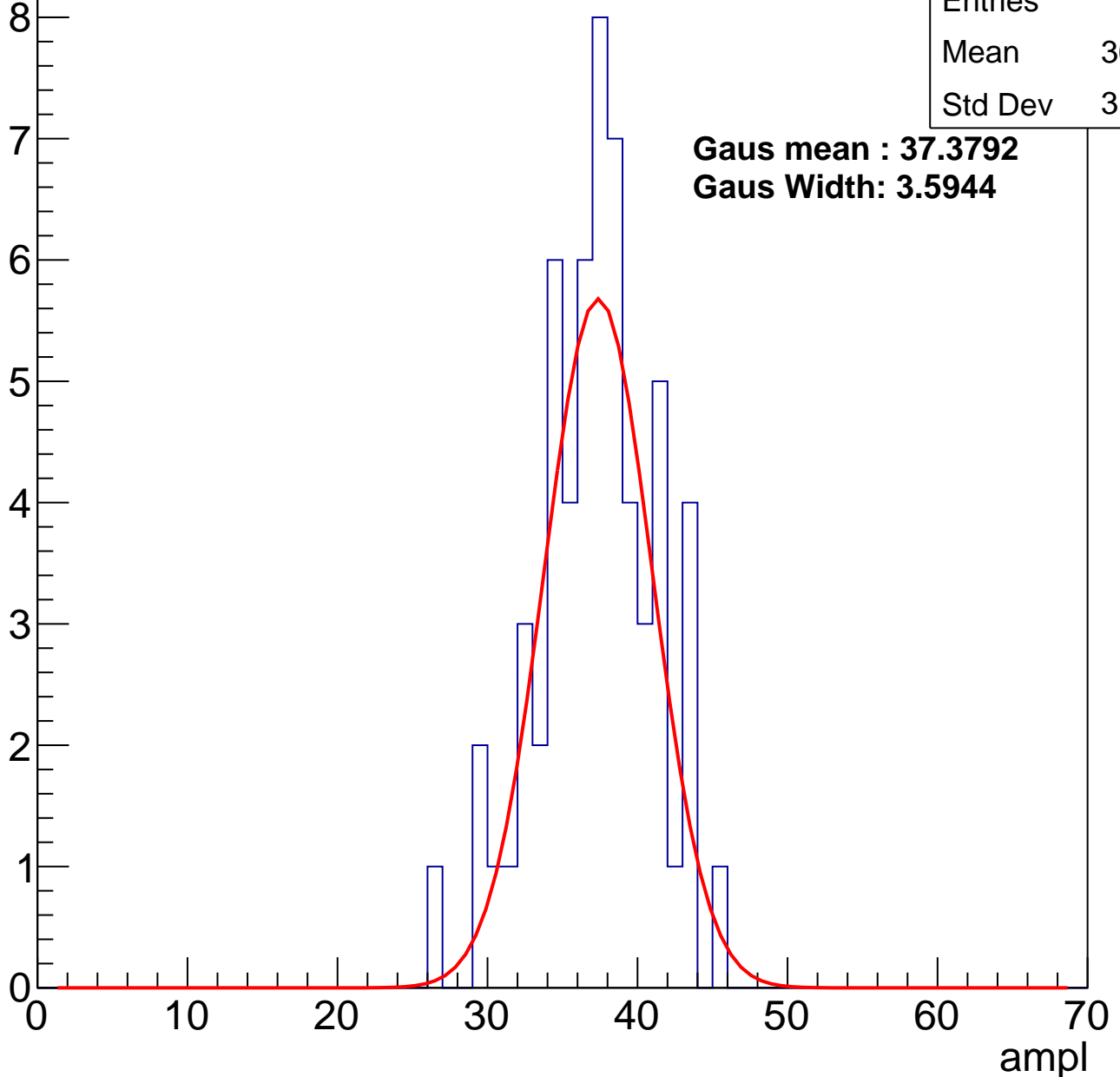
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	36.76
Std Dev	3.855

**Gaus mean : 37.3792**

**Gaus Width: 3.5944**



# B0L001S, U5-ch122, adc2

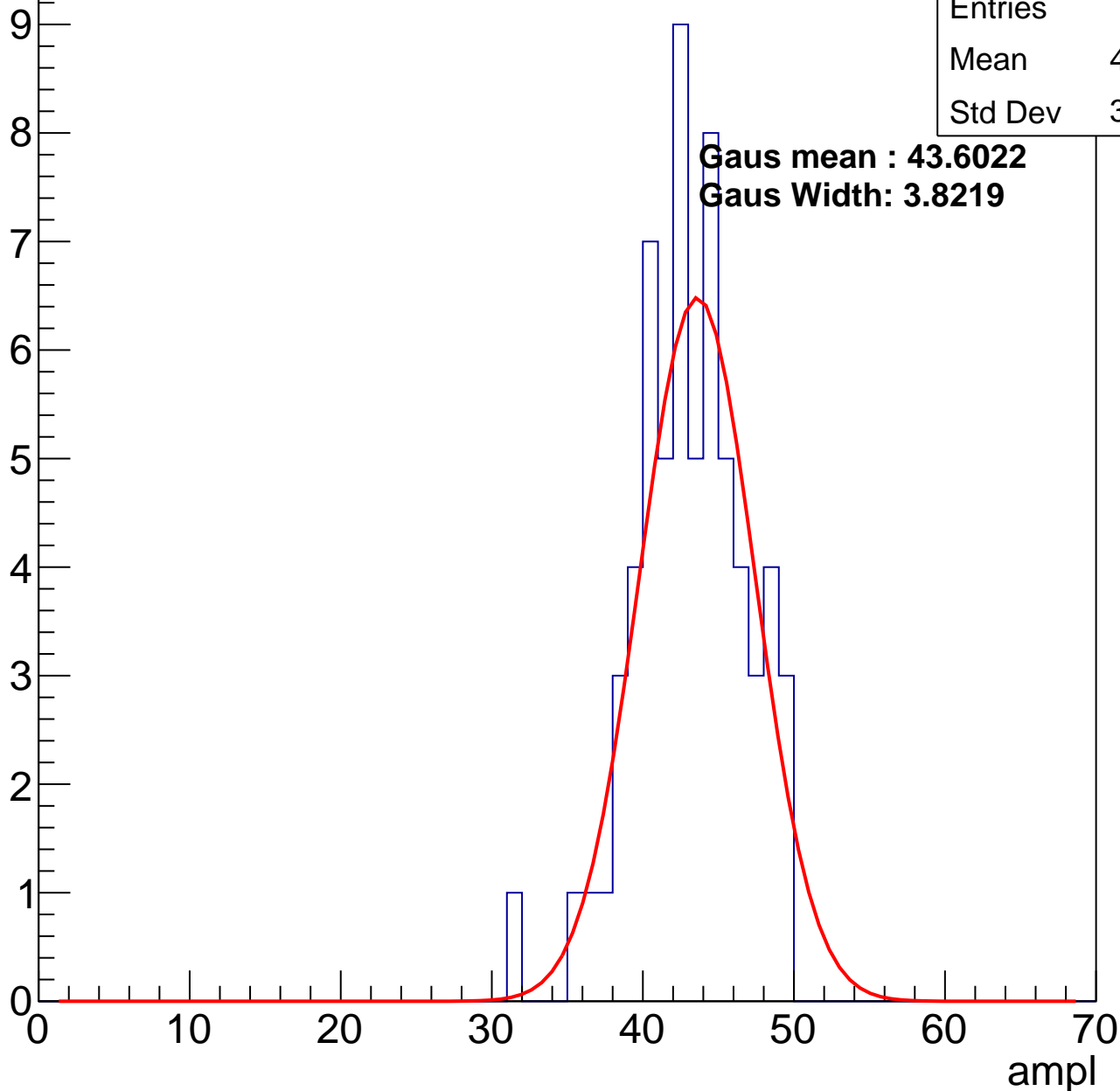
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	42.62
Std Dev	3.612

**Gaus mean : 43.6022**

**Gaus Width: 3.8219**

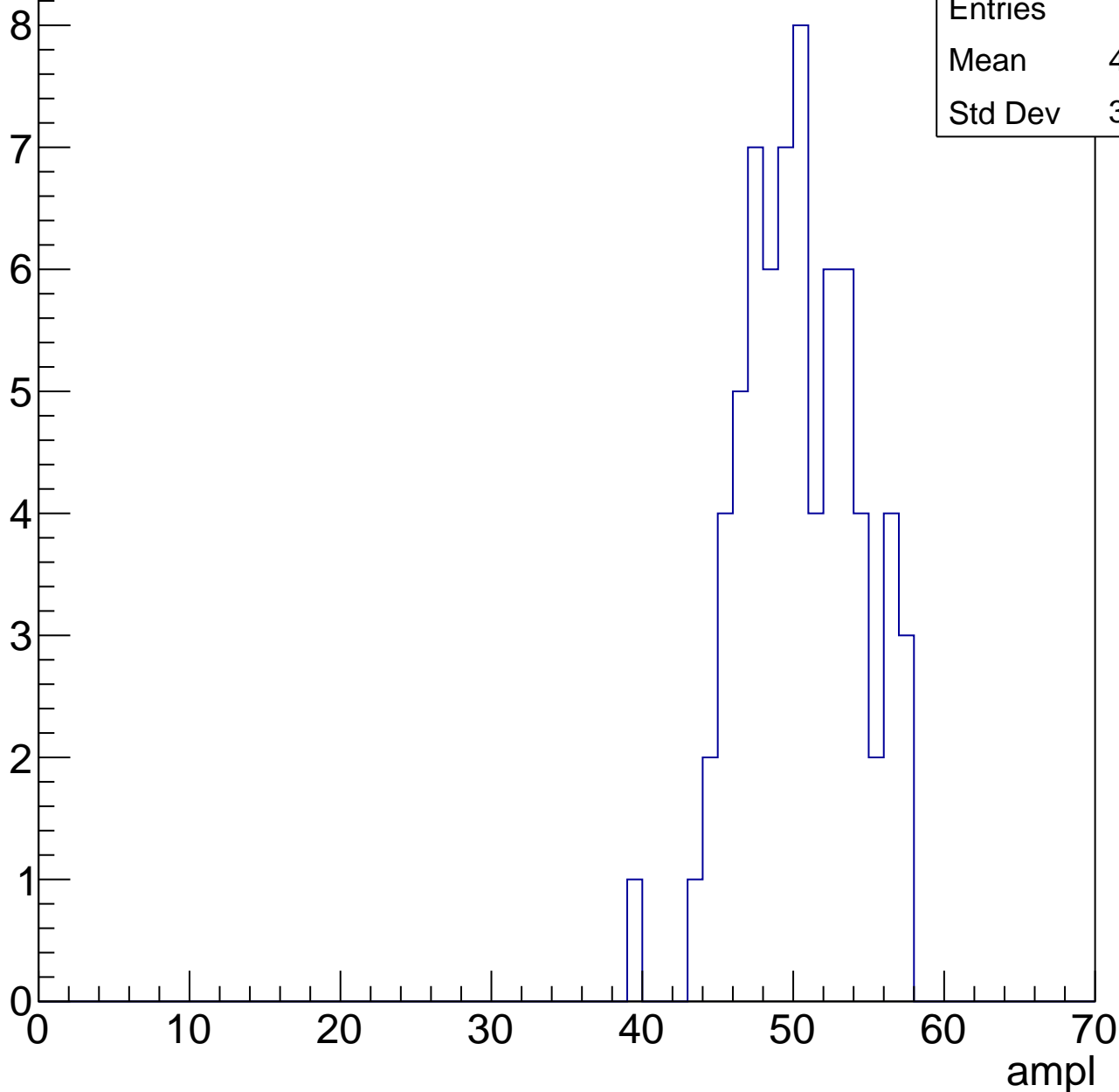


# B0L001S, U5-ch122, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	49.93
Std Dev	3.785

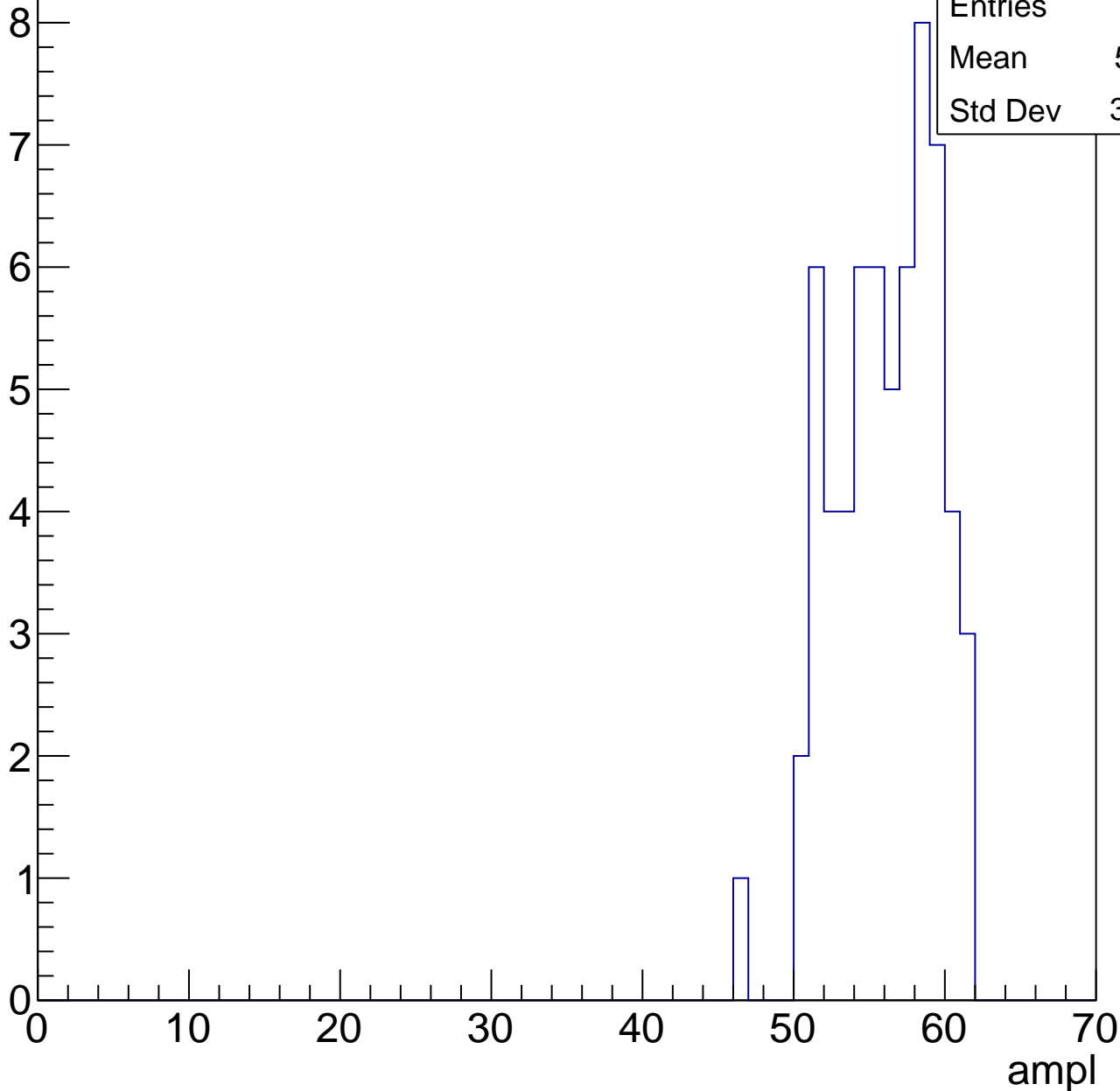


# B0L001S, U5-ch122, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	55.61
Std Dev	3.318

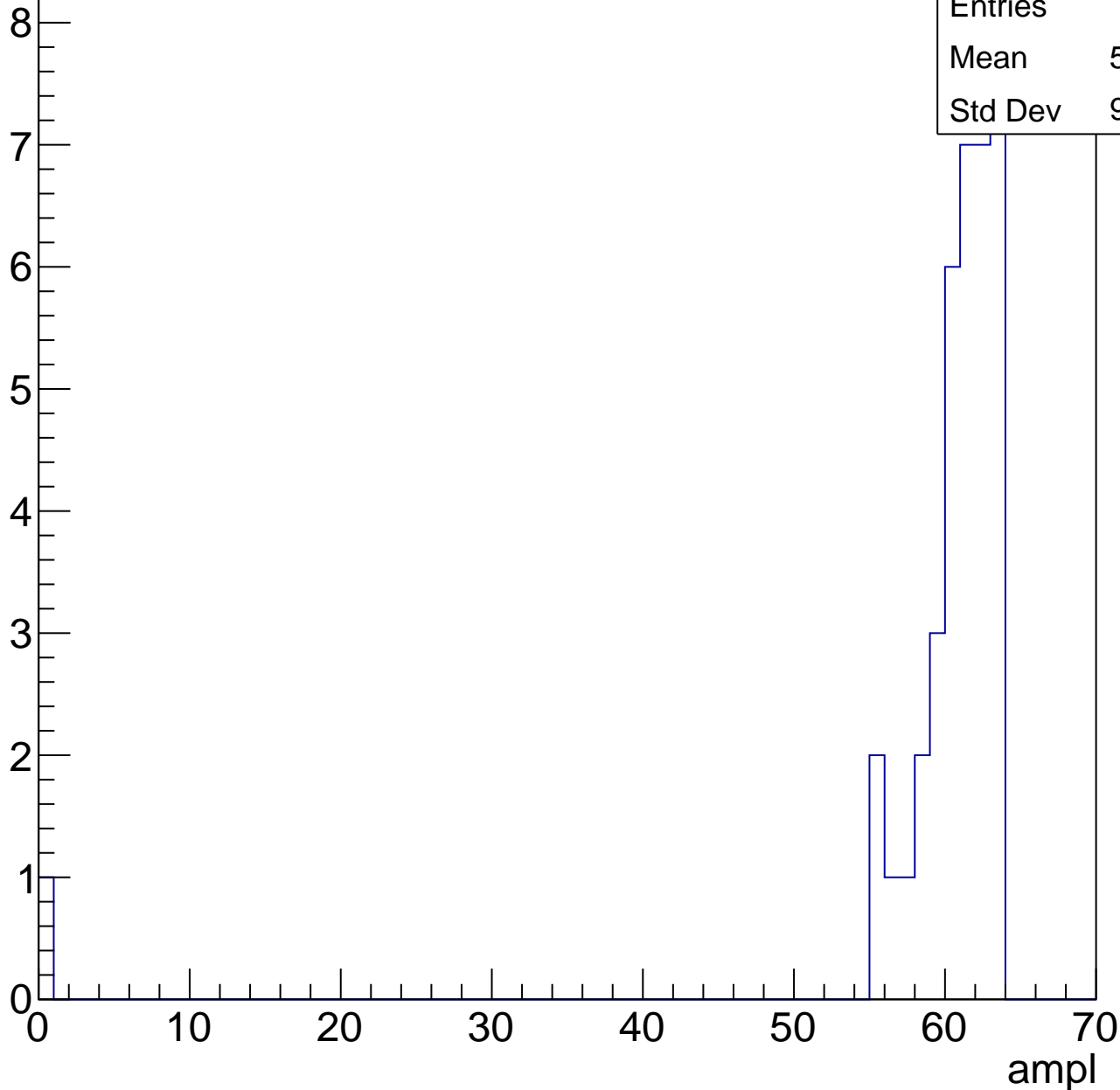


# B0L001S, U5-ch122, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	38
Mean	58.97
Std Dev	9.938



# B0L001S, U5-ch122, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch122, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U5-ch123, adc0

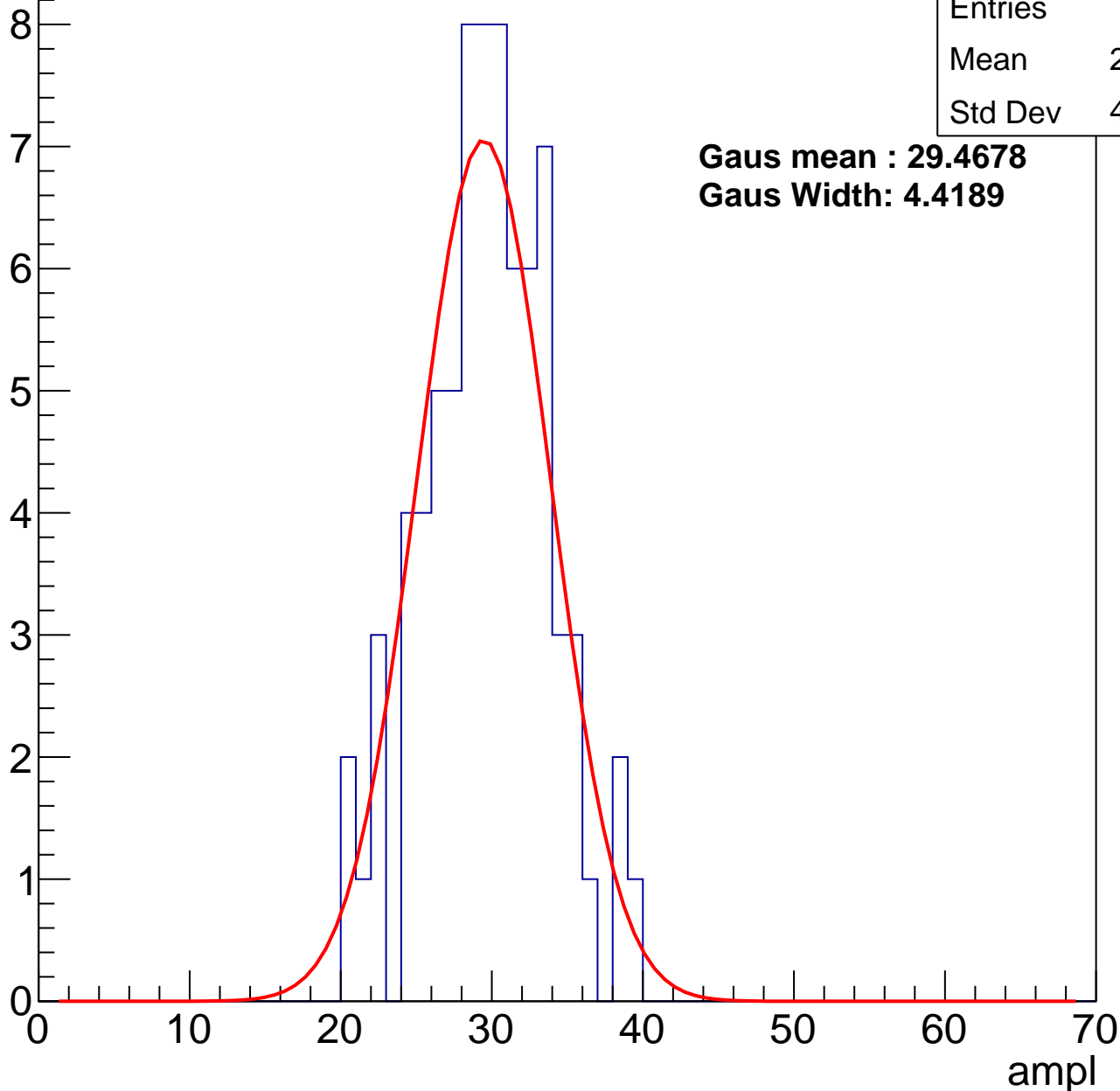
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	77
Mean	29.23
Std Dev	4.105

**Gaus mean : 29.4678**

**Gaus Width: 4.4189**



# B0L001S, U5-ch123, adc1

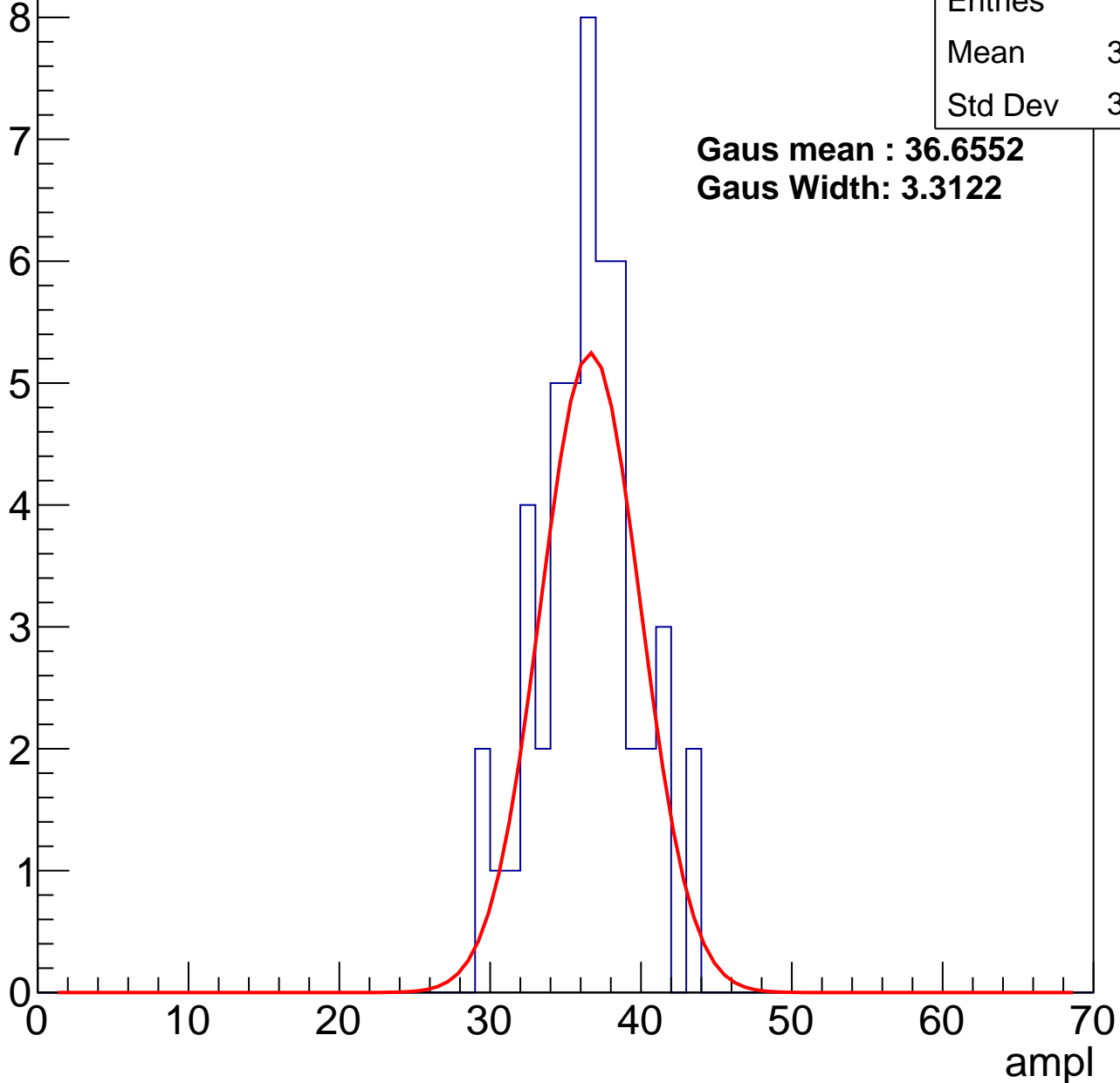
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	49
Mean	35.98
Std Dev	3.254

**Gaus mean : 36.6552**

**Gaus Width: 3.3122**



# B0L001S, U5-ch123, adc2

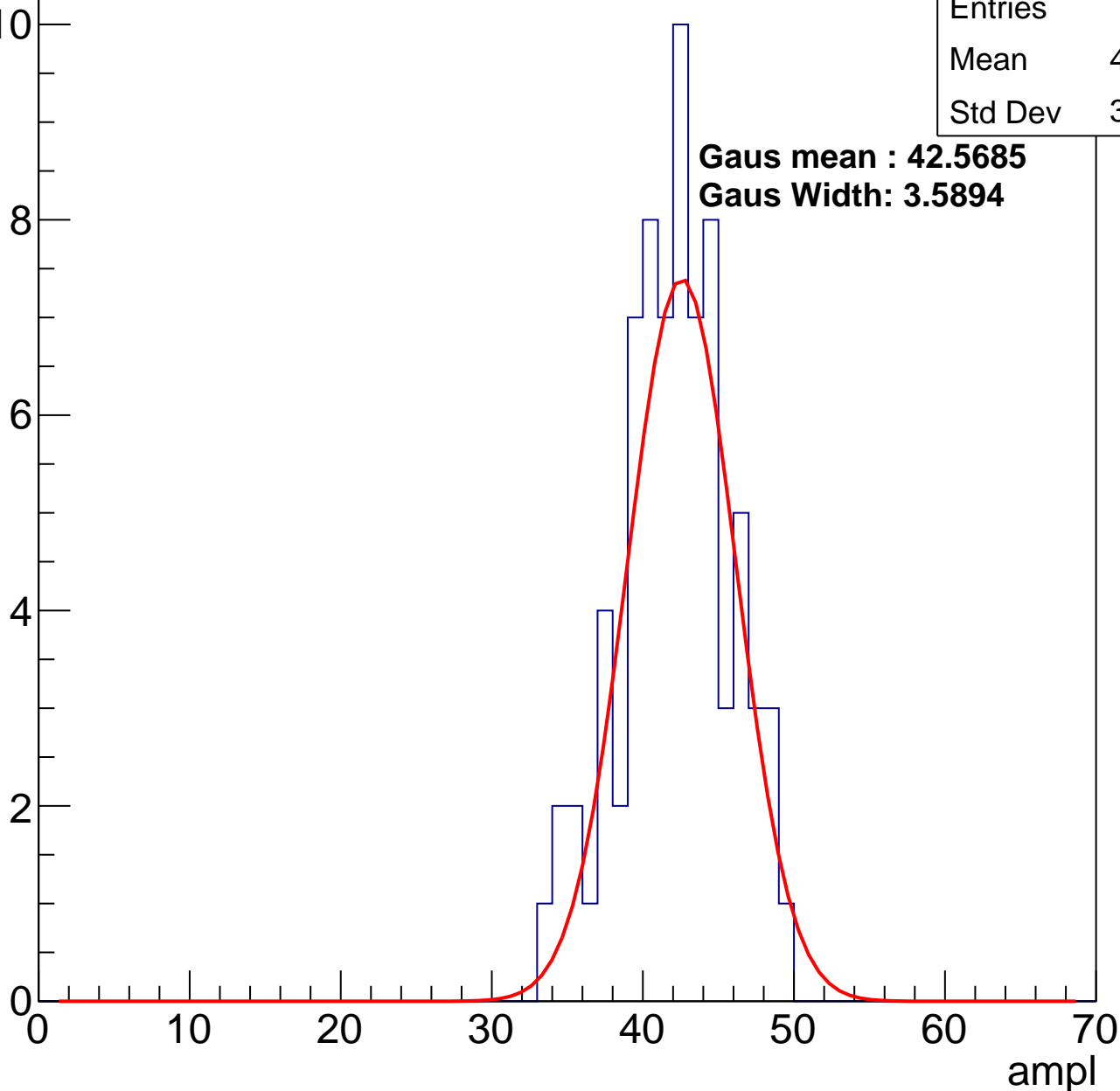
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	41.66
Std Dev	3.576

**Gaus mean : 42.5685**

**Gaus Width: 3.5894**

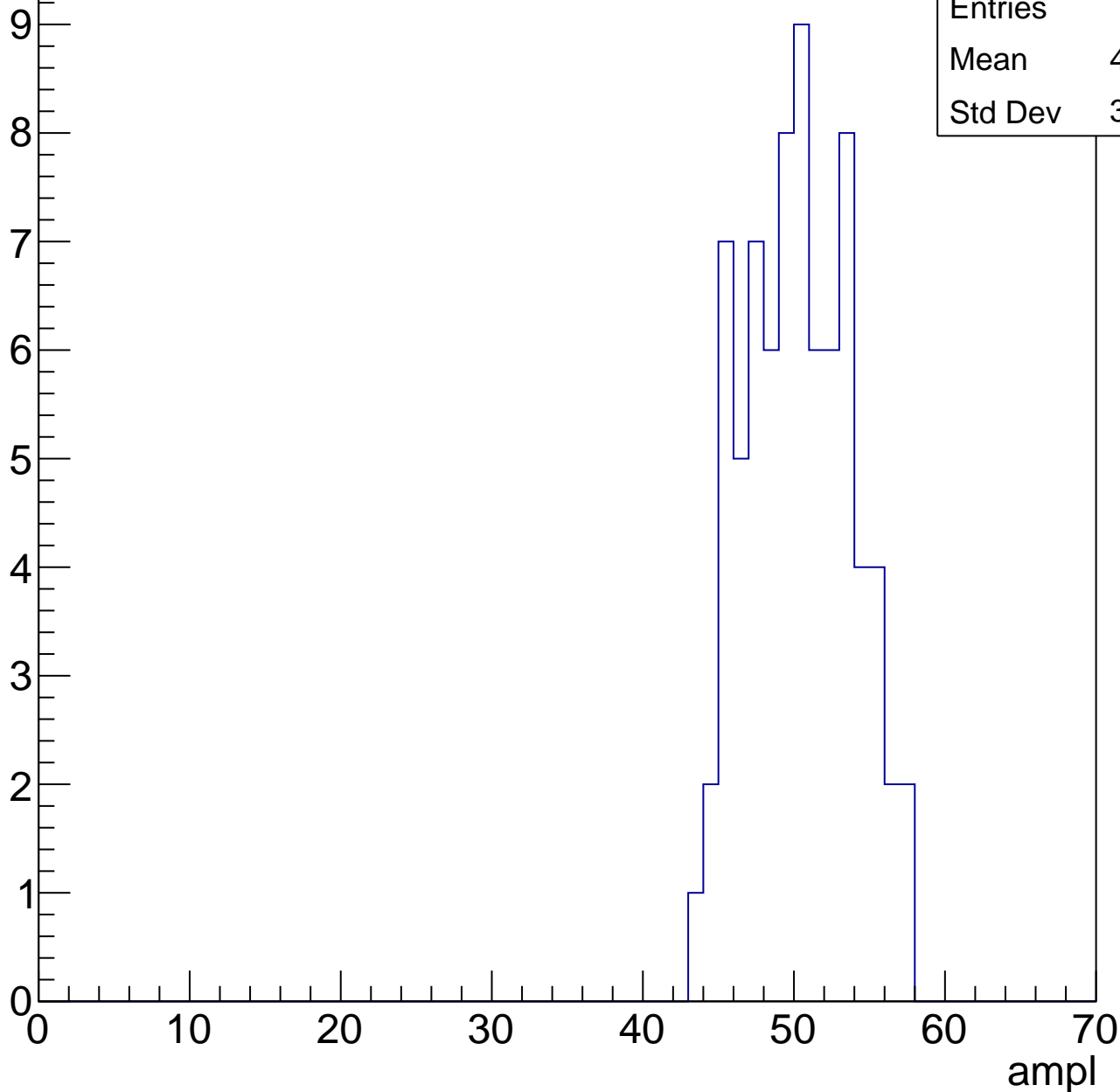


# B0L001S, U5-ch123, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

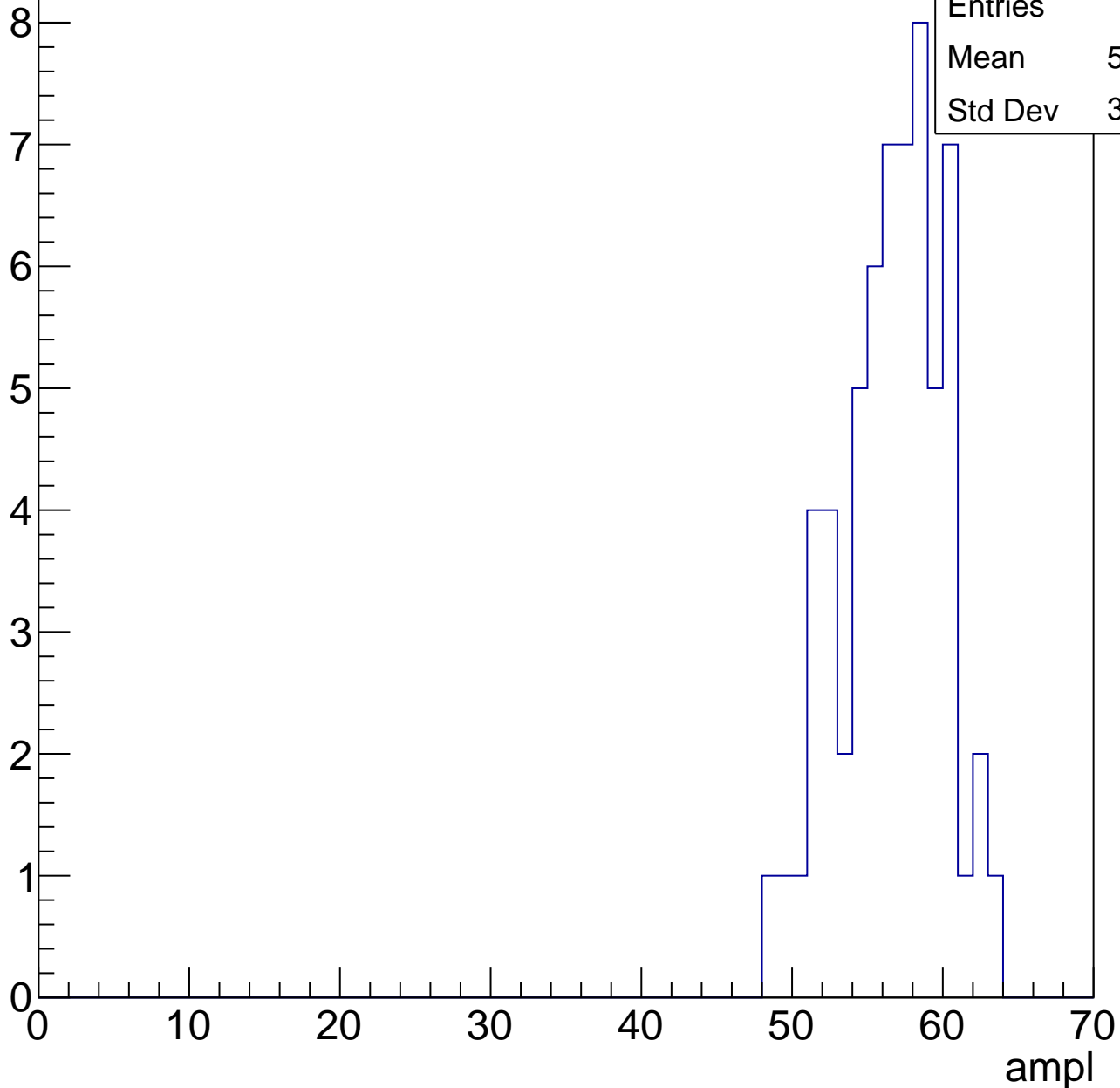
Entries	77
Mean	49.86
Std Dev	3.429



# B0L001S, U5-ch123, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

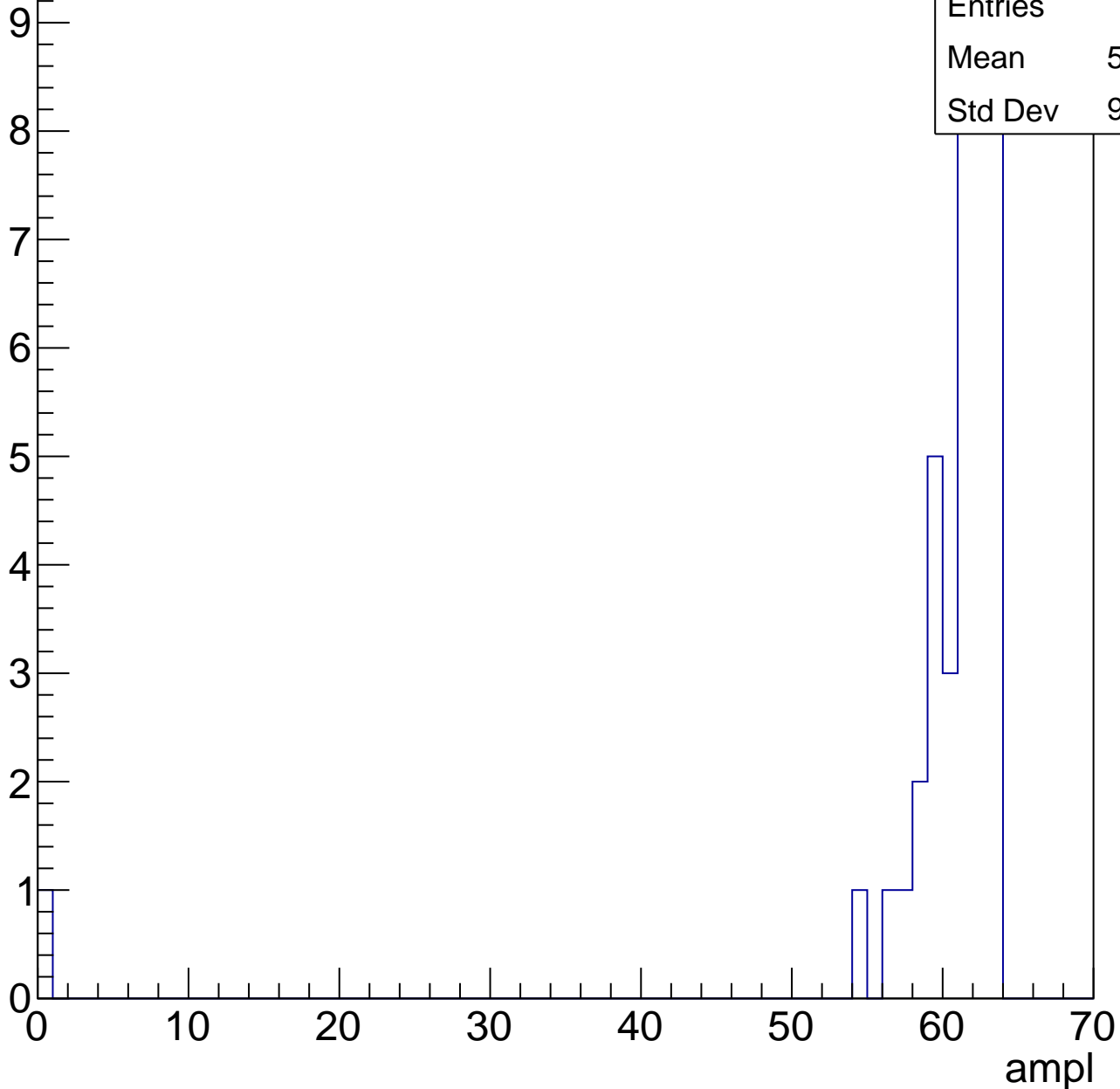


# B0L001S, U5-ch123, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	39
Mean	59.15
Std Dev	9.818



# B0L001S, U5-ch123, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch123, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U5-ch124, adc0

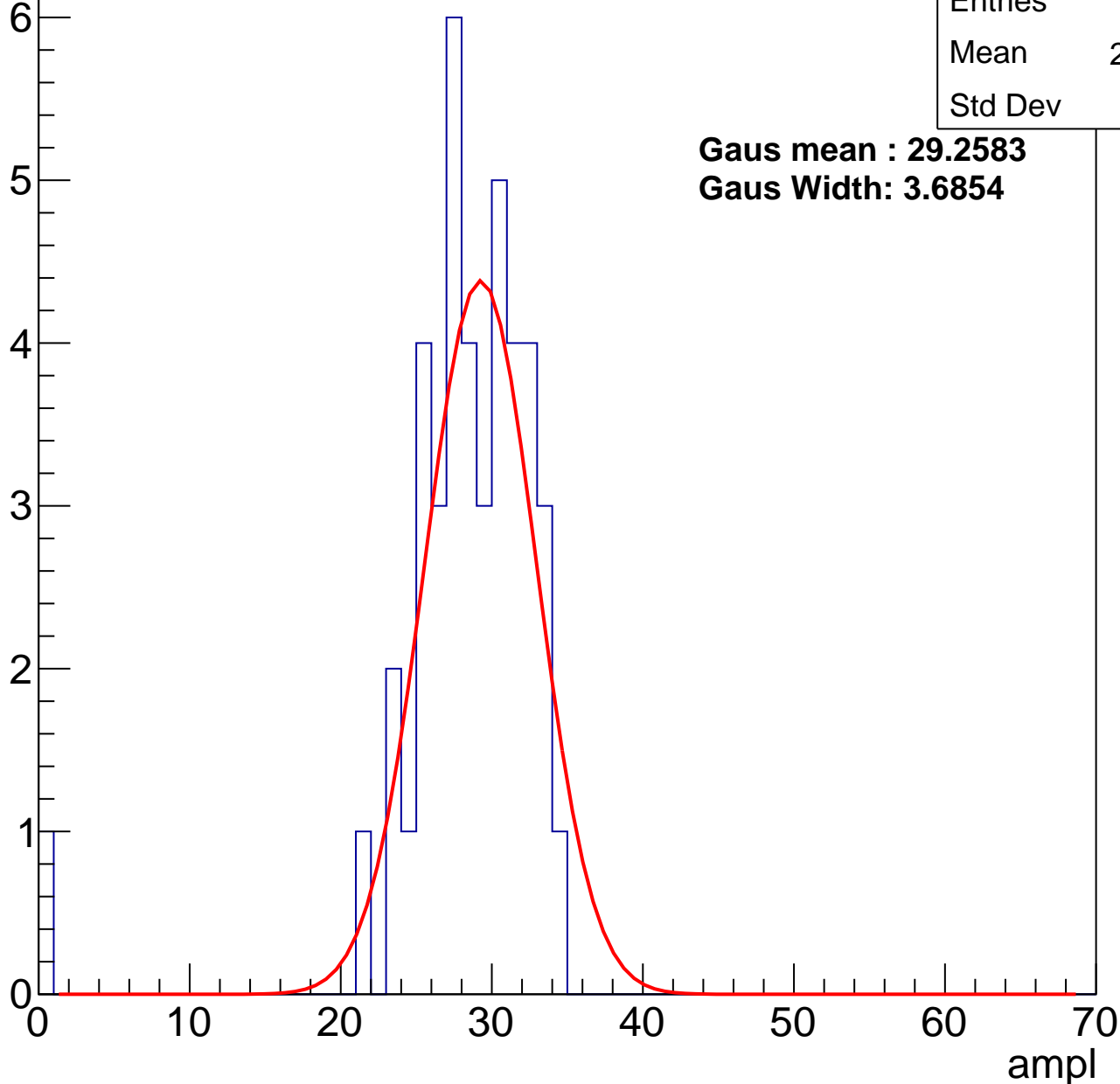
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	42
Mean	27.74
Std Dev	5.31

**Gaus mean : 29.2583**

**Gaus Width: 3.6854**



# B0L001S, U5-ch124, adc1

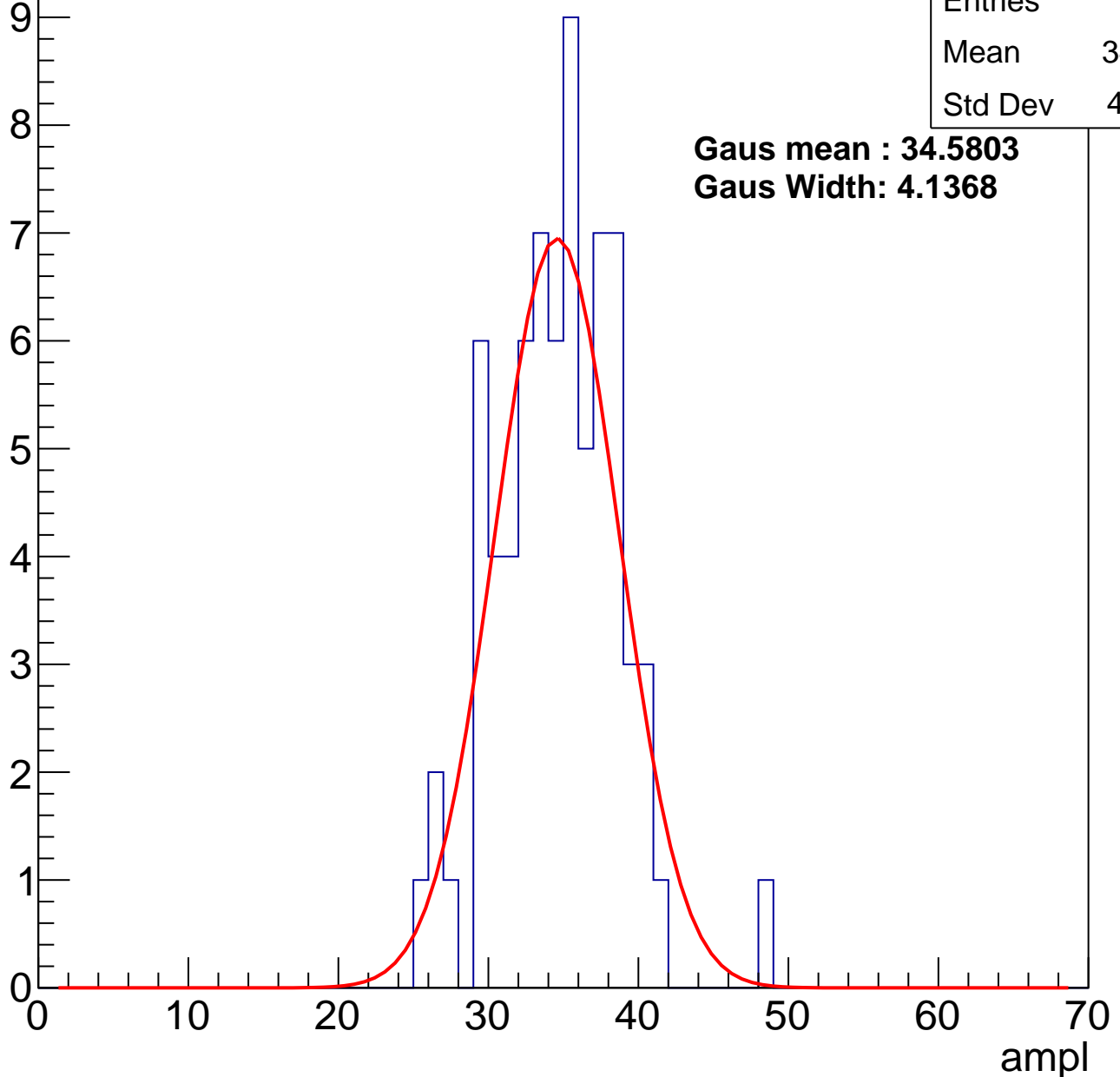
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	34.18
Std Dev	4.001

**Gaus mean : 34.5803**

**Gaus Width: 4.1368**



# B0L001S, U5-ch124, adc2

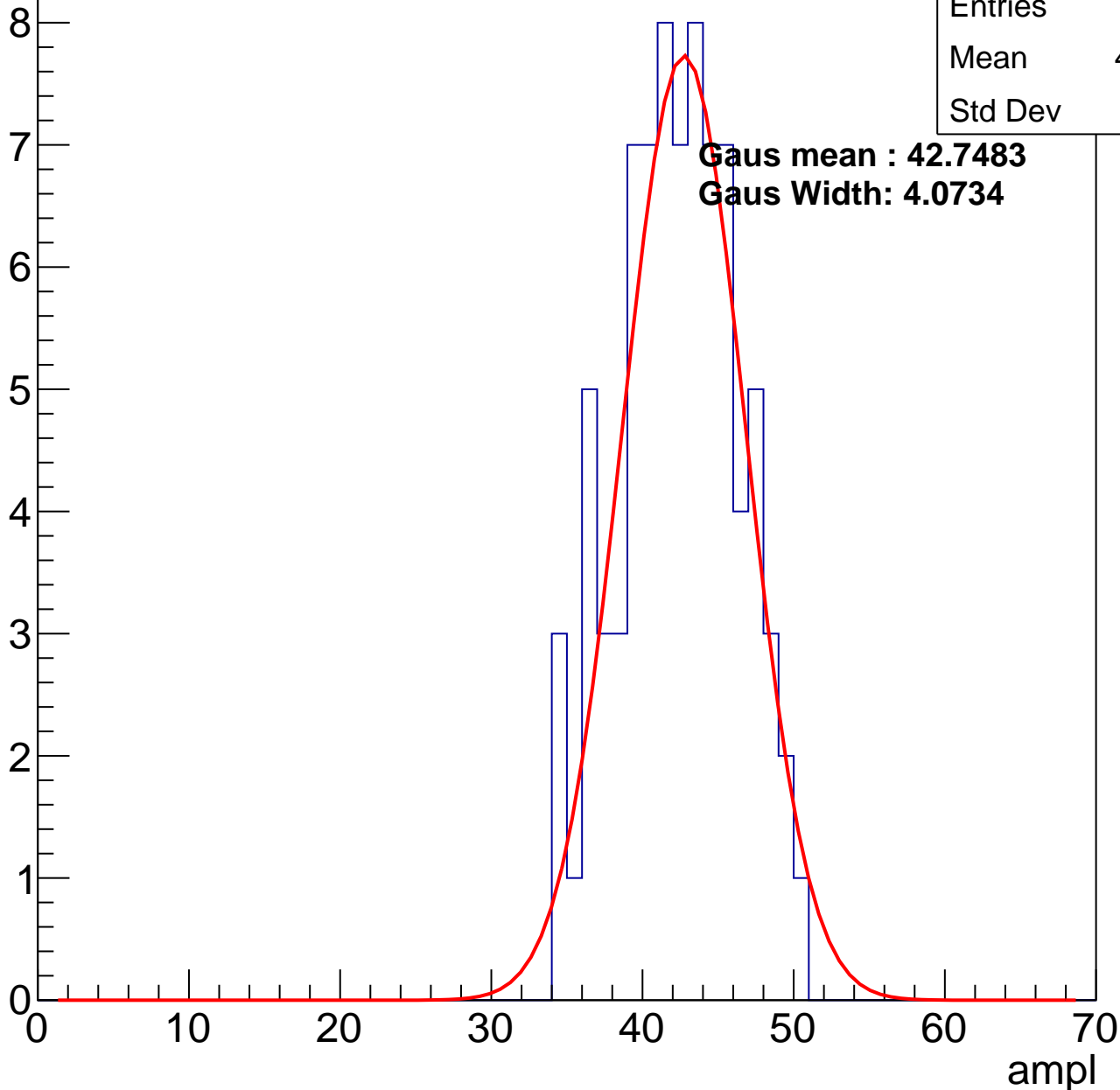
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	81
Mean	41.91
Std Dev	3.85

**Gaus mean : 42.7483**

**Gaus Width: 4.0734**

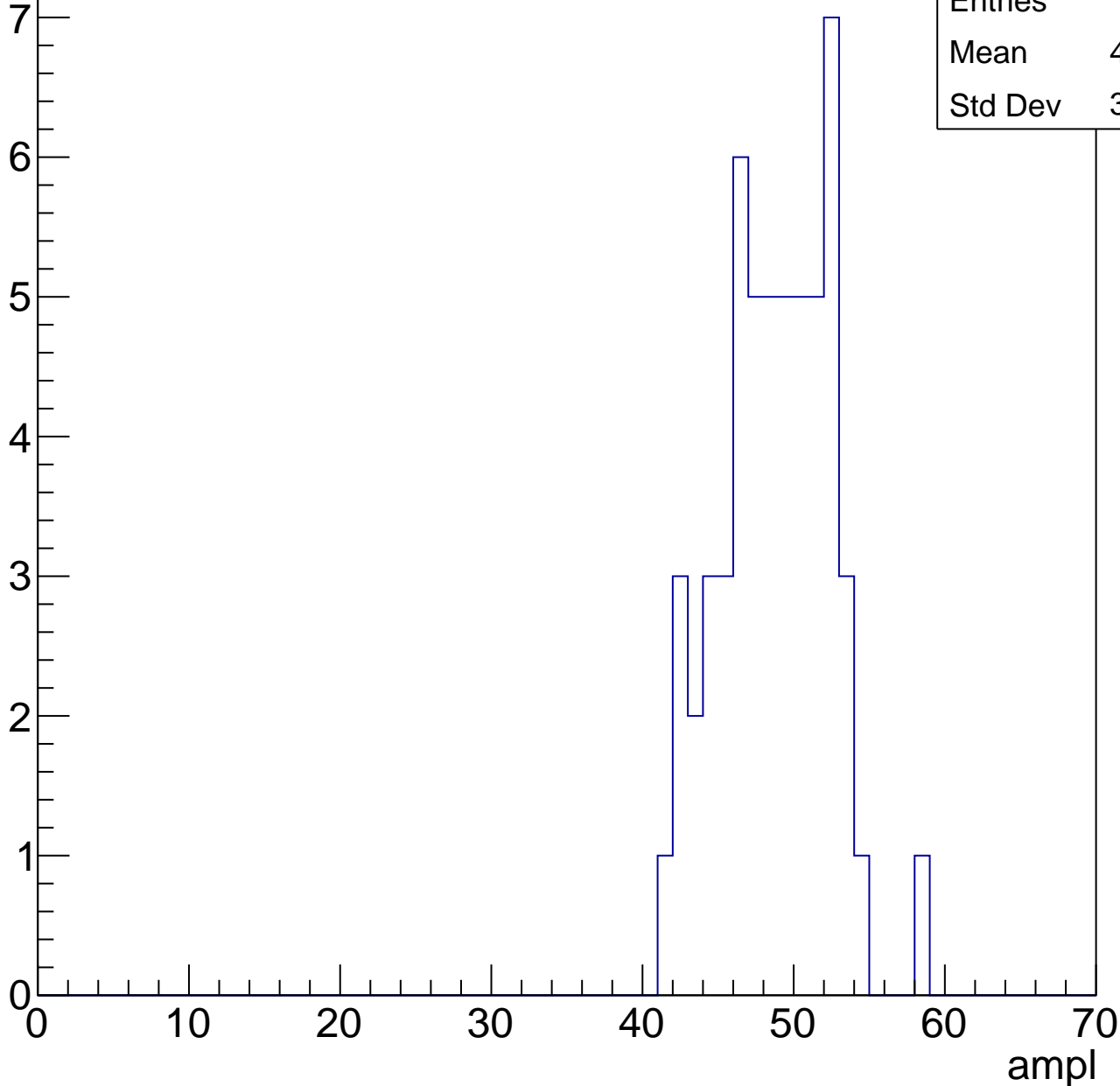


# B0L001S, U5-ch124, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	48.29
Std Dev	3.566

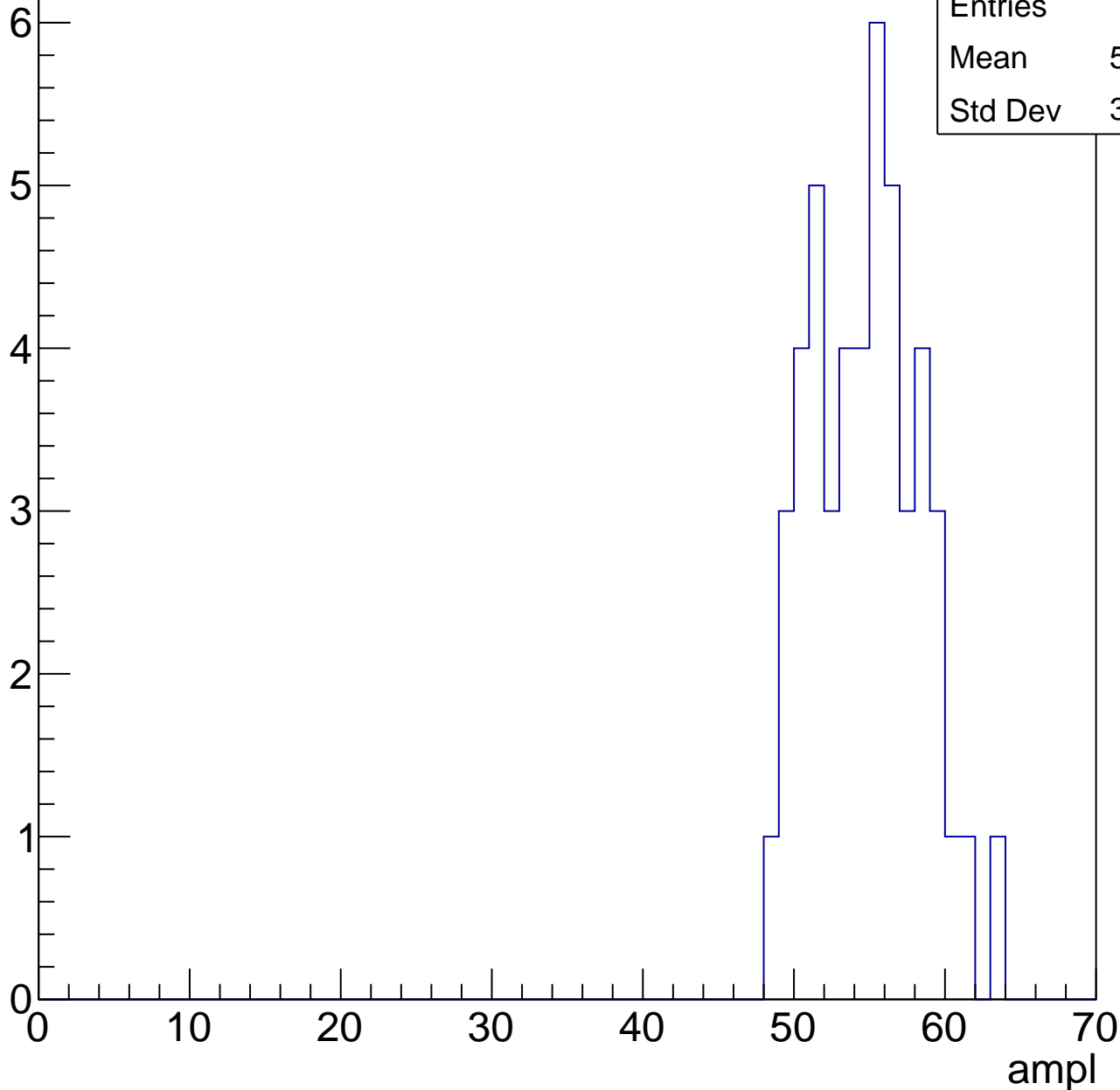


# B0L001S, U5-ch124, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	48
Mean	54.33
Std Dev	3.502



# B0L001S, U5-ch124, adc5

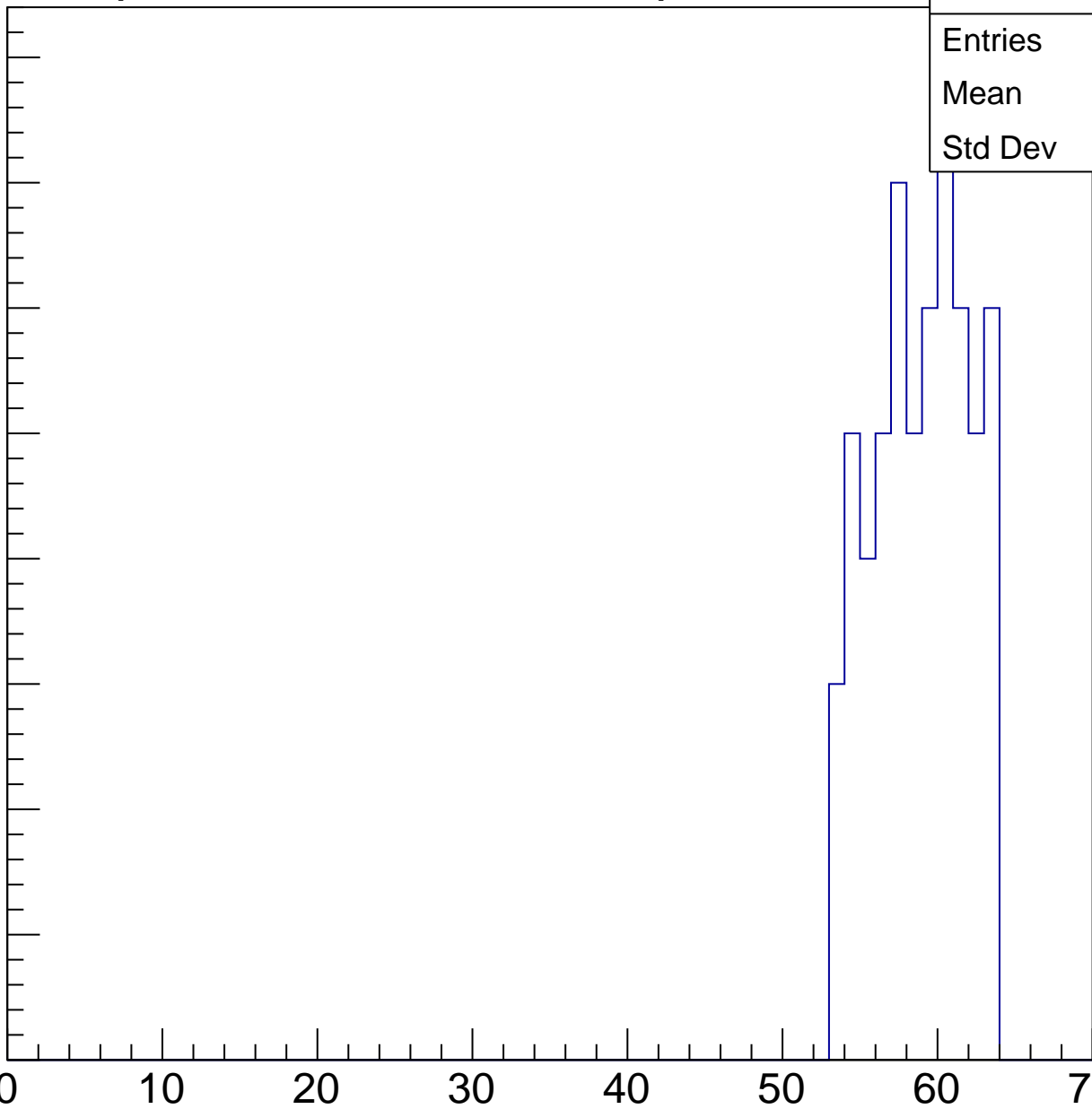
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	60
Mean	58.43
Std Dev	2.969

ampl

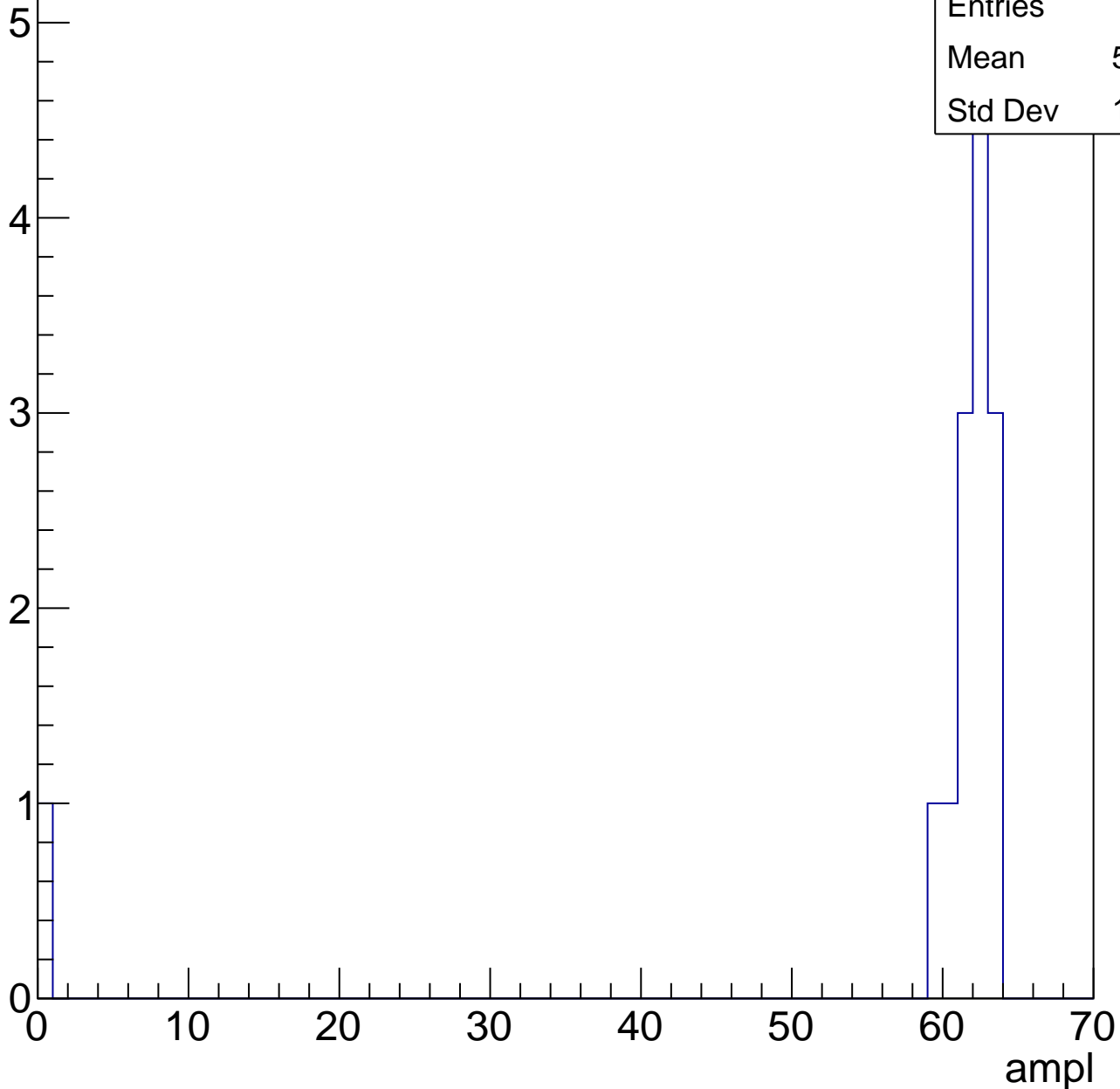


# B0L001S, U5-ch124, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	14
Mean	57.21
Std Dev	15.91





# B0L001S, U5-ch124, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch125, adc0

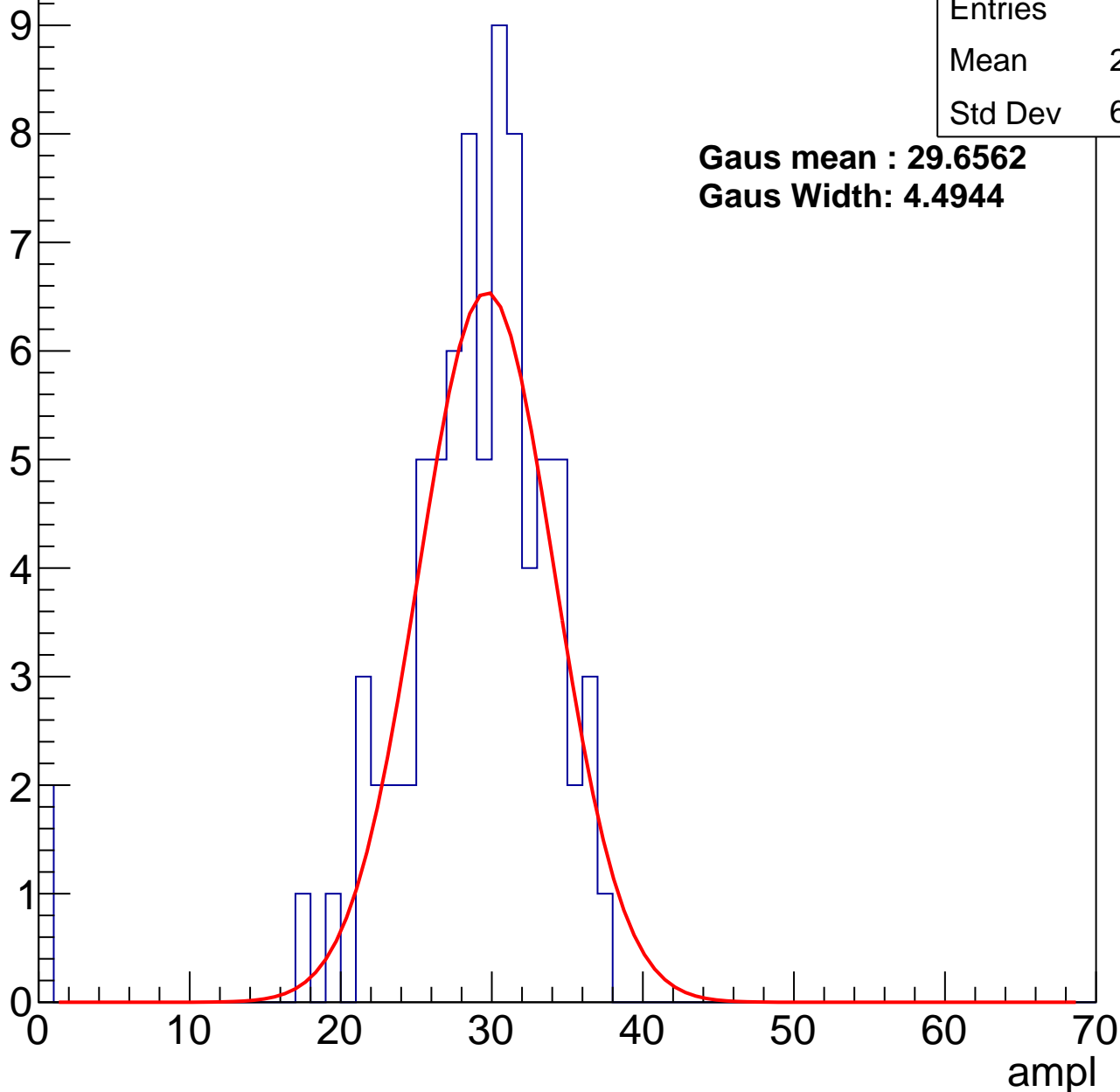
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	79
Mean	28.09
Std Dev	6.157

**Gaus mean : 29.6562**

**Gaus Width: 4.4944**



# B0L001S, U5-ch125, adc1

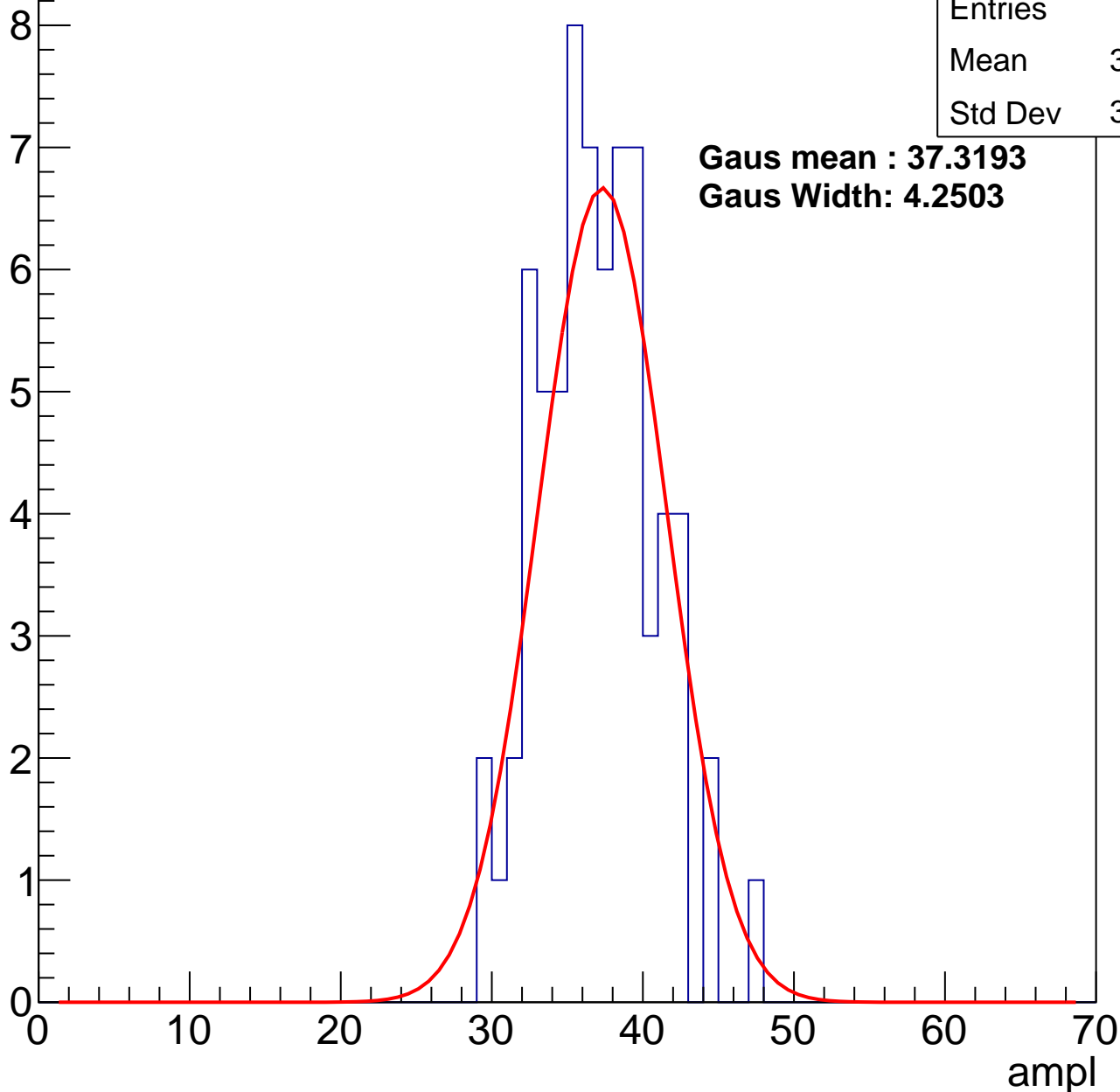
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	36.53
Std Dev	3.725

**Gaus mean : 37.3193**

**Gaus Width: 4.2503**



# B0L001S, U5-ch125, adc2

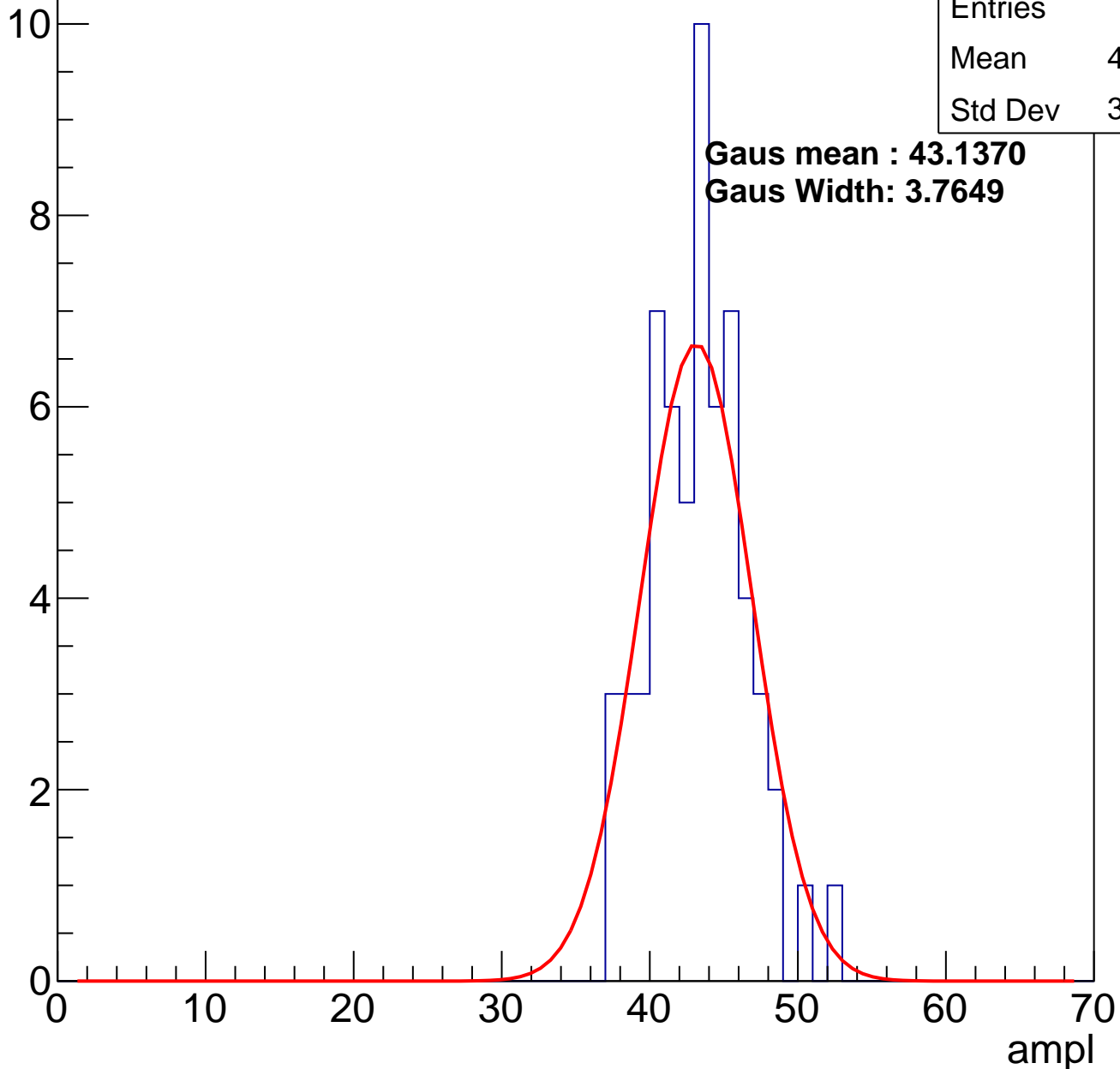
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	61
Mean	42.79
Std Dev	3.184

**Gaus mean : 43.1370**

**Gaus Width: 3.7649**

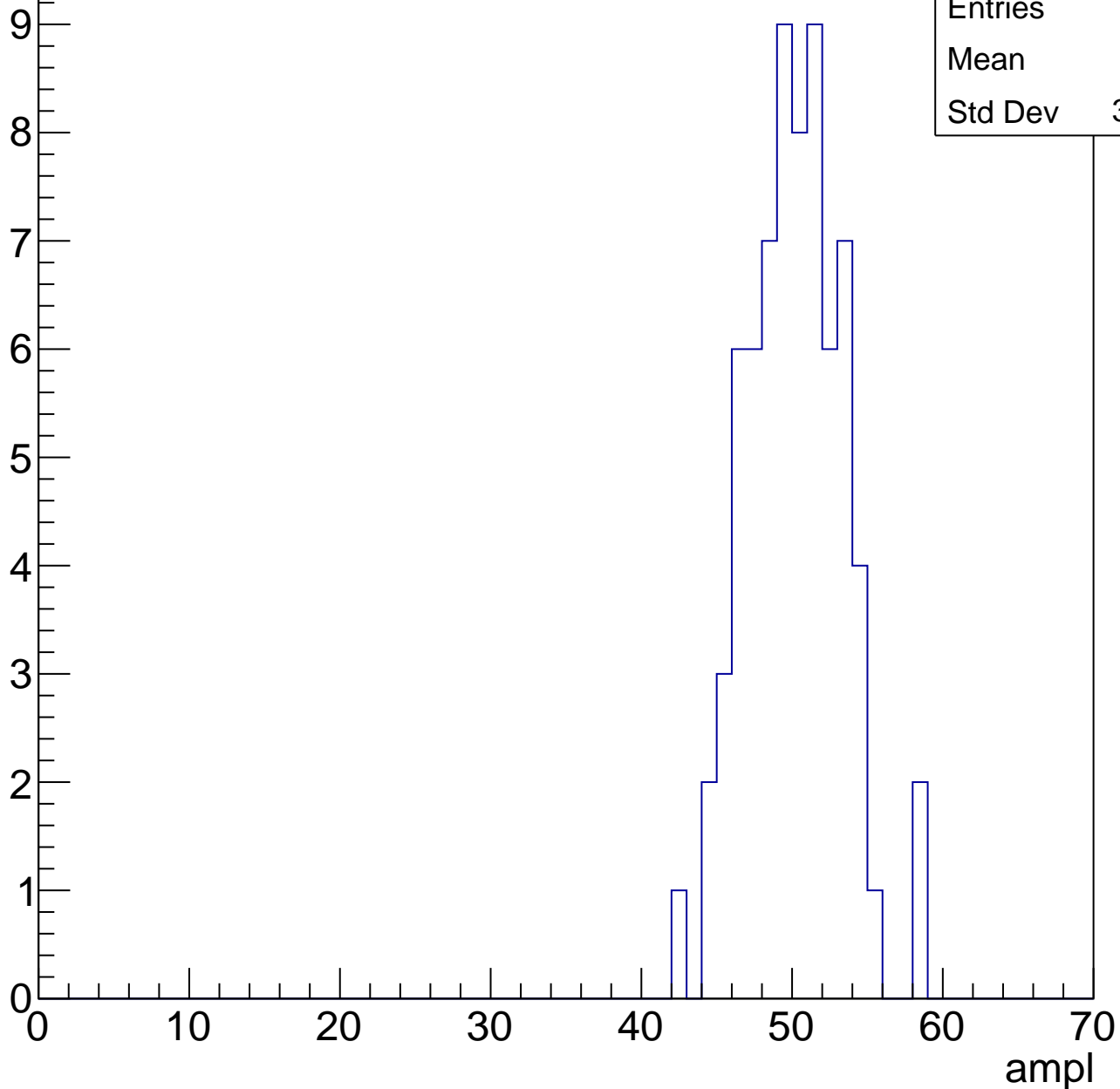
Entry



# B0L001S, U5-ch125, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



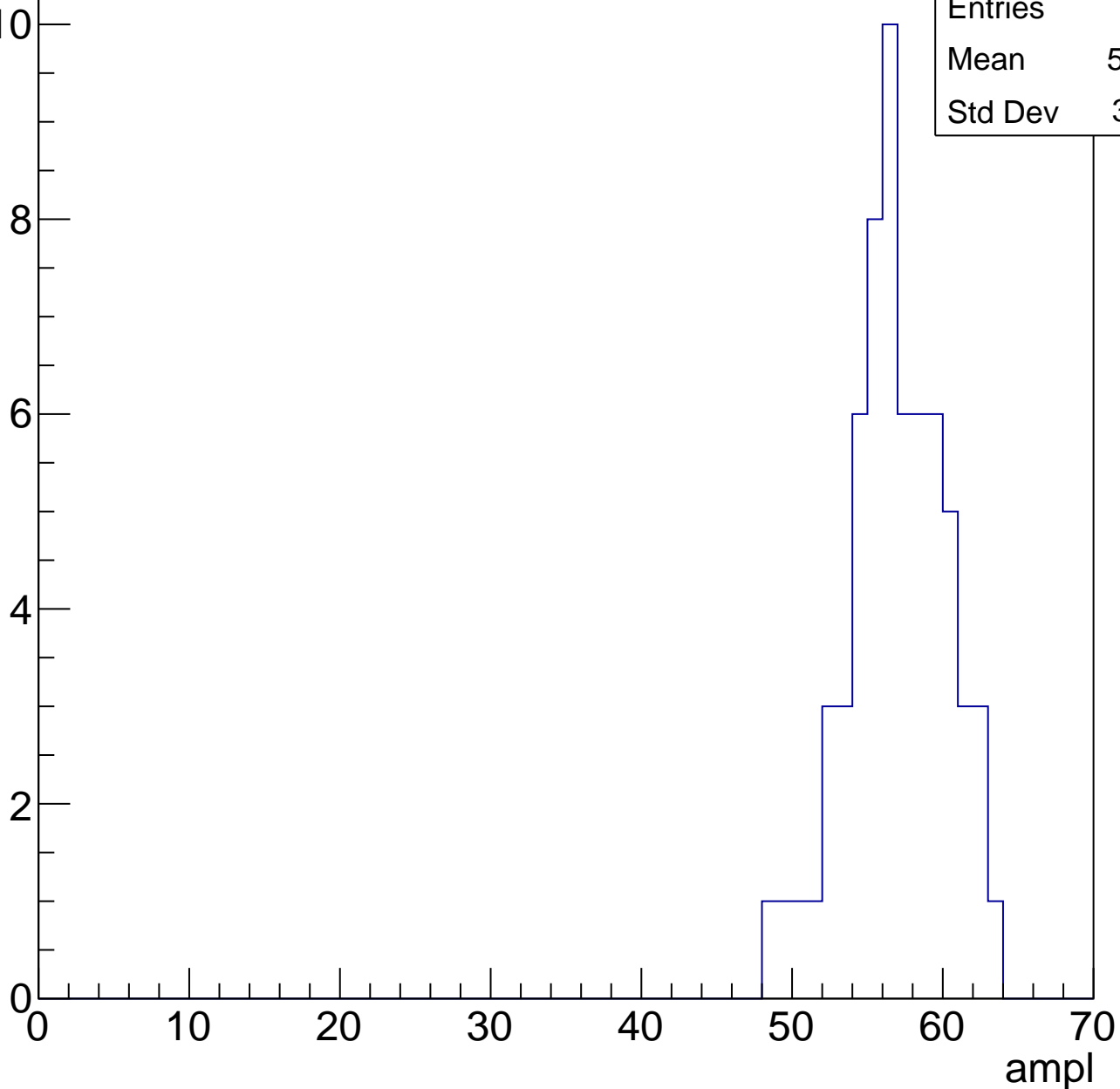
Entries	71
Mean	49.7
Std Dev	3.151

# B0L001S, U5-ch125, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	56.45
Std Dev	3.221

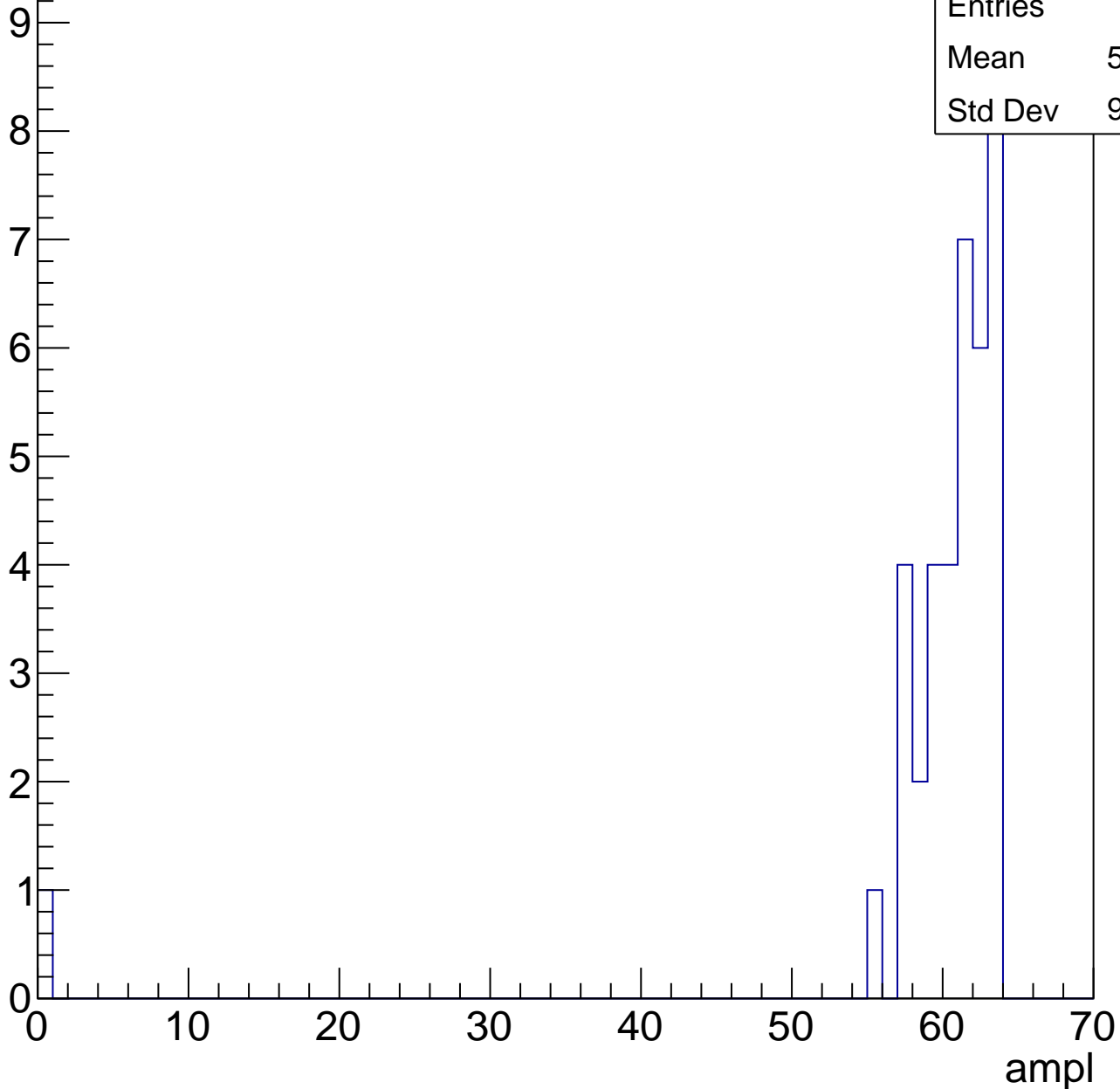


# B0L001S, U5-ch125, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	38
Mean	58.97
Std Dev	9.927



# B0L001S, U5-ch125, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch125, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U5-ch126, adc0

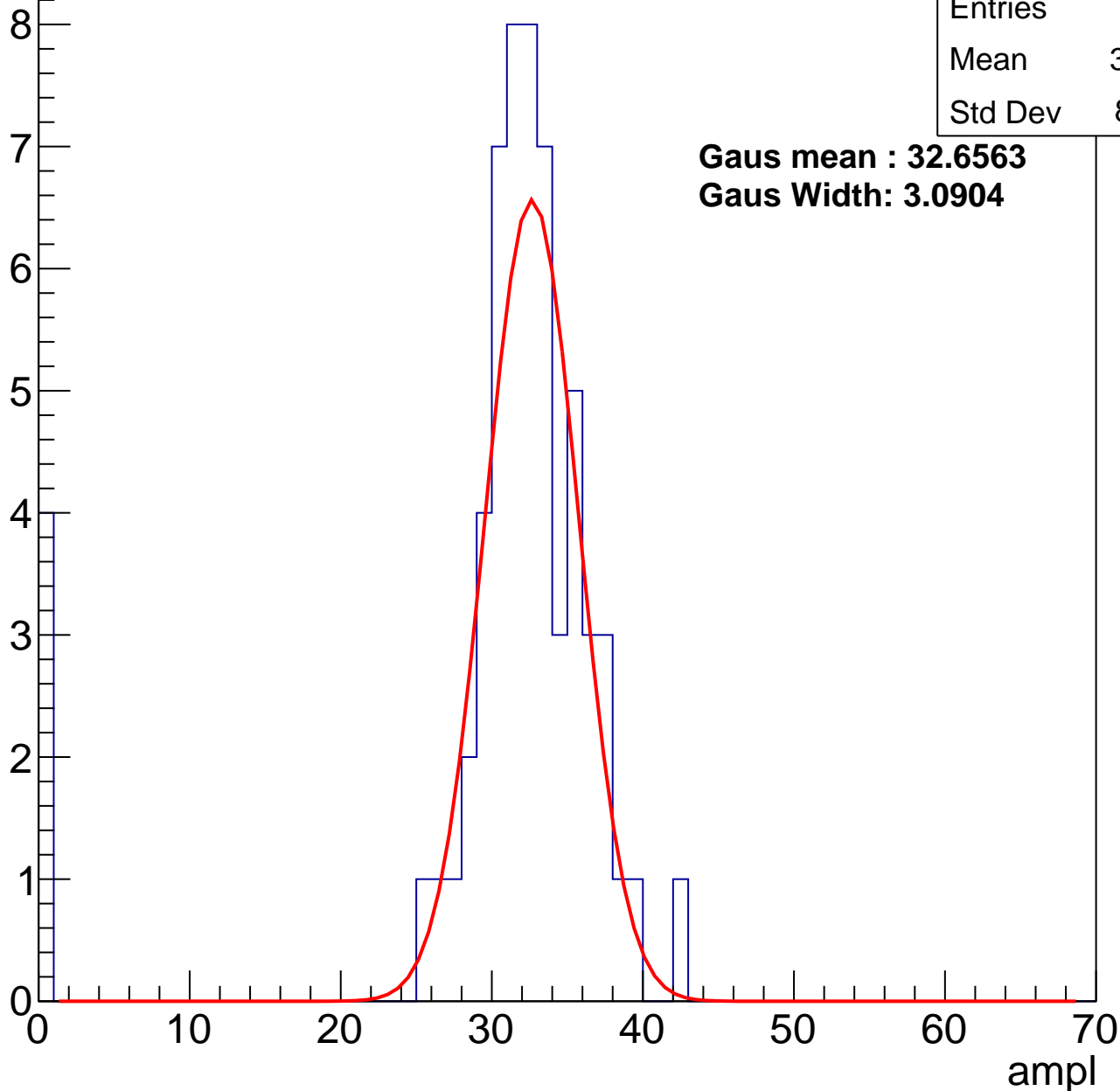
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	30.17
Std Dev	8.641

**Gaus mean : 32.6563**

**Gaus Width: 3.0904**



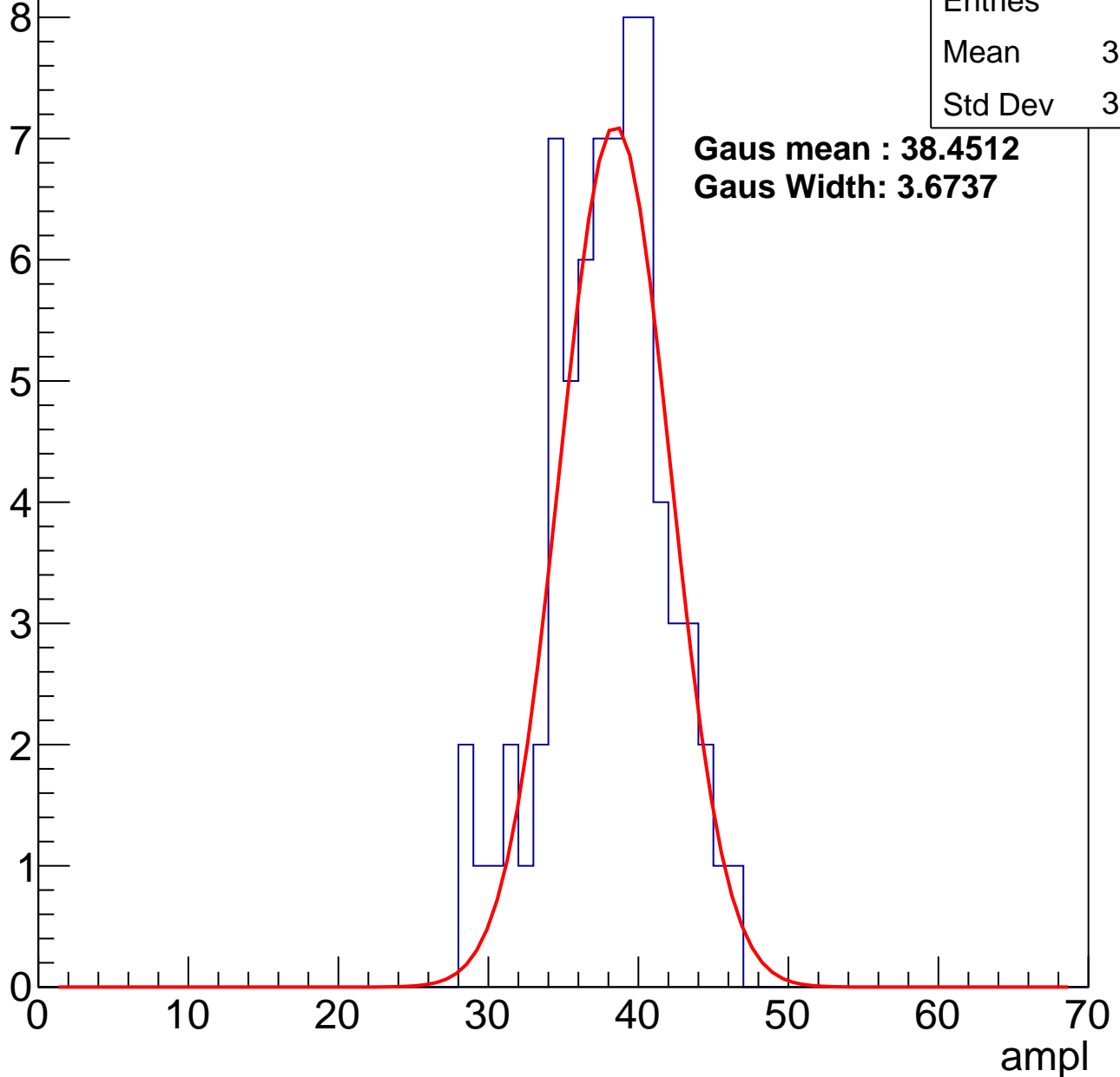
# B0L001S, U5-ch126, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	37.45
Std Dev	3.899

**Gaus mean : 38.4512**  
**Gaus Width: 3.6737**



# B0L001S, U5-ch126, adc2

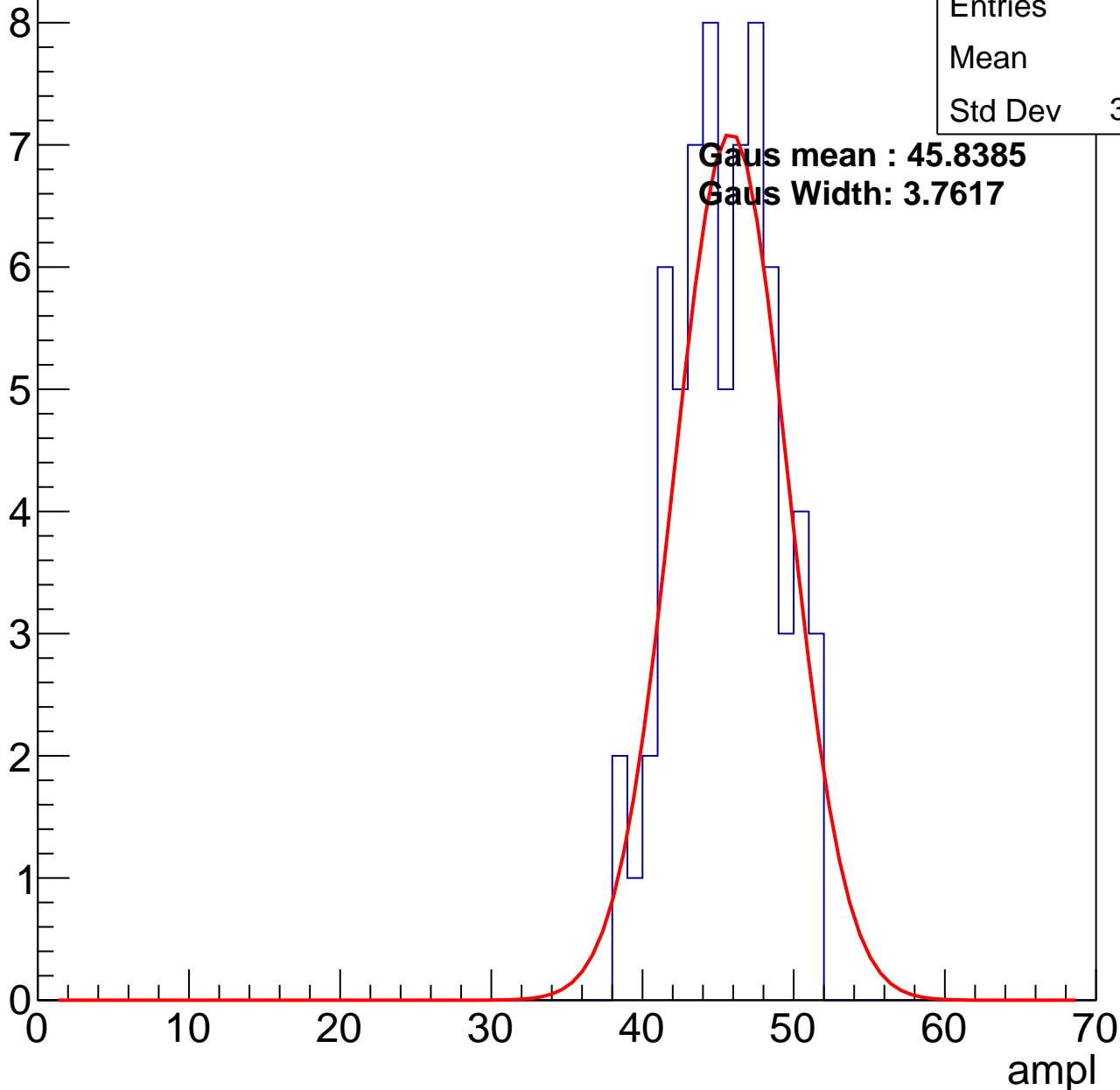
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	45
Std Dev	3.255

**Gaus mean : 45.8385**

**Gaus Width: 3.7617**

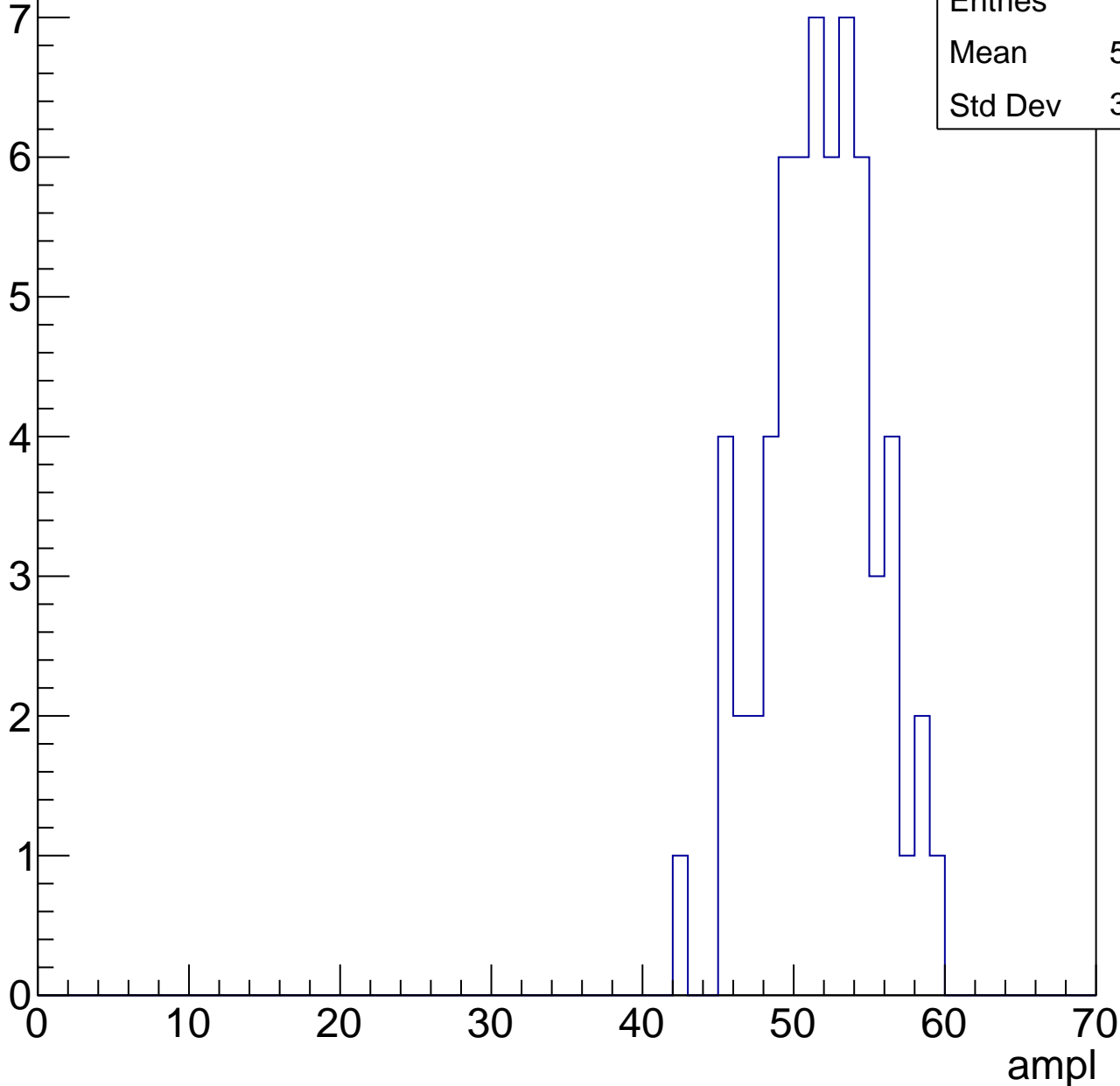


# B0L001S, U5-ch126, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

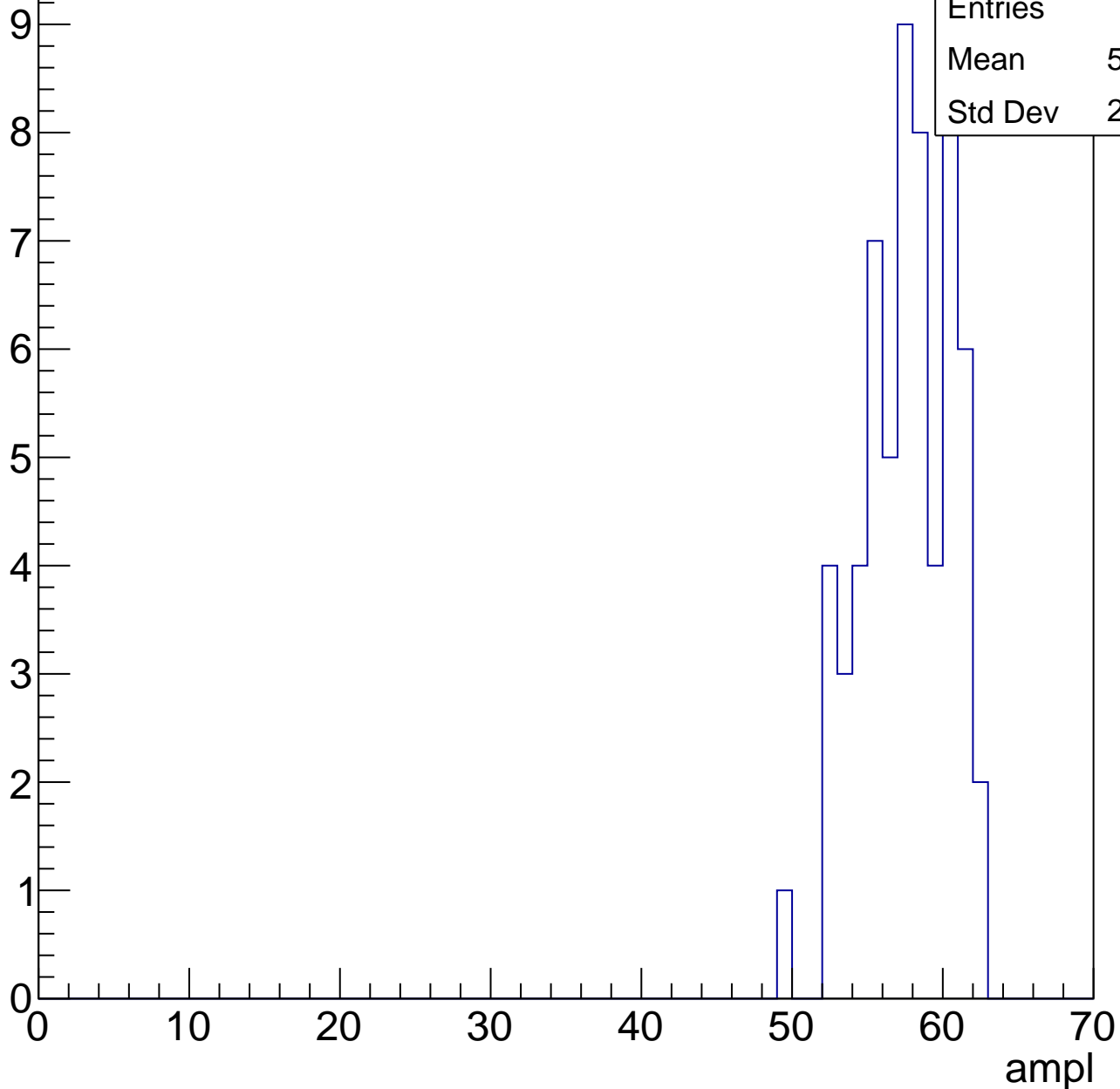
Entries	62
Mean	51.27
Std Dev	3.597



# B0L001S, U5-ch126, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



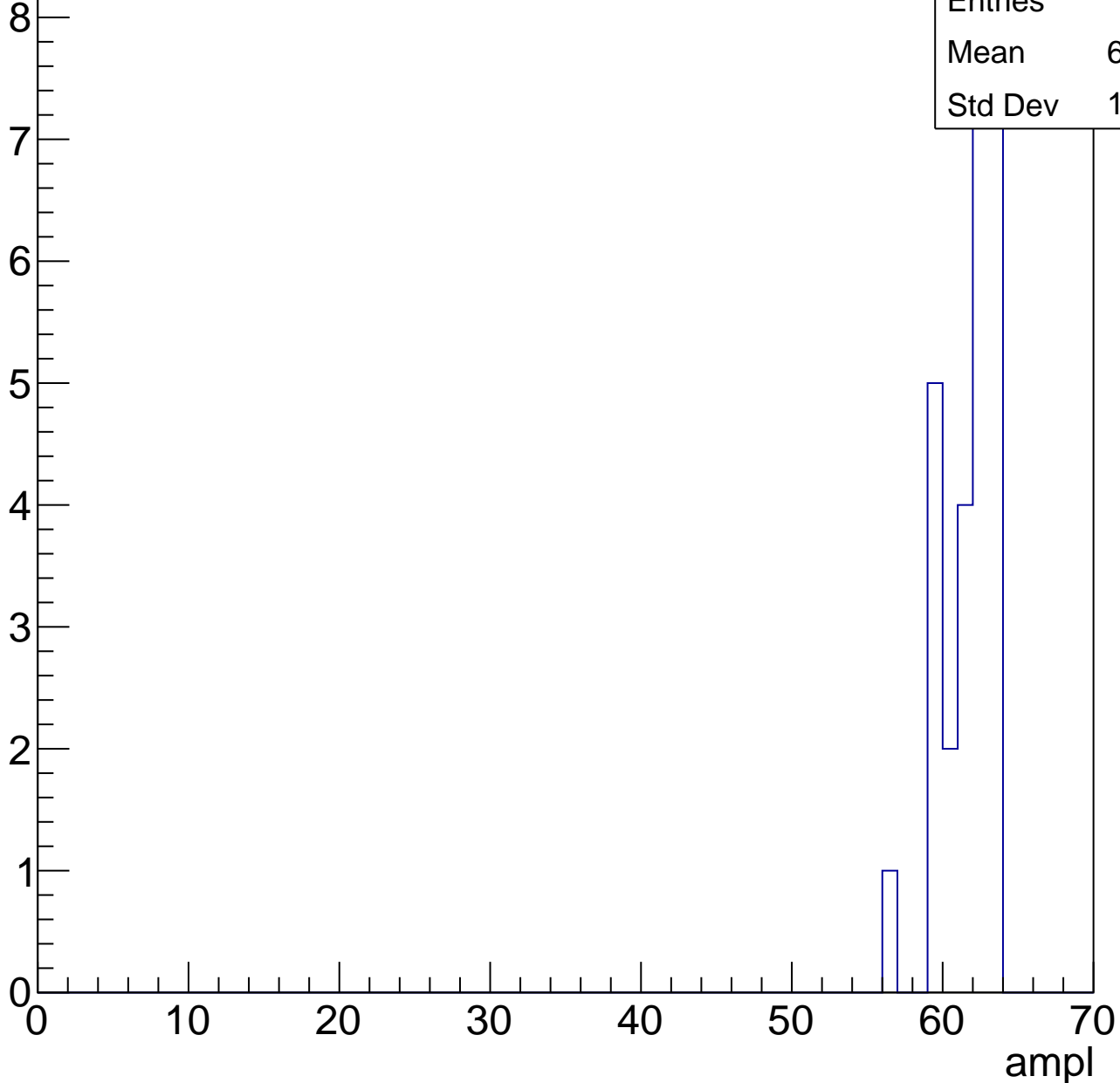
Entries	61
Mean	57.05
Std Dev	2.928

# B0L001S, U5-ch126, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	28
Mean	61.25
Std Dev	1.745



# B0L001S, U5-ch126, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch126, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U5-ch127, adc0

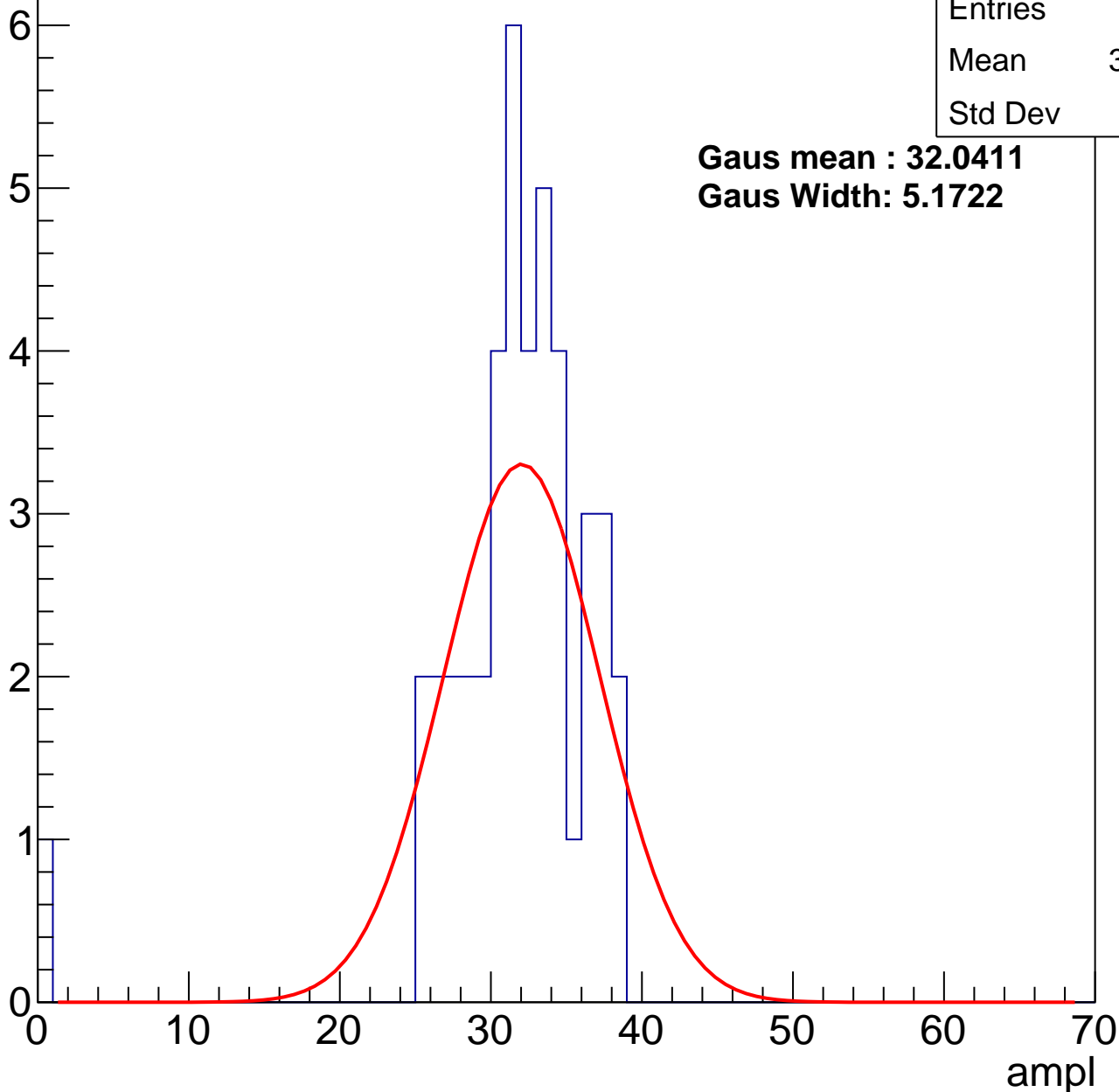
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	43
Mean	31.05
Std Dev	5.91

**Gaus mean : 32.0411**

**Gaus Width: 5.1722**



# B0L001S, U5-ch127, adc1

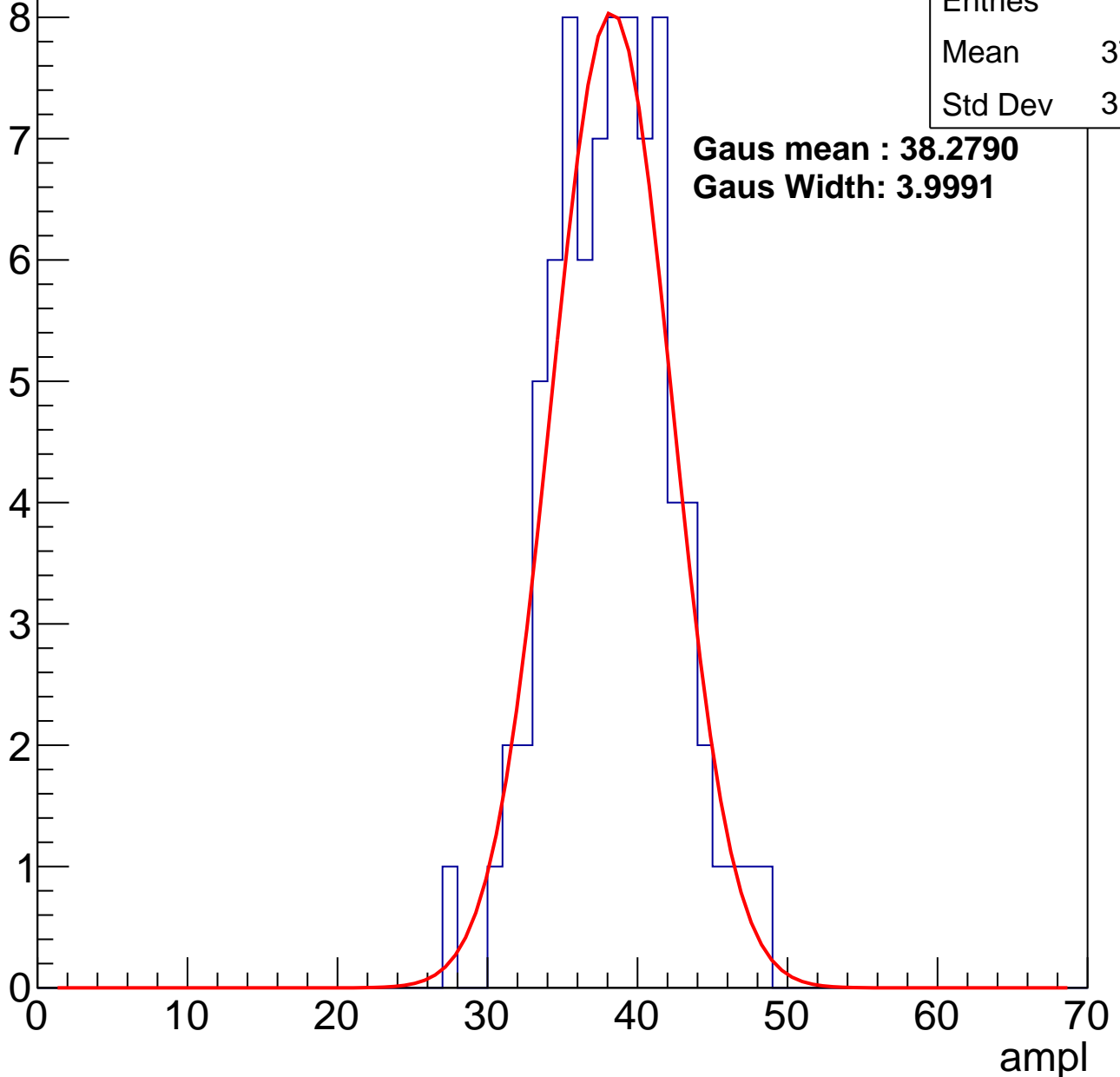
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	83
Mean	37.89
Std Dev	3.982

**Gaus mean : 38.2790**

**Gaus Width: 3.9991**



# B0L001S, U5-ch127, adc2

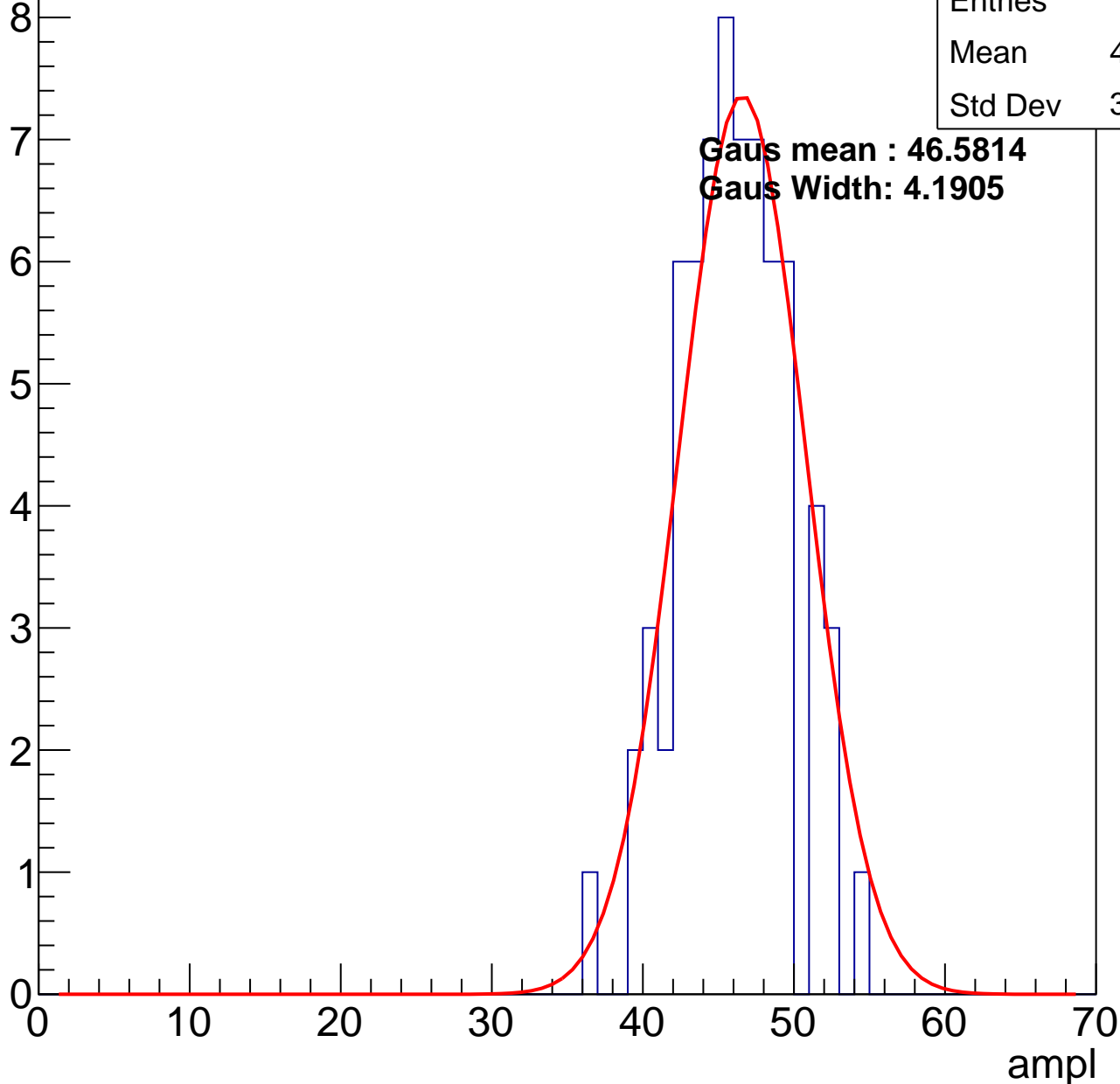
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	45.52
Std Dev	3.578

**Gaus mean : 46.5814**

**Gaus Width: 4.1905**

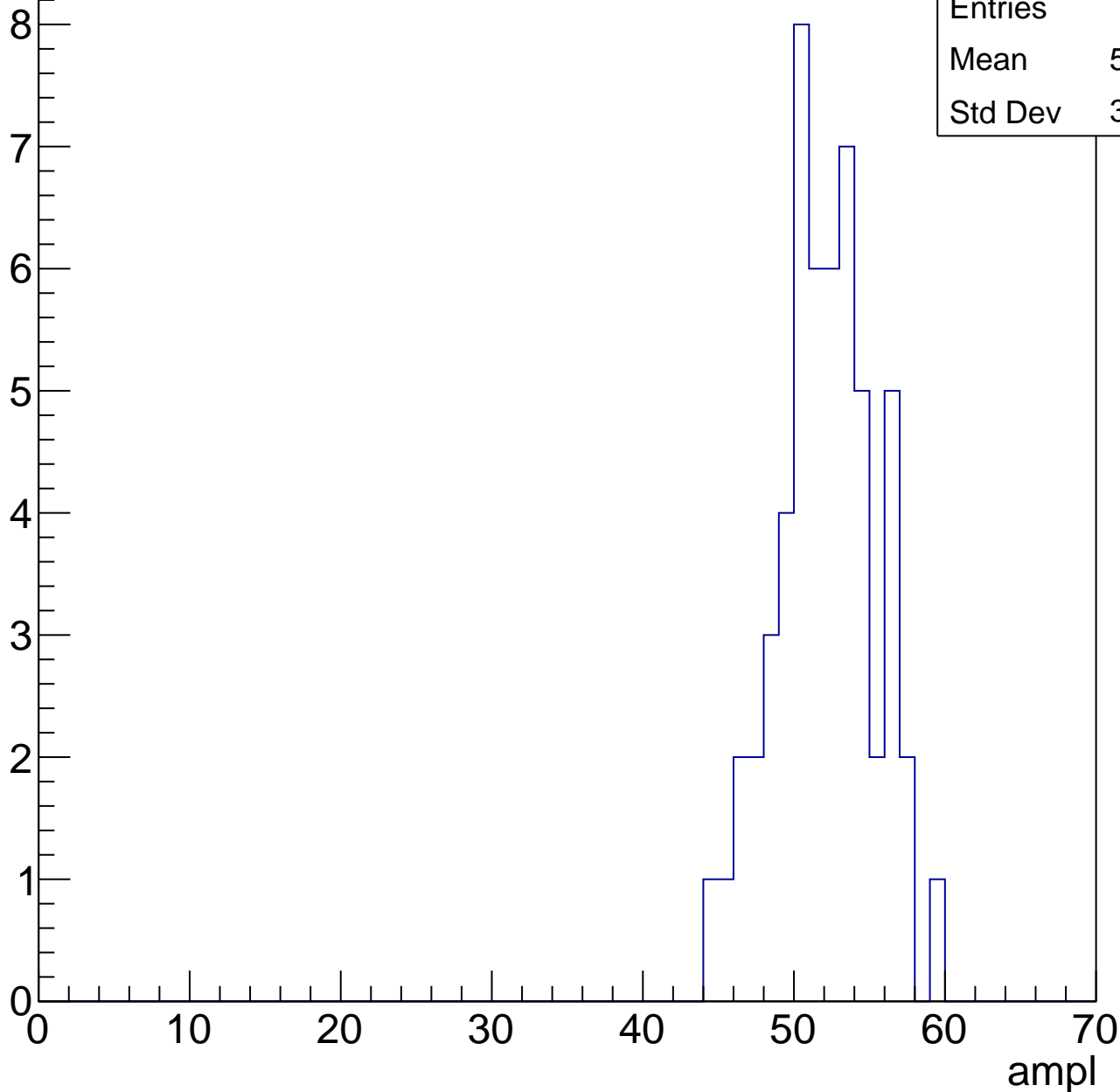


# B0L001S, U5-ch127, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	51.58
Std Dev	3.223

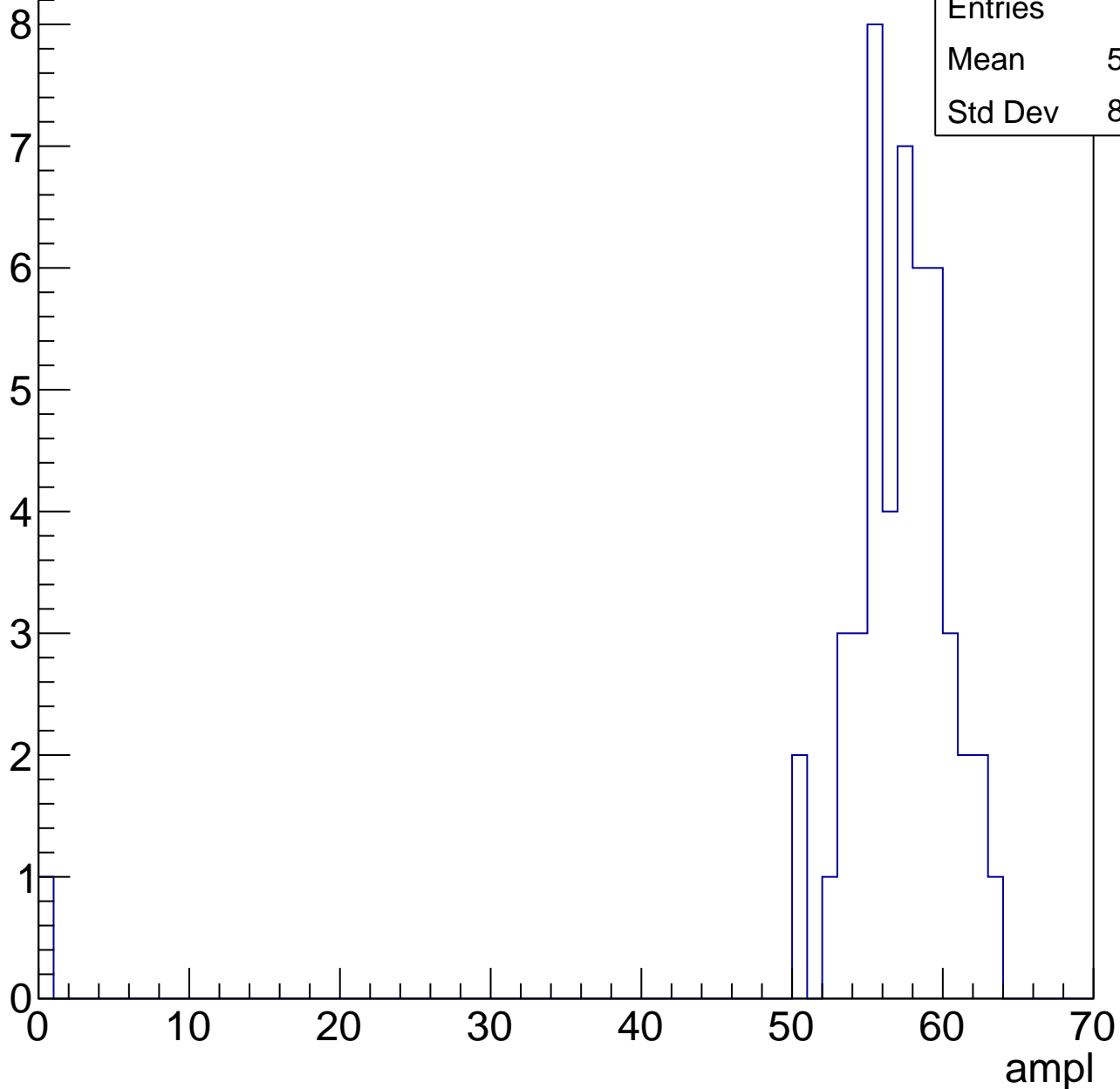


# B0L001S, U5-ch127, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	49
Mean	55.65
Std Dev	8.535

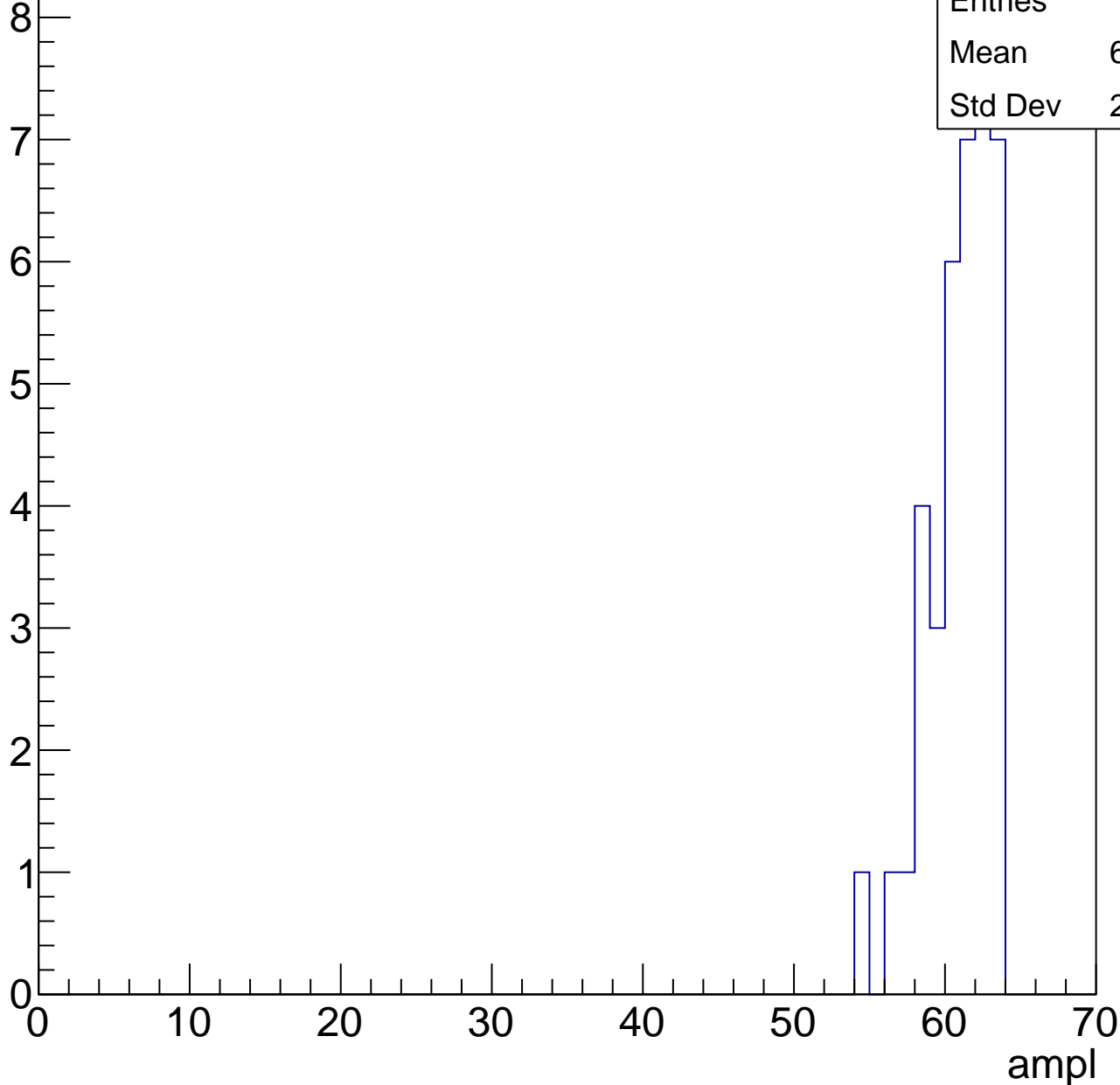


# B0L001S, U5-ch127, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	38
Mean	60.53
Std Dev	2.124



# B0L001S, U5-ch127, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U5-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U5-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0