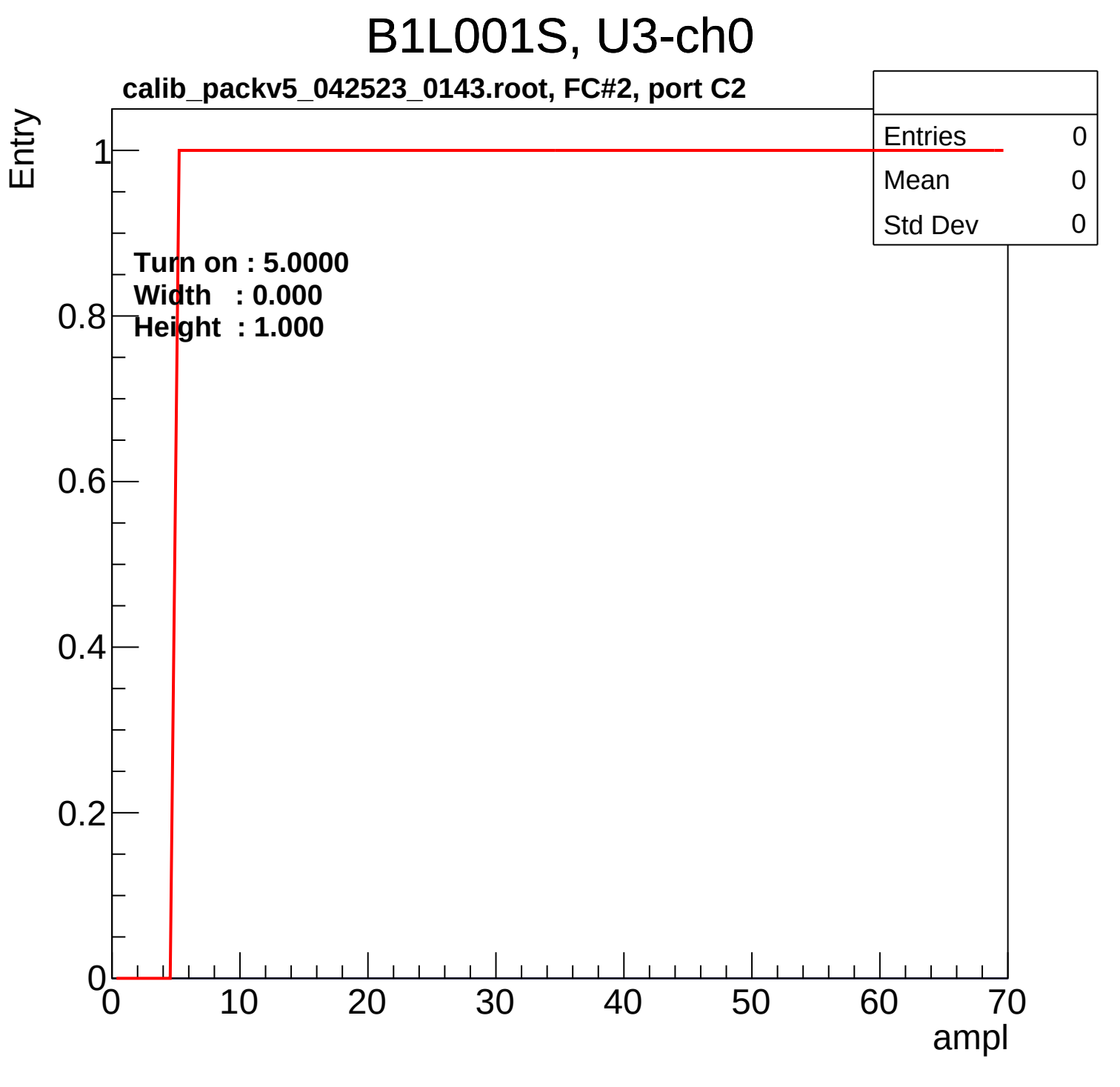
B1L001S, U3-ch0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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0.6
0.4
0.2
0
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10
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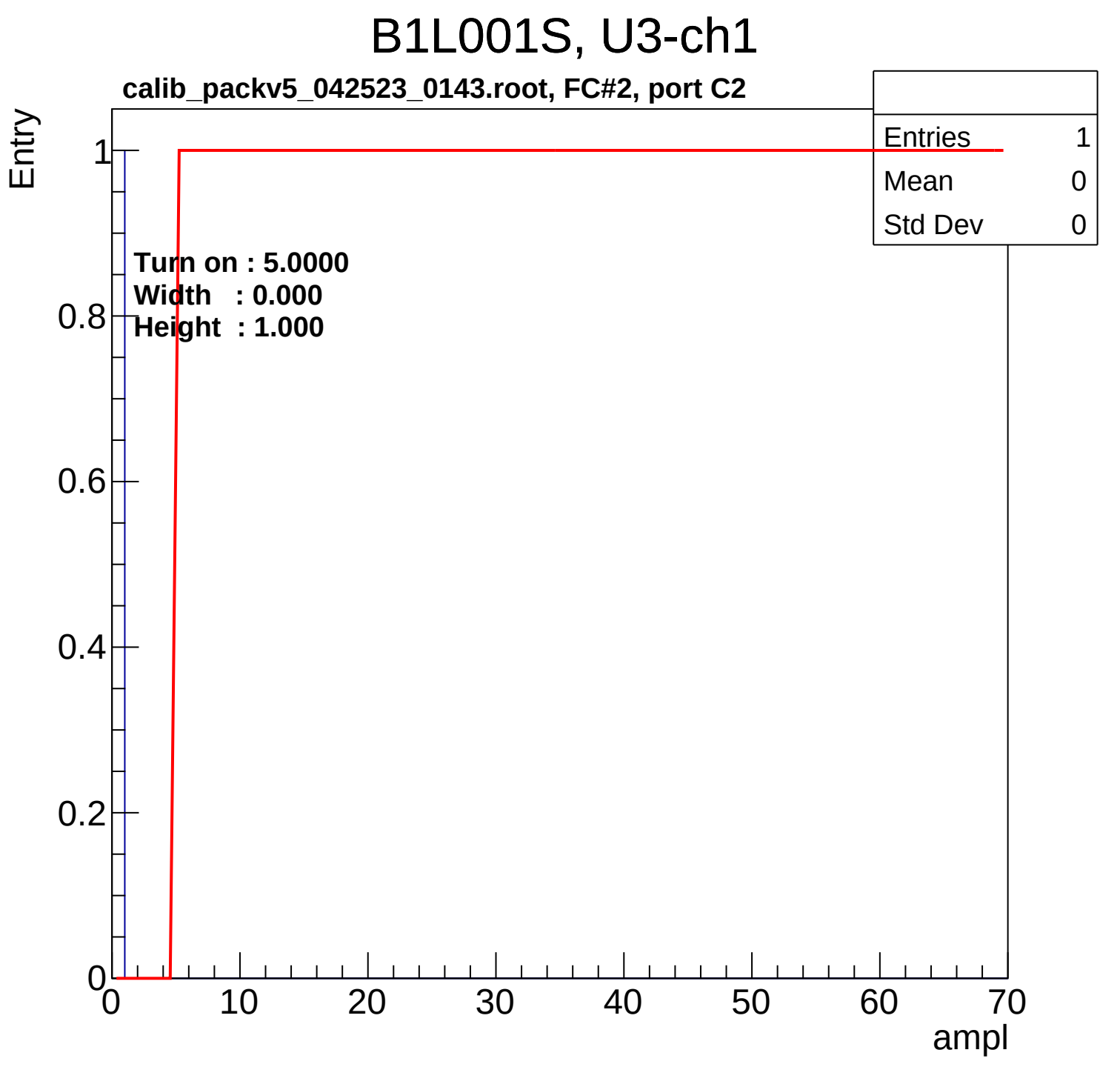
ampl


B1L001S, U3-ch1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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0.6
0.4
0.2
0
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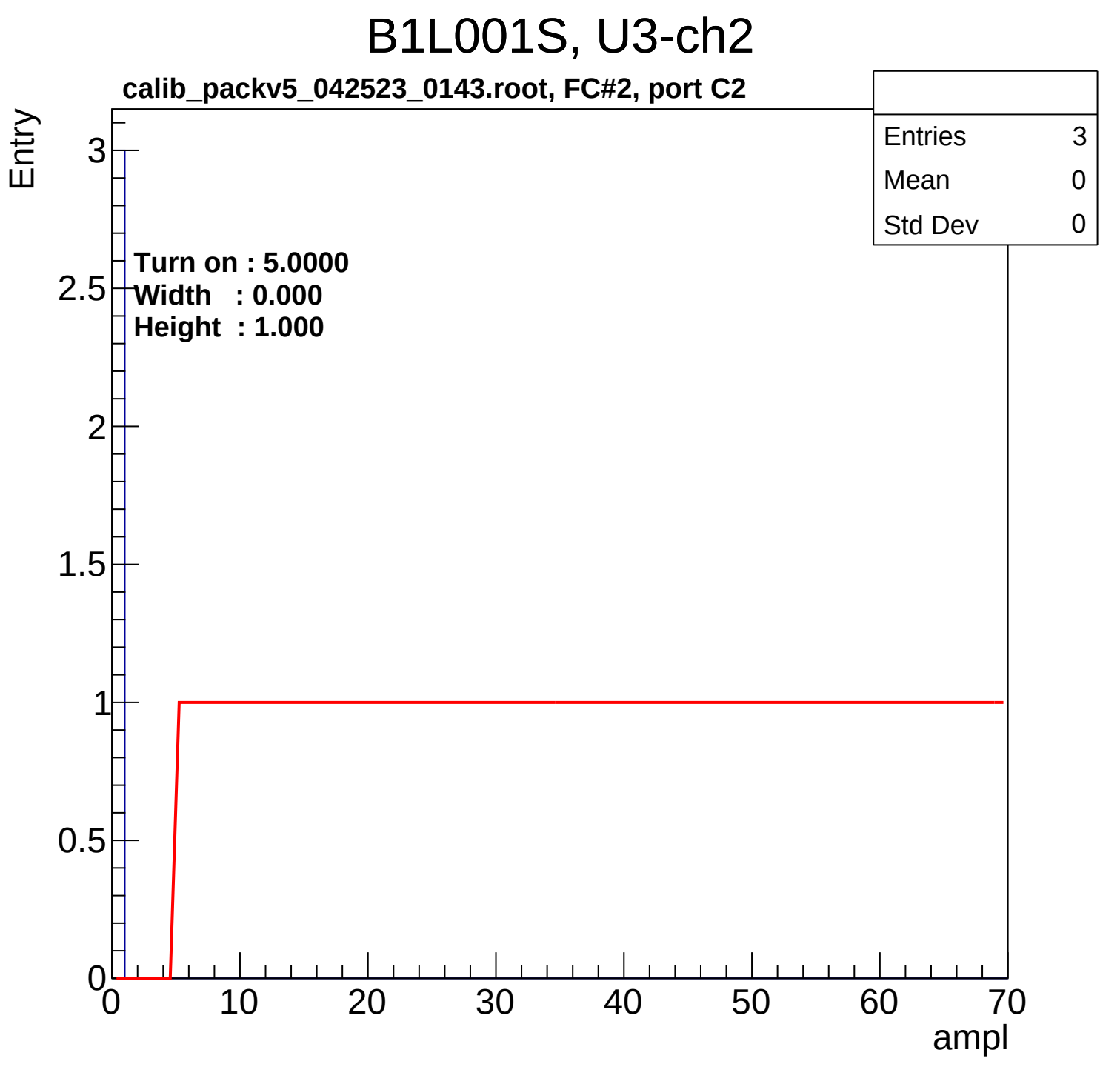
70
ampl


B1L001S, U3-ch2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
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40
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60
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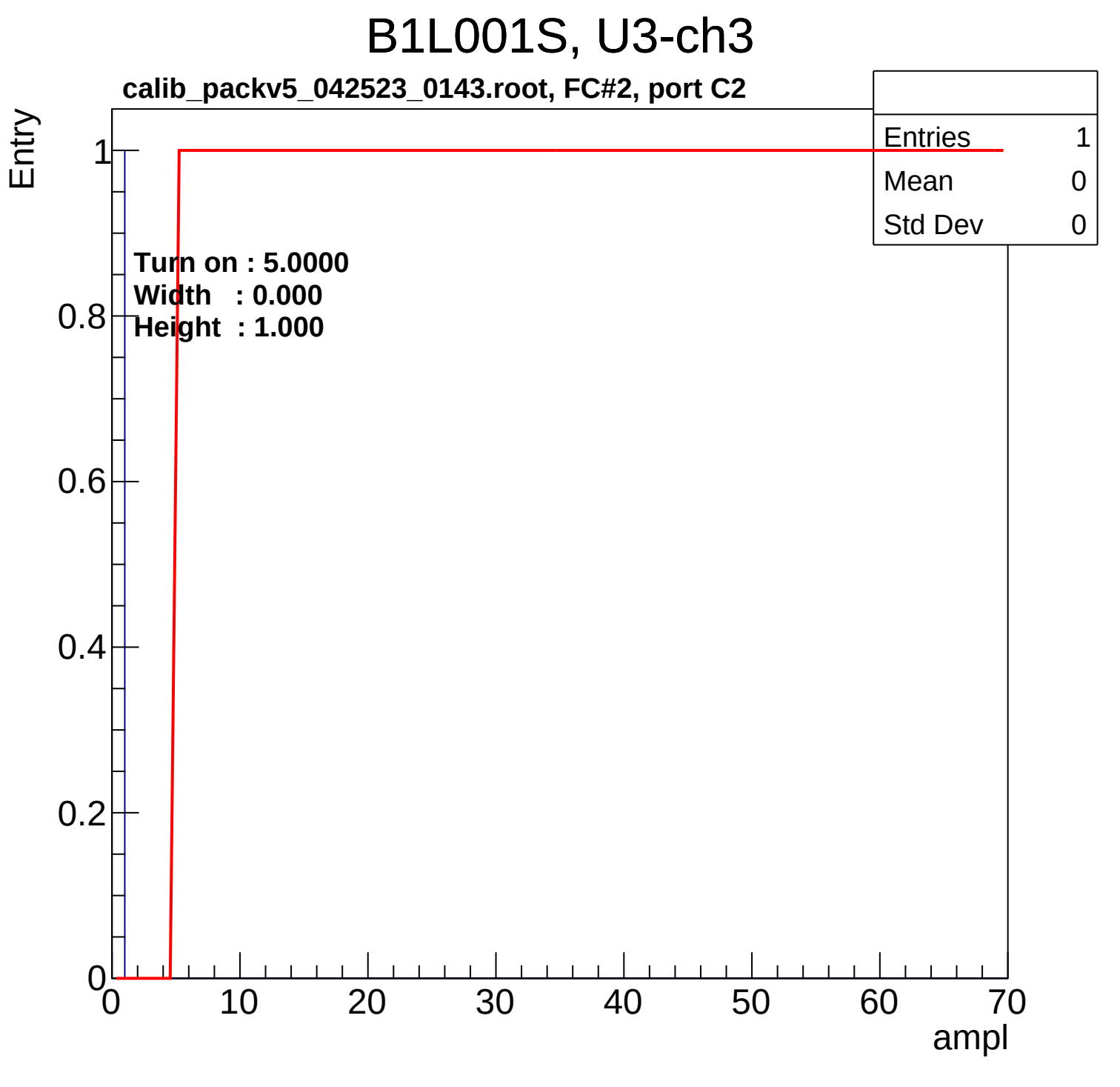
B1L001S, U3-ch3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
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0.8
0.6
0.4
0.2
0
0
10
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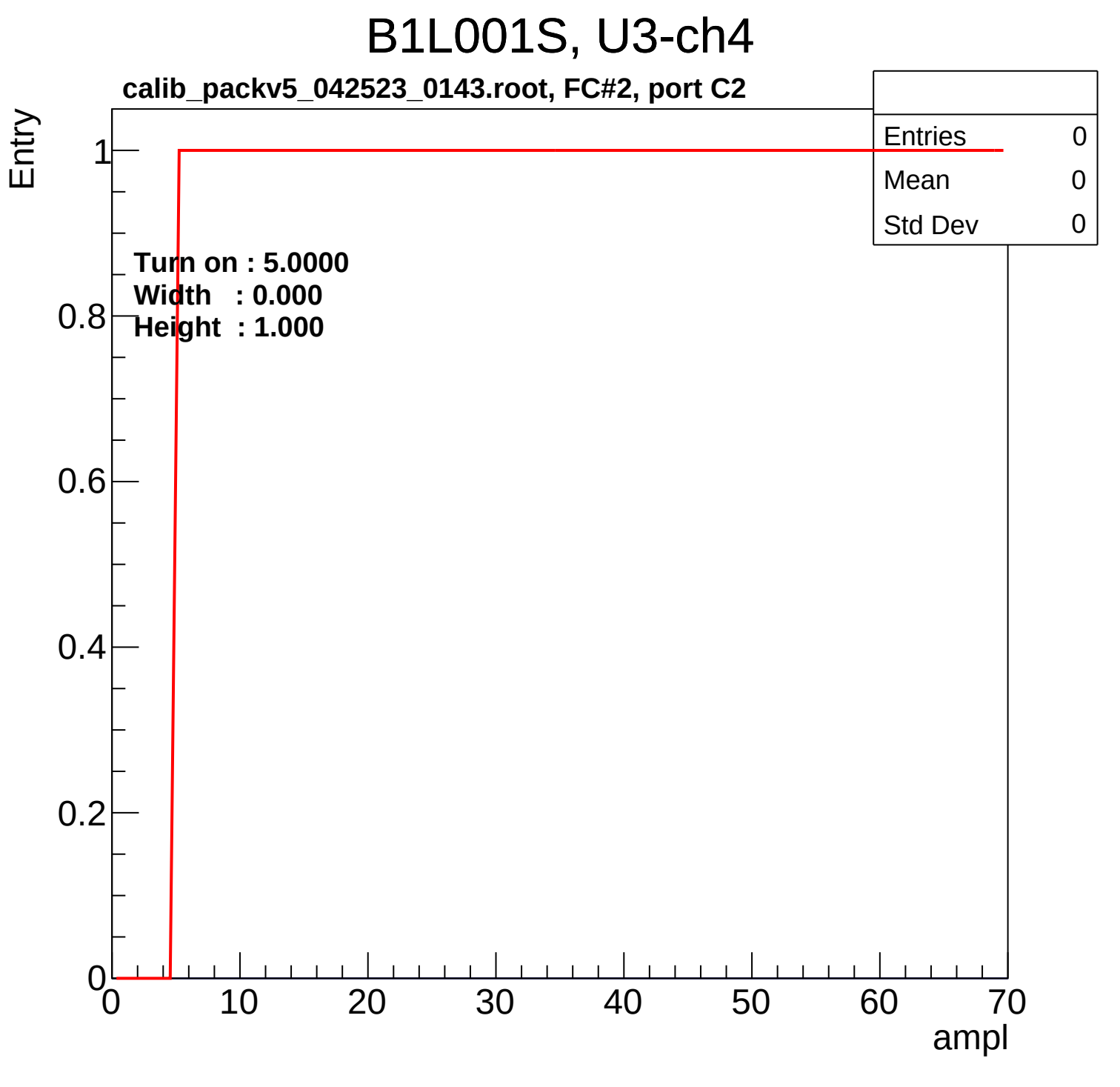
50
60
70
ampl


B1L001S, U3-ch4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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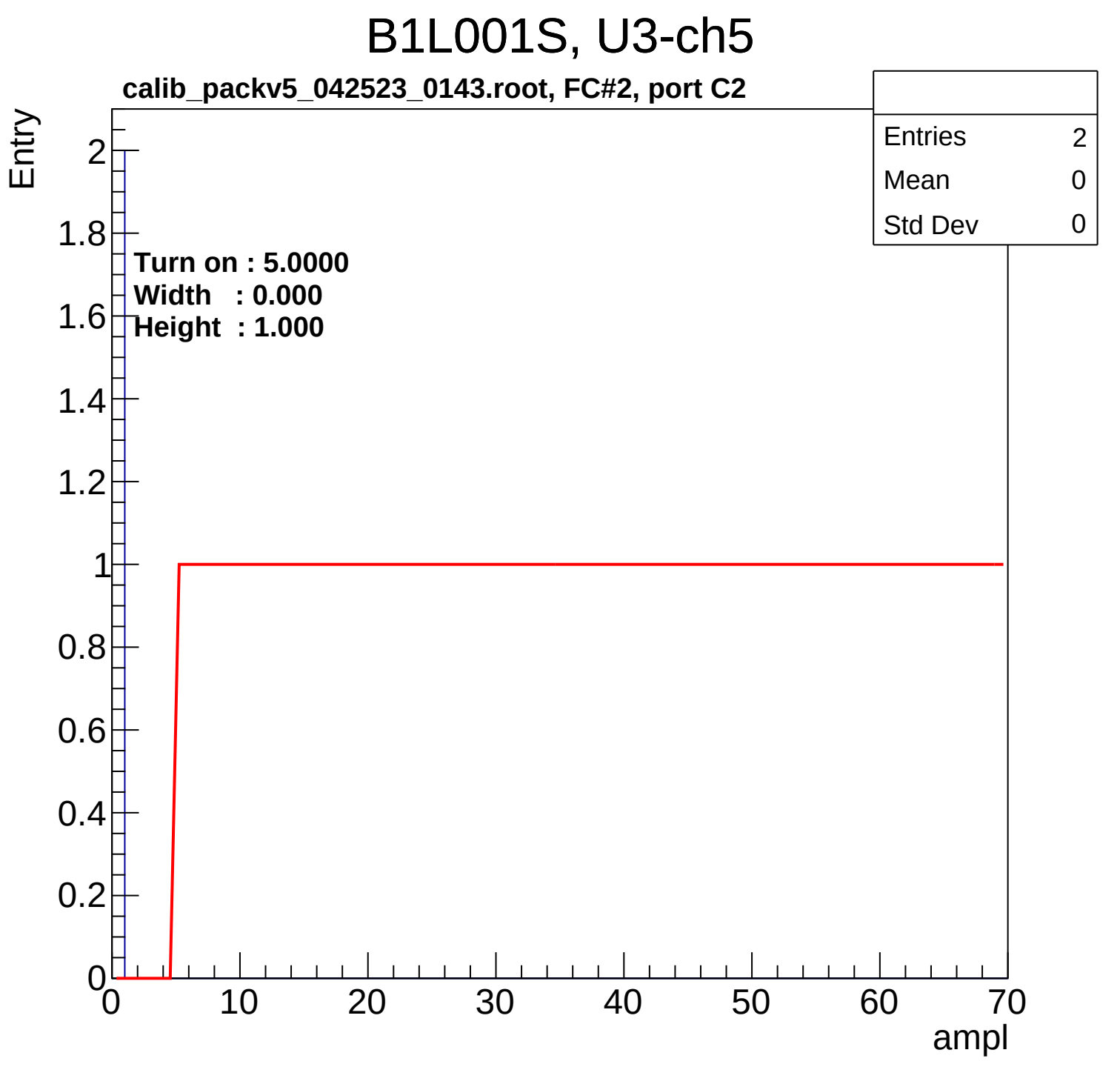
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U3-ch5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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60
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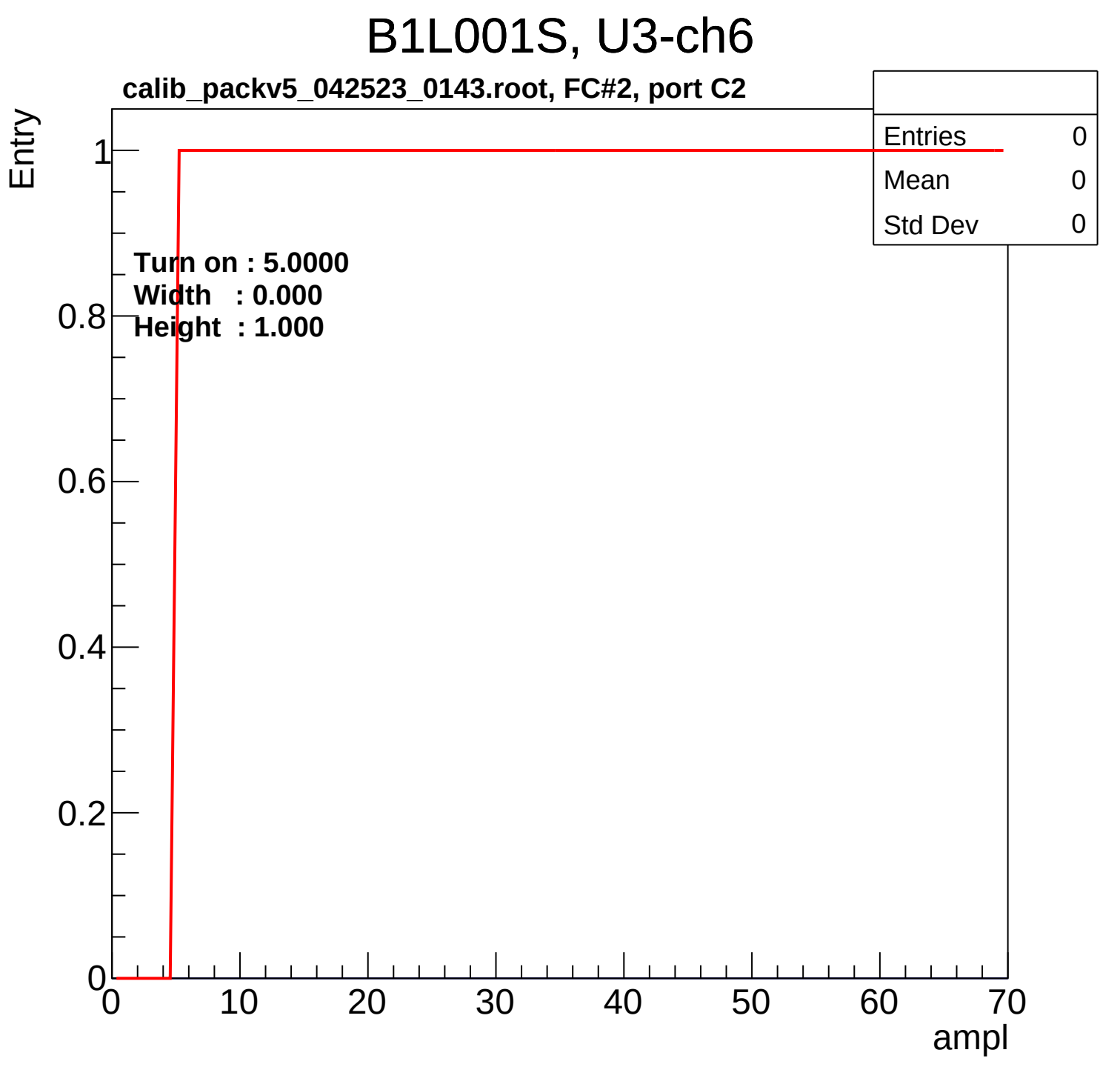
B1L001S, U3-ch6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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0.8
0.6
0.4
0.2
0
0
10
20
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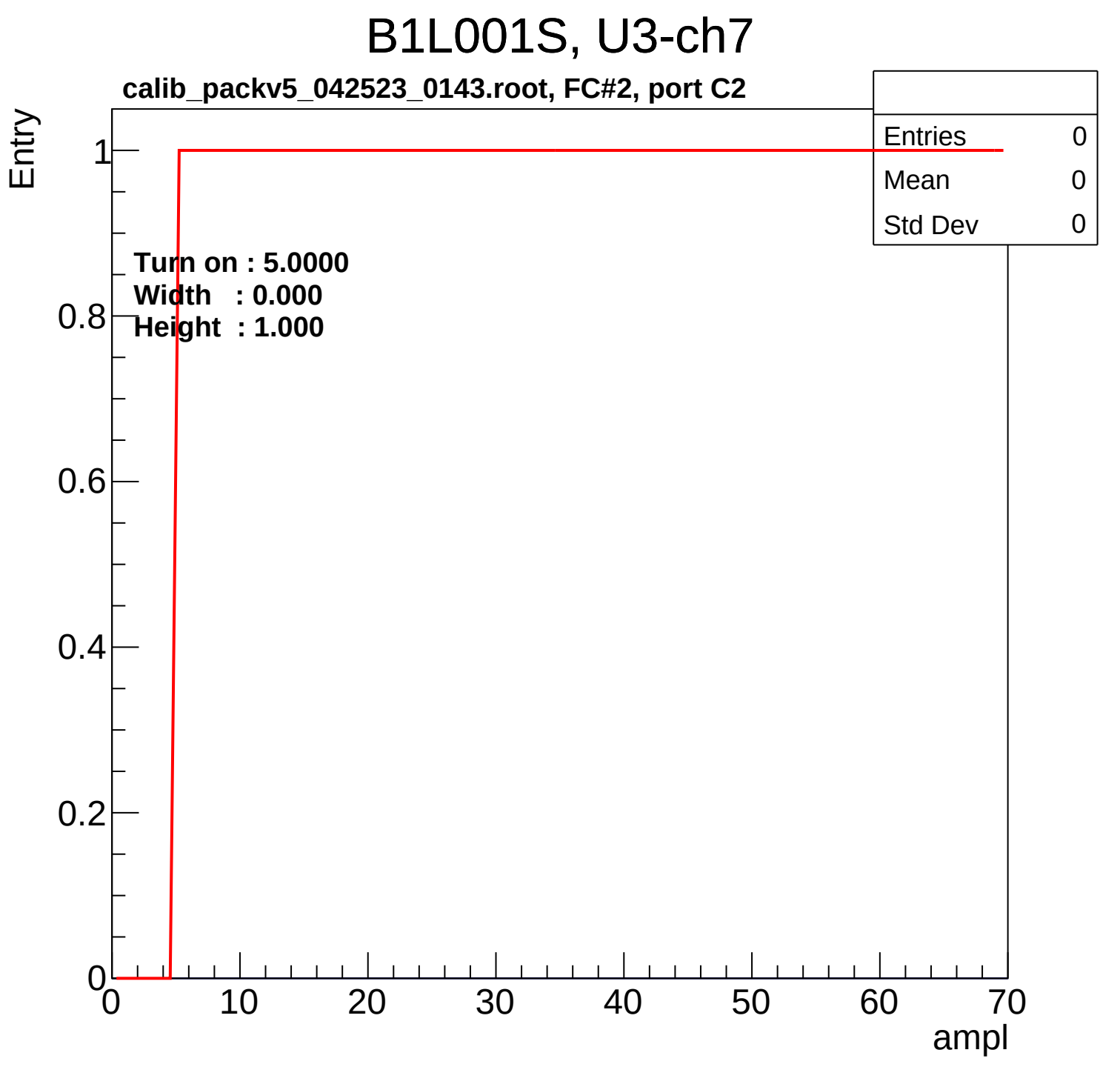
50
60
70
ampl


B1L001S, U3-ch7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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0.8
0.6
0.4
0.2
0
0
10
20
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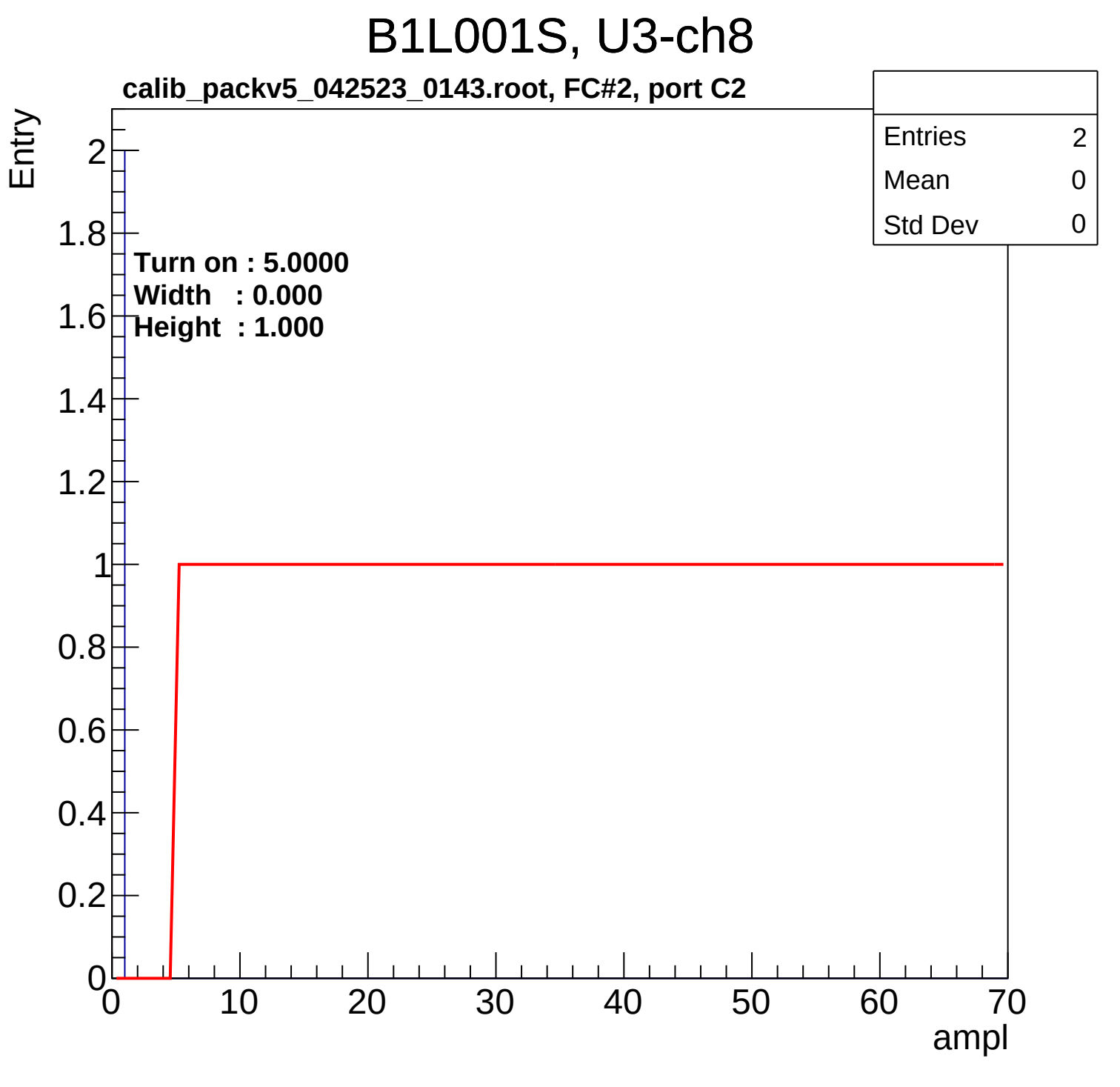
50
60
70
ampl


B1L001S, U3-ch8
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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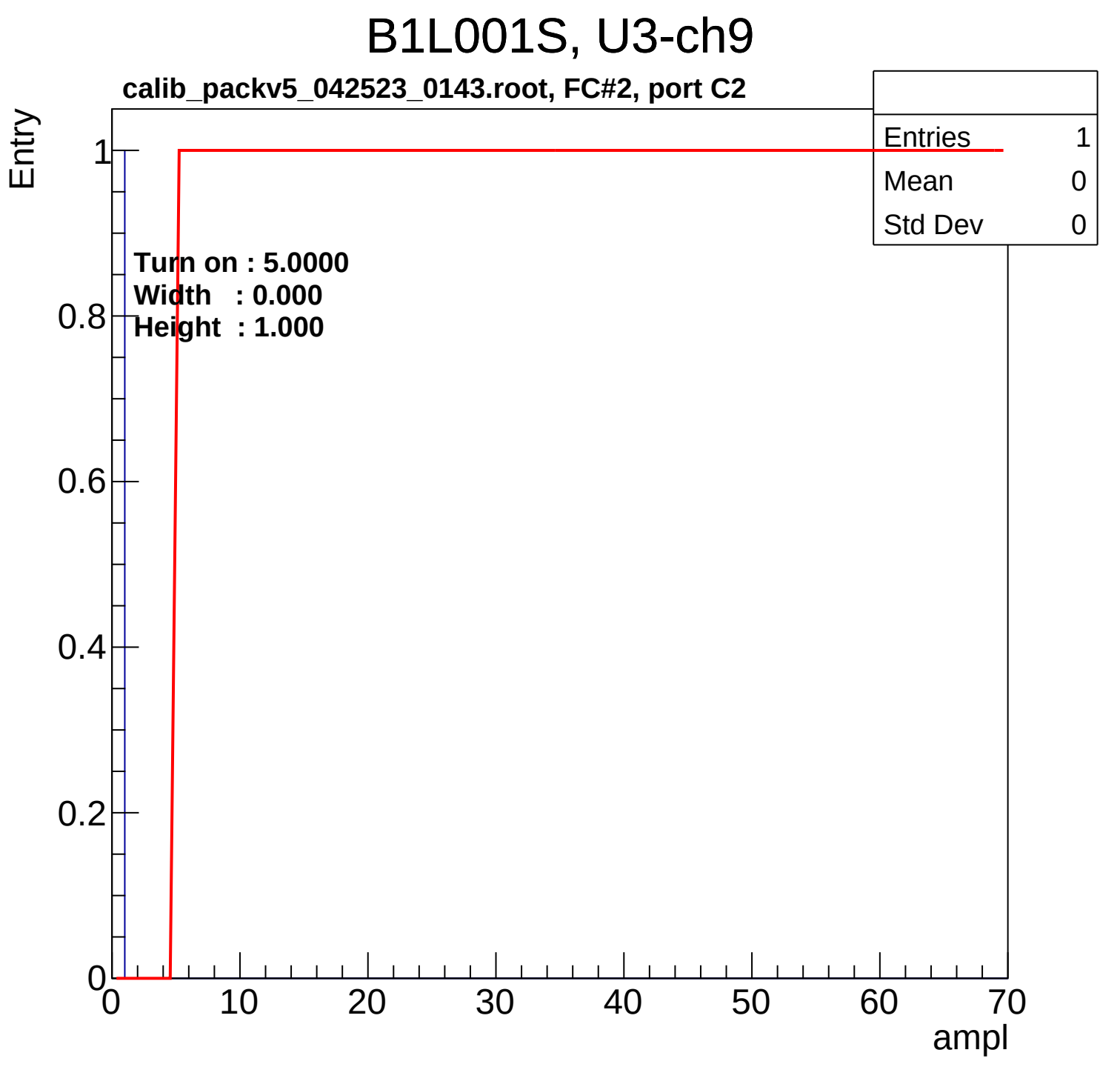
B1L001S, U3-ch9
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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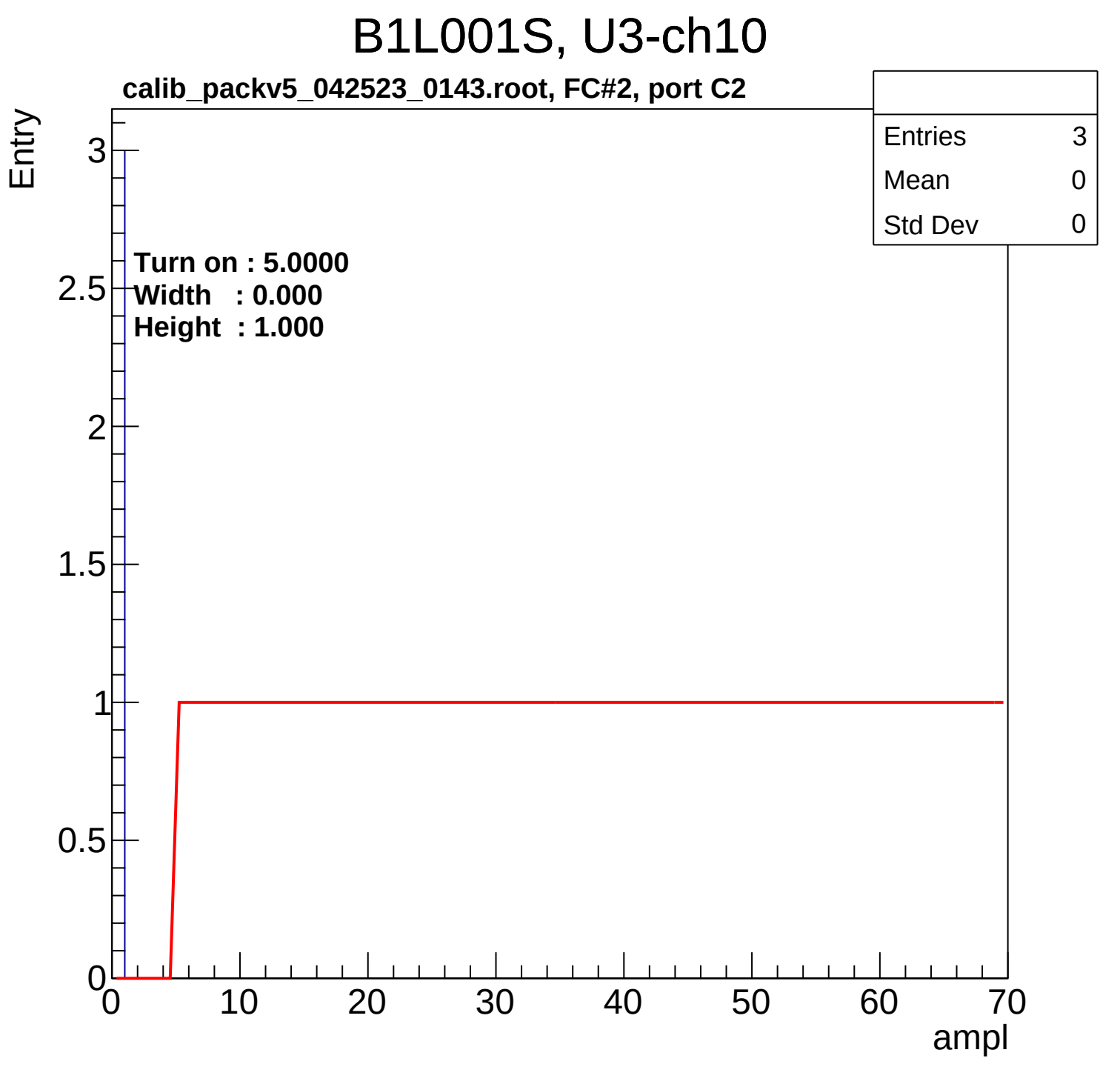
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U3-ch10
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
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20
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40
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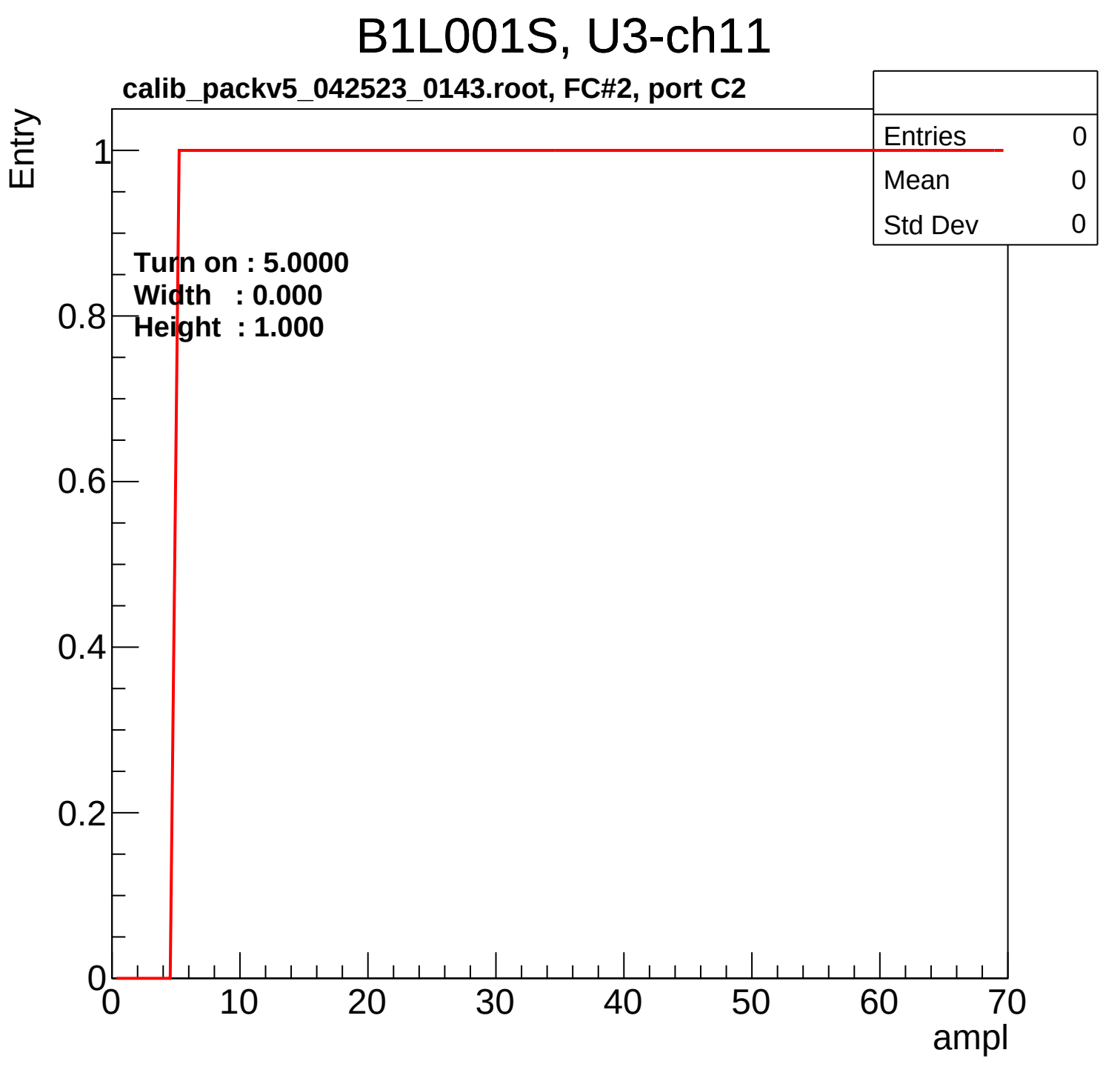
B1L001S, U3-ch11
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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0.8
0.6
0.4
0.2
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20
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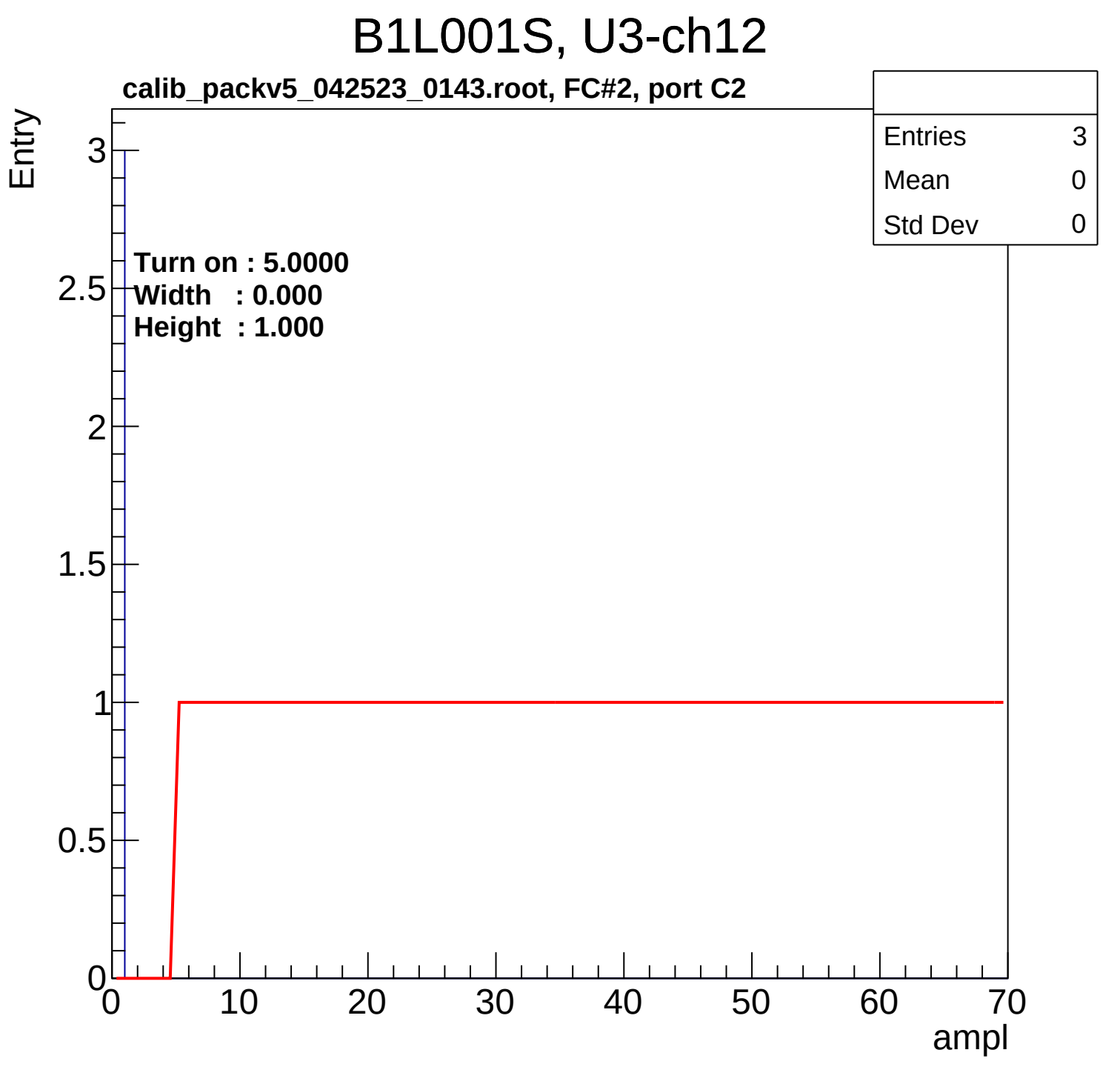
50
60
70
ampl


B1L001S, U3-ch12
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
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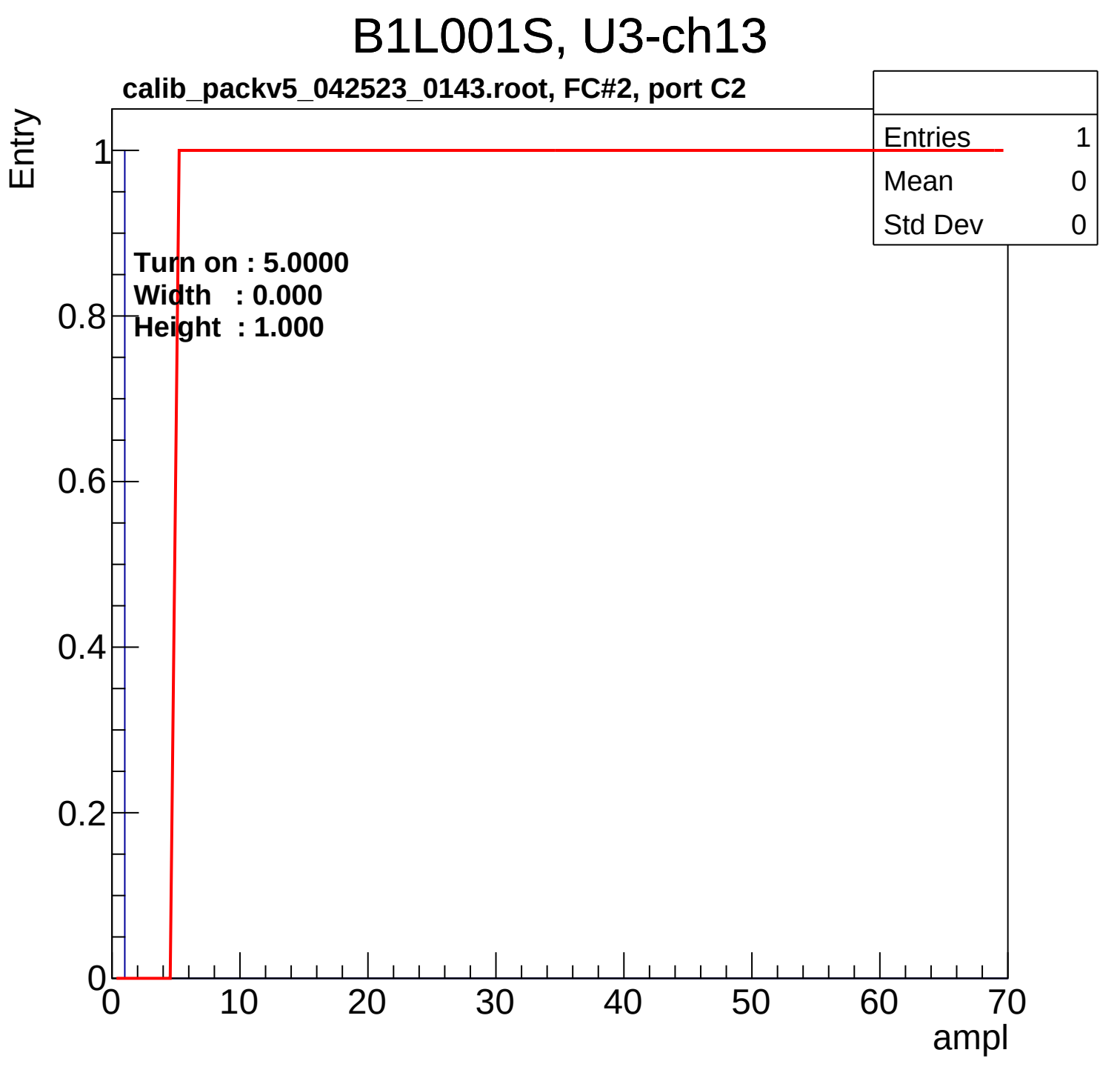
B1L001S, U3-ch13
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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0.6
0.4
0.2
0
0
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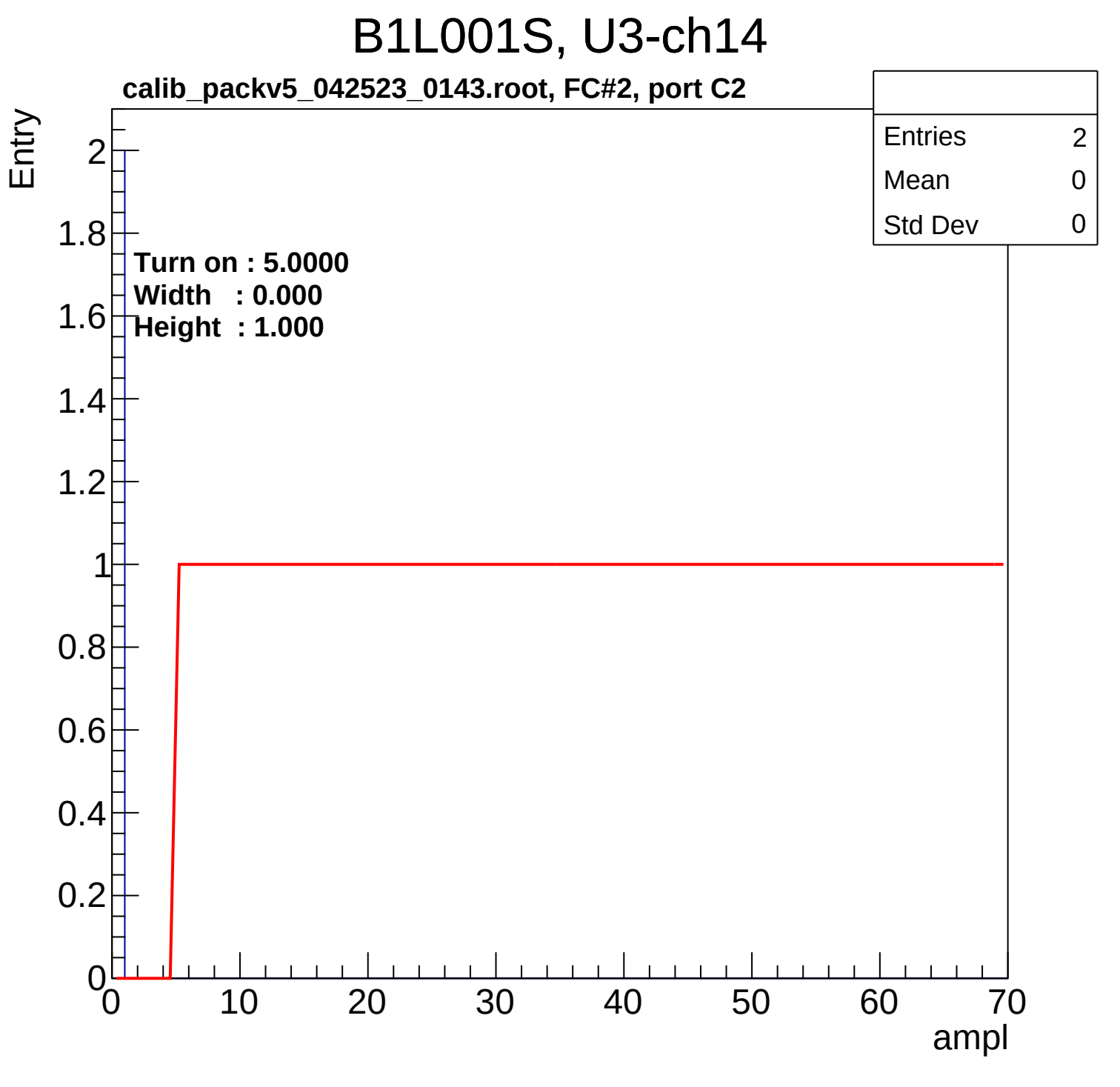
20
30
40
50
60
70
ampl


B1L001S, U3-ch14
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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20
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60
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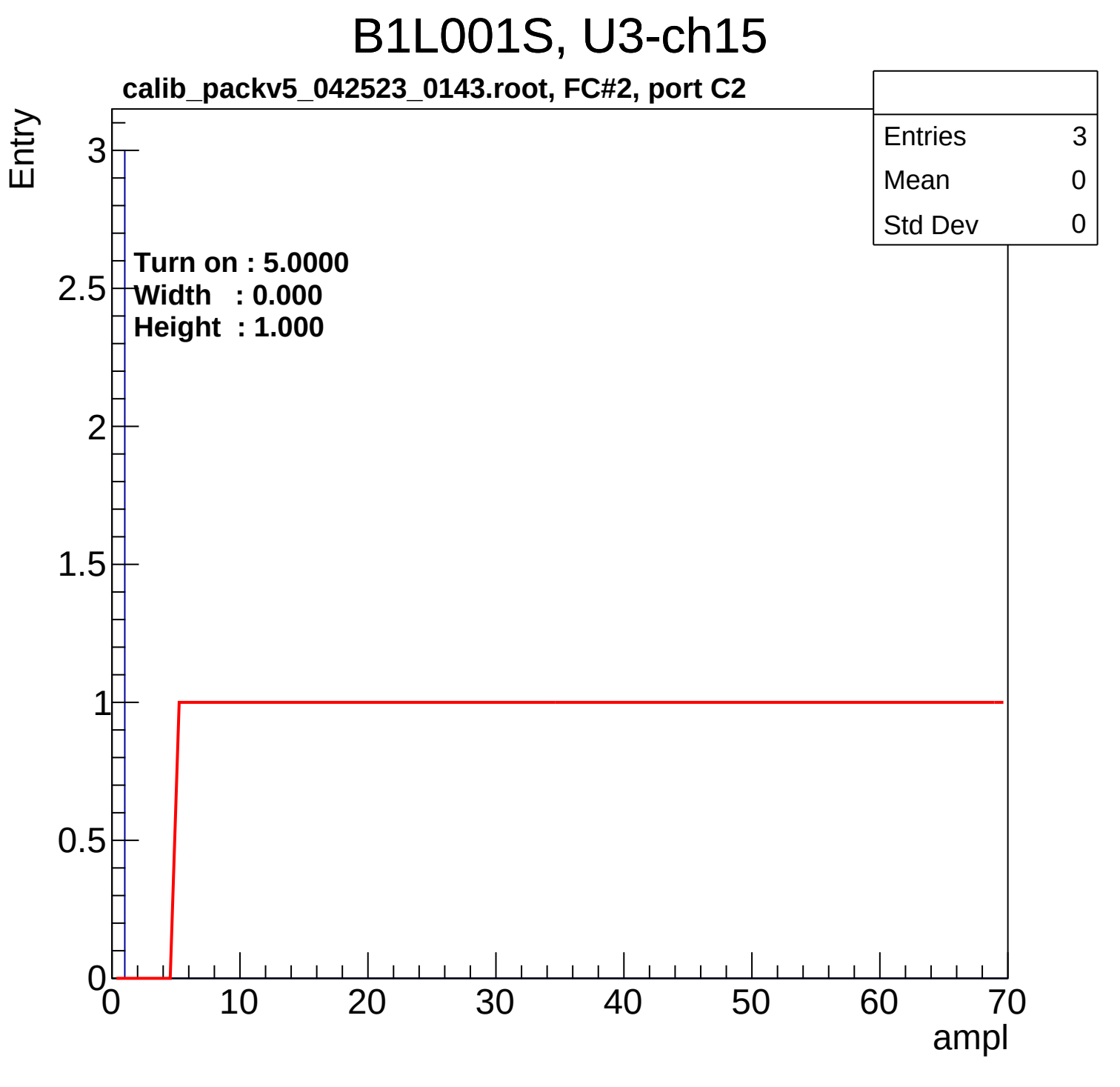
B1L001S, U3-ch15
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
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20
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60
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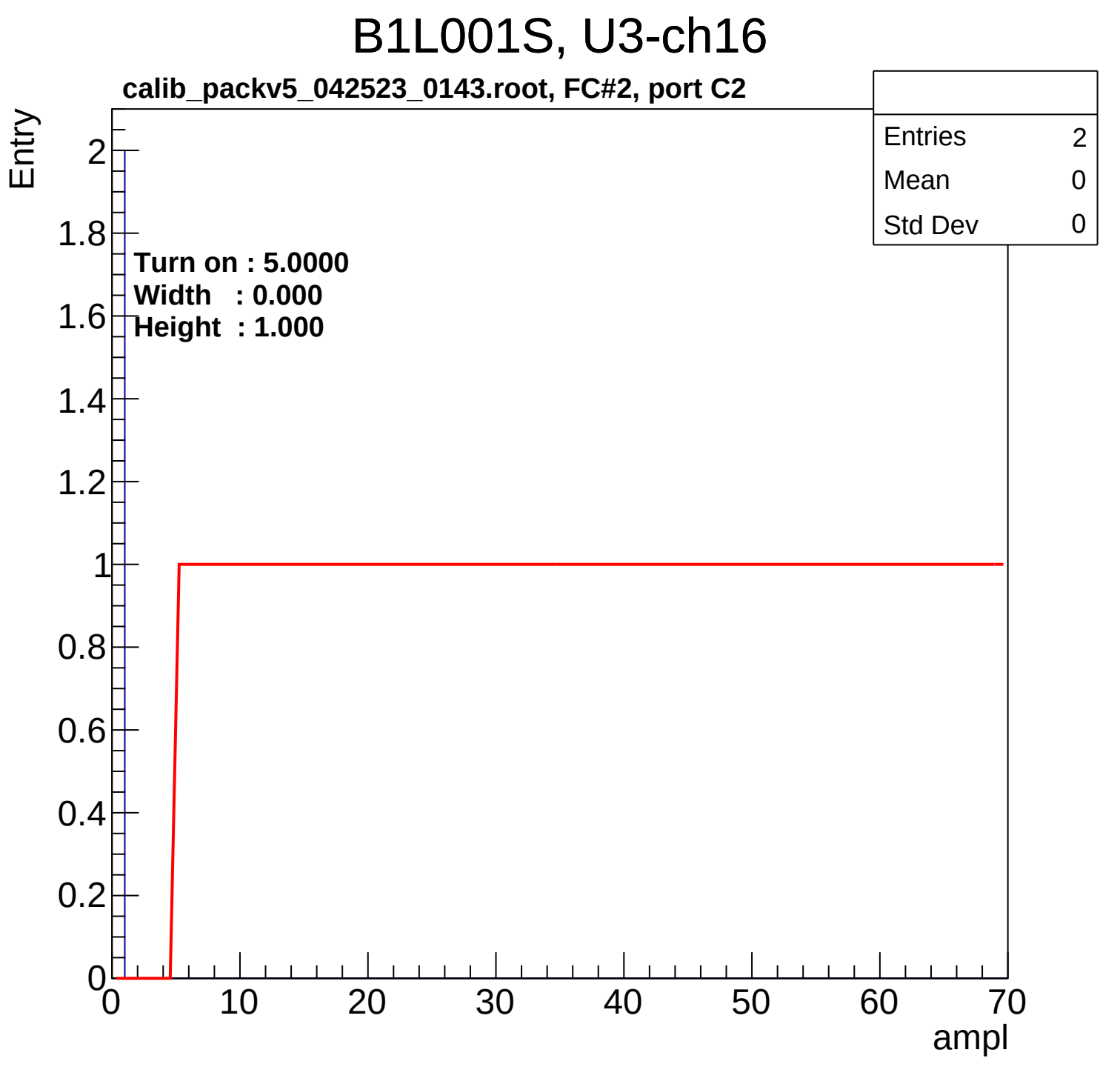
B1L001S, U3-ch16
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
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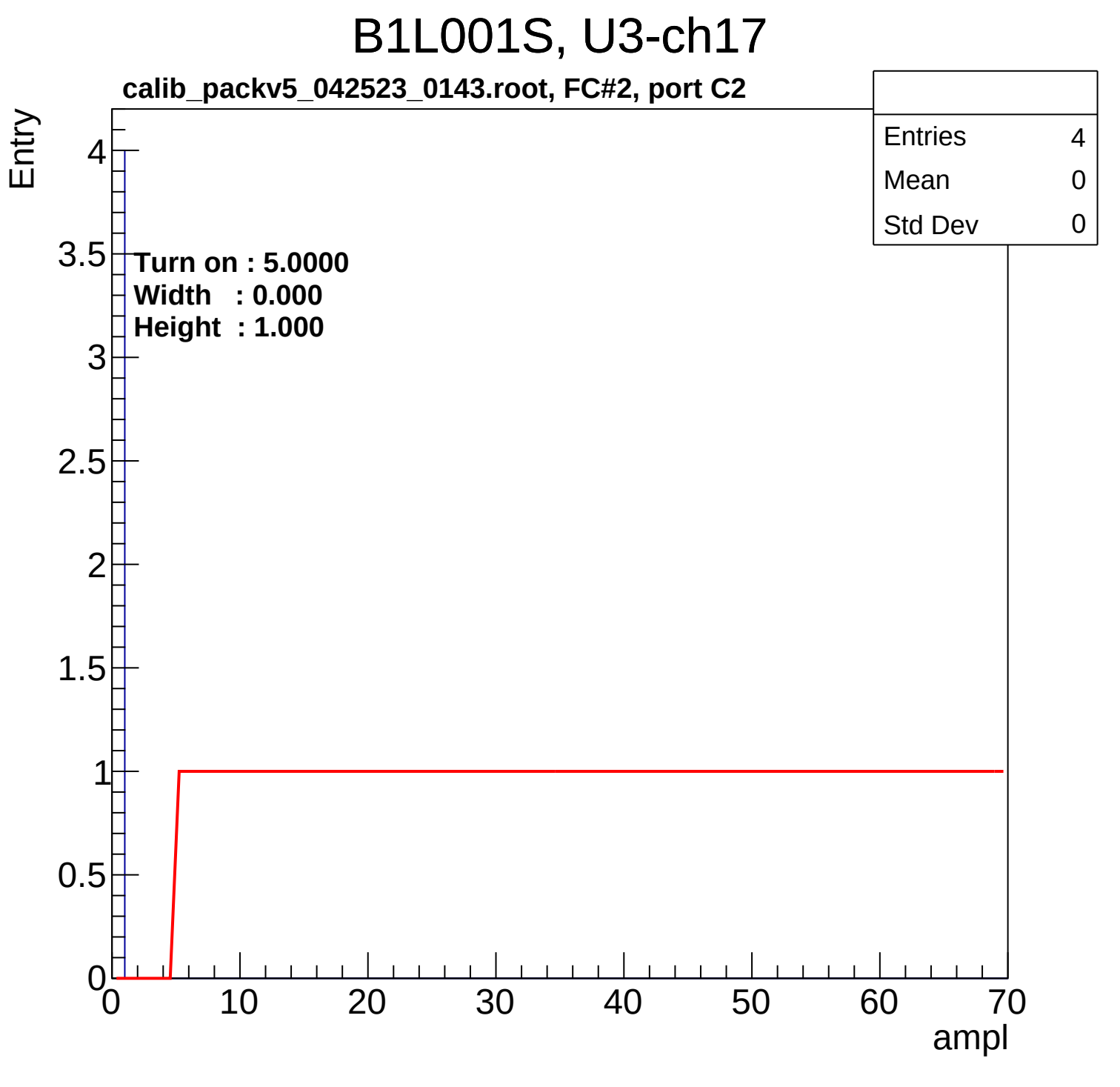
B1L001S, U3-ch17
calib_packv5_042523_0143.root, FC#2, port C2
Entries 4
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
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60
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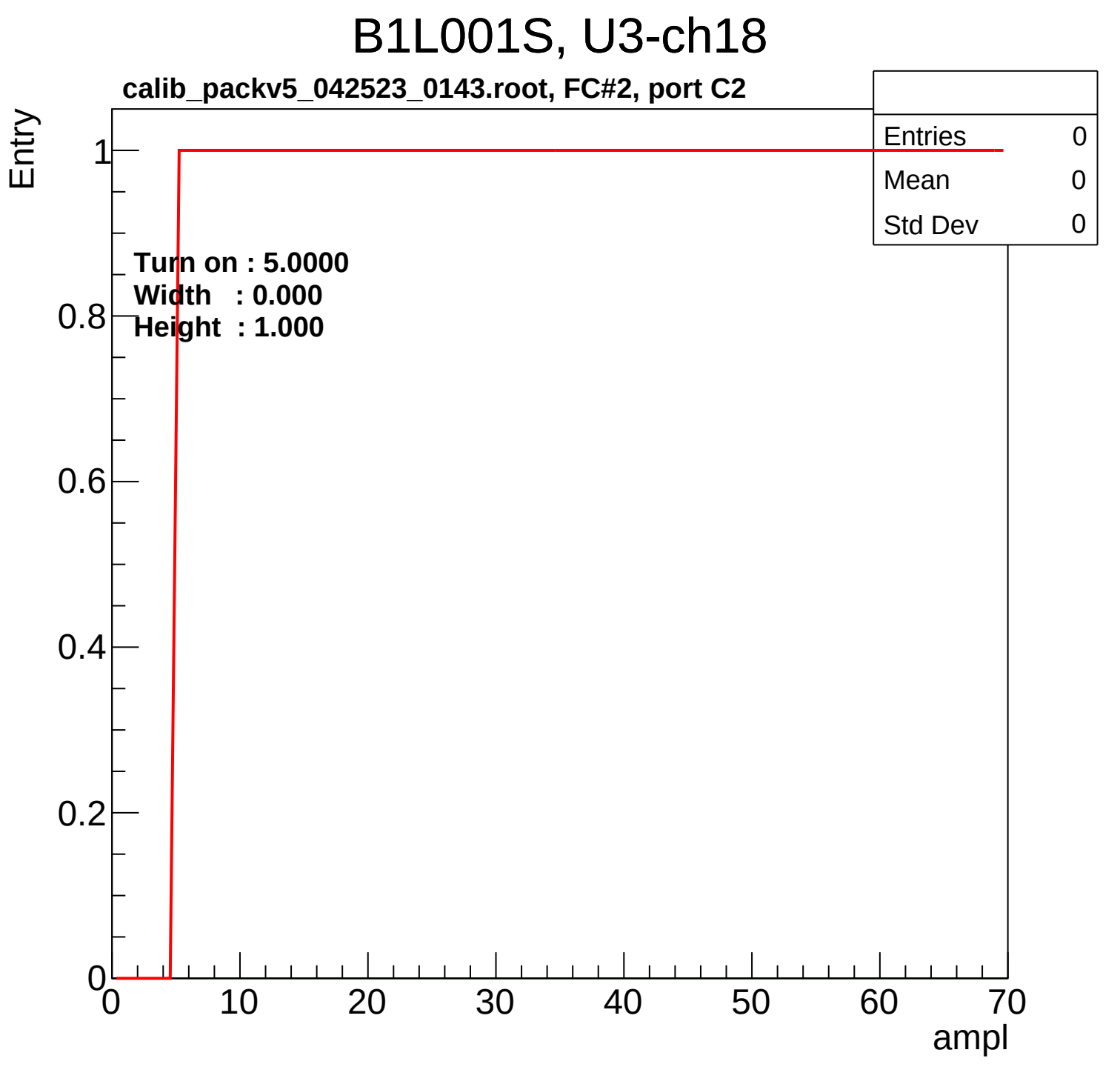
B1L001S, U3-ch18
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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0.4
0.2
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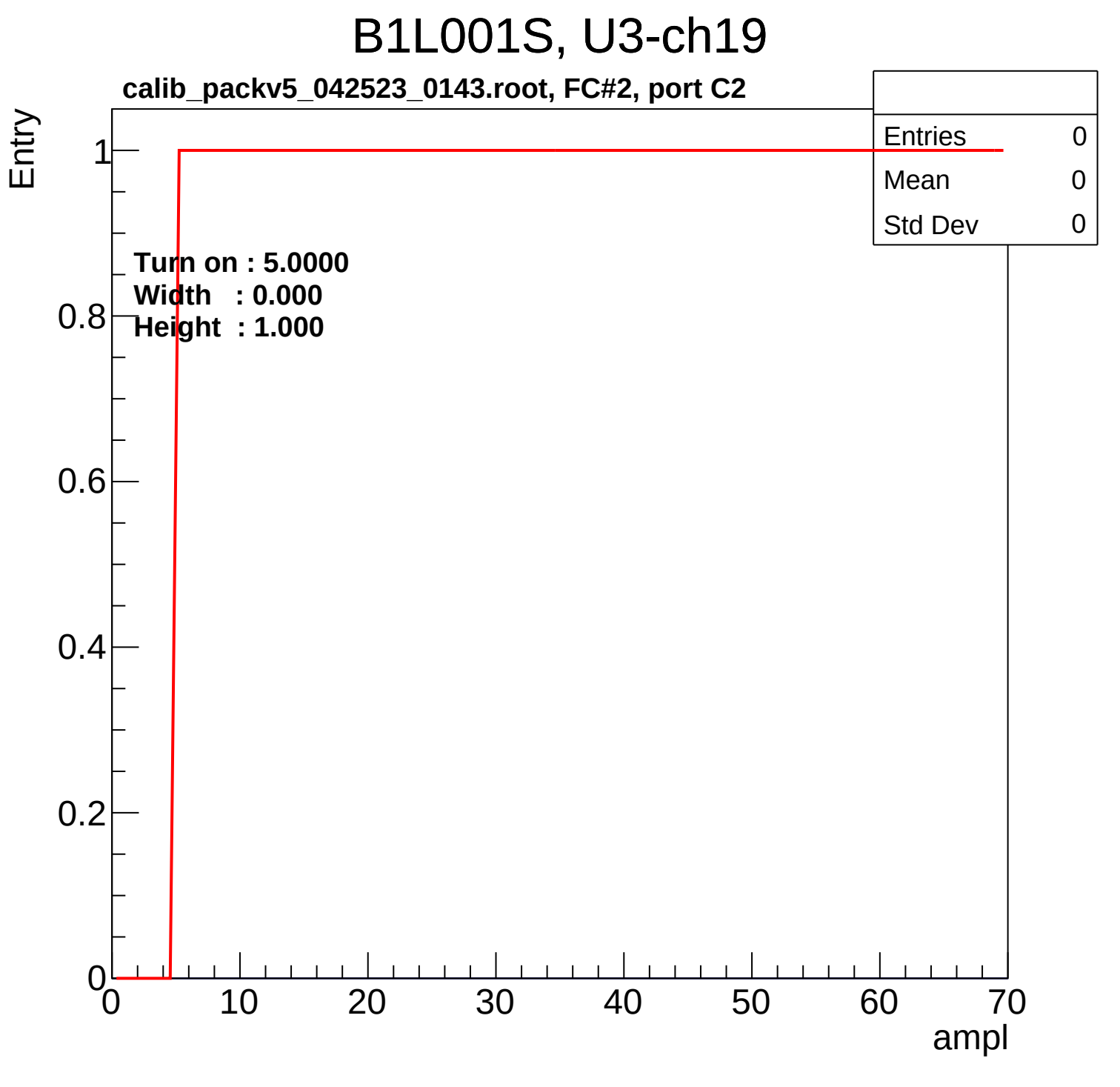
ampl


B1L001S, U3-ch19
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
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0.4
0.2
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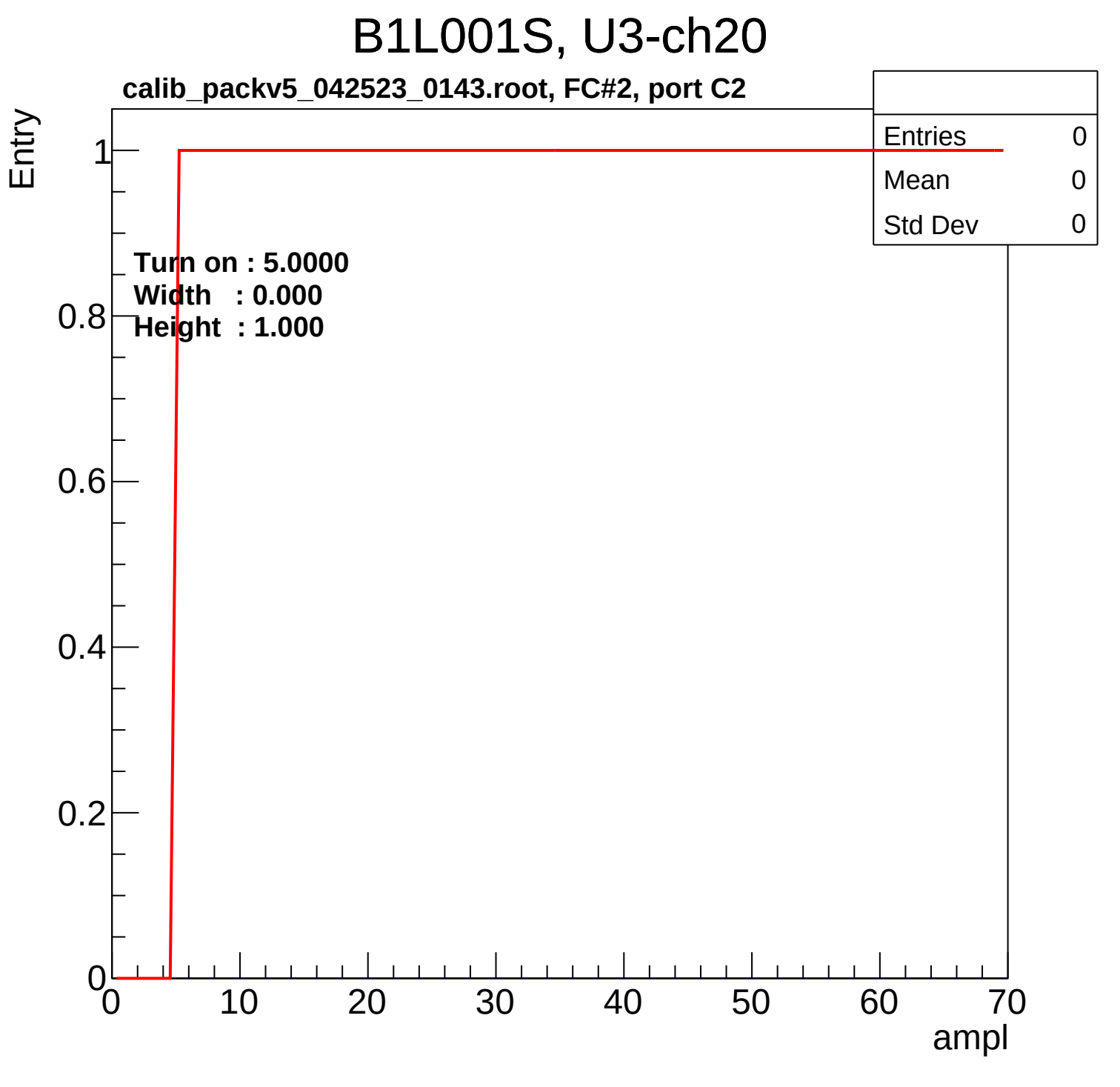
70
ampl


B1L001S, U3-ch20
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
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0.4
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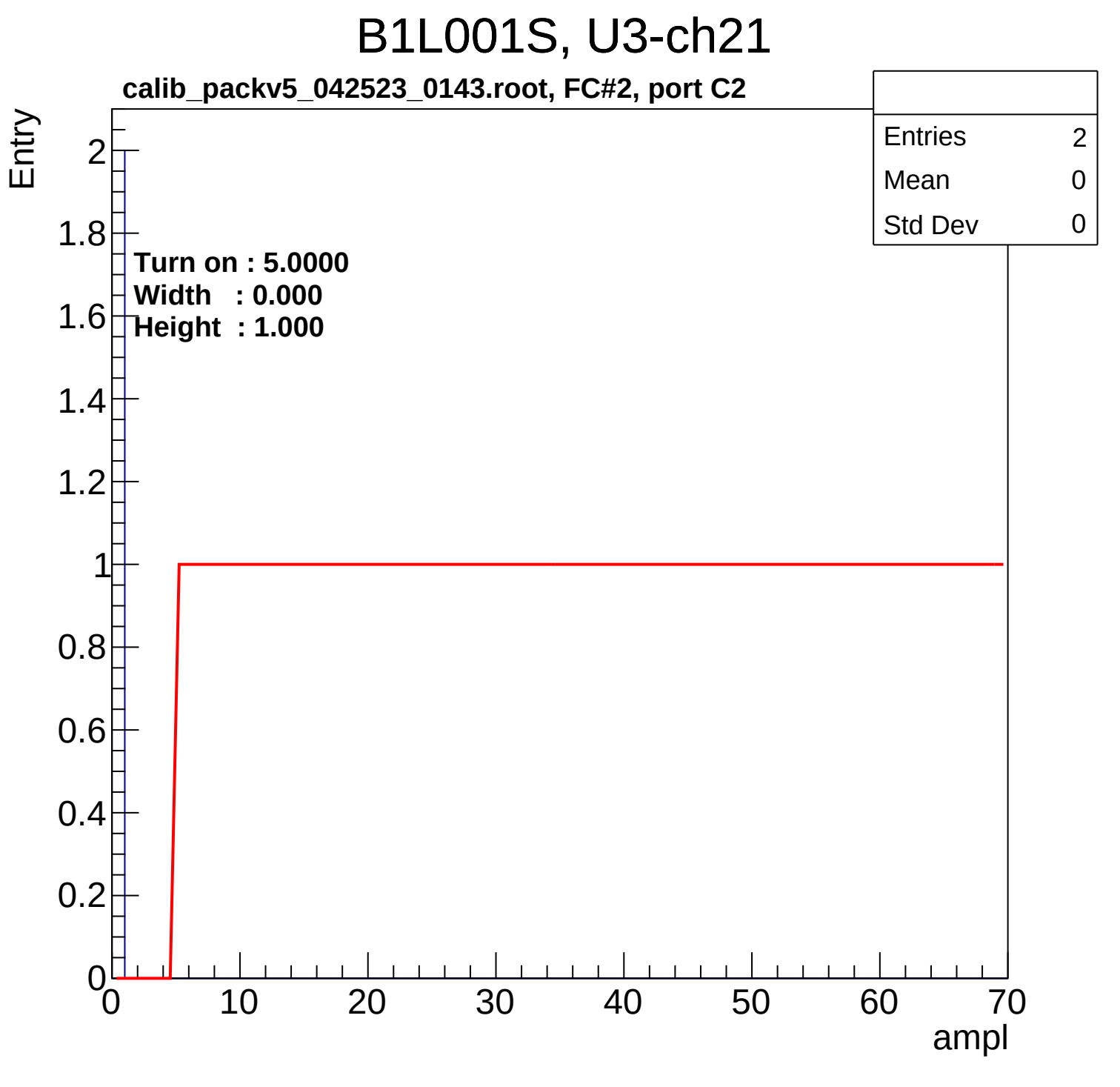
70
ampl


B1L001S, U3-ch21
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.2
0.4
0.6
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1.2
1.4
1.6
1.8
2
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60
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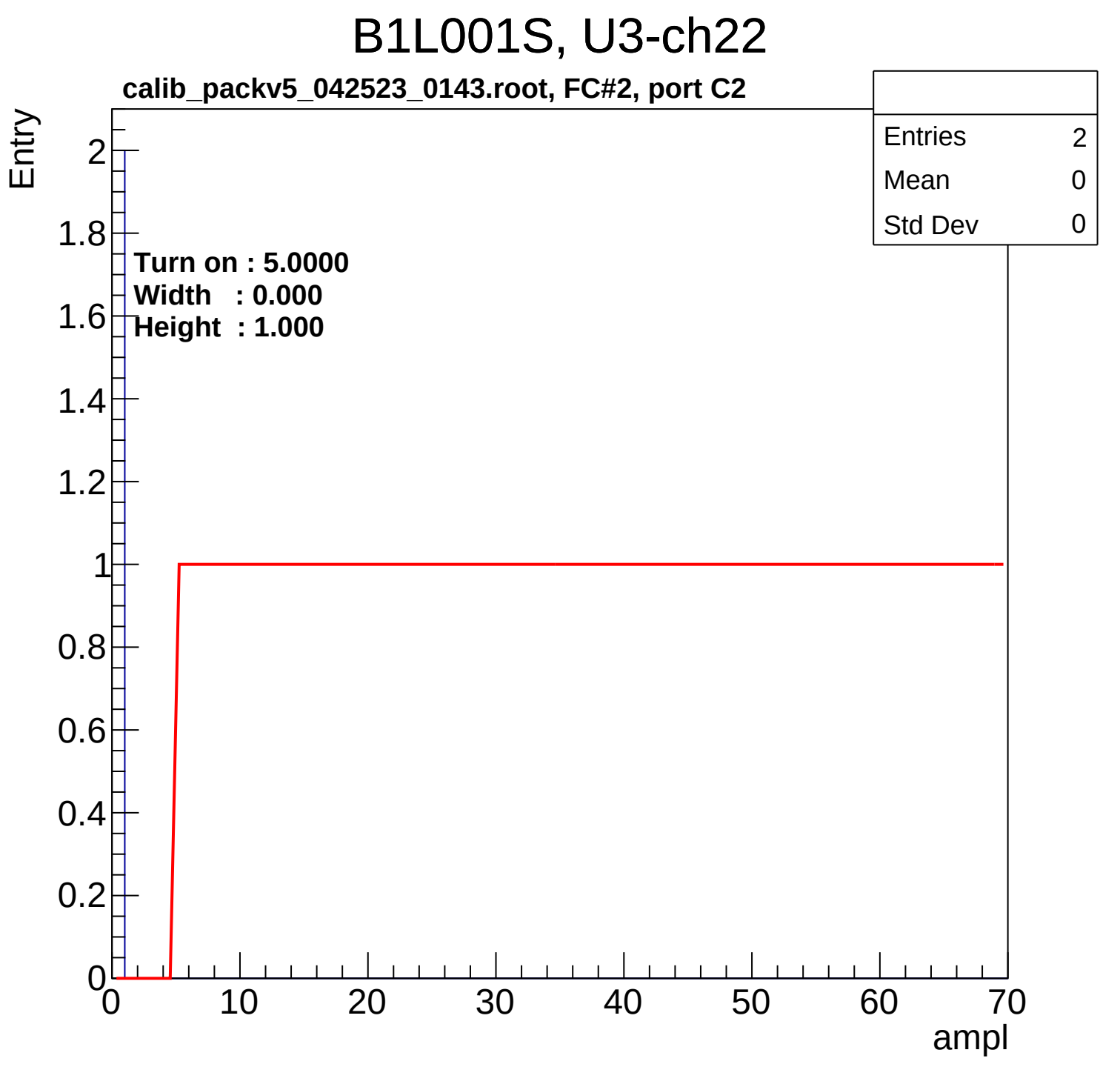
B1L001S, U3-ch22
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.2
0.4
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1.2
1.4
1.6
1.8
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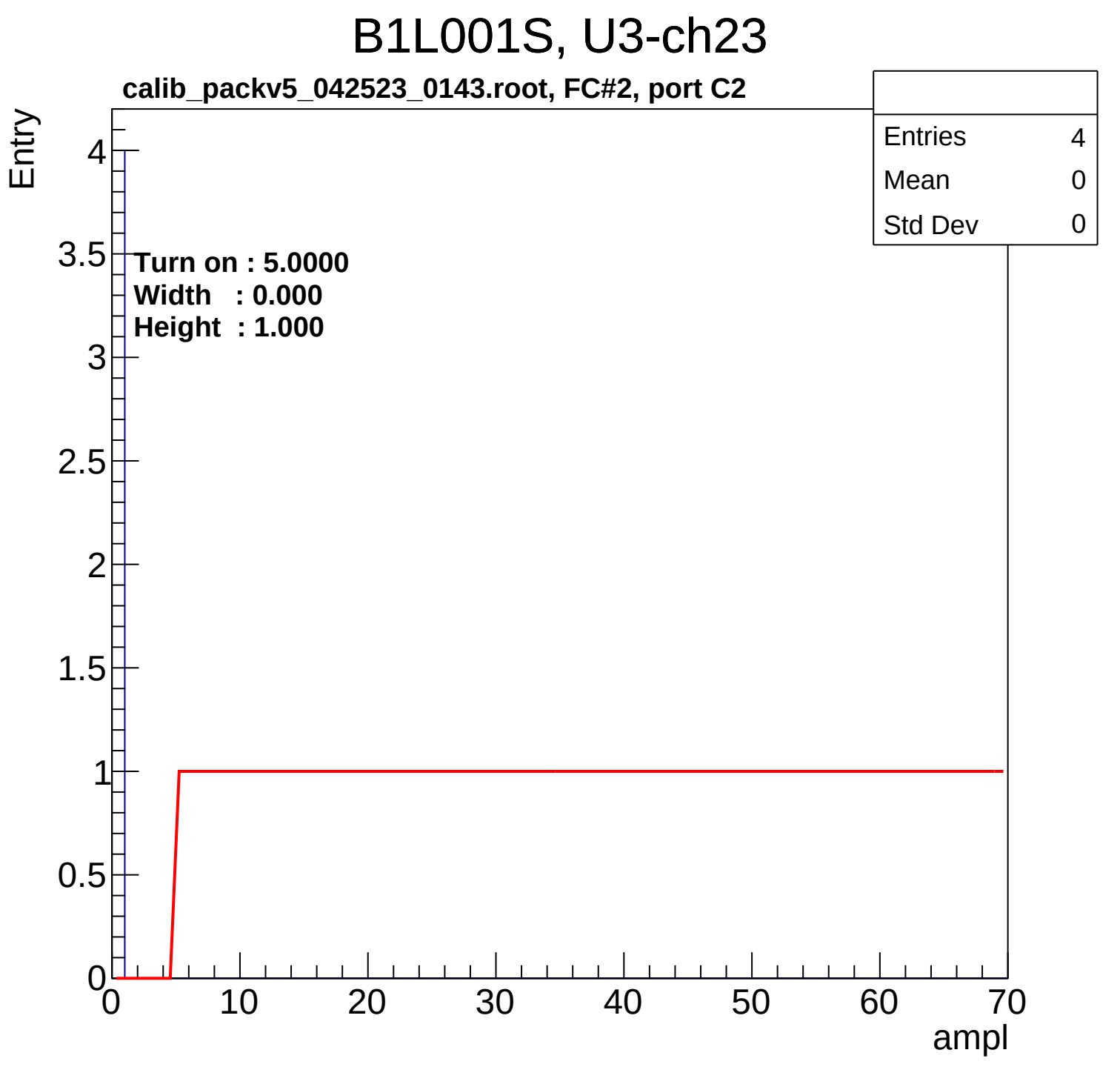
B1L001S, U3-ch23
calib_packv5_042523_0143.root, FC#2, port C2
Entries 4
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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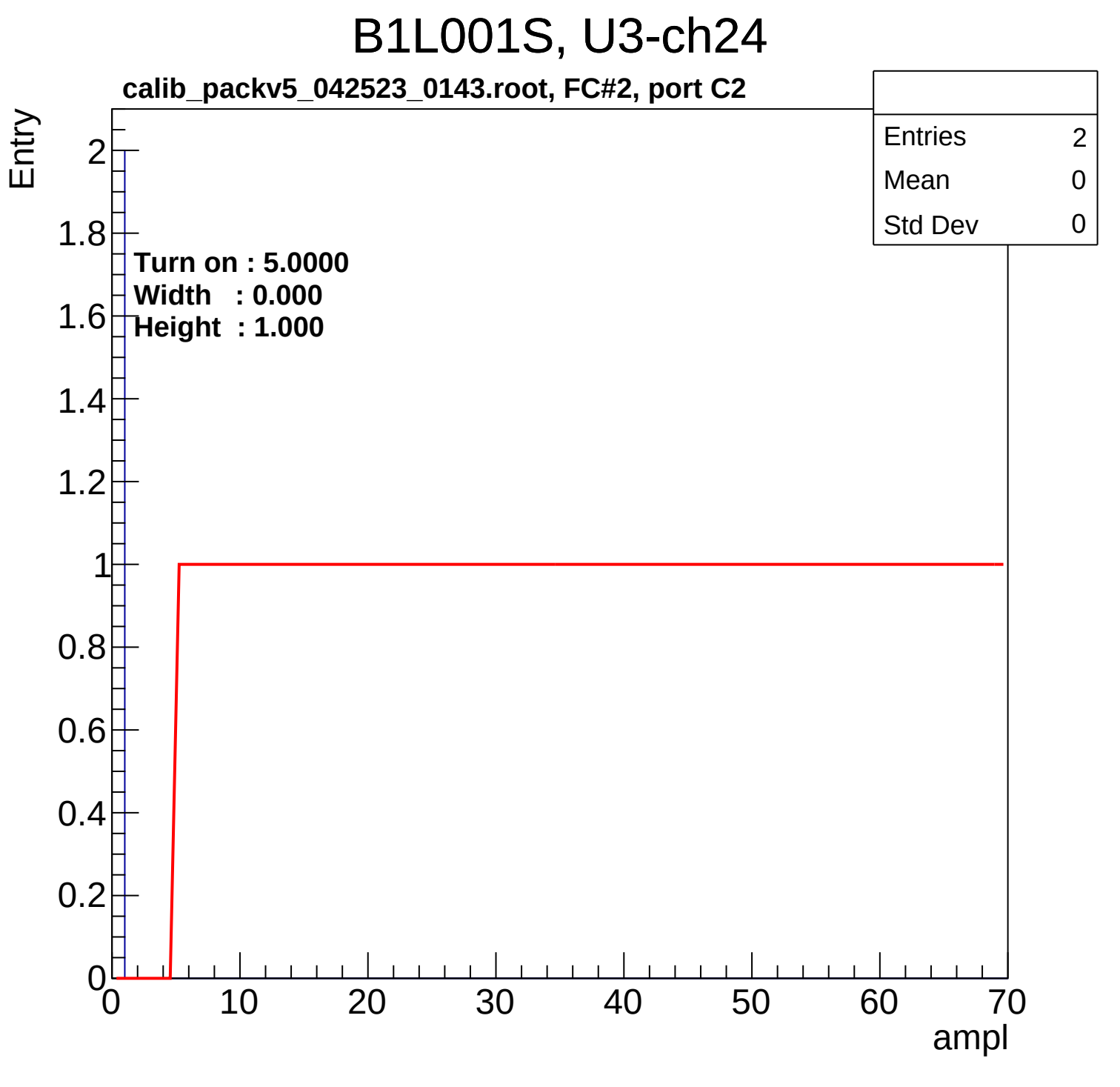
B1L001S, U3-ch24
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
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Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.2
0.4
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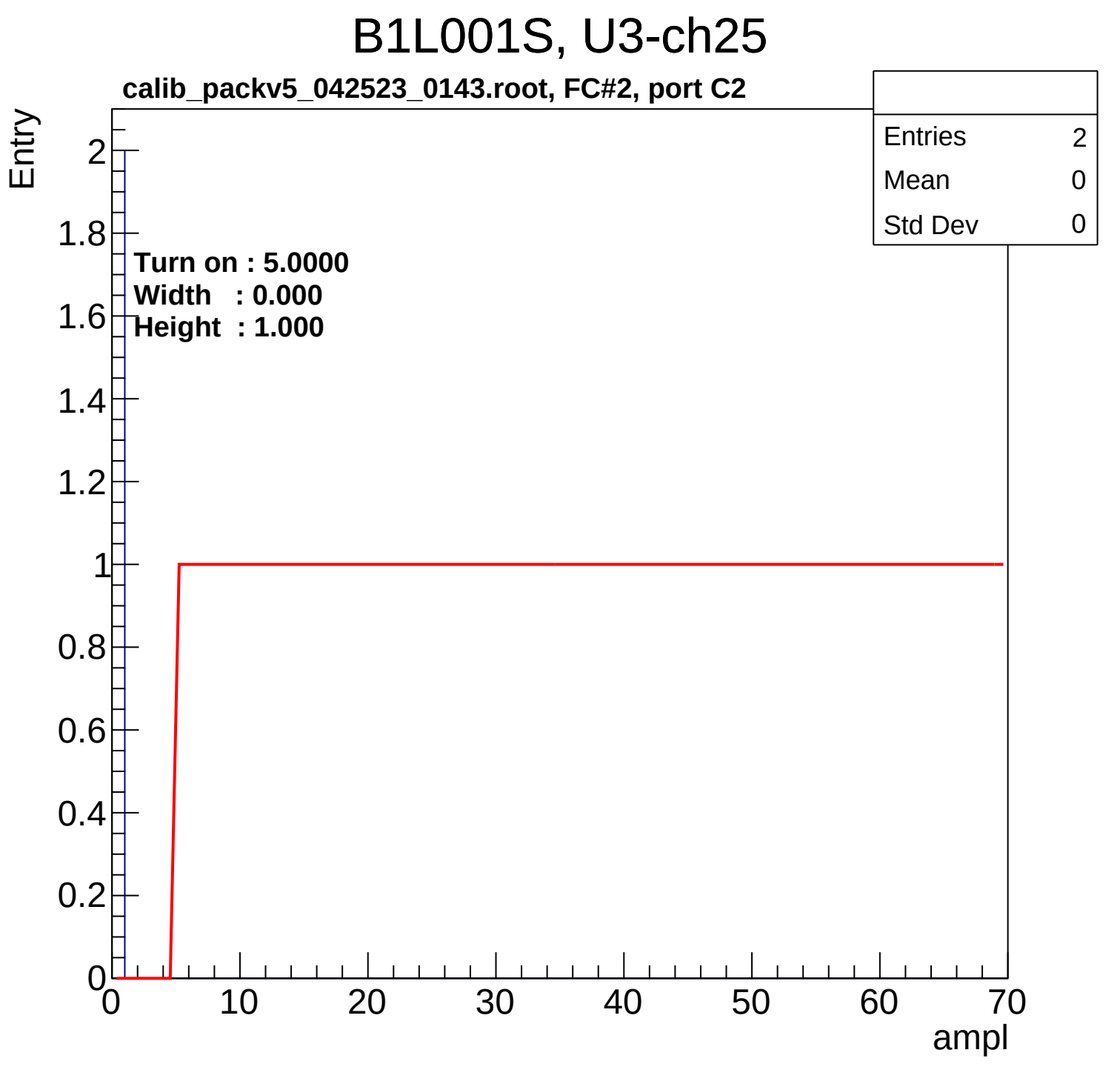
B1L001S, U3-ch25
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.2
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1.8
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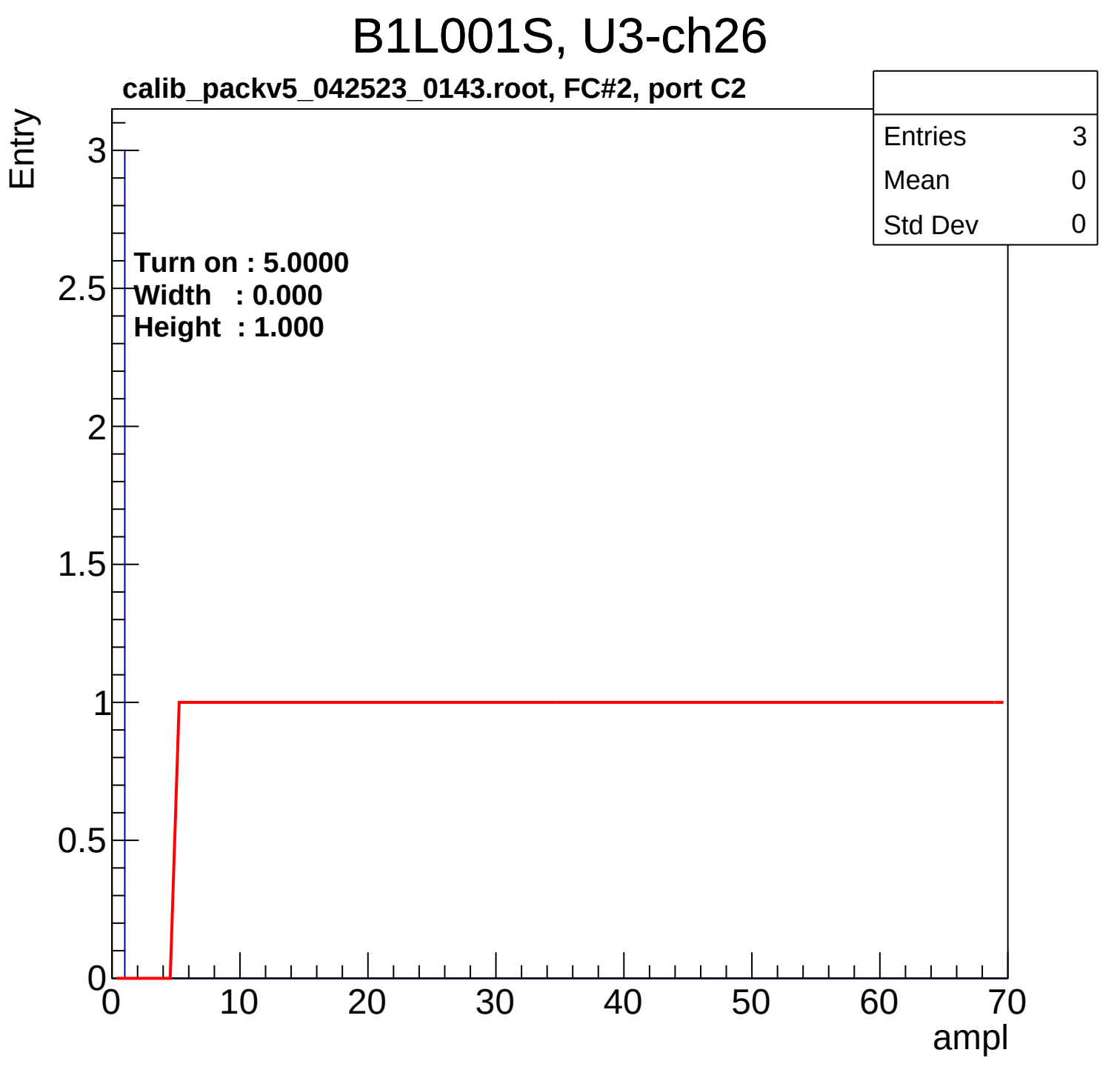
B1L001S, U3-ch26
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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1
1.5
2
2.5
3
0
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60
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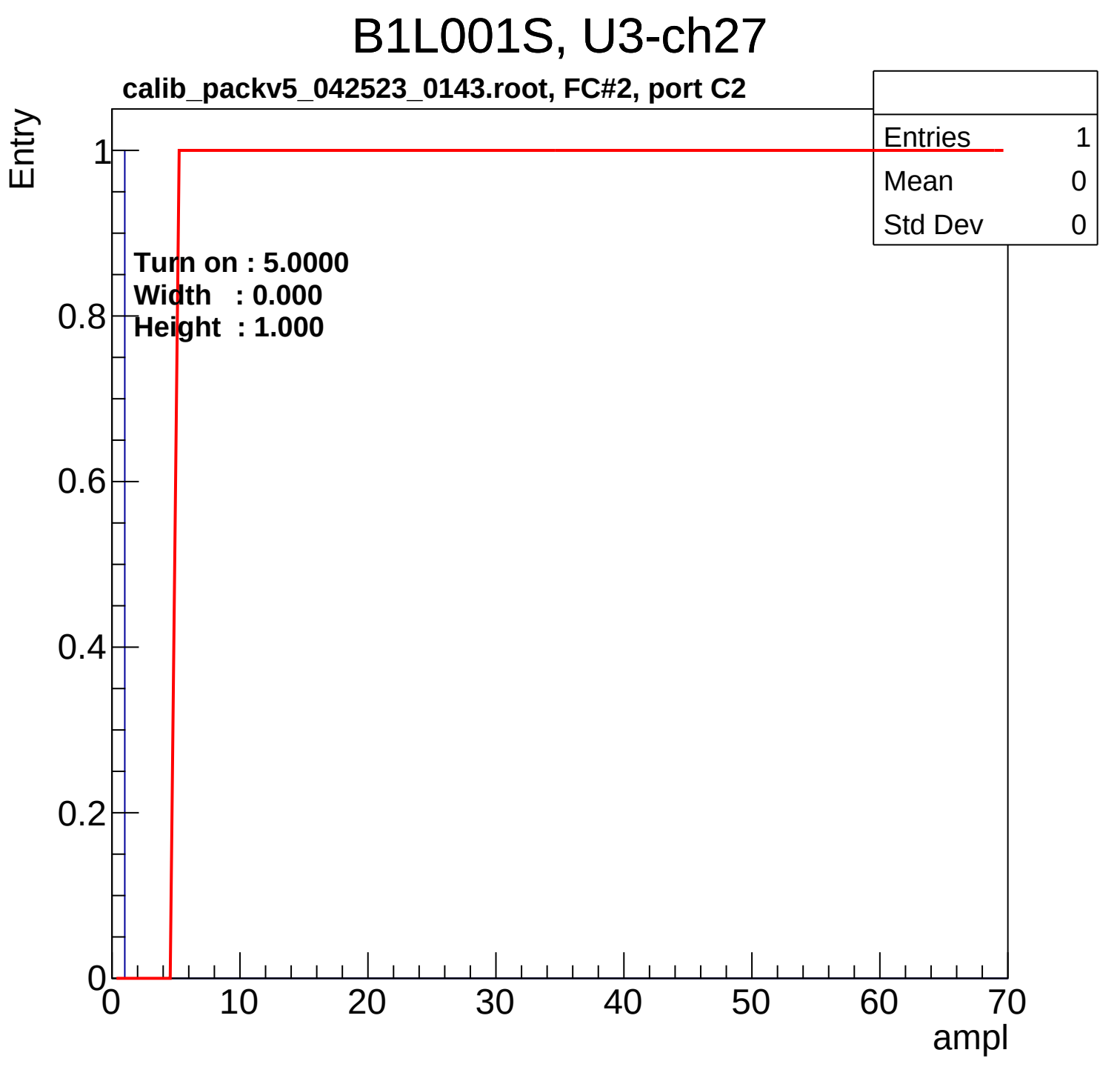
B1L001S, U3-ch27
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
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0.4
0.2
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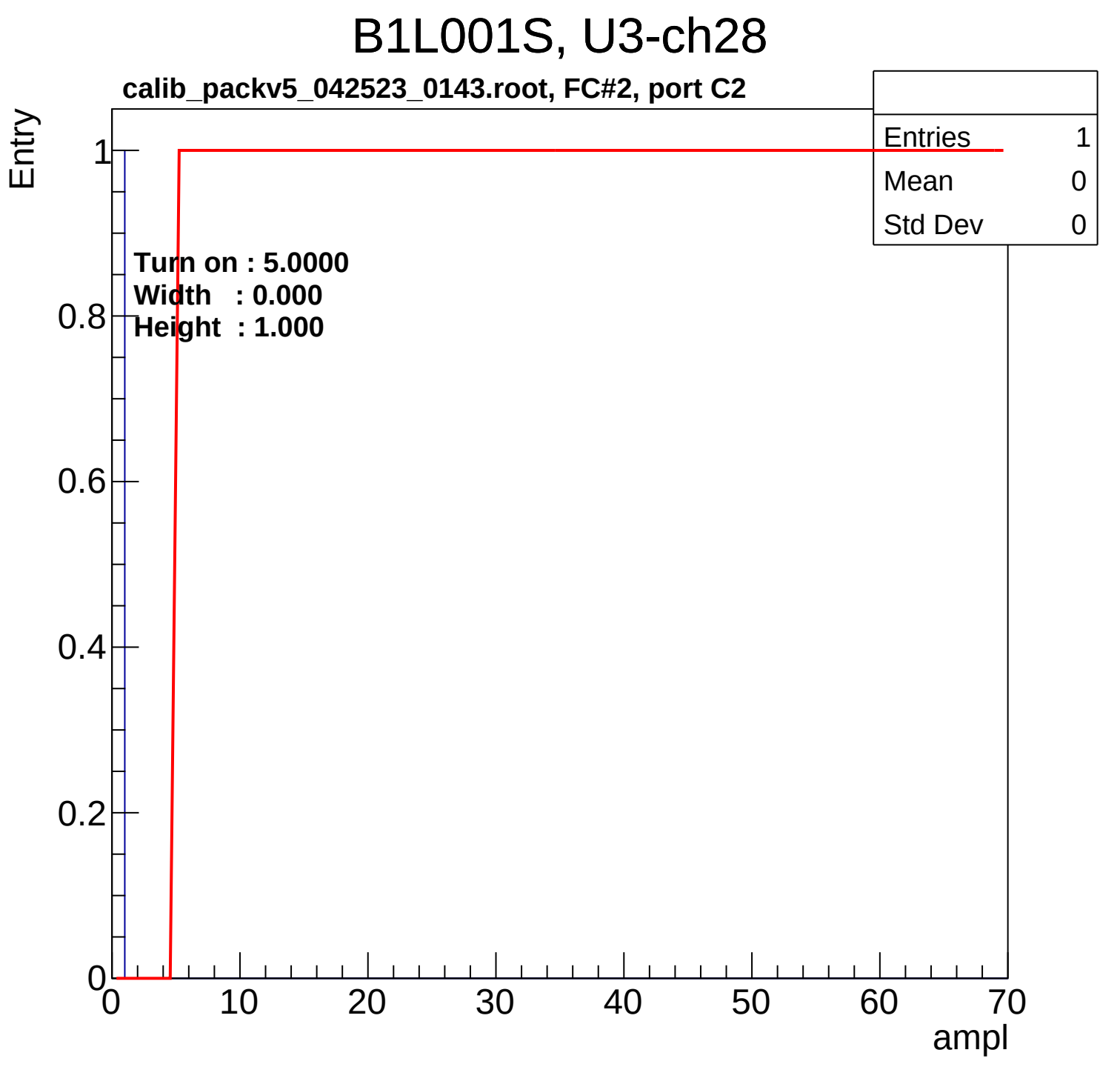
60
70
ampl


B1L001S, U3-ch28
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
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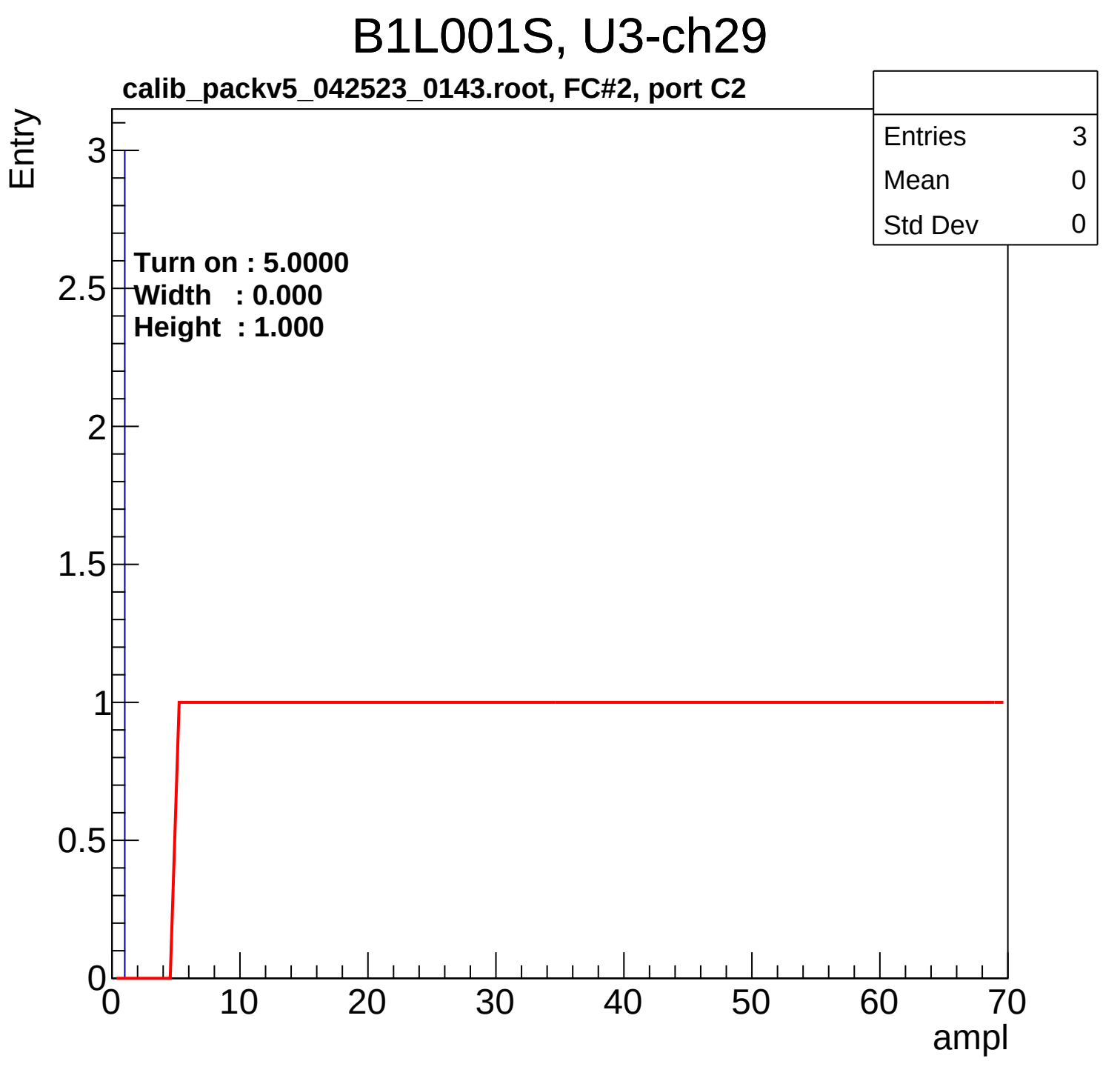
ampl


B1L001S, U3-ch29
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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1.5
2
2.5
3
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20
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60
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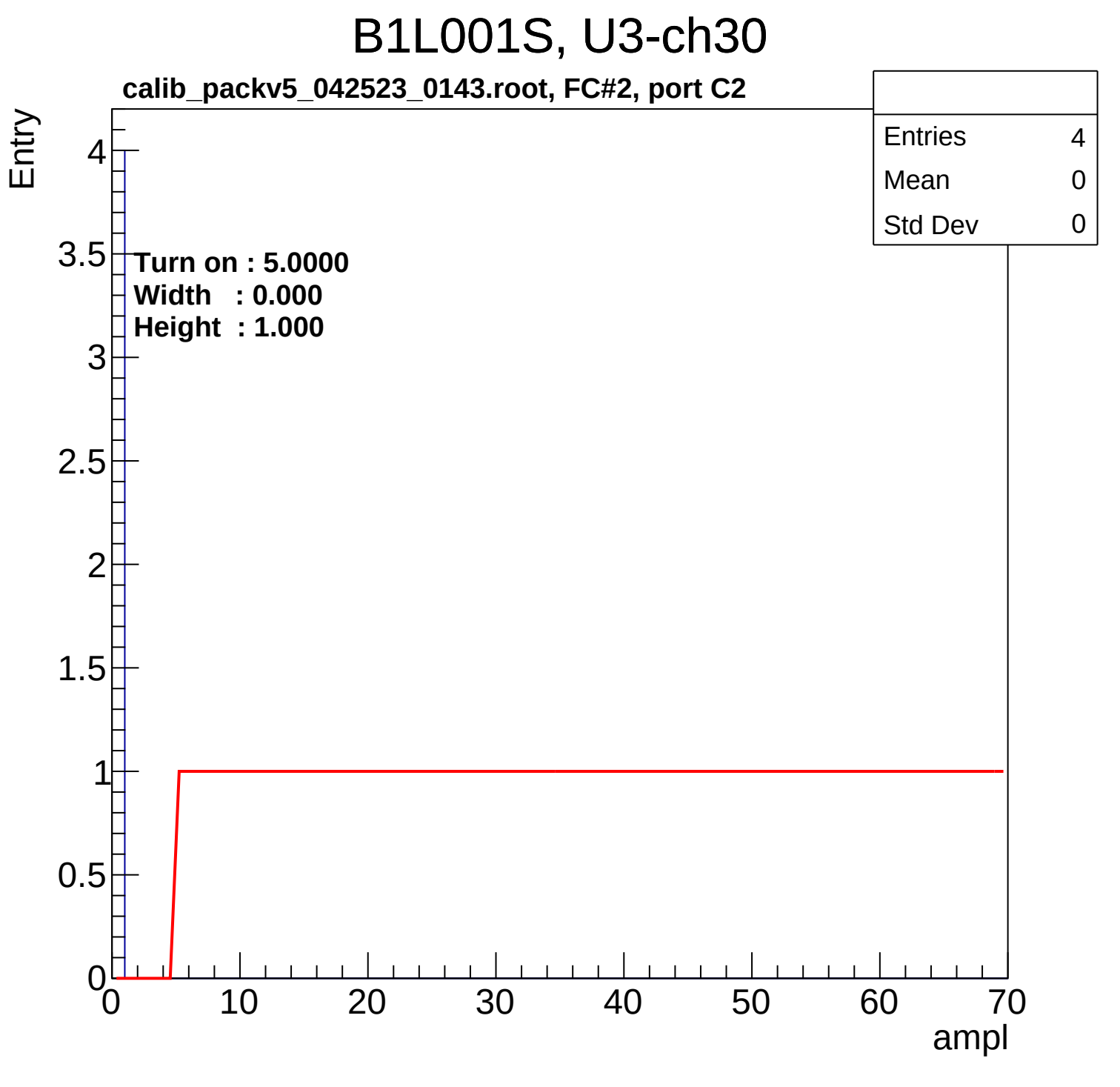
B1L001S, U3-ch30
calib_packv5_042523_0143.root, FC#2, port C2
Entries 4
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
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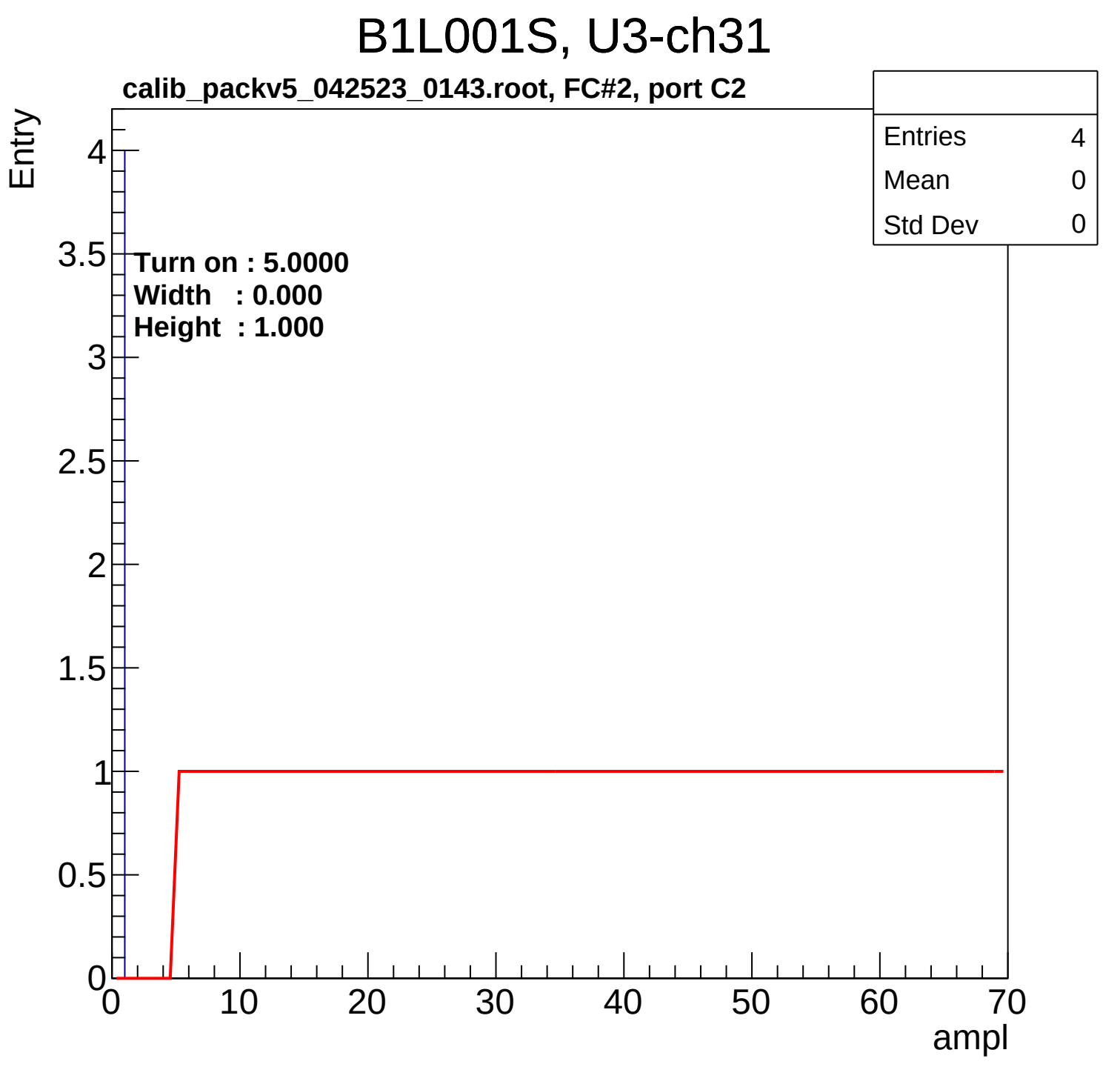
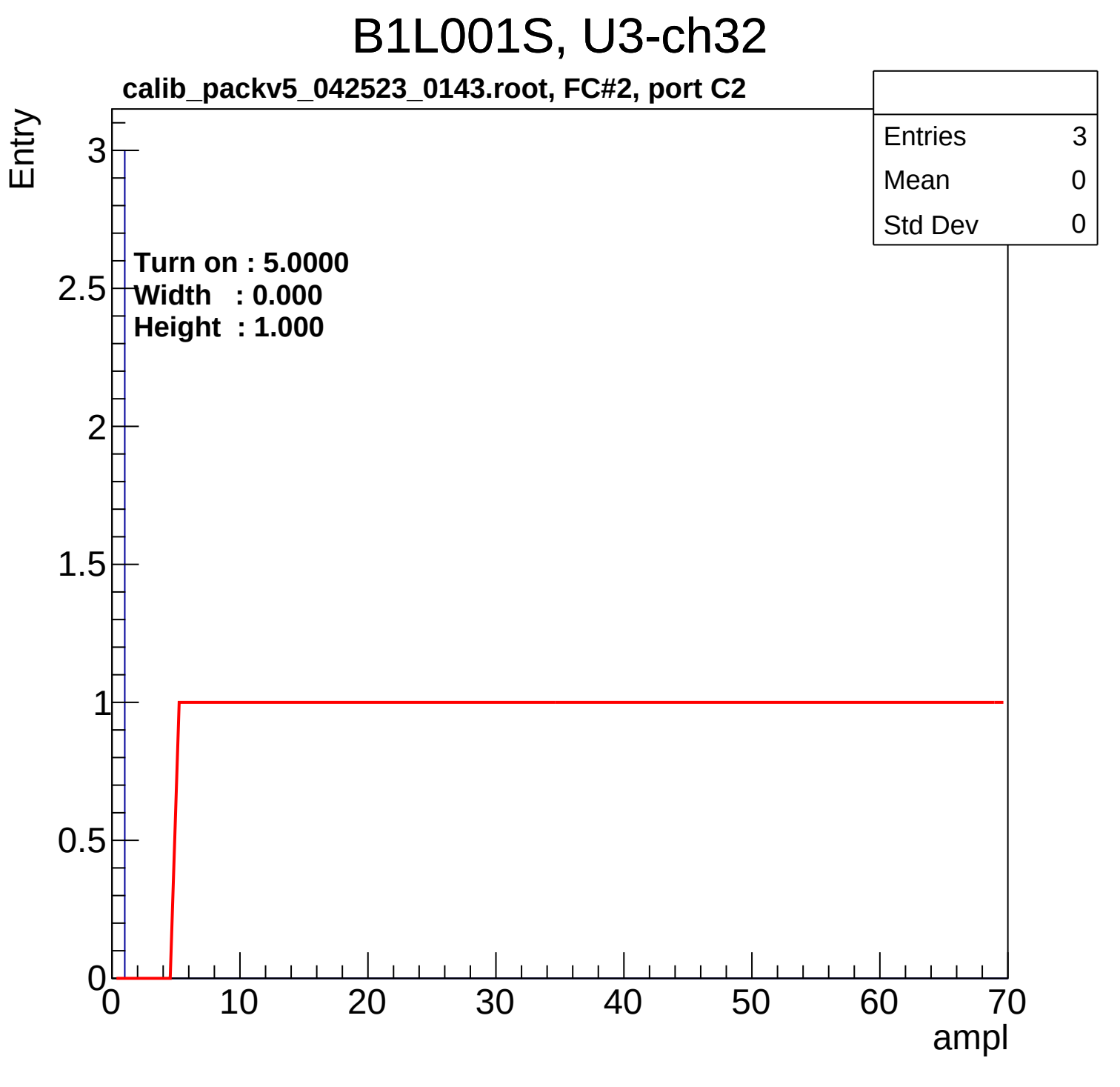
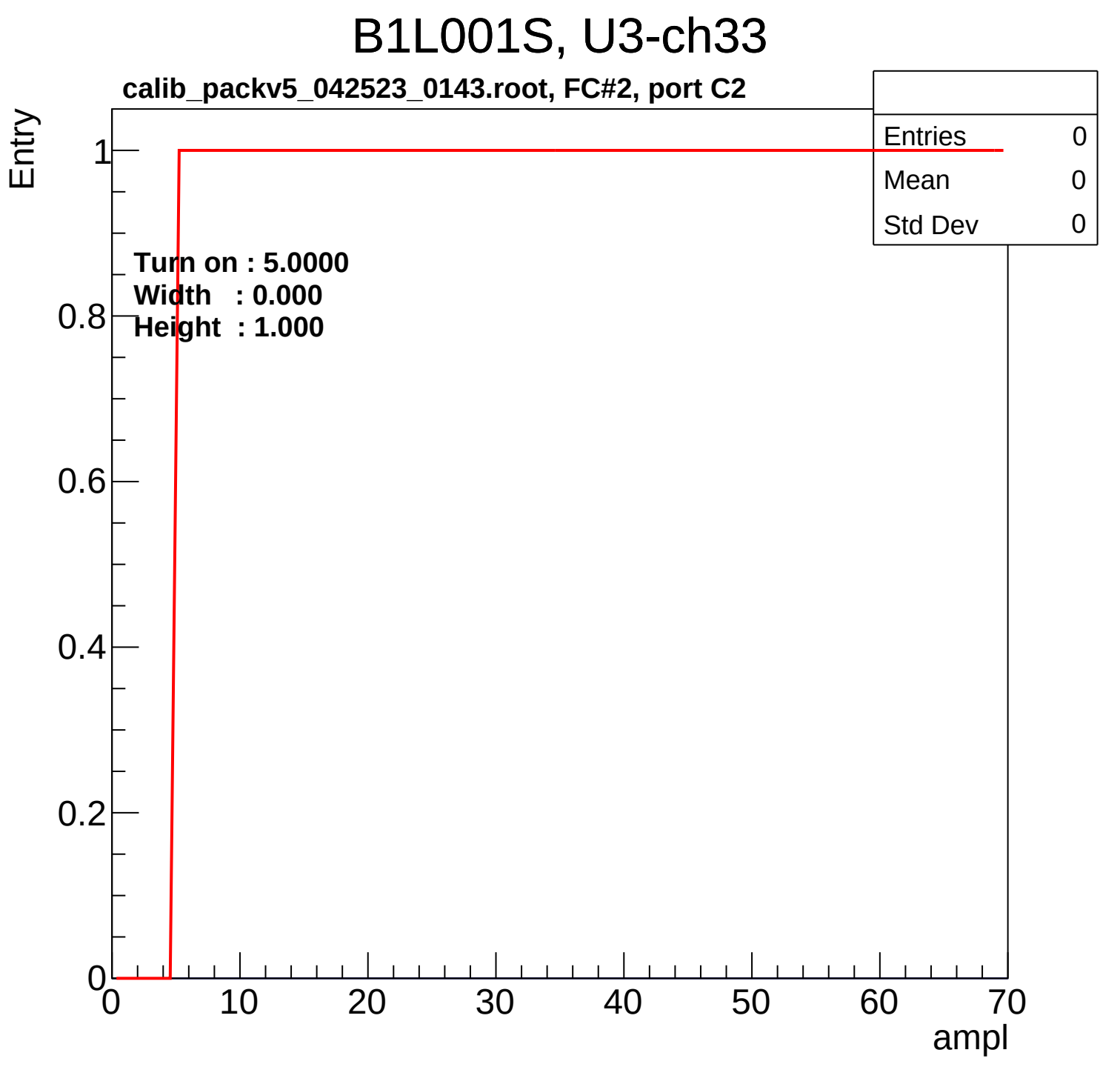
20
30
40
50
60
70


B1L001S, U3-ch31
calib_packv5_042523_0143.root, FC#2, port C2
Entries 4
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L001S, U3-ch32
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L001S, U3-ch33
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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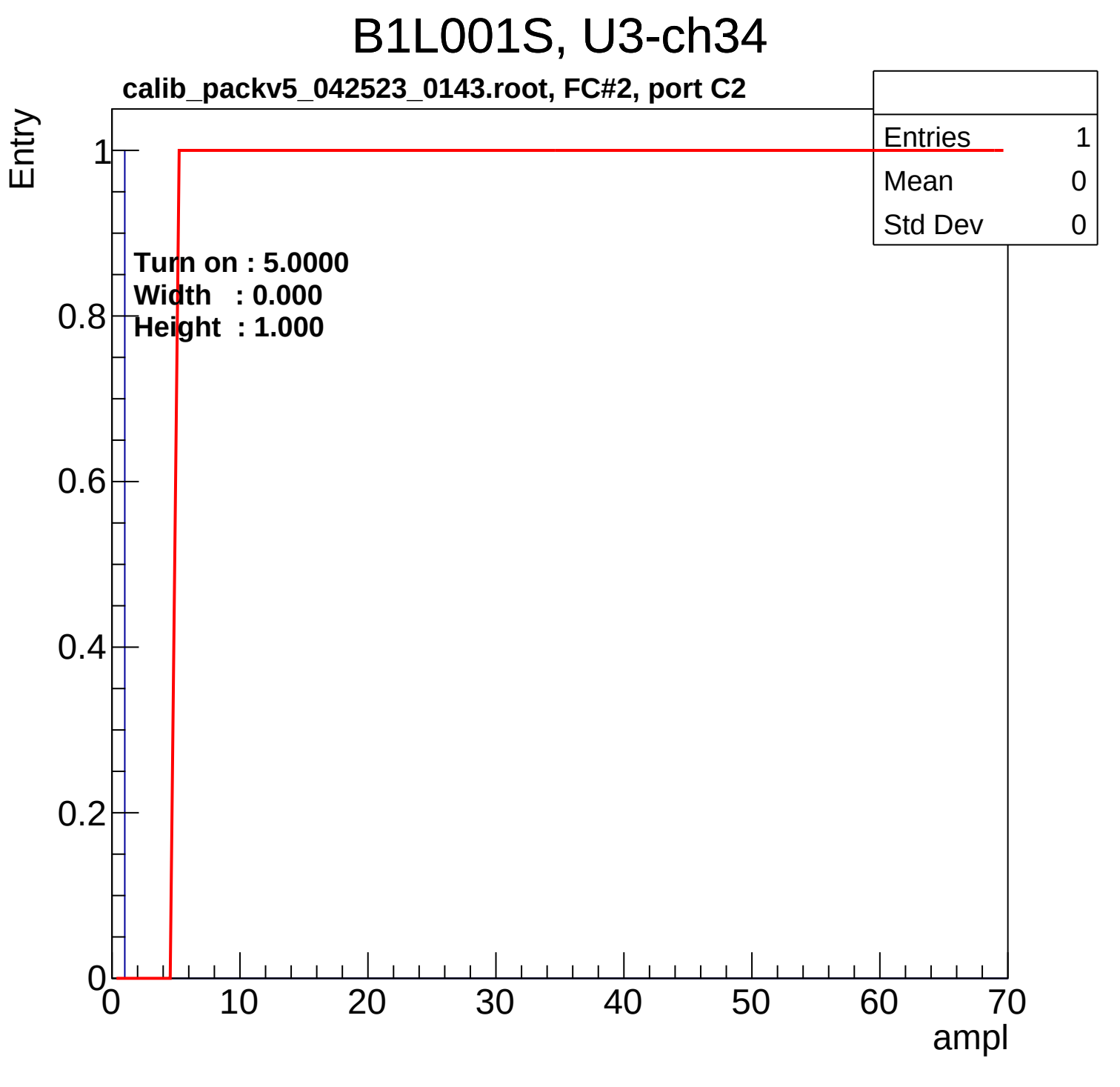
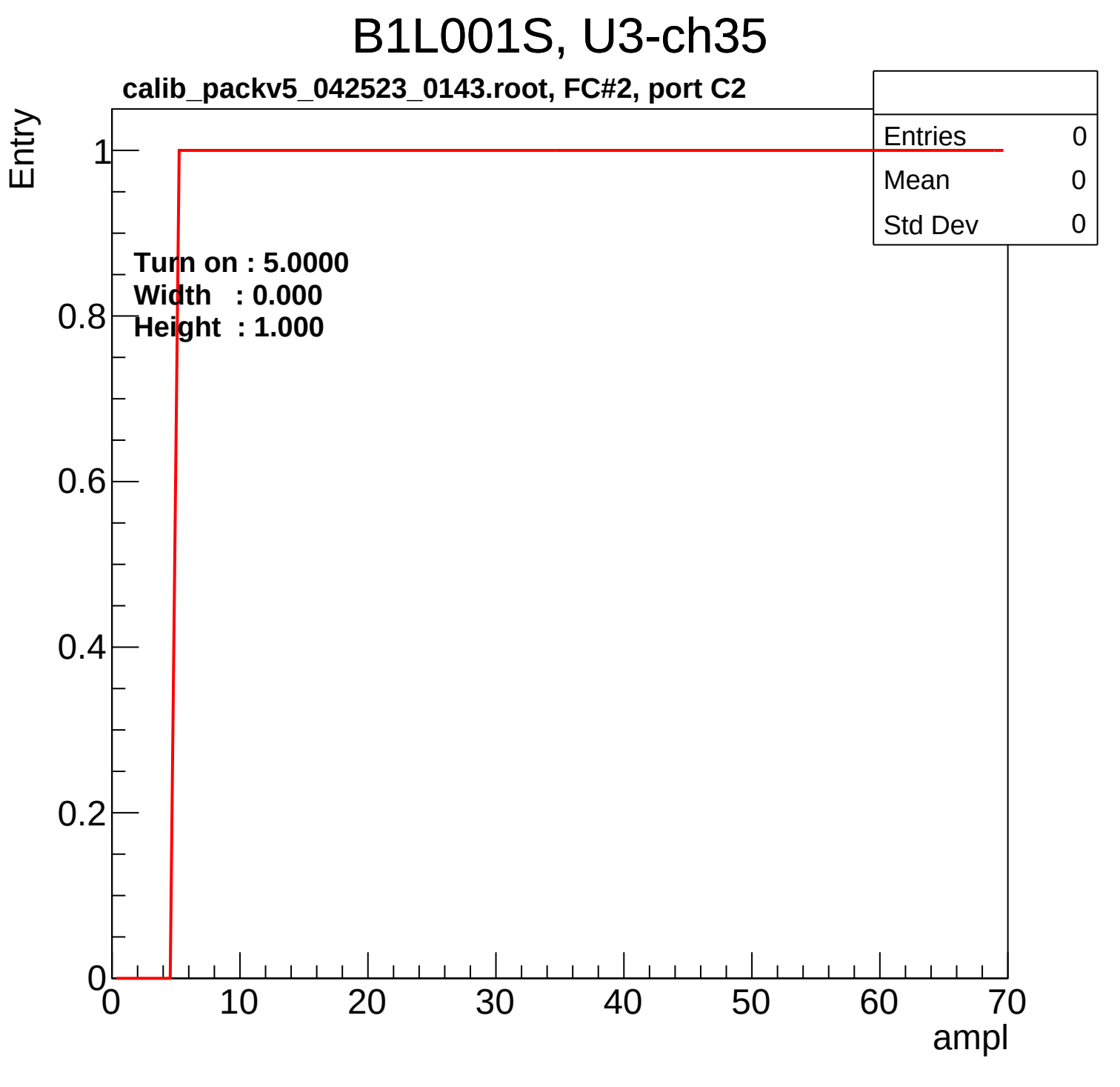
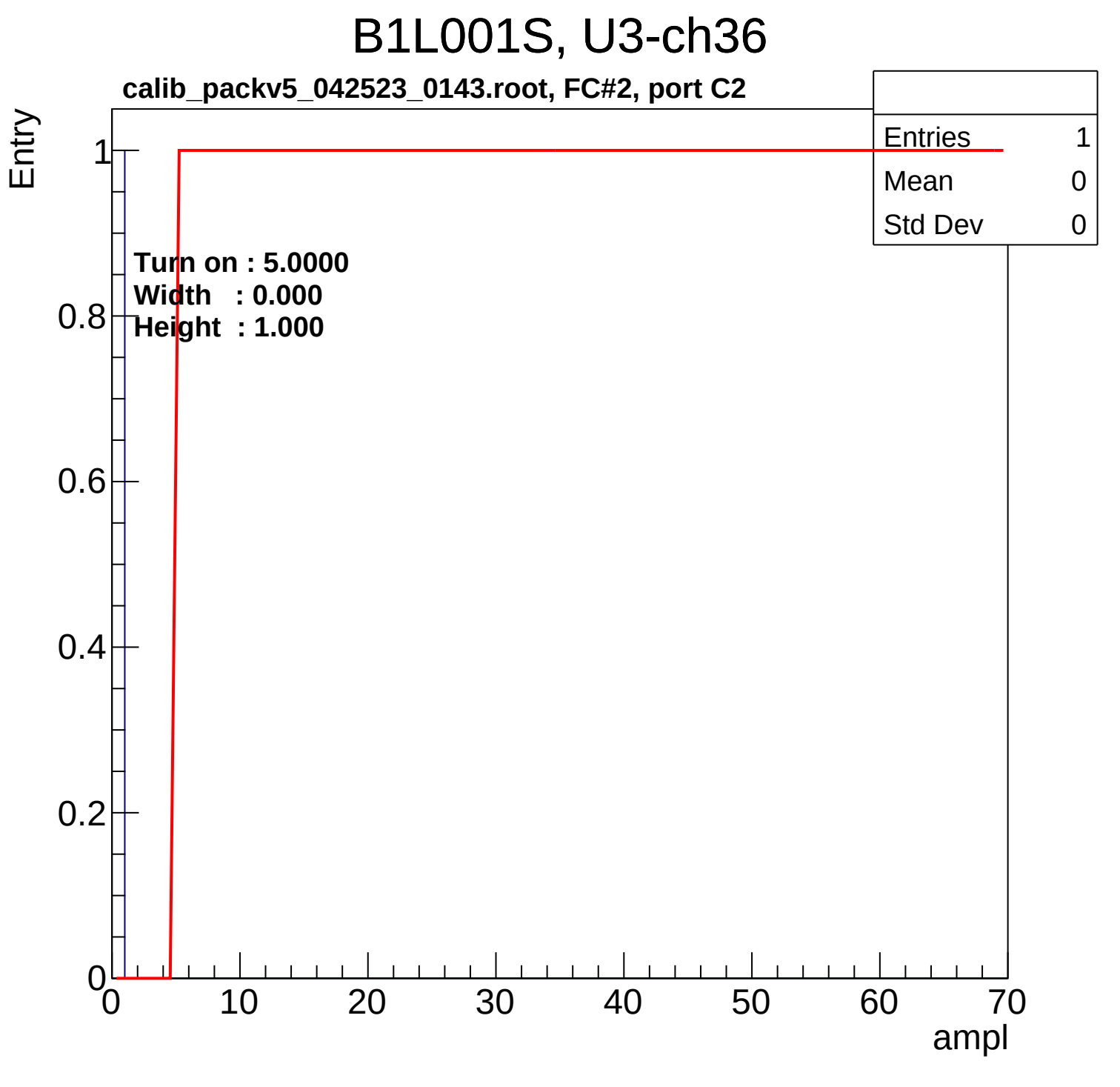
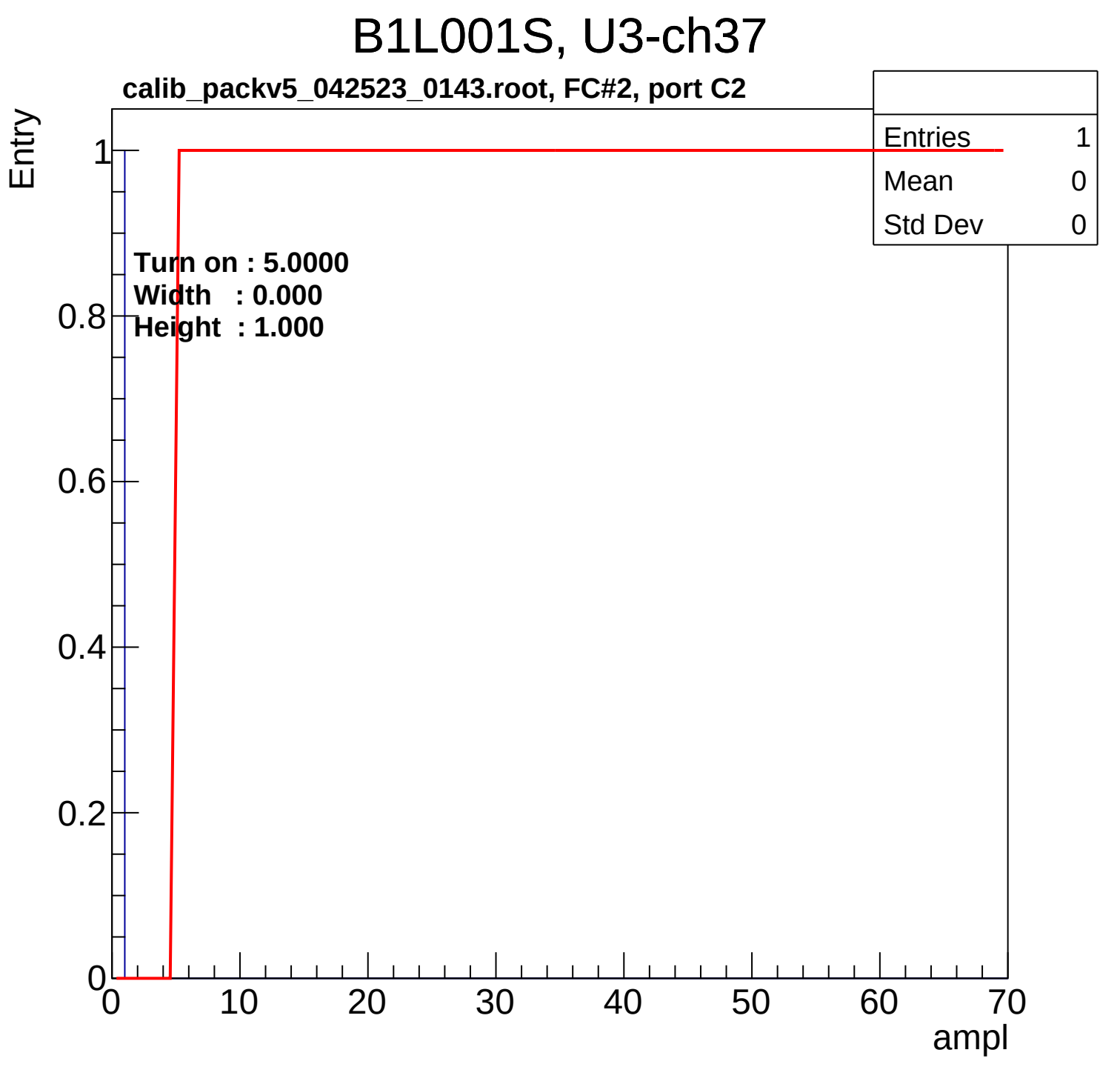
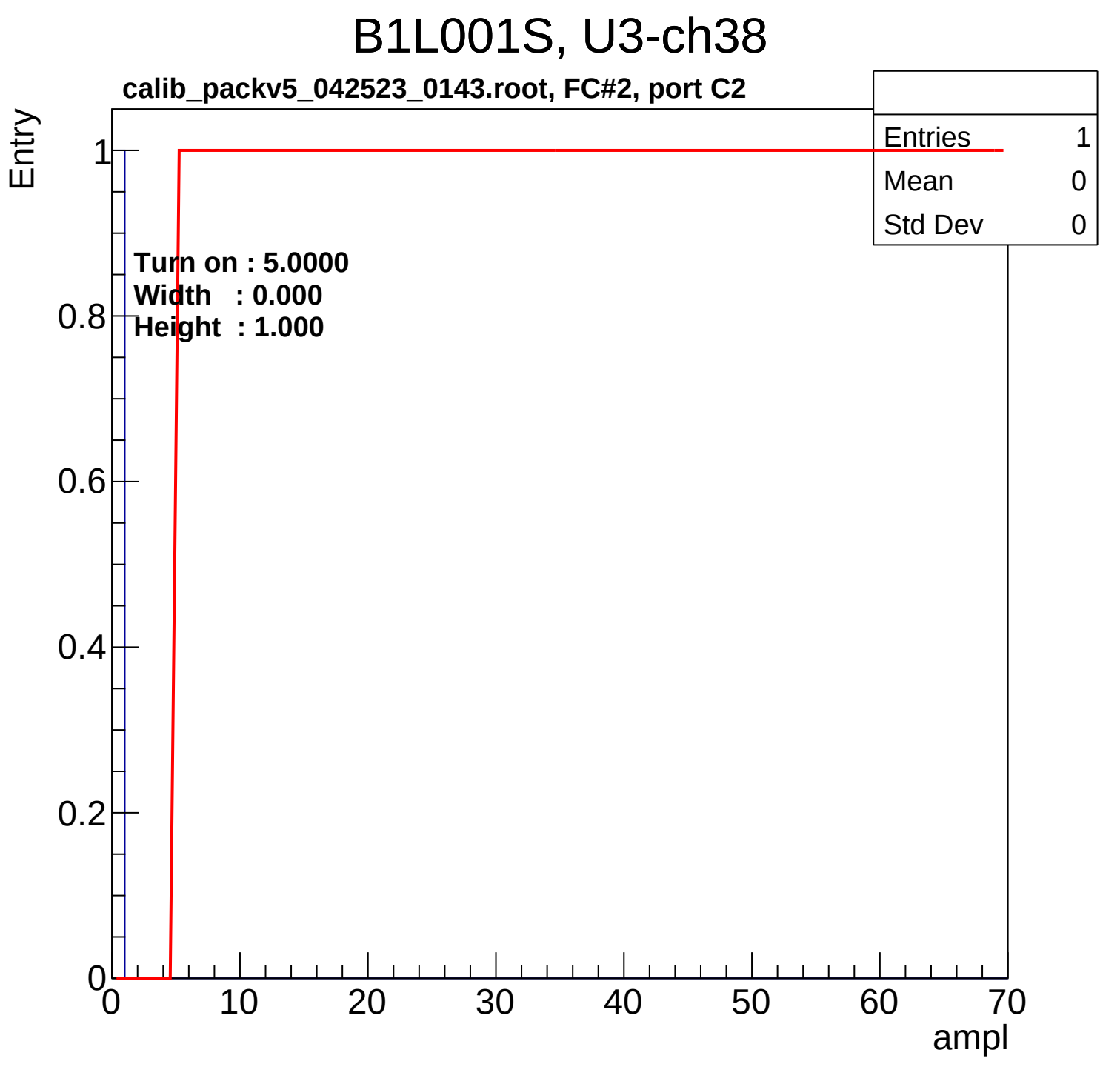
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

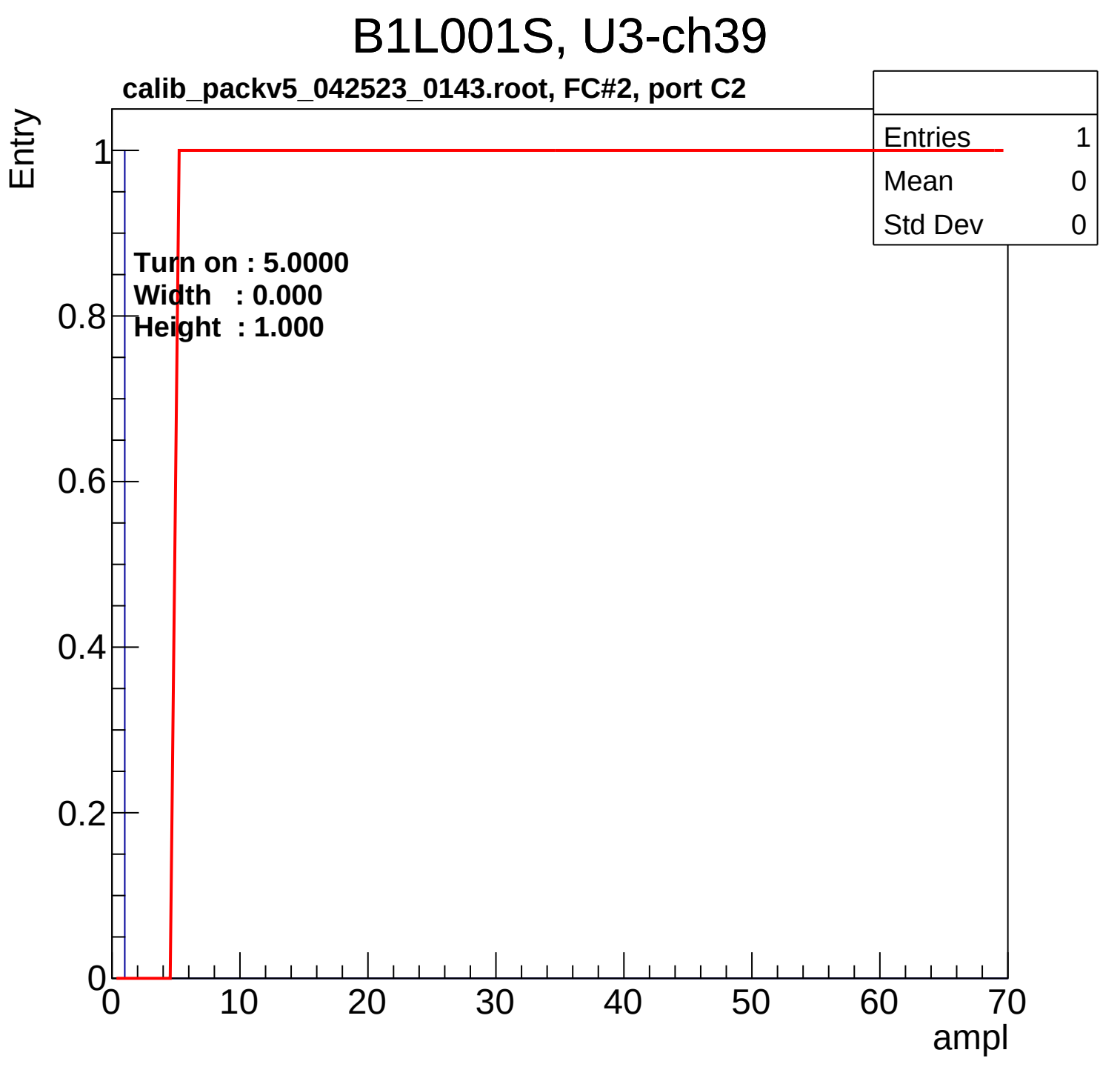

B1L001S, U3-ch34
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

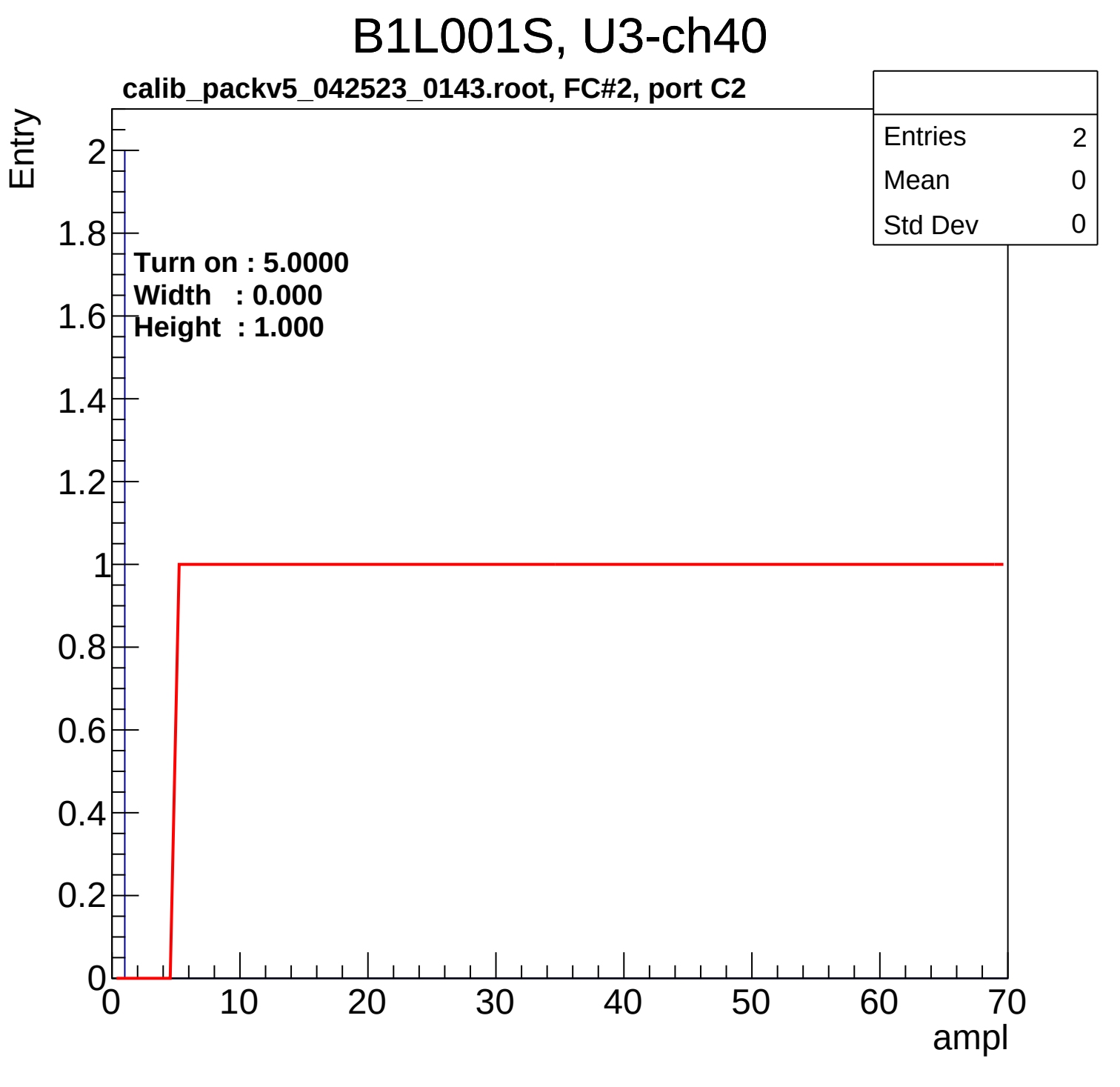

B1L001S, U3-ch35
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

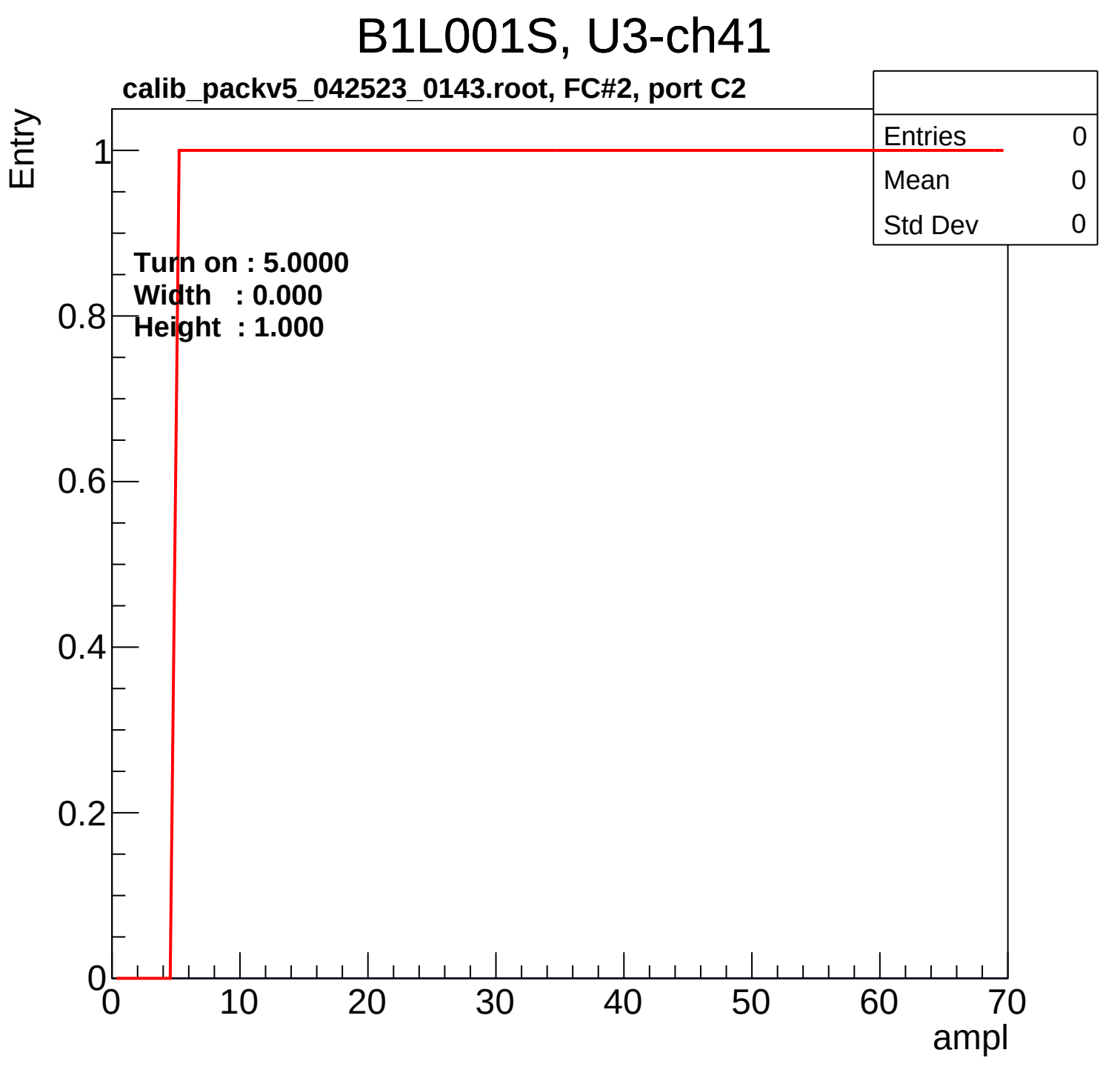

B1L001S, U3-ch36
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

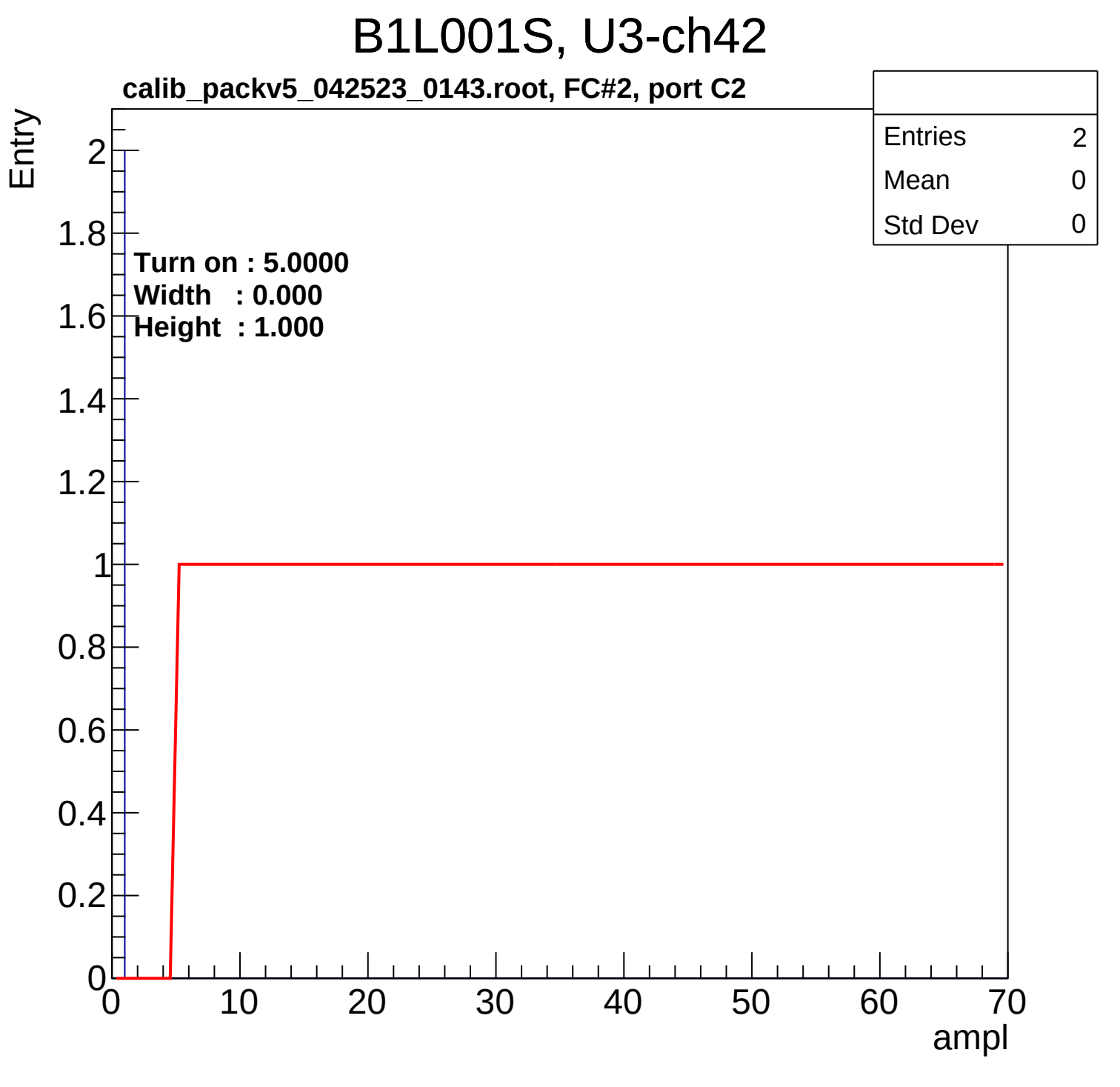

B1L001S, U3-ch37
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

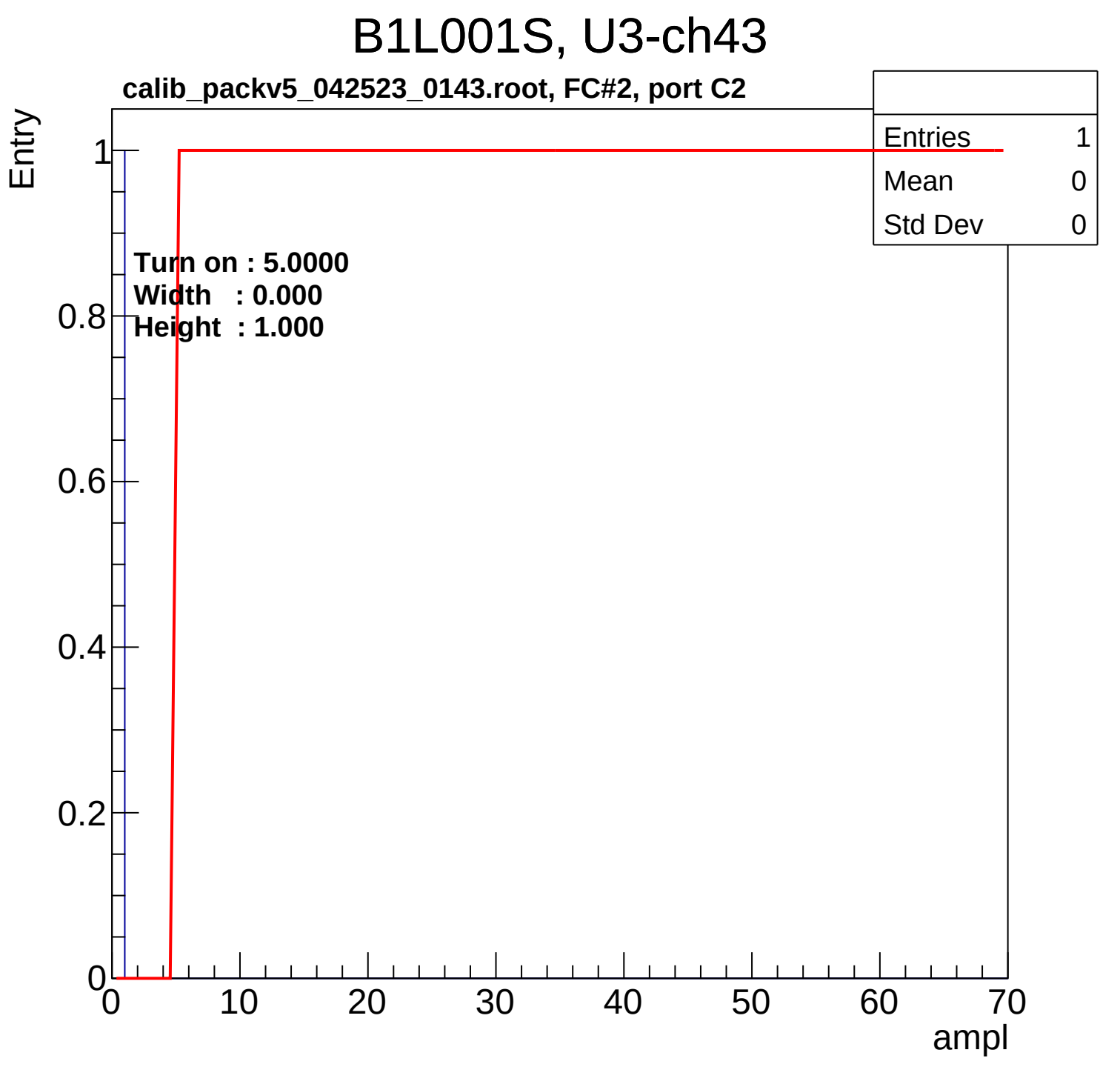

B1L001S, U3-ch38
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

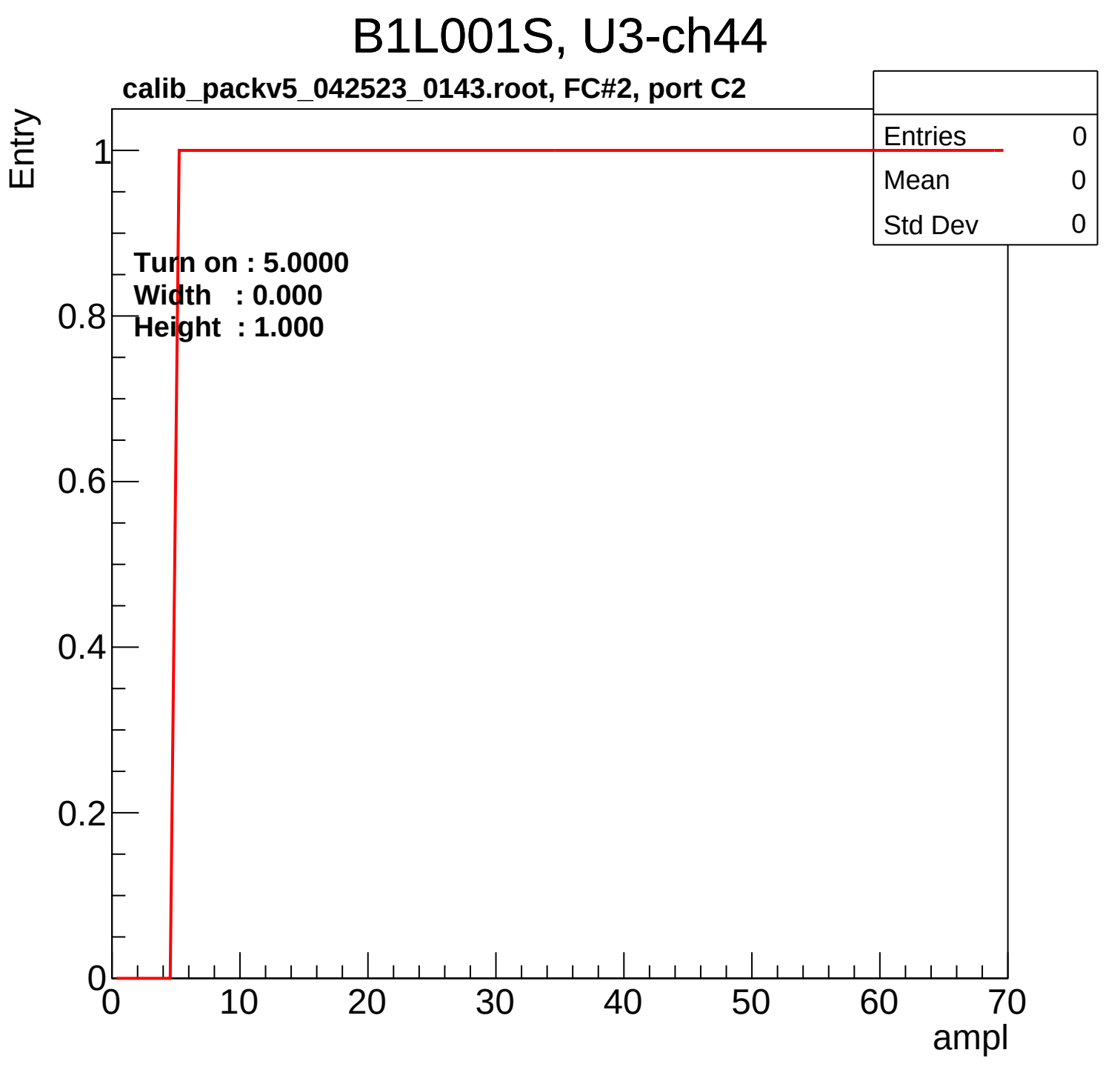

B1L001S, U3-ch39
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

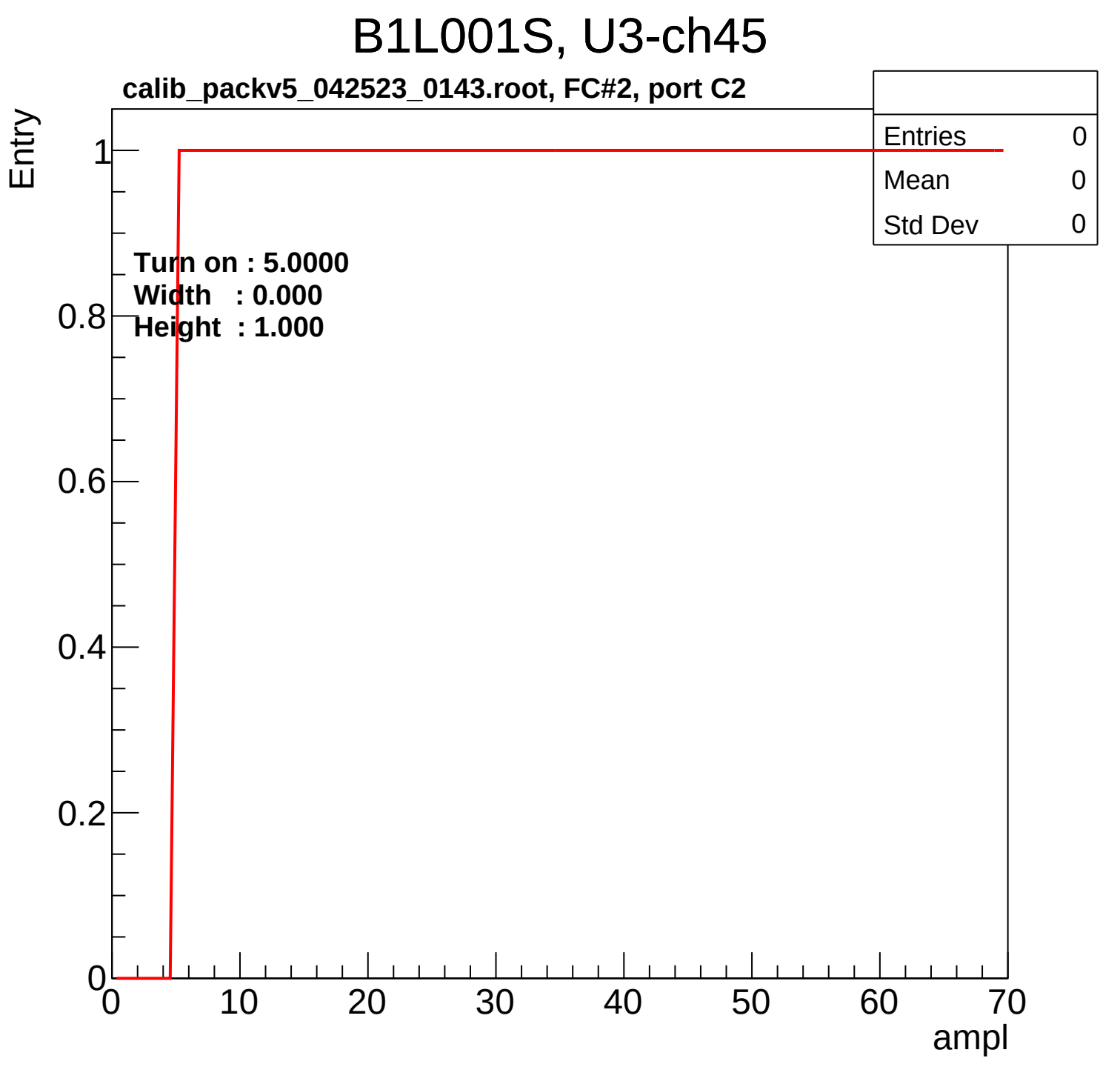

B1L001S, U3-ch40
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

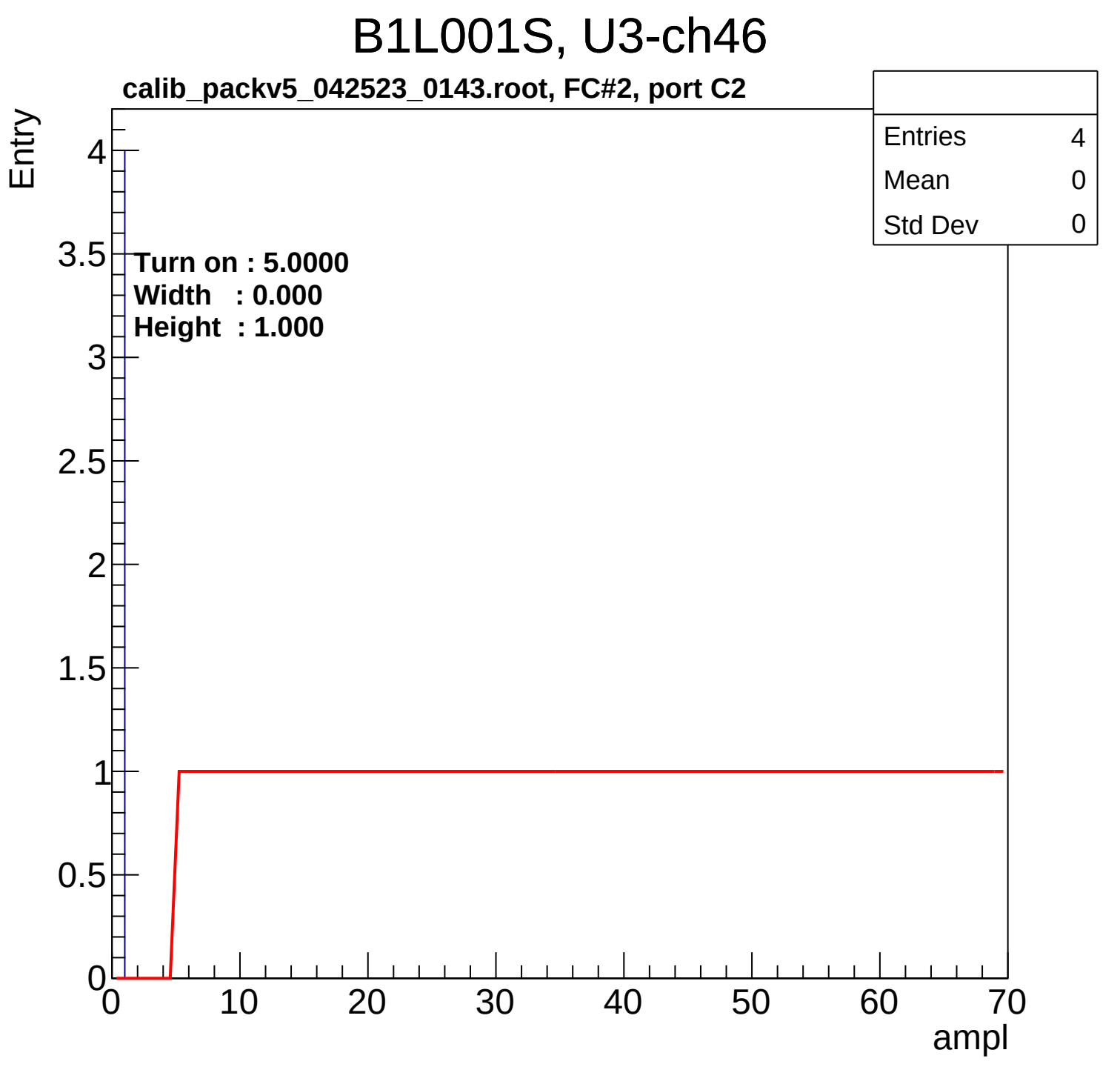

B1L001S, U3-ch41
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

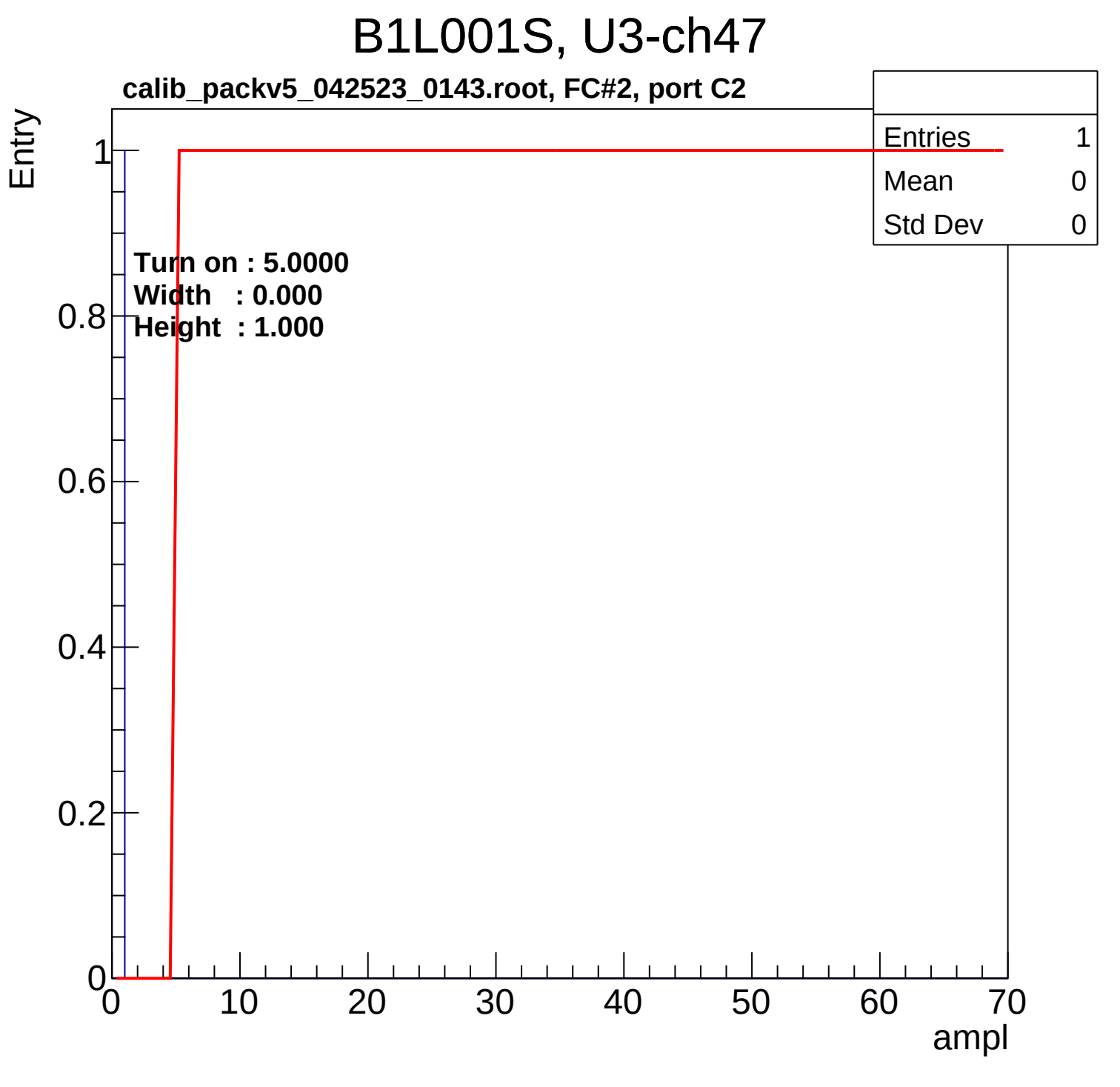

B1L001S, U3-ch42
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

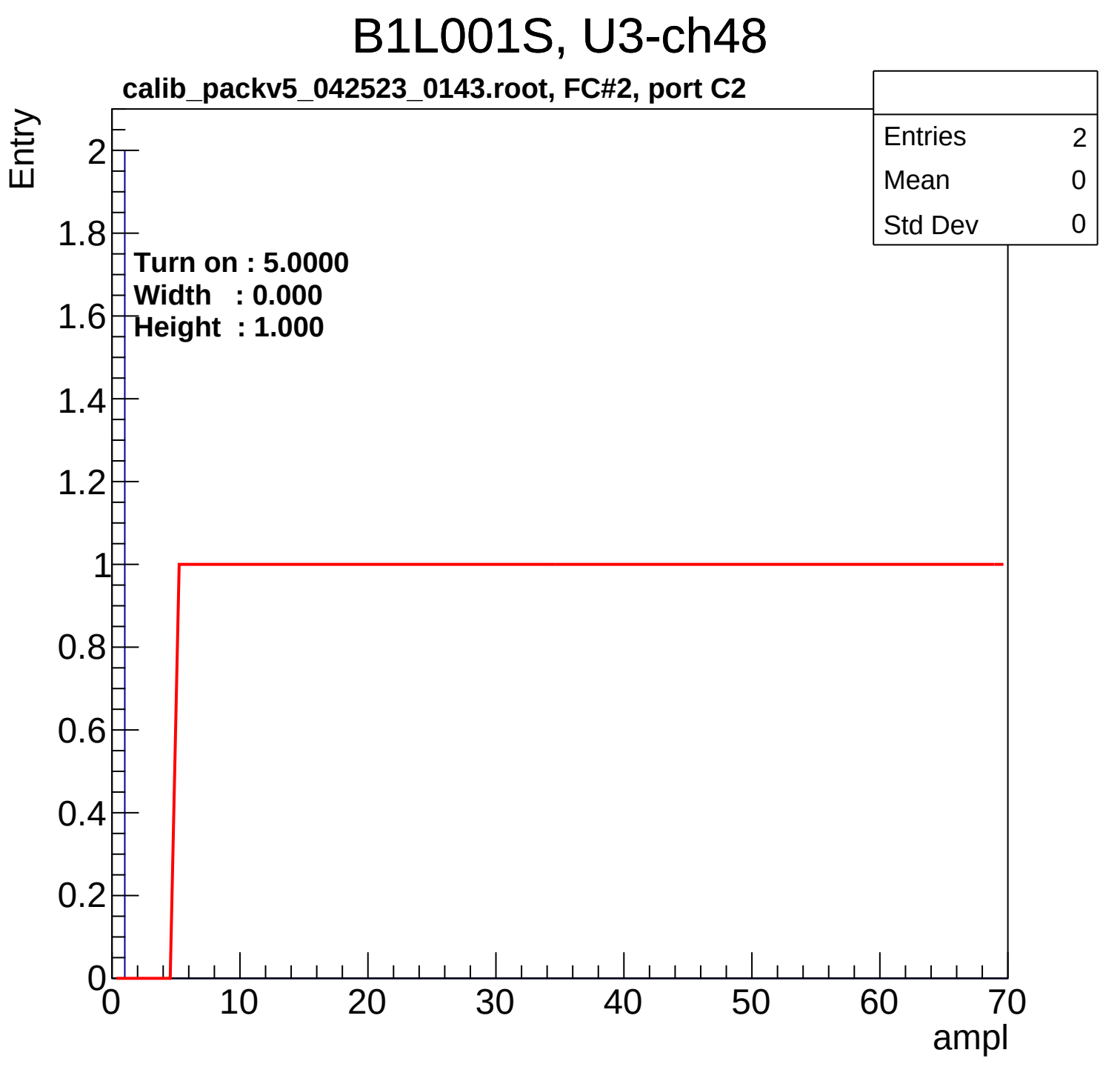

B1L001S, U3-ch43
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

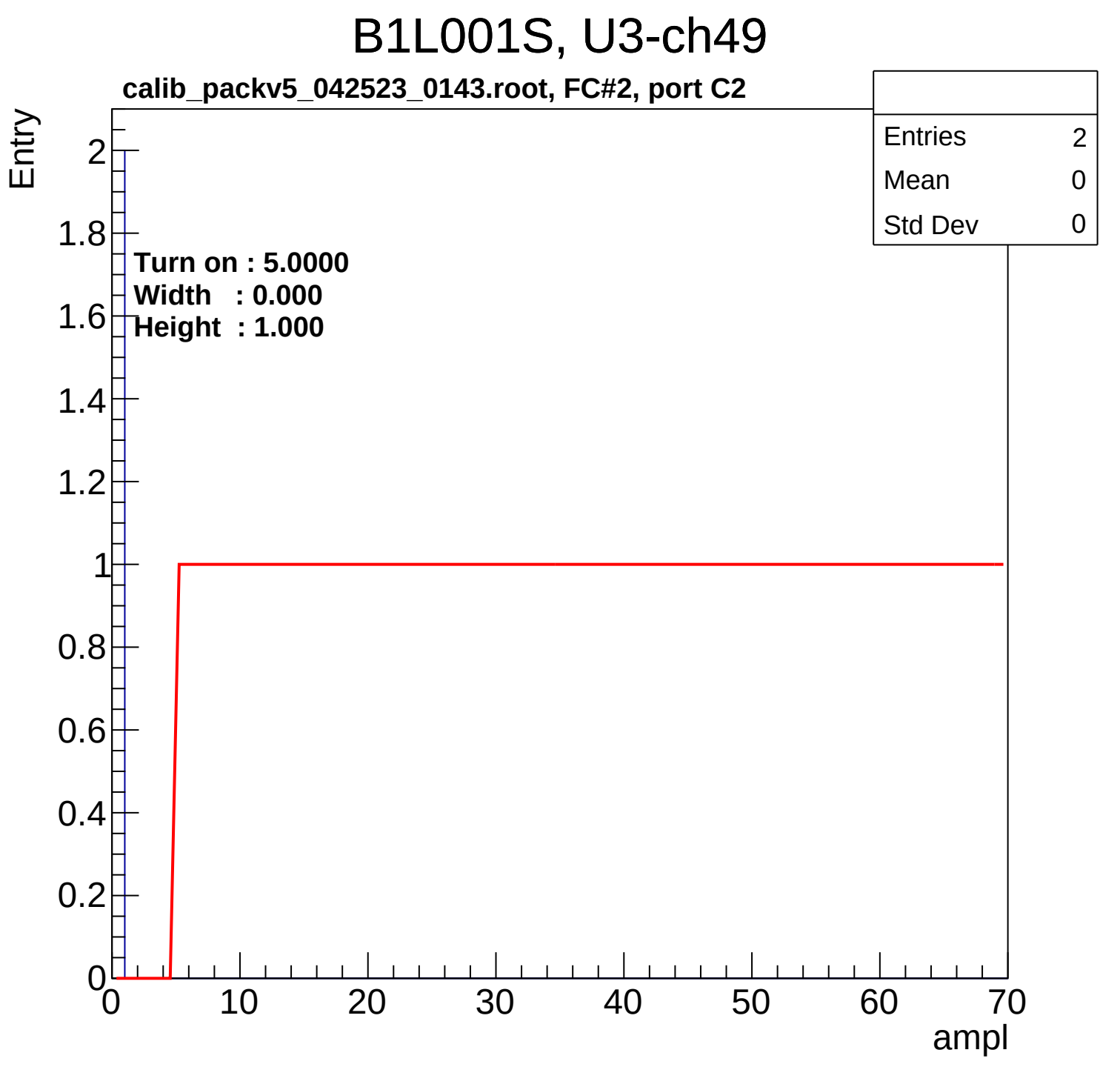

B1L001S, U3-ch44
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

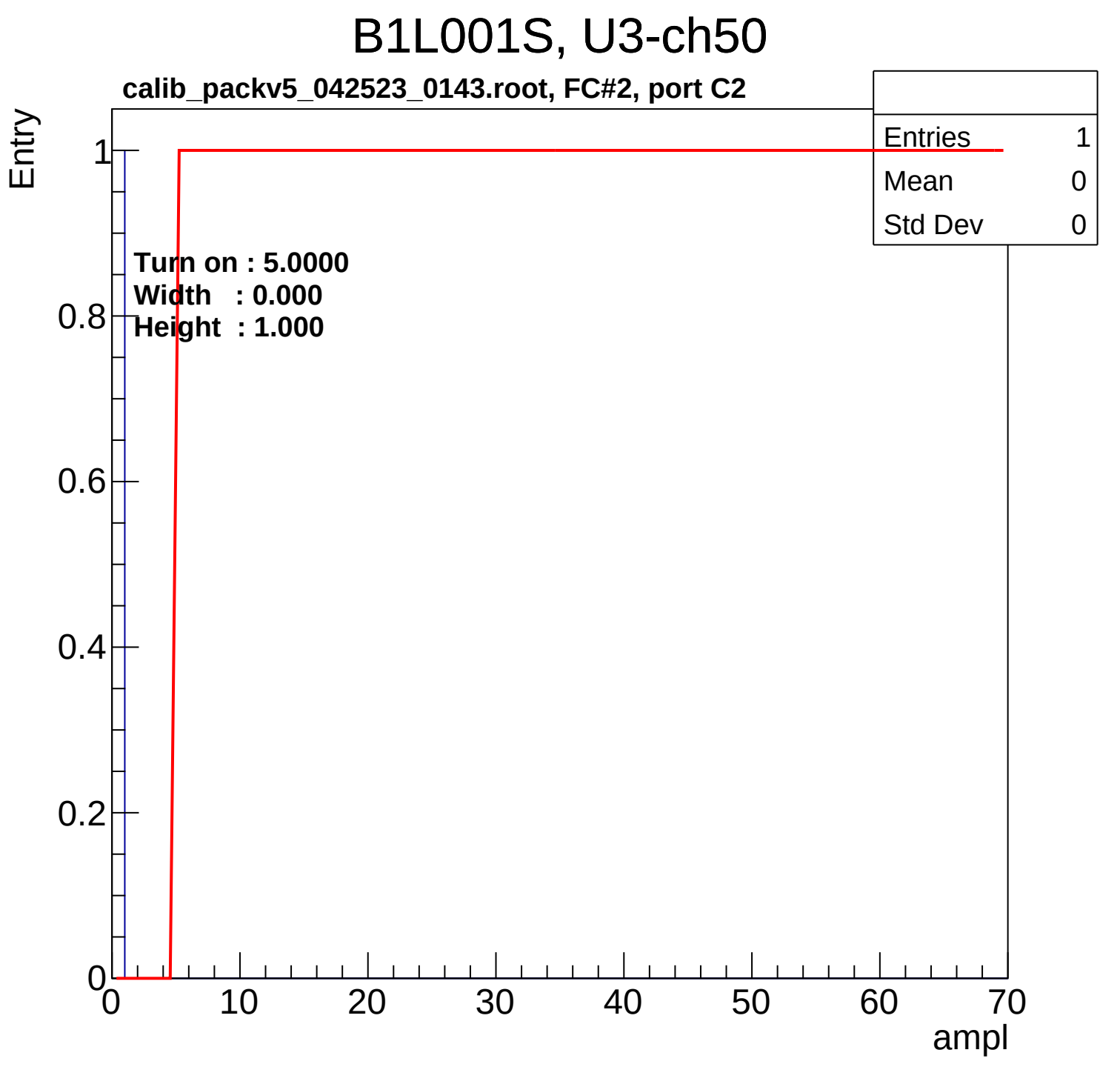

B1L001S, U3-ch45
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

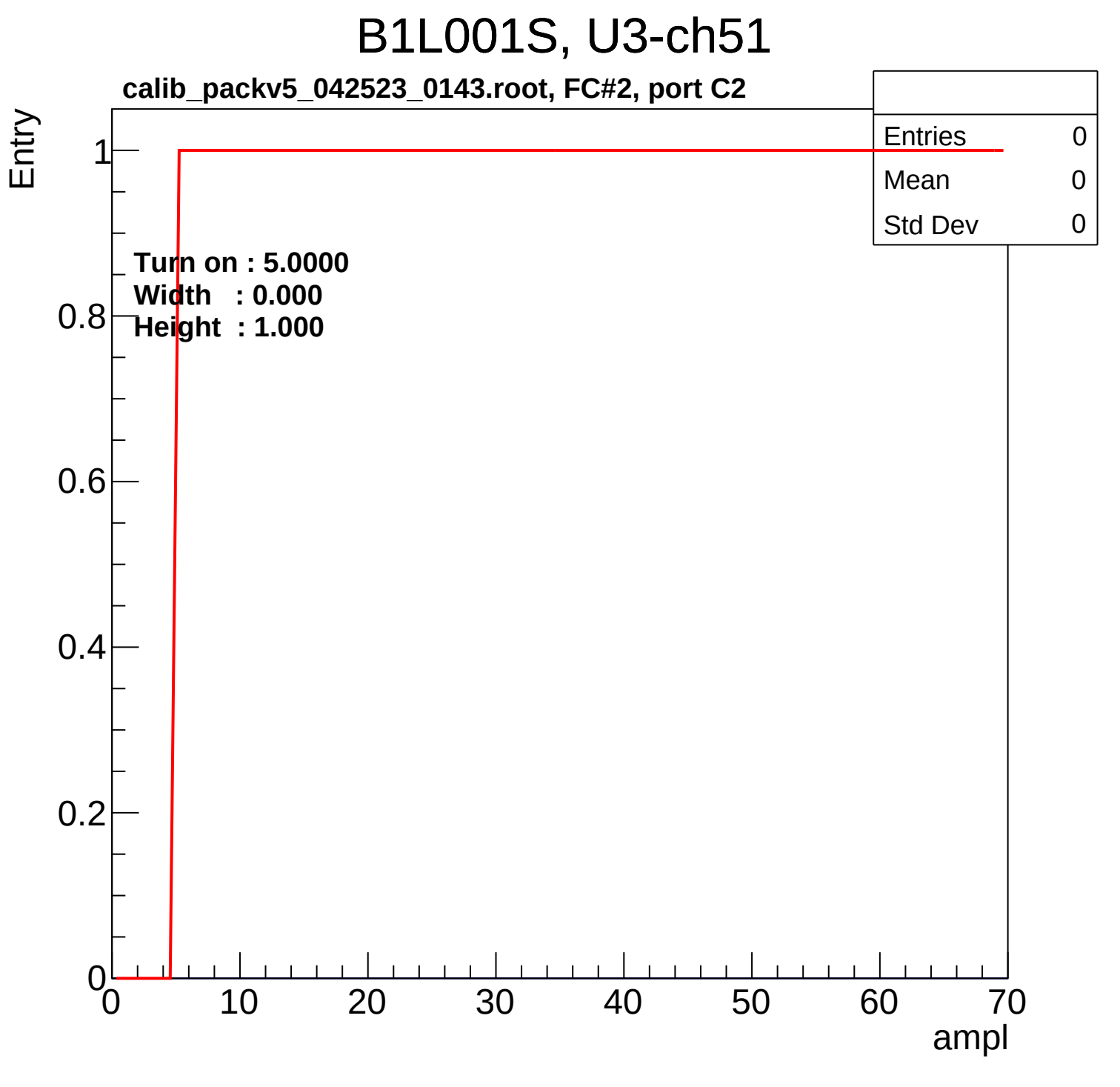

B1L001S, U3-ch46
calib_packv5_042523_0143.root, FC#2, port C2
Entries 4
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

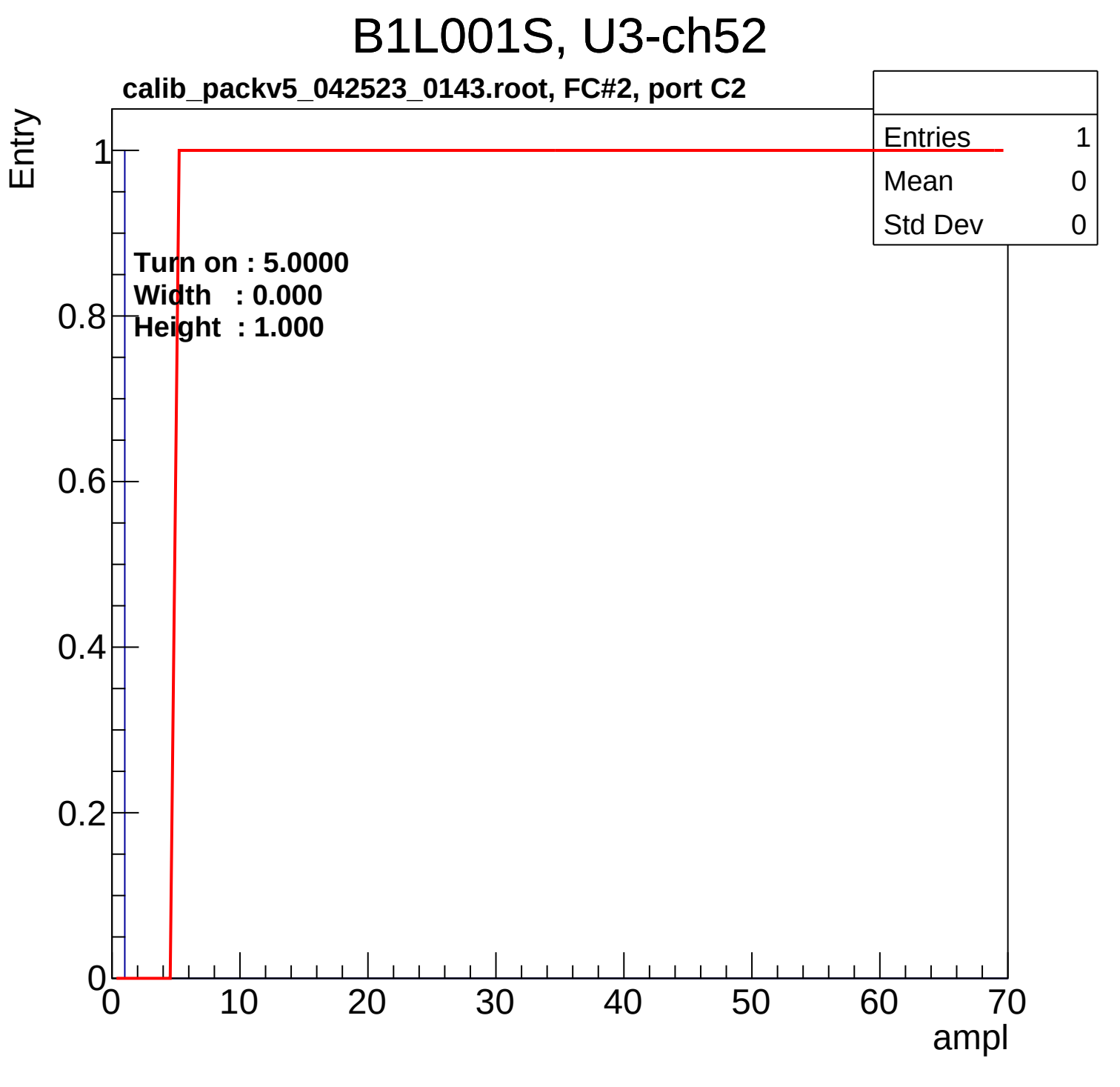

B1L001S, U3-ch47
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

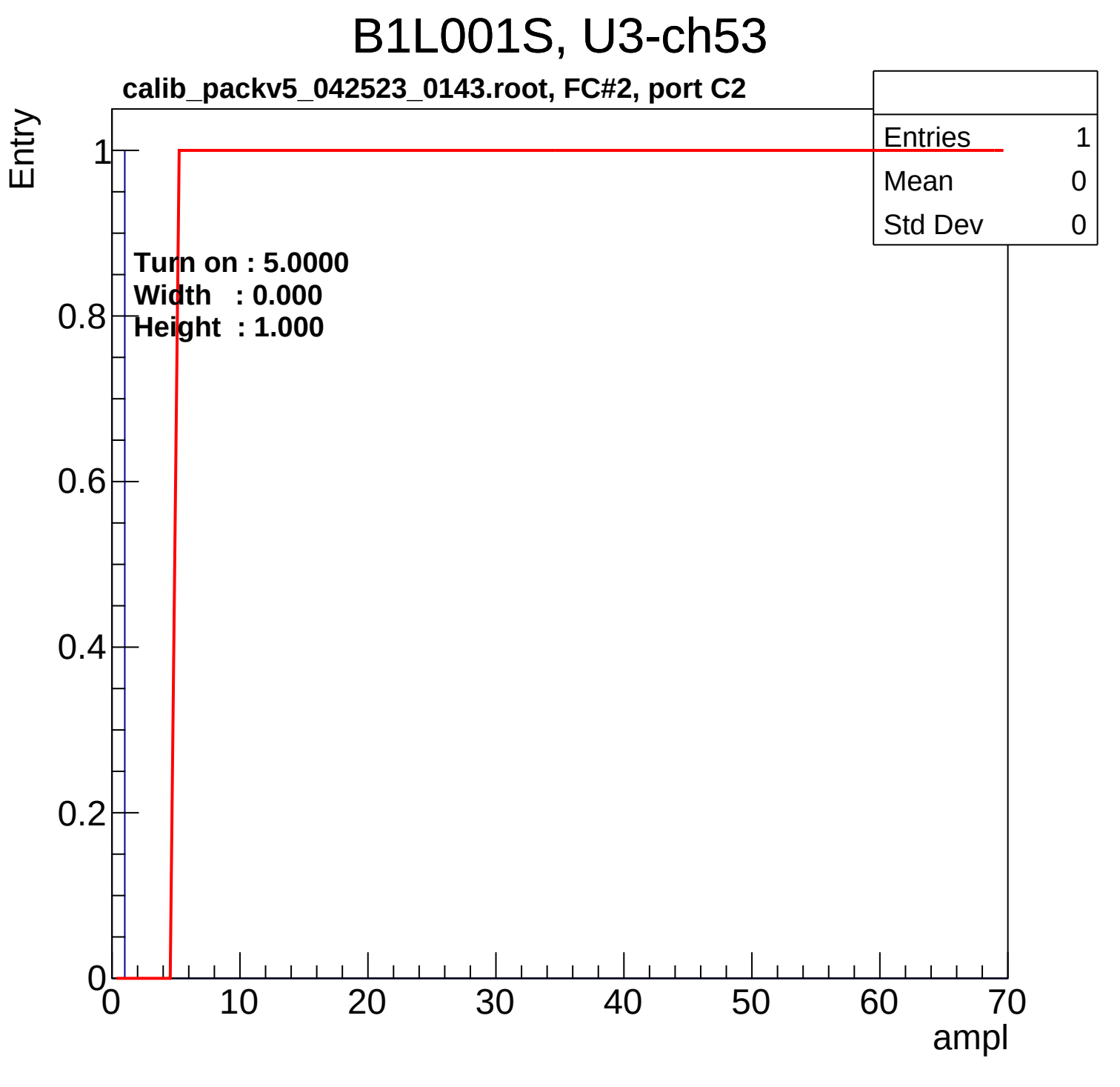

B1L001S, U3-ch48
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

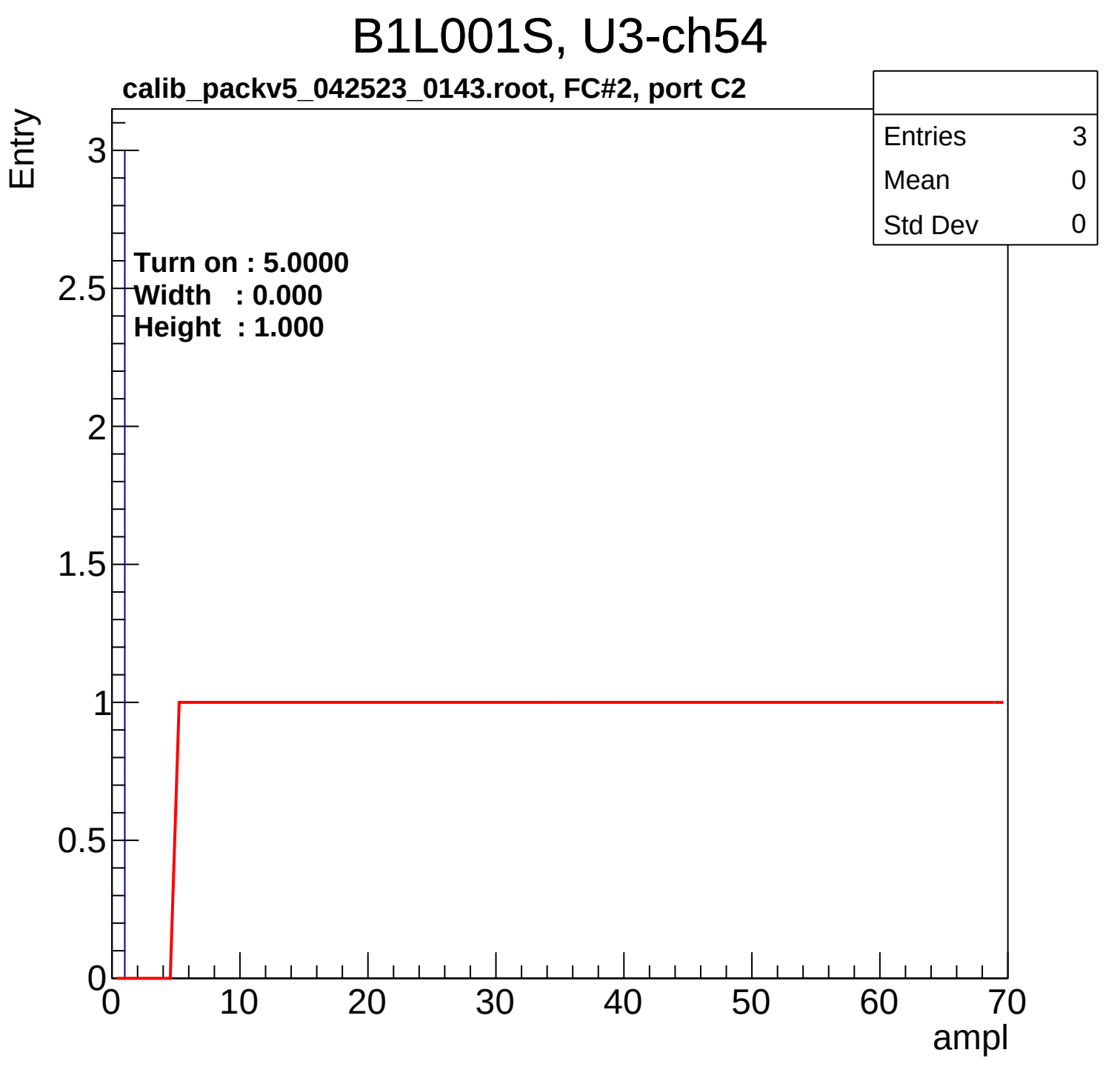

B1L001S, U3-ch49
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

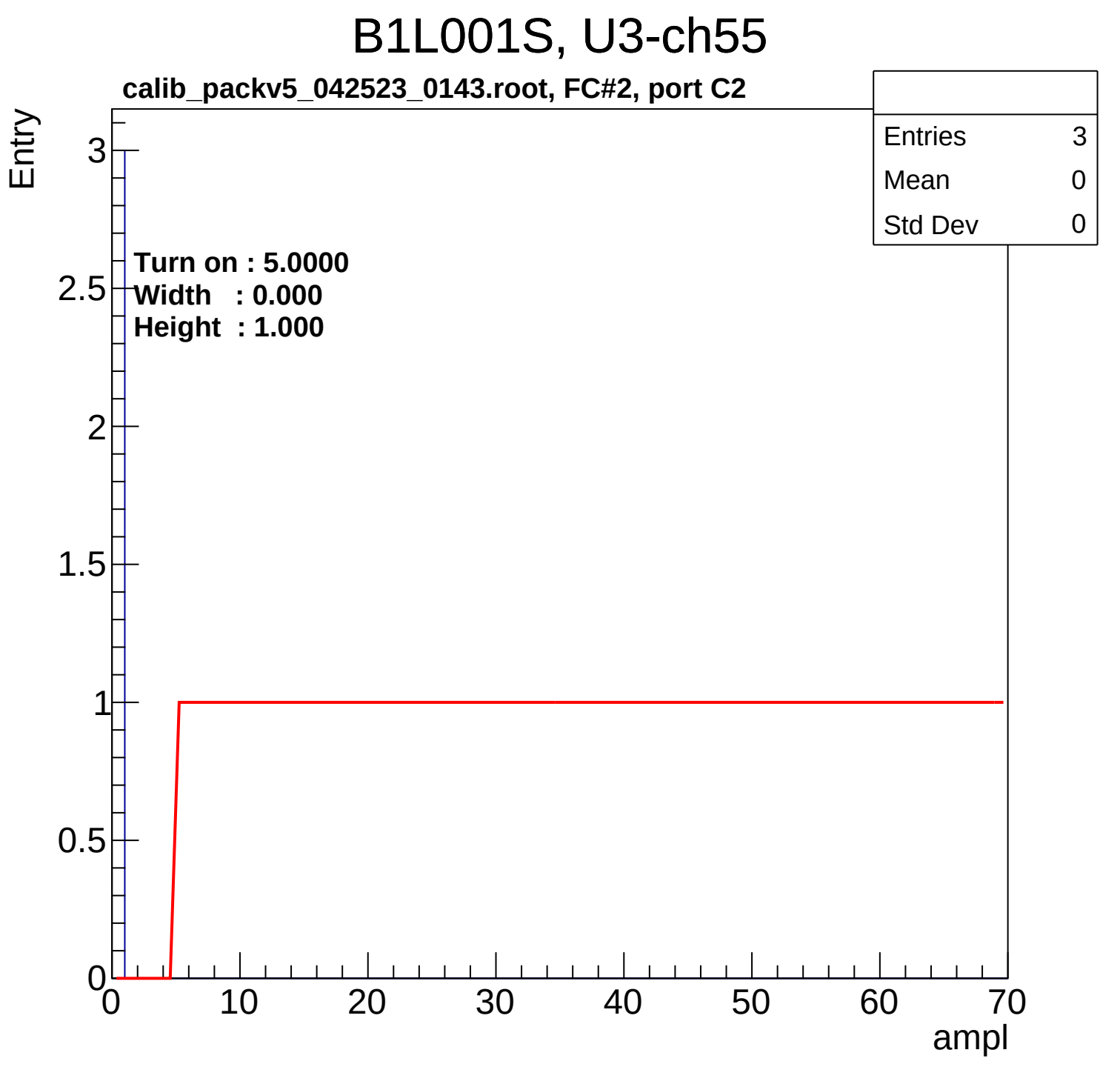

B1L001S, U3-ch50
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

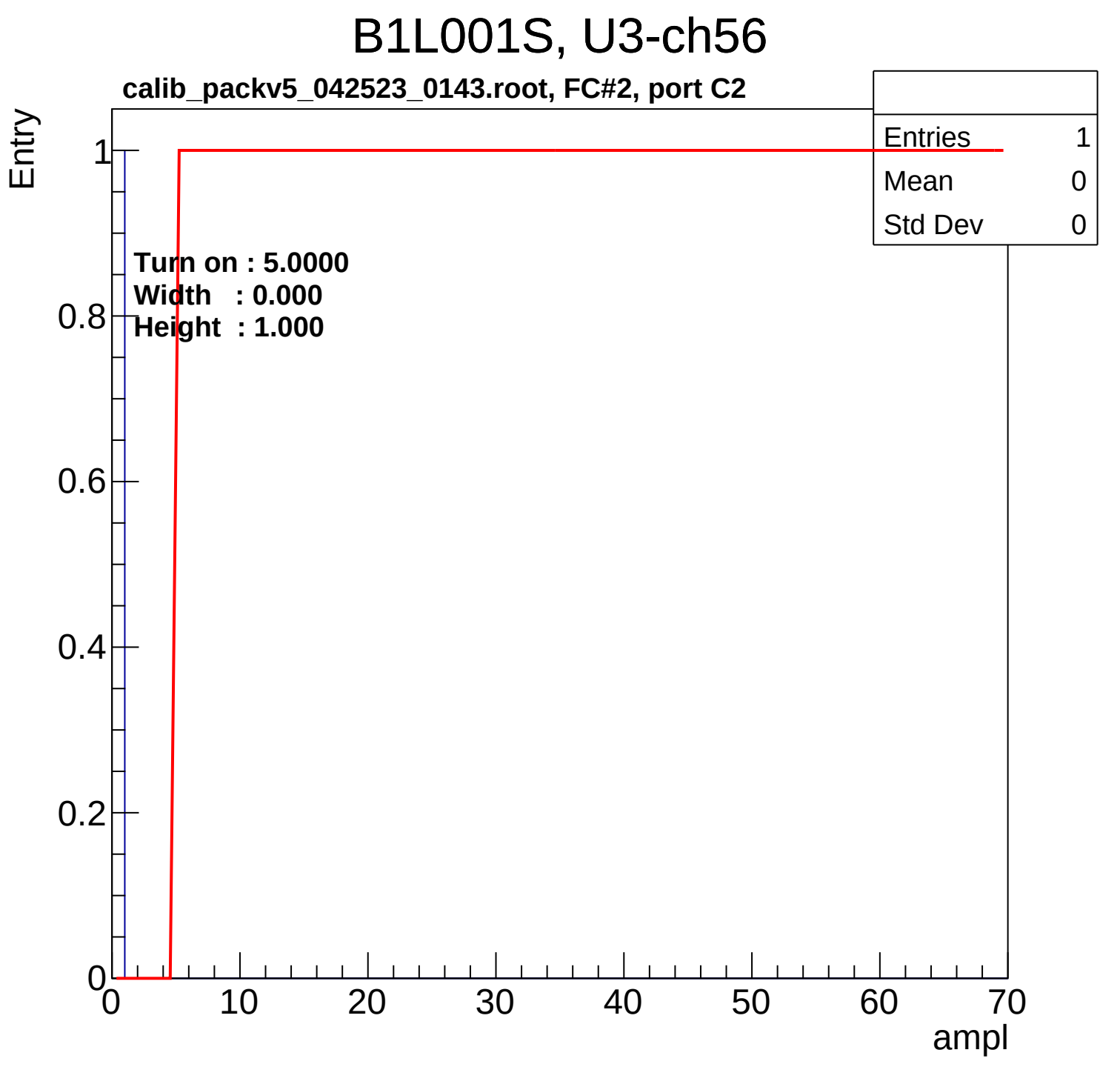

B1L001S, U3-ch51
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

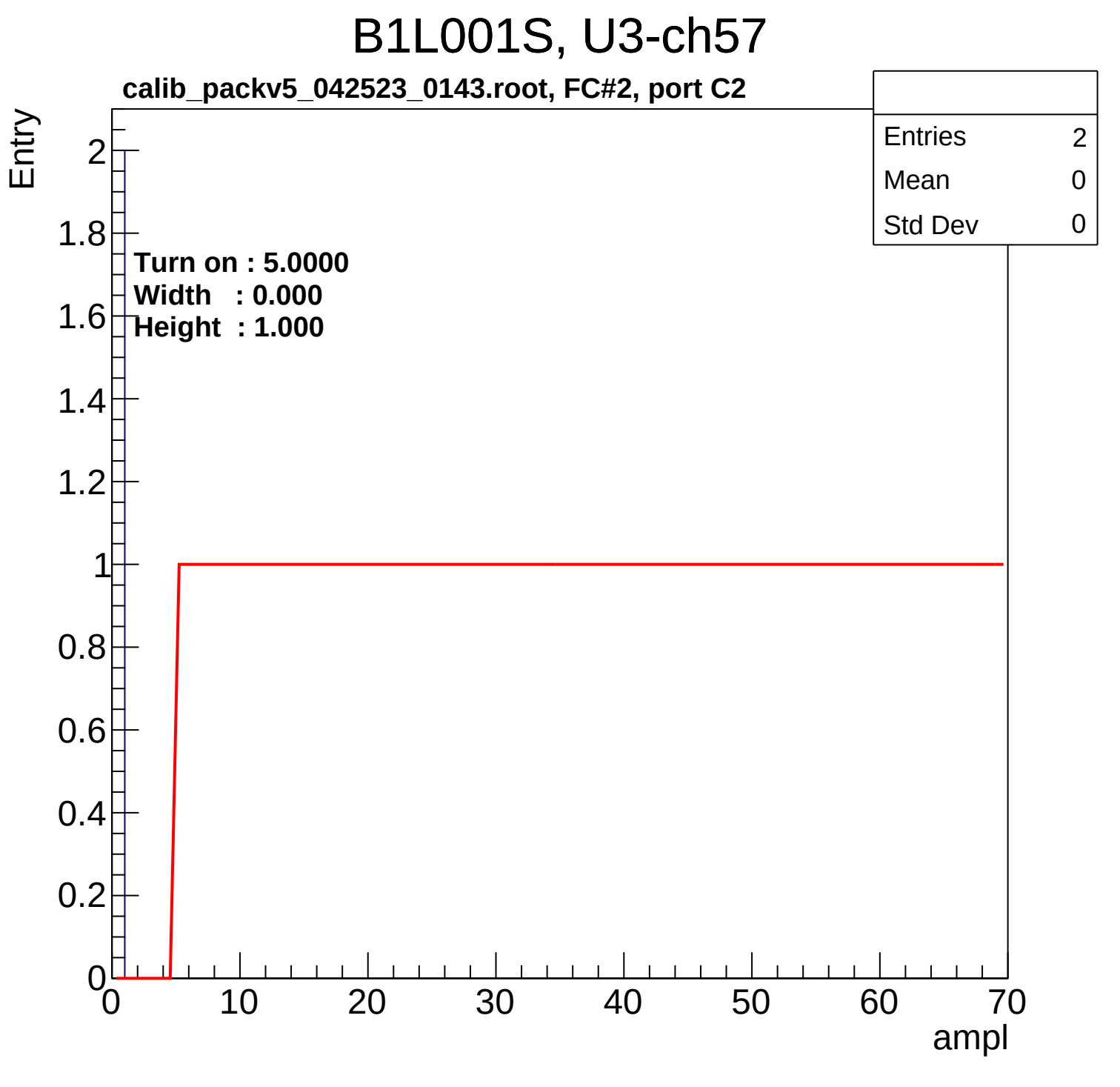

B1L001S, U3-ch52
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

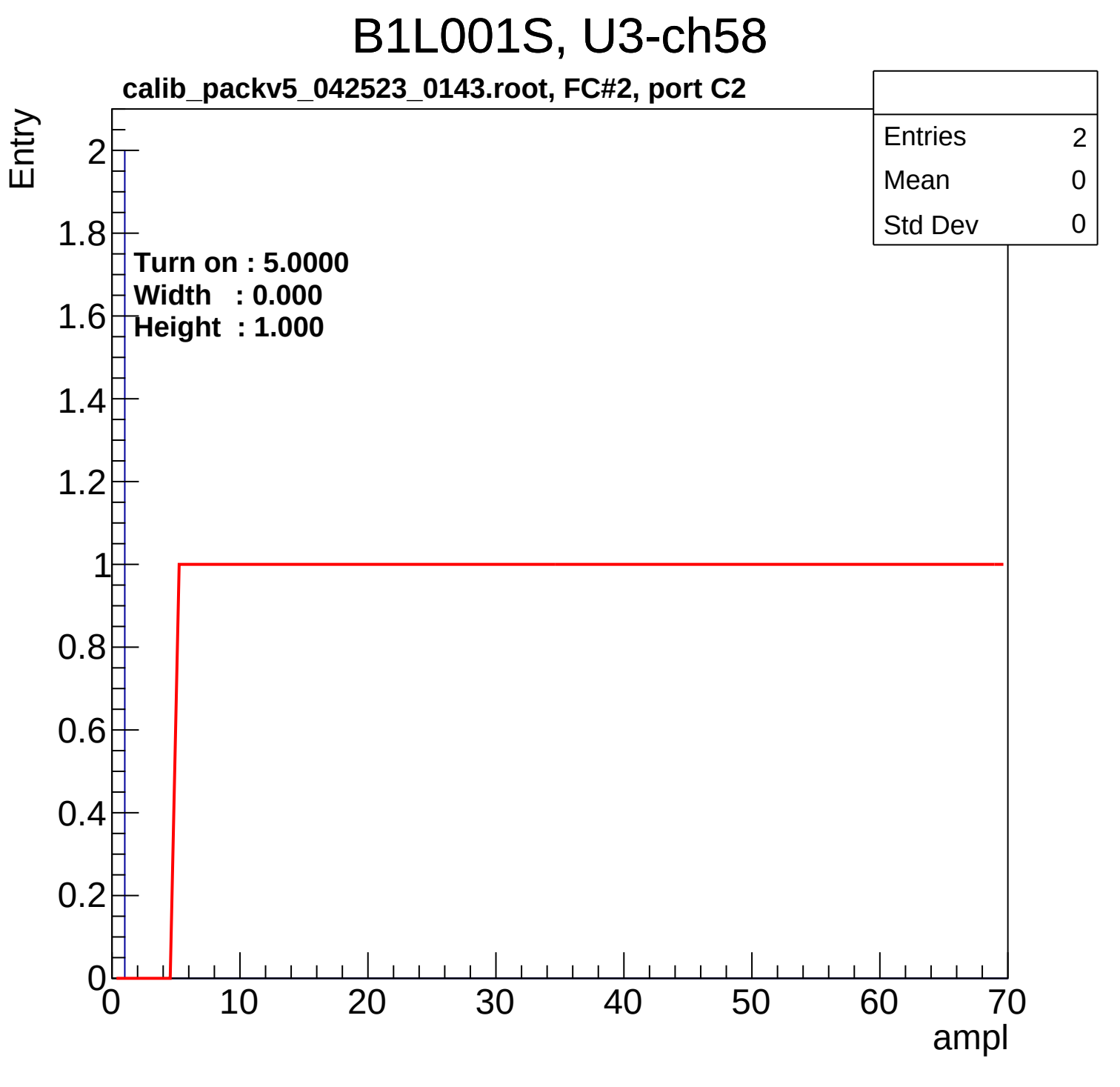

B1L001S, U3-ch53
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

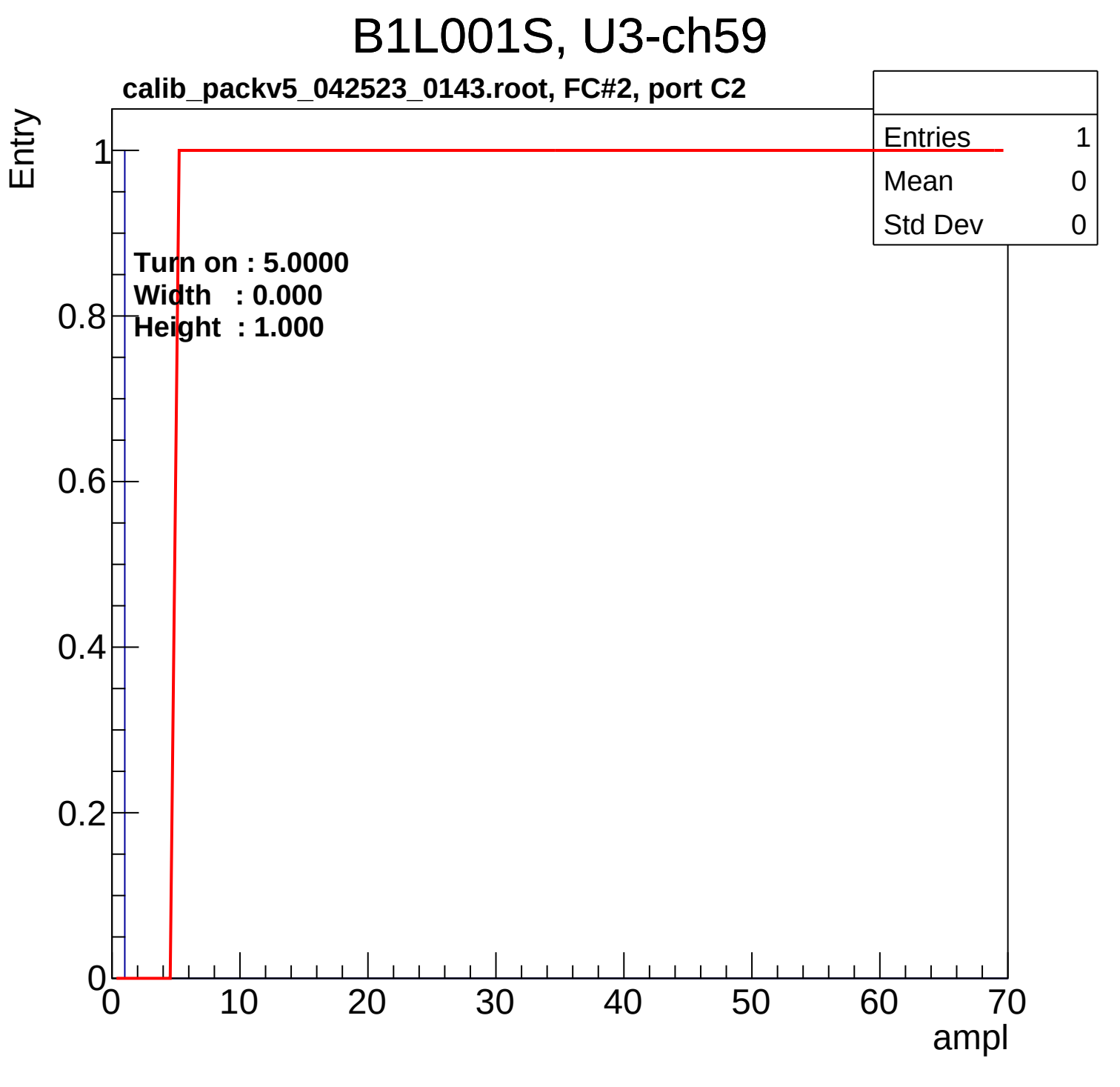

B1L001S, U3-ch54
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

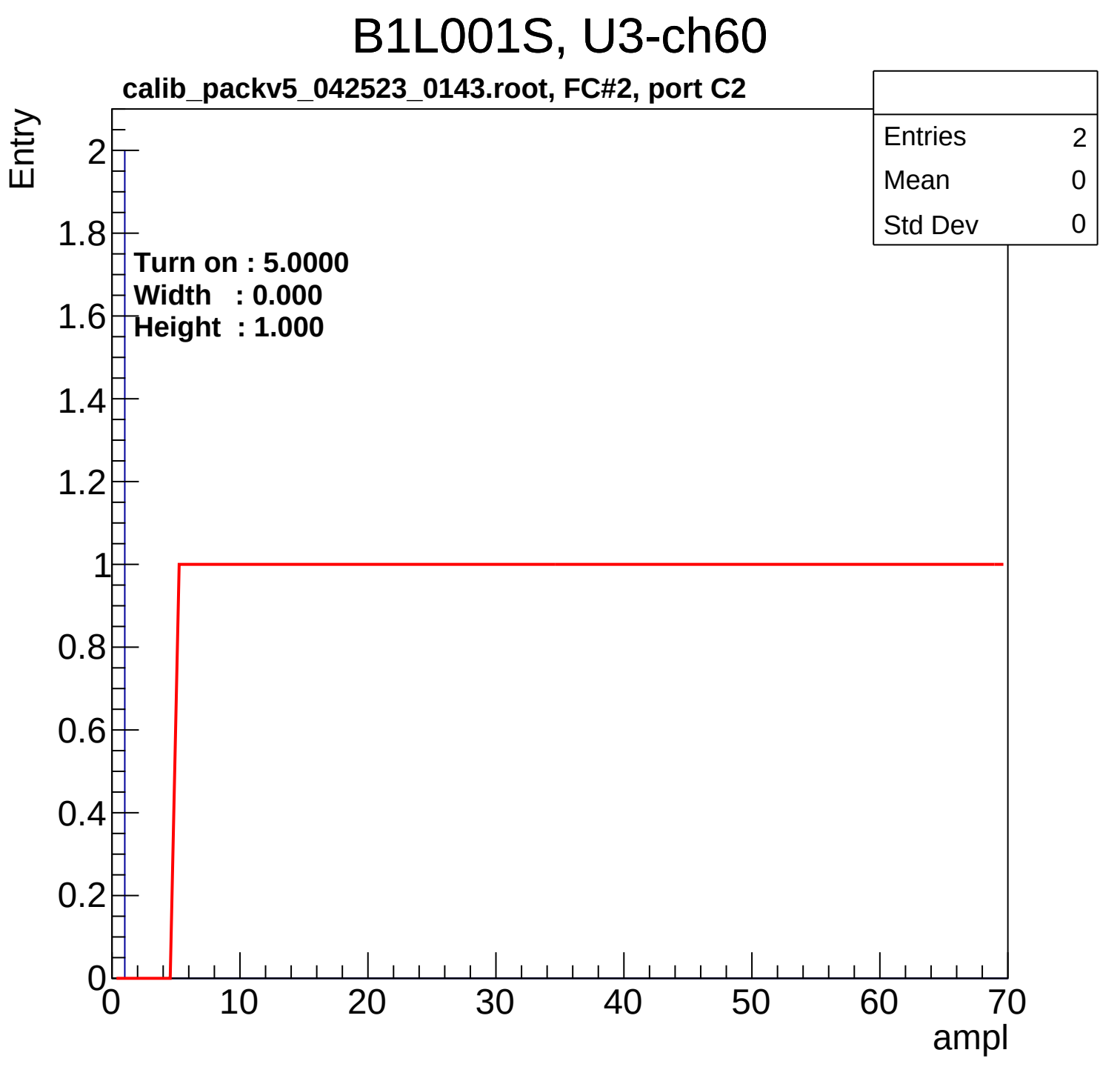

B1L001S, U3-ch55
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

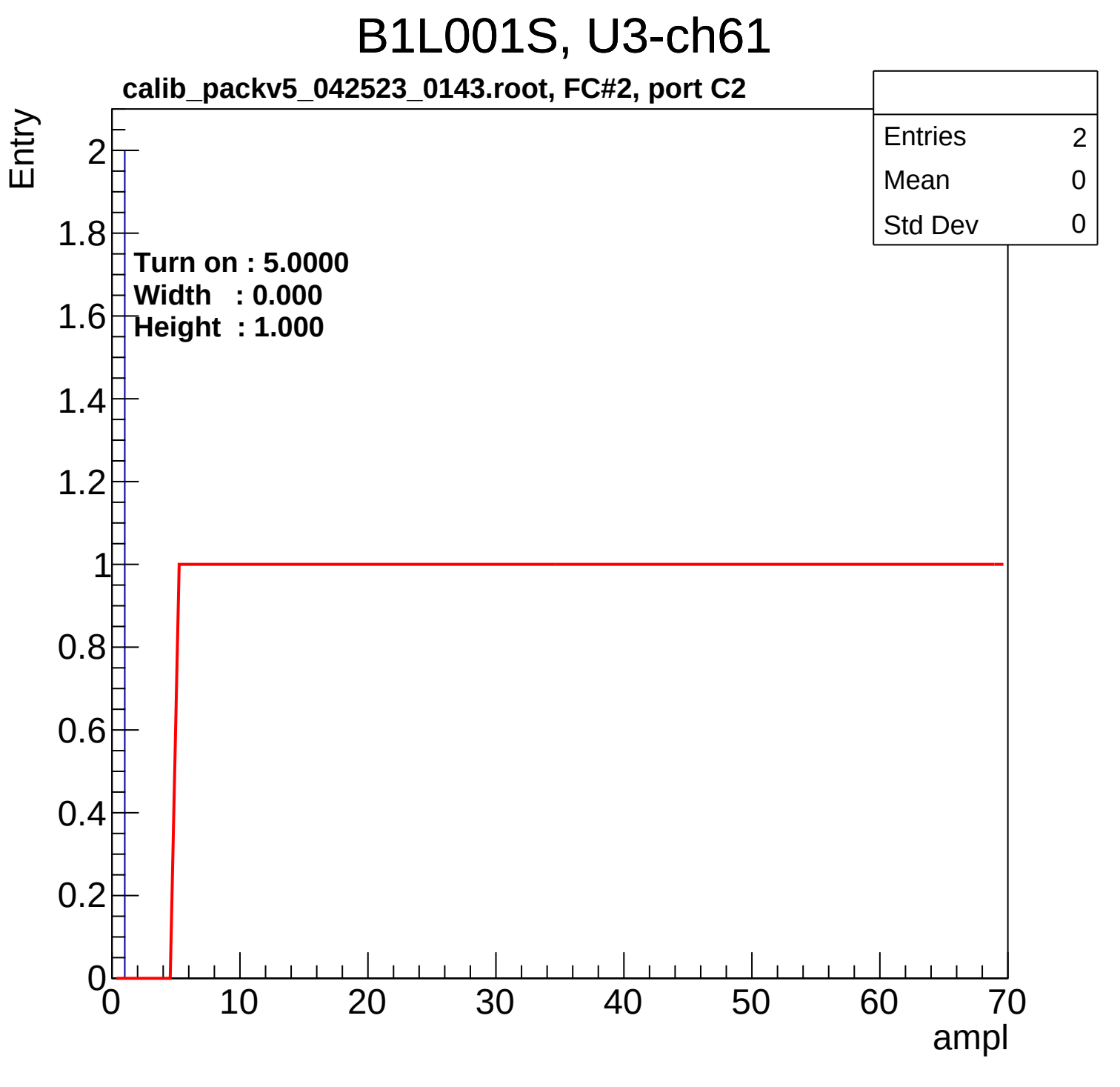

B1L001S, U3-ch56
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

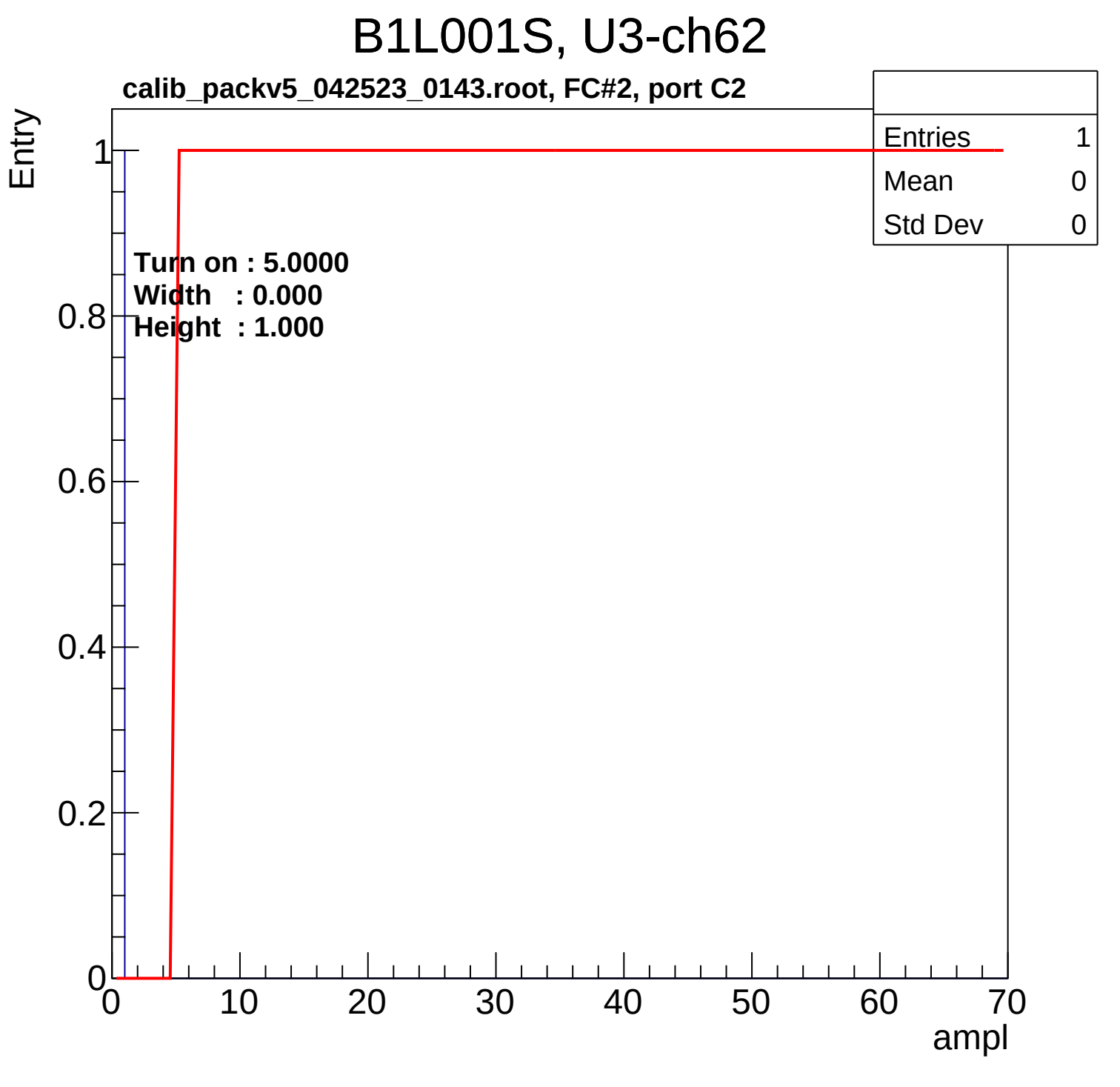

B1L001S, U3-ch57
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

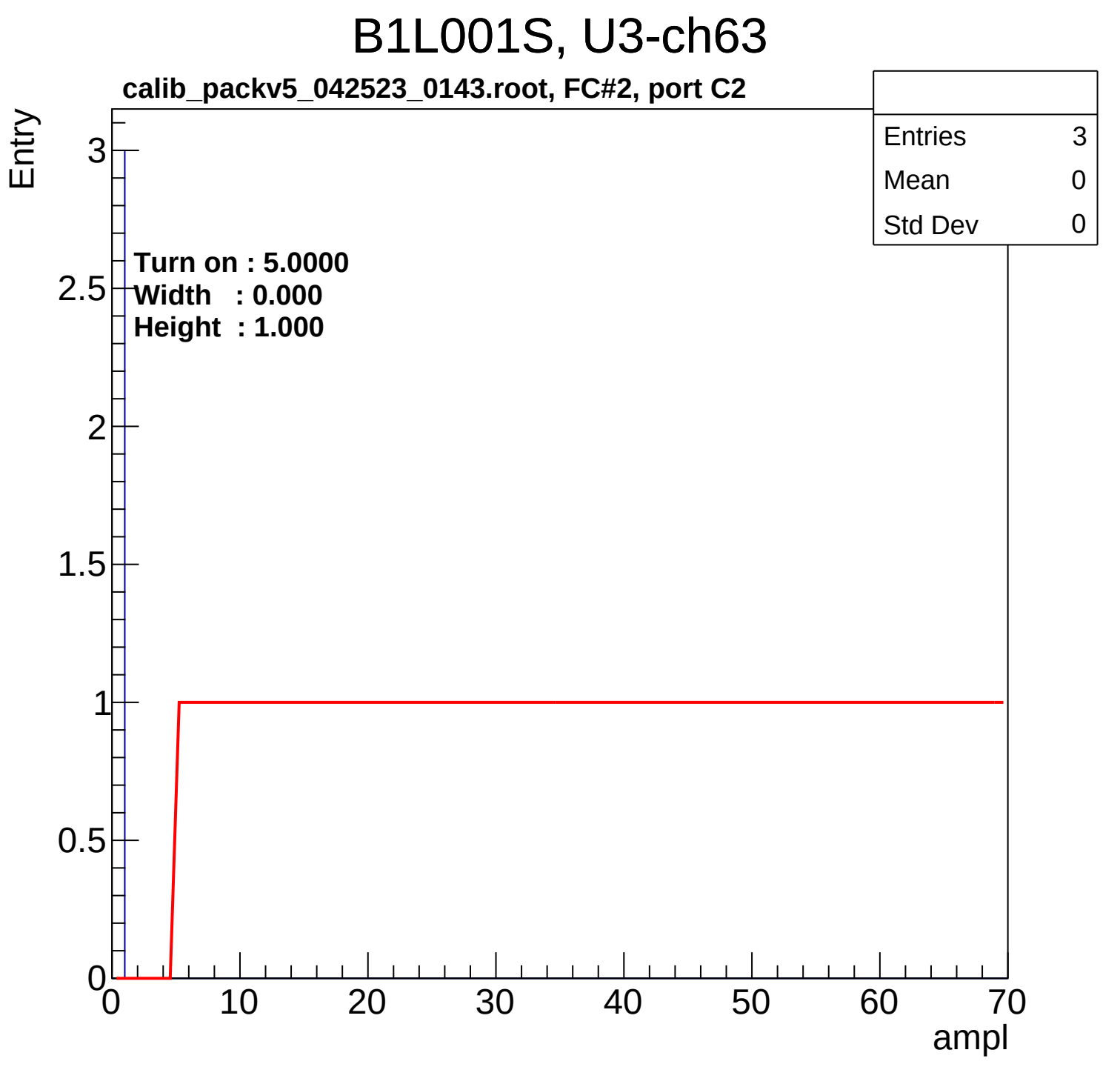

B1L001S, U3-ch58
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

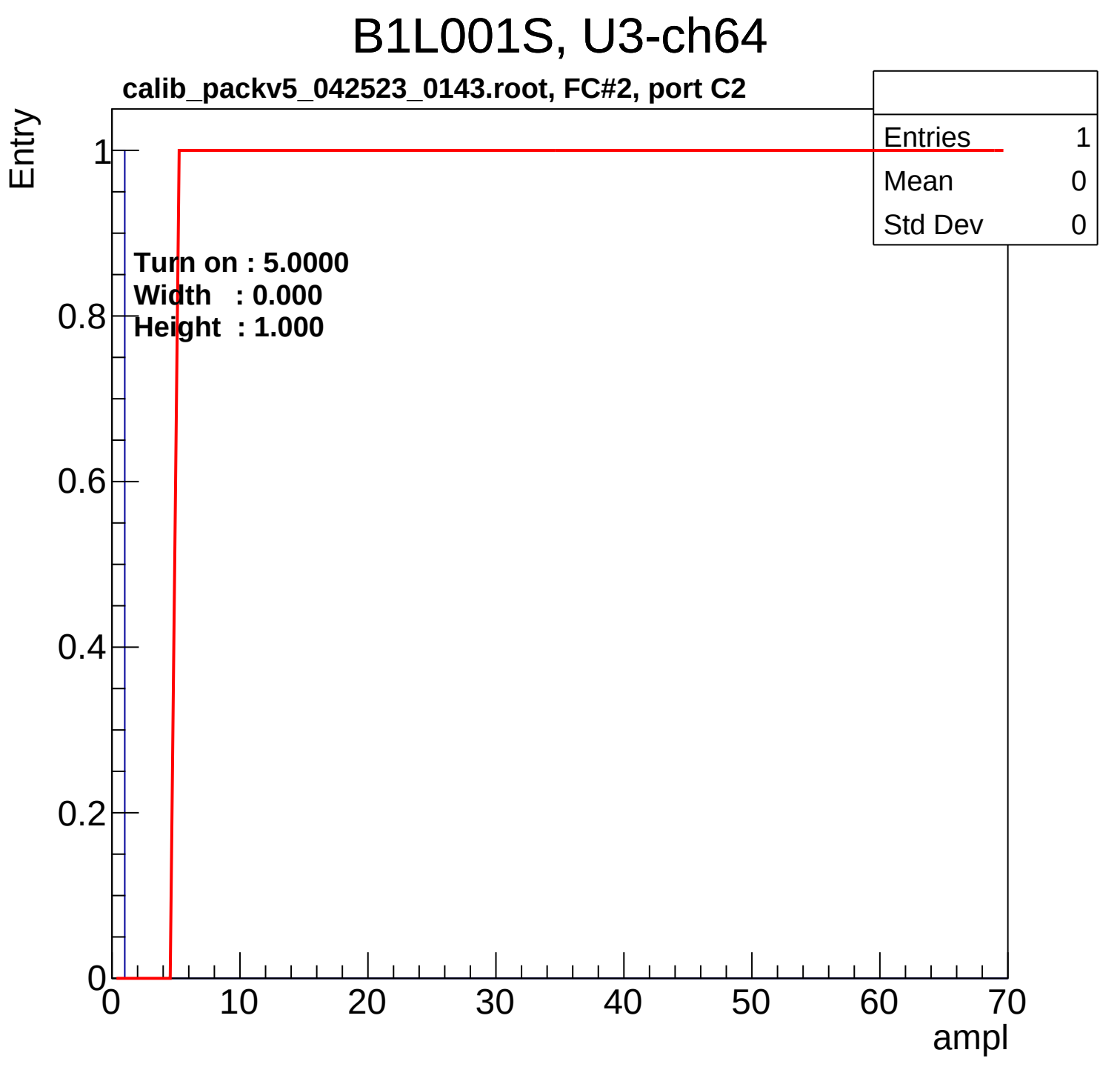

B1L001S, U3-ch59
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

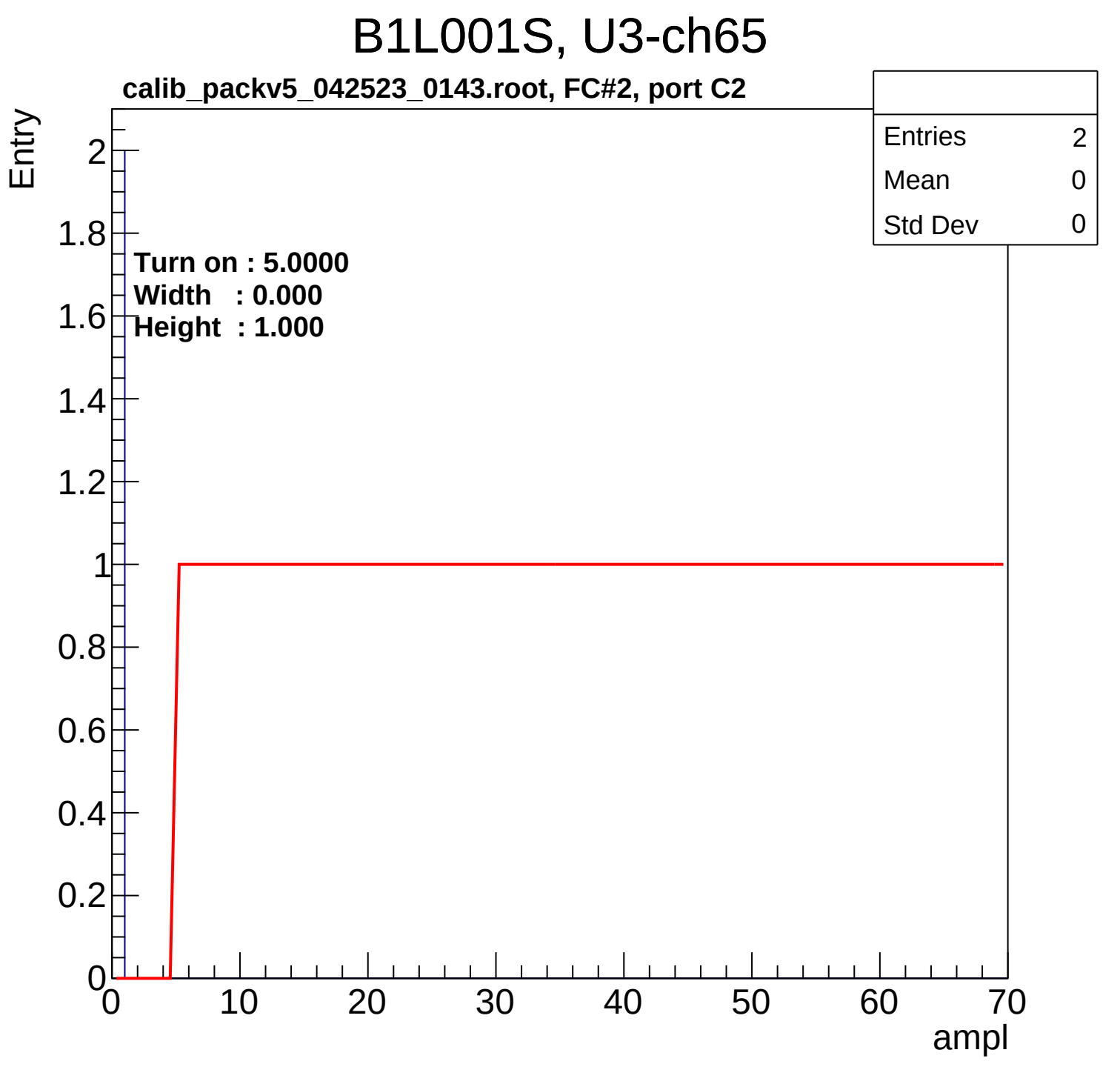

B1L001S, U3-ch60
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

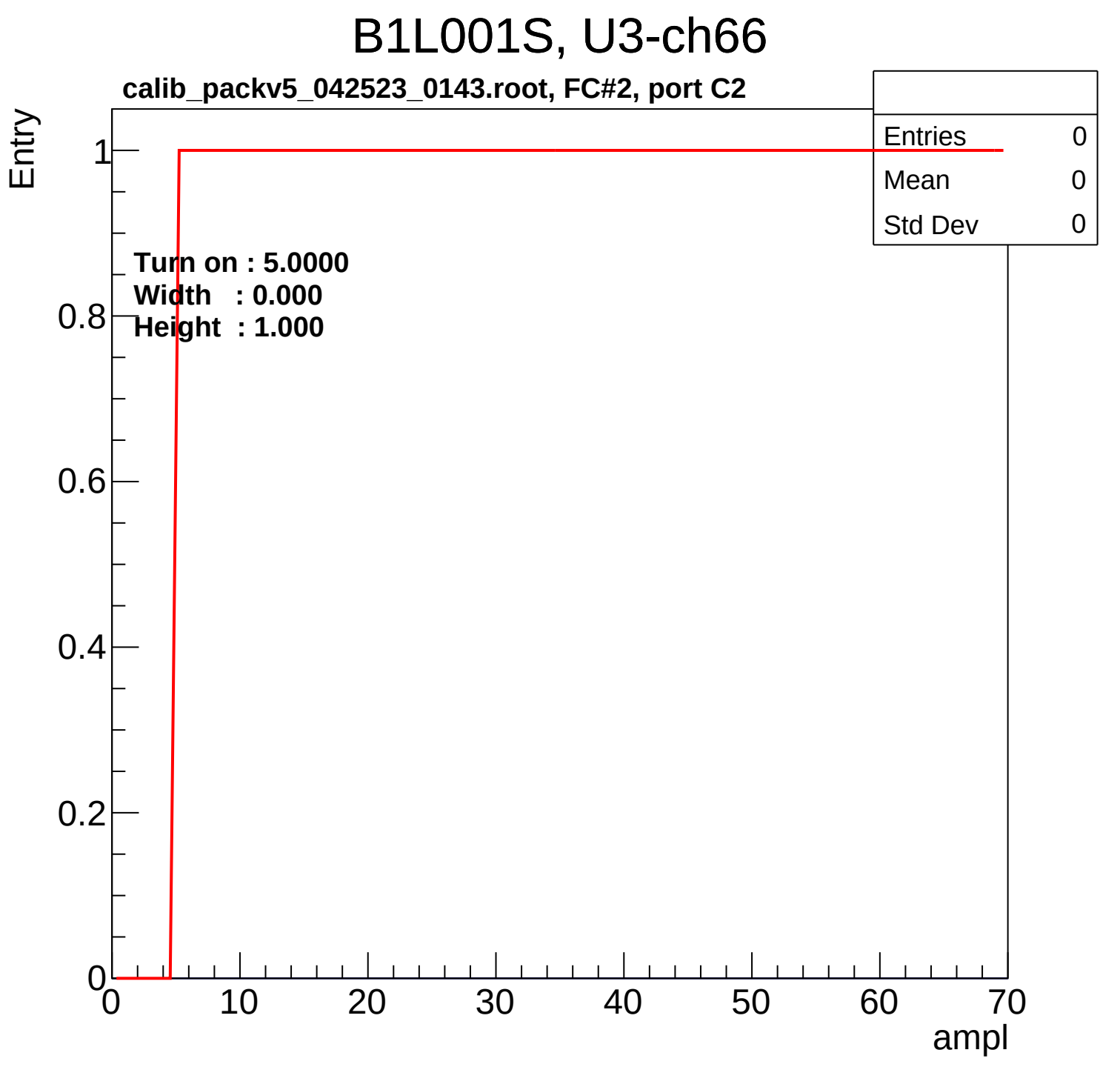

B1L001S, U3-ch61
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

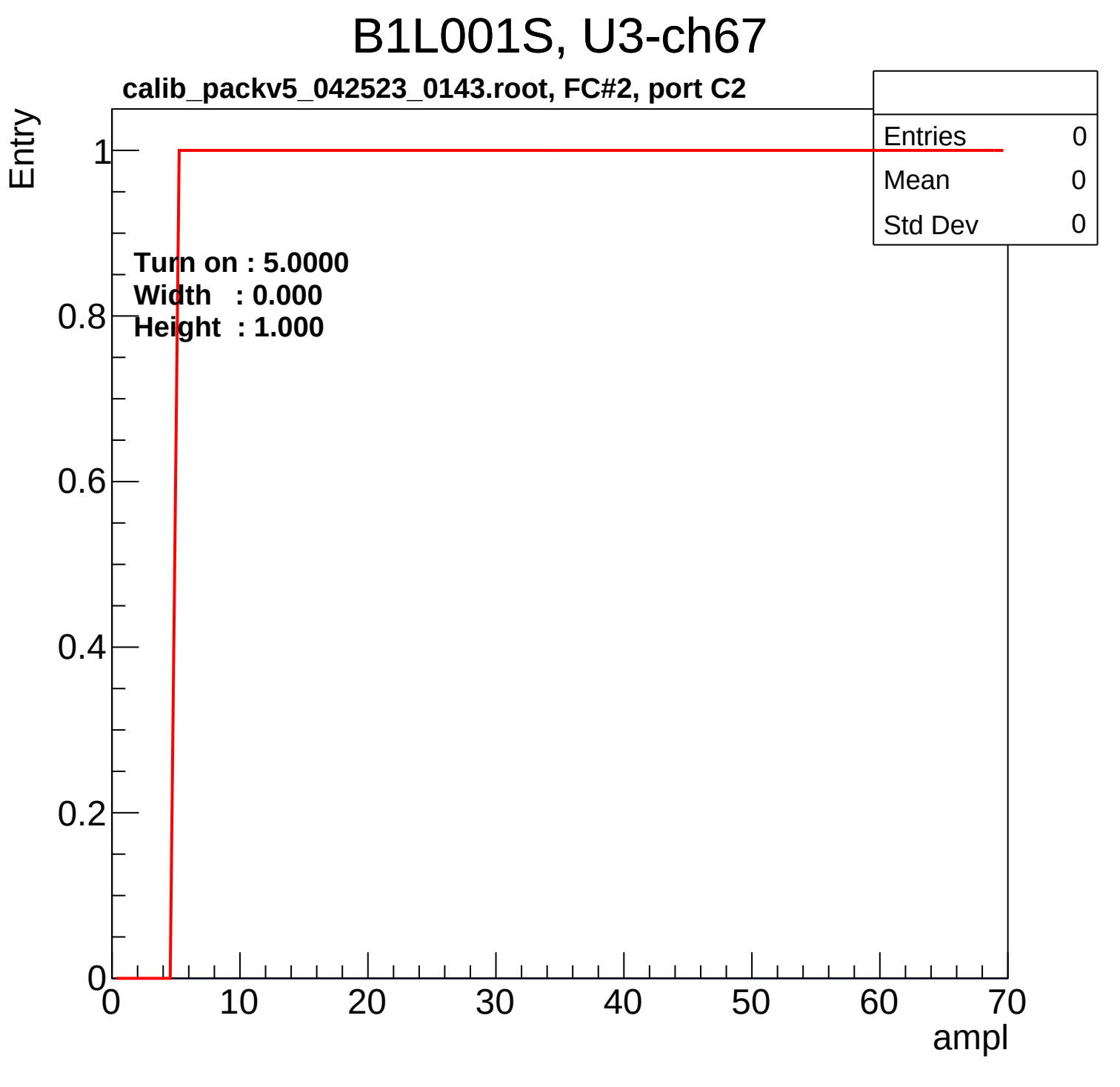

B1L001S, U3-ch62
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

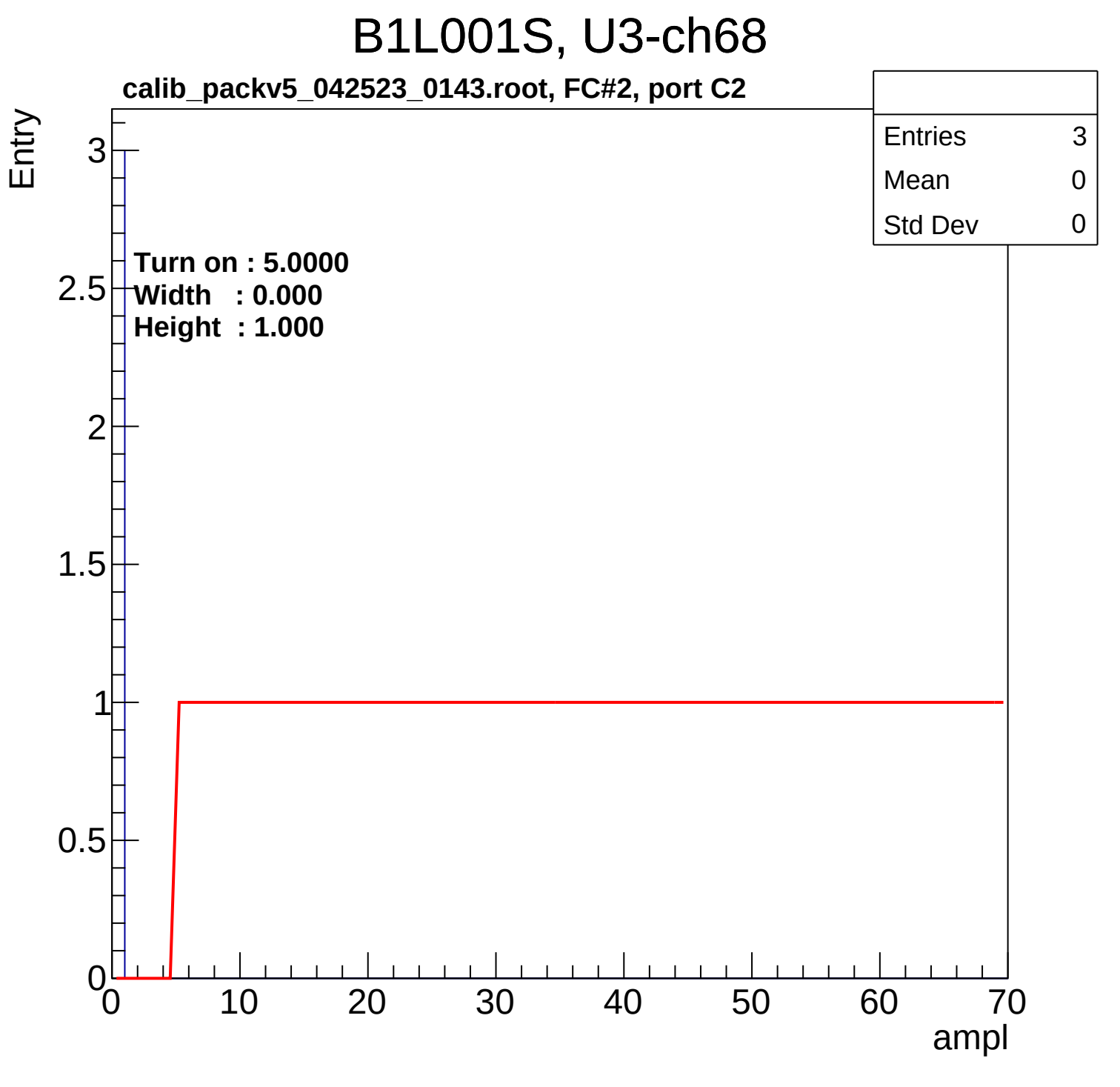

B1L001S, U3-ch63
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

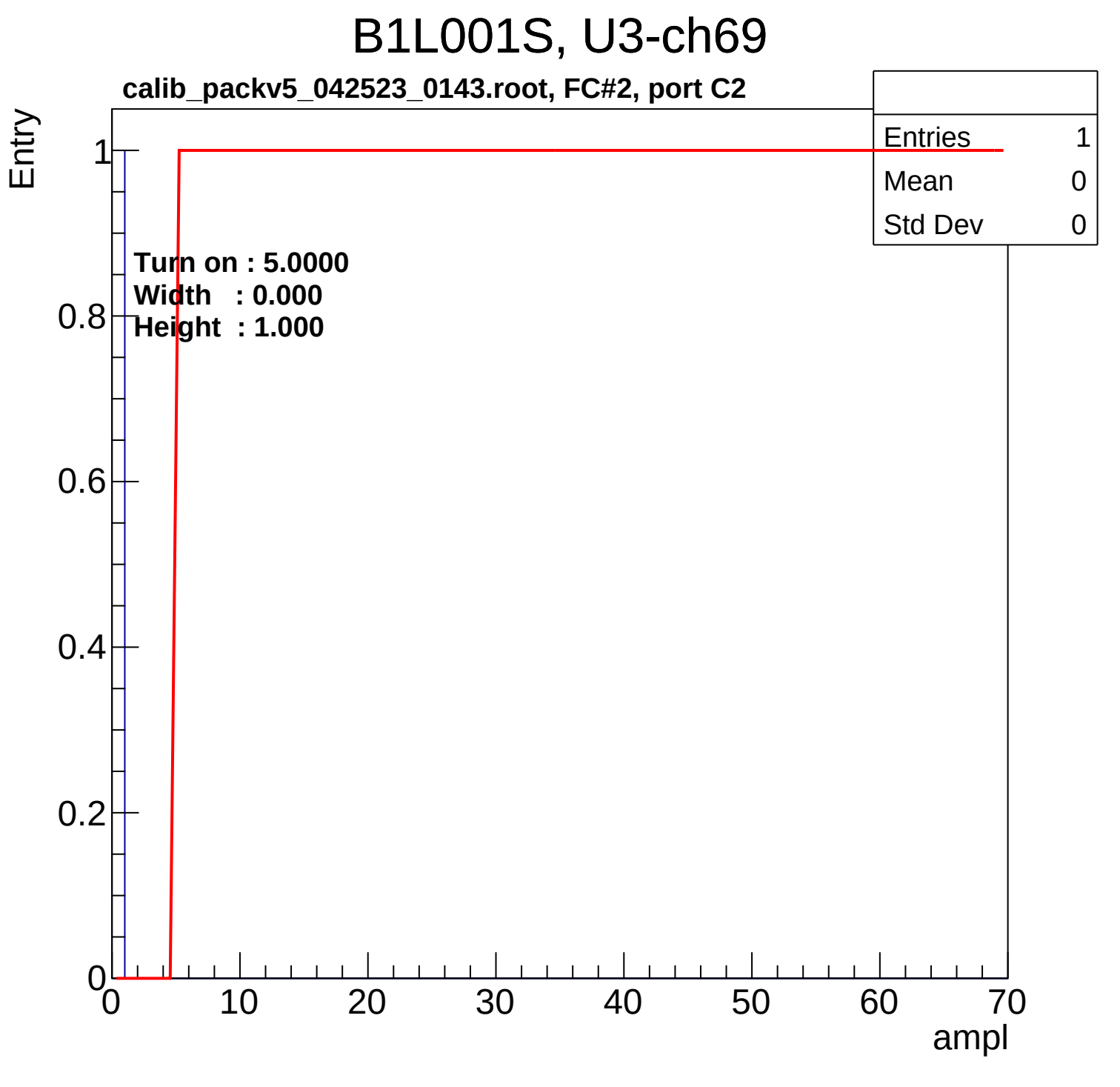

B1L001S, U3-ch64
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

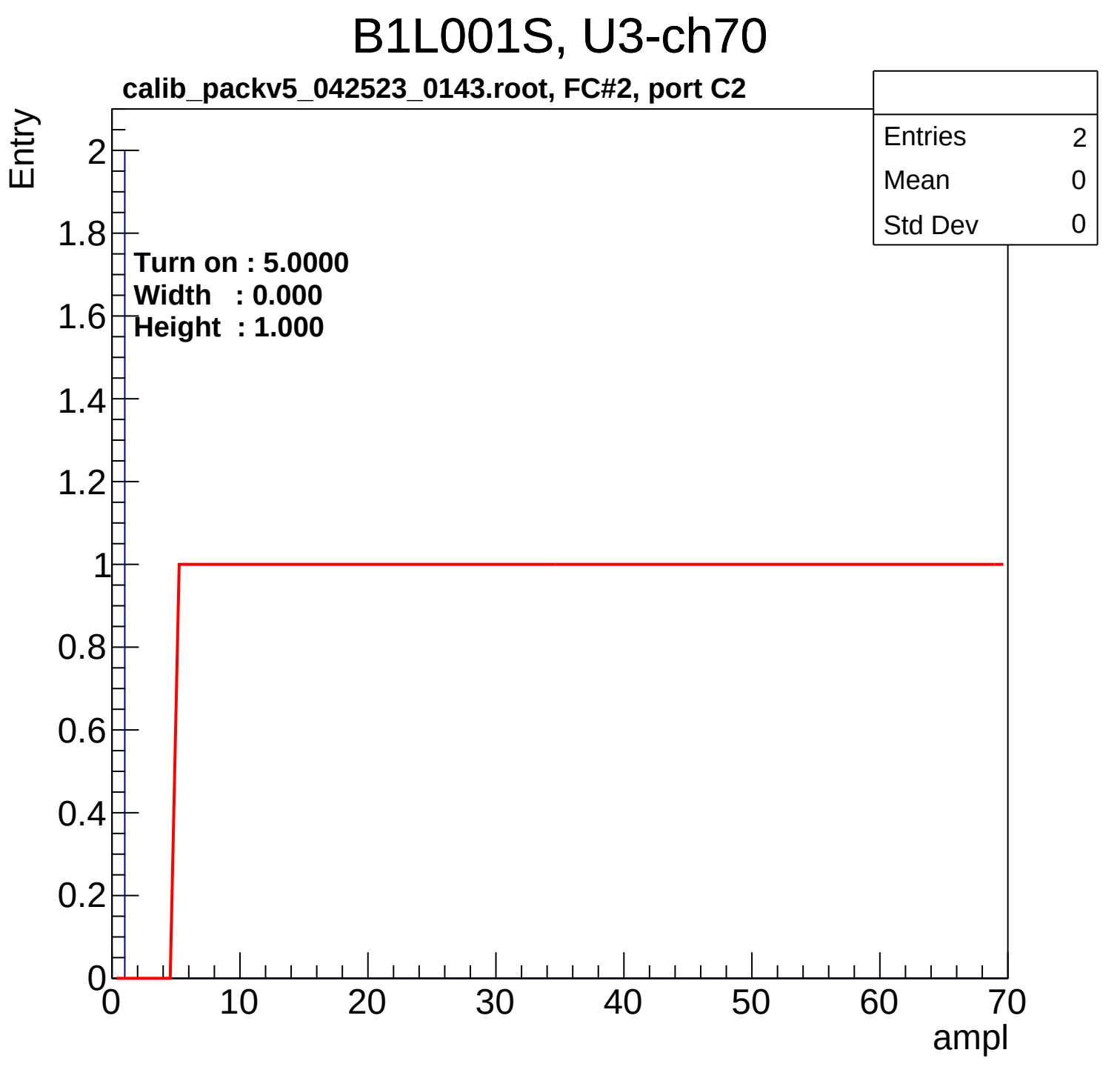

B1L001S, U3-ch65
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

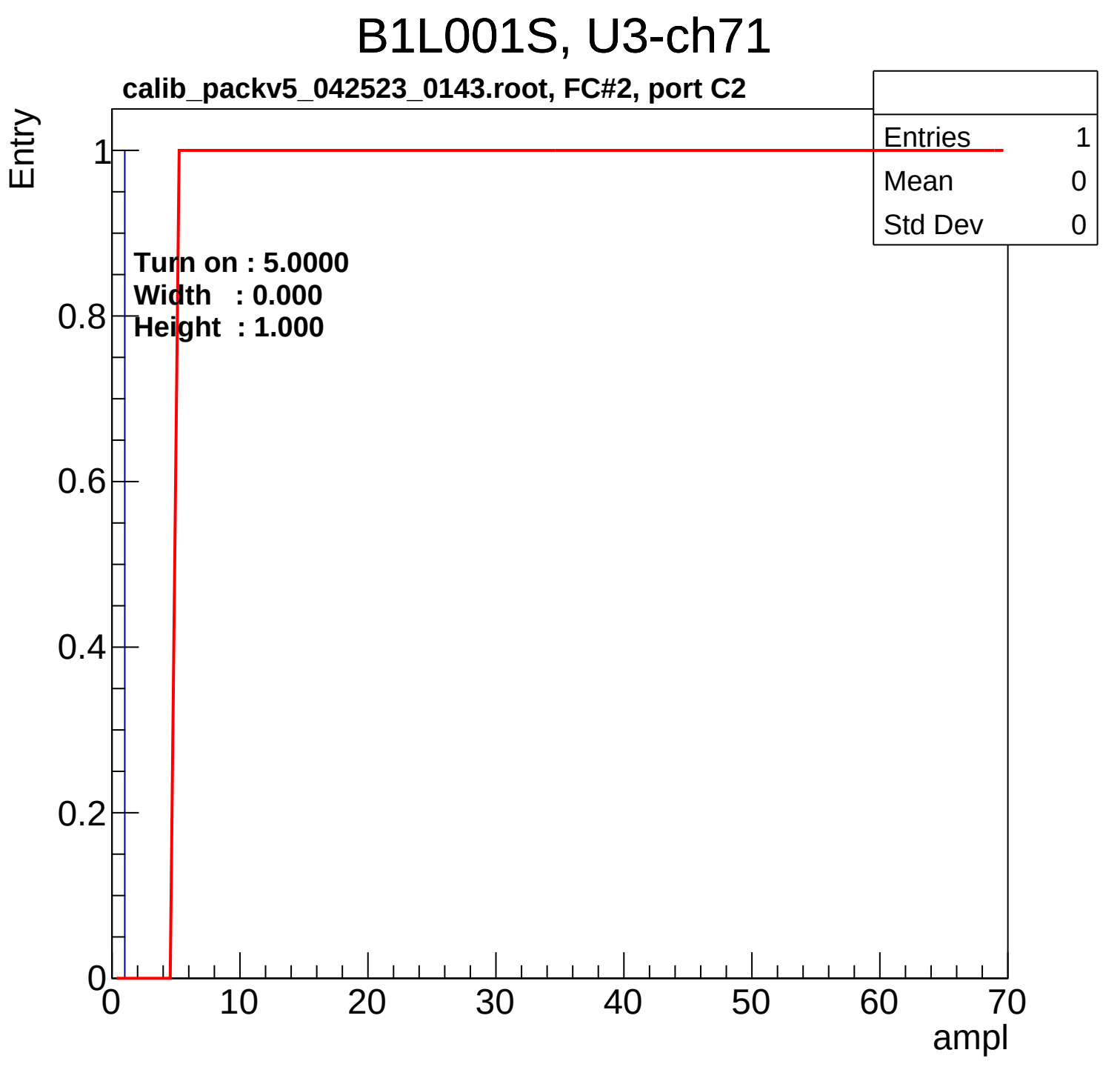

B1L001S, U3-ch66
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

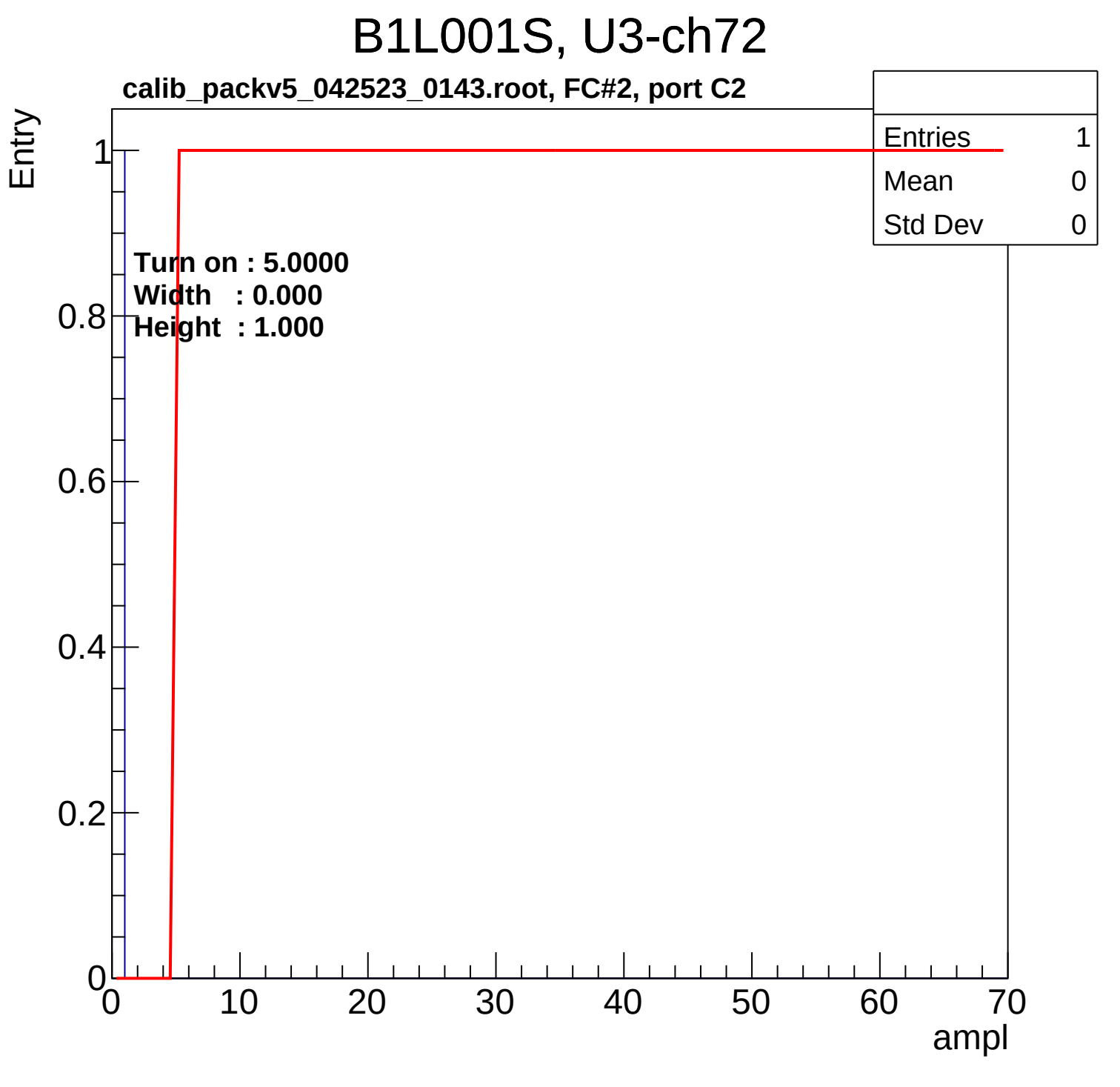

B1L001S, U3-ch67
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

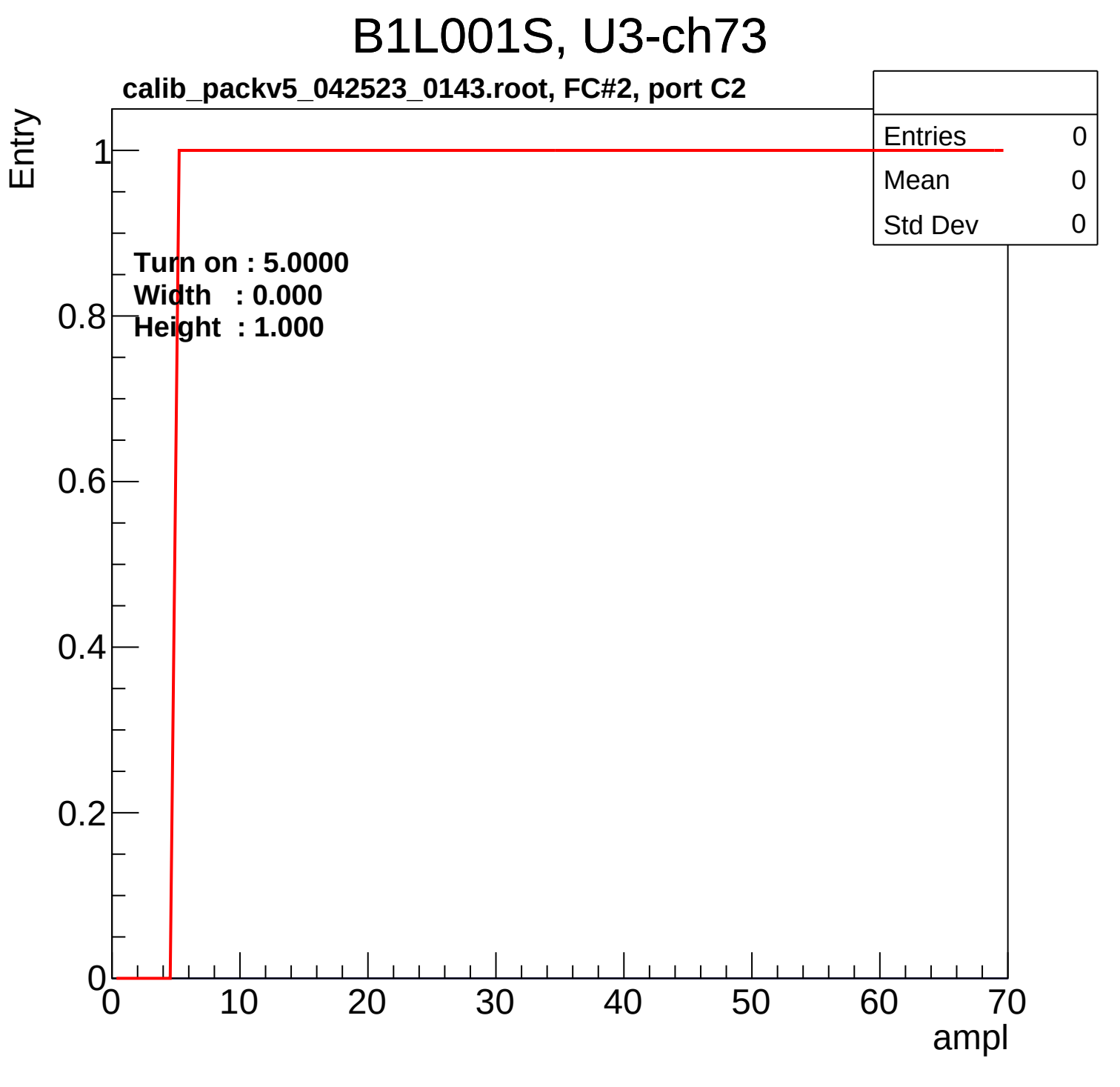

B1L001S, U3-ch68
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

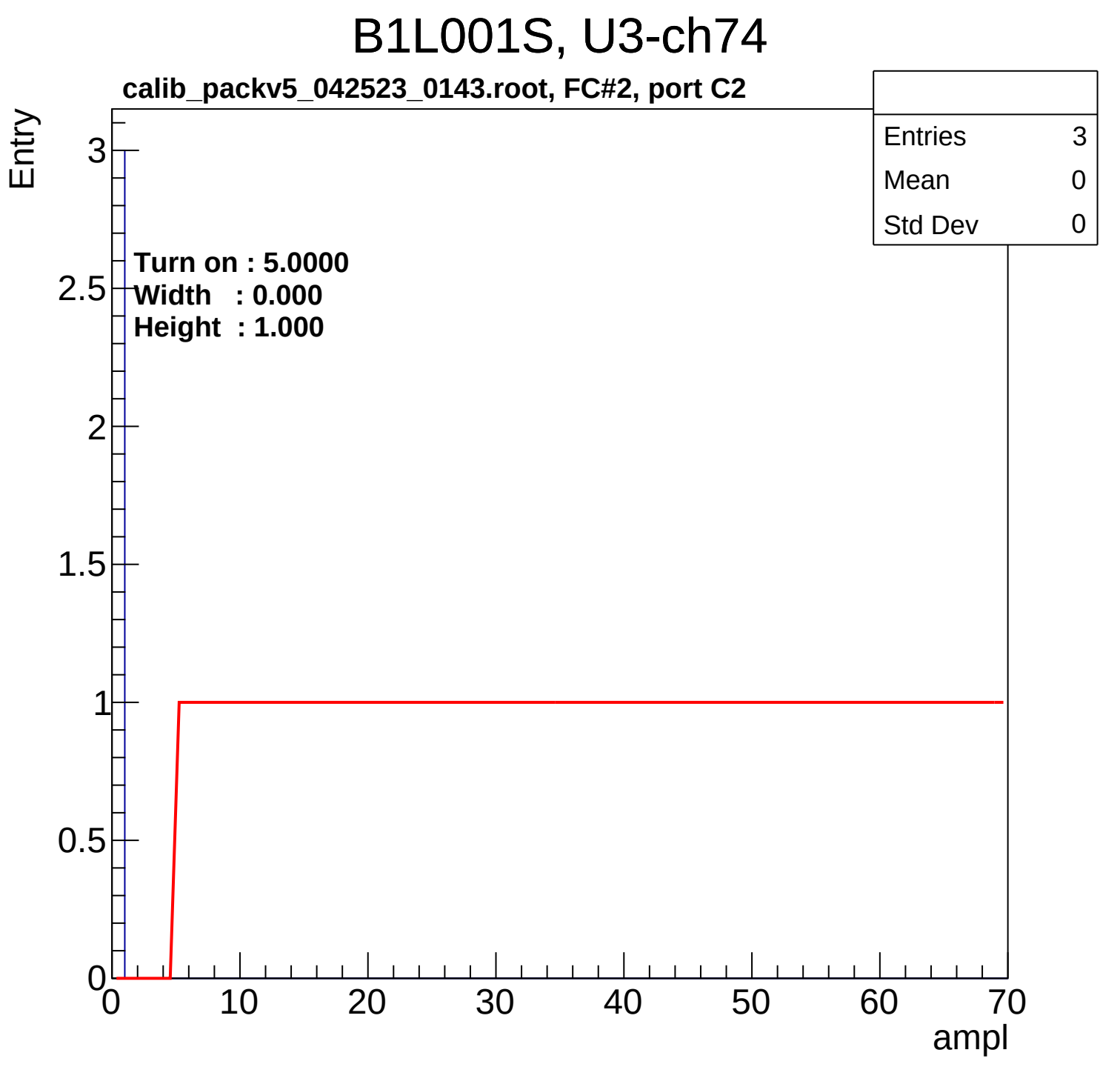

B1L001S, U3-ch69
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

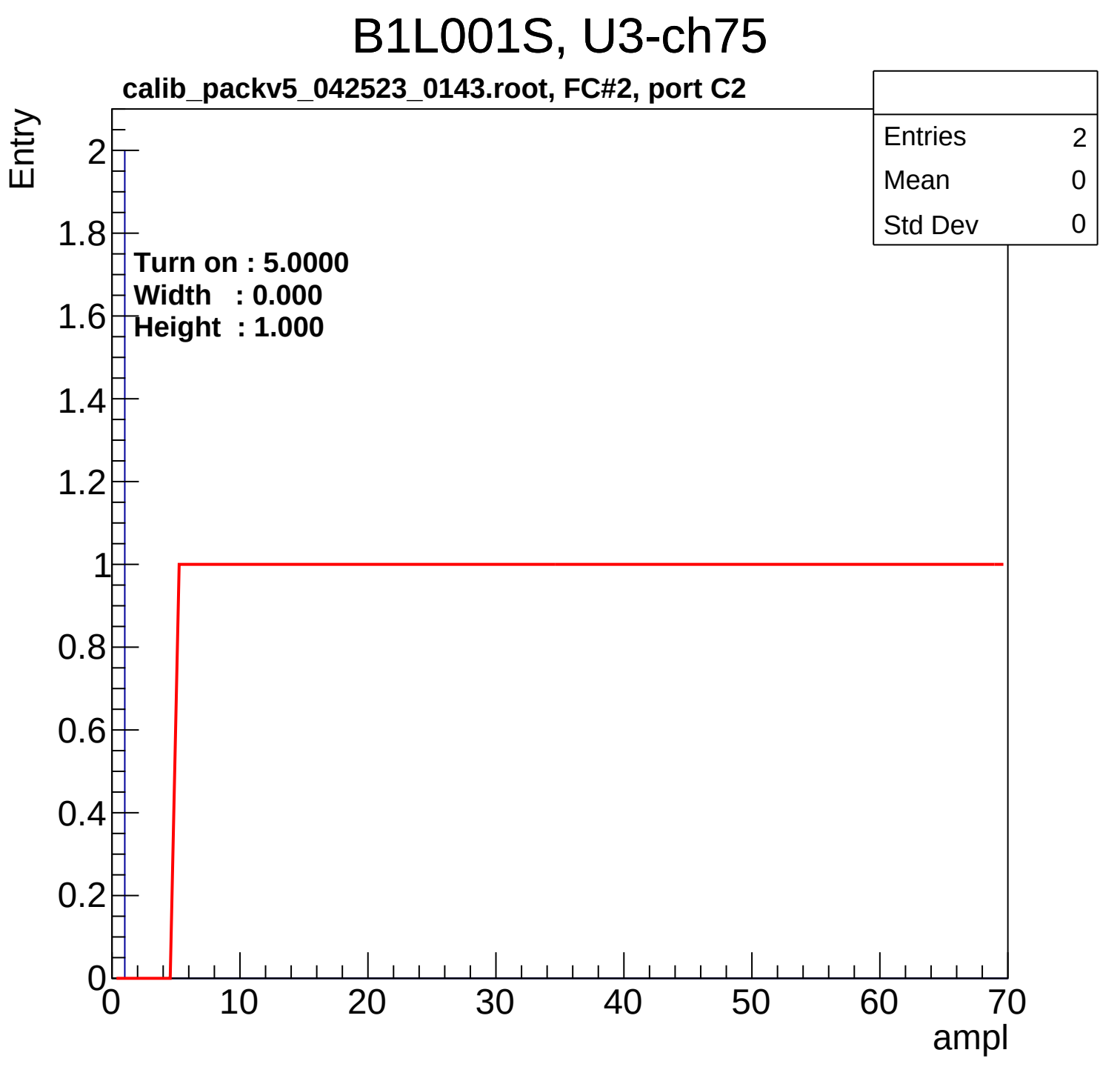

B1L001S, U3-ch70
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

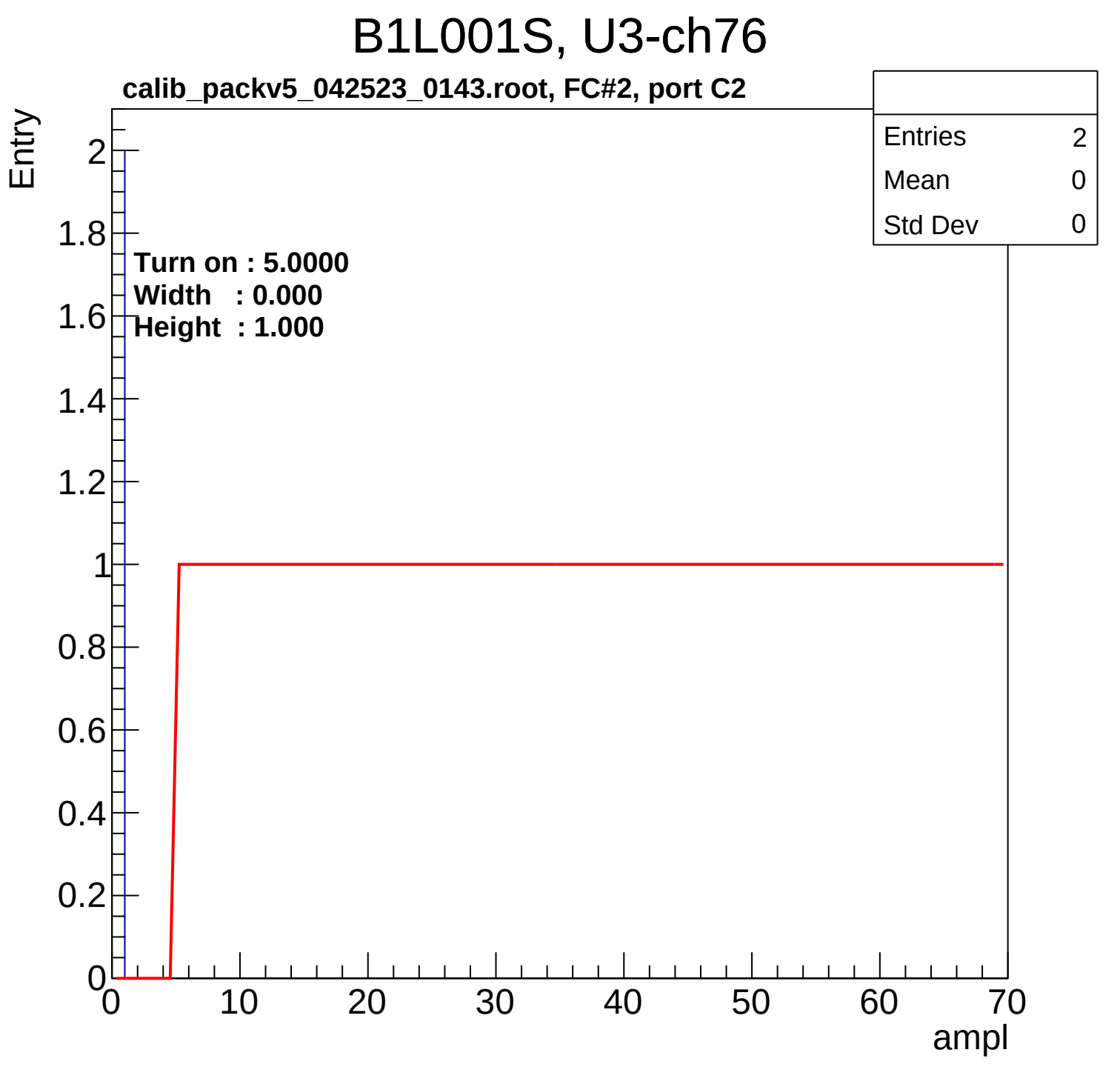

B1L001S, U3-ch71
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

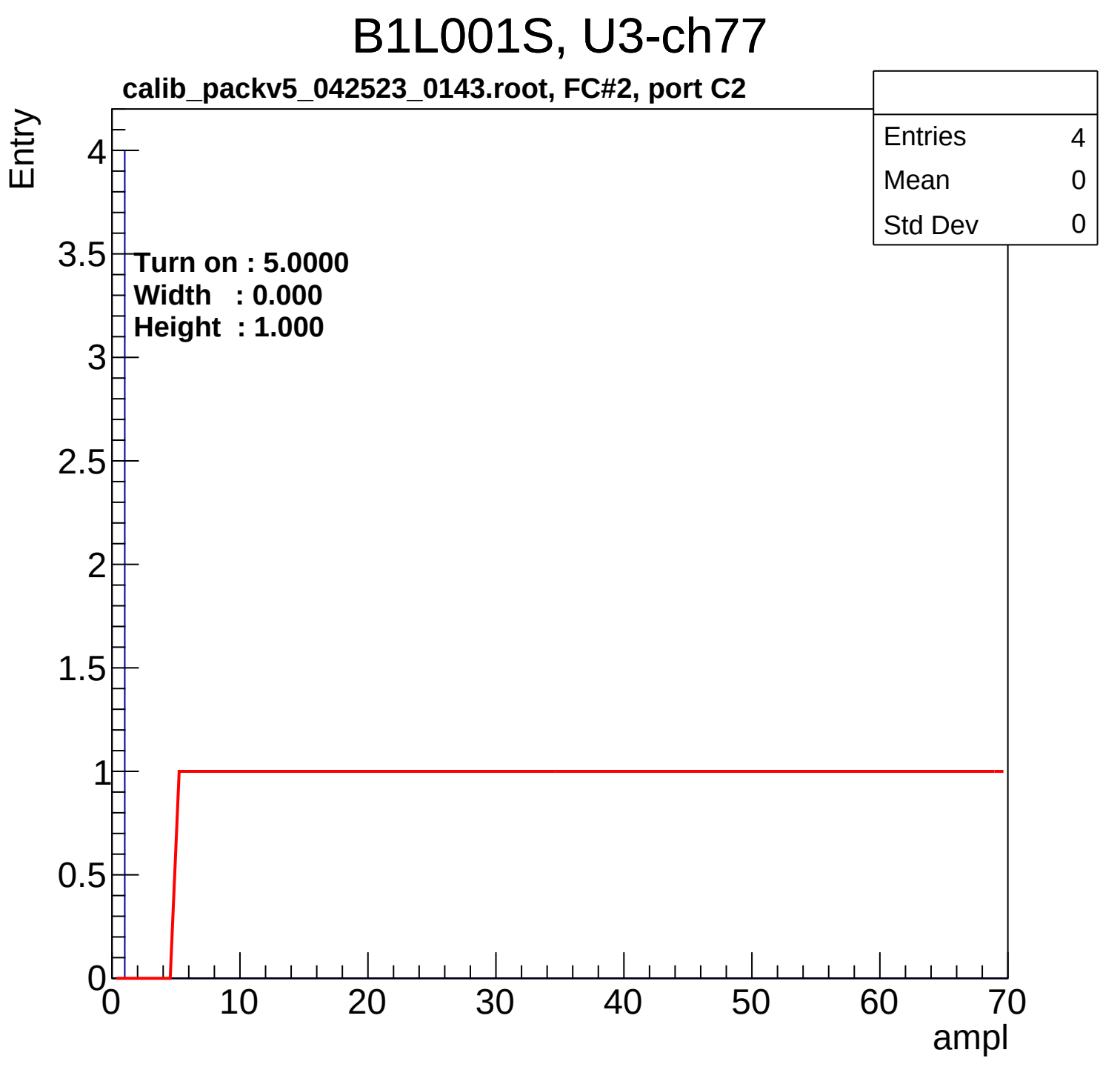

B1L001S, U3-ch72
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

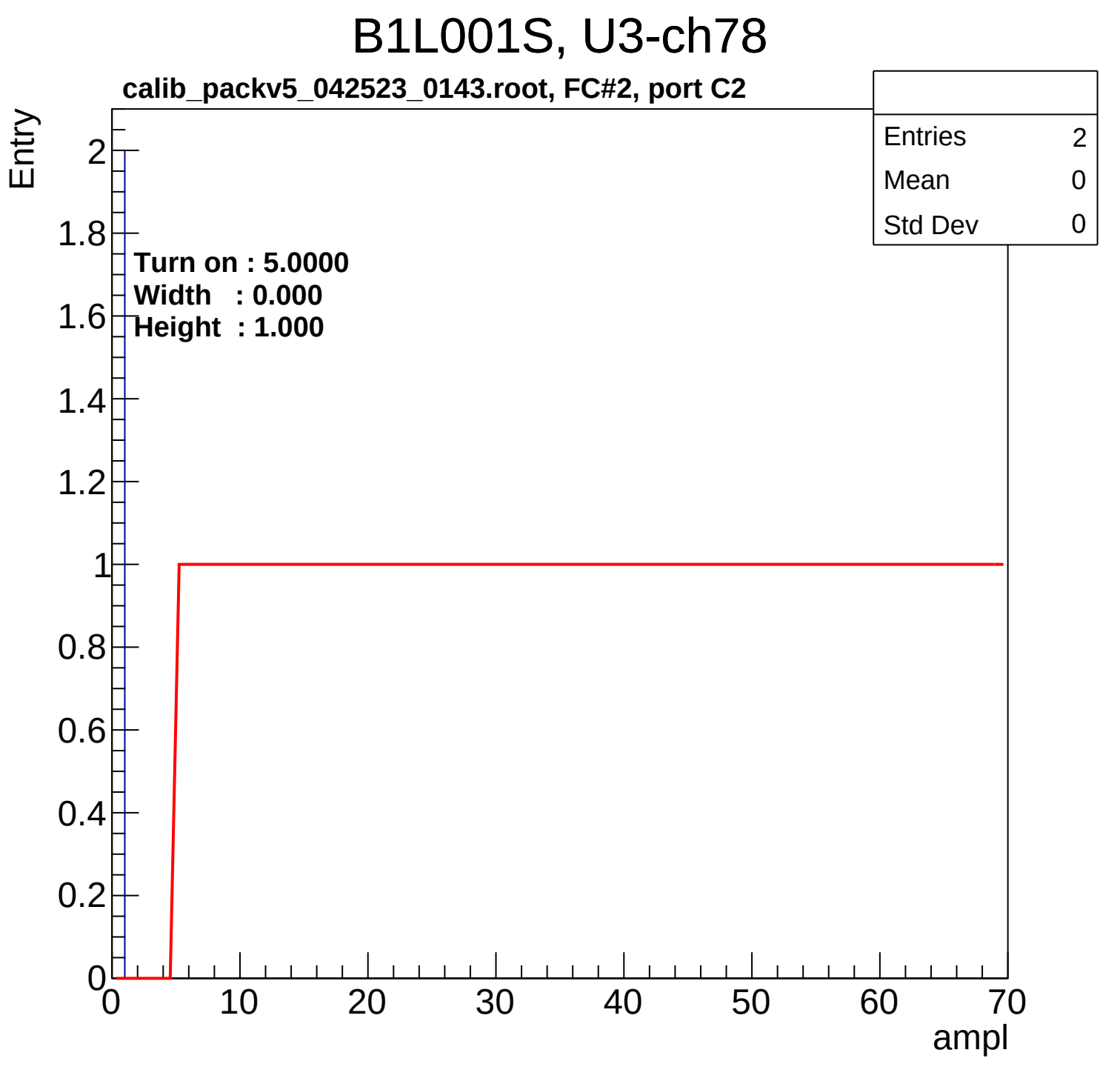

B1L001S, U3-ch73
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U3-ch74
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L001S, U3-ch75
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L001S, U3-ch76
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L001S, U3-ch77
calib_packv5_042523_0143.root, FC#2, port C2
Entries 4
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L001S, U3-ch78
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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40
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60
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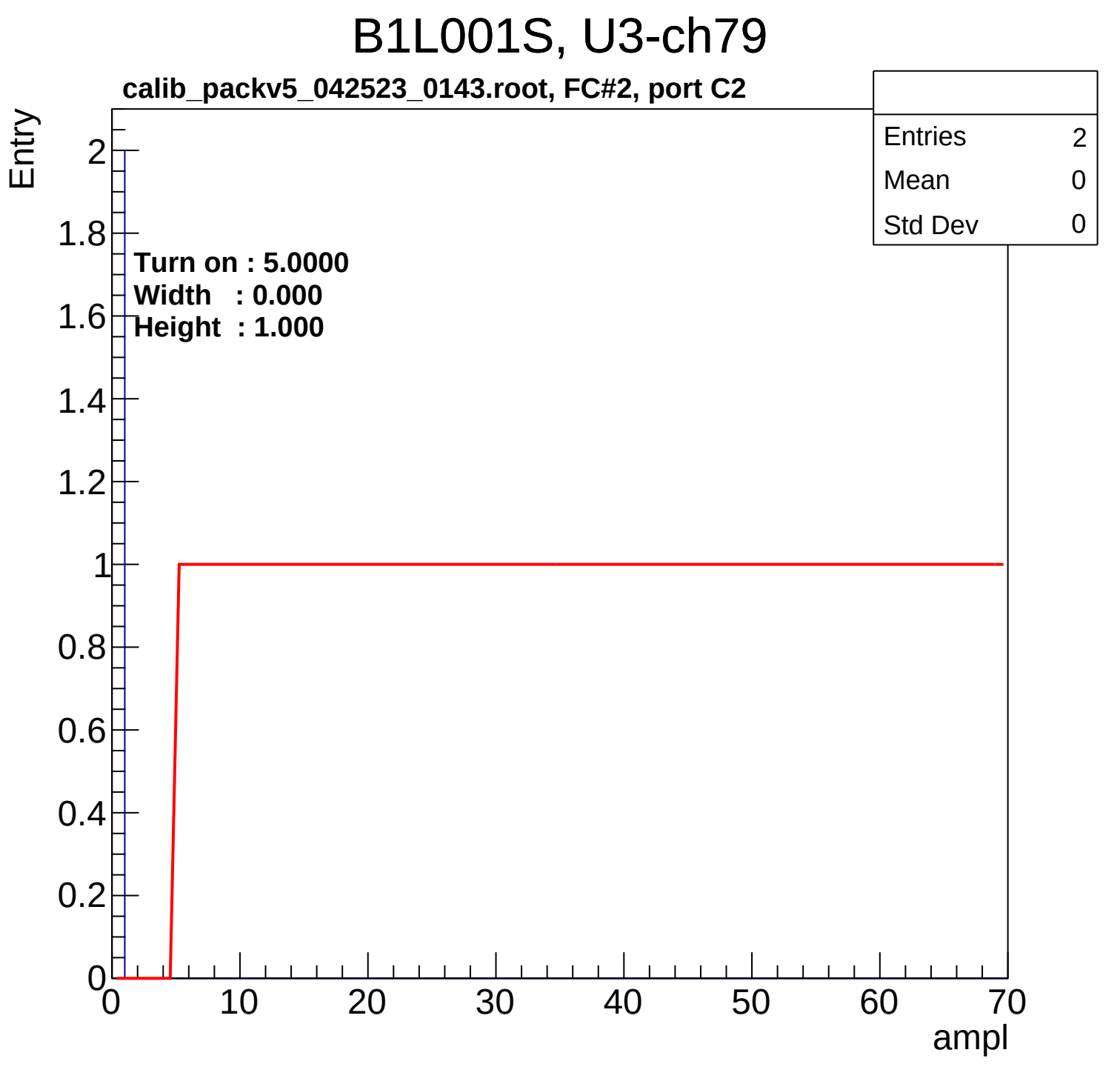
B1L001S, U3-ch79
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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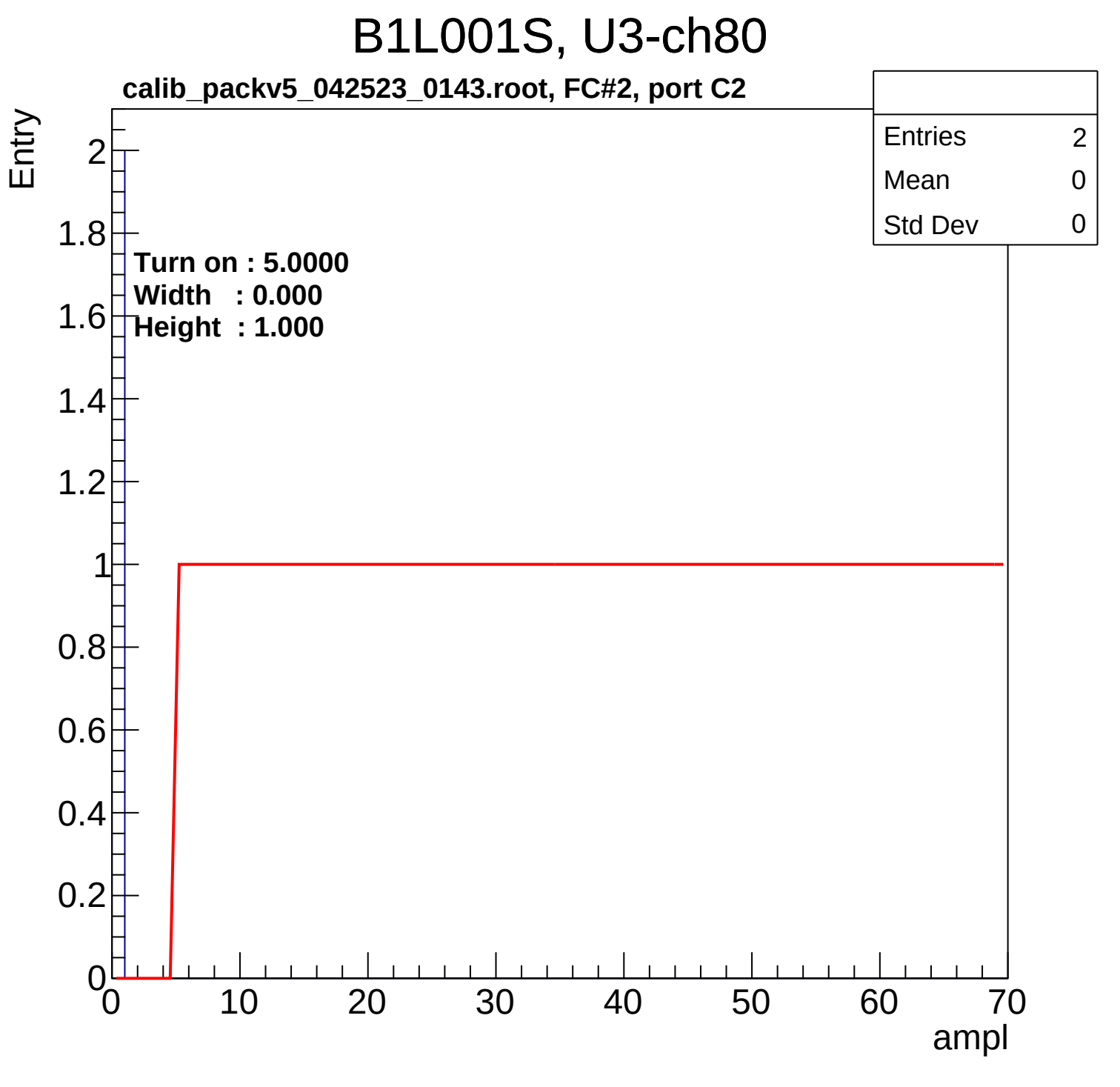
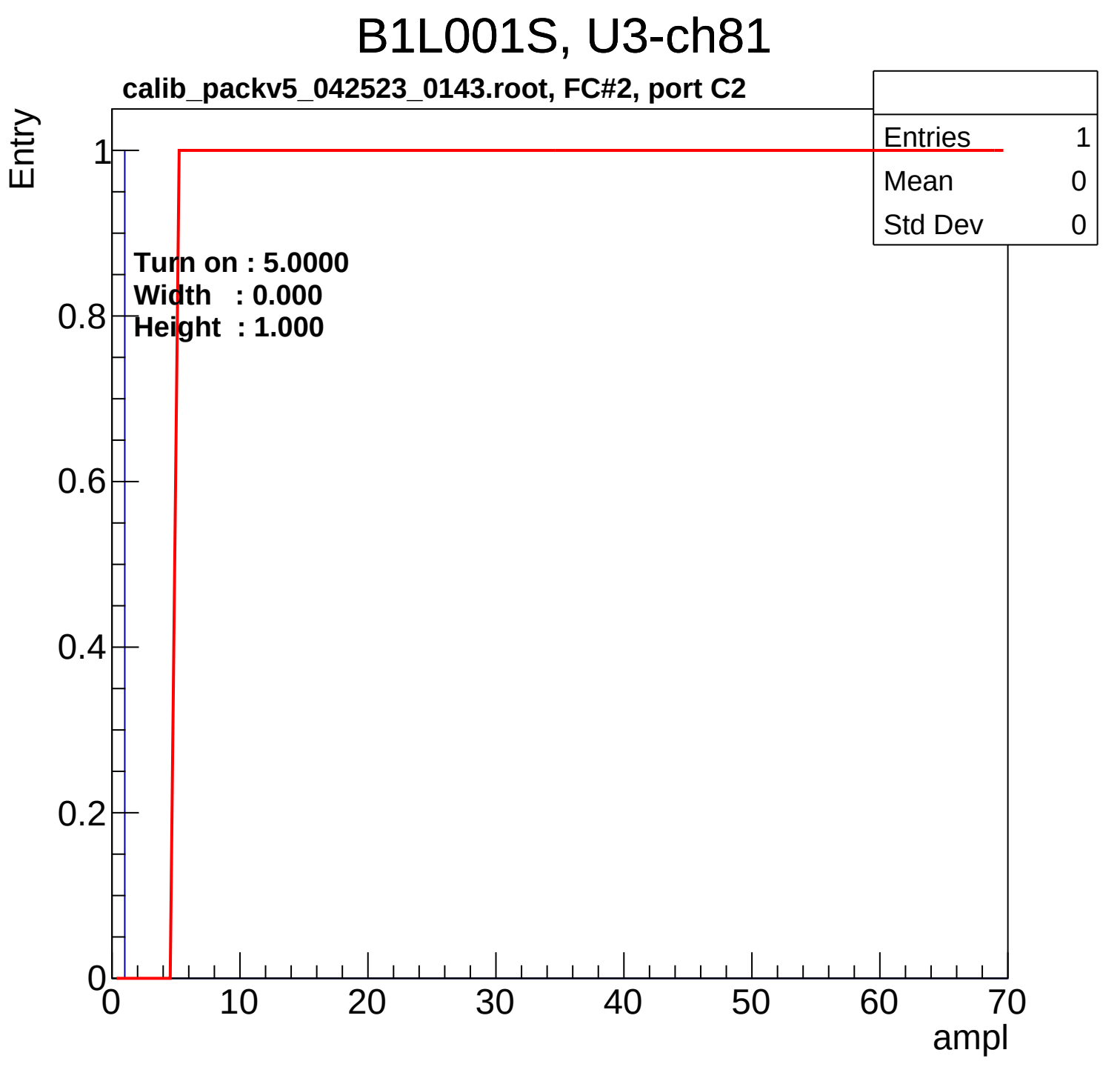
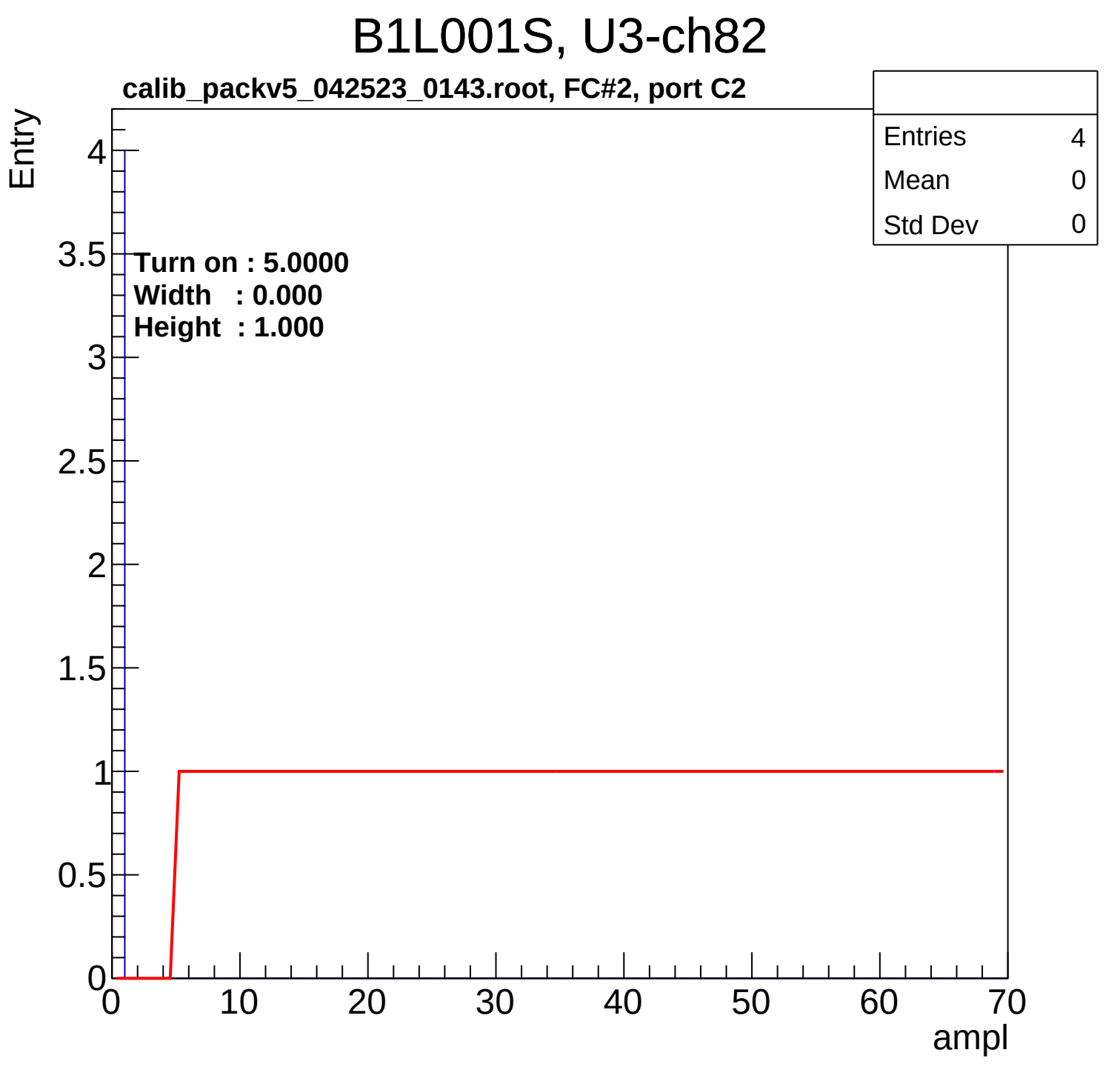
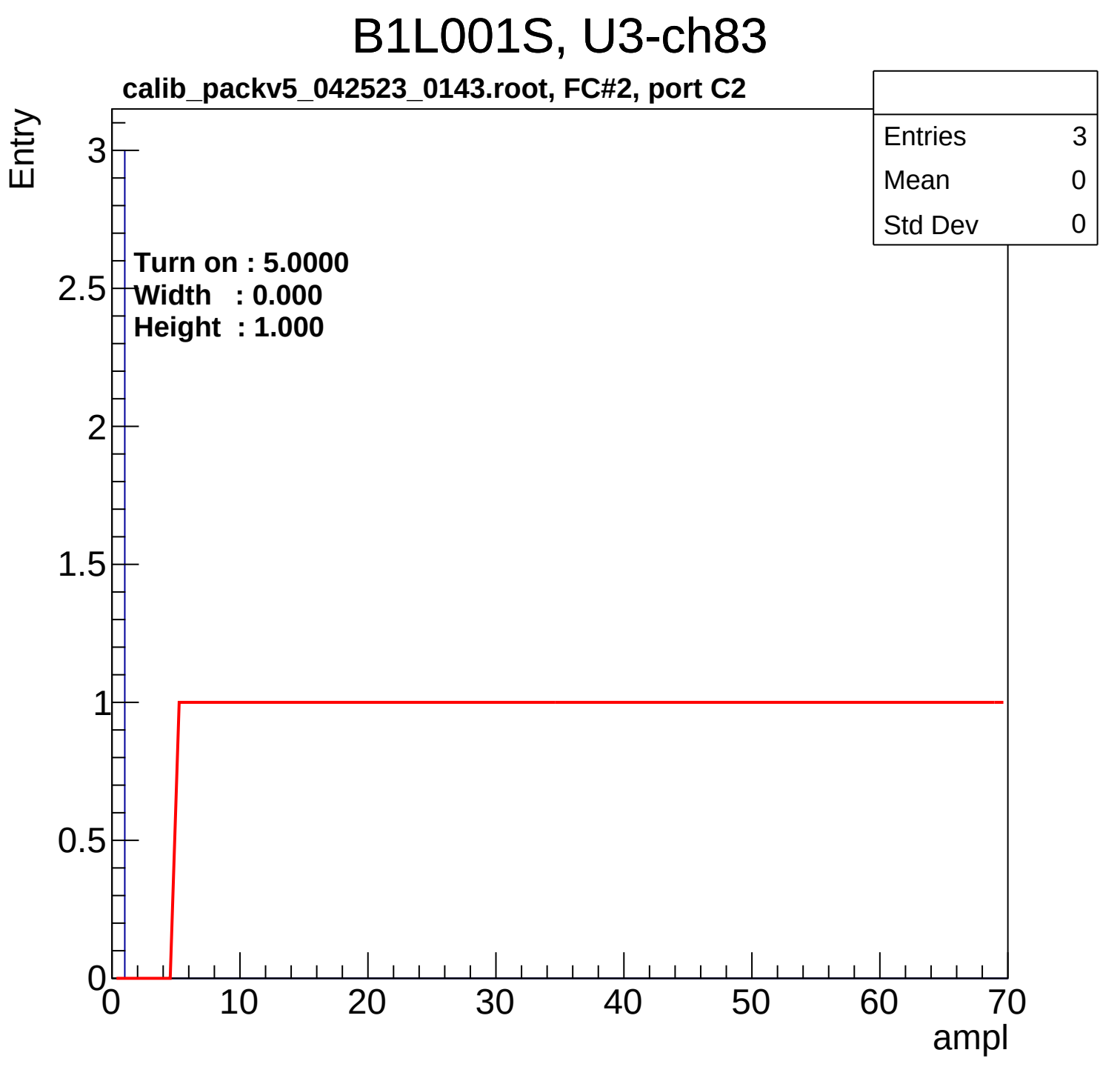

B1L001S, U3-ch80
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L001S, U3-ch81
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U3-ch82
calib_packv5_042523_0143.root, FC#2, port C2
Entries 4
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L001S, U3-ch83
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
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40
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60
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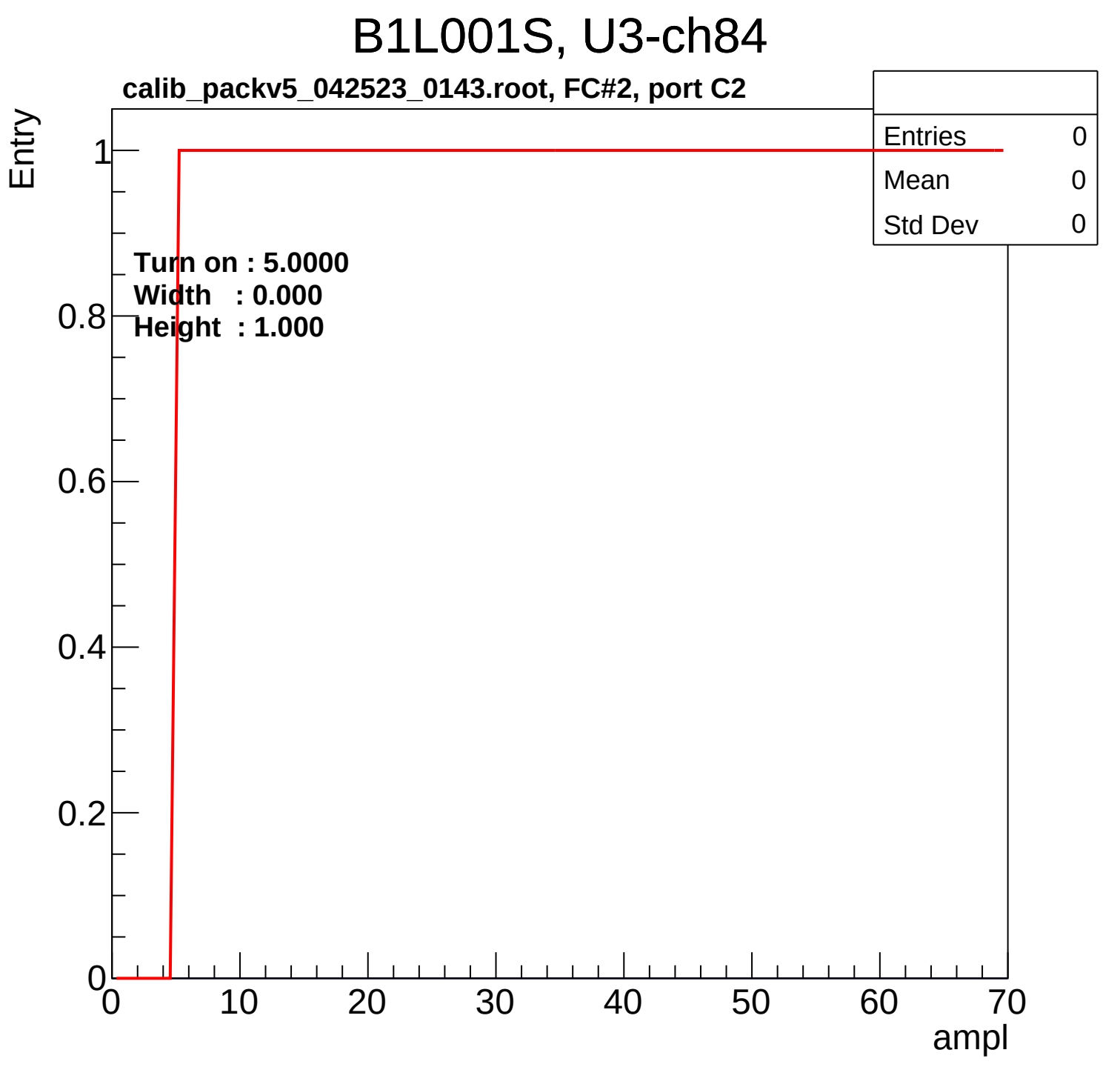
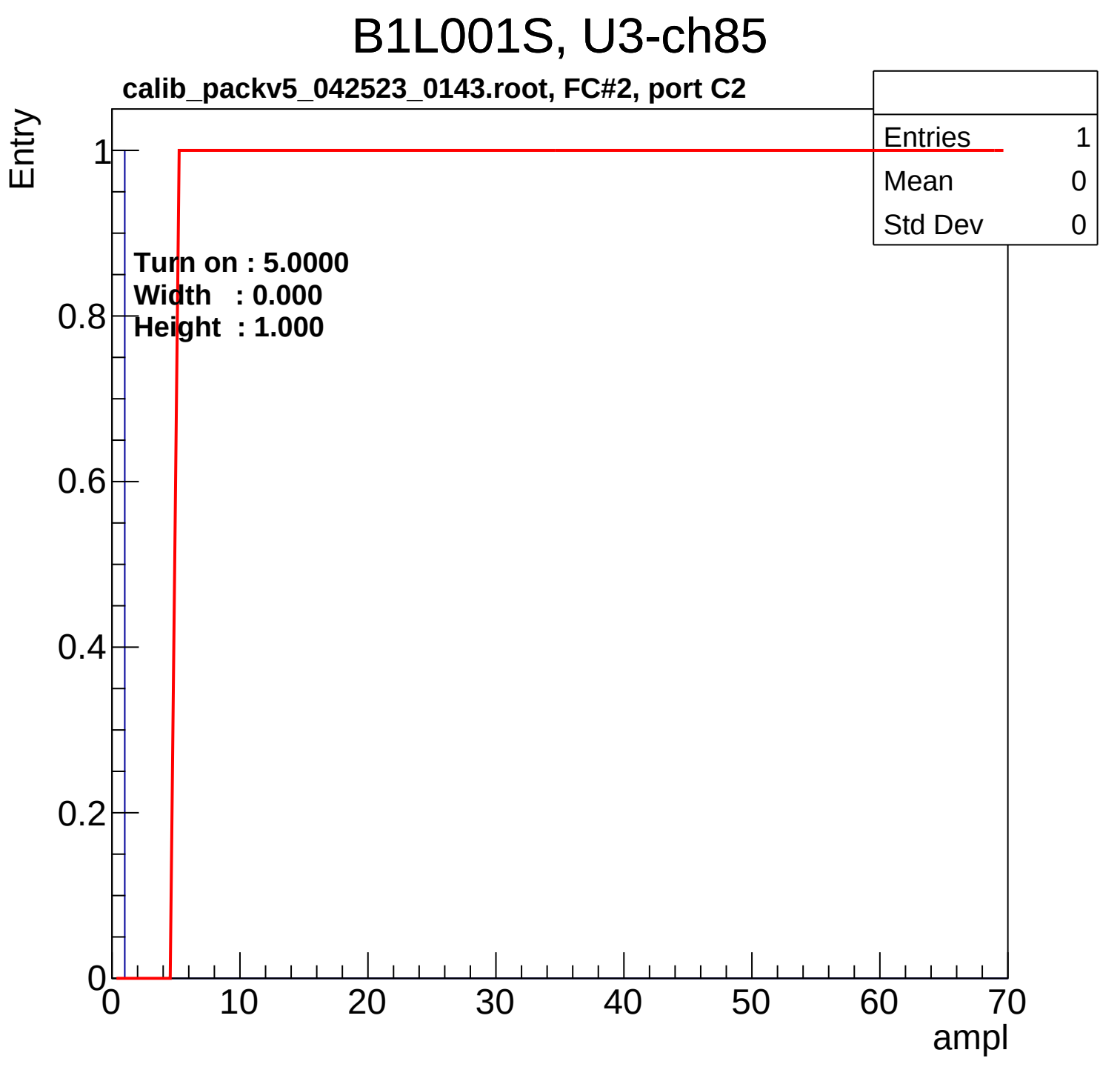
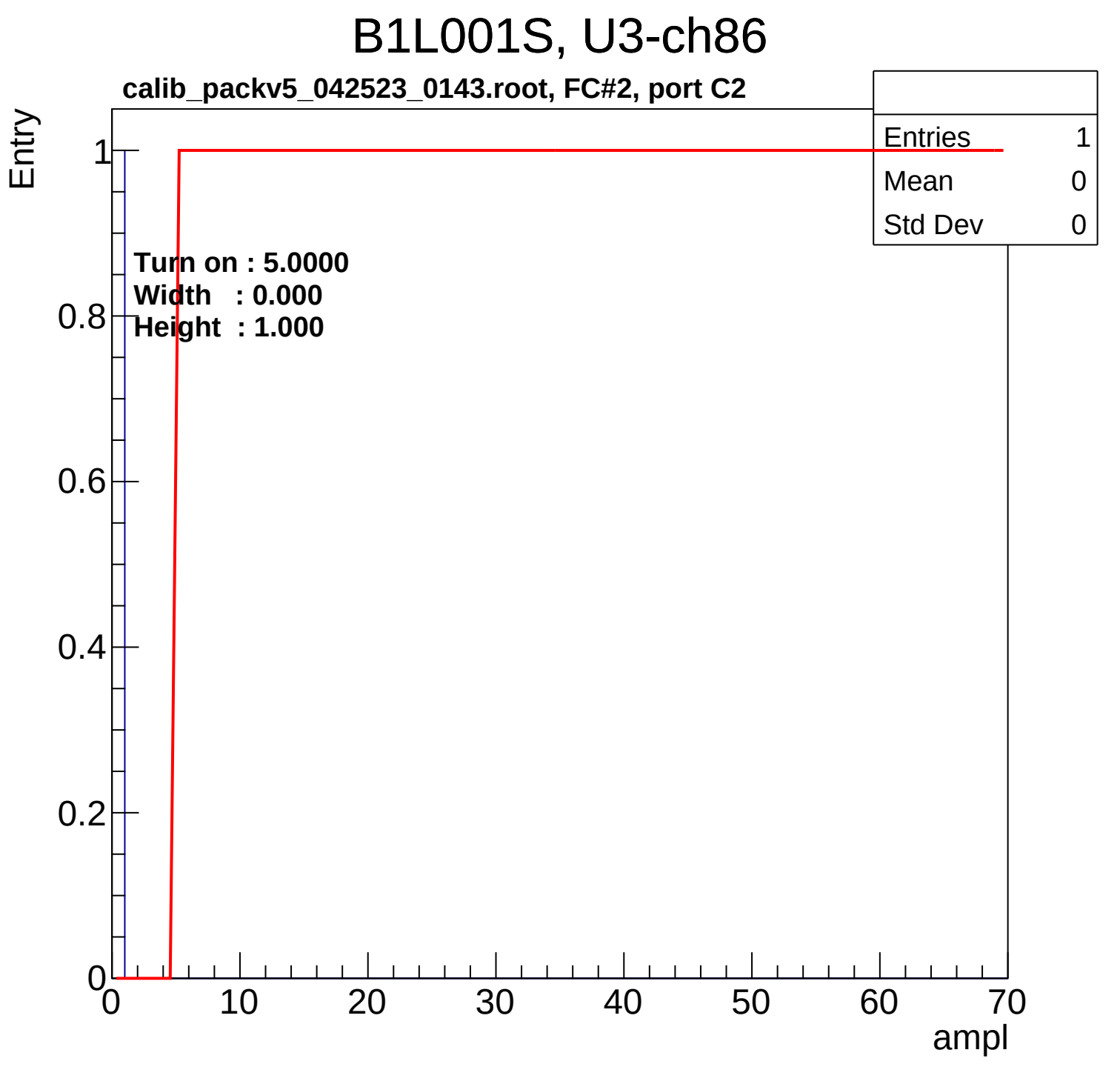
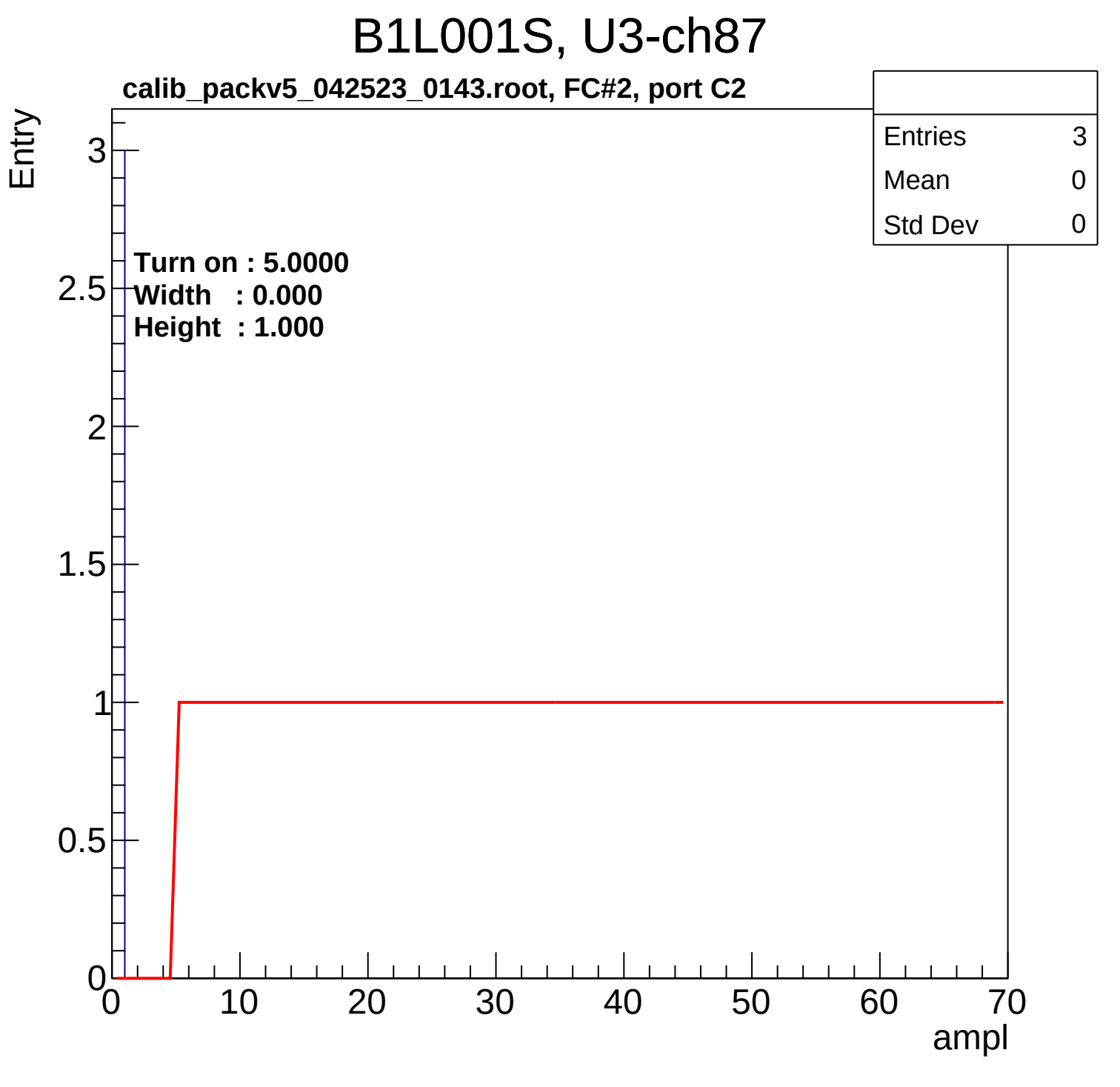
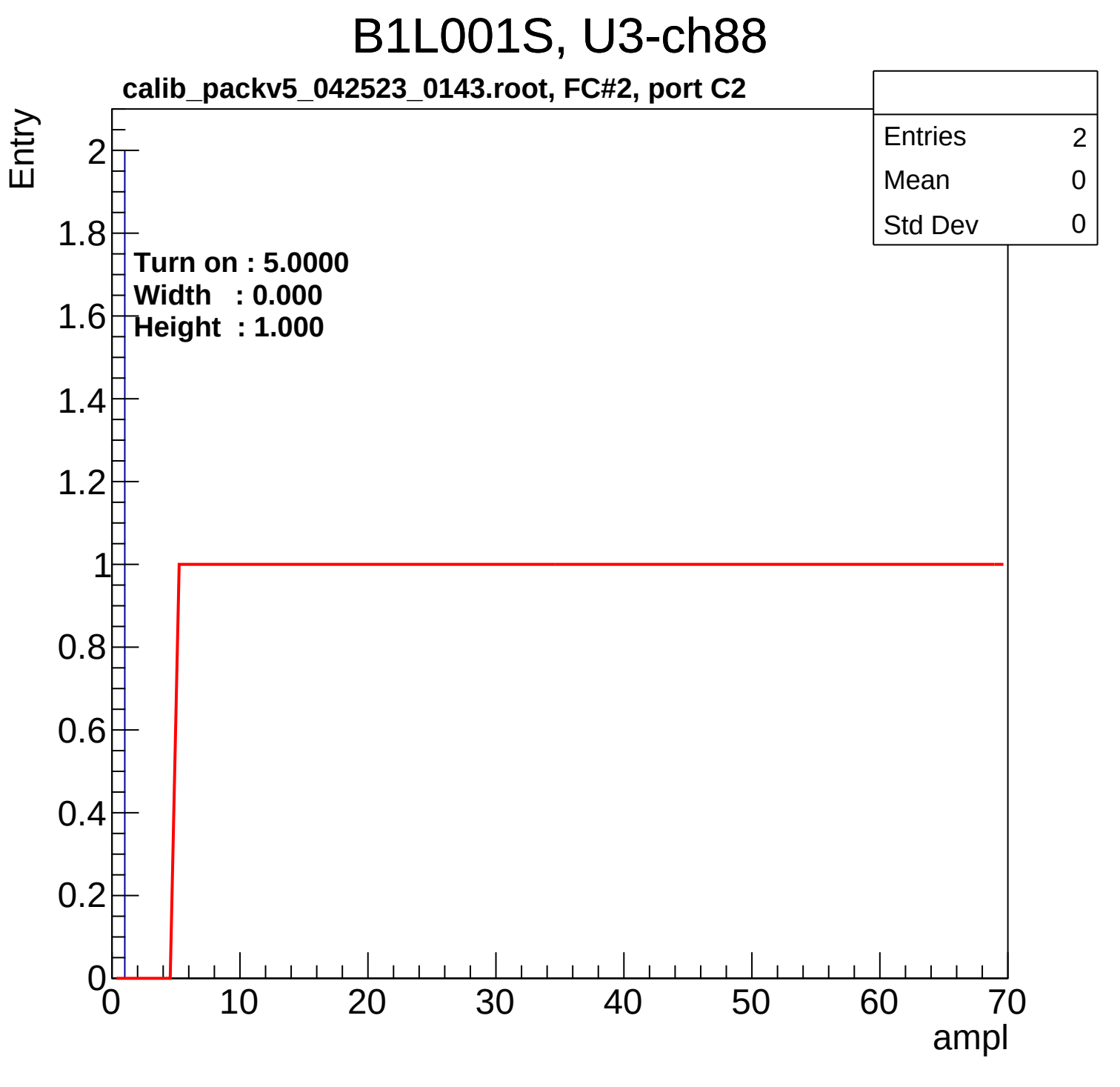

B1L001S, U3-ch84
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U3-ch85
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U3-ch86
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U3-ch87
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L001S, U3-ch88
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
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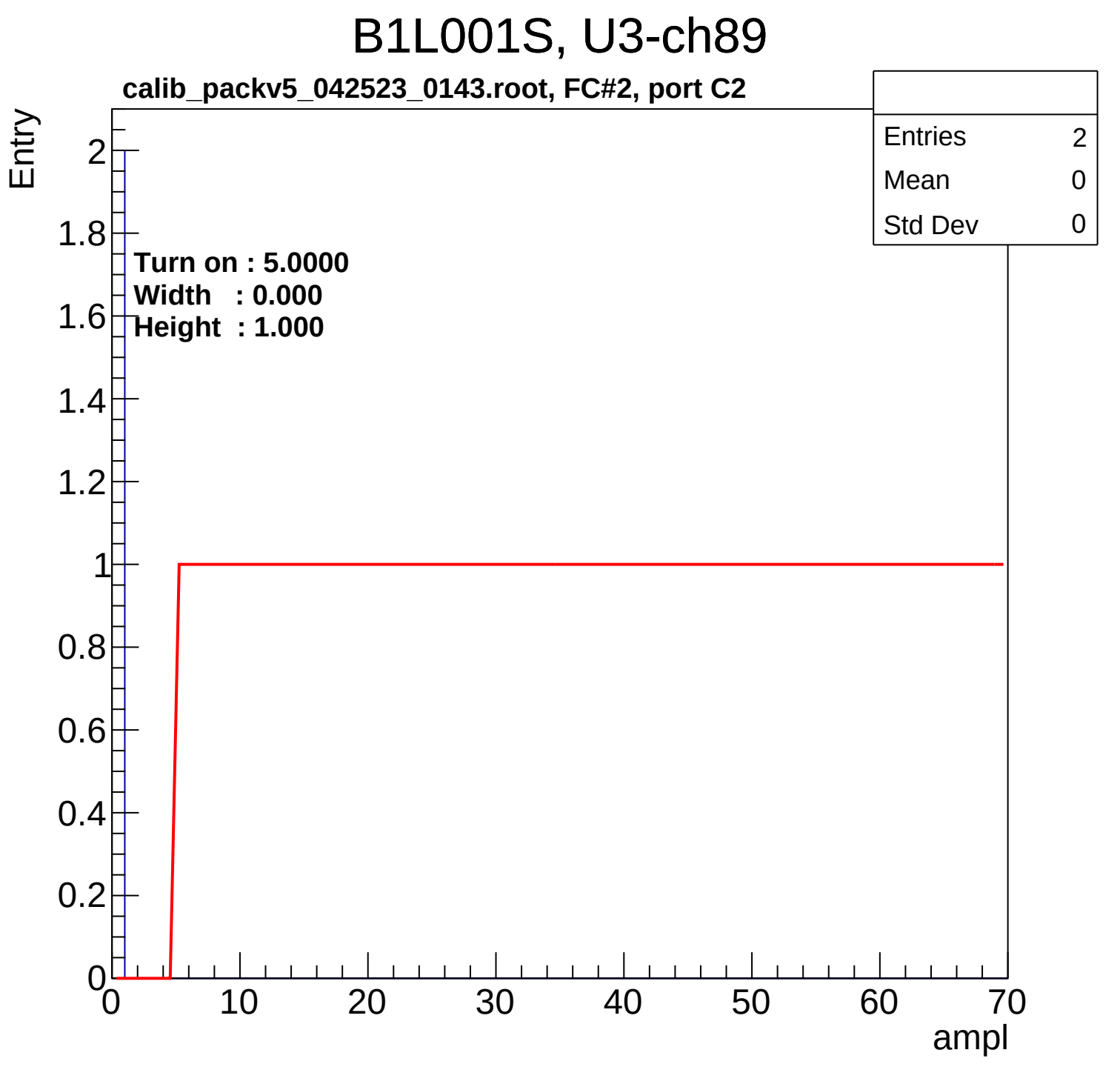
60
70


B1L001S, U3-ch89
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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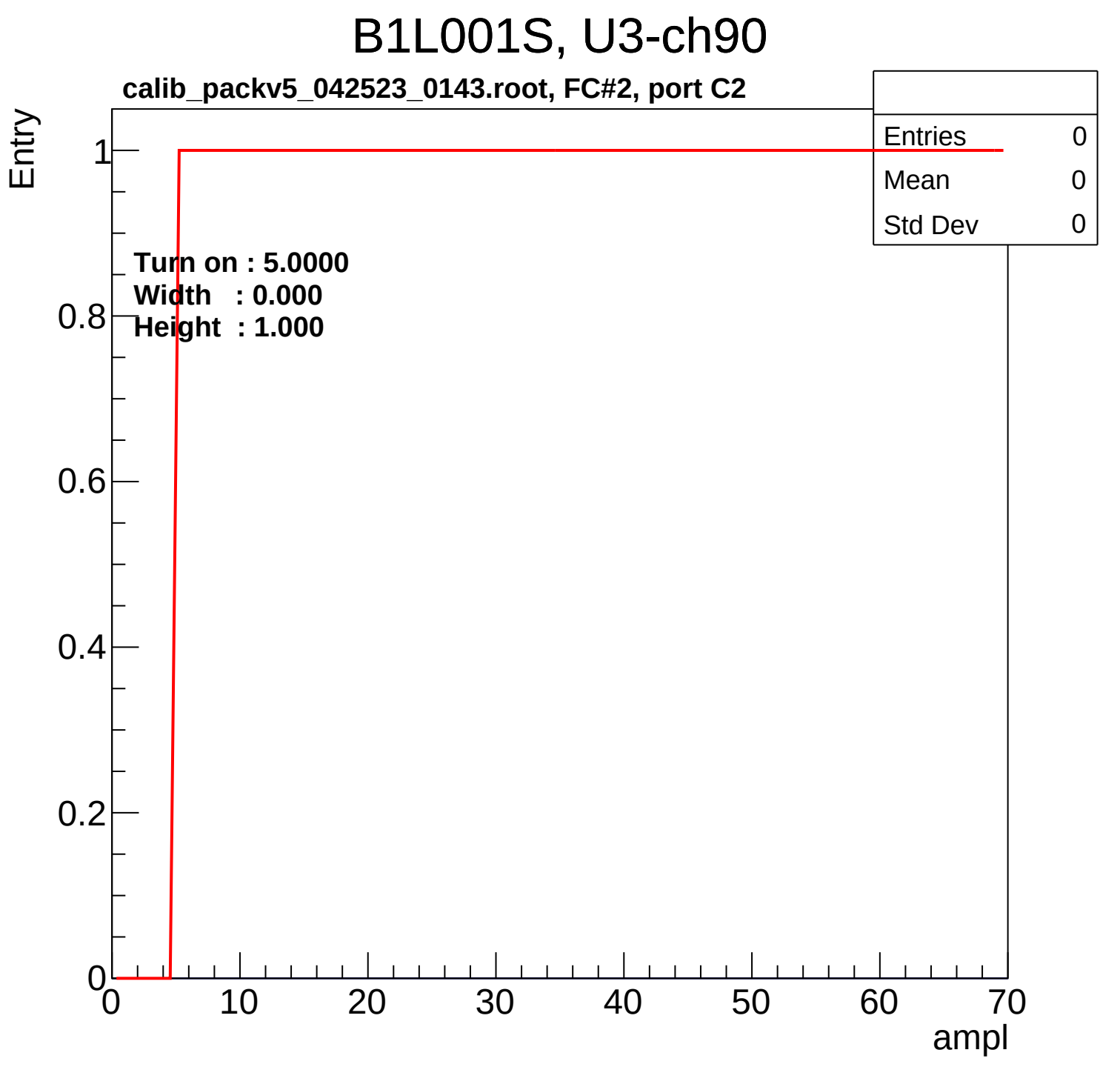
B1L001S, U3-ch90
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
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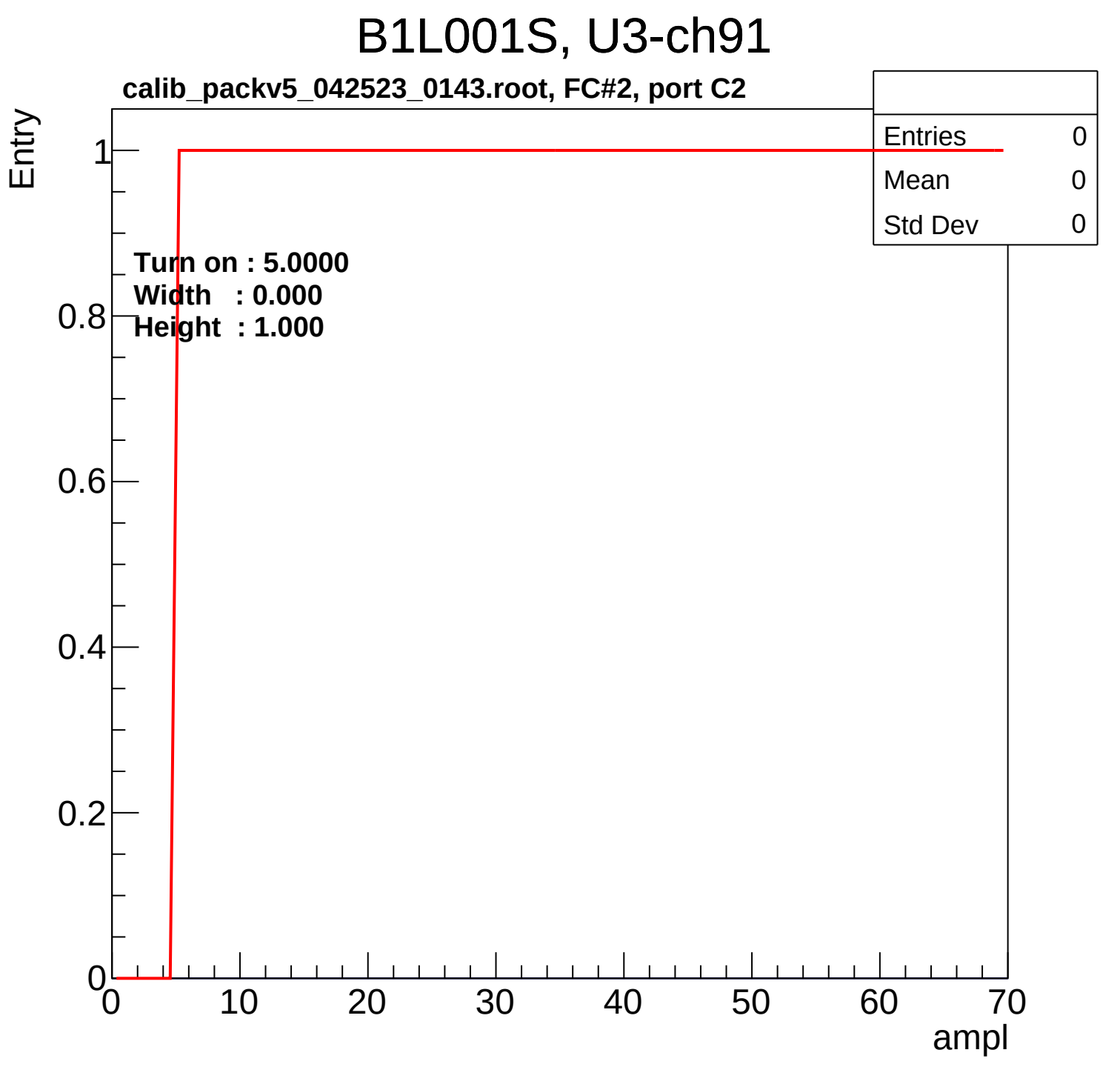
50
60
70
ampl


B1L001S, U3-ch91
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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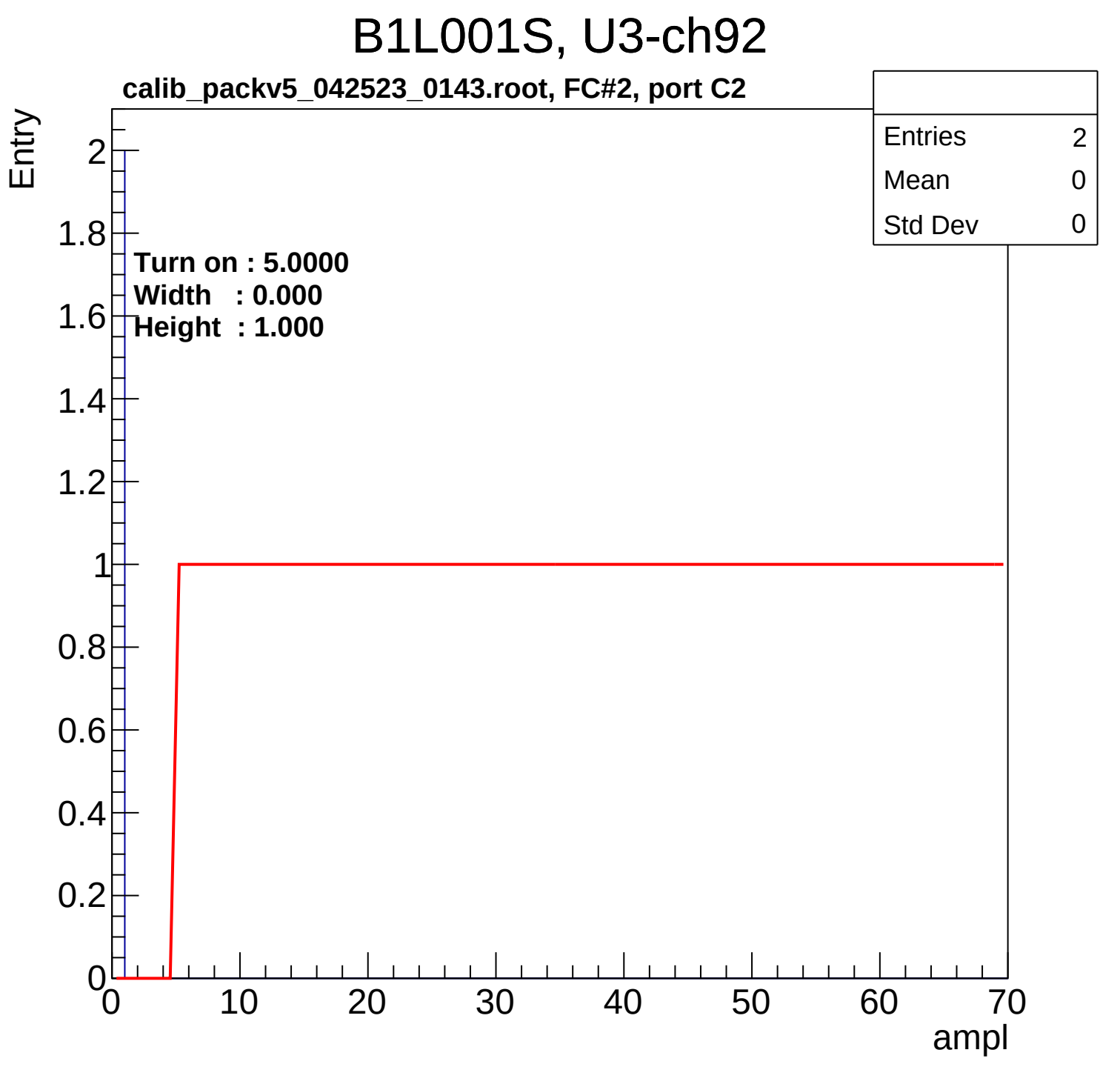
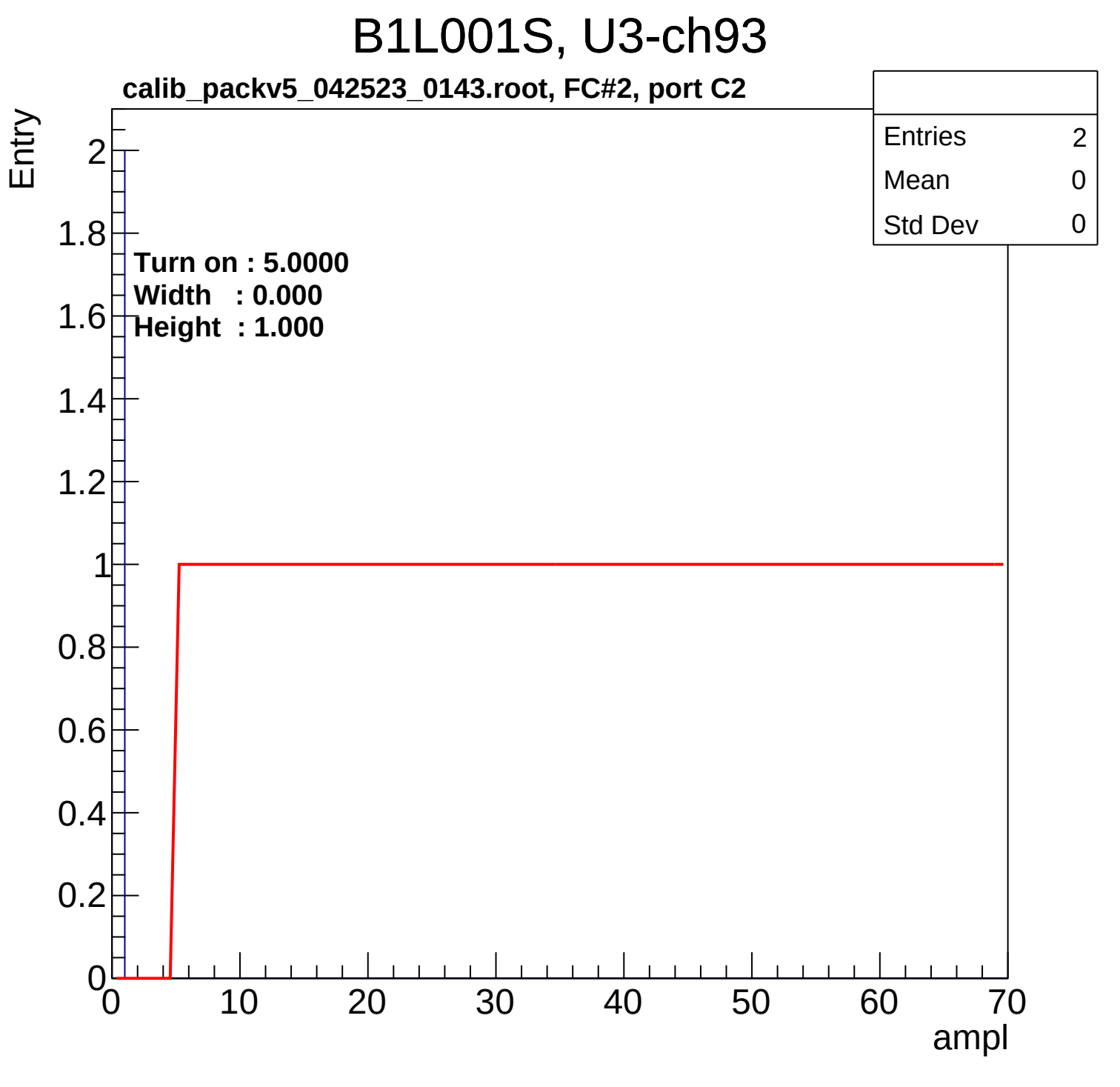
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U3-ch92
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L001S, U3-ch93
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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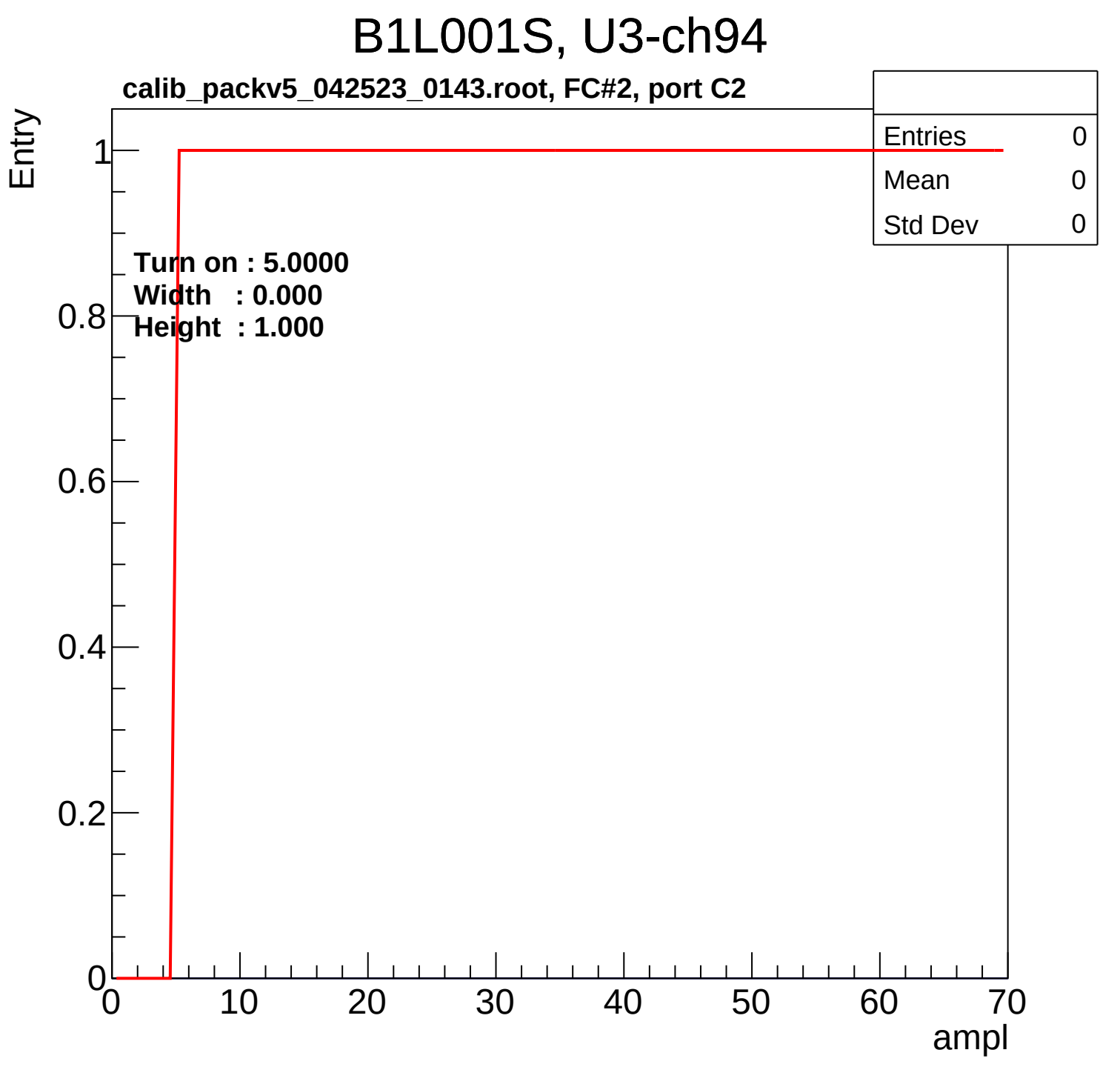
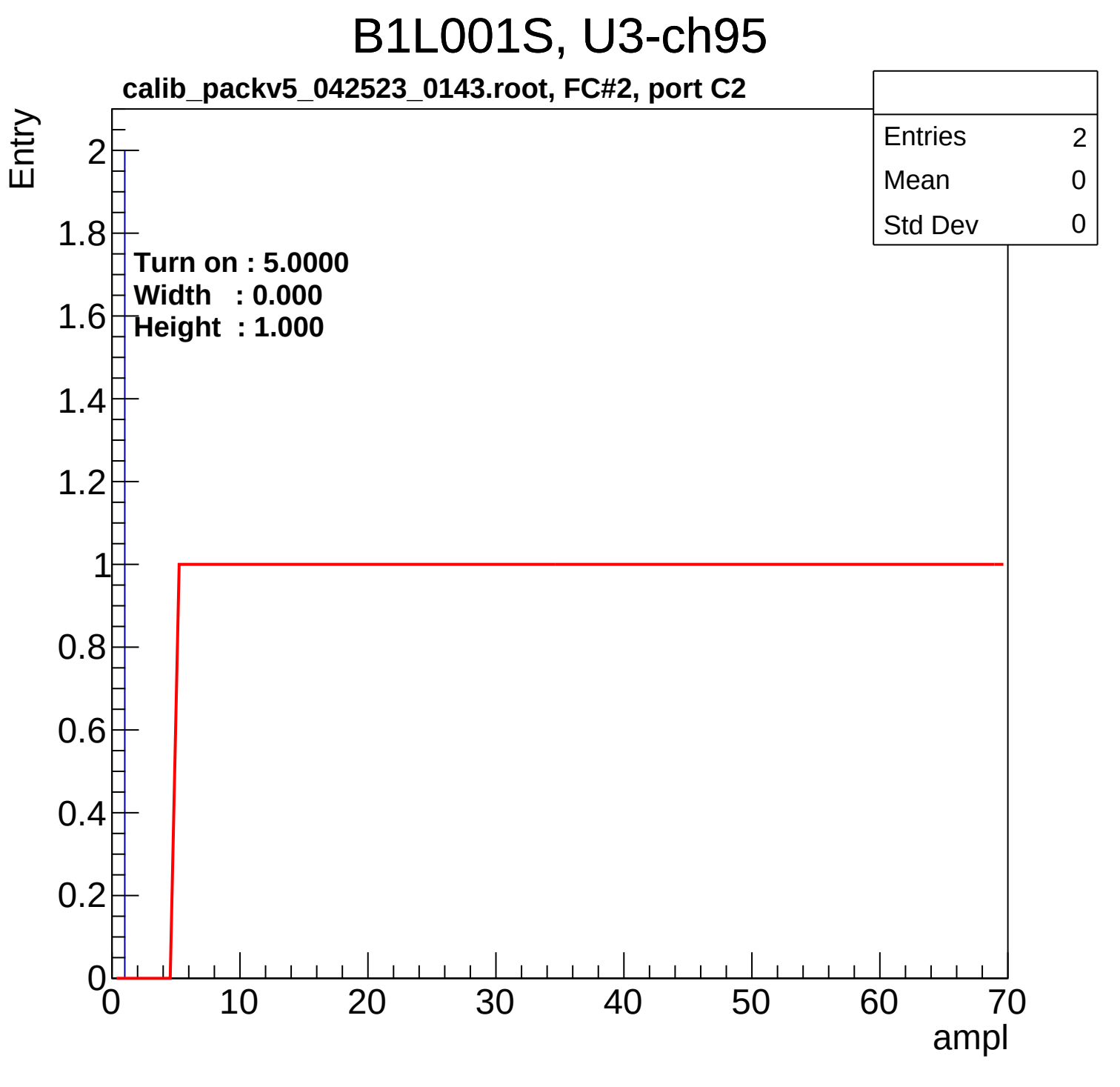
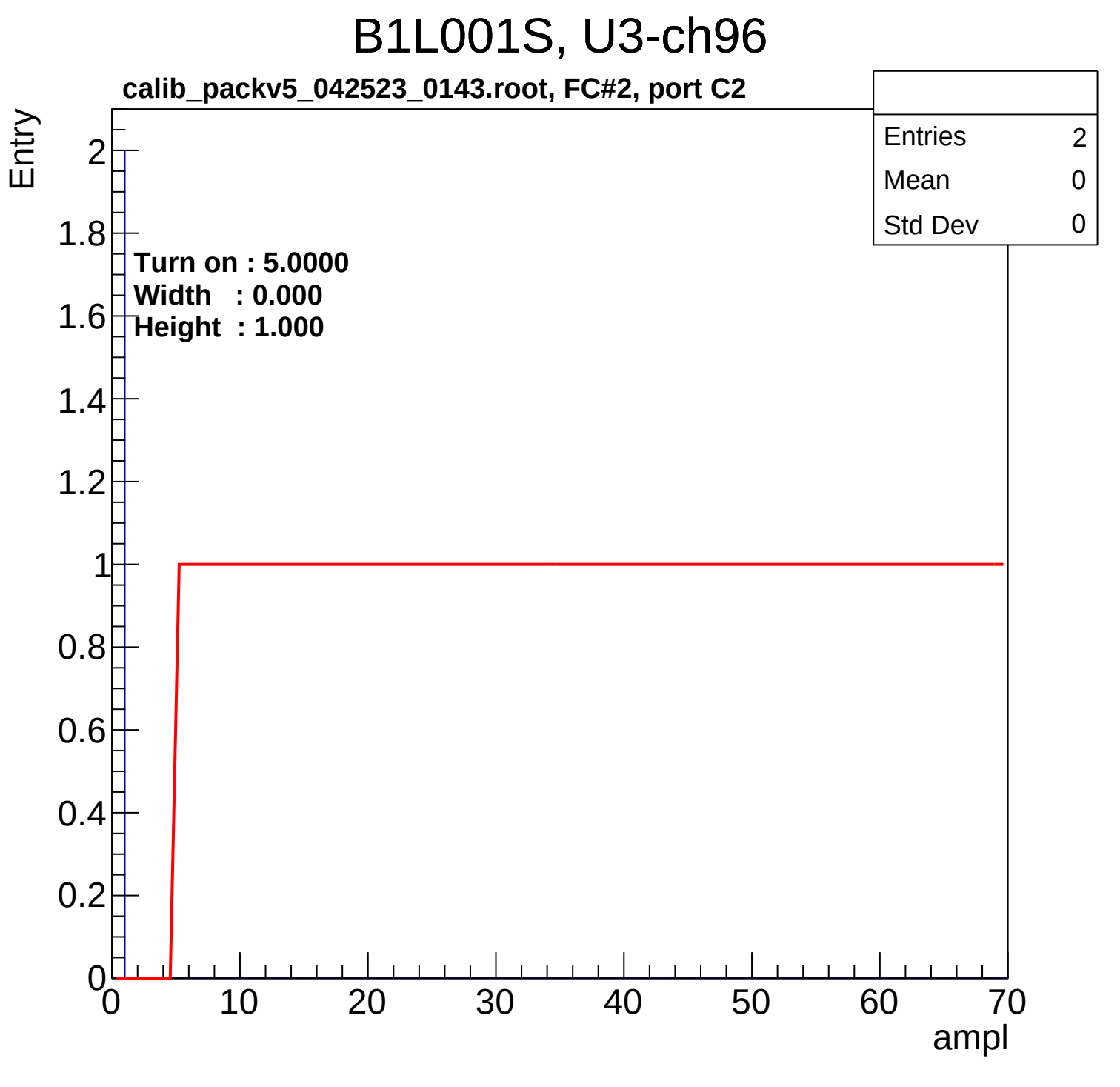
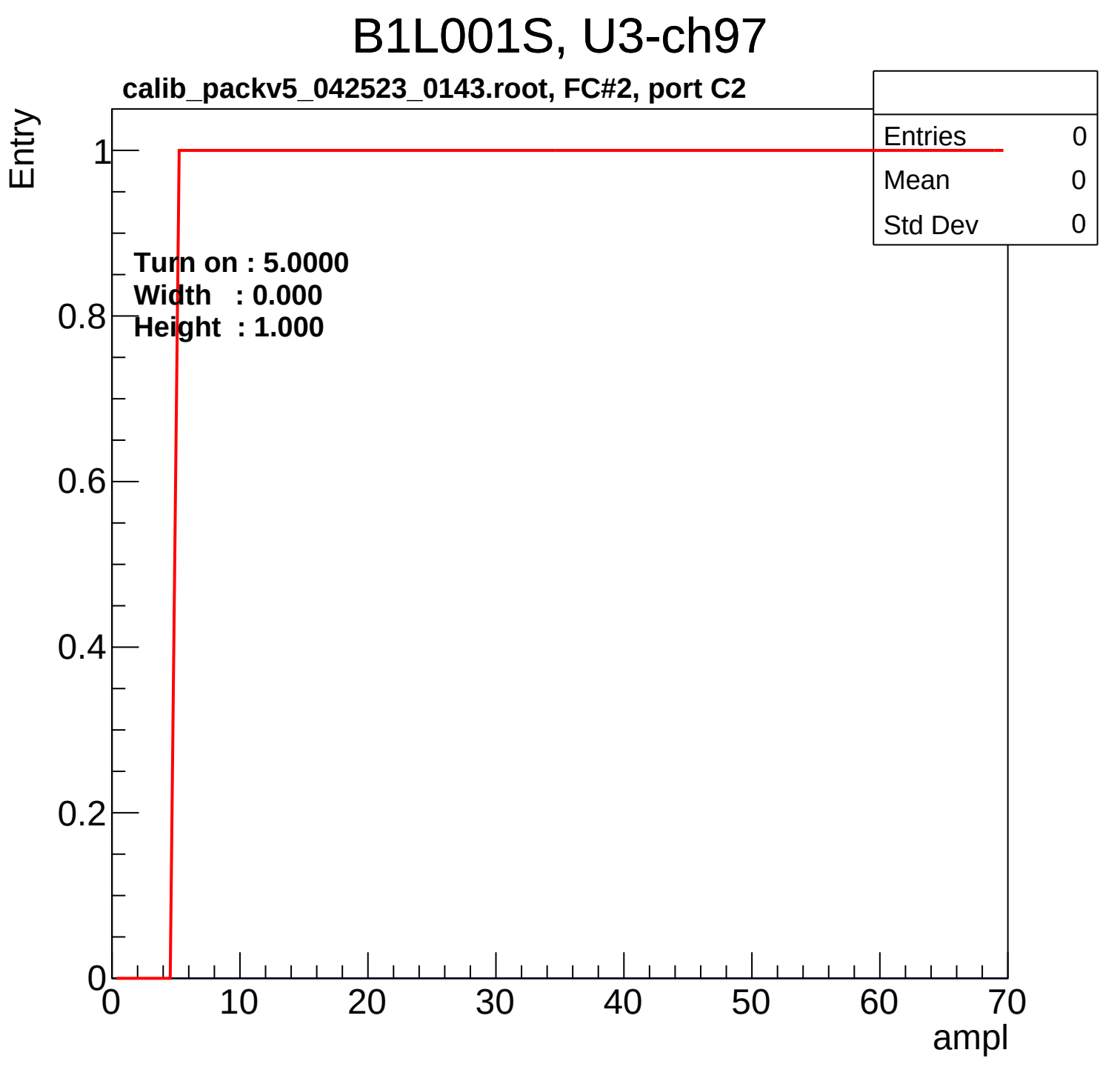
40
50
60
70


B1L001S, U3-ch94
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U3-ch95
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L001S, U3-ch96
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L001S, U3-ch97
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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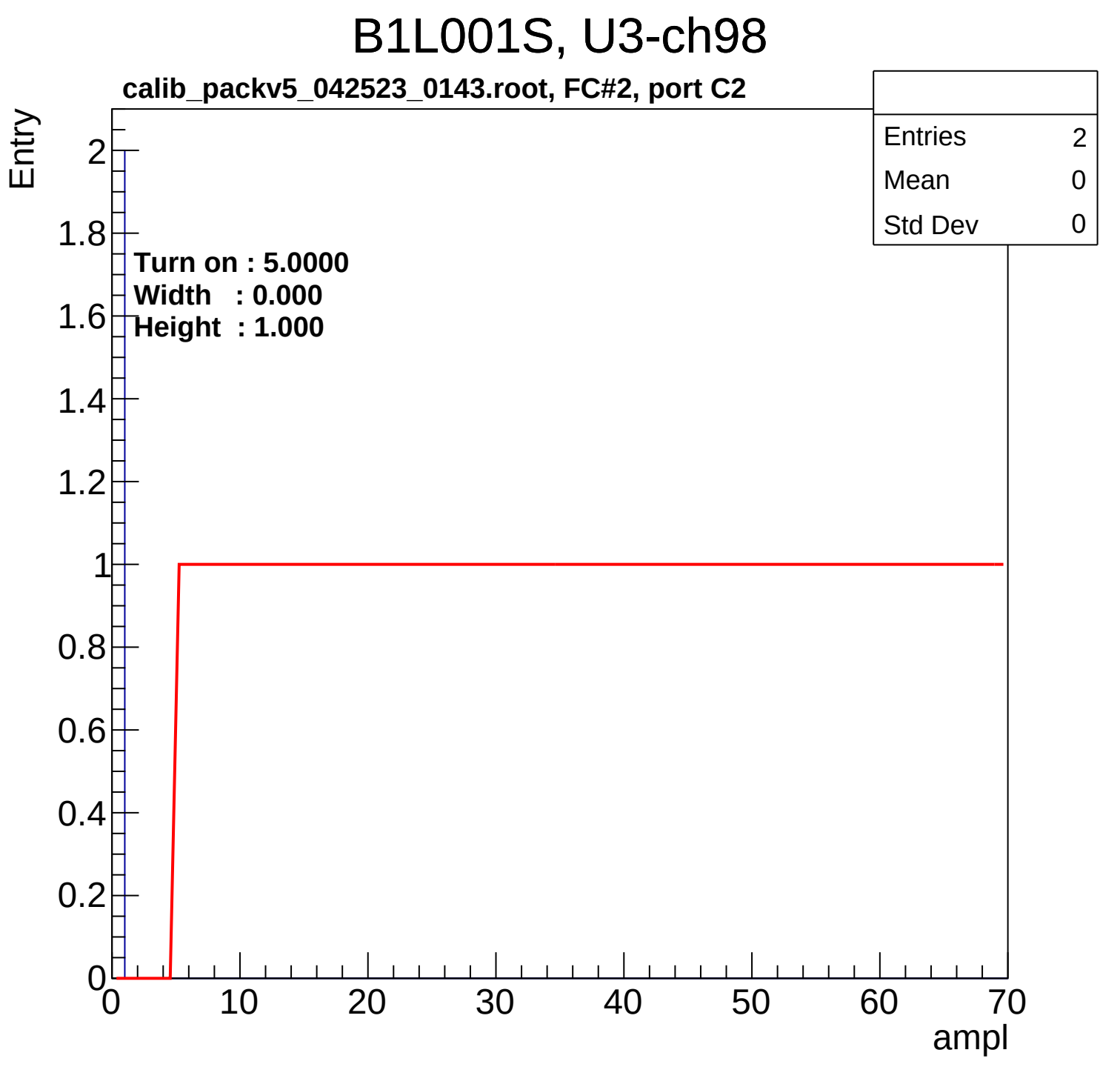
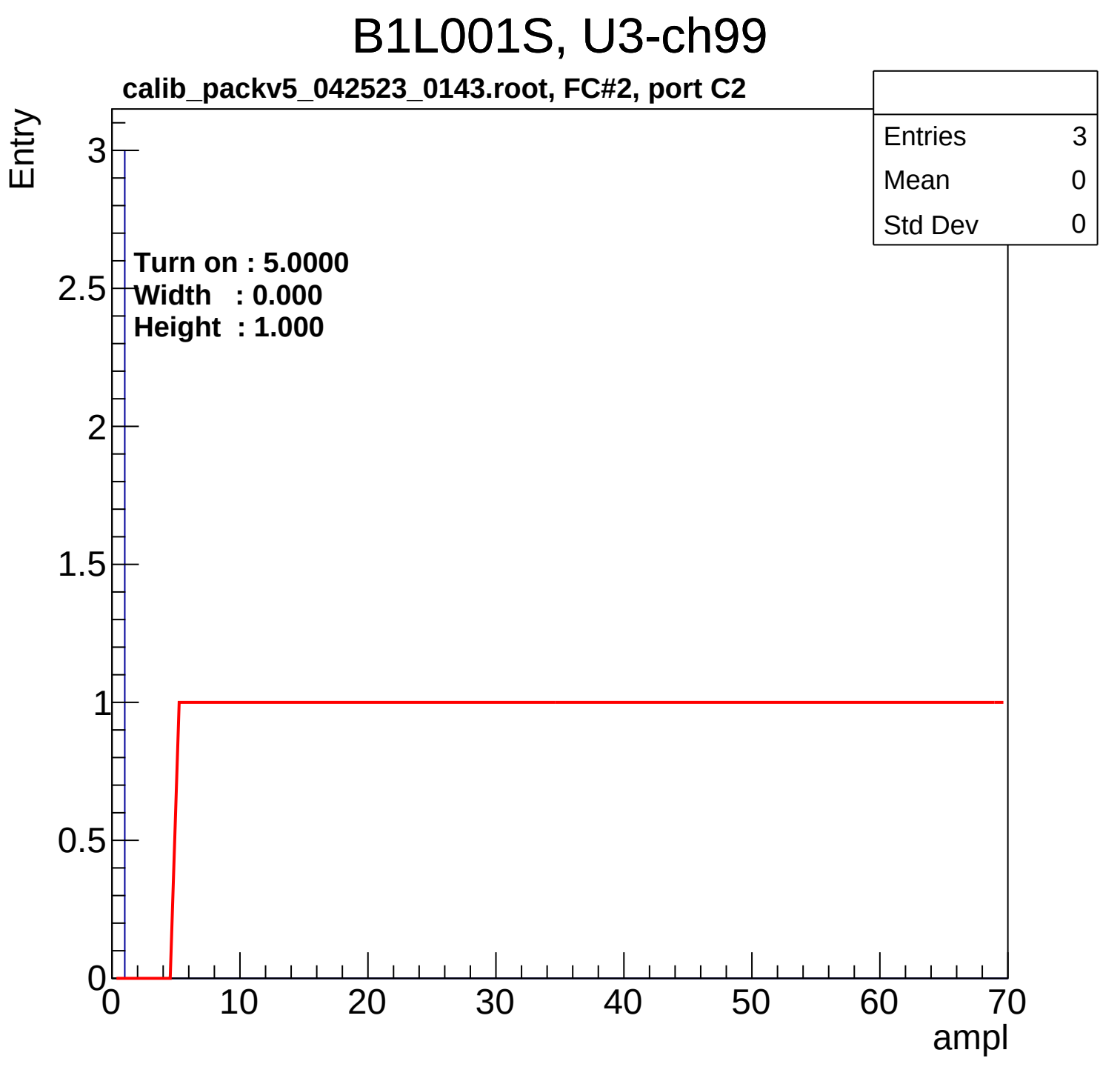
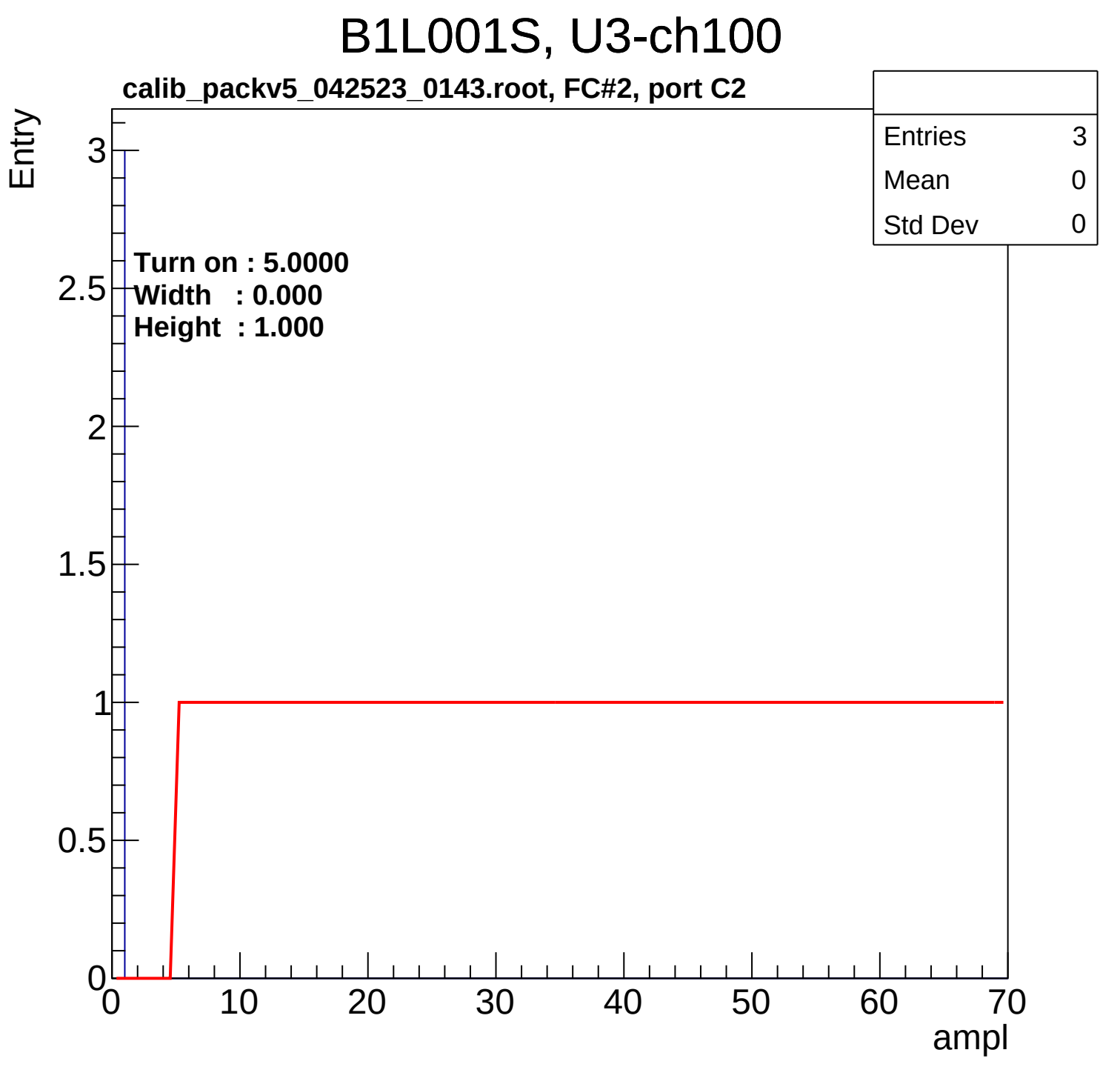
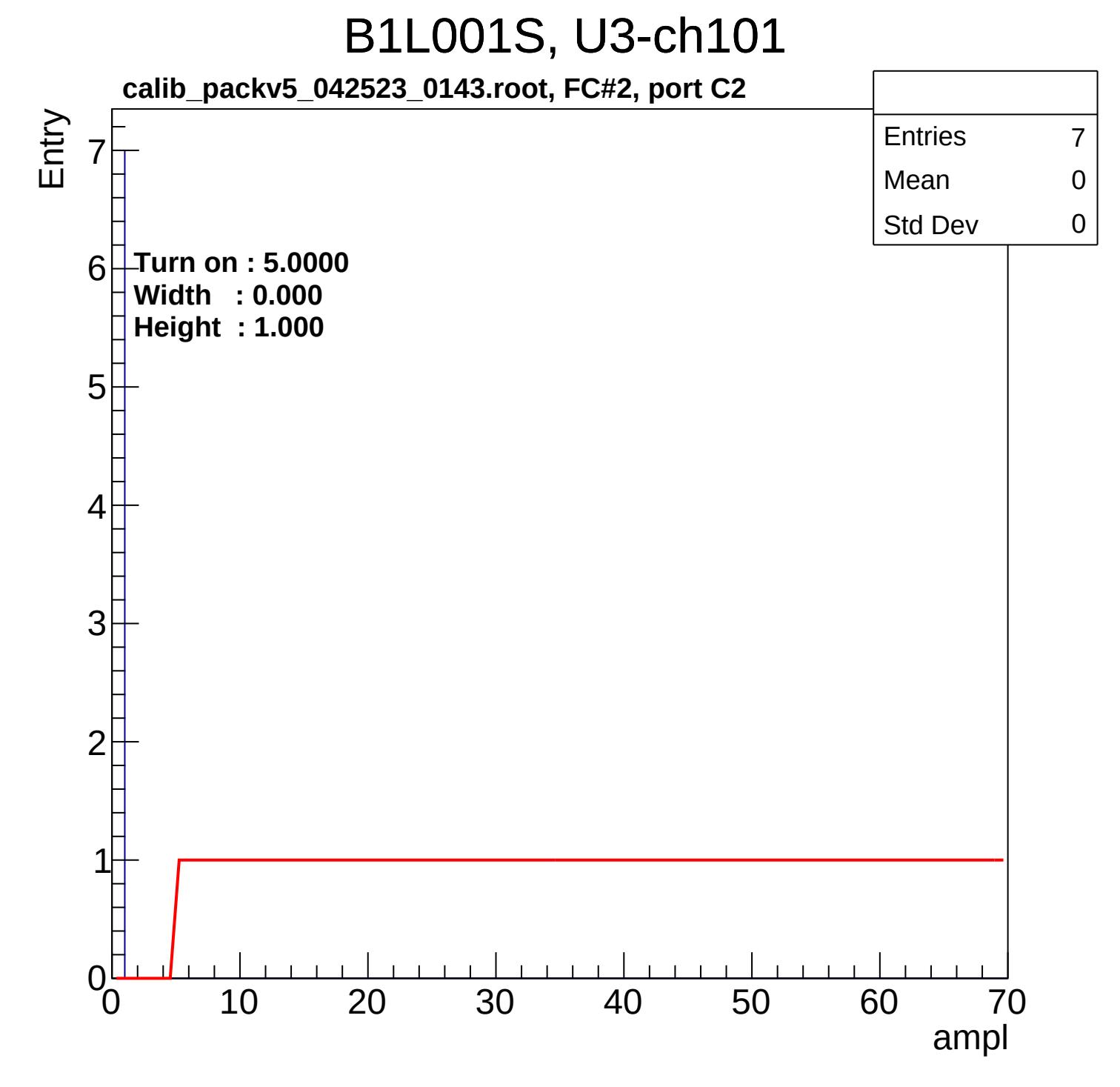
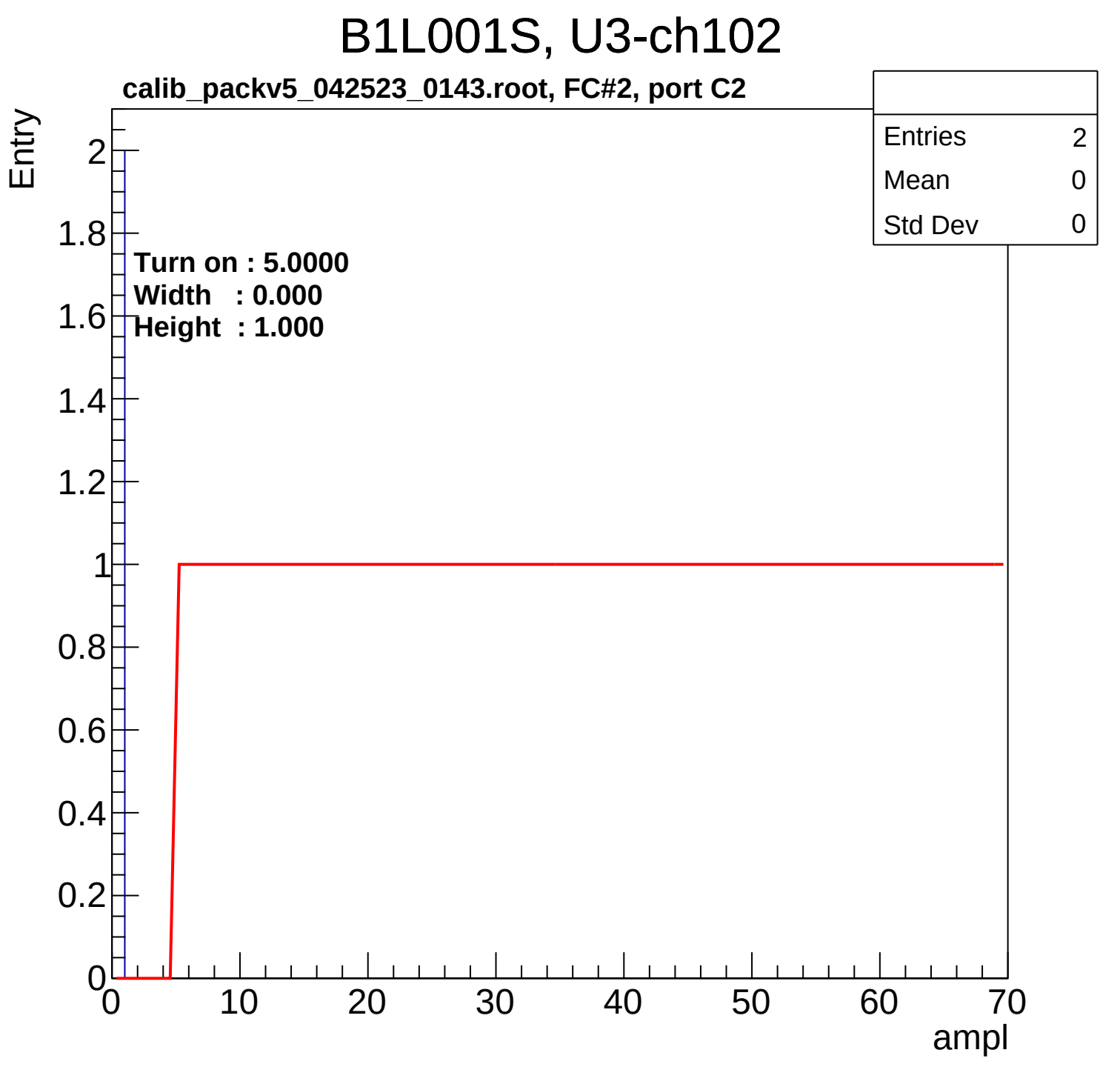
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

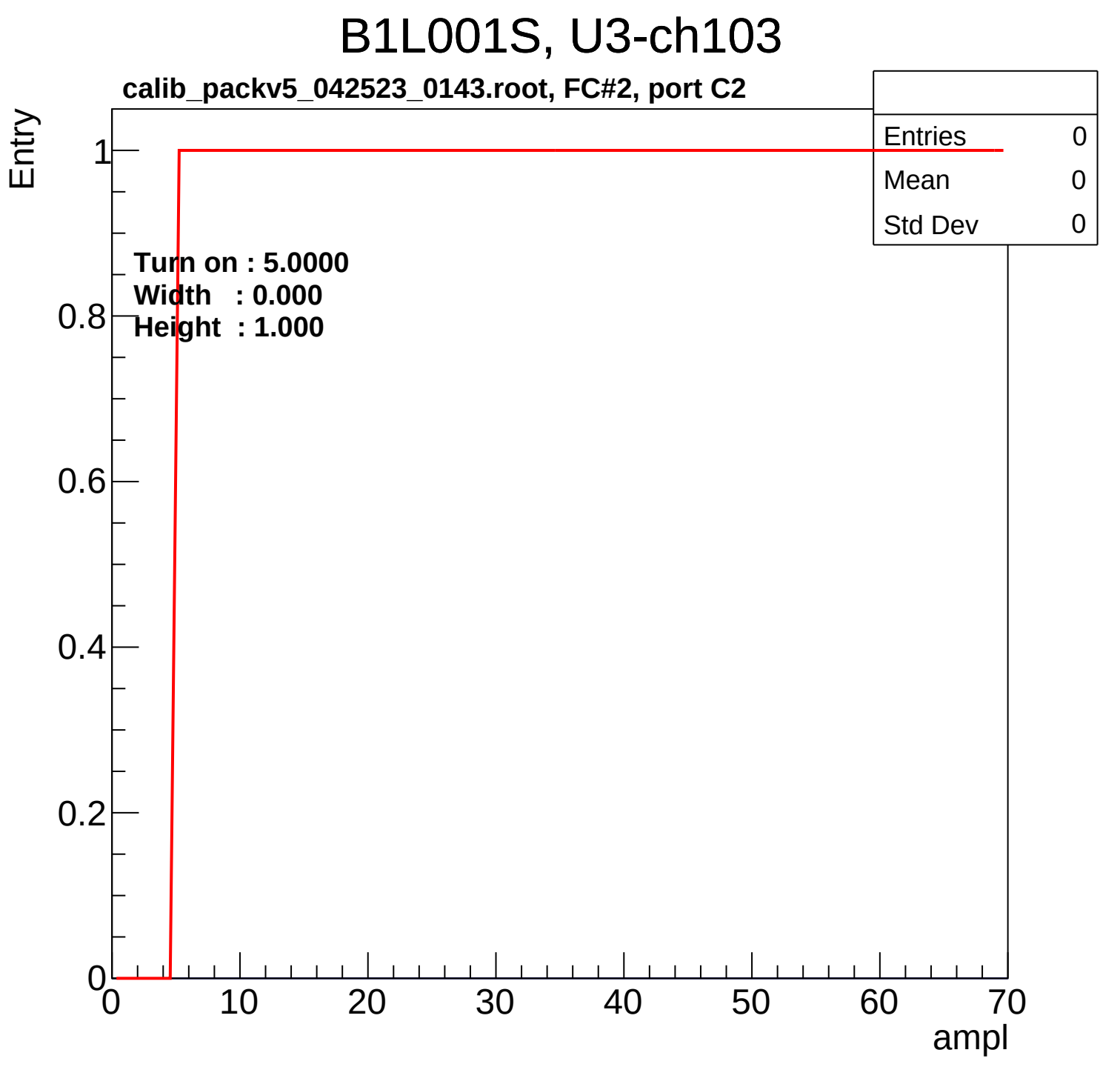

B1L001S, U3-ch98
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

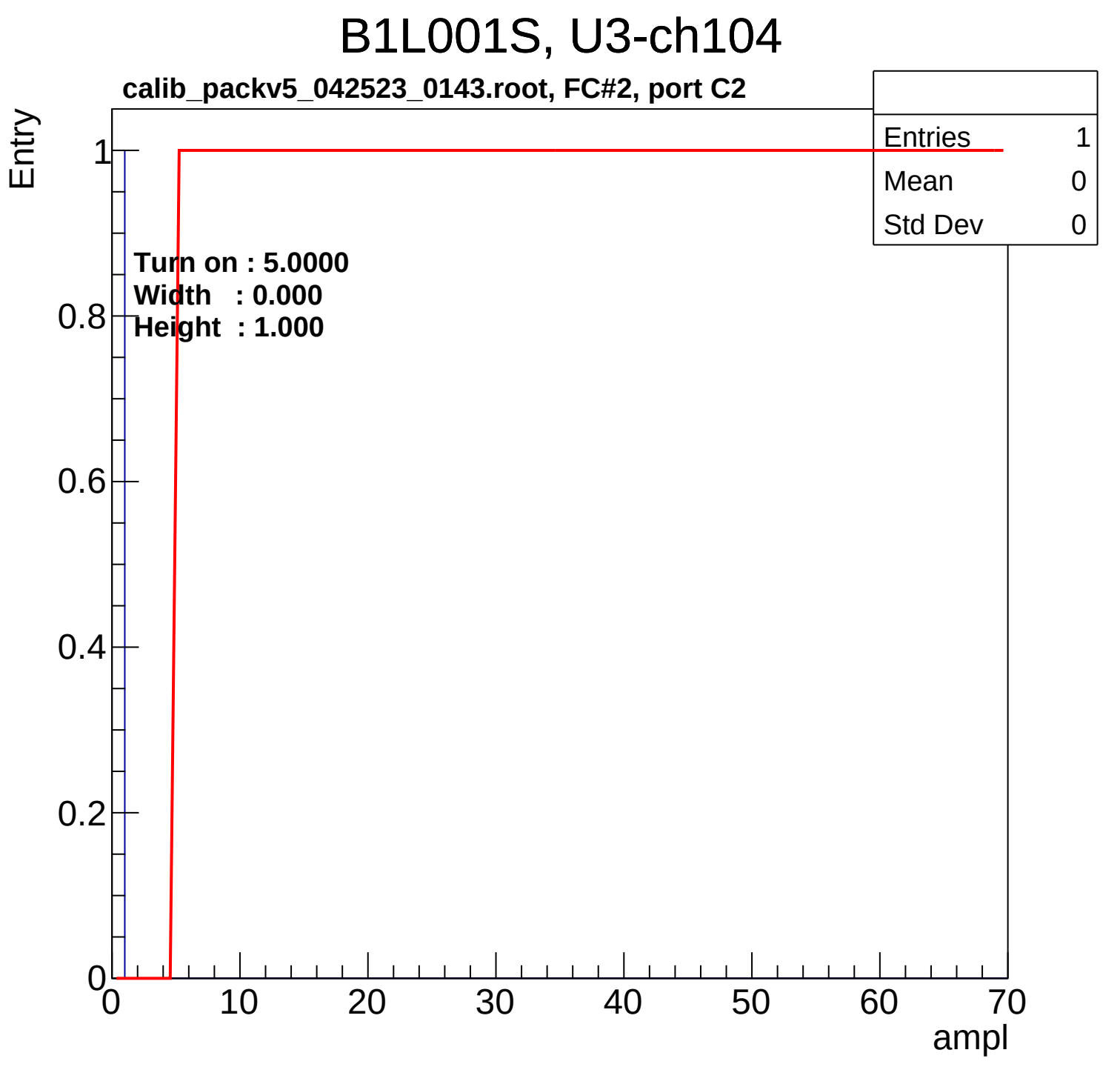

B1L001S, U3-ch99
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

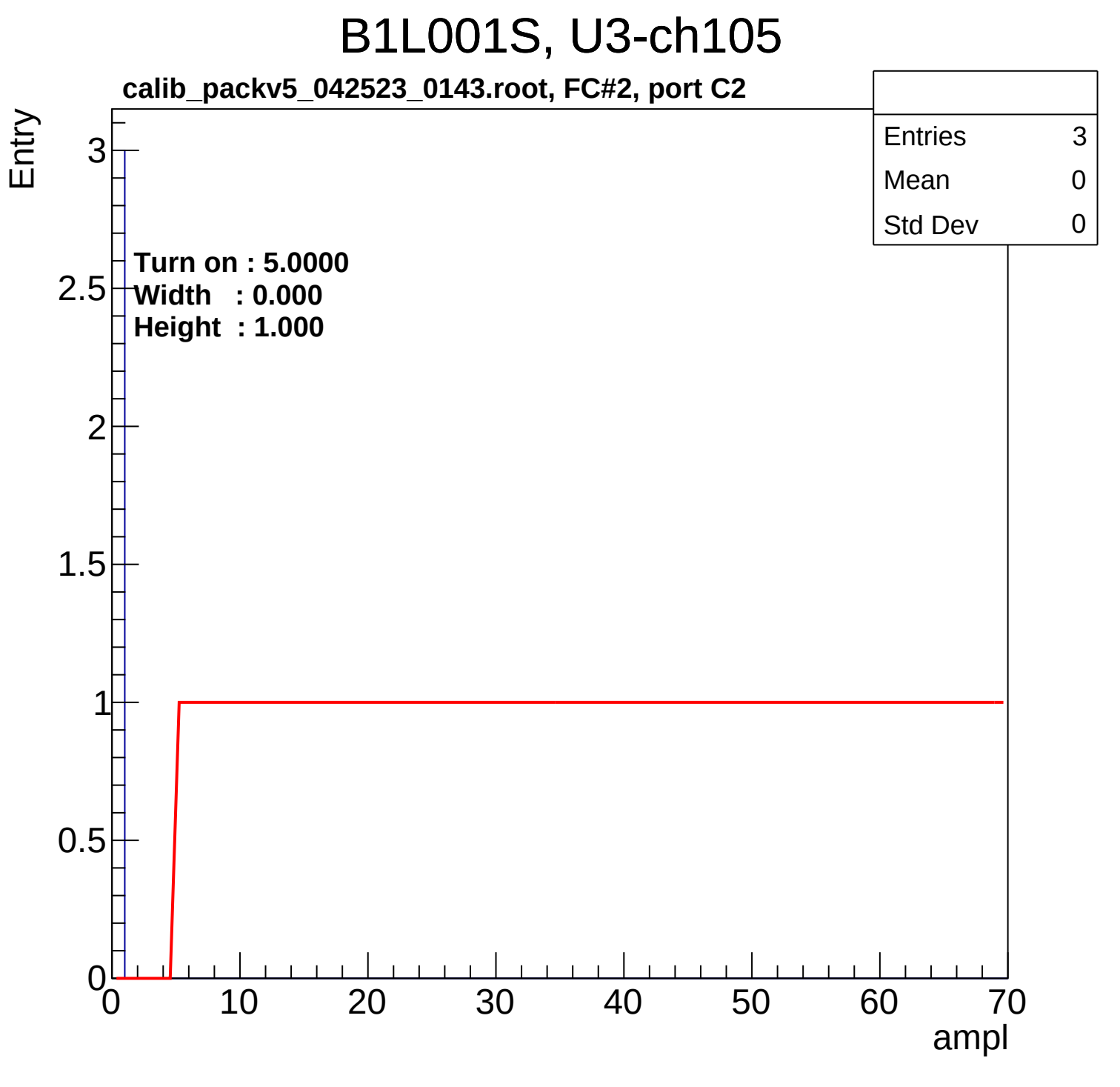

B1L001S, U3-ch100
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L001S, U3-ch101
calib_packv5_042523_0143.root, FC#2, port C2
Entries 7
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L001S, U3-ch102
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L001S, U3-ch103
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U3-ch104
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U3-ch105
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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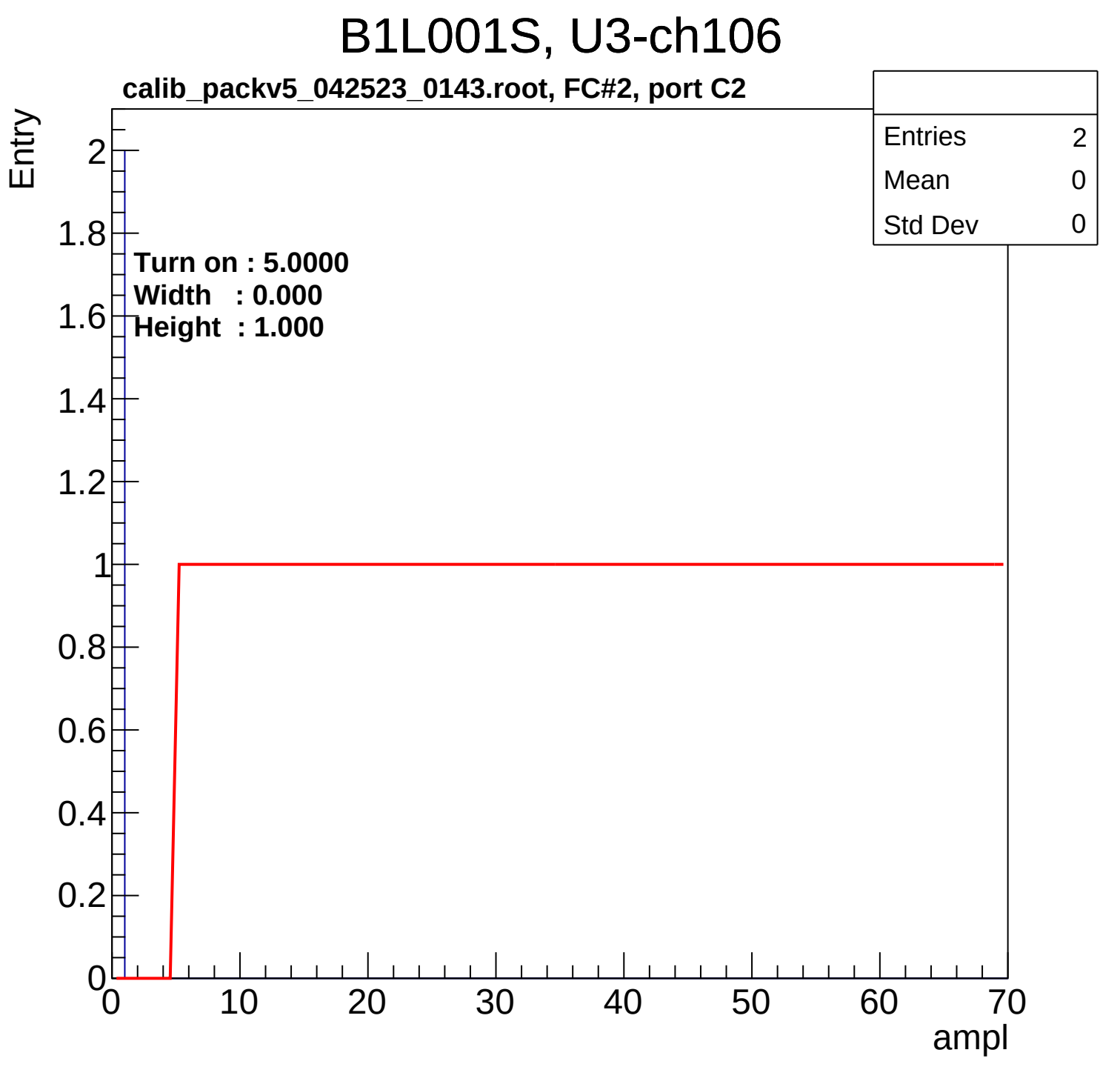
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L001S, U3-ch106
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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40
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60
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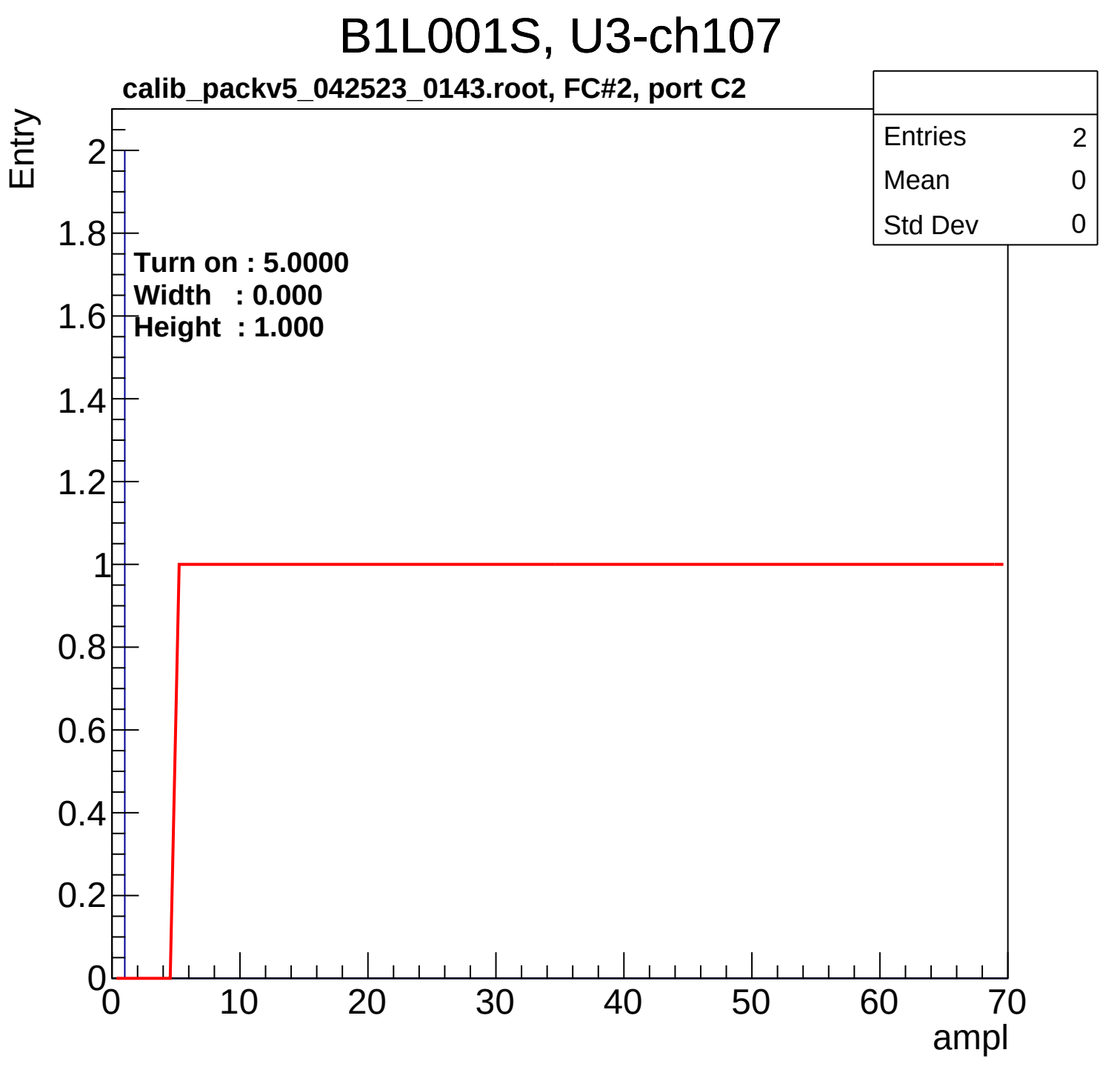
B1L001S, U3-ch107
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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40
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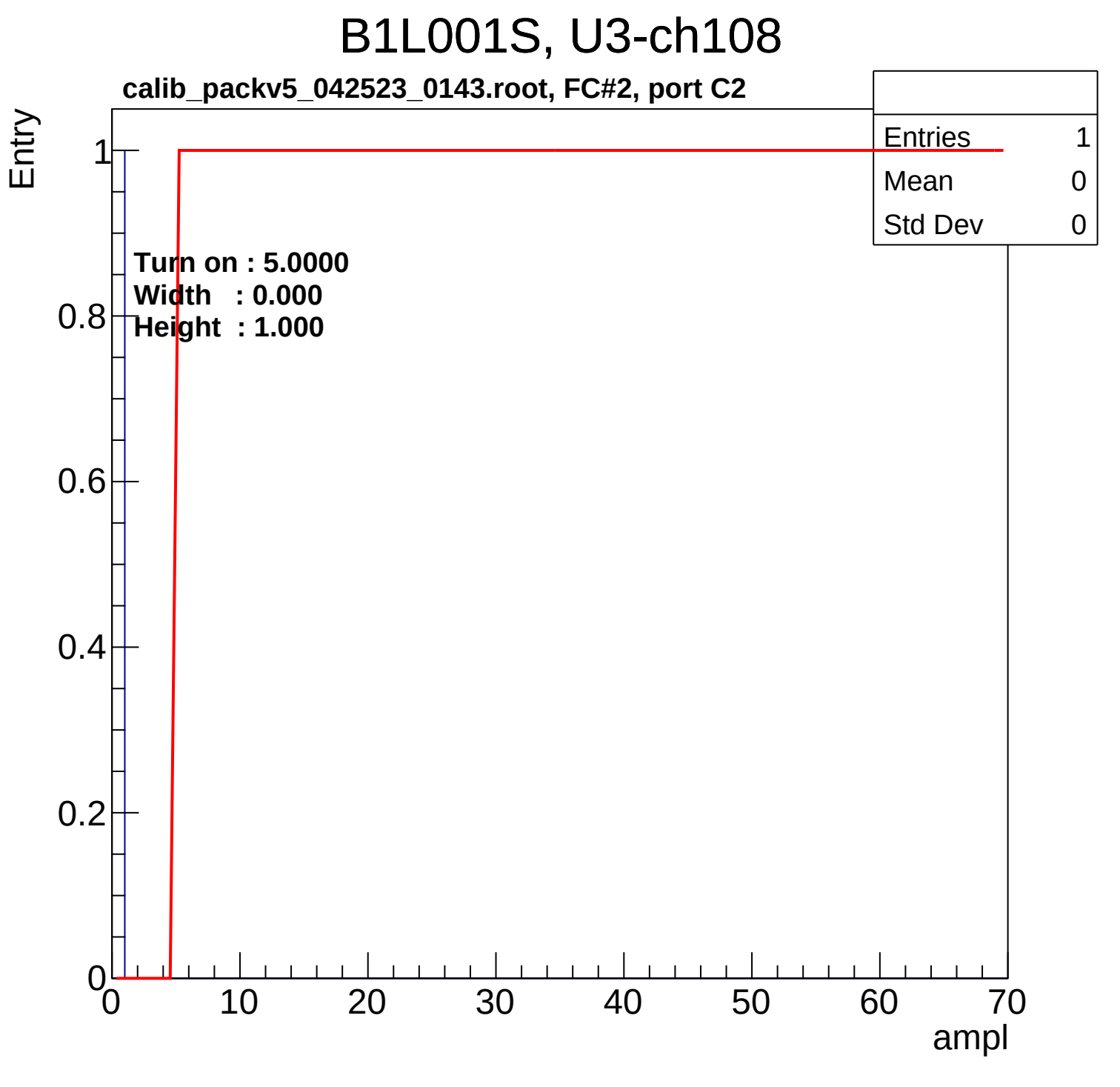
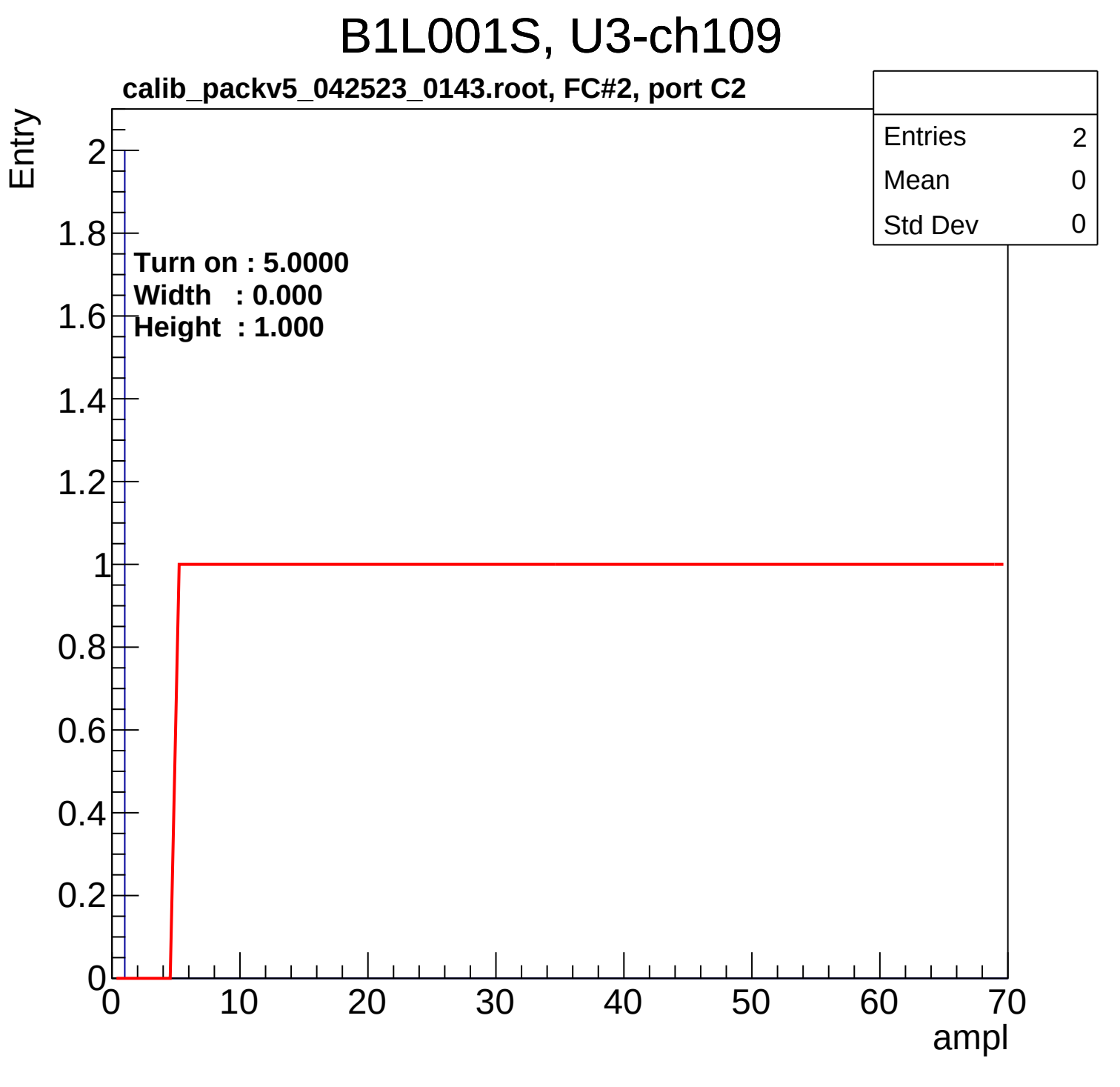
60
70


B1L001S, U3-ch108
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U3-ch109
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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20
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60
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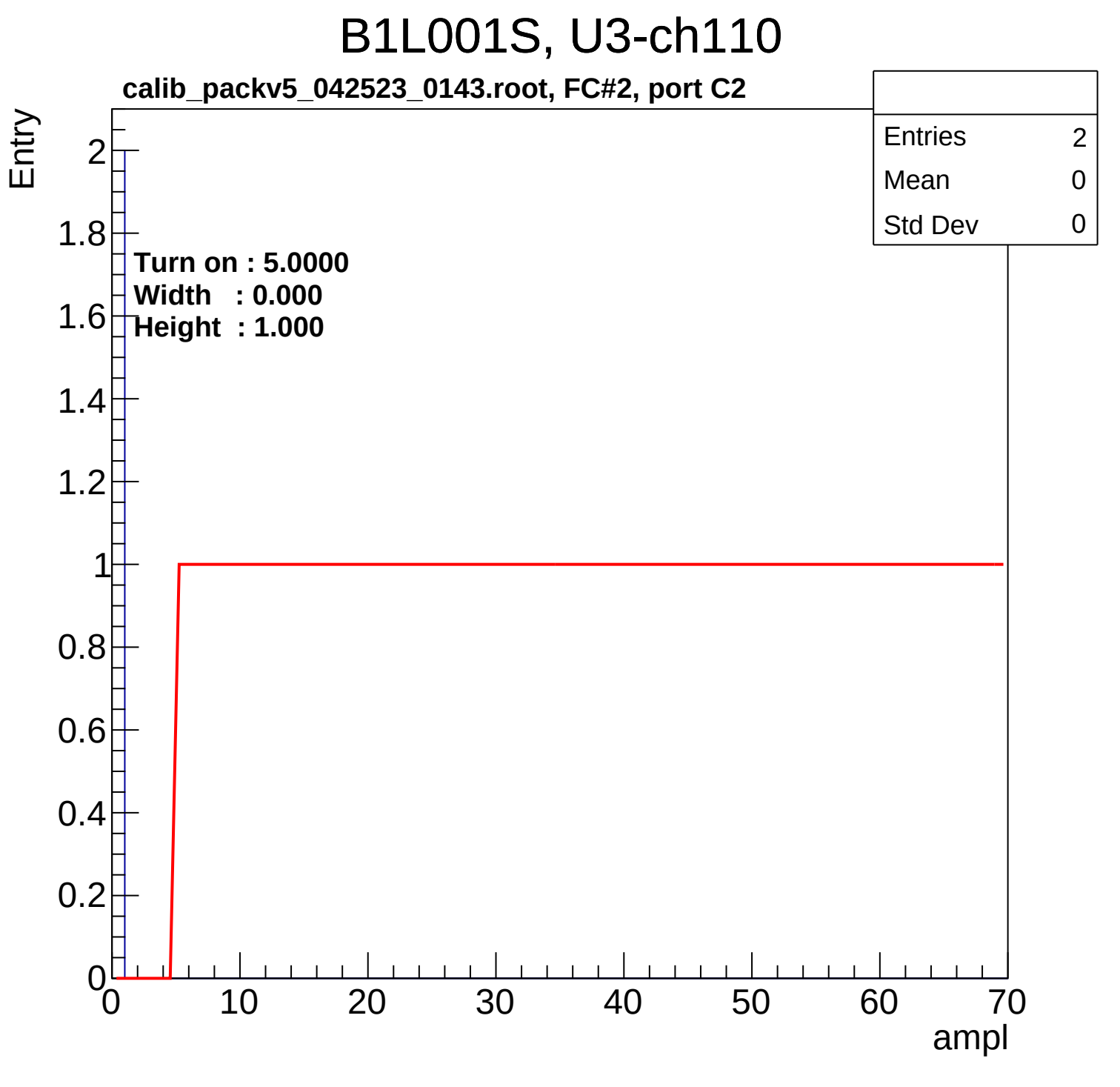
B1L001S, U3-ch110
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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40
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60
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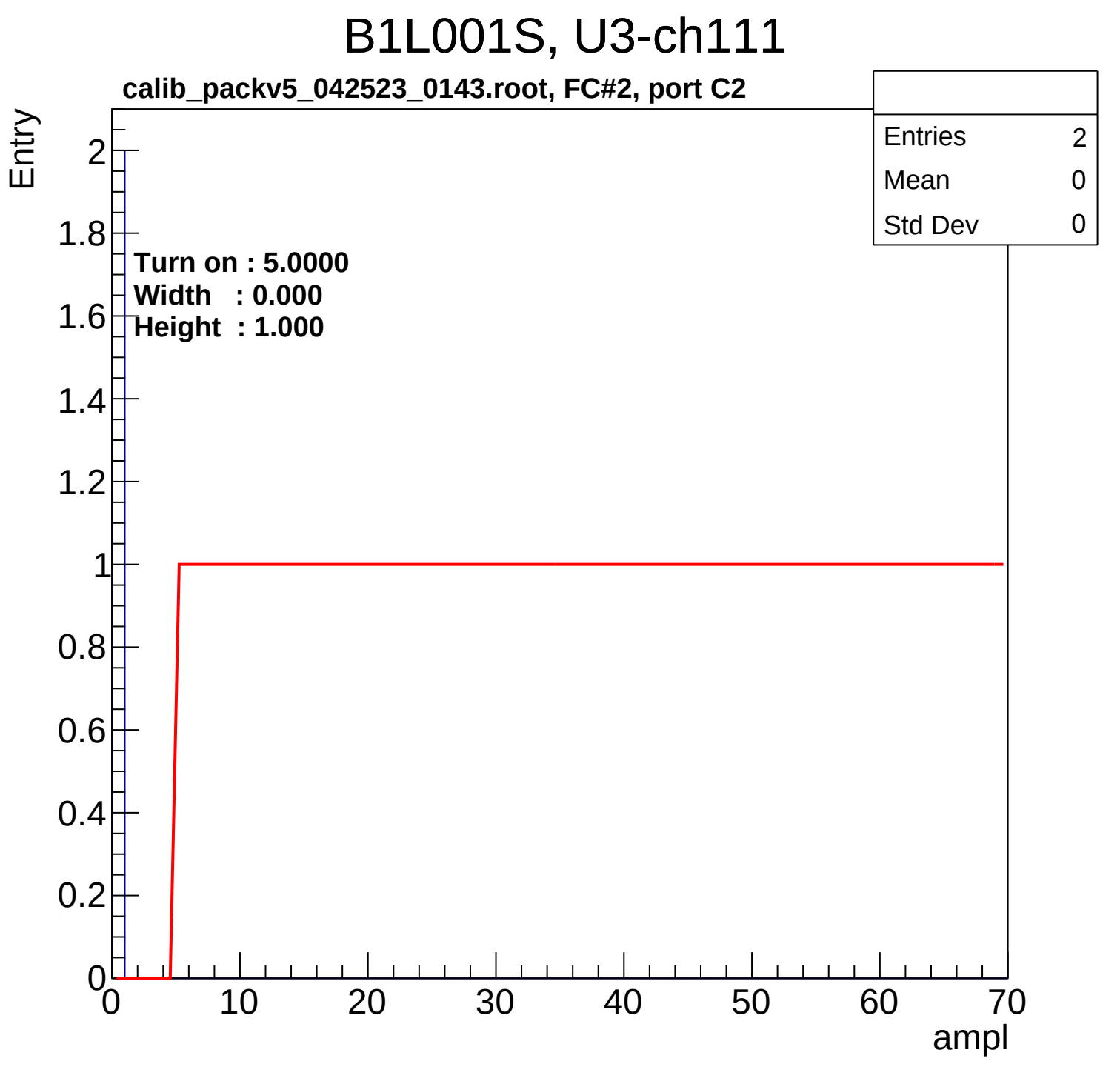
B1L001S, U3-ch111
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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40
50
60
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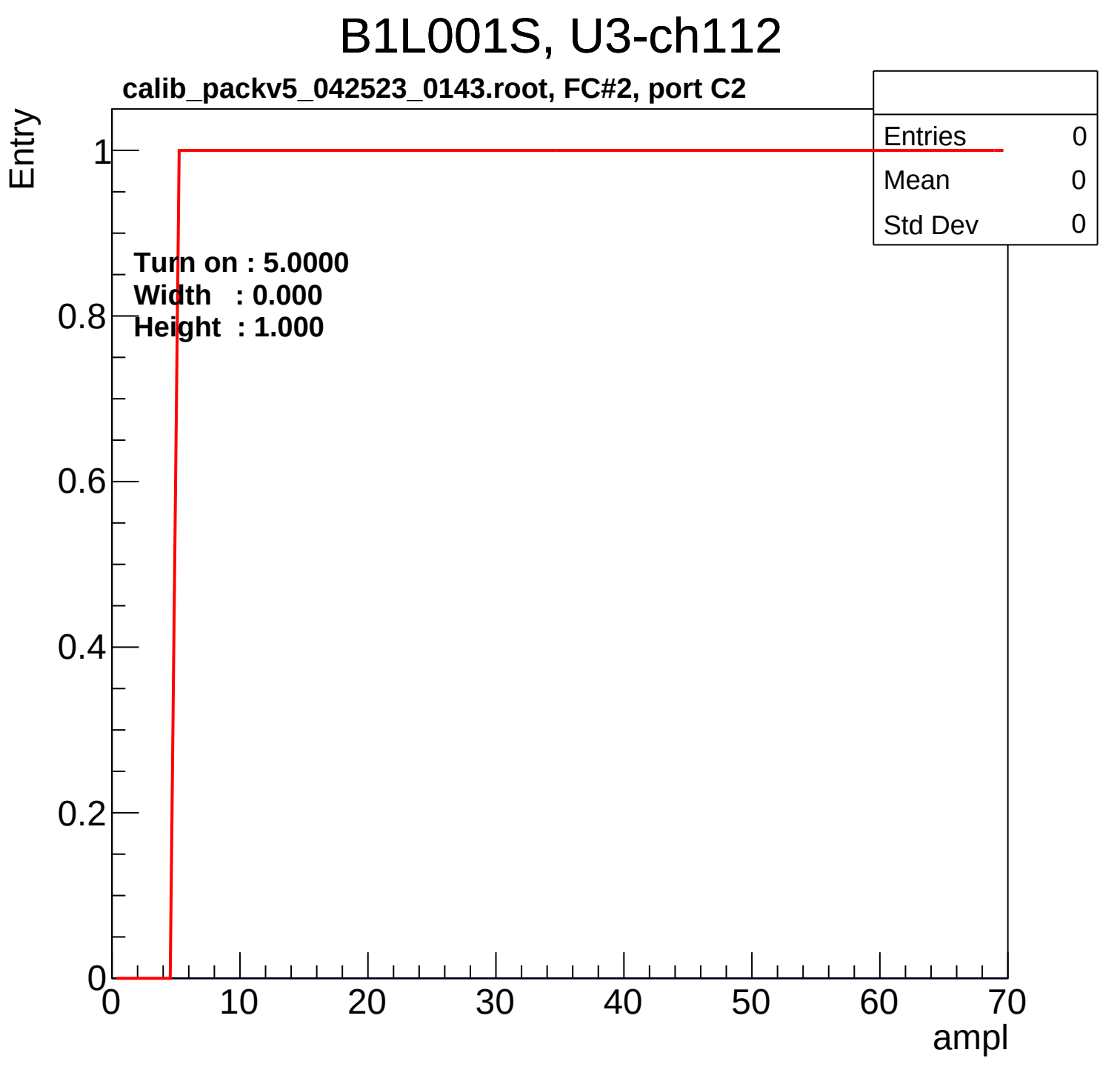
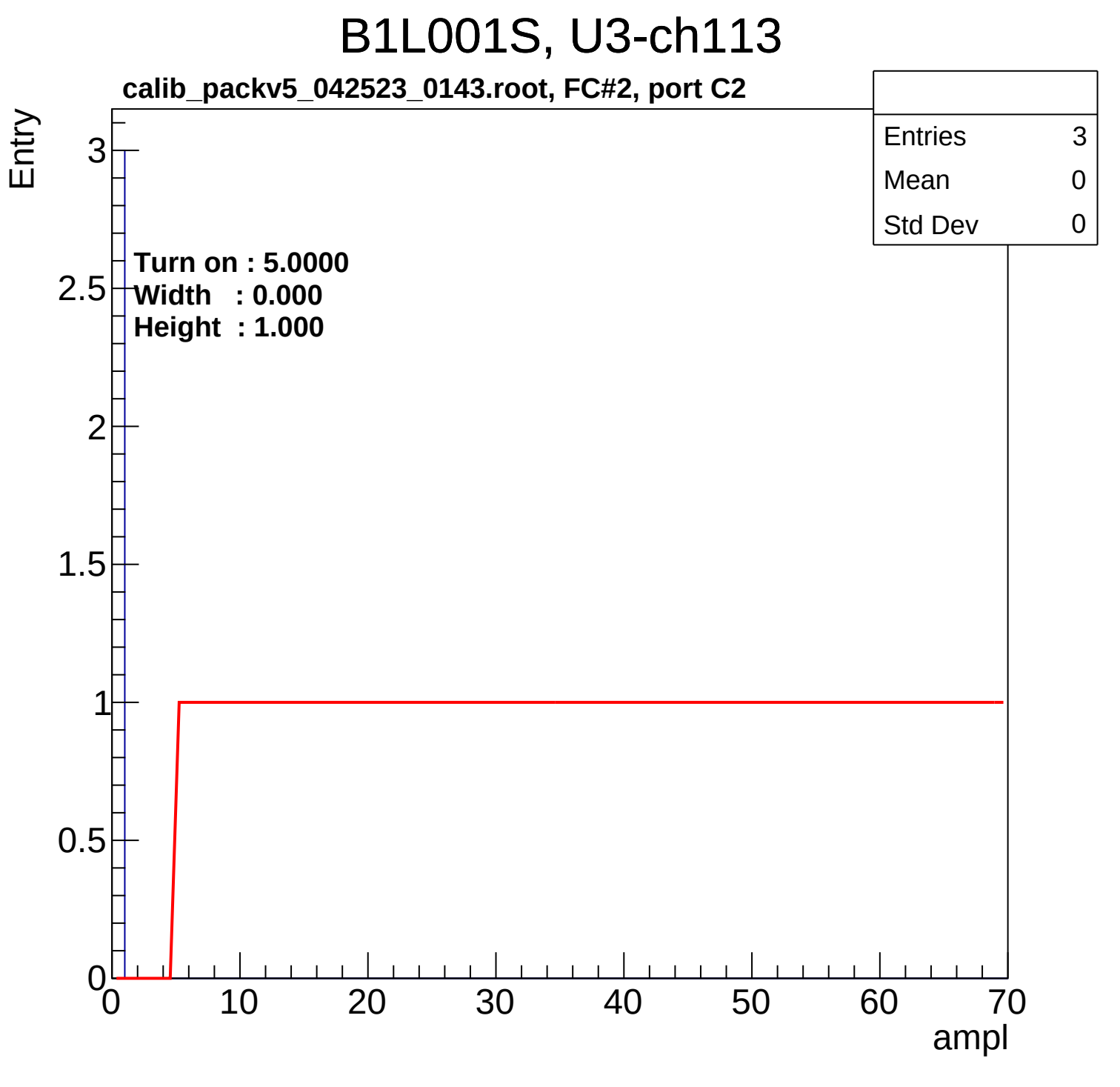

B1L001S, U3-ch112
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B1L001S, U3-ch113
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
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20
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40
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60
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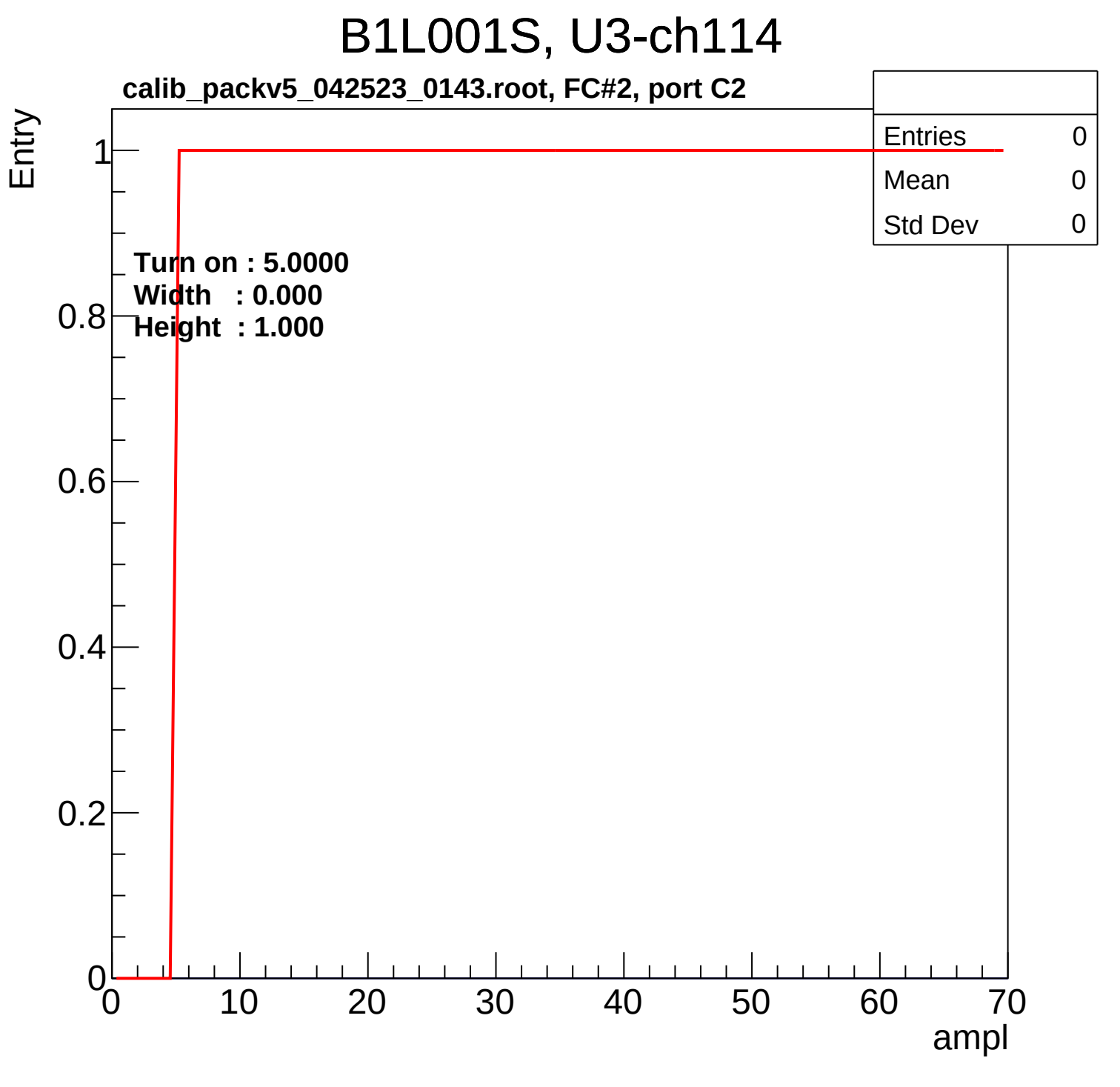
B1L001S, U3-ch114
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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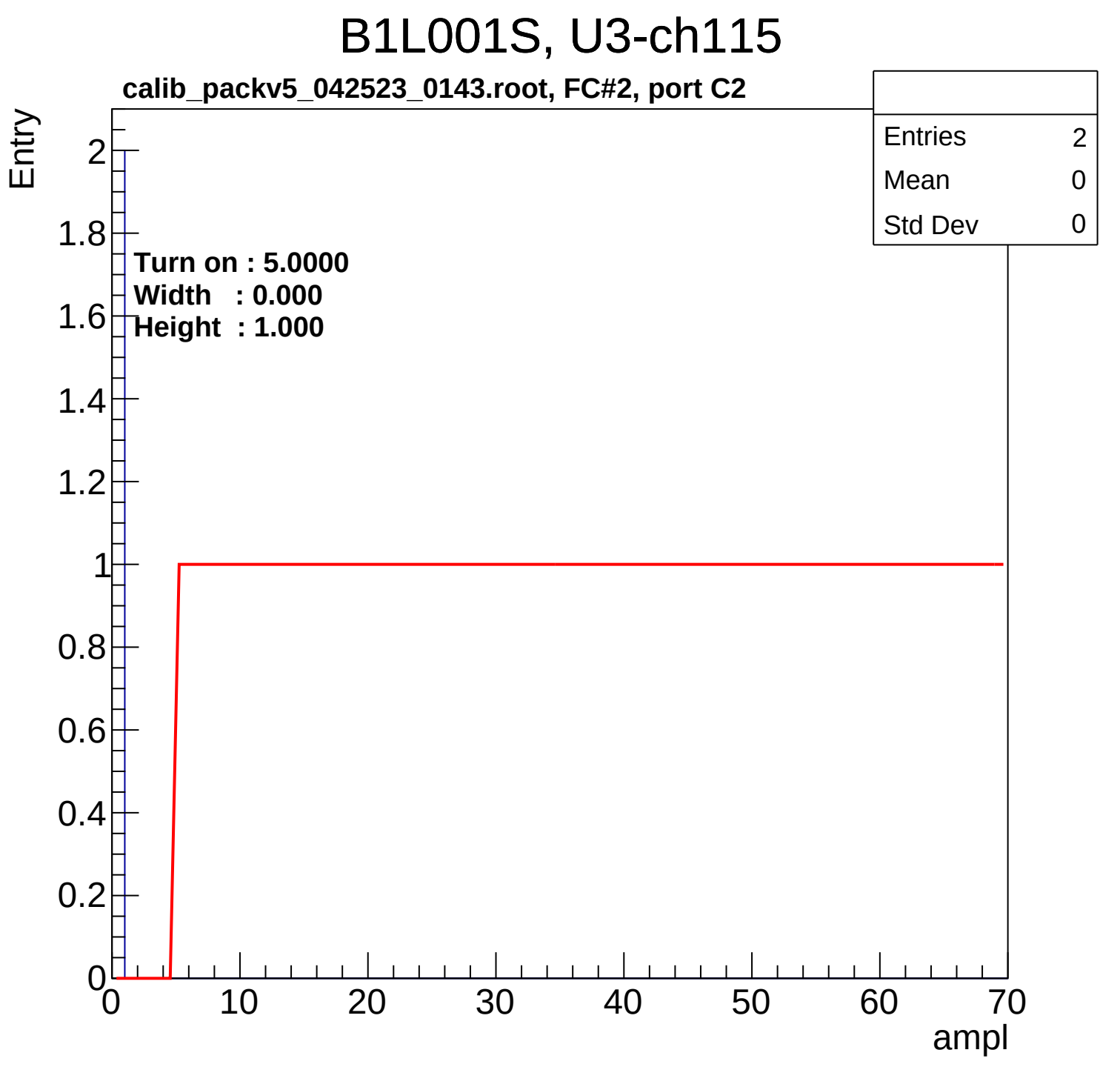
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U3-ch115
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
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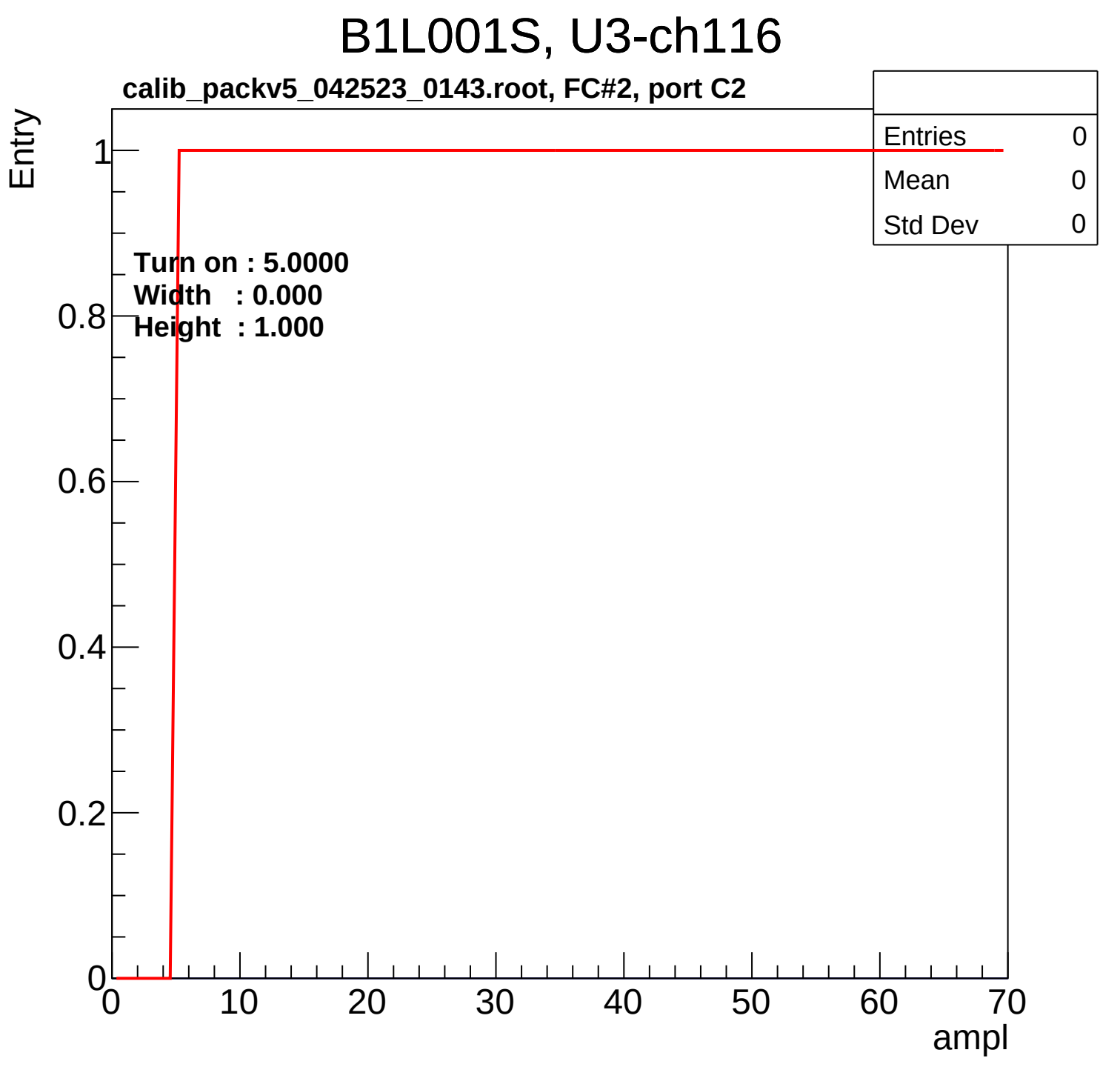
60
70


B1L001S, U3-ch116
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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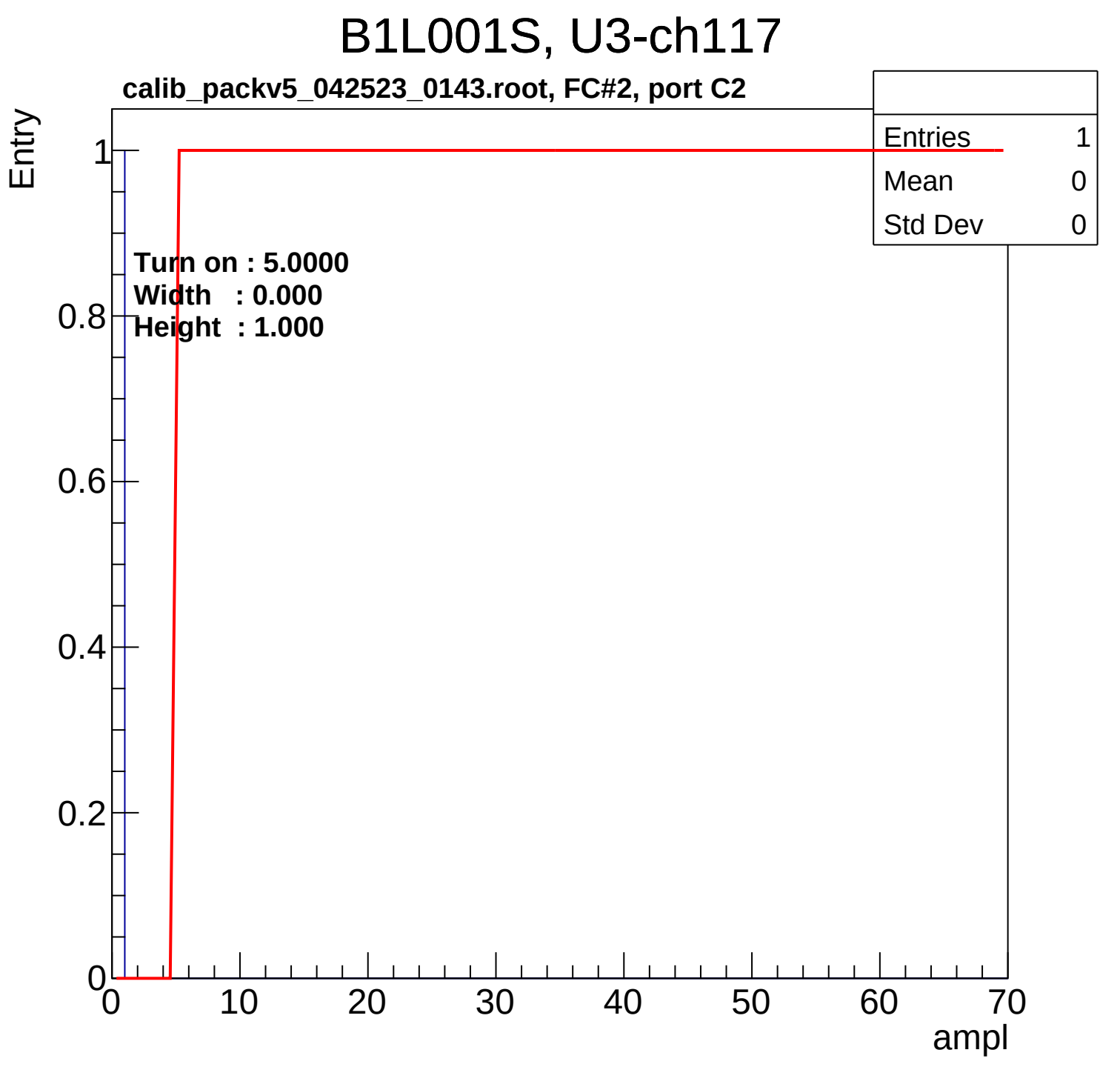
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U3-ch117
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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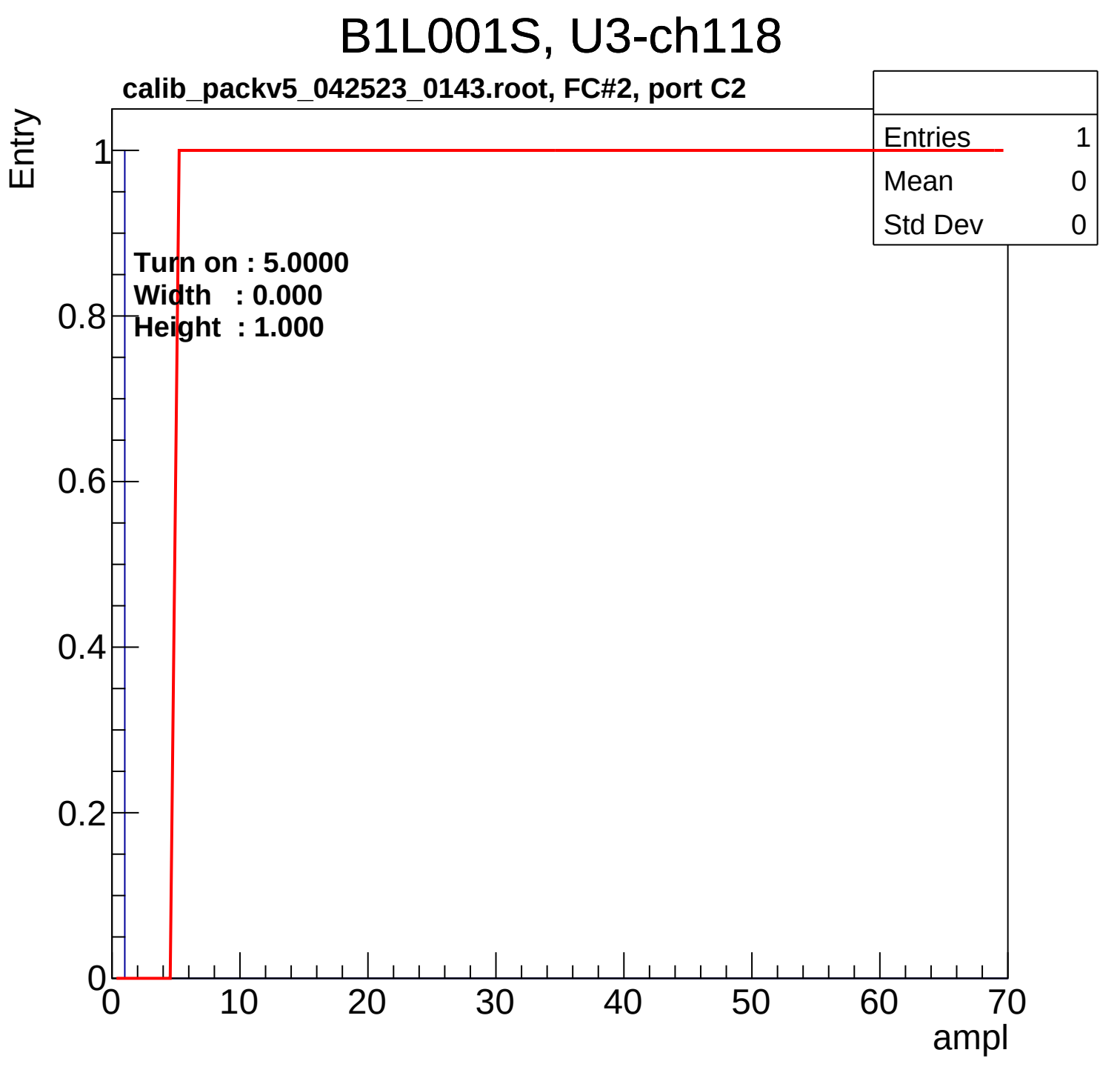
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U3-ch118
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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0.6
0.4
0.2
0
0
10
20
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40
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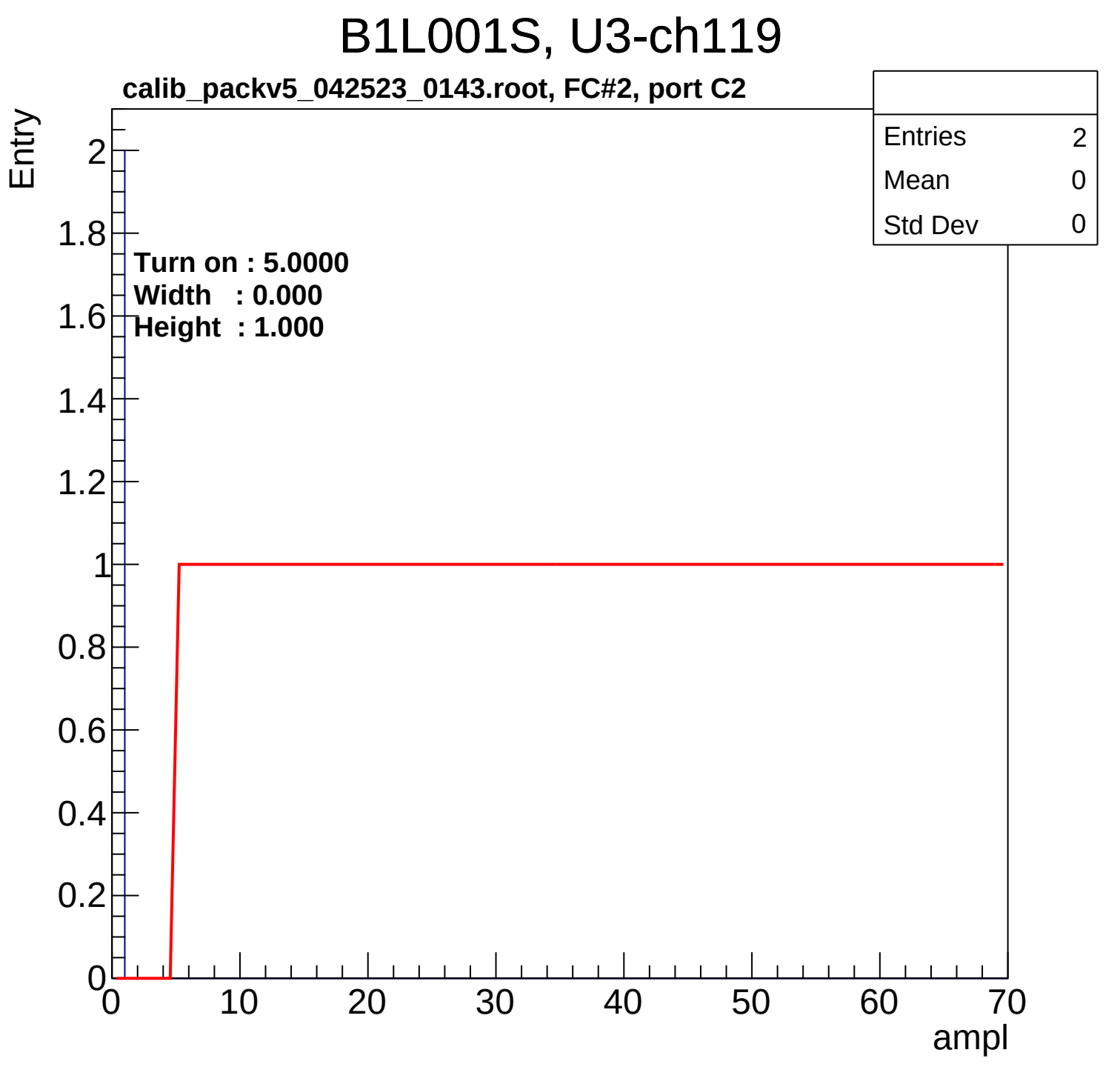
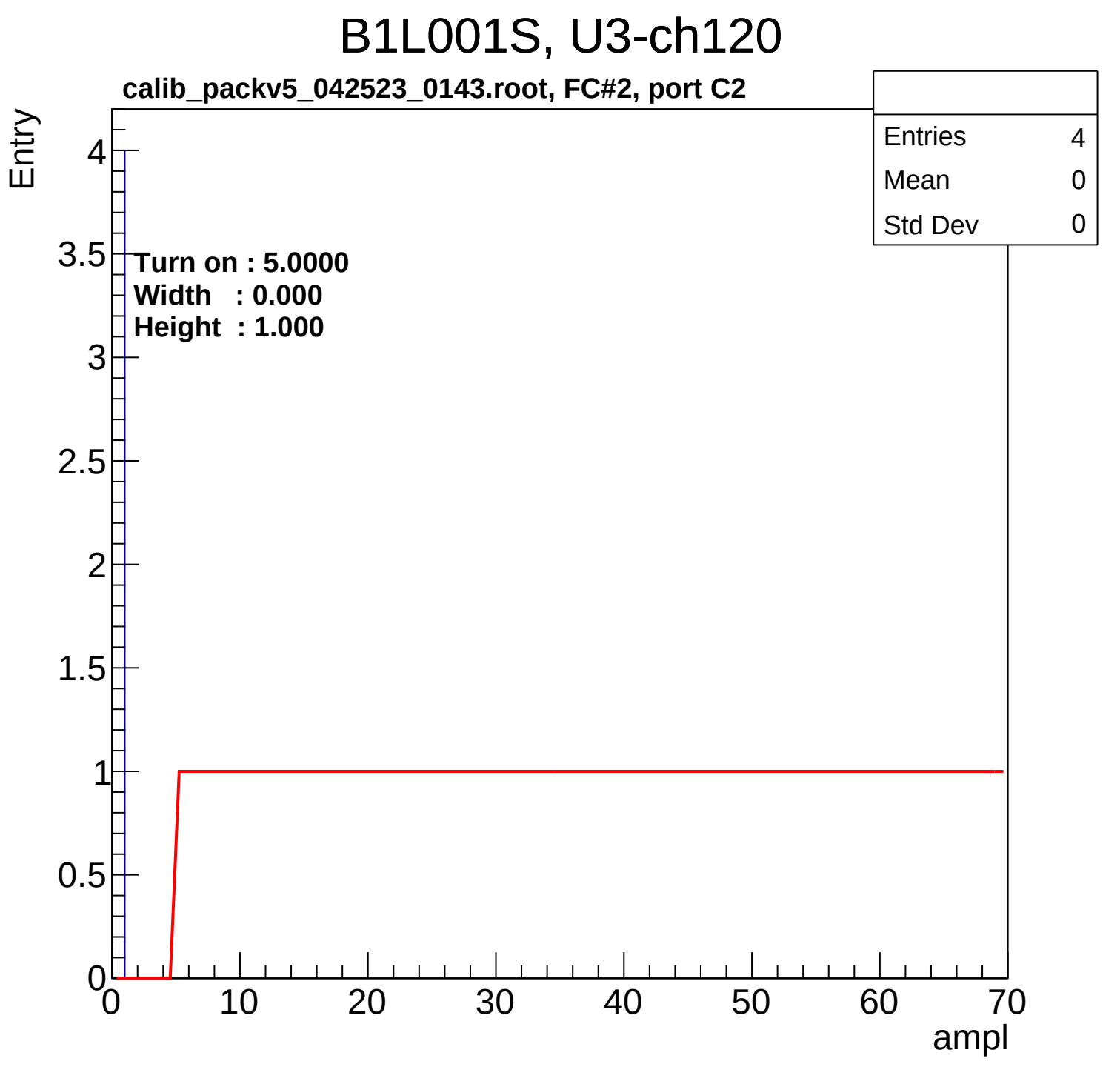
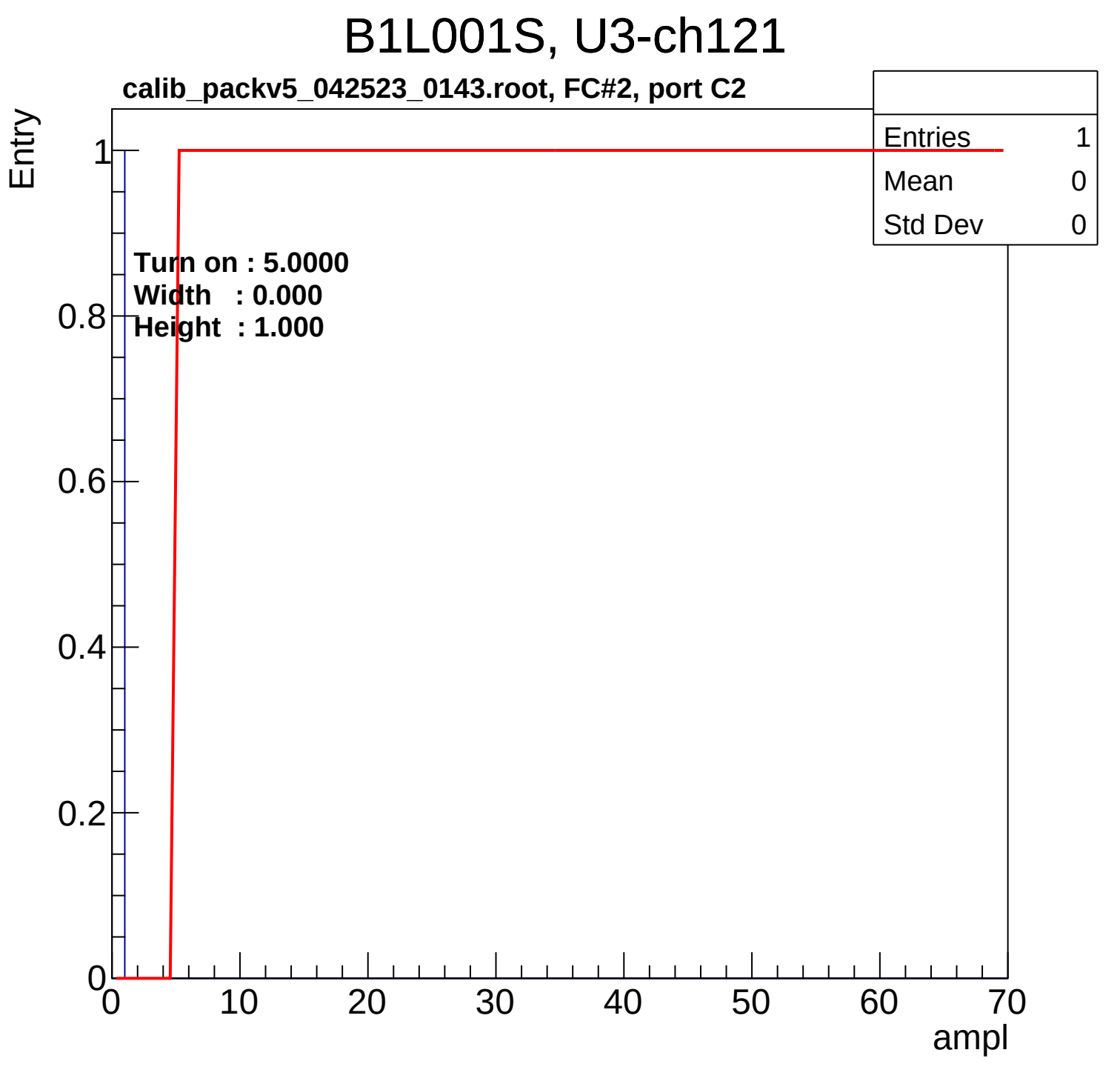
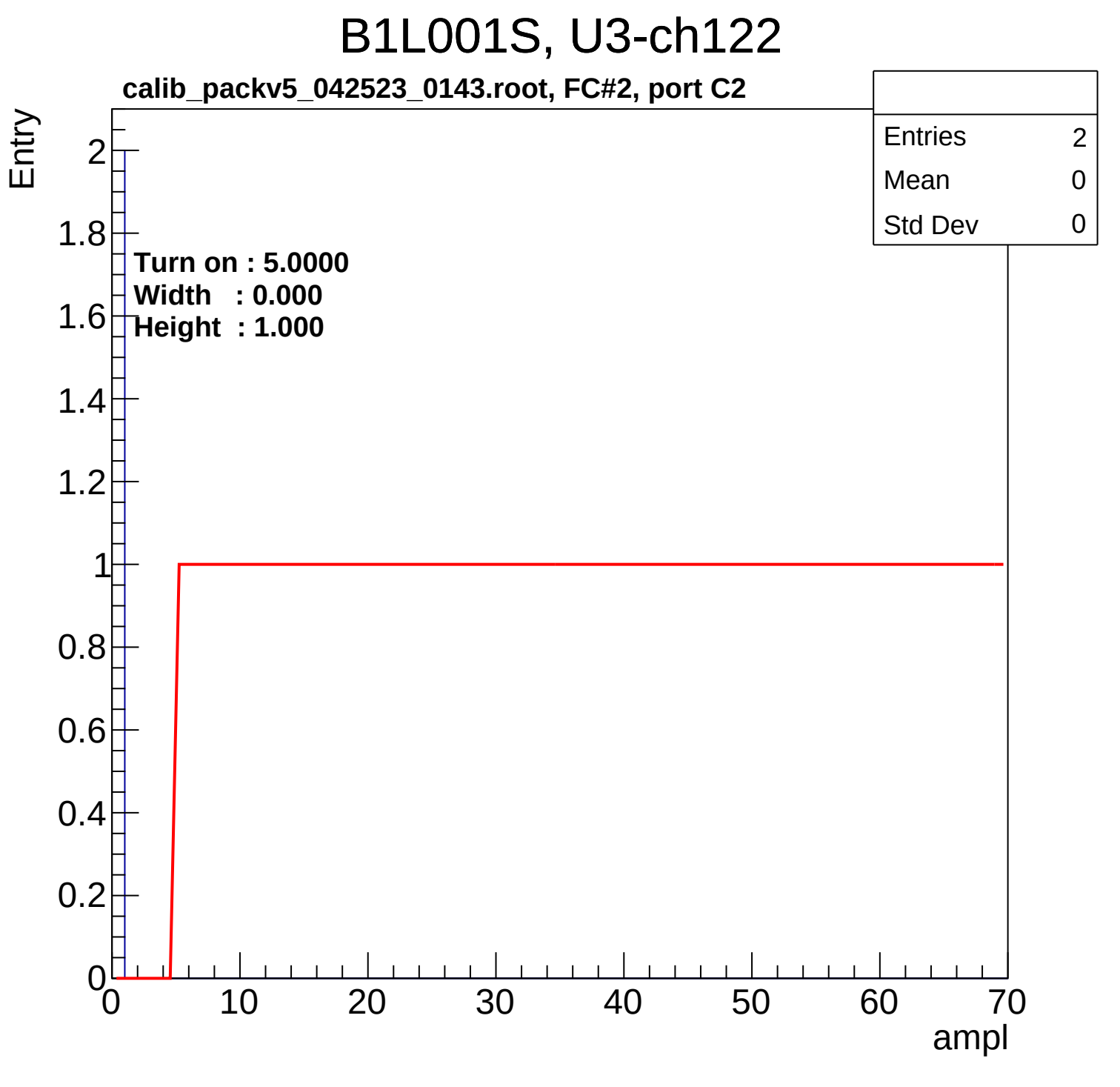
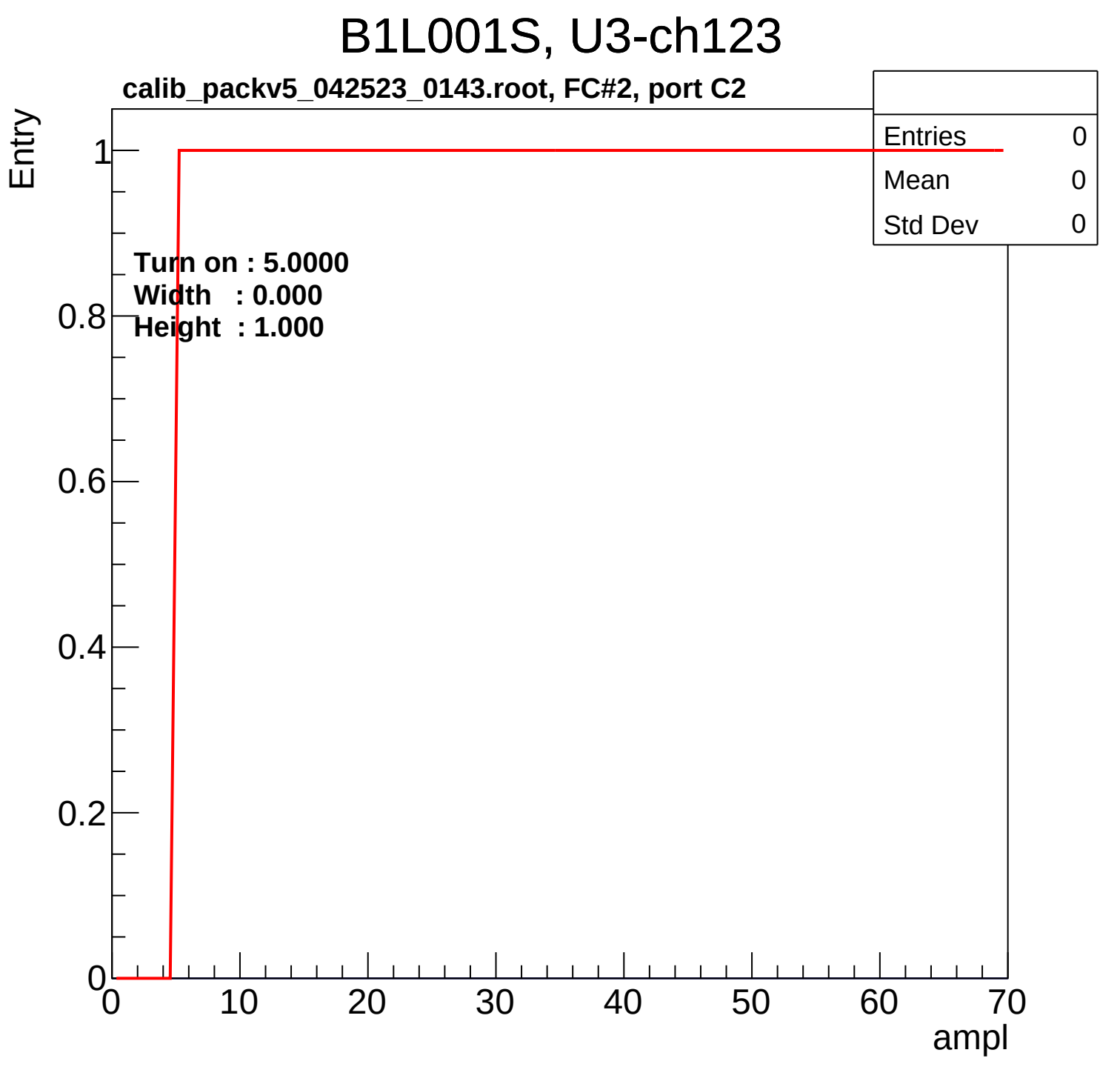
70
ampl

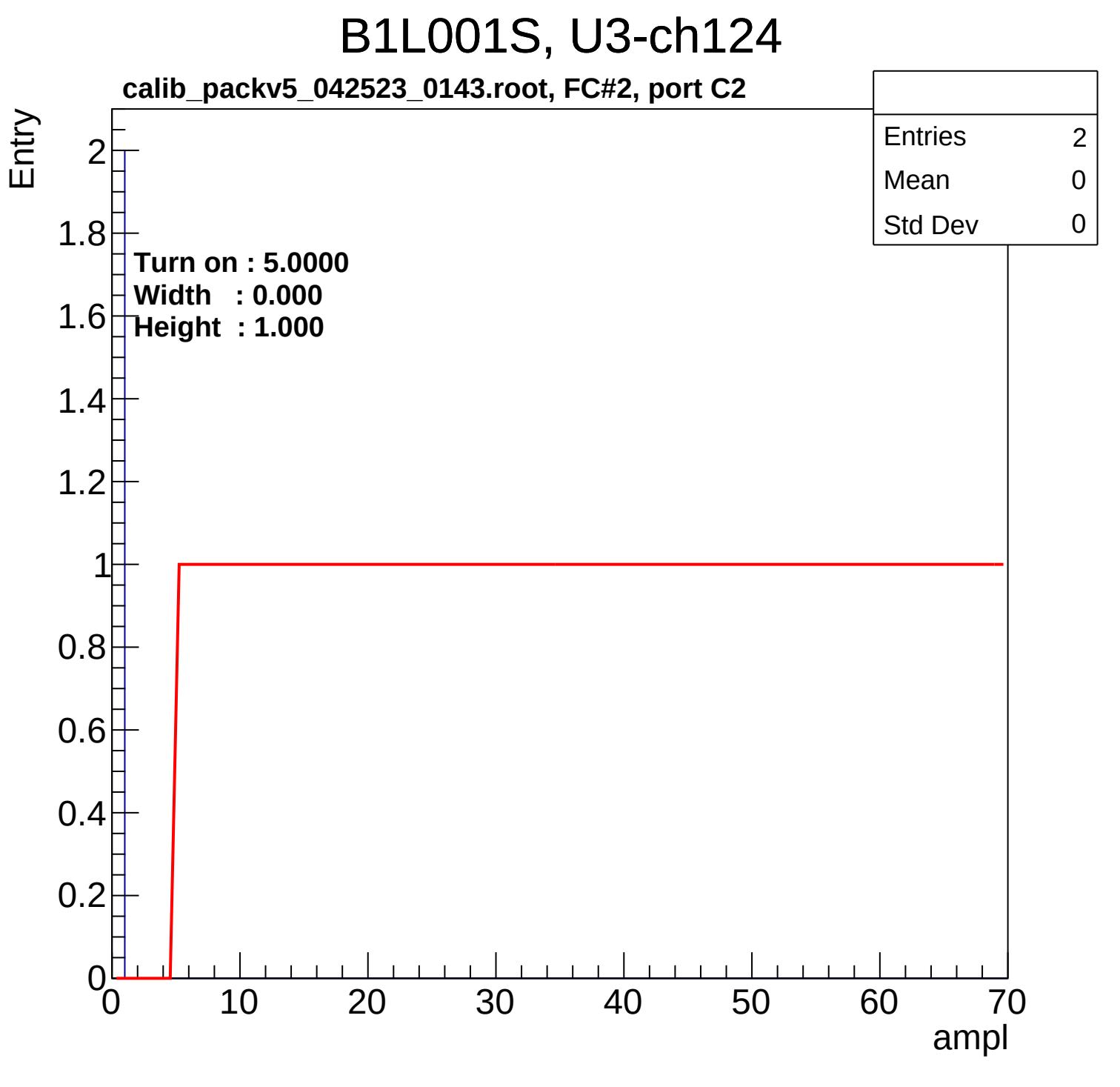

B1L001S, U3-ch119
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

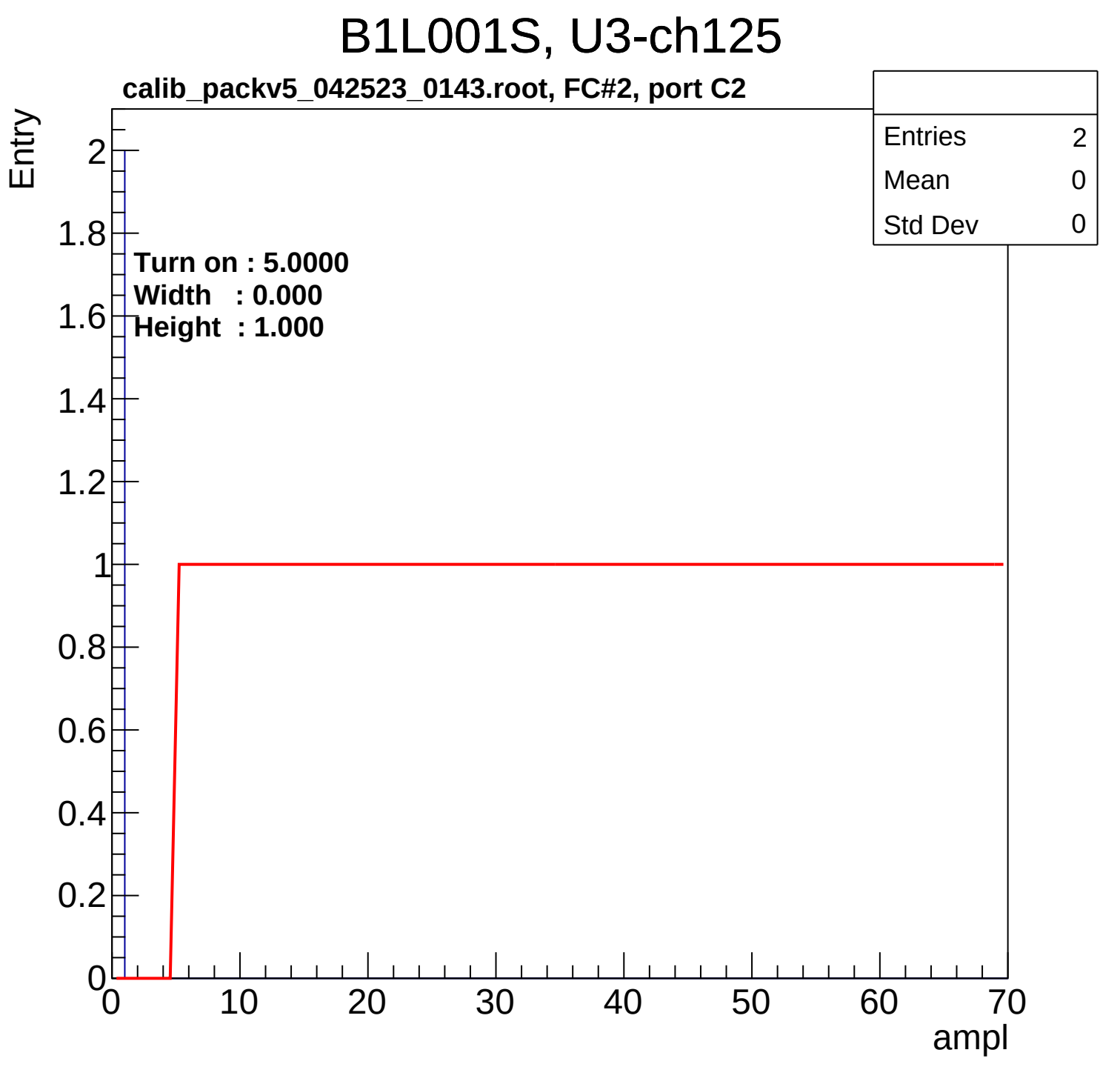

B1L001S, U3-ch120
calib_packv5_042523_0143.root, FC#2, port C2
Entries 4
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

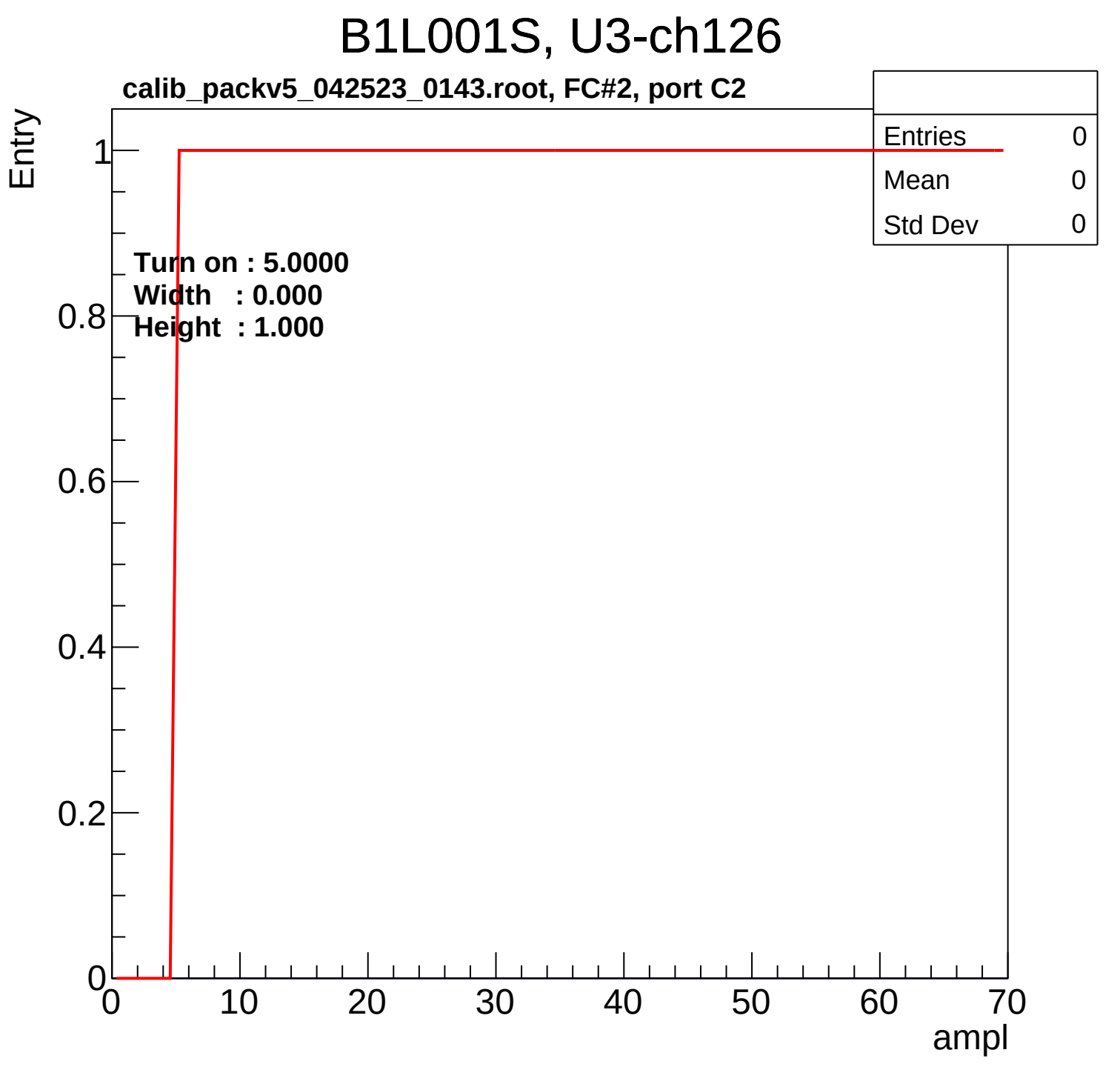

B1L001S, U3-ch121
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

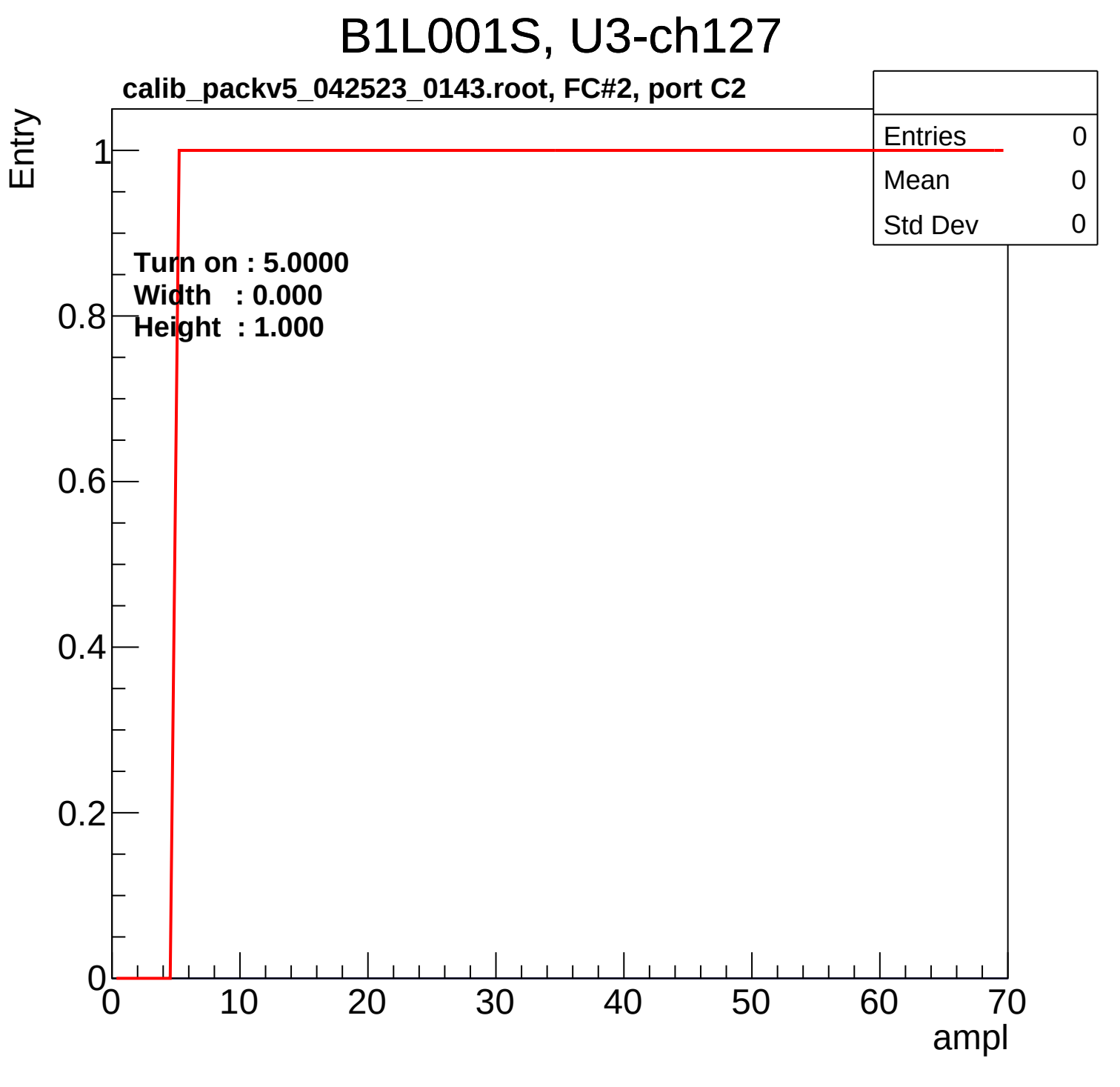

B1L001S, U3-ch122
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

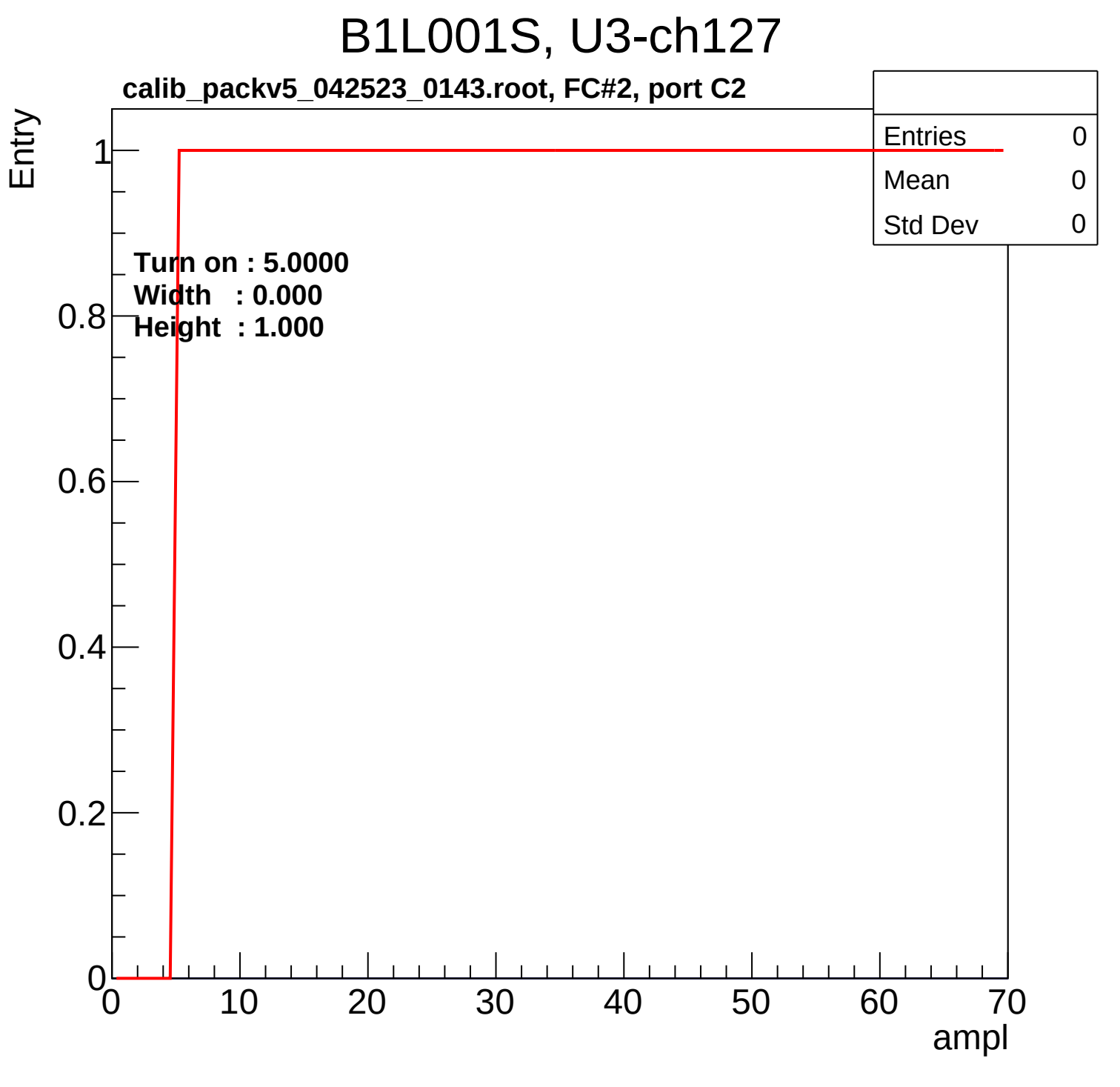

B1L001S, U3-ch123
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U3-ch124
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L001S, U3-ch125
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L001S, U3-ch126
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U3-ch127
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U3-ch127
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70