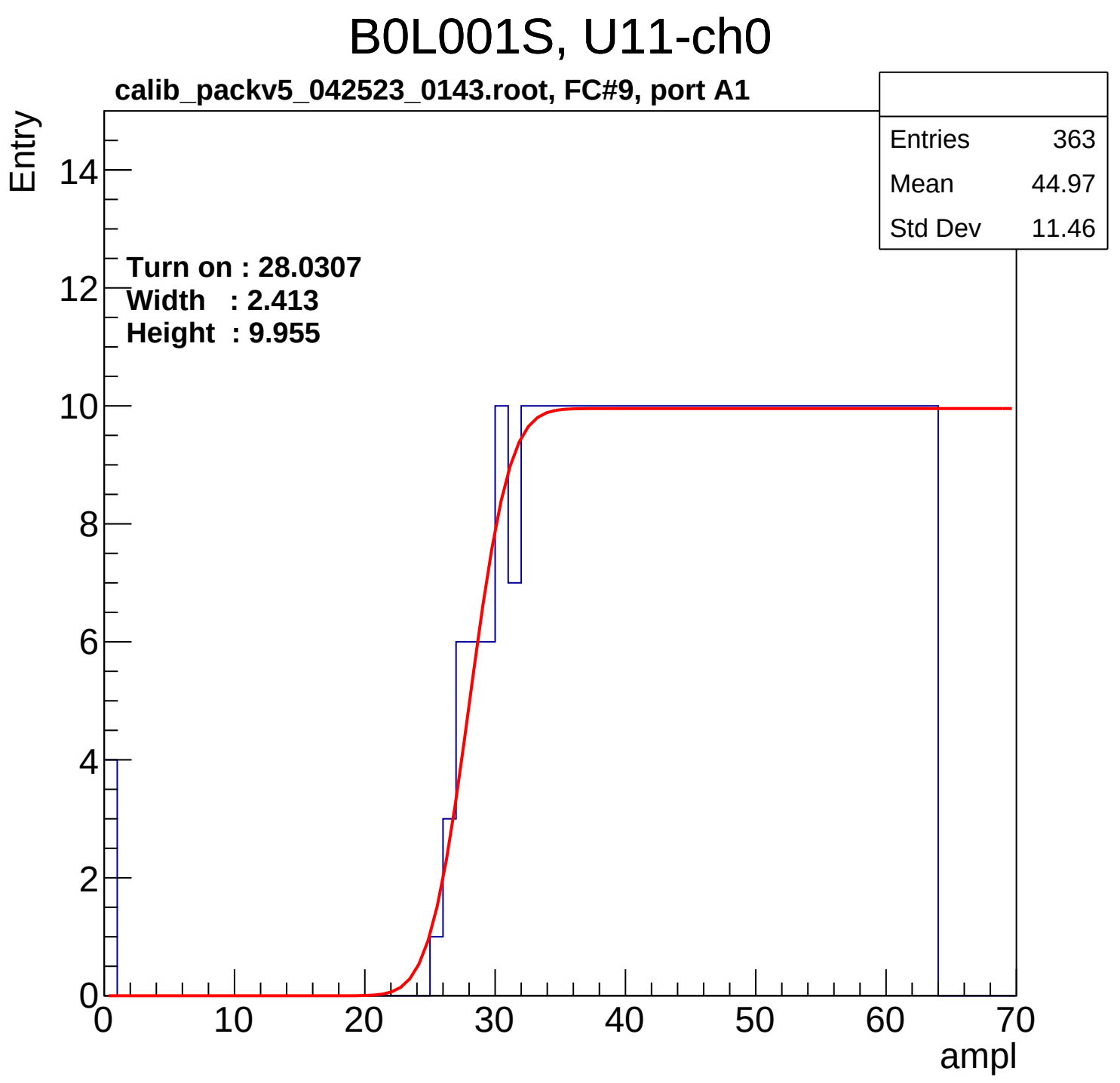
B0L001S, U11-ch0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 44.97
Std Dev 11.46
Turn on : 28.0307
Width : 2.413
Height : 9.955
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ampl
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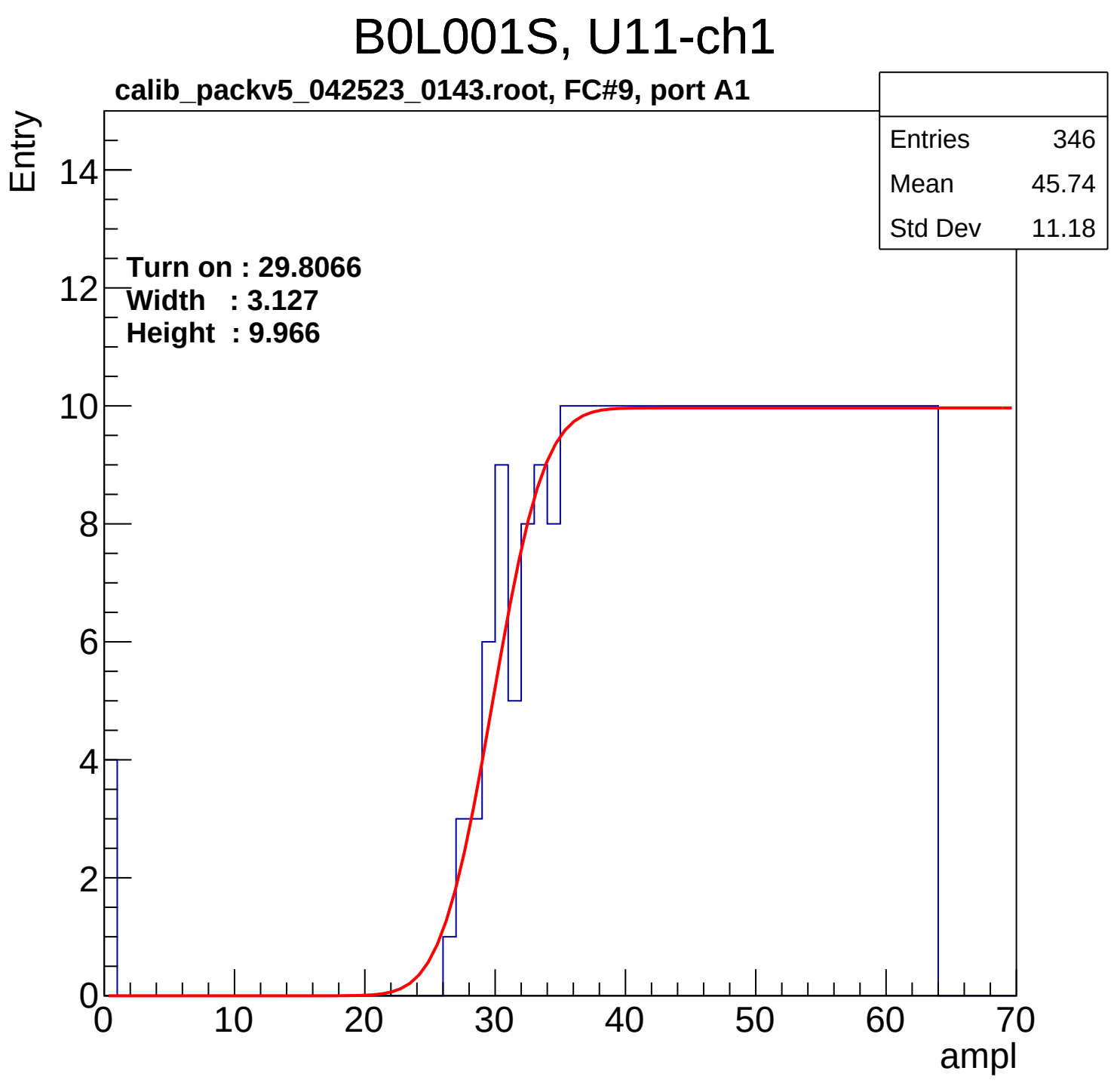
B0L001S, U11-ch1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 346
Mean 45.74
Std Dev 11.18
Turn on : 29.8066
Width : 3.127
Height : 9.966
Entry
ampl
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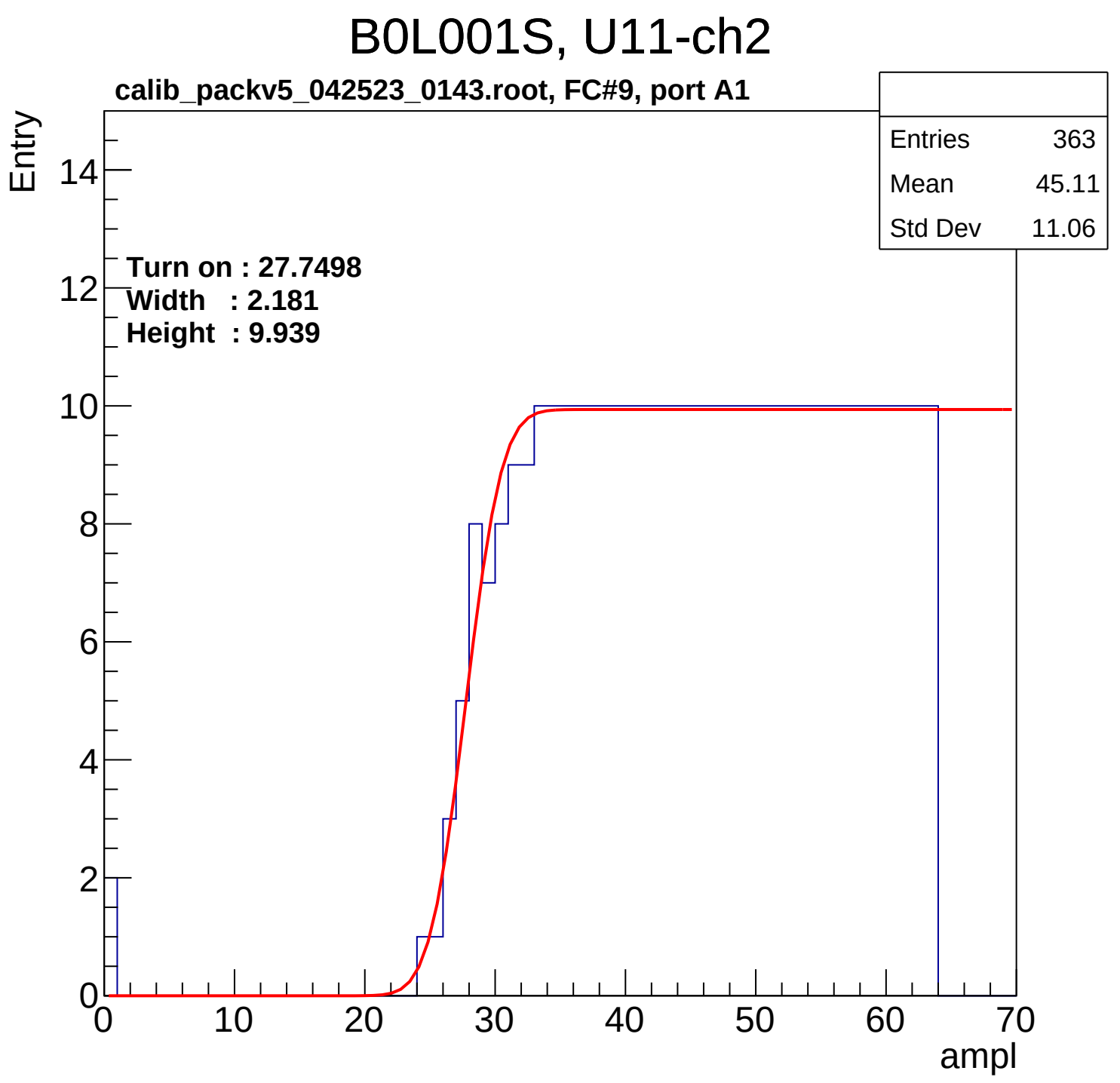
B0L001S, U11-ch2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 45.11
Std Dev 11.06
Turn on : 27.7498
Width : 2.181
Height : 9.939
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ampl
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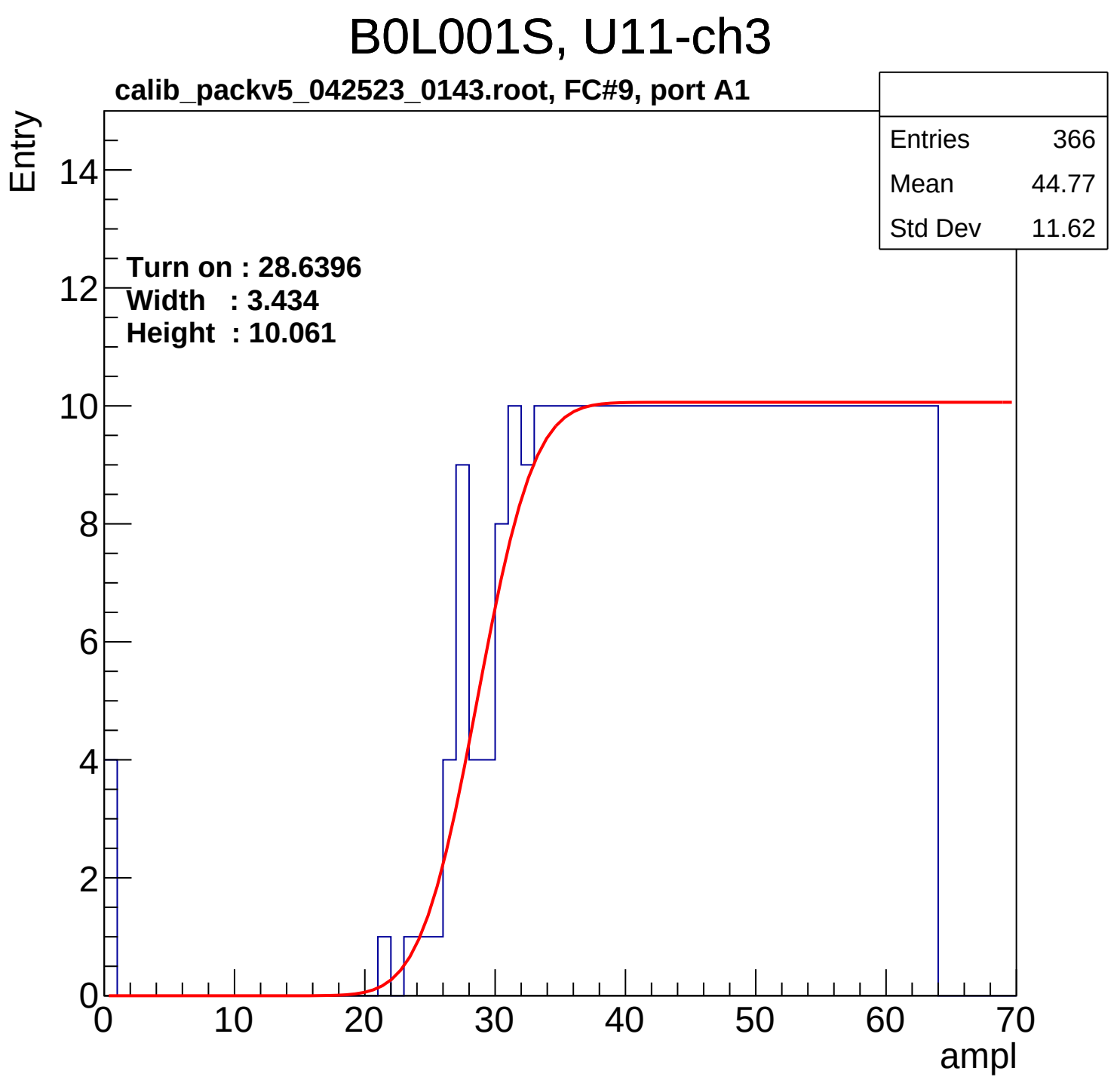
B0L001S, U11-ch3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.77
Std Dev 11.62
Turn on : 28.6396
Width : 3.434
Height : 10.061
Entry
ampl
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2
4
6
8
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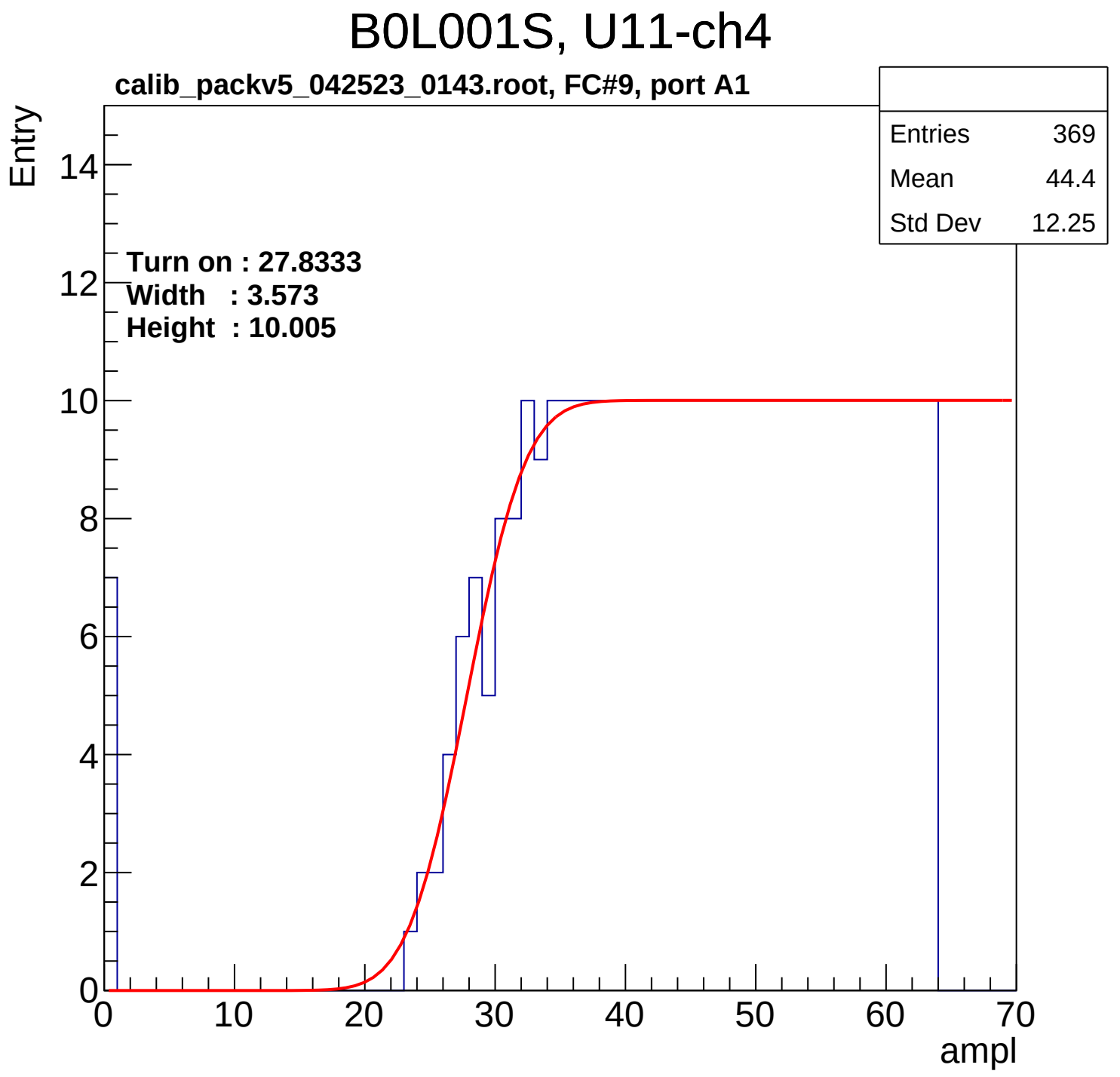
B0L001S, U11-ch4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.4
Std Dev 12.25
Turn on : 27.8333
Width : 3.573
Height : 10.005
Entry
ampl
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6
8
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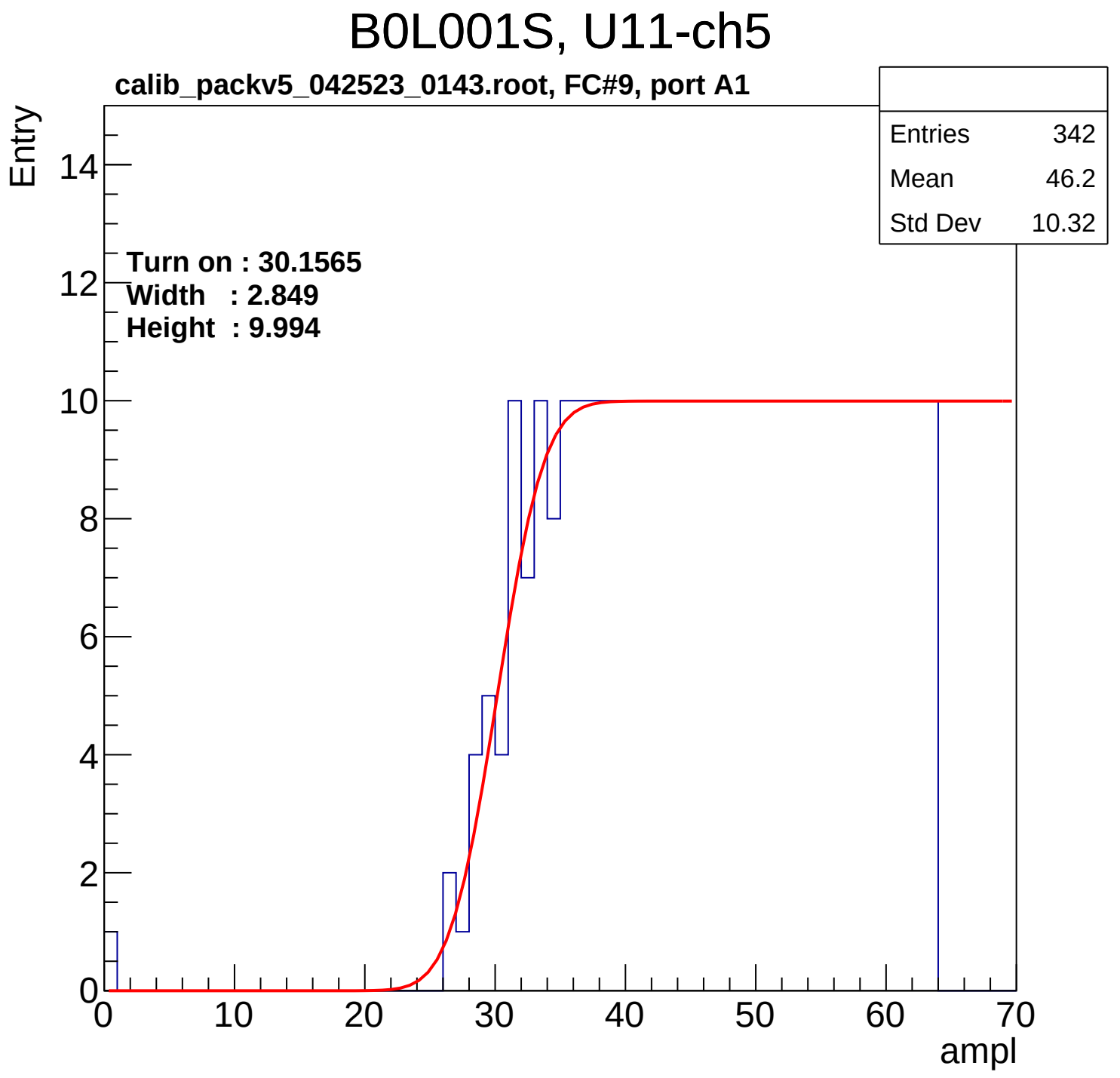
B0L001S, U11-ch5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 342
Mean 46.2
Std Dev 10.32
Turn on : 30.1565
Width : 2.849
Height : 9.994
Entry
ampl
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2
4
6
8
10
12
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0
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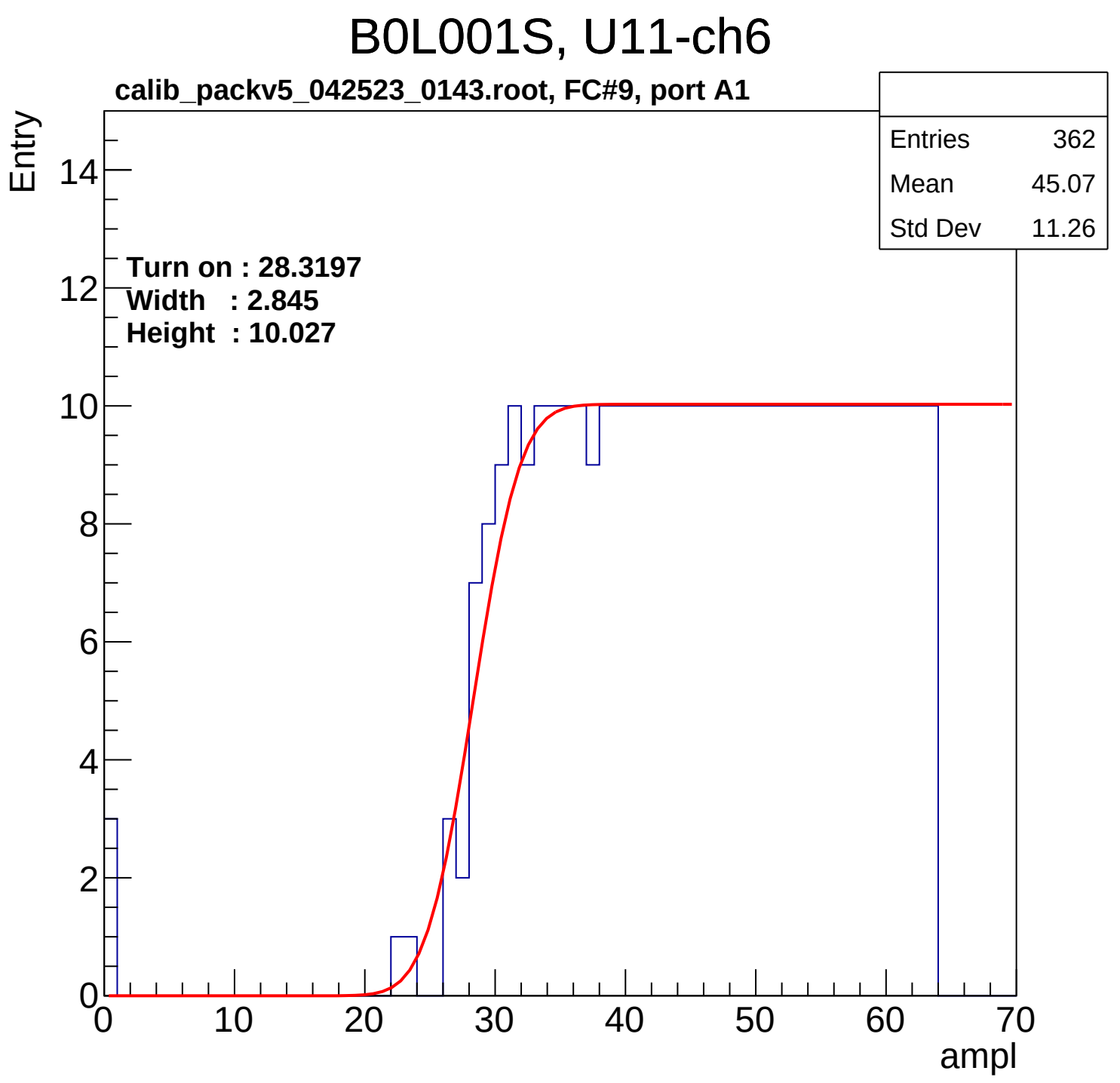
B0L001S, U11-ch6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 45.07
Std Dev 11.26
Turn on : 28.3197
Width : 2.845
Height : 10.027
Entry
ampl
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6
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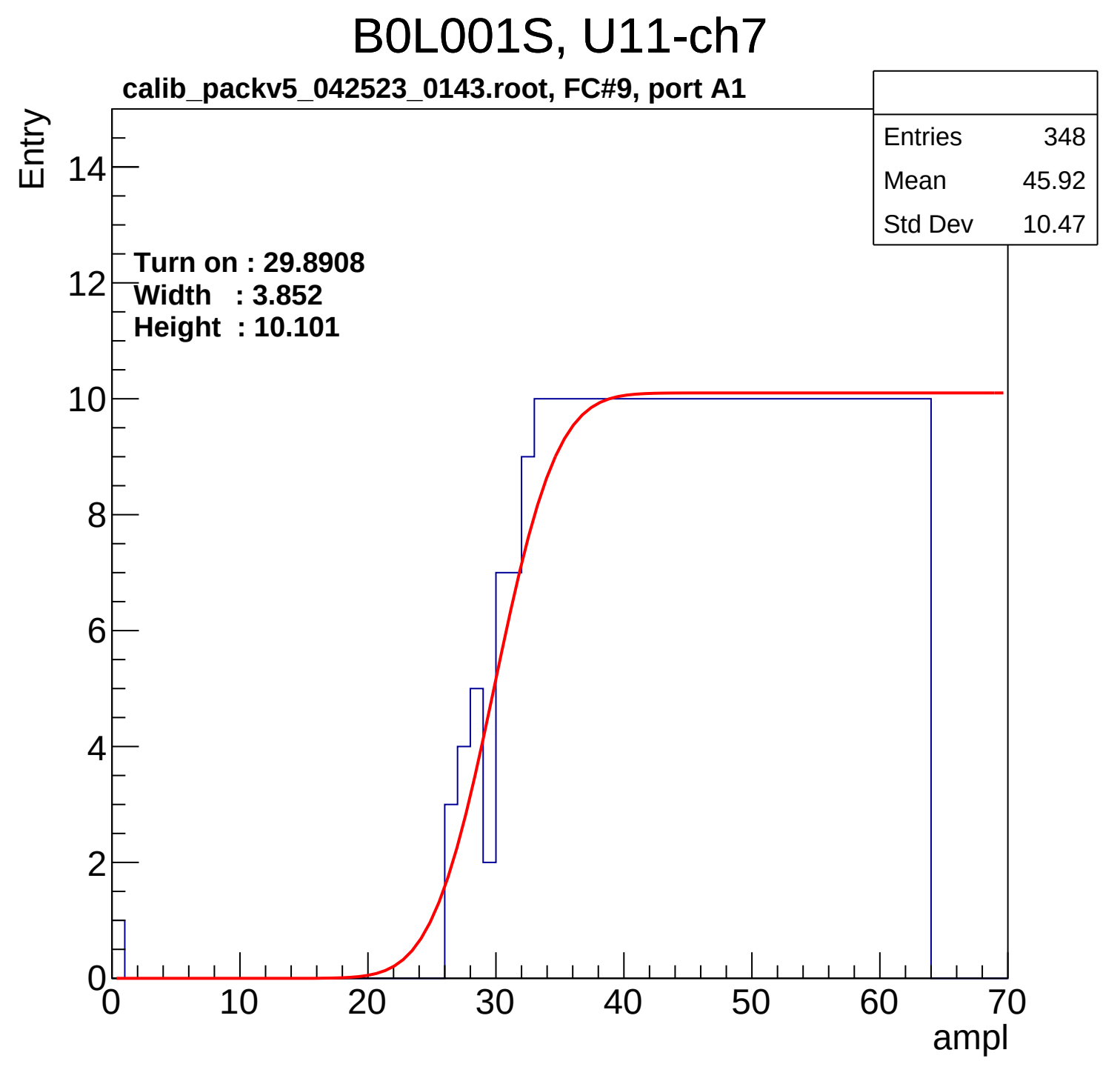
B0L001S, U11-ch7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 348
Mean 45.92
Std Dev 10.47
Turn on : 29.8908
Width : 3.852
Height : 10.101
Entry
ampl
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6
8
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12
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0
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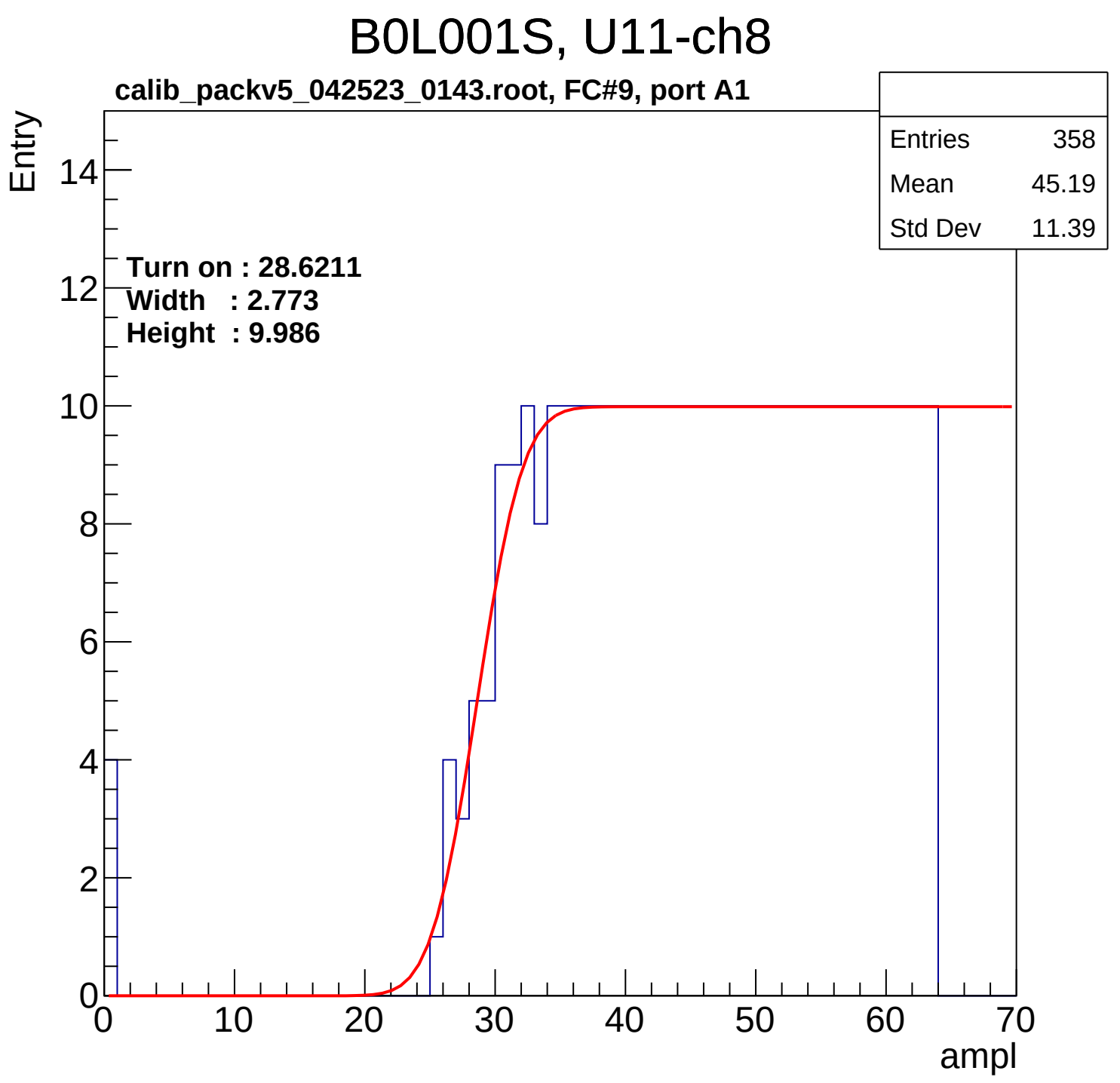
B0L001S, U11-ch8
calib_packv5_042523_0143.root, FC#9, port A1
Entries 358
Mean 45.19
Std Dev 11.39
Turn on : 28.6211
Width : 2.773
Height : 9.986
Entry
ampl
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2
4
6
8
10
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0
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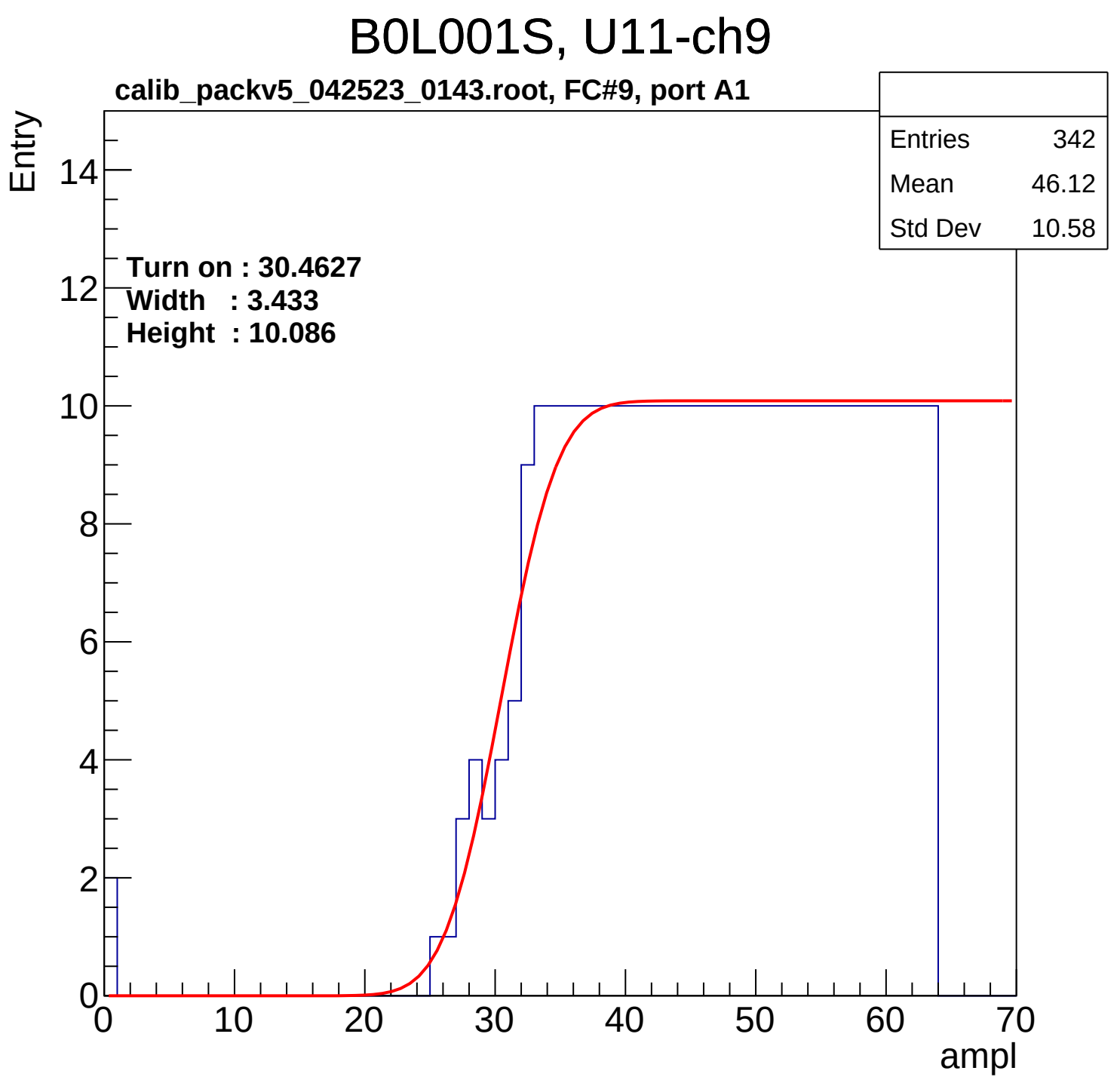
B0L001S, U11-ch9
calib_packv5_042523_0143.root, FC#9, port A1
Entries 342
Mean 46.12
Std Dev 10.58
Turn on : 30.4627
Width : 3.433
Height : 10.086
Entry
ampl
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2
4
6
8
10
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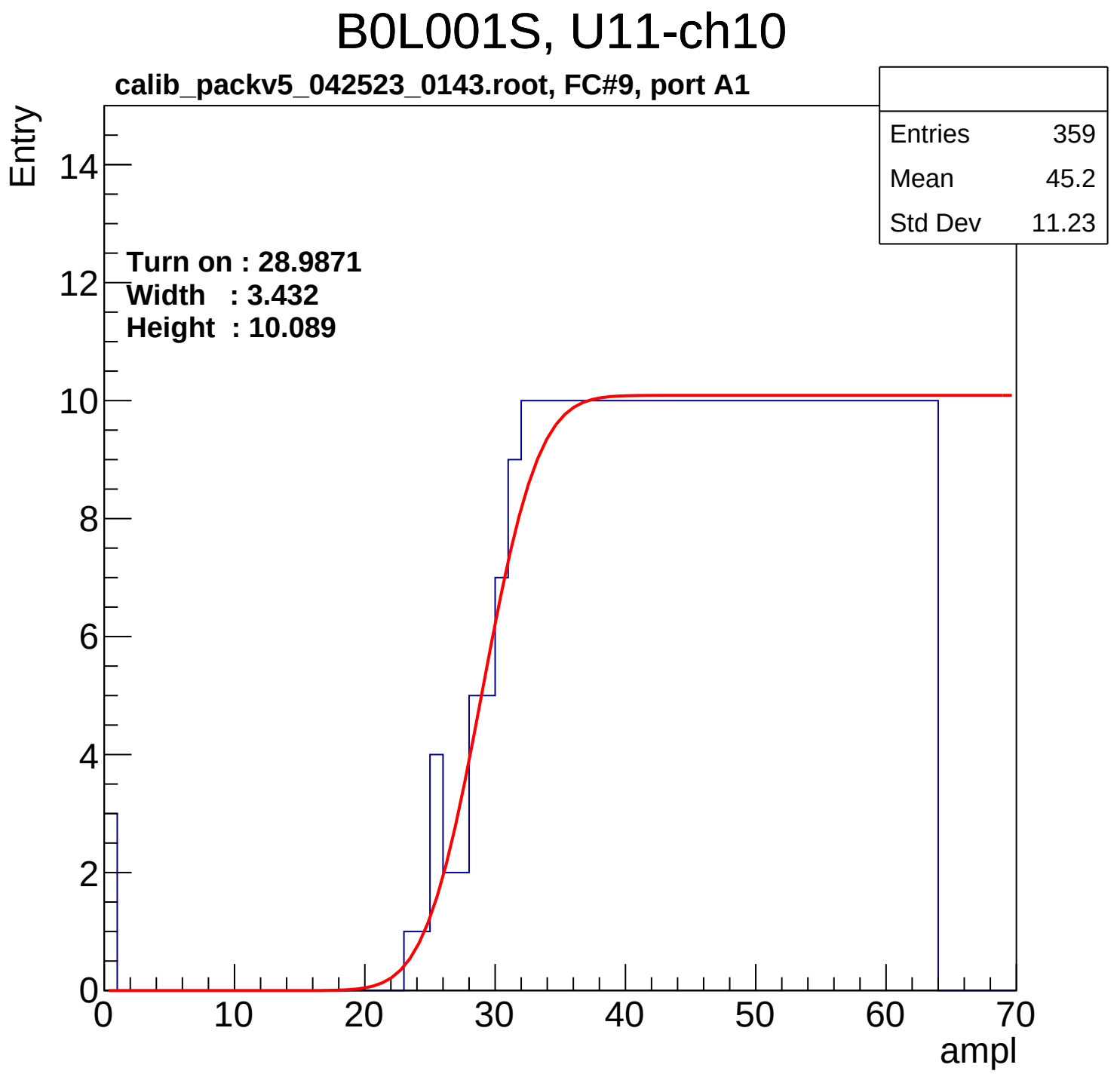
B0L001S, U11-ch10
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 45.2
Std Dev 11.23
Turn on : 28.9871
Width : 3.432
Height : 10.089
Entry
ampl
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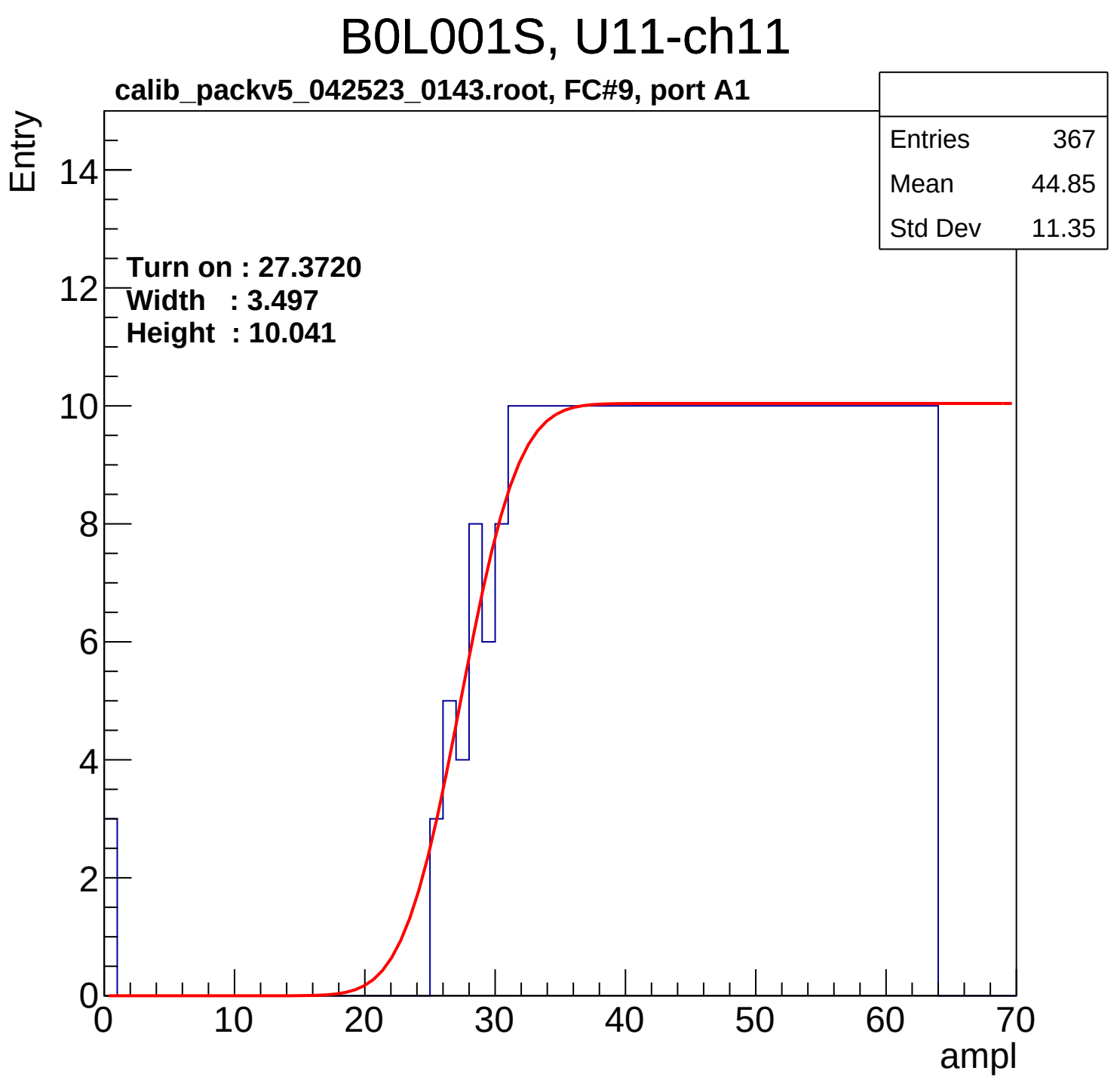
B0L001S, U11-ch11
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.85
Std Dev 11.35
Turn on : 27.3720
Width : 3.497
Height : 10.041
Entry
ampl
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6
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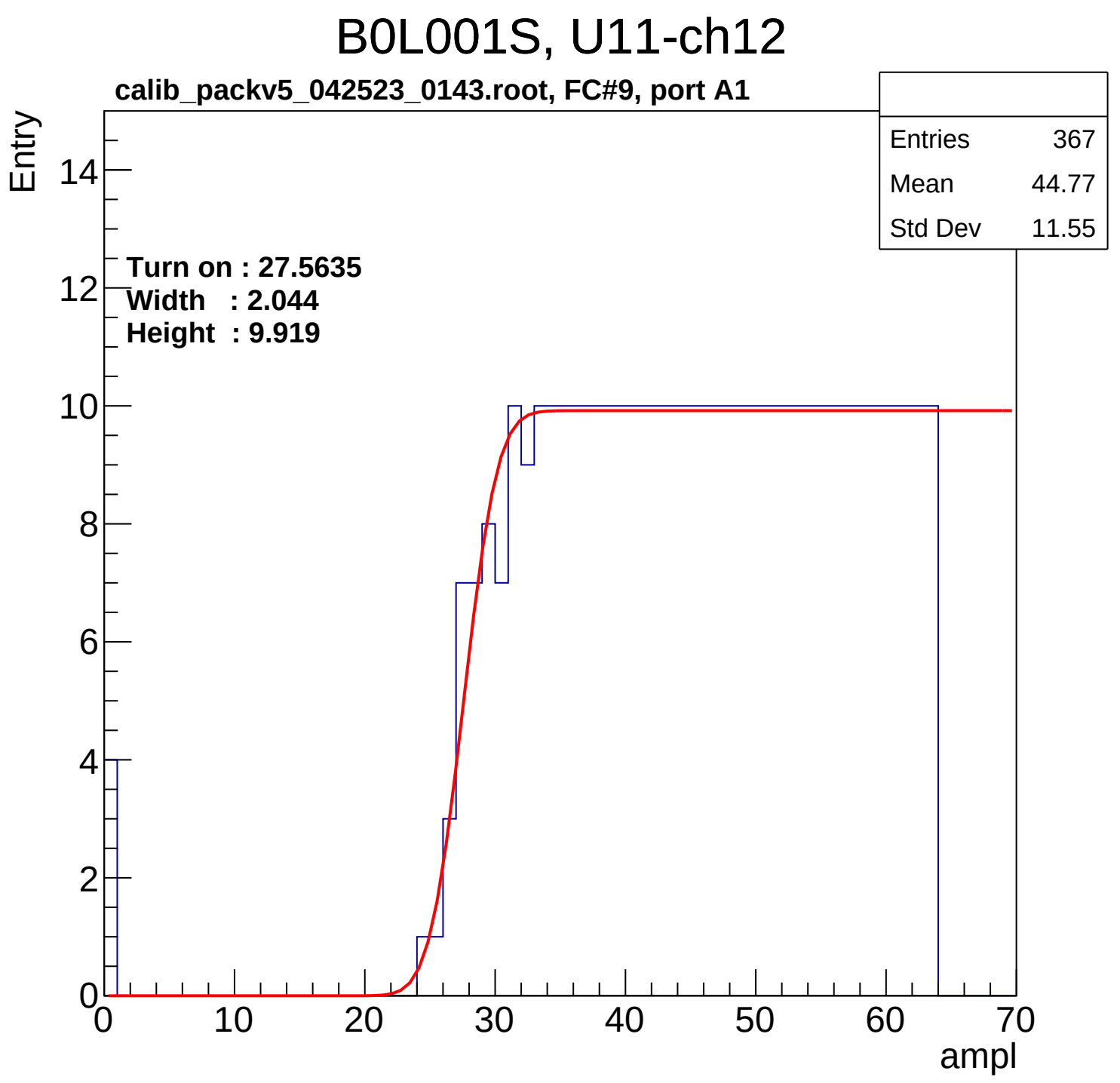
B0L001S, U11-ch12
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.77
Std Dev 11.55
Turn on : 27.5635
Width : 2.044
Height : 9.919
Entry
ampl
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6
8
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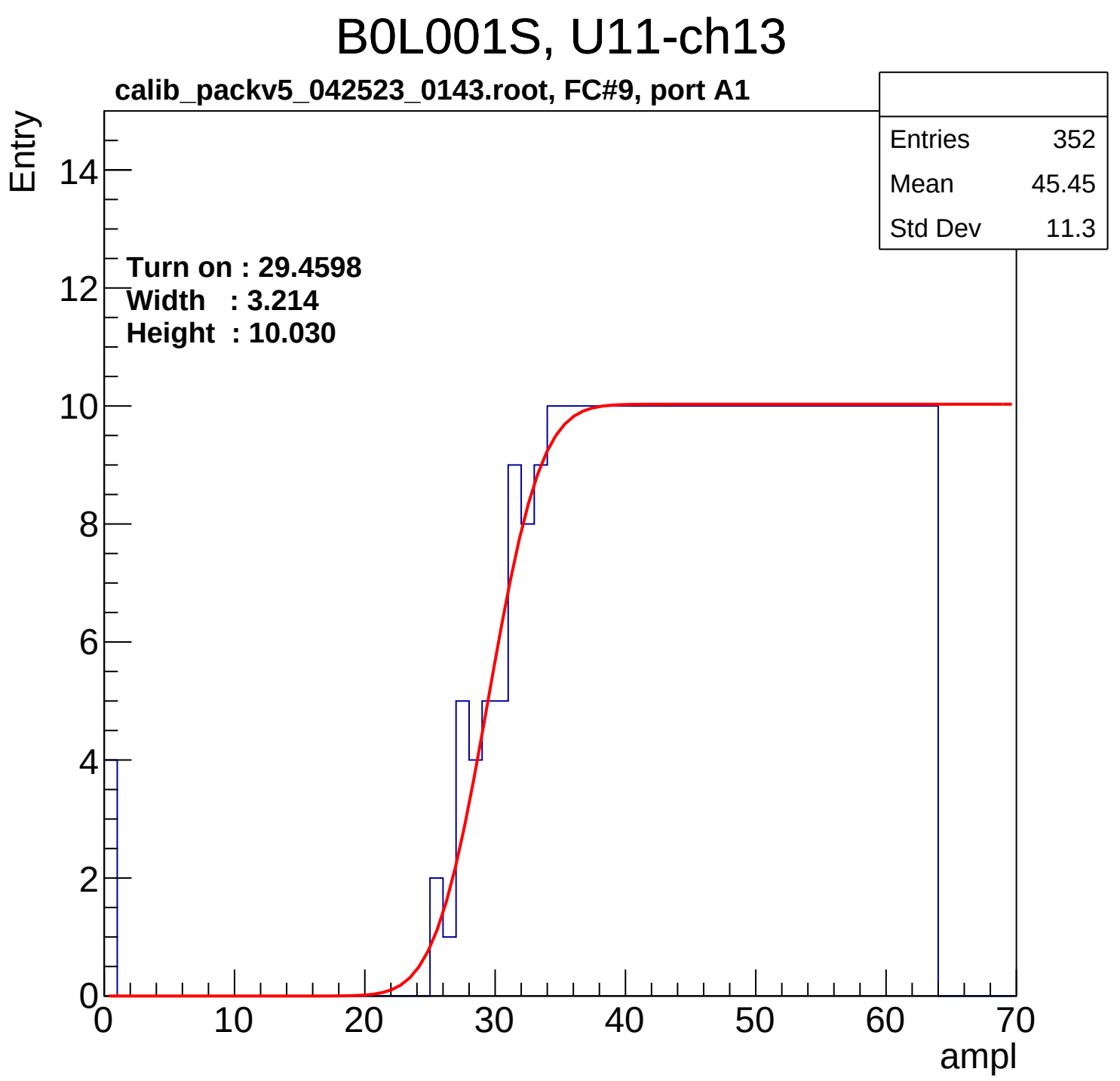
B0L001S, U11-ch13
calib_packv5_042523_0143.root, FC#9, port A1
Entries 352
Mean 45.45
Std Dev 11.3
Turn on : 29.4598
Width : 3.214
Height : 10.030
Entry
ampl
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6
8
10
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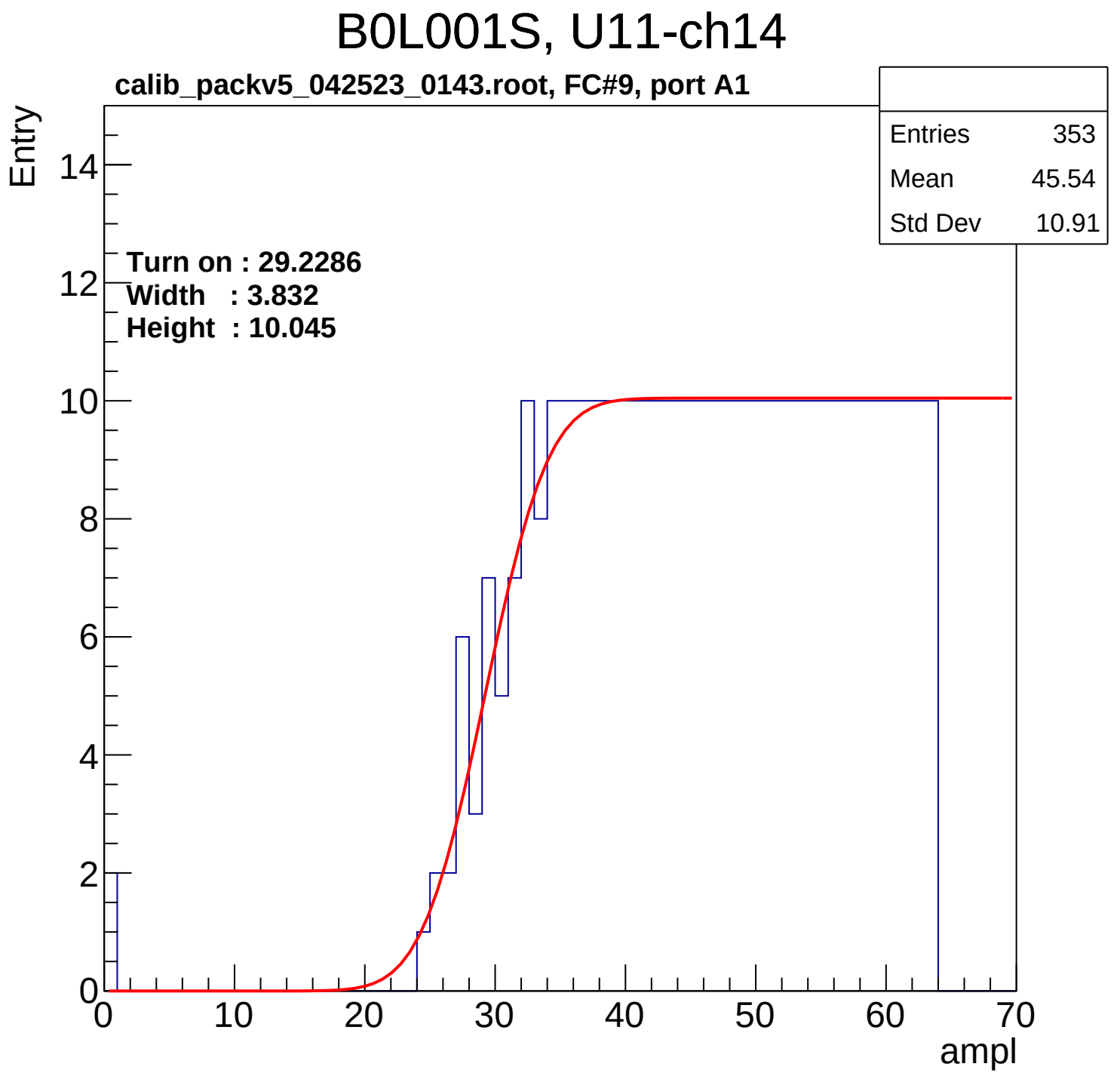
B0L001S, U11-ch14
calib_packv5_042523_0143.root, FC#9, port A1
Entries 353
Mean 45.54
Std Dev 10.91
Turn on : 29.2286
Width : 3.832
Height : 10.045
Entry
ampl
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6
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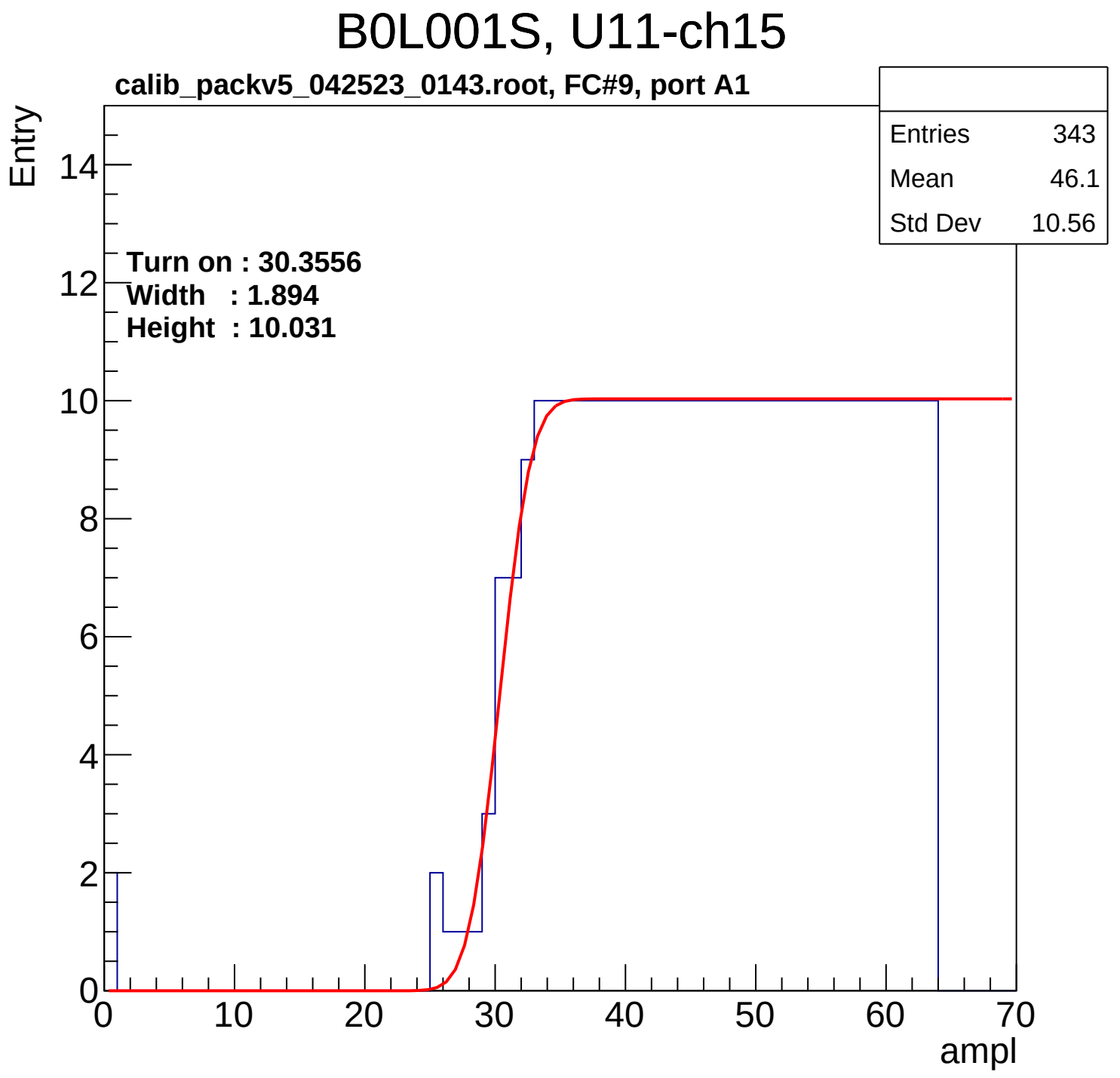
B0L001S, U11-ch15
calib_packv5_042523_0143.root, FC#9, port A1
Entries 343
Mean 46.1
Std Dev 10.56
Turn on : 30.3556
Width : 1.894
Height : 10.031
Entry
ampl
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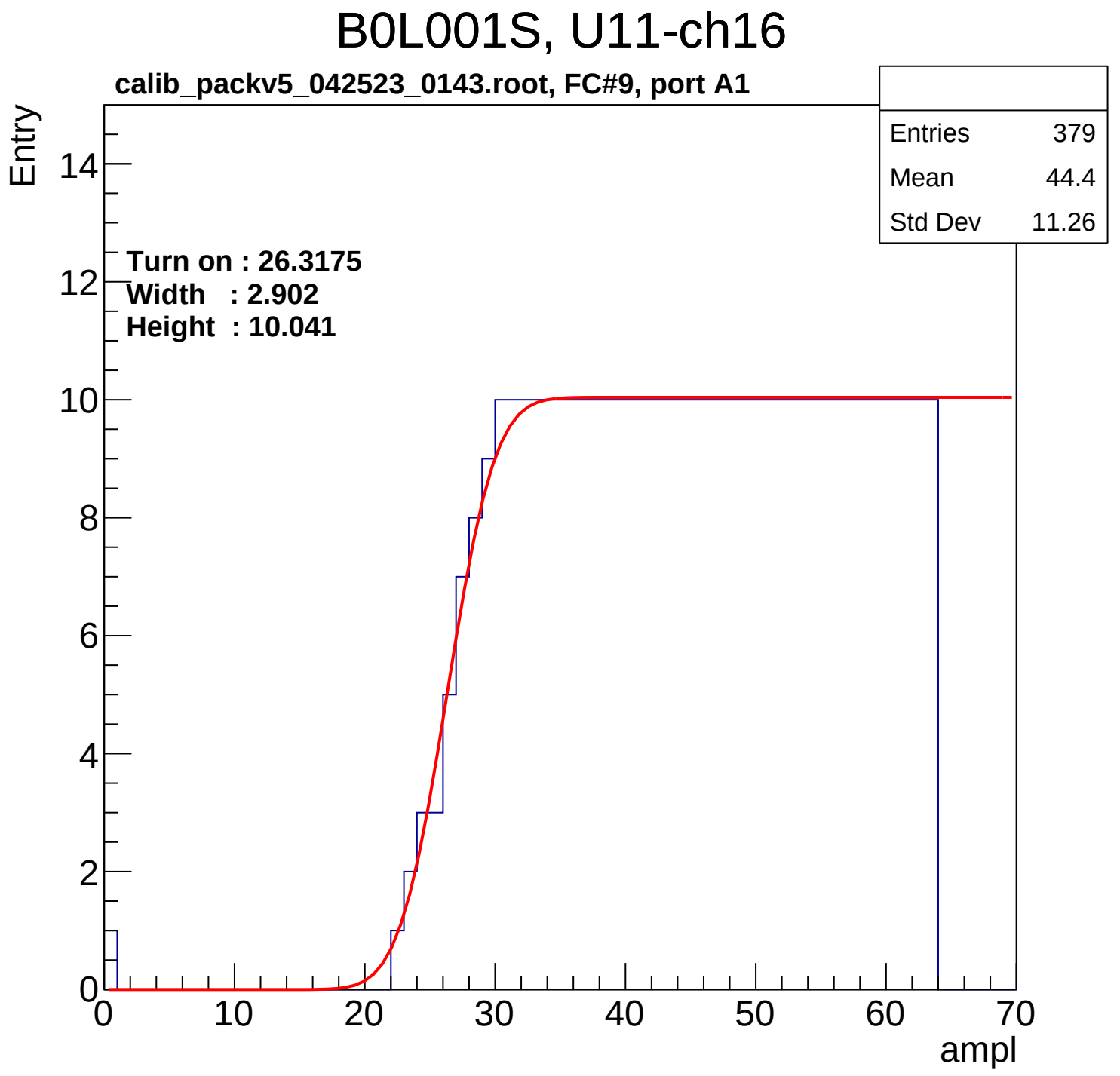
B0L001S, U11-ch16
calib_packv5_042523_0143.root, FC#9, port A1
Entries 379
Mean 44.4
Std Dev 11.26
Turn on : 26.3175
Width : 2.902
Height : 10.041
Entry
ampl
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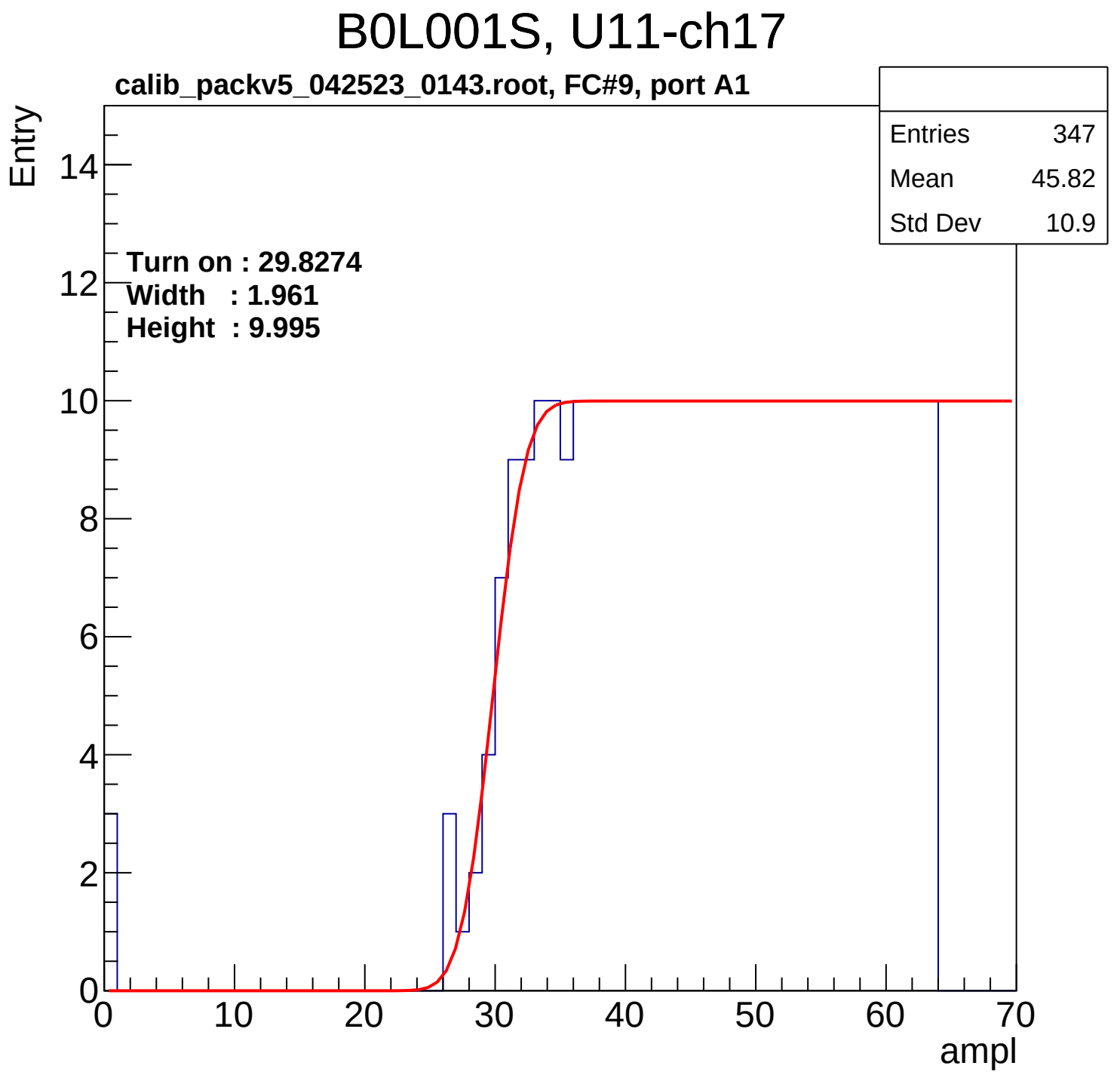
B0L001S, U11-ch17
calib_packv5_042523_0143.root, FC#9, port A1
Entries 347
Mean 45.82
Std Dev 10.9
Turn on : 29.8274
Width : 1.961
Height : 9.995
Entry
ampl
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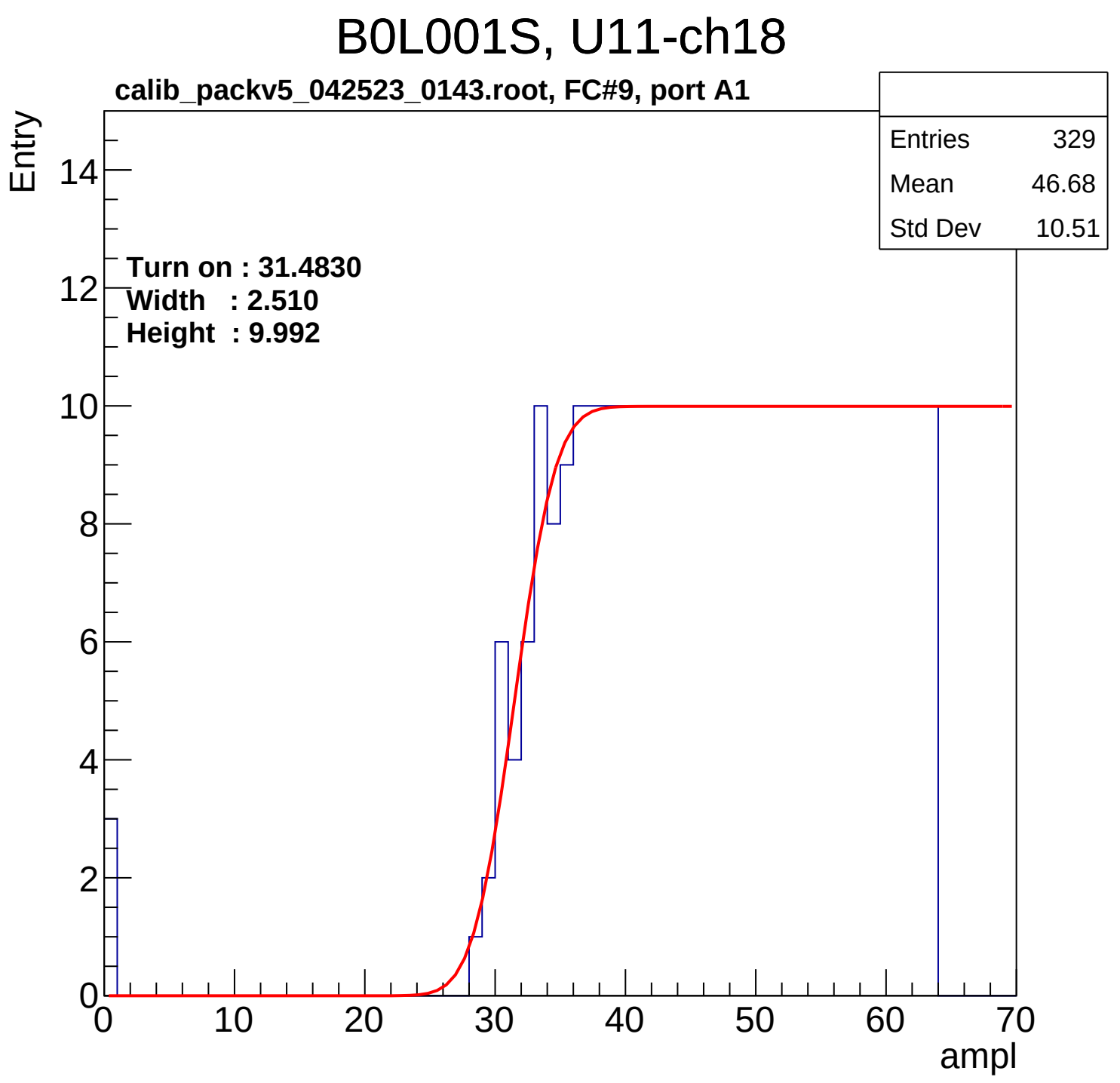
B0L001S, U11-ch18
calib_packv5_042523_0143.root, FC#9, port A1
Entries 329
Mean 46.68
Std Dev 10.51
Turn on : 31.4830
Width : 2.510
Height : 9.992
Entry
ampl
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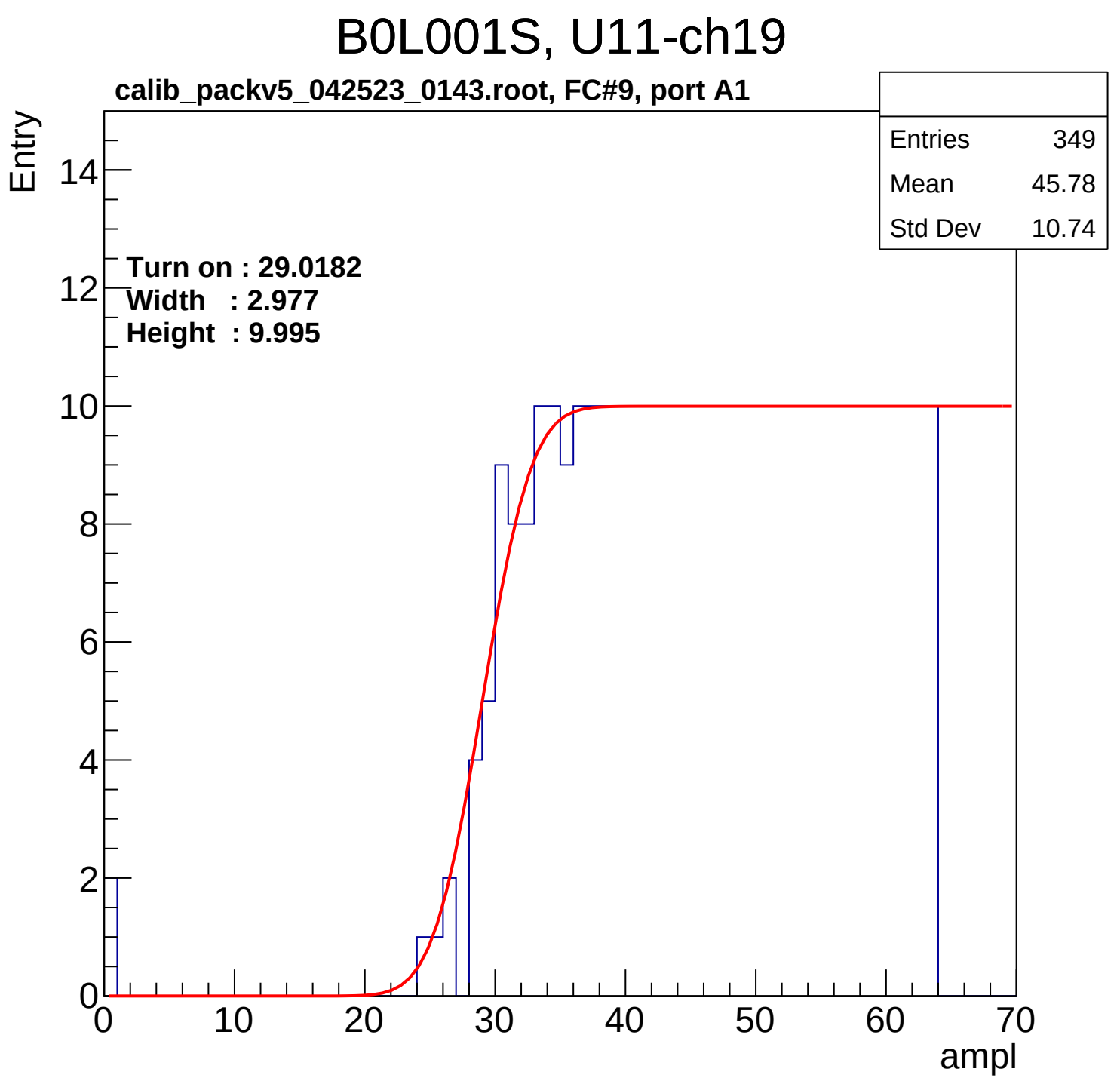
B0L001S, U11-ch19
calib_packv5_042523_0143.root, FC#9, port A1
Entries 349
Mean 45.78
Std Dev 10.74
Turn on : 29.0182
Width : 2.977
Height : 9.995
Entry
ampl
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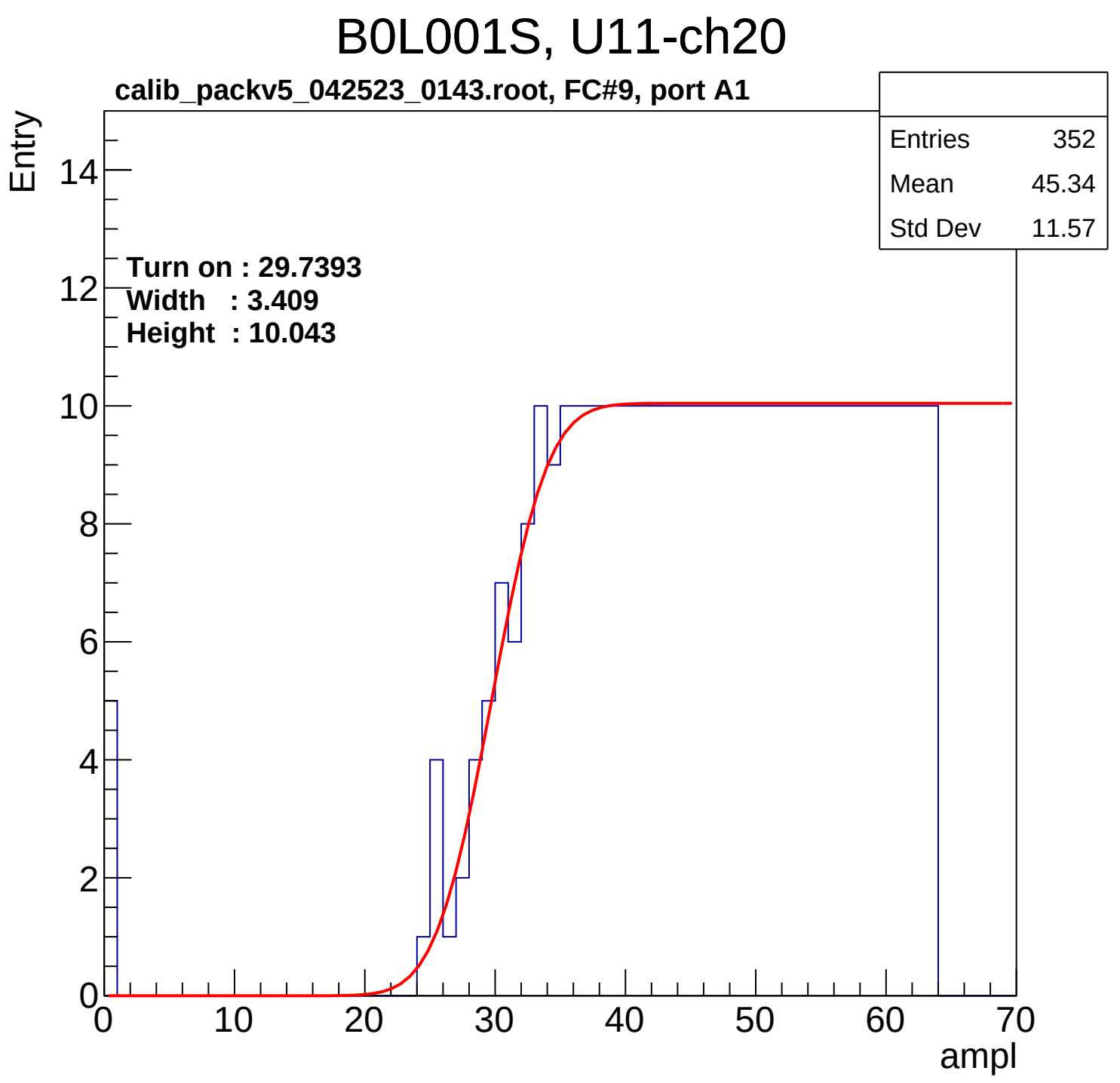
B0L001S, U11-ch20
calib_packv5_042523_0143.root, FC#9, port A1
Entries 352
Mean 45.34
Std Dev 11.57
Turn on : 29.7393
Width : 3.409
Height : 10.043
Entry
ampl
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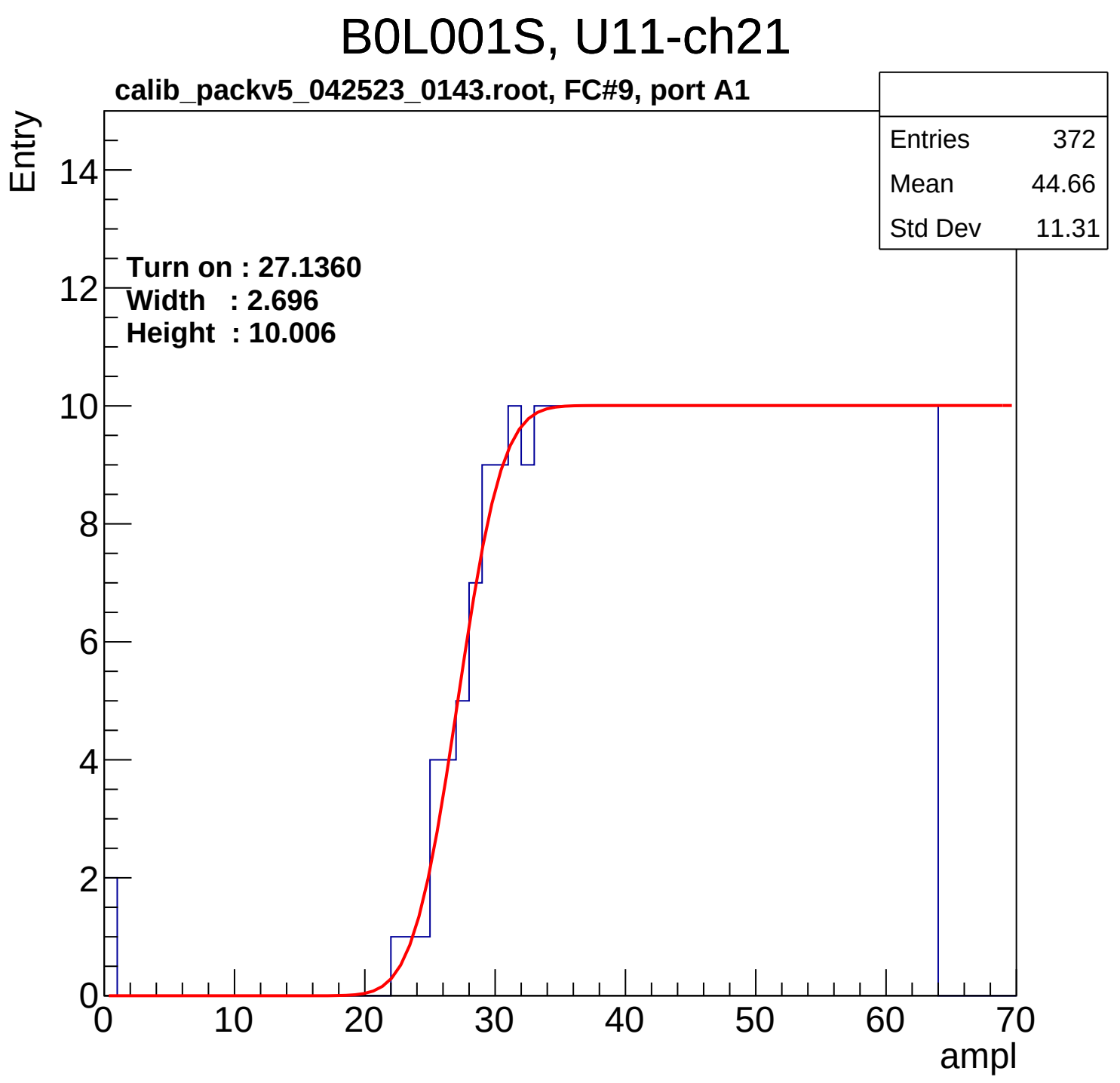
B0L001S, U11-ch21
calib_packv5_042523_0143.root, FC#9, port A1
Entries 372
Mean 44.66
Std Dev 11.31
Turn on : 27.1360
Width : 2.696
Height : 10.006
Entry
ampl
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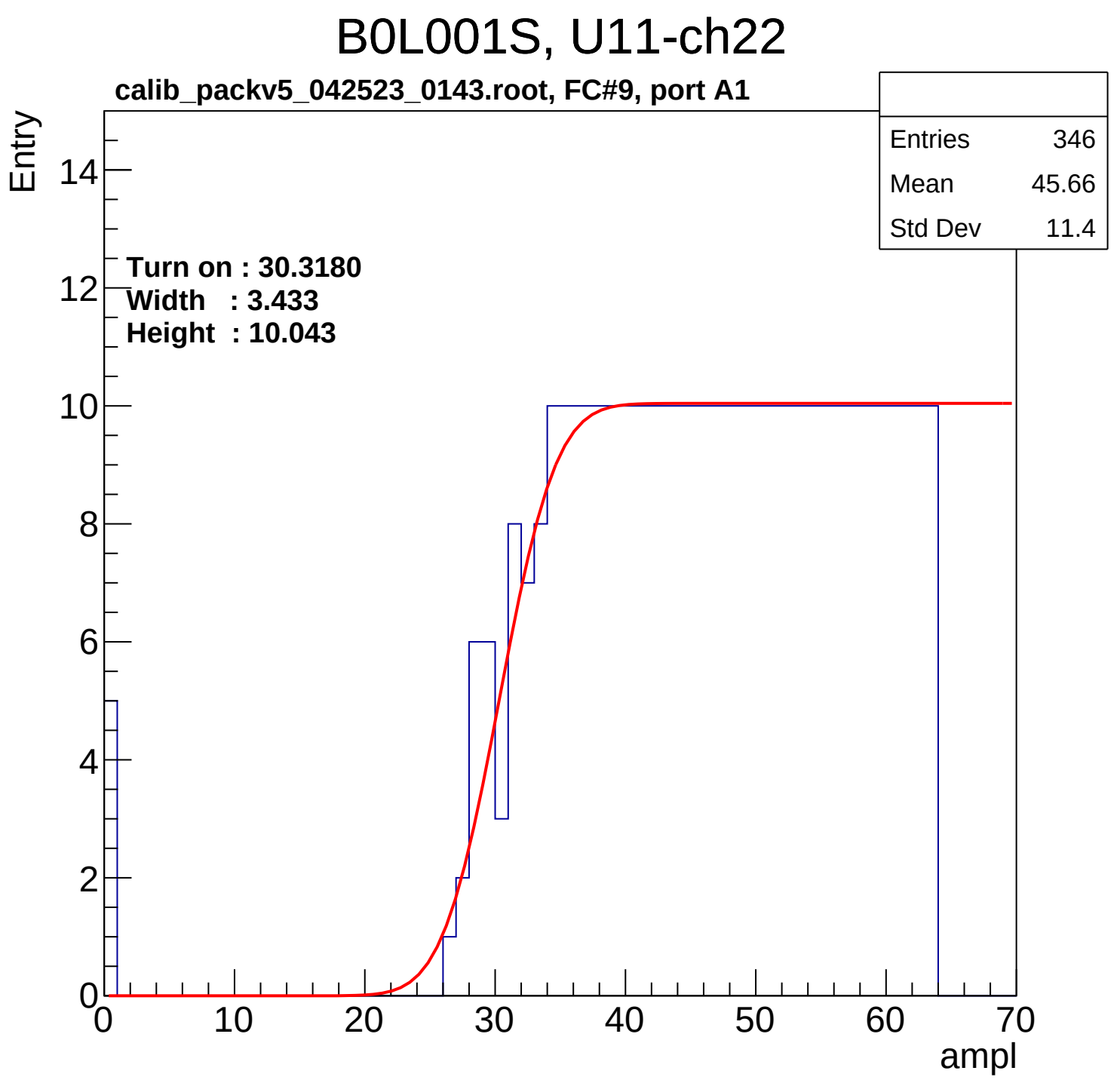
B0L001S, U11-ch22
calib_packv5_042523_0143.root, FC#9, port A1
Entries 346
Mean 45.66
Std Dev 11.4
Turn on : 30.3180
Width : 3.433
Height : 10.043
Entry
ampl
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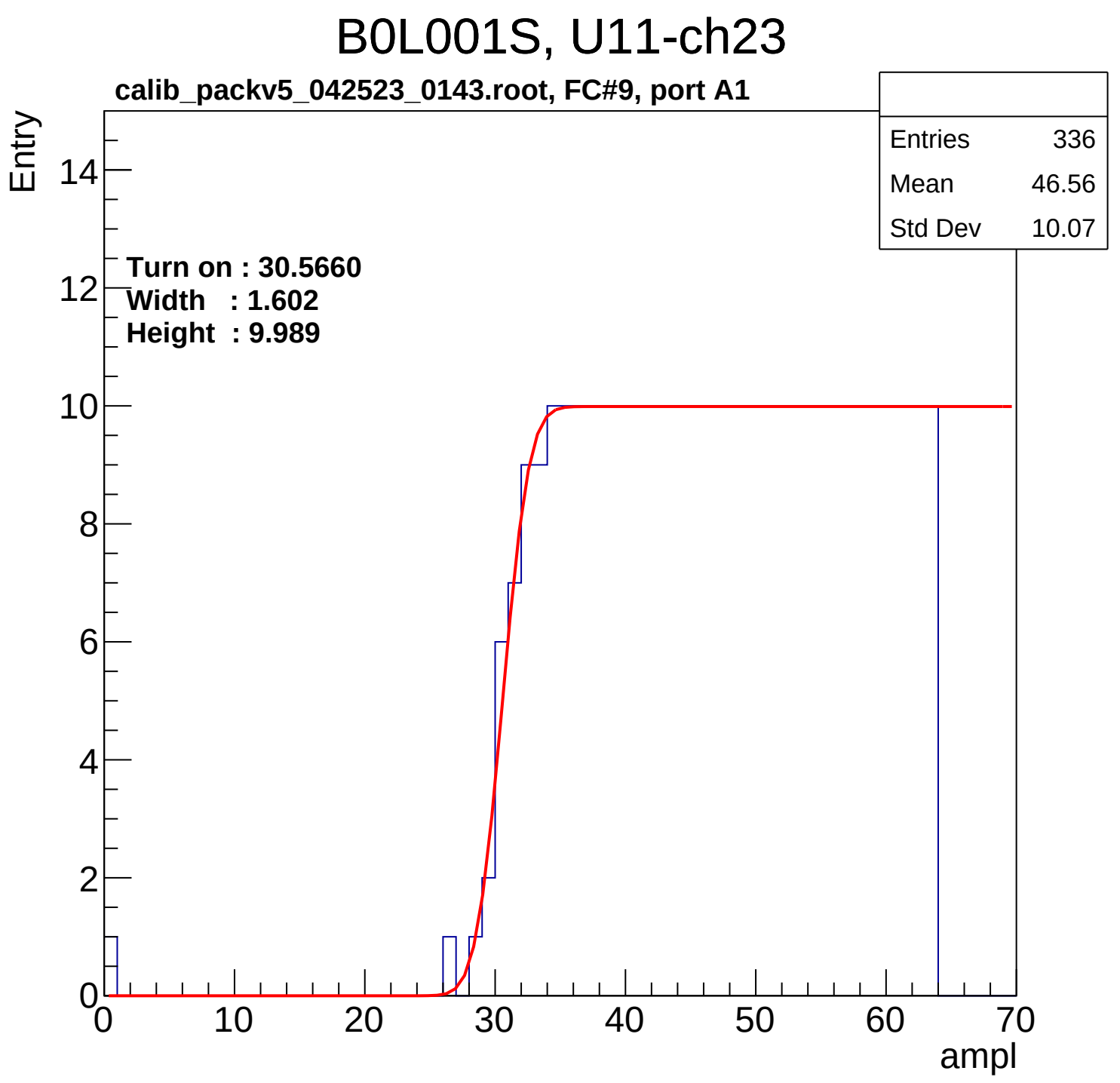
B0L001S, U11-ch23
calib_packv5_042523_0143.root, FC#9, port A1
Entries 336
Mean 46.56
Std Dev 10.07
Turn on : 30.5660
Width : 1.602
Height : 9.989
Entry
ampl
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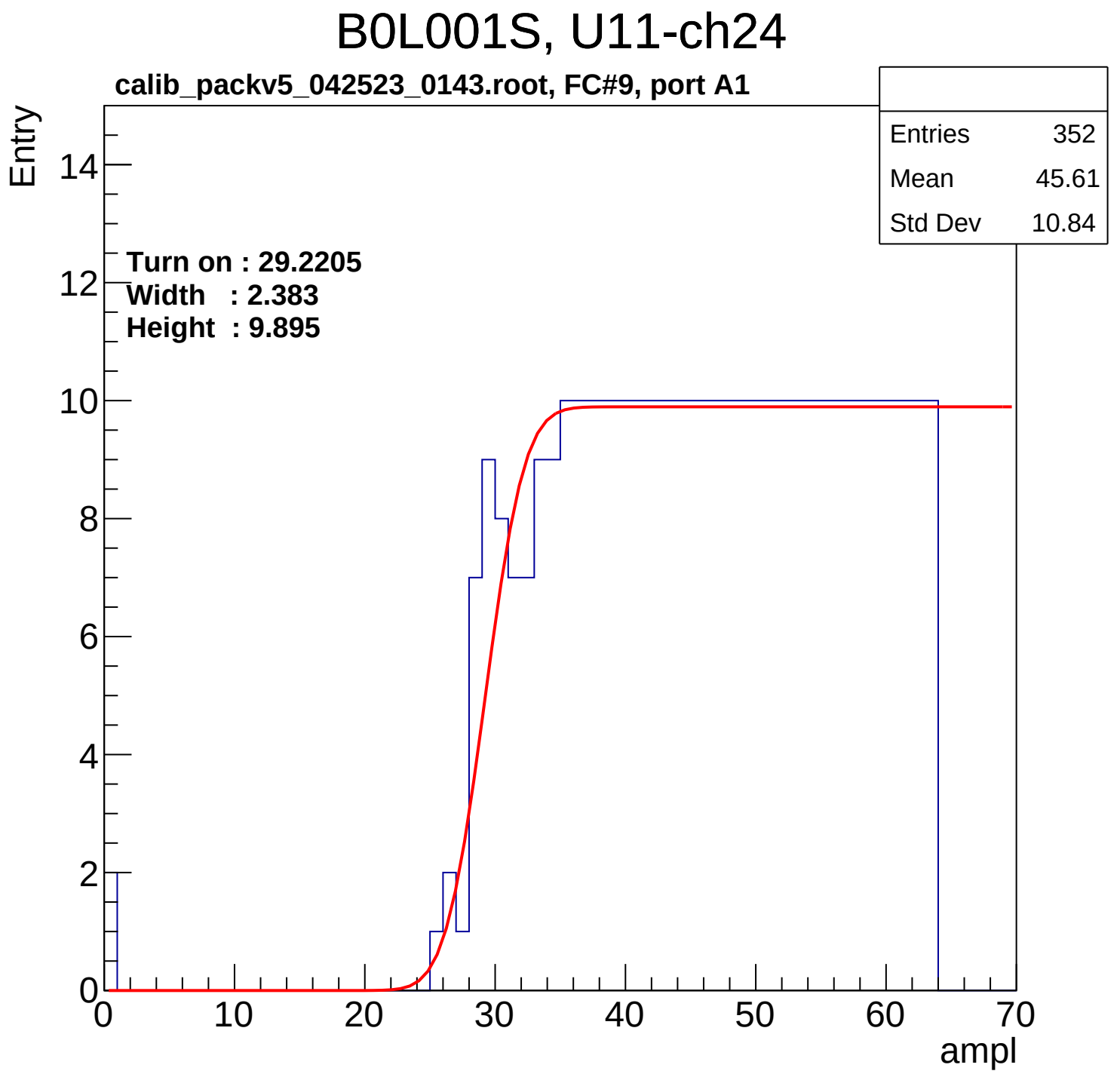
B0L001S, U11-ch24
calib_packv5_042523_0143.root, FC#9, port A1
Entries 352
Mean 45.61
Std Dev 10.84
Turn on : 29.2205
Width : 2.383
Height : 9.895
Entry
ampl
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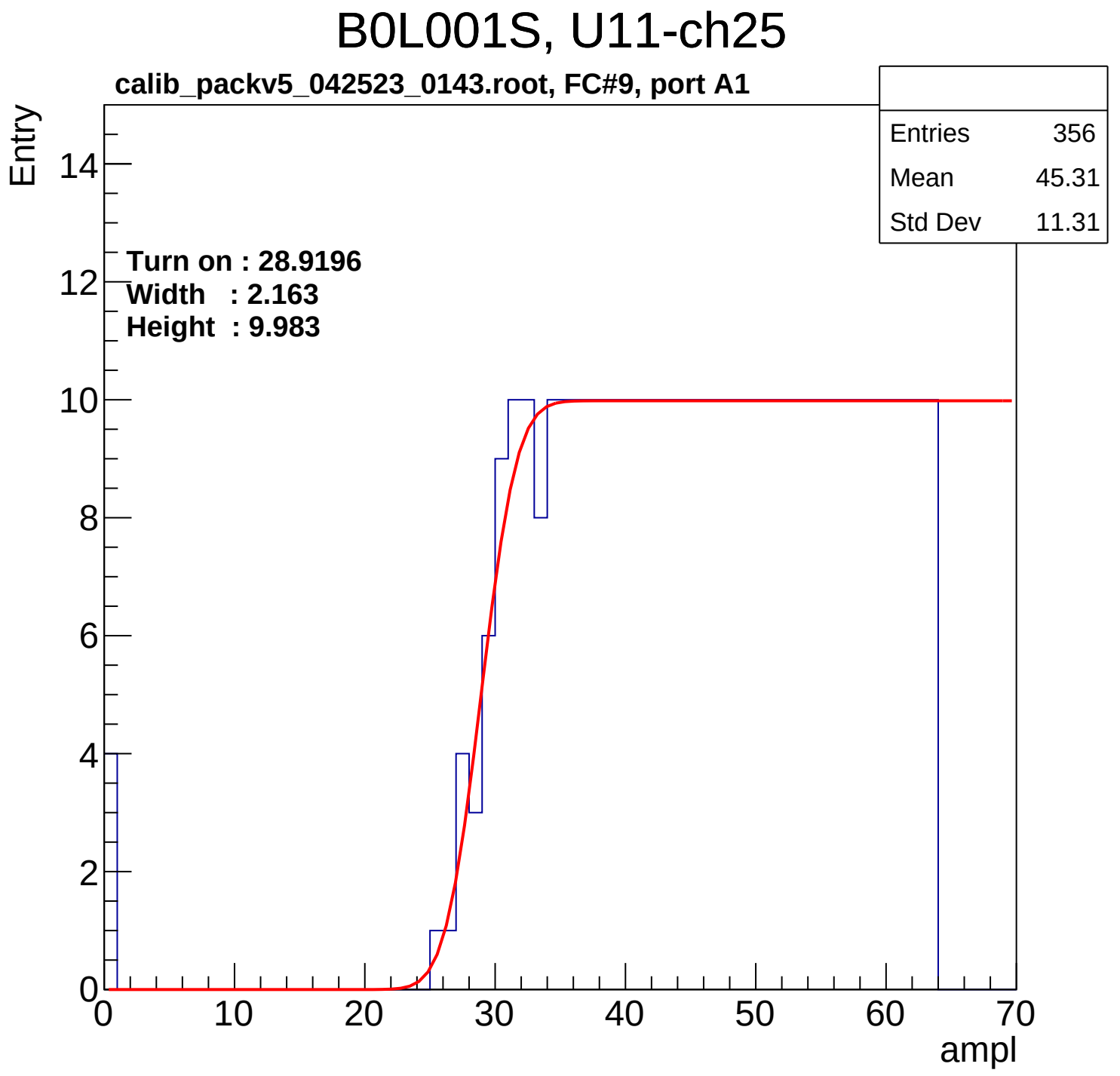
B0L001S, U11-ch25
calib_packv5_042523_0143.root, FC#9, port A1
Entries 356
Mean 45.31
Std Dev 11.31
Turn on : 28.9196
Width : 2.163
Height : 9.983
Entry
ampl
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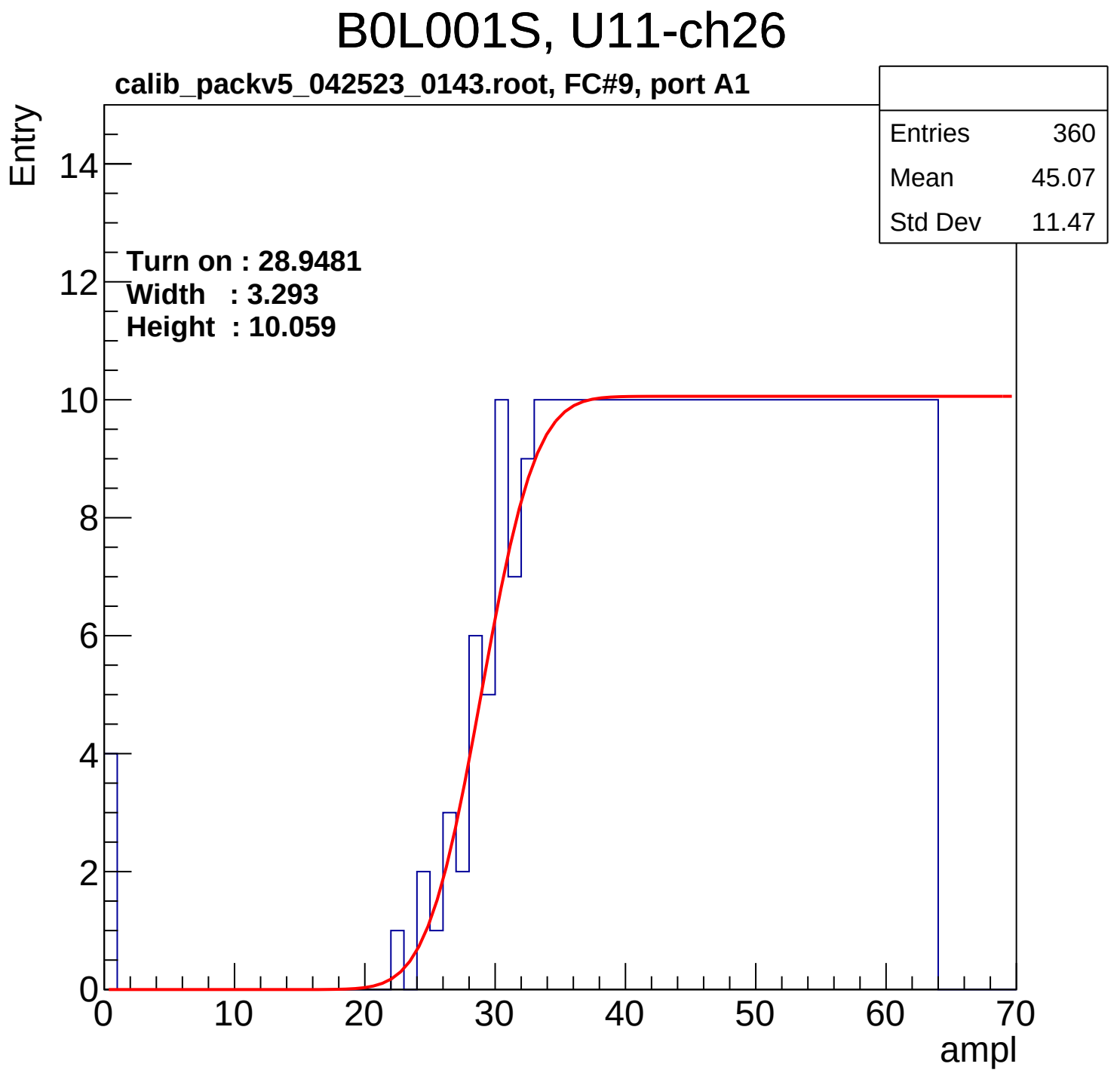
B0L001S, U11-ch26
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 45.07
Std Dev 11.47
Turn on : 28.9481
Width : 3.293
Height : 10.059
Entry
ampl
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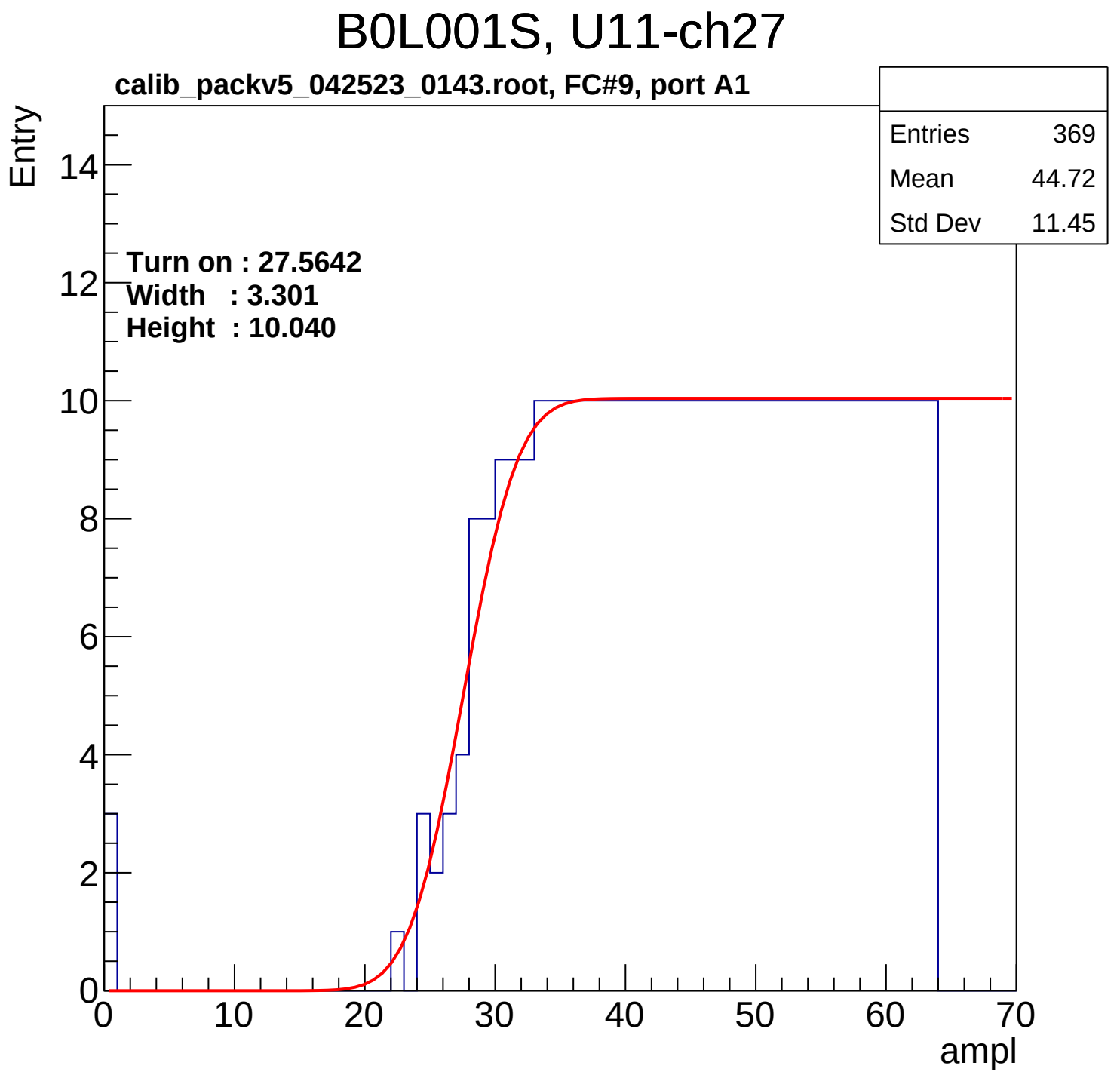
B0L001S, U11-ch27
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.72
Std Dev 11.45
Turn on : 27.5642
Width : 3.301
Height : 10.040
Entry
ampl
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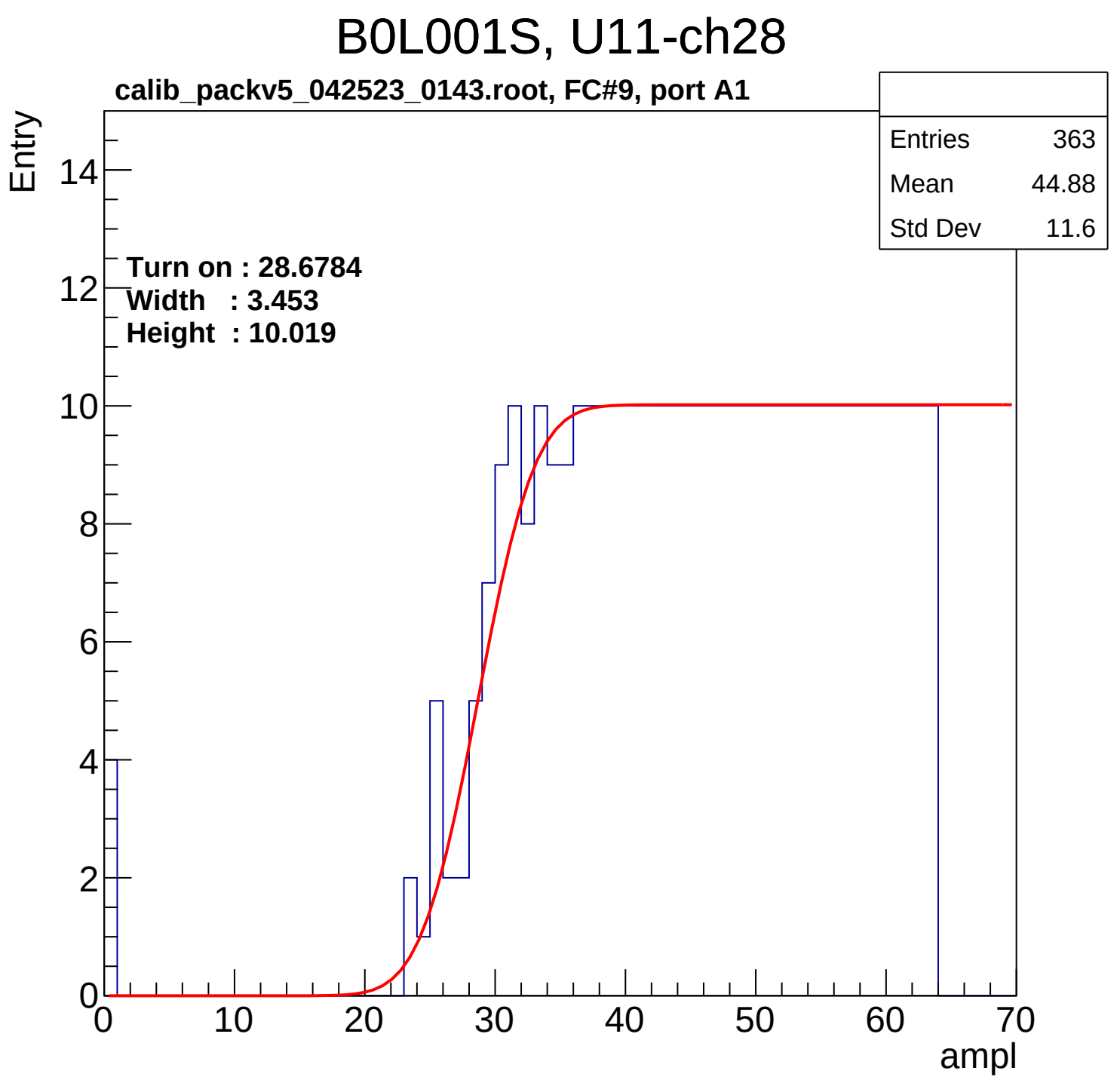
B0L001S, U11-ch28
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 44.88
Std Dev 11.6
Turn on : 28.6784
Width : 3.453
Height : 10.019
Entry
ampl
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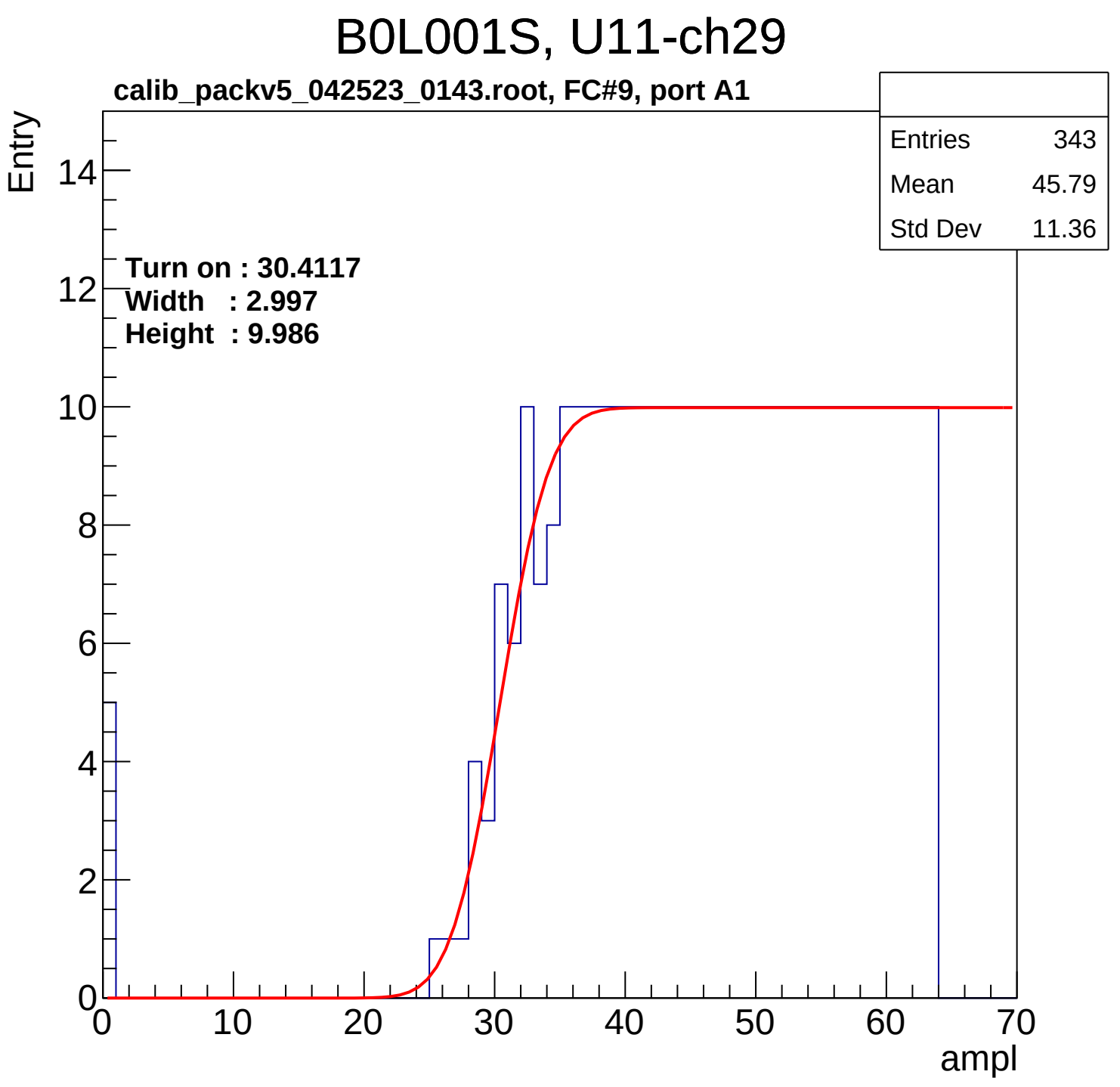
B0L001S, U11-ch29
calib_packv5_042523_0143.root, FC#9, port A1
Entries 343
Mean 45.79
Std Dev 11.36
Turn on : 30.4117
Width : 2.997
Height : 9.986
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ampl
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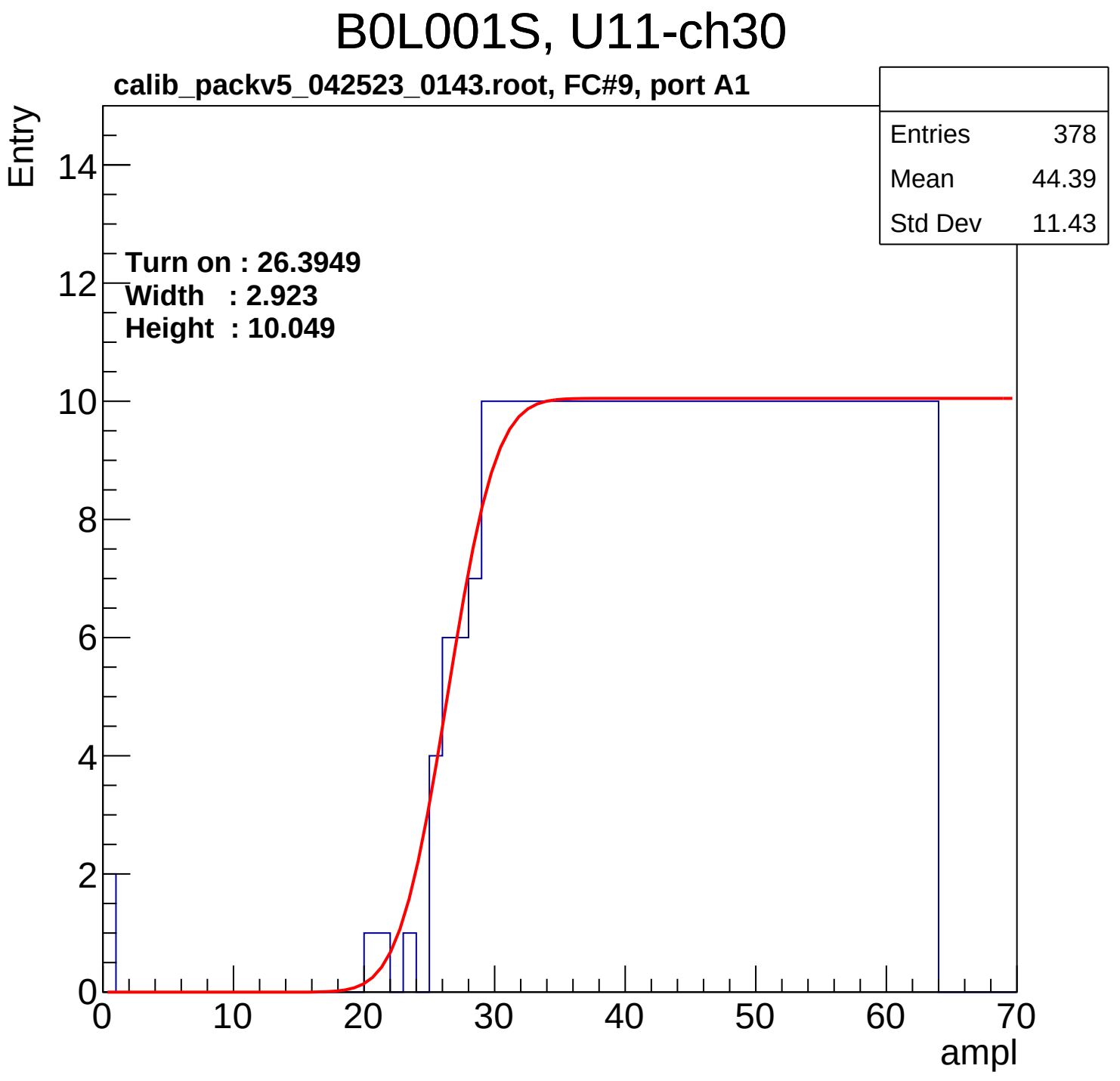
B0L001S, U11-ch30
calib_packv5_042523_0143.root, FC#9, port A1
Entries 378
Mean 44.39
Std Dev 11.43
Turn on : 26.3949
Width : 2.923
Height : 10.049
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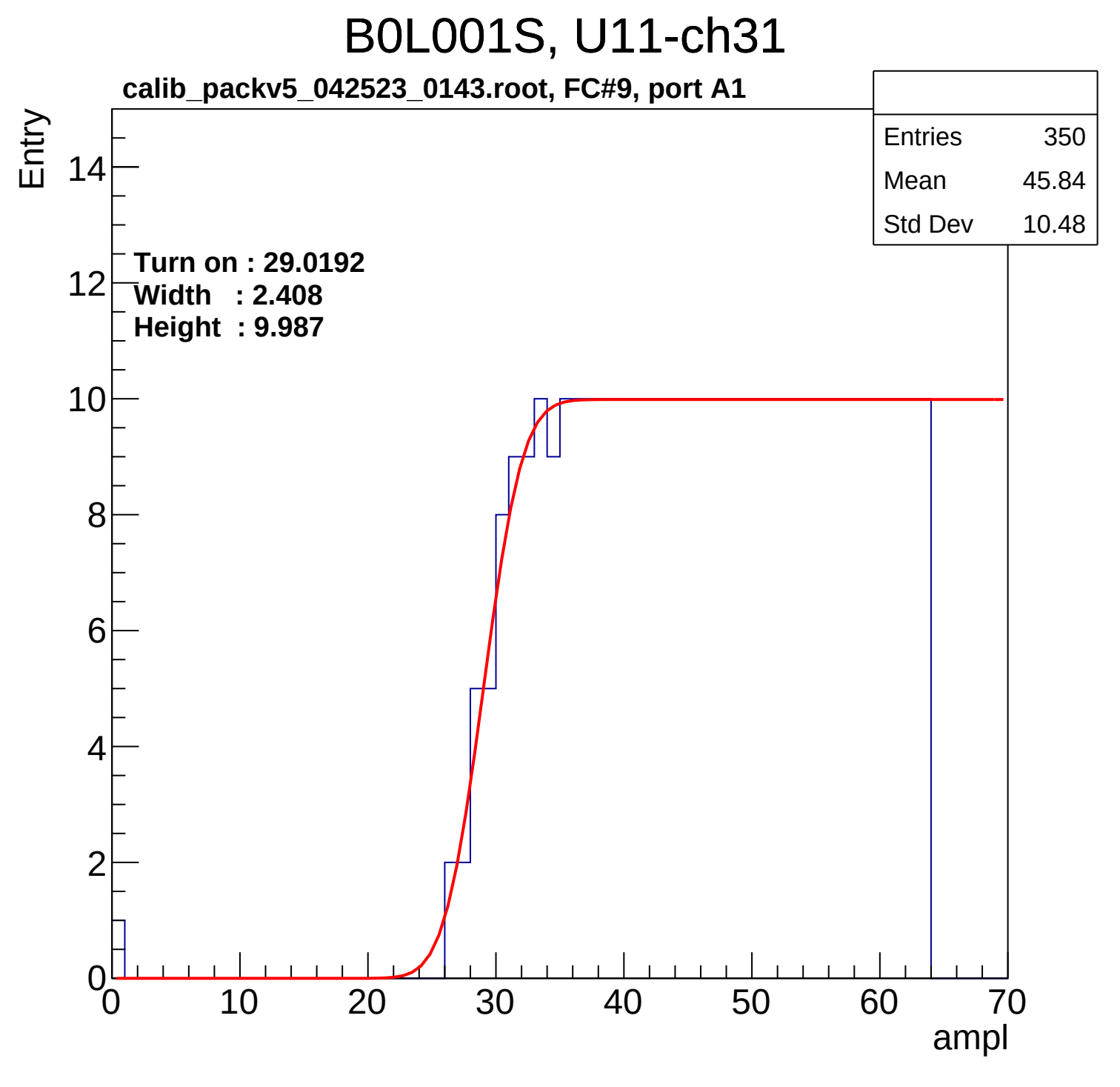
B0L001S, U11-ch31
calib_packv5_042523_0143.root, FC#9, port A1
Entries 350
Mean 45.84
Std Dev 10.48
Turn on : 29.0192
Width : 2.408
Height : 9.987
Entry
ampl
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2
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8
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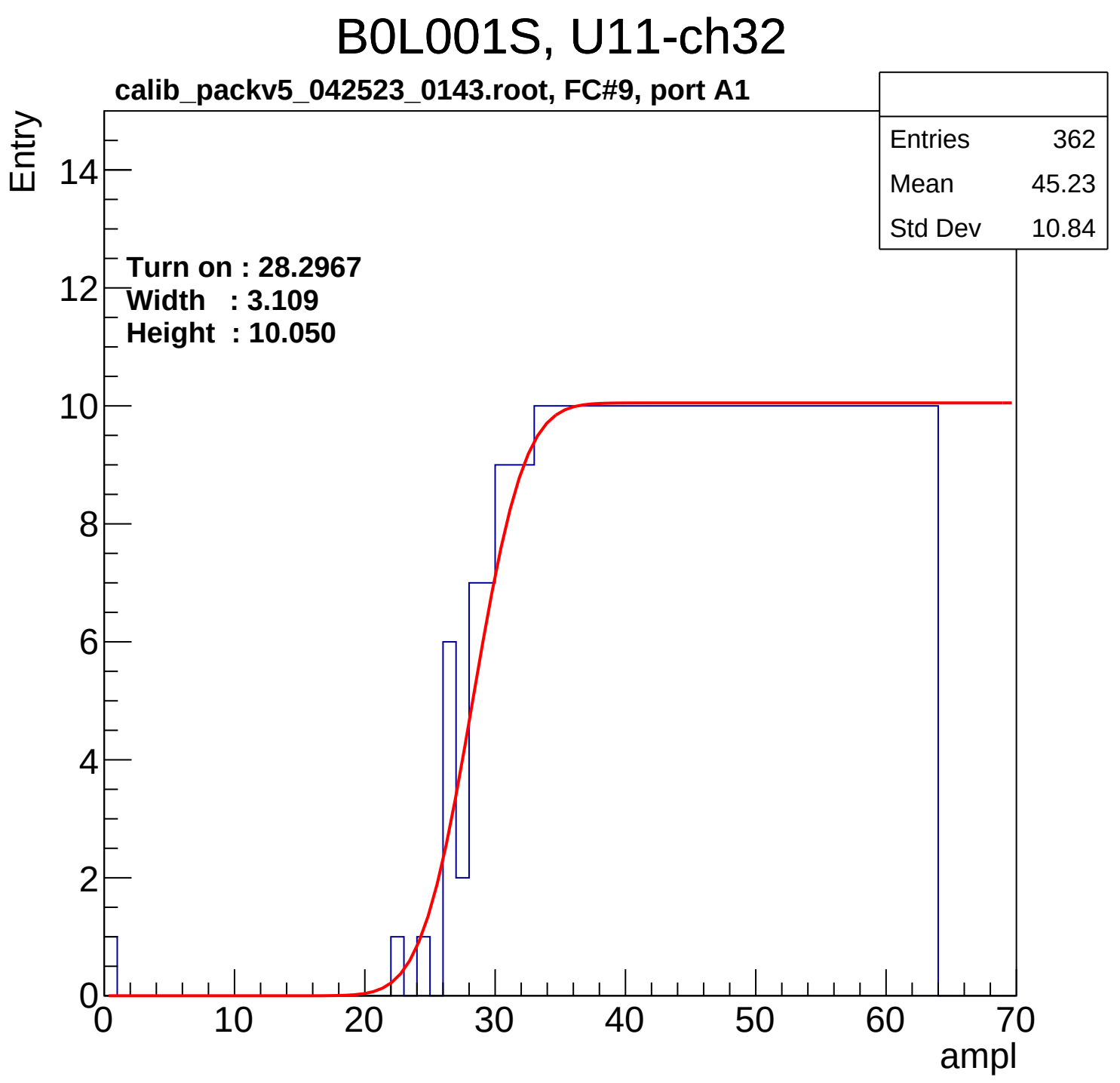
B0L001S, U11-ch32
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 45.23
Std Dev 10.84
Turn on : 28.2967
Width : 3.109
Height : 10.050
Entry
ampl
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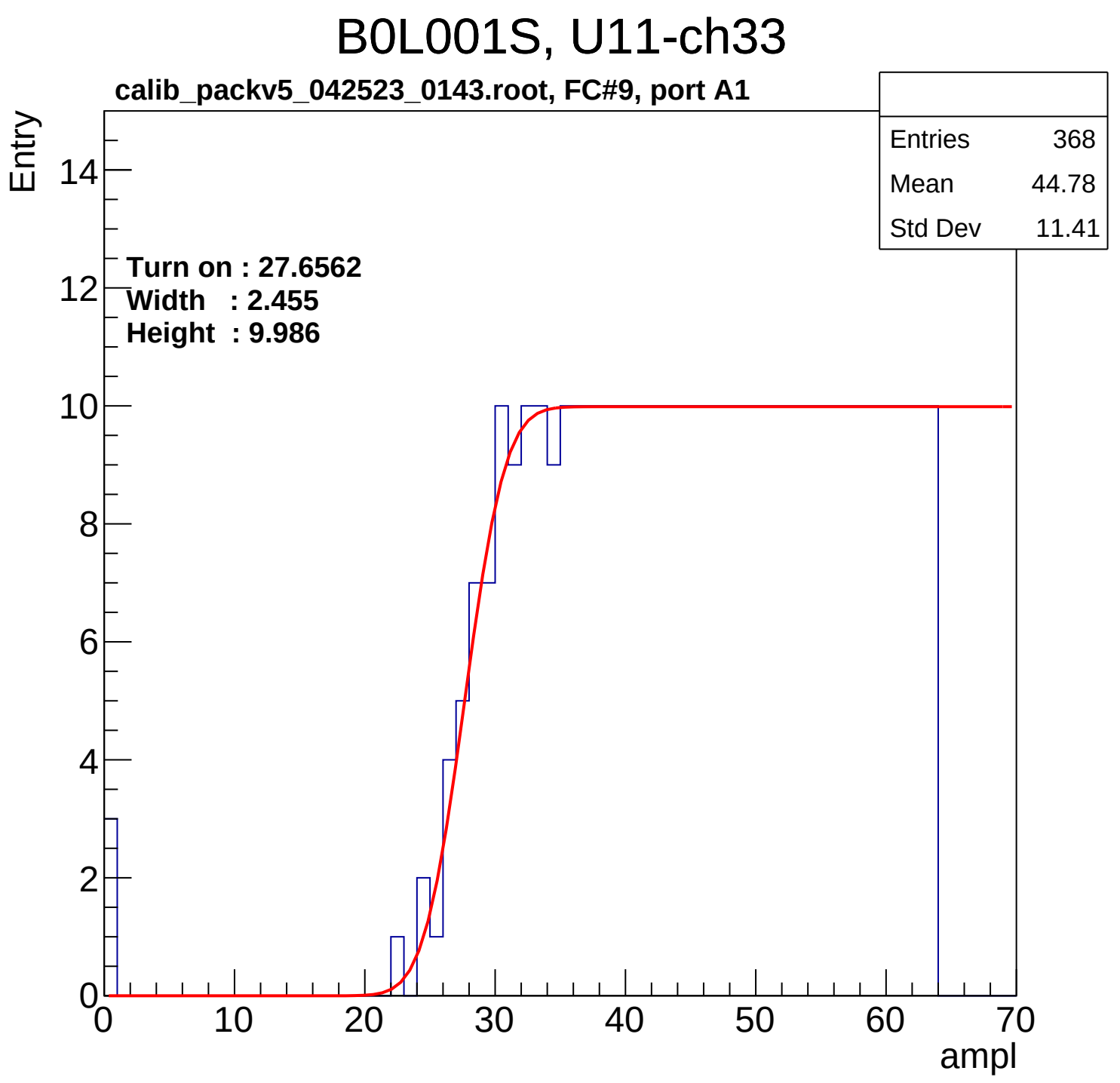
B0L001S, U11-ch33
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.78
Std Dev 11.41
Turn on : 27.6562
Width : 2.455
Height : 9.986
Entry
ampl
0
2
4
6
8
10
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0
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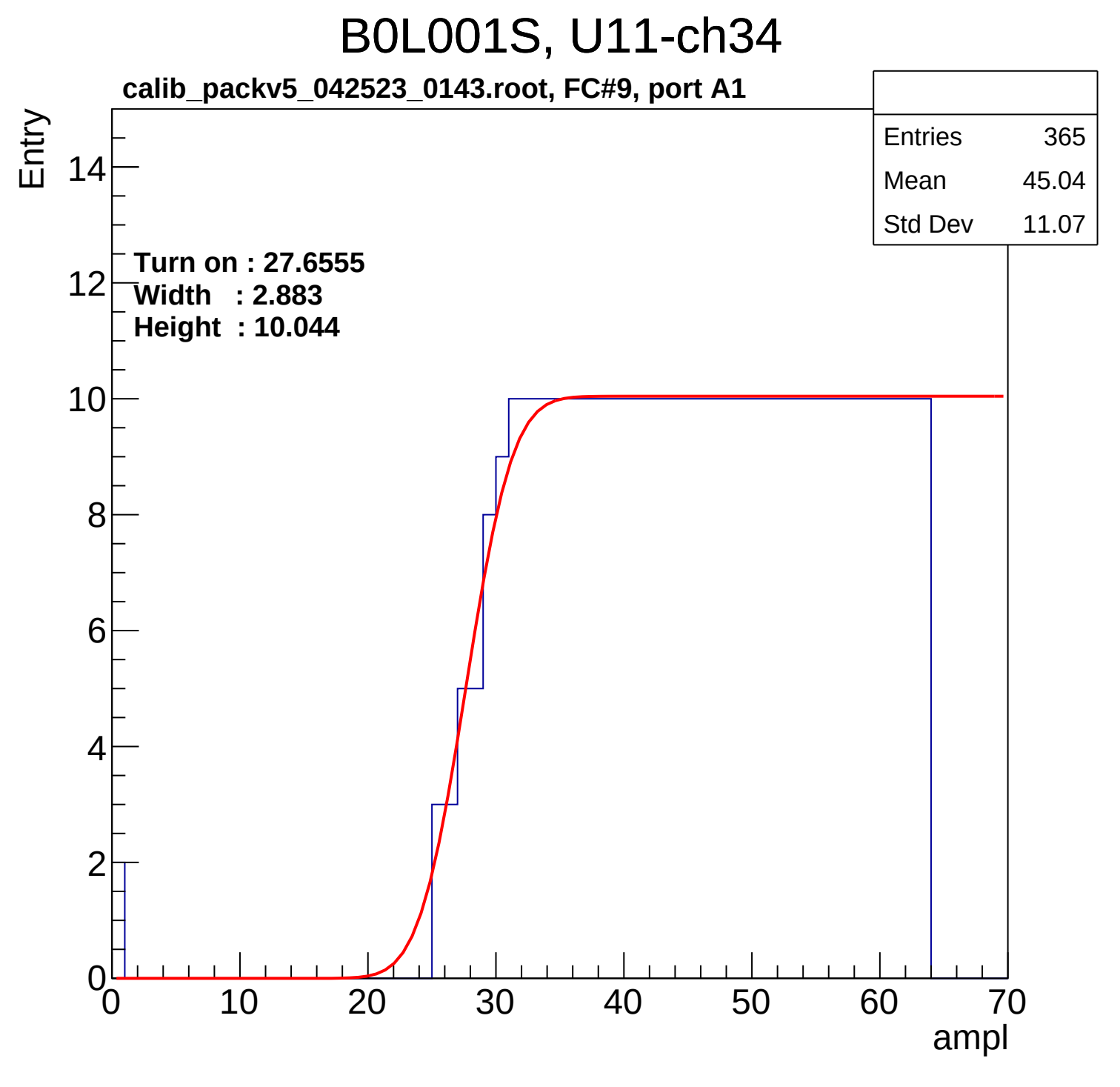
B0L001S, U11-ch34
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 45.04
Std Dev 11.07
Turn on : 27.6555
Width : 2.883
Height : 10.044
Entry
ampl
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2
4
6
8
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12
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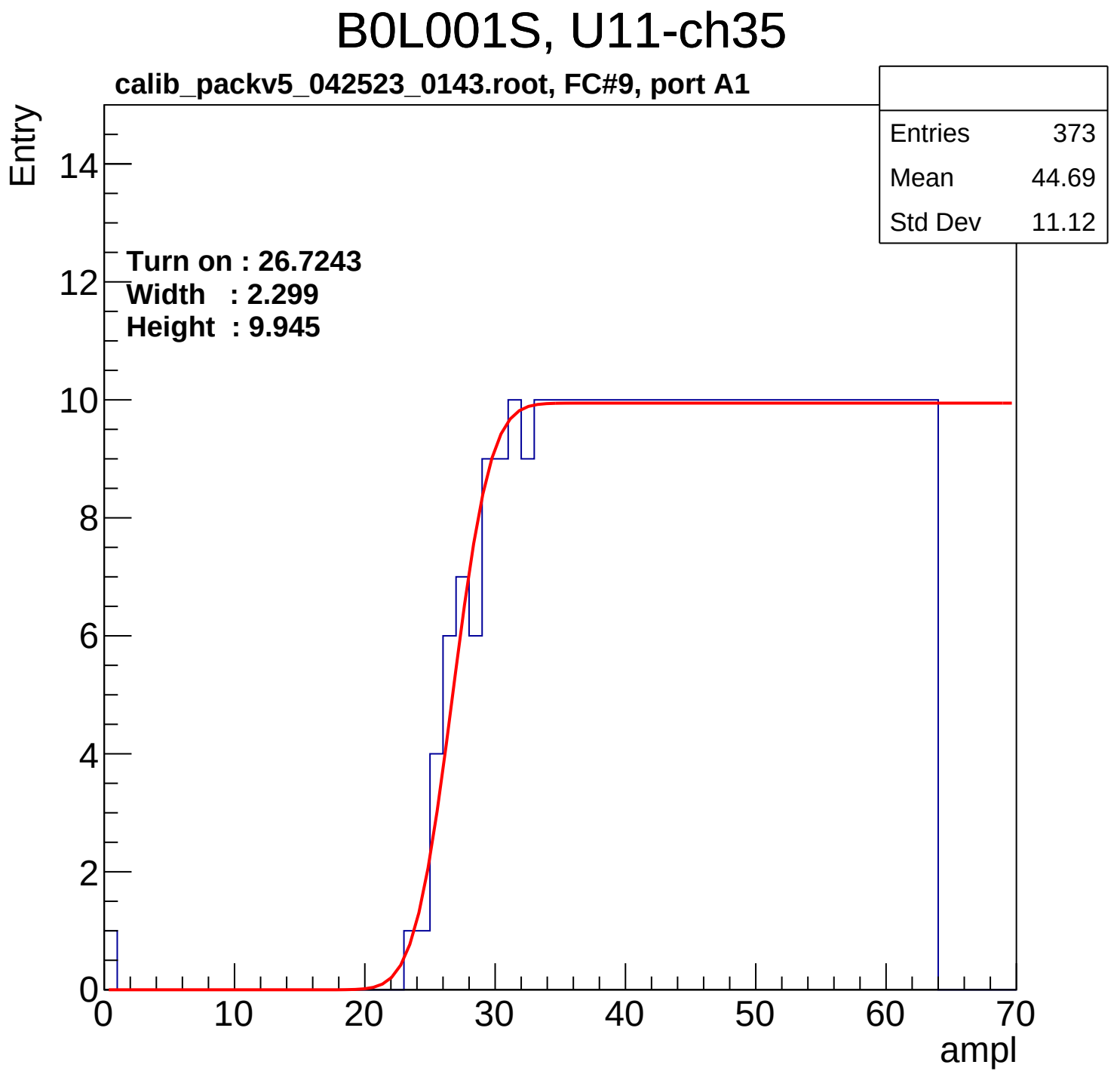
B0L001S, U11-ch35
calib_packv5_042523_0143.root, FC#9, port A1
Entries 373
Mean 44.69
Std Dev 11.12
Turn on : 26.7243
Width : 2.299
Height : 9.945
Entry
ampl
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2
4
6
8
10
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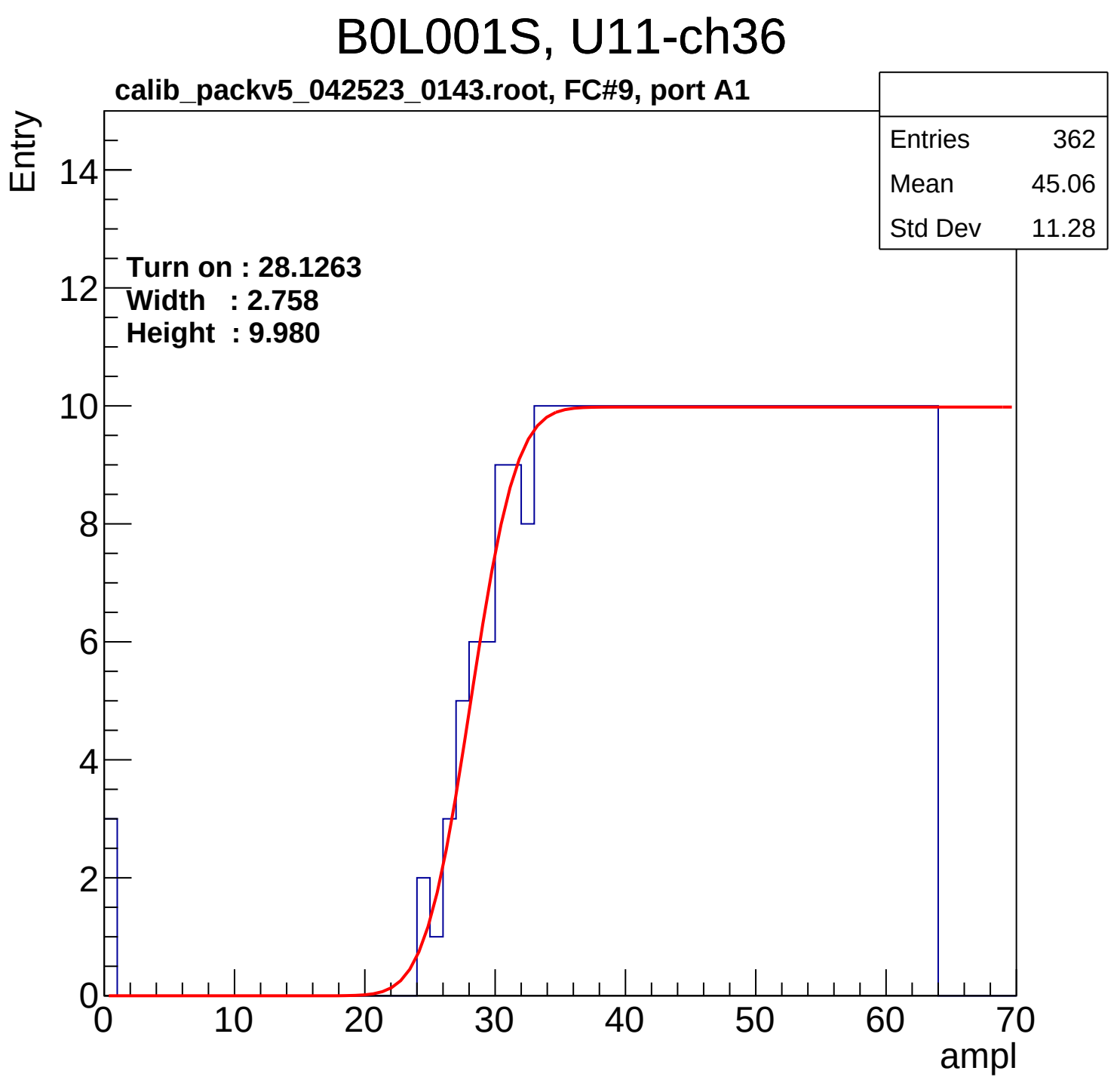
B0L001S, U11-ch36
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 45.06
Std Dev 11.28
Turn on : 28.1263
Width : 2.758
Height : 9.980
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
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60
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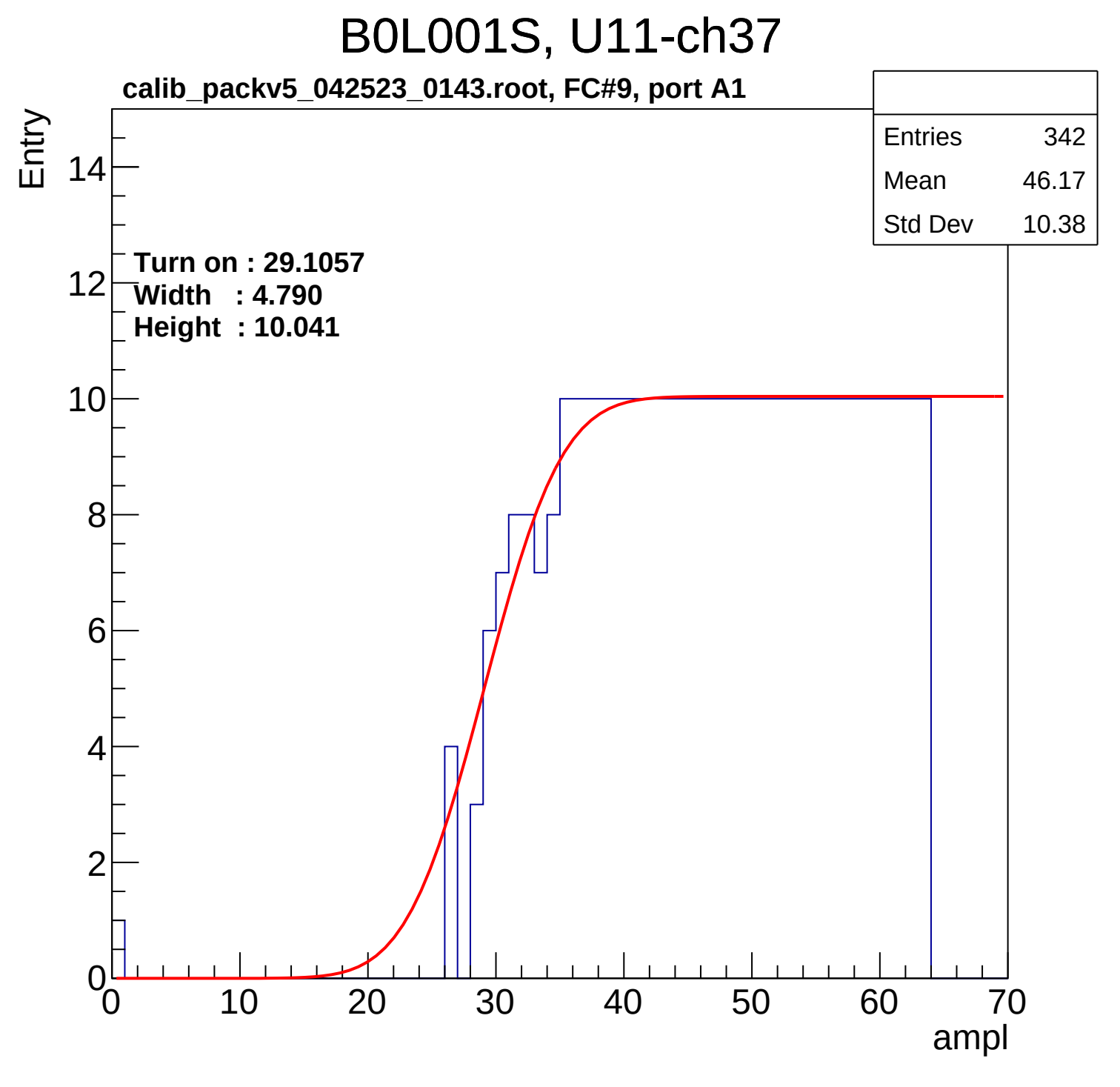
B0L001S, U11-ch37
calib_packv5_042523_0143.root, FC#9, port A1
Entries 342
Mean 46.17
Std Dev 10.38
Turn on : 29.1057
Width : 4.790
Height : 10.041
Entry
ampl
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6
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10
12
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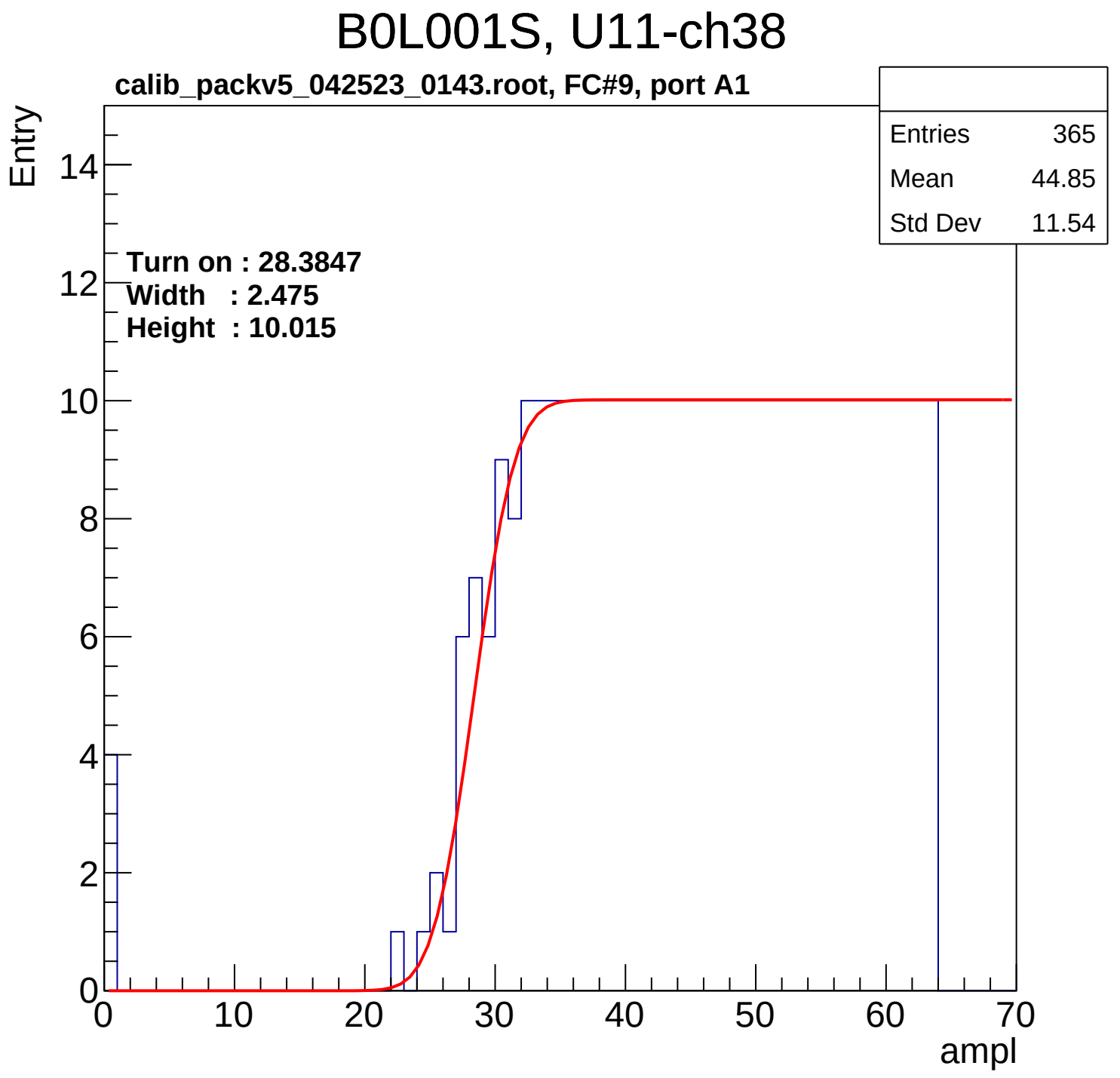
B0L001S, U11-ch38
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 44.85
Std Dev 11.54
Turn on : 28.3847
Width : 2.475
Height : 10.015
Entry
ampl
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6
8
10
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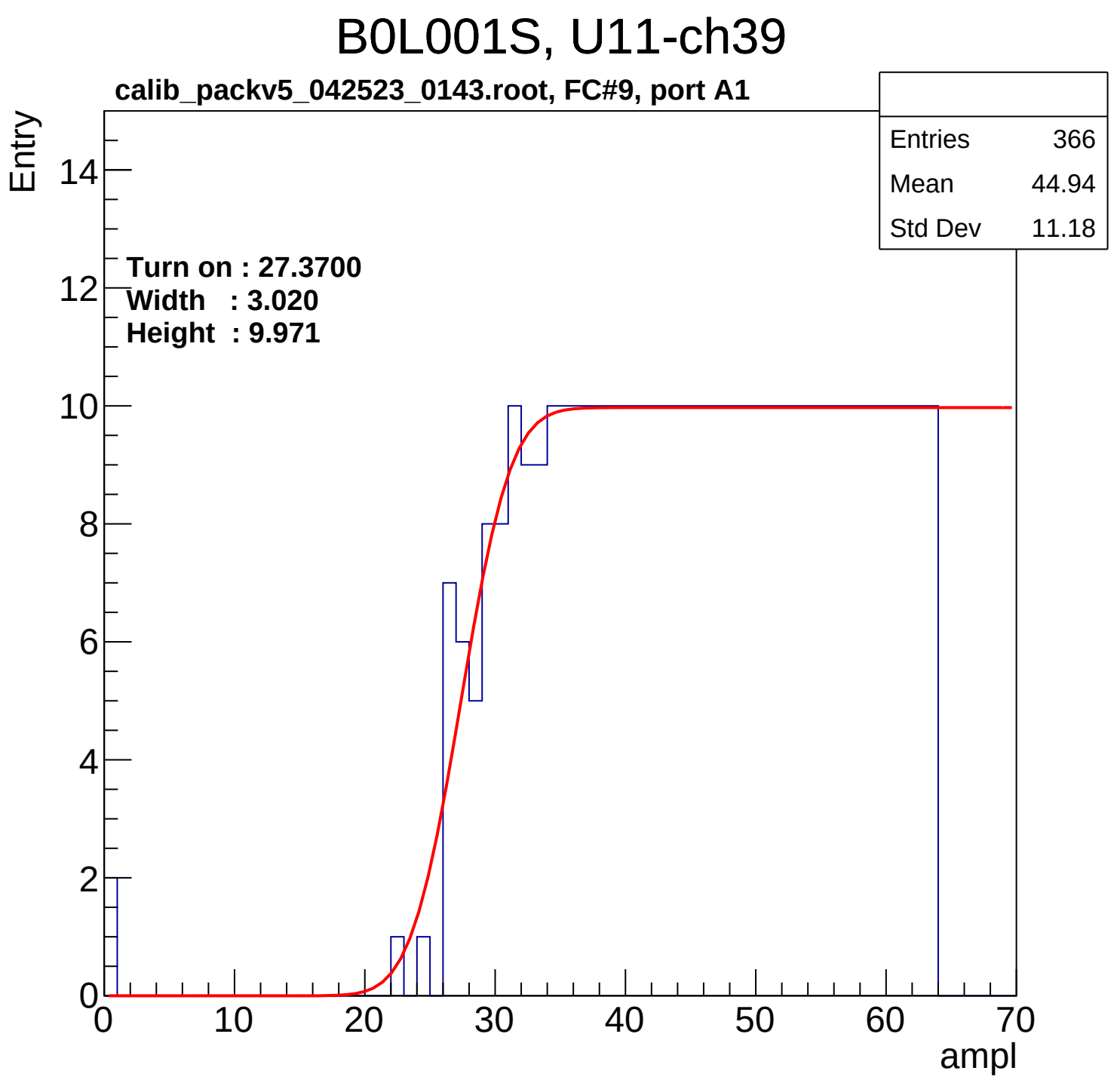
B0L001S, U11-ch39
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.94
Std Dev 11.18
Turn on : 27.3700
Width : 3.020
Height : 9.971
Entry
ampl
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6
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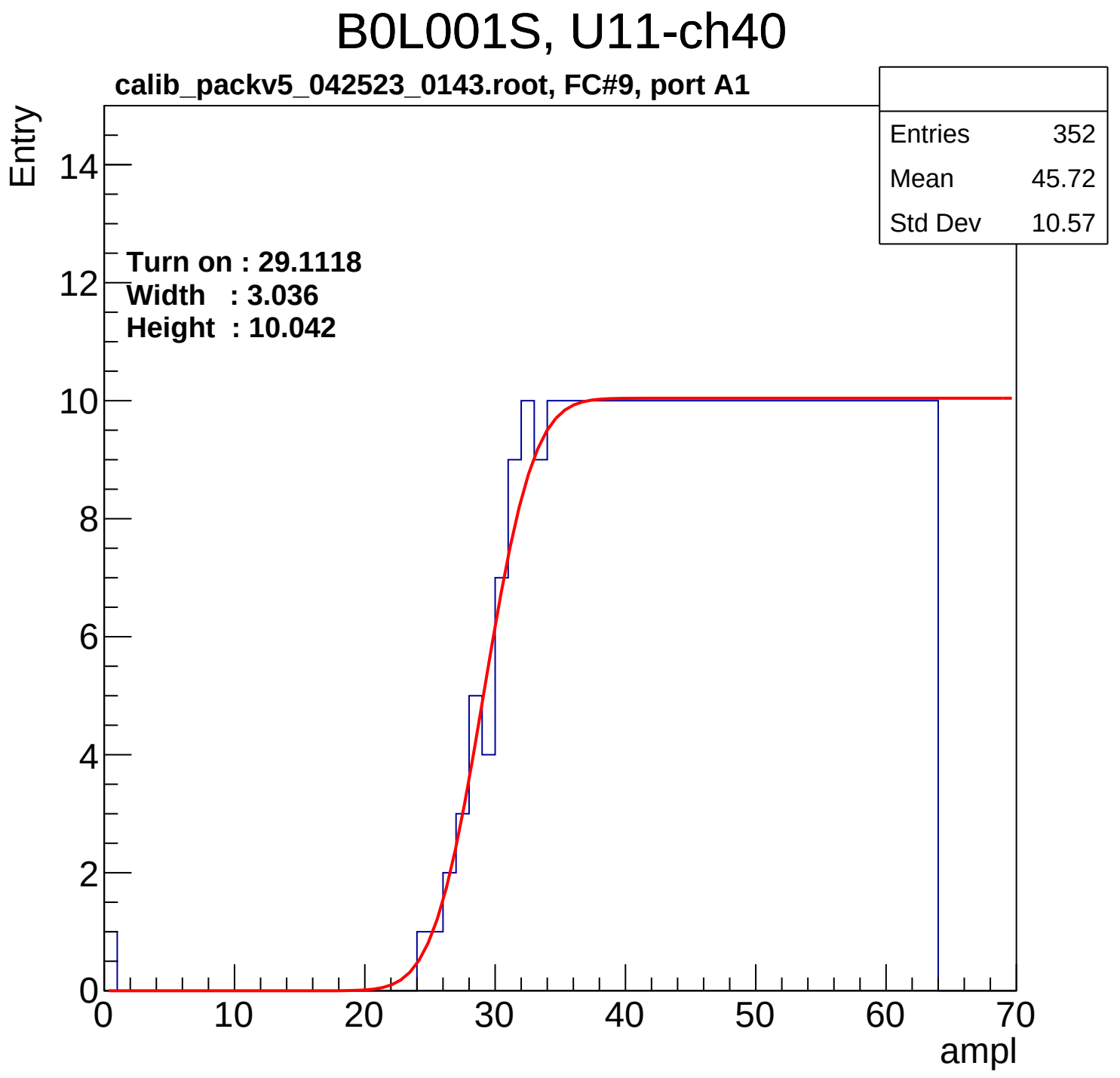
B0L001S, U11-ch40
calib_packv5_042523_0143.root, FC#9, port A1
Entries 352
Mean 45.72
Std Dev 10.57
Turn on : 29.1118
Width : 3.036
Height : 10.042
Entry
ampl
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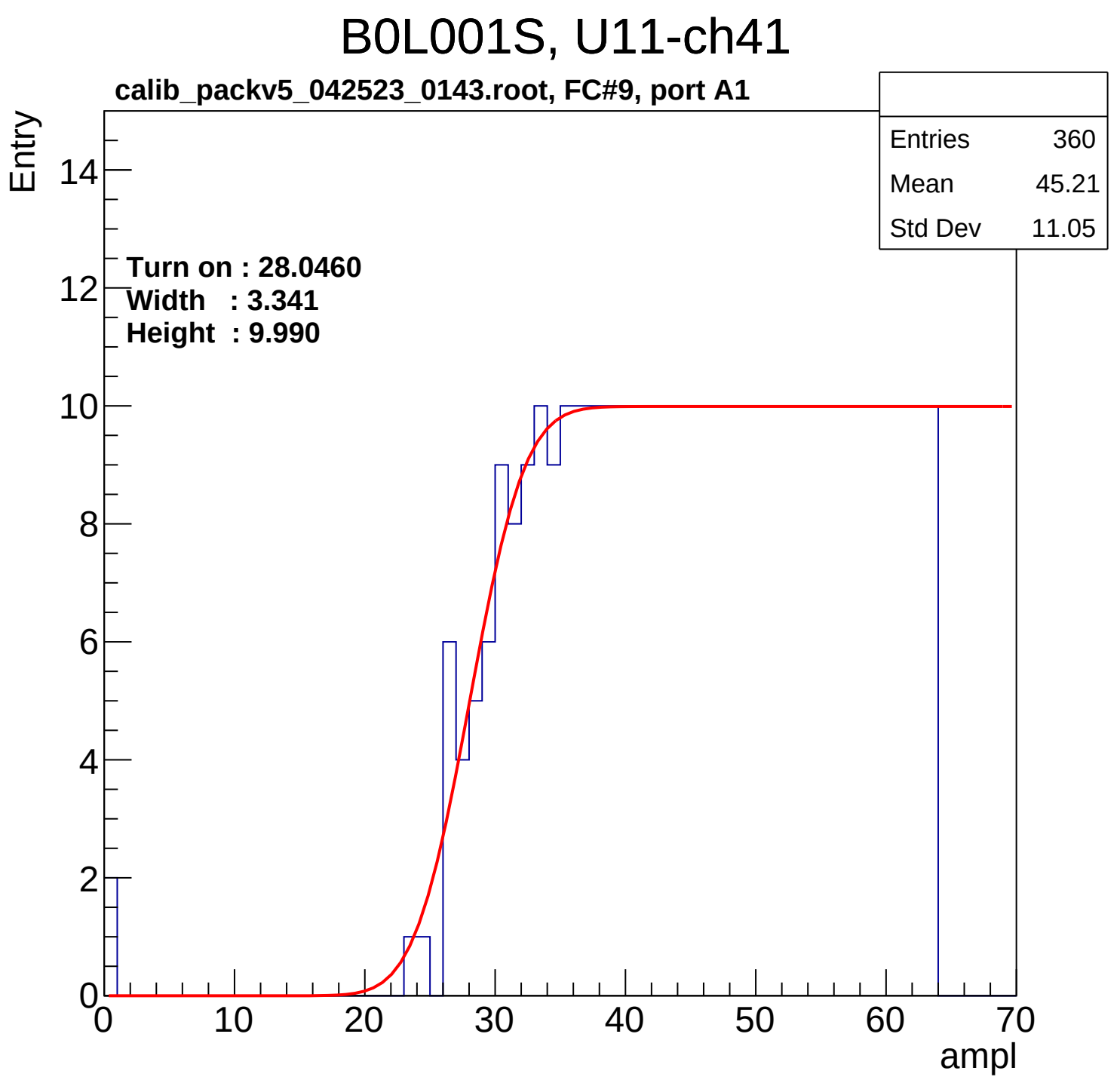
B0L001S, U11-ch41
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 45.21
Std Dev 11.05
Turn on : 28.0460
Width : 3.341
Height : 9.990
Entry
ampl
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6
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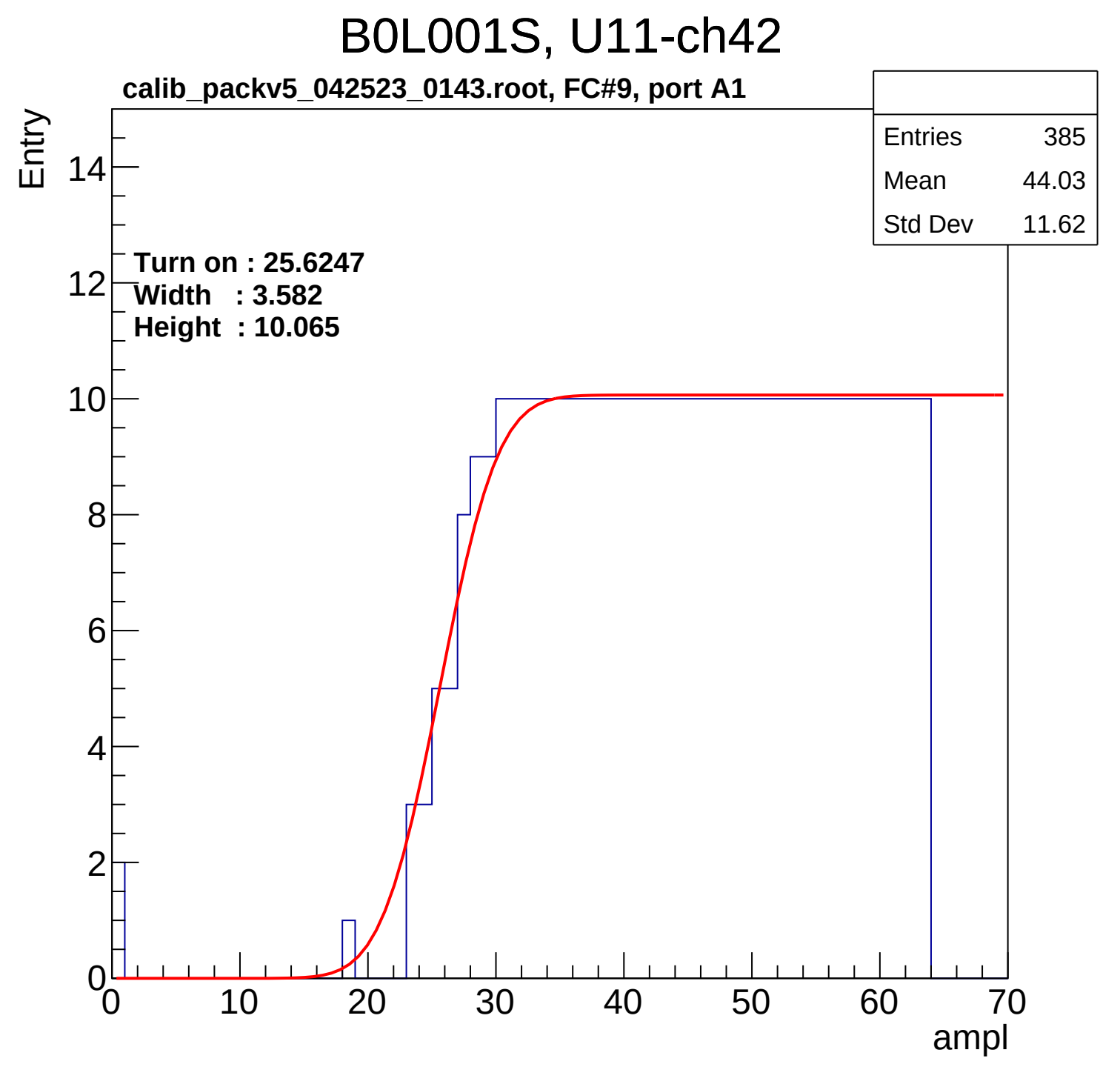
B0L001S, U11-ch42
calib_packv5_042523_0143.root, FC#9, port A1
Entries 385
Mean 44.03
Std Dev 11.62
Turn on : 25.6247
Width : 3.582
Height : 10.065
Entry
ampl
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6
8
10
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0
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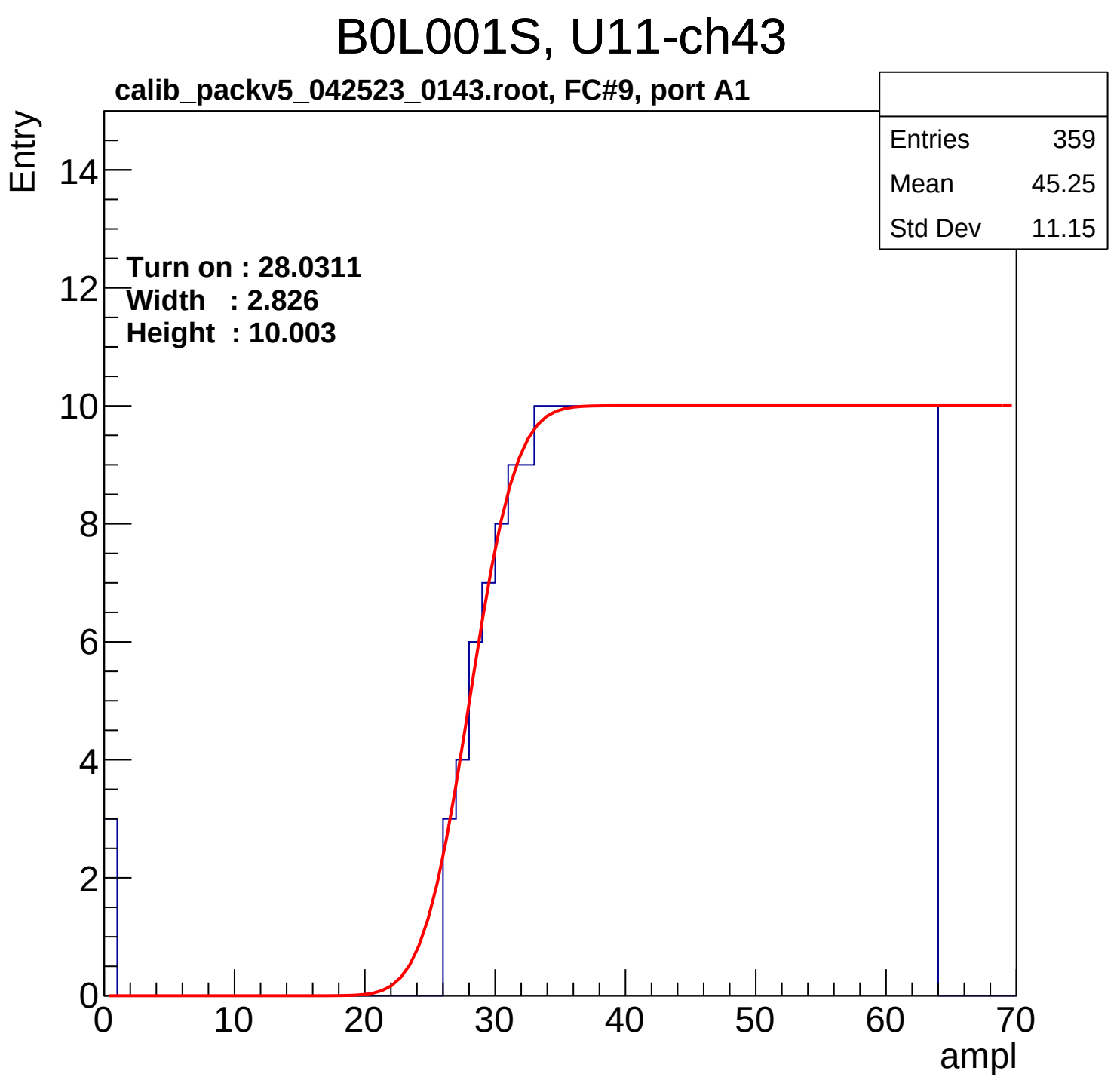
B0L001S, U11-ch43
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 45.25
Std Dev 11.15
Turn on : 28.0311
Width : 2.826
Height : 10.003
Entry
ampl
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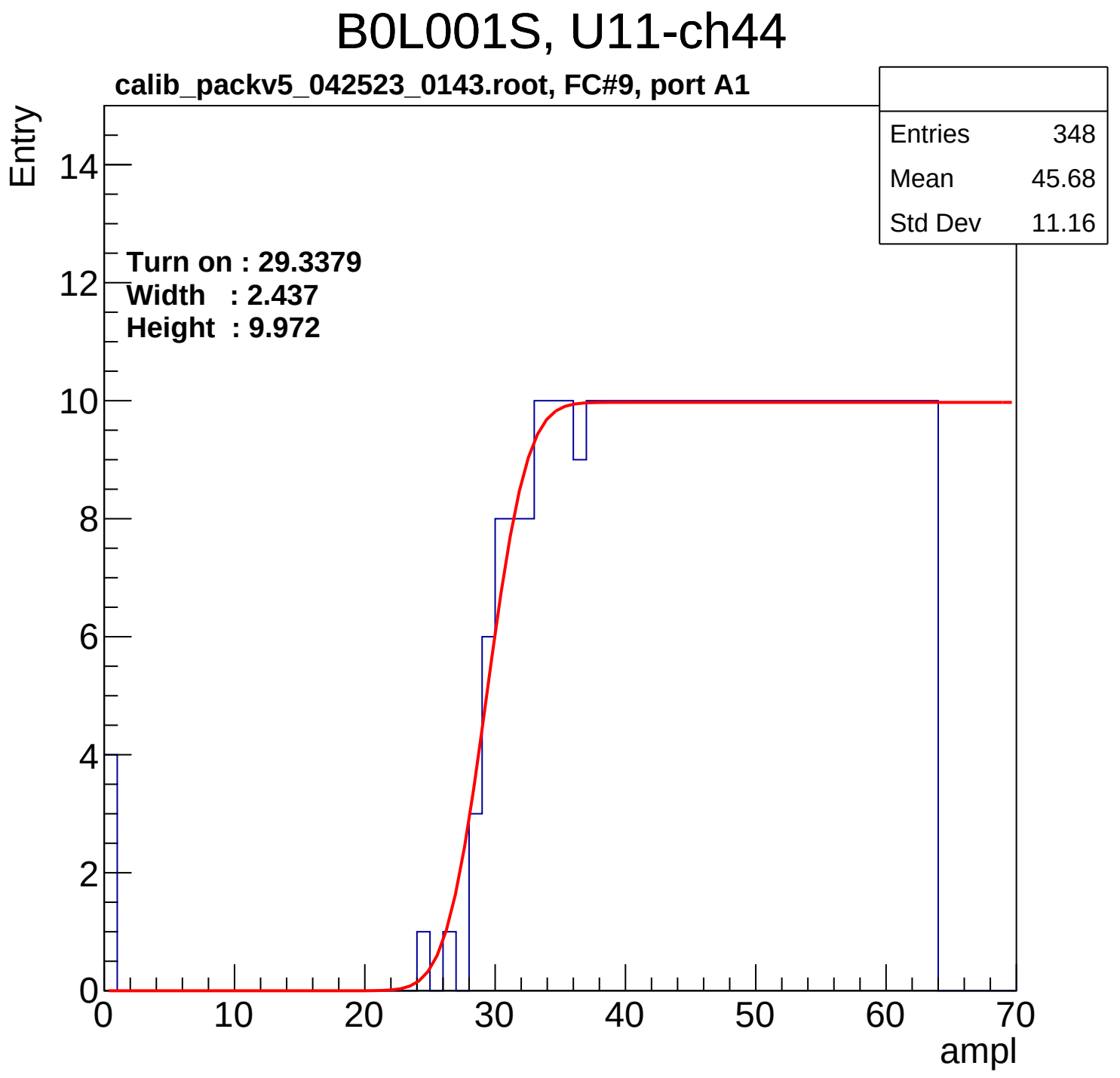
B0L001S, U11-ch44
calib_packv5_042523_0143.root, FC#9, port A1
Entries 348
Mean 45.68
Std Dev 11.16
Turn on : 29.3379
Width : 2.437
Height : 9.972
Entry
ampl
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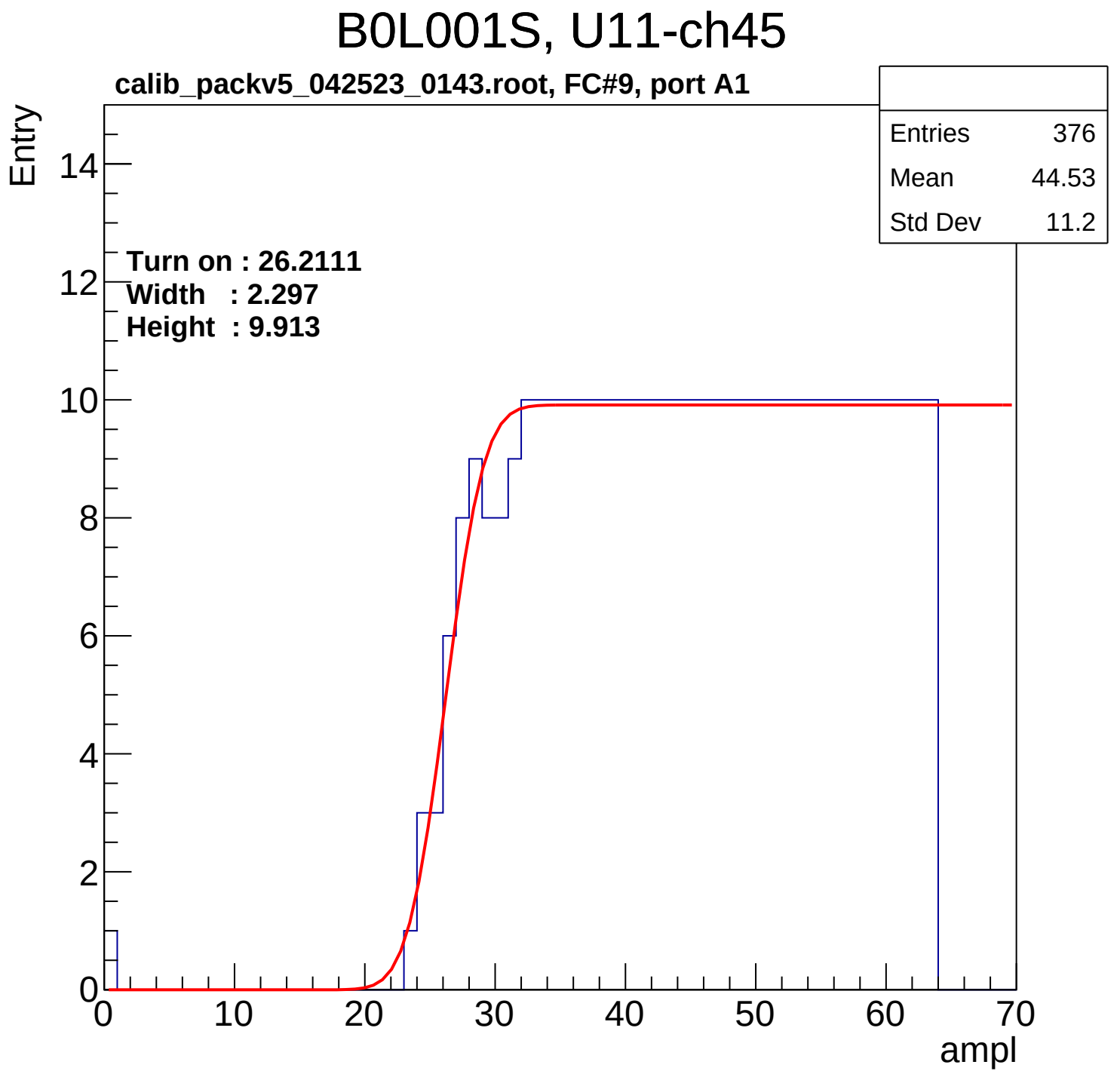
B0L001S, U11-ch45
calib_packv5_042523_0143.root, FC#9, port A1
Entries 376
Mean 44.53
Std Dev 11.2
Turn on : 26.2111
Width : 2.297
Height : 9.913
Entry
ampl
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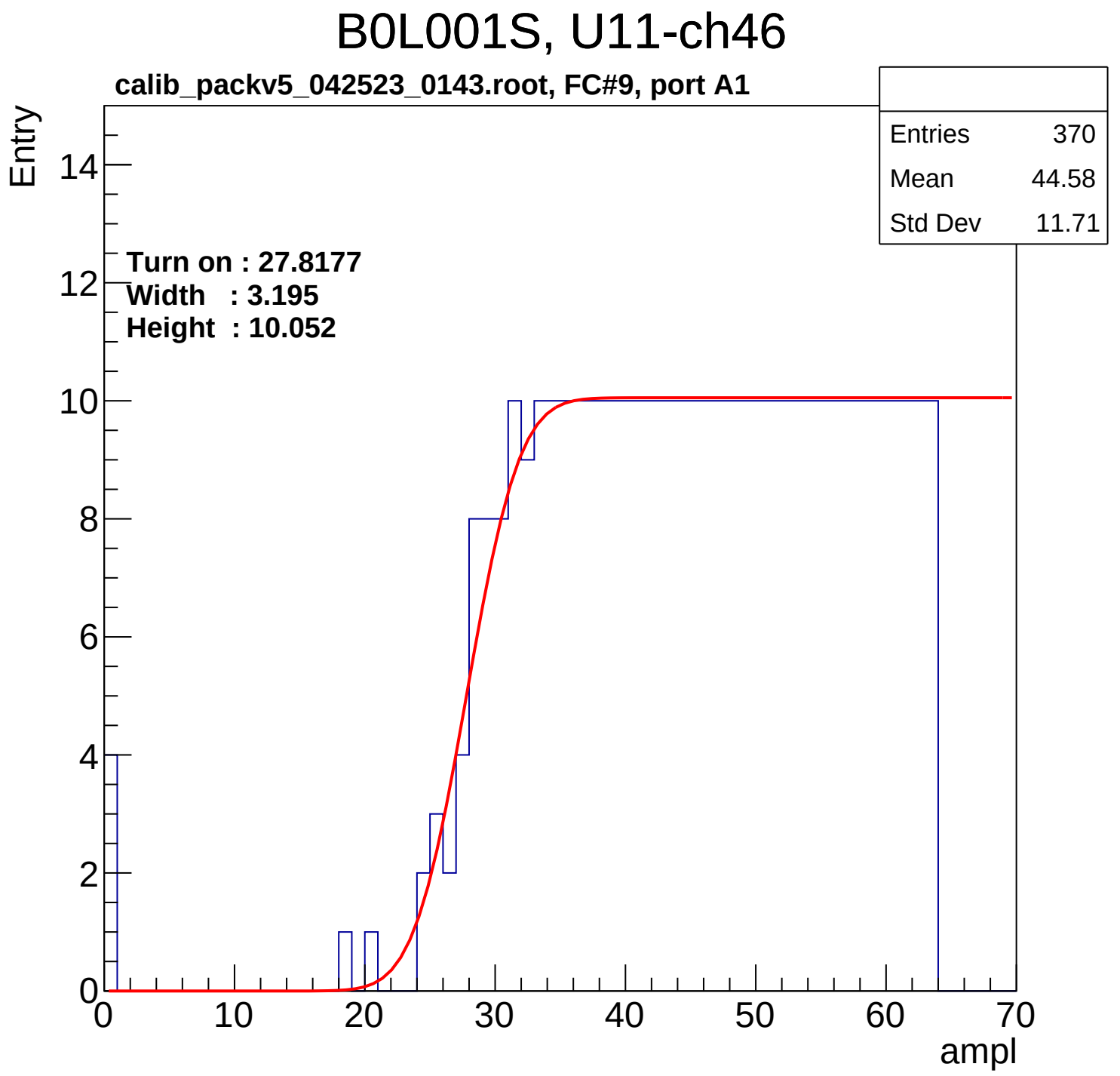
B0L001S, U11-ch46
calib_packv5_042523_0143.root, FC#9, port A1
Entries 370
Mean 44.58
Std Dev 11.71
Turn on : 27.8177
Width : 3.195
Height : 10.052
Entry
ampl
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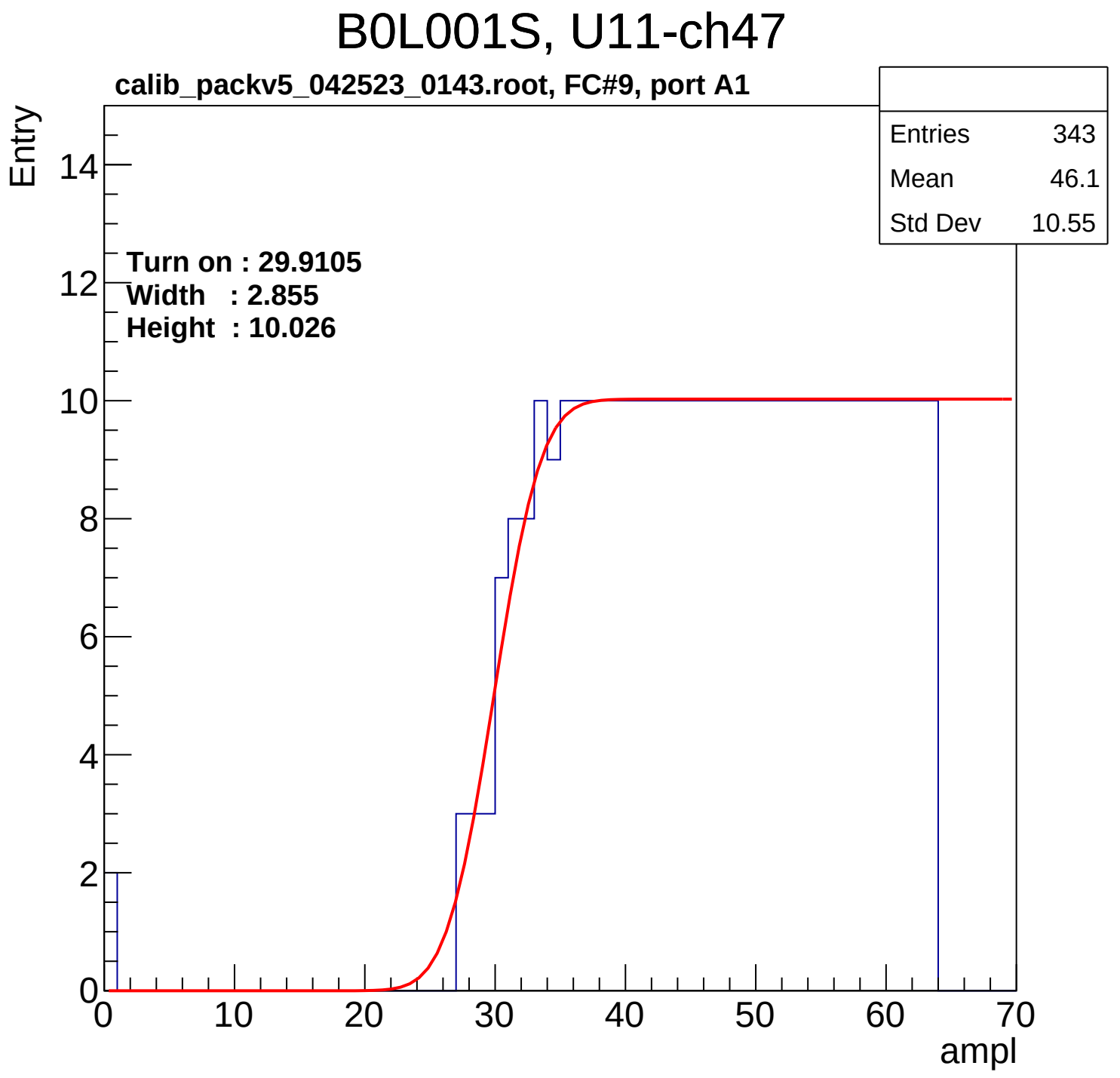
B0L001S, U11-ch47
calib_packv5_042523_0143.root, FC#9, port A1
Entries 343
Mean 46.1
Std Dev 10.55
Turn on : 29.9105
Width : 2.855
Height : 10.026
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ampl
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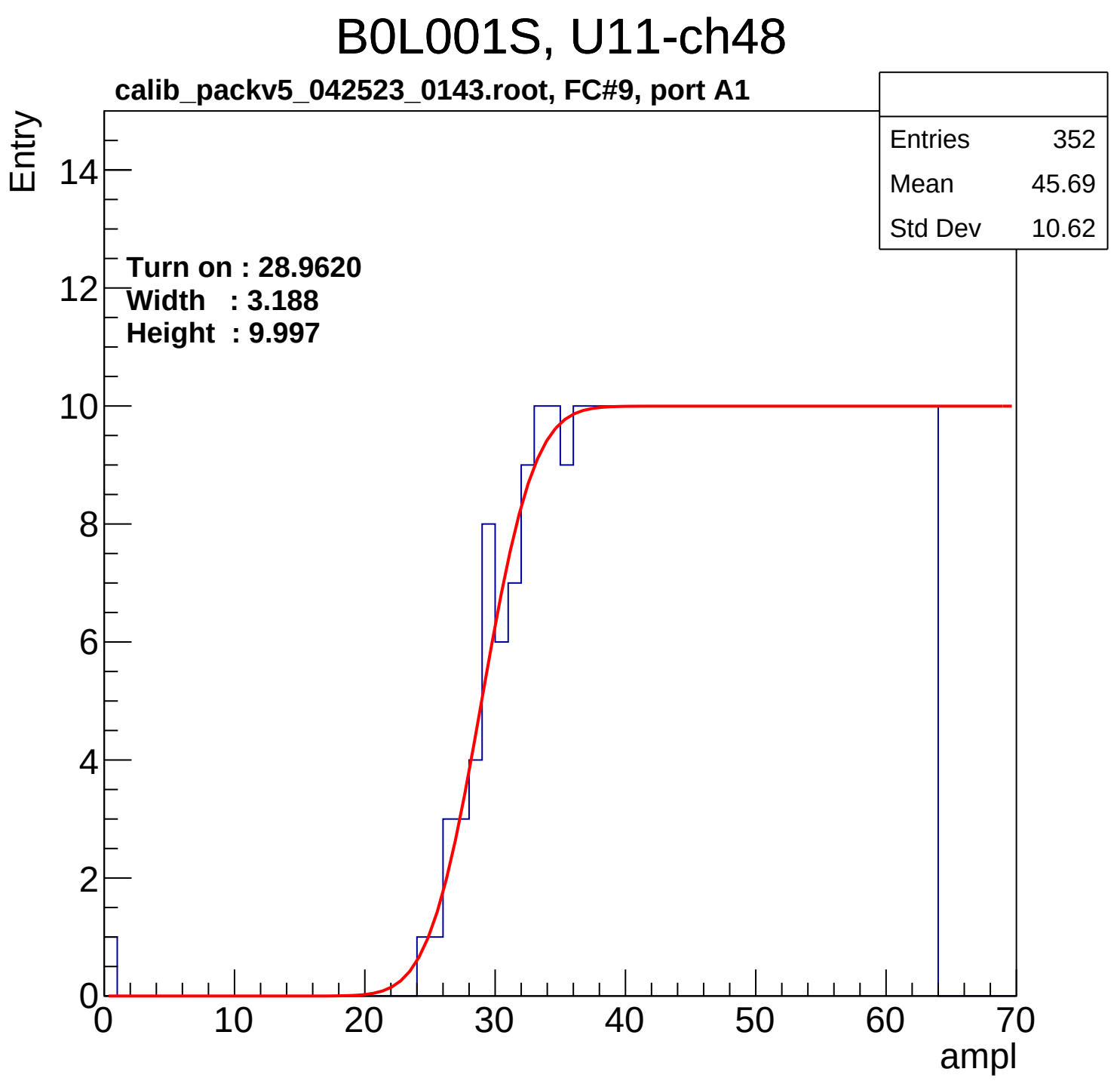
B0L001S, U11-ch48
calib_packv5_042523_0143.root, FC#9, port A1
Entries 352
Mean 45.69
Std Dev 10.62
Turn on : 28.9620
Width : 3.188
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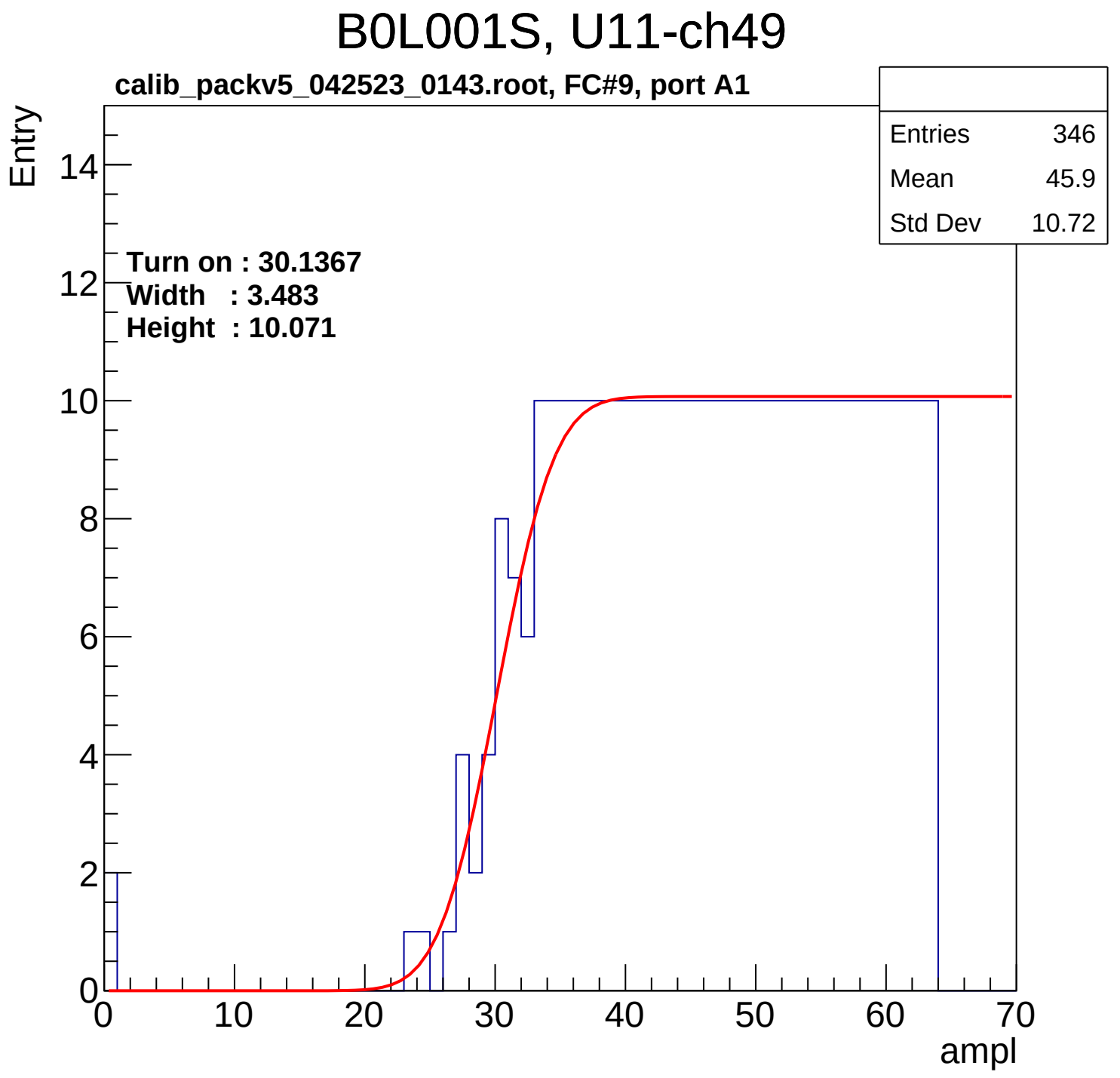
B0L001S, U11-ch49
calib_packv5_042523_0143.root, FC#9, port A1
Entries 346
Mean 45.9
Std Dev 10.72
Turn on : 30.1367
Width : 3.483
Height : 10.071
Entry
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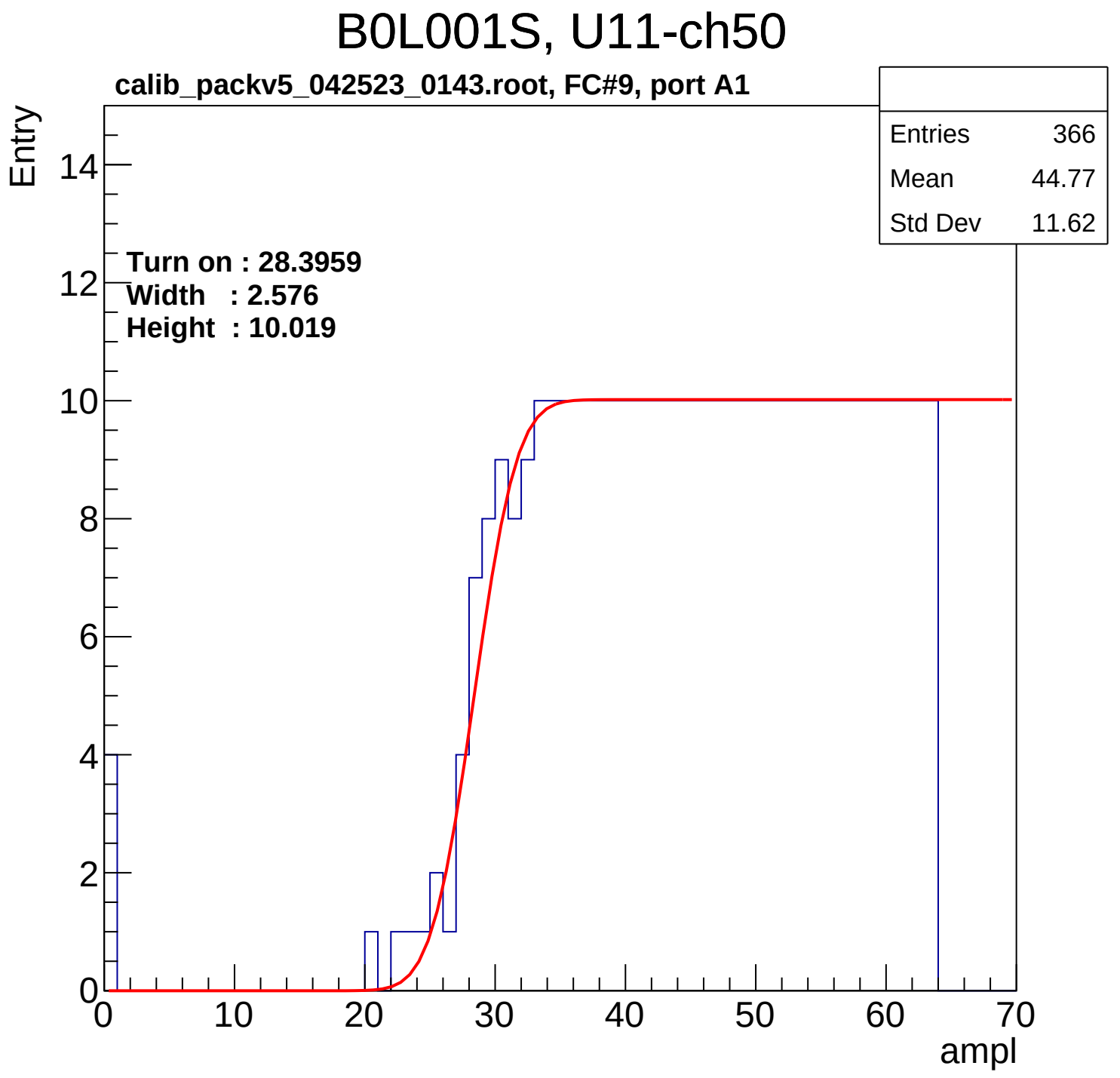
B0L001S, U11-ch50
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.77
Std Dev 11.62
Turn on : 28.3959
Width : 2.576
Height : 10.019
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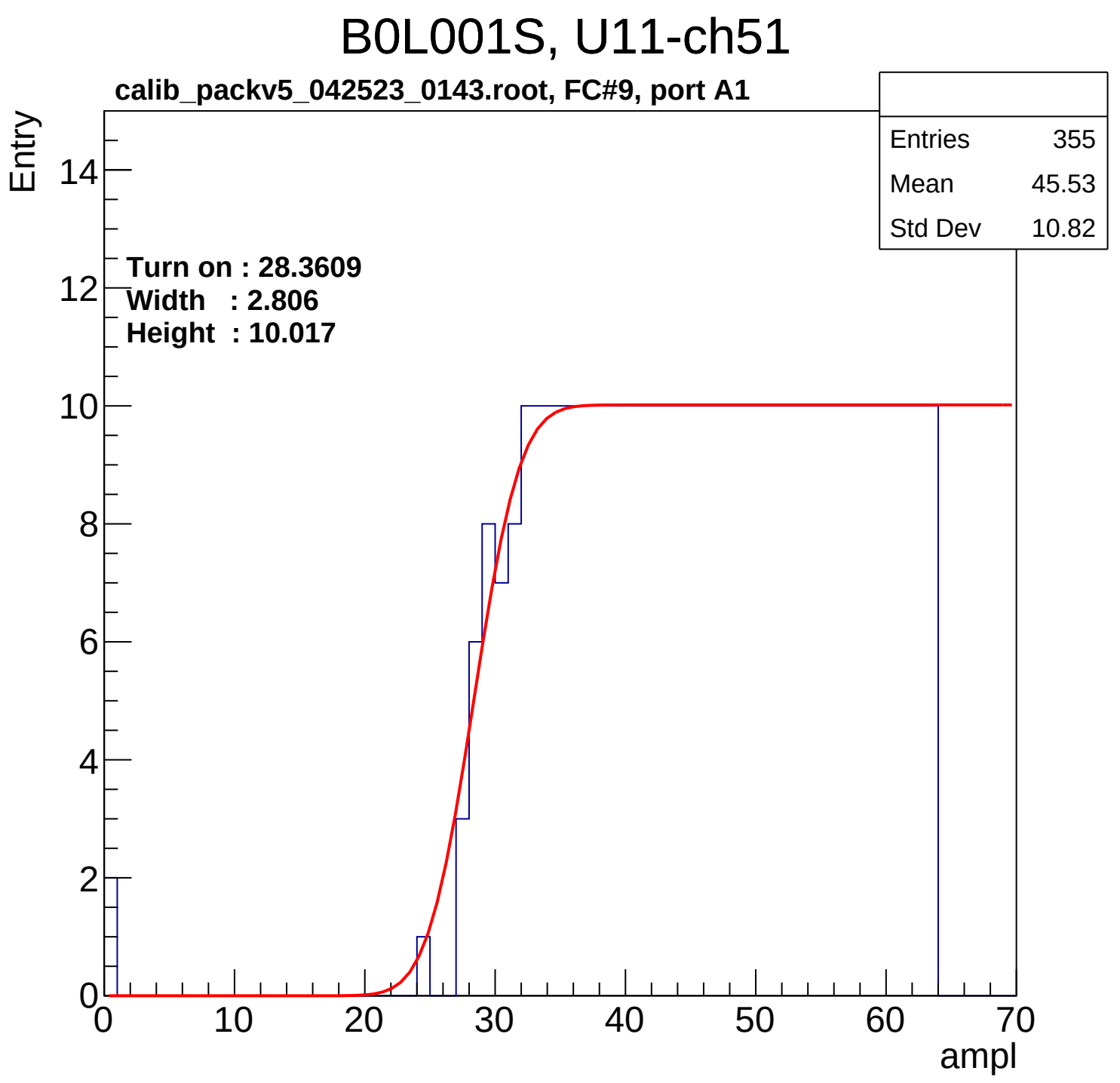
B0L001S, U11-ch51
calib_packv5_042523_0143.root, FC#9, port A1
Entries 355
Mean 45.53
Std Dev 10.82
Turn on : 28.3609
Width : 2.806
Height : 10.017
Entry
ampl
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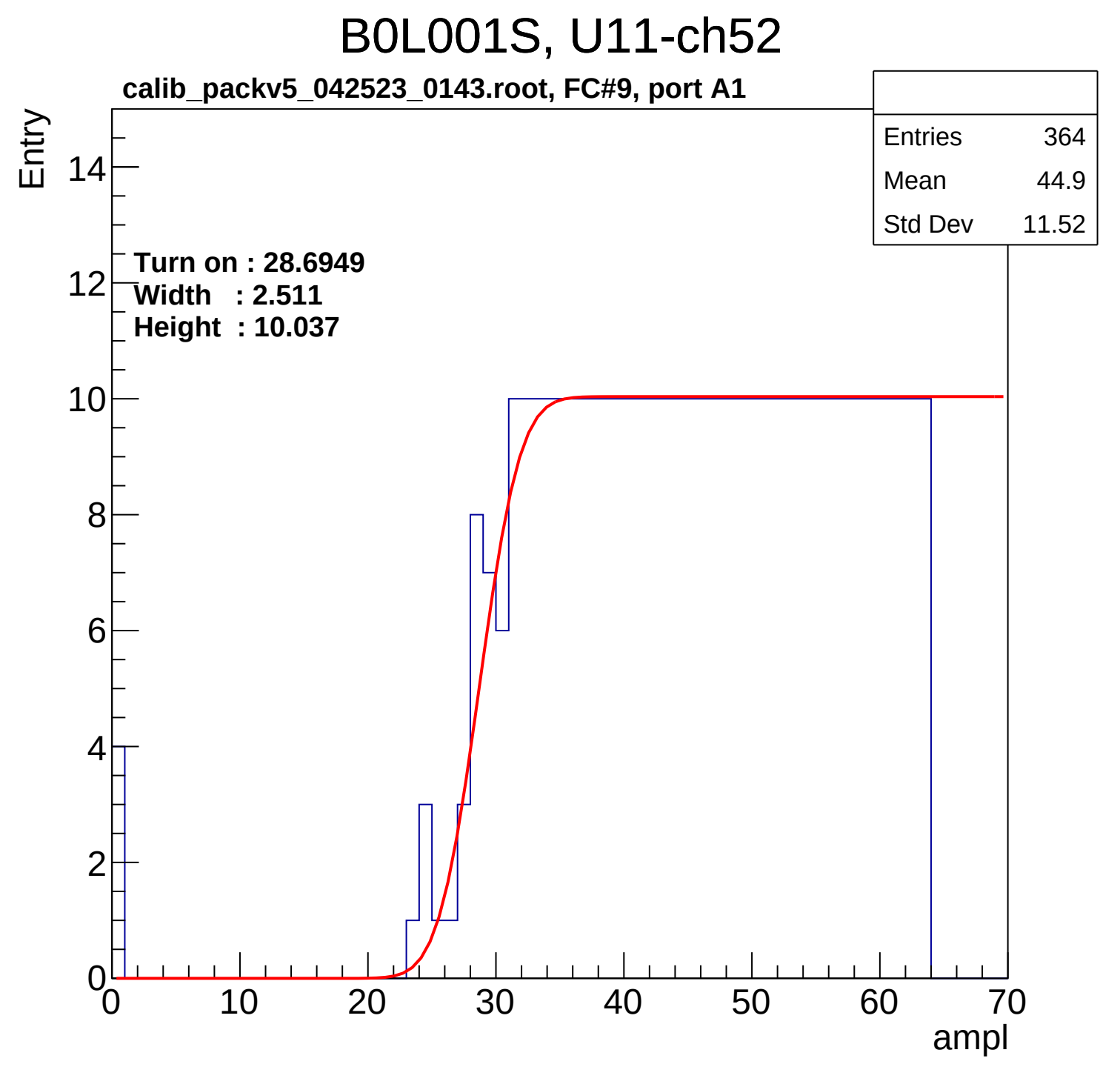
B0L001S, U11-ch52
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 44.9
Std Dev 11.52
Turn on : 28.6949
Width : 2.511
Height : 10.037
Entry
ampl
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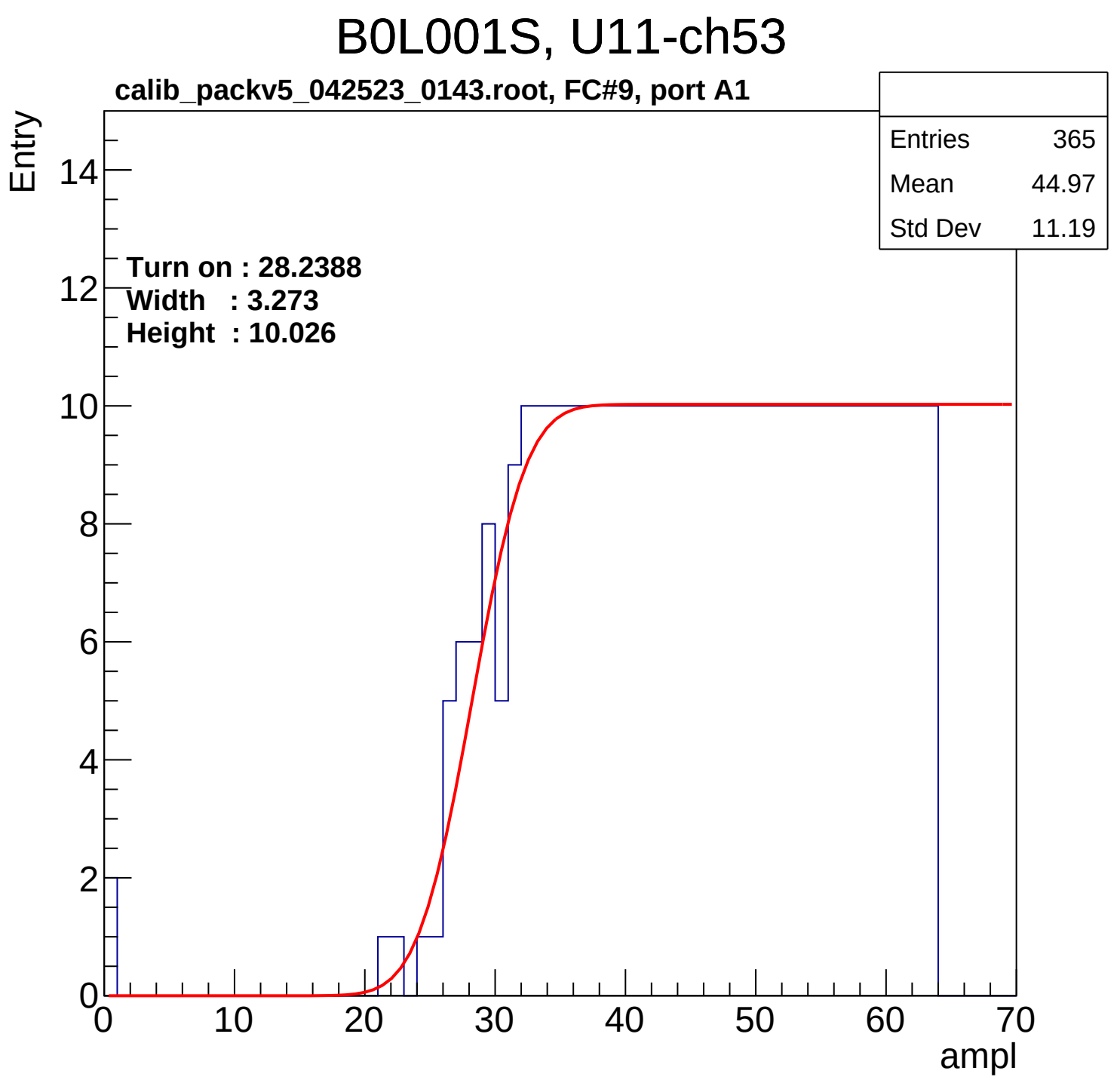
B0L001S, U11-ch53
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 44.97
Std Dev 11.19
Turn on : 28.2388
Width : 3.273
Height : 10.026
Entry
ampl
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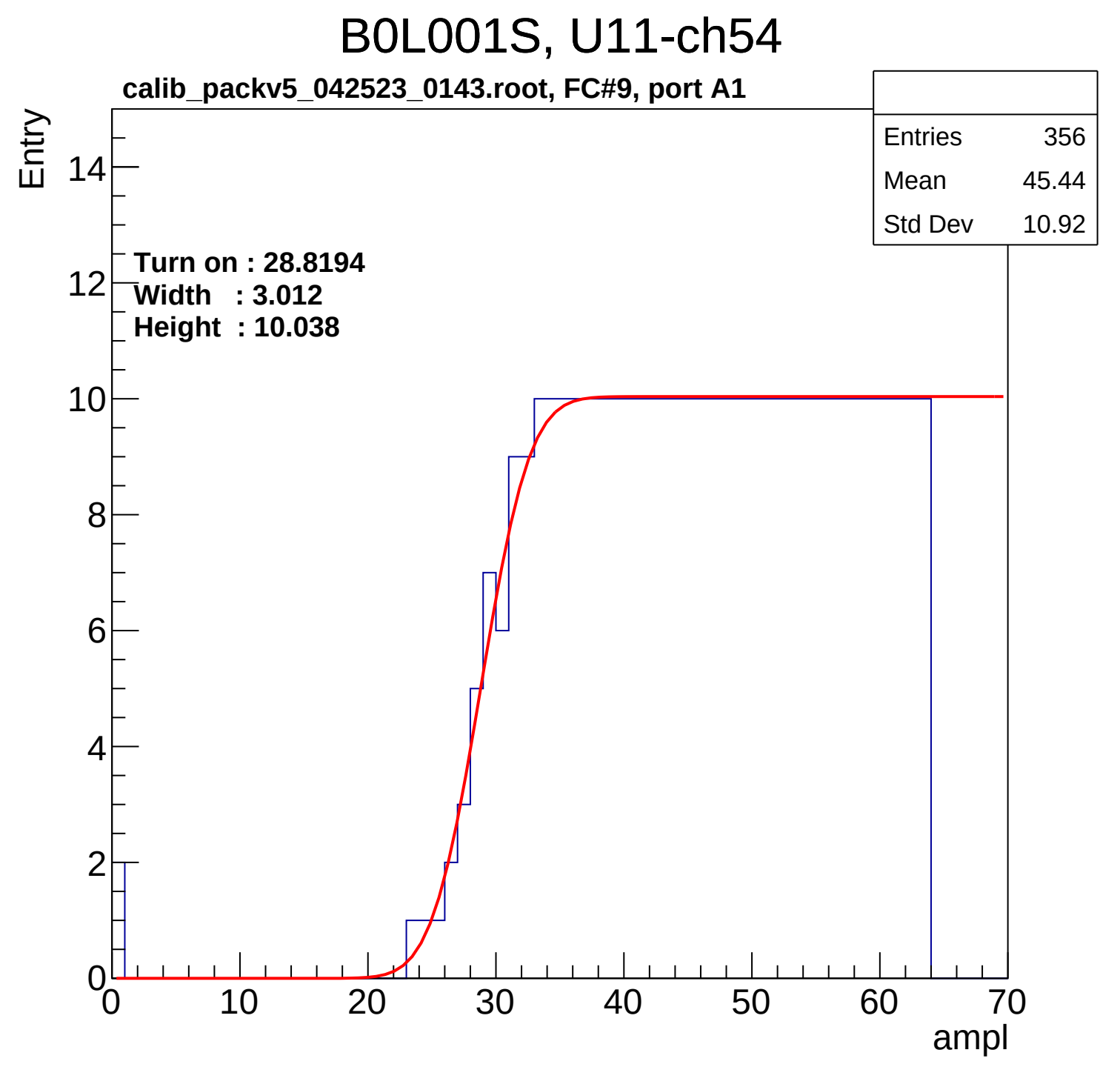
B0L001S, U11-ch54
calib_packv5_042523_0143.root, FC#9, port A1
Entries 356
Mean 45.44
Std Dev 10.92
Turn on : 28.8194
Width : 3.012
Height : 10.038
Entry
ampl
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8
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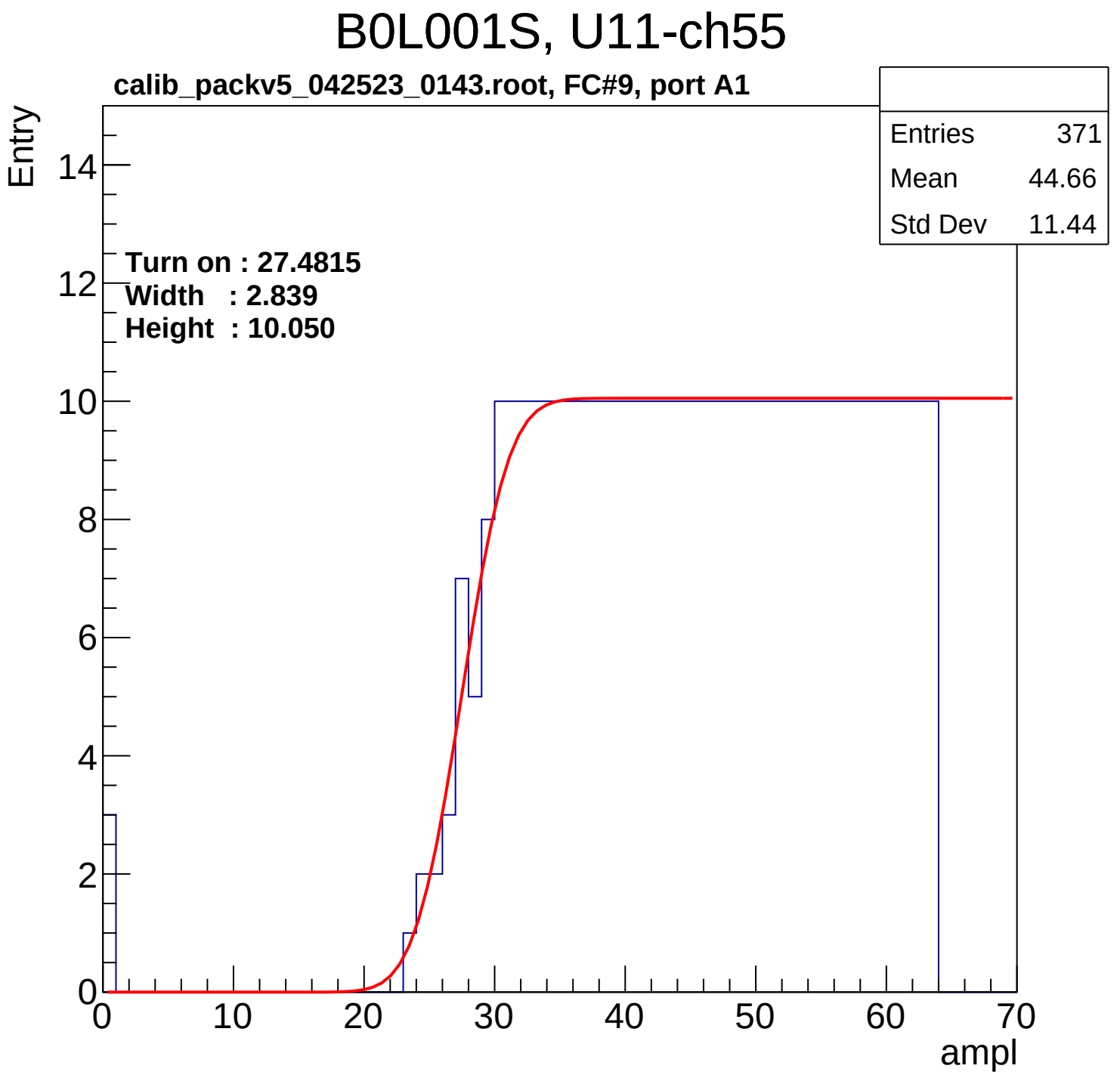
B0L001S, U11-ch55
calib_packv5_042523_0143.root, FC#9, port A1
Entries 371
Mean 44.66
Std Dev 11.44
Turn on : 27.4815
Width : 2.839
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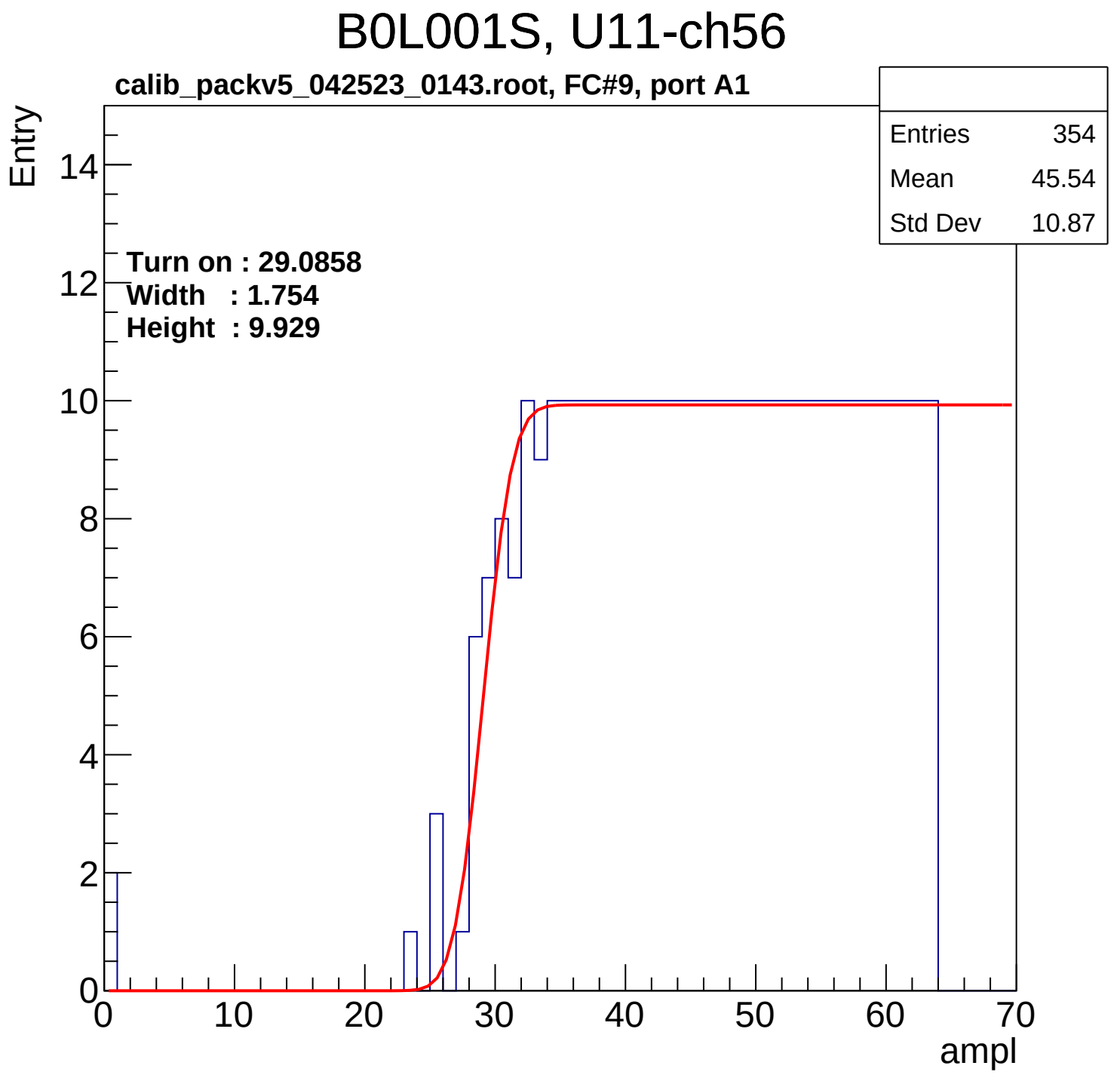
B0L001S, U11-ch56
calib_packv5_042523_0143.root, FC#9, port A1
Entries 354
Mean 45.54
Std Dev 10.87
Turn on : 29.0858
Width : 1.754
Height : 9.929
Entry
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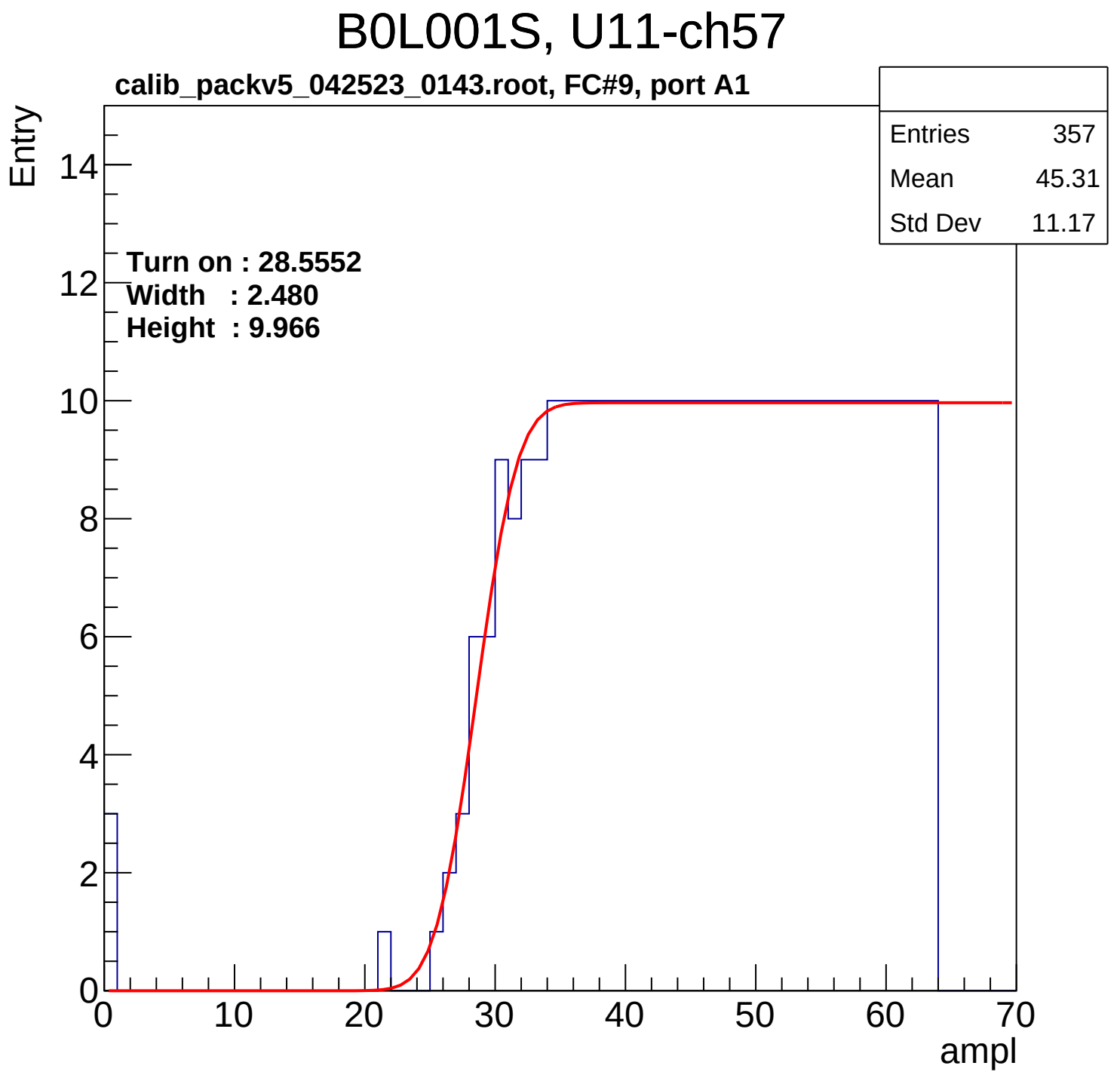
B0L001S, U11-ch57
calib_packv5_042523_0143.root, FC#9, port A1
Entries 357
Mean 45.31
Std Dev 11.17
Turn on : 28.5552
Width : 2.480
Height : 9.966
Entry
ampl
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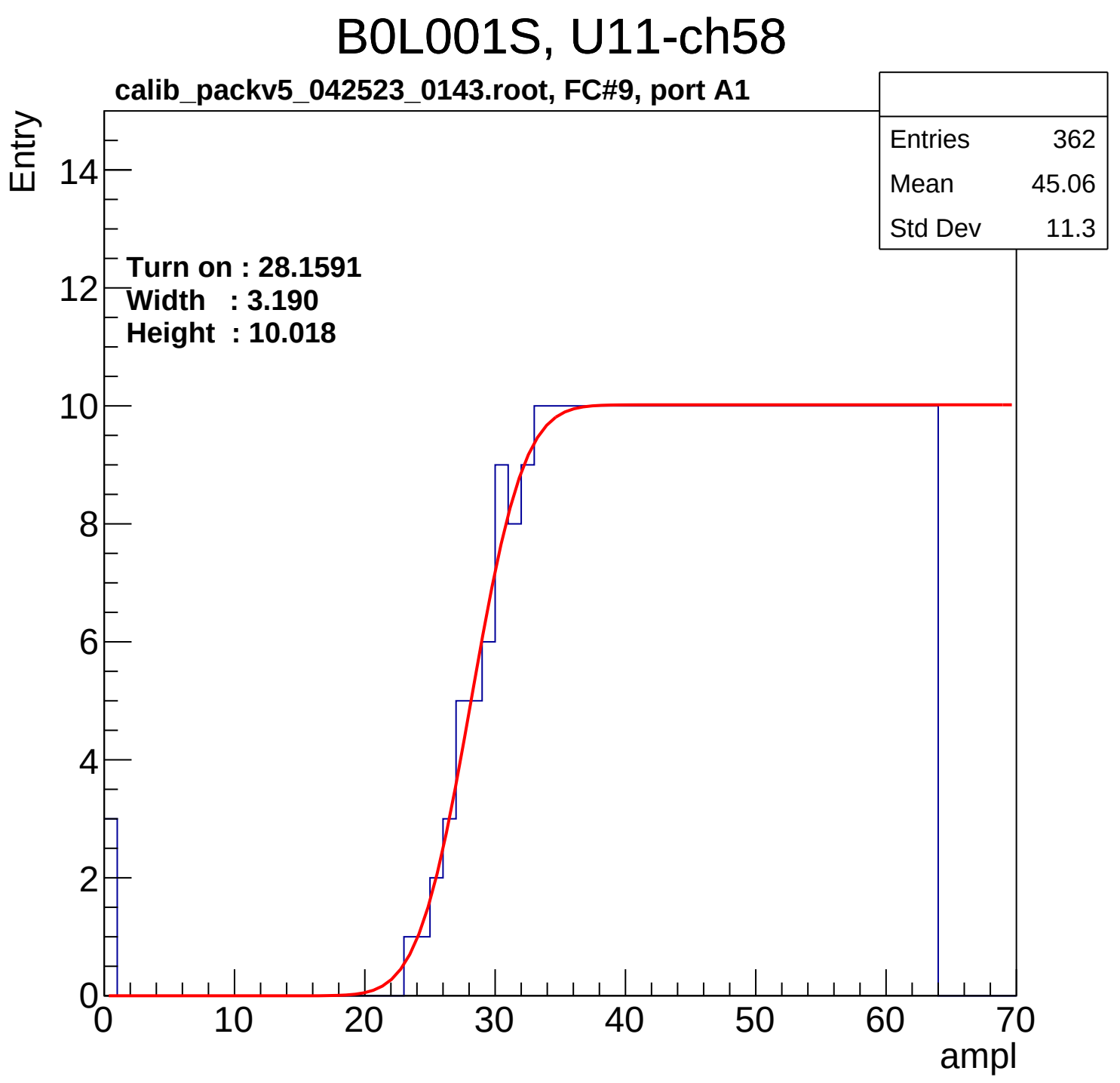
B0L001S, U11-ch58
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 45.06
Std Dev 11.3
Turn on : 28.1591
Width : 3.190
Height : 10.018
Entry
ampl
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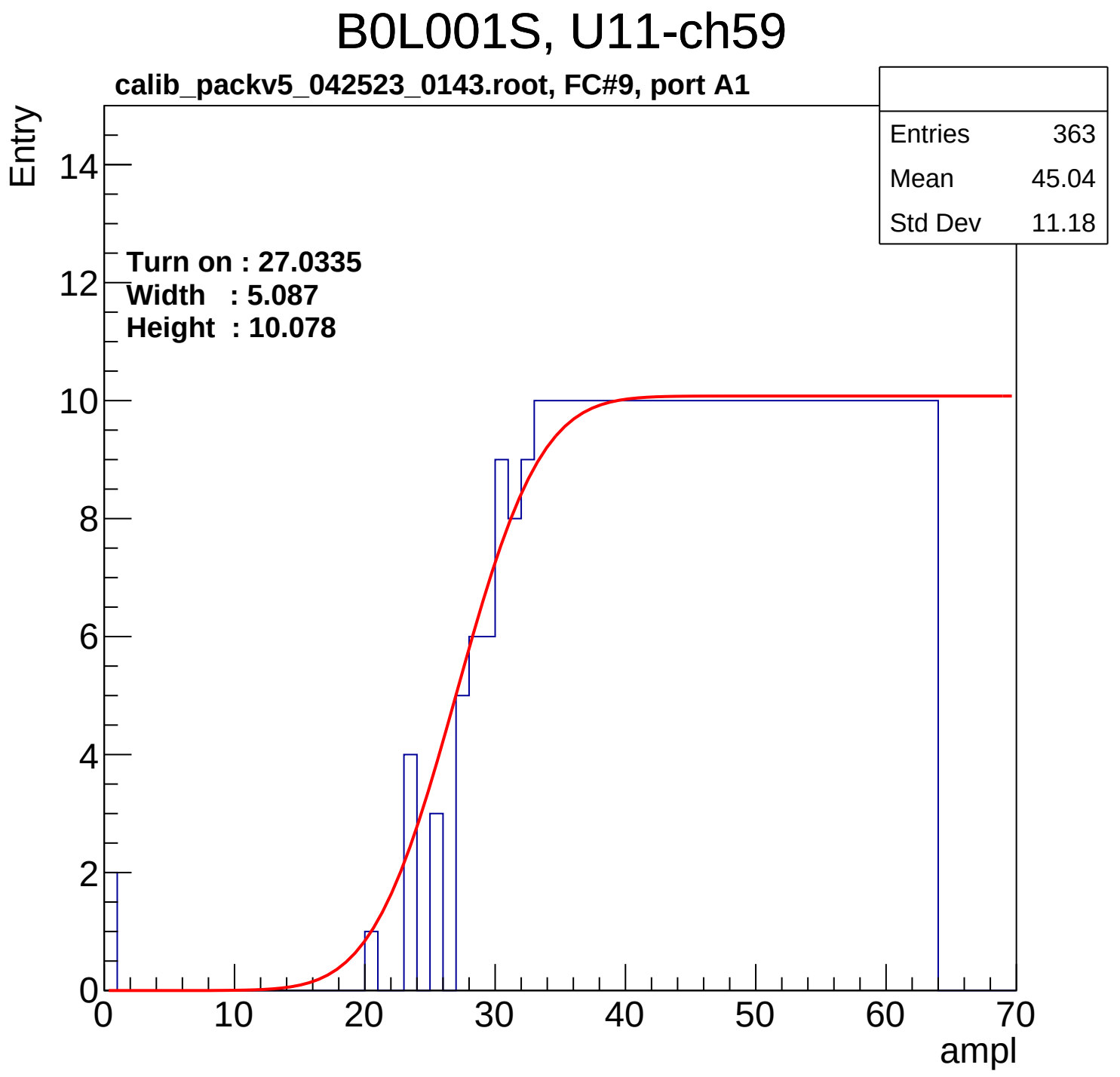
B0L001S, U11-ch59
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 45.04
Std Dev 11.18
Turn on : 27.0335
Width : 5.087
Height : 10.078
Entry
ampl
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4
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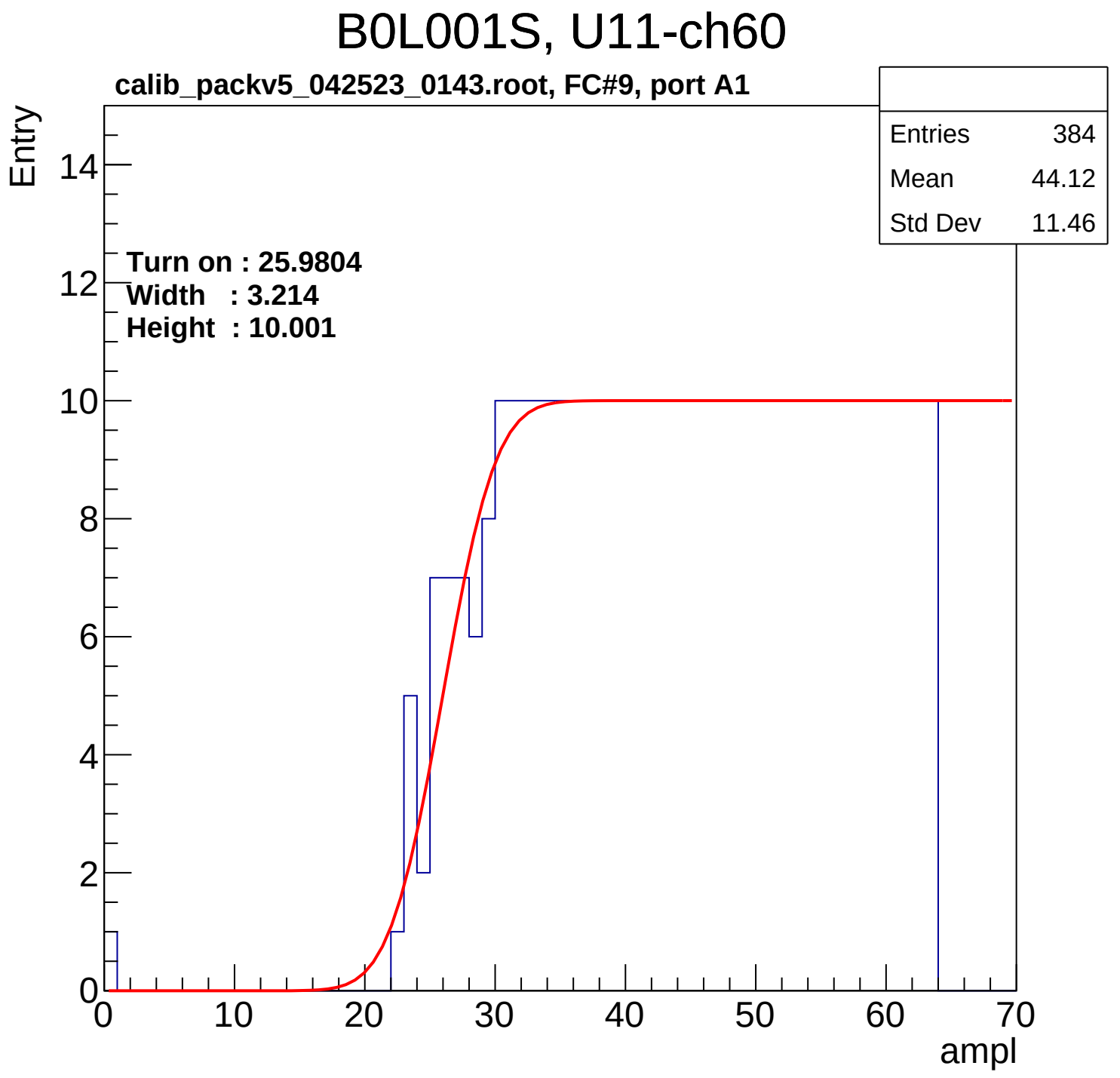
B0L001S, U11-ch60
calib_packv5_042523_0143.root, FC#9, port A1
Entries 384
Mean 44.12
Std Dev 11.46
Turn on : 25.9804
Width : 3.214
Height : 10.001
Entry
ampl
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2
4
6
8
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0
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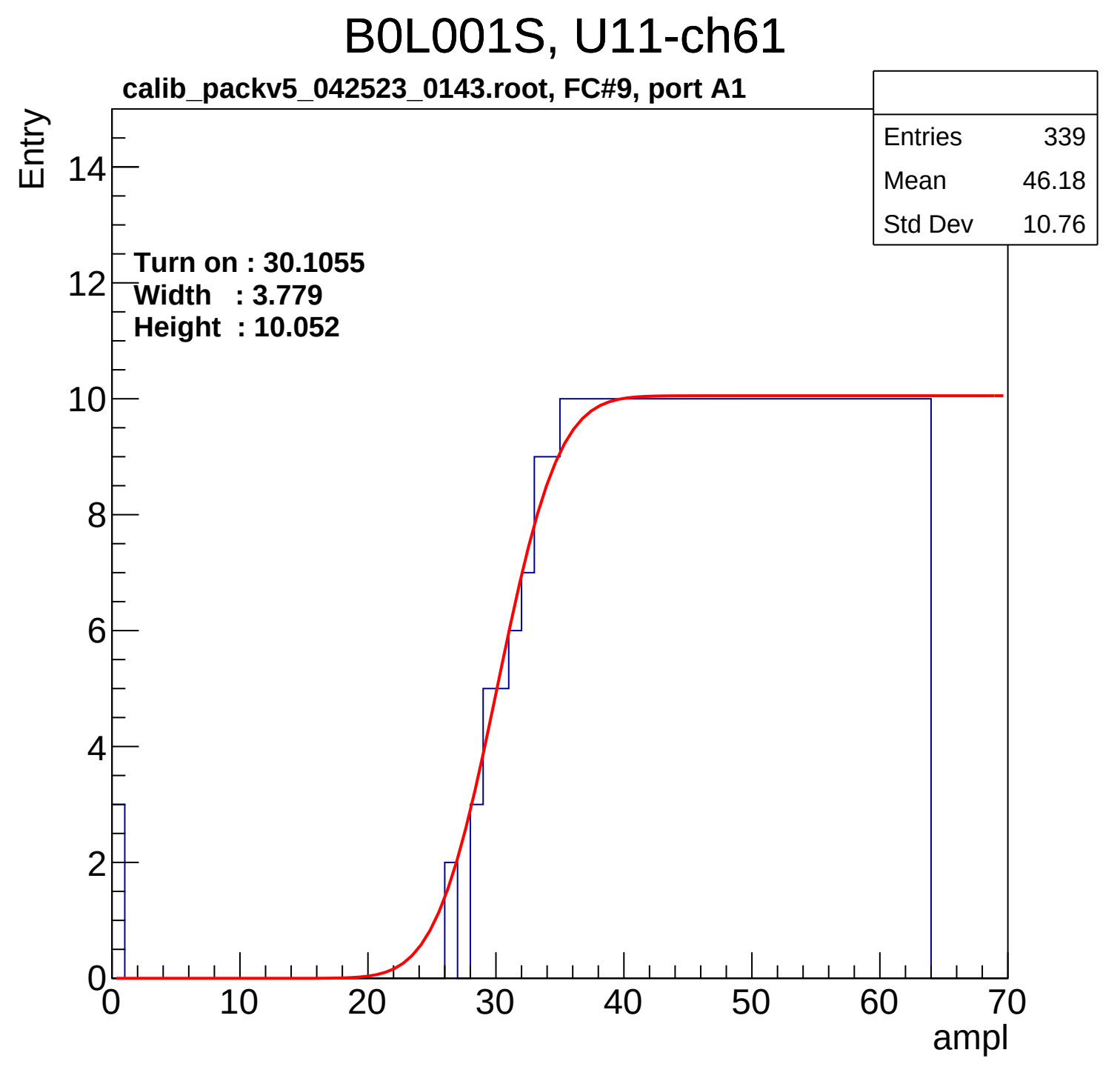
B0L001S, U11-ch61
calib_packv5_042523_0143.root, FC#9, port A1
Entries 339
Mean 46.18
Std Dev 10.76
Turn on : 30.1055
Width : 3.779
Height : 10.052
Entry
ampl
0
2
4
6
8
10
12
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0
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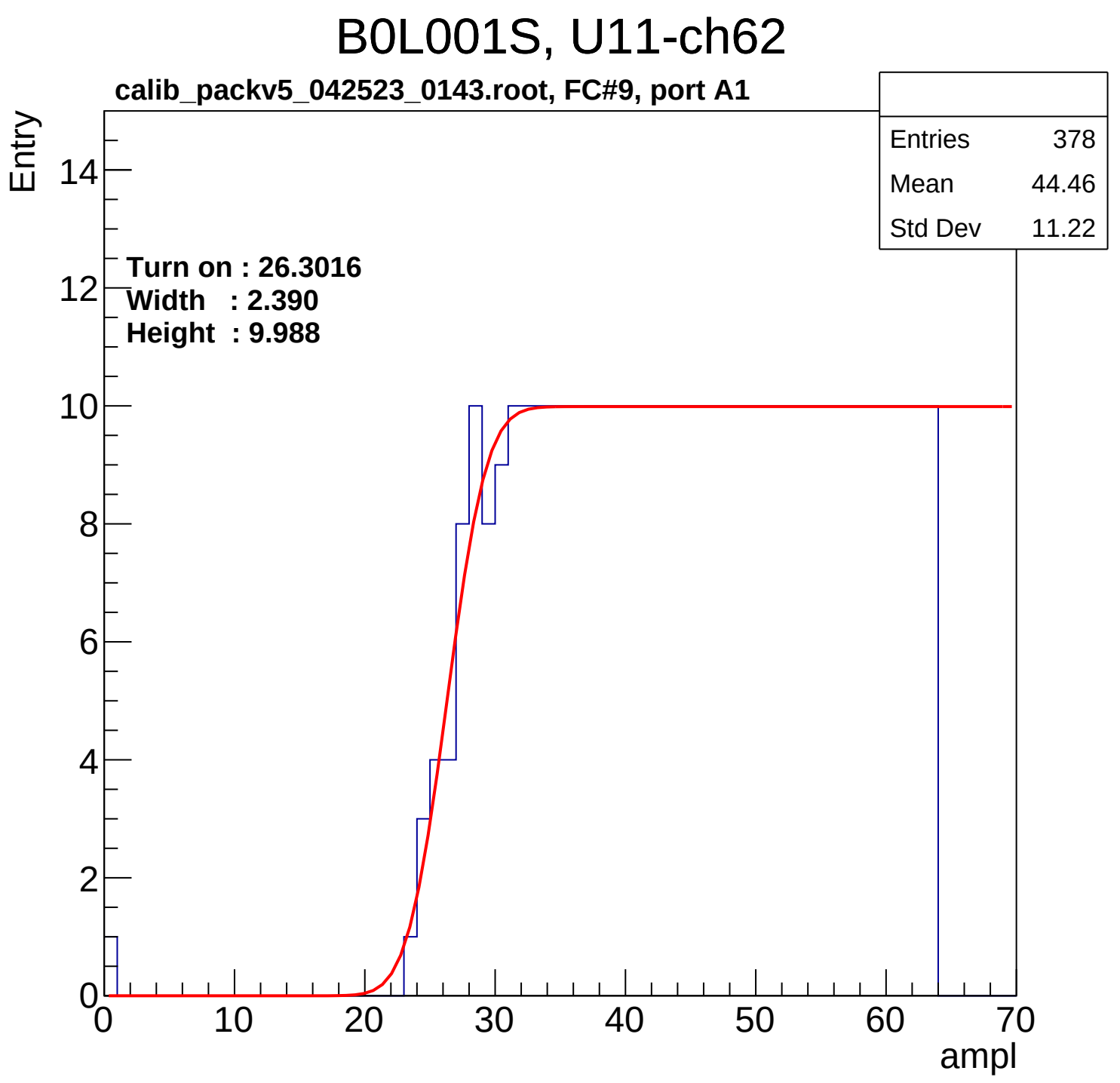
B0L001S, U11-ch62
calib_packv5_042523_0143.root, FC#9, port A1
Entries 378
Mean 44.46
Std Dev 11.22
Turn on : 26.3016
Width : 2.390
Height : 9.988
Entry
ampl
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2
4
6
8
10
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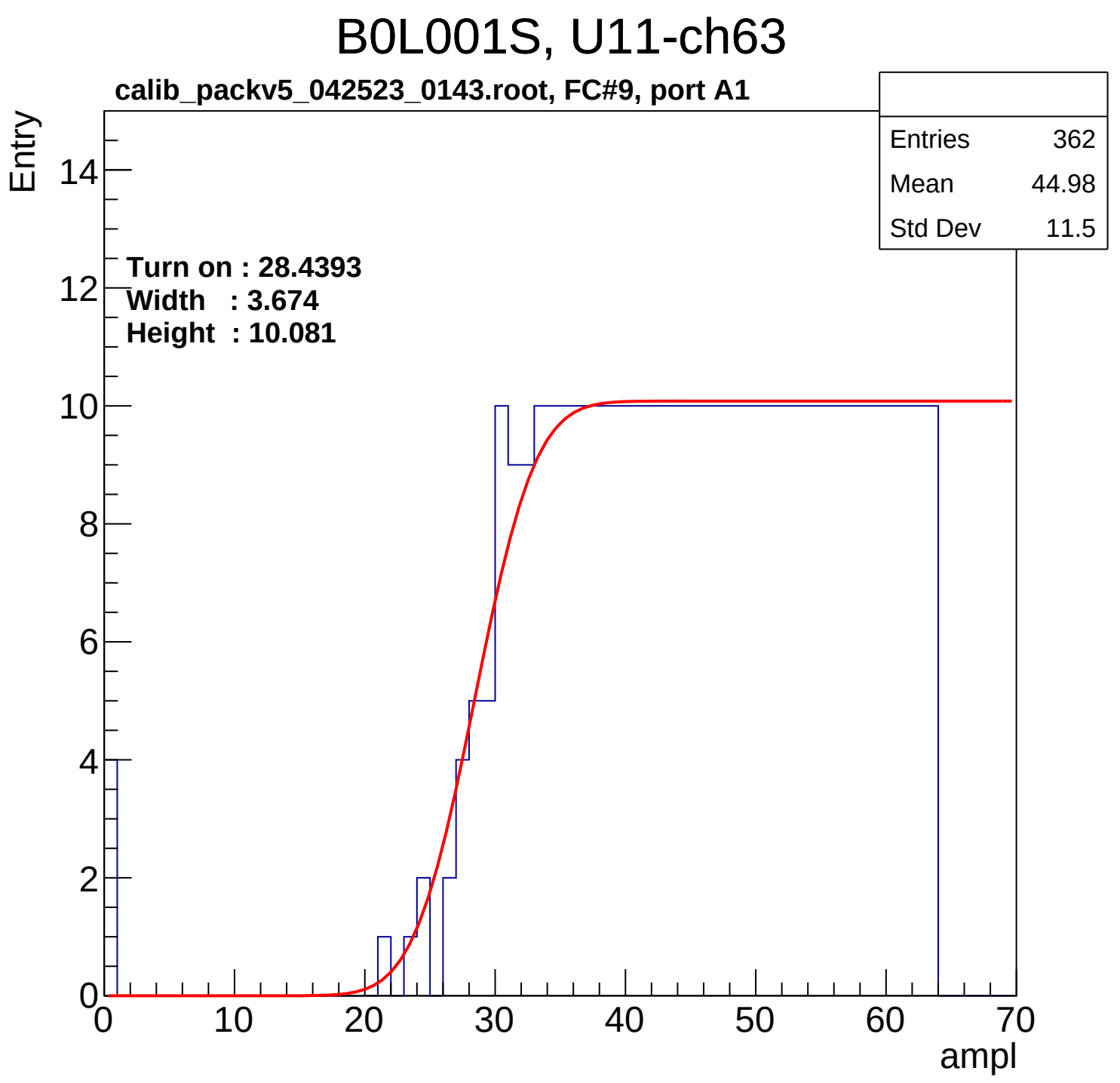
B0L001S, U11-ch63
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 44.98
Std Dev 11.5
Turn on : 28.4393
Width : 3.674
Height : 10.081
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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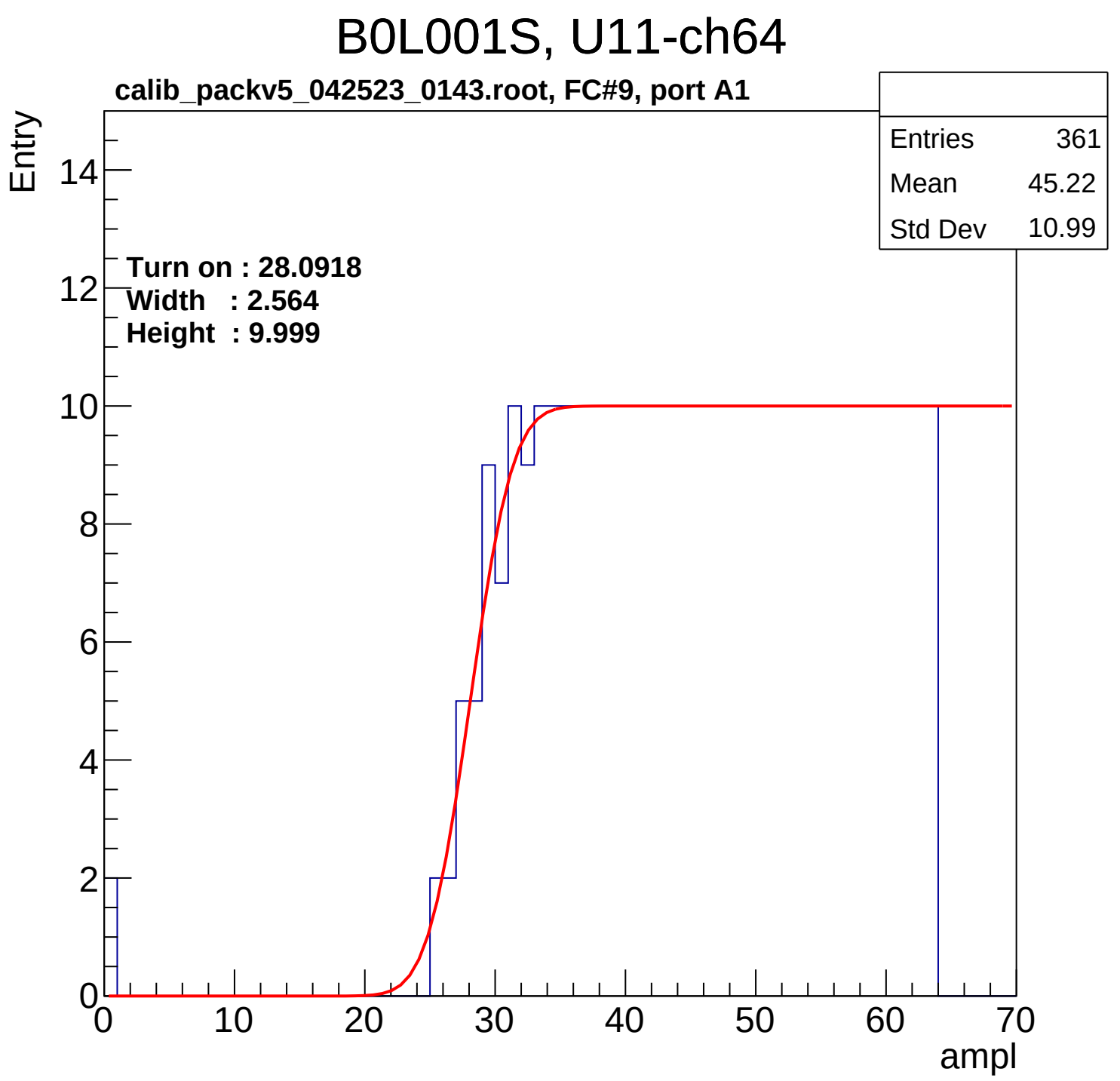
B0L001S, U11-ch64
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 45.22
Std Dev 10.99
Turn on : 28.0918
Width : 2.564
Height : 9.999
Entry
ampl
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2
4
6
8
10
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0
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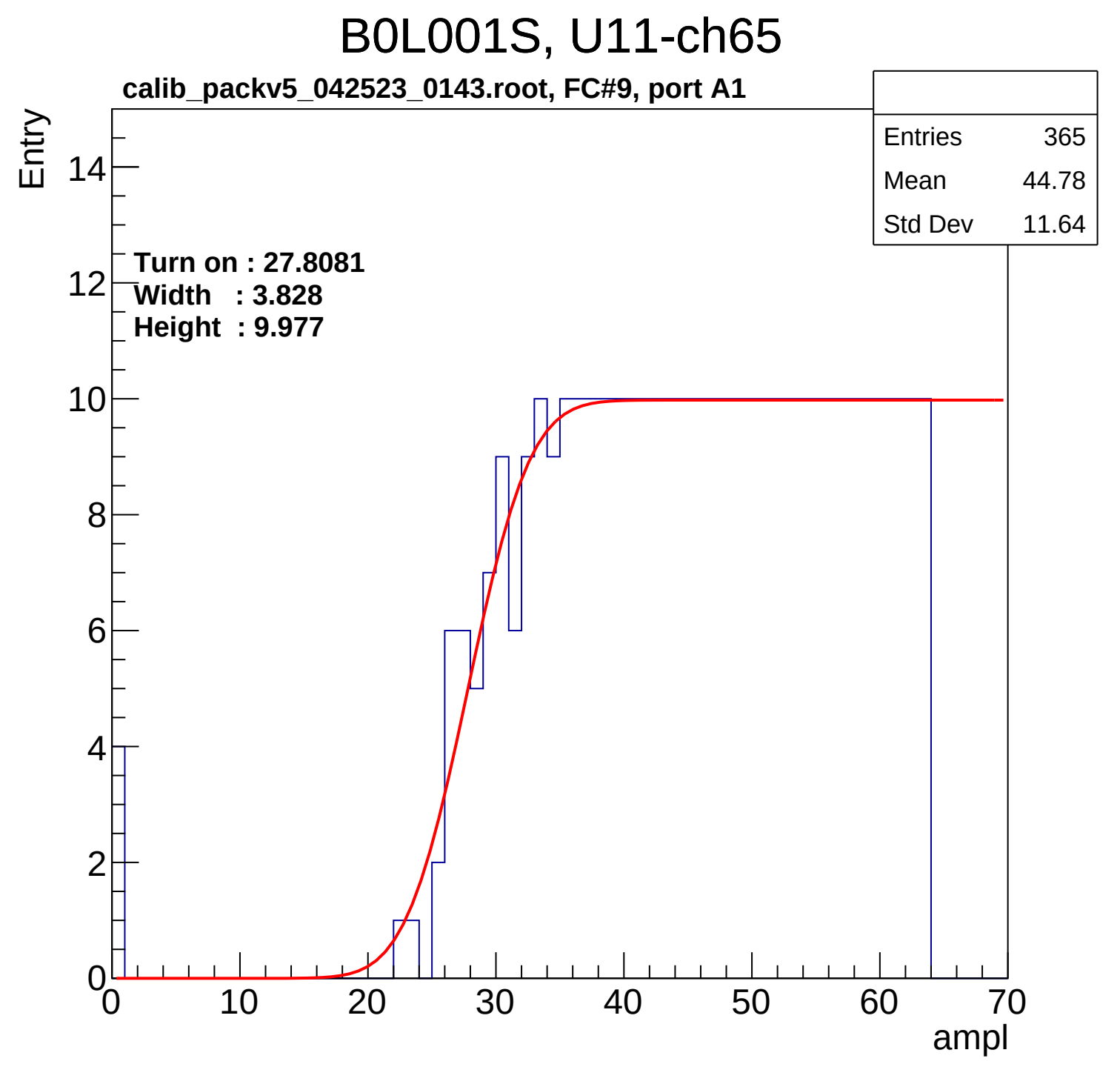
B0L001S, U11-ch65
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 44.78
Std Dev 11.64
Turn on : 27.8081
Width : 3.828
Height : 9.977
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
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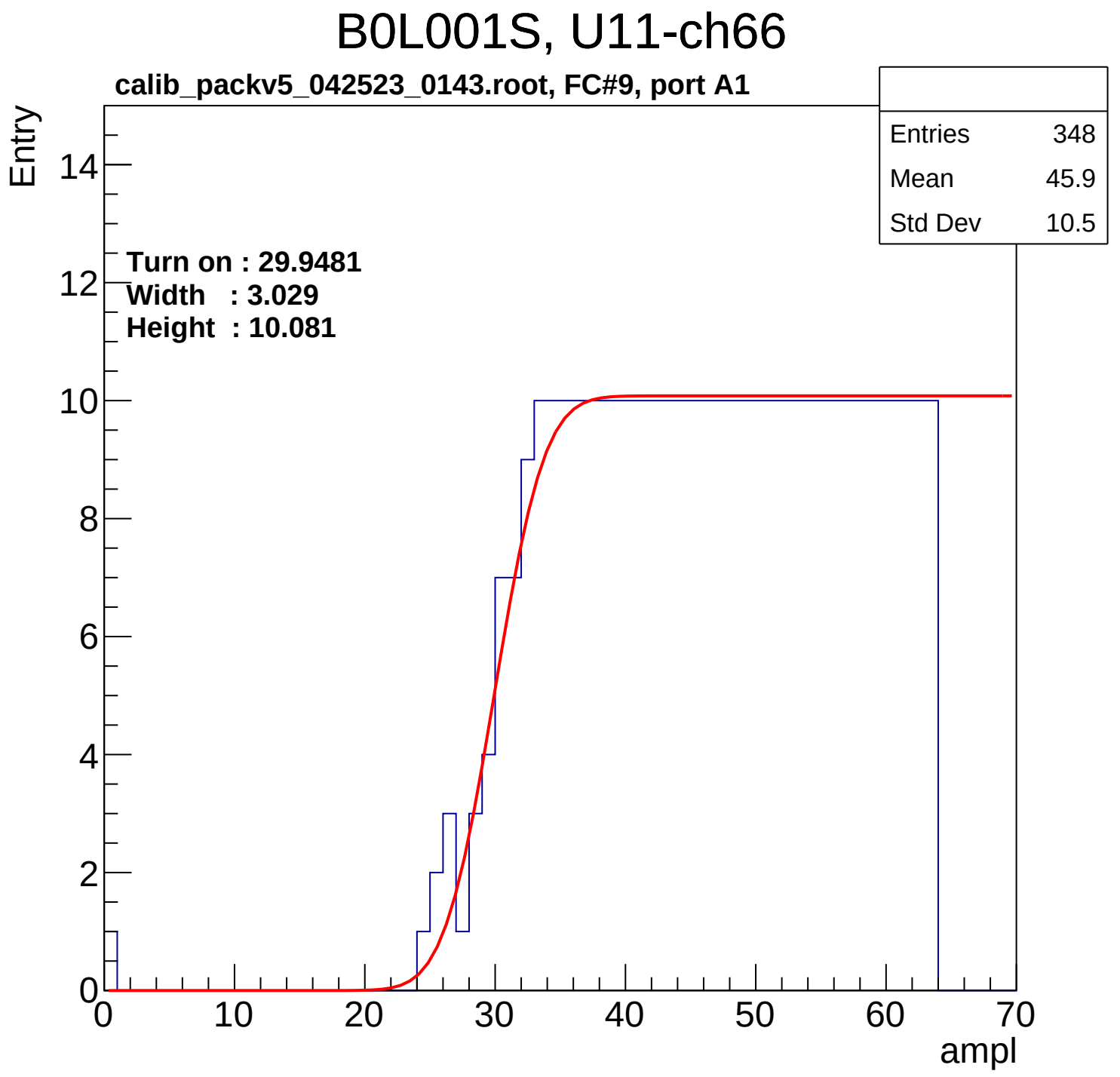
60
70


B0L001S, U11-ch66
calib_packv5_042523_0143.root, FC#9, port A1
Entries 348
Mean 45.9
Std Dev 10.5
Turn on : 29.9481
Width : 3.029
Height : 10.081
Entry
ampl
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2
4
6
8
10
12
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0
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20
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40
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60
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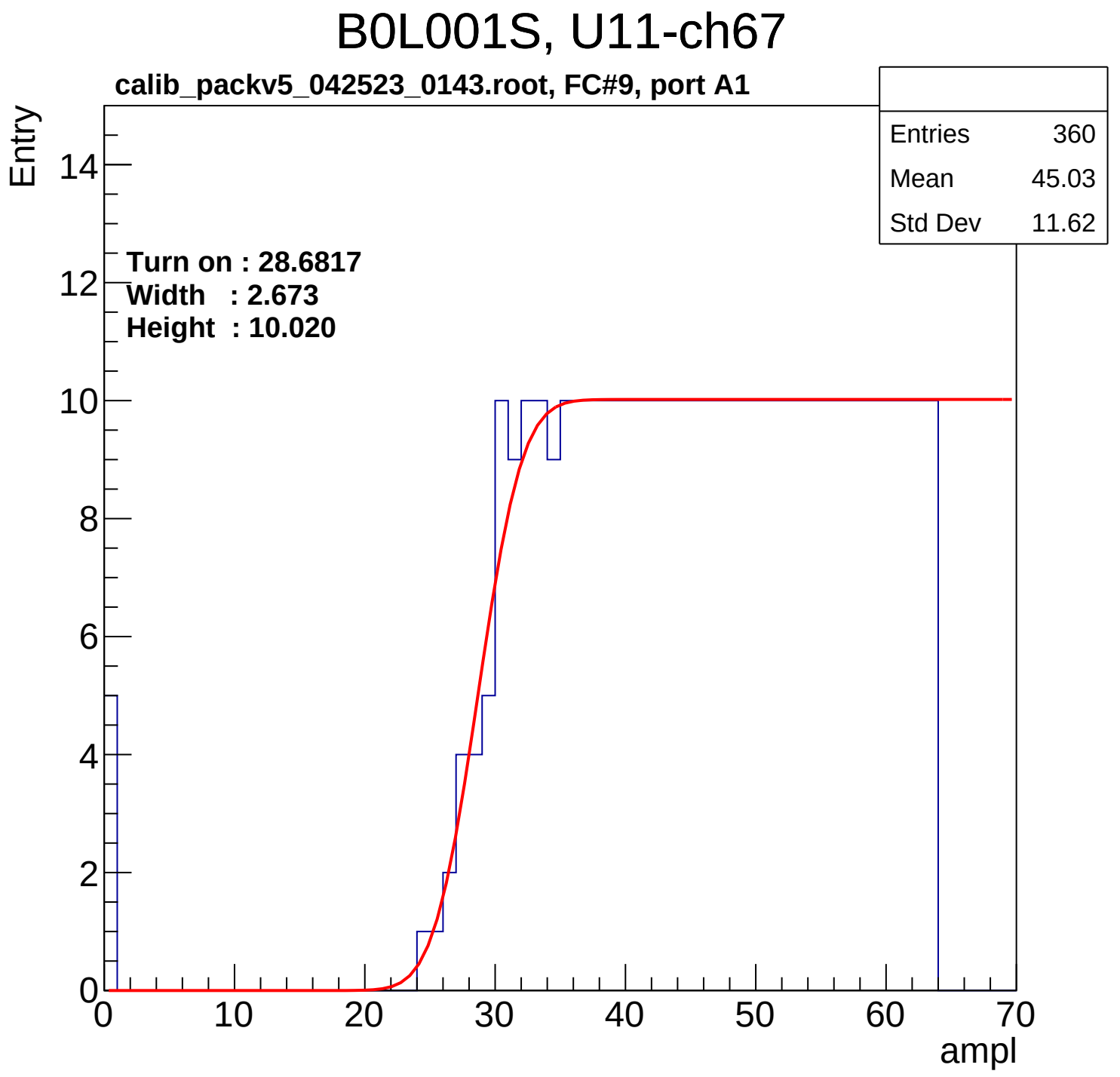
B0L001S, U11-ch67
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 45.03
Std Dev 11.62
Turn on : 28.6817
Width : 2.673
Height : 10.020
Entry
ampl
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2
4
6
8
10
12
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0
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60
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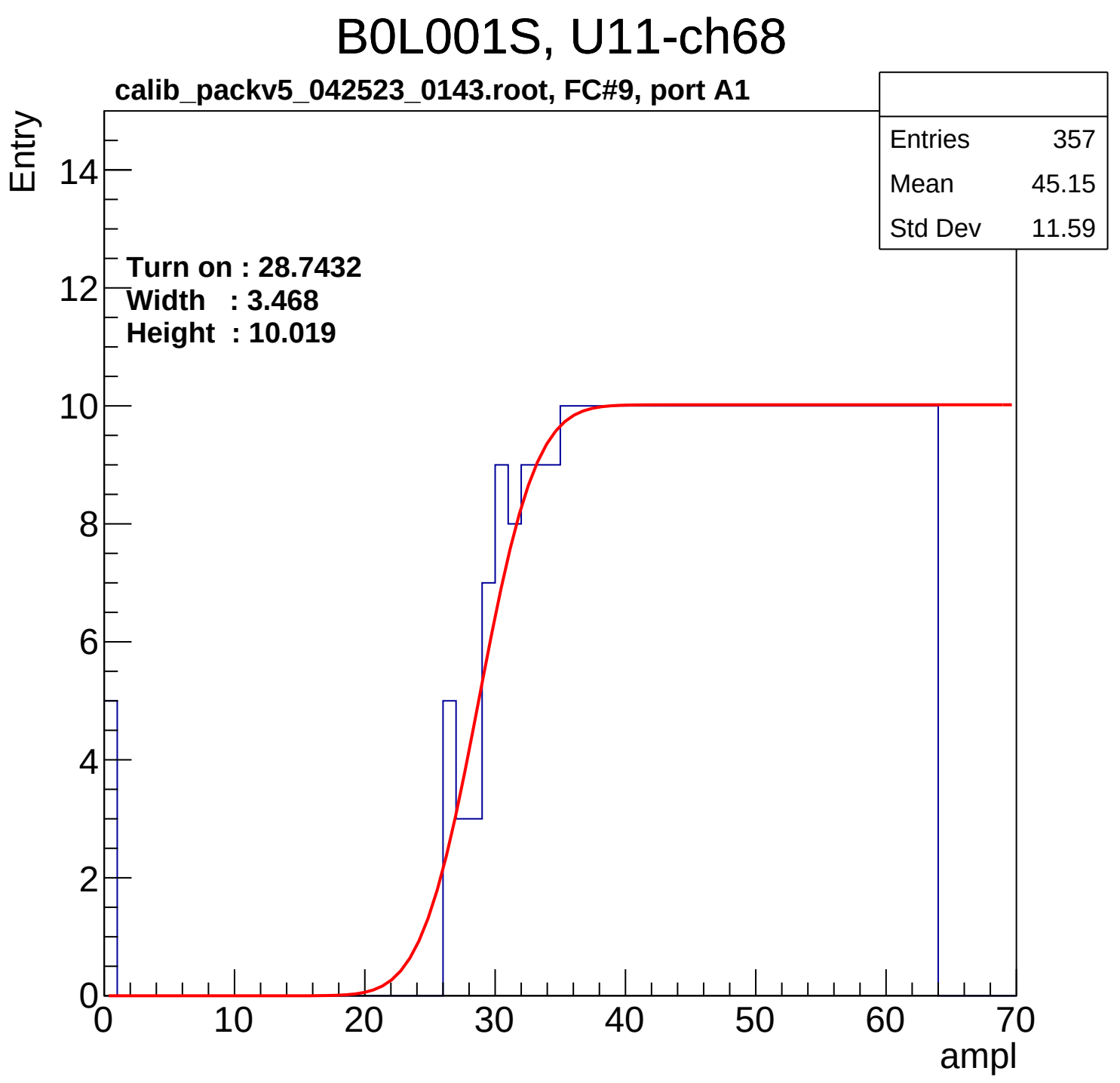
B0L001S, U11-ch68
calib_packv5_042523_0143.root, FC#9, port A1
Entries 357
Mean 45.15
Std Dev 11.59
Turn on : 28.7432
Width : 3.468
Height : 10.019
Entry
ampl
0
2
4
6
8
10
12
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0
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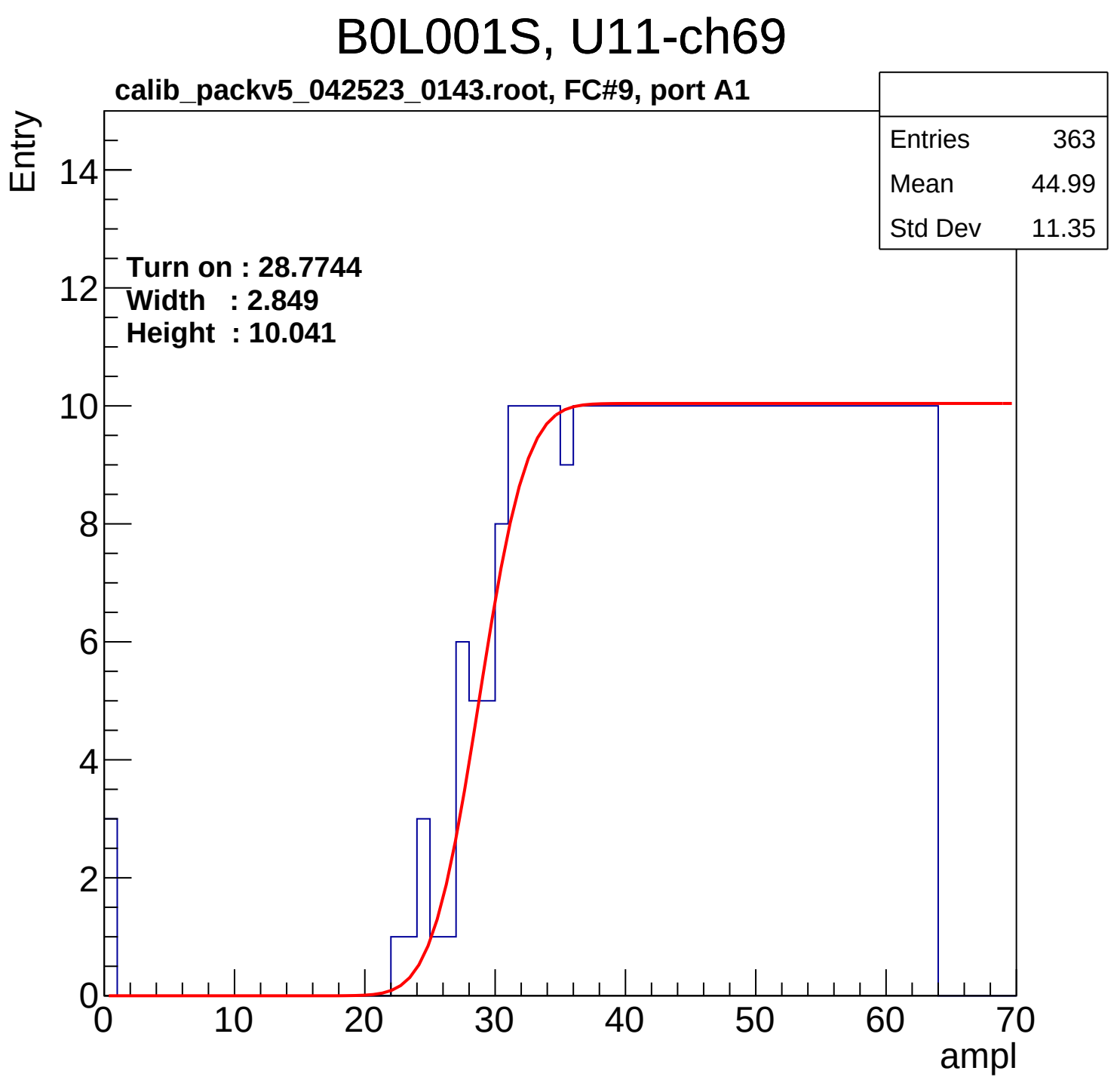
B0L001S, U11-ch69
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 44.99
Std Dev 11.35
Turn on : 28.7744
Width : 2.849
Height : 10.041
Entry
ampl
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2
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6
8
10
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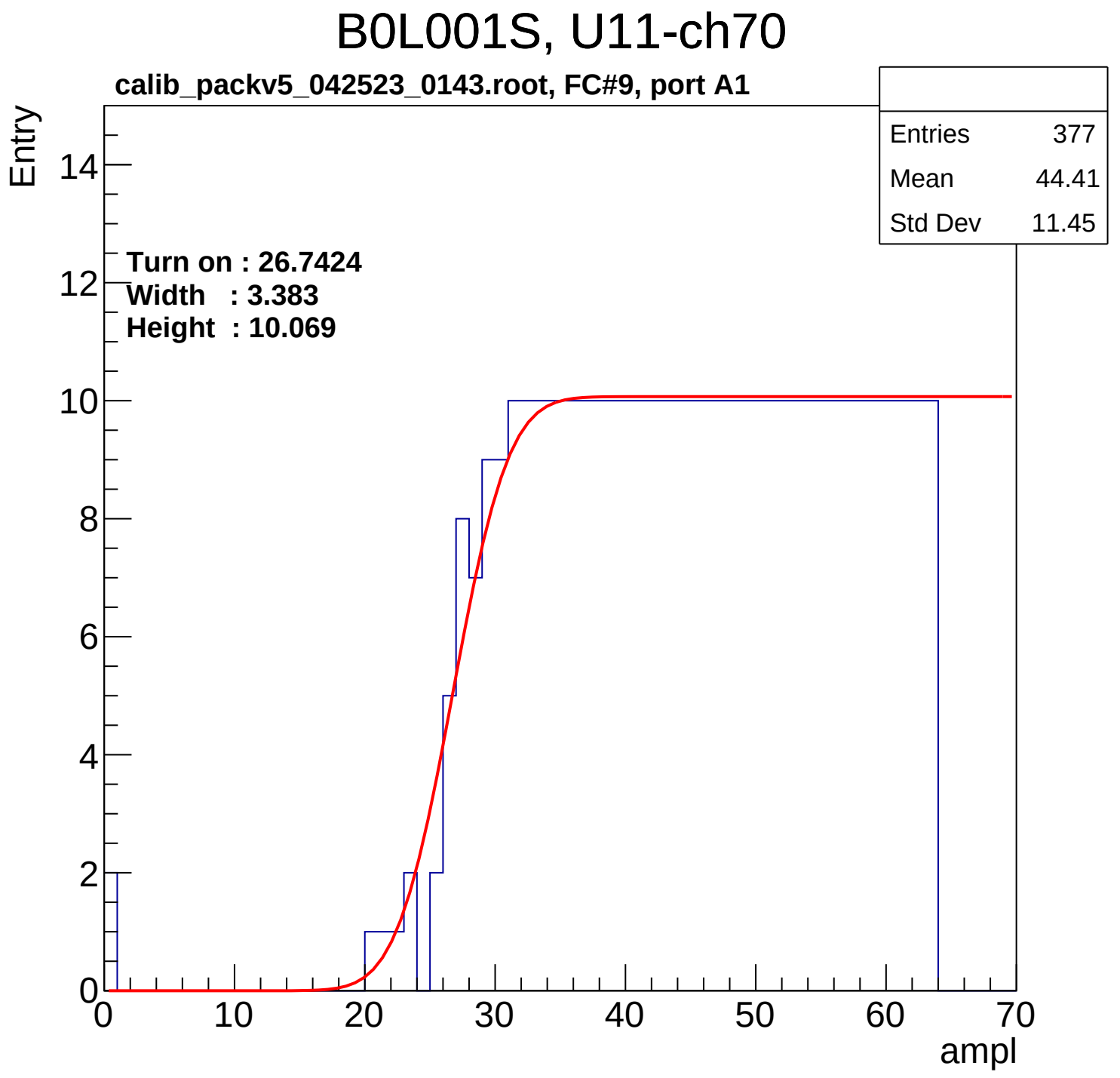
B0L001S, U11-ch70
calib_packv5_042523_0143.root, FC#9, port A1
Entries 377
Mean 44.41
Std Dev 11.45
Turn on : 26.7424
Width : 3.383
Height : 10.069
Entry
ampl
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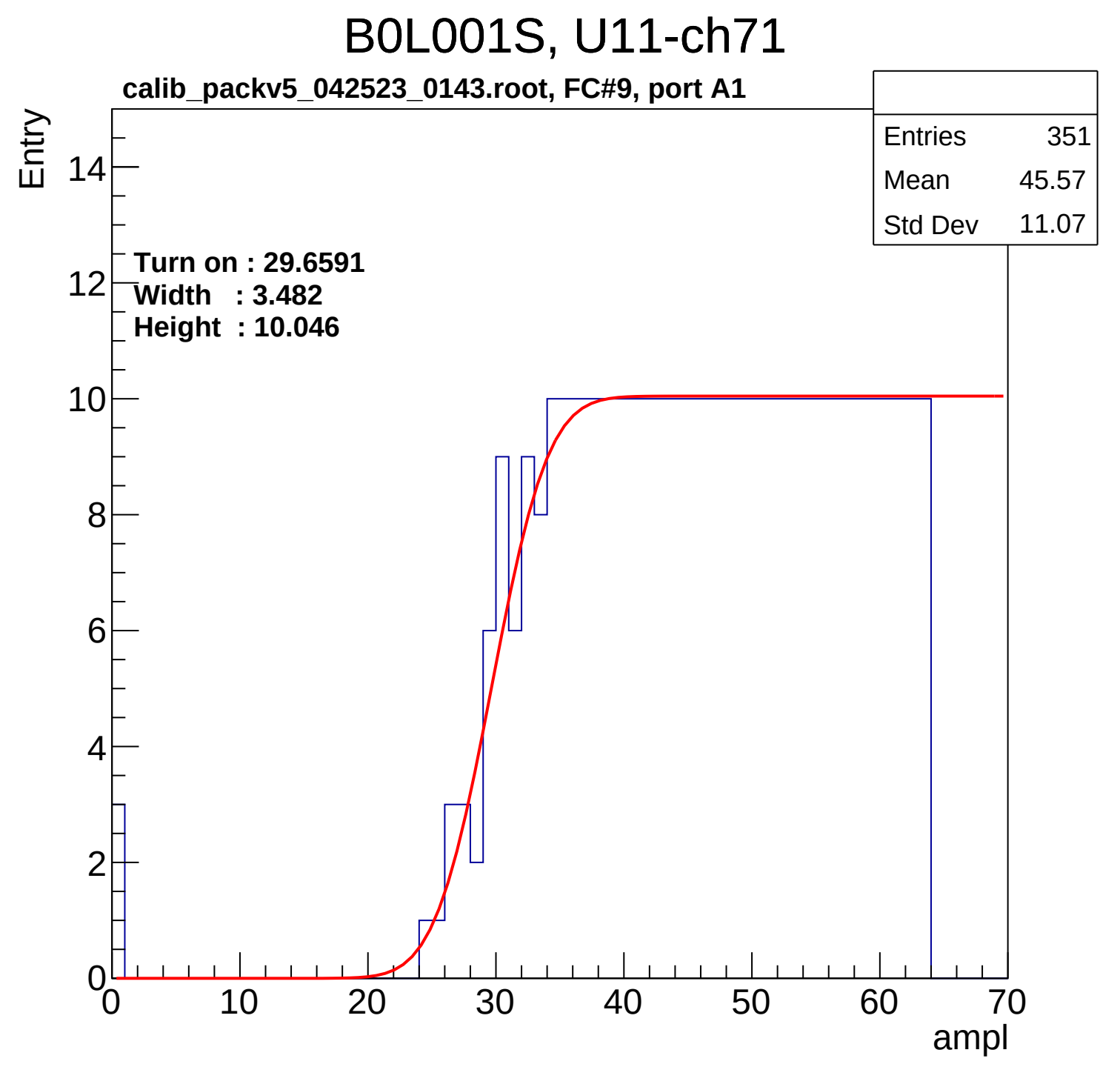
B0L001S, U11-ch71
calib_packv5_042523_0143.root, FC#9, port A1
Entries 351
Mean 45.57
Std Dev 11.07
Turn on : 29.6591
Width : 3.482
Height : 10.046
Entry
ampl
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6
8
10
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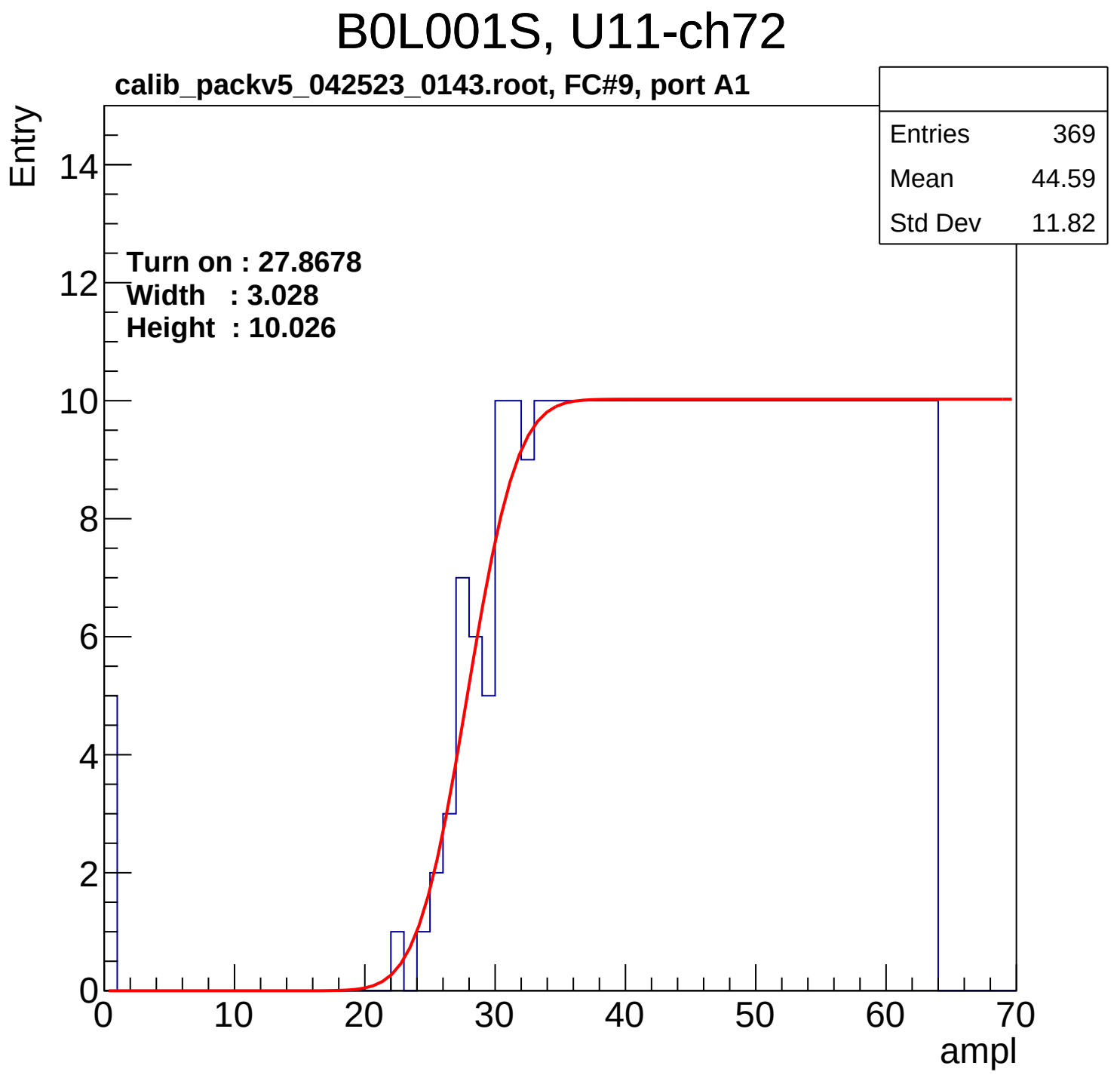
B0L001S, U11-ch72
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.59
Std Dev 11.82
Turn on : 27.8678
Width : 3.028
Height : 10.026
Entry
ampl
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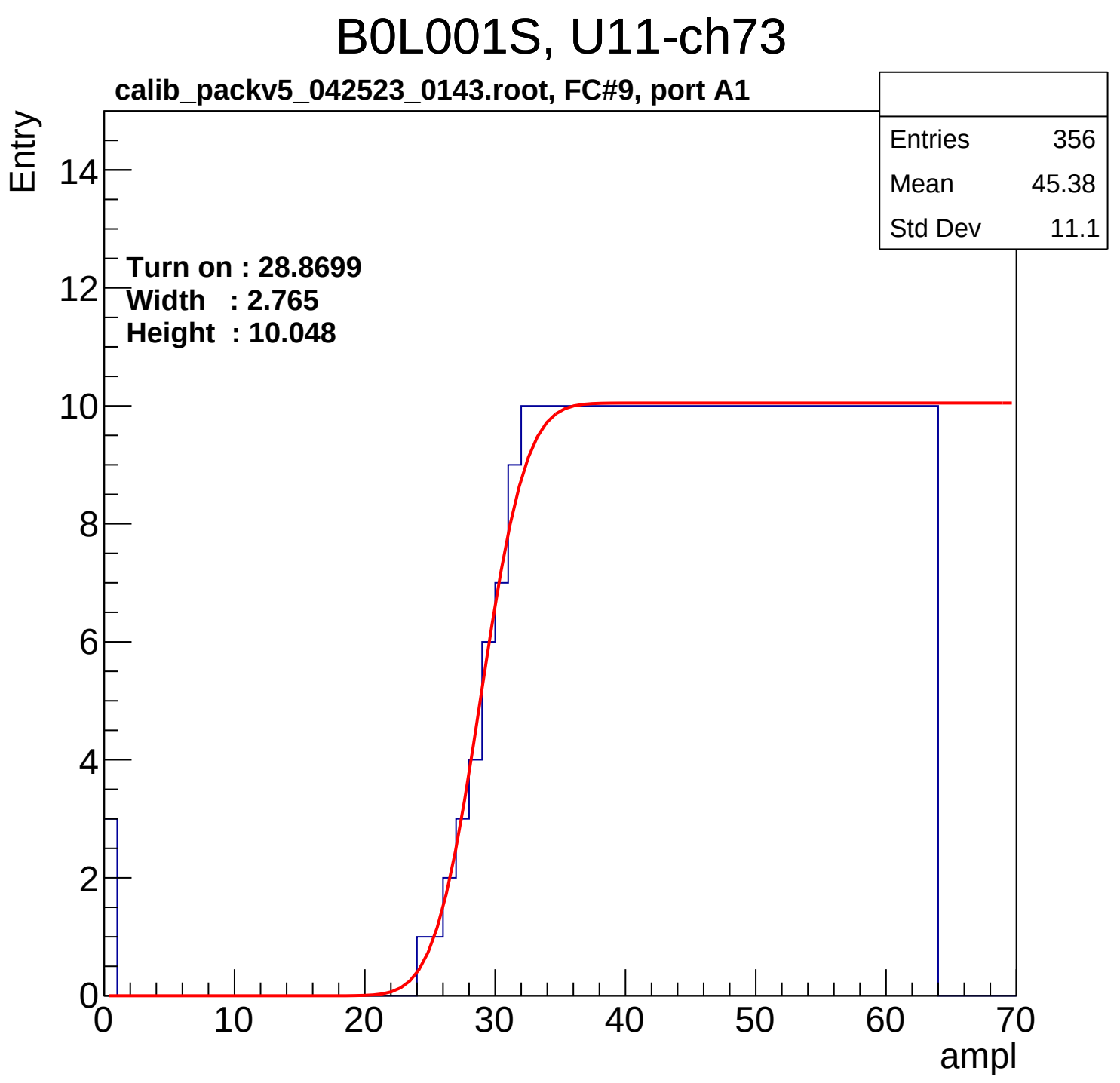
B0L001S, U11-ch73
calib_packv5_042523_0143.root, FC#9, port A1
Entries 356
Mean 45.38
Std Dev 11.1
Turn on : 28.8699
Width : 2.765
Height : 10.048
Entry
ampl
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8
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12
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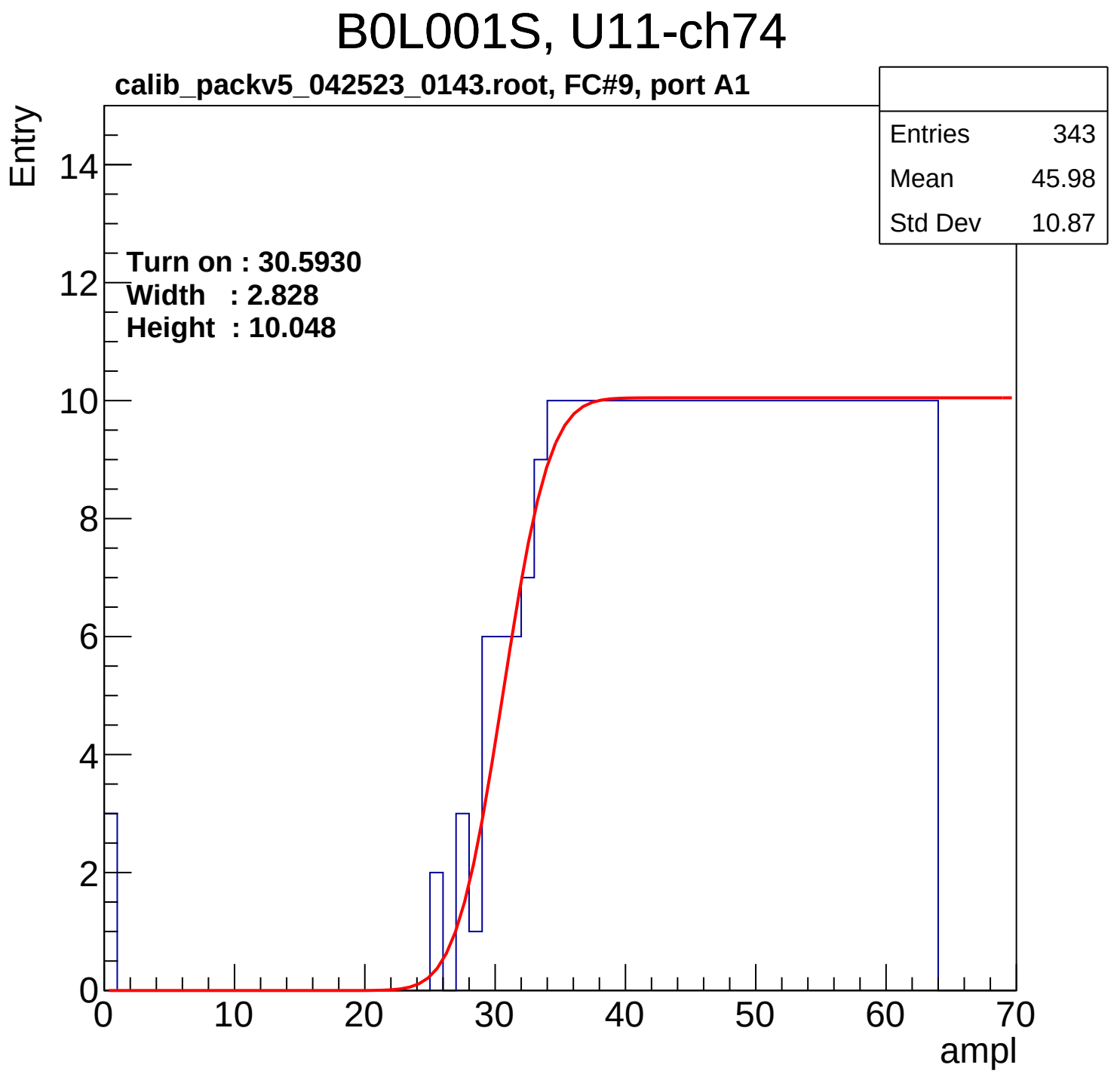
B0L001S, U11-ch74
calib_packv5_042523_0143.root, FC#9, port A1
Entries 343
Mean 45.98
Std Dev 10.87
Turn on : 30.5930
Width : 2.828
Height : 10.048
Entry
ampl
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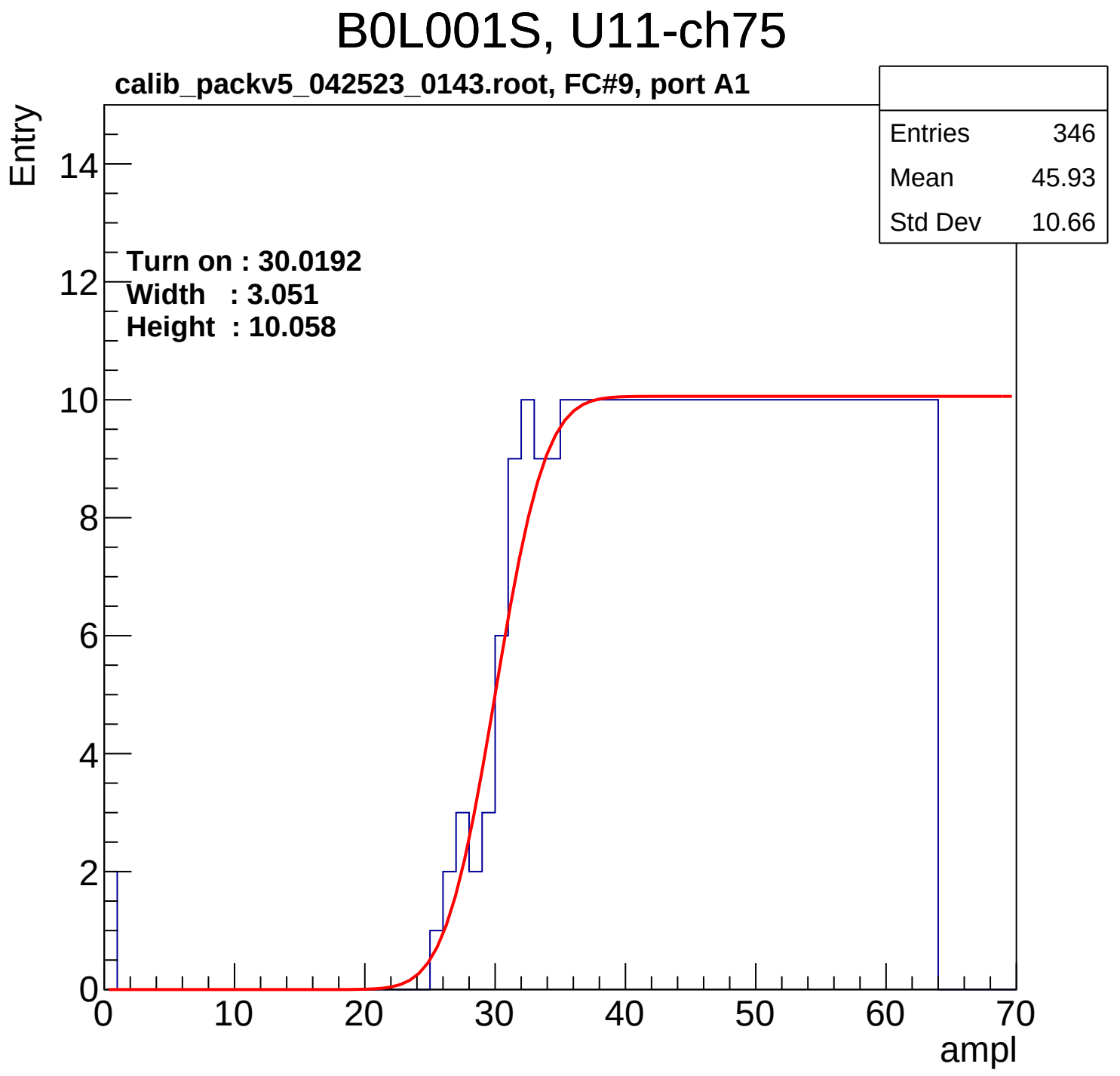
B0L001S, U11-ch75
calib_packv5_042523_0143.root, FC#9, port A1
Entries 346
Mean 45.93
Std Dev 10.66
Turn on : 30.0192
Width : 3.051
Height : 10.058
Entry
ampl
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8
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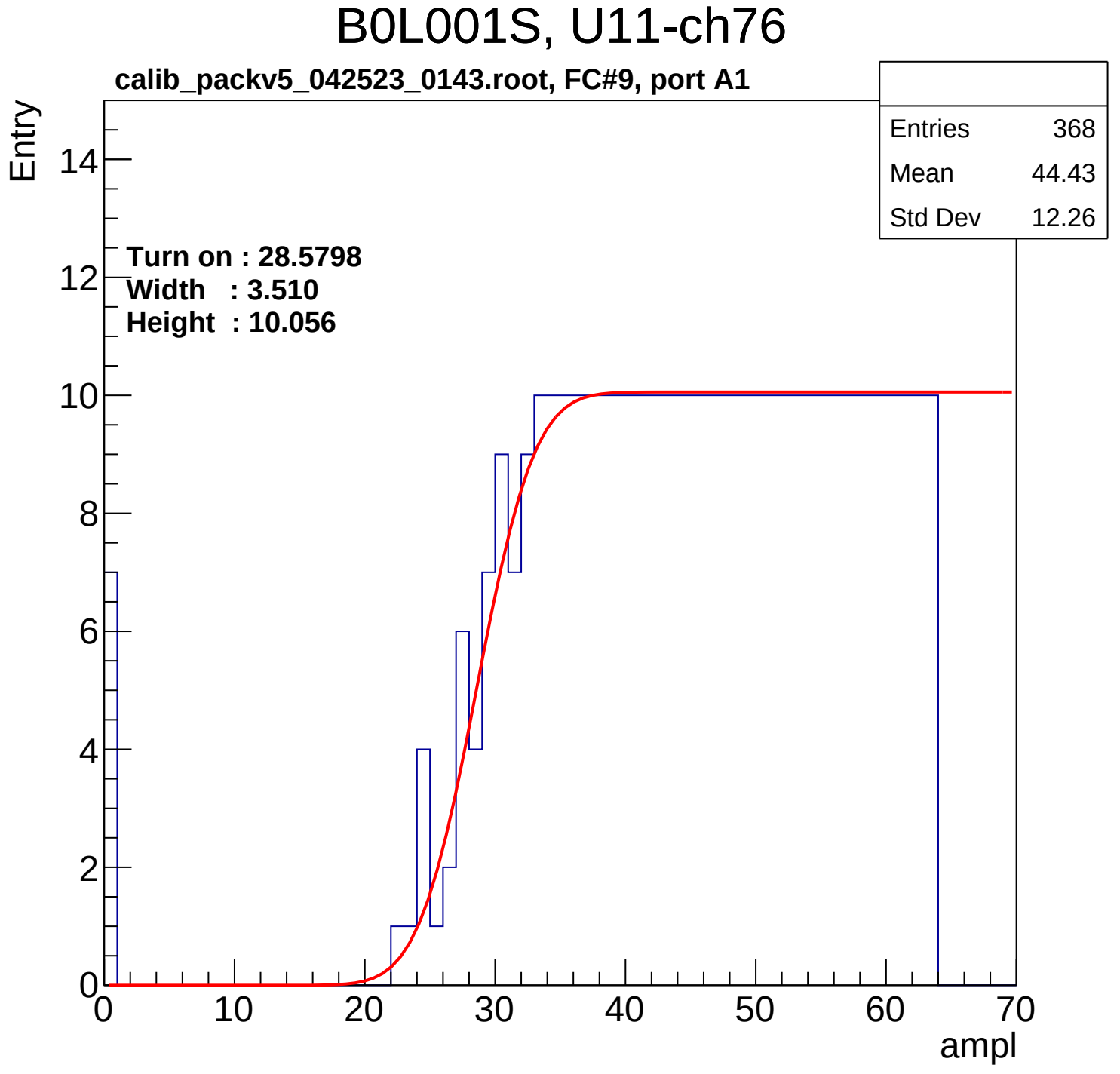
B0L001S, U11-ch76
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.43
Std Dev 12.26
Turn on : 28.5798
Width : 3.510
Height : 10.056
Entry
ampl
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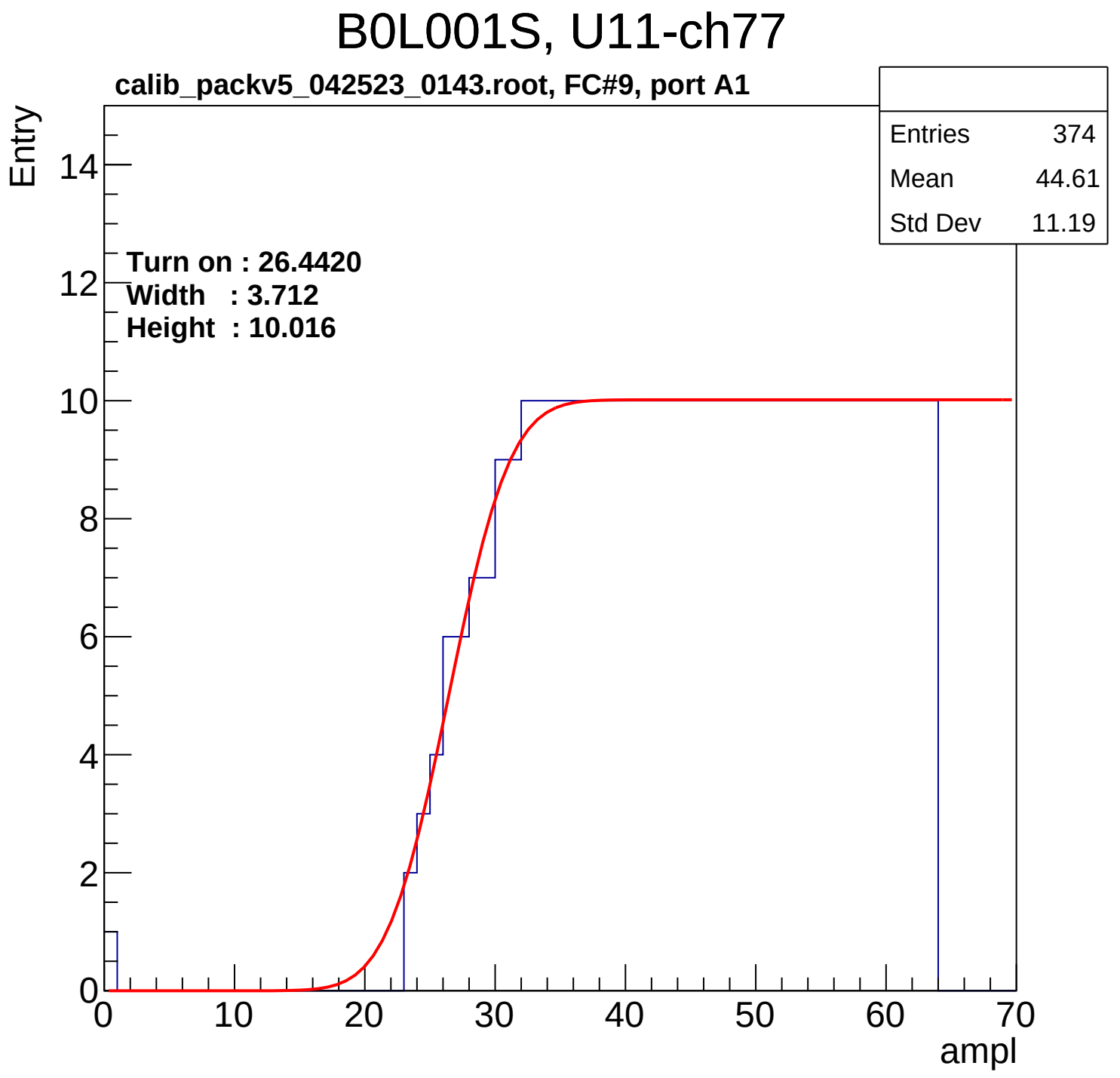
B0L001S, U11-ch77
calib_packv5_042523_0143.root, FC#9, port A1
Entries 374
Mean 44.61
Std Dev 11.19
Turn on : 26.4420
Width : 3.712
Height : 10.016
Entry
ampl
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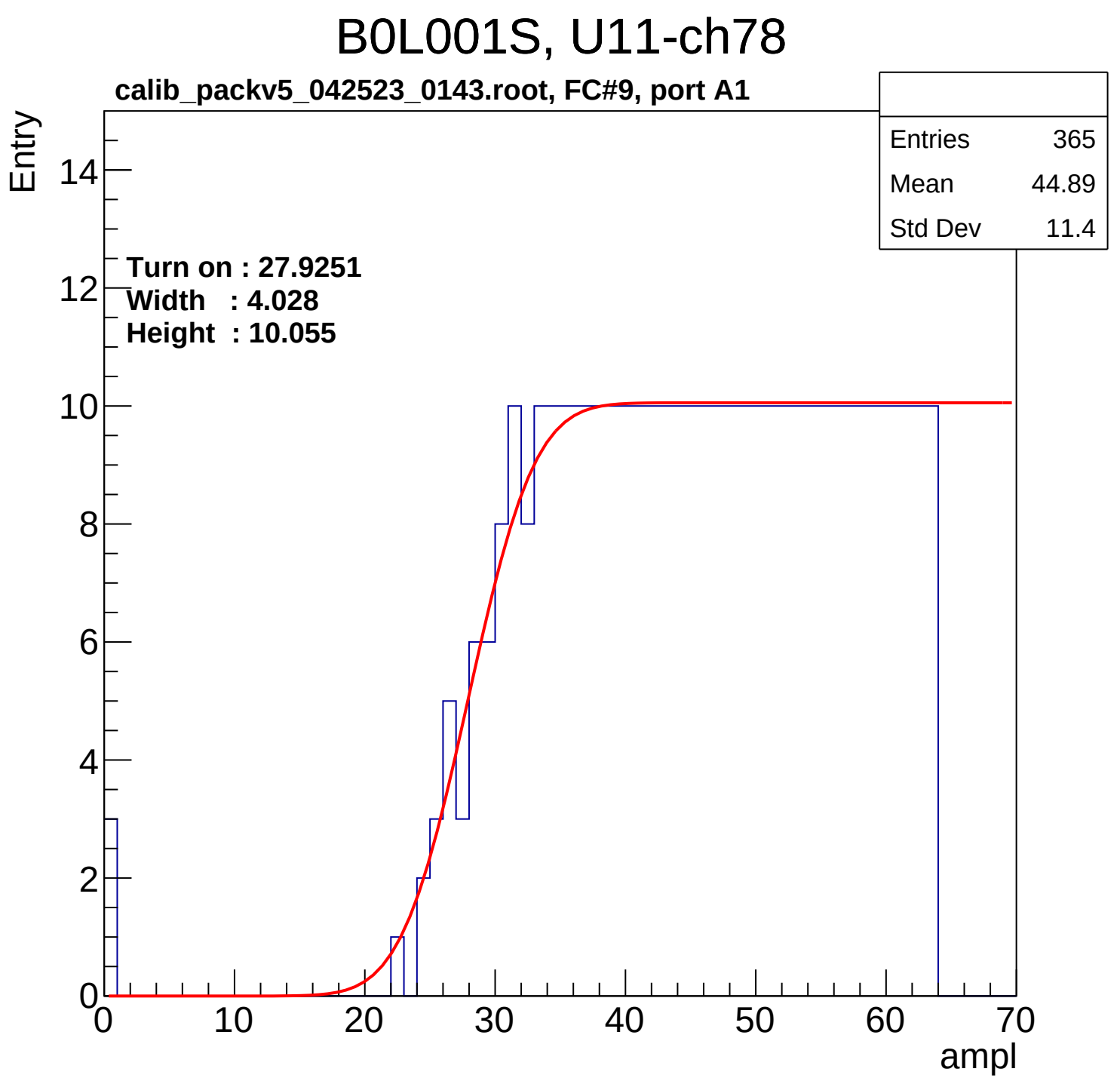
B0L001S, U11-ch78
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 44.89
Std Dev 11.4
Turn on : 27.9251
Width : 4.028
Height : 10.055
Entry
ampl
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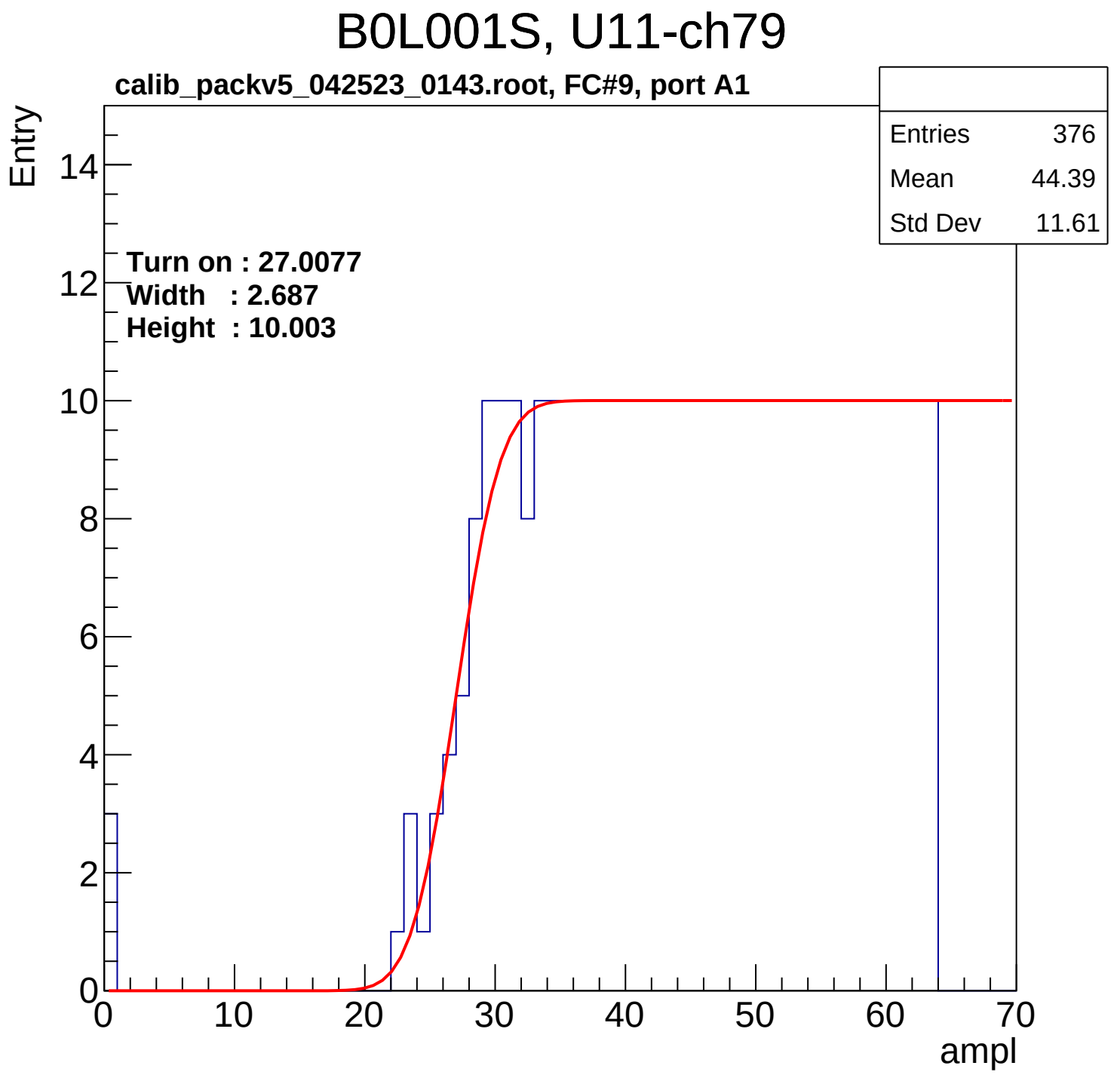
B0L001S, U11-ch79
calib_packv5_042523_0143.root, FC#9, port A1
Entries 376
Mean 44.39
Std Dev 11.61
Turn on : 27.0077
Width : 2.687
Height : 10.003
Entry
ampl
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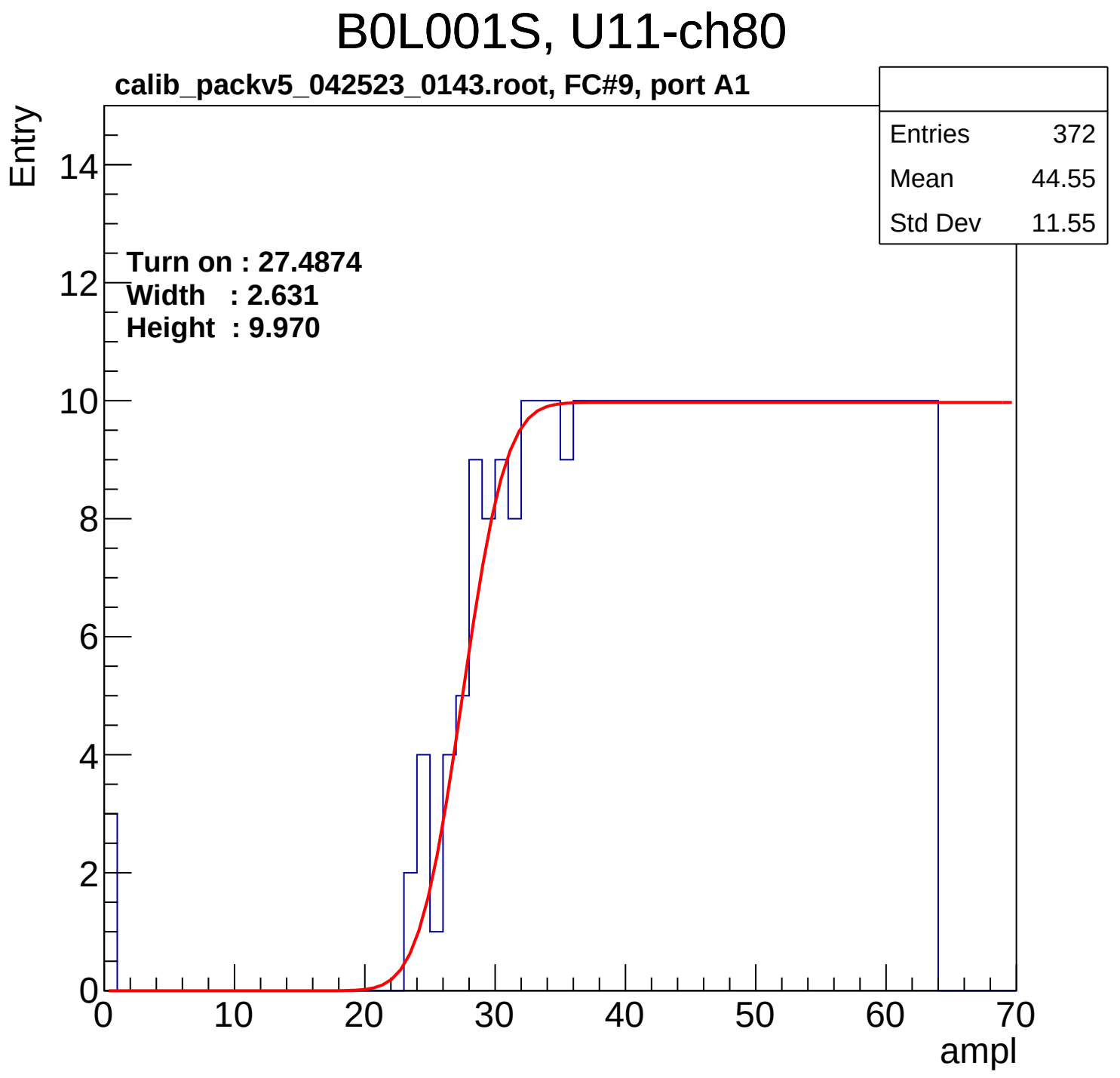
B0L001S, U11-ch80
calib_packv5_042523_0143.root, FC#9, port A1
Entries 372
Mean 44.55
Std Dev 11.55
Turn on : 27.4874
Width : 2.631
Height : 9.970
Entry
ampl
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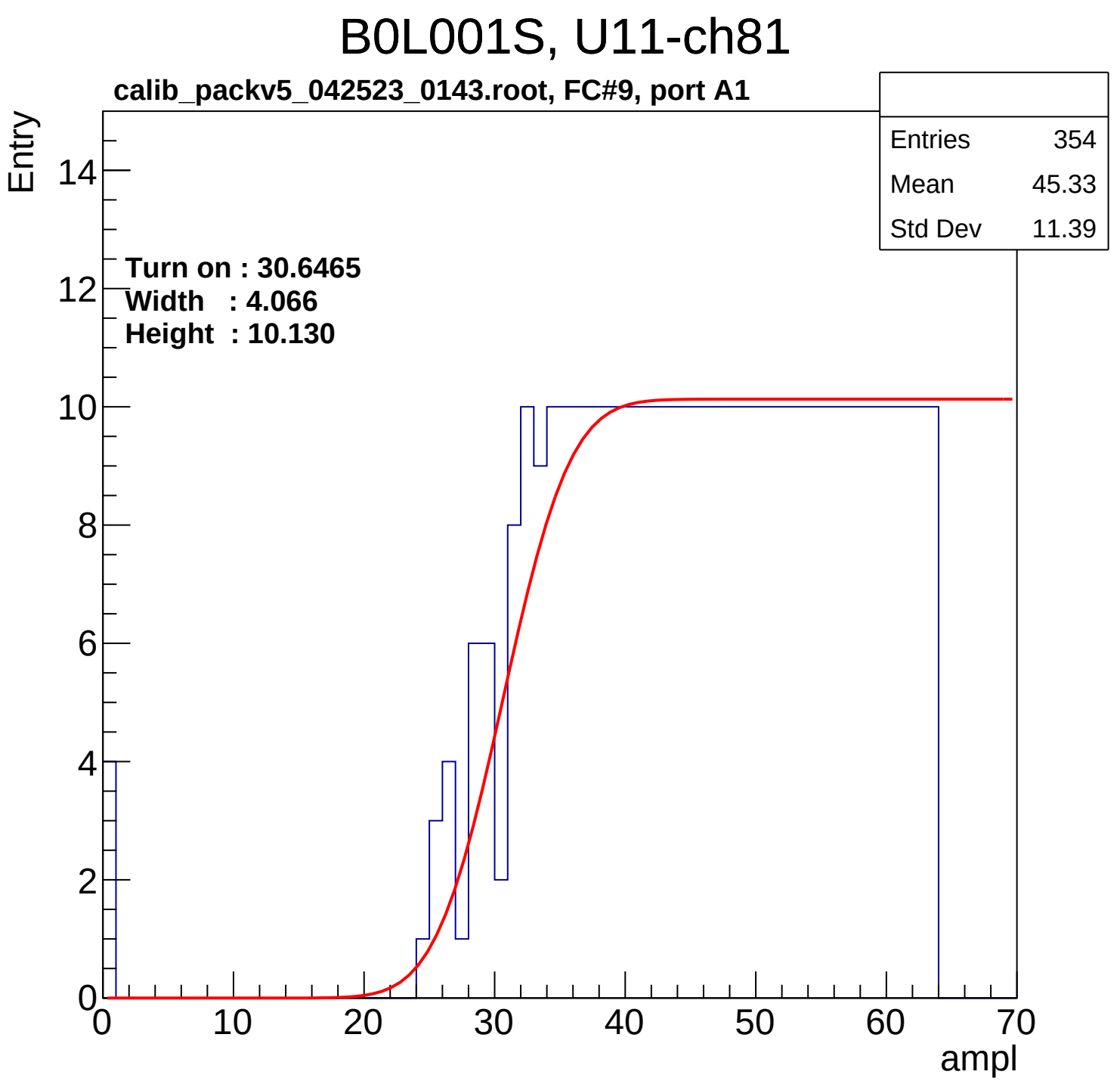
B0L001S, U11-ch81
calib_packv5_042523_0143.root, FC#9, port A1
Entries 354
Mean 45.33
Std Dev 11.39
Turn on : 30.6465
Width : 4.066
Height : 10.130
Entry
ampl
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6
8
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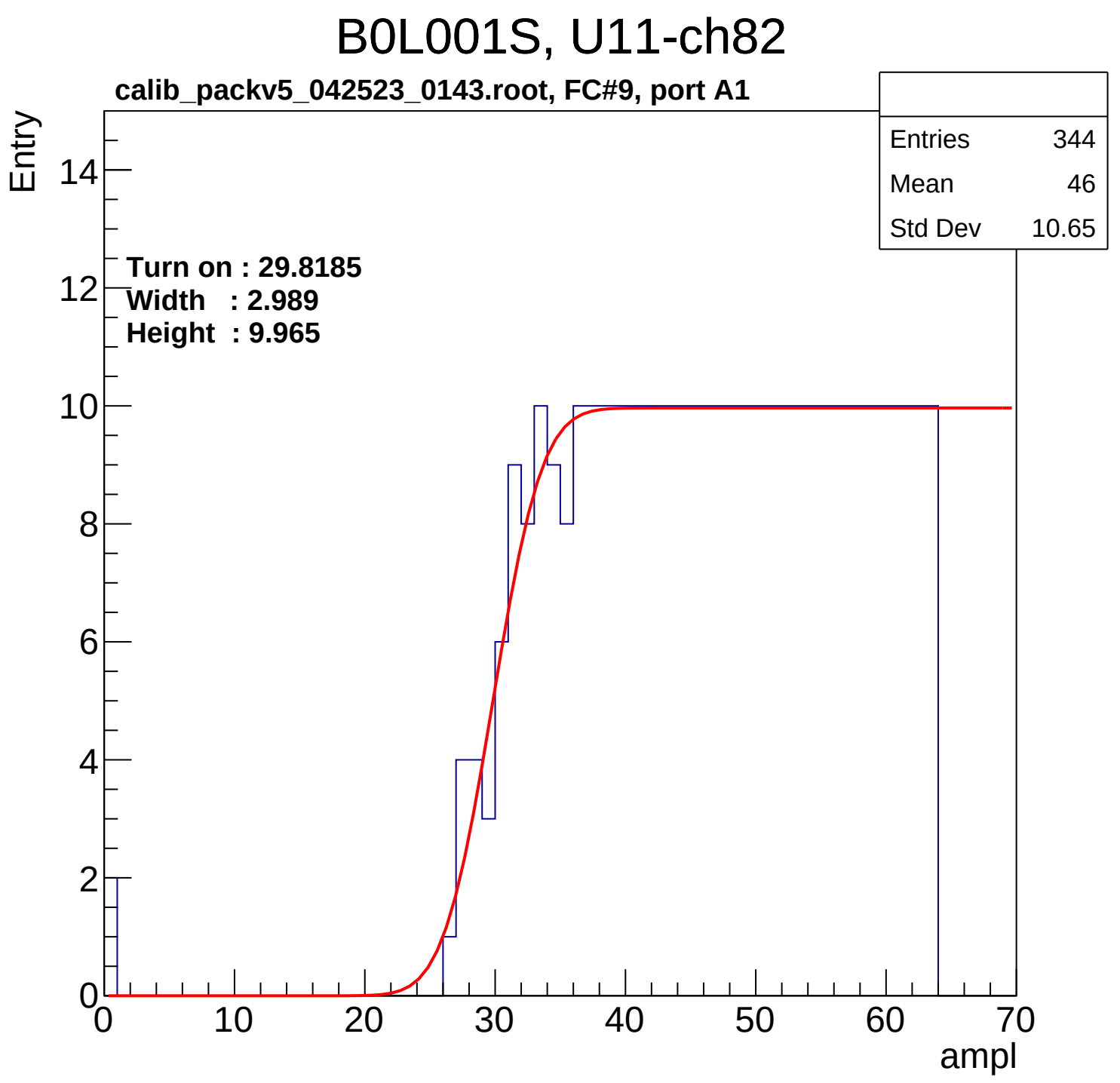
B0L001S, U11-ch82
calib_packv5_042523_0143.root, FC#9, port A1
Entries 344
Mean 46
Std Dev 10.65
Turn on : 29.8185
Width : 2.989
Height : 9.965
Entry
ampl
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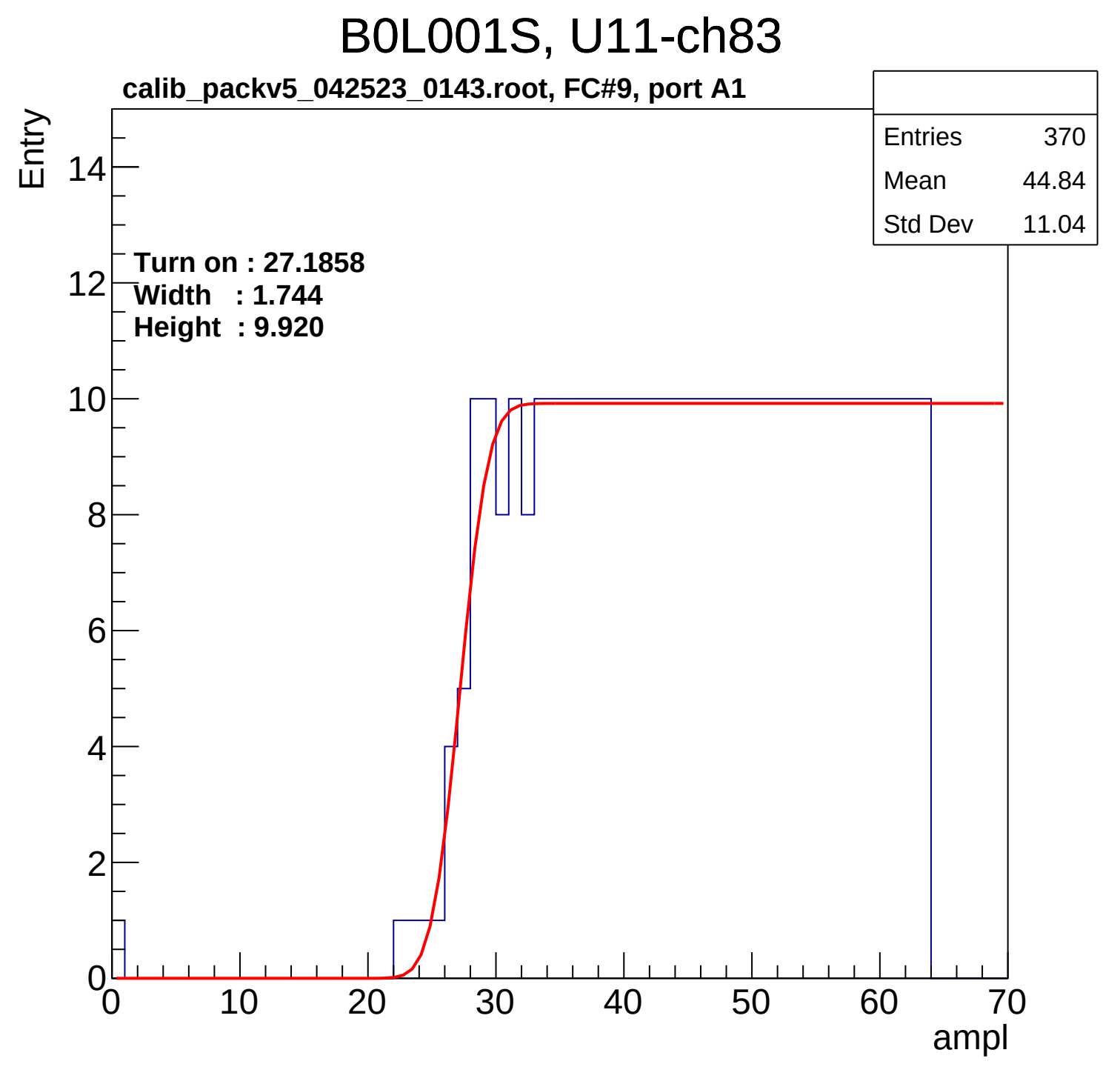
B0L001S, U11-ch83
calib_packv5_042523_0143.root, FC#9, port A1
Entries 370
Mean 44.84
Std Dev 11.04
Turn on : 27.1858
Width : 1.744
Height : 9.920
Entry
ampl
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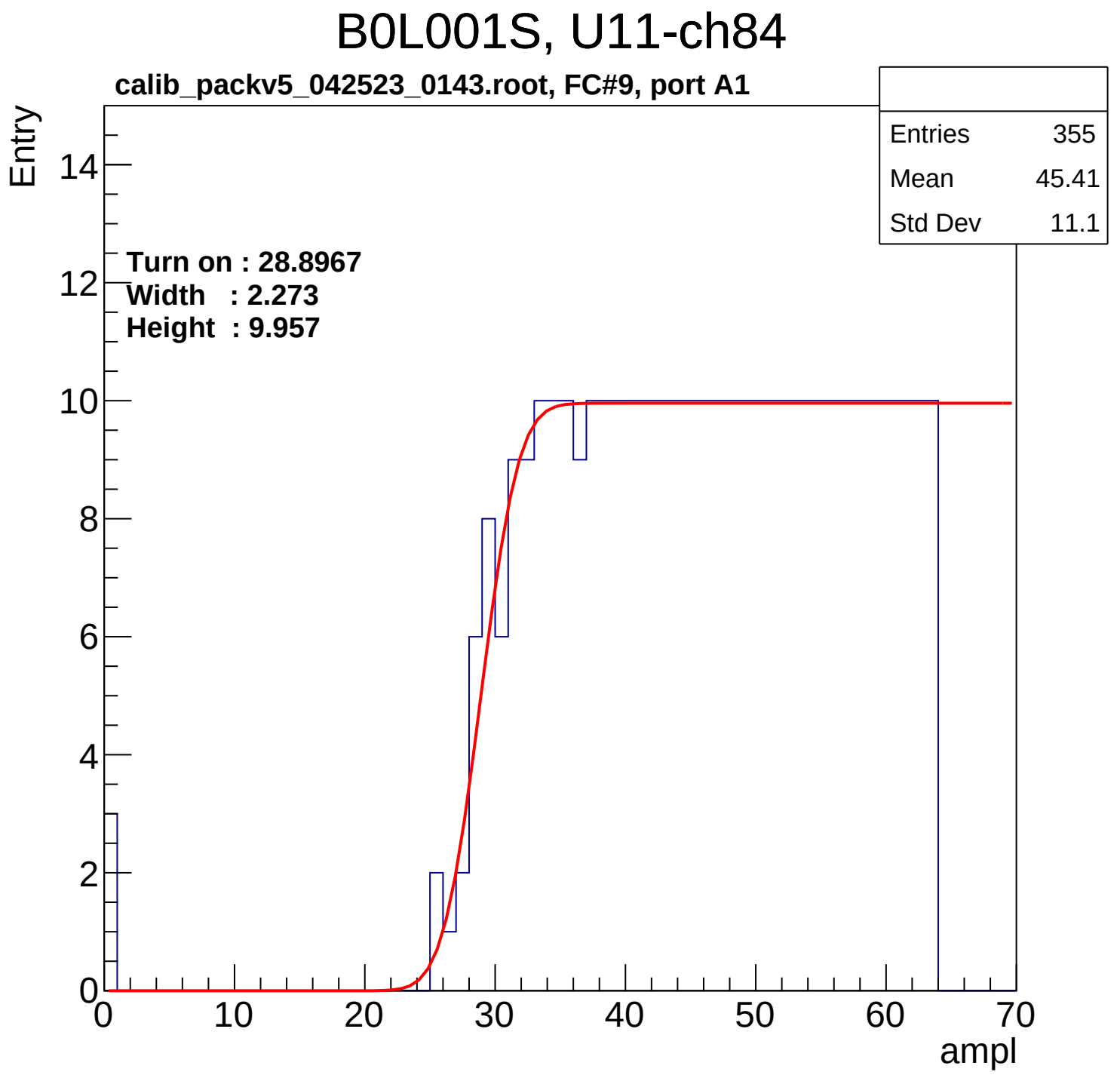
B0L001S, U11-ch84
calib_packv5_042523_0143.root, FC#9, port A1
Entries 355
Mean 45.41
Std Dev 11.1
Turn on : 28.8967
Width : 2.273
Height : 9.957
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ampl
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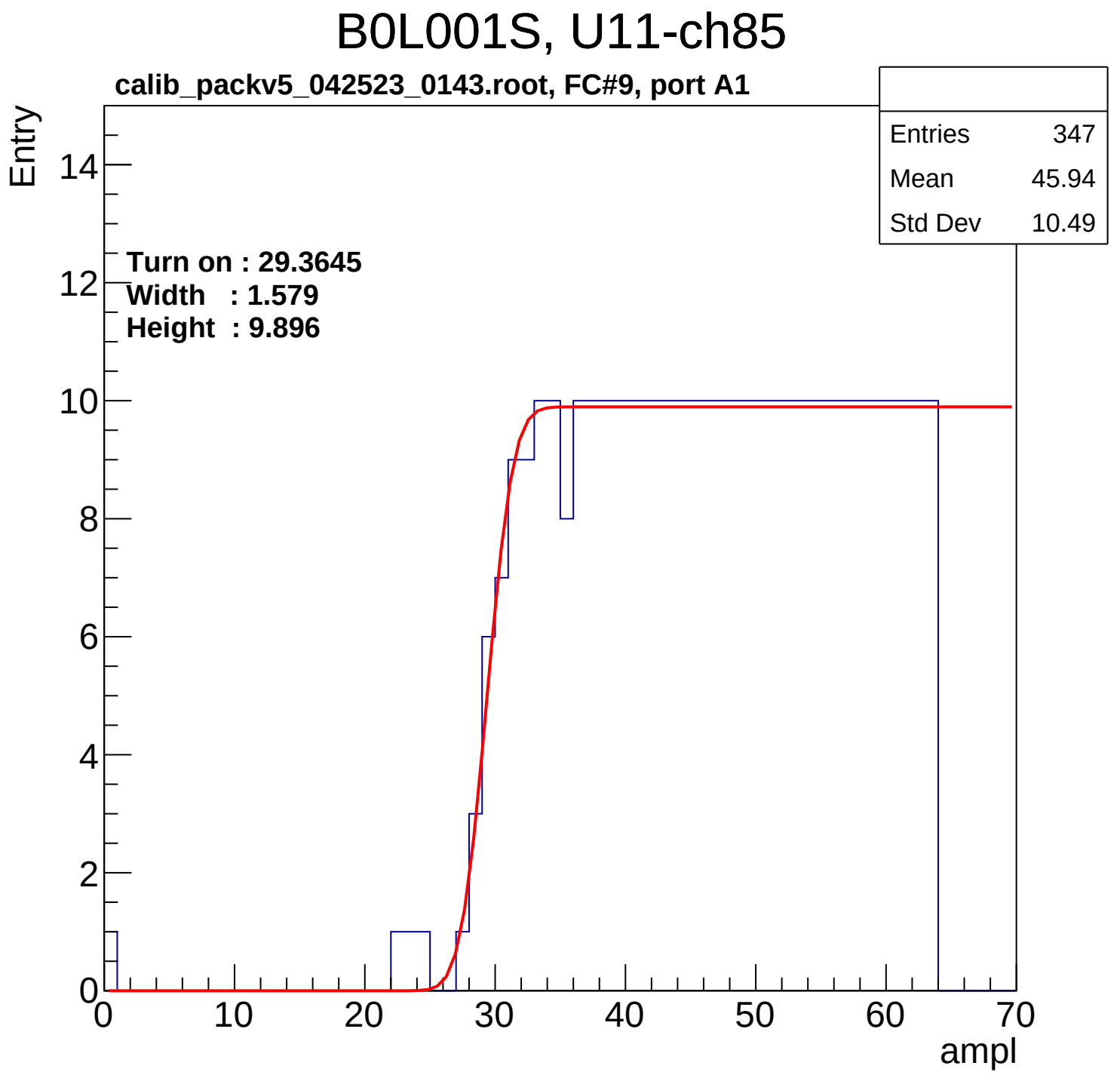
B0L001S, U11-ch85
calib_packv5_042523_0143.root, FC#9, port A1
Entries 347
Mean 45.94
Std Dev 10.49
Turn on : 29.3645
Width : 1.579
Height : 9.896
Entry
ampl
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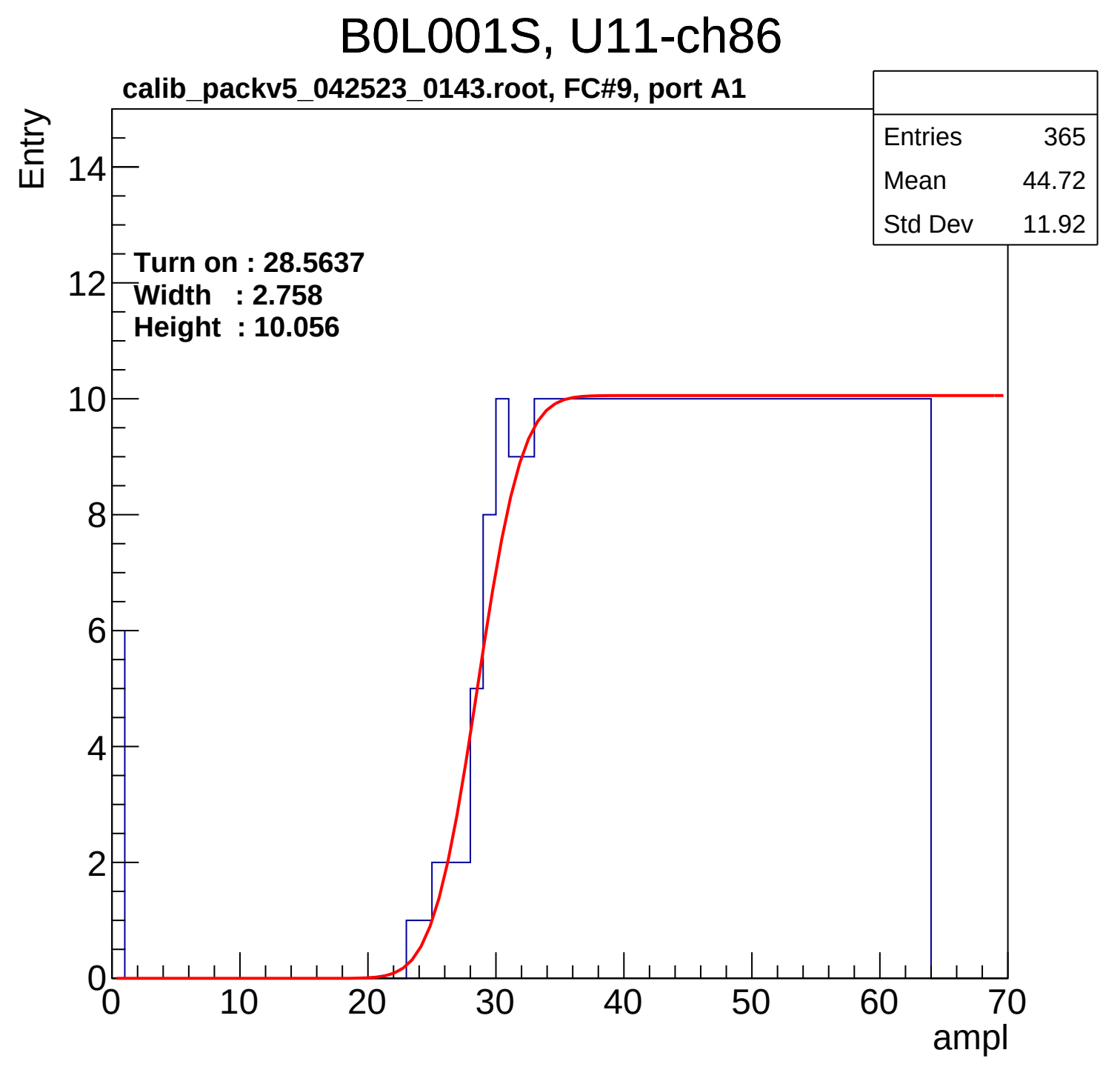
B0L001S, U11-ch86
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 44.72
Std Dev 11.92
Turn on : 28.5637
Width : 2.758
Height : 10.056
Entry
ampl
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2
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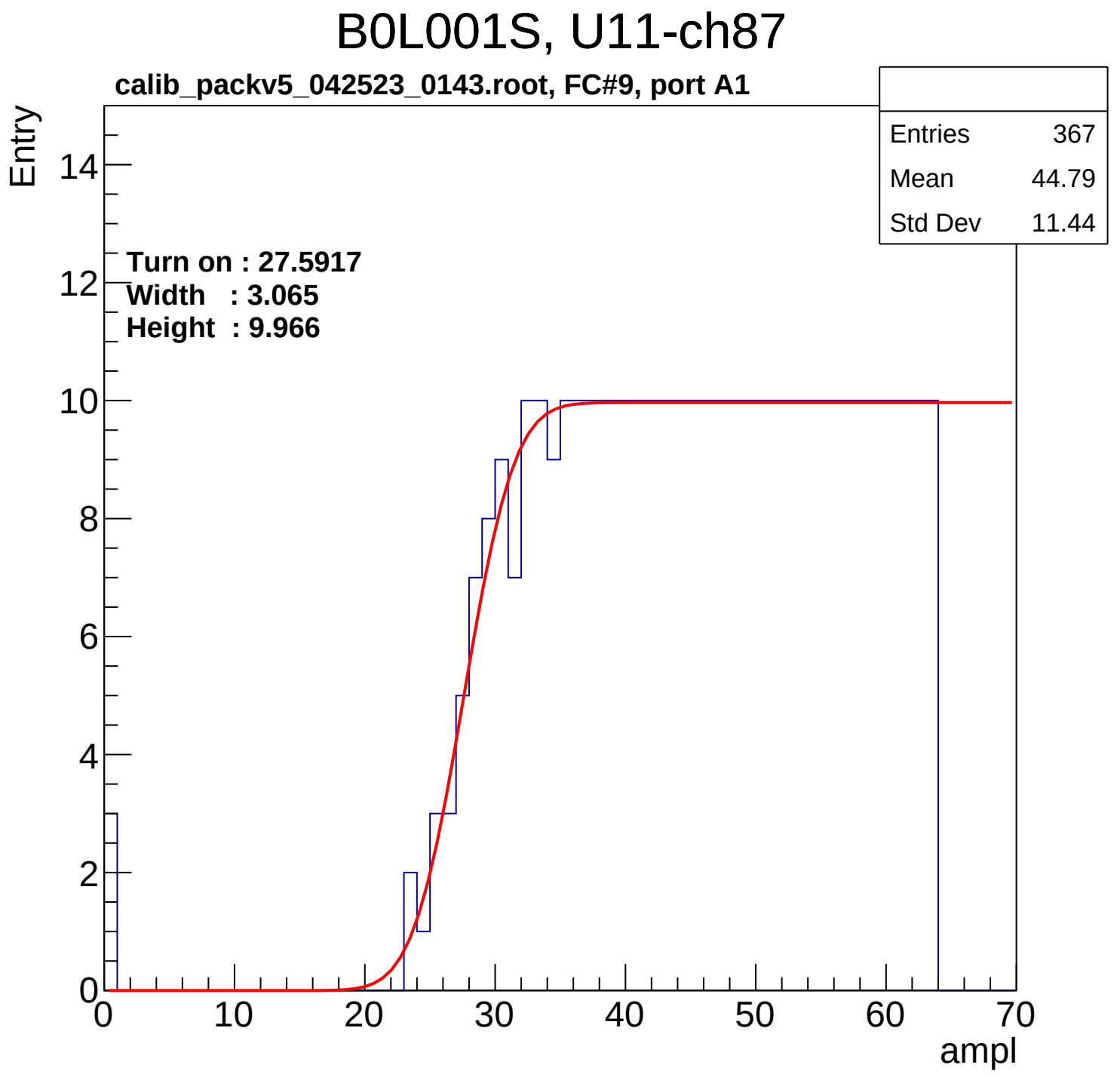
B0L001S, U11-ch87
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.79
Std Dev 11.44
Turn on : 27.5917
Width : 3.065
Height : 9.966
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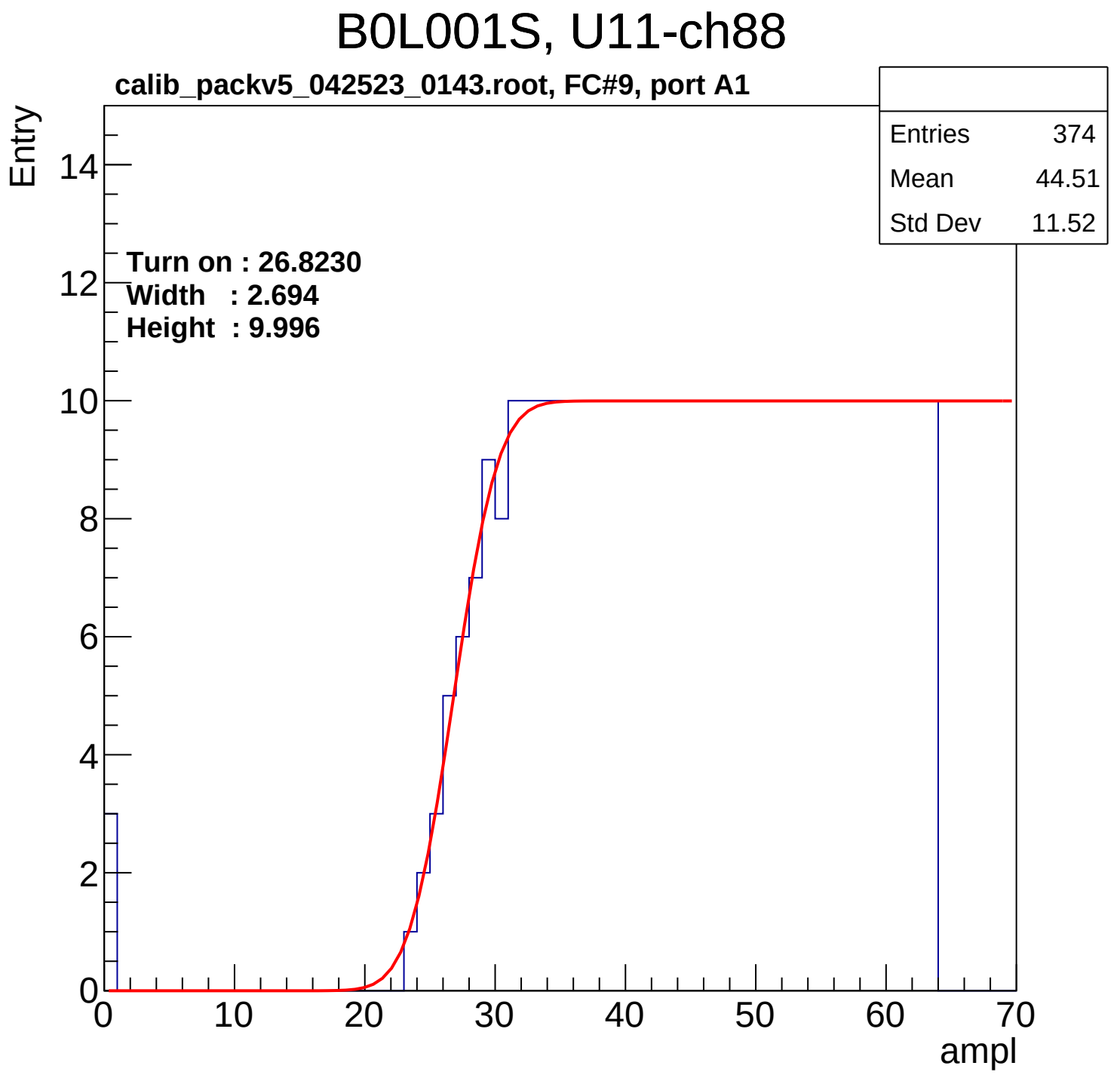
B0L001S, U11-ch88
calib_packv5_042523_0143.root, FC#9, port A1
Entries 374
Mean 44.51
Std Dev 11.52
Turn on : 26.8230
Width : 2.694
Height : 9.996
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ampl
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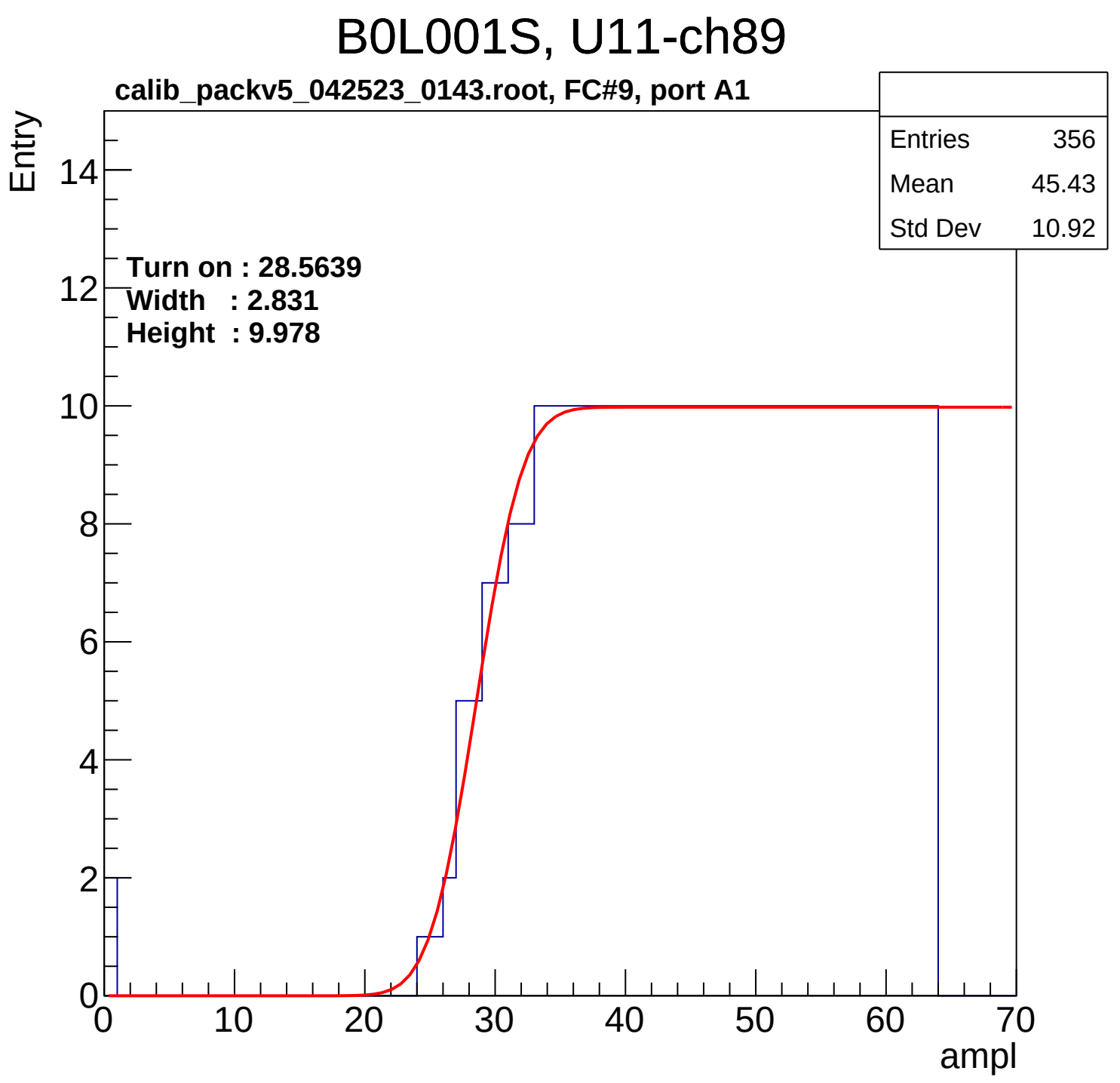
B0L001S, U11-ch89
calib_packv5_042523_0143.root, FC#9, port A1
Entries 356
Mean 45.43
Std Dev 10.92
Turn on : 28.5639
Width : 2.831
Height : 9.978
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ampl
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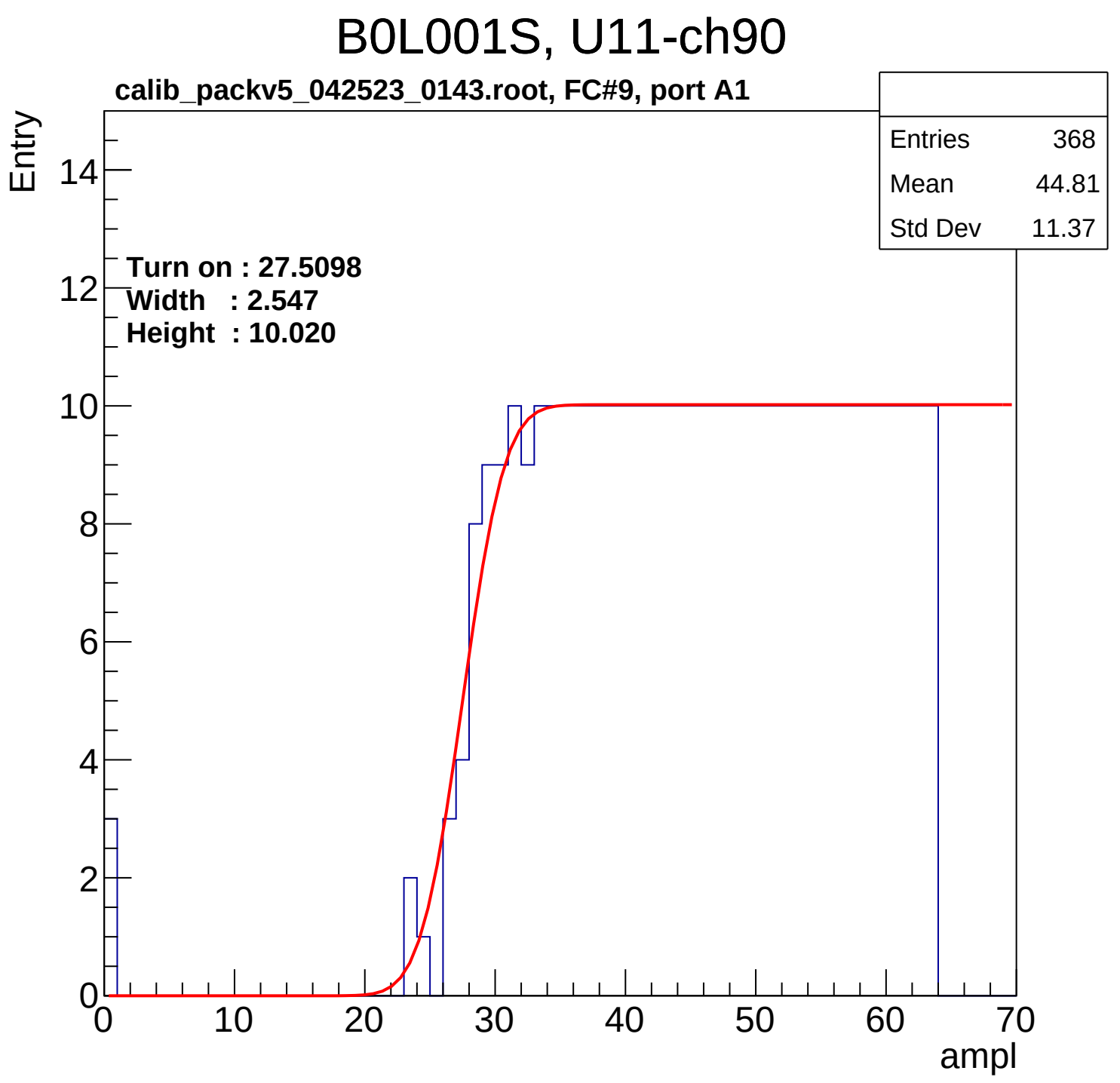
B0L001S, U11-ch90
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.81
Std Dev 11.37
Turn on : 27.5098
Width : 2.547
Height : 10.020
Entry
ampl
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6
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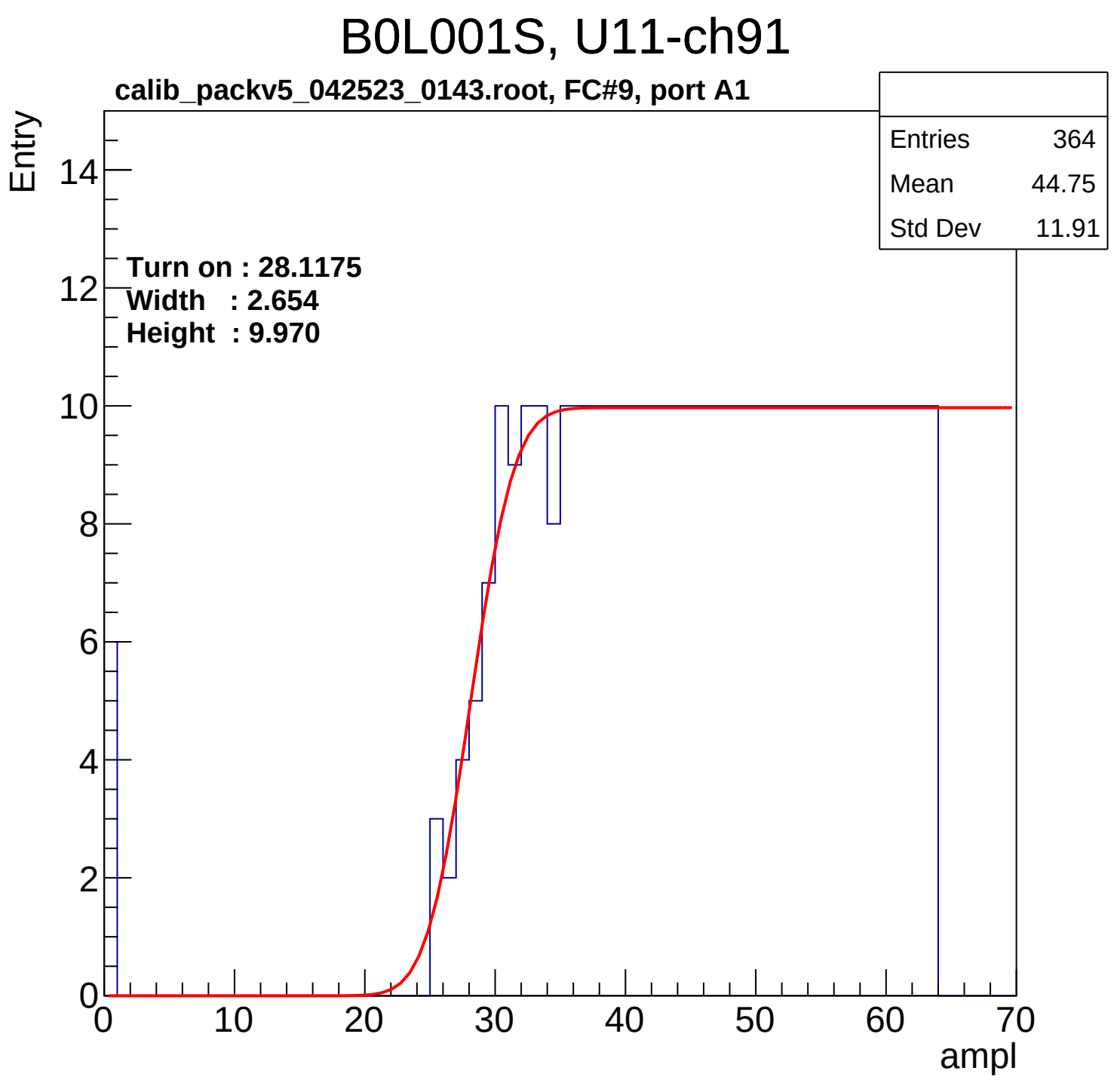
B0L001S, U11-ch91
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 44.75
Std Dev 11.91
Turn on : 28.1175
Width : 2.654
Height : 9.970
Entry
ampl
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6
8
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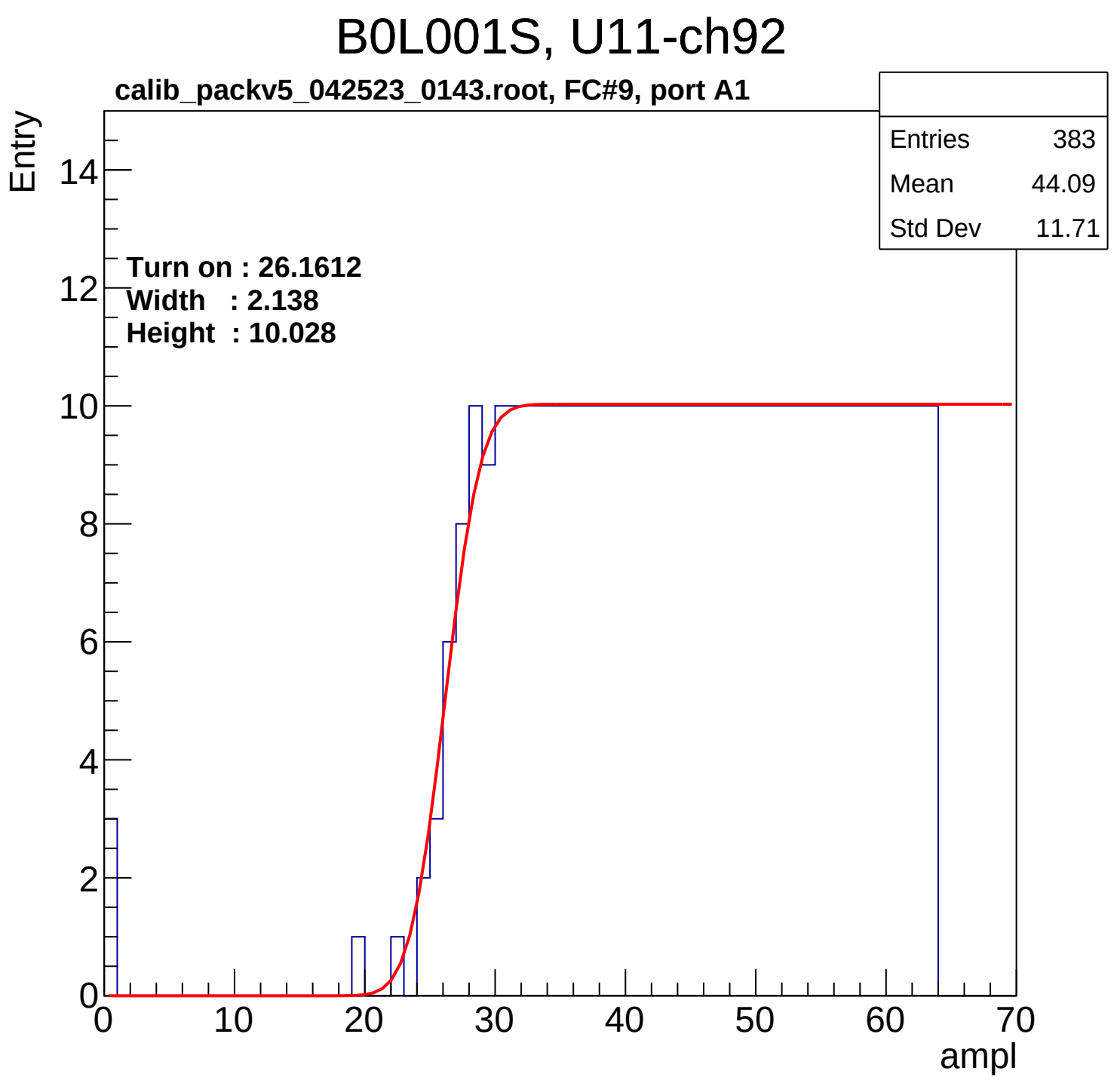
B0L001S, U11-ch92
calib_packv5_042523_0143.root, FC#9, port A1
Entries 383
Mean 44.09
Std Dev 11.71
Turn on : 26.1612
Width : 2.138
Height : 10.028
Entry
ampl
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2
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6
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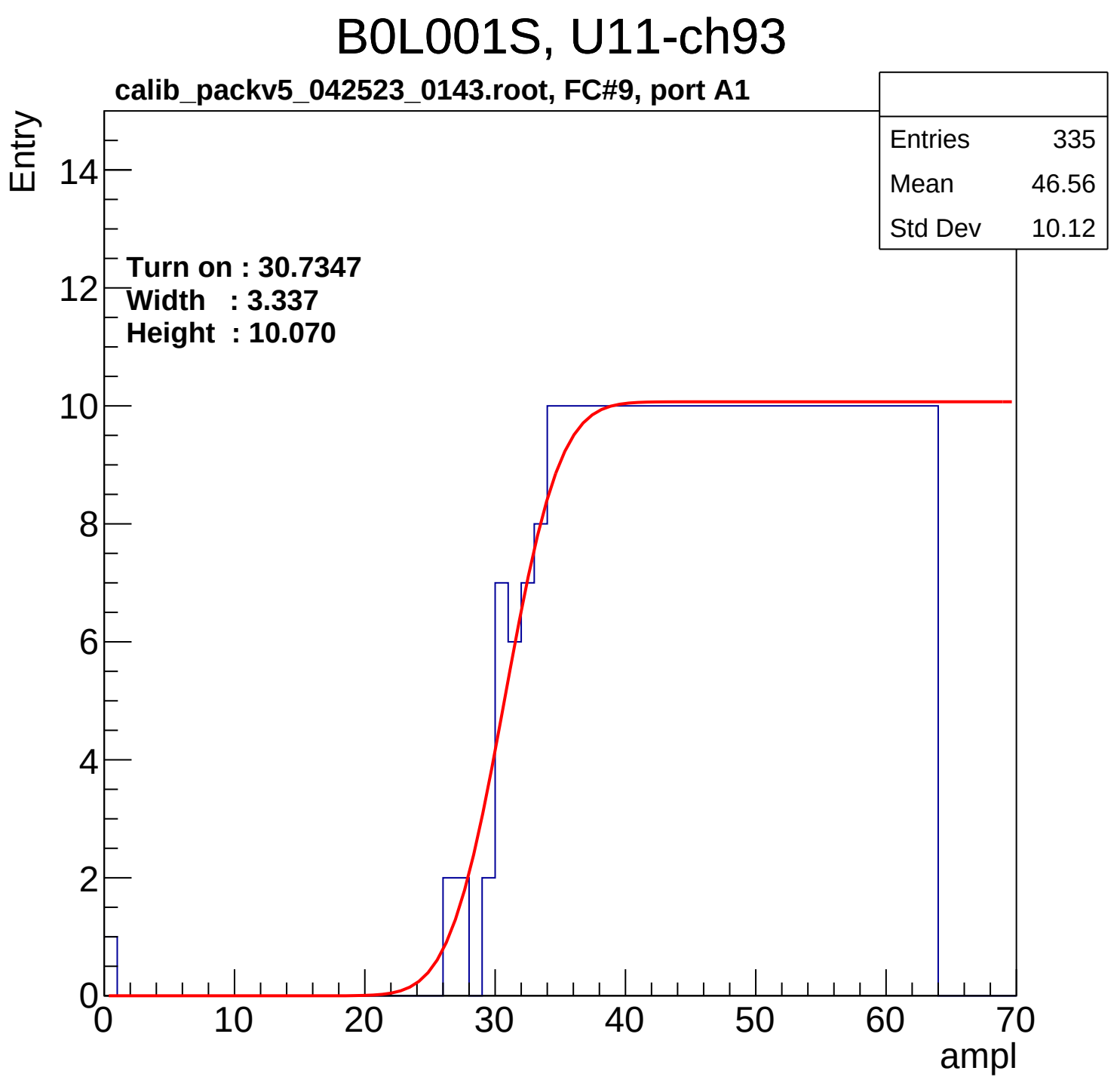
B0L001S, U11-ch93
calib_packv5_042523_0143.root, FC#9, port A1
Entries 335
Mean 46.56
Std Dev 10.12
Turn on : 30.7347
Width : 3.337
Height : 10.070
Entry
ampl
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6
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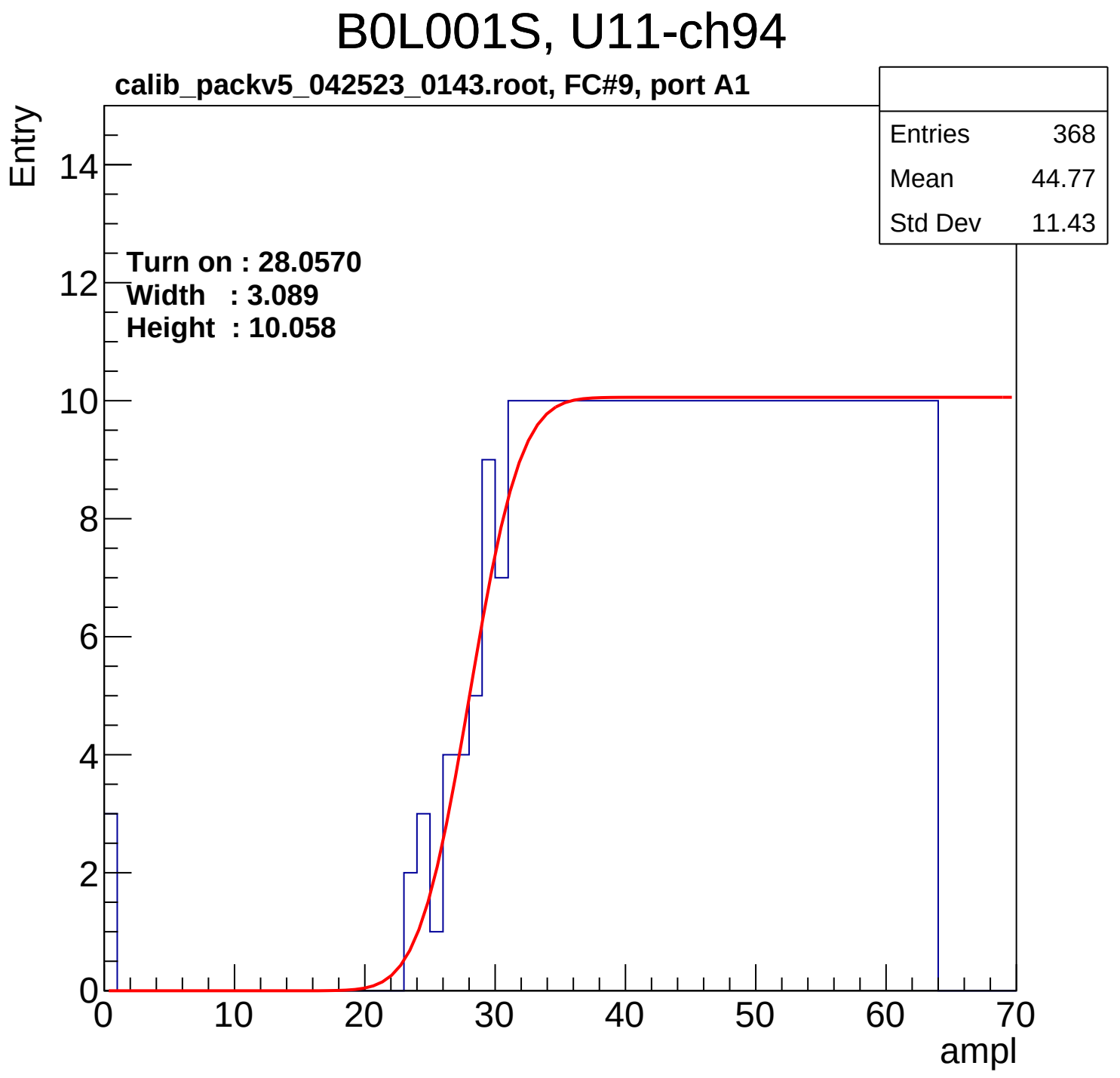
B0L001S, U11-ch94
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.77
Std Dev 11.43
Turn on : 28.0570
Width : 3.089
Height : 10.058
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
30
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60
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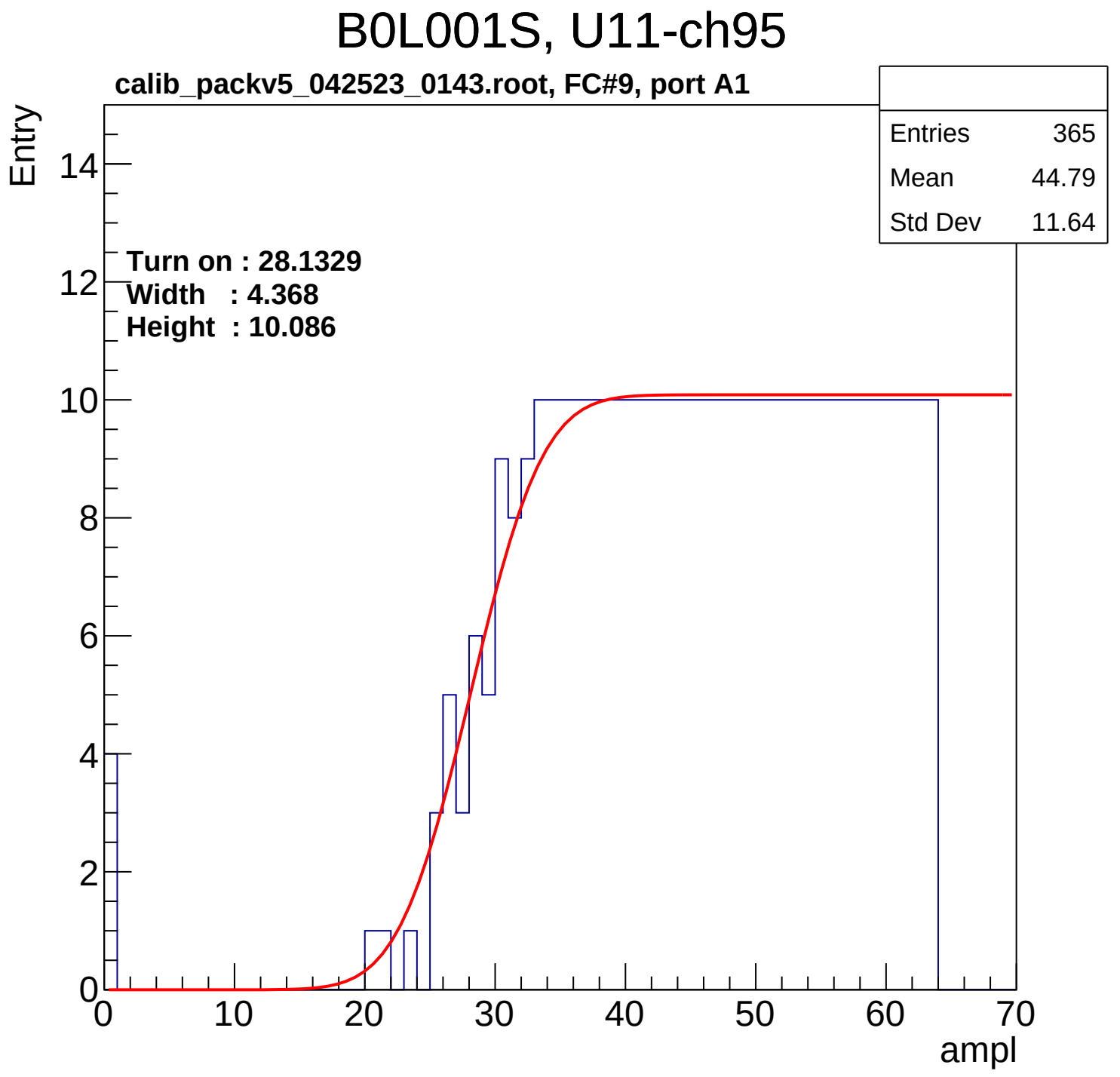
B0L001S, U11-ch95
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 44.79
Std Dev 11.64
Turn on : 28.1329
Width : 4.368
Height : 10.086
Entry
ampl
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6
8
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12
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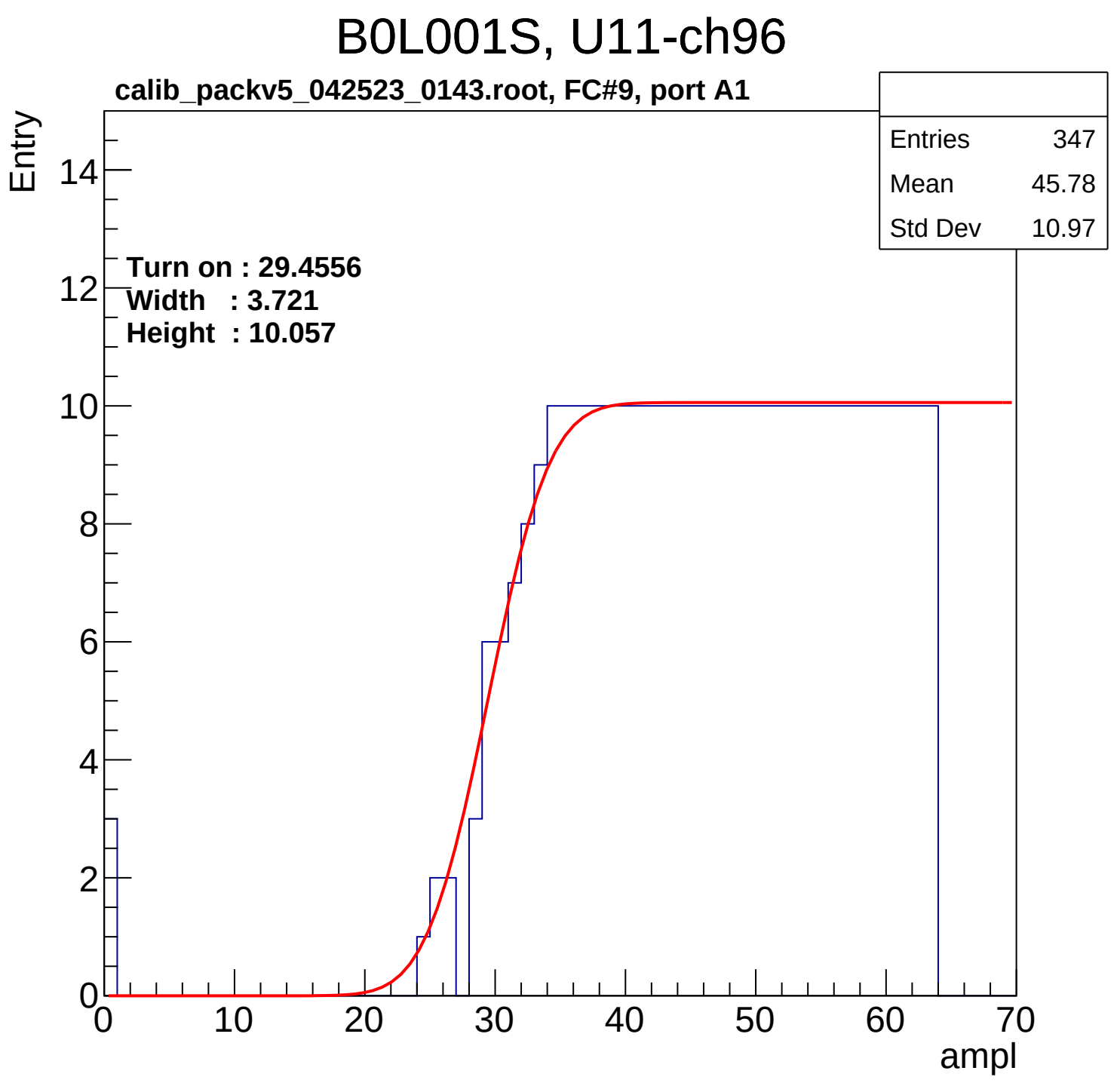
B0L001S, U11-ch96
calib_packv5_042523_0143.root, FC#9, port A1
Entries 347
Mean 45.78
Std Dev 10.97
Turn on : 29.4556
Width : 3.721
Height : 10.057
Entry
ampl
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6
8
10
12
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20
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60
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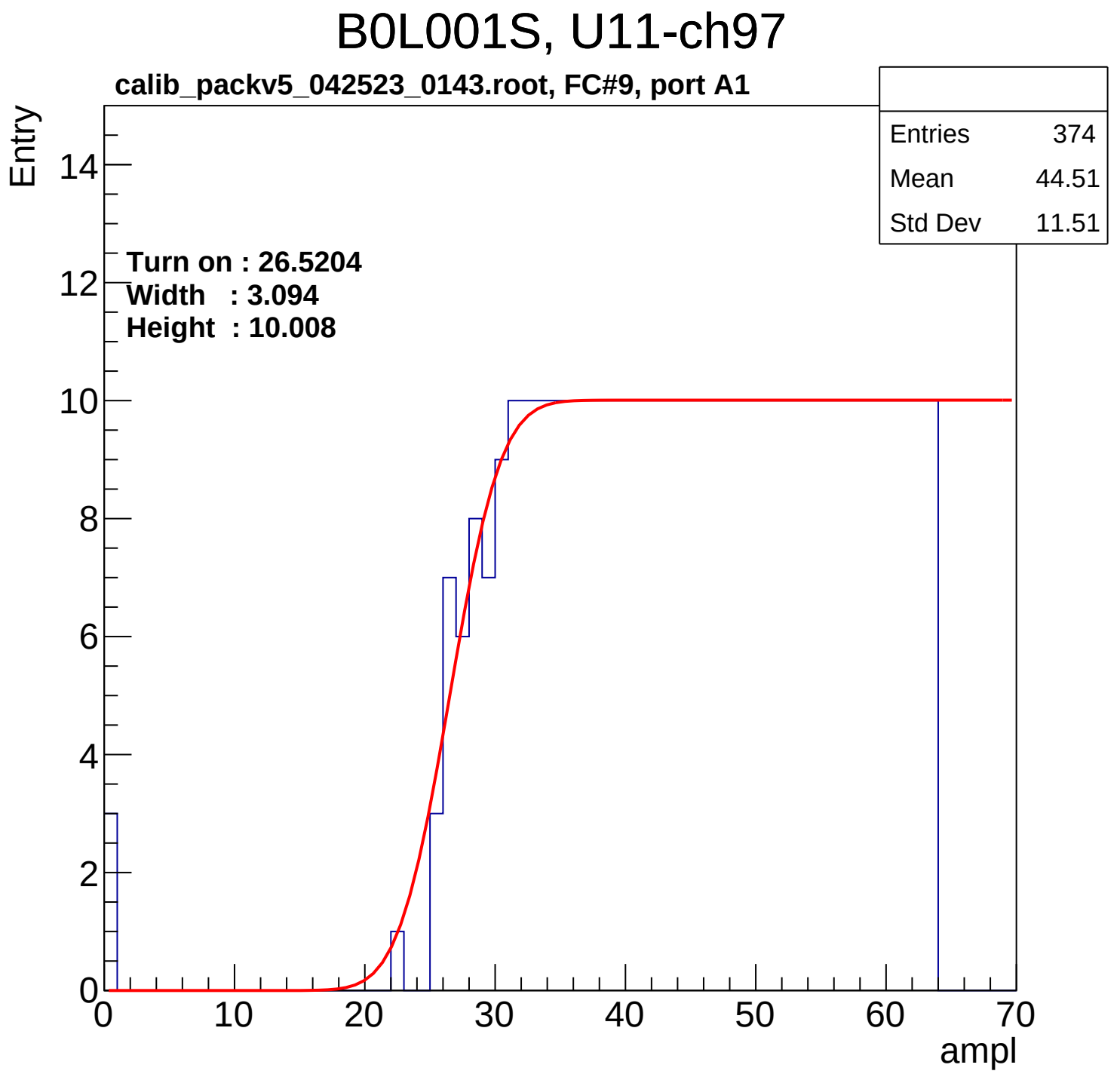
B0L001S, U11-ch97
calib_packv5_042523_0143.root, FC#9, port A1
Entries 374
Mean 44.51
Std Dev 11.51
Turn on : 26.5204
Width : 3.094
Height : 10.008
Entry
ampl
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6
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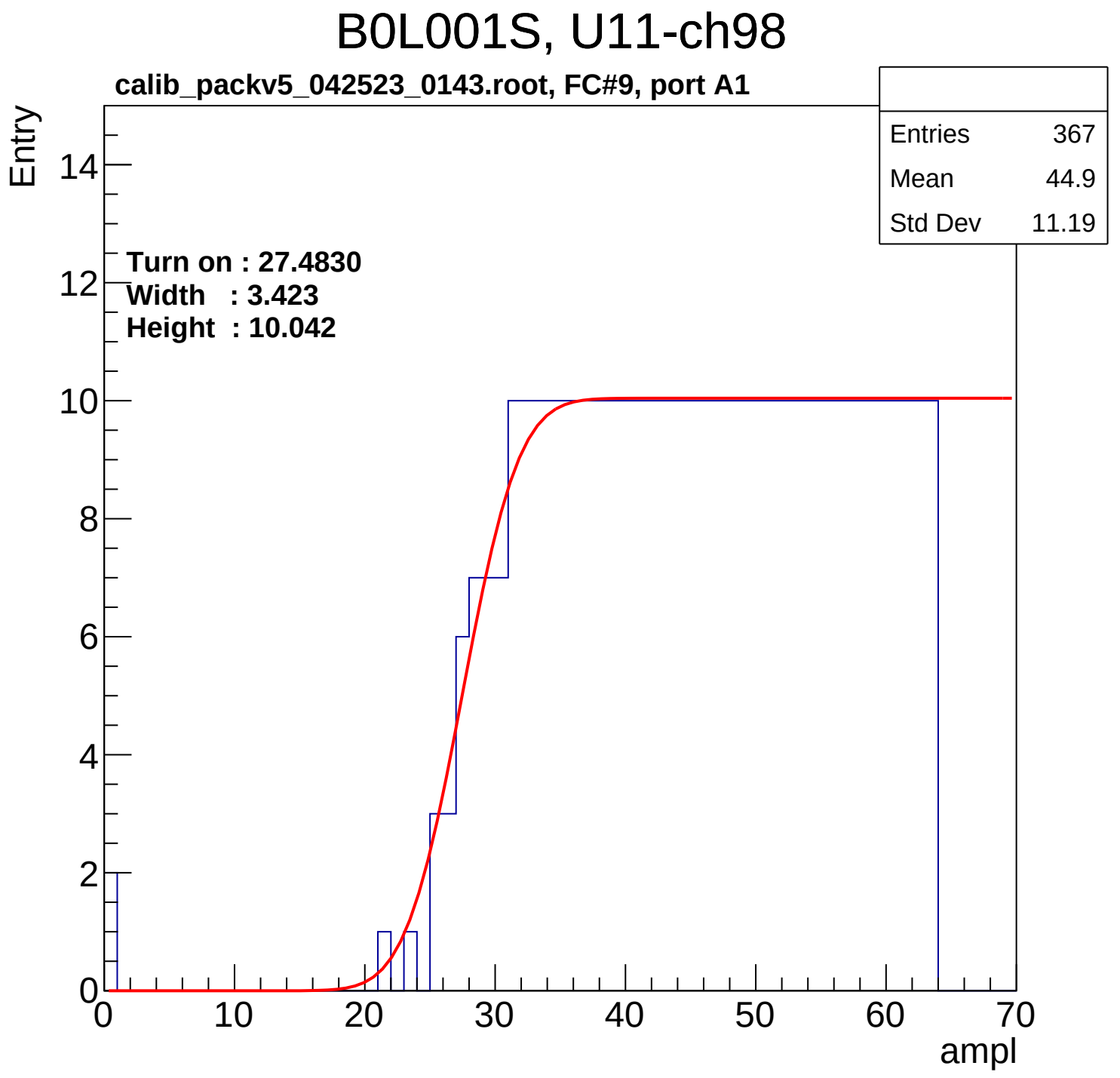
B0L001S, U11-ch98
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.9
Std Dev 11.19
Turn on : 27.4830
Width : 3.423
Height : 10.042
Entry
ampl
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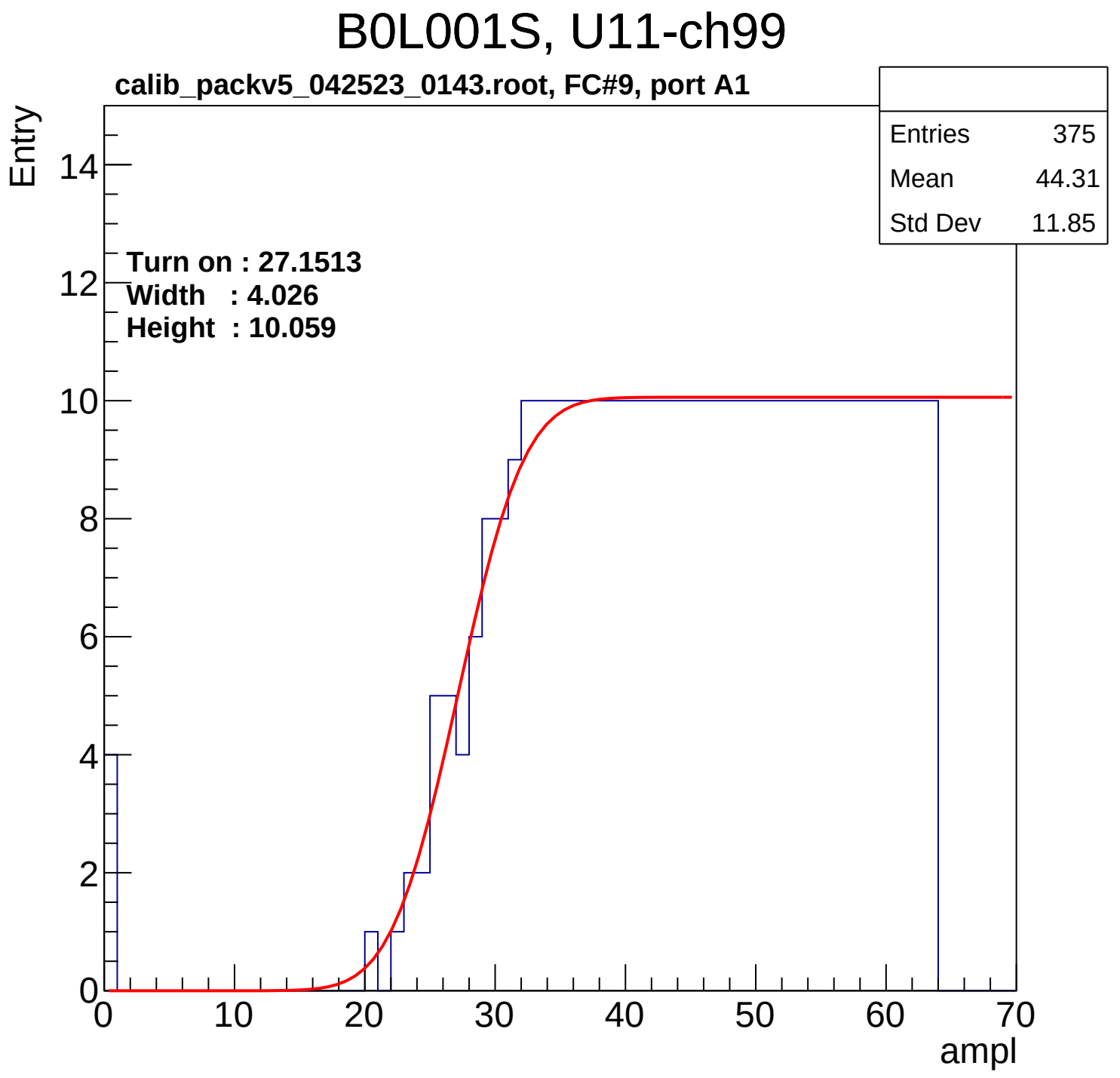
B0L001S, U11-ch99
calib_packv5_042523_0143.root, FC#9, port A1
Entries 375
Mean 44.31
Std Dev 11.85
Turn on : 27.1513
Width : 4.026
Height : 10.059
Entry
ampl
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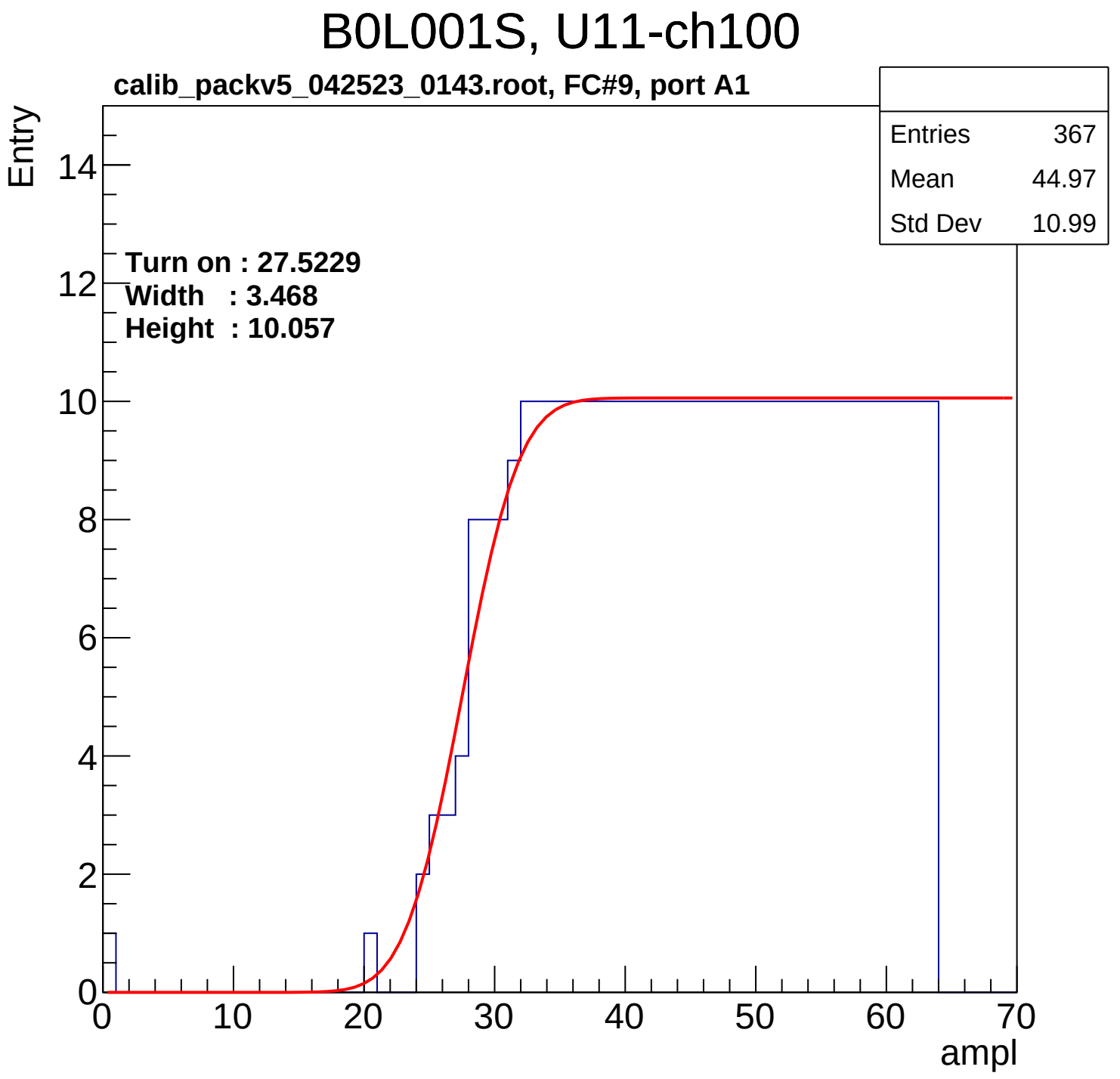
B0L001S, U11-ch100
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.97
Std Dev 10.99
Turn on : 27.5229
Width : 3.468
Height : 10.057
Entry
ampl
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2
4
6
8
10
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60
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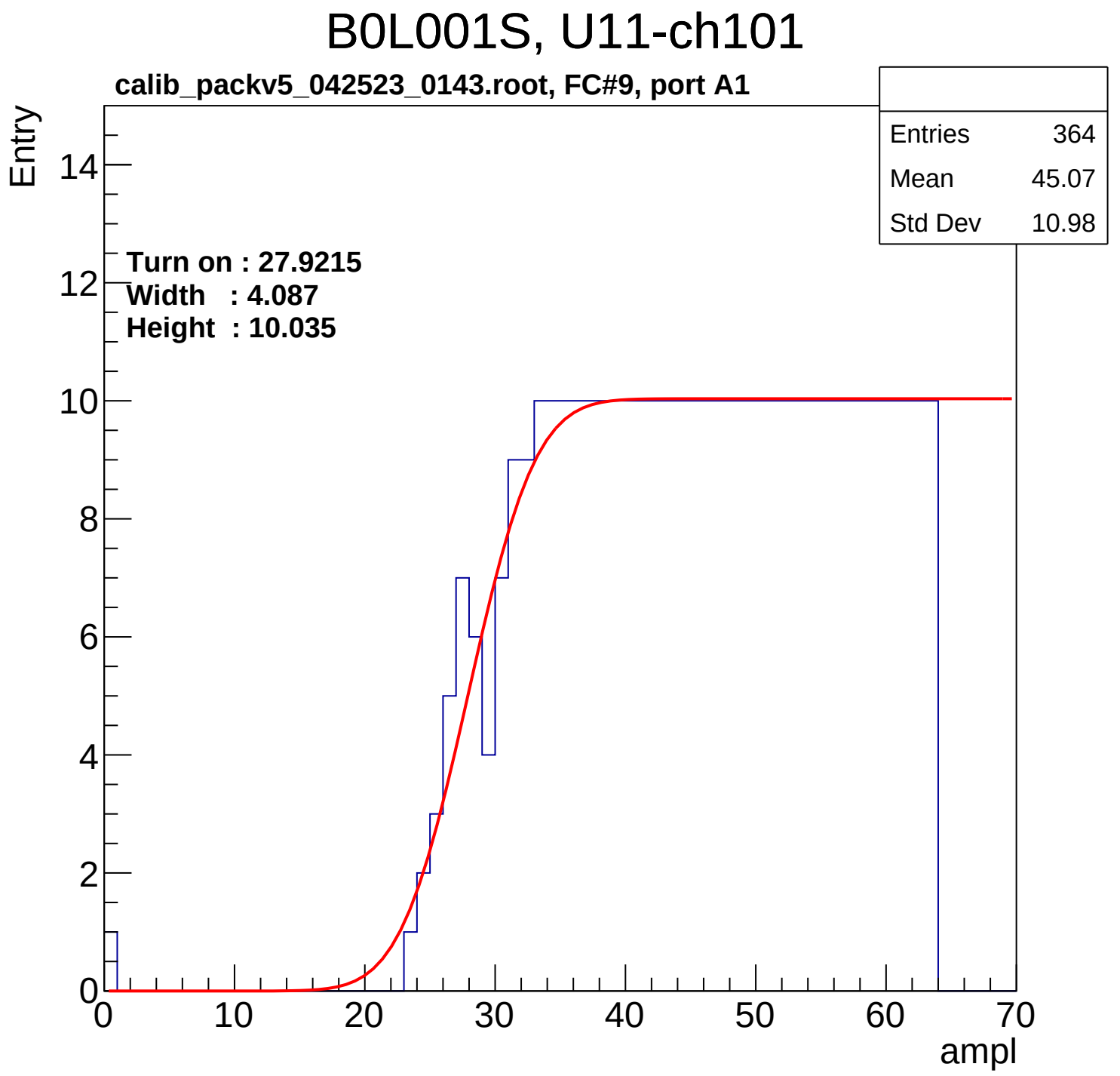
B0L001S, U11-ch101
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 45.07
Std Dev 10.98
Turn on : 27.9215
Width : 4.087
Height : 10.035
Entry
ampl
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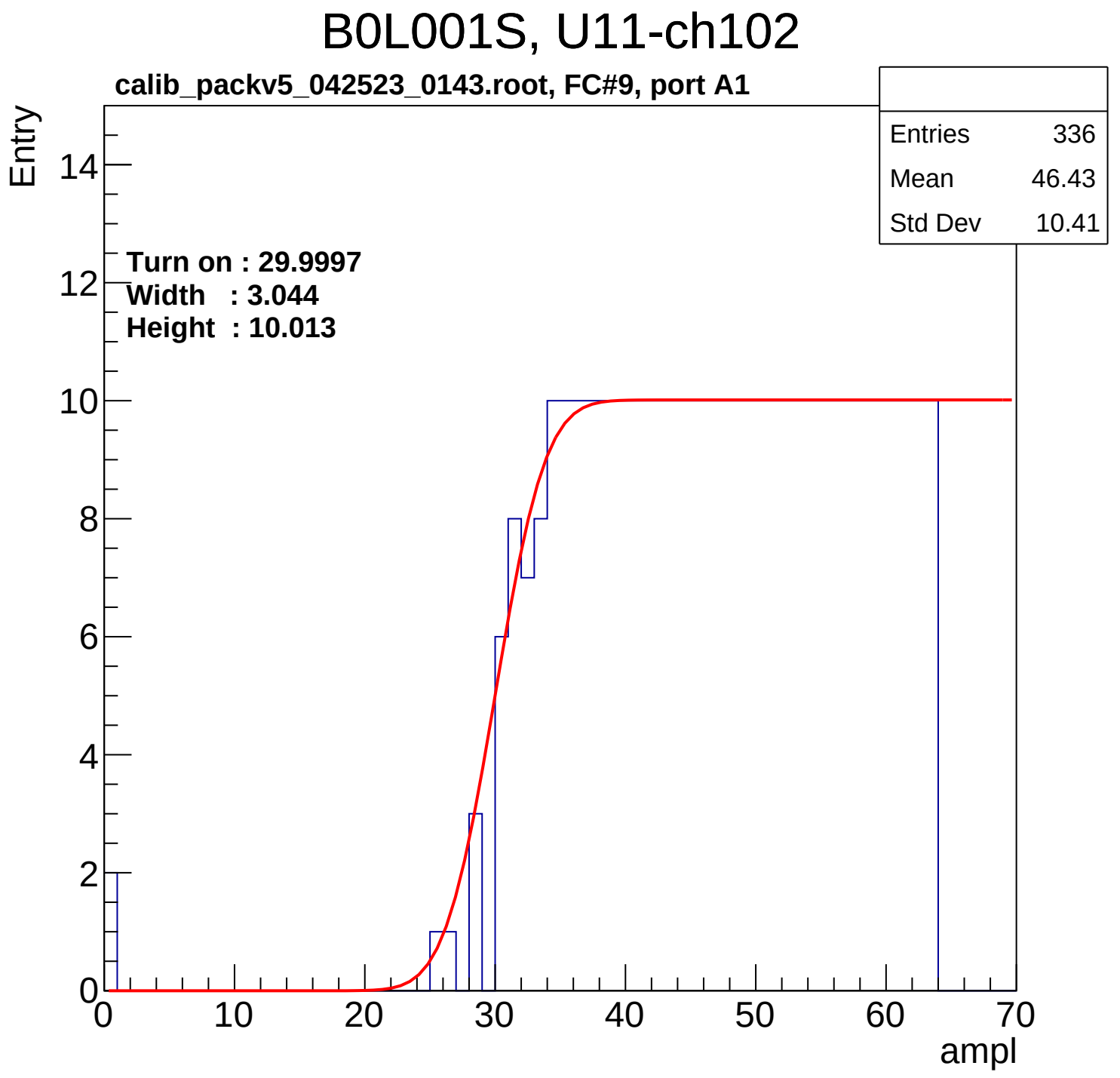
B0L001S, U11-ch102
calib_packv5_042523_0143.root, FC#9, port A1
Entries 336
Mean 46.43
Std Dev 10.41
Turn on : 29.9997
Width : 3.044
Height : 10.013
Entry
ampl
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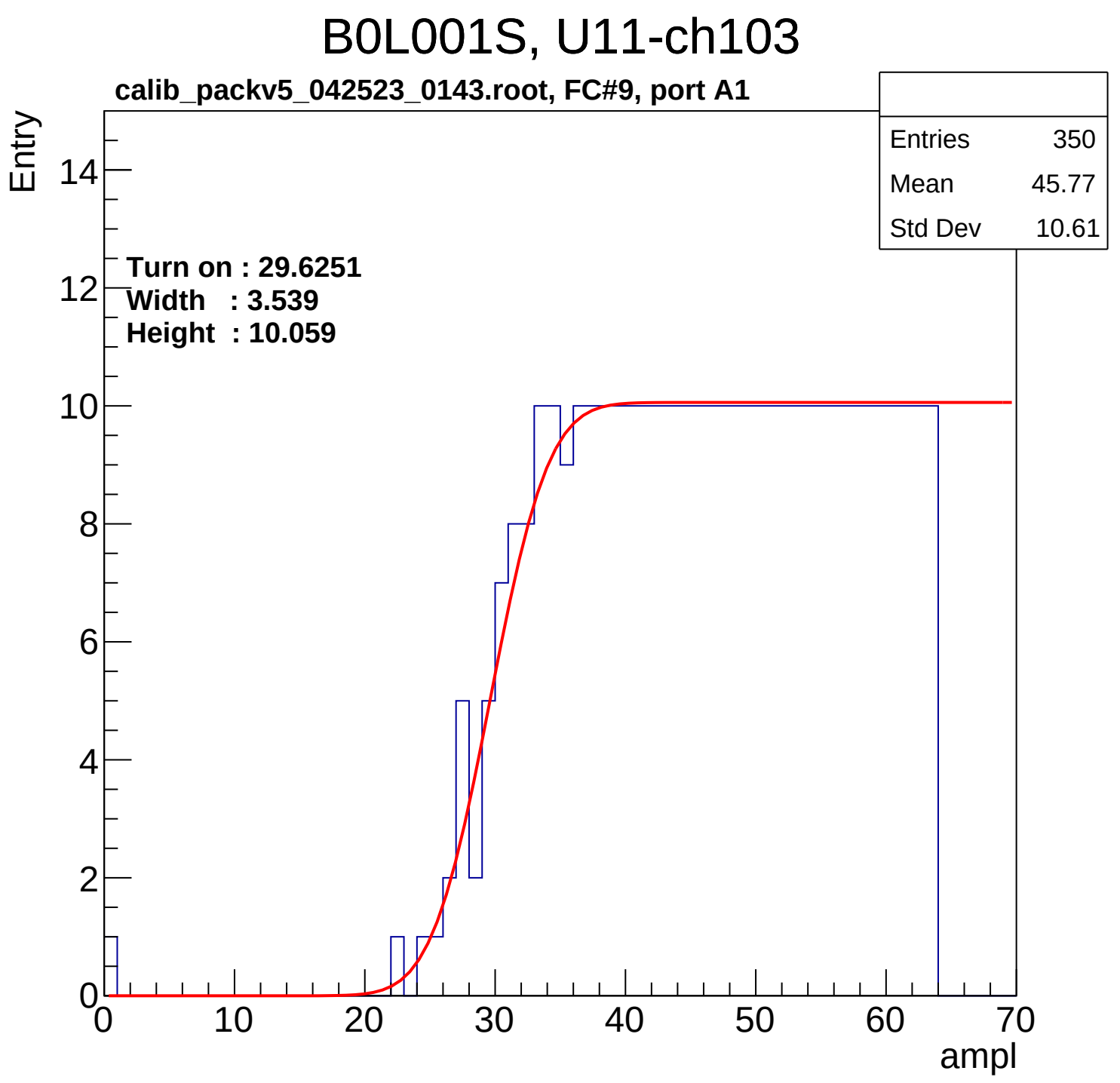
B0L001S, U11-ch103
calib_packv5_042523_0143.root, FC#9, port A1
Entries 350
Mean 45.77
Std Dev 10.61
Turn on : 29.6251
Width : 3.539
Height : 10.059
Entry
ampl
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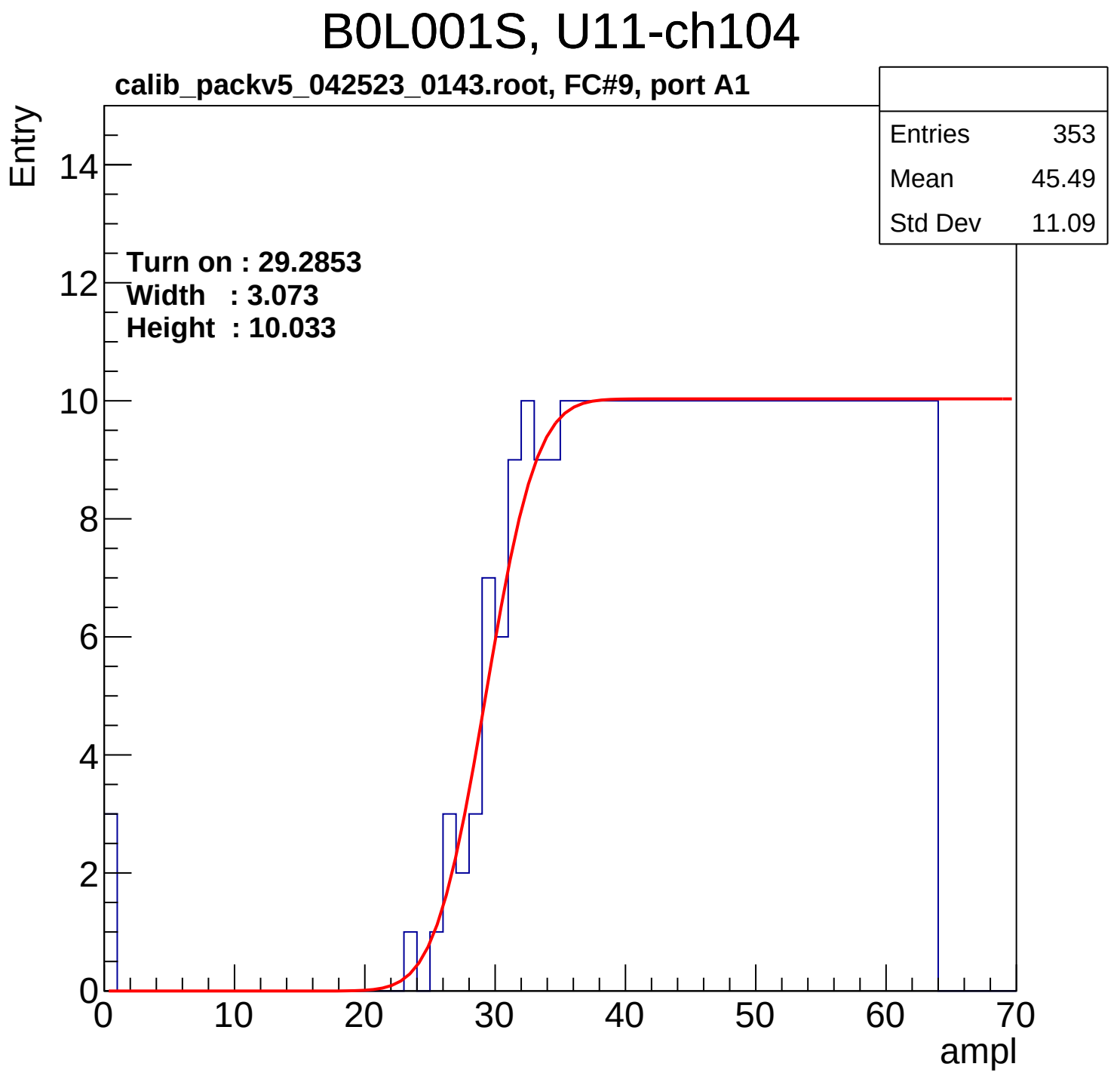
B0L001S, U11-ch104
calib_packv5_042523_0143.root, FC#9, port A1
Entries 353
Mean 45.49
Std Dev 11.09
Turn on : 29.2853
Width : 3.073
Height : 10.033
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ampl
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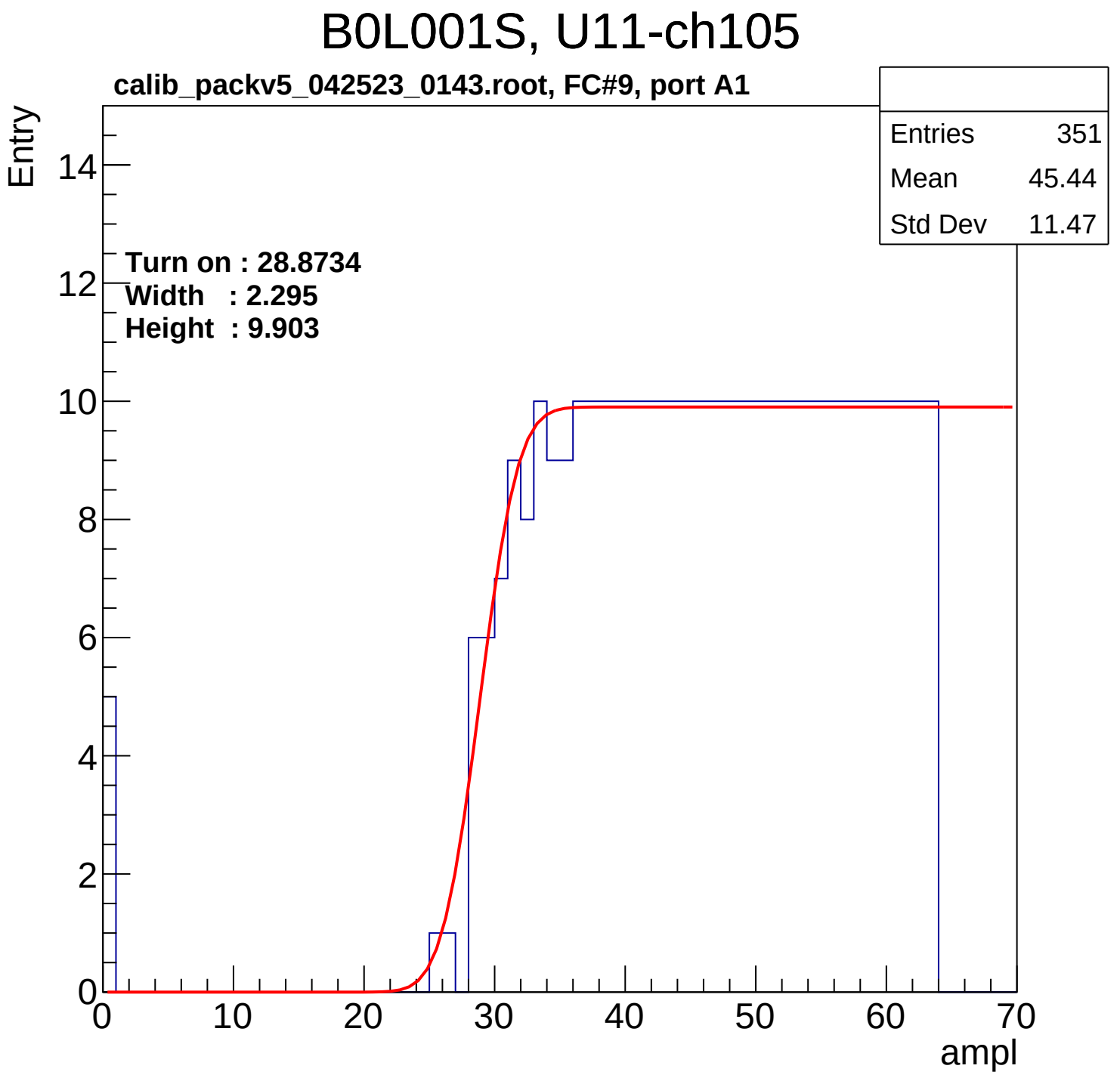
B0L001S, U11-ch105
calib_packv5_042523_0143.root, FC#9, port A1
Entries 351
Mean 45.44
Std Dev 11.47
Turn on : 28.8734
Width : 2.295
Height : 9.903
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ampl
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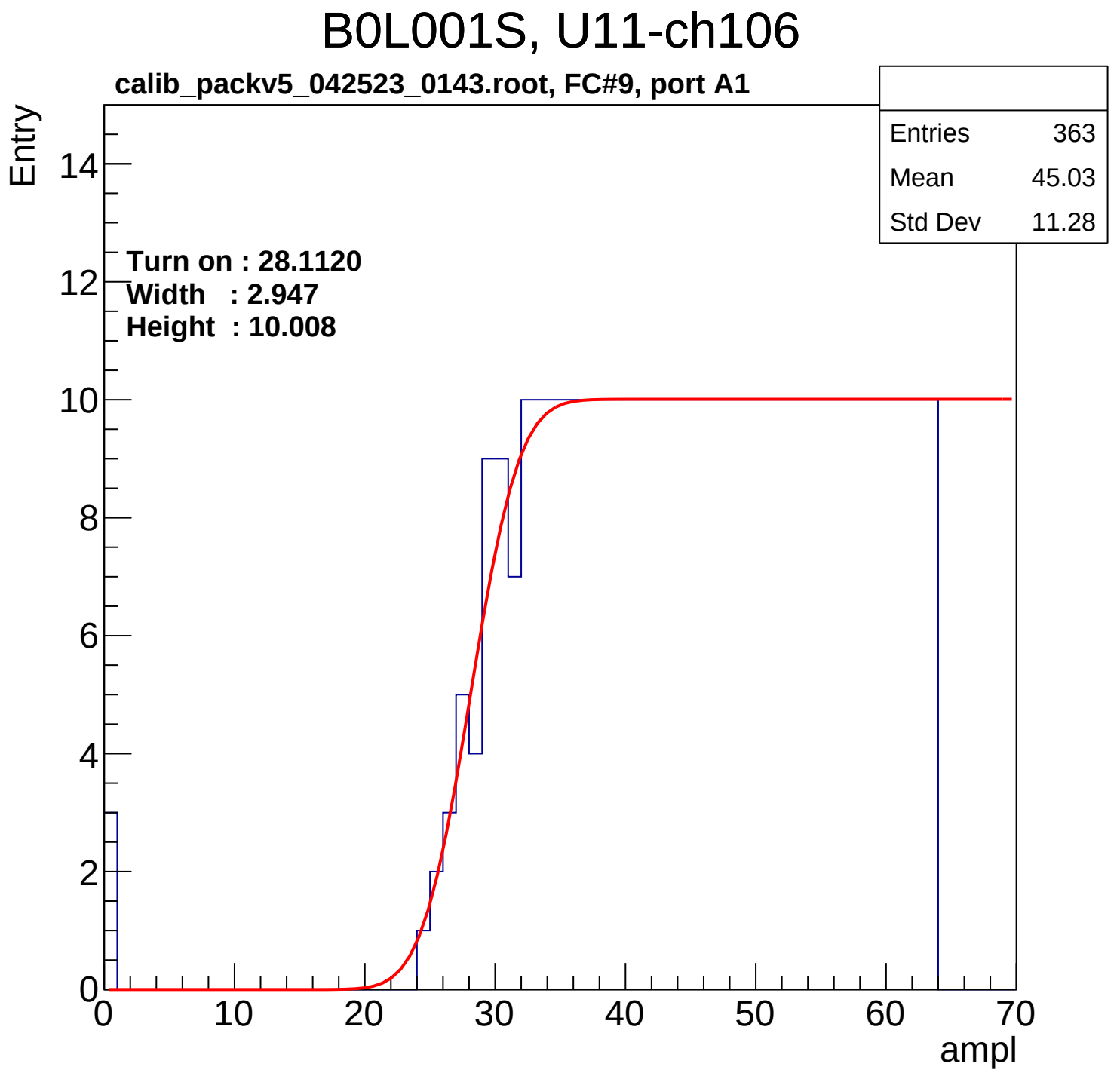
B0L001S, U11-ch106
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 45.03
Std Dev 11.28
Turn on : 28.1120
Width : 2.947
Height : 10.008
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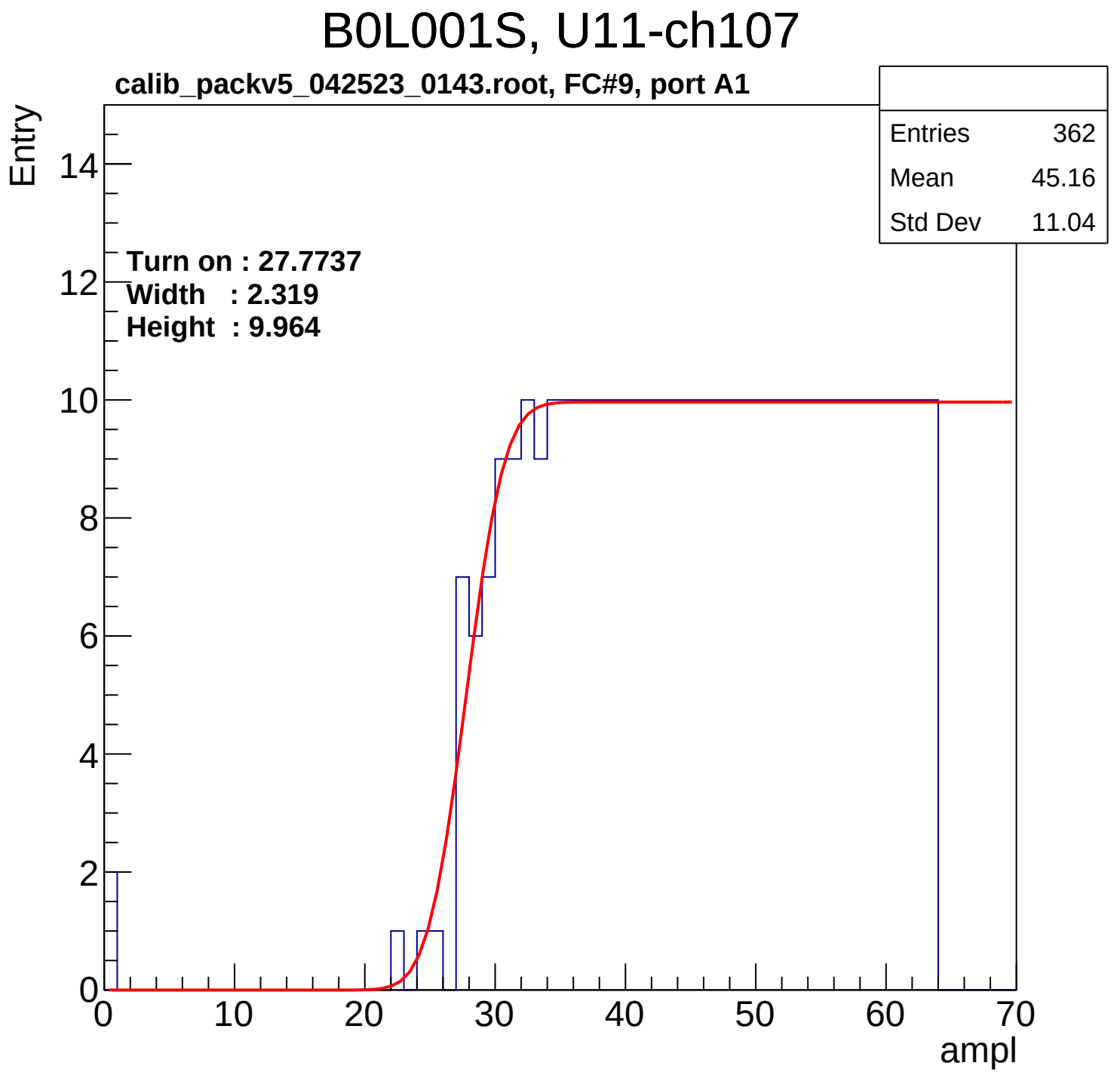
B0L001S, U11-ch107
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 45.16
Std Dev 11.04
Turn on : 27.7737
Width : 2.319
Height : 9.964
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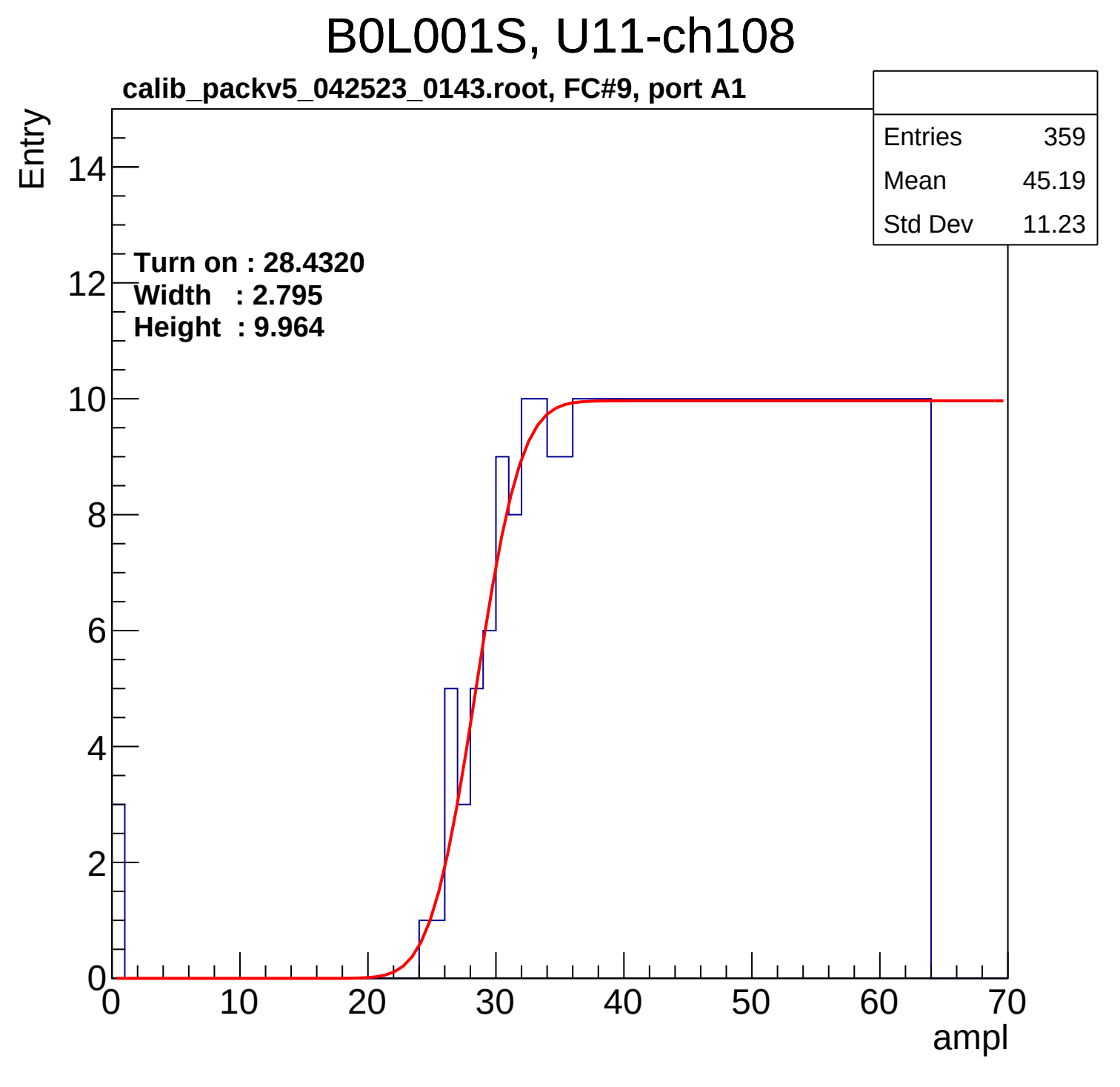
B0L001S, U11-ch108
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 45.19
Std Dev 11.23
Turn on : 28.4320
Width : 2.795
Height : 9.964
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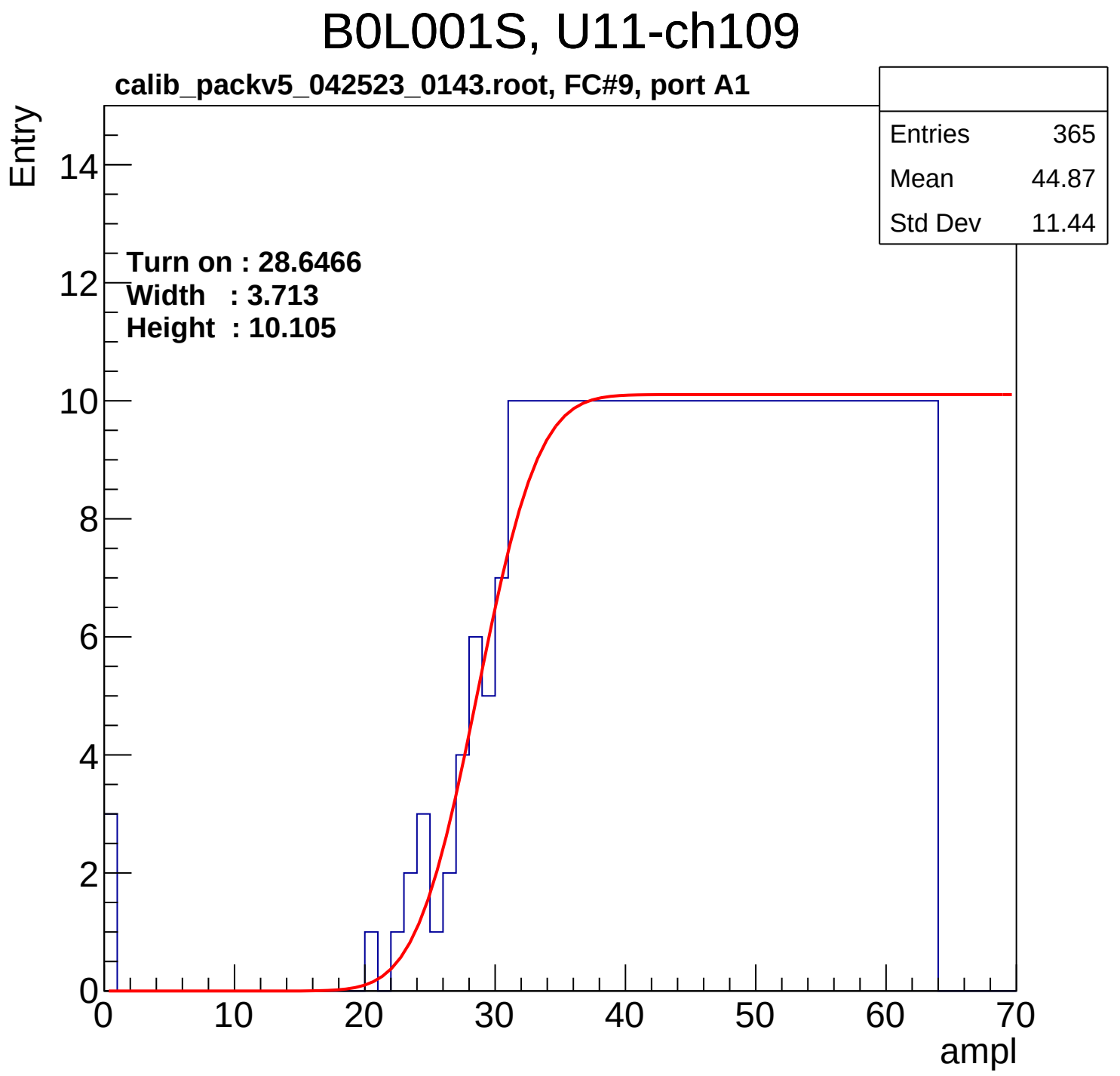
B0L001S, U11-ch109
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 44.87
Std Dev 11.44
Turn on : 28.6466
Width : 3.713
Height : 10.105
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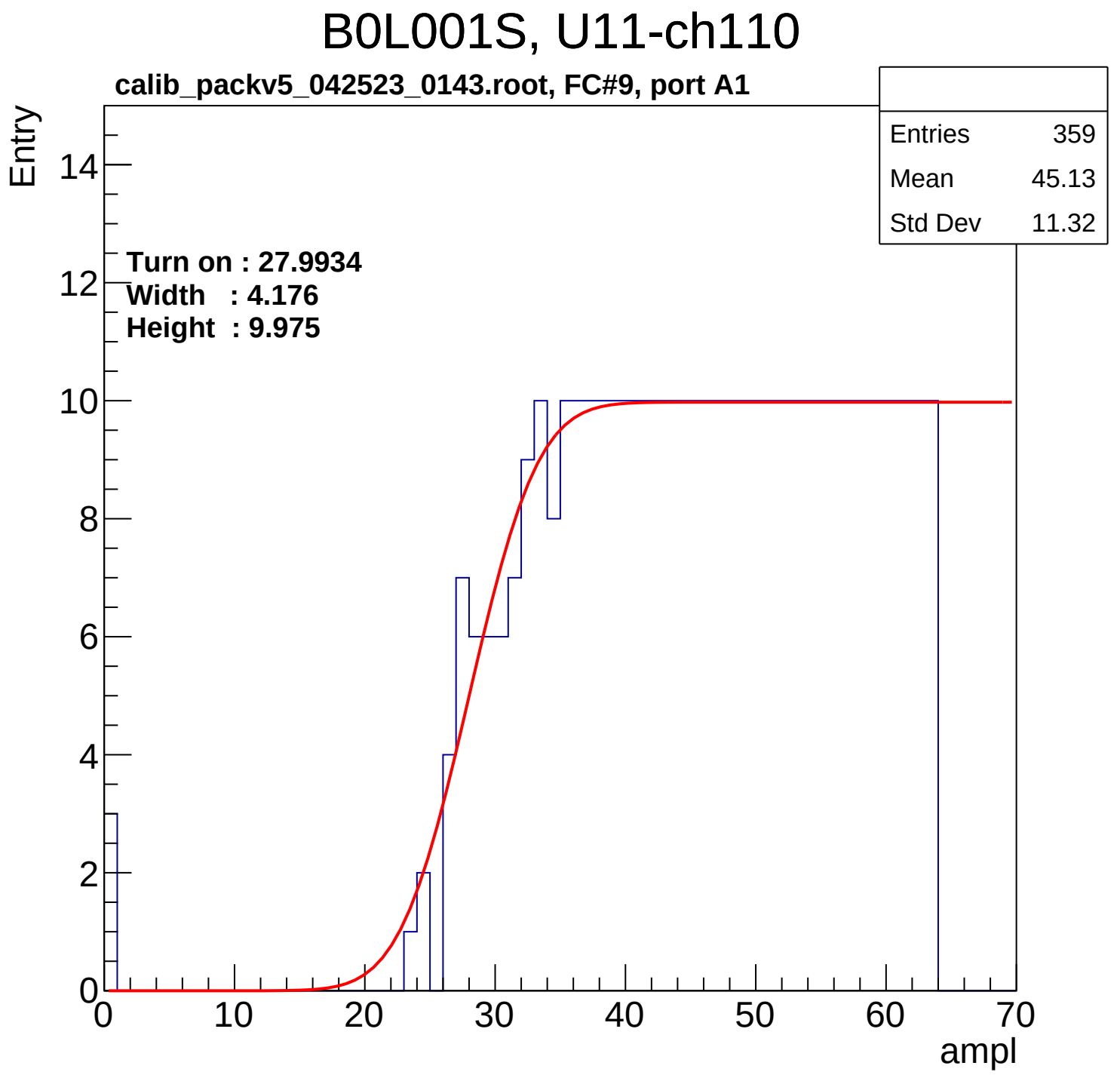
B0L001S, U11-ch110
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 45.13
Std Dev 11.32
Turn on : 27.9934
Width : 4.176
Height : 9.975
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ampl
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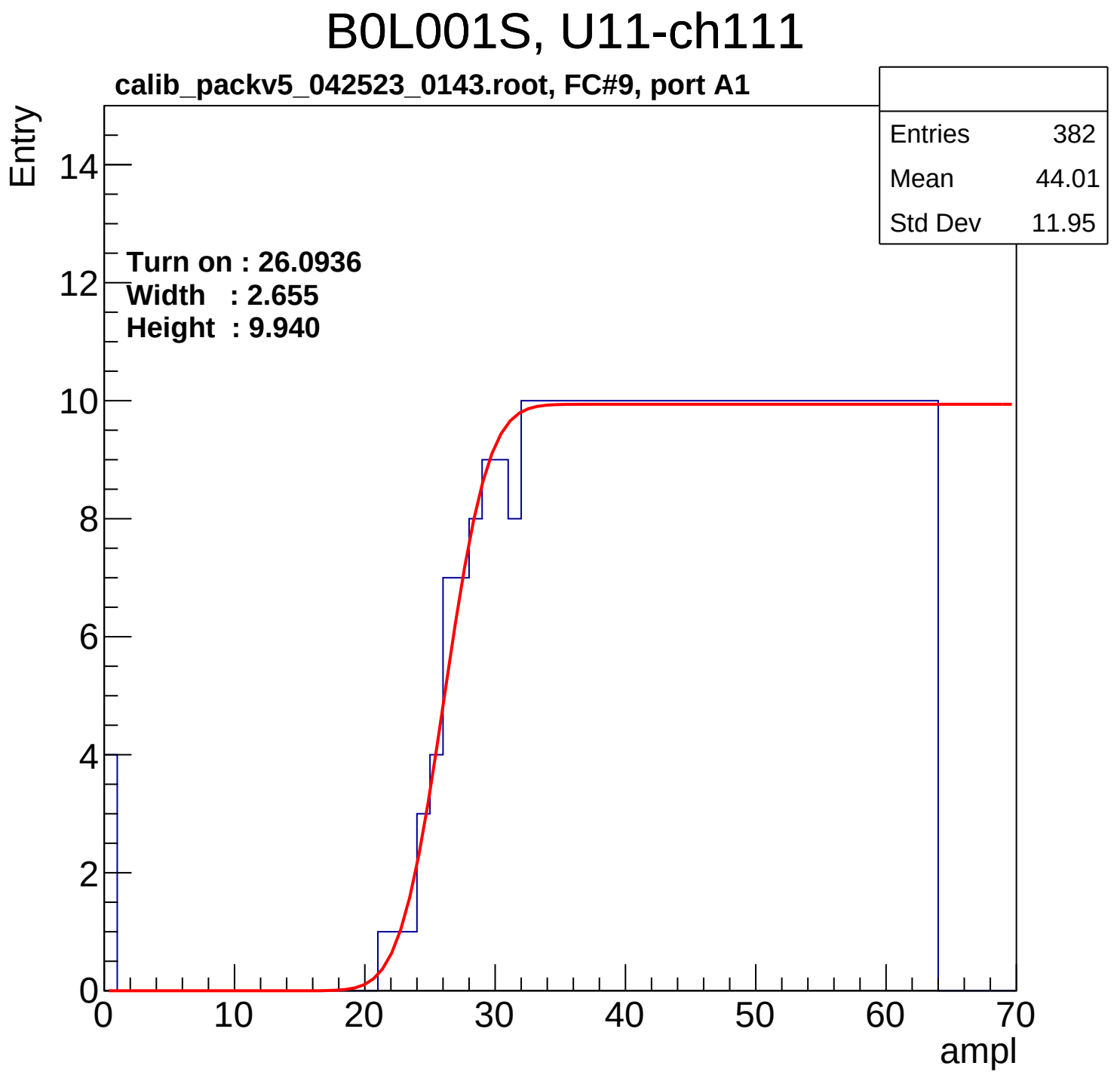
B0L001S, U11-ch111
calib_packv5_042523_0143.root, FC#9, port A1
Entries 382
Mean 44.01
Std Dev 11.95
Turn on : 26.0936
Width : 2.655
Height : 9.940
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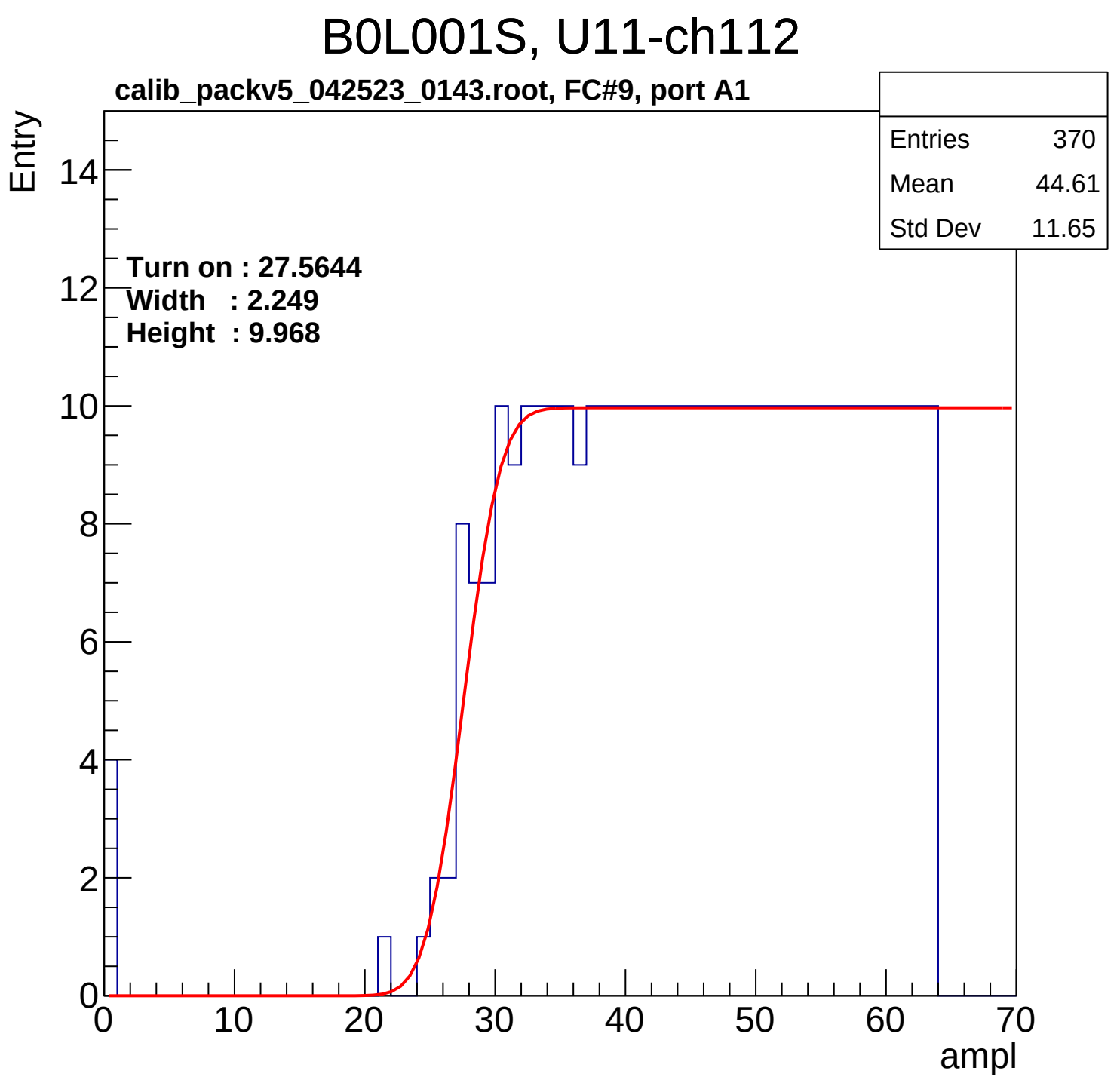
B0L001S, U11-ch112
calib_packv5_042523_0143.root, FC#9, port A1
Entries 370
Mean 44.61
Std Dev 11.65
Turn on : 27.5644
Width : 2.249
Height : 9.968
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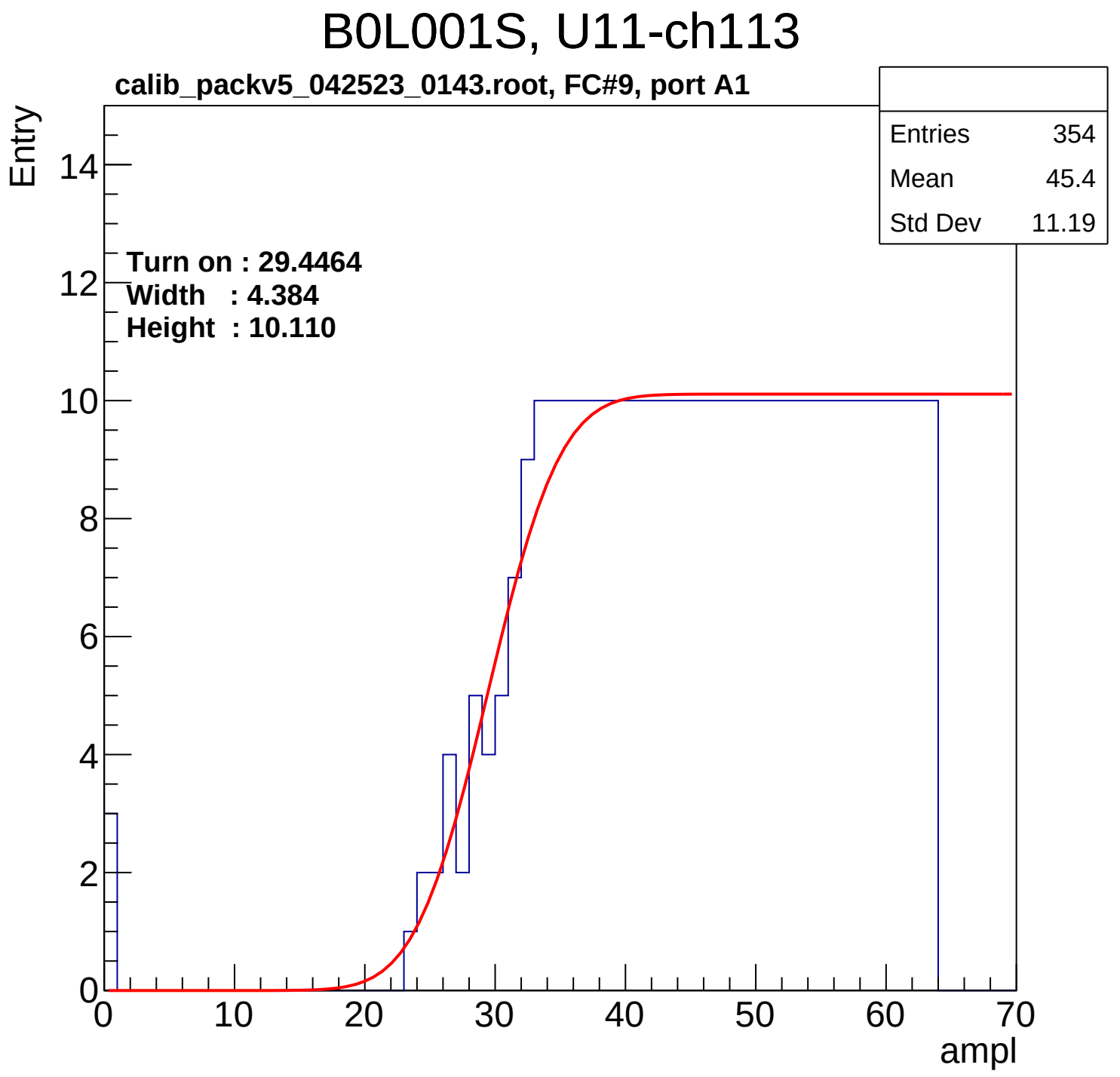
B0L001S, U11-ch113
calib_packv5_042523_0143.root, FC#9, port A1
Entries 354
Mean 45.4
Std Dev 11.19
Turn on : 29.4464
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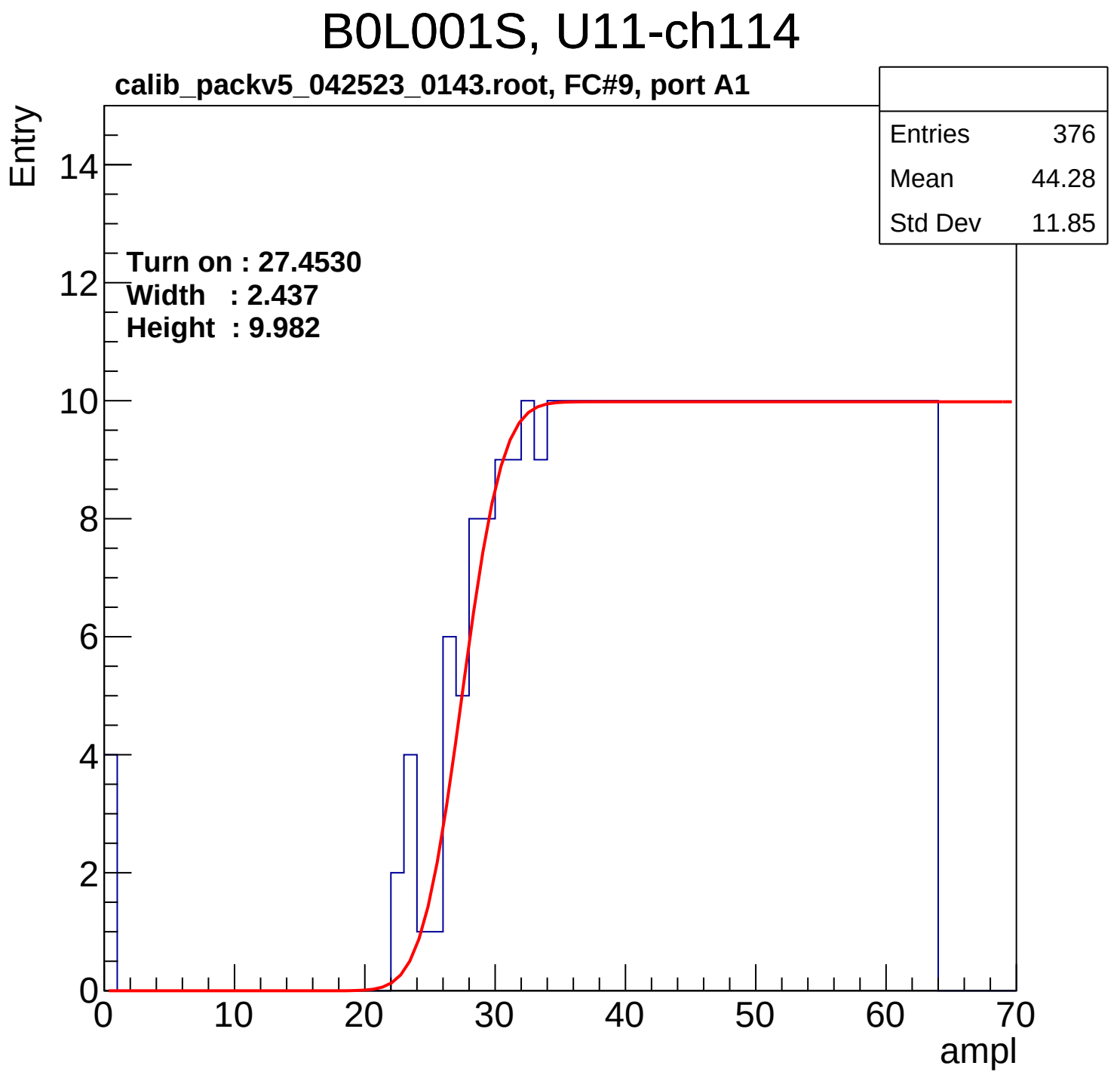
B0L001S, U11-ch114
calib_packv5_042523_0143.root, FC#9, port A1
Entries 376
Mean 44.28
Std Dev 11.85
Turn on : 27.4530
Width : 2.437
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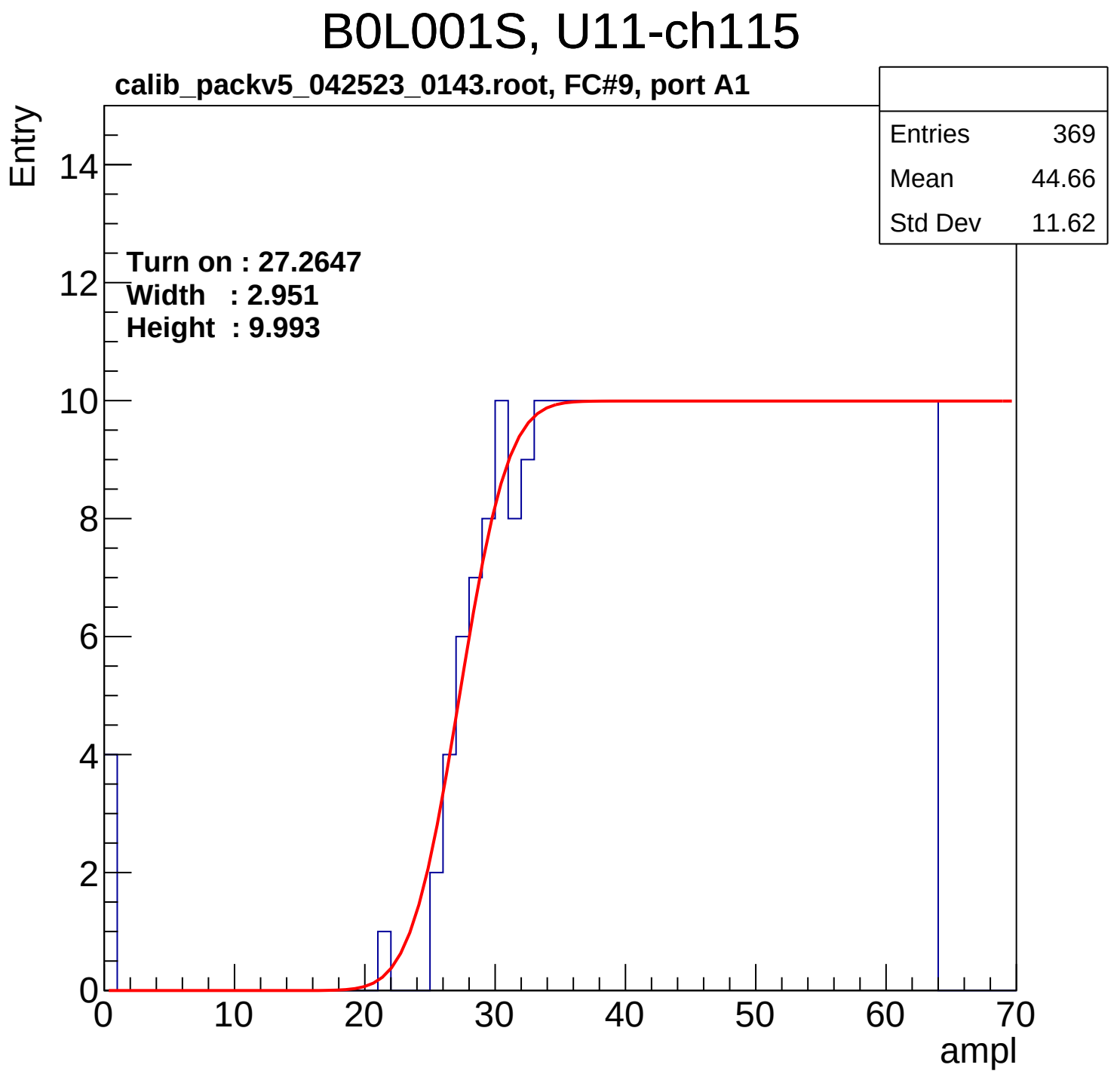
B0L001S, U11-ch115
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.66
Std Dev 11.62
Turn on : 27.2647
Width : 2.951
Height : 9.993
Entry
ampl
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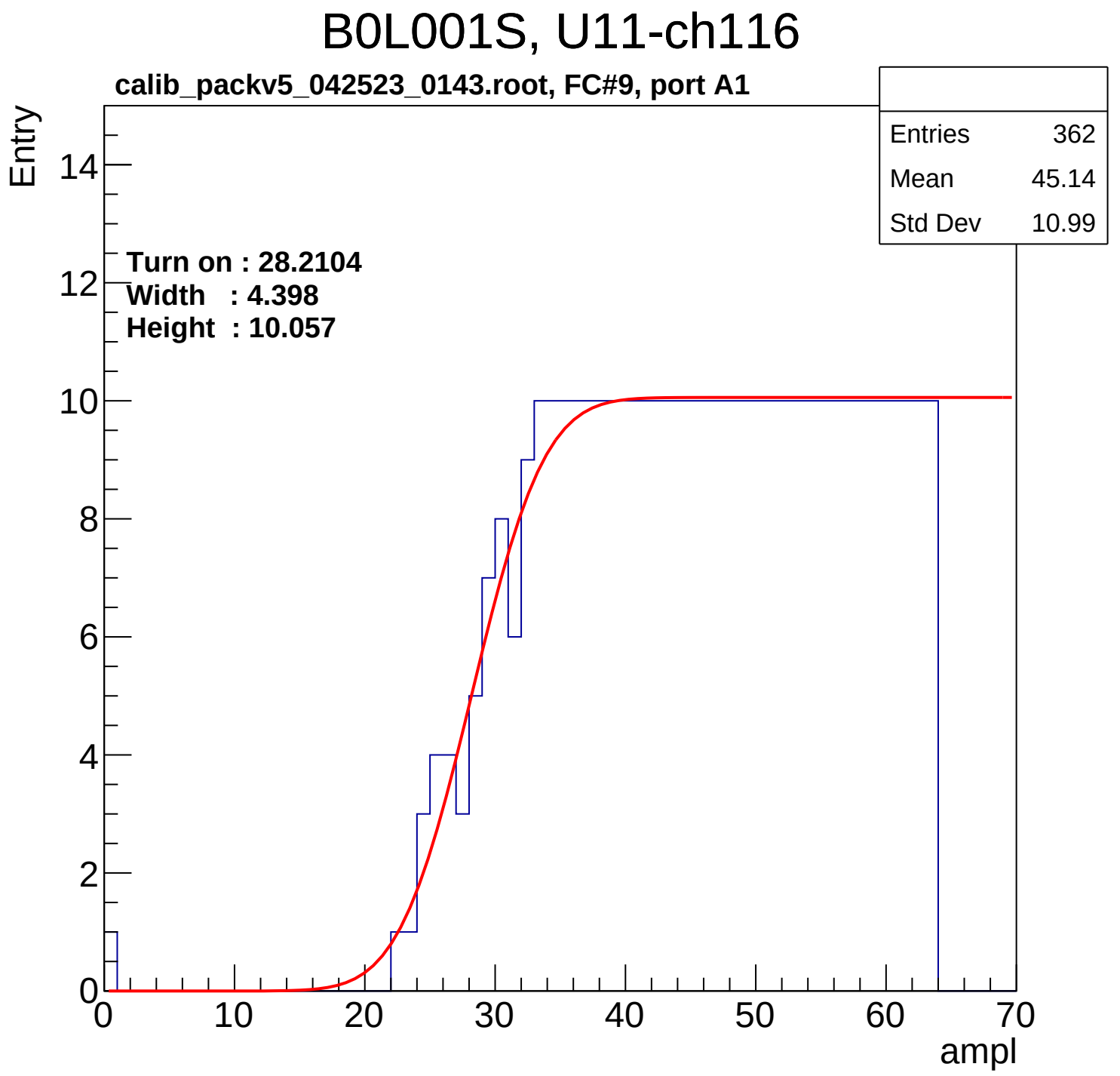
B0L001S, U11-ch116
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 45.14
Std Dev 10.99
Turn on : 28.2104
Width : 4.398
Height : 10.057
Entry
ampl
0
2
4
6
8
10
12
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0
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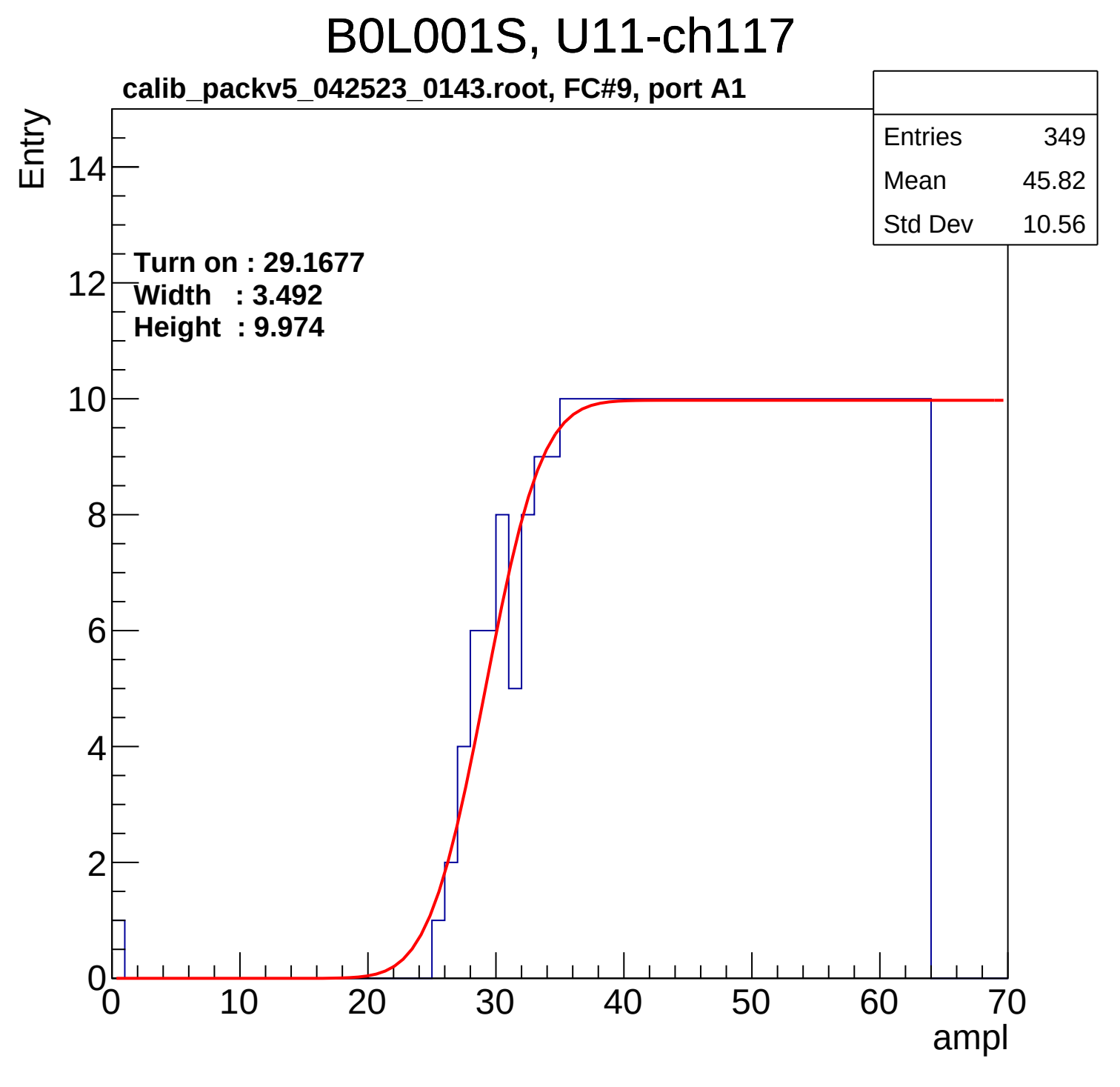
B0L001S, U11-ch117
calib_packv5_042523_0143.root, FC#9, port A1
Entries 349
Mean 45.82
Std Dev 10.56
Turn on : 29.1677
Width : 3.492
Height : 9.974
Entry
ampl
0
2
4
6
8
10
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0
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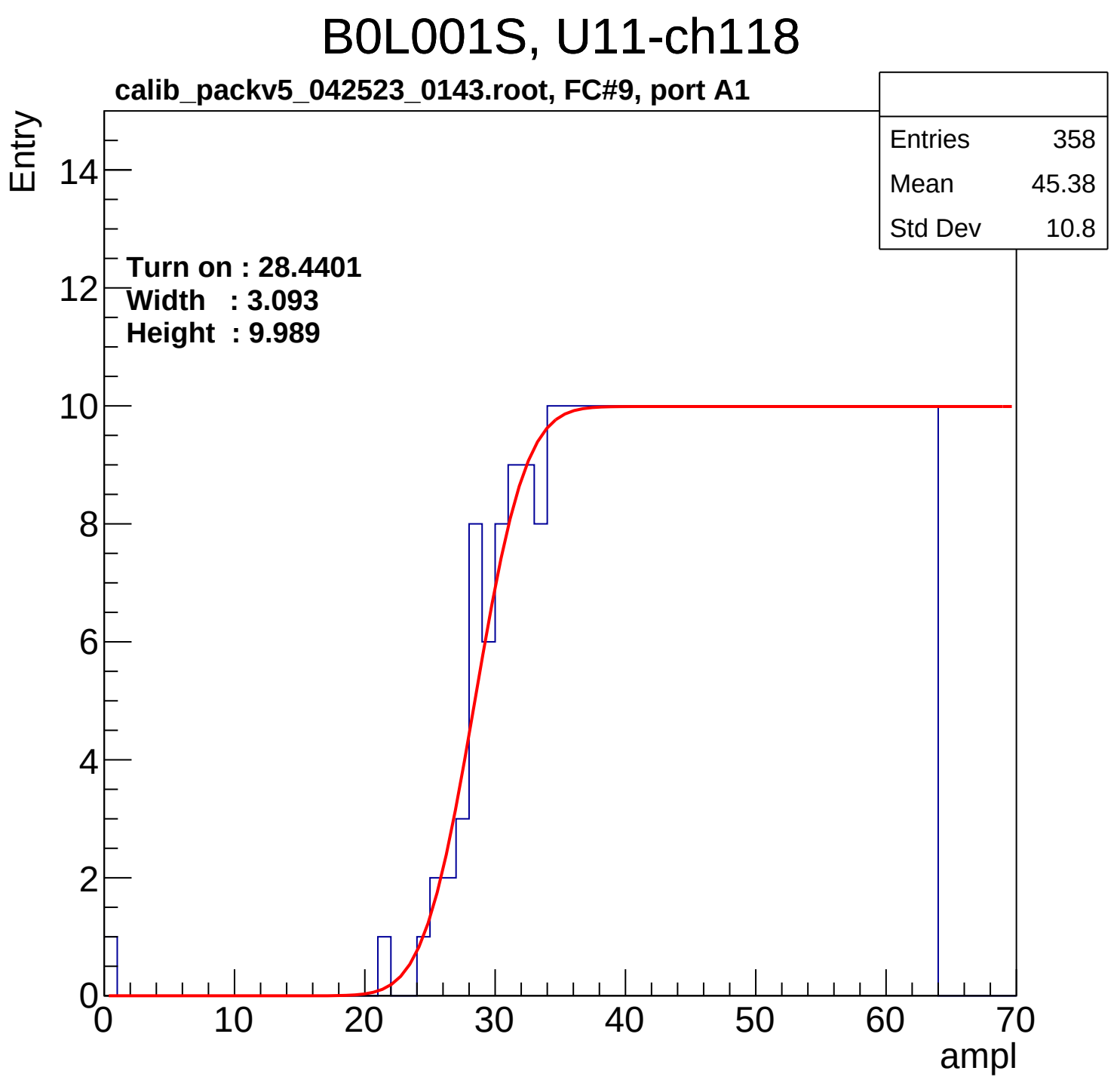
B0L001S, U11-ch118
calib_packv5_042523_0143.root, FC#9, port A1
Entries 358
Mean 45.38
Std Dev 10.8
Turn on : 28.4401
Width : 3.093
Height : 9.989
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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60
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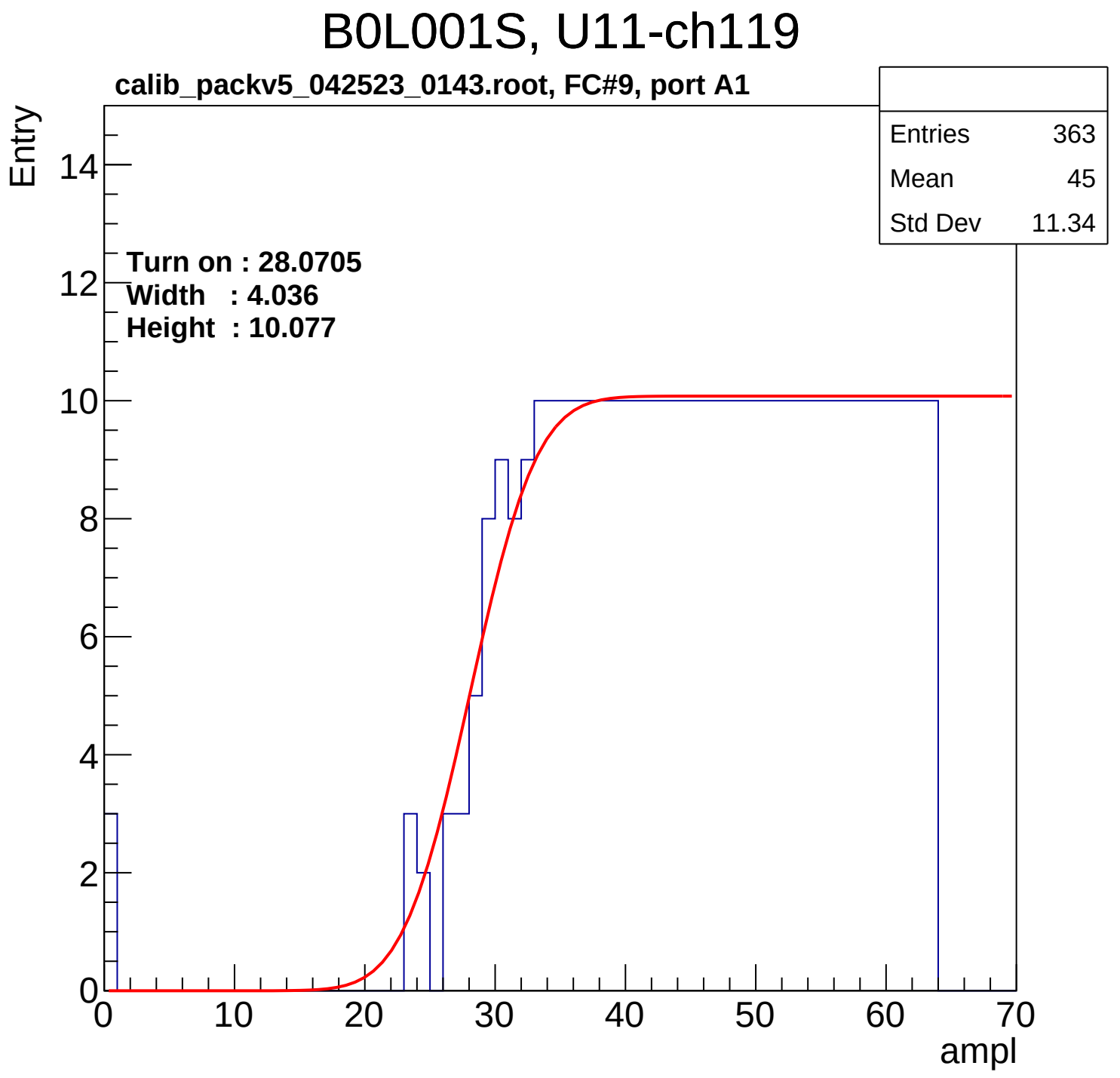
B0L001S, U11-ch119
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 45
Std Dev 11.34
Turn on : 28.0705
Width : 4.036
Height : 10.077
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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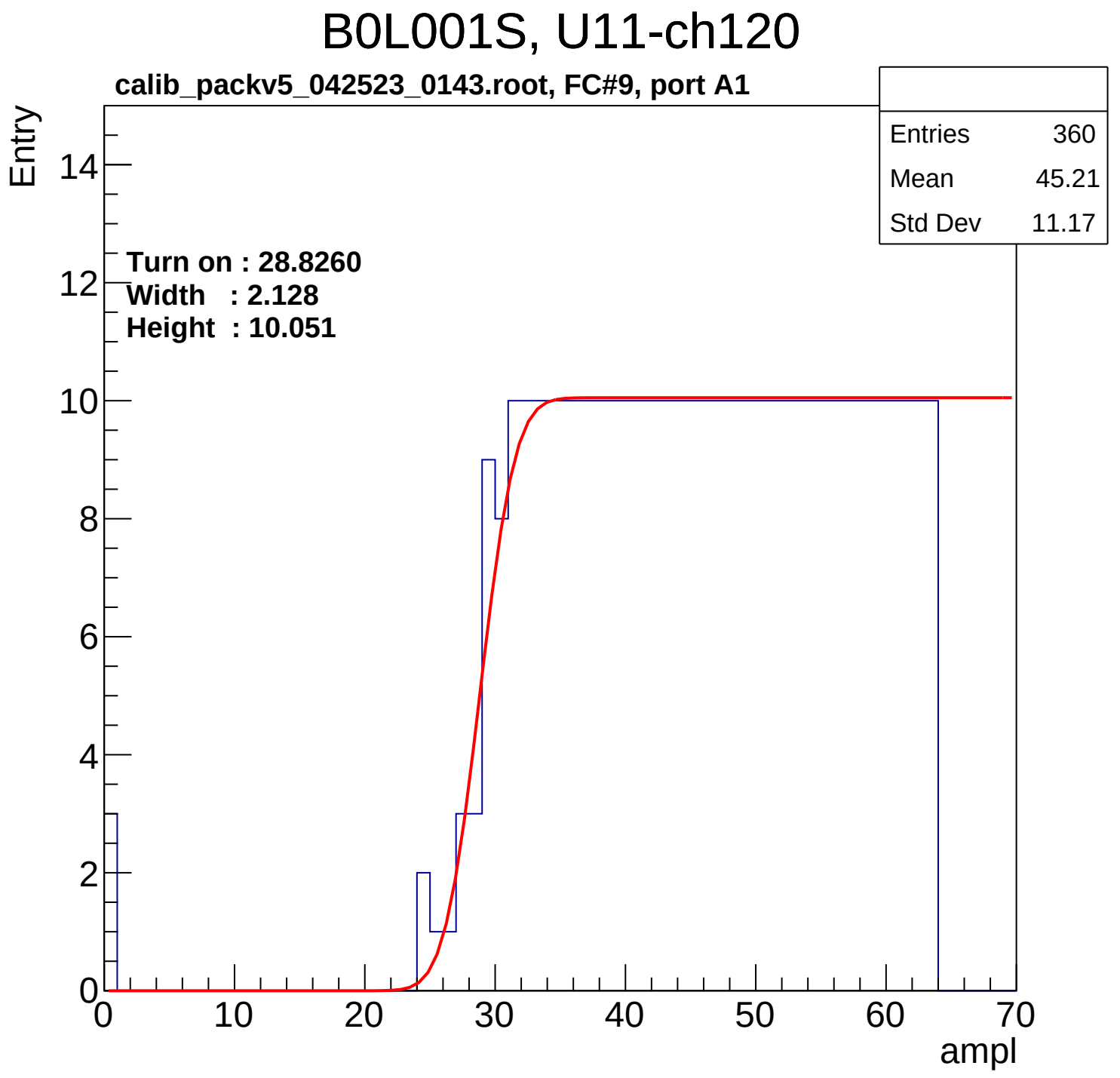
B0L001S, U11-ch120
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 45.21
Std Dev 11.17
Turn on : 28.8260
Width : 2.128
Height : 10.051
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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60
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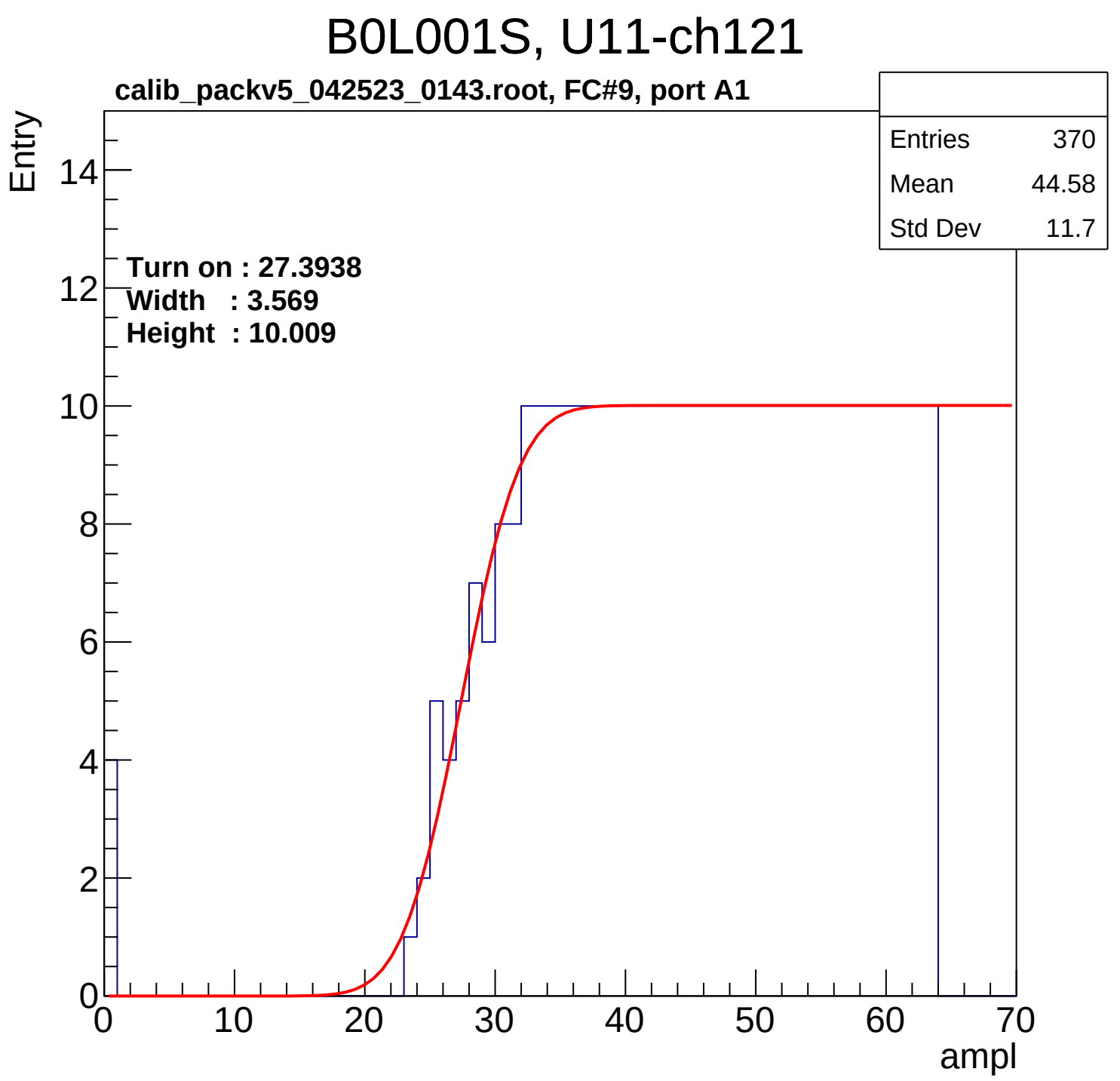
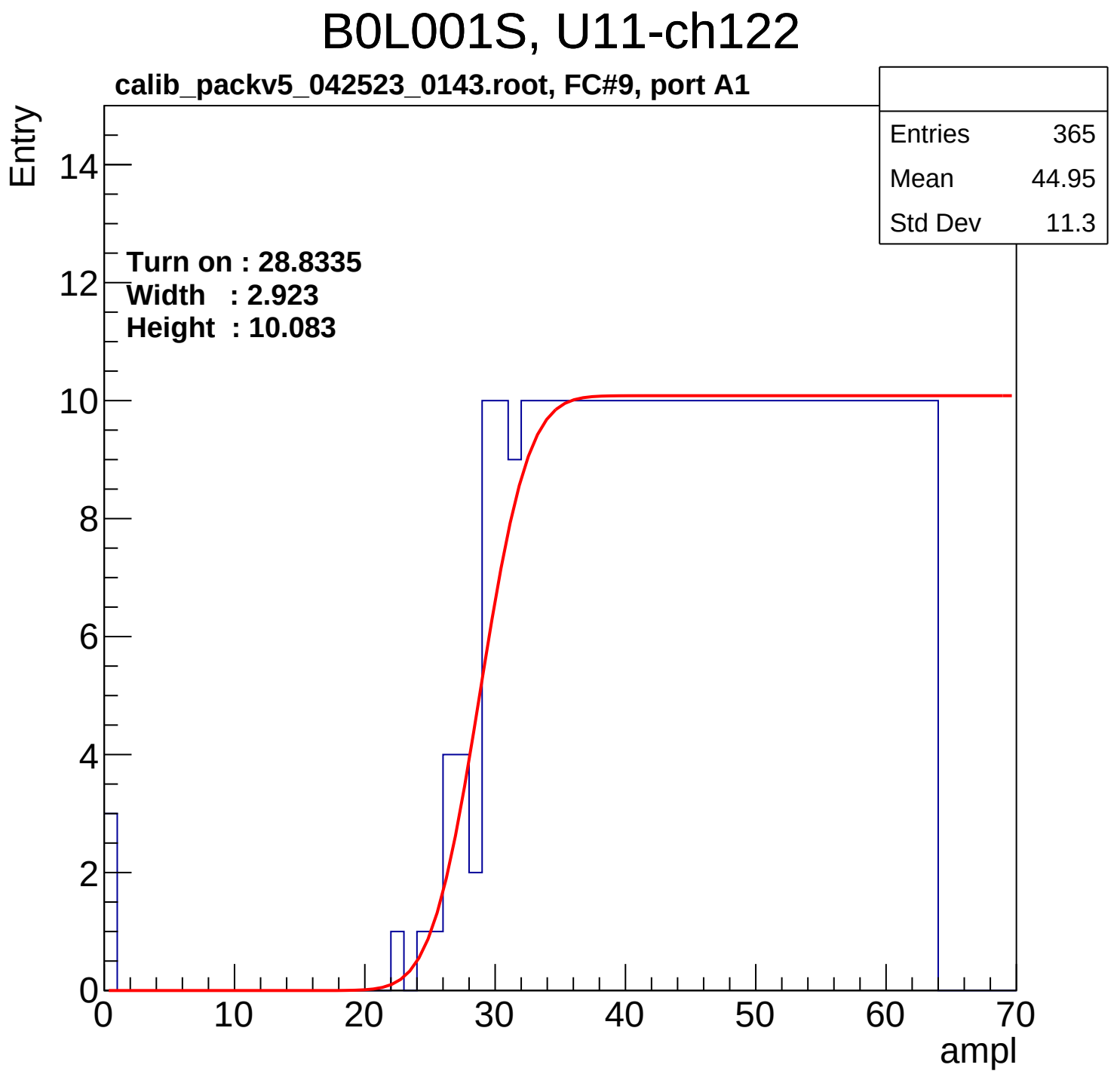

B0L001S, U11-ch121
calib_packv5_042523_0143.root, FC#9, port A1
Entries 370
Mean 44.58
Std Dev 11.7
Turn on : 27.3938
Width : 3.569
Height : 10.009
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U11-ch122
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 44.95
Std Dev 11.3
Turn on : 28.8335
Width : 2.923
Height : 10.083
Entry
ampl
0
2
4
6
8
10
12
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0
10
20
30
40
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60
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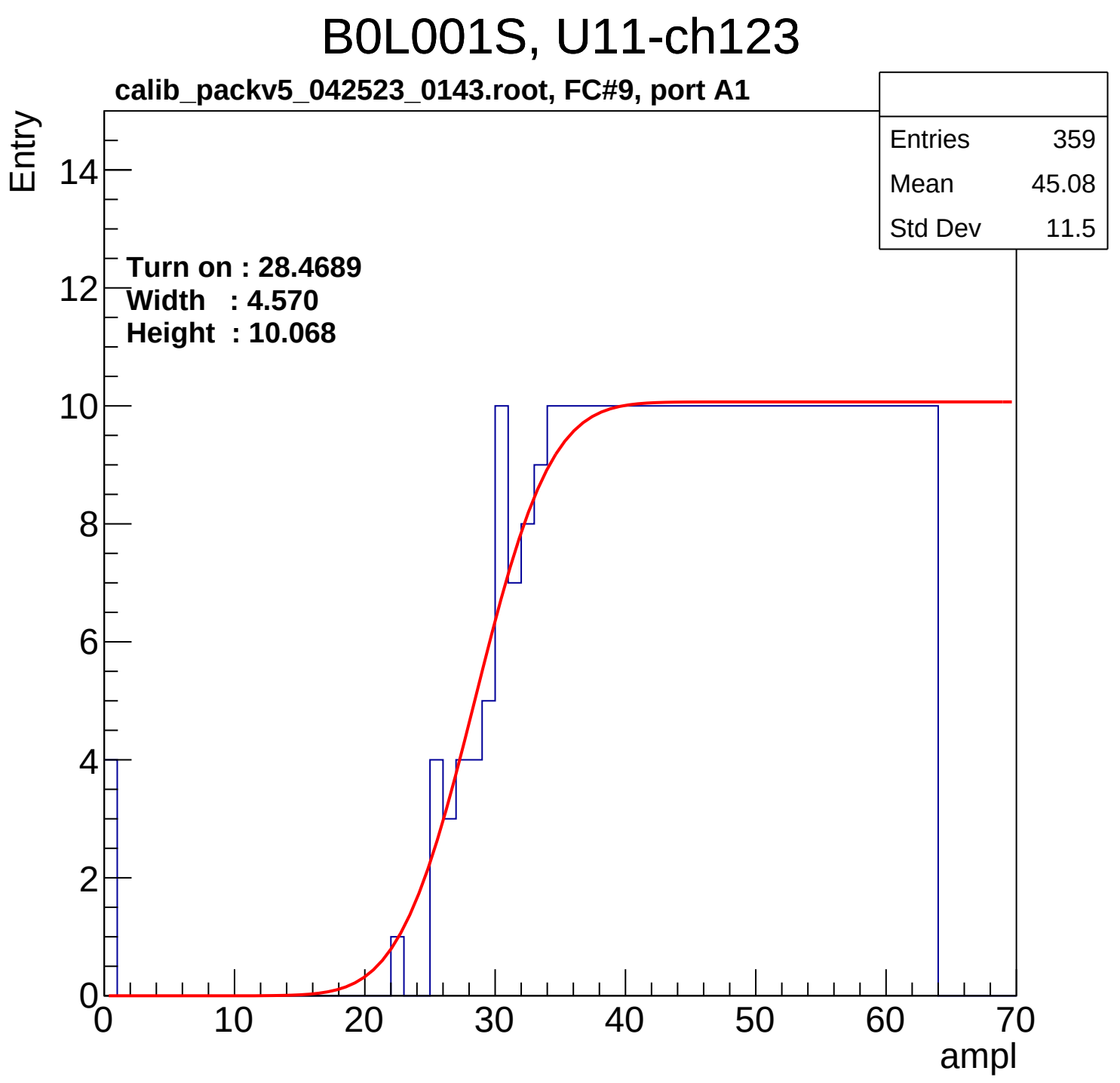
B0L001S, U11-ch123
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 45.08
Std Dev 11.5
Turn on : 28.4689
Width : 4.570
Height : 10.068
Entry
ampl
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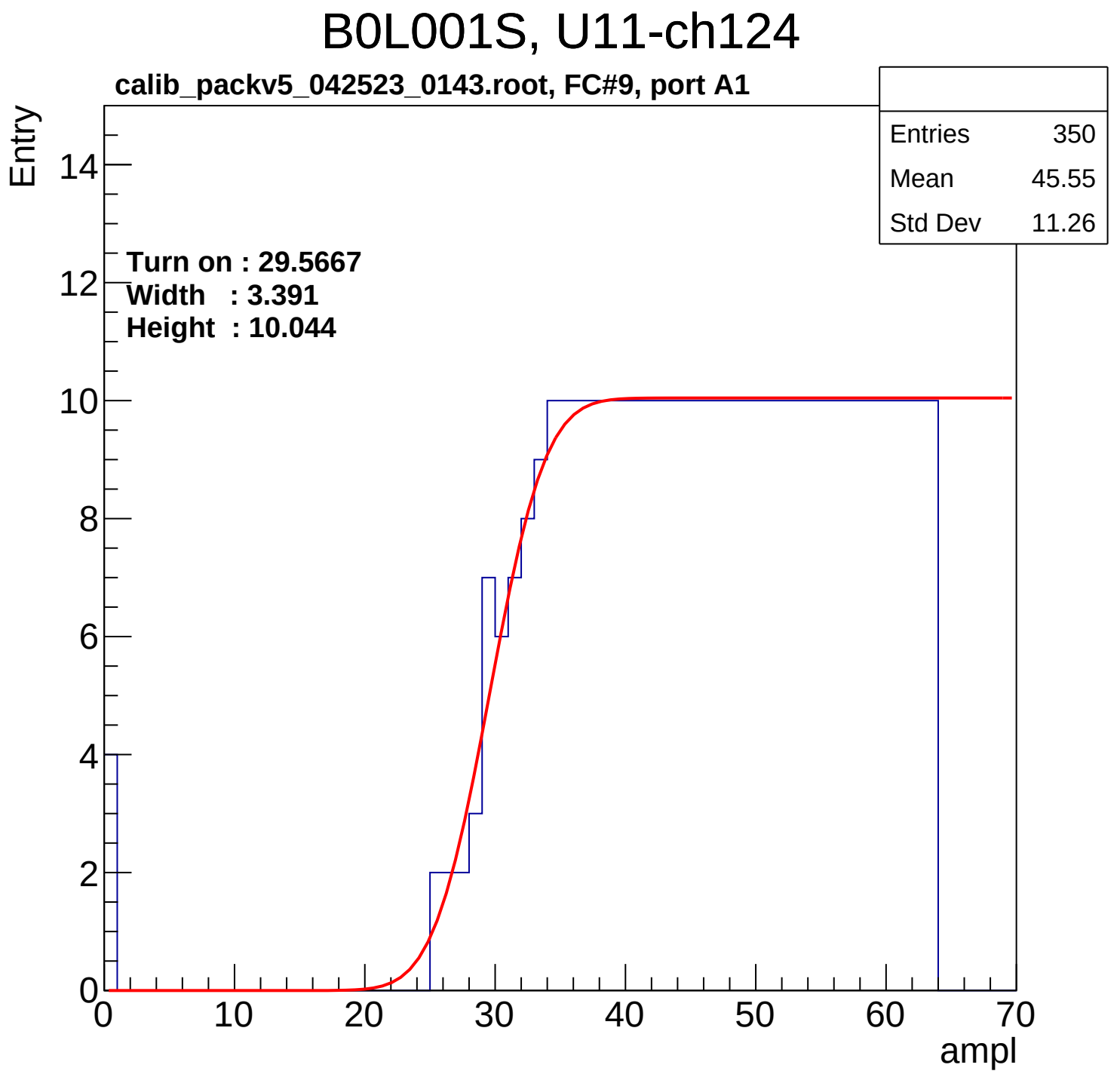
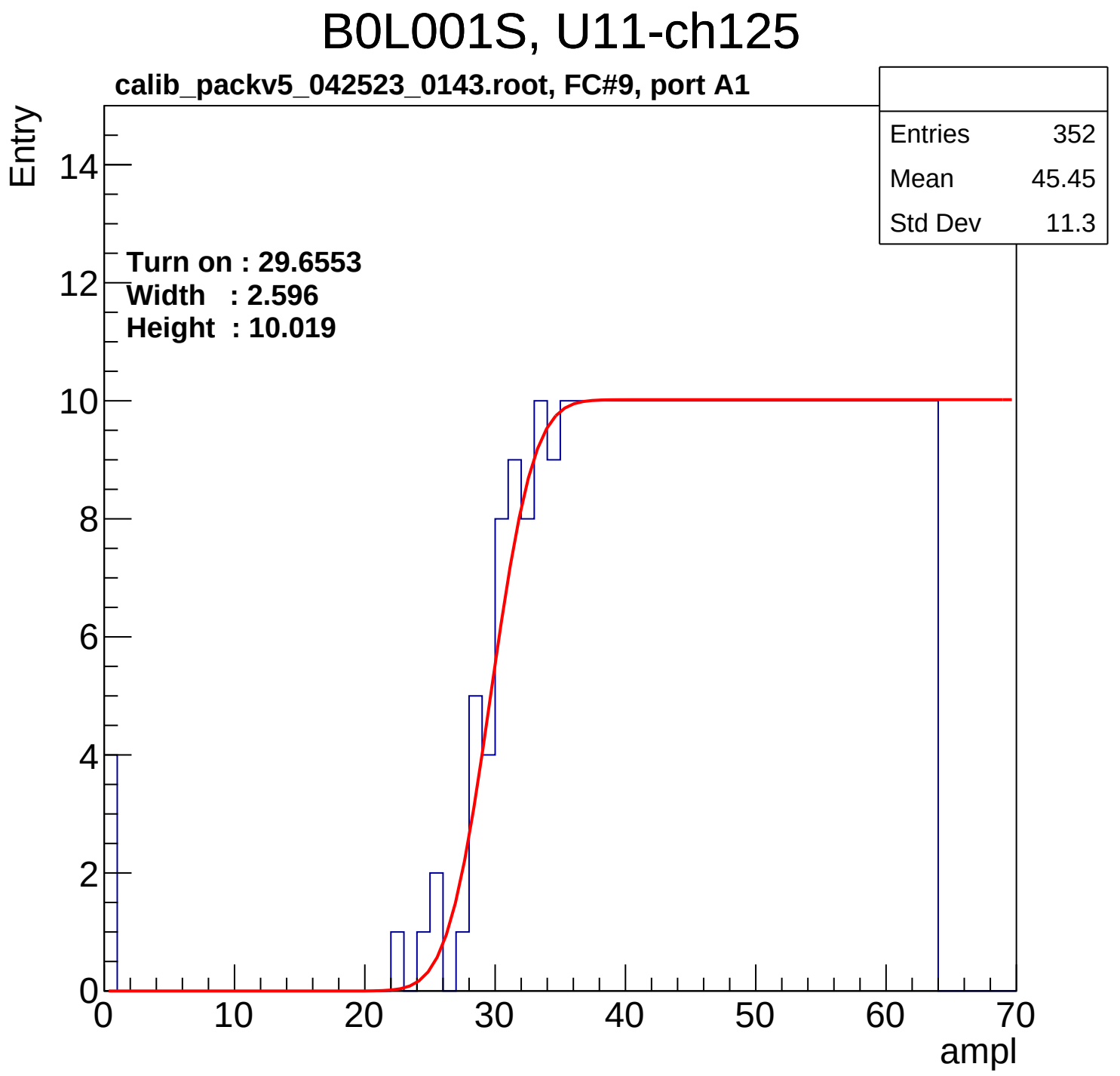
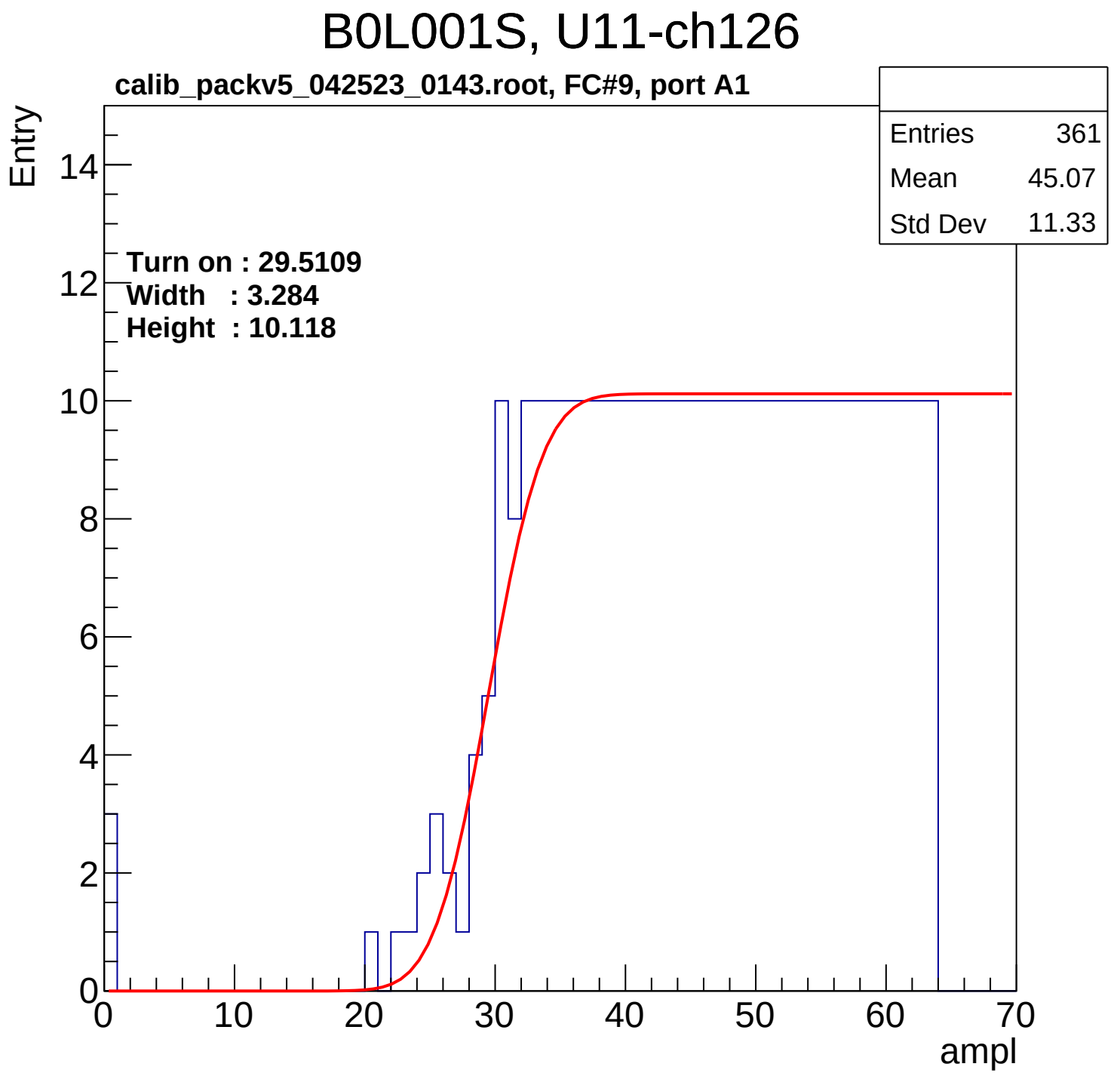
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U11-ch124
calib_packv5_042523_0143.root, FC#9, port A1
Entries 350
Mean 45.55
Std Dev 11.26
Turn on : 29.5667
Width : 3.391
Height : 10.044
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U11-ch125
calib_packv5_042523_0143.root, FC#9, port A1
Entries 352
Mean 45.45
Std Dev 11.3
Turn on : 29.6553
Width : 2.596
Height : 10.019
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U11-ch126
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 45.07
Std Dev 11.33
Turn on : 29.5109
Width : 3.284
Height : 10.118
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
50
60
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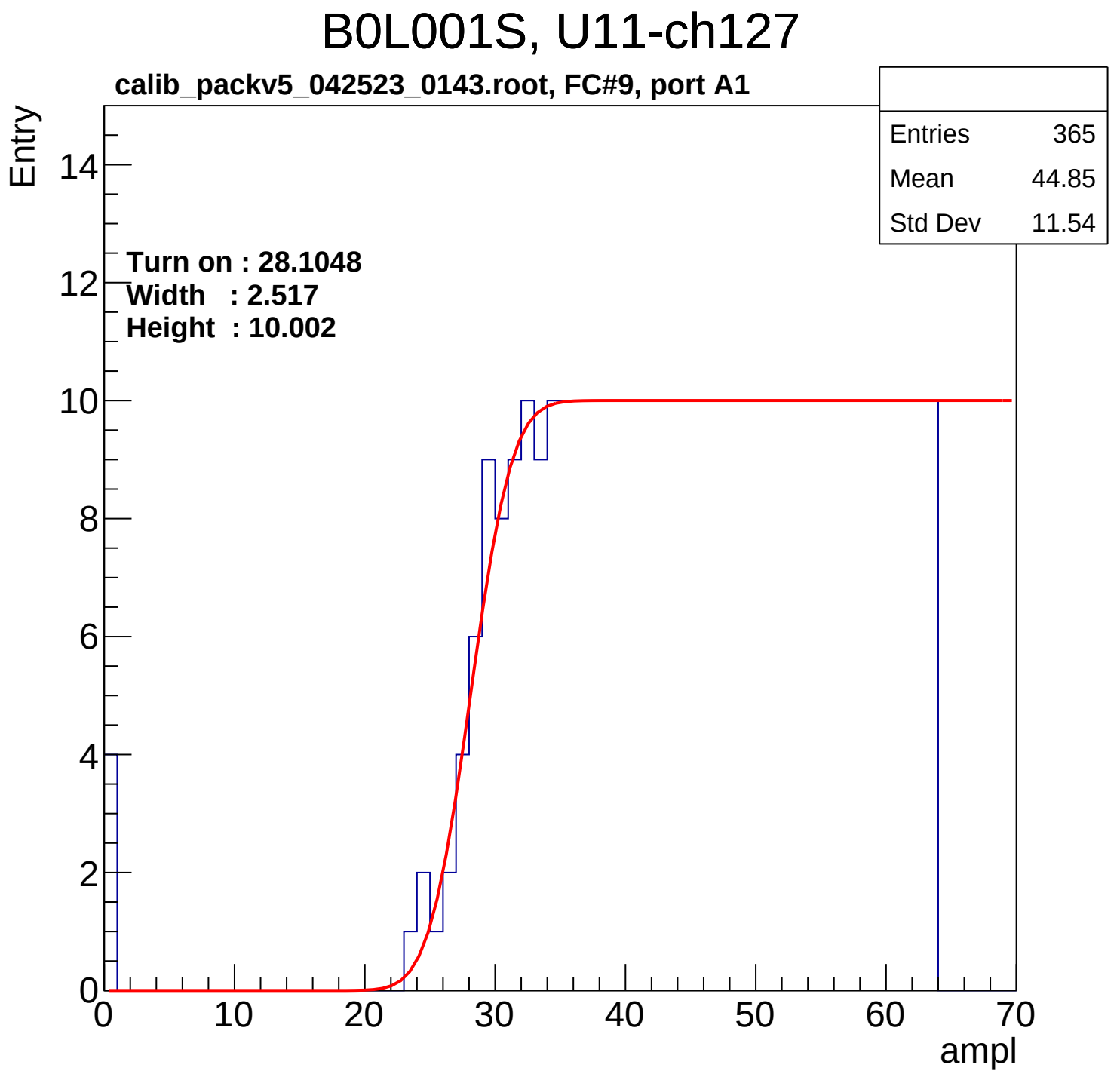
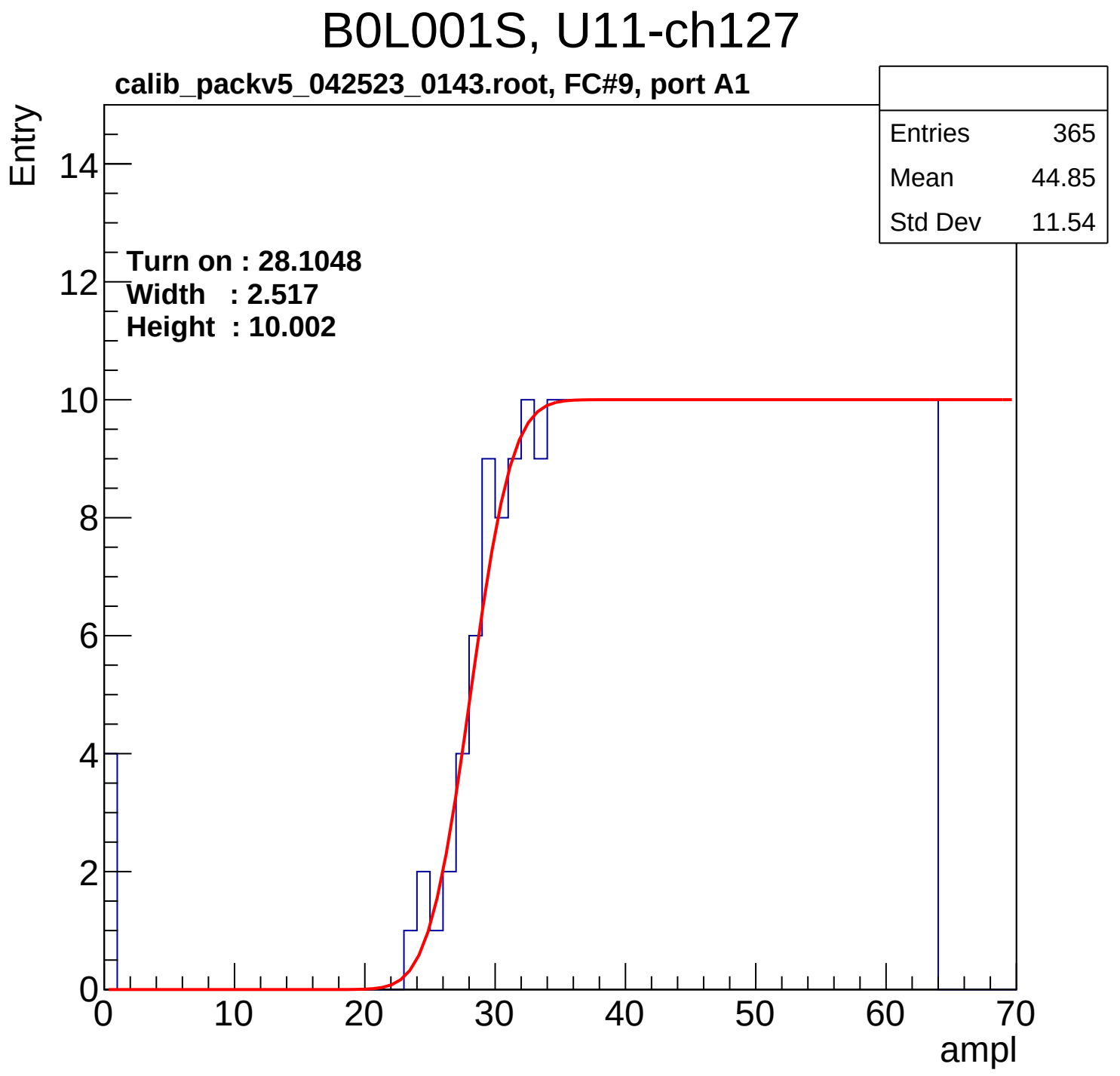

B0L001S, U11-ch127
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 44.85
Std Dev 11.54
Turn on : 28.1048
Width : 2.517
Height : 10.002
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U11-ch127
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 44.85
Std Dev 11.54
Turn on : 28.1048
Width : 2.517
Height : 10.002
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70