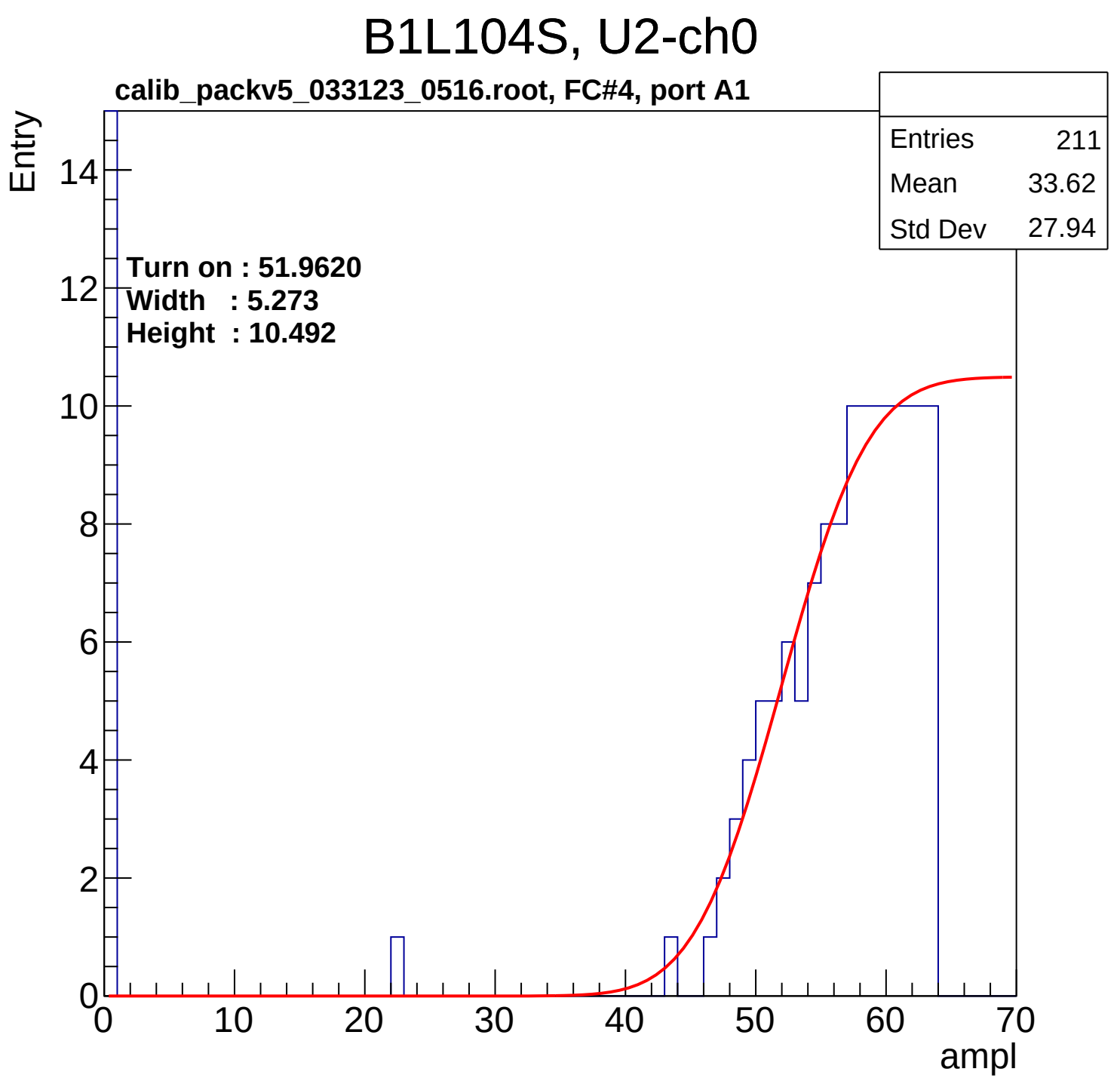
B1L104S, U2-ch0
calib_packv5_033123_0516.root, FC#4, port A1
Entries 211
Mean 33.62
Std Dev 27.94
Turn on : 51.9620
Width : 5.273
Height : 10.492
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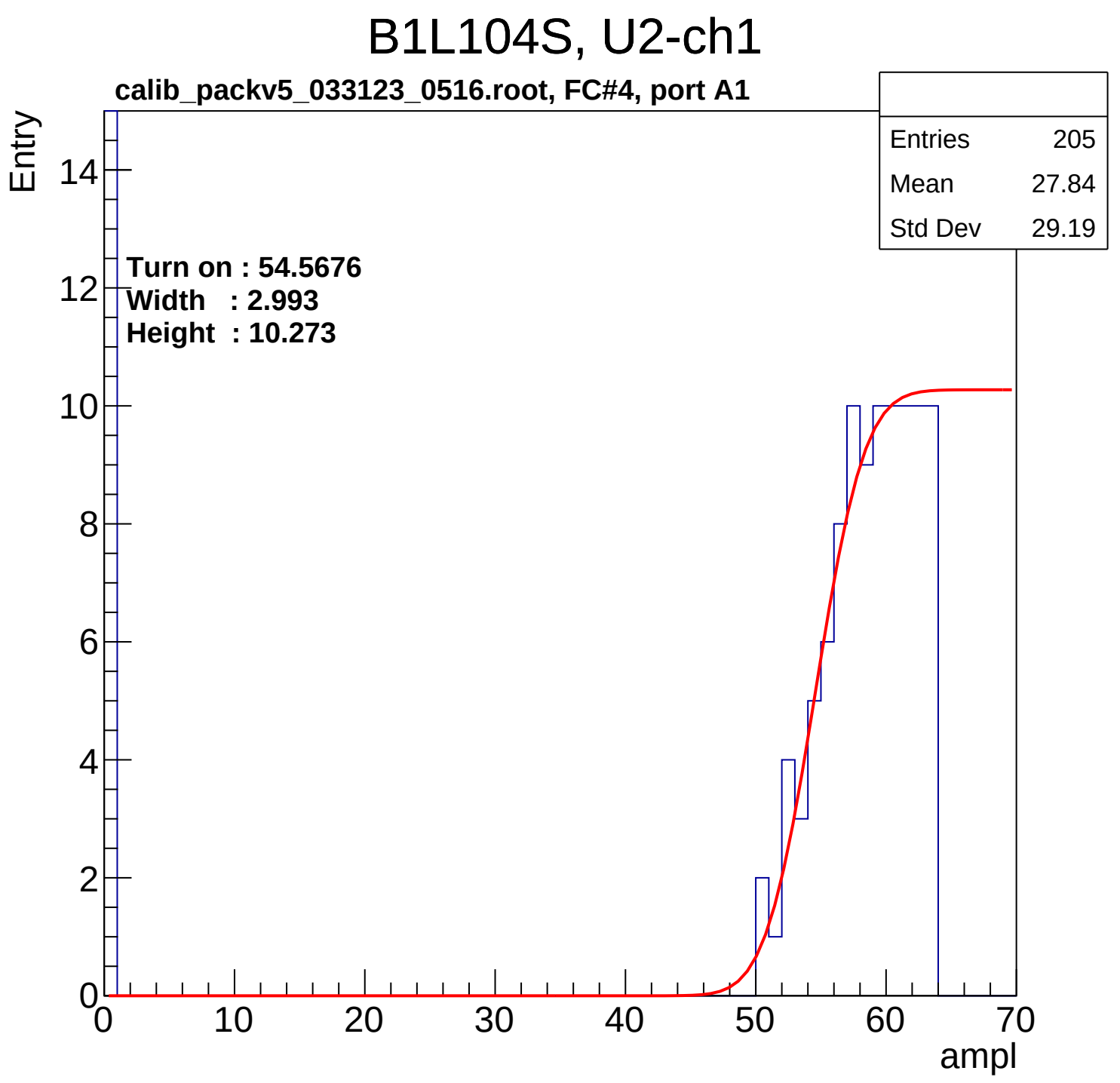
B1L104S, U2-ch1
calib_packv5_033123_0516.root, FC#4, port A1
Entries 205
Mean 27.84
Std Dev 29.19
Turn on : 54.5676
Width : 2.993
Height : 10.273
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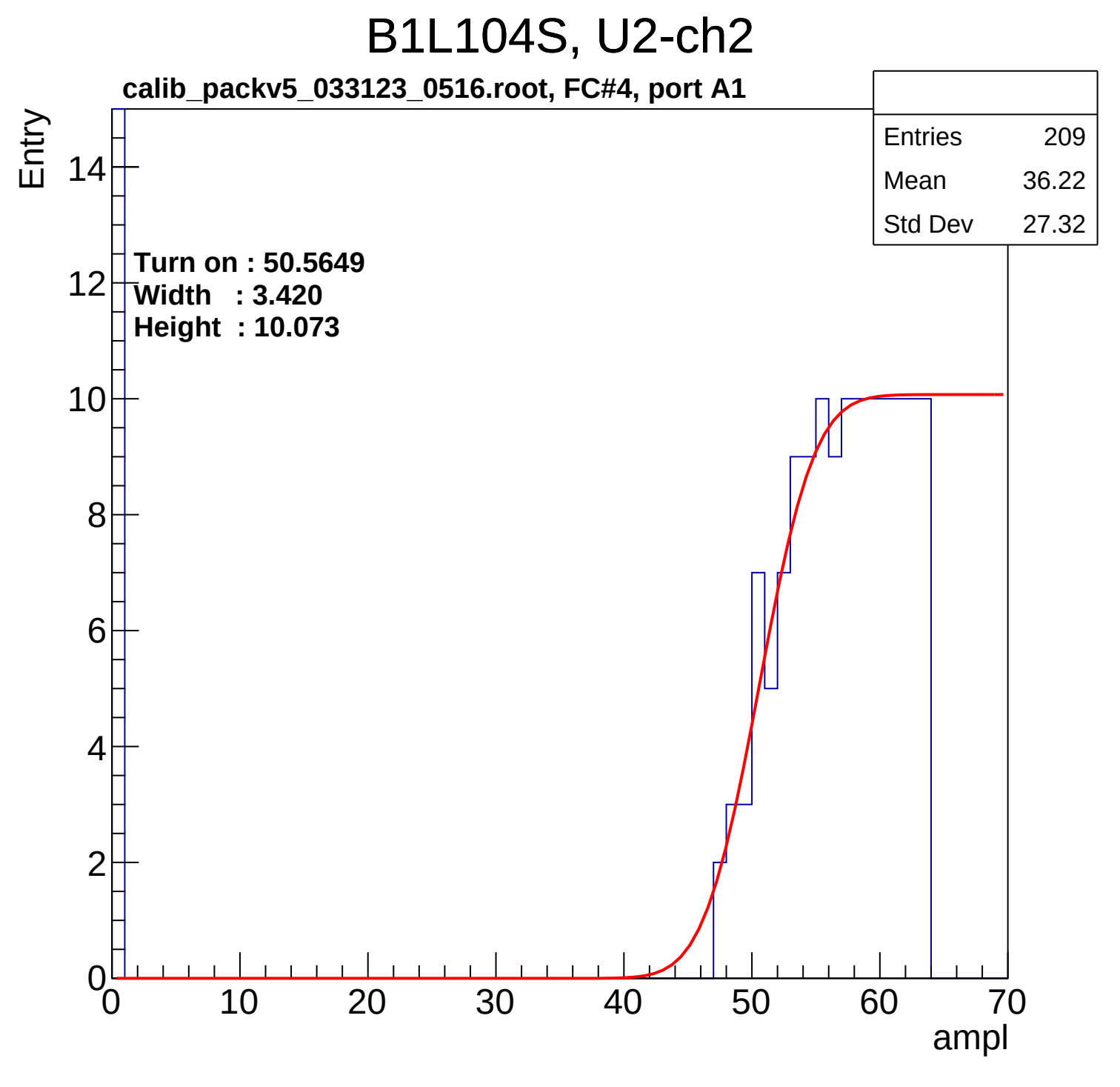
B1L104S, U2-ch2
calib_packv5_033123_0516.root, FC#4, port A1
Entries 209
Mean 36.22
Std Dev 27.32
Turn on : 50.5649
Width : 3.420
Height : 10.073
Entry
ampl
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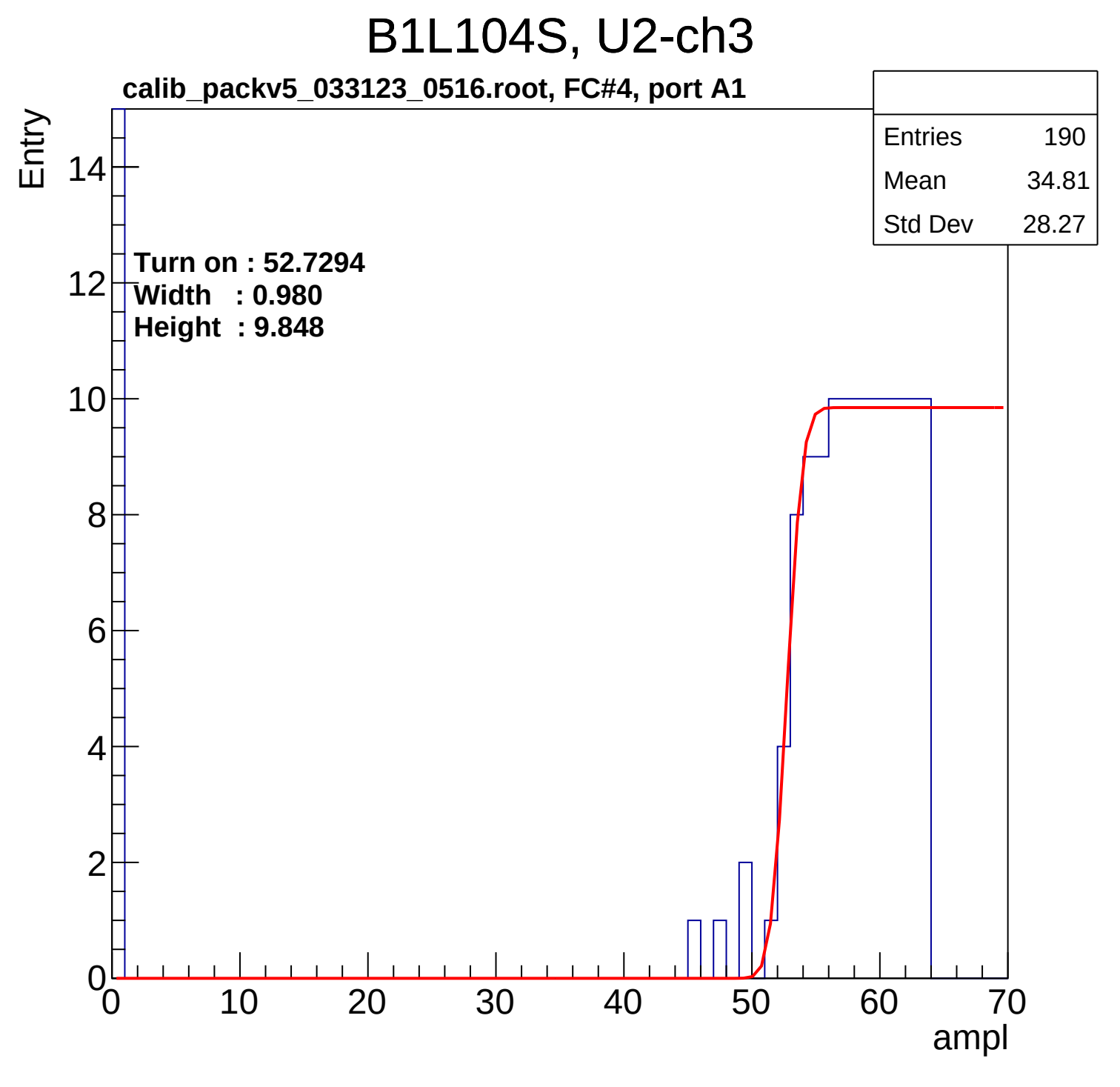
B1L104S, U2-ch3
calib_packv5_033123_0516.root, FC#4, port A1
Entries 190
Mean 34.81
Std Dev 28.27
Turn on : 52.7294
Width : 0.980
Height : 9.848
Entry
ampl
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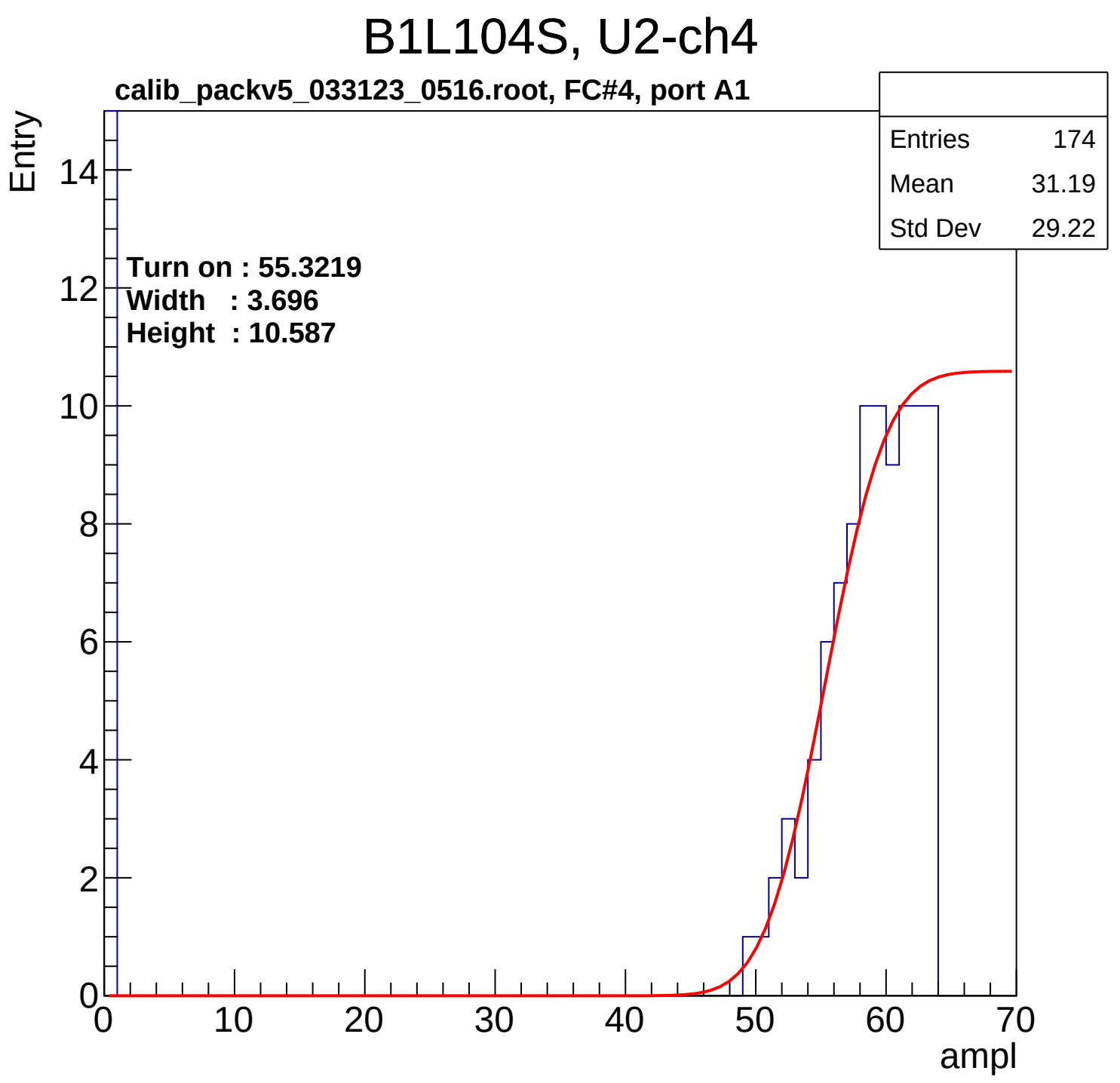
B1L104S, U2-ch4
calib_packv5_033123_0516.root, FC#4, port A1
Entries 174
Mean 31.19
Std Dev 29.22
Turn on : 55.3219
Width : 3.696
Height : 10.587
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ampl
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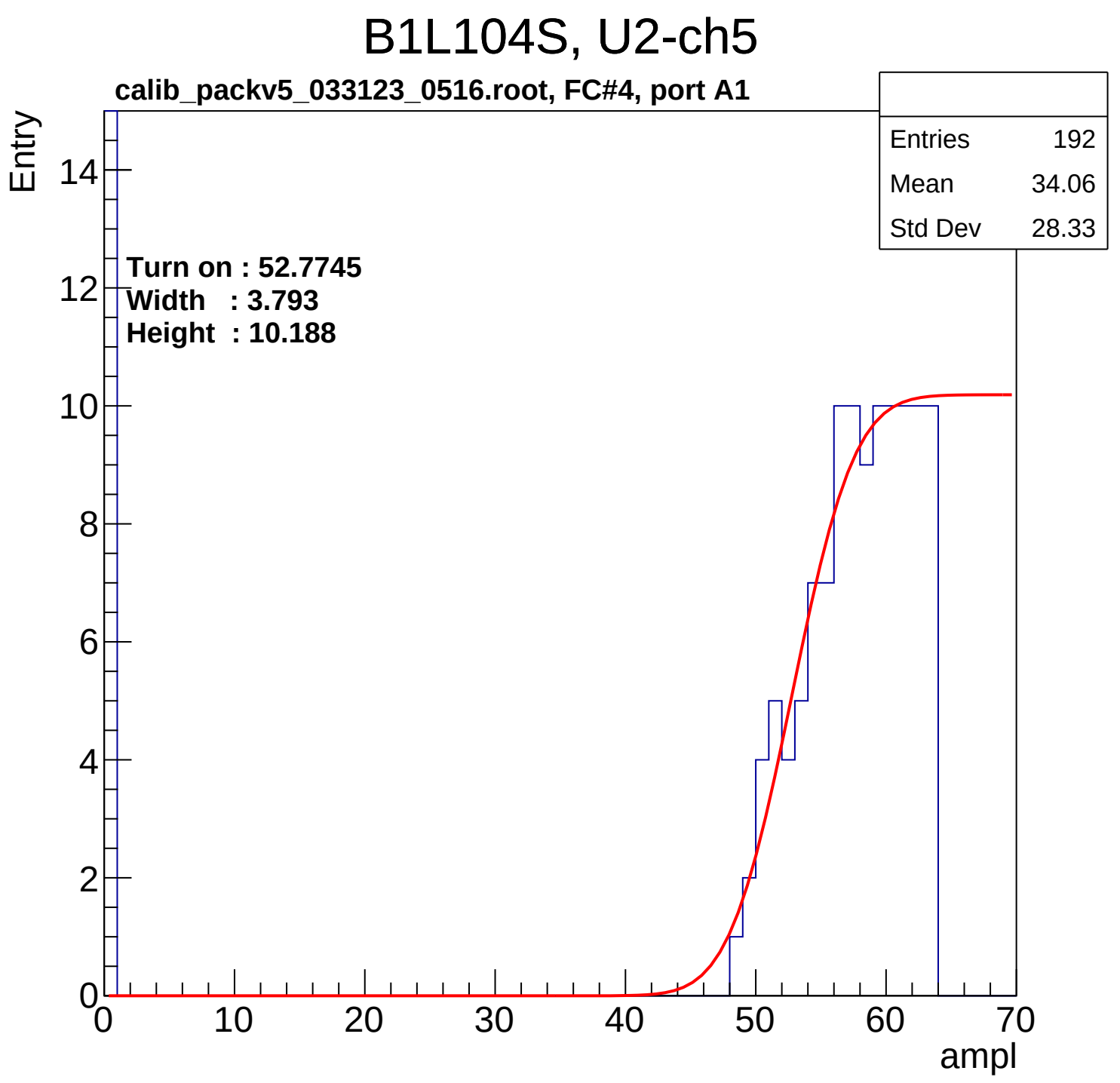
B1L104S, U2-ch5
calib_packv5_033123_0516.root, FC#4, port A1
Entries 192
Mean 34.06
Std Dev 28.33
Turn on : 52.7745
Width : 3.793
Height : 10.188
Entry
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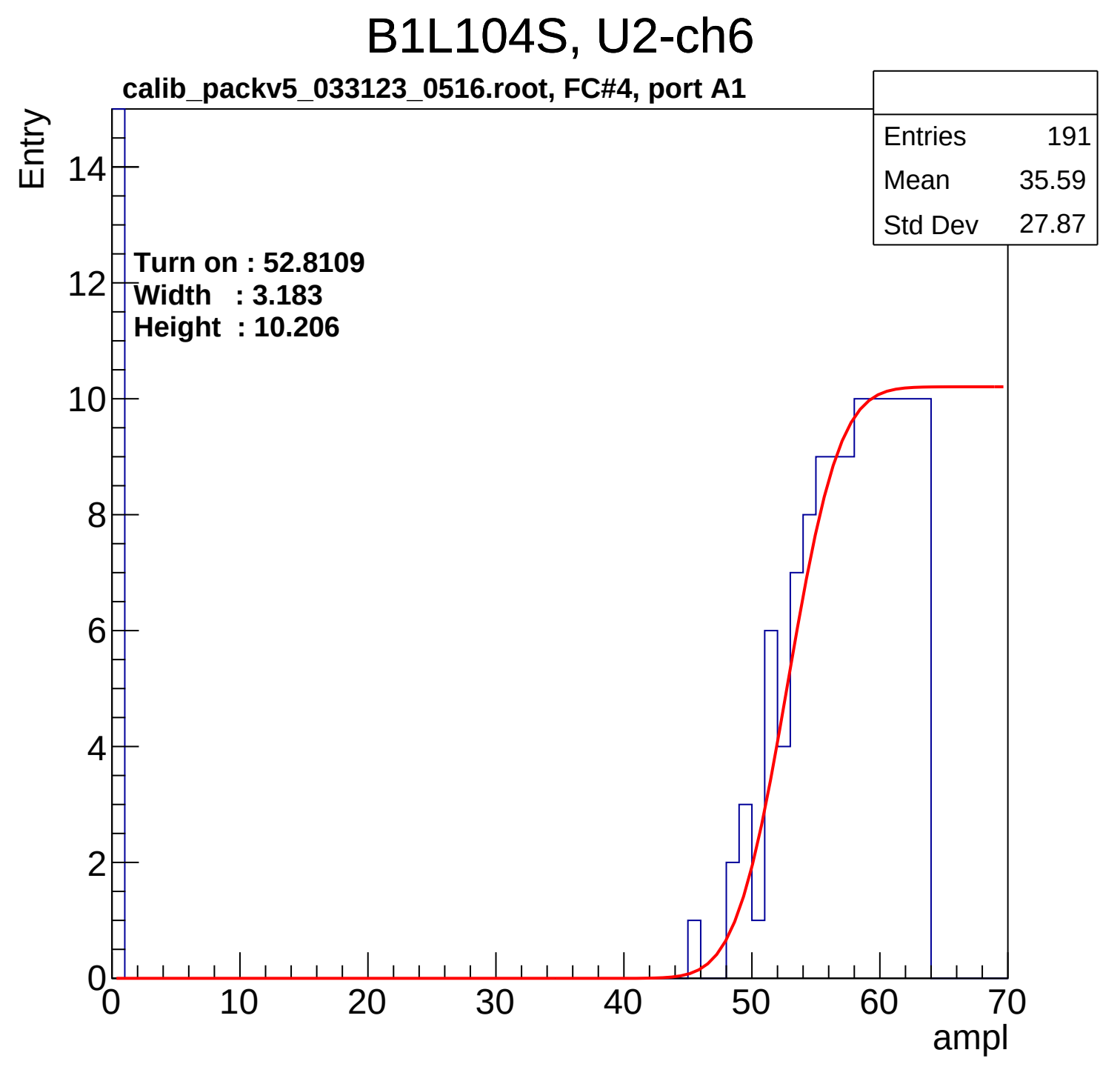
B1L104S, U2-ch6
calib_packv5_033123_0516.root, FC#4, port A1
Entries 191
Mean 35.59
Std Dev 27.87
Turn on : 52.8109
Width : 3.183
Height : 10.206
Entry
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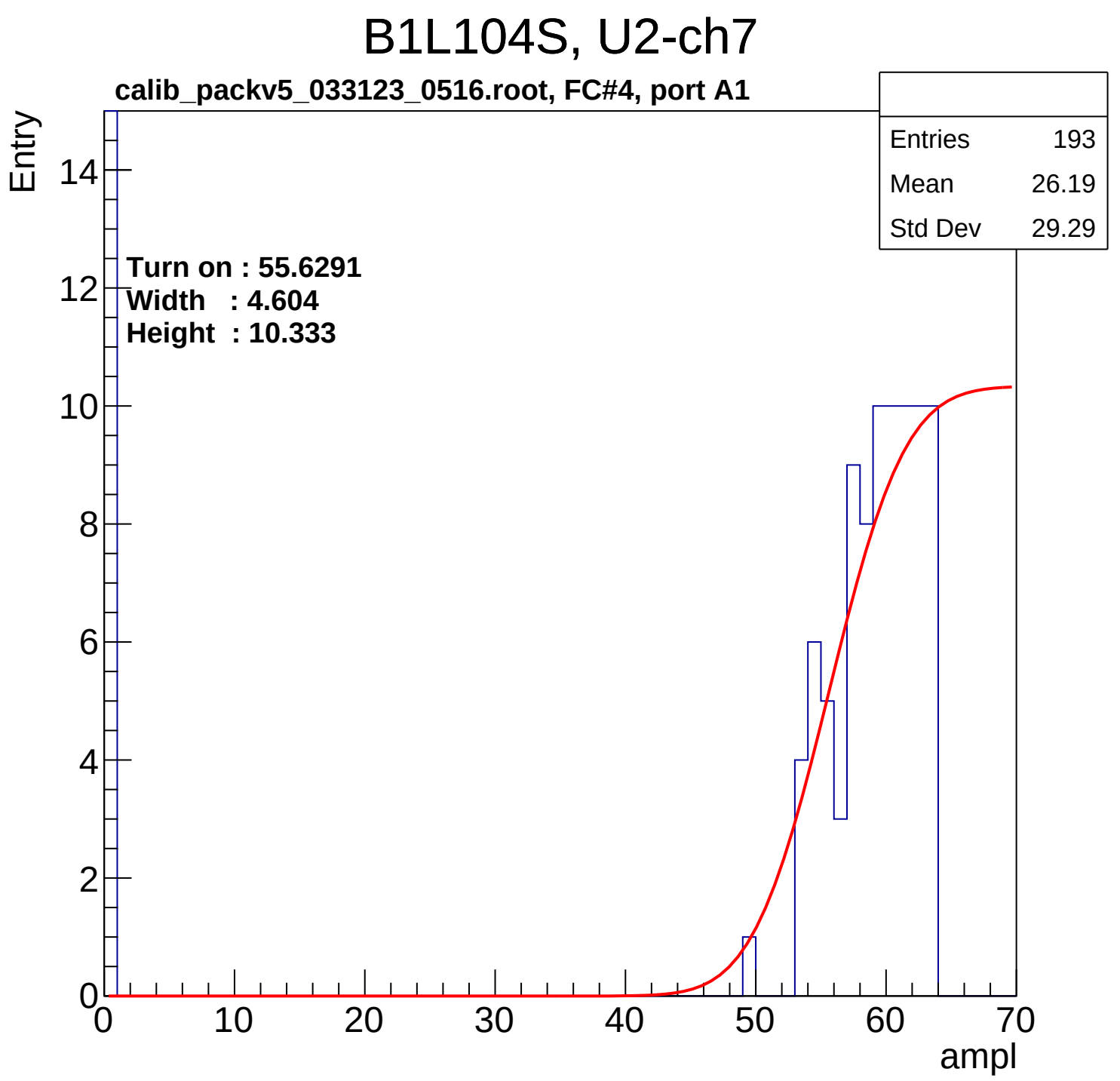
B1L104S, U2-ch7
calib_packv5_033123_0516.root, FC#4, port A1
Entries 193
Mean 26.19
Std Dev 29.29
Turn on : 55.6291
Width : 4.604
Height : 10.333
Entry
ampl
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2
4
6
8
10
12
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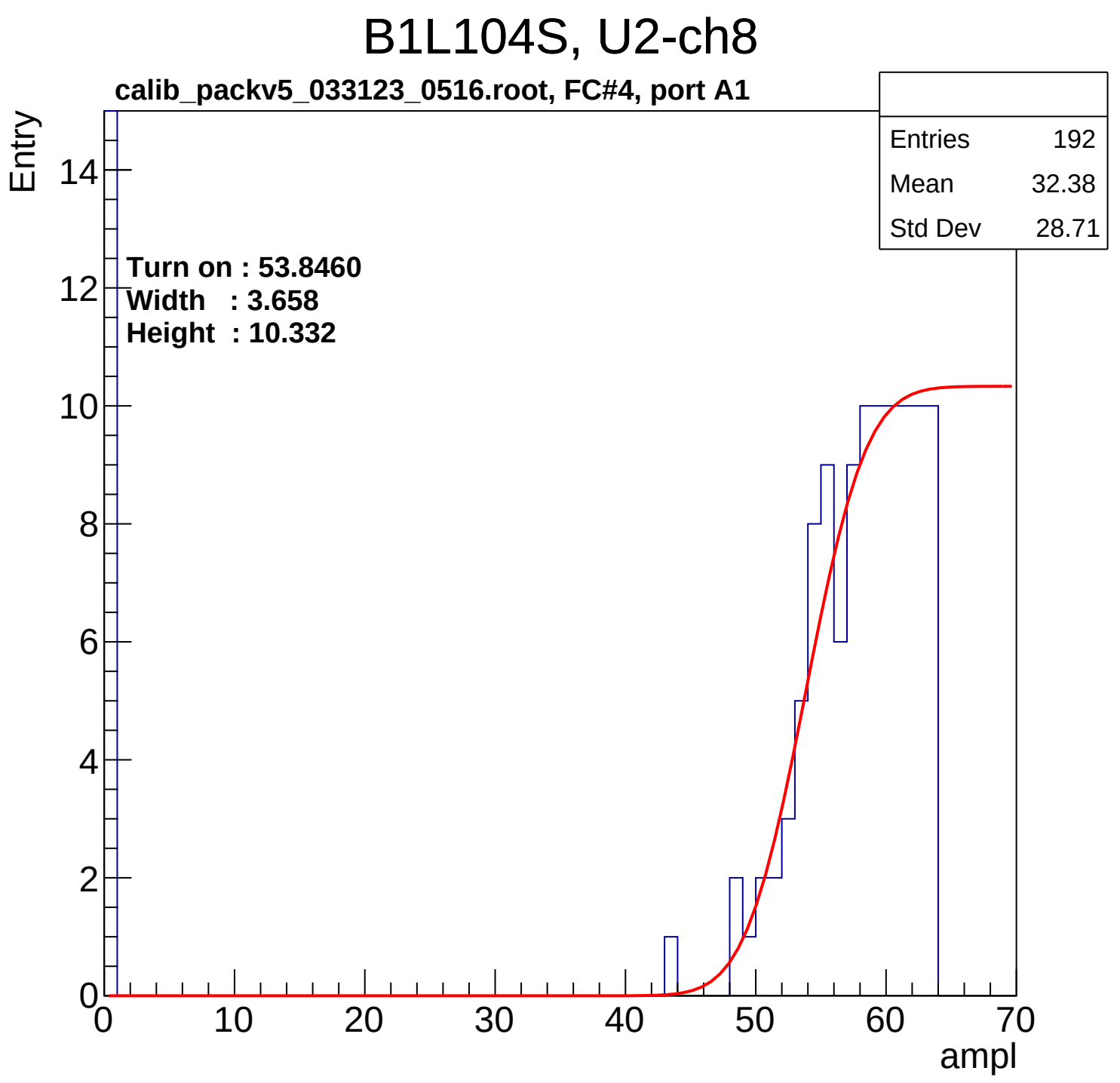
B1L104S, U2-ch8
calib_packv5_033123_0516.root, FC#4, port A1
Entries 192
Mean 32.38
Std Dev 28.71
Turn on : 53.8460
Width : 3.658
Height : 10.332
Entry
ampl
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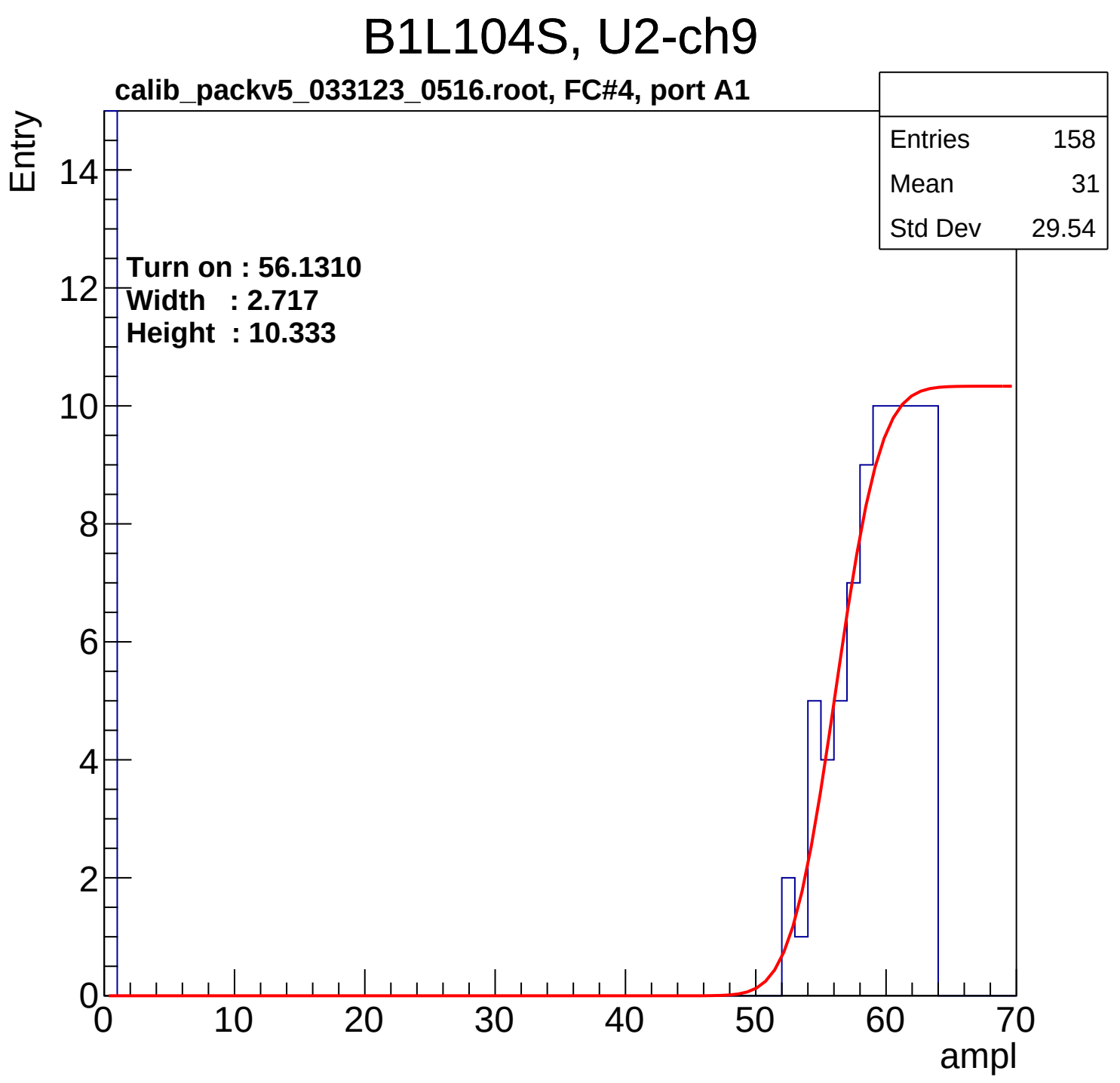
B1L104S, U2-ch9
calib_packv5_033123_0516.root, FC#4, port A1
Entries 158
Mean 31
Std Dev 29.54
Turn on : 56.1310
Width : 2.717
Height : 10.333
Entry
ampl
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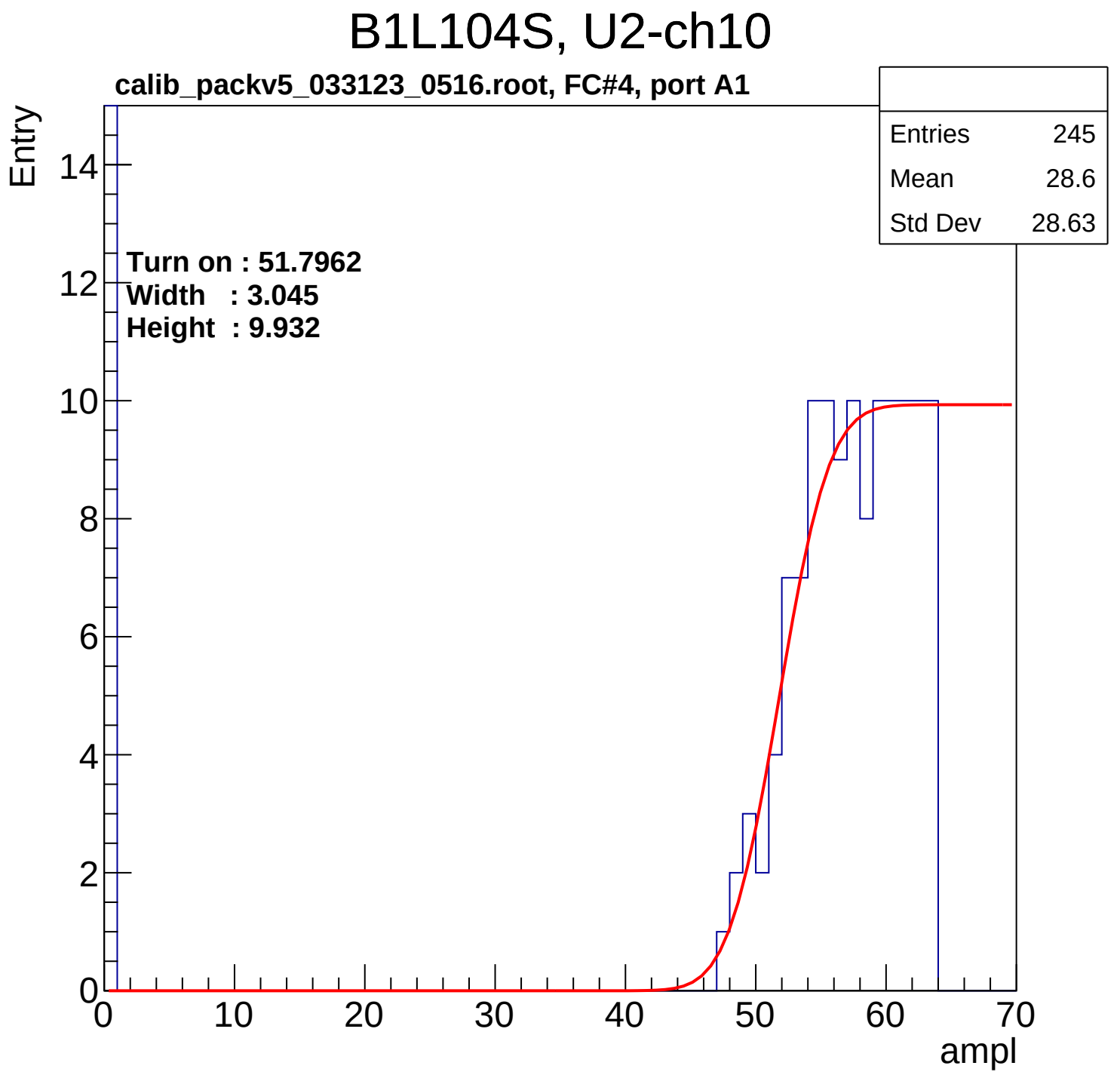
B1L104S, U2-ch10
calib_packv5_033123_0516.root, FC#4, port A1
Entries 245
Mean 28.6
Std Dev 28.63
Turn on : 51.7962
Width : 3.045
Height : 9.932
Entry
ampl
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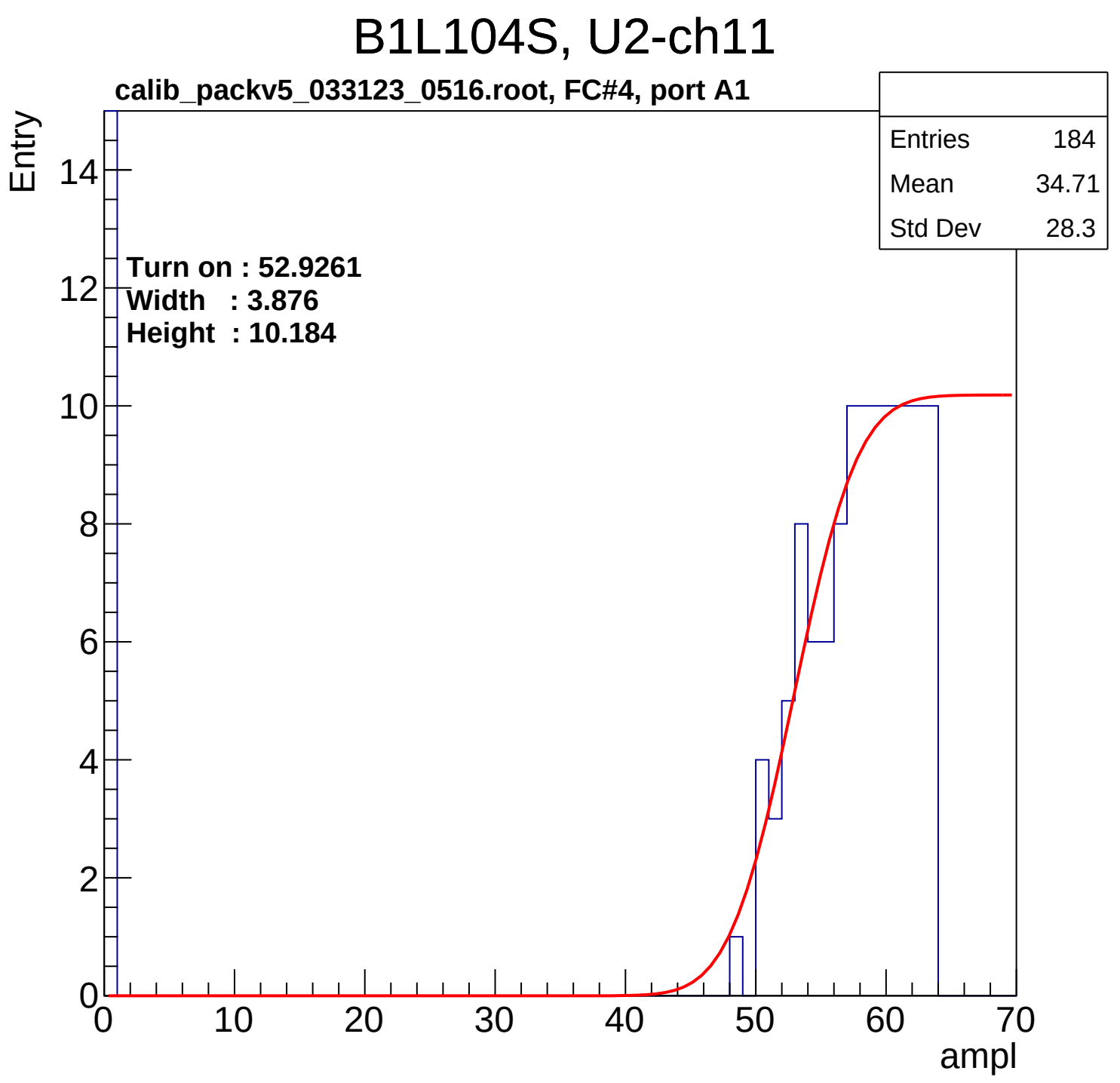
B1L104S, U2-ch11
calib_packv5_033123_0516.root, FC#4, port A1
Entries 184
Mean 34.71
Std Dev 28.3
Turn on : 52.9261
Width : 3.876
Height : 10.184
Entry
ampl
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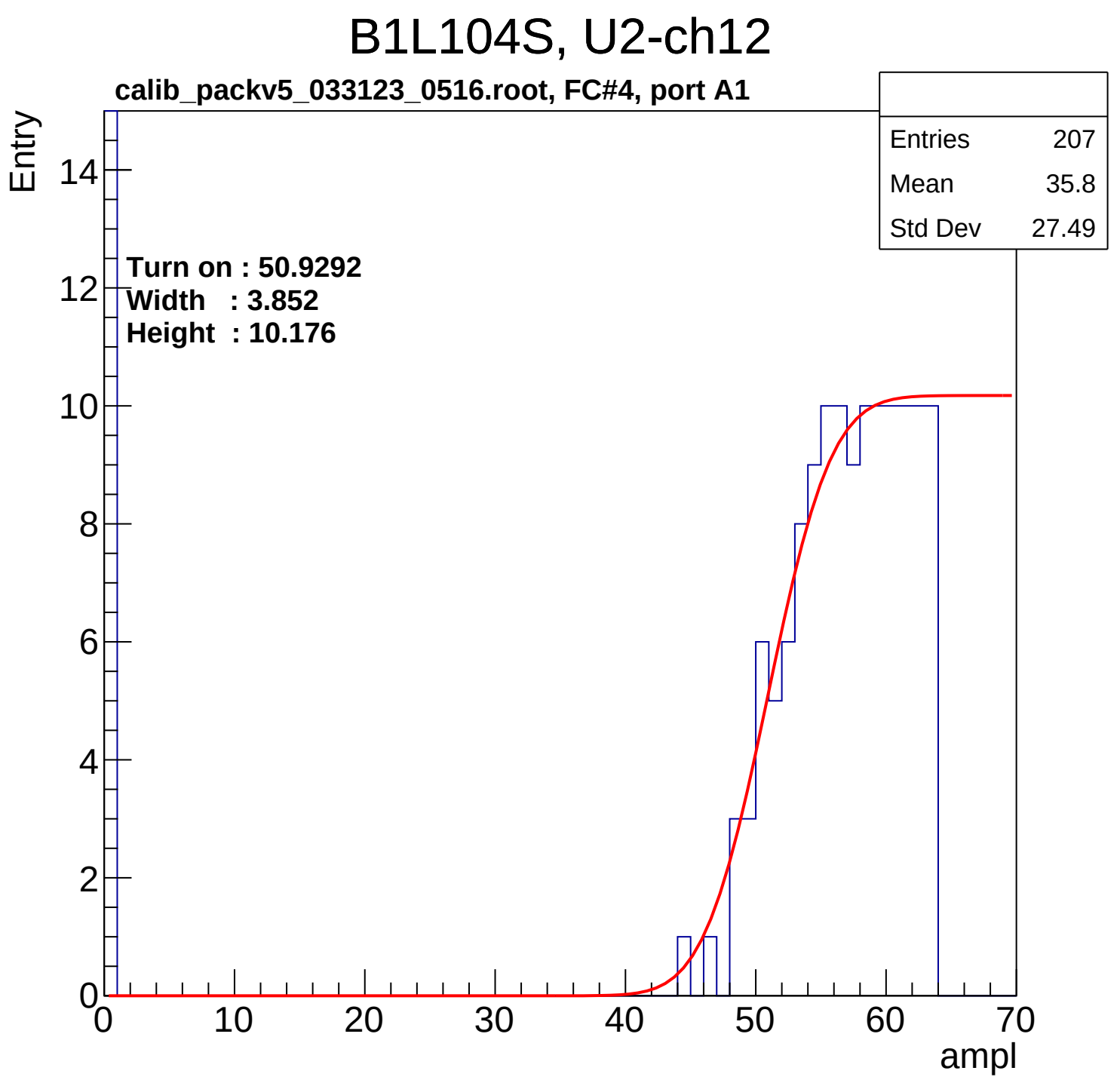
B1L104S, U2-ch12
calib_packv5_033123_0516.root, FC#4, port A1
Entries 207
Mean 35.8
Std Dev 27.49
Turn on : 50.9292
Width : 3.852
Height : 10.176
Entry
ampl
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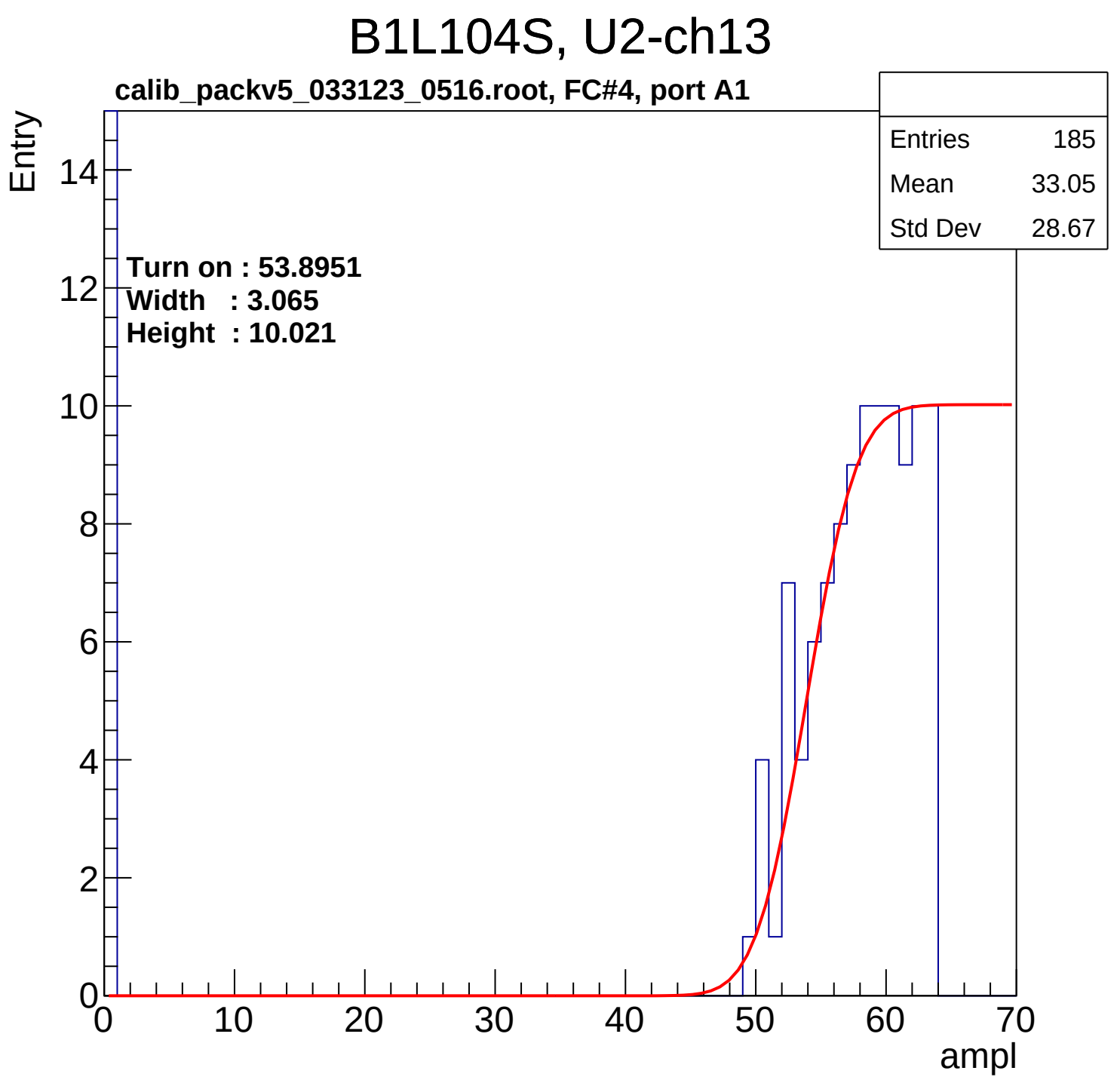
B1L104S, U2-ch13
calib_packv5_033123_0516.root, FC#4, port A1
Entries 185
Mean 33.05
Std Dev 28.67
Turn on : 53.8951
Width : 3.065
Height : 10.021
Entry
ampl
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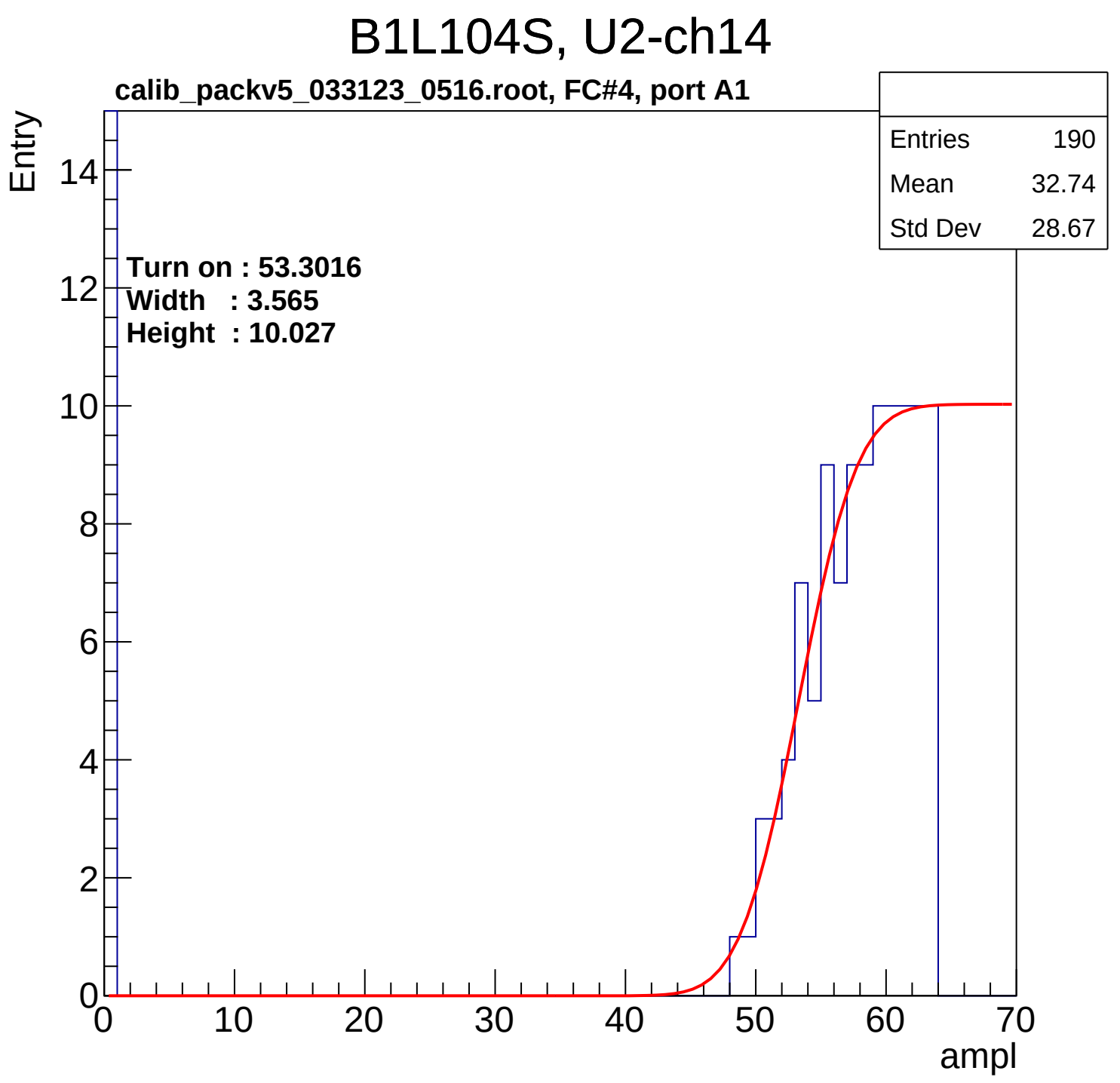
B1L104S, U2-ch14
calib_packv5_033123_0516.root, FC#4, port A1
Entries 190
Mean 32.74
Std Dev 28.67
Turn on : 53.3016
Width : 3.565
Height : 10.027
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ampl
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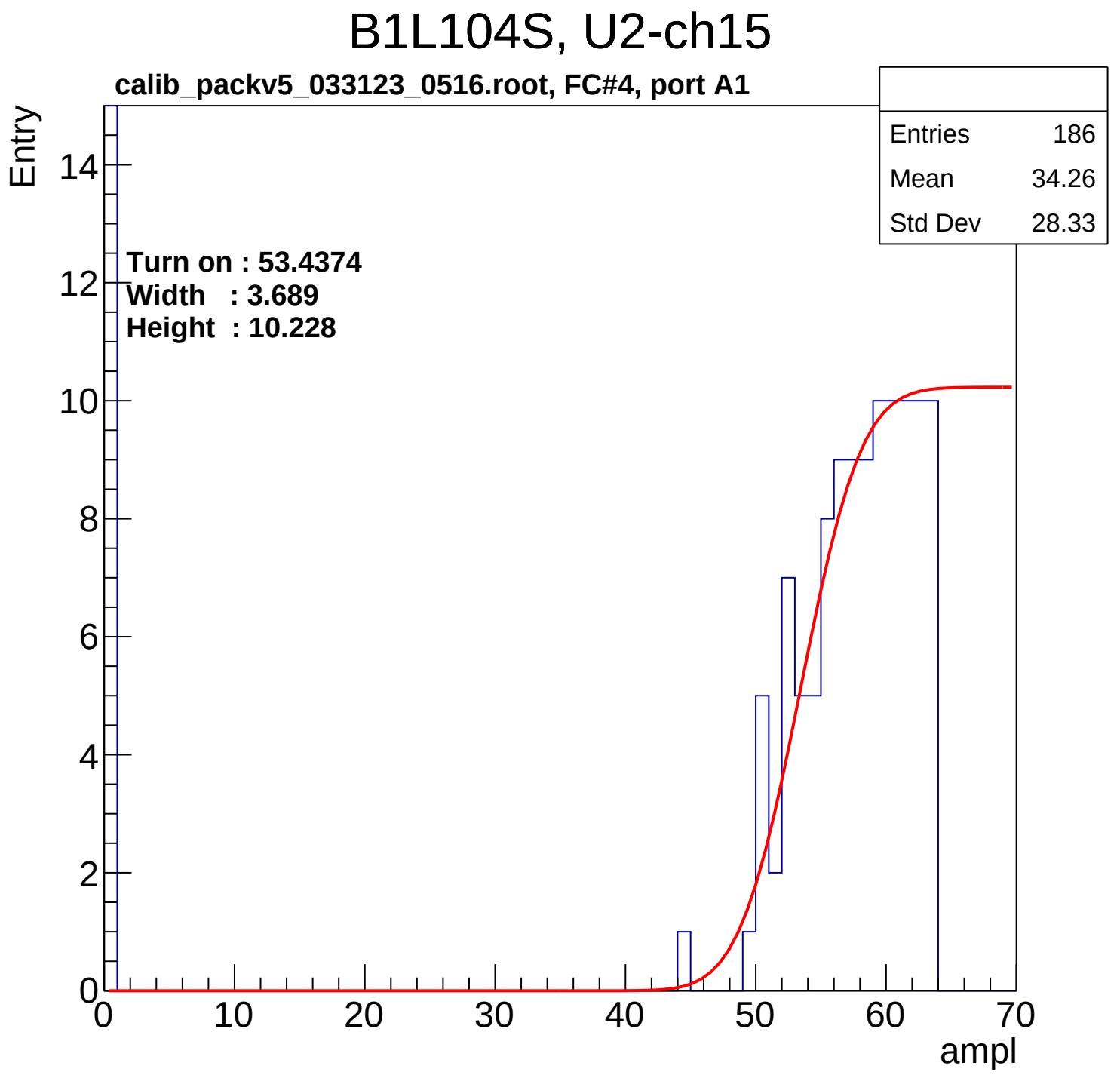
B1L104S, U2-ch15
calib_packv5_033123_0516.root, FC#4, port A1
Entries 186
Mean 34.26
Std Dev 28.33
Turn on : 53.4374
Width : 3.689
Height : 10.228
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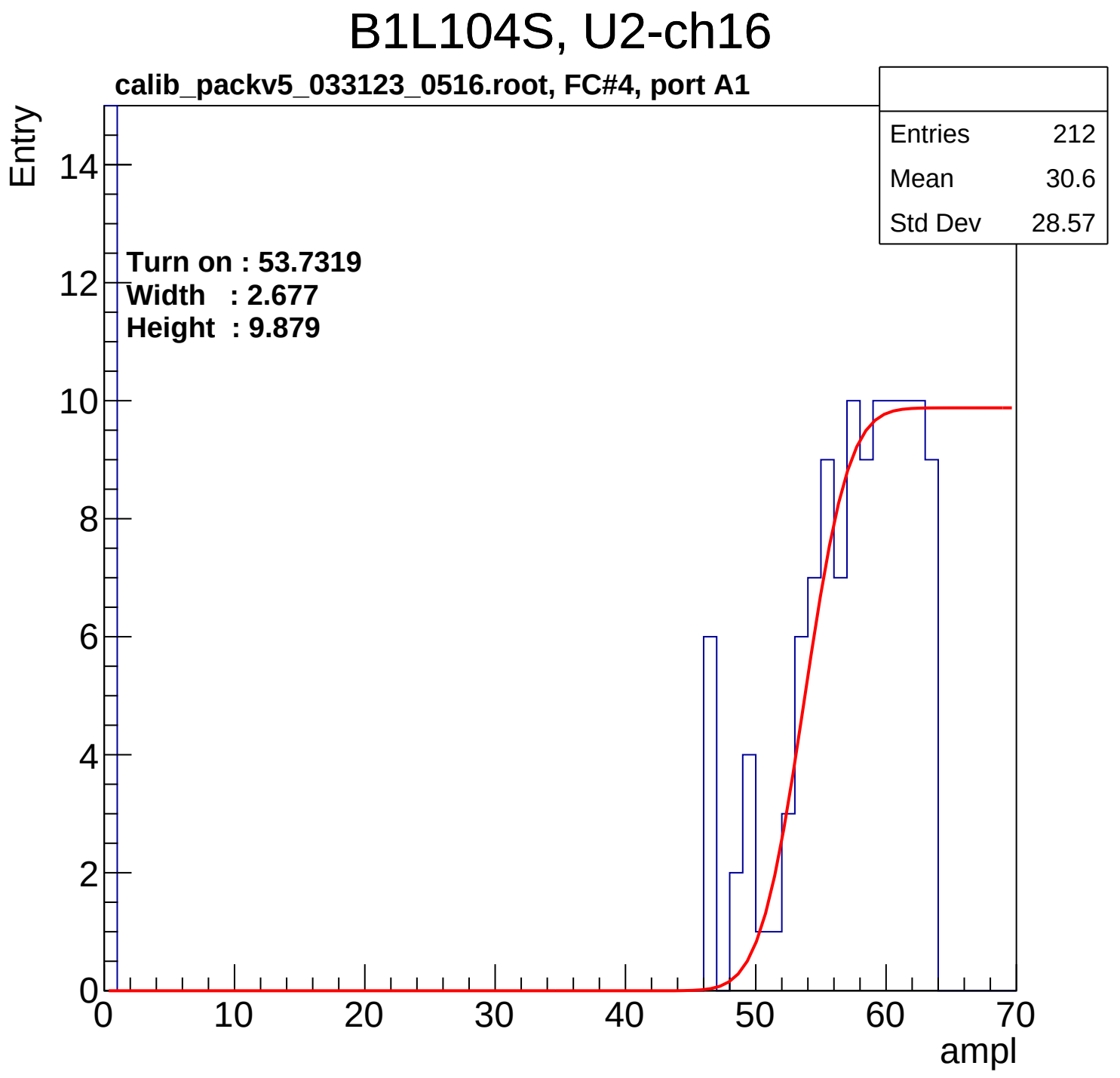
B1L104S, U2-ch16
calib_packv5_033123_0516.root, FC#4, port A1
Entries 212
Mean 30.6
Std Dev 28.57
Turn on : 53.7319
Width : 2.677
Height : 9.879
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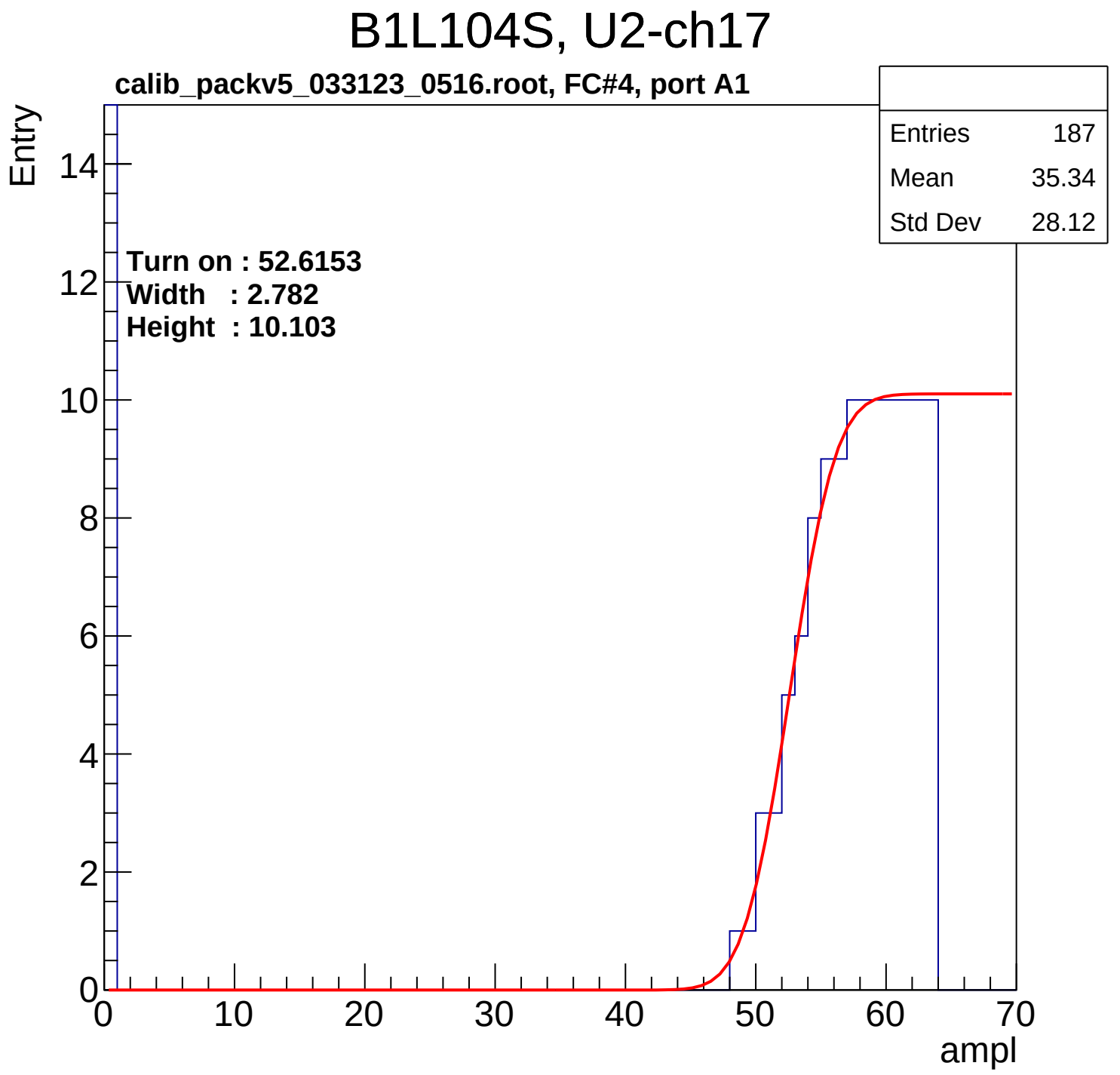
B1L104S, U2-ch17
calib_packv5_033123_0516.root, FC#4, port A1
Entries 187
Mean 35.34
Std Dev 28.12
Turn on : 52.6153
Width : 2.782
Height : 10.103
Entry
ampl
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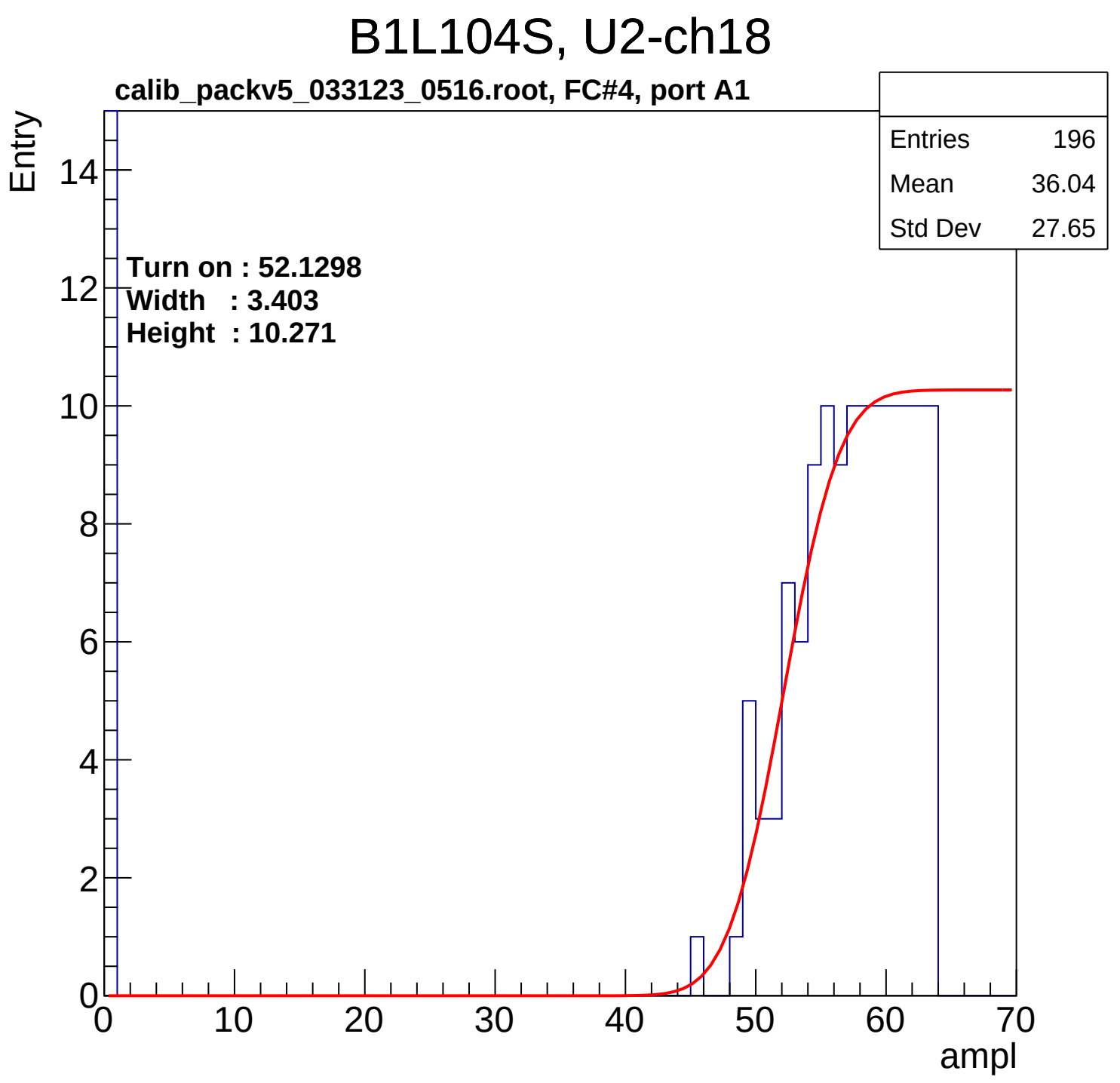
B1L104S, U2-ch18
calib_packv5_033123_0516.root, FC#4, port A1
Entries 196
Mean 36.04
Std Dev 27.65
Turn on : 52.1298
Width : 3.403
Height : 10.271
Entry
ampl
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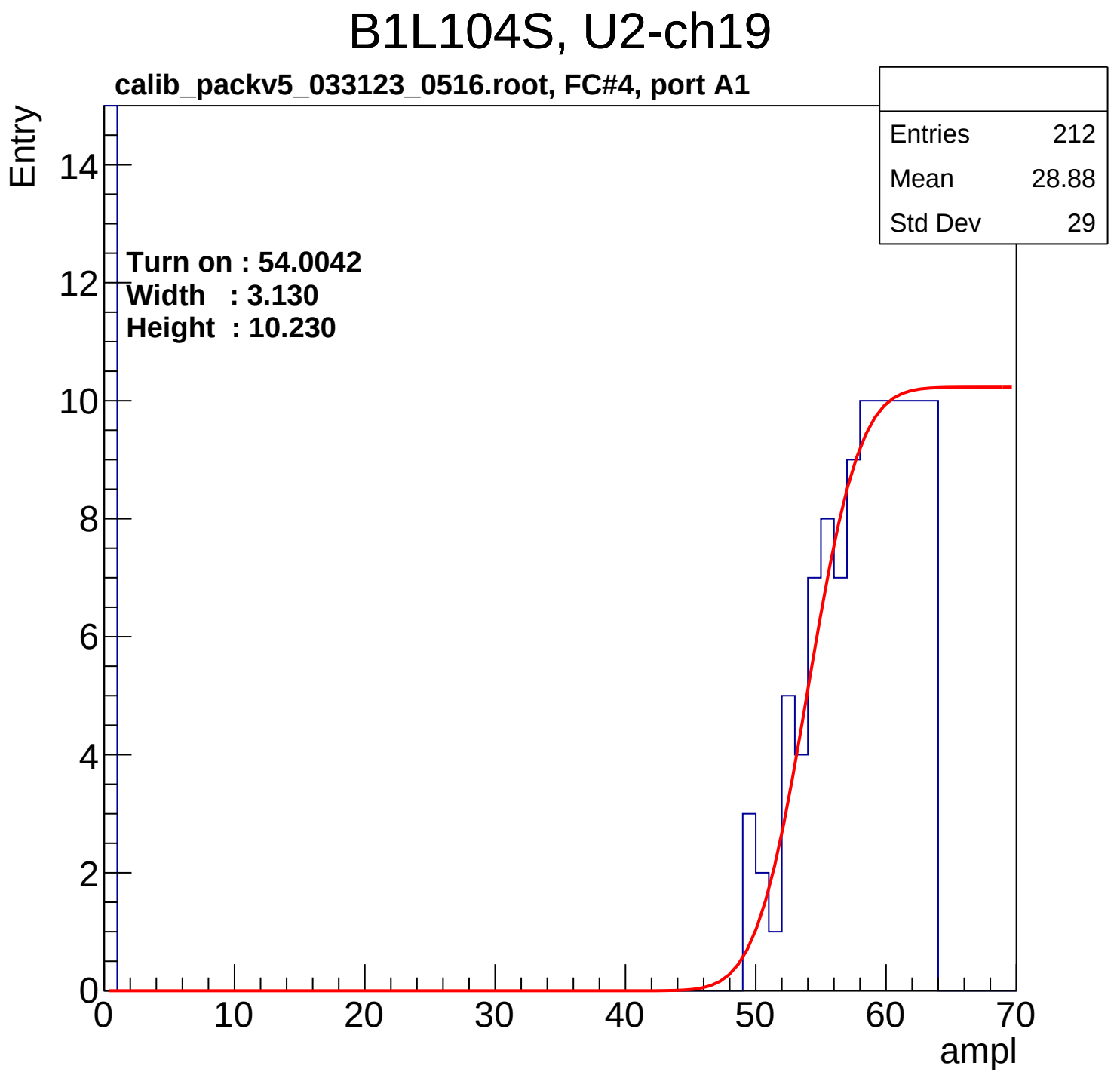
B1L104S, U2-ch19
calib_packv5_033123_0516.root, FC#4, port A1
Entries 212
Mean 28.88
Std Dev 29
Turn on : 54.0042
Width : 3.130
Height : 10.230
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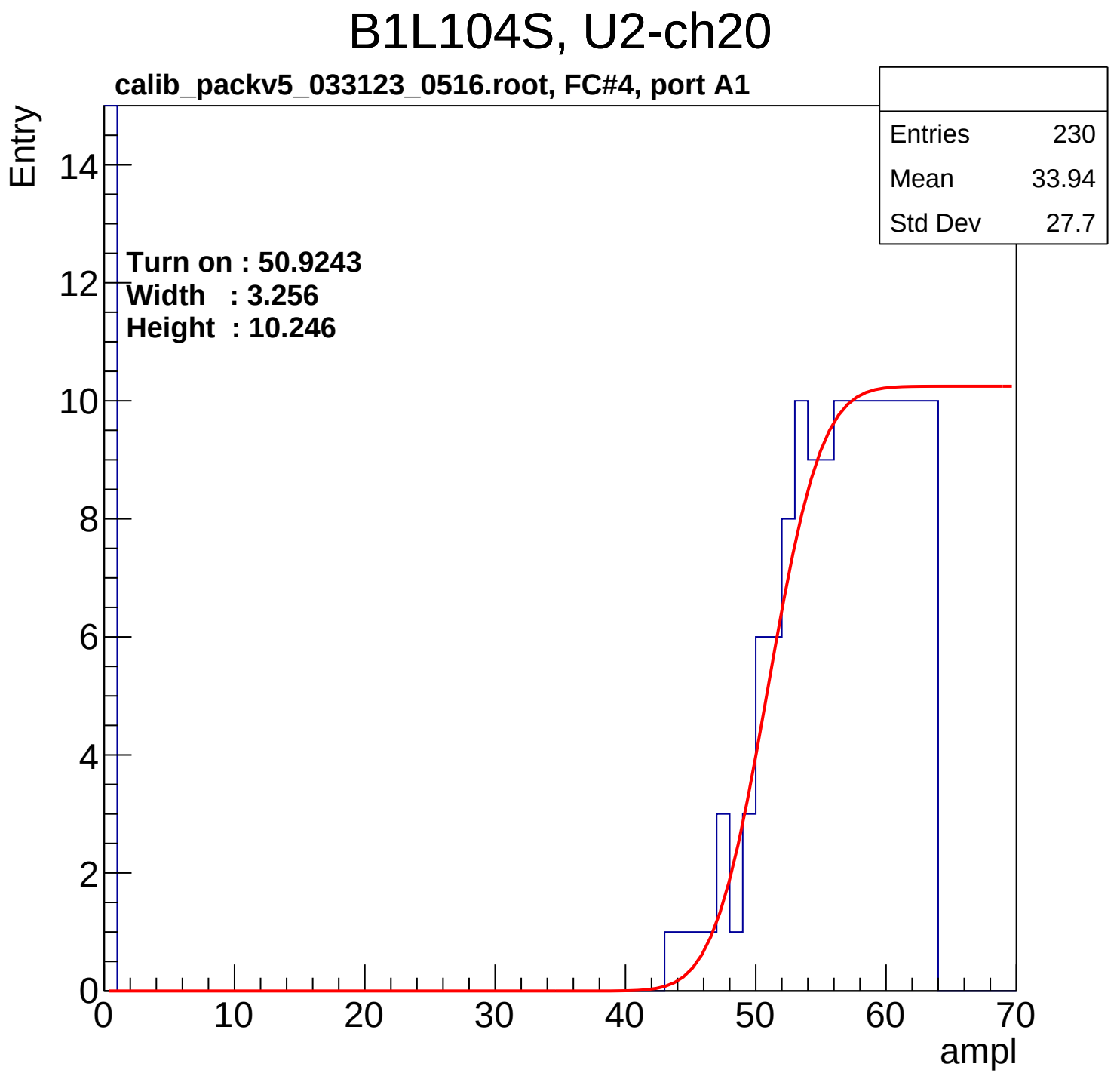
B1L104S, U2-ch20
calib_packv5_033123_0516.root, FC#4, port A1
Entries 230
Mean 33.94
Std Dev 27.7
Turn on : 50.9243
Width : 3.256
Height : 10.246
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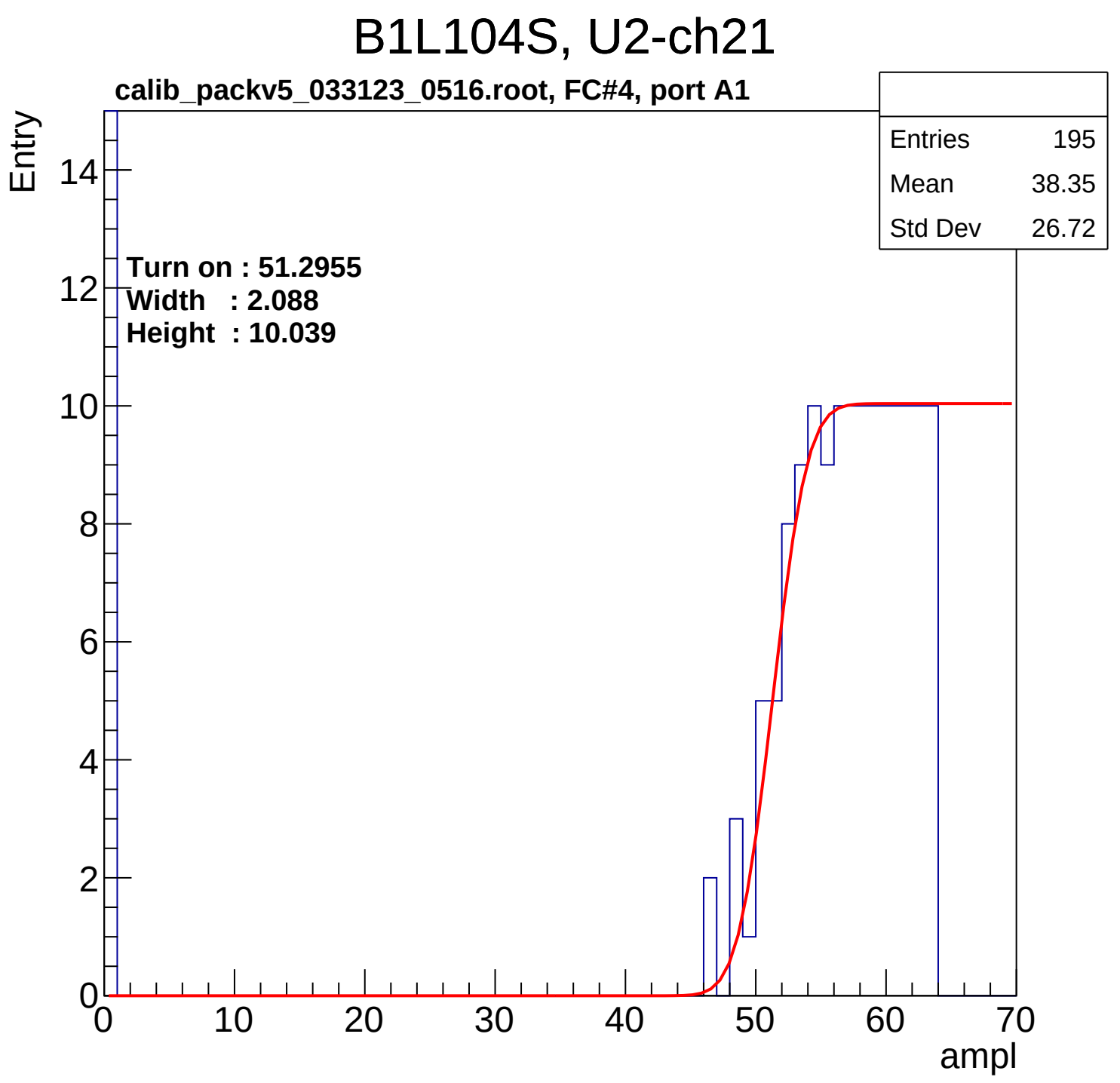
B1L104S, U2-ch21
calib_packv5_033123_0516.root, FC#4, port A1
Entries 195
Mean 38.35
Std Dev 26.72
Turn on : 51.2955
Width : 2.088
Height : 10.039
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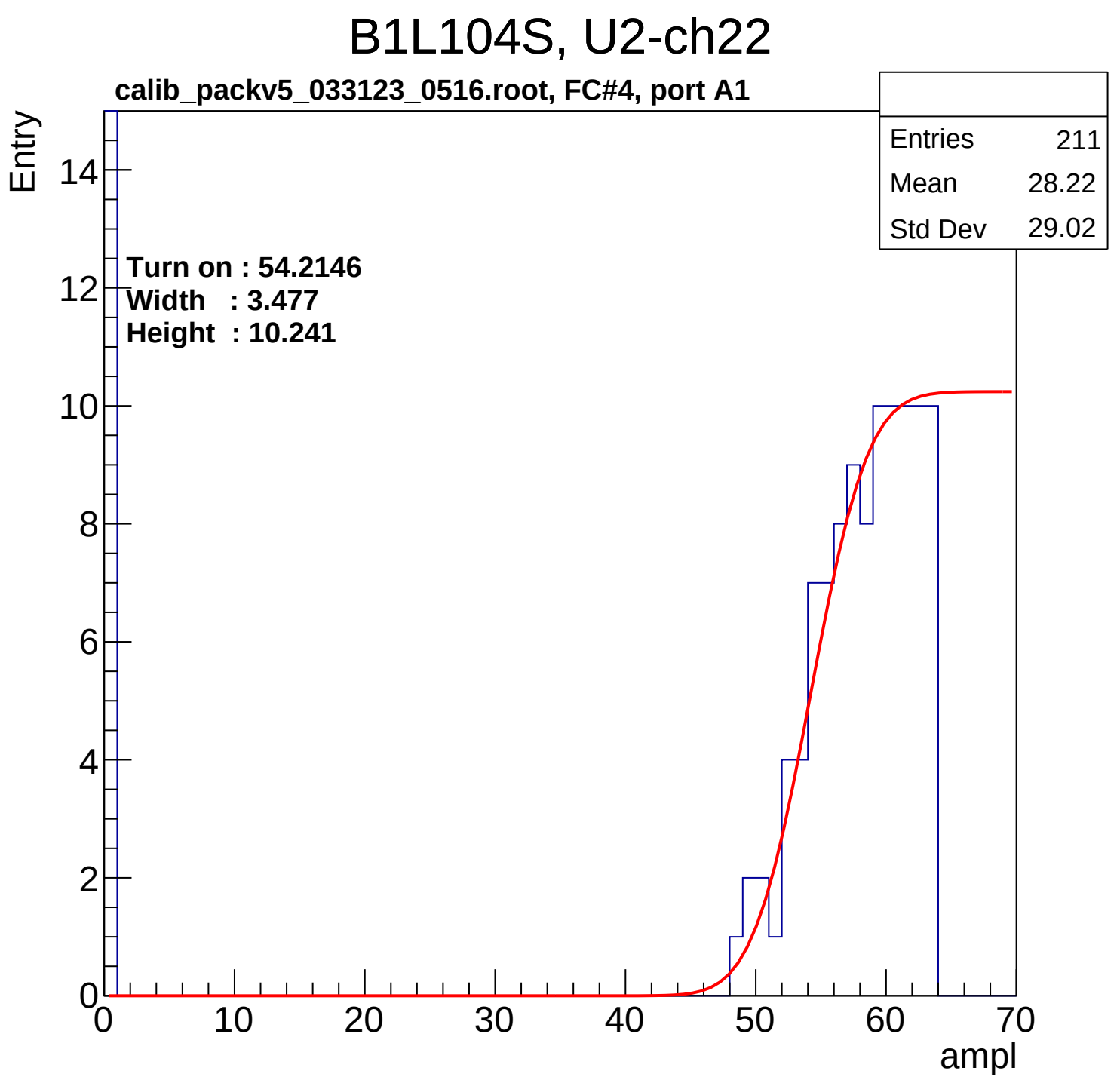
B1L104S, U2-ch22
calib_packv5_033123_0516.root, FC#4, port A1
Entries 211
Mean 28.22
Std Dev 29.02
Turn on : 54.2146
Width : 3.477
Height : 10.241
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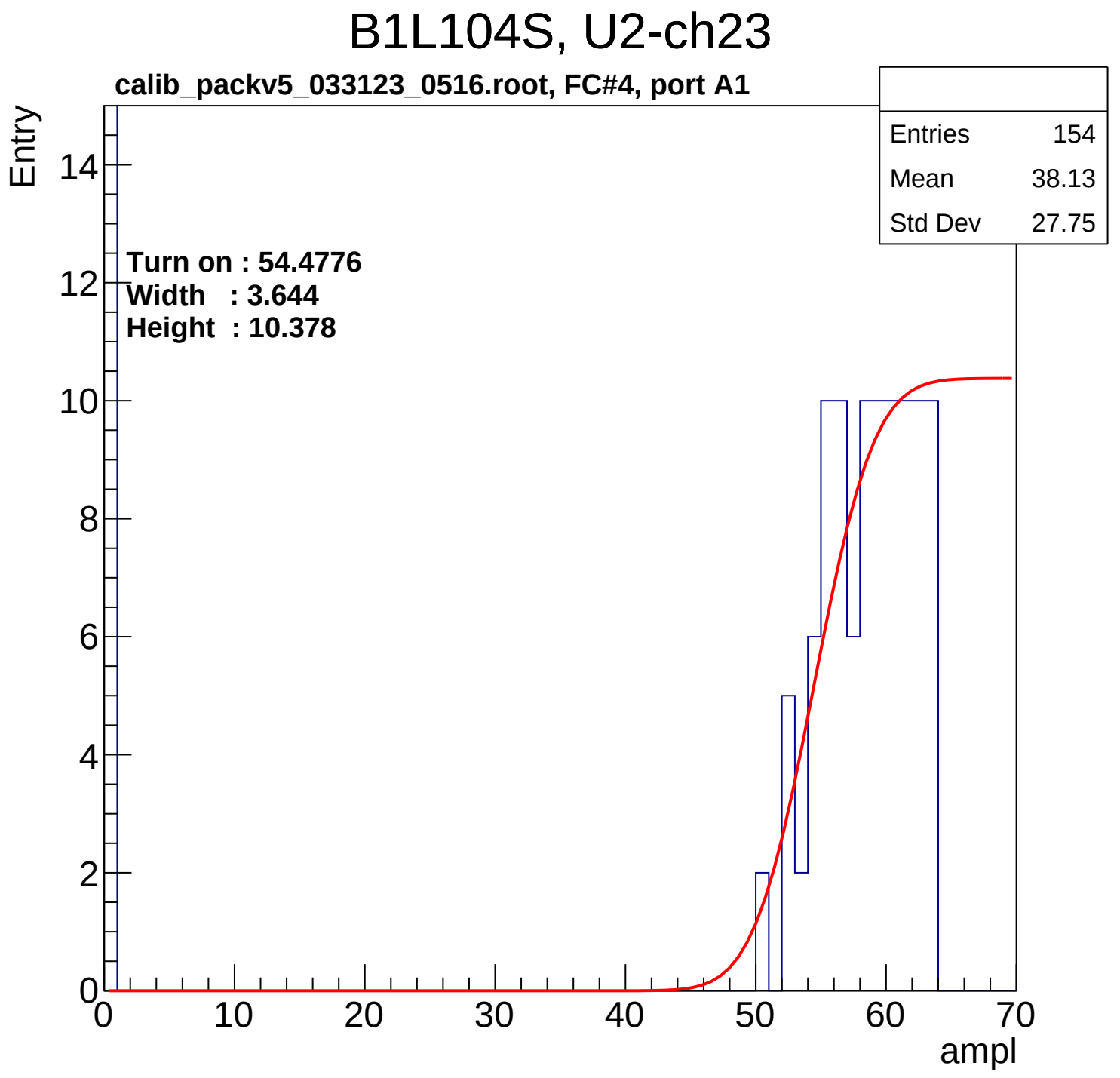
B1L104S, U2-ch23
calib_packv5_033123_0516.root, FC#4, port A1
Entries 154
Mean 38.13
Std Dev 27.75
Turn on : 54.4776
Width : 3.644
Height : 10.378
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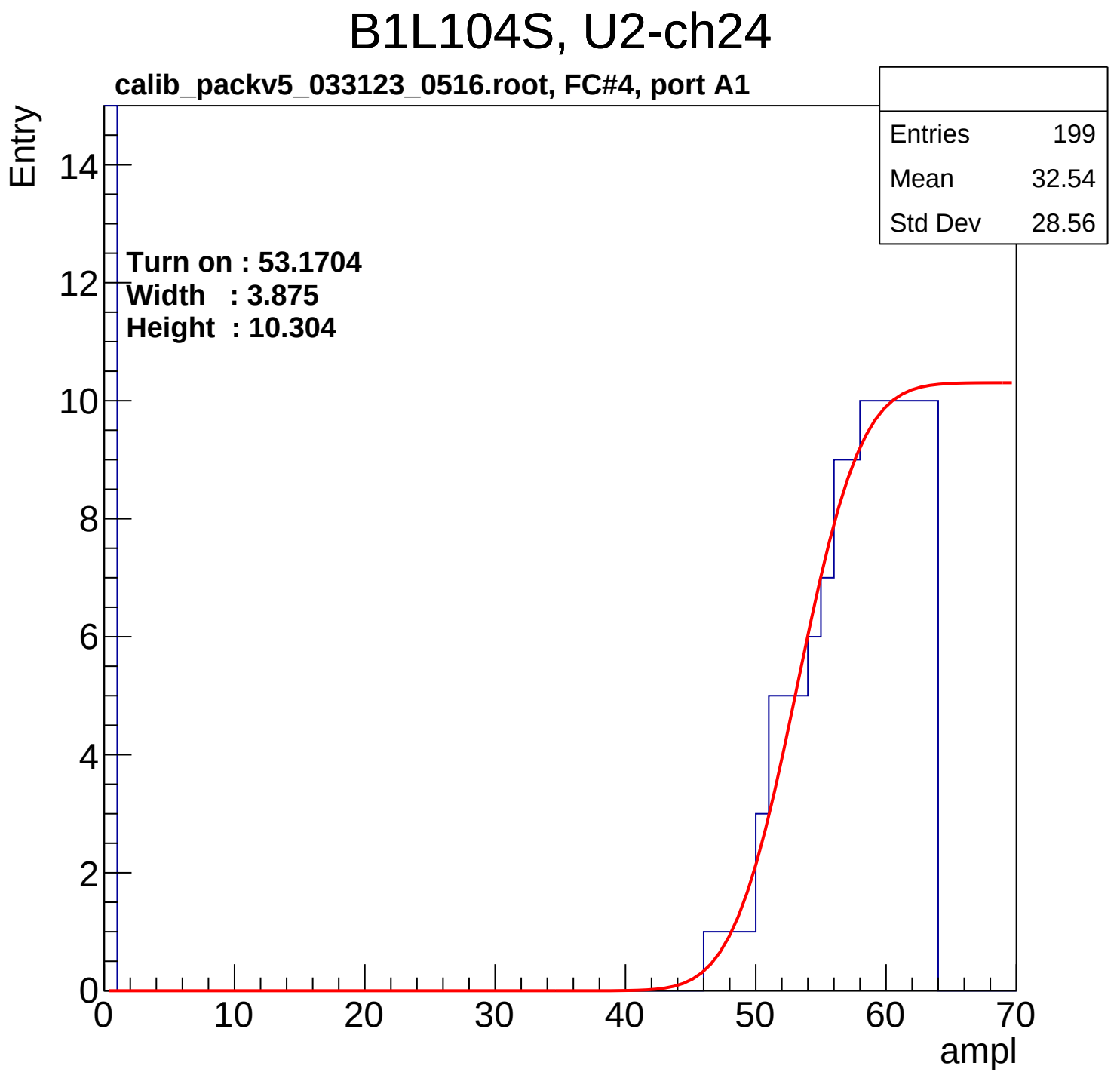
B1L104S, U2-ch24
calib_packv5_033123_0516.root, FC#4, port A1
Entries 199
Mean 32.54
Std Dev 28.56
Turn on : 53.1704
Width : 3.875
Height : 10.304
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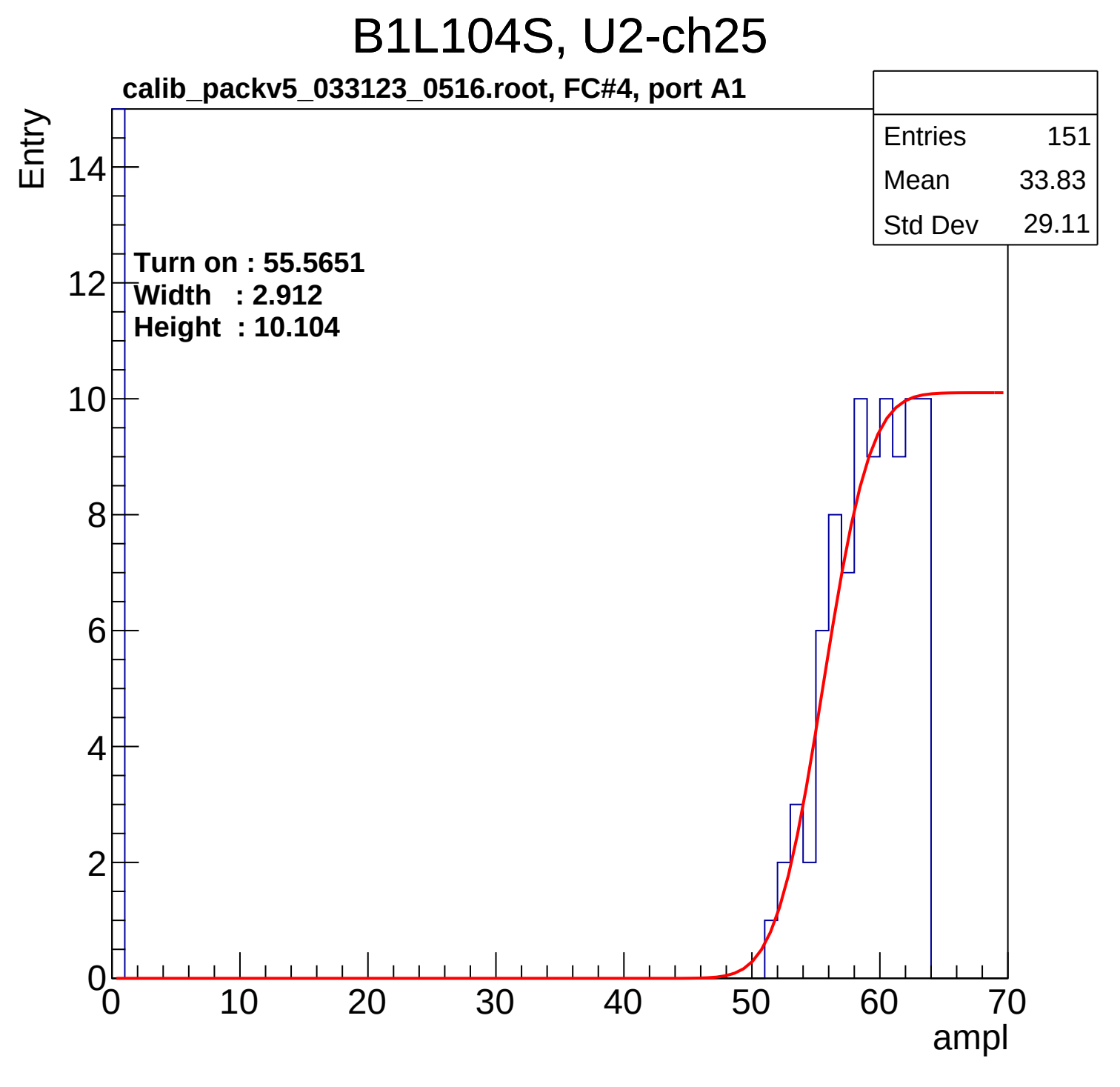
B1L104S, U2-ch25
calib_packv5_033123_0516.root, FC#4, port A1
Entries 151
Mean 33.83
Std Dev 29.11
Turn on : 55.5651
Width : 2.912
Height : 10.104
Entry
ampl
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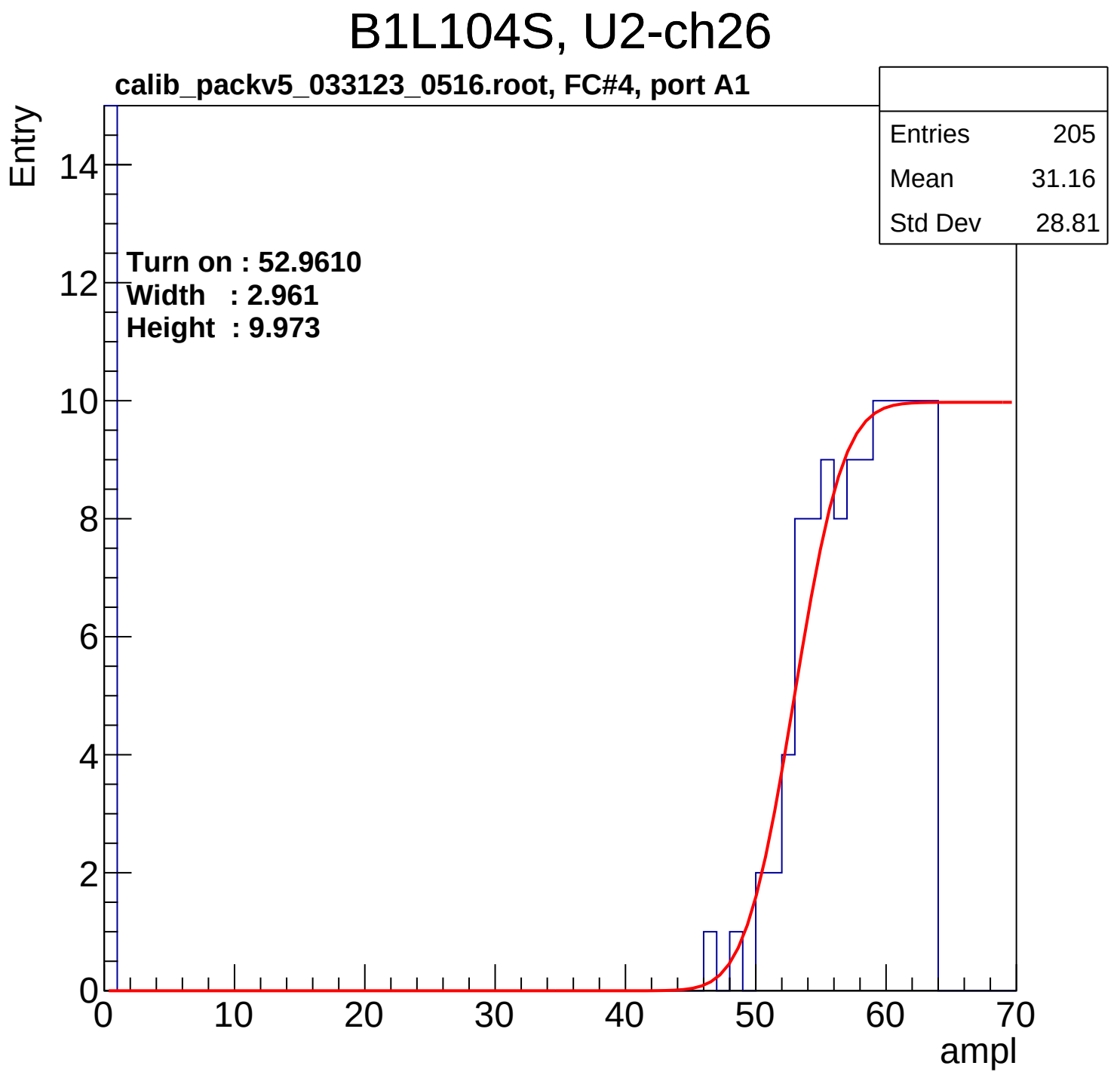
B1L104S, U2-ch26
calib_packv5_033123_0516.root, FC#4, port A1
Entries 205
Mean 31.16
Std Dev 28.81
Turn on : 52.9610
Width : 2.961
Height : 9.973
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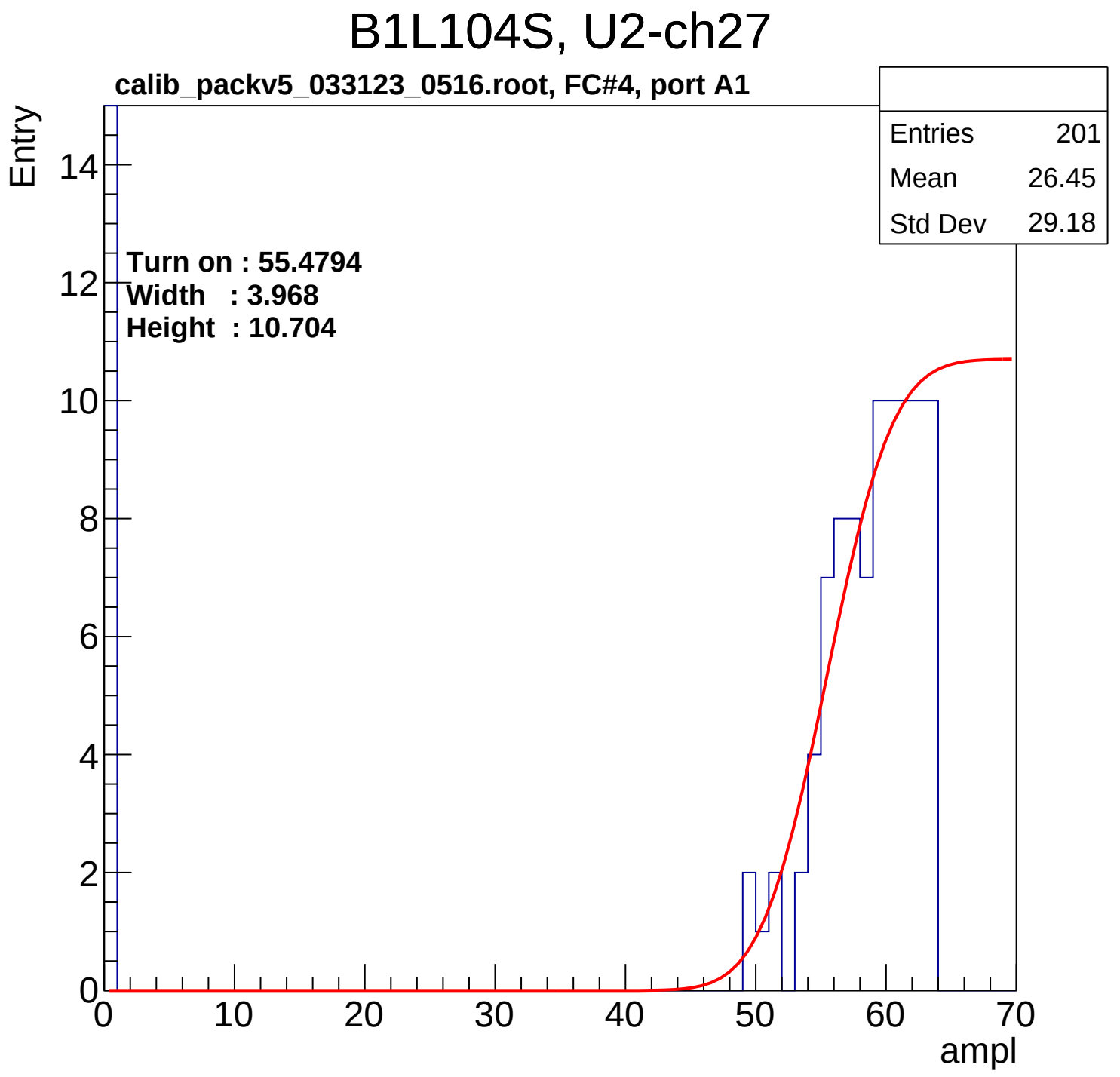
B1L104S, U2-ch27
calib_packv5_033123_0516.root, FC#4, port A1
Entries 201
Mean 26.45
Std Dev 29.18
Turn on : 55.4794
Width : 3.968
Height : 10.704
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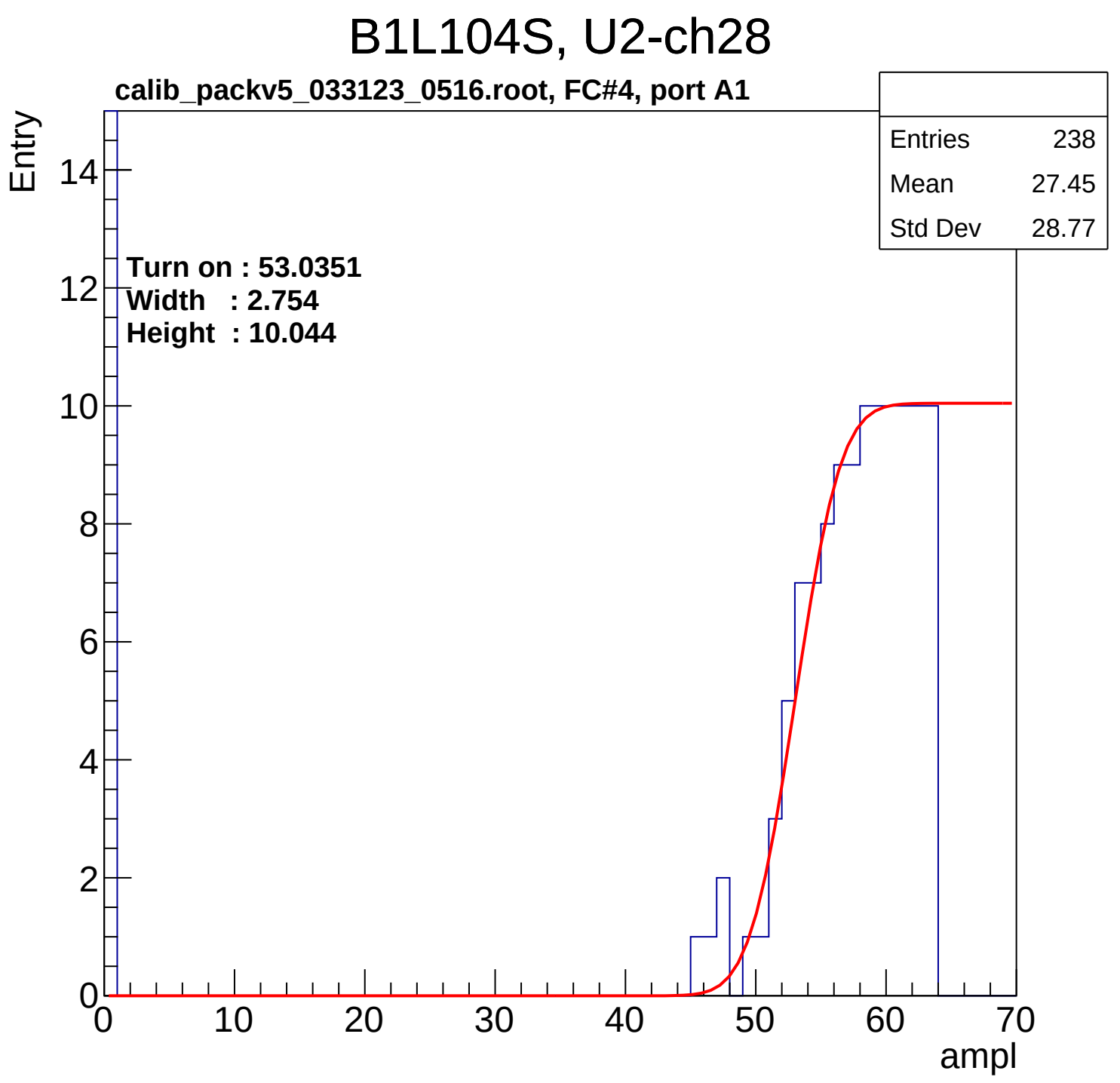
B1L104S, U2-ch28
calib_packv5_033123_0516.root, FC#4, port A1
Entries 238
Mean 27.45
Std Dev 28.77
Turn on : 53.0351
Width : 2.754
Height : 10.044
Entry
ampl
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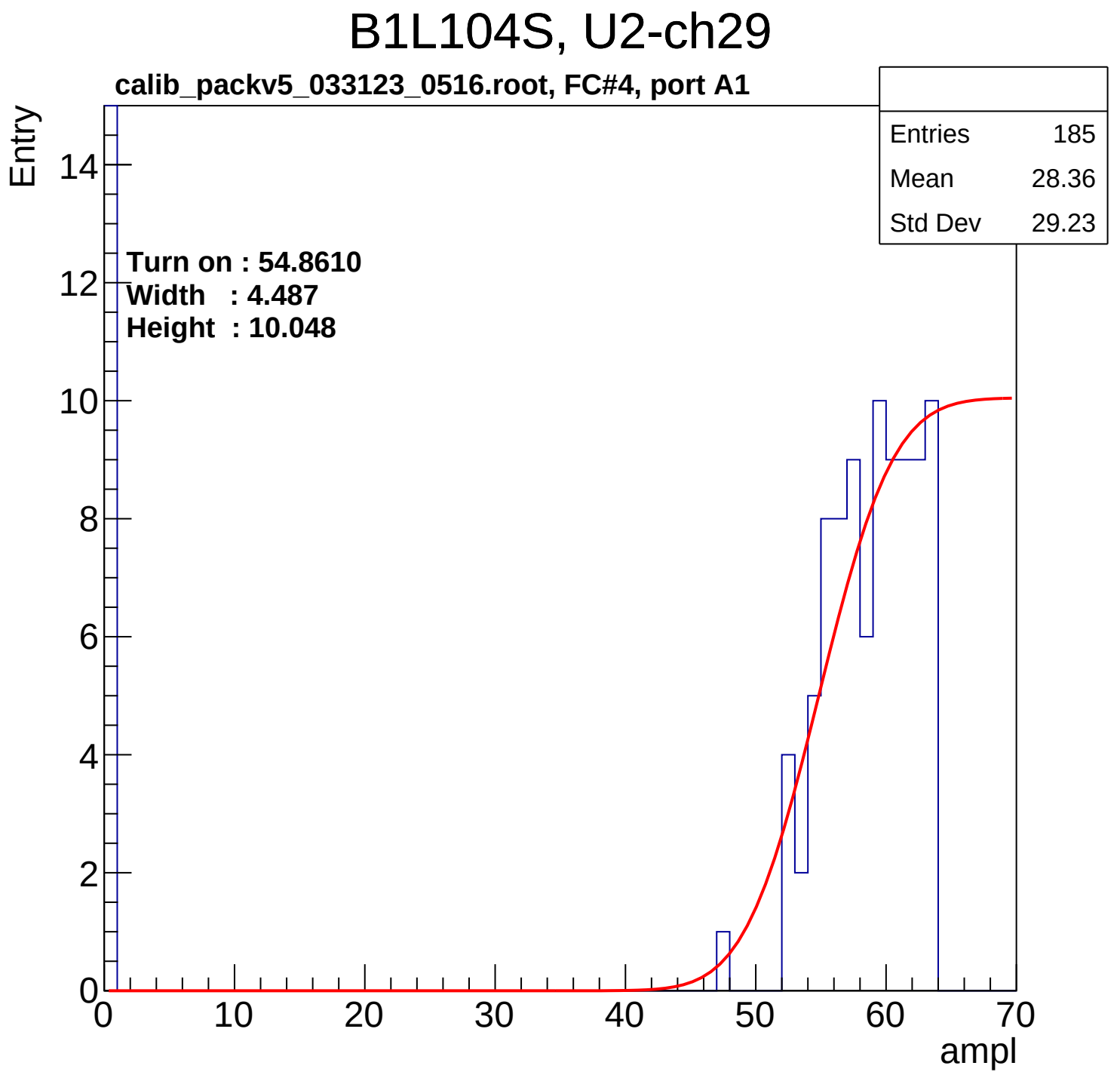
B1L104S, U2-ch29
calib_packv5_033123_0516.root, FC#4, port A1
Entries 185
Mean 28.36
Std Dev 29.23
Turn on : 54.8610
Width : 4.487
Height : 10.048
Entry
ampl
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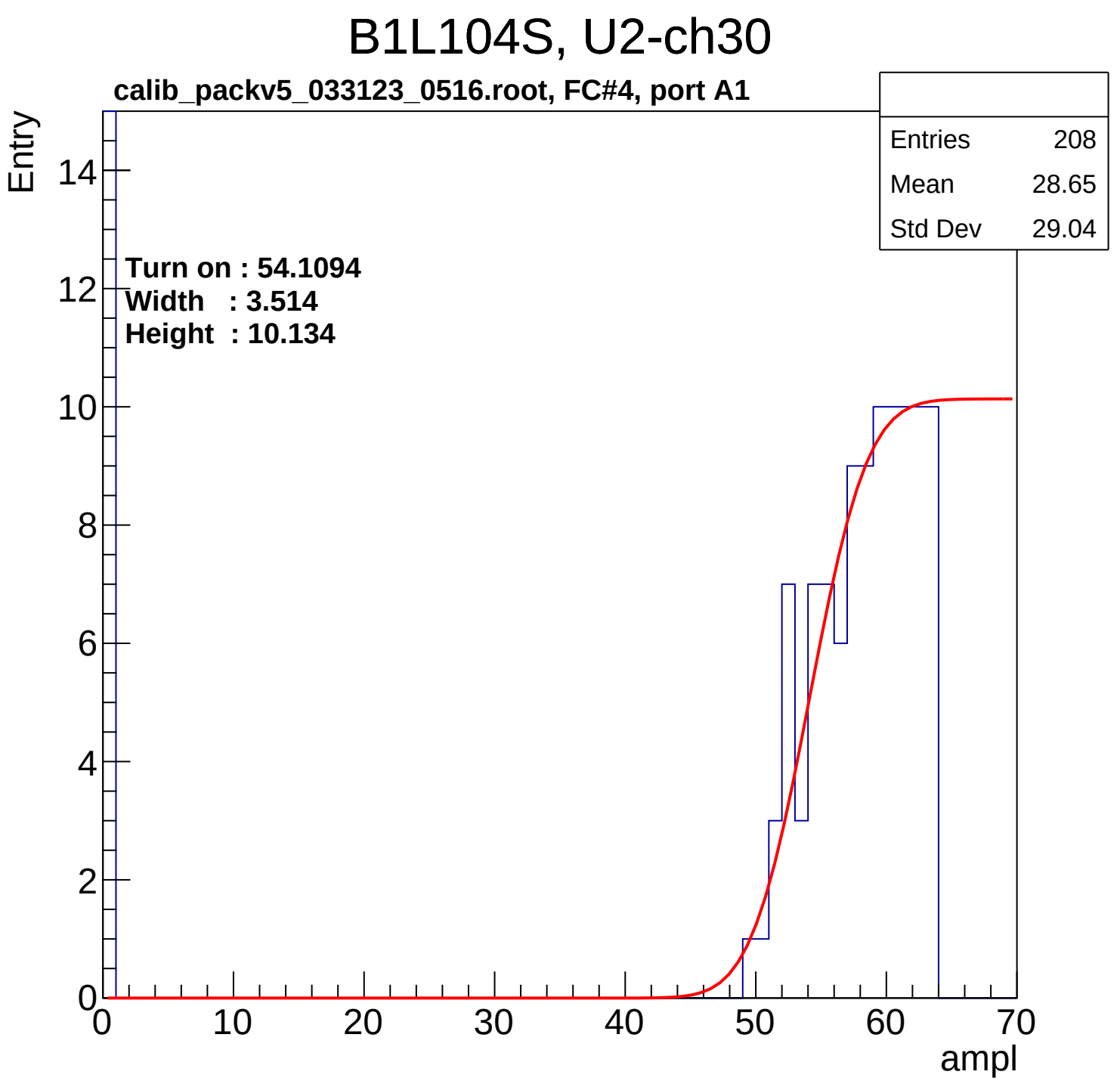
B1L104S, U2-ch30
calib_packv5_033123_0516.root, FC#4, port A1
Entries 208
Mean 28.65
Std Dev 29.04
Turn on : 54.1094
Width : 3.514
Height : 10.134
Entry
ampl
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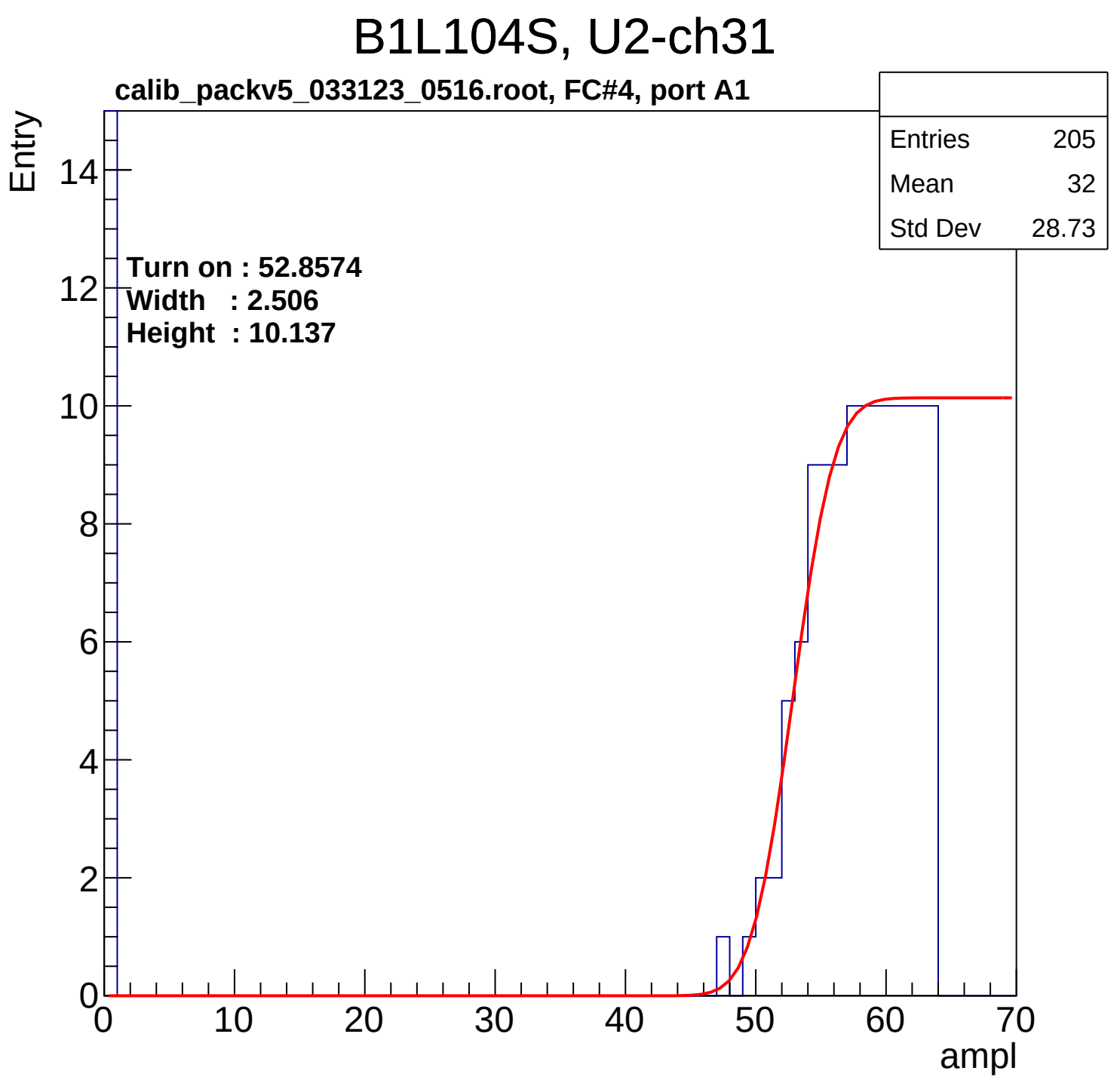
B1L104S, U2-ch31
calib_packv5_033123_0516.root, FC#4, port A1
Entries 205
Mean 32
Std Dev 28.73
Turn on : 52.8574
Width : 2.506
Height : 10.137
Entry
ampl
0
2
4
6
8
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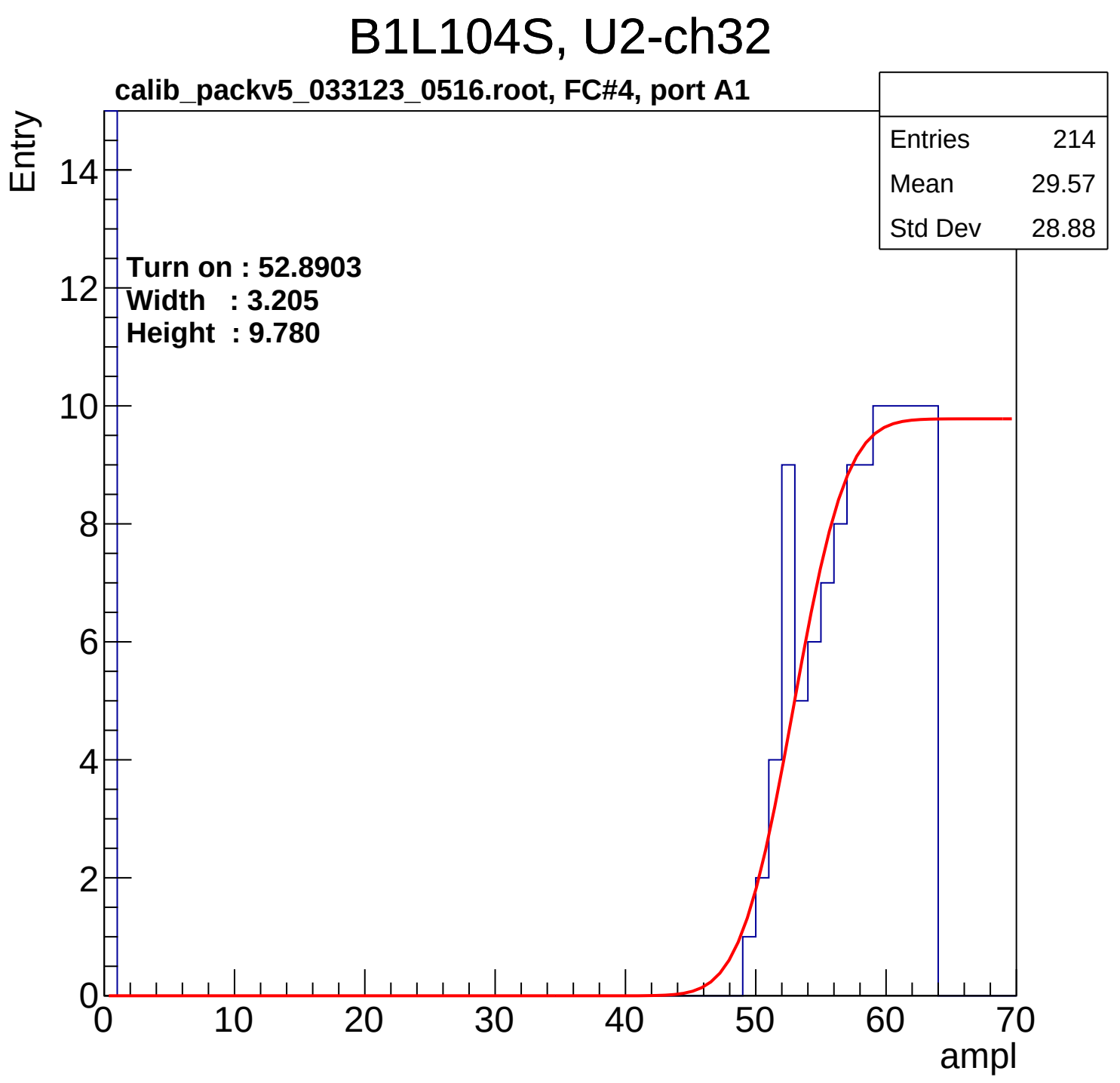
B1L104S, U2-ch32
calib_packv5_033123_0516.root, FC#4, port A1
Entries 214
Mean 29.57
Std Dev 28.88
Turn on : 52.8903
Width : 3.205
Height : 9.780
Entry
ampl
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2
4
6
8
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12
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0
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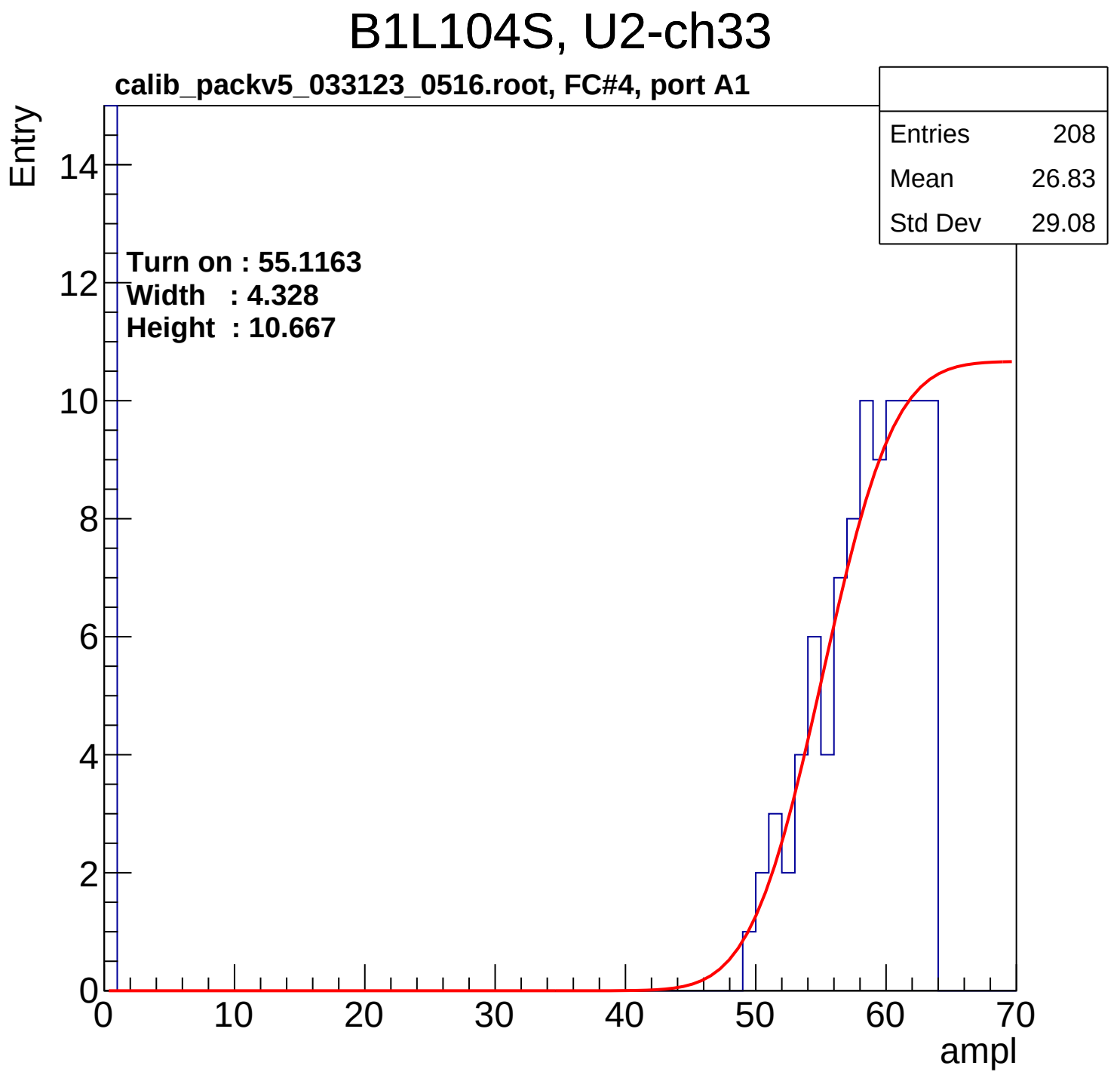
B1L104S, U2-ch33
calib_packv5_033123_0516.root, FC#4, port A1
Entries 208
Mean 26.83
Std Dev 29.08
Turn on : 55.1163
Width : 4.328
Height : 10.667
Entry
ampl
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2
4
6
8
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12
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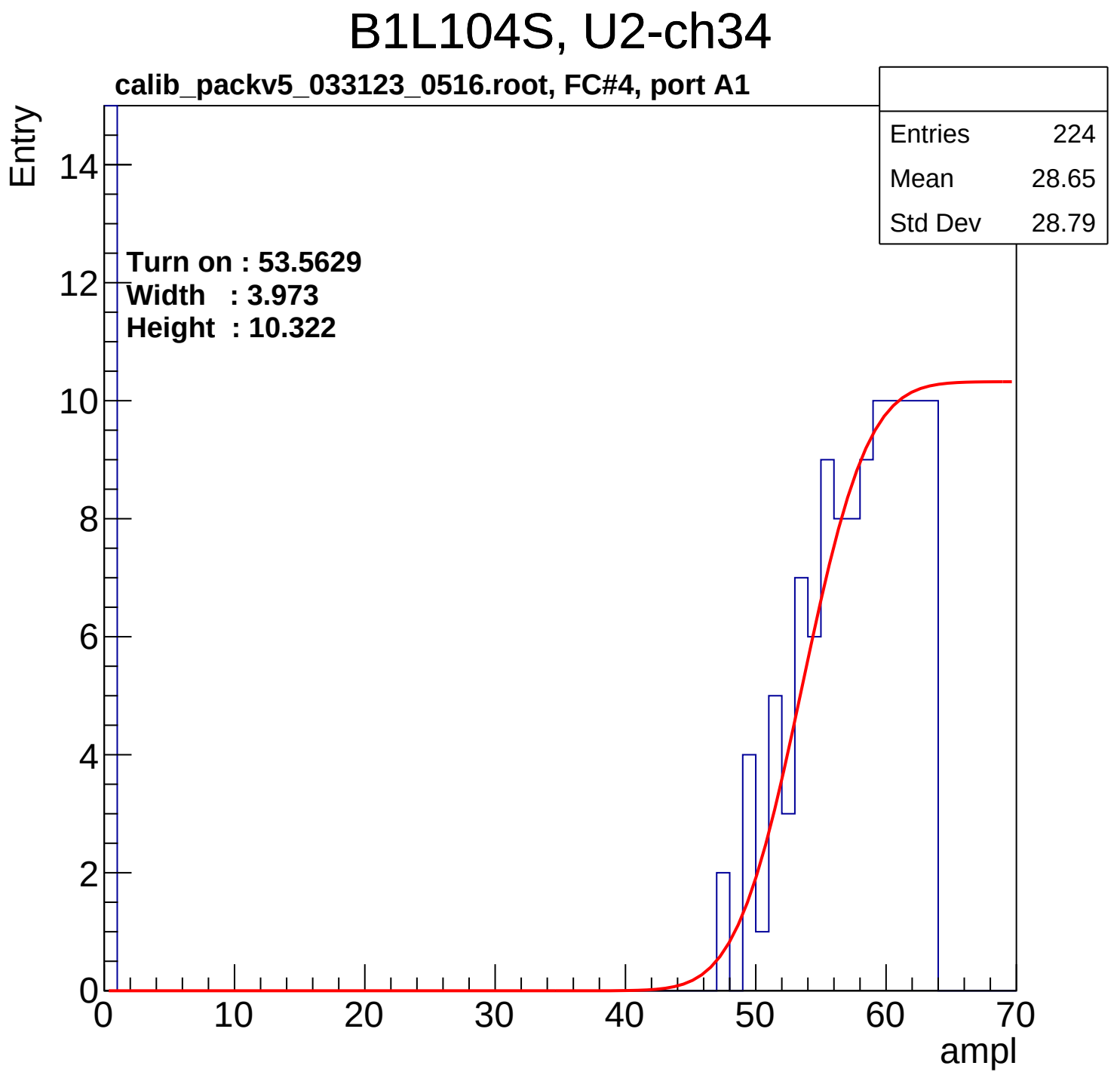
B1L104S, U2-ch34
calib_packv5_033123_0516.root, FC#4, port A1
Entries 224
Mean 28.65
Std Dev 28.79
Turn on : 53.5629
Width : 3.973
Height : 10.322
Entry
ampl
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2
4
6
8
10
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0
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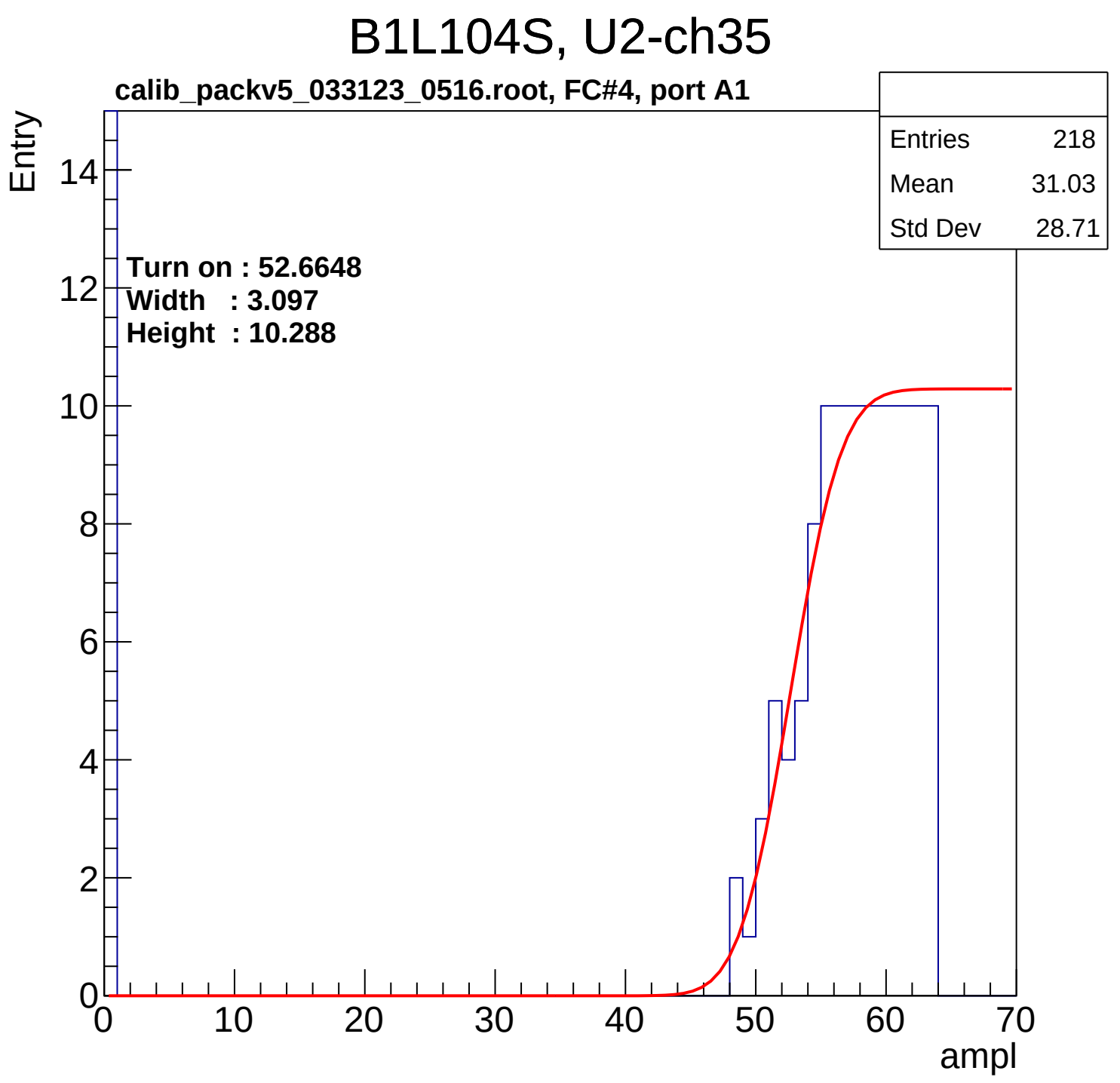
B1L104S, U2-ch35
calib_packv5_033123_0516.root, FC#4, port A1
Entries 218
Mean 31.03
Std Dev 28.71
Turn on : 52.6648
Width : 3.097
Height : 10.288
Entry
ampl
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2
4
6
8
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12
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0
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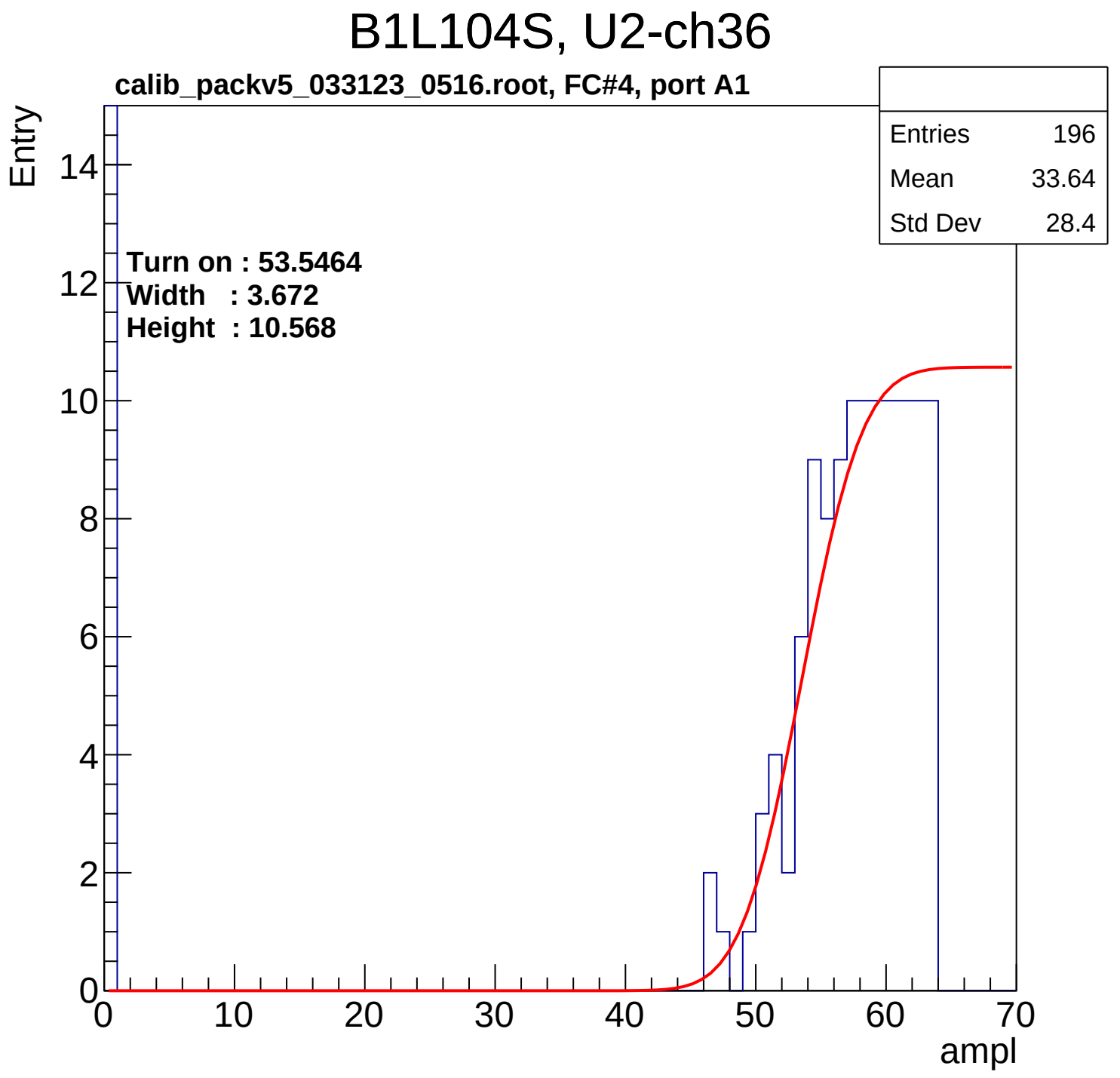
B1L104S, U2-ch36
calib_packv5_033123_0516.root, FC#4, port A1
Entries 196
Mean 33.64
Std Dev 28.4
Turn on : 53.5464
Width : 3.672
Height : 10.568
Entry
ampl
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2
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6
8
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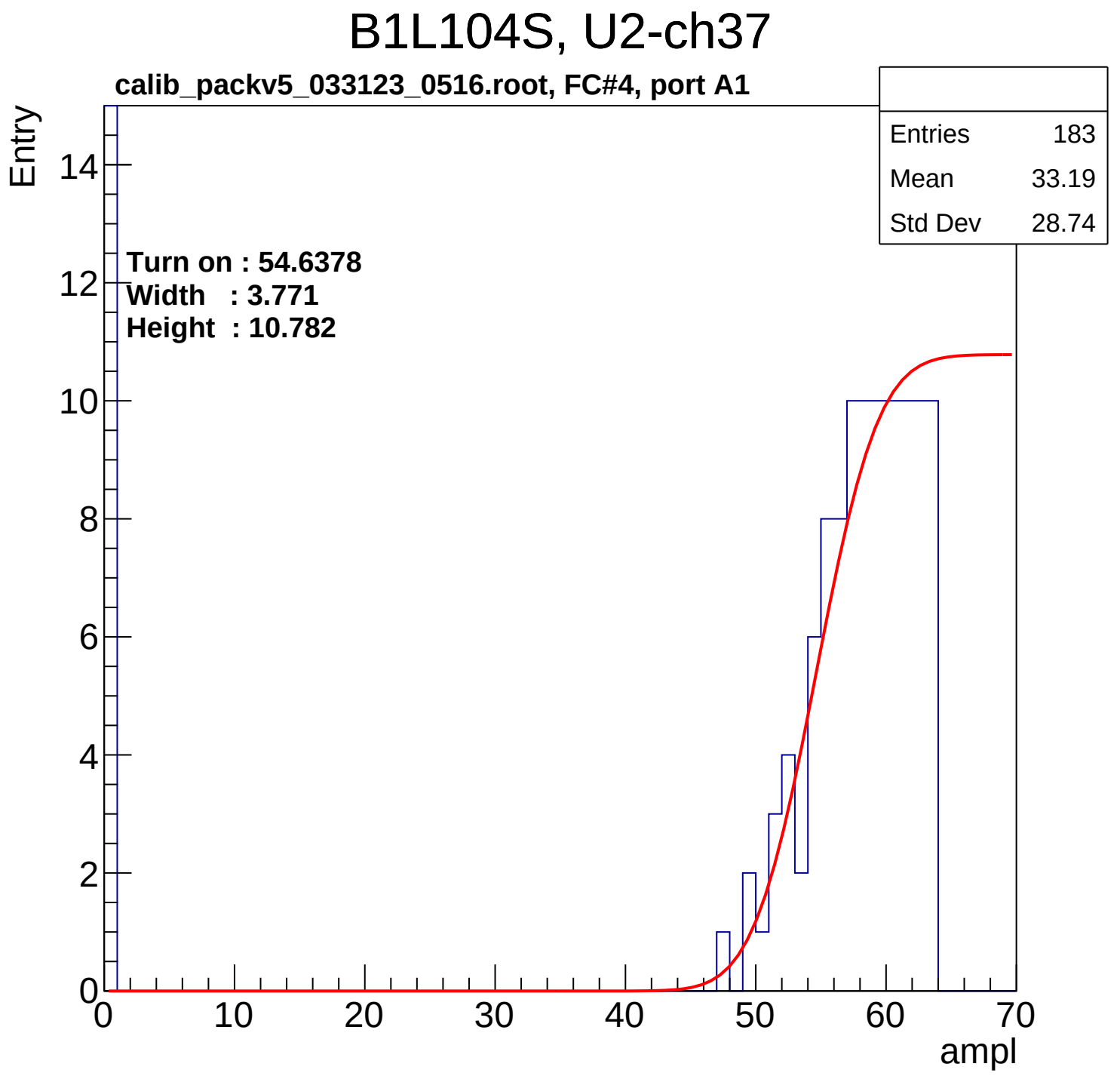
B1L104S, U2-ch37
calib_packv5_033123_0516.root, FC#4, port A1
Entries 183
Mean 33.19
Std Dev 28.74
Turn on : 54.6378
Width : 3.771
Height : 10.782
Entry
ampl
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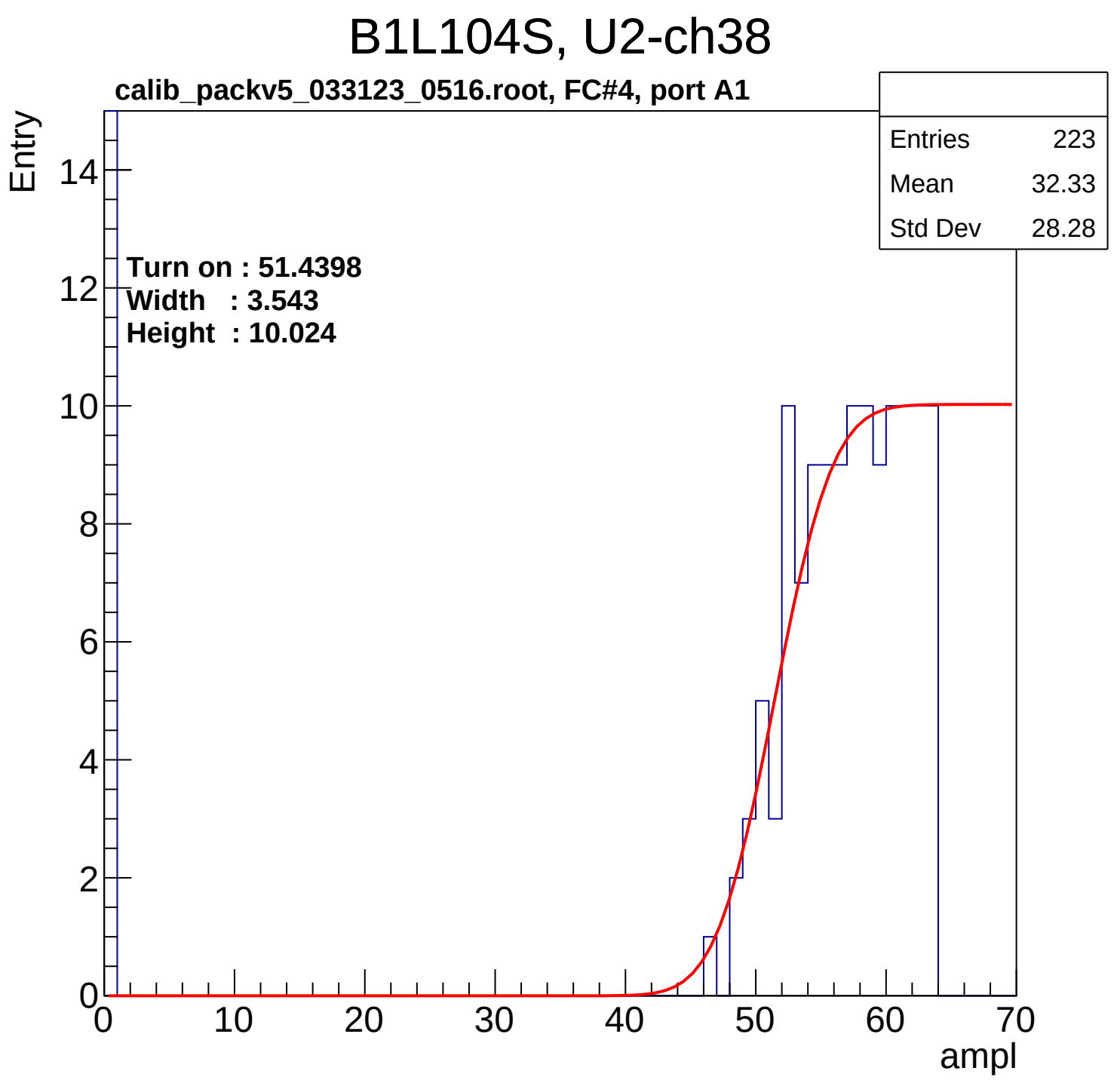
B1L104S, U2-ch38
calib_packv5_033123_0516.root, FC#4, port A1
Entries 223
Mean 32.33
Std Dev 28.28
Turn on : 51.4398
Width : 3.543
Height : 10.024
Entry
ampl
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6
8
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12
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0
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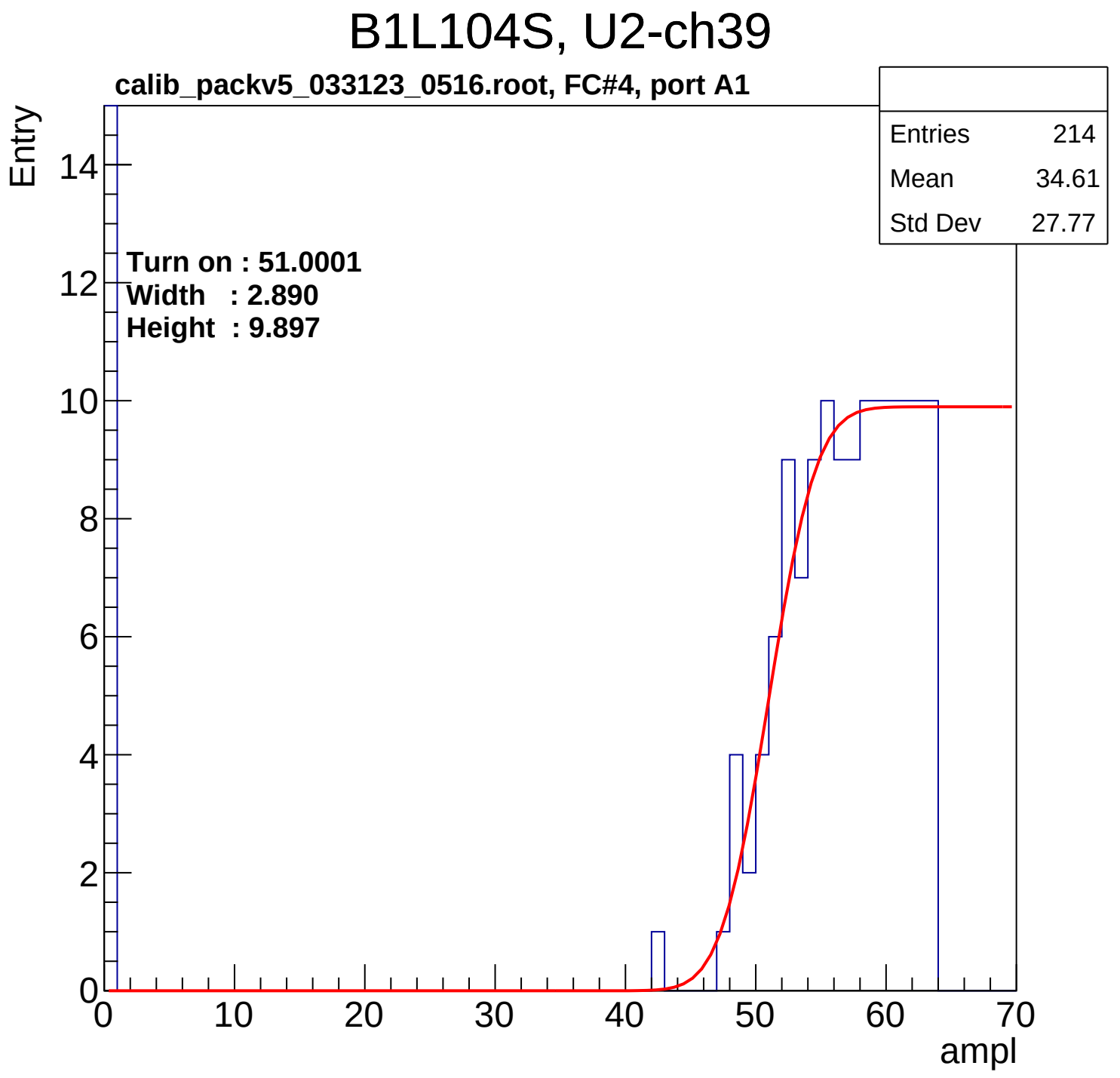
B1L104S, U2-ch39
calib_packv5_033123_0516.root, FC#4, port A1
Entries 214
Mean 34.61
Std Dev 27.77
Turn on : 51.0001
Width : 2.890
Height : 9.897
Entry
ampl
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2
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6
8
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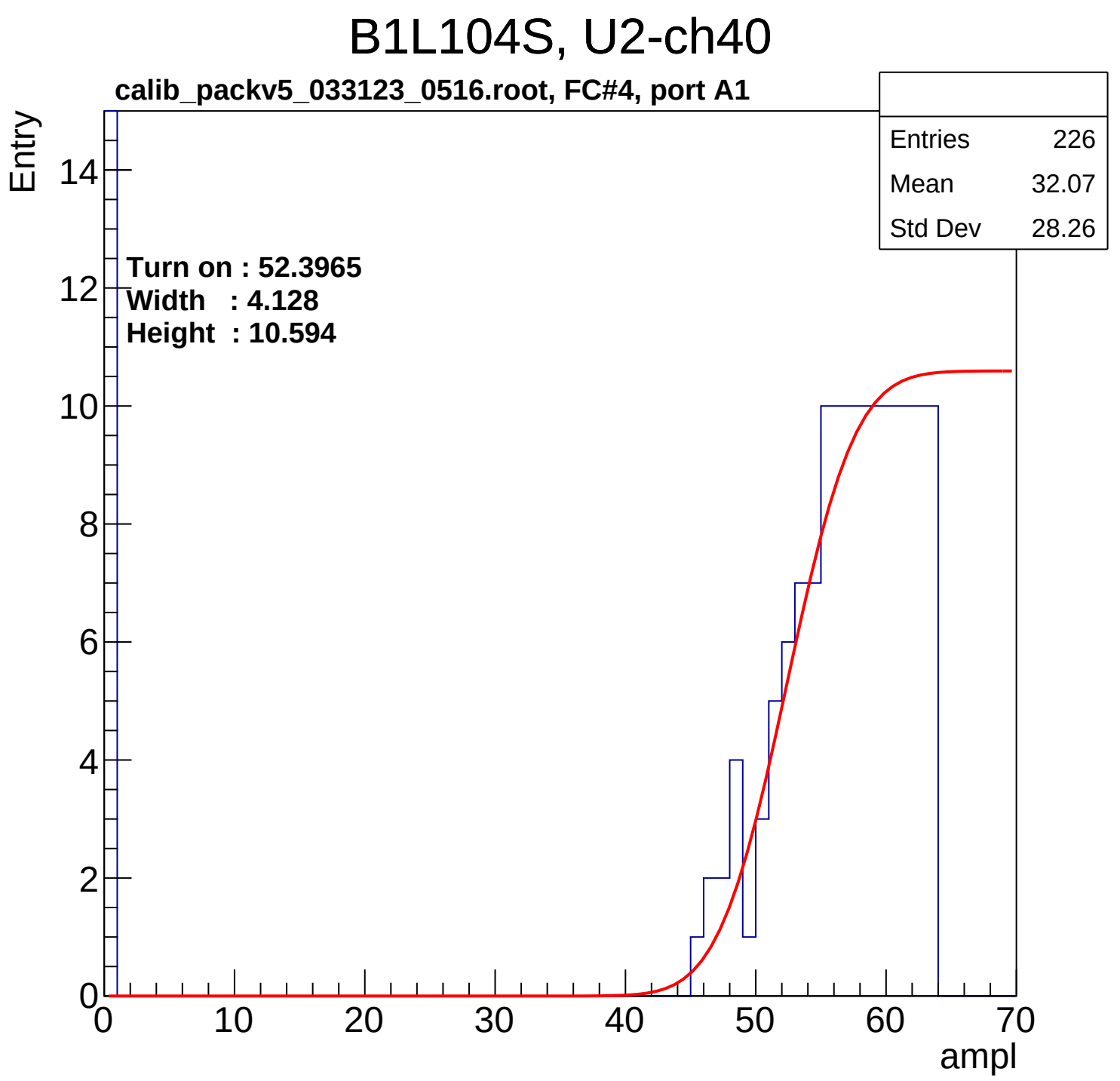
B1L104S, U2-ch40
calib_packv5_033123_0516.root, FC#4, port A1
Entries 226
Mean 32.07
Std Dev 28.26
Turn on : 52.3965
Width : 4.128
Height : 10.594
Entry
ampl
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6
8
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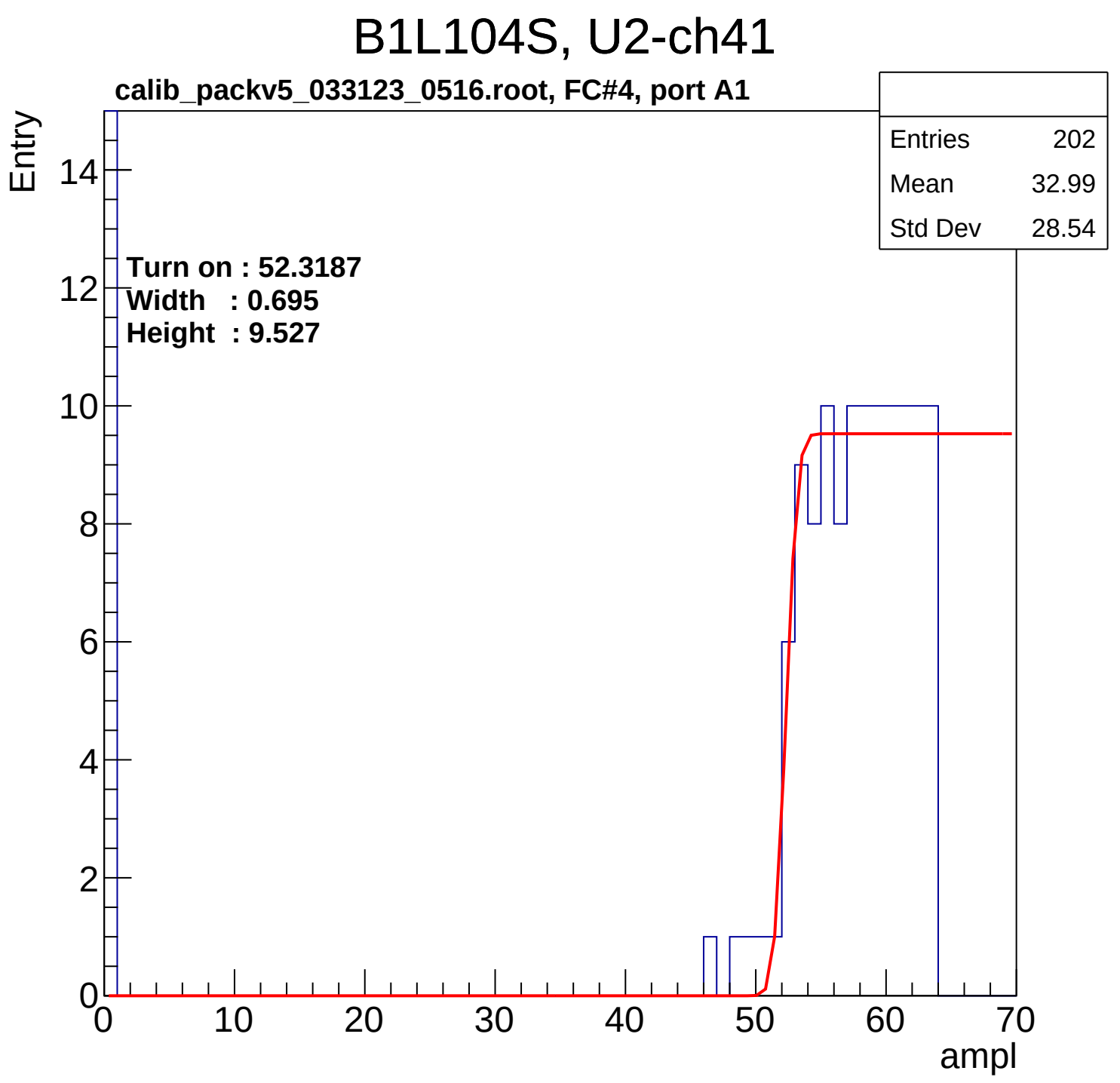
B1L104S, U2-ch41
calib_packv5_033123_0516.root, FC#4, port A1
Entries 202
Mean 32.99
Std Dev 28.54
Turn on : 52.3187
Width : 0.695
Height : 9.527
Entry
ampl
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6
8
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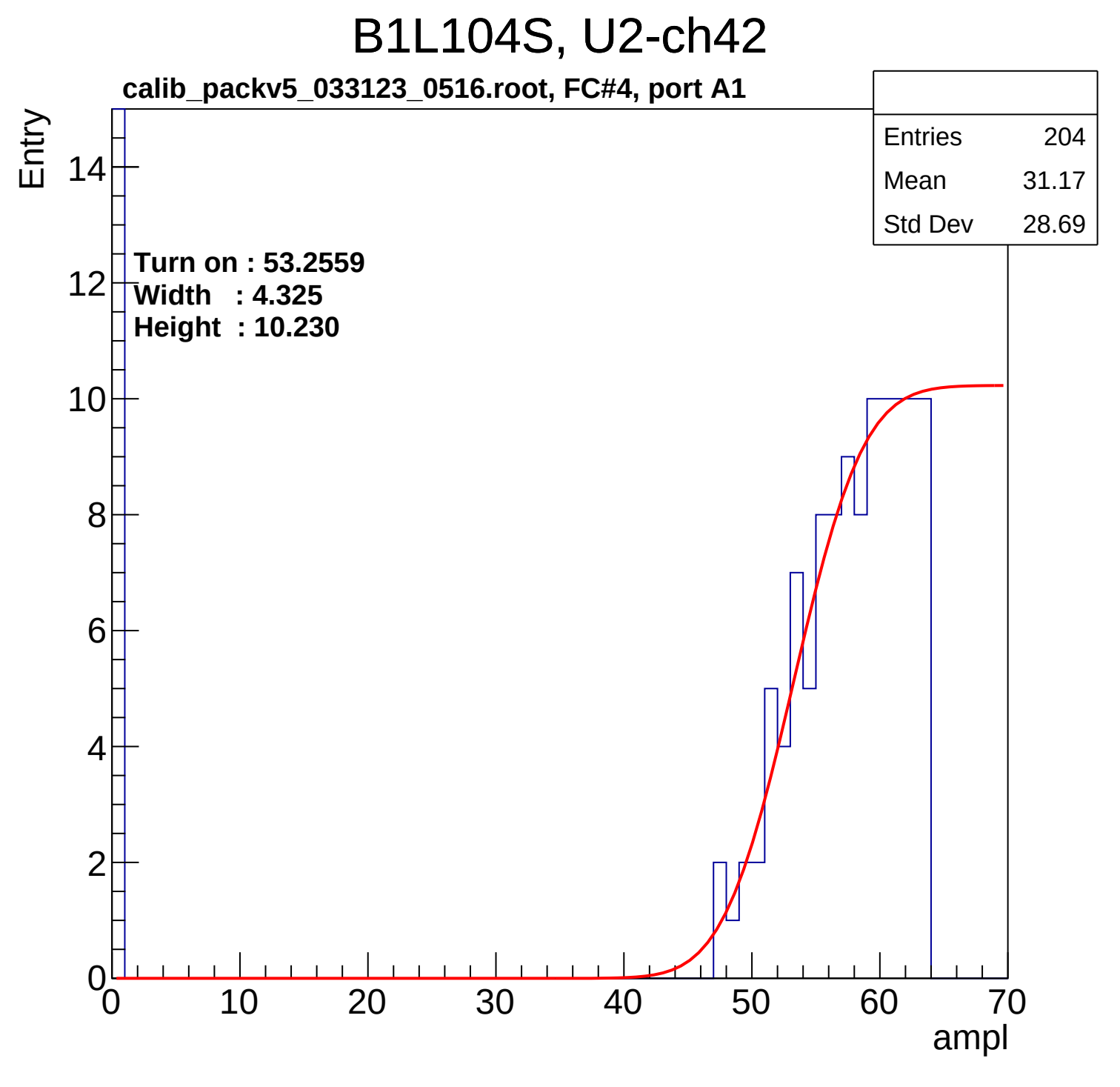
B1L104S, U2-ch42
calib_packv5_033123_0516.root, FC#4, port A1
Entries 204
Mean 31.17
Std Dev 28.69
Turn on : 53.2559
Width : 4.325
Height : 10.230
Entry
ampl
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6
8
10
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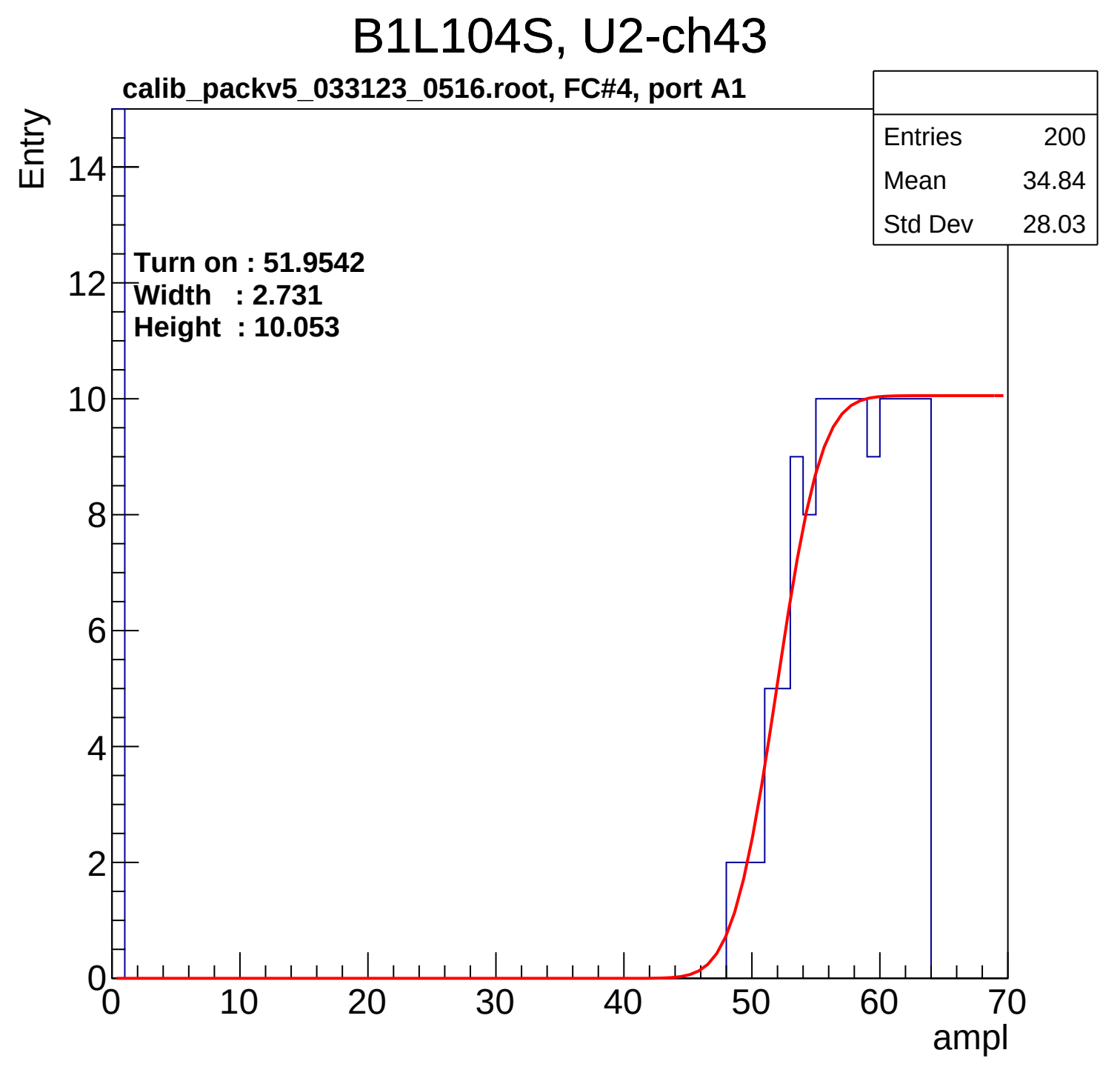
B1L104S, U2-ch43
calib_packv5_033123_0516.root, FC#4, port A1
Entries 200
Mean 34.84
Std Dev 28.03
Turn on : 51.9542
Width : 2.731
Height : 10.053
Entry
ampl
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6
8
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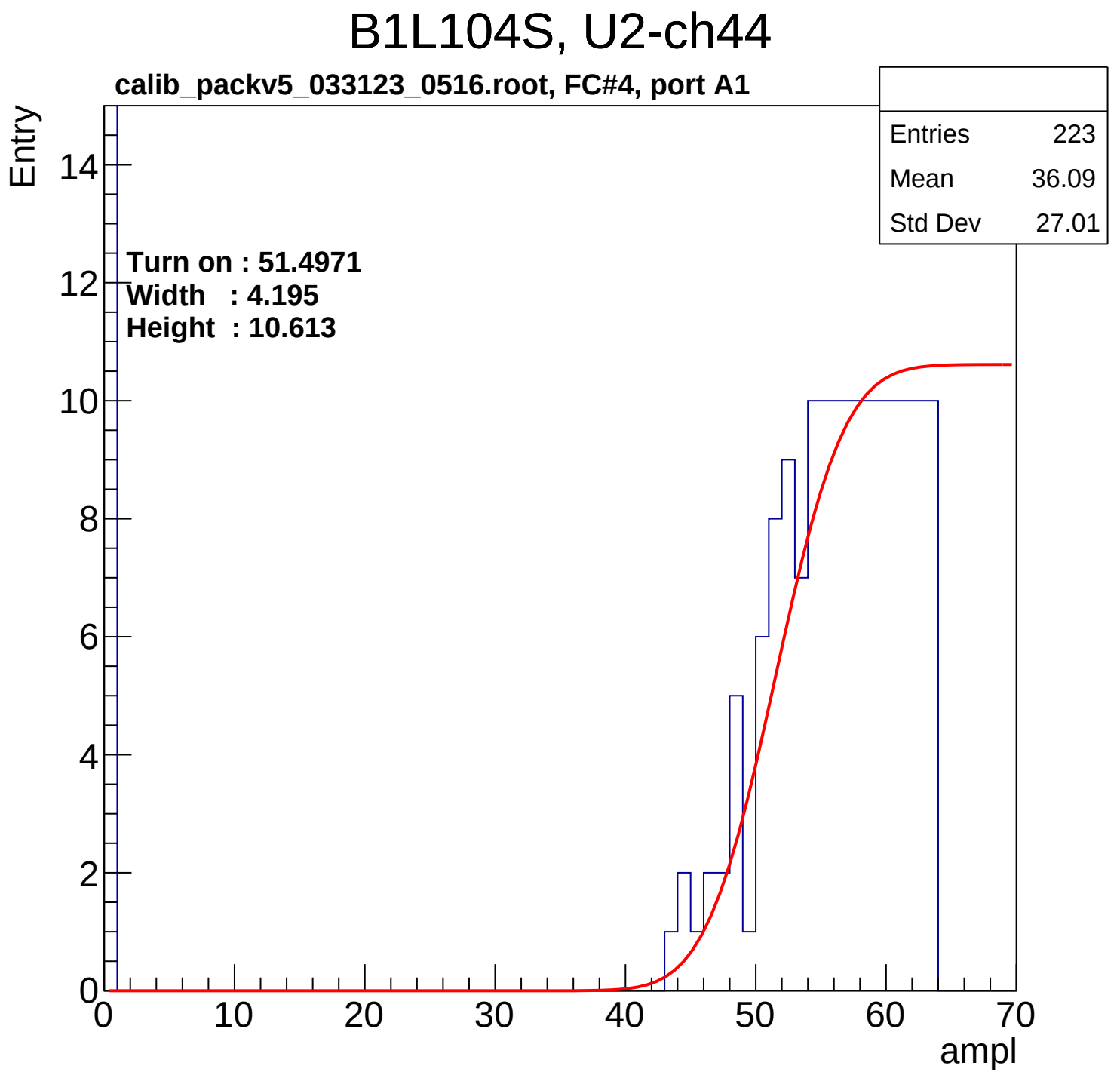
B1L104S, U2-ch44
calib_packv5_033123_0516.root, FC#4, port A1
Entries 223
Mean 36.09
Std Dev 27.01
Turn on : 51.4971
Width : 4.195
Height : 10.613
Entry
ampl
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6
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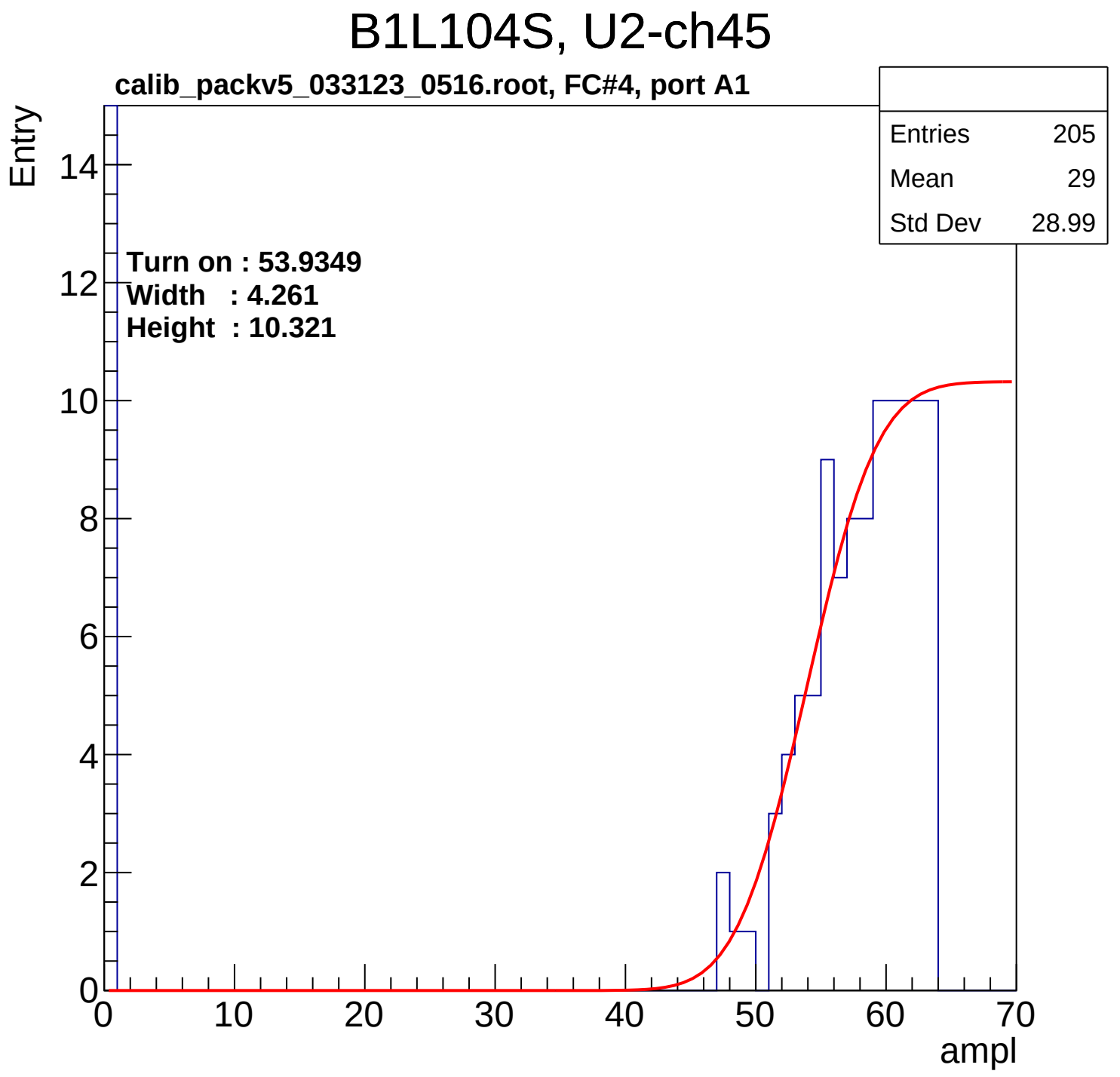
B1L104S, U2-ch45
calib_packv5_033123_0516.root, FC#4, port A1
Entries 205
Mean 29
Std Dev 28.99
Turn on : 53.9349
Width : 4.261
Height : 10.321
Entry
ampl
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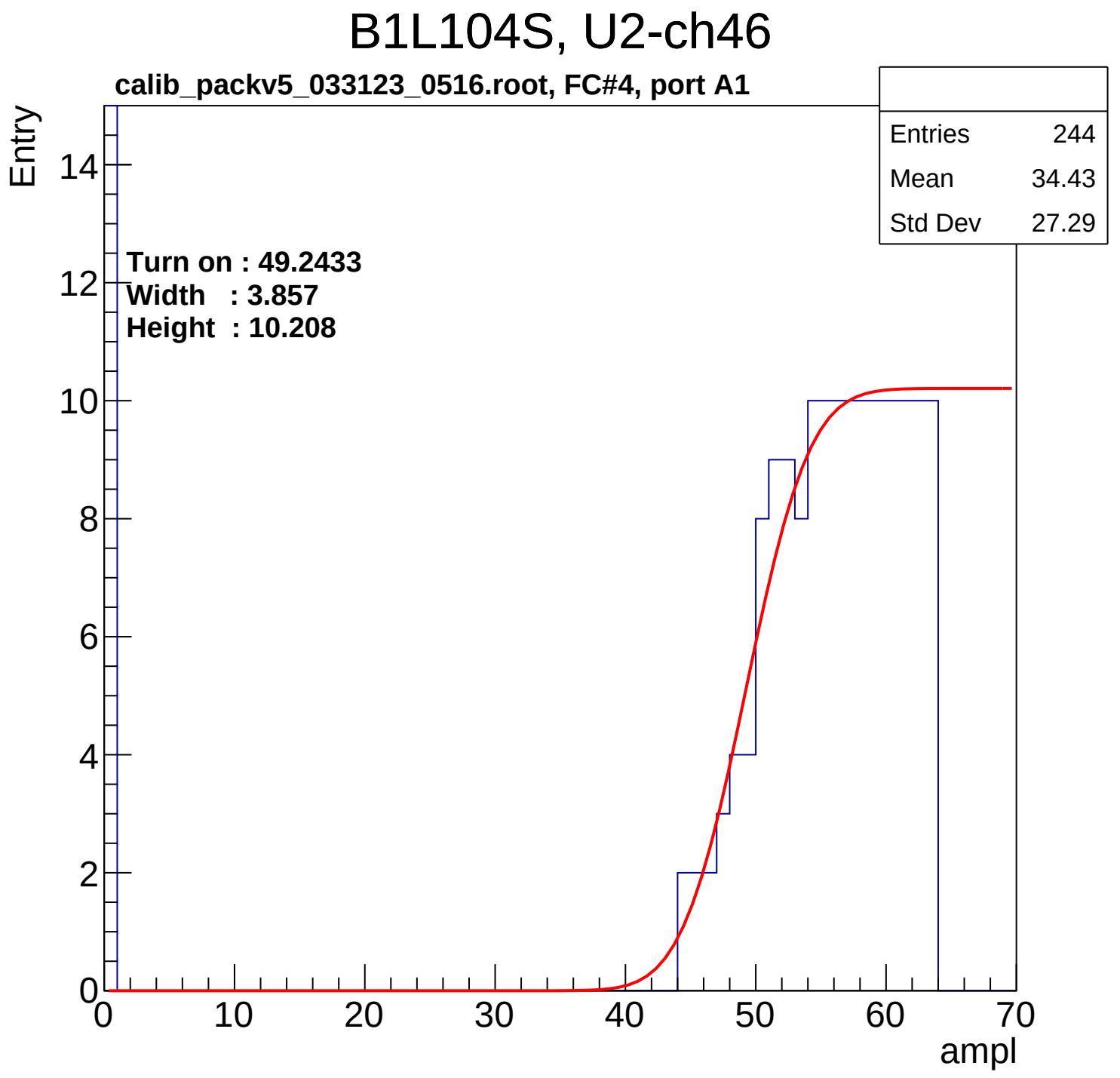
B1L104S, U2-ch46
calib_packv5_033123_0516.root, FC#4, port A1
Entries 244
Mean 34.43
Std Dev 27.29
Turn on : 49.2433
Width : 3.857
Height : 10.208
Entry
ampl
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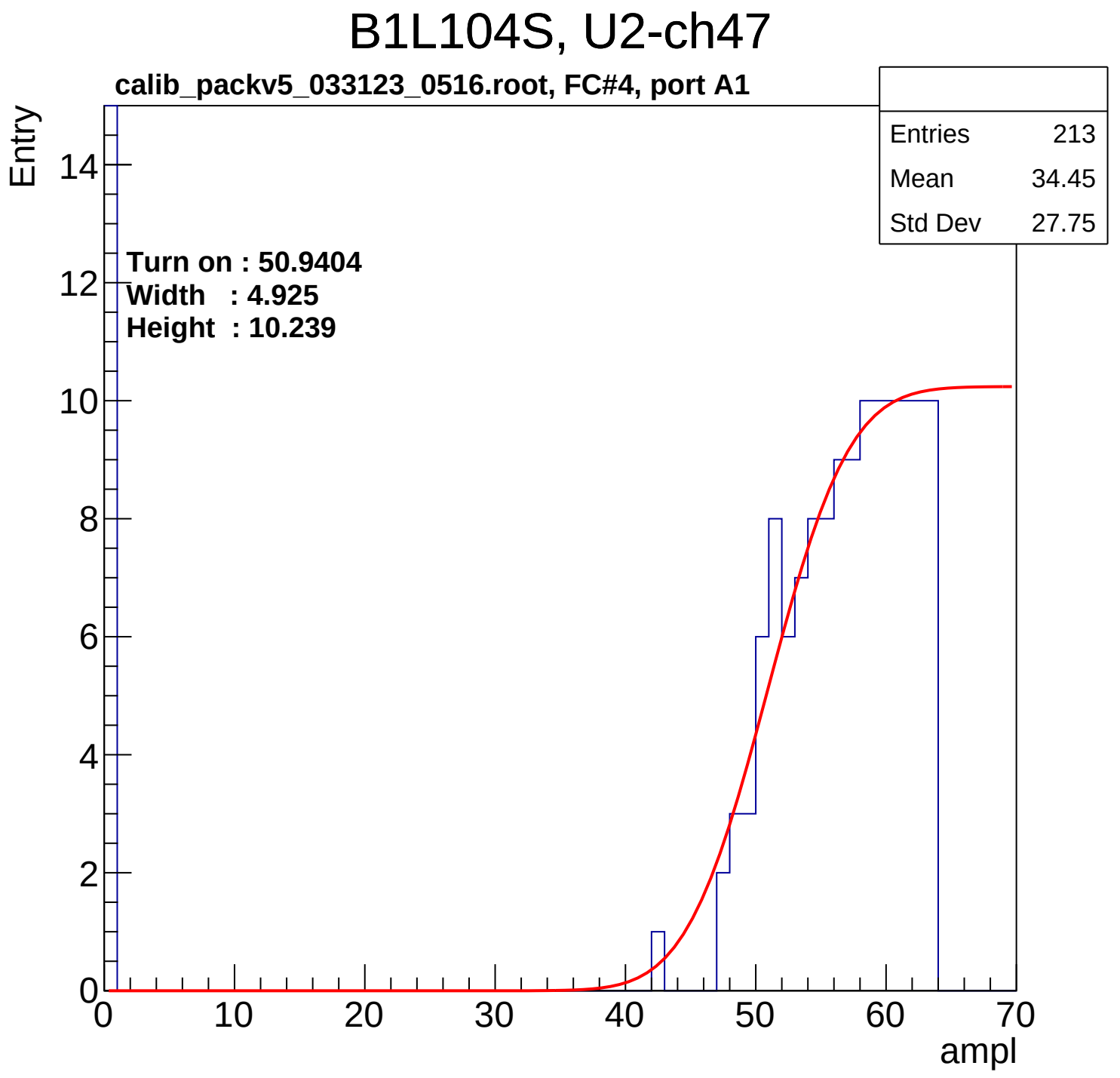
B1L104S, U2-ch47
calib_packv5_033123_0516.root, FC#4, port A1
Entries 213
Mean 34.45
Std Dev 27.75
Turn on : 50.9404
Width : 4.925
Height : 10.239
Entry
ampl
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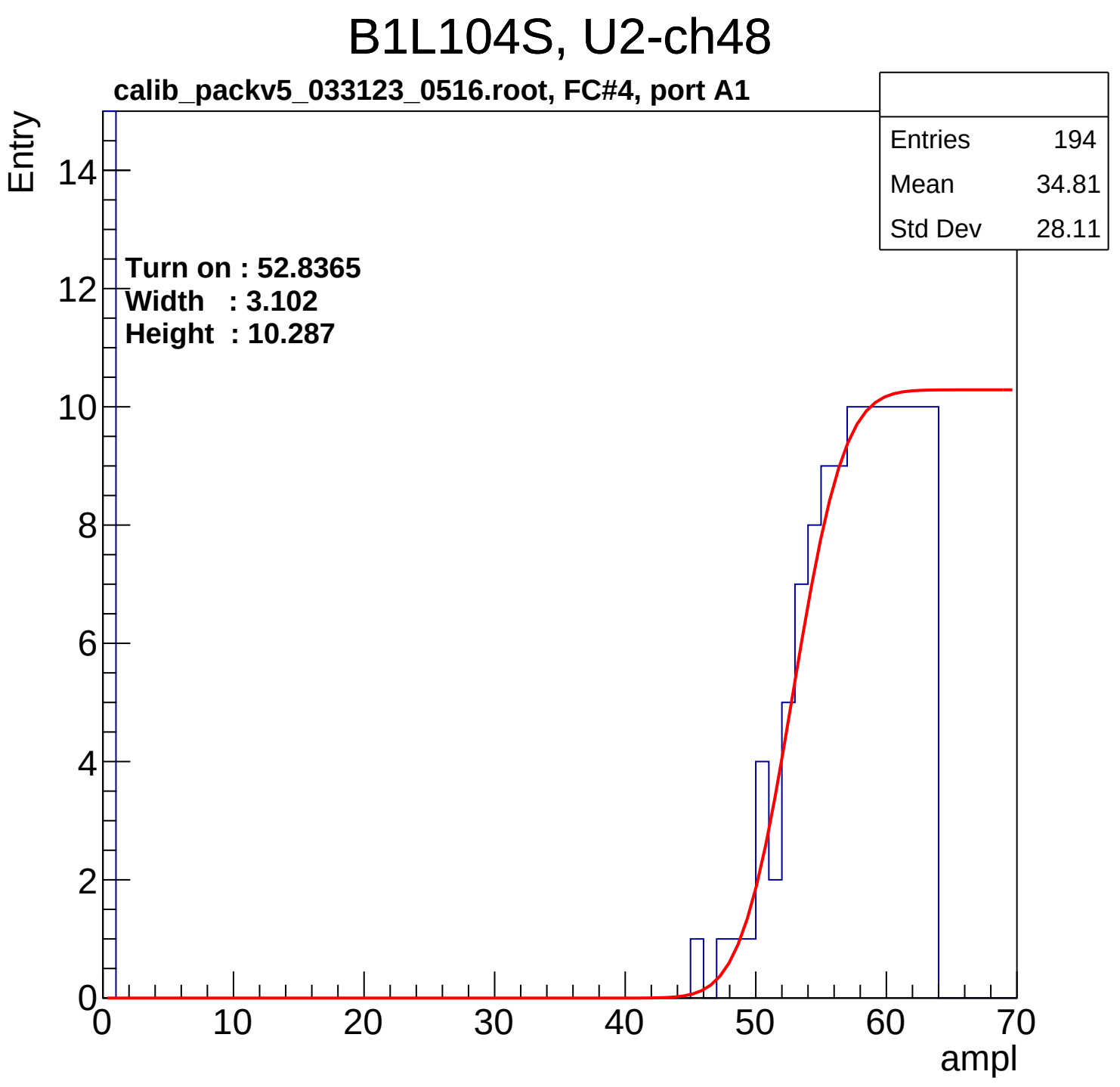
B1L104S, U2-ch48
calib_packv5_033123_0516.root, FC#4, port A1
Entries 194
Mean 34.81
Std Dev 28.11
Turn on : 52.8365
Width : 3.102
Height : 10.287
Entry
ampl
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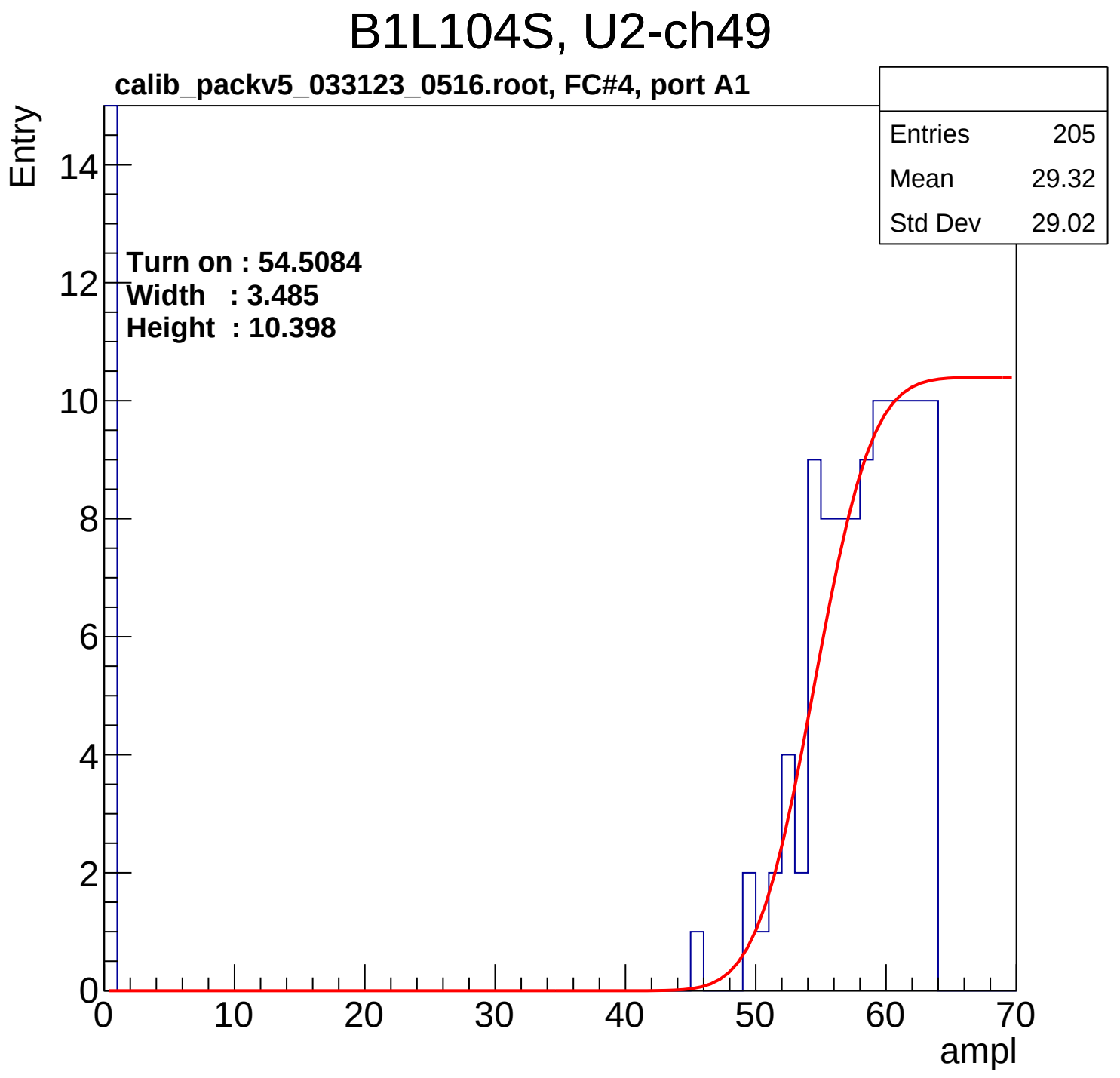
B1L104S, U2-ch49
calib_packv5_033123_0516.root, FC#4, port A1
Entries 205
Mean 29.32
Std Dev 29.02
Turn on : 54.5084
Width : 3.485
Height : 10.398
Entry
ampl
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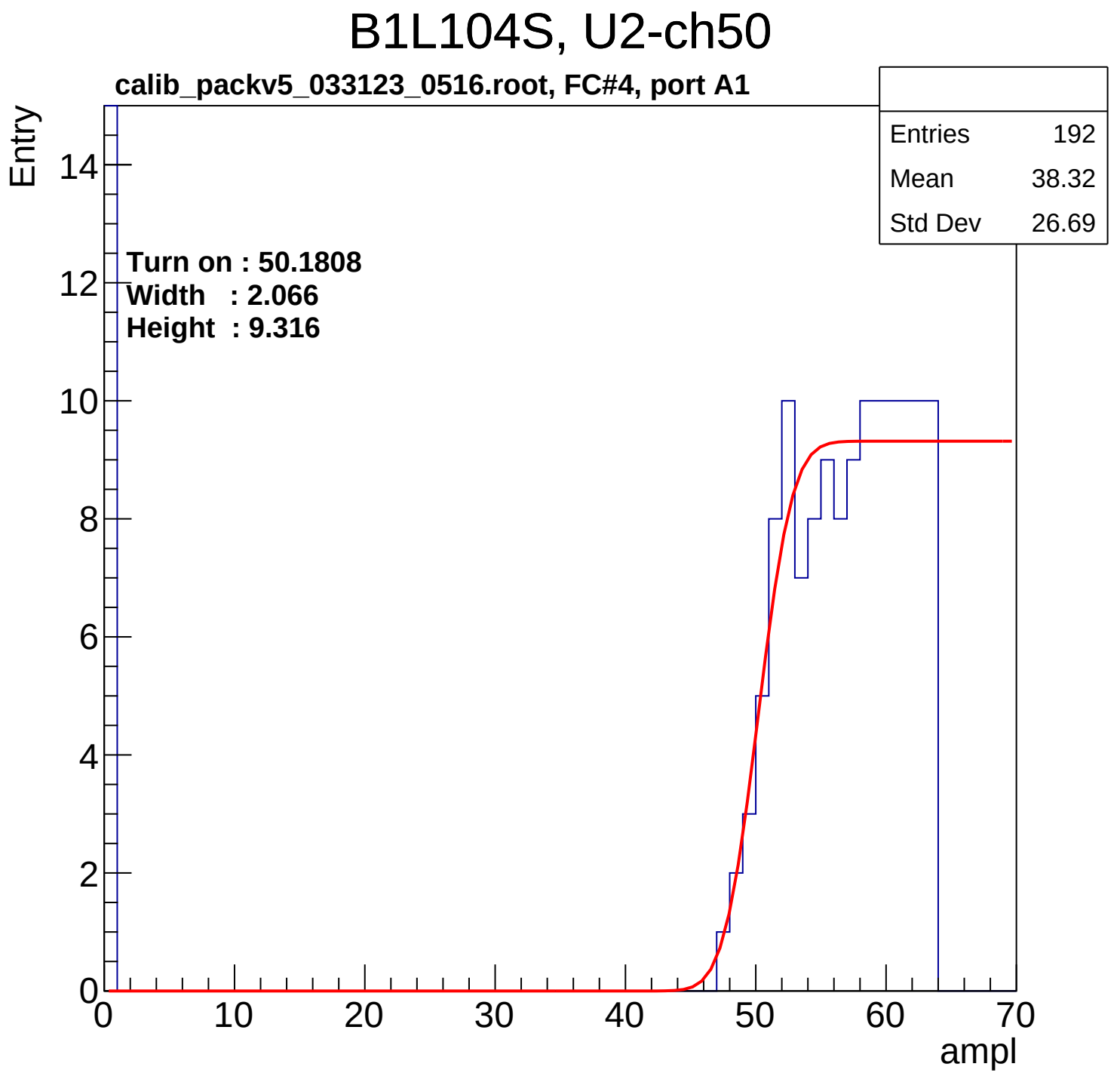
B1L104S, U2-ch50
calib_packv5_033123_0516.root, FC#4, port A1
Entries 192
Mean 38.32
Std Dev 26.69
Turn on : 50.1808
Width : 2.066
Height : 9.316
Entry
ampl
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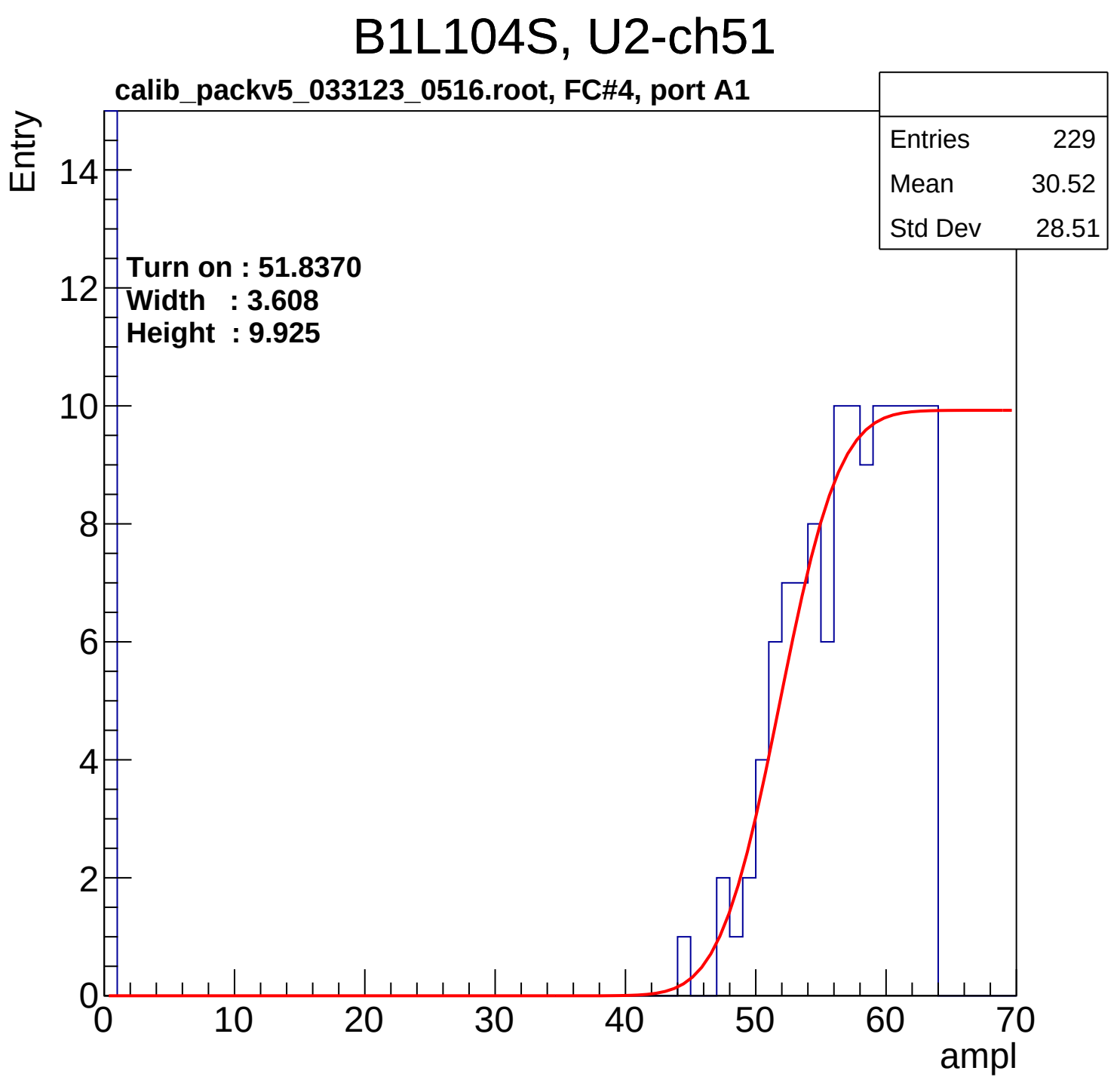
B1L104S, U2-ch51
calib_packv5_033123_0516.root, FC#4, port A1
Entries 229
Mean 30.52
Std Dev 28.51
Turn on : 51.8370
Width : 3.608
Height : 9.925
Entry
ampl
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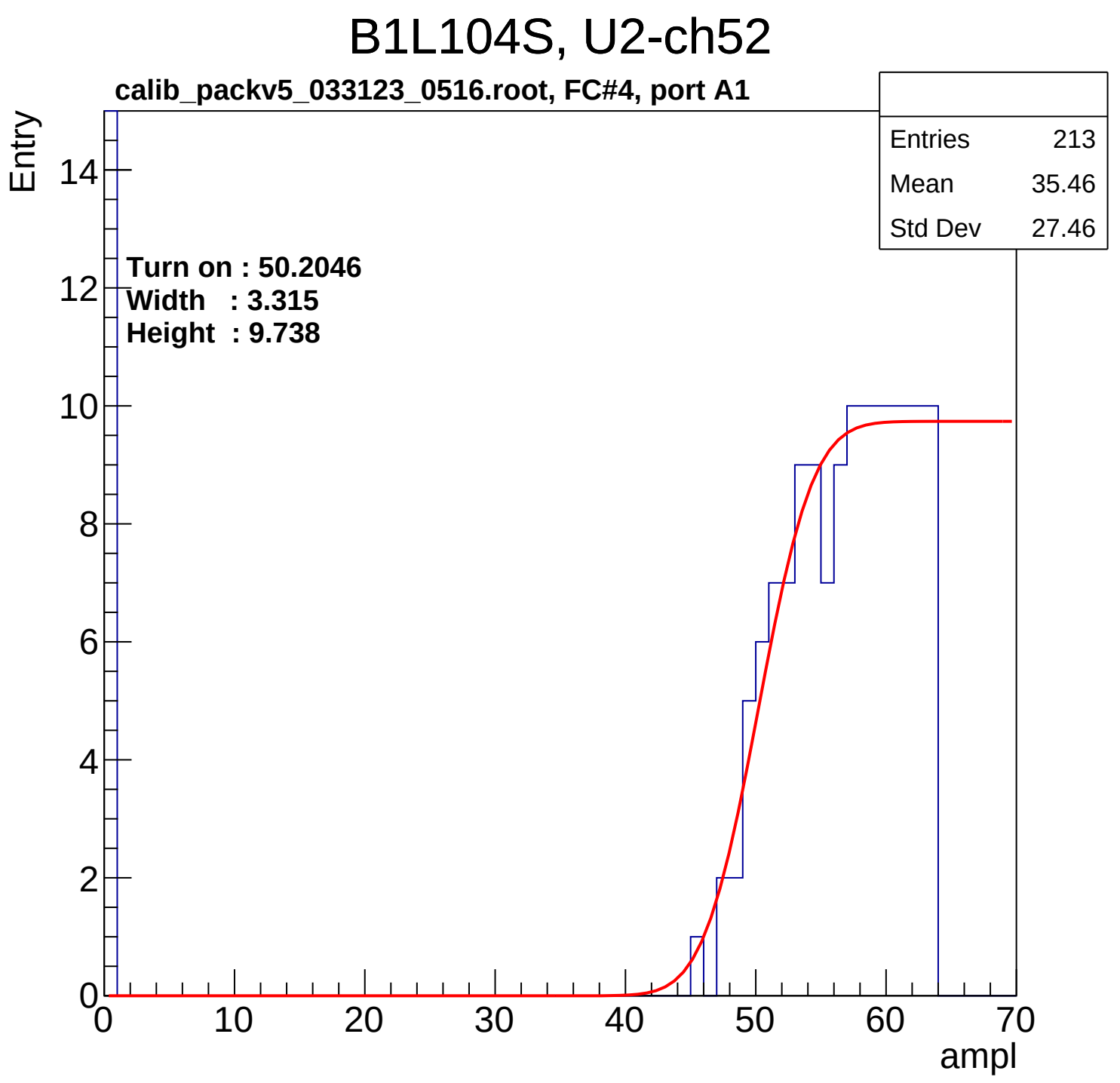
B1L104S, U2-ch52
calib_packv5_033123_0516.root, FC#4, port A1
Entries 213
Mean 35.46
Std Dev 27.46
Turn on : 50.2046
Width : 3.315
Height : 9.738
Entry
ampl
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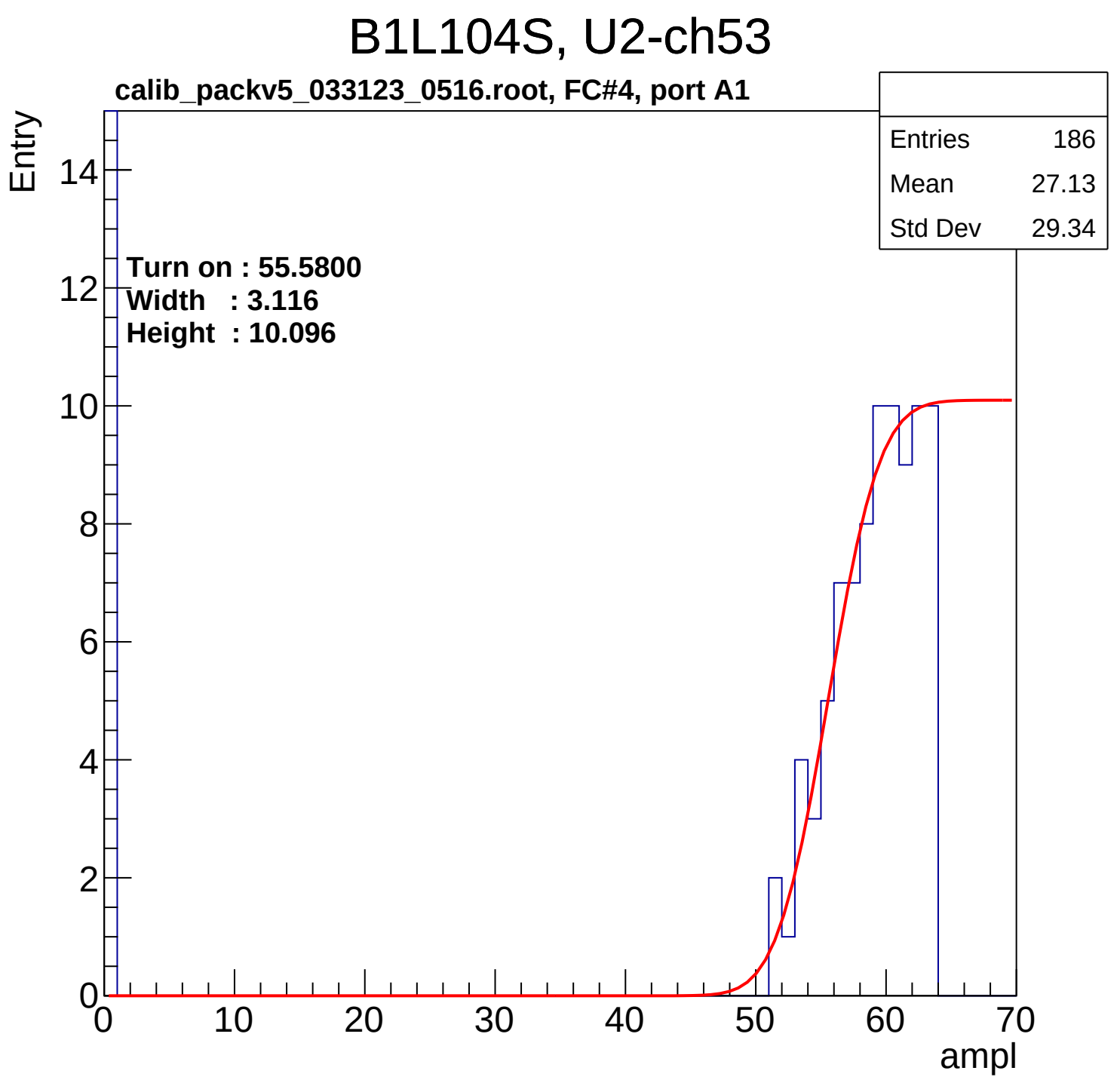
B1L104S, U2-ch53
calib_packv5_033123_0516.root, FC#4, port A1
Entries 186
Mean 27.13
Std Dev 29.34
Turn on : 55.5800
Width : 3.116
Height : 10.096
Entry
ampl
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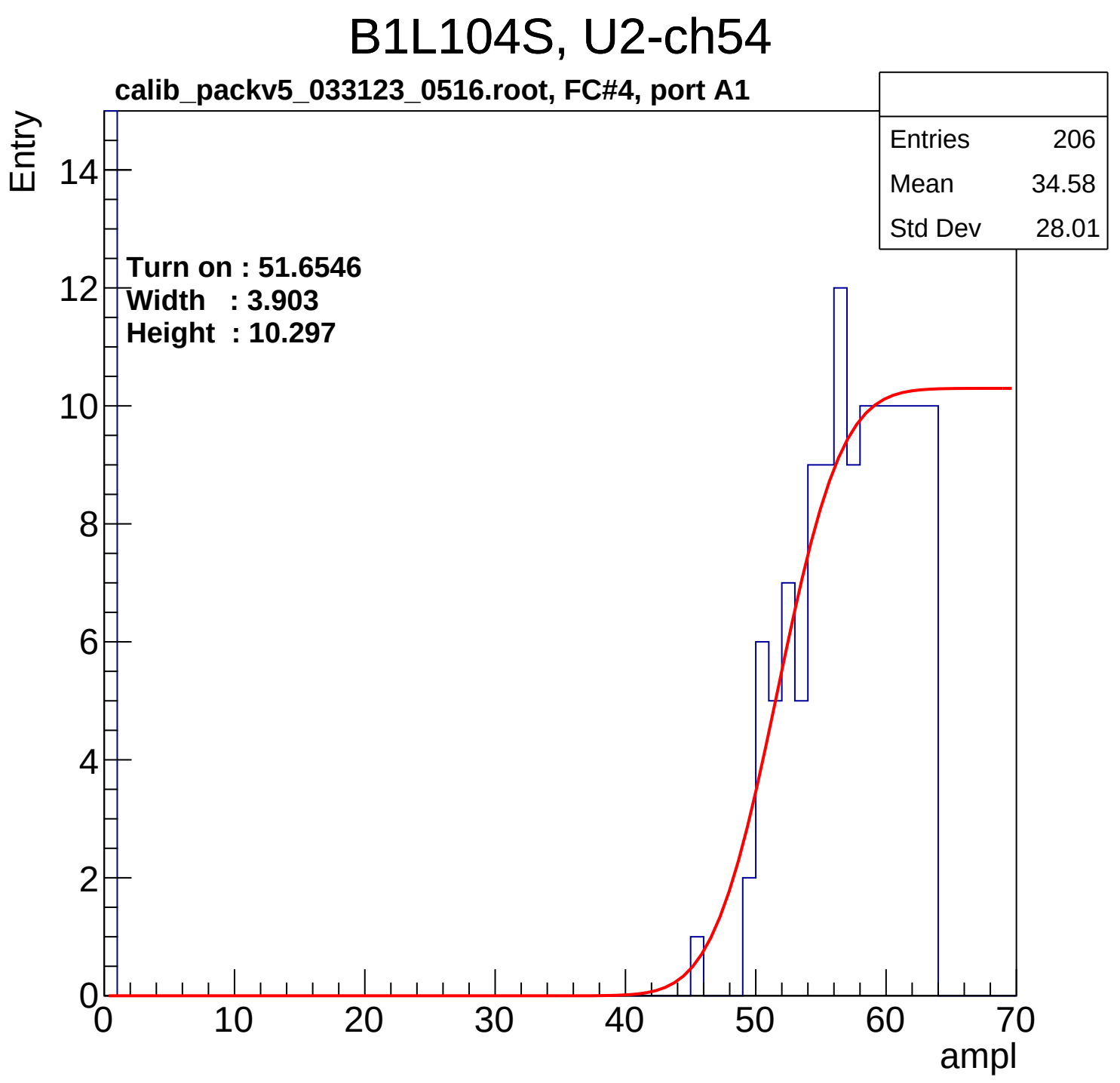
B1L104S, U2-ch54
calib_packv5_033123_0516.root, FC#4, port A1
Entries 206
Mean 34.58
Std Dev 28.01
Turn on : 51.6546
Width : 3.903
Height : 10.297
Entry
ampl
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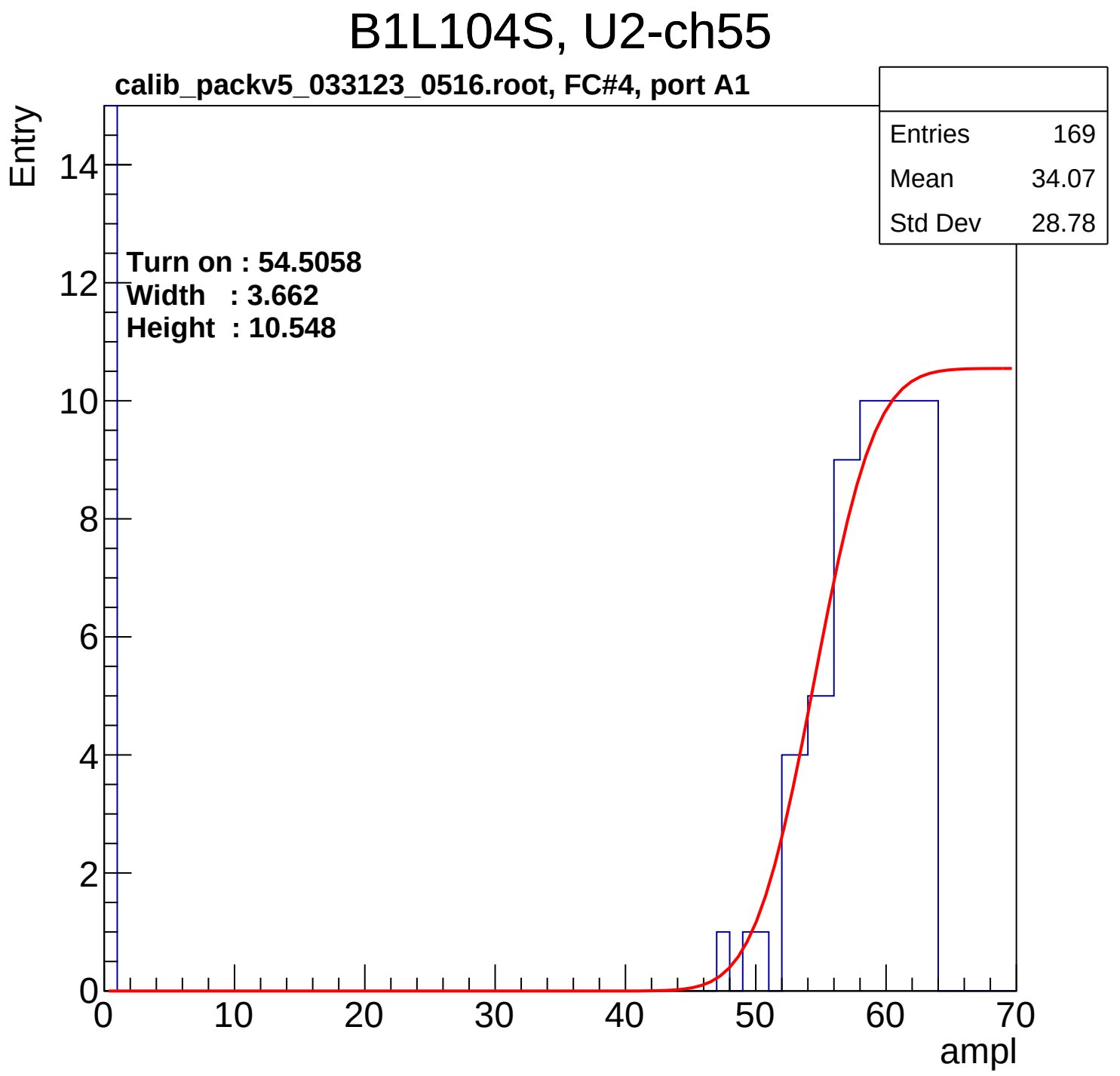
B1L104S, U2-ch55
calib_packv5_033123_0516.root, FC#4, port A1
Entries 169
Mean 34.07
Std Dev 28.78
Turn on : 54.5058
Width : 3.662
Height : 10.548
Entry
ampl
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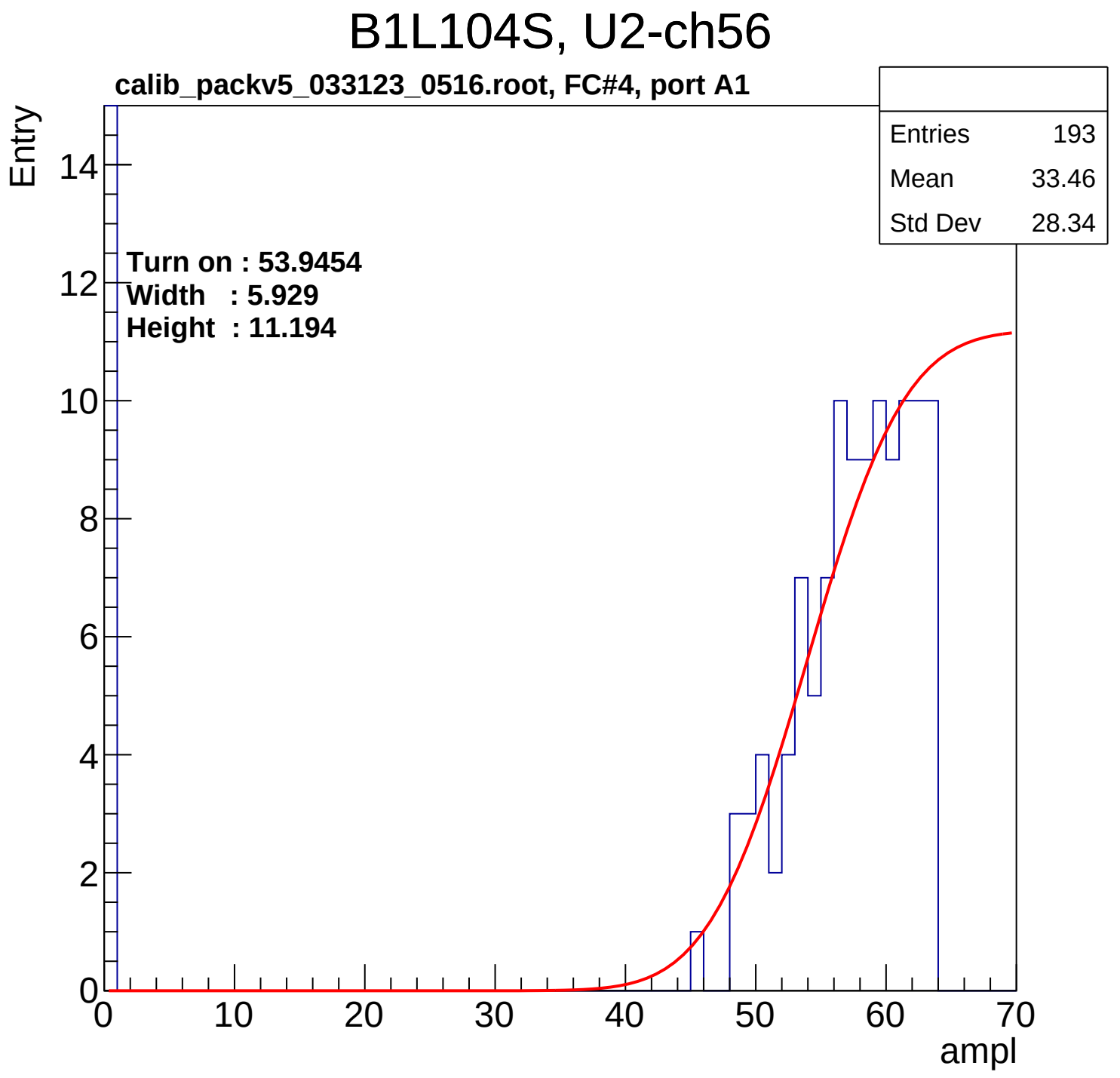
B1L104S, U2-ch56
calib_packv5_033123_0516.root, FC#4, port A1
Entries 193
Mean 33.46
Std Dev 28.34
Turn on : 53.9454
Width : 5.929
Height : 11.194
Entry
ampl
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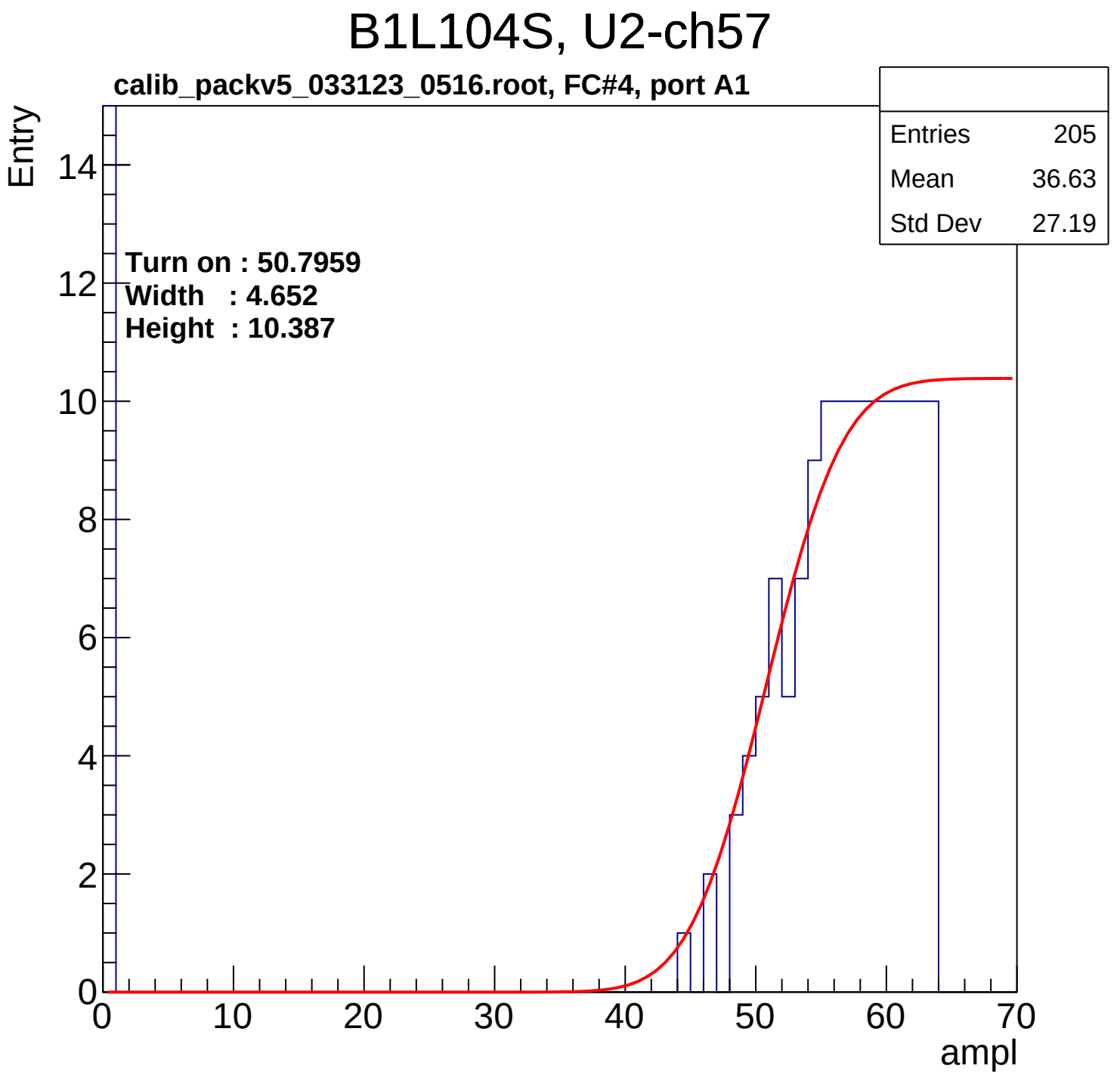
B1L104S, U2-ch57
calib_packv5_033123_0516.root, FC#4, port A1
Entries 205
Mean 36.63
Std Dev 27.19
Turn on : 50.7959
Width : 4.652
Height : 10.387
Entry
ampl
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4
6
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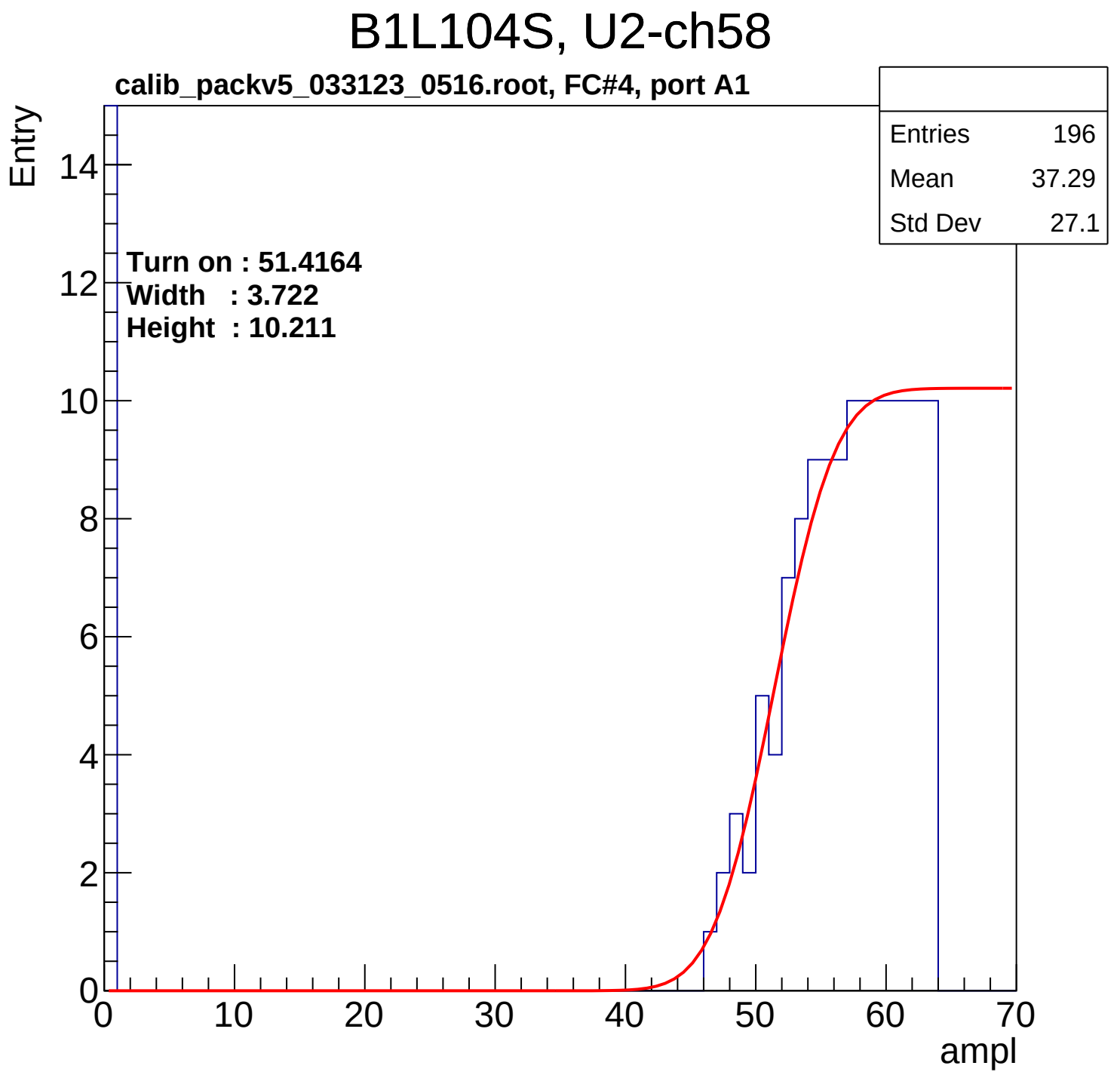
B1L104S, U2-ch58
calib_packv5_033123_0516.root, FC#4, port A1
Entries 196
Mean 37.29
Std Dev 27.1
Turn on : 51.4164
Width : 3.722
Height : 10.211
Entry
ampl
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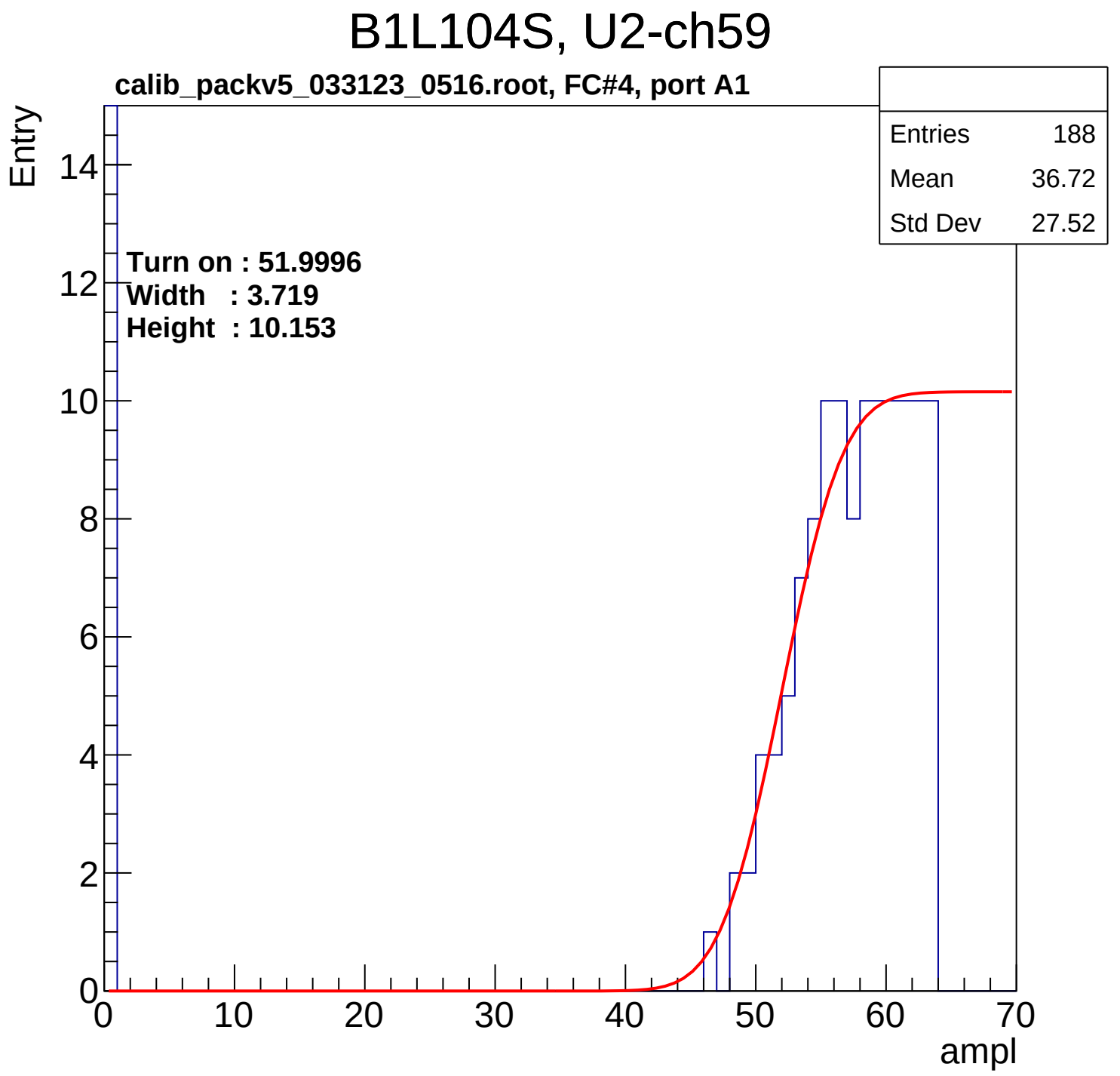
B1L104S, U2-ch59
calib_packv5_033123_0516.root, FC#4, port A1
Entries 188
Mean 36.72
Std Dev 27.52
Turn on : 51.9996
Width : 3.719
Height : 10.153
Entry
ampl
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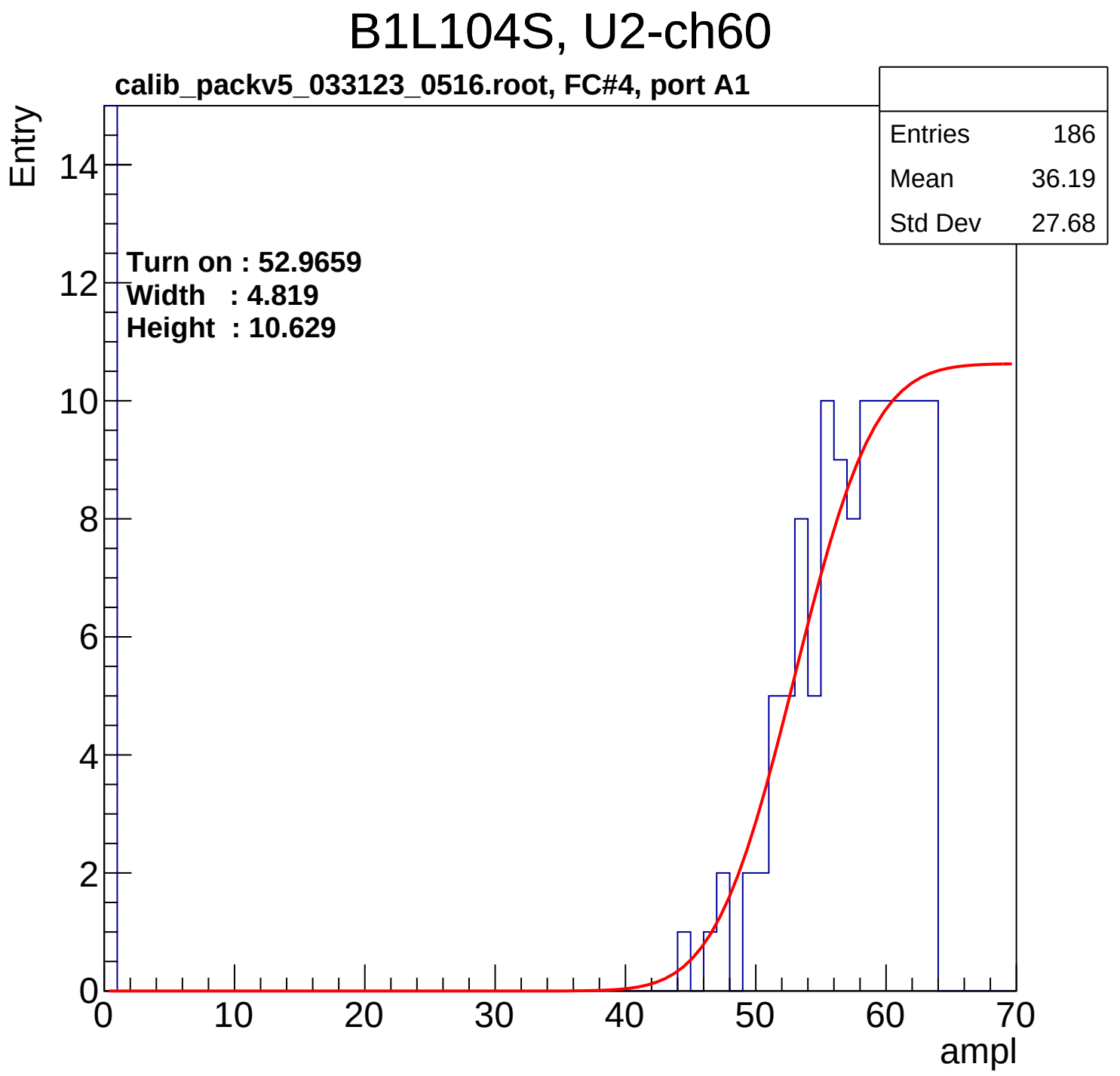
B1L104S, U2-ch60
calib_packv5_033123_0516.root, FC#4, port A1
Entries 186
Mean 36.19
Std Dev 27.68
Turn on : 52.9659
Width : 4.819
Height : 10.629
Entry
ampl
0
2
4
6
8
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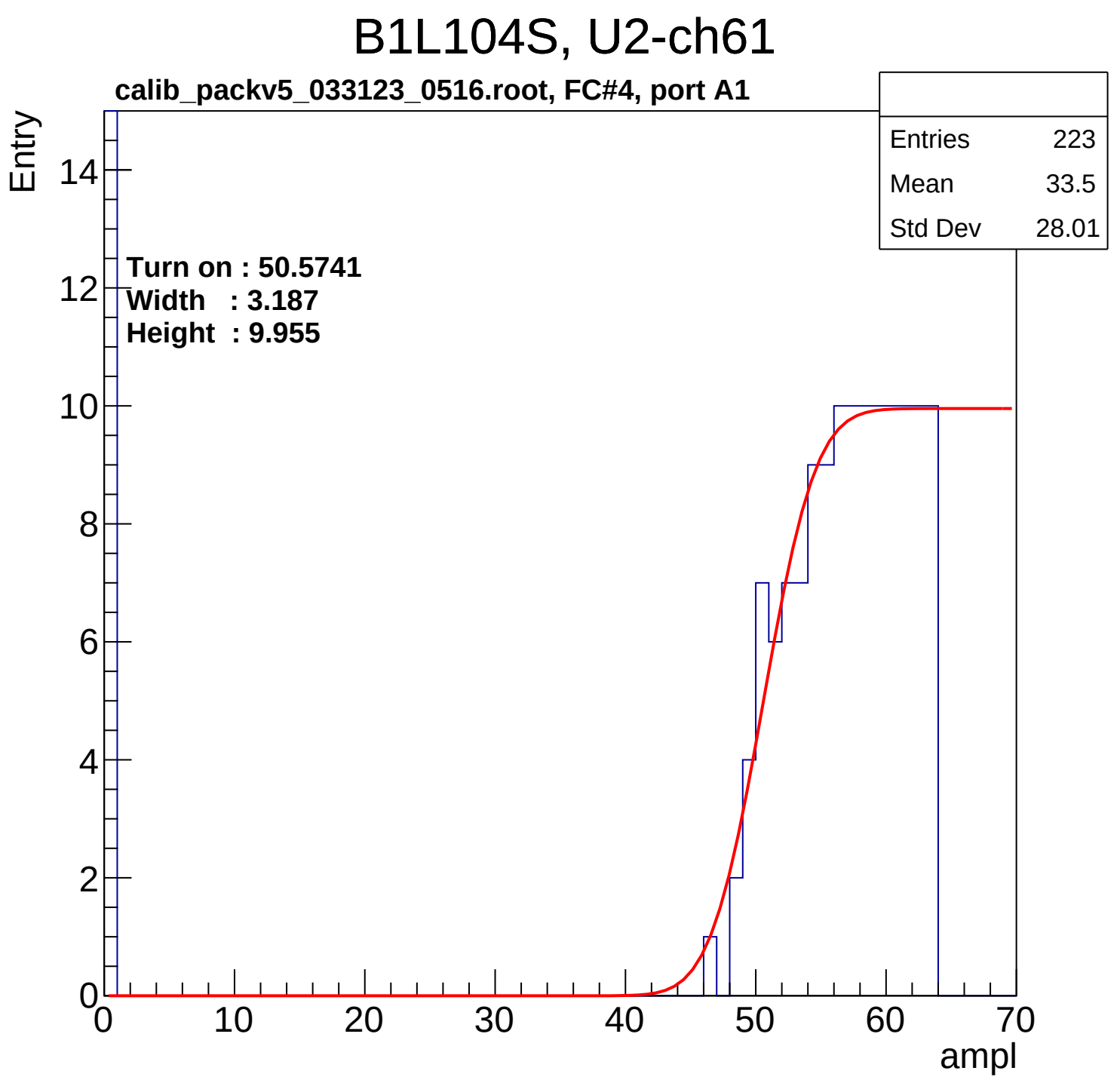
B1L104S, U2-ch61
calib_packv5_033123_0516.root, FC#4, port A1
Entries 223
Mean 33.5
Std Dev 28.01
Turn on : 50.5741
Width : 3.187
Height : 9.955
Entry
ampl
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2
4
6
8
10
12
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0
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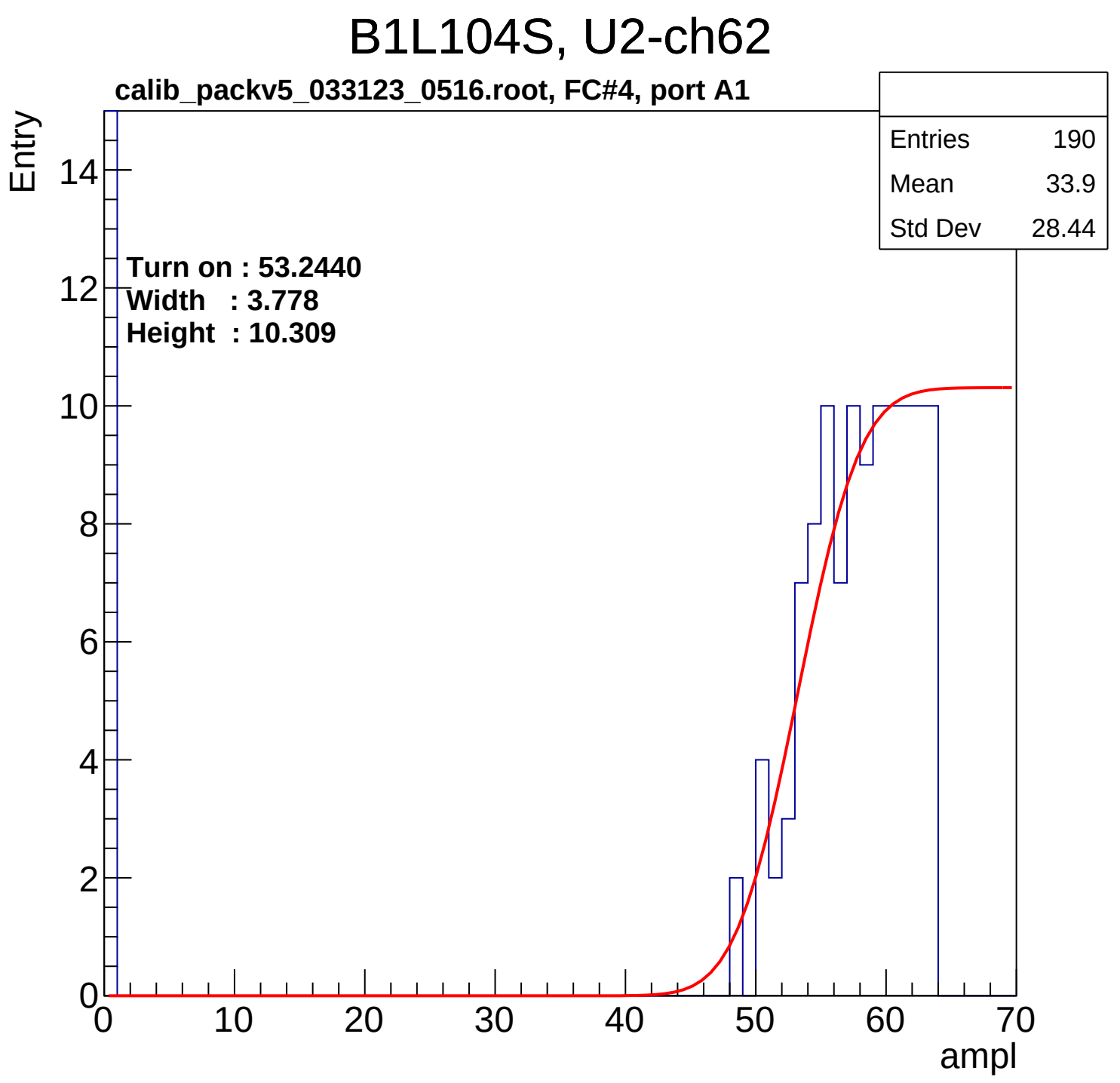
B1L104S, U2-ch62
calib_packv5_033123_0516.root, FC#4, port A1
Entries 190
Mean 33.9
Std Dev 28.44
Turn on : 53.2440
Width : 3.778
Height : 10.309
Entry
ampl
0
2
4
6
8
10
12
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0
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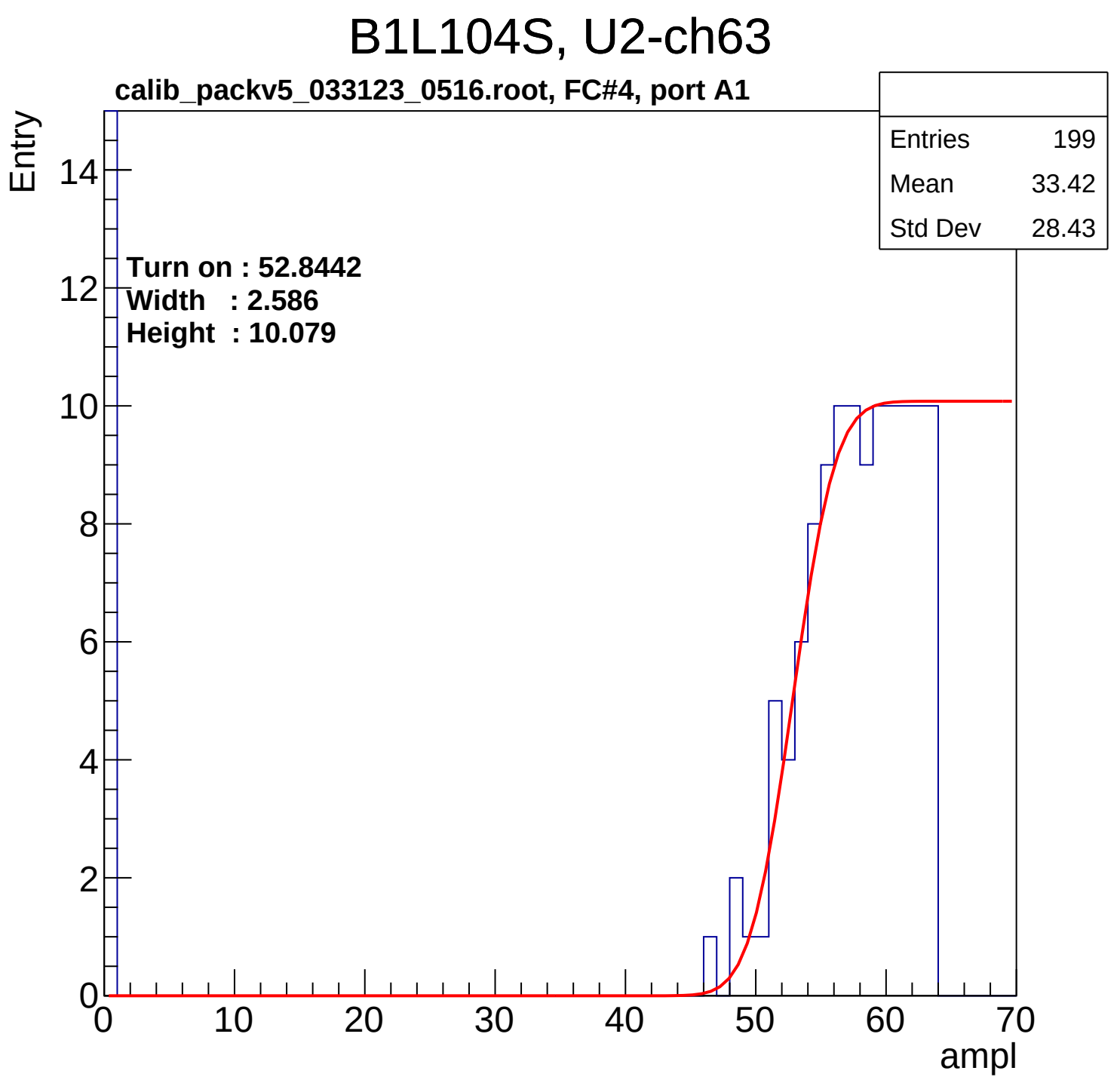
B1L104S, U2-ch63
calib_packv5_033123_0516.root, FC#4, port A1
Entries 199
Mean 33.42
Std Dev 28.43
Turn on : 52.8442
Width : 2.586
Height : 10.079
Entry
ampl
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2
4
6
8
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0
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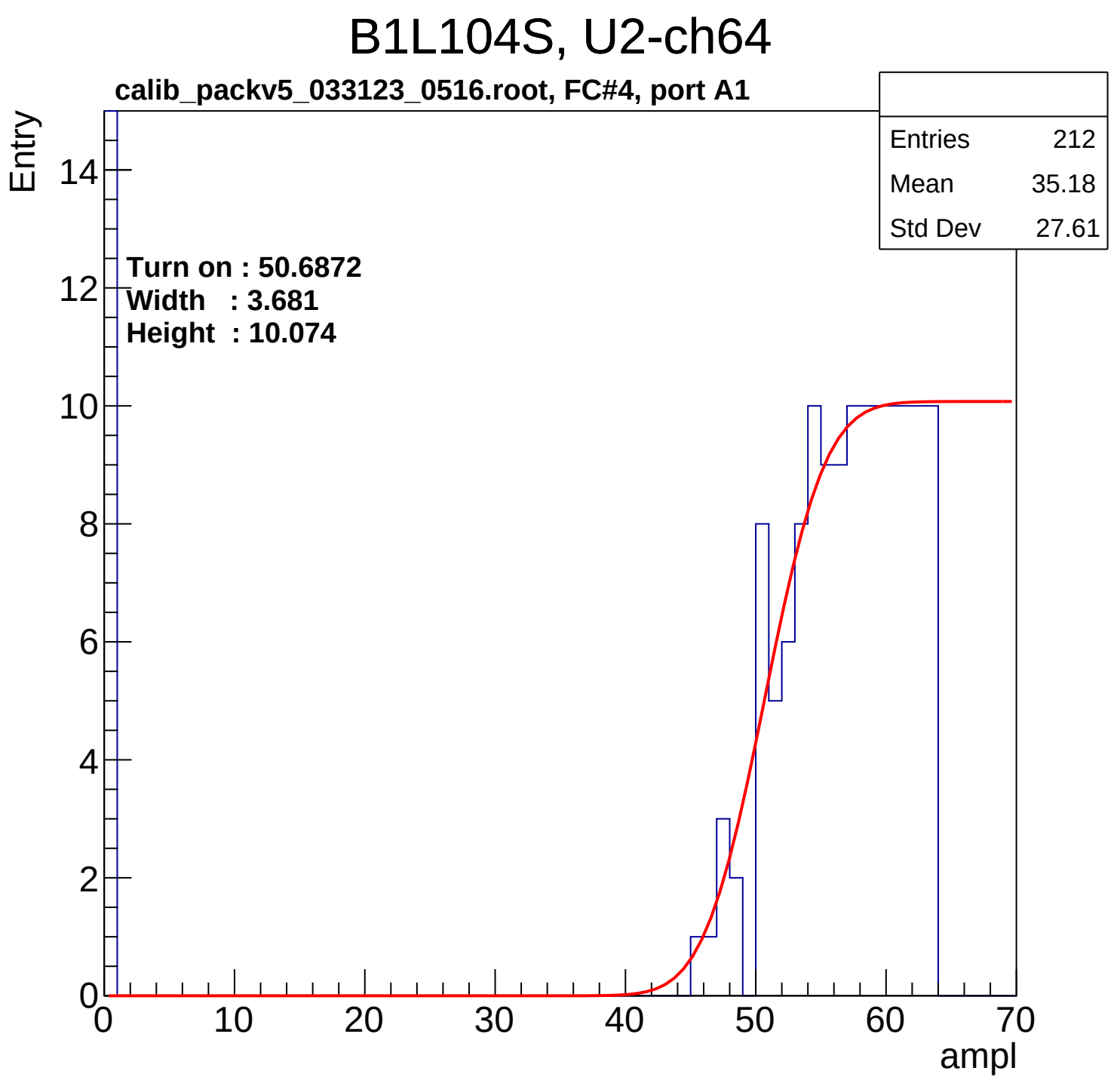
B1L104S, U2-ch64
calib_packv5_033123_0516.root, FC#4, port A1
Entries 212
Mean 35.18
Std Dev 27.61
Turn on : 50.6872
Width : 3.681
Height : 10.074
Entry
ampl
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2
4
6
8
10
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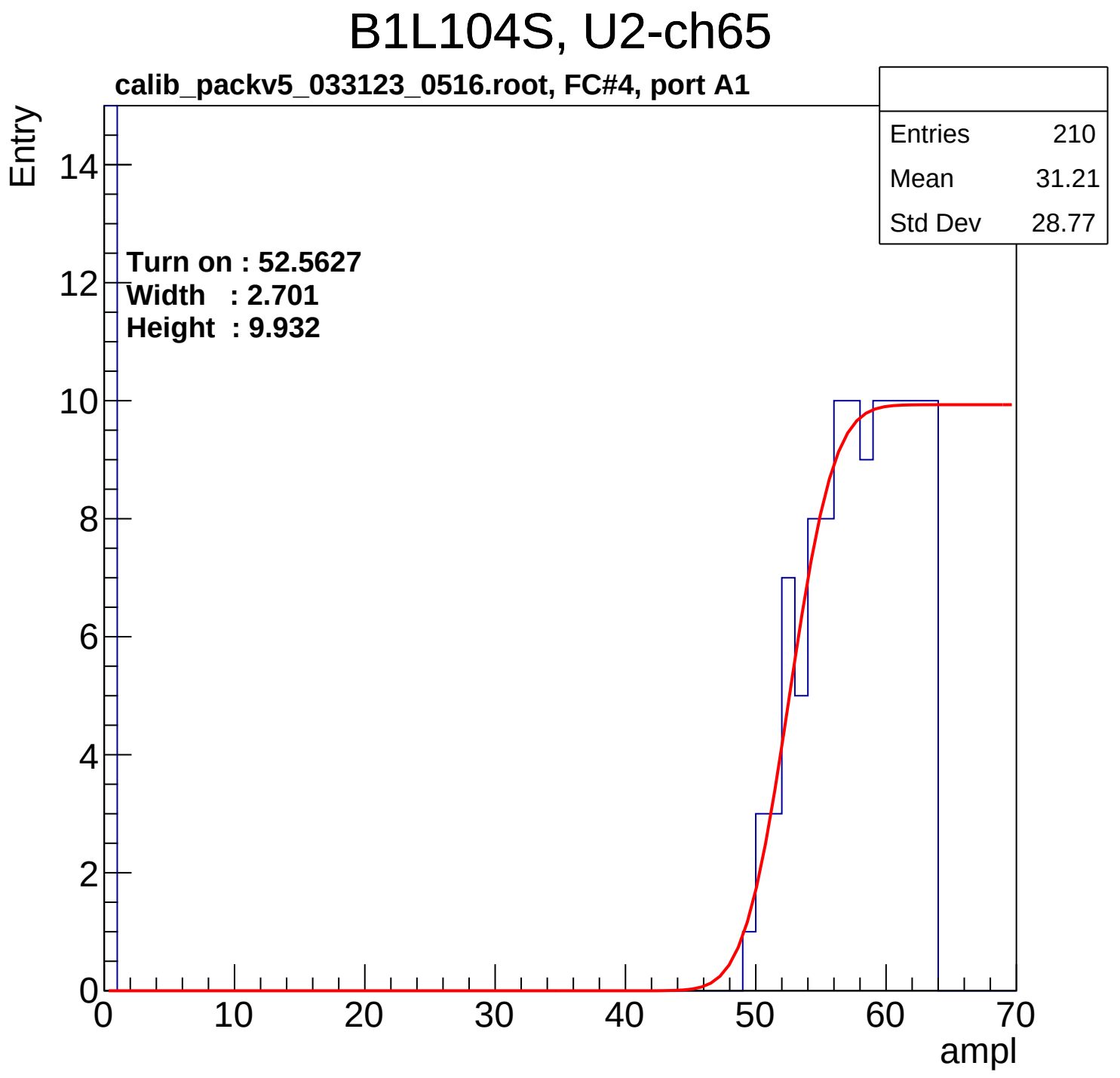
B1L104S, U2-ch65
calib_packv5_033123_0516.root, FC#4, port A1
Entries 210
Mean 31.21
Std Dev 28.77
Turn on : 52.5627
Width : 2.701
Height : 9.932
Entry
ampl
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2
4
6
8
10
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0
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60
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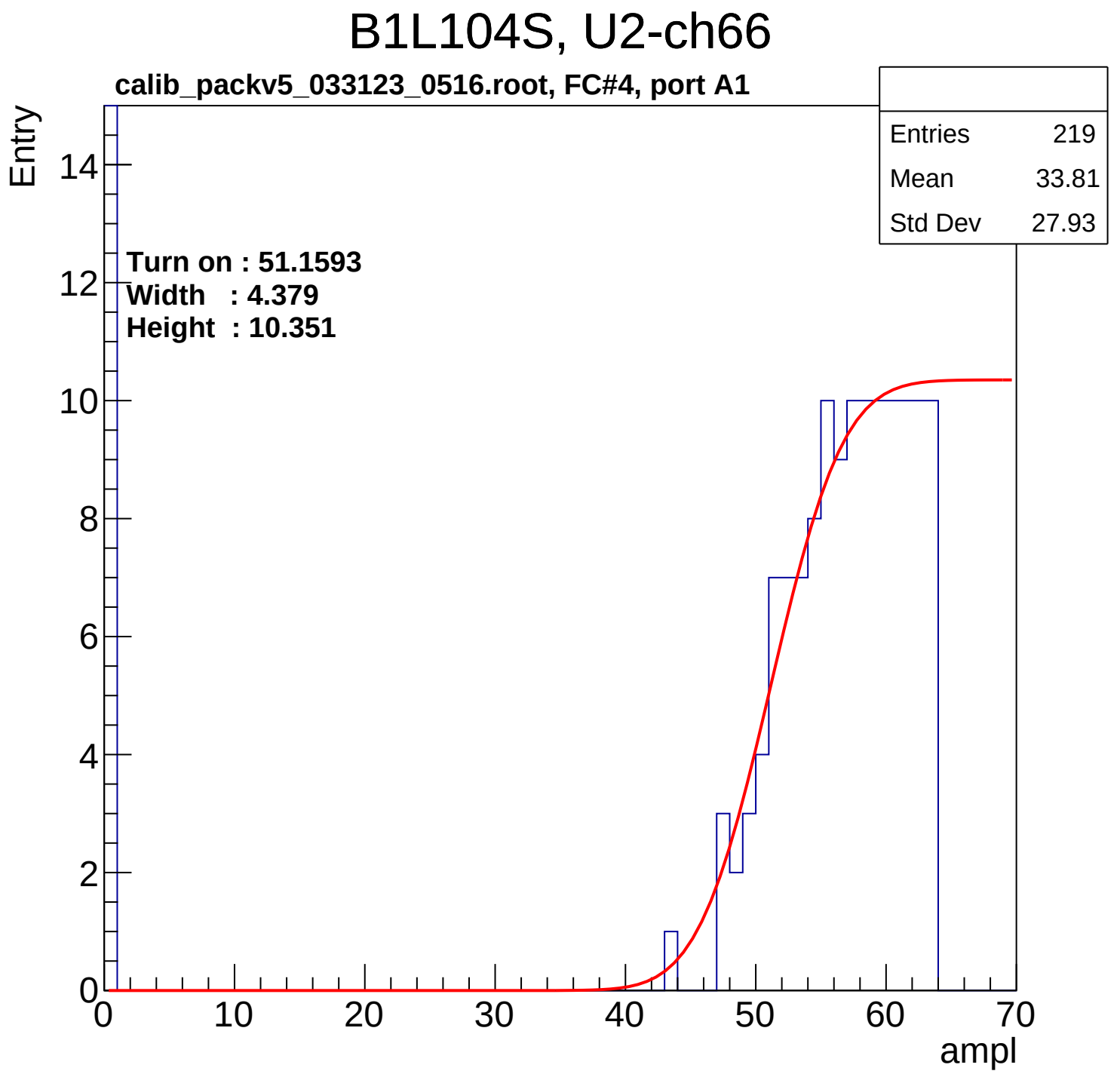
B1L104S, U2-ch66
calib_packv5_033123_0516.root, FC#4, port A1
Entries 219
Mean 33.81
Std Dev 27.93
Turn on : 51.1593
Width : 4.379
Height : 10.351
Entry
ampl
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6
8
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12
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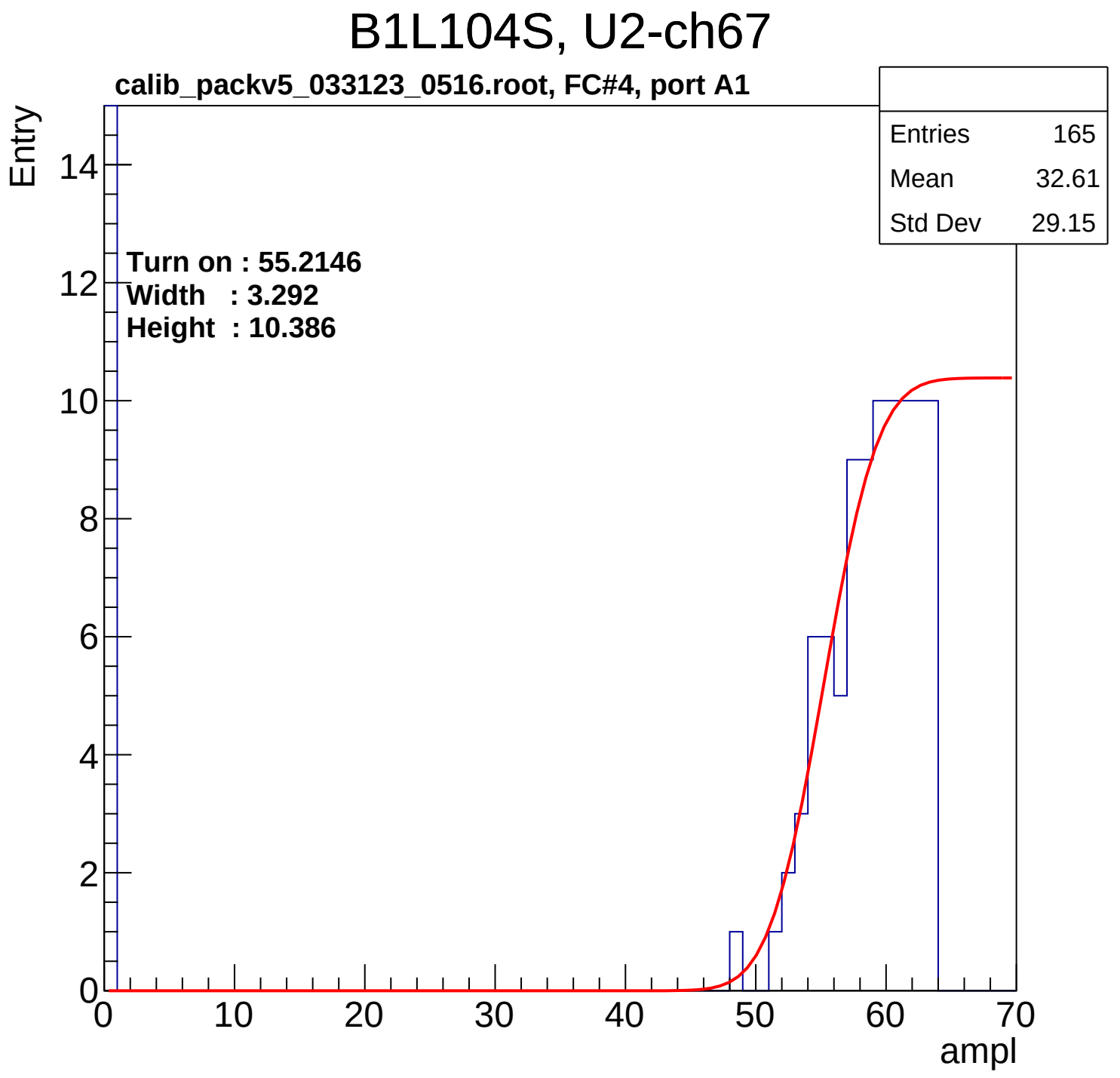
B1L104S, U2-ch67
calib_packv5_033123_0516.root, FC#4, port A1
Entries 165
Mean 32.61
Std Dev 29.15
Turn on : 55.2146
Width : 3.292
Height : 10.386
Entry
ampl
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4
6
8
10
12
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0
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20
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60
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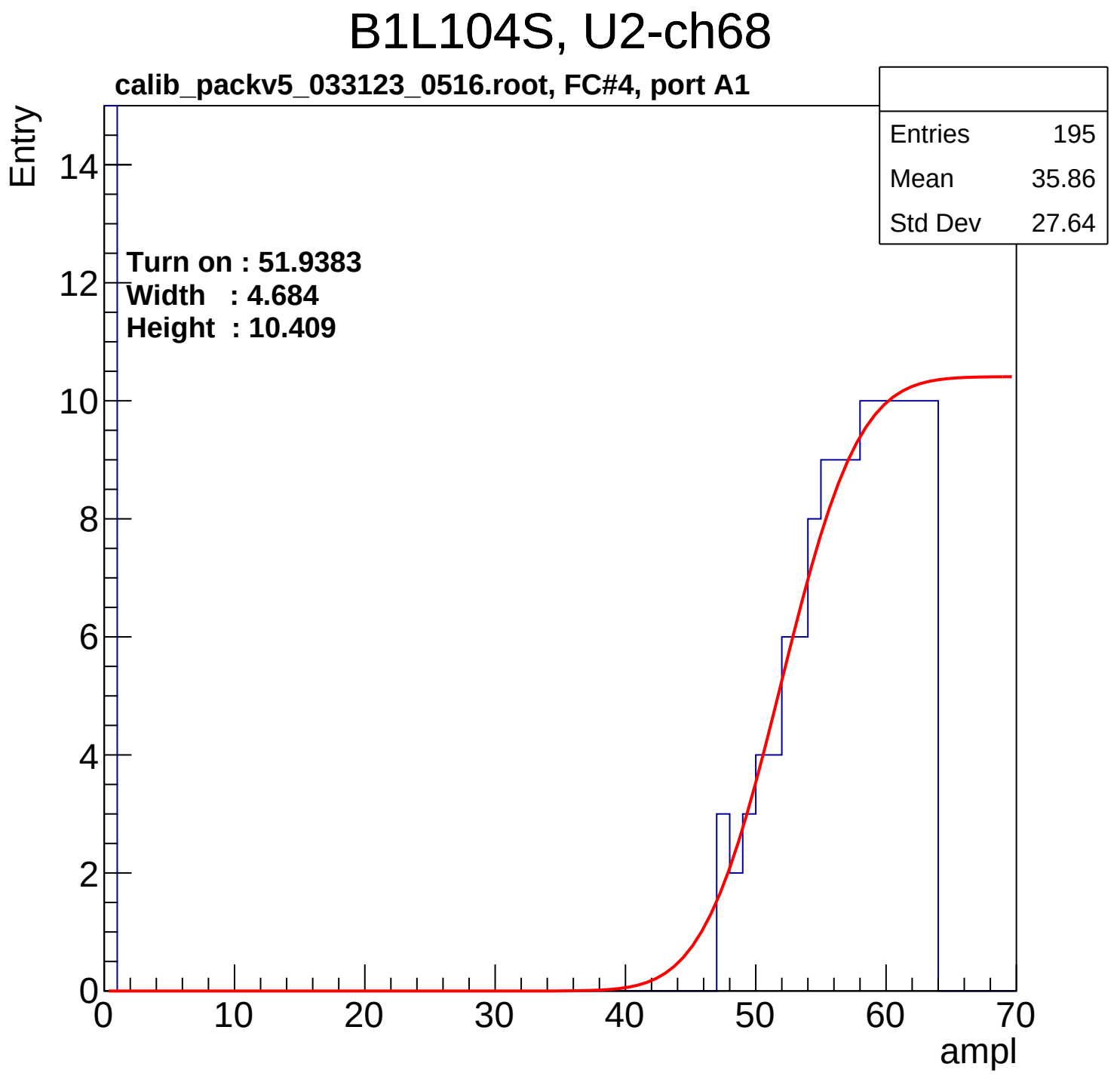
B1L104S, U2-ch68
calib_packv5_033123_0516.root, FC#4, port A1
Entries 195
Mean 35.86
Std Dev 27.64
Turn on : 51.9383
Width : 4.684
Height : 10.409
Entry
ampl
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4
6
8
10
12
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20
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60
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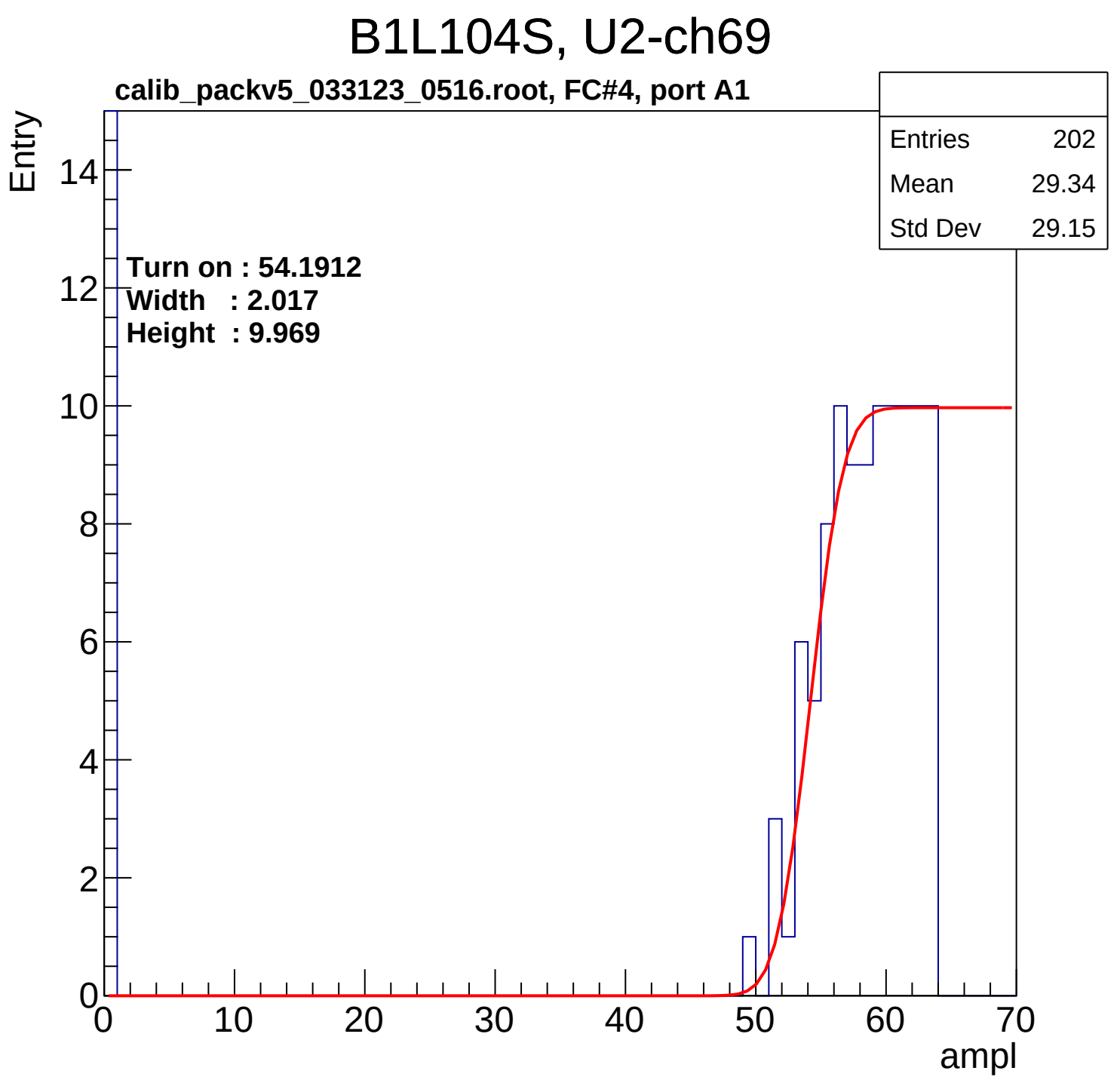
B1L104S, U2-ch69
calib_packv5_033123_0516.root, FC#4, port A1
Entries 202
Mean 29.34
Std Dev 29.15
Turn on : 54.1912
Width : 2.017
Height : 9.969
Entry
ampl
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2
4
6
8
10
12
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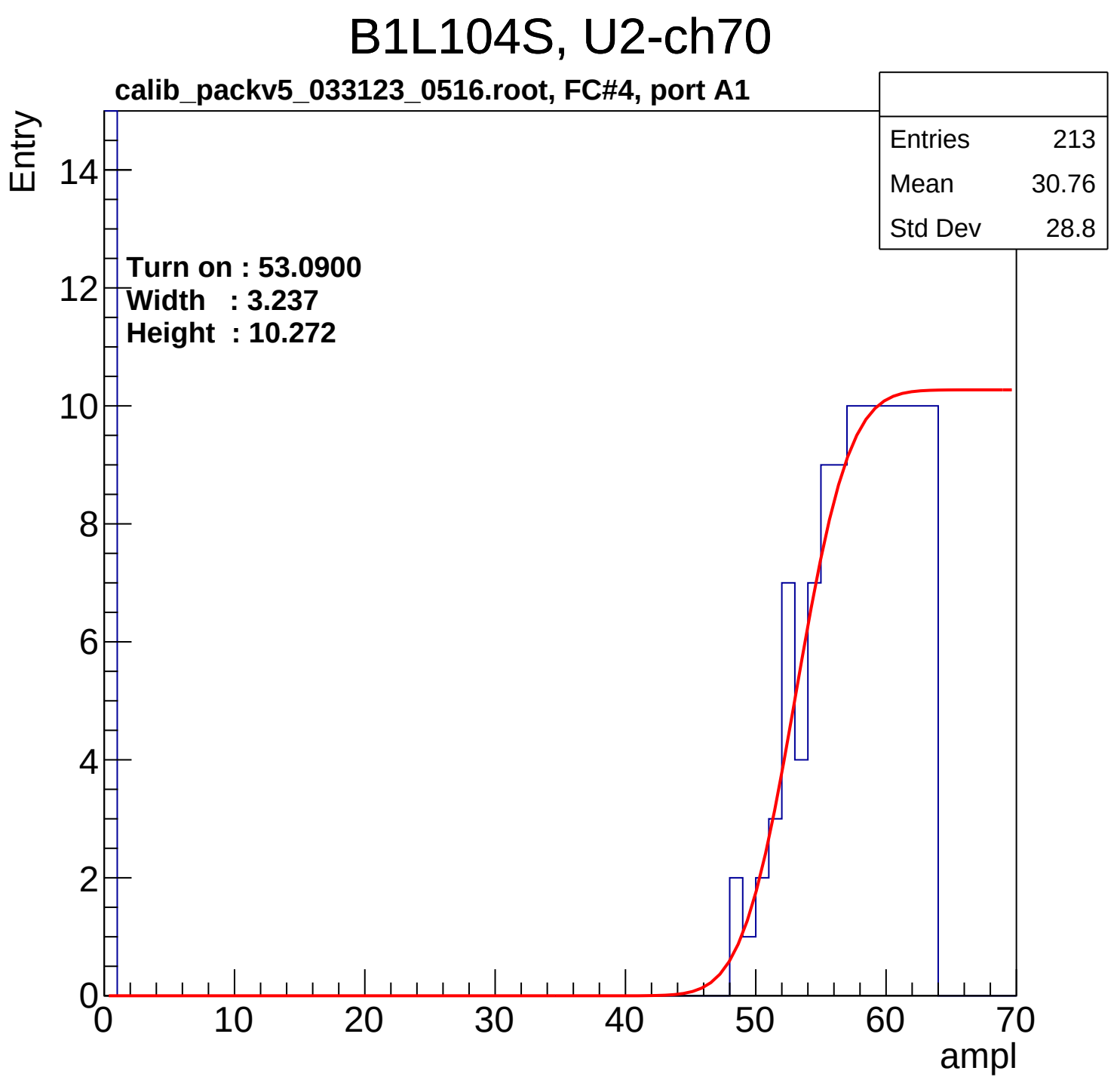
B1L104S, U2-ch70
calib_packv5_033123_0516.root, FC#4, port A1
Entries 213
Mean 30.76
Std Dev 28.8
Turn on : 53.0900
Width : 3.237
Height : 10.272
Entry
ampl
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6
8
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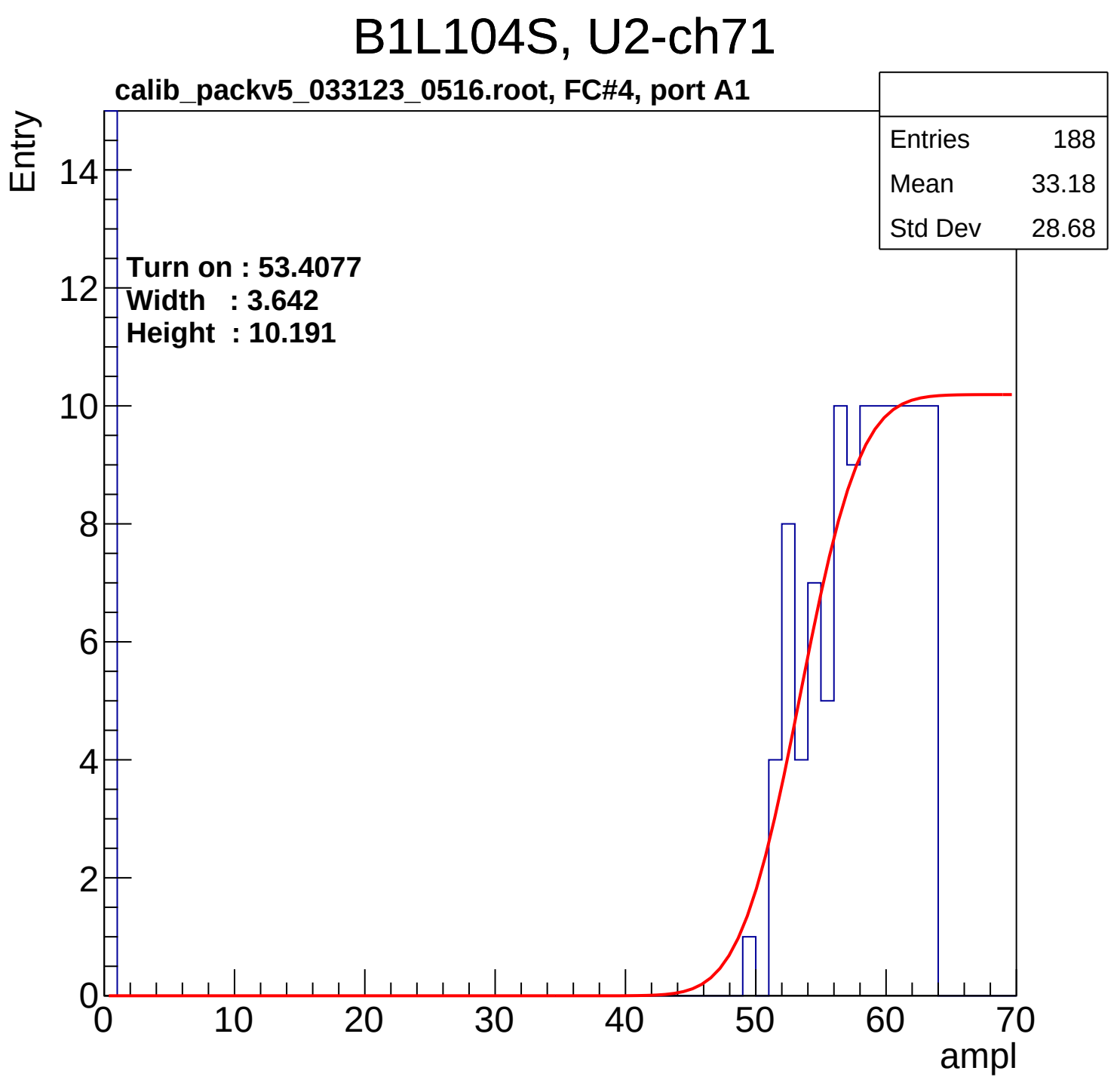
B1L104S, U2-ch71
calib_packv5_033123_0516.root, FC#4, port A1
Entries 188
Mean 33.18
Std Dev 28.68
Turn on : 53.4077
Width : 3.642
Height : 10.191
Entry
ampl
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8
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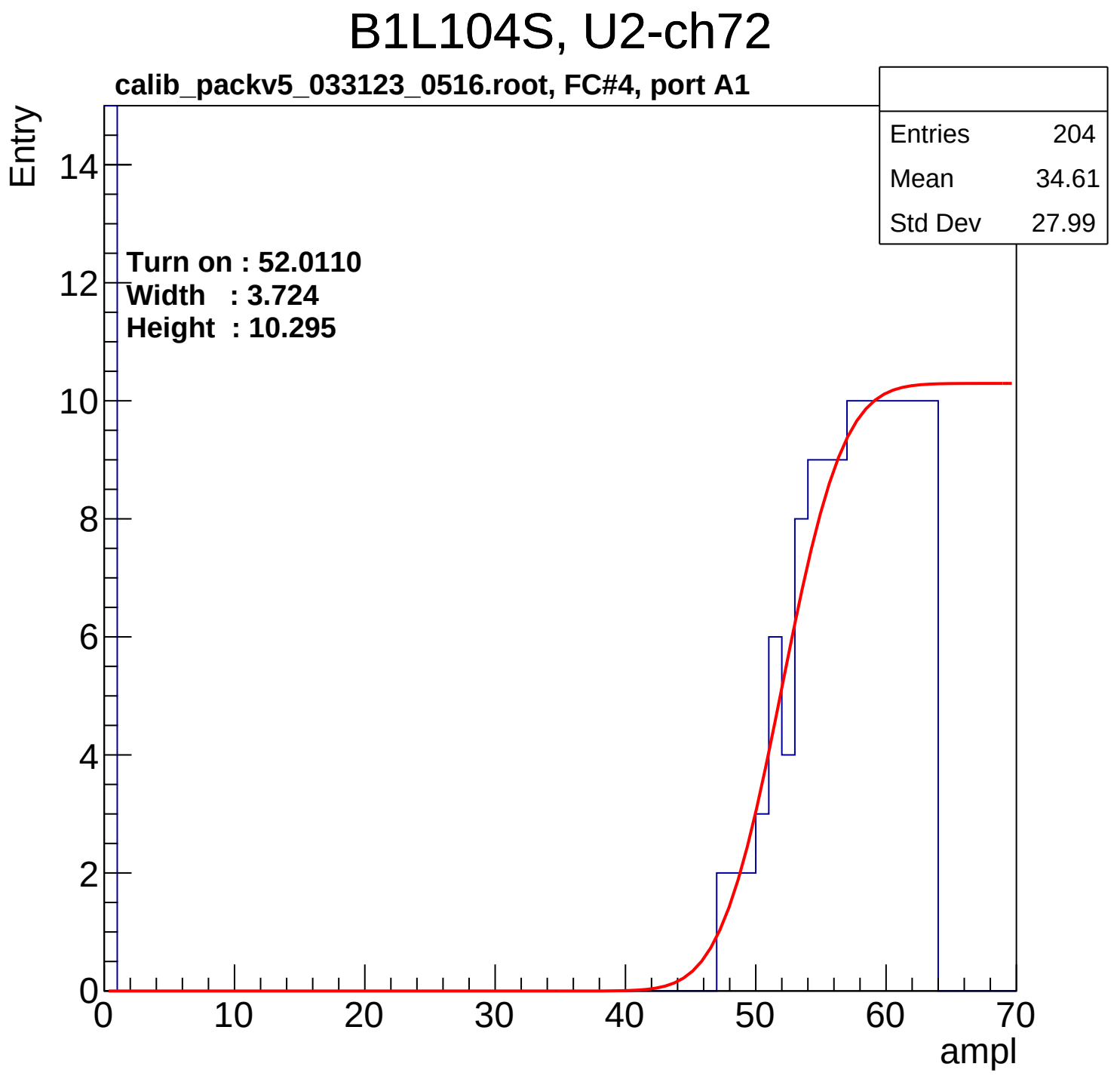
B1L104S, U2-ch72
calib_packv5_033123_0516.root, FC#4, port A1
Entries 204
Mean 34.61
Std Dev 27.99
Turn on : 52.0110
Width : 3.724
Height : 10.295
Entry
ampl
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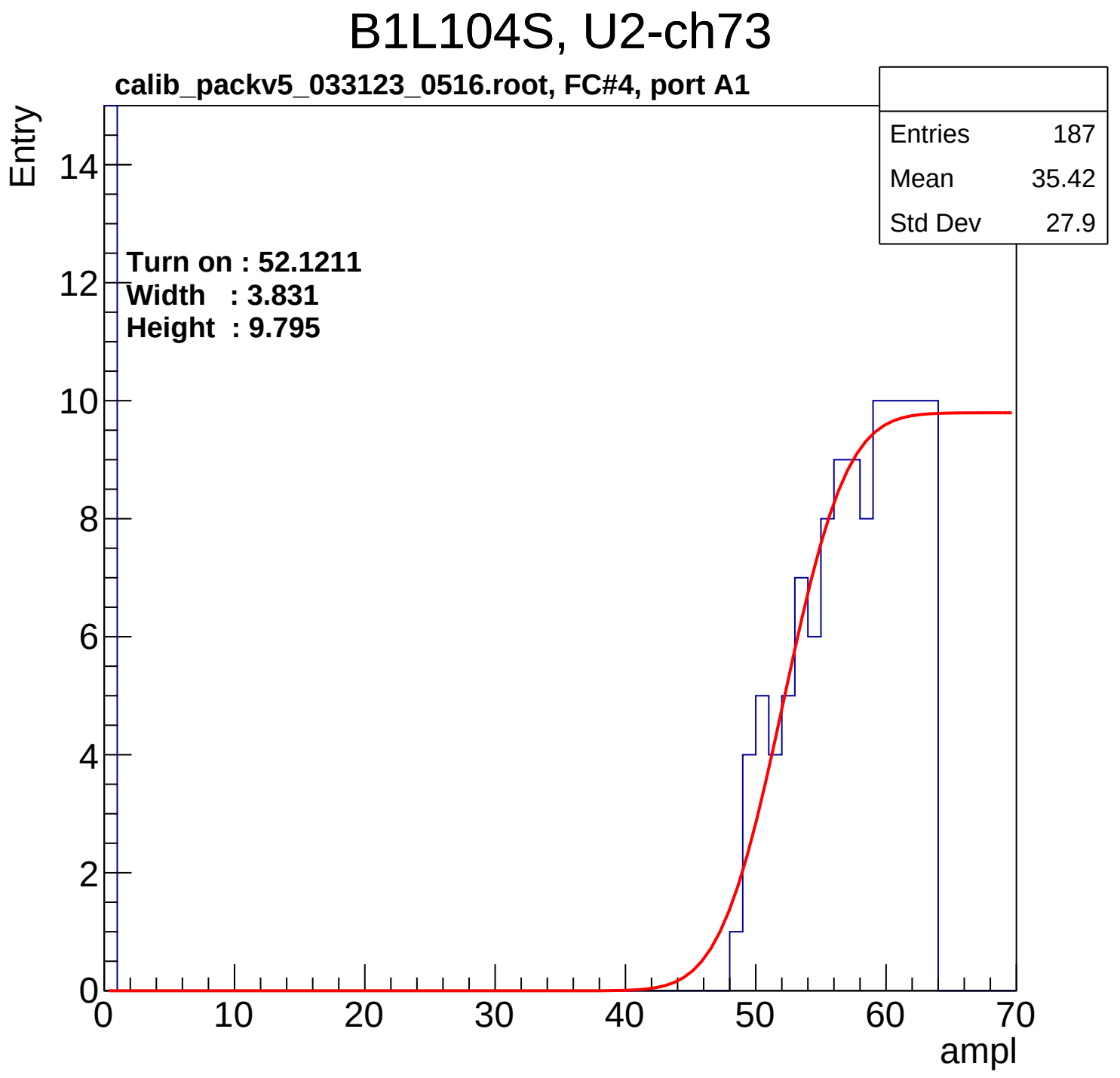
B1L104S, U2-ch73
calib_packv5_033123_0516.root, FC#4, port A1
Entries 187
Mean 35.42
Std Dev 27.9
Turn on : 52.1211
Width : 3.831
Height : 9.795
Entry
ampl
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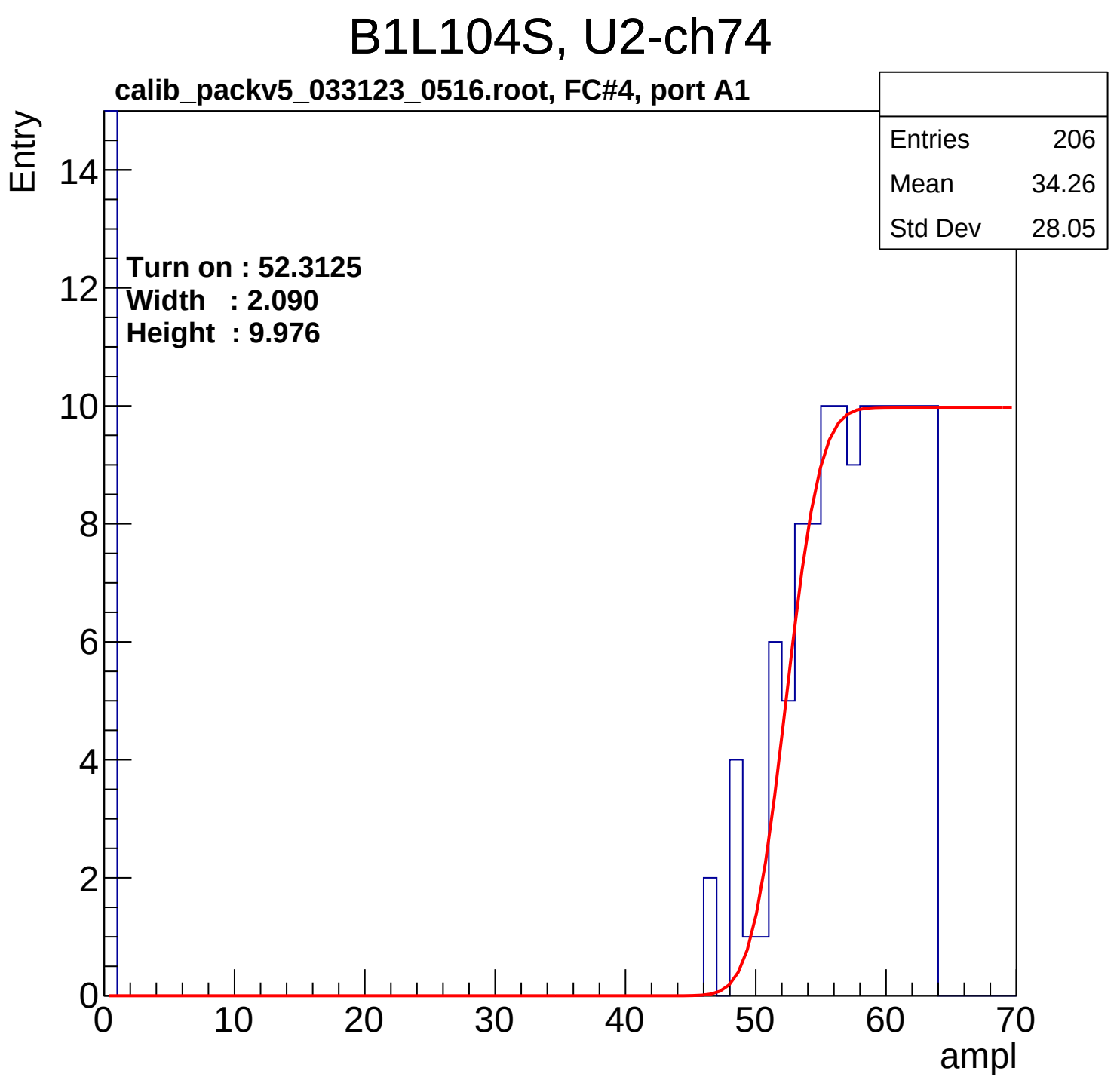
B1L104S, U2-ch74
calib_packv5_033123_0516.root, FC#4, port A1
Entries 206
Mean 34.26
Std Dev 28.05
Turn on : 52.3125
Width : 2.090
Height : 9.976
Entry
ampl
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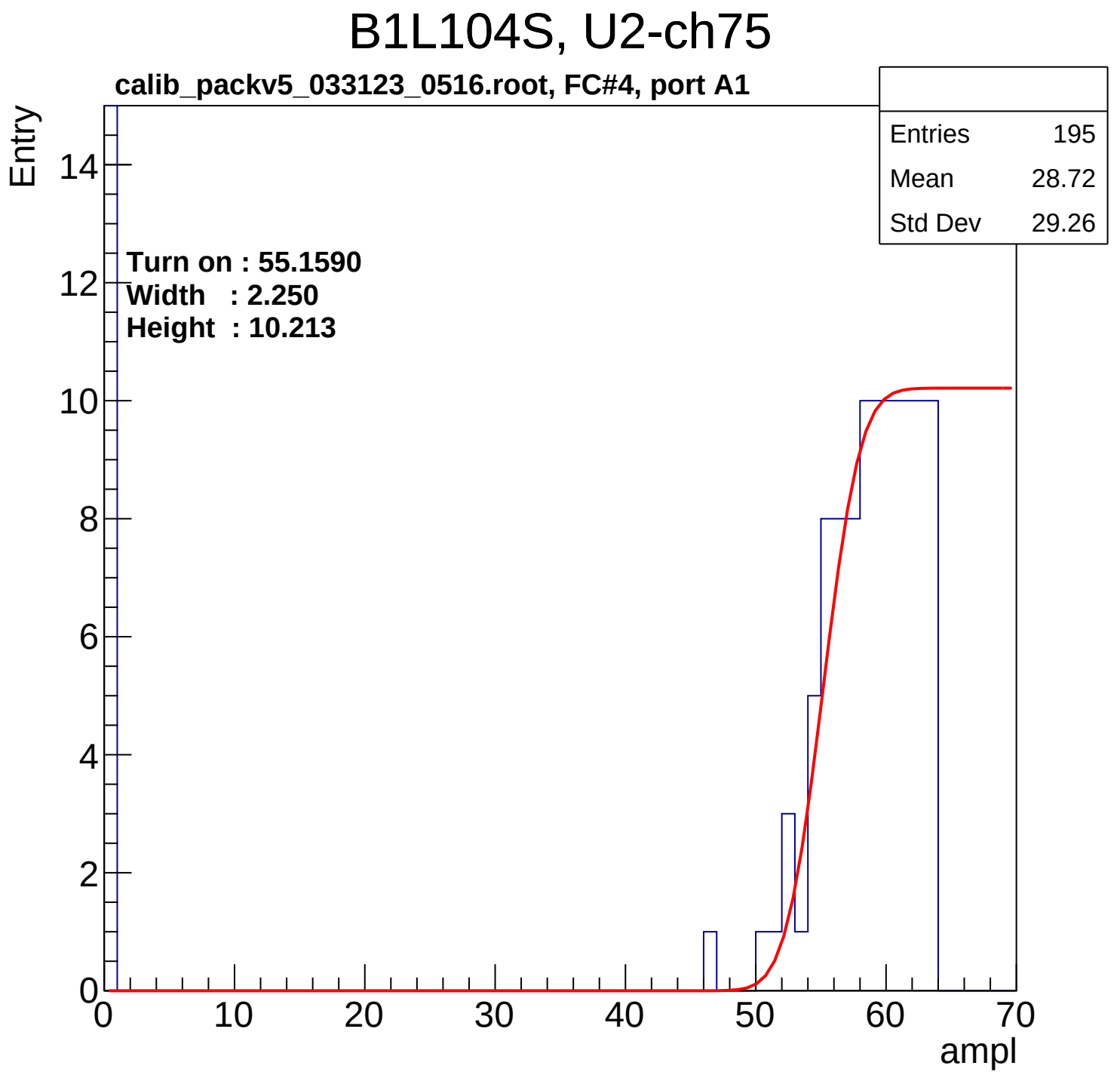
B1L104S, U2-ch75
calib_packv5_033123_0516.root, FC#4, port A1
Entries 195
Mean 28.72
Std Dev 29.26
Turn on : 55.1590
Width : 2.250
Height : 10.213
Entry
ampl
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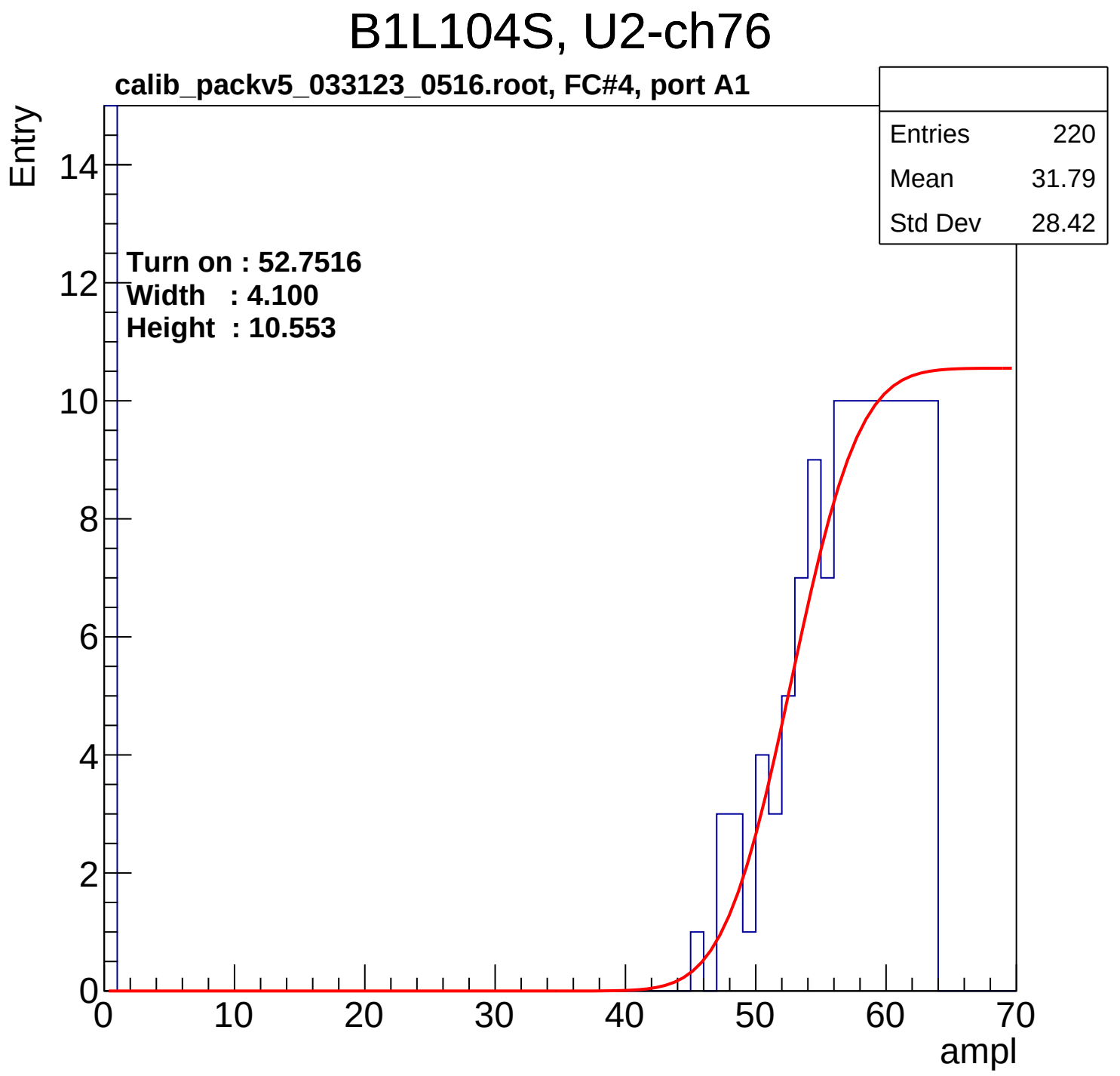
B1L104S, U2-ch76
calib_packv5_033123_0516.root, FC#4, port A1
Entries 220
Mean 31.79
Std Dev 28.42
Turn on : 52.7516
Width : 4.100
Height : 10.553
Entry
ampl
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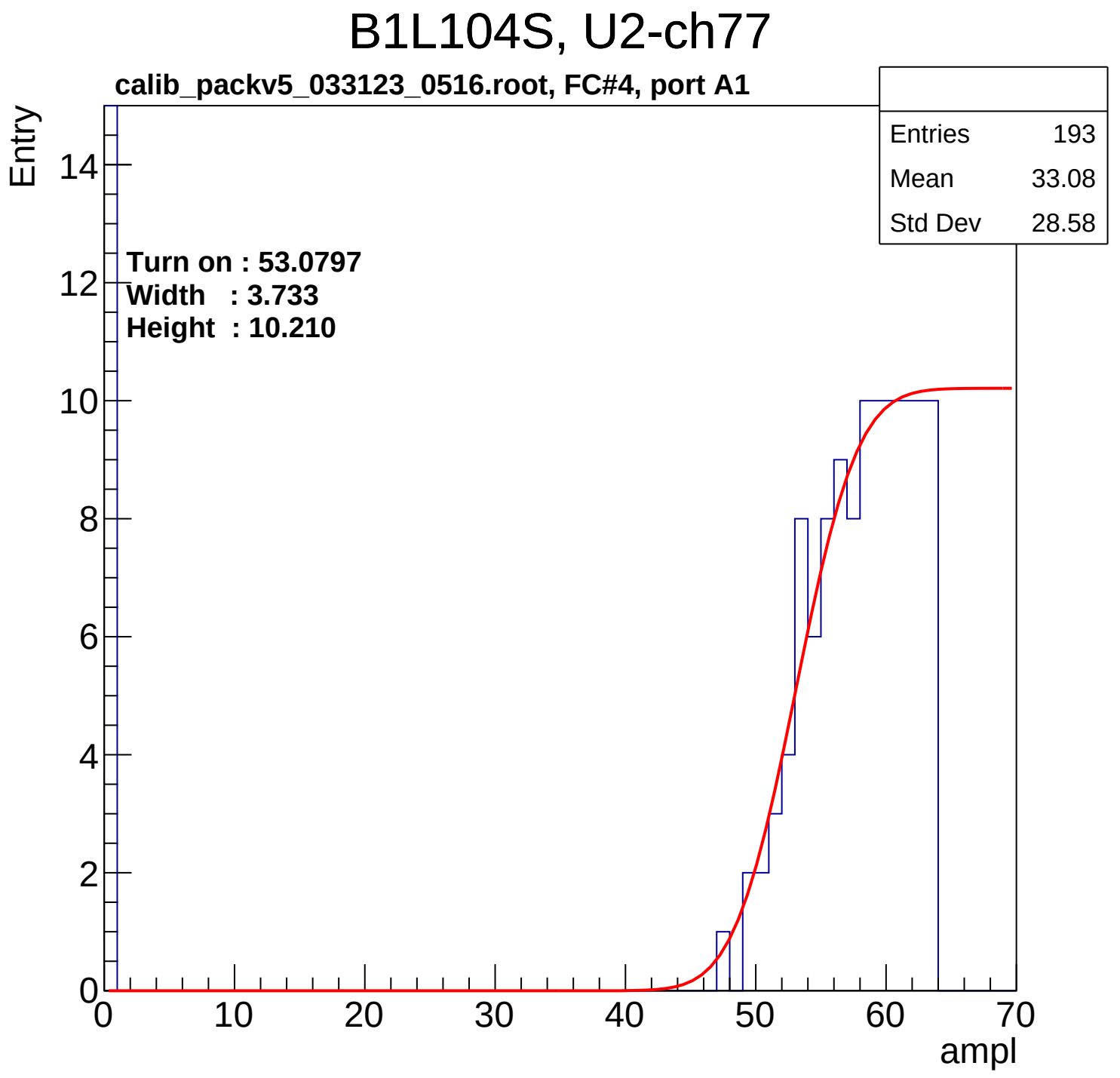
B1L104S, U2-ch77
calib_packv5_033123_0516.root, FC#4, port A1
Entries 193
Mean 33.08
Std Dev 28.58
Turn on : 53.0797
Width : 3.733
Height : 10.210
Entry
ampl
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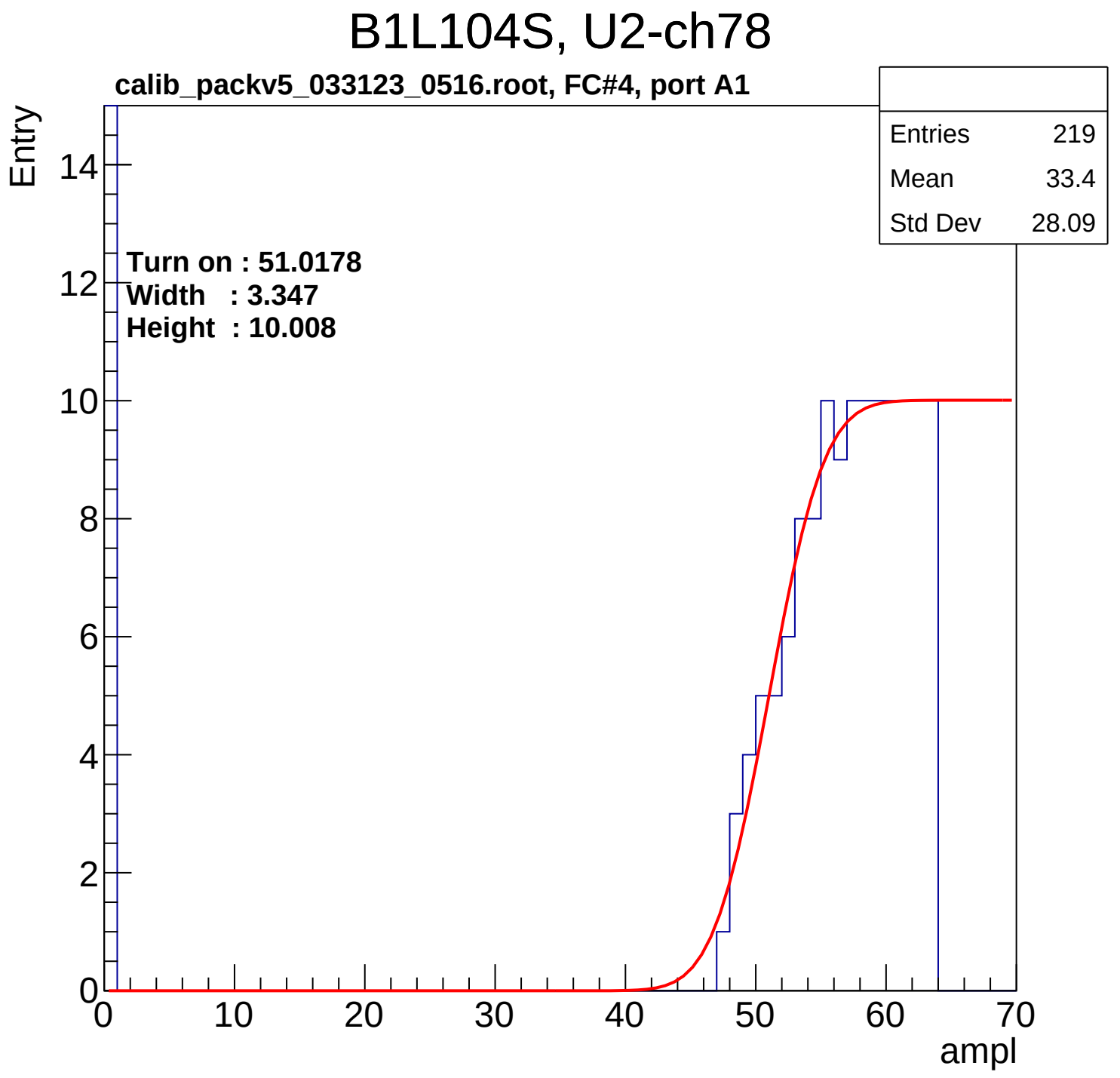
B1L104S, U2-ch78
calib_packv5_033123_0516.root, FC#4, port A1
Entries 219
Mean 33.4
Std Dev 28.09
Turn on : 51.0178
Width : 3.347
Height : 10.008
Entry
ampl
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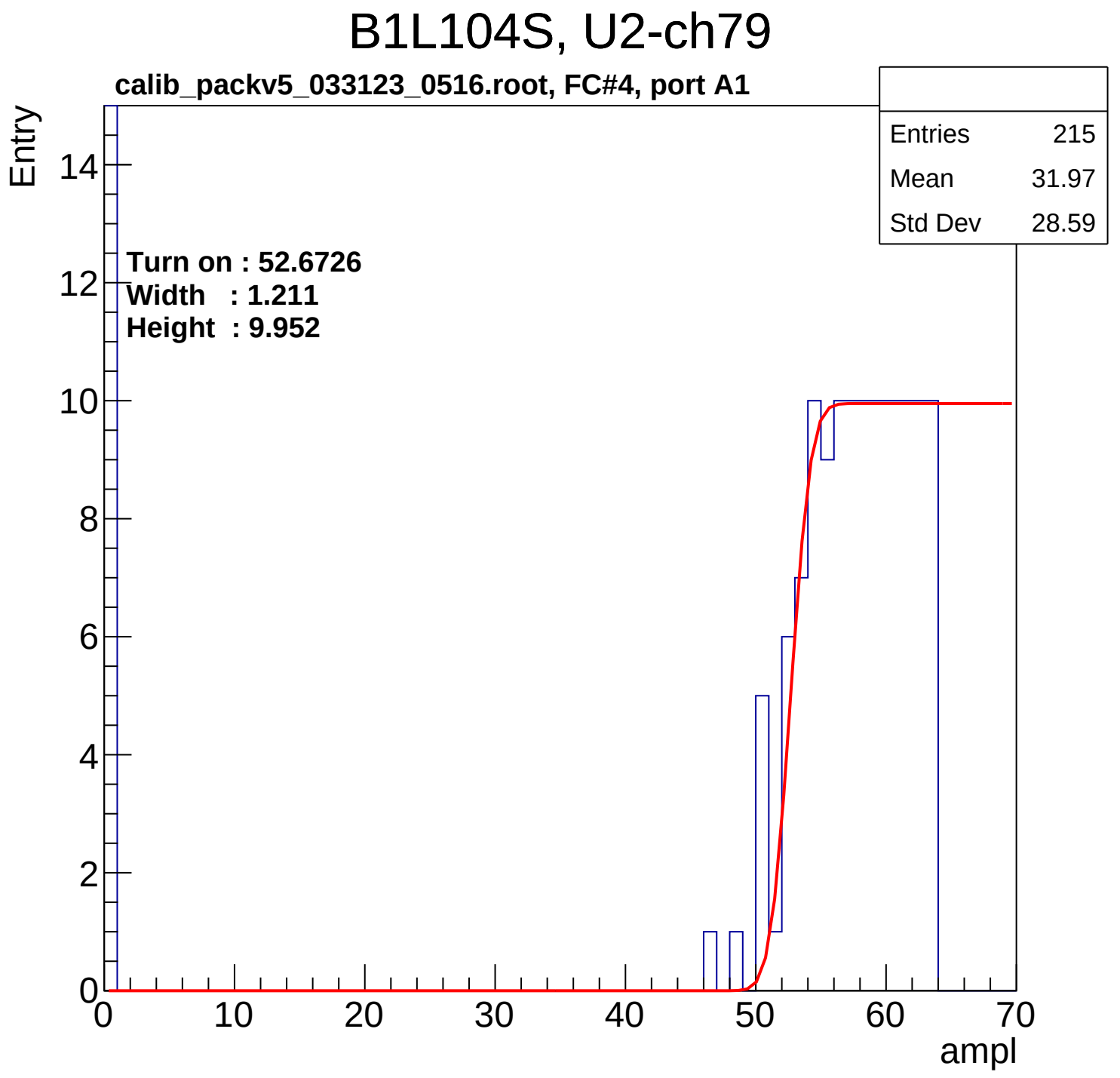
B1L104S, U2-ch79
calib_packv5_033123_0516.root, FC#4, port A1
Entries 215
Mean 31.97
Std Dev 28.59
Turn on : 52.6726
Width : 1.211
Height : 9.952
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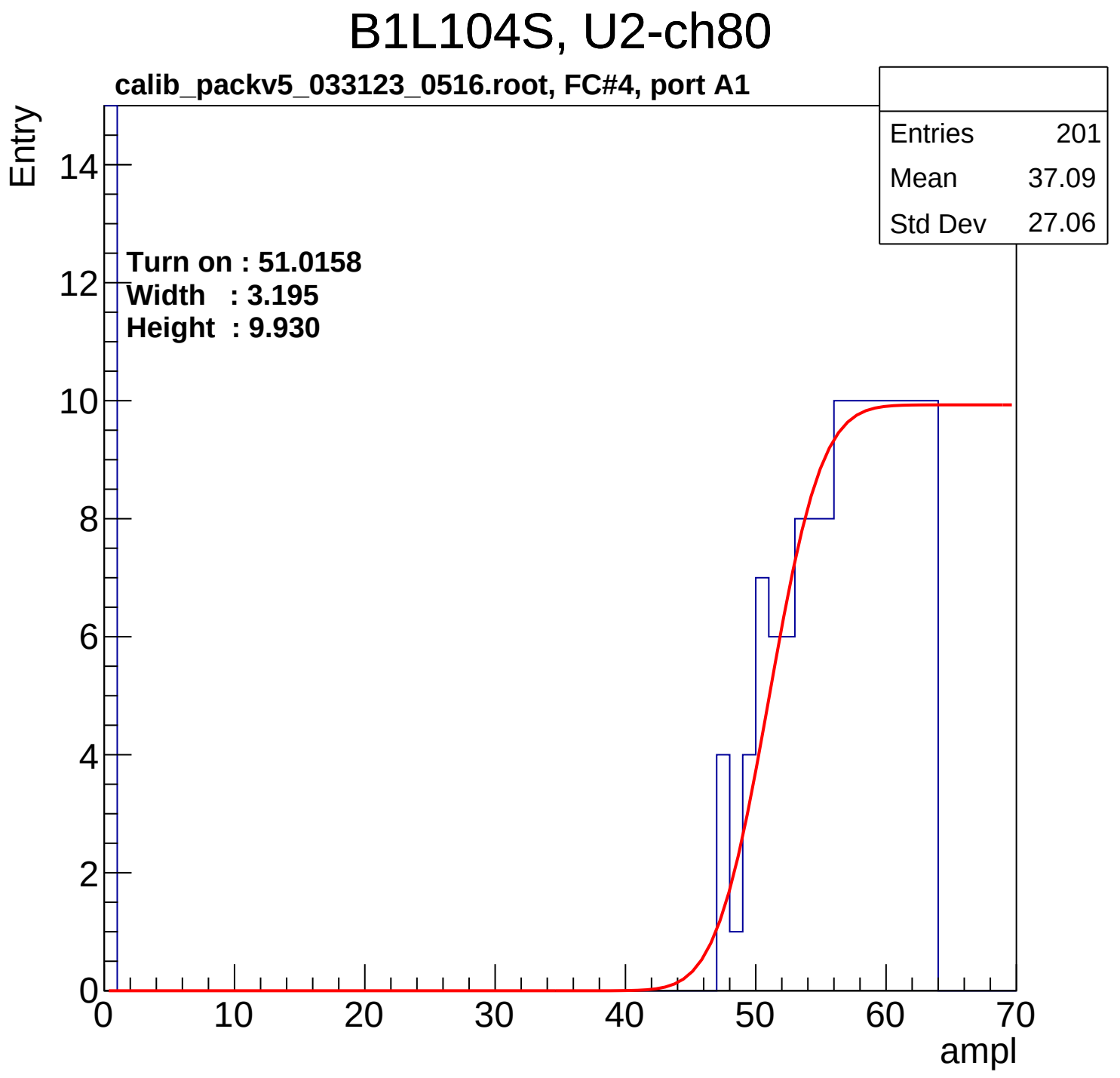
B1L104S, U2-ch80
calib_packv5_033123_0516.root, FC#4, port A1
Entries 201
Mean 37.09
Std Dev 27.06
Turn on : 51.0158
Width : 3.195
Height : 9.930
Entry
ampl
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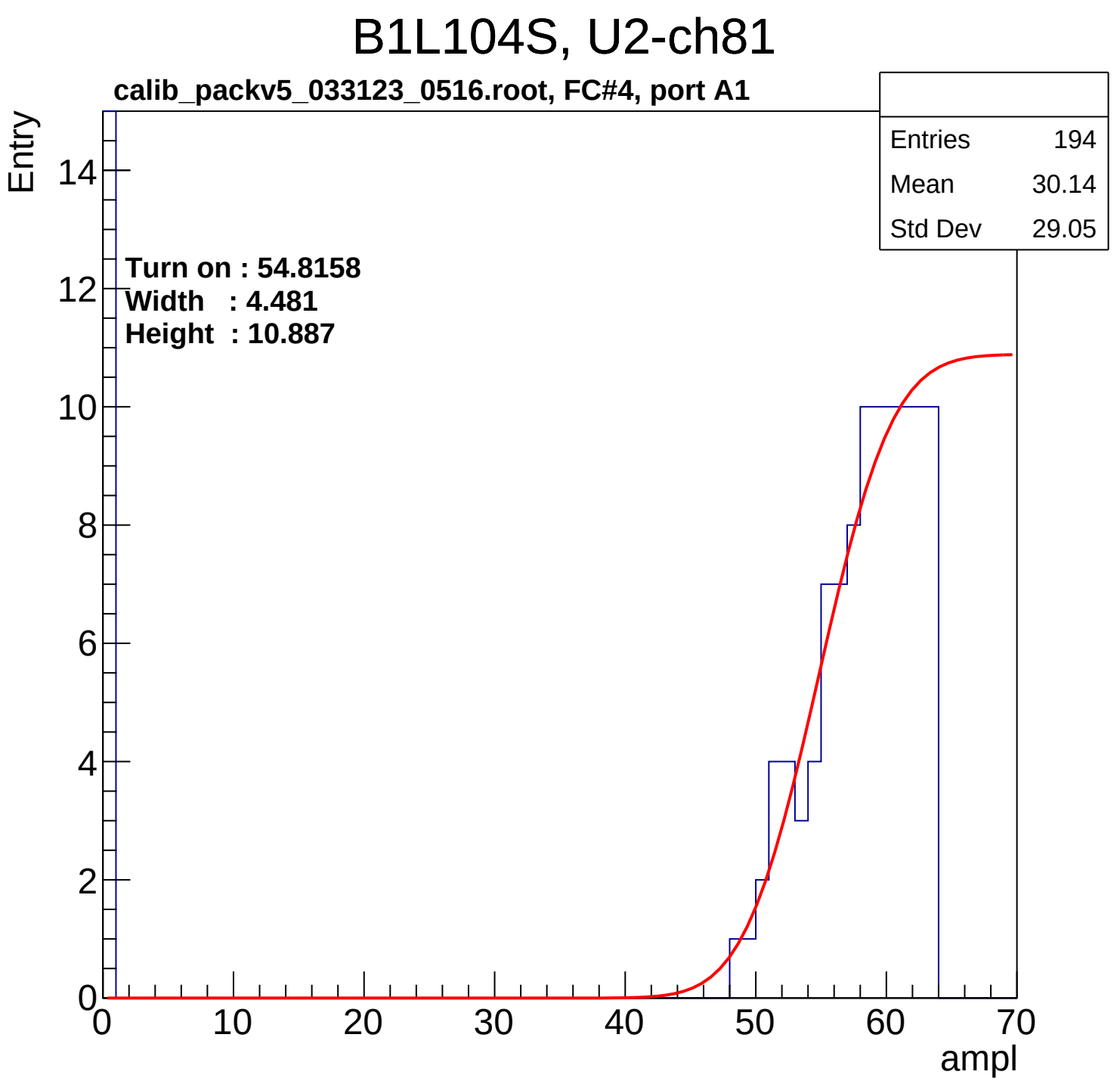
B1L104S, U2-ch81
calib_packv5_033123_0516.root, FC#4, port A1
Entries 194
Mean 30.14
Std Dev 29.05
Turn on : 54.8158
Width : 4.481
Height : 10.887
Entry
ampl
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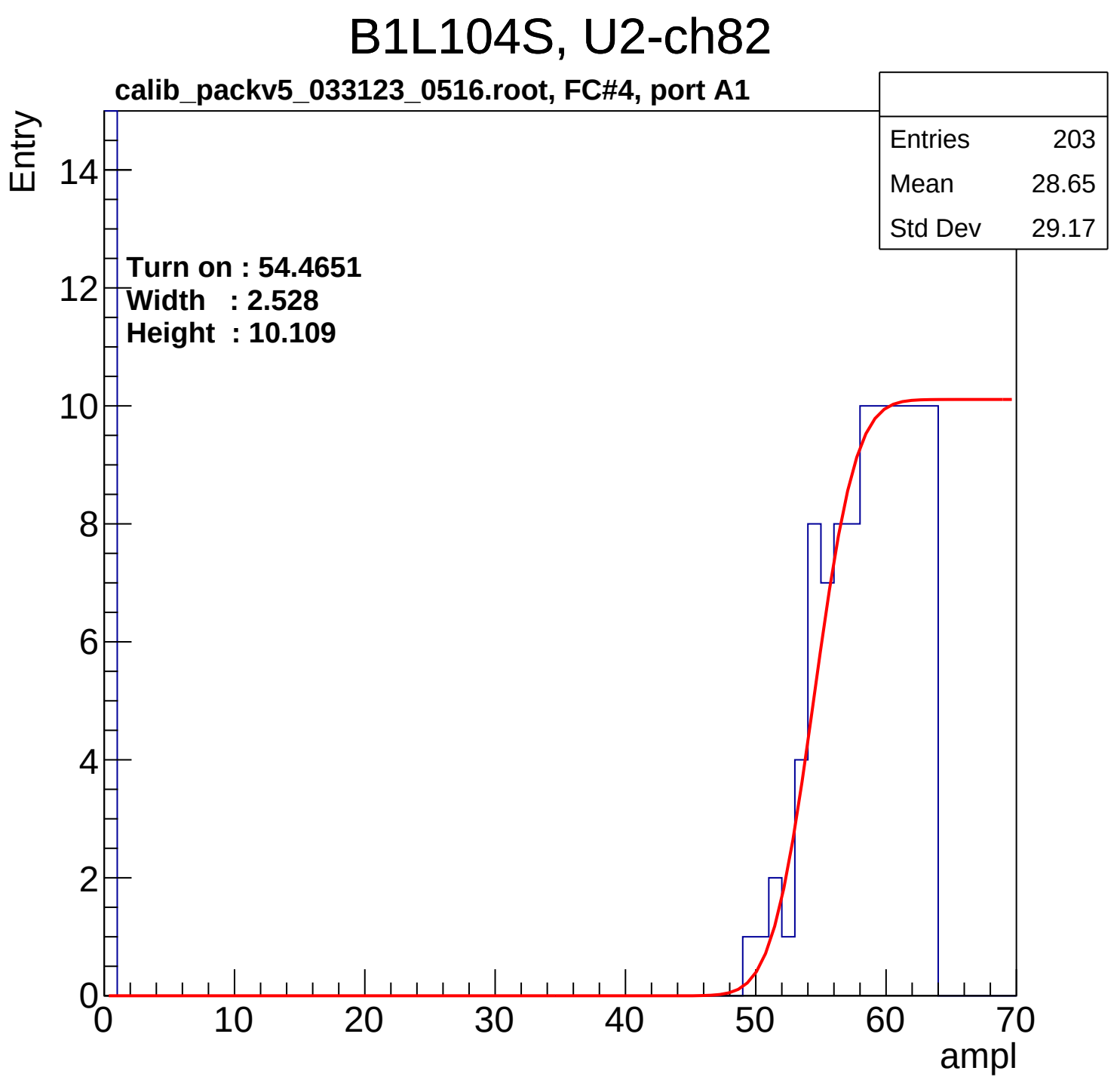
B1L104S, U2-ch82
calib_packv5_033123_0516.root, FC#4, port A1
Entries 203
Mean 28.65
Std Dev 29.17
Turn on : 54.4651
Width : 2.528
Height : 10.109
Entry
ampl
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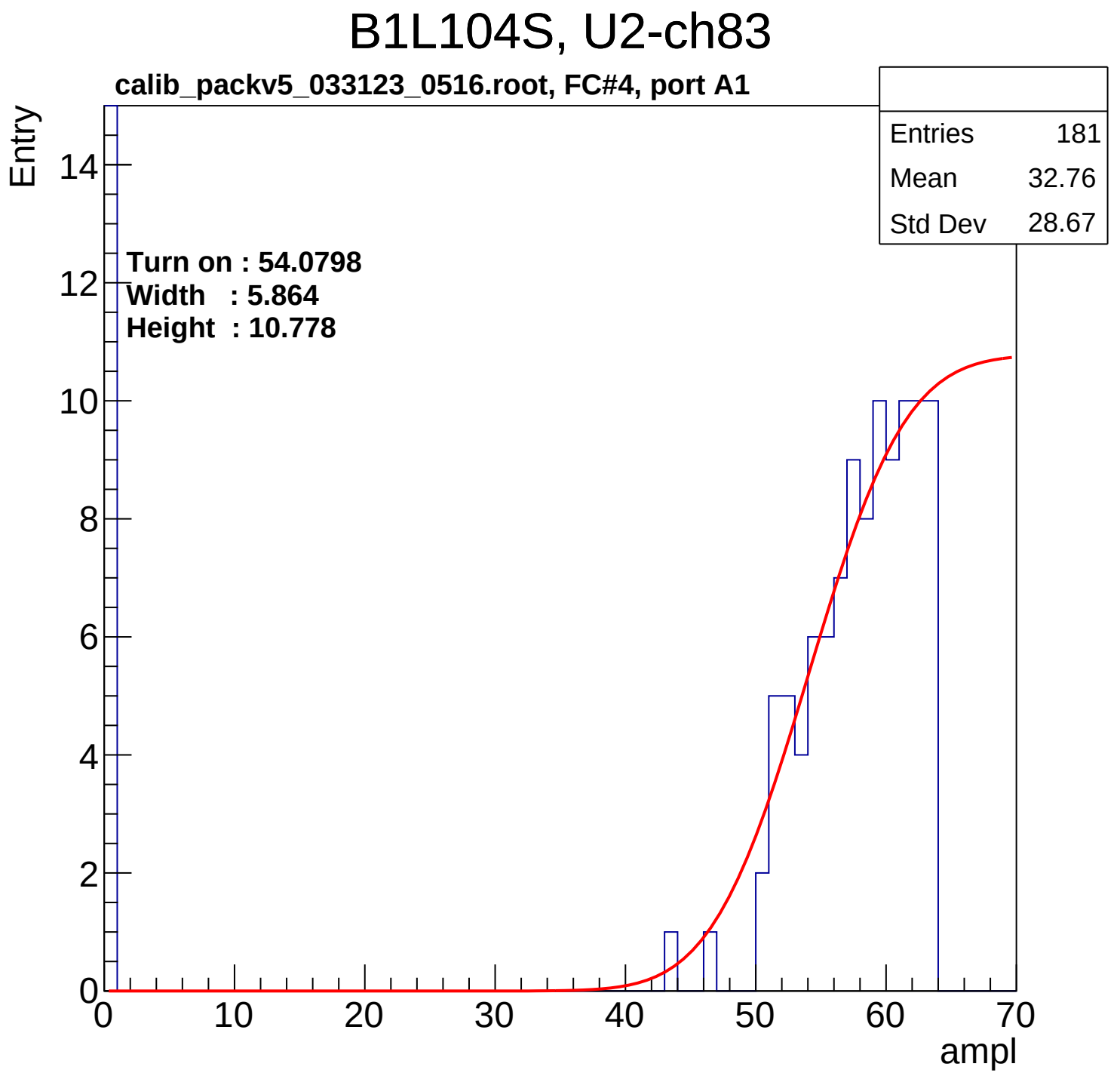
B1L104S, U2-ch83
calib_packv5_033123_0516.root, FC#4, port A1
Entries 181
Mean 32.76
Std Dev 28.67
Turn on : 54.0798
Width : 5.864
Height : 10.778
Entry
ampl
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8
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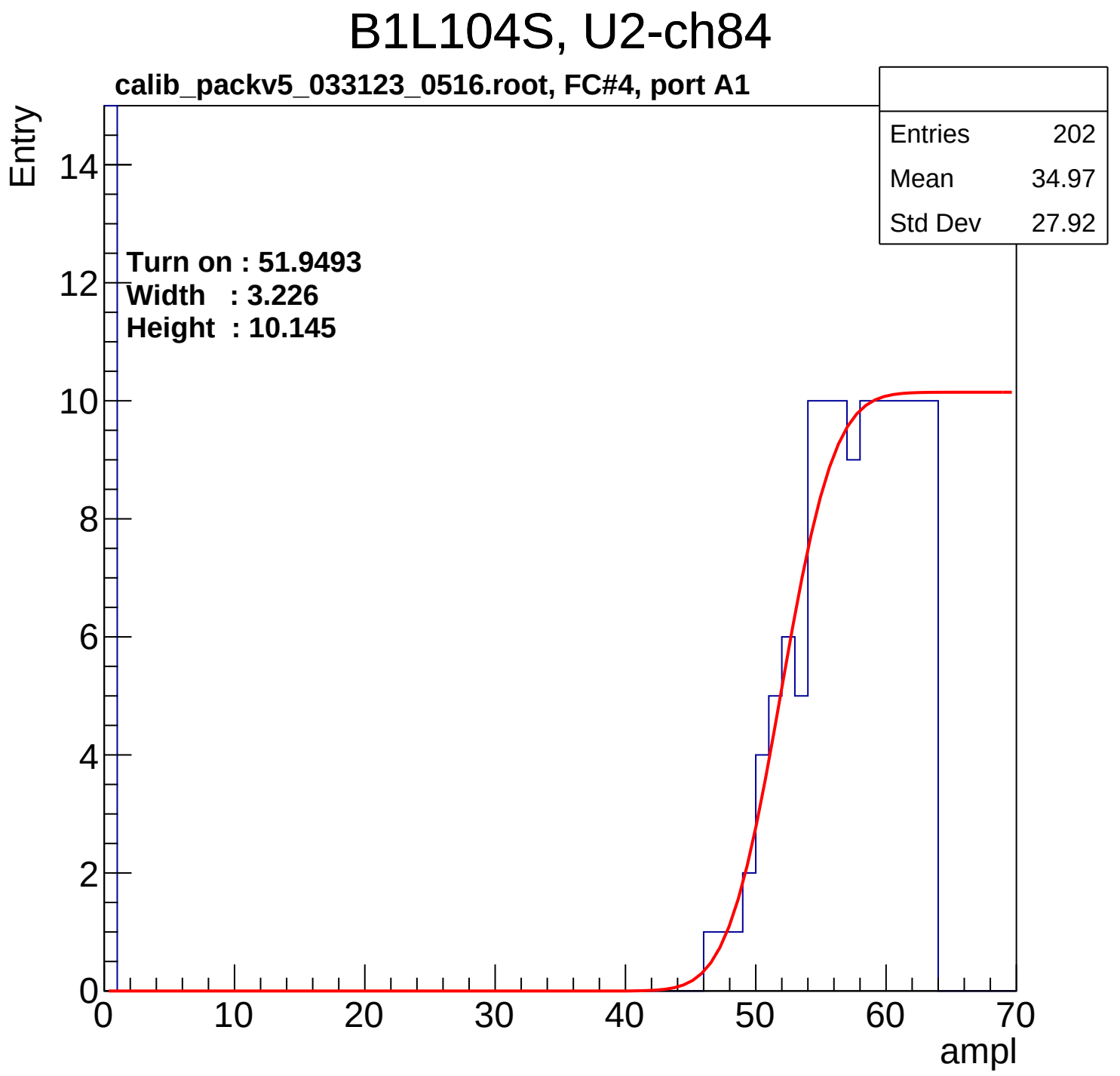
B1L104S, U2-ch84
calib_packv5_033123_0516.root, FC#4, port A1
Entries 202
Mean 34.97
Std Dev 27.92
Turn on : 51.9493
Width : 3.226
Height : 10.145
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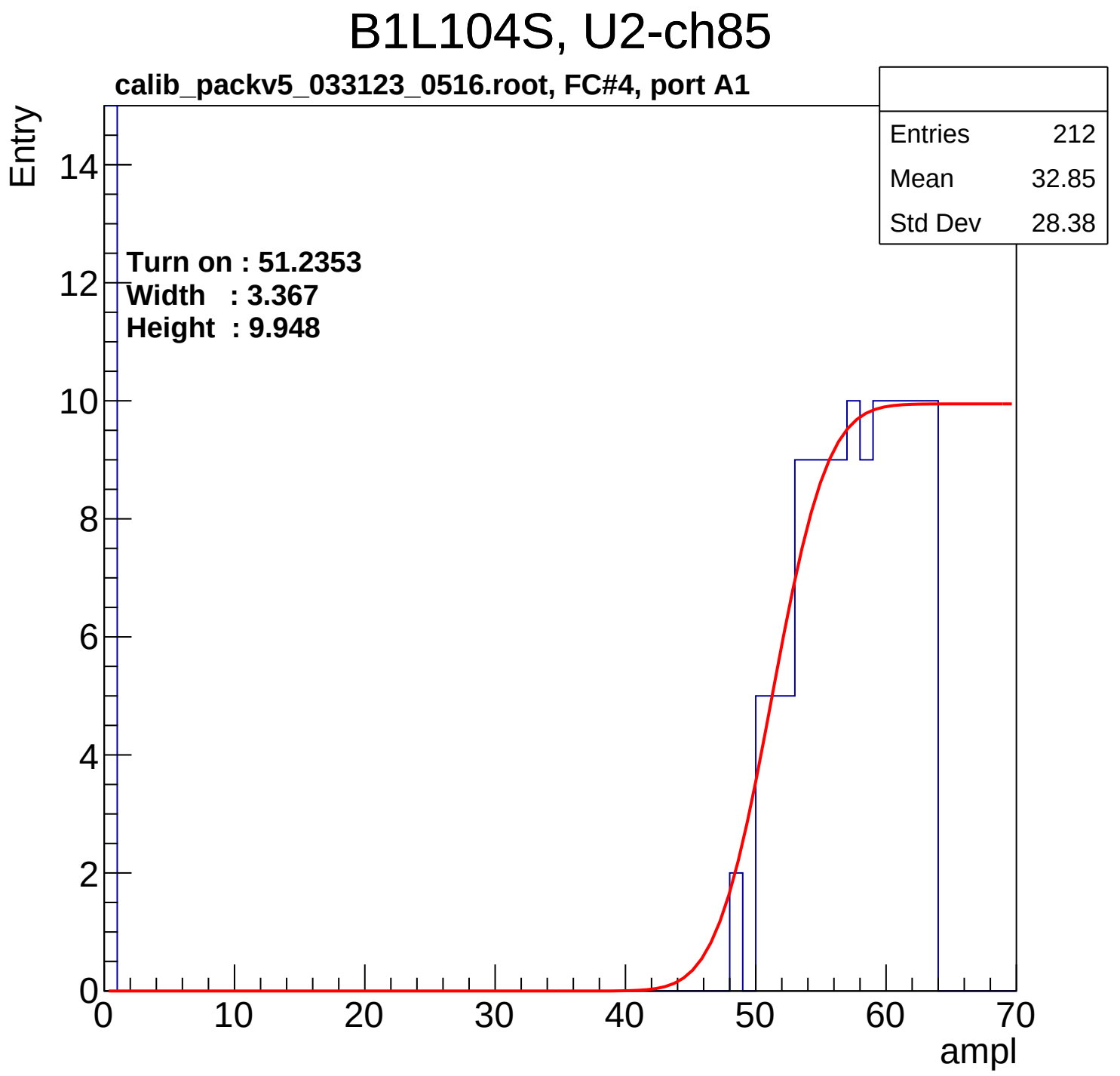
B1L104S, U2-ch85
calib_packv5_033123_0516.root, FC#4, port A1
Entries 212
Mean 32.85
Std Dev 28.38
Turn on : 51.2353
Width : 3.367
Height : 9.948
Entry
ampl
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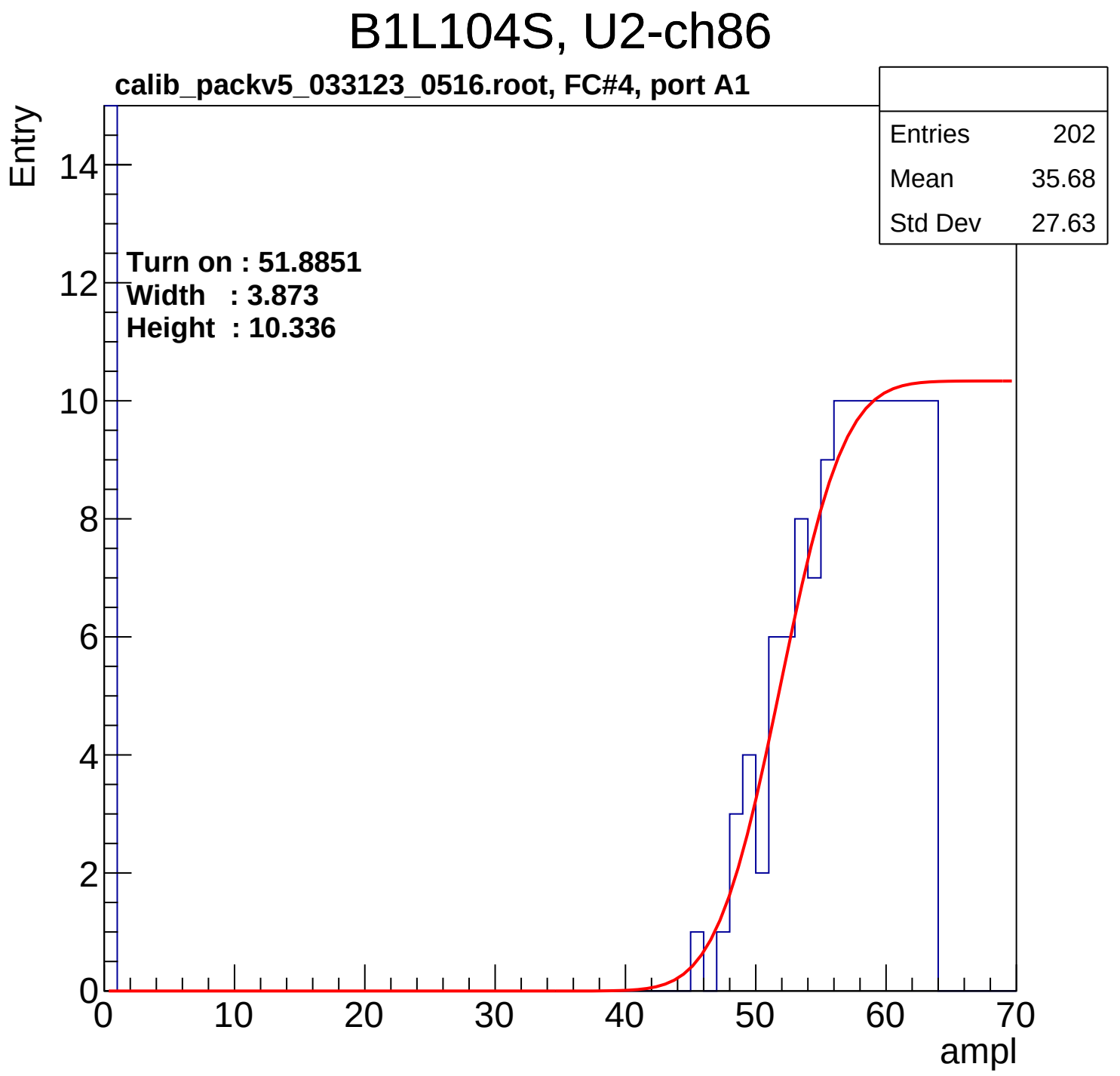
B1L104S, U2-ch86
calib_packv5_033123_0516.root, FC#4, port A1
Entries 202
Mean 35.68
Std Dev 27.63
Turn on : 51.8851
Width : 3.873
Height : 10.336
Entry
ampl
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6
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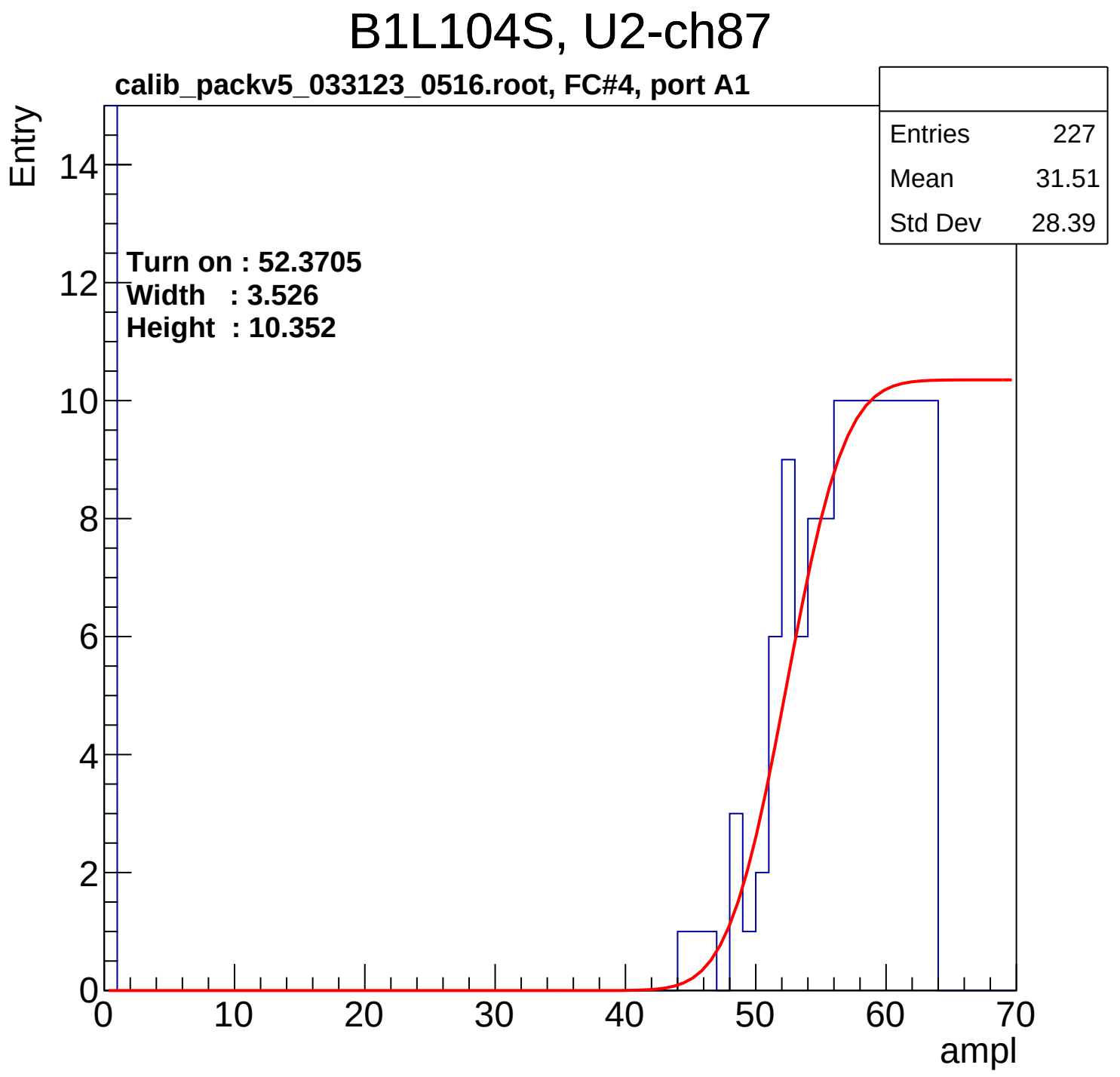
B1L104S, U2-ch87
calib_packv5_033123_0516.root, FC#4, port A1
Entries 227
Mean 31.51
Std Dev 28.39
Turn on : 52.3705
Width : 3.526
Height : 10.352
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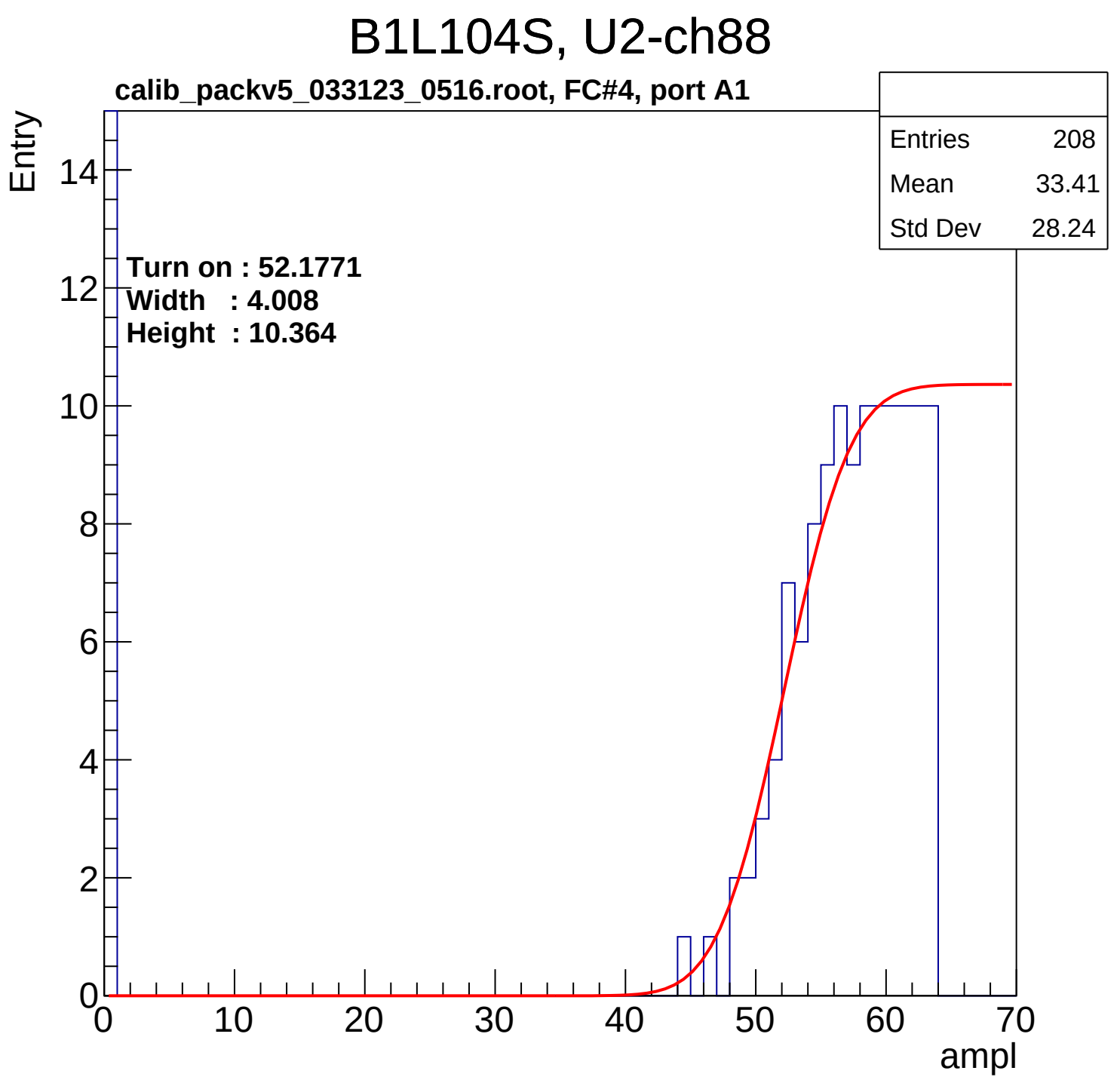
B1L104S, U2-ch88
calib_packv5_033123_0516.root, FC#4, port A1
Entries 208
Mean 33.41
Std Dev 28.24
Turn on : 52.1771
Width : 4.008
Height : 10.364
Entry
ampl
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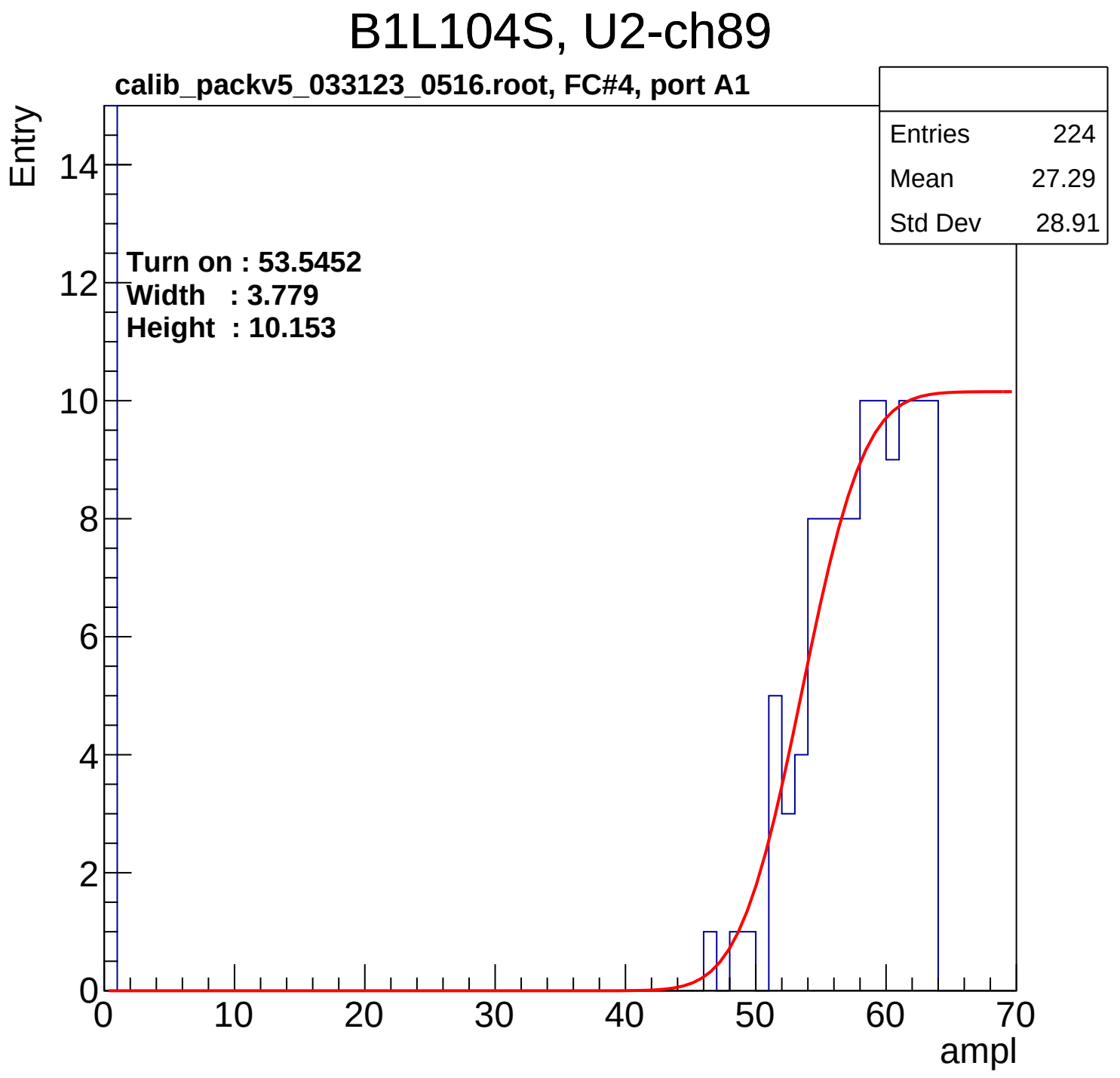
B1L104S, U2-ch89
calib_packv5_033123_0516.root, FC#4, port A1
Entries 224
Mean 27.29
Std Dev 28.91
Turn on : 53.5452
Width : 3.779
Height : 10.153
Entry
ampl
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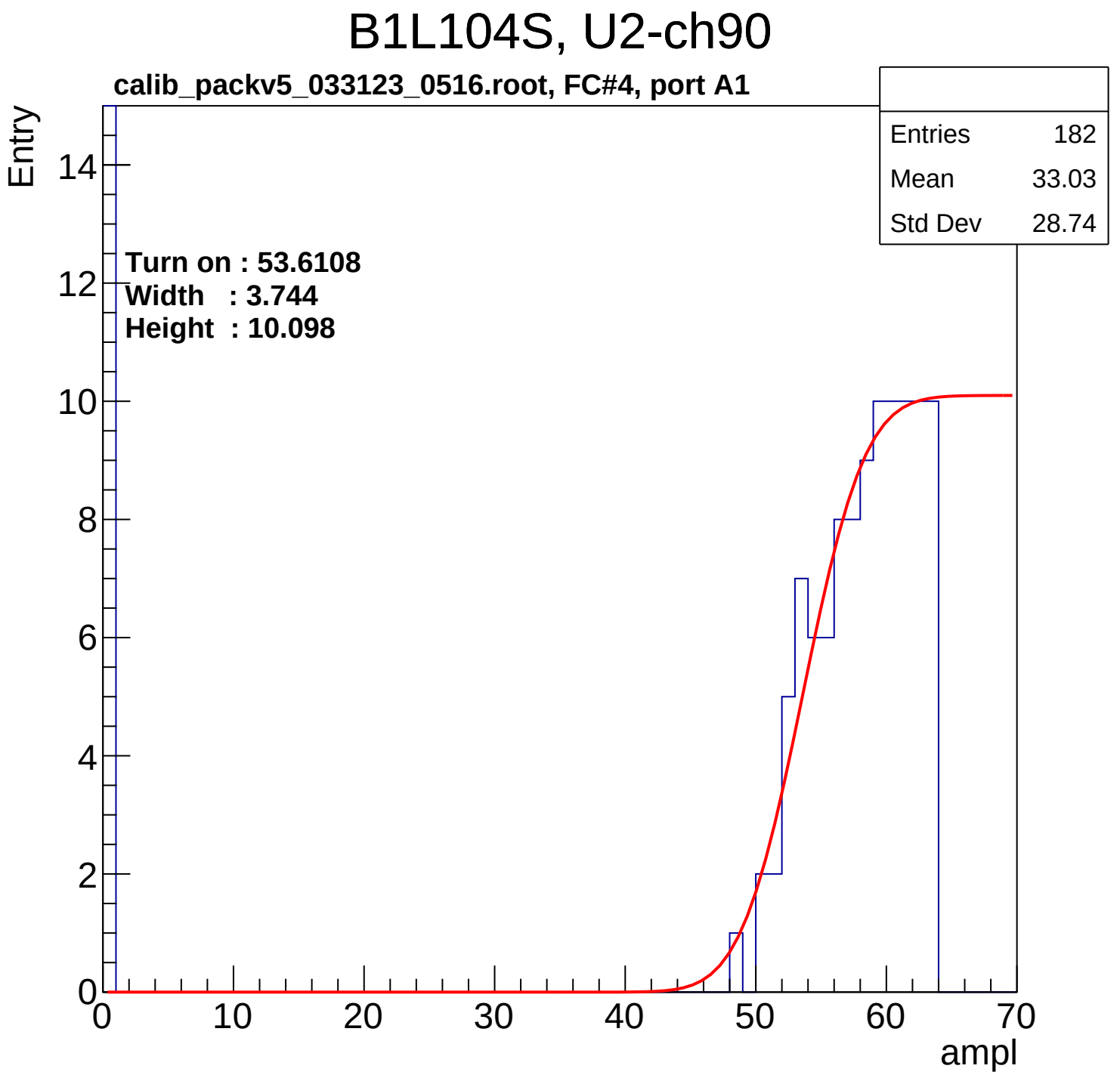
B1L104S, U2-ch90
calib_packv5_033123_0516.root, FC#4, port A1
Entries 182
Mean 33.03
Std Dev 28.74
Turn on : 53.6108
Width : 3.744
Height : 10.098
Entry
ampl
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2
4
6
8
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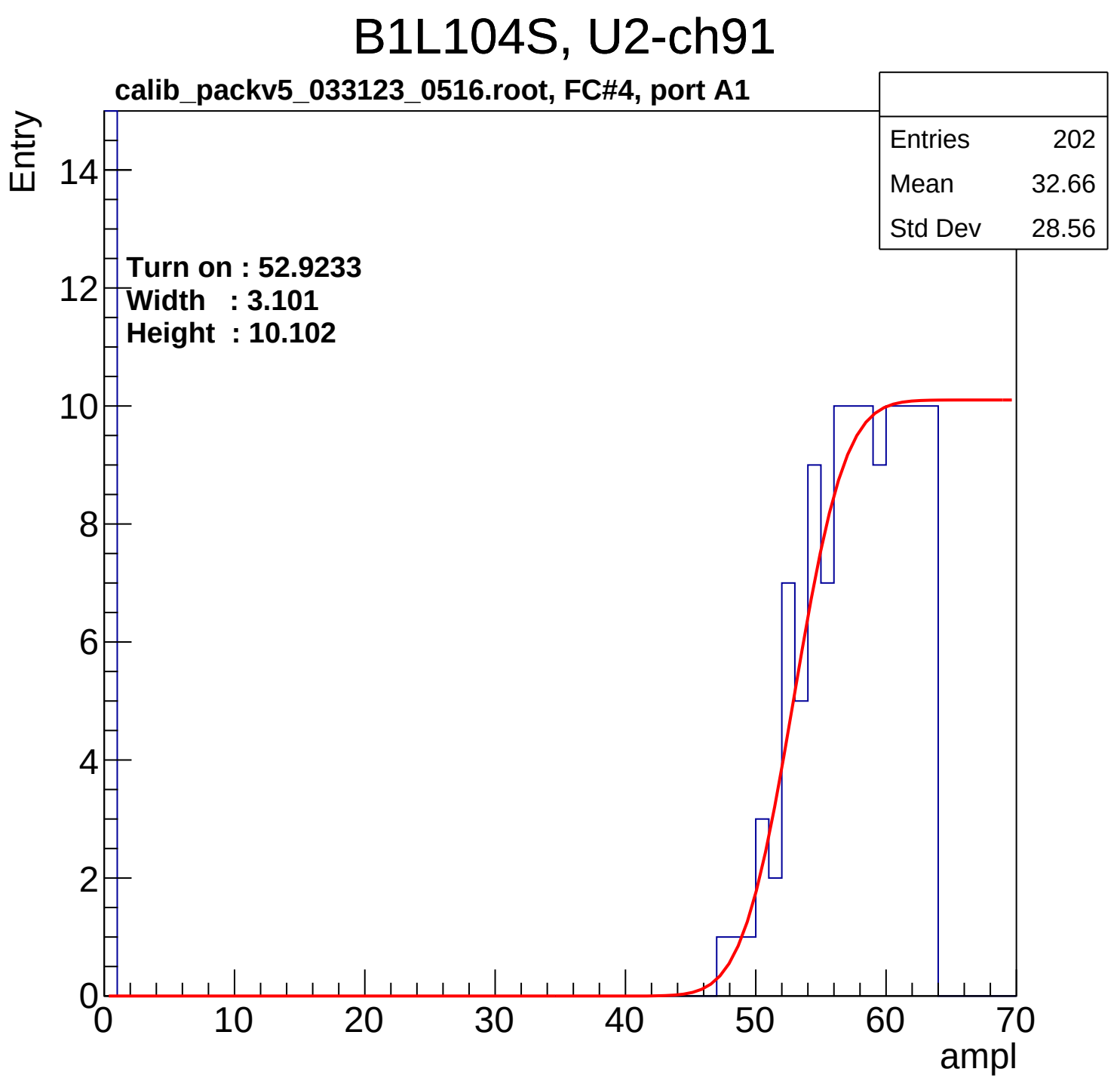
B1L104S, U2-ch91
calib_packv5_033123_0516.root, FC#4, port A1
Entries 202
Mean 32.66
Std Dev 28.56
Turn on : 52.9233
Width : 3.101
Height : 10.102
Entry
ampl
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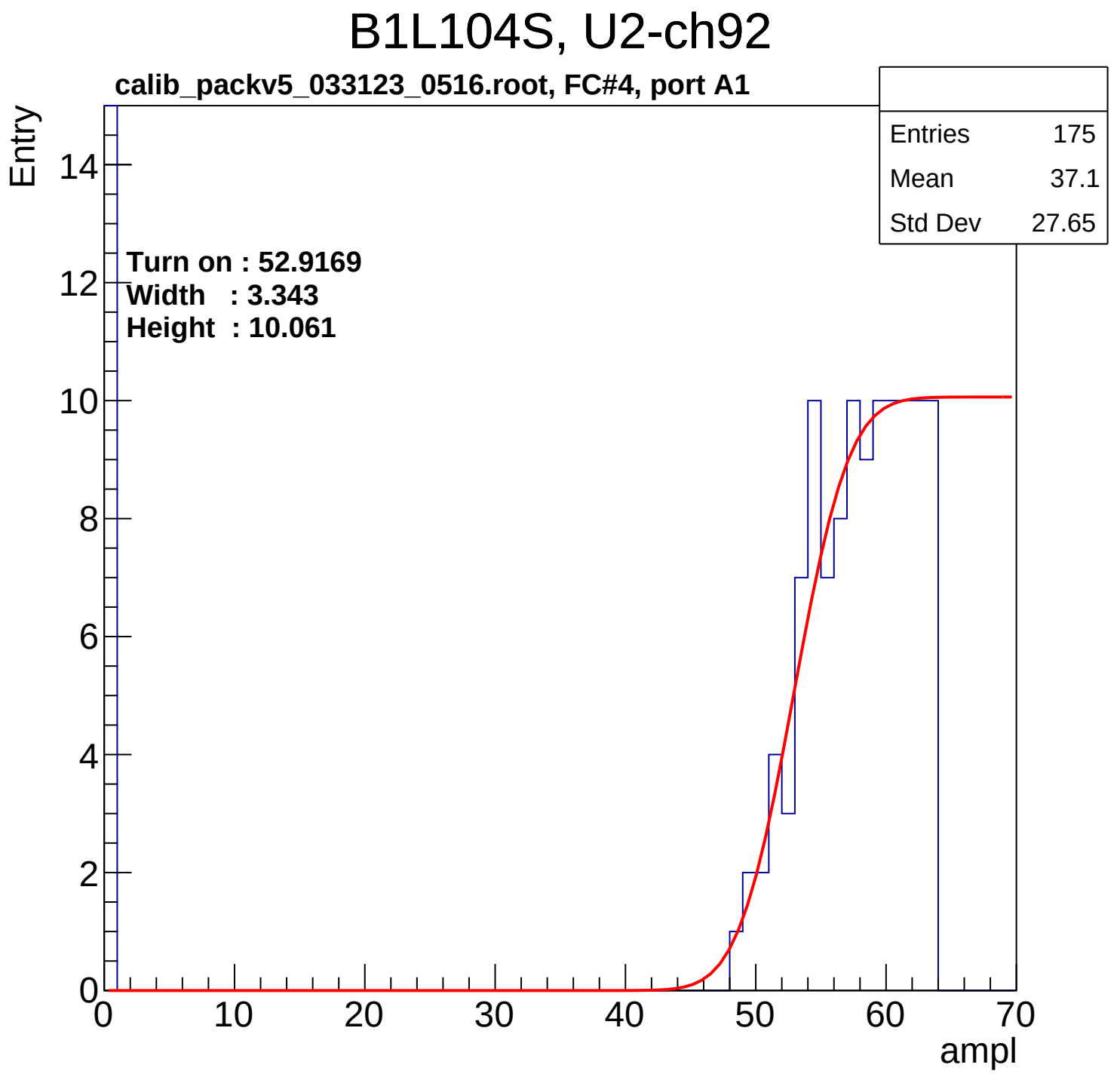
B1L104S, U2-ch92
calib_packv5_033123_0516.root, FC#4, port A1
Entries 175
Mean 37.1
Std Dev 27.65
Turn on : 52.9169
Width : 3.343
Height : 10.061
Entry
ampl
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2
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6
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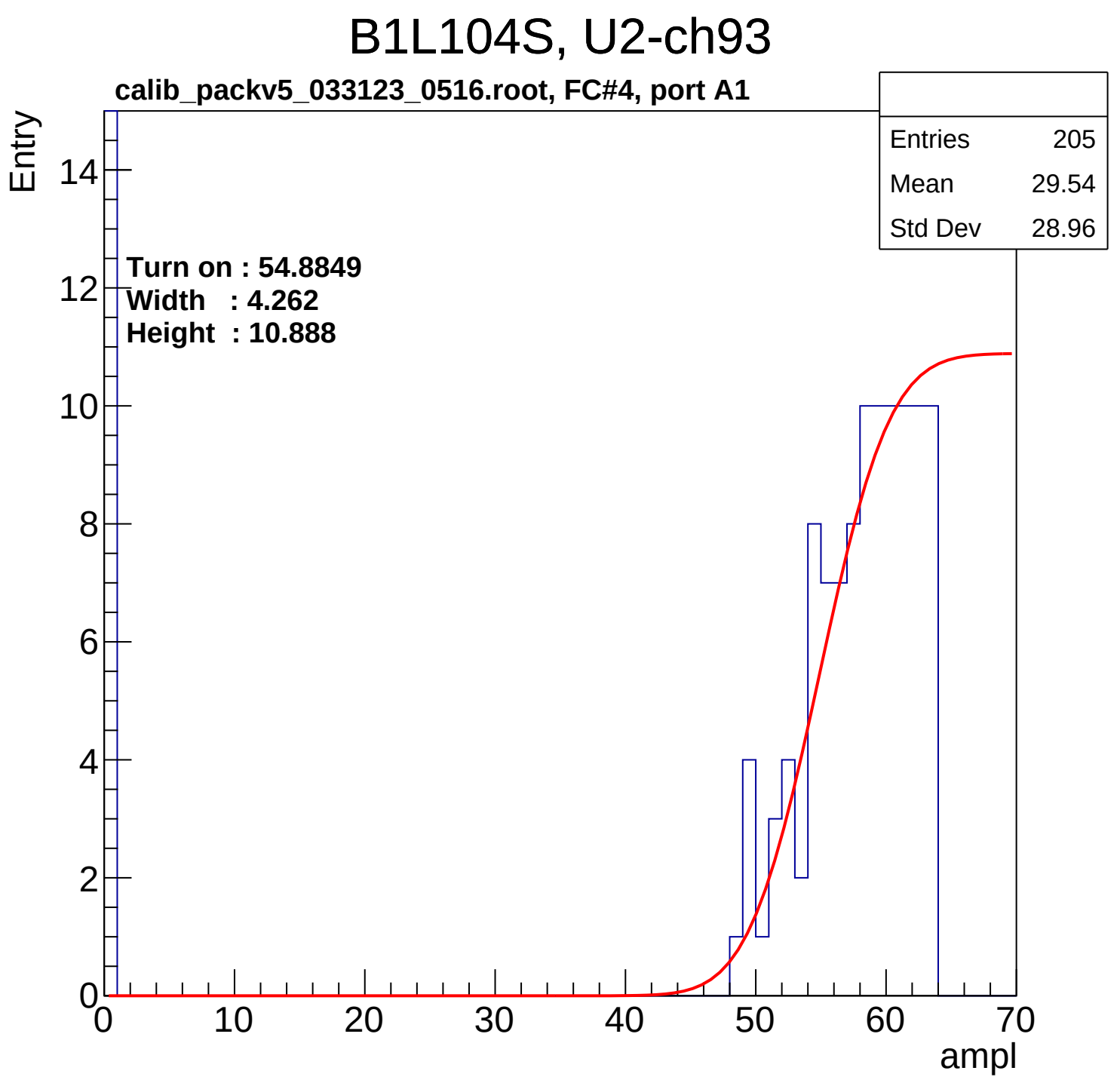
B1L104S, U2-ch93
calib_packv5_033123_0516.root, FC#4, port A1
Entries 205
Mean 29.54
Std Dev 28.96
Turn on : 54.8849
Width : 4.262
Height : 10.888
Entry
ampl
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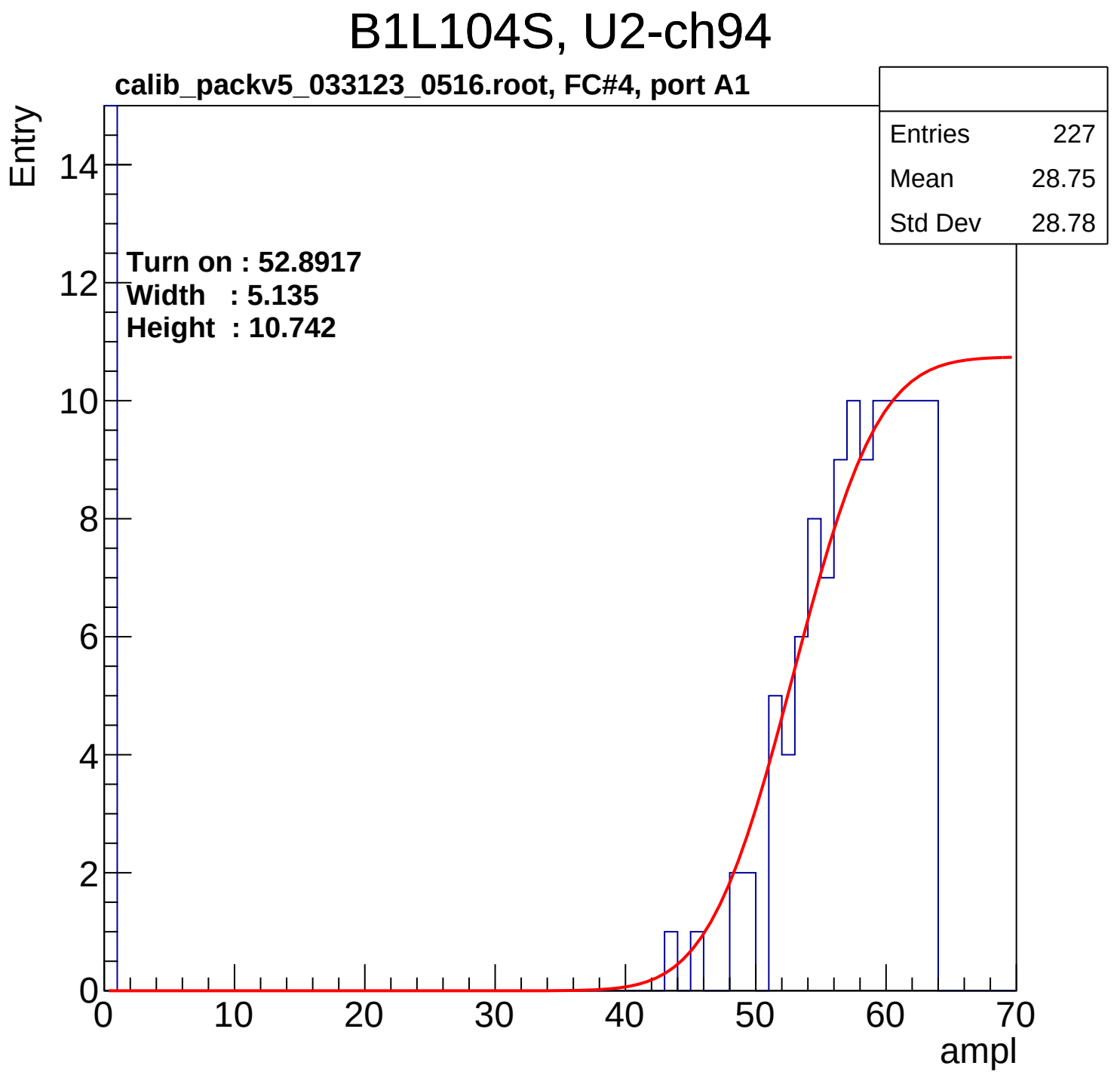
B1L104S, U2-ch94
calib_packv5_033123_0516.root, FC#4, port A1
Entries 227
Mean 28.75
Std Dev 28.78
Turn on : 52.8917
Width : 5.135
Height : 10.742
Entry
ampl
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6
8
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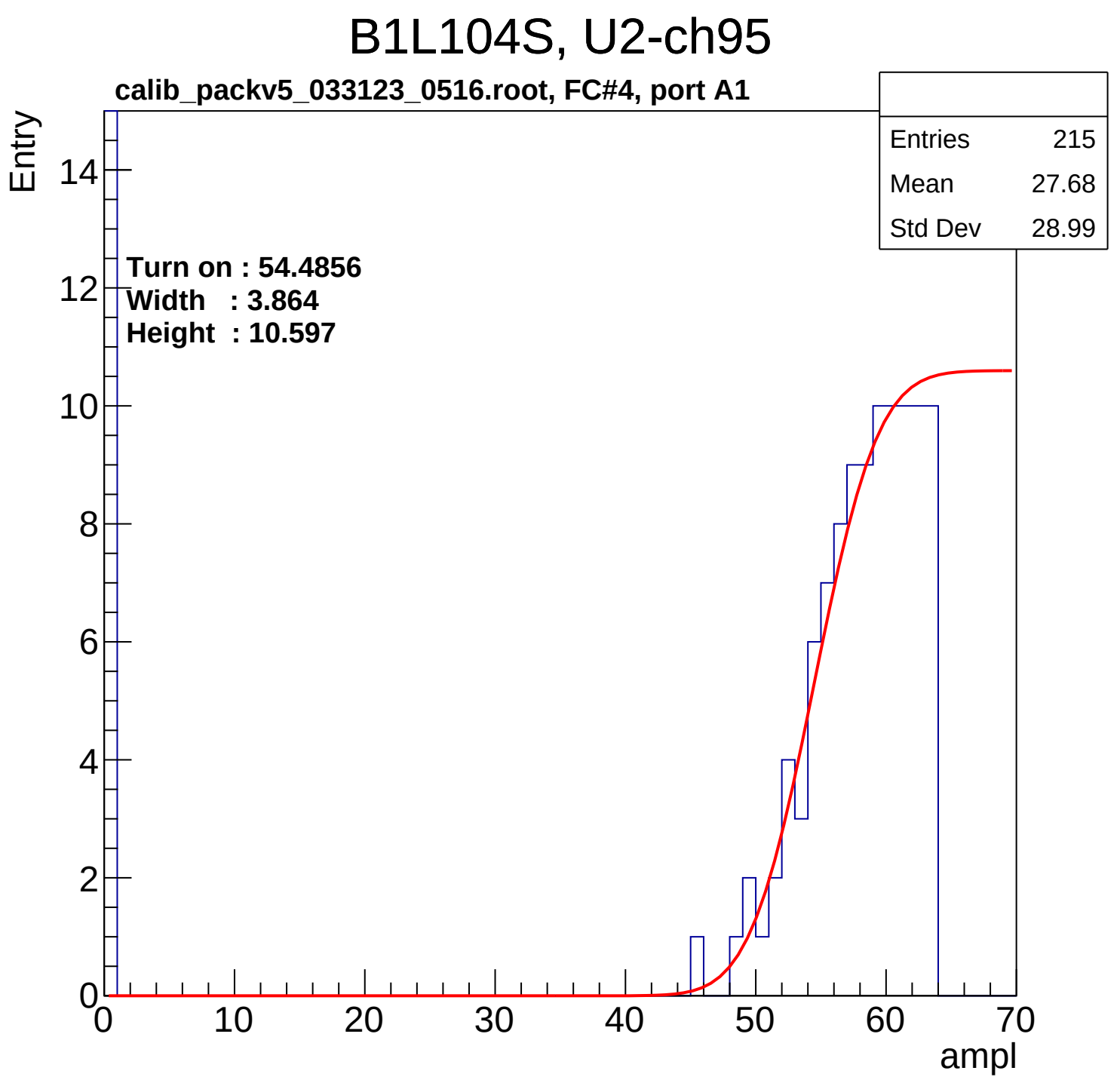
B1L104S, U2-ch95
calib_packv5_033123_0516.root, FC#4, port A1
Entries 215
Mean 27.68
Std Dev 28.99
Turn on : 54.4856
Width : 3.864
Height : 10.597
Entry
ampl
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6
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12
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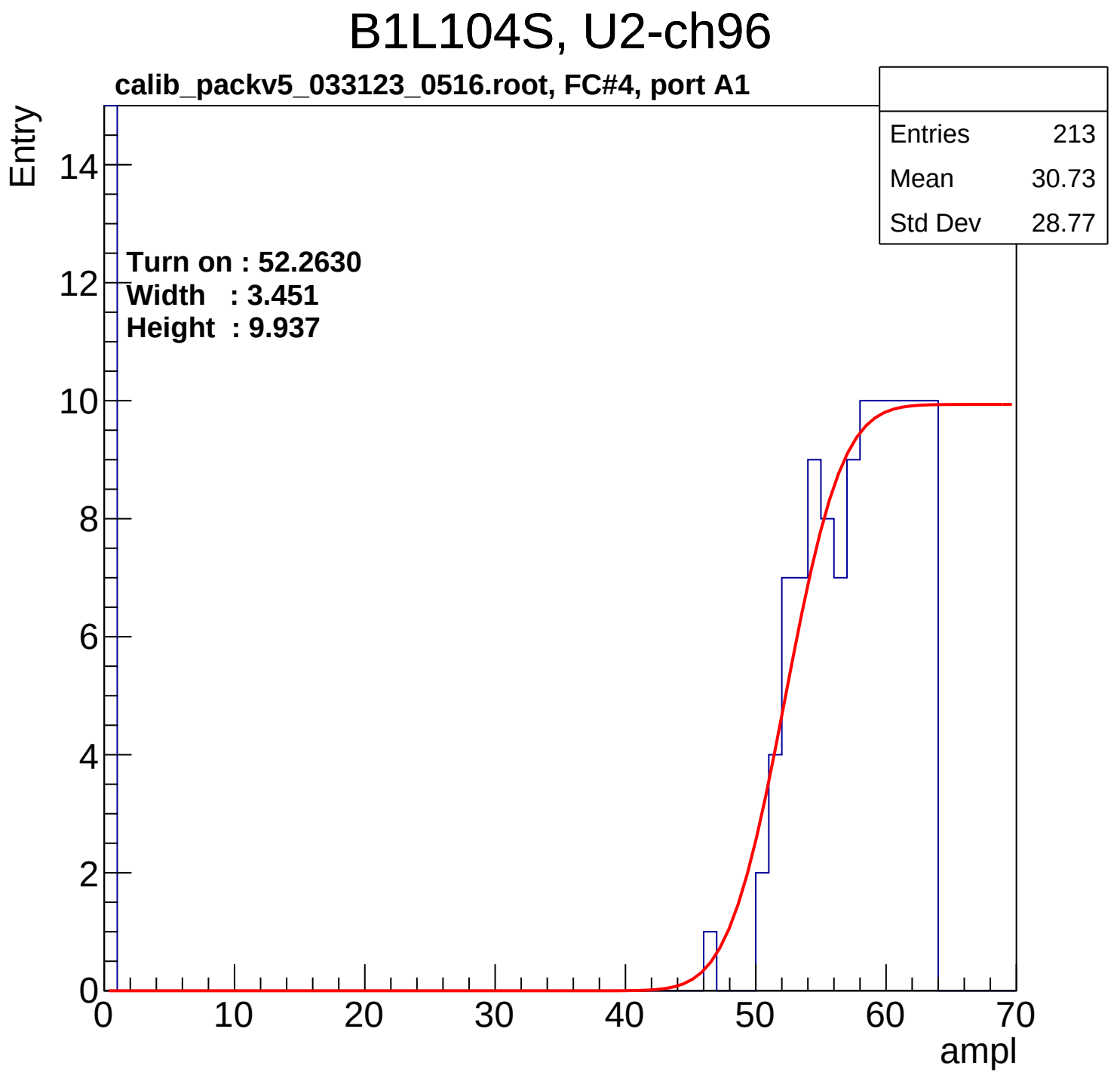
B1L104S, U2-ch96
calib_packv5_033123_0516.root, FC#4, port A1
Entries 213
Mean 30.73
Std Dev 28.77
Turn on : 52.2630
Width : 3.451
Height : 9.937
Entry
ampl
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6
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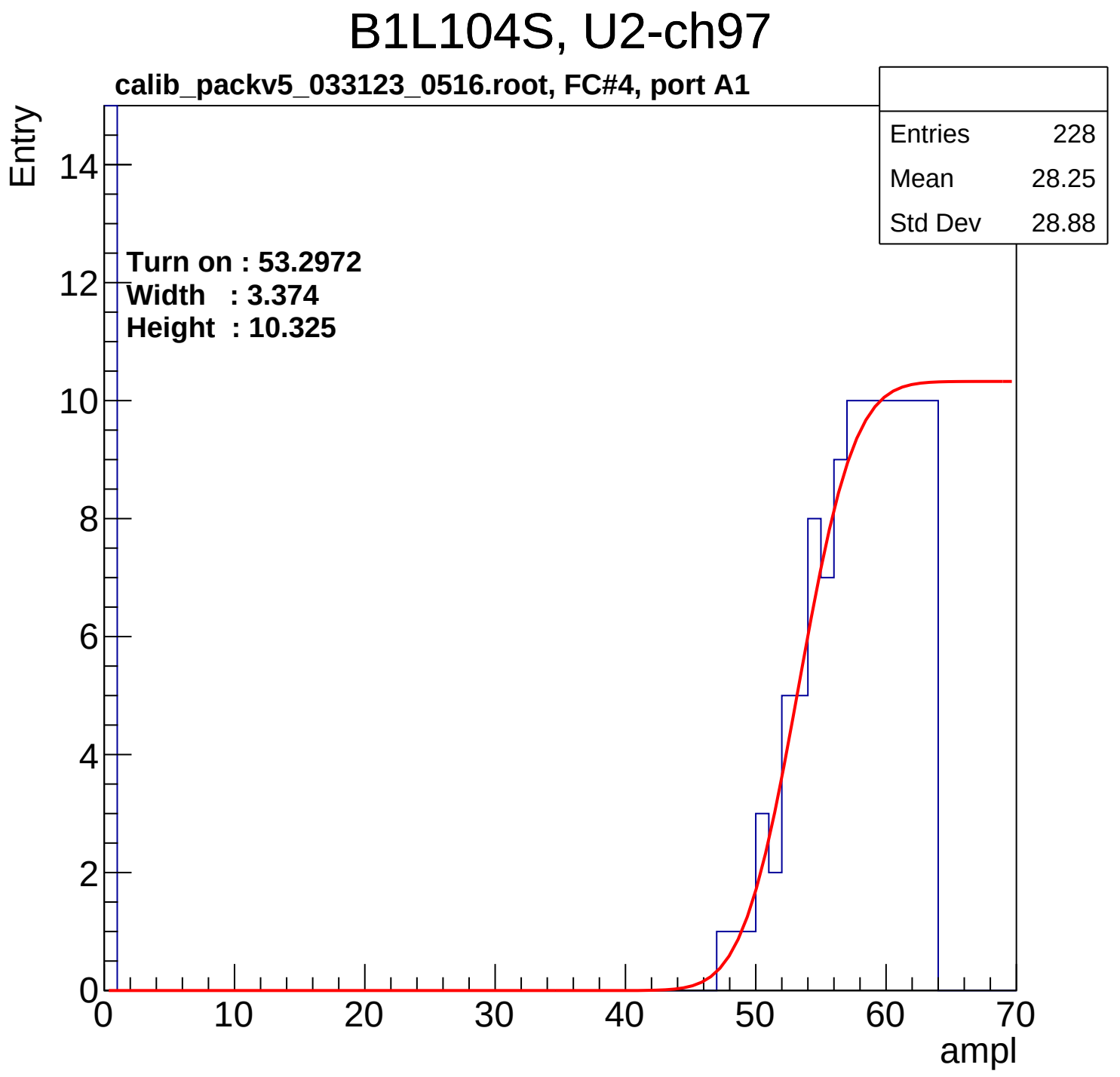
B1L104S, U2-ch97
calib_packv5_033123_0516.root, FC#4, port A1
Entries 228
Mean 28.25
Std Dev 28.88
Turn on : 53.2972
Width : 3.374
Height : 10.325
Entry
ampl
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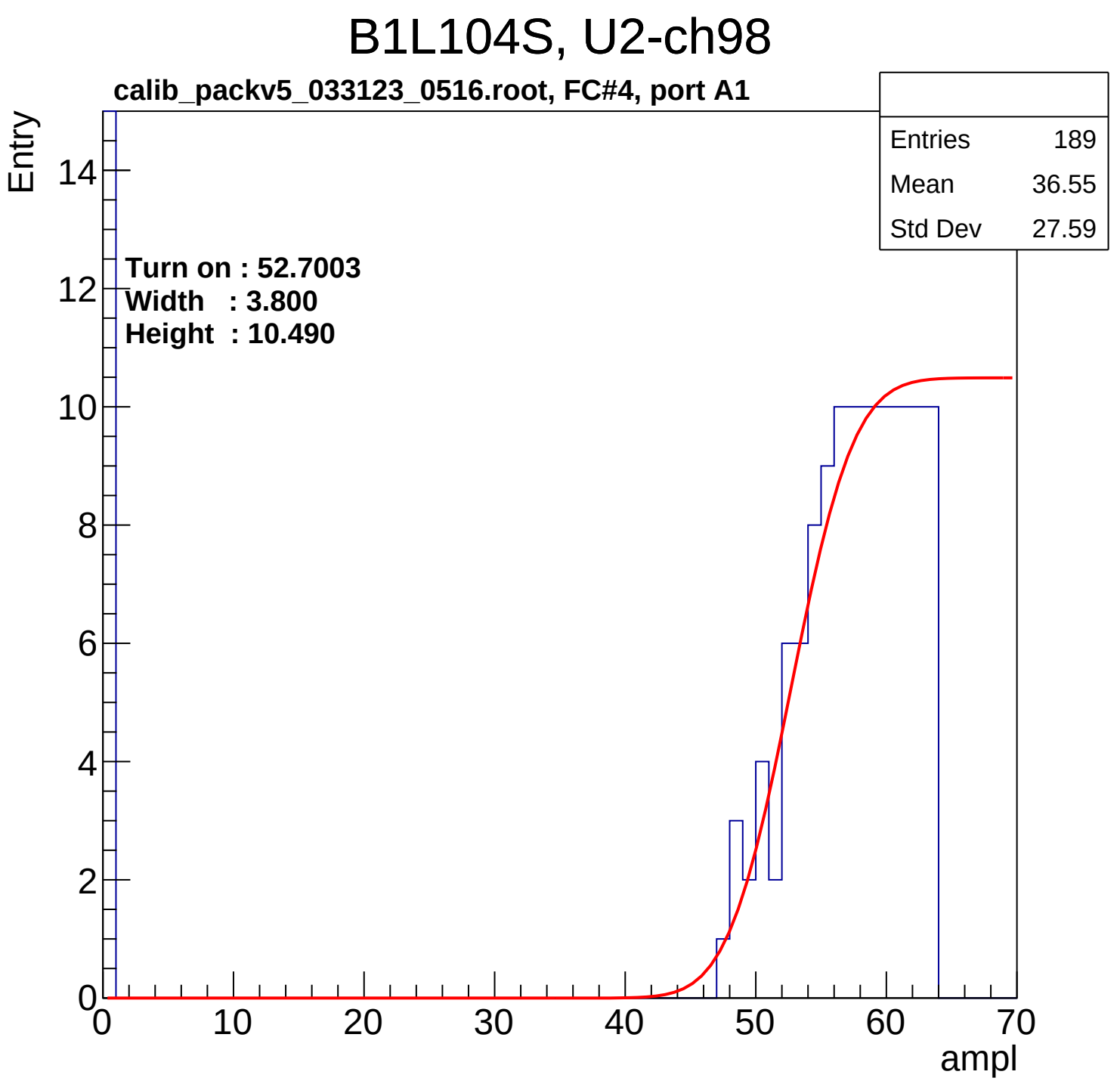
B1L104S, U2-ch98
calib_packv5_033123_0516.root, FC#4, port A1
Entries 189
Mean 36.55
Std Dev 27.59
Turn on : 52.7003
Width : 3.800
Height : 10.490
Entry
ampl
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8
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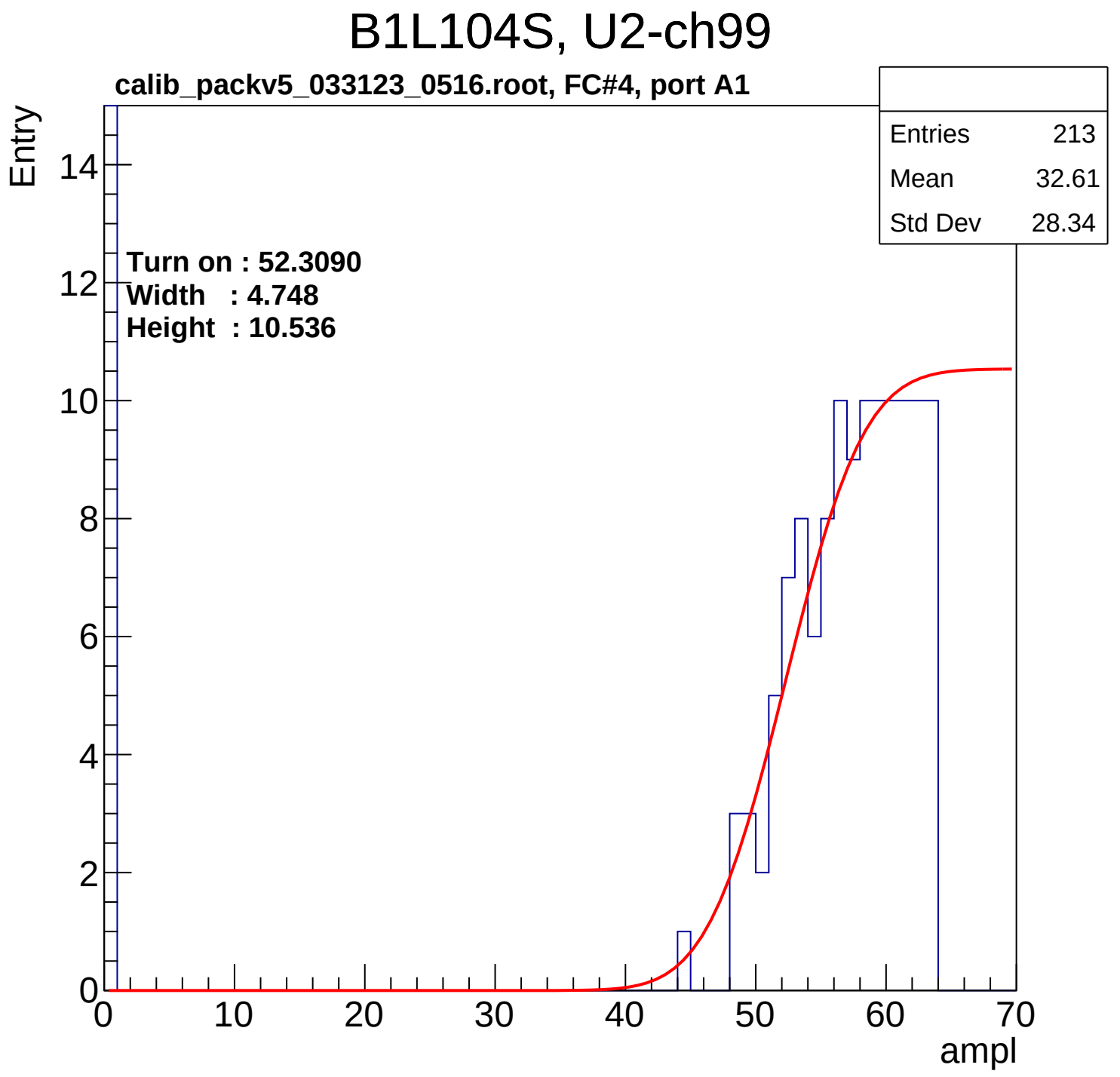
B1L104S, U2-ch99
calib_packv5_033123_0516.root, FC#4, port A1
Entries 213
Mean 32.61
Std Dev 28.34
Turn on : 52.3090
Width : 4.748
Height : 10.536
Entry
ampl
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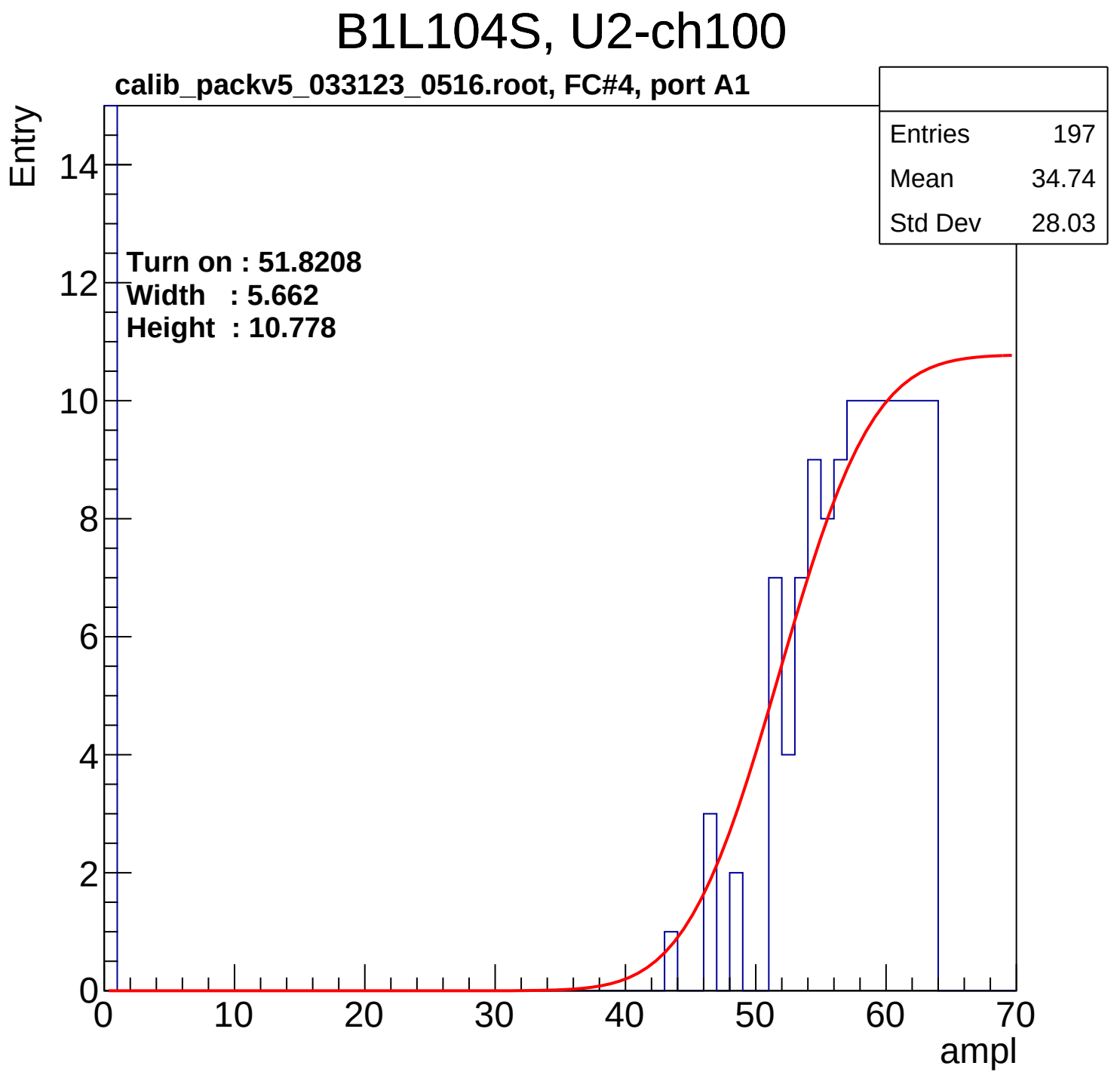
B1L104S, U2-ch100
calib_packv5_033123_0516.root, FC#4, port A1
Entries 197
Mean 34.74
Std Dev 28.03
Turn on : 51.8208
Width : 5.662
Height : 10.778
Entry
ampl
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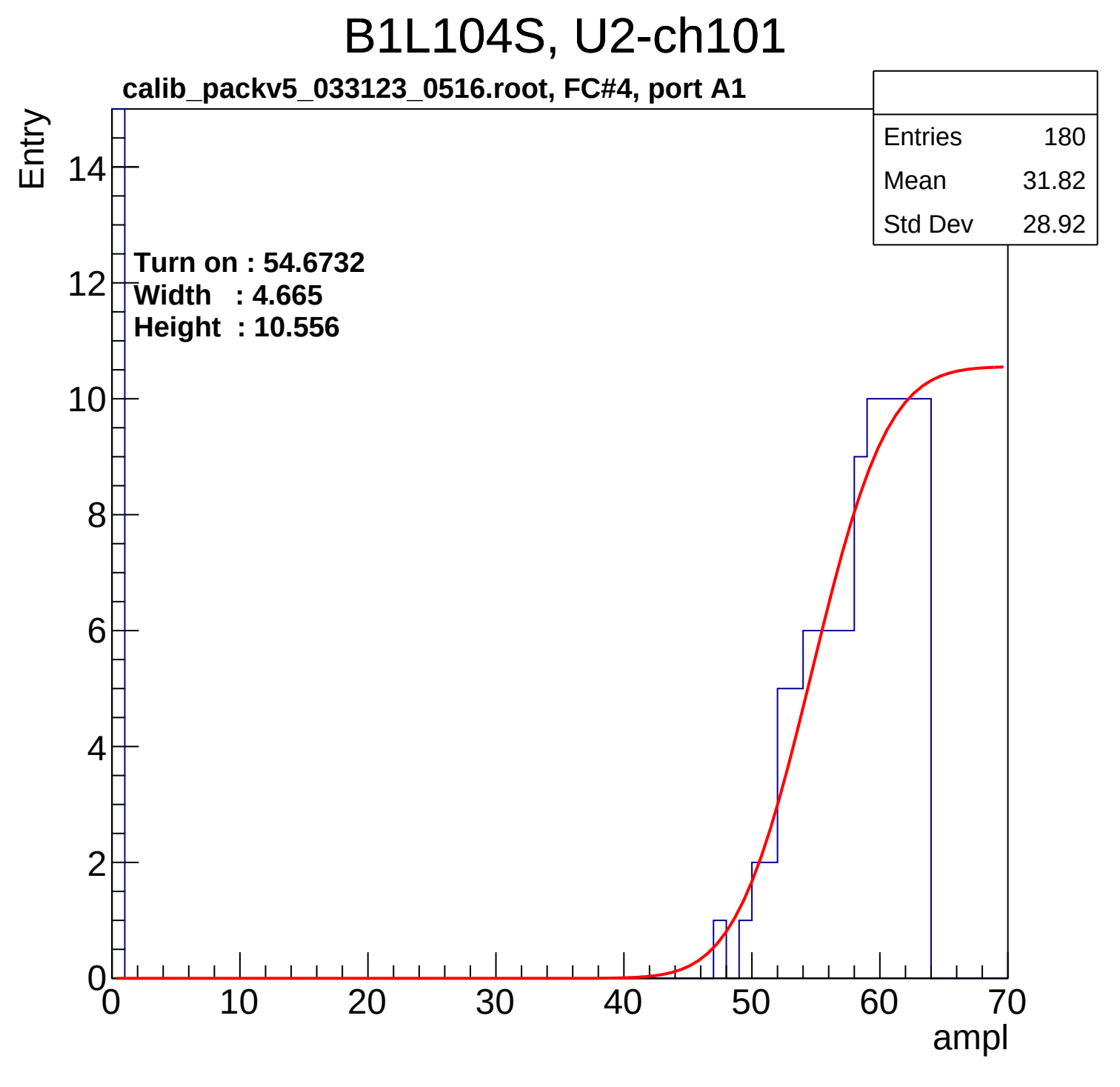
B1L104S, U2-ch101
calib_packv5_033123_0516.root, FC#4, port A1
Entries 180
Mean 31.82
Std Dev 28.92
Turn on : 54.6732
Width : 4.665
Height : 10.556
Entry
ampl
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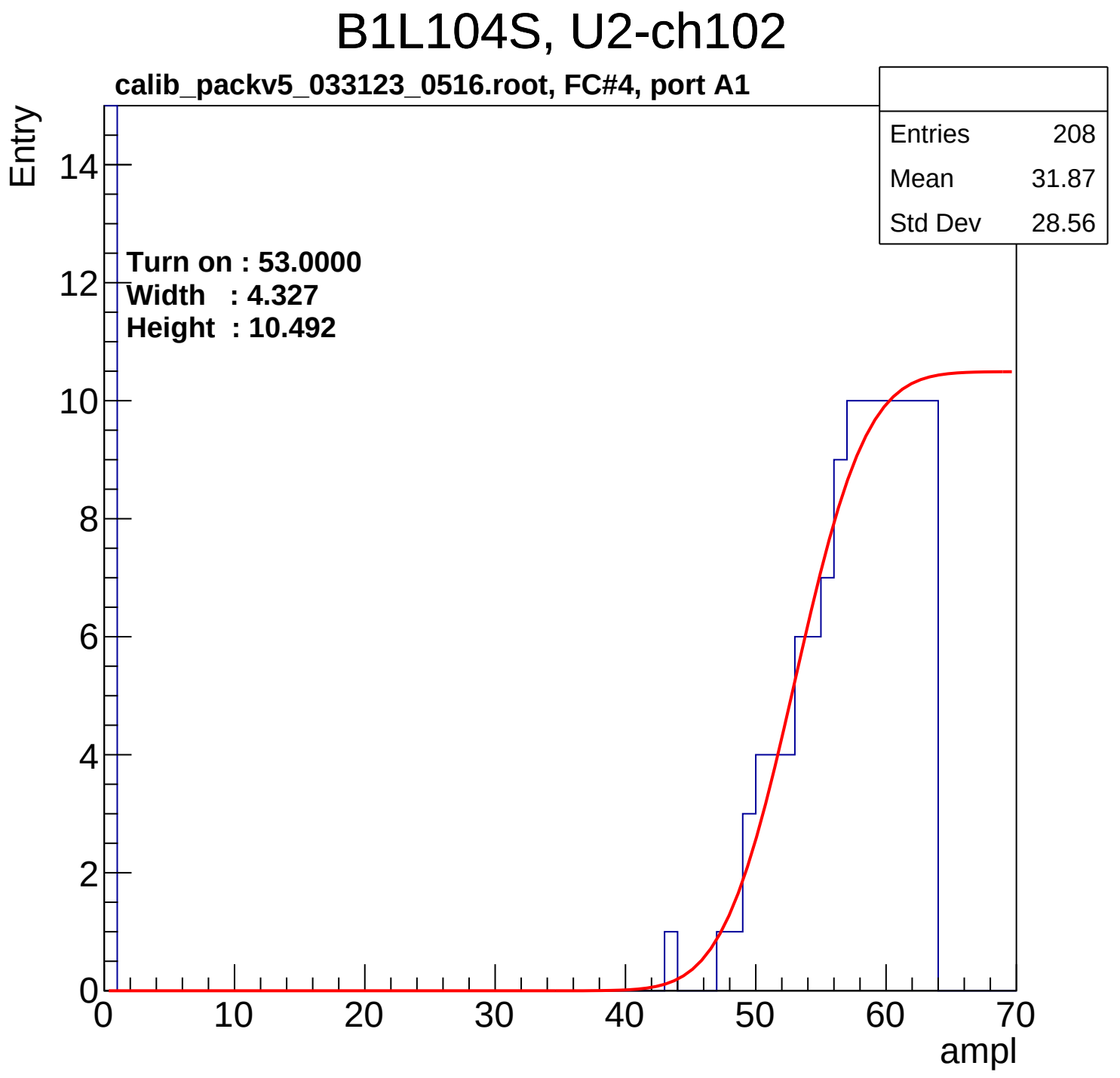
B1L104S, U2-ch102
calib_packv5_033123_0516.root, FC#4, port A1
Entries 208
Mean 31.87
Std Dev 28.56
Turn on : 53.0000
Width : 4.327
Height : 10.492
Entry
ampl
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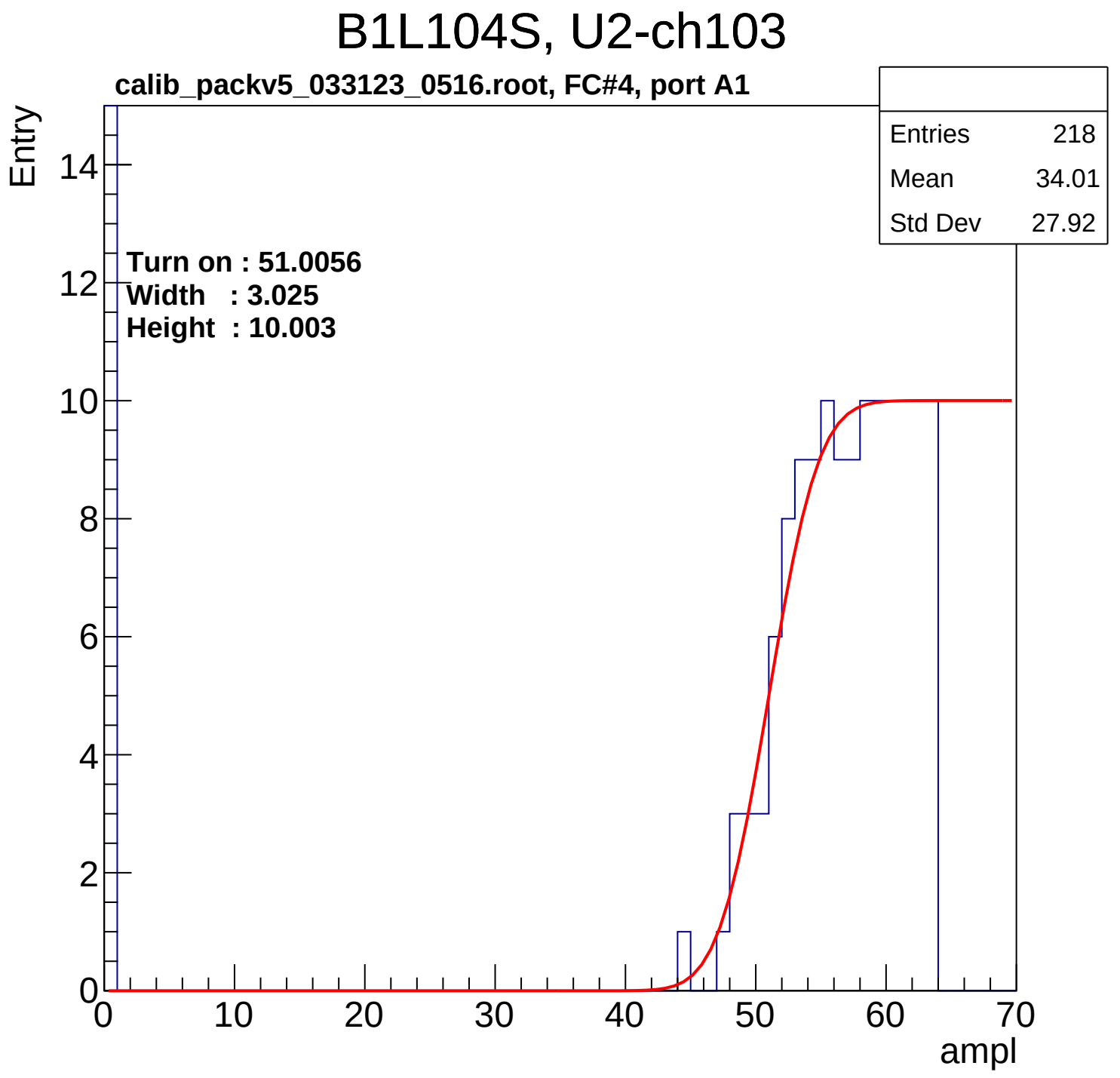
B1L104S, U2-ch103
calib_packv5_033123_0516.root, FC#4, port A1
Entries 218
Mean 34.01
Std Dev 27.92
Turn on : 51.0056
Width : 3.025
Height : 10.003
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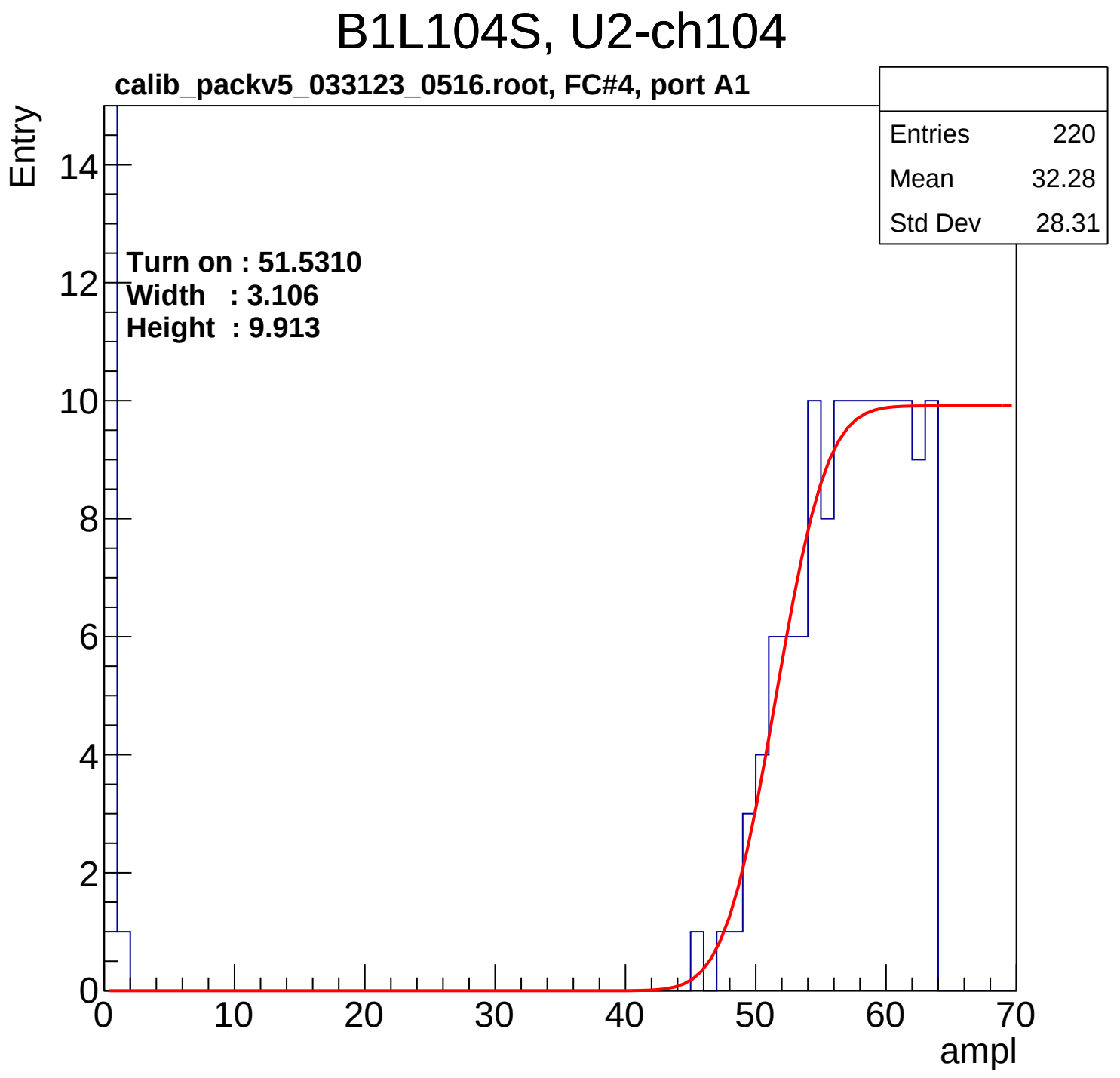
B1L104S, U2-ch104
calib_packv5_033123_0516.root, FC#4, port A1
Entries 220
Mean 32.28
Std Dev 28.31
Turn on : 51.5310
Width : 3.106
Height : 9.913
Entry
ampl
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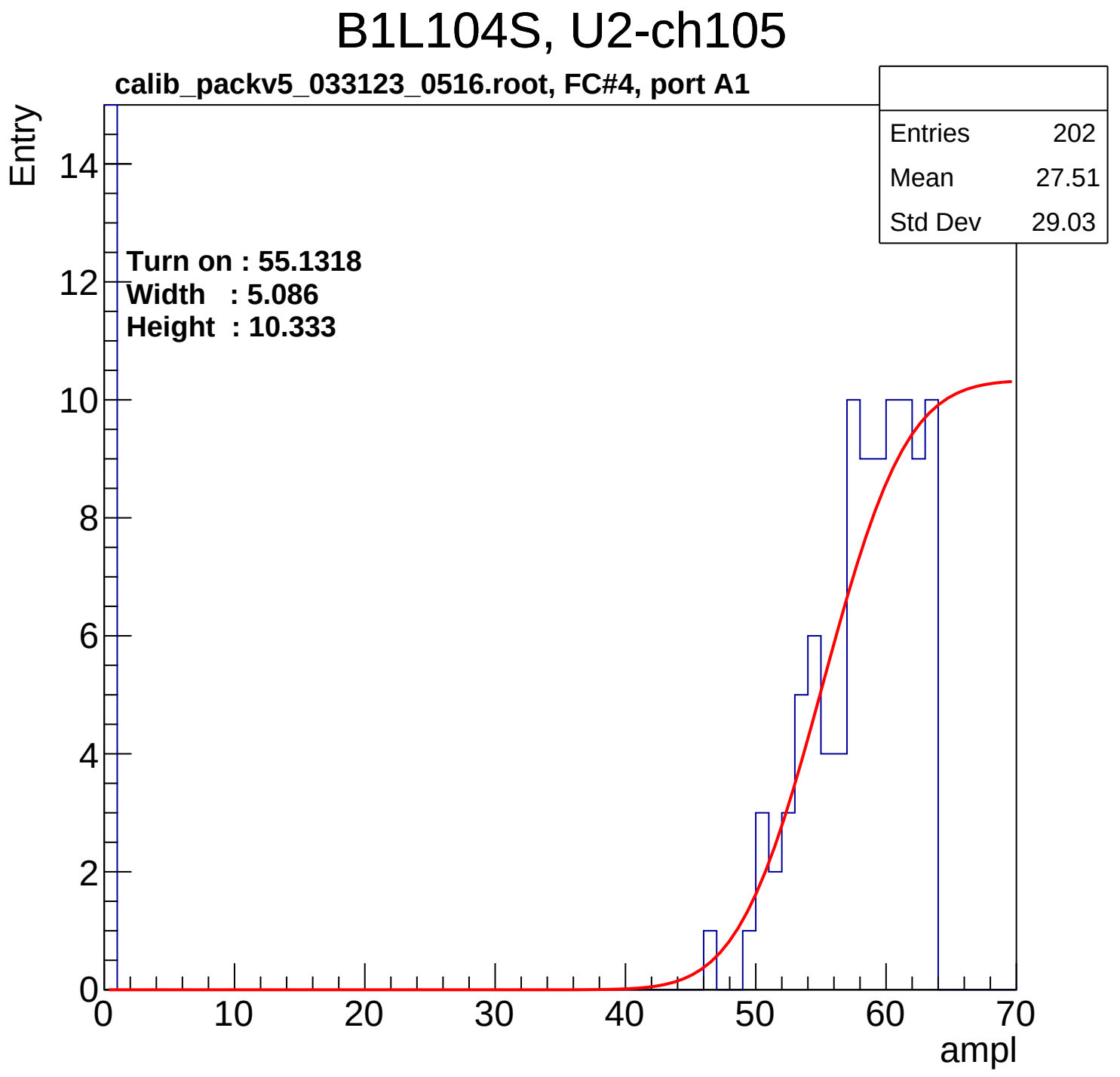
B1L104S, U2-ch105
calib_packv5_033123_0516.root, FC#4, port A1
Entries 202
Mean 27.51
Std Dev 29.03
Turn on : 55.1318
Width : 5.086
Height : 10.333
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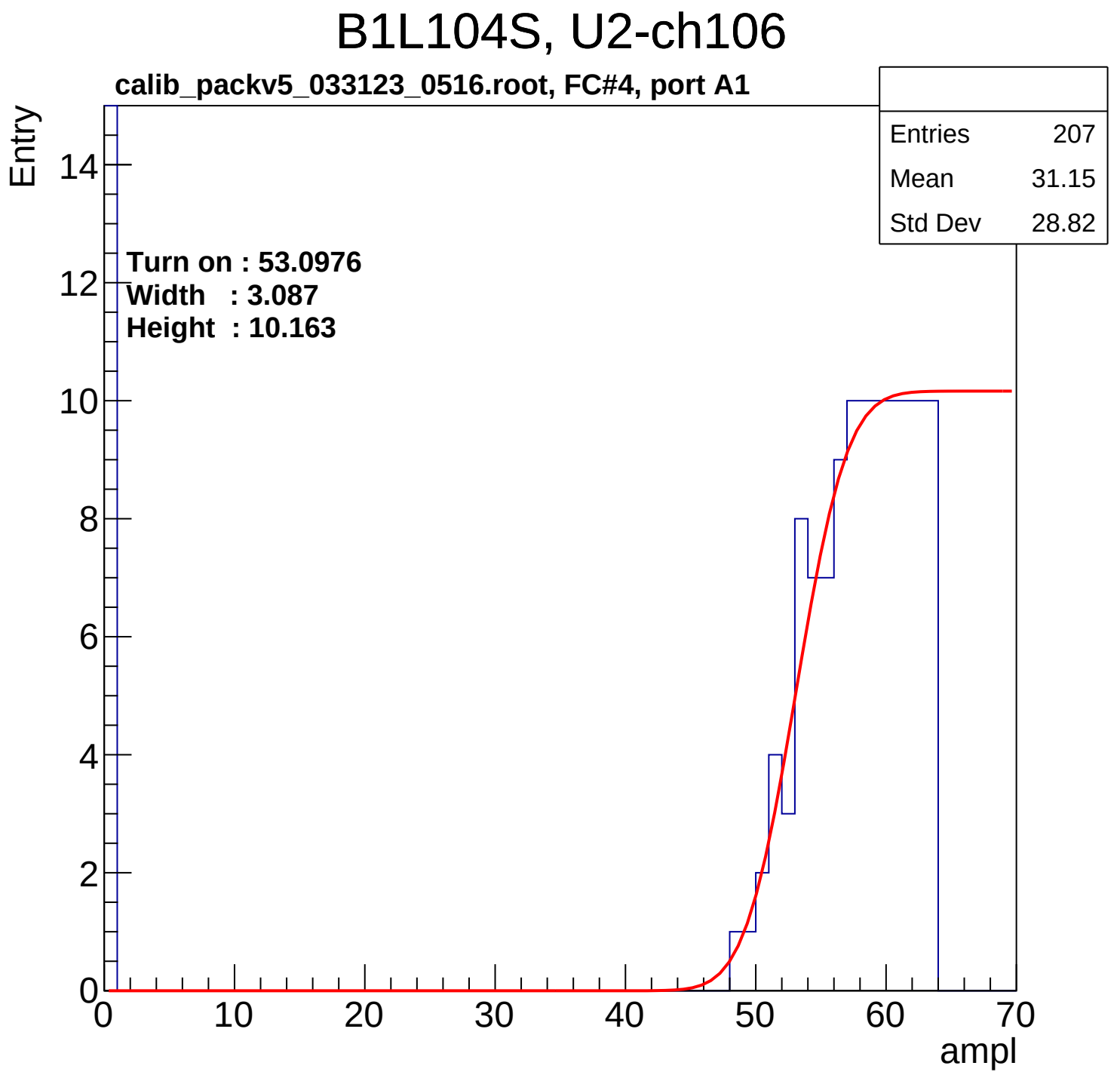
B1L104S, U2-ch106
calib_packv5_033123_0516.root, FC#4, port A1
Entries 207
Mean 31.15
Std Dev 28.82
Turn on : 53.0976
Width : 3.087
Height : 10.163
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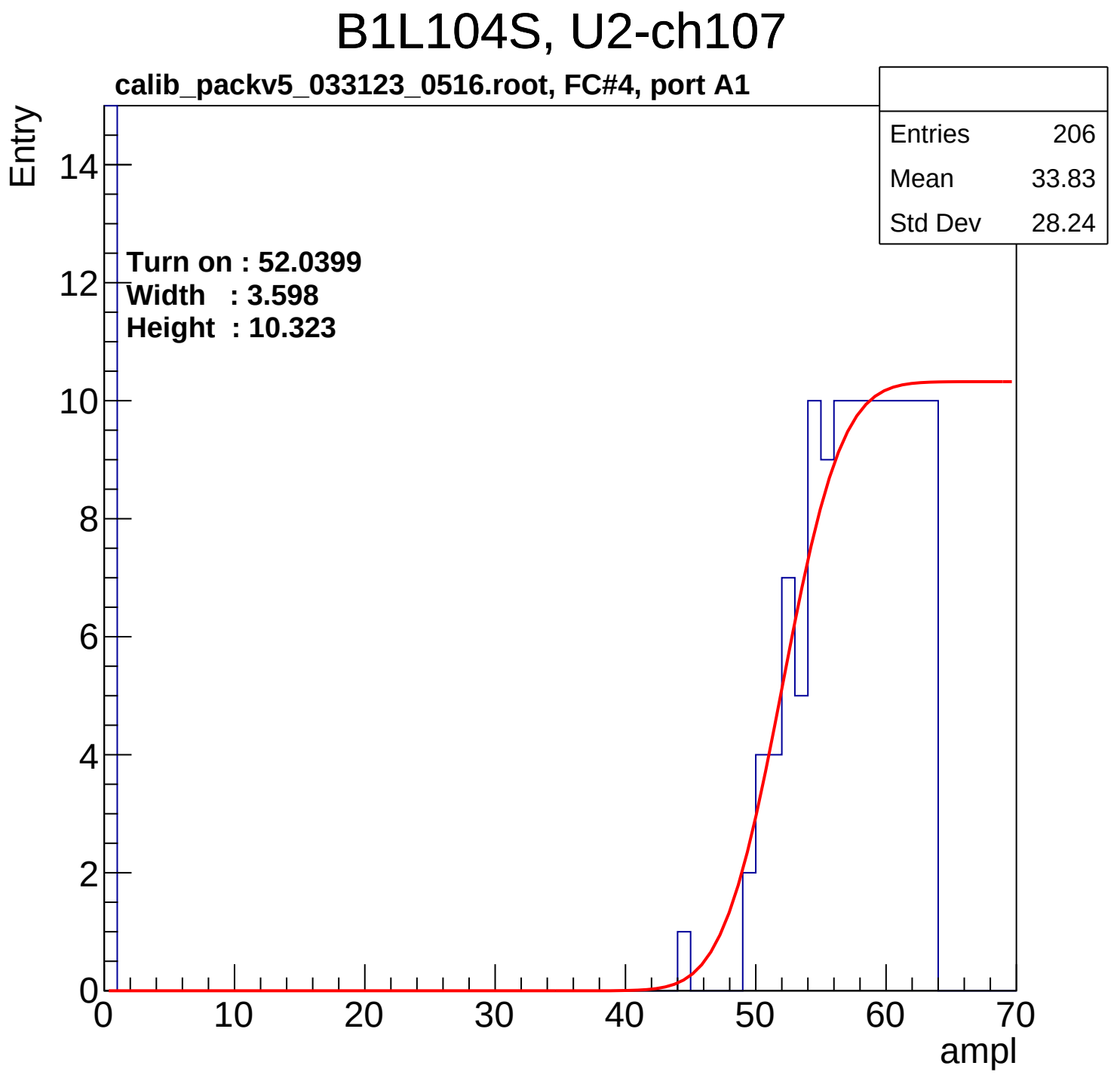
B1L104S, U2-ch107
calib_packv5_033123_0516.root, FC#4, port A1
Entries 206
Mean 33.83
Std Dev 28.24
Turn on : 52.0399
Width : 3.598
Height : 10.323
Entry
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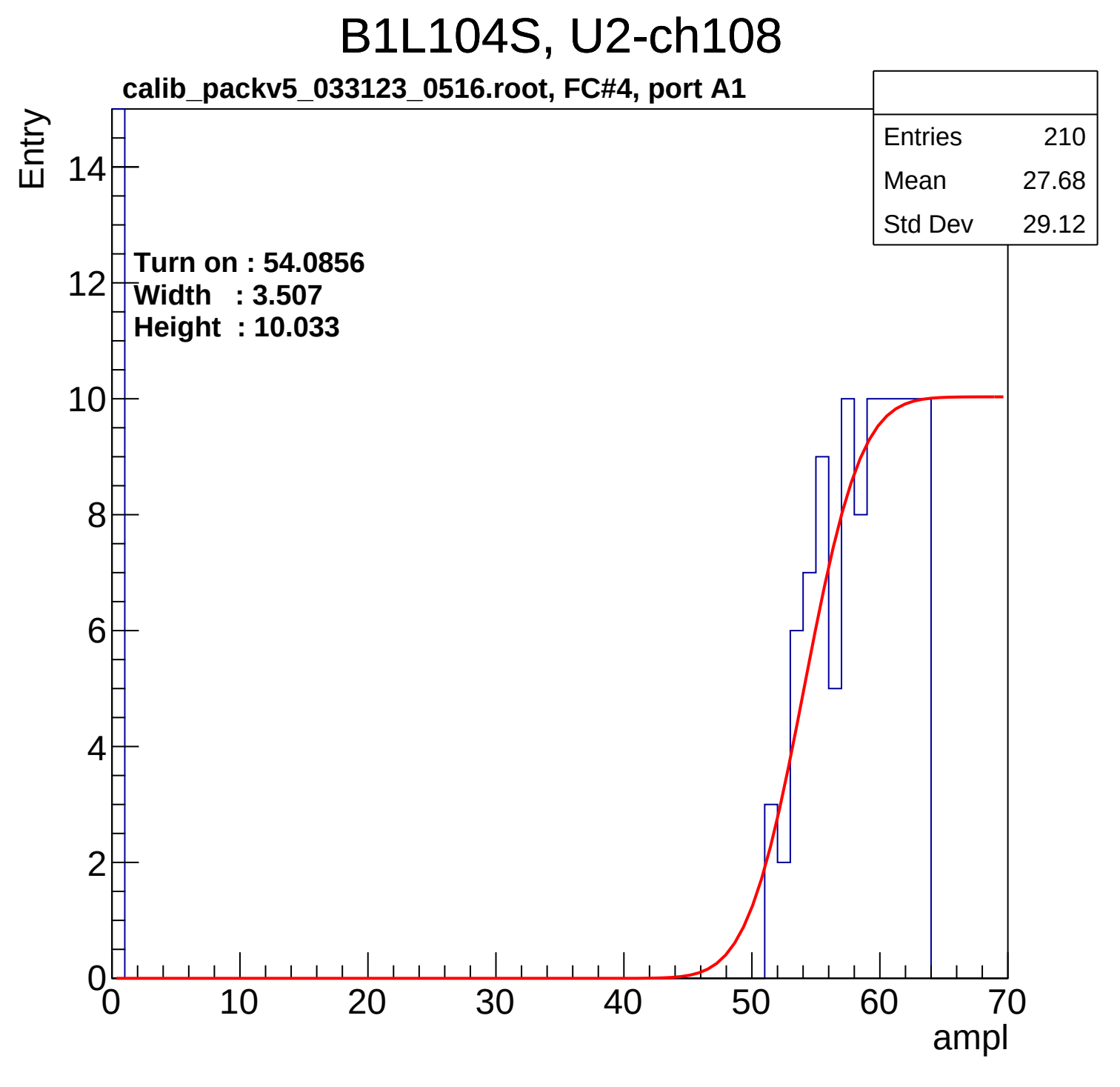
B1L104S, U2-ch108
calib_packv5_033123_0516.root, FC#4, port A1
Entries 210
Mean 27.68
Std Dev 29.12
Turn on : 54.0856
Width : 3.507
Height : 10.033
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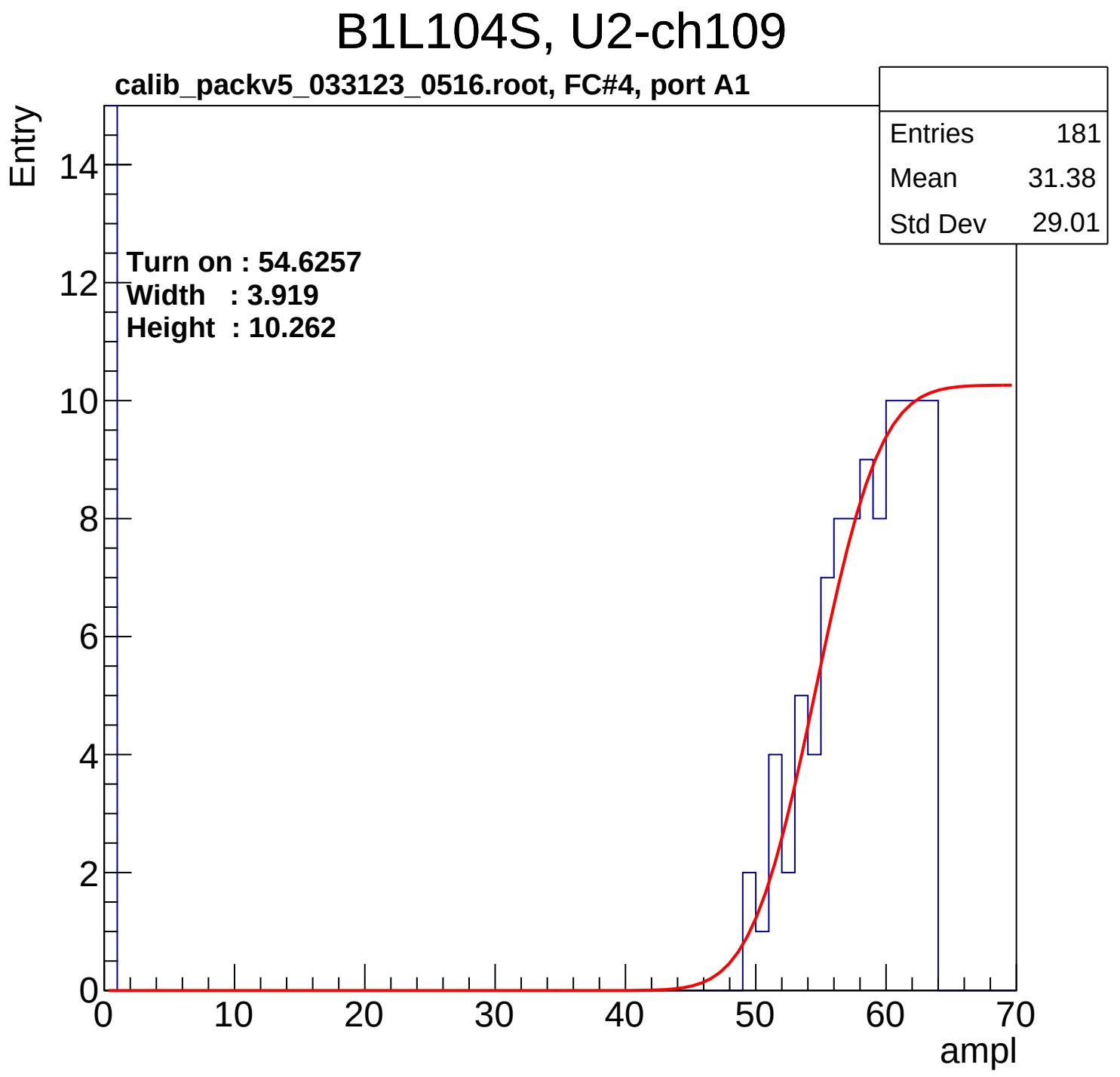
B1L104S, U2-ch109
calib_packv5_033123_0516.root, FC#4, port A1
Entries 181
Mean 31.38
Std Dev 29.01
Turn on : 54.6257
Width : 3.919
Height : 10.262
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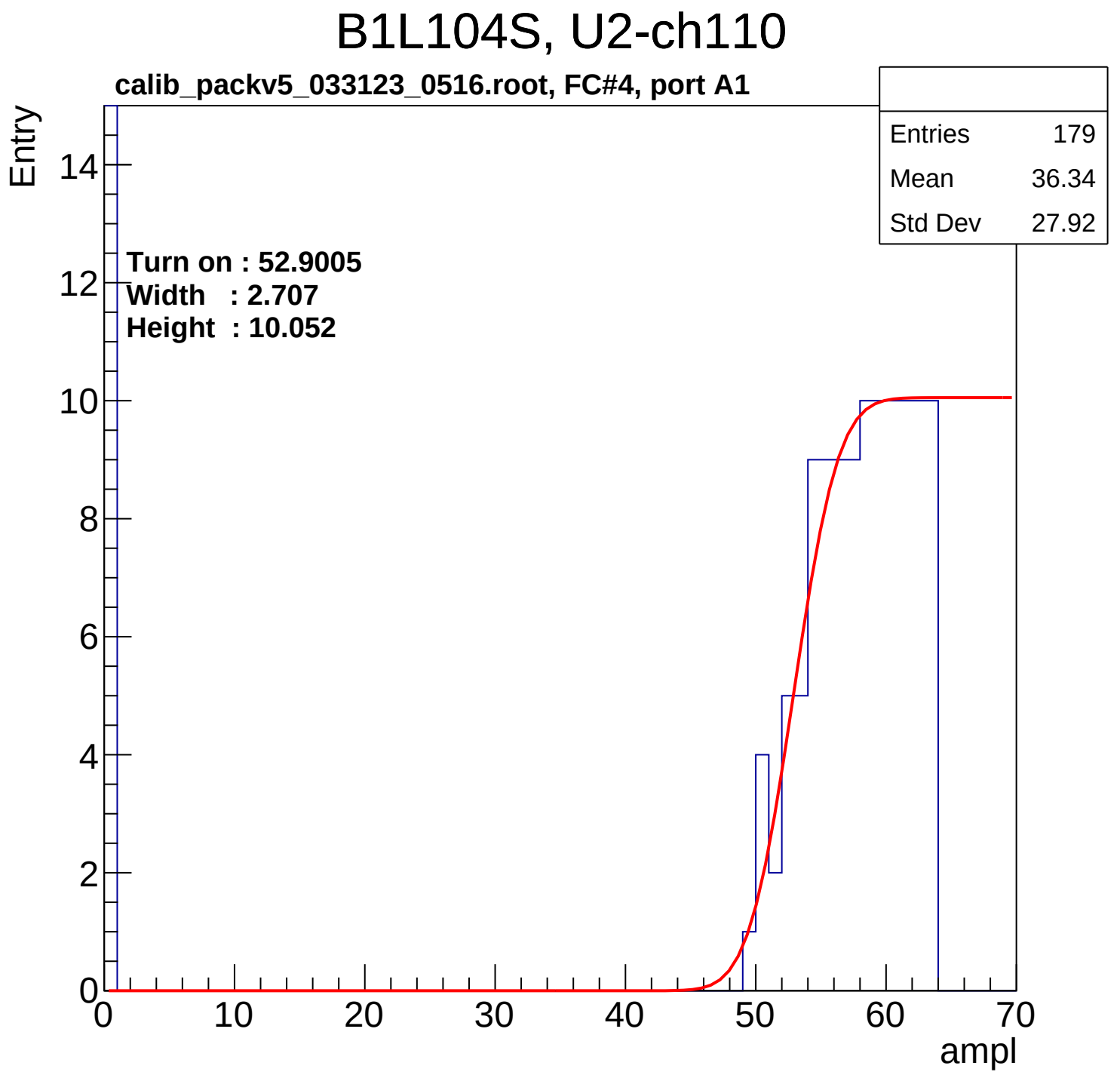
B1L104S, U2-ch110
calib_packv5_033123_0516.root, FC#4, port A1
Entries 179
Mean 36.34
Std Dev 27.92
Turn on : 52.9005
Width : 2.707
Height : 10.052
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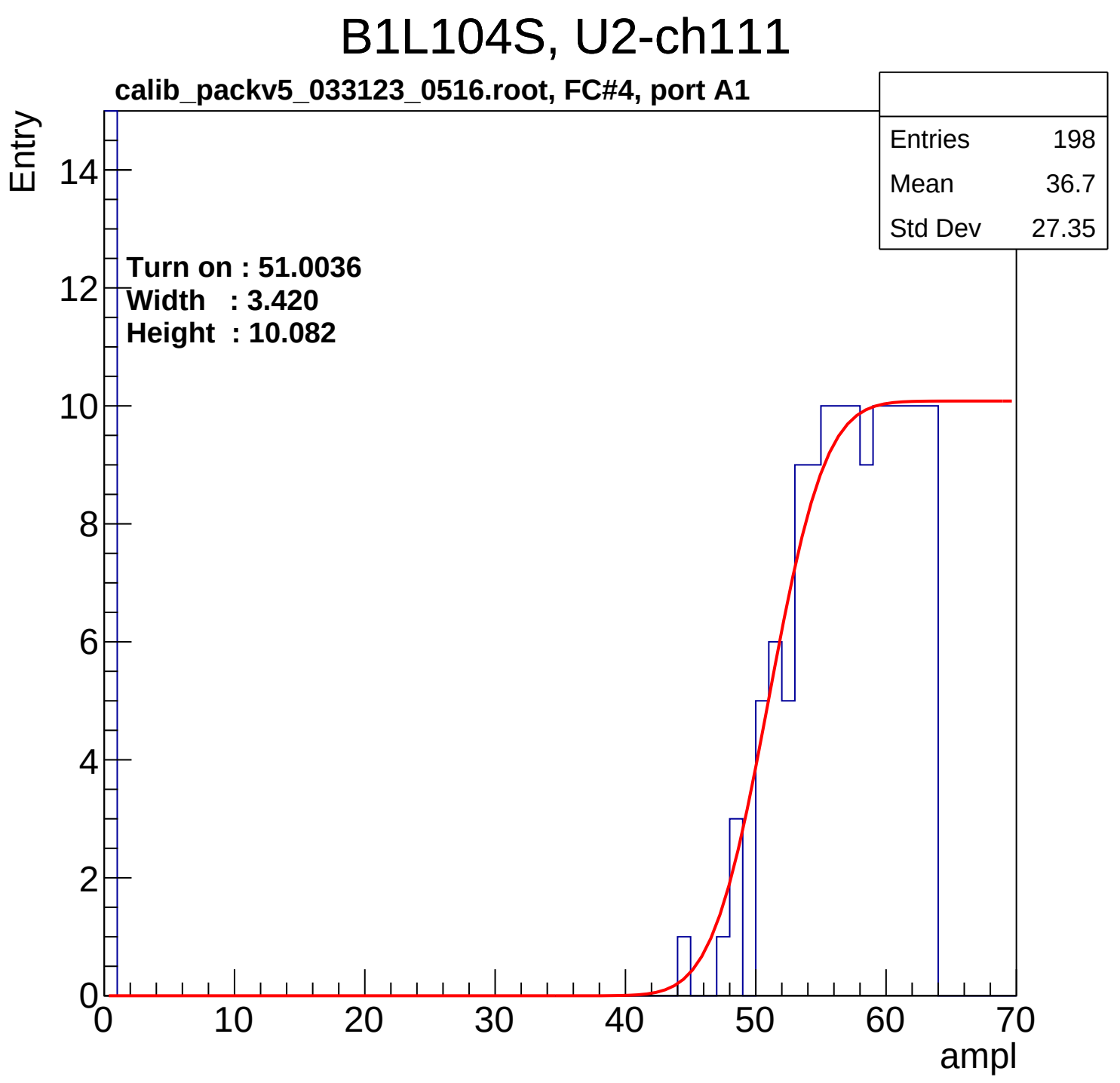
B1L104S, U2-ch111
calib_packv5_033123_0516.root, FC#4, port A1
Entries 198
Mean 36.7
Std Dev 27.35
Turn on : 51.0036
Width : 3.420
Height : 10.082
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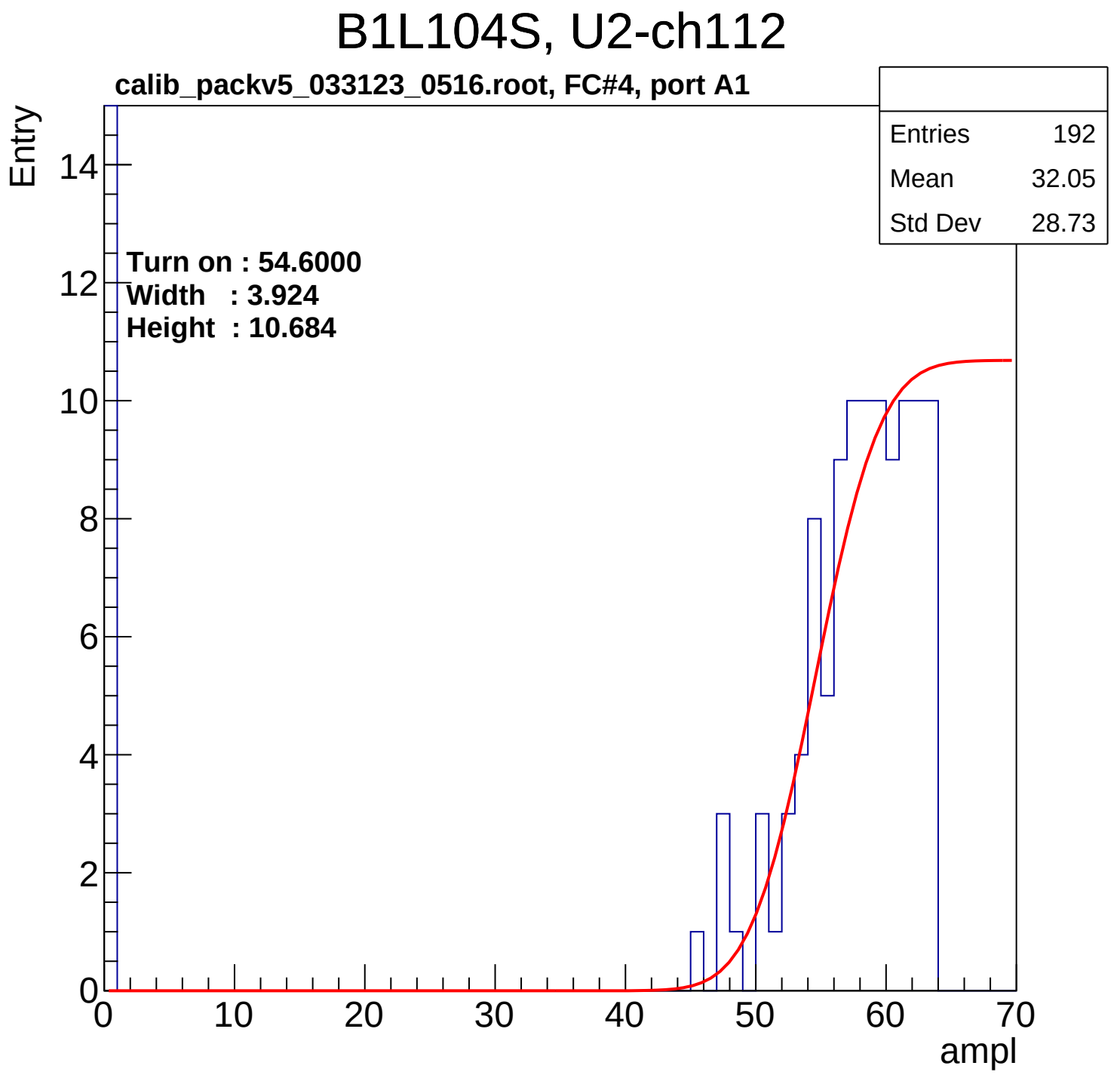
B1L104S, U2-ch112
calib_packv5_033123_0516.root, FC#4, port A1
Entries 192
Mean 32.05
Std Dev 28.73
Turn on : 54.6000
Width : 3.924
Height : 10.684
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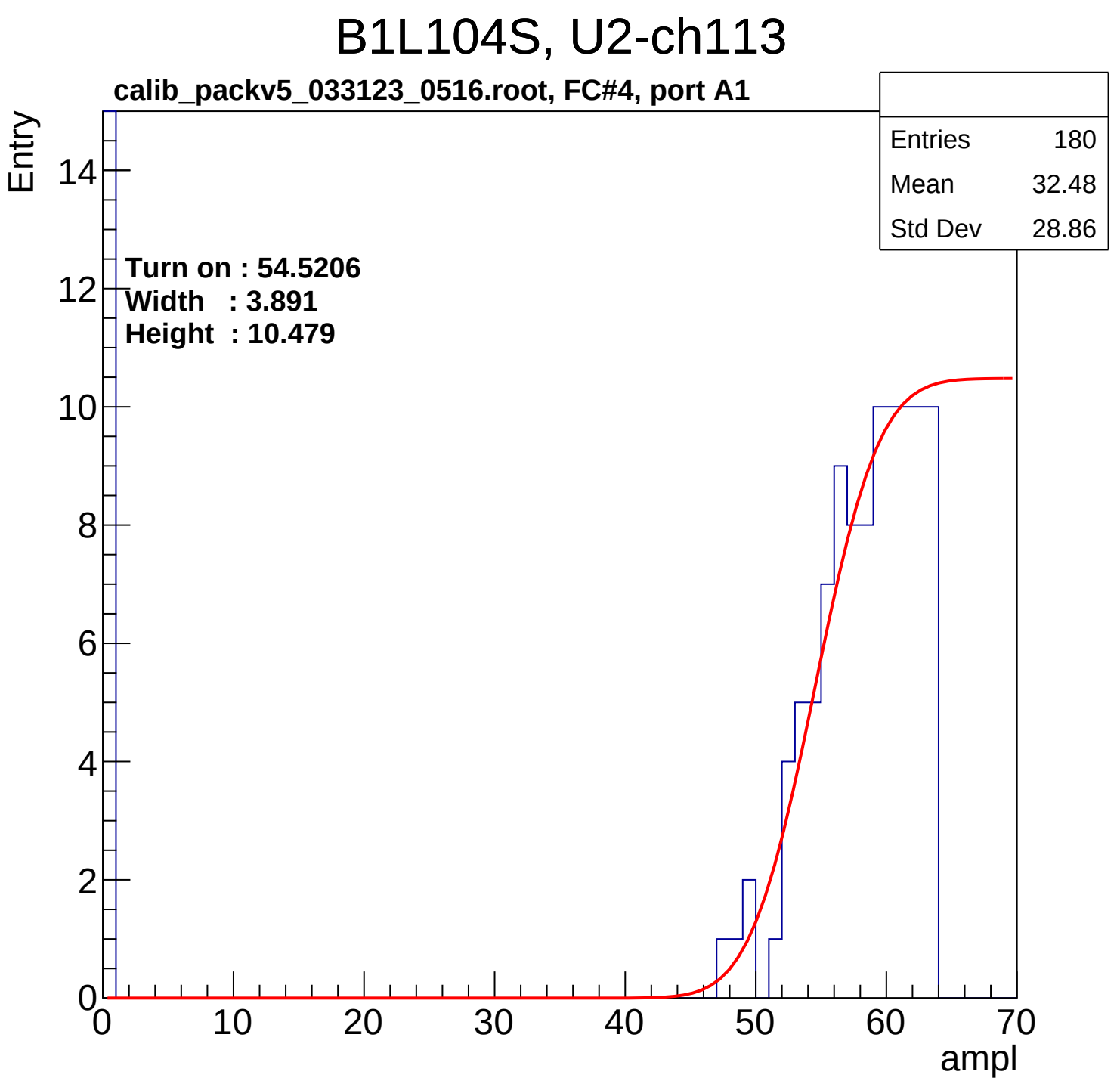
B1L104S, U2-ch113
calib_packv5_033123_0516.root, FC#4, port A1
Entries 180
Mean 32.48
Std Dev 28.86
Turn on : 54.5206
Width : 3.891
Height : 10.479
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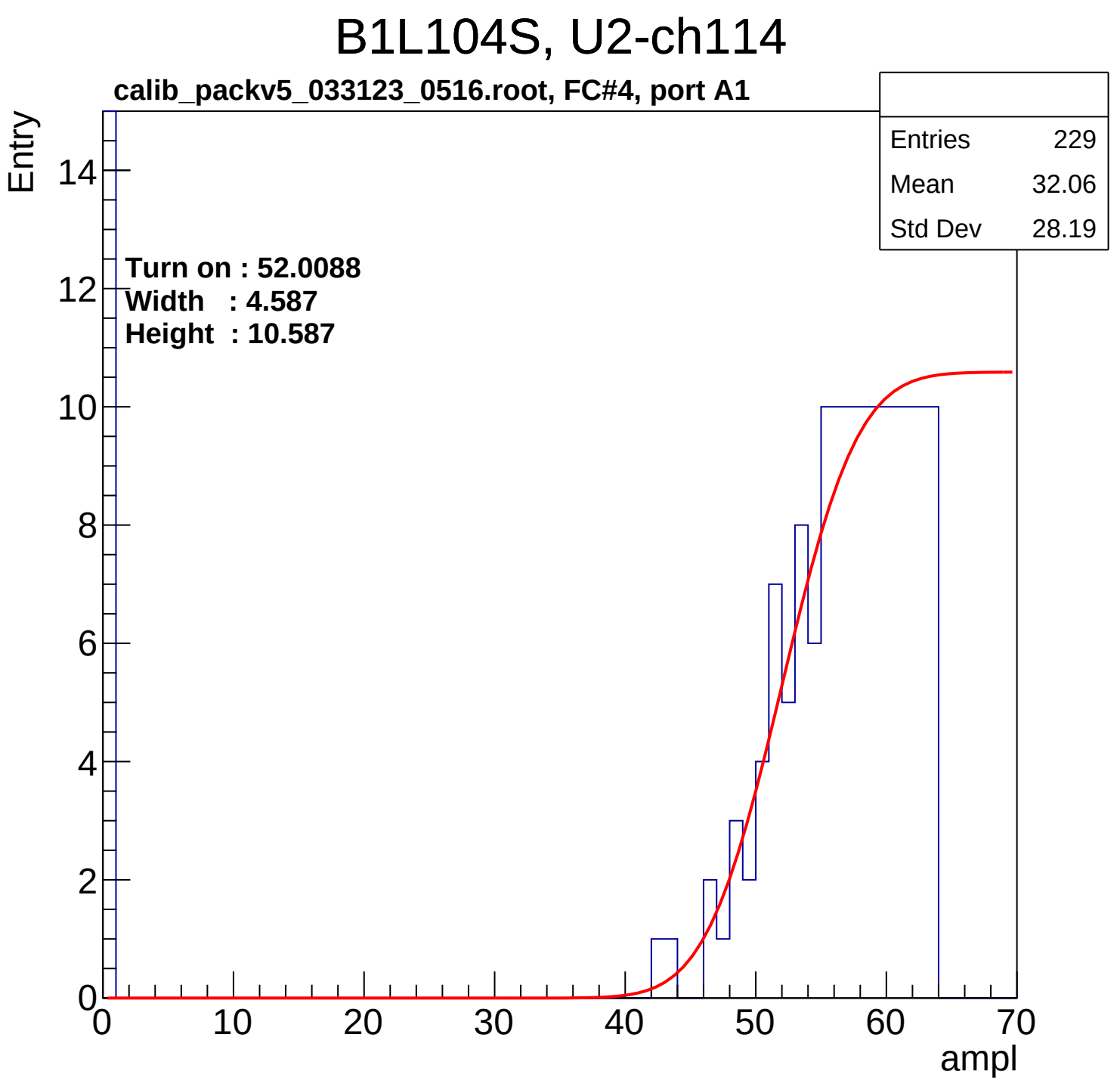
B1L104S, U2-ch114
calib_packv5_033123_0516.root, FC#4, port A1
Entries 229
Mean 32.06
Std Dev 28.19
Turn on : 52.0088
Width : 4.587
Height : 10.587
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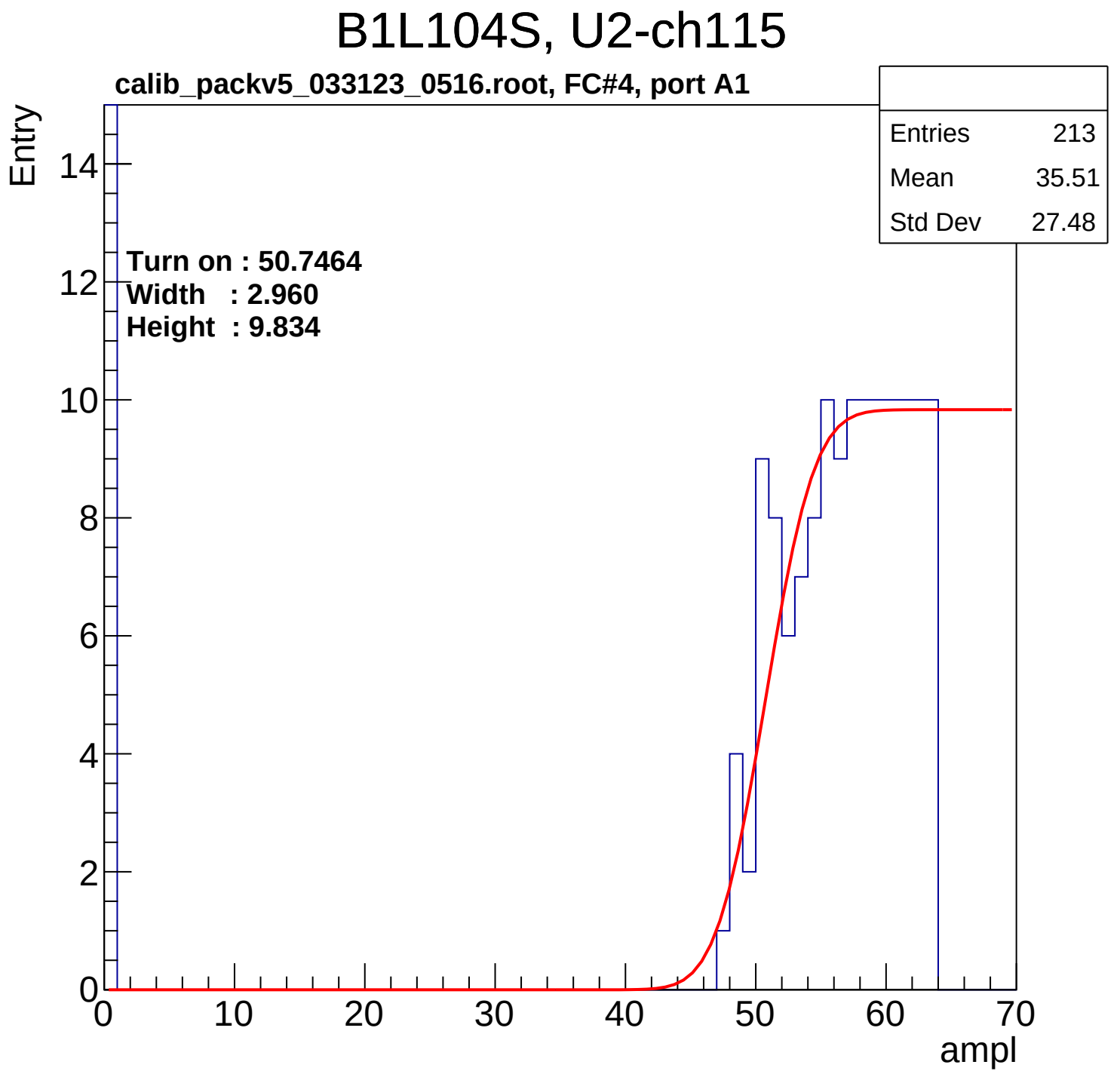
B1L104S, U2-ch115
calib_packv5_033123_0516.root, FC#4, port A1
Entries 213
Mean 35.51
Std Dev 27.48
Turn on : 50.7464
Width : 2.960
Height : 9.834
Entry
ampl
0
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4
6
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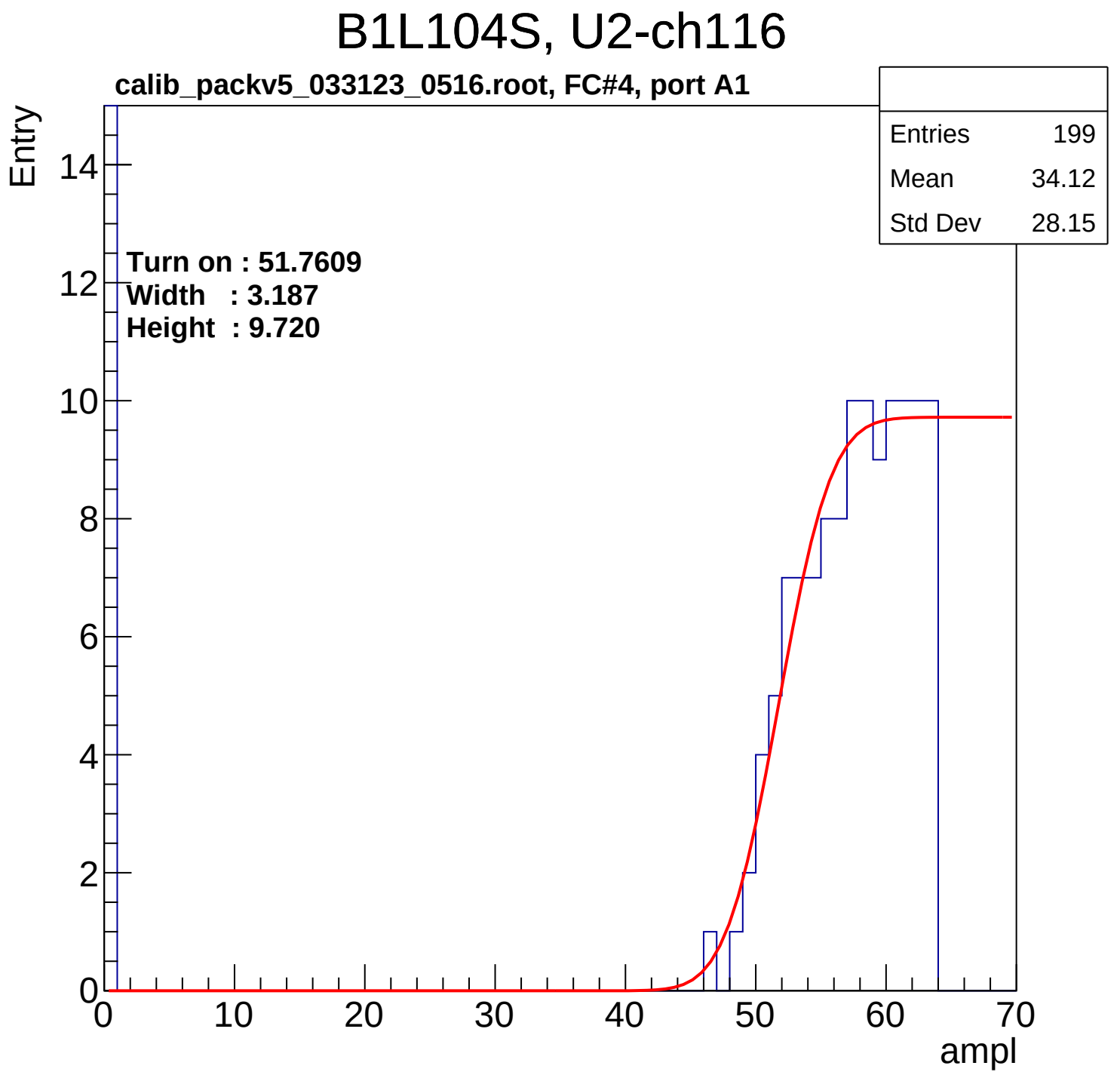
B1L104S, U2-ch116
calib_packv5_033123_0516.root, FC#4, port A1
Entries 199
Mean 34.12
Std Dev 28.15
Turn on : 51.7609
Width : 3.187
Height : 9.720
Entry
ampl
0
2
4
6
8
10
12
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0
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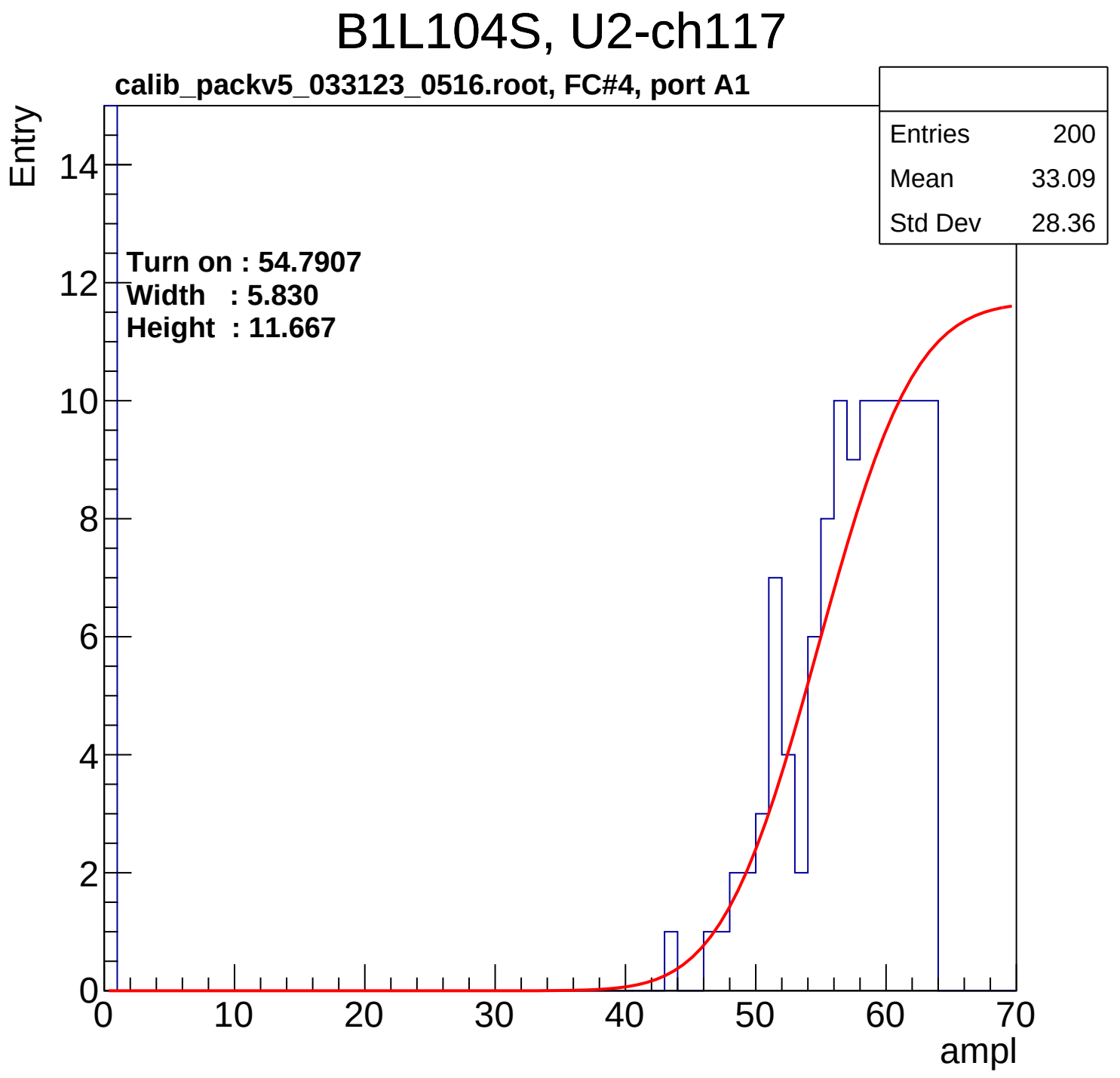
B1L104S, U2-ch117
calib_packv5_033123_0516.root, FC#4, port A1
Entries 200
Mean 33.09
Std Dev 28.36
Turn on : 54.7907
Width : 5.830
Height : 11.667
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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40
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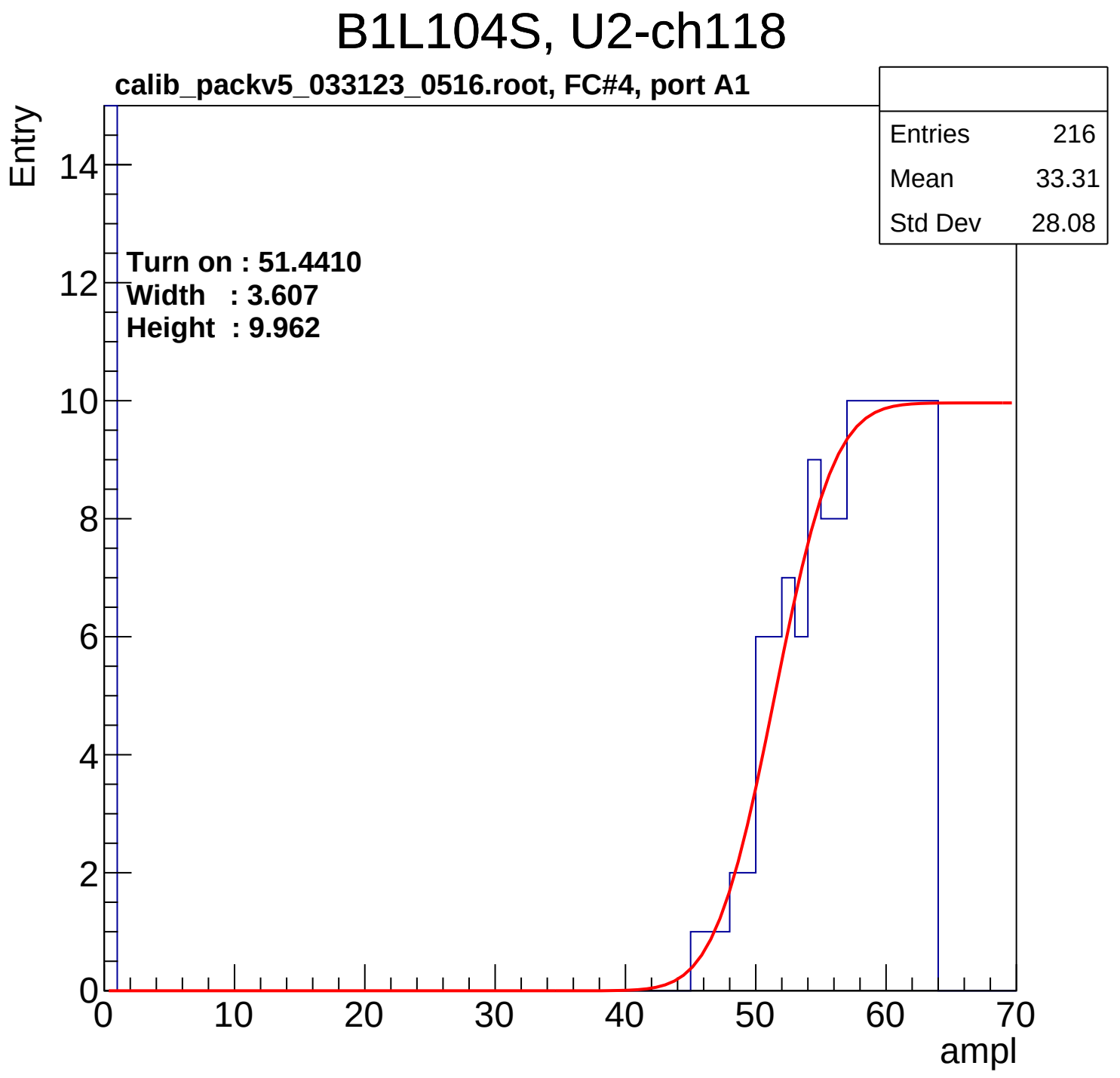
B1L104S, U2-ch118
calib_packv5_033123_0516.root, FC#4, port A1
Entries 216
Mean 33.31
Std Dev 28.08
Turn on : 51.4410
Width : 3.607
Height : 9.962
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
50
60
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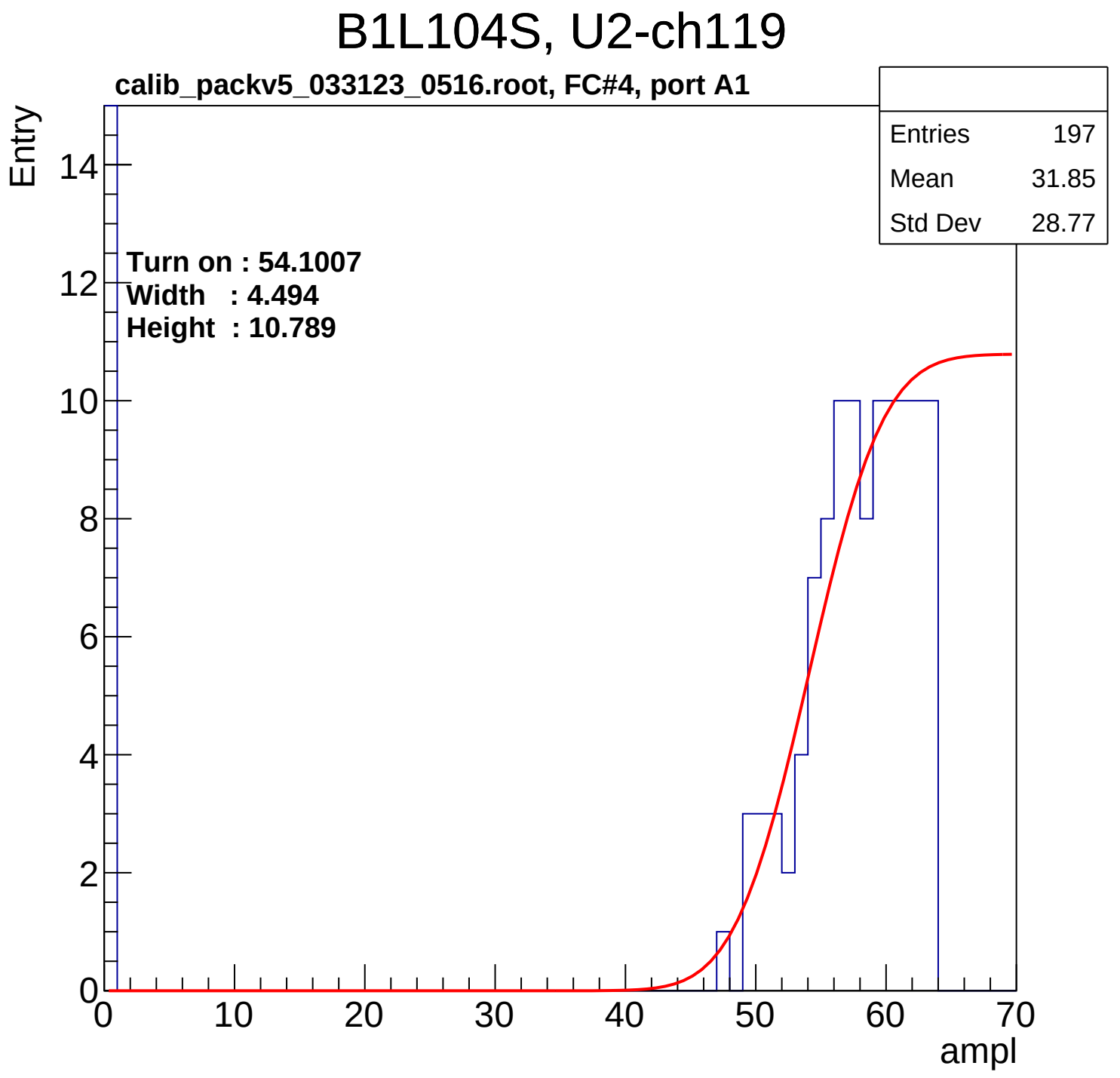
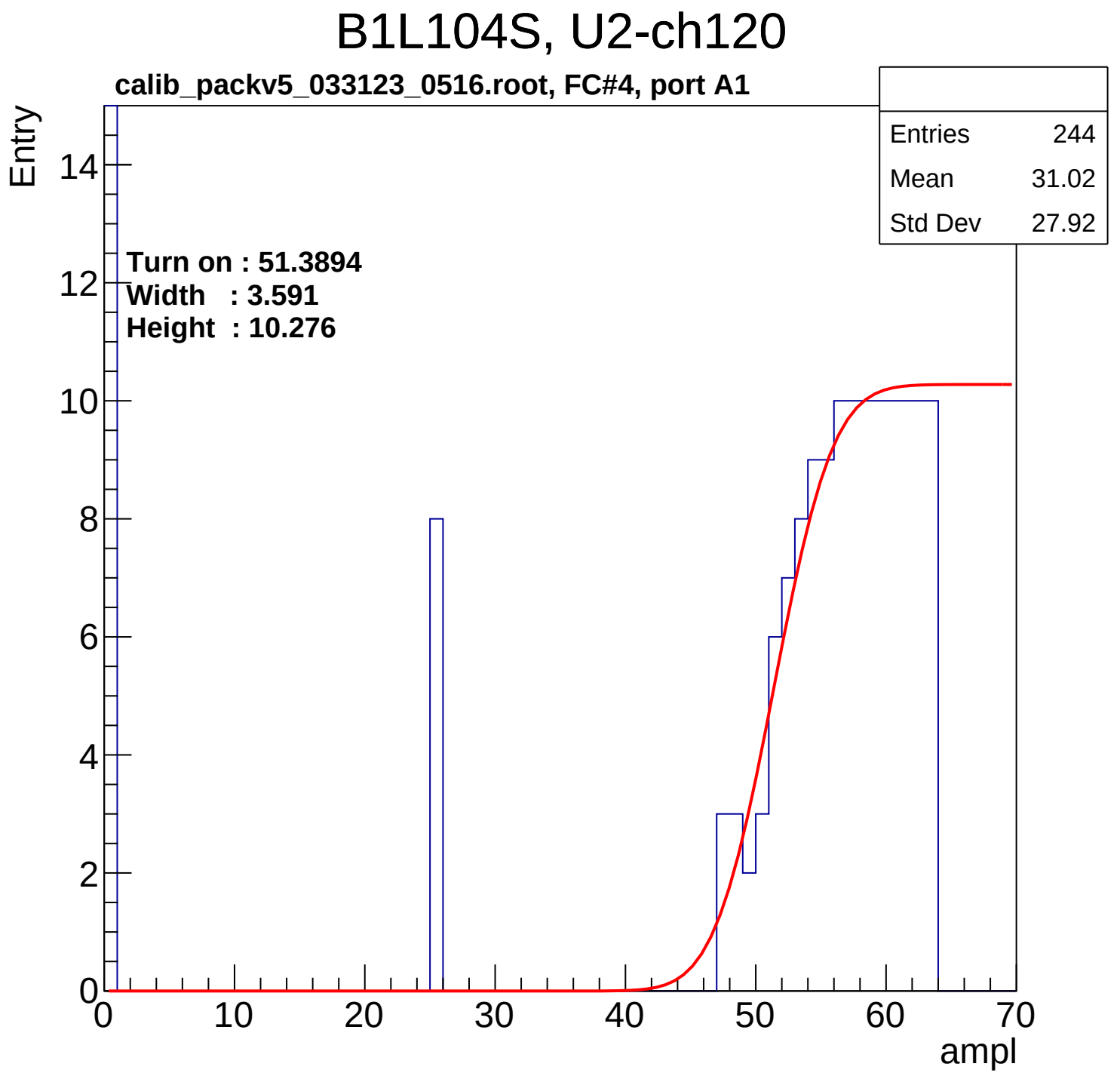
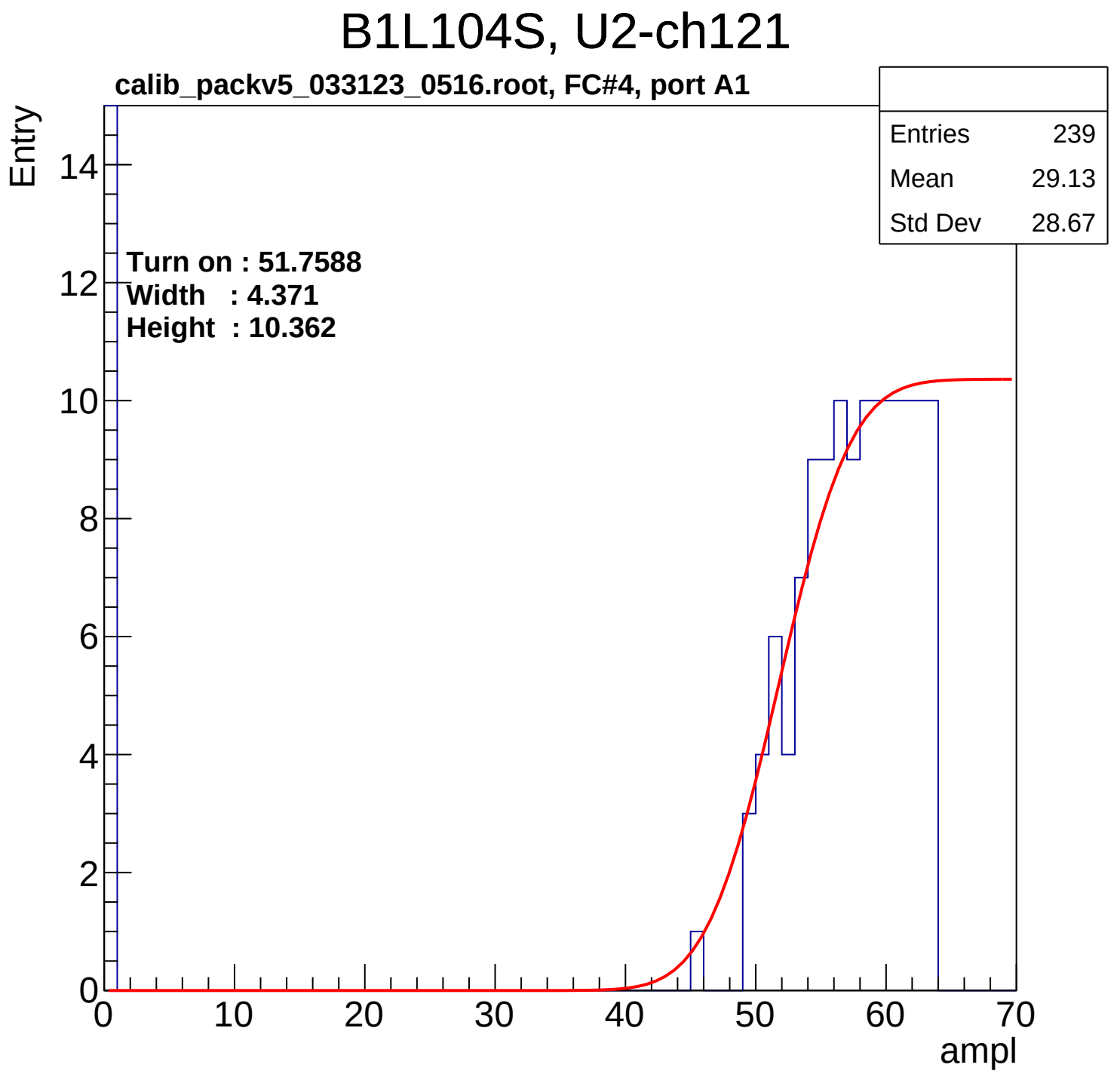

B1L104S, U2-ch119
calib_packv5_033123_0516.root, FC#4, port A1
Entries 197
Mean 31.85
Std Dev 28.77
Turn on : 54.1007
Width : 4.494
Height : 10.789
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L104S, U2-ch120
calib_packv5_033123_0516.root, FC#4, port A1
Entries 244
Mean 31.02
Std Dev 27.92
Turn on : 51.3894
Width : 3.591
Height : 10.276
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L104S, U2-ch121
calib_packv5_033123_0516.root, FC#4, port A1
Entries 239
Mean 29.13
Std Dev 28.67
Turn on : 51.7588
Width : 4.371
Height : 10.362
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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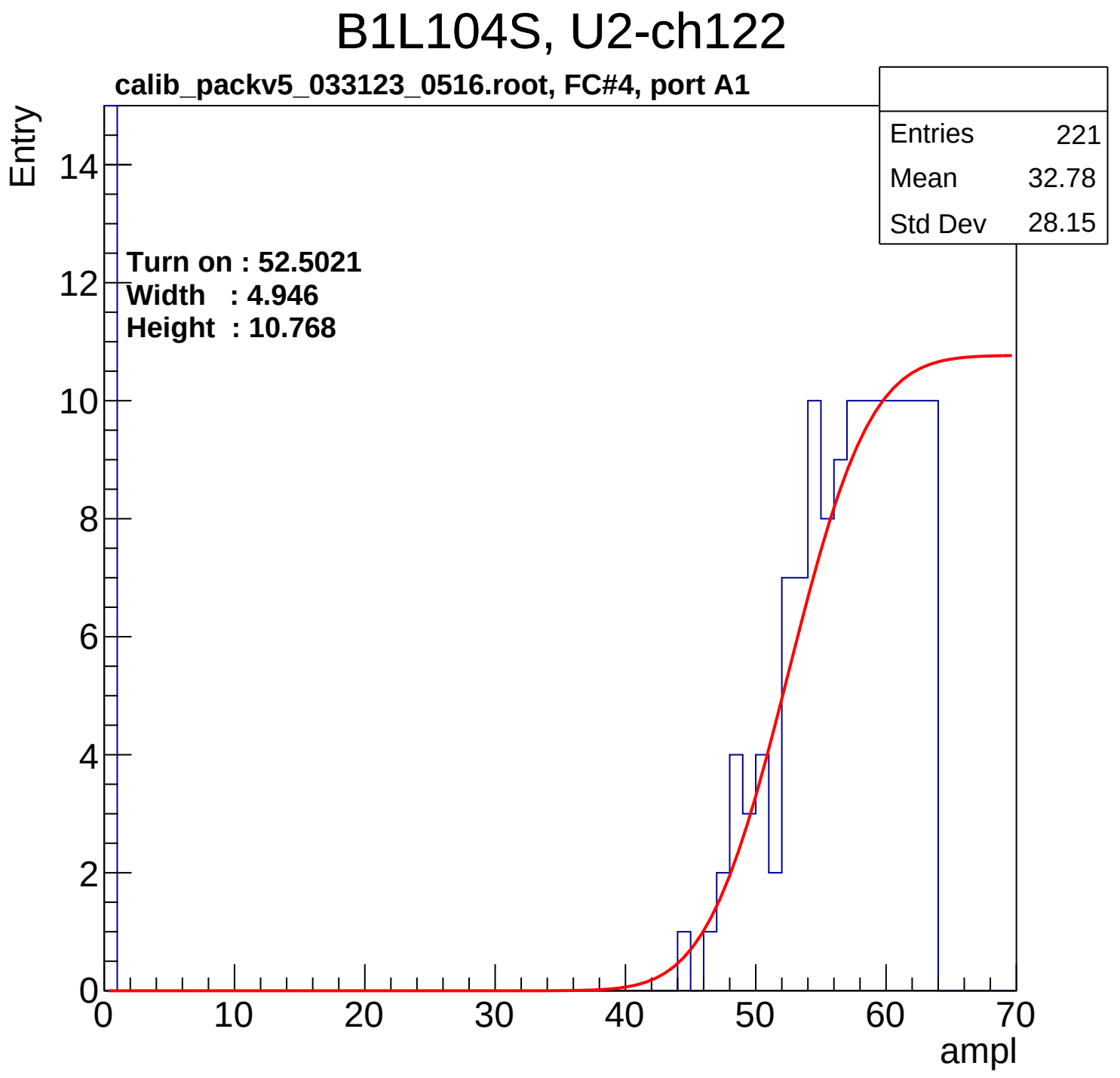
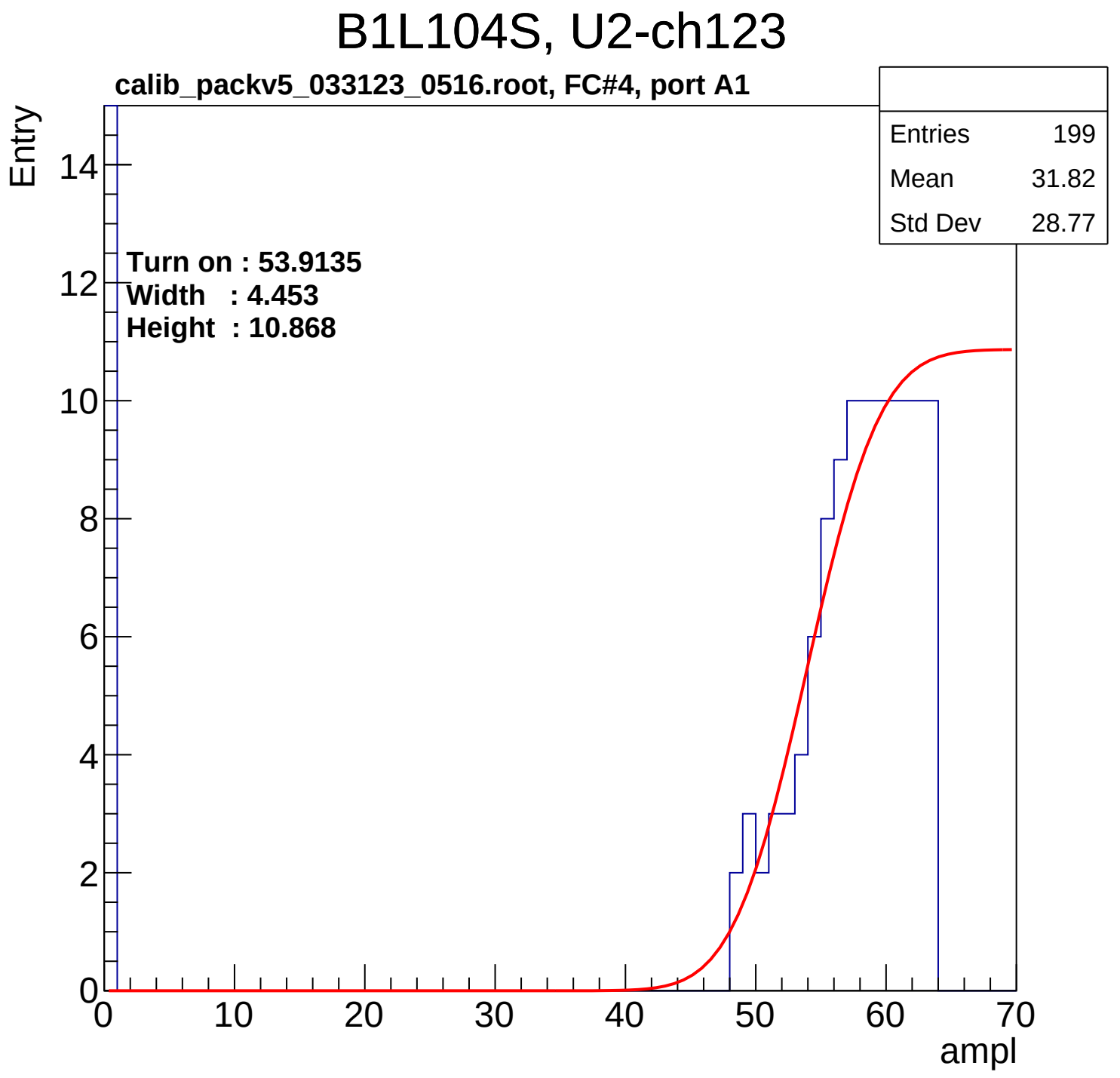

B1L104S, U2-ch122
calib_packv5_033123_0516.root, FC#4, port A1
Entries 221
Mean 32.78
Std Dev 28.15
Turn on : 52.5021
Width : 4.946
Height : 10.768
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L104S, U2-ch123
calib_packv5_033123_0516.root, FC#4, port A1
Entries 199
Mean 31.82
Std Dev 28.77
Turn on : 53.9135
Width : 4.453
Height : 10.868
Entry
ampl
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2
4
6
8
10
12
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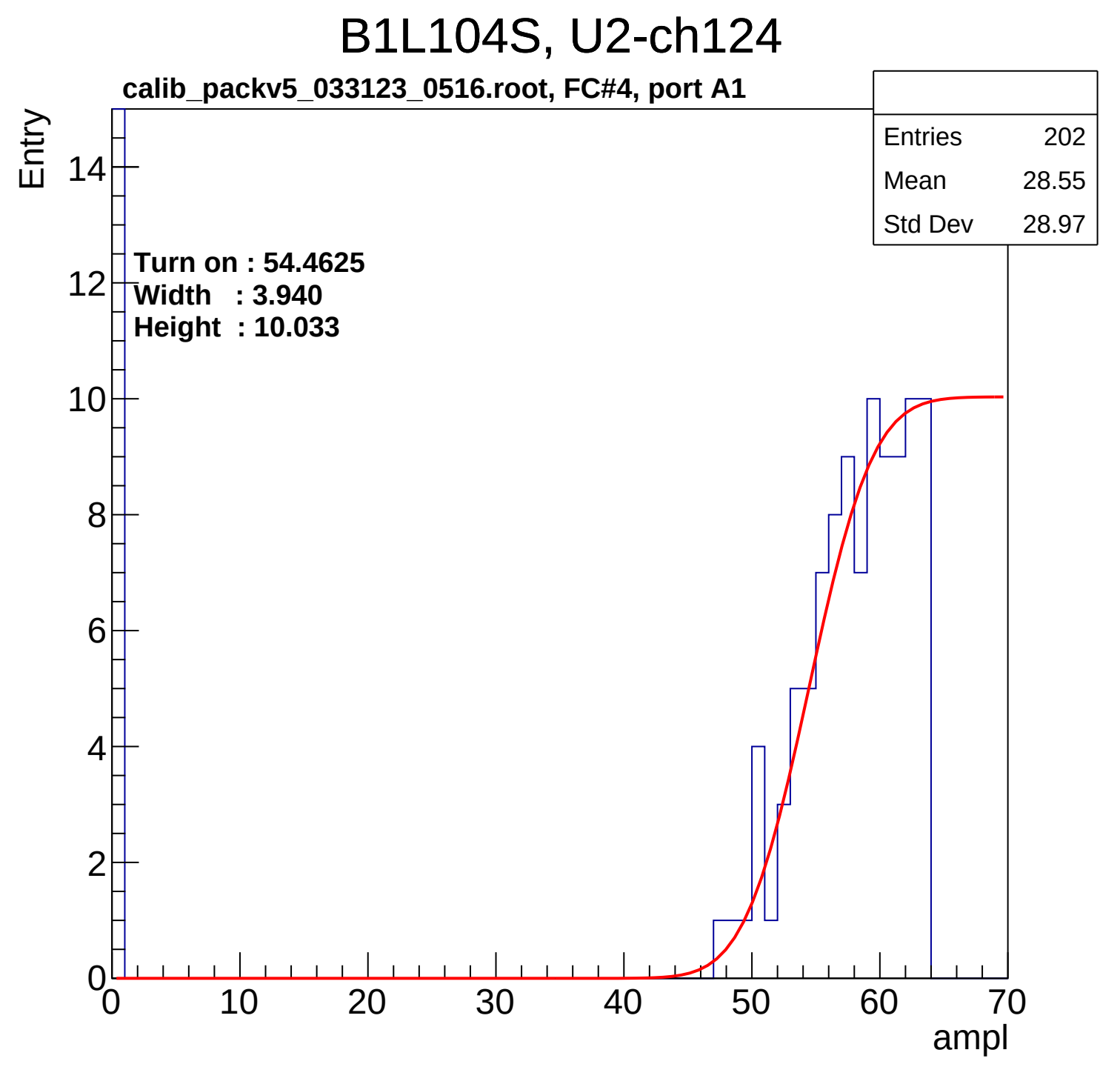
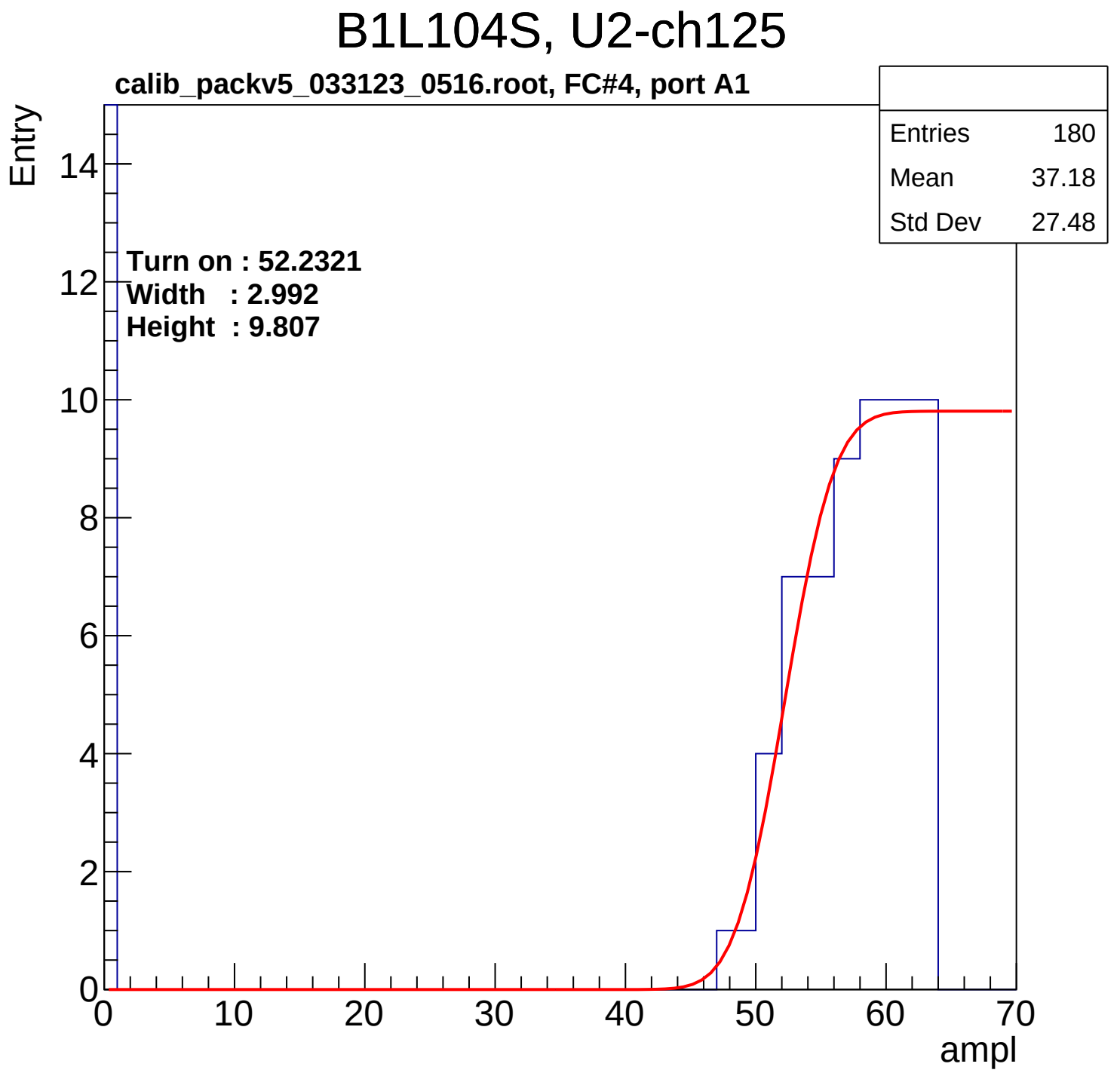
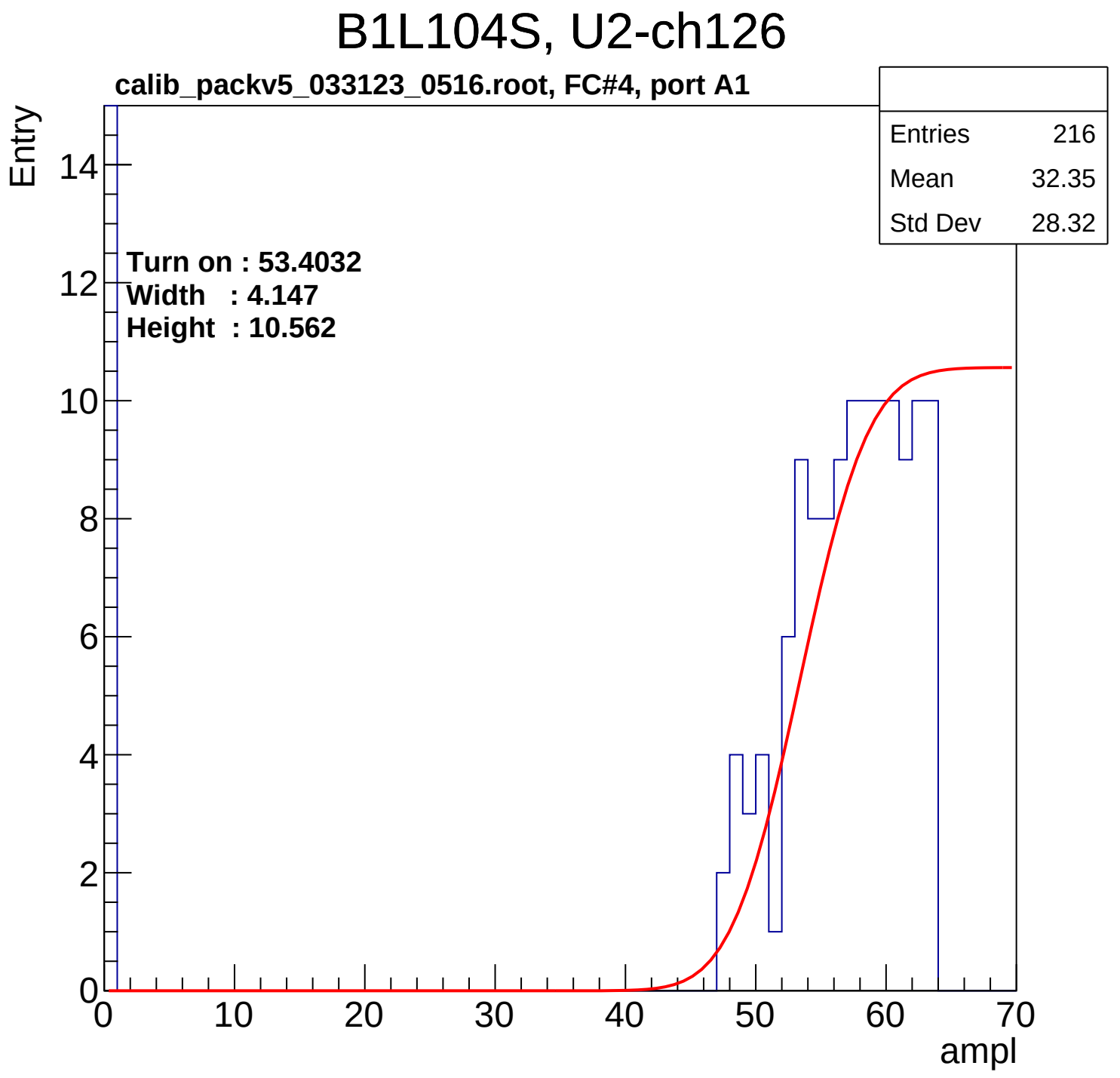
0
10
20
30
40
50
60
70


B1L104S, U2-ch124
calib_packv5_033123_0516.root, FC#4, port A1
Entries 202
Mean 28.55
Std Dev 28.97
Turn on : 54.4625
Width : 3.940
Height : 10.033
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L104S, U2-ch125
calib_packv5_033123_0516.root, FC#4, port A1
Entries 180
Mean 37.18
Std Dev 27.48
Turn on : 52.2321
Width : 2.992
Height : 9.807
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L104S, U2-ch126
calib_packv5_033123_0516.root, FC#4, port A1
Entries 216
Mean 32.35
Std Dev 28.32
Turn on : 53.4032
Width : 4.147
Height : 10.562
Entry
ampl
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4
6
8
10
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0
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20
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40
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60
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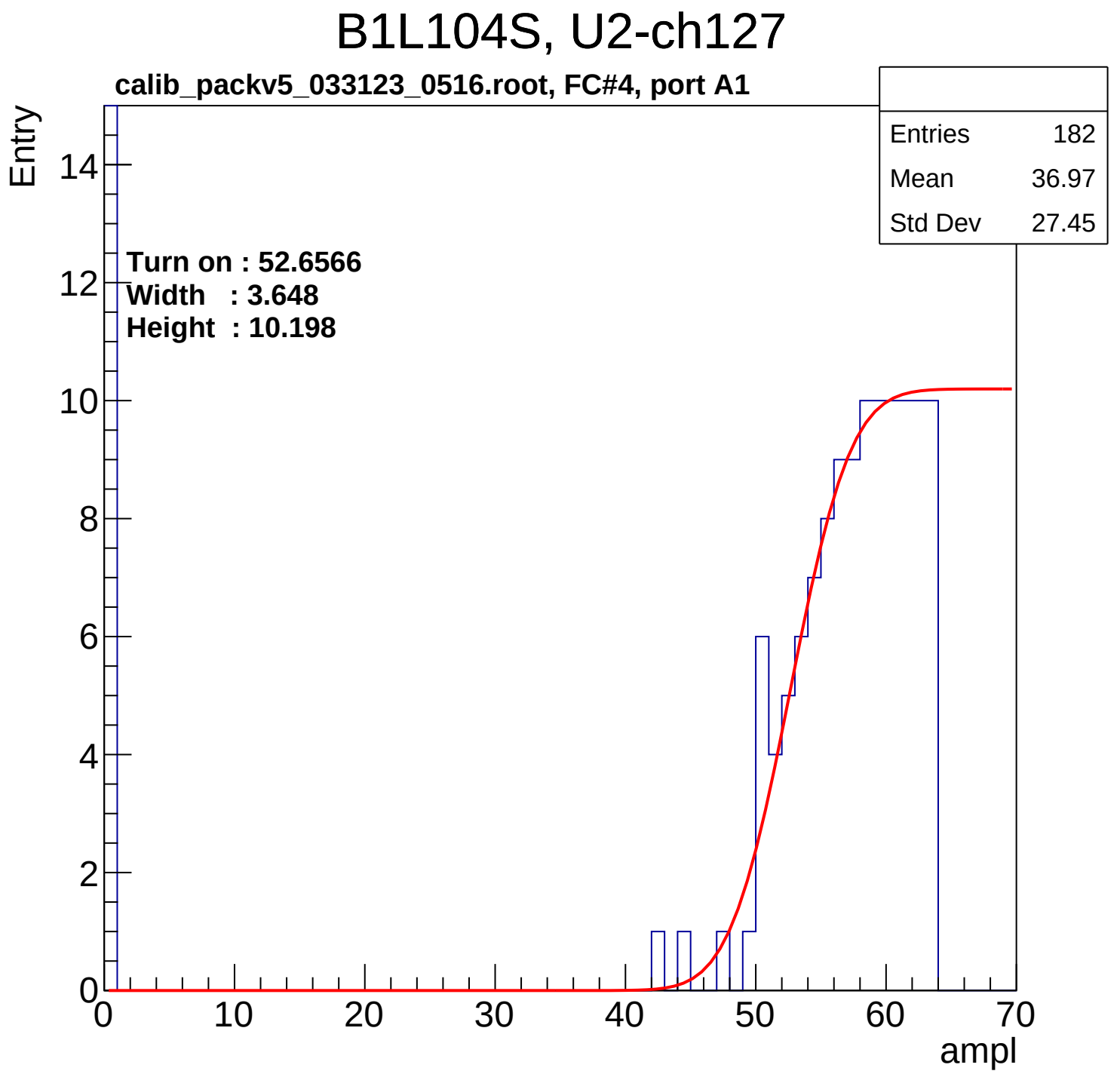
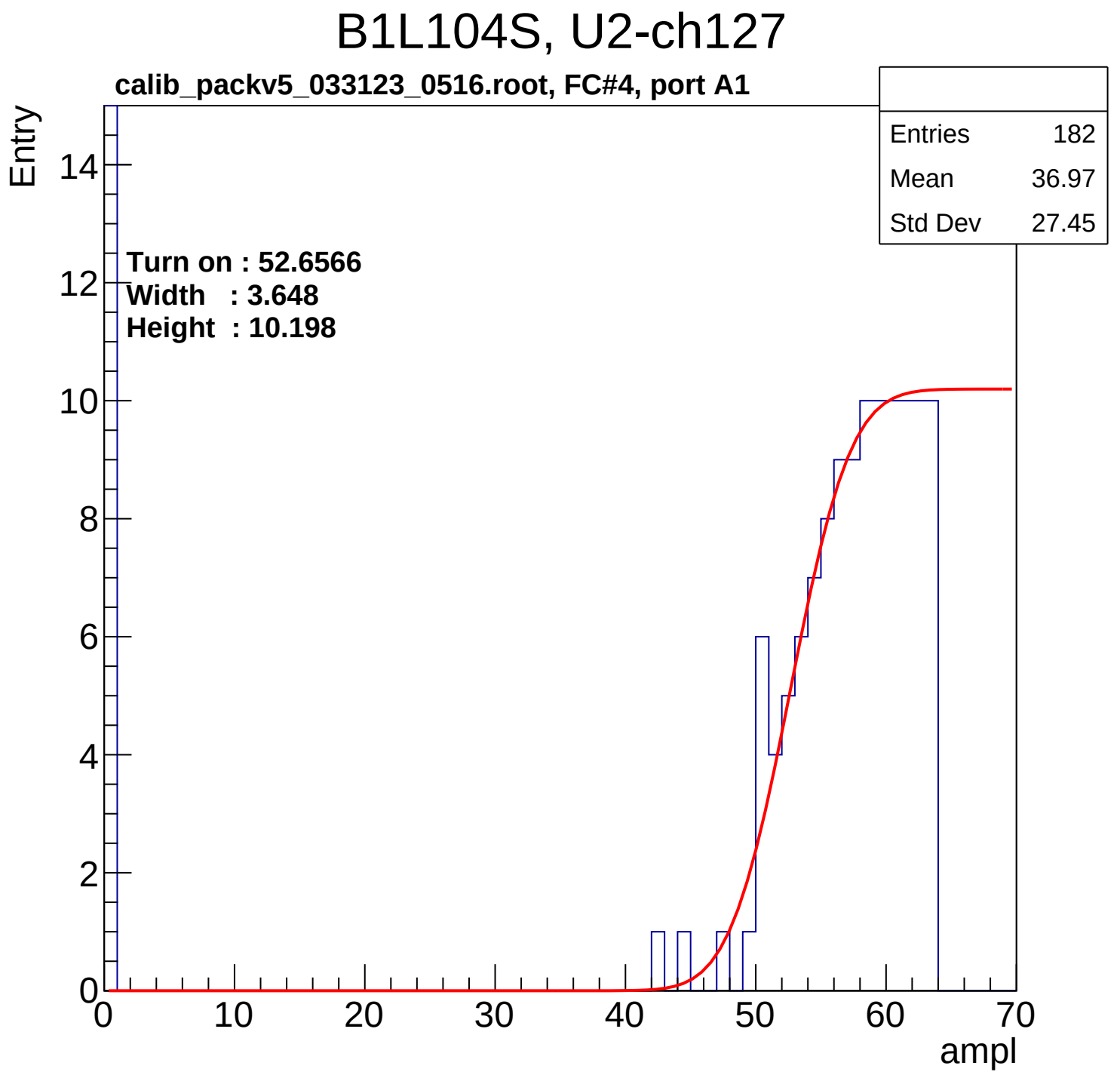

B1L104S, U2-ch127
calib_packv5_033123_0516.root, FC#4, port A1
Entries 182
Mean 36.97
Std Dev 27.45
Turn on : 52.6566
Width : 3.648
Height : 10.198
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L104S, U2-ch127
calib_packv5_033123_0516.root, FC#4, port A1
Entries 182
Mean 36.97
Std Dev 27.45
Turn on : 52.6566
Width : 3.648
Height : 10.198
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70