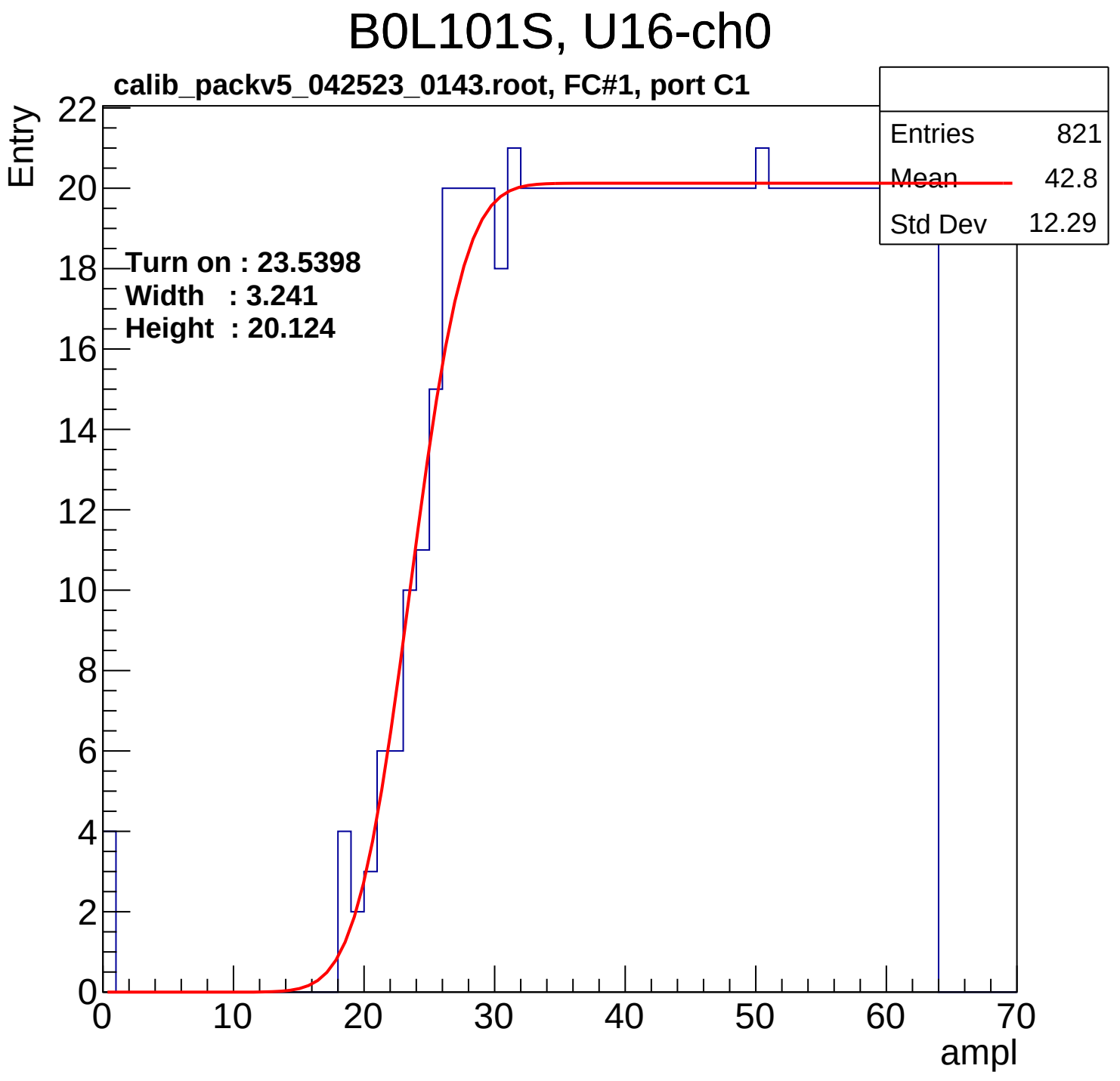
B0L101S, U16-ch0
calib_packv5_042523_0143.root, FC#1, port C1
Entries 821
Mean 42.8
Std Dev 12.29
Turn on : 23.5398
Width : 3.241
Height : 20.124
Entry
ampl
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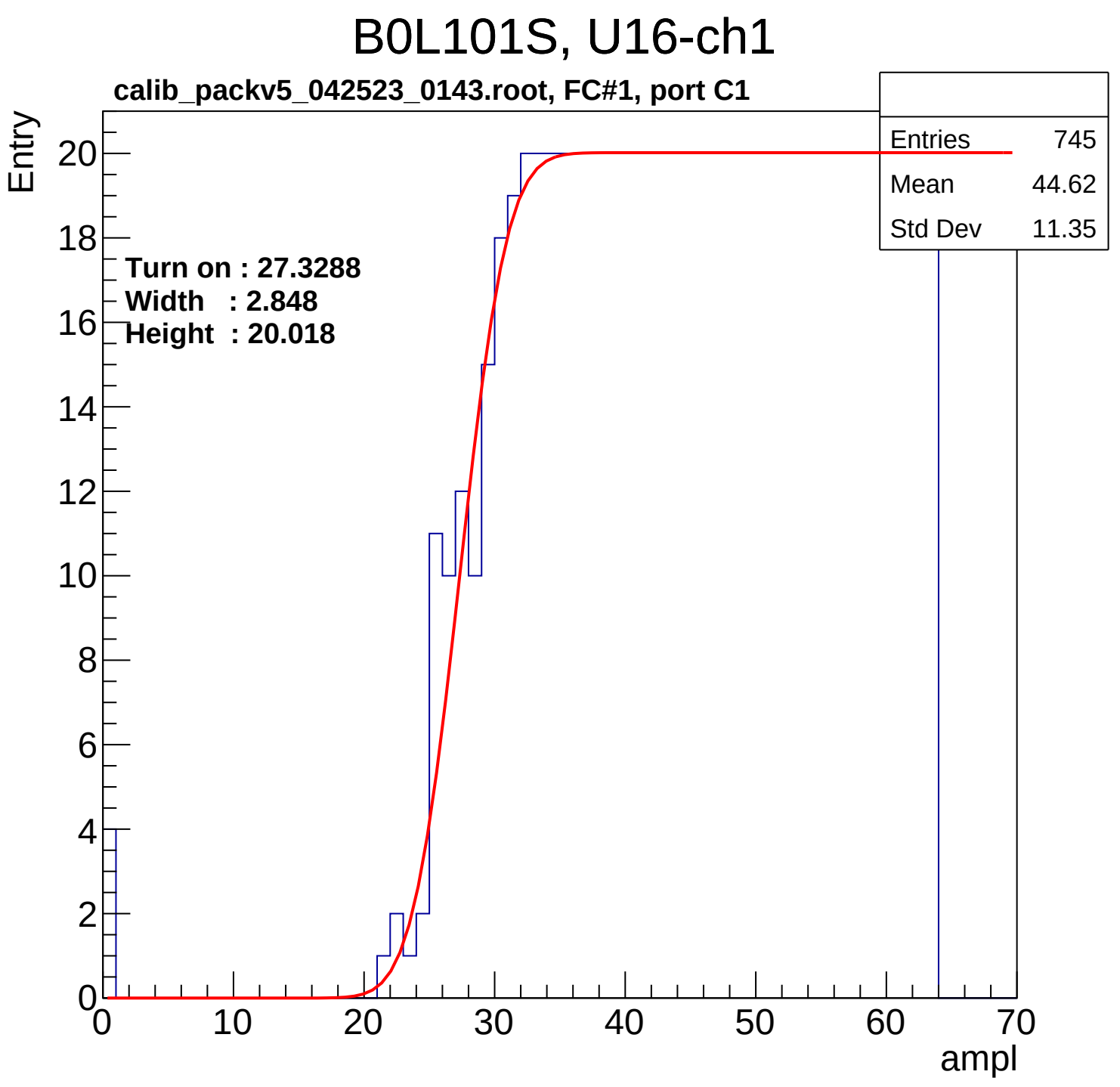
B0L101S, U16-ch1
calib_packv5_042523_0143.root, FC#1, port C1
Entries 745
Mean 44.62
Std Dev 11.35
Turn on : 27.3288
Width : 2.848
Height : 20.018
Entry
ampl
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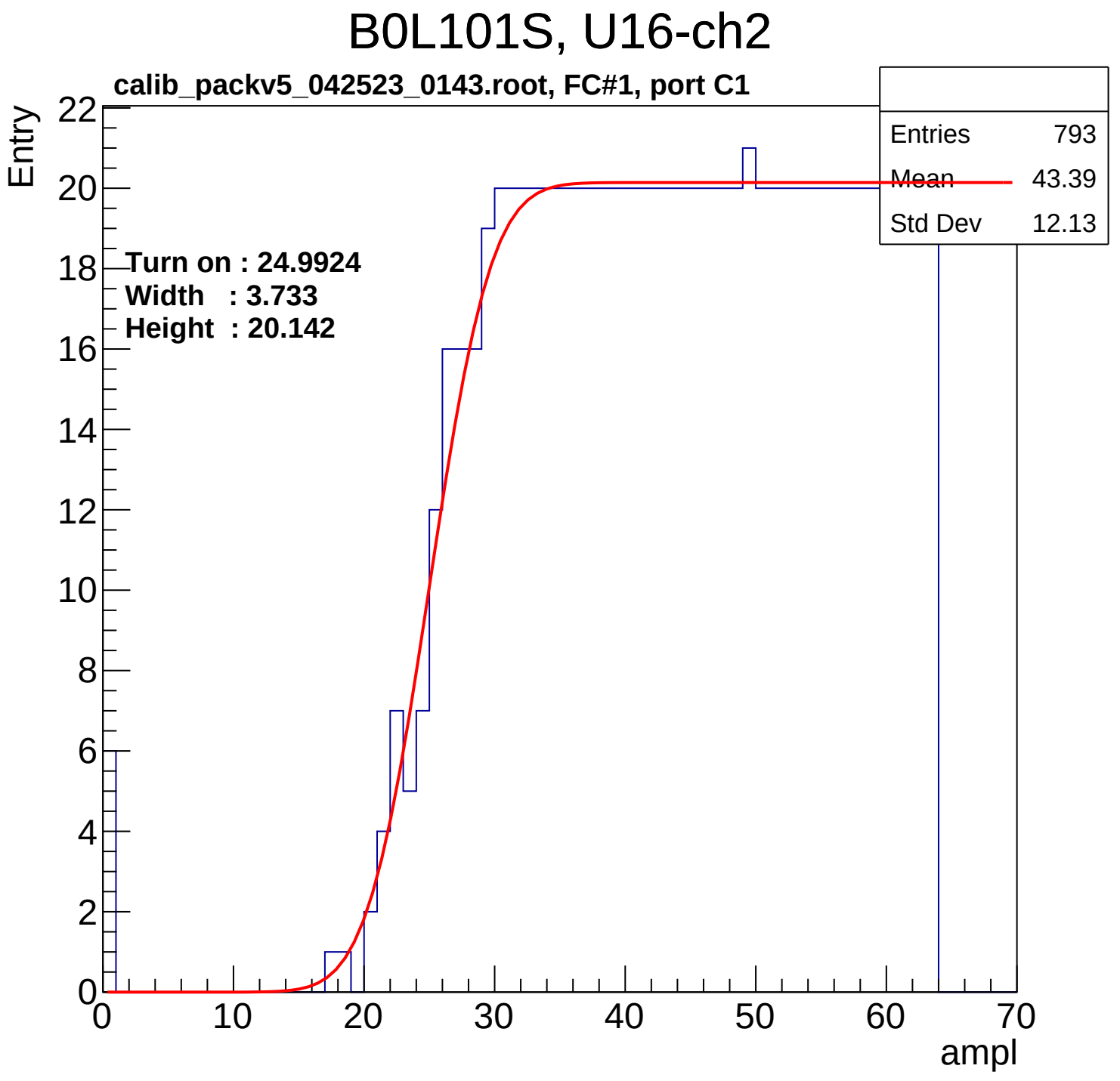
B0L101S, U16-ch2
calib_packv5_042523_0143.root, FC#1, port C1
Entries 793
Mean 43.39
Std Dev 12.13
Turn on : 24.9924
Width : 3.733
Height : 20.142
Entry
ampl
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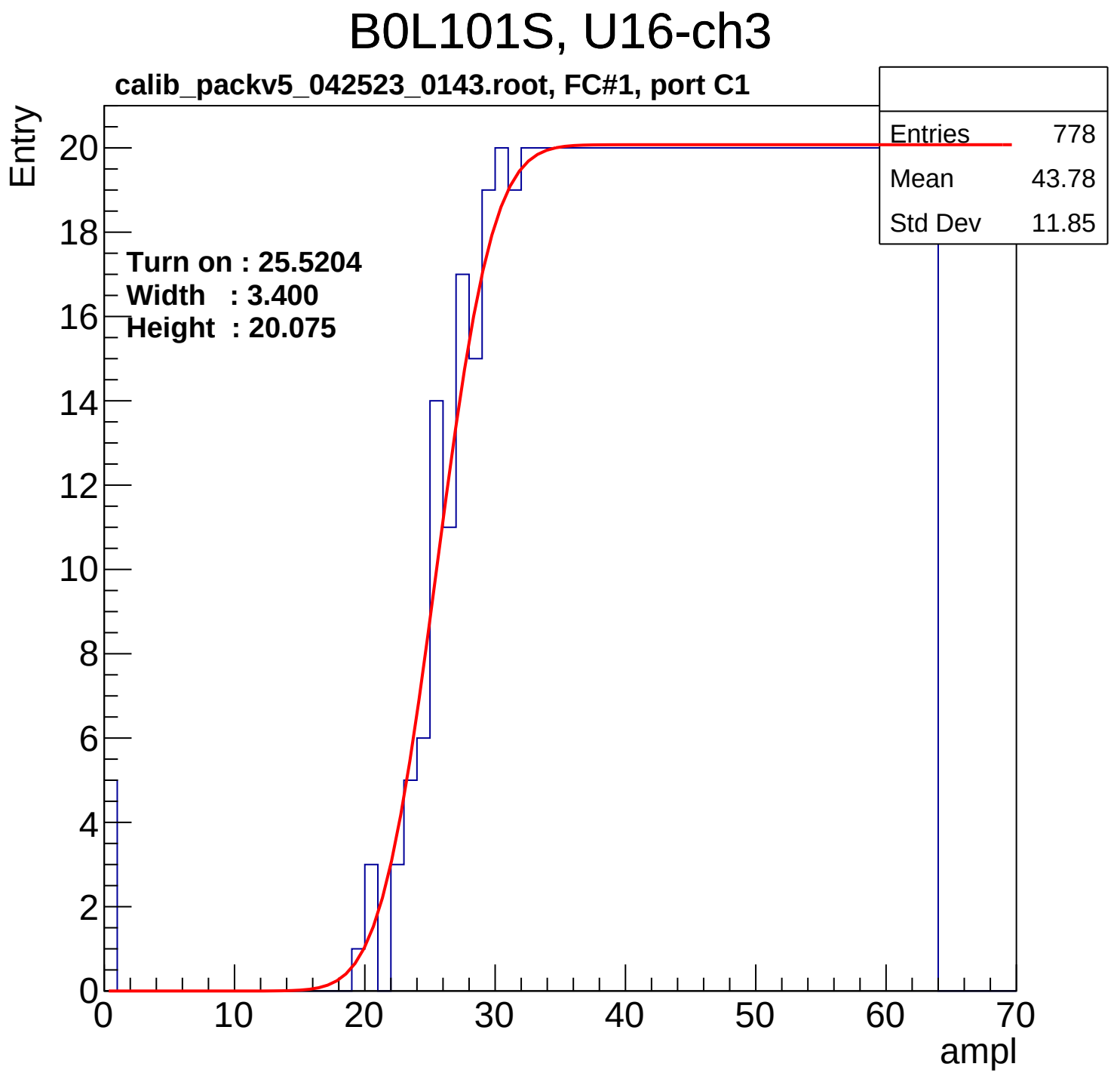
B0L101S, U16-ch3
calib_packv5_042523_0143.root, FC#1, port C1
Entries 778
Mean 43.78
Std Dev 11.85
Turn on : 25.5204
Width : 3.400
Height : 20.075
Entry
ampl
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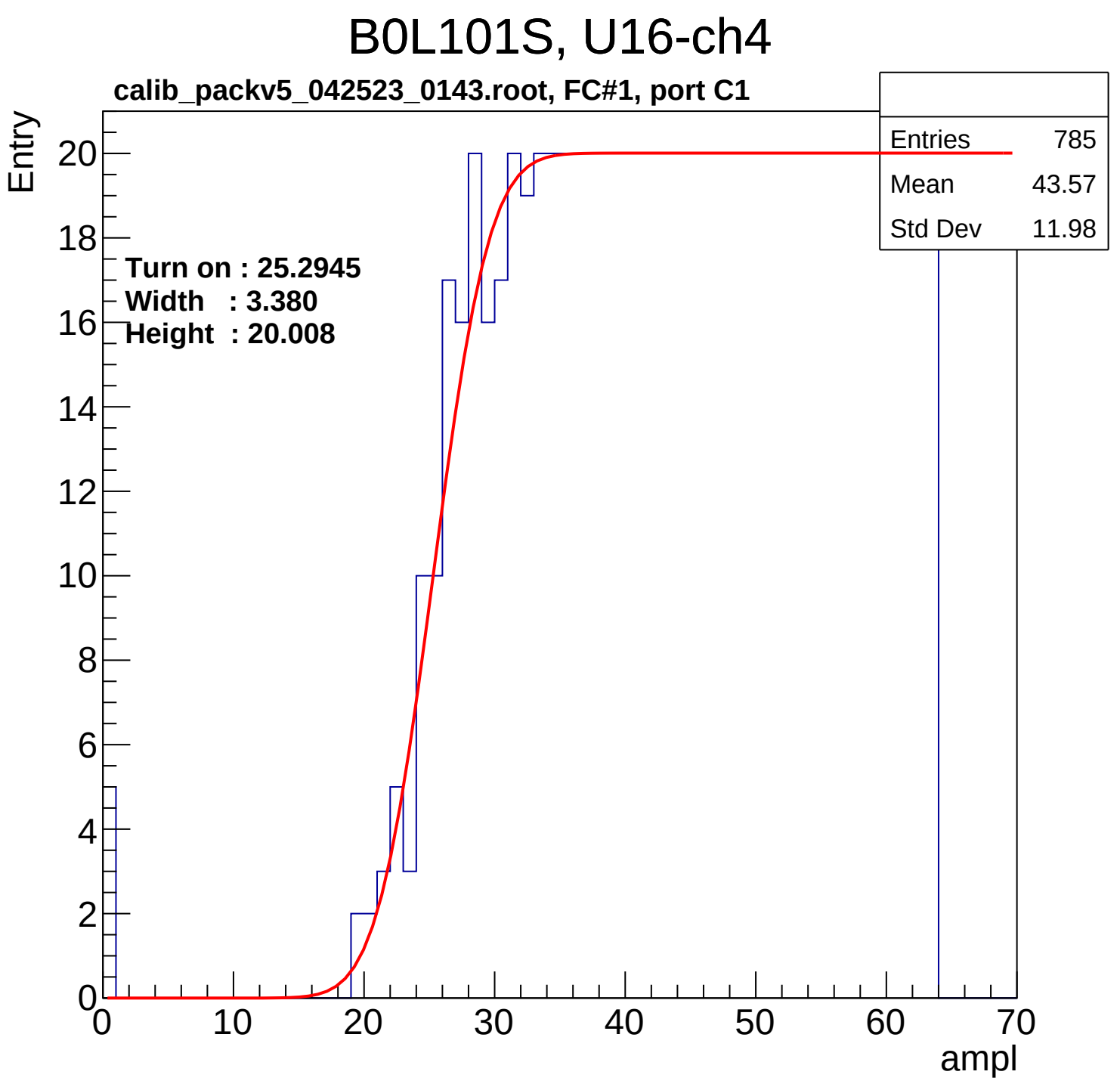
B0L101S, U16-ch4
calib_packv5_042523_0143.root, FC#1, port C1
Entries 785
Mean 43.57
Std Dev 11.98
Turn on : 25.2945
Width : 3.380
Height : 20.008
Entry
ampl
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6
8
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14
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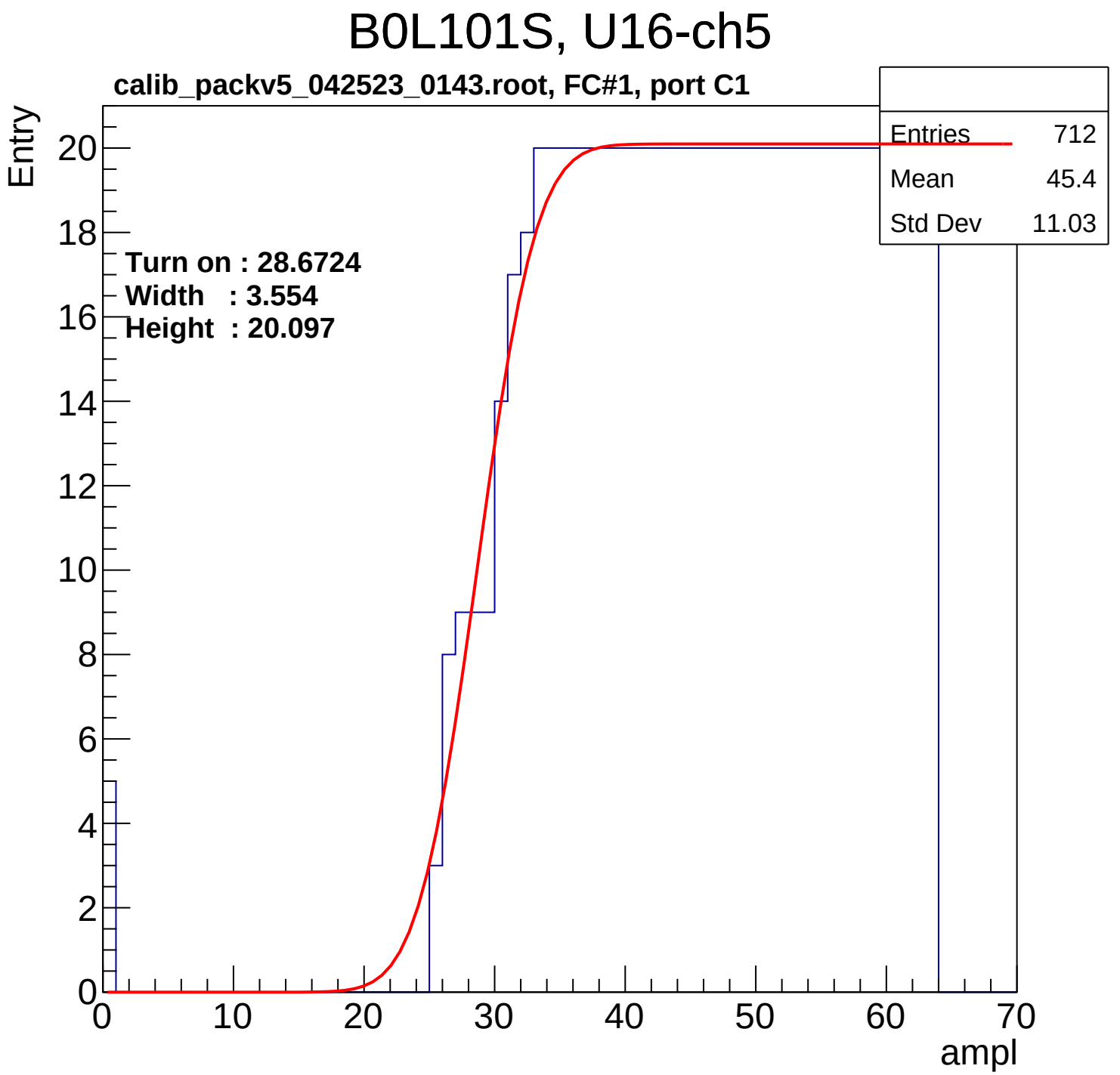
B0L101S, U16-ch5
calib_packv5_042523_0143.root, FC#1, port C1
Entries 712
Mean 45.4
Std Dev 11.03
Turn on : 28.6724
Width : 3.554
Height : 20.097
Entry
ampl
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6
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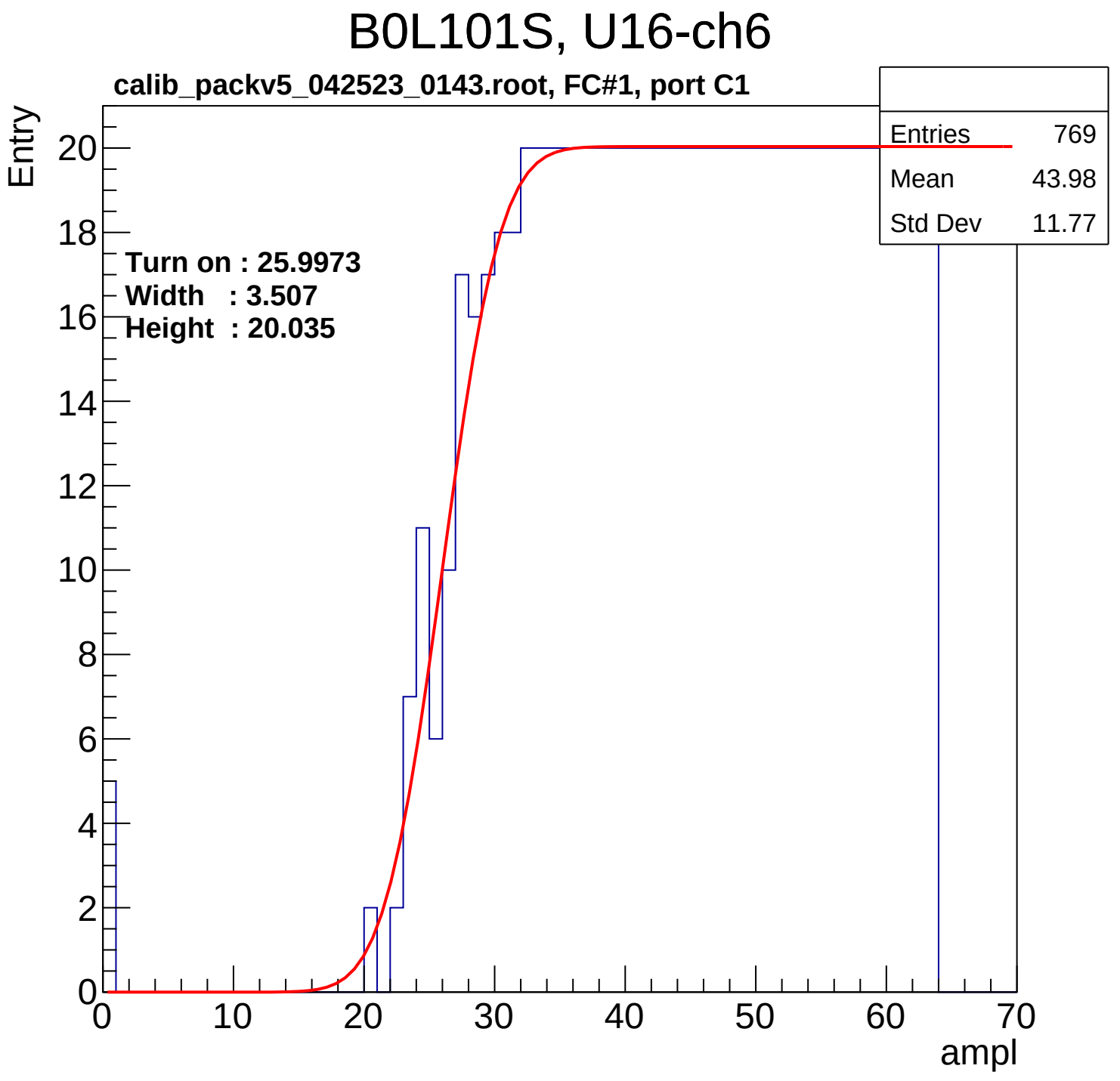
B0L101S, U16-ch6
calib_packv5_042523_0143.root, FC#1, port C1
Entries 769
Mean 43.98
Std Dev 11.77
Turn on : 25.9973
Width : 3.507
Height : 20.035
Entry
ampl
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8
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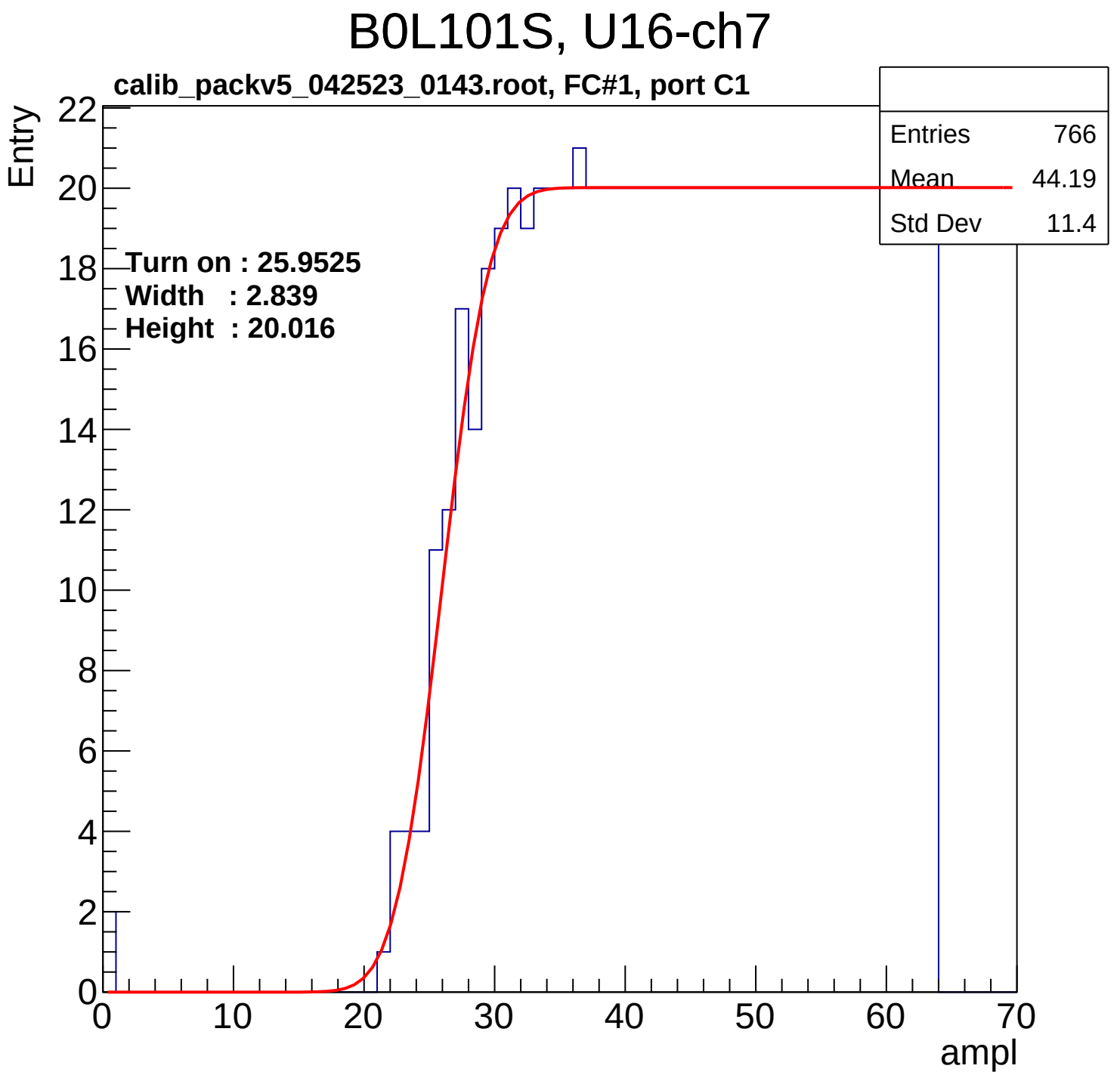
B0L101S, U16-ch7
calib_packv5_042523_0143.root, FC#1, port C1
Entries 766
Mean 44.19
Std Dev 11.4
Turn on : 25.9525
Width : 2.839
Height : 20.016
Entry
ampl
0
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8
10
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0
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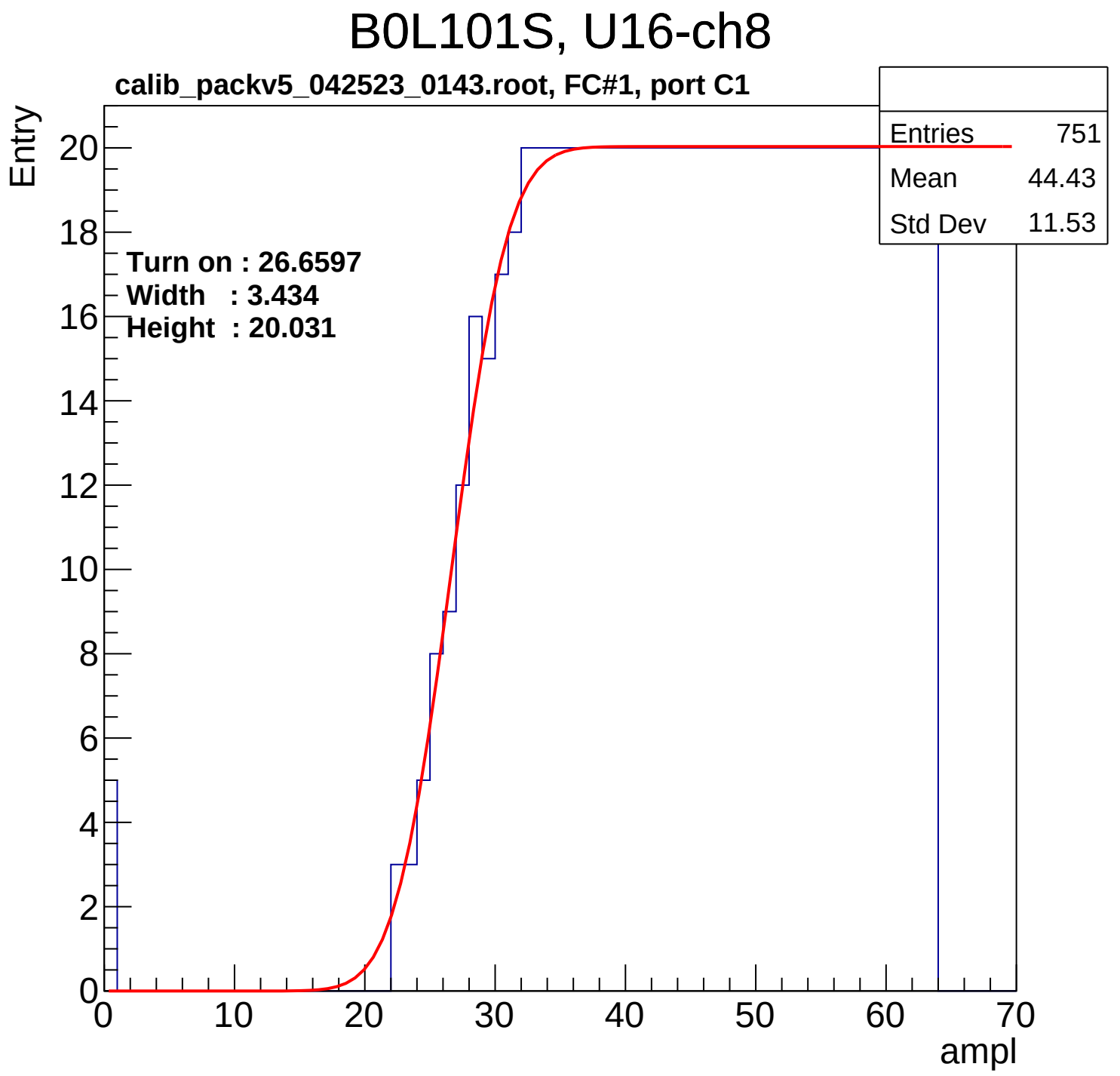
B0L101S, U16-ch8
calib_packv5_042523_0143.root, FC#1, port C1
Entries 751
Mean 44.43
Std Dev 11.53
Turn on : 26.6597
Width : 3.434
Height : 20.031
Entry
ampl
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6
8
10
12
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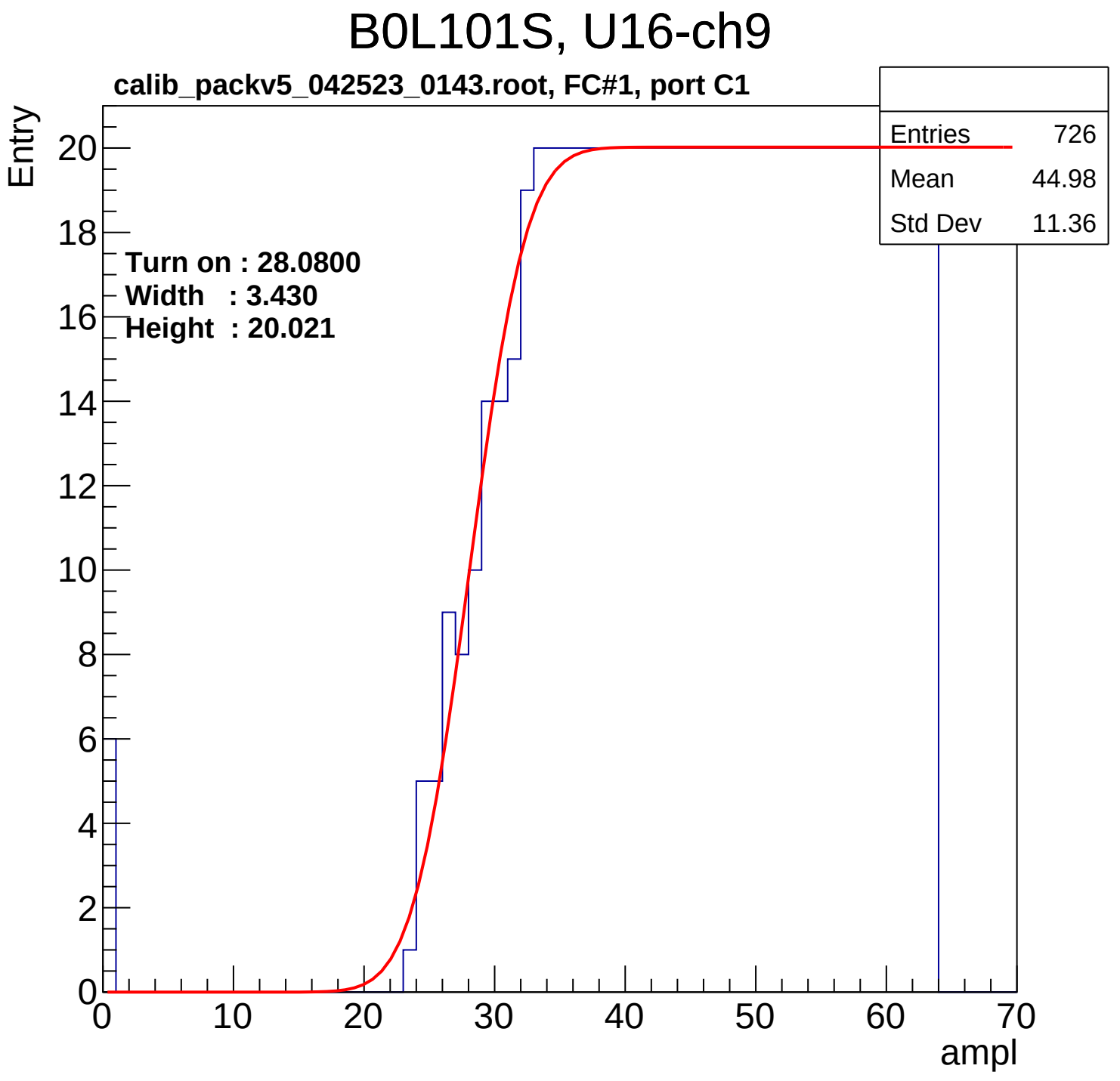
B0L101S, U16-ch9
calib_packv5_042523_0143.root, FC#1, port C1
Entries 726
Mean 44.98
Std Dev 11.36
Turn on : 28.0800
Width : 3.430
Height : 20.021
Entry
ampl
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6
8
10
12
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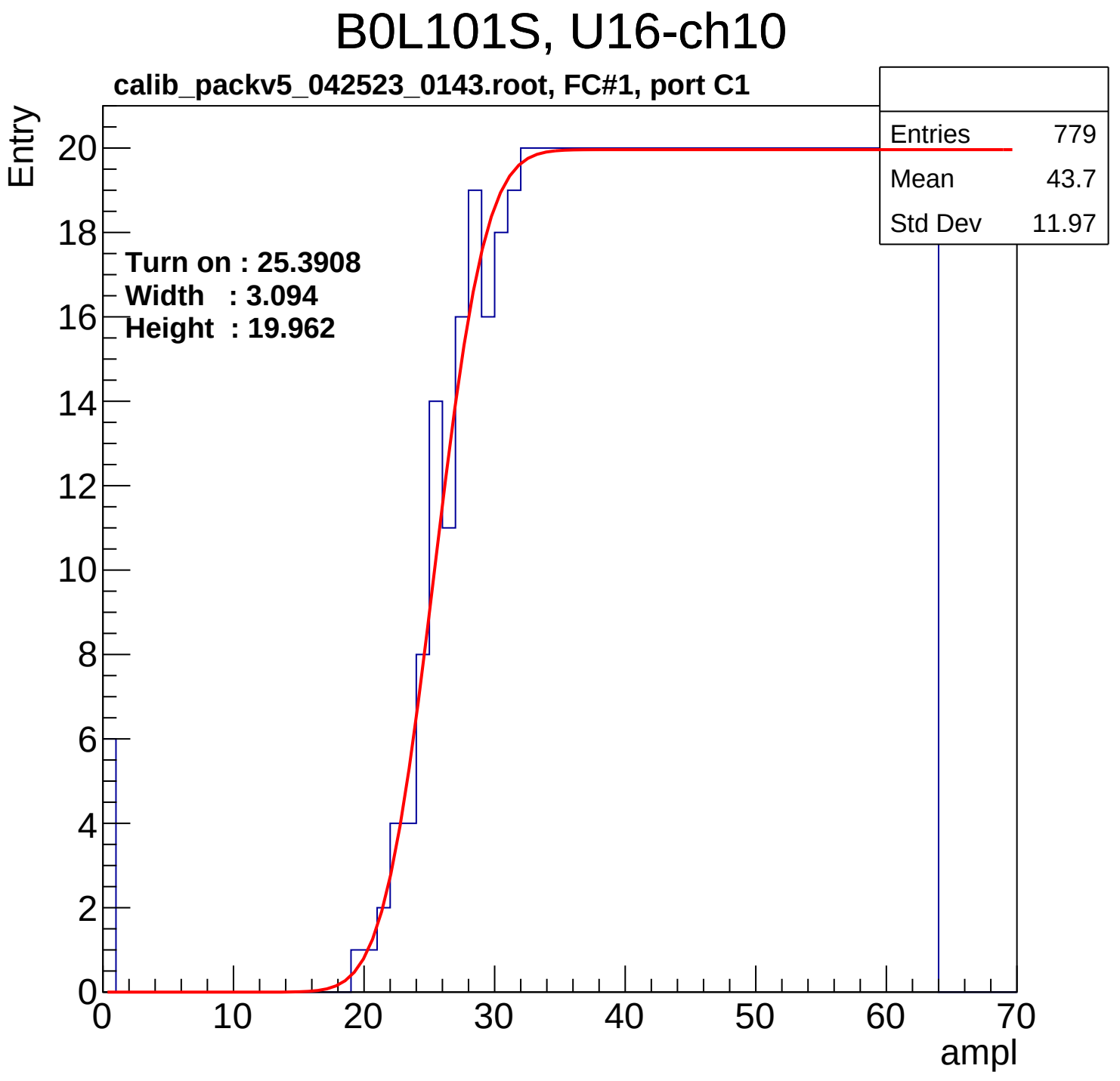
B0L101S, U16-ch10
calib_packv5_042523_0143.root, FC#1, port C1
Entries 779
Mean 43.7
Std Dev 11.97
Turn on : 25.3908
Width : 3.094
Height : 19.962
Entry
ampl
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6
8
10
12
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16
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0
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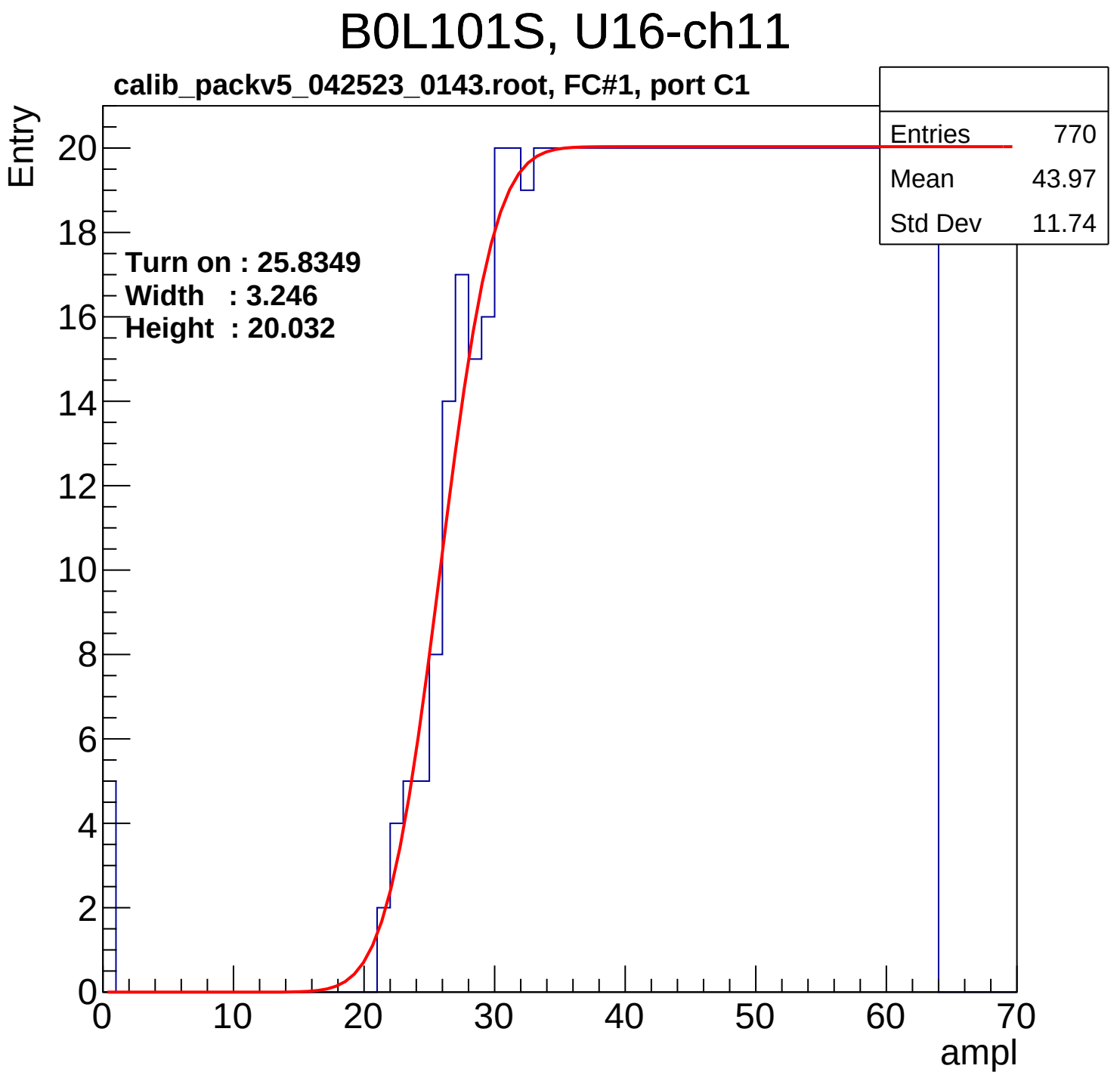
B0L101S, U16-ch11
calib_packv5_042523_0143.root, FC#1, port C1
Entries 770
Mean 43.97
Std Dev 11.74
Turn on : 25.8349
Width : 3.246
Height : 20.032
Entry
ampl
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6
8
10
12
14
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18
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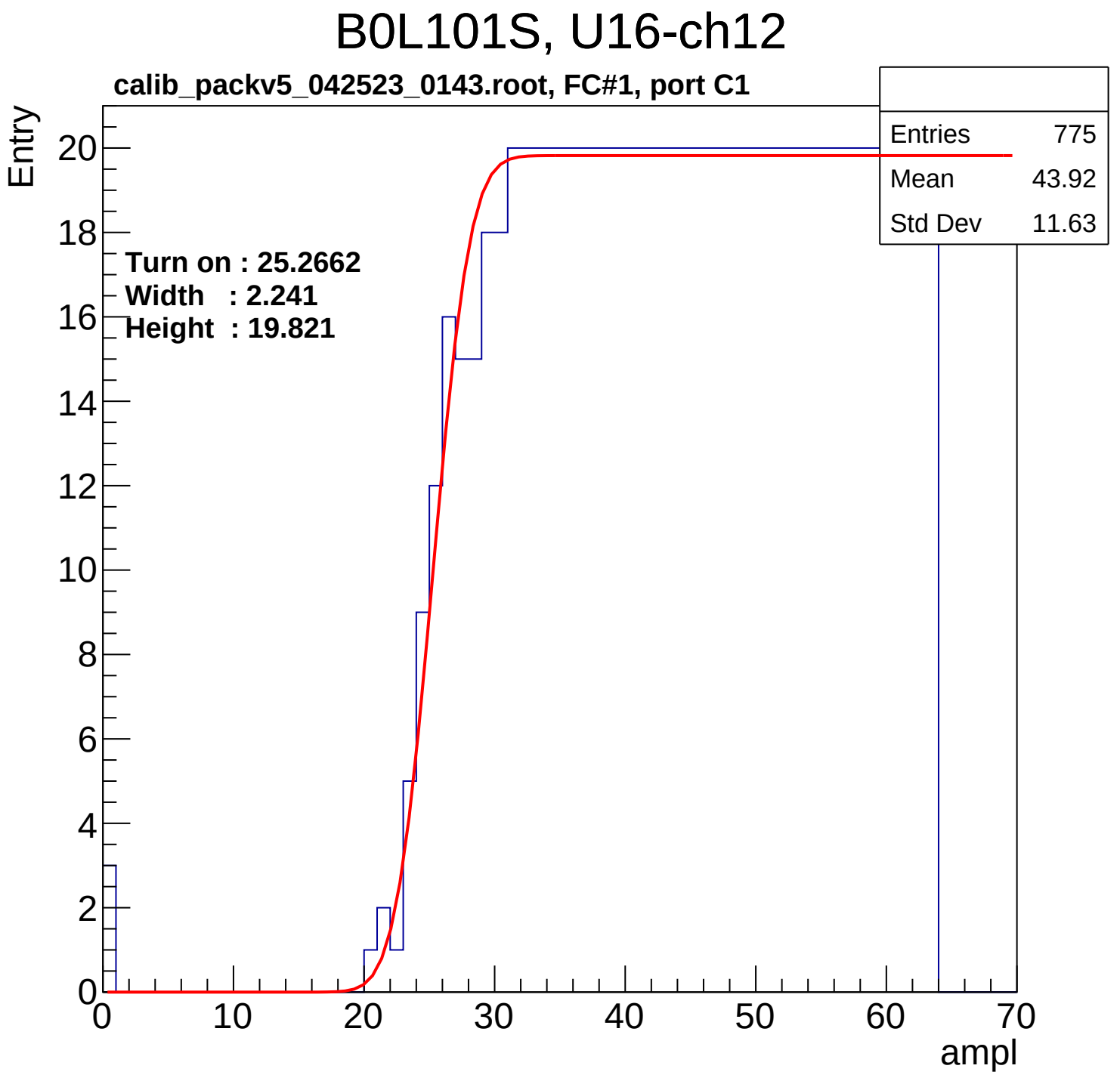
B0L101S, U16-ch12
calib_packv5_042523_0143.root, FC#1, port C1
Entries 775
Mean 43.92
Std Dev 11.63
Turn on : 25.2662
Width : 2.241
Height : 19.821
Entry
ampl
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6
8
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0
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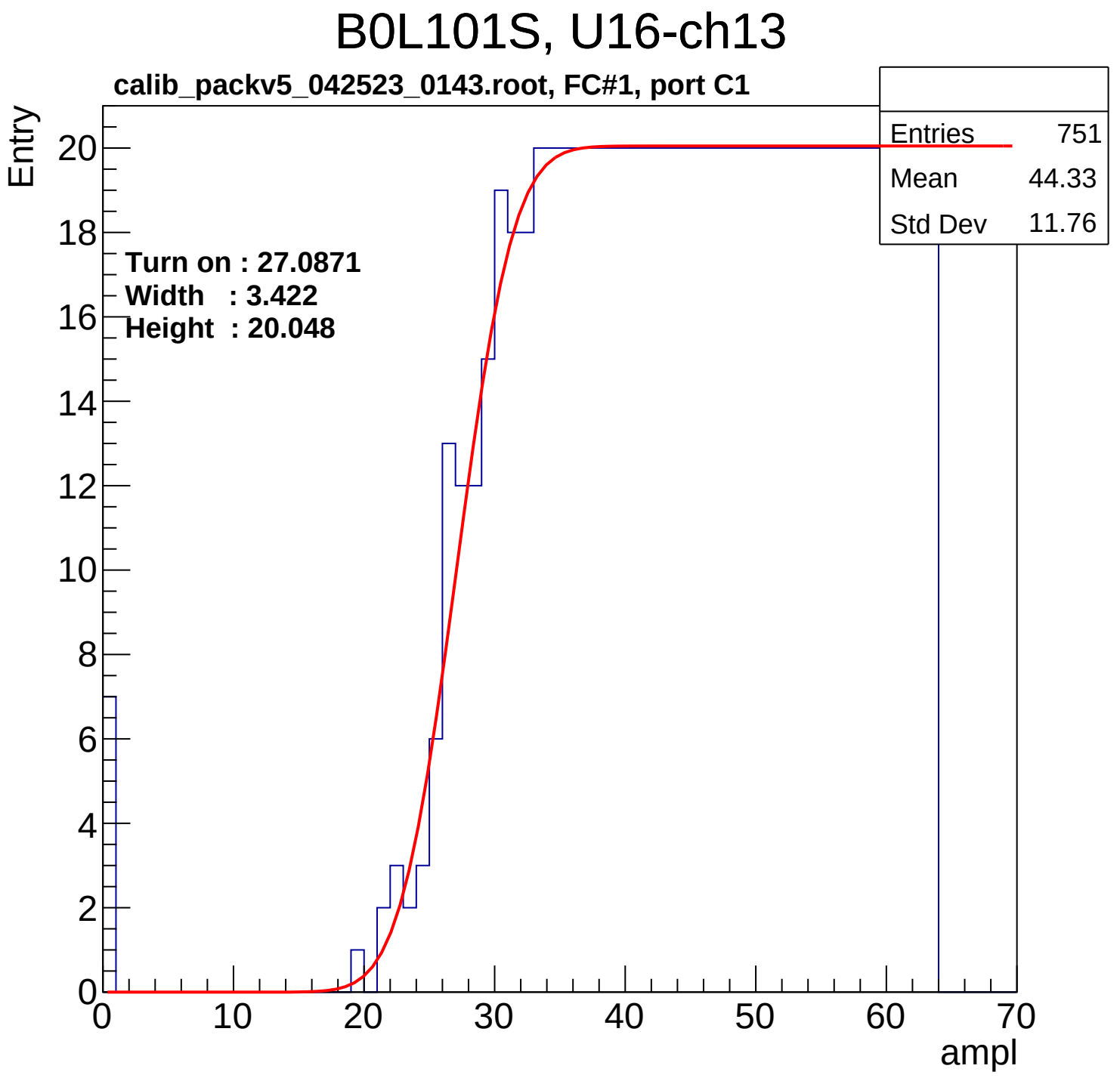
B0L101S, U16-ch13
calib_packv5_042523_0143.root, FC#1, port C1
Entries 751
Mean 44.33
Std Dev 11.76
Turn on : 27.0871
Width : 3.422
Height : 20.048
Entry
ampl
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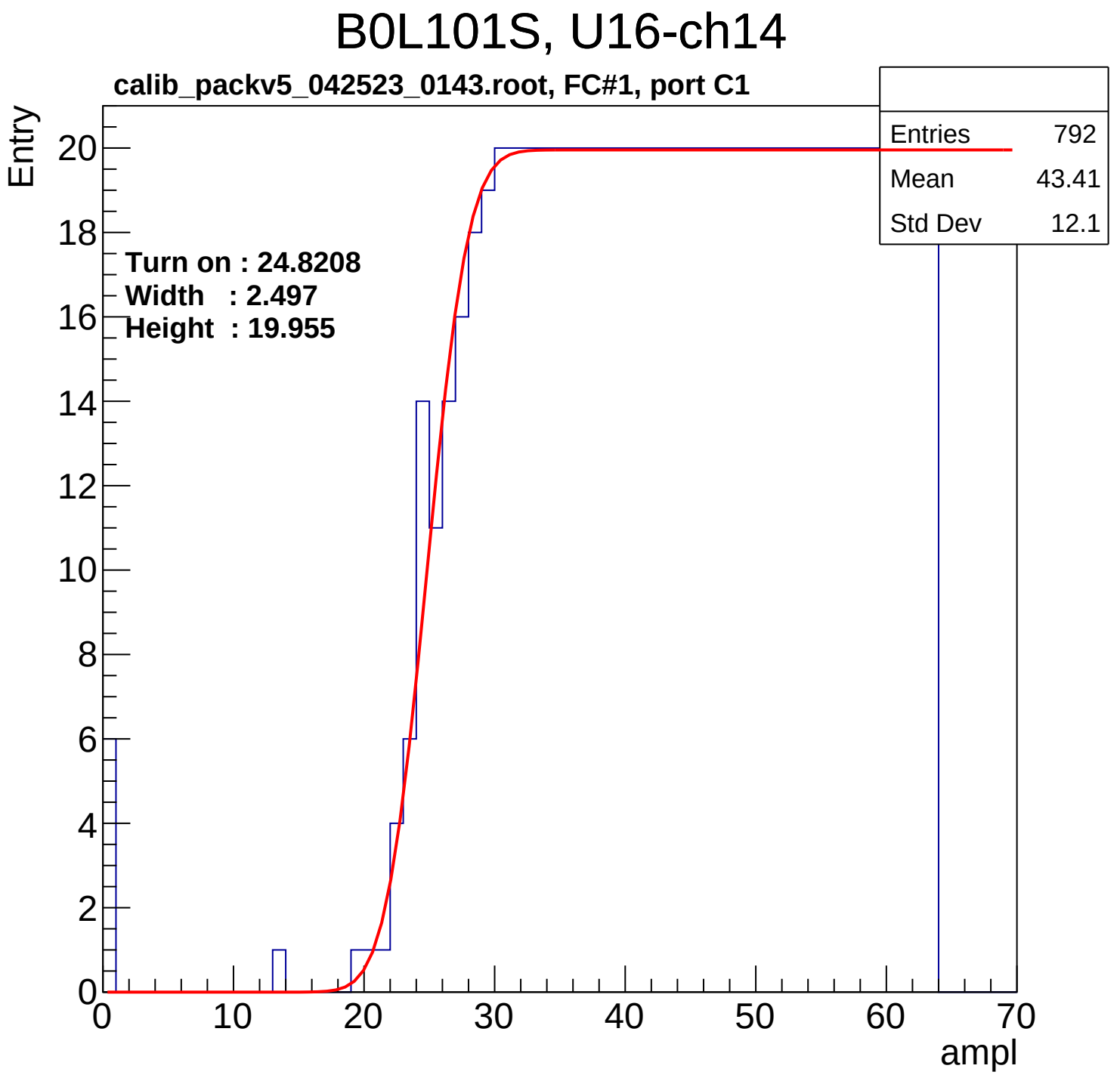
B0L101S, U16-ch14
calib_packv5_042523_0143.root, FC#1, port C1
Entries 792
Mean 43.41
Std Dev 12.1
Turn on : 24.8208
Width : 2.497
Height : 19.955
Entry
ampl
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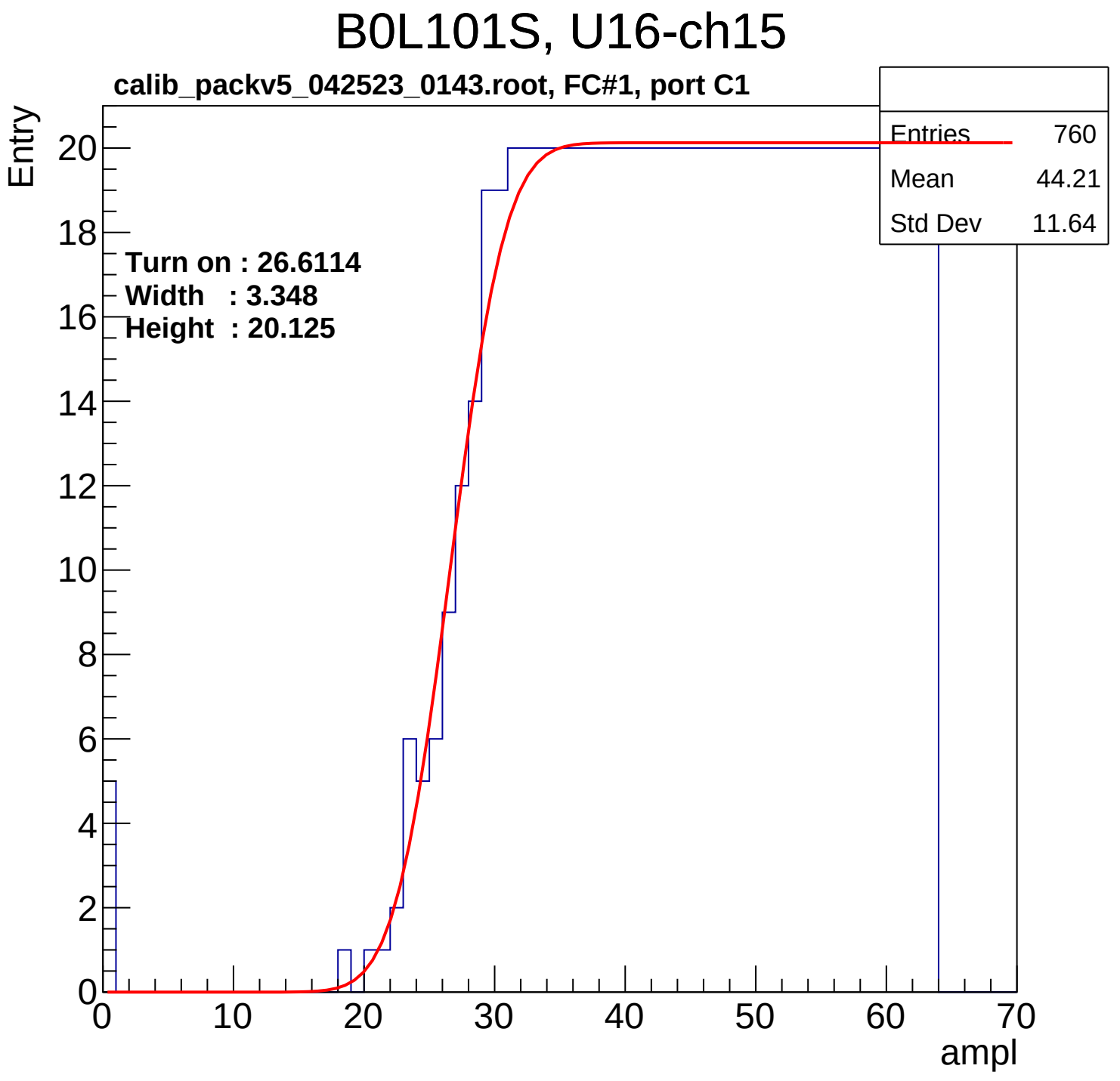
B0L101S, U16-ch15
calib_packv5_042523_0143.root, FC#1, port C1
Entries 760
Mean 44.21
Std Dev 11.64
Turn on : 26.6114
Width : 3.348
Height : 20.125
Entry
ampl
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8
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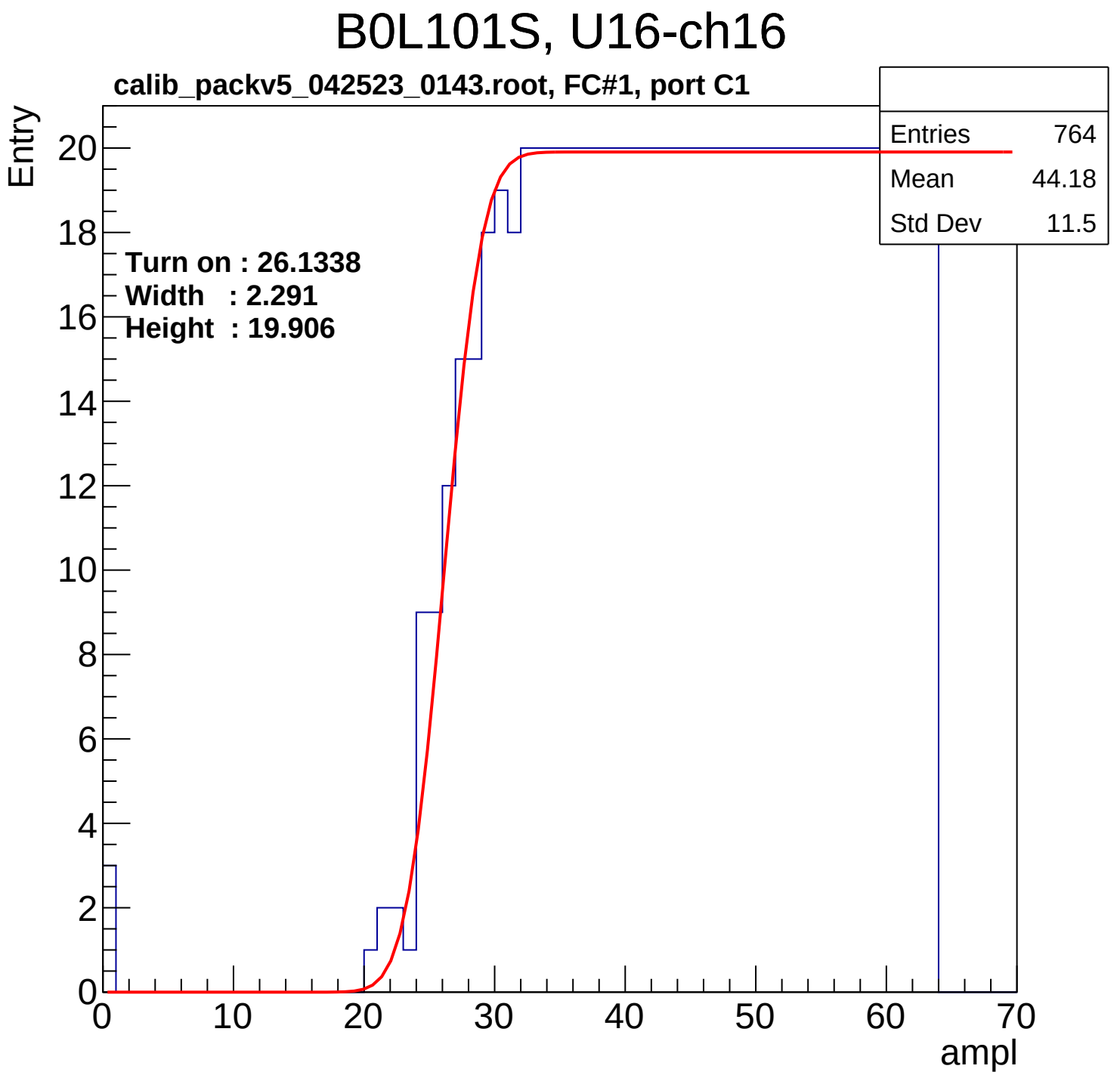
B0L101S, U16-ch16
calib_packv5_042523_0143.root, FC#1, port C1
Entries 764
Mean 44.18
Std Dev 11.5
Turn on : 26.1338
Width : 2.291
Height : 19.906
Entry
ampl
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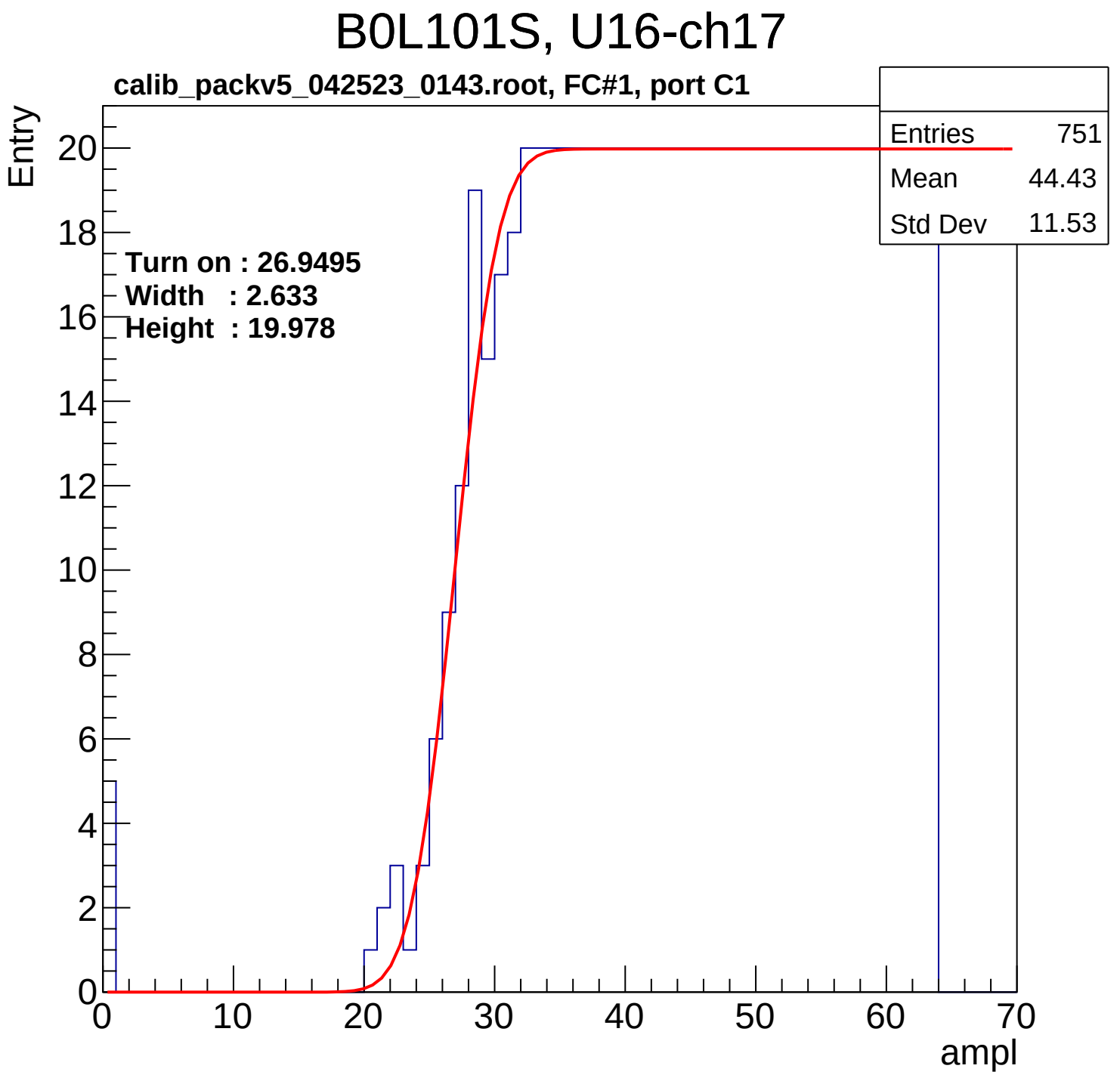
B0L101S, U16-ch17
calib_packv5_042523_0143.root, FC#1, port C1
Entries 751
Mean 44.43
Std Dev 11.53
Turn on : 26.9495
Width : 2.633
Height : 19.978
Entry
ampl
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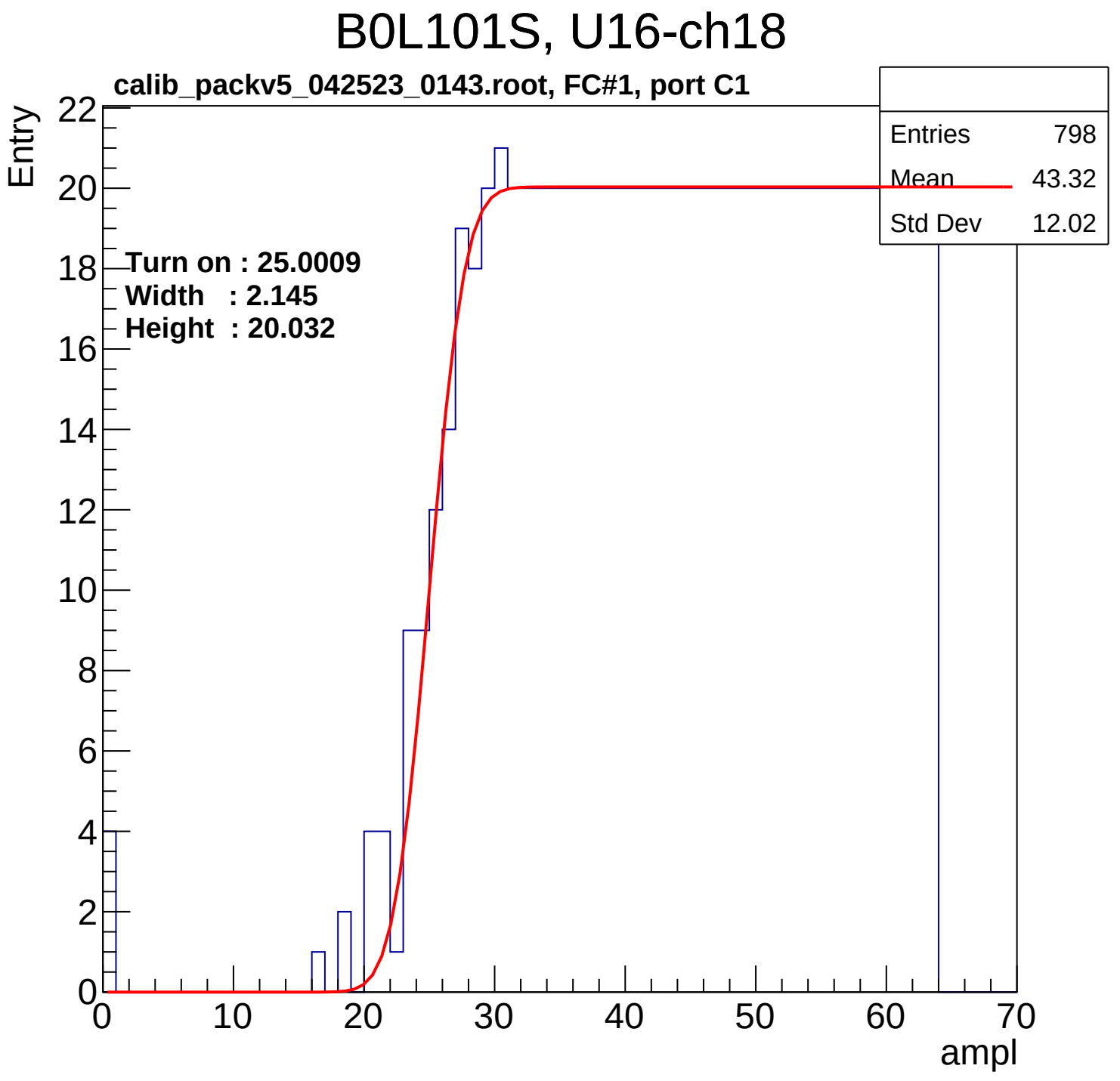
B0L101S, U16-ch18
calib_packv5_042523_0143.root, FC#1, port C1
Entries 798
Mean 43.32
Std Dev 12.02
Turn on : 25.0009
Width : 2.145
Height : 20.032
Entry
ampl
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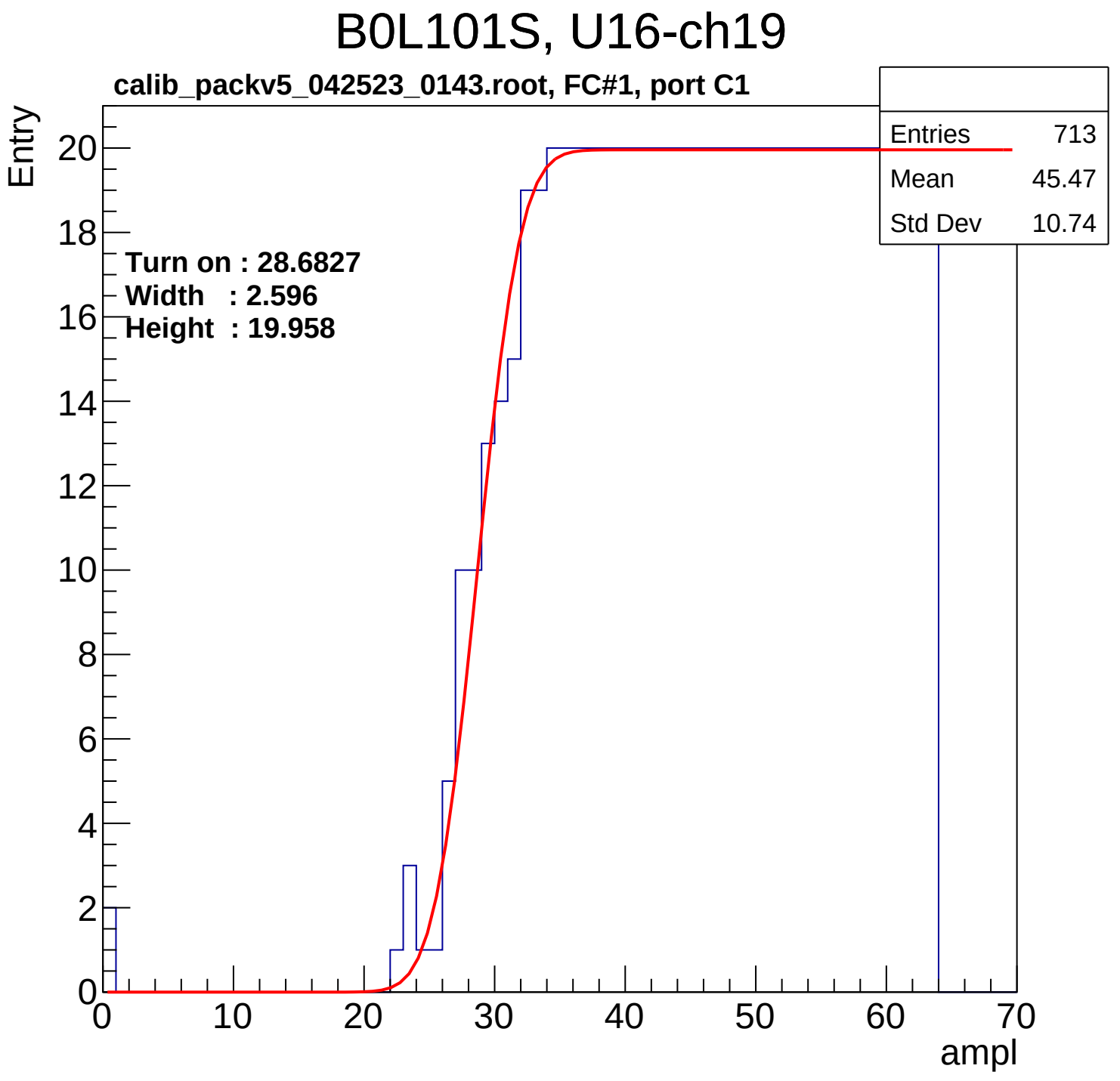
B0L101S, U16-ch19
calib_packv5_042523_0143.root, FC#1, port C1
Entries 713
Mean 45.47
Std Dev 10.74
Turn on : 28.6827
Width : 2.596
Height : 19.958
Entry
ampl
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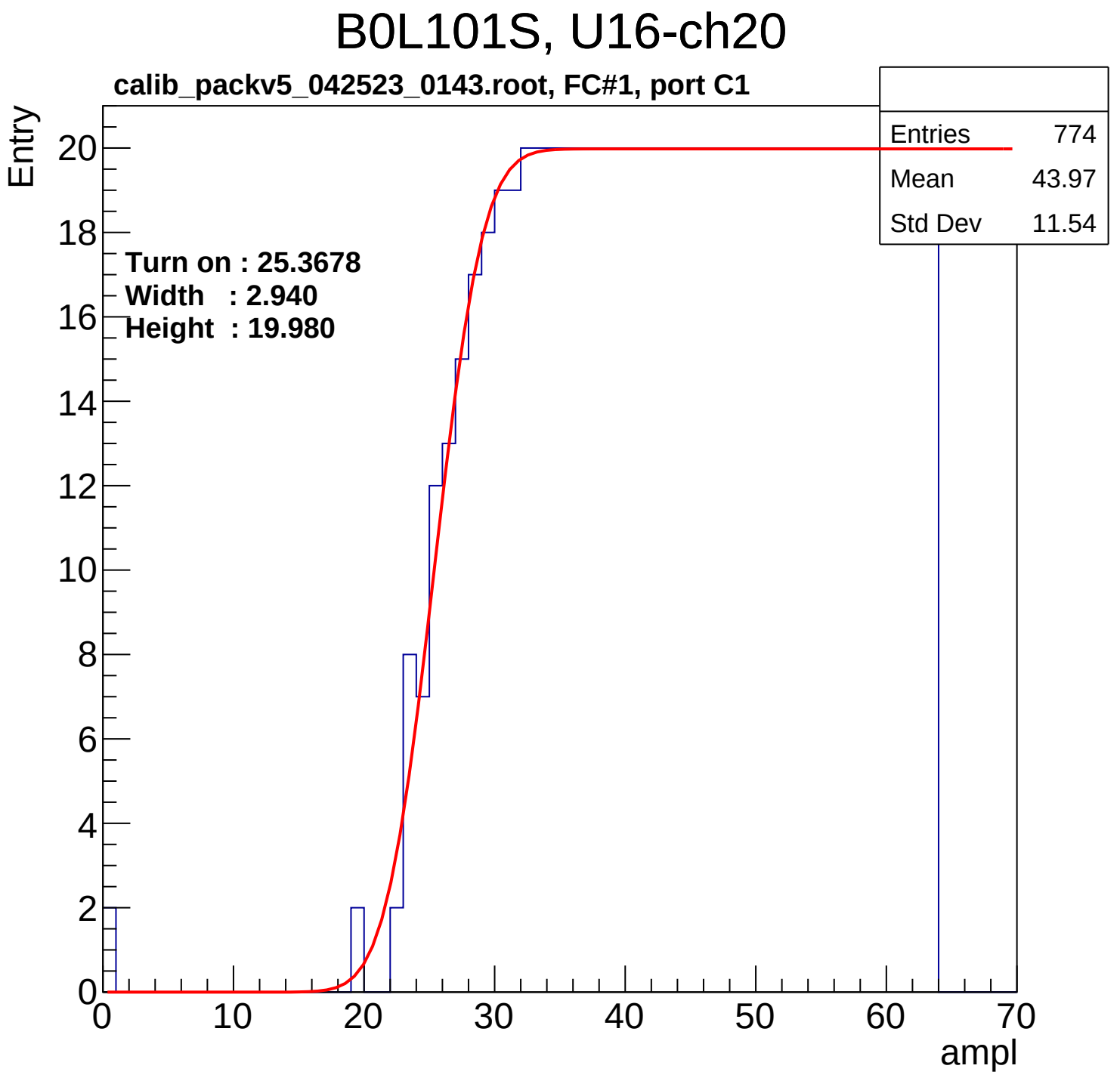
B0L101S, U16-ch20
calib_packv5_042523_0143.root, FC#1, port C1
Entries 774
Mean 43.97
Std Dev 11.54
Turn on : 25.3678
Width : 2.940
Height : 19.980
Entry
ampl
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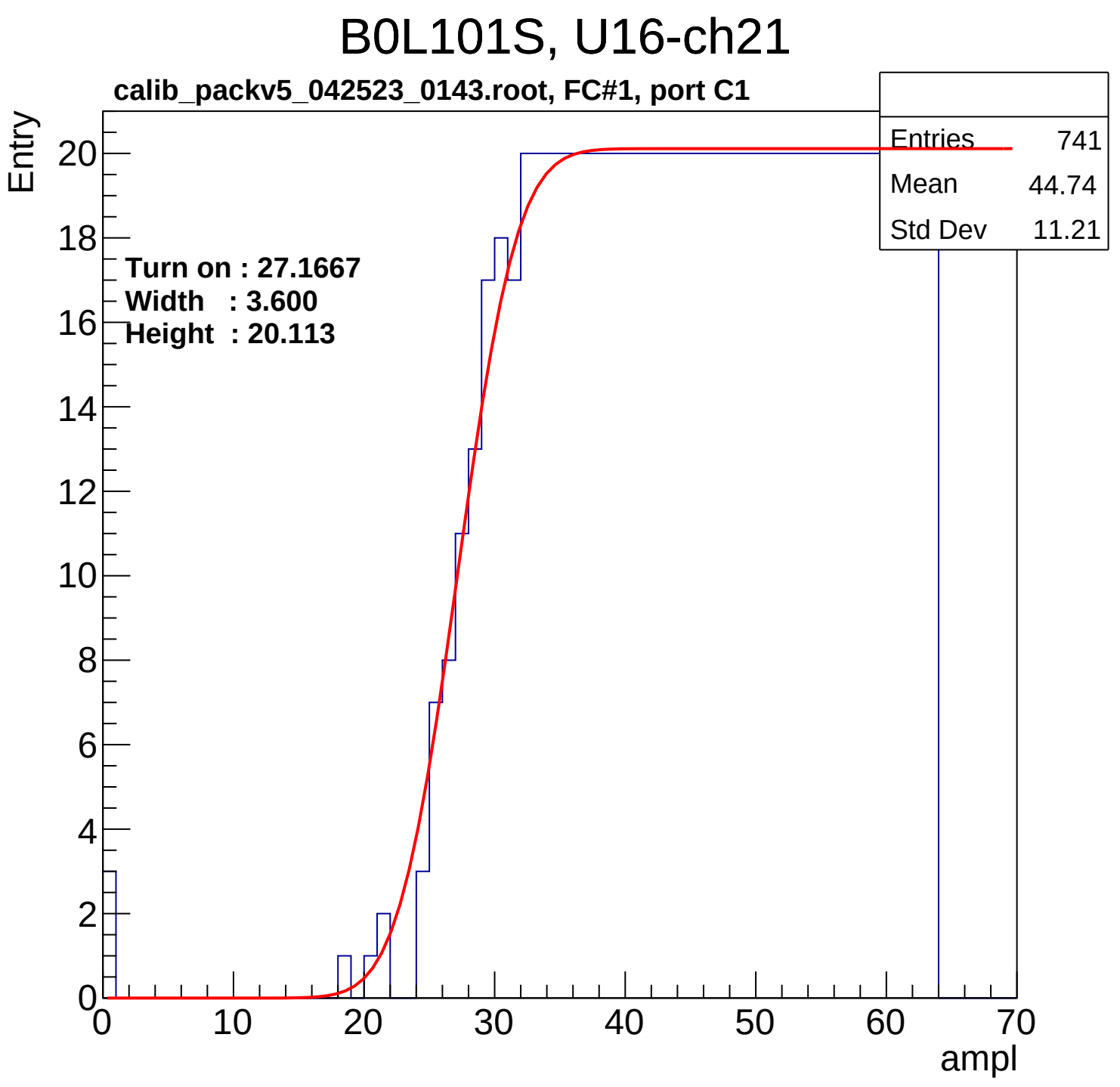
B0L101S, U16-ch21
calib_packv5_042523_0143.root, FC#1, port C1
Entries 741
Mean 44.74
Std Dev 11.21
Turn on : 27.1667
Width : 3.600
Height : 20.113
Entry
ampl
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6
8
10
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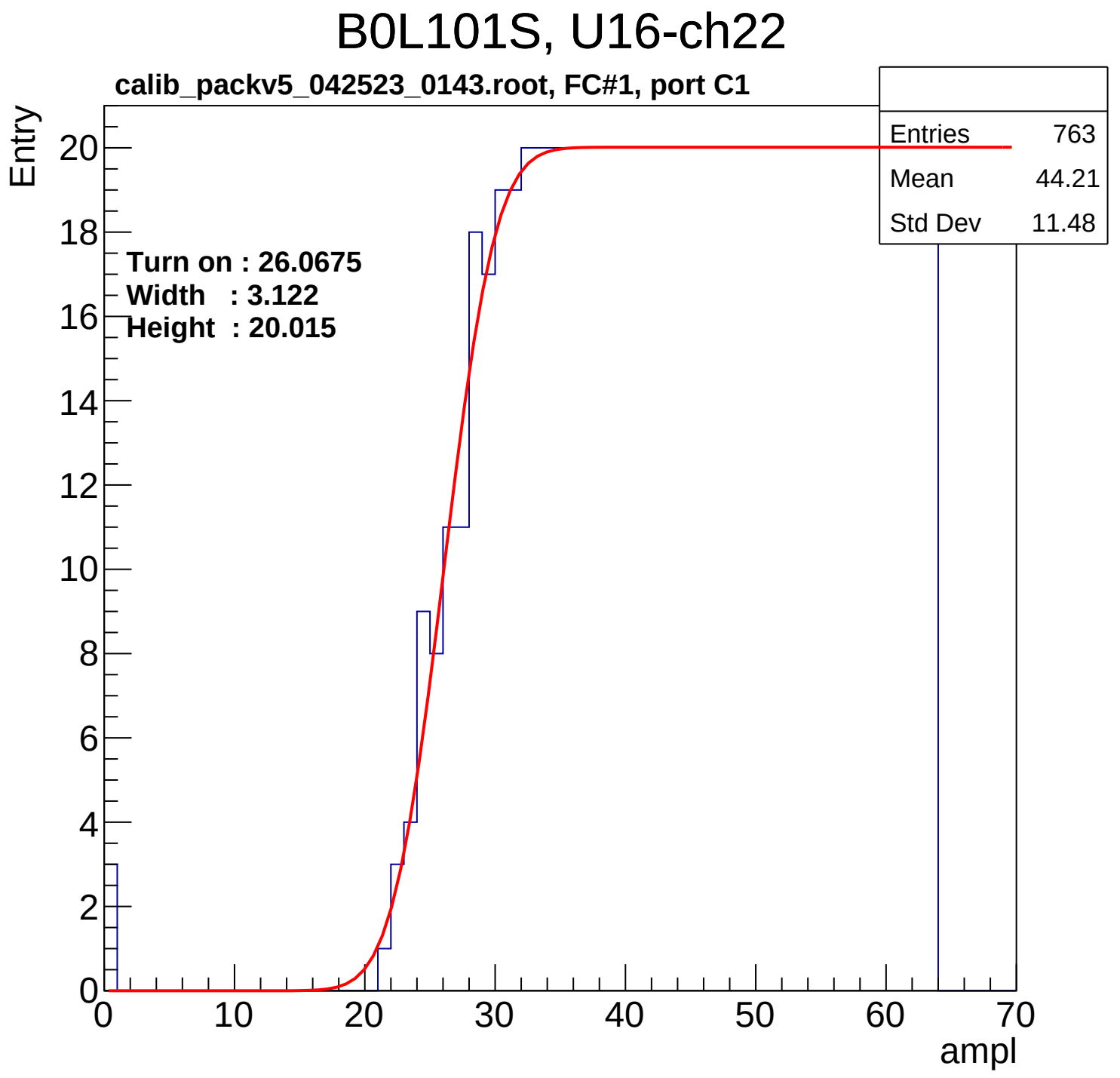
B0L101S, U16-ch22
calib_packv5_042523_0143.root, FC#1, port C1
Entries 763
Mean 44.21
Std Dev 11.48
Turn on : 26.0675
Width : 3.122
Height : 20.015
Entry
ampl
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6
8
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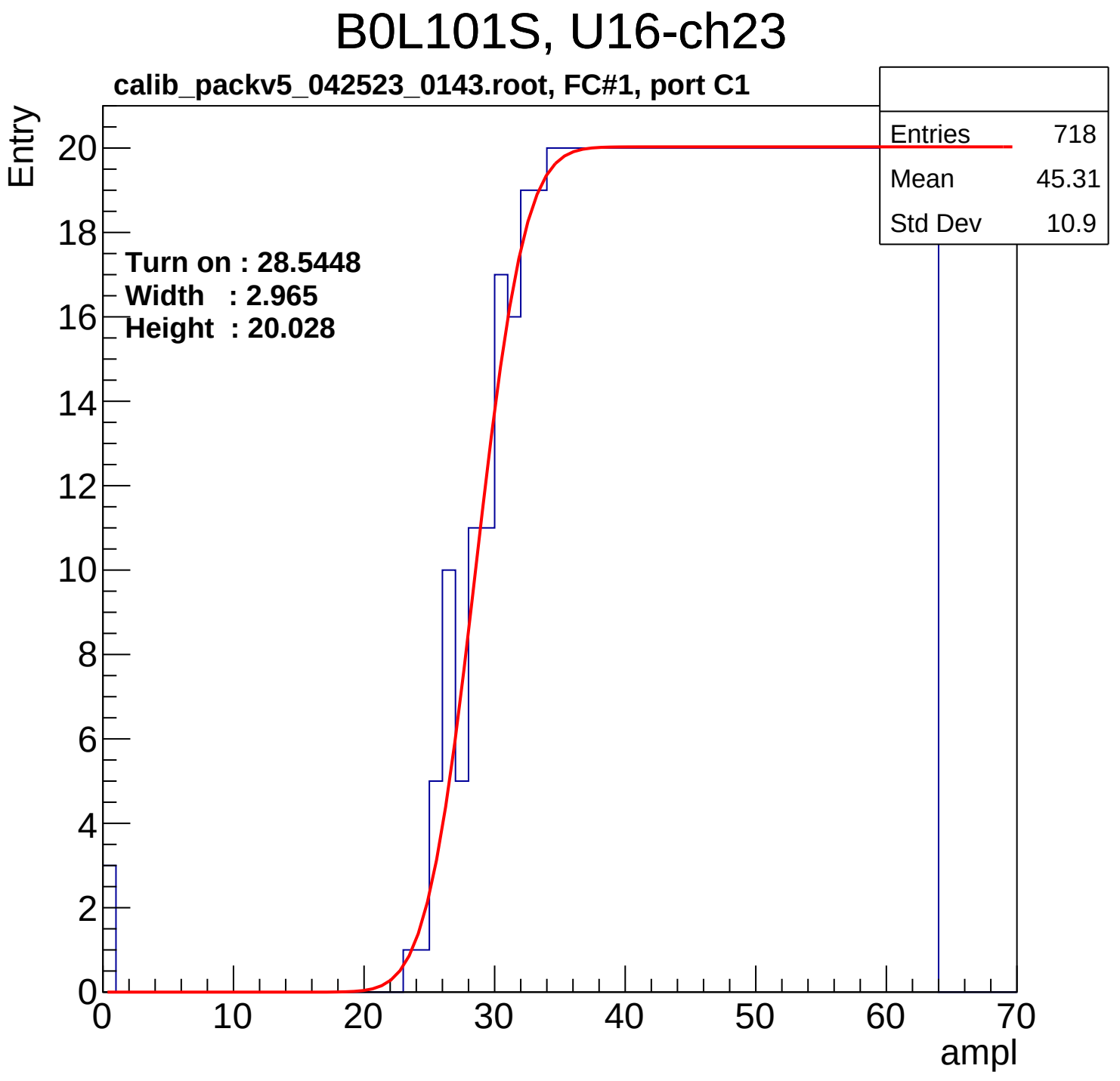
B0L101S, U16-ch23
calib_packv5_042523_0143.root, FC#1, port C1
Entries 718
Mean 45.31
Std Dev 10.9
Turn on : 28.5448
Width : 2.965
Height : 20.028
Entry
ampl
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8
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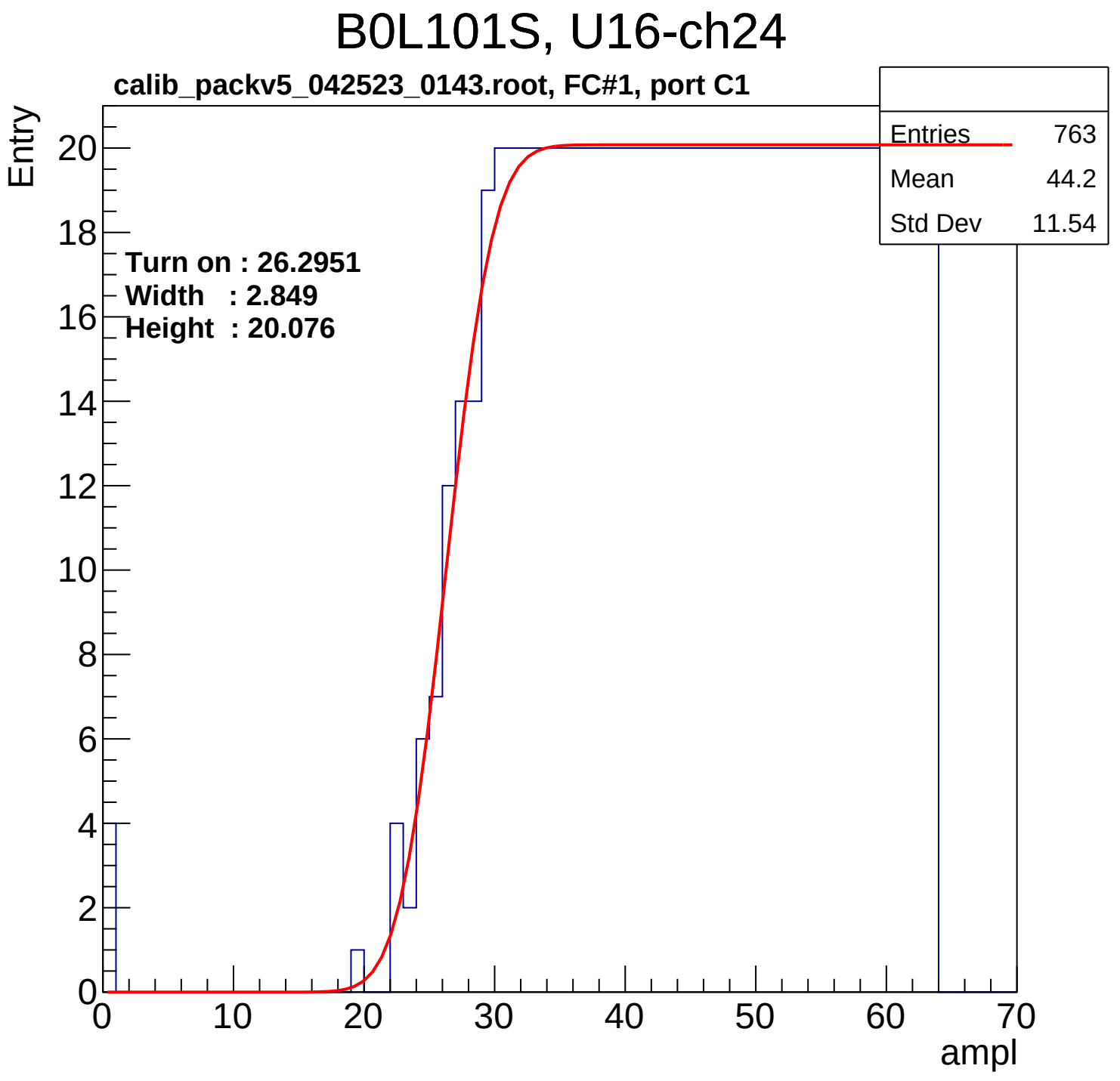
B0L101S, U16-ch24
calib_packv5_042523_0143.root, FC#1, port C1
Entries 763
Mean 44.2
Std Dev 11.54
Turn on : 26.2951
Width : 2.849
Height : 20.076
Entry
ampl
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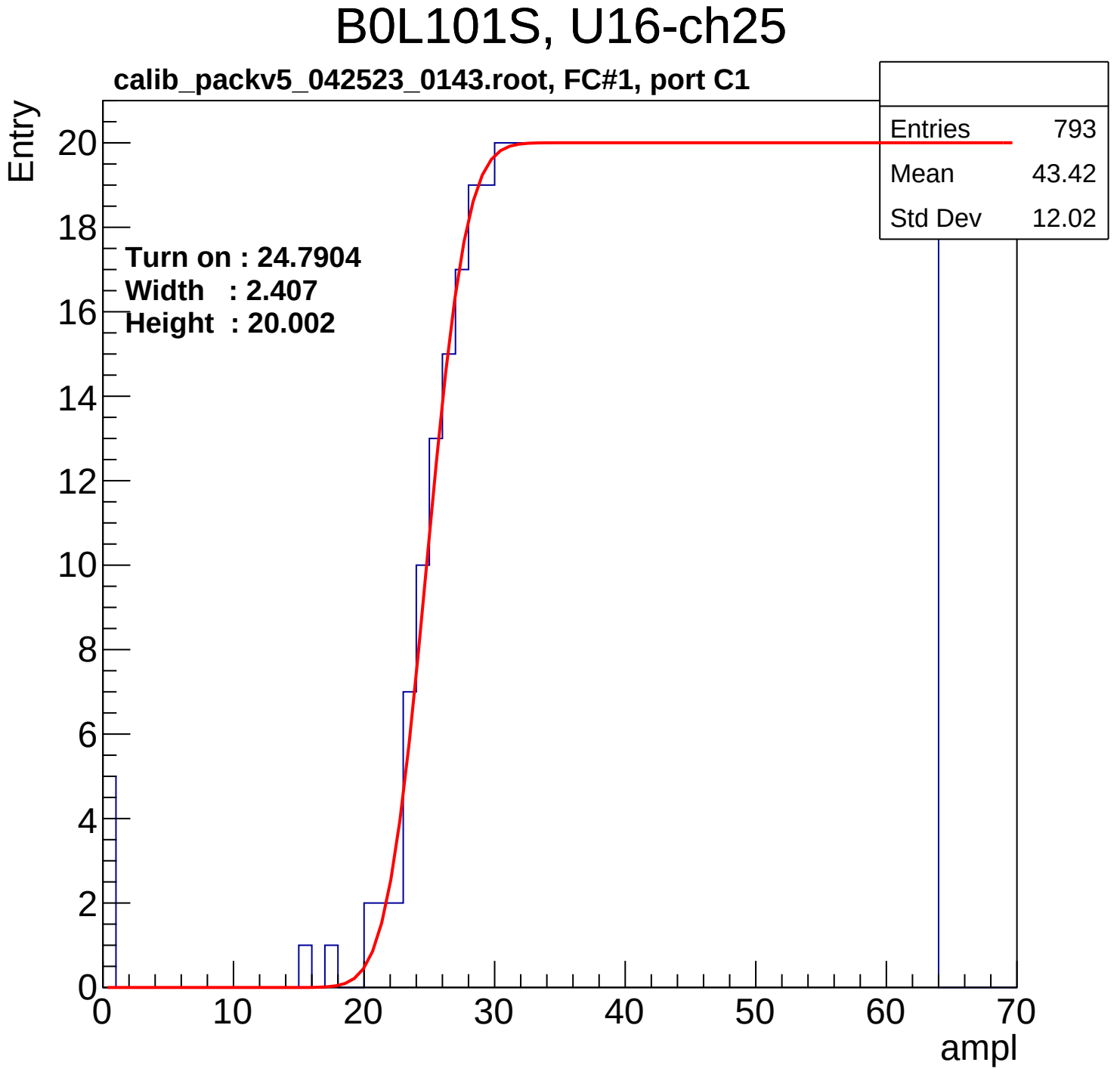
B0L101S, U16-ch25
calib_packv5_042523_0143.root, FC#1, port C1
Entries 793
Mean 43.42
Std Dev 12.02
Turn on : 24.7904
Width : 2.407
Height : 20.002
Entry
ampl
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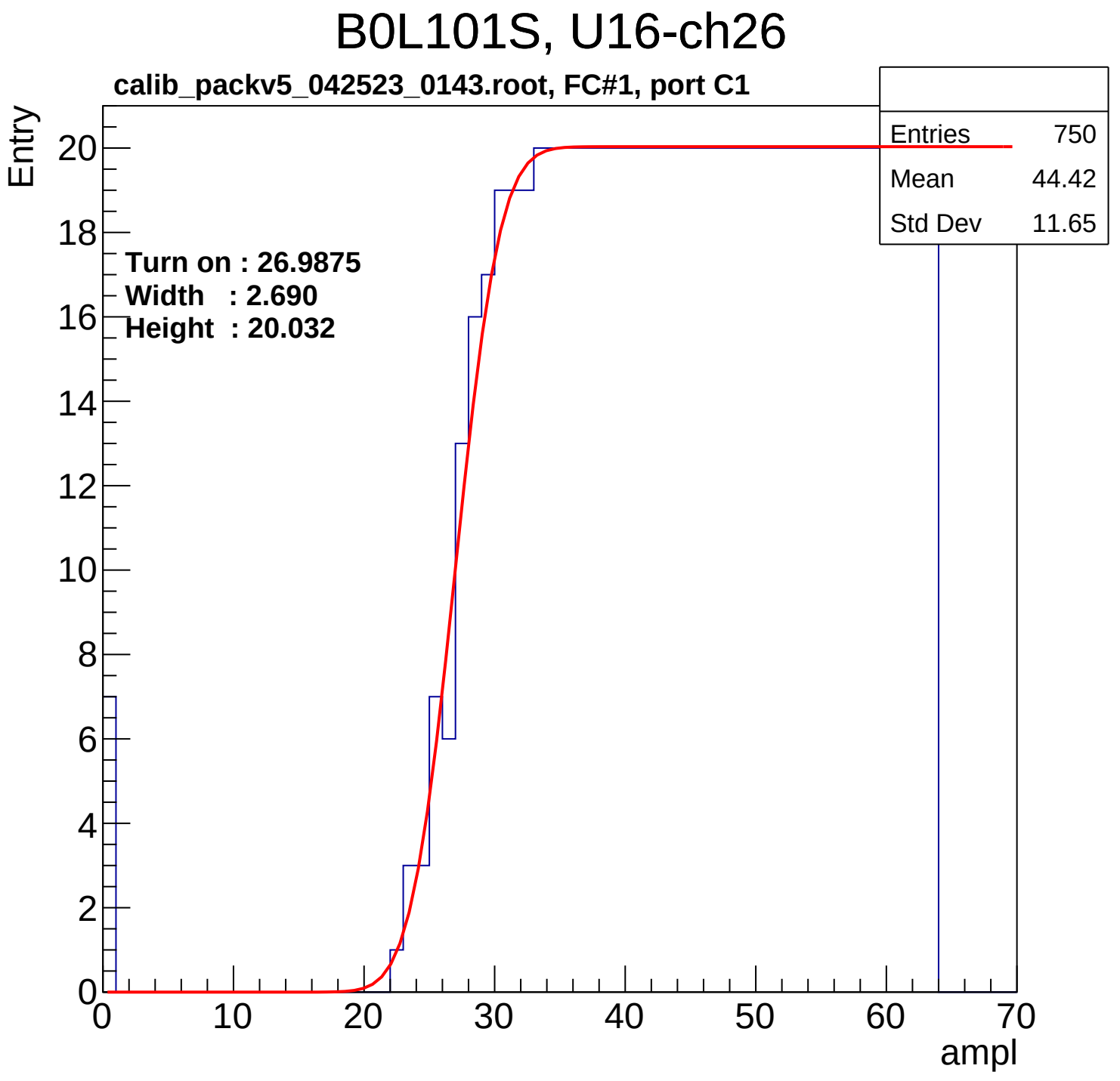
B0L101S, U16-ch26
calib_packv5_042523_0143.root, FC#1, port C1
Entries 750
Mean 44.42
Std Dev 11.65
Turn on : 26.9875
Width : 2.690
Height : 20.032
Entry
ampl
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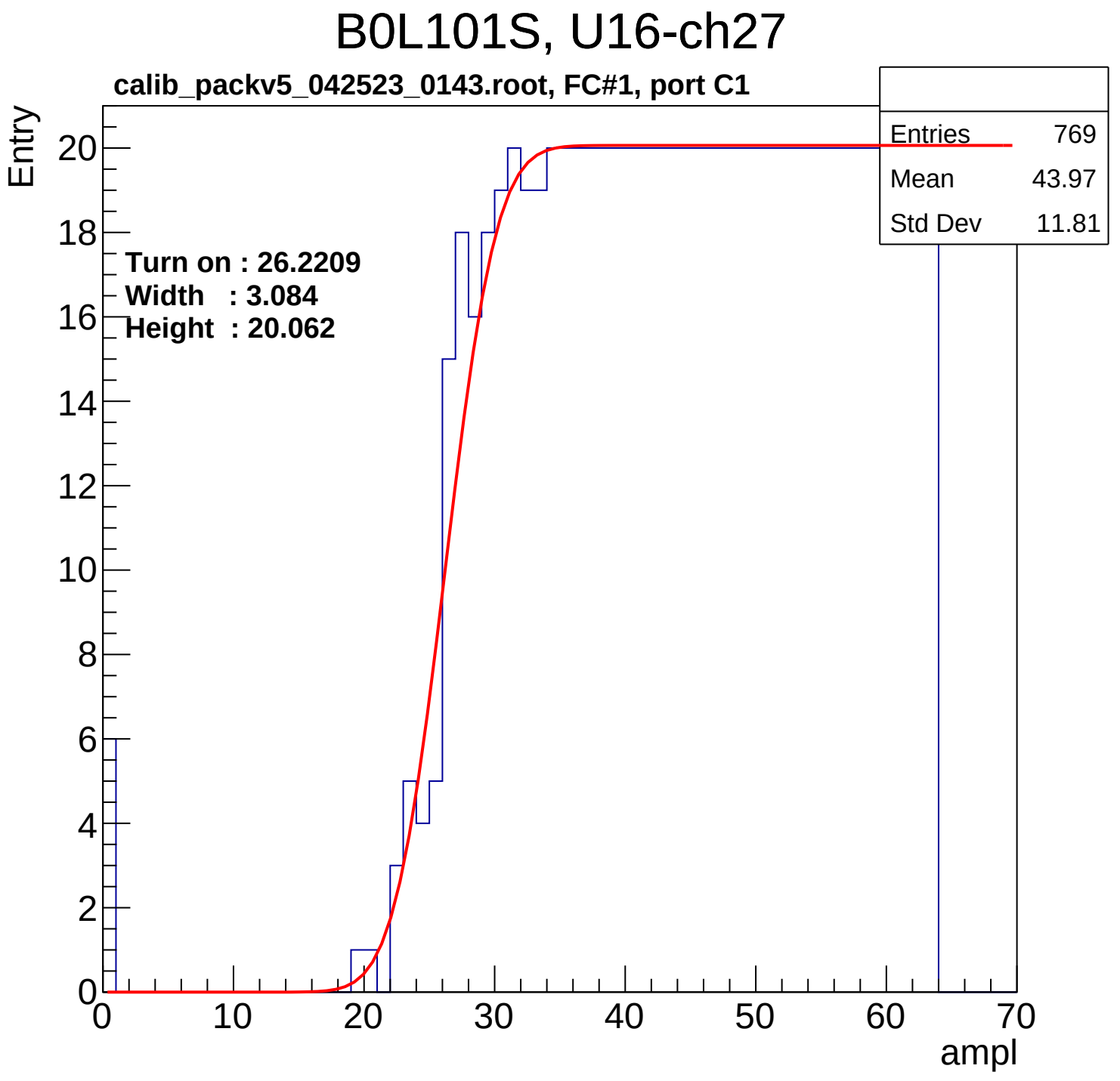
B0L101S, U16-ch27
calib_packv5_042523_0143.root, FC#1, port C1
Entries 769
Mean 43.97
Std Dev 11.81
Turn on : 26.2209
Width : 3.084
Height : 20.062
Entry
ampl
0
2
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6
8
10
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18
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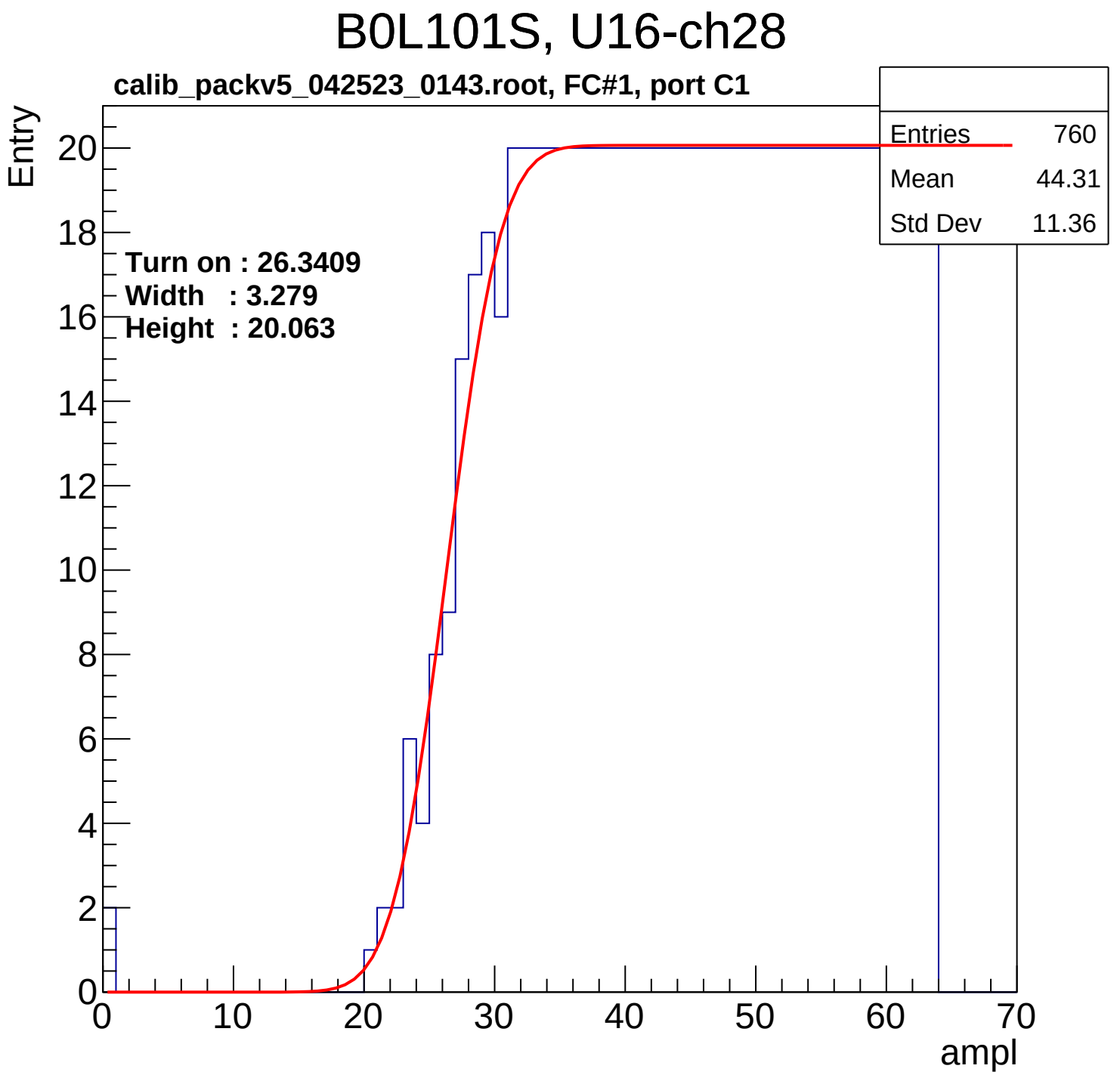
B0L101S, U16-ch28
calib_packv5_042523_0143.root, FC#1, port C1
Entries 760
Mean 44.31
Std Dev 11.36
Turn on : 26.3409
Width : 3.279
Height : 20.063
Entry
ampl
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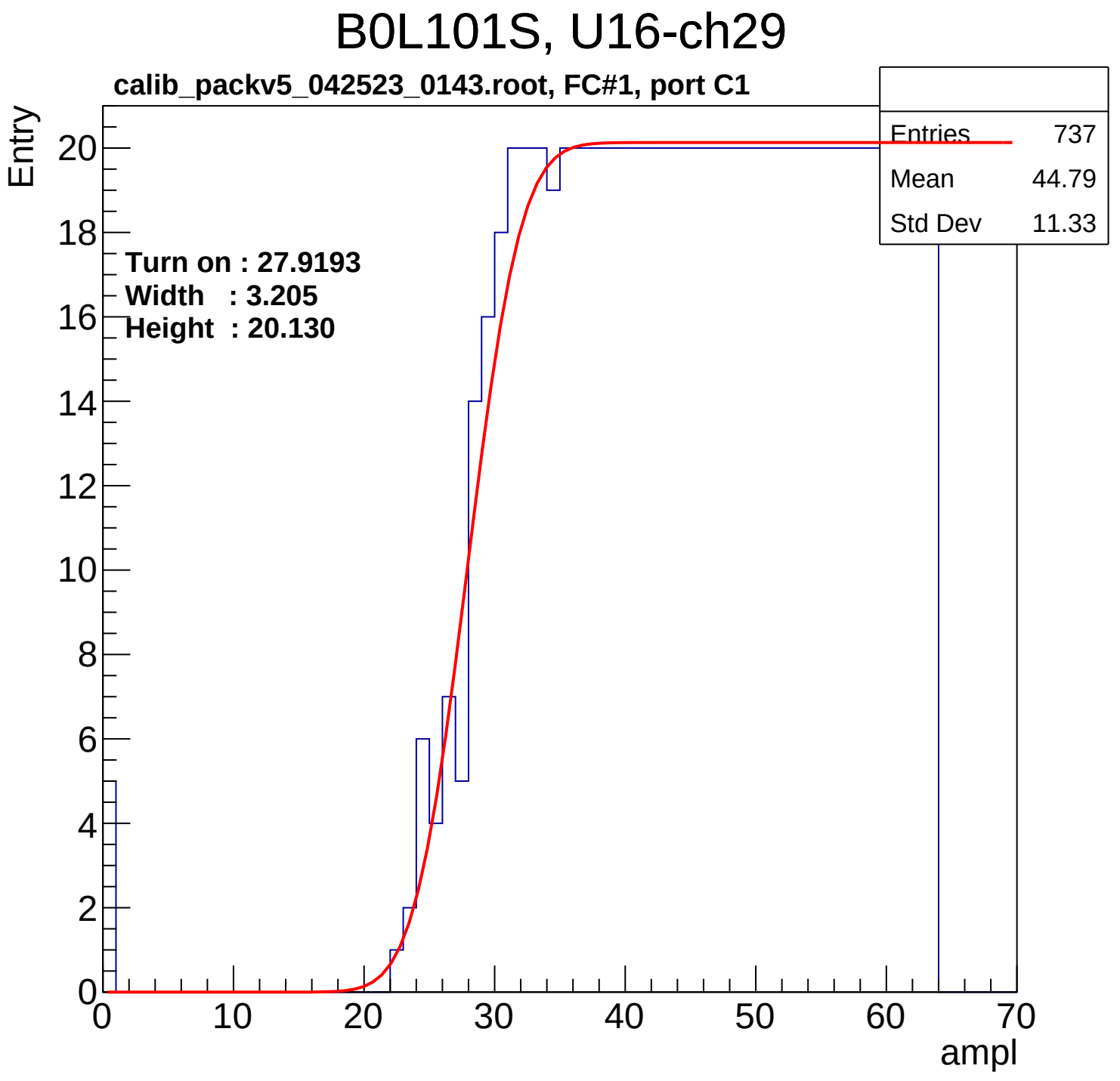
B0L101S, U16-ch29
calib_packv5_042523_0143.root, FC#1, port C1
Entries 737
Mean 44.79
Std Dev 11.33
Turn on : 27.9193
Width : 3.205
Height : 20.130
Entry
ampl
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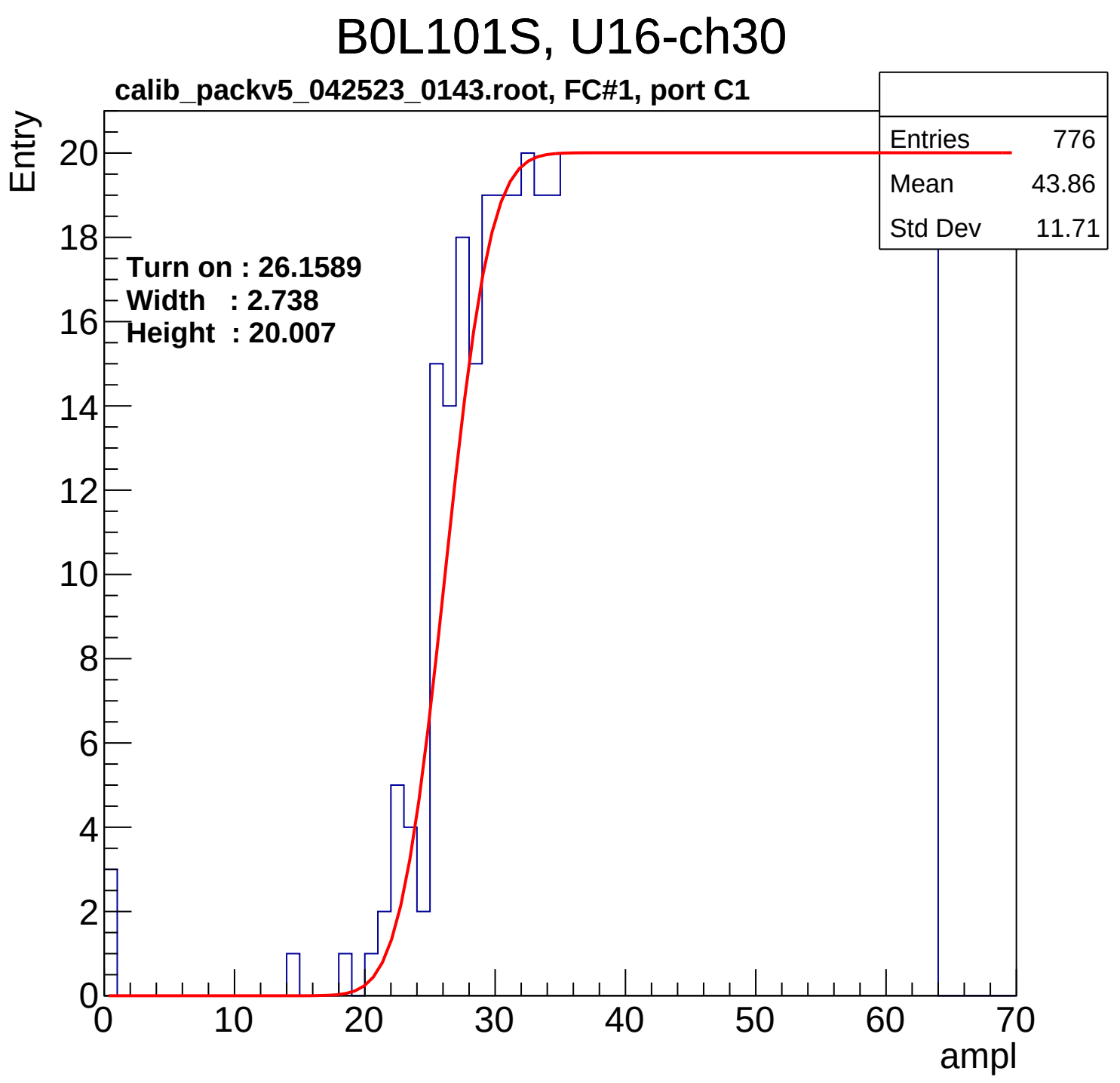
B0L101S, U16-ch30
calib_packv5_042523_0143.root, FC#1, port C1
Entries 776
Mean 43.86
Std Dev 11.71
Turn on : 26.1589
Width : 2.738
Height : 20.007
Entry
ampl
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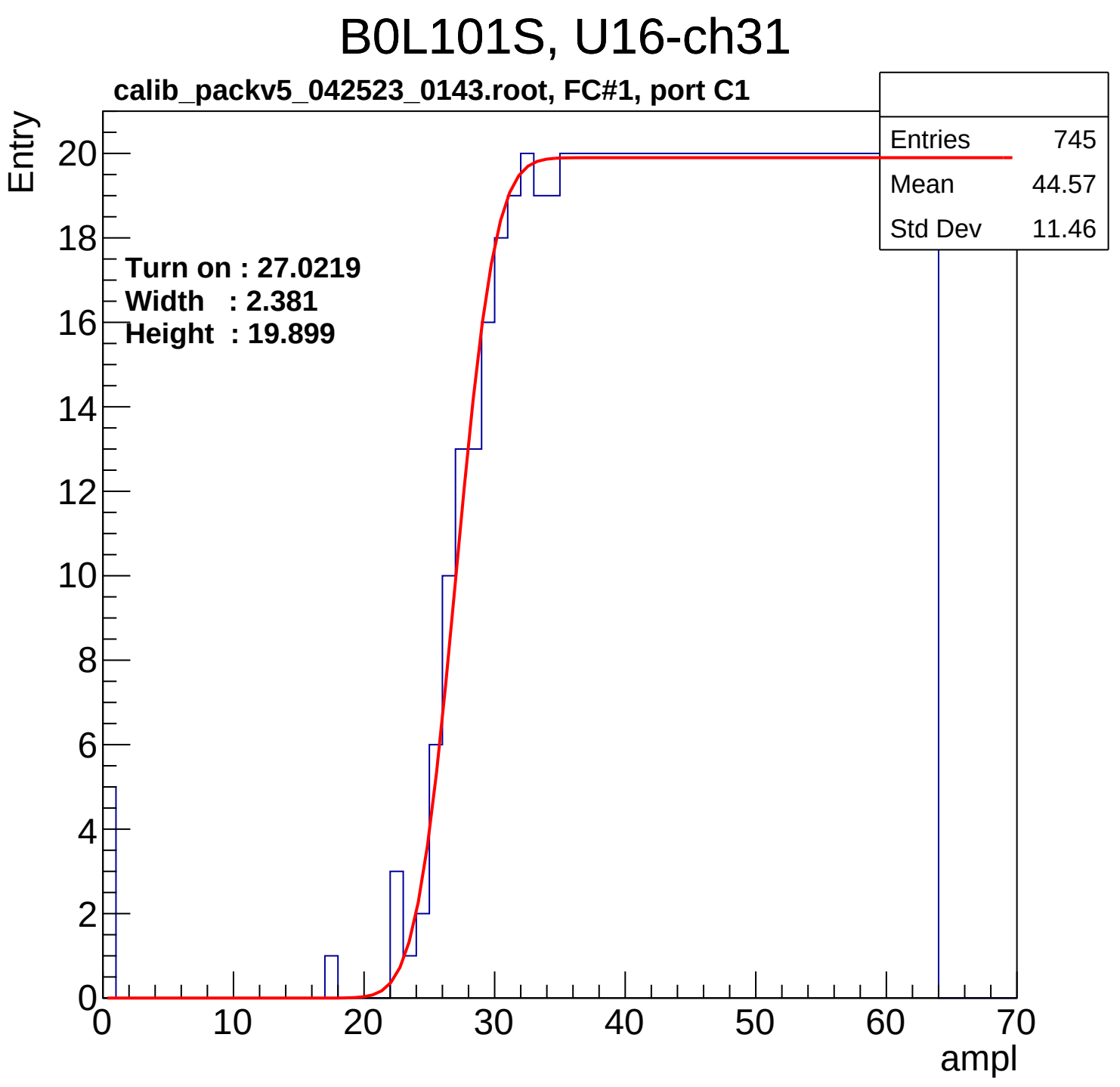
B0L101S, U16-ch31
calib_packv5_042523_0143.root, FC#1, port C1
Entries 745
Mean 44.57
Std Dev 11.46
Turn on : 27.0219
Width : 2.381
Height : 19.899
Entry
ampl
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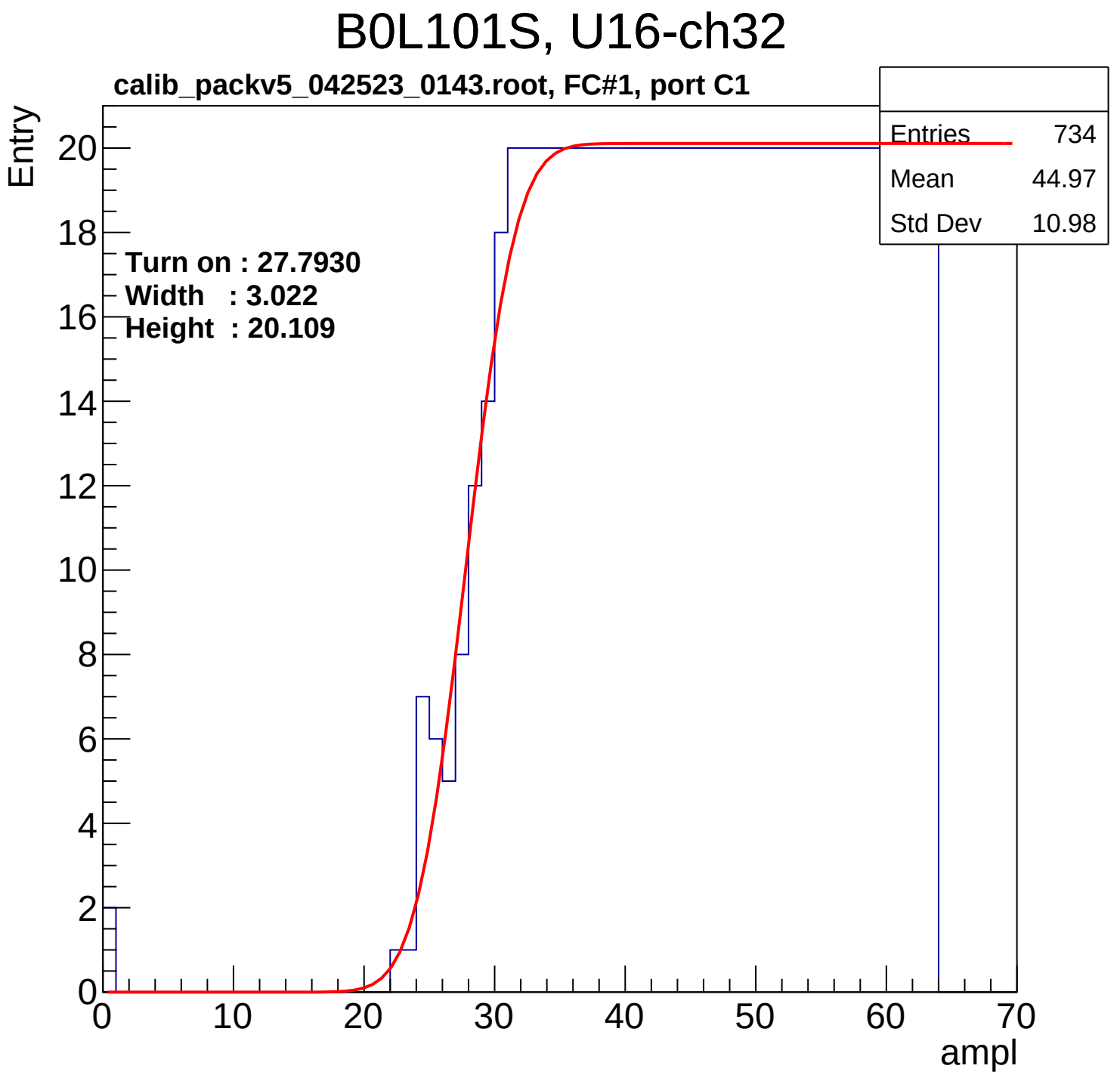
B0L101S, U16-ch32
calib_packv5_042523_0143.root, FC#1, port C1
Entries 734
Mean 44.97
Std Dev 10.98
Turn on : 27.7930
Width : 3.022
Height : 20.109
Entry
ampl
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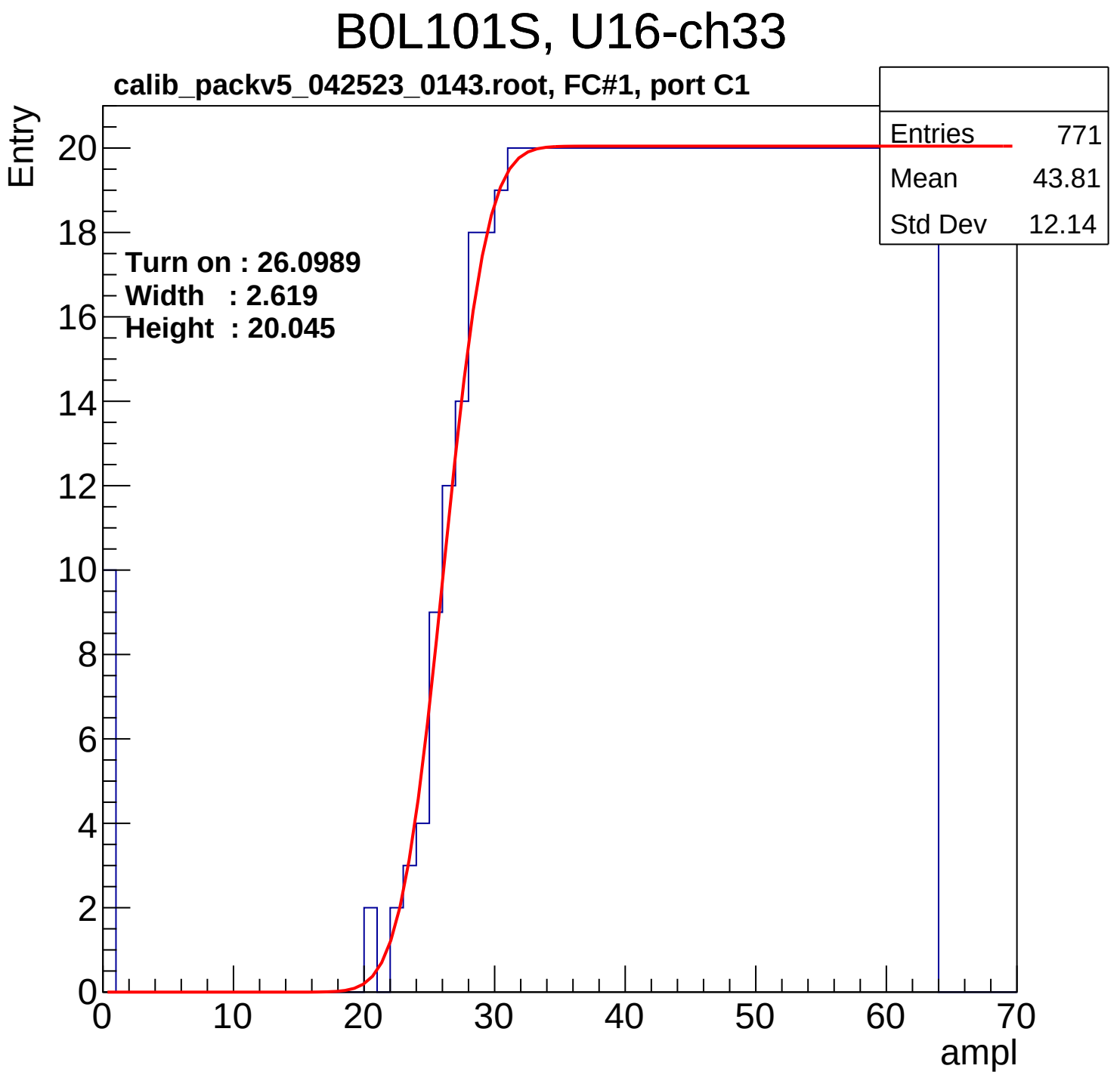
B0L101S, U16-ch33
calib_packv5_042523_0143.root, FC#1, port C1
Entries 771
Mean 43.81
Std Dev 12.14
Turn on : 26.0989
Width : 2.619
Height : 20.045
Entry
ampl
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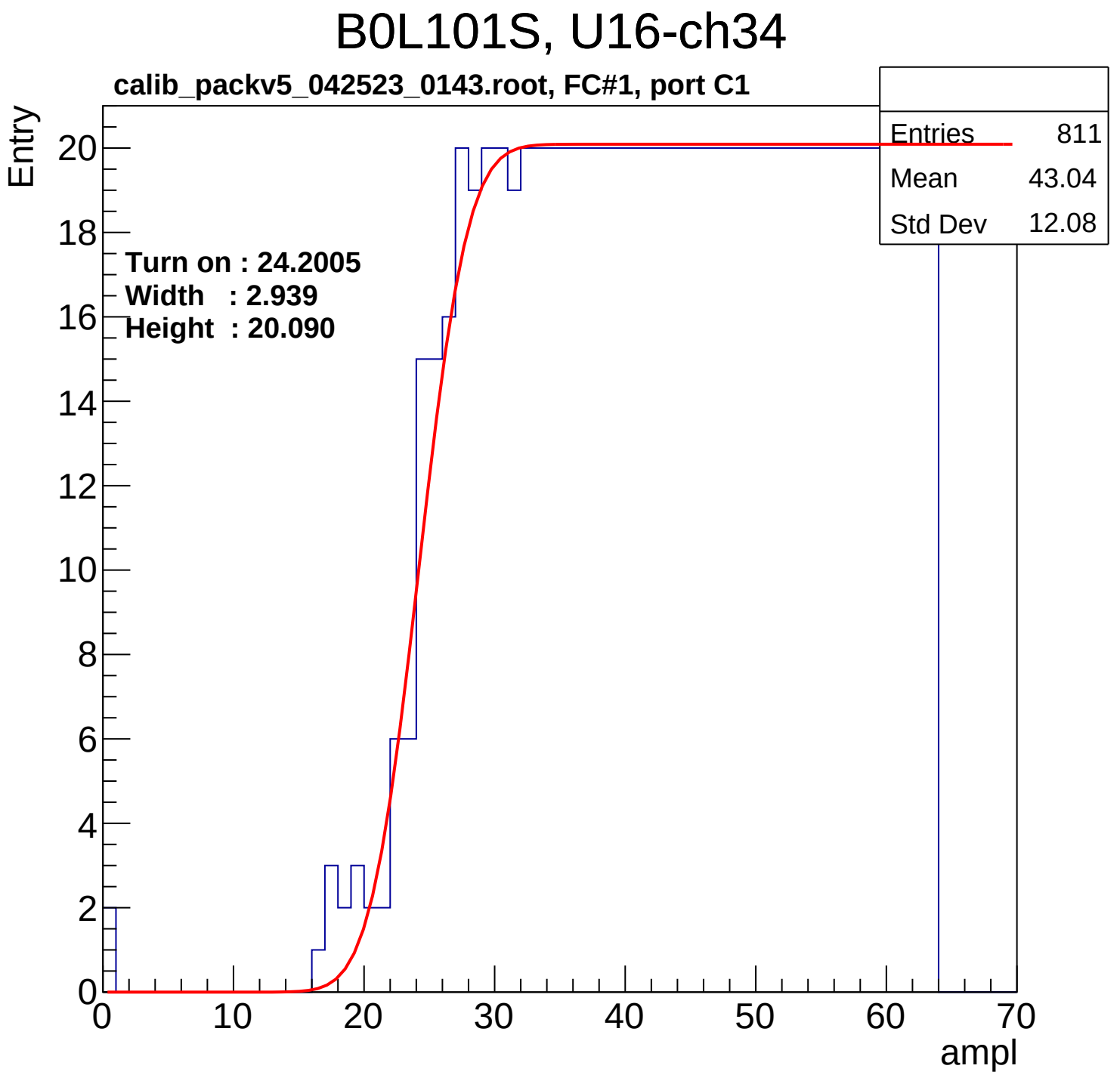
B0L101S, U16-ch34
calib_packv5_042523_0143.root, FC#1, port C1
Entries 811
Mean 43.04
Std Dev 12.08
Turn on : 24.2005
Width : 2.939
Height : 20.090
Entry
ampl
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12
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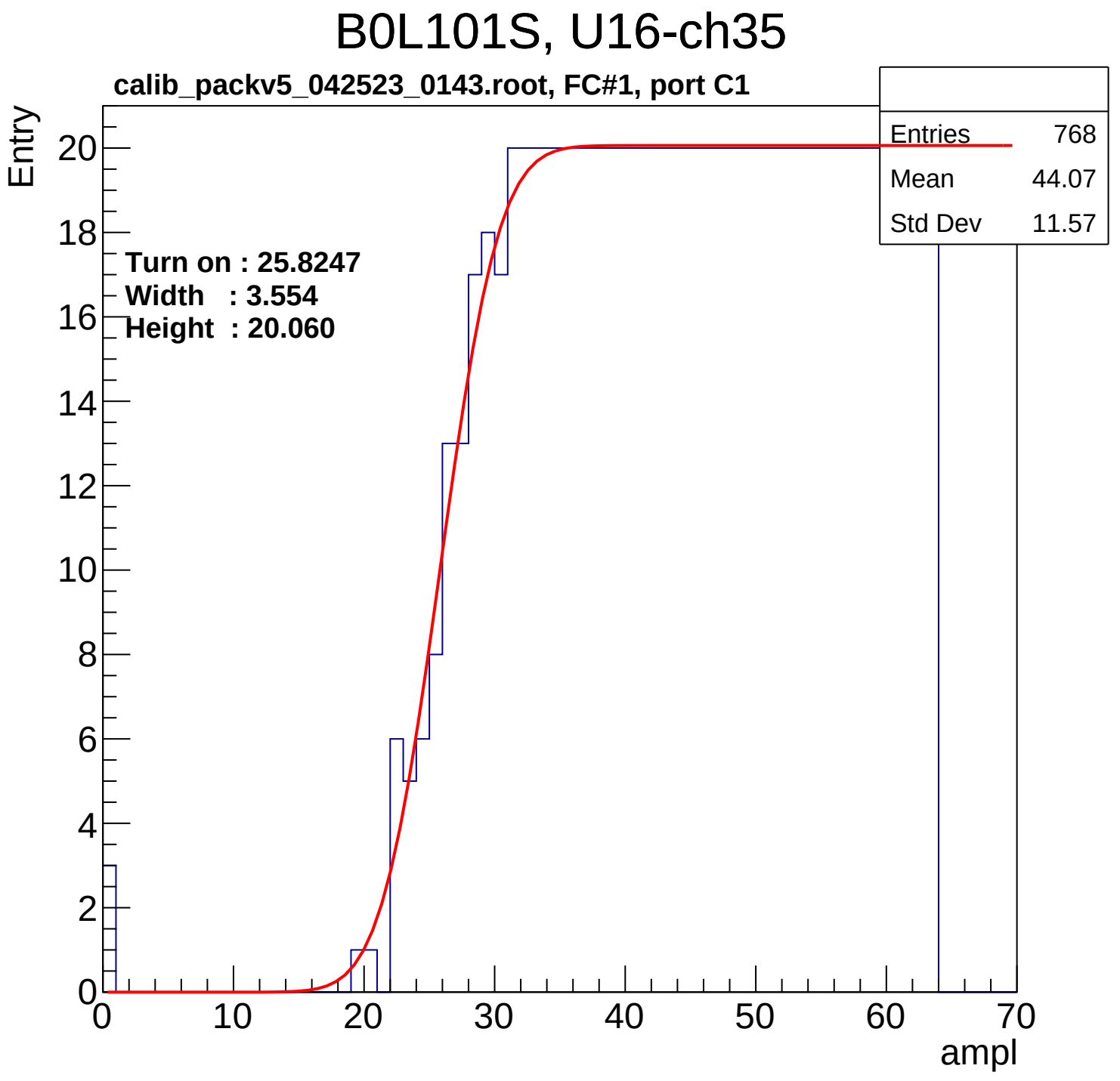
B0L101S, U16-ch35
calib_packv5_042523_0143.root, FC#1, port C1
Entries 768
Mean 44.07
Std Dev 11.57
Turn on : 25.8247
Width : 3.554
Height : 20.060
Entry
ampl
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6
8
10
12
14
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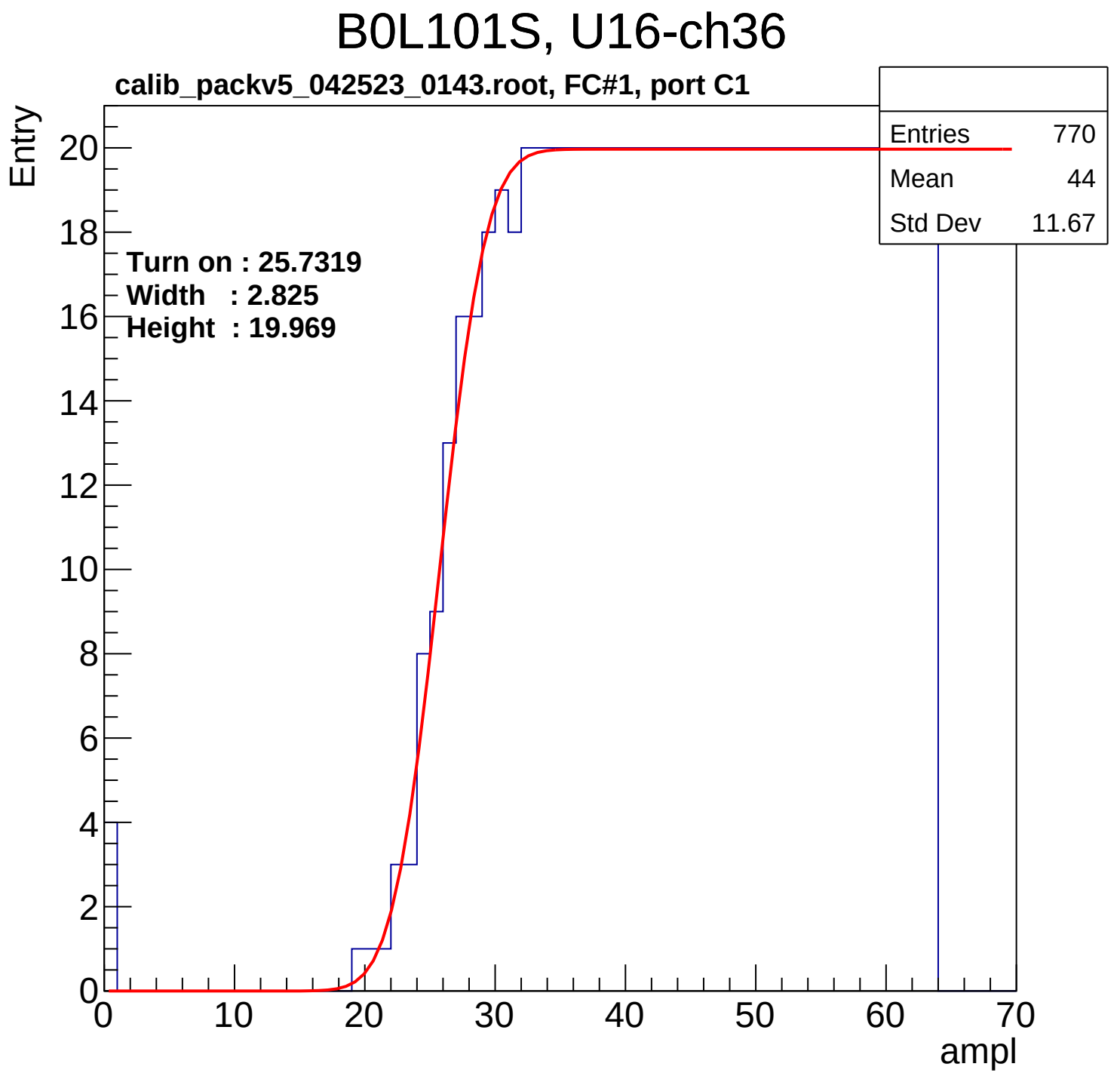
B0L101S, U16-ch36
calib_packv5_042523_0143.root, FC#1, port C1
Entries 770
Mean 44
Std Dev 11.67
Turn on : 25.7319
Width : 2.825
Height : 19.969
Entry
ampl
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6
8
10
12
14
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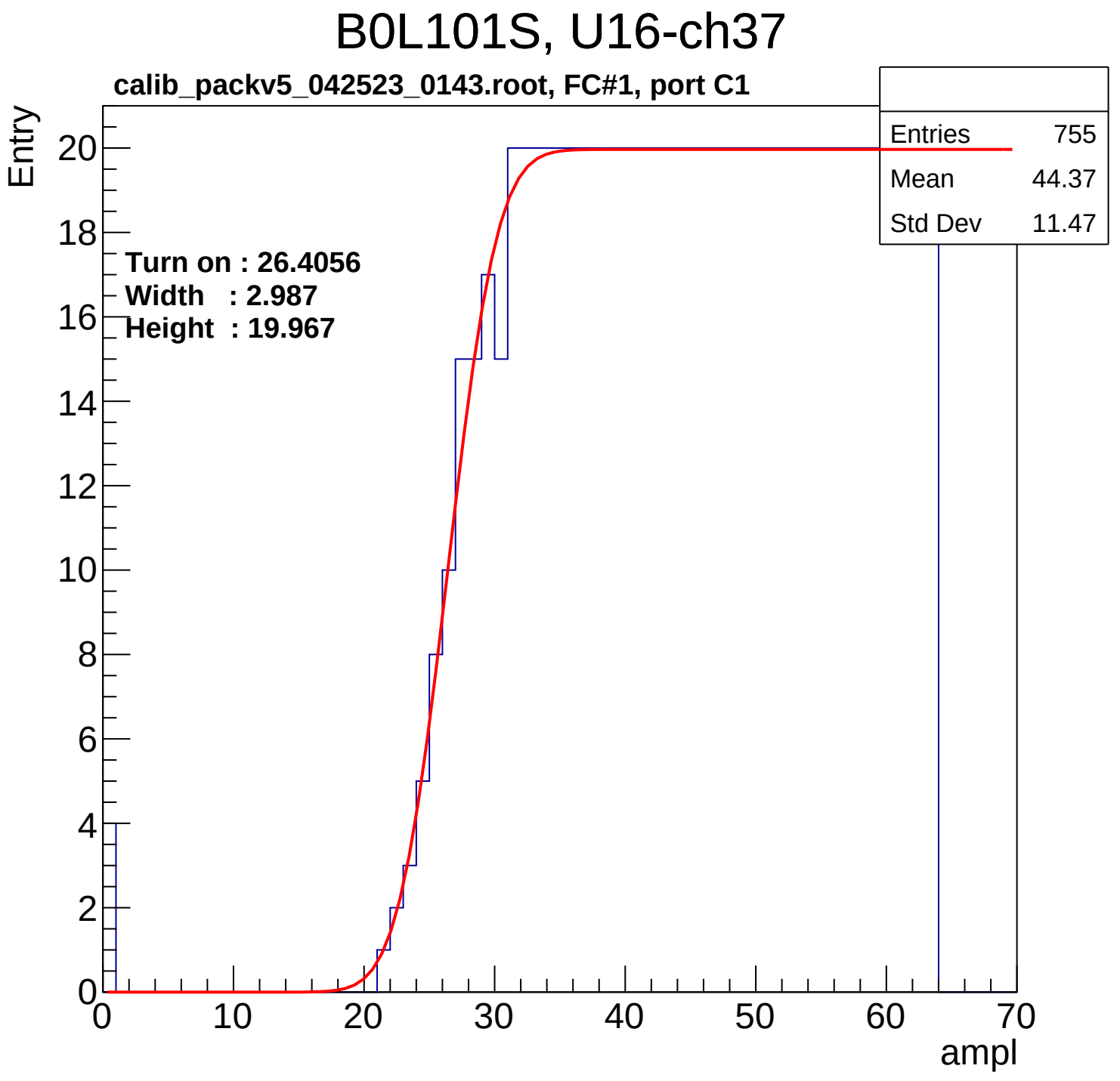
B0L101S, U16-ch37
calib_packv5_042523_0143.root, FC#1, port C1
Entries 755
Mean 44.37
Std Dev 11.47
Turn on : 26.4056
Width : 2.987
Height : 19.967
Entry
ampl
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6
8
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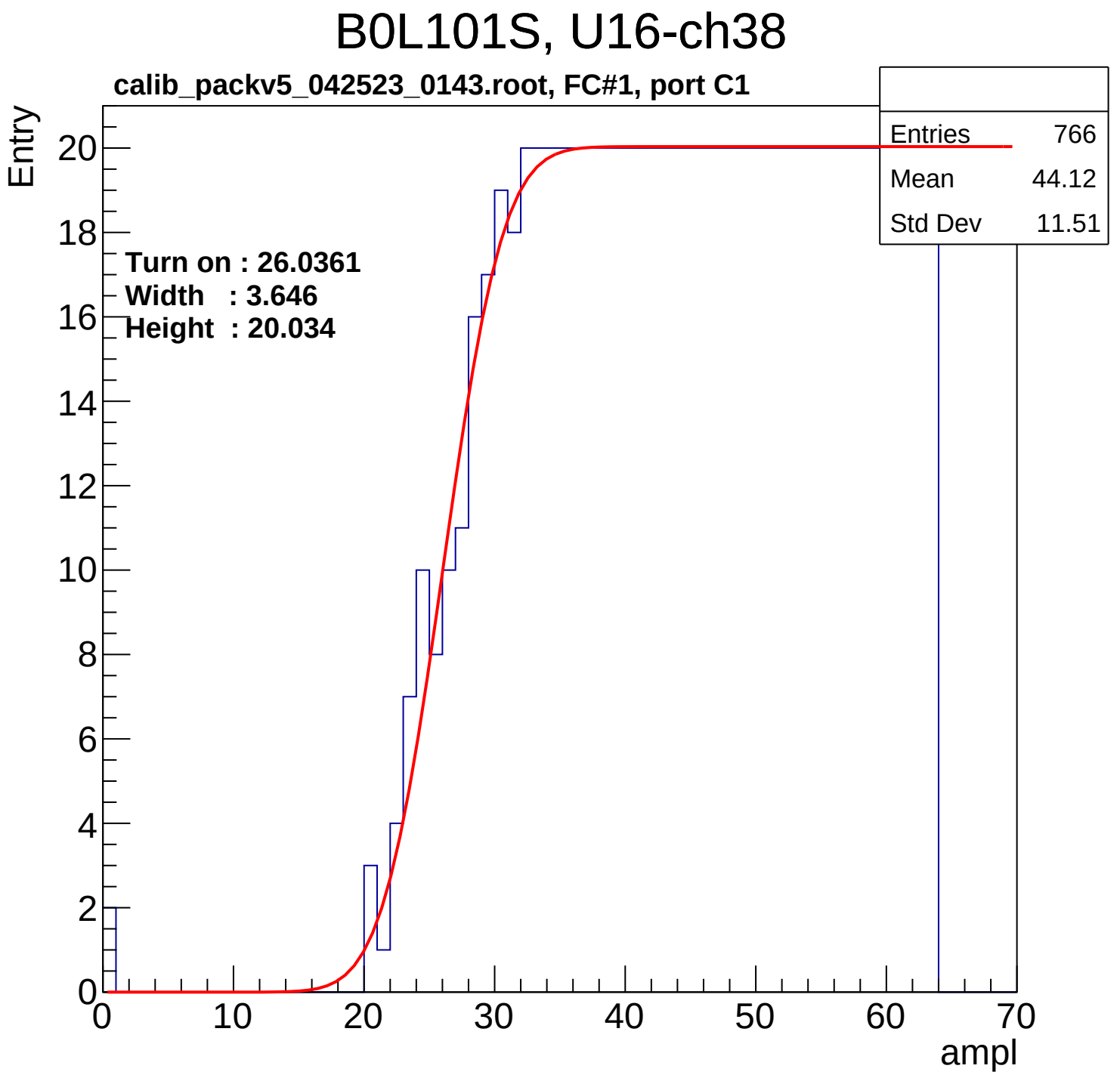
B0L101S, U16-ch38
calib_packv5_042523_0143.root, FC#1, port C1
Entries 766
Mean 44.12
Std Dev 11.51
Turn on : 26.0361
Width : 3.646
Height : 20.034
Entry
ampl
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6
8
10
12
14
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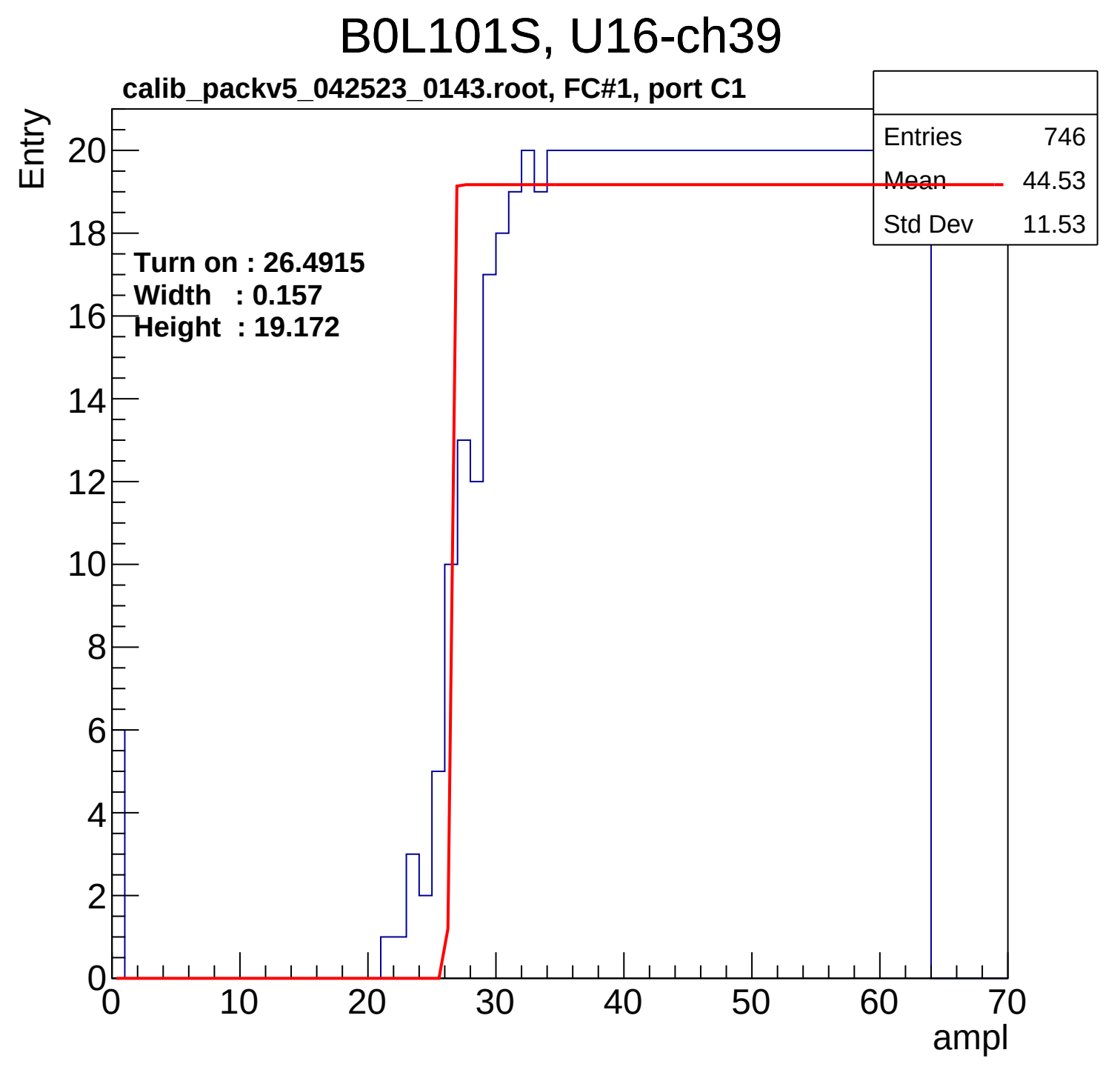
B0L101S, U16-ch39
calib_packv5_042523_0143.root, FC#1, port C1
Entries 746
Mean 44.53
Std Dev 11.53
Turn on : 26.4915
Width : 0.157
Height : 19.172
Entry
ampl
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6
8
10
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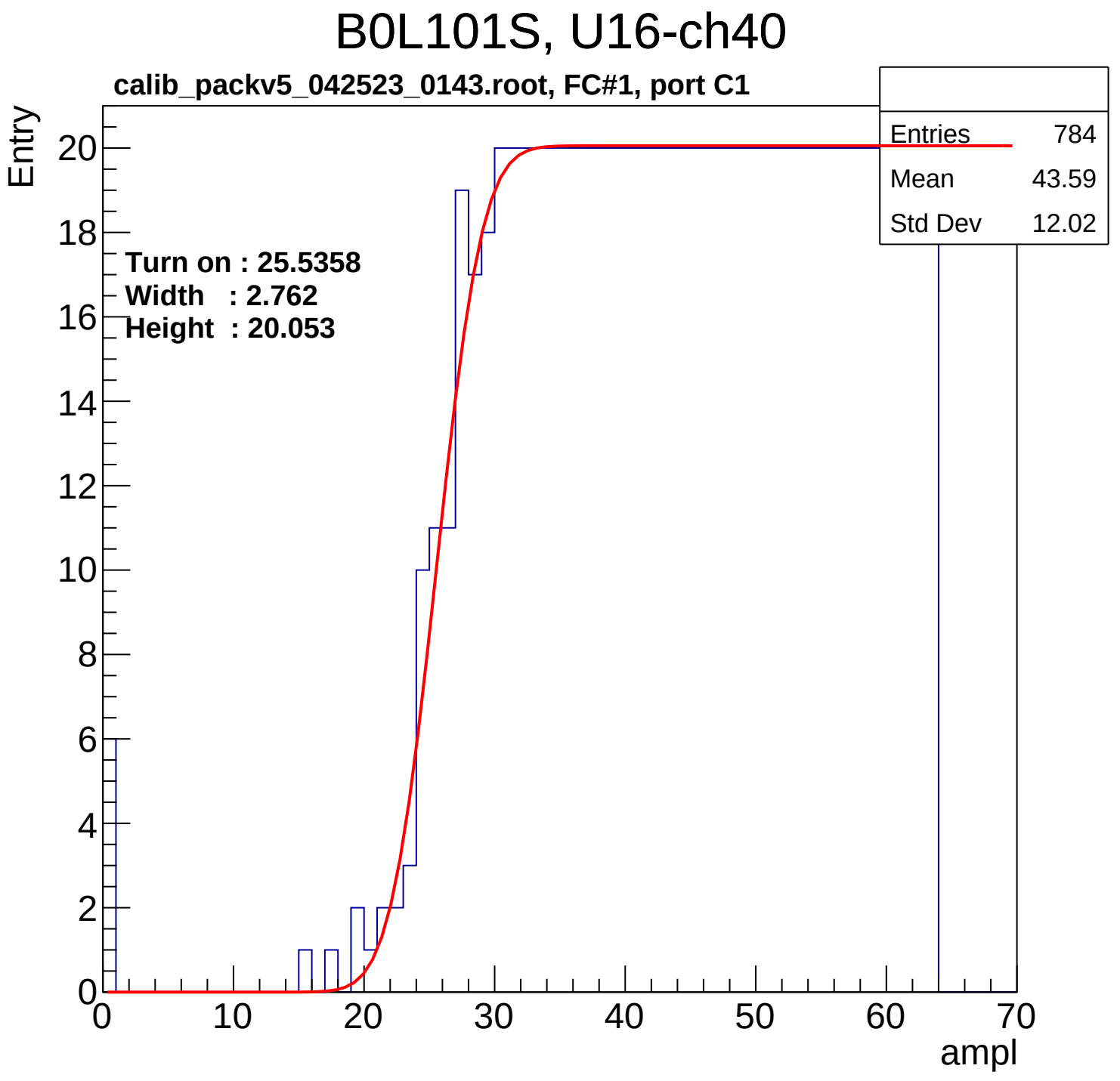
B0L101S, U16-ch40
calib_packv5_042523_0143.root, FC#1, port C1
Entries 784
Mean 43.59
Std Dev 12.02
Turn on : 25.5358
Width : 2.762
Height : 20.053
Entry
ampl
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6
8
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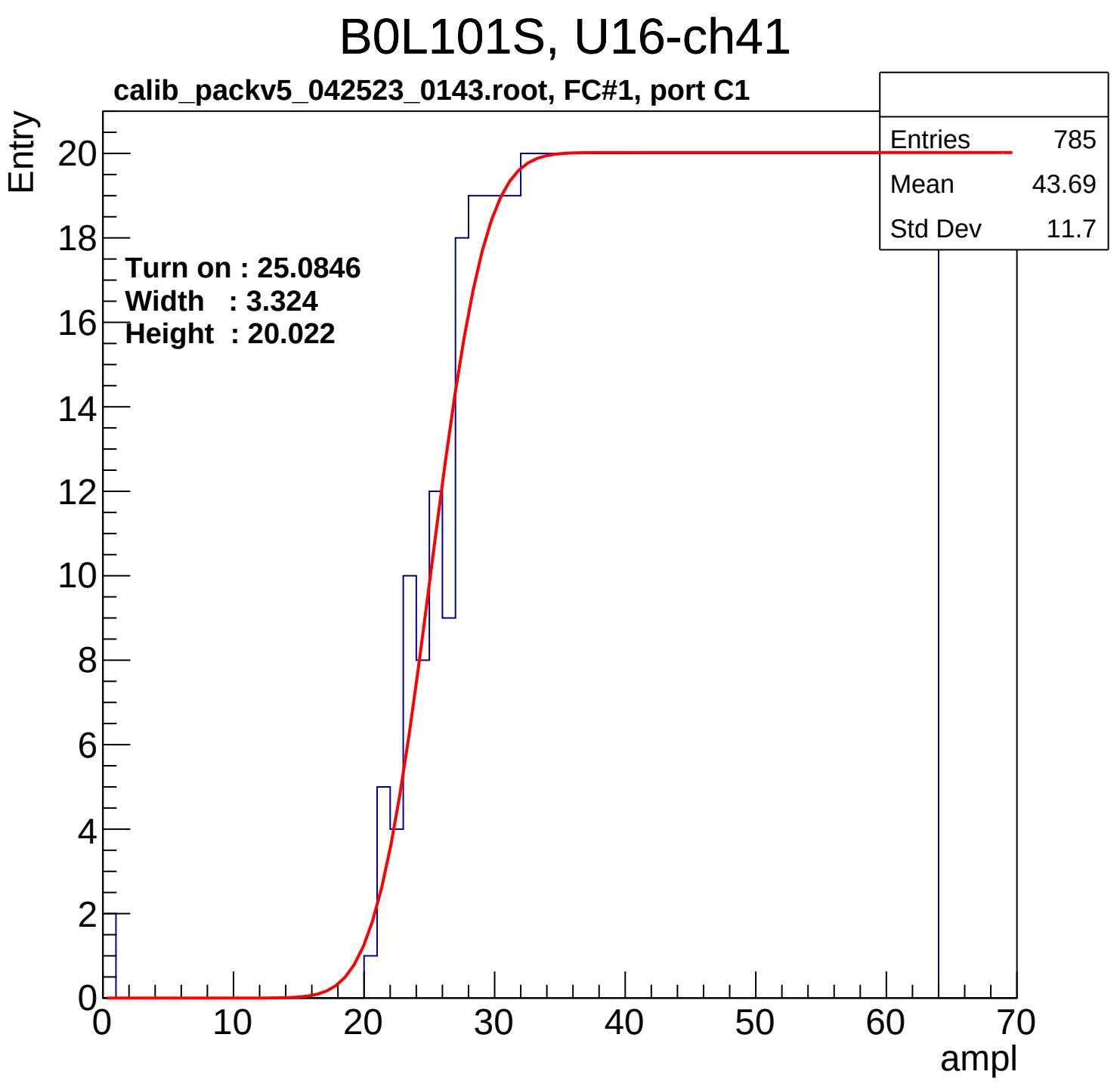
B0L101S, U16-ch41
calib_packv5_042523_0143.root, FC#1, port C1
Entries 785
Mean 43.69
Std Dev 11.7
Turn on : 25.0846
Width : 3.324
Height : 20.022
Entry
ampl
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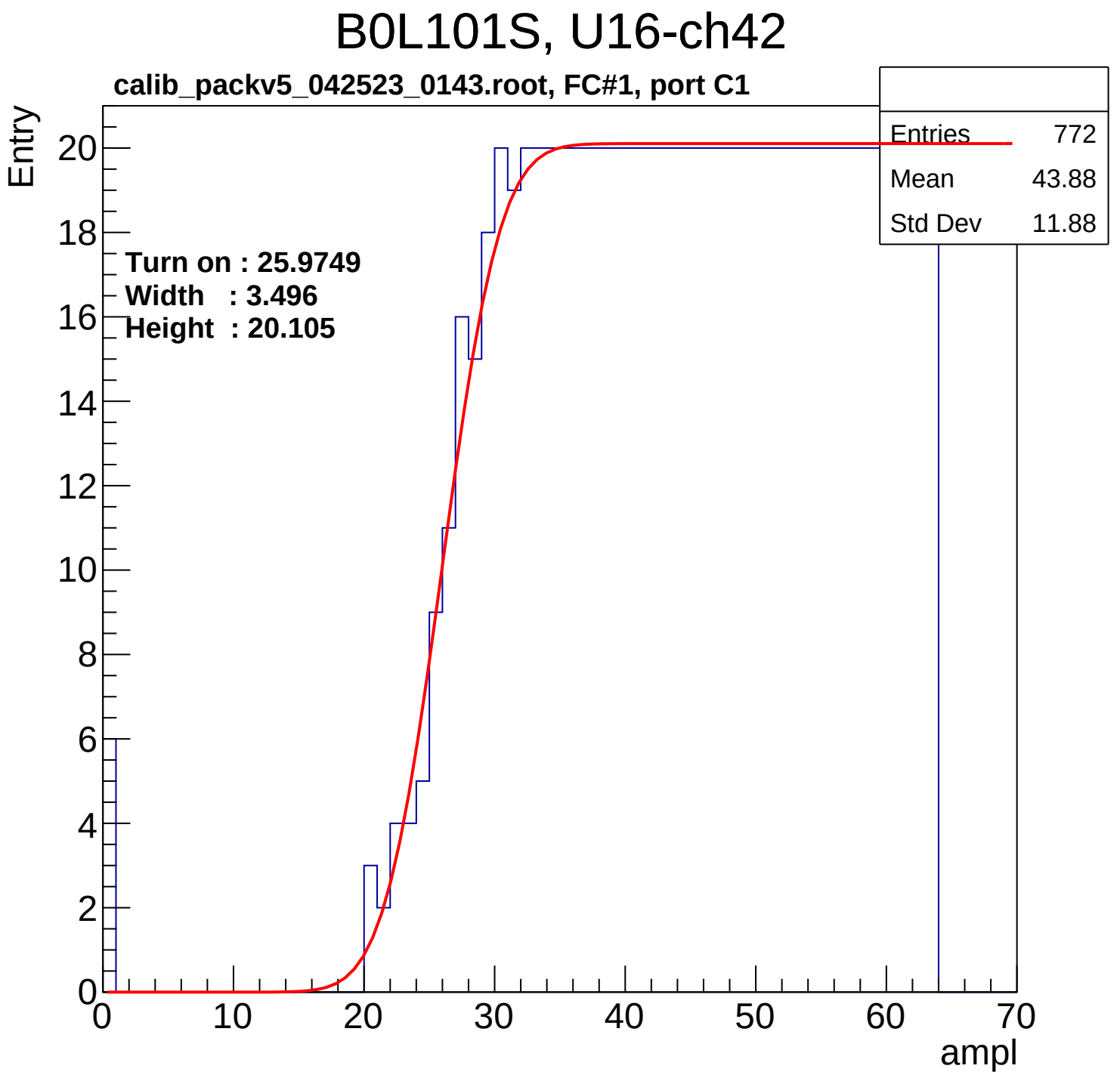
B0L101S, U16-ch42
calib_packv5_042523_0143.root, FC#1, port C1
Entries 772
Mean 43.88
Std Dev 11.88
Turn on : 25.9749
Width : 3.496
Height : 20.105
Entry
ampl
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10
12
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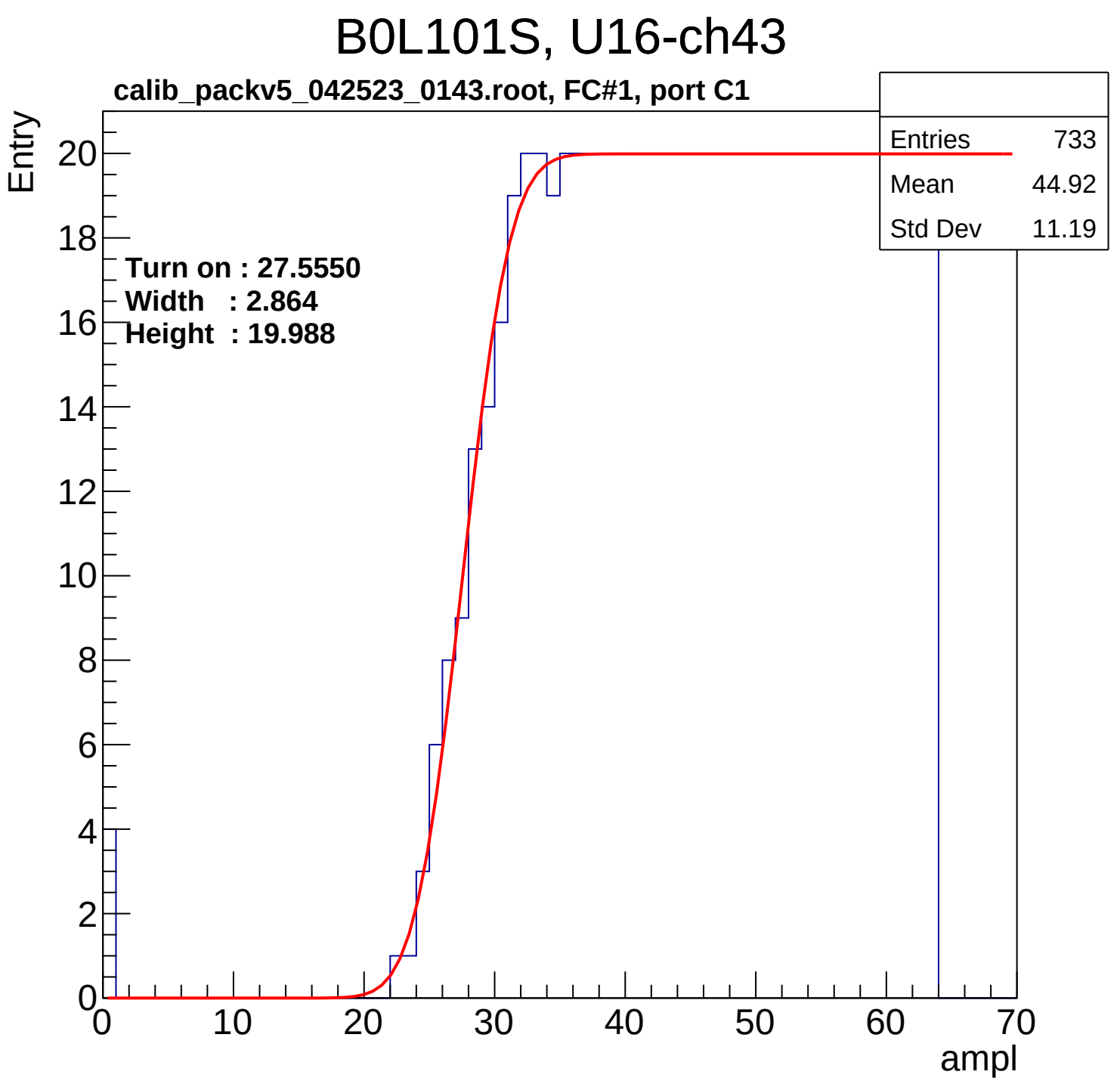
B0L101S, U16-ch43
calib_packv5_042523_0143.root, FC#1, port C1
Entries 733
Mean 44.92
Std Dev 11.19
Turn on : 27.5550
Width : 2.864
Height : 19.988
Entry
ampl
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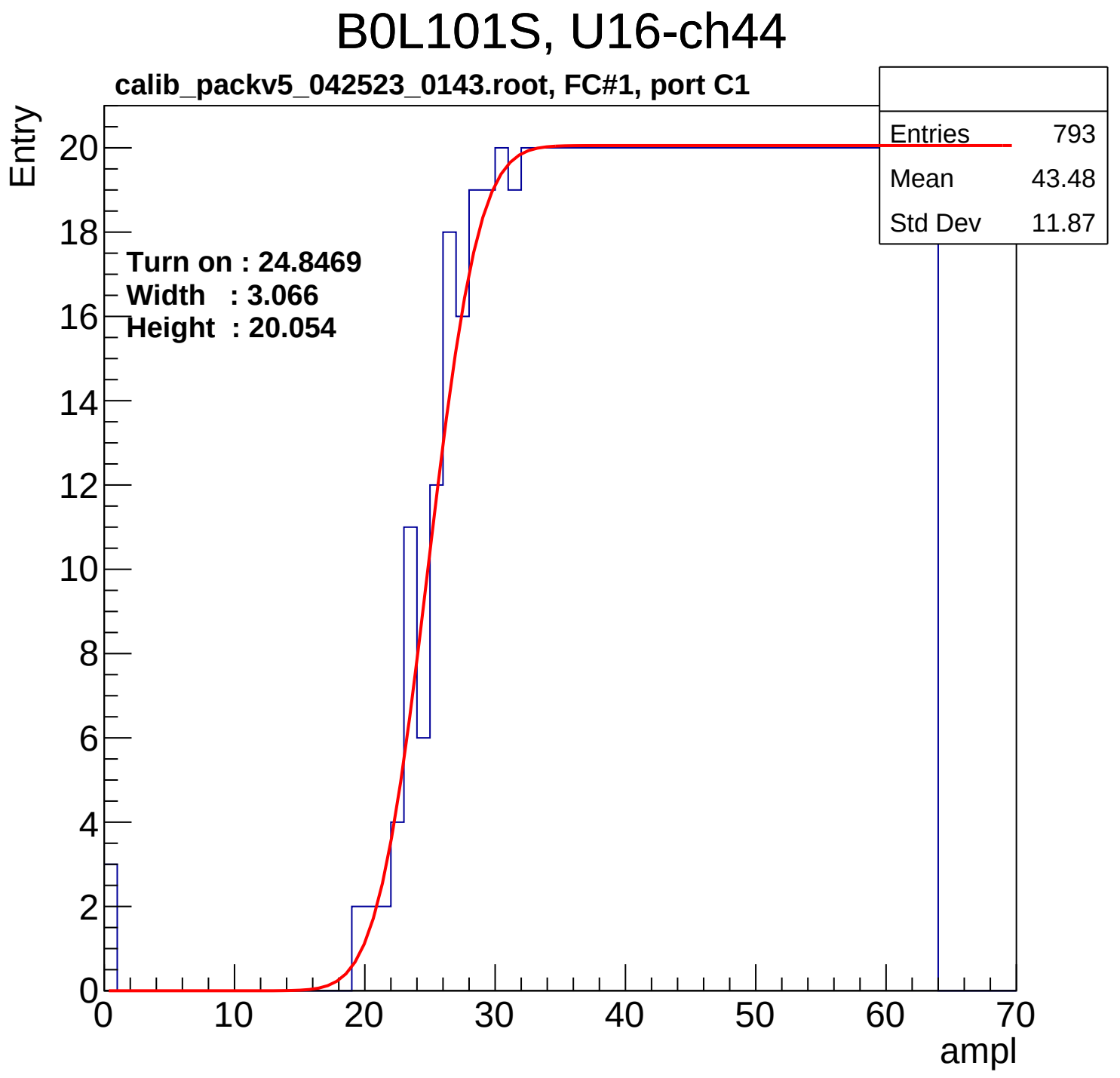
B0L101S, U16-ch44
calib_packv5_042523_0143.root, FC#1, port C1
Entries 793
Mean 43.48
Std Dev 11.87
Turn on : 24.8469
Width : 3.066
Height : 20.054
Entry
ampl
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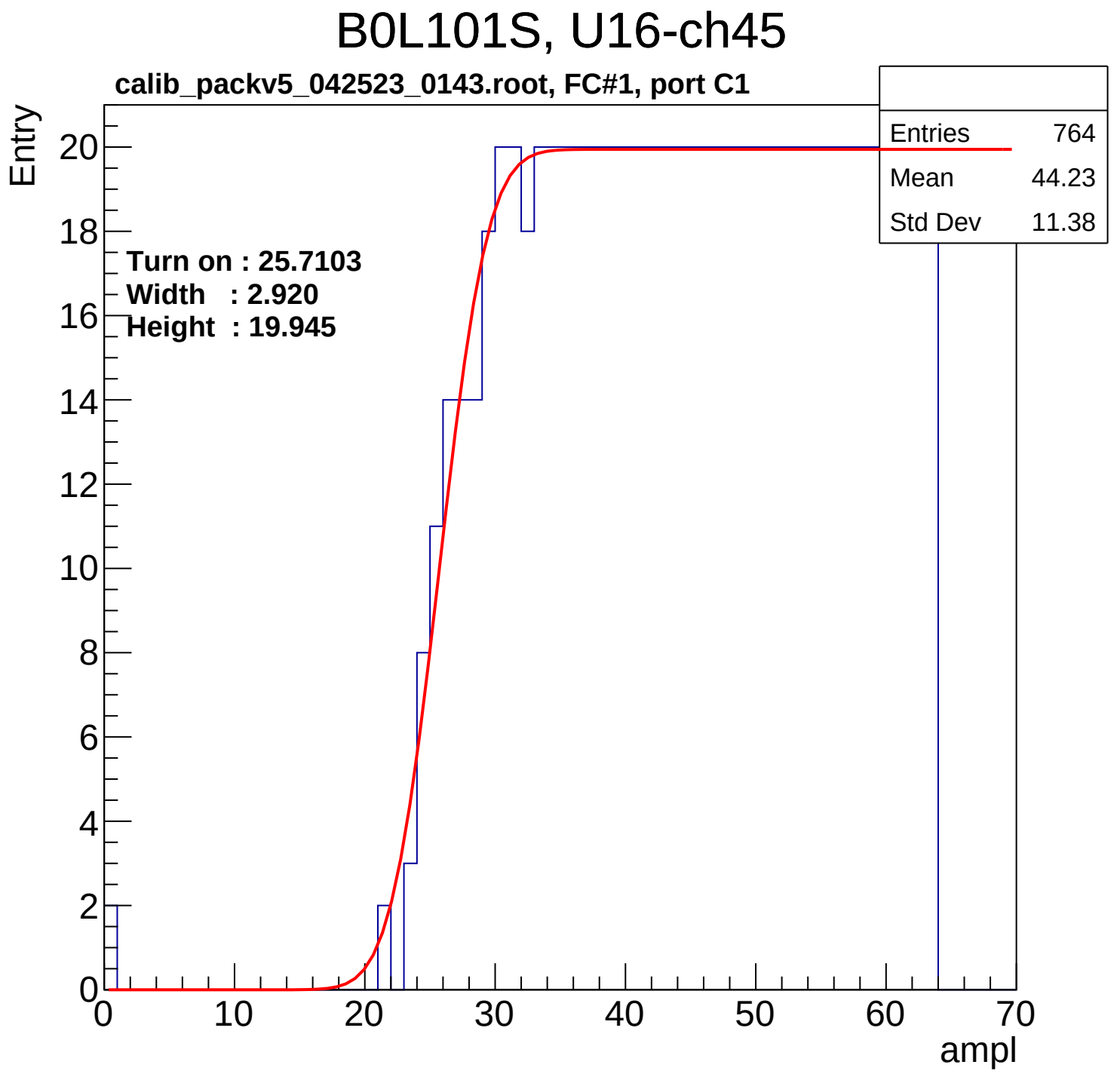
B0L101S, U16-ch45
calib_packv5_042523_0143.root, FC#1, port C1
Entries 764
Mean 44.23
Std Dev 11.38
Turn on : 25.7103
Width : 2.920
Height : 19.945
Entry
ampl
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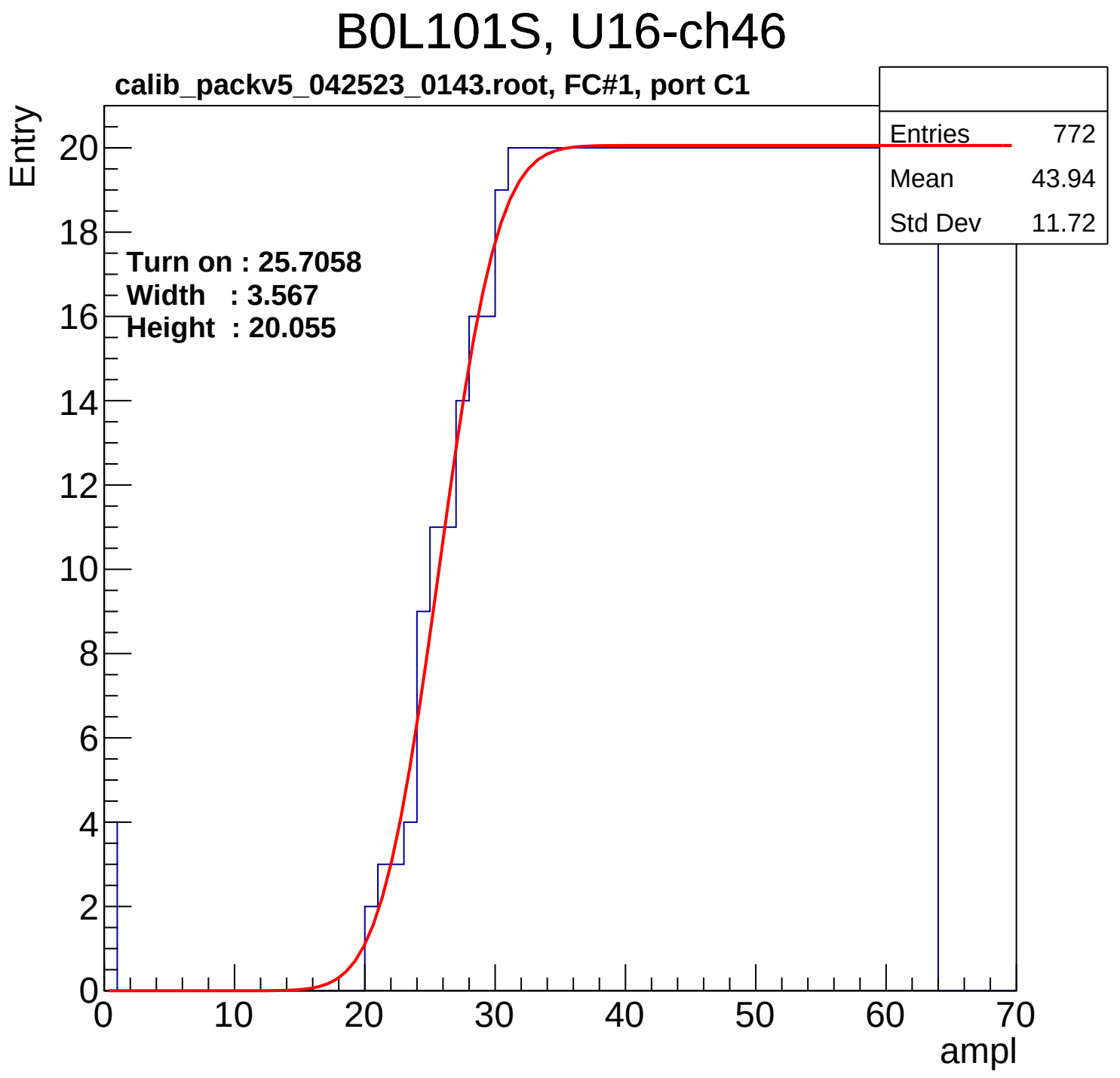
B0L101S, U16-ch46
calib_packv5_042523_0143.root, FC#1, port C1
Entries 772
Mean 43.94
Std Dev 11.72
Turn on : 25.7058
Width : 3.567
Height : 20.055
Entry
ampl
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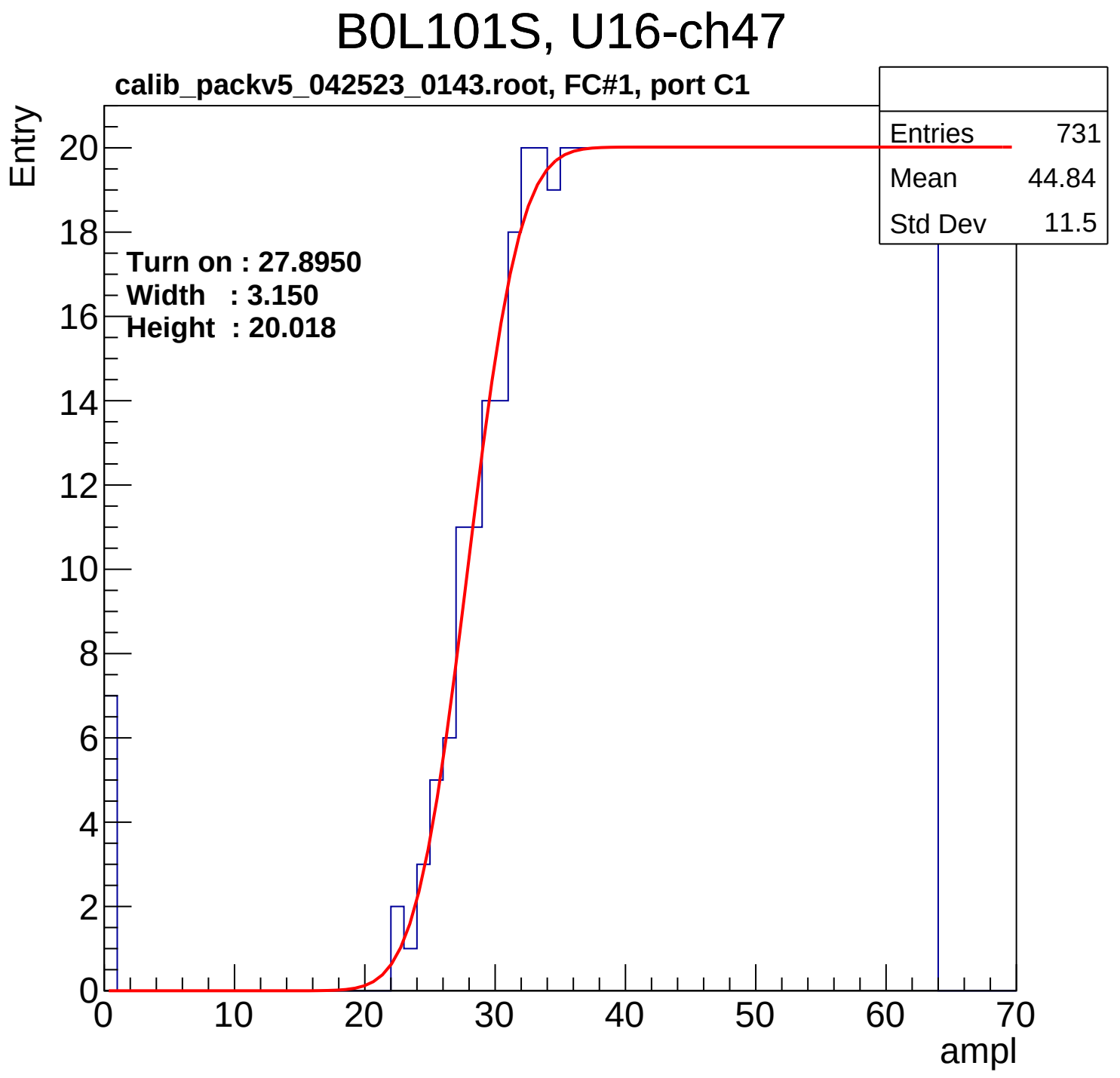
B0L101S, U16-ch47
calib_packv5_042523_0143.root, FC#1, port C1
Entries 731
Mean 44.84
Std Dev 11.5
Turn on : 27.8950
Width : 3.150
Height : 20.018
Entry
ampl
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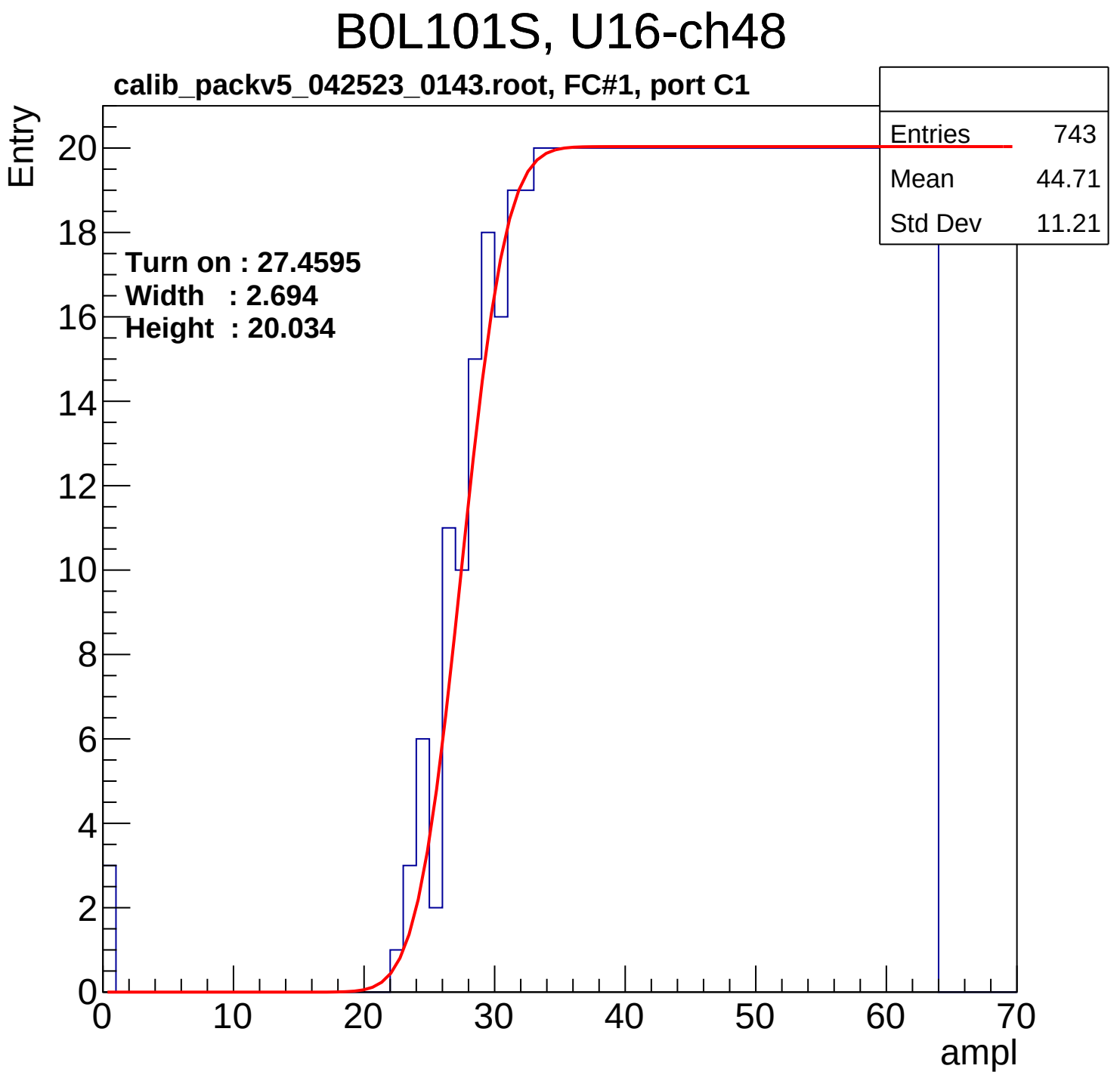
B0L101S, U16-ch48
calib_packv5_042523_0143.root, FC#1, port C1
Entries 743
Mean 44.71
Std Dev 11.21
Turn on : 27.4595
Width : 2.694
Height : 20.034
Entry
ampl
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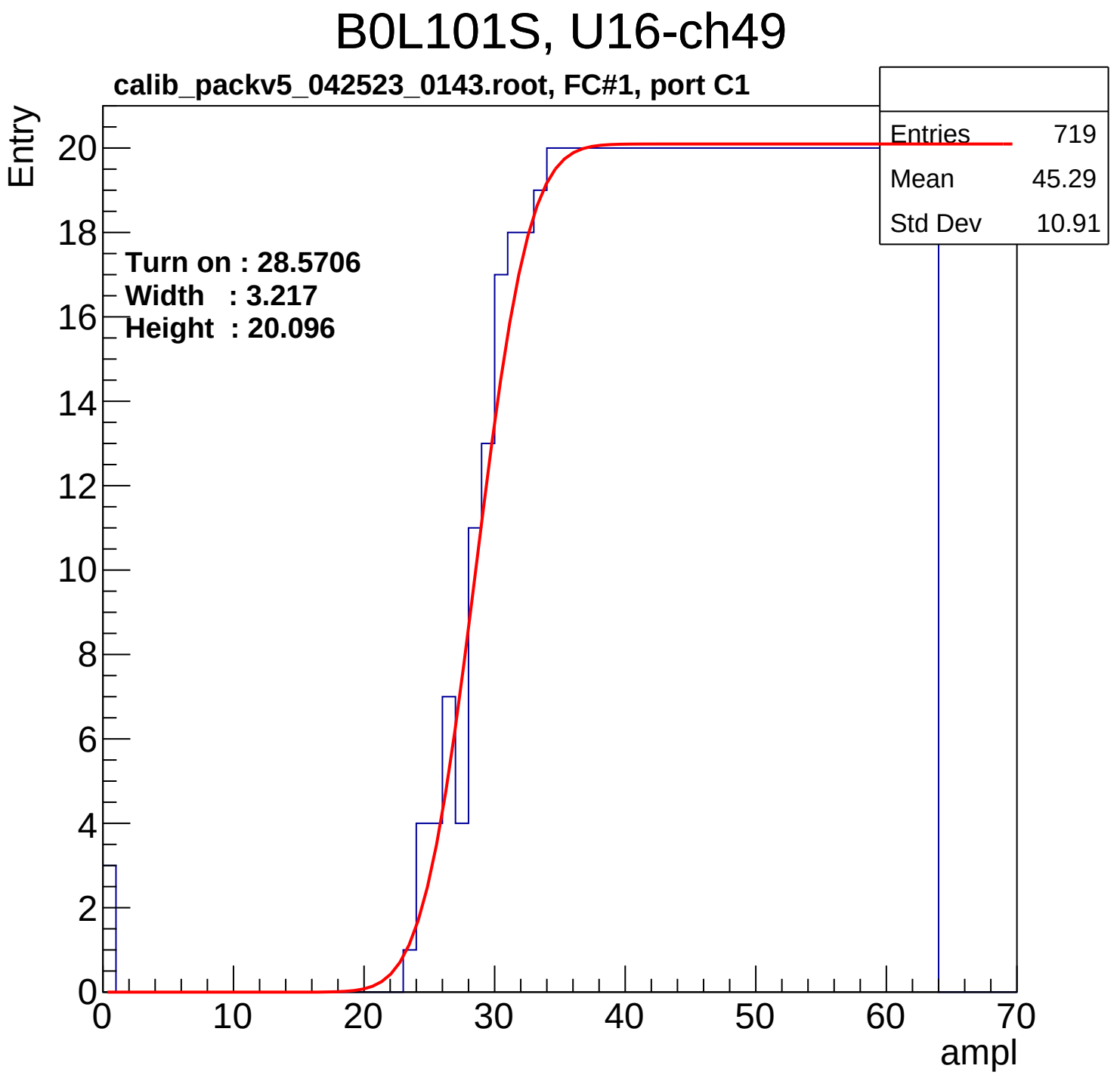
B0L101S, U16-ch49
calib_packv5_042523_0143.root, FC#1, port C1
Entries 719
Mean 45.29
Std Dev 10.91
Turn on : 28.5706
Width : 3.217
Height : 20.096
Entry
ampl
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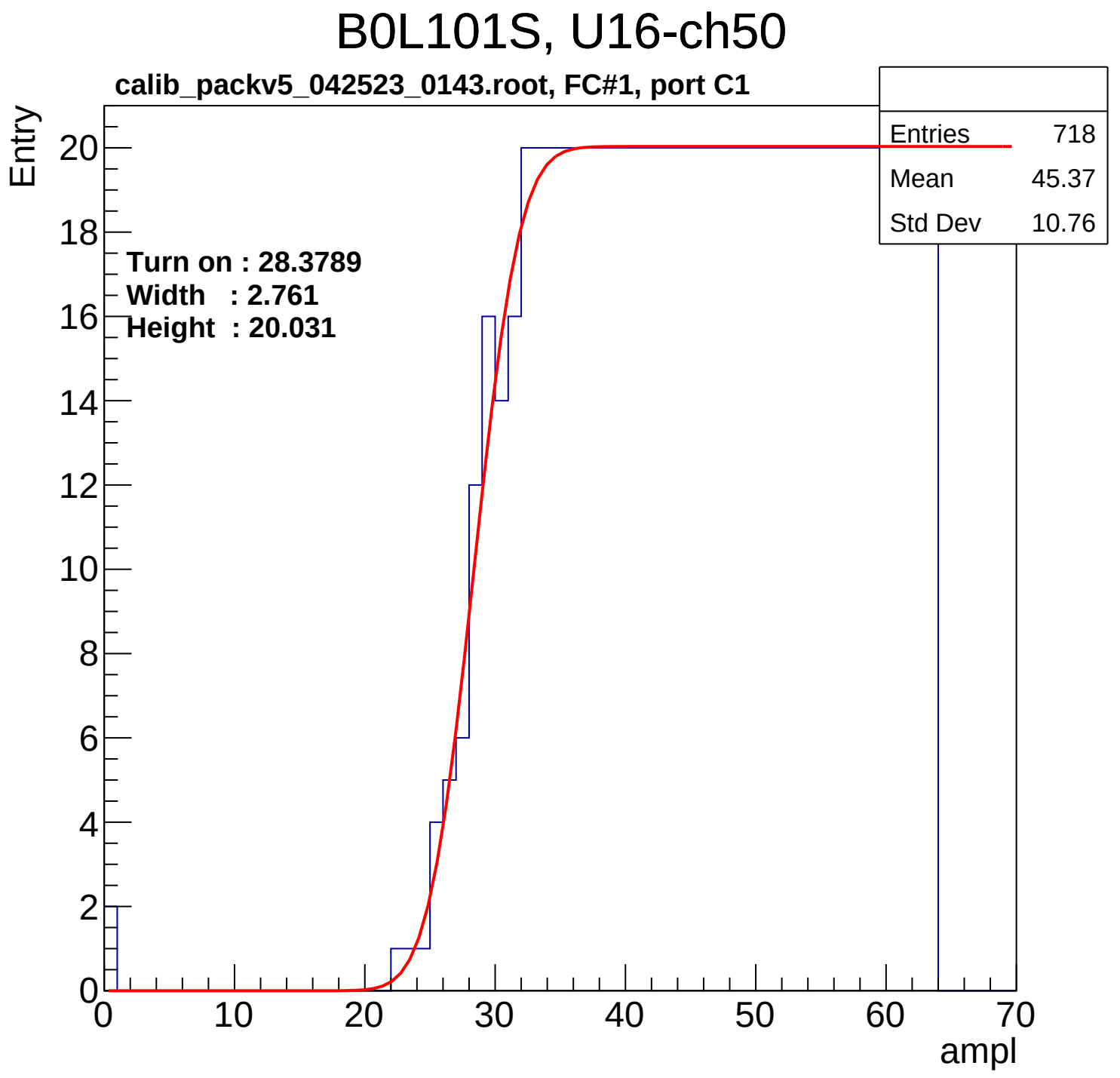
B0L101S, U16-ch50
calib_packv5_042523_0143.root, FC#1, port C1
Entries 718
Mean 45.37
Std Dev 10.76
Turn on : 28.3789
Width : 2.761
Height : 20.031
Entry
ampl
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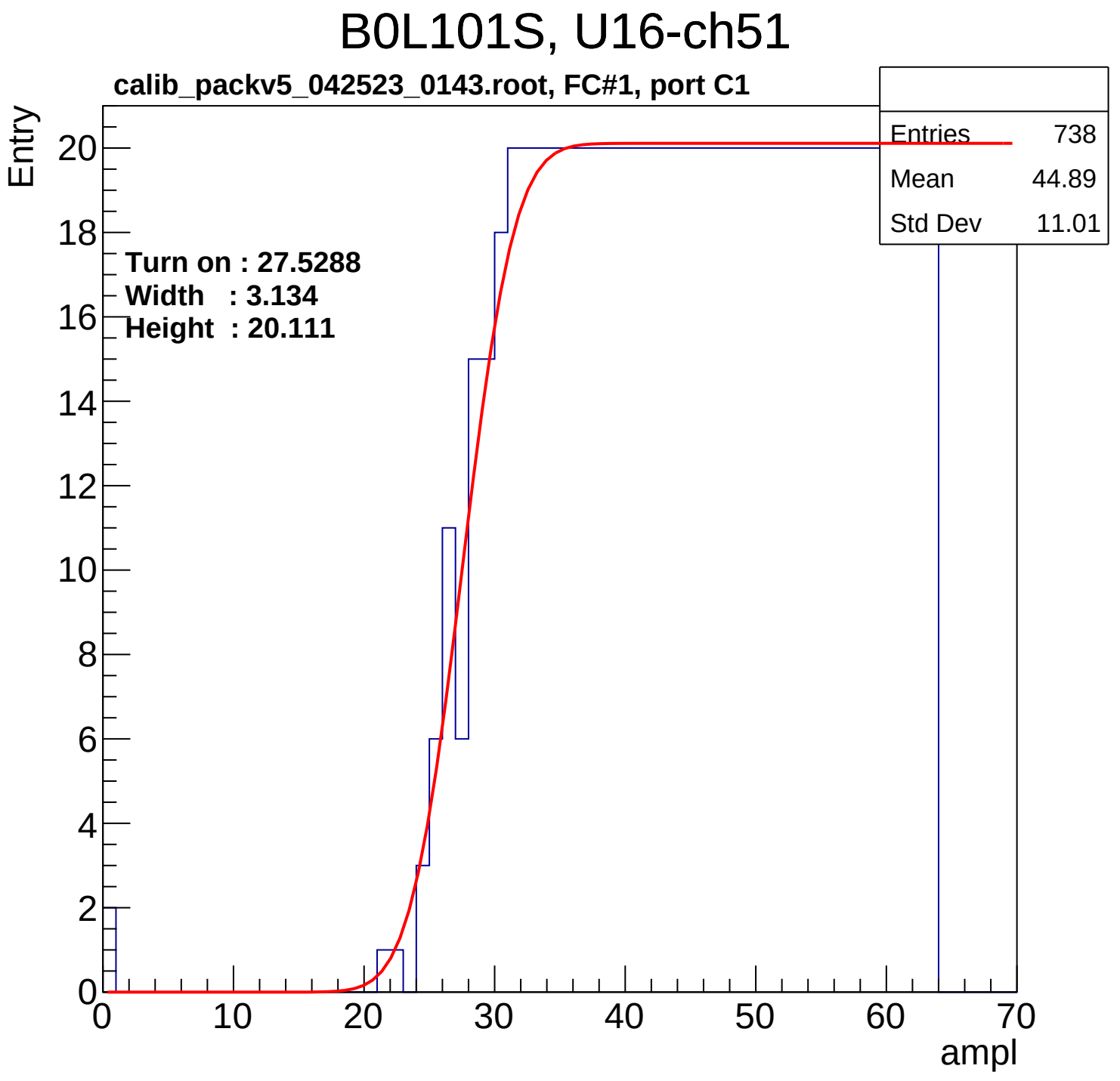
B0L101S, U16-ch51
calib_packv5_042523_0143.root, FC#1, port C1
Entries 738
Mean 44.89
Std Dev 11.01
Turn on : 27.5288
Width : 3.134
Height : 20.111
Entry
ampl
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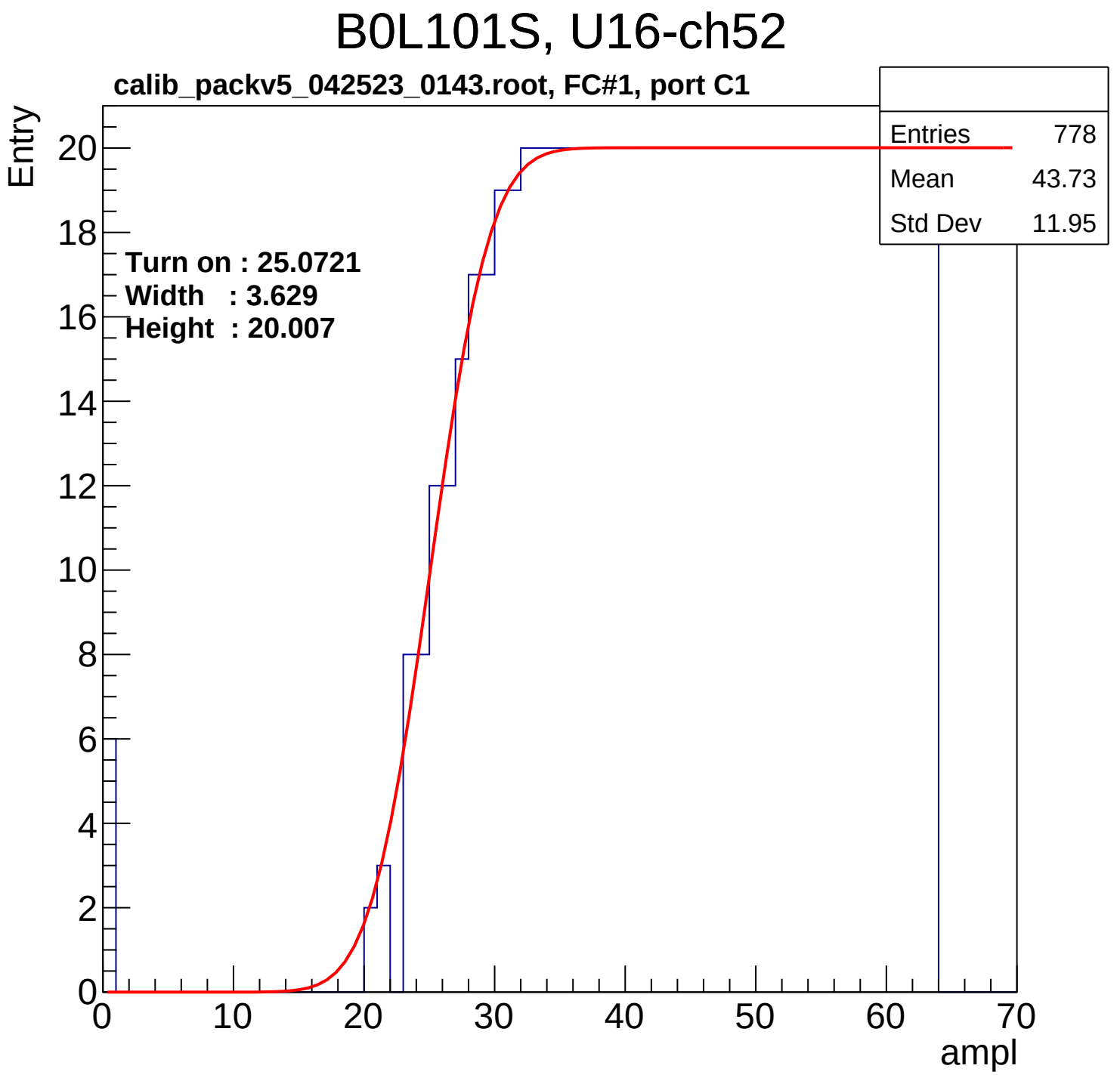
B0L101S, U16-ch52
calib_packv5_042523_0143.root, FC#1, port C1
Entries 778
Mean 43.73
Std Dev 11.95
Turn on : 25.0721
Width : 3.629
Height : 20.007
Entry
ampl
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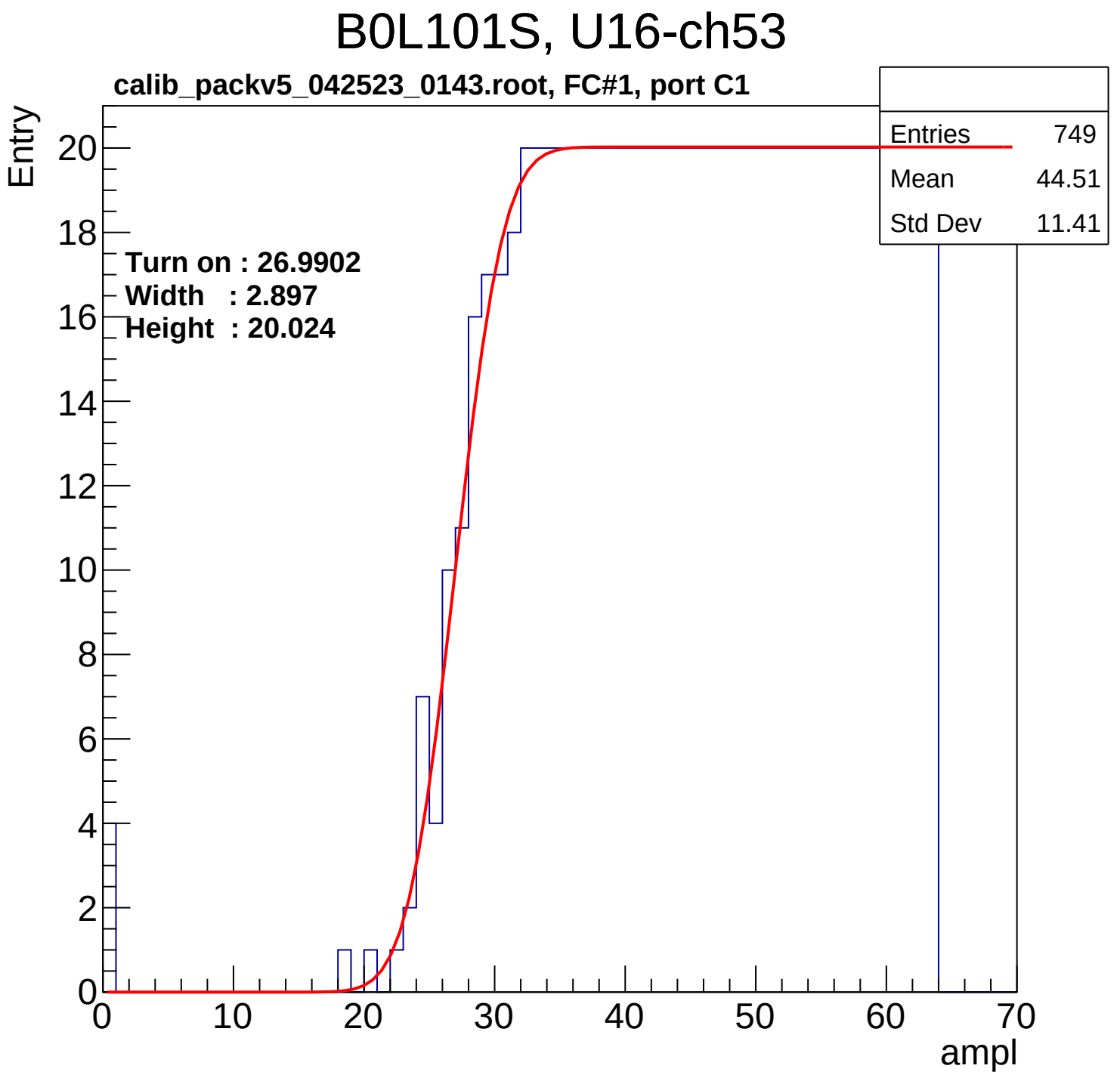
B0L101S, U16-ch53
calib_packv5_042523_0143.root, FC#1, port C1
Entries 749
Mean 44.51
Std Dev 11.41
Turn on : 26.9902
Width : 2.897
Height : 20.024
Entry
ampl
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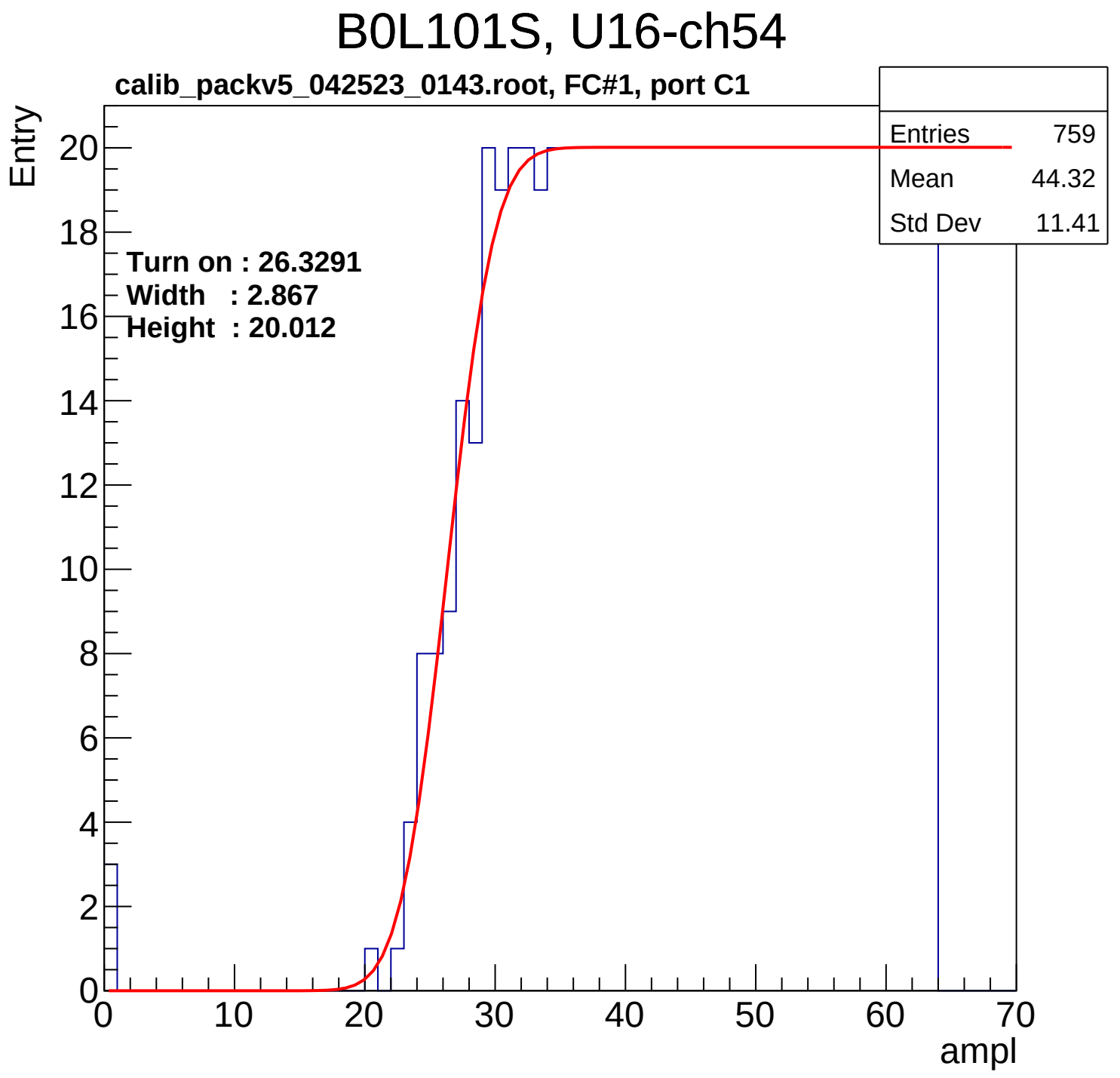
B0L101S, U16-ch54
calib_packv5_042523_0143.root, FC#1, port C1
Entries 759
Mean 44.32
Std Dev 11.41
Turn on : 26.3291
Width : 2.867
Height : 20.012
Entry
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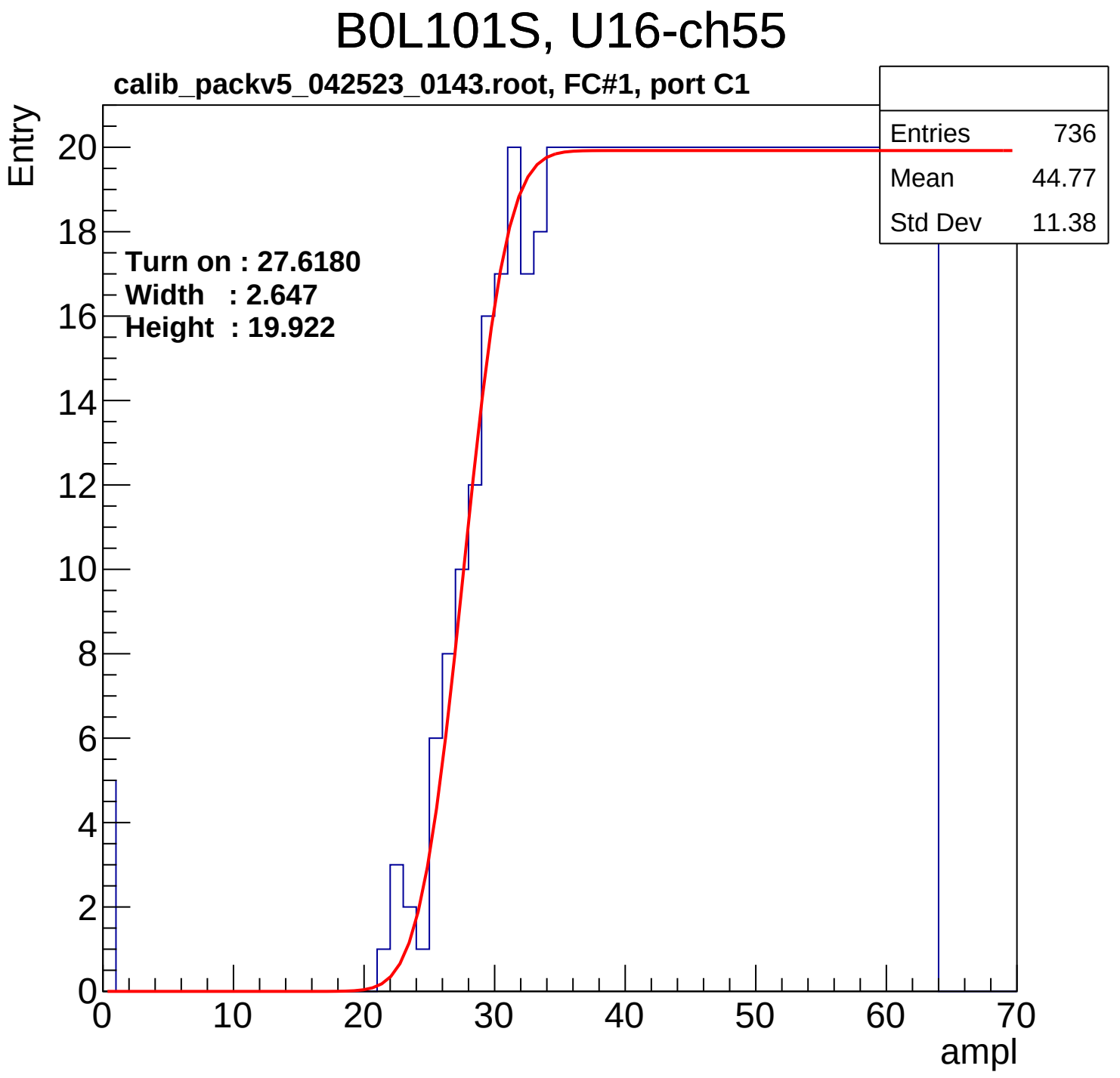
B0L101S, U16-ch55
calib_packv5_042523_0143.root, FC#1, port C1
Entries 736
Mean 44.77
Std Dev 11.38
Turn on : 27.6180
Width : 2.647
Height : 19.922
Entry
ampl
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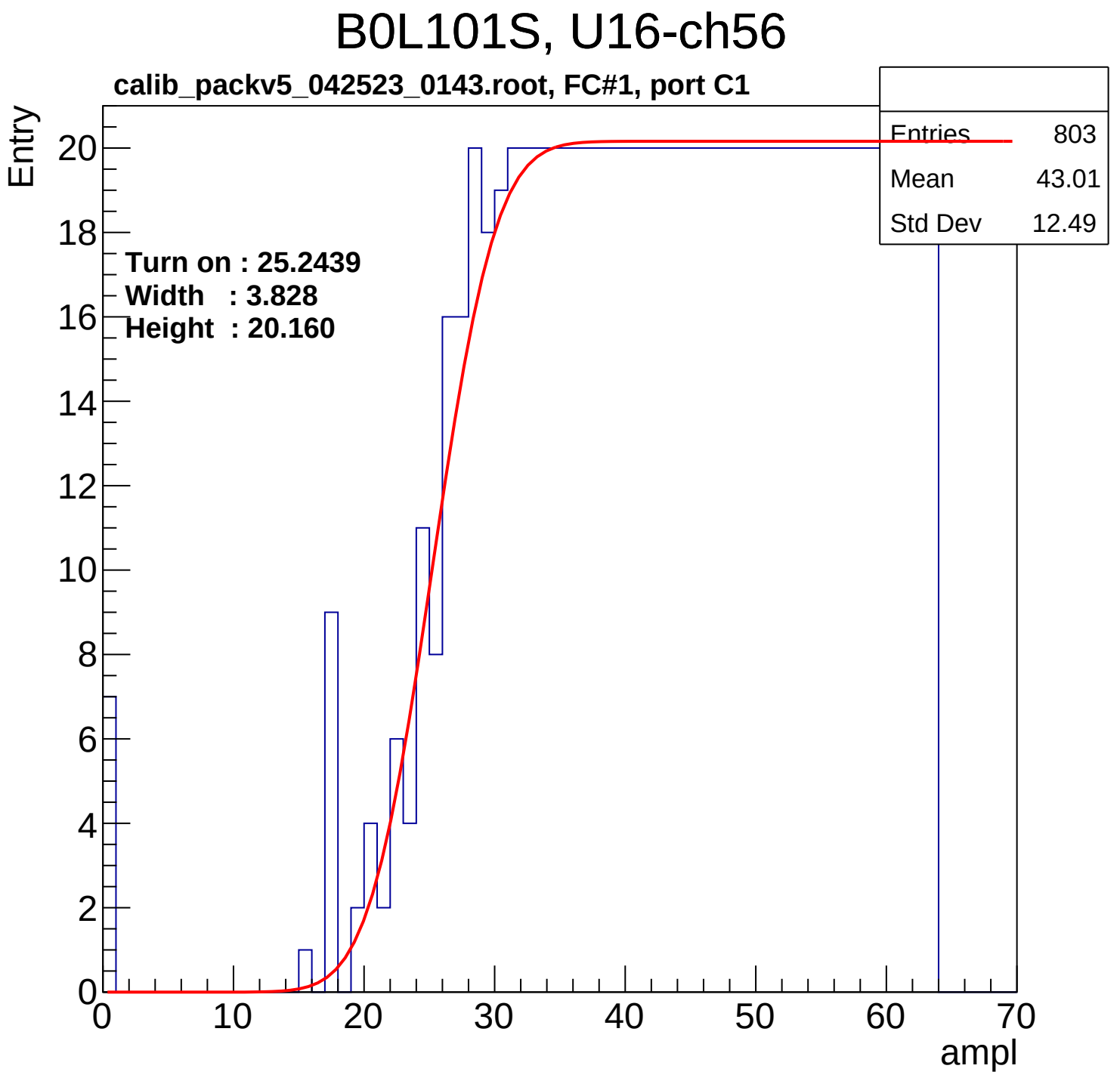
B0L101S, U16-ch56
calib_packv5_042523_0143.root, FC#1, port C1
Entries 803
Mean 43.01
Std Dev 12.49
Turn on : 25.2439
Width : 3.828
Height : 20.160
Entry
ampl
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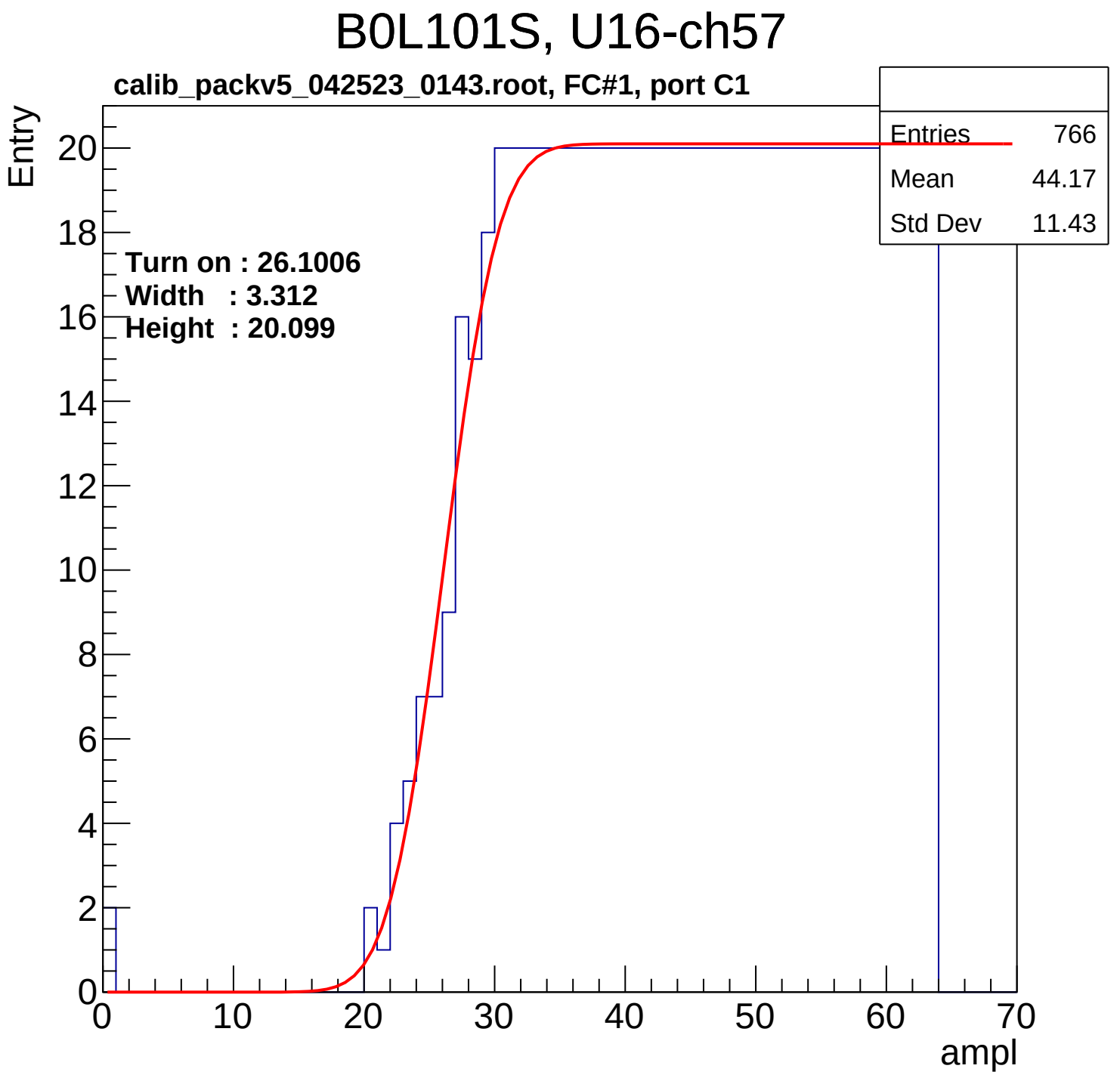
B0L101S, U16-ch57
calib_packv5_042523_0143.root, FC#1, port C1
Entries 766
Mean 44.17
Std Dev 11.43
Turn on : 26.1006
Width : 3.312
Height : 20.099
Entry
ampl
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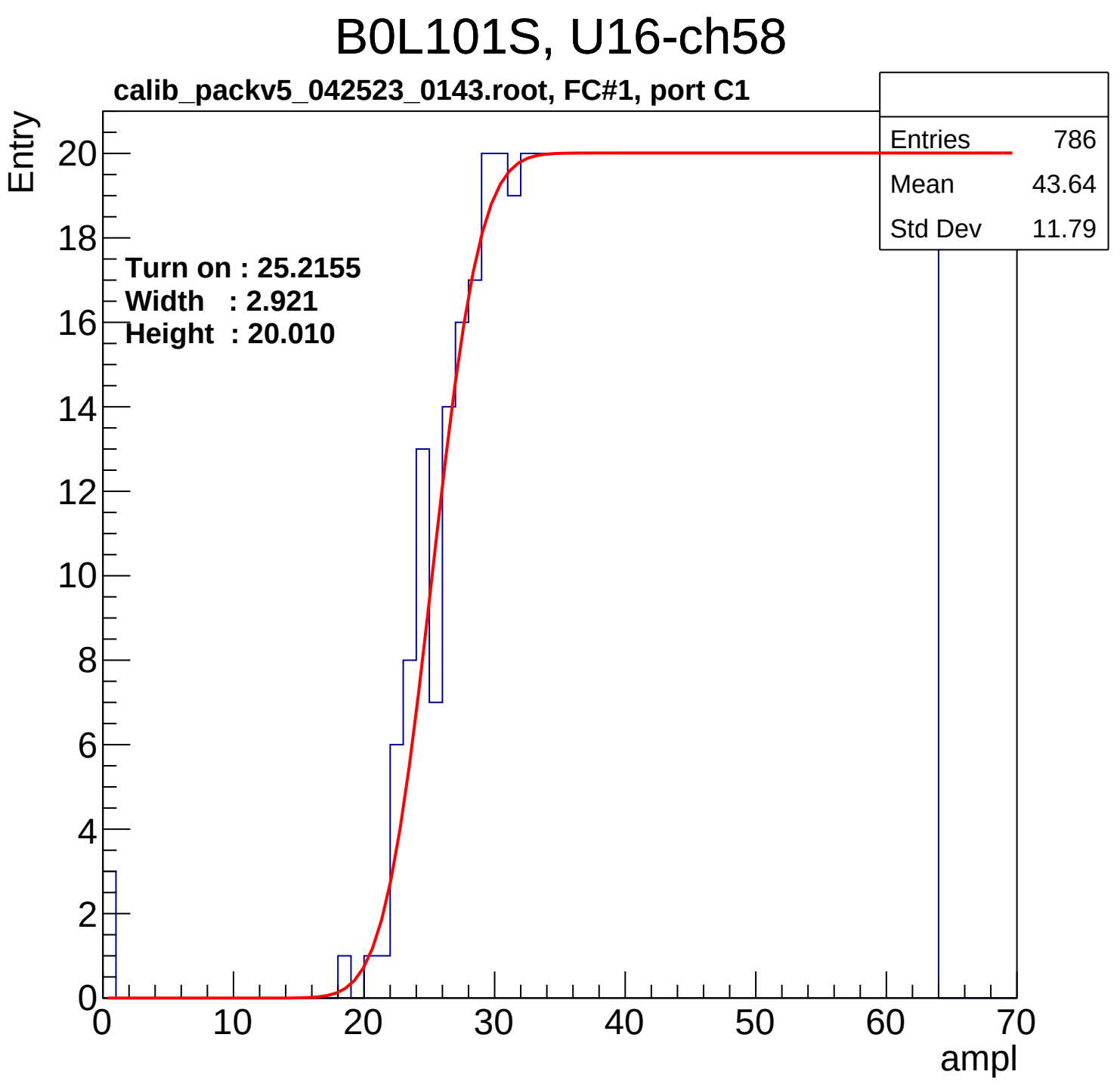
B0L101S, U16-ch58
calib_packv5_042523_0143.root, FC#1, port C1
Entries 786
Mean 43.64
Std Dev 11.79
Turn on : 25.2155
Width : 2.921
Height : 20.010
Entry
ampl
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6
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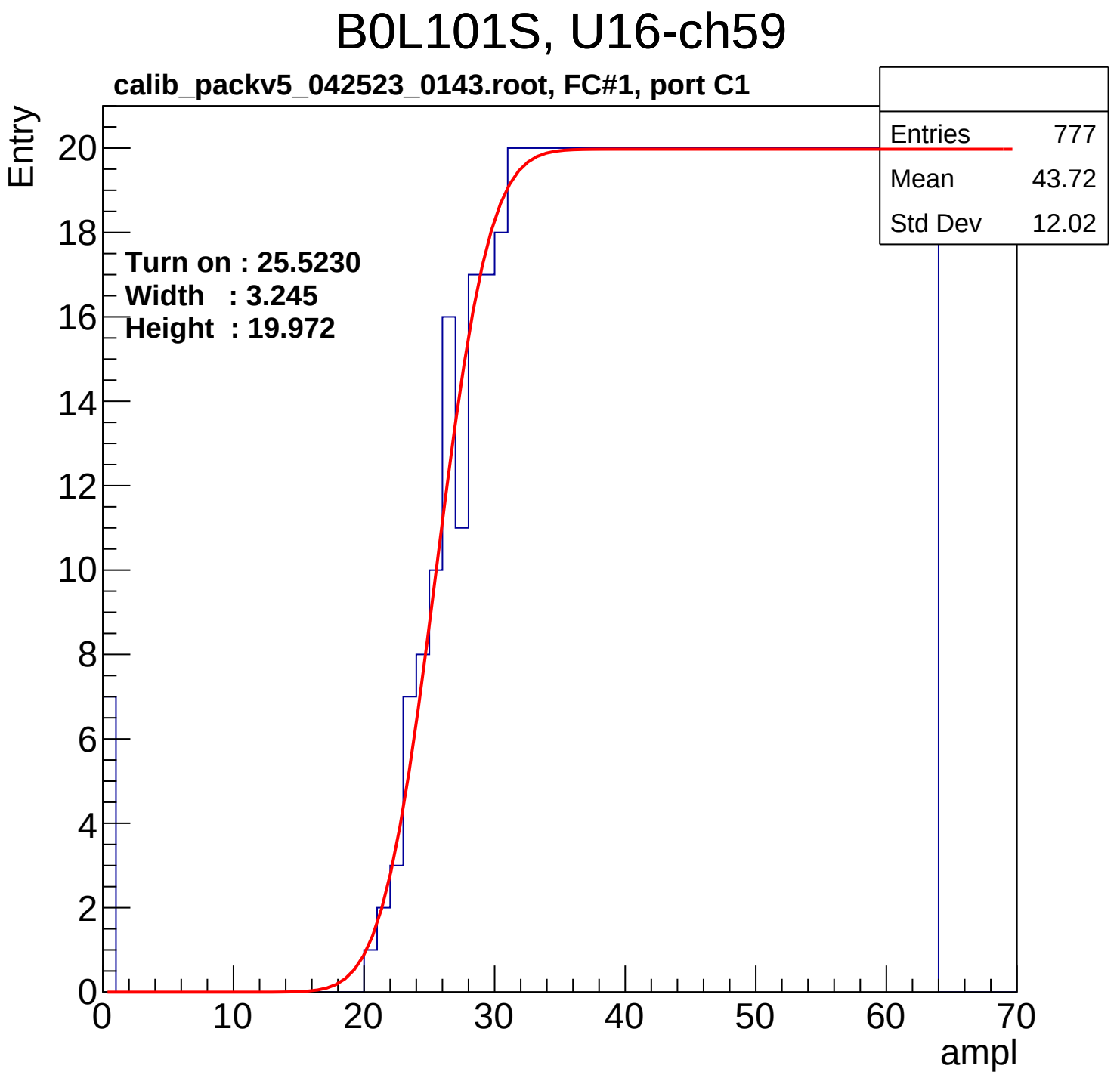
B0L101S, U16-ch59
calib_packv5_042523_0143.root, FC#1, port C1
Entries 777
Mean 43.72
Std Dev 12.02
Turn on : 25.5230
Width : 3.245
Height : 19.972
Entry
ampl
0
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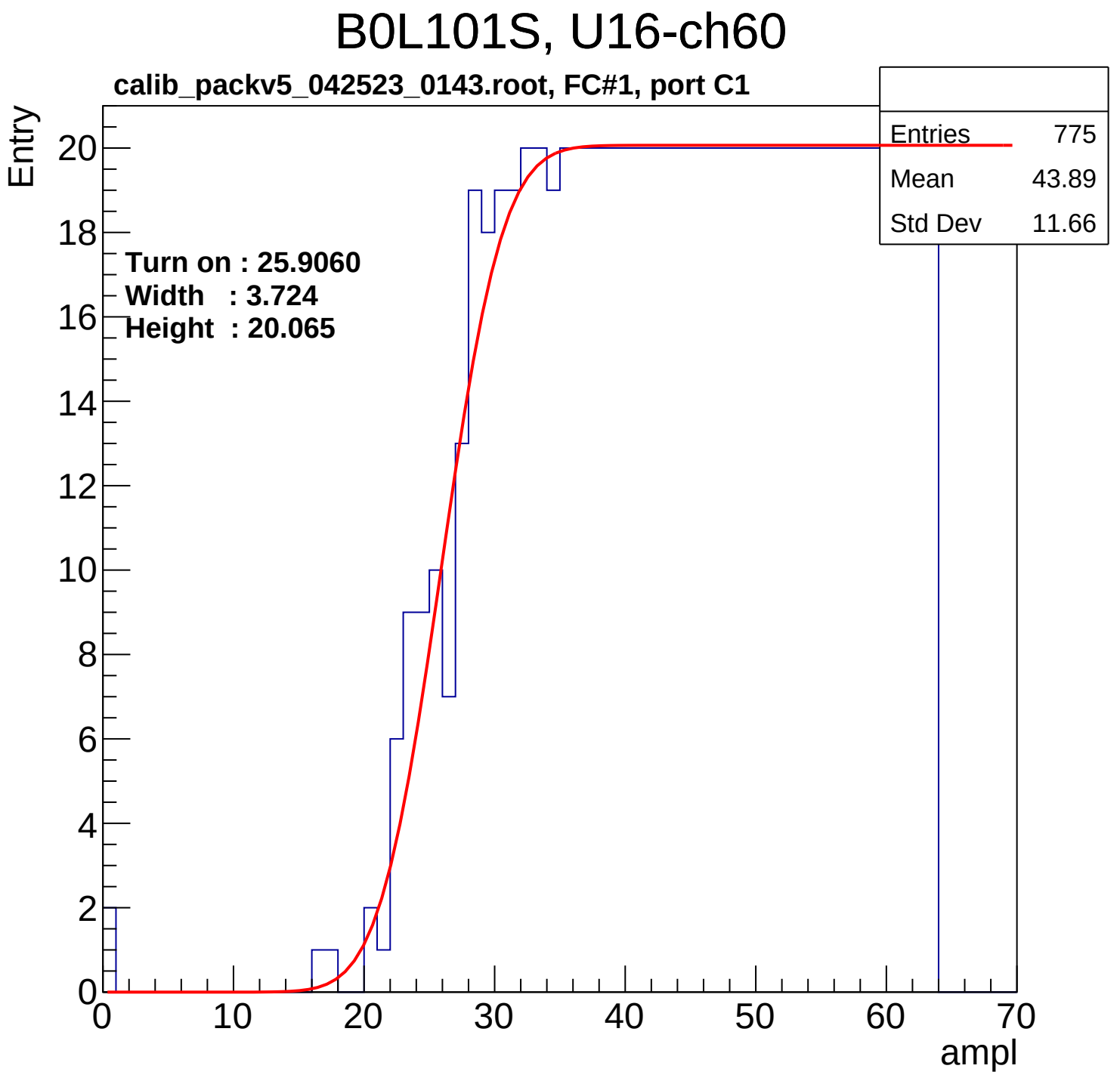
B0L101S, U16-ch60
calib_packv5_042523_0143.root, FC#1, port C1
Entries 775
Mean 43.89
Std Dev 11.66
Turn on : 25.9060
Width : 3.724
Height : 20.065
Entry
ampl
0
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6
8
10
12
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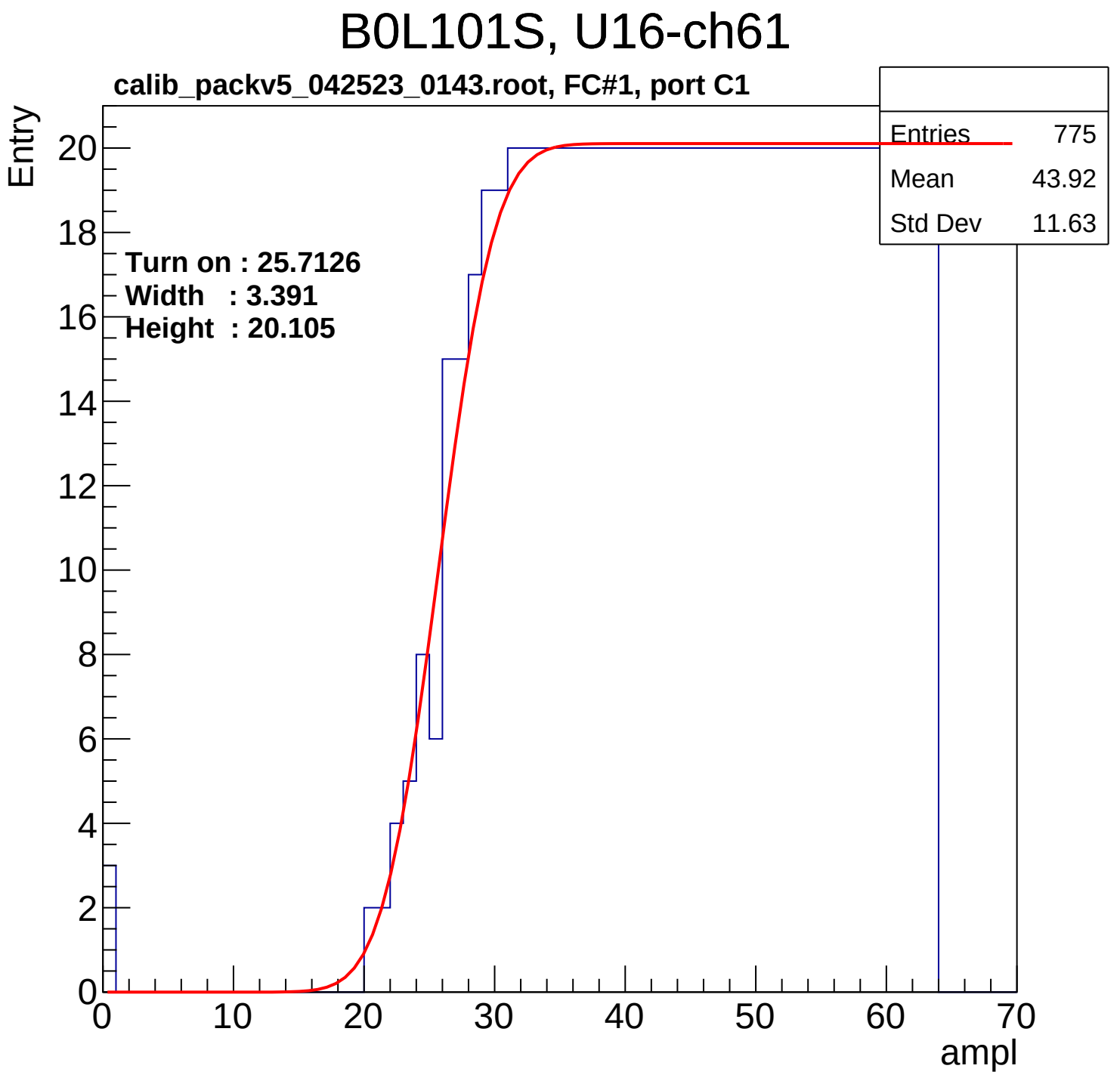
B0L101S, U16-ch61
calib_packv5_042523_0143.root, FC#1, port C1
Entries 775
Mean 43.92
Std Dev 11.63
Turn on : 25.7126
Width : 3.391
Height : 20.105
Entry
ampl
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6
8
10
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14
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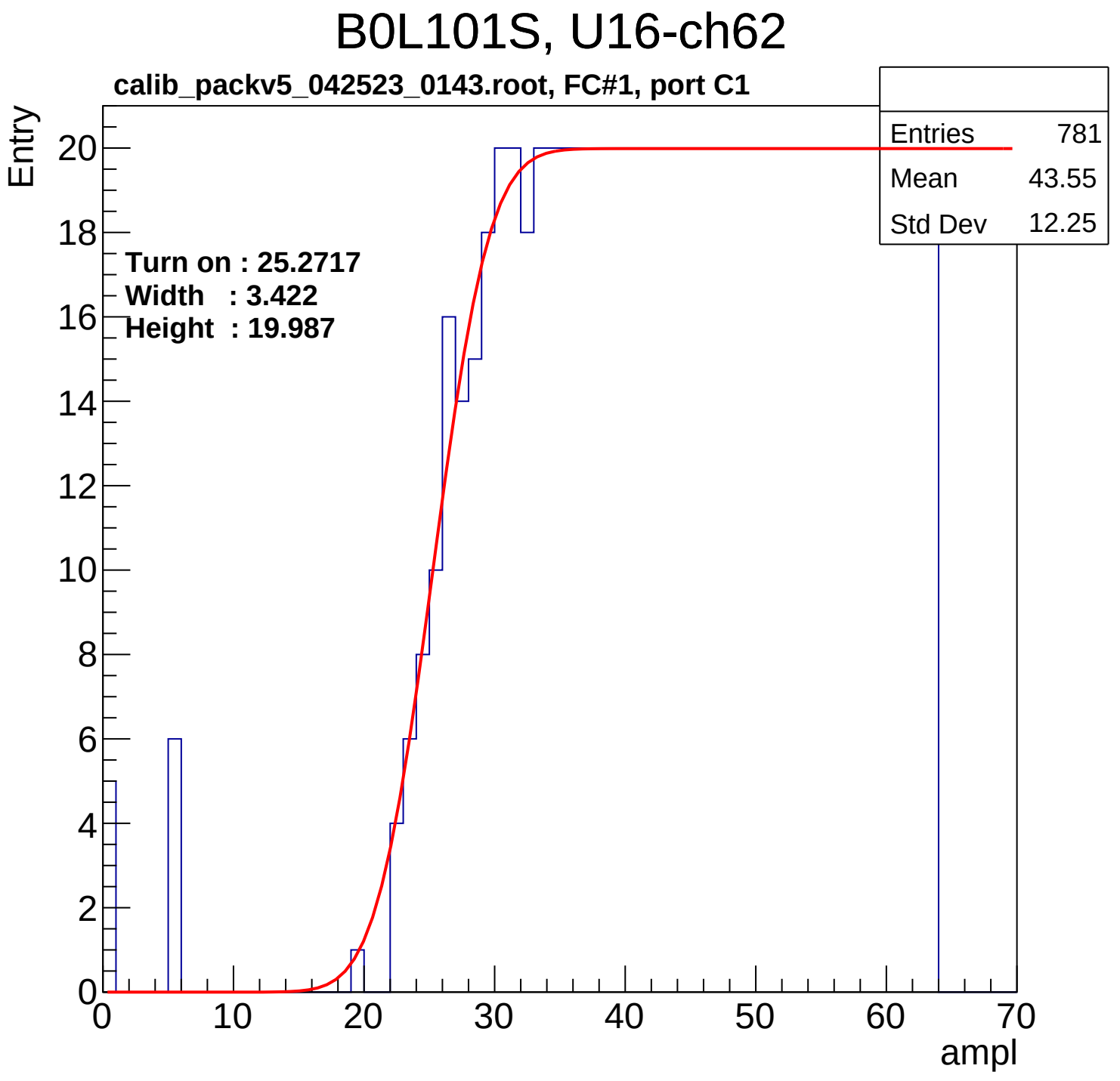
B0L101S, U16-ch62
calib_packv5_042523_0143.root, FC#1, port C1
Entries 781
Mean 43.55
Std Dev 12.25
Turn on : 25.2717
Width : 3.422
Height : 19.987
Entry
ampl
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6
8
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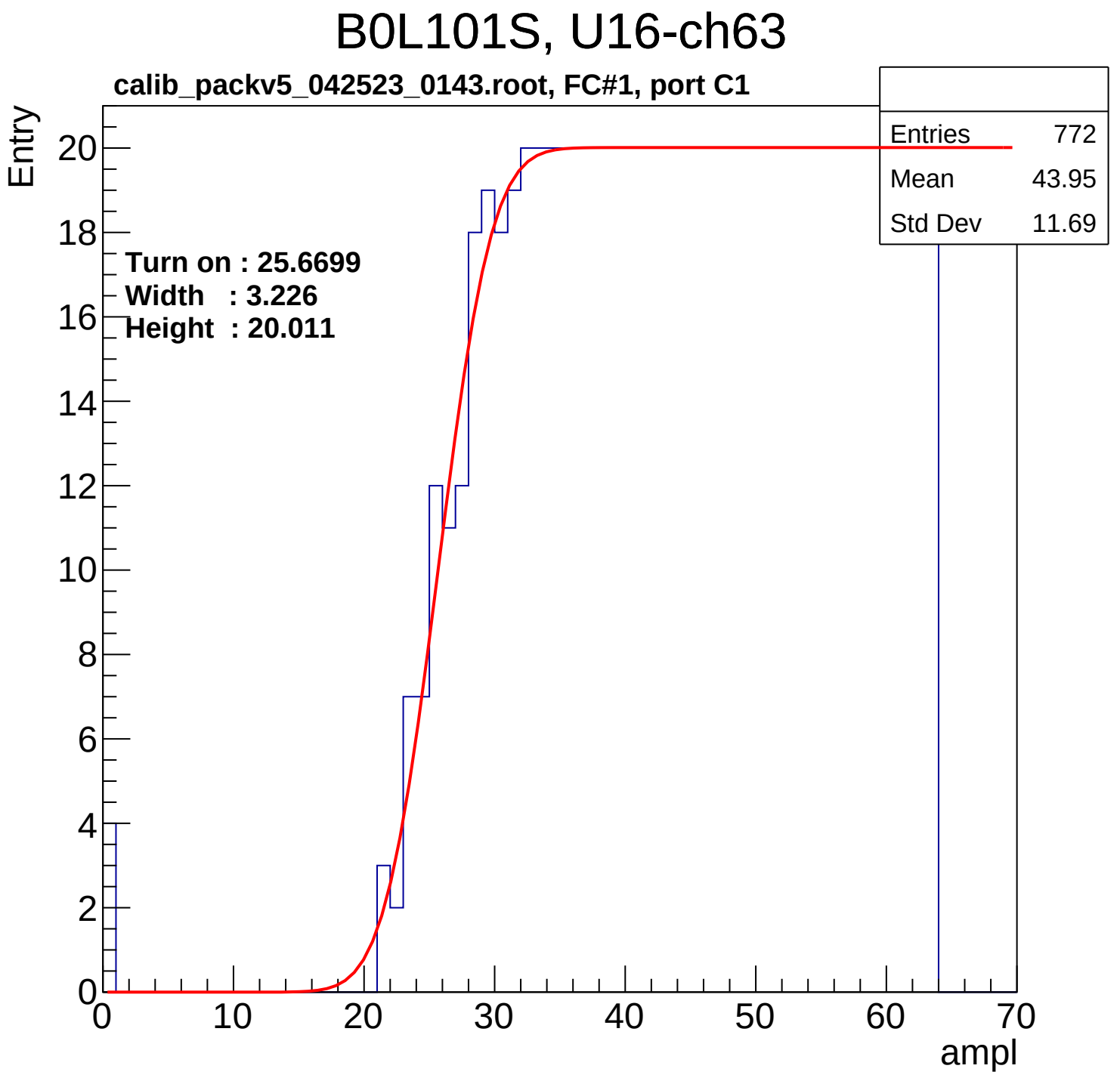
B0L101S, U16-ch63
calib_packv5_042523_0143.root, FC#1, port C1
Entries 772
Mean 43.95
Std Dev 11.69
Turn on : 25.6699
Width : 3.226
Height : 20.011
Entry
ampl
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6
8
10
12
14
16
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0
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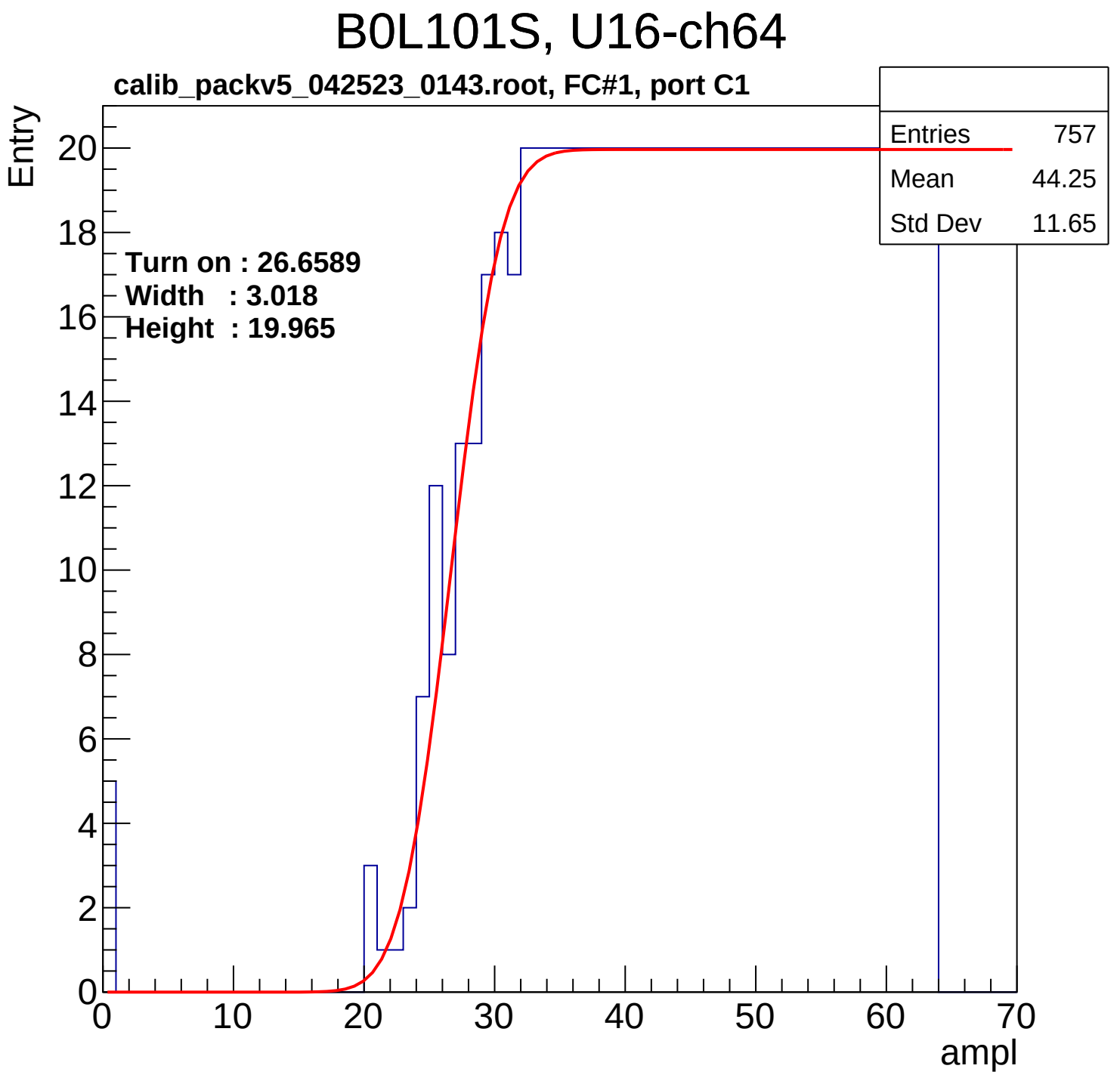
B0L101S, U16-ch64
calib_packv5_042523_0143.root, FC#1, port C1
Entries 757
Mean 44.25
Std Dev 11.65
Turn on : 26.6589
Width : 3.018
Height : 19.965
Entry
ampl
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6
8
10
12
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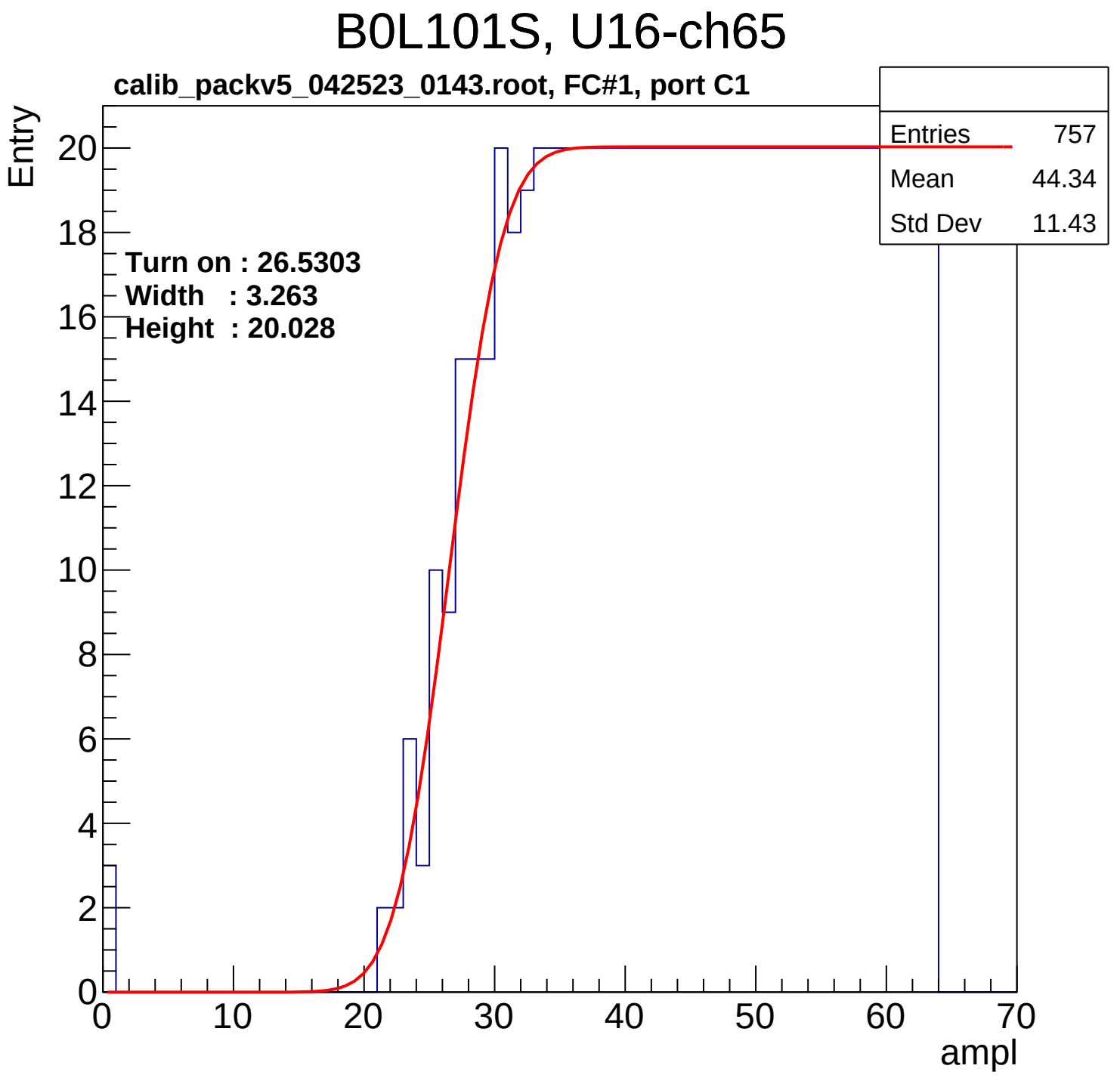
B0L101S, U16-ch65
calib_packv5_042523_0143.root, FC#1, port C1
Entries 757
Mean 44.34
Std Dev 11.43
Turn on : 26.5303
Width : 3.263
Height : 20.028
Entry
ampl
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6
8
10
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14
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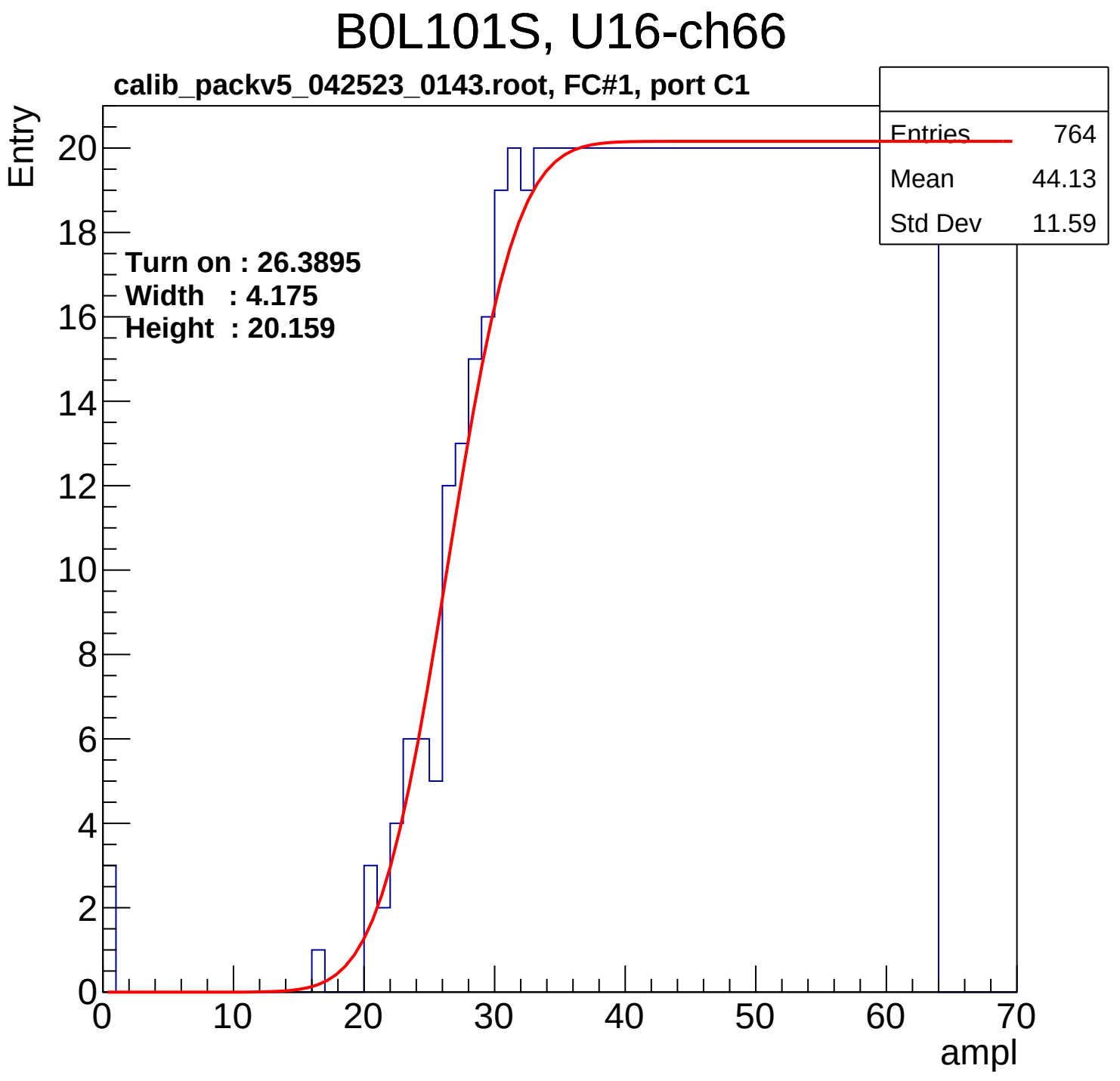
B0L101S, U16-ch66
calib_packv5_042523_0143.root, FC#1, port C1
Entries 764
Mean 44.13
Std Dev 11.59
Turn on : 26.3895
Width : 4.175
Height : 20.159
Entry
ampl
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6
8
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12
14
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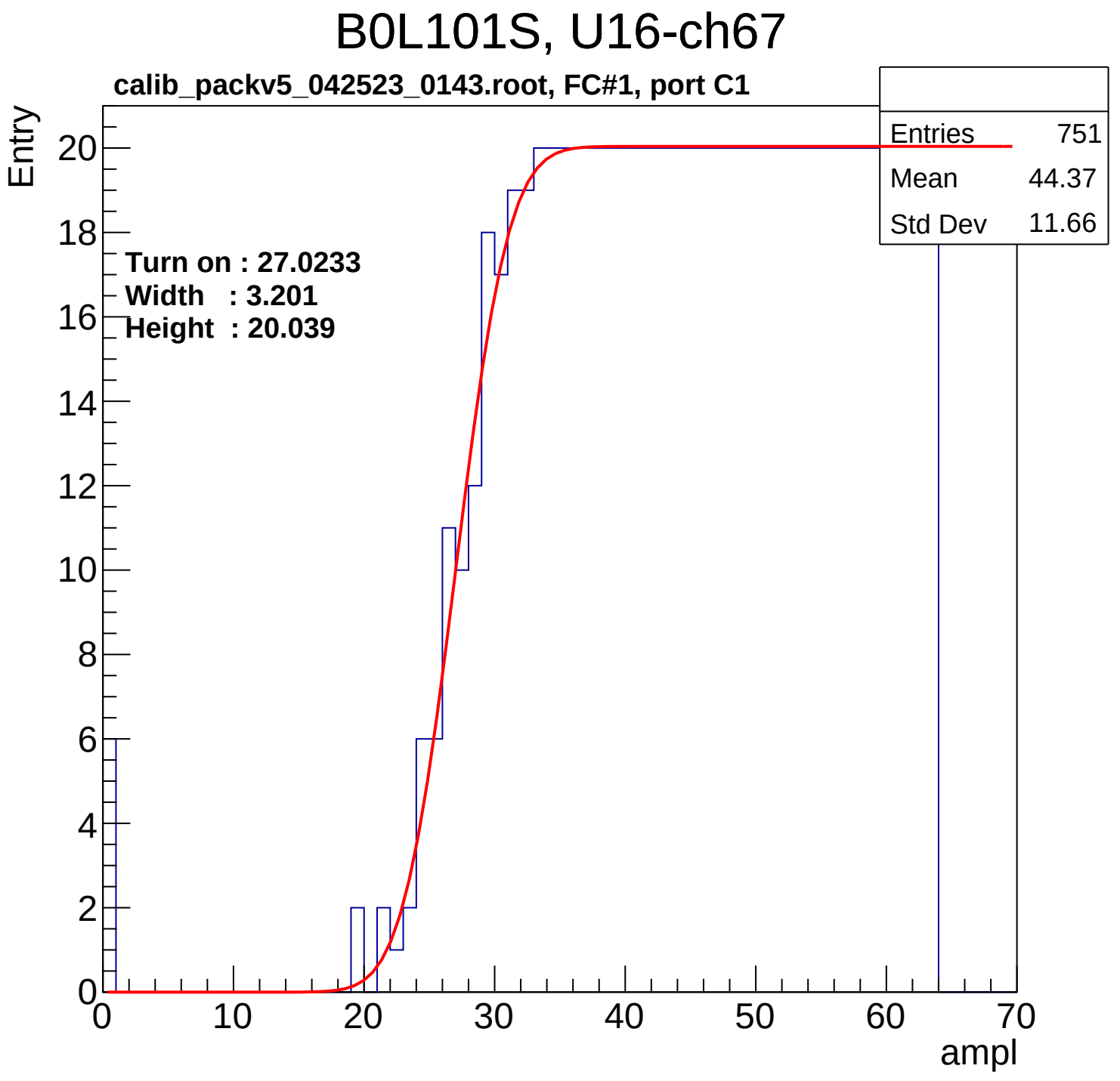
B0L101S, U16-ch67
calib_packv5_042523_0143.root, FC#1, port C1
Entries 751
Mean 44.37
Std Dev 11.66
Turn on : 27.0233
Width : 3.201
Height : 20.039
Entry
ampl
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6
8
10
12
14
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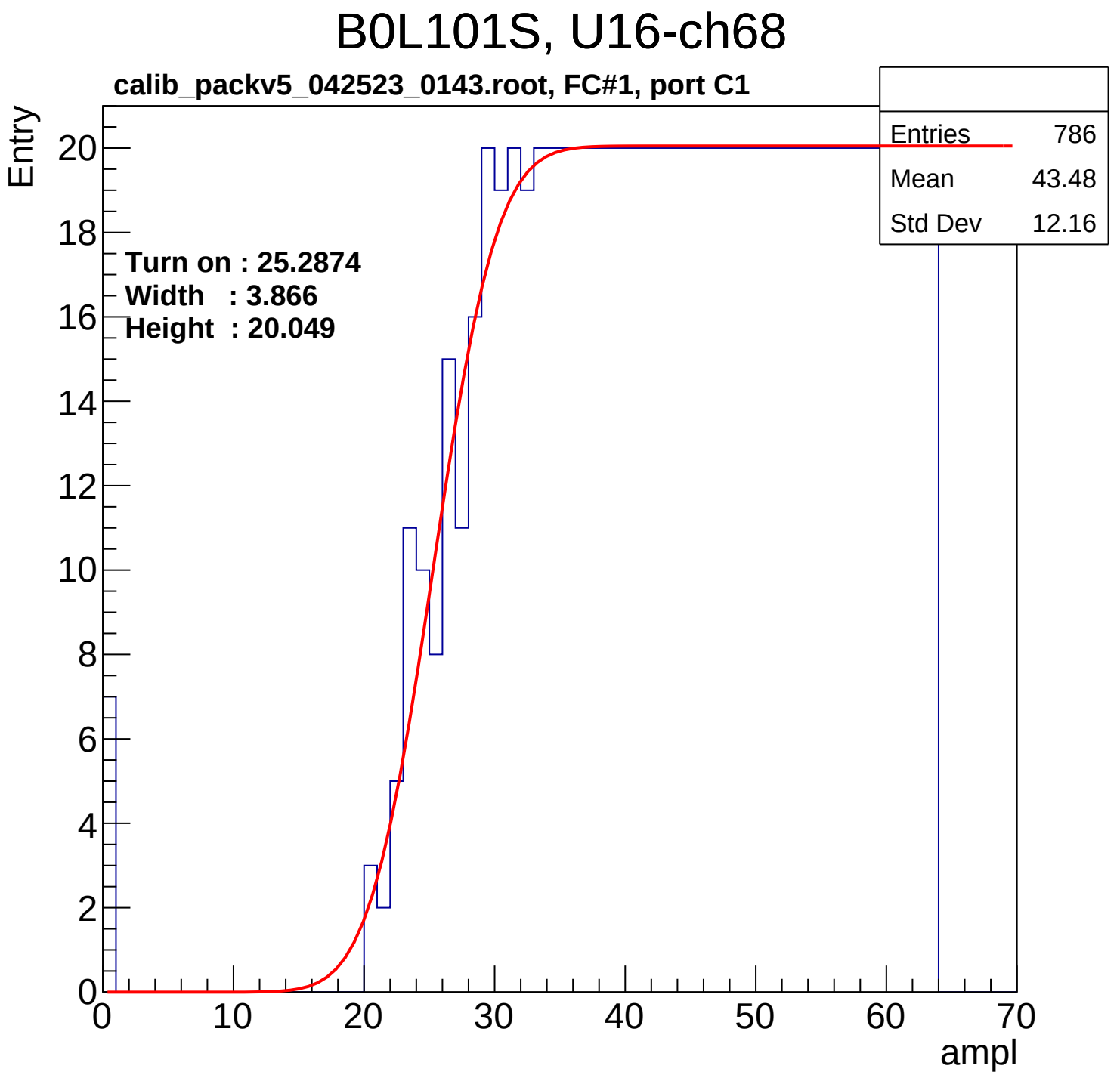
B0L101S, U16-ch68
calib_packv5_042523_0143.root, FC#1, port C1
Entries 786
Mean 43.48
Std Dev 12.16
Turn on : 25.2874
Width : 3.866
Height : 20.049
Entry
ampl
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8
10
12
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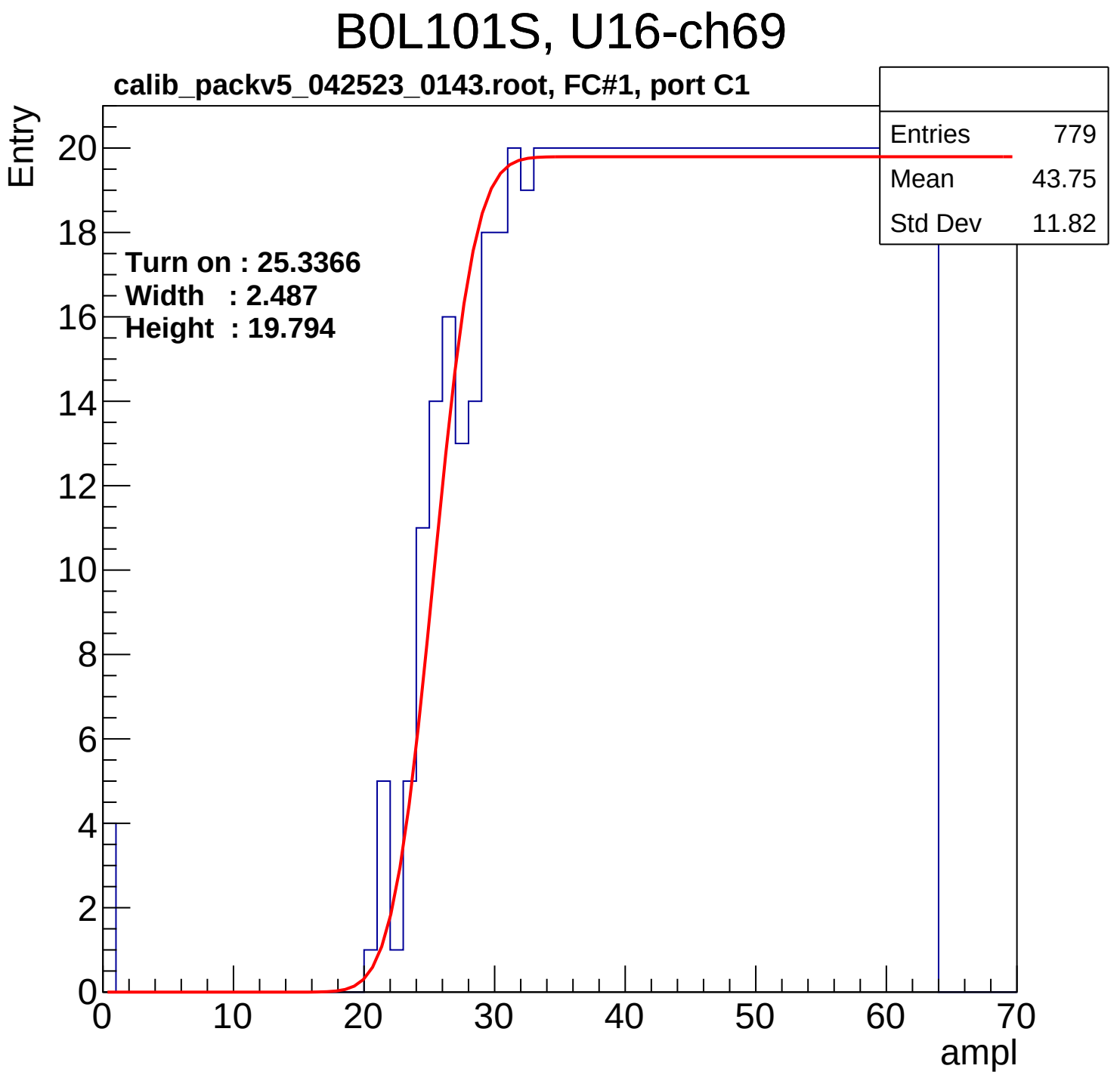
B0L101S, U16-ch69
calib_packv5_042523_0143.root, FC#1, port C1
Entries 779
Mean 43.75
Std Dev 11.82
Turn on : 25.3366
Width : 2.487
Height : 19.794
Entry
ampl
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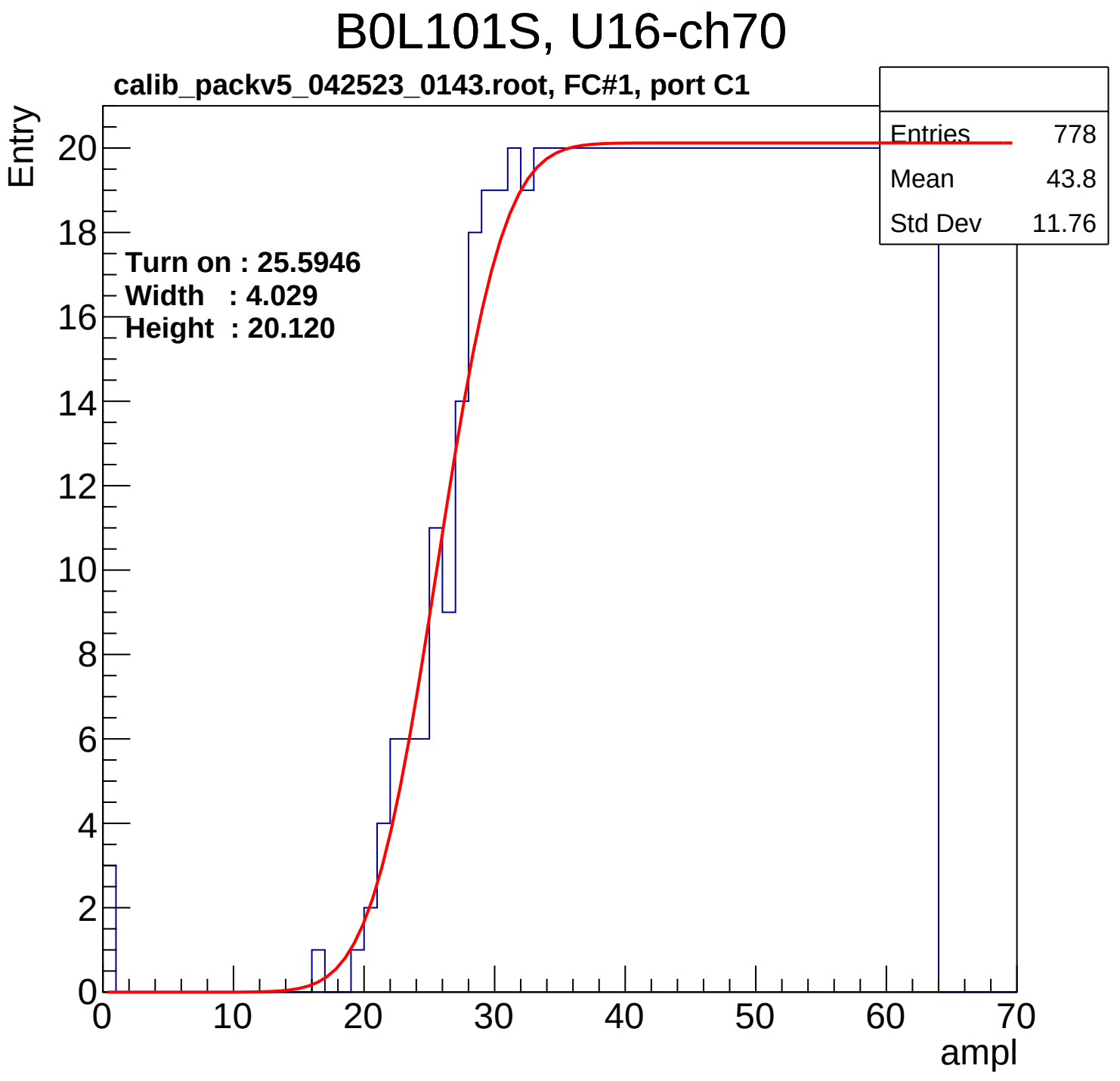
B0L101S, U16-ch70
calib_packv5_042523_0143.root, FC#1, port C1
Entries 778
Mean 43.8
Std Dev 11.76
Turn on : 25.5946
Width : 4.029
Height : 20.120
Entry
ampl
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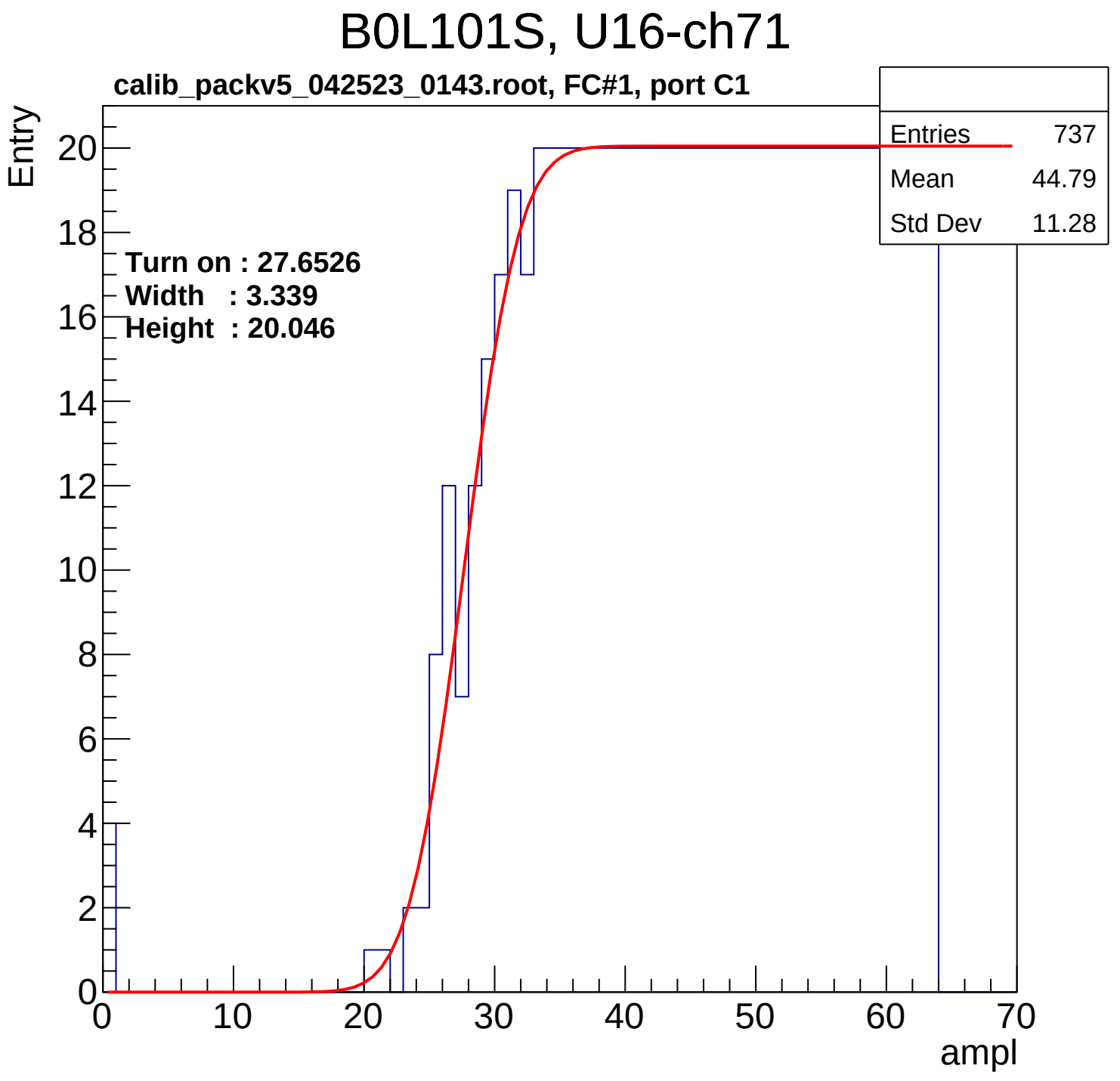
B0L101S, U16-ch71
calib_packv5_042523_0143.root, FC#1, port C1
Entries 737
Mean 44.79
Std Dev 11.28
Turn on : 27.6526
Width : 3.339
Height : 20.046
Entry
ampl
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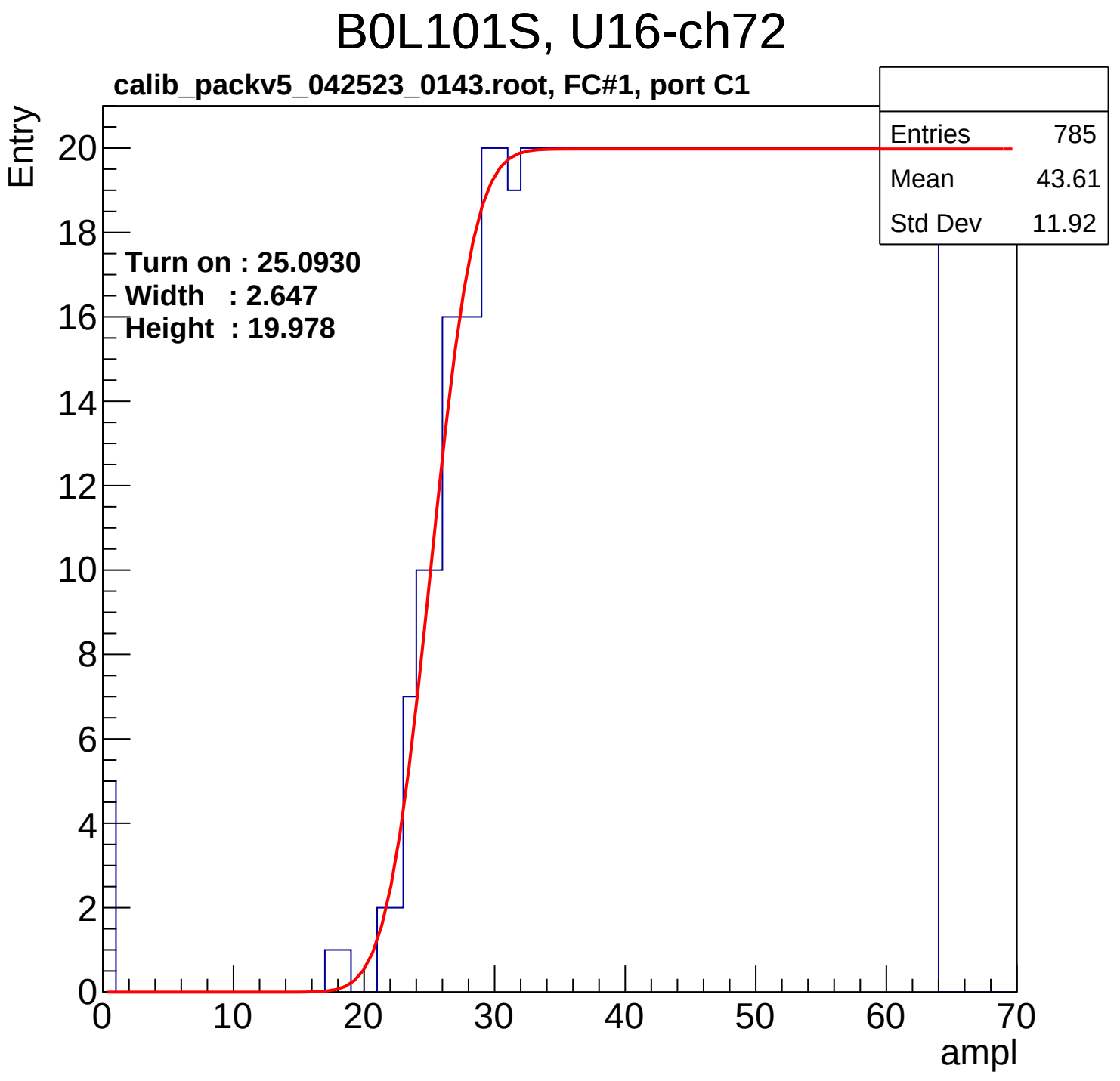
B0L101S, U16-ch72
calib_packv5_042523_0143.root, FC#1, port C1
Entries 785
Mean 43.61
Std Dev 11.92
Turn on : 25.0930
Width : 2.647
Height : 19.978
Entry
ampl
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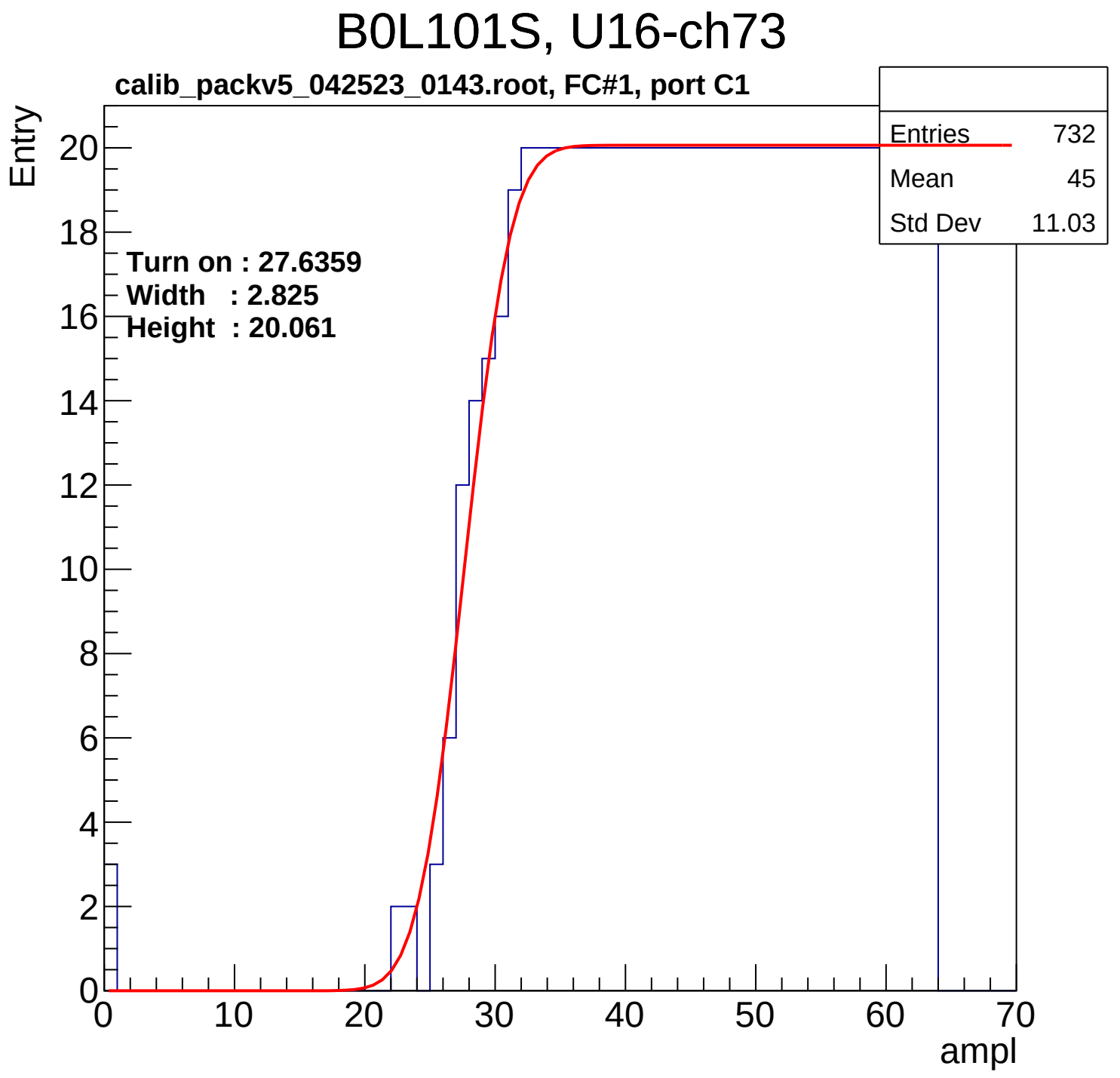
B0L101S, U16-ch73
calib_packv5_042523_0143.root, FC#1, port C1
Entries 732
Mean 45
Std Dev 11.03
Turn on : 27.6359
Width : 2.825
Height : 20.061
Entry
ampl
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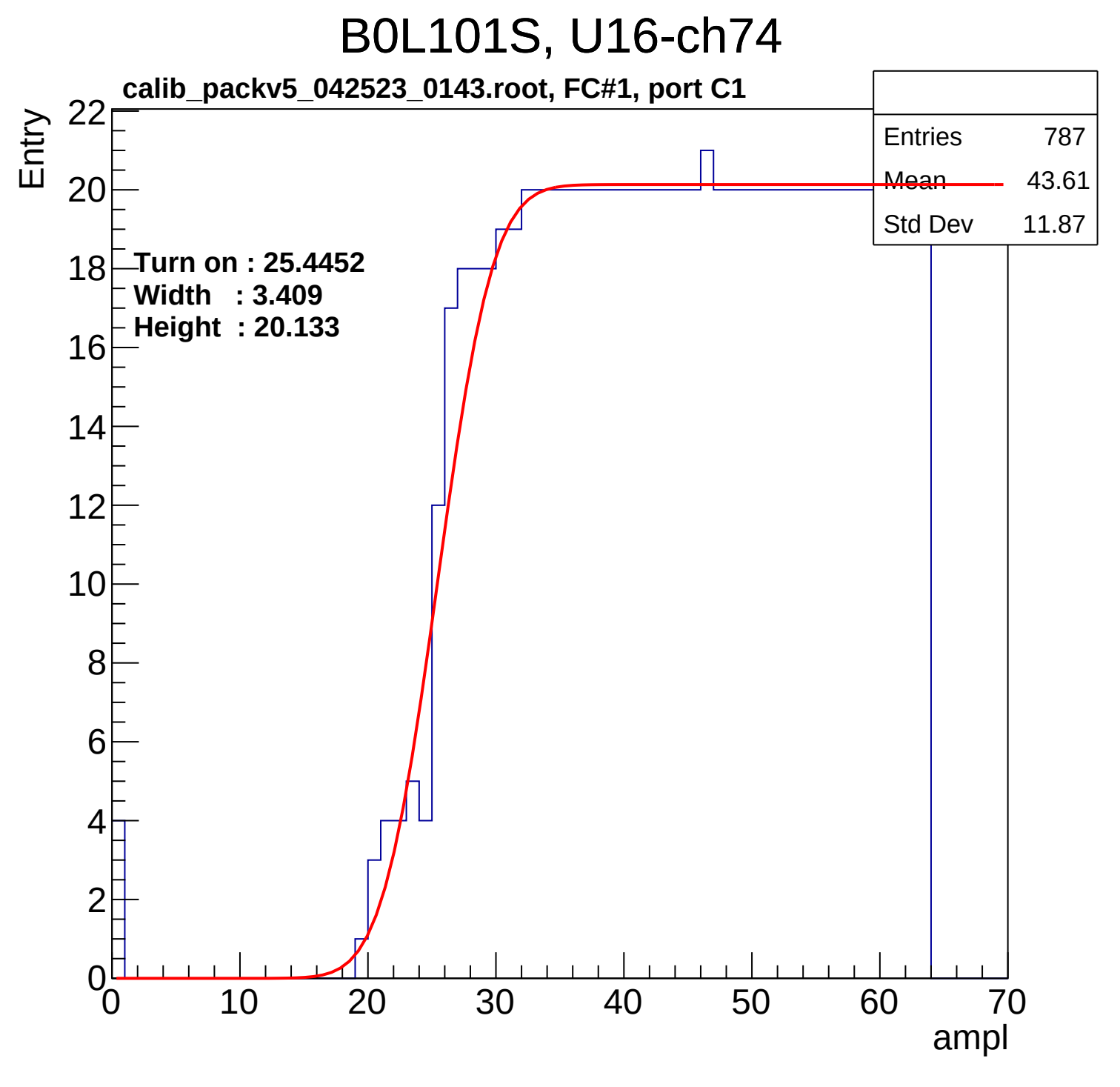
B0L101S, U16-ch74
calib_packv5_042523_0143.root, FC#1, port C1
Entries 787
Mean 43.61
Std Dev 11.87
Turn on : 25.4452
Width : 3.409
Height : 20.133
Entry
ampl
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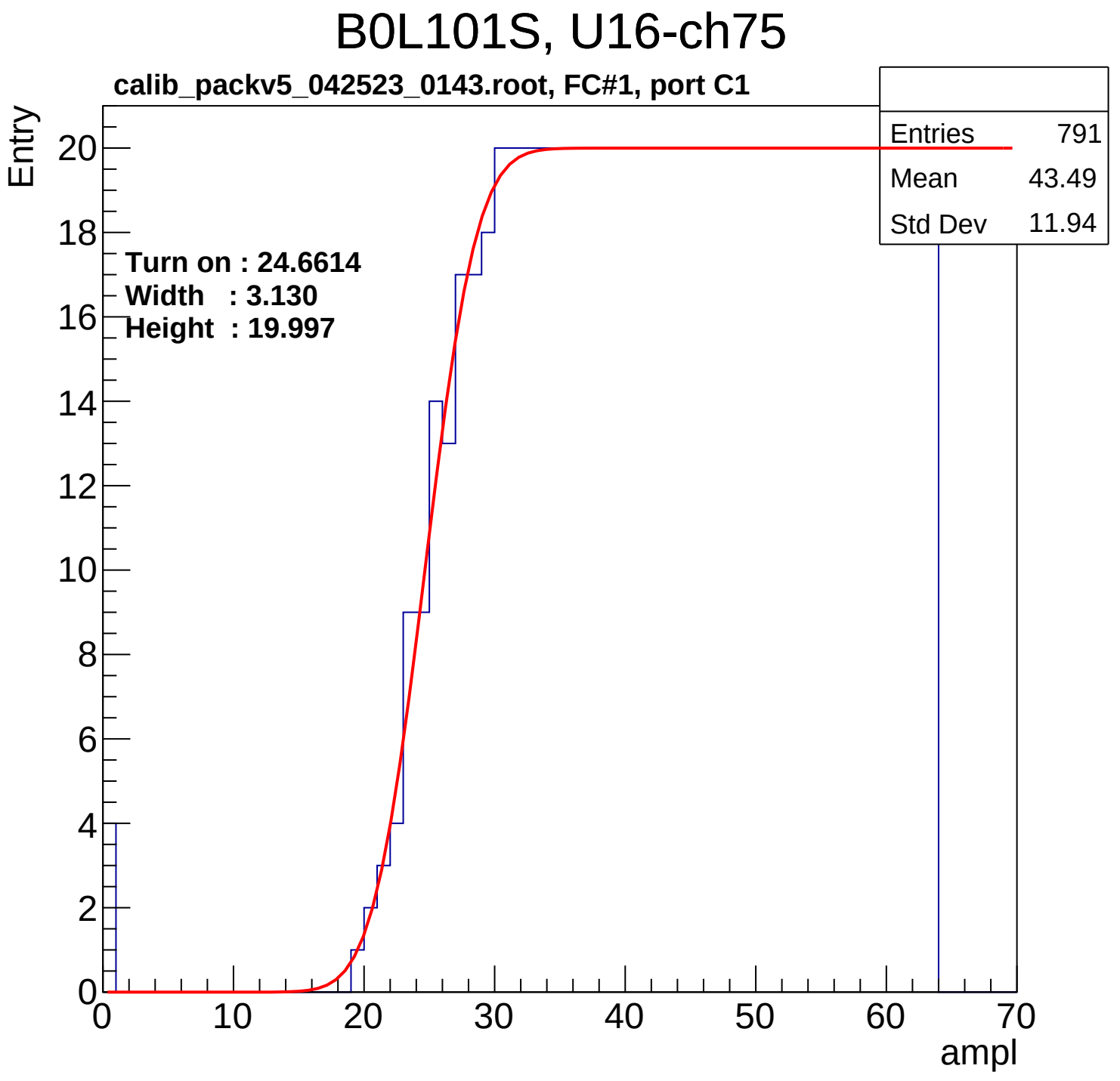
B0L101S, U16-ch75
calib_packv5_042523_0143.root, FC#1, port C1
Entries 791
Mean 43.49
Std Dev 11.94
Turn on : 24.6614
Width : 3.130
Height : 19.997
Entry
ampl
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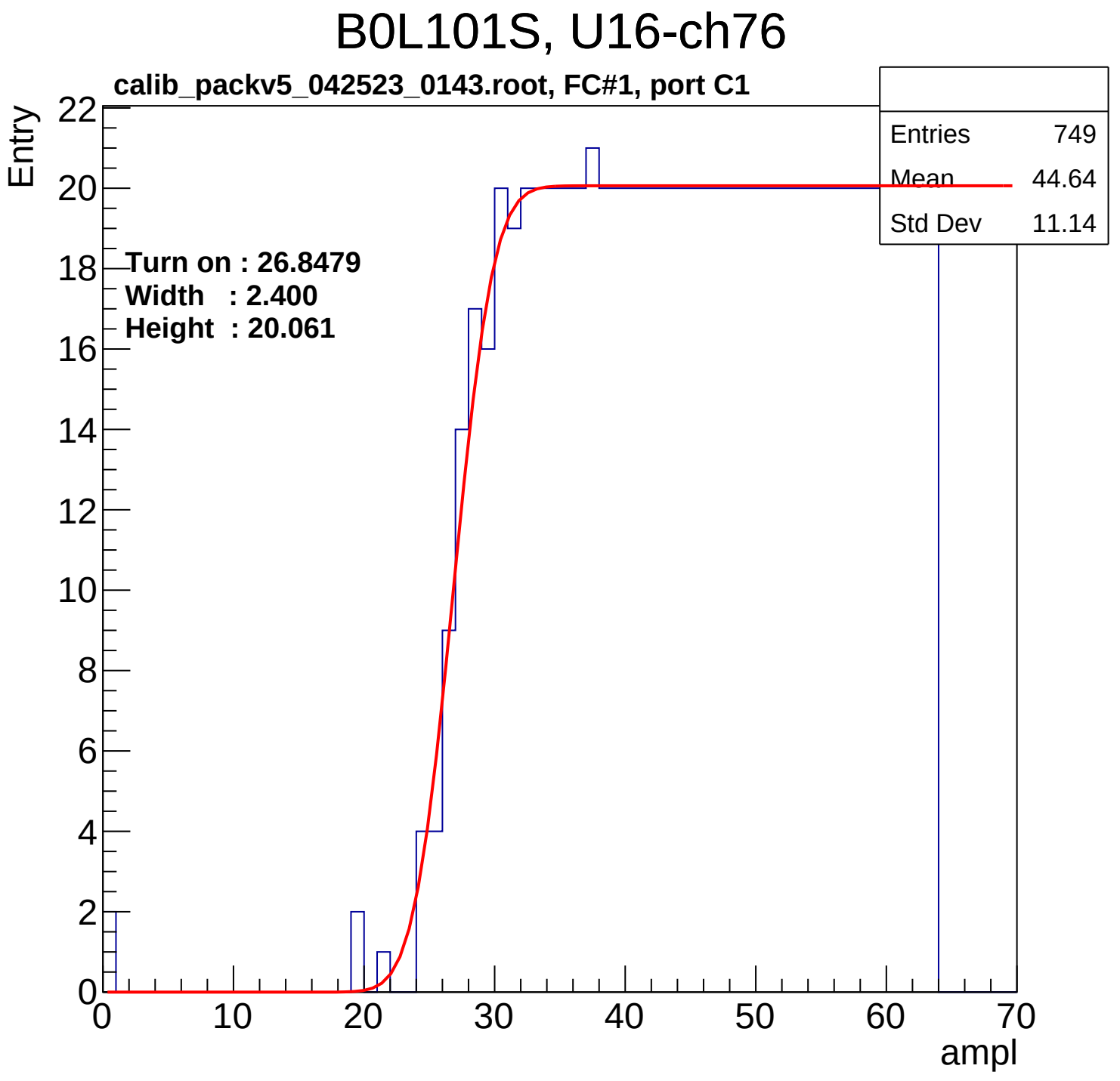
B0L101S, U16-ch76
calib_packv5_042523_0143.root, FC#1, port C1
Entries 749
Mean 44.64
Std Dev 11.14
Turn on : 26.8479
Width : 2.400
Height : 20.061
Entry
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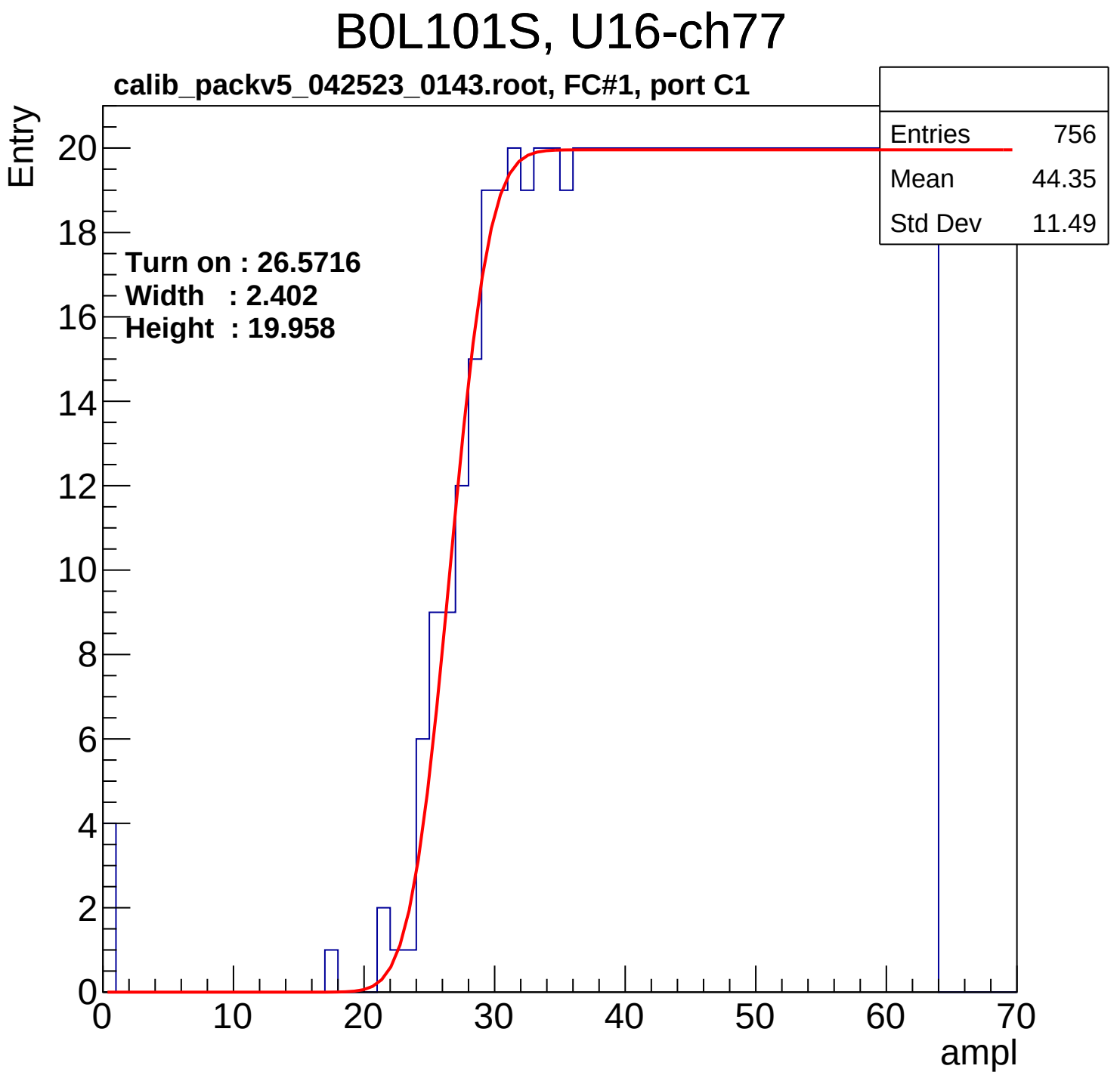
B0L101S, U16-ch77
calib_packv5_042523_0143.root, FC#1, port C1
Entries 756
Mean 44.35
Std Dev 11.49
Turn on : 26.5716
Width : 2.402
Height : 19.958
Entry
ampl
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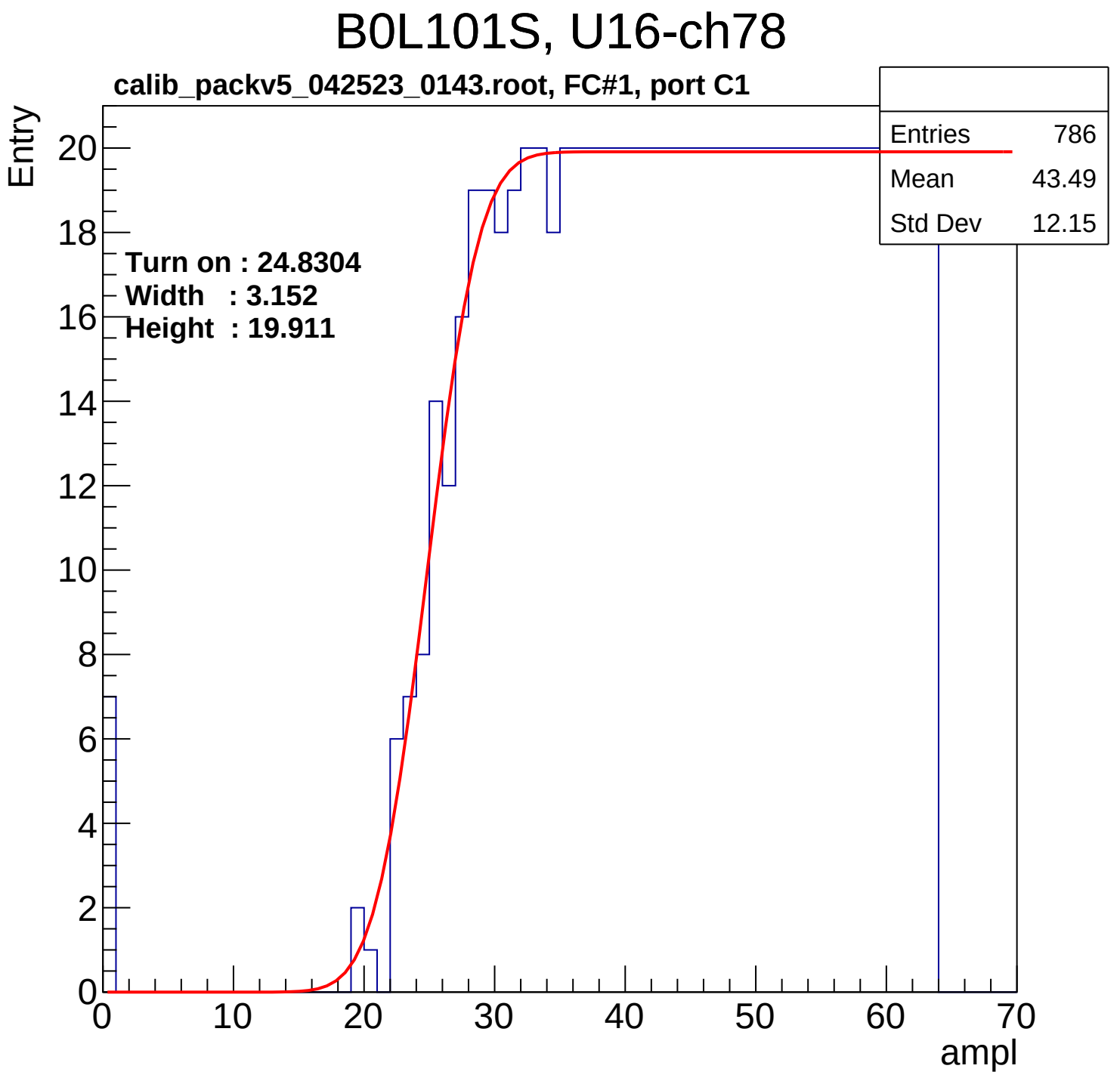
B0L101S, U16-ch78
calib_packv5_042523_0143.root, FC#1, port C1
Entries 786
Mean 43.49
Std Dev 12.15
Turn on : 24.8304
Width : 3.152
Height : 19.911
Entry
ampl
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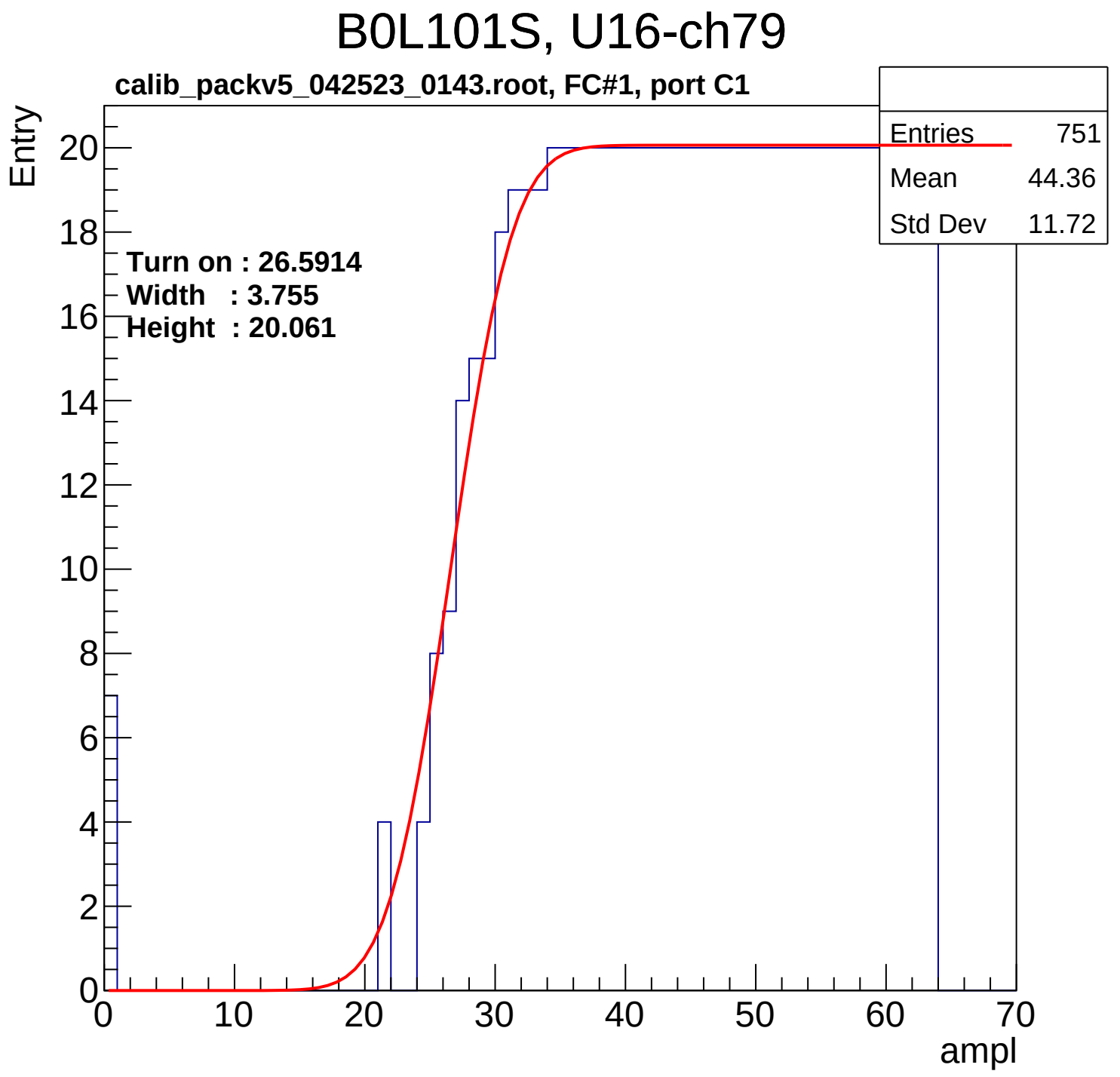
B0L101S, U16-ch79
calib_packv5_042523_0143.root, FC#1, port C1
Entries 751
Mean 44.36
Std Dev 11.72
Turn on : 26.5914
Width : 3.755
Height : 20.061
Entry
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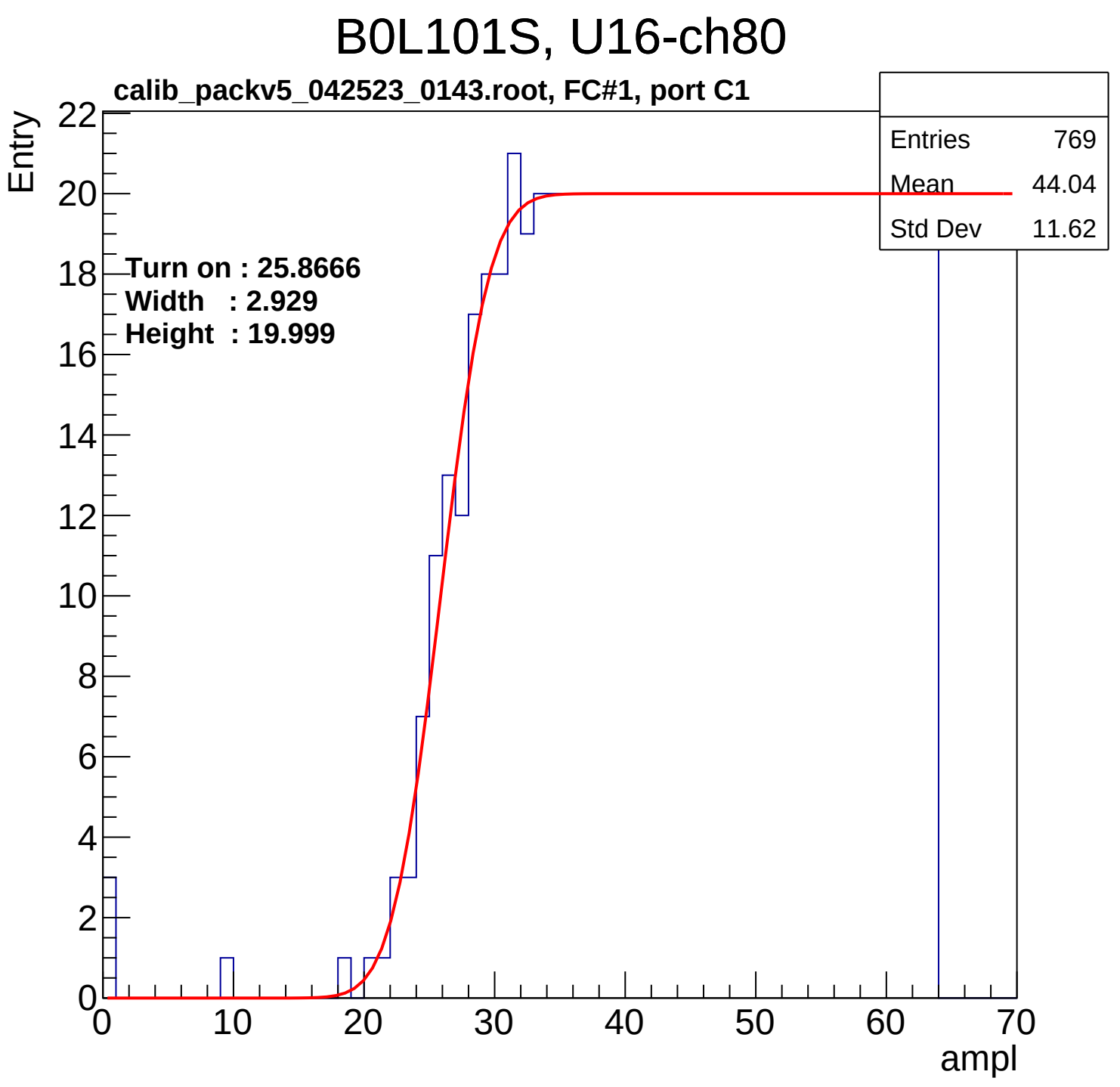
B0L101S, U16-ch80
calib_packv5_042523_0143.root, FC#1, port C1
Entries 769
Mean 44.04
Std Dev 11.62
Turn on : 25.8666
Width : 2.929
Height : 19.999
Entry
ampl
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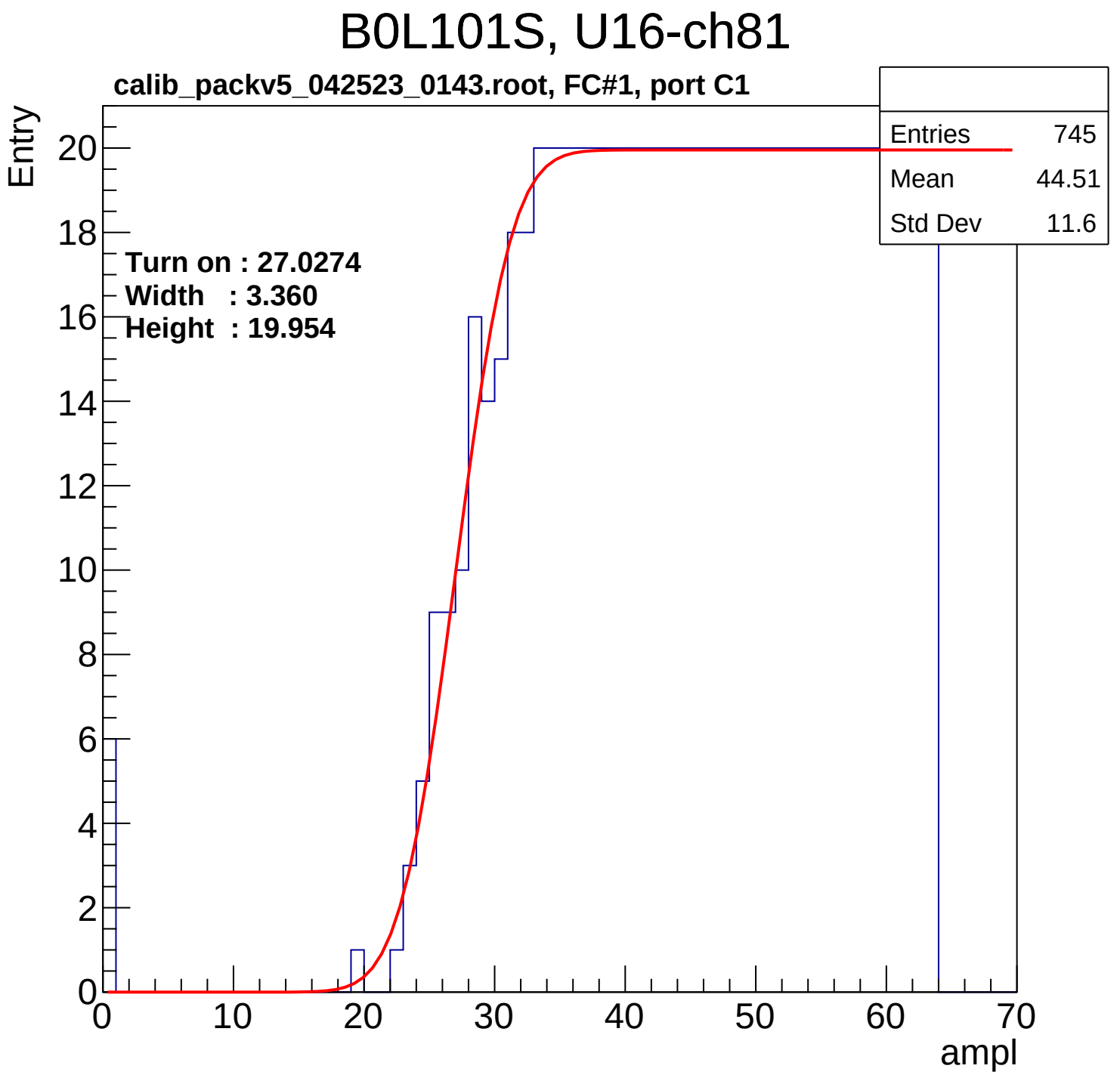
B0L101S, U16-ch81
calib_packv5_042523_0143.root, FC#1, port C1
Entries 745
Mean 44.51
Std Dev 11.6
Turn on : 27.0274
Width : 3.360
Height : 19.954
Entry
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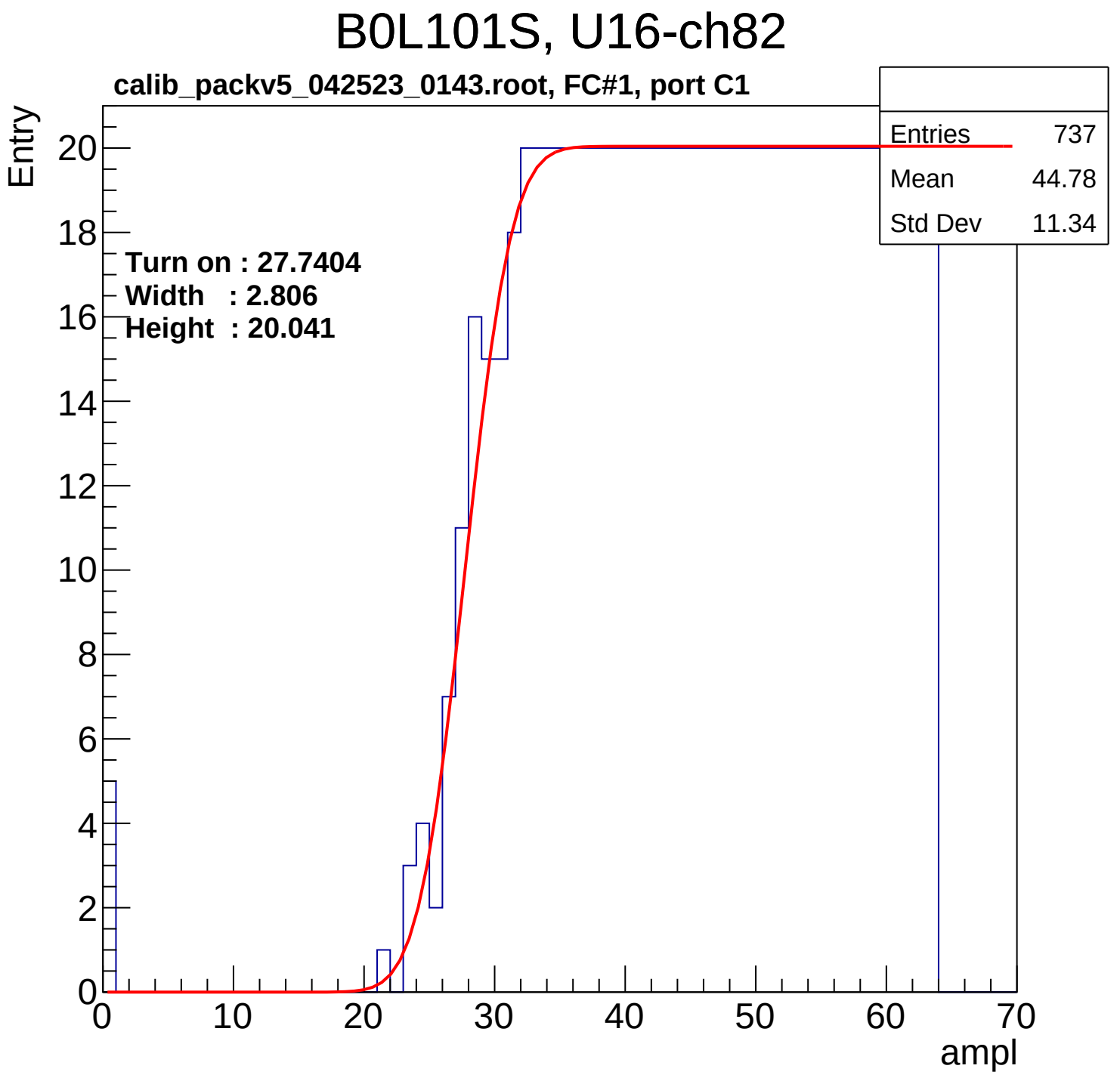
B0L101S, U16-ch82
calib_packv5_042523_0143.root, FC#1, port C1
Entries 737
Mean 44.78
Std Dev 11.34
Turn on : 27.7404
Width : 2.806
Height : 20.041
Entry
ampl
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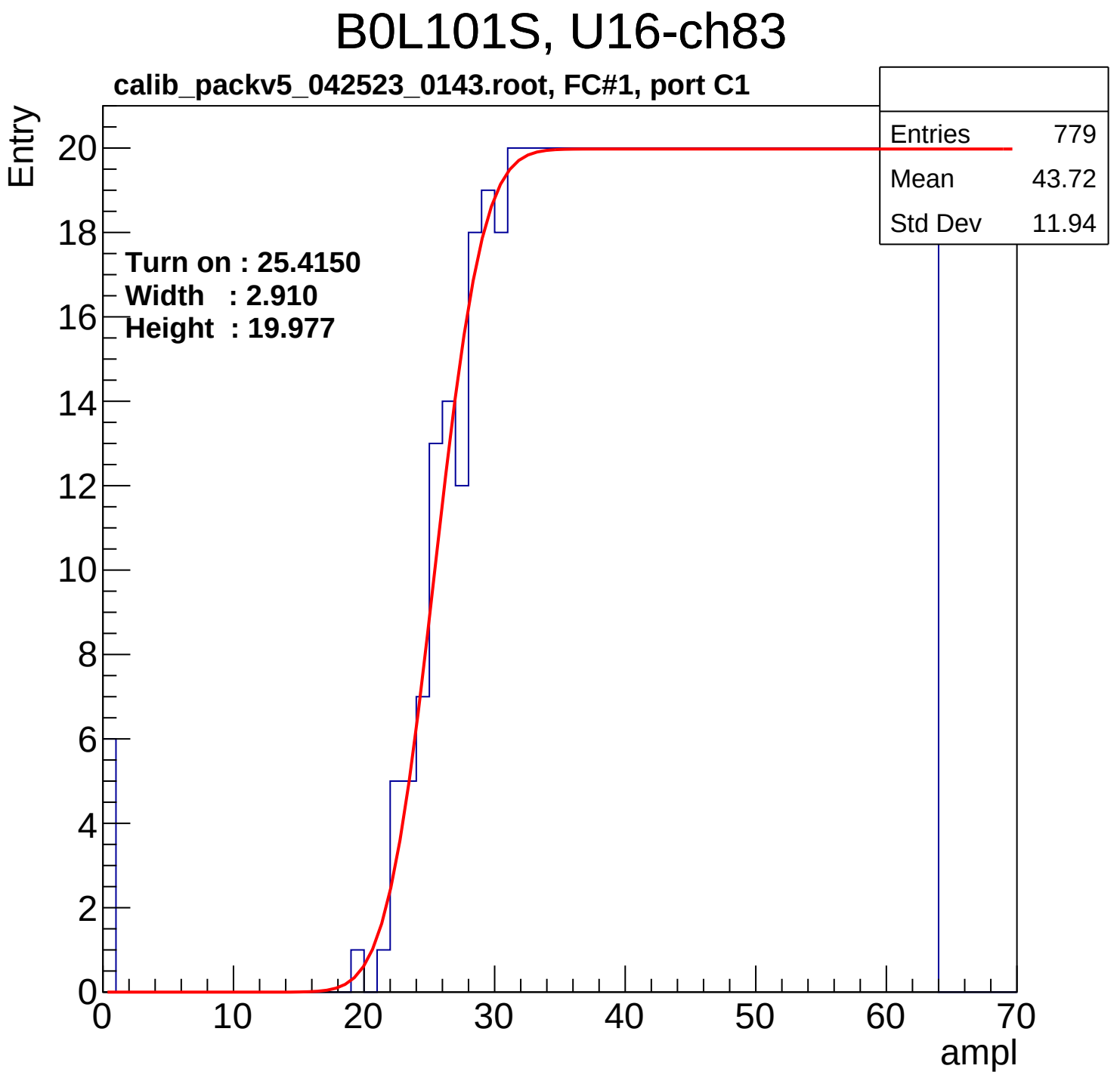
B0L101S, U16-ch83
calib_packv5_042523_0143.root, FC#1, port C1
Entries 779
Mean 43.72
Std Dev 11.94
Turn on : 25.4150
Width : 2.910
Height : 19.977
Entry
ampl
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2
4
6
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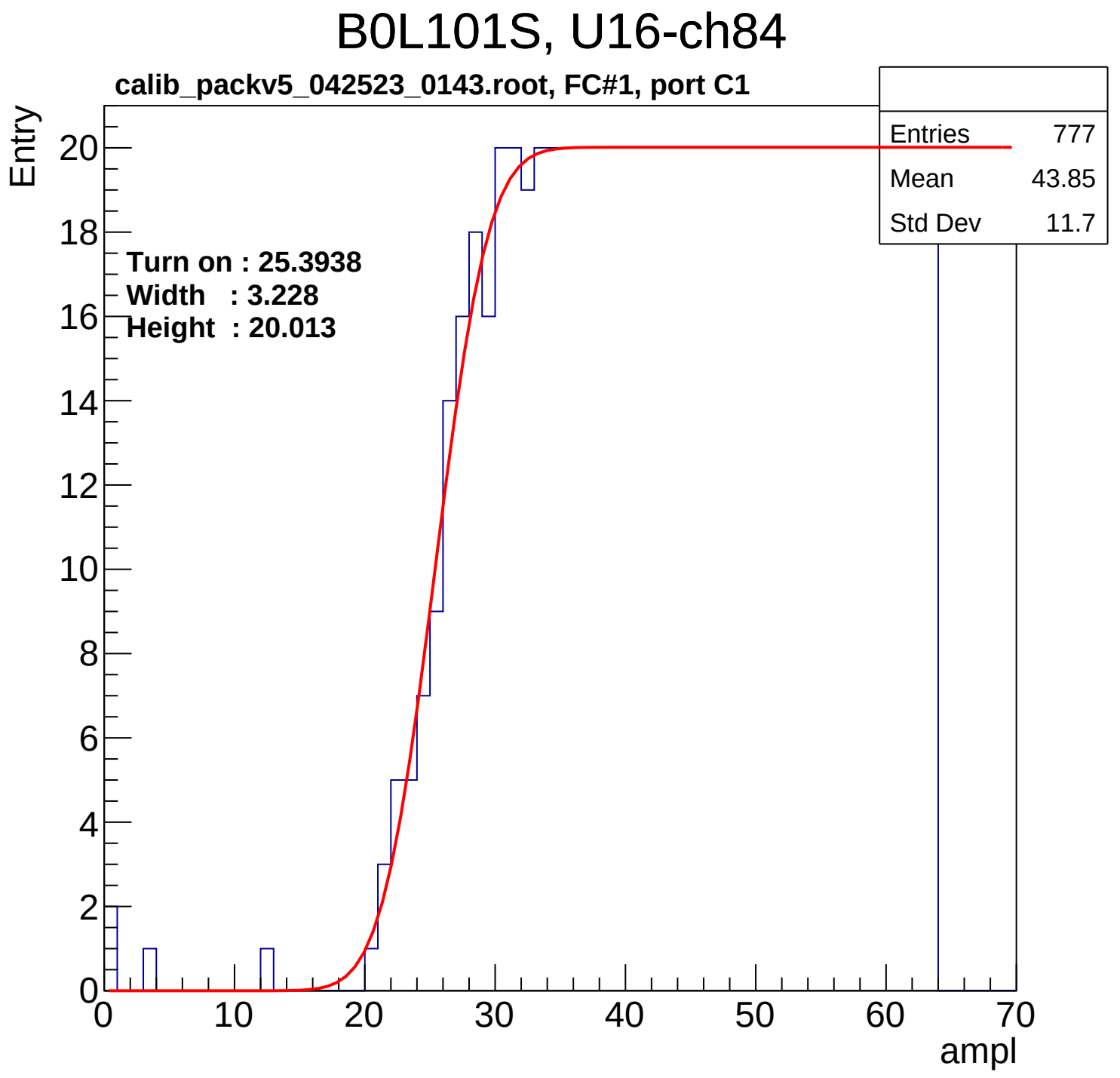
B0L101S, U16-ch84
calib_packv5_042523_0143.root, FC#1, port C1
Entries 777
Mean 43.85
Std Dev 11.7
Turn on : 25.3938
Width : 3.228
Height : 20.013
Entry
ampl
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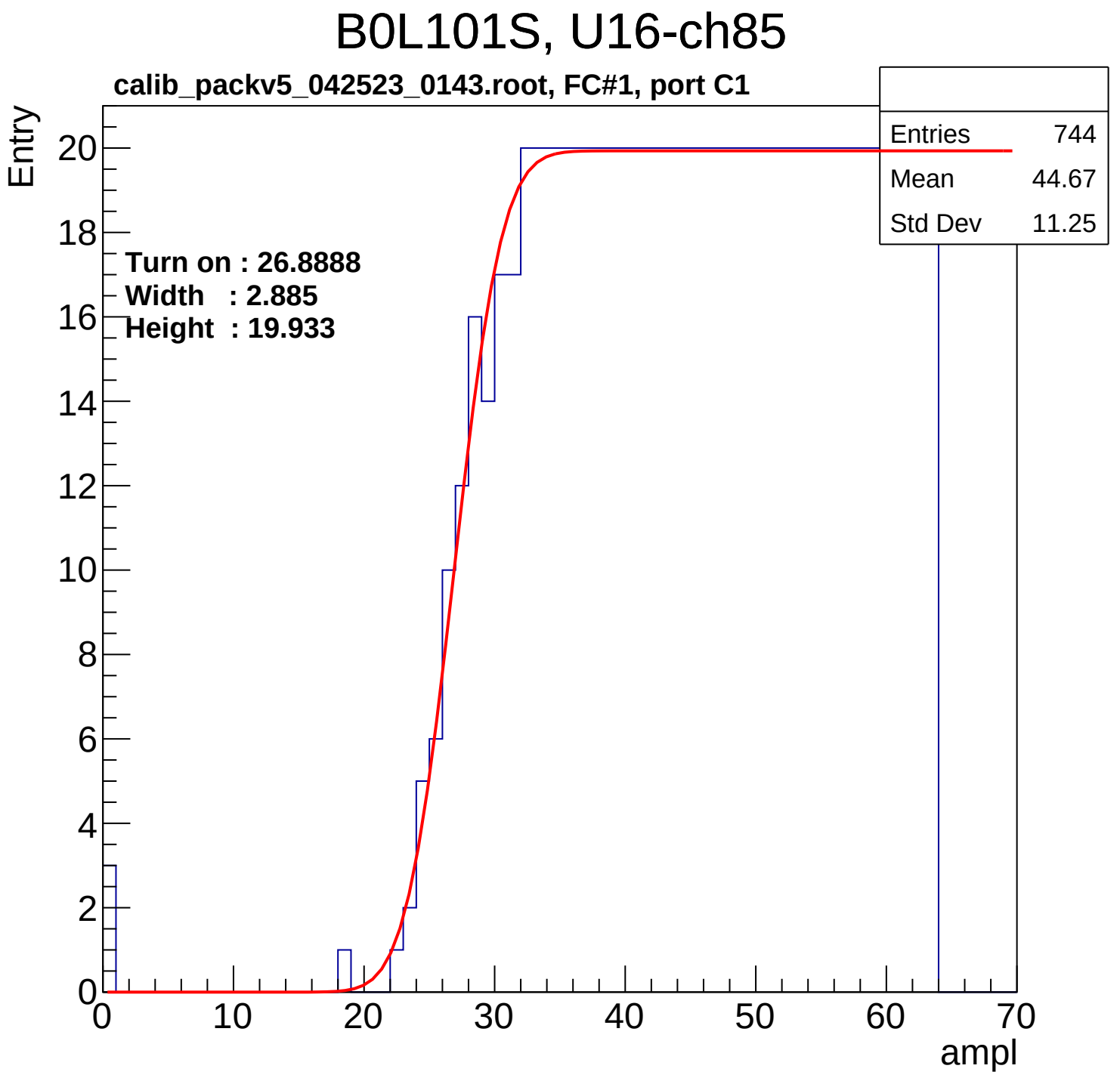
B0L101S, U16-ch85
calib_packv5_042523_0143.root, FC#1, port C1
Entries 744
Mean 44.67
Std Dev 11.25
Turn on : 26.8888
Width : 2.885
Height : 19.933
Entry
ampl
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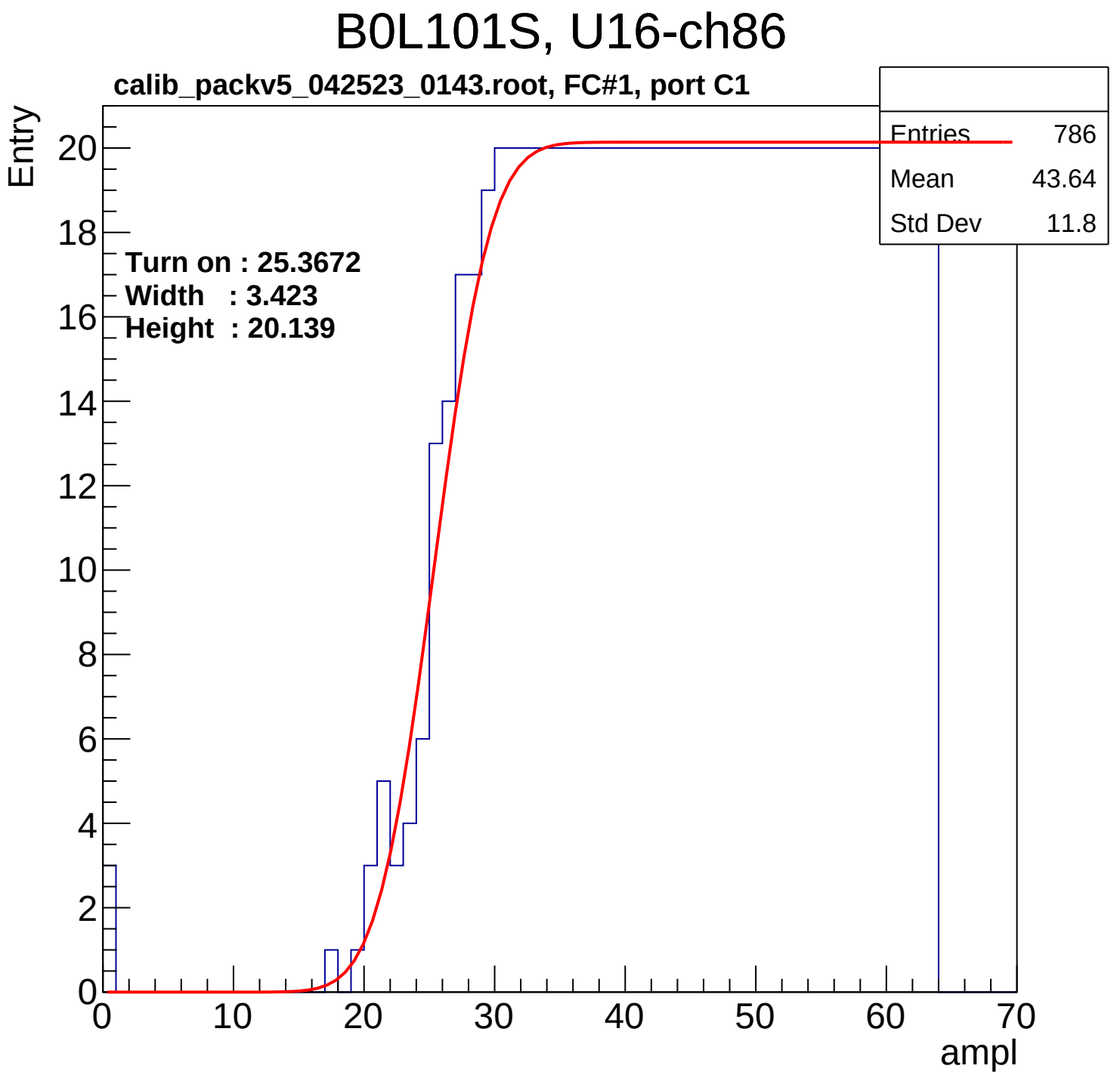
B0L101S, U16-ch86
calib_packv5_042523_0143.root, FC#1, port C1
Entries 786
Mean 43.64
Std Dev 11.8
Turn on : 25.3672
Width : 3.423
Height : 20.139
Entry
ampl
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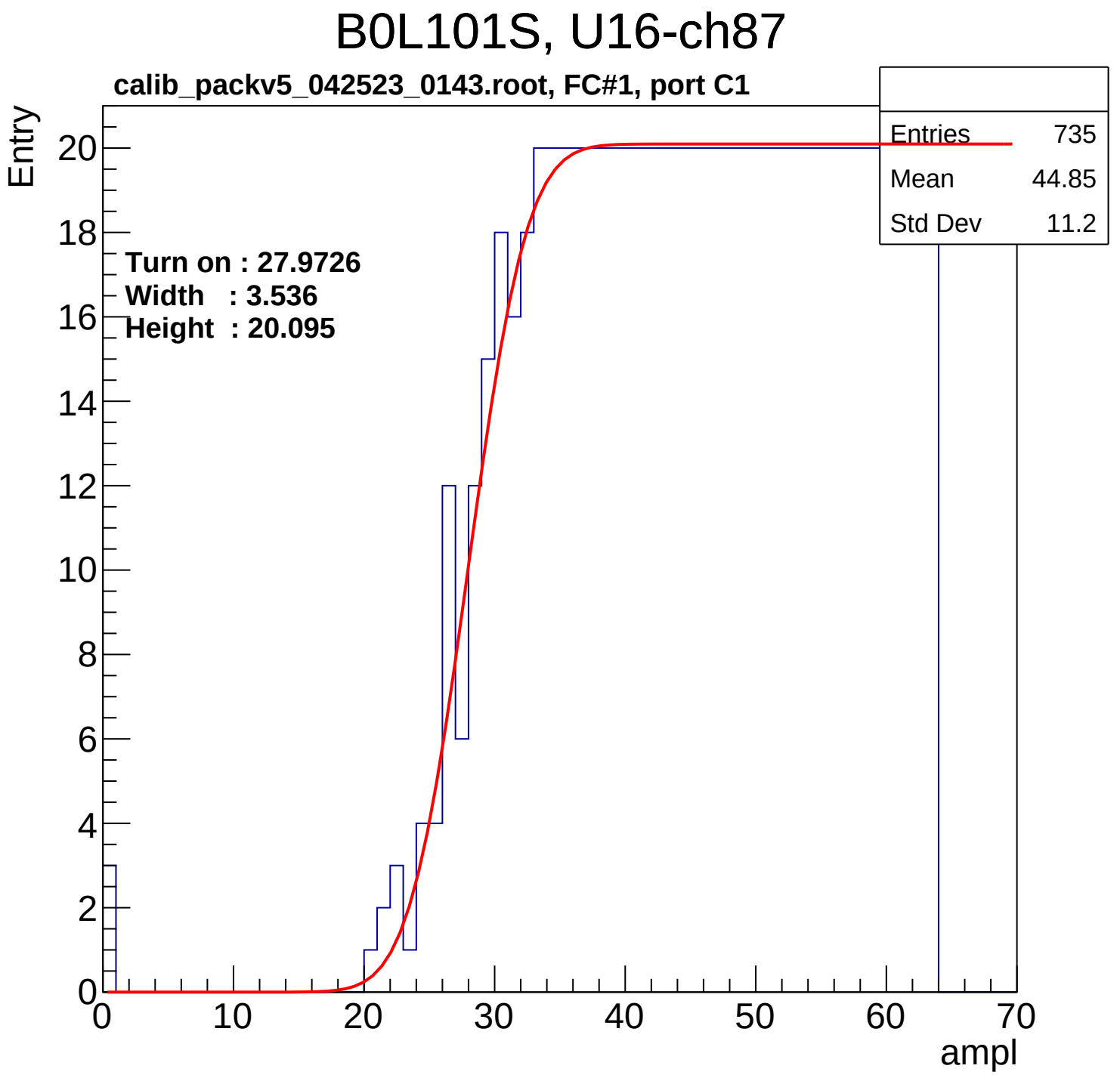
B0L101S, U16-ch87
calib_packv5_042523_0143.root, FC#1, port C1
Entries 735
Mean 44.85
Std Dev 11.2
Turn on : 27.9726
Width : 3.536
Height : 20.095
Entry
ampl
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6
8
10
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14
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0
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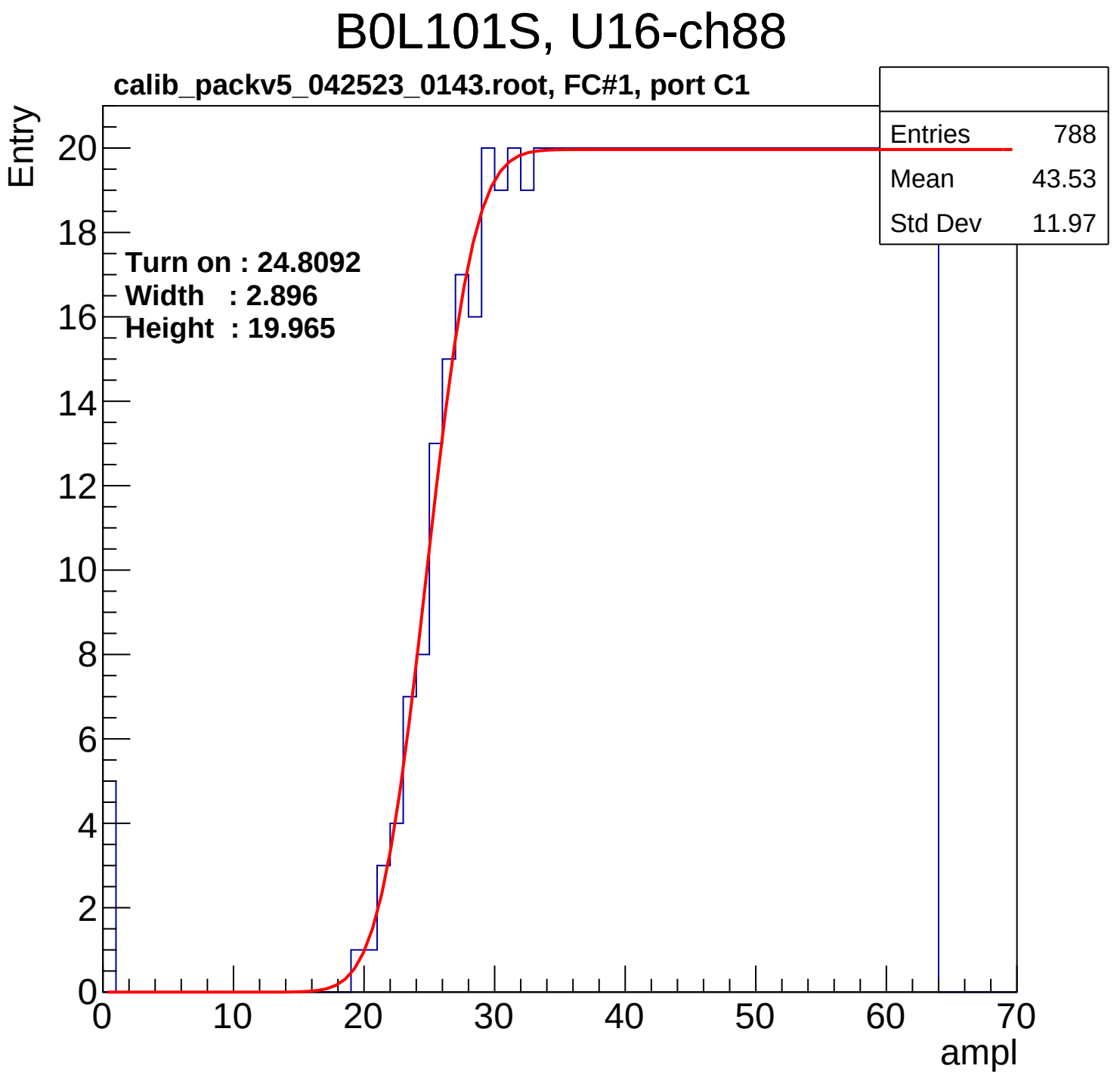
B0L101S, U16-ch88
calib_packv5_042523_0143.root, FC#1, port C1
Entries 788
Mean 43.53
Std Dev 11.97
Turn on : 24.8092
Width : 2.896
Height : 19.965
Entry
ampl
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6
8
10
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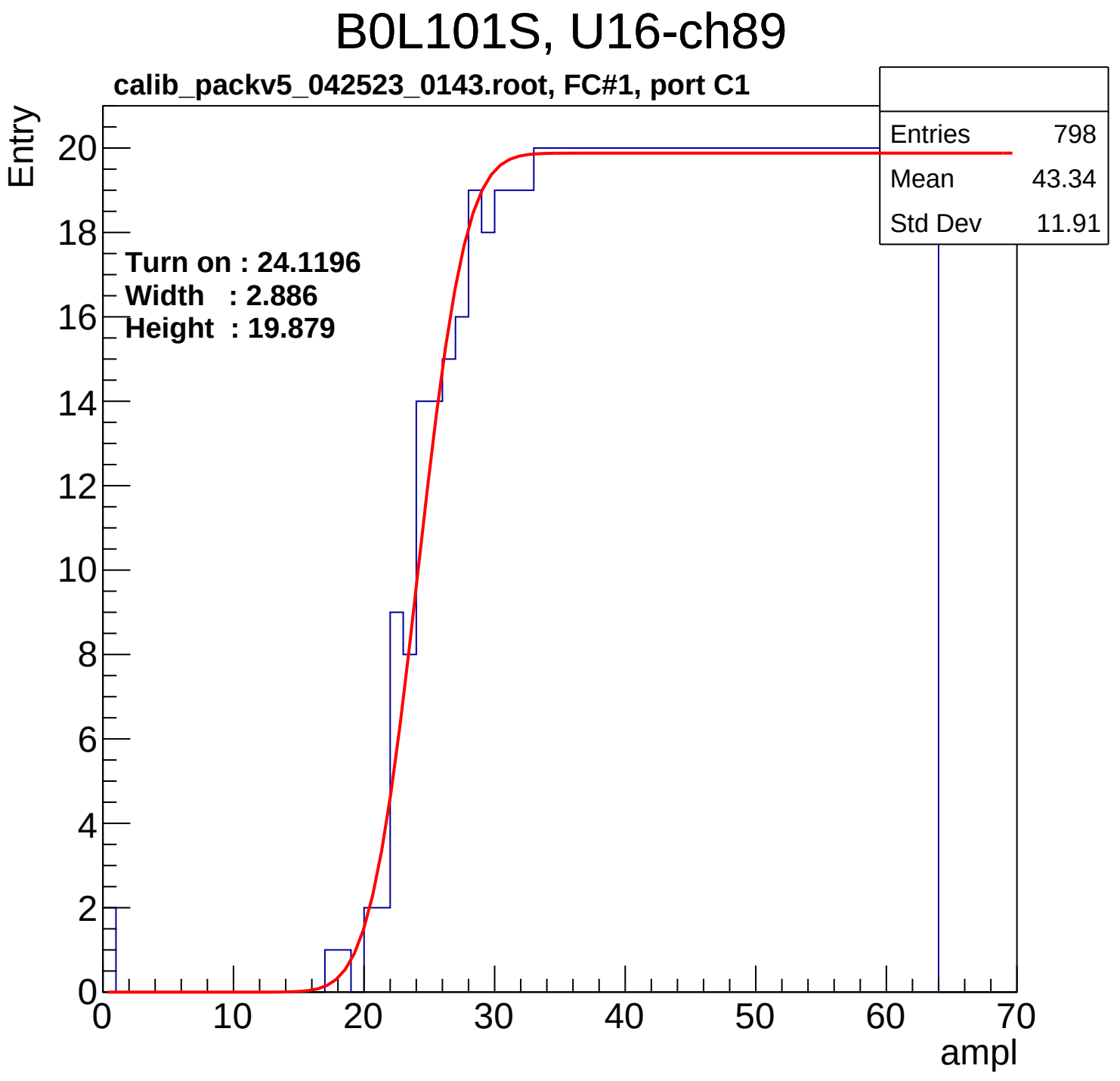
B0L101S, U16-ch89
calib_packv5_042523_0143.root, FC#1, port C1
Entries 798
Mean 43.34
Std Dev 11.91
Turn on : 24.1196
Width : 2.886
Height : 19.879
Entry
ampl
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6
8
10
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0
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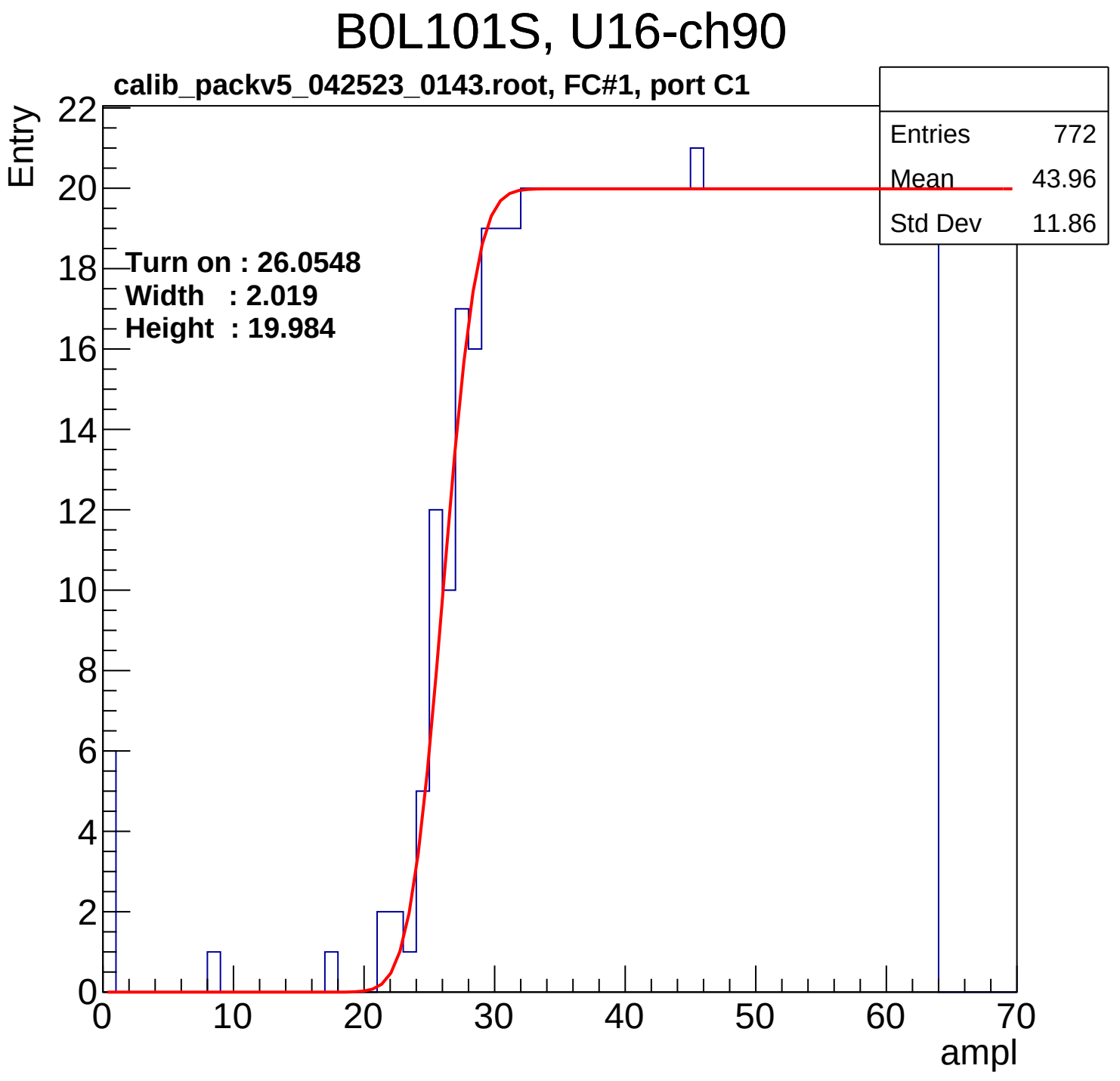
B0L101S, U16-ch90
calib_packv5_042523_0143.root, FC#1, port C1
Entries 772
Mean 43.96
Std Dev 11.86
Turn on : 26.0548
Width : 2.019
Height : 19.984
Entry
ampl
0
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8
10
12
14
16
18
20
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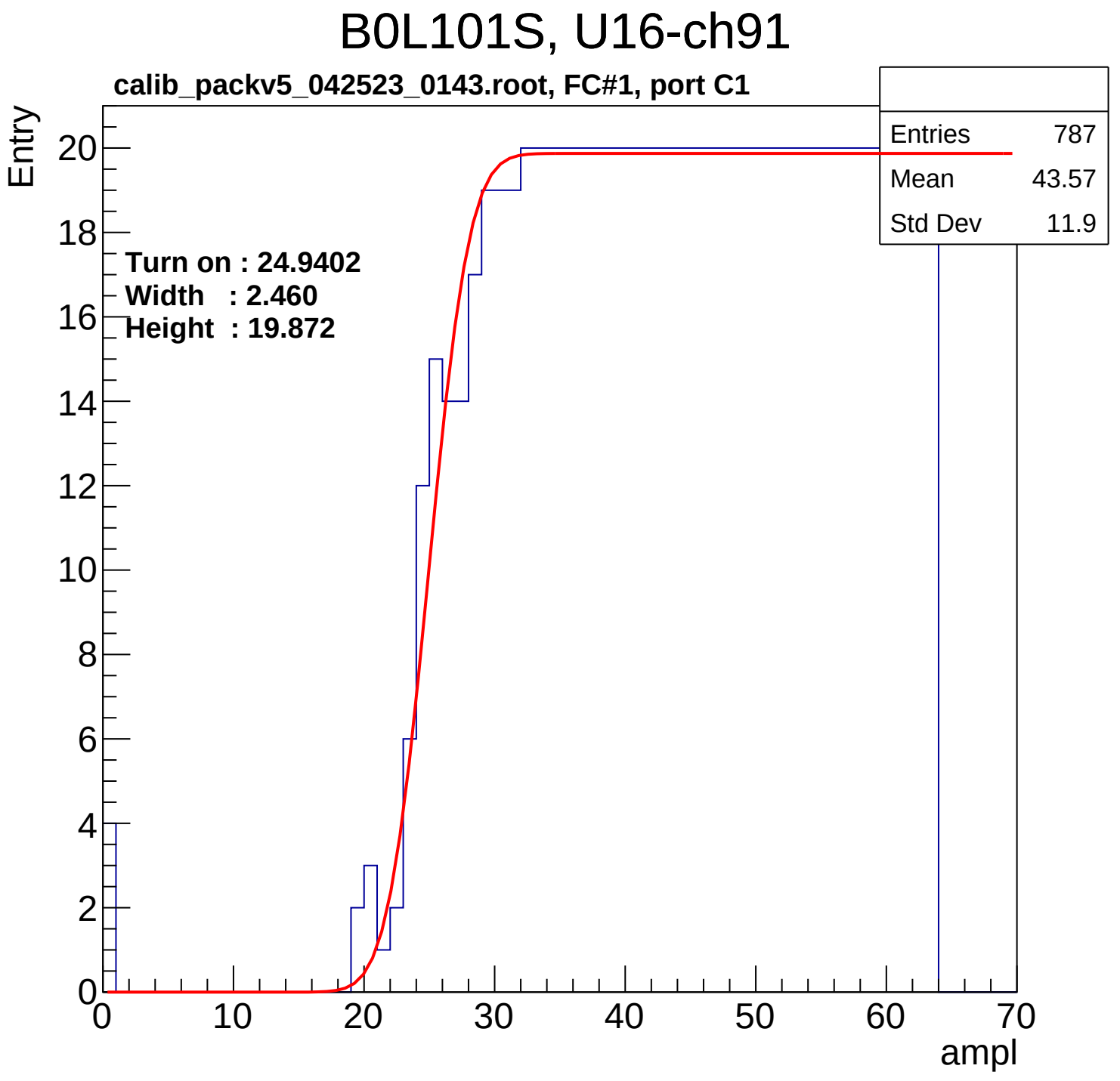
B0L101S, U16-ch91
calib_packv5_042523_0143.root, FC#1, port C1
Entries 787
Mean 43.57
Std Dev 11.9
Turn on : 24.9402
Width : 2.460
Height : 19.872
Entry
ampl
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6
8
10
12
14
16
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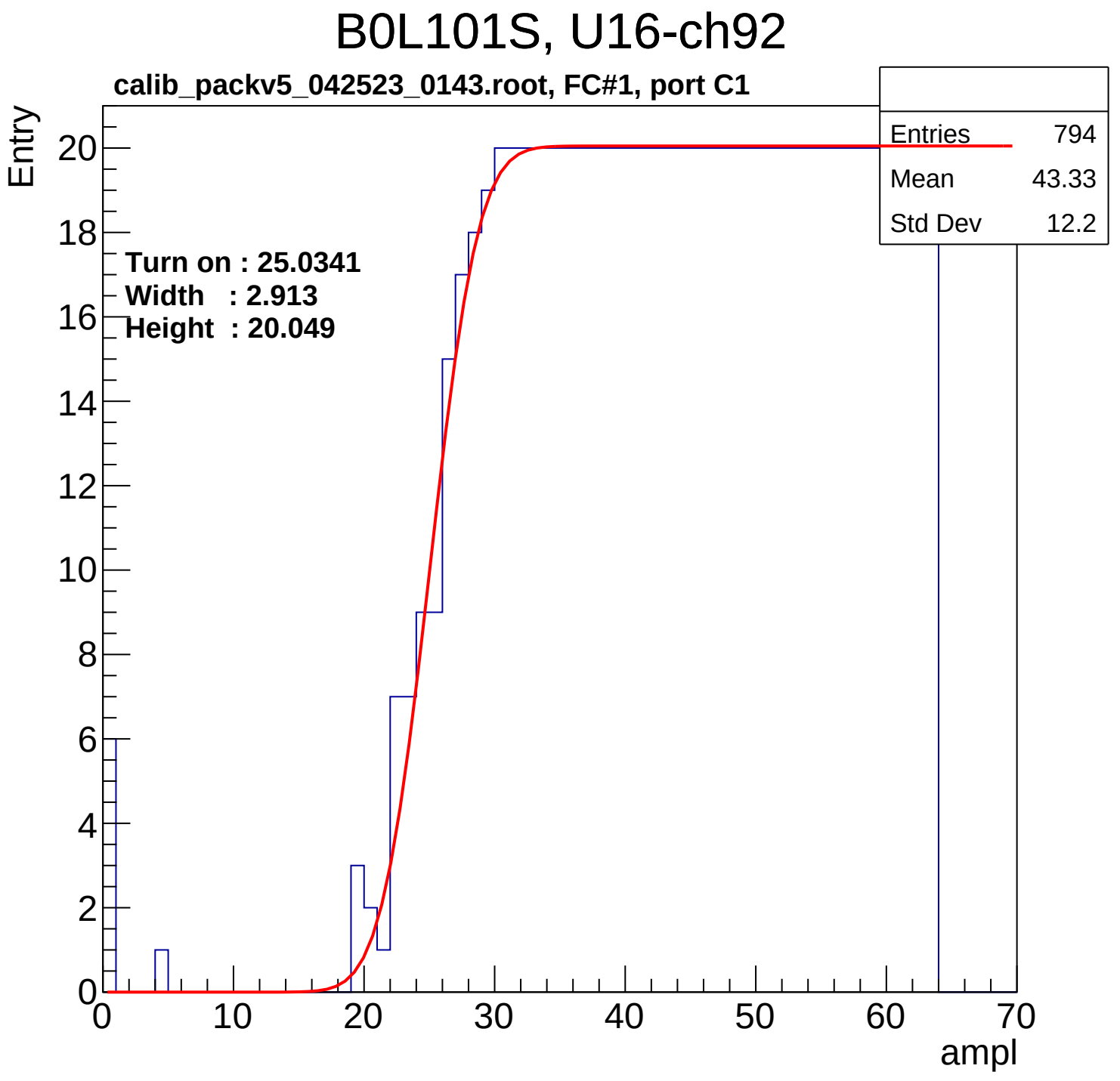
B0L101S, U16-ch92
calib_packv5_042523_0143.root, FC#1, port C1
Entries 794
Mean 43.33
Std Dev 12.2
Turn on : 25.0341
Width : 2.913
Height : 20.049
Entry
ampl
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6
8
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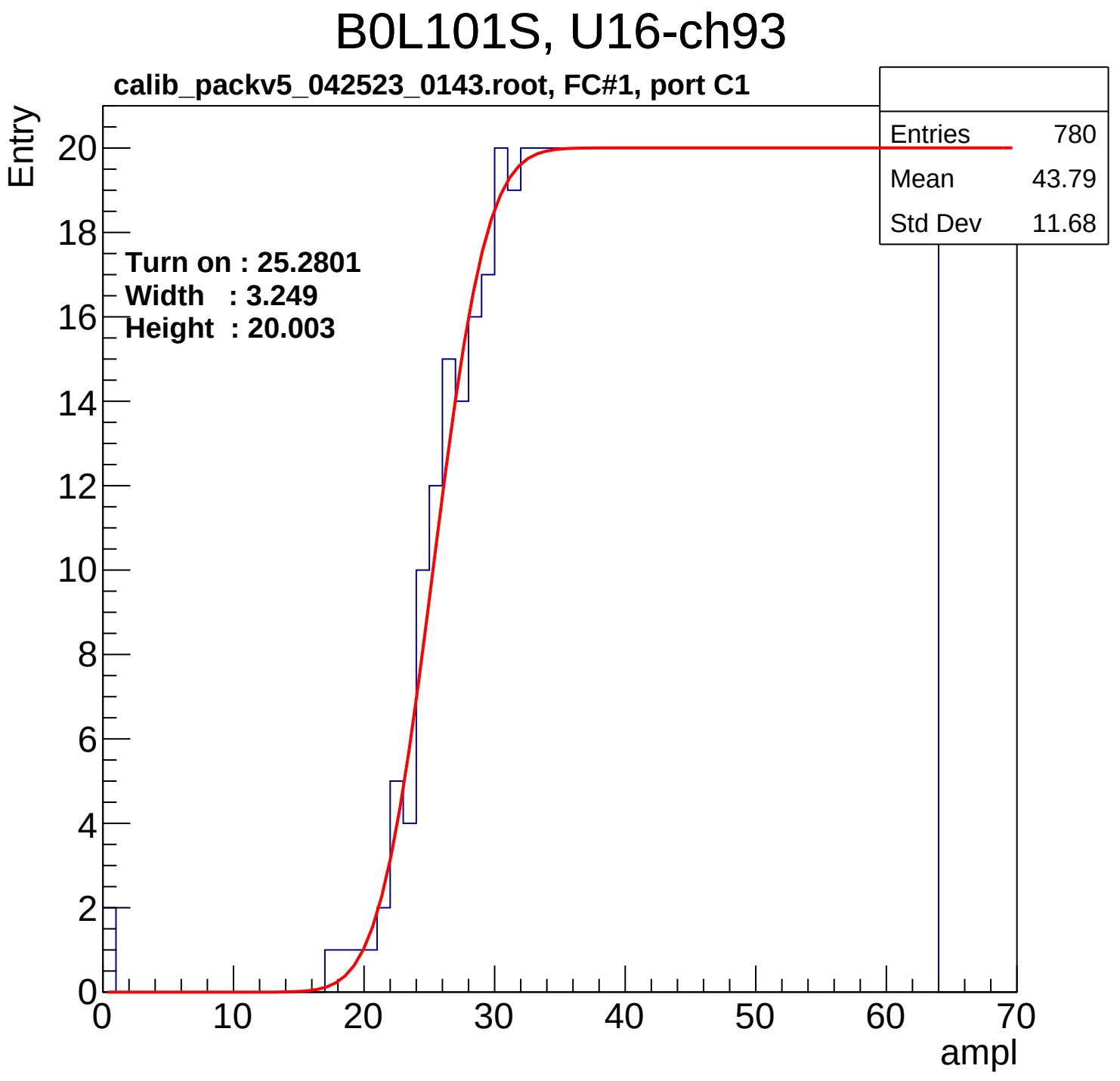
B0L101S, U16-ch93
calib_packv5_042523_0143.root, FC#1, port C1
Entries 780
Mean 43.79
Std Dev 11.68
Turn on : 25.2801
Width : 3.249
Height : 20.003
Entry
ampl
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6
8
10
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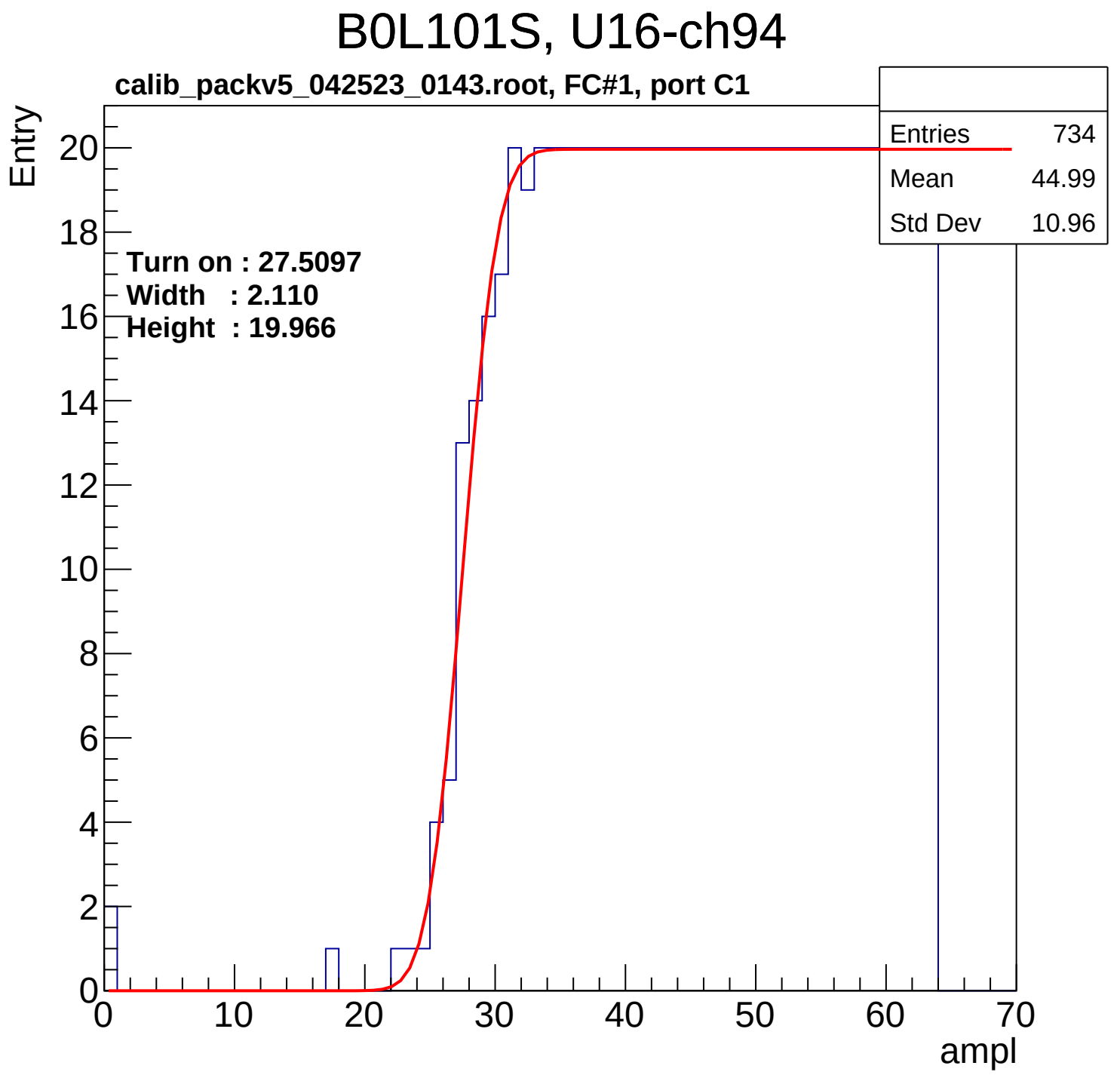
B0L101S, U16-ch94
calib_packv5_042523_0143.root, FC#1, port C1
Entries 734
Mean 44.99
Std Dev 10.96
Turn on : 27.5097
Width : 2.110
Height : 19.966
Entry
ampl
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6
8
10
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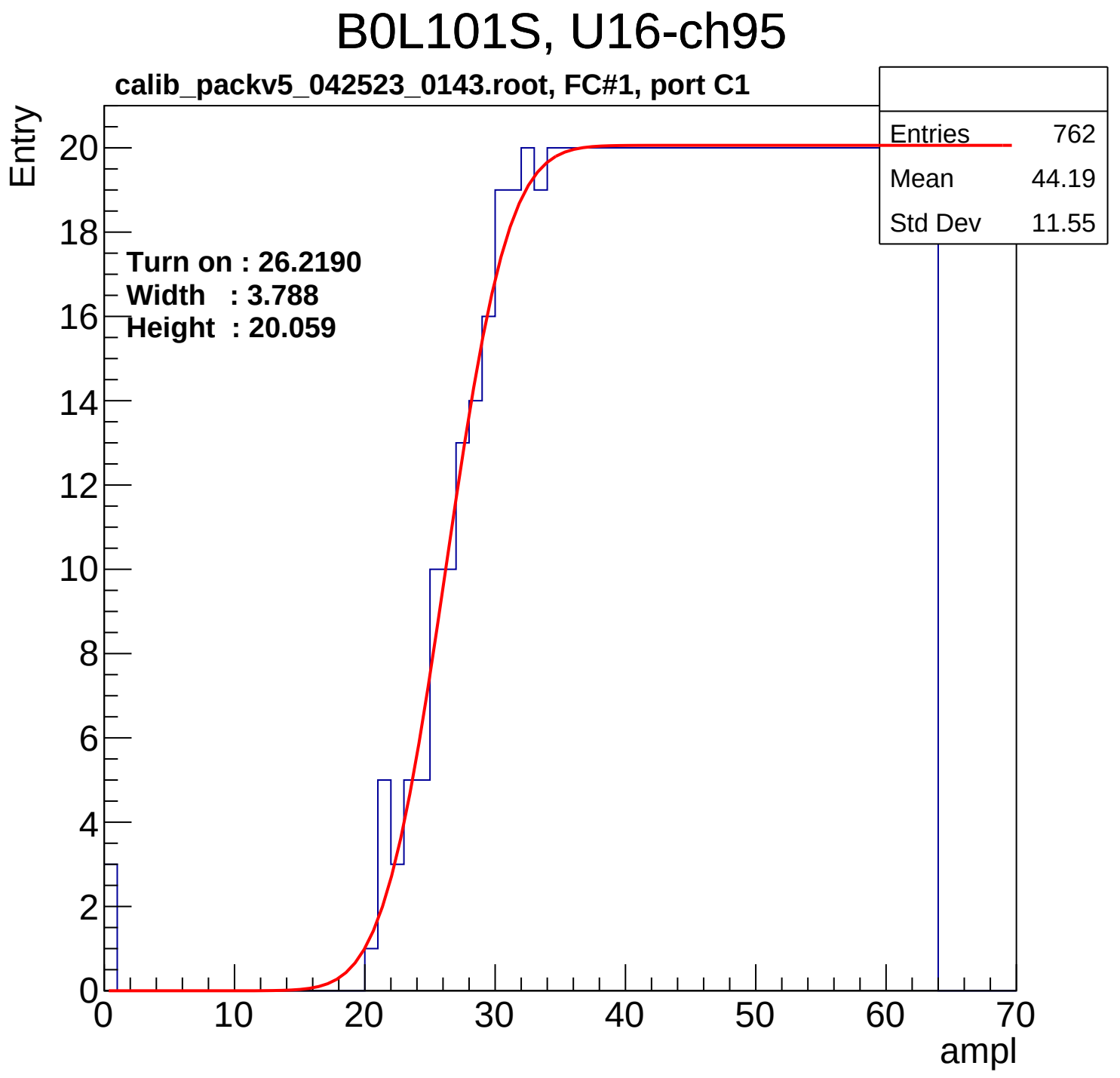
B0L101S, U16-ch95
calib_packv5_042523_0143.root, FC#1, port C1
Entries 762
Mean 44.19
Std Dev 11.55
Turn on : 26.2190
Width : 3.788
Height : 20.059
Entry
ampl
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6
8
10
12
14
16
18
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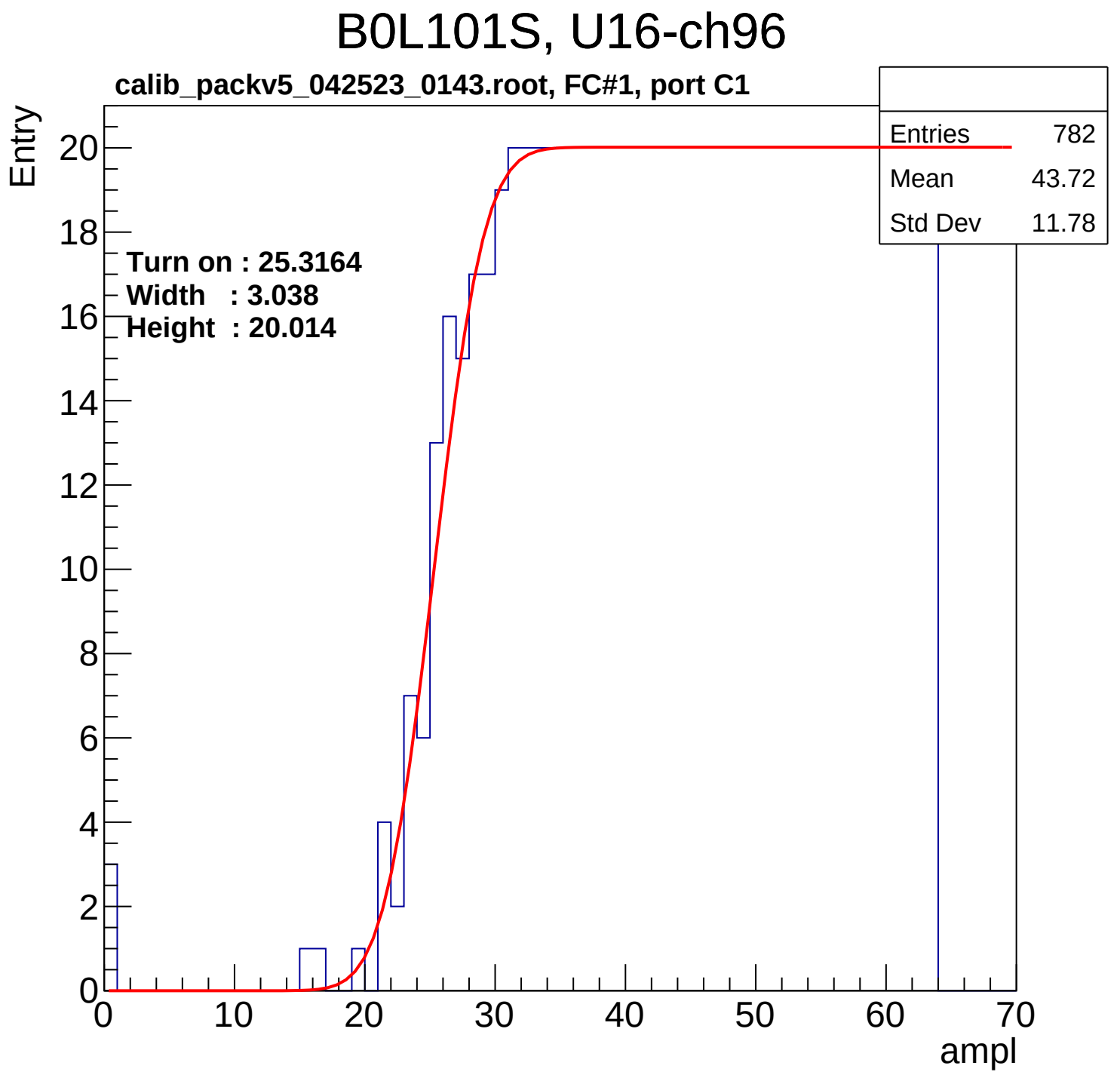
B0L101S, U16-ch96
calib_packv5_042523_0143.root, FC#1, port C1
Entries 782
Mean 43.72
Std Dev 11.78
Turn on : 25.3164
Width : 3.038
Height : 20.014
Entry
ampl
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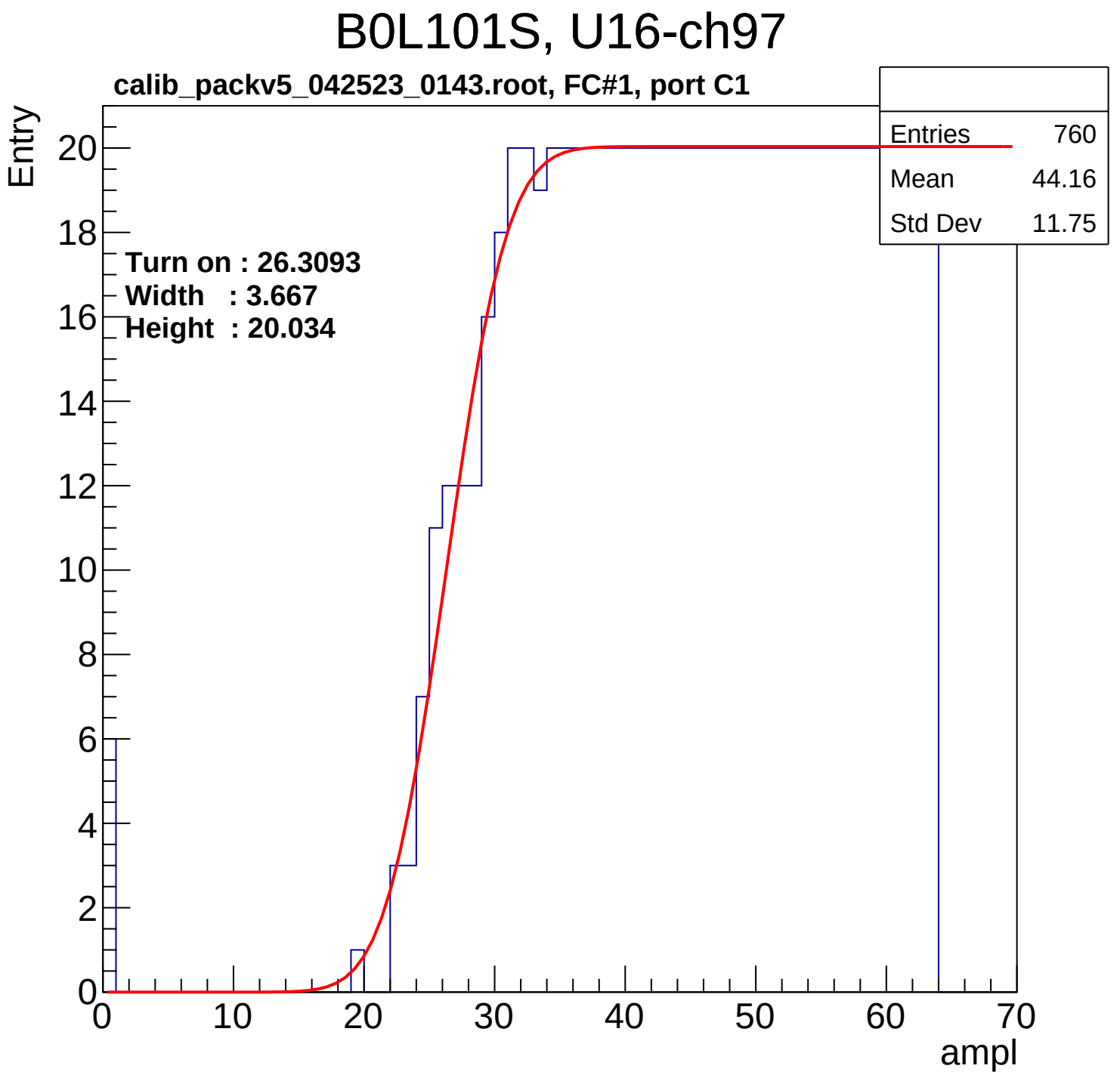
B0L101S, U16-ch97
calib_packv5_042523_0143.root, FC#1, port C1
Entries 760
Mean 44.16
Std Dev 11.75
Turn on : 26.3093
Width : 3.667
Height : 20.034
Entry
ampl
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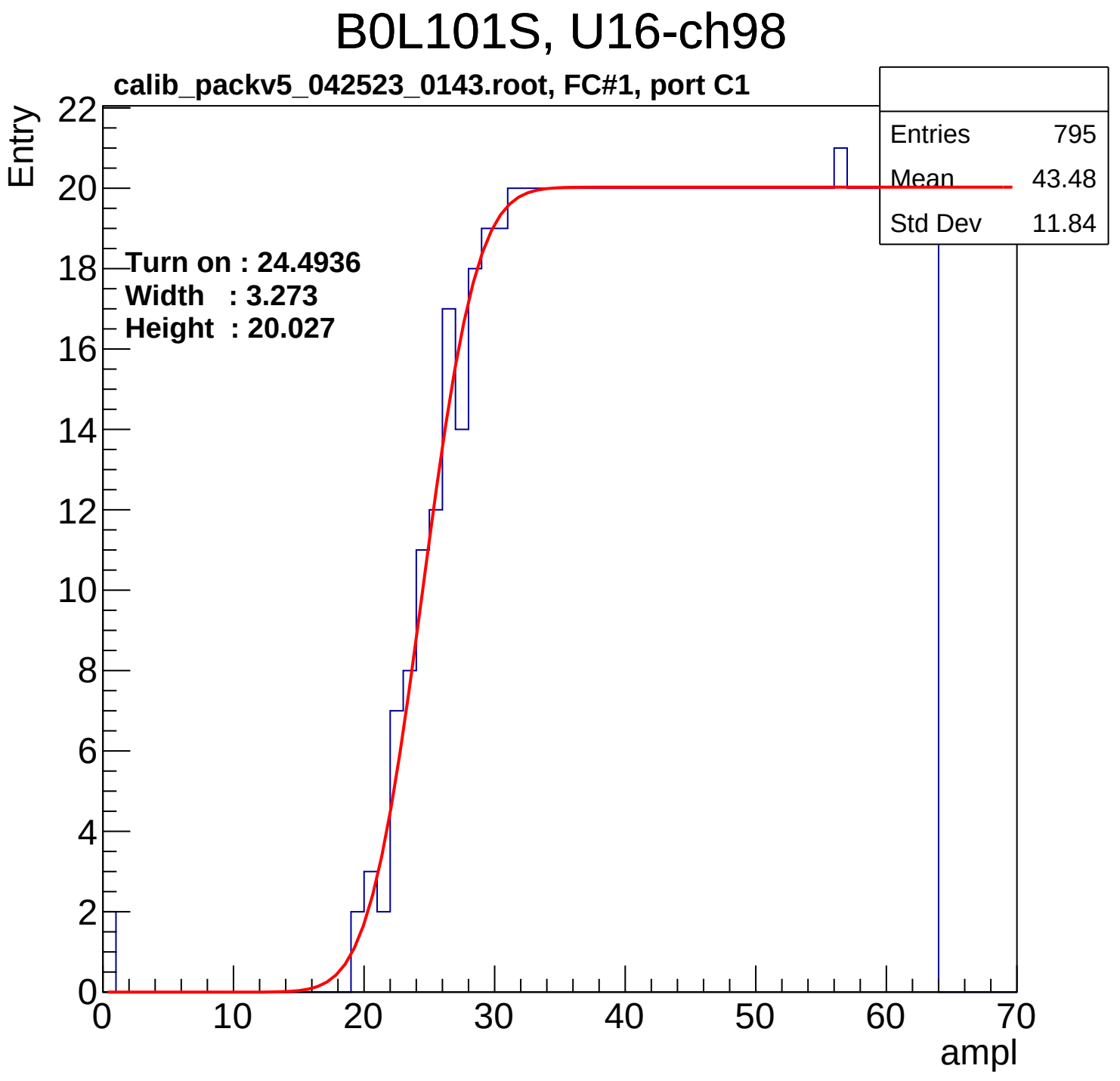
B0L101S, U16-ch98
calib_packv5_042523_0143.root, FC#1, port C1
Entries 795
Mean 43.48
Std Dev 11.84
Turn on : 24.4936
Width : 3.273
Height : 20.027
Entry
ampl
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8
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16
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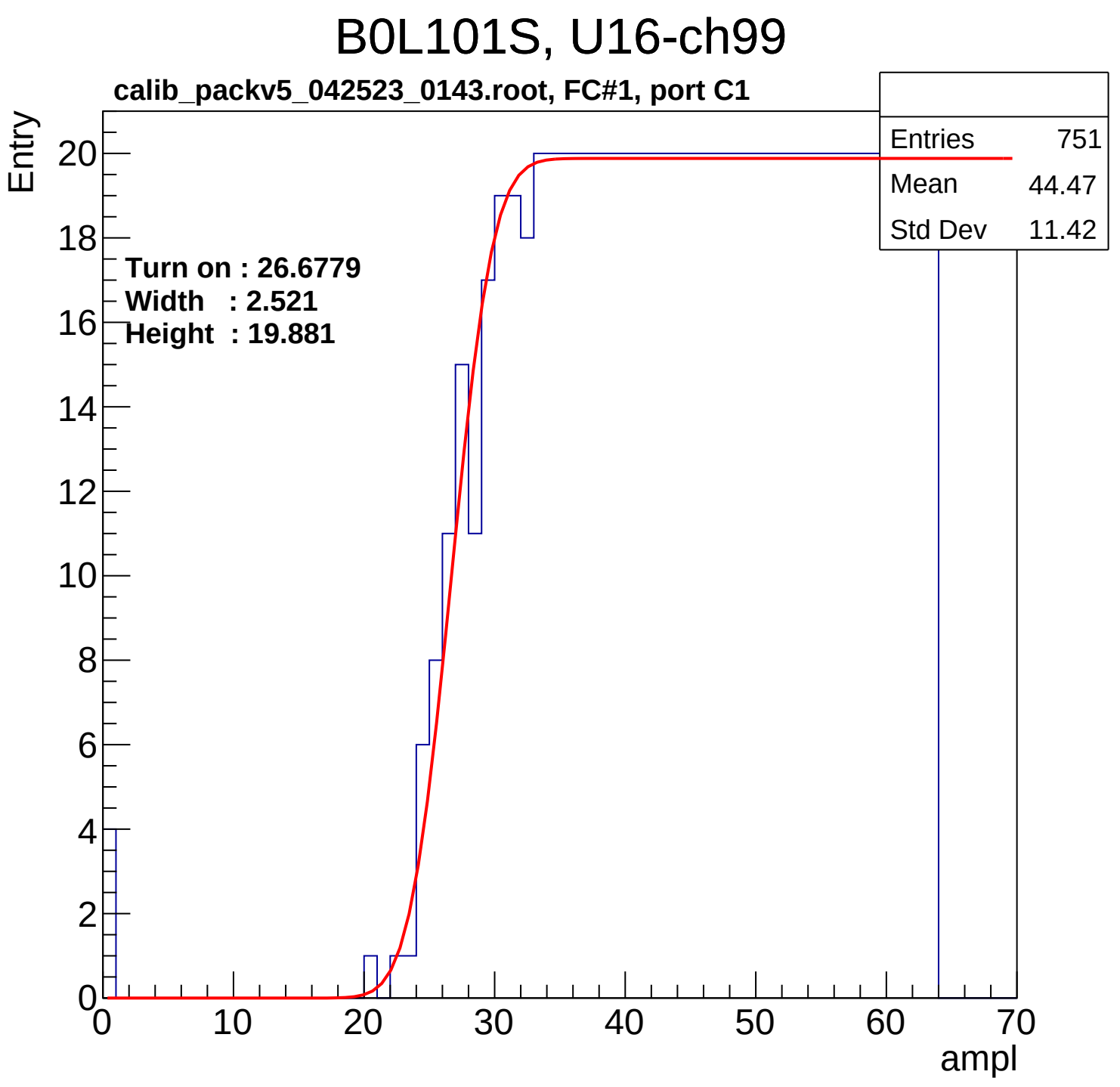
B0L101S, U16-ch99
calib_packv5_042523_0143.root, FC#1, port C1
Entries 751
Mean 44.47
Std Dev 11.42
Turn on : 26.6779
Width : 2.521
Height : 19.881
Entry
ampl
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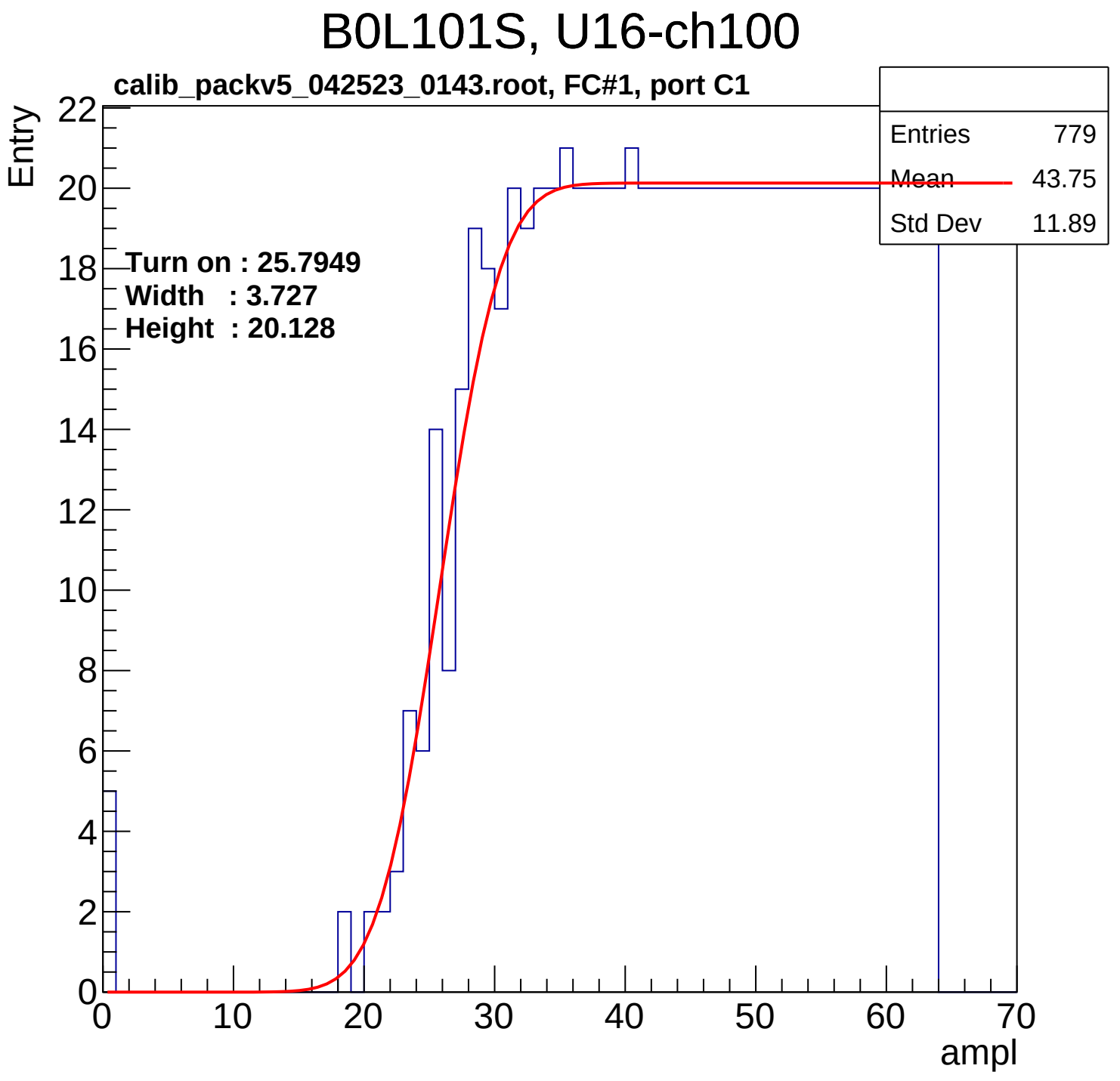
B0L101S, U16-ch100
calib_packv5_042523_0143.root, FC#1, port C1
Entries 779
Mean 43.75
Std Dev 11.89
Turn on : 25.7949
Width : 3.727
Height : 20.128
Entry
ampl
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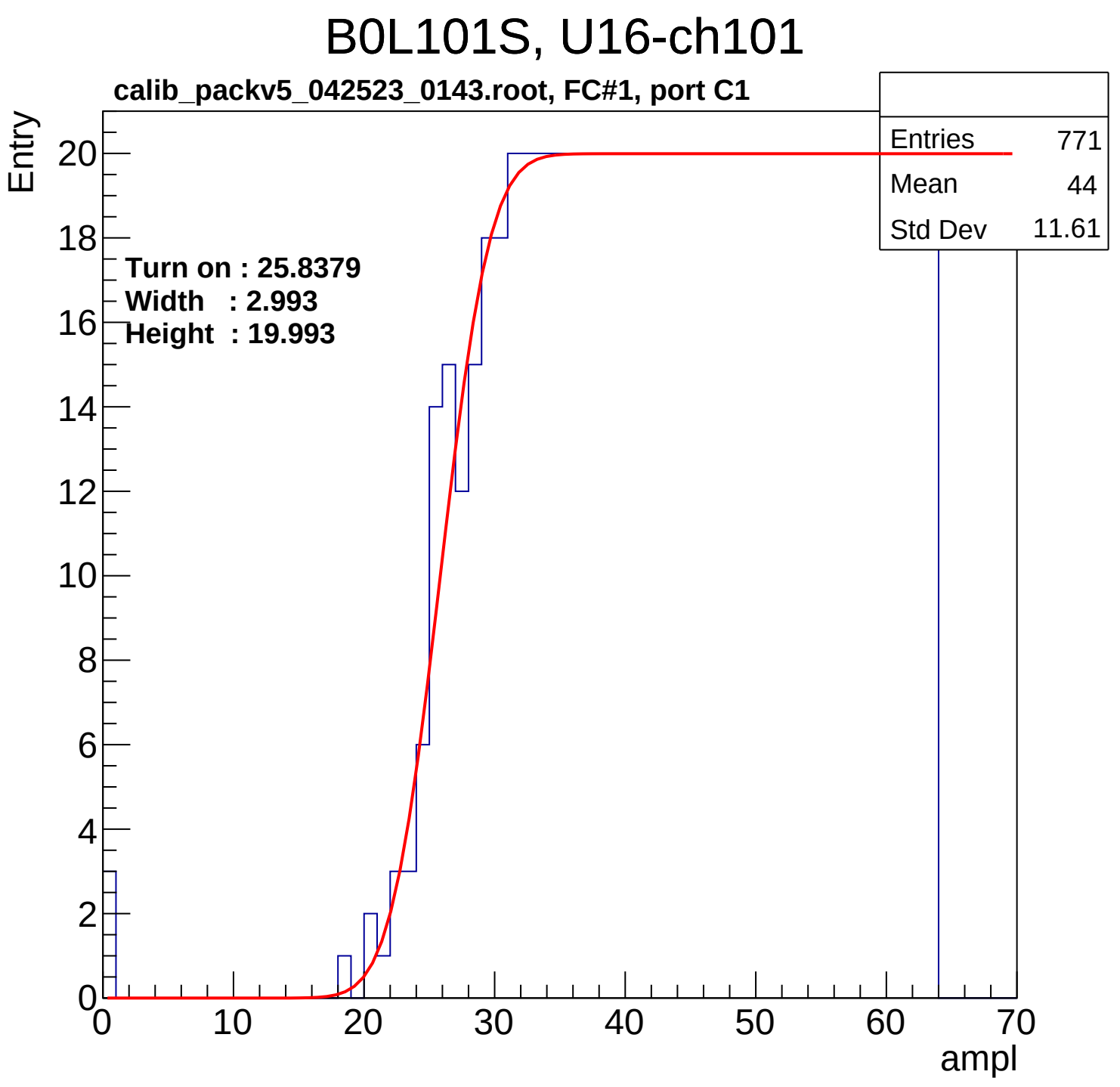
B0L101S, U16-ch101
calib_packv5_042523_0143.root, FC#1, port C1
Entries 771
Mean 44
Std Dev 11.61
Turn on : 25.8379
Width : 2.993
Height : 19.993
Entry
ampl
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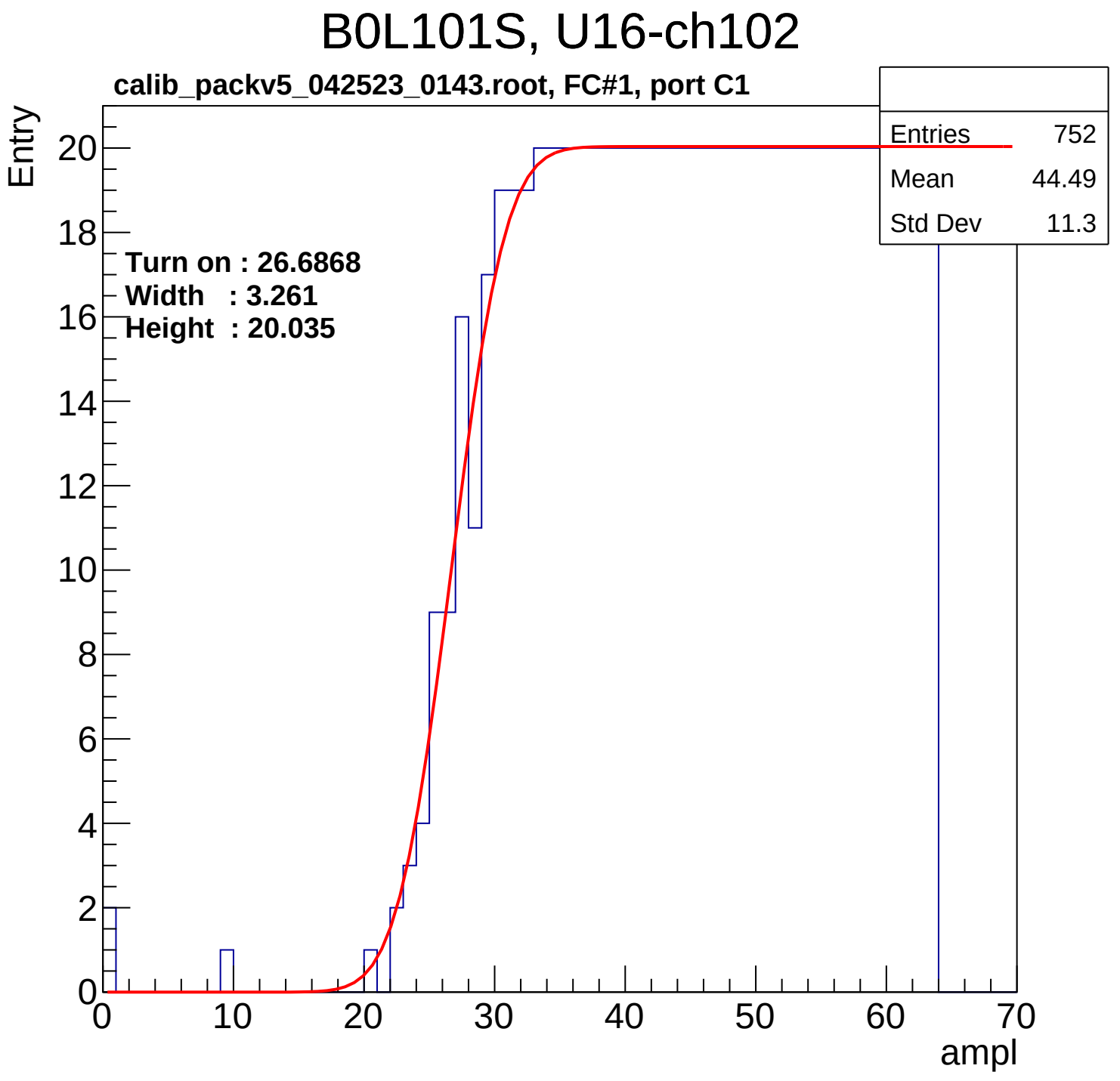
B0L101S, U16-ch102
calib_packv5_042523_0143.root, FC#1, port C1
Entries 752
Mean 44.49
Std Dev 11.3
Turn on : 26.6868
Width : 3.261
Height : 20.035
Entry
ampl
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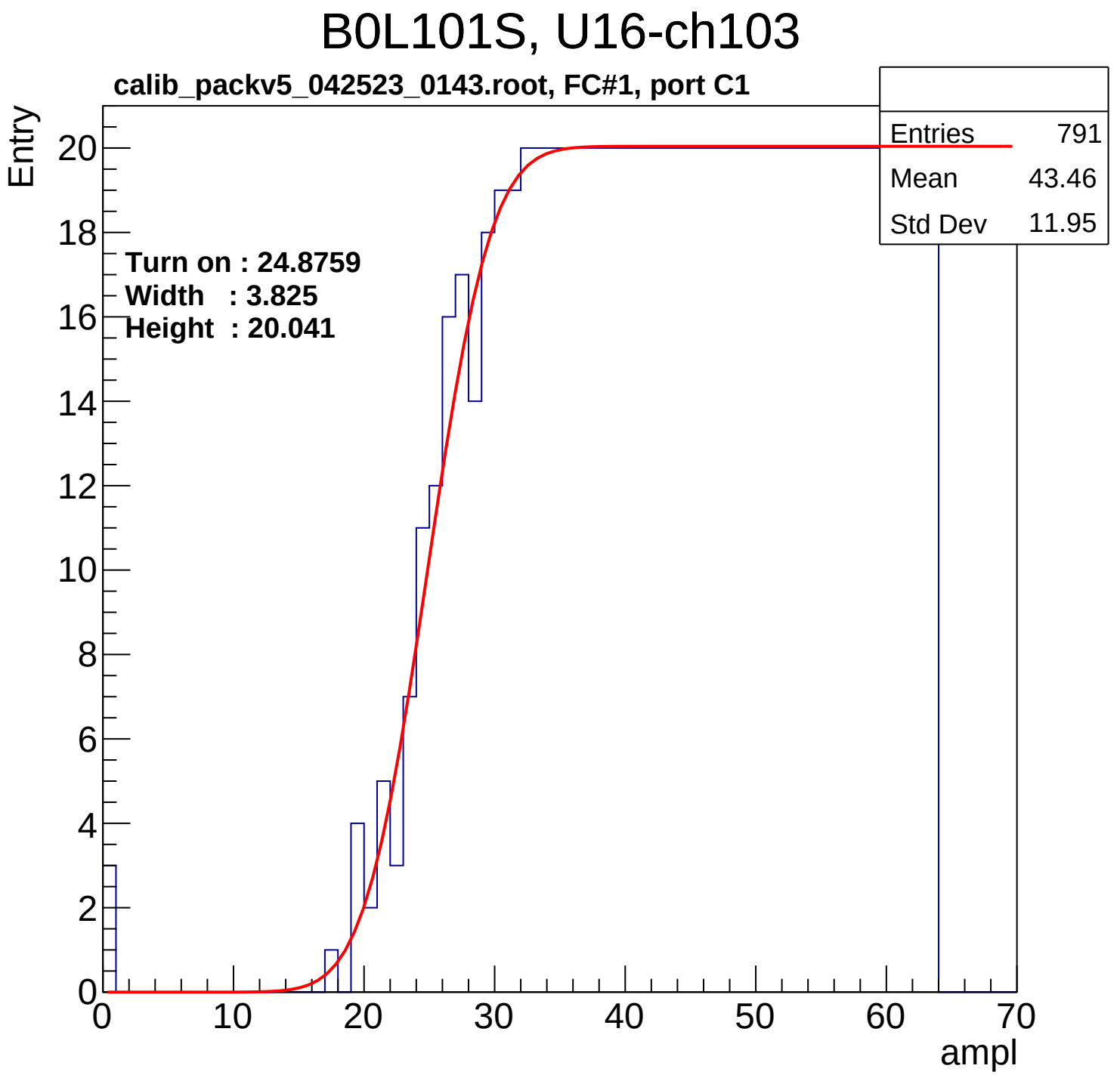
B0L101S, U16-ch103
calib_packv5_042523_0143.root, FC#1, port C1
Entries 791
Mean 43.46
Std Dev 11.95
Turn on : 24.8759
Width : 3.825
Height : 20.041
Entry
ampl
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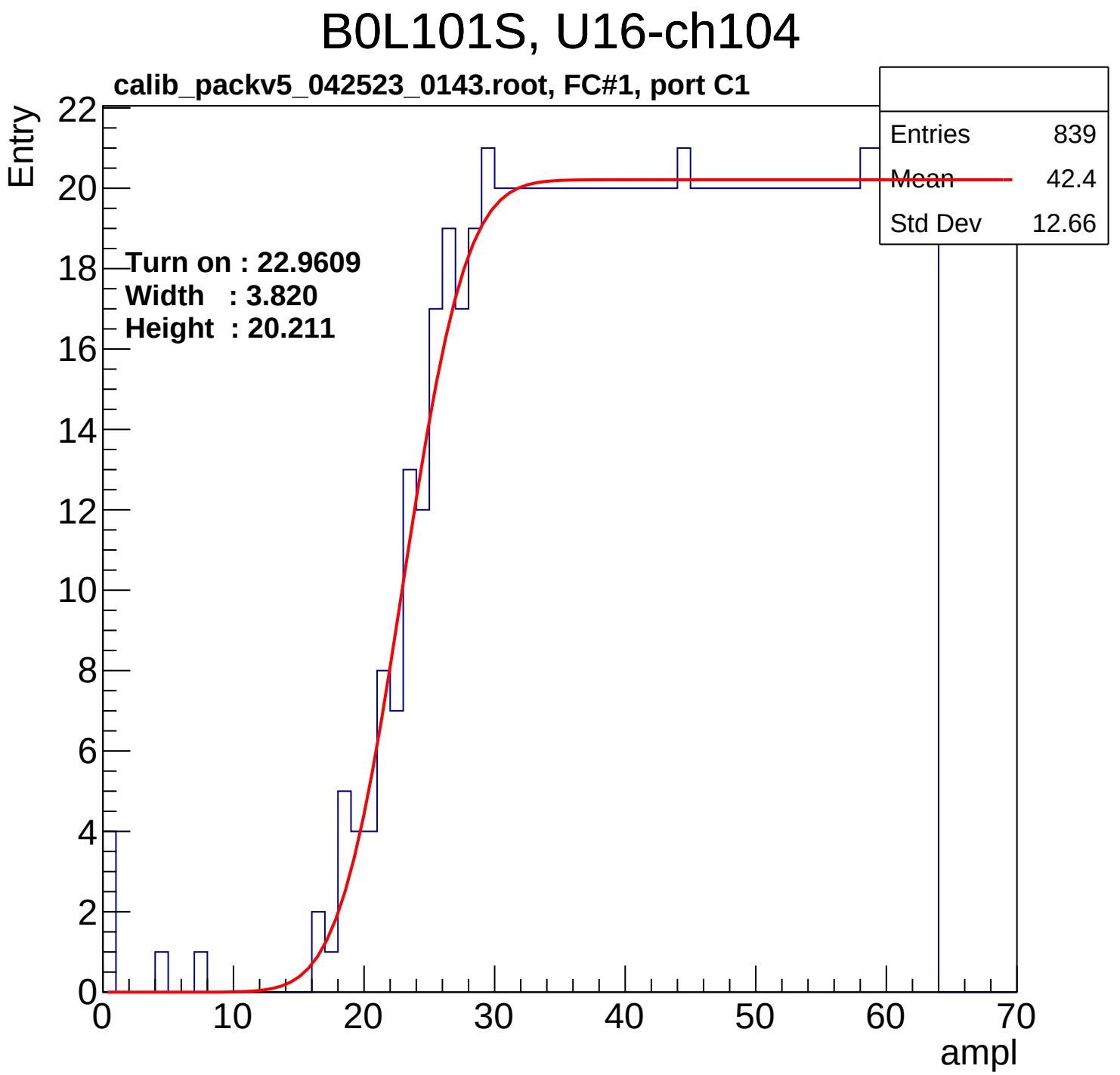
B0L101S, U16-ch104
calib_packv5_042523_0143.root, FC#1, port C1
Entries 839
Mean 42.4
Std Dev 12.66
Turn on : 22.9609
Width : 3.820
Height : 20.211
Entry
ampl
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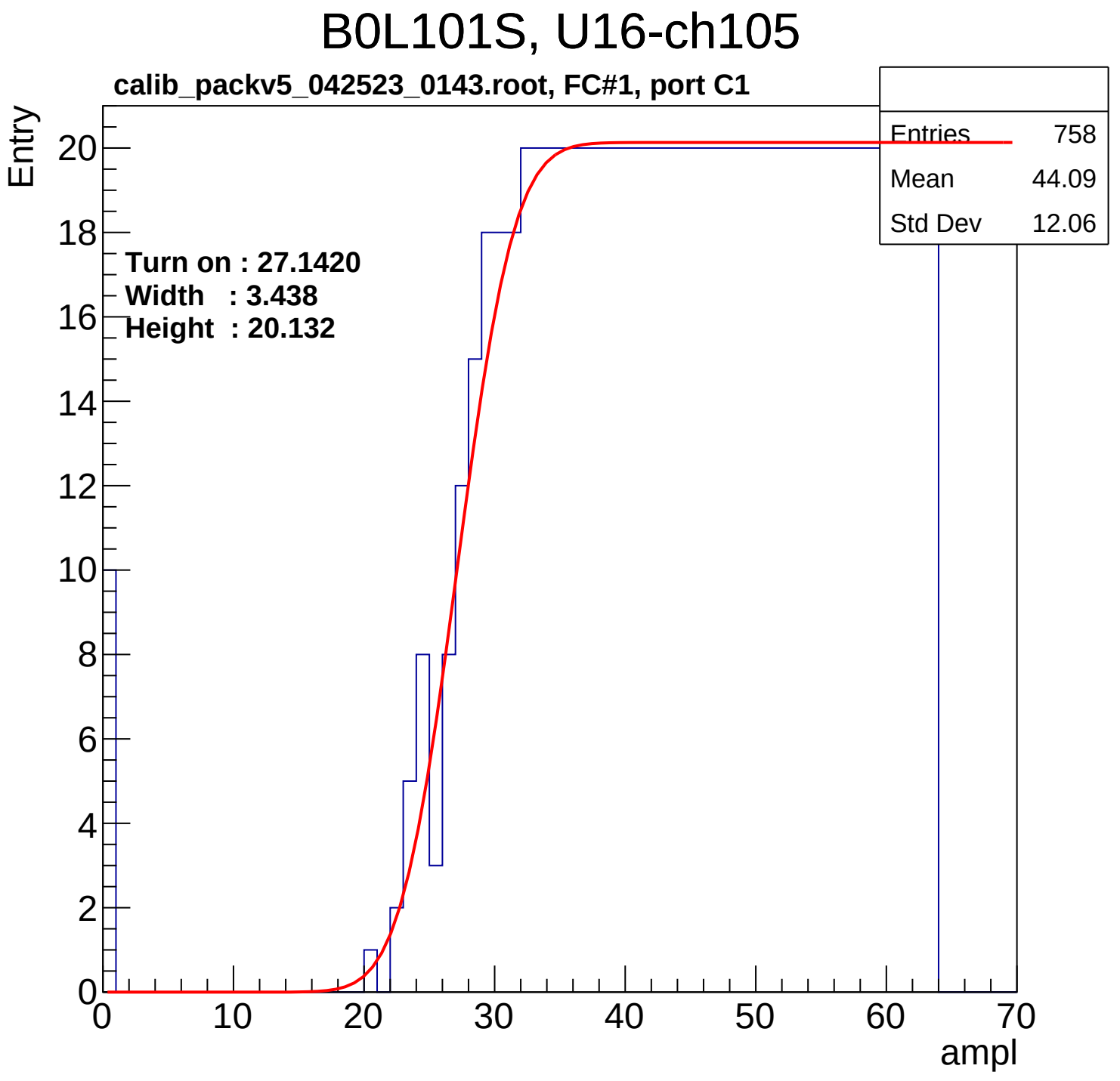
B0L101S, U16-ch105
calib_packv5_042523_0143.root, FC#1, port C1
Entries 758
Mean 44.09
Std Dev 12.06
Turn on : 27.1420
Width : 3.438
Height : 20.132
Entry
ampl
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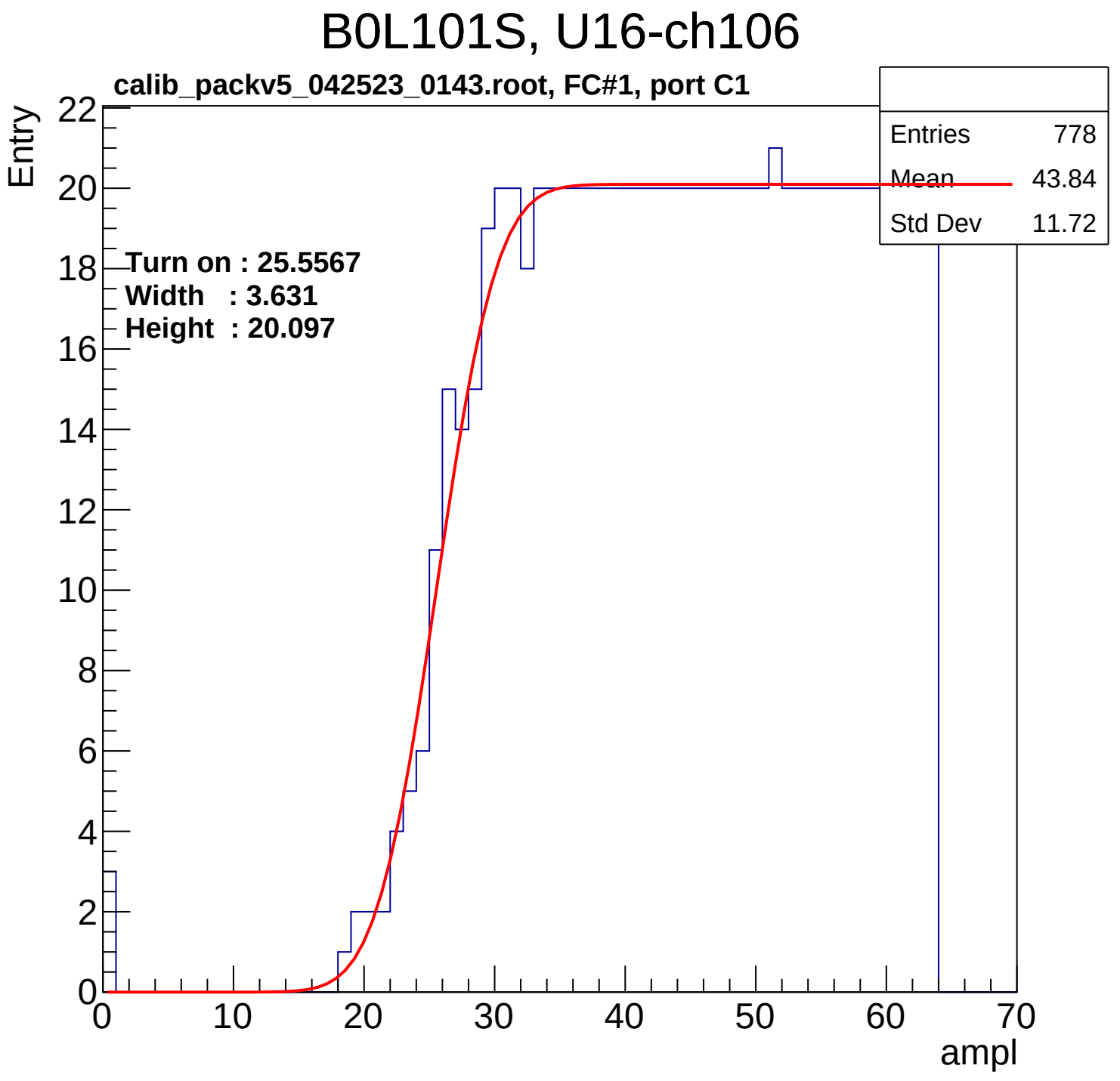
B0L101S, U16-ch106
calib_packv5_042523_0143.root, FC#1, port C1
Entries 778
Mean 43.84
Std Dev 11.72
Turn on : 25.5567
Width : 3.631
Height : 20.097
Entry
ampl
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8
10
12
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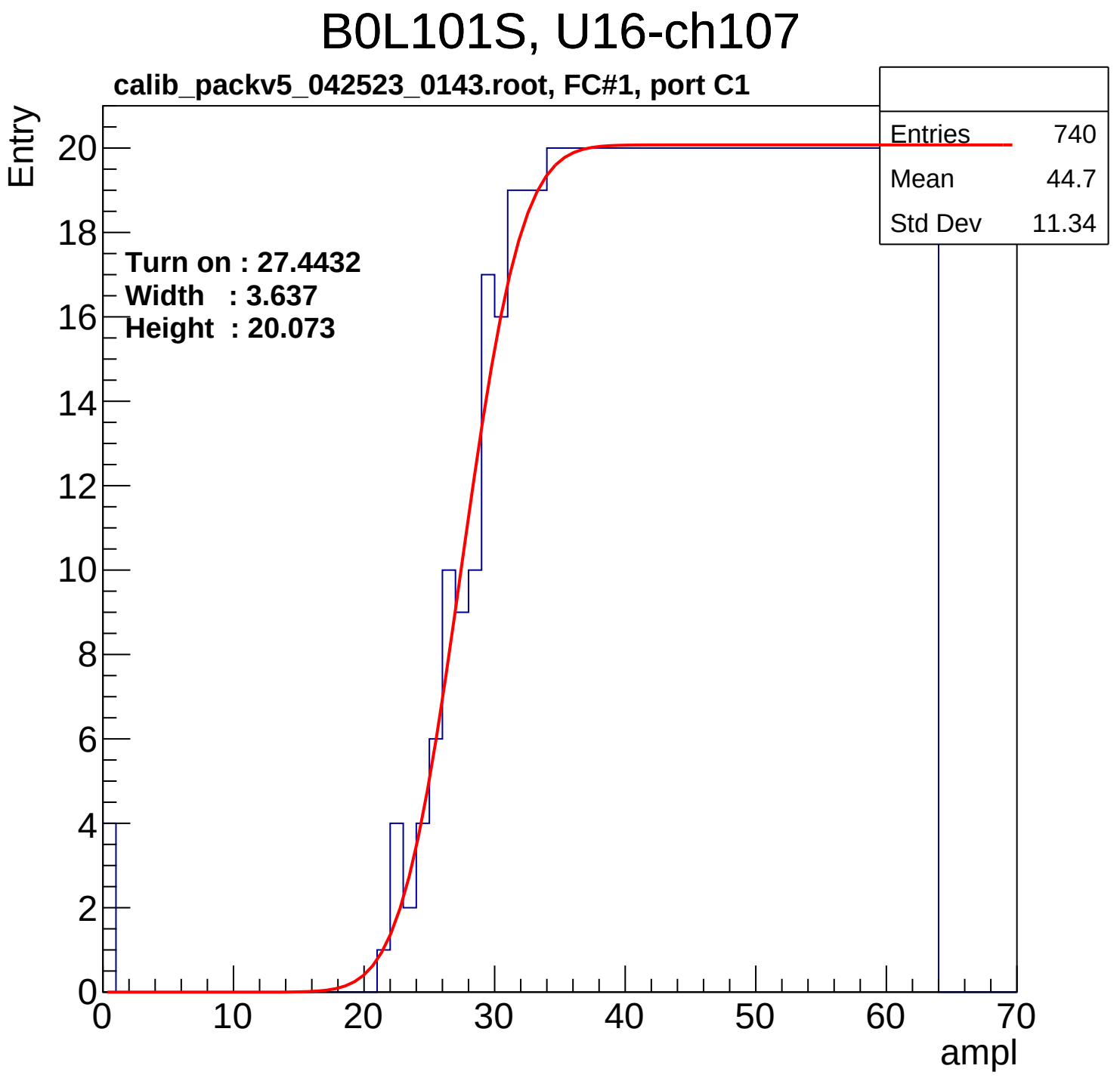
B0L101S, U16-ch107
calib_packv5_042523_0143.root, FC#1, port C1
Entries 740
Mean 44.7
Std Dev 11.34
Turn on : 27.4432
Width : 3.637
Height : 20.073
Entry
ampl
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6
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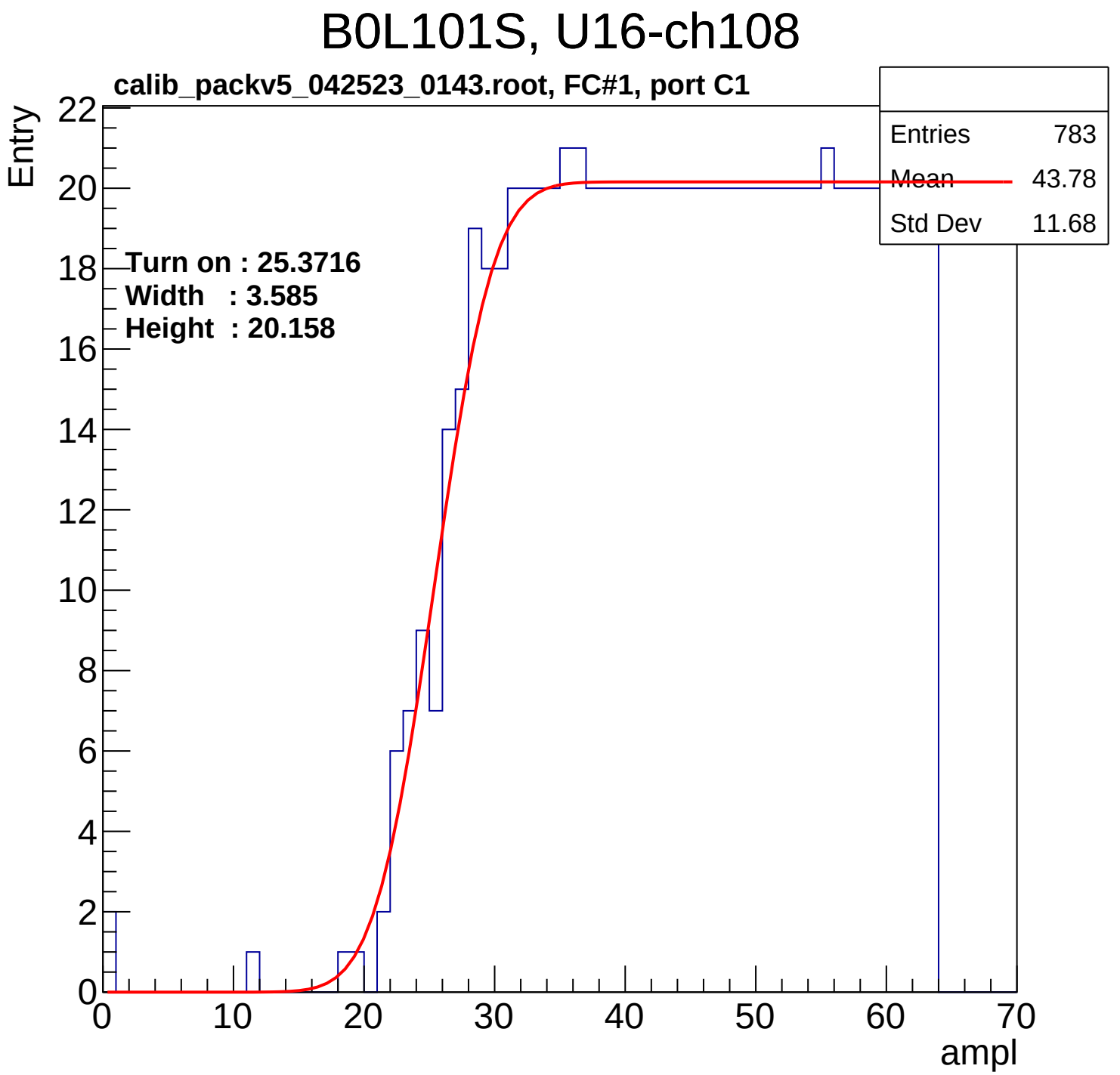
B0L101S, U16-ch108
calib_packv5_042523_0143.root, FC#1, port C1
Entries 783
Mean 43.78
Std Dev 11.68
Turn on : 25.3716
Width : 3.585
Height : 20.158
Entry
ampl
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8
10
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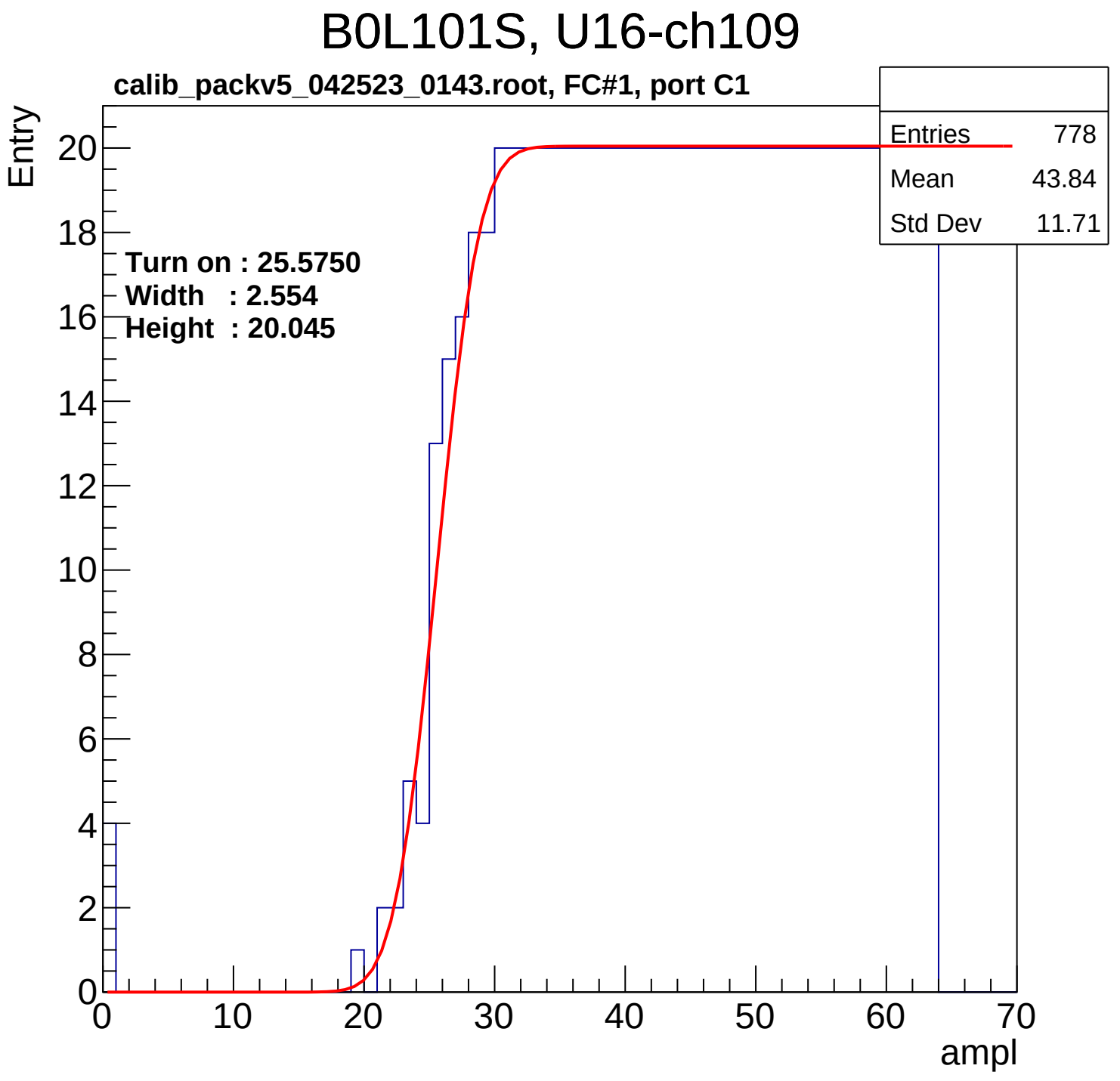
B0L101S, U16-ch109
calib_packv5_042523_0143.root, FC#1, port C1
Entries 778
Mean 43.84
Std Dev 11.71
Turn on : 25.5750
Width : 2.554
Height : 20.045
Entry
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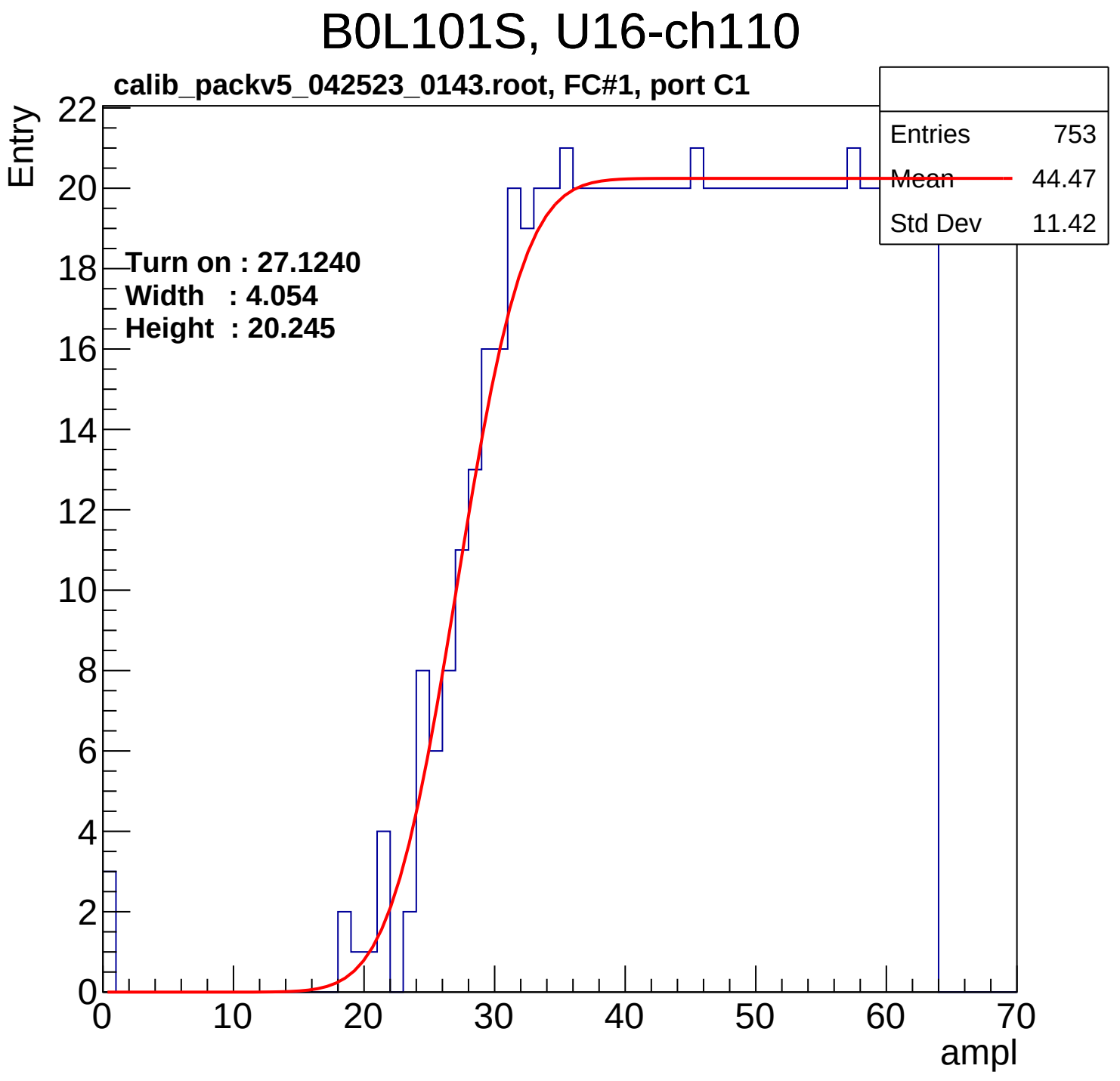
B0L101S, U16-ch110
calib_packv5_042523_0143.root, FC#1, port C1
Entries 753
Mean 44.47
Std Dev 11.42
Turn on : 27.1240
Width : 4.054
Height : 20.245
Entry
ampl
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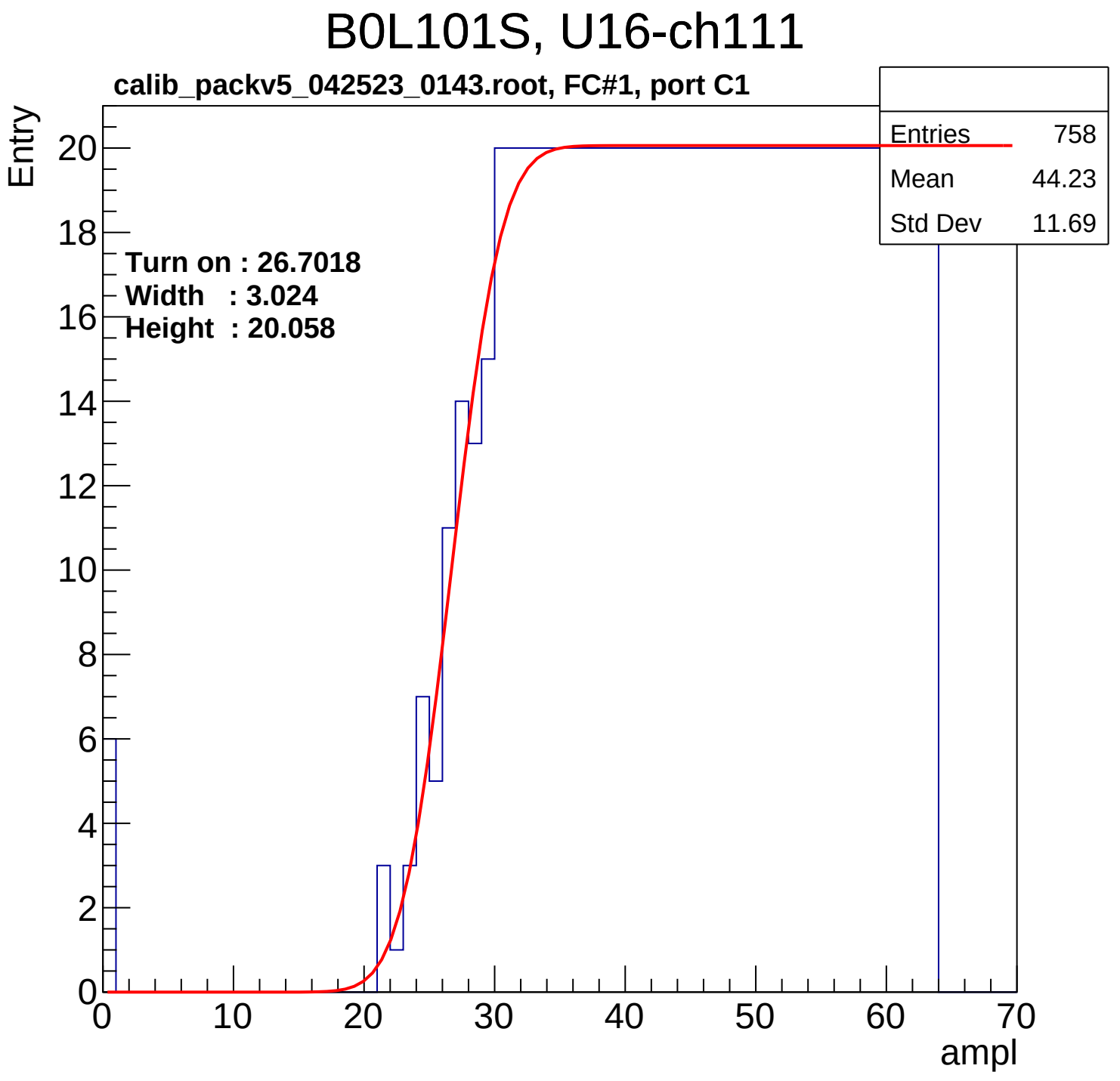
B0L101S, U16-ch111
calib_packv5_042523_0143.root, FC#1, port C1
Entries 758
Mean 44.23
Std Dev 11.69
Turn on : 26.7018
Width : 3.024
Height : 20.058
Entry
ampl
0
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4
6
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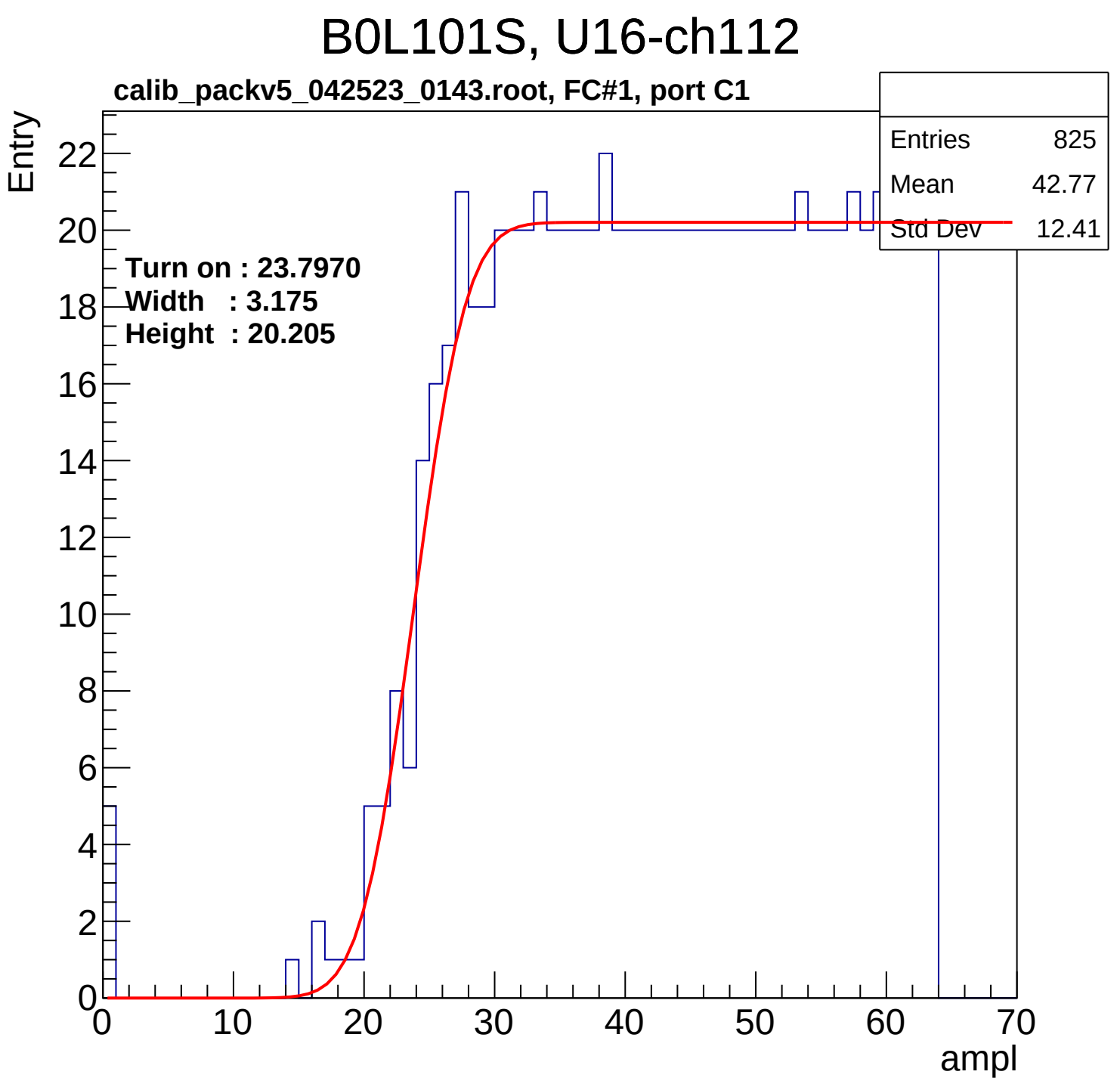
B0L101S, U16-ch112
calib_packv5_042523_0143.root, FC#1, port C1
Entries 825
Mean 42.77
Std Dev 12.41
Turn on : 23.7970
Width : 3.175
Height : 20.205
Entry
ampl
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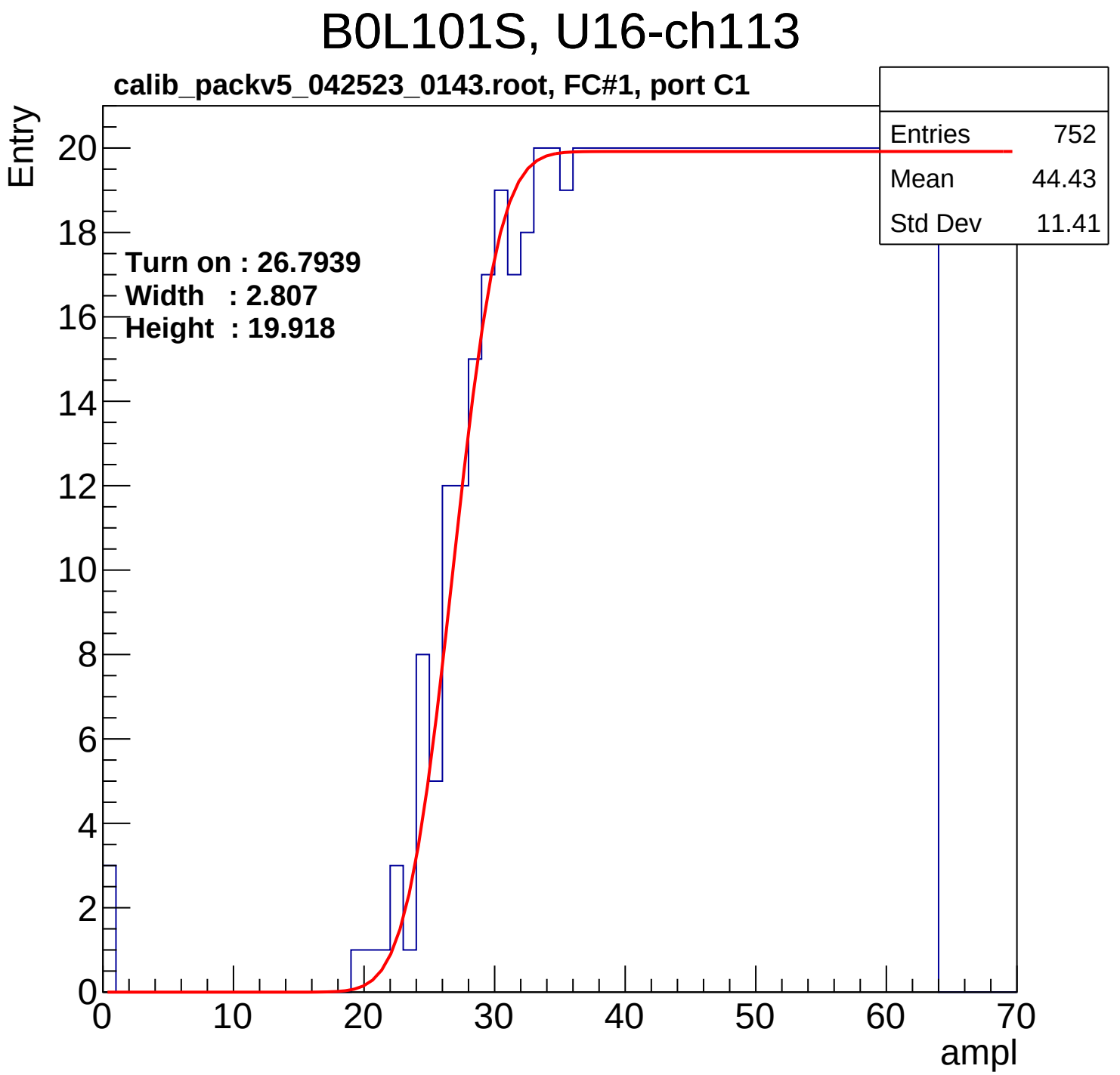
B0L101S, U16-ch113
calib_packv5_042523_0143.root, FC#1, port C1
Entries 752
Mean 44.43
Std Dev 11.41
Turn on : 26.7939
Width : 2.807
Height : 19.918
Entry
ampl
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6
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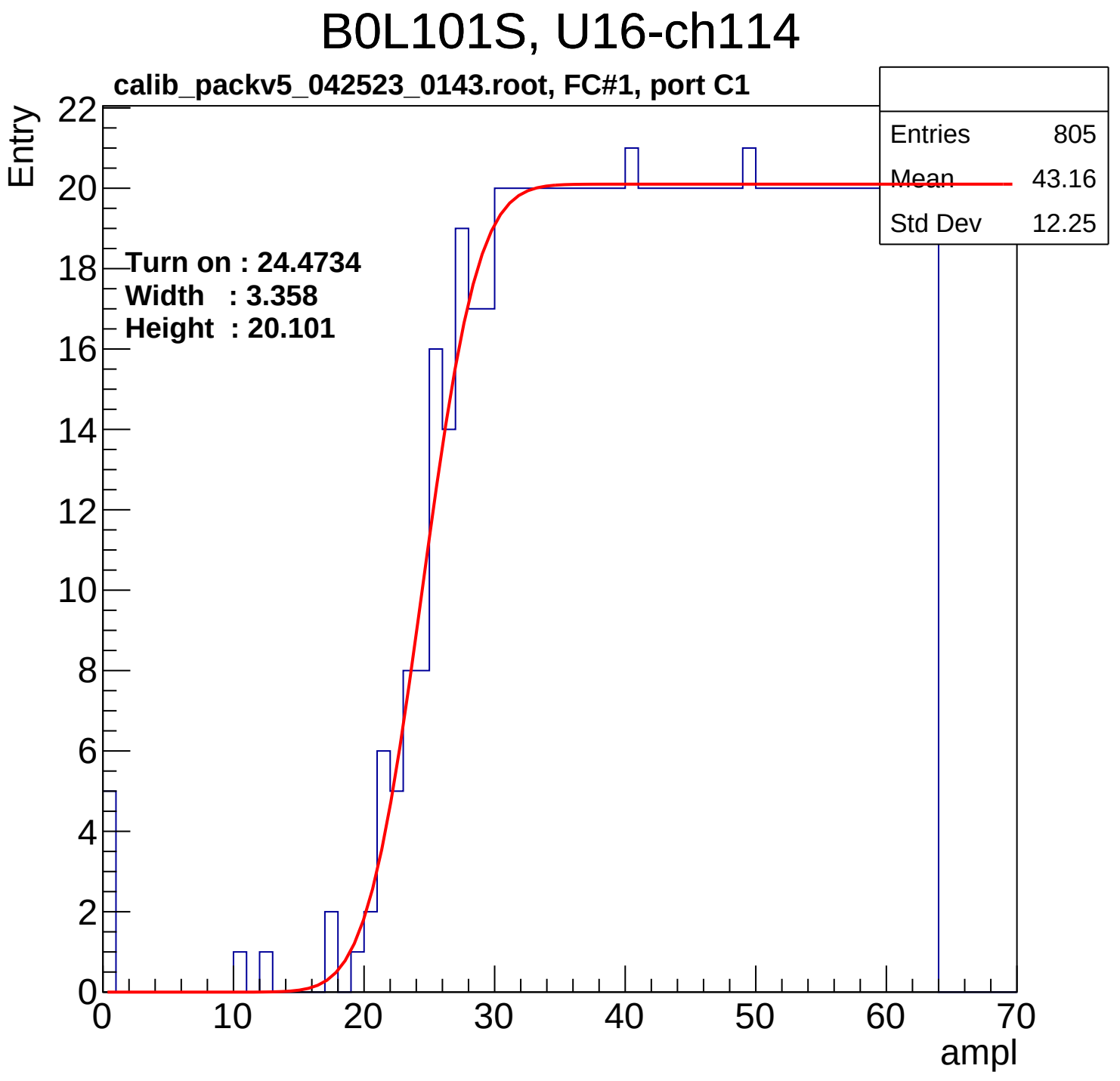
B0L101S, U16-ch114
calib_packv5_042523_0143.root, FC#1, port C1
Entries 805
Mean 43.16
Std Dev 12.25
Turn on : 24.4734
Width : 3.358
Height : 20.101
Entry
ampl
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8
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16
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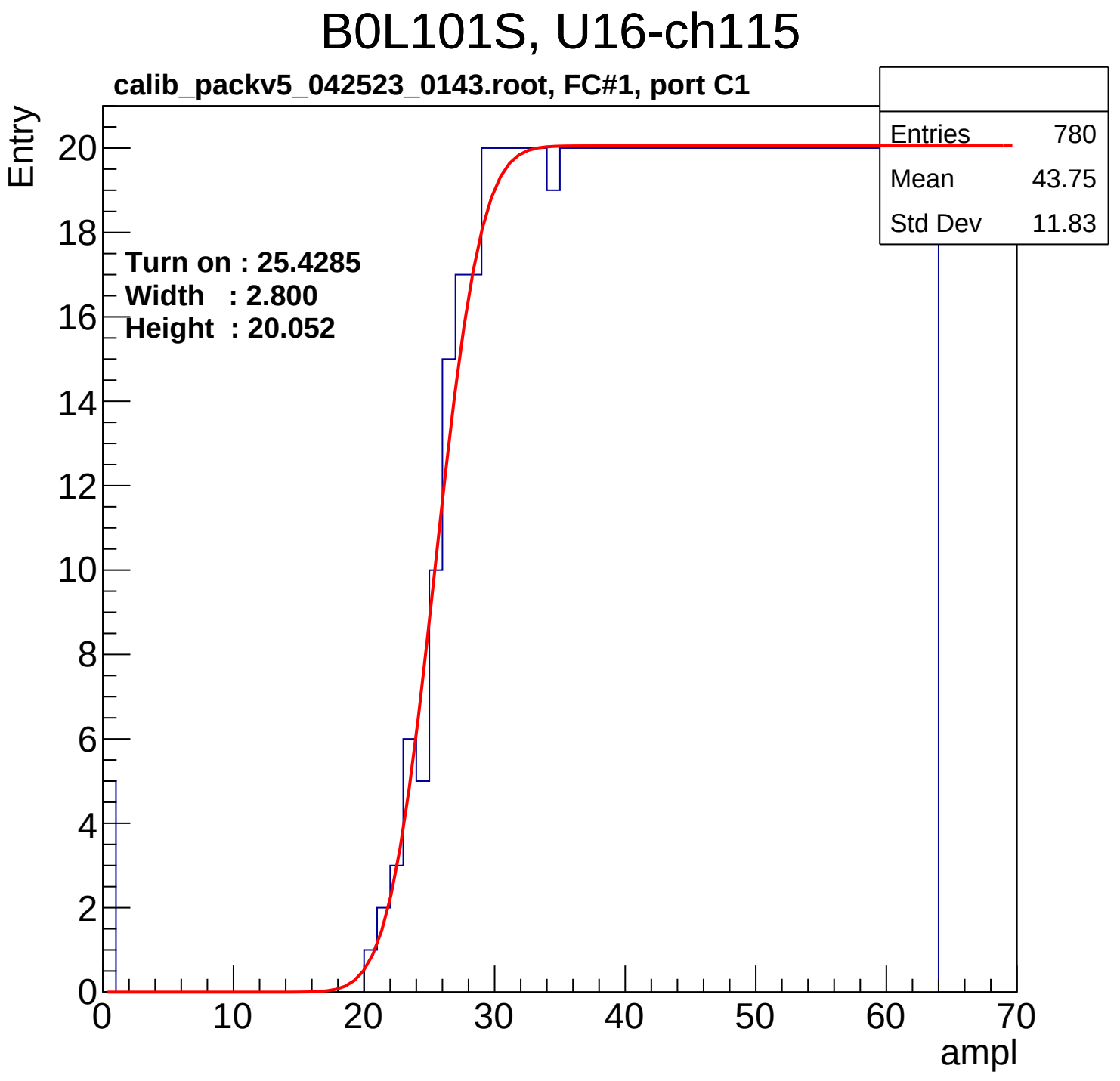
B0L101S, U16-ch115
calib_packv5_042523_0143.root, FC#1, port C1
Entries 780
Mean 43.75
Std Dev 11.83
Turn on : 25.4285
Width : 2.800
Height : 20.052
Entry
ampl
0
2
4
6
8
10
12
14
16
18
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0
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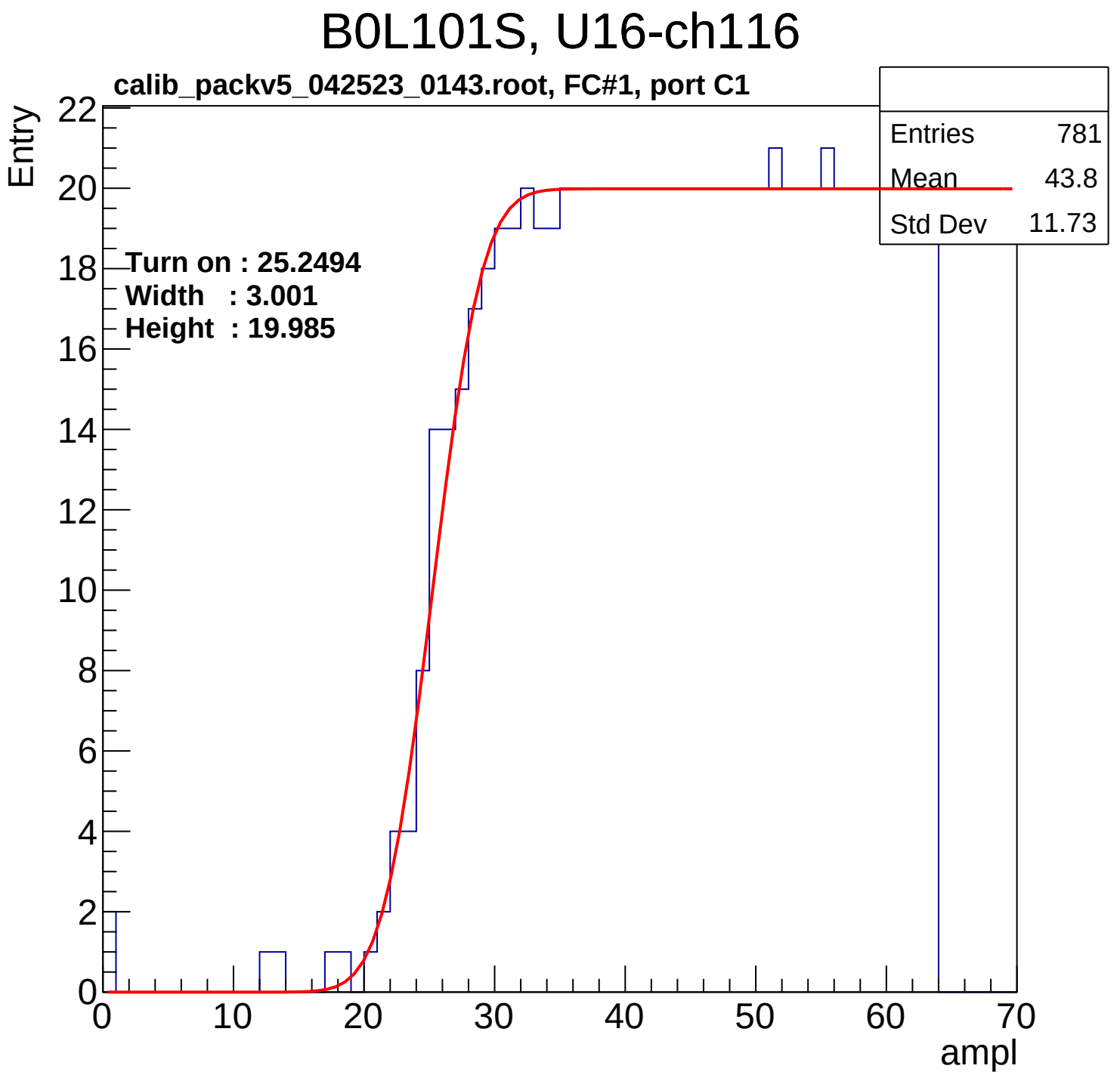
B0L101S, U16-ch116
calib_packv5_042523_0143.root, FC#1, port C1
Entries 781
Mean 43.8
Std Dev 11.73
Turn on : 25.2494
Width : 3.001
Height : 19.985
Entry
ampl
0
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6
8
10
12
14
16
18
20
22
0
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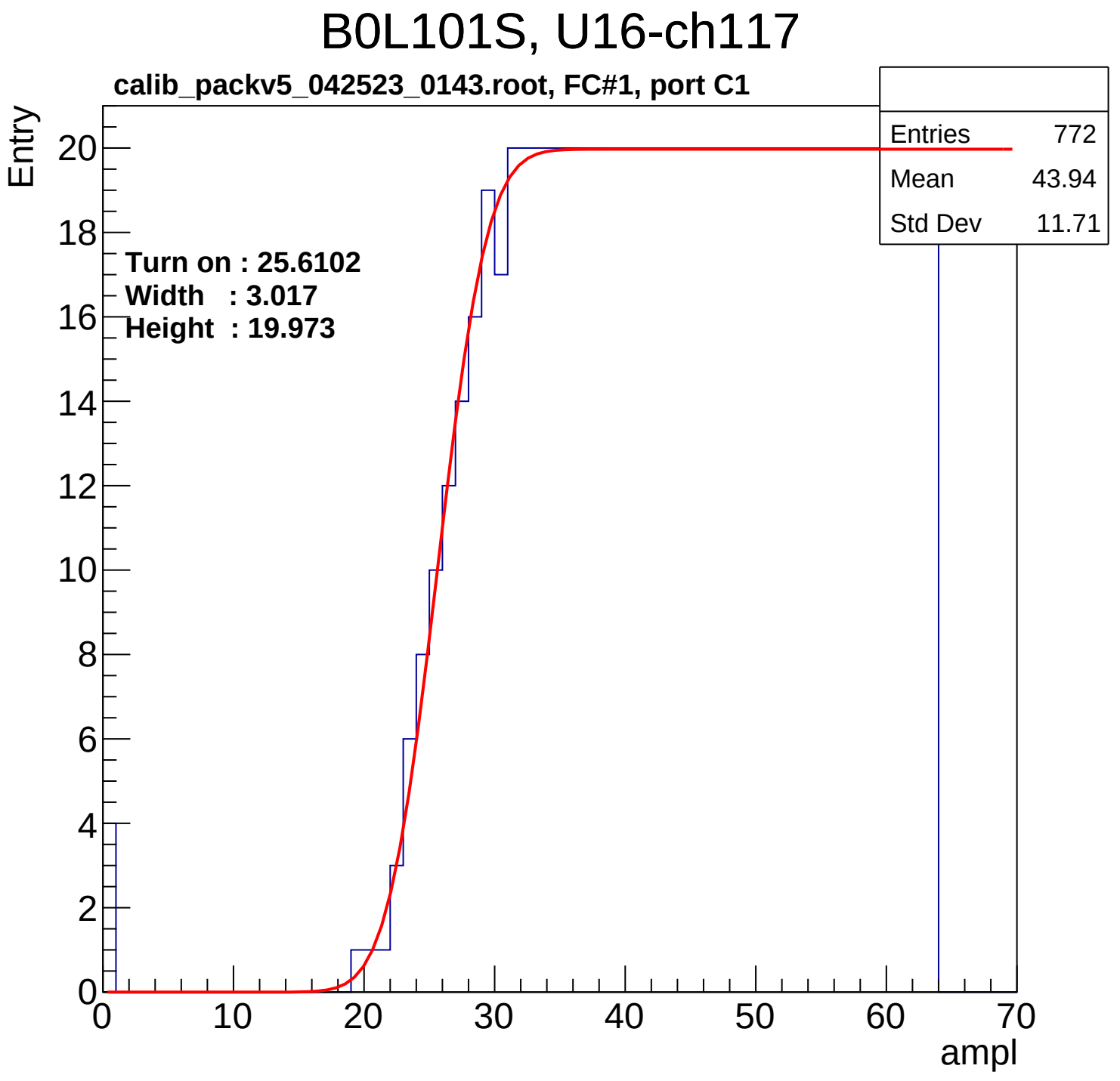
B0L101S, U16-ch117
calib_packv5_042523_0143.root, FC#1, port C1
Entries 772
Mean 43.94
Std Dev 11.71
Turn on : 25.6102
Width : 3.017
Height : 19.973
Entry
ampl
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6
8
10
12
14
16
18
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0
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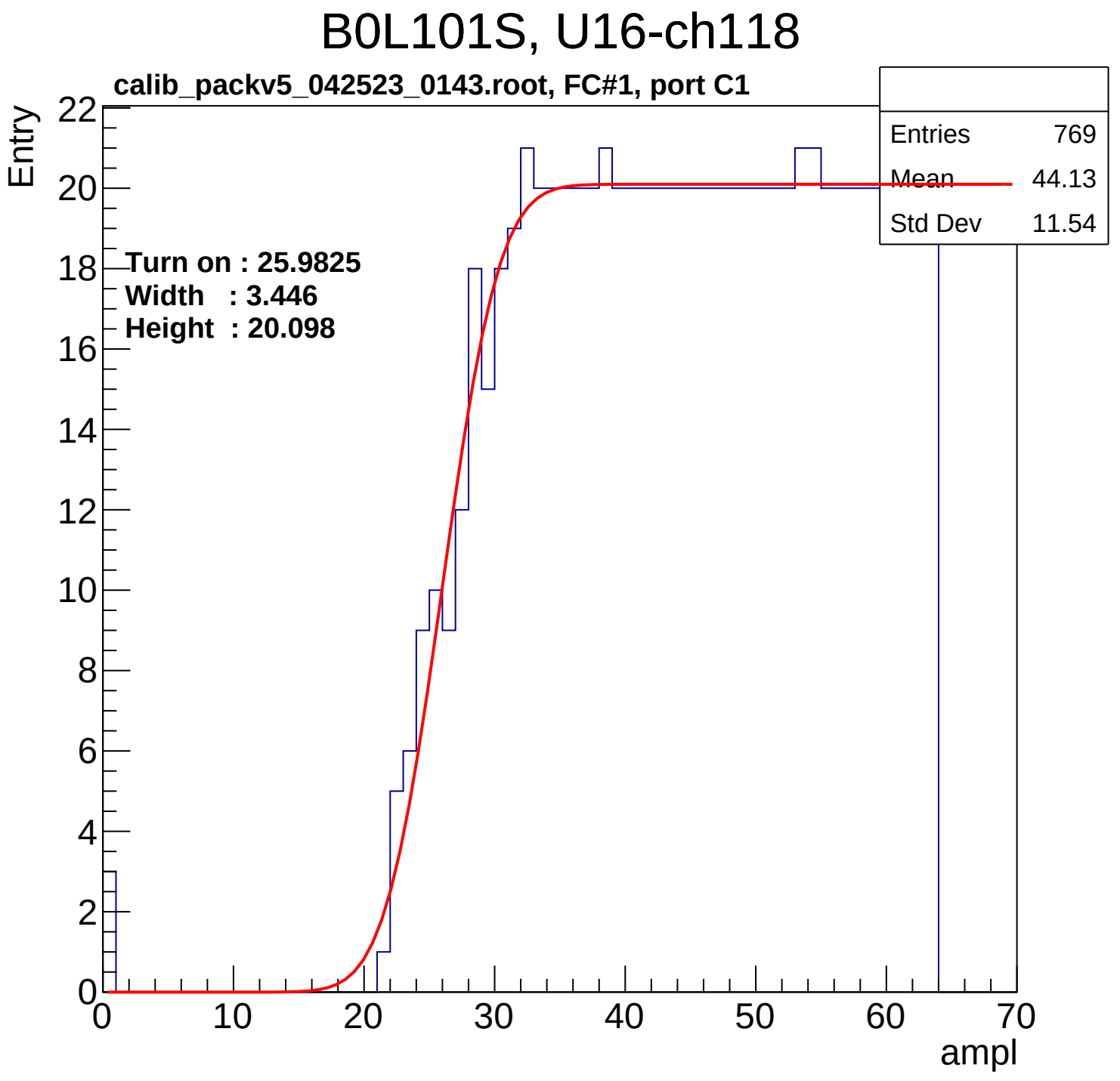
B0L101S, U16-ch118
calib_packv5_042523_0143.root, FC#1, port C1
Entries 769
Mean 44.13
Std Dev 11.54
Turn on : 25.9825
Width : 3.446
Height : 20.098
Entry
ampl
0
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8
10
12
14
16
18
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0
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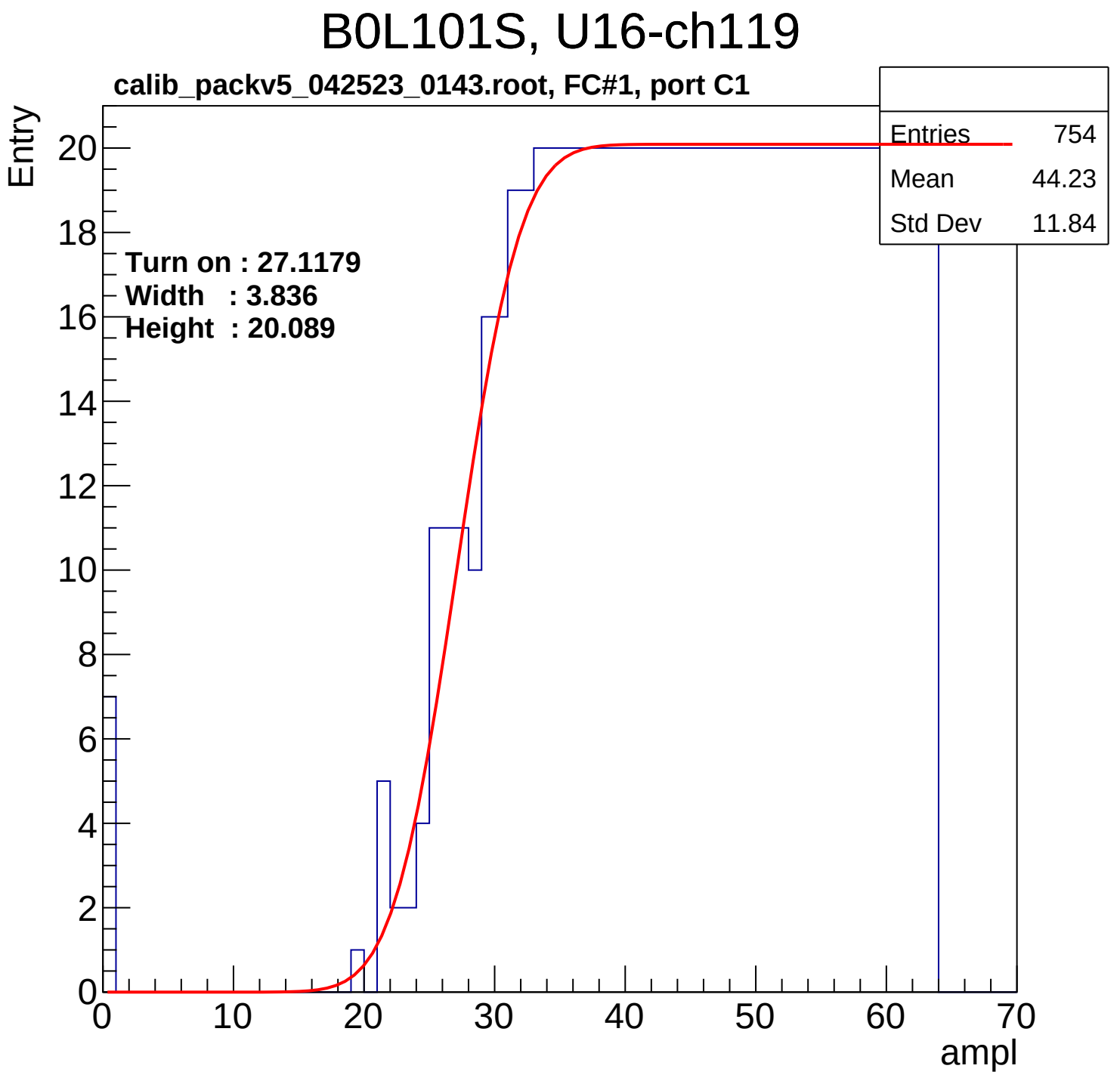
B0L101S, U16-ch119
calib_packv5_042523_0143.root, FC#1, port C1
Entries 754
Mean 44.23
Std Dev 11.84
Turn on : 27.1179
Width : 3.836
Height : 20.089
Entry
ampl
0
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4
6
8
10
12
14
16
18
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0
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20
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40
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60
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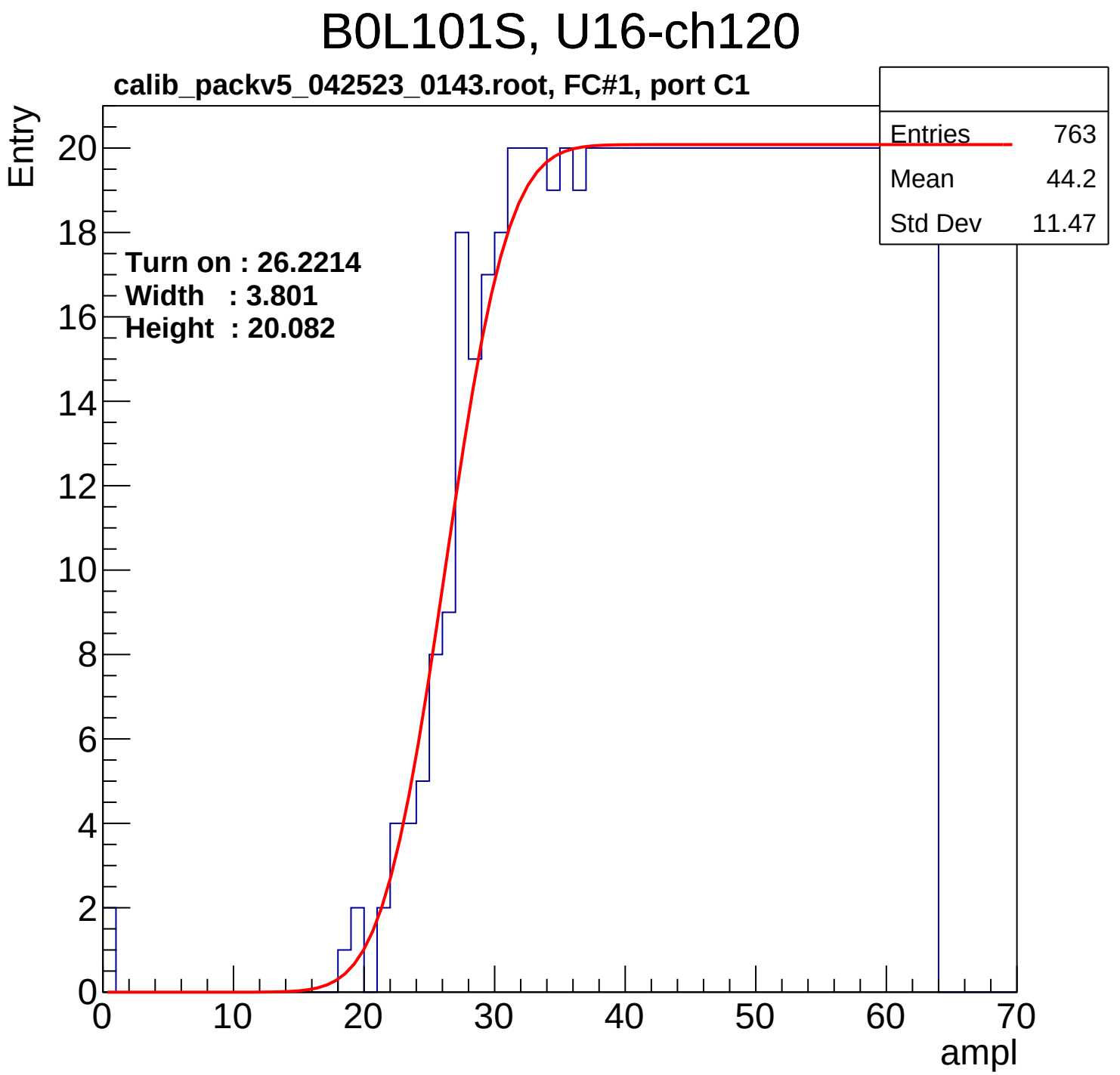
B0L101S, U16-ch120
calib_packv5_042523_0143.root, FC#1, port C1
Entries 763
Mean 44.2
Std Dev 11.47
Turn on : 26.2214
Width : 3.801
Height : 20.082
Entry
ampl
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6
8
10
12
14
16
18
20
0
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20
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40
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60
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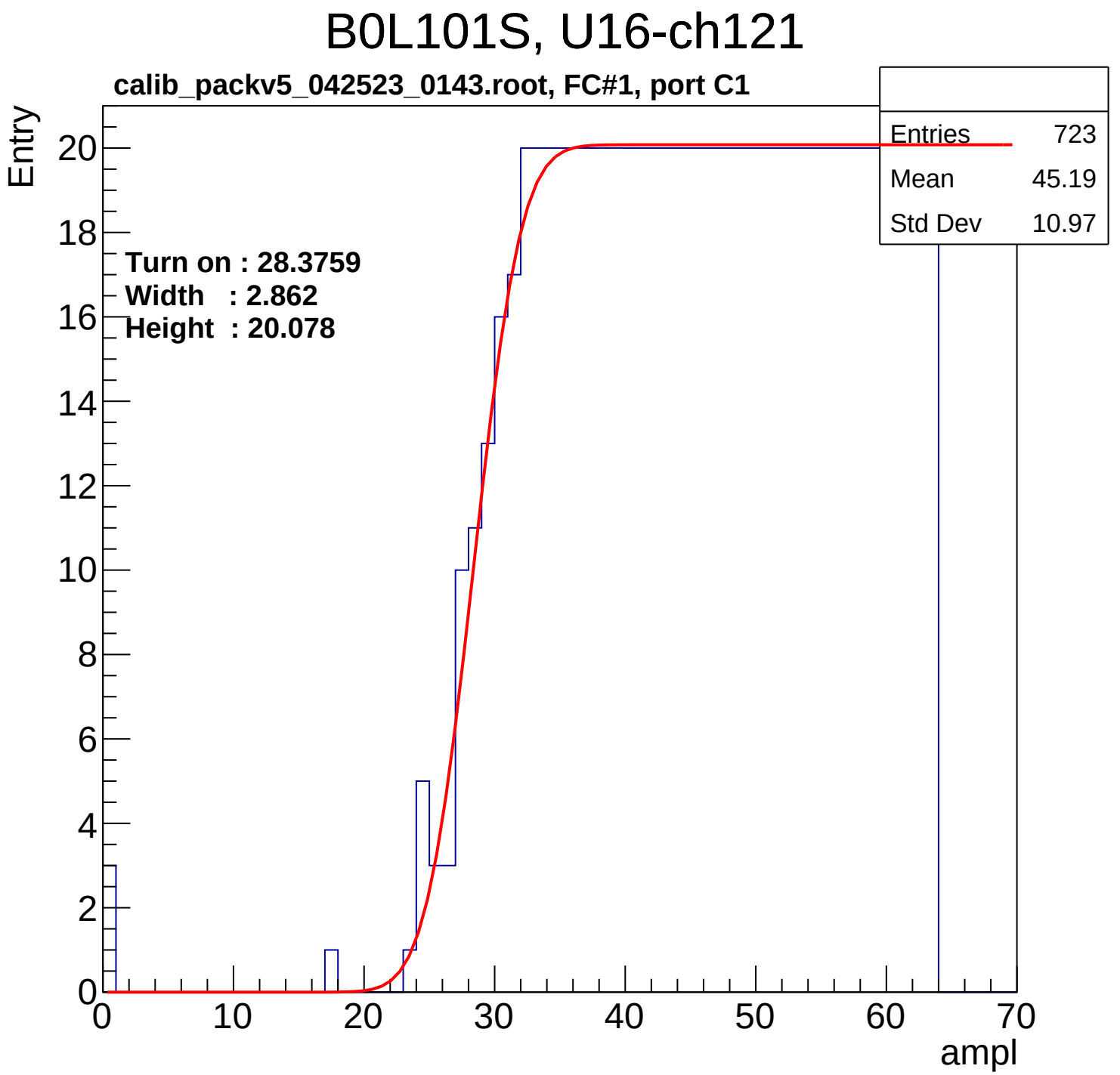
B0L101S, U16-ch121
calib_packv5_042523_0143.root, FC#1, port C1
Entries 723
Mean 45.19
Std Dev 10.97
Turn on : 28.3759
Width : 2.862
Height : 20.078
Entry
ampl
0
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6
8
10
12
14
16
18
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0
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20
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40
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60
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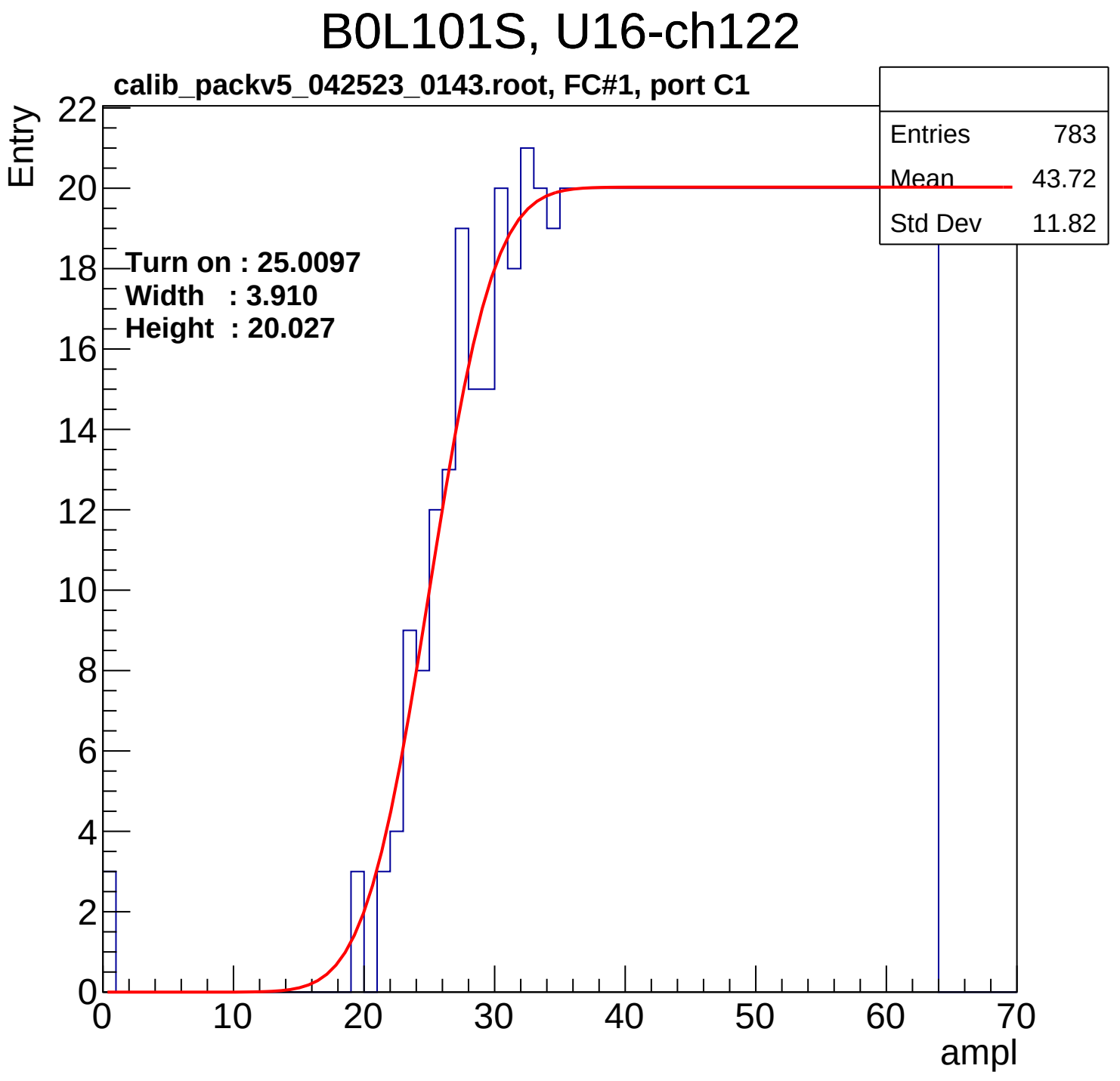
B0L101S, U16-ch122
calib_packv5_042523_0143.root, FC#1, port C1
Entries 783
Mean 43.72
Std Dev 11.82
Turn on : 25.0097
Width : 3.910
Height : 20.027
Entry
ampl
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6
8
10
12
14
16
18
20
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0
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60
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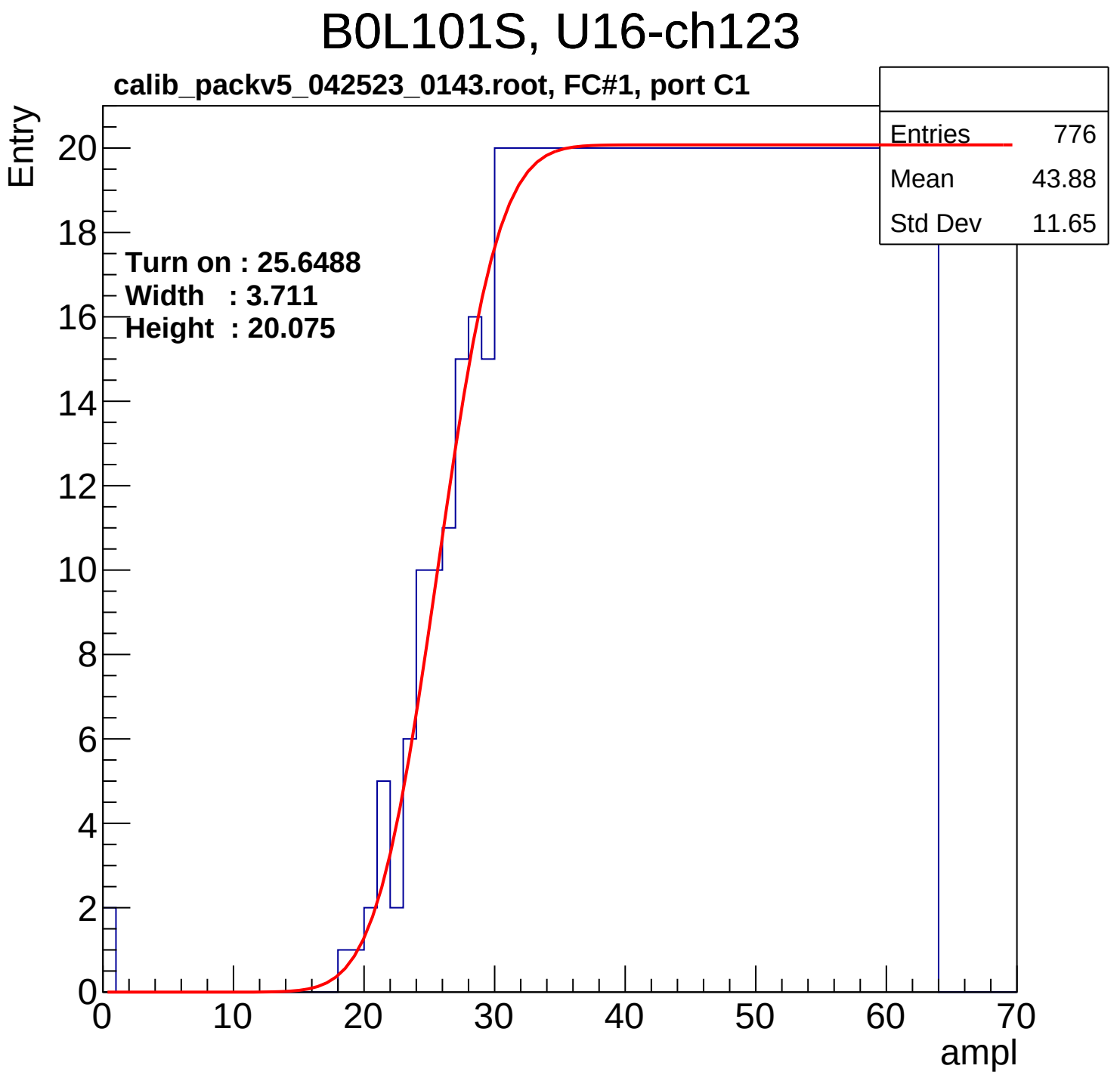
B0L101S, U16-ch123
calib_packv5_042523_0143.root, FC#1, port C1
Entries 776
Mean 43.88
Std Dev 11.65
Turn on : 25.6488
Width : 3.711
Height : 20.075
Entry
ampl
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6
8
10
12
14
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0
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60
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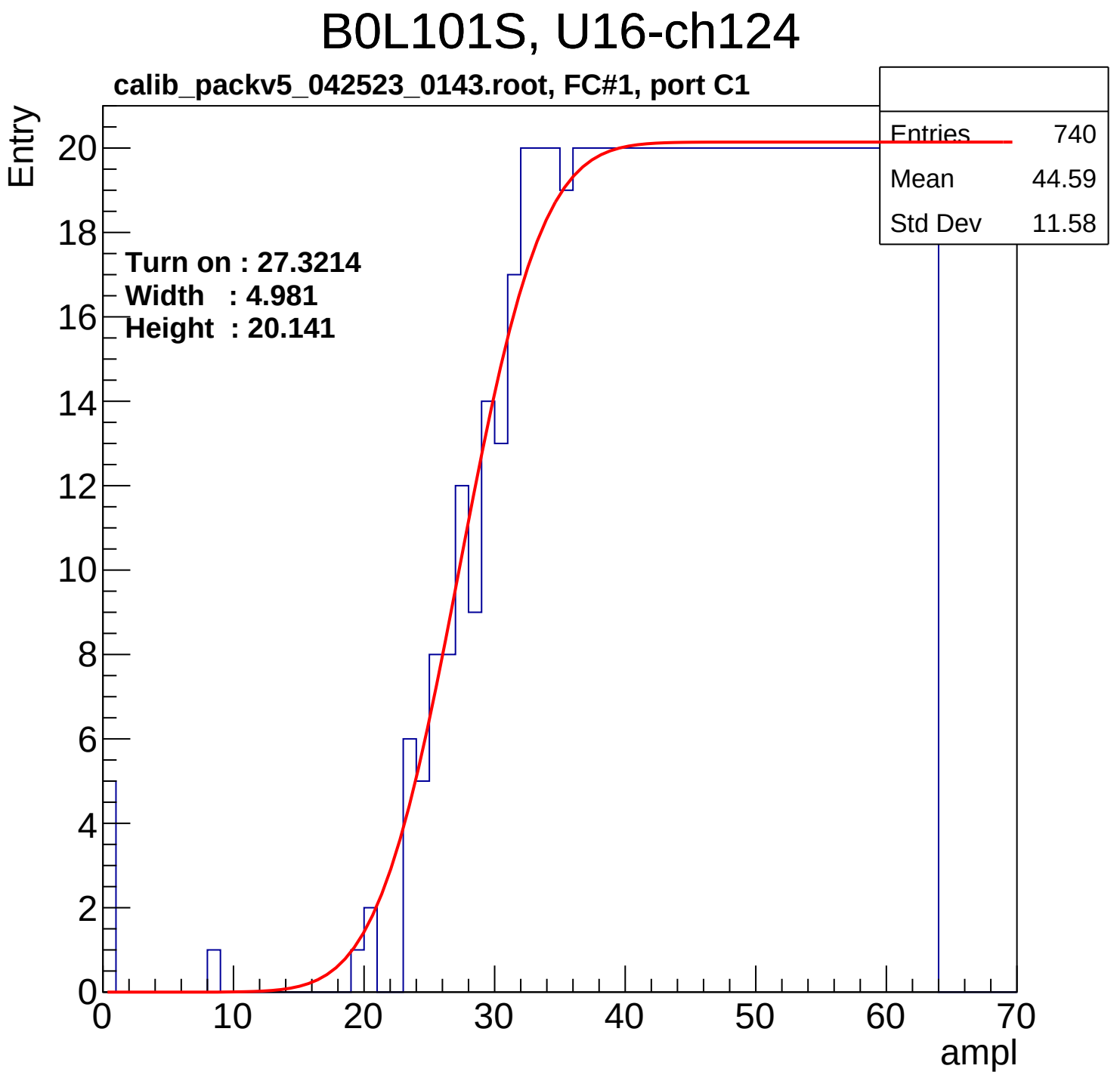
B0L101S, U16-ch124
calib_packv5_042523_0143.root, FC#1, port C1
Entries 740
Mean 44.59
Std Dev 11.58
Turn on : 27.3214
Width : 4.981
Height : 20.141
Entry
ampl
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6
8
10
12
14
16
18
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0
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60
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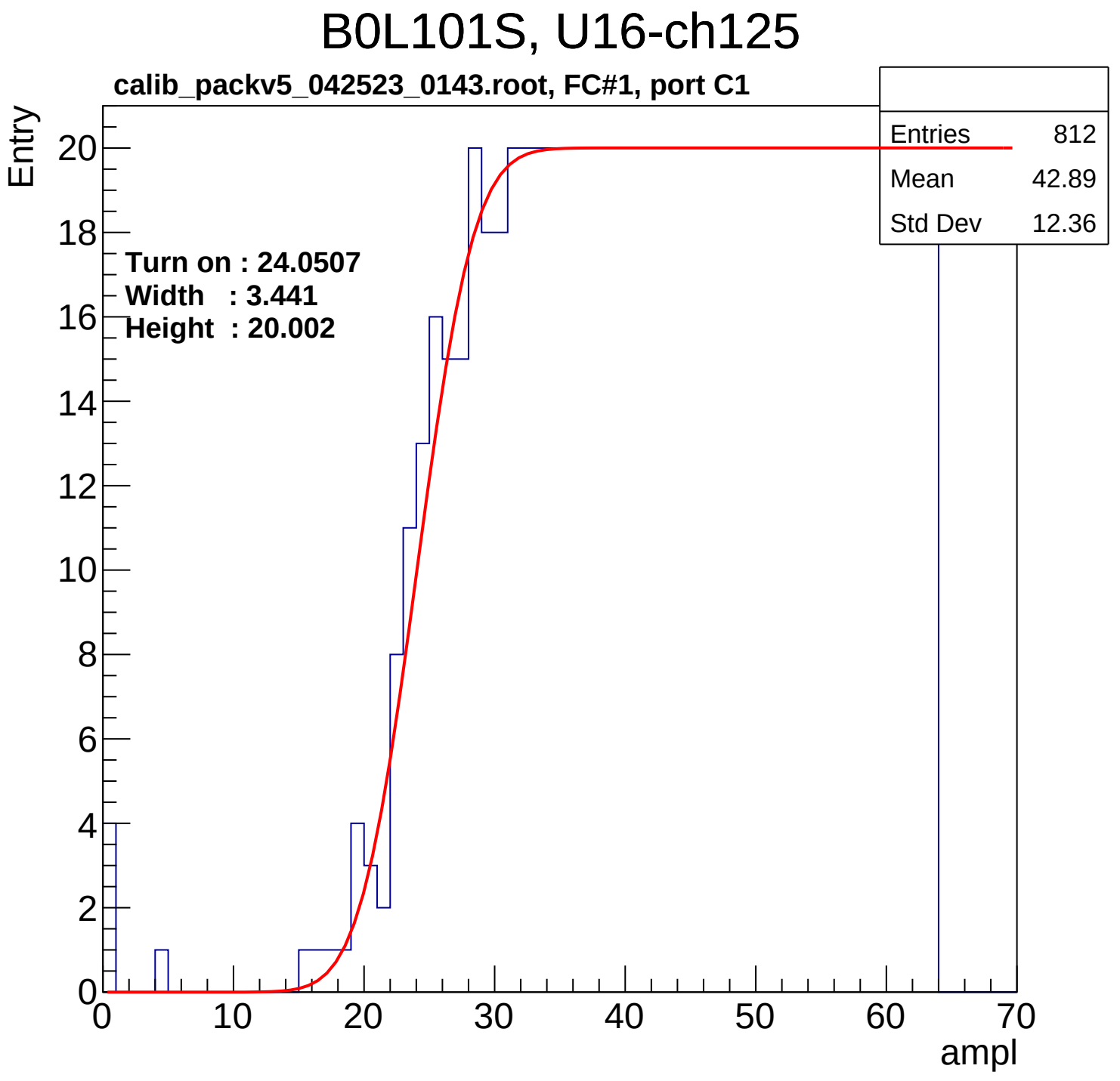
B0L101S, U16-ch125
calib_packv5_042523_0143.root, FC#1, port C1
Entries 812
Mean 42.89
Std Dev 12.36
Turn on : 24.0507
Width : 3.441
Height : 20.002
Entry
ampl
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6
8
10
12
14
16
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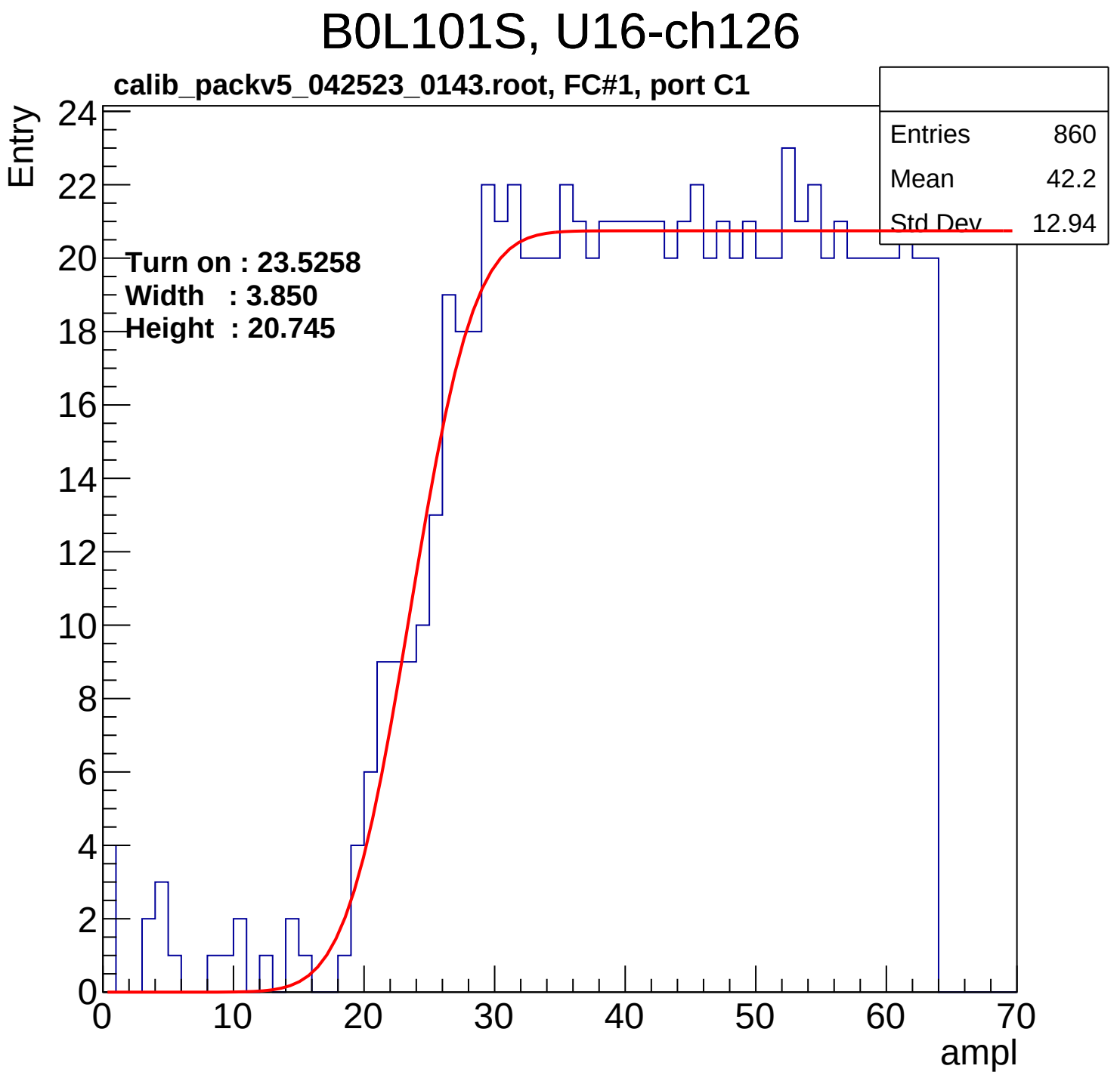
B0L101S, U16-ch126
calib_packv5_042523_0143.root, FC#1, port C1
Entries 860
Mean 42.2
Std Dev 12.94
Turn on : 23.5258
Width : 3.850
Height : 20.745
Entry
ampl
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10
12
14
16
18
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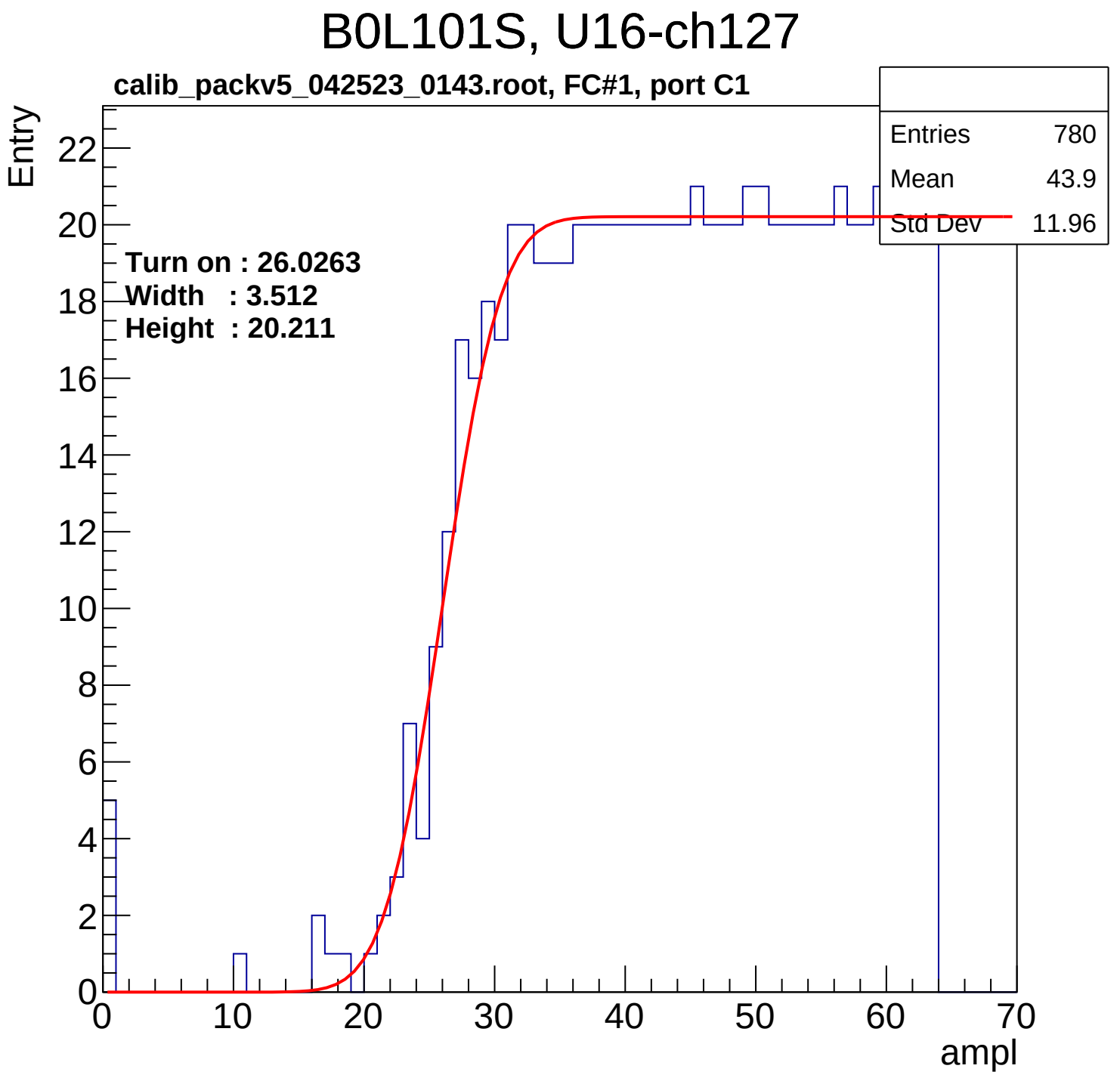
B0L101S, U16-ch127
calib_packv5_042523_0143.root, FC#1, port C1
Entries 780
Mean 43.9
Std Dev 11.96
Turn on : 26.0263
Width : 3.512
Height : 20.211
Entry
ampl
0
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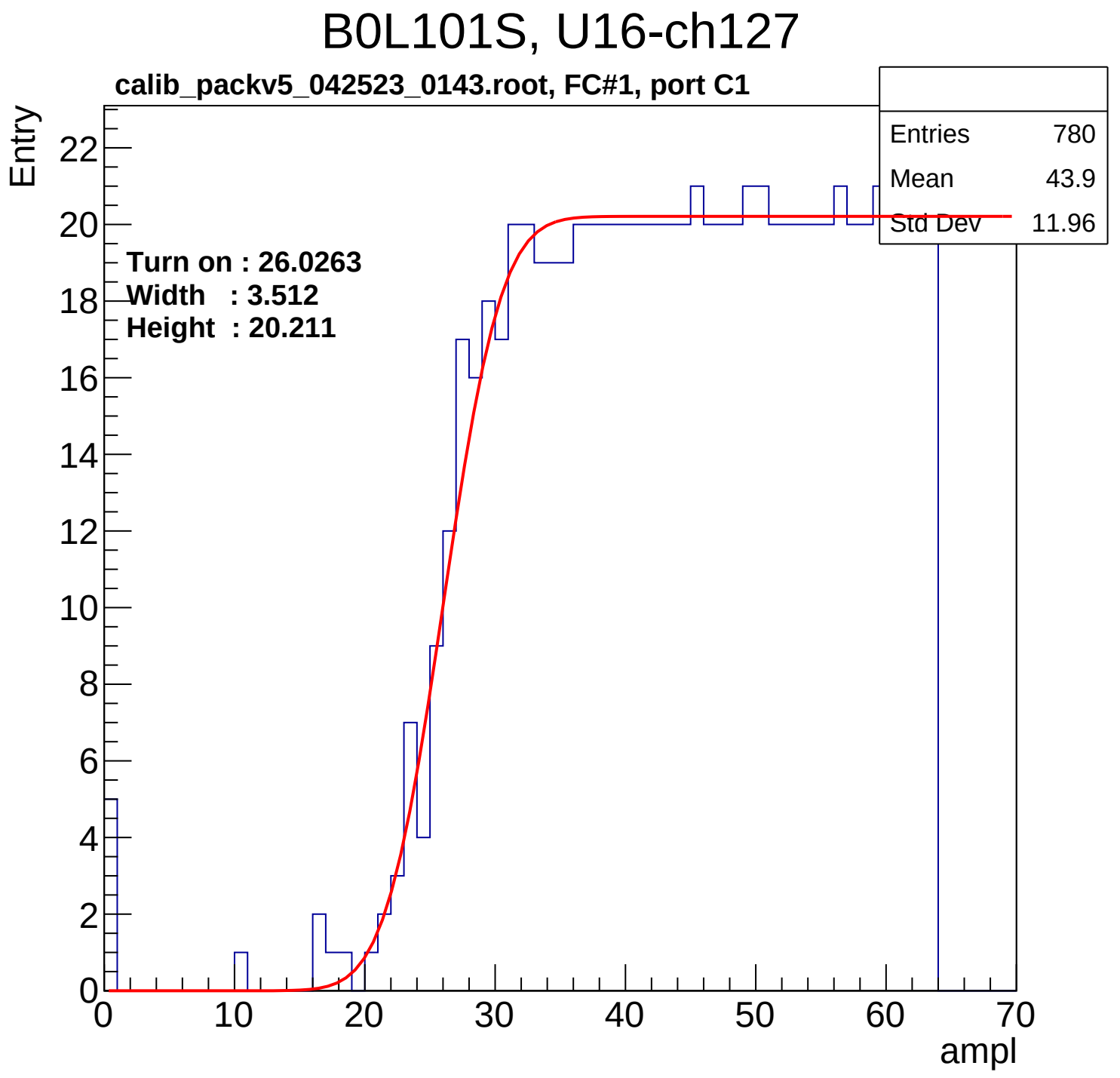
B0L101S, U16-ch127
calib_packv5_042523_0143.root, FC#1, port C1
Entries 780
Mean 43.9
Std Dev 11.96
Turn on : 26.0263
Width : 3.512
Height : 20.211
Entry
ampl
0
2
4
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8
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