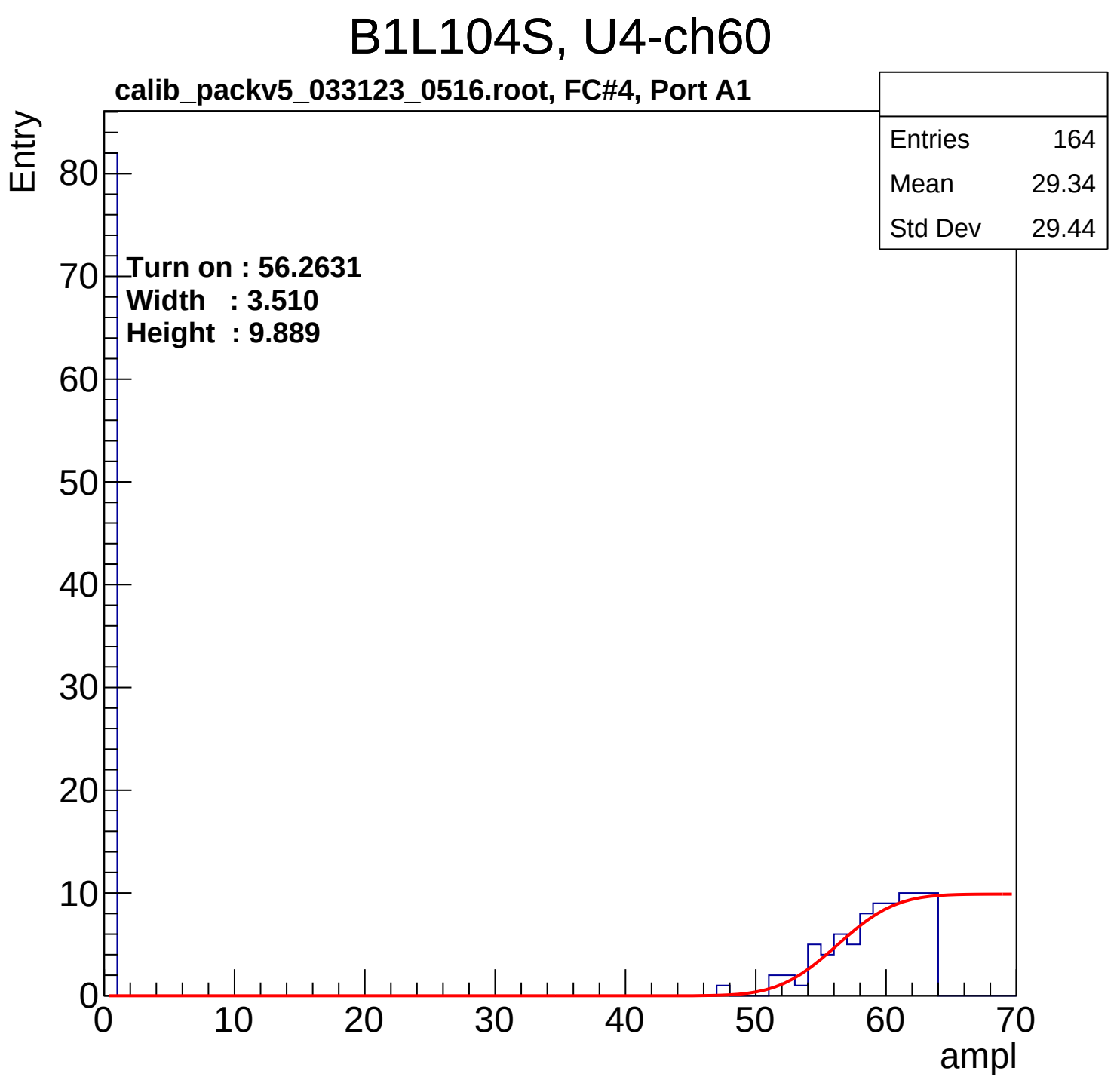
B1L104S, U4-ch60
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 164
Mean 29.34
Std Dev 29.44
Turn on : 56.2631
Width : 3.510
Height : 9.889
Entry
ampl
0
10
20
30
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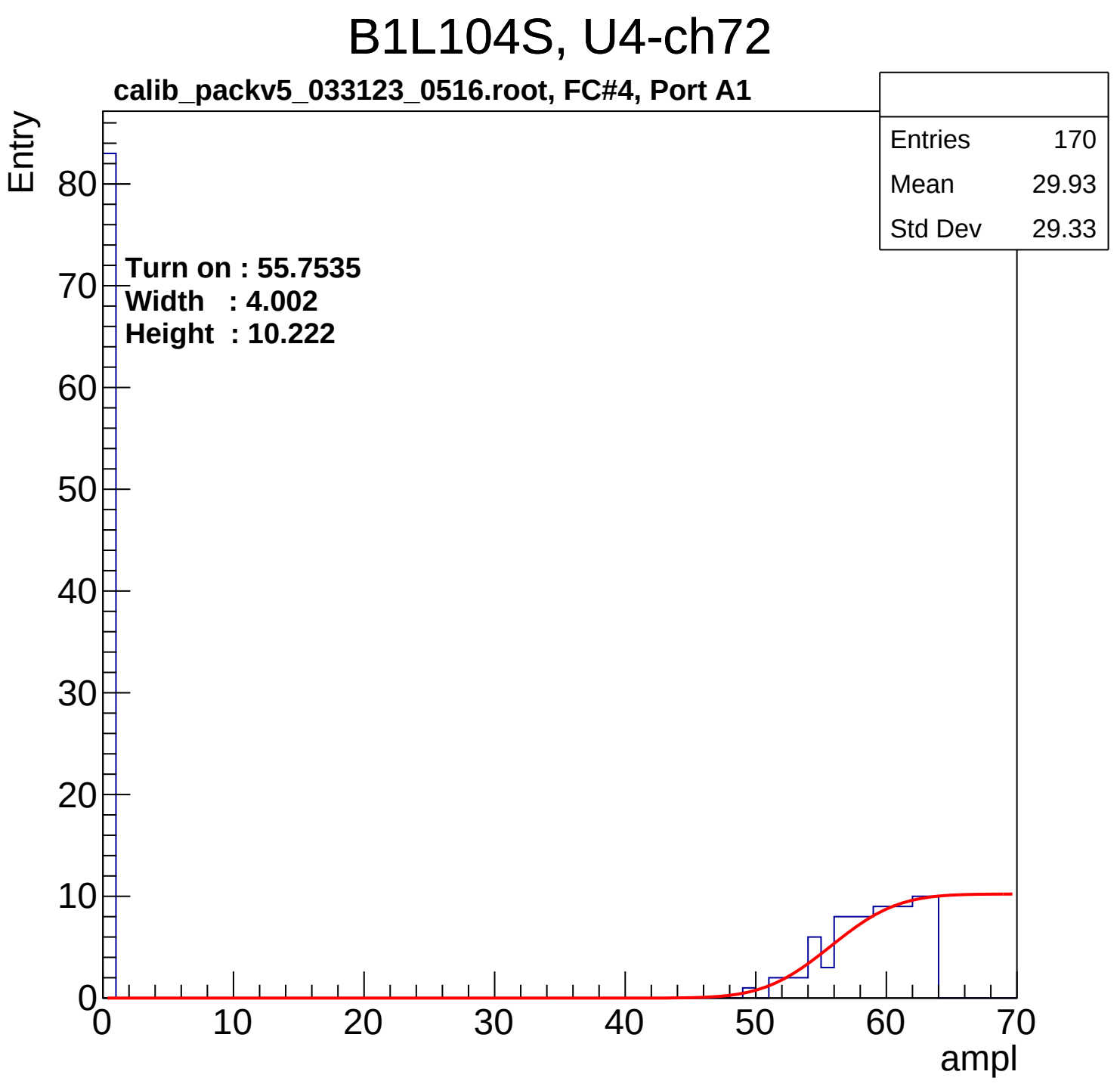
50
60
70
80


B1L104S, U4-ch72
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 170
Mean 29.93
Std Dev 29.33
Turn on : 55.7535
Width : 4.002
Height : 10.222
Entry
ampl
0
10
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30
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70
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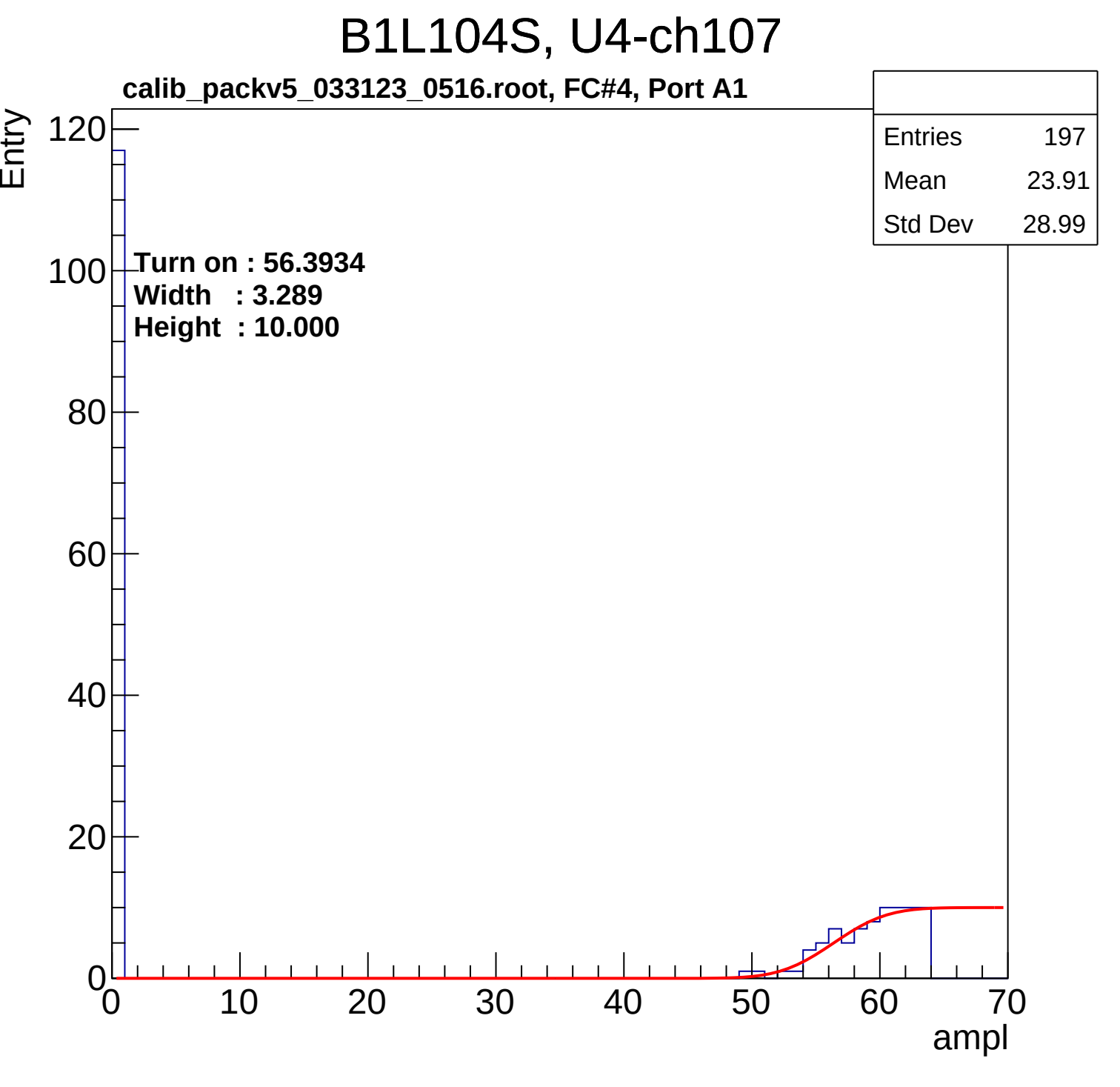
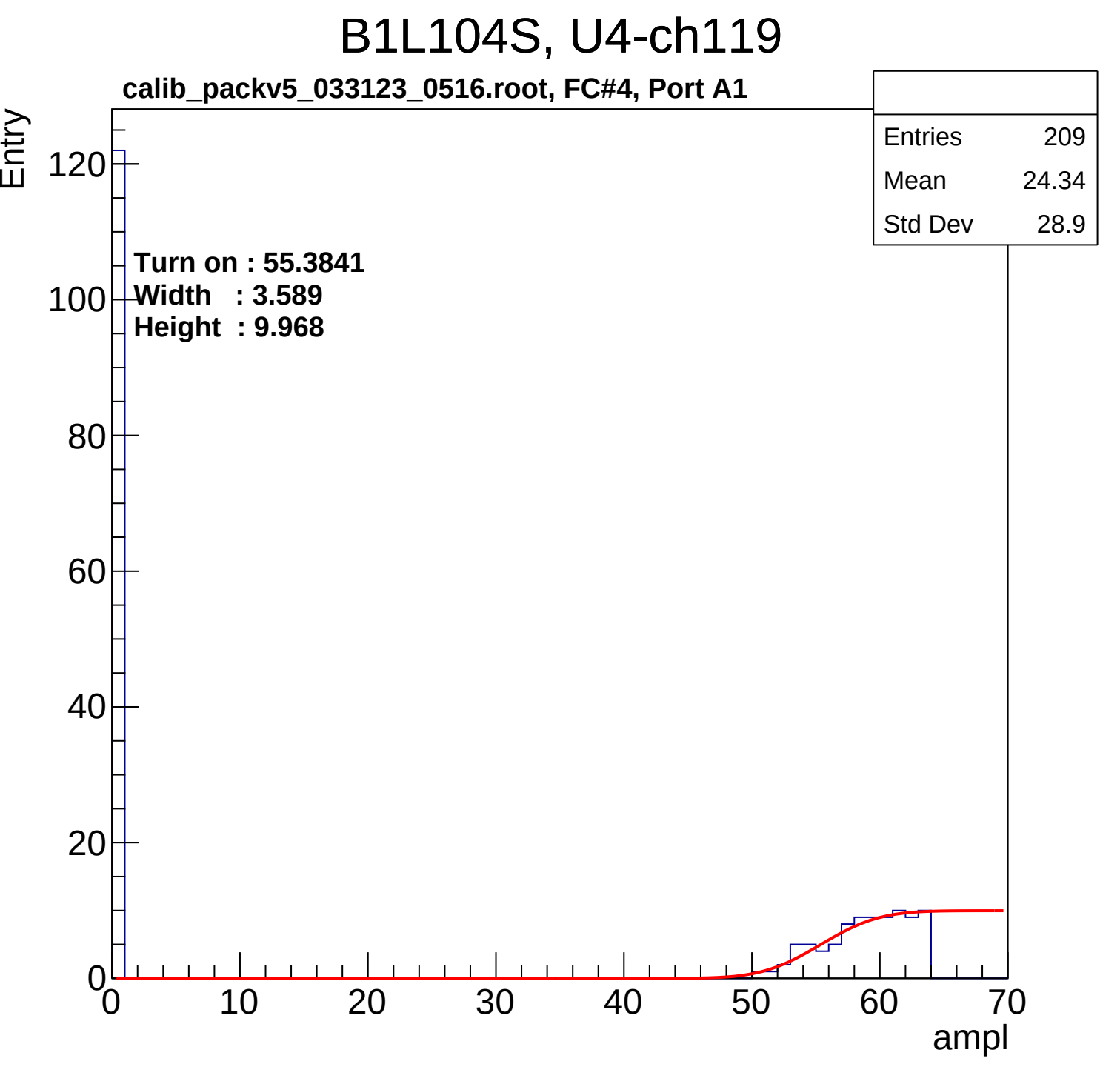
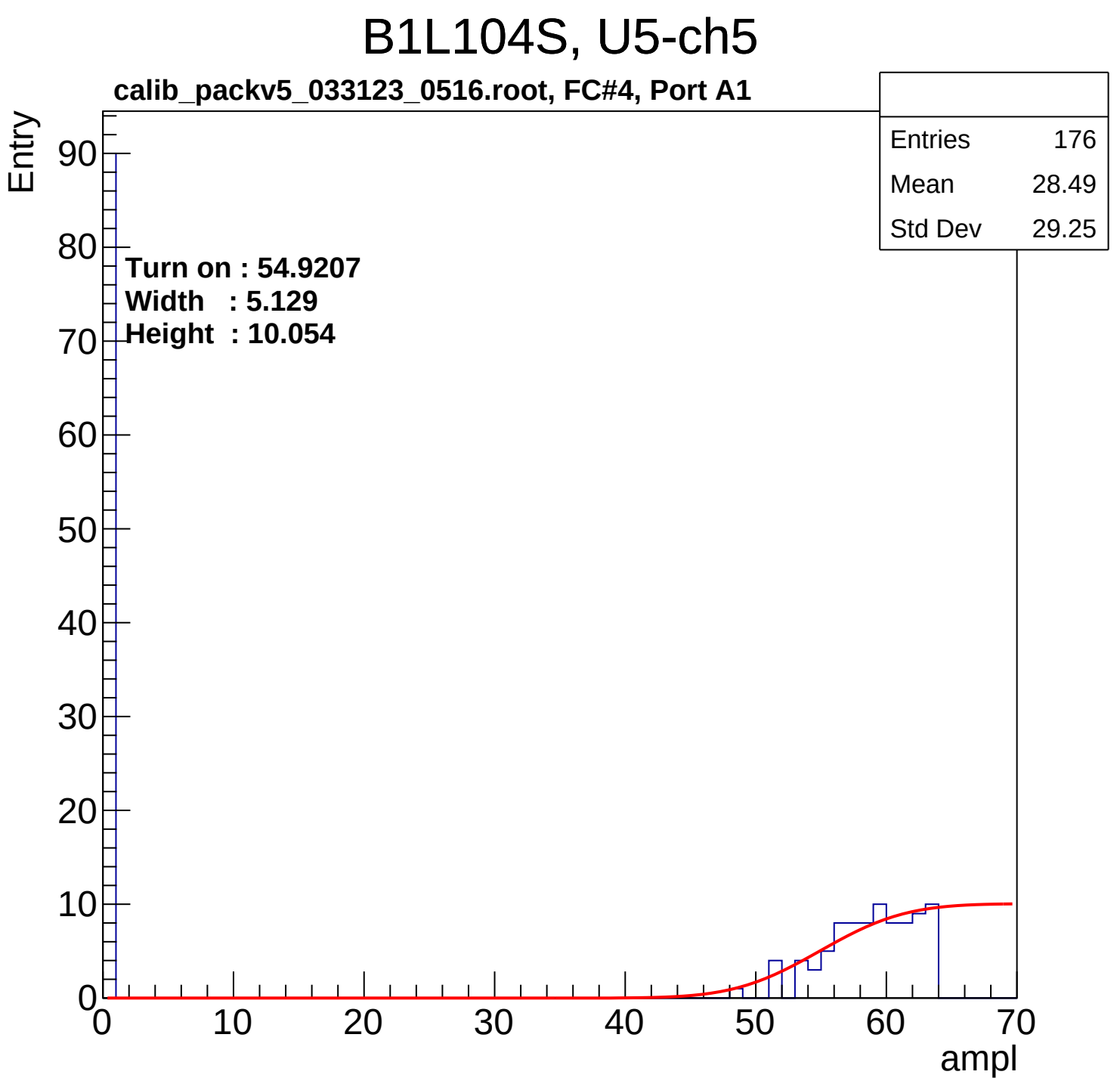
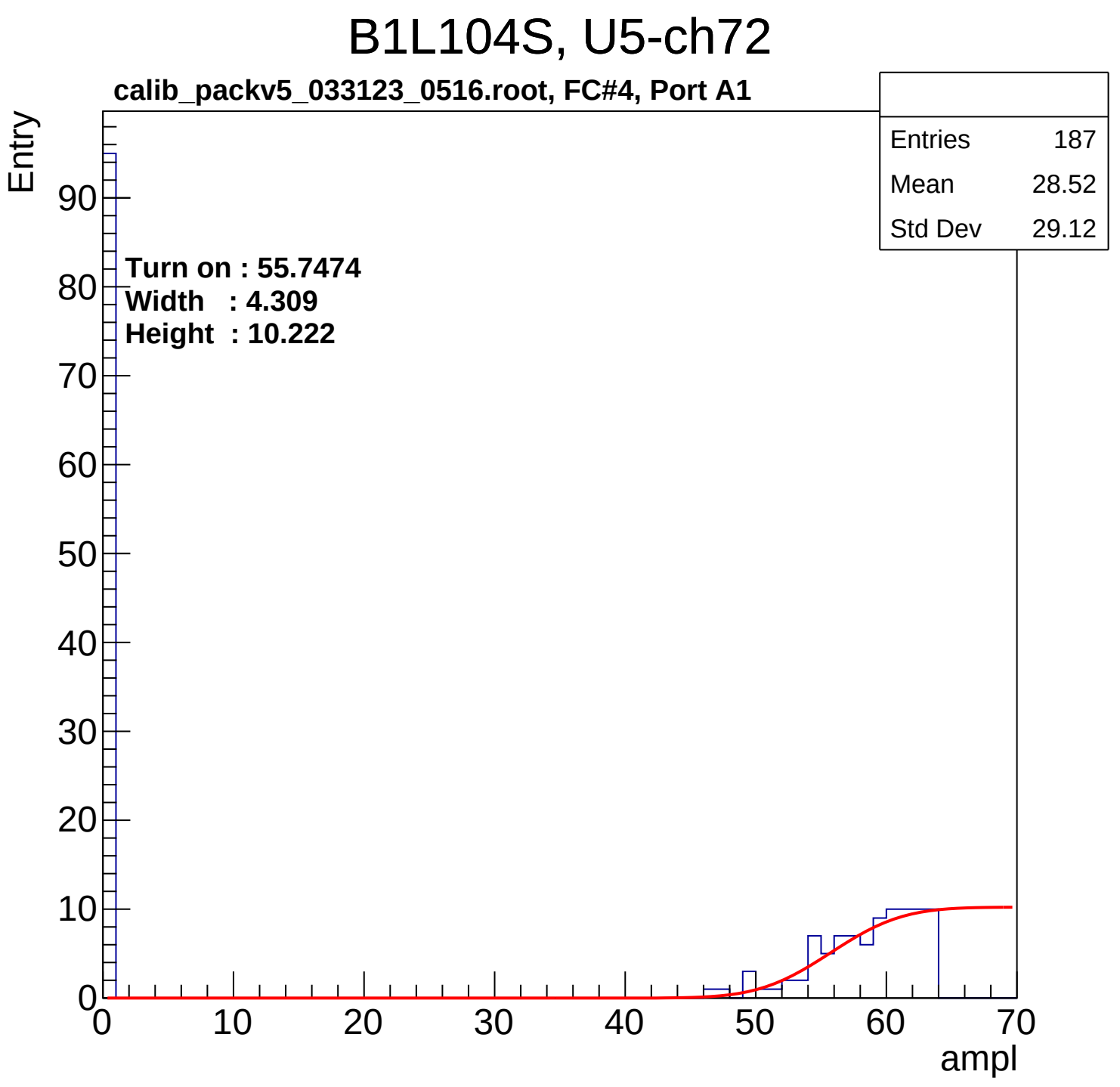
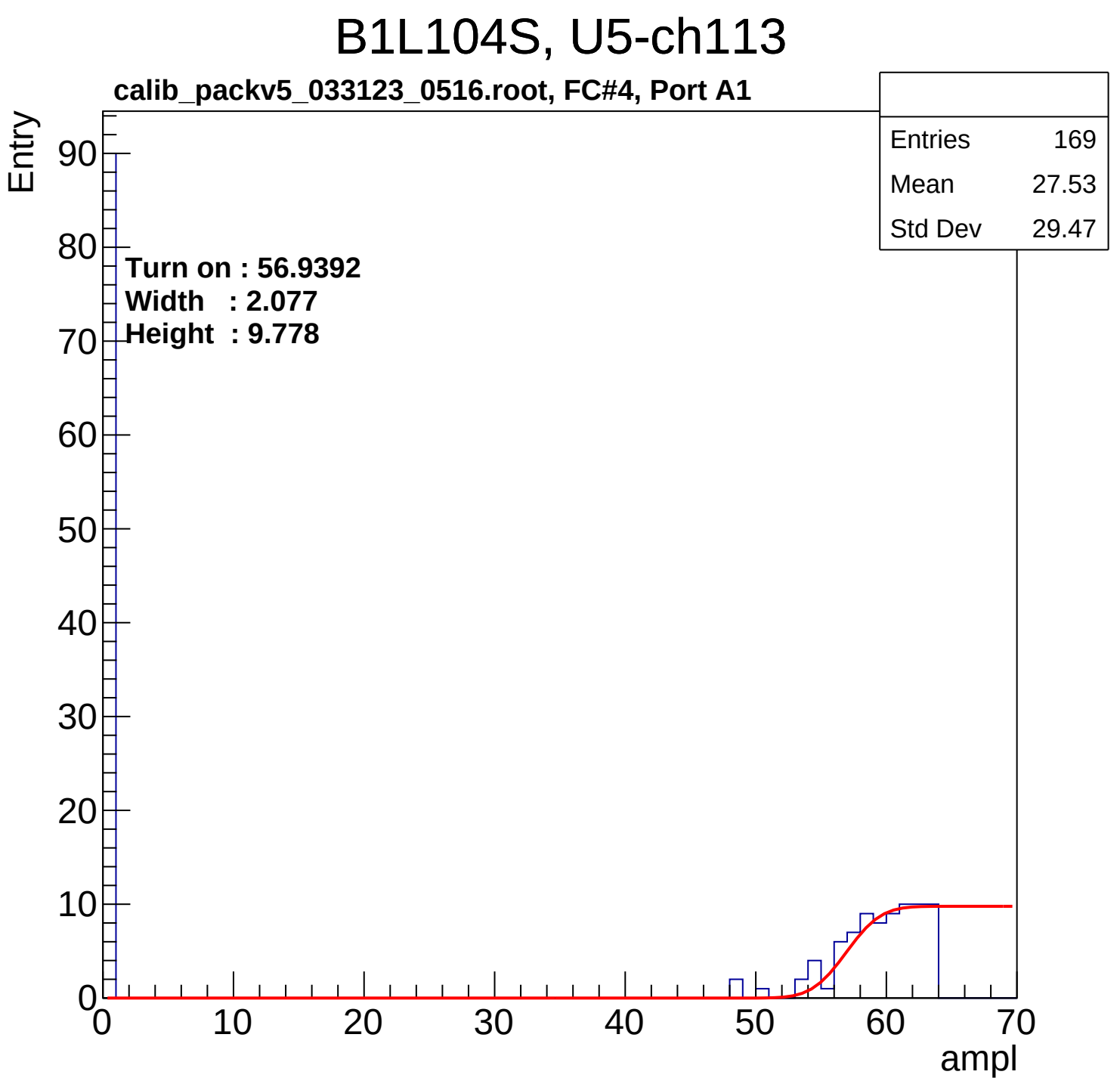
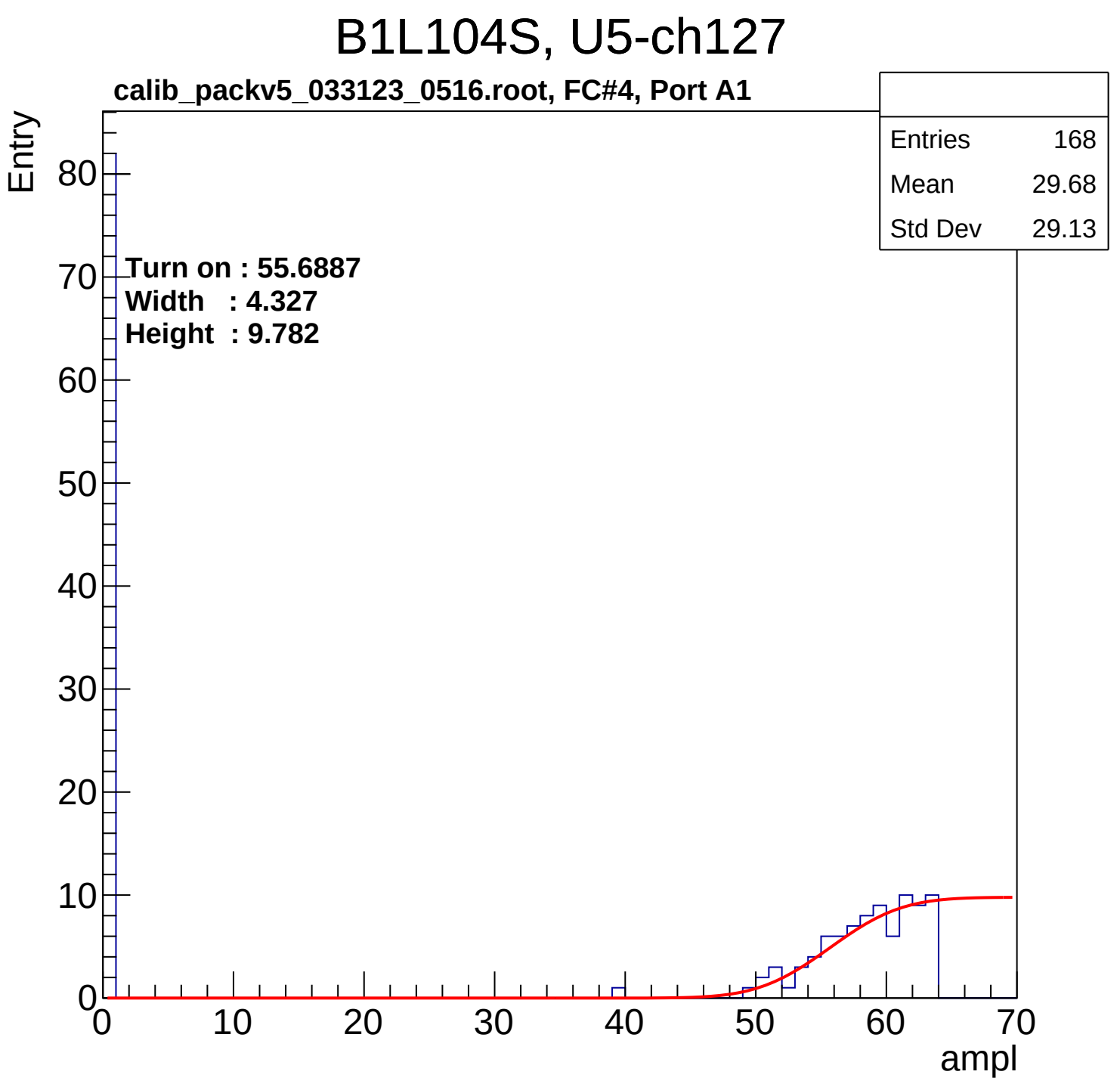

B1L104S, U4-ch107
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 197
Mean 23.91
Std Dev 28.99
Turn on : 56.3934
Width : 3.289
Height : 10.000
Entry
ampl
0
20
40
60
80
100
120
0
10
20
30
40
50
60
70


B1L104S, U4-ch119
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 209
Mean 24.34
Std Dev 28.9
Turn on : 55.3841
Width : 3.589
Height : 9.968
Entry
0
20
40
60
80
100
120
0
10
20
30
40
50
60
70
ampl


B1L104S, U5-ch5
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 176
Mean 28.49
Std Dev 29.25
Turn on : 54.9207
Width : 5.129
Height : 10.054
Entry
ampl
0
10
20
30
40
50
60
70
80
90


B1L104S, U5-ch72
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 187
Mean 28.52
Std Dev 29.12
Turn on : 55.7474
Width : 4.309
Height : 10.222
Entry
ampl
0
10
20
30
40
50
60
70
80
90


B1L104S, U5-ch113
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 169
Mean 27.53
Std Dev 29.47
Turn on : 56.9392
Width : 2.077
Height : 9.778
Entry
ampl
0
10
20
30
40
50
60
70
80
90


B1L104S, U5-ch127
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 168
Mean 29.68
Std Dev 29.13
Turn on : 55.6887
Width : 4.327
Height : 9.782
Entry
ampl
0
10
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30
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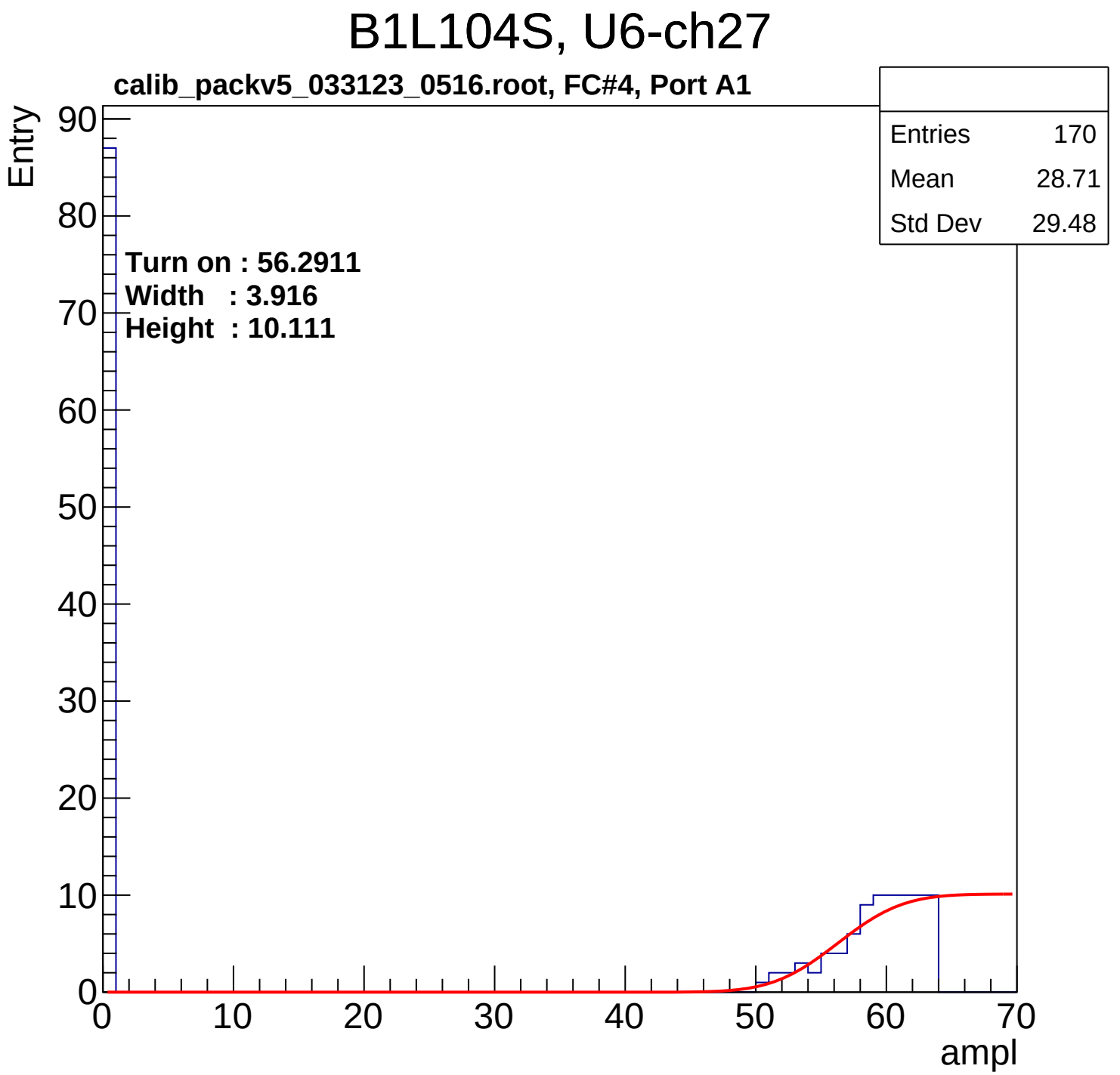
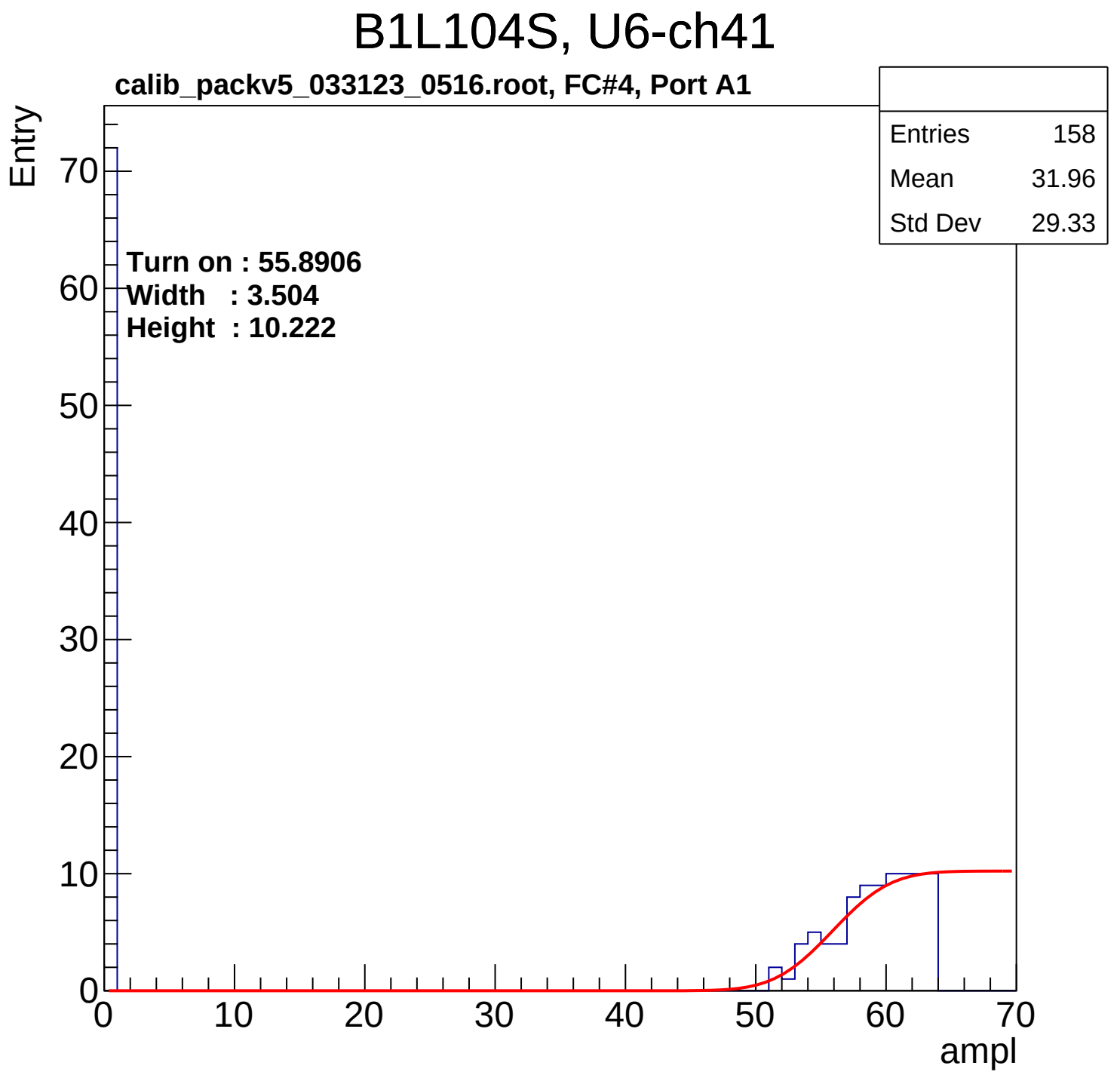
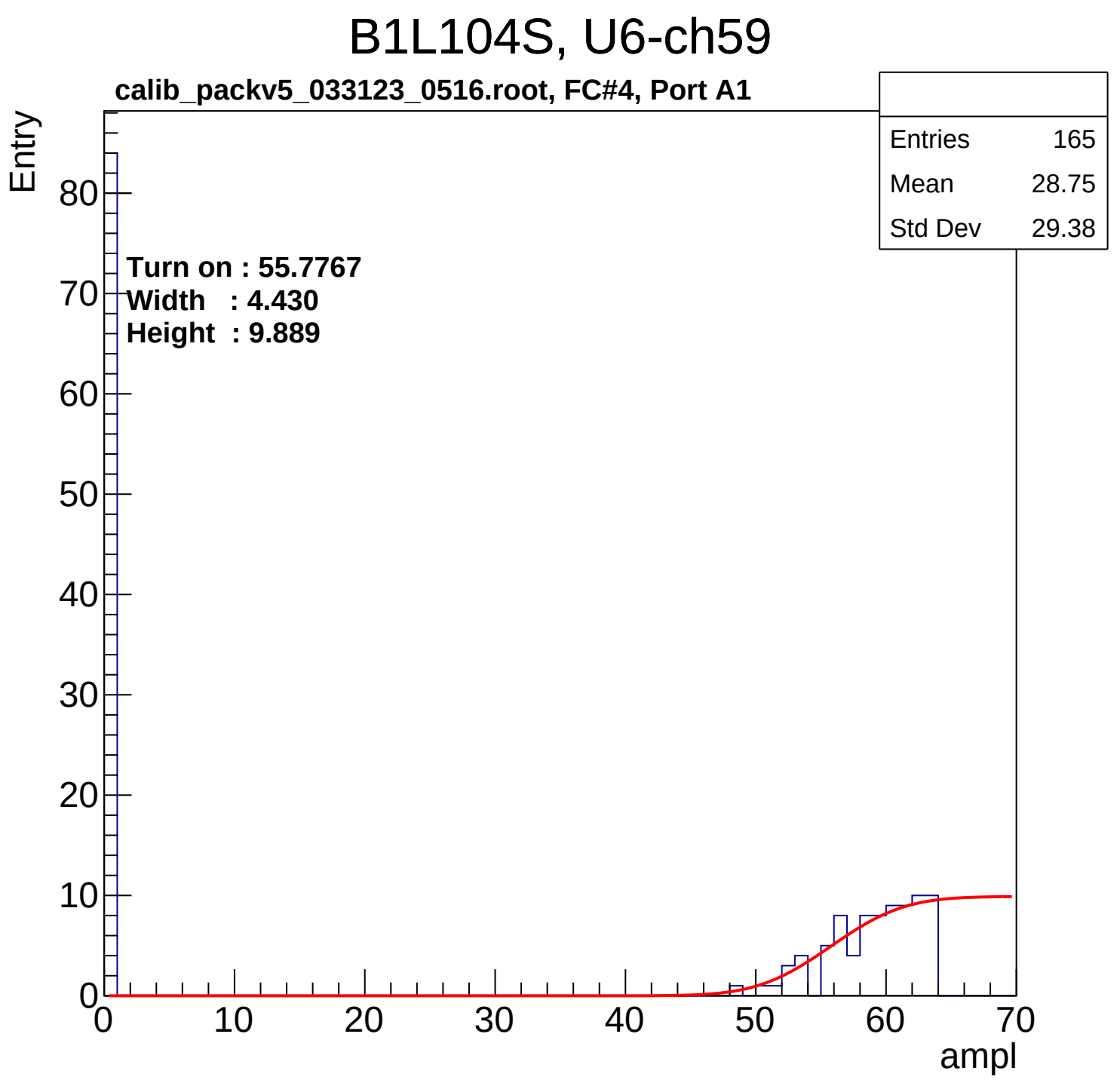
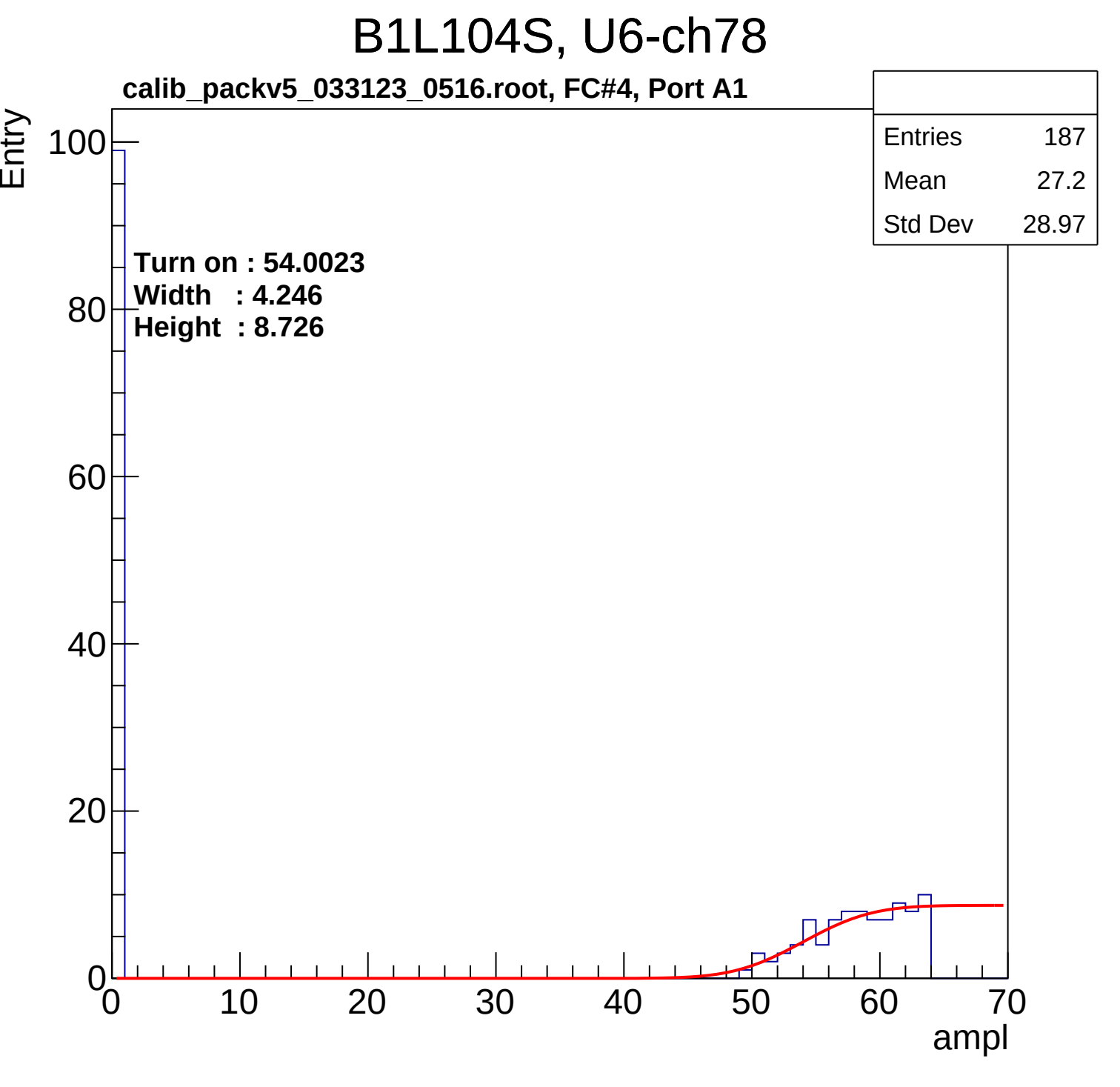
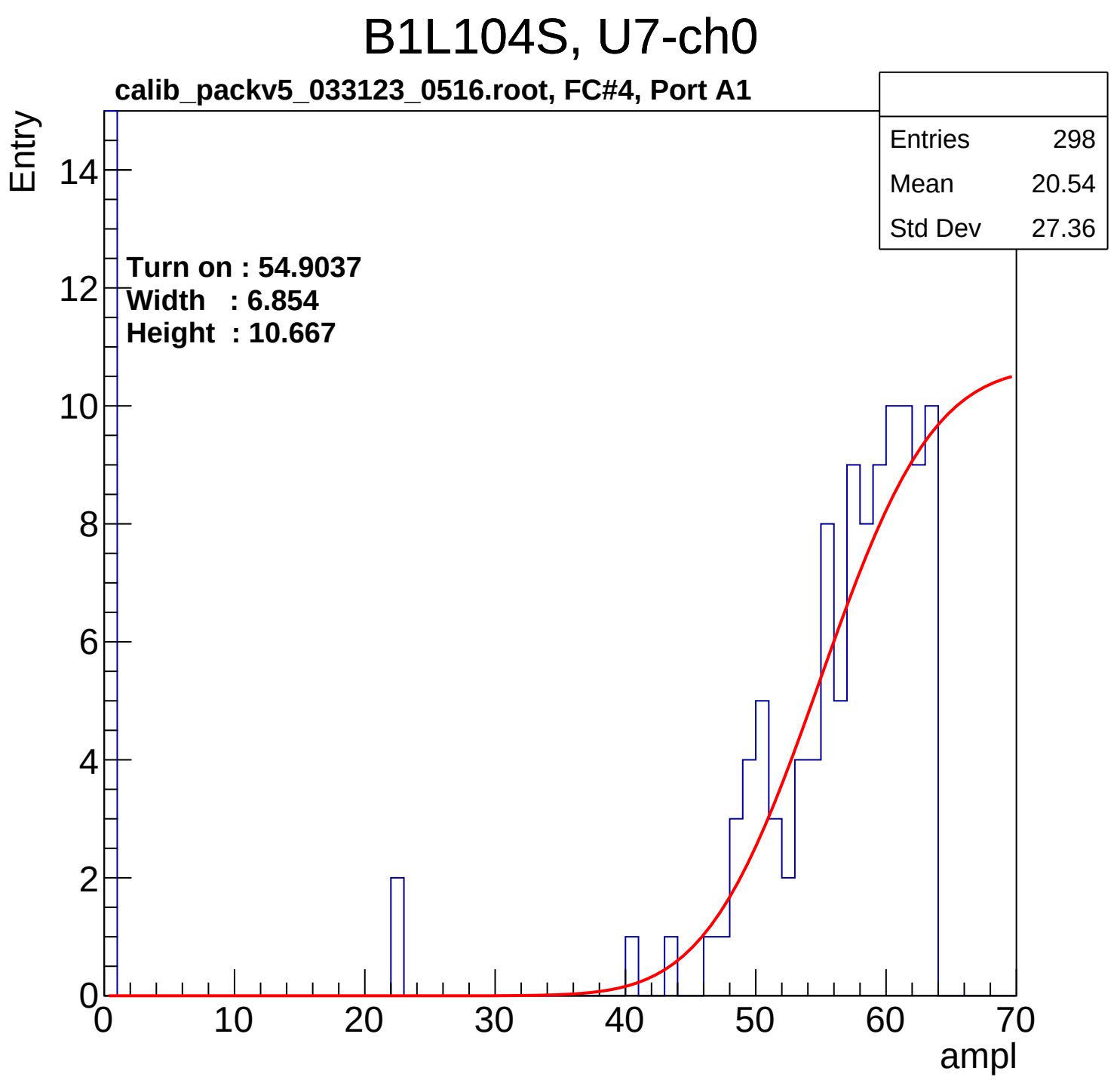
50
60
70
80

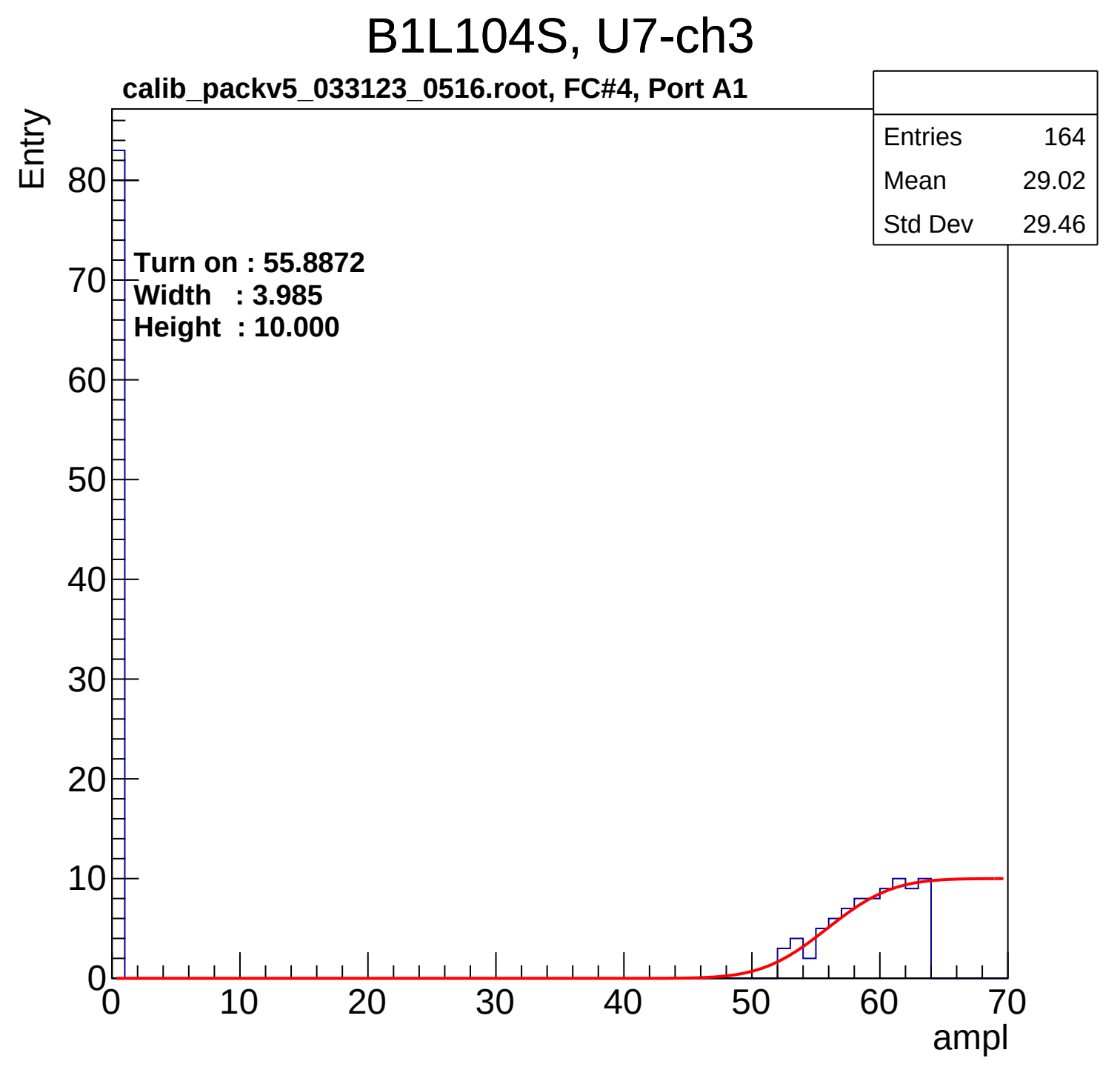

B1L104S, U6-ch27
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 170
Mean 28.71
Std Dev 29.48
Turn on : 56.2911
Width : 3.916
Height : 10.111
Entry
ampl
0
10
20
30
40
50
60
70
80
90

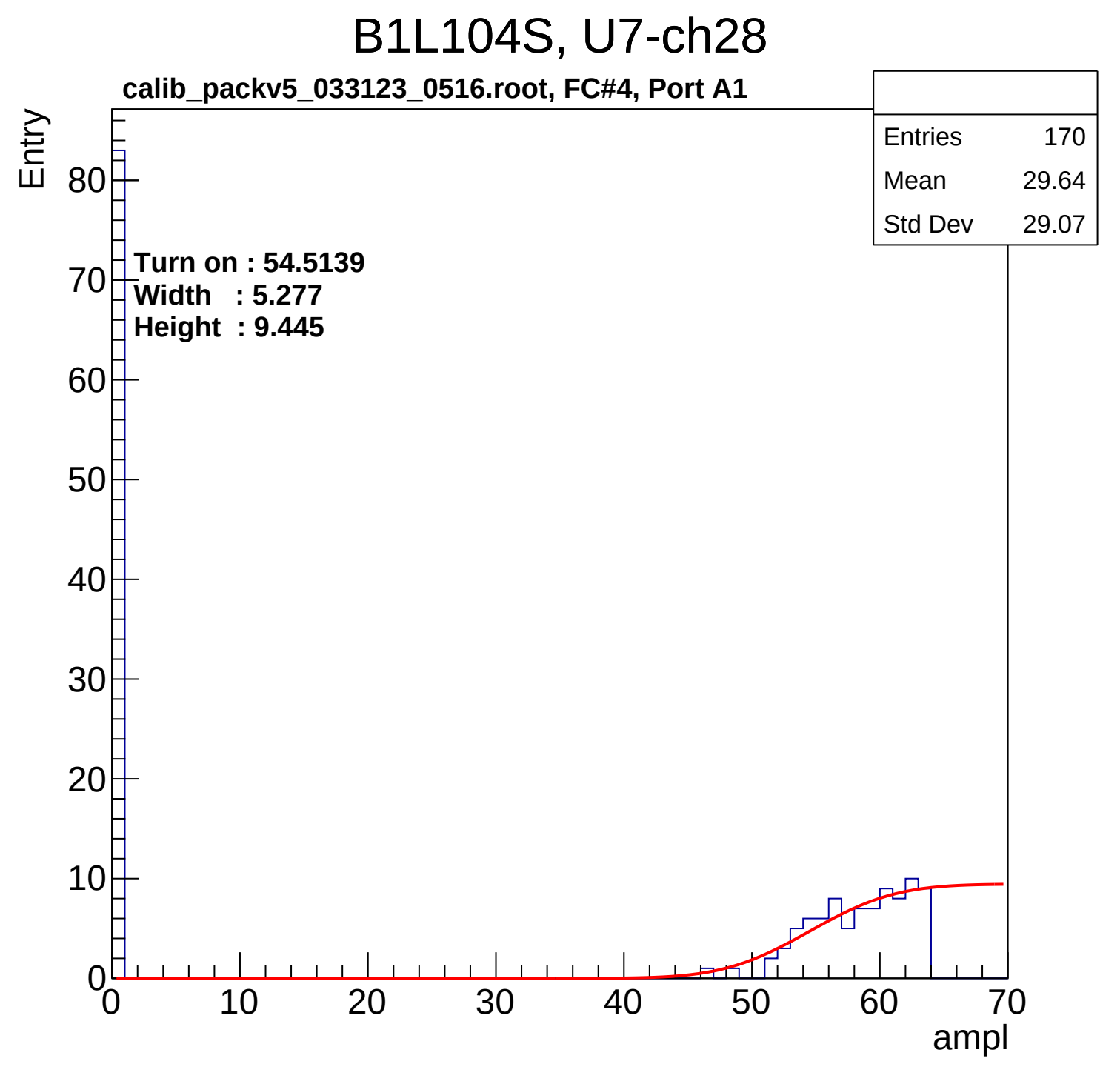

B1L104S, U6-ch41
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 158
Mean 31.96
Std Dev 29.33
Turn on : 55.8906
Width : 3.504
Height : 10.222
Entry
ampl
0
10
20
30
40
50
60
70


B1L104S, U6-ch59
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 165
Mean 28.75
Std Dev 29.38
Turn on : 55.7767
Width : 4.430
Height : 9.889
Entry
ampl
0
10
20
30
40
50
60
70
80


B1L104S, U6-ch78
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 187
Mean 27.2
Std Dev 28.97
Turn on : 54.0023
Width : 4.246
Height : 8.726
Entry
ampl
0
20
40
60
80
100
0
10
20
30
40
50
60
70


B1L104S, U7-ch0
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 298
Mean 20.54
Std Dev 27.36
Turn on : 54.9037
Width : 6.854
Height : 10.667
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L104S, U7-ch3
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 164
Mean 29.02
Std Dev 29.46
Turn on : 55.8872
Width : 3.985
Height : 10.000
Entry
0
10
20
30
40
50
60
70
80
ampl


B1L104S, U7-ch28
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 170
Mean 29.64
Std Dev 29.07
Turn on : 54.5139
Width : 5.277
Height : 9.445
Entry
ampl
0
10
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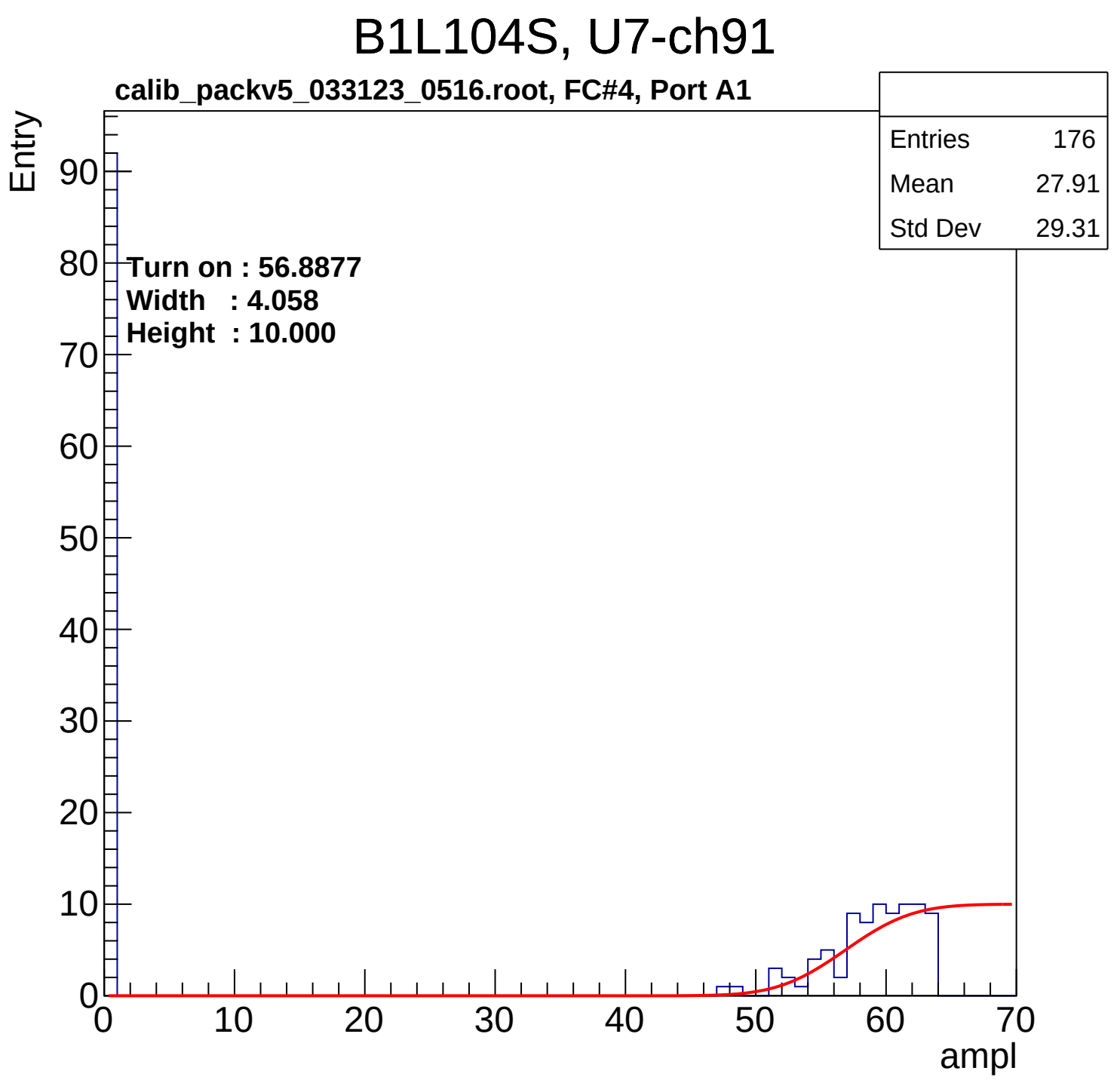
40
50
60
70
80


B1L104S, U7-ch91
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 176
Mean 27.91
Std Dev 29.31
Turn on : 56.8877
Width : 4.058
Height : 10.000
Entry
ampl
0
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60
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80
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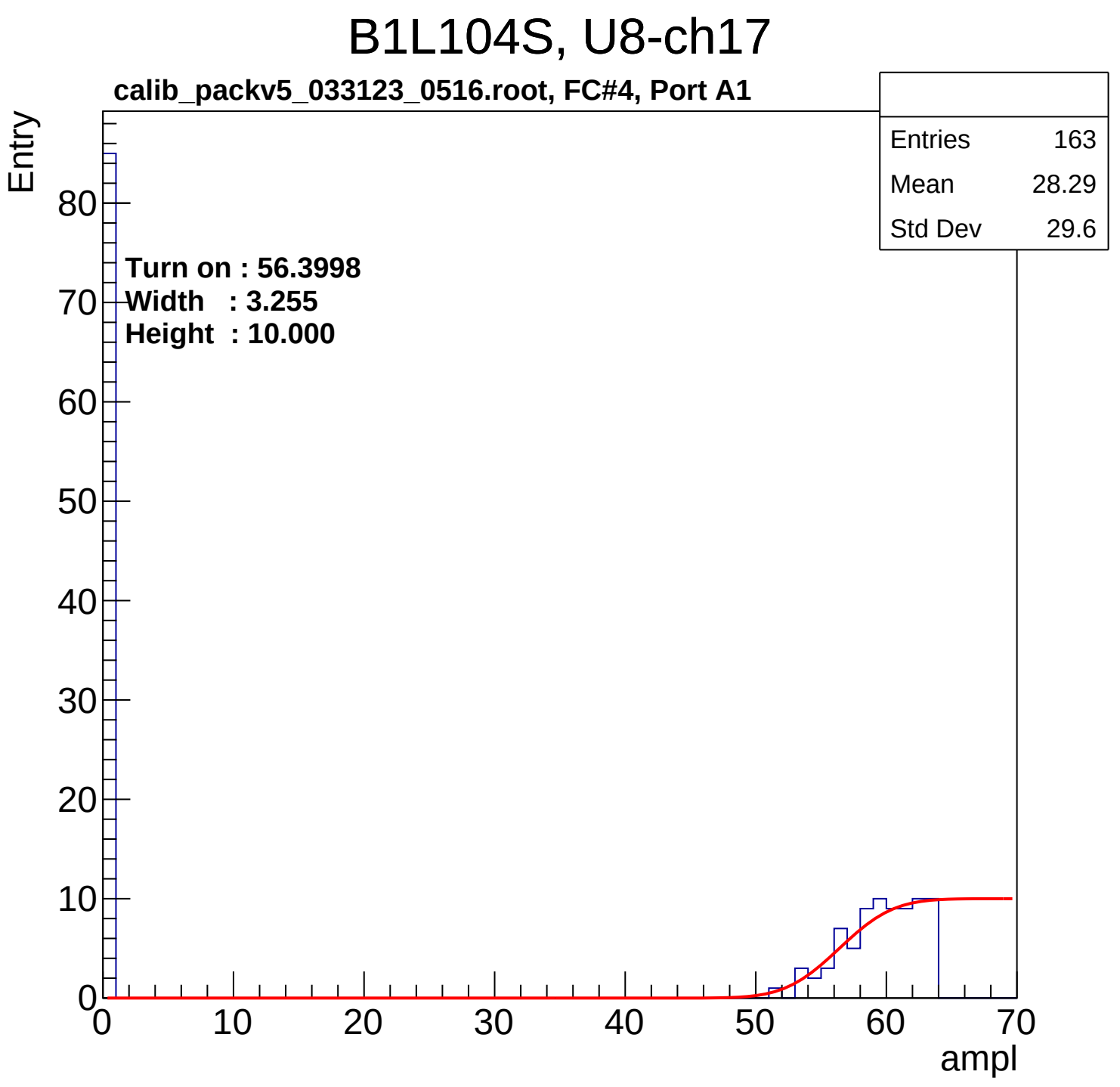
B1L104S, U8-ch17
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 163
Mean 28.29
Std Dev 29.6
Turn on : 56.3998
Width : 3.255
Height : 10.000
Entry
ampl
0
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50
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70
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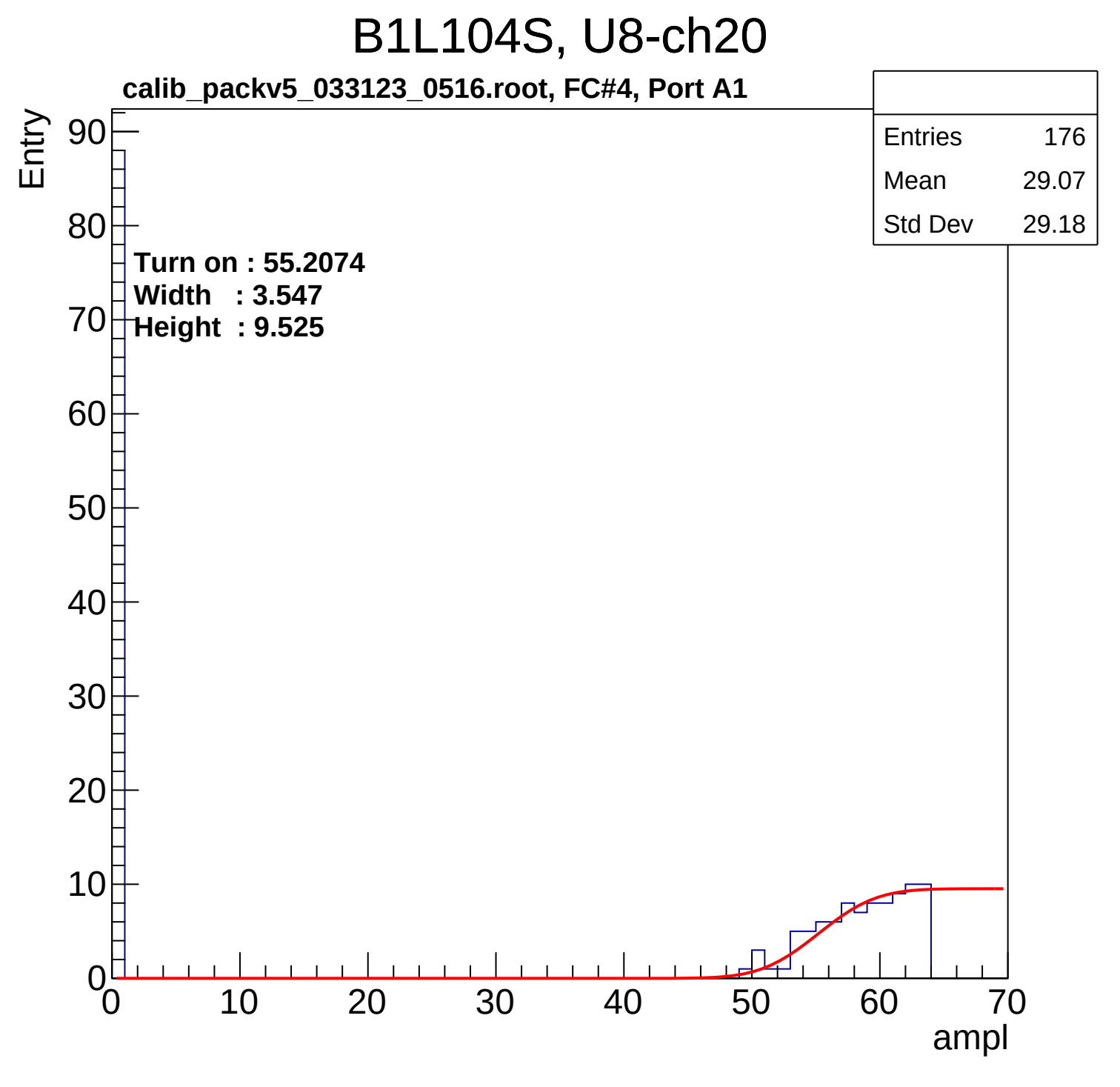
B1L104S, U8-ch20
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 176
Mean 29.07
Std Dev 29.18
Turn on : 55.2074
Width : 3.547
Height : 9.525
Entry
ampl
0
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40
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60
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80
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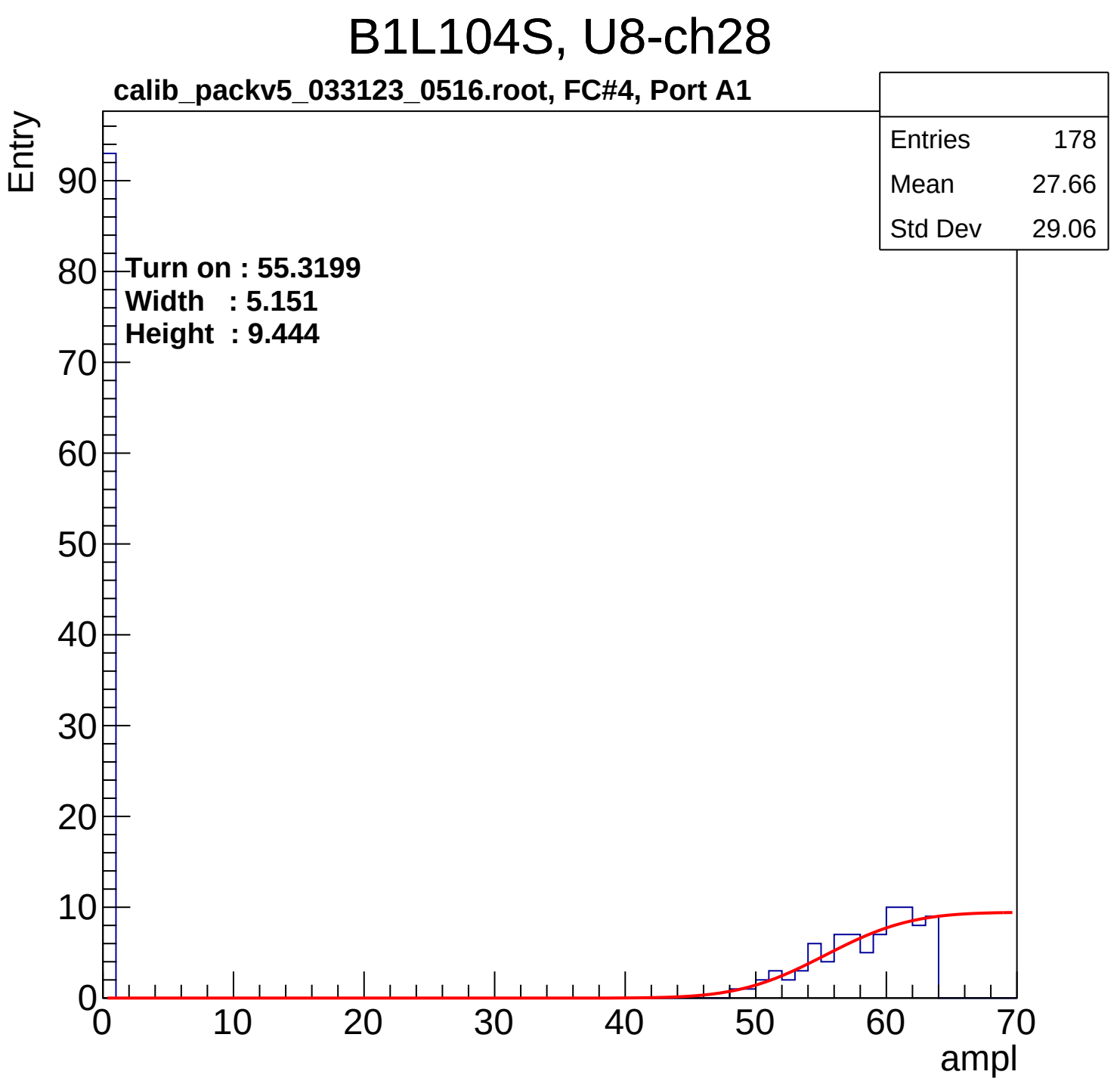
B1L104S, U8-ch28
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 178
Mean 27.66
Std Dev 29.06
Turn on : 55.3199
Width : 5.151
Height : 9.444
Entry
ampl
0
10
20
30
40
50
60
70
80
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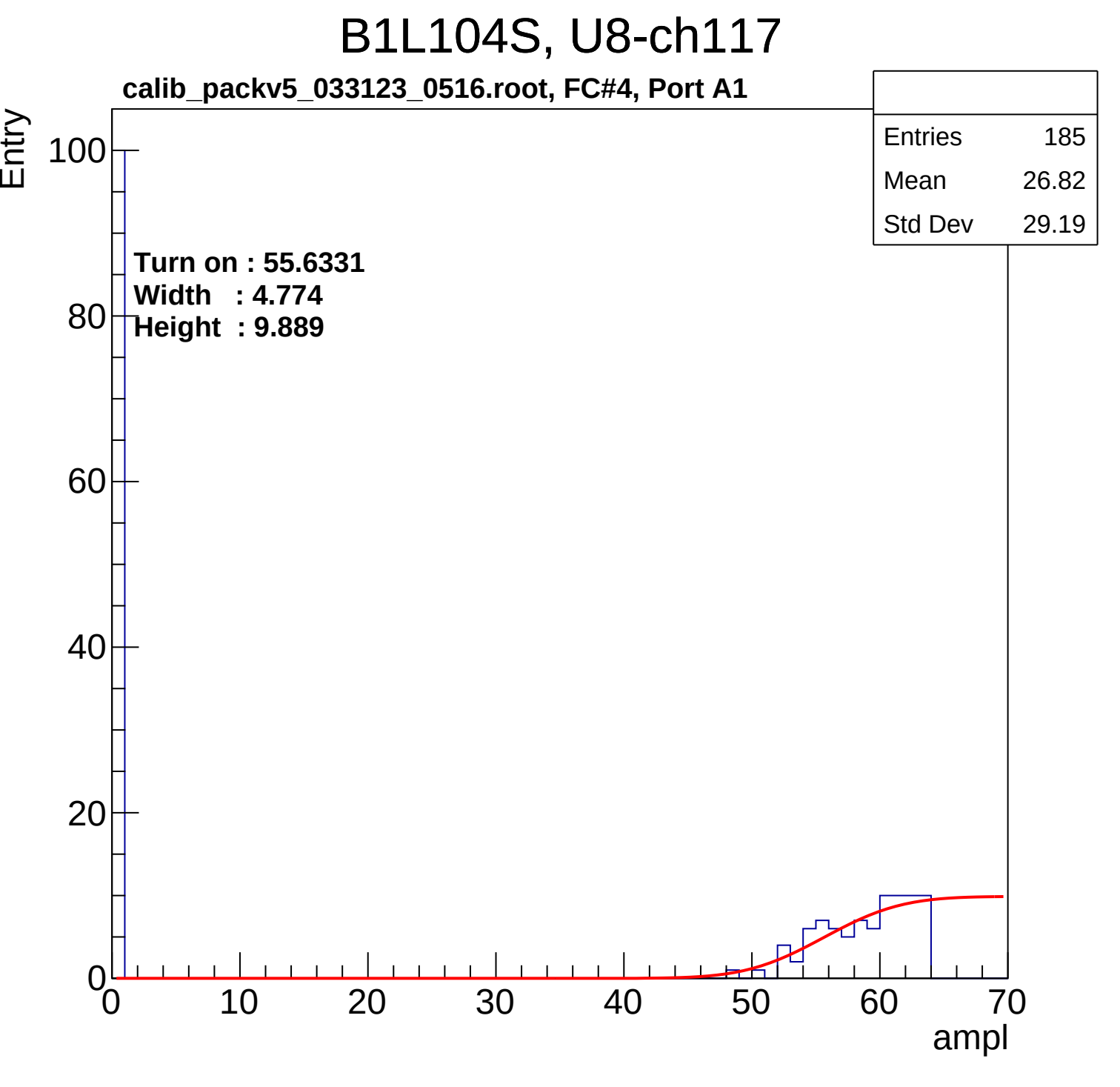
B1L104S, U8-ch117
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 185
Mean 26.82
Std Dev 29.19
Turn on : 55.6331
Width : 4.774
Height : 9.889
Entry
ampl
0
20
40
60
80
100
0
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20
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40
50
60
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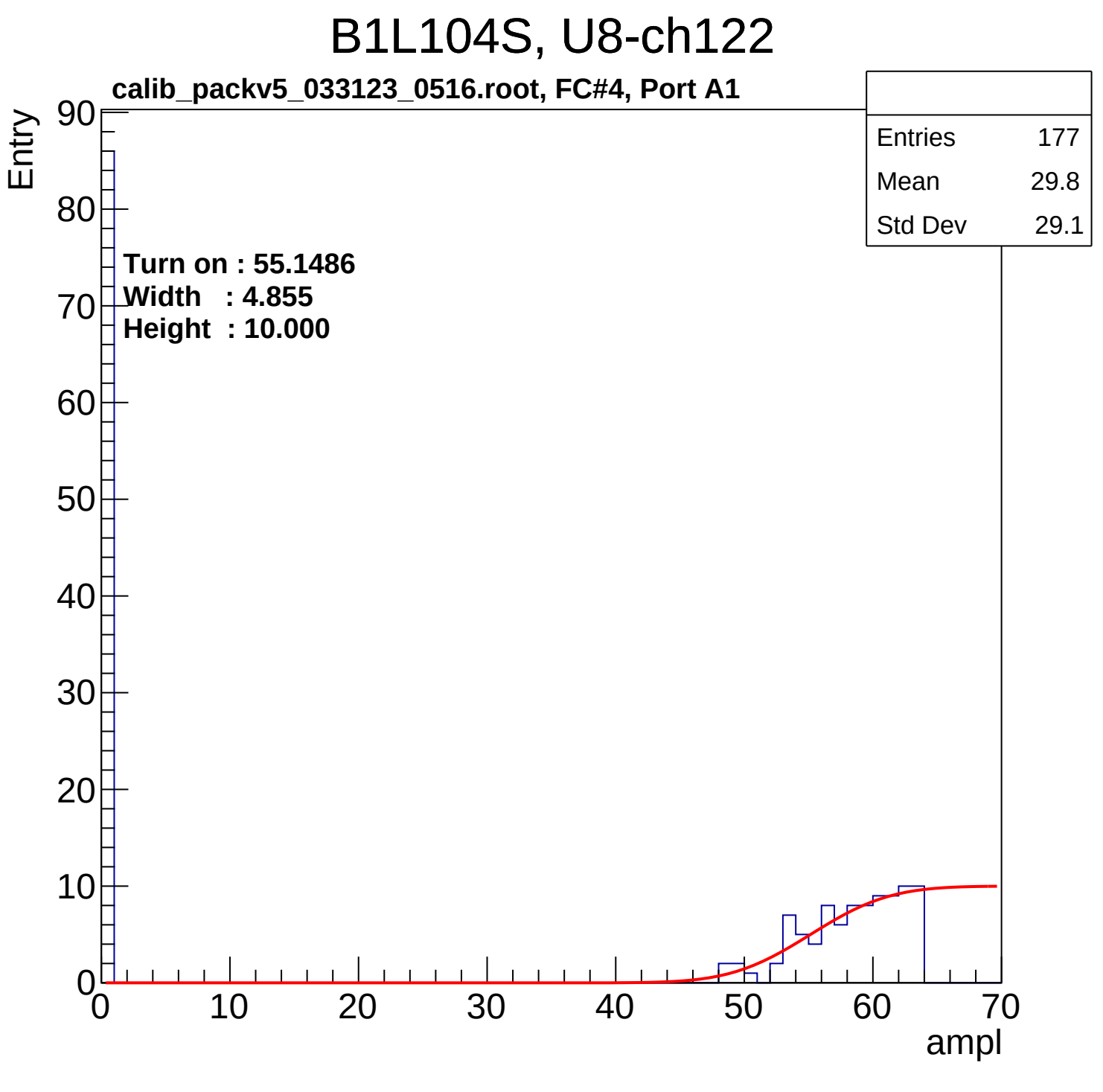
B1L104S, U8-ch122
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 177
Mean 29.8
Std Dev 29.1
Turn on : 55.1486
Width : 4.855
Height : 10.000
Entry
ampl
0
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60
70
80
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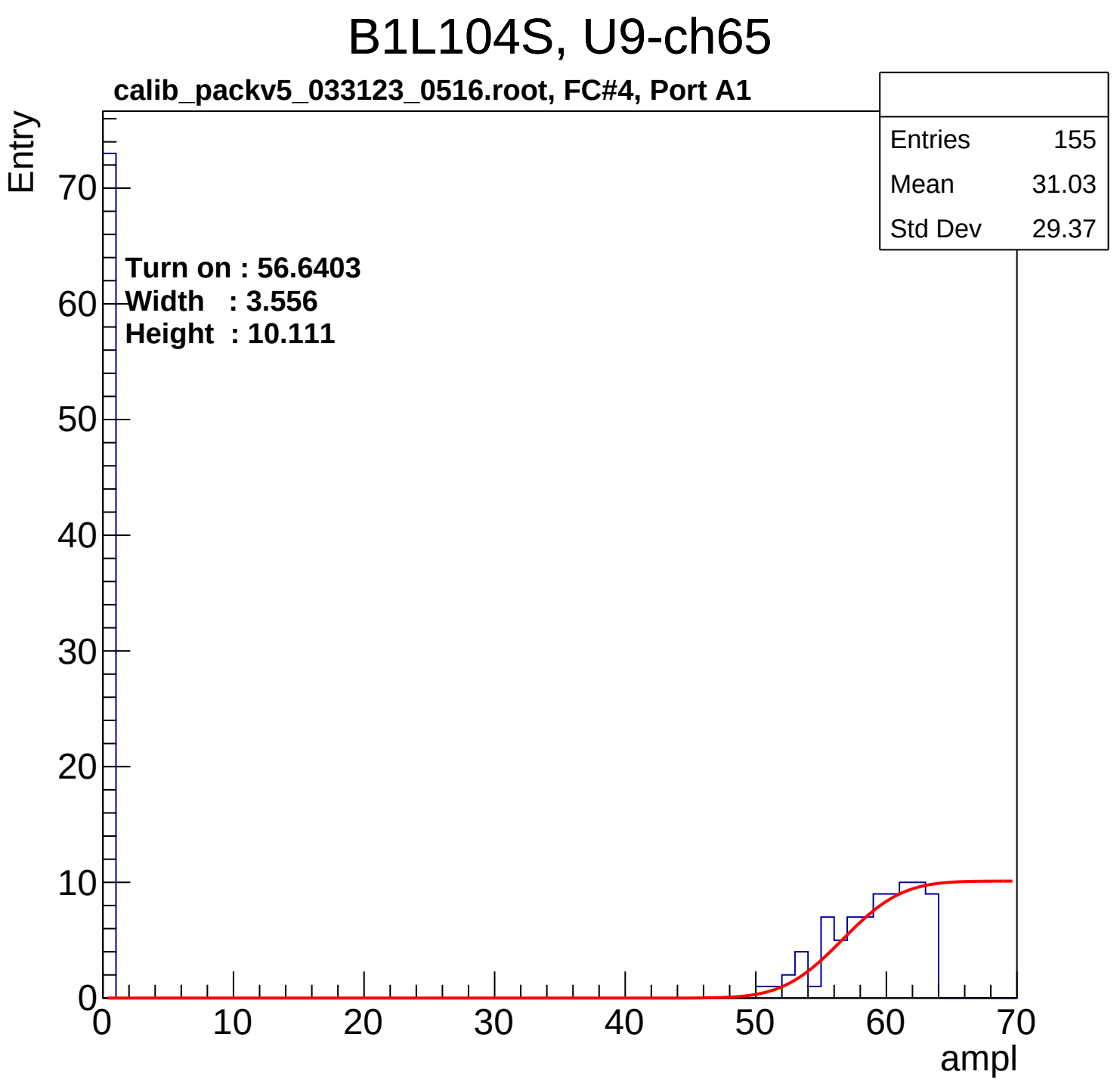
B1L104S, U9-ch65
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 155
Mean 31.03
Std Dev 29.37
Turn on : 56.6403
Width : 3.556
Height : 10.111
Entry
ampl
0
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40
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60
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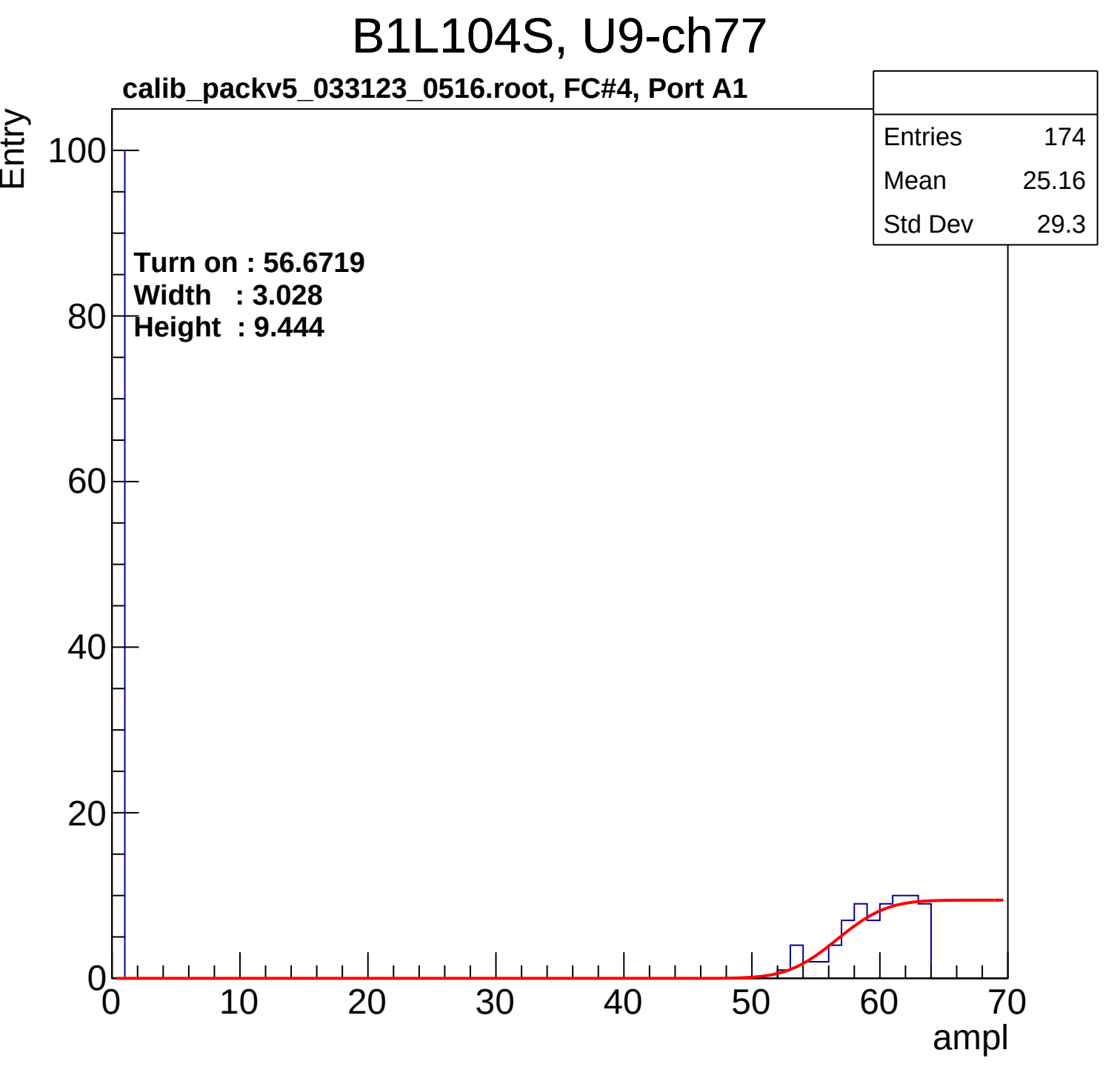
B1L104S, U9-ch77
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 174
Mean 25.16
Std Dev 29.3
Turn on : 56.6719
Width : 3.028
Height : 9.444
Entry
ampl
0
20
40
60
80
100
0
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20
30
40
50
60
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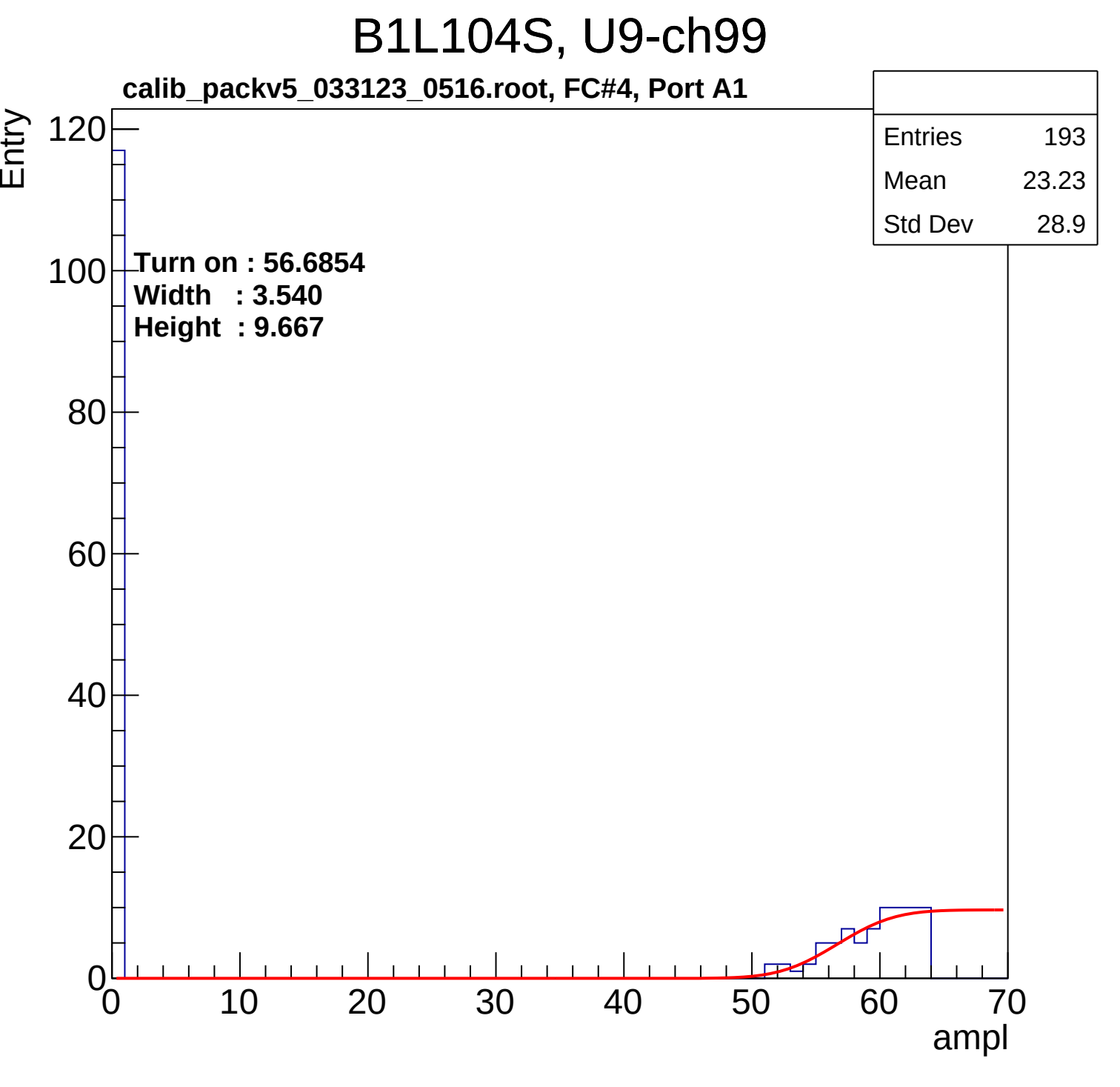
B1L104S, U9-ch99
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 193
Mean 23.23
Std Dev 28.9
Turn on : 56.6854
Width : 3.540
Height : 9.667
Entry
ampl
0
20
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60
80
100
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0
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20
30
40
50
60
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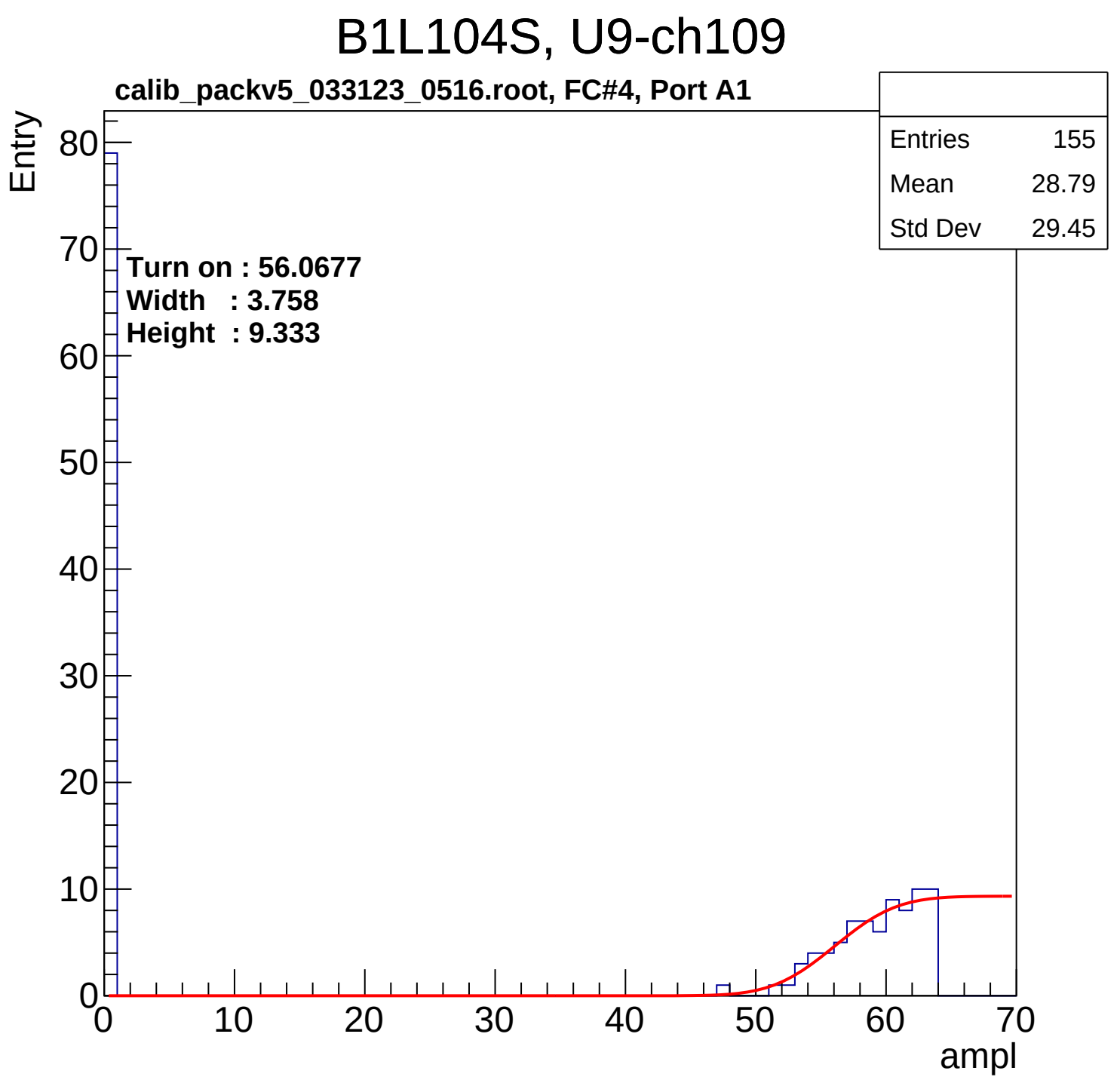
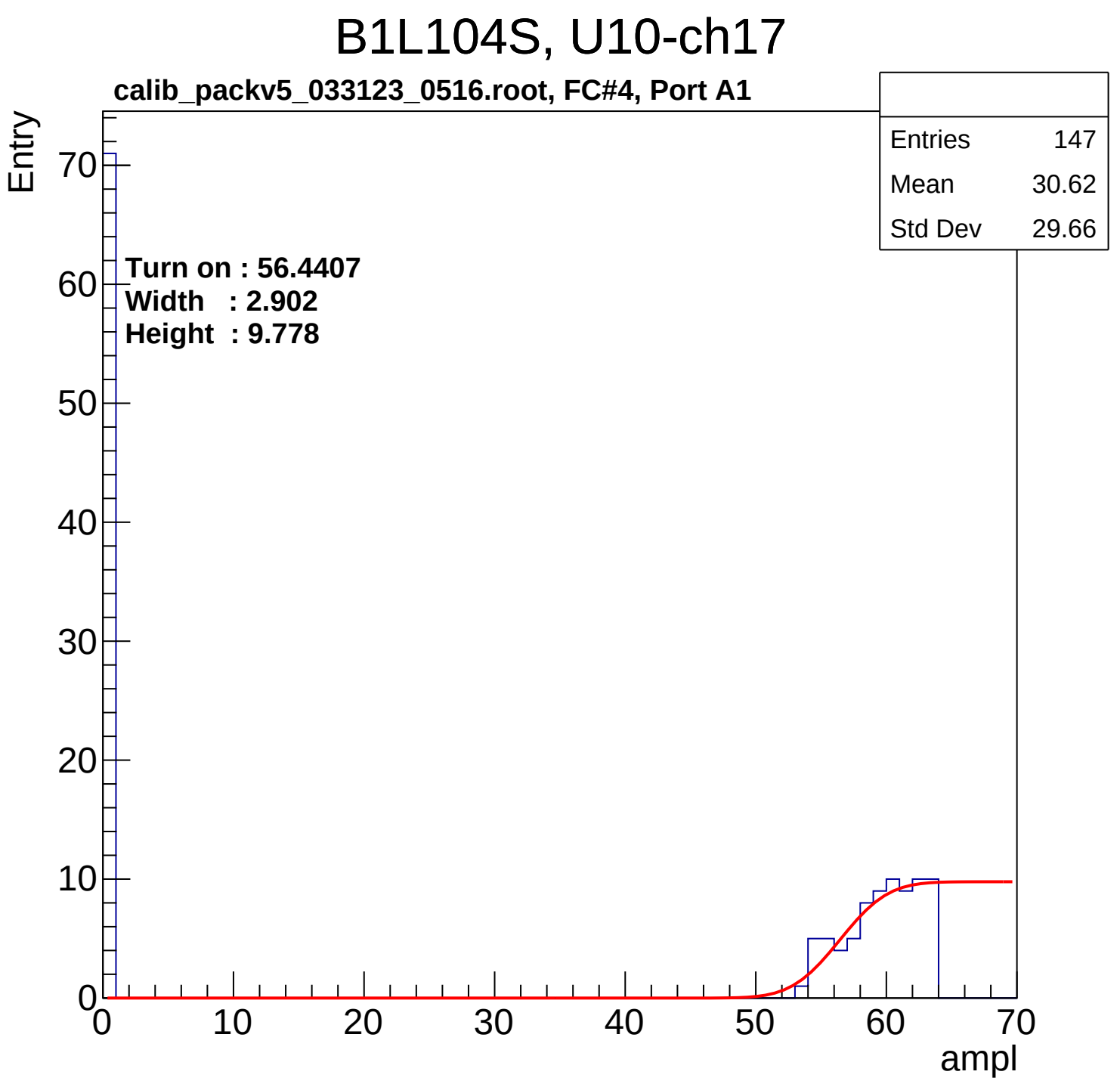

B1L104S, U9-ch109
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 155
Mean 28.79
Std Dev 29.45
Turn on : 56.0677
Width : 3.758
Height : 9.333
Entry
ampl
0
10
20
30
40
50
60
70
80


B1L104S, U10-ch17
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 147
Mean 30.62
Std Dev 29.66
Turn on : 56.4407
Width : 2.902
Height : 9.778
Entry
ampl
0
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40
50
60
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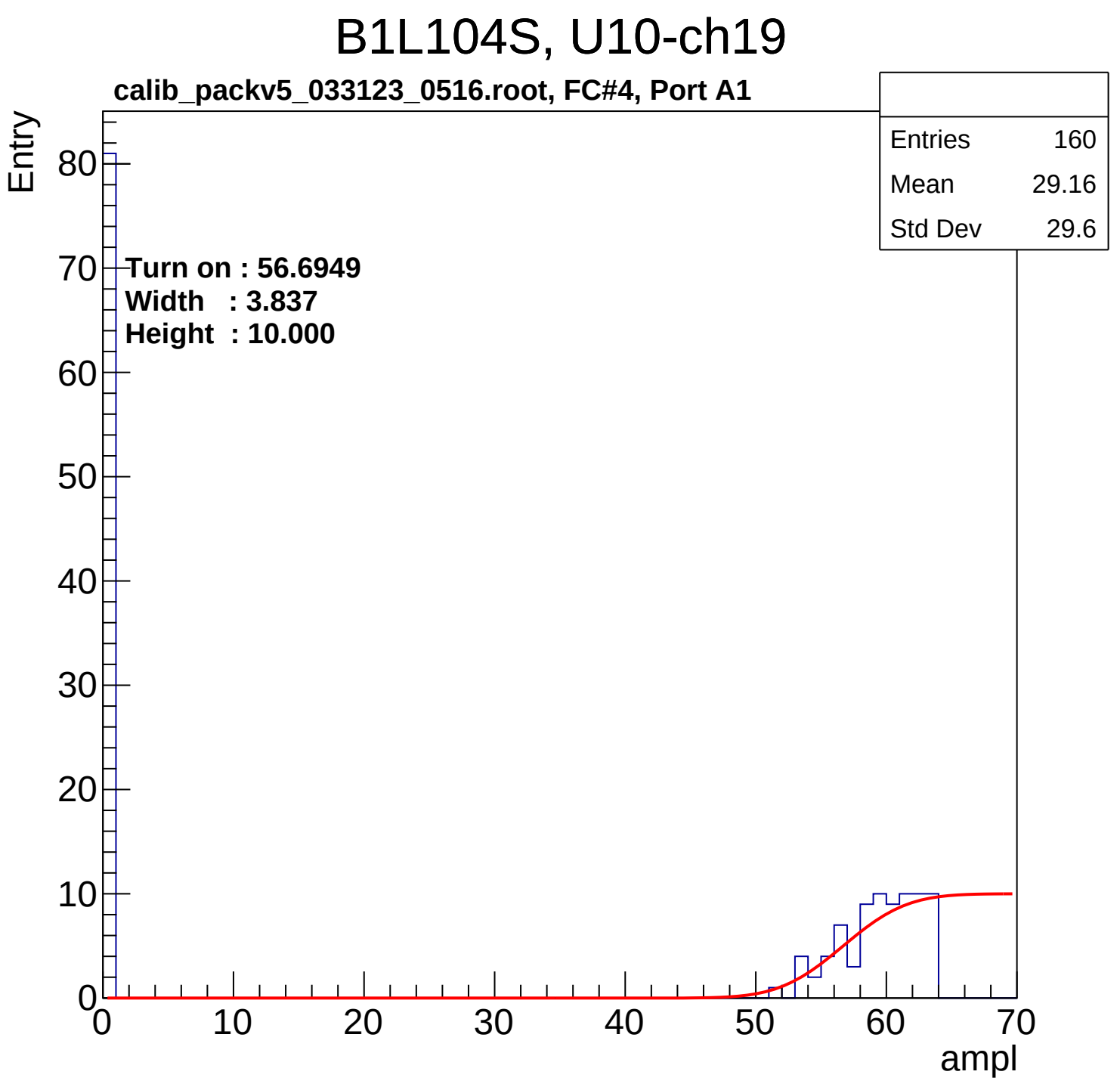
B1L104S, U10-ch19
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 160
Mean 29.16
Std Dev 29.6
Turn on : 56.6949
Width : 3.837
Height : 10.000
Entry
ampl
0
10
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50
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70
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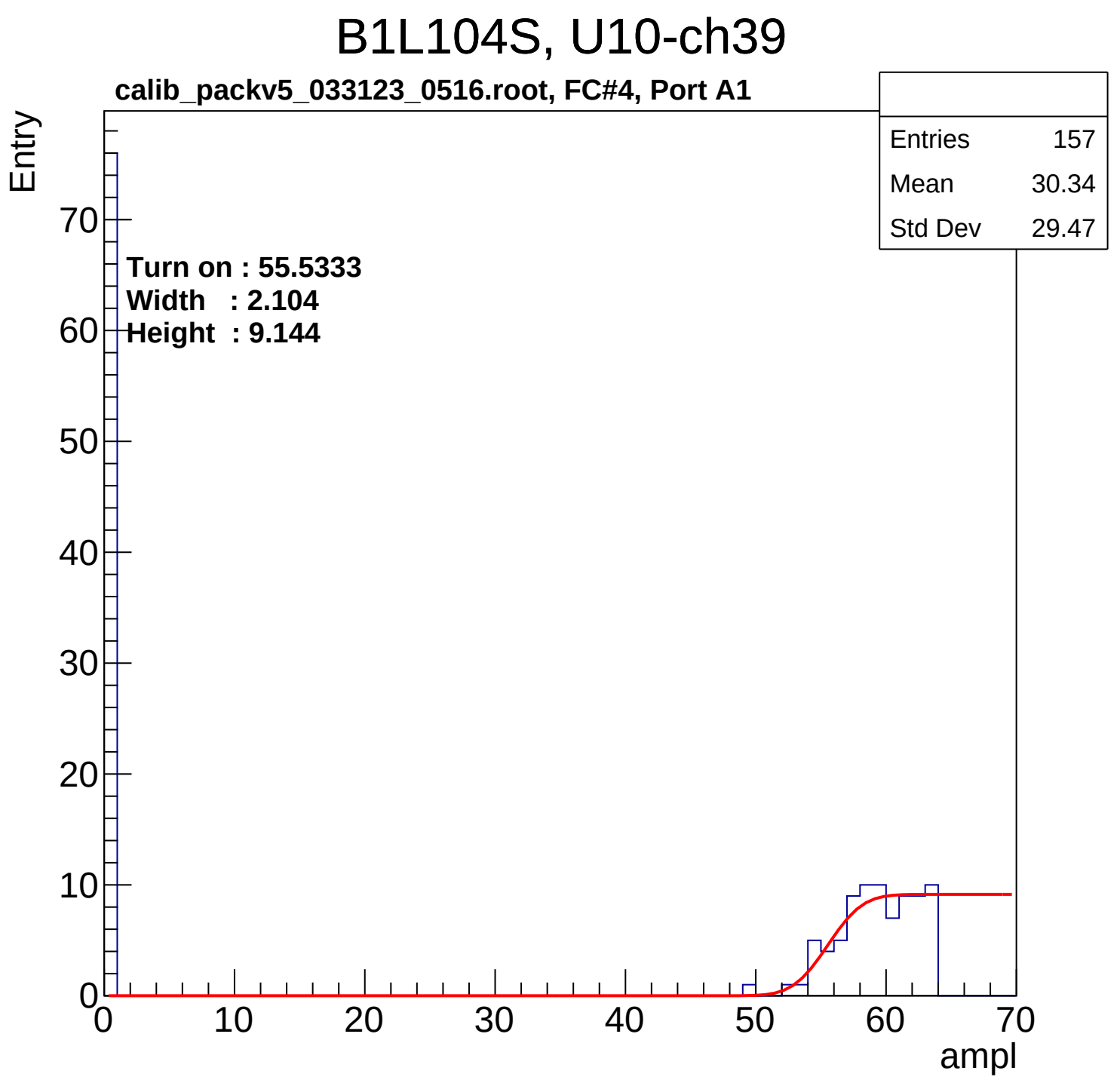
B1L104S, U10-ch39
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 157
Mean 30.34
Std Dev 29.47
Turn on : 55.5333
Width : 2.104
Height : 9.144
Entry
ampl
0
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40
50
60
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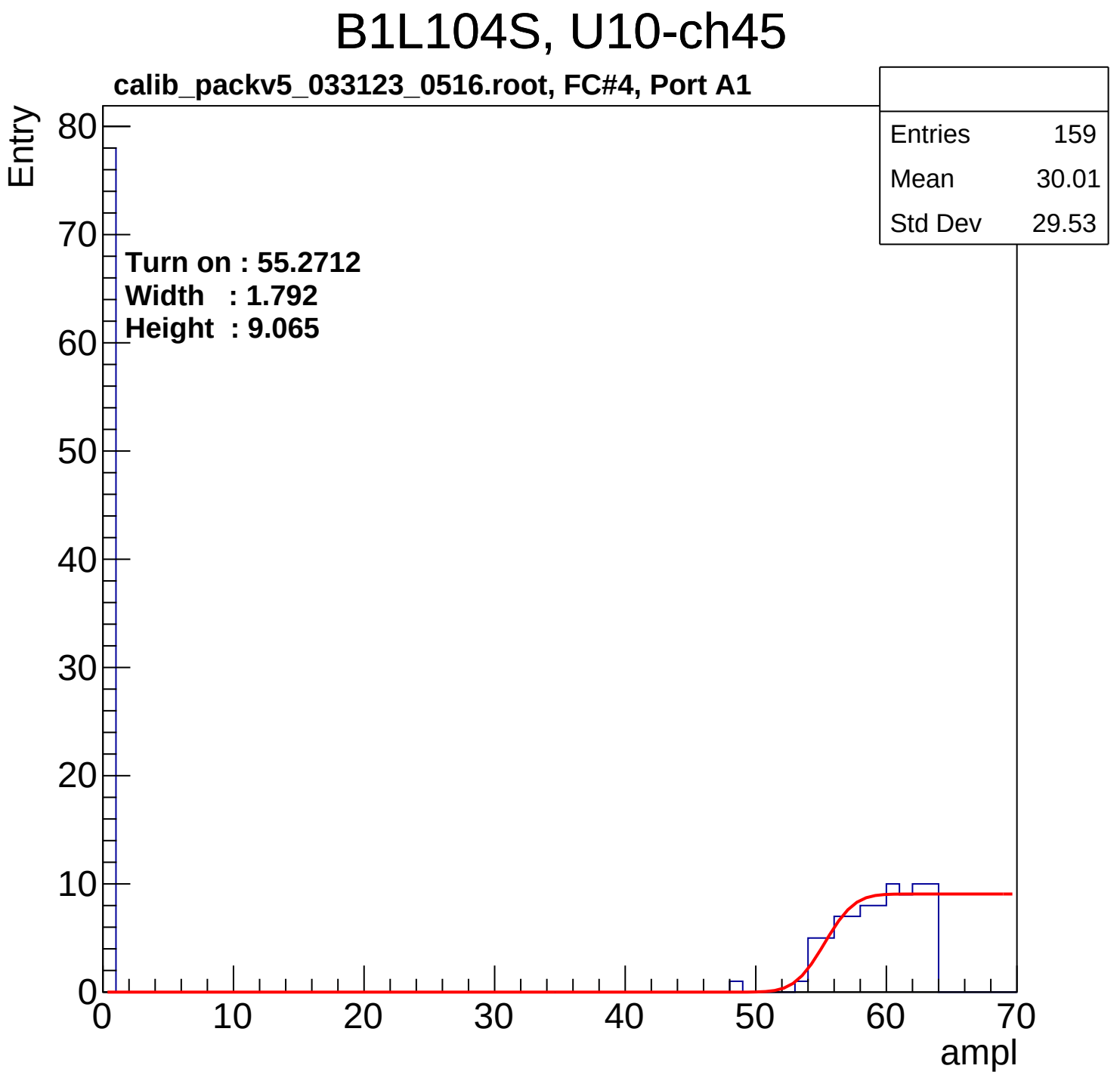
B1L104S, U10-ch45
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 159
Mean 30.01
Std Dev 29.53
Turn on : 55.2712
Width : 1.792
Height : 9.065
Entry
ampl
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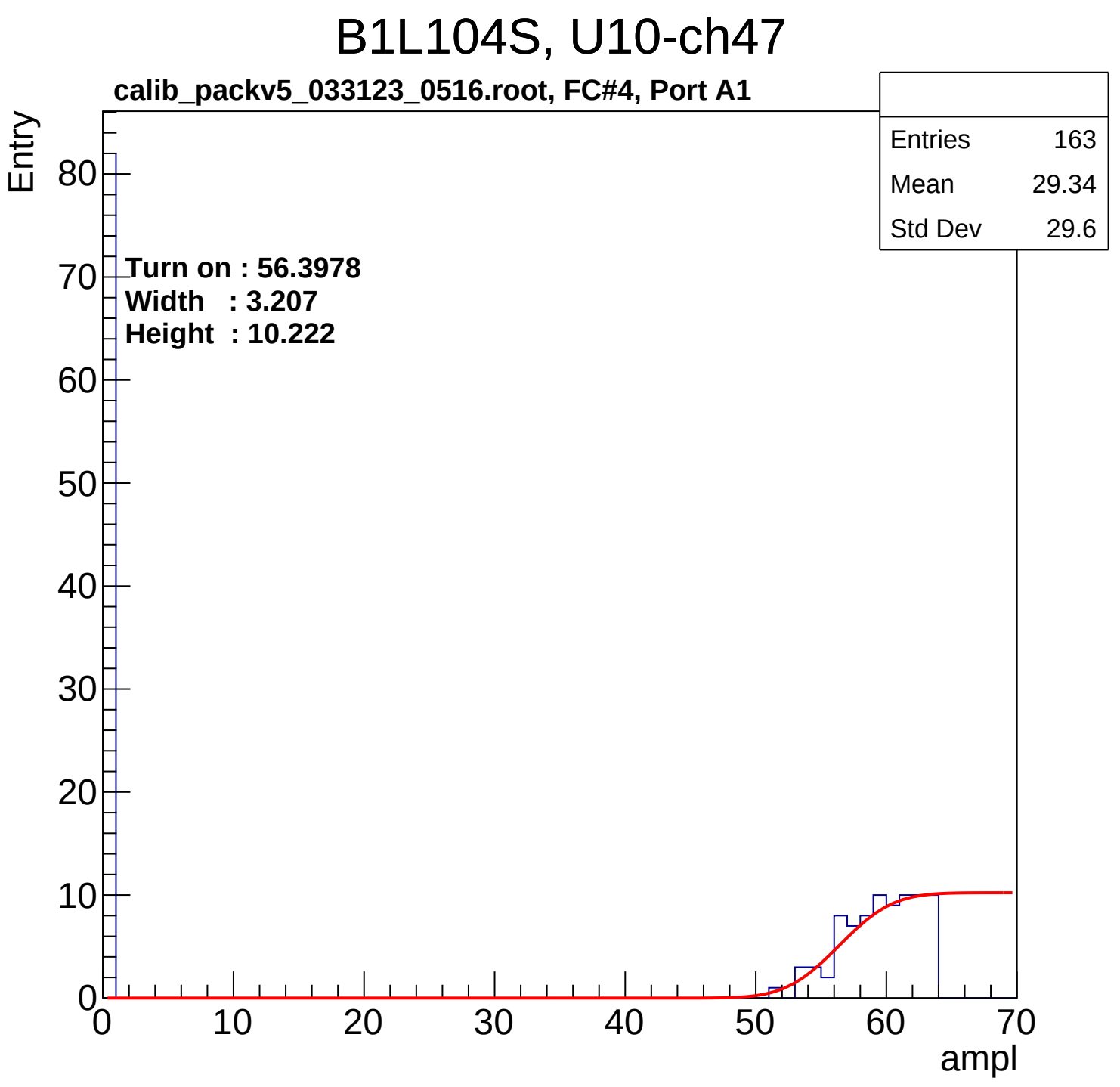
B1L104S, U10-ch47
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 163
Mean 29.34
Std Dev 29.6
Turn on : 56.3978
Width : 3.207
Height : 10.222
Entry
ampl
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10
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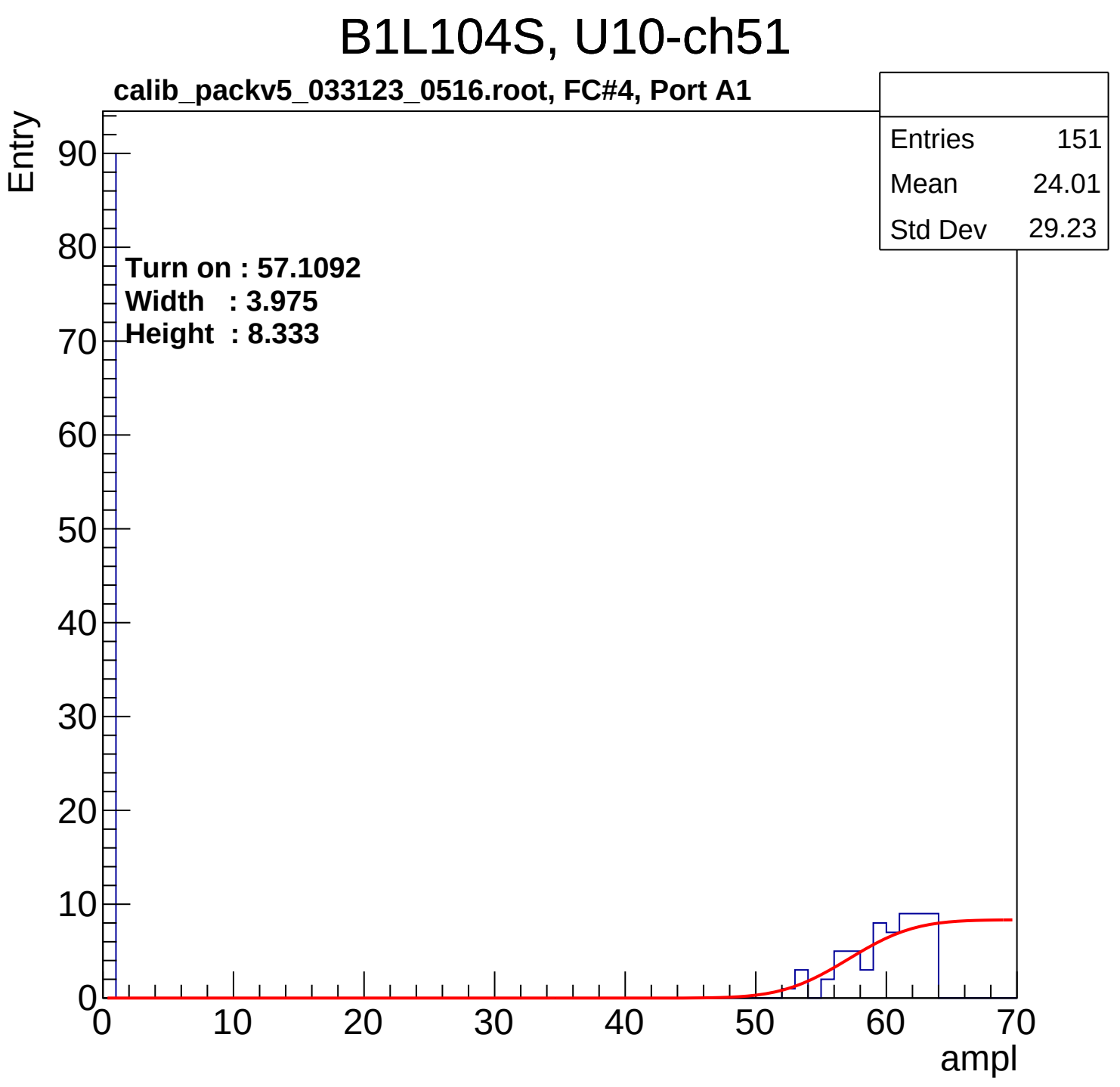
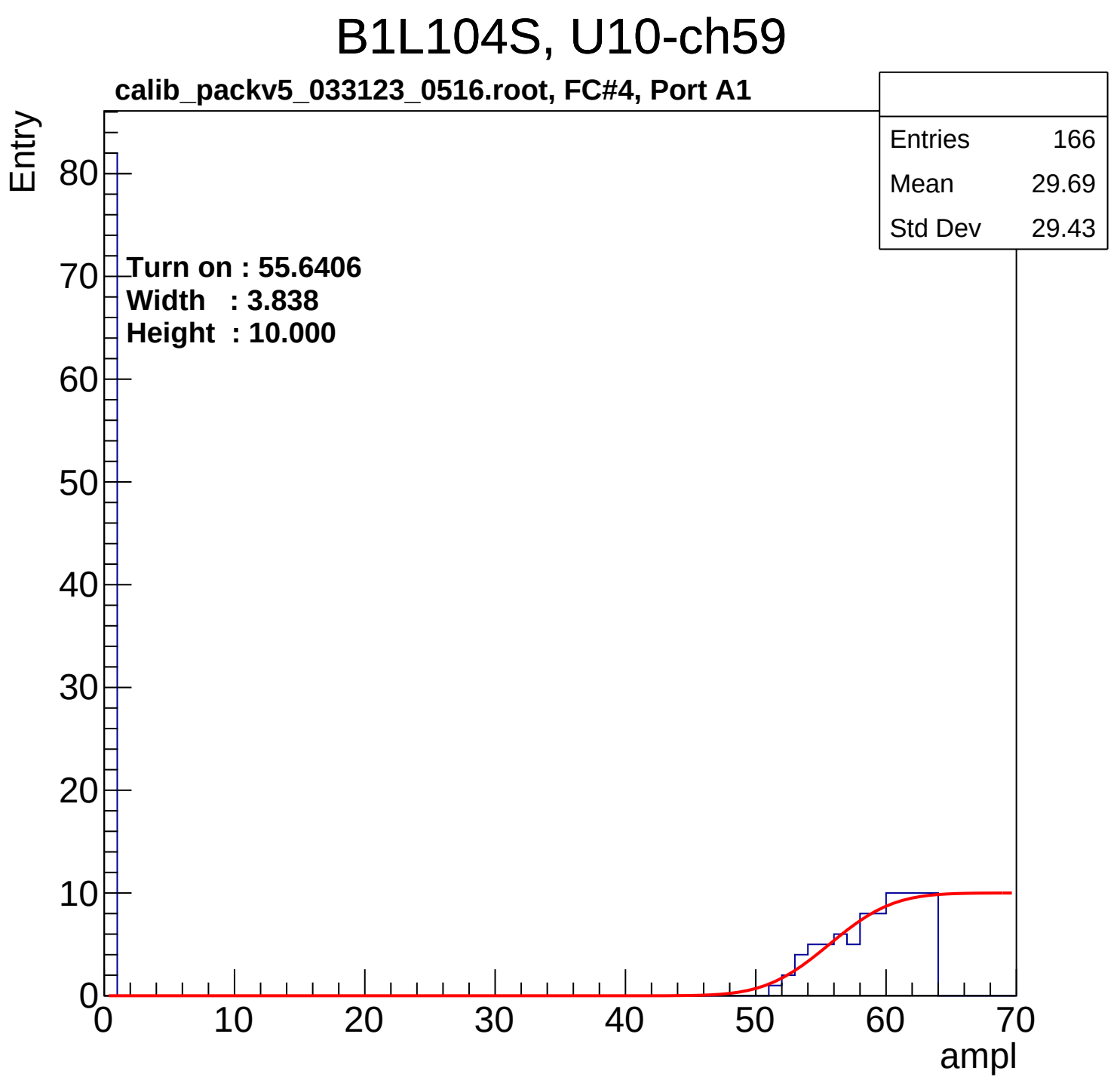
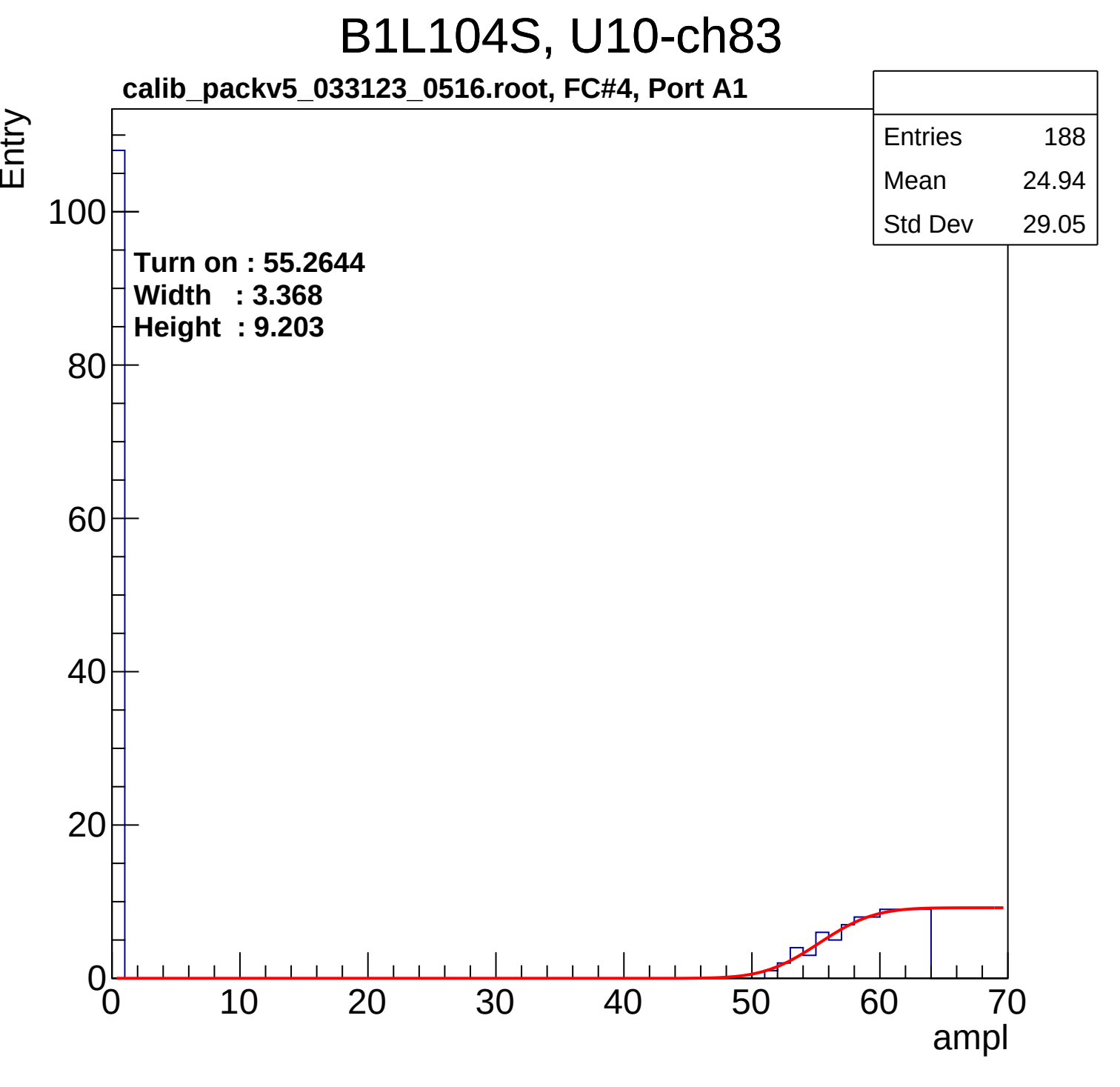

B1L104S, U10-ch51
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 151
Mean 24.01
Std Dev 29.23
Turn on : 57.1092
Width : 3.975
Height : 8.333
Entry
ampl
0
10
20
30
40
50
60
70
80
90


B1L104S, U10-ch59
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 166
Mean 29.69
Std Dev 29.43
Turn on : 55.6406
Width : 3.838
Height : 10.000
Entry
ampl
0
10
20
30
40
50
60
70
80


B1L104S, U10-ch83
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 188
Mean 24.94
Std Dev 29.05
Turn on : 55.2644
Width : 3.368
Height : 9.203
Entry
ampl
0
20
40
60
80
100
0
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20
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40
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60
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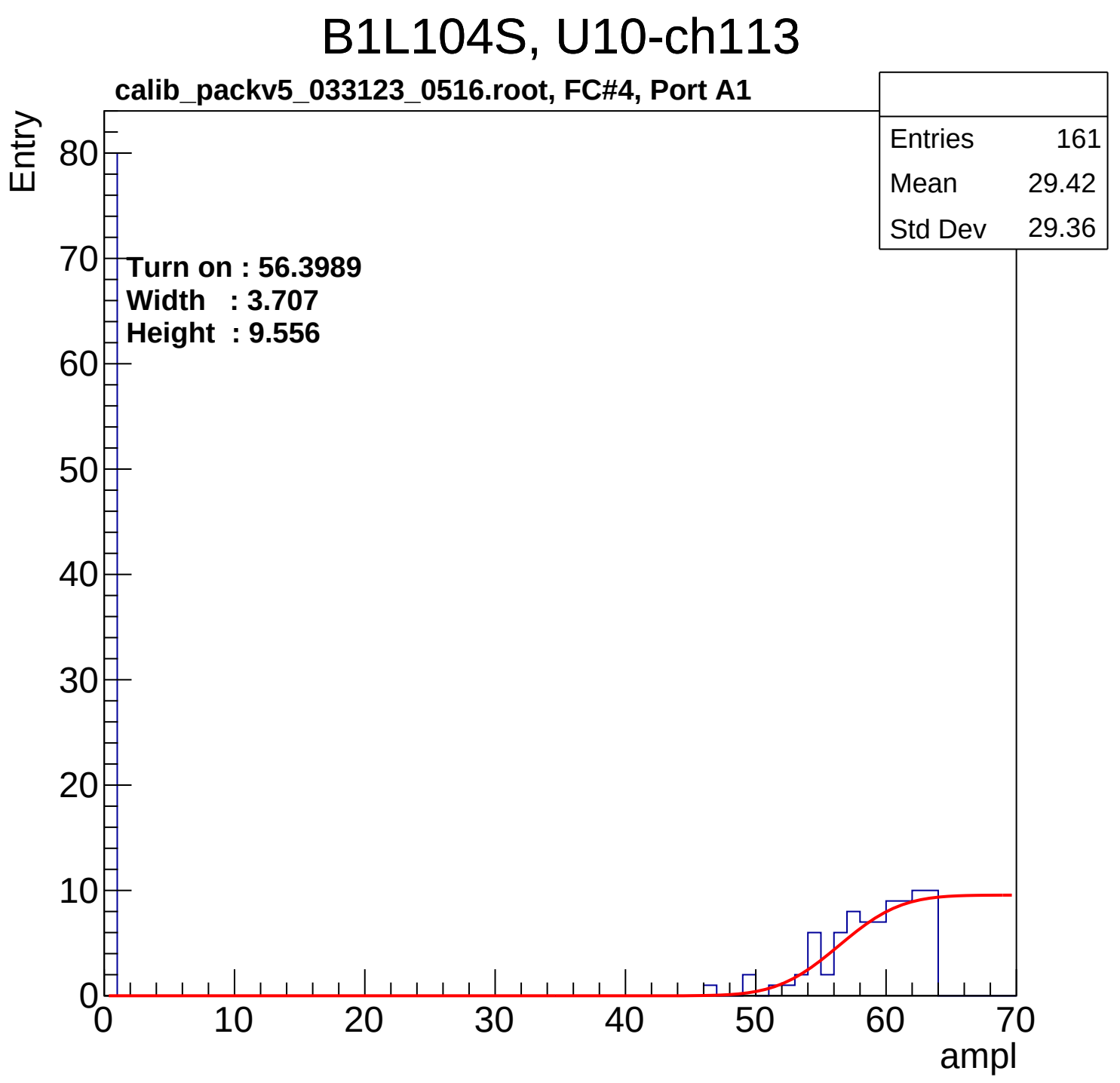
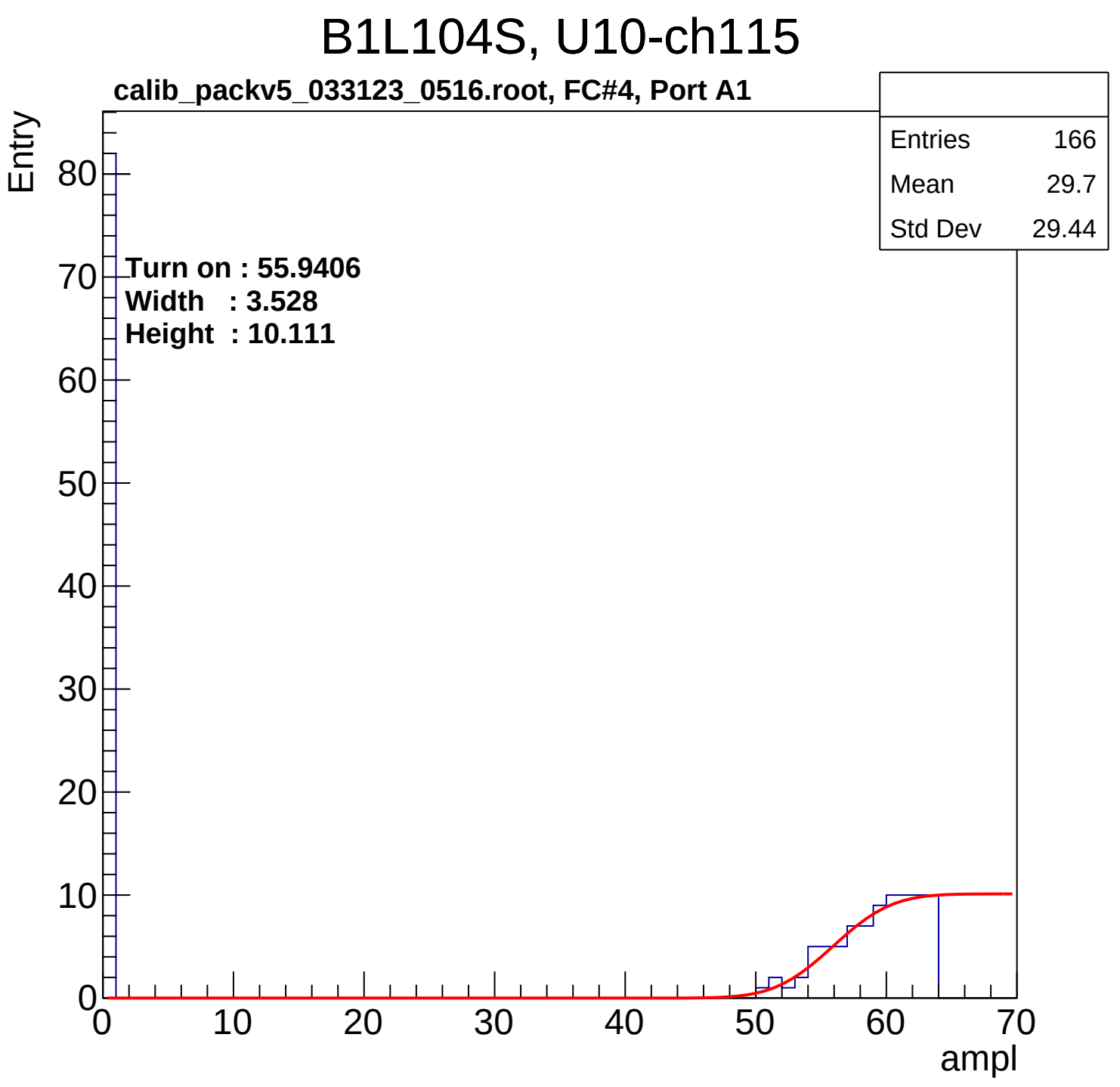
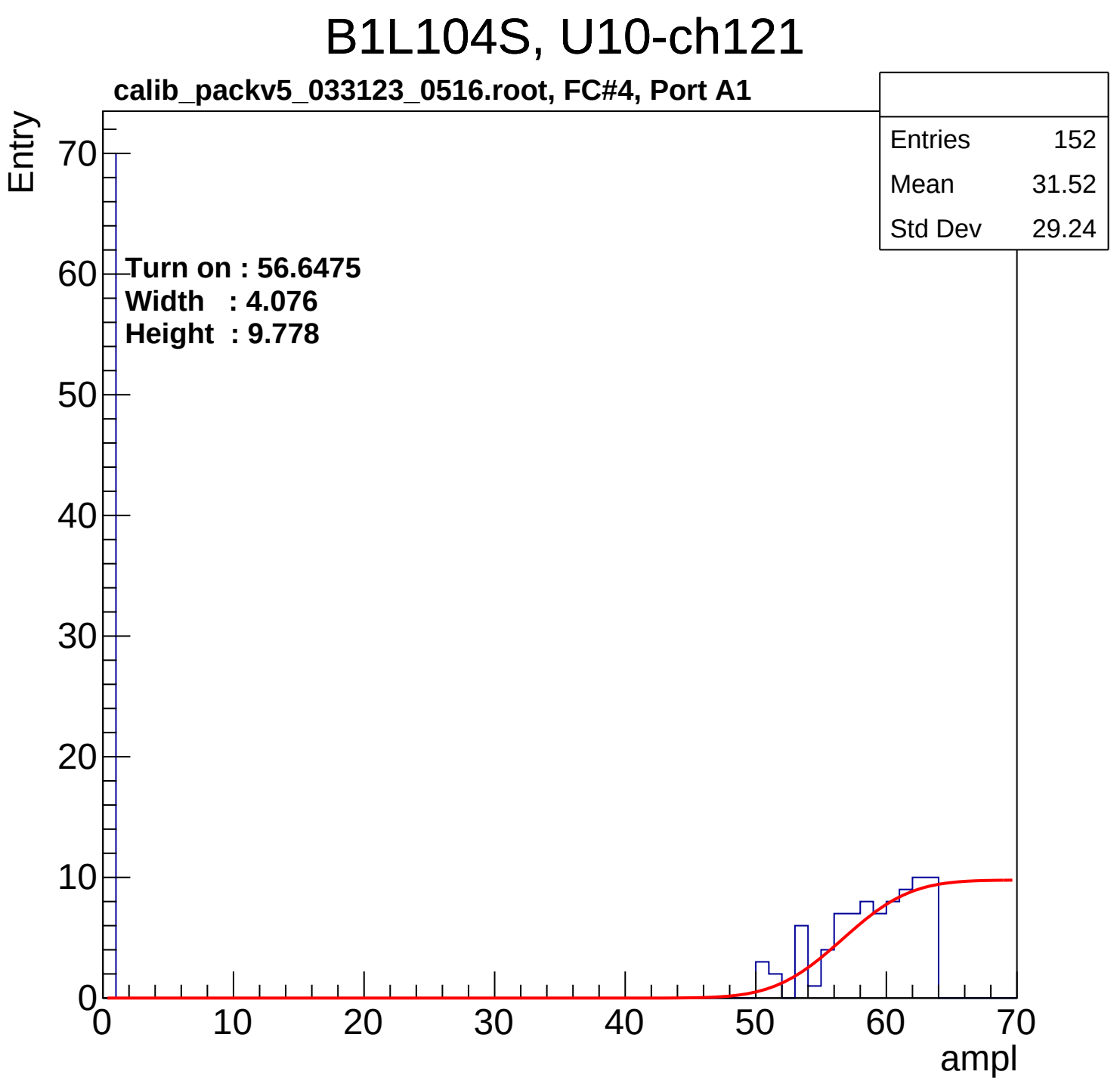
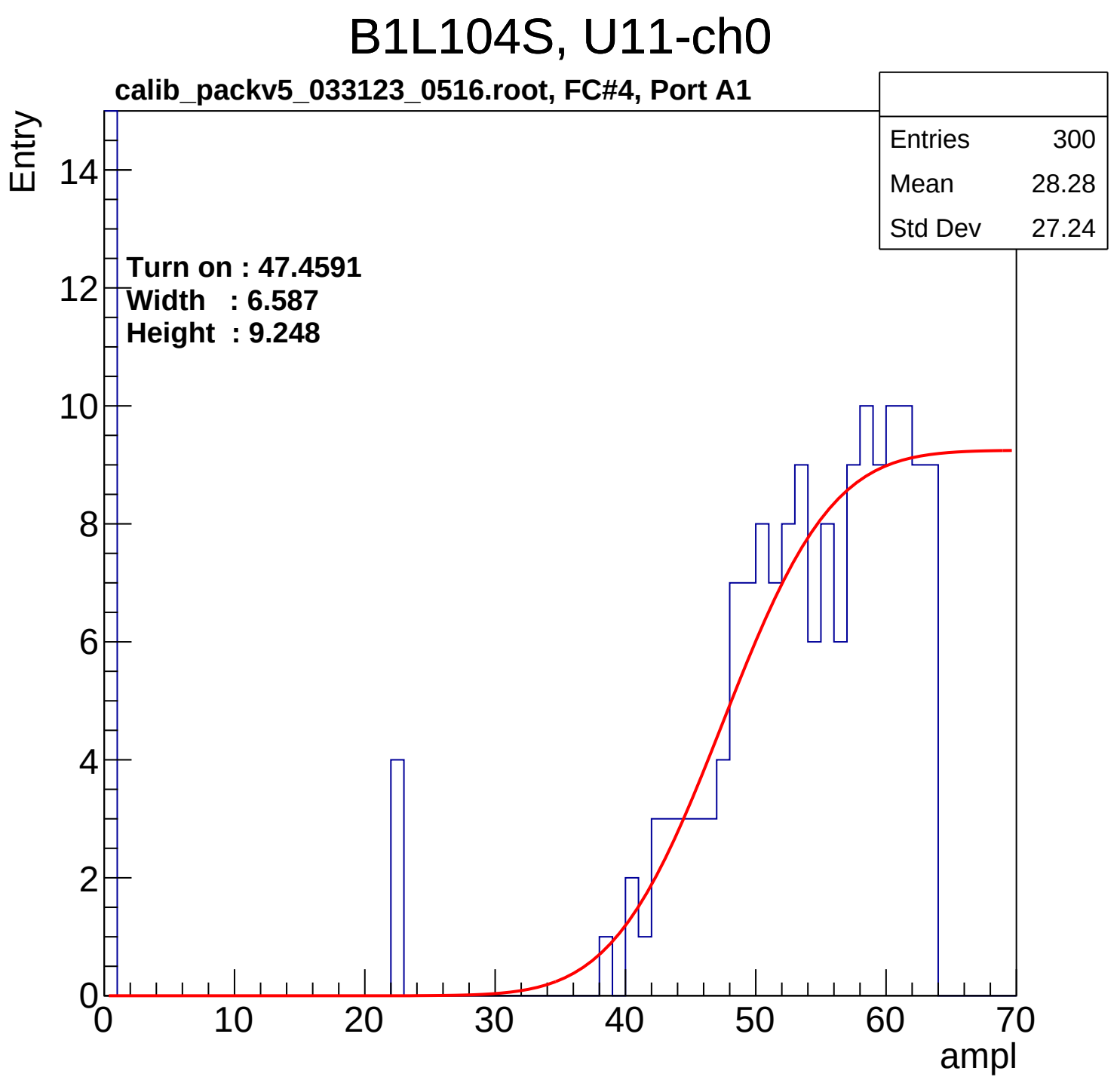
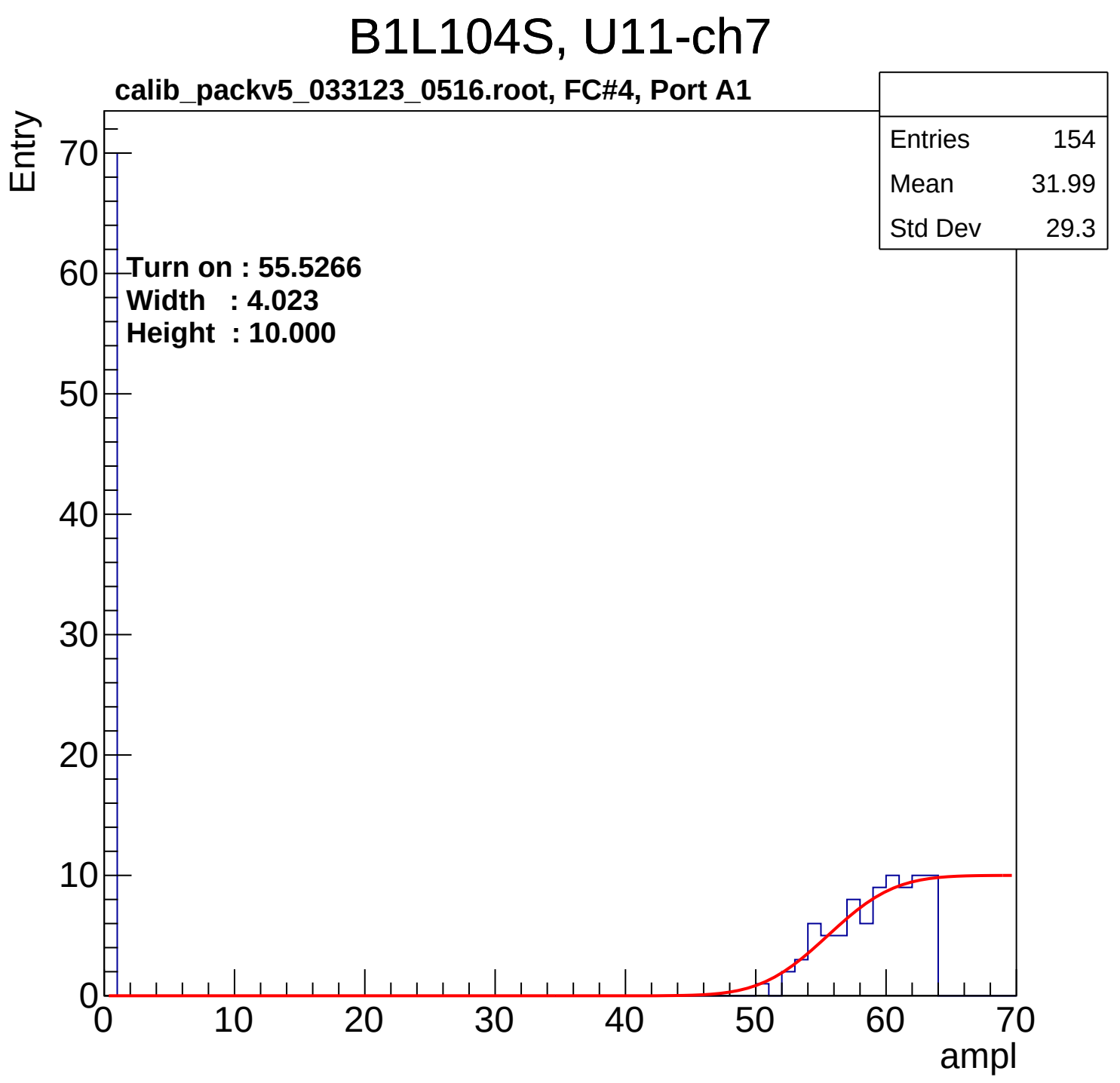
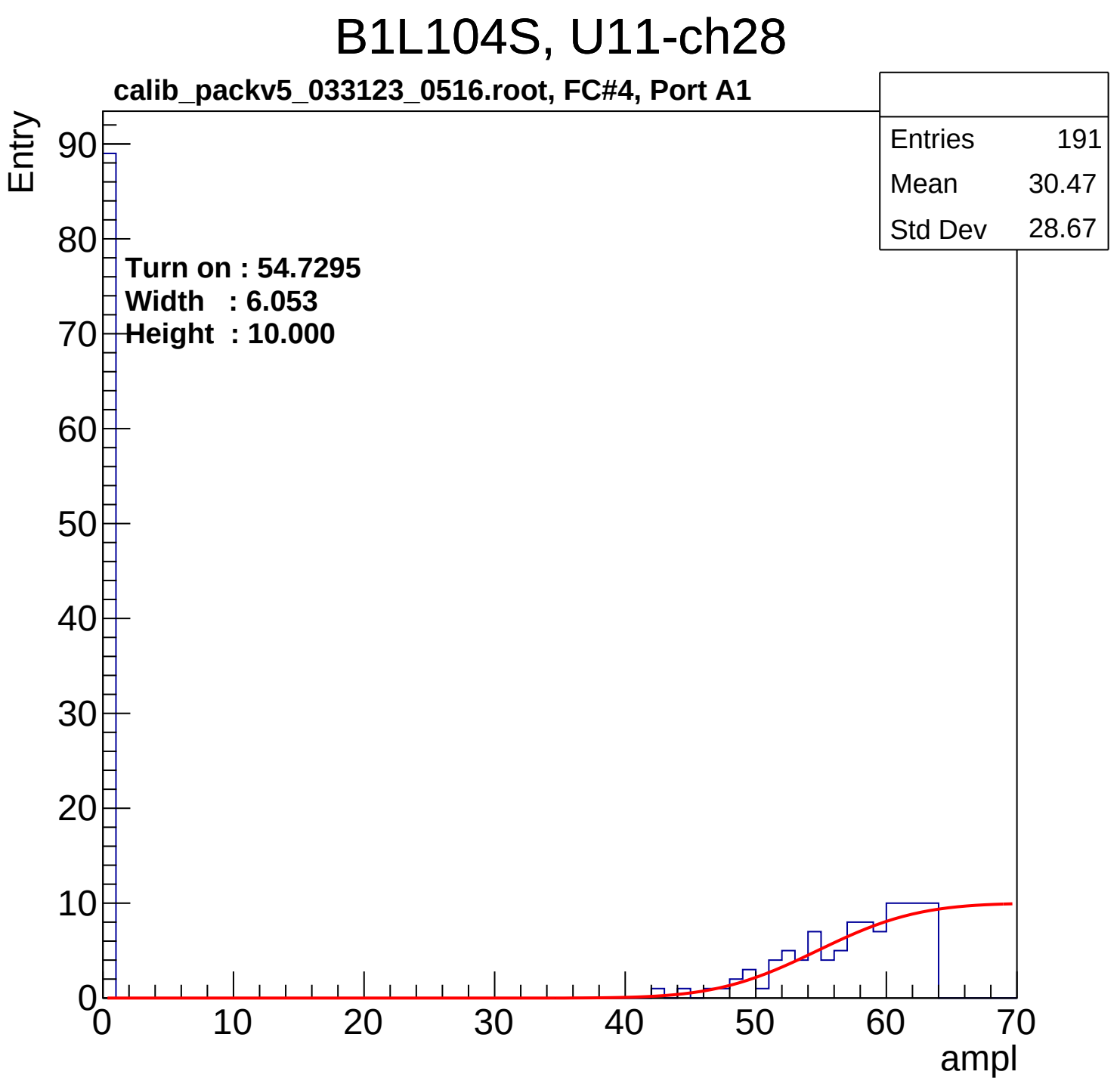

B1L104S, U10-ch113
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 161
Mean 29.42
Std Dev 29.36
Turn on : 56.3989
Width : 3.707
Height : 9.556
Entry
ampl
0
10
20
30
40
50
60
70
80

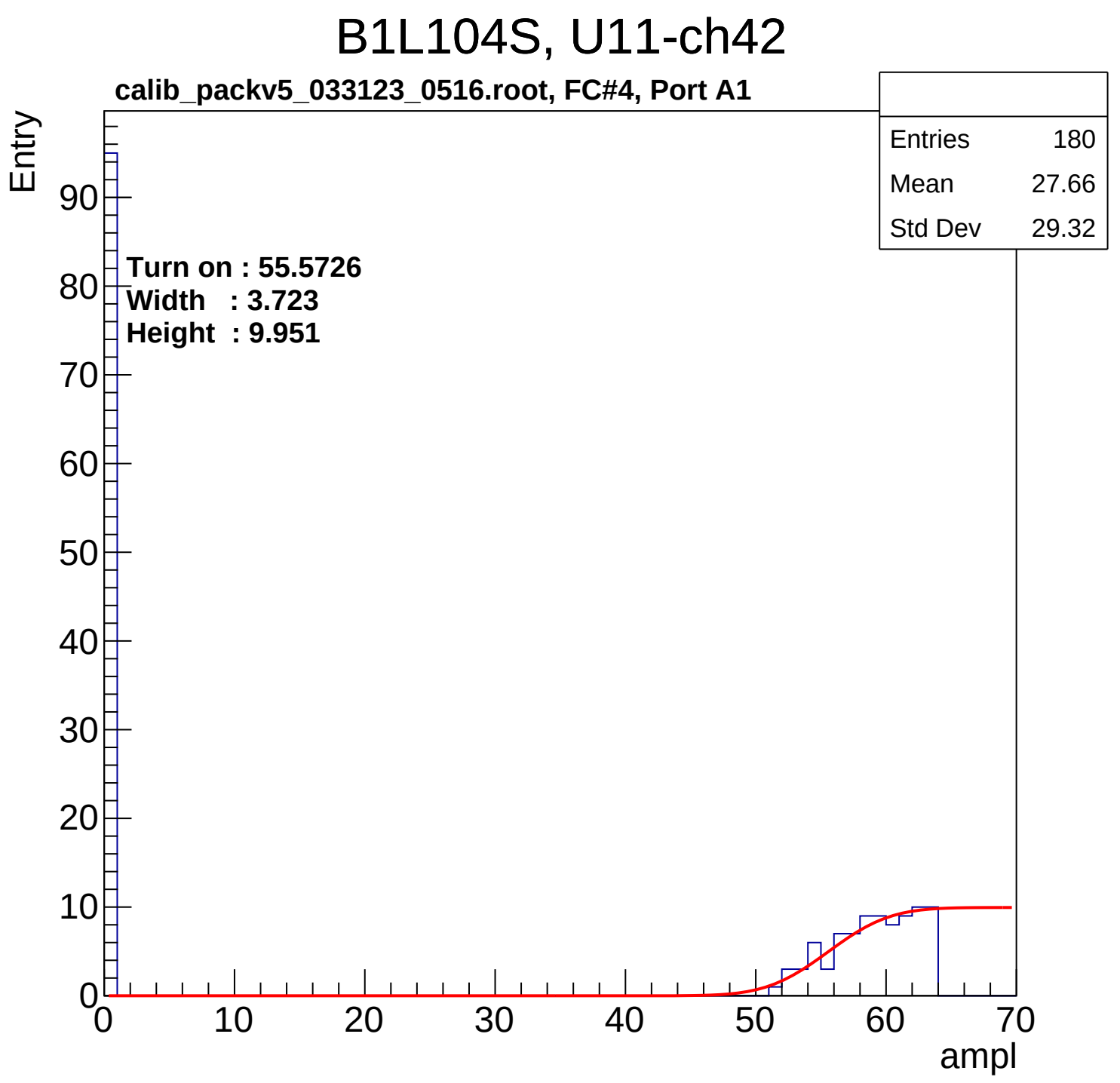

B1L104S, U10-ch115
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 166
Mean 29.7
Std Dev 29.44
Turn on : 55.9406
Width : 3.528
Height : 10.111
Entry
ampl
0
10
20
30
40
50
60
70
80

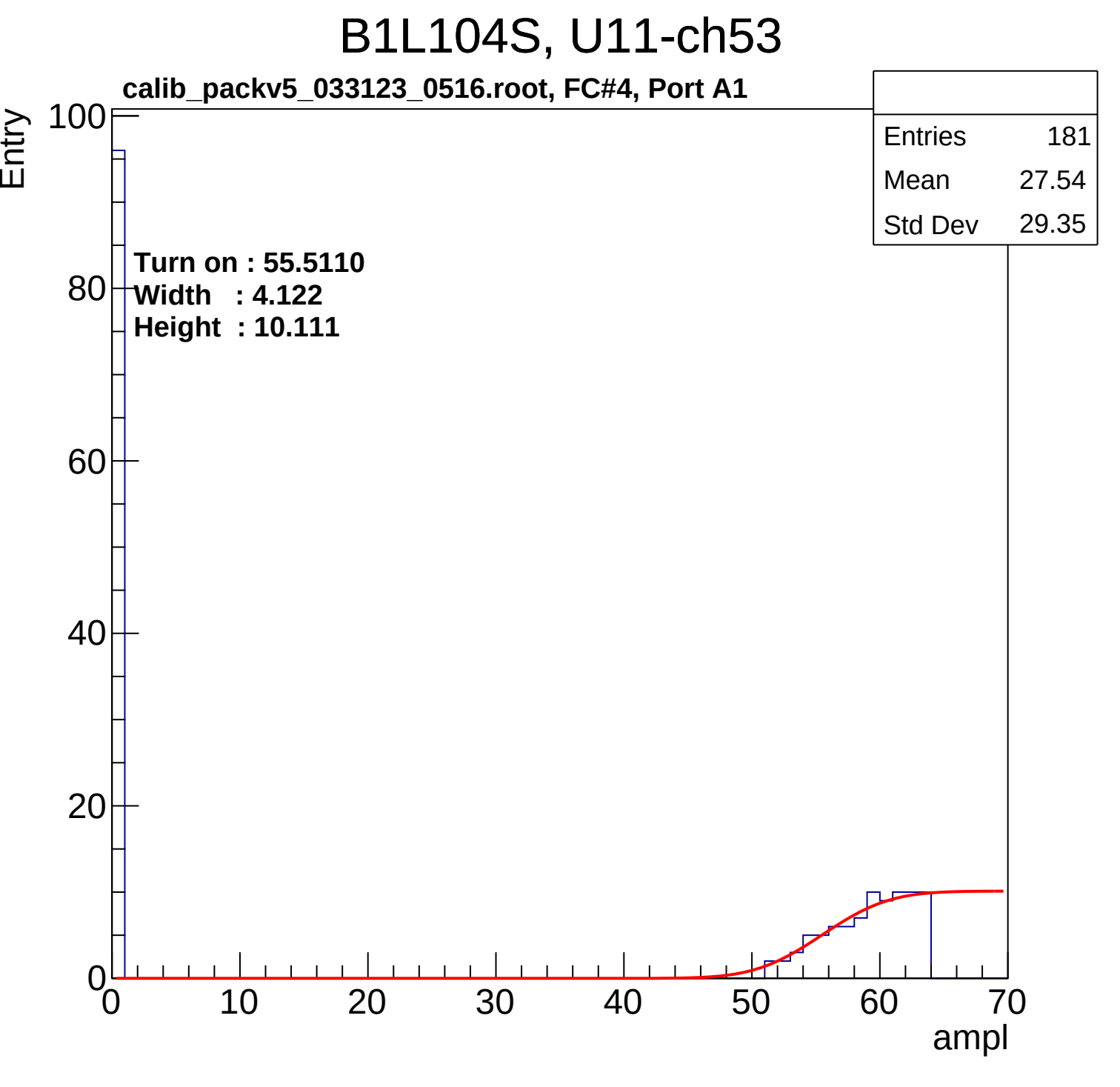

B1L104S, U10-ch121
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 152
Mean 31.52
Std Dev 29.24
Turn on : 56.6475
Width : 4.076
Height : 9.778
Entry
ampl
0
10
20
30
40
50
60
70

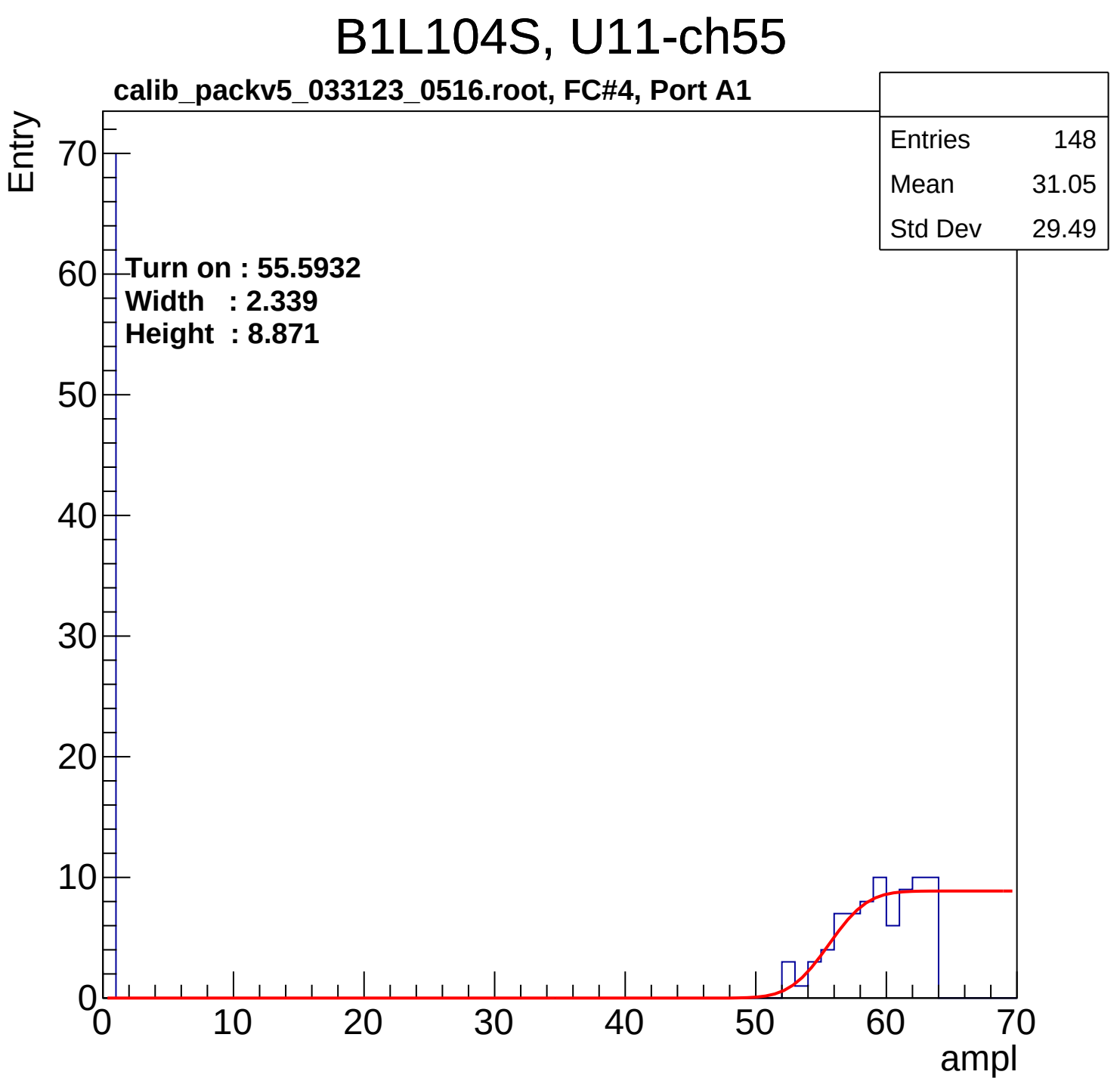

B1L104S, U11-ch0
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 300
Mean 28.28
Std Dev 27.24
Turn on : 47.4591
Width : 6.587
Height : 9.248
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

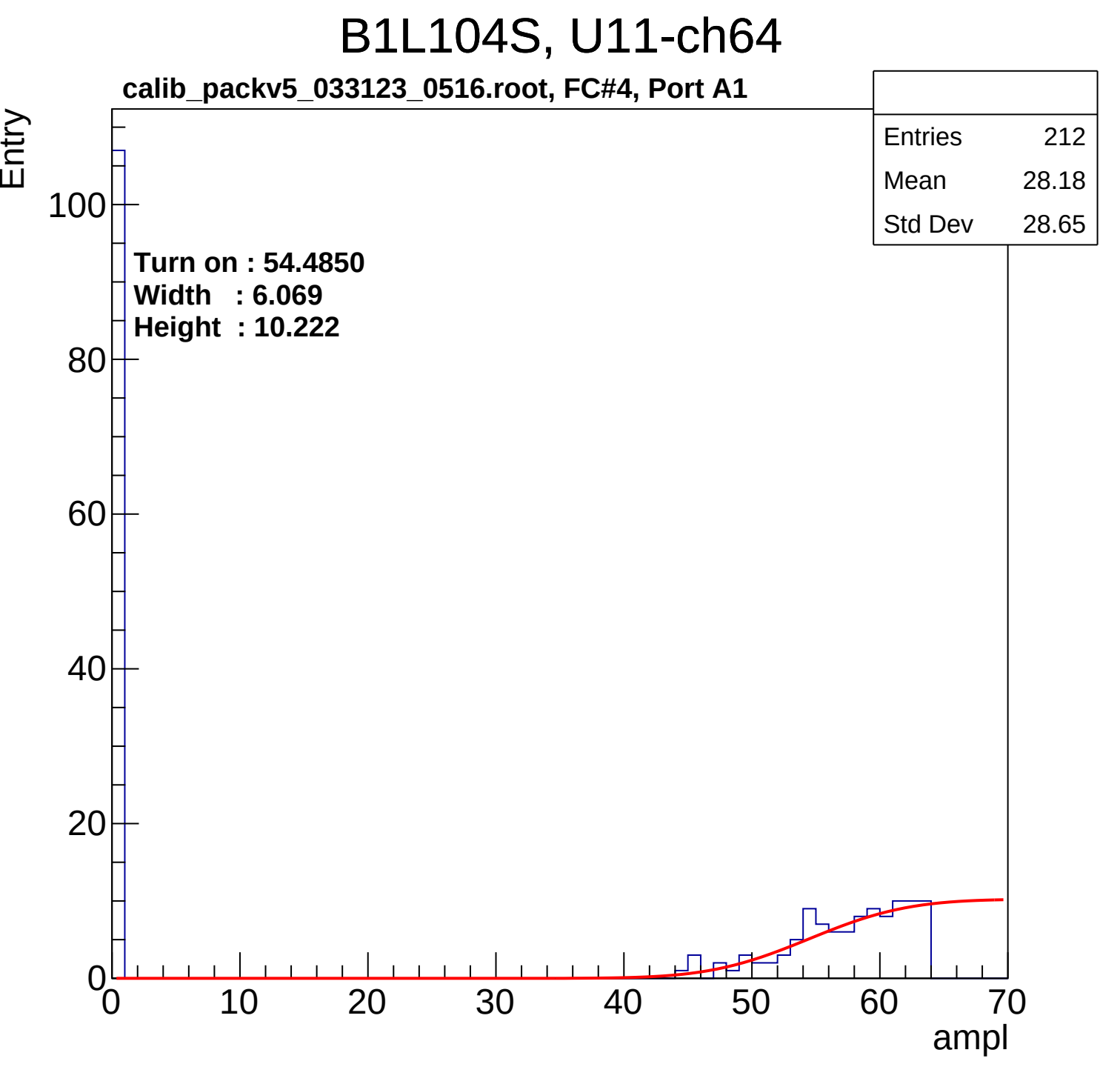

B1L104S, U11-ch7
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 154
Mean 31.99
Std Dev 29.3
Turn on : 55.5266
Width : 4.023
Height : 10.000
Entry
ampl
0
10
20
30
40
50
60
70

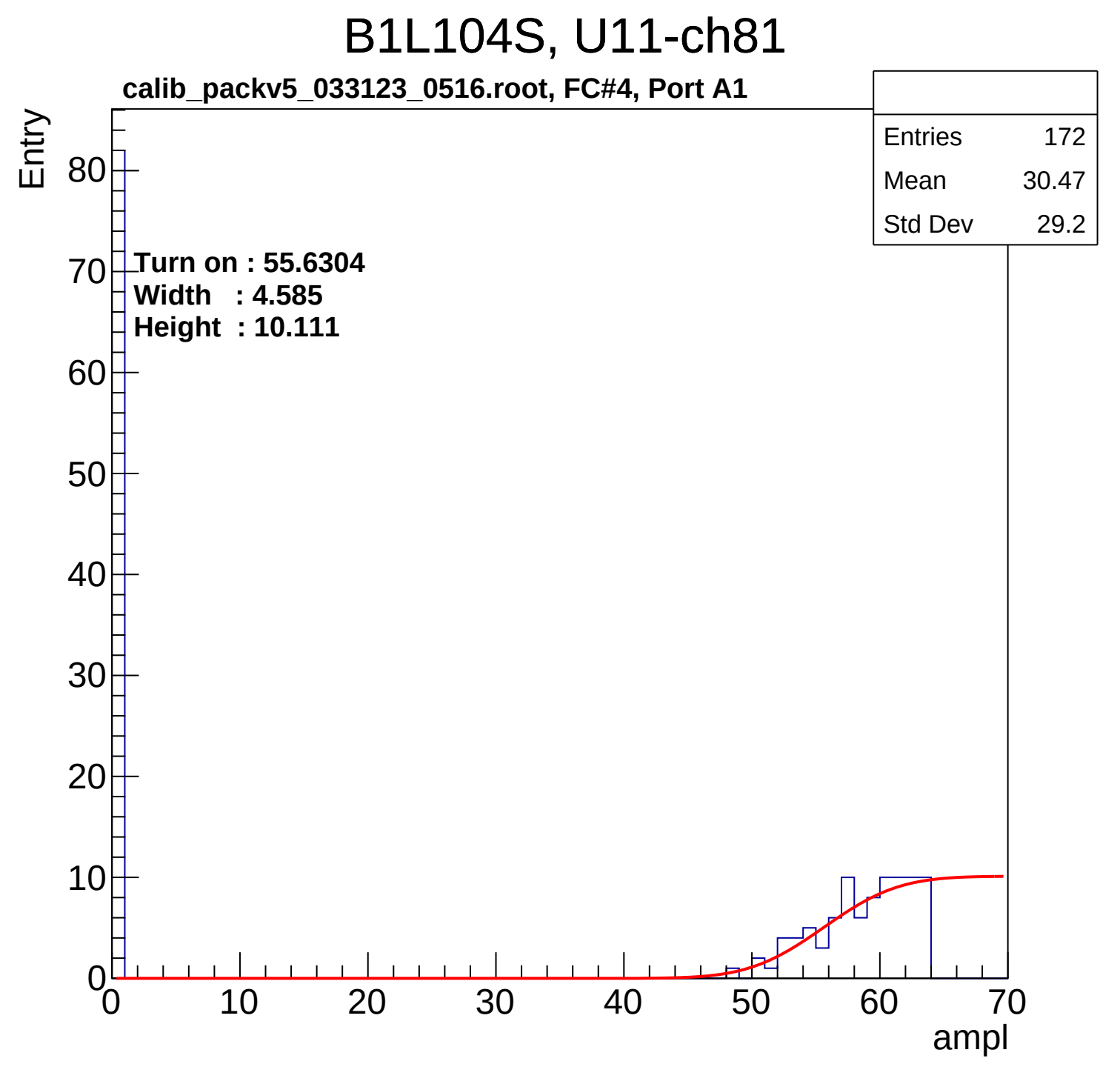

B1L104S, U11-ch28
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 191
Mean 30.47
Std Dev 28.67
Turn on : 54.7295
Width : 6.053
Height : 10.000
Entry
ampl
0
10
20
30
40
50
60
70
80
90

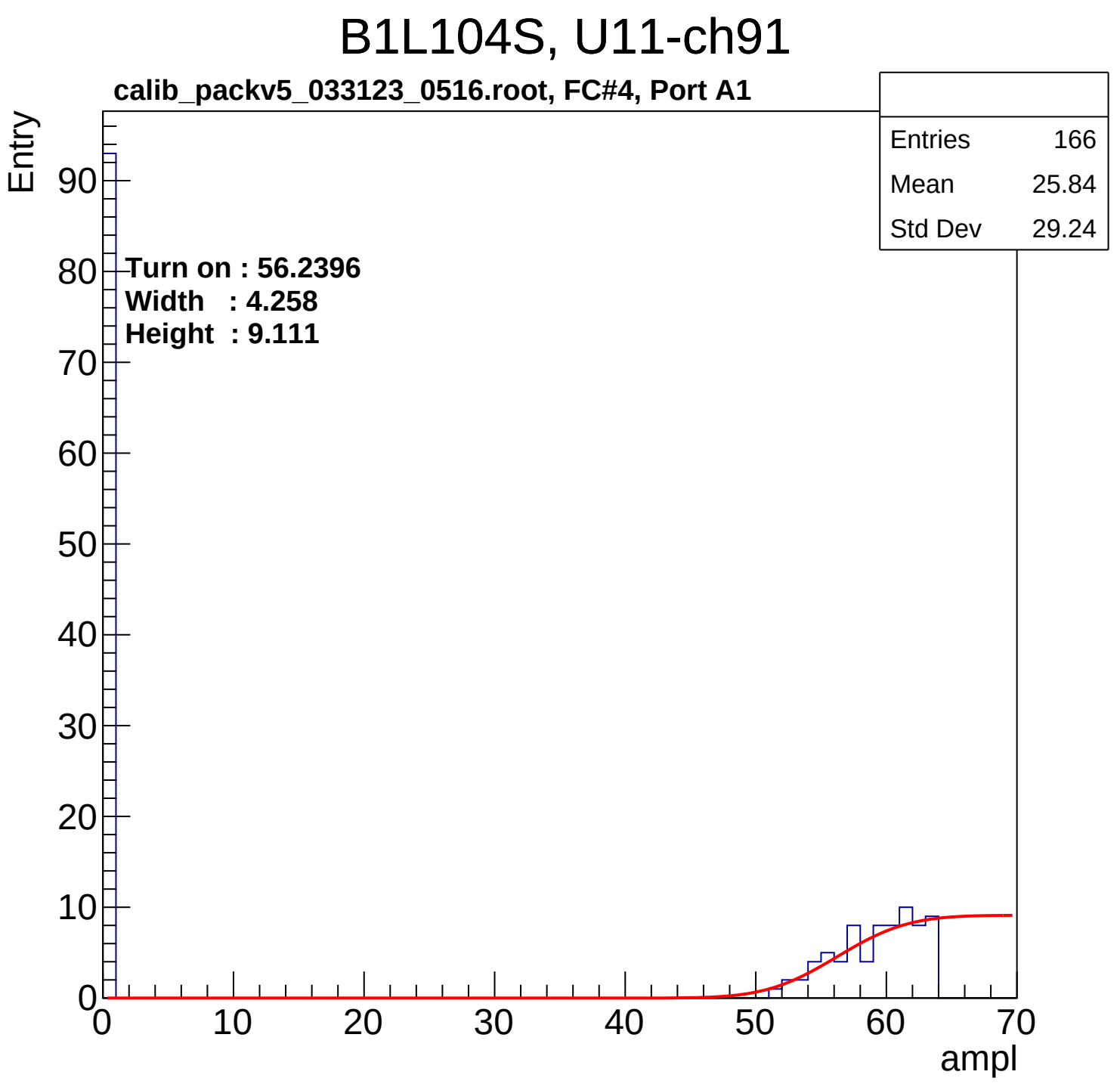

B1L104S, U11-ch42
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 180
Mean 27.66
Std Dev 29.32
Turn on : 55.5726
Width : 3.723
Height : 9.951
Entry
ampl
0
10
20
30
40
50
60
70
80
90

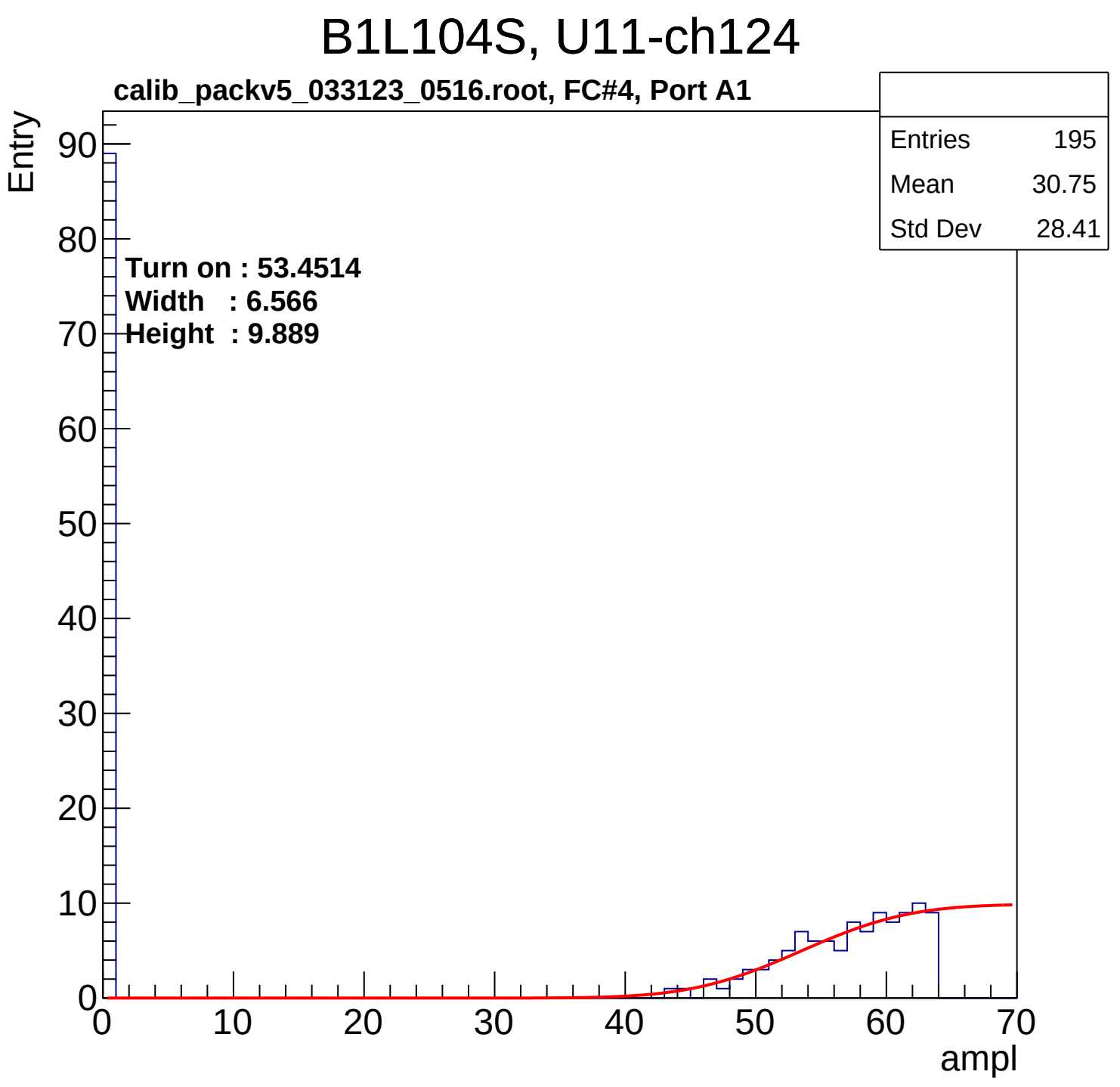

B1L104S, U11-ch53
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 181
Mean 27.54
Std Dev 29.35
Turn on : 55.5110
Width : 4.122
Height : 10.111
Entry
ampl
0
20
40
60
80
100
0
10
20
30
40
50
60
70

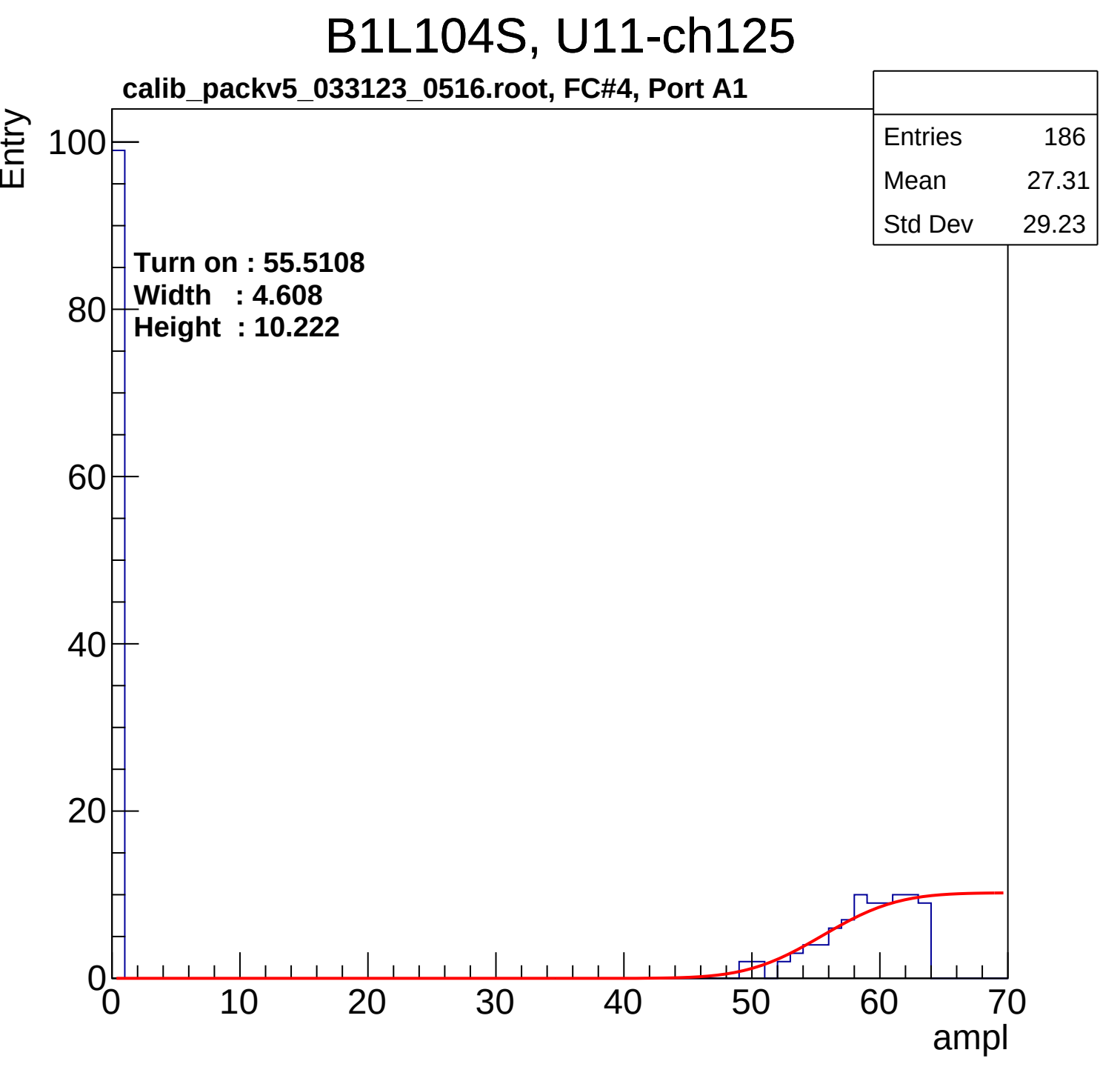

B1L104S, U11-ch55
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 148
Mean 31.05
Std Dev 29.49
Turn on : 55.5932
Width : 2.339
Height : 8.871
Entry
ampl
0
10
20
30
40
50
60
70


B1L104S, U11-ch64
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 212
Mean 28.18
Std Dev 28.65
Turn on : 54.4850
Width : 6.069
Height : 10.222
Entry
0
20
40
60
80
100
0
10
20
30
40
50
60
70
ampl


B1L104S, U11-ch81
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 172
Mean 30.47
Std Dev 29.2
Turn on : 55.6304
Width : 4.585
Height : 10.111
Entry
ampl
0
10
20
30
40
50
60
70
80


B1L104S, U11-ch91
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 166
Mean 25.84
Std Dev 29.24
Turn on : 56.2396
Width : 4.258
Height : 9.111
Entry
ampl
0
10
20
30
40
50
60
70
80
90


B1L104S, U11-ch124
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 195
Mean 30.75
Std Dev 28.41
Turn on : 53.4514
Width : 6.566
Height : 9.889
Entry
ampl
0
10
20
30
40
50
60
70
80
90


B1L104S, U11-ch125
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 186
Mean 27.31
Std Dev 29.23
Turn on : 55.5108
Width : 4.608
Height : 10.222
Entry
ampl
0
20
40
60
80
100
0
10
20
30
40
50
60
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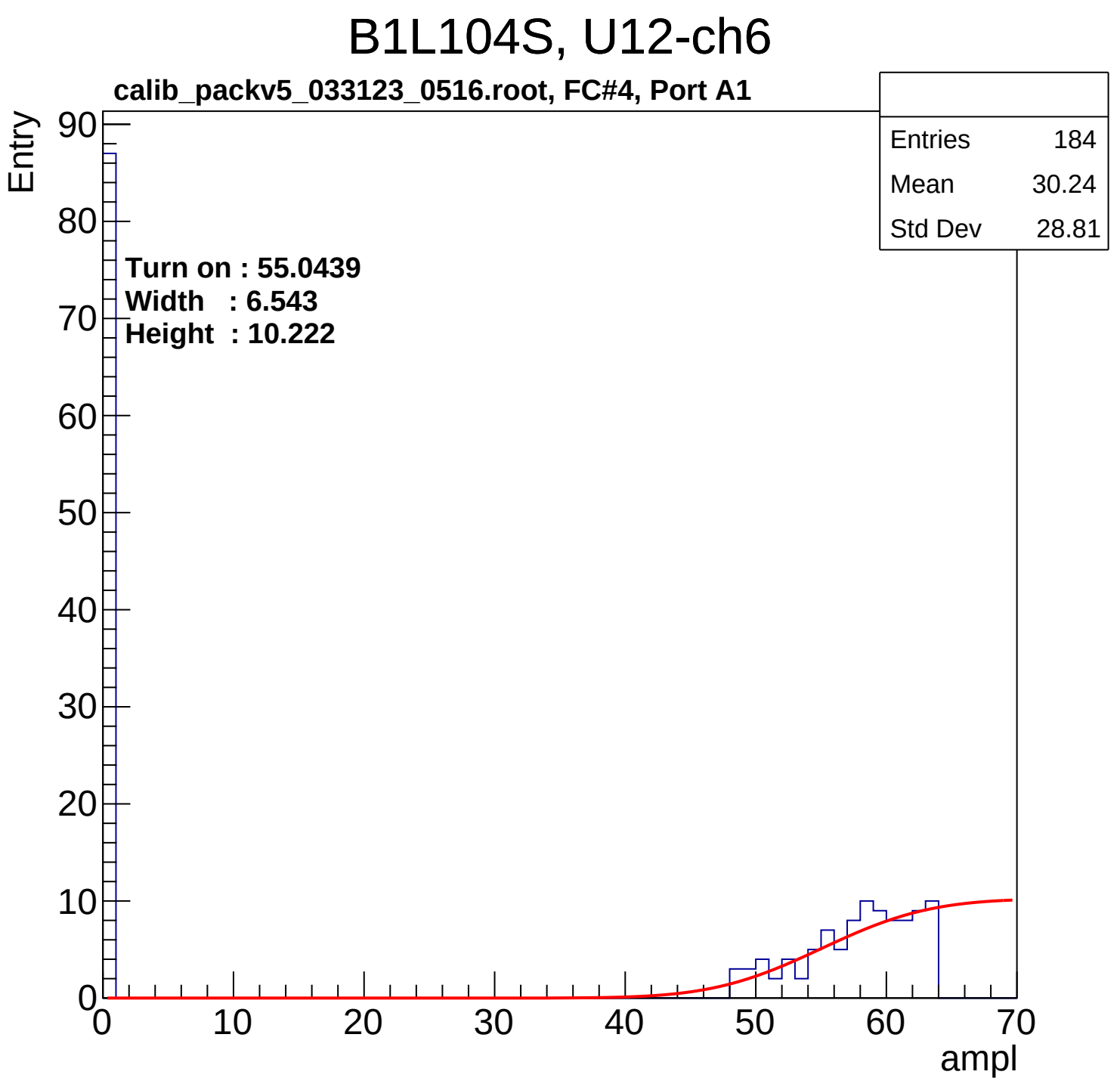
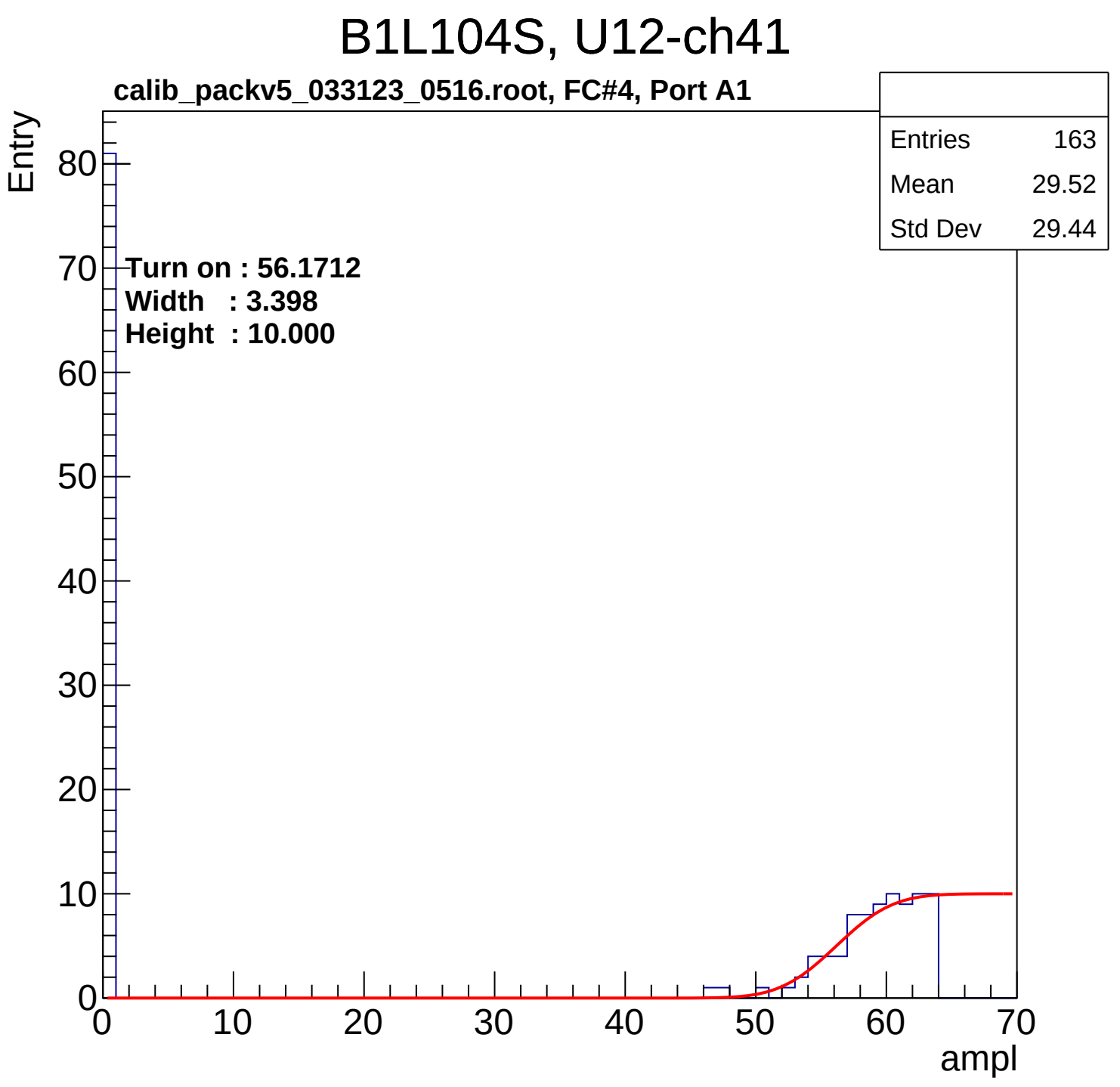
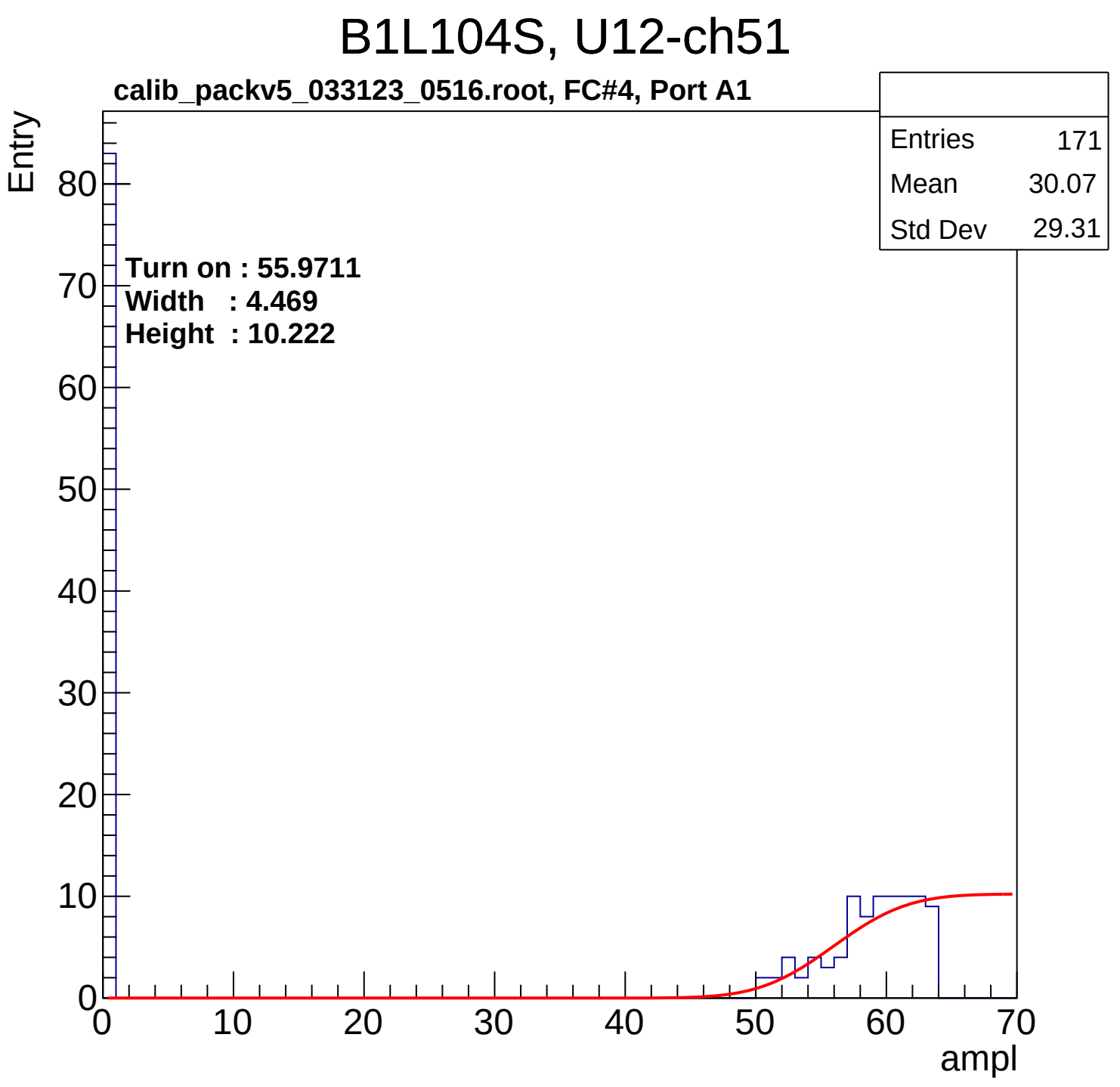
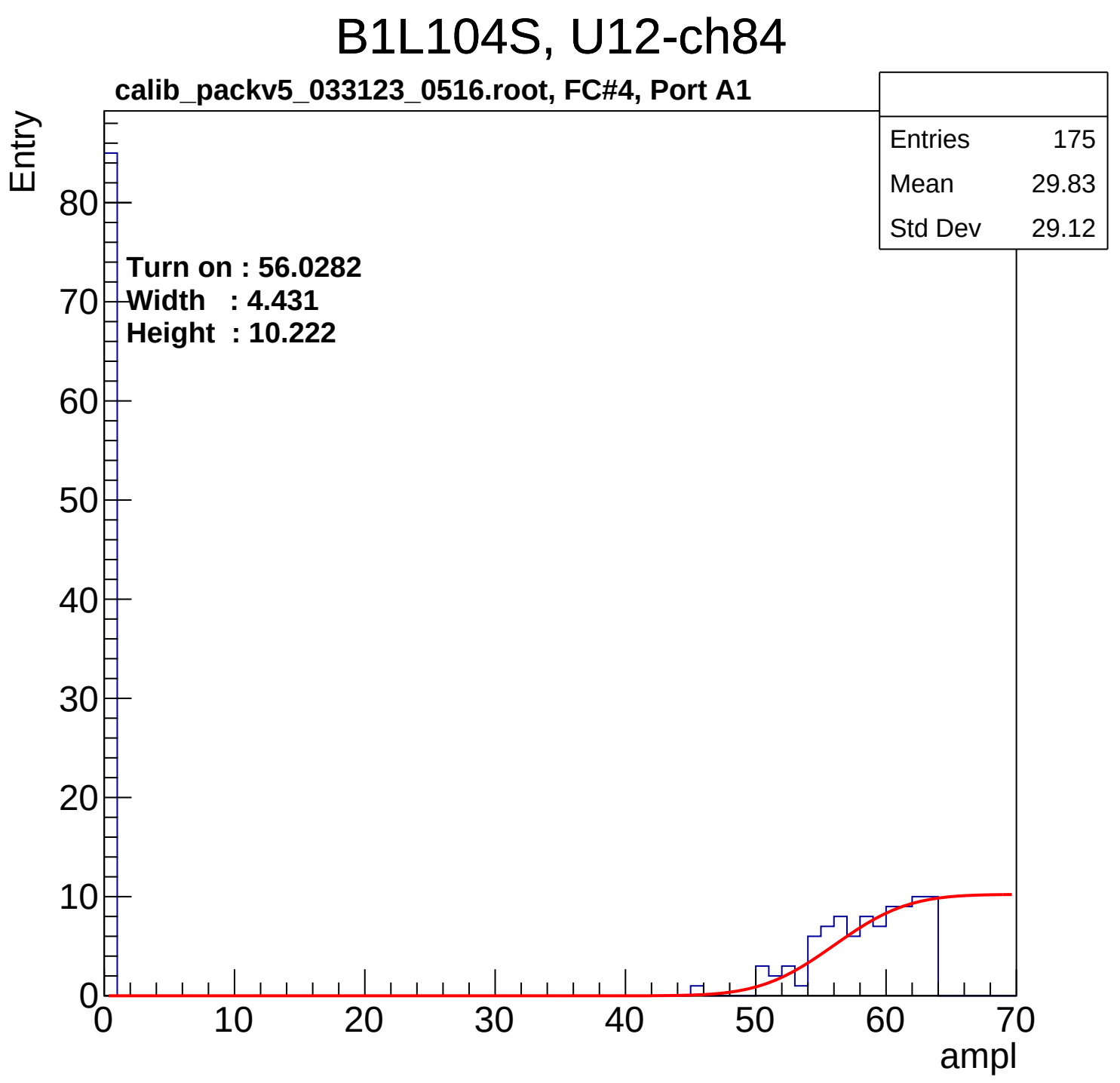

B1L104S, U12-ch6
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 184
Mean 30.24
Std Dev 28.81
Turn on : 55.0439
Width : 6.543
Height : 10.222
Entry
ampl
0
10
20
30
40
50
60
70
80
90


B1L104S, U12-ch41
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 163
Mean 29.52
Std Dev 29.44
Turn on : 56.1712
Width : 3.398
Height : 10.000
Entry
ampl
0
10
20
30
40
50
60
70
80


B1L104S, U12-ch51
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 171
Mean 30.07
Std Dev 29.31
Turn on : 55.9711
Width : 4.469
Height : 10.222
Entry
ampl
0
10
20
30
40
50
60
70
80


B1L104S, U12-ch84
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 175
Mean 29.83
Std Dev 29.12
Turn on : 56.0282
Width : 4.431
Height : 10.222
Entry
ampl
0
10
20
30
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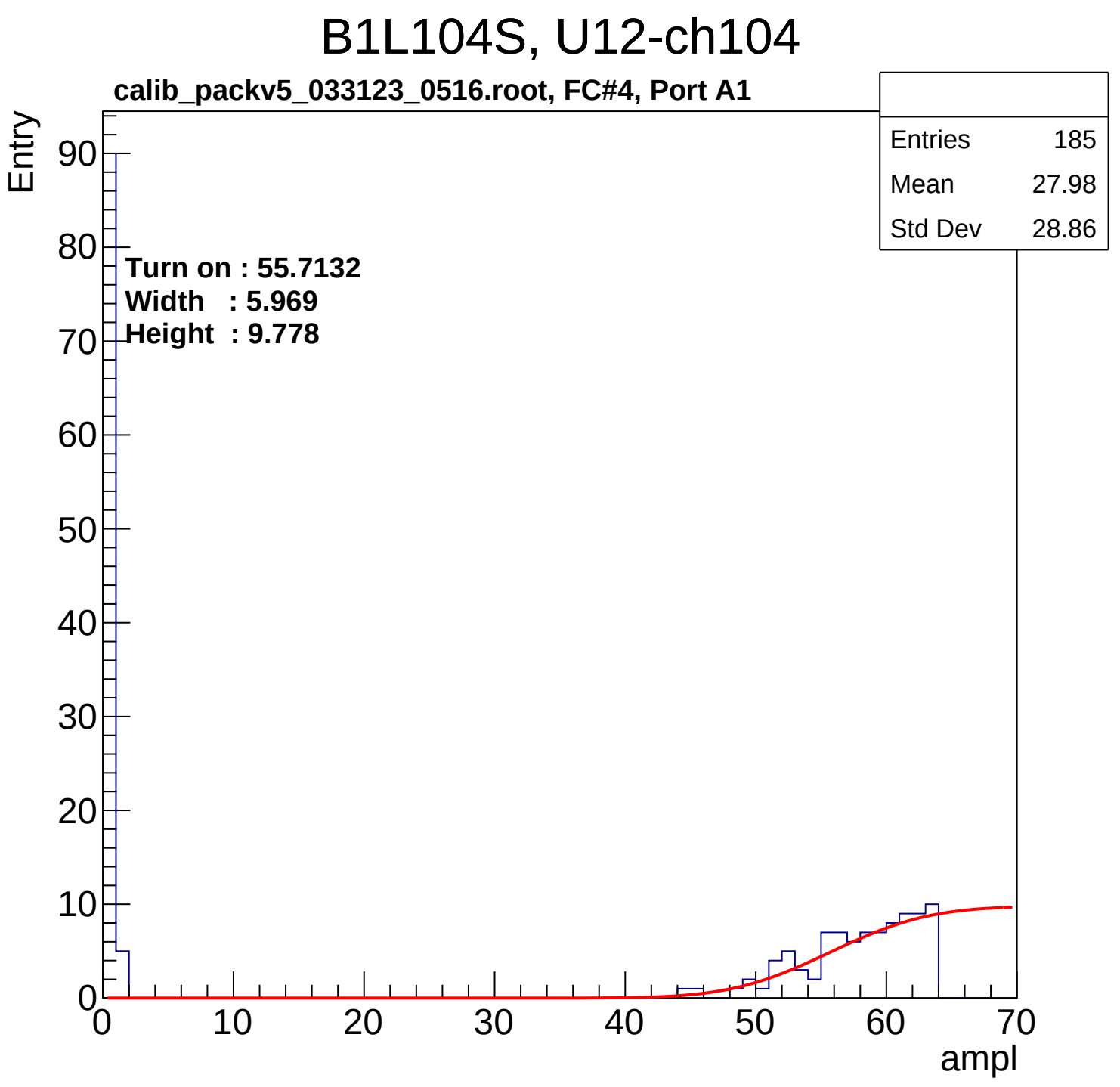
50
60
70
80


B1L104S, U12-ch104
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 185
Mean 27.98
Std Dev 28.86
Turn on : 55.7132
Width : 5.969
Height : 9.778
Entry
ampl
0
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20
30
40
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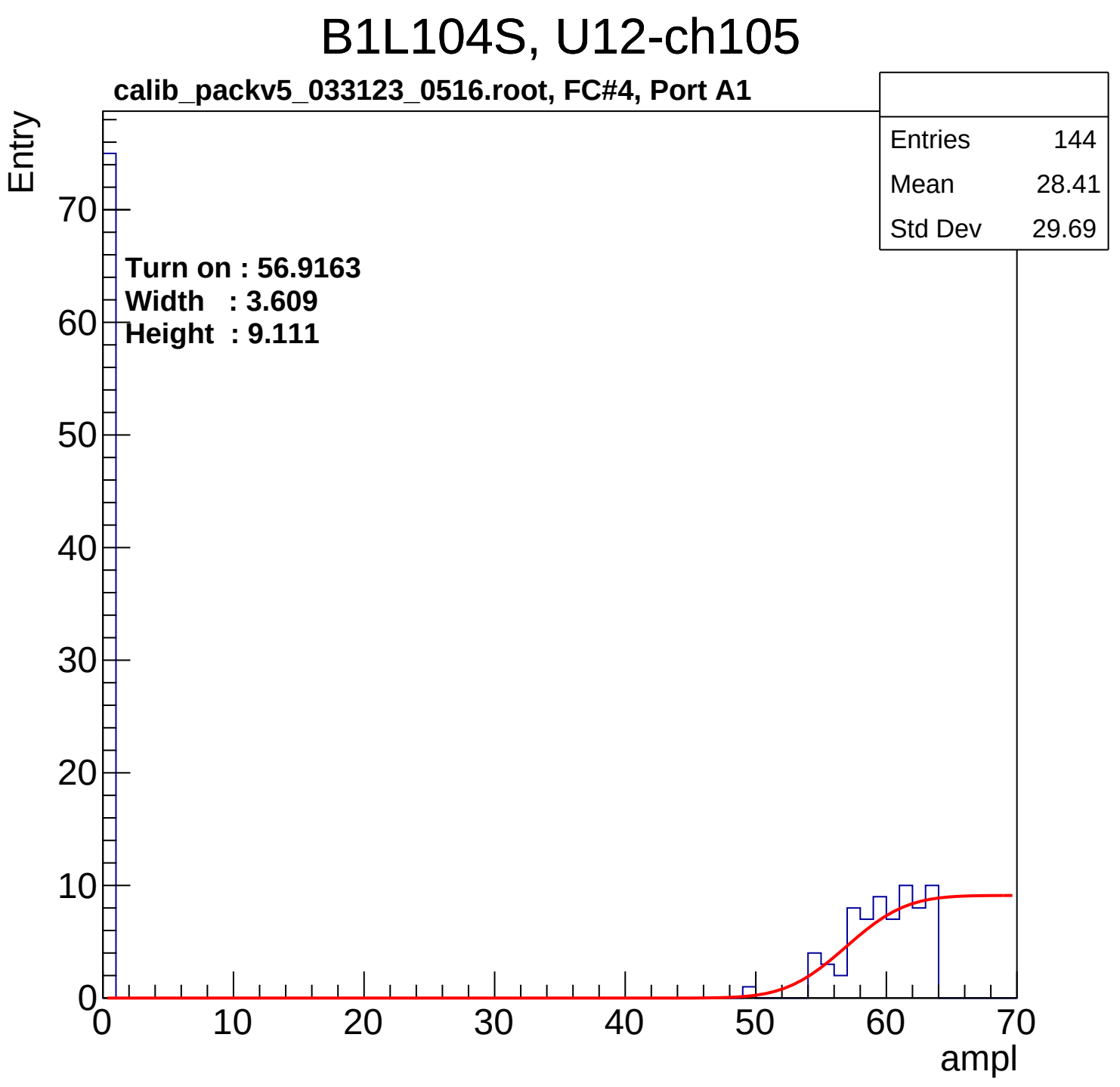
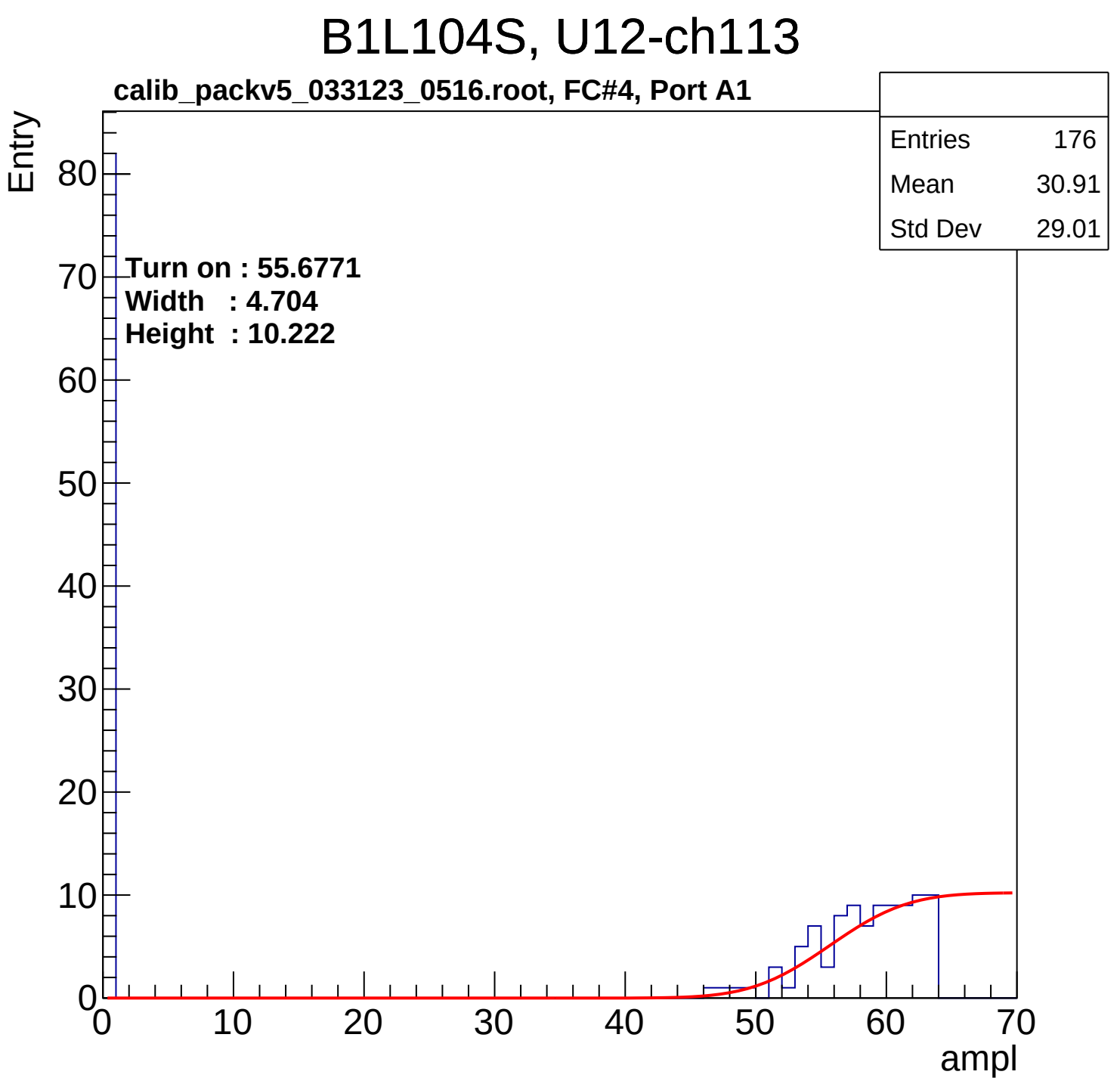
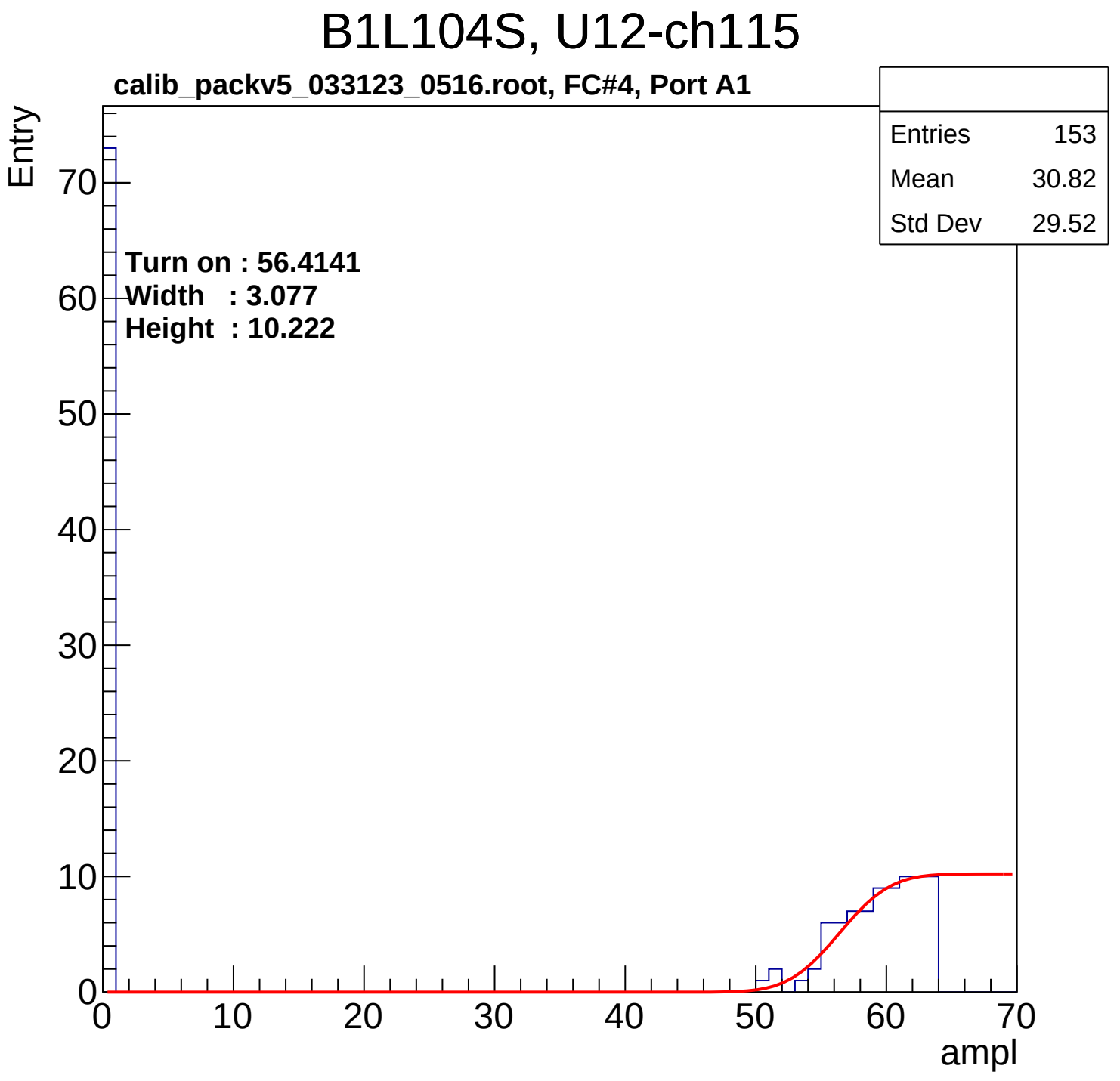
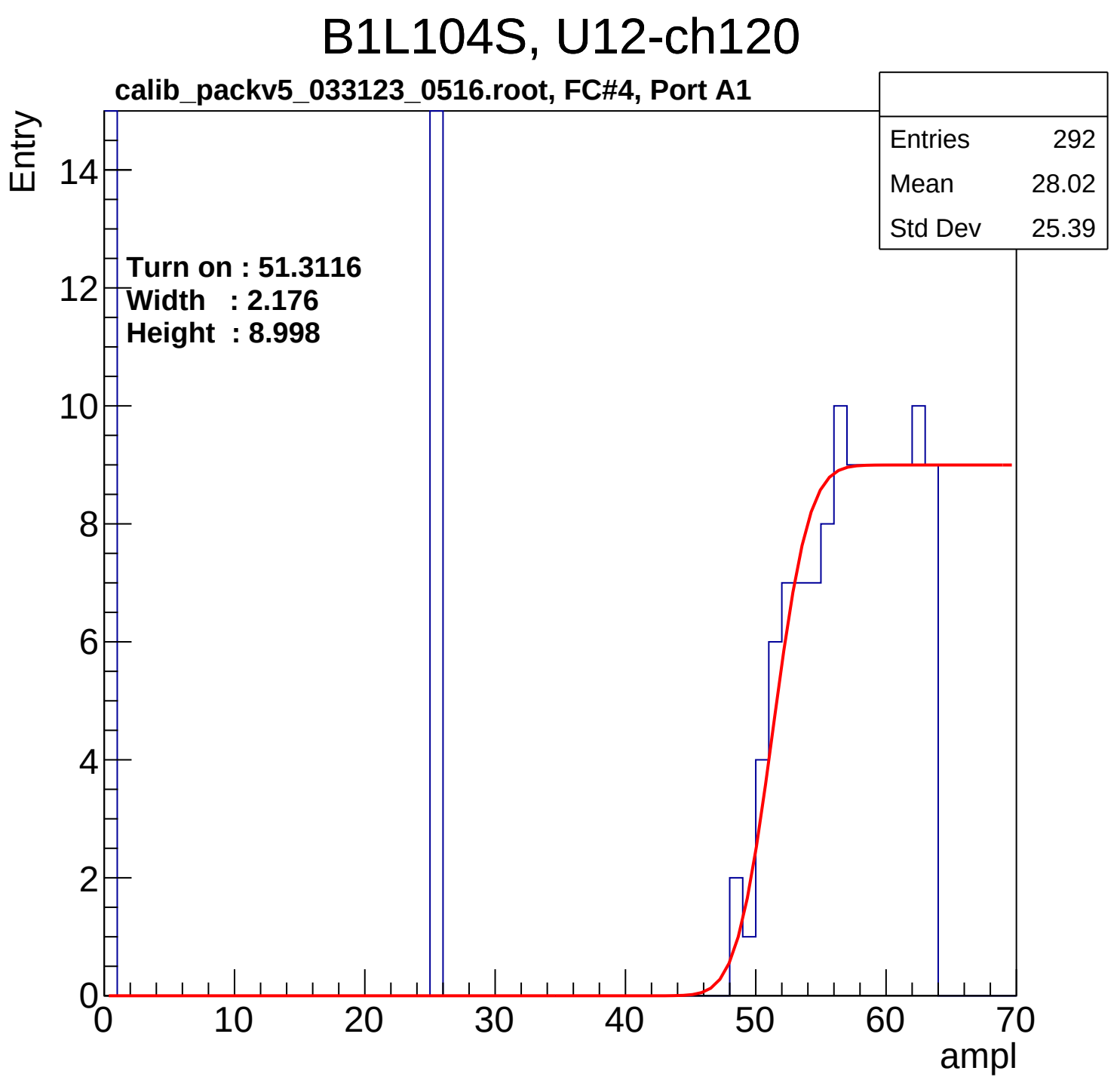
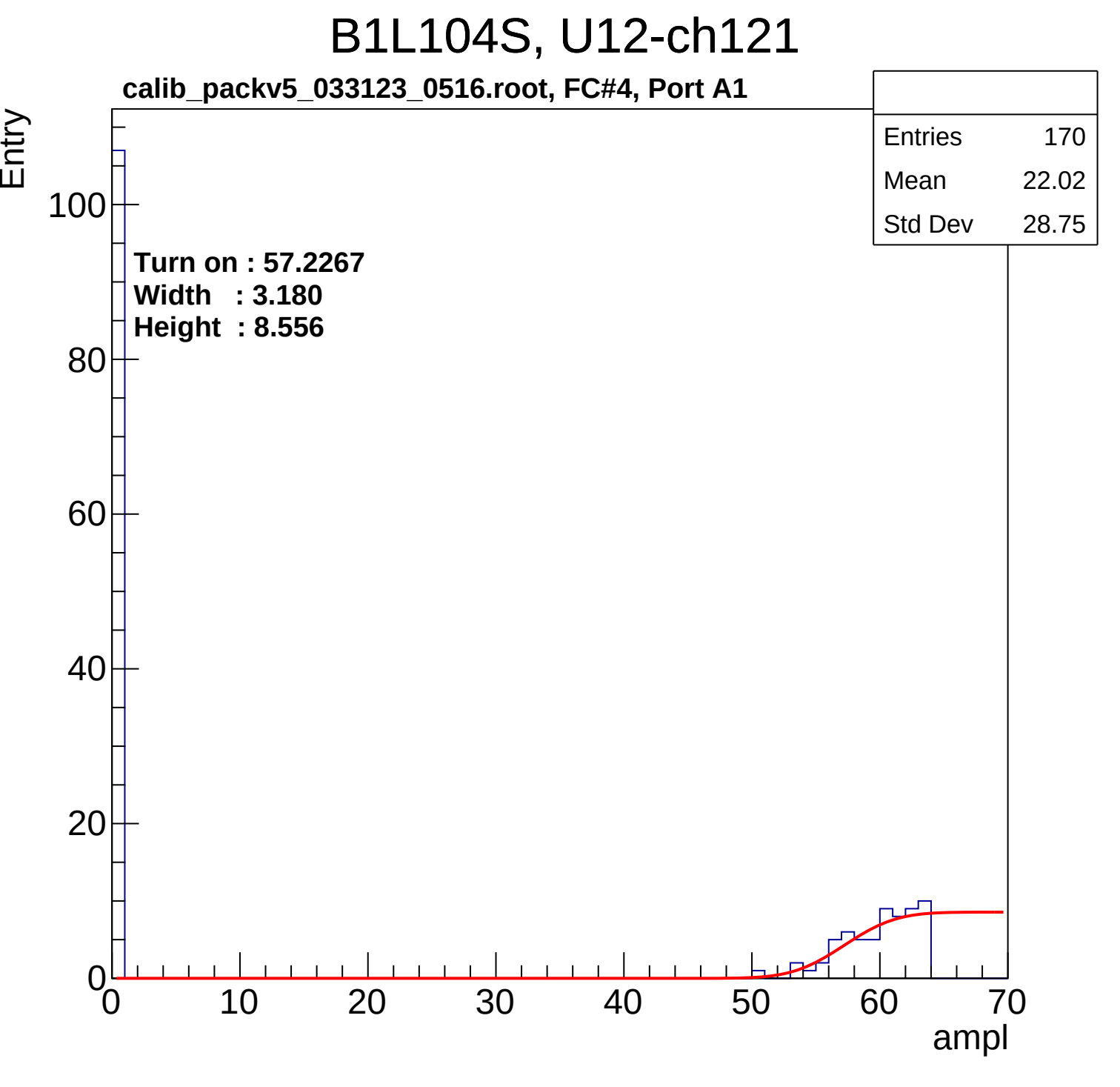
60
70
80
90


B1L104S, U12-ch105
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 144
Mean 28.41
Std Dev 29.69
Turn on : 56.9163
Width : 3.609
Height : 9.111
Entry
ampl
0
10
20
30
40
50
60
70


B1L104S, U12-ch113
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 176
Mean 30.91
Std Dev 29.01
Turn on : 55.6771
Width : 4.704
Height : 10.222
Entry
ampl
0
10
20
30
40
50
60
70
80


B1L104S, U12-ch115
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 153
Mean 30.82
Std Dev 29.52
Turn on : 56.4141
Width : 3.077
Height : 10.222
Entry
ampl
0
10
20
30
40
50
60
70


B1L104S, U12-ch120
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 292
Mean 28.02
Std Dev 25.39
Turn on : 51.3116
Width : 2.176
Height : 8.998
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L104S, U12-ch121
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 170
Mean 22.02
Std Dev 28.75
Turn on : 57.2267
Width : 3.180
Height : 8.556
Entry
ampl
0
20
40
60
80
100
0
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20
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40
50
60
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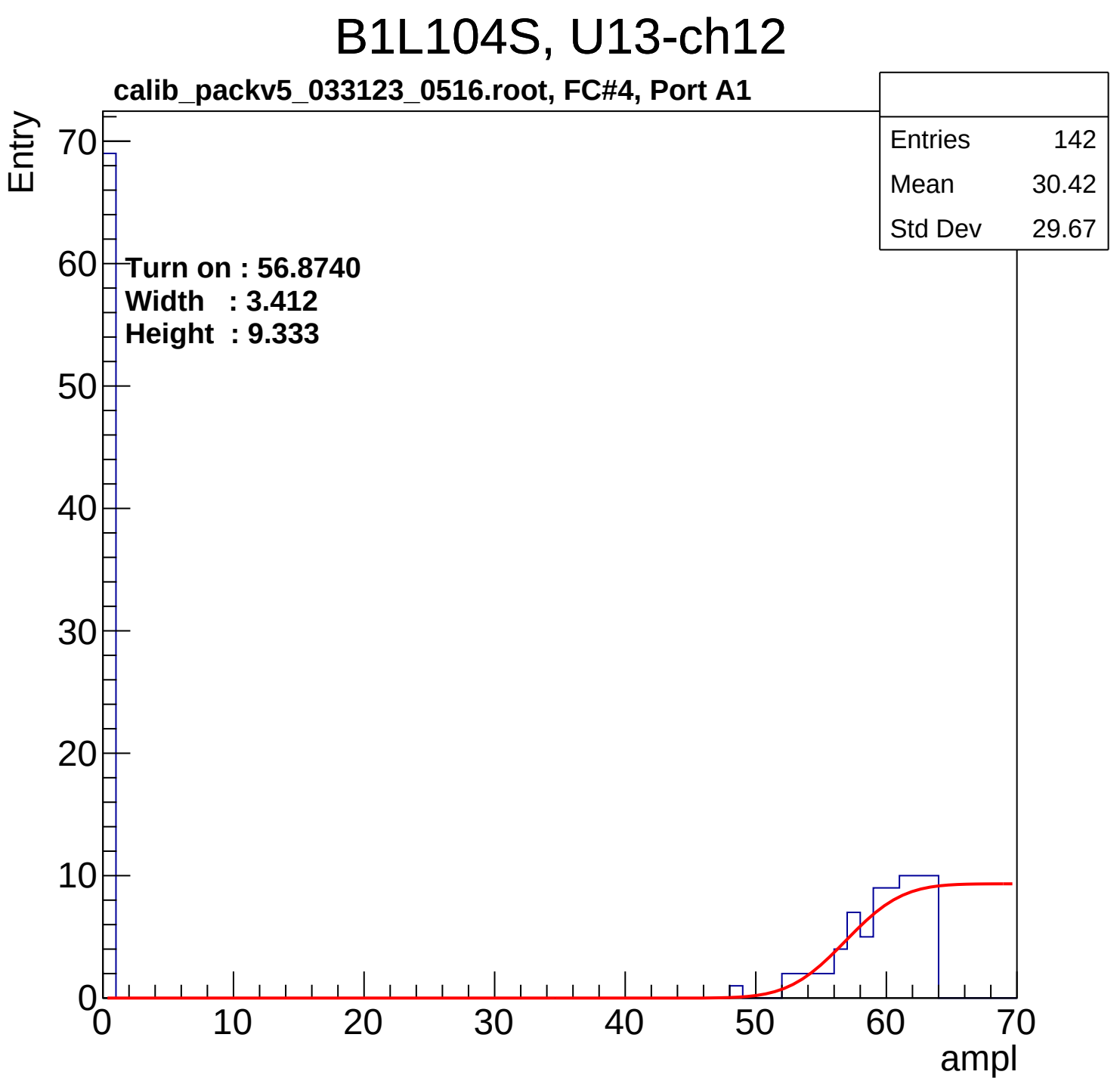
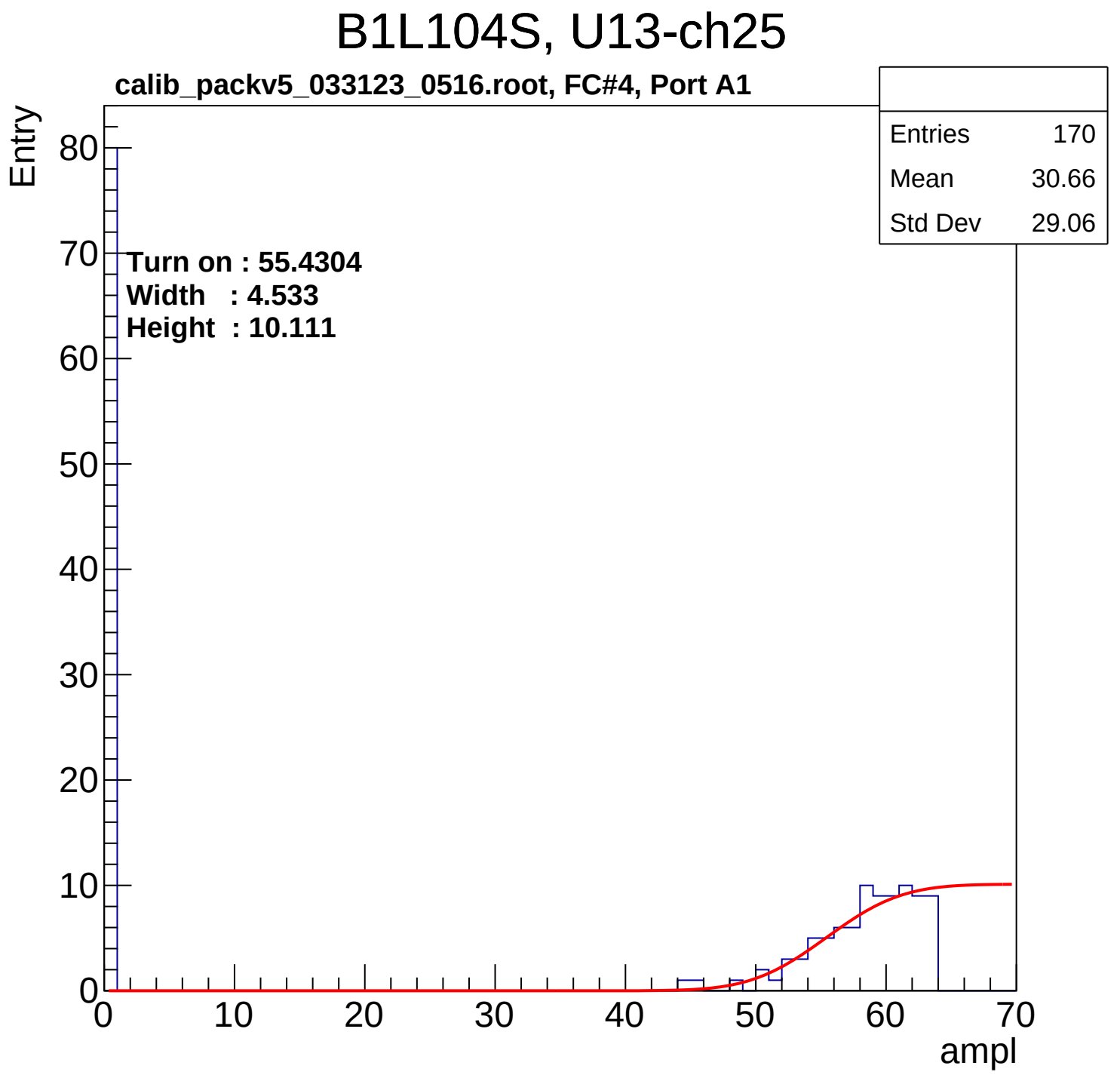
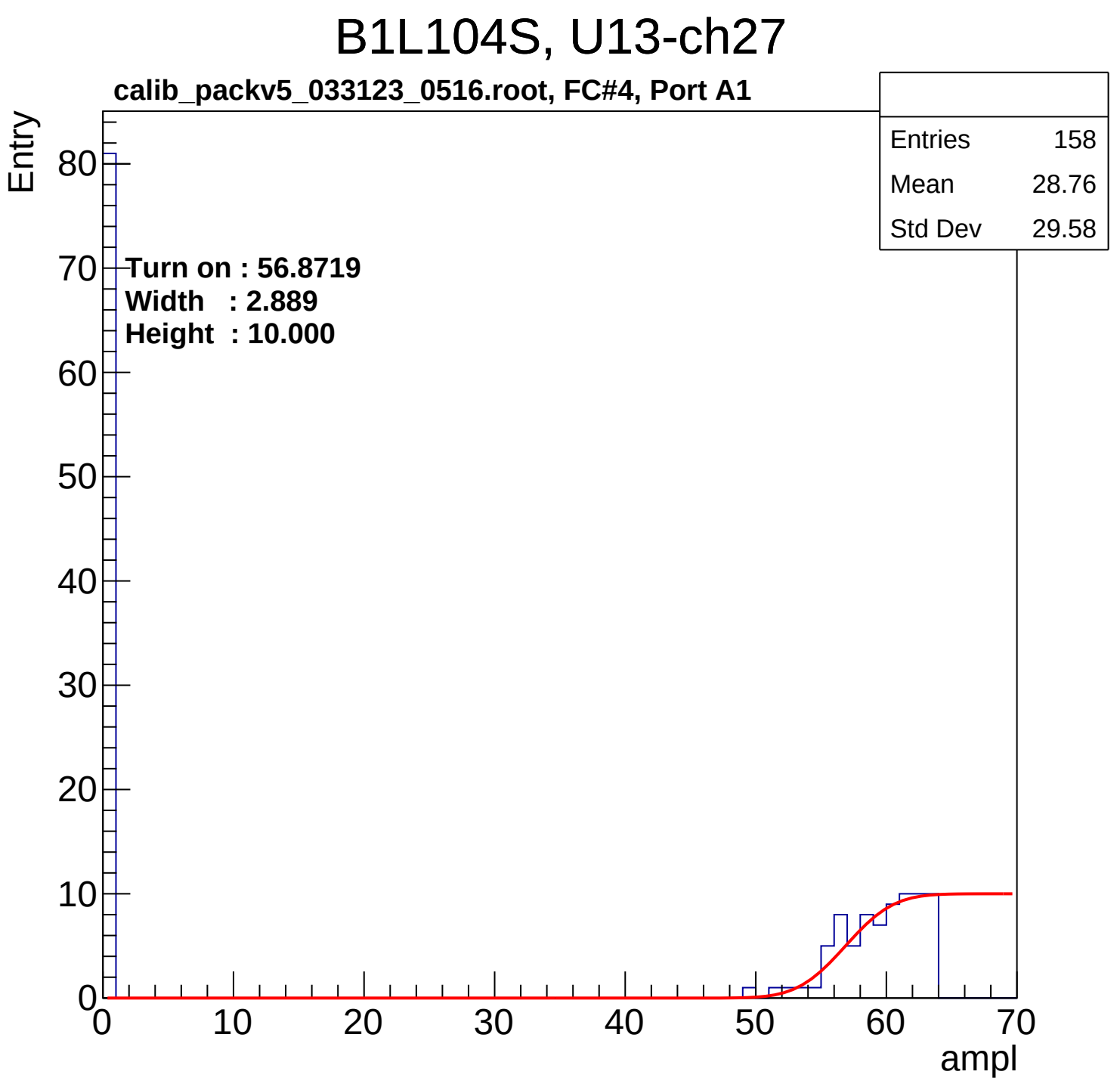

B1L104S, U13-ch12
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 142
Mean 30.42
Std Dev 29.67
Turn on : 56.8740
Width : 3.412
Height : 9.333
Entry
ampl
0
10
20
30
40
50
60
70


B1L104S, U13-ch25
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 170
Mean 30.66
Std Dev 29.06
Turn on : 55.4304
Width : 4.533
Height : 10.111
Entry
ampl
0
10
20
30
40
50
60
70
80


B1L104S, U13-ch27
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 158
Mean 28.76
Std Dev 29.58
Turn on : 56.8719
Width : 2.889
Height : 10.000
Entry
ampl
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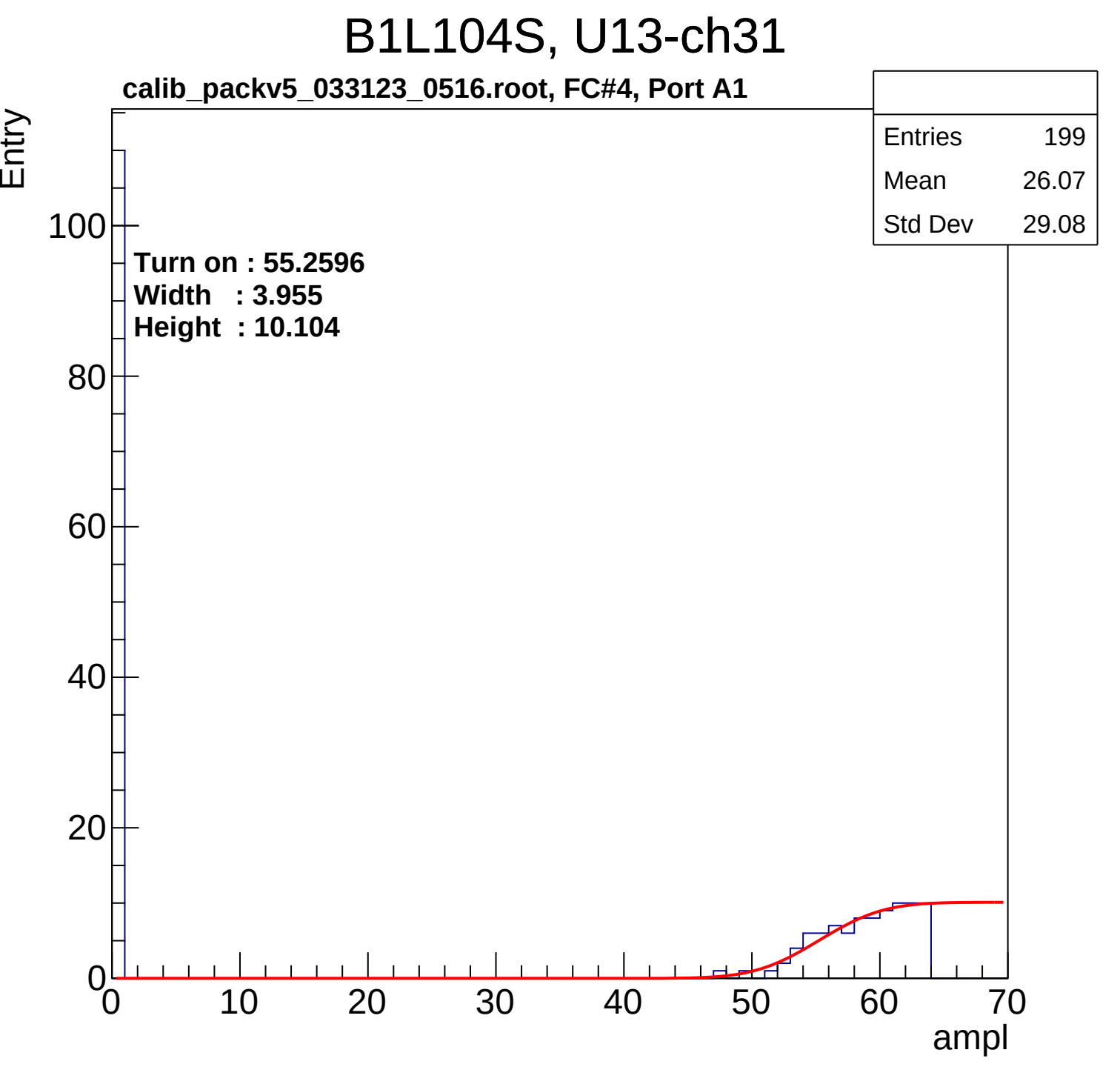
B1L104S, U13-ch31
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 199
Mean 26.07
Std Dev 29.08
Turn on : 55.2596
Width : 3.955
Height : 10.104
Entry
ampl
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20
40
60
80
100
0
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40
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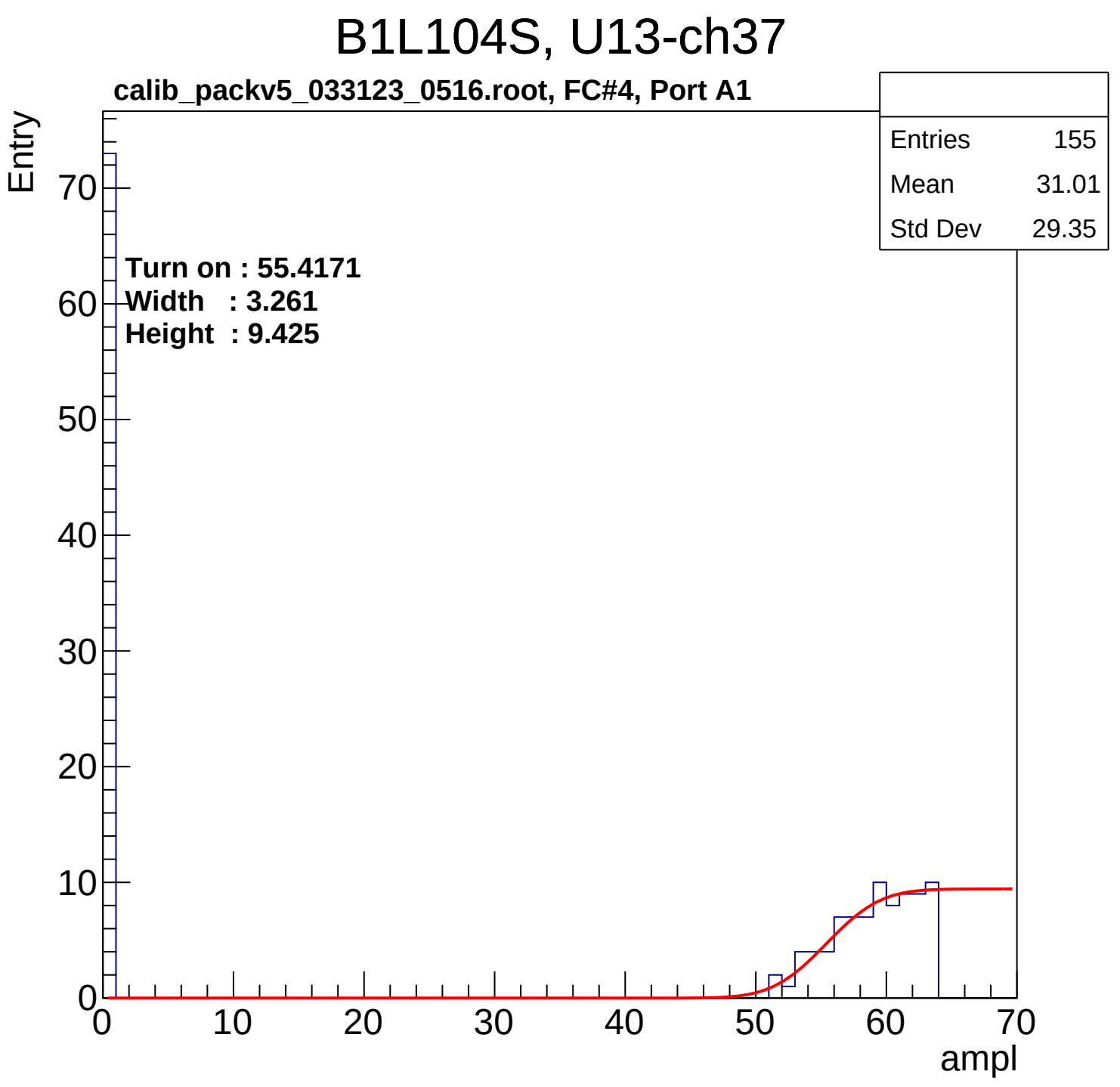
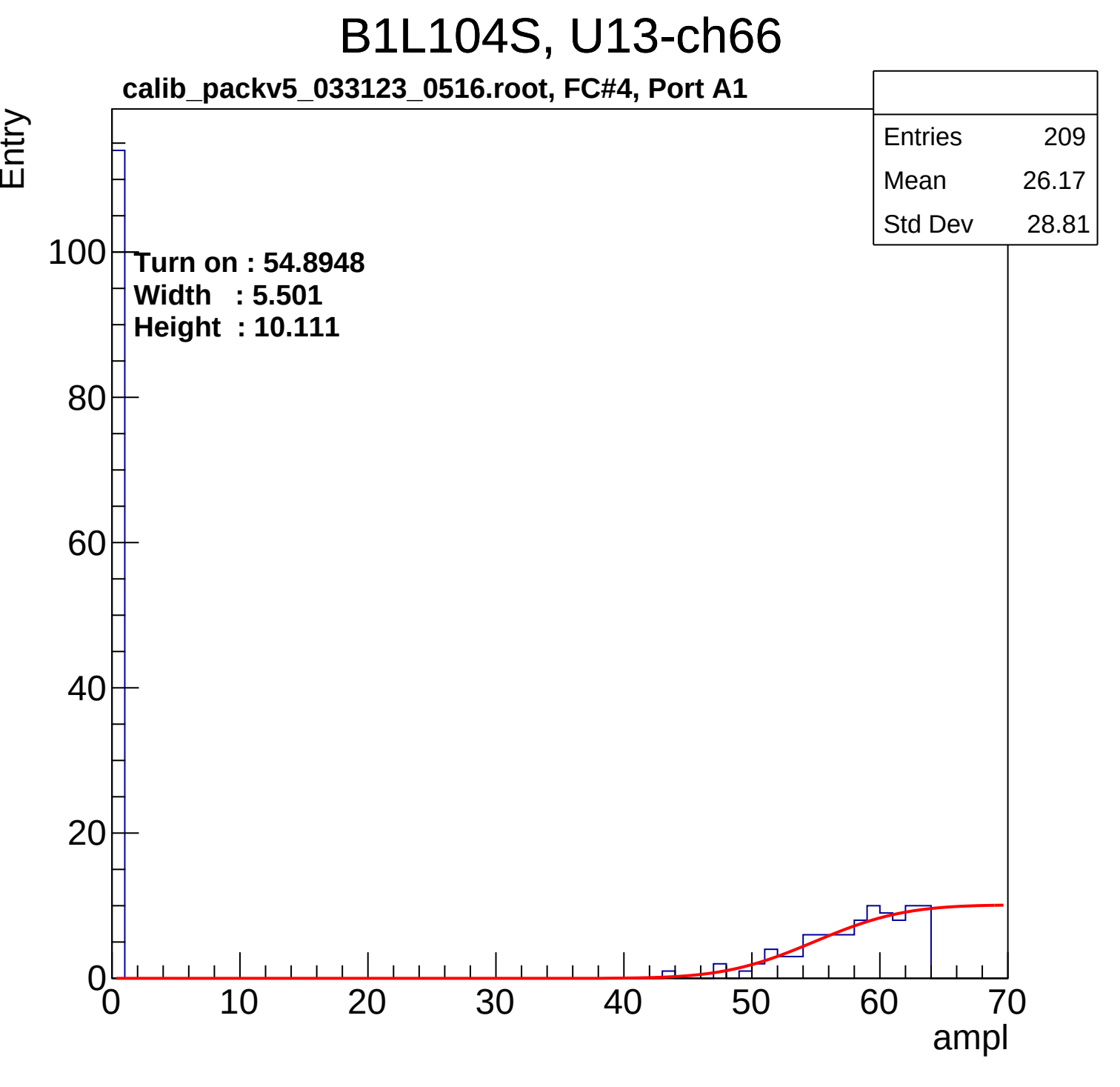

B1L104S, U13-ch37
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 155
Mean 31.01
Std Dev 29.35
Turn on : 55.4171
Width : 3.261
Height : 9.425
Entry
ampl
0
10
20
30
40
50
60
70


B1L104S, U13-ch66
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 209
Mean 26.17
Std Dev 28.81
Turn on : 54.8948
Width : 5.501
Height : 10.111
Entry
ampl
0
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40
60
80
100
0
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20
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40
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60
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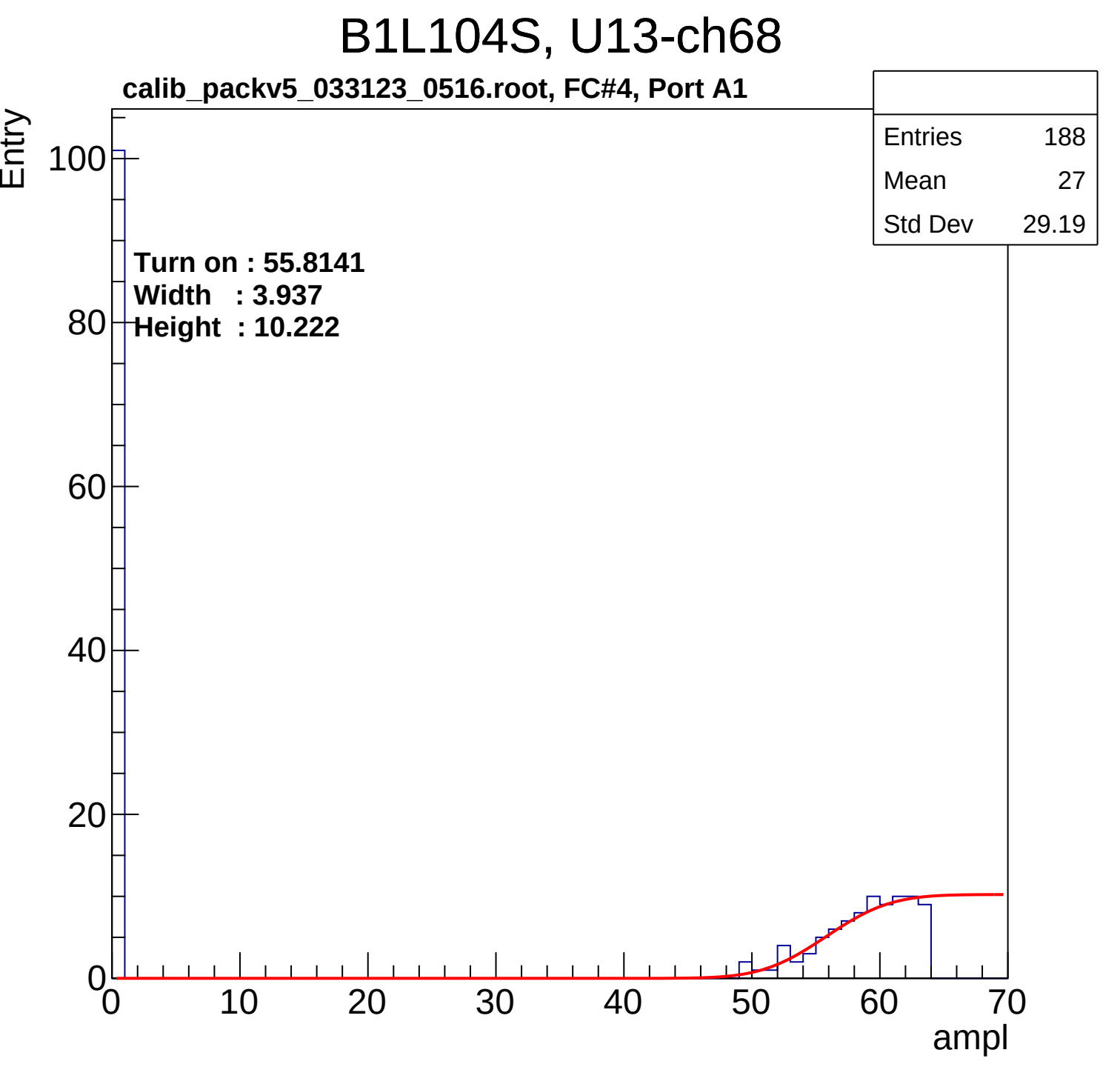
B1L104S, U13-ch68
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 188
Mean 27
Std Dev 29.19
Turn on : 55.8141
Width : 3.937
Height : 10.222
Entry
ampl
0
20
40
60
80
100
0
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20
30
40
50
60
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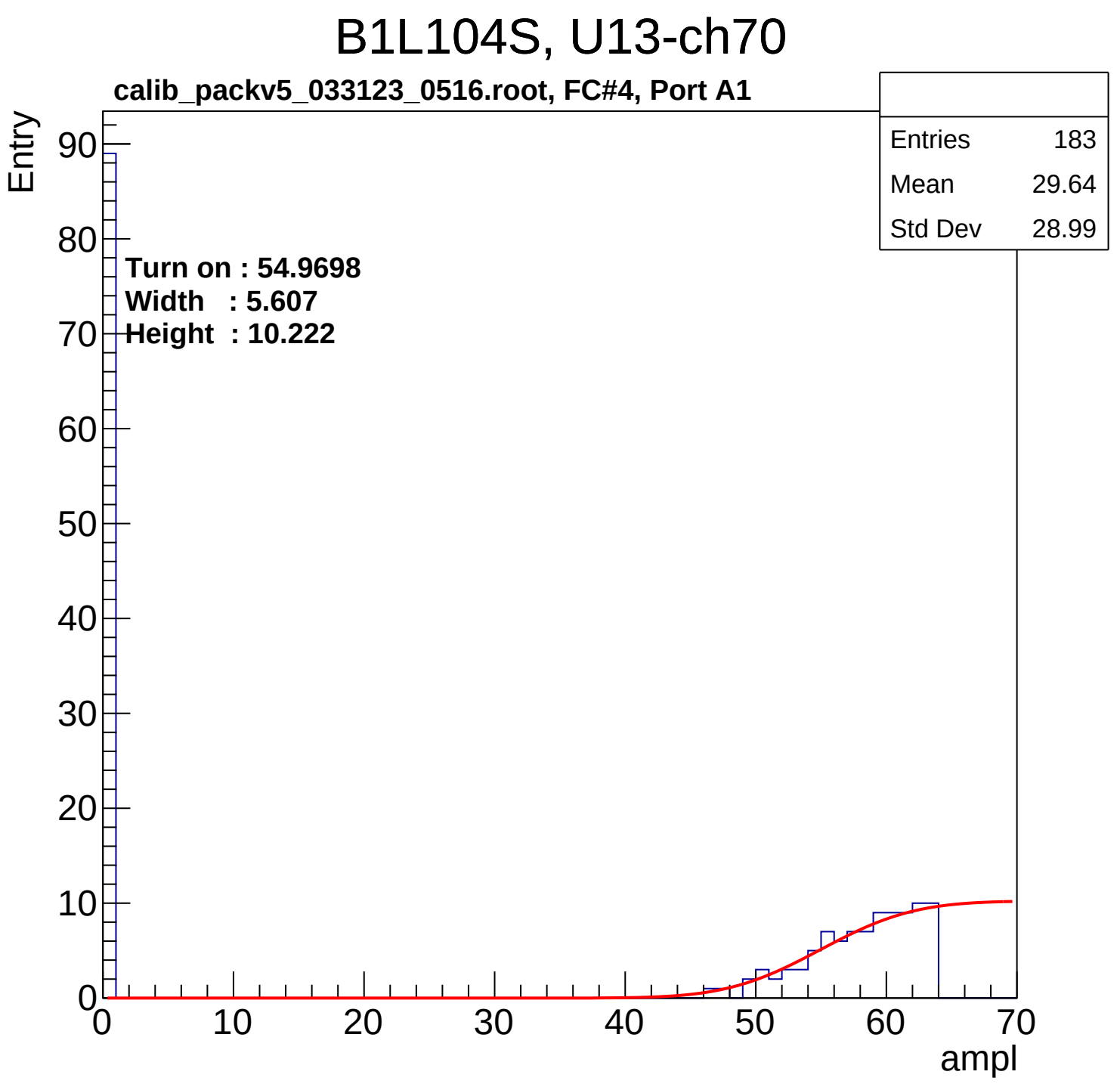
B1L104S, U13-ch70
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 183
Mean 29.64
Std Dev 28.99
Turn on : 54.9698
Width : 5.607
Height : 10.222
Entry
ampl
0
10
20
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40
50
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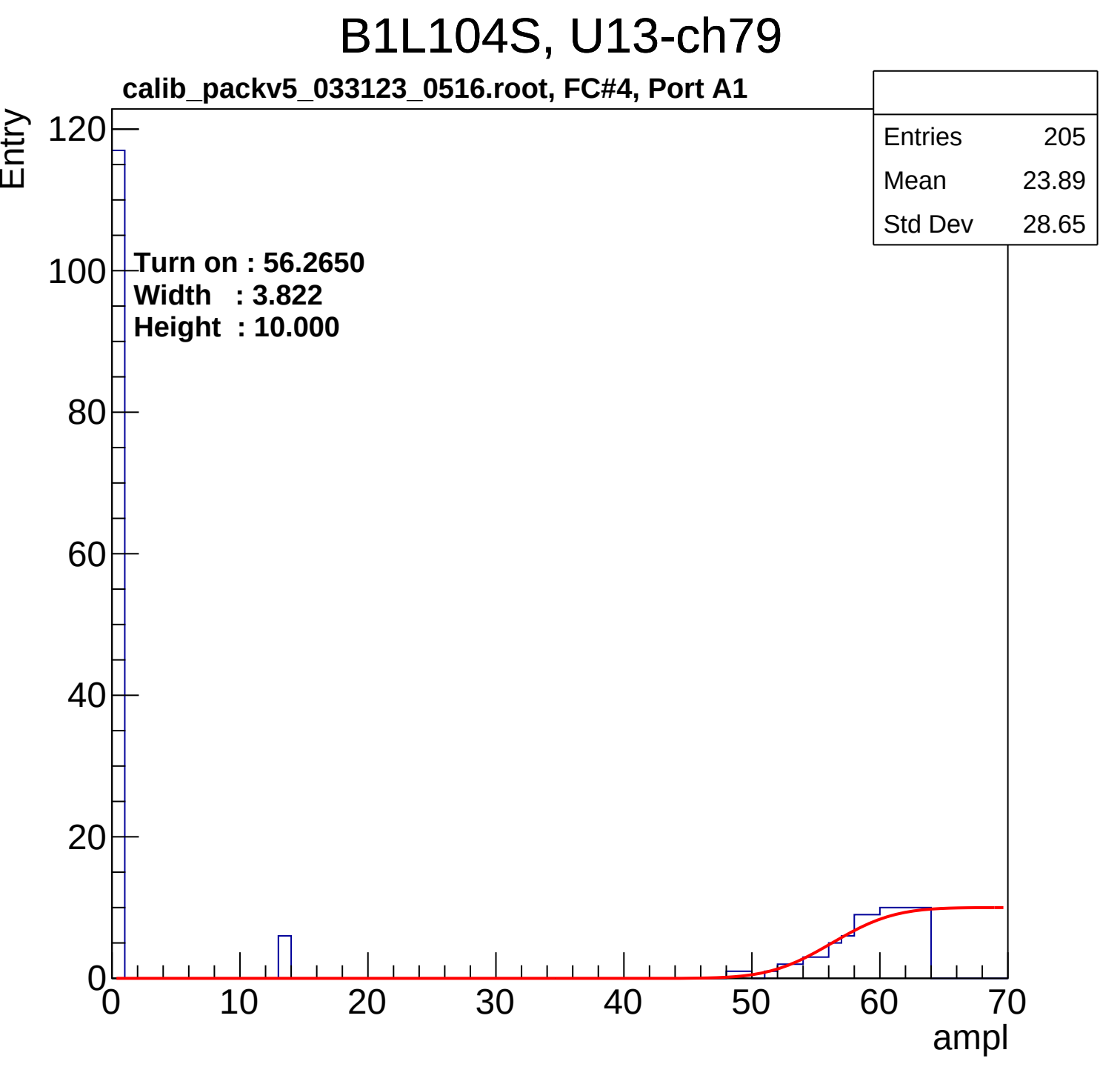
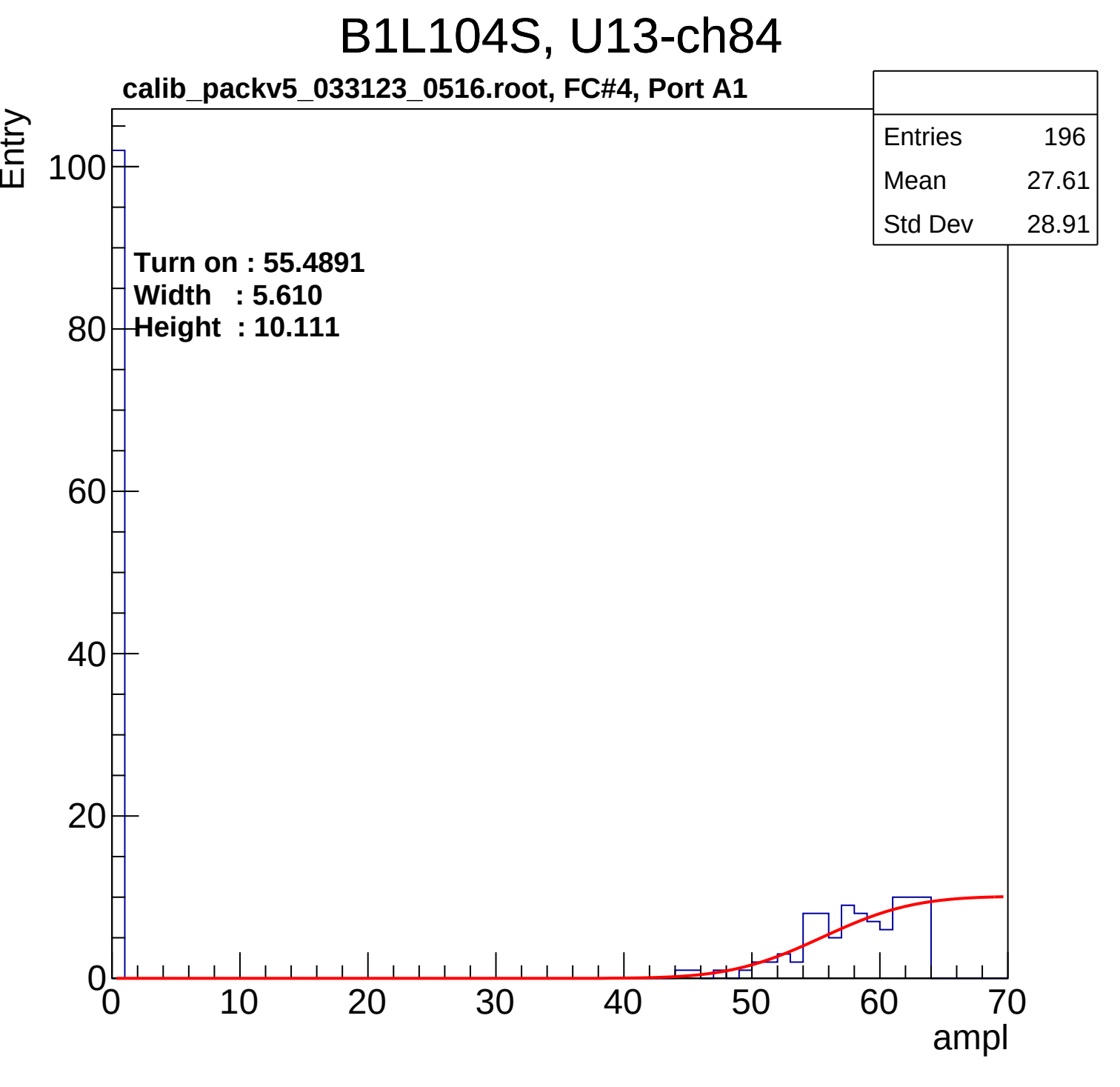
80
90


B1L104S, U13-ch79
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 205
Mean 23.89
Std Dev 28.65
Turn on : 56.2650
Width : 3.822
Height : 10.000
Entry
120
100
80
60
40
20
0
0
10
20
30
40
50
60
70
ampl


B1L104S, U13-ch84
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 196
Mean 27.61
Std Dev 28.91
Turn on : 55.4891
Width : 5.610
Height : 10.111
Entry
ampl
0
20
40
60
80
100
0
10
20
30
40
50
60
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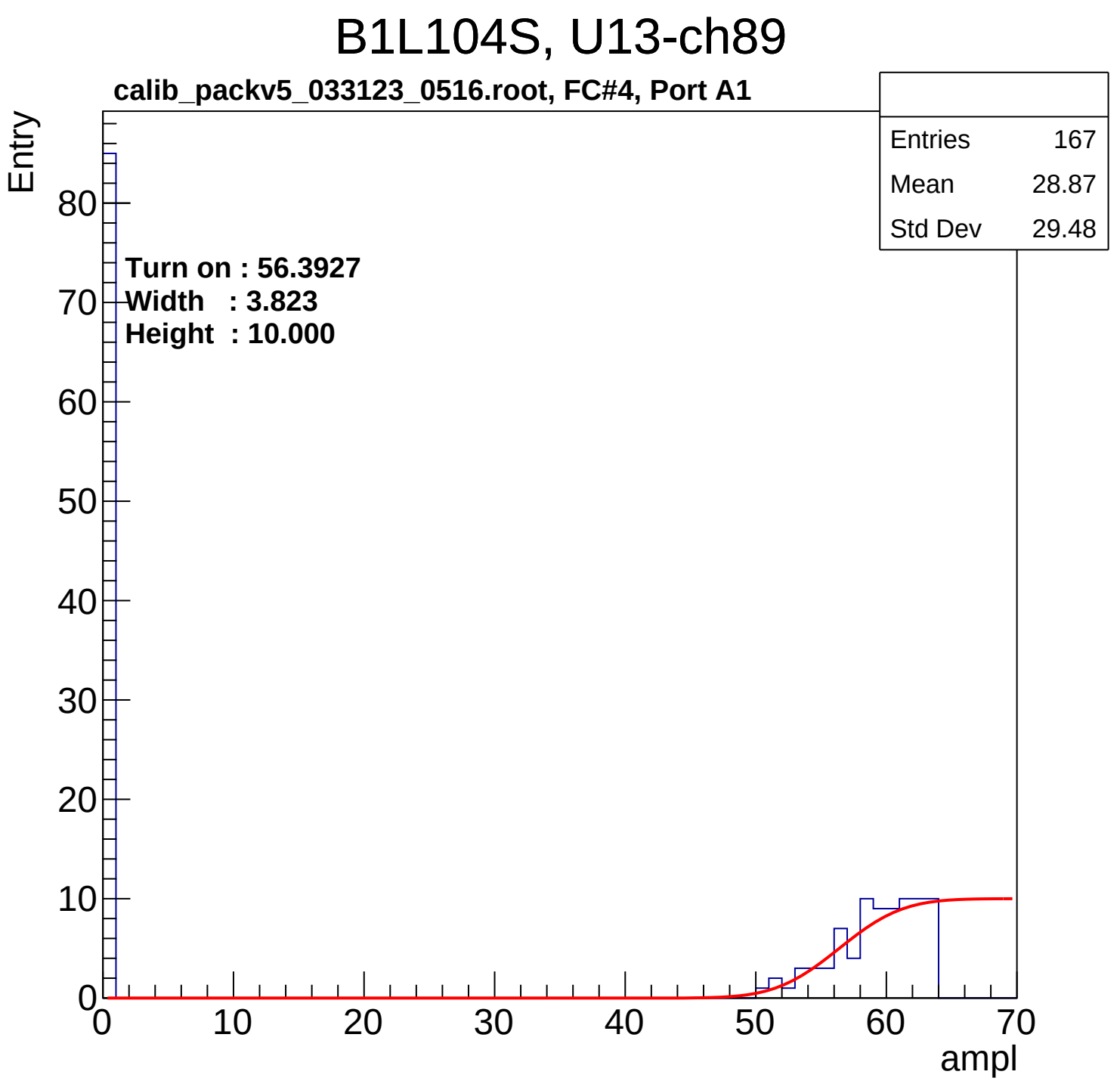
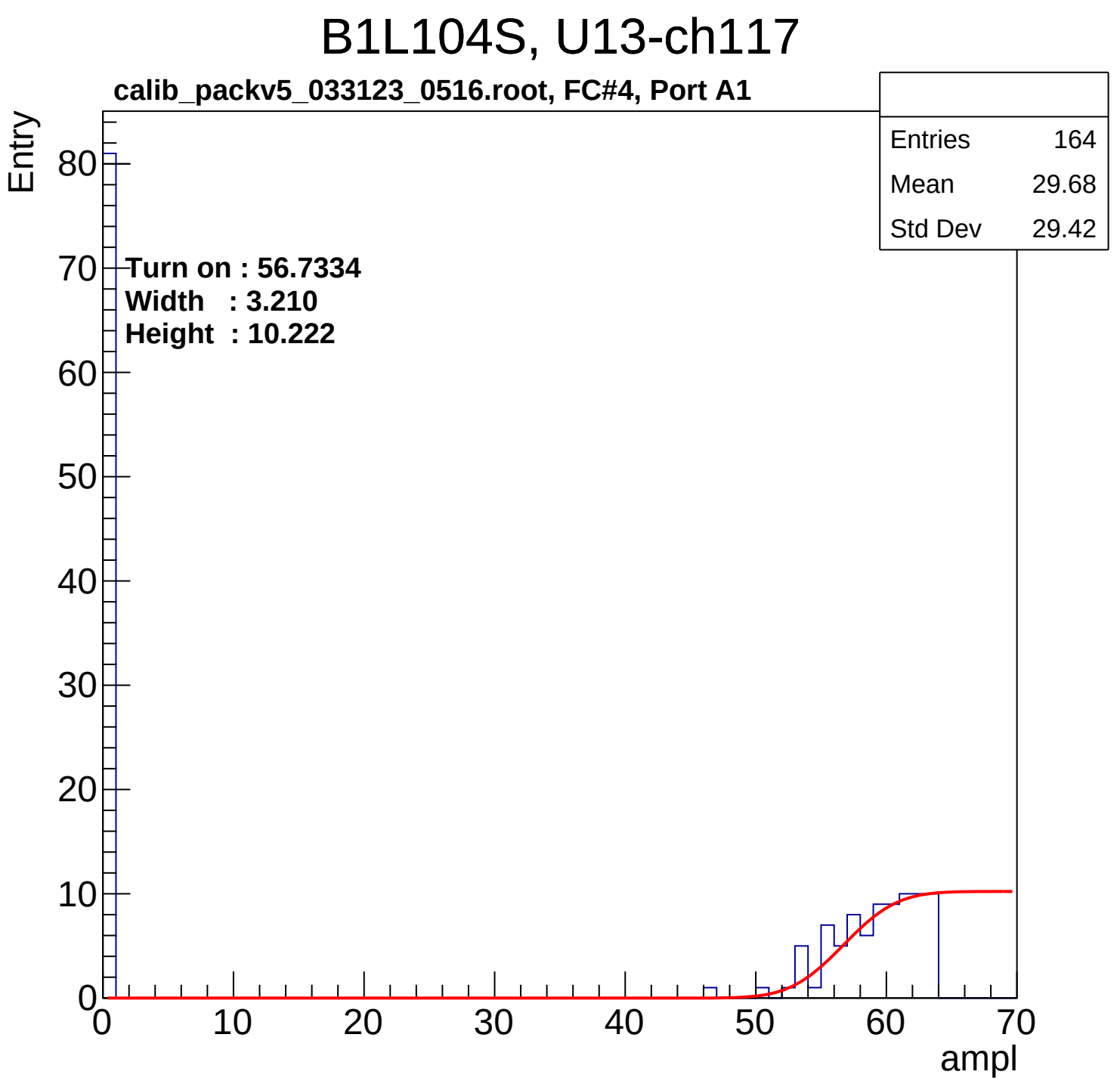
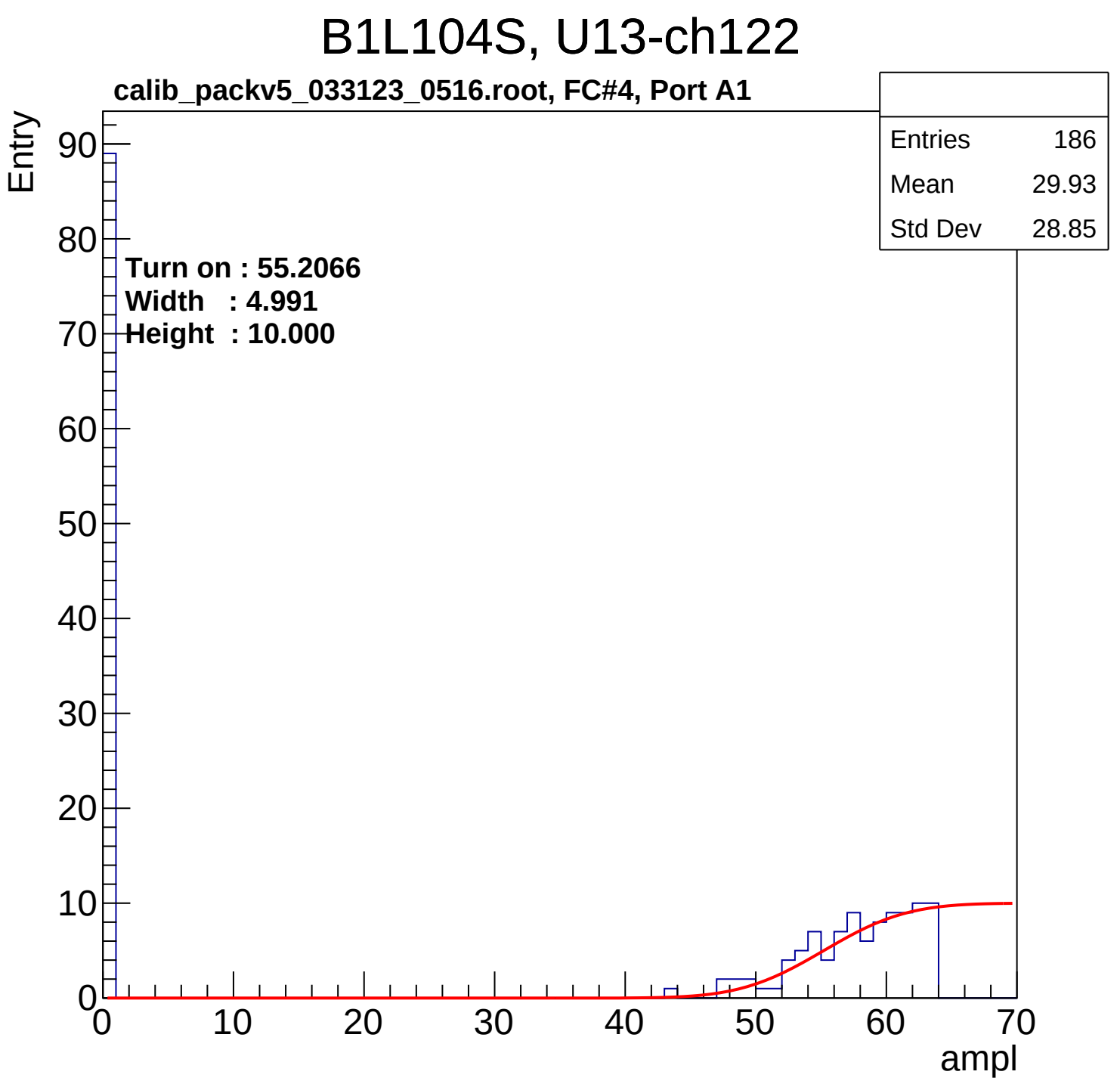
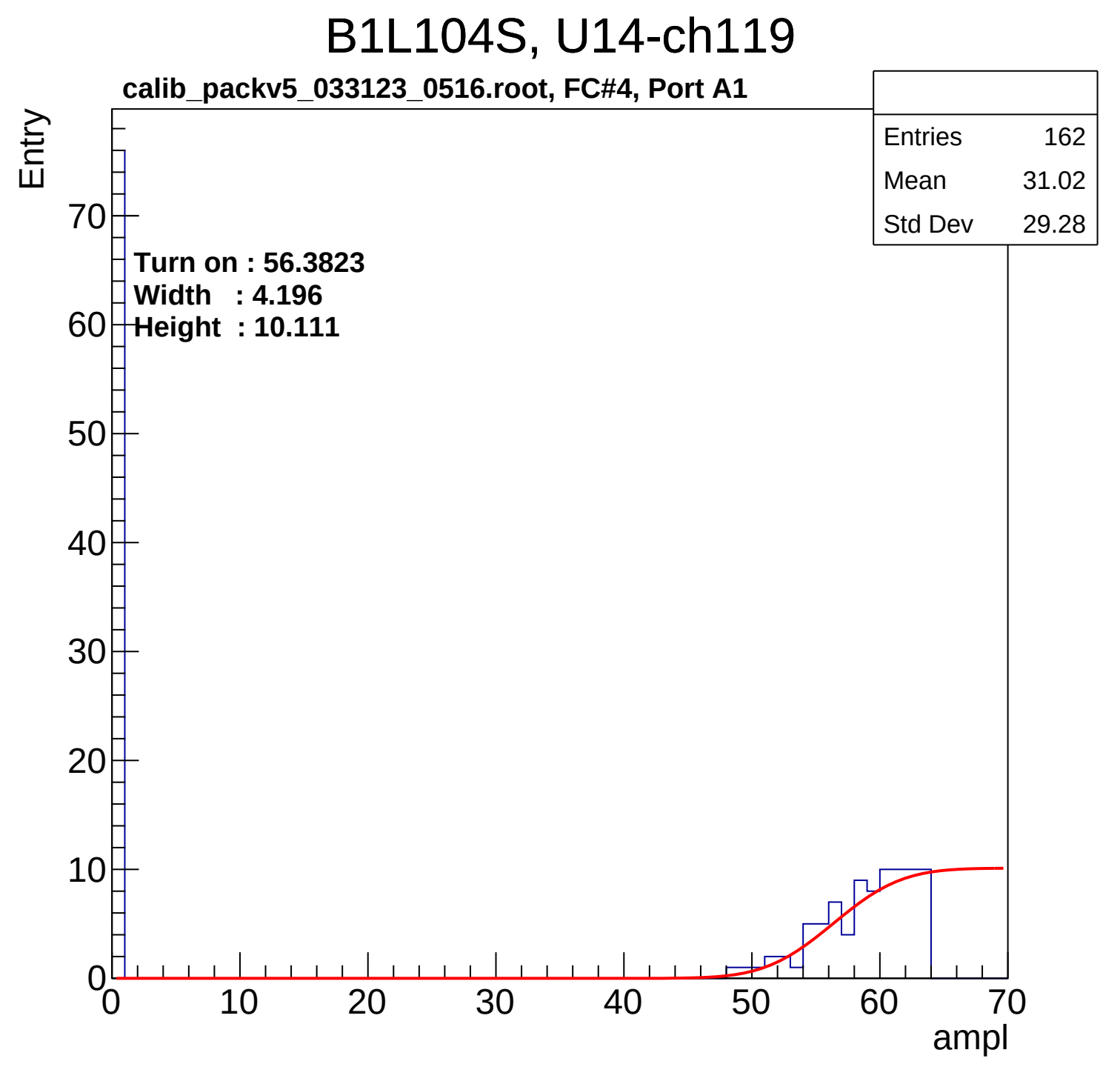
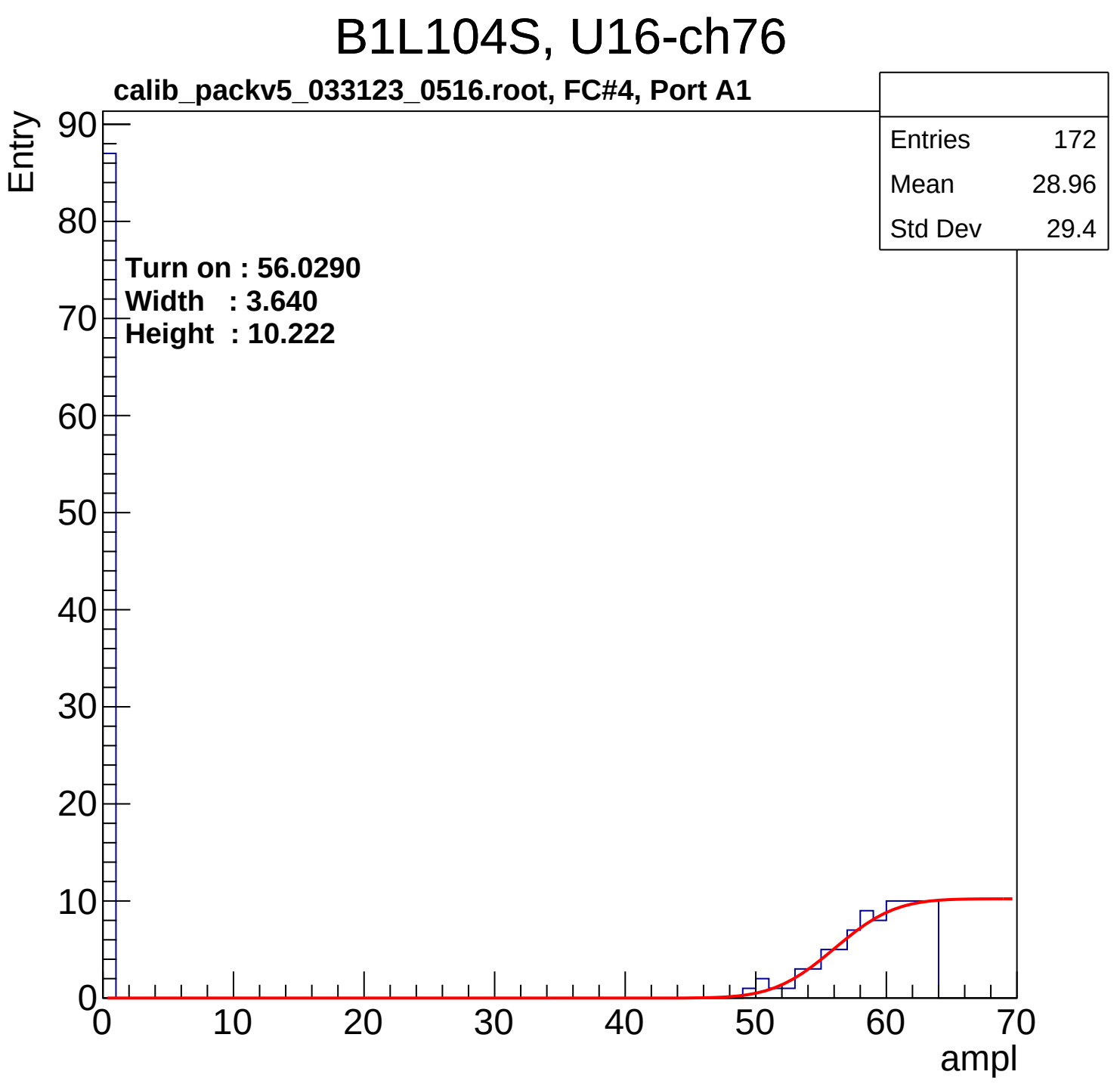

B1L104S, U13-ch89
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 167
Mean 28.87
Std Dev 29.48
Turn on : 56.3927
Width : 3.823
Height : 10.000
Entry
ampl
0
10
20
30
40
50
60
70
80


B1L104S, U13-ch117
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 164
Mean 29.68
Std Dev 29.42
Turn on : 56.7334
Width : 3.210
Height : 10.222
Entry
ampl
0
10
20
30
40
50
60
70
80


B1L104S, U13-ch122
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 186
Mean 29.93
Std Dev 28.85
Turn on : 55.2066
Width : 4.991
Height : 10.000
Entry
ampl
0
10
20
30
40
50
60
70
80
90


B1L104S, U14-ch119
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 162
Mean 31.02
Std Dev 29.28
Turn on : 56.3823
Width : 4.196
Height : 10.111
Entry
ampl
0
10
20
30
40
50
60
70


B1L104S, U16-ch76
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 172
Mean 28.96
Std Dev 29.4
Turn on : 56.0290
Width : 3.640
Height : 10.222
Entry
ampl
0
10
20
30
40
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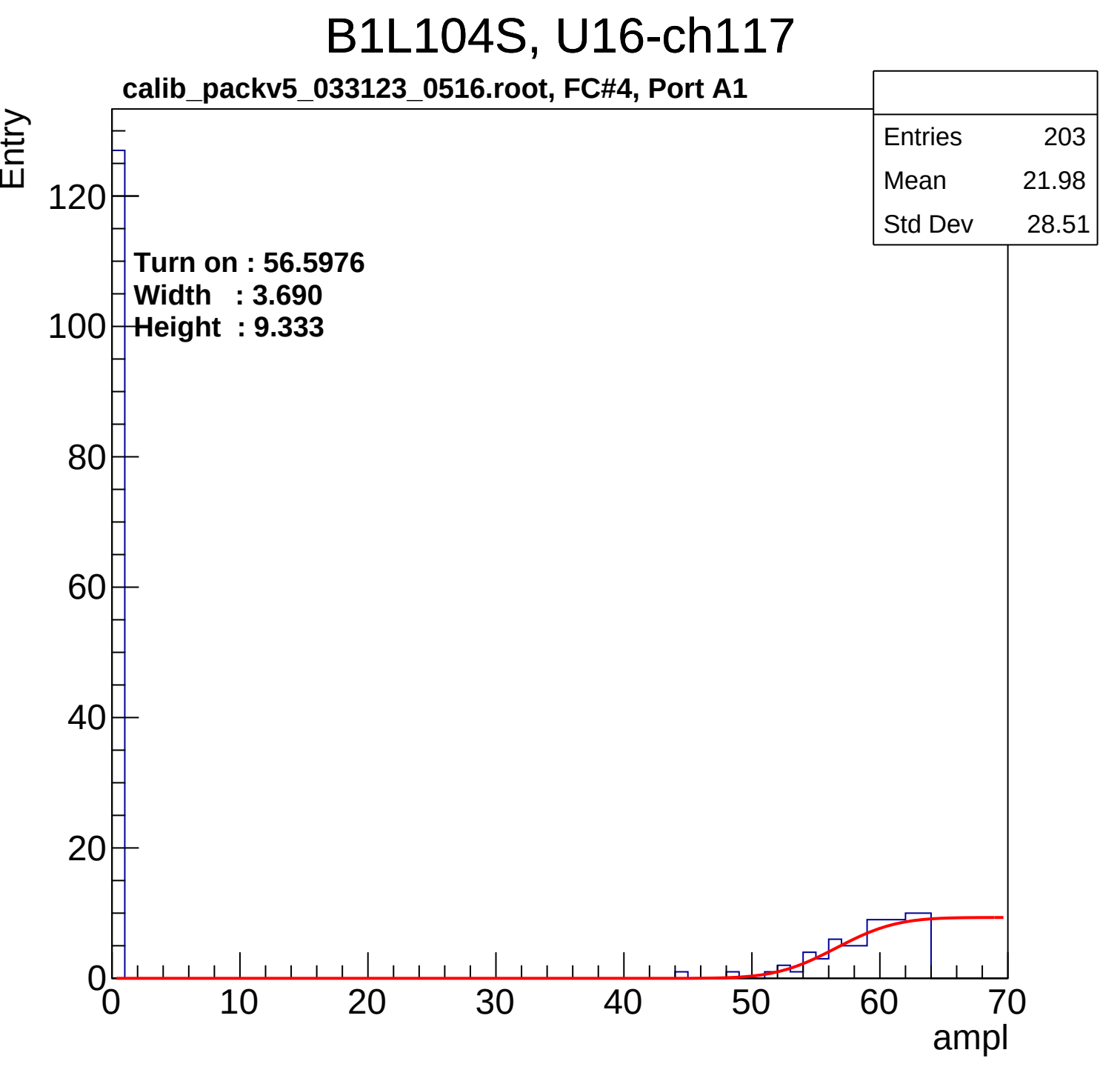
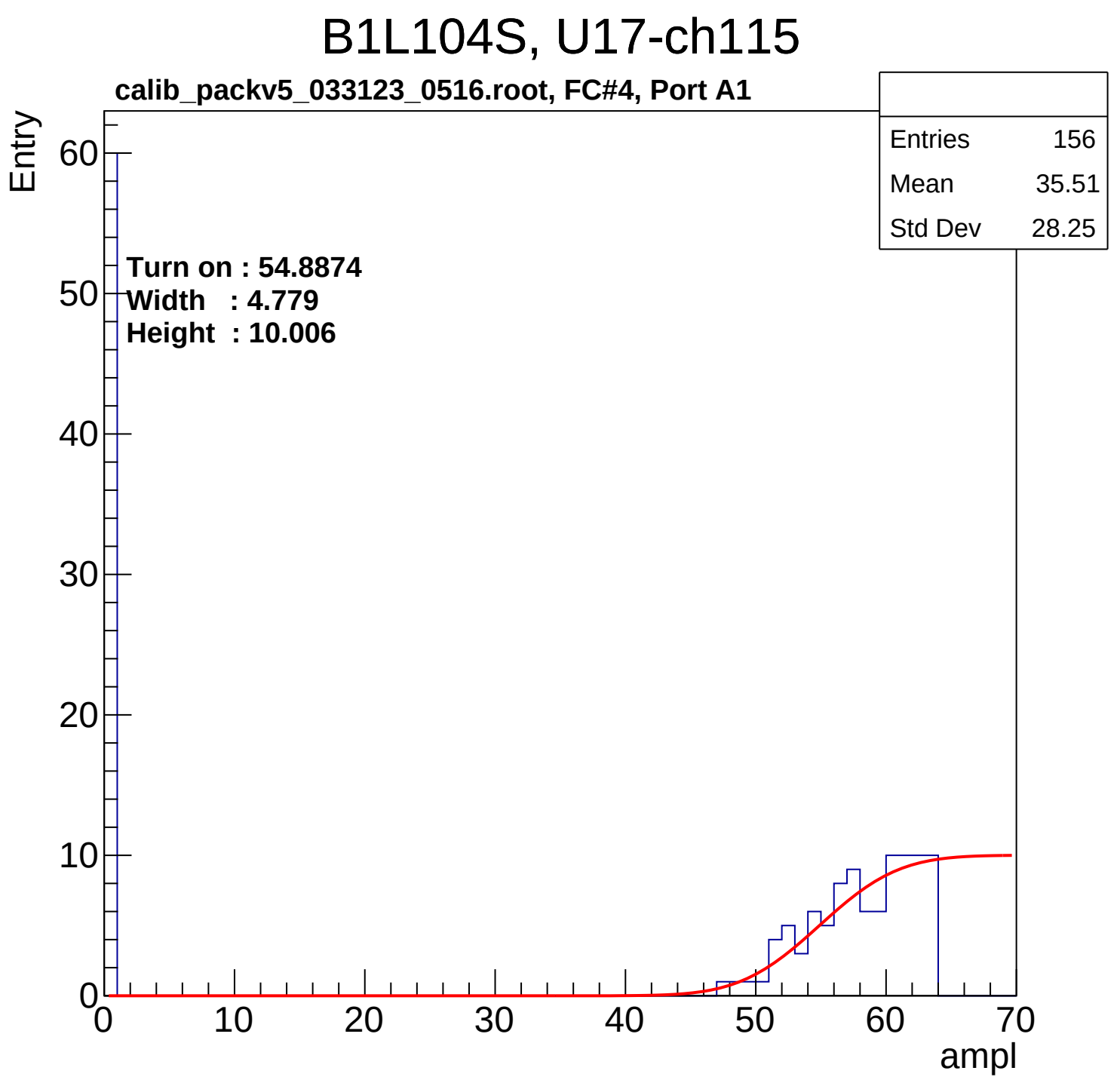
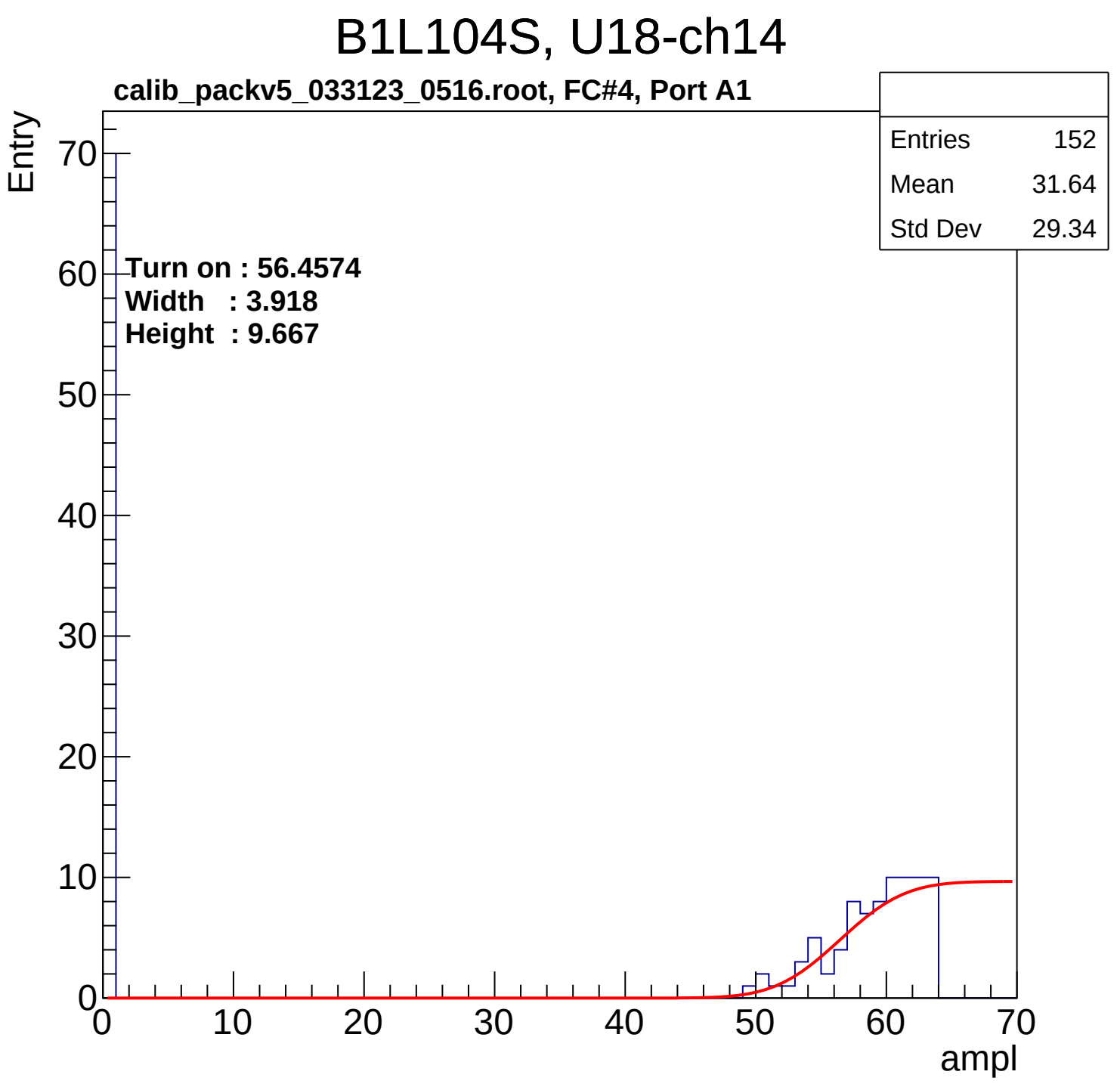
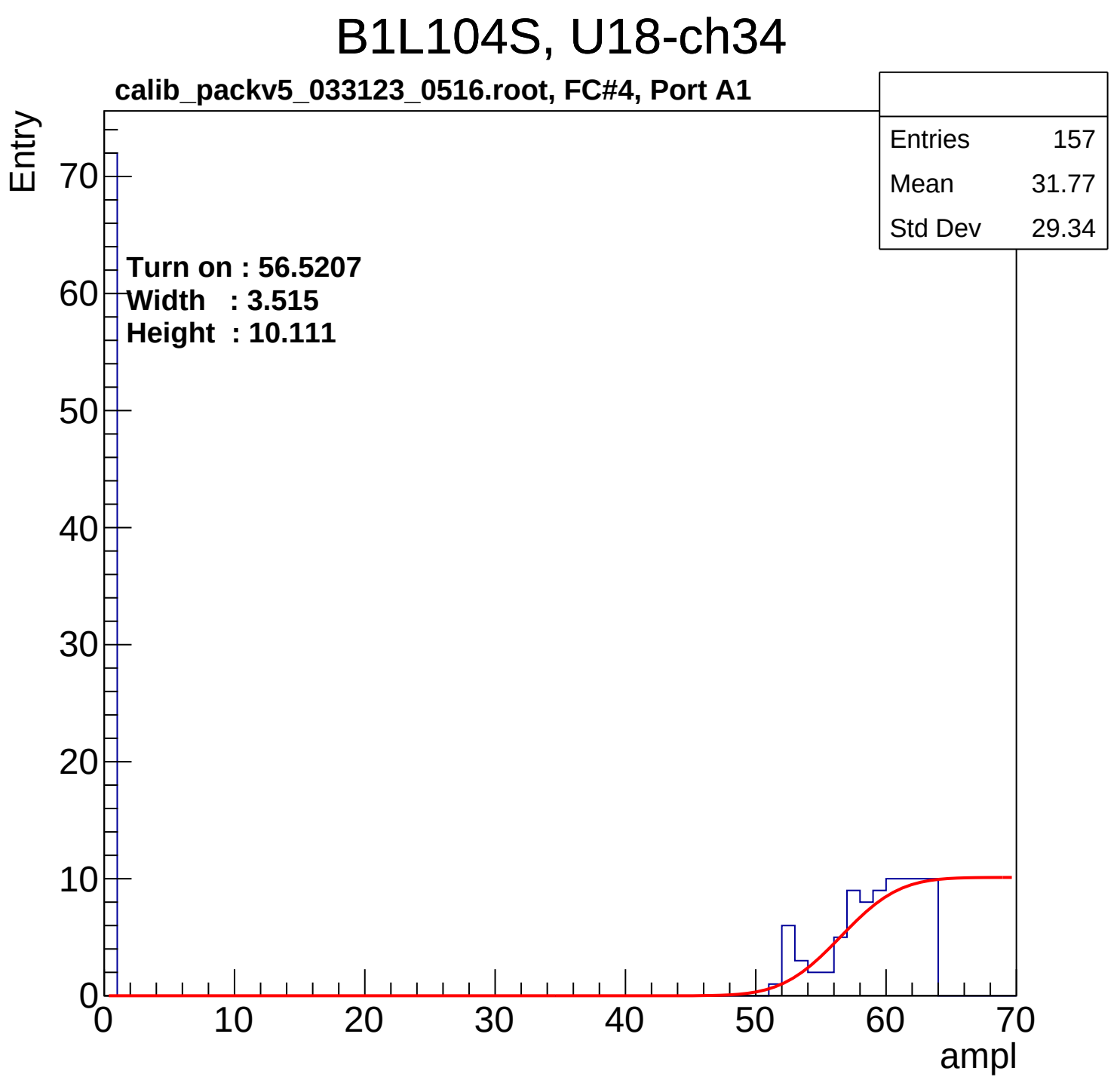
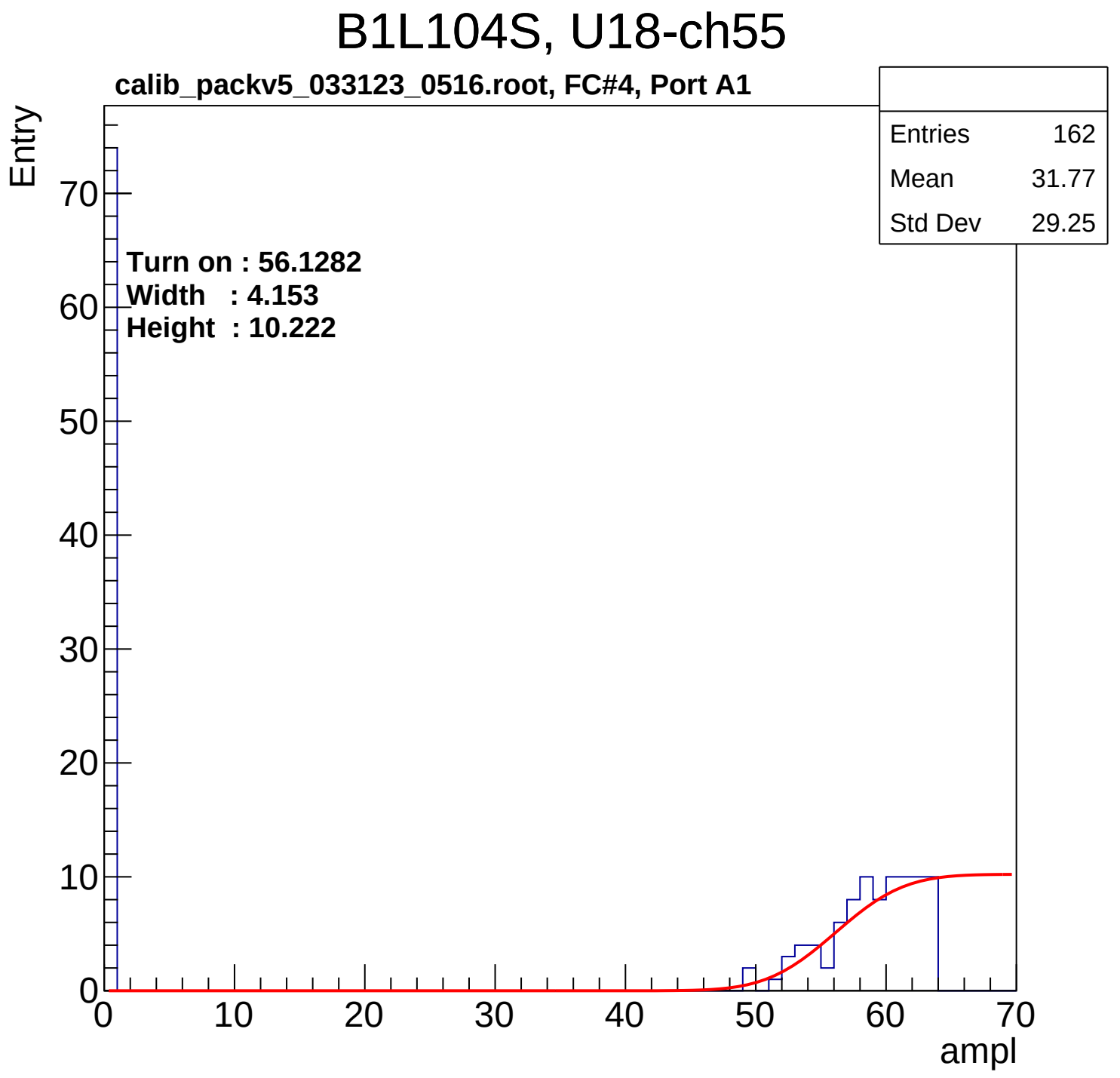
60
70
80
90

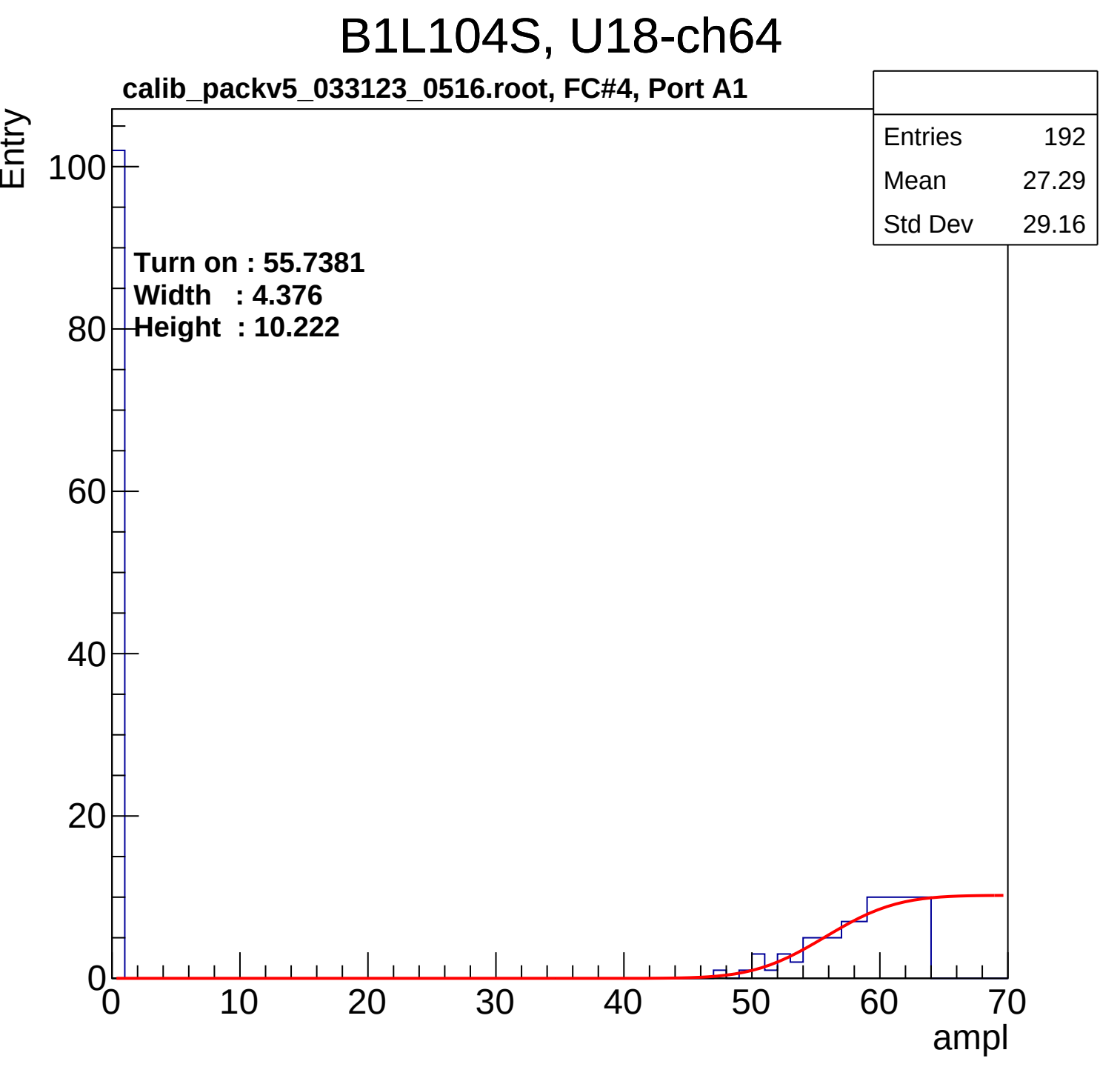

B1L104S, U16-ch117
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 203
Mean 21.98
Std Dev 28.51
Turn on : 56.5976
Width : 3.690
Height : 9.333
Entry
ampl
0
20
40
60
80
100
120
0
10
20
30
40
50
60
70


B1L104S, U17-ch115
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 156
Mean 35.51
Std Dev 28.25
Turn on : 54.8874
Width : 4.779
Height : 10.006
Entry
ampl
0
10
20
30
40
50
60
70


B1L104S, U18-ch14
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 152
Mean 31.64
Std Dev 29.34
Turn on : 56.4574
Width : 3.918
Height : 9.667
Entry
ampl
0
10
20
30
40
50
60
70


B1L104S, U18-ch34
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 157
Mean 31.77
Std Dev 29.34
Turn on : 56.5207
Width : 3.515
Height : 10.111
Entry
ampl
0
10
20
30
40
50
60
70


B1L104S, U18-ch55
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 162
Mean 31.77
Std Dev 29.25
Turn on : 56.1282
Width : 4.153
Height : 10.222
Entry
ampl
0
10
20
30
40
50
60
70


B1L104S, U18-ch64
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 192
Mean 27.29
Std Dev 29.16
Turn on : 55.7381
Width : 4.376
Height : 10.222
Entry
ampl
0
20
40
60
80
100
0
10
20
30
40
50
60
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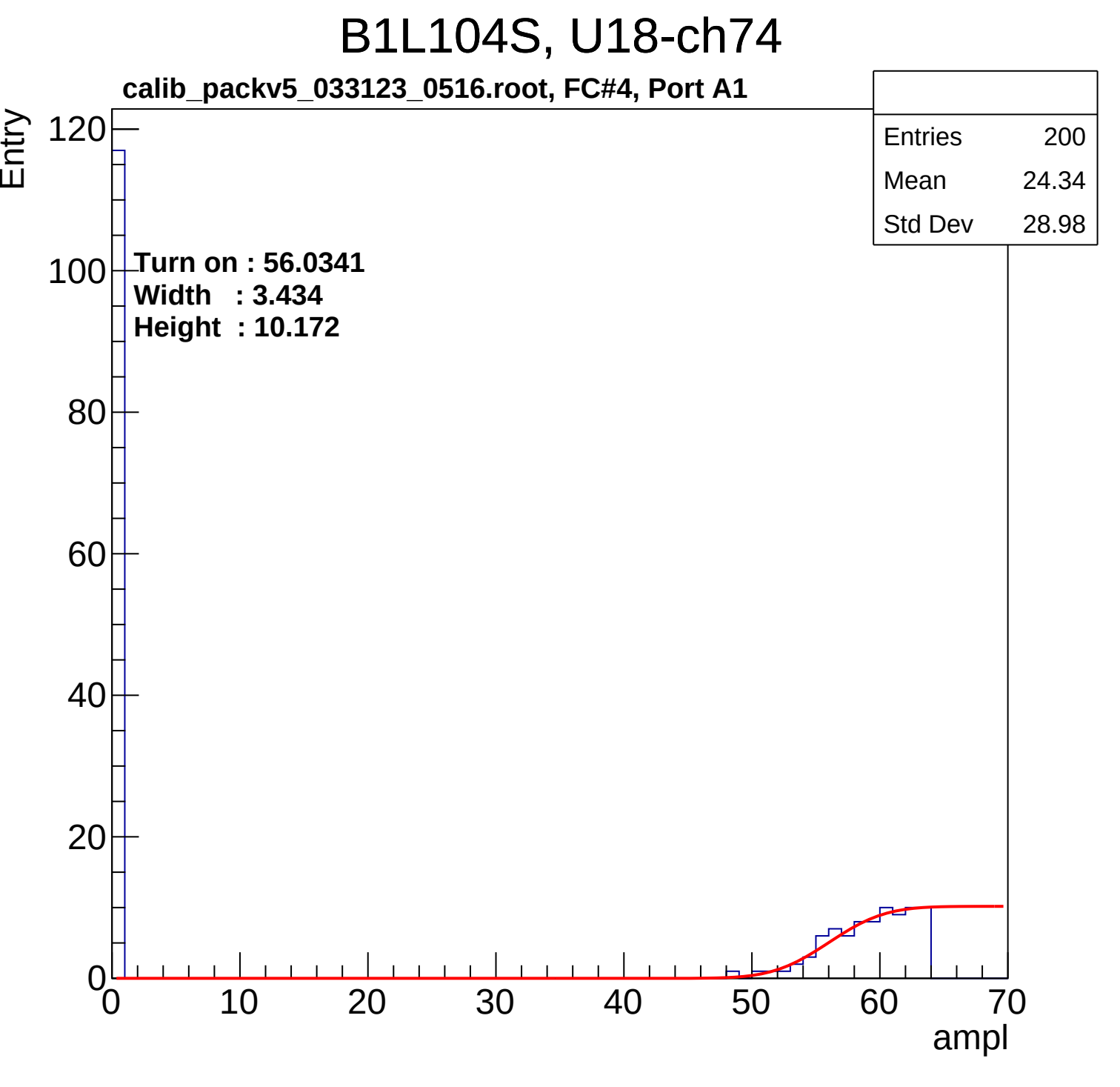
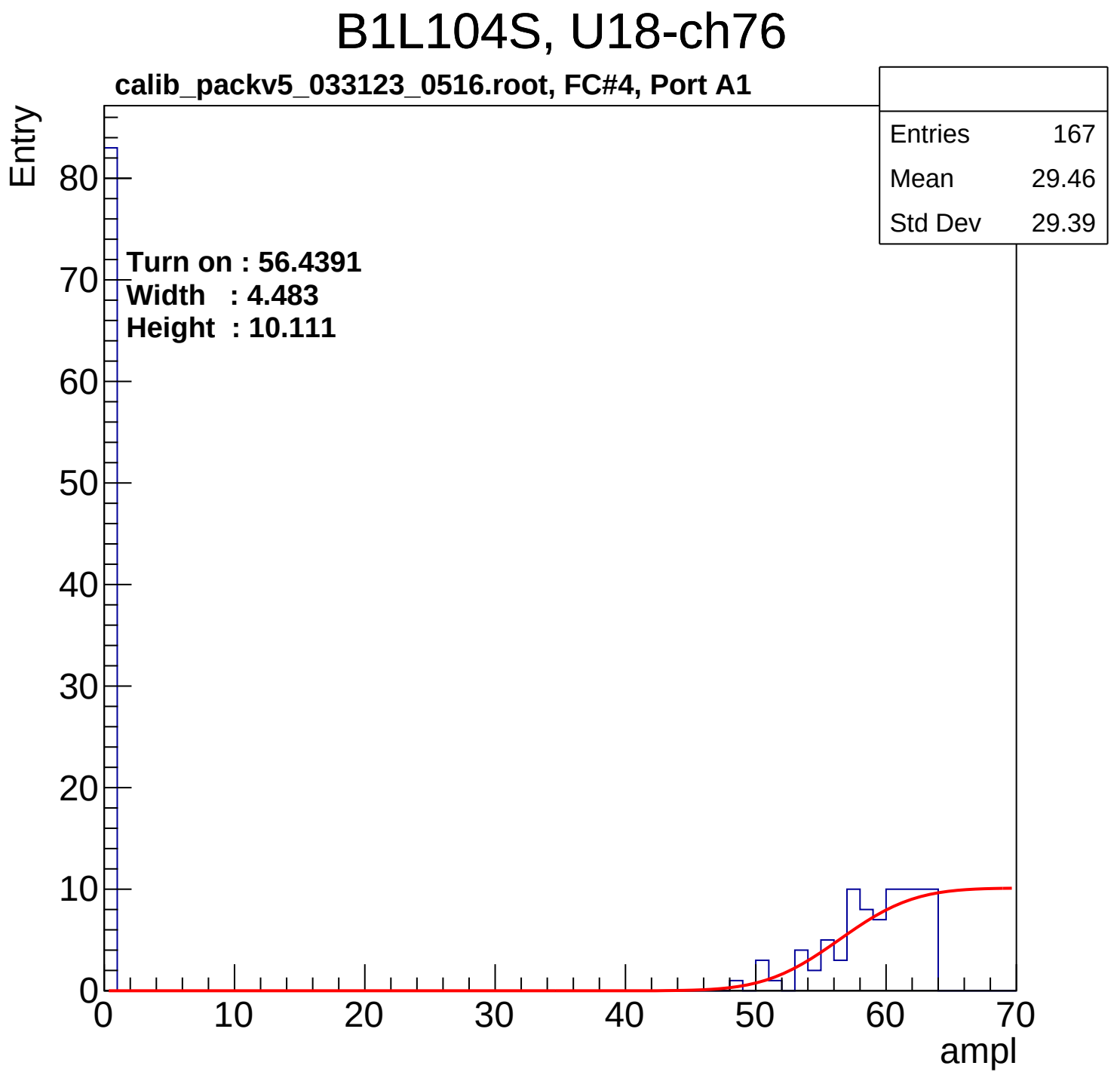
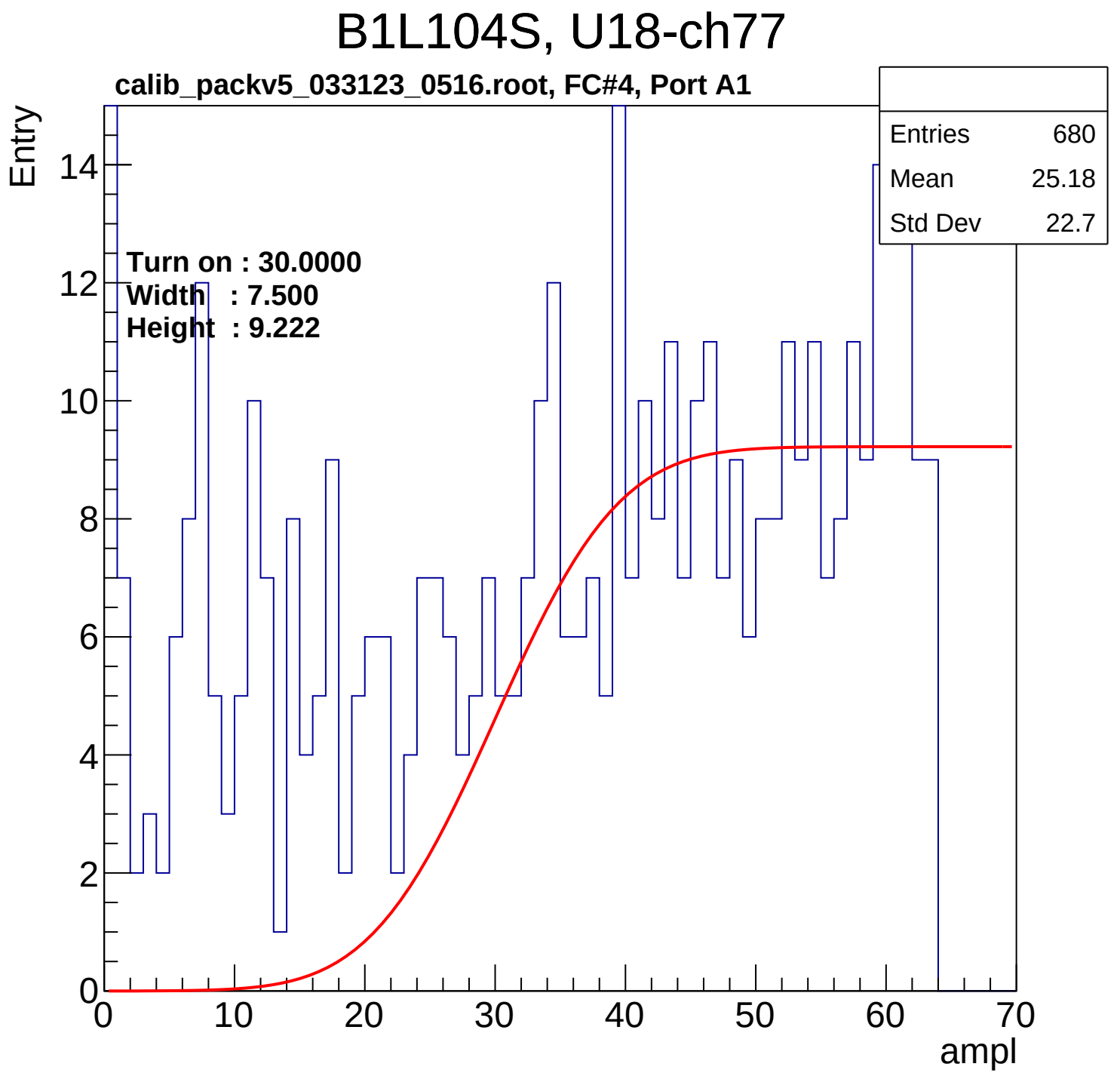

B1L104S, U18-ch74
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 200
Mean 24.34
Std Dev 28.98
Turn on : 56.0341
Width : 3.434
Height : 10.172
Entry
ampl
0
20
40
60
80
100
120
0
10
20
30
40
50
60
70


B1L104S, U18-ch76
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 167
Mean 29.46
Std Dev 29.39
Turn on : 56.4391
Width : 4.483
Height : 10.111
Entry
ampl
0
10
20
30
40
50
60
70
80


B1L104S, U18-ch77
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 680
Mean 25.18
Std Dev 22.7
Turn on : 30.0000
Width : 7.500
Height : 9.222
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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40
50
60
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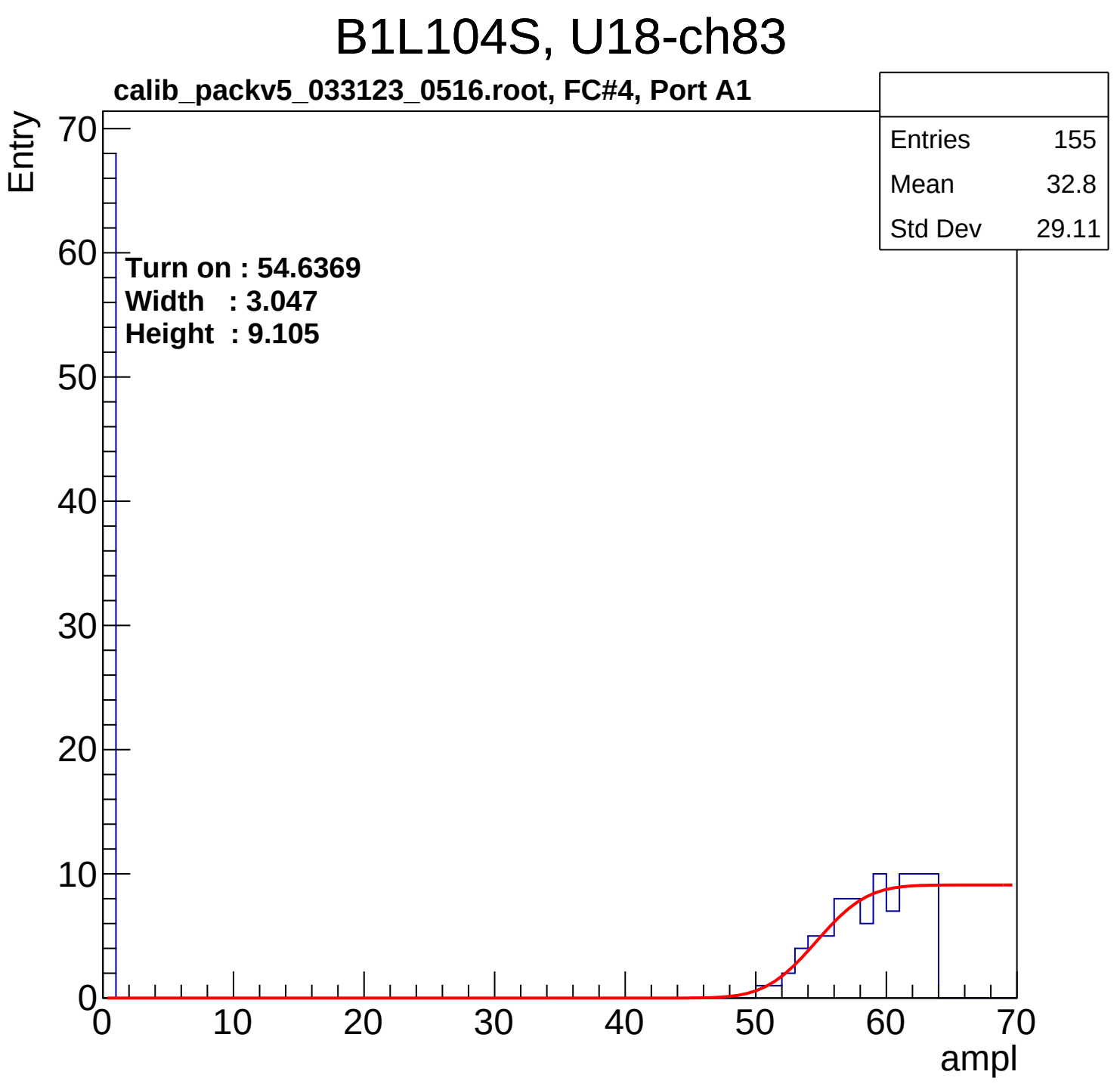
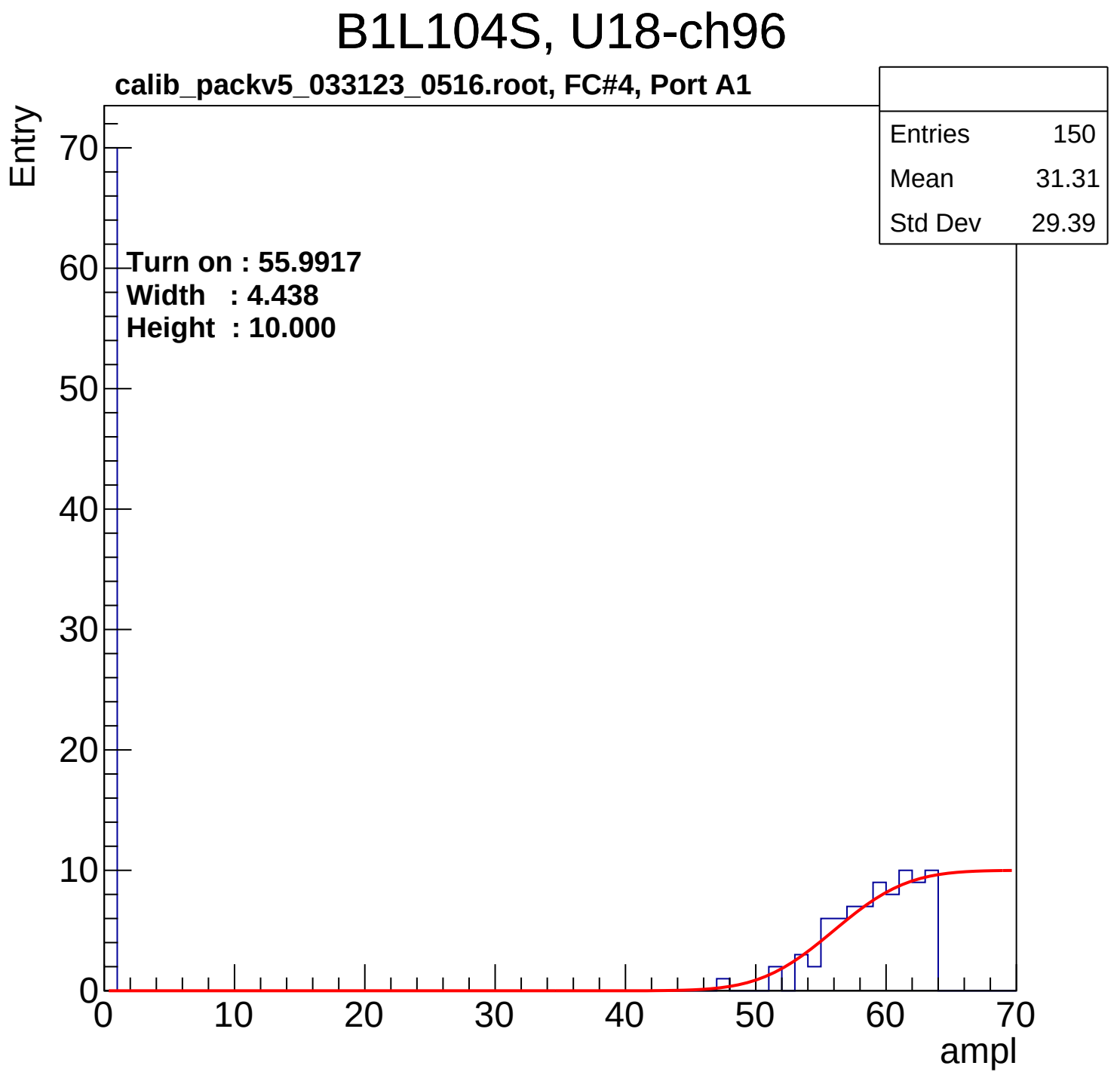
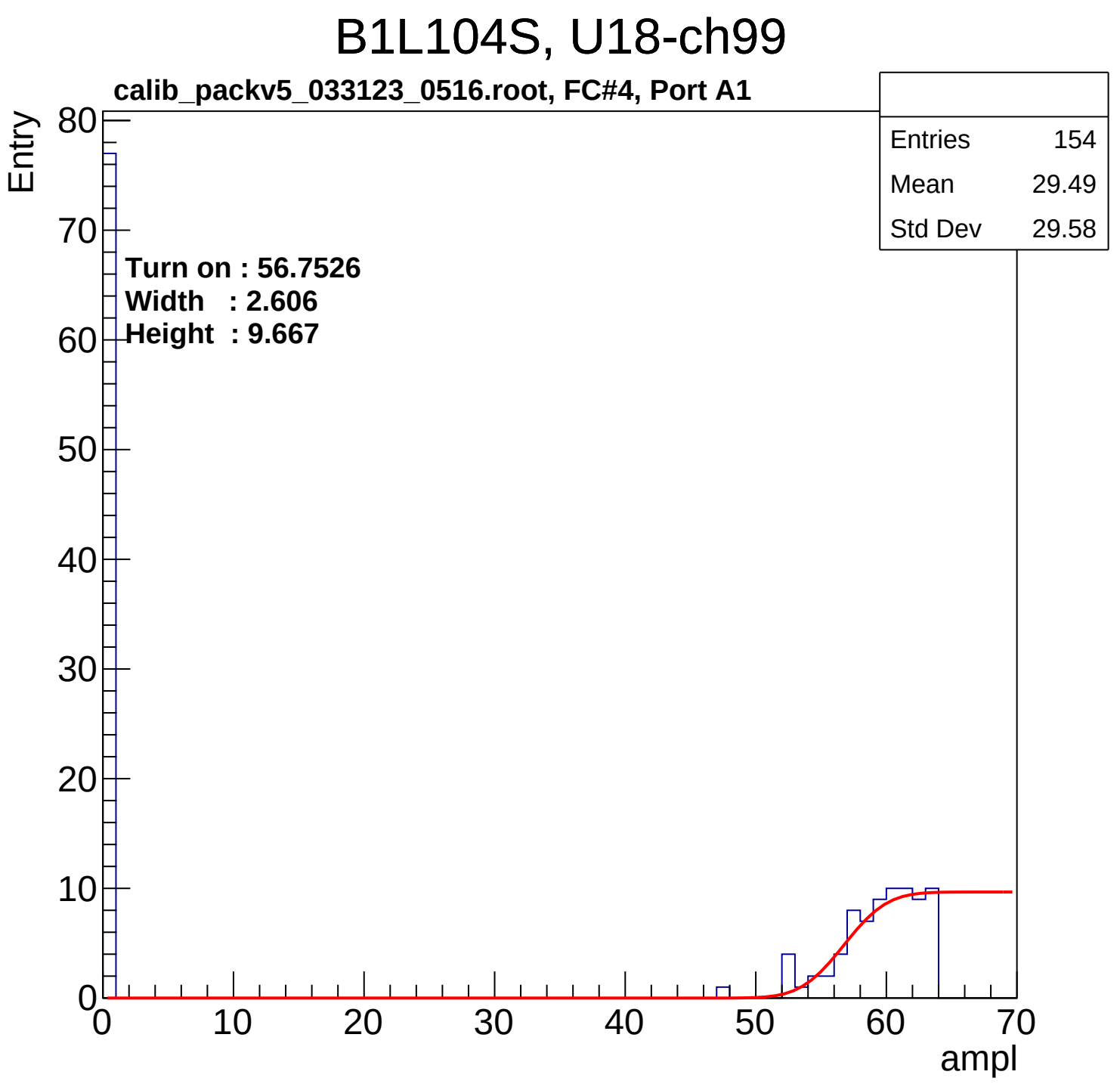

B1L104S, U18-ch83
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 155
Mean 32.8
Std Dev 29.11
Turn on : 54.6369
Width : 3.047
Height : 9.105
Entry
ampl
0
10
20
30
40
50
60
70


B1L104S, U18-ch96
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 150
Mean 31.31
Std Dev 29.39
Turn on : 55.9917
Width : 4.438
Height : 10.000
Entry
ampl
0
10
20
30
40
50
60
70


B1L104S, U18-ch99
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 154
Mean 29.49
Std Dev 29.58
Turn on : 56.7526
Width : 2.606
Height : 9.667
Entry
ampl
0
10
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30
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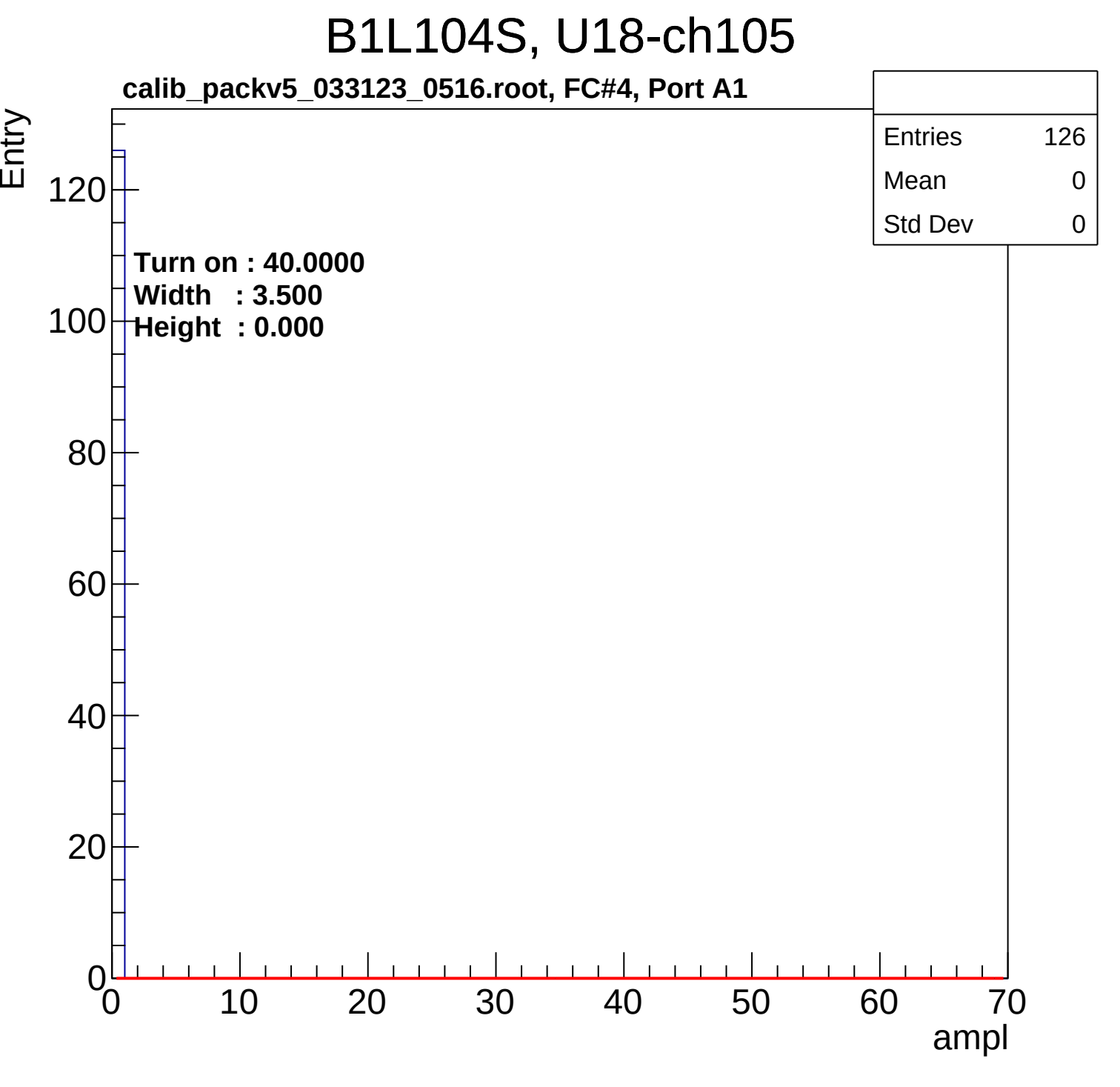
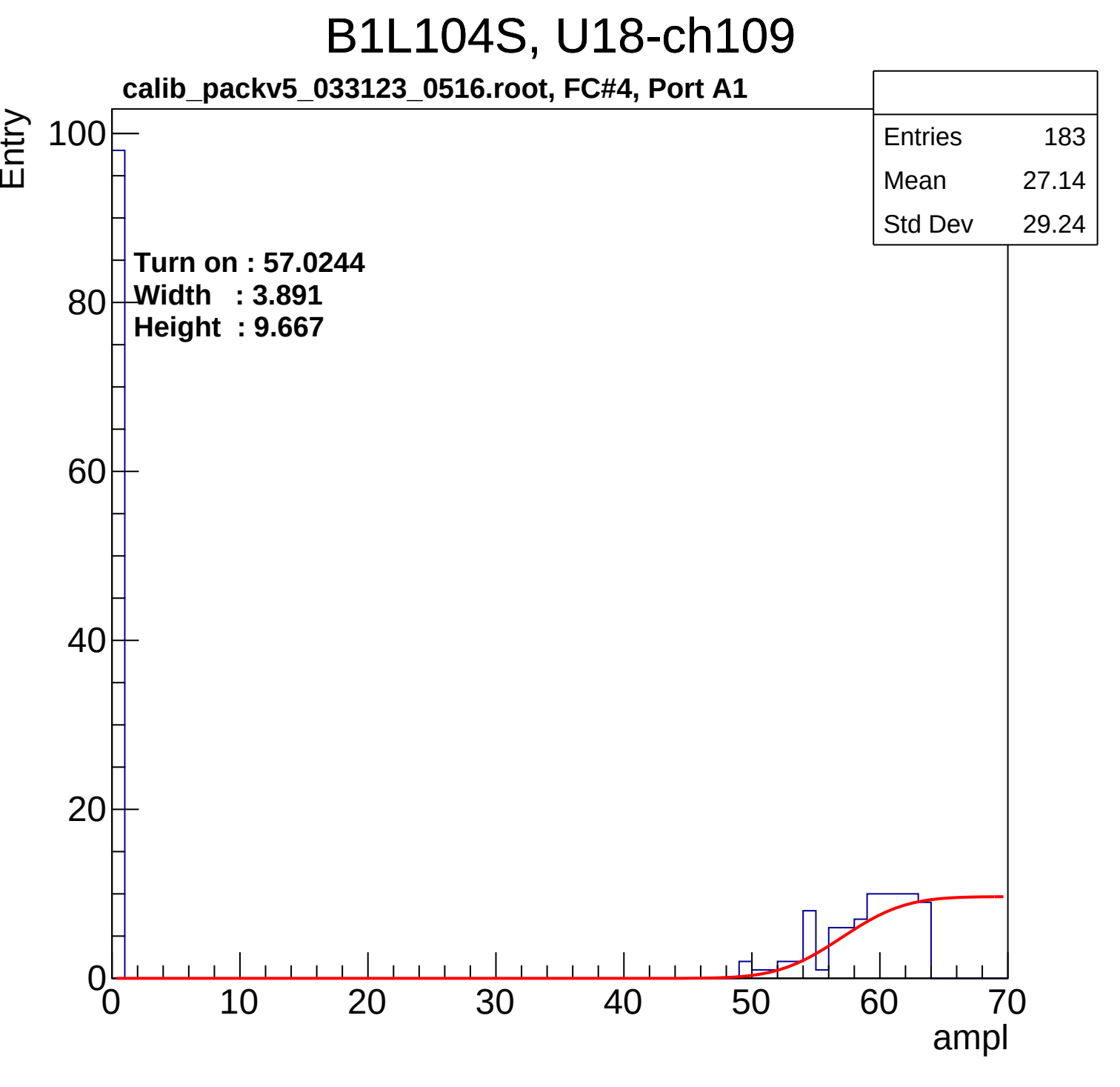
50
60
70
80


B1L104S, U18-ch105
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 126
Mean 0
Std Dev 0
Turn on : 40.0000
Width : 3.500
Height : 0.000
Entry
0
20
40
60
80
100
120
0
10
20
30
40
50
60
70
ampl


B1L104S, U18-ch109
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 183
Mean 27.14
Std Dev 29.24
Turn on : 57.0244
Width : 3.891
Height : 9.667
Entry
ampl
0
20
40
60
80
100
0
10
20
30
40
50
60
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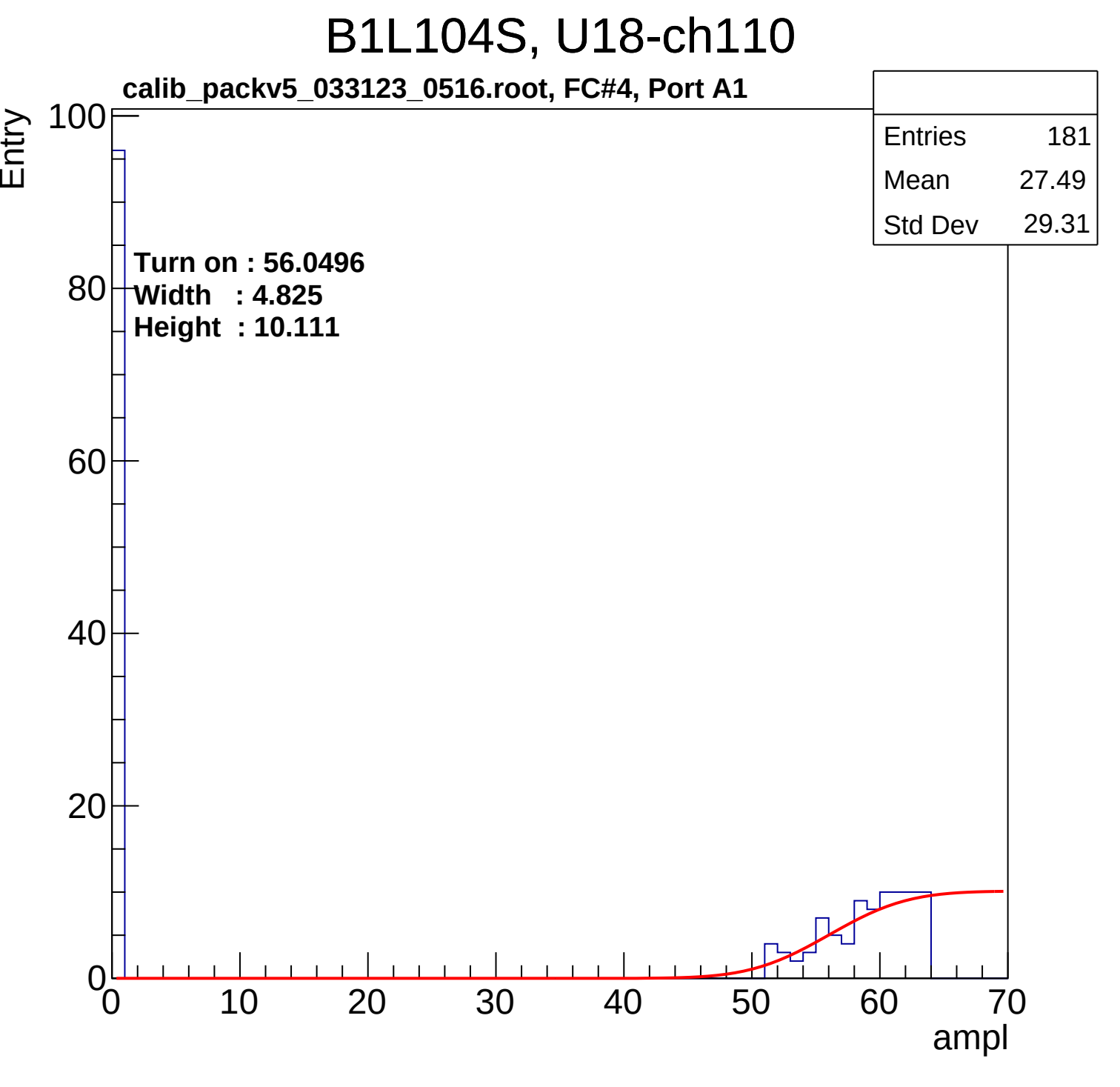
B1L104S, U18-ch110
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 181
Mean 27.49
Std Dev 29.31
Turn on : 56.0496
Width : 4.825
Height : 10.111
Entry
ampl
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100
0
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20
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40
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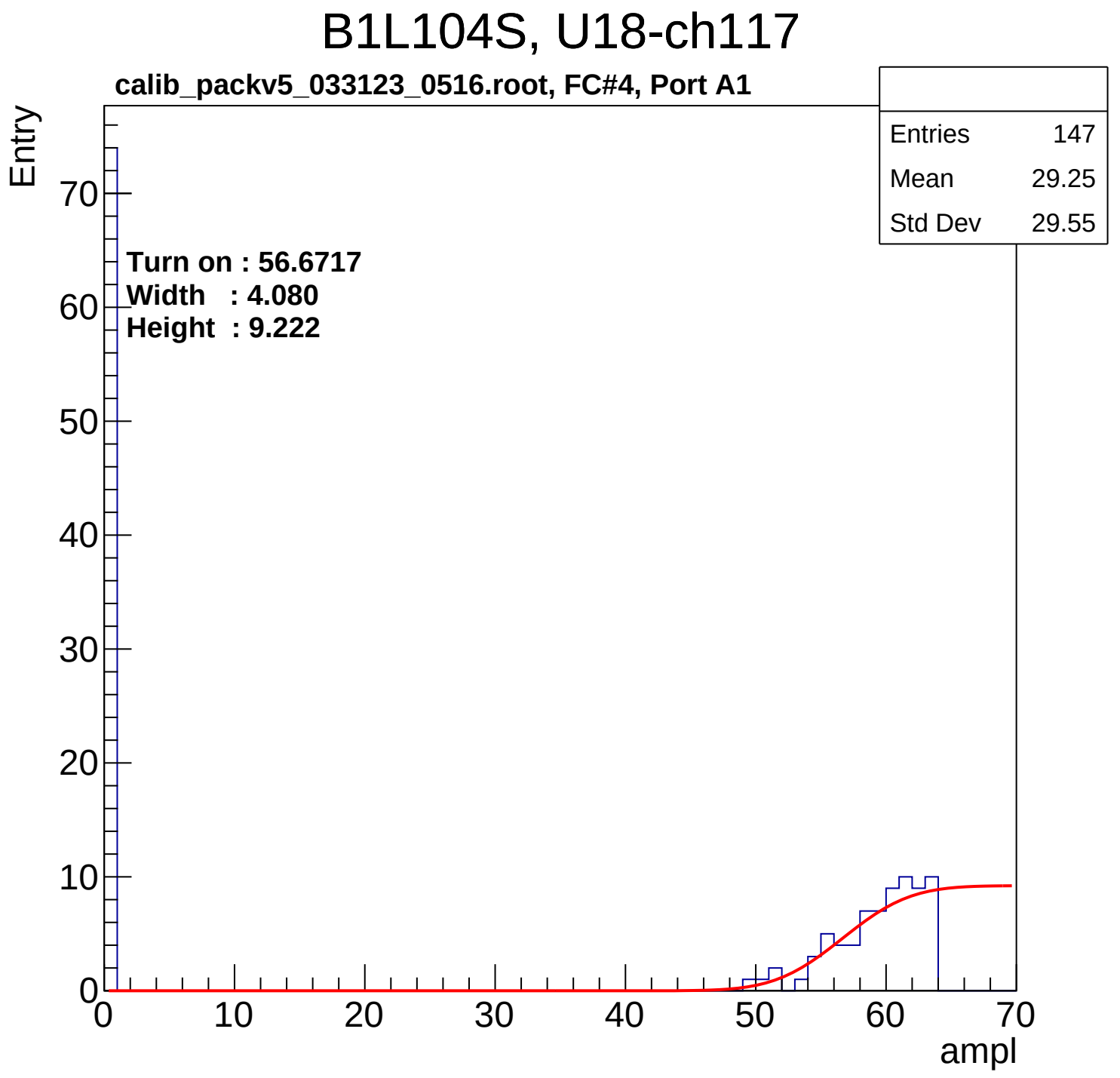
B1L104S, U18-ch117
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 147
Mean 29.25
Std Dev 29.55
Turn on : 56.6717
Width : 4.080
Height : 9.222
Entry
ampl
0
10
20
30
40
50
60
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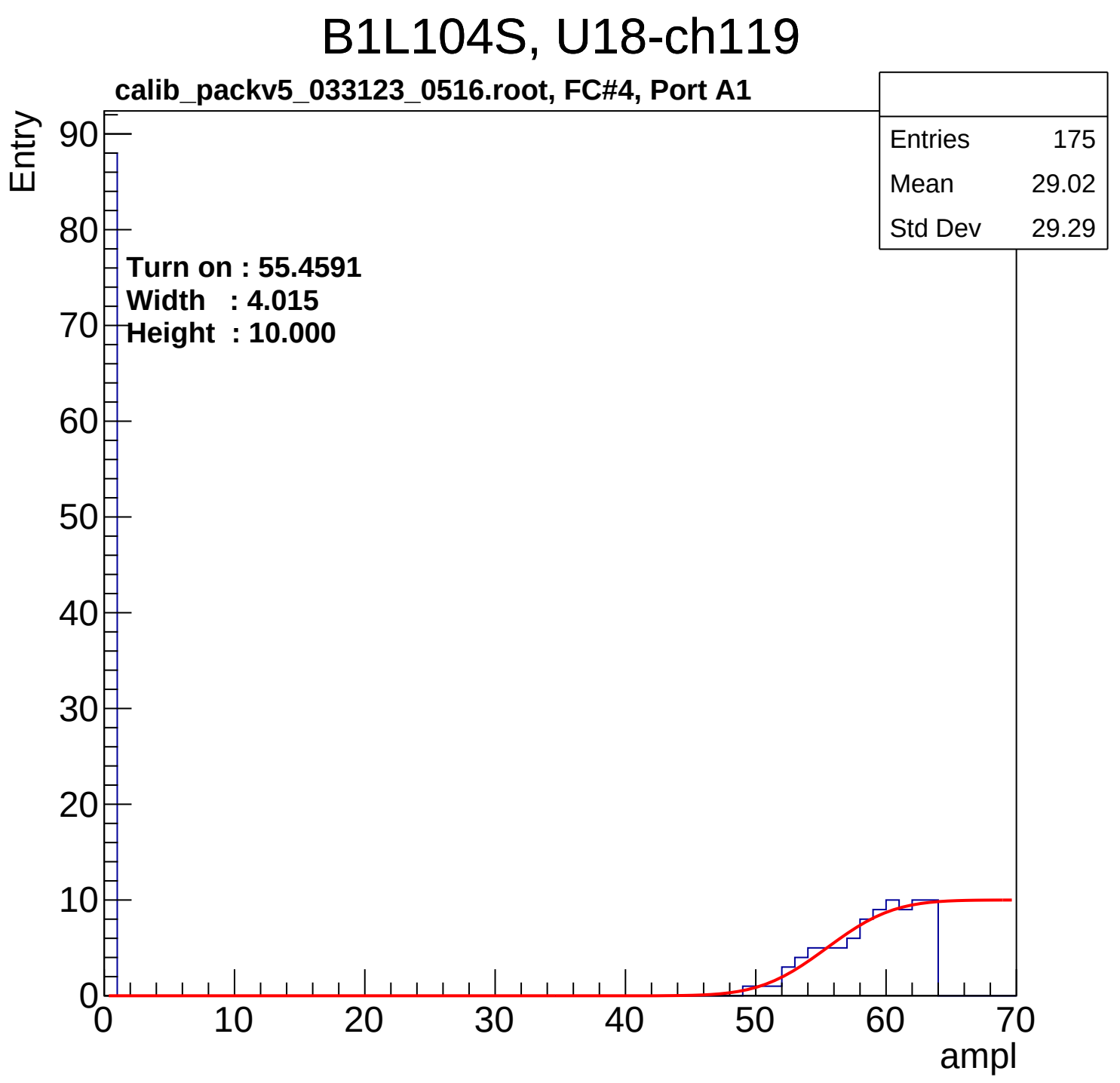
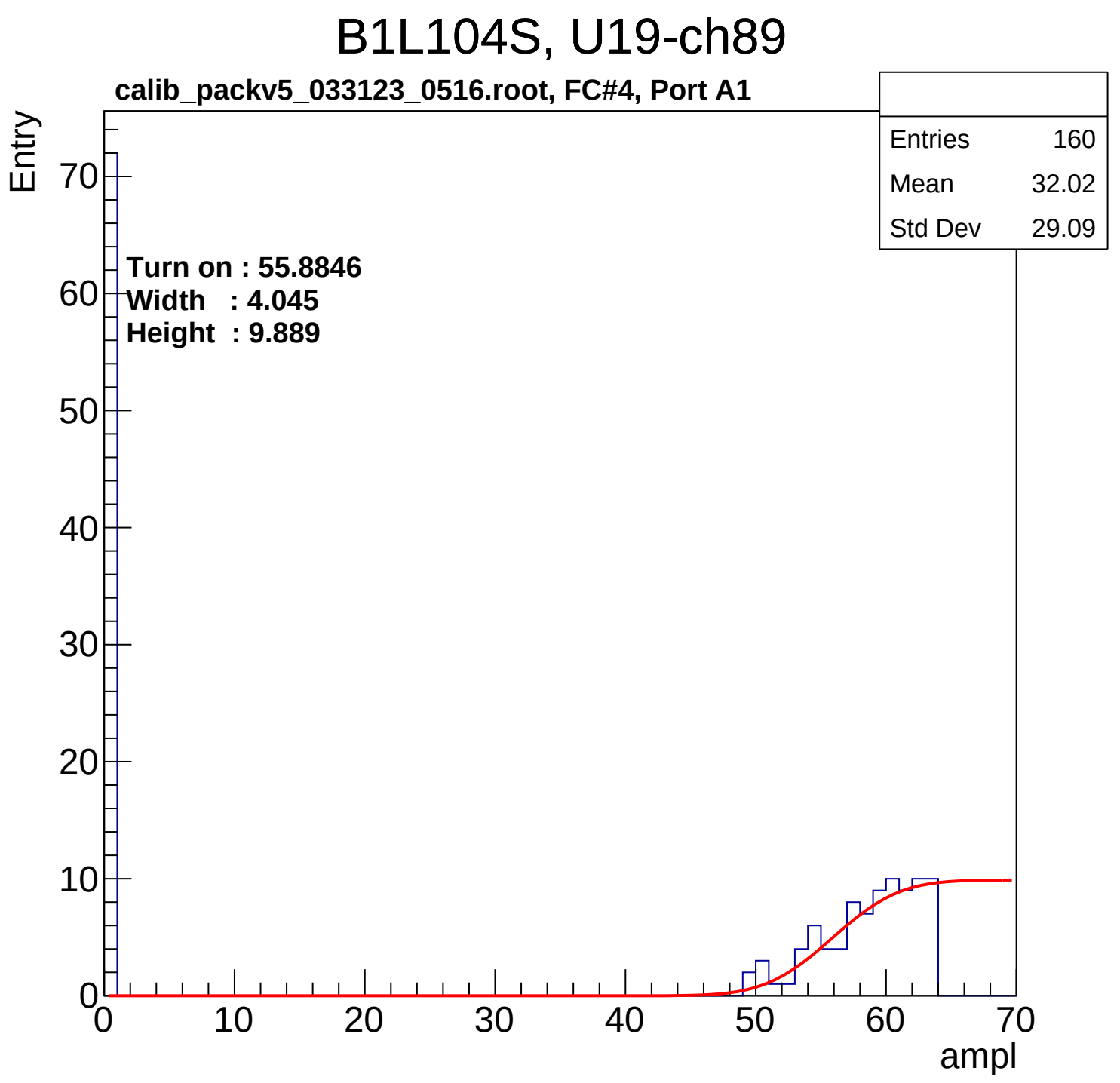

B1L104S, U18-ch119
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 175
Mean 29.02
Std Dev 29.29
Turn on : 55.4591
Width : 4.015
Height : 10.000
Entry
ampl
0
10
20
30
40
50
60
70
80
90


B1L104S, U19-ch89
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 160
Mean 32.02
Std Dev 29.09
Turn on : 55.8846
Width : 4.045
Height : 9.889
Entry
ampl
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30
40
50
60
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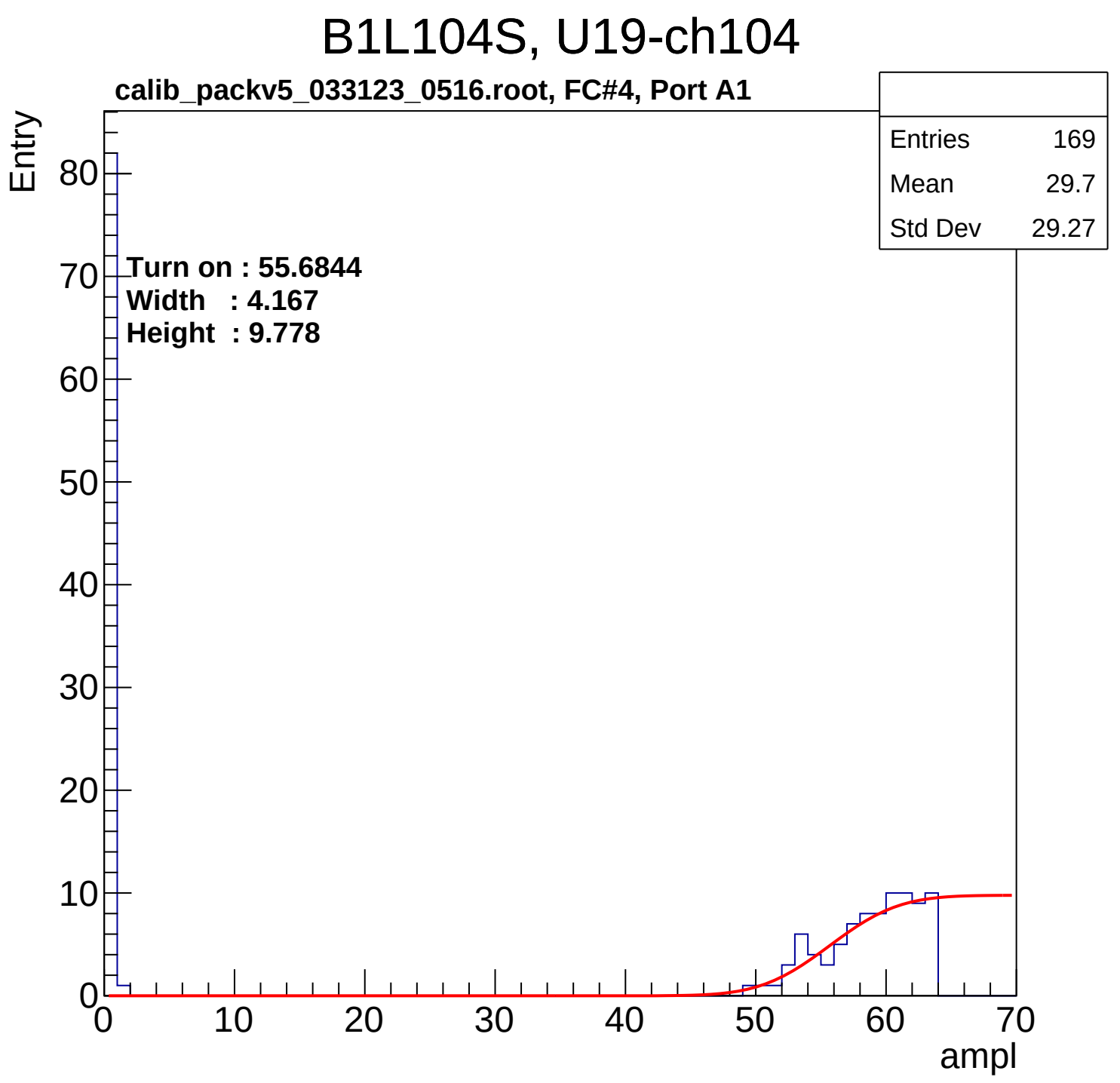
B1L104S, U19-ch104
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 169
Mean 29.7
Std Dev 29.27
Turn on : 55.6844
Width : 4.167
Height : 9.778
Entry
ampl
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10
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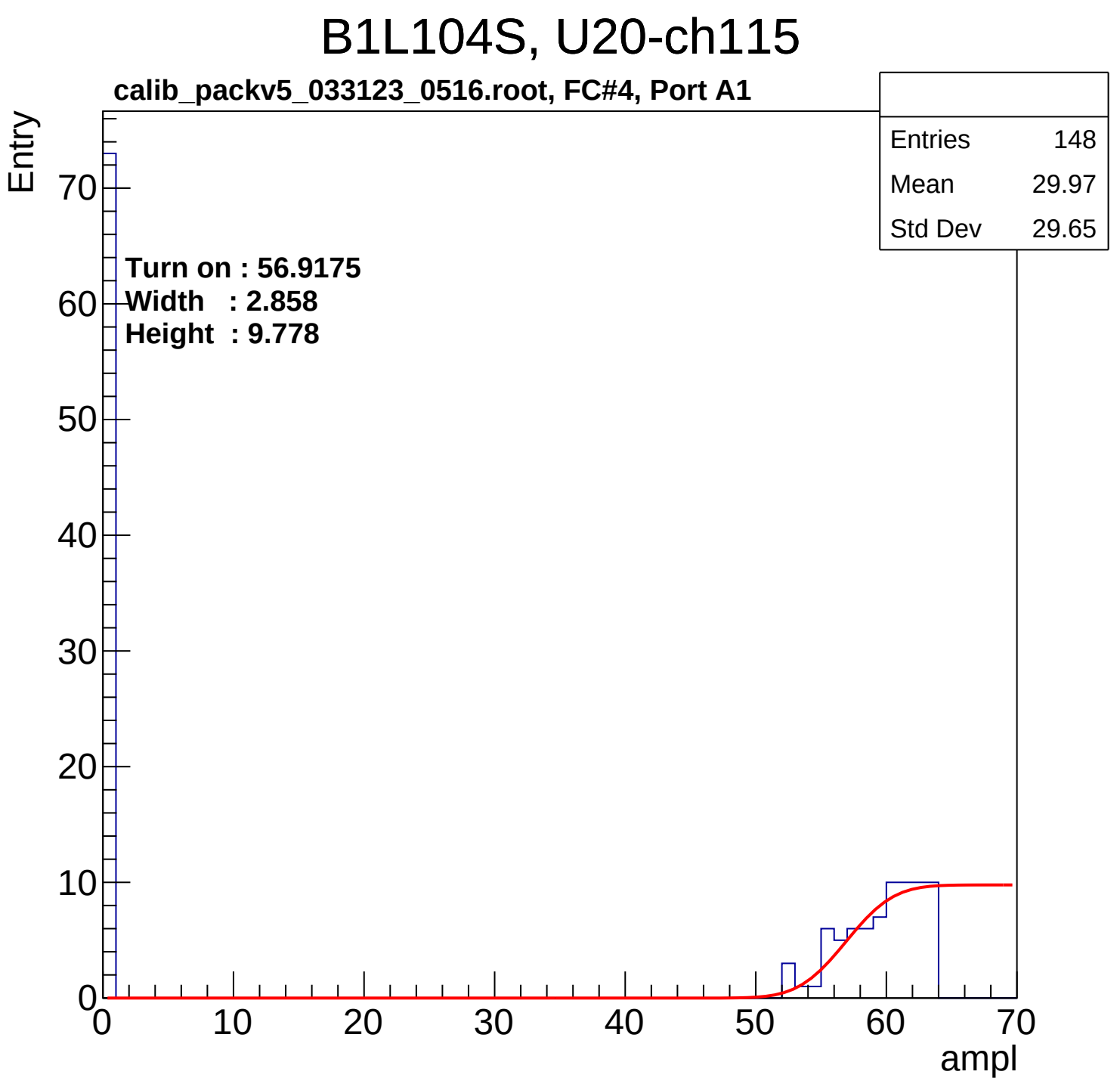
B1L104S, U20-ch115
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 148
Mean 29.97
Std Dev 29.65
Turn on : 56.9175
Width : 2.858
Height : 9.778
Entry
ampl
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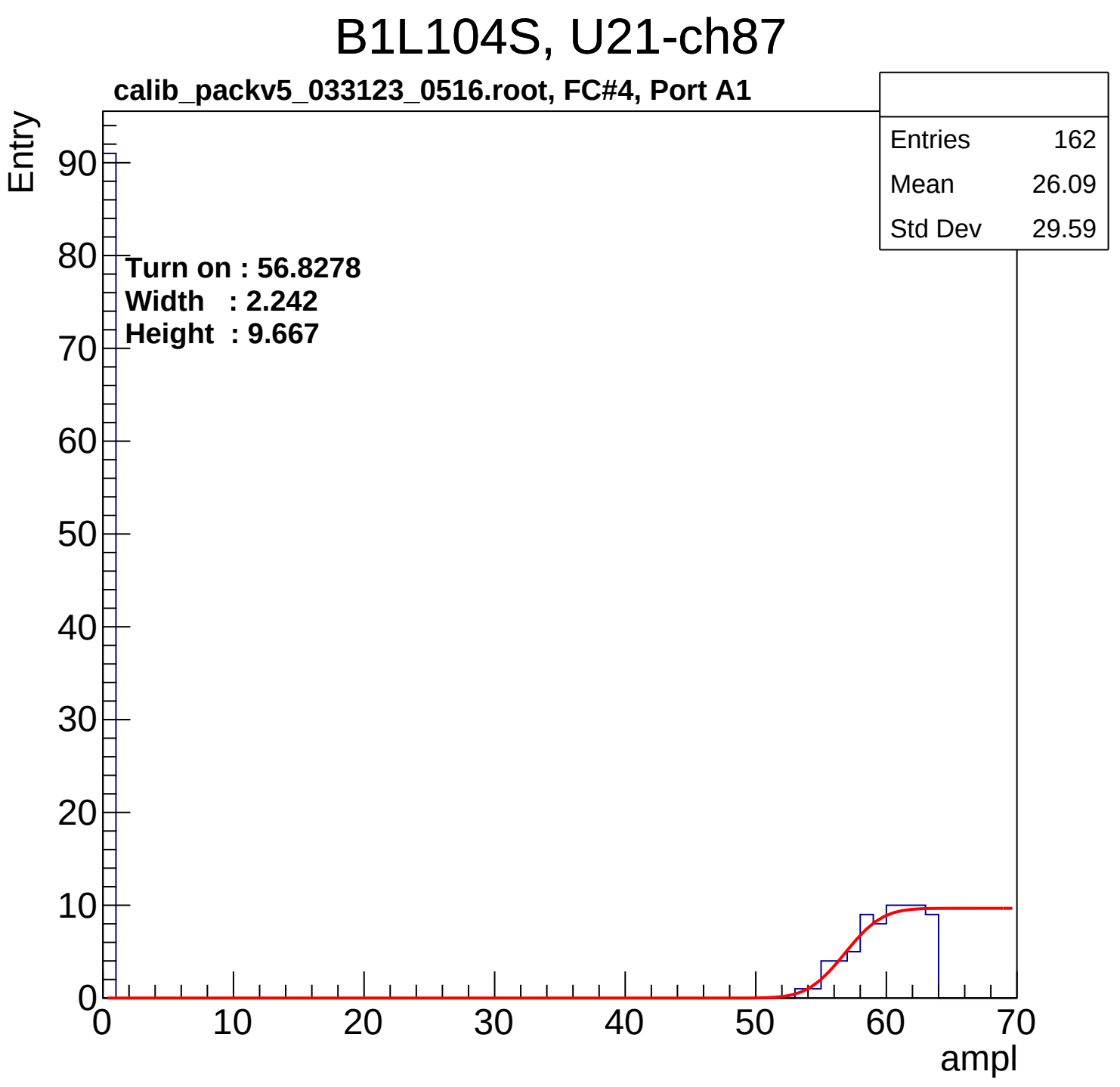
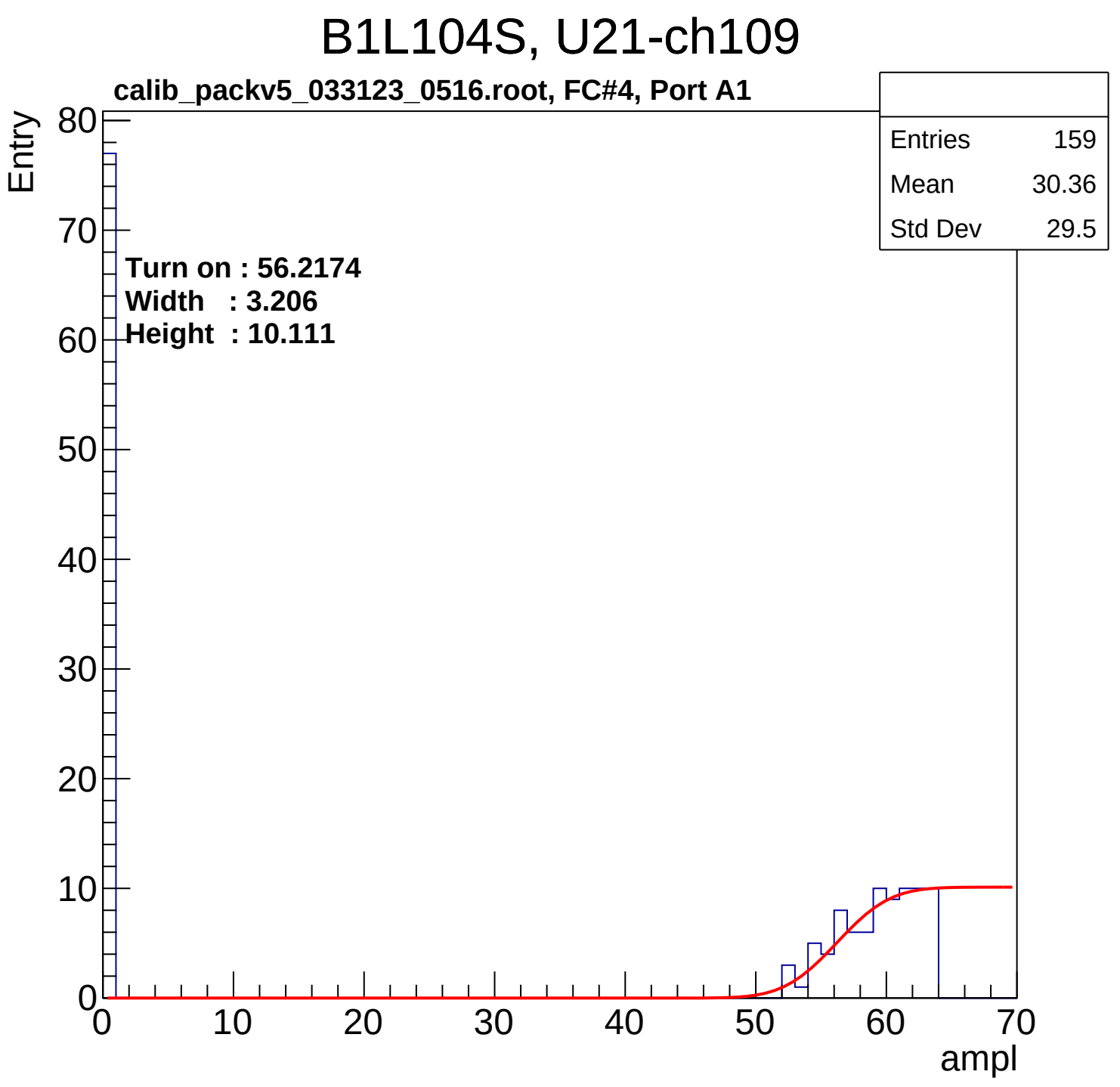

B1L104S, U21-ch87
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 162
Mean 26.09
Std Dev 29.59
Turn on : 56.8278
Width : 2.242
Height : 9.667
Entry
ampl
0
10
20
30
40
50
60
70
80
90


B1L104S, U21-ch109
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 159
Mean 30.36
Std Dev 29.5
Turn on : 56.2174
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Height : 10.111
Entry
ampl
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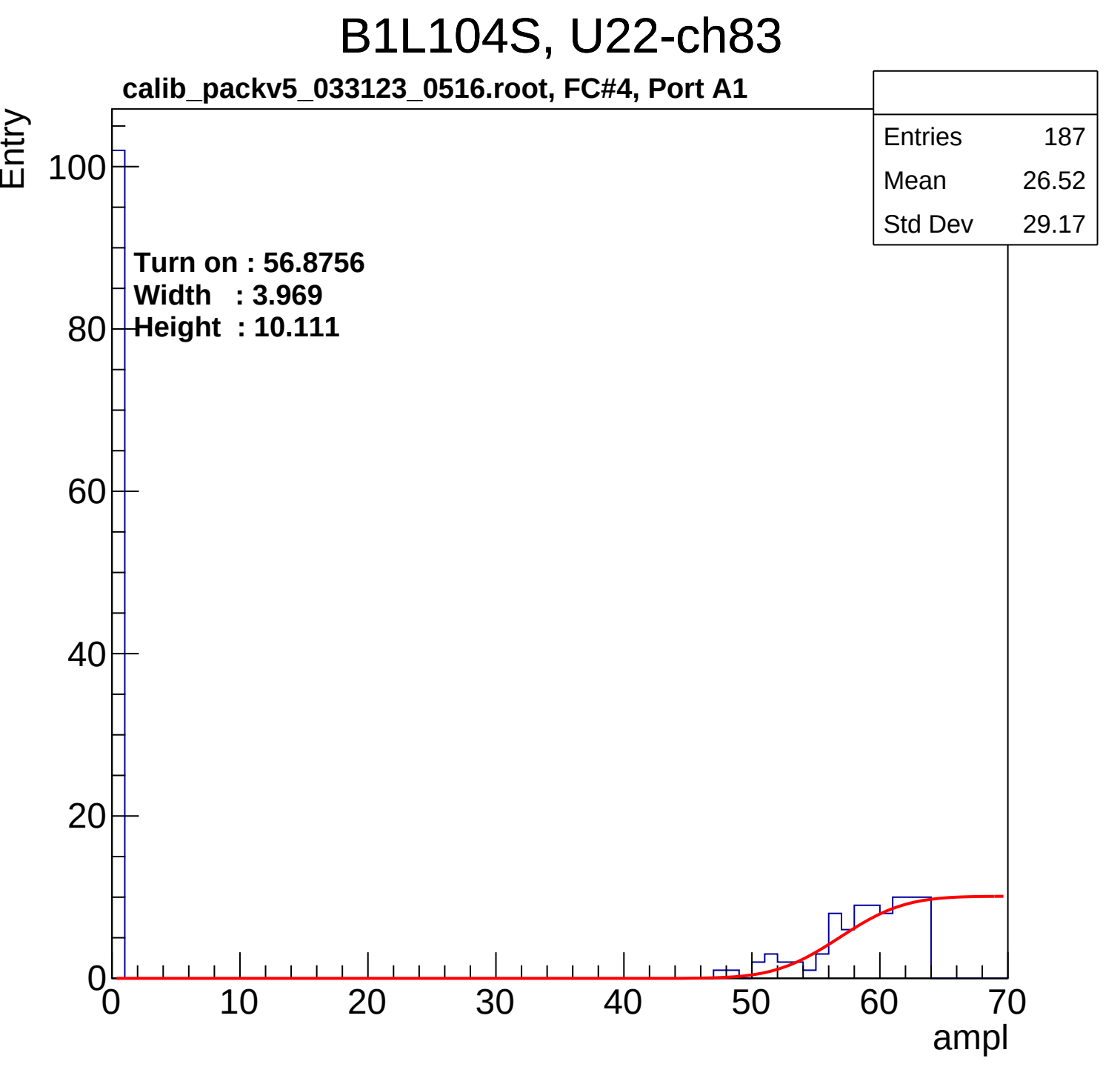
B1L104S, U22-ch83
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 187
Mean 26.52
Std Dev 29.17
Turn on : 56.8756
Width : 3.969
Height : 10.111
Entry
ampl
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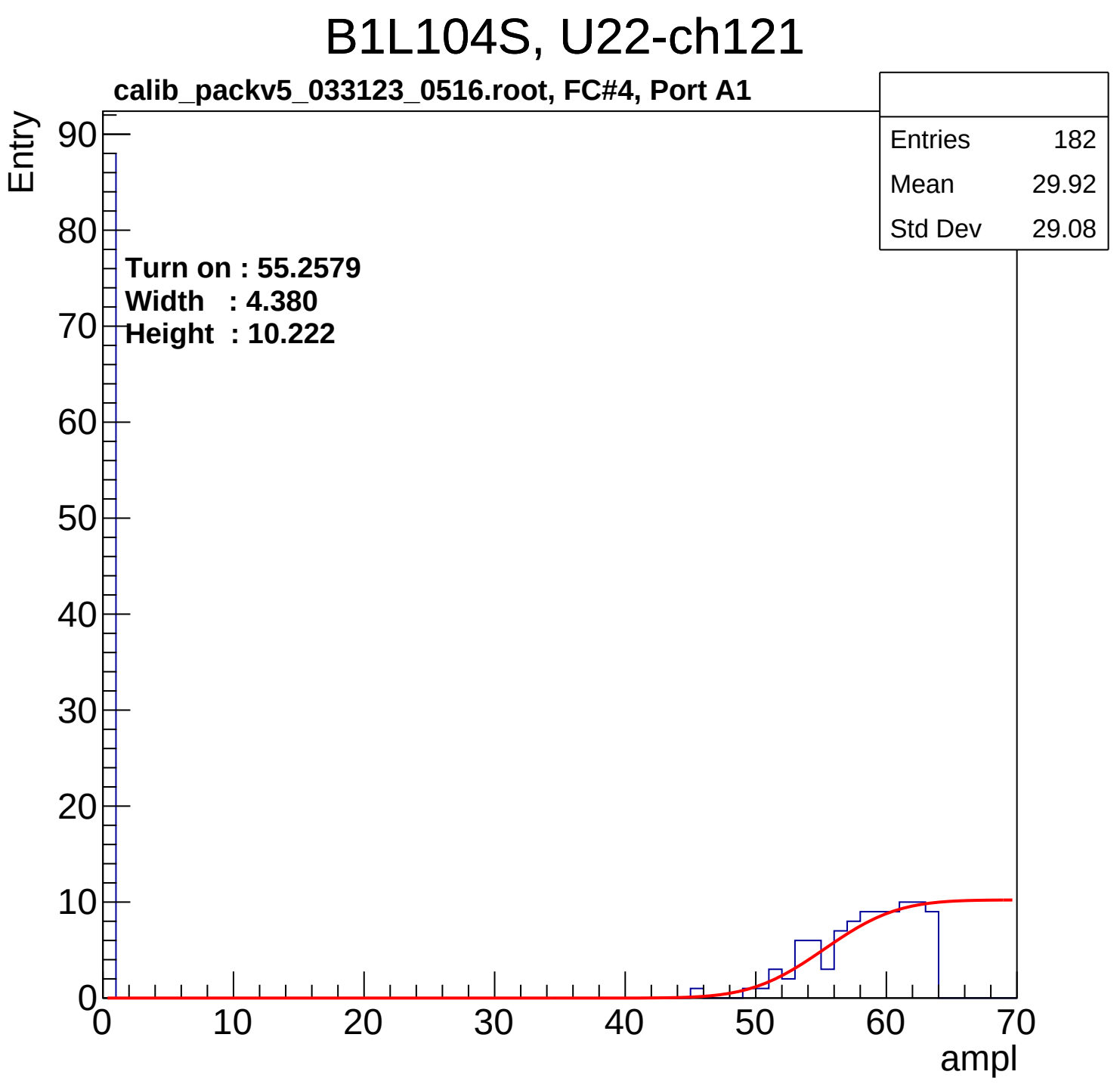
B1L104S, U22-ch121
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 182
Mean 29.92
Std Dev 29.08
Turn on : 55.2579
Width : 4.380
Height : 10.222
Entry
ampl
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80
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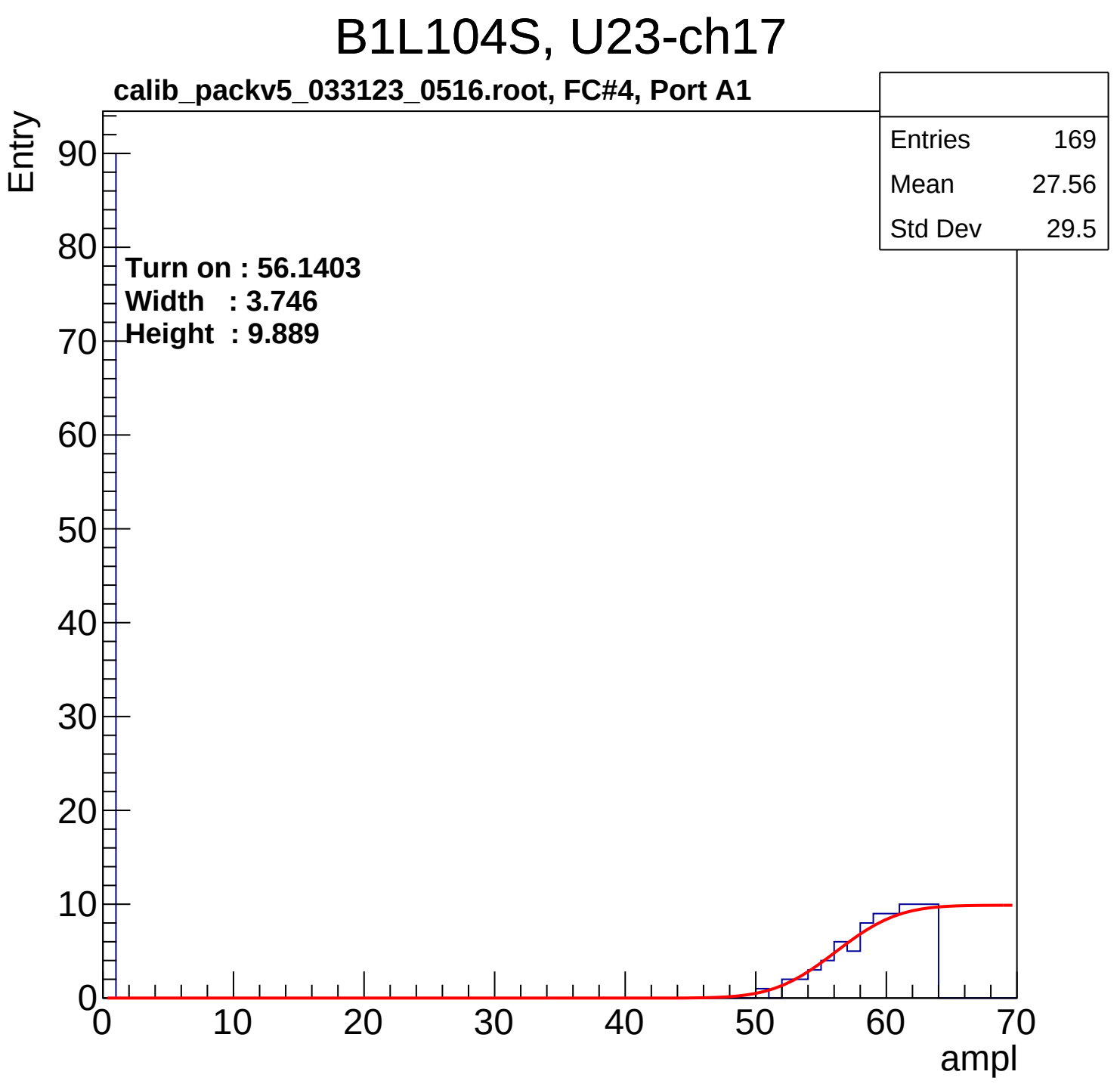
B1L104S, U23-ch17
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 169
Mean 27.56
Std Dev 29.5
Turn on : 56.1403
Width : 3.746
Height : 9.889
Entry
ampl
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80
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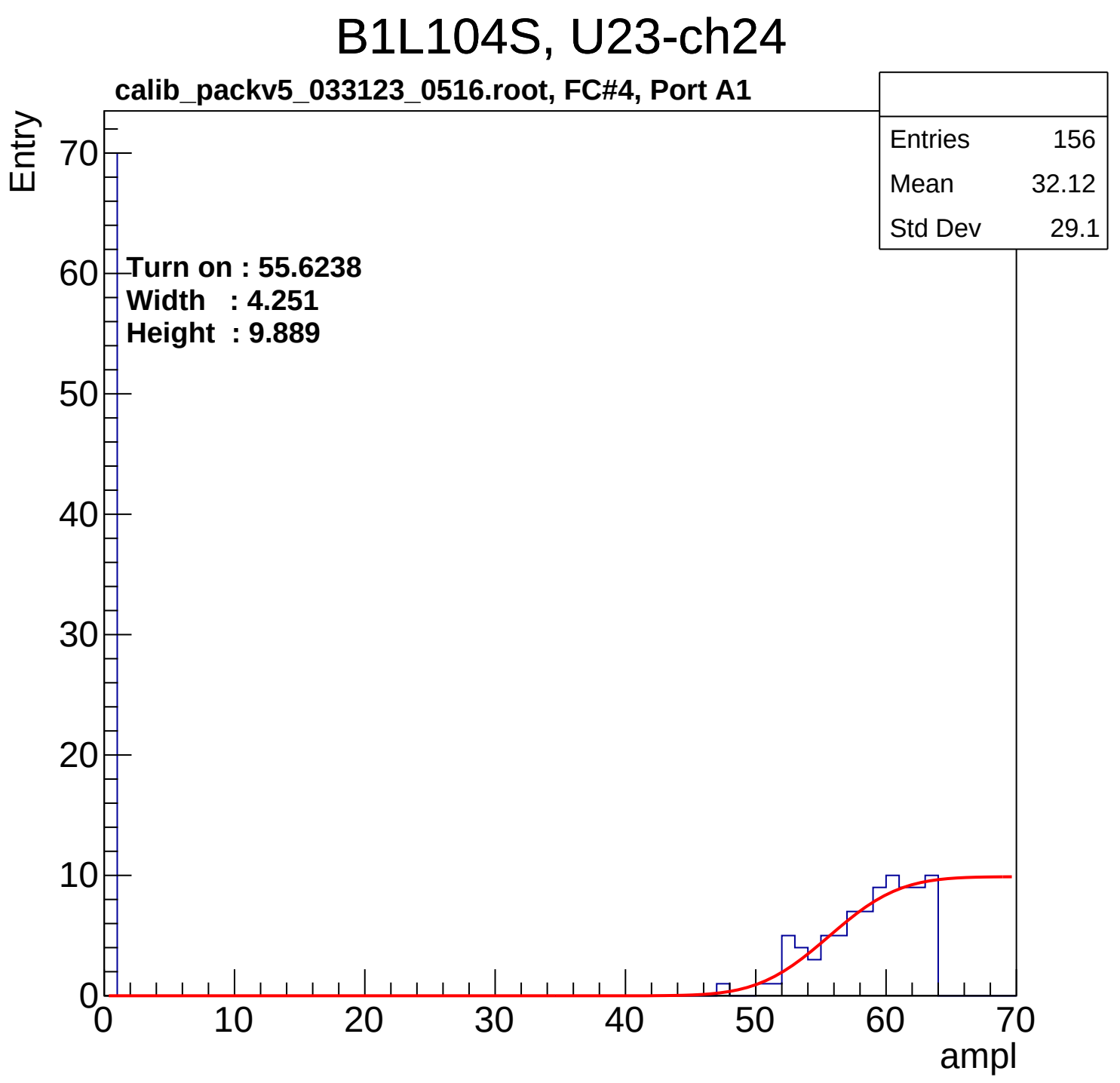
B1L104S, U23-ch24
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 156
Mean 32.12
Std Dev 29.1
Turn on : 55.6238
Width : 4.251
Height : 9.889
Entry
ampl
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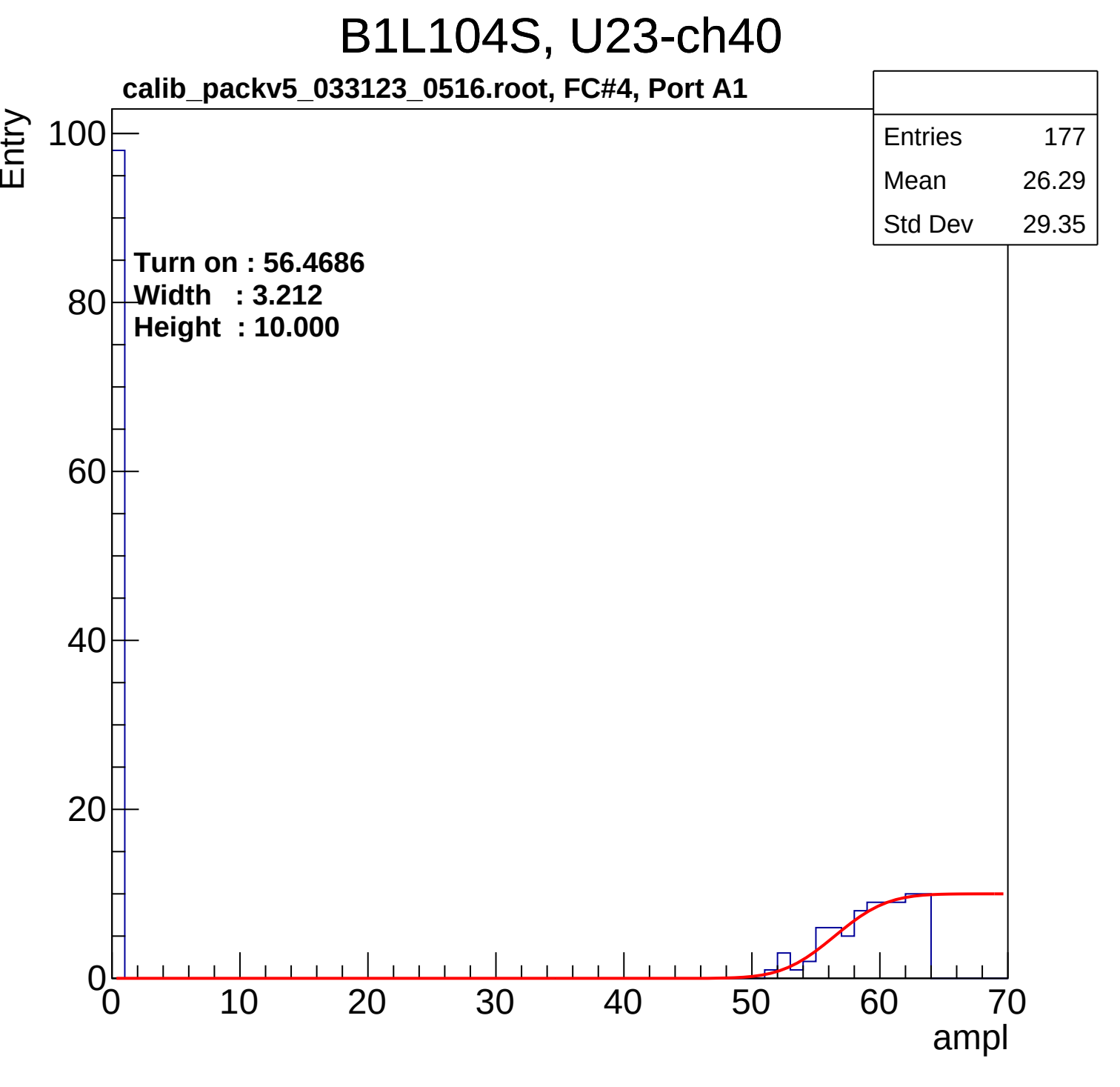
B1L104S, U23-ch40
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 177
Mean 26.29
Std Dev 29.35
Turn on : 56.4686
Width : 3.212
Height : 10.000
Entry
ampl
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20
40
60
80
100
0
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40
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60
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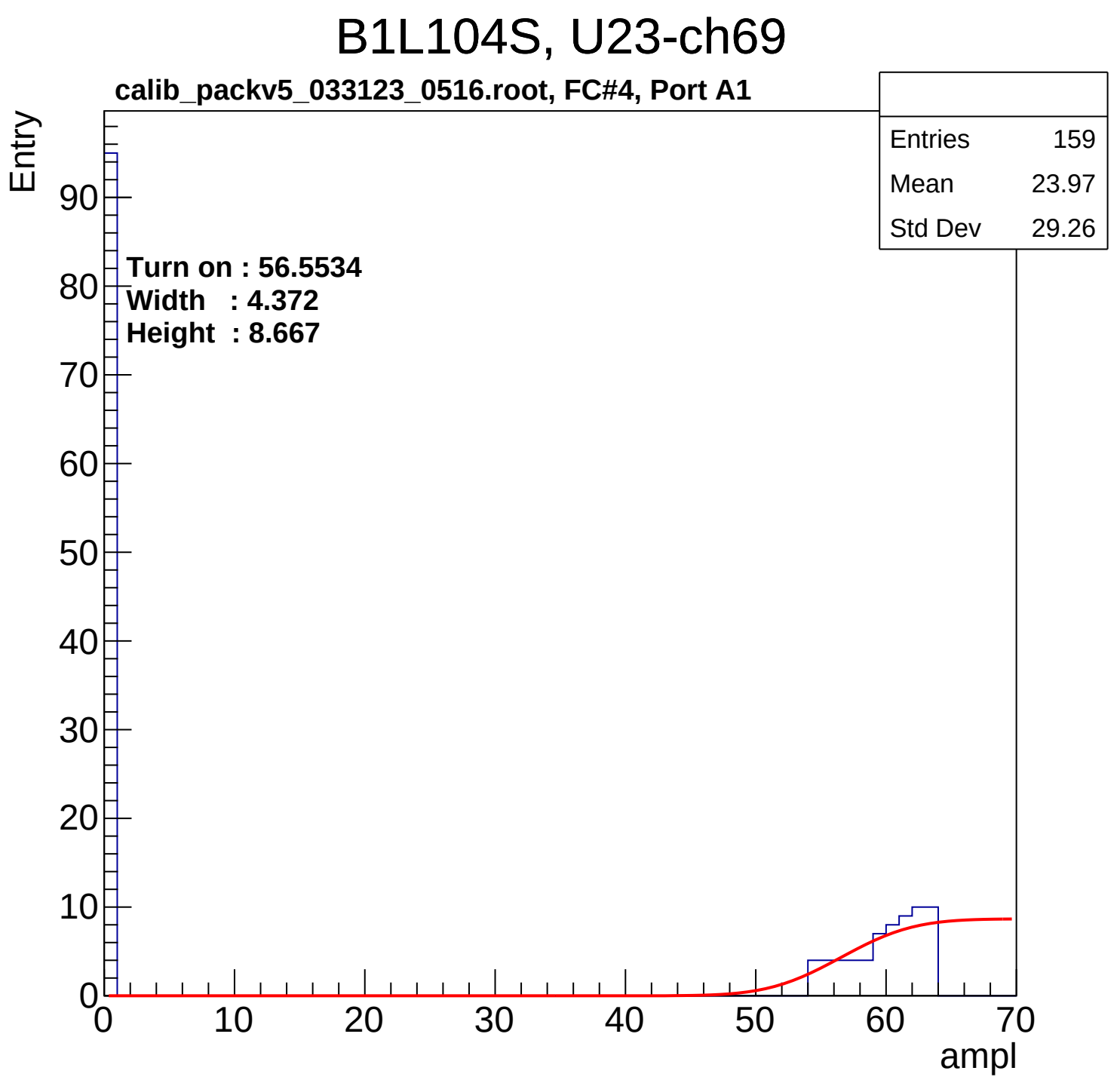
B1L104S, U23-ch69
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 159
Mean 23.97
Std Dev 29.26
Turn on : 56.5534
Width : 4.372
Height : 8.667
Entry
ampl
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10
20
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60
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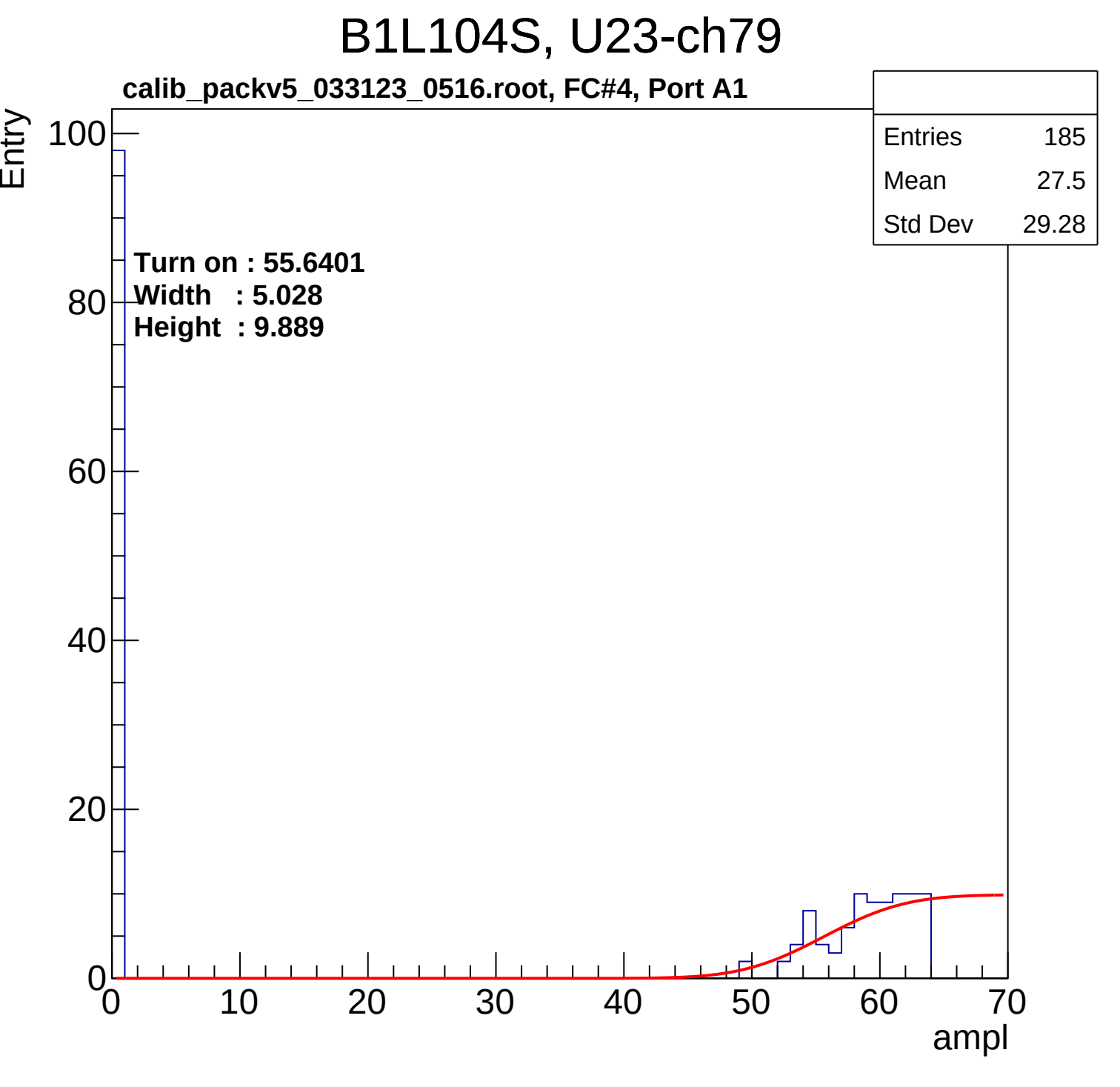
80
90


B1L104S, U23-ch79
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 185
Mean 27.5
Std Dev 29.28
Turn on : 55.6401
Width : 5.028
Height : 9.889
Entry
ampl
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20
40
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80
100
0
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20
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40
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60
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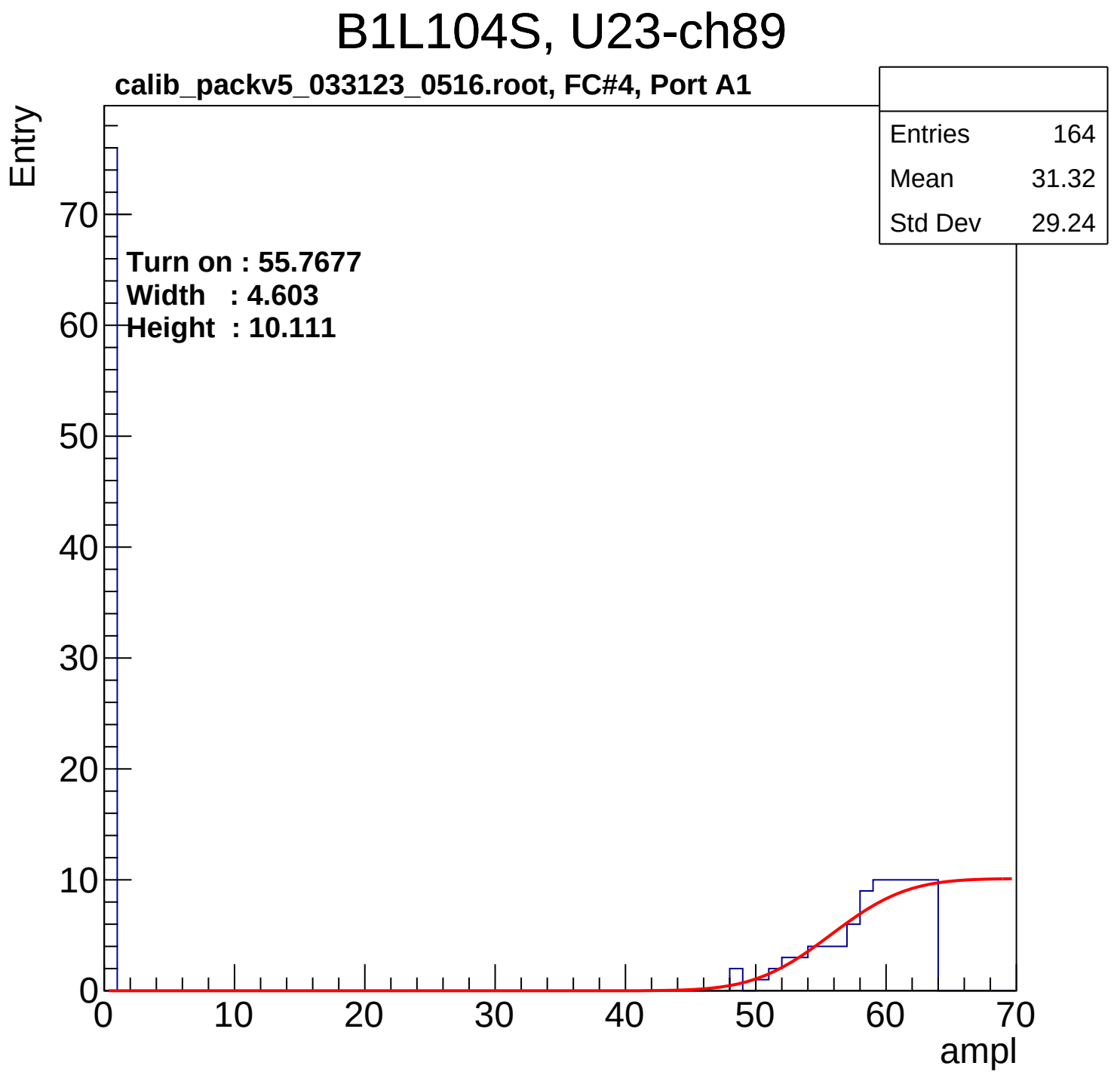
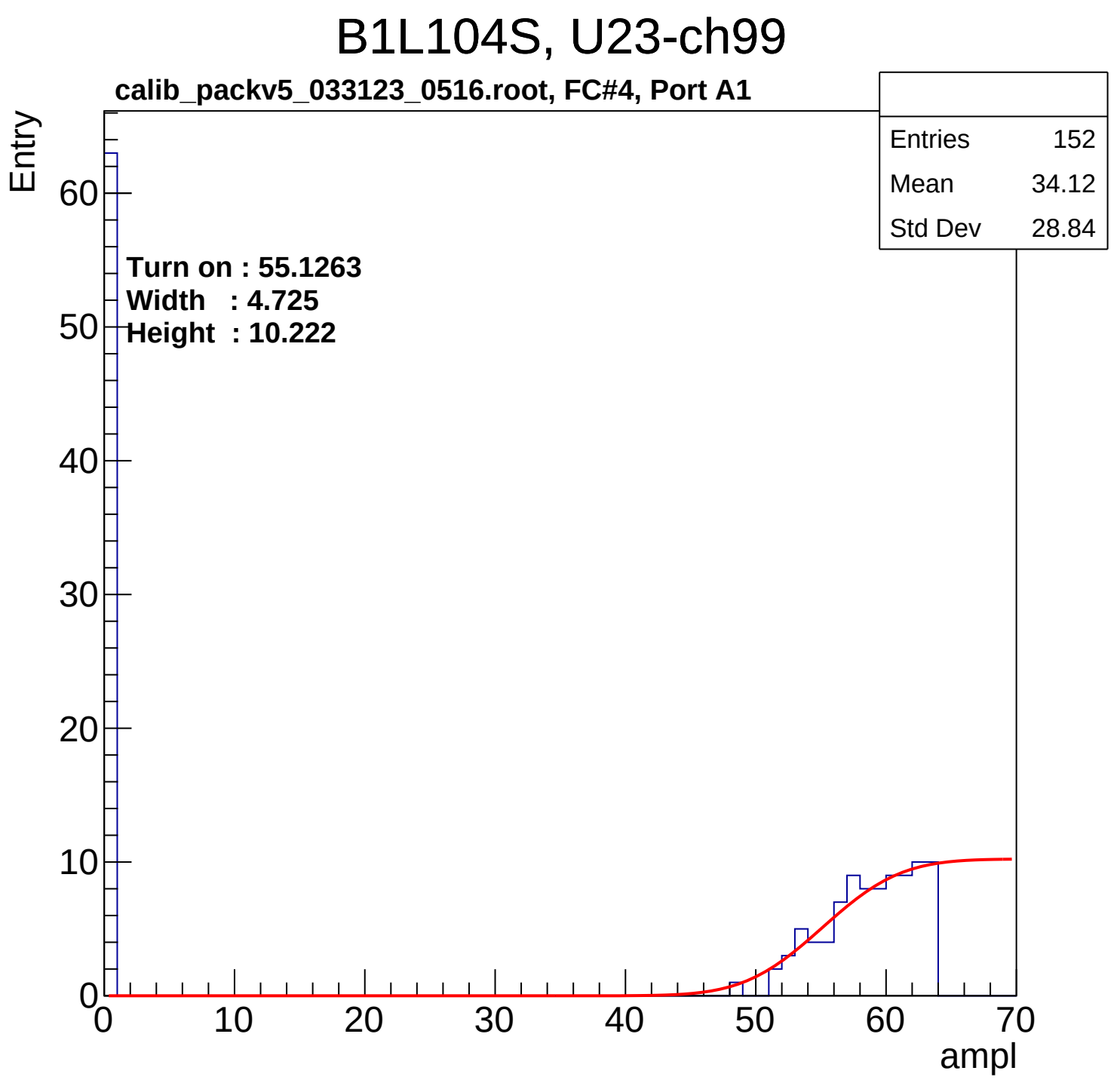
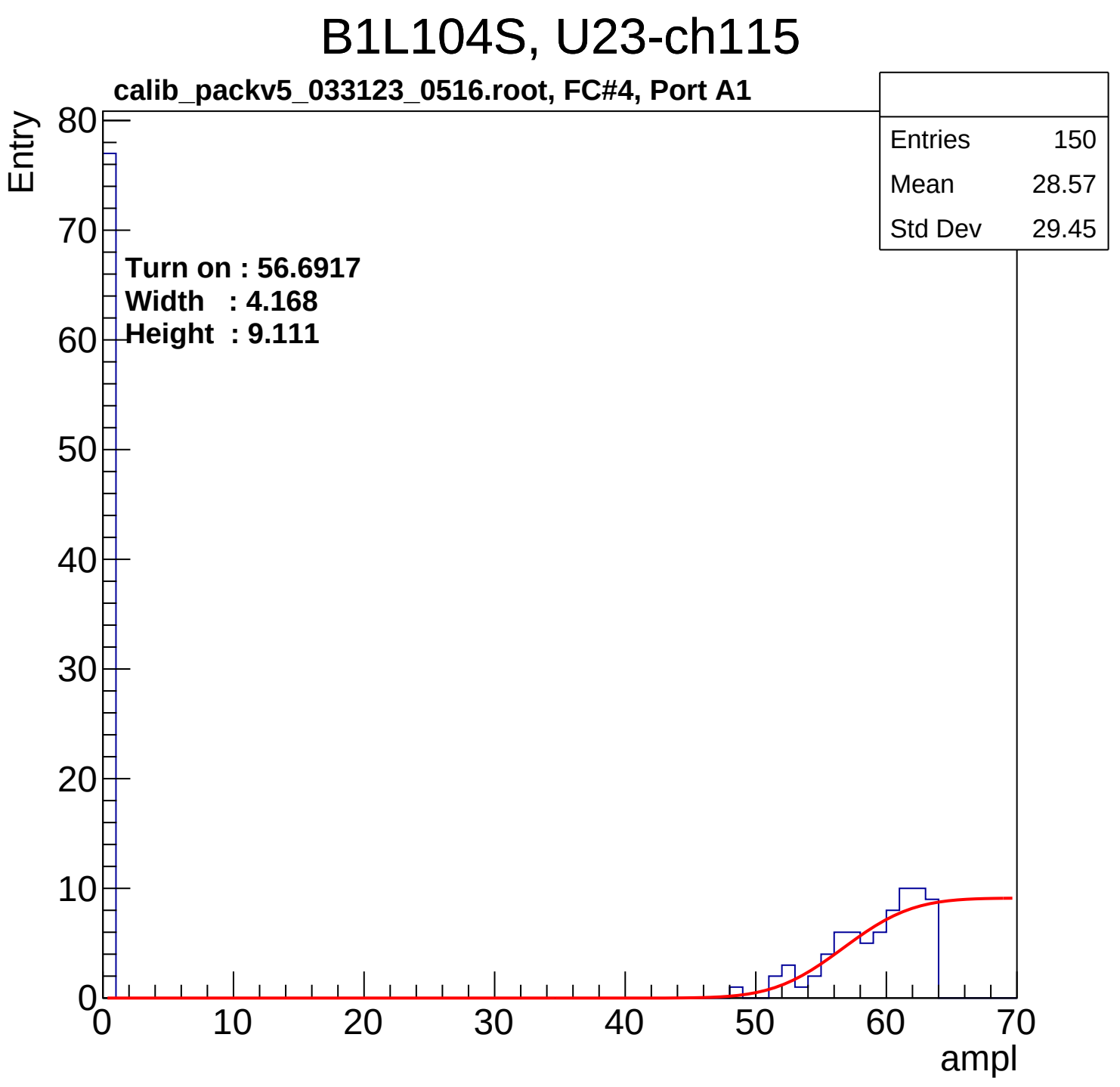

B1L104S, U23-ch89
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 164
Mean 31.32
Std Dev 29.24
Turn on : 55.7677
Width : 4.603
Height : 10.111
Entry
ampl
0
10
20
30
40
50
60
70


B1L104S, U23-ch99
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 152
Mean 34.12
Std Dev 28.84
Turn on : 55.1263
Width : 4.725
Height : 10.222
Entry
ampl
0
10
20
30
40
50
60
70


B1L104S, U23-ch115
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 150
Mean 28.57
Std Dev 29.45
Turn on : 56.6917
Width : 4.168
Height : 9.111
Entry
ampl
0
10
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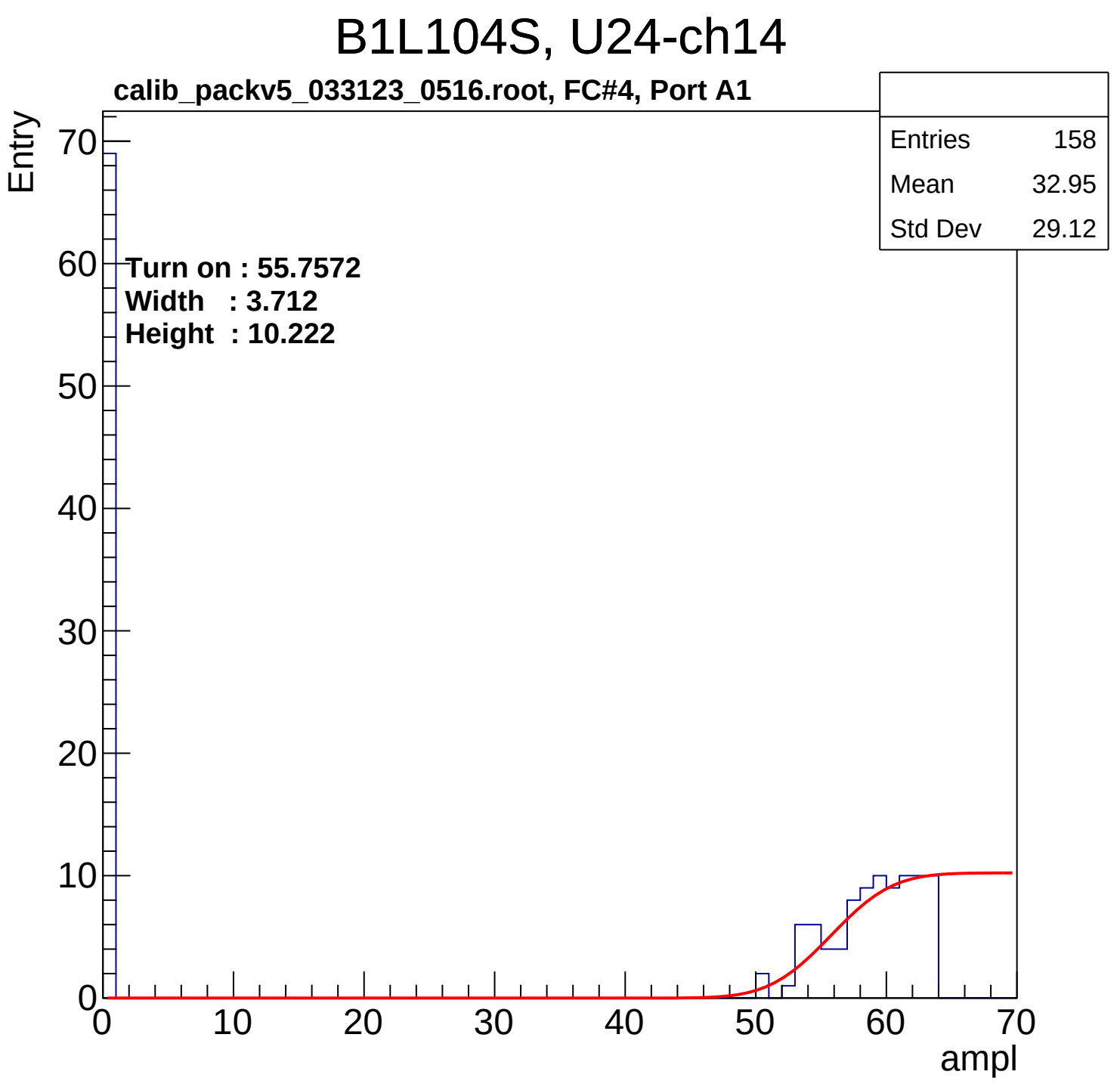
30
40
50
60
70
80


B1L104S, U24-ch14
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 158
Mean 32.95
Std Dev 29.12
Turn on : 55.7572
Width : 3.712
Height : 10.222
Entry
ampl
0
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40
50
60
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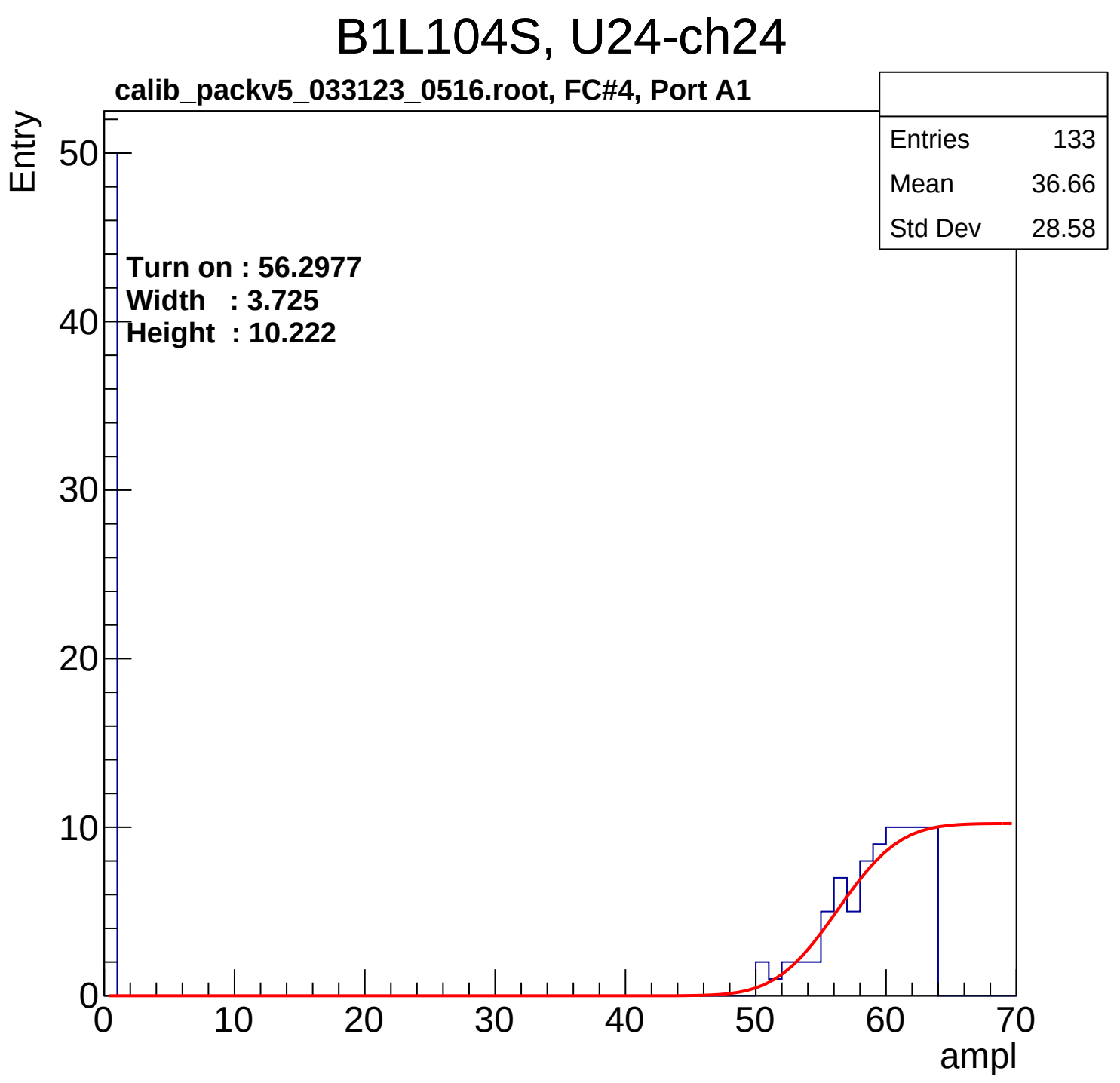
B1L104S, U24-ch24
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 133
Mean 36.66
Std Dev 28.58
Turn on : 56.2977
Width : 3.725
Height : 10.222
Entry
ampl
0
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30
40
50
60
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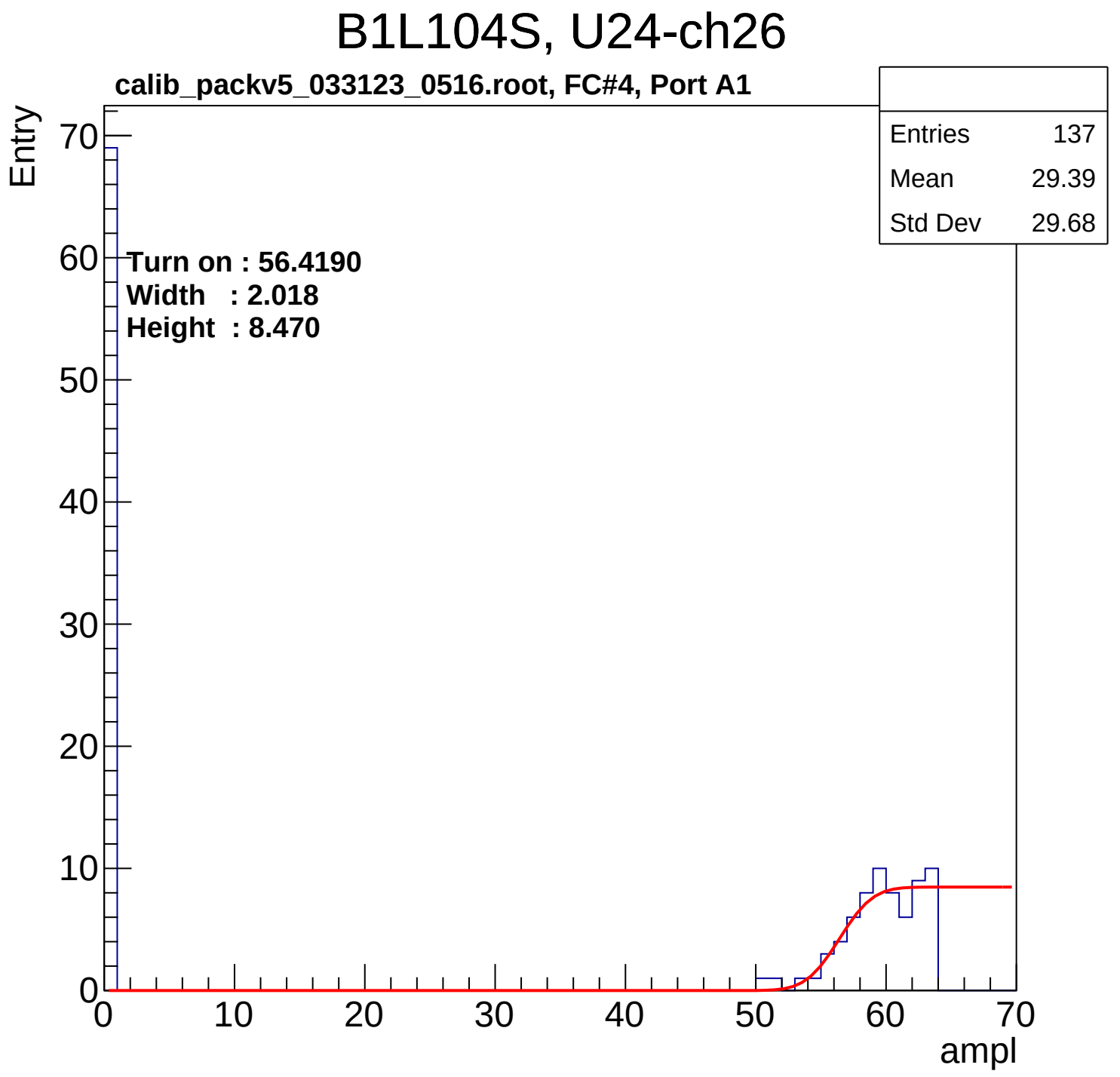
B1L104S, U24-ch26
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 137
Mean 29.39
Std Dev 29.68
Turn on : 56.4190
Width : 2.018
Height : 8.470
Entry
ampl
0
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20
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40
50
60
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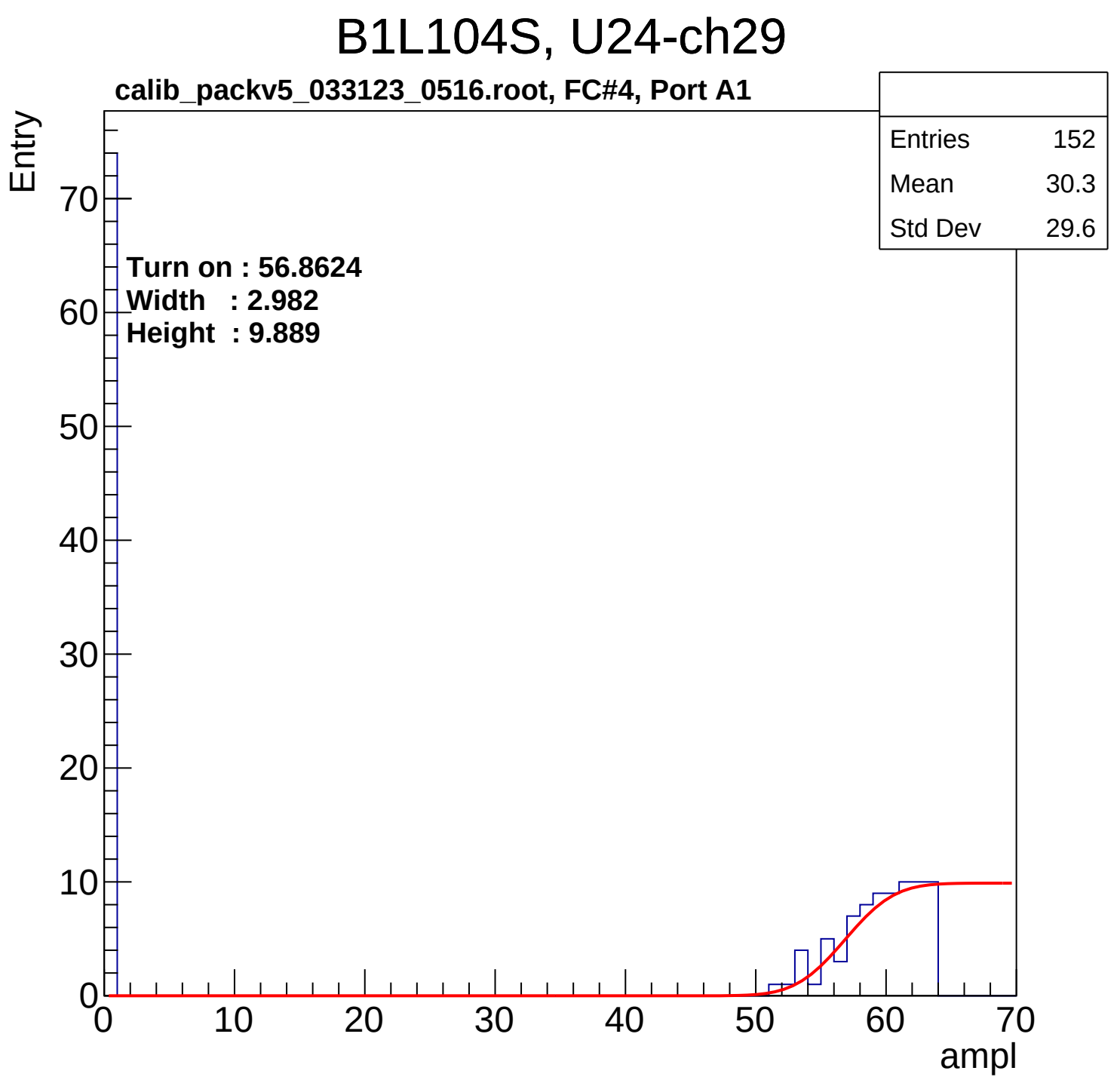
B1L104S, U24-ch29
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 152
Mean 30.3
Std Dev 29.6
Turn on : 56.8624
Width : 2.982
Height : 9.889
Entry
ampl
0
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30
40
50
60
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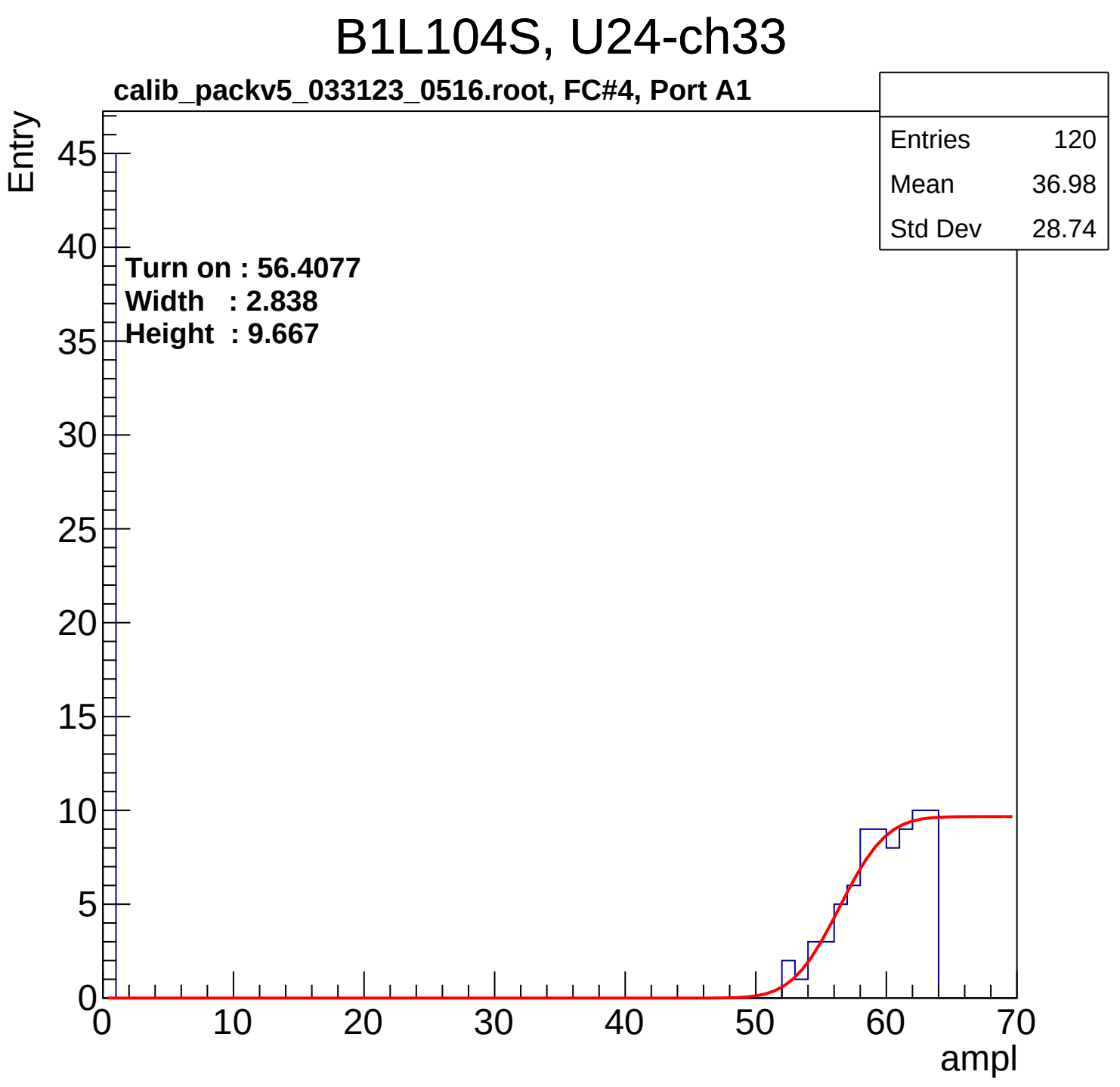
B1L104S, U24-ch33
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 120
Mean 36.98
Std Dev 28.74
Turn on : 56.4077
Width : 2.838
Height : 9.667
Entry
ampl
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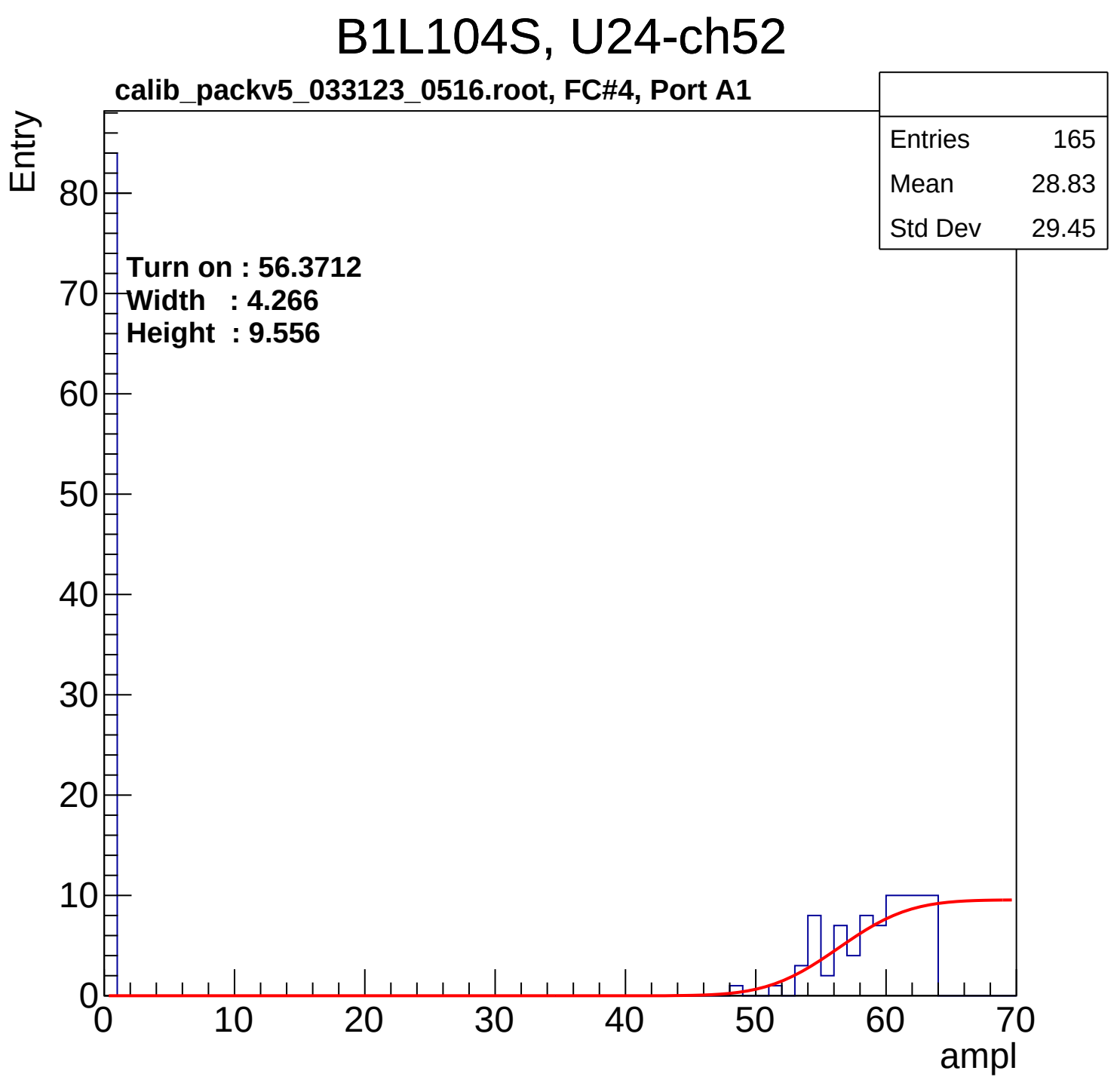
10
15
20
25
30
35
40
45
0
10
20
30
40
50
60
70


B1L104S, U24-ch52
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 165
Mean 28.83
Std Dev 29.45
Turn on : 56.3712
Width : 4.266
Height : 9.556
Entry
ampl
0
10
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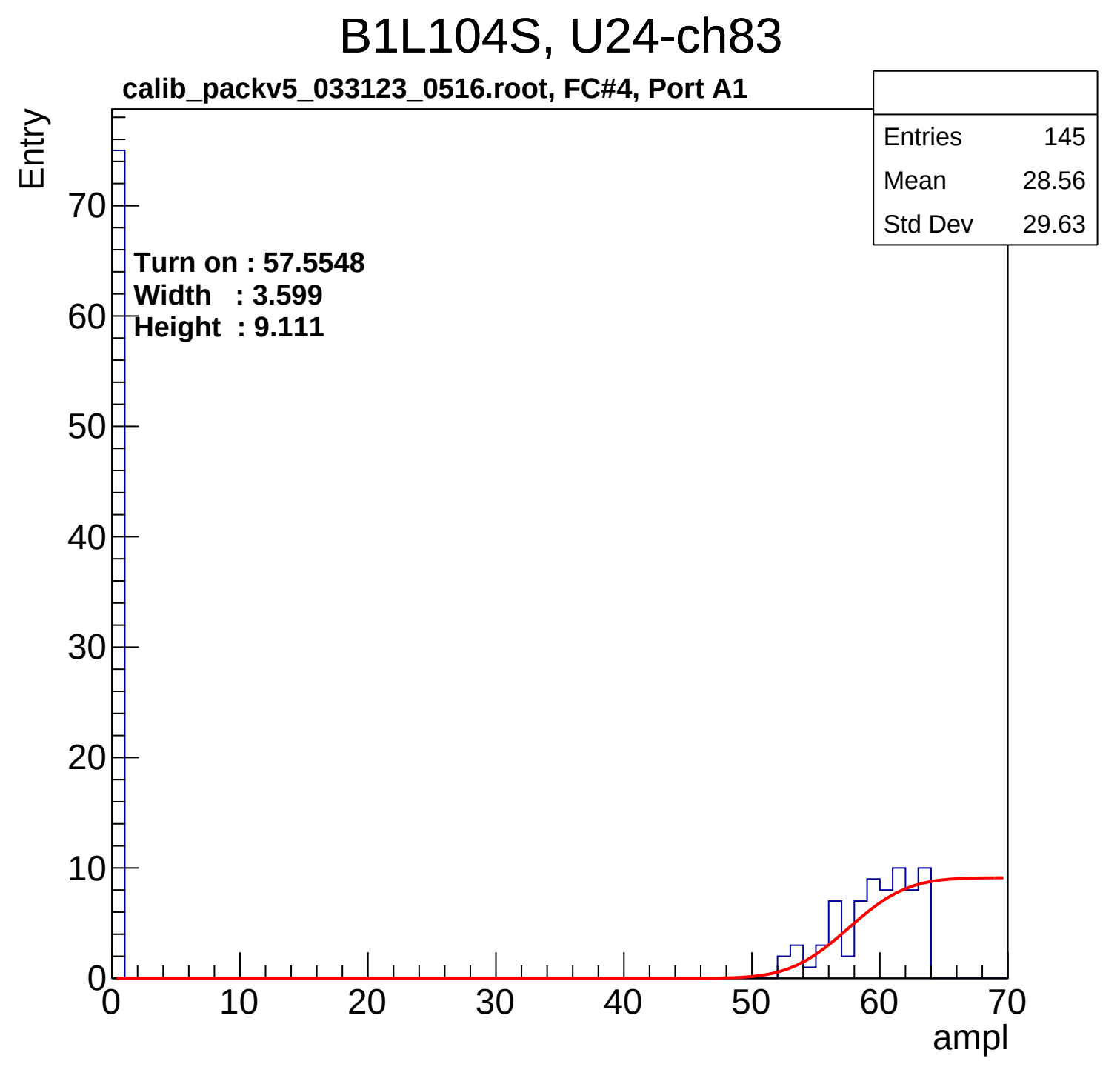
30
40
50
60
70
80


B1L104S, U24-ch83
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 145
Mean 28.56
Std Dev 29.63
Turn on : 57.5548
Width : 3.599
Height : 9.111
Entry
ampl
0
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40
50
60
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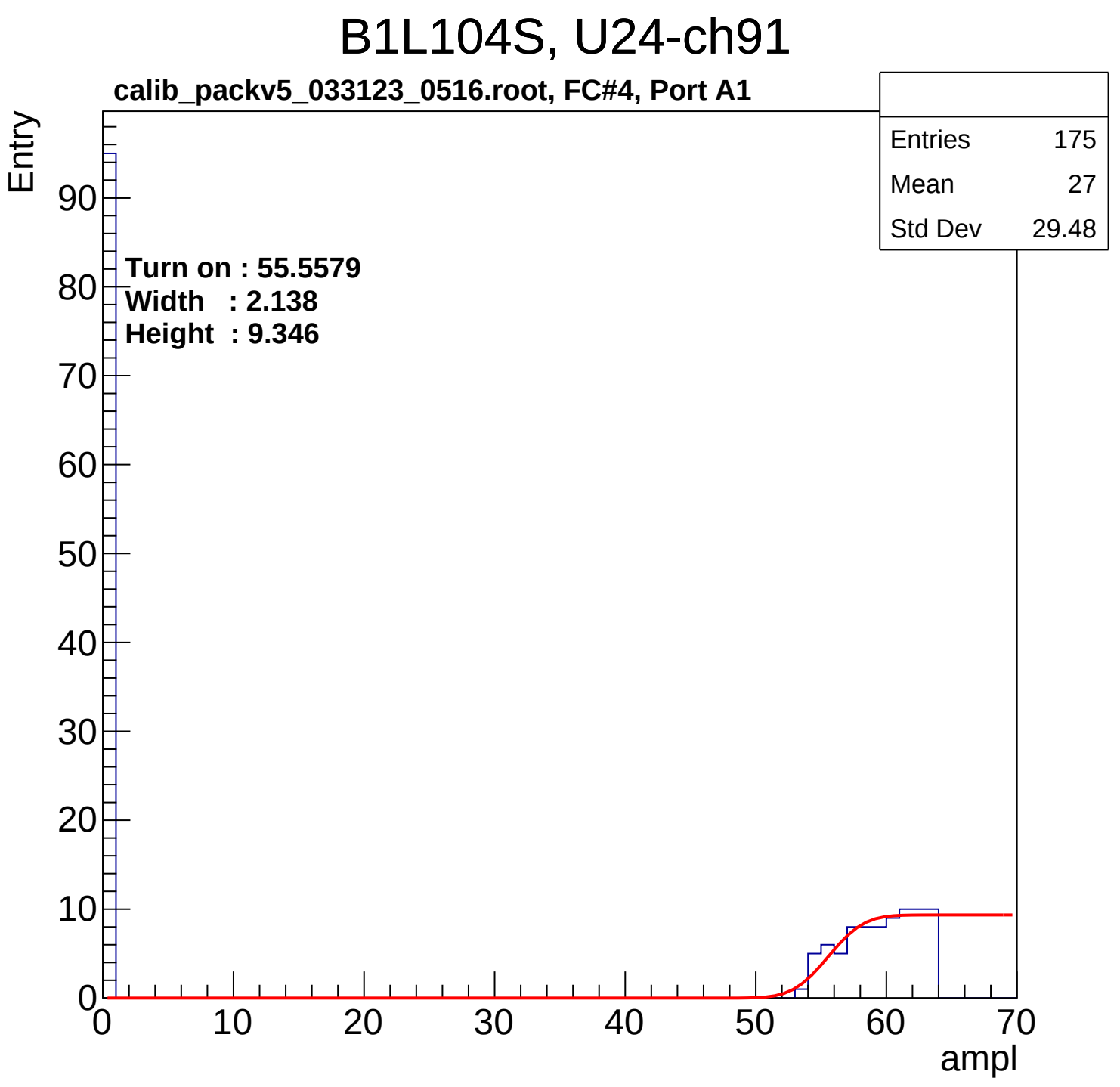
B1L104S, U24-ch91
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 175
Mean 27
Std Dev 29.48
Turn on : 55.5579
Width : 2.138
Height : 9.346
Entry
ampl
0
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20
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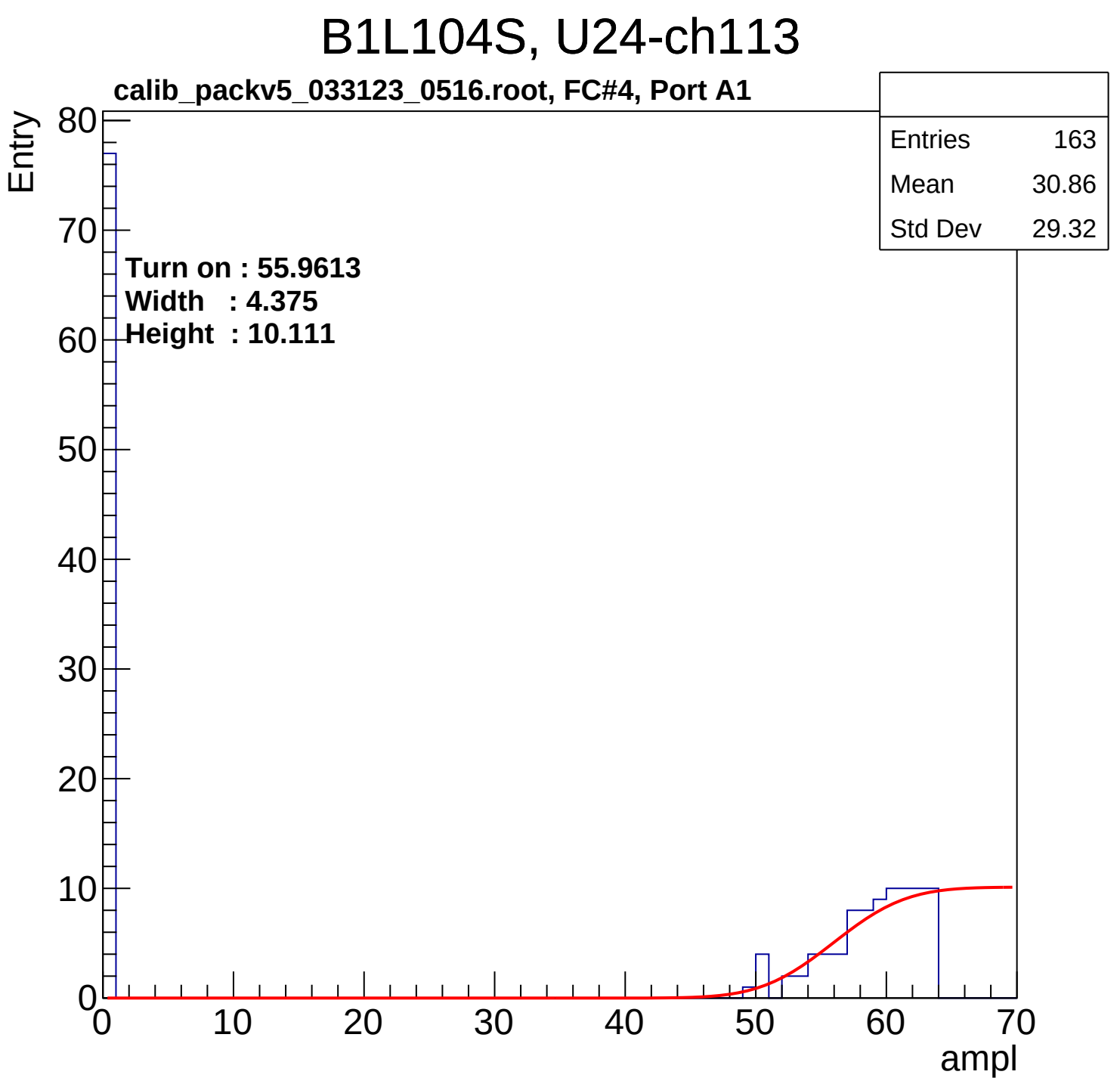
60
70
80
90


B1L104S, U24-ch113
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 163
Mean 30.86
Std Dev 29.32
Turn on : 55.9613
Width : 4.375
Height : 10.111
Entry
ampl
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70
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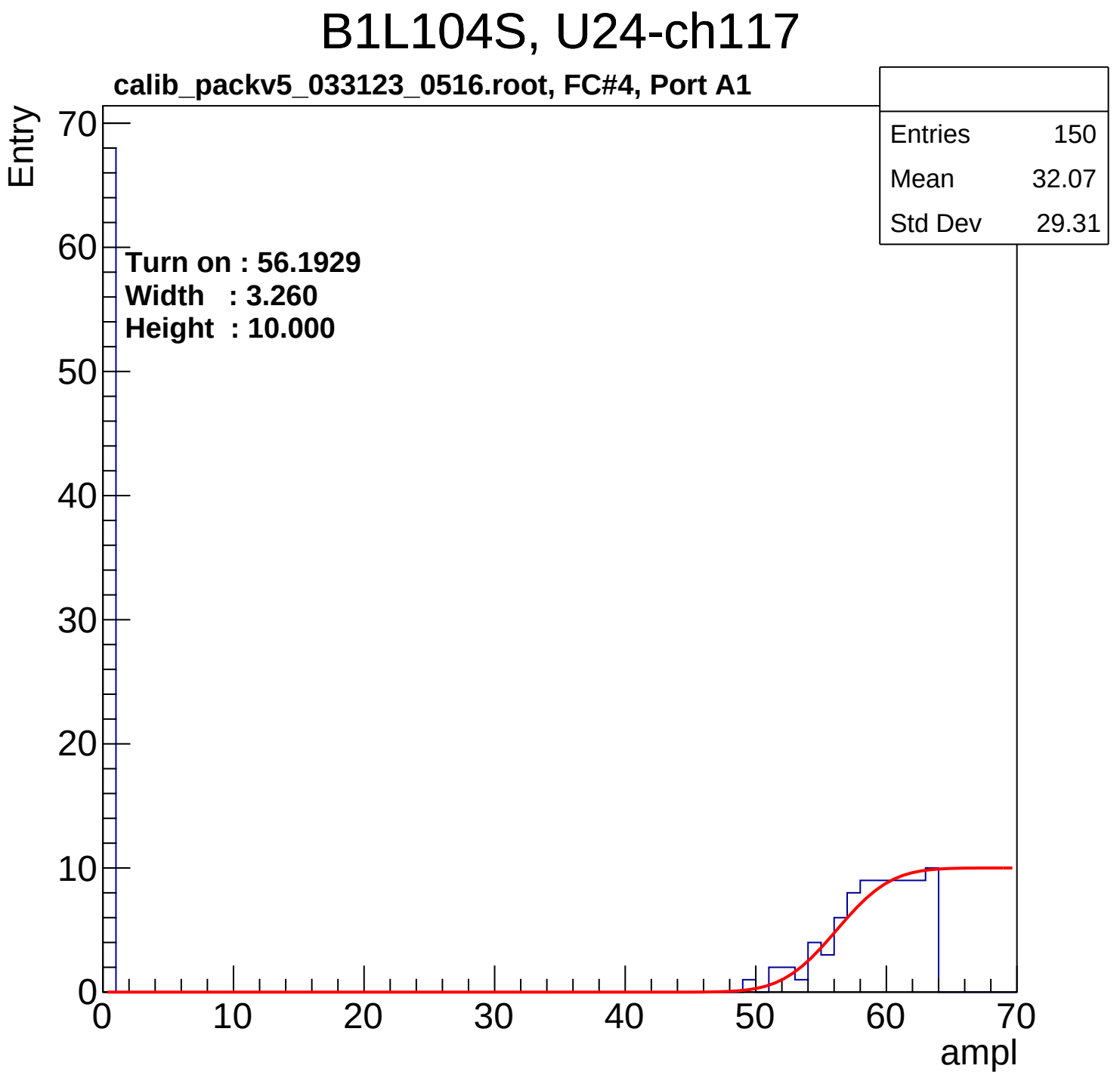
B1L104S, U24-ch117
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 150
Mean 32.07
Std Dev 29.31
Turn on : 56.1929
Width : 3.260
Height : 10.000
Entry
ampl
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60
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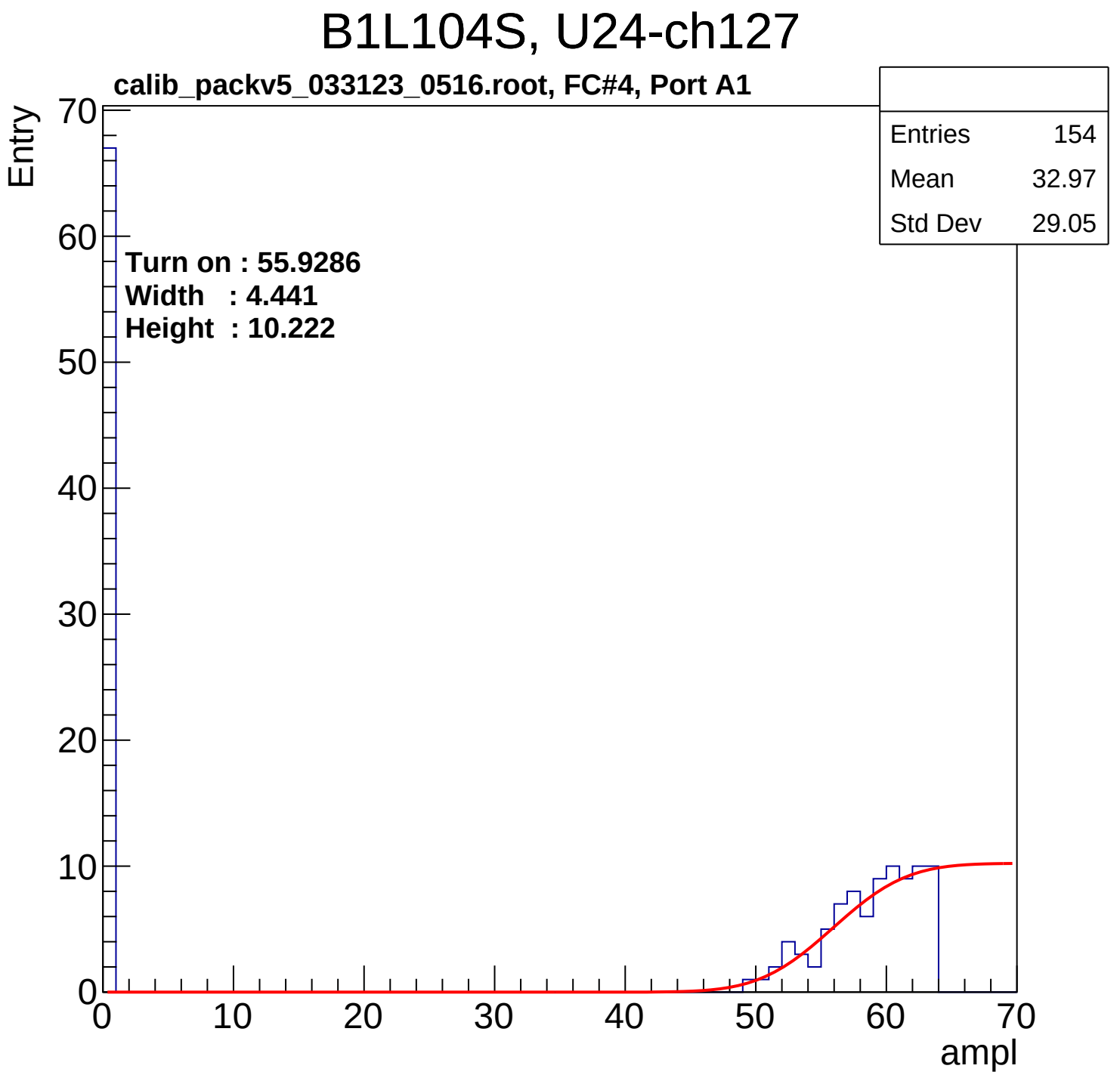
B1L104S, U24-ch127
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 154
Mean 32.97
Std Dev 29.05
Turn on : 55.9286
Width : 4.441
Height : 10.222
Entry
ampl
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60
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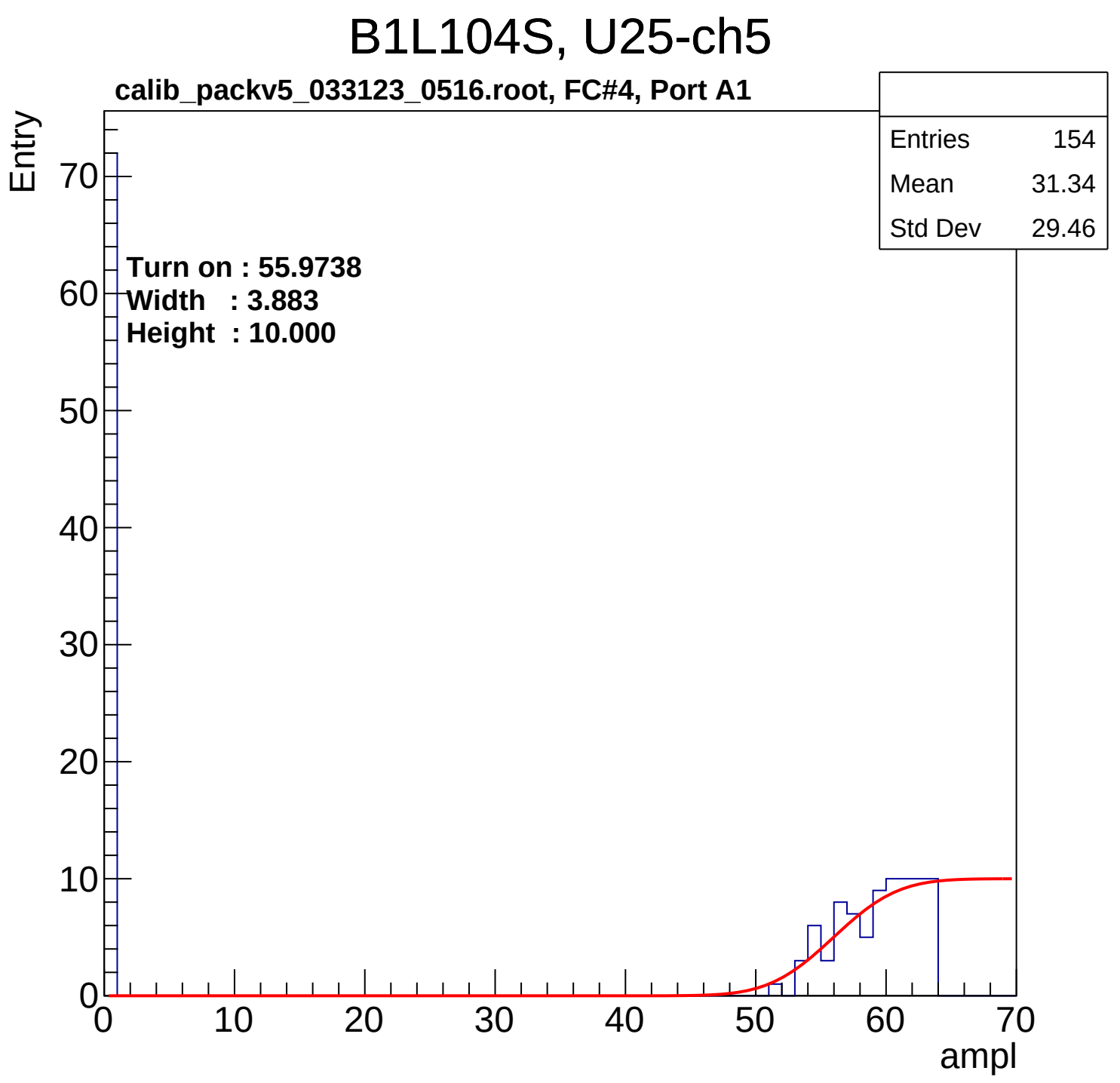
B1L104S, U25-ch5
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 154
Mean 31.34
Std Dev 29.46
Turn on : 55.9738
Width : 3.883
Height : 10.000
Entry
ampl
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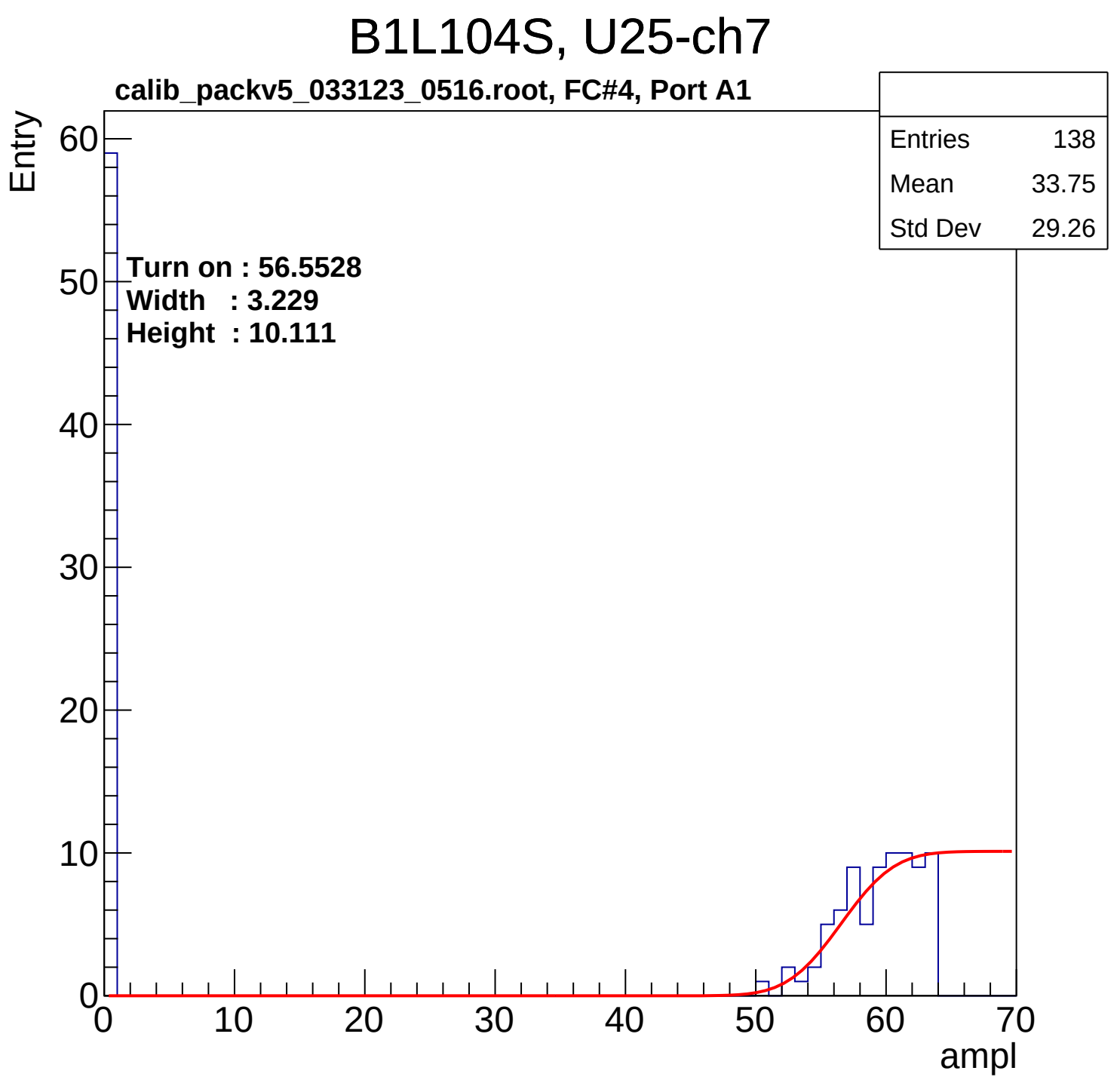
B1L104S, U25-ch7
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 138
Mean 33.75
Std Dev 29.26
Turn on : 56.5528
Width : 3.229
Height : 10.111
Entry
ampl
0
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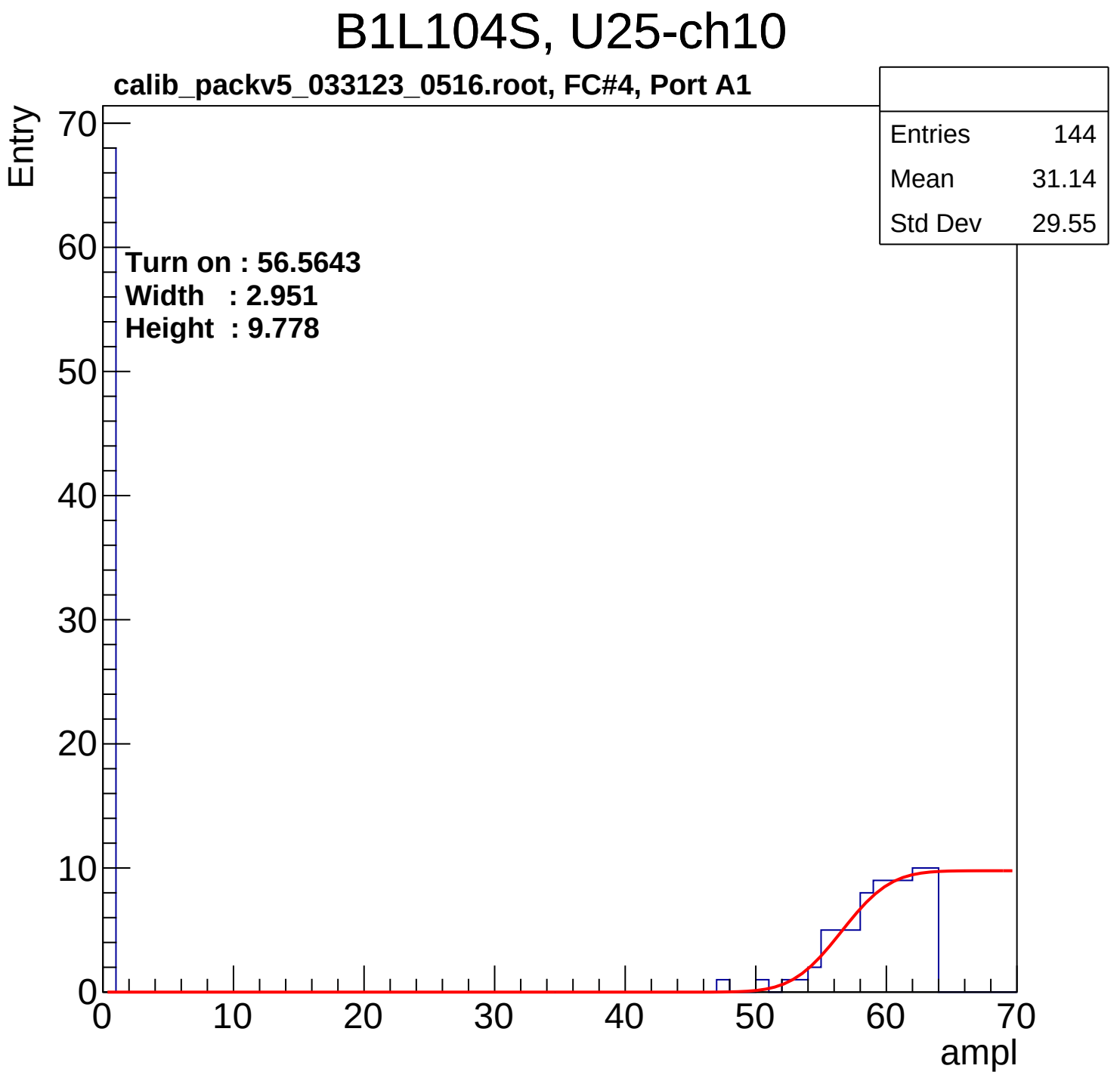
B1L104S, U25-ch10
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 144
Mean 31.14
Std Dev 29.55
Turn on : 56.5643
Width : 2.951
Height : 9.778
Entry
ampl
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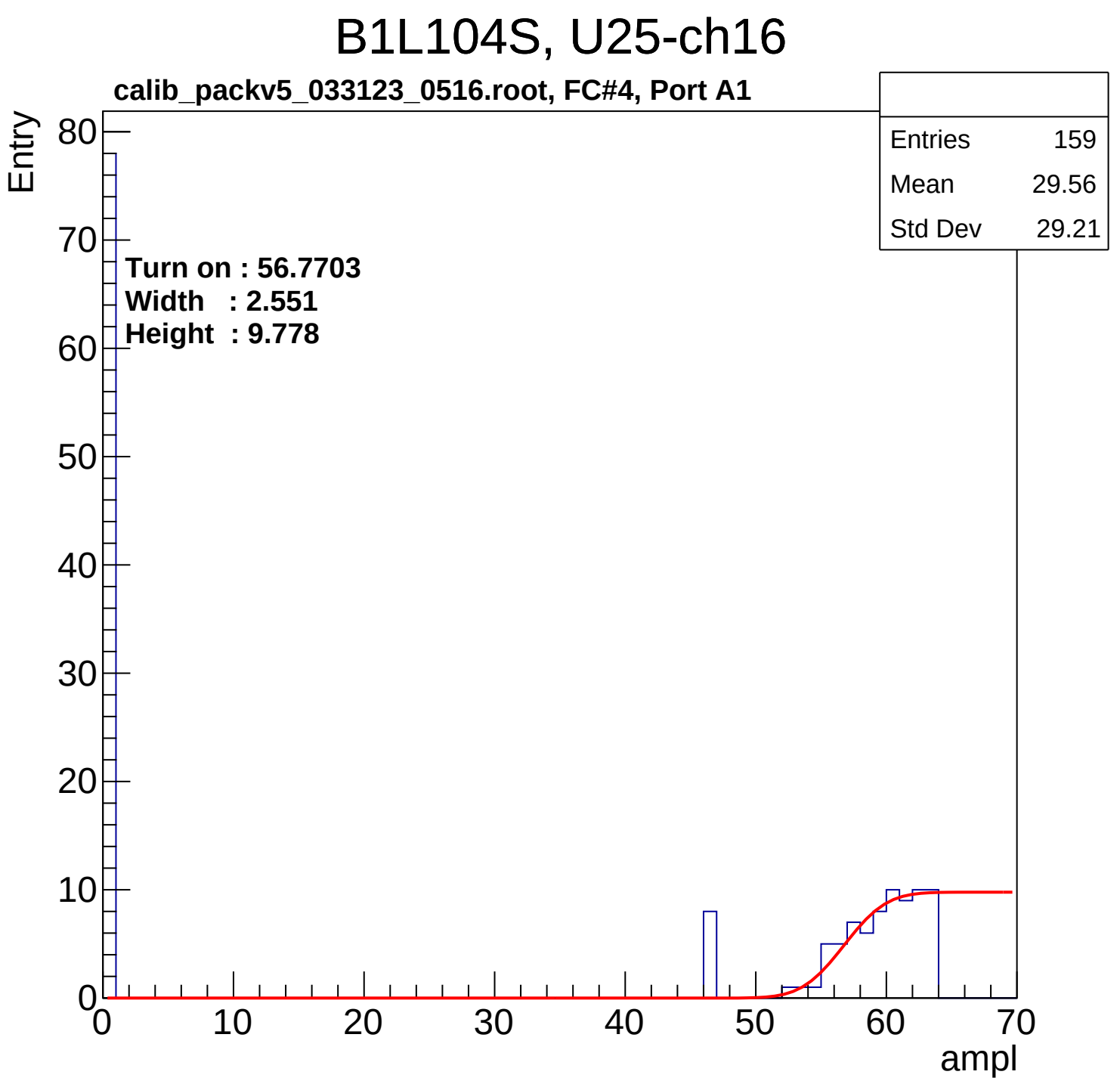
B1L104S, U25-ch16
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 159
Mean 29.56
Std Dev 29.21
Turn on : 56.7703
Width : 2.551
Height : 9.778
Entry
ampl
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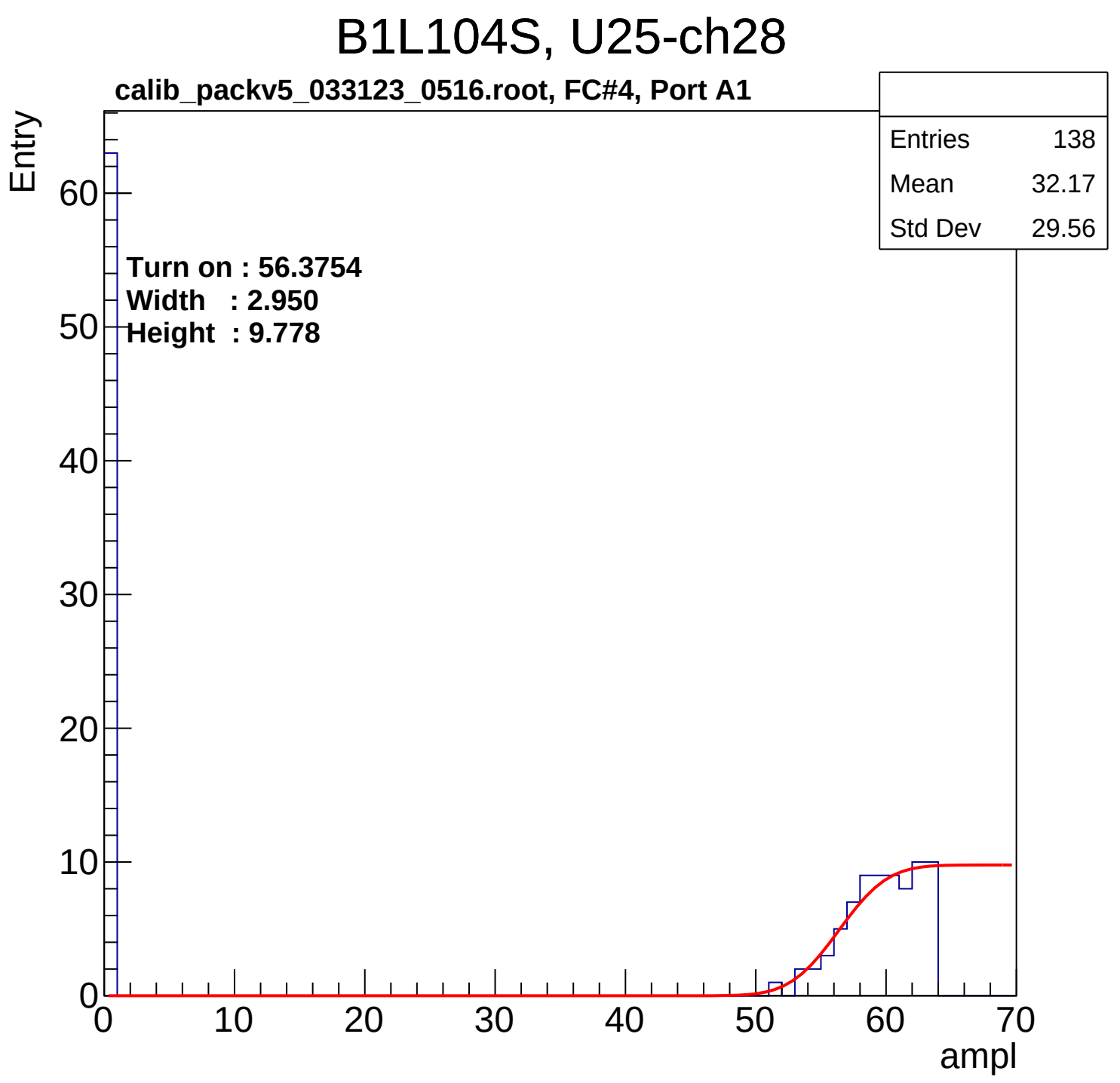
B1L104S, U25-ch28
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 138
Mean 32.17
Std Dev 29.56
Turn on : 56.3754
Width : 2.950
Height : 9.778
Entry
ampl
0
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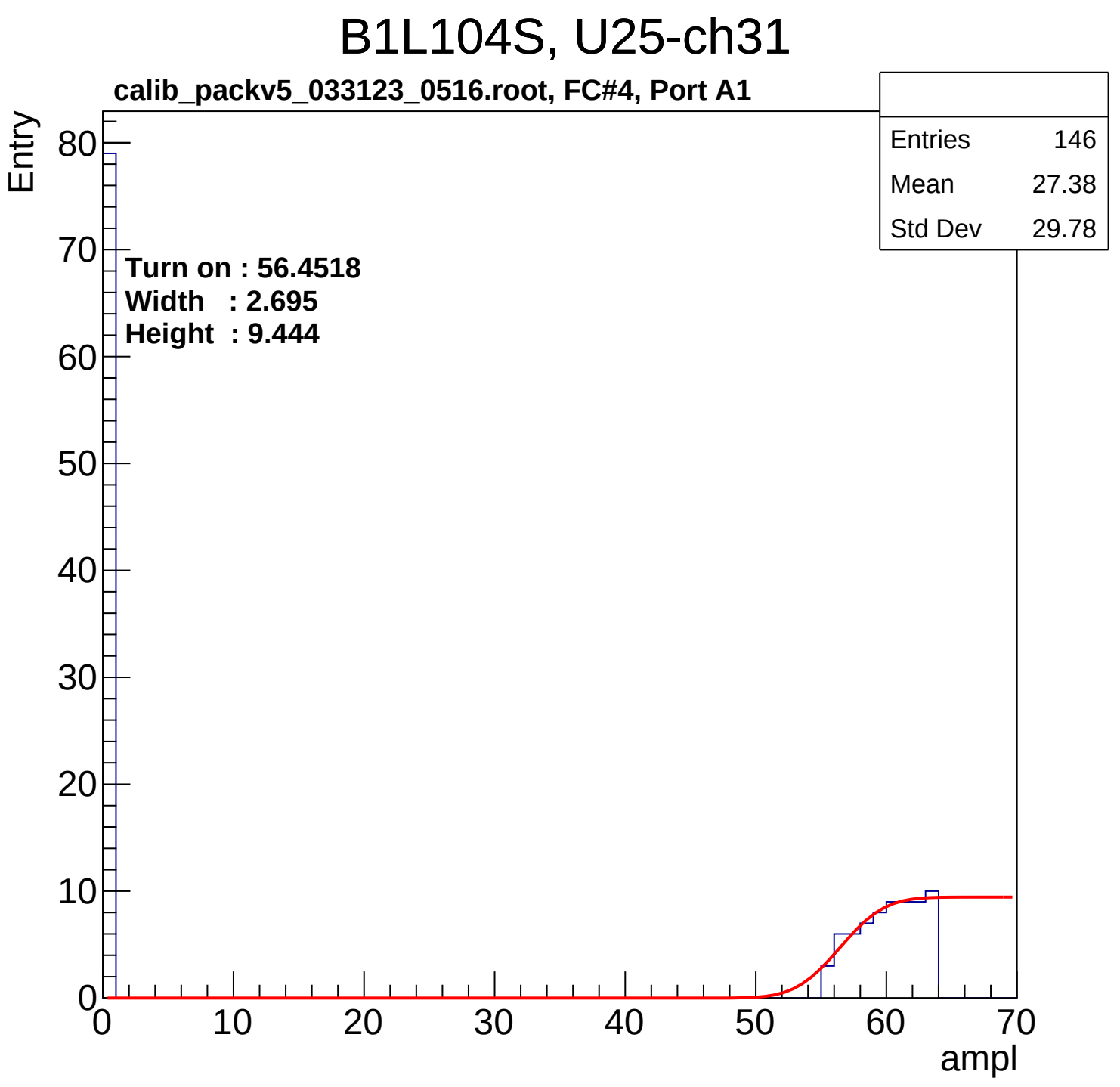
B1L104S, U25-ch31
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 146
Mean 27.38
Std Dev 29.78
Turn on : 56.4518
Width : 2.695
Height : 9.444
Entry
ampl
0
10
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30
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50
60
70
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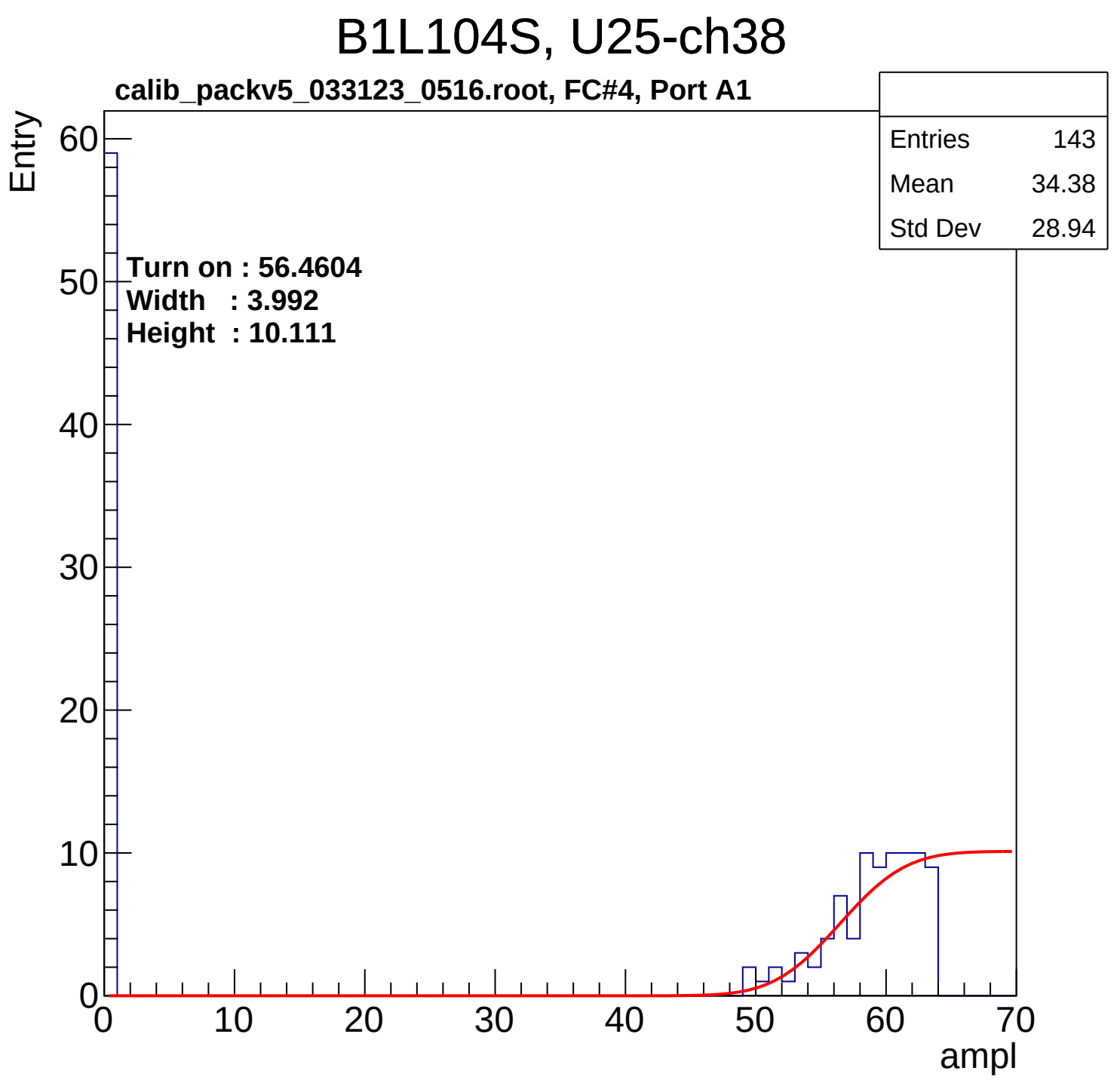
B1L104S, U25-ch38
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 143
Mean 34.38
Std Dev 28.94
Turn on : 56.4604
Width : 3.992
Height : 10.111
Entry
ampl
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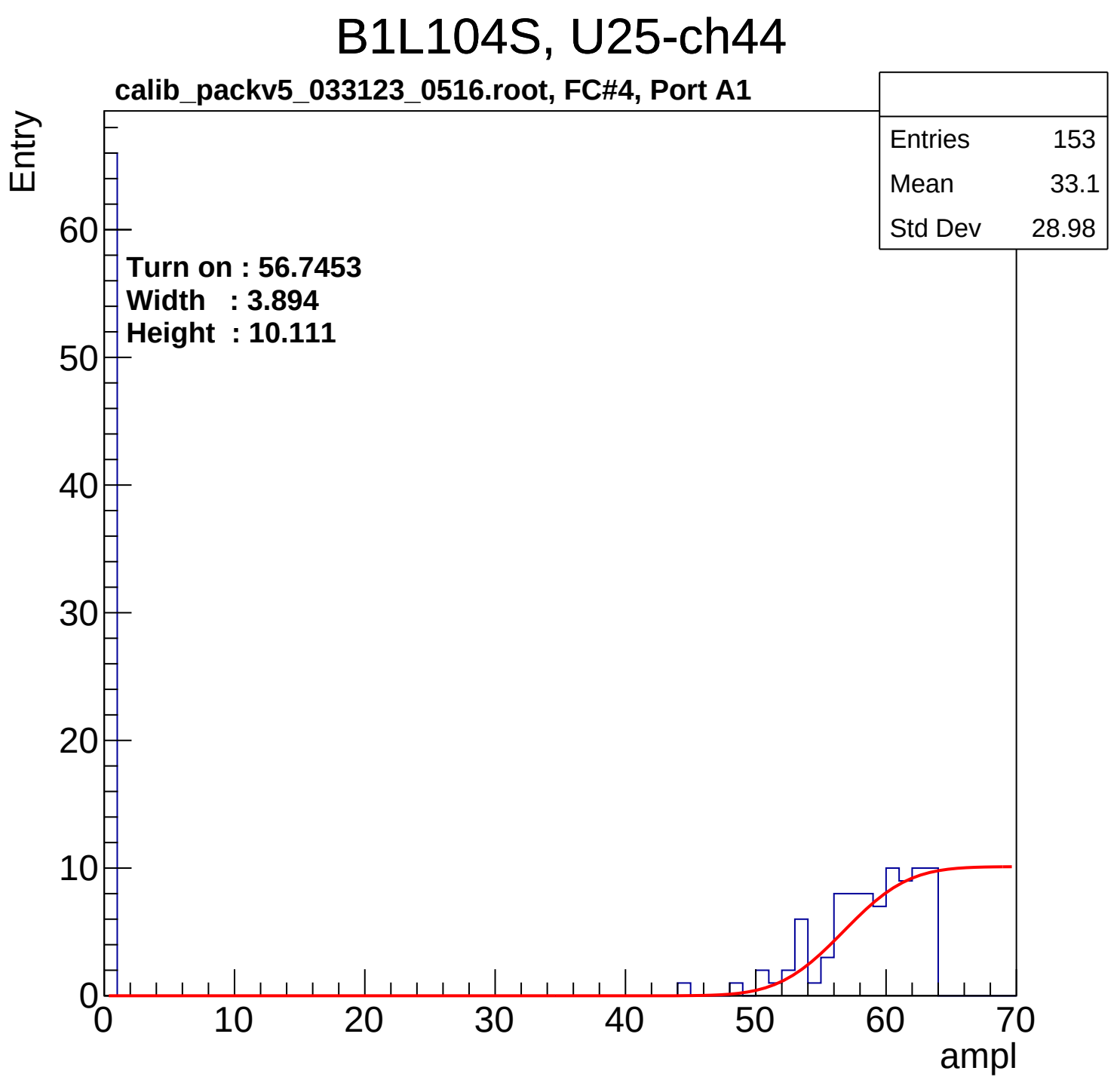
B1L104S, U25-ch44
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 153
Mean 33.1
Std Dev 28.98
Turn on : 56.7453
Width : 3.894
Height : 10.111
Entry
ampl
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40
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60
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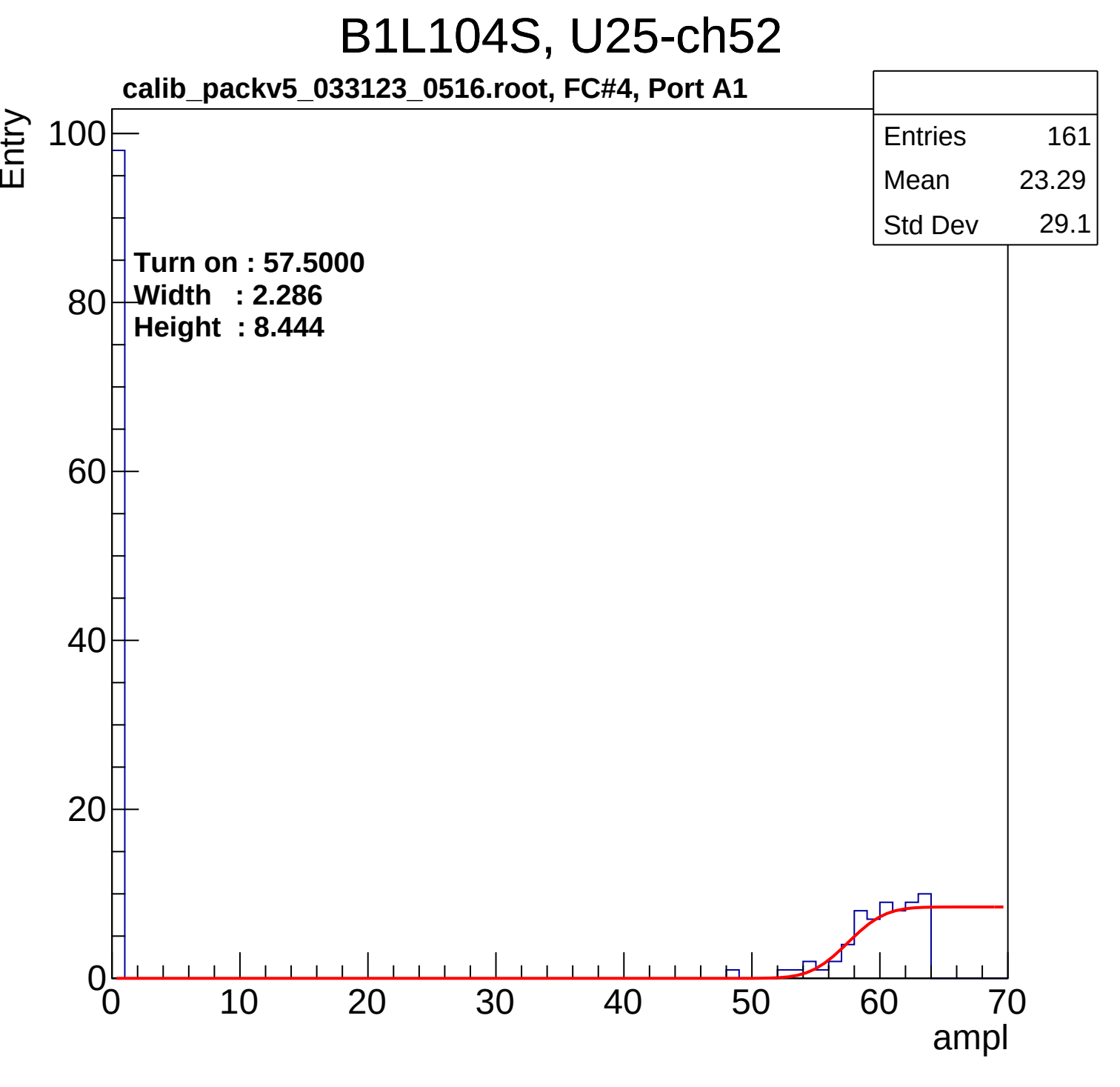
B1L104S, U25-ch52
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 161
Mean 23.29
Std Dev 29.1
Turn on : 57.5000
Width : 2.286
Height : 8.444
Entry
ampl
0
20
40
60
80
100
0
10
20
30
40
50
60
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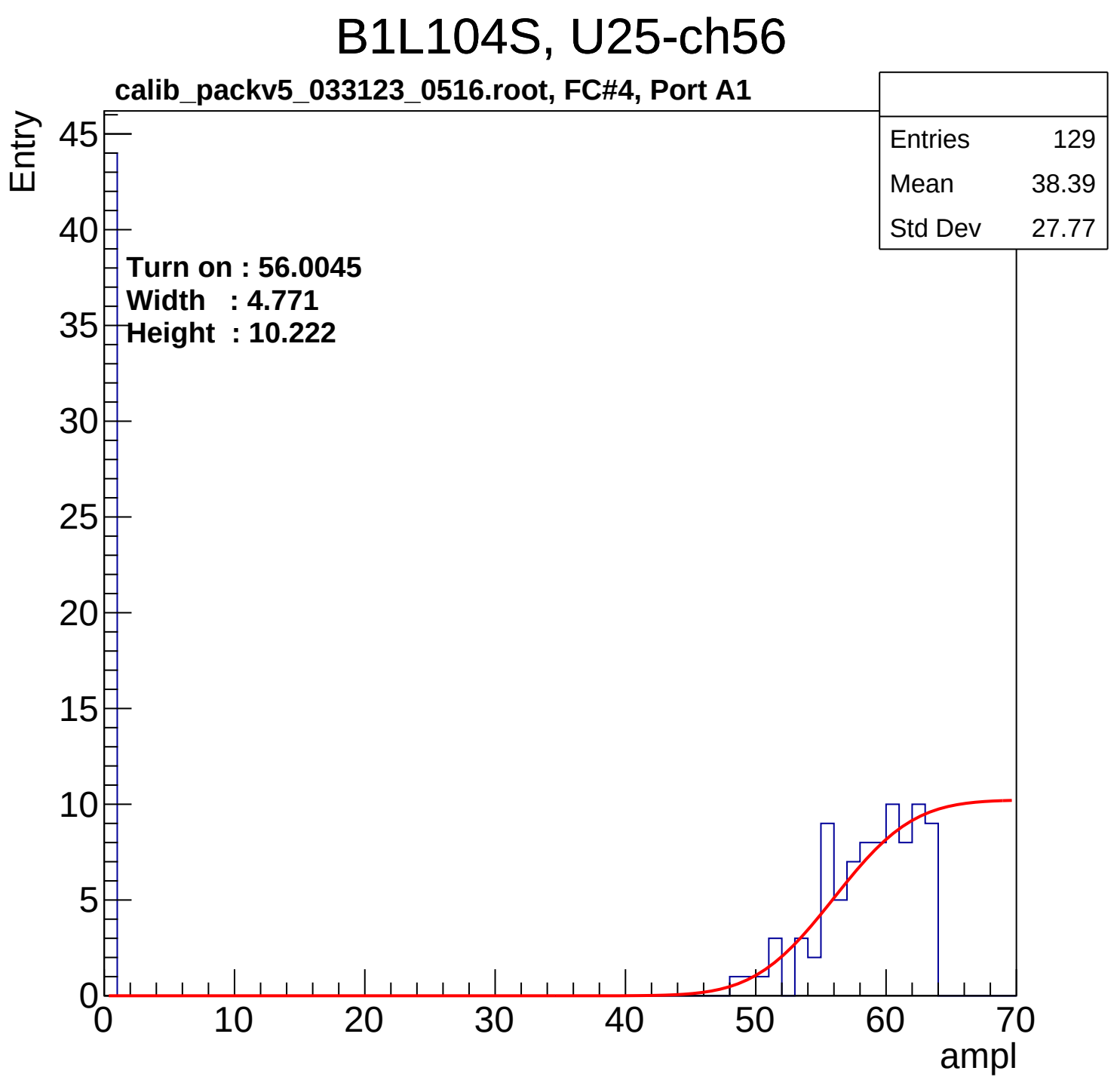
B1L104S, U25-ch56
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 129
Mean 38.39
Std Dev 27.77
Turn on : 56.0045
Width : 4.771
Height : 10.222
Entry
ampl
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10
15
20
25
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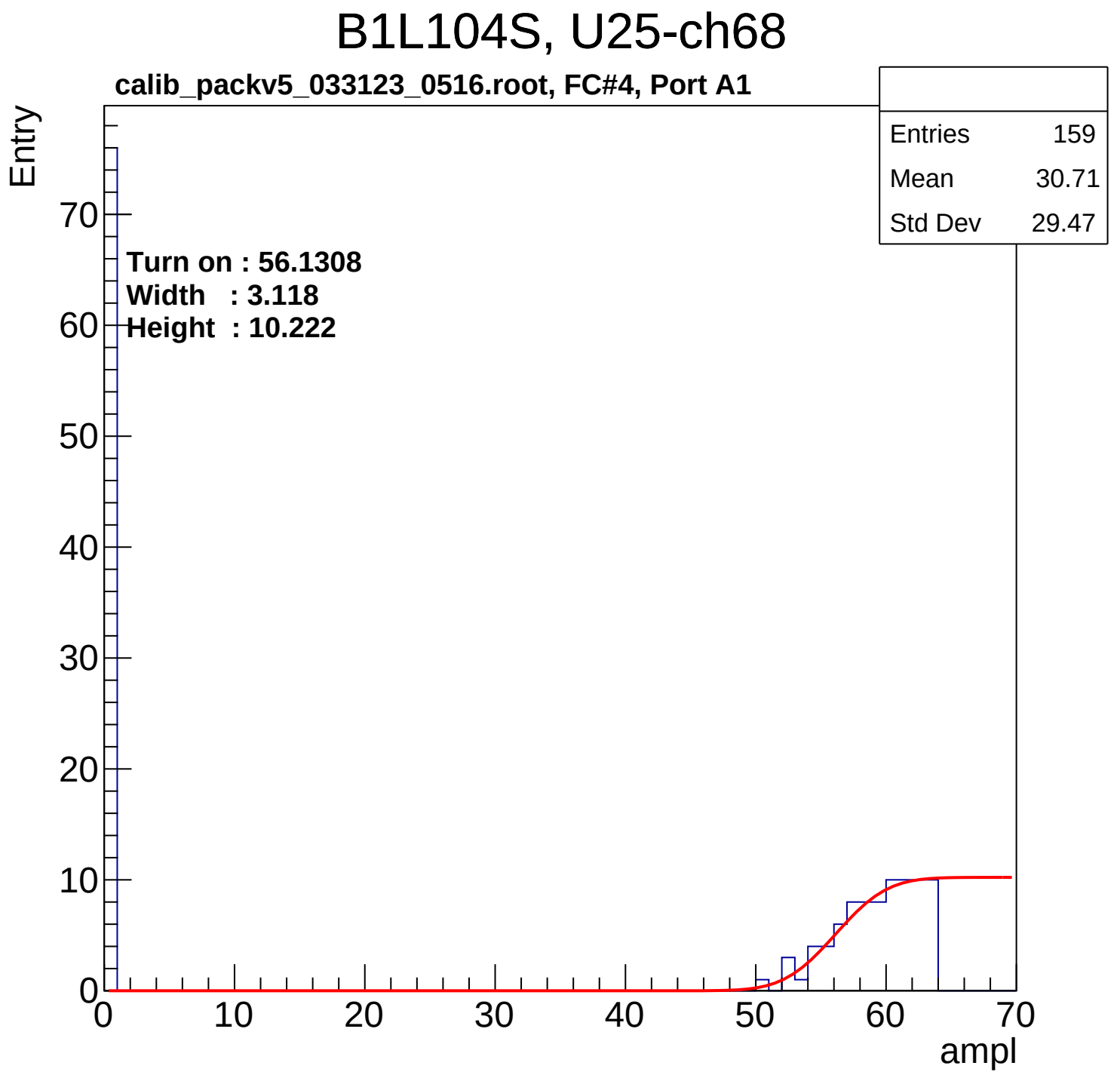
B1L104S, U25-ch68
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 159
Mean 30.71
Std Dev 29.47
Turn on : 56.1308
Width : 3.118
Height : 10.222
Entry
ampl
0
10
20
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40
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60
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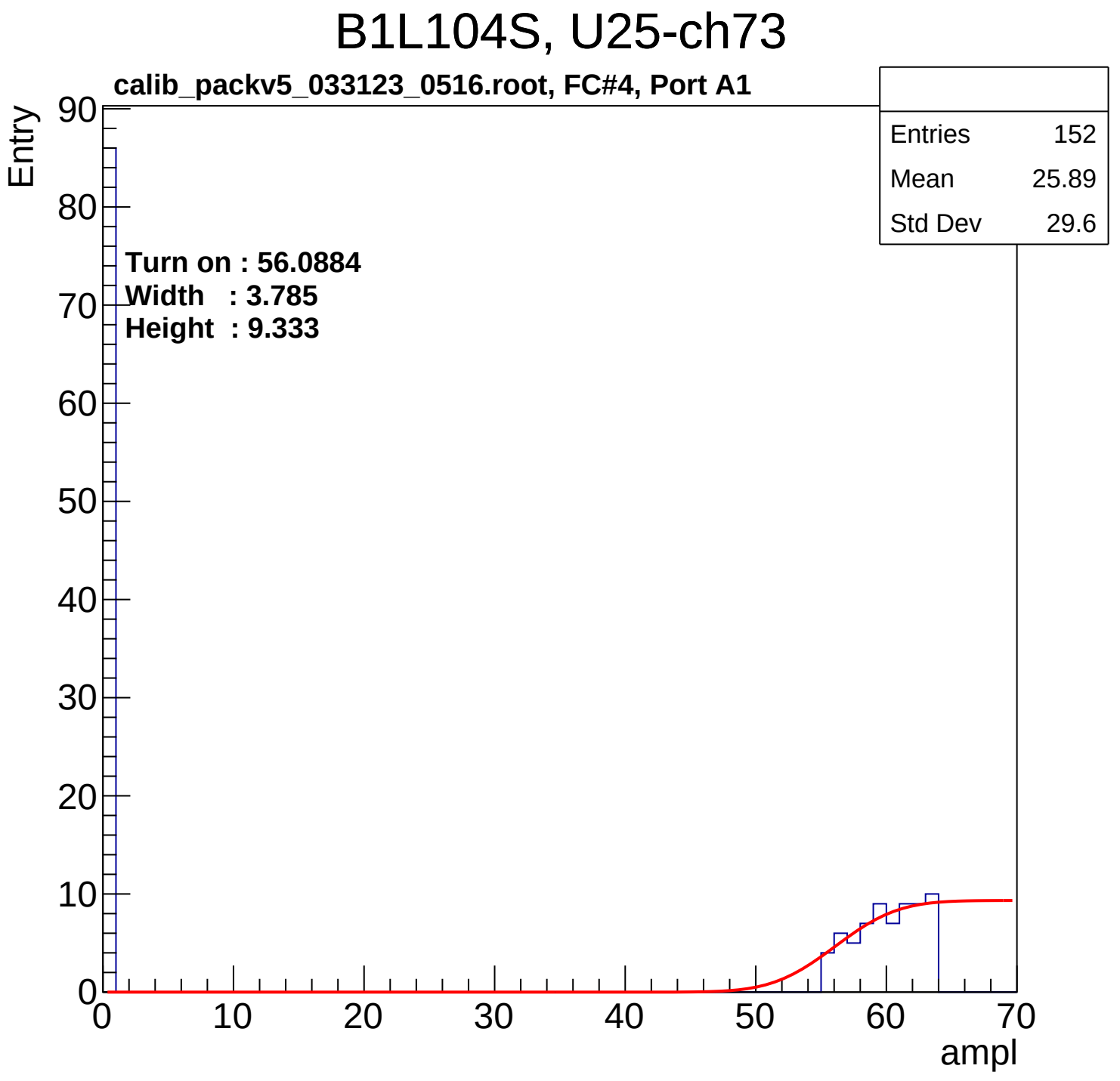
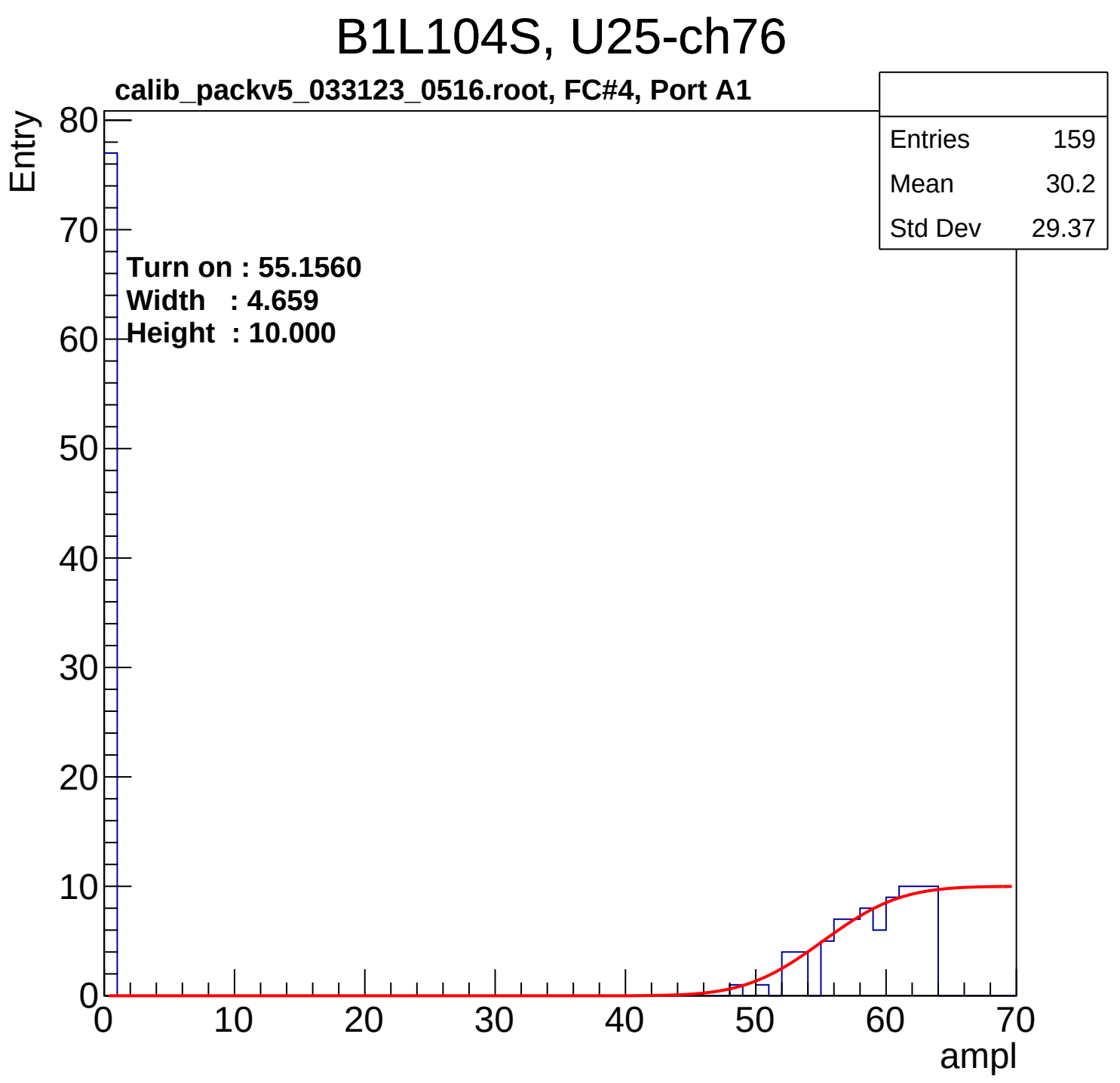

B1L104S, U25-ch73
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 152
Mean 25.89
Std Dev 29.6
Turn on : 56.0884
Width : 3.785
Height : 9.333
Entry
ampl
0
10
20
30
40
50
60
70
80
90


B1L104S, U25-ch76
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 159
Mean 30.2
Std Dev 29.37
Turn on : 55.1560
Width : 4.659
Height : 10.000
Entry
ampl
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10
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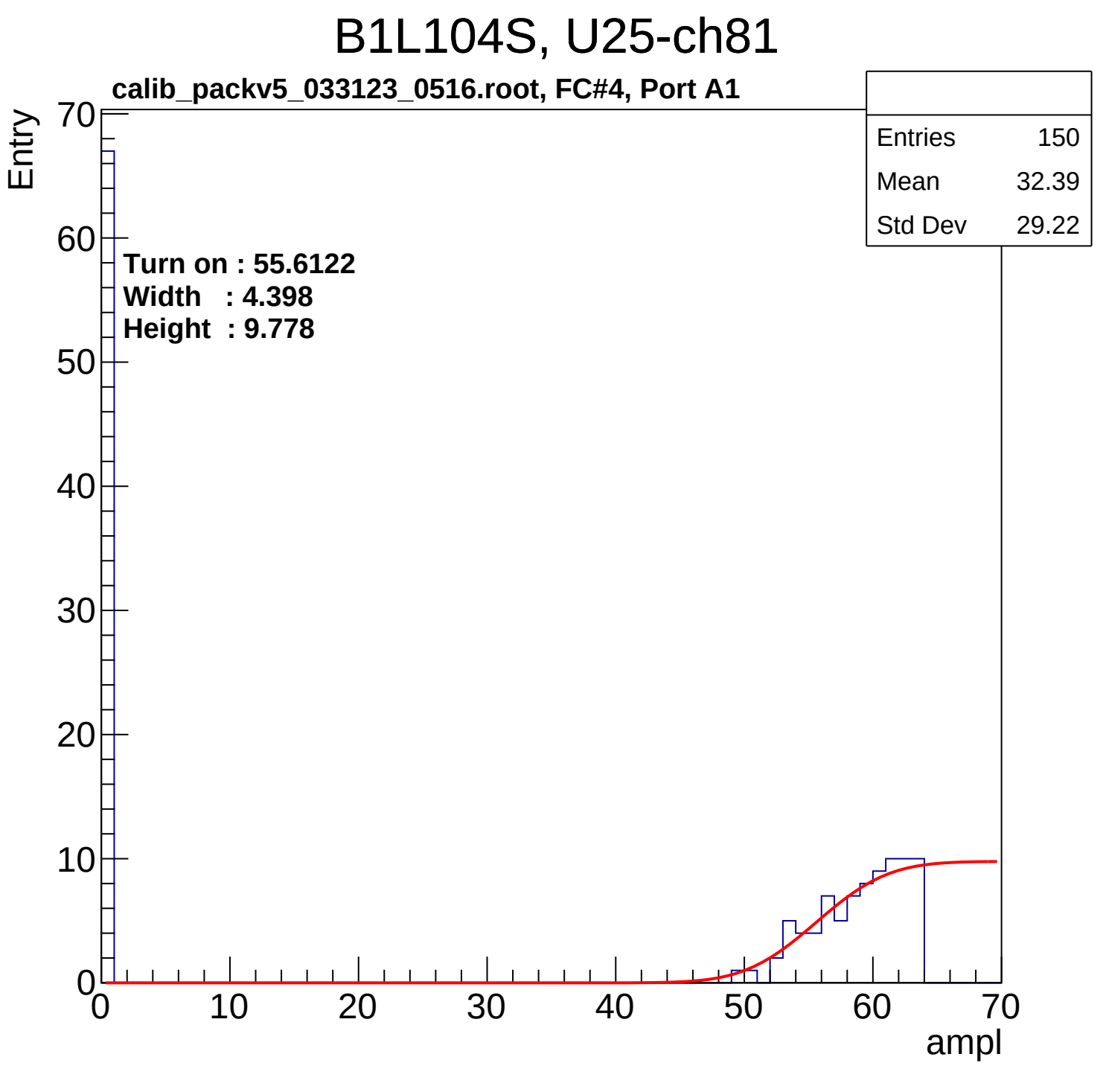
30
40
50
60
70
80


B1L104S, U25-ch81
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 150
Mean 32.39
Std Dev 29.22
Turn on : 55.6122
Width : 4.398
Height : 9.778
Entry
ampl
0
10
20
30
40
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60
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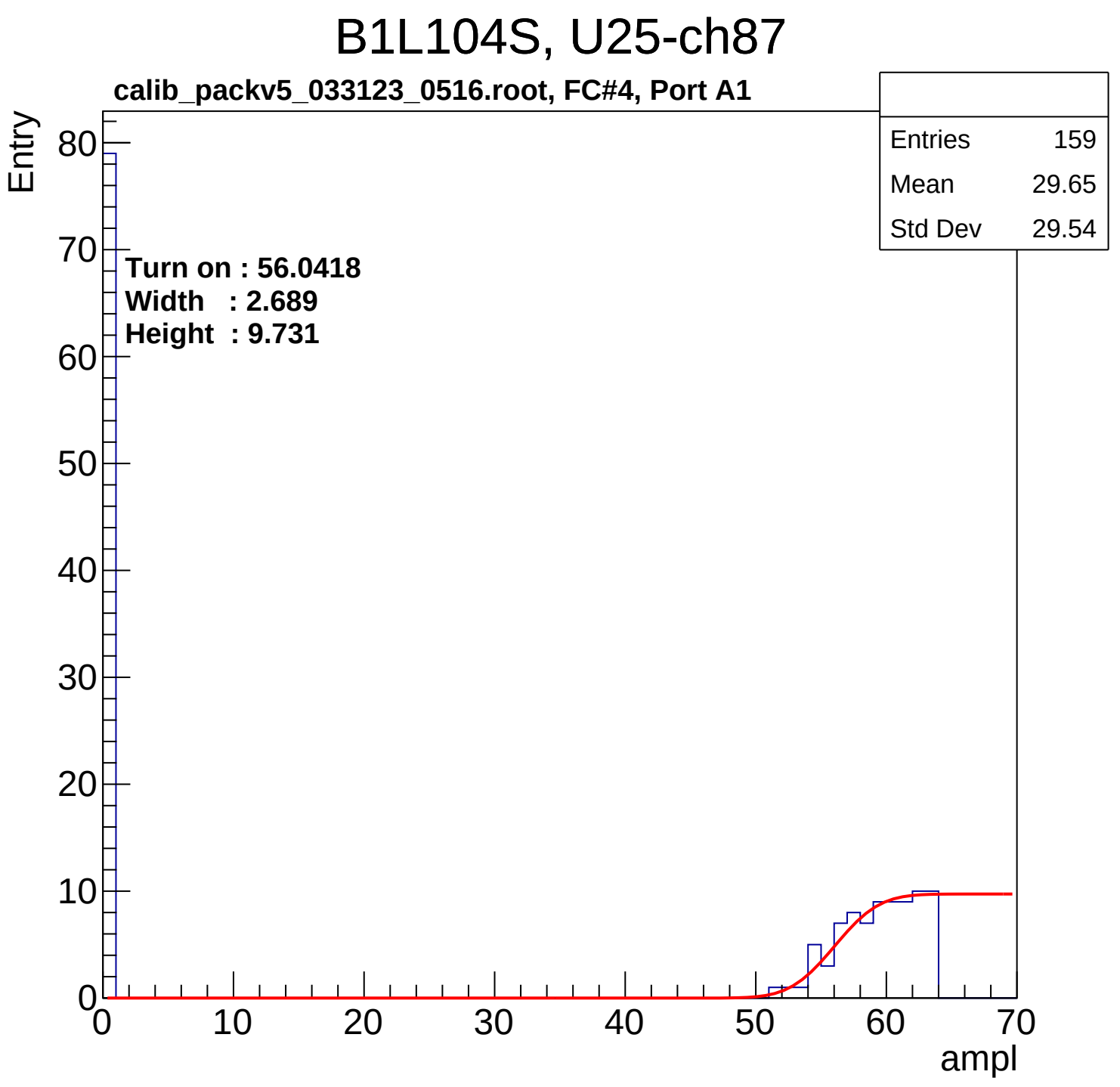
B1L104S, U25-ch87
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 159
Mean 29.65
Std Dev 29.54
Turn on : 56.0418
Width : 2.689
Height : 9.731
Entry
ampl
0
10
20
30
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50
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70
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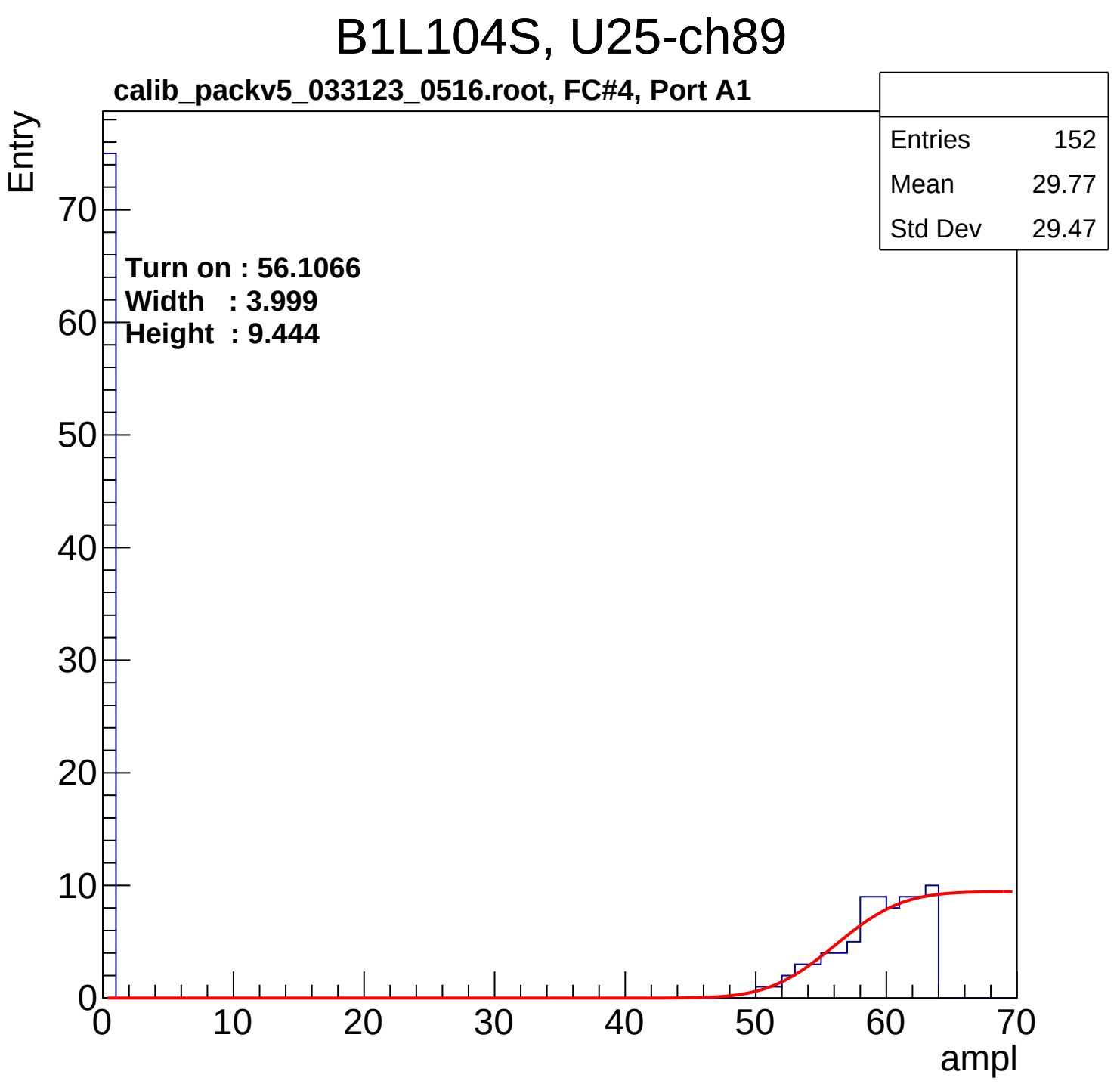
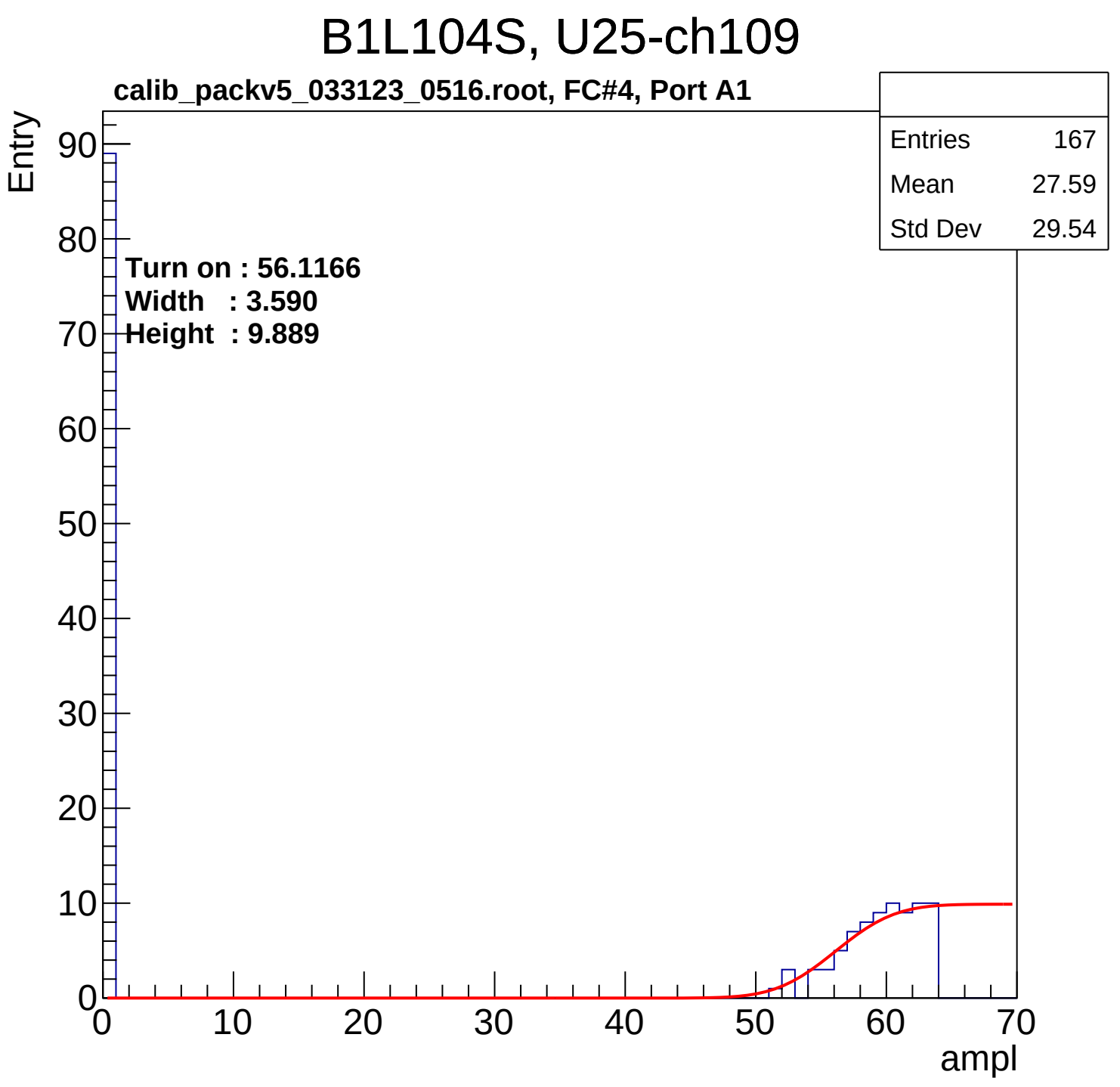
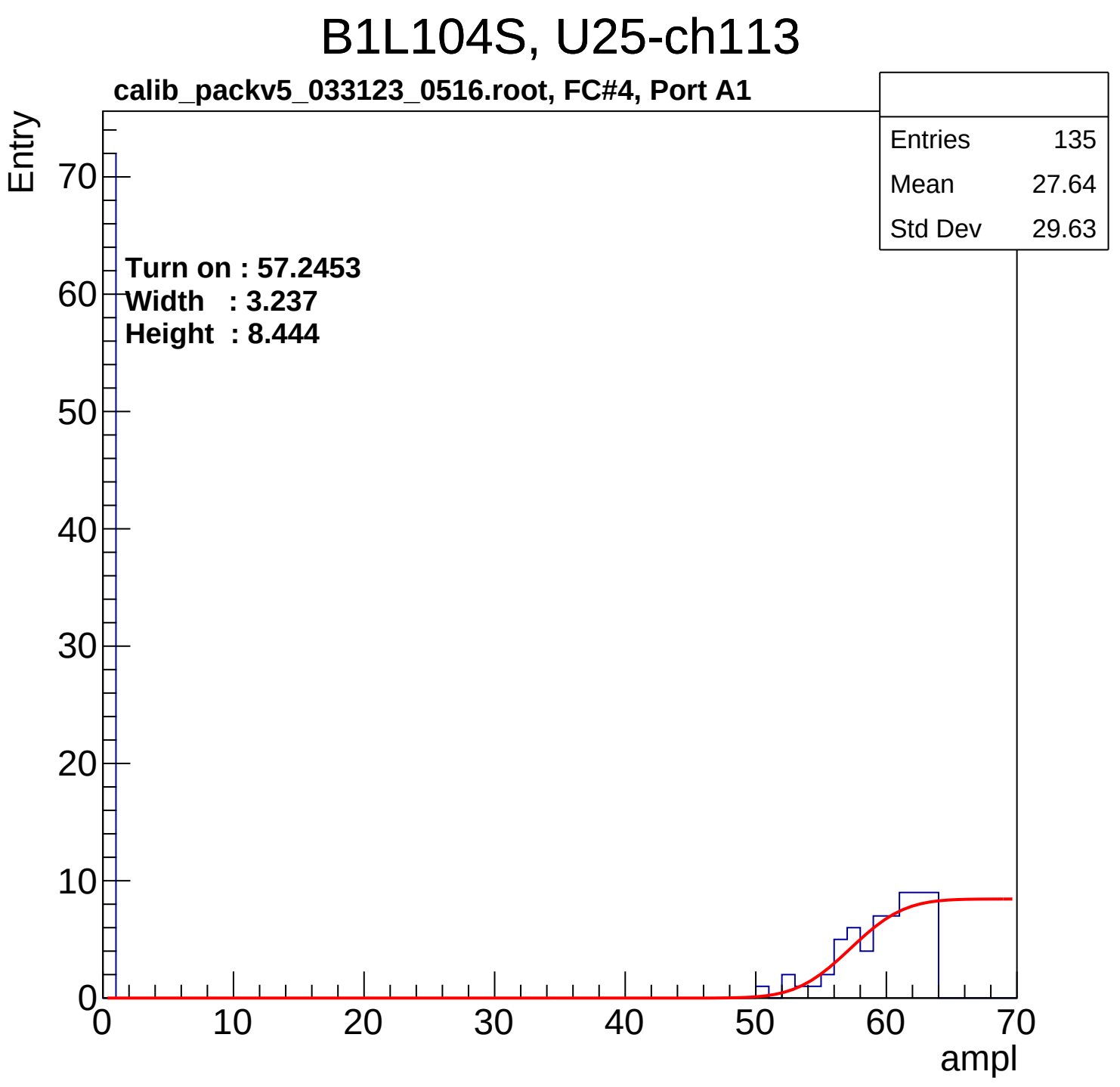
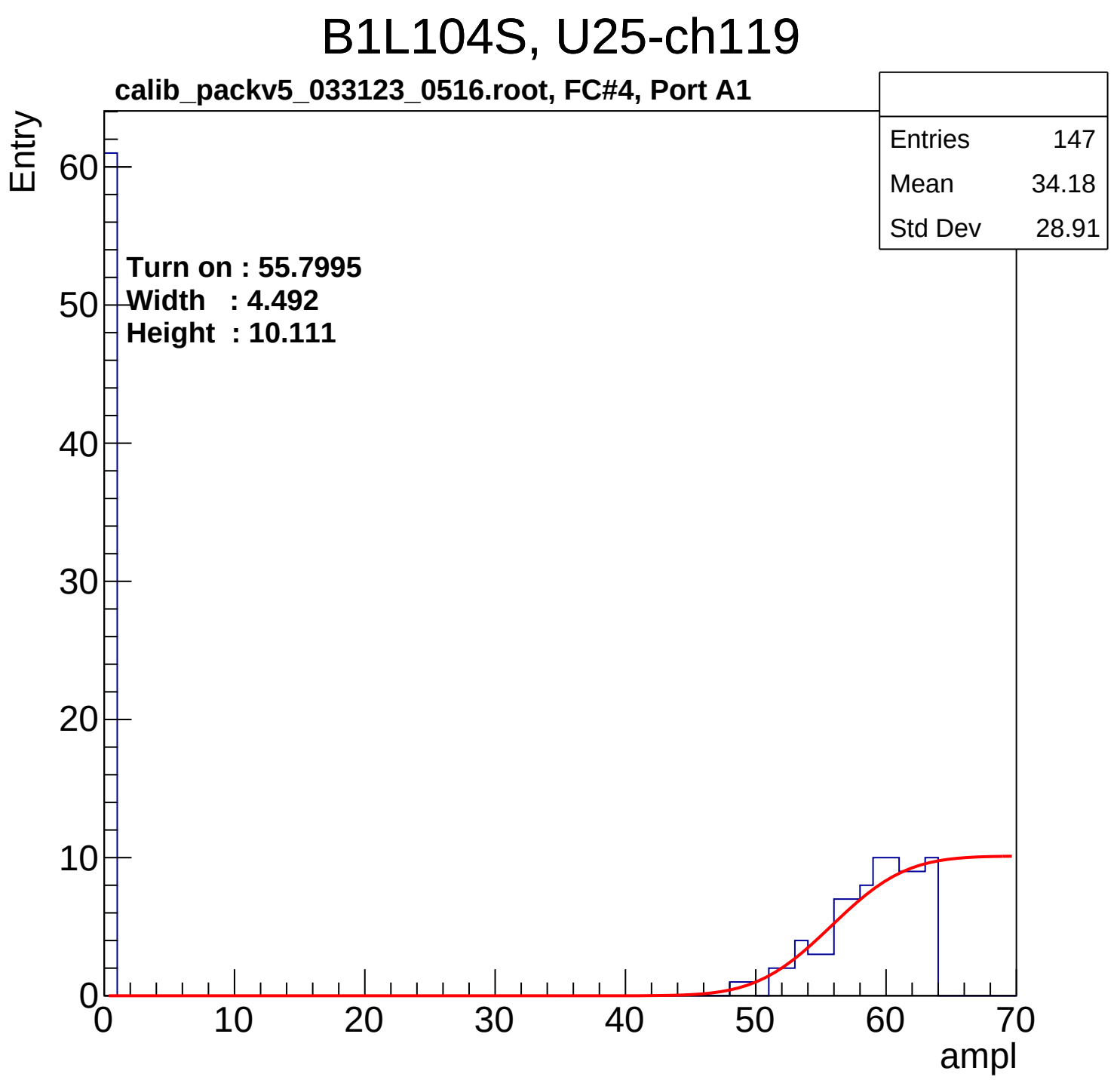
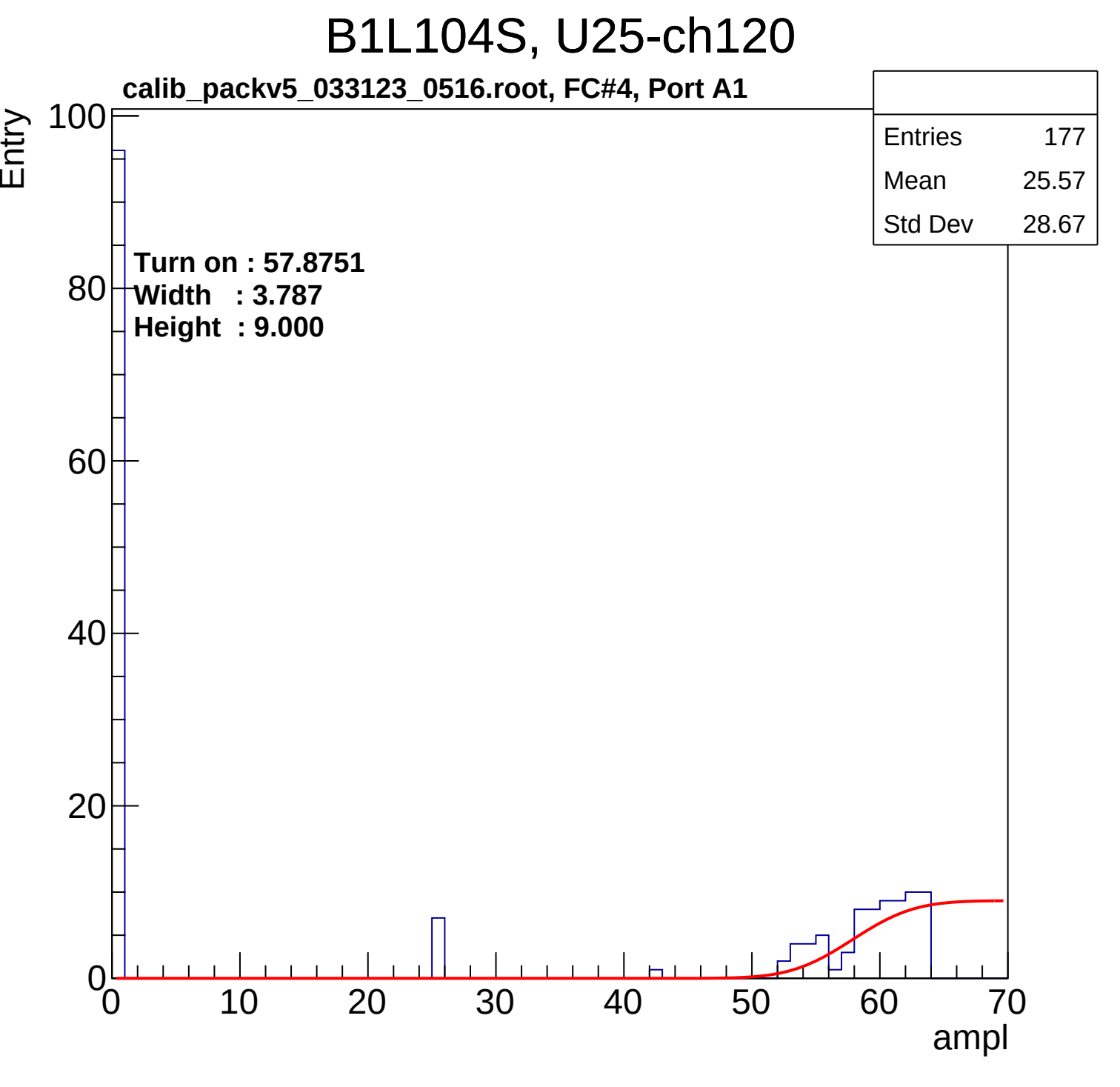
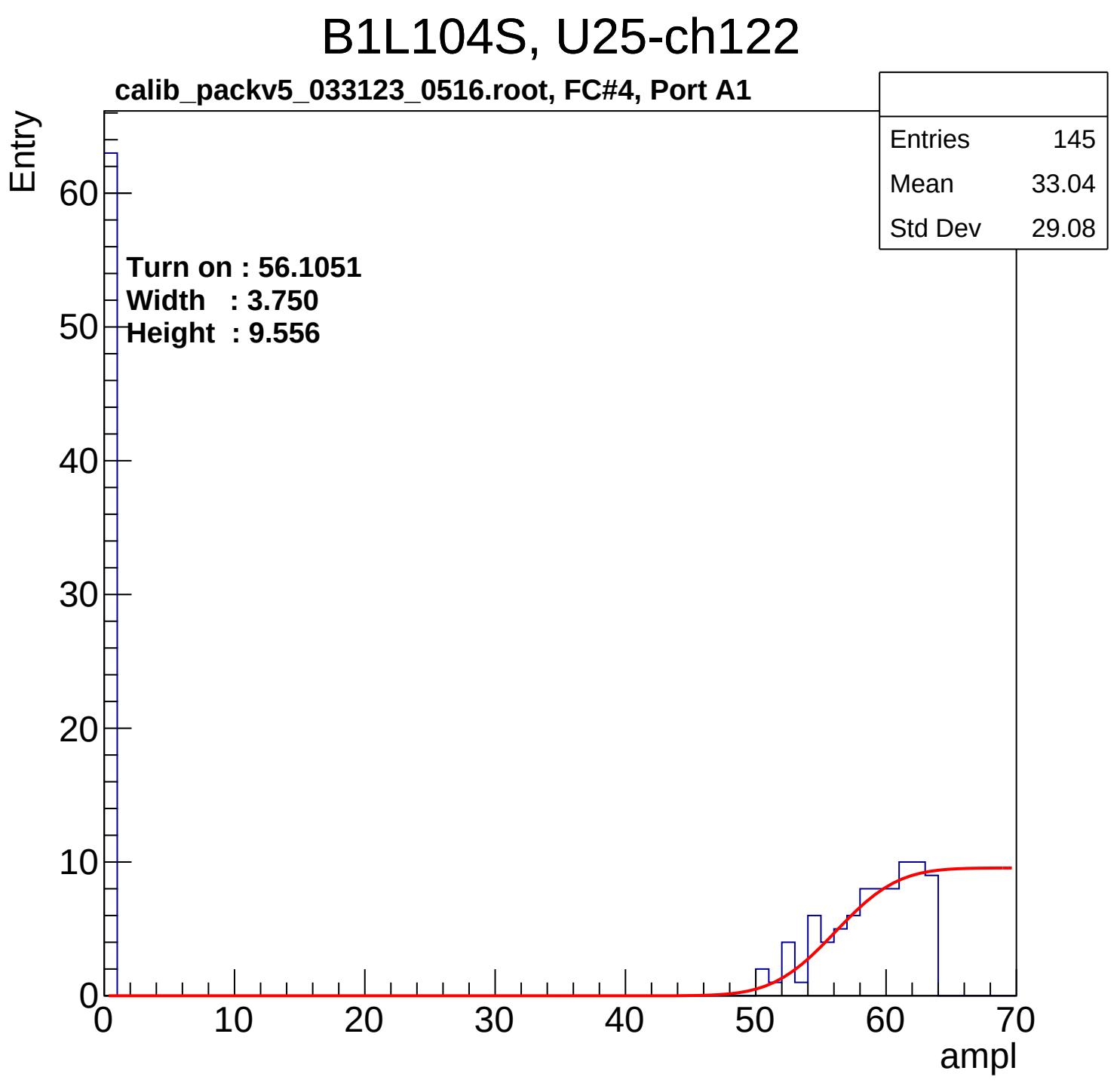

B1L104S, U25-ch89
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 152
Mean 29.77
Std Dev 29.47
Turn on : 56.1066
Width : 3.999
Height : 9.444
Entry
ampl
0
10
20
30
40
50
60
70


B1L104S, U25-ch109
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 167
Mean 27.59
Std Dev 29.54
Turn on : 56.1166
Width : 3.590
Height : 9.889
Entry
ampl
0
10
20
30
40
50
60
70
80
90


B1L104S, U25-ch113
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 135
Mean 27.64
Std Dev 29.63
Turn on : 57.2453
Width : 3.237
Height : 8.444
Entry
ampl
0
10
20
30
40
50
60
70


B1L104S, U25-ch119
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 147
Mean 34.18
Std Dev 28.91
Turn on : 55.7995
Width : 4.492
Height : 10.111
Entry
ampl
0
10
20
30
40
50
60
70


B1L104S, U25-ch120
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 177
Mean 25.57
Std Dev 28.67
Turn on : 57.8751
Width : 3.787
Height : 9.000
Entry
ampl
0
20
40
60
80
100
0
10
20
30
40
50
60
70


B1L104S, U25-ch122
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 145
Mean 33.04
Std Dev 29.08
Turn on : 56.1051
Width : 3.750
Height : 9.556
Entry
ampl
0
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20
30
40
50
60
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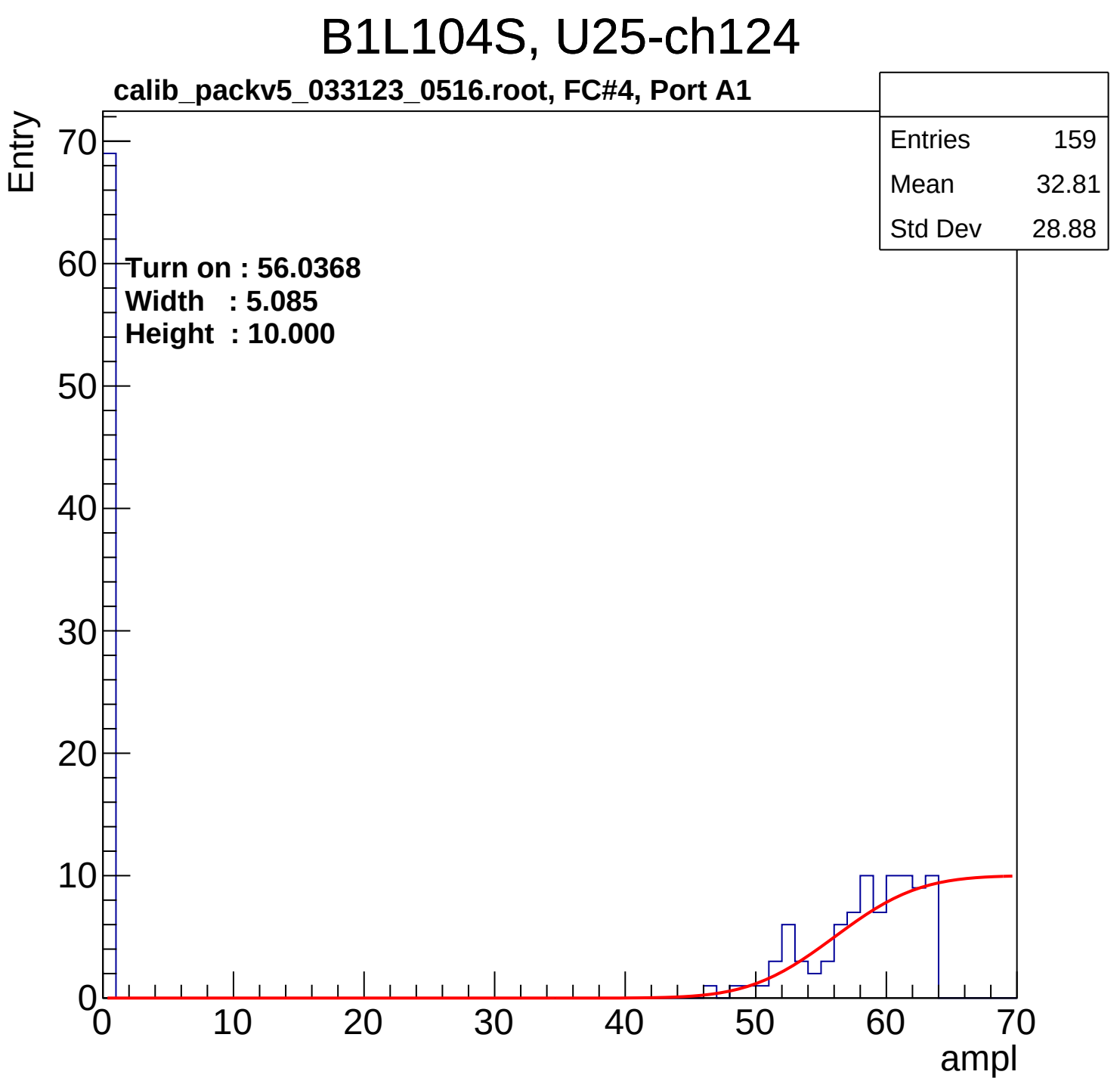
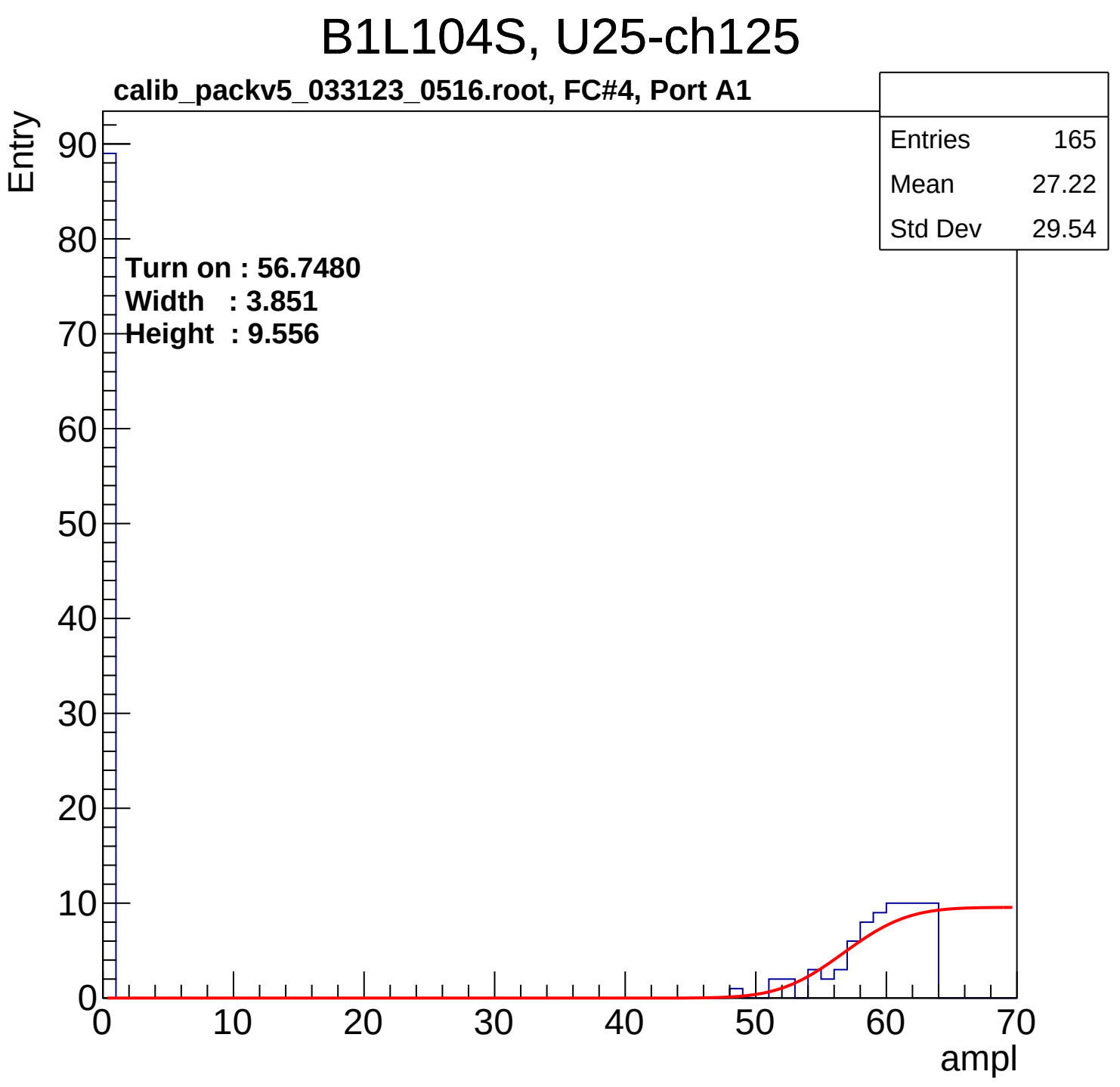
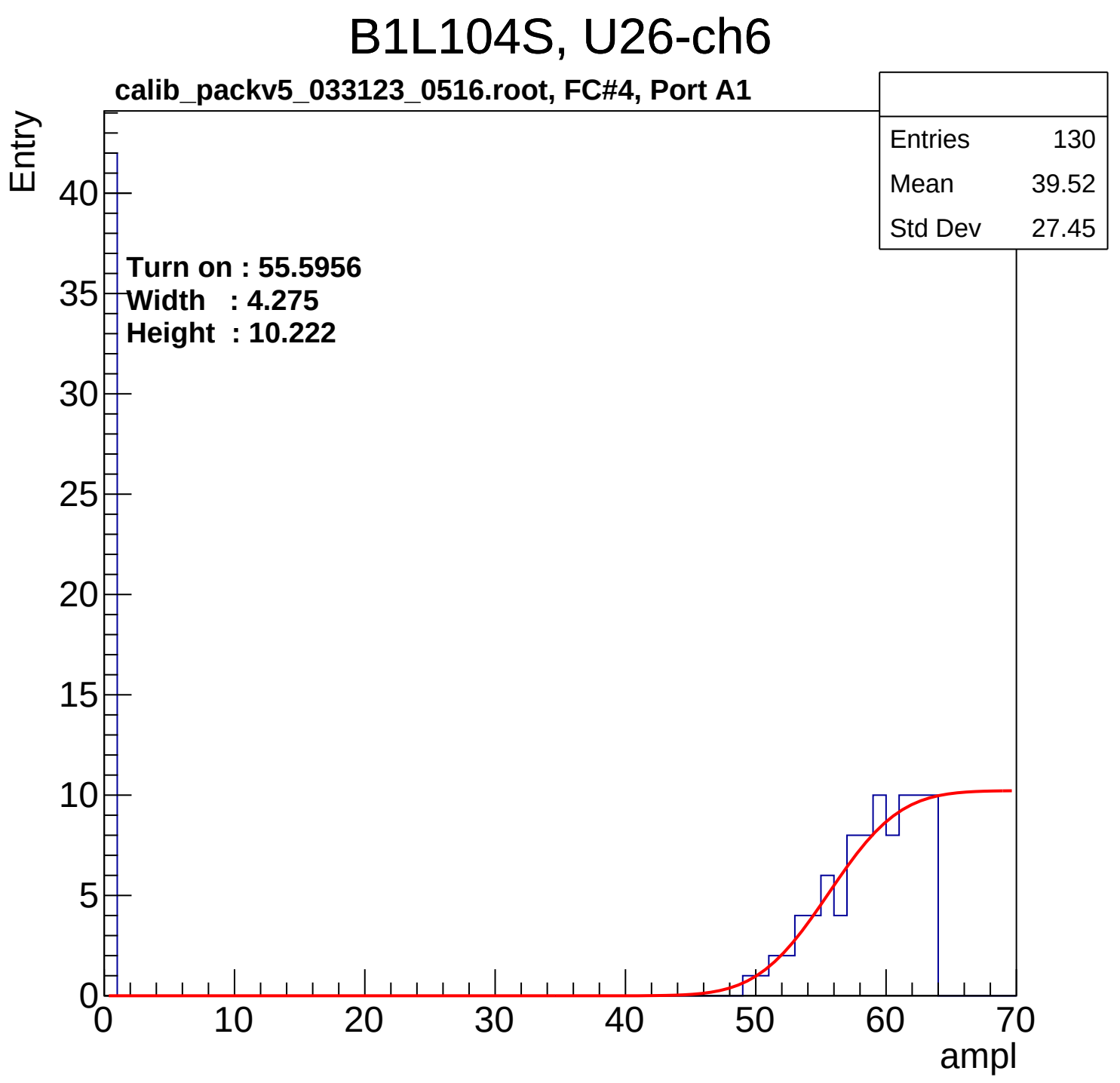

B1L104S, U25-ch124
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 159
Mean 32.81
Std Dev 28.88
Turn on : 56.0368
Width : 5.085
Height : 10.000
Entry
ampl
0
10
20
30
40
50
60
70


B1L104S, U25-ch125
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 165
Mean 27.22
Std Dev 29.54
Turn on : 56.7480
Width : 3.851
Height : 9.556
Entry
ampl
0
10
20
30
40
50
60
70
80
90


B1L104S, U26-ch6
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 130
Mean 39.52
Std Dev 27.45
Turn on : 55.5956
Width : 4.275
Height : 10.222
Entry
ampl
0
5
10
15
20
25
30
35
40
0
10
20
30
40
50
60
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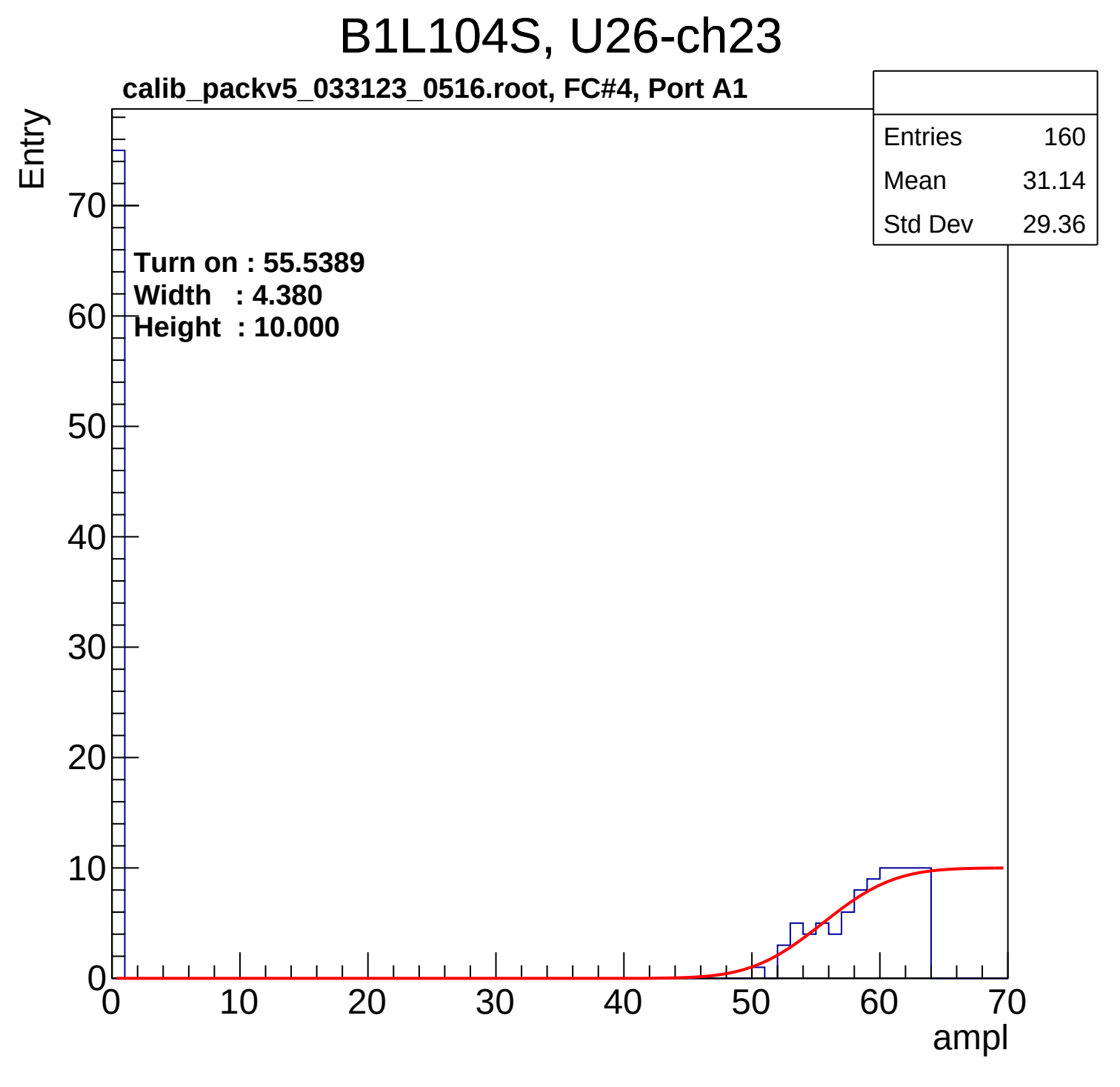
B1L104S, U26-ch23
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 160
Mean 31.14
Std Dev 29.36
Turn on : 55.5389
Width : 4.380
Height : 10.000
Entry
ampl
0
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20
30
40
50
60
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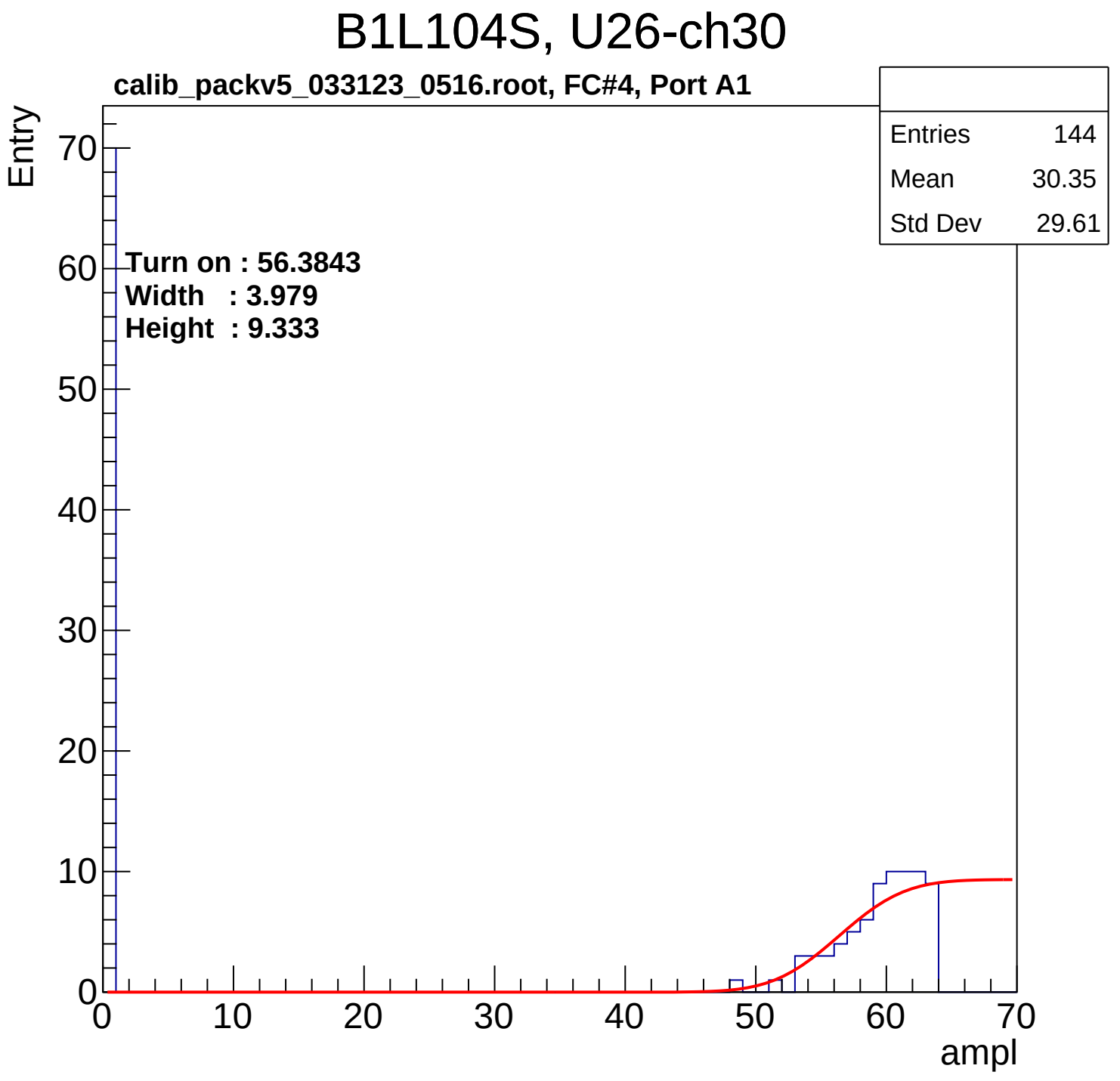
B1L104S, U26-ch30
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 144
Mean 30.35
Std Dev 29.61
Turn on : 56.3843
Width : 3.979
Height : 9.333
Entry
ampl
0
10
20
30
40
50
60
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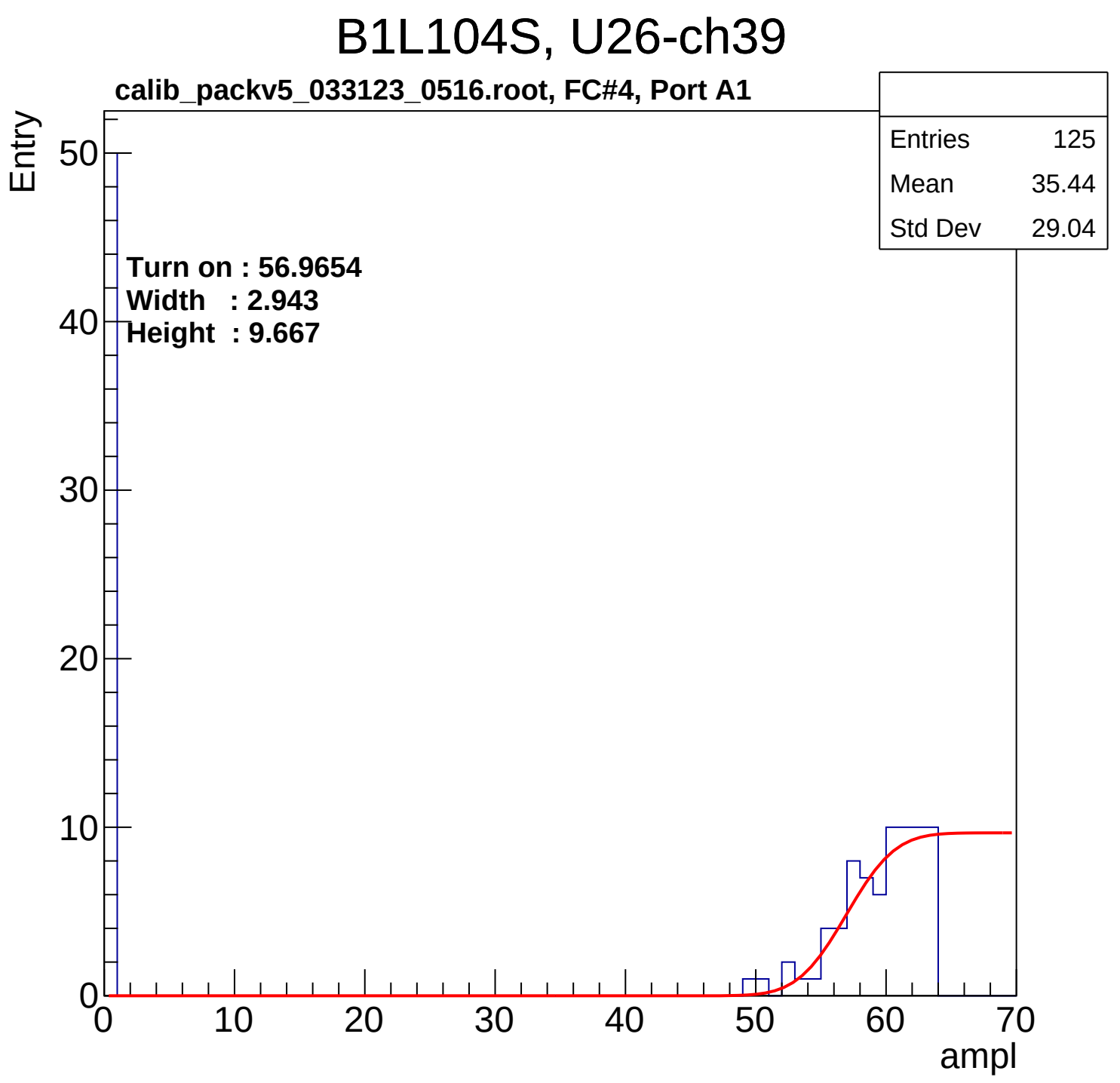
B1L104S, U26-ch39
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 125
Mean 35.44
Std Dev 29.04
Turn on : 56.9654
Width : 2.943
Height : 9.667
Entry
ampl
0
10
20
30
40
50
60
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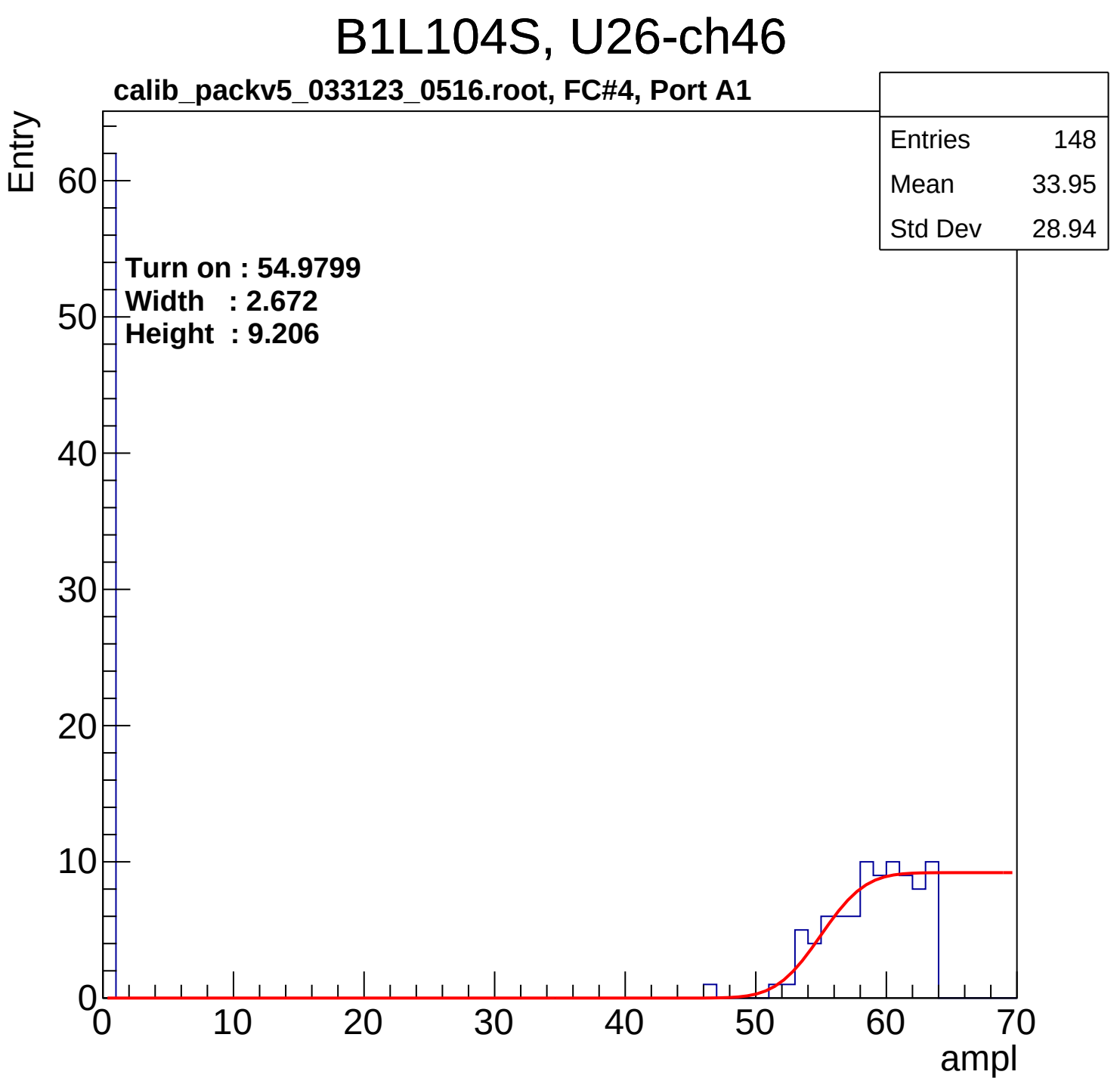
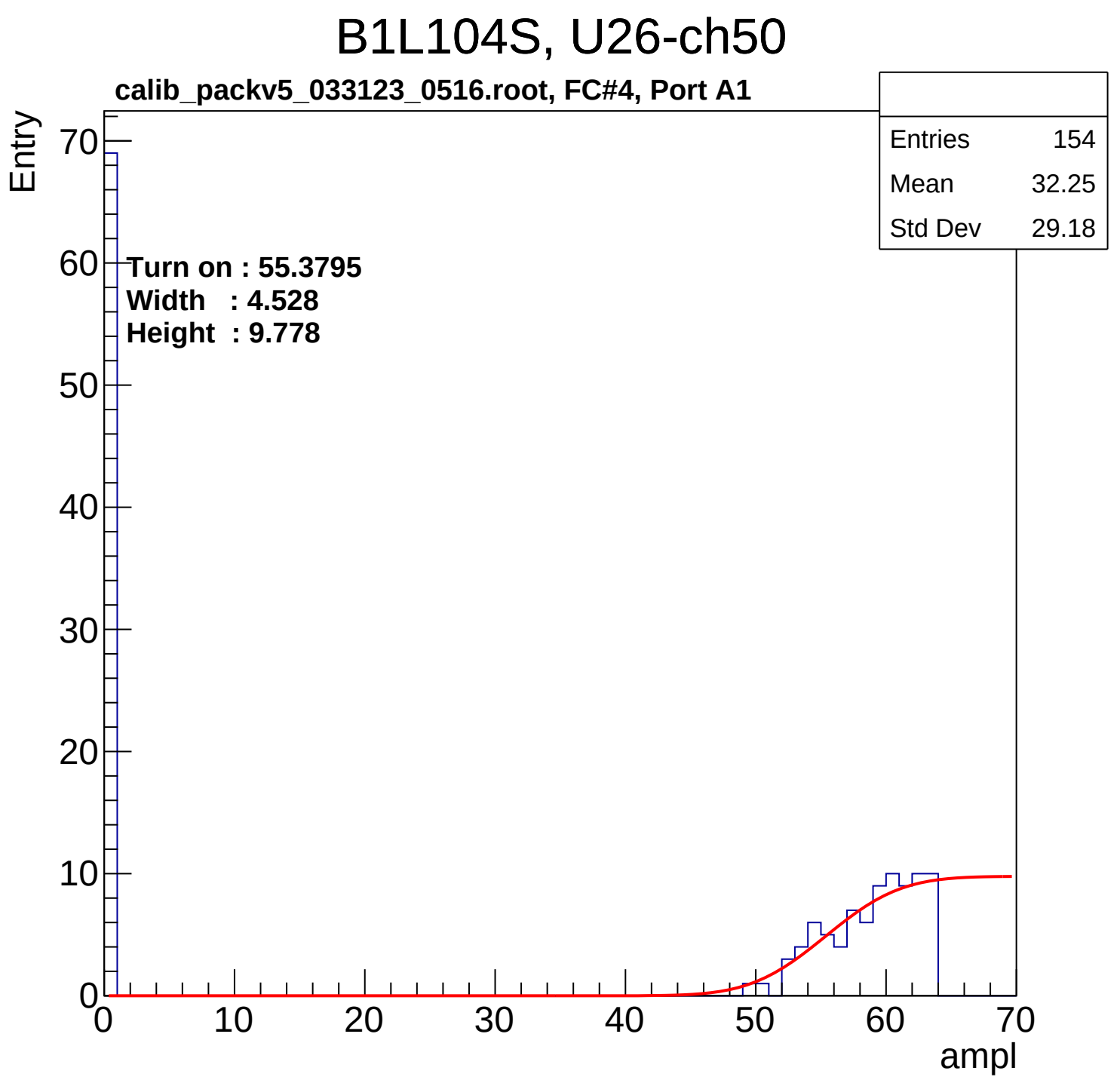

B1L104S, U26-ch46
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 148
Mean 33.95
Std Dev 28.94
Turn on : 54.9799
Width : 2.672
Height : 9.206
Entry
ampl
0
10
20
30
40
50
60
70


B1L104S, U26-ch50
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 154
Mean 32.25
Std Dev 29.18
Turn on : 55.3795
Width : 4.528
Height : 9.778
Entry
ampl
0
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40
50
60
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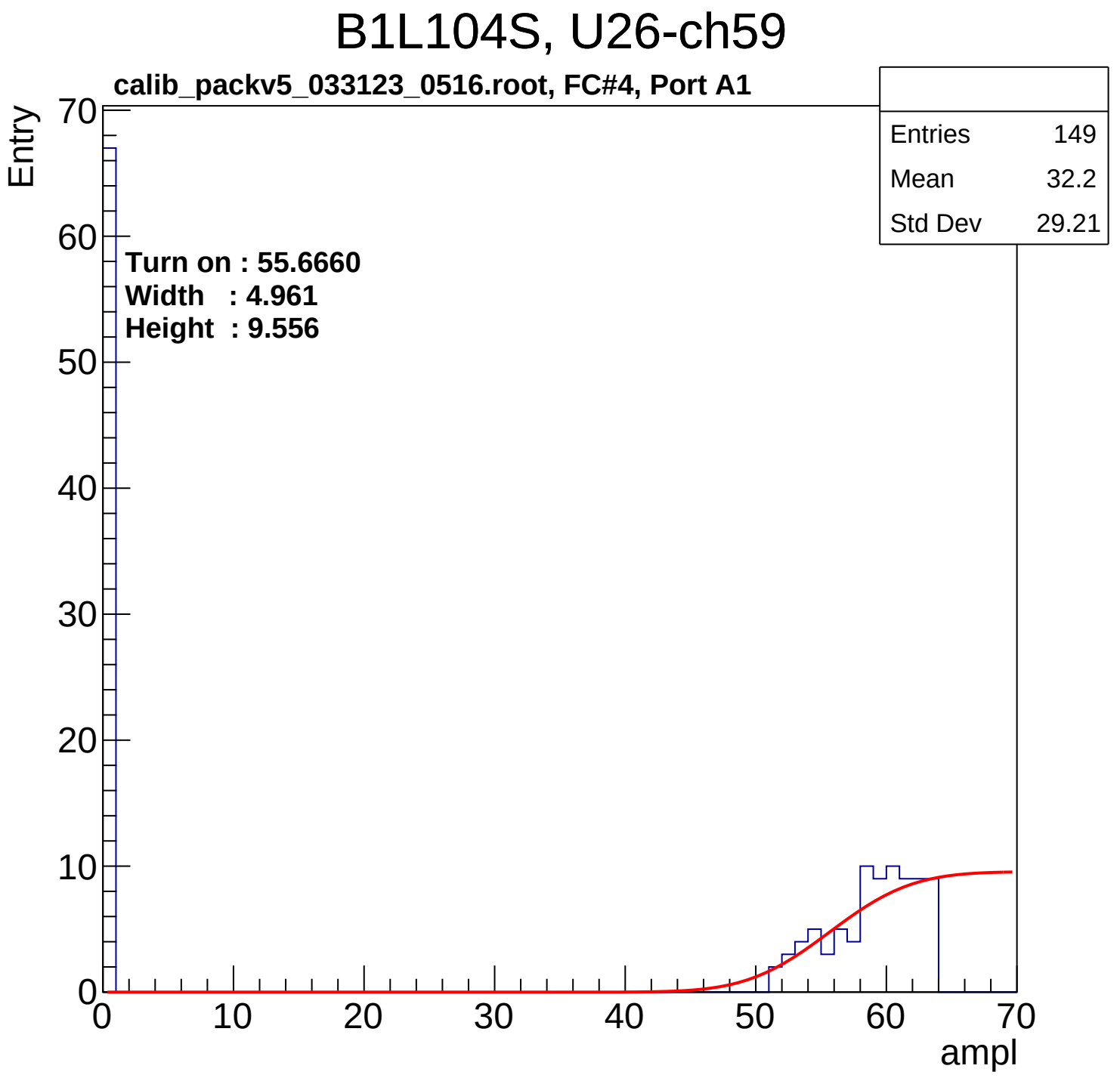
B1L104S, U26-ch59
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 149
Mean 32.2
Std Dev 29.21
Turn on : 55.6660
Width : 4.961
Height : 9.556
Entry
ampl
0
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40
50
60
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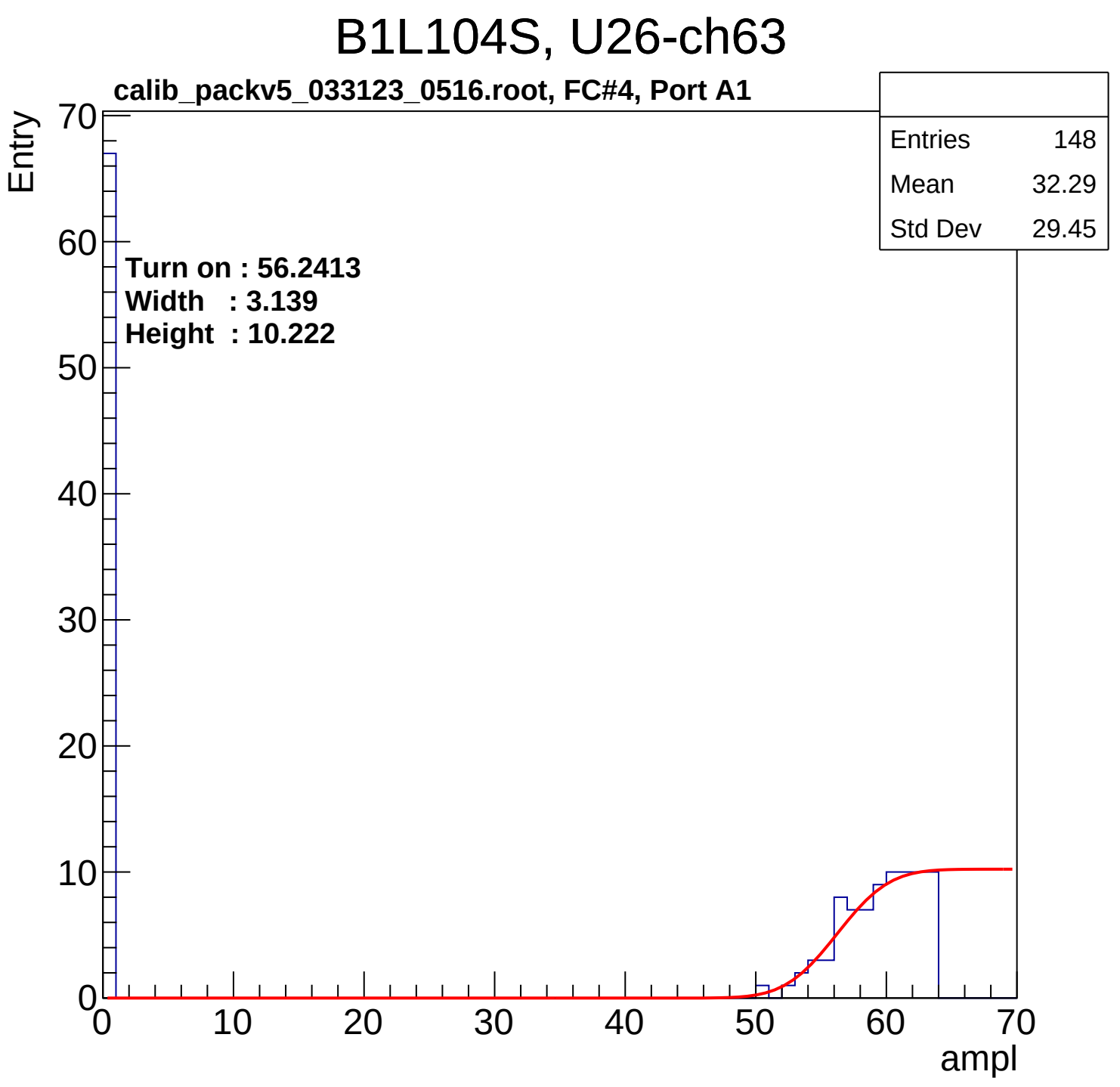
B1L104S, U26-ch63
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 148
Mean 32.29
Std Dev 29.45
Turn on : 56.2413
Width : 3.139
Height : 10.222
Entry
ampl
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20
30
40
50
60
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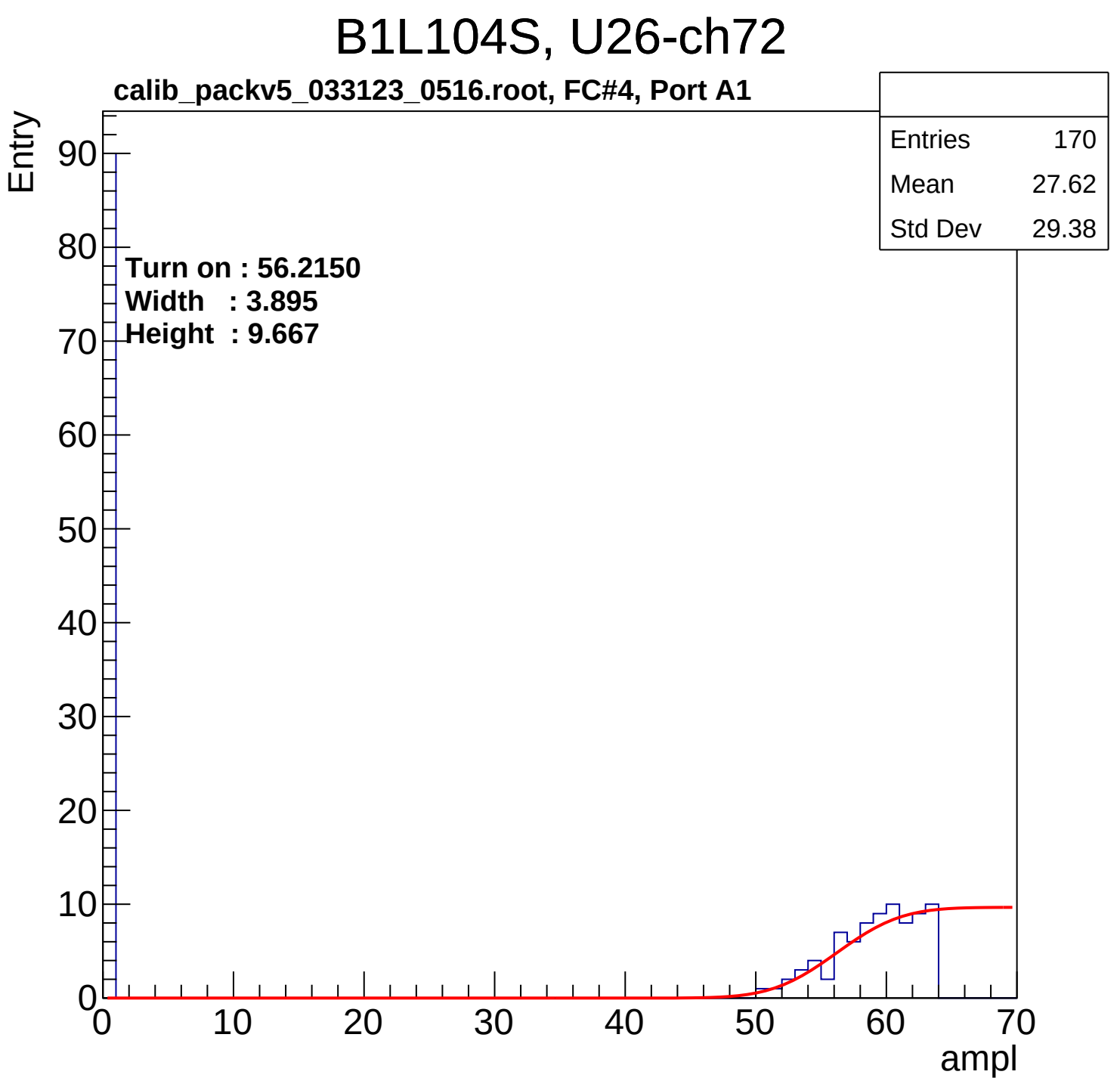
B1L104S, U26-ch72
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 170
Mean 27.62
Std Dev 29.38
Turn on : 56.2150
Width : 3.895
Height : 9.667
Entry
ampl
0
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20
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40
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60
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80
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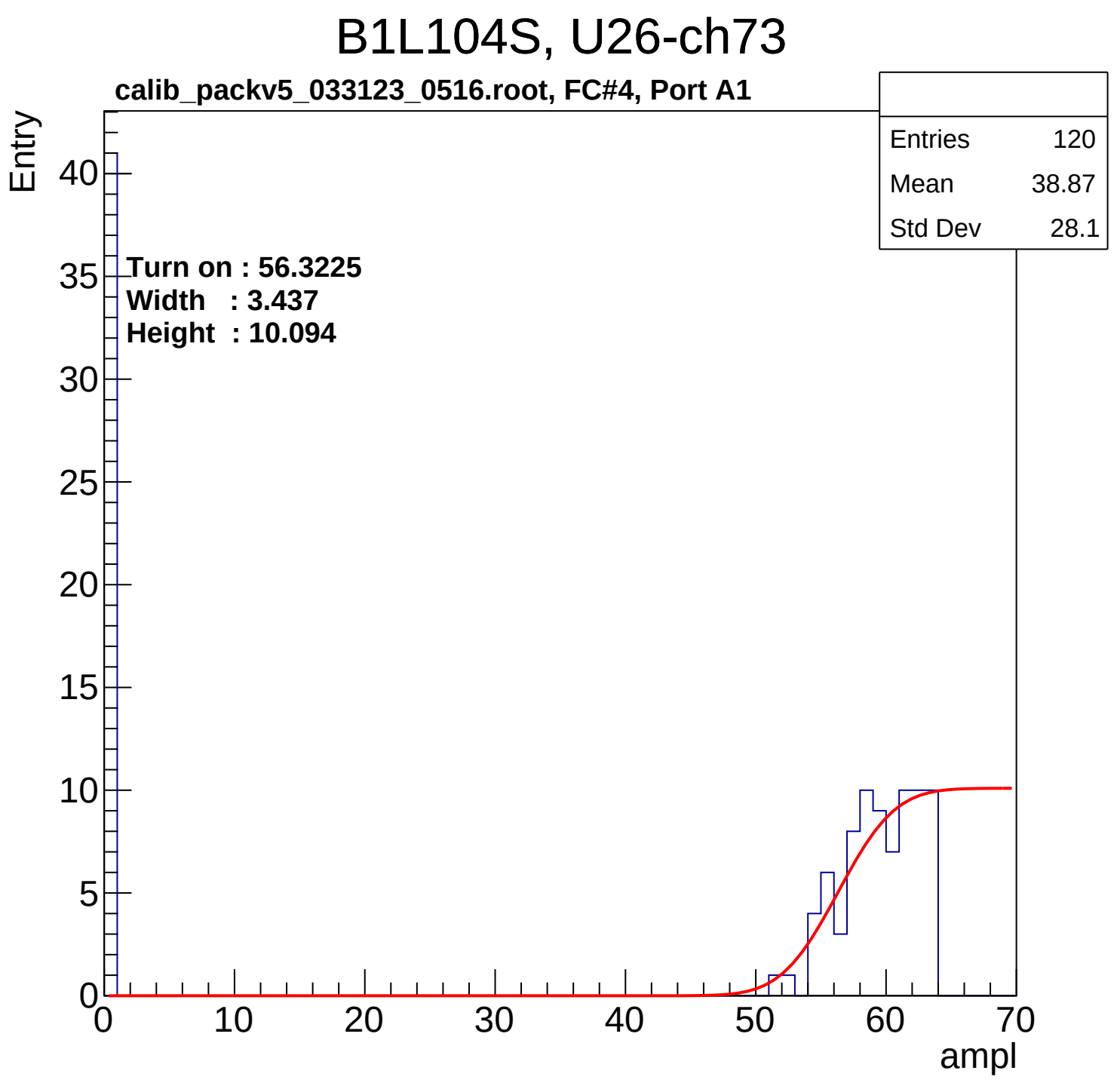
B1L104S, U26-ch73
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 120
Mean 38.87
Std Dev 28.1
Turn on : 56.3225
Width : 3.437
Height : 10.094
Entry
ampl
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10
15
20
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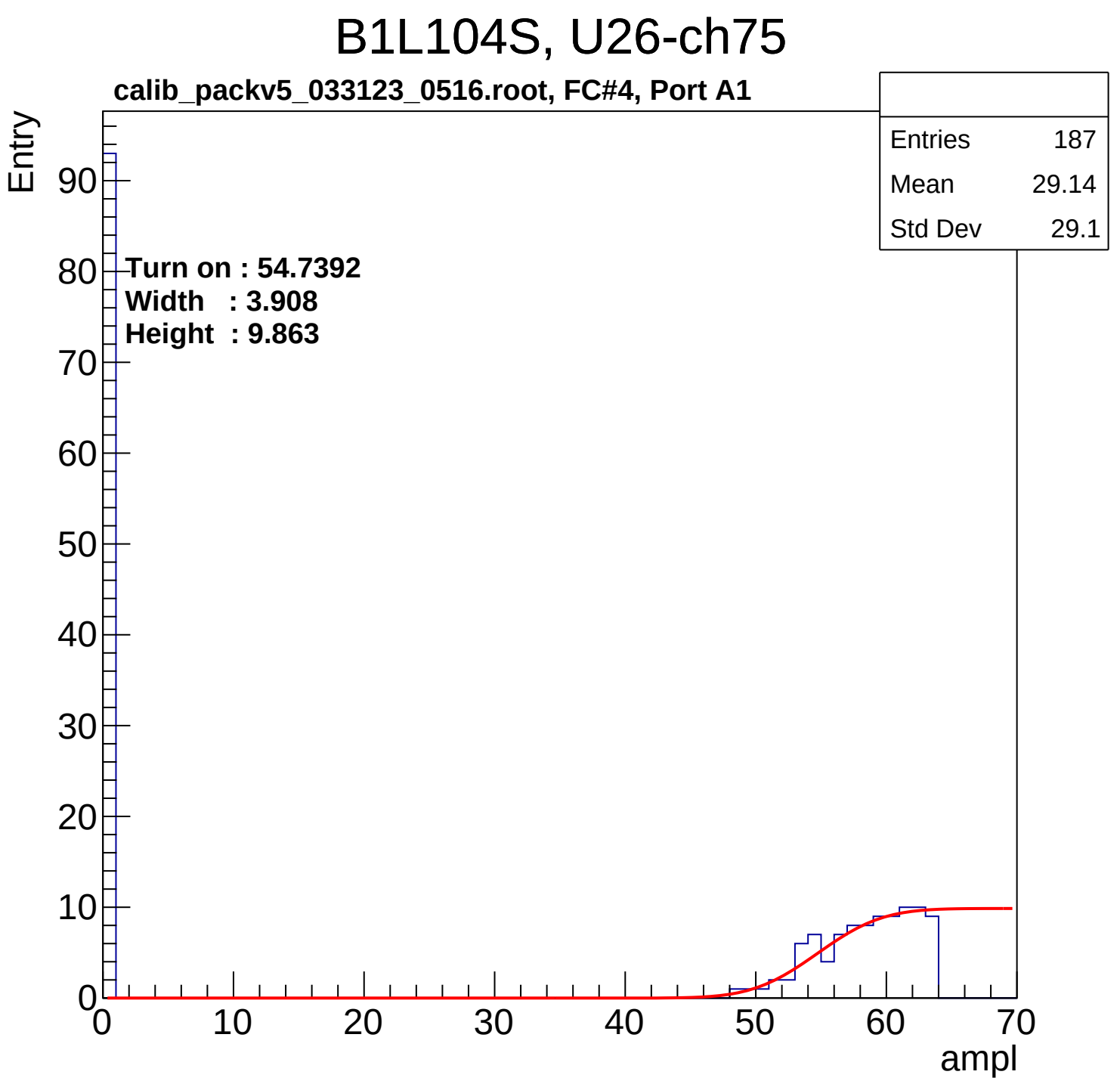
B1L104S, U26-ch75
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 187
Mean 29.14
Std Dev 29.1
Turn on : 54.7392
Width : 3.908
Height : 9.863
Entry
ampl
0
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20
30
40
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60
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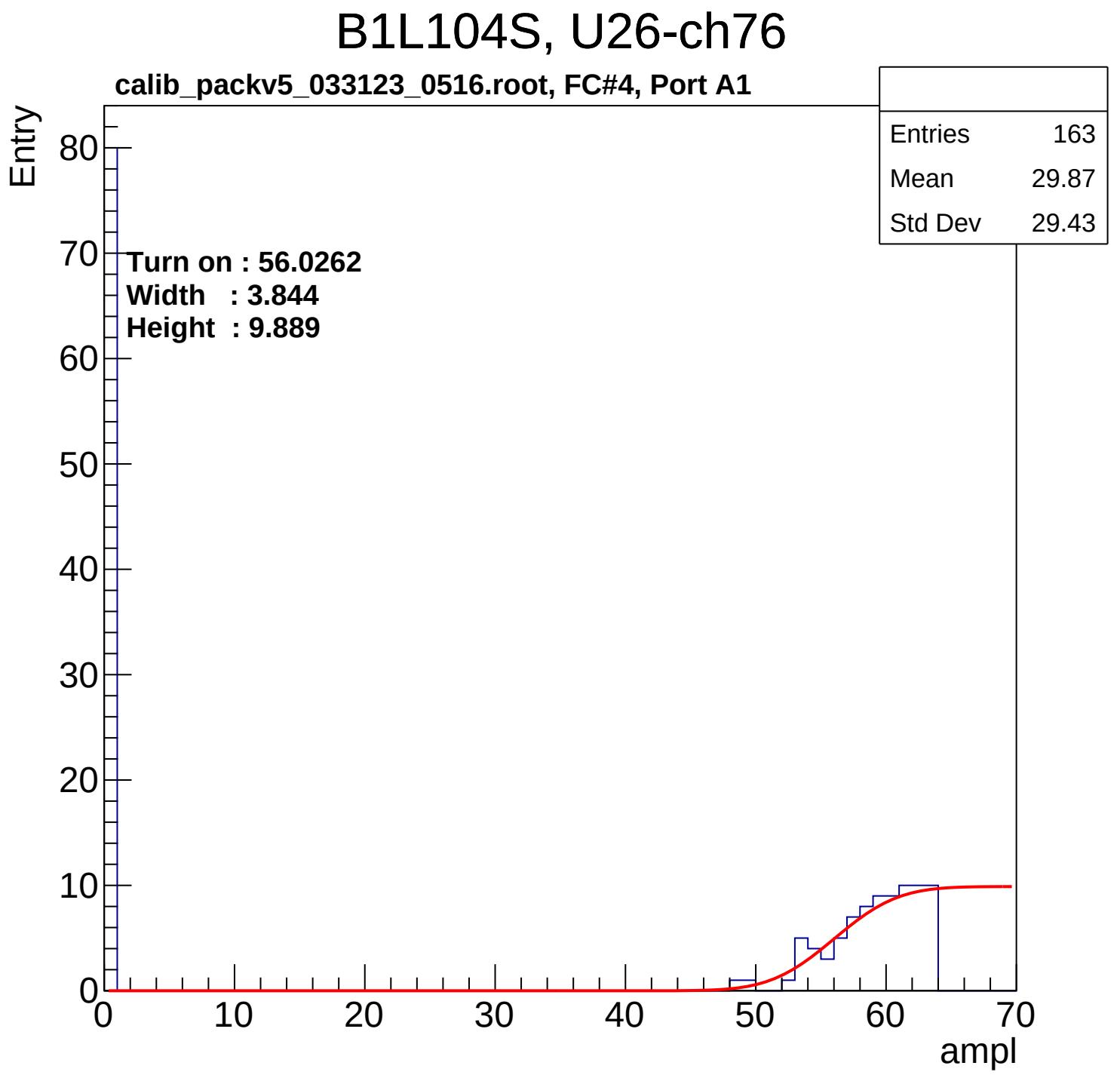
80
90


B1L104S, U26-ch76
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 163
Mean 29.87
Std Dev 29.43
Turn on : 56.0262
Width : 3.844
Height : 9.889
Entry
ampl
0
10
20
30
40
50
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70
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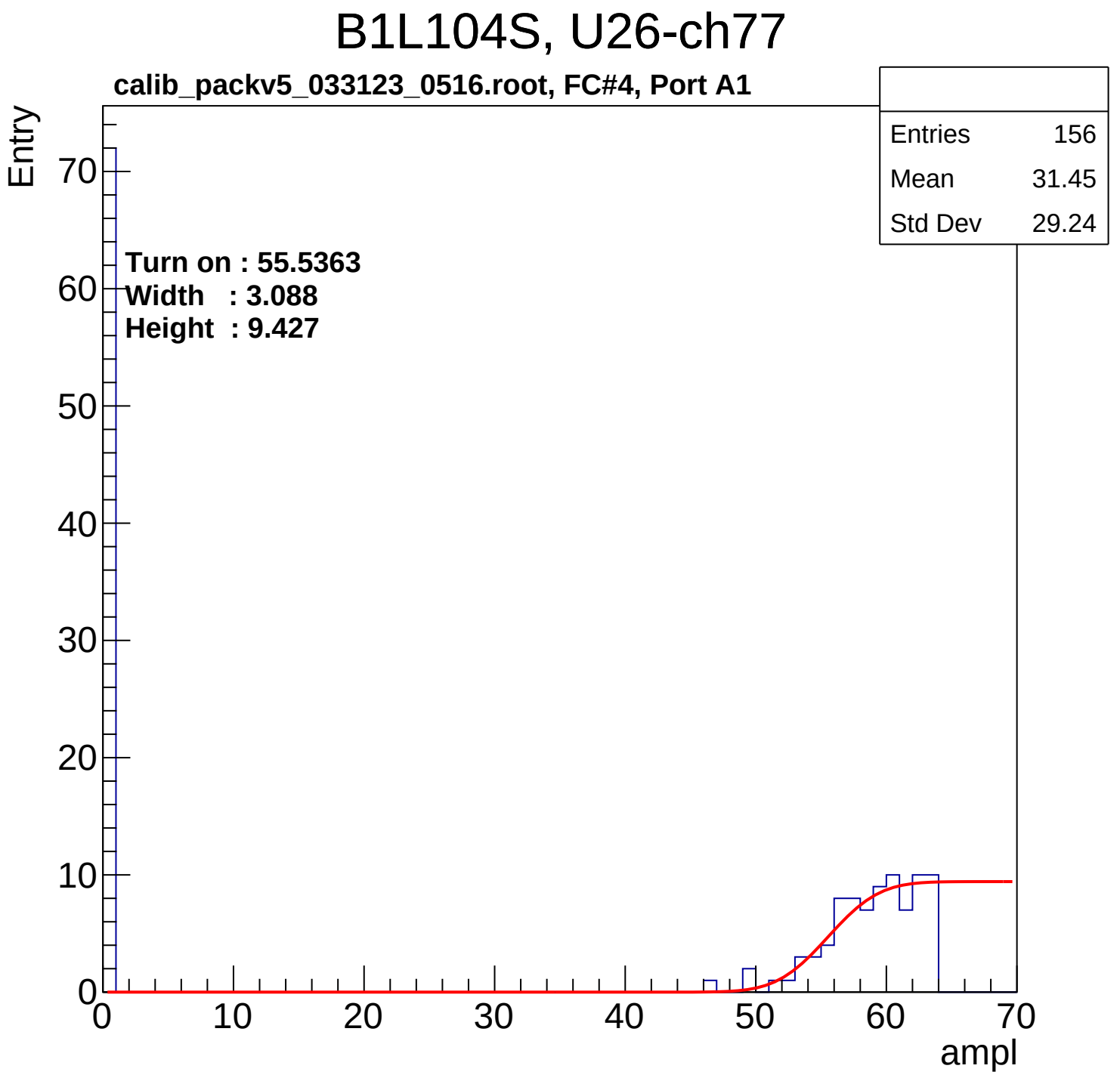
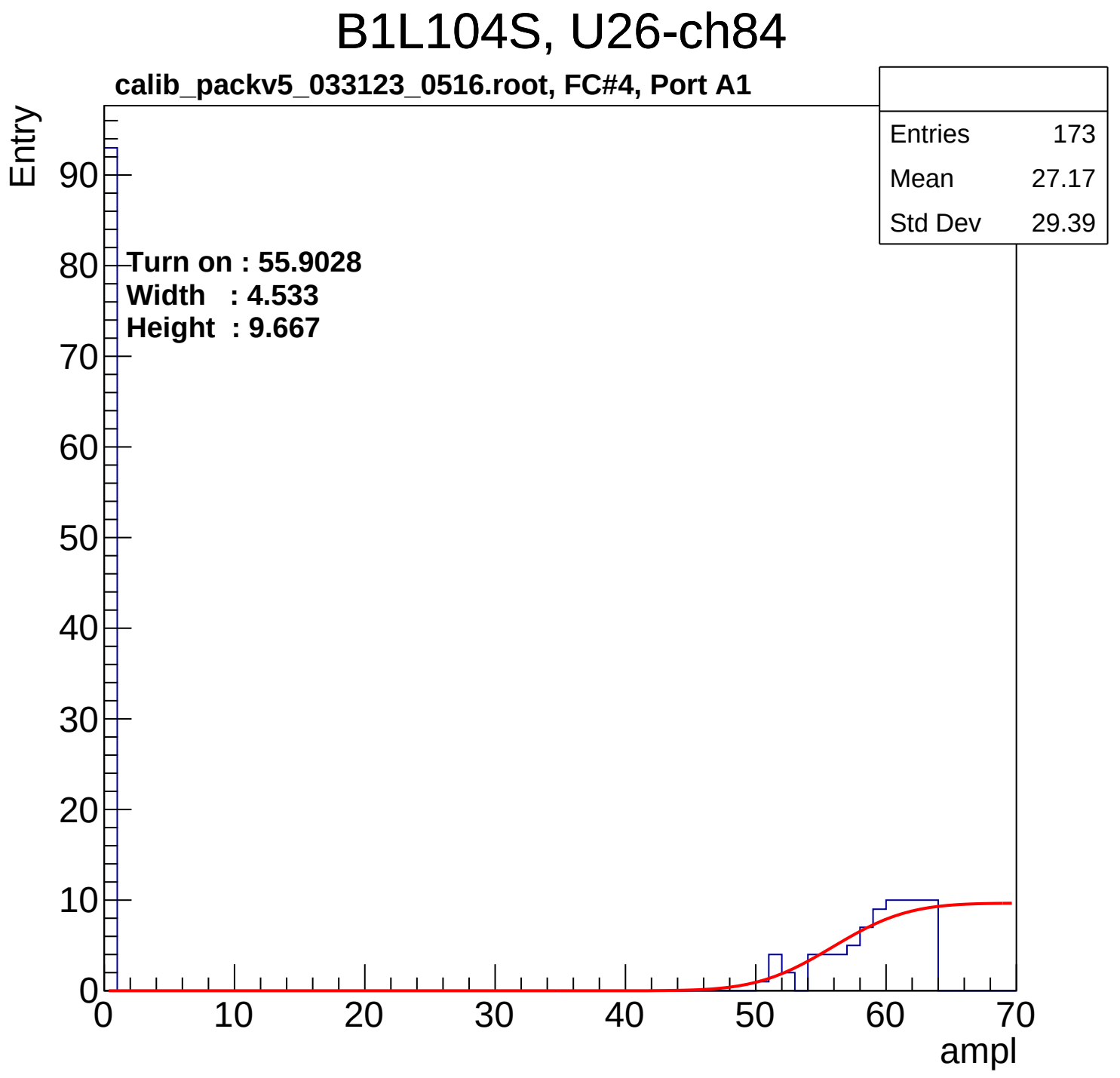
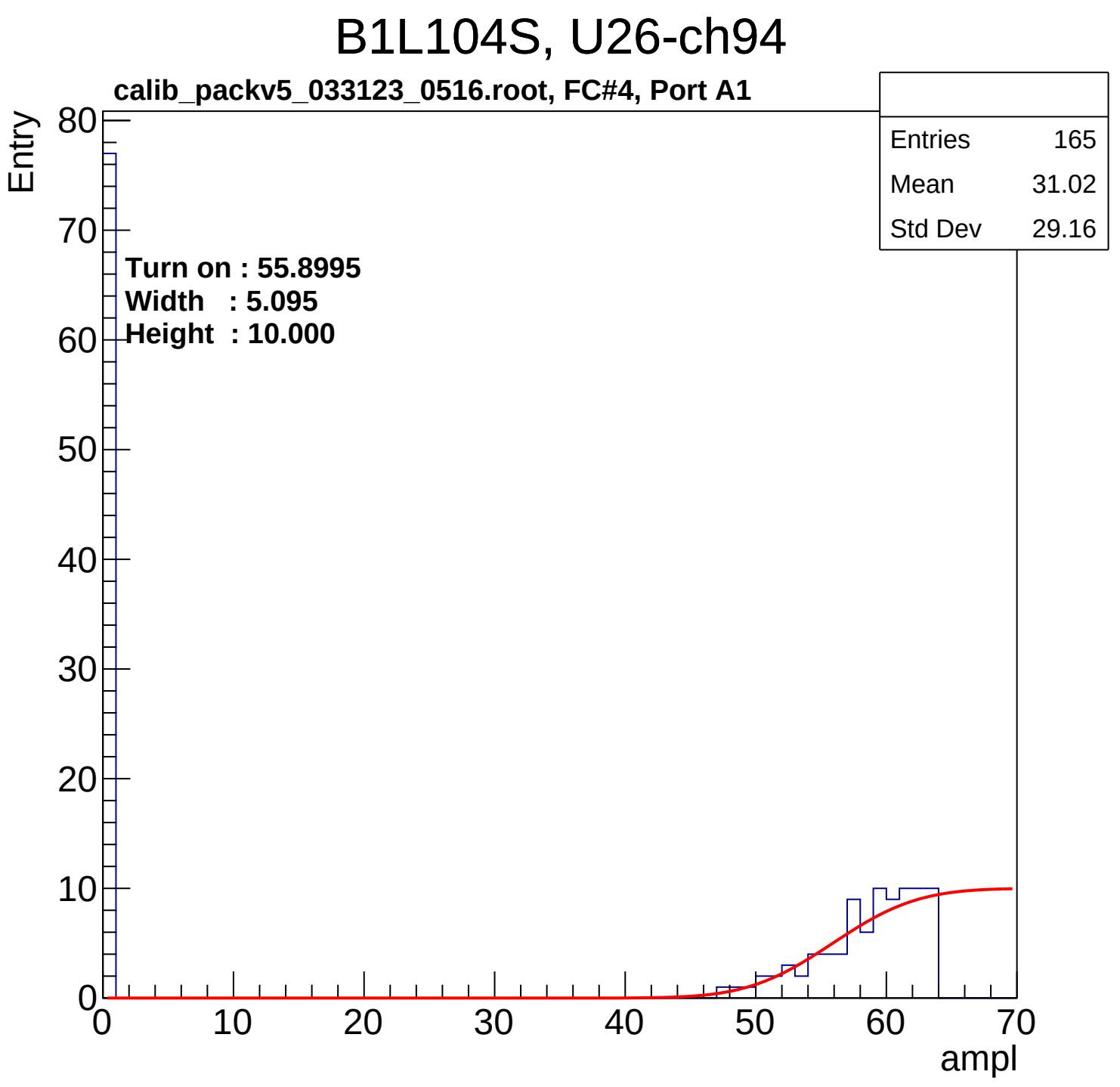

B1L104S, U26-ch77
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 156
Mean 31.45
Std Dev 29.24
Turn on : 55.5363
Width : 3.088
Height : 9.427
Entry
ampl
0
10
20
30
40
50
60
70


B1L104S, U26-ch84
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 173
Mean 27.17
Std Dev 29.39
Turn on : 55.9028
Width : 4.533
Height : 9.667
Entry
ampl
0
10
20
30
40
50
60
70
80
90


B1L104S, U26-ch94
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 165
Mean 31.02
Std Dev 29.16
Turn on : 55.8995
Width : 5.095
Height : 10.000
Entry
ampl
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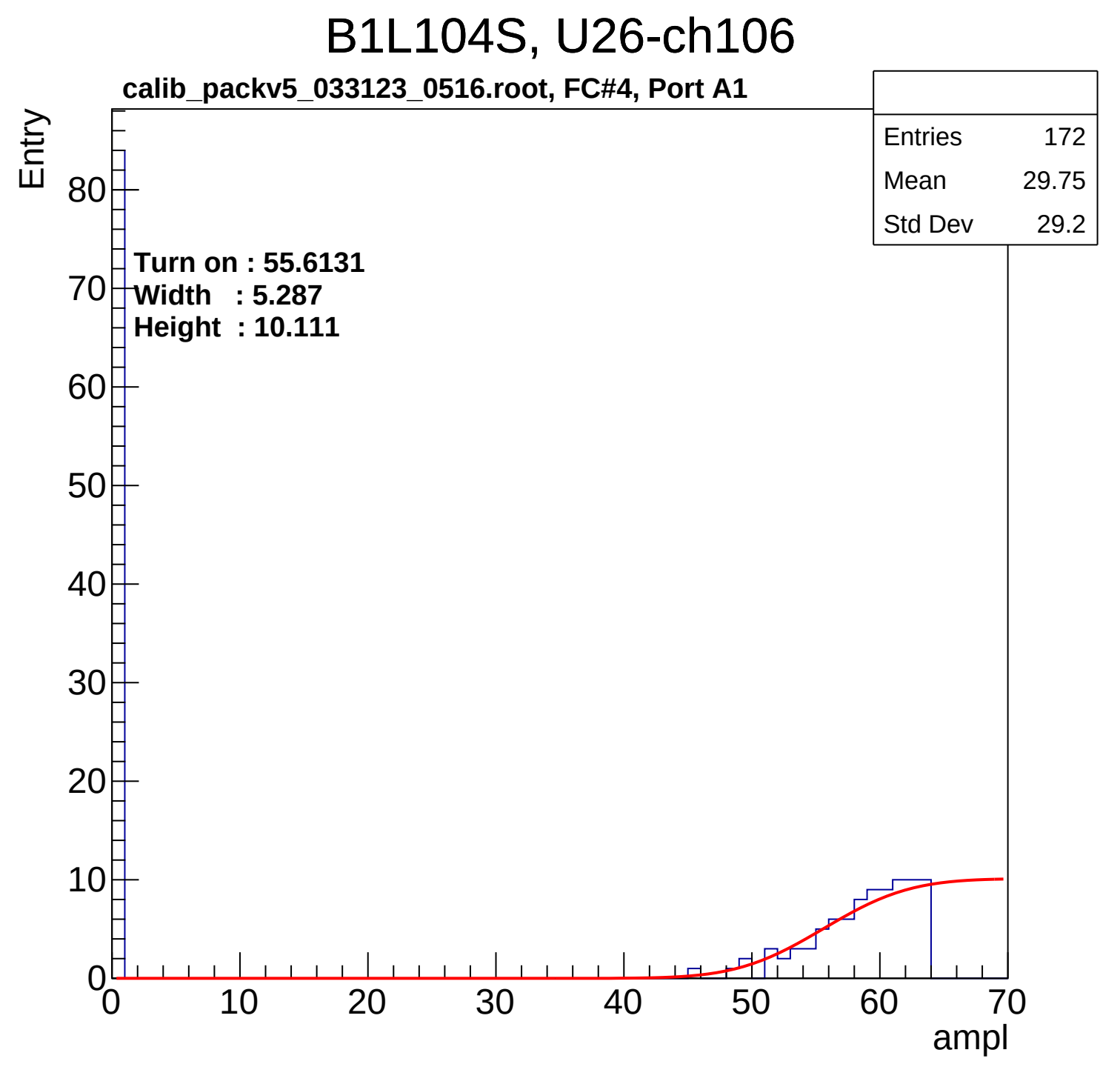
B1L104S, U26-ch106
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 172
Mean 29.75
Std Dev 29.2
Turn on : 55.6131
Width : 5.287
Height : 10.111
Entry
ampl
0
10
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30
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50
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70
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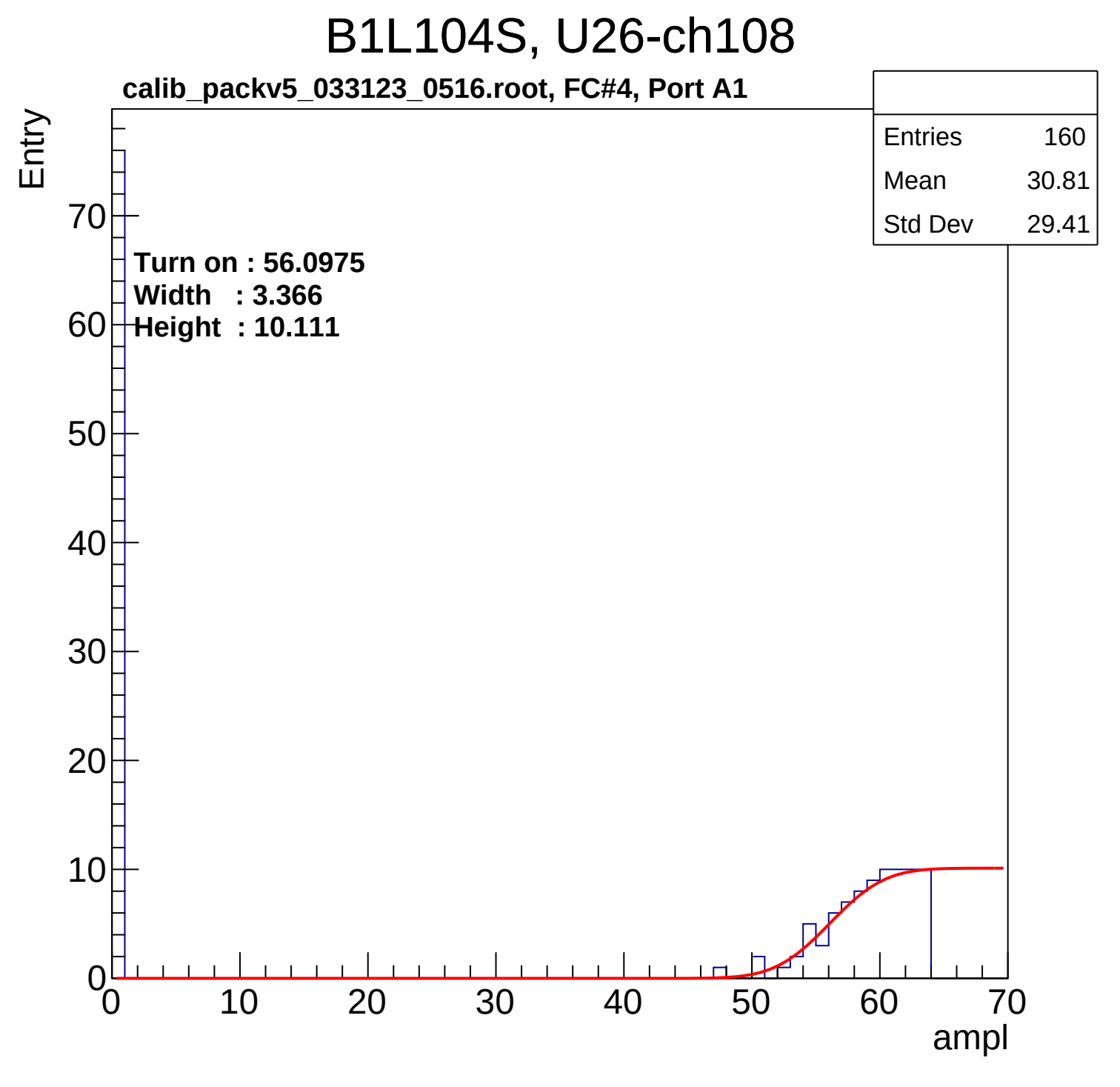
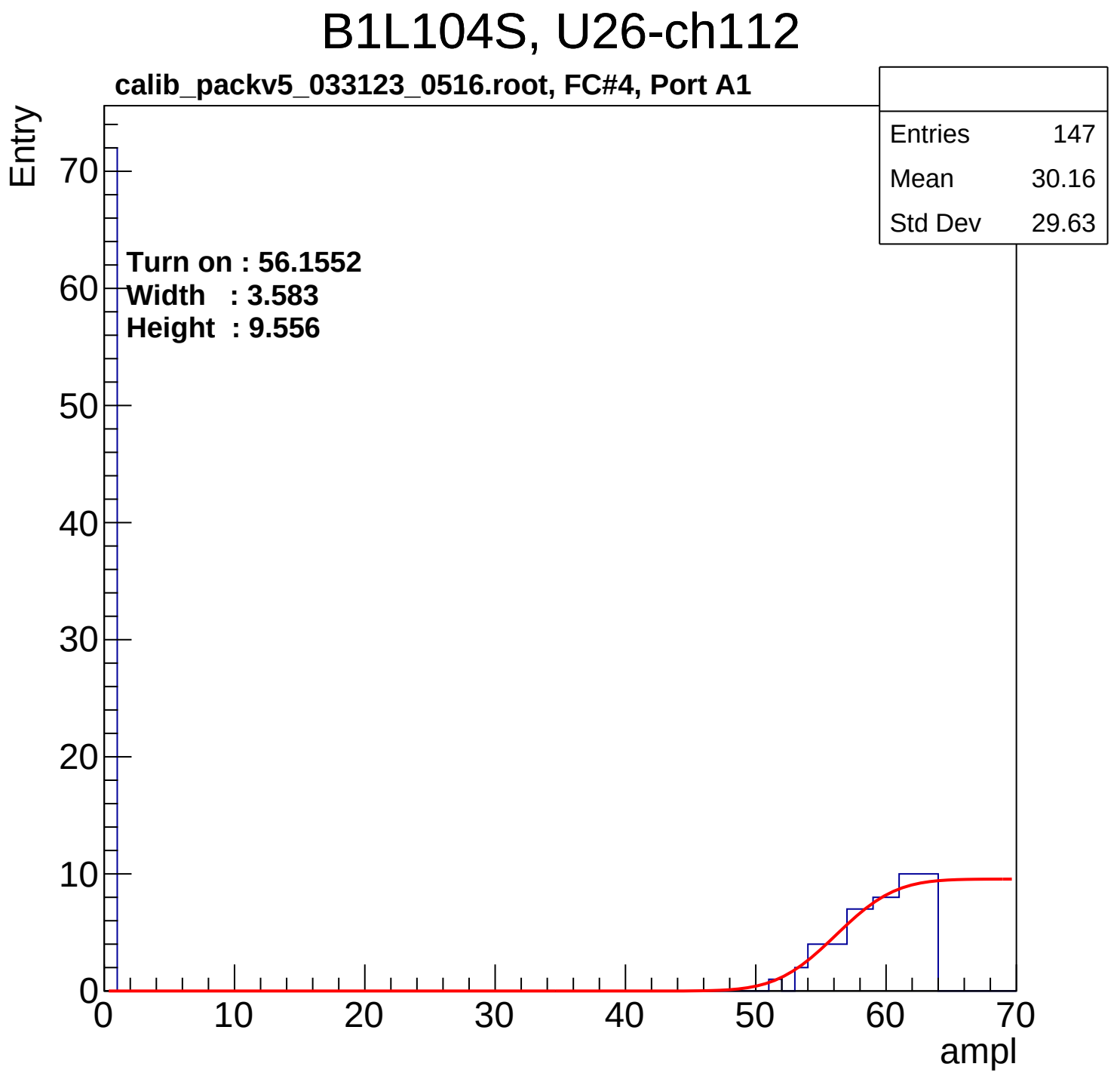
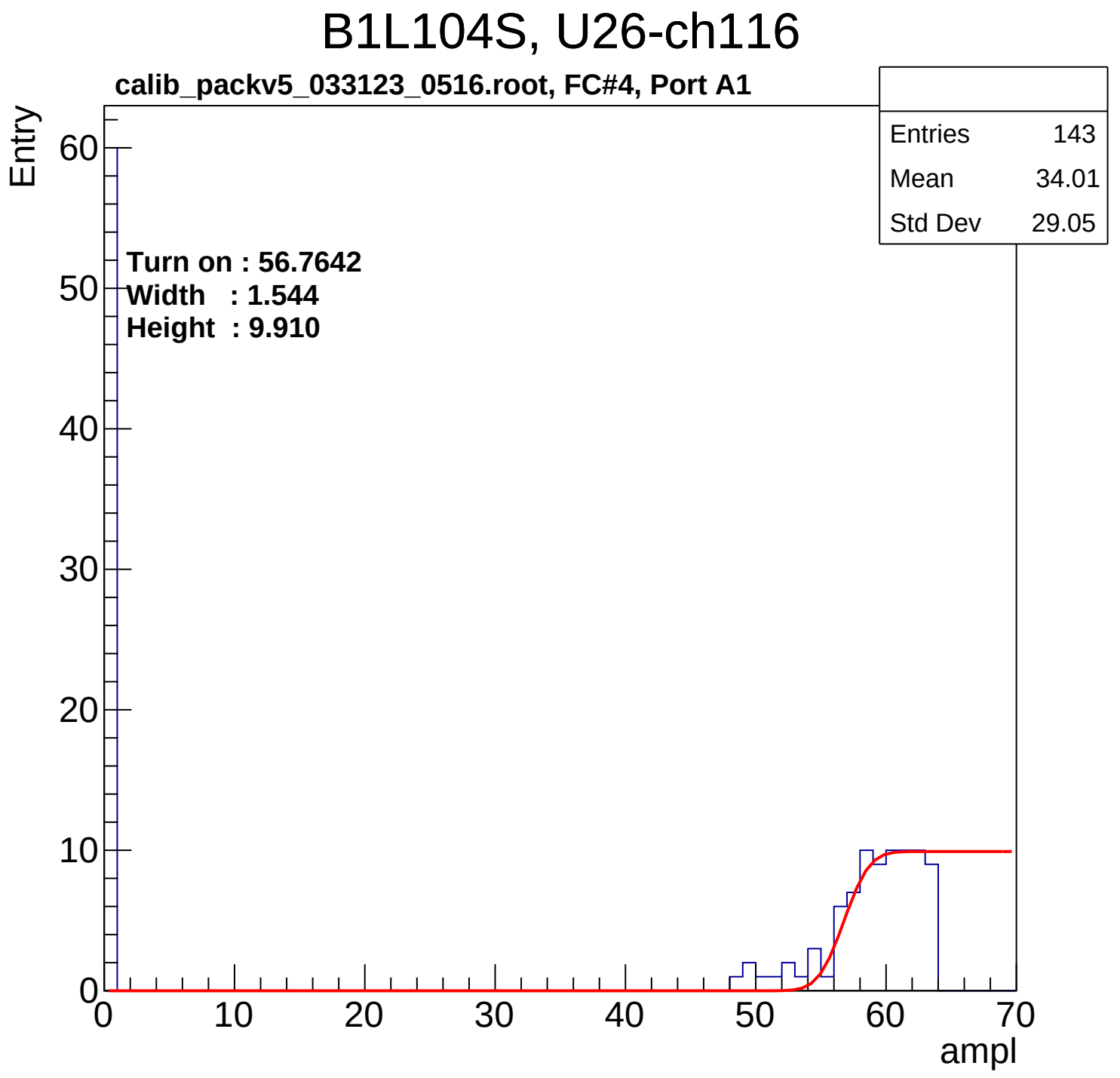
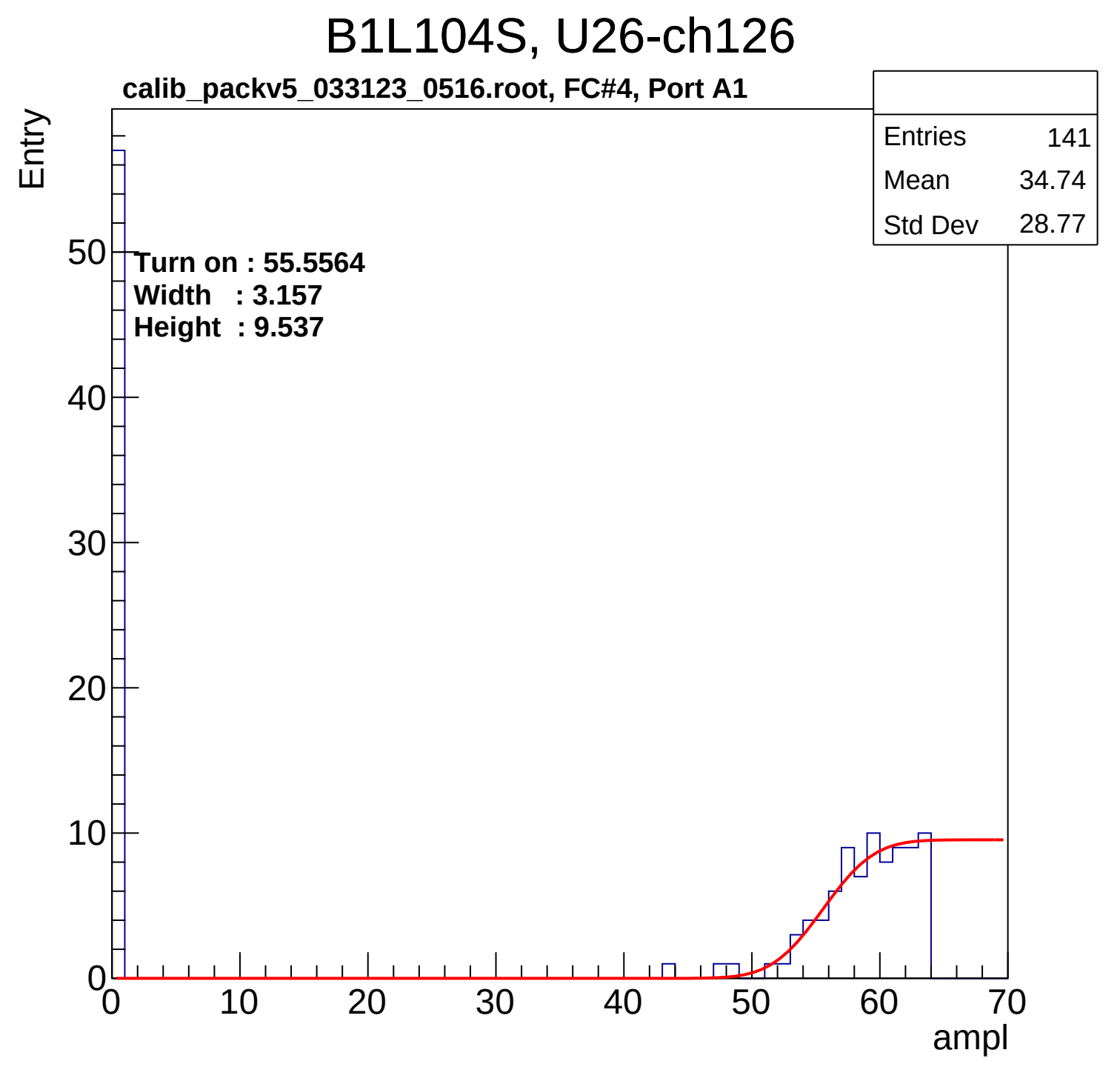

B1L104S, U26-ch108
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 160
Mean 30.81
Std Dev 29.41
Turn on : 56.0975
Width : 3.366
Height : 10.111
Entry
ampl
0
10
20
30
40
50
60
70


B1L104S, U26-ch112
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 147
Mean 30.16
Std Dev 29.63
Turn on : 56.1552
Width : 3.583
Height : 9.556
Entry
ampl
0
10
20
30
40
50
60
70


B1L104S, U26-ch116
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 143
Mean 34.01
Std Dev 29.05
Turn on : 56.7642
Width : 1.544
Height : 9.910
Entry
ampl
0
10
20
30
40
50
60
70


B1L104S, U26-ch126
calib_packv5_033123_0516.root, FC#4, Port A1
Entries 141
Mean 34.74
Std Dev 28.77
Turn on : 55.5564
Width : 3.157
Height : 9.537
Entry
ampl
0
10
20
30
40
50
60
70