



# B0L001S, U24-ch0, adc0

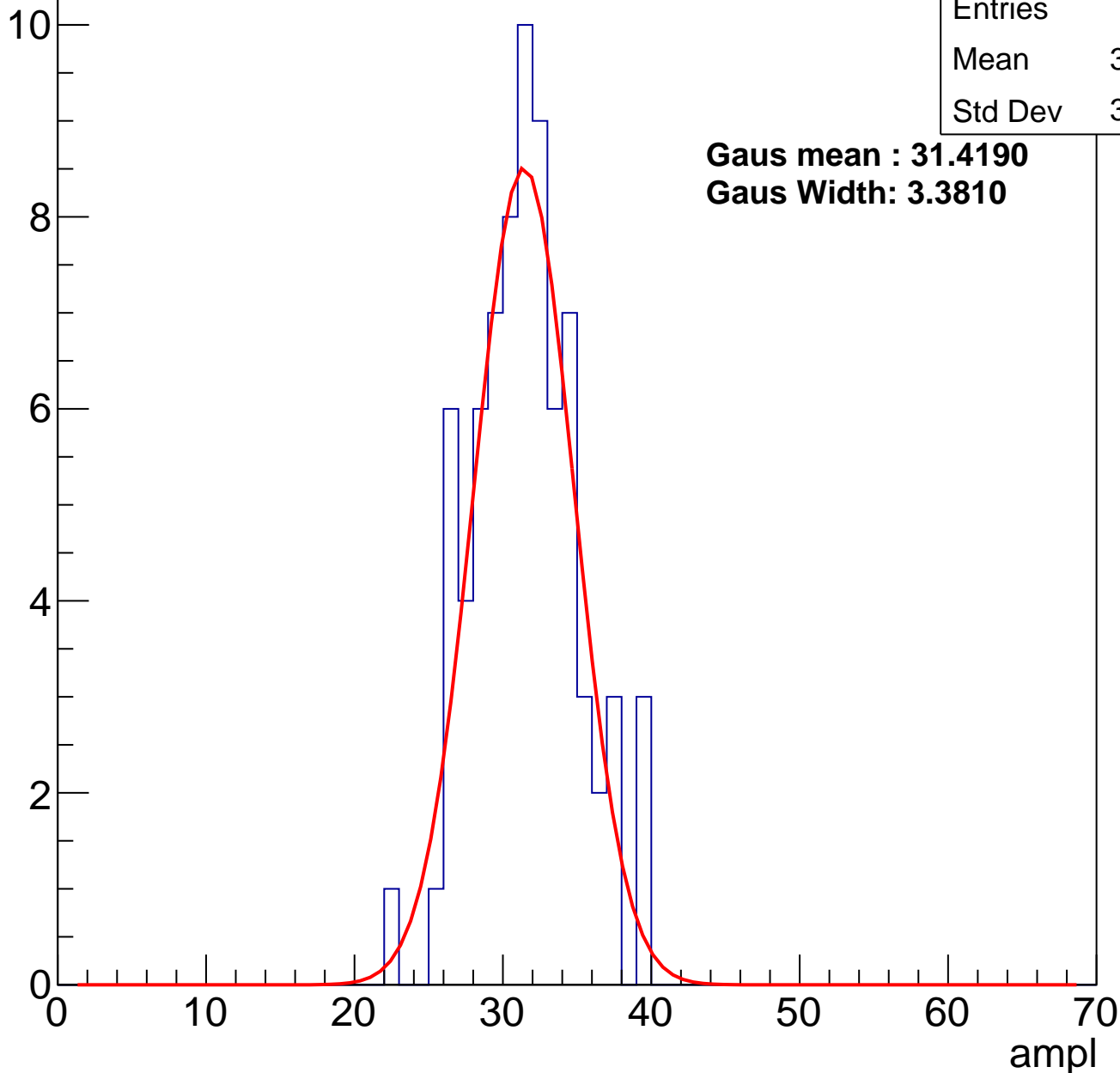
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	76
Mean	31.07
Std Dev	3.469

**Gaus mean : 31.4190**

**Gaus Width: 3.3810**

Entry



# B0L001S, U24-ch0, adc1

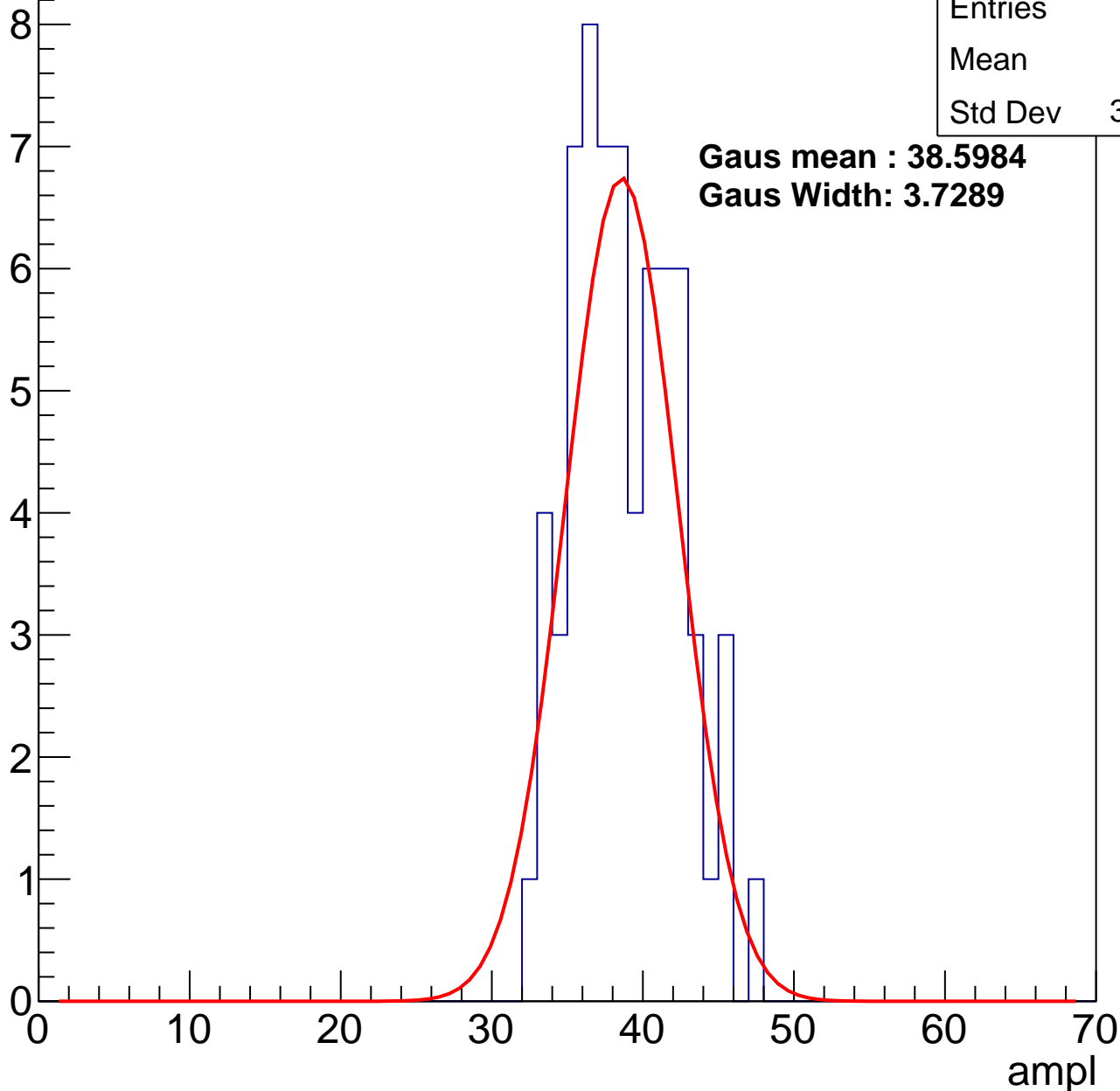
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	38.4
Std Dev	3.438

**Gaus mean : 38.5984**

**Gaus Width: 3.7289**



# B0L001S, U24-ch0, adc2

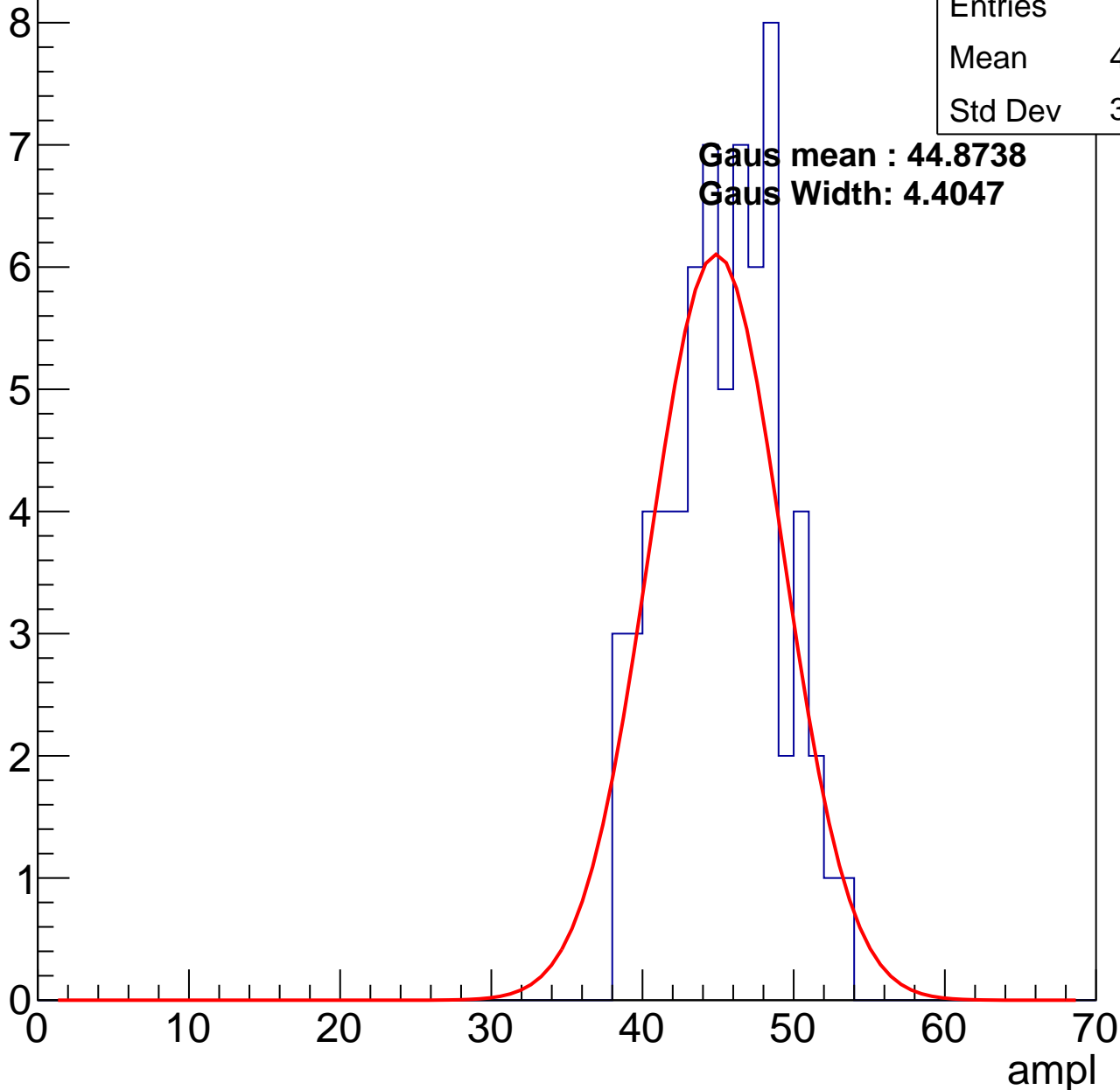
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	44.88
Std Dev	3.675

**Gaus mean : 44.8738**

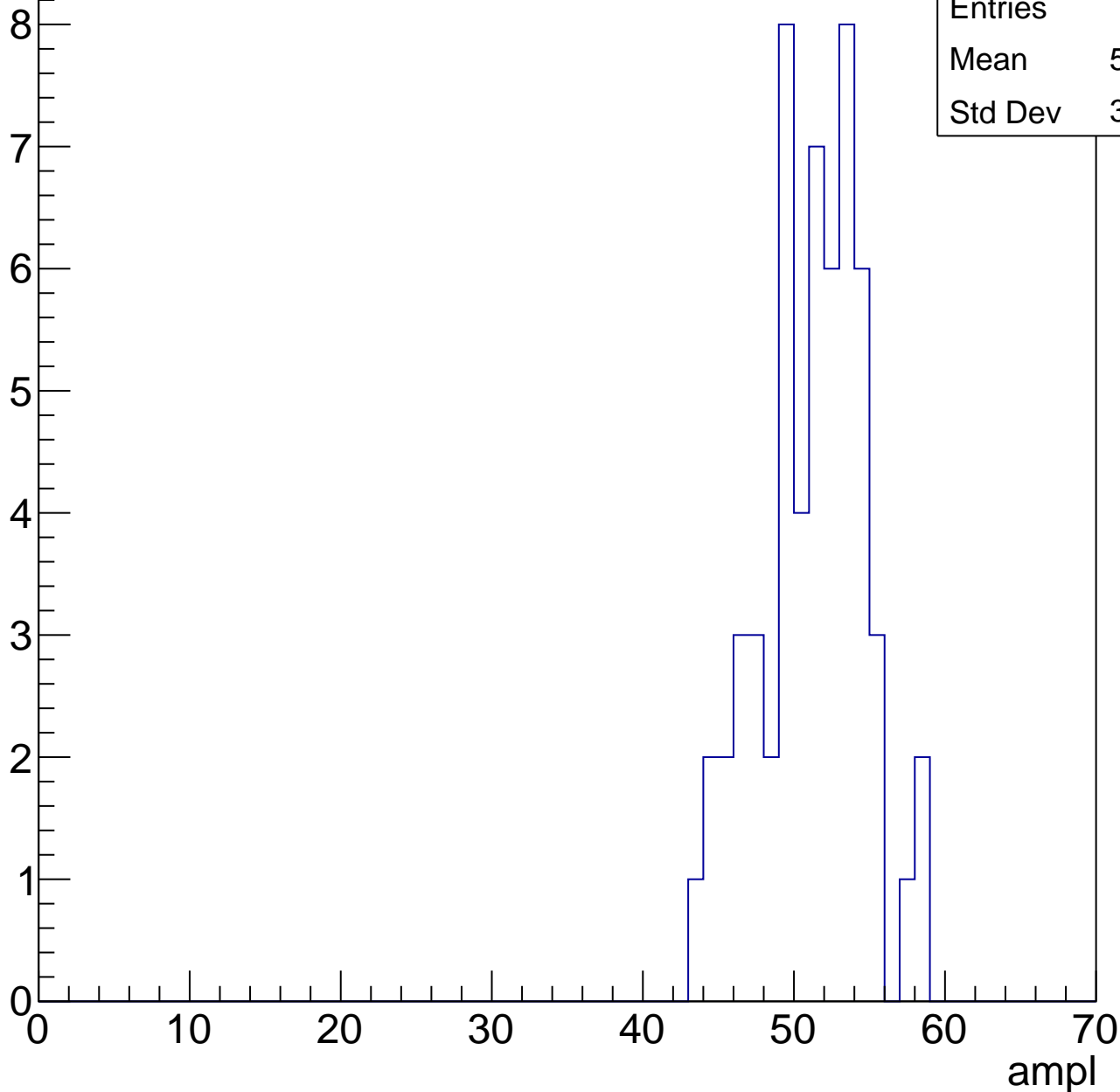
**Gaus Width: 4.4047**



# B0L001S, U24-ch0, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



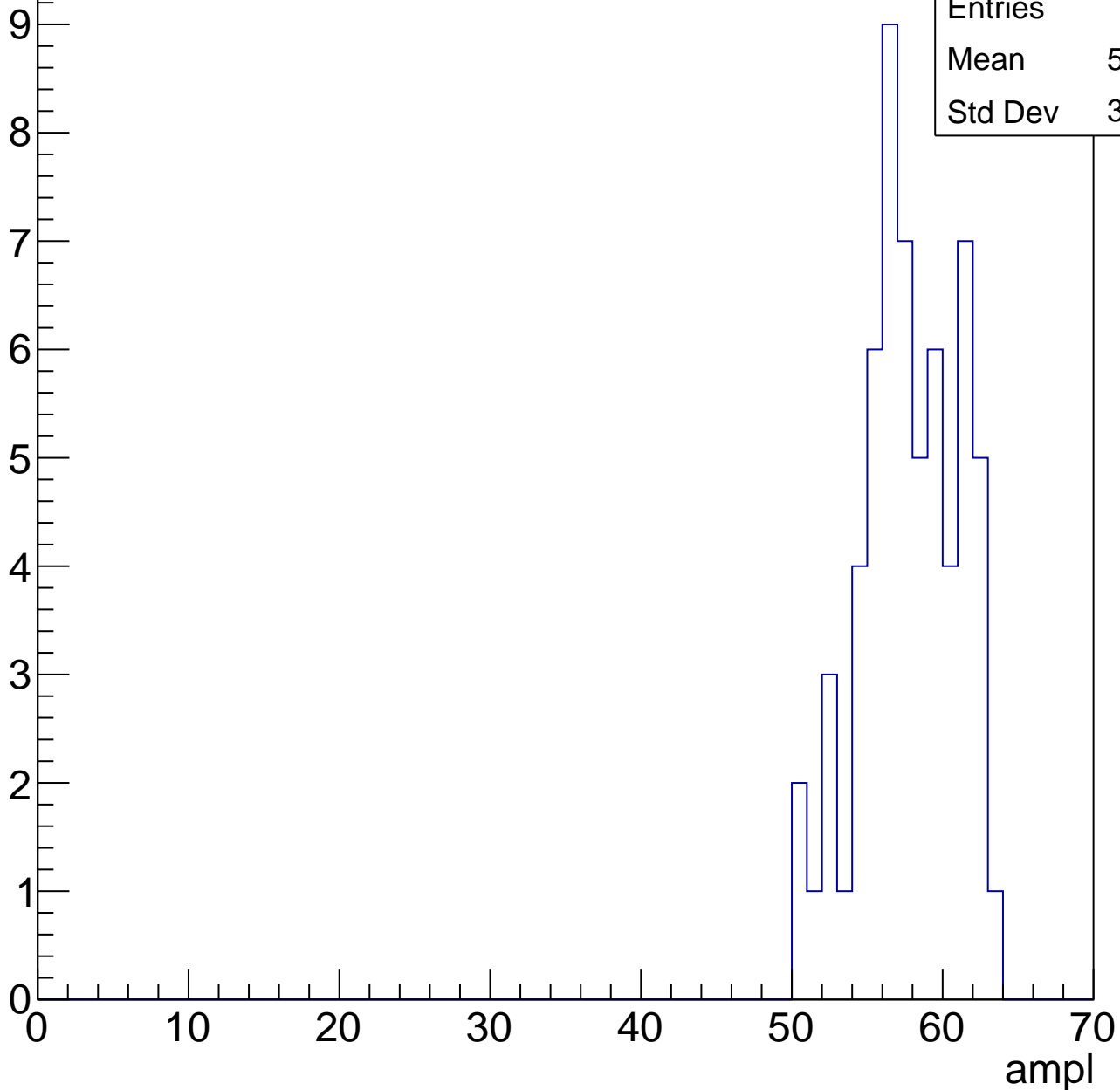
Entries	58
Mean	50.74
Std Dev	3.427

# B0L001S, U24-ch0, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	57.26
Std Dev	3.208

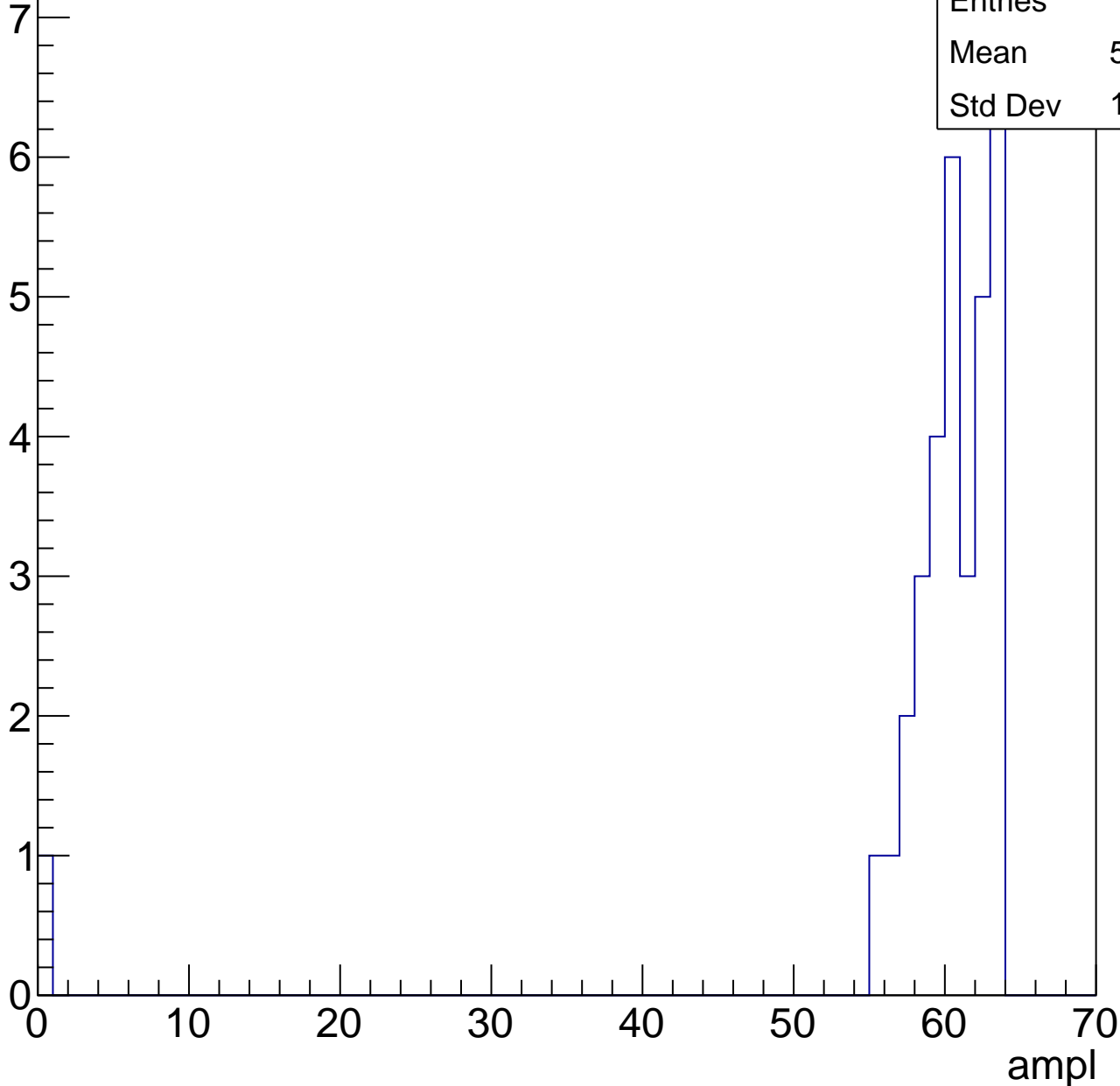


# B0L001S, U24-ch0, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	33
Mean	58.45
Std Dev	10.56



# B0L001S, U24-ch0, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	63
Std Dev	0

0 10 20 30 40 50 60 70

ampl



# B0L001S, U24-ch0, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U24-ch1, adc0

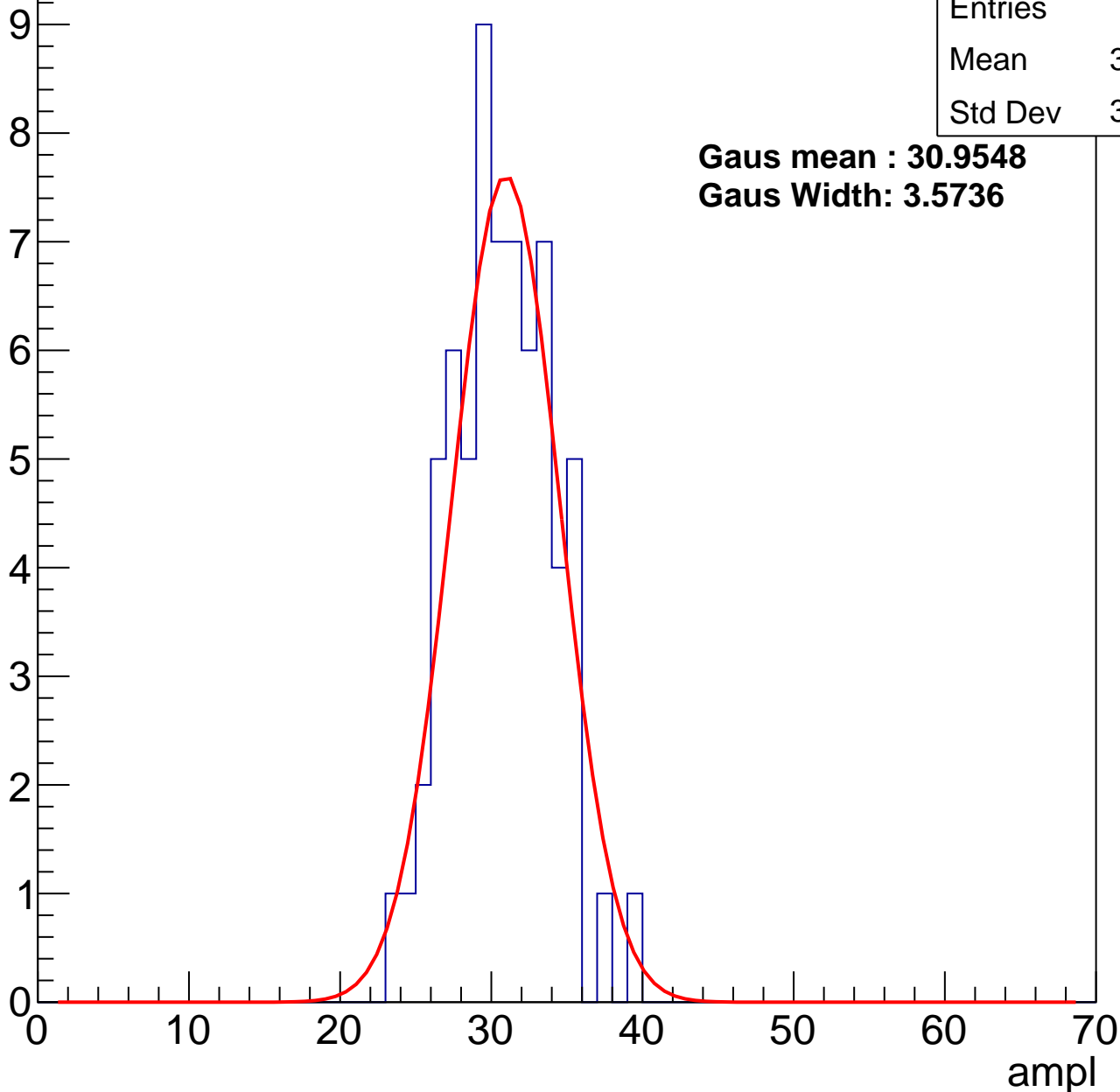
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	30.25
Std Dev	3.248

**Gaus mean : 30.9548**

**Gaus Width: 3.5736**



# B0L001S, U24-ch1, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	92
Mean	38.21
Std Dev	4.004

**Gaus mean : 38.4196**

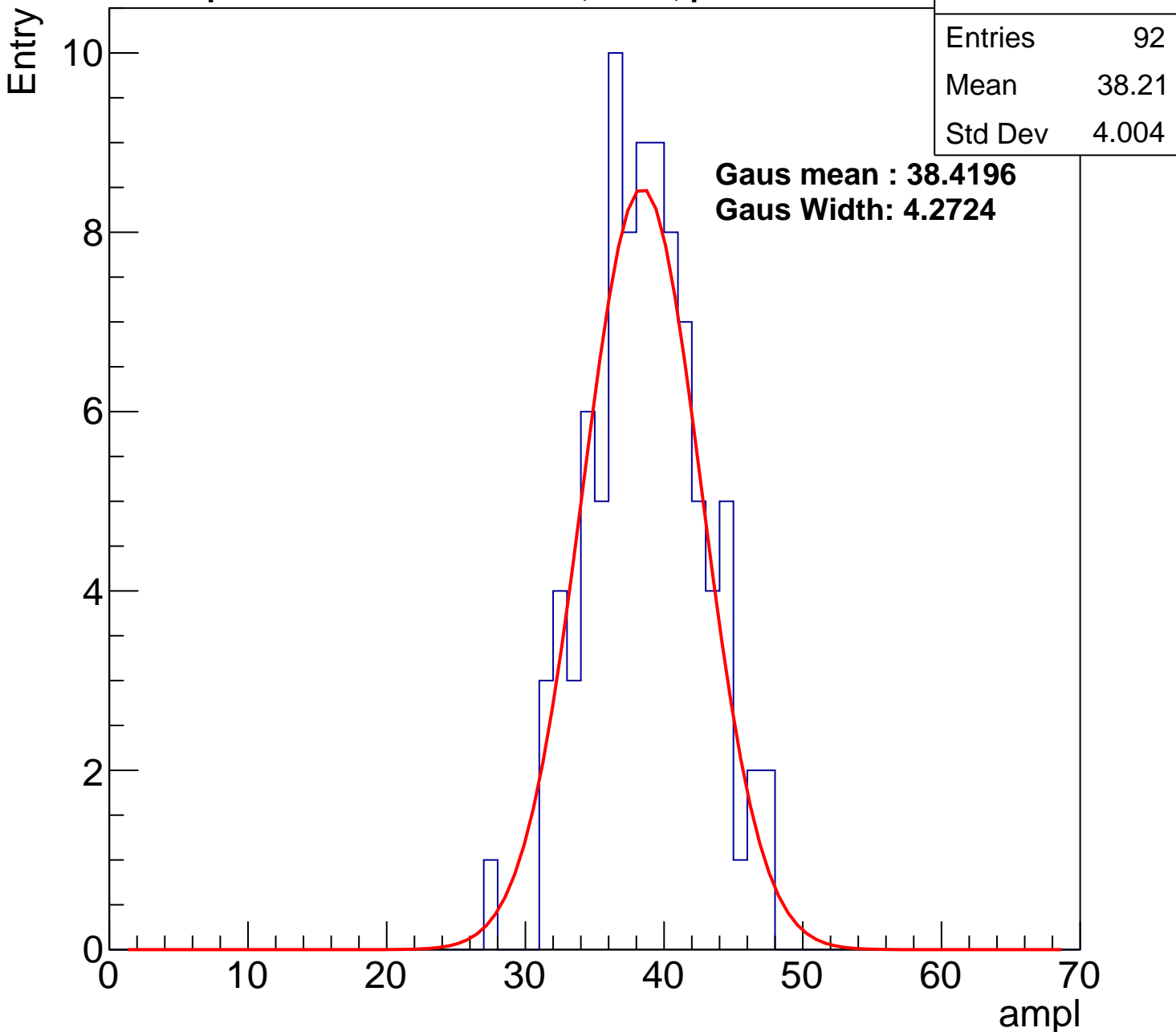
**Gaus Width: 4.2724**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B0L001S, U24-ch1, adc2

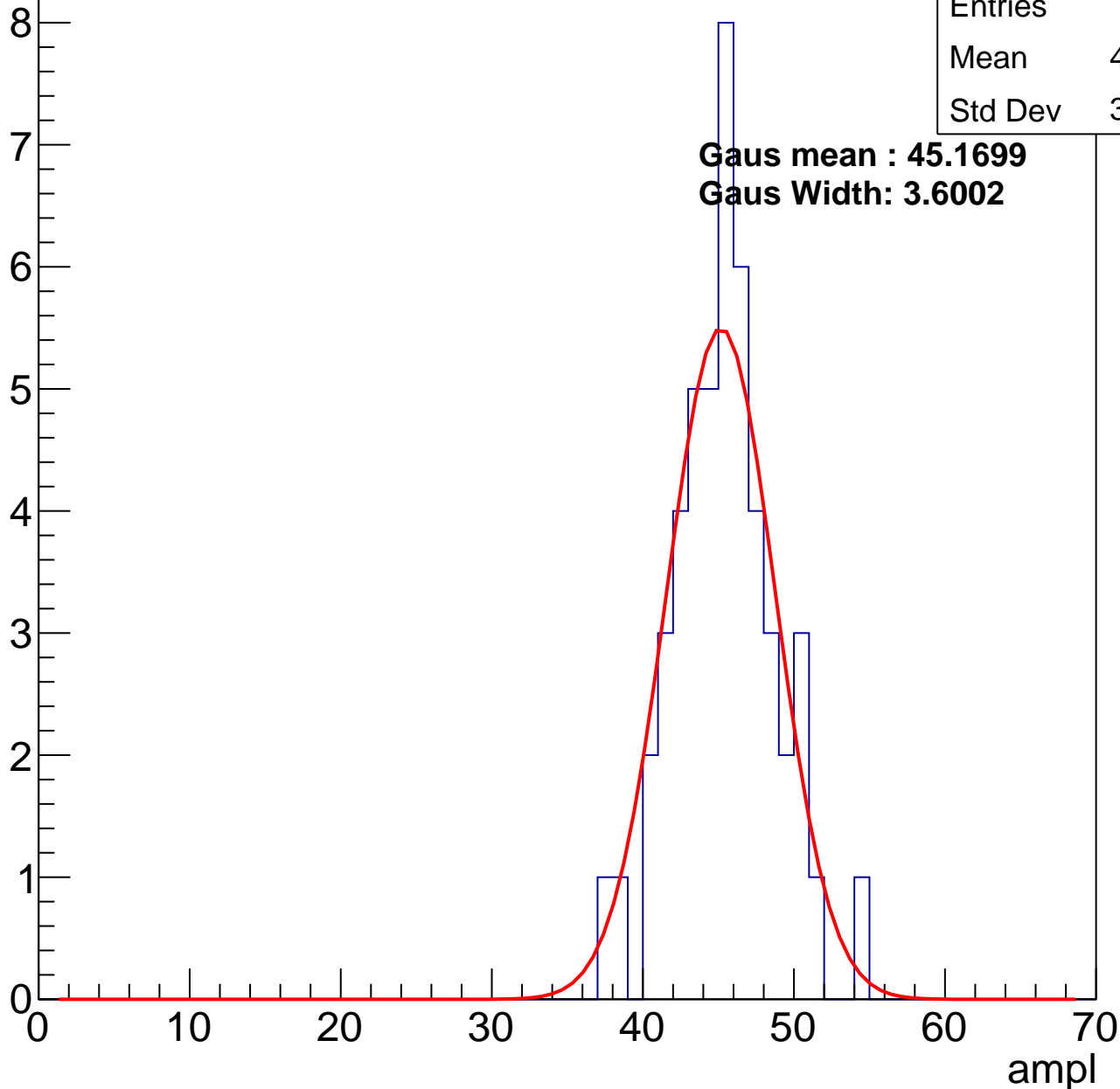
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	49
Mean	44.94
Std Dev	3.334

**Gaus mean : 45.1699**

**Gaus Width: 3.6002**

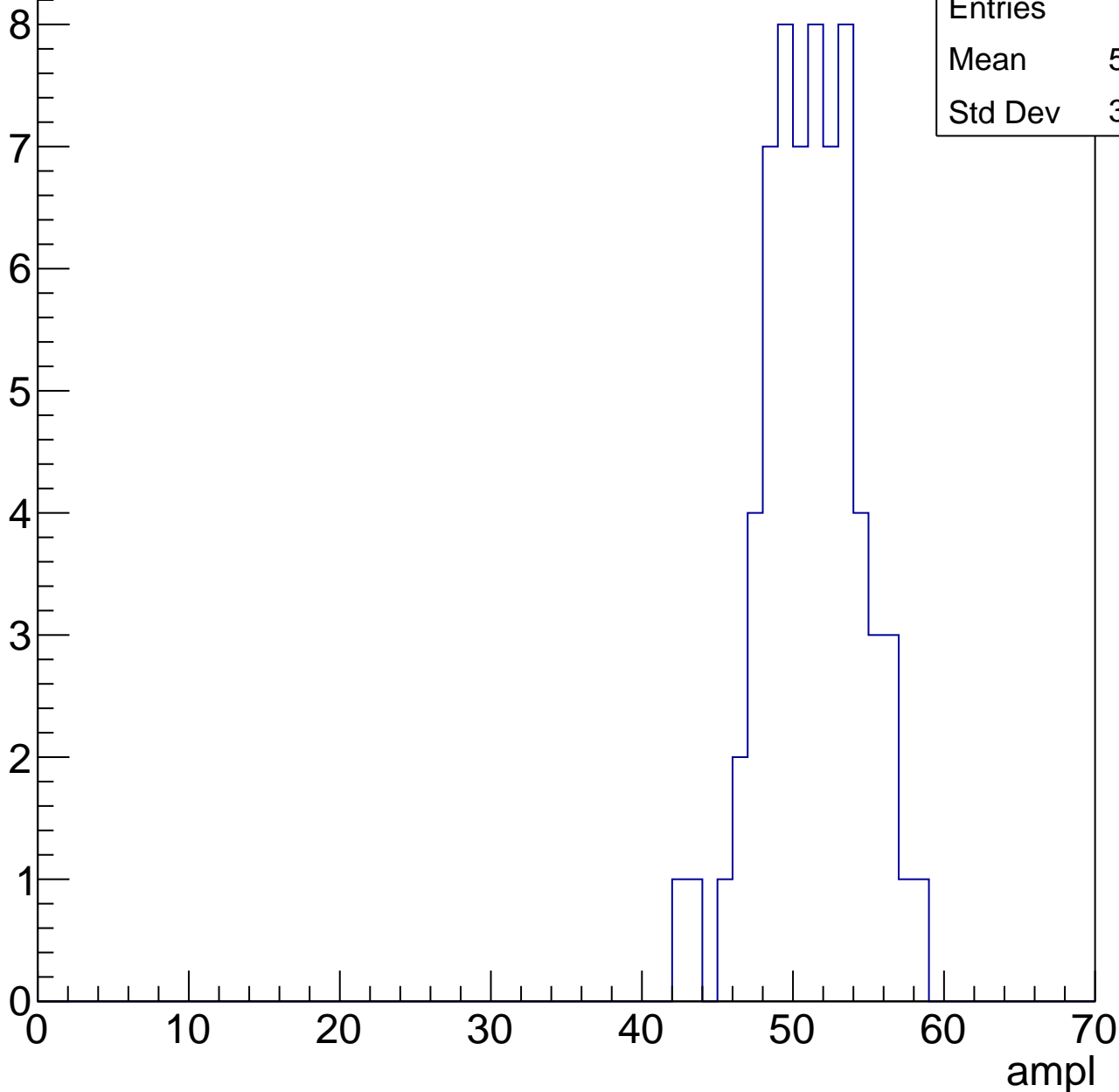


# B0L001S, U24-ch1, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

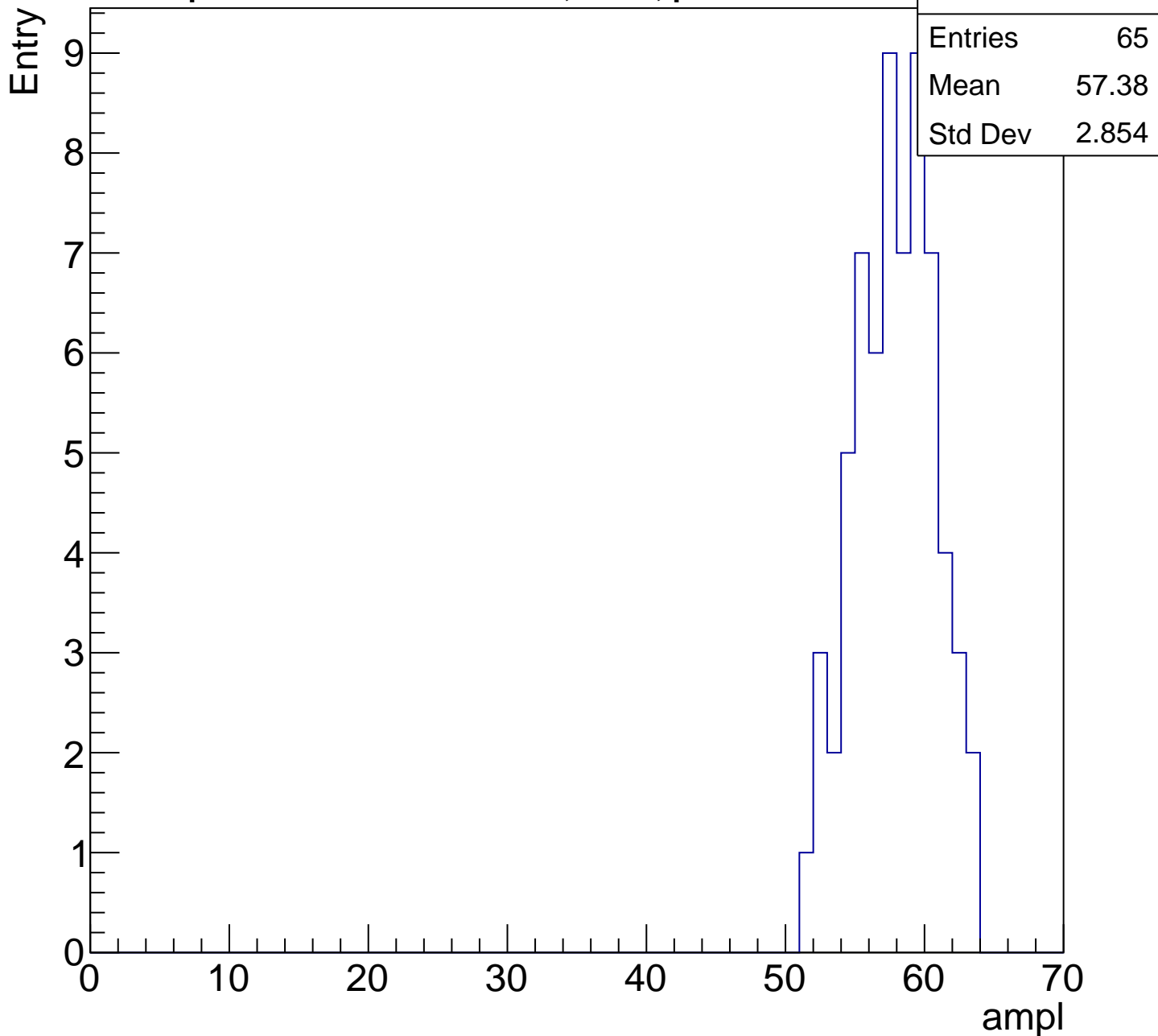
Entry

Entries	66
Mean	50.73
Std Dev	3.198



# B0L001S, U24-ch1, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

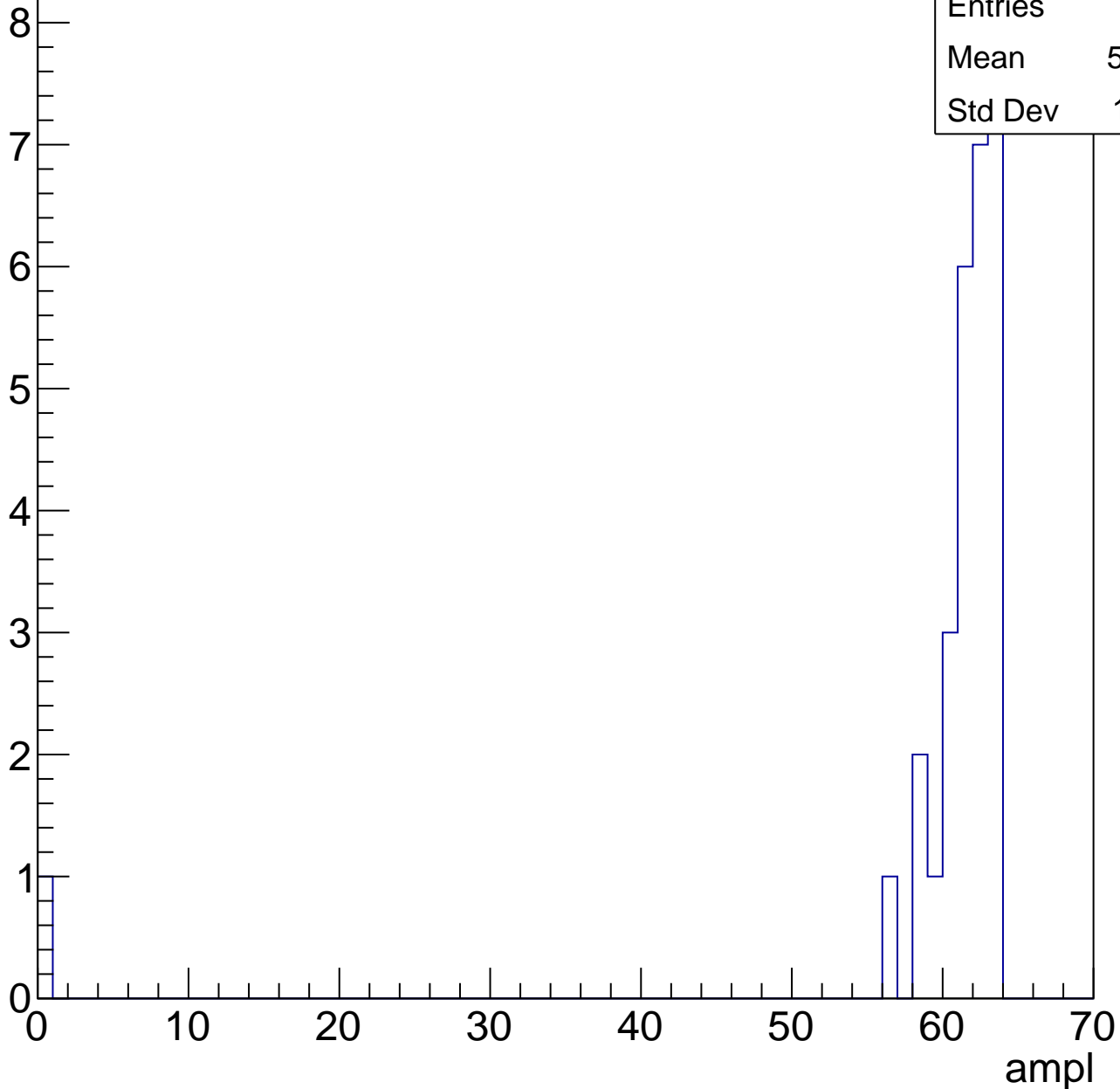


# B0L001S, U24-ch1, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	29
Mean	59.14
Std Dev	11.31



# B0L001S, U24-ch1, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U24-ch1, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U24-ch2, adc0

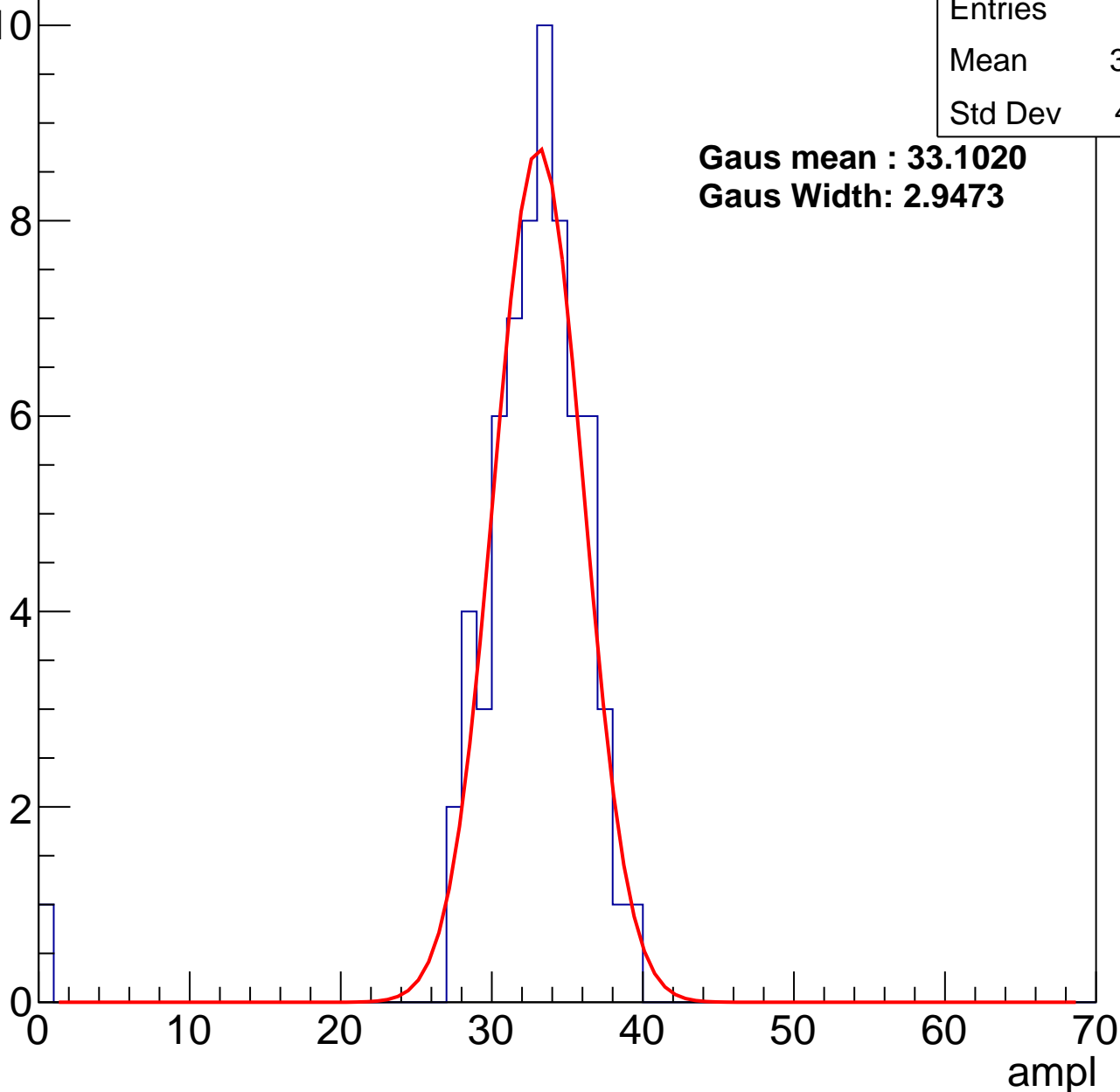
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	32.15
Std Dev	4.841

**Gaus mean : 33.1020**

**Gaus Width: 2.9473**



# B0L001S, U24-ch2, adc1

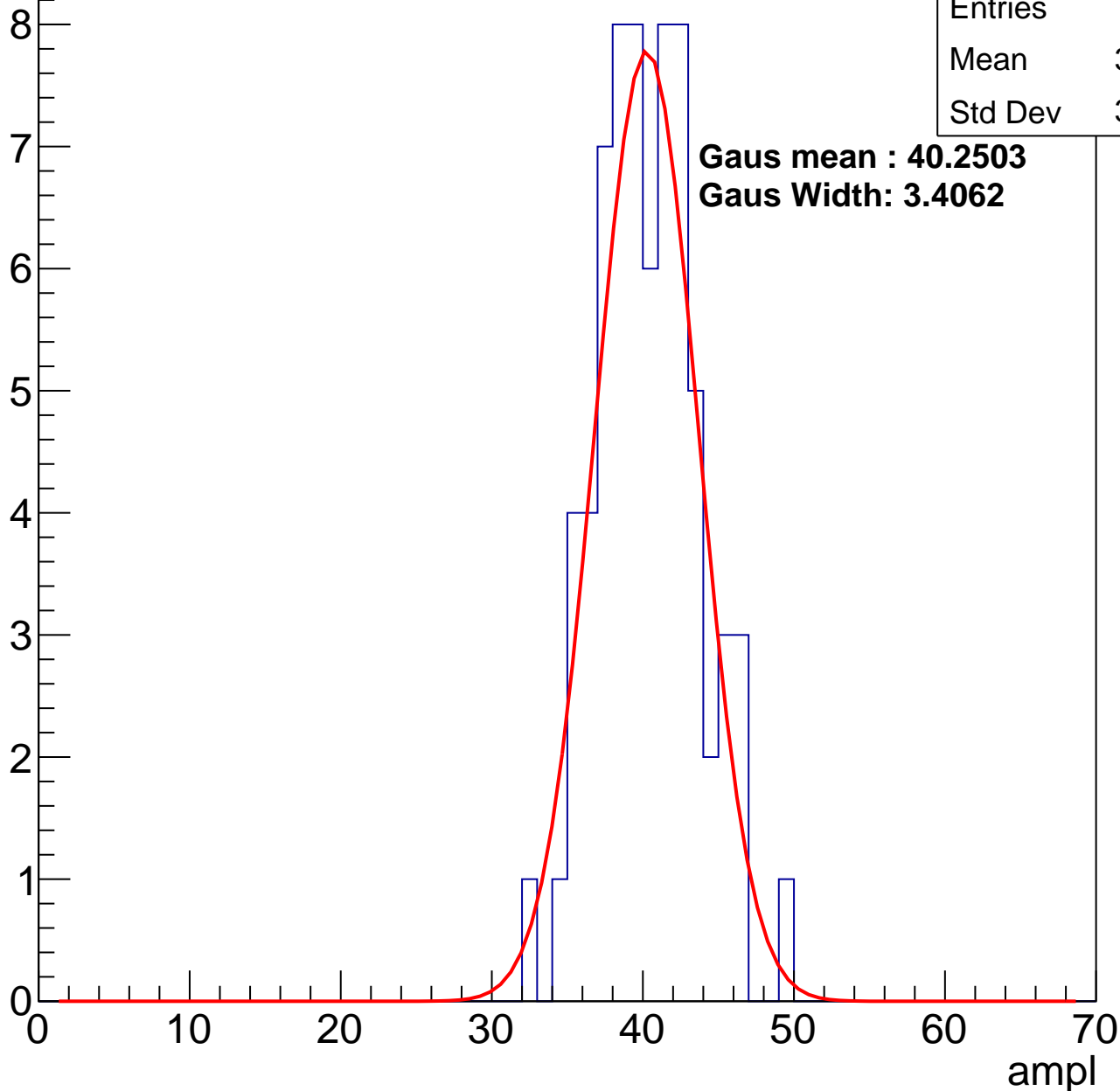
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	39.91
Std Dev	3.291

**Gaus mean : 40.2503**

**Gaus Width: 3.4062**



# B0L001S, U24-ch2, adc2

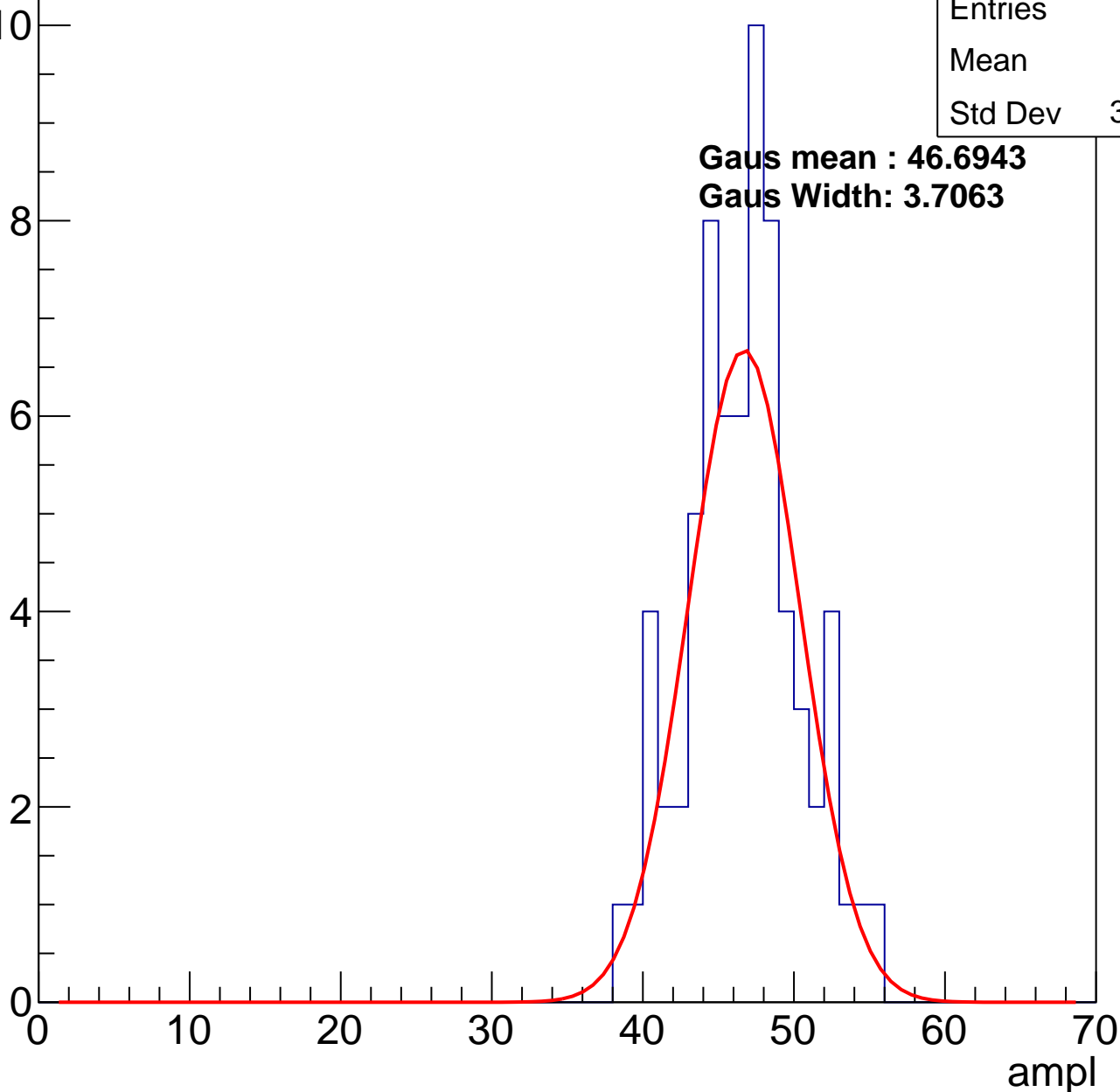
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	46.2
Std Dev	3.678

**Gaus mean : 46.6943**

**Gaus Width: 3.7063**

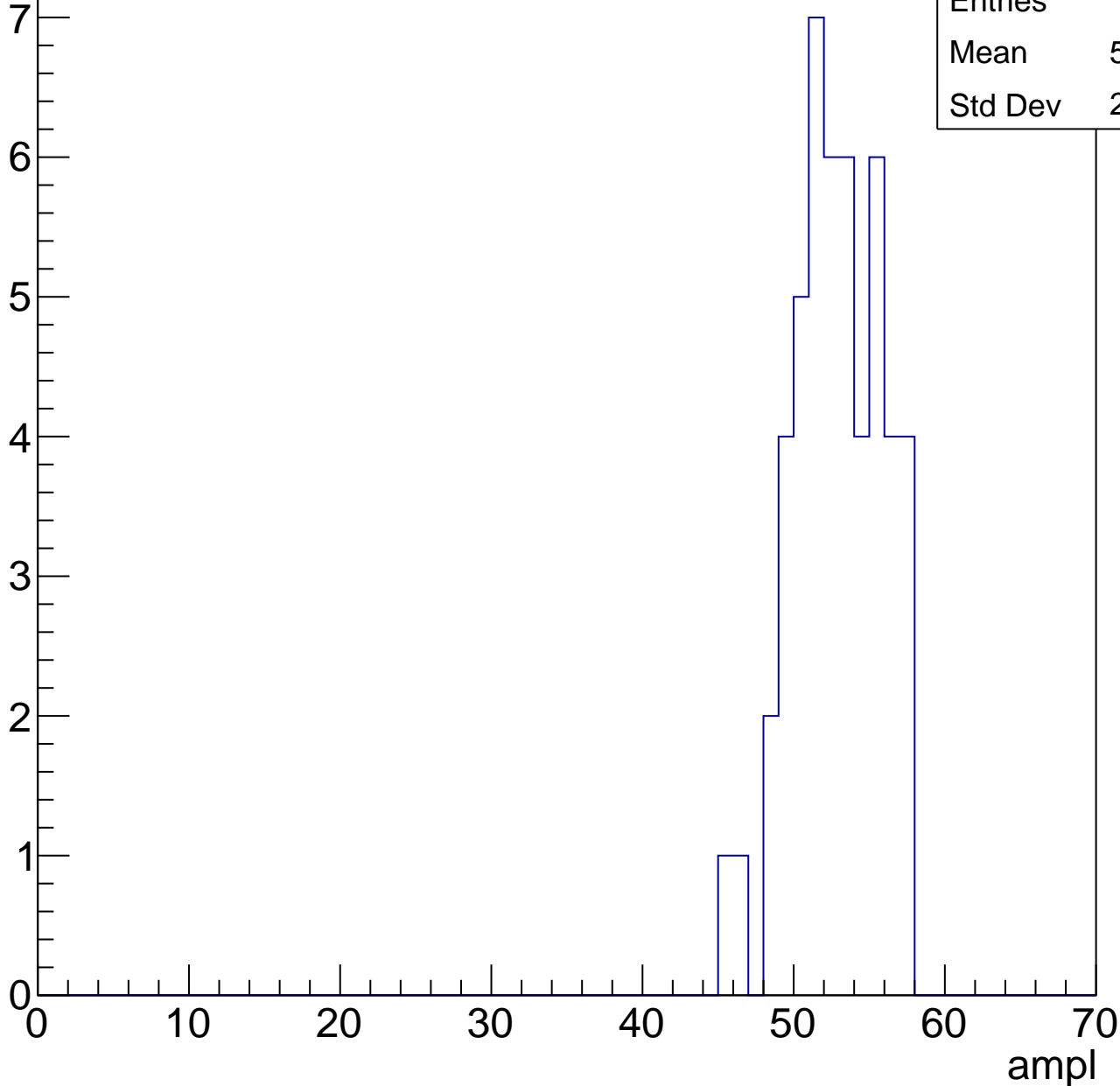


# B0L001S, U24-ch2, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	50
Mean	52.36
Std Dev	2.876

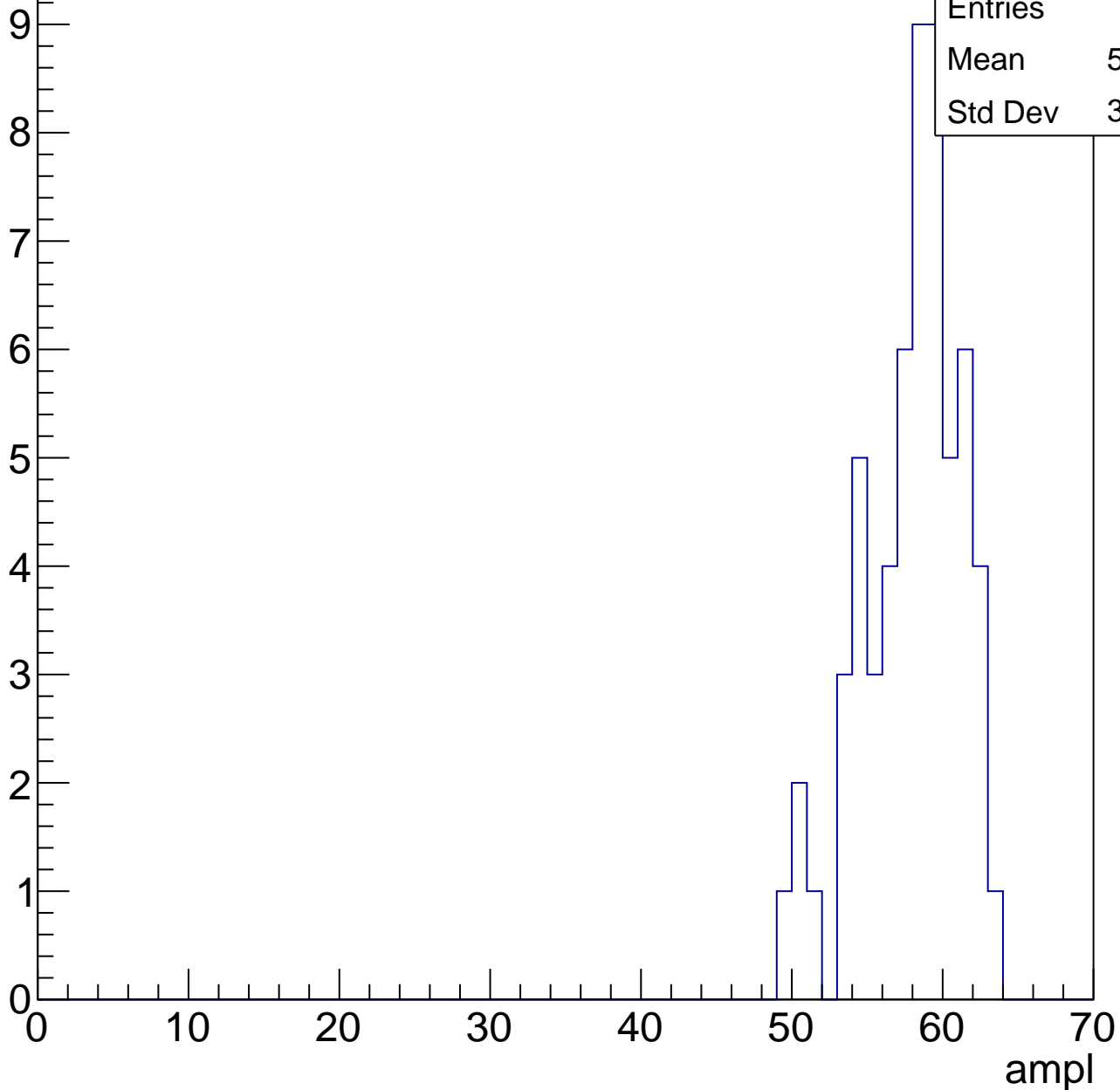


# B0L001S, U24-ch2, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	57.46
Std Dev	3.233

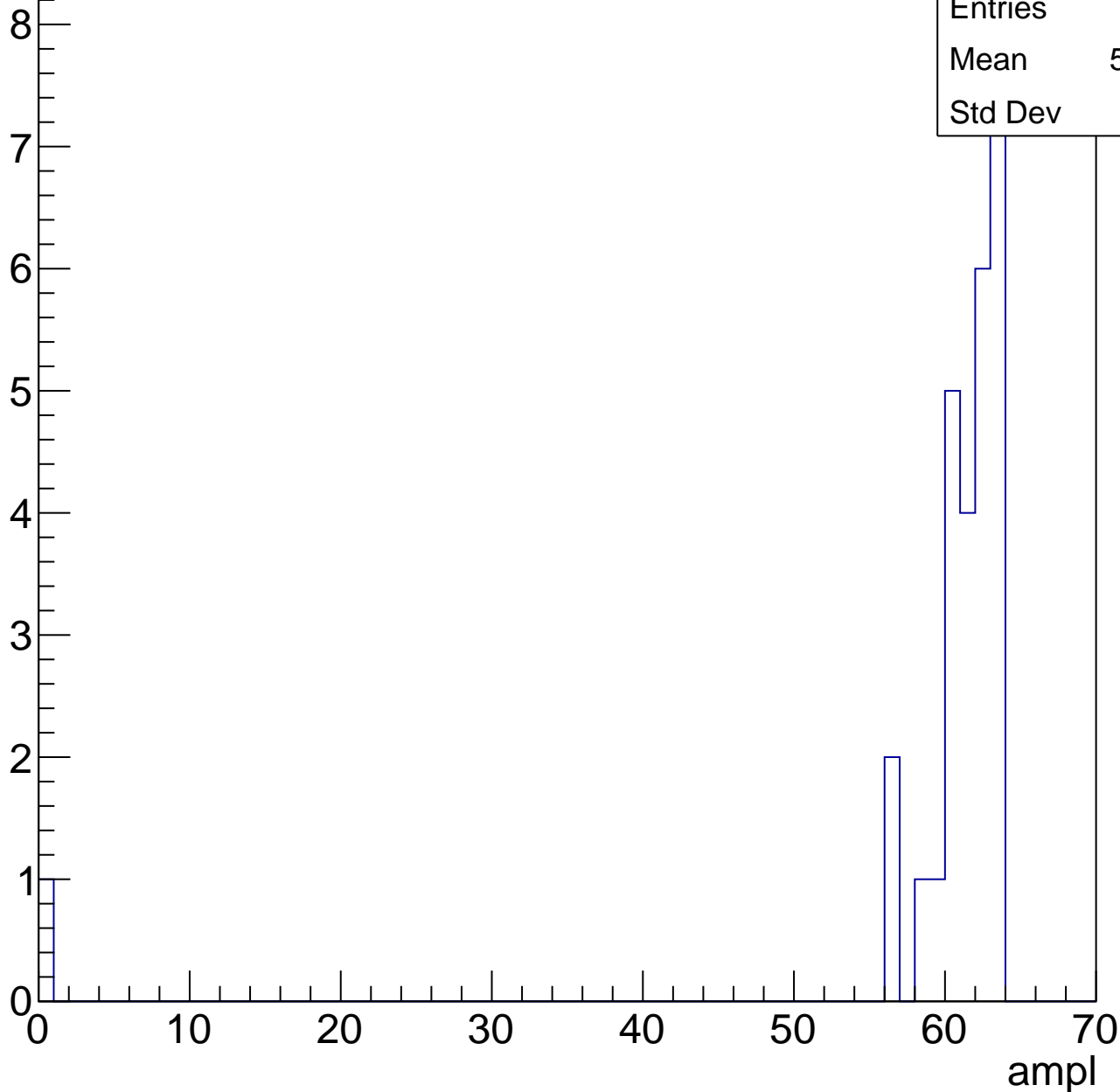


# B0L001S, U24-ch2, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

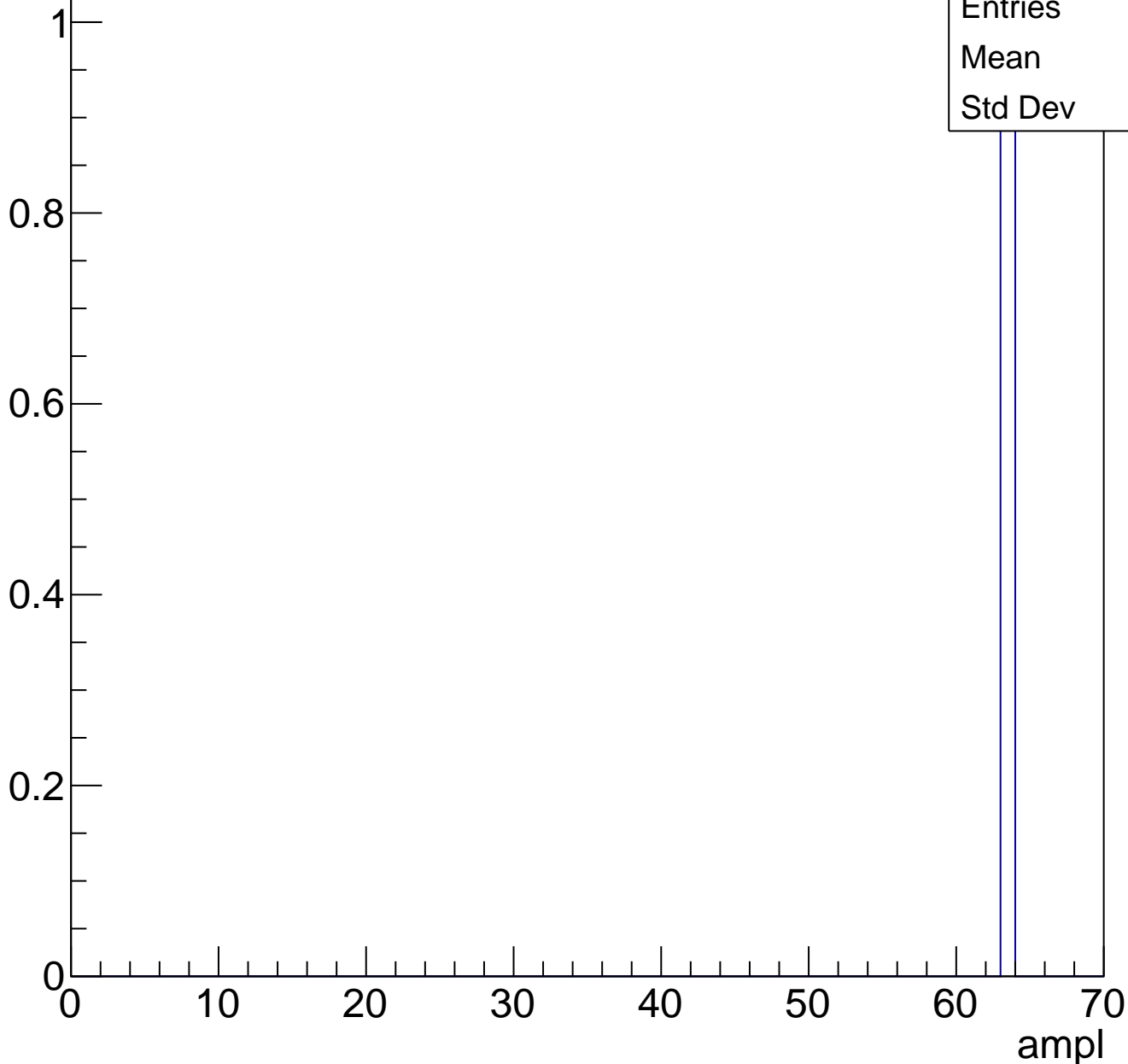
Entries	28
Mean	58.89
Std Dev	11.5



# B0L001S, U24-ch2, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch2, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U24-ch3, adc0

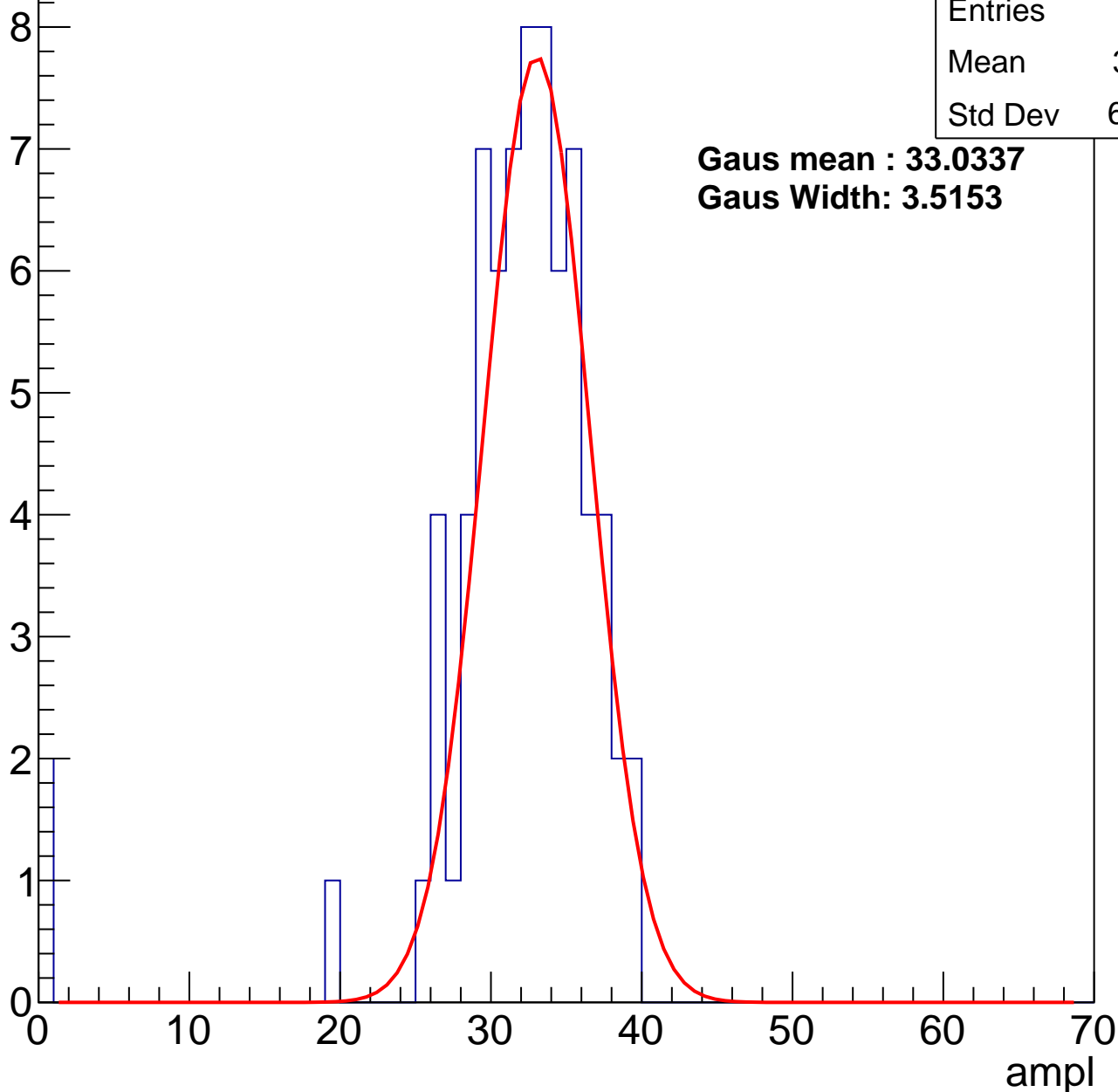
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	31.11
Std Dev	6.328

**Gaus mean : 33.0337**

**Gaus Width: 3.5153**



# B0L001S, U24-ch3, adc1

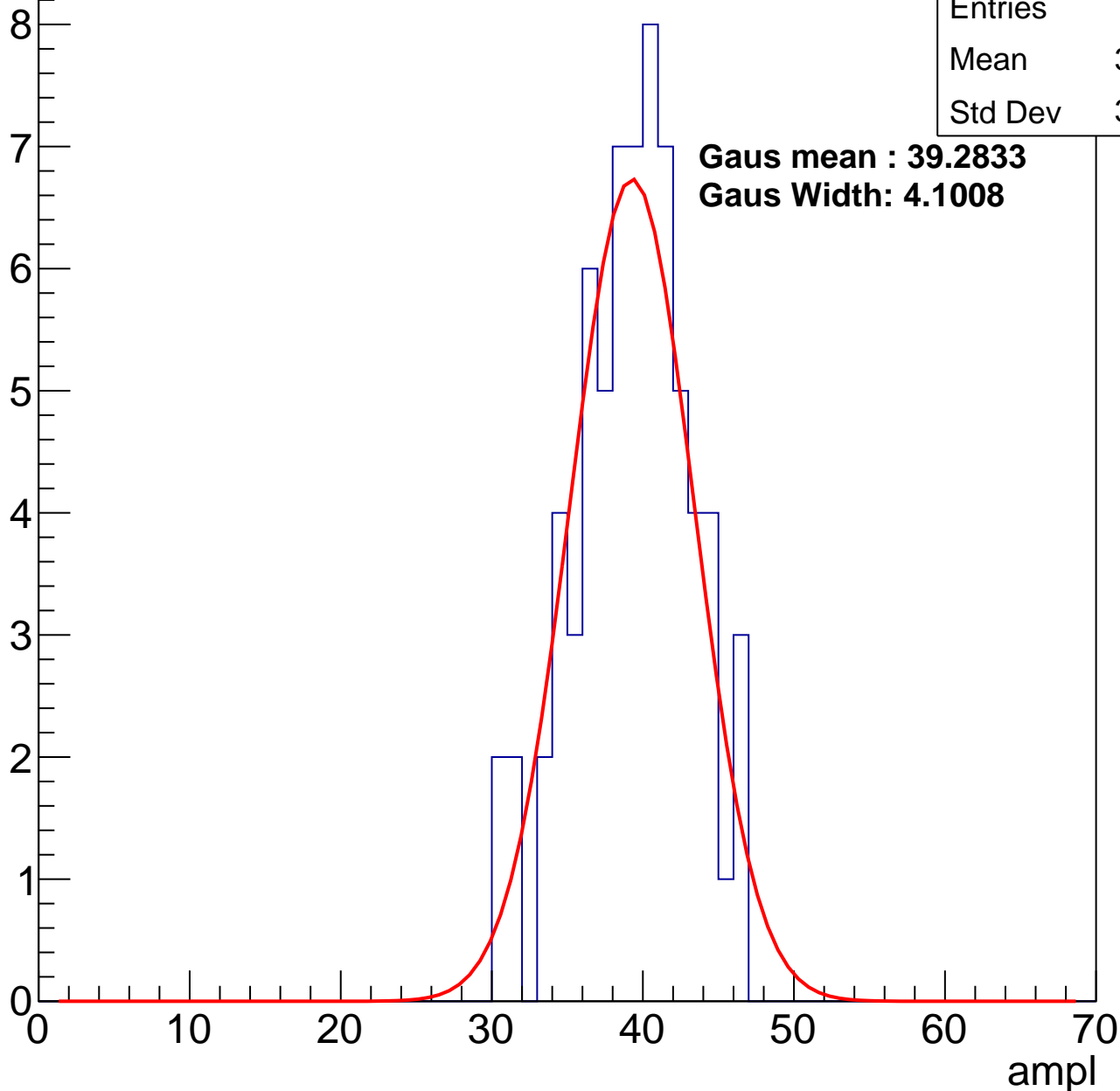
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	38.81
Std Dev	3.811

**Gaus mean : 39.2833**

**Gaus Width: 4.1008**



# B0L001S, U24-ch3, adc2

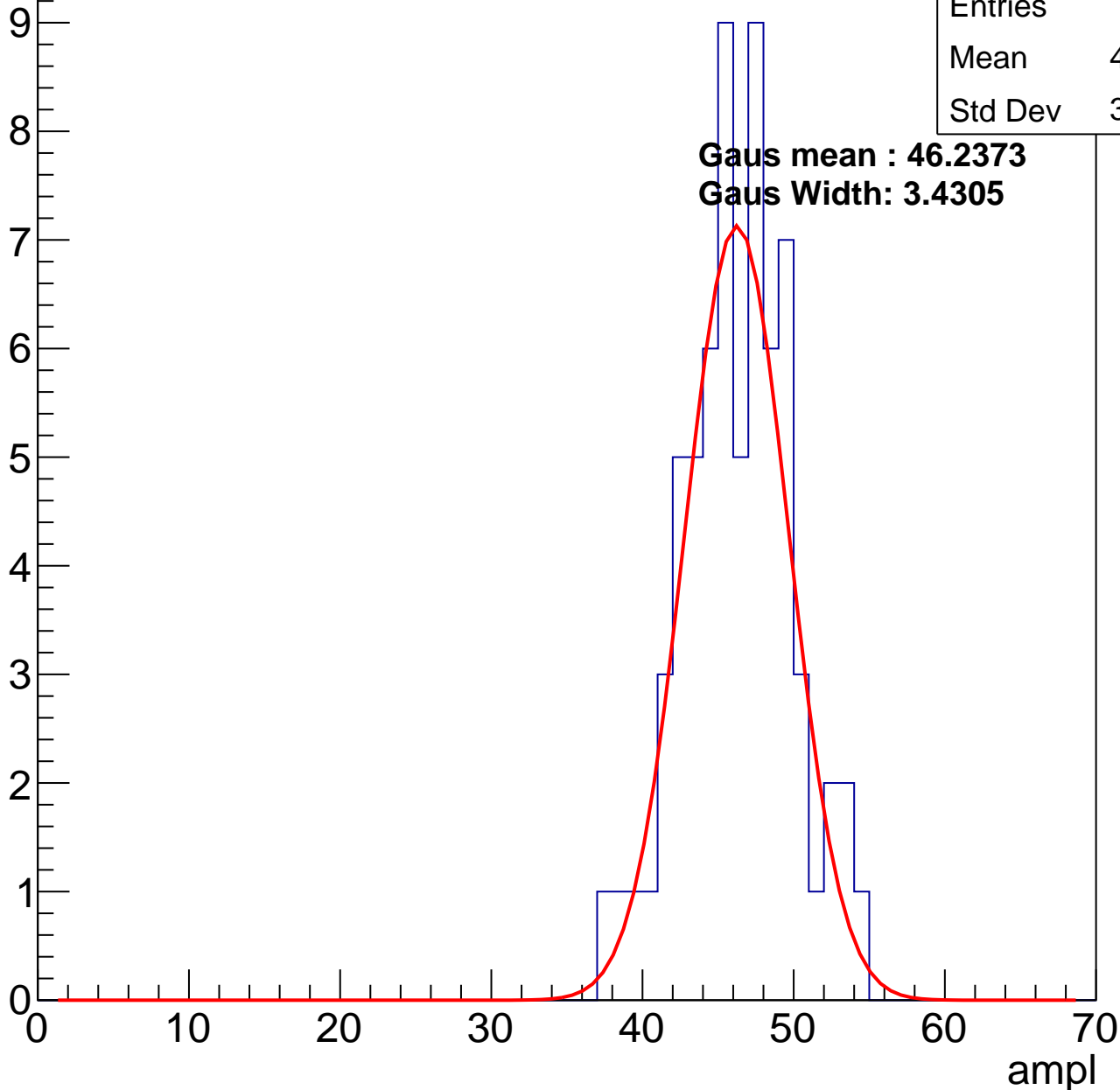
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	45.88
Std Dev	3.567

**Gaus mean : 46.2373**

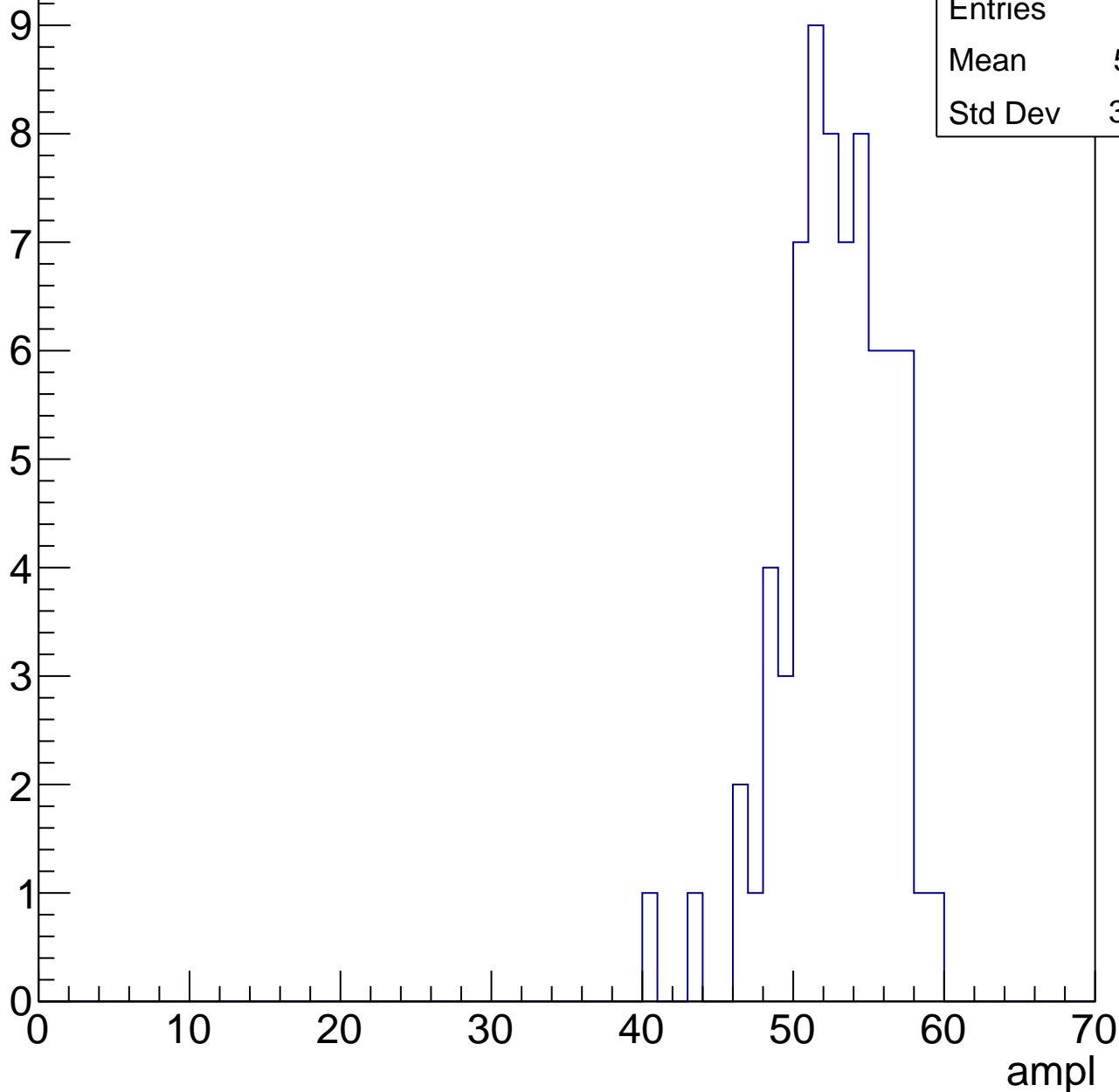
**Gaus Width: 3.4305**



# B0L001S, U24-ch3, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U24-ch3, adc4

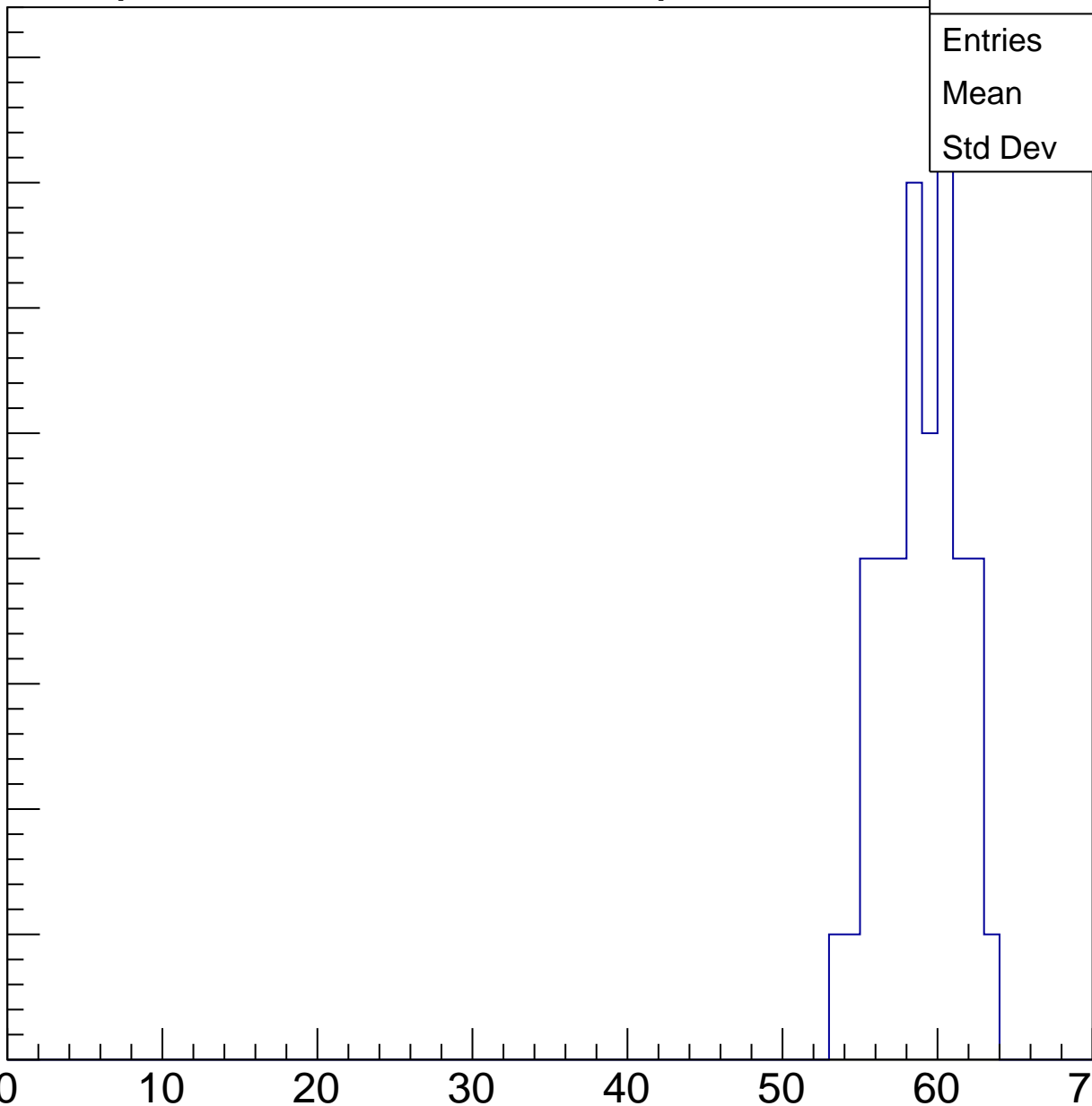
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	43
Mean	58.49
Std Dev	2.405

ampl

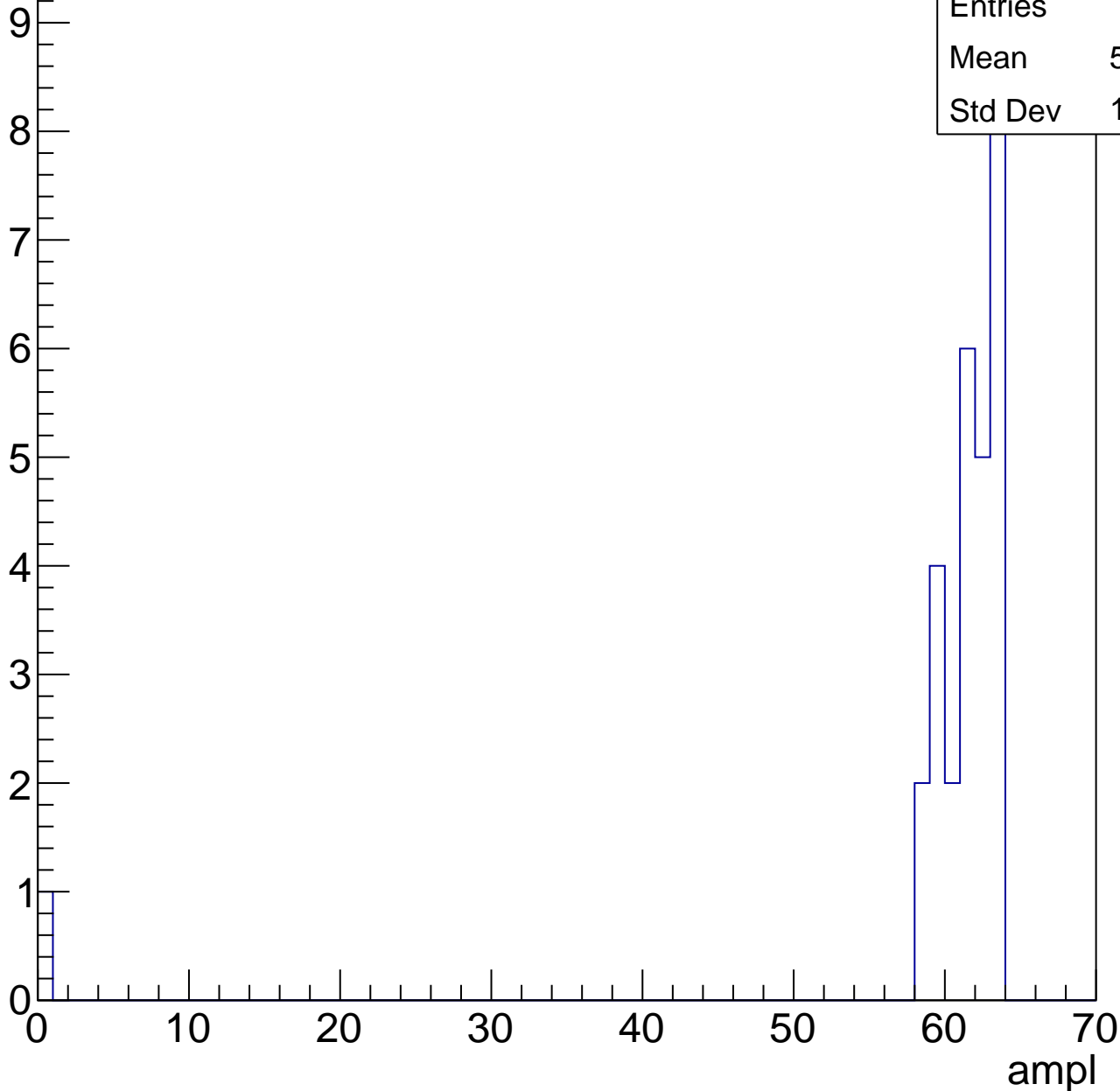


# B0L001S, U24-ch3, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	29
Mean	59.14
Std Dev	11.29



# B0L001S, U24-ch3, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch3, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U24-ch4, adc0

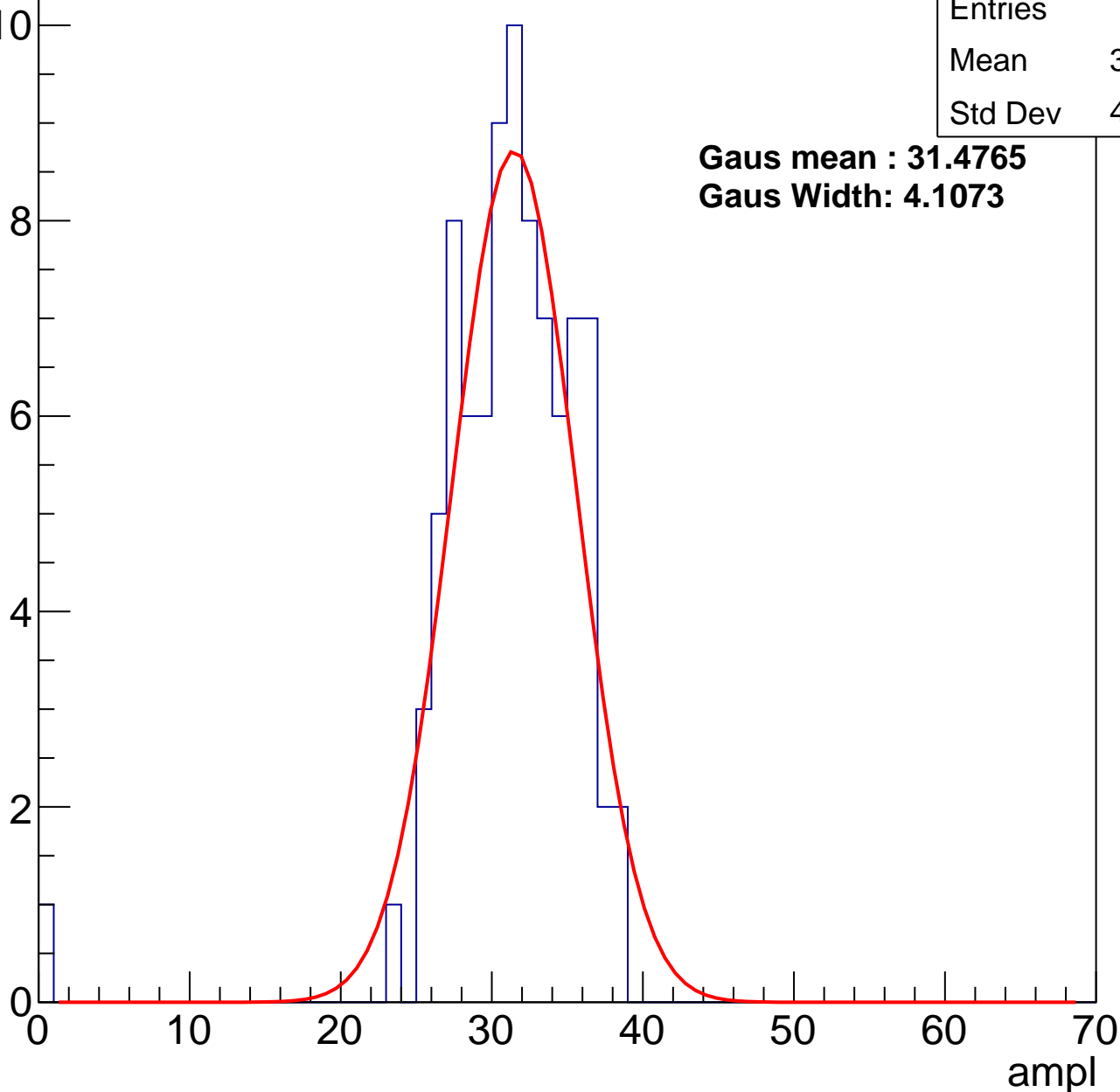
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	88
Mean	30.73
Std Dev	4.783

**Gaus mean : 31.4765**

**Gaus Width: 4.1073**



# B0L001S, U24-ch4, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	64
Mean	38.06
Std Dev	3.427

**Gaus mean : 38.6926**

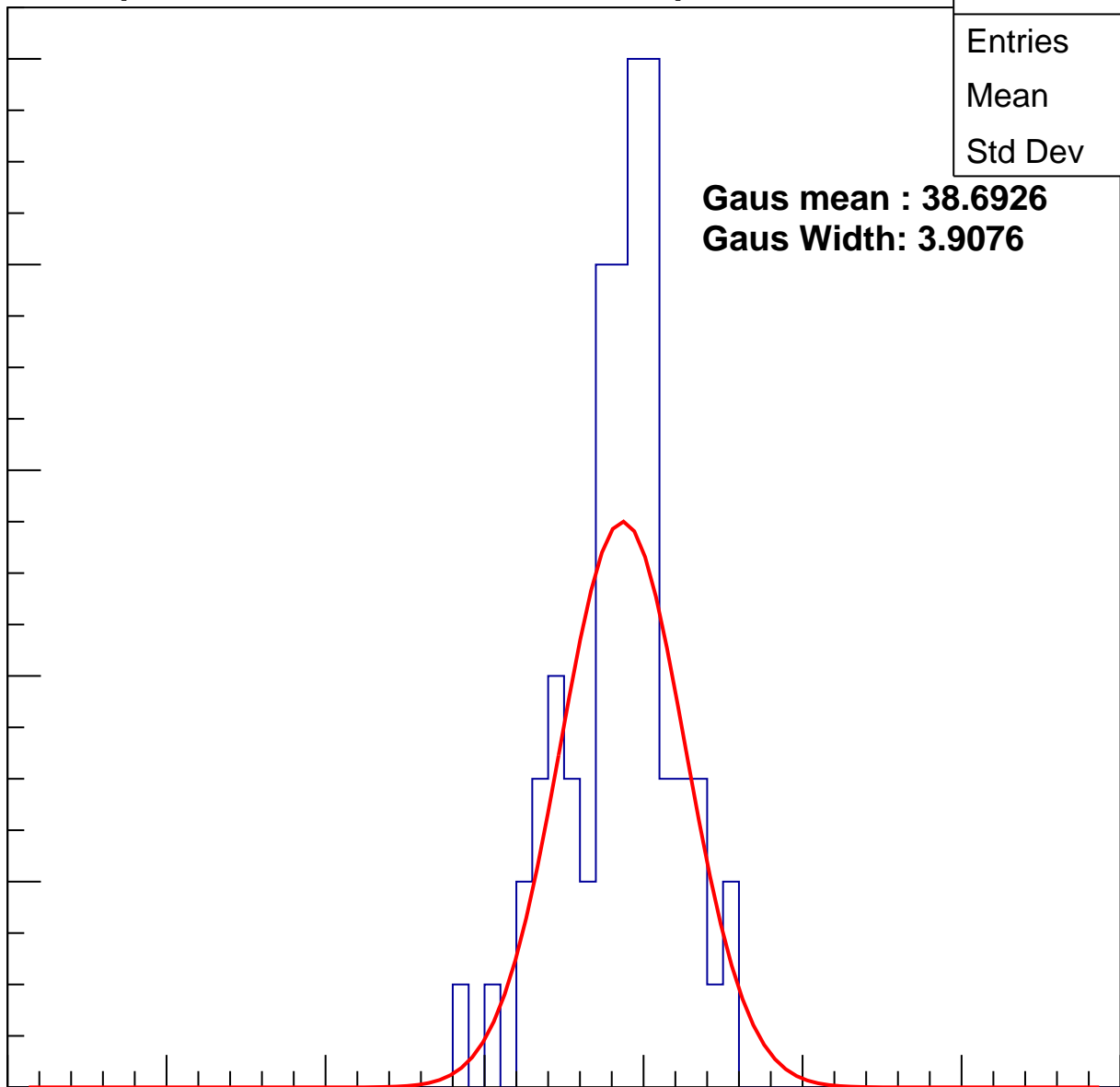
**Gaus Width: 3.9076**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

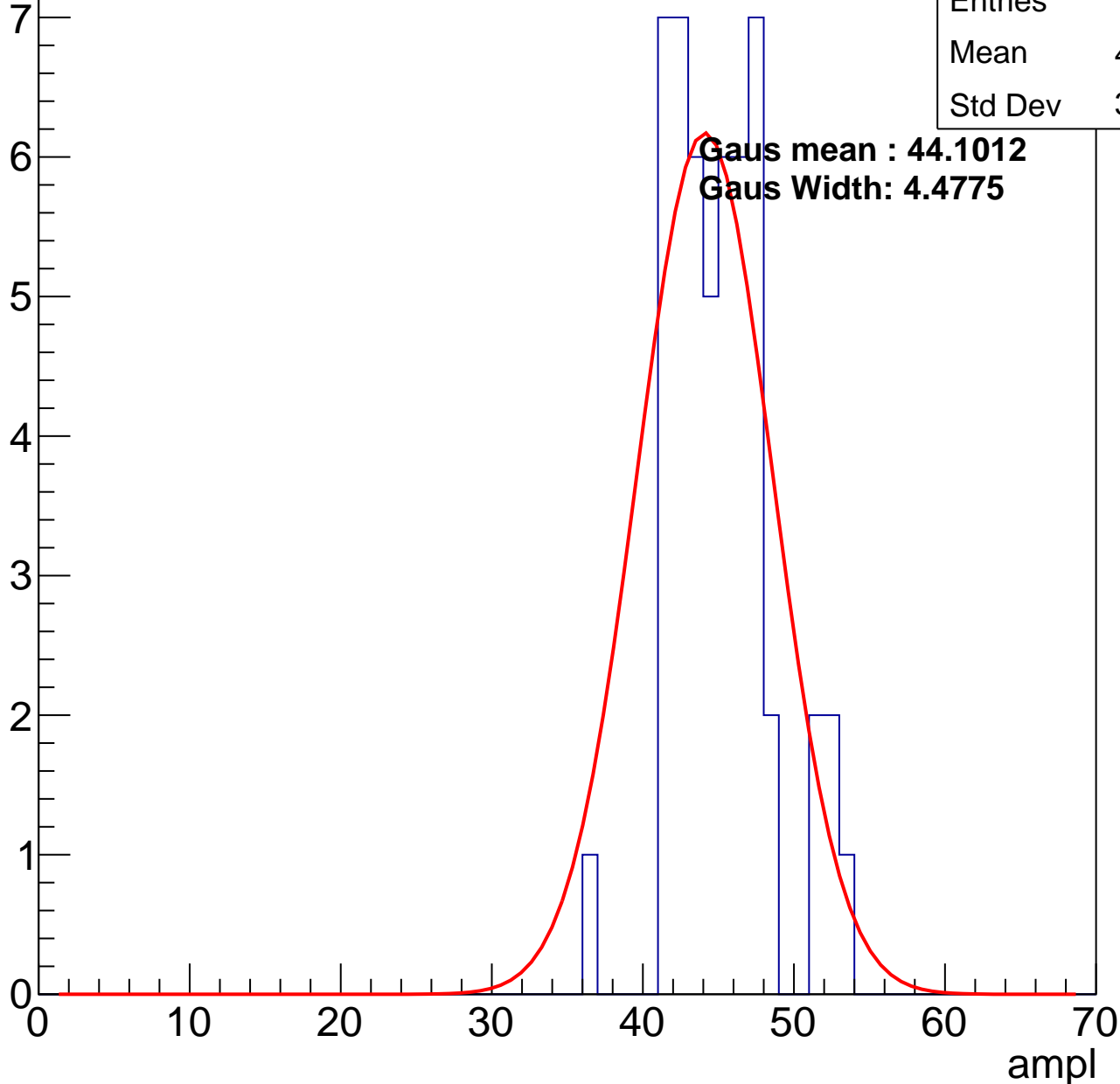


# B0L001S, U24-ch4, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	44.71
Std Dev	3.301

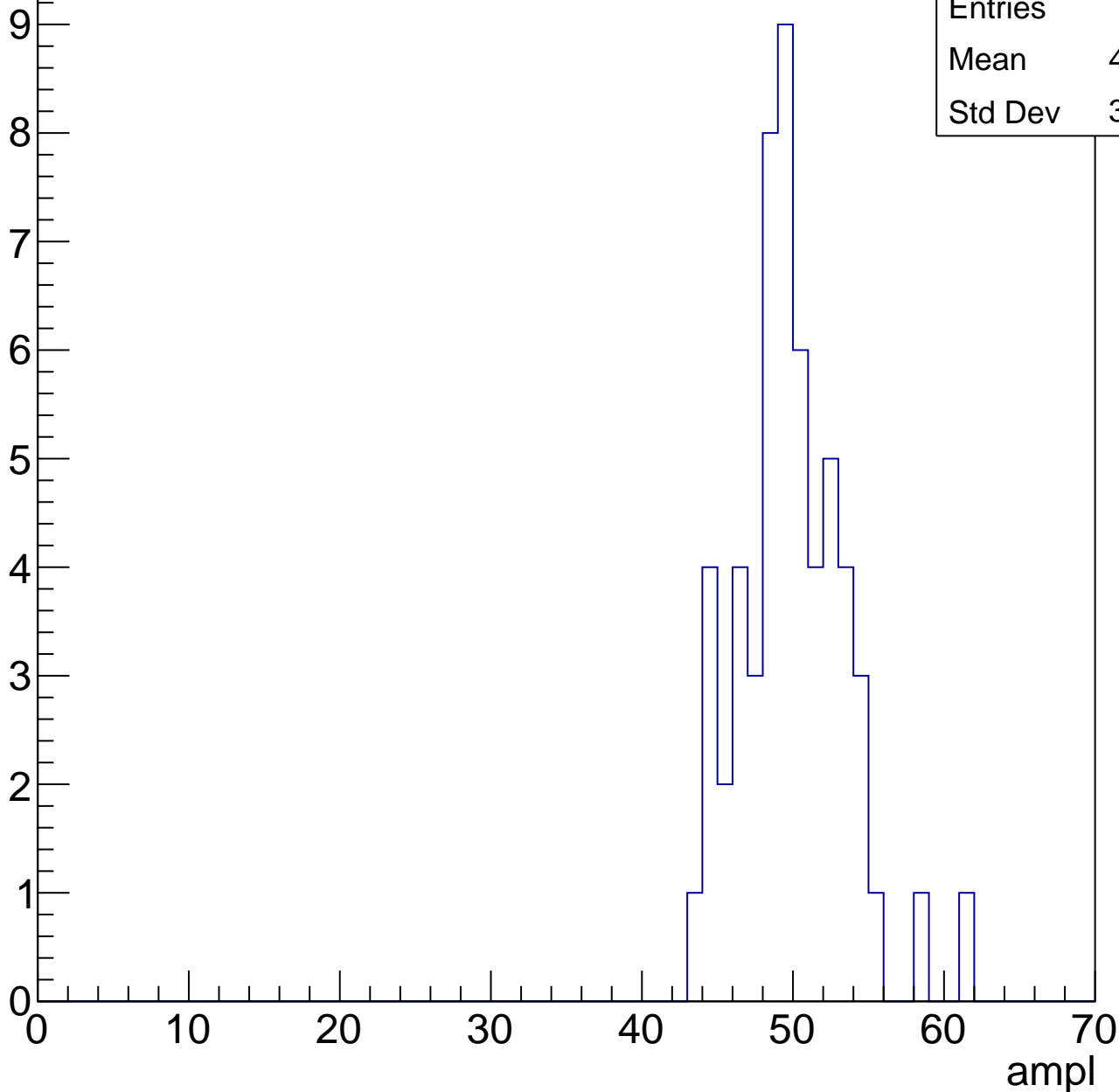


# B0L001S, U24-ch4, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	49.48
Std Dev	3.479

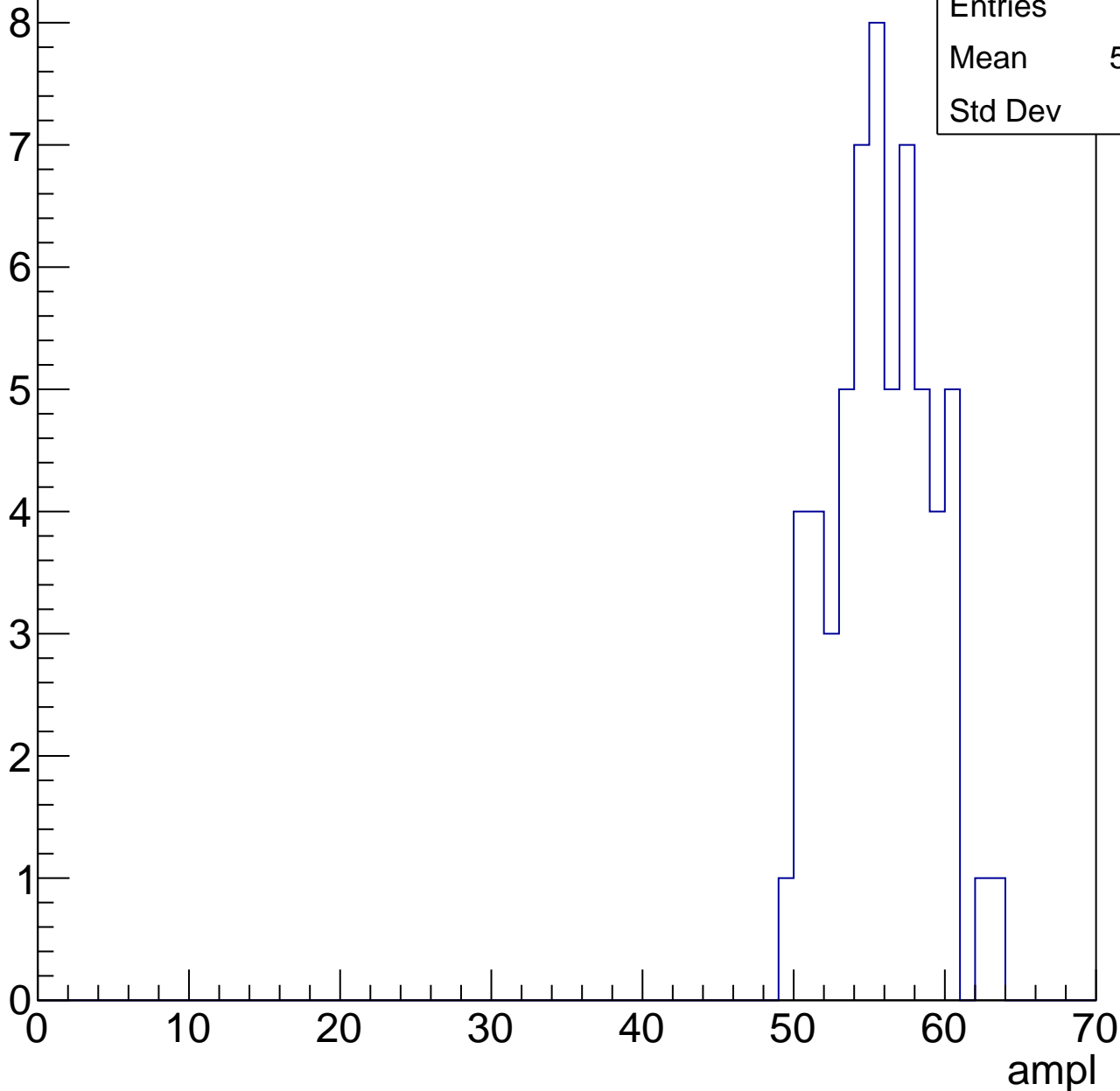


# B0L001S, U24-ch4, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	55.37
Std Dev	3.23

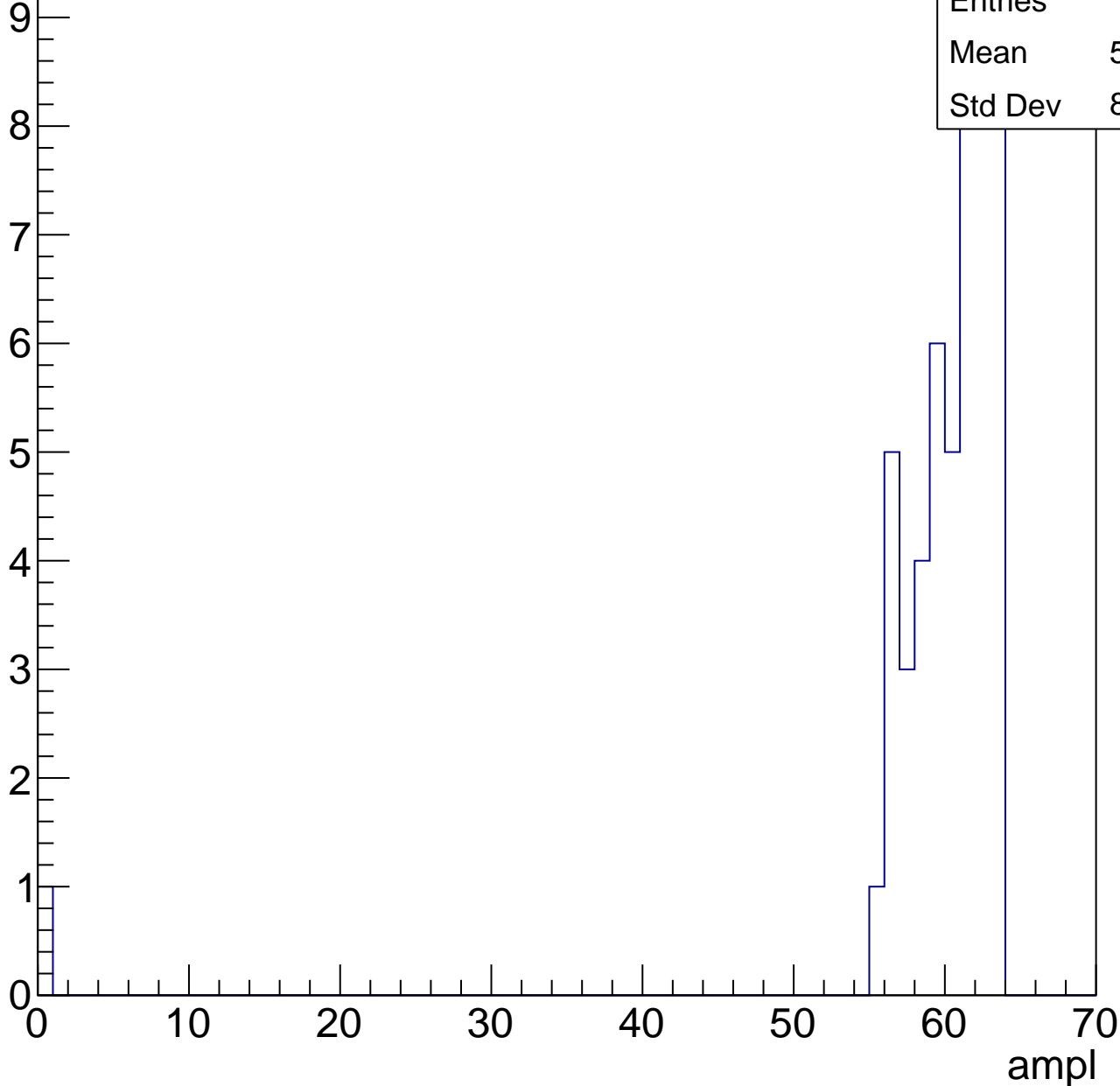


# B0L001S, U24-ch4, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	50
Mean	58.82
Std Dev	8.715



# B0L001S, U24-ch4, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch4, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U24-ch5, adc0

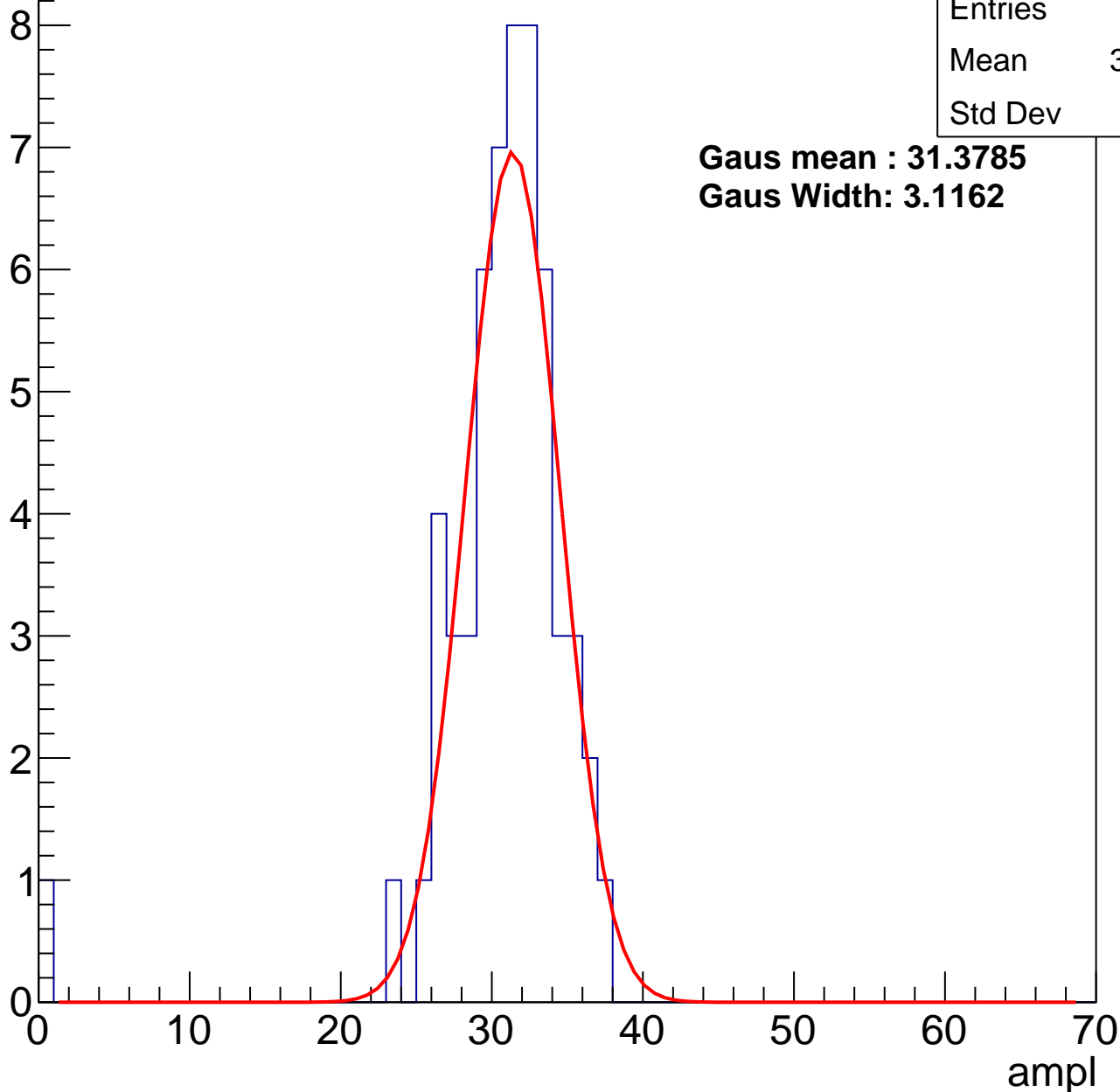
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	30.16
Std Dev	4.99

**Gaus mean : 31.3785**

**Gaus Width: 3.1162**



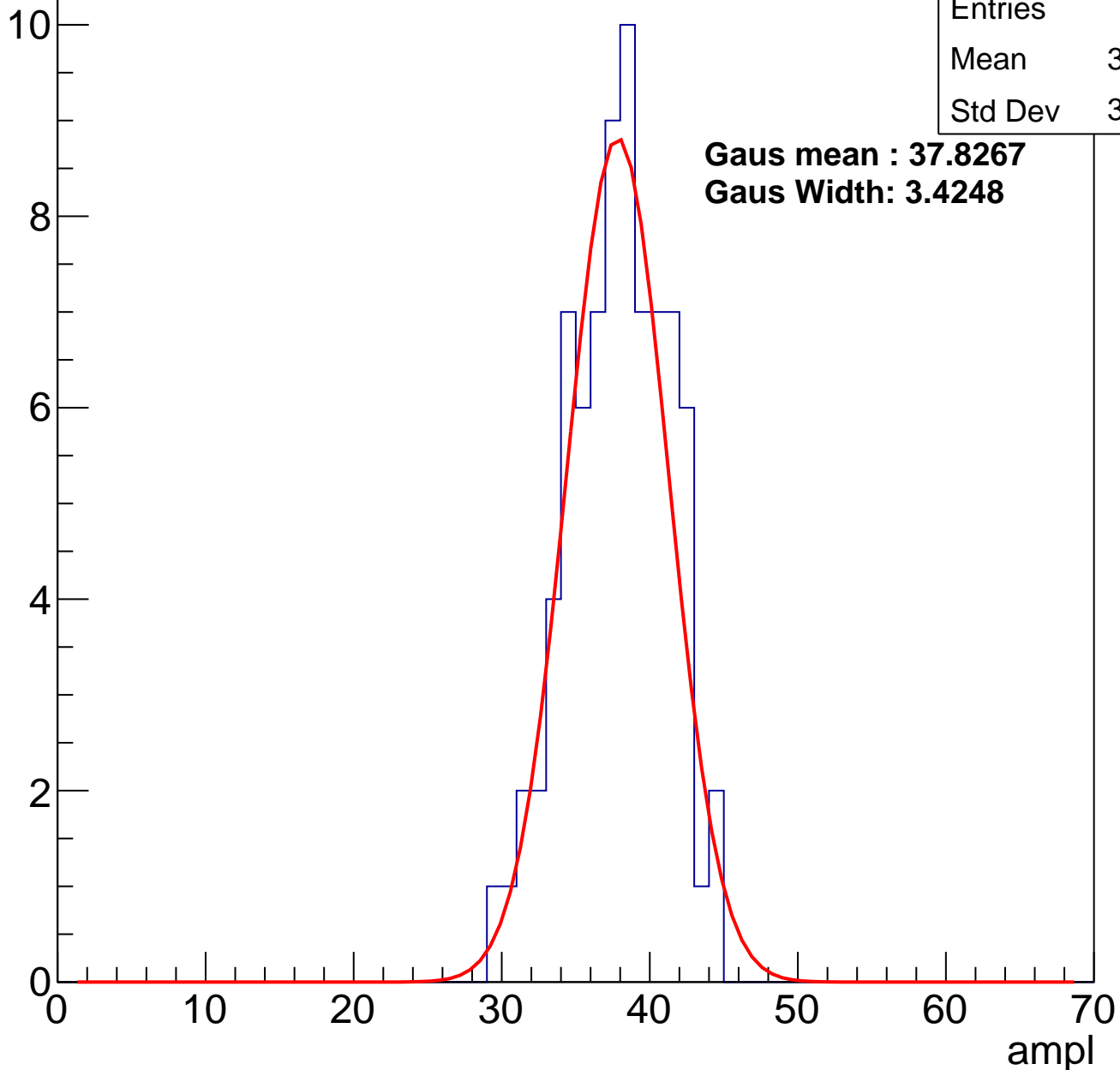
# B0L001S, U24-ch5, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	79
Mean	37.38
Std Dev	3.335

**Gaus mean : 37.8267**  
**Gaus Width: 3.4248**

Entry



# B0L001S, U24-ch5, adc2

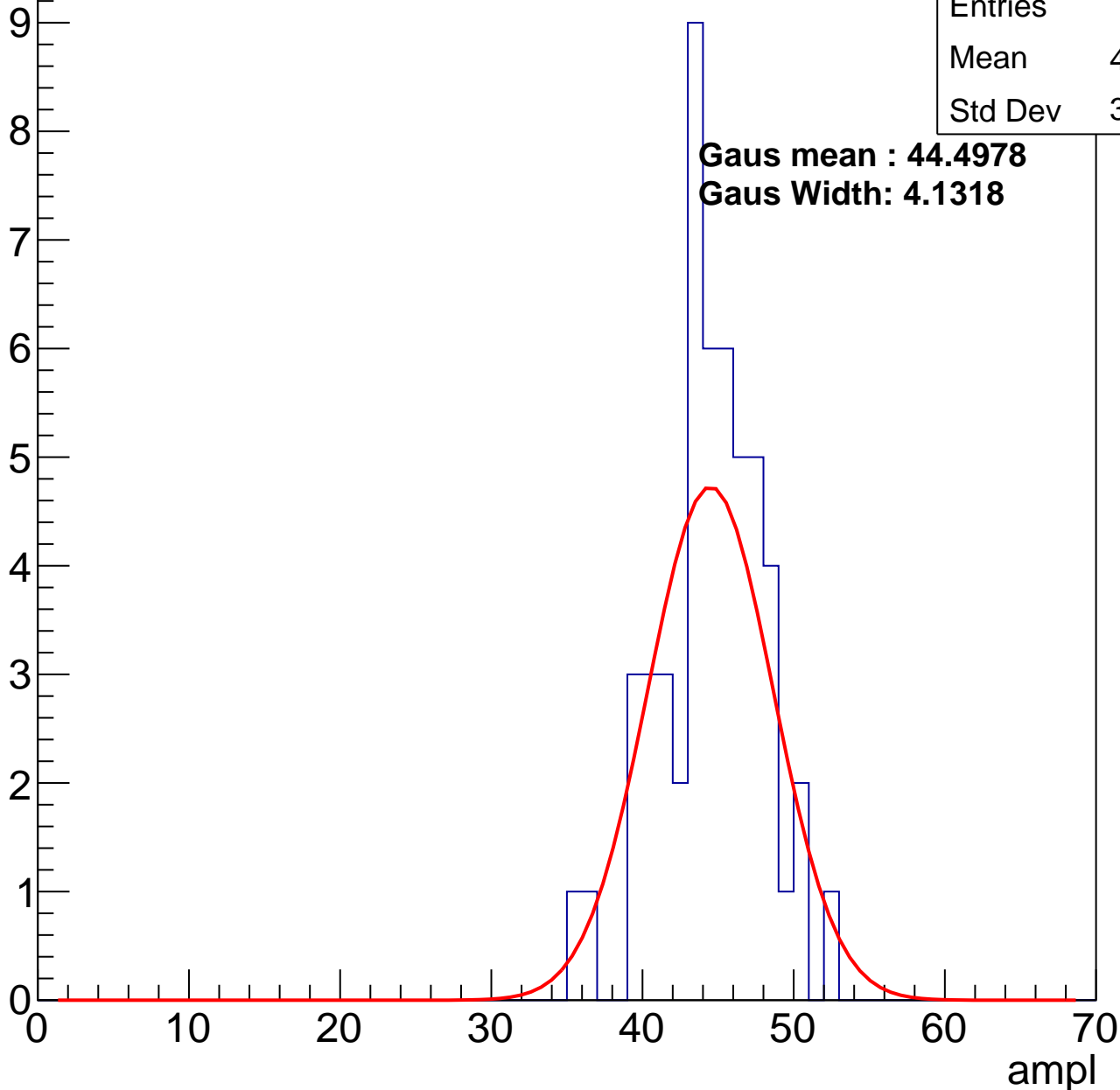
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	44.12
Std Dev	3.417

**Gaus mean : 44.4978**

**Gaus Width: 4.1318**

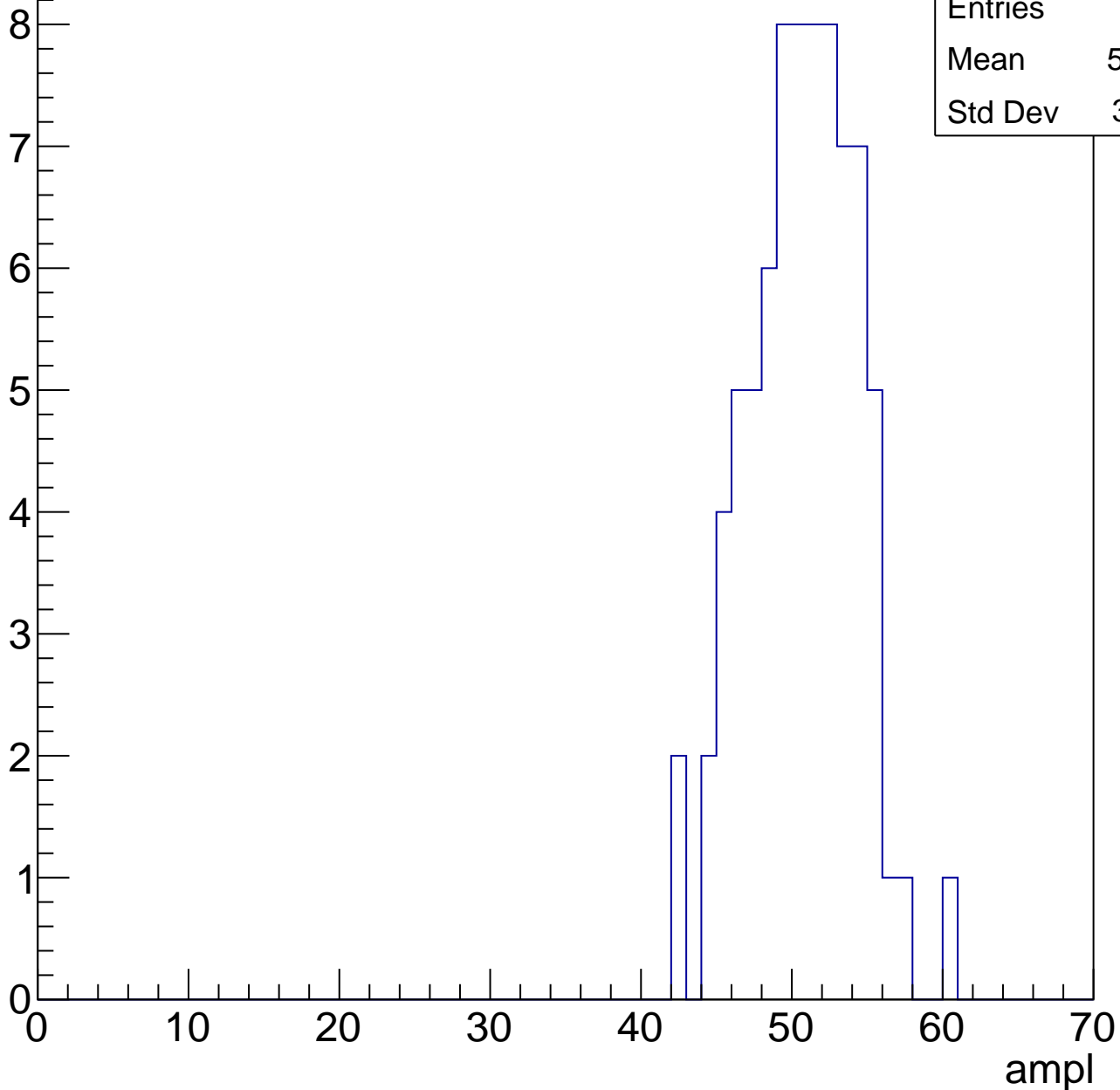


# B0L001S, U24-ch5, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	78
Mean	50.23
Std Dev	3.541

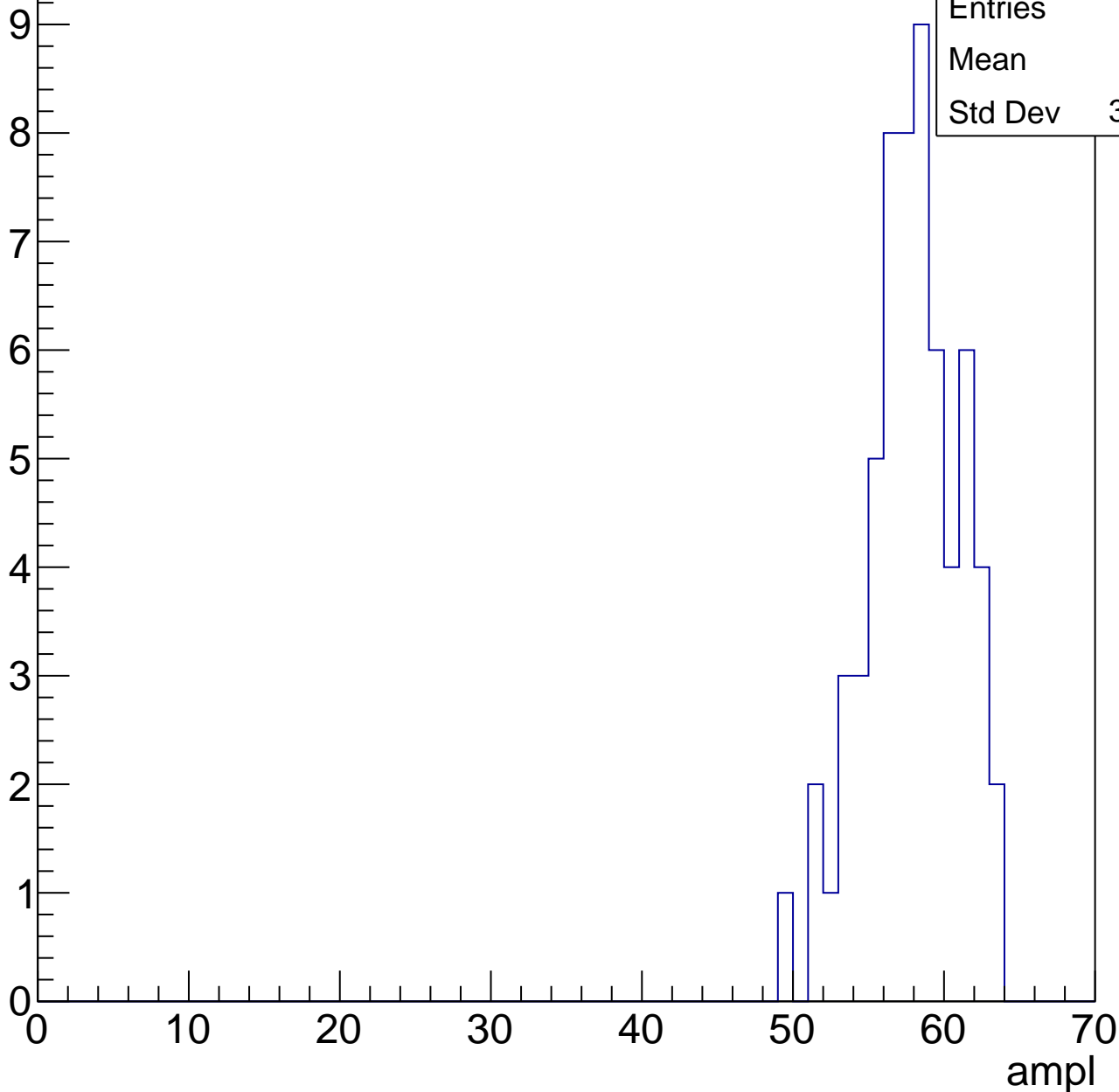


# B0L001S, U24-ch5, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	57.4
Std Dev	3.087

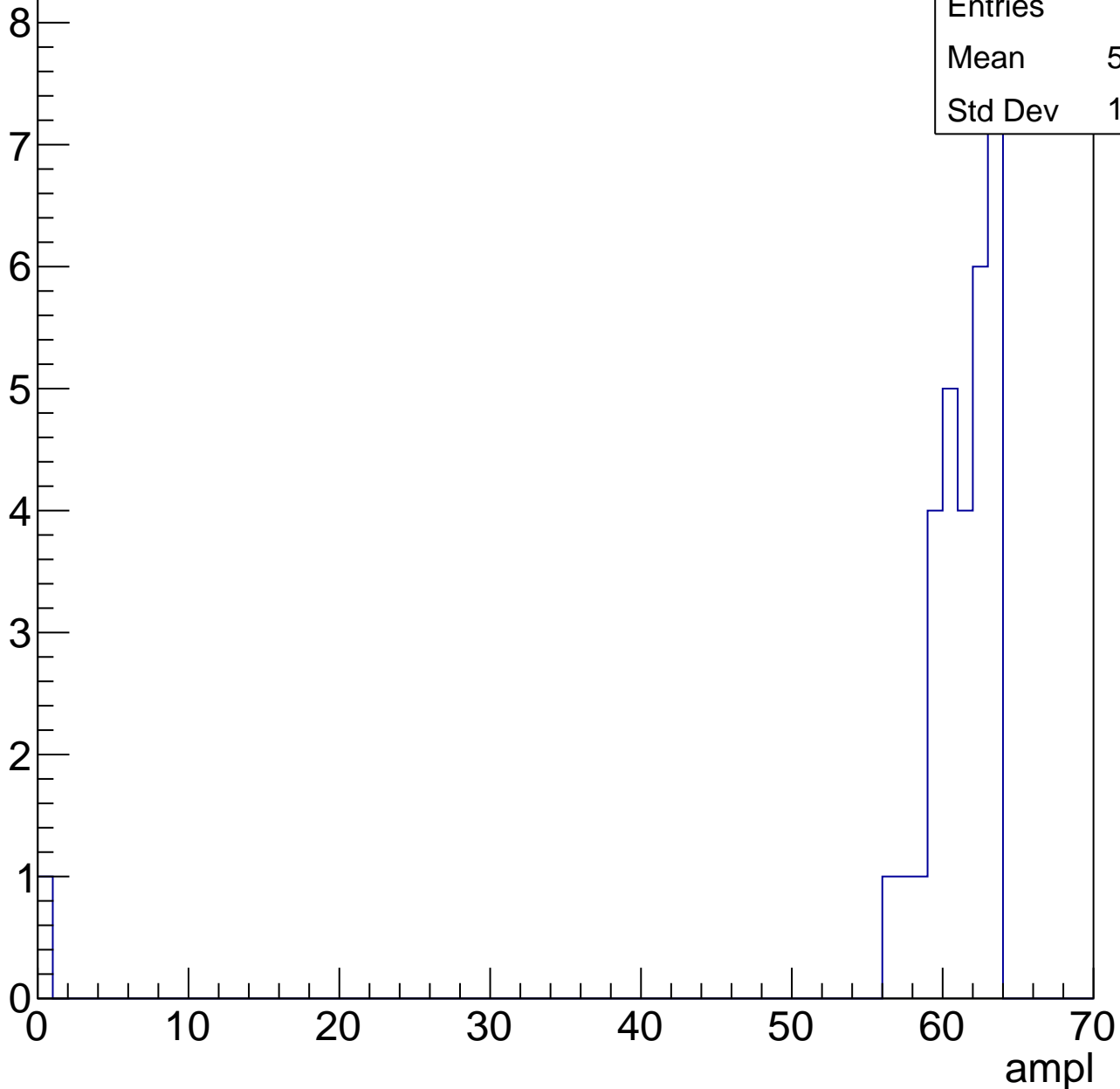


# B0L001S, U24-ch5, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	31
Mean	58.94
Std Dev	10.92



# B0L001S, U24-ch5, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U24-ch5, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U24-ch6, adc0

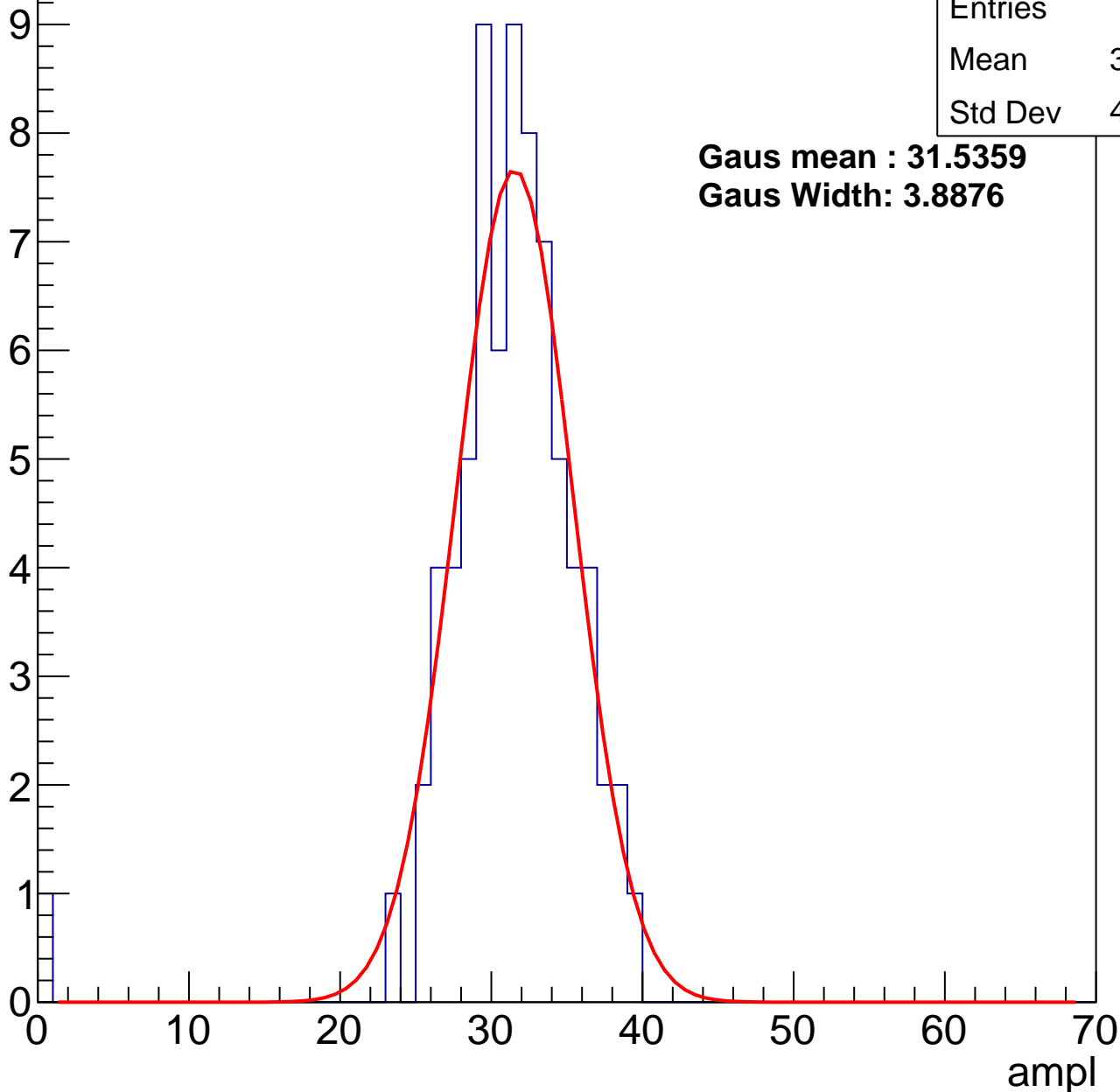
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	30.74
Std Dev	4.962

**Gaus mean : 31.5359**

**Gaus Width: 3.8876**



# B0L001S, U24-ch6, adc1

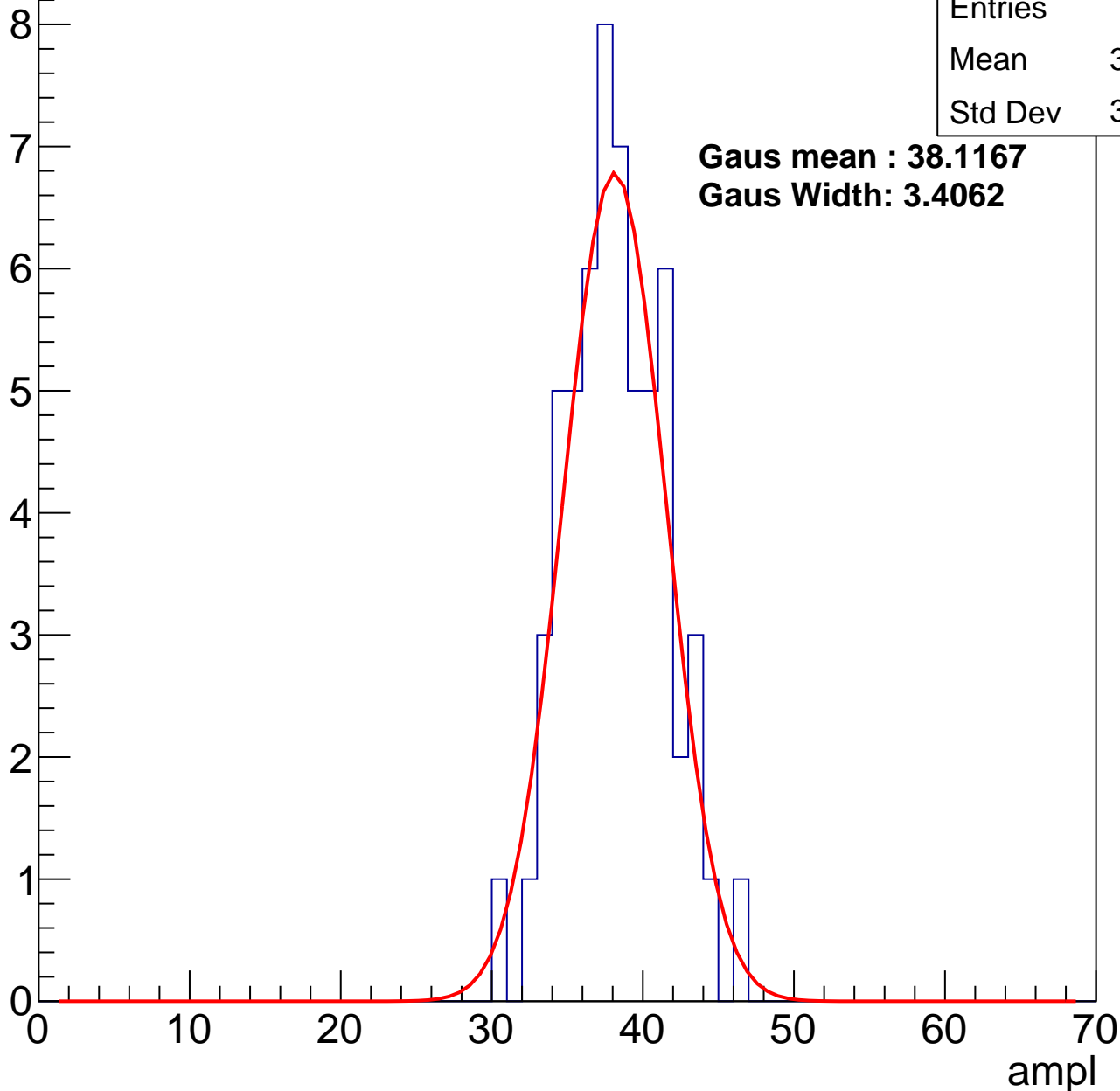
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	37.76
Std Dev	3.228

**Gaus mean : 38.1167**

**Gaus Width: 3.4062**



# B0L001S, U24-ch6, adc2

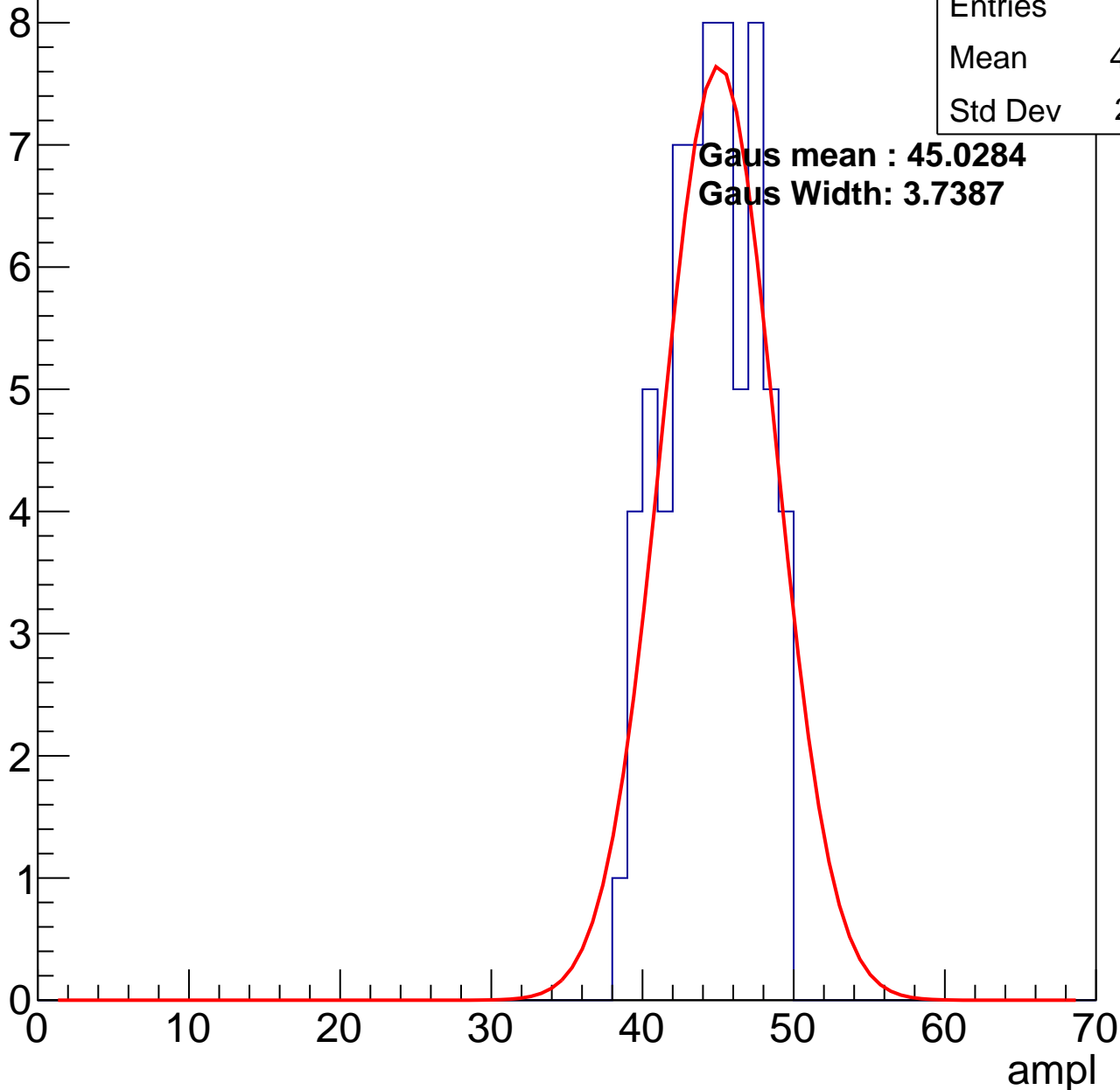
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	44.05
Std Dev	2.931

**Gaus mean : 45.0284**

**Gaus Width: 3.7387**

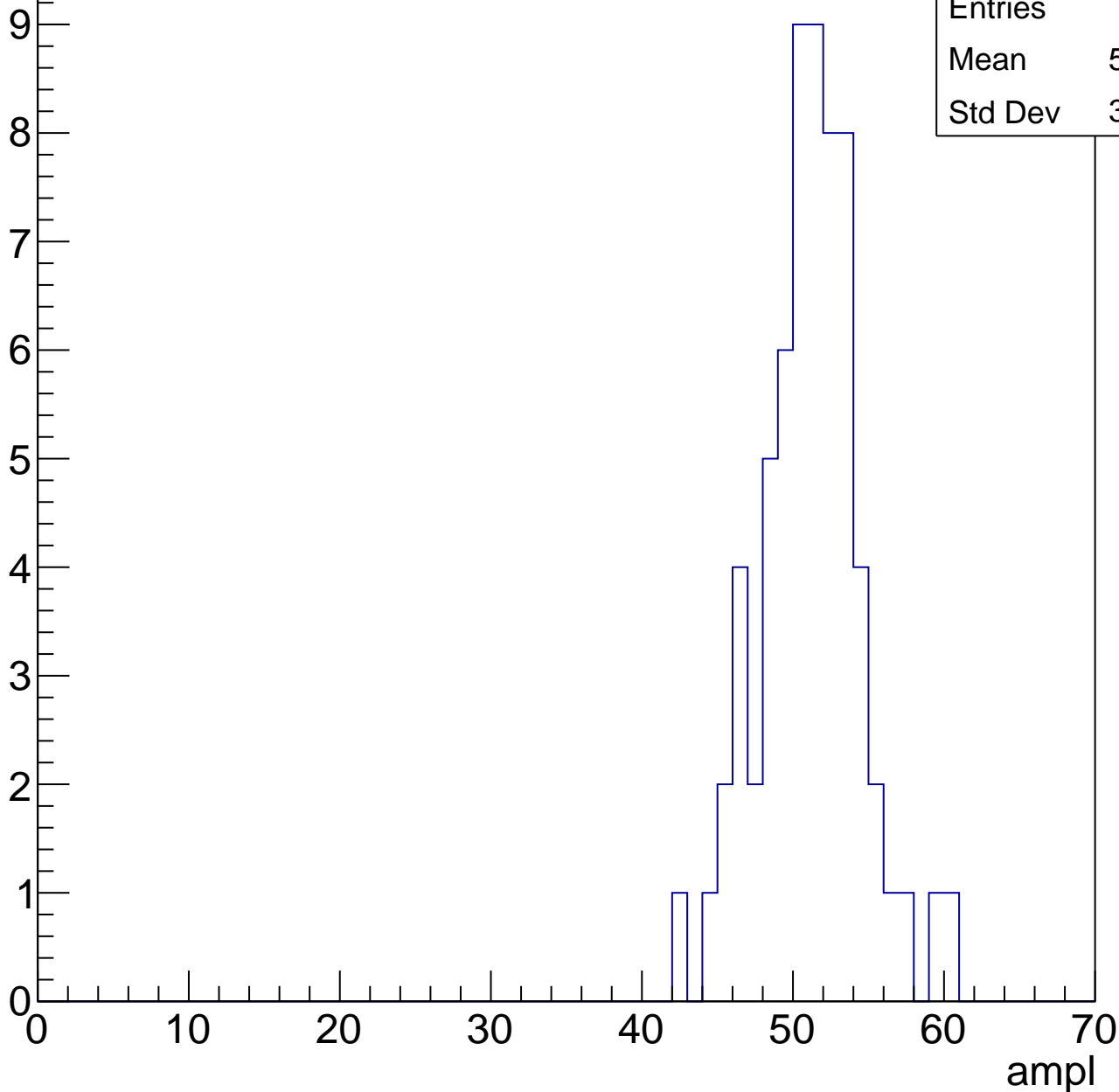


# B0L001S, U24-ch6, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	50.69
Std Dev	3.328

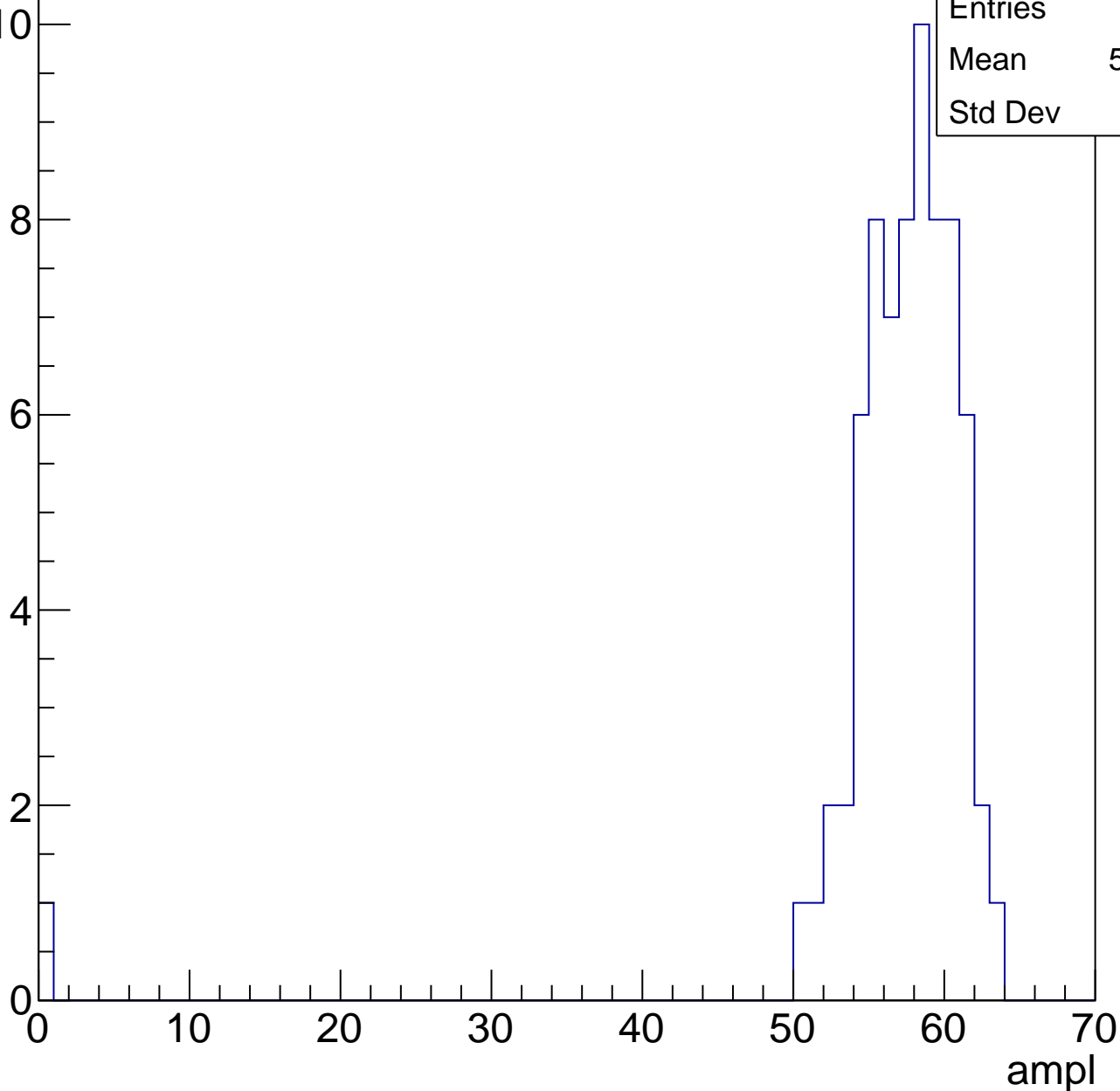


# B0L001S, U24-ch6, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	56.45
Std Dev	7.3

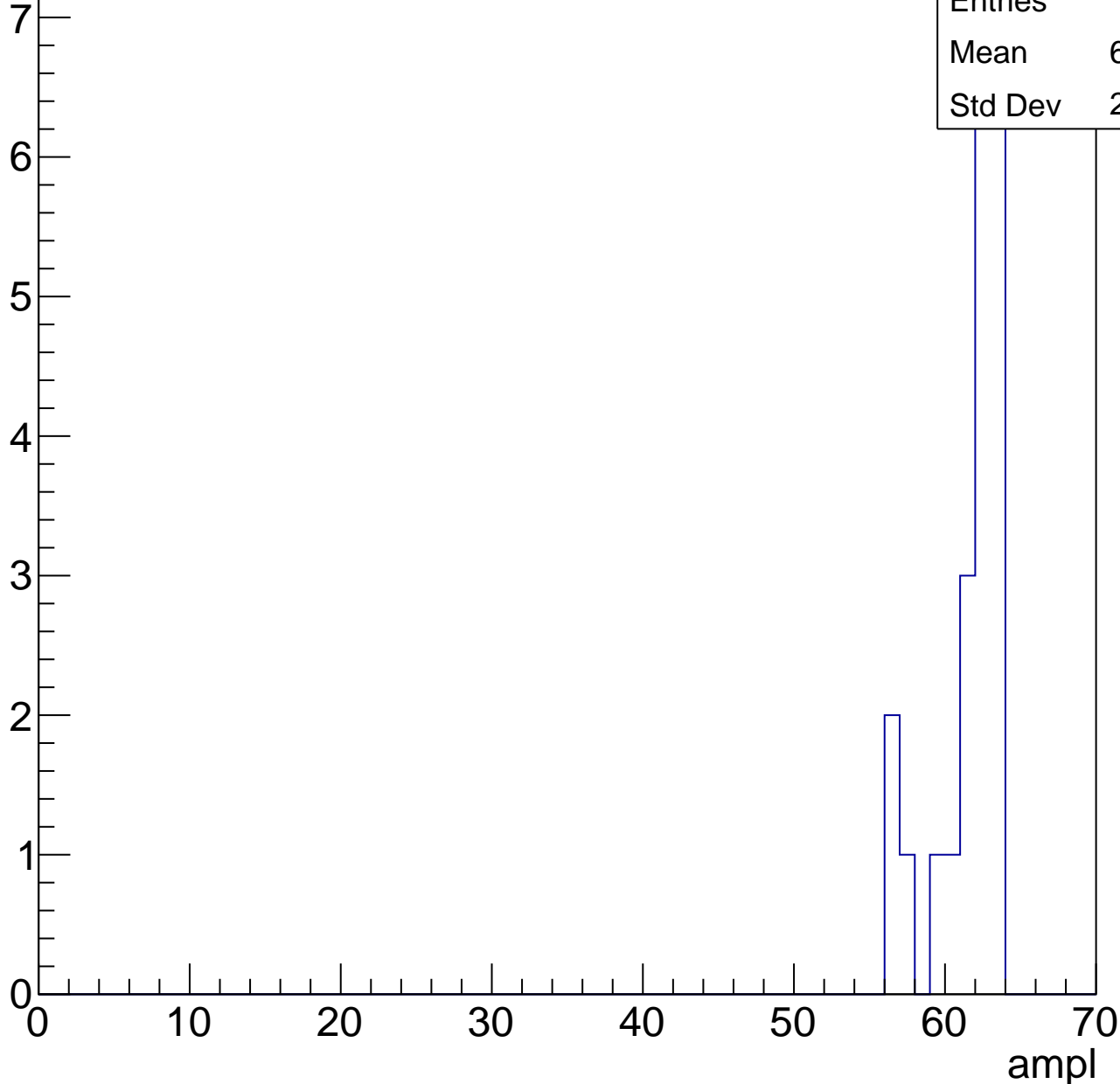


# B0L001S, U24-ch6, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

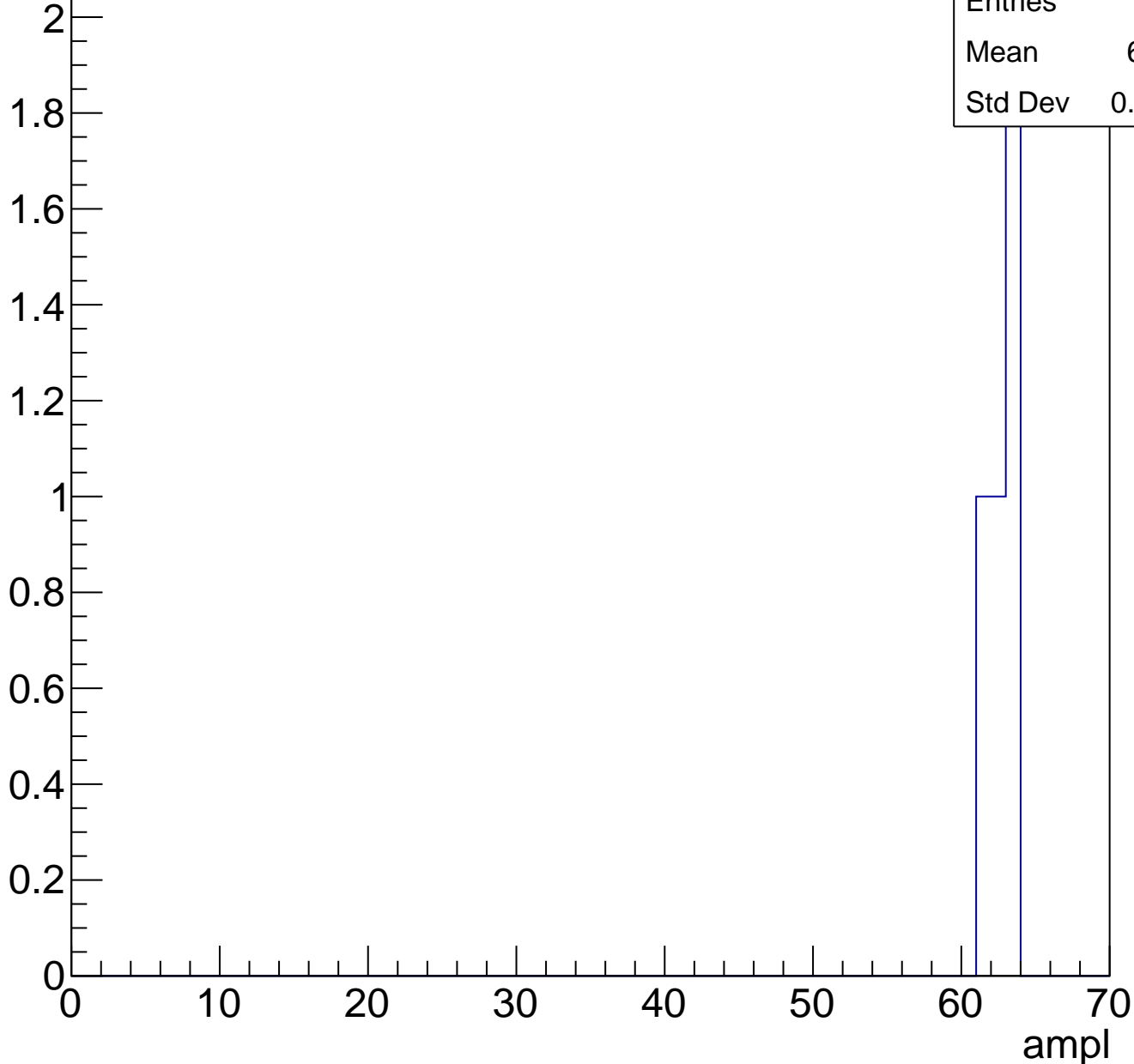
Entries	22
Mean	61.18
Std Dev	2.187



# B0L001S, U24-ch6, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch6, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U24-ch7, adc0

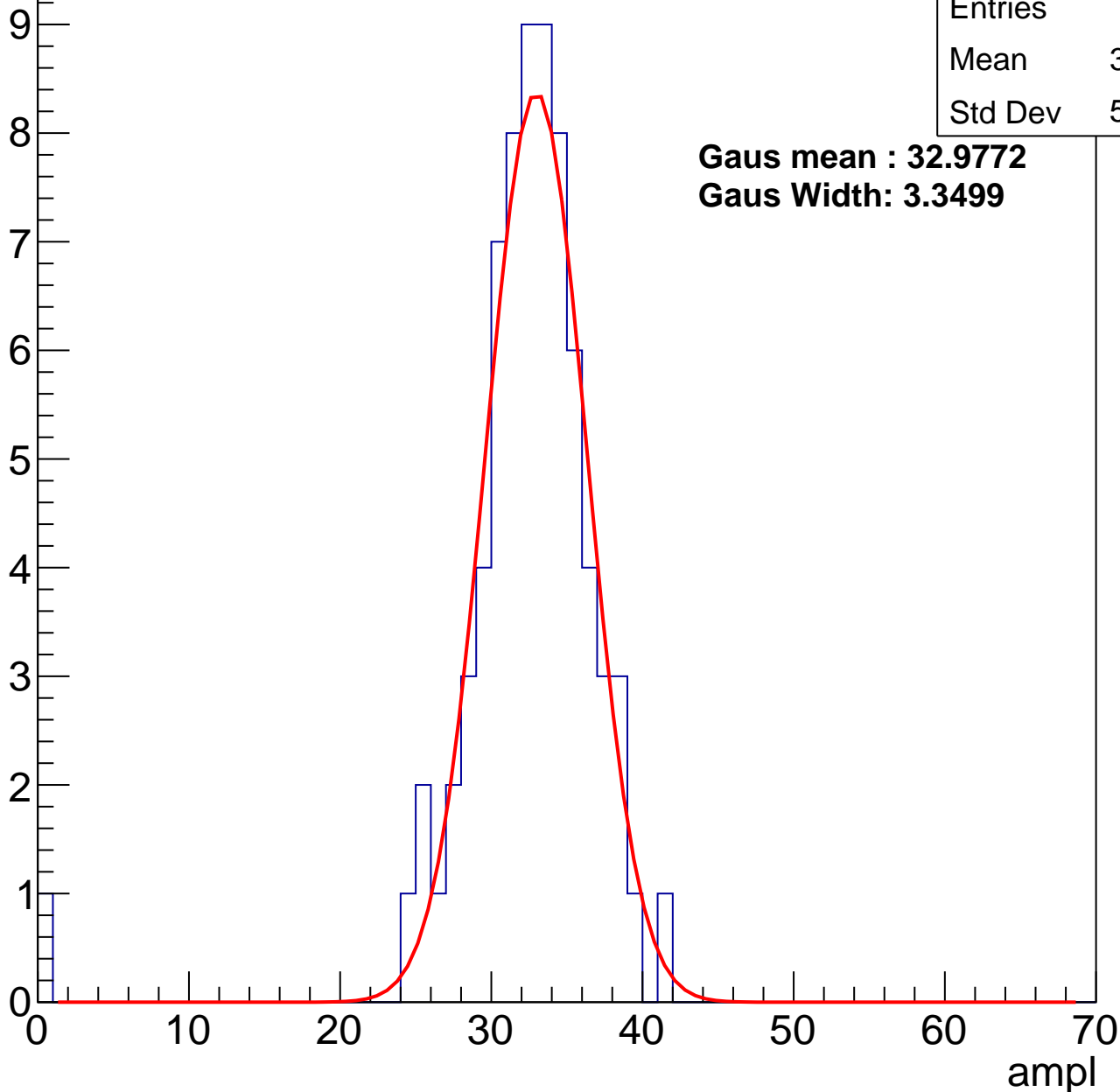
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	31.89
Std Dev	5.052

**Gaus mean : 32.9772**

**Gaus Width: 3.3499**



# B0L001S, U24-ch7, adc1

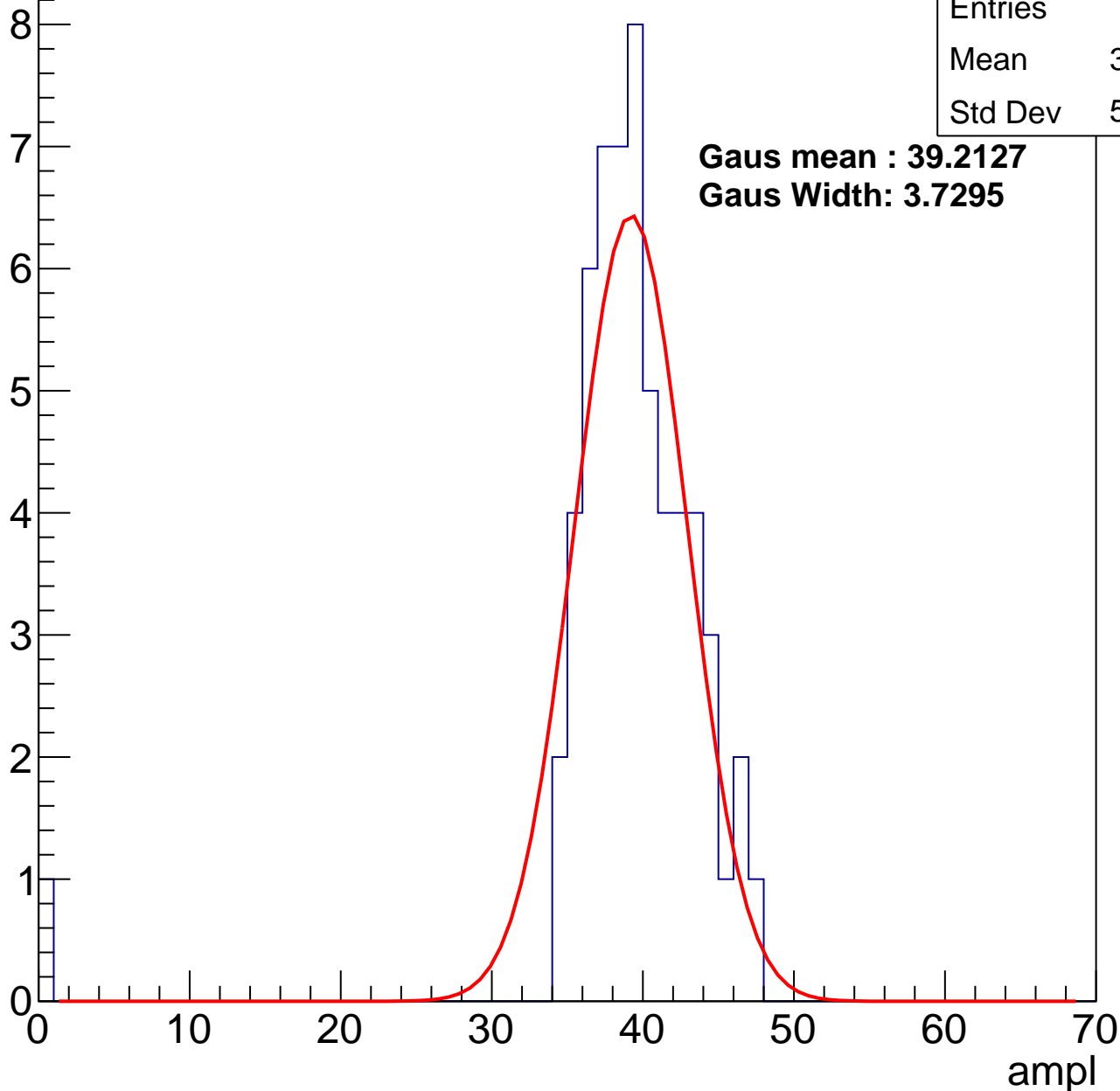
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	38.66
Std Dev	5.982

**Gaus mean : 39.2127**

**Gaus Width: 3.7295**



# B0L001S, U24-ch7, adc2

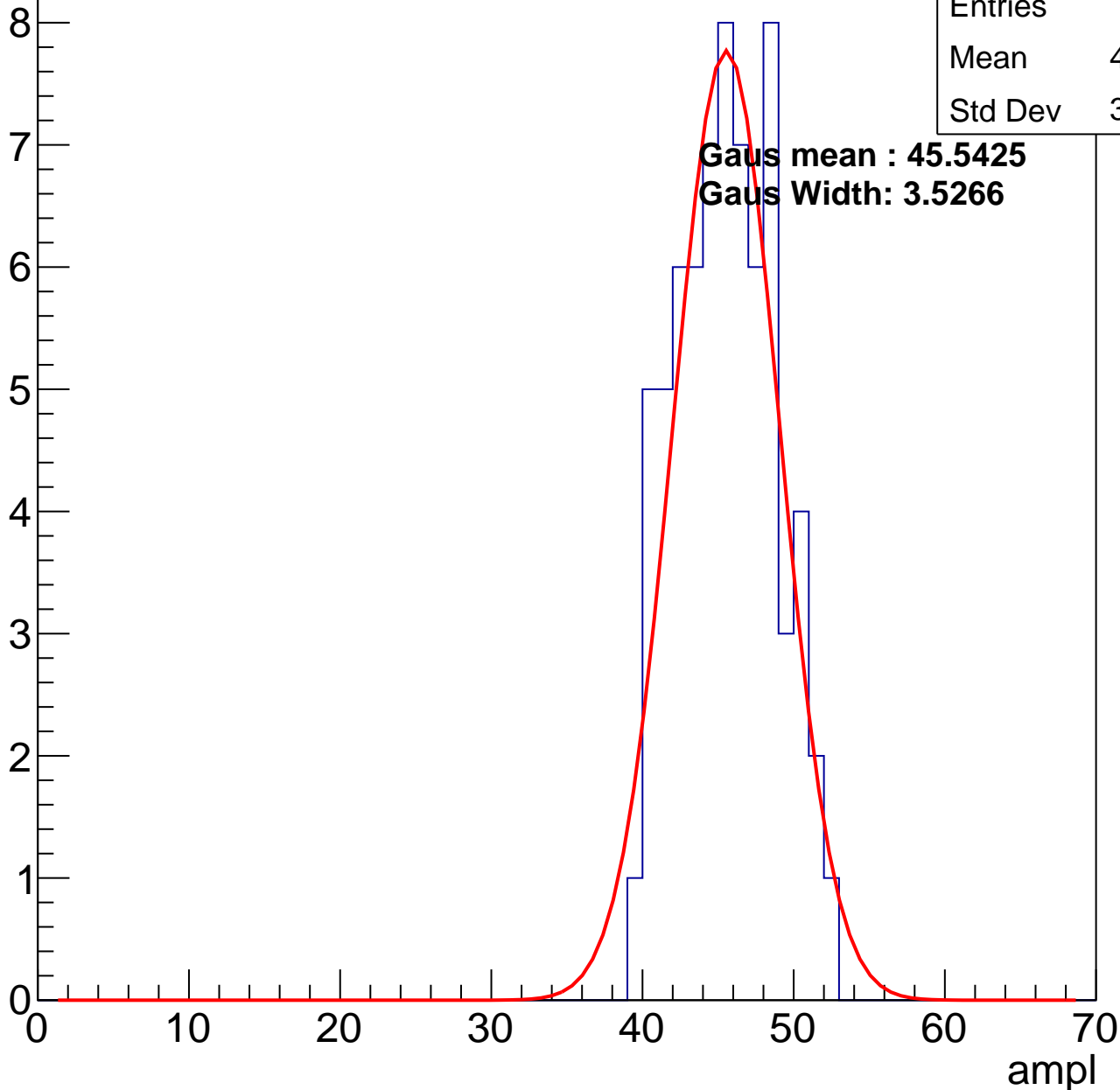
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	45.09
Std Dev	3.179

**Gaus mean : 45.5425**

**Gaus Width: 3.5266**

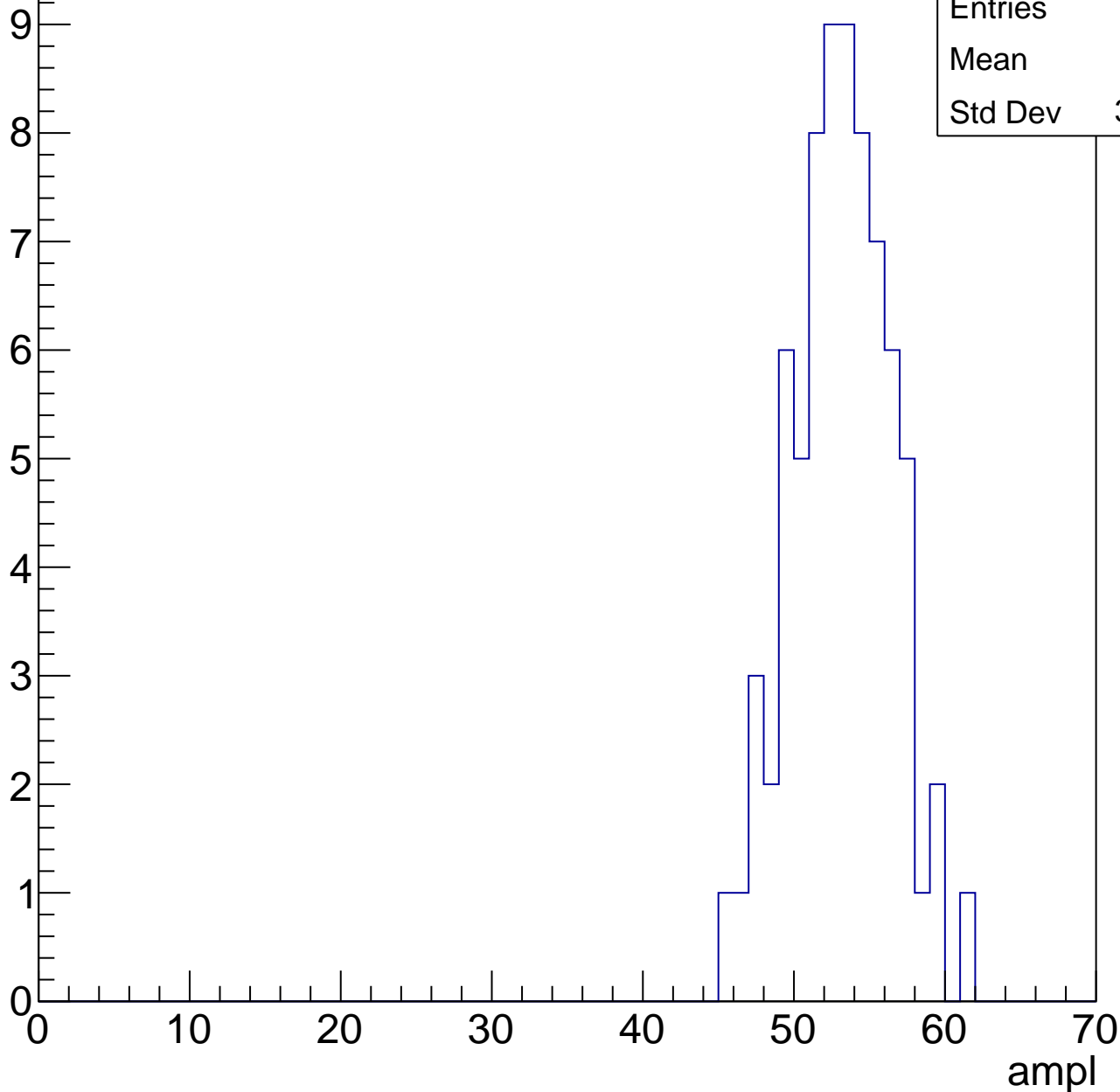


# B0L001S, U24-ch7, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	52.7
Std Dev	3.241

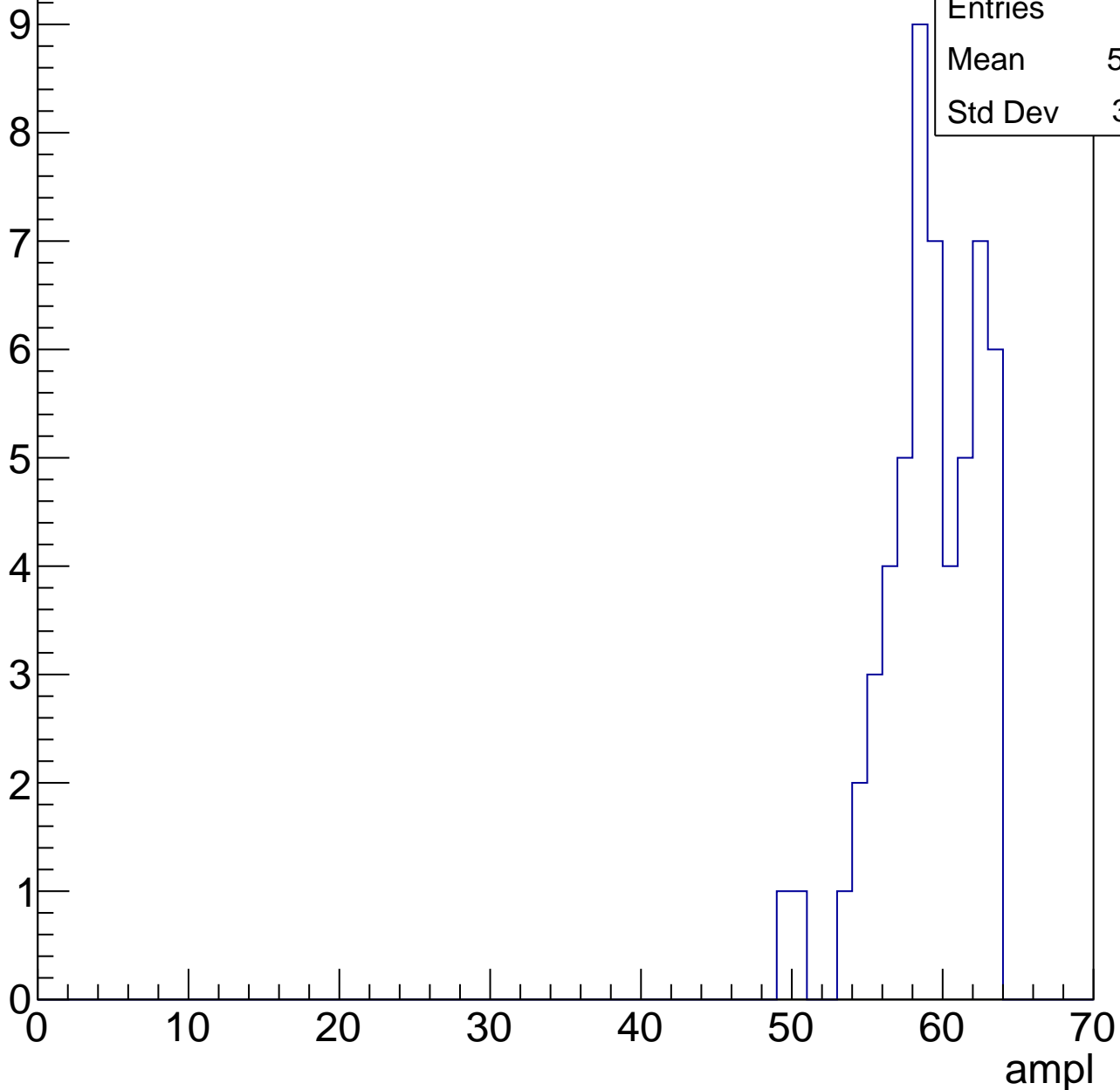


# B0L001S, U24-ch7, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	58.65
Std Dev	3.181

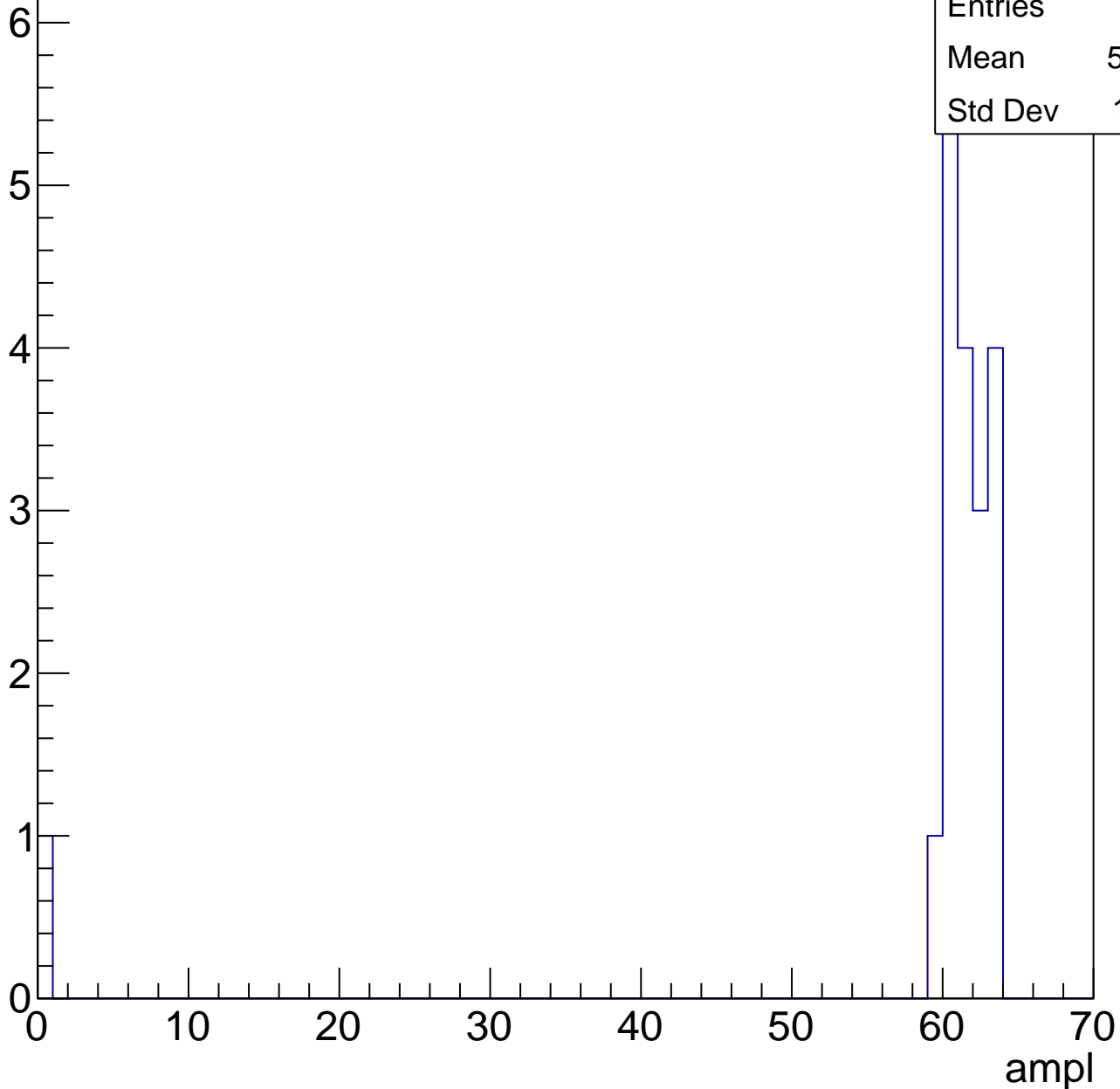


# B0L001S, U24-ch7, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	19
Mean	57.95
Std Dev	13.71



# B0L001S, U24-ch7, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U24-ch7, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U24-ch8, adc0

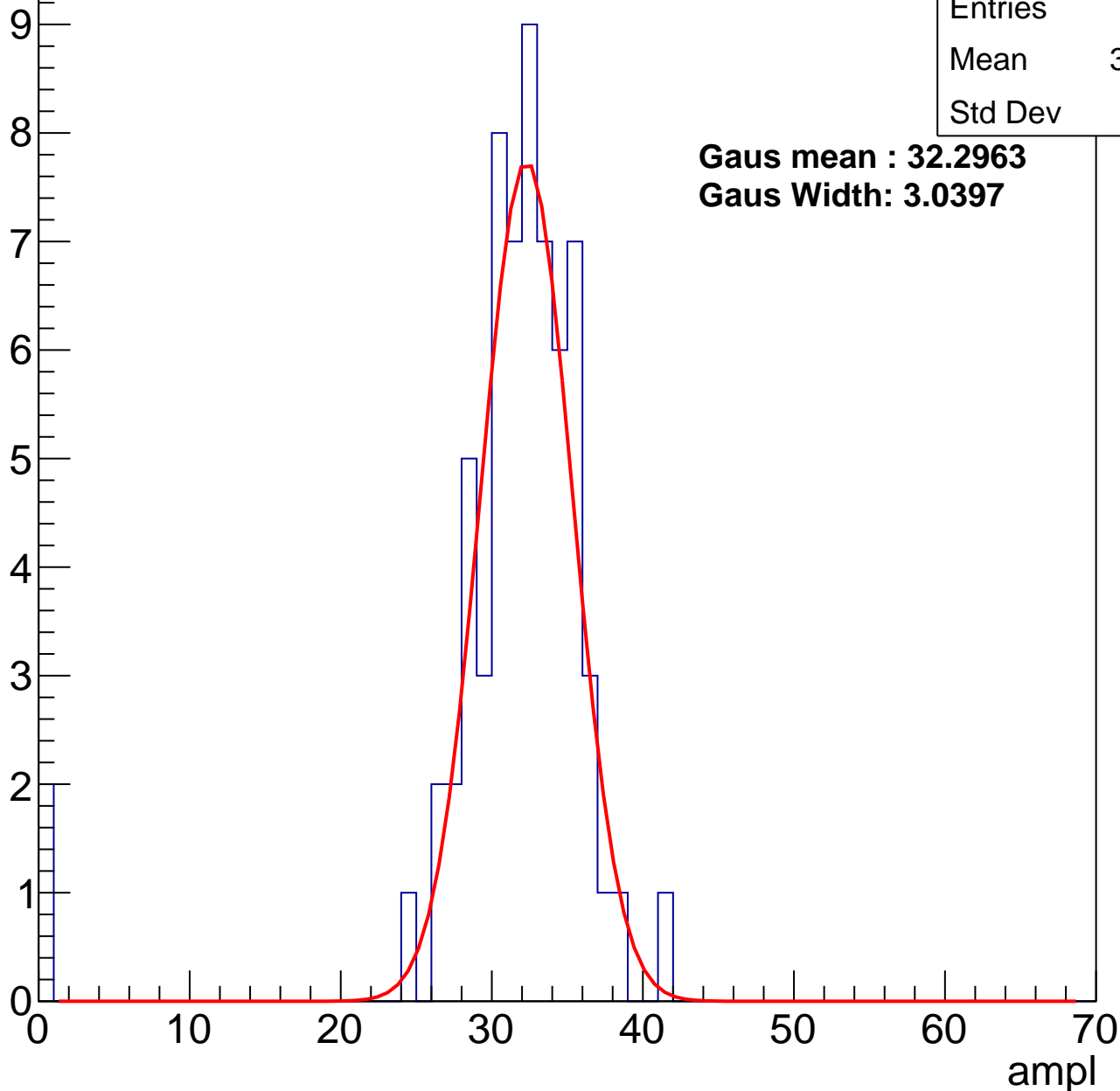
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	30.86
Std Dev	6.3

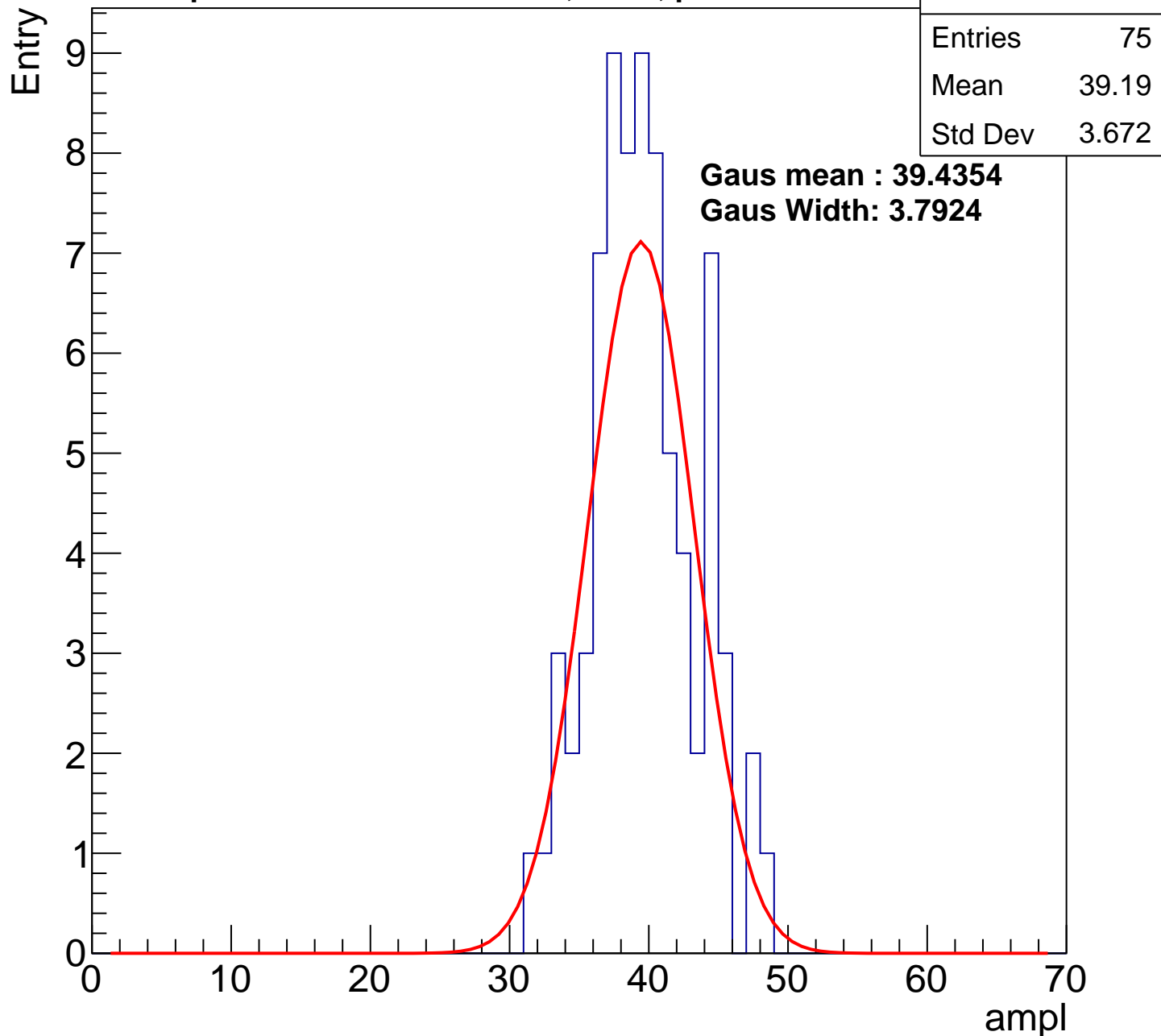
**Gaus mean : 32.2963**

**Gaus Width: 3.0397**



# B0L001S, U24-ch8, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U24-ch8, adc2

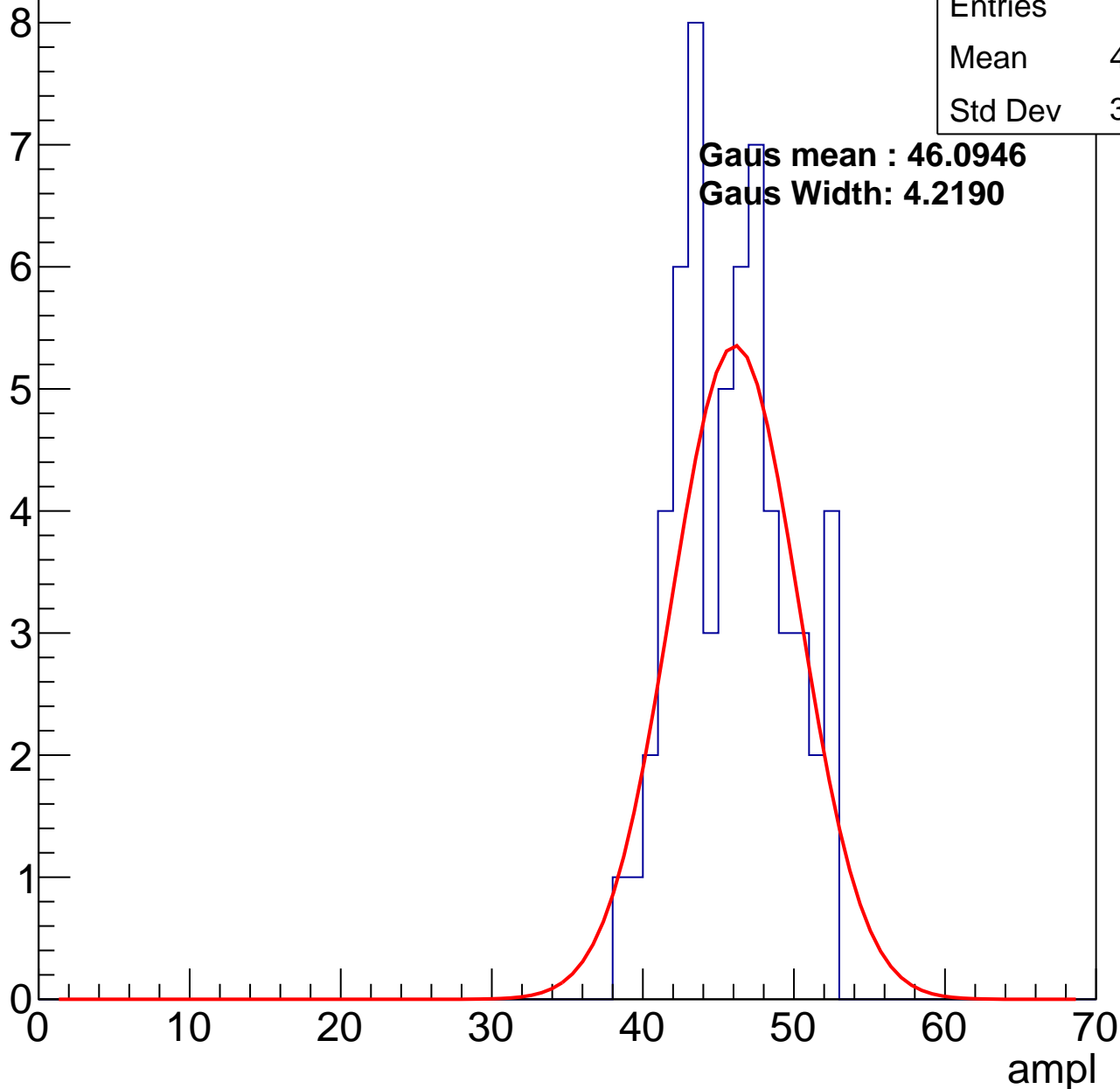
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	45.39
Std Dev	3.542

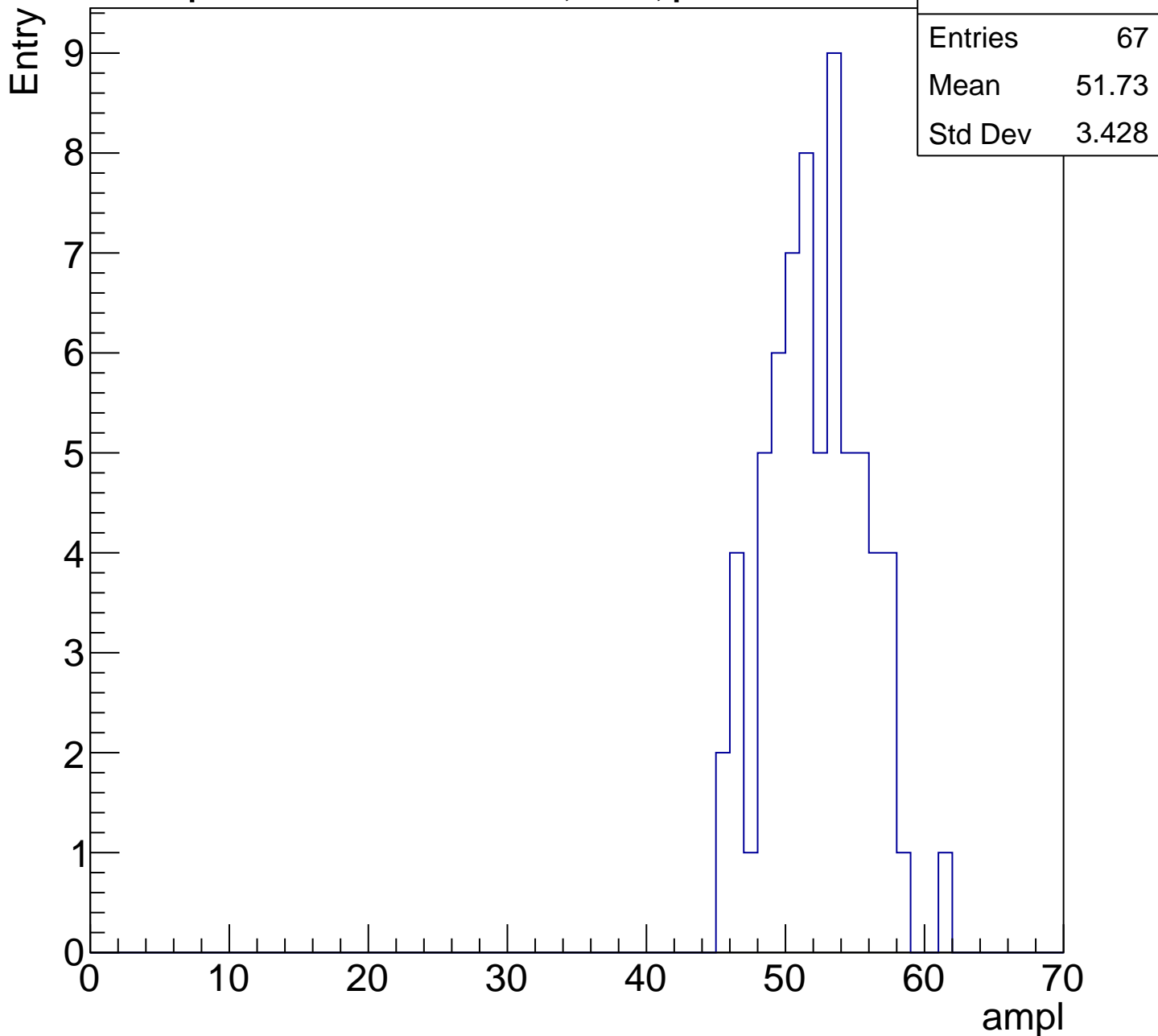
**Gaus mean : 46.0946**

**Gaus Width: 4.2190**



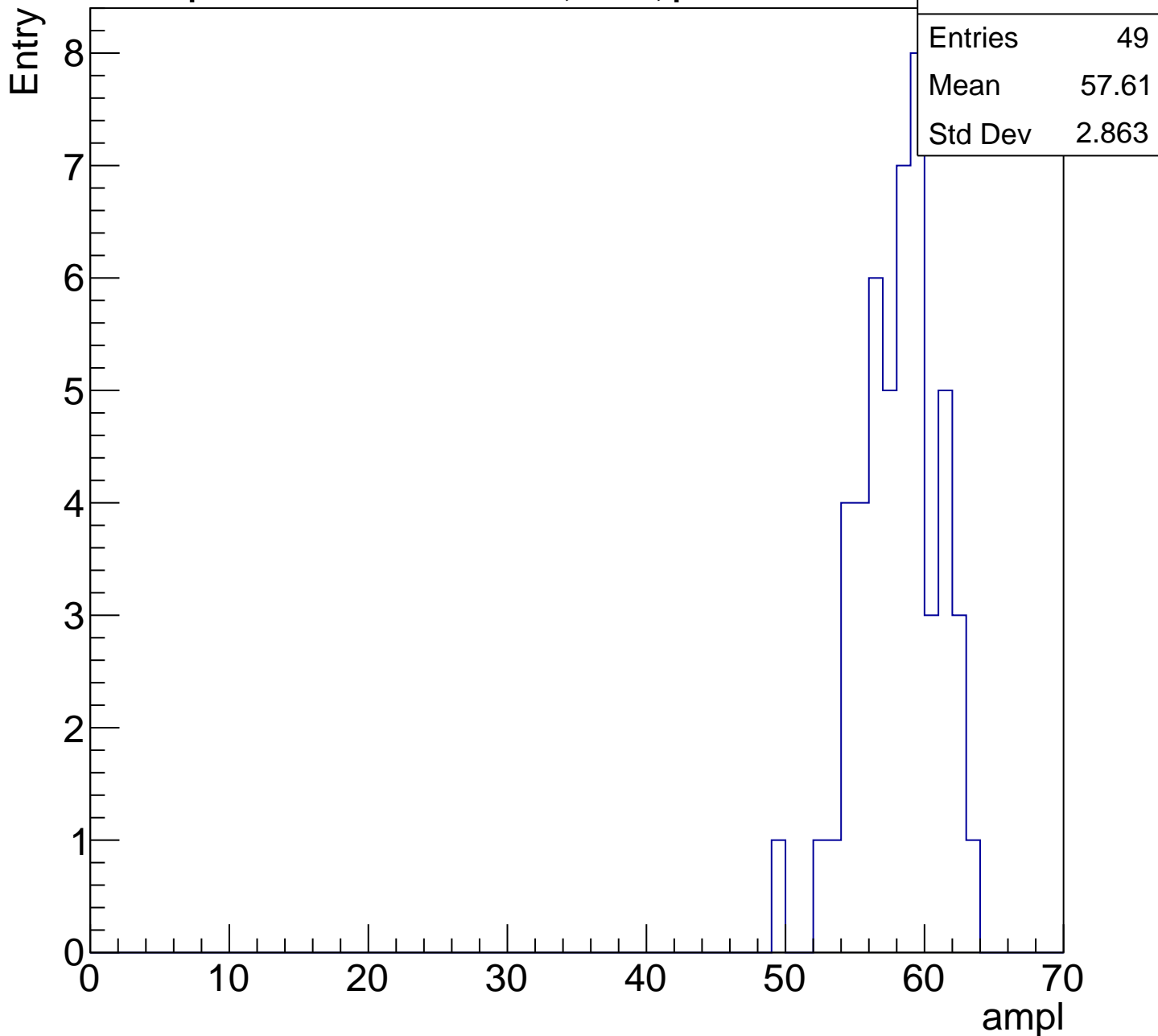
# B0L001S, U24-ch8, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U24-ch8, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U24-ch8, adc5

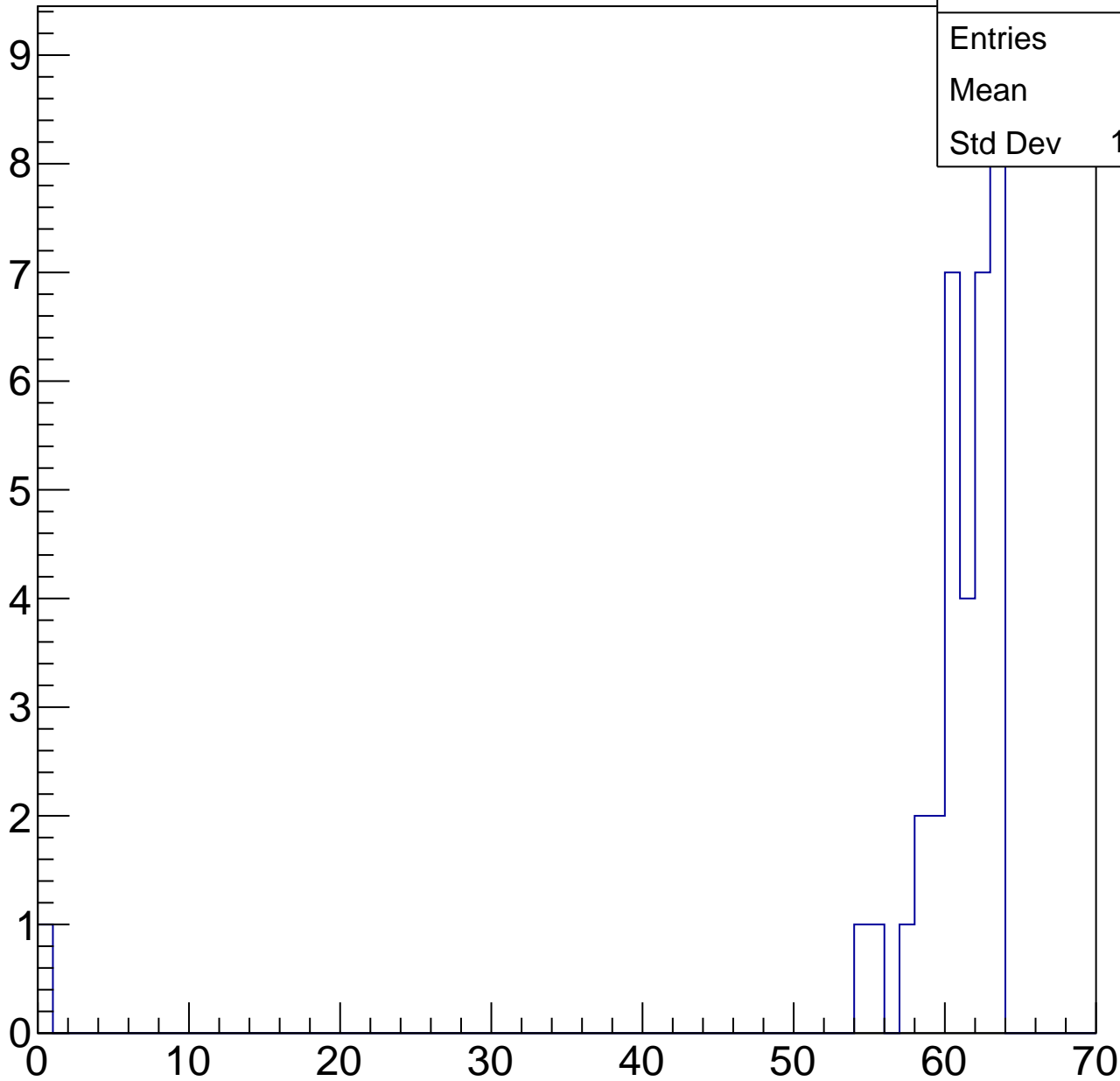
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	35
Mean	59
Std Dev	10.36

ampl



# B0L001S, U24-ch8, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U24-ch8, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U24-ch9, adc0

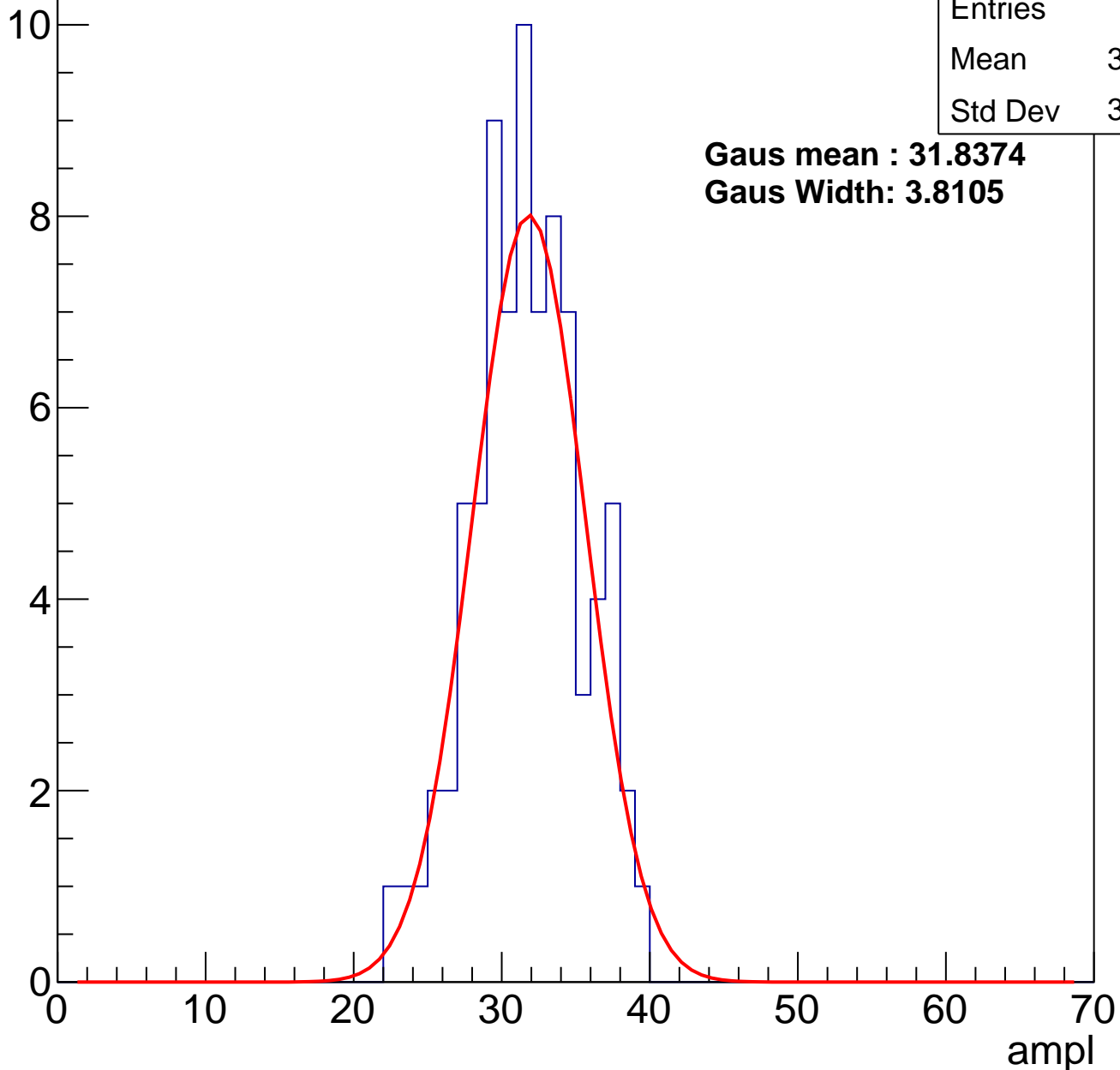
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	80
Mean	31.27
Std Dev	3.657

**Gaus mean : 31.8374**

**Gaus Width: 3.8105**

Entry



# B0L001S, U24-ch9, adc1

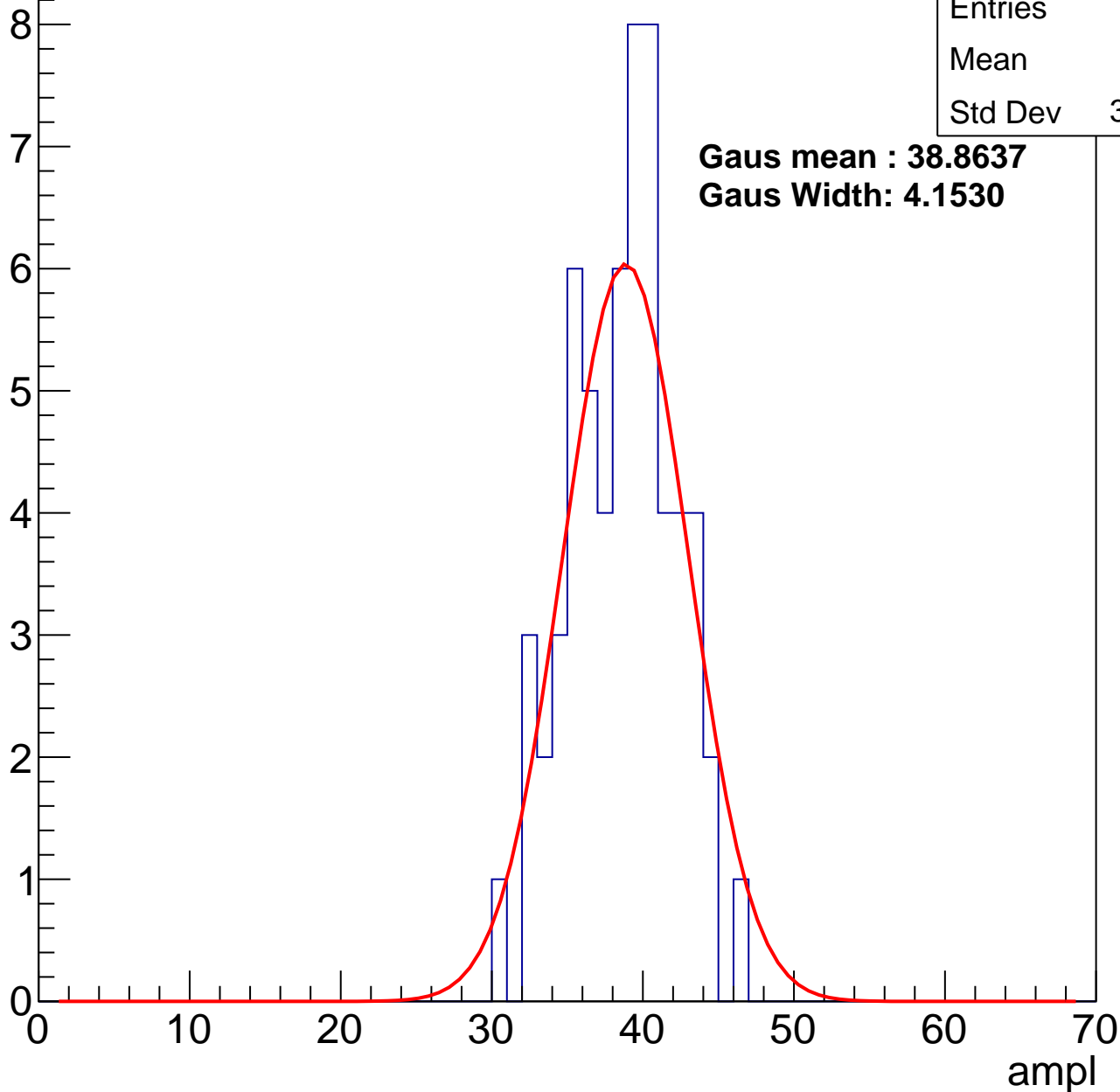
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	38.2
Std Dev	3.439

**Gaus mean : 38.8637**

**Gaus Width: 4.1530**



# B0L001S, U24-ch9, adc2

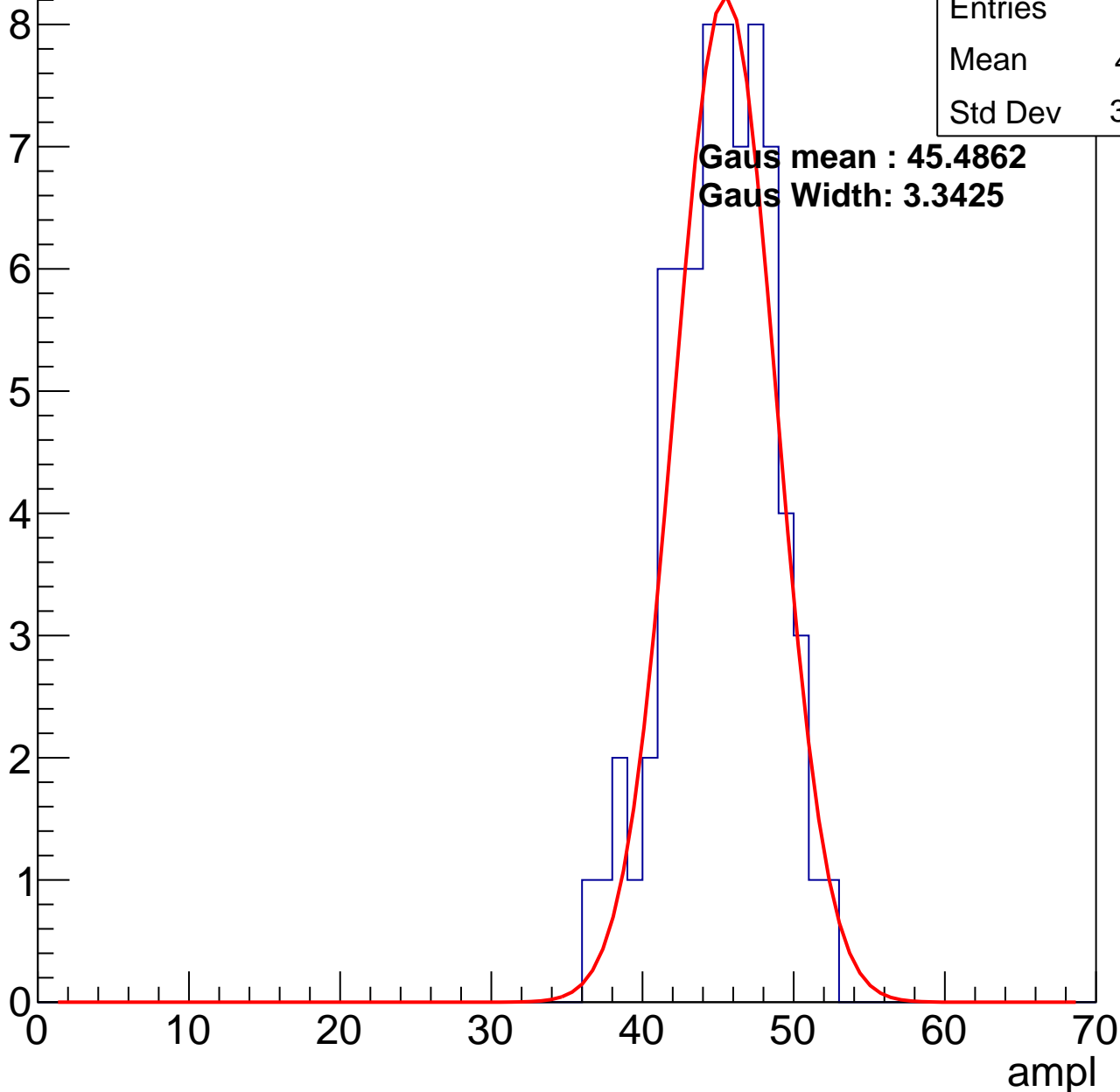
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	44.71
Std Dev	3.397

**Gaus mean : 45.4862**

**Gaus Width: 3.3425**

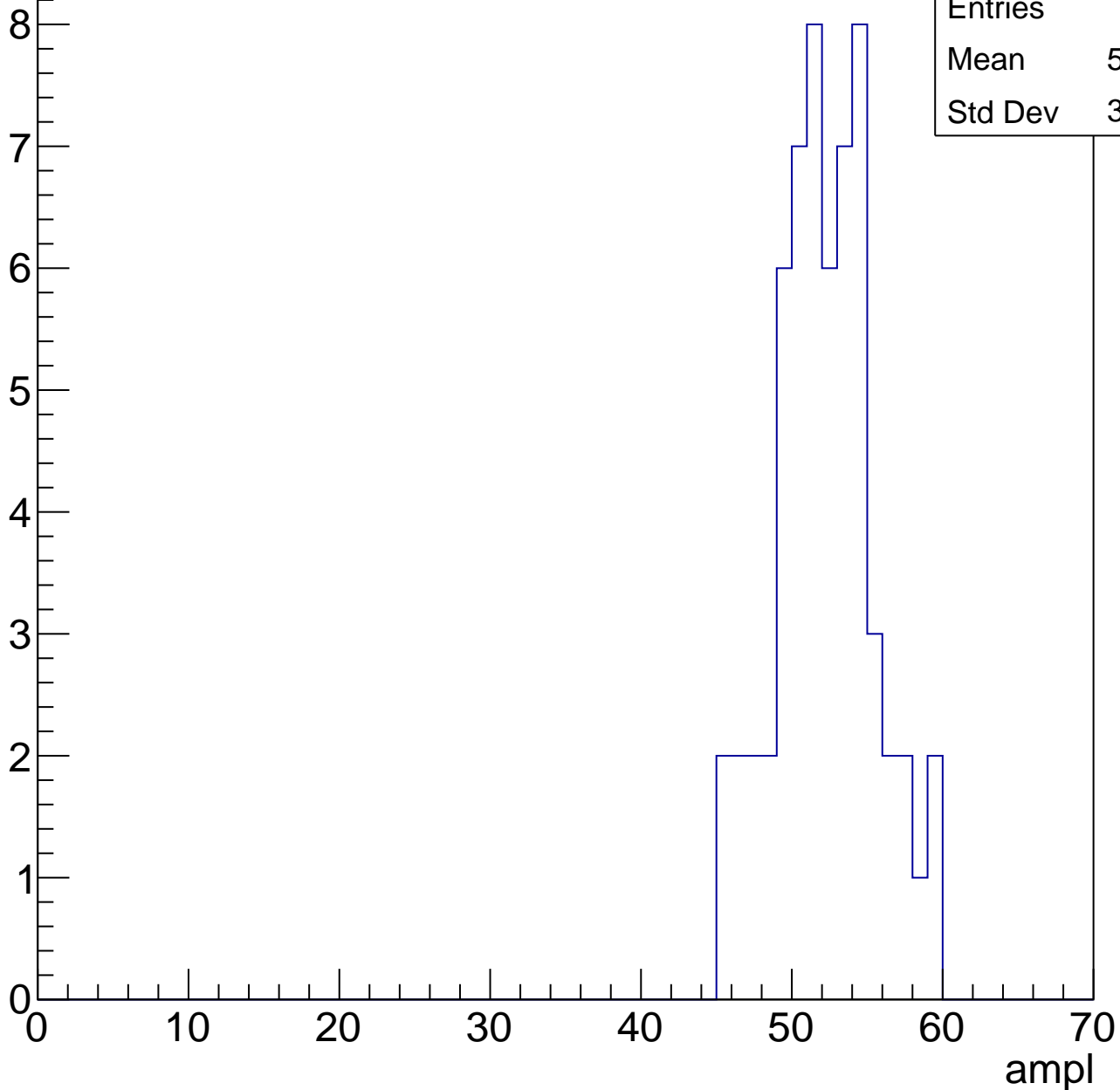


# B0L001S, U24-ch9, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	51.77
Std Dev	3.216

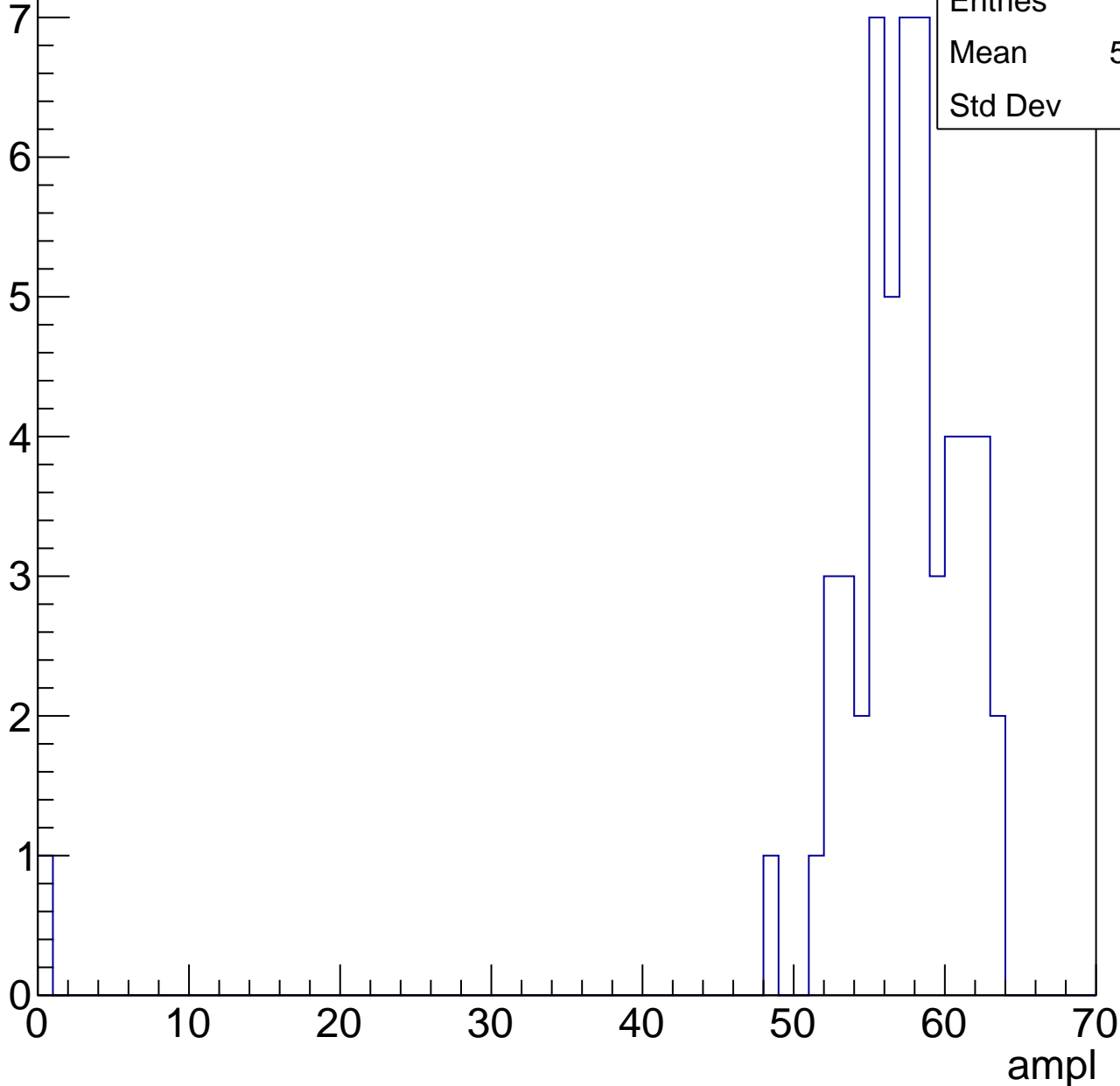


# B0L001S, U24-ch9, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

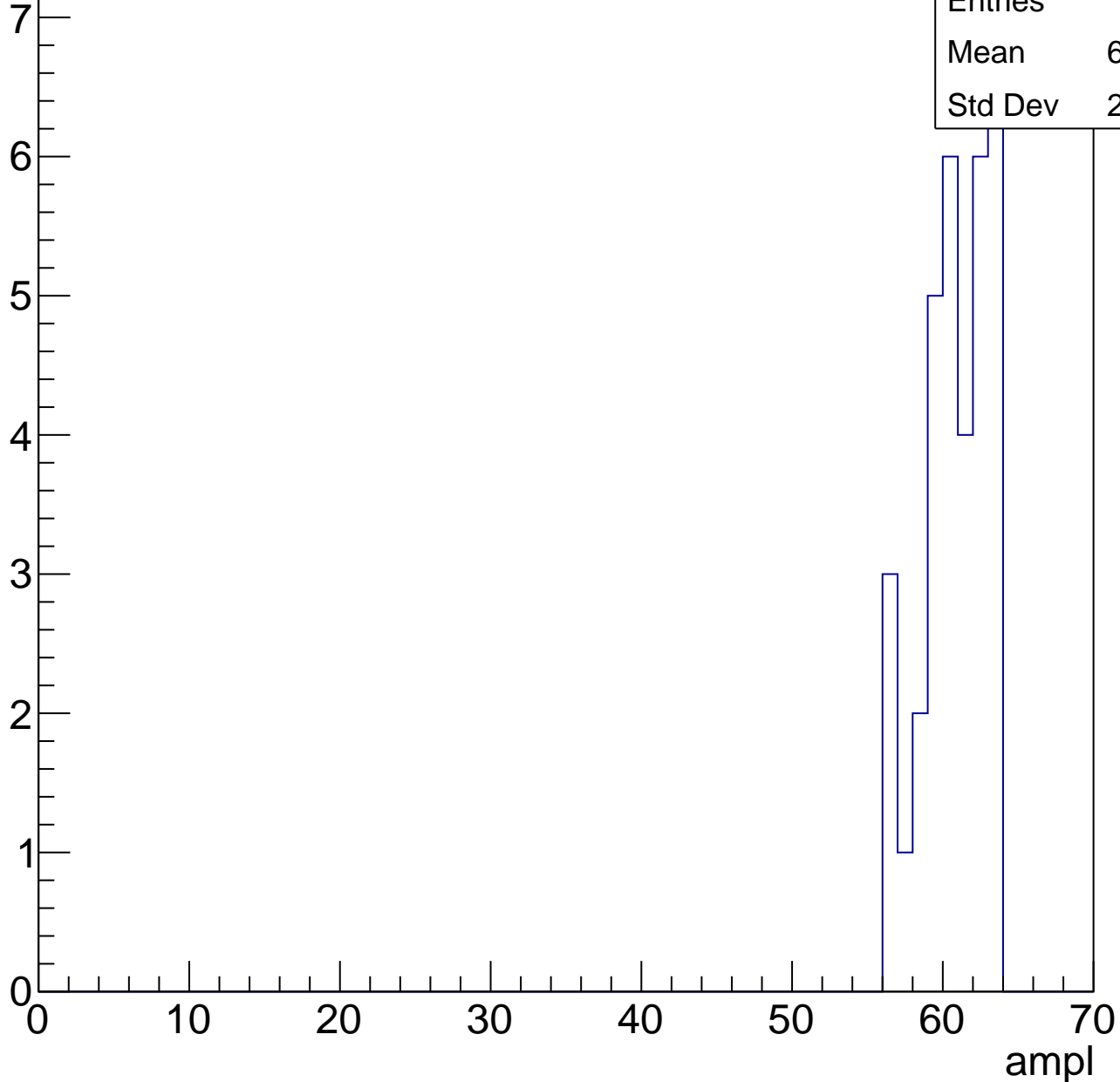
Entries	54
Mean	56.06
Std Dev	8.37



# B0L001S, U24-ch9, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

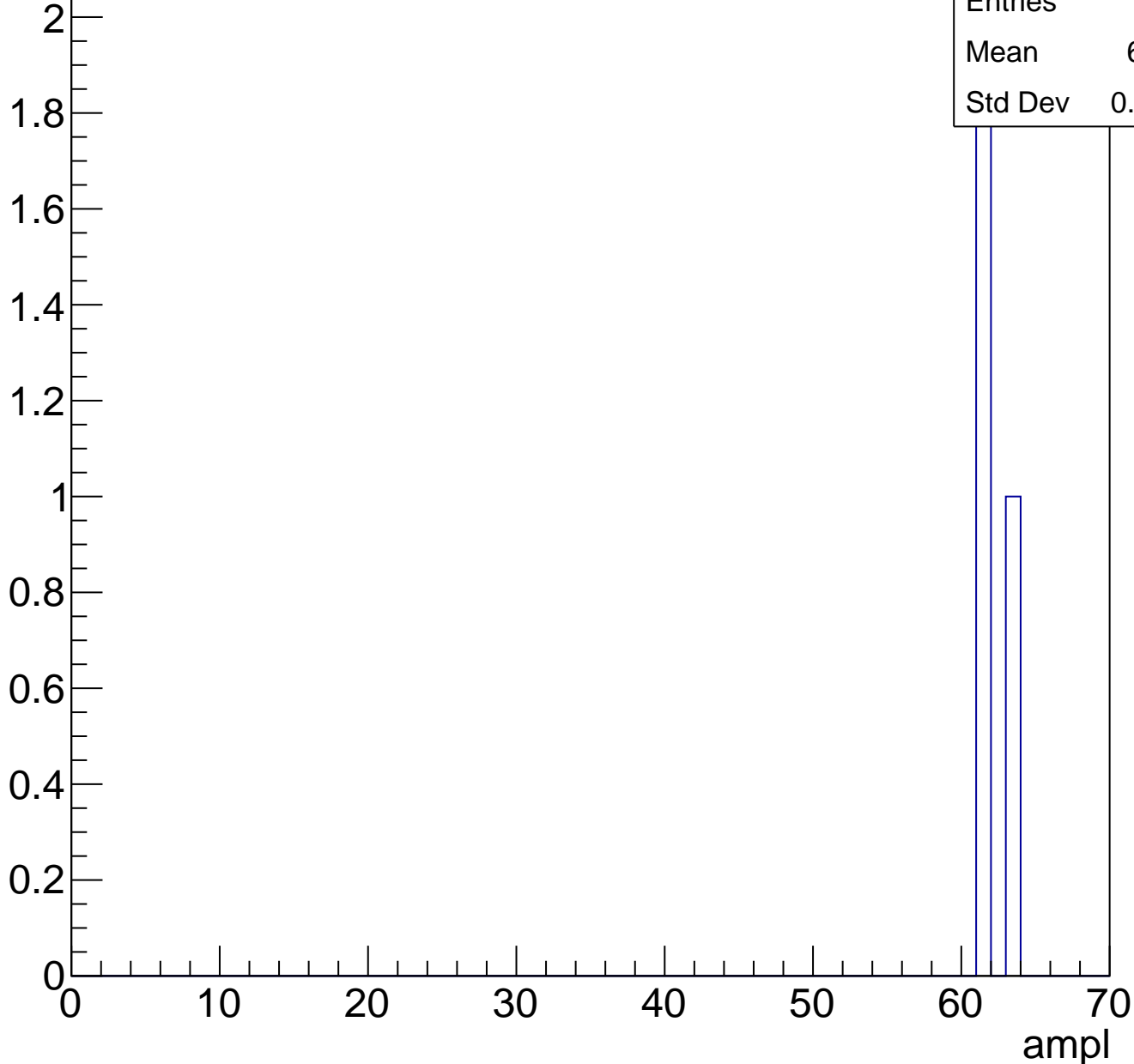
Entry



# B0L001S, U24-ch9, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch9, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U24-ch10, adc0

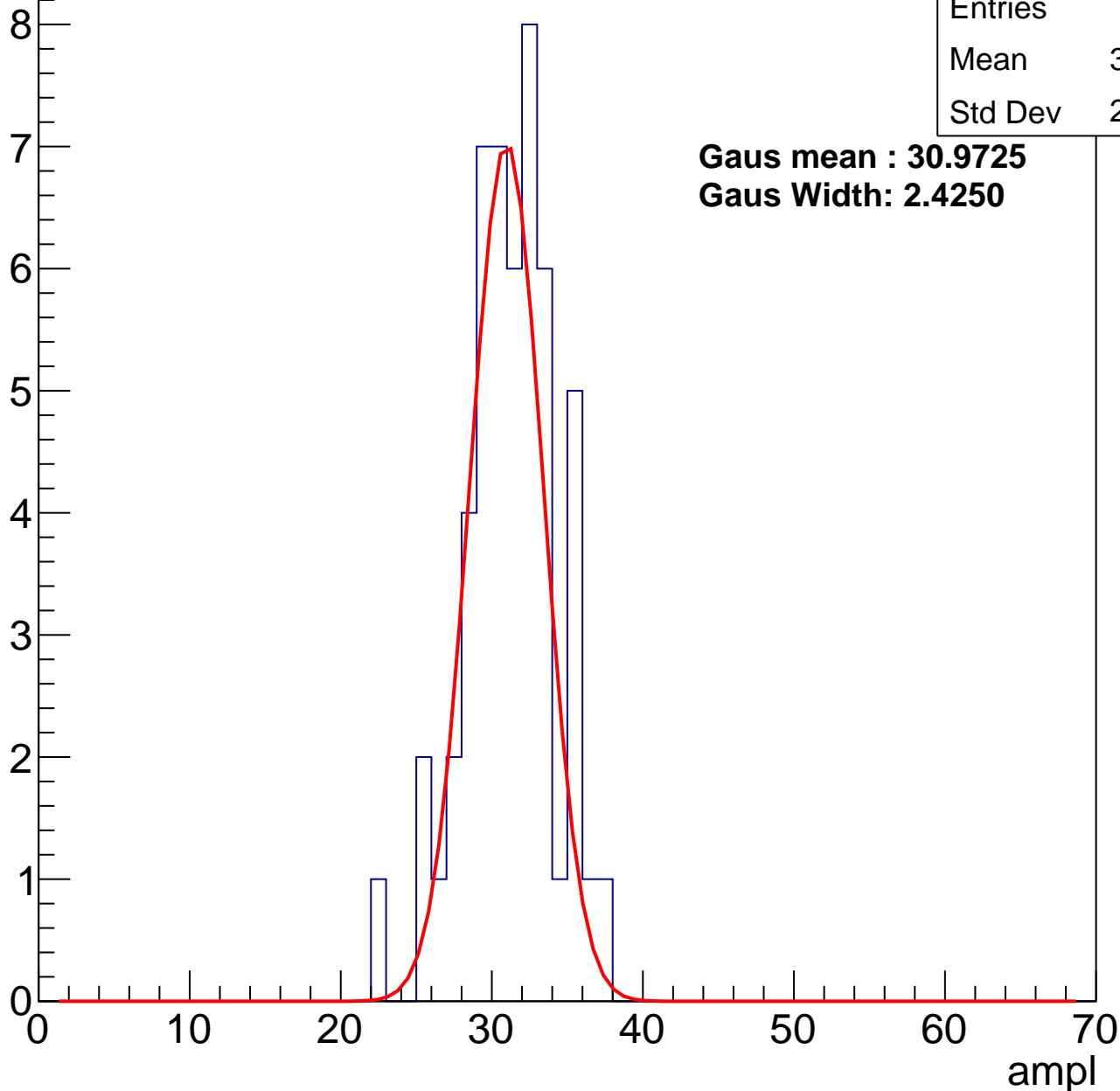
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	30.75
Std Dev	2.973

**Gaus mean : 30.9725**

**Gaus Width: 2.4250**



# B0L001S, U24-ch10, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	74
Mean	37.14
Std Dev	3.277

**Gaus mean : 37.7016**

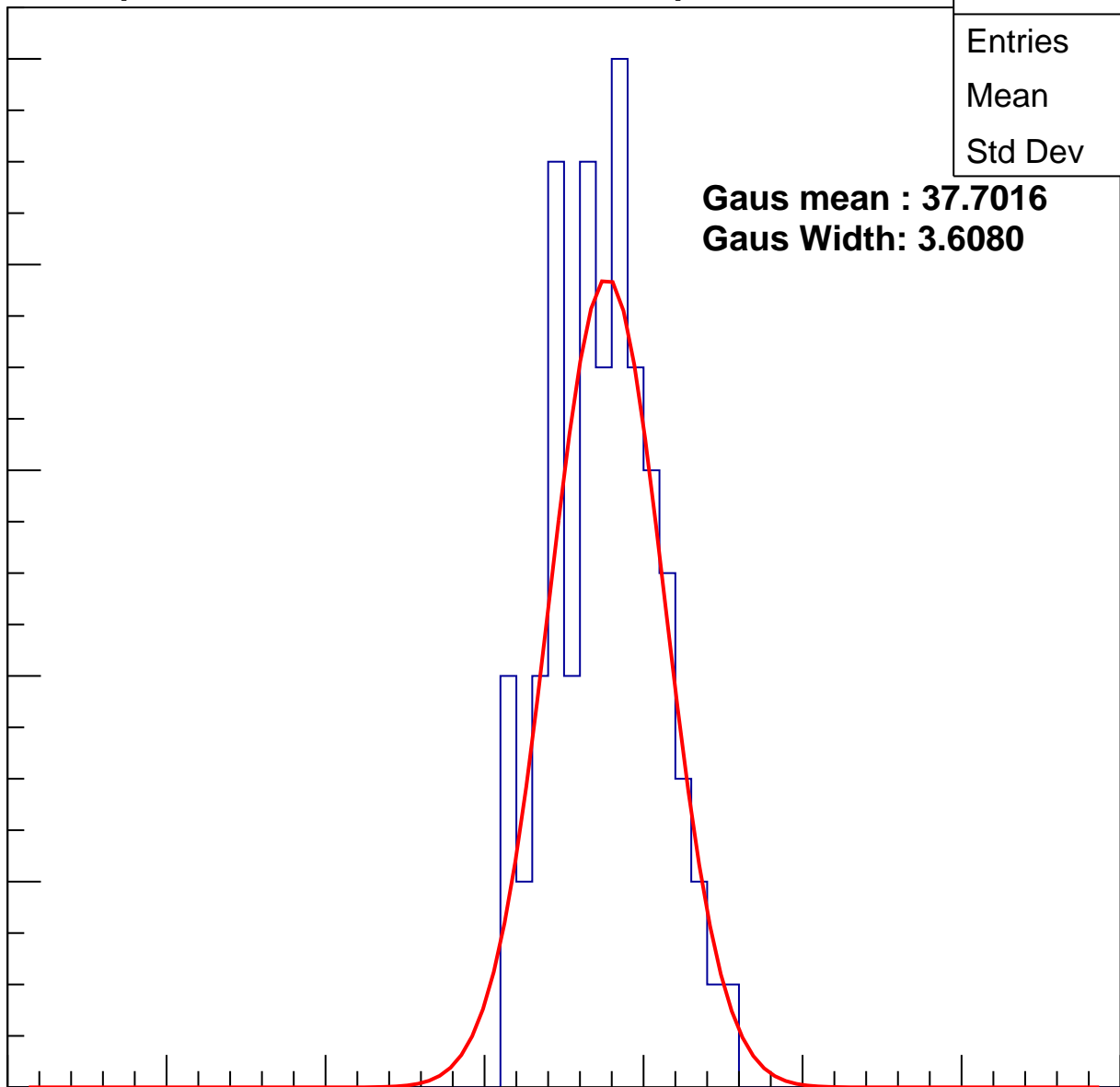
**Gaus Width: 3.6080**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U24-ch10, adc2

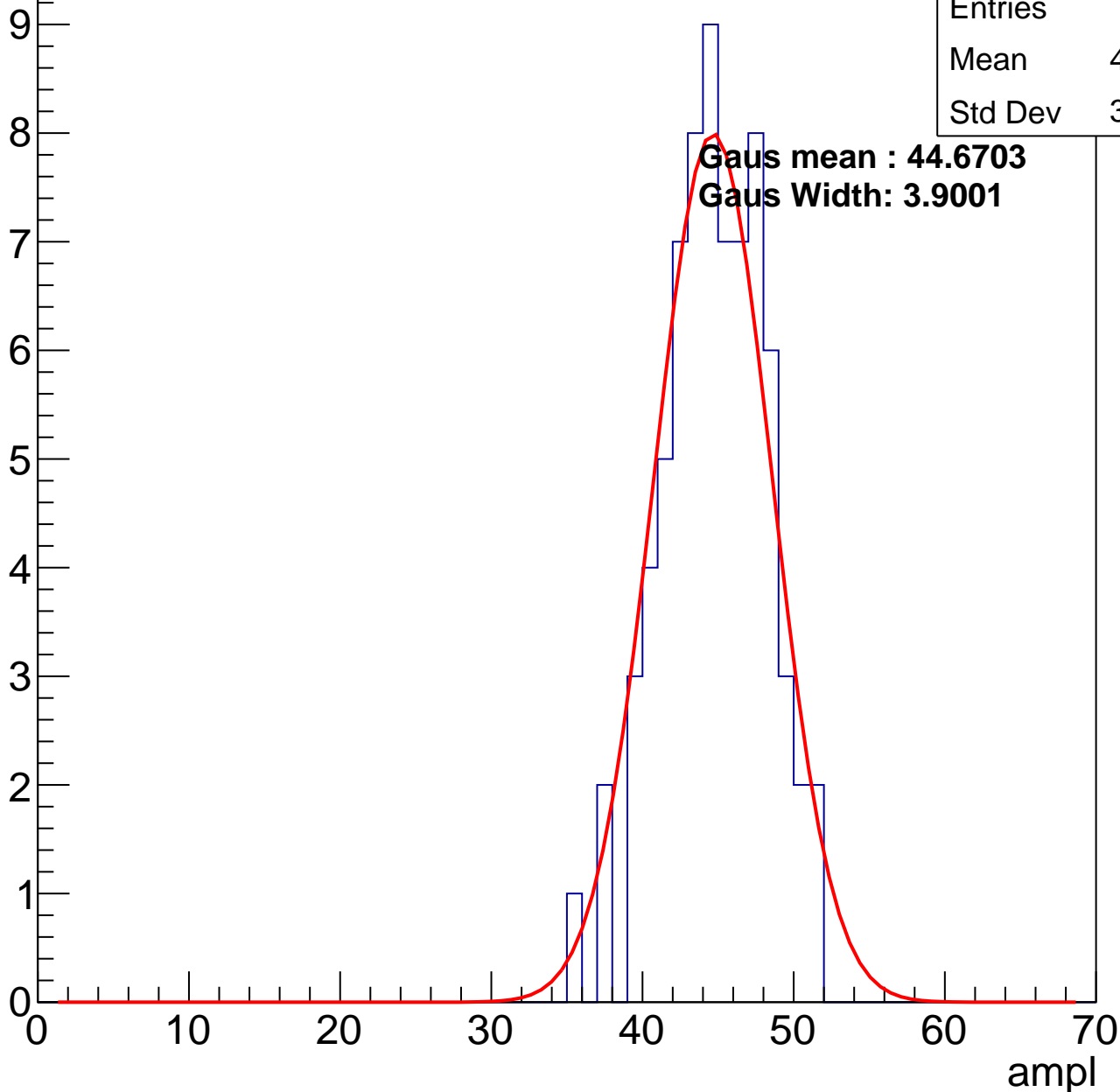
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	44.26
Std Dev	3.373

**Gaus mean : 44.6703**

**Gaus Width: 3.9001**

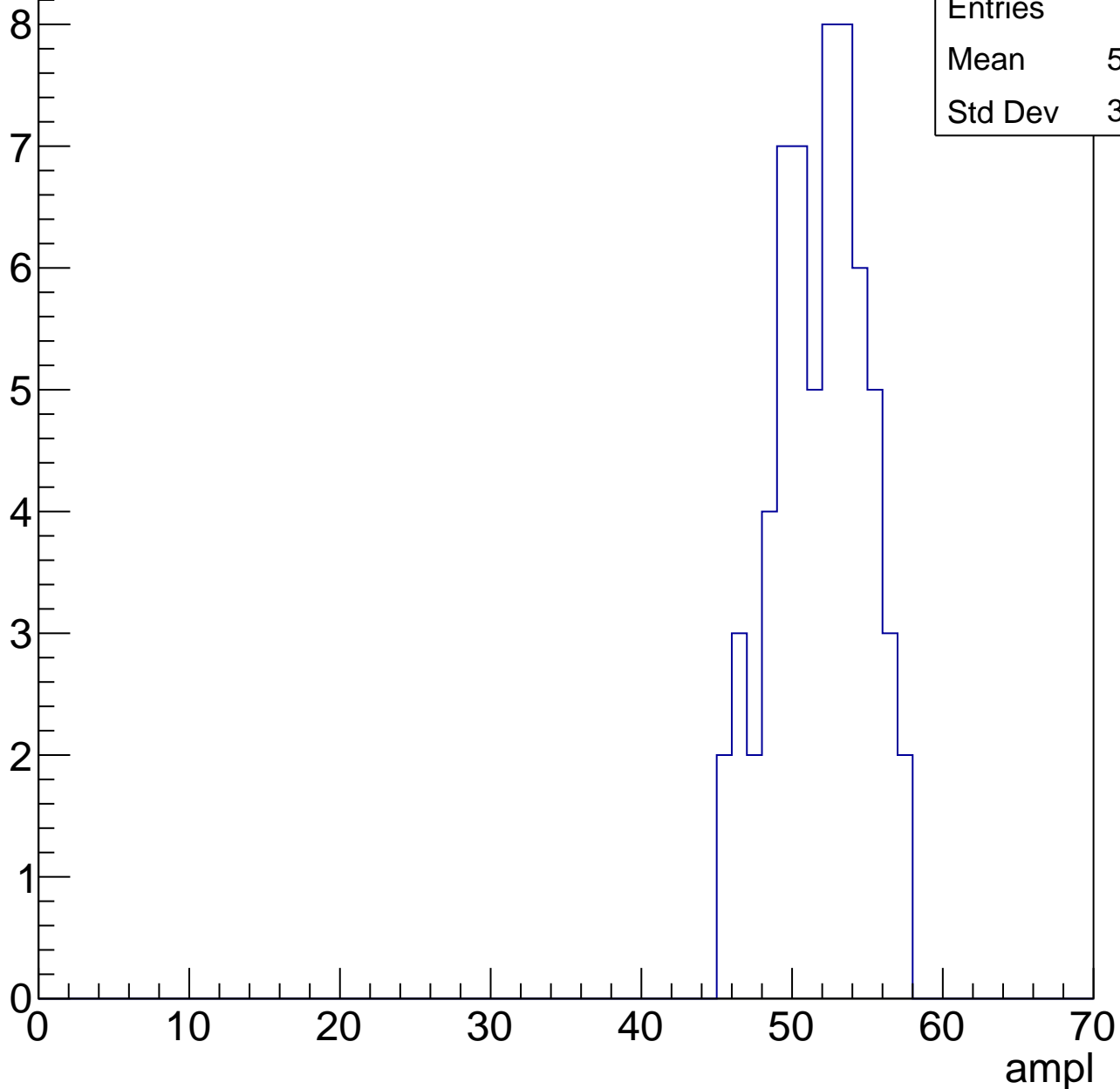


# B0L001S, U24-ch10, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	51.34
Std Dev	3.016

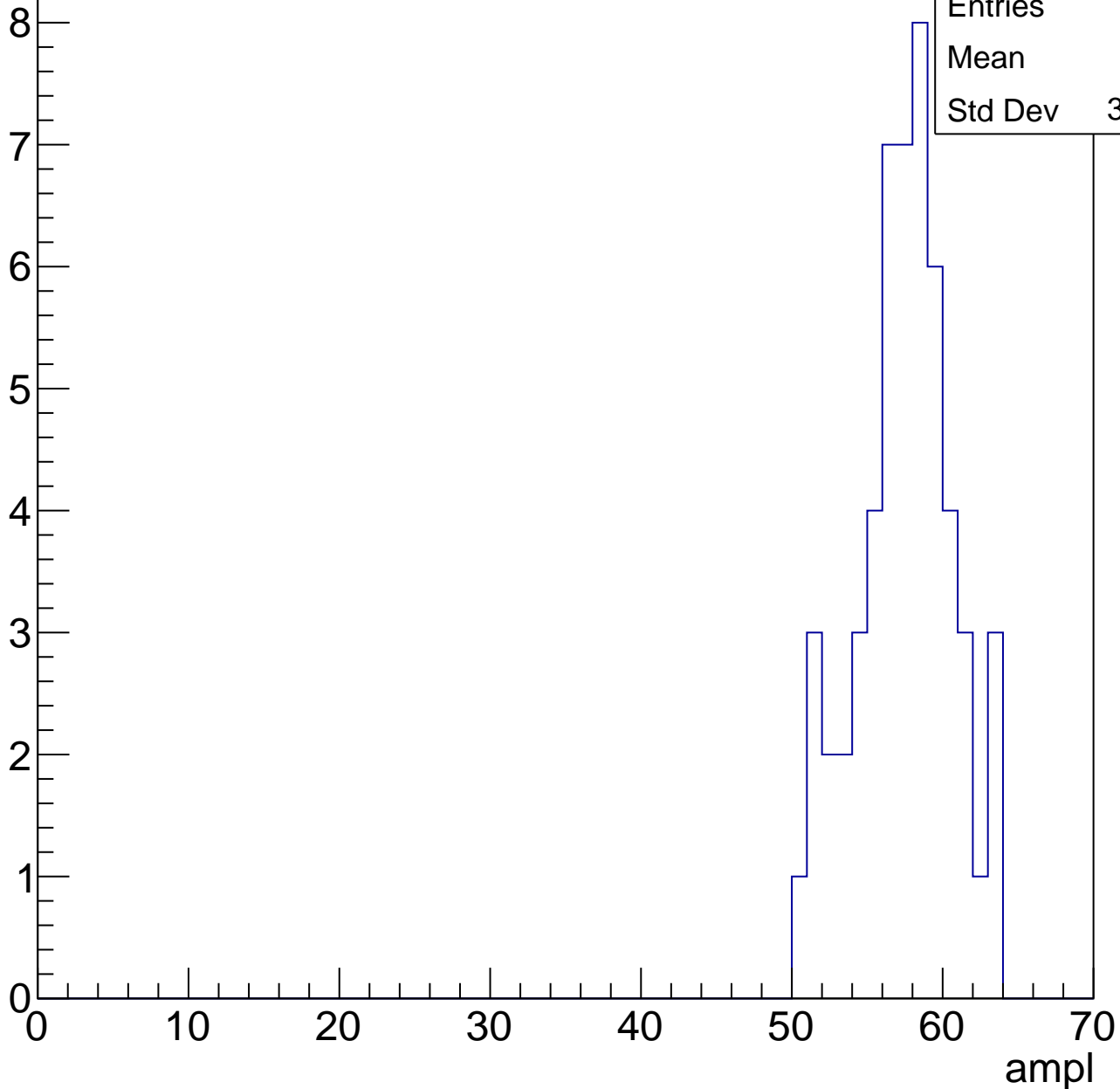


# B0L001S, U24-ch10, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	57
Std Dev	3.156

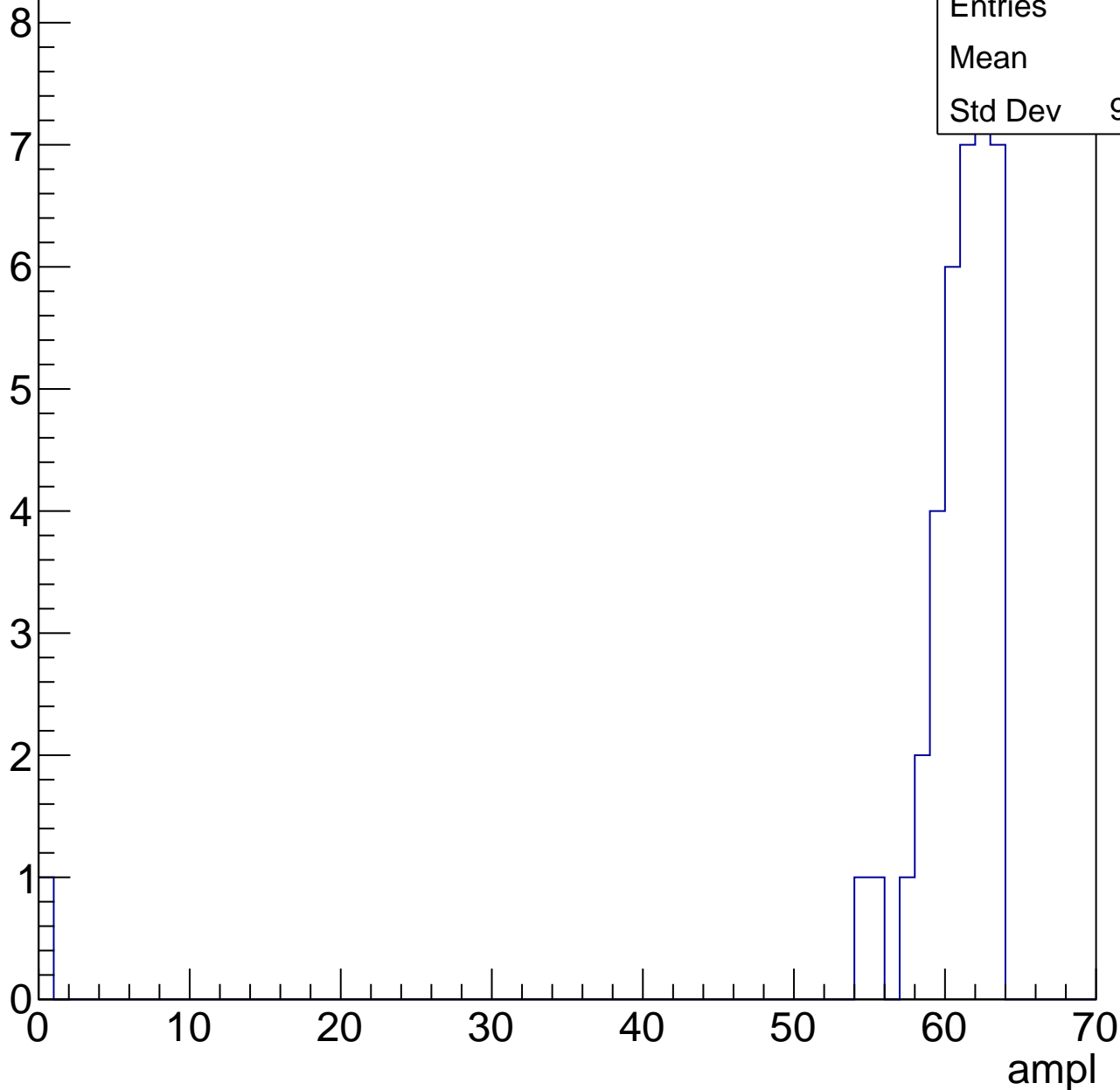


# B0L001S, U24-ch10, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	38
Mean	59
Std Dev	9.929



# B0L001S, U24-ch10, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch10, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U24-ch11, adc0

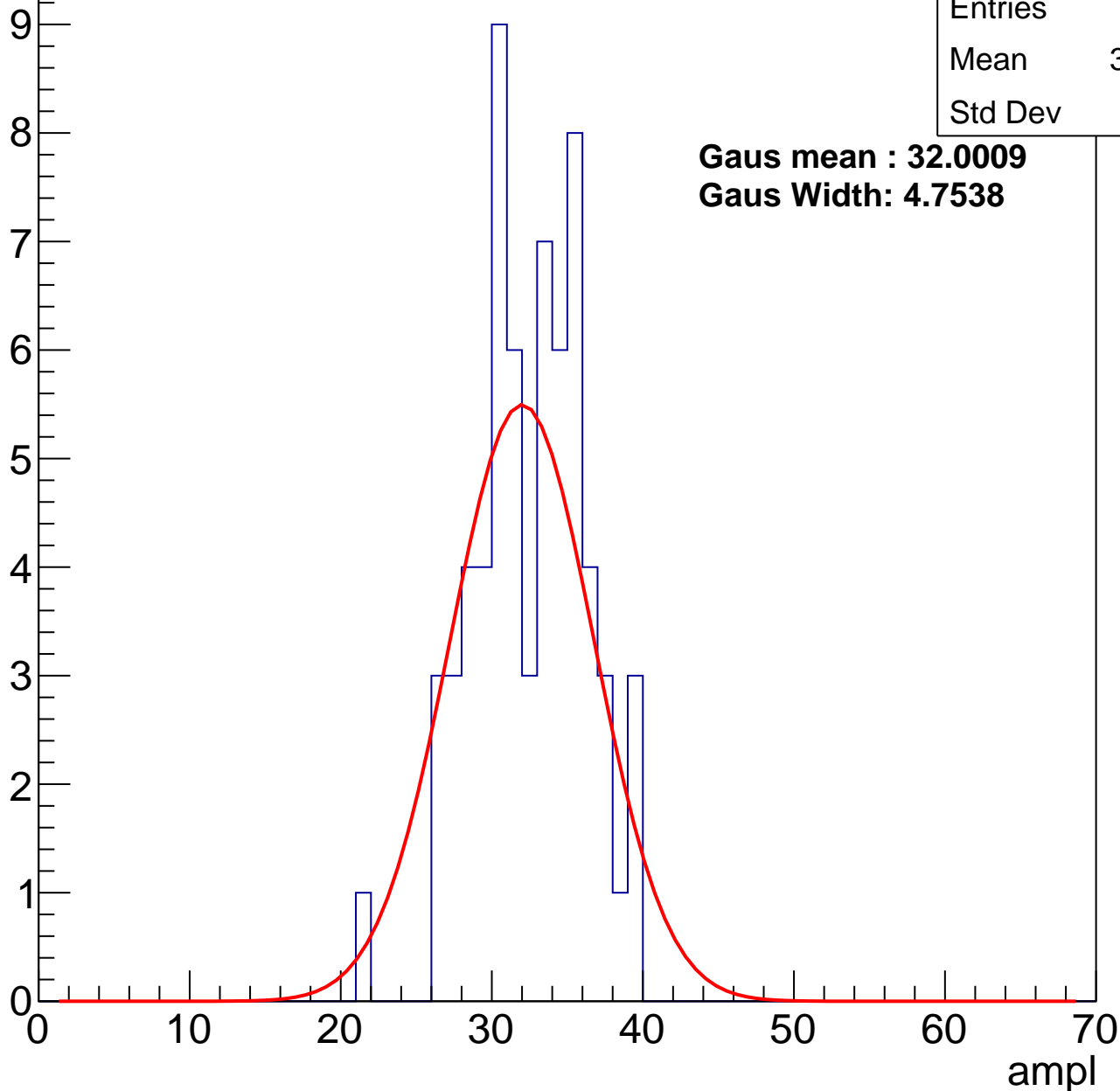
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	32.08
Std Dev	3.66

**Gaus mean : 32.0009**

**Gaus Width: 4.7538**



# B0L001S, U24-ch11, adc1

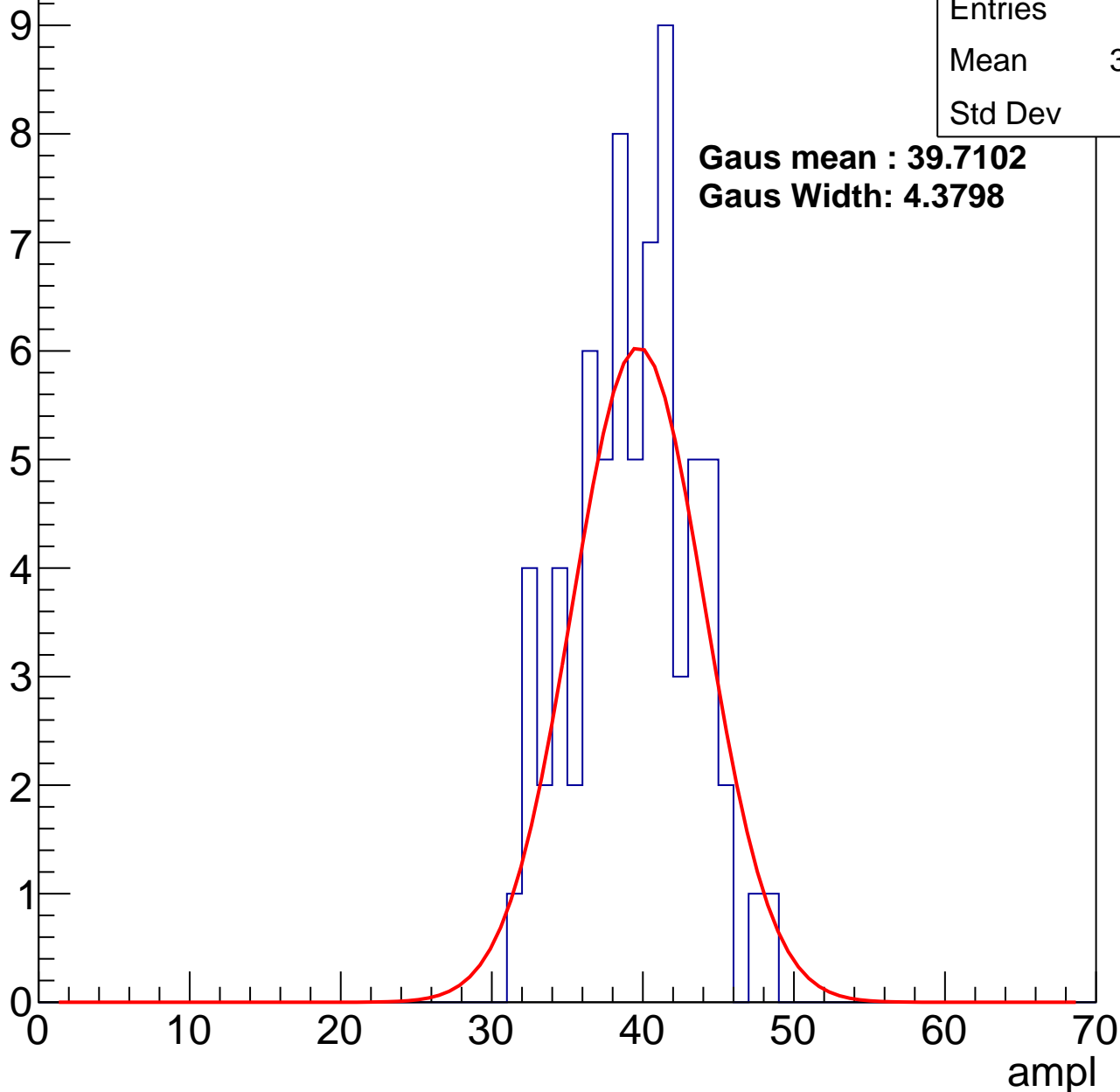
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	38.94
Std Dev	3.85

**Gaus mean : 39.7102**

**Gaus Width: 4.3798**



# B0L001S, U24-ch11, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	72
Mean	45.49
Std Dev	3.586

**Gaus mean : 46.6709**

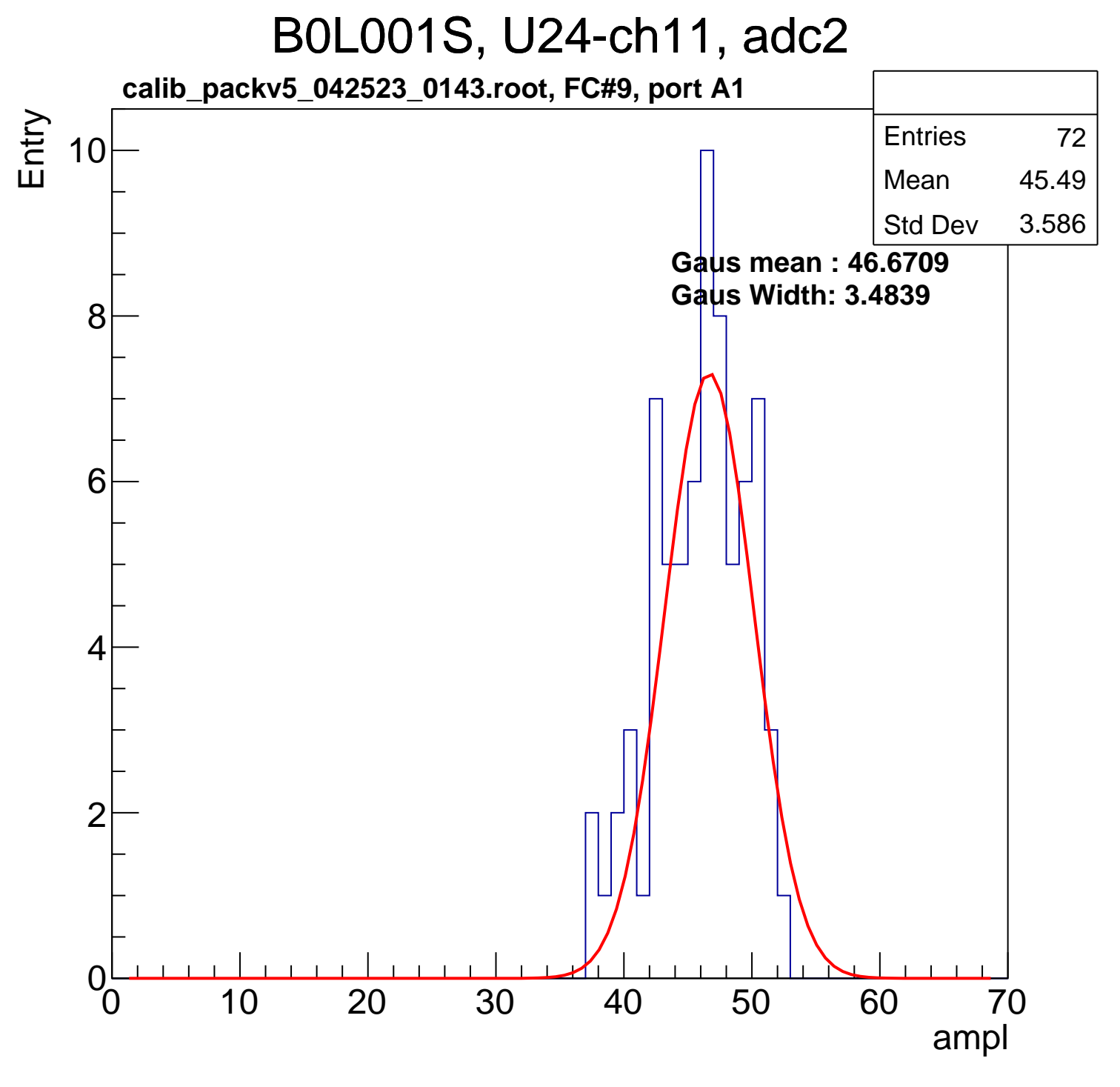
**Gaus Width: 3.4839**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

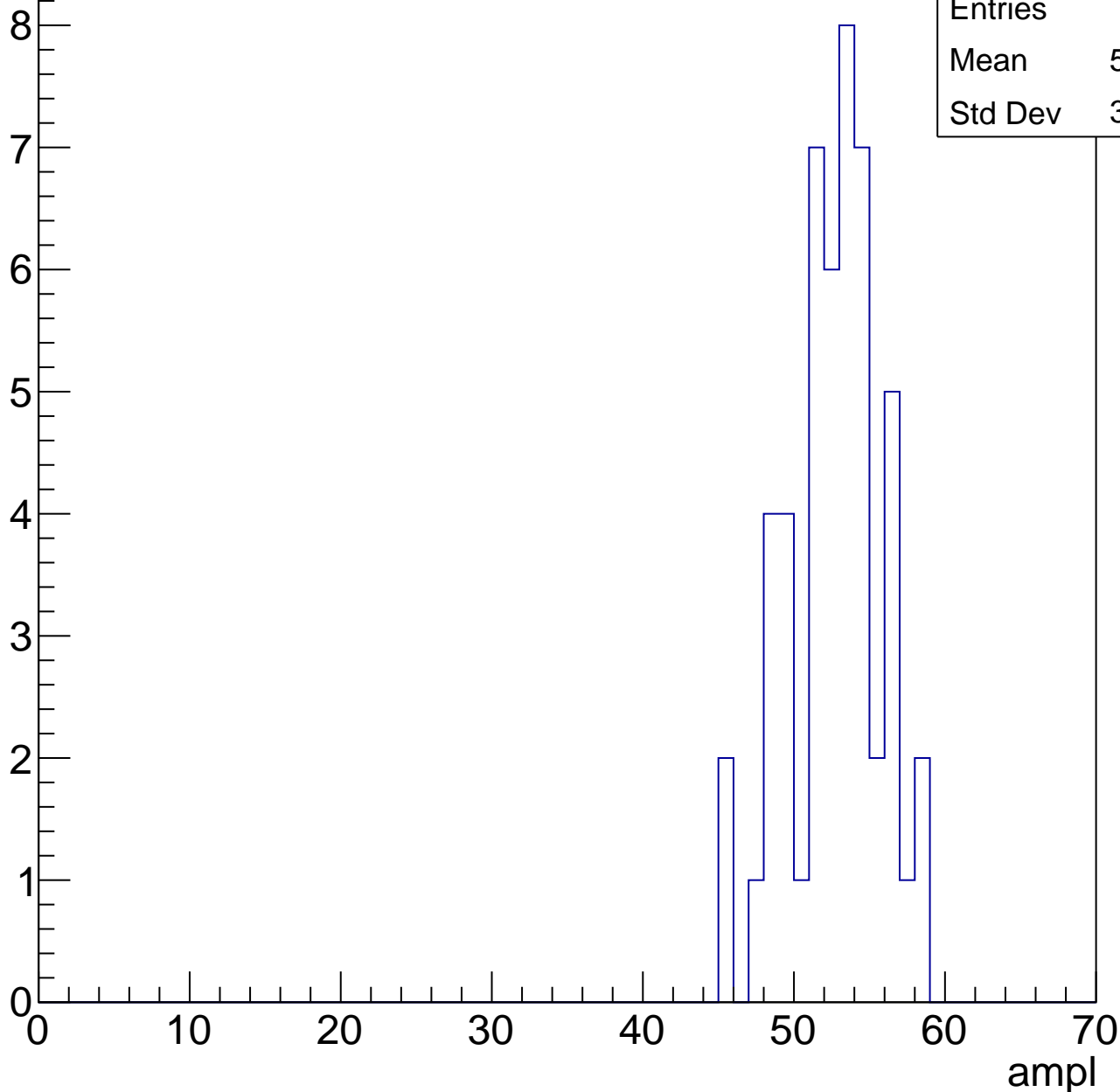


# B0L001S, U24-ch11, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	50
Mean	52.18
Std Dev	3.044

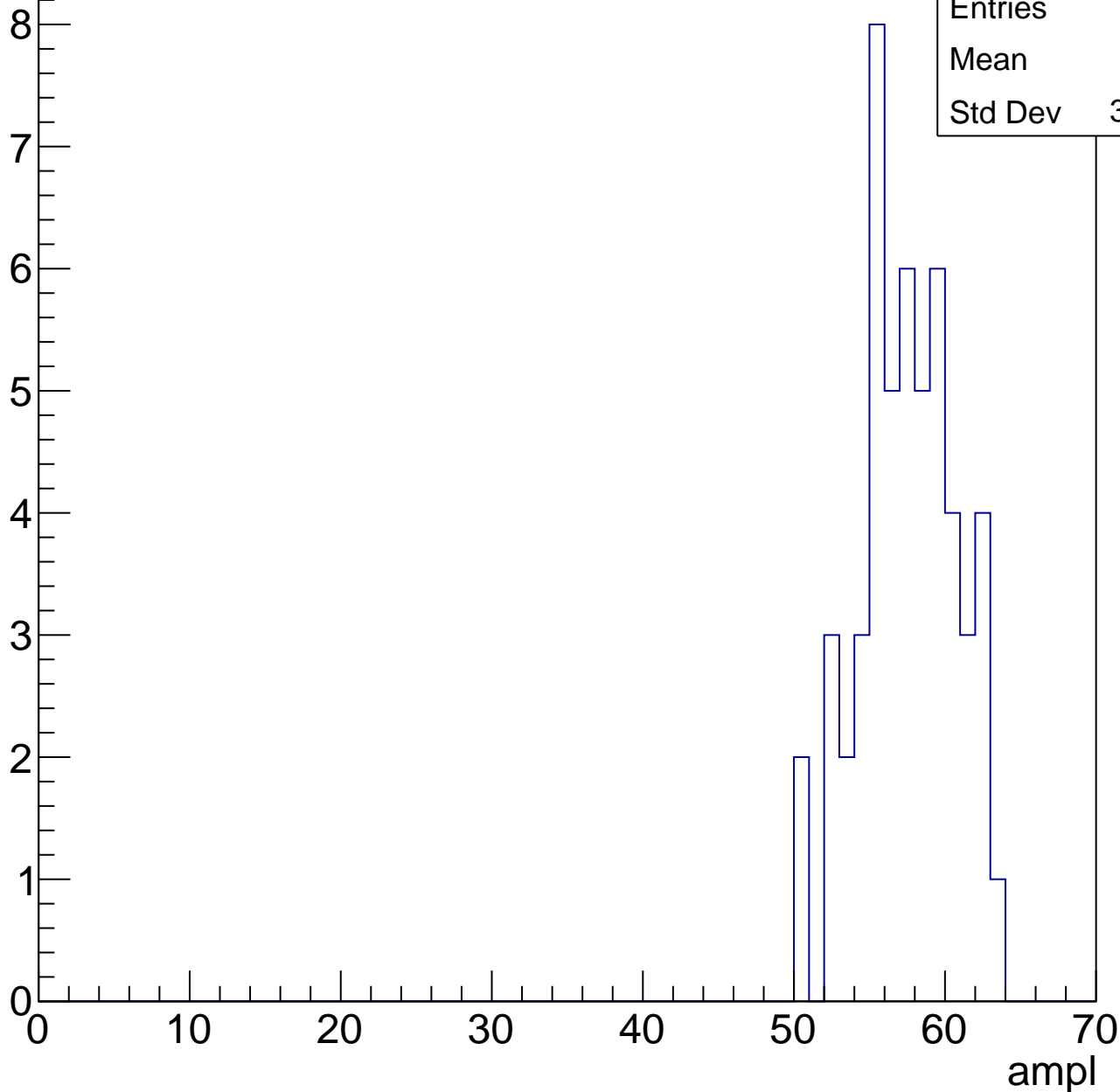


# B0L001S, U24-ch11, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	57
Std Dev	3.156

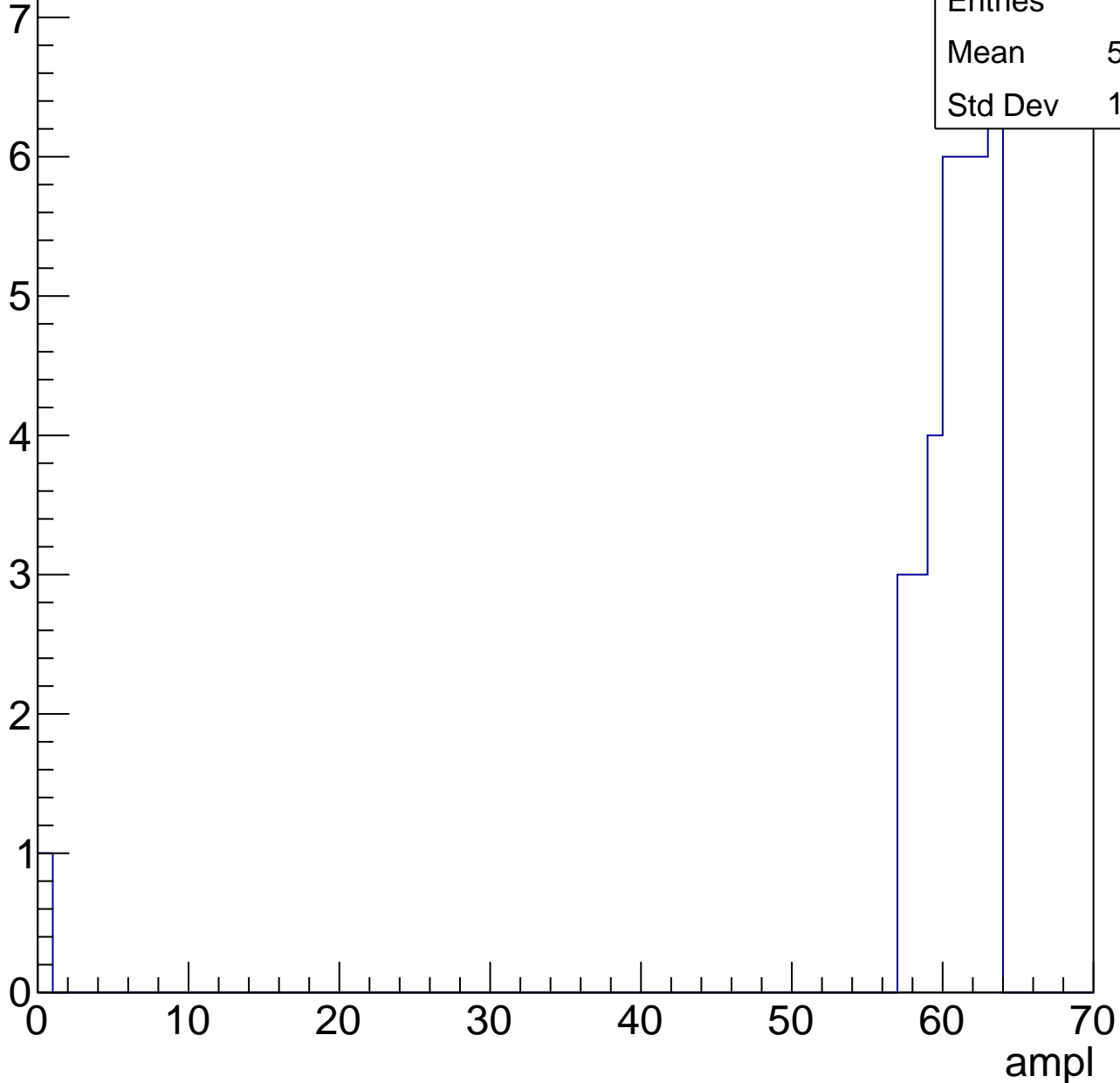


# B0L001S, U24-ch11, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	36
Mean	58.89
Std Dev	10.13



# B0L001S, U24-ch11, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch11, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U24-ch12, adc0

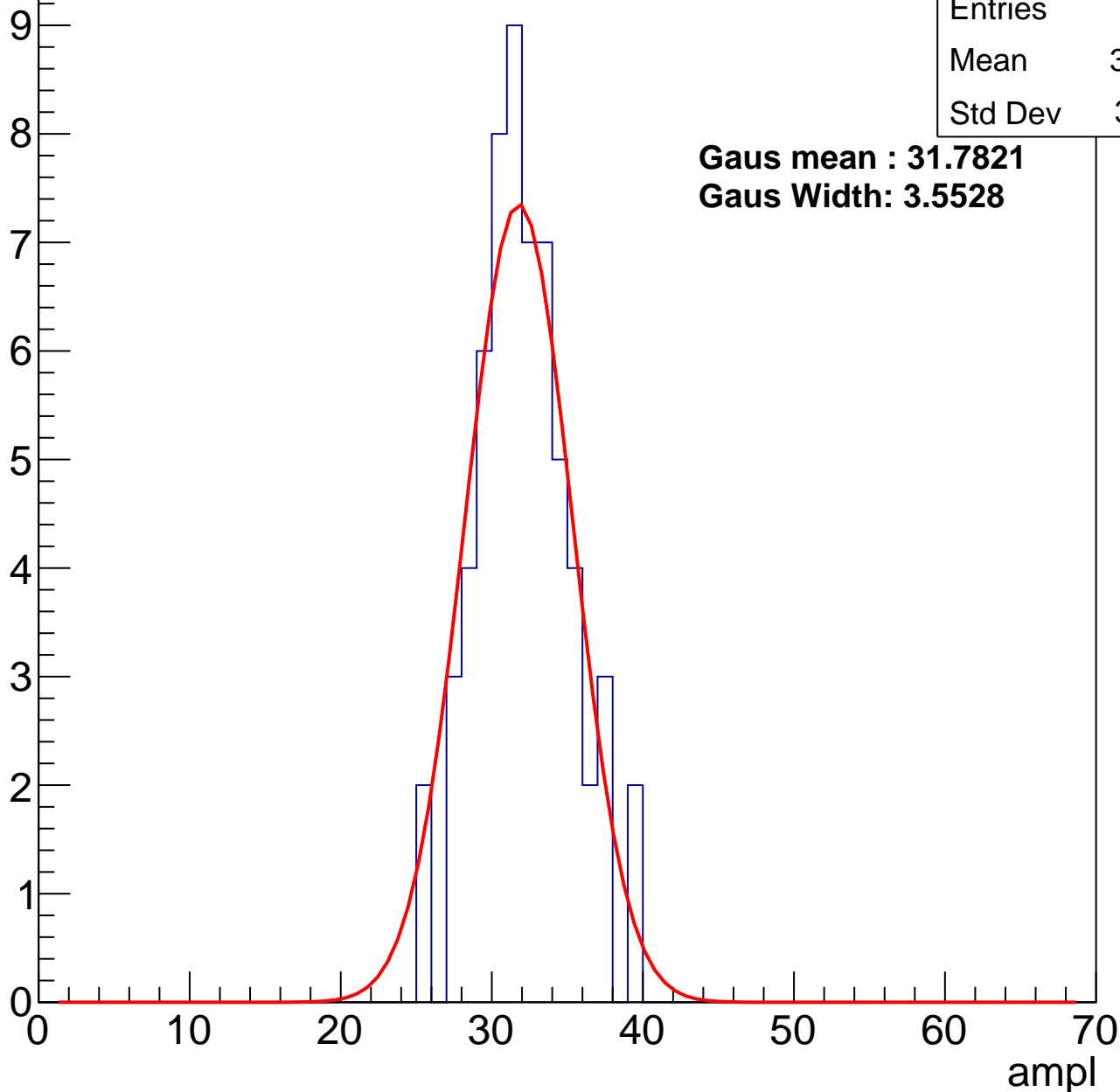
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	31.65
Std Dev	3.091

**Gaus mean : 31.7821**

**Gaus Width: 3.5528**



# B0L001S, U24-ch12, adc1

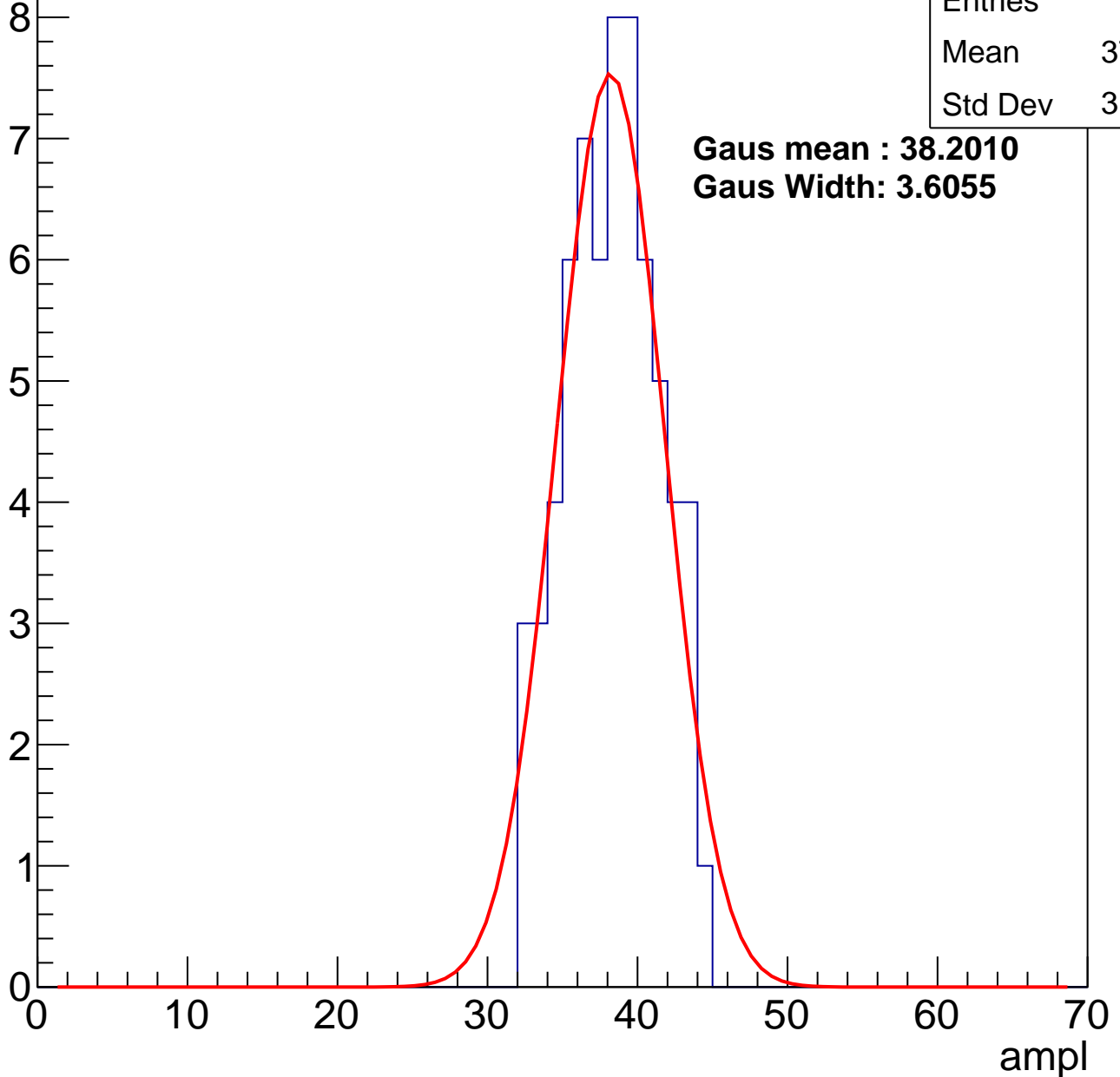
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	37.85
Std Dev	3.065

**Gaus mean : 38.2010**

**Gaus Width: 3.6055**



# B0L001S, U24-ch12, adc2

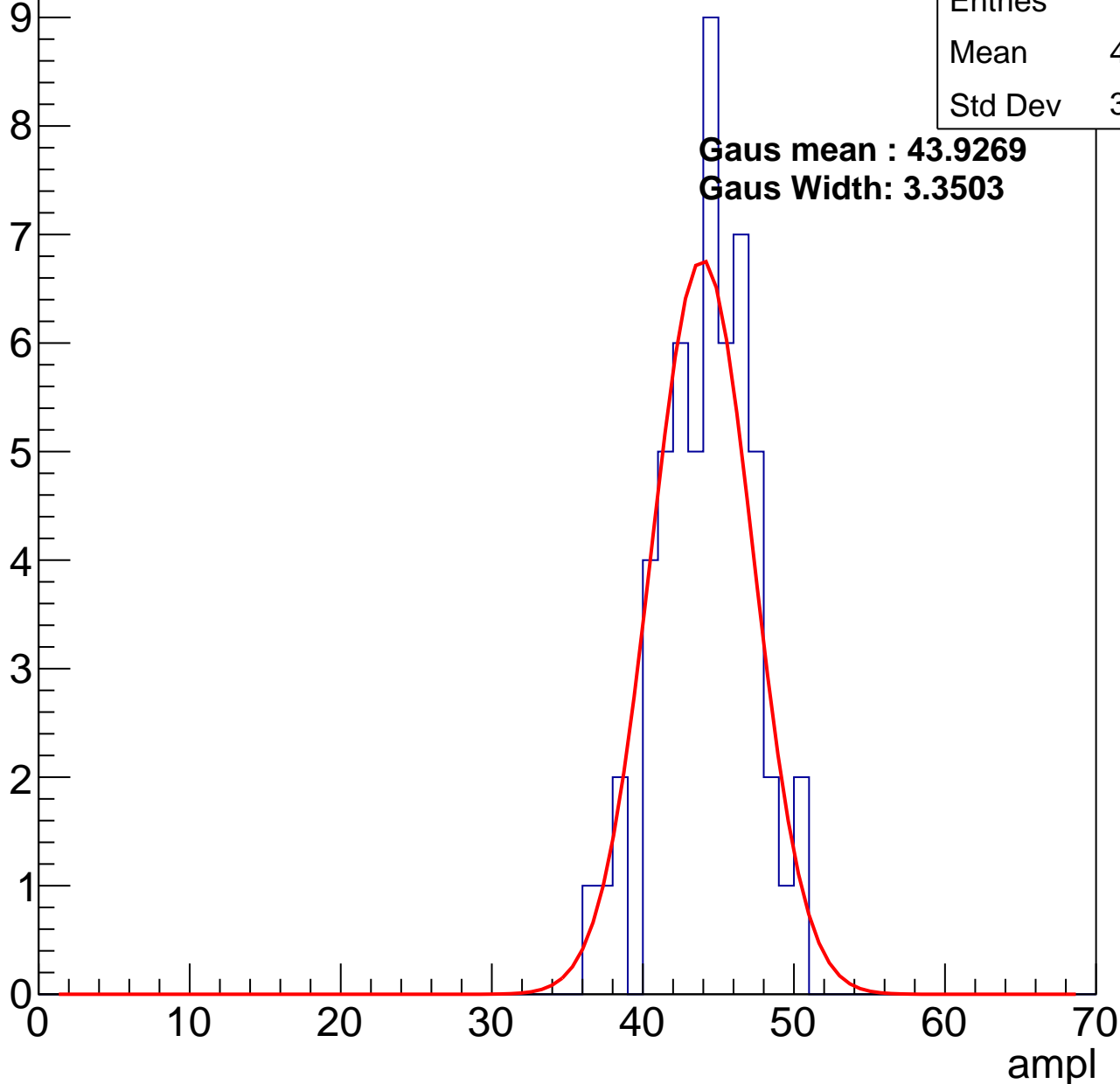
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	43.73
Std Dev	3.068

**Gaus mean : 43.9269**

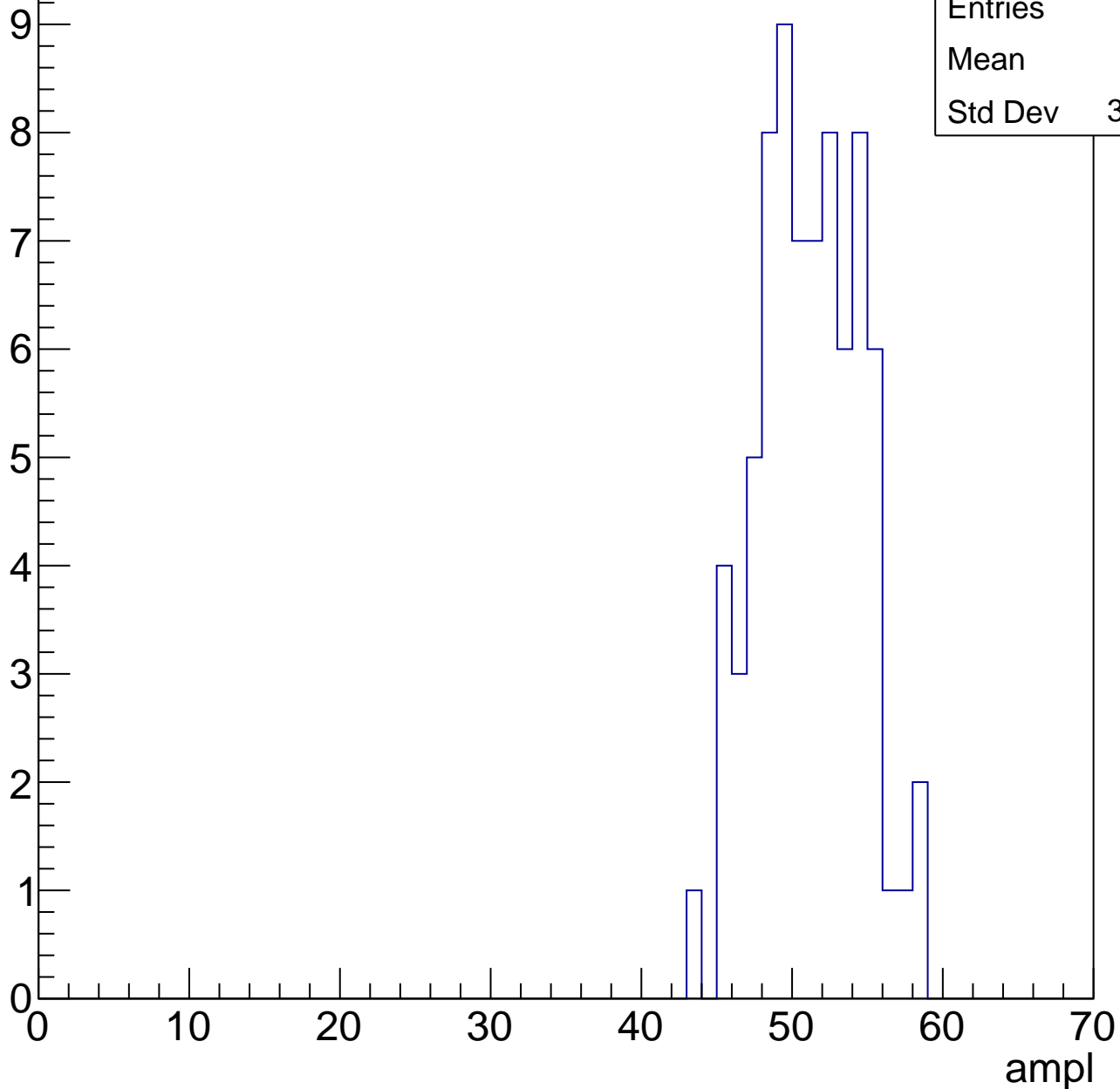
**Gaus Width: 3.3503**



# B0L001S, U24-ch12, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

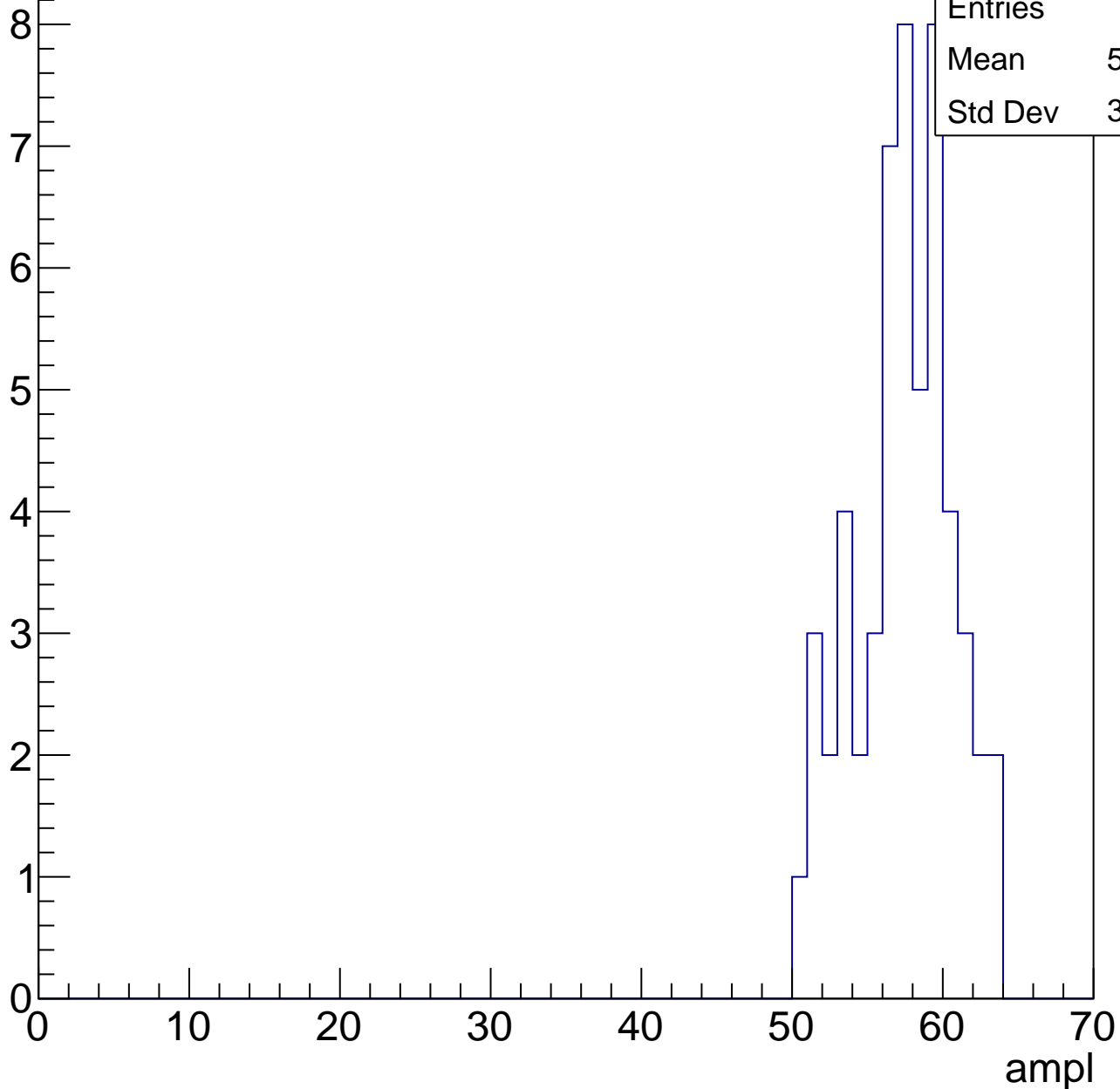


# B0L001S, U24-ch12, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	56.94
Std Dev	3.194

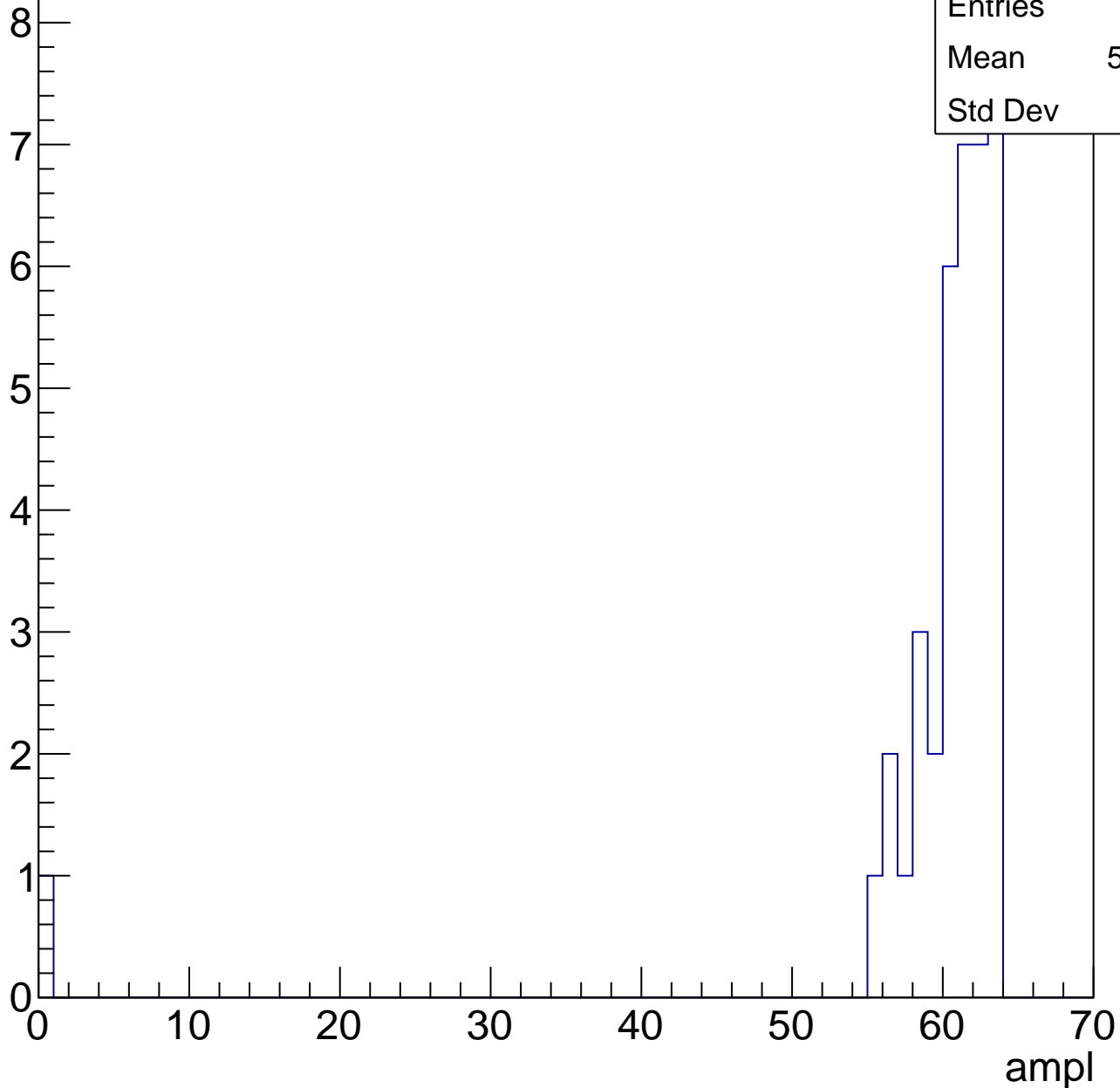


# B0L001S, U24-ch12, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	38
Mean	58.97
Std Dev	9.93



# B0L001S, U24-ch12, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

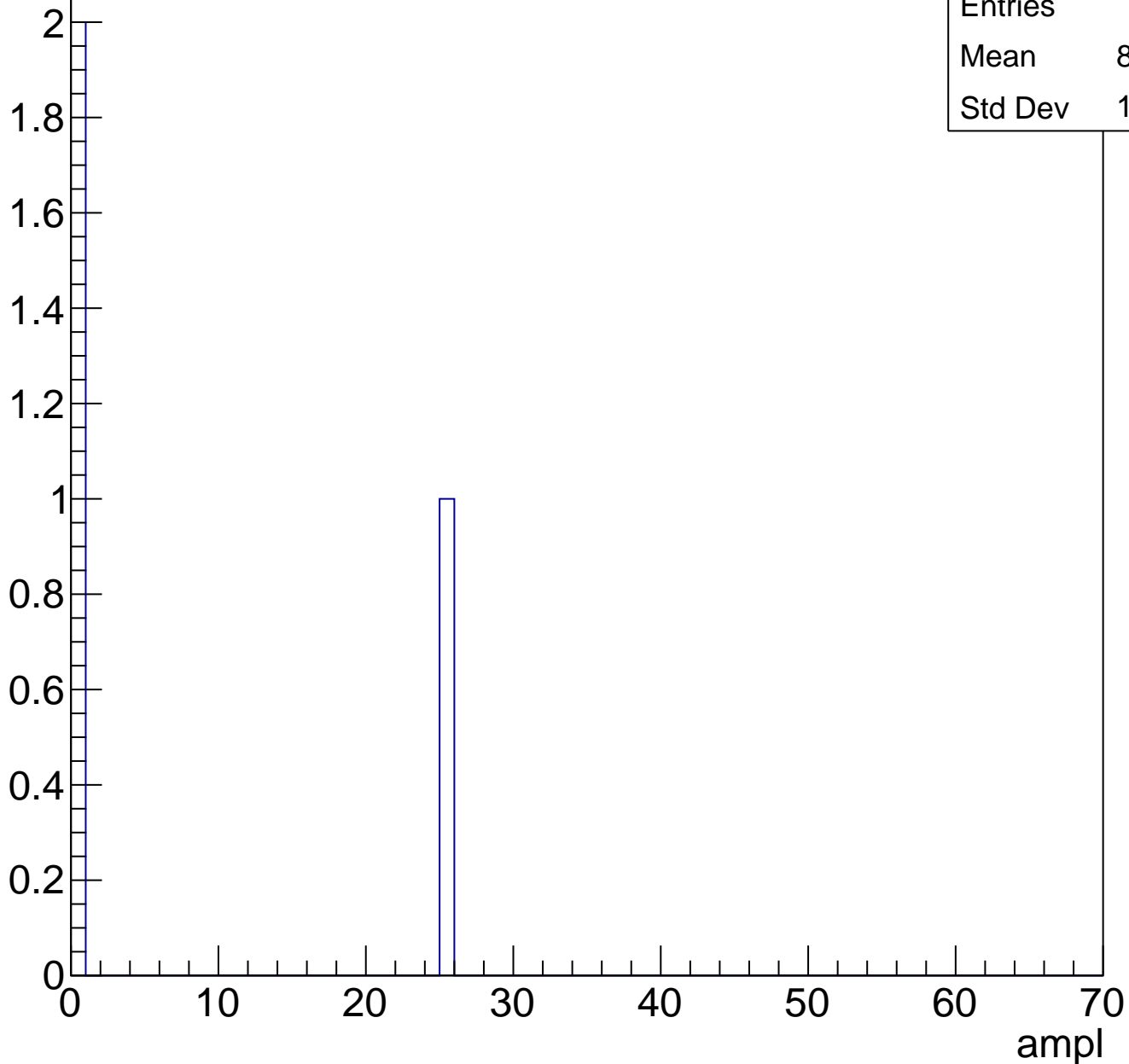




# B0L001S, U24-ch12, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	3
Mean	8.333
Std Dev	11.79

# B0L001S, U24-ch13, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	75
Mean	31.83
Std Dev	4.826

**Gaus mean : 32.8441**

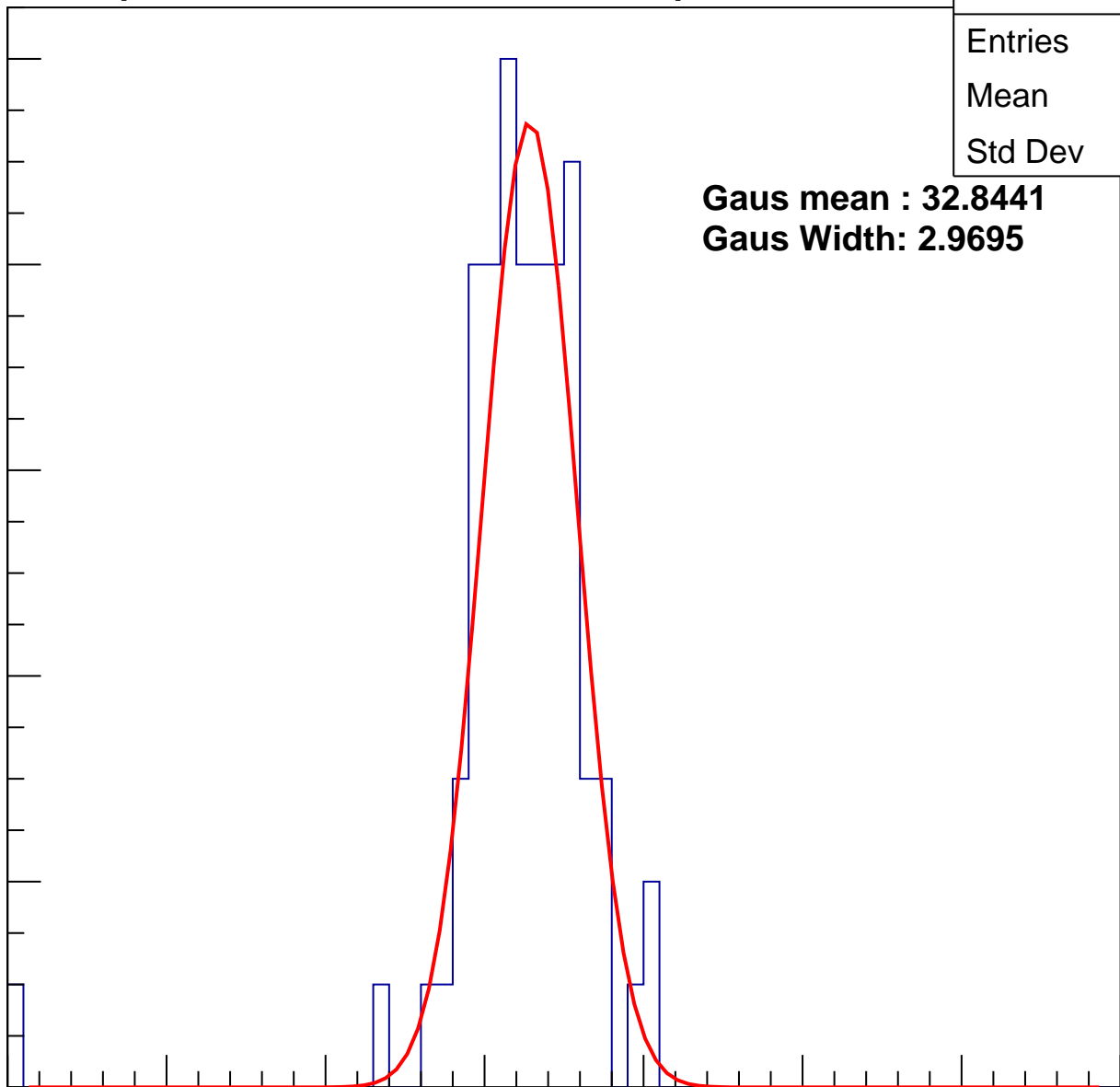
**Gaus Width: 2.9695**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



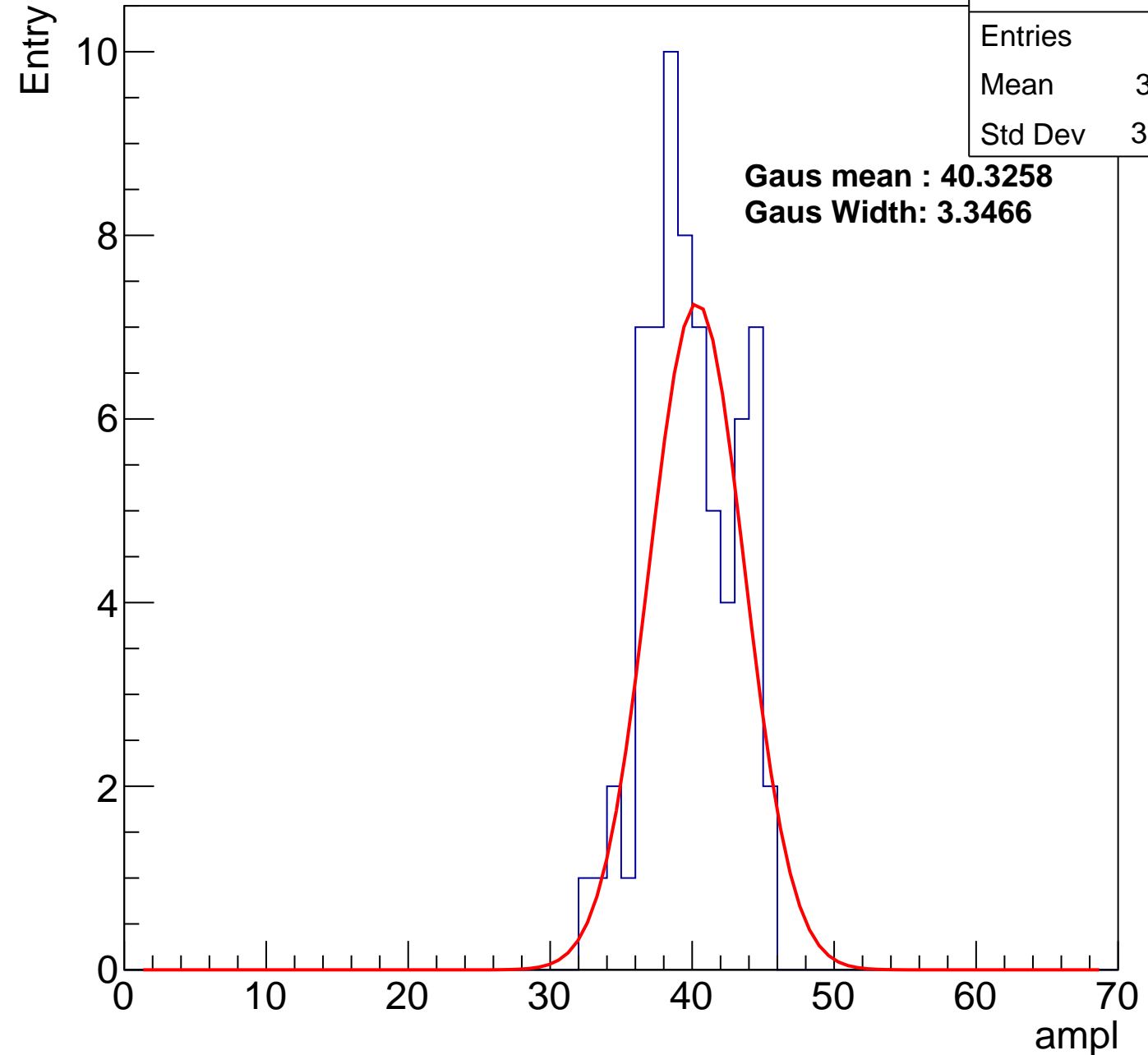
# B0L001S, U24-ch13, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	68
Mean	39.41
Std Dev	3.083

**Gaus mean : 40.3258**

**Gaus Width: 3.3466**



# B0L001S, U24-ch13, adc2

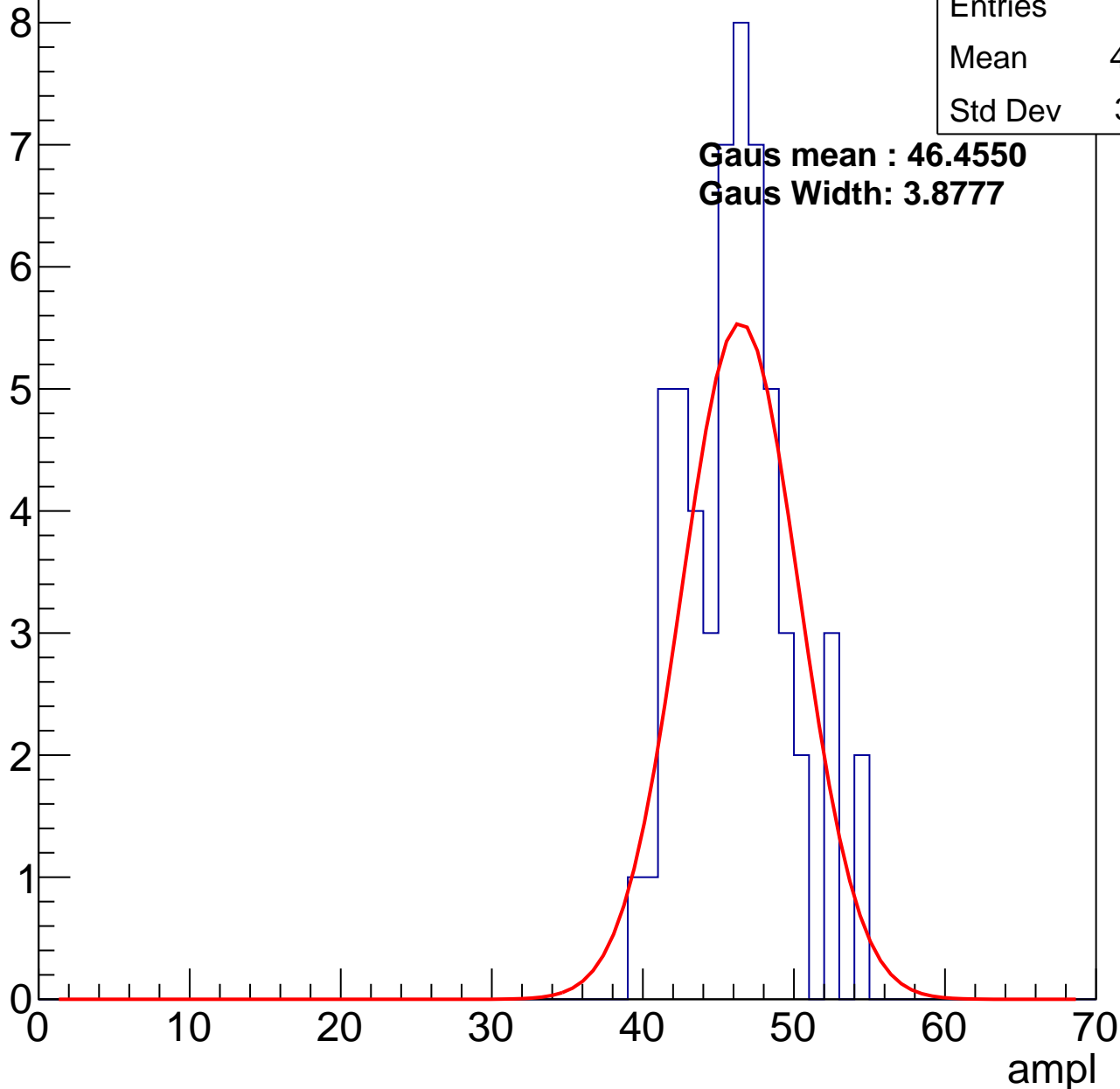
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	45.73
Std Dev	3.441

**Gaus mean : 46.4550**

**Gaus Width: 3.8777**



# B0L001S, U24-ch13, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	84
Mean	52.44
Std Dev	3.768

Entry

10

8

6

4

2

0

0

10

20

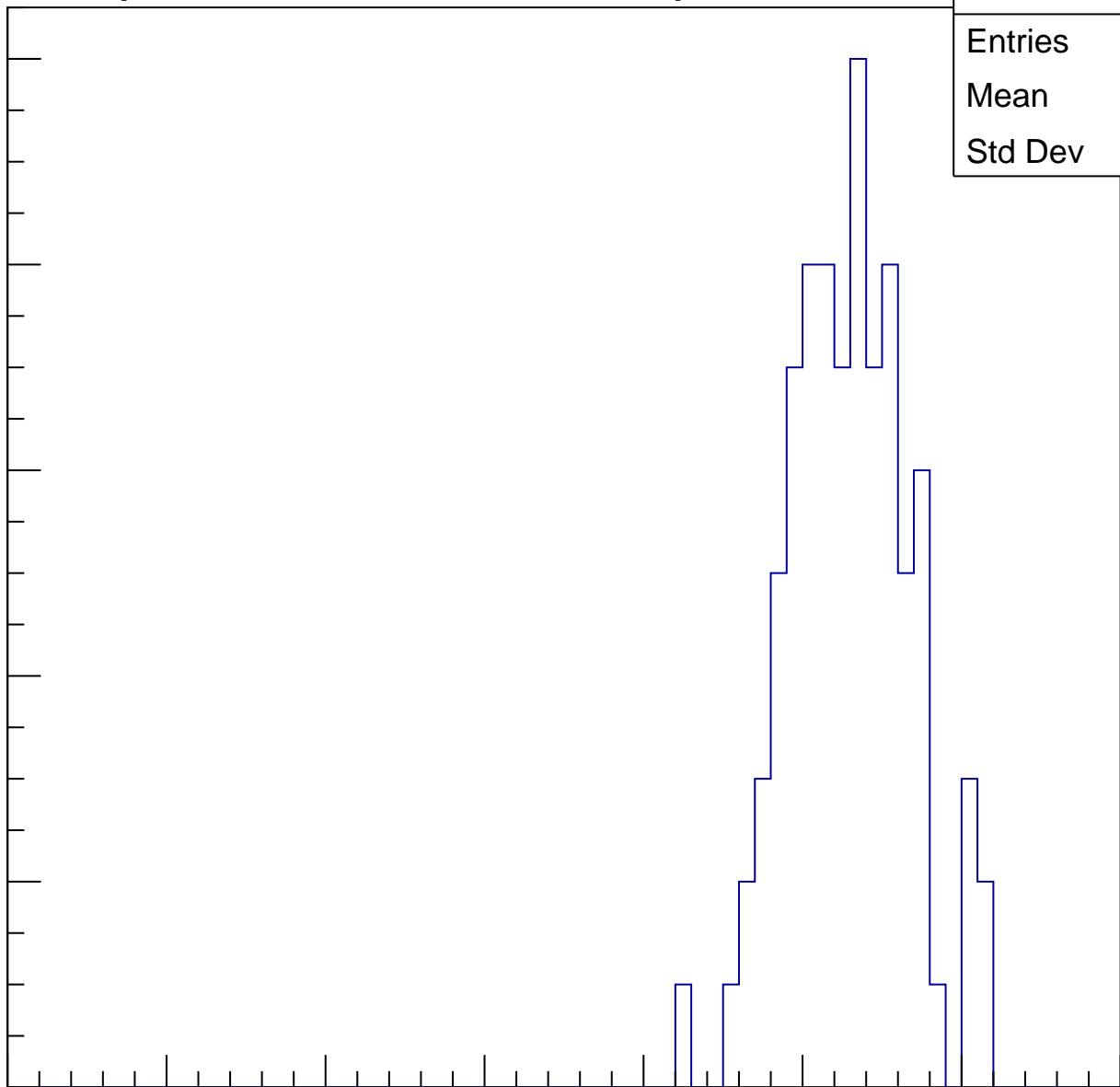
30

40

50

60

ampl

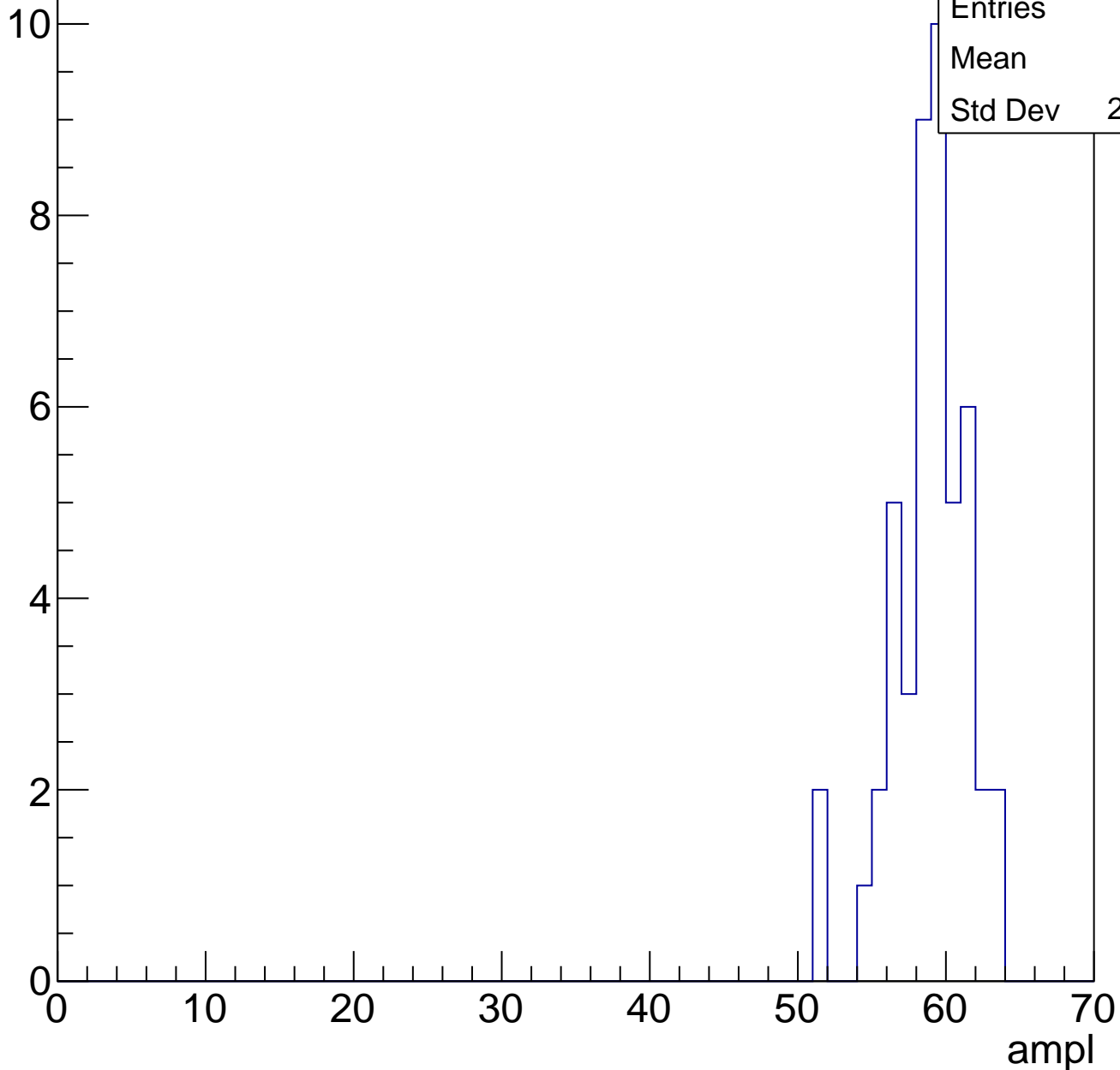


# B0L001S, U24-ch13, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	47
Mean	58.4
Std Dev	2.582

Entry

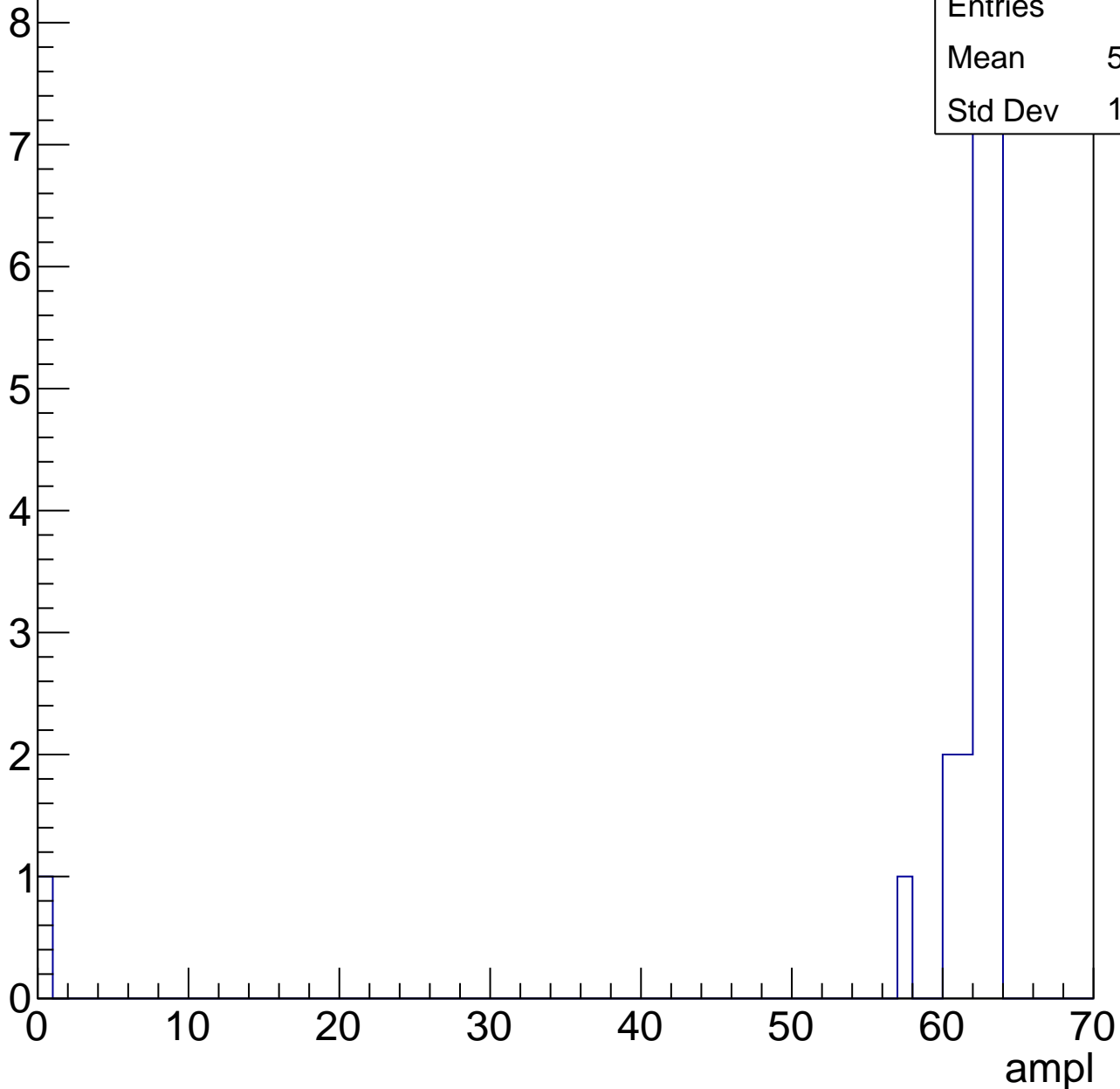


# B0L001S, U24-ch13, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	22
Mean	59.05
Std Dev	12.96



# B0L001S, U24-ch13, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U24-ch13, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U24-ch14, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	69
Mean	29.42
Std Dev	3.329

**Gaus mean : 30.0085**

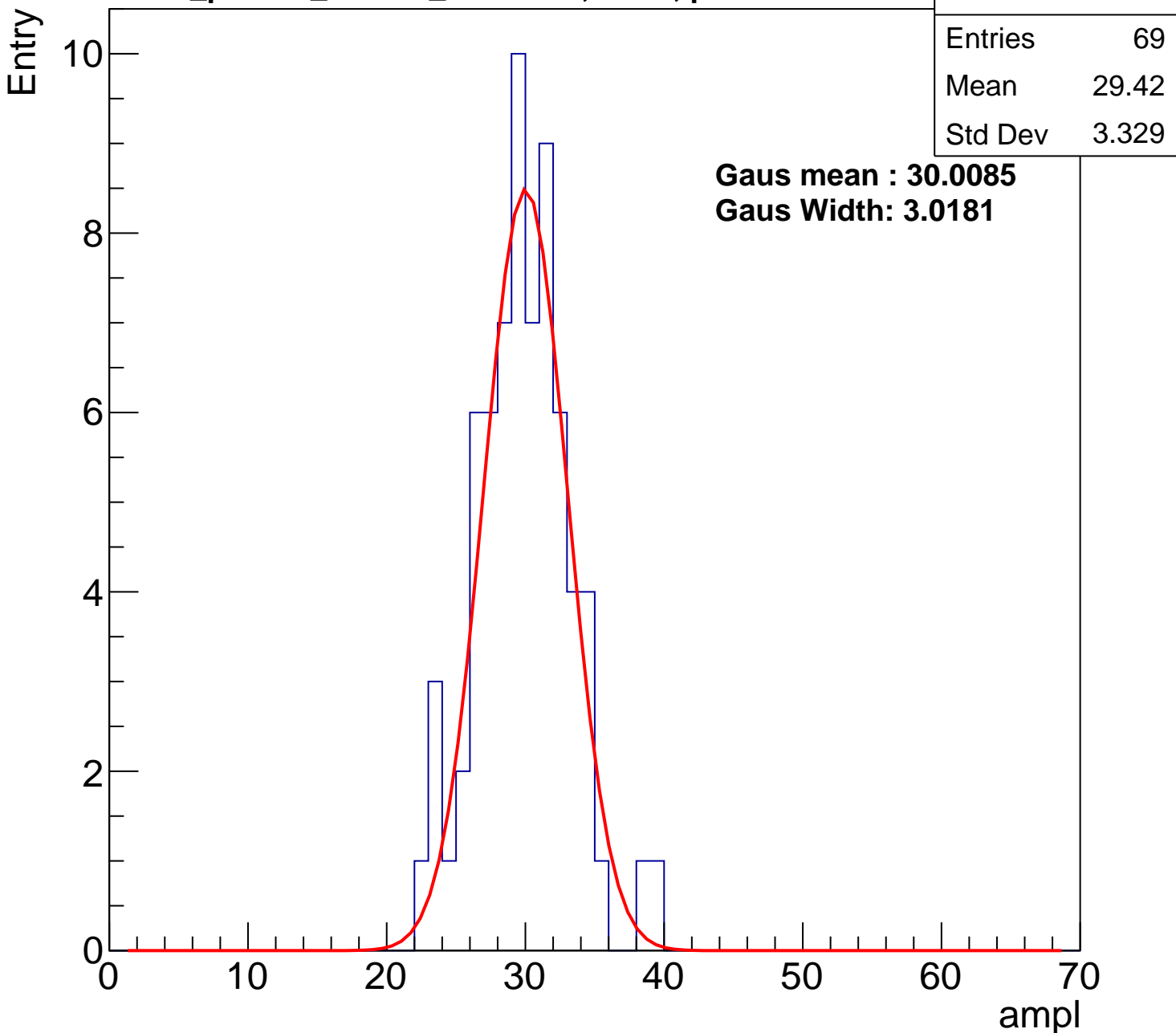
**Gaus Width: 3.0181**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



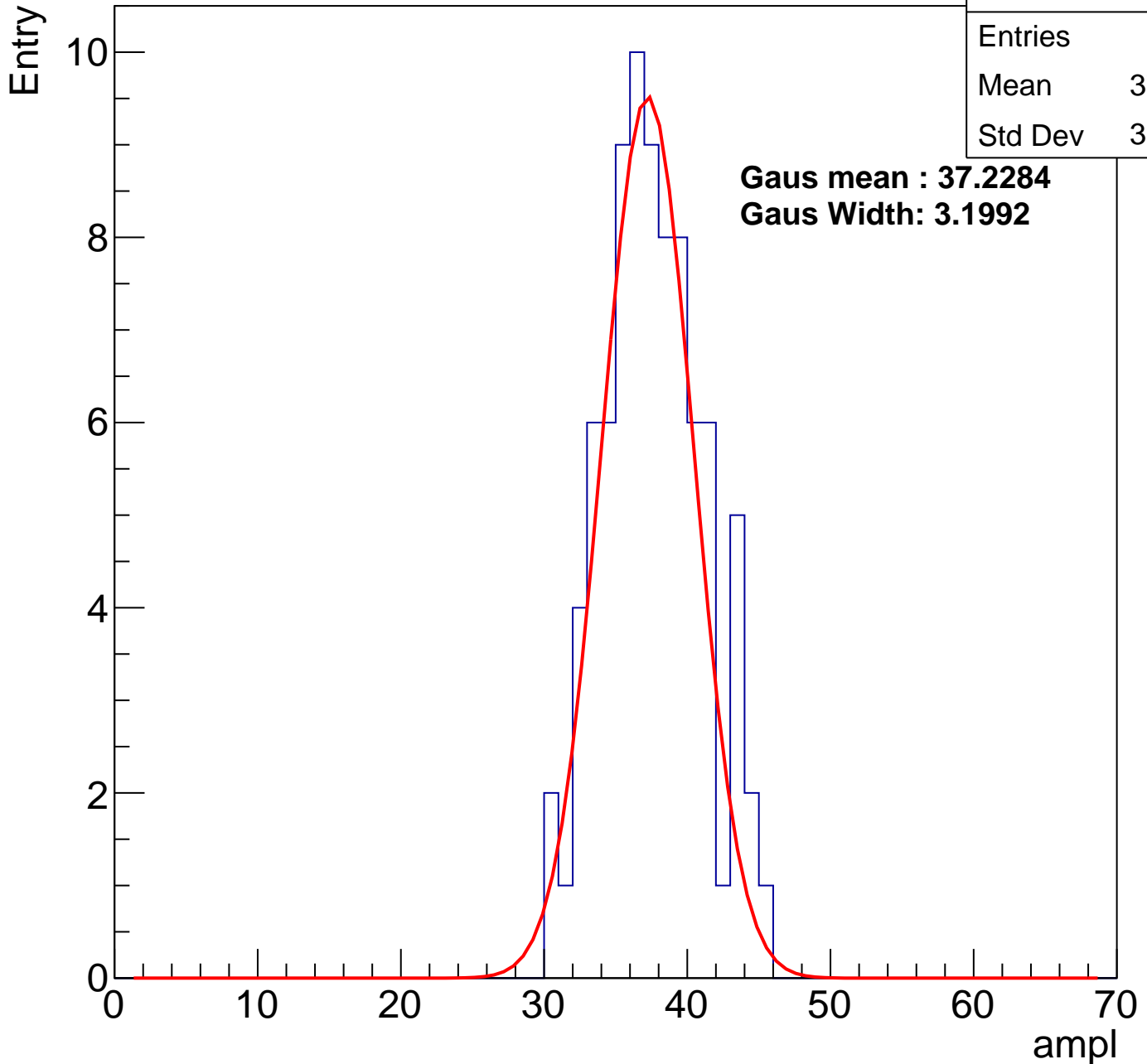
# B0L001S, U24-ch14, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	84
Mean	37.15
Std Dev	3.424

**Gaus mean : 37.2284**

**Gaus Width: 3.1992**



# B0L001S, U24-ch14, adc2

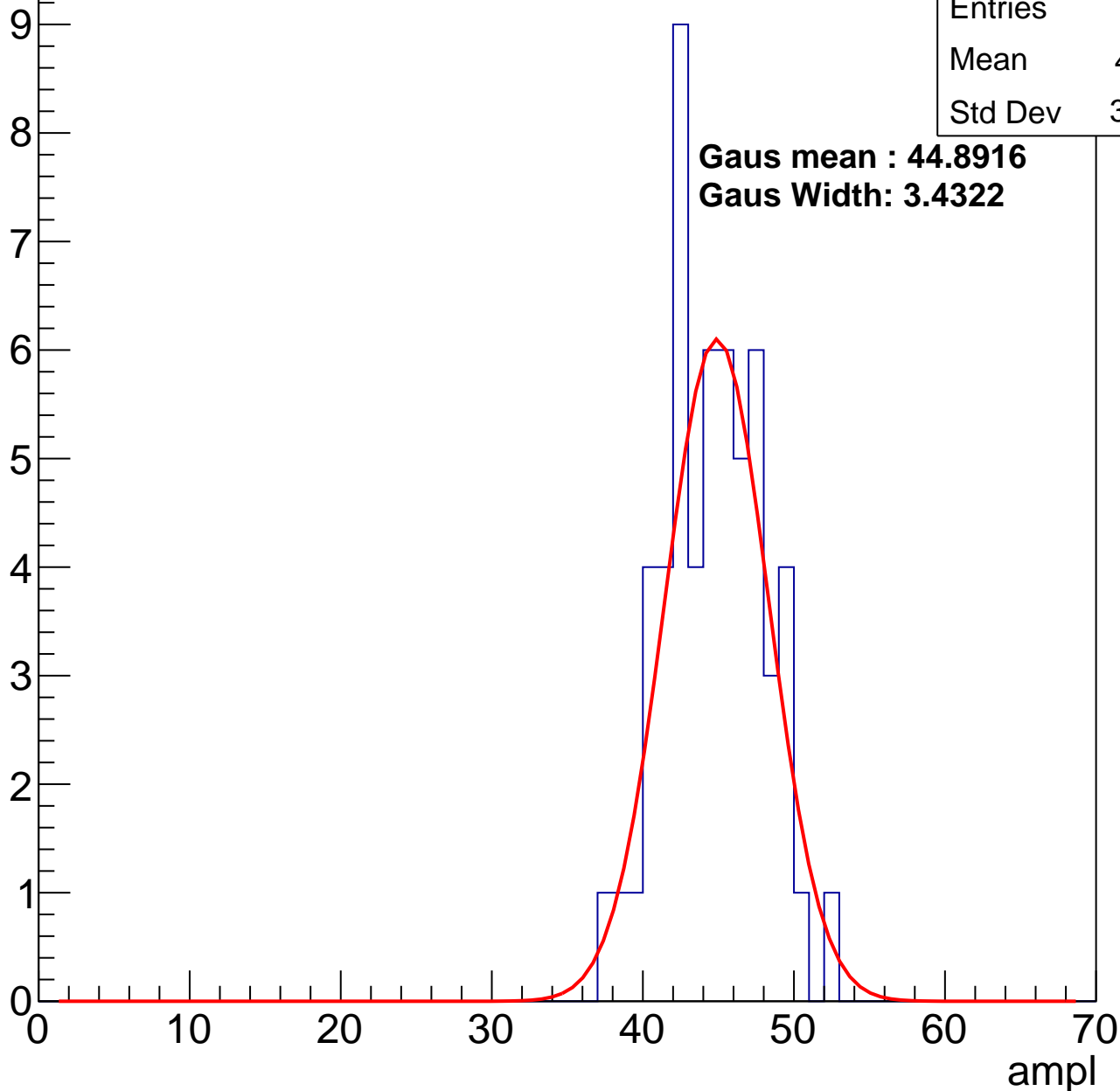
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	44.21
Std Dev	3.206

**Gaus mean : 44.8916**

**Gaus Width: 3.4322**

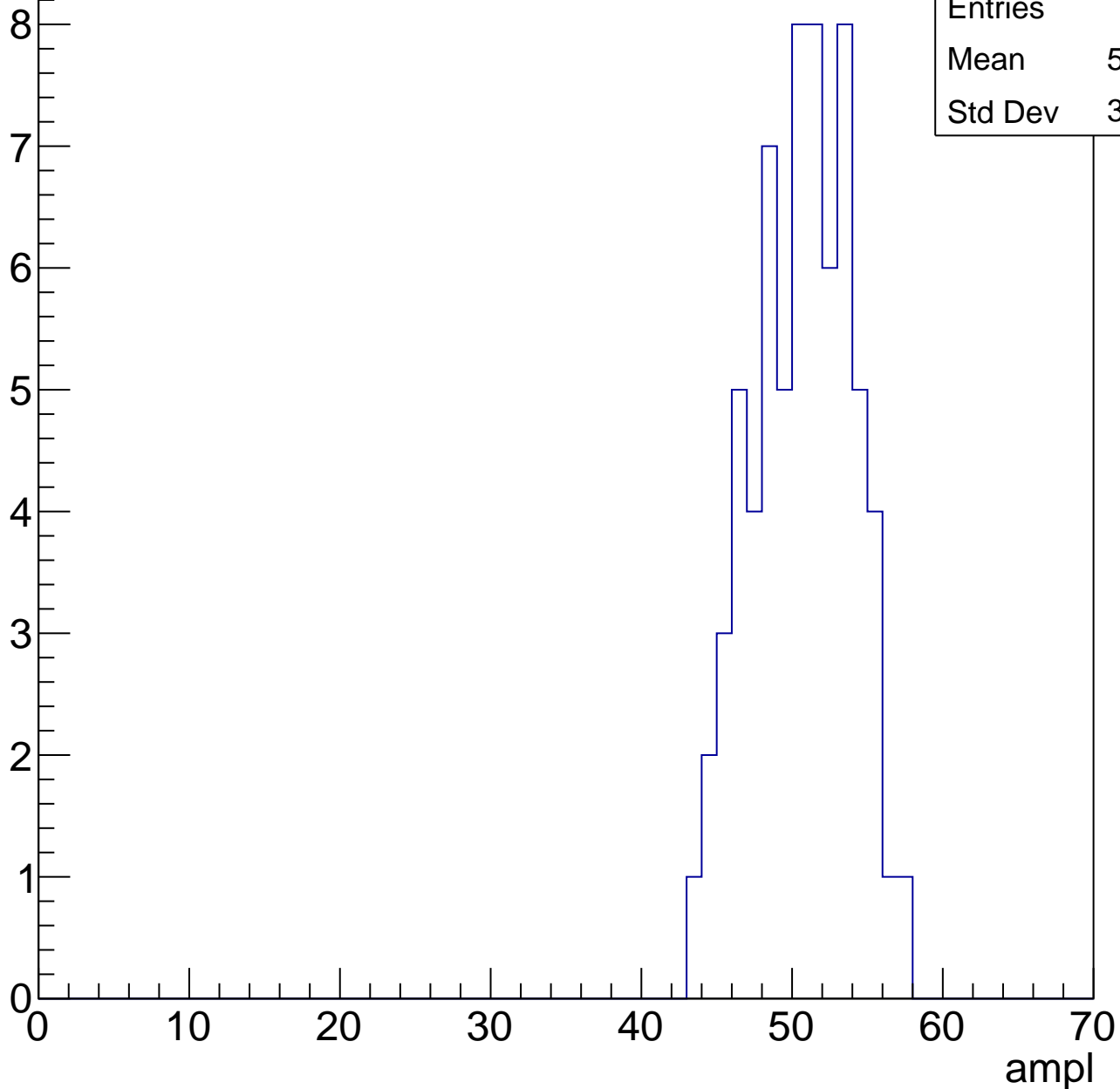


# B0L001S, U24-ch14, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	50.18
Std Dev	3.236

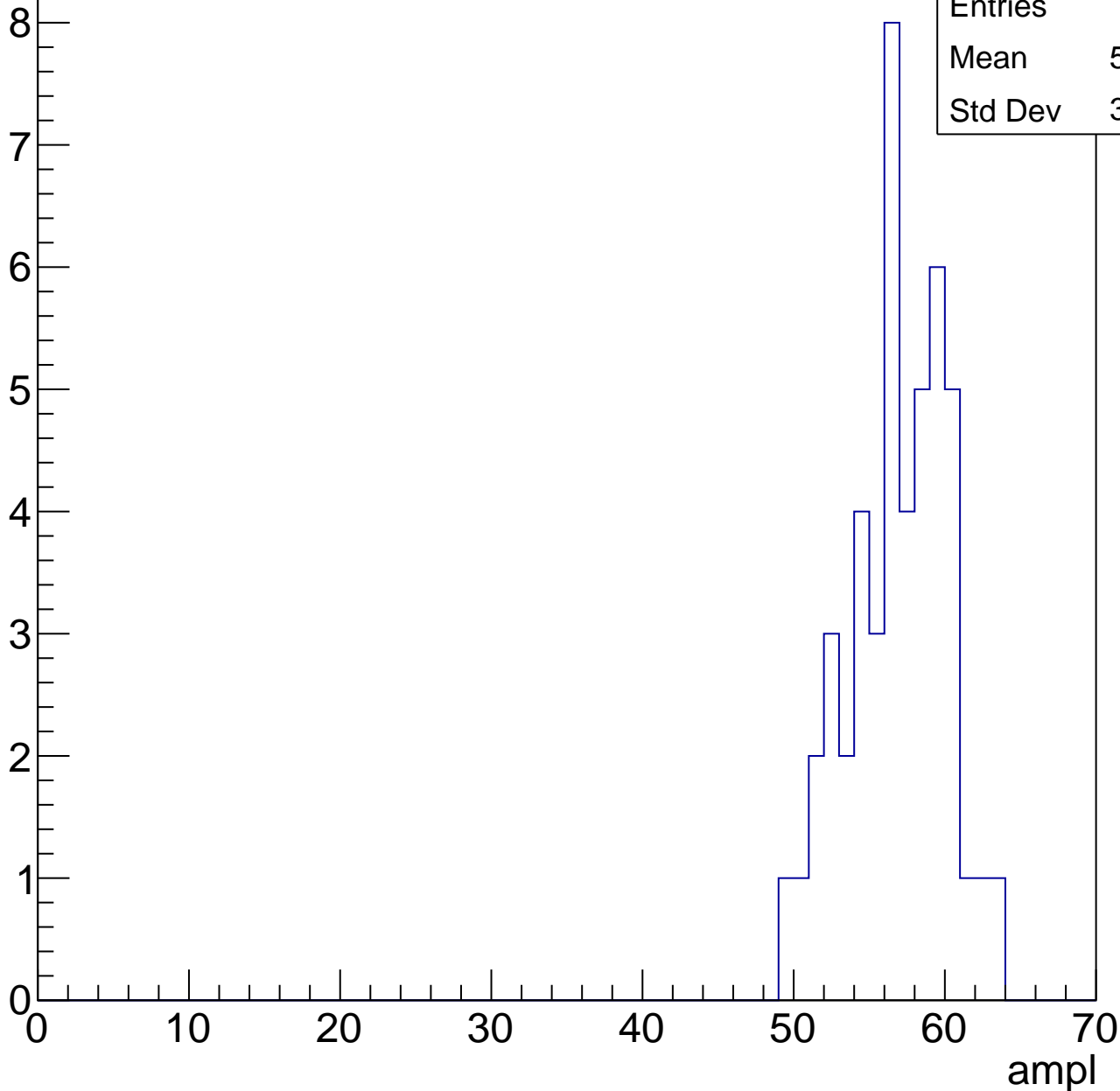


# B0L001S, U24-ch14, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	47
Mean	56.38
Std Dev	3.199

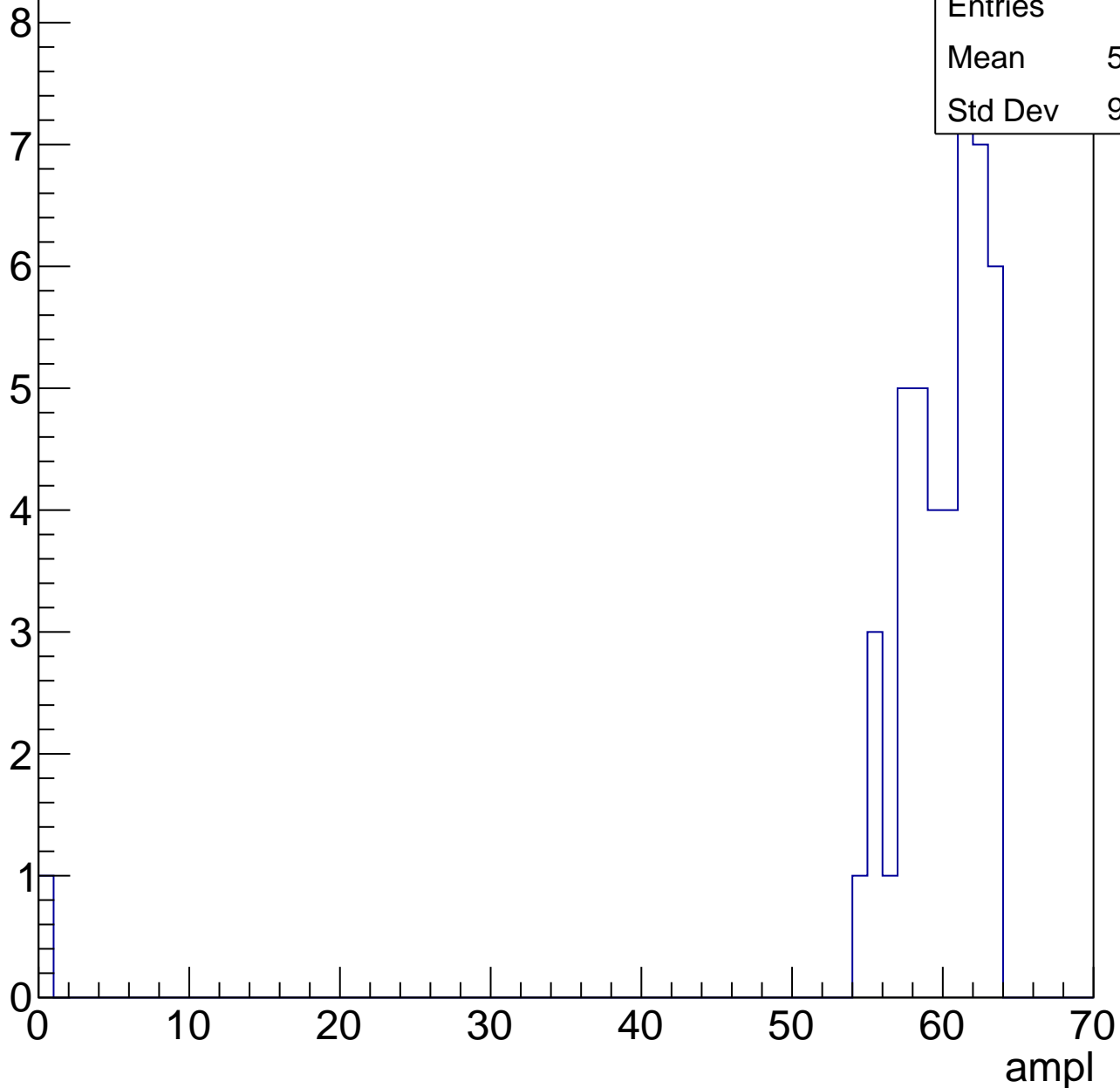


# B0L001S, U24-ch14, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	45
Mean	58.36
Std Dev	9.146



# B0L001S, U24-ch14, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch14, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

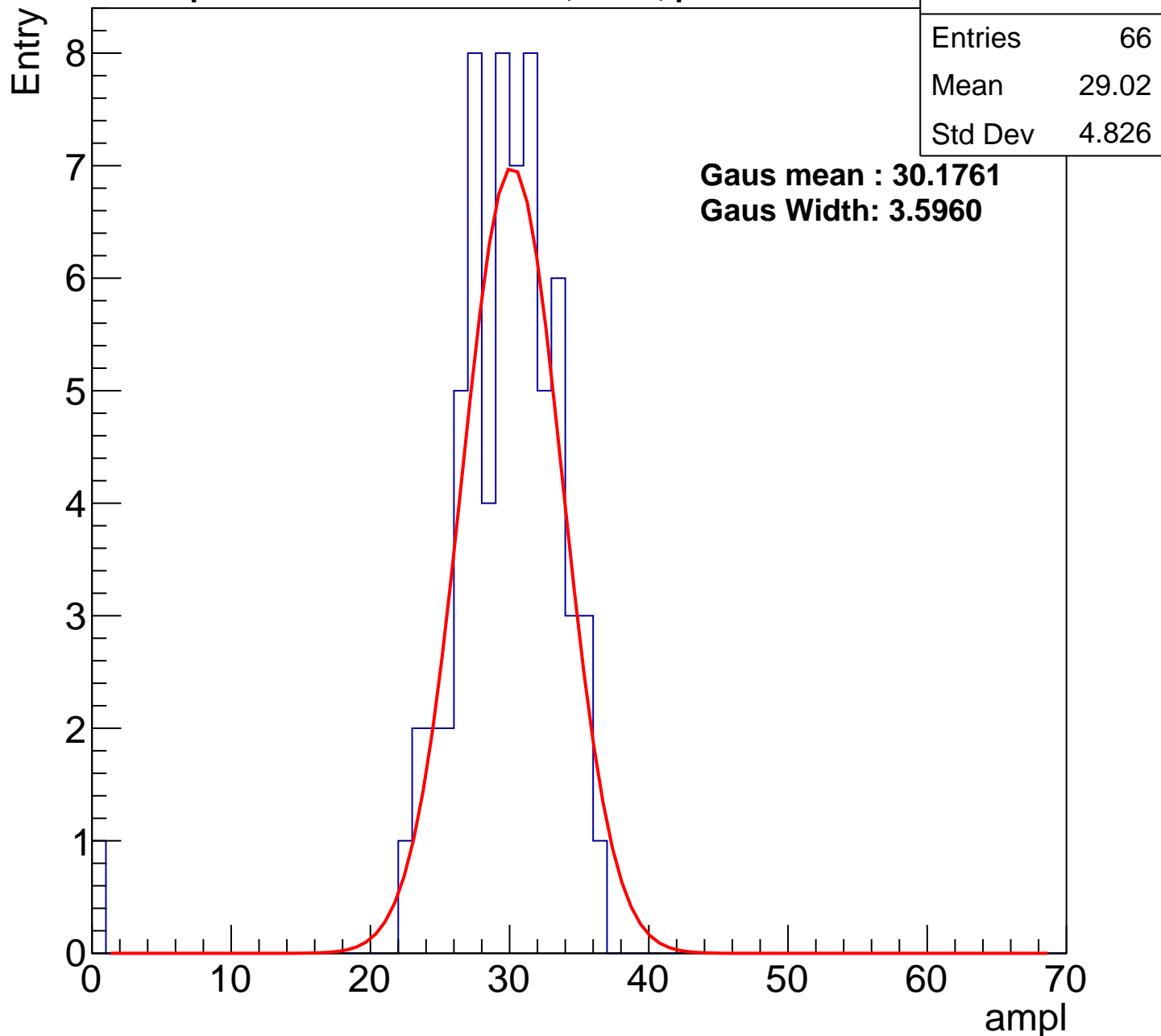
Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U24-ch15, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1



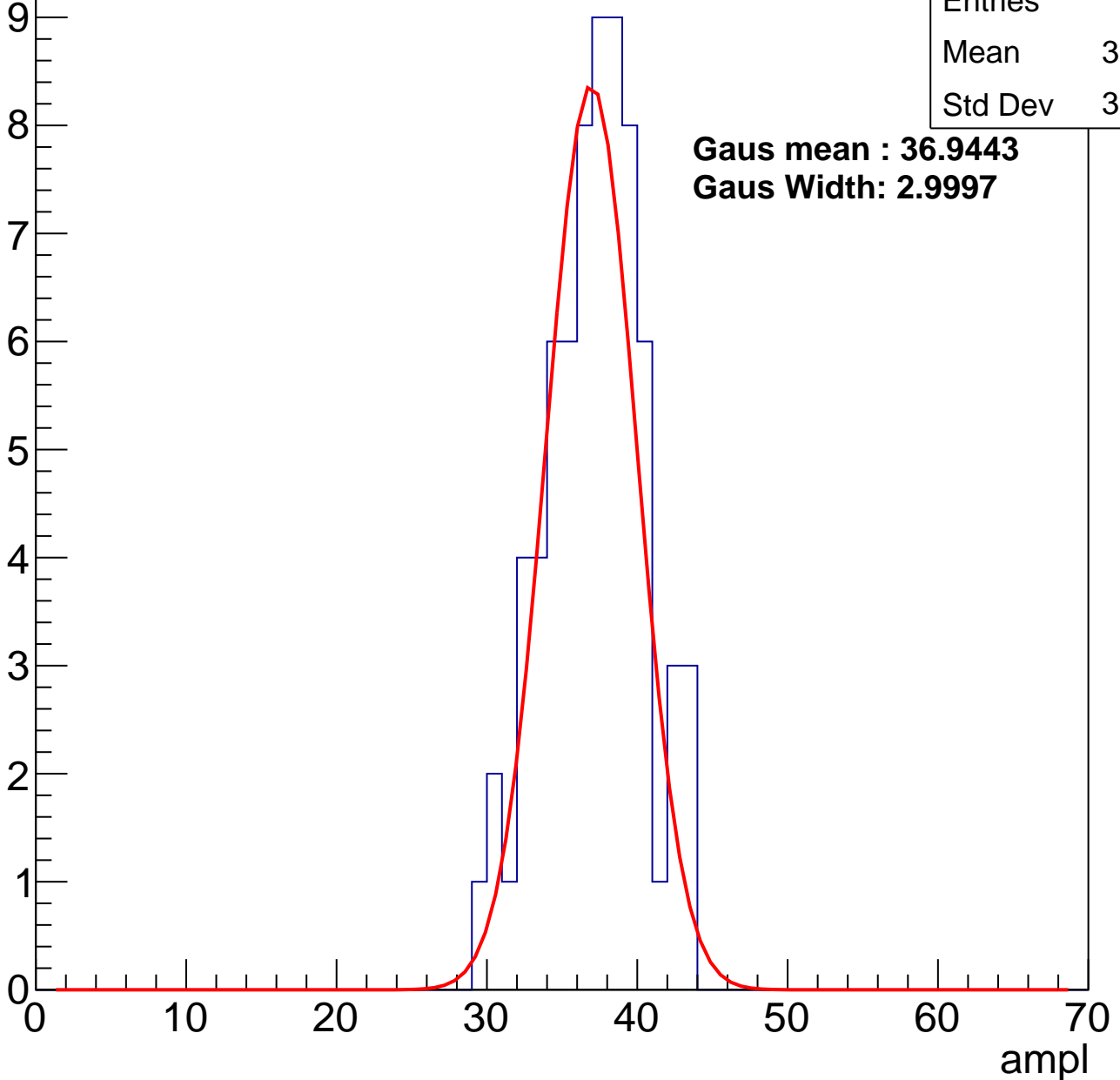
# B0L001S, U24-ch15, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	36.69
Std Dev	3.218

**Gaus mean : 36.9443**  
**Gaus Width: 2.9997**



# B0L001S, U24-ch15, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	76
Mean	43.92
Std Dev	3.716

**Gaus mean : 44.7974**

**Gaus Width: 3.6696**

10

8

6

4

2

0

0

10

20

30

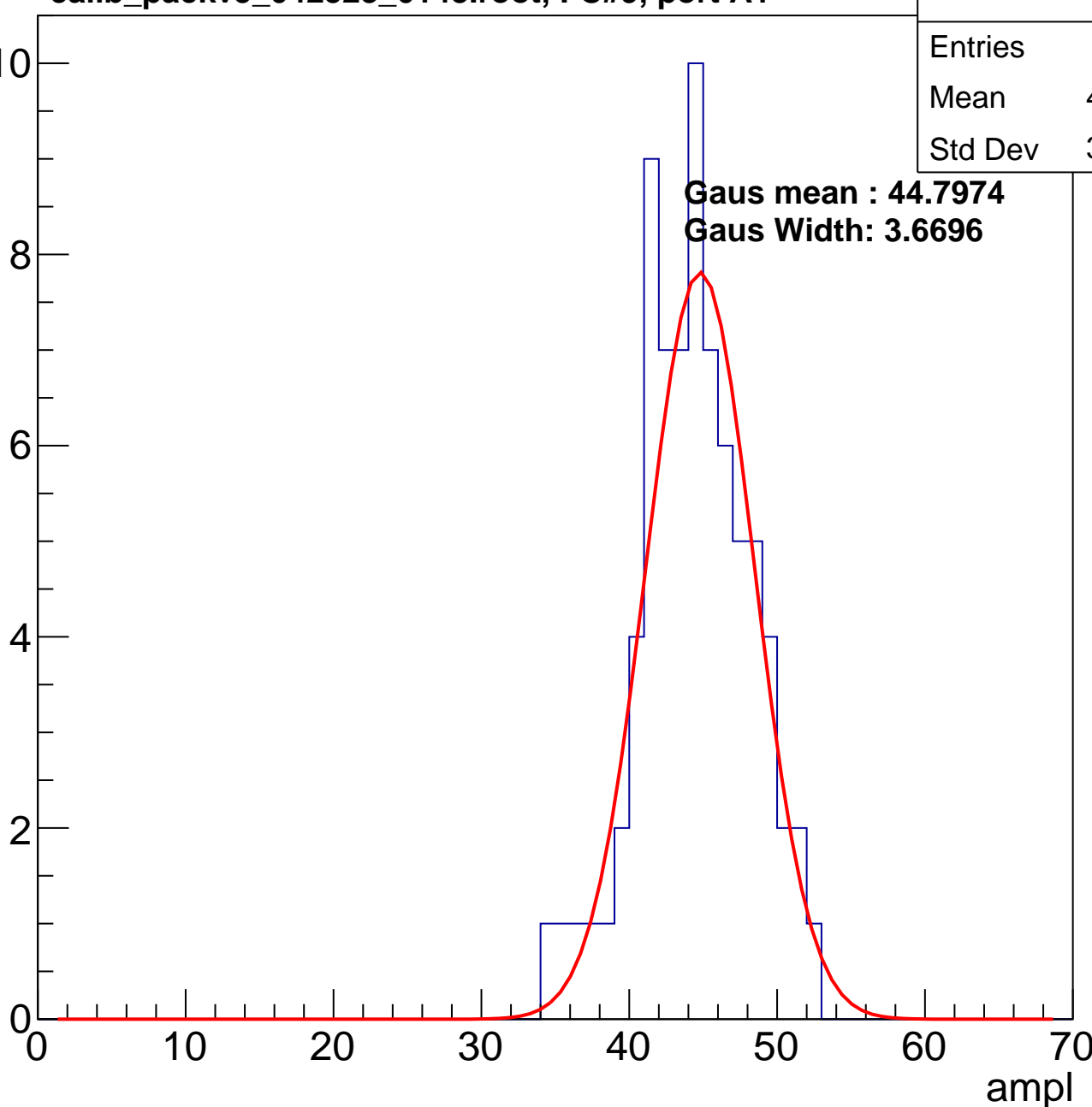
40

50

60

70

ampl

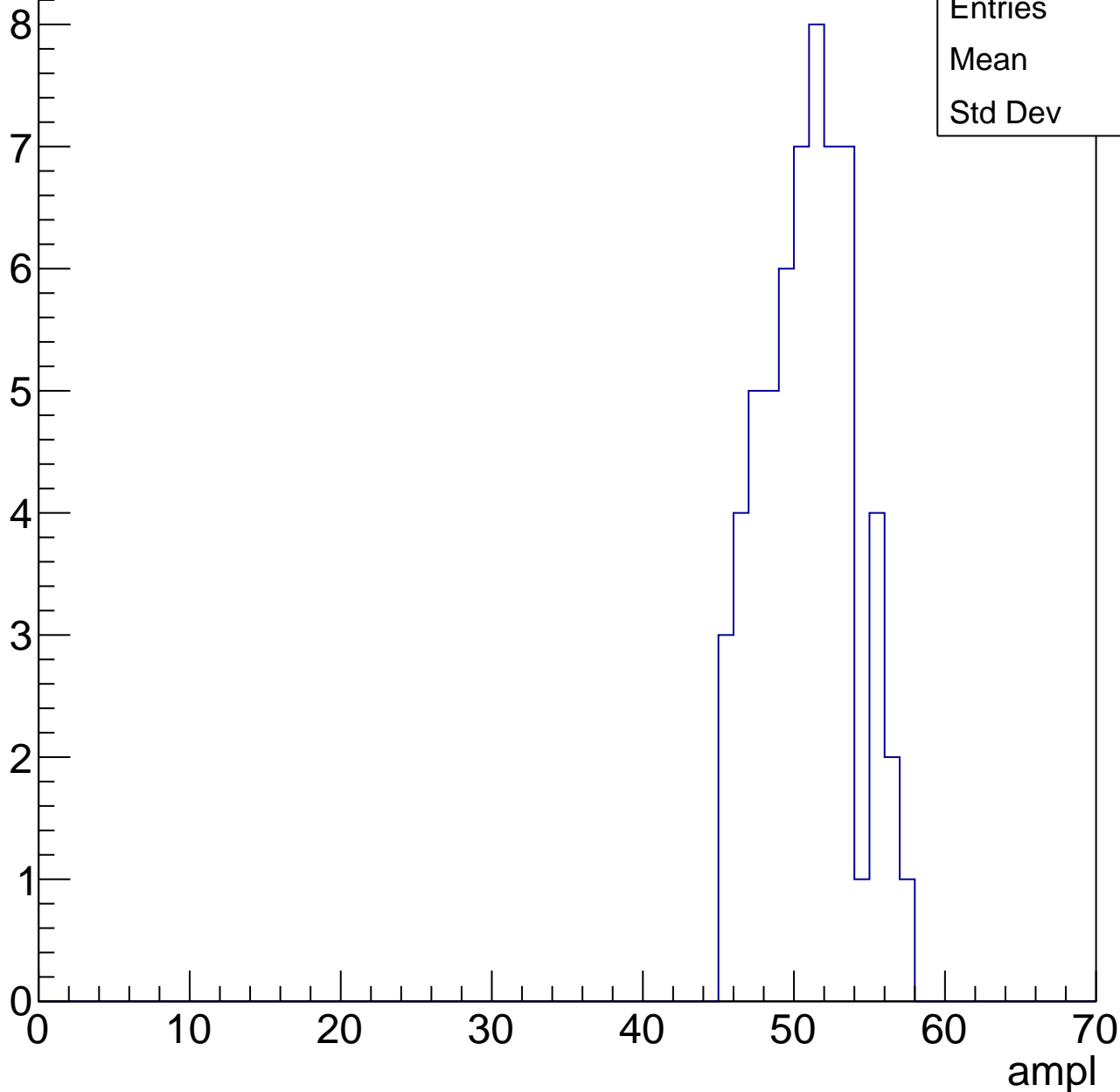


# B0L001S, U24-ch15, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	50.4
Std Dev	2.99

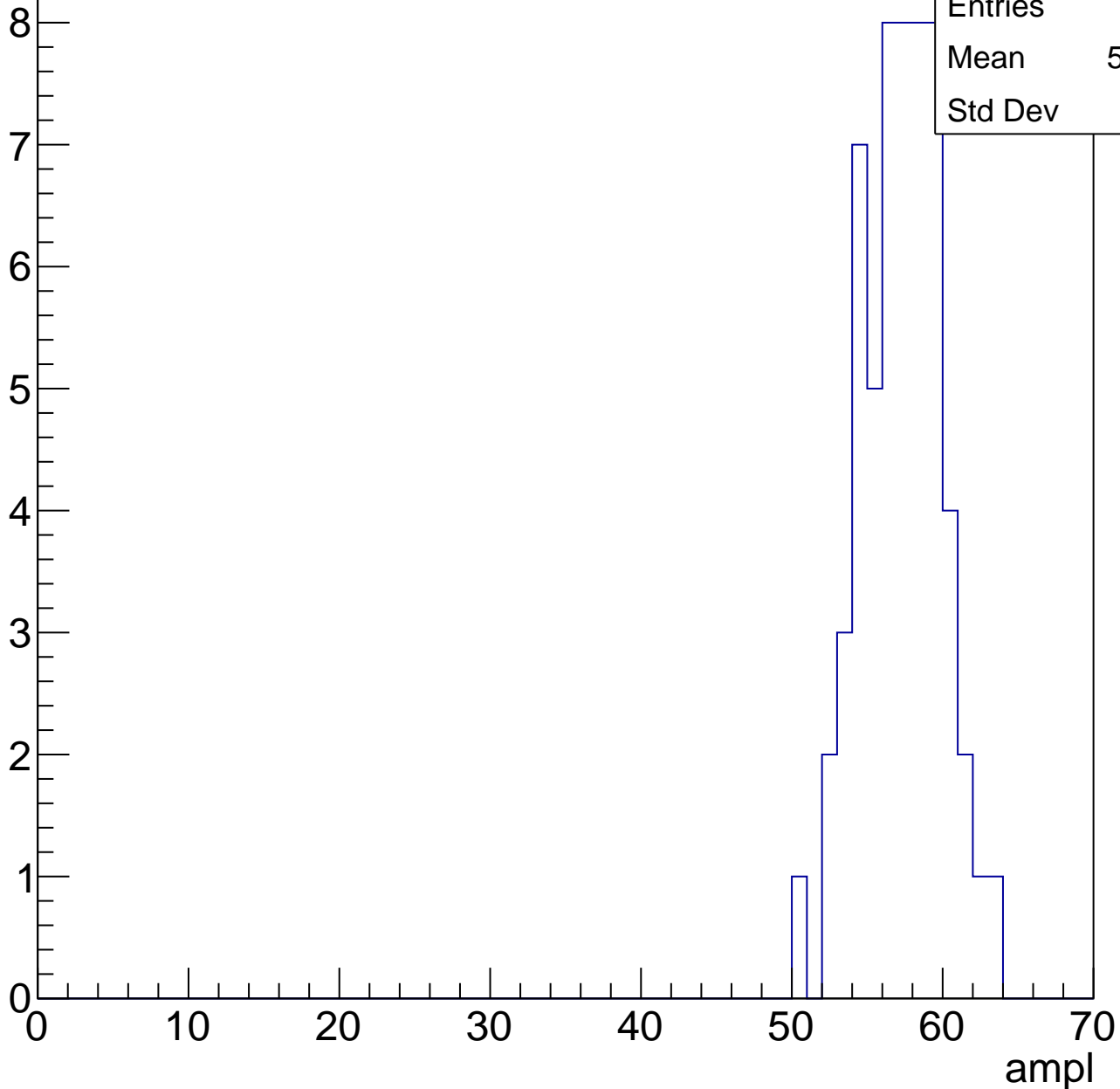


# B0L001S, U24-ch15, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	56.78
Std Dev	2.64

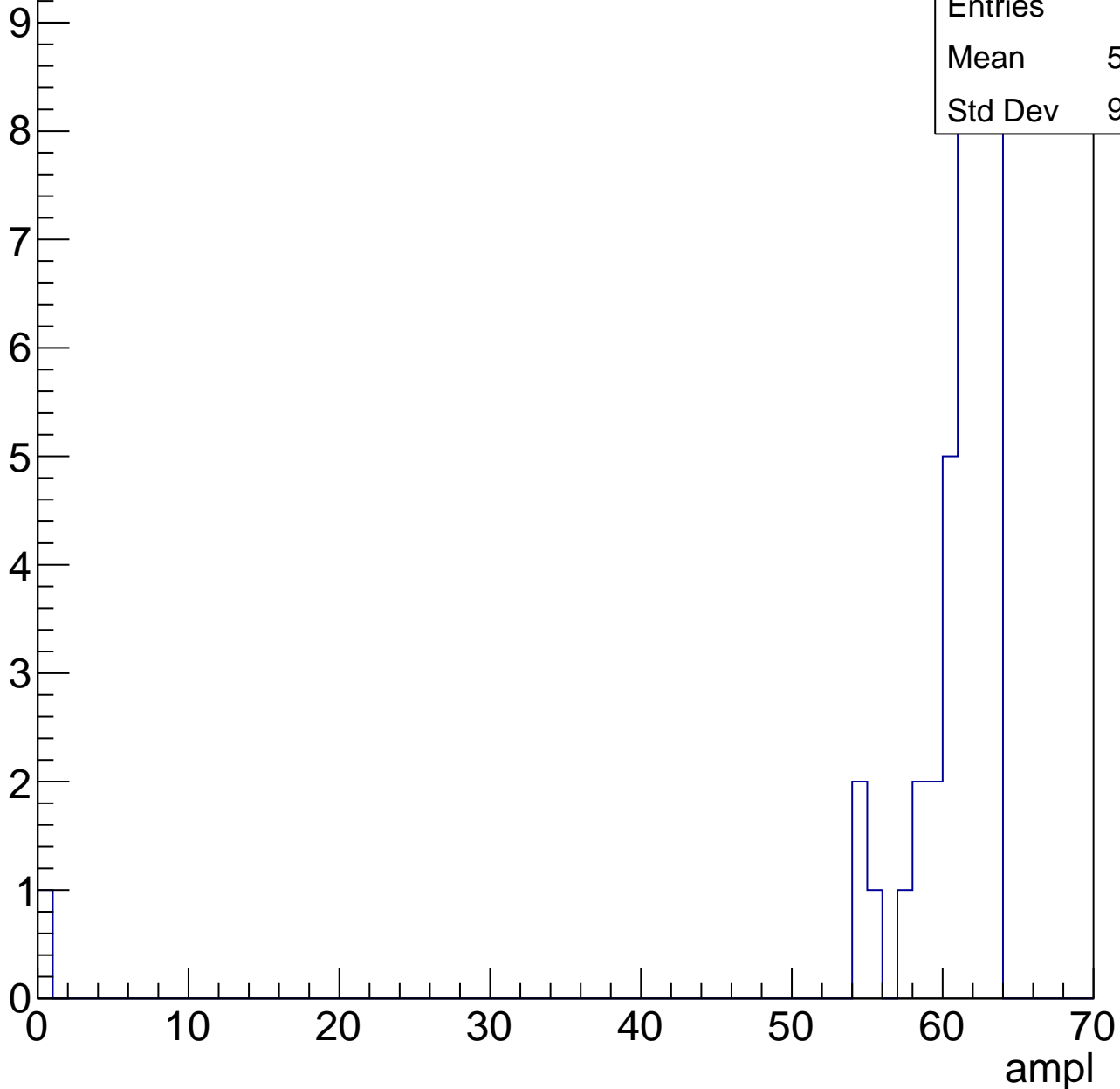


# B0L001S, U24-ch15, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	39
Mean	59.08
Std Dev	9.869



# B0L001S, U24-ch15, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch15, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U24-ch16, adc0

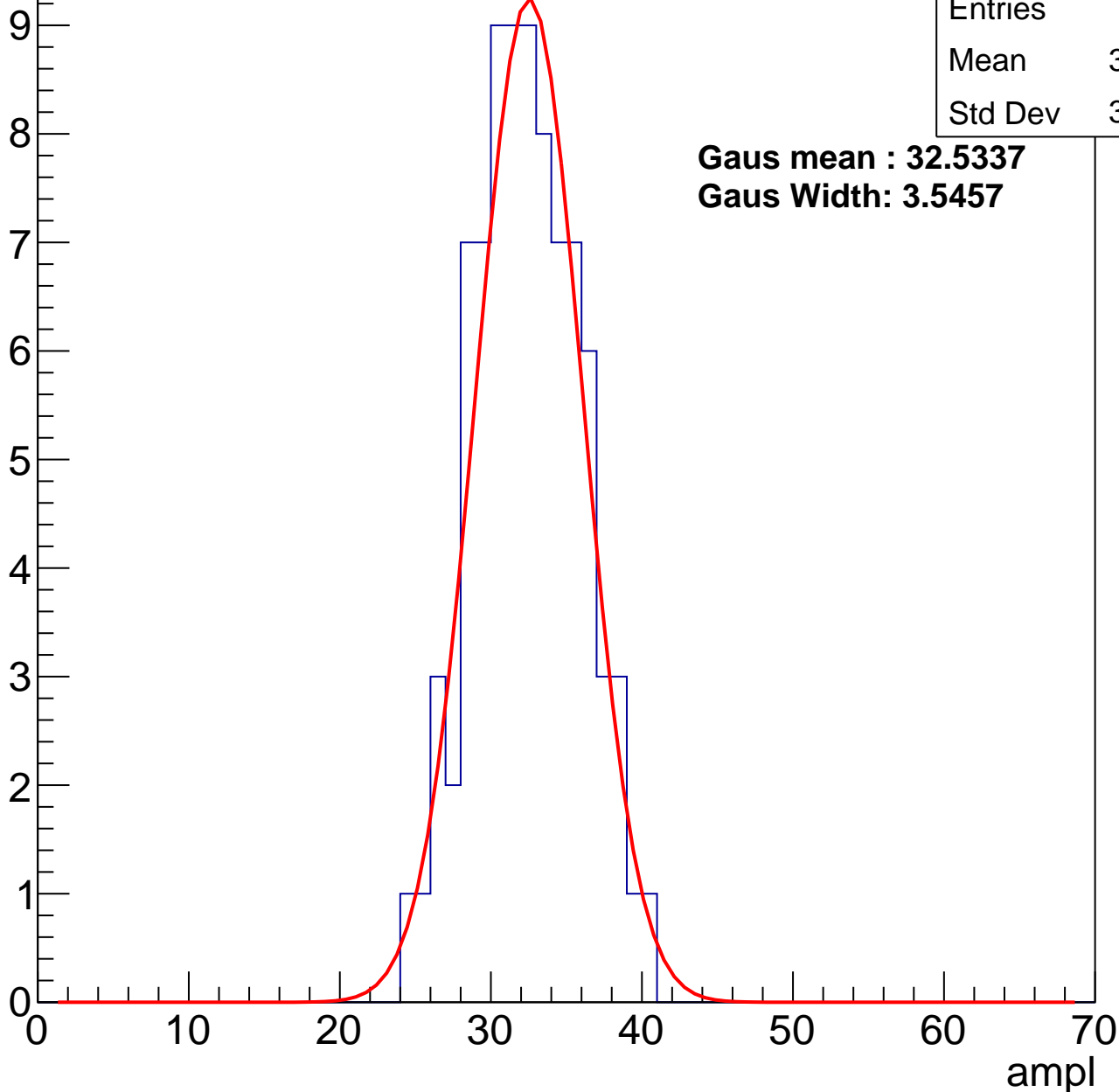
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	84
Mean	31.95
Std Dev	3.419

**Gaus mean : 32.5337**

**Gaus Width: 3.5457**



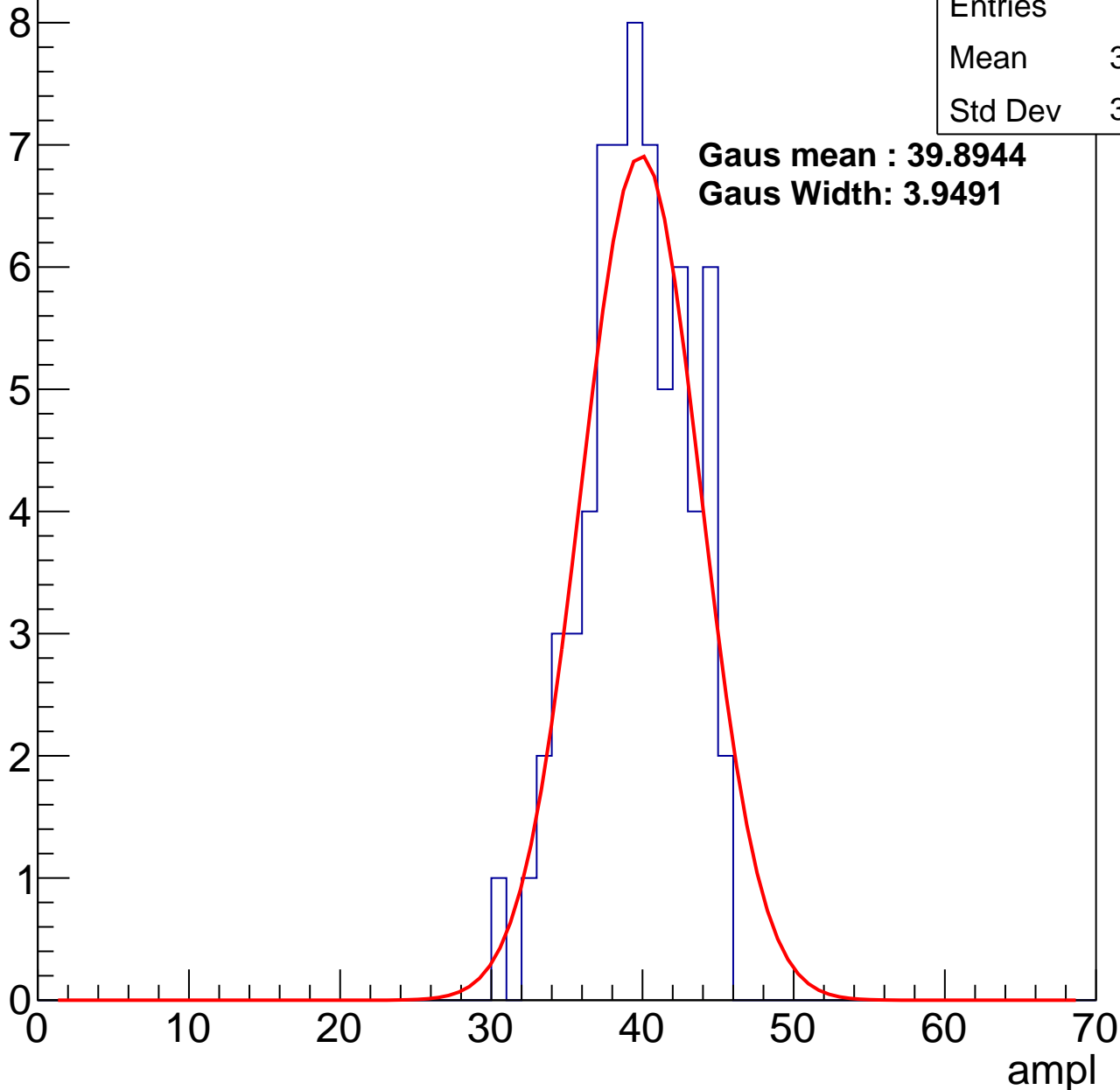
# B0L001S, U24-ch16, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	39.08
Std Dev	3.399

**Gaus mean : 39.8944**  
**Gaus Width: 3.9491**



# B0L001S, U24-ch16, adc2

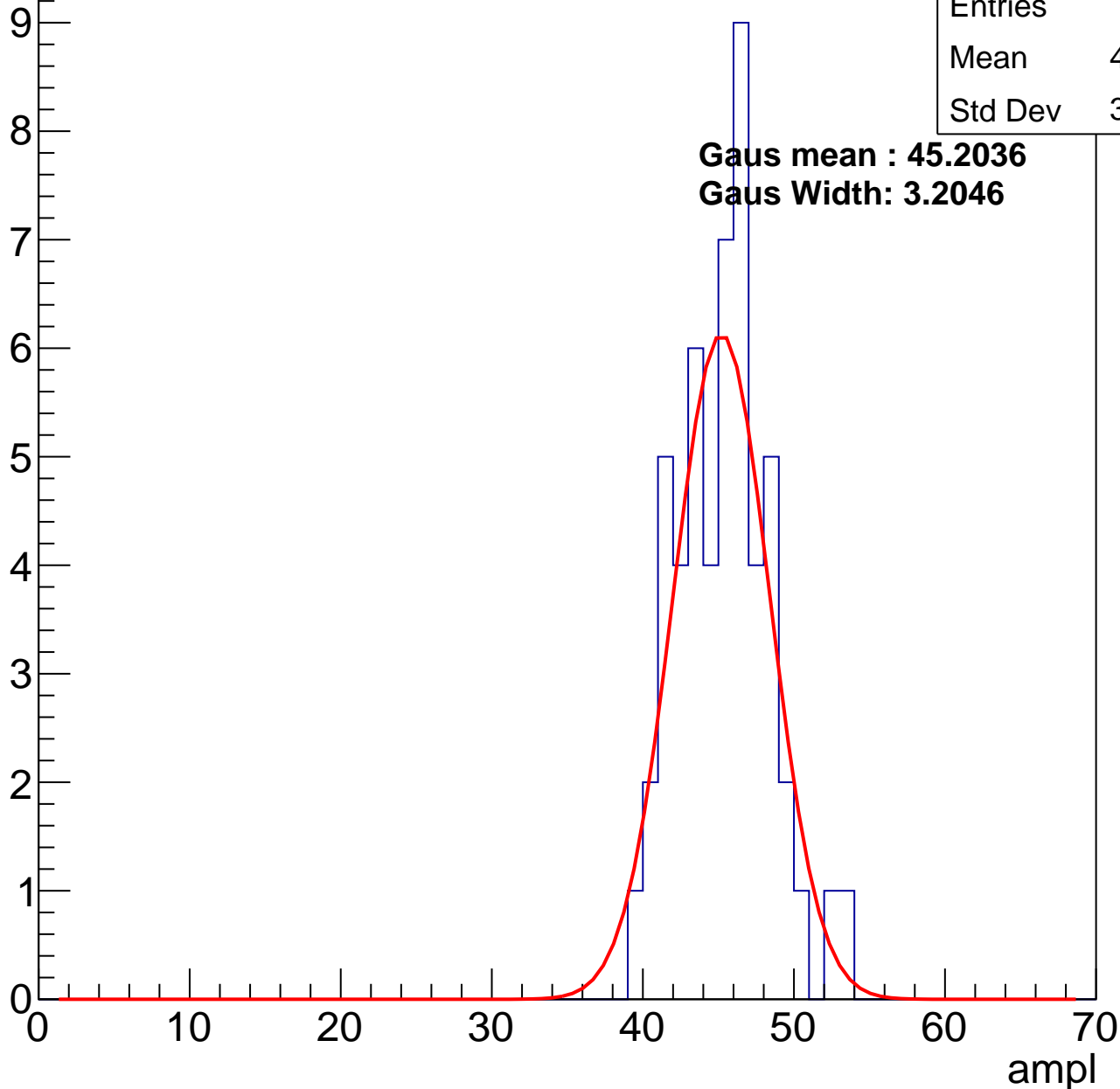
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	44.92
Std Dev	3.005

**Gaus mean : 45.2036**

**Gaus Width: 3.2046**



# B0L001S, U24-ch16, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	75
Mean	51.67
Std Dev	3.275

Entry

10

8

6

4

2

0

0

10

20

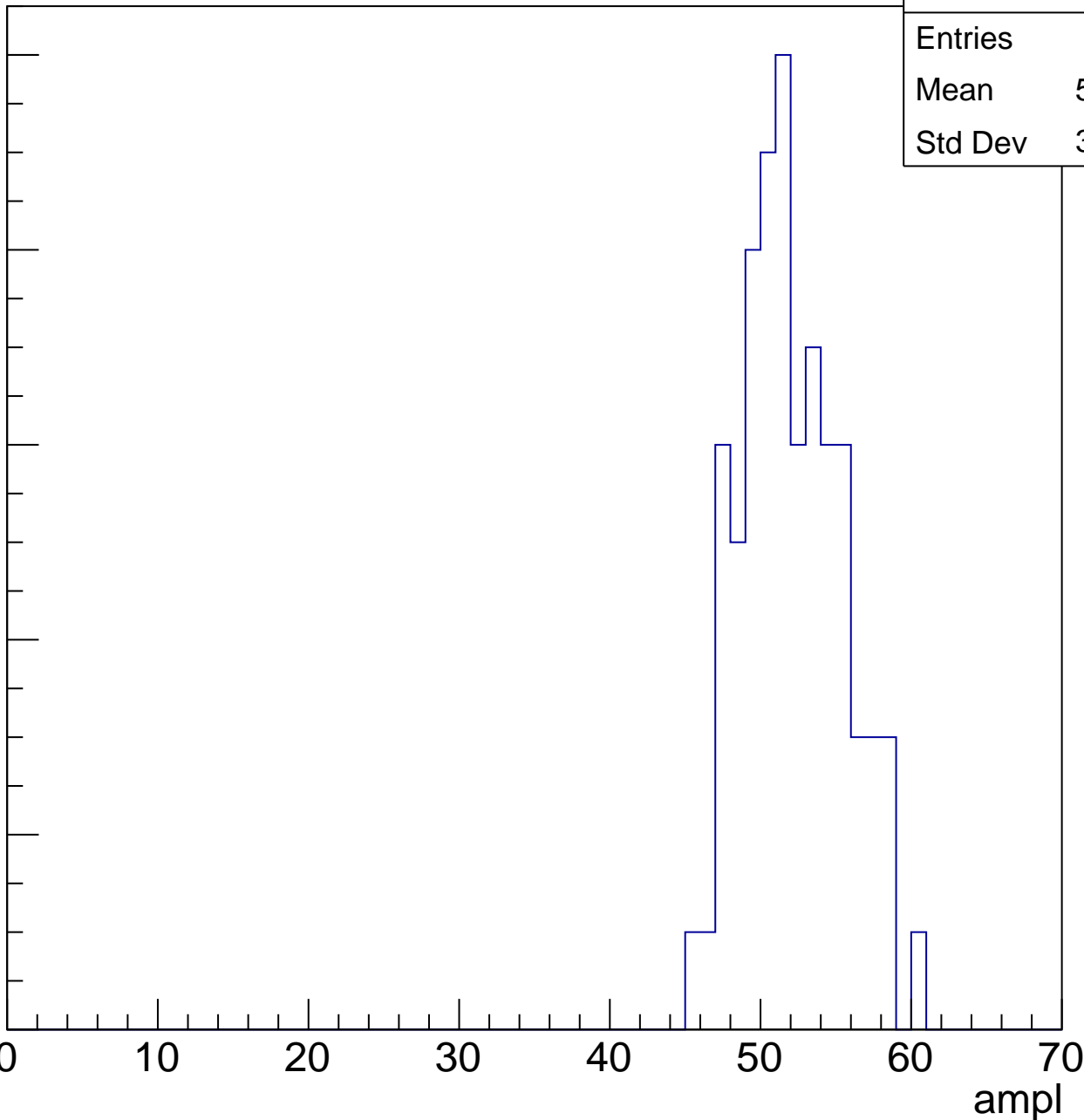
30

40

50

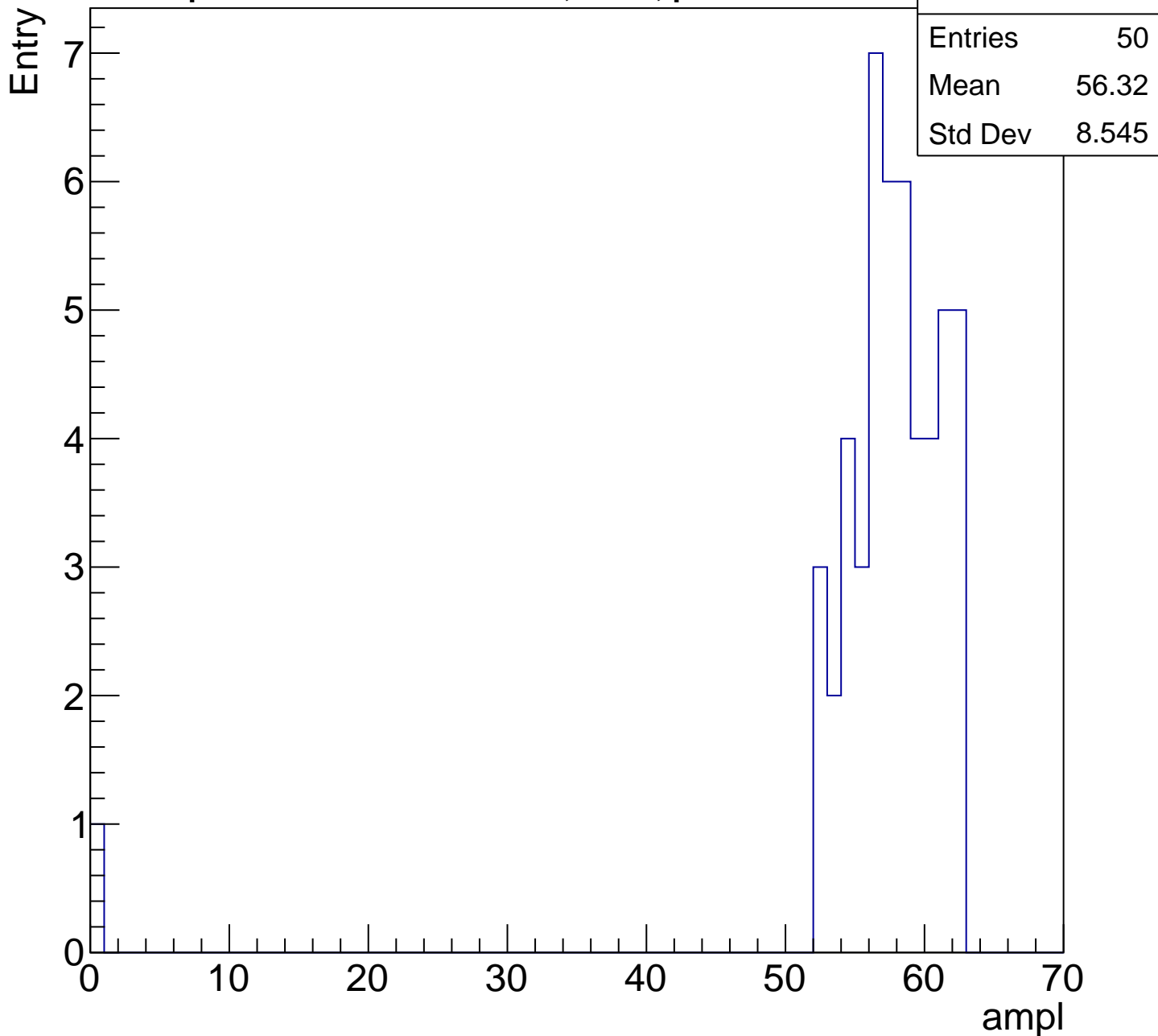
60

ampl



# B0L001S, U24-ch16, adc4

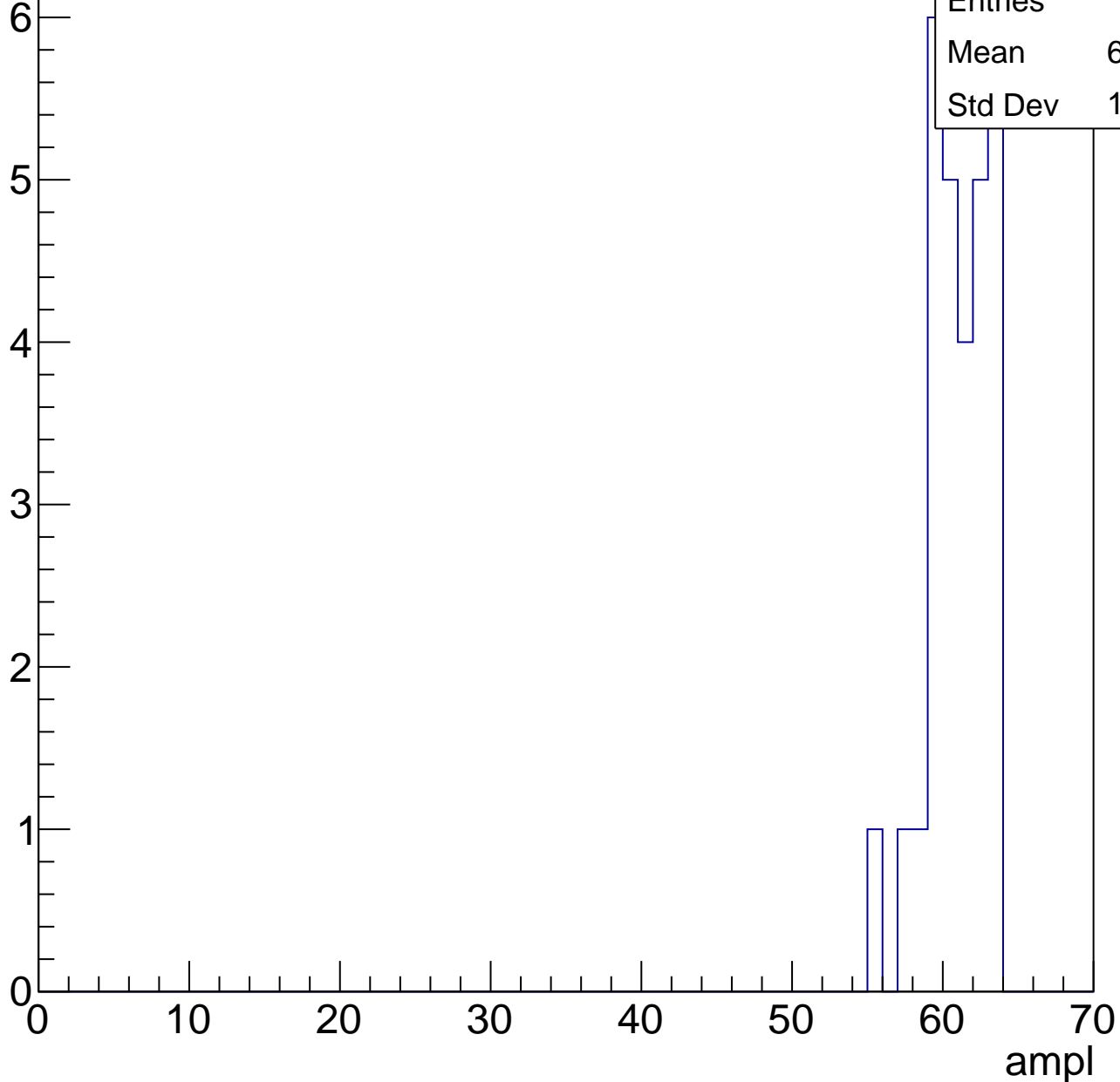
calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U24-ch16, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

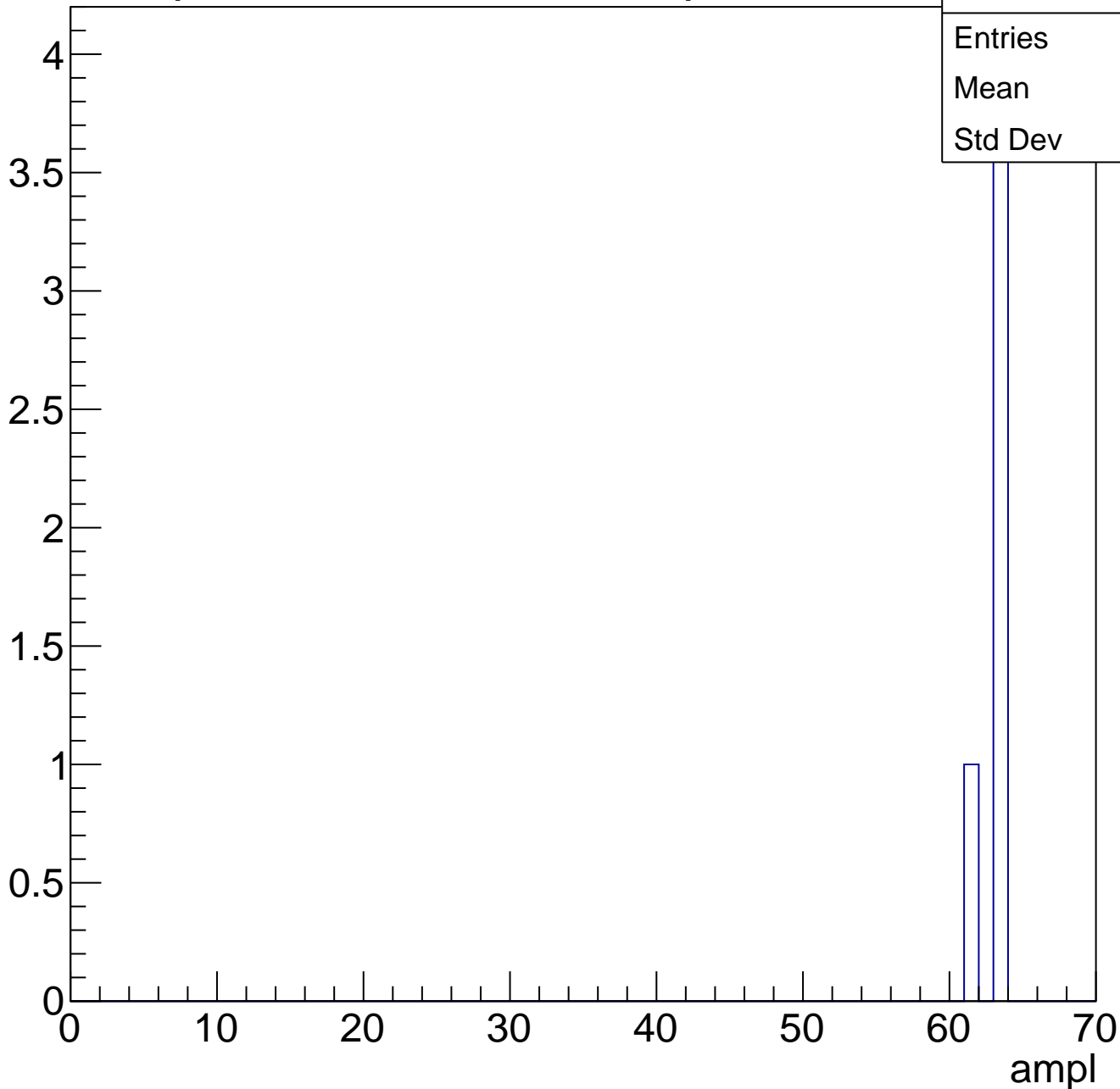
Entry



# B0L001S, U24-ch16, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch16, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U24-ch17, adc0

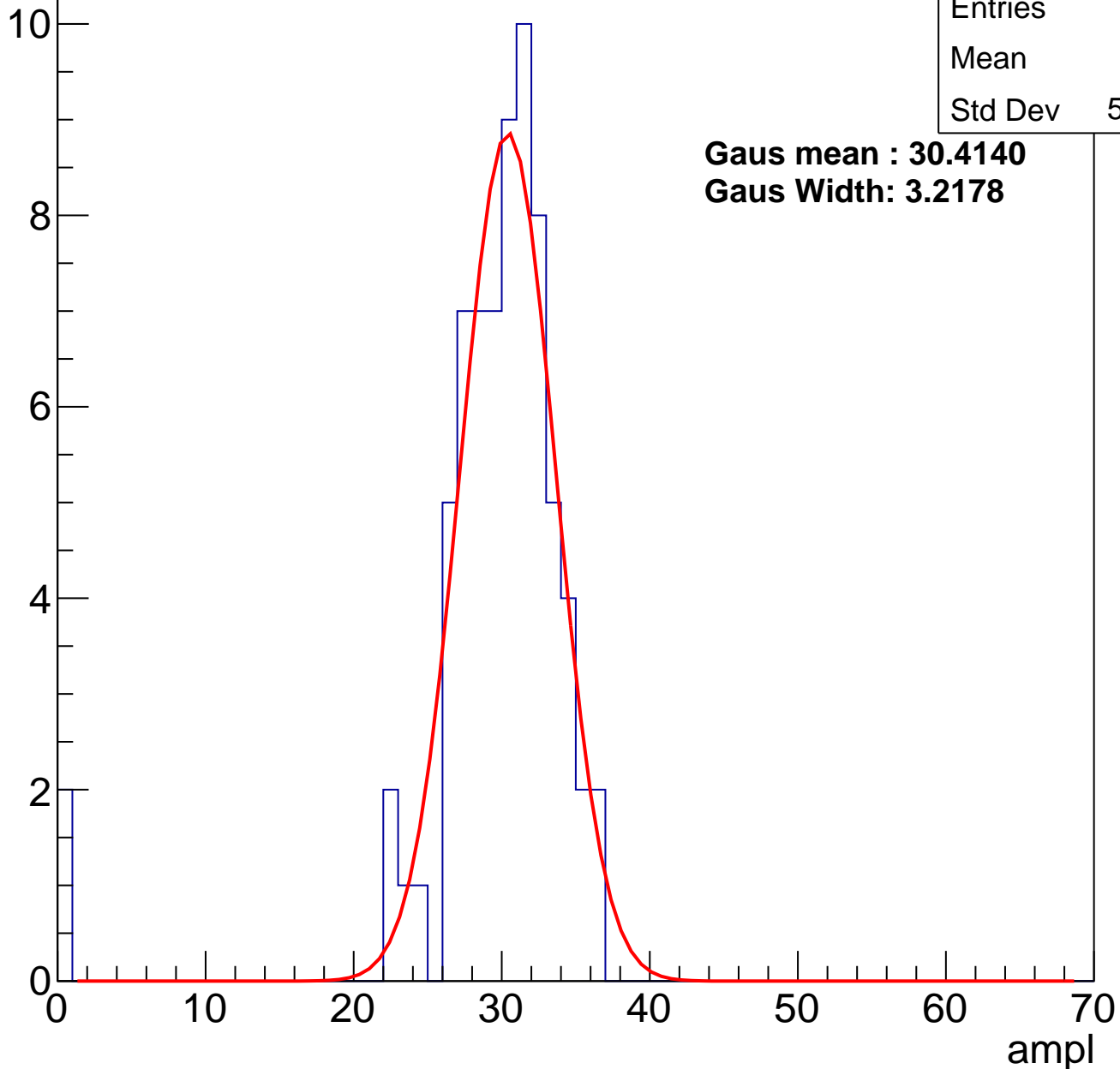
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	72
Mean	29
Std Dev	5.764

**Gaus mean : 30.4140**

**Gaus Width: 3.2178**

Entry



# B0L001S, U24-ch17, adc1

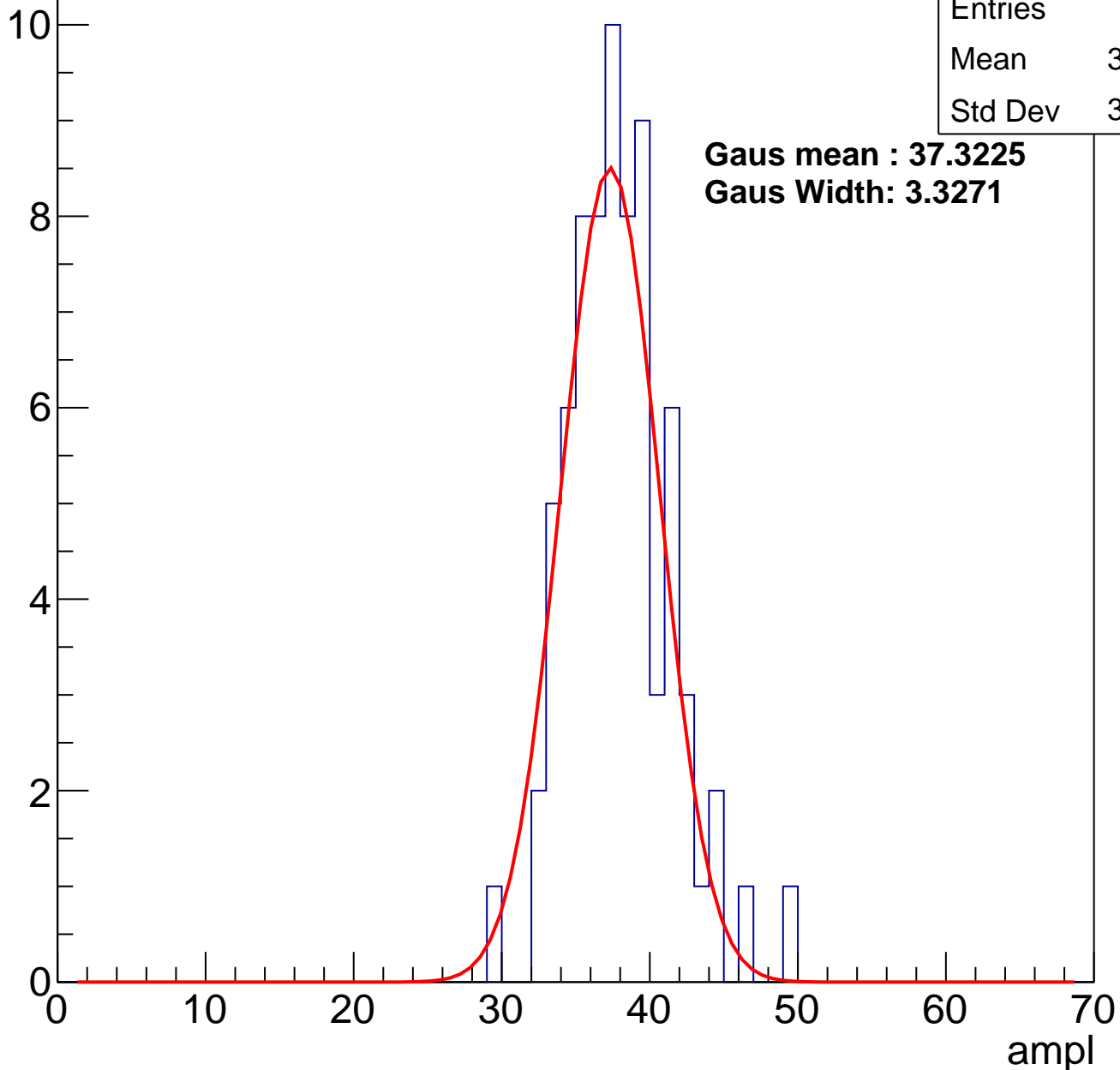
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	74
Mean	37.47
Std Dev	3.434

**Gaus mean : 37.3225**

**Gaus Width: 3.3271**

Entry



# B0L001S, U24-ch17, adc2

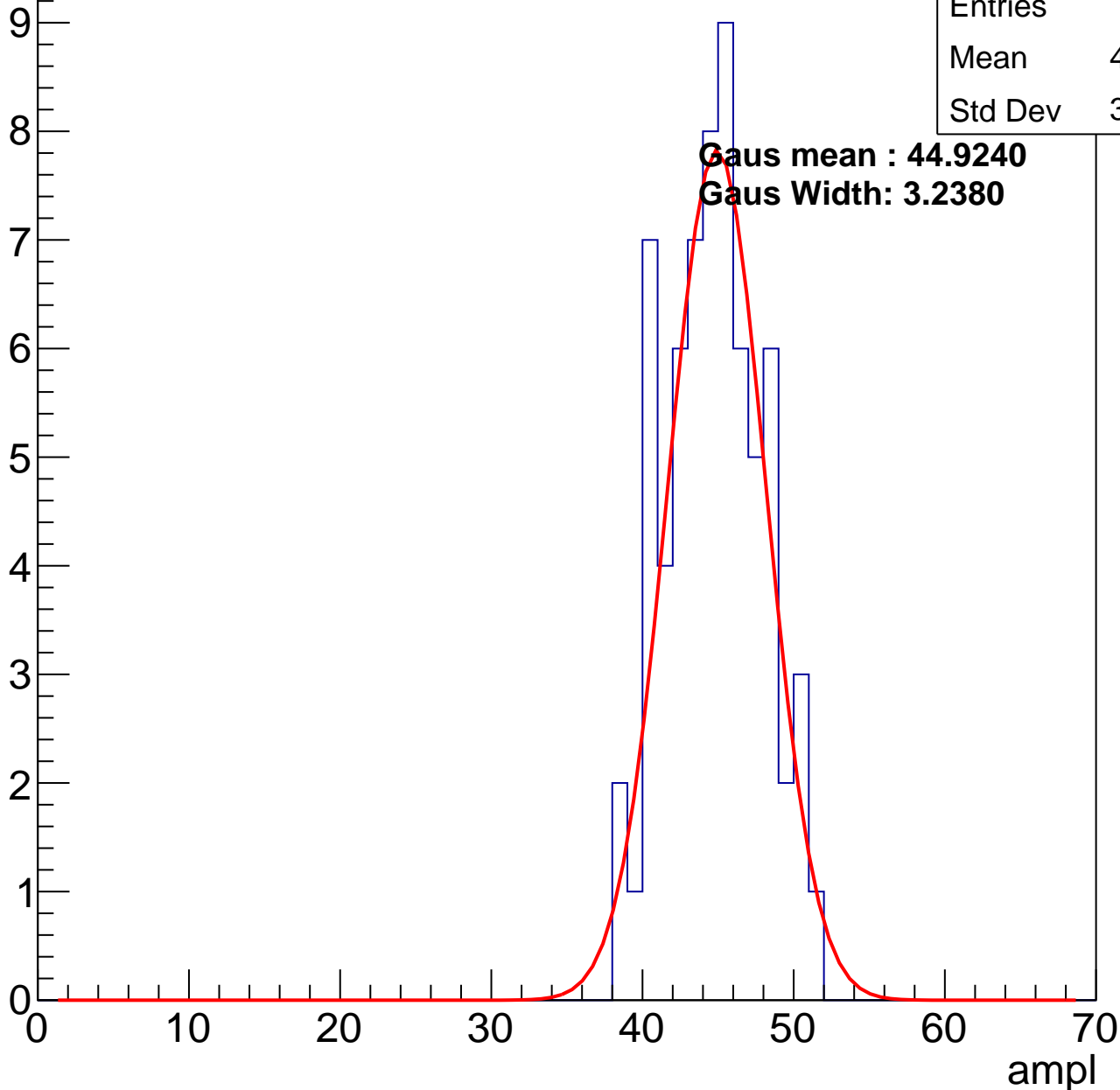
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	44.28
Std Dev	3.119

**Gaus mean : 44.9240**

**Gaus Width: 3.2380**

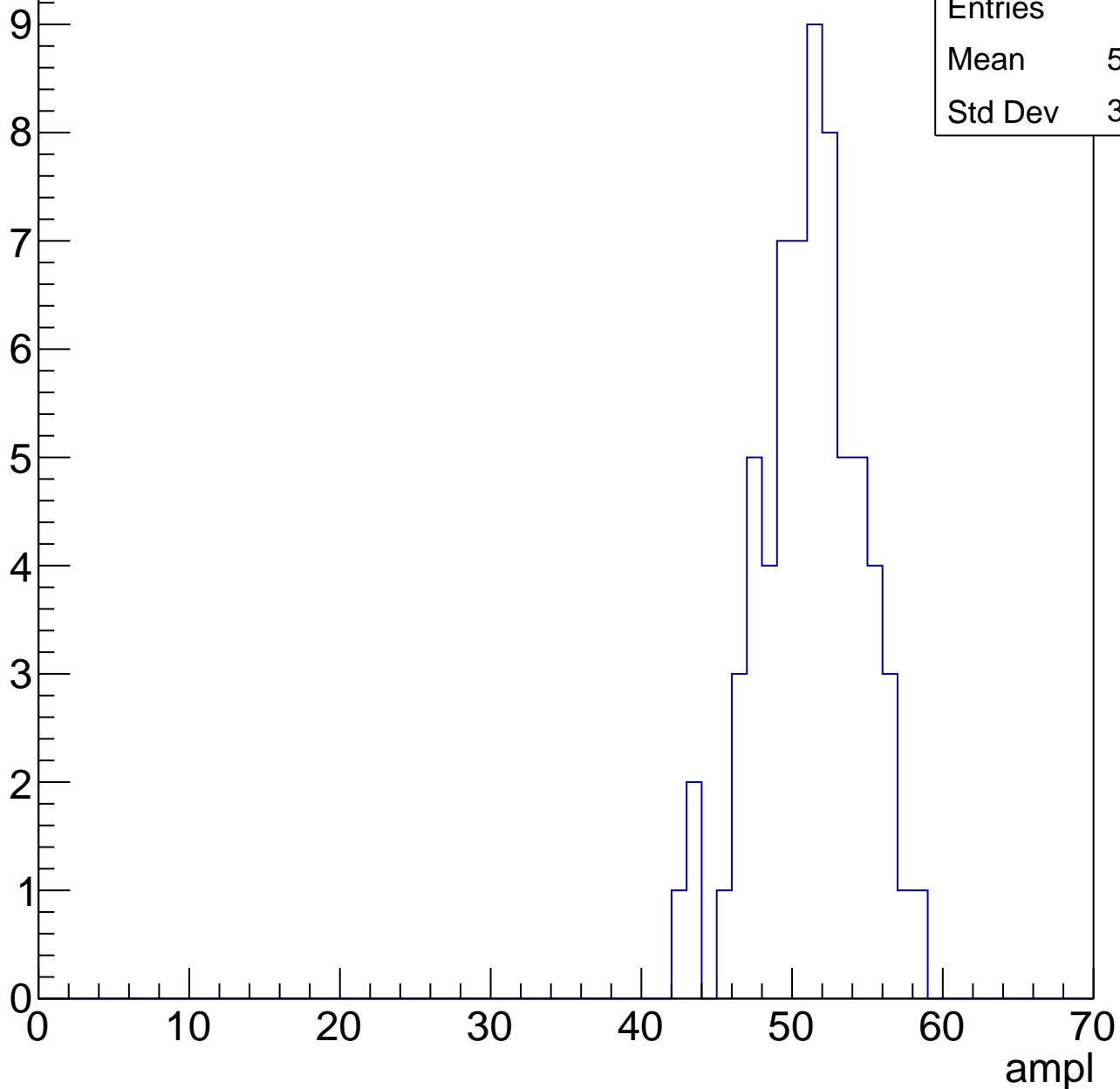


# B0L001S, U24-ch17, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

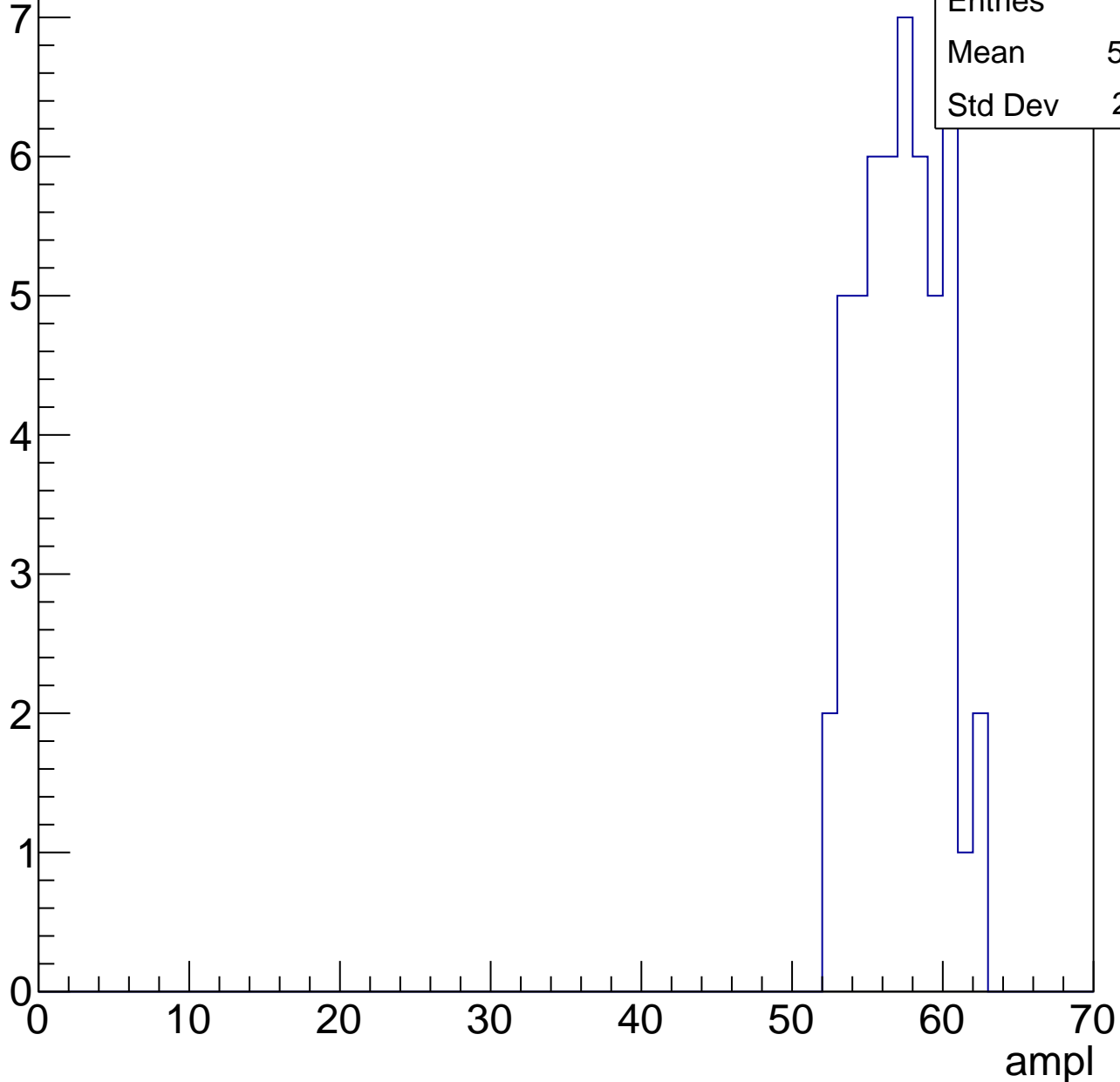
Entries	66
Mean	50.67
Std Dev	3.395



# B0L001S, U24-ch17, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

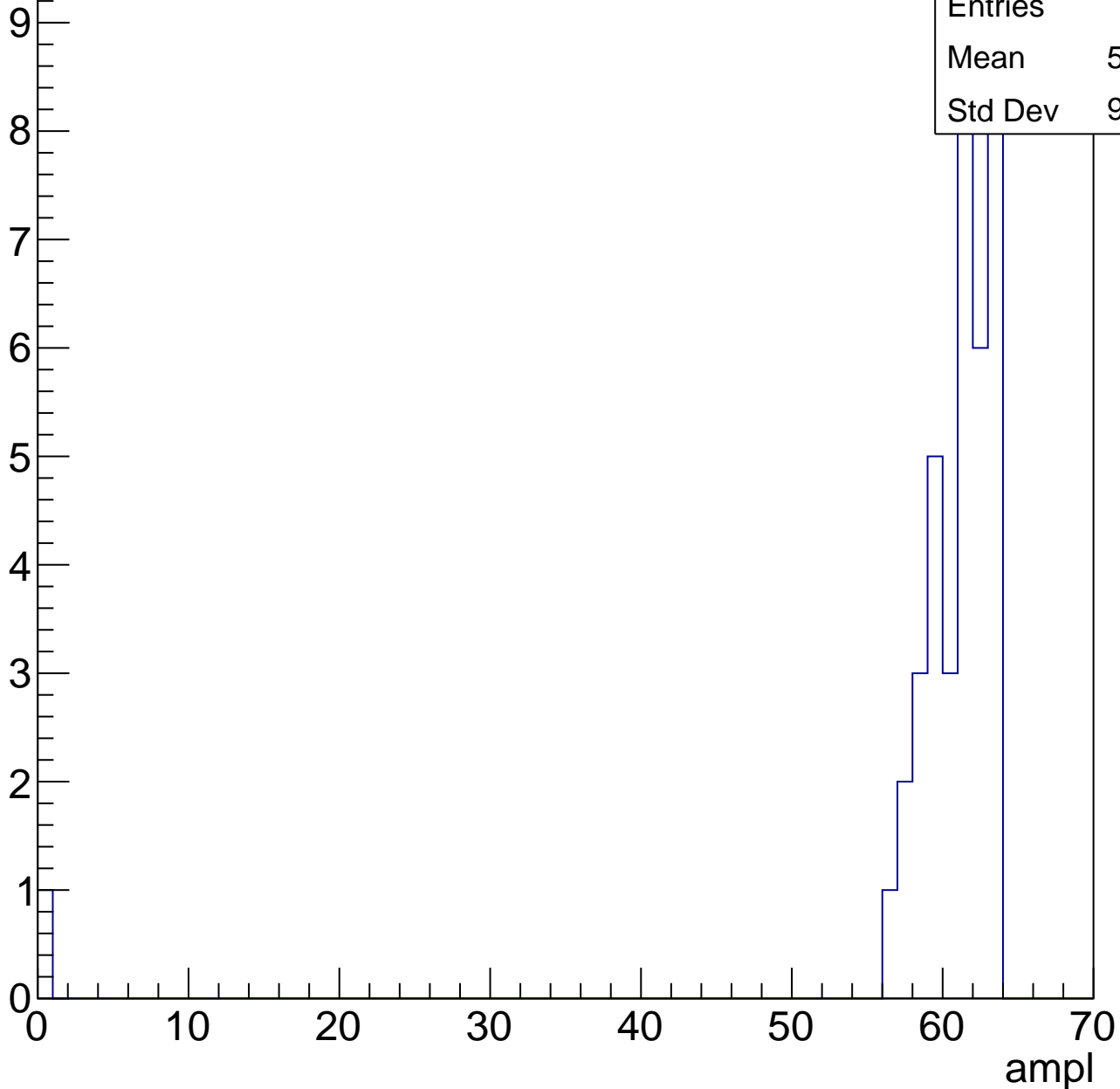


# B0L001S, U24-ch17, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	39
Mean	59.15
Std Dev	9.789



# B0L001S, U24-ch17, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.33
Std Dev	0.4714

ampl

0 10 20 30 40 50 60 70



# B0L001S, U24-ch17, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U24-ch18, adc0

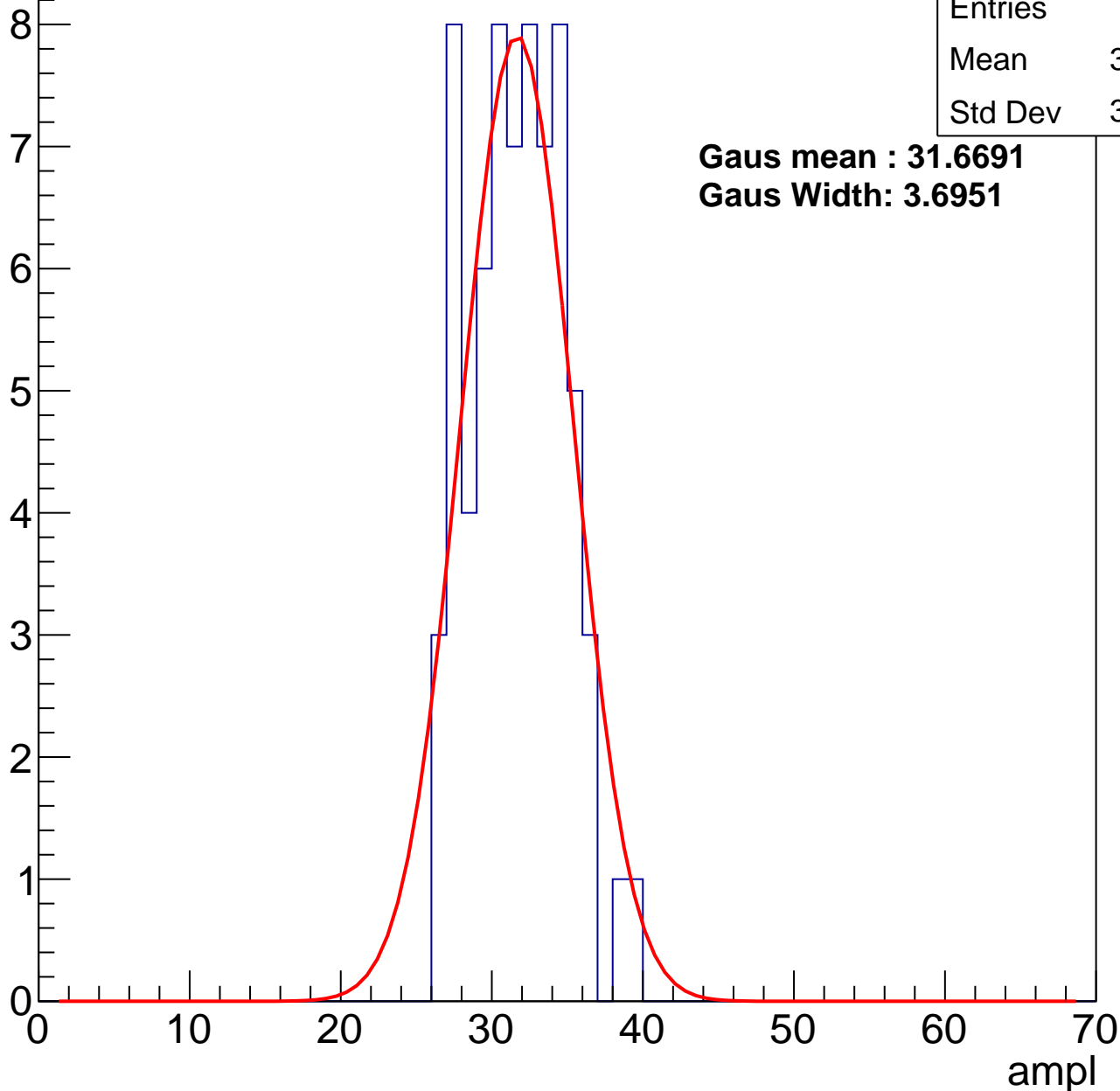
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	31.25
Std Dev	3.052

**Gaus mean : 31.6691**

**Gaus Width: 3.6951**



# B0L001S, U24-ch18, adc1

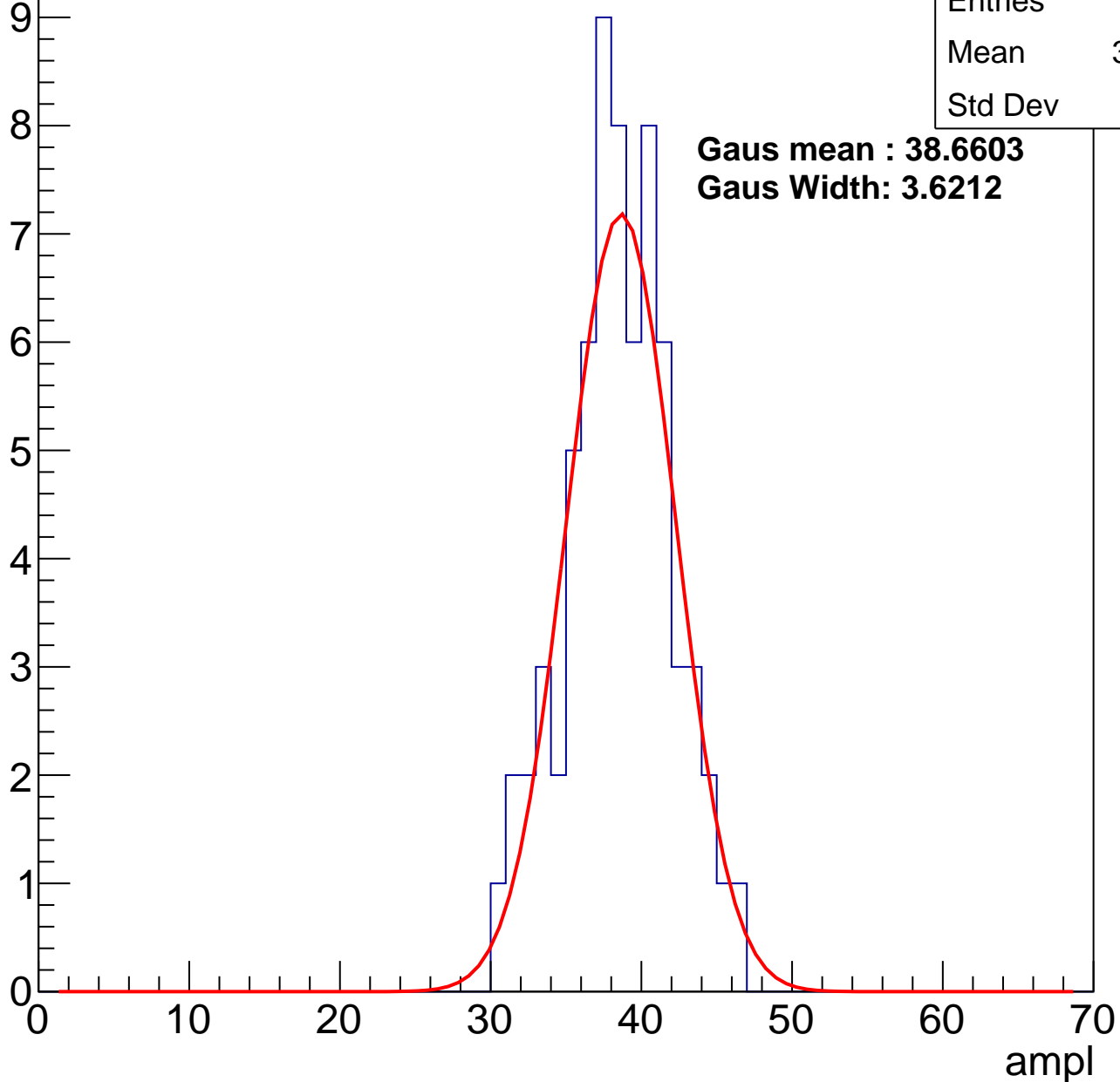
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	38.01
Std Dev	3.47

**Gaus mean : 38.6603**

**Gaus Width: 3.6212**

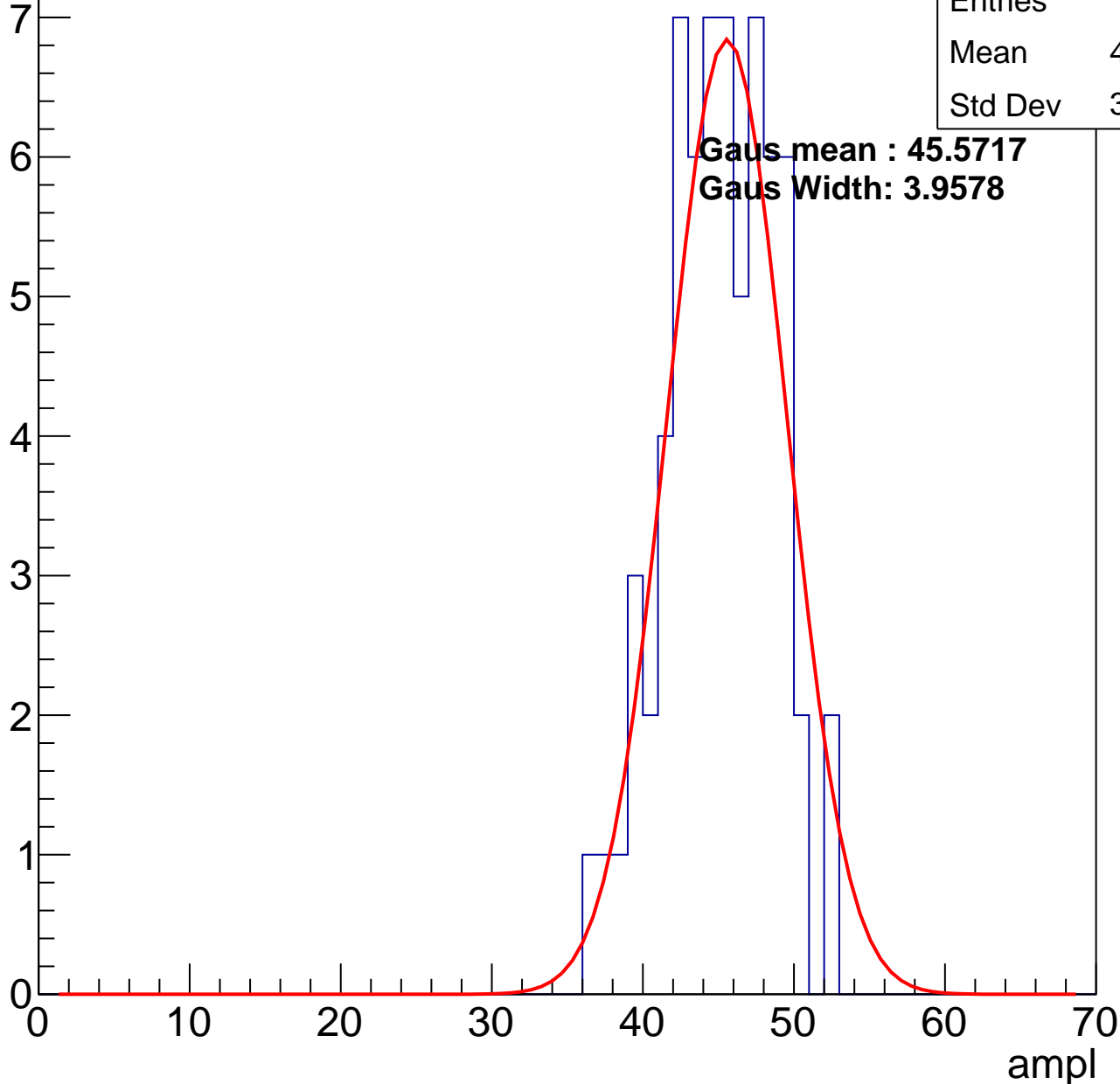


# B0L001S, U24-ch18, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	44.66
Std Dev	3.526

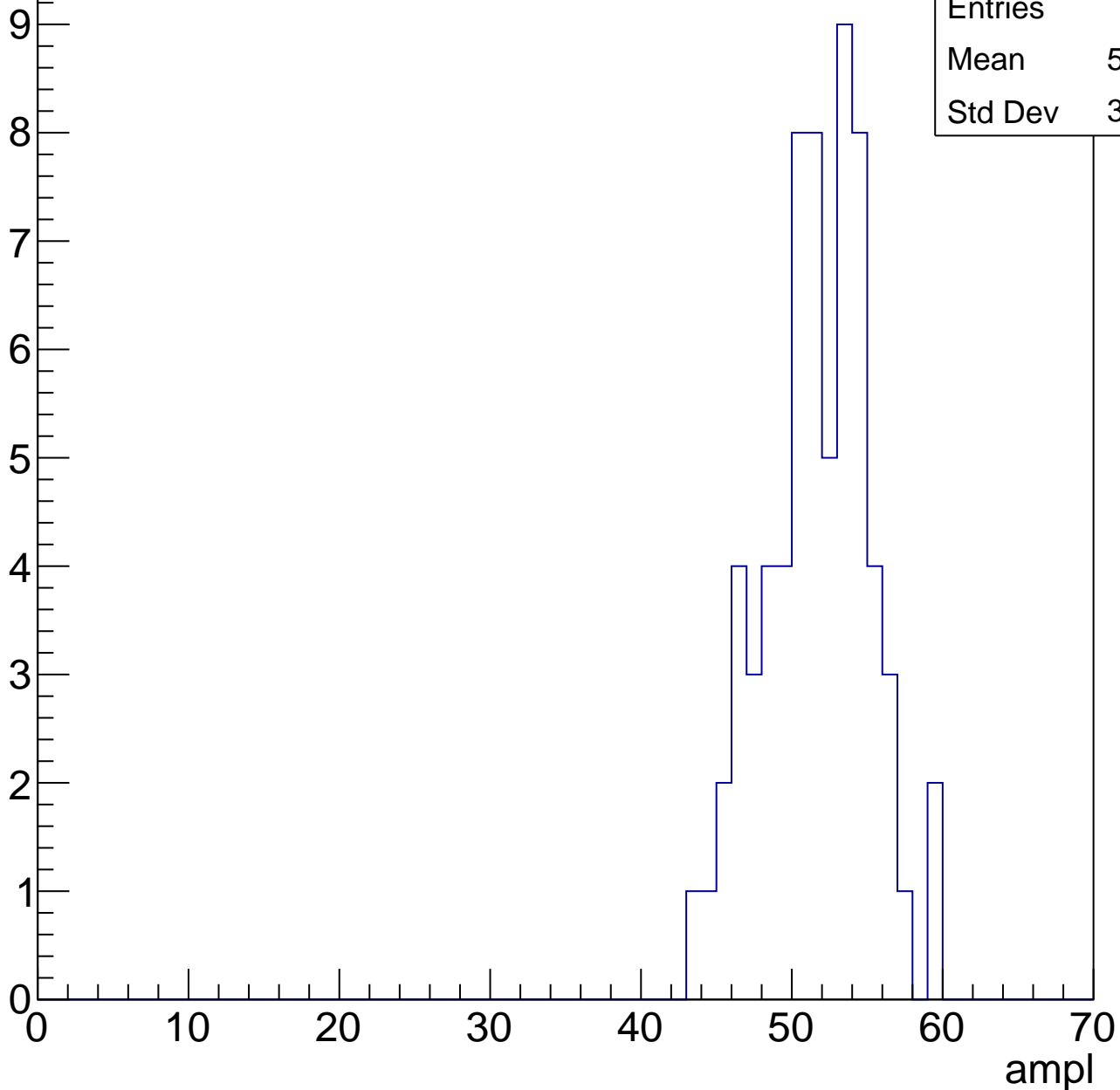


# B0L001S, U24-ch18, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	51.19
Std Dev	3.469



# B0L001S, U24-ch18, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	57.13
Std Dev	2.703

10

8

6

4

2

0

0

10

20

30

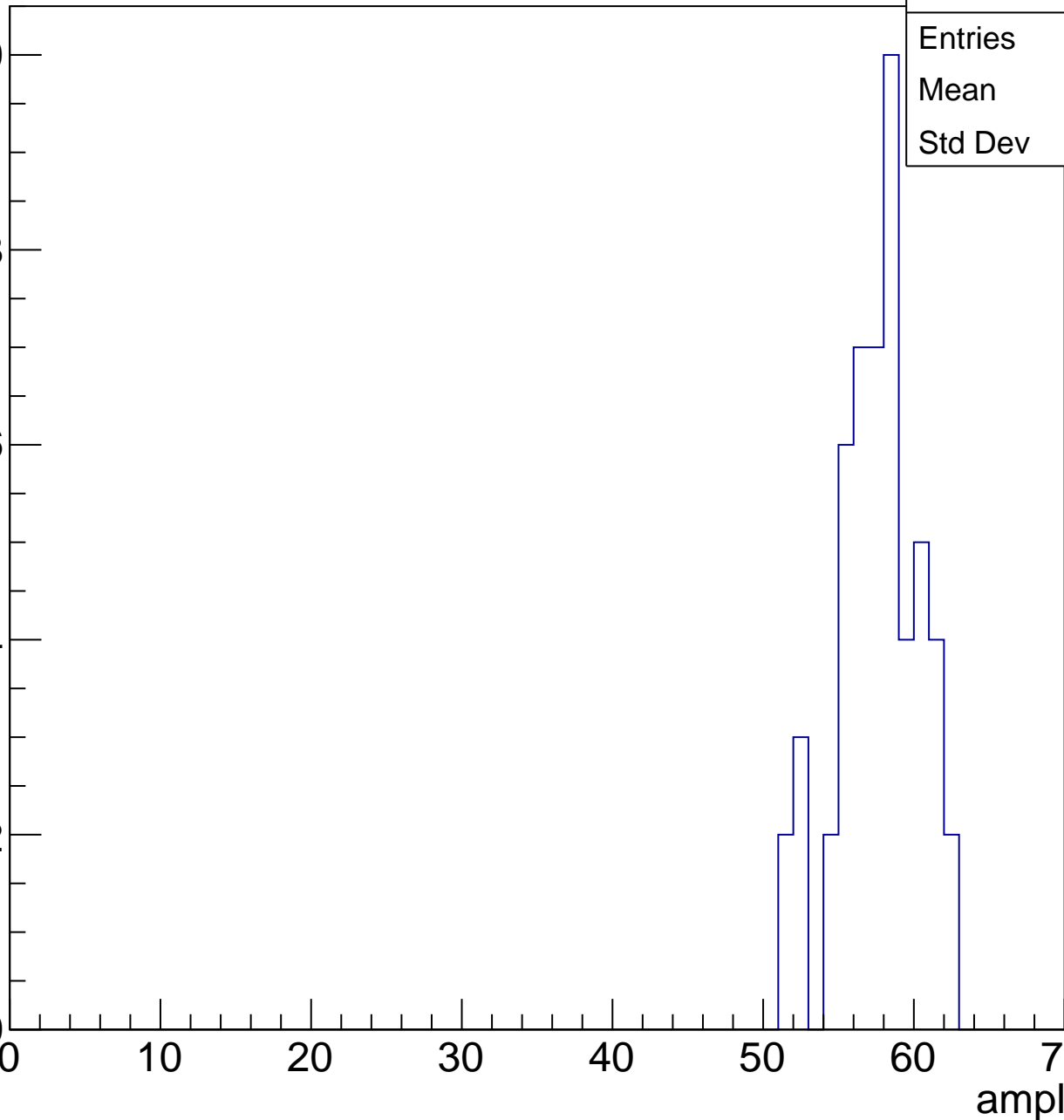
40

50

60

70

ampl

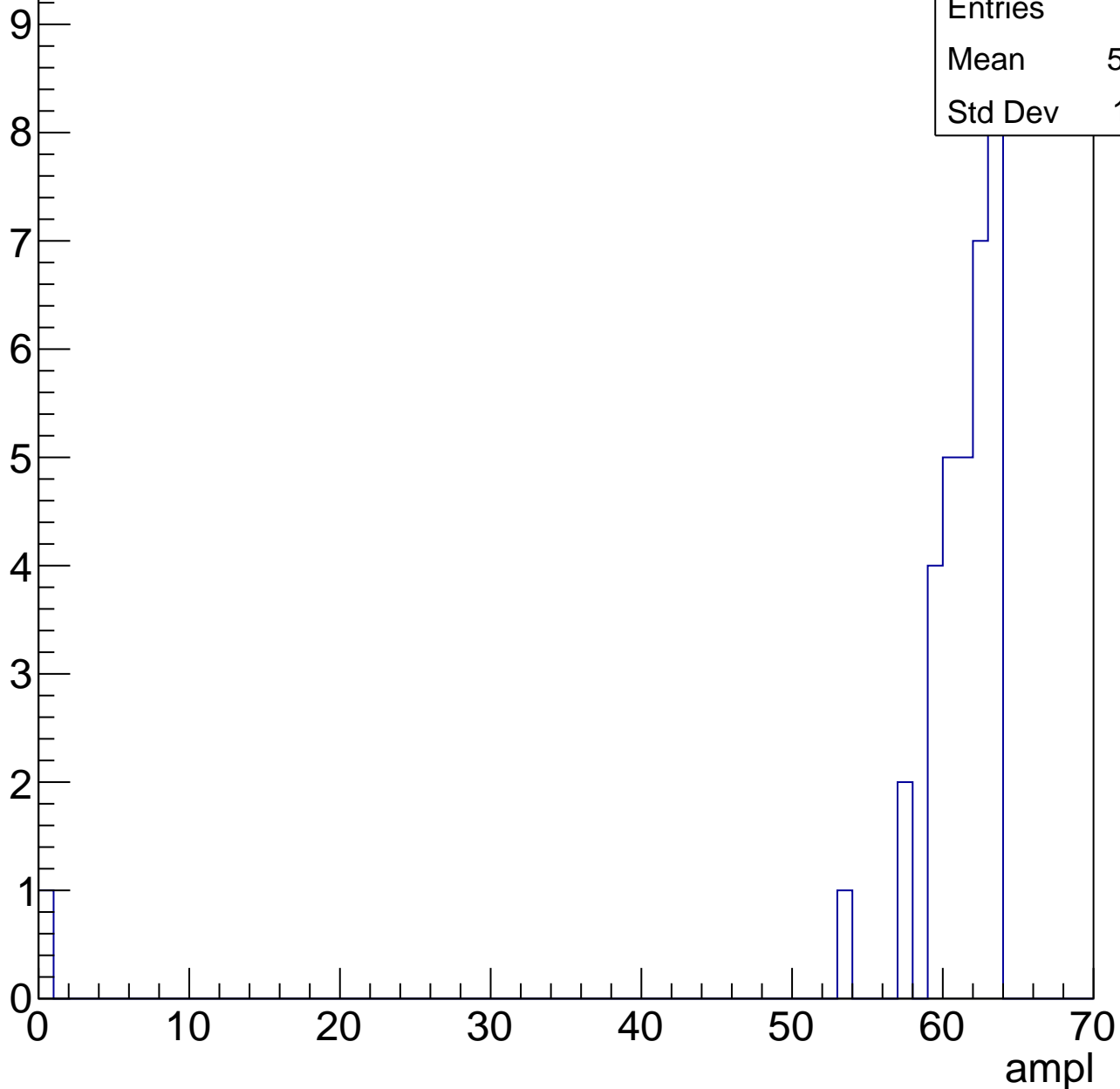


# B0L001S, U24-ch18, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	34
Mean	59.09
Std Dev	10.51



# B0L001S, U24-ch18, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch18, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U24-ch19, adc0

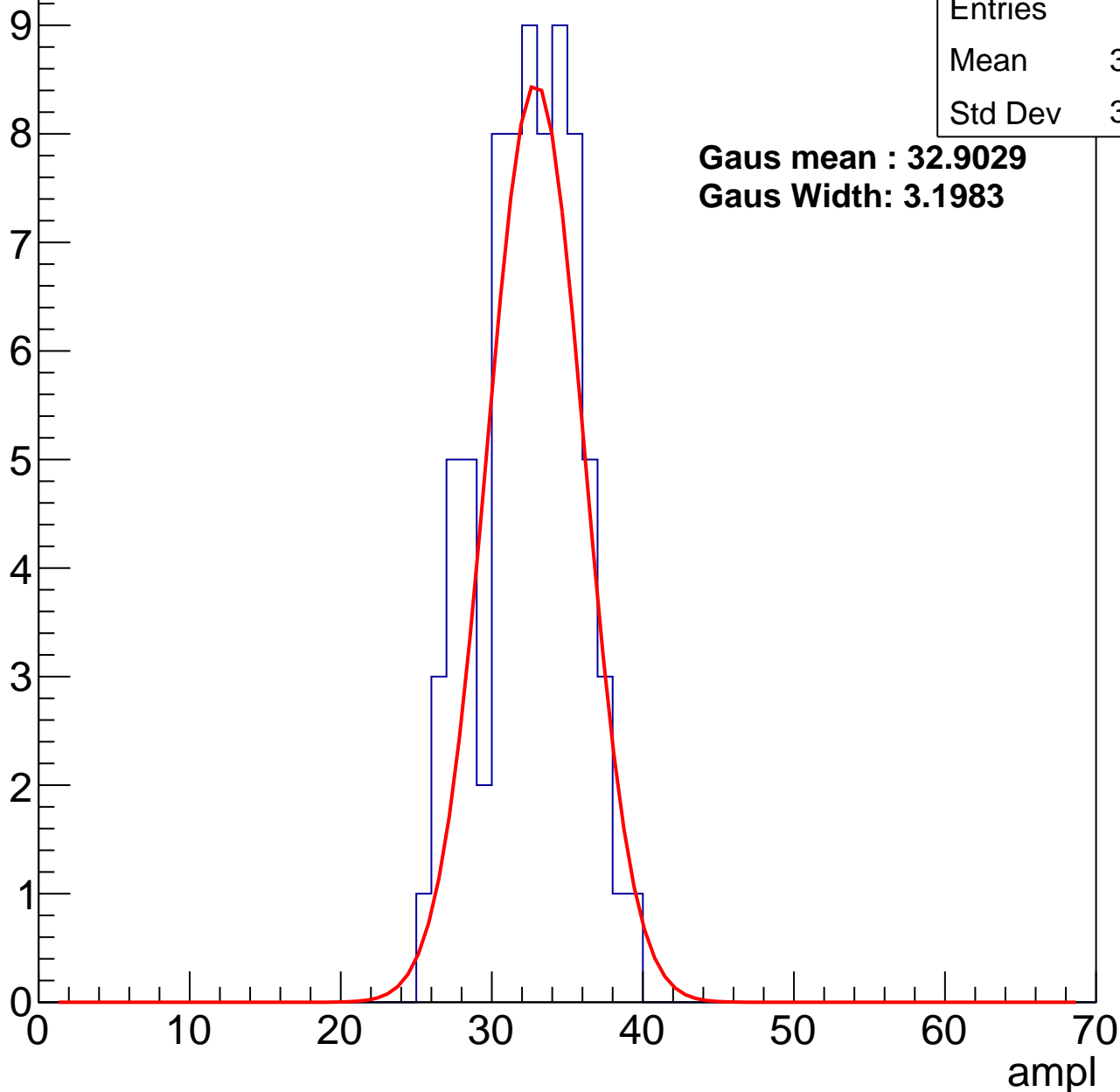
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	76
Mean	31.97
Std Dev	3.195

**Gaus mean : 32.9029**

**Gaus Width: 3.1983**



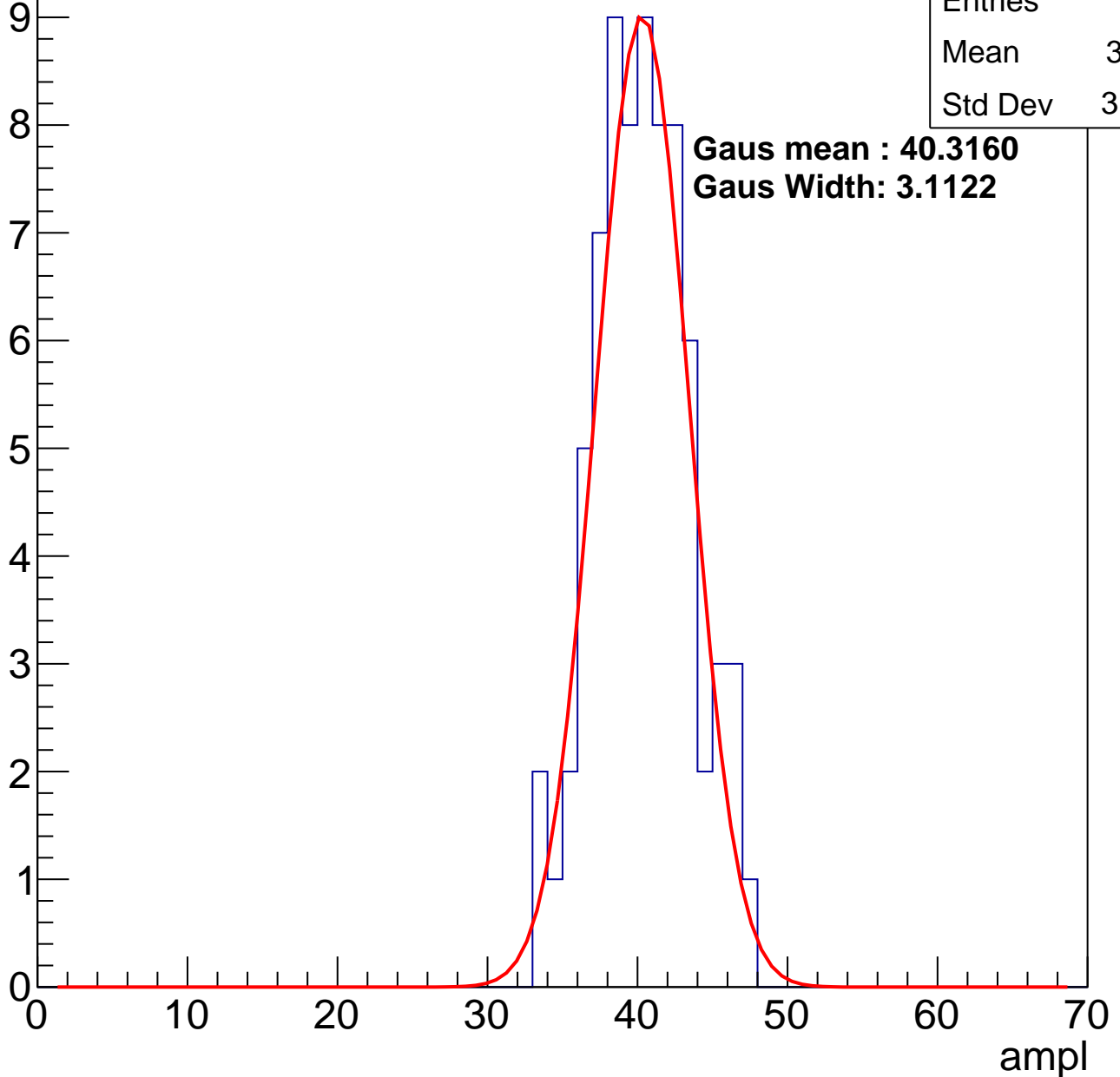
# B0L001S, U24-ch19, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	39.91
Std Dev	3.137

**Gaus mean : 40.3160**  
**Gaus Width: 3.1122**



# B0L001S, U24-ch19, adc2

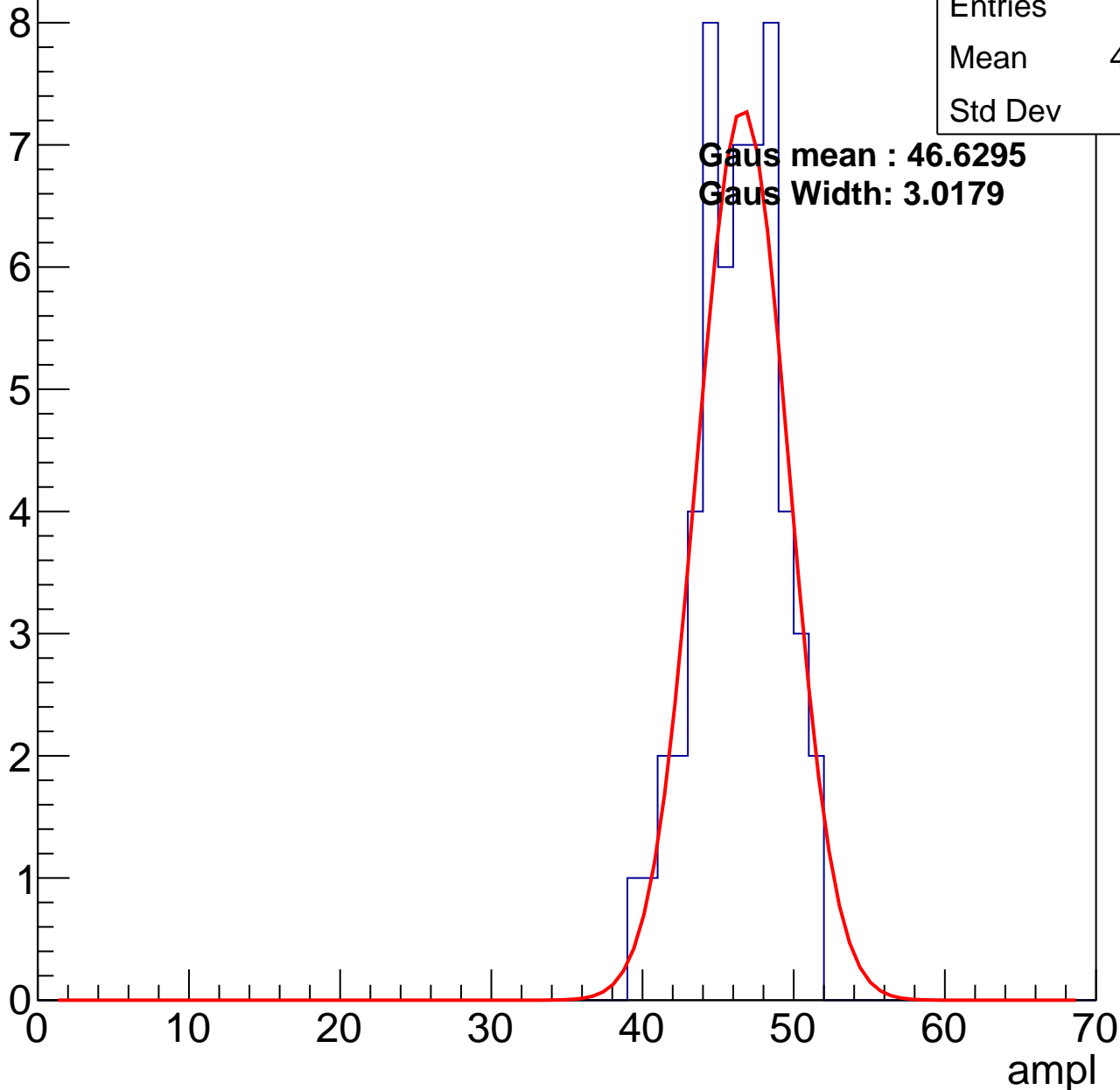
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	45.85
Std Dev	2.74

**Gaus mean : 46.6295**

**Gaus Width: 3.0179**

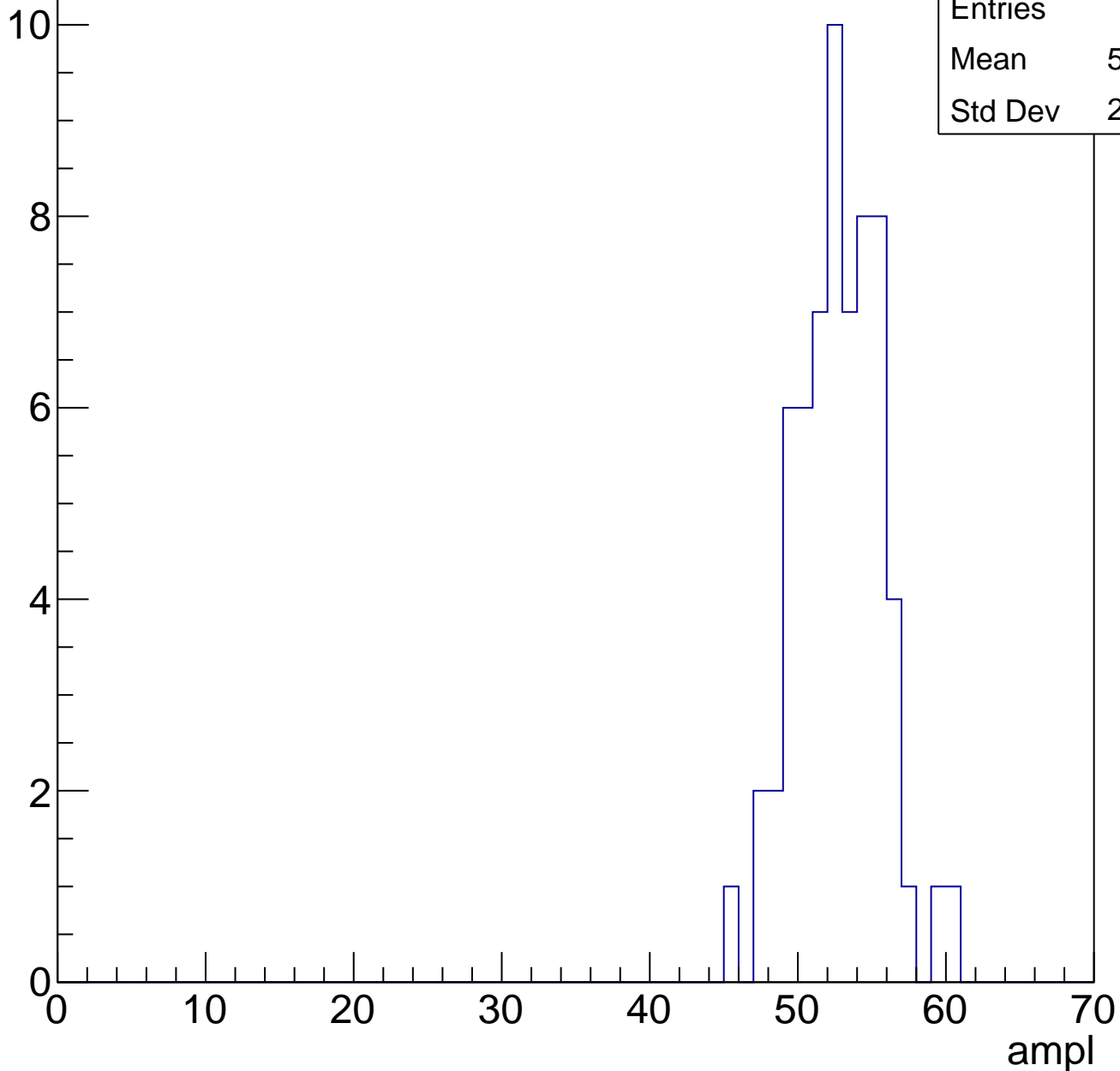


# B0L001S, U24-ch19, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	64
Mean	52.33
Std Dev	2.856

Entry

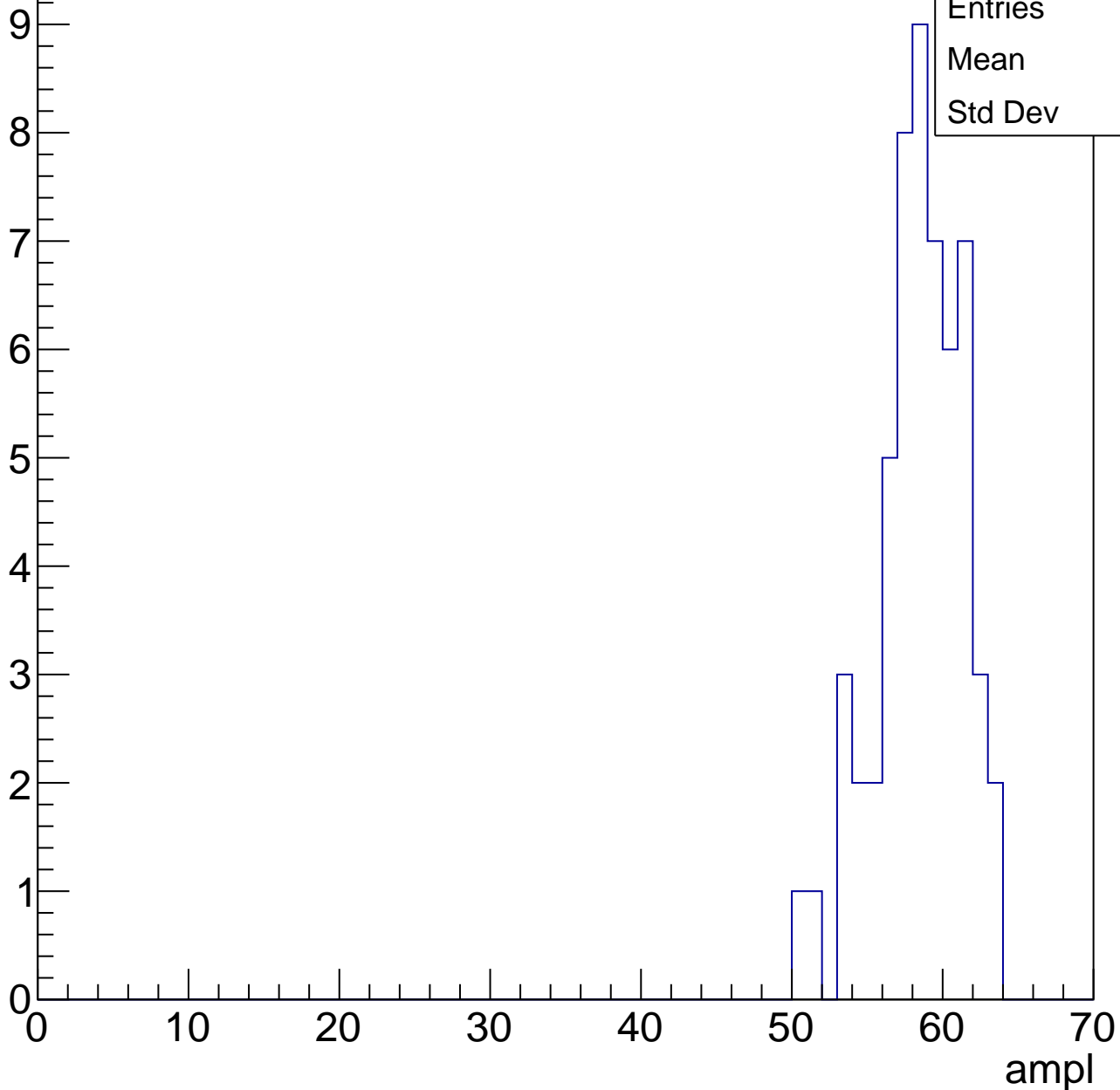


# B0L001S, U24-ch19, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	58
Std Dev	2.86

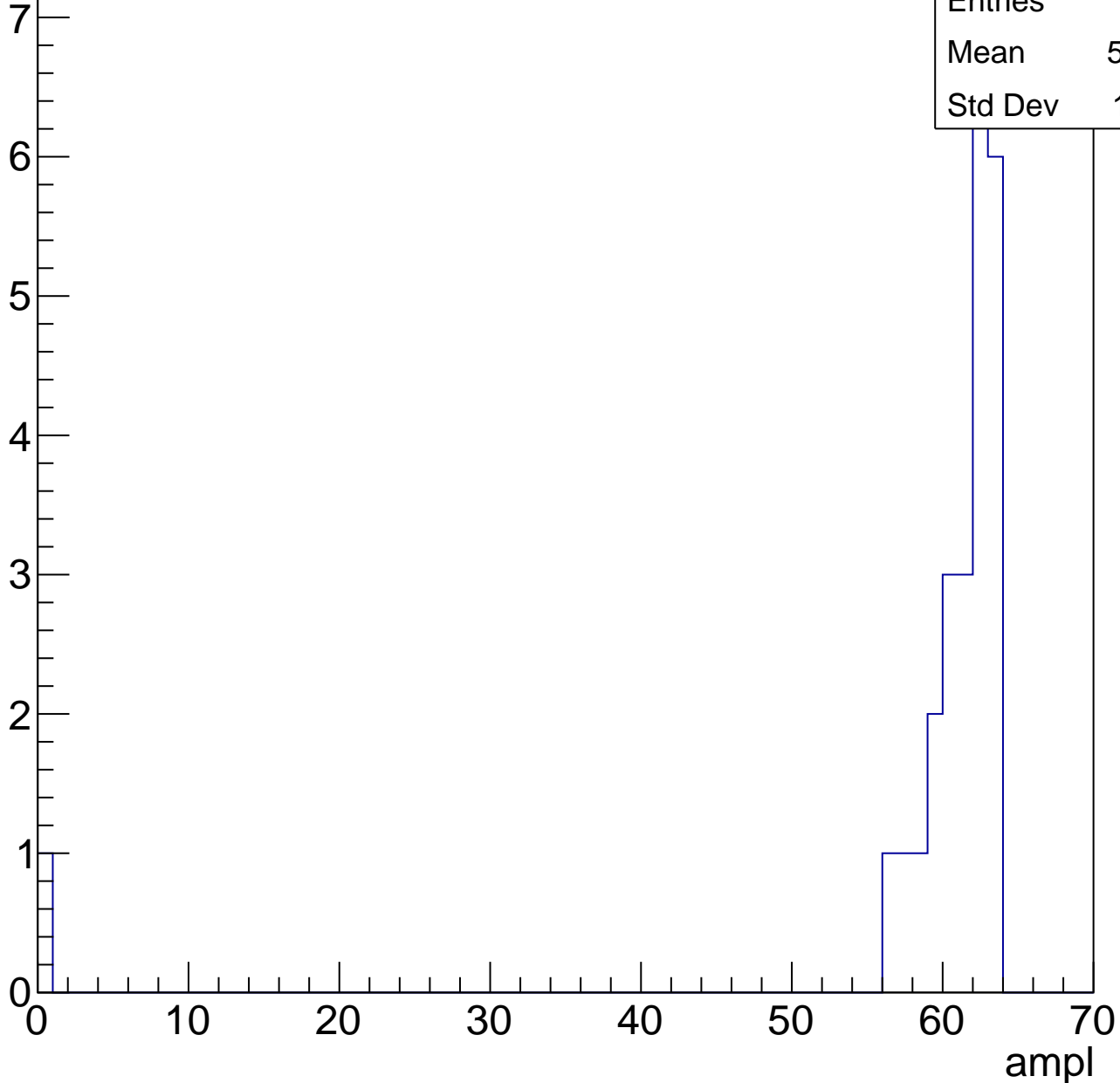


# B0L001S, U24-ch19, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	25
Mean	58.56
Std Dev	12.11



# B0L001S, U24-ch19, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

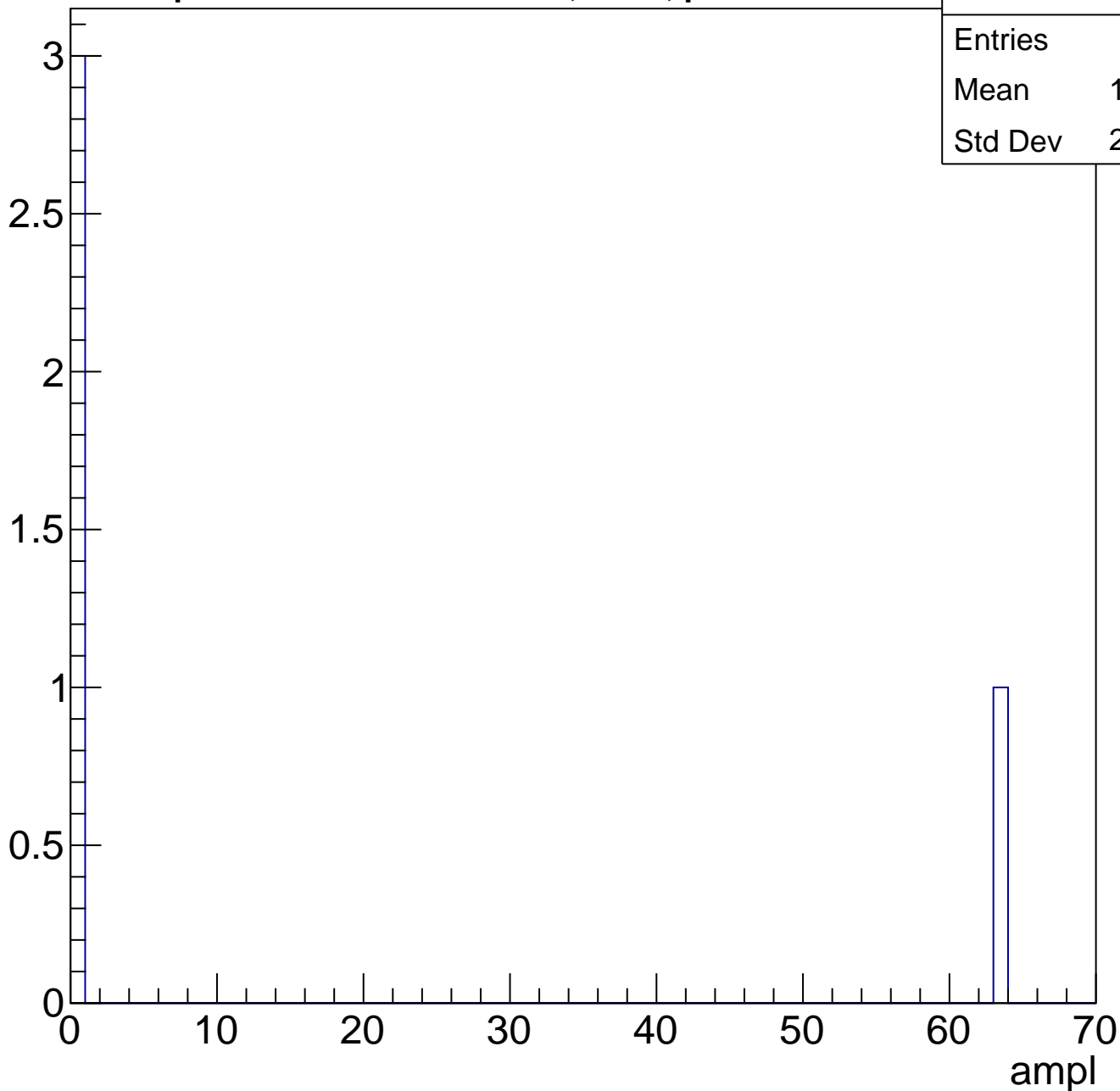




# B0L001S, U24-ch19, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U24-ch20, adc0

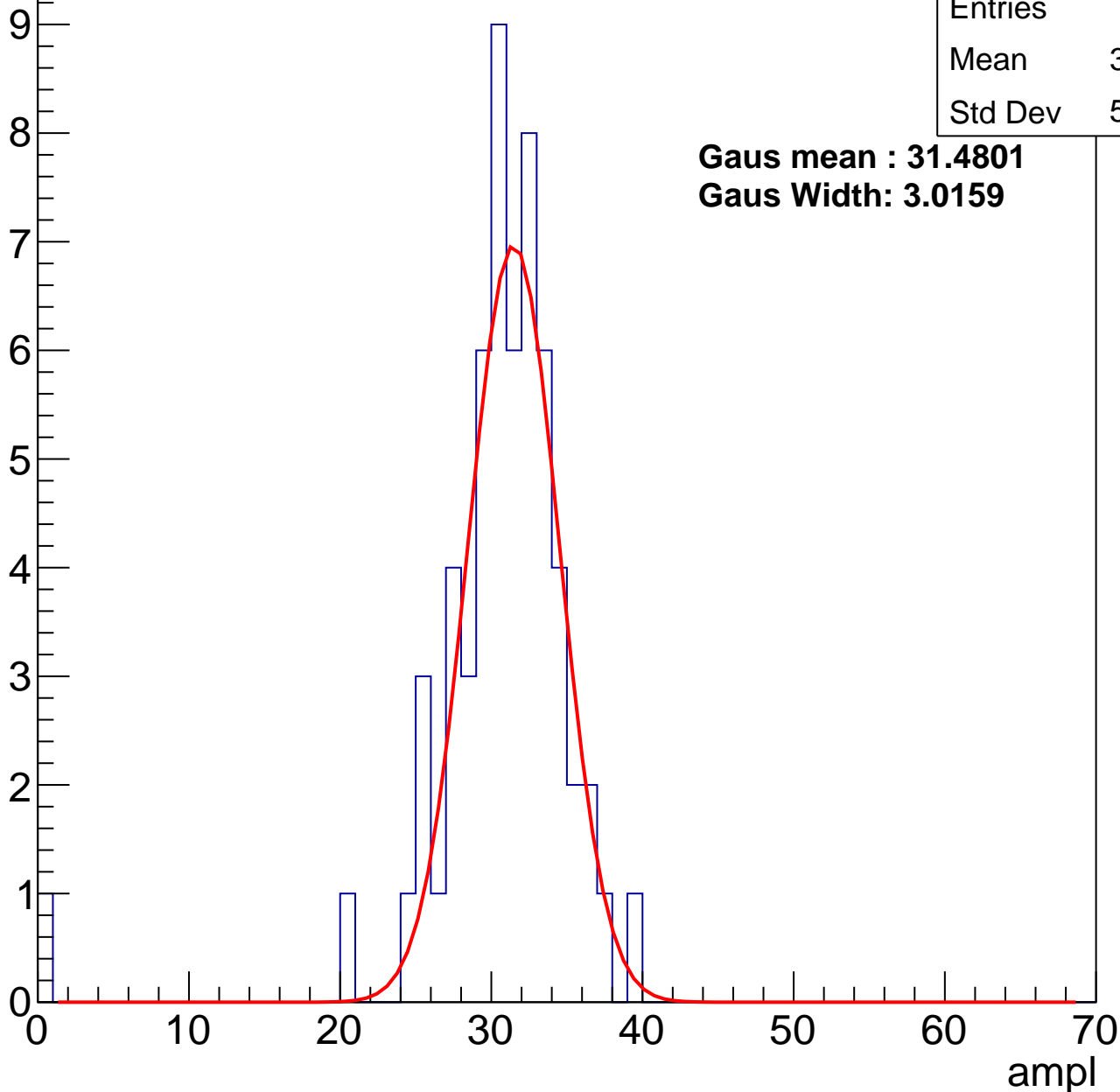
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	30.08
Std Dev	5.189

**Gaus mean : 31.4801**

**Gaus Width: 3.0159**



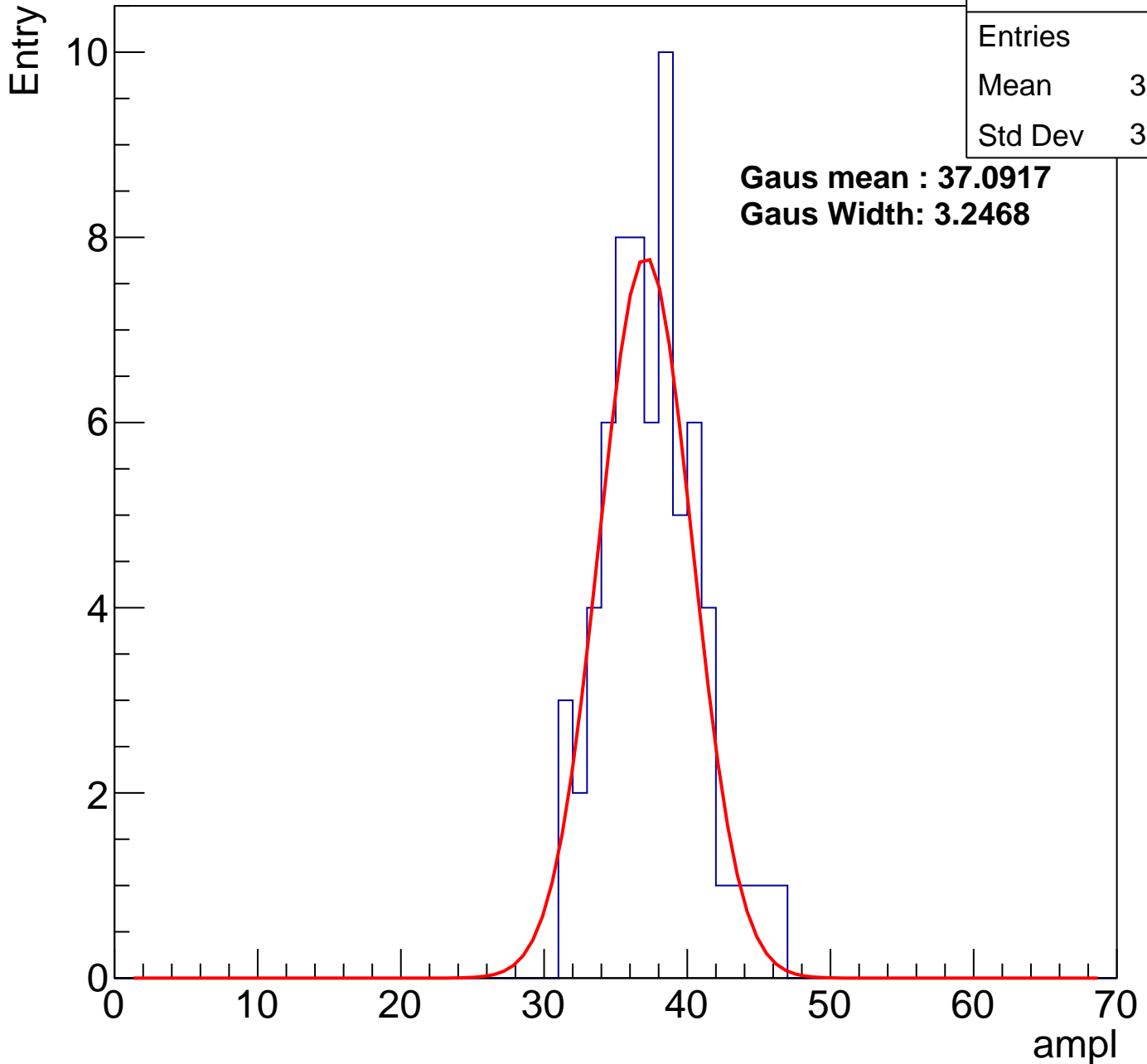
# B0L001S, U24-ch20, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	67
Mean	37.04
Std Dev	3.276

**Gaus mean : 37.0917**

**Gaus Width: 3.2468**



# B0L001S, U24-ch20, adc2

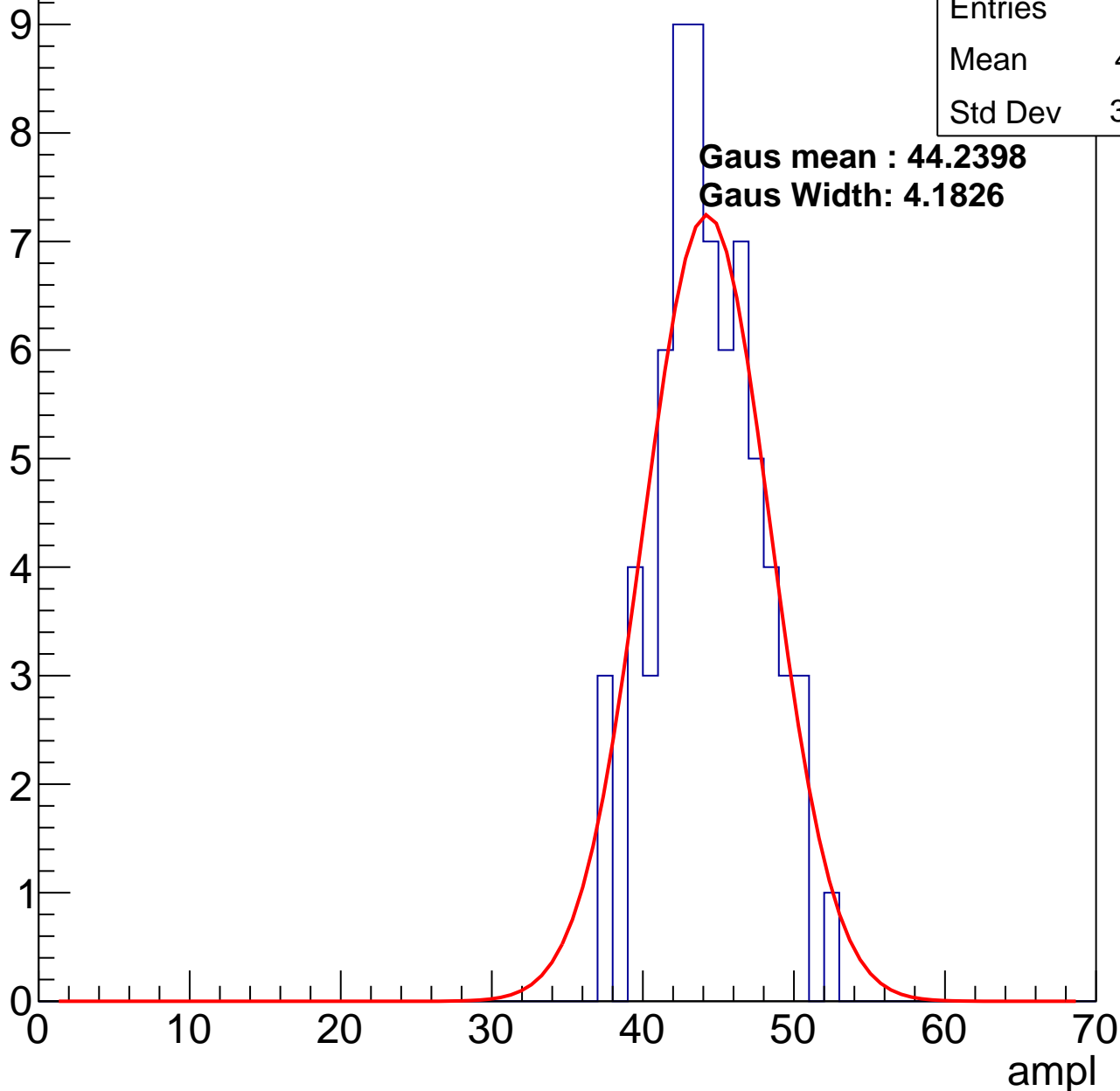
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	43.91
Std Dev	3.346

**Gaus mean : 44.2398**

**Gaus Width: 4.1826**

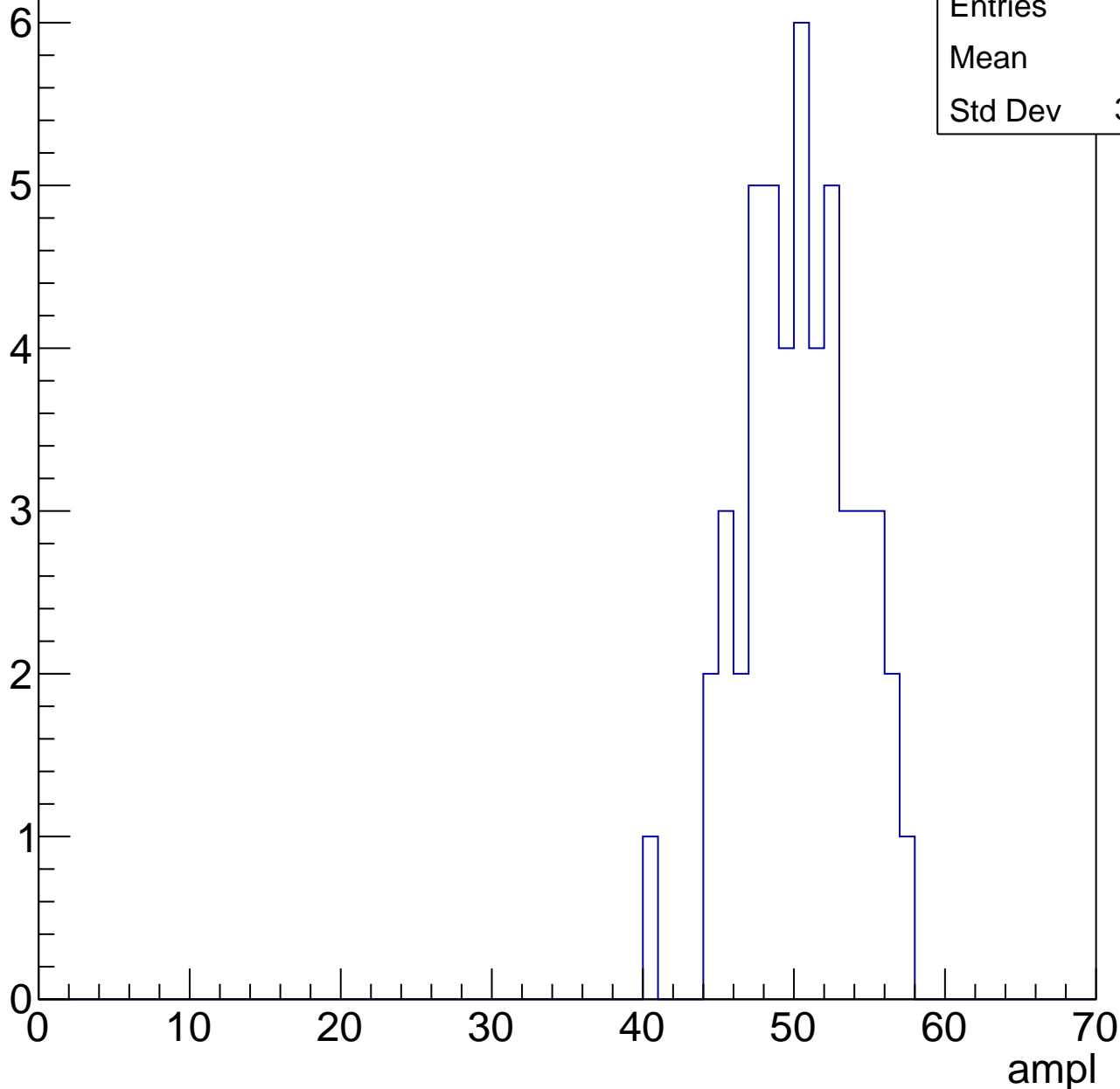


# B0L001S, U24-ch20, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	49
Mean	49.9
Std Dev	3.621

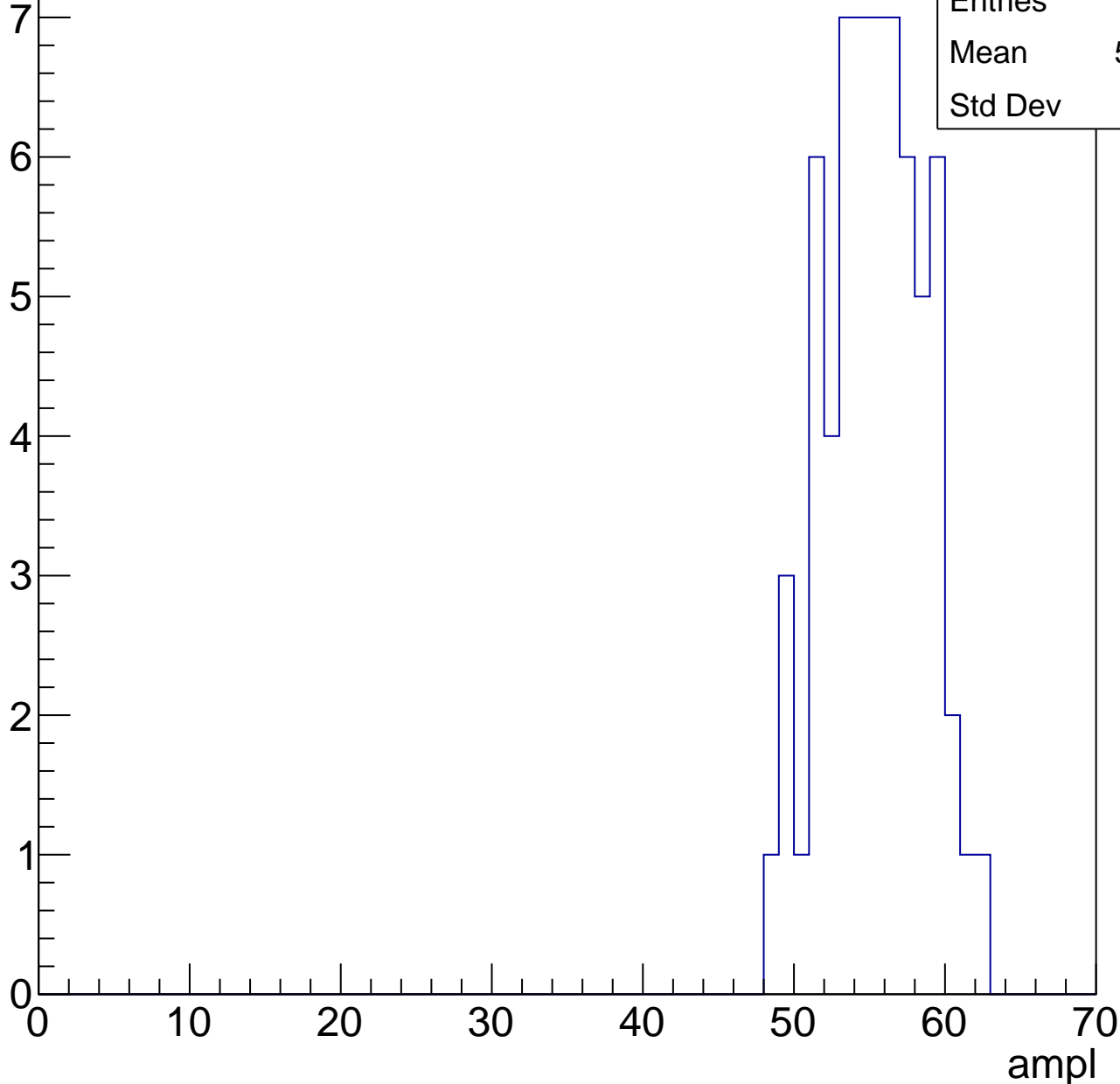


# B0L001S, U24-ch20, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	54.91
Std Dev	3.2

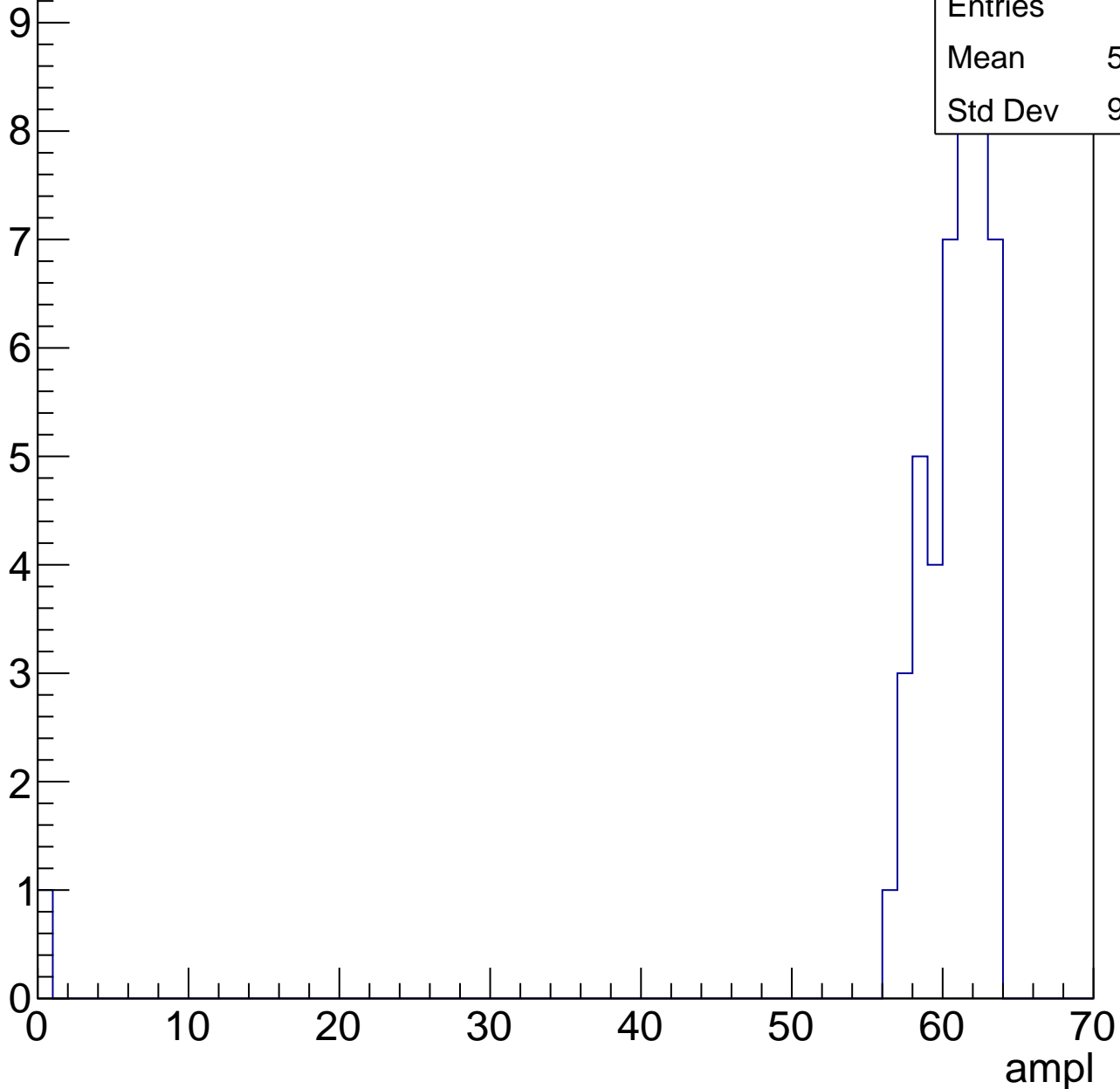


# B0L001S, U24-ch20, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	45
Mean	59.09
Std Dev	9.109



# B0L001S, U24-ch20, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch20, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U24-ch21, adc0

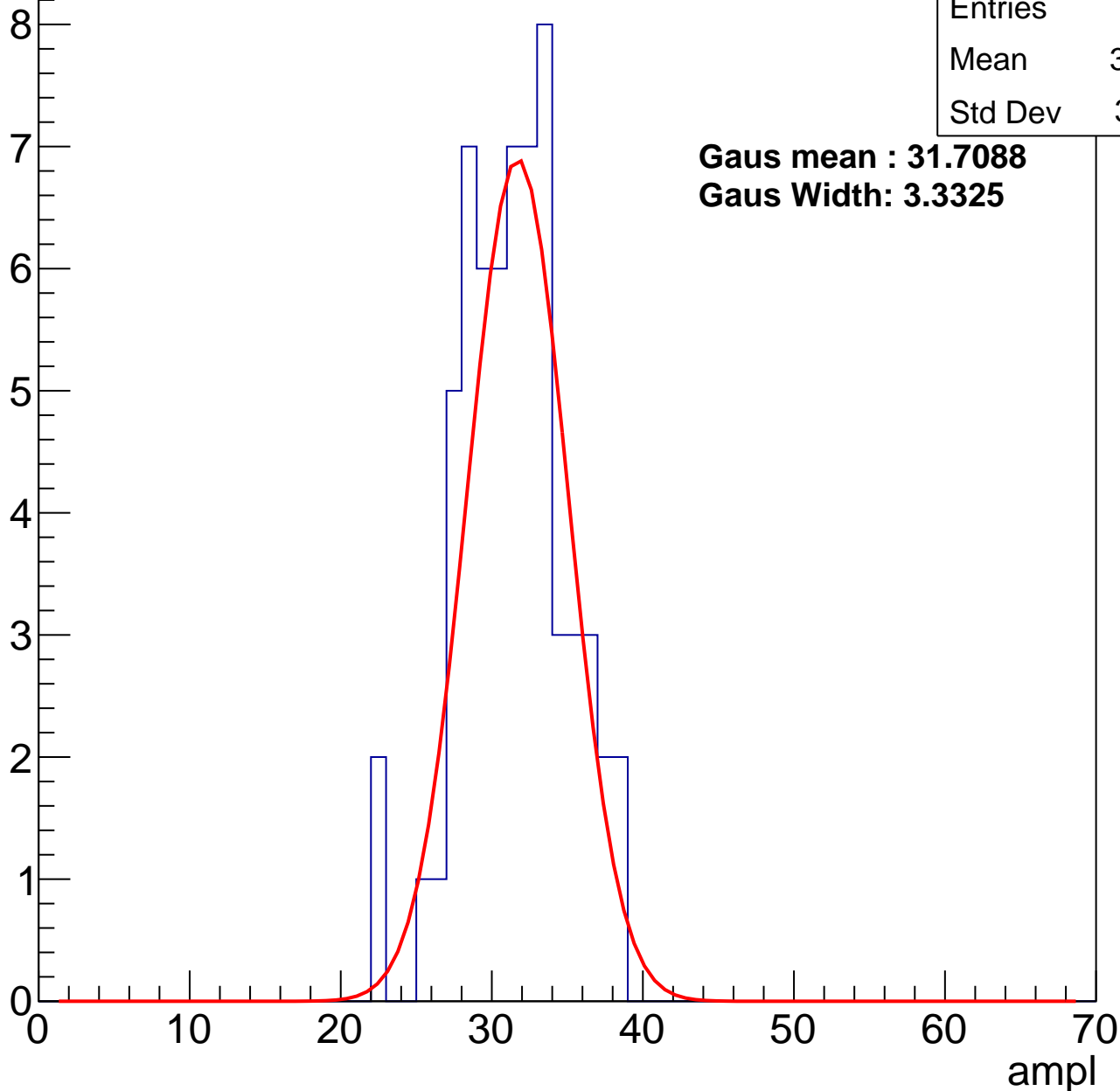
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	30.95
Std Dev	3.461

**Gaus mean : 31.7088**

**Gaus Width: 3.3325**



# B0L001S, U24-ch21, adc1

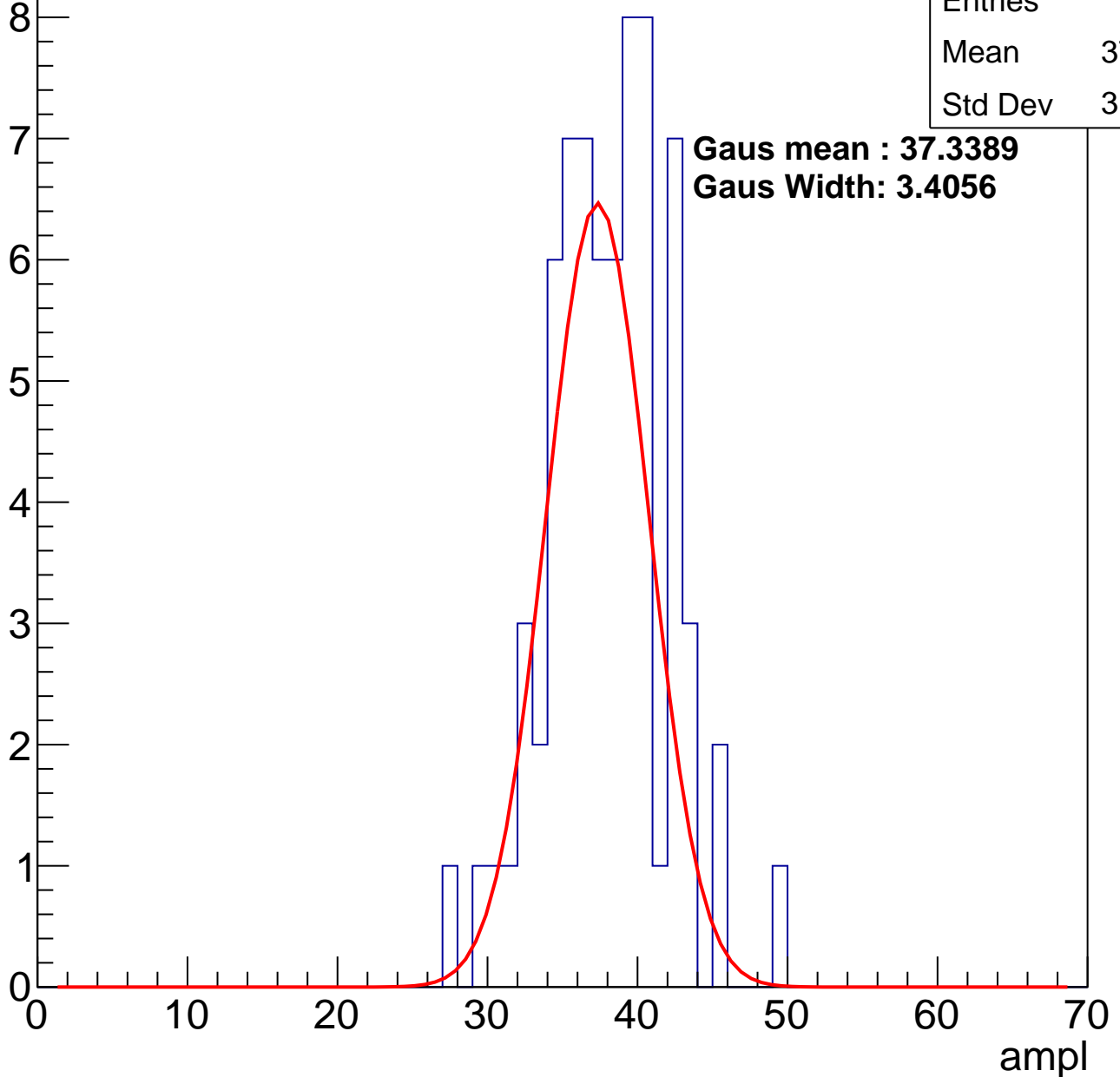
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	37.54
Std Dev	3.946

**Gaus mean : 37.3389**

**Gaus Width: 3.4056**



# B0L001S, U24-ch21, adc2

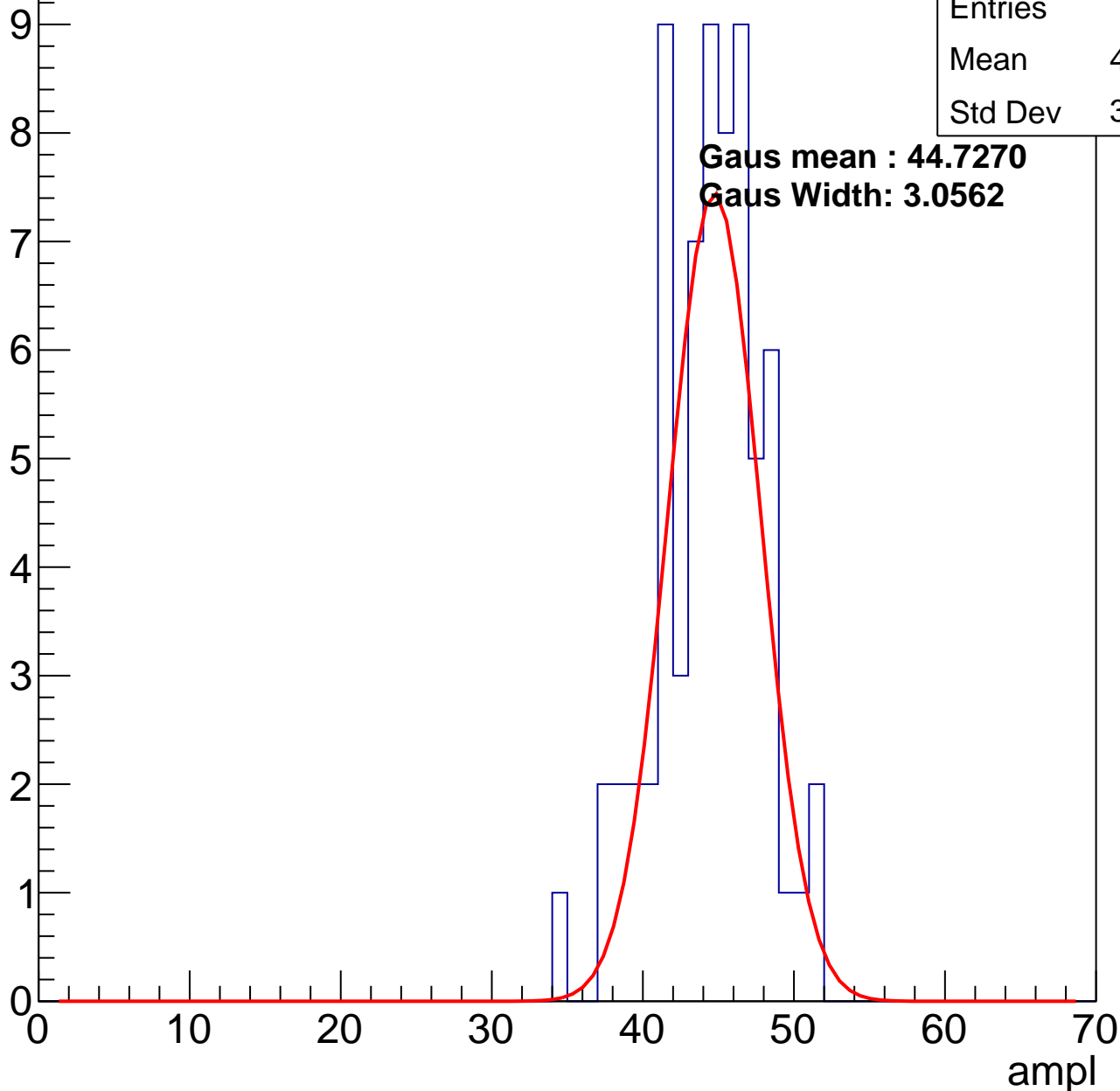
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	43.94
Std Dev	3.396

**Gaus mean : 44.7270**

**Gaus Width: 3.0562**

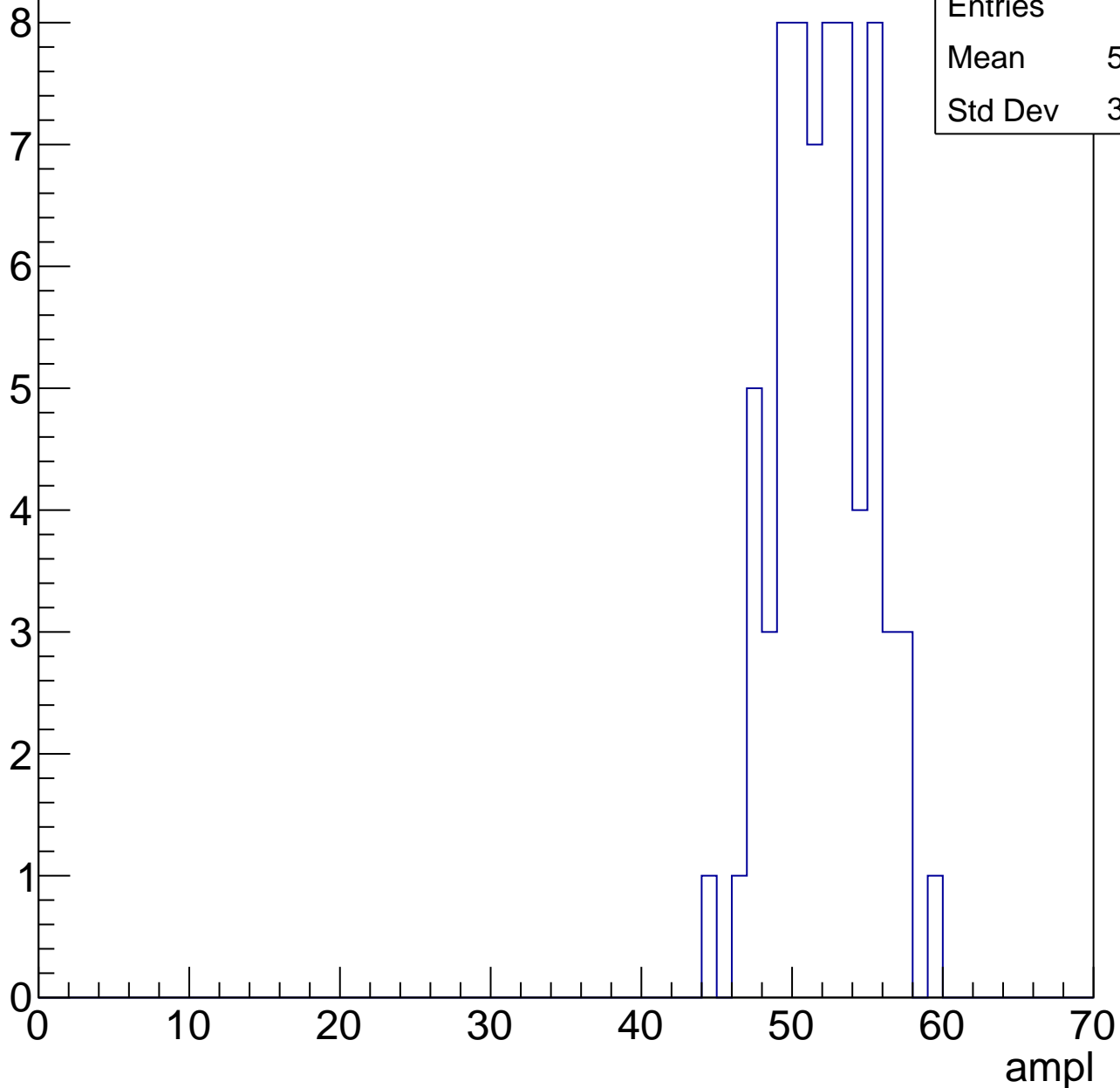


# B0L001S, U24-ch21, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

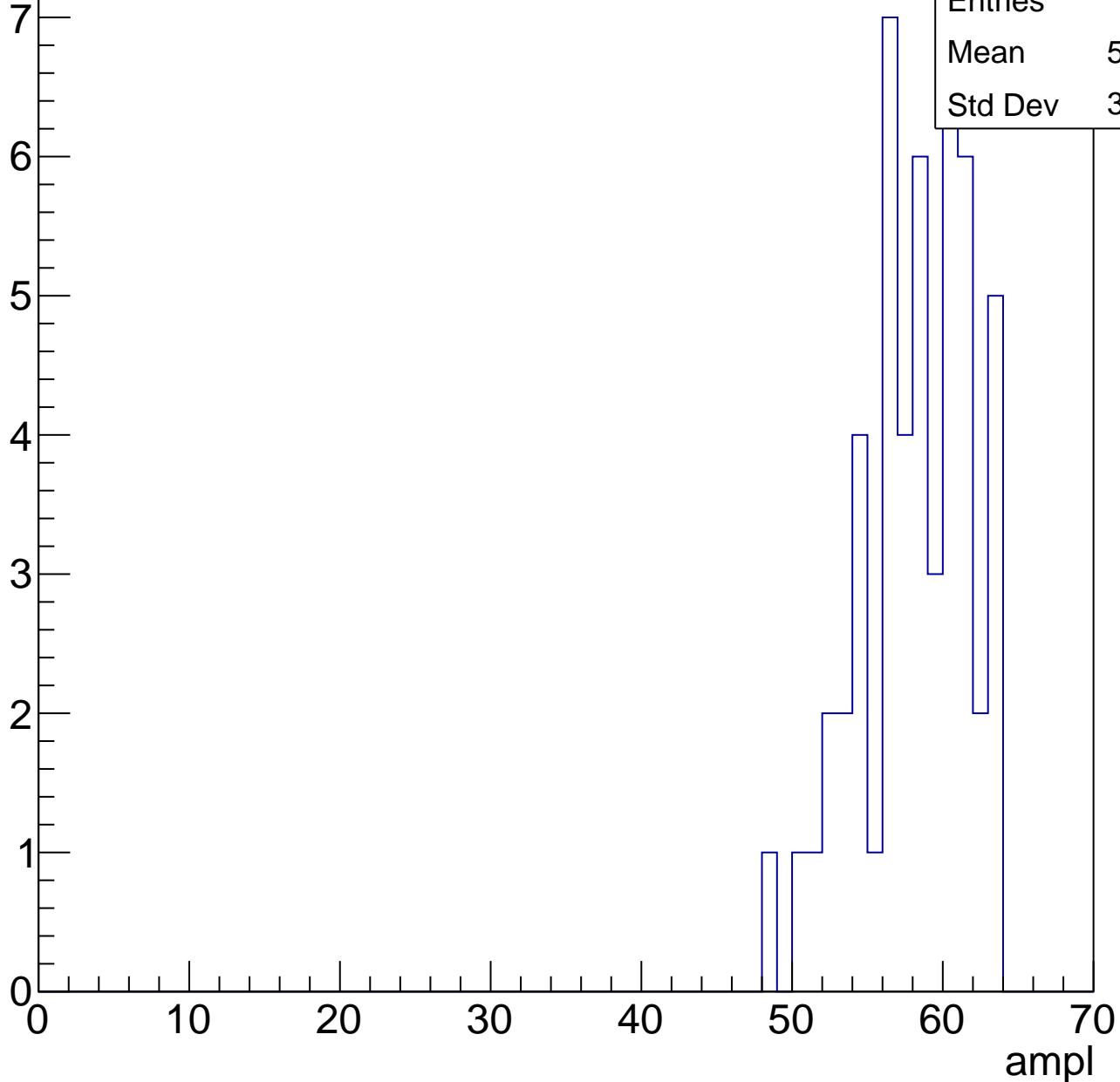
Entries	68
Mean	51.65
Std Dev	3.076



# B0L001S, U24-ch21, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

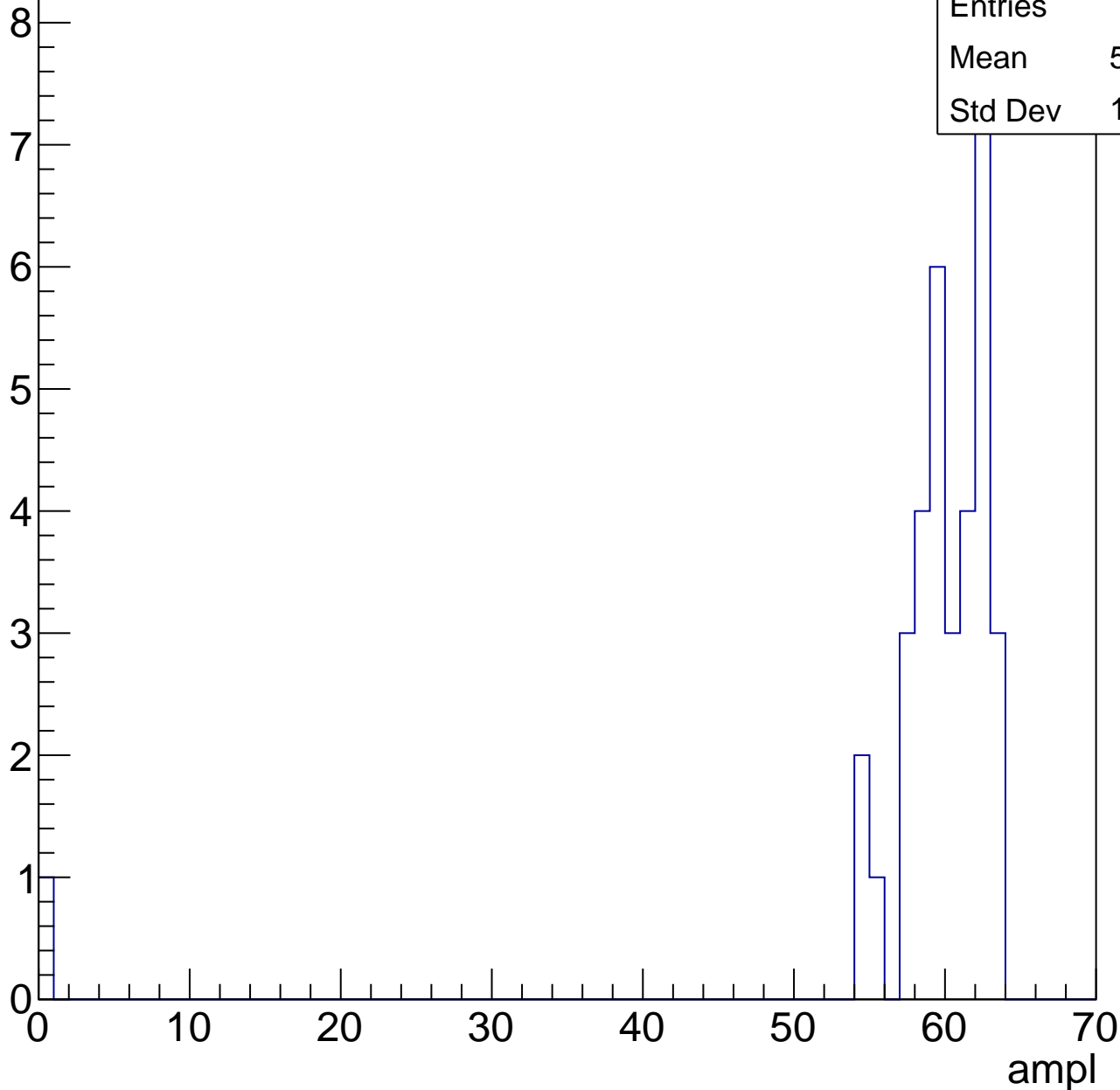


# B0L001S, U24-ch21, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	35
Mean	57.97
Std Dev	10.23



# B0L001S, U24-ch21, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch21, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U24-ch22, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	30.51
Std Dev	3.334

**Gaus mean : 30.9633**

**Gaus Width: 3.2772**

10

8

6

4

2

0

0

10

20

30

40

50

60

70

ampl

10

8

6

4

2

0

0

10

20

30

40

50

60

70

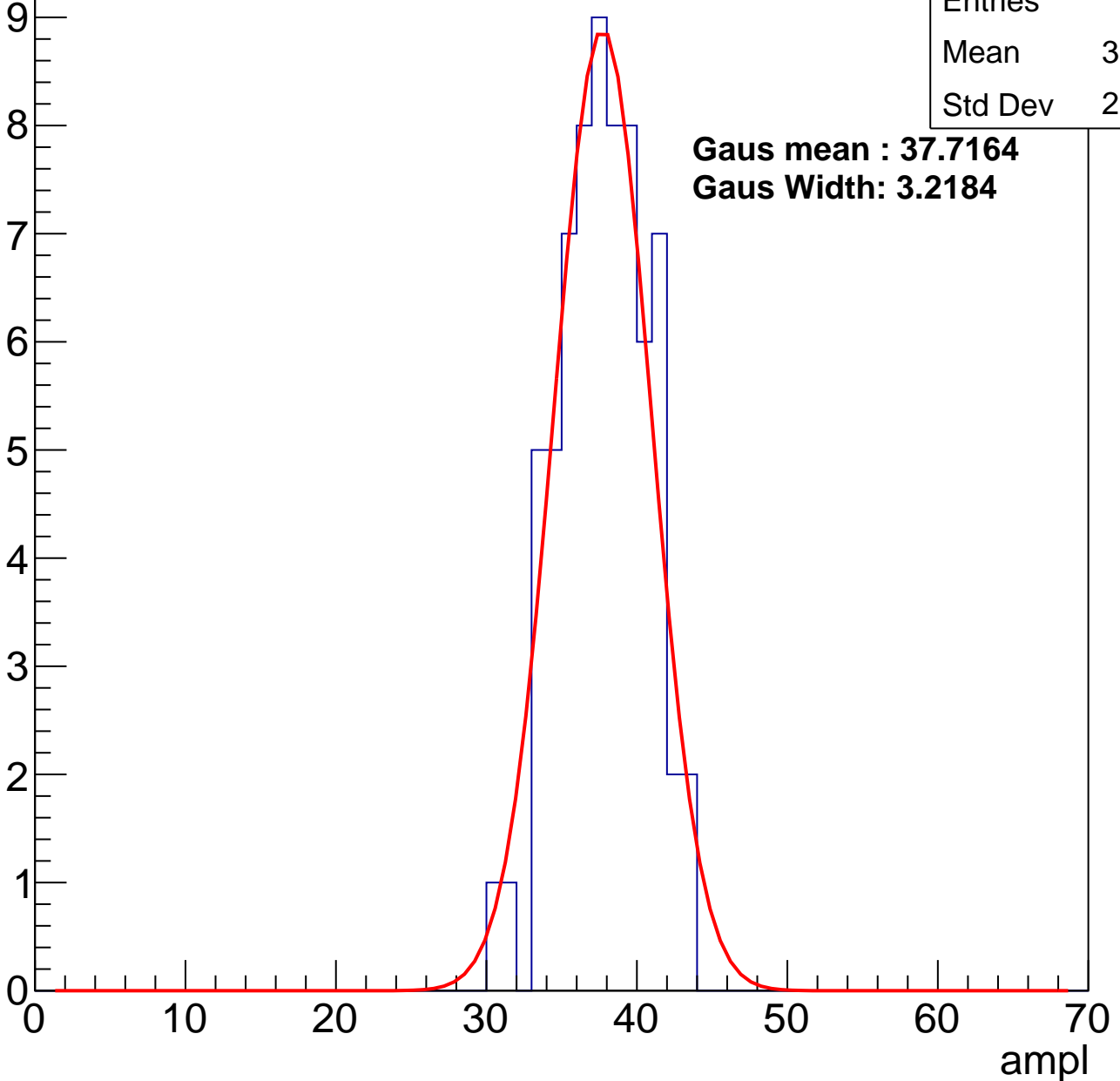
# B0L001S, U24-ch22, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	37.32
Std Dev	2.867

**Gaus mean : 37.7164**  
**Gaus Width: 3.2184**



# B0L001S, U24-ch22, adc2

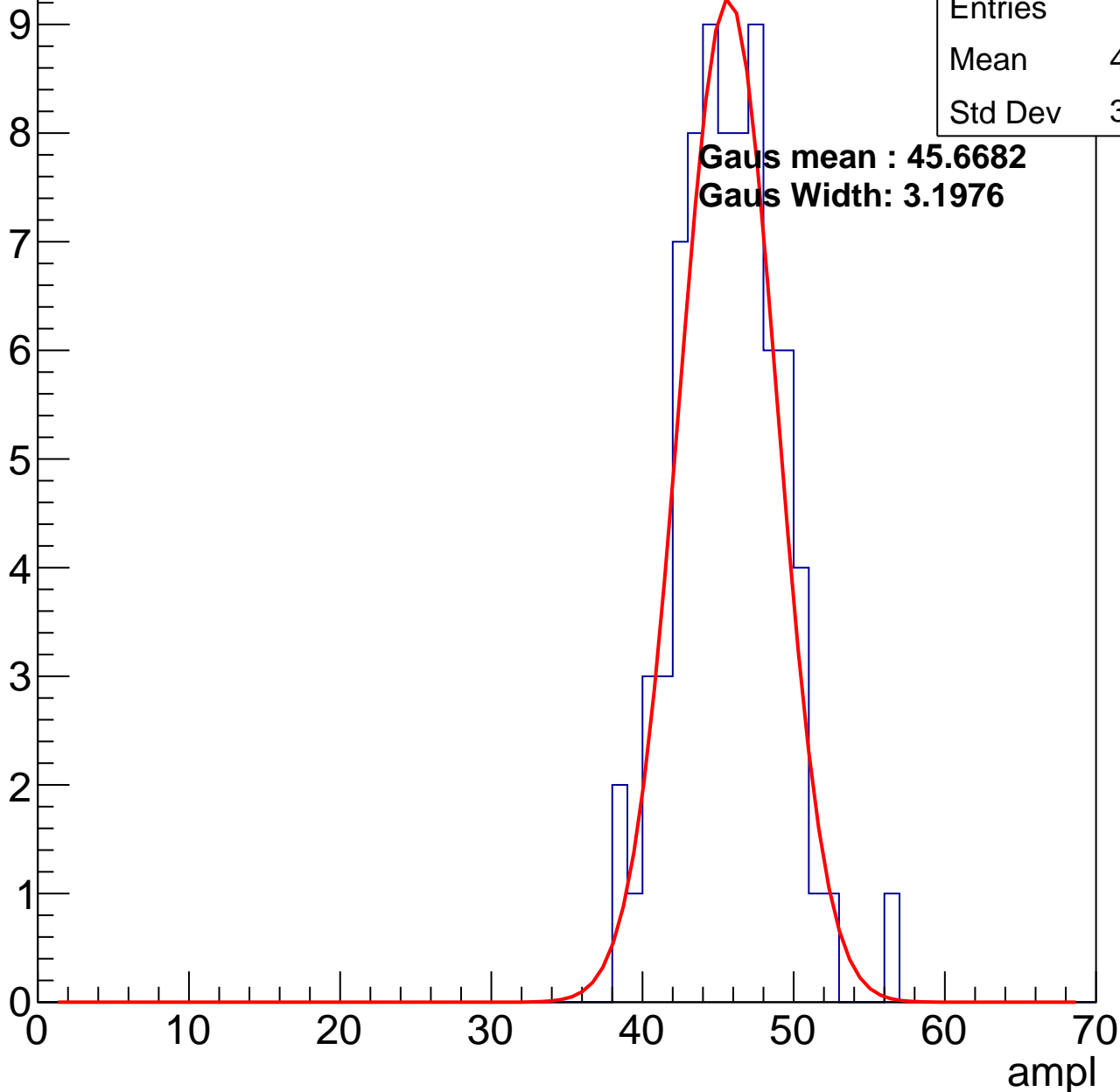
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	77
Mean	45.25
Std Dev	3.335

**Gaus mean : 45.6682**

**Gaus Width: 3.1976**

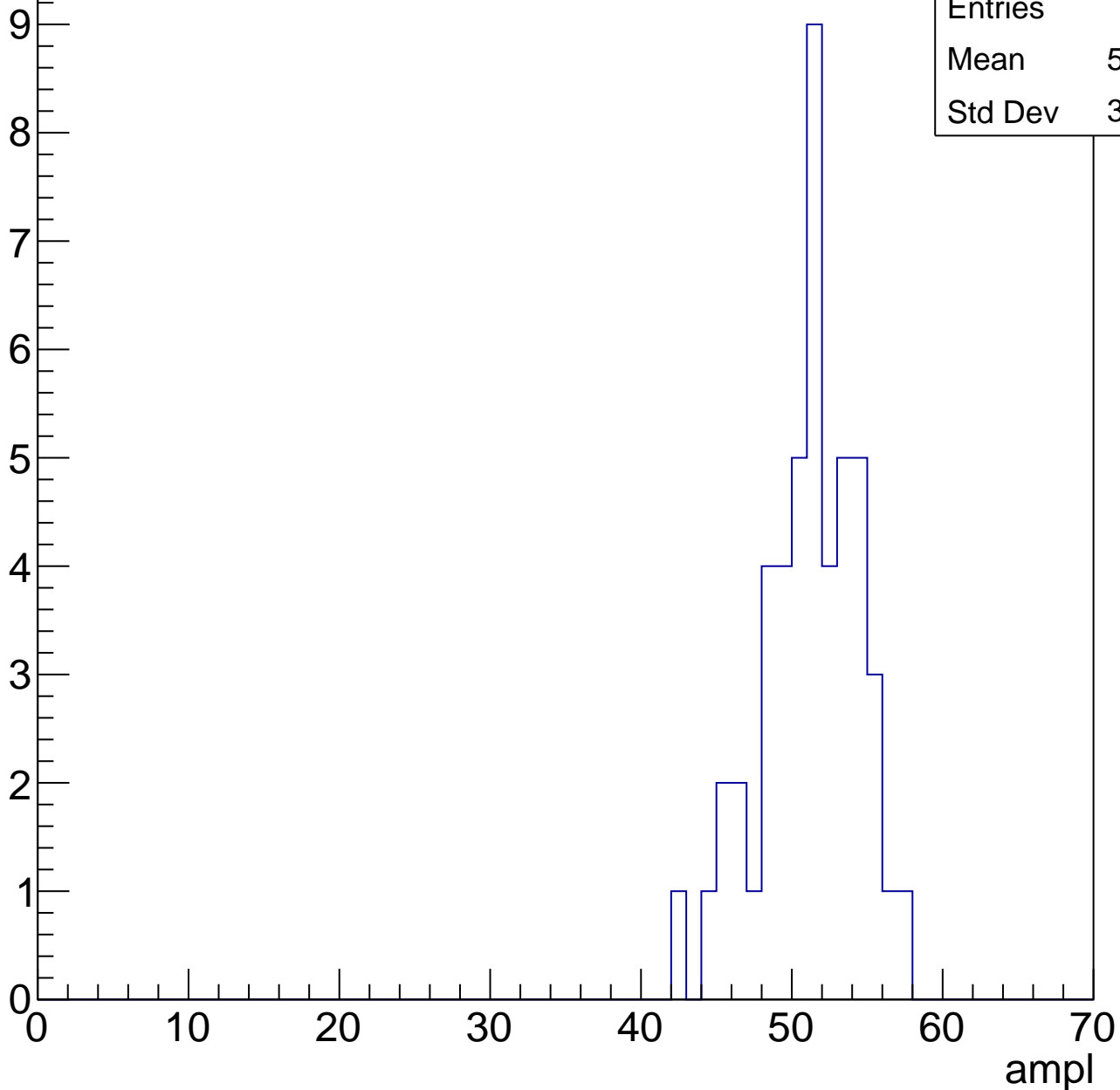


# B0L001S, U24-ch22, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

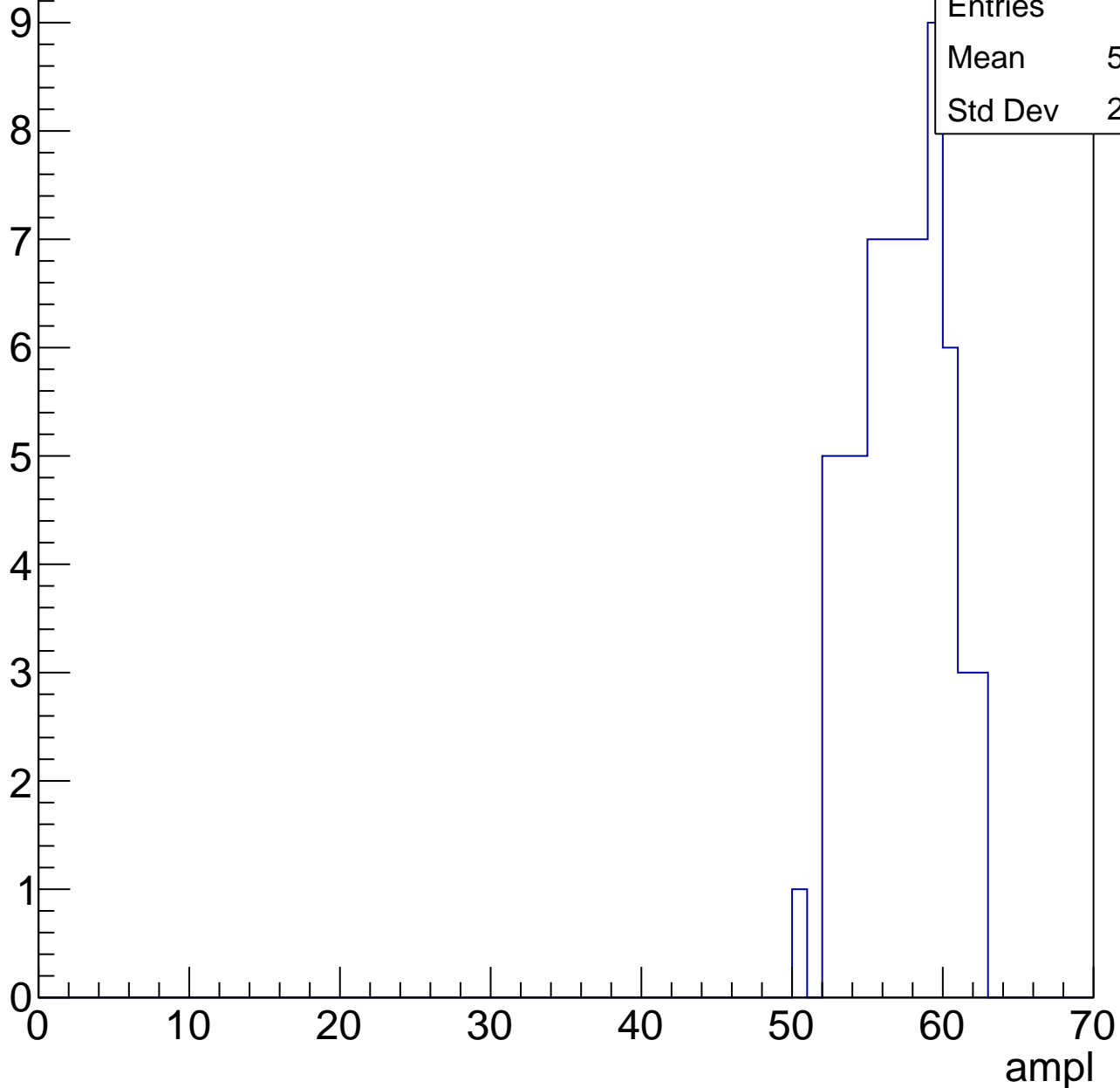
Entries	48
Mean	50.69
Std Dev	3.222



# B0L001S, U24-ch22, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

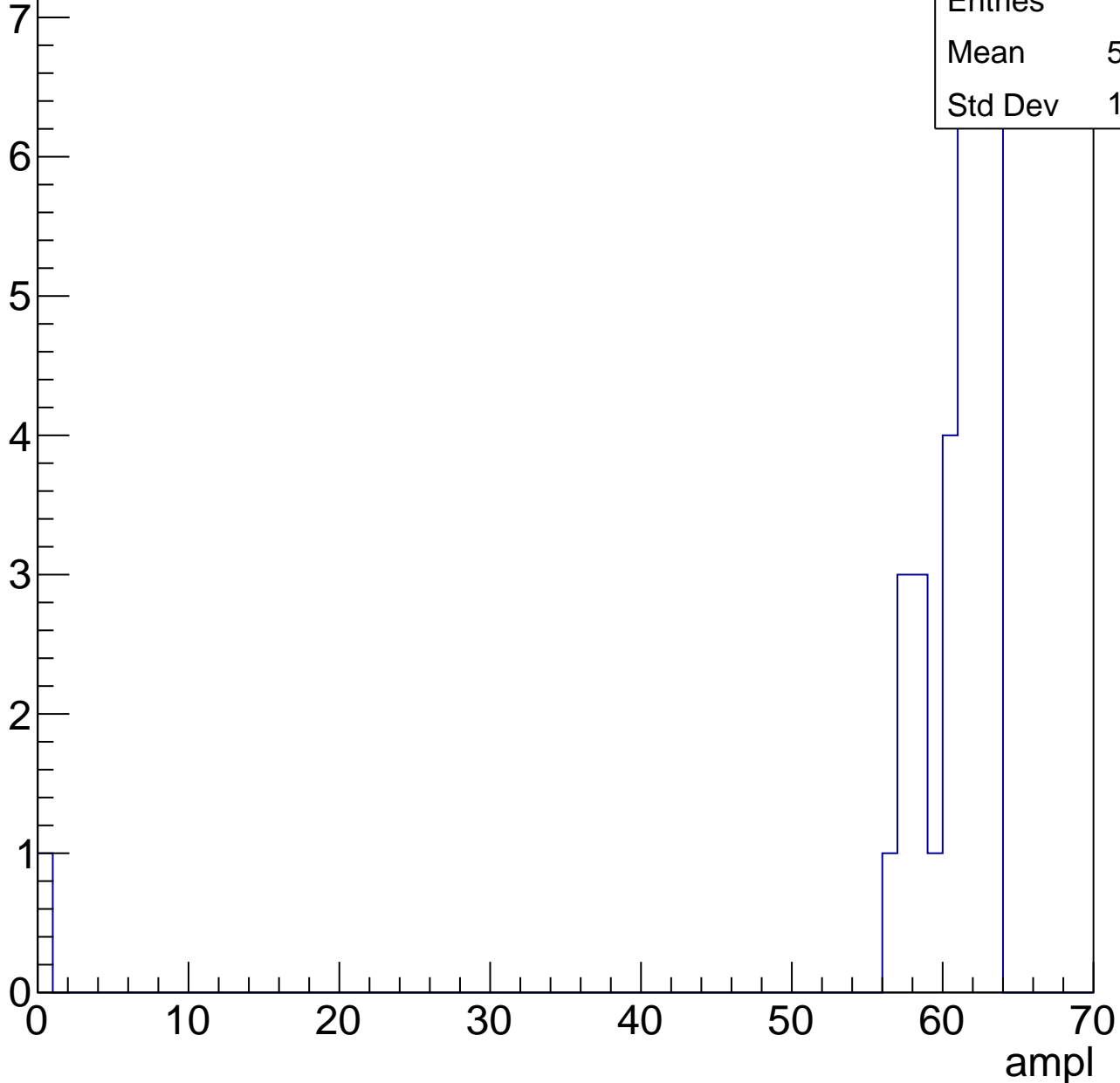


# B0L001S, U24-ch22, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	34
Mean	58.88
Std Dev	10.45



# B0L001S, U24-ch22, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

3  
2.5  
2  
1.5  
1  
0.5  
0

Entries	3
Mean	63
Std Dev	0

ampl



# B0L001S, U24-ch22, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U24-ch23, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	86
Mean	30.07
Std Dev	3.47

**Gaus mean : 30.4674**

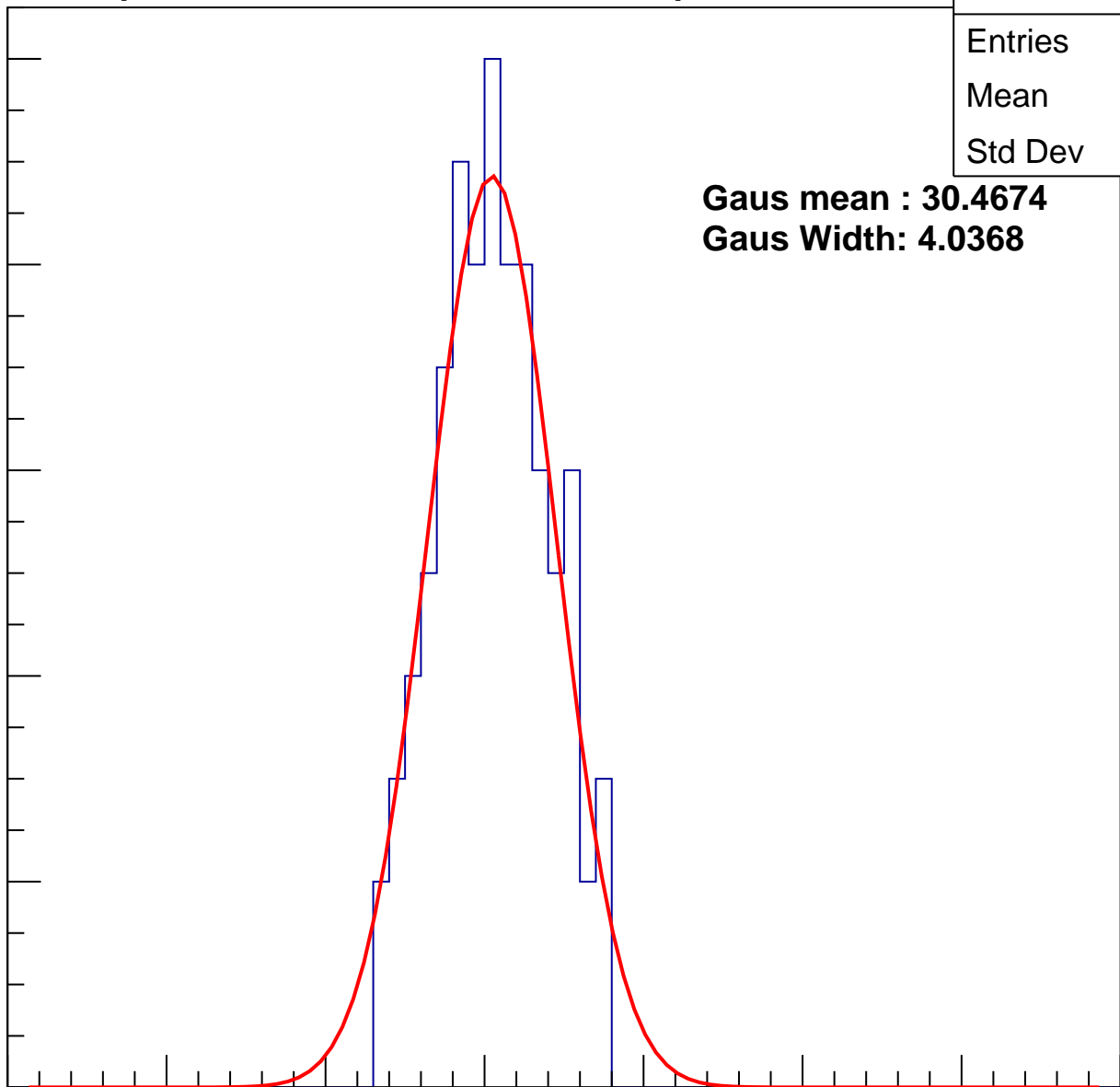
**Gaus Width: 4.0368**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U24-ch23, adc1

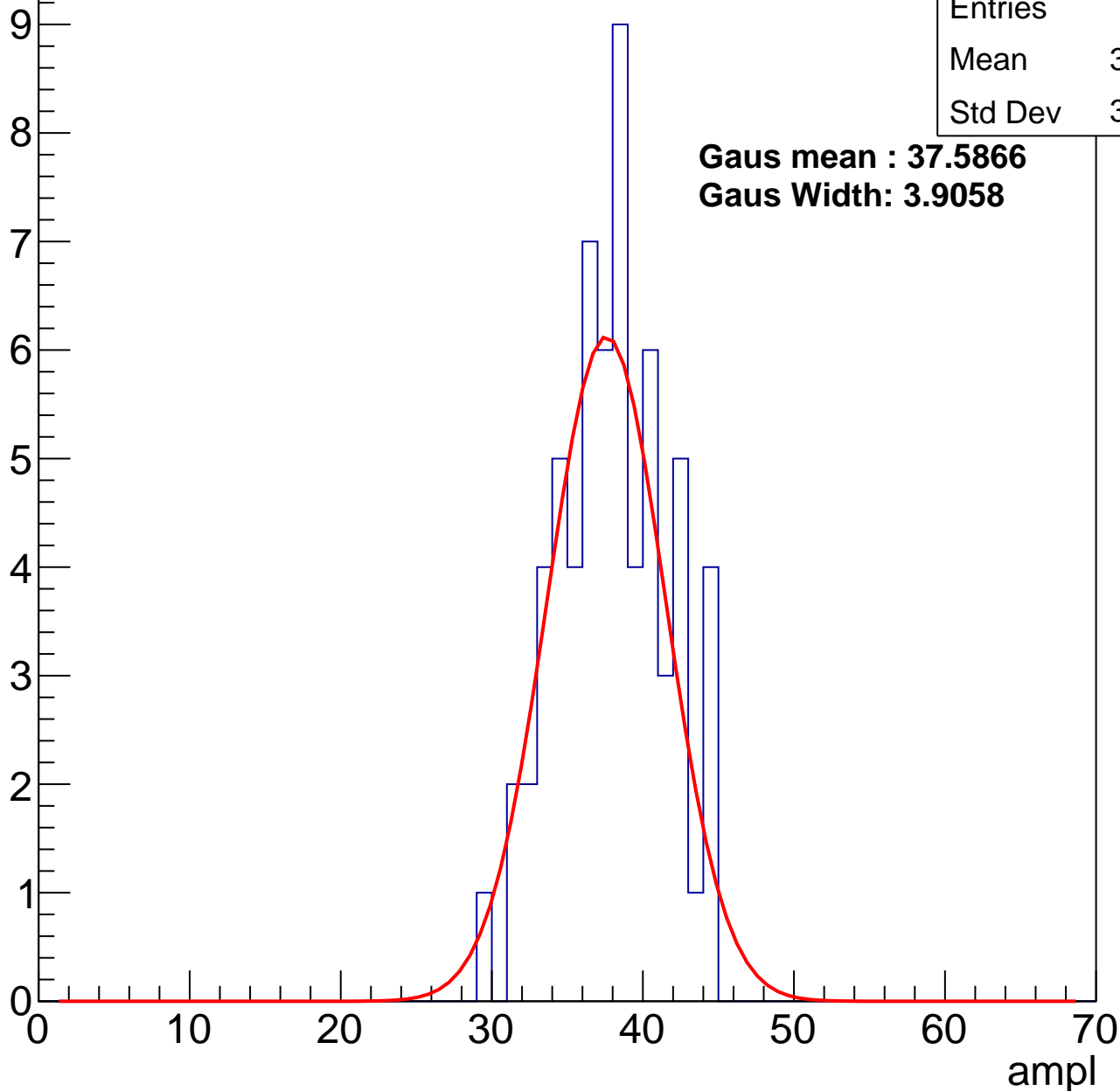
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	37.48
Std Dev	3.536

**Gaus mean : 37.5866**

**Gaus Width: 3.9058**



# B0L001S, U24-ch23, adc2

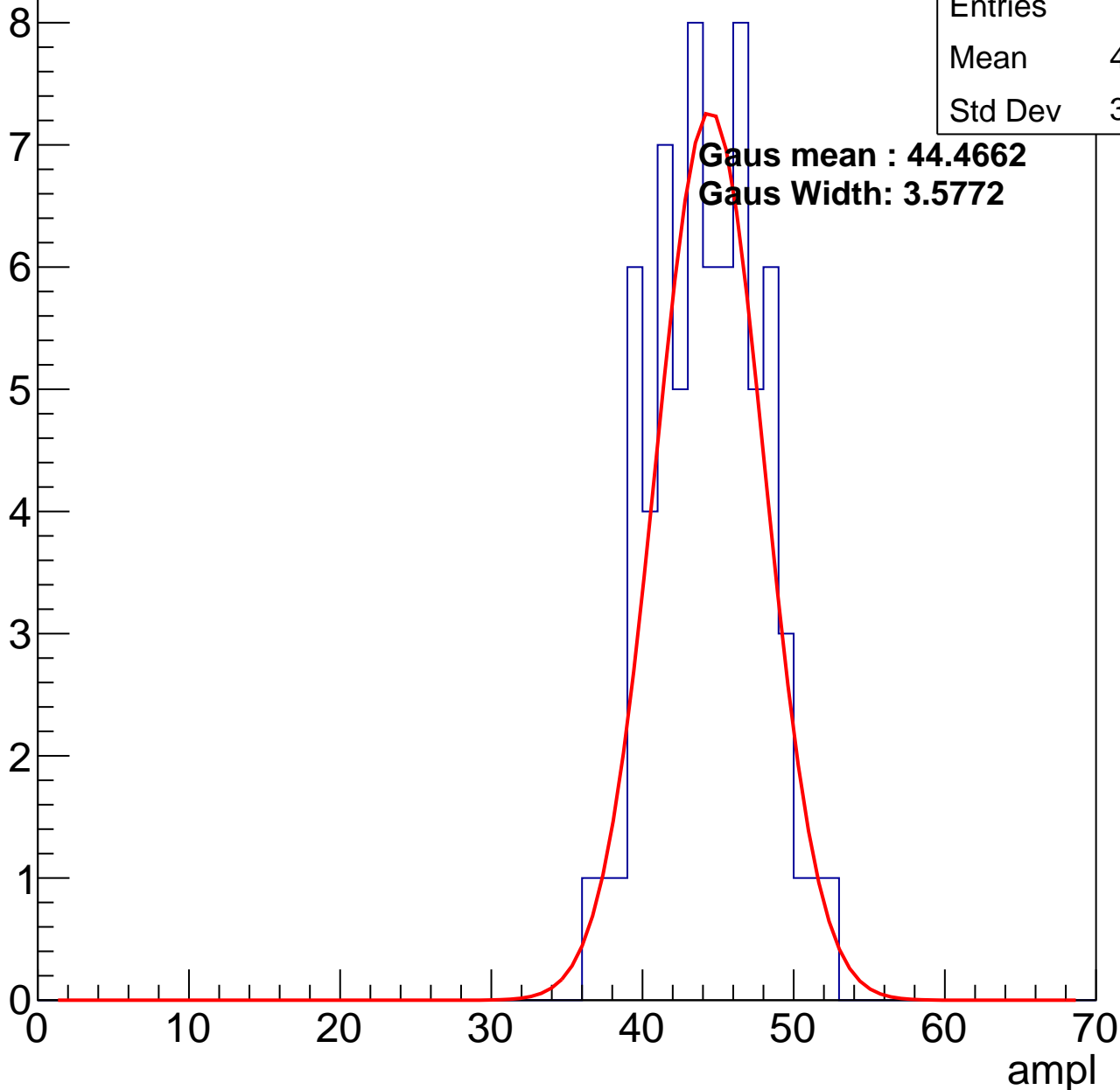
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	43.87
Std Dev	3.497

**Gaus mean : 44.4662**

**Gaus Width: 3.5772**

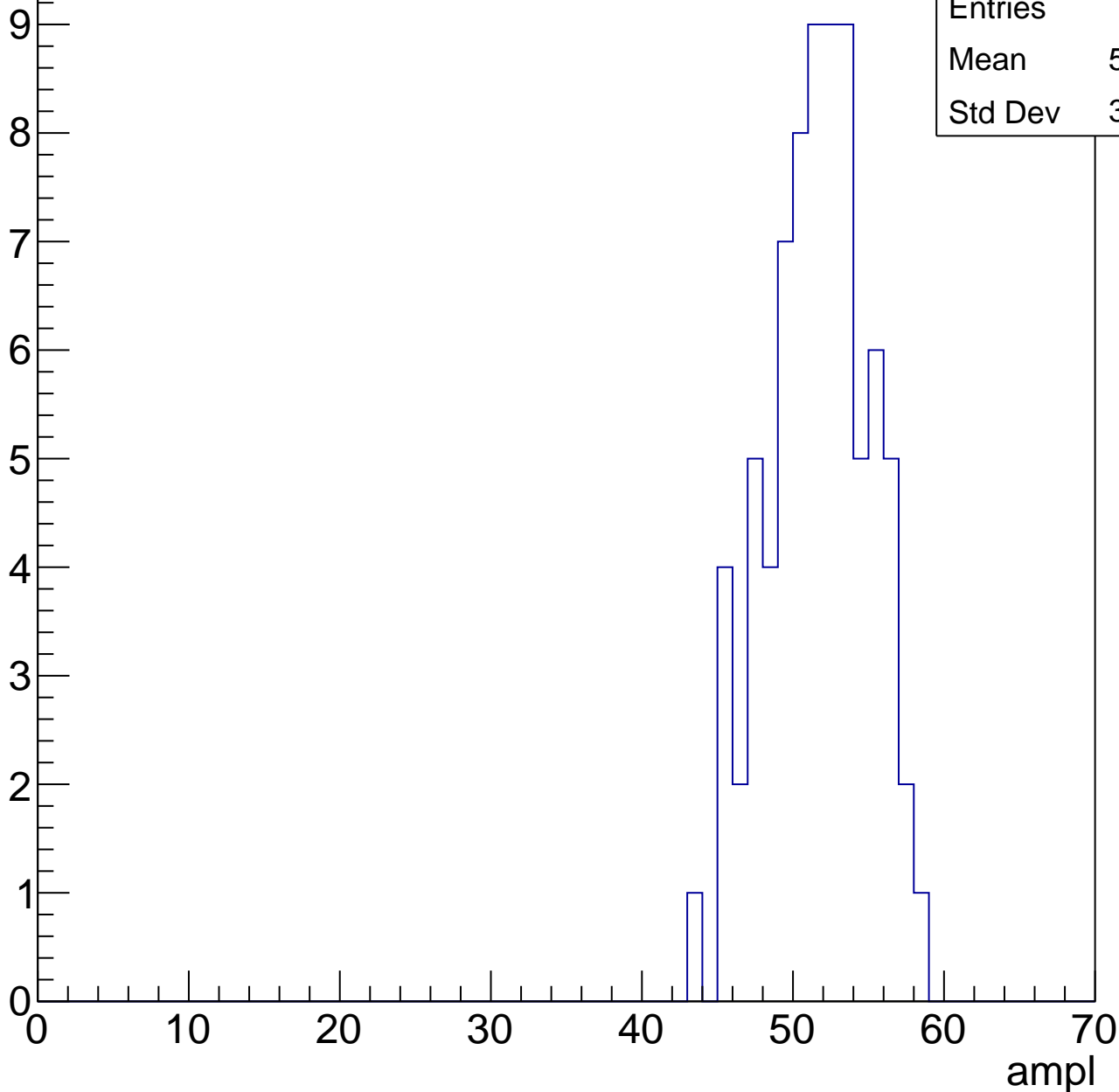


# B0L001S, U24-ch23, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	77
Mean	51.18
Std Dev	3.302

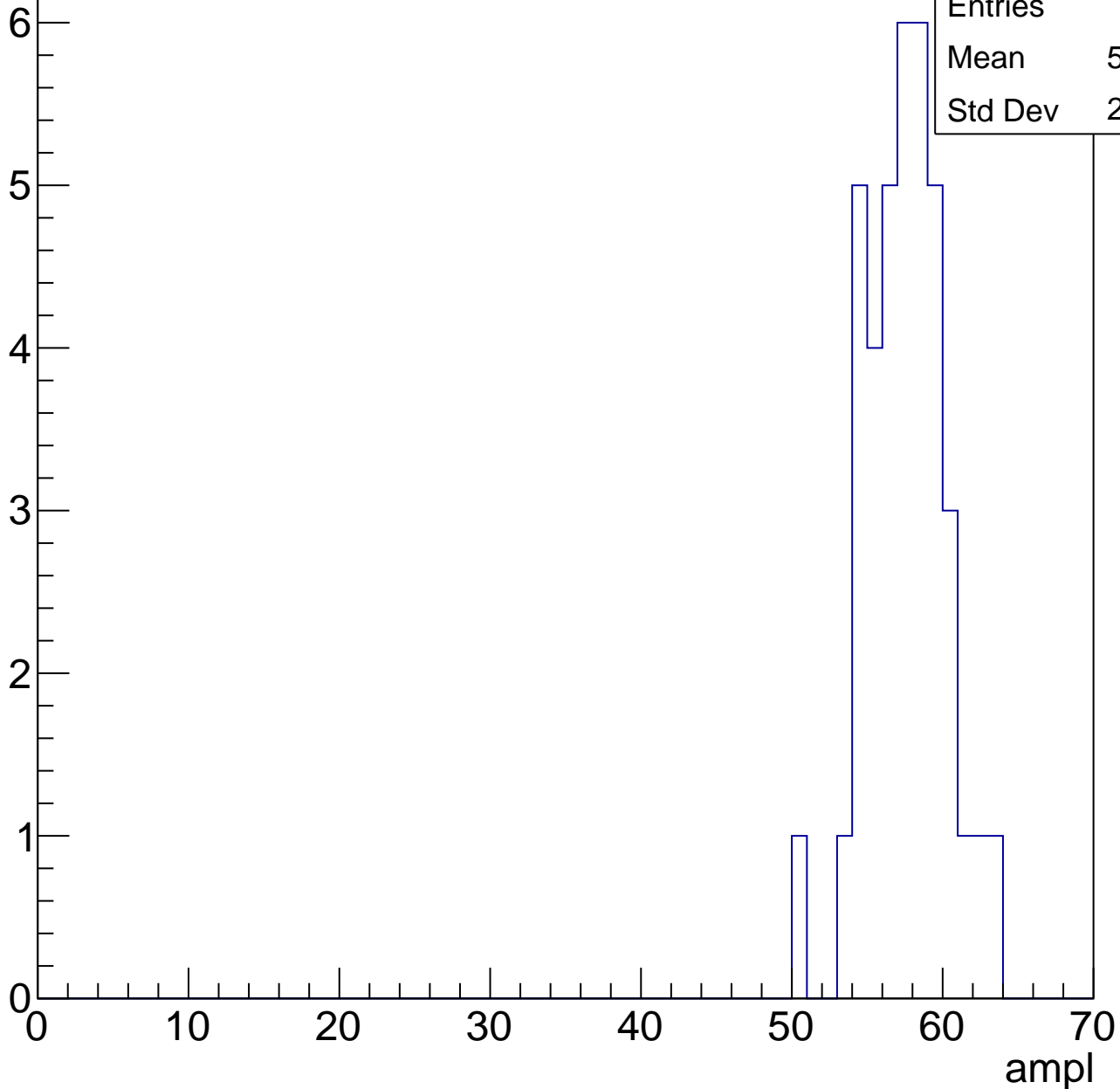


# B0L001S, U24-ch23, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	39
Mean	57.03
Std Dev	2.587

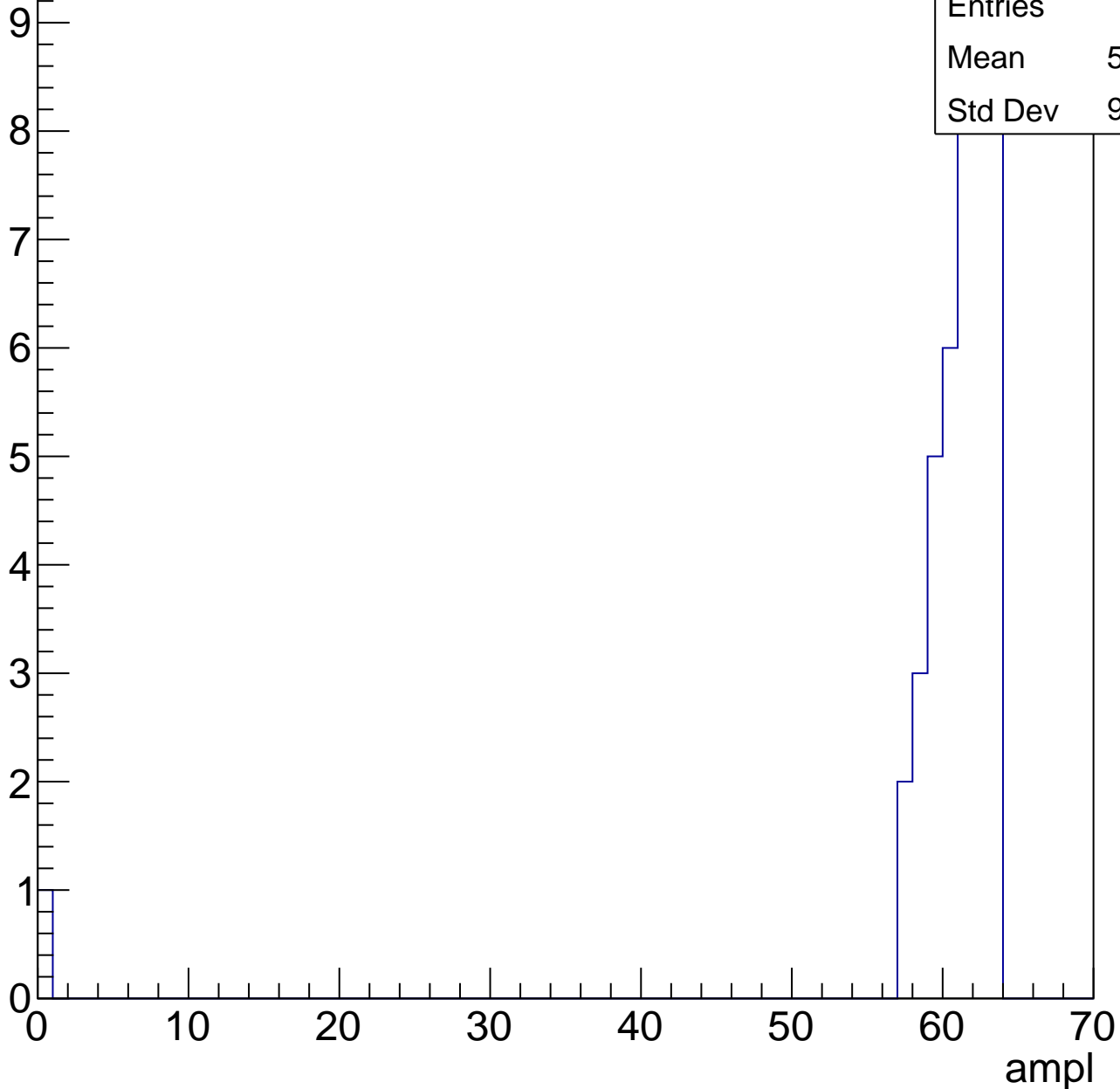


# B0L001S, U24-ch23, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	42
Mean	59.33
Std Dev	9.423



# B0L001S, U24-ch23, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch23, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U24-ch24, adc0

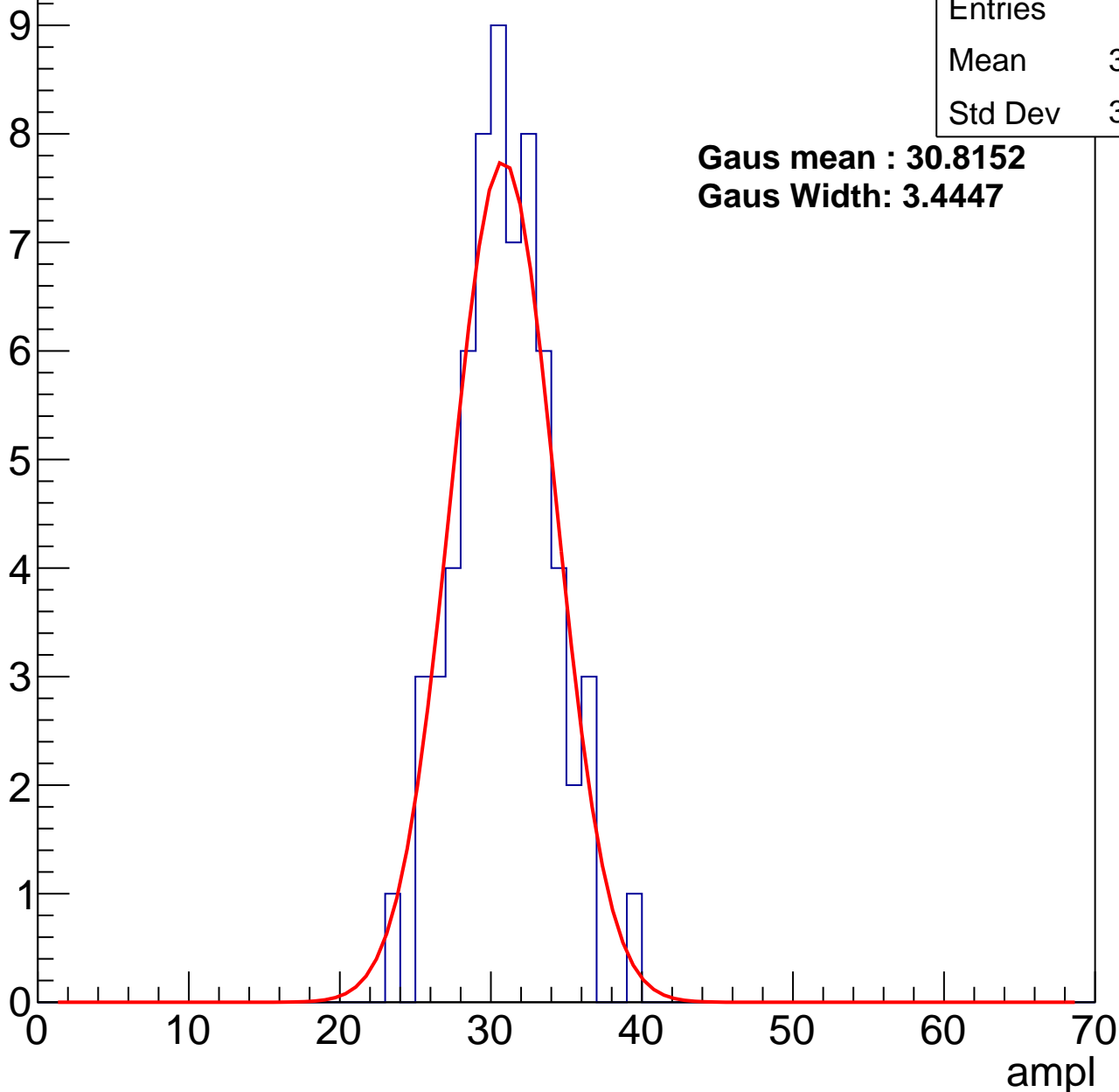
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	30.43
Std Dev	3.098

**Gaus mean : 30.8152**

**Gaus Width: 3.4447**



# B0L001S, U24-ch24, adc1

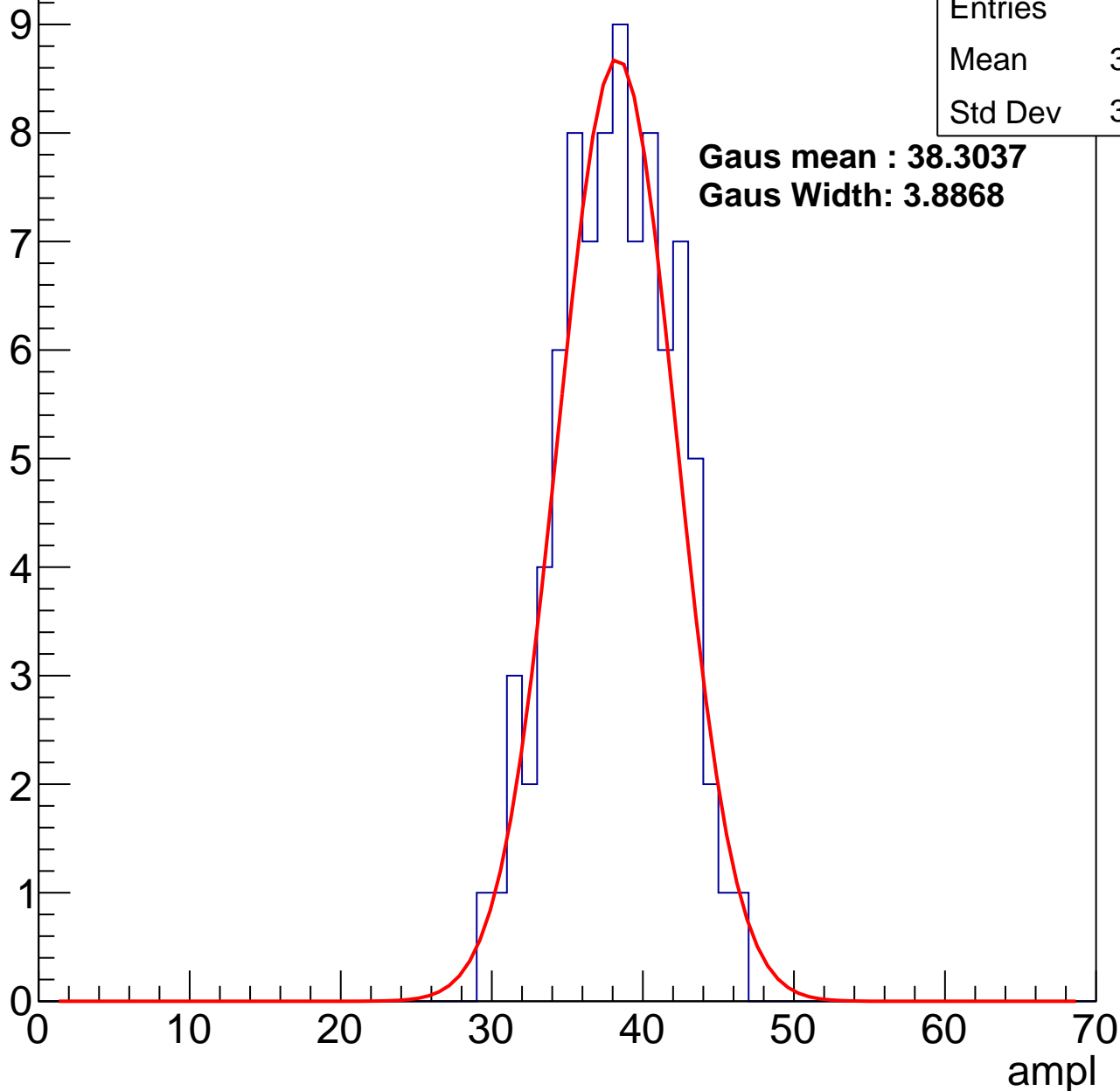
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	86
Mean	37.78
Std Dev	3.702

**Gaus mean : 38.3037**

**Gaus Width: 3.8868**



# B0L001S, U24-ch24, adc2

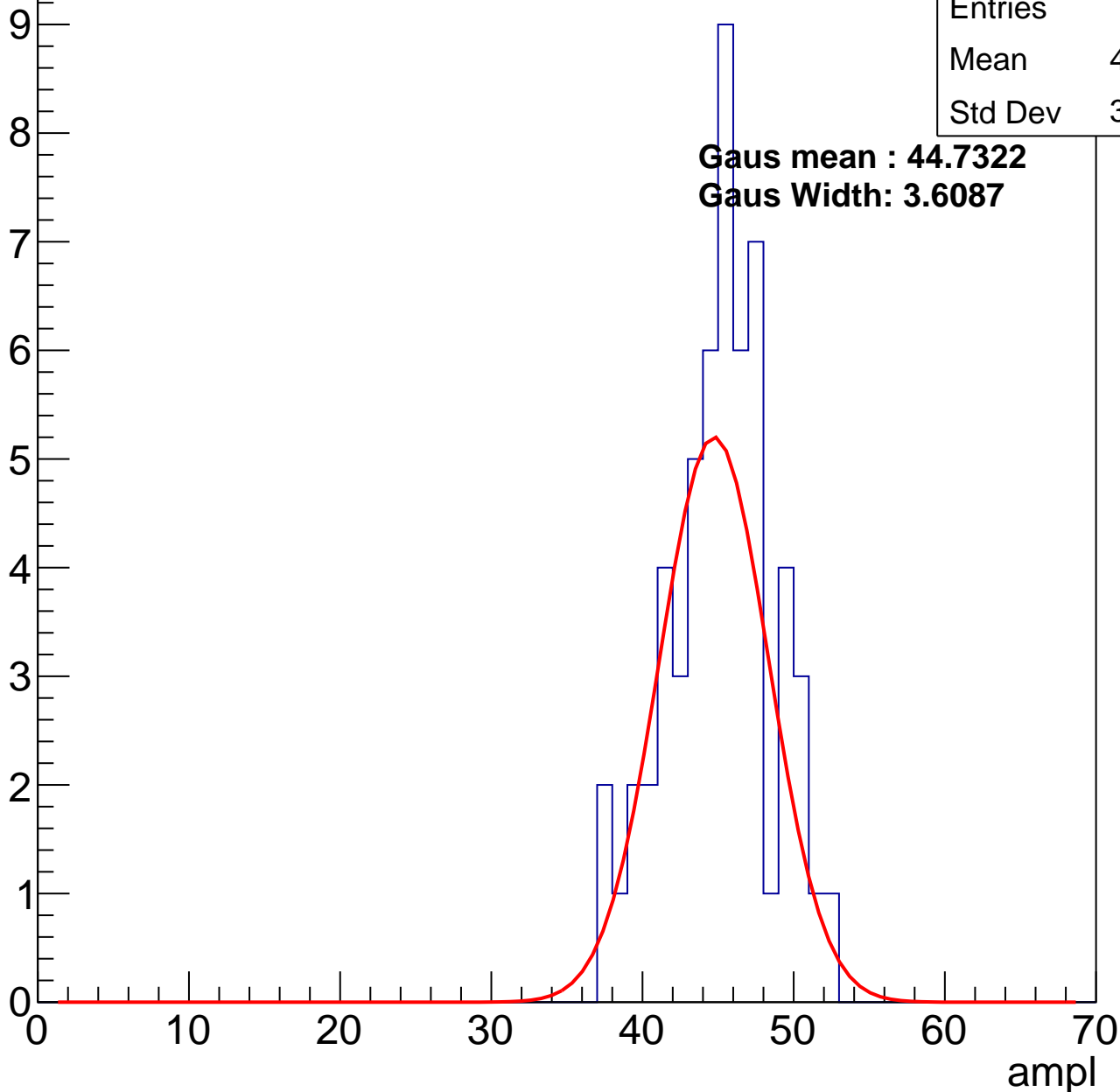
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	44.67
Std Dev	3.445

**Gaus mean : 44.7322**

**Gaus Width: 3.6087**

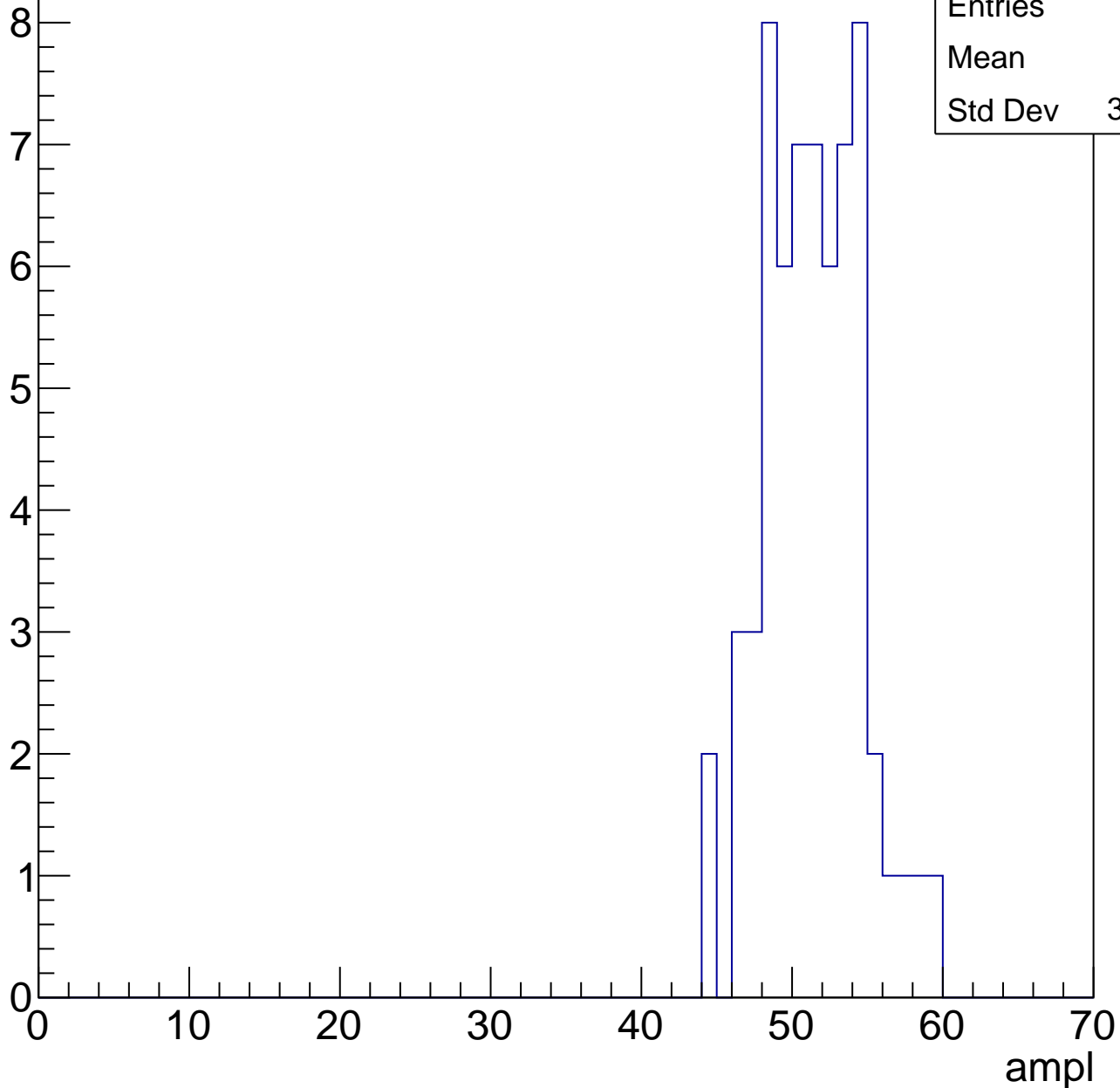


# B0L001S, U24-ch24, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	50.9
Std Dev	3.176

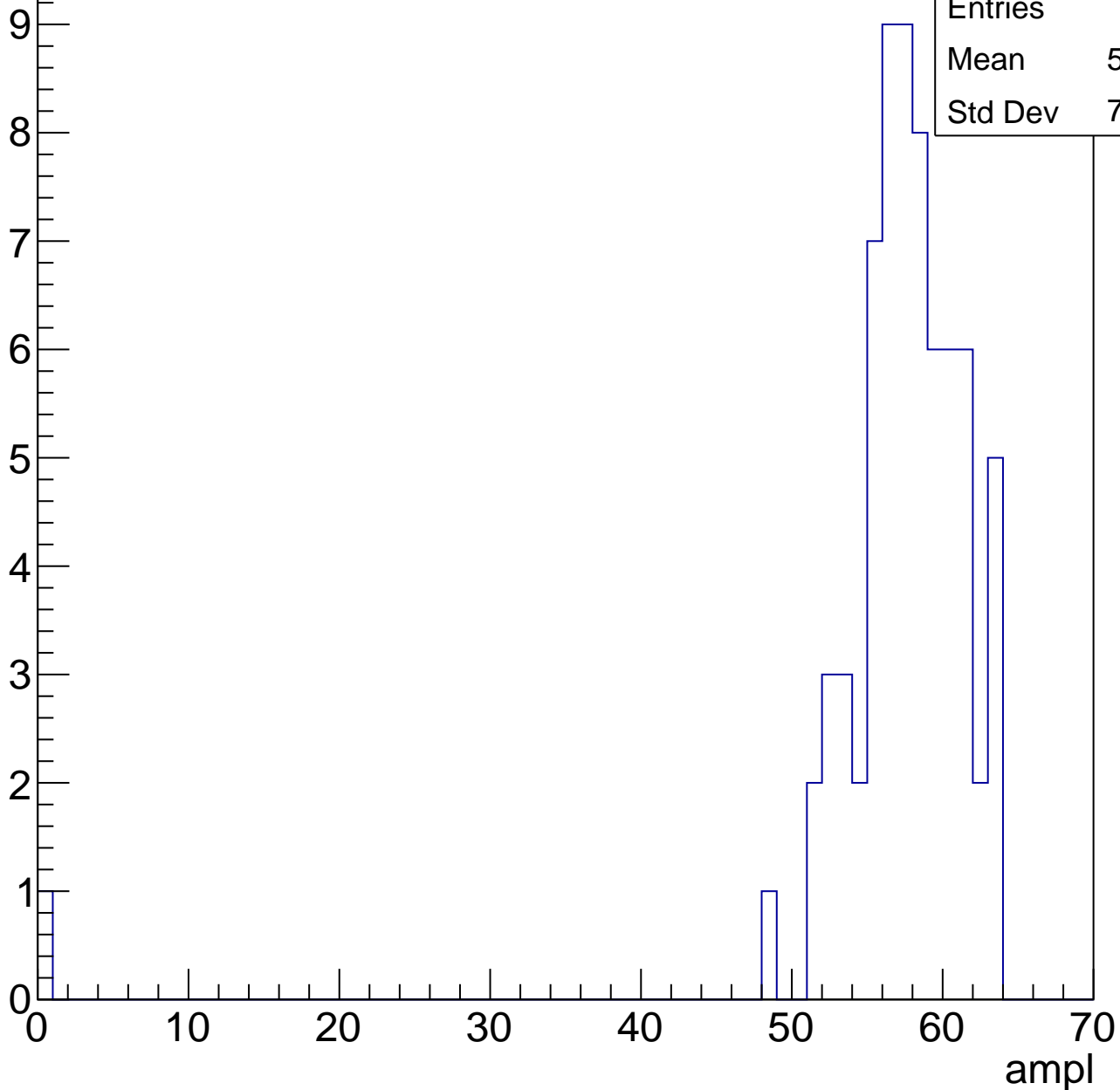


# B0L001S, U24-ch24, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	56.54
Std Dev	7.538

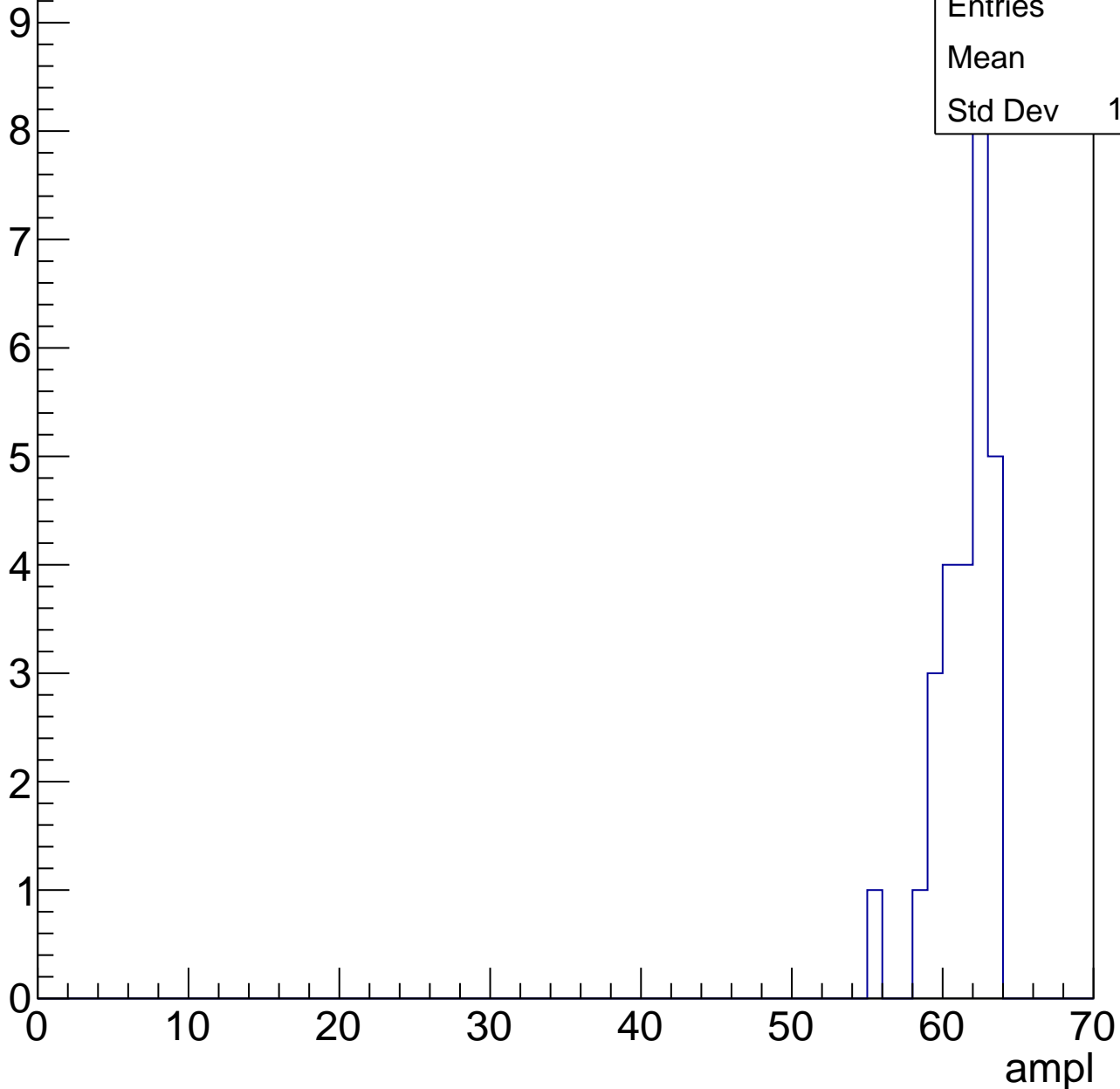


# B0L001S, U24-ch24, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

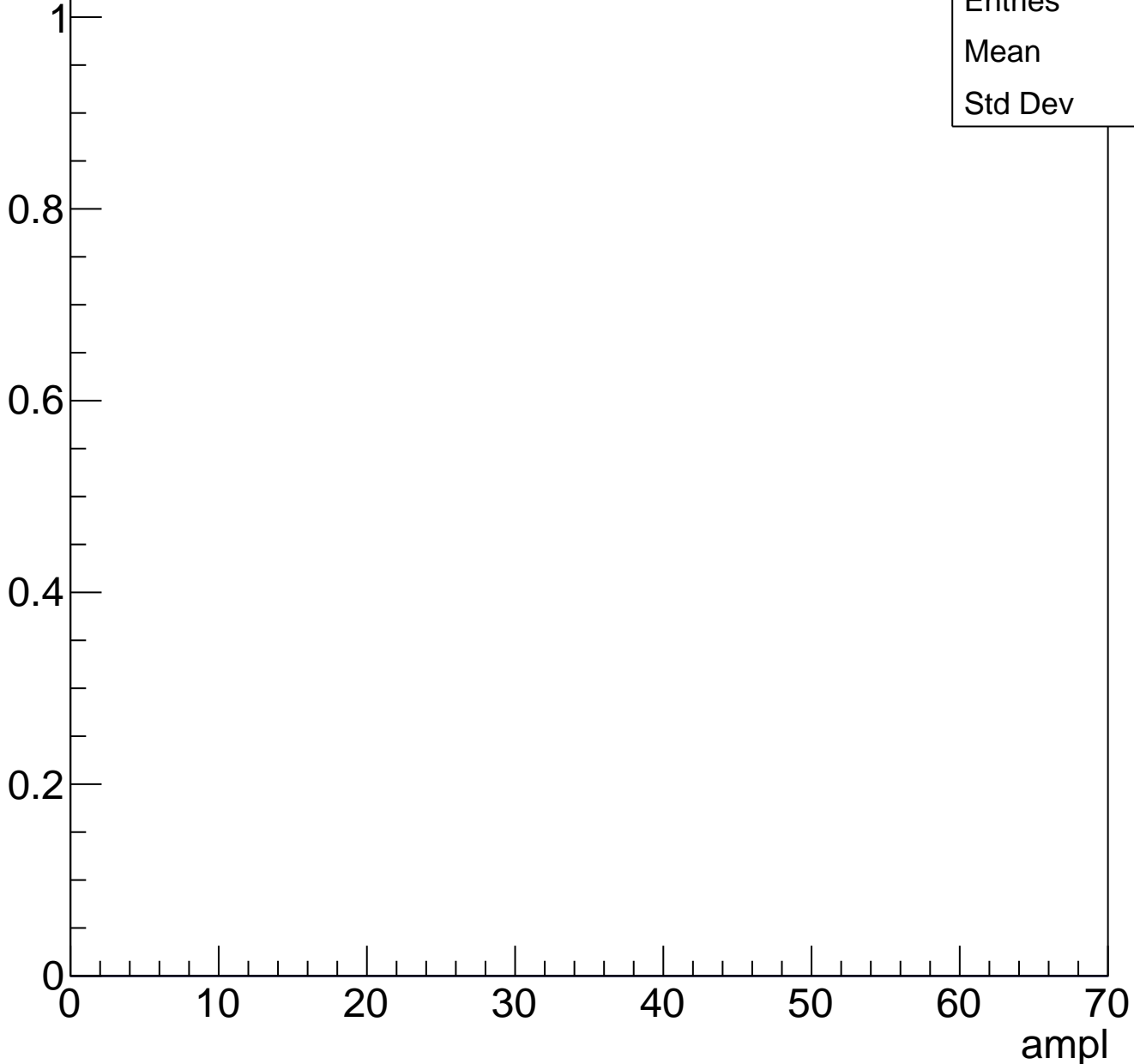
Entries	27
Mean	61
Std Dev	1.826



# B0L001S, U24-ch24, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U24-ch24, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L001S, U24-ch25, adc0

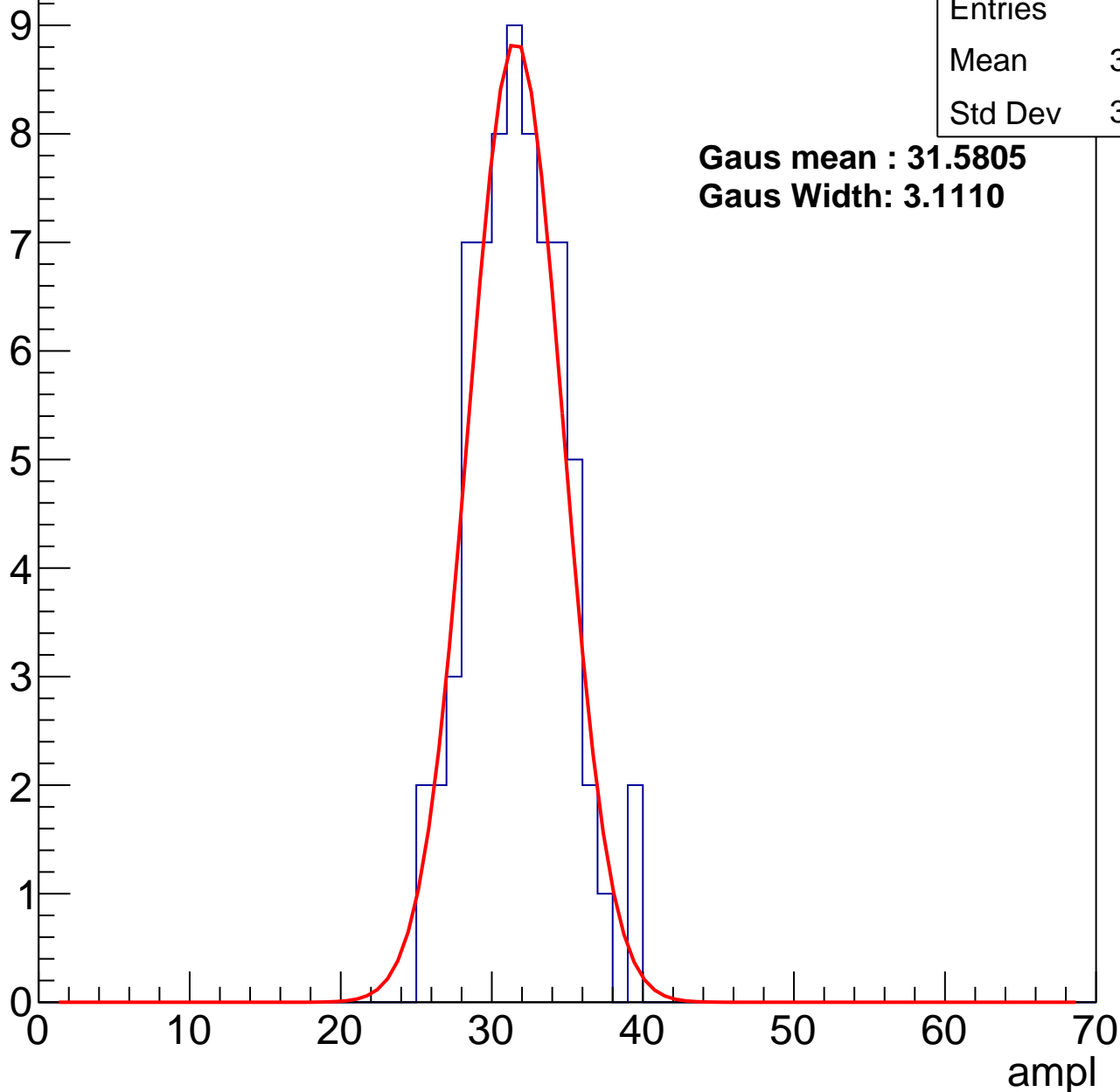
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	31.26
Std Dev	3.064

**Gaus mean : 31.5805**

**Gaus Width: 3.1110**



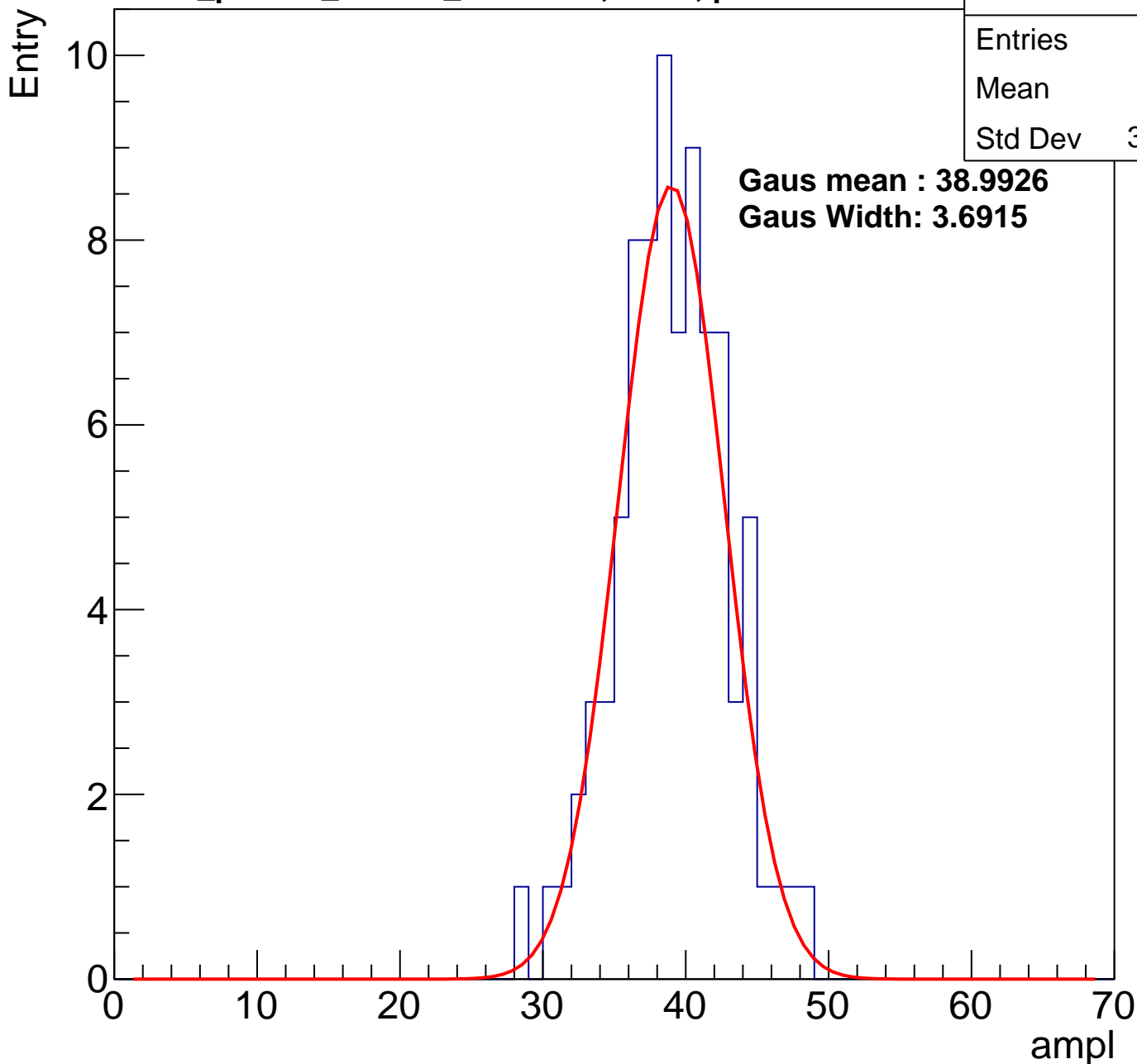
# B0L001S, U24-ch25, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	84
Mean	38.6
Std Dev	3.827

**Gaus mean : 38.9926**

**Gaus Width: 3.6915**



# B0L001S, U24-ch25, adc2

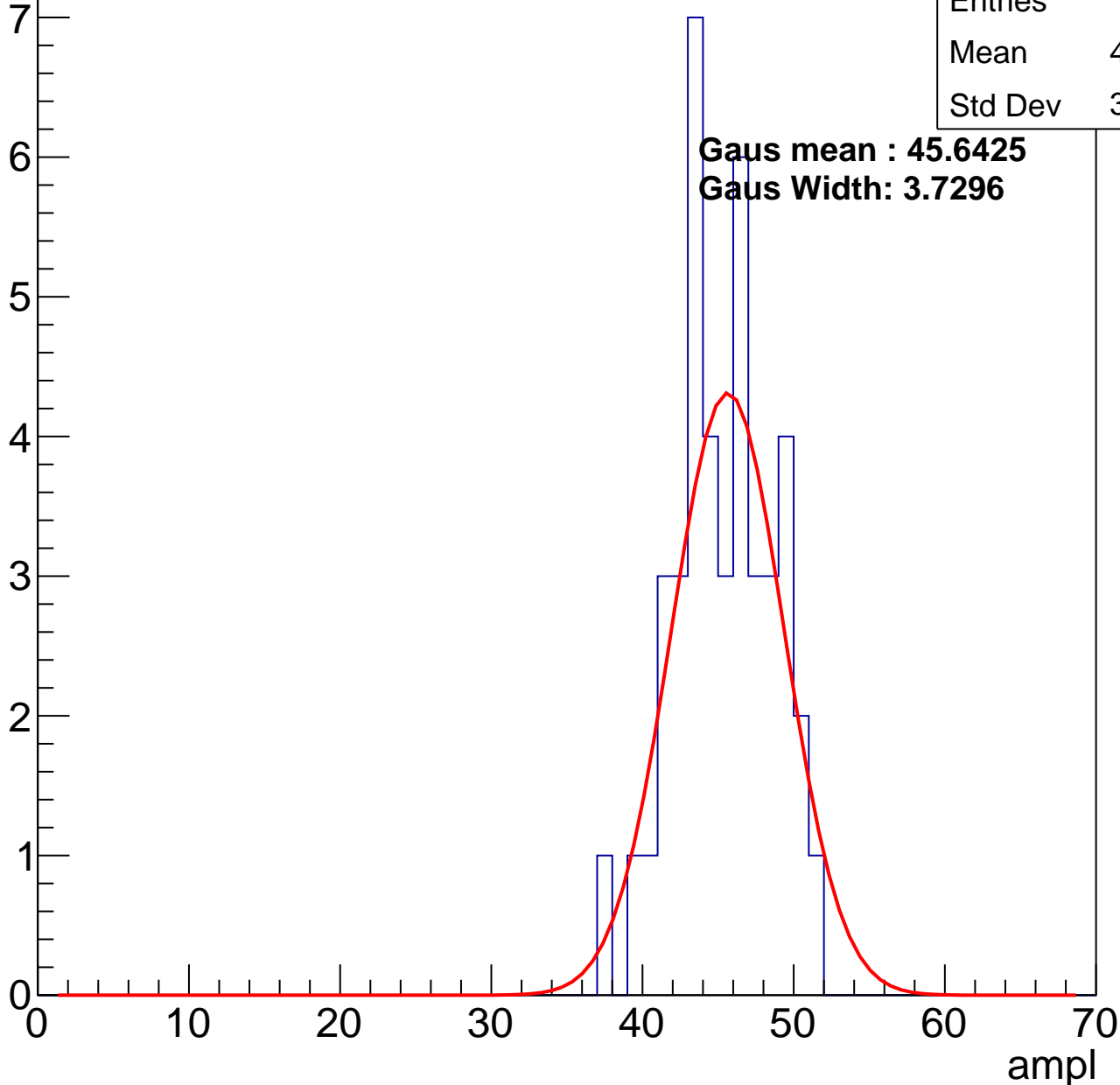
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	42
Mean	44.88
Std Dev	3.186

**Gaus mean : 45.6425**

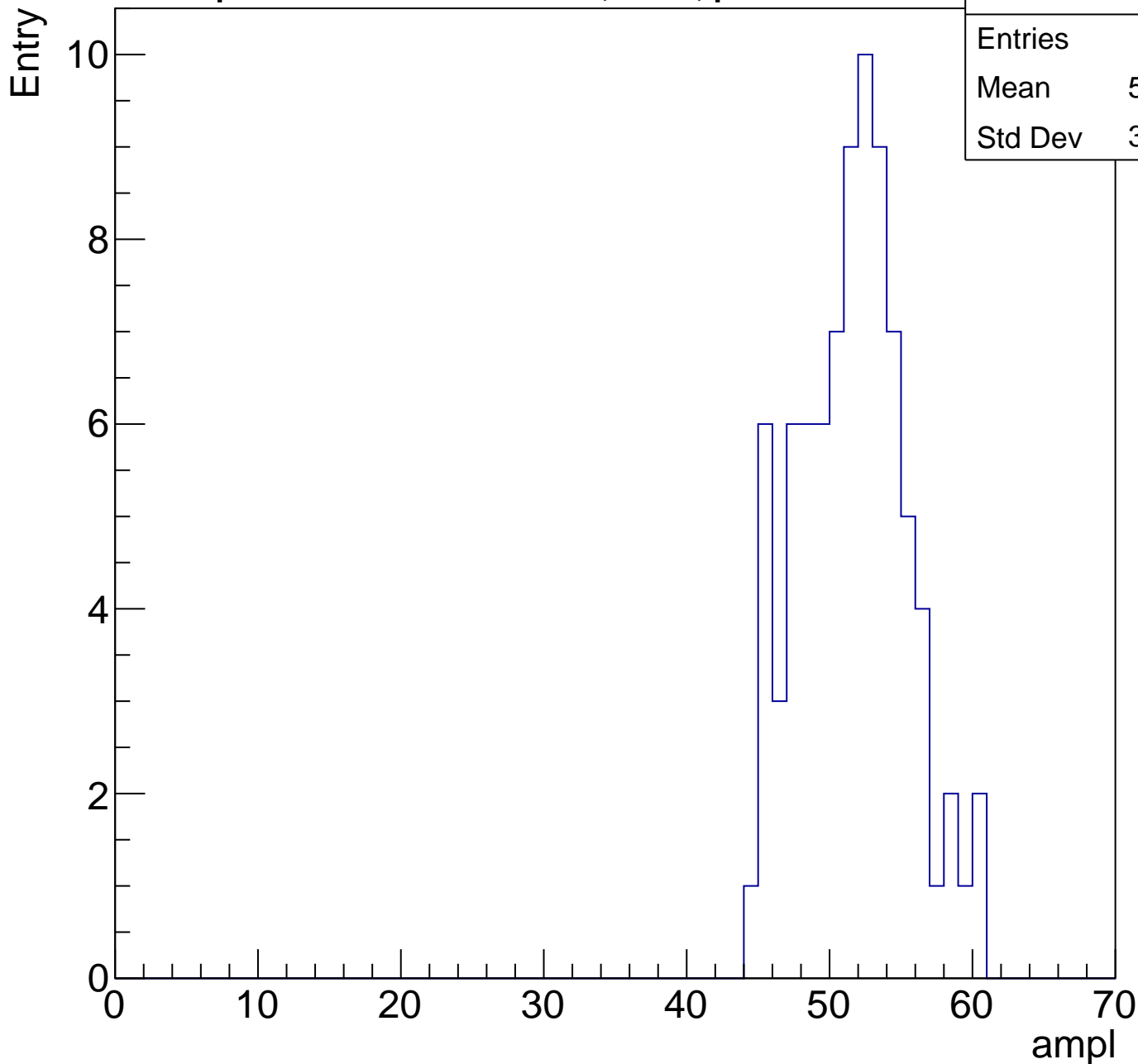
**Gaus Width: 3.7296**



# B0L001S, U24-ch25, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	85
Mean	51.19
Std Dev	3.705

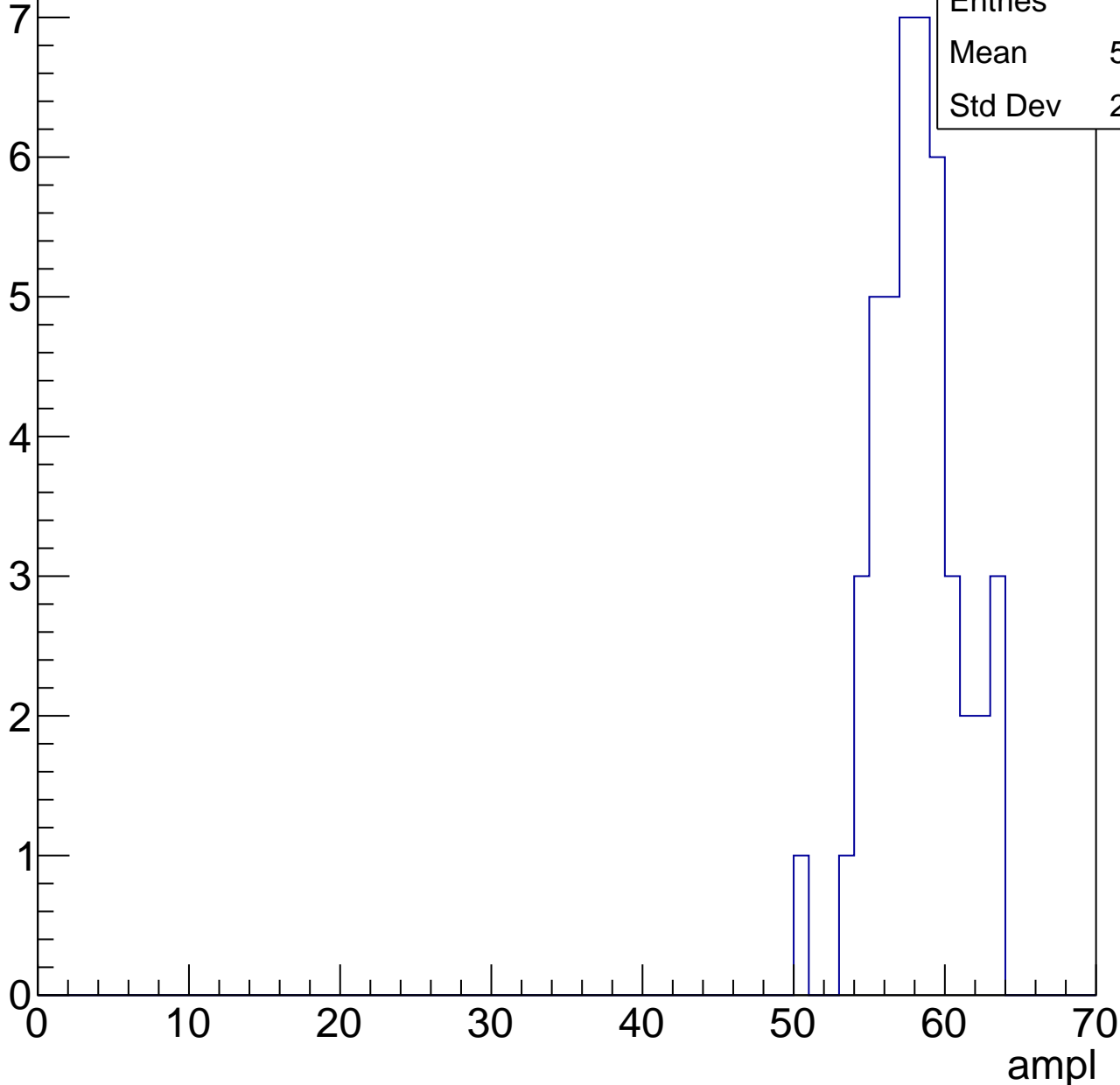


# B0L001S, U24-ch25, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	45
Mean	57.64
Std Dev	2.774

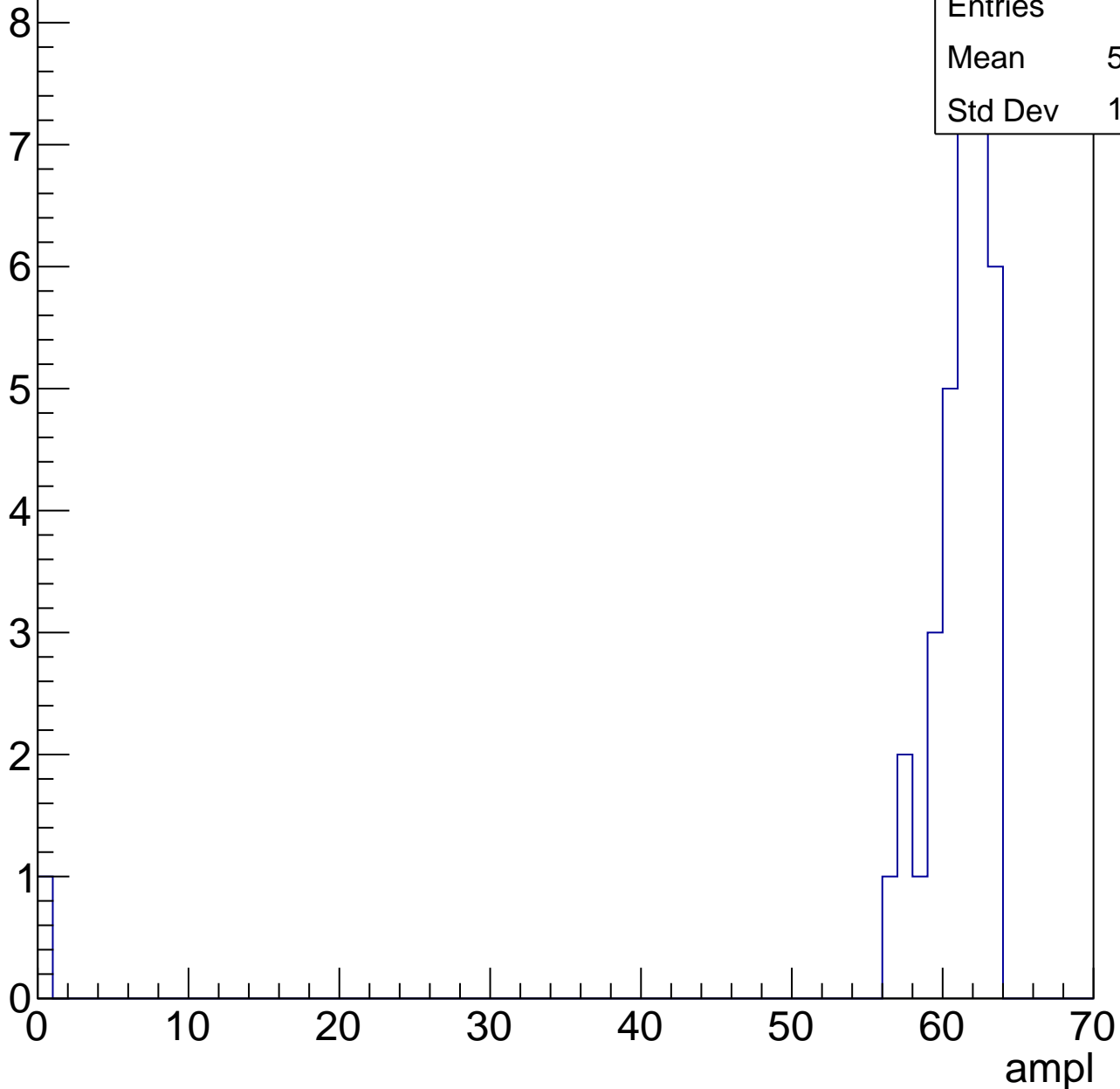


# B0L001S, U24-ch25, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	35
Mean	59.06
Std Dev	10.29



# B0L001S, U24-ch25, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch25, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U24-ch26, adc0

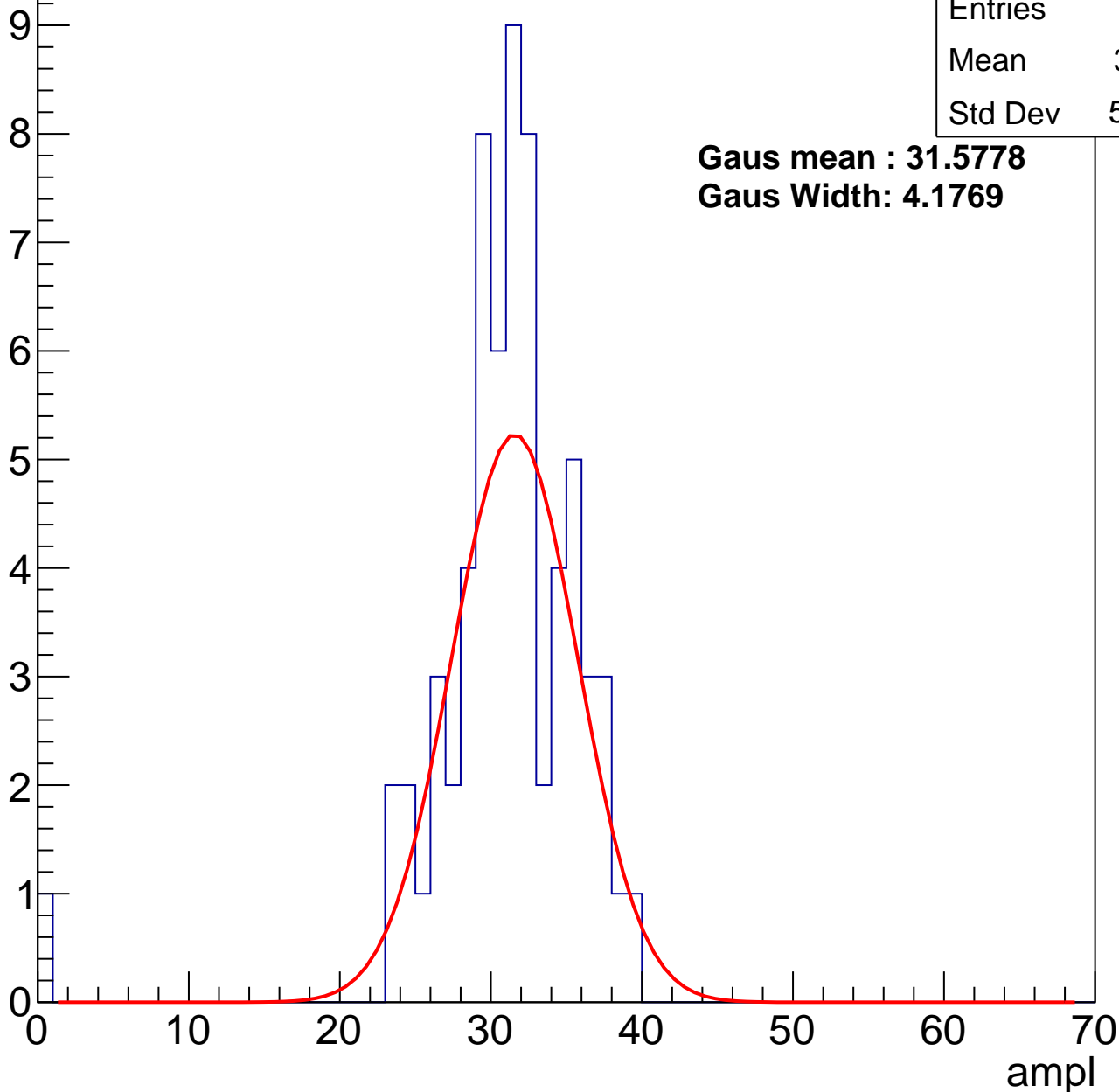
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	30.51
Std Dev	5.286

**Gaus mean : 31.5778**

**Gaus Width: 4.1769**



# B0L001S, U24-ch26, adc1

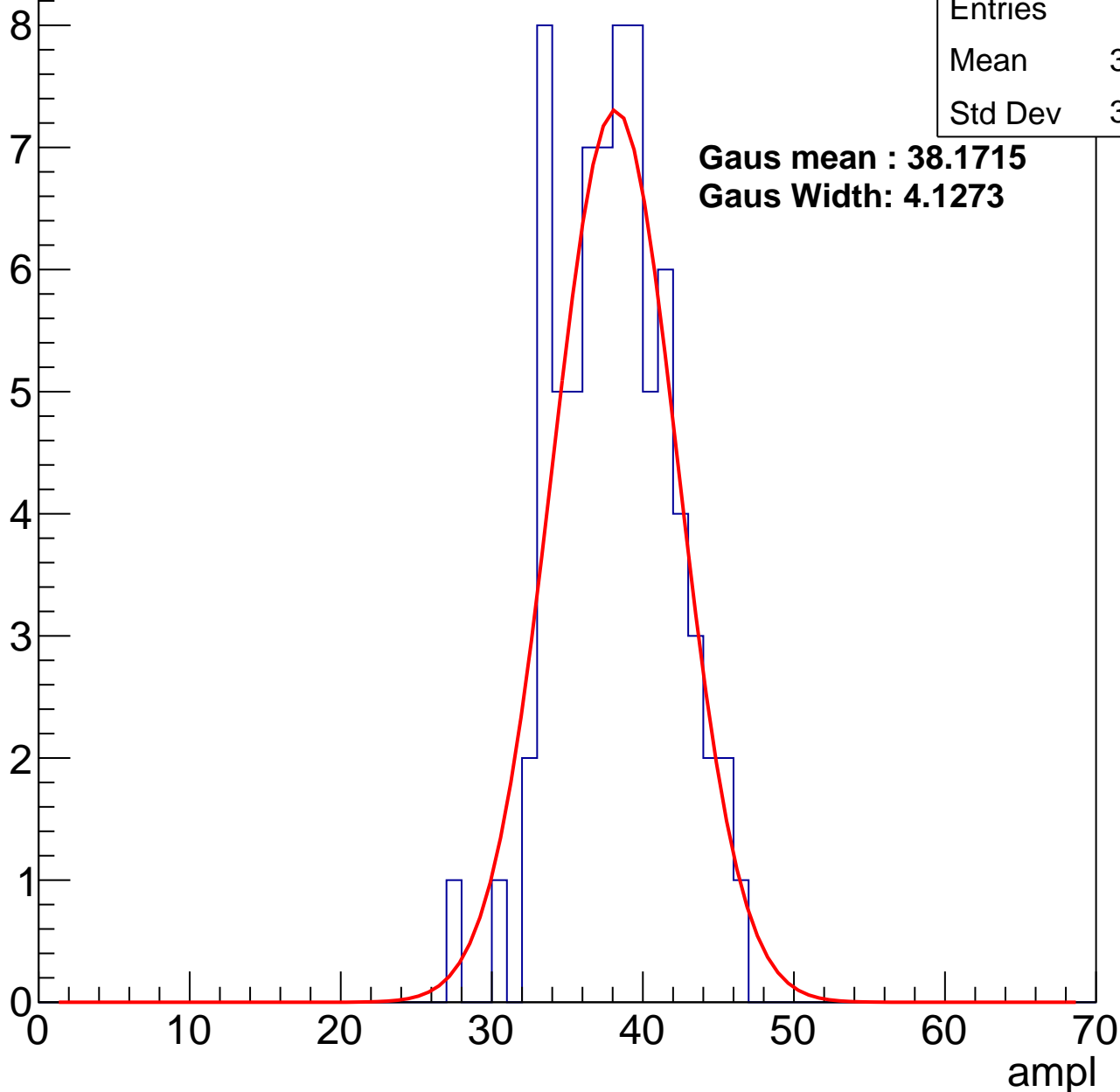
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	75
Mean	37.65
Std Dev	3.765

**Gaus mean : 38.1715**

**Gaus Width: 4.1273**



# B0L001S, U24-ch26, adc2

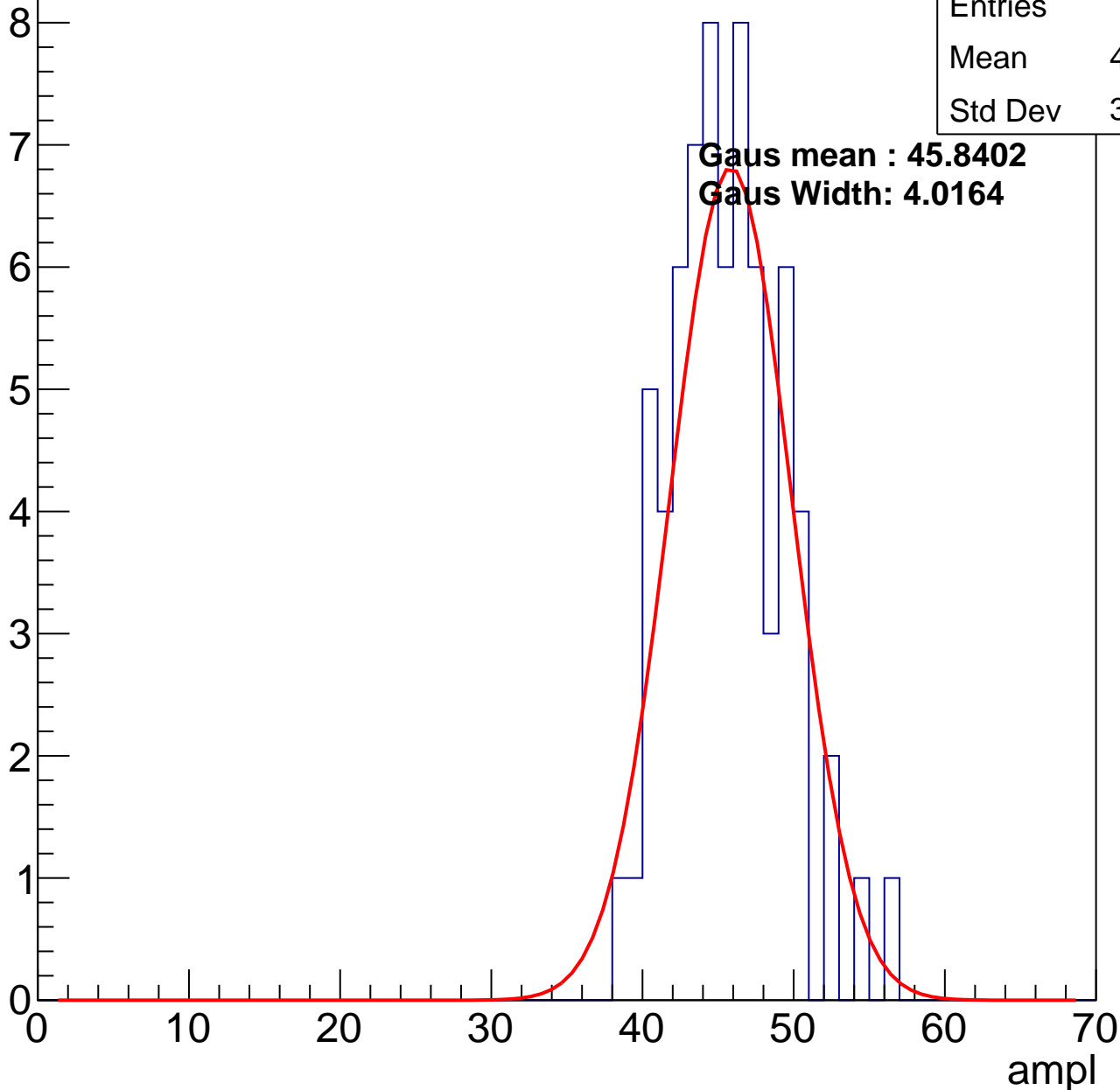
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	45.19
Std Dev	3.645

**Gaus mean : 45.8402**

**Gaus Width: 4.0164**



# B0L001S, U24-ch26, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	55
Mean	50.87
Std Dev	2.961

Entry

10

8

6

4

2

0

0

10

20

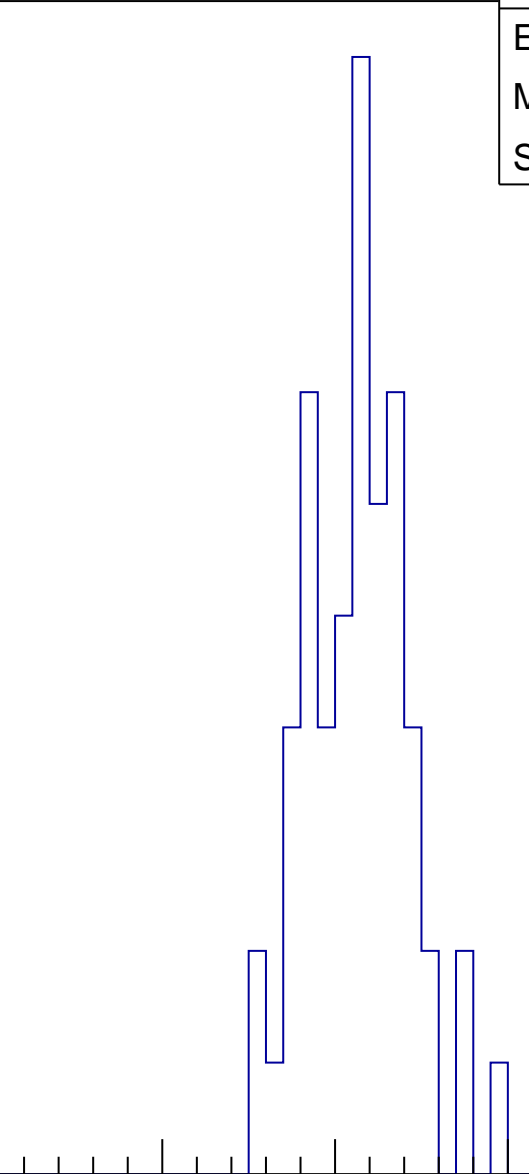
30

40

50

60

ampl

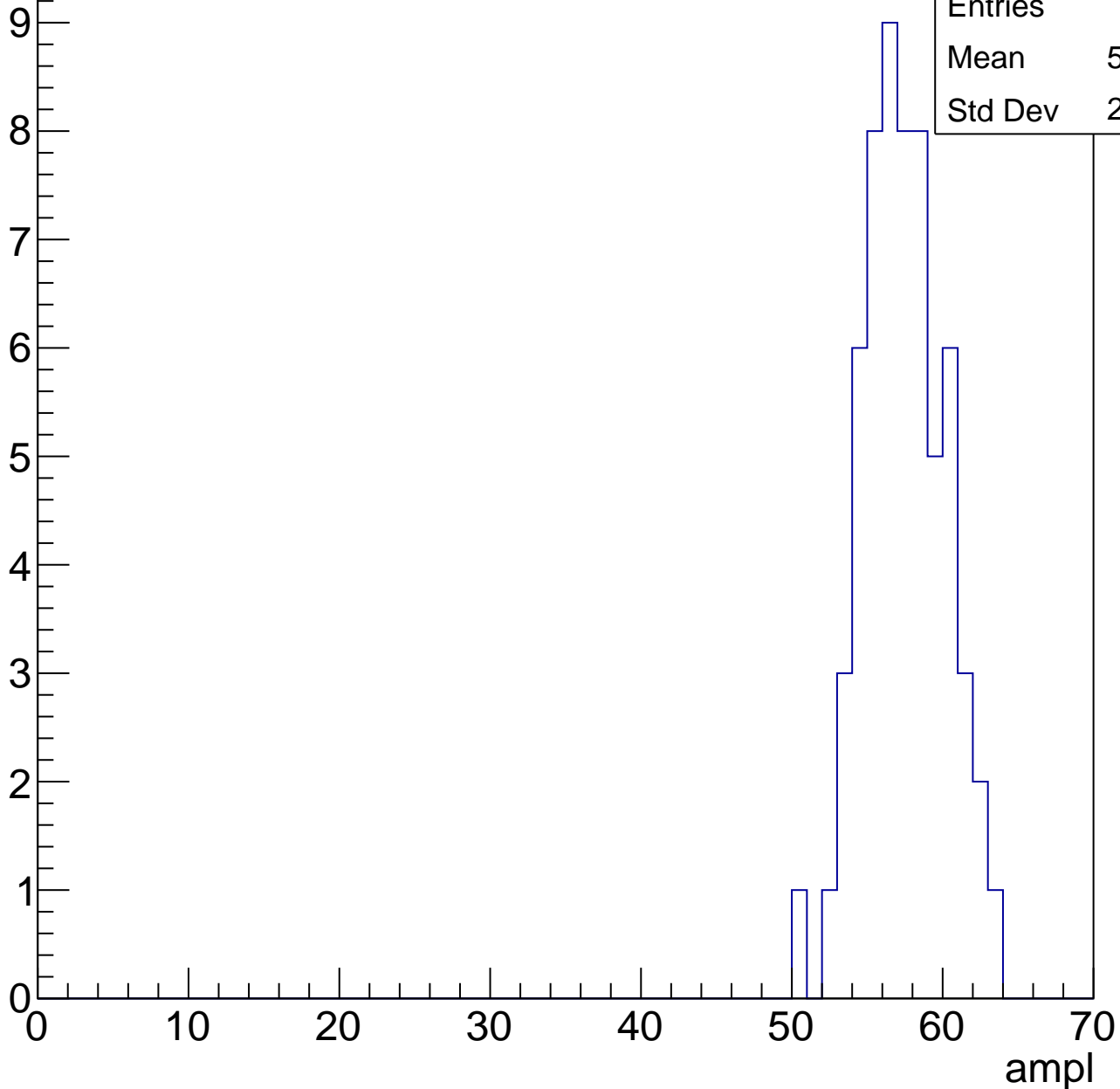


# B0L001S, U24-ch26, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	56.95
Std Dev	2.664

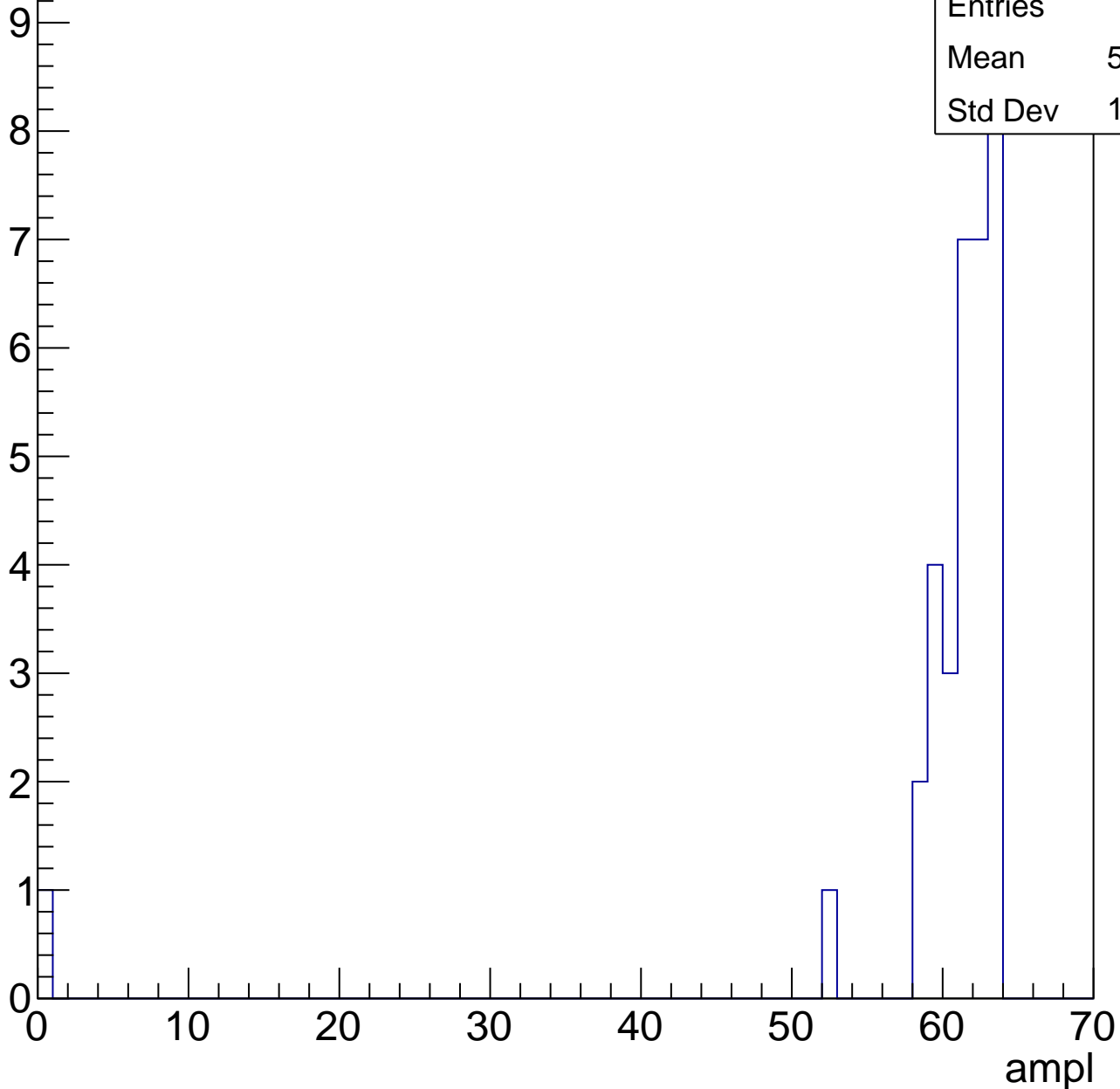


# B0L001S, U24-ch26, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	34
Mean	59.18
Std Dev	10.53



# B0L001S, U24-ch26, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch26, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U24-ch27, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	53
Mean	31.21
Std Dev	2.757

**Gaus mean : 31.8853**

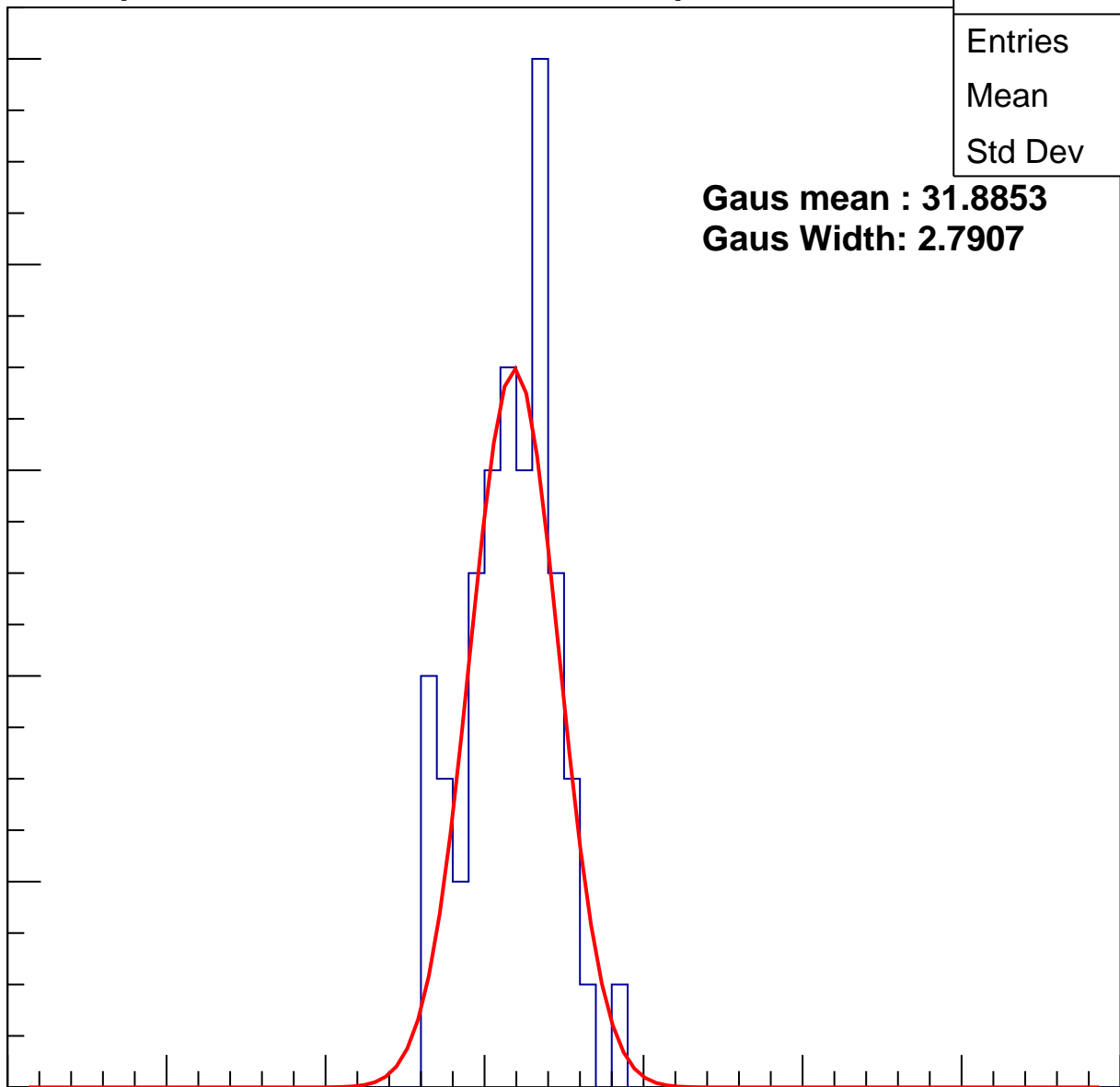
**Gaus Width: 2.7907**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U24-ch27, adc1

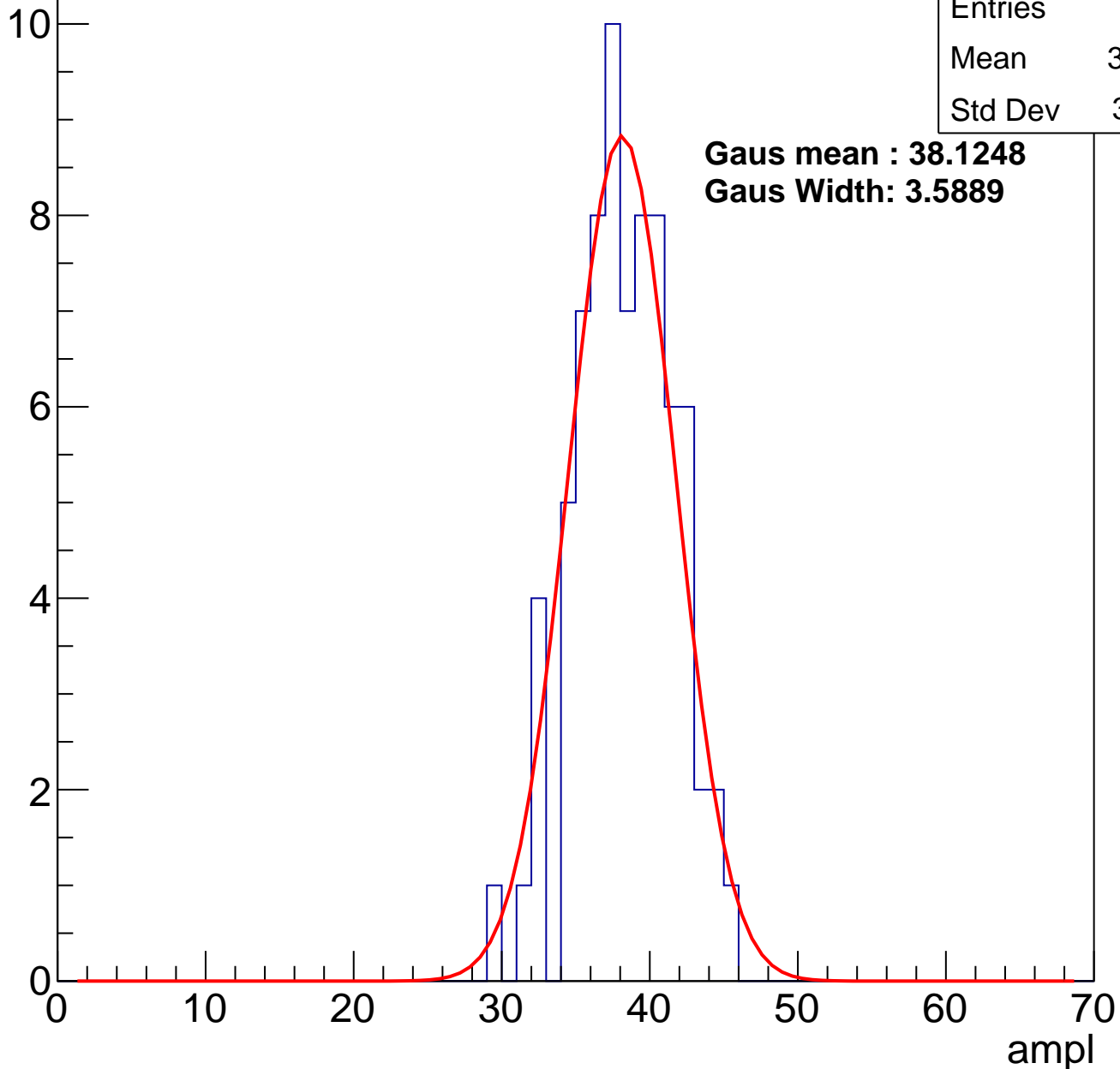
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	76
Mean	37.84
Std Dev	3.281

**Gaus mean : 38.1248**

**Gaus Width: 3.5889**

Entry



# B0L001S, U24-ch27, adc2

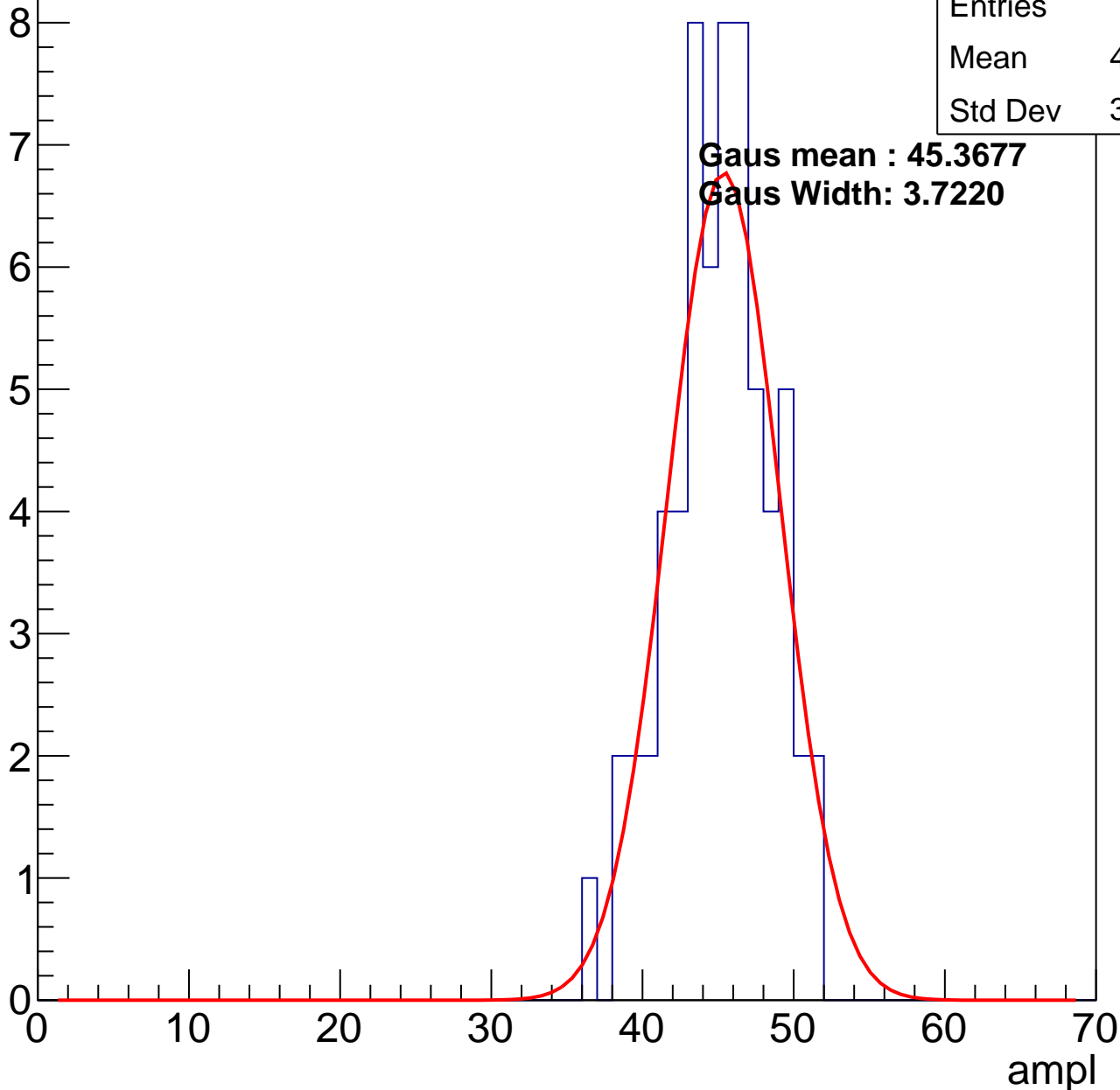
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	44.63
Std Dev	3.325

**Gaus mean : 45.3677**

**Gaus Width: 3.7220**

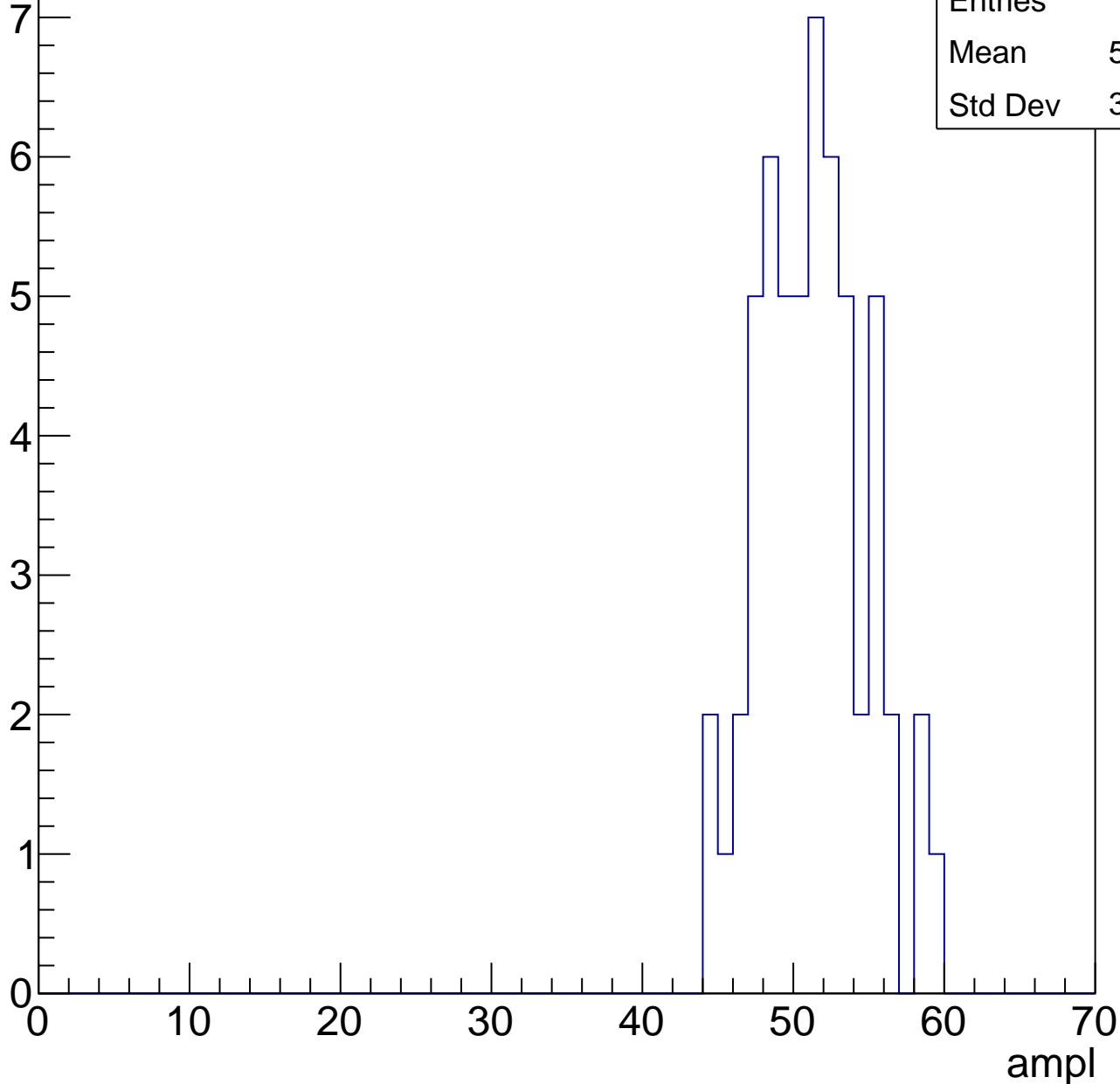


# B0L001S, U24-ch27, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

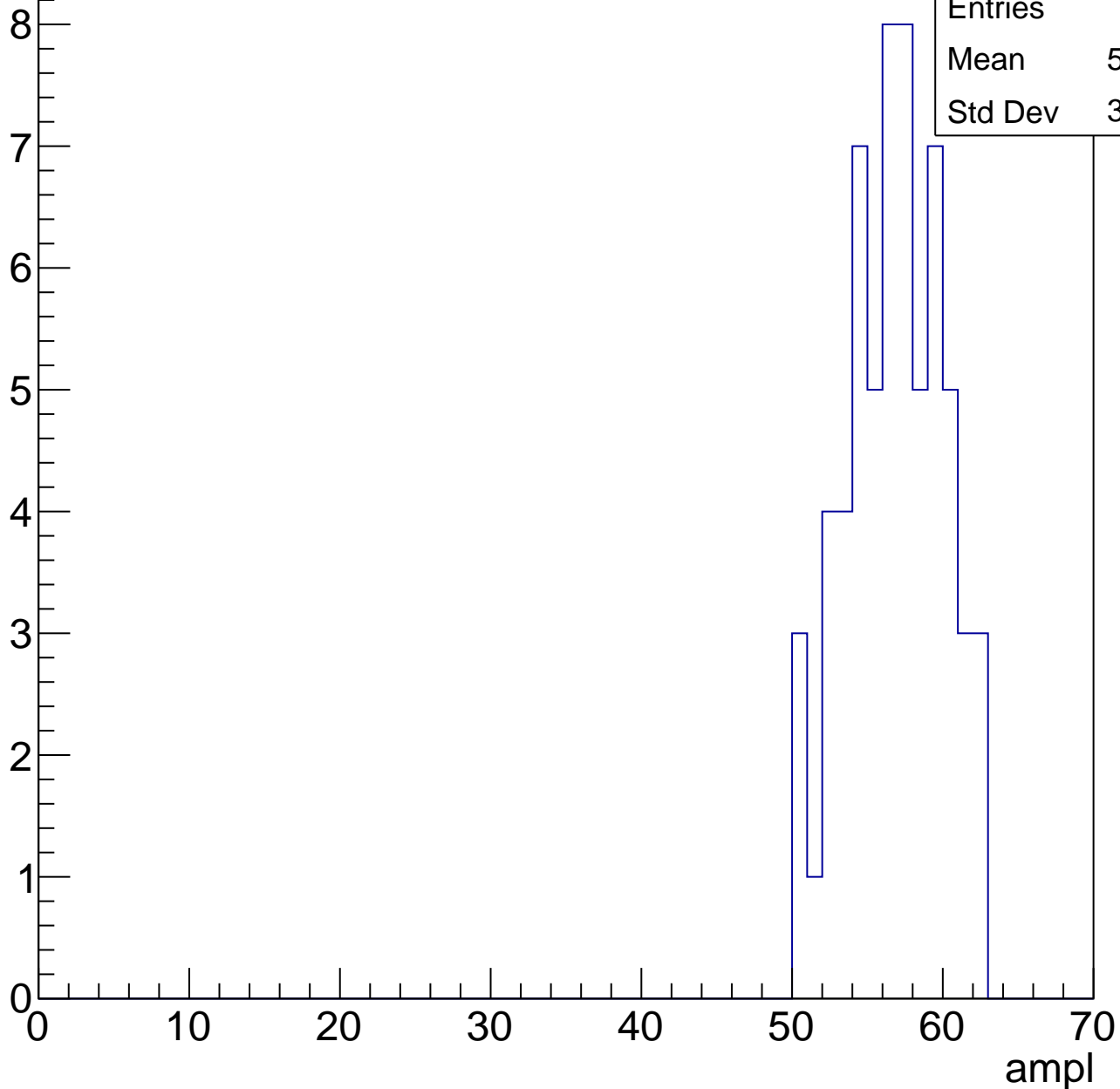
Entries	56
Mean	50.84
Std Dev	3.478



# B0L001S, U24-ch27, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



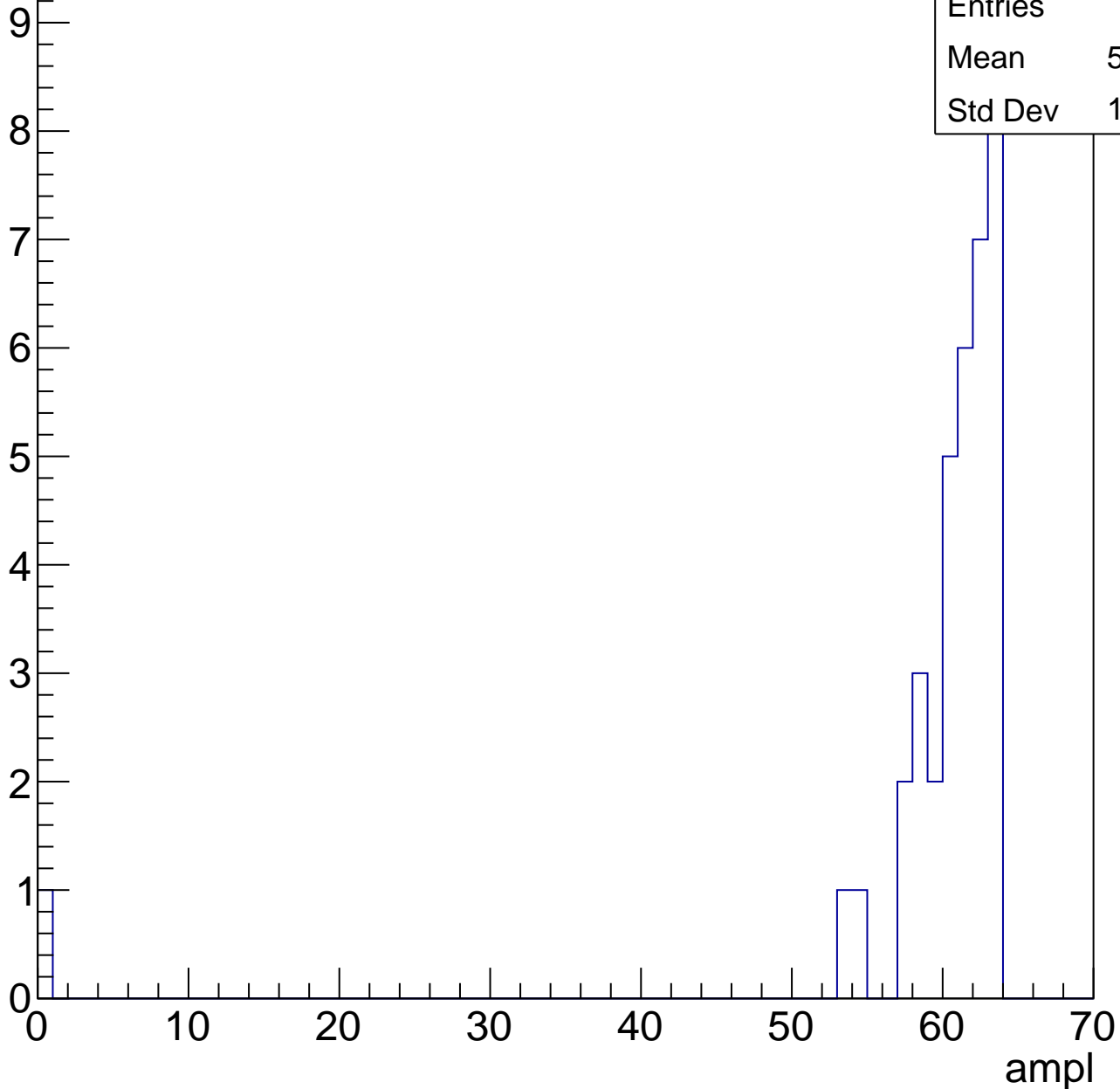
Entries	63
Mean	56.35
Std Dev	3.118

# B0L001S, U24-ch27, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	37
Mean	58.92
Std Dev	10.12



# B0L001S, U24-ch27, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

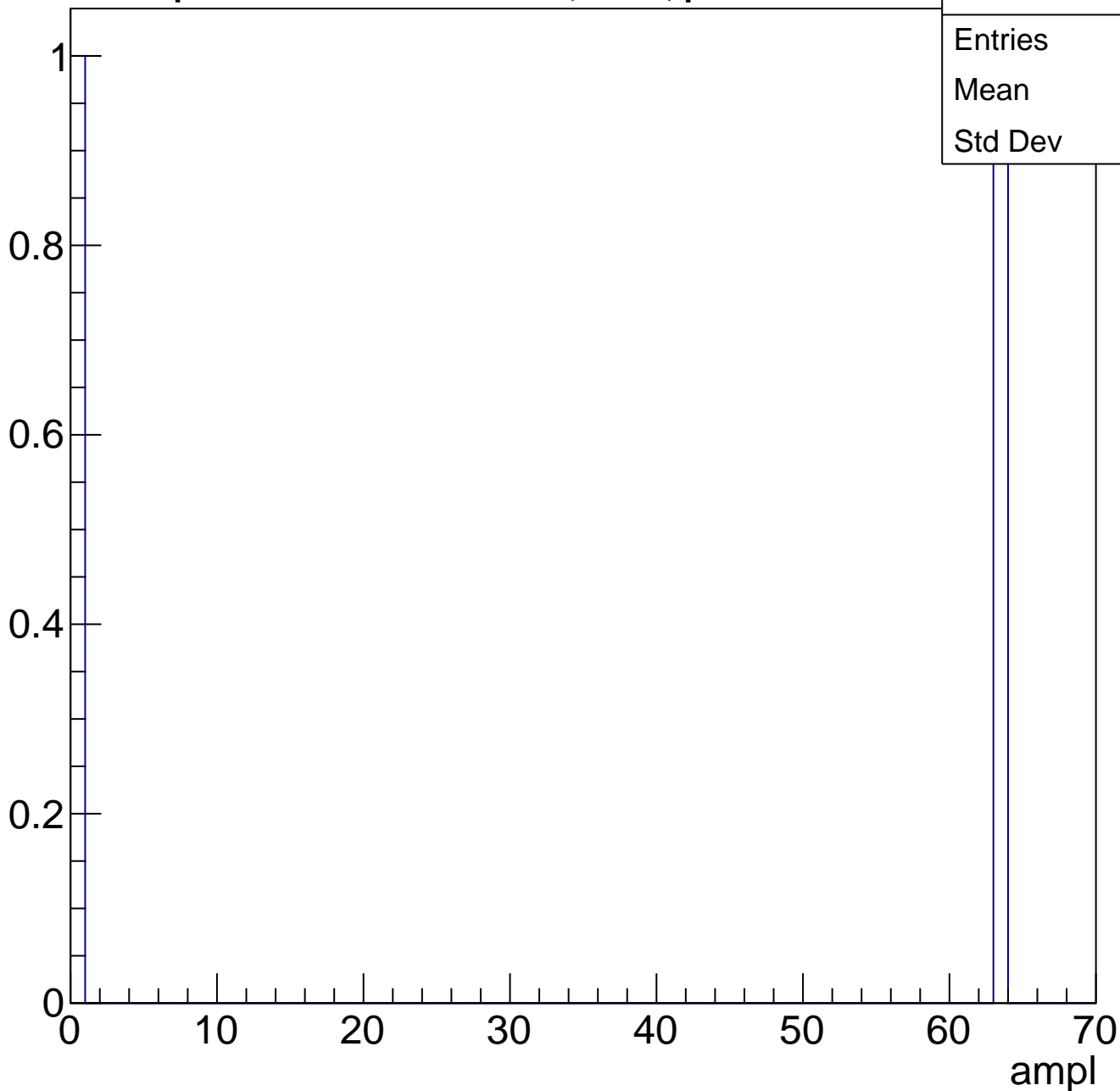




# B0L001S, U24-ch27, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U24-ch28, adc0

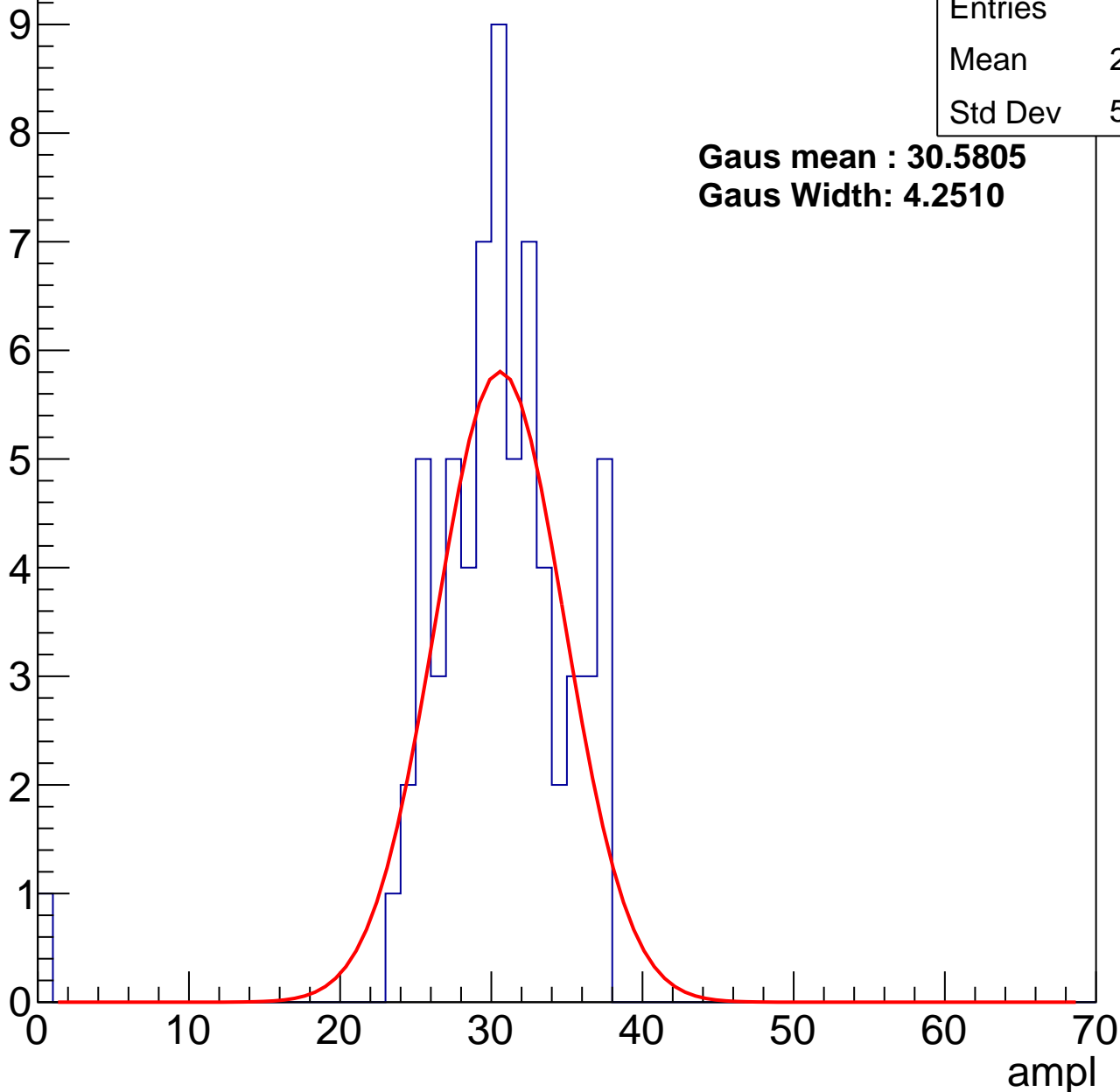
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	29.86
Std Dev	5.207

**Gaus mean : 30.5805**

**Gaus Width: 4.2510**



# B0L001S, U24-ch28, adc1

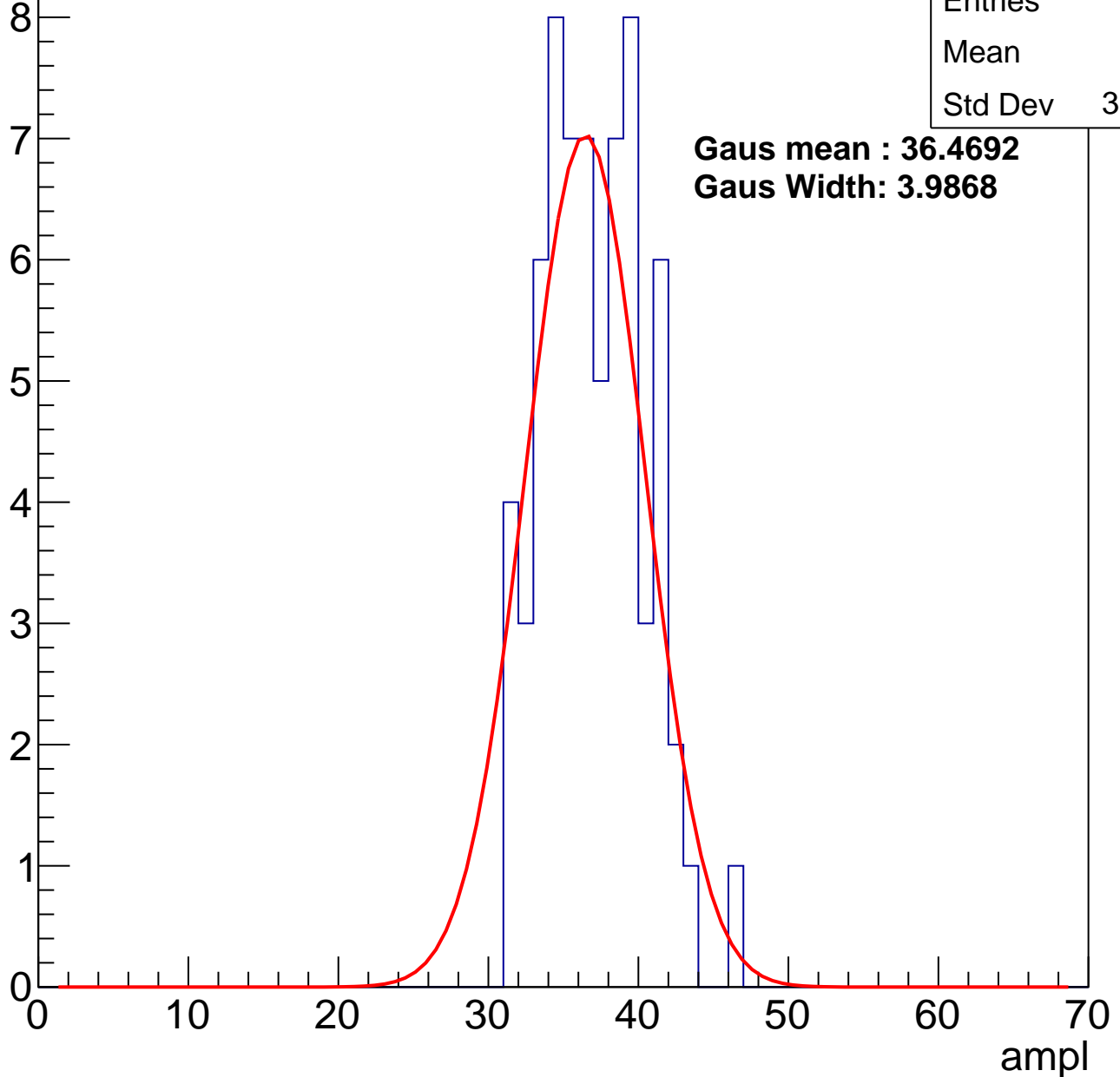
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	36.6
Std Dev	3.299

**Gaus mean : 36.4692**

**Gaus Width: 3.9868**



# B0L001S, U24-ch28, adc2

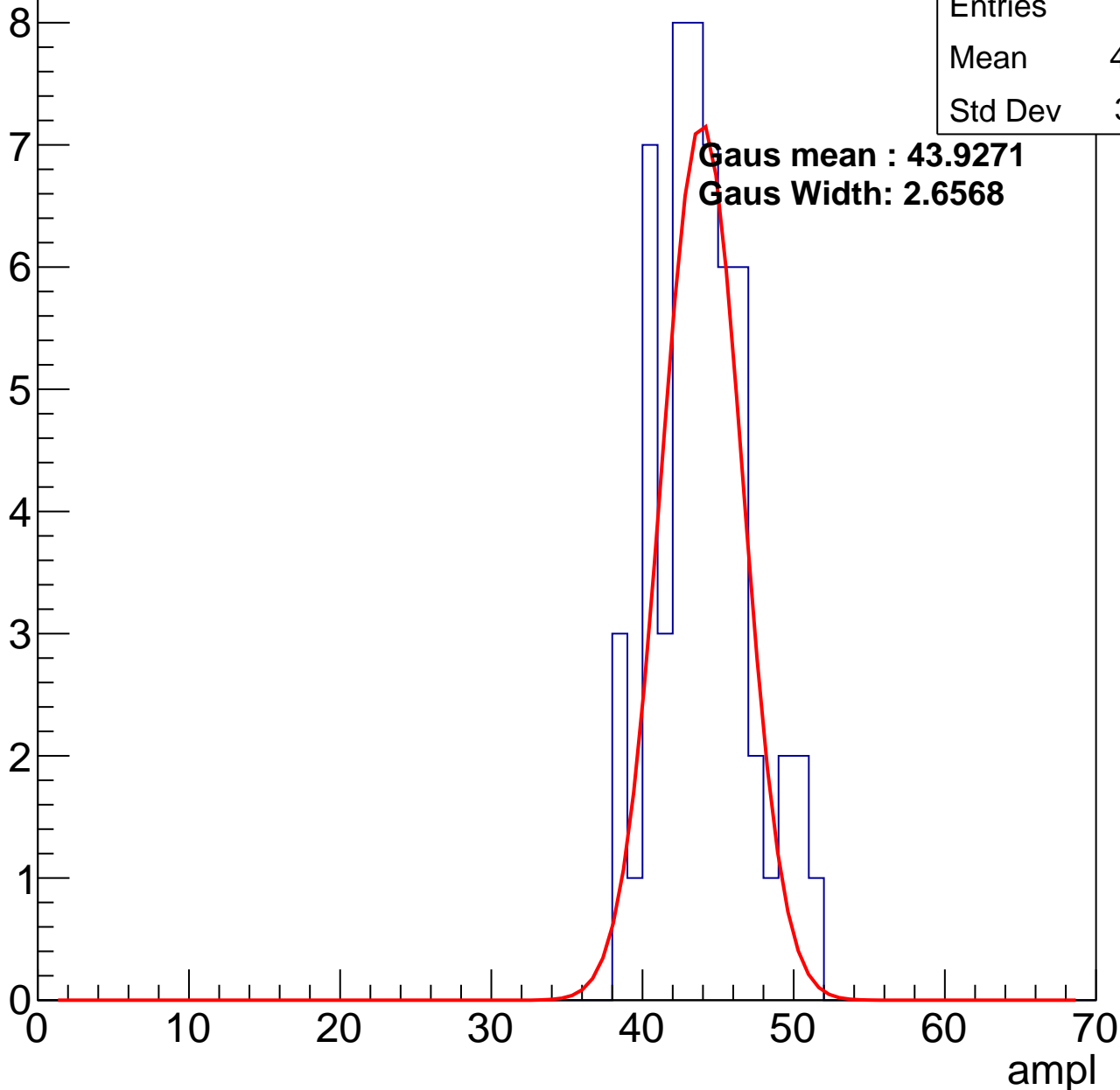
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	43.53
Std Dev	3.061

**Gaus mean : 43.9271**

**Gaus Width: 2.6568**

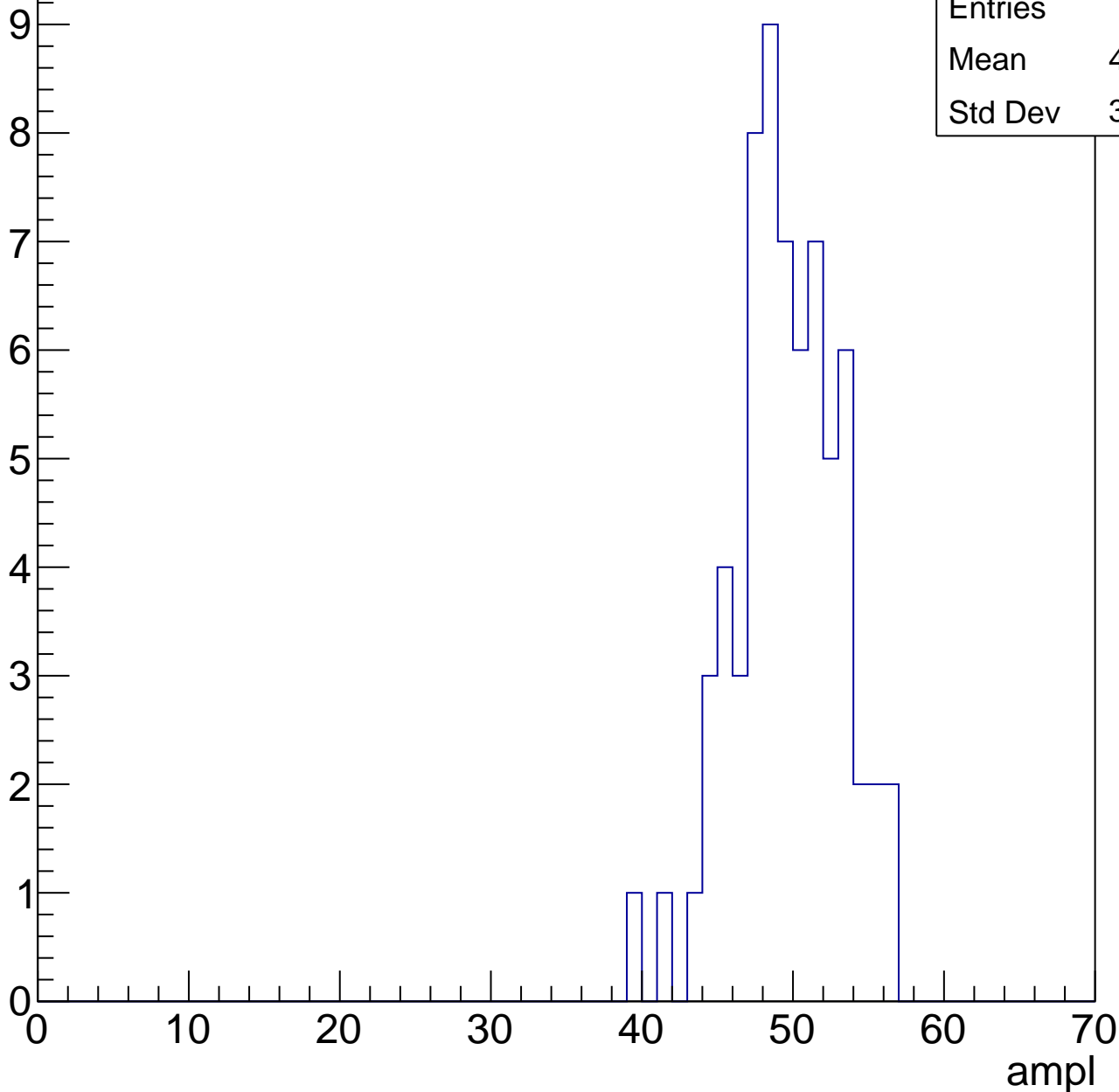


# B0L001S, U24-ch28, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	49.09
Std Dev	3.459

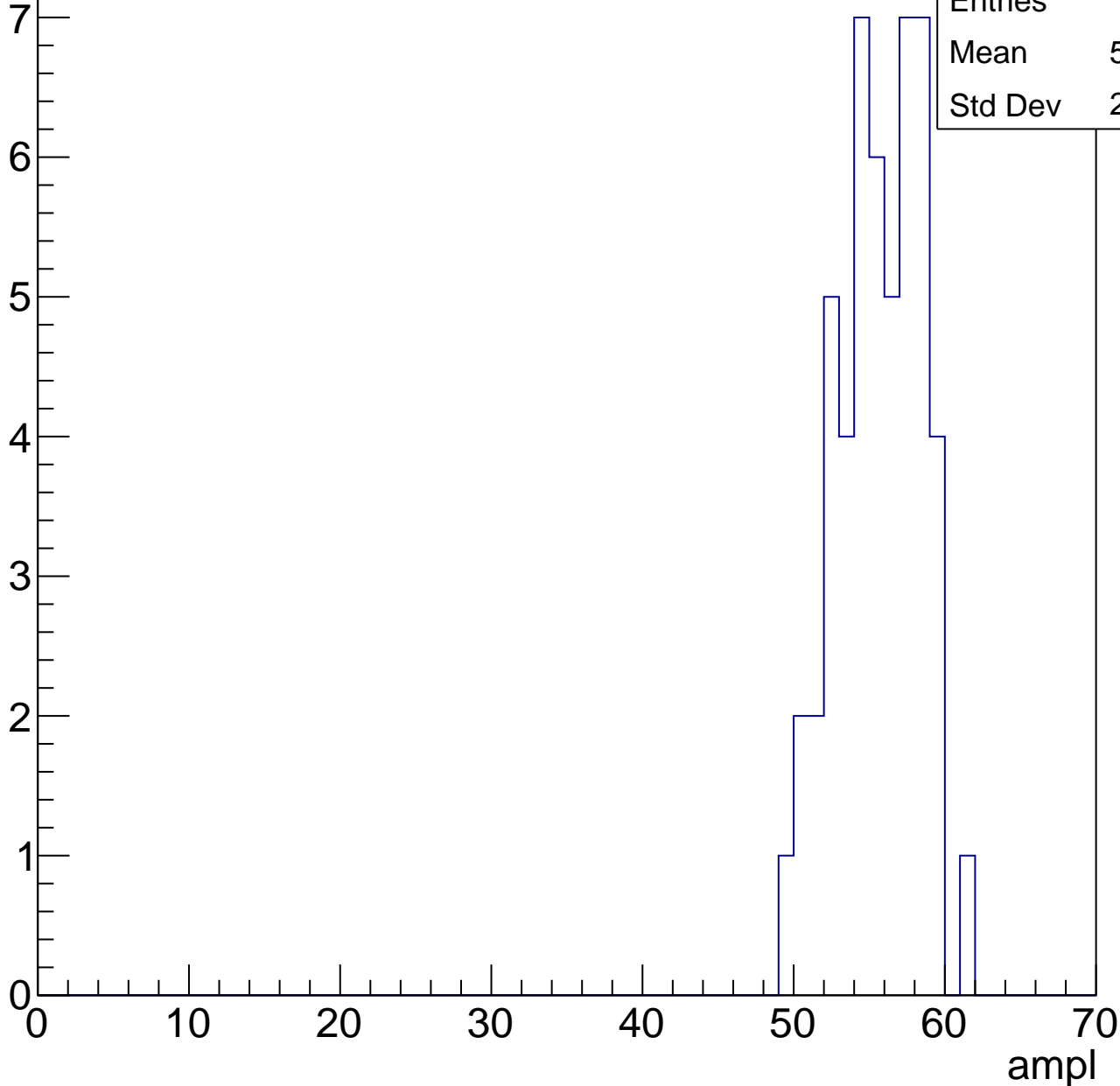


# B0L001S, U24-ch28, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	51
Mean	55.16
Std Dev	2.732

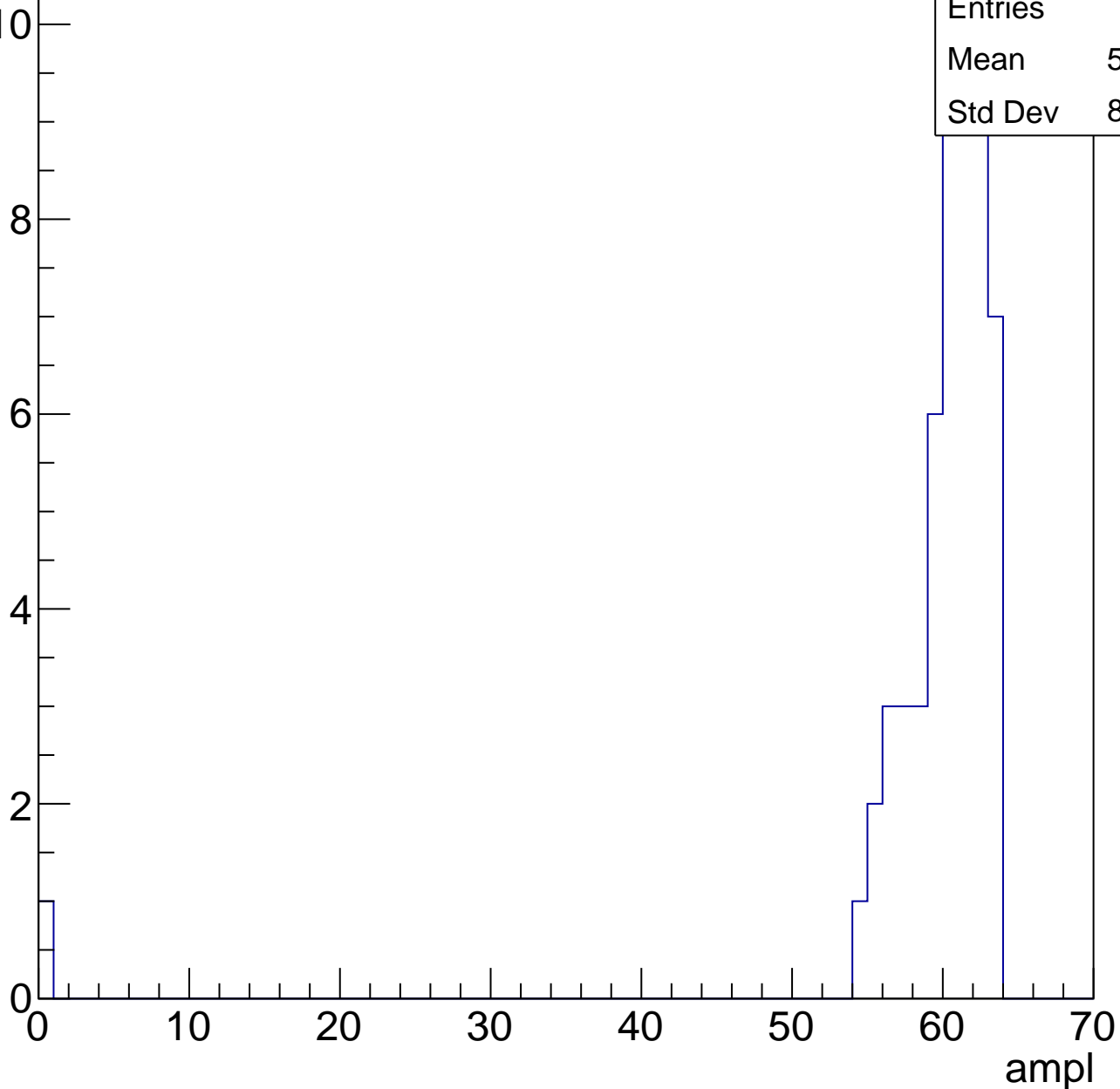


# B0L001S, U24-ch28, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	58.87
Std Dev	8.409



# B0L001S, U24-ch28, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch28, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U24-ch29, adc0

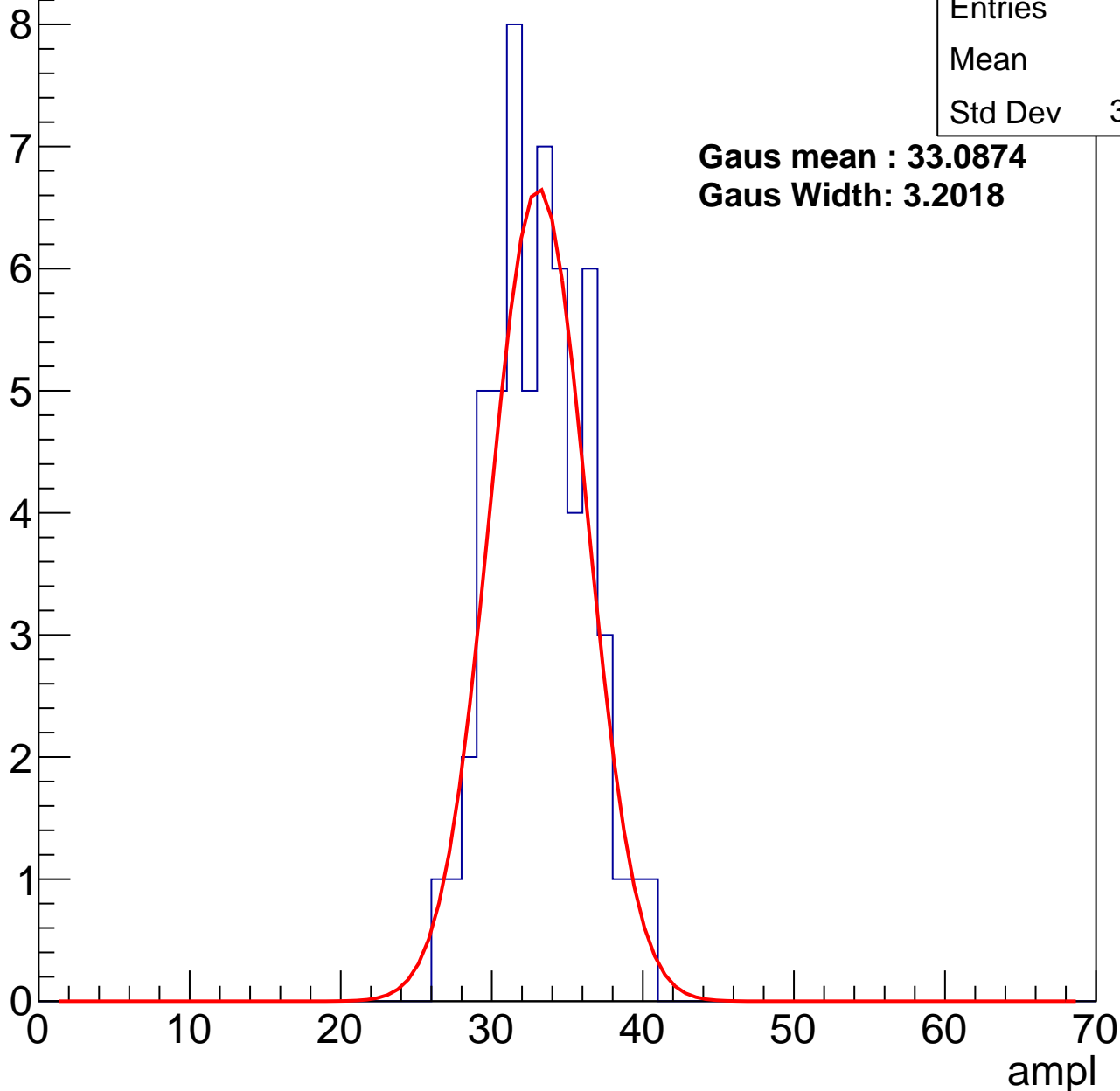
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	32.7
Std Dev	3.064

**Gaus mean : 33.0874**

**Gaus Width: 3.2018**



# B0L001S, U24-ch29, adc1

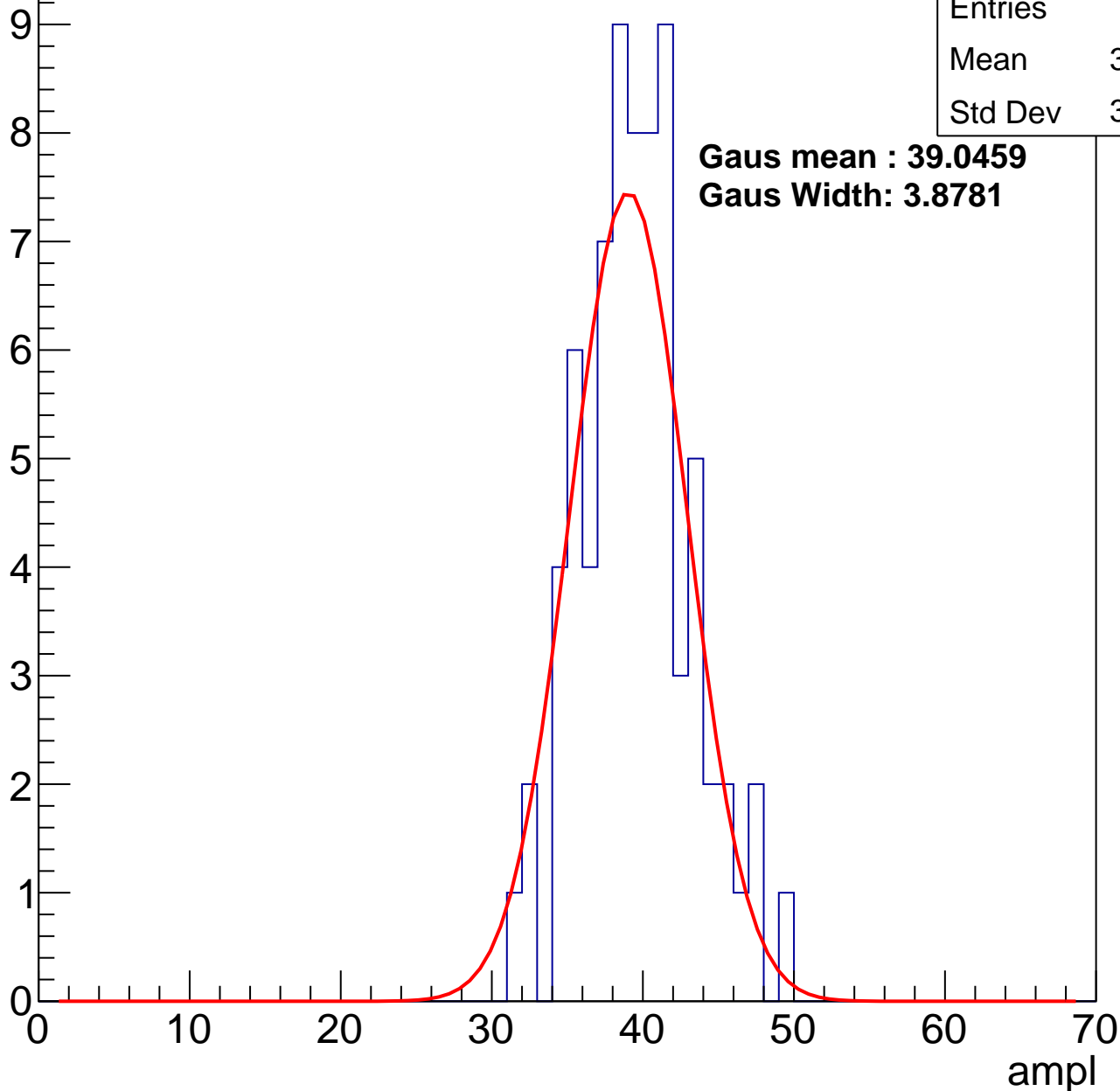
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	39.12
Std Dev	3.639

**Gaus mean : 39.0459**

**Gaus Width: 3.8781**



# B0L001S, U24-ch29, adc2

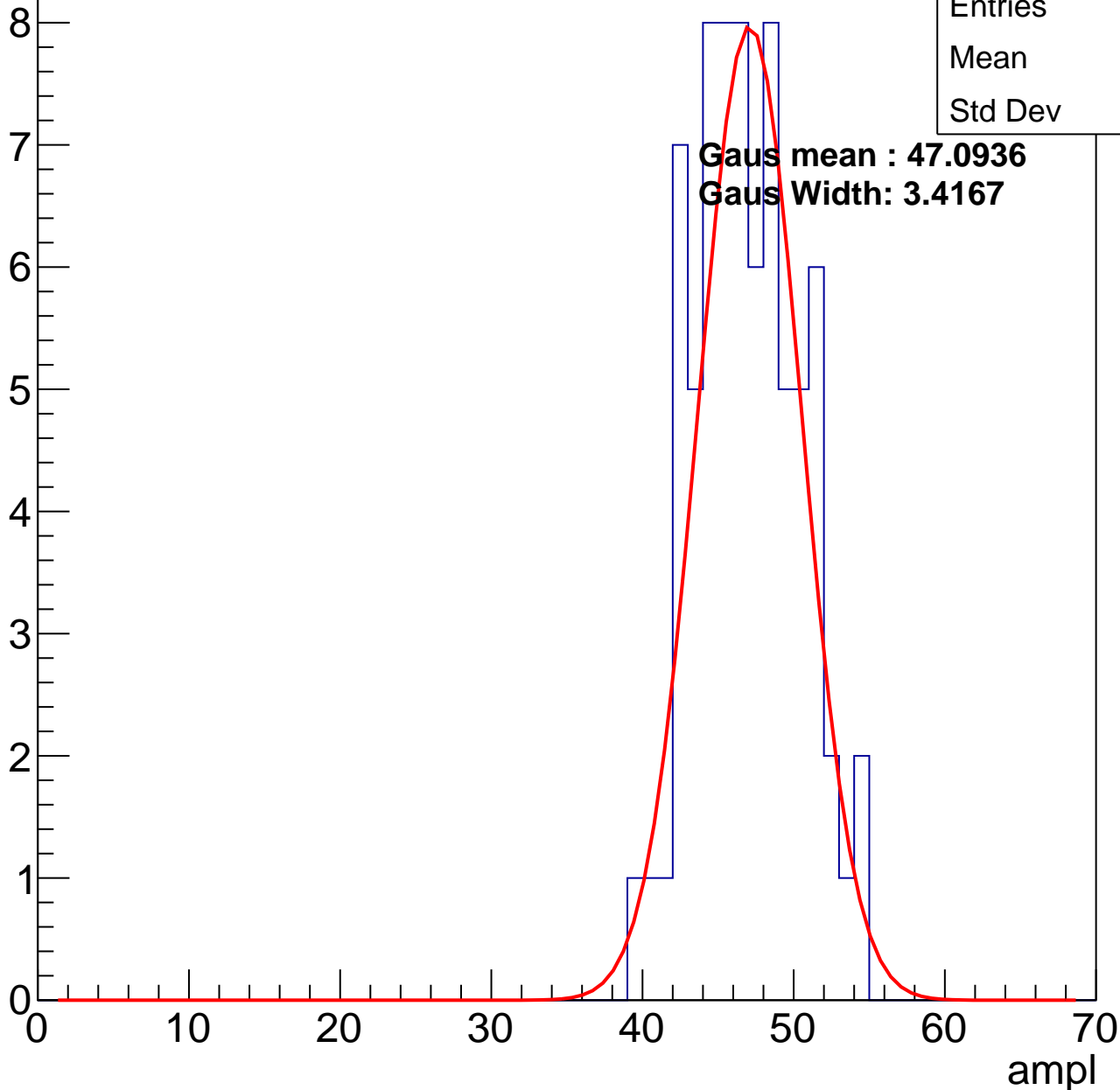
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	46.5
Std Dev	3.39

**Gaus mean : 47.0936**

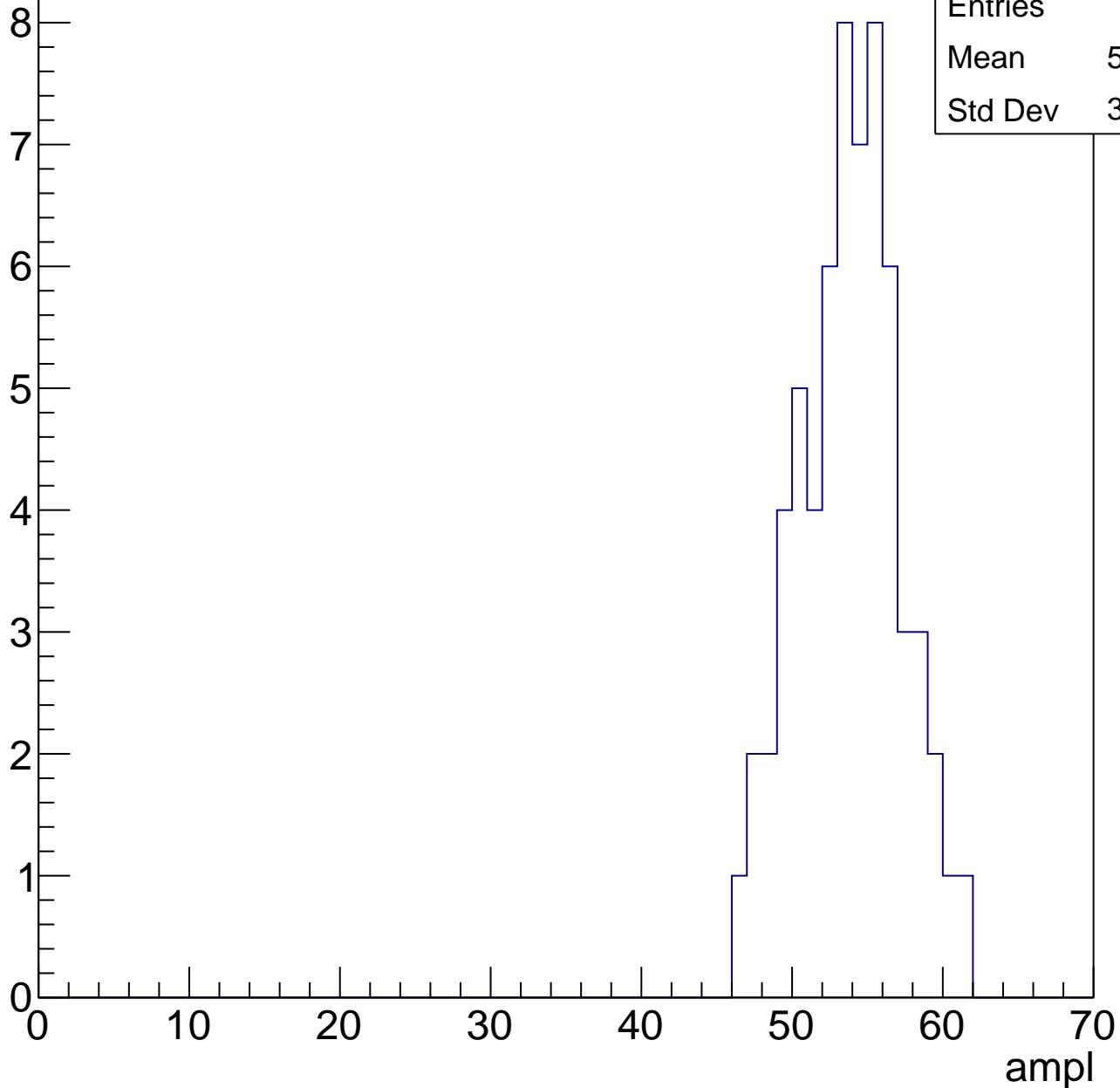
**Gaus Width: 3.4167**



# B0L001S, U24-ch29, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

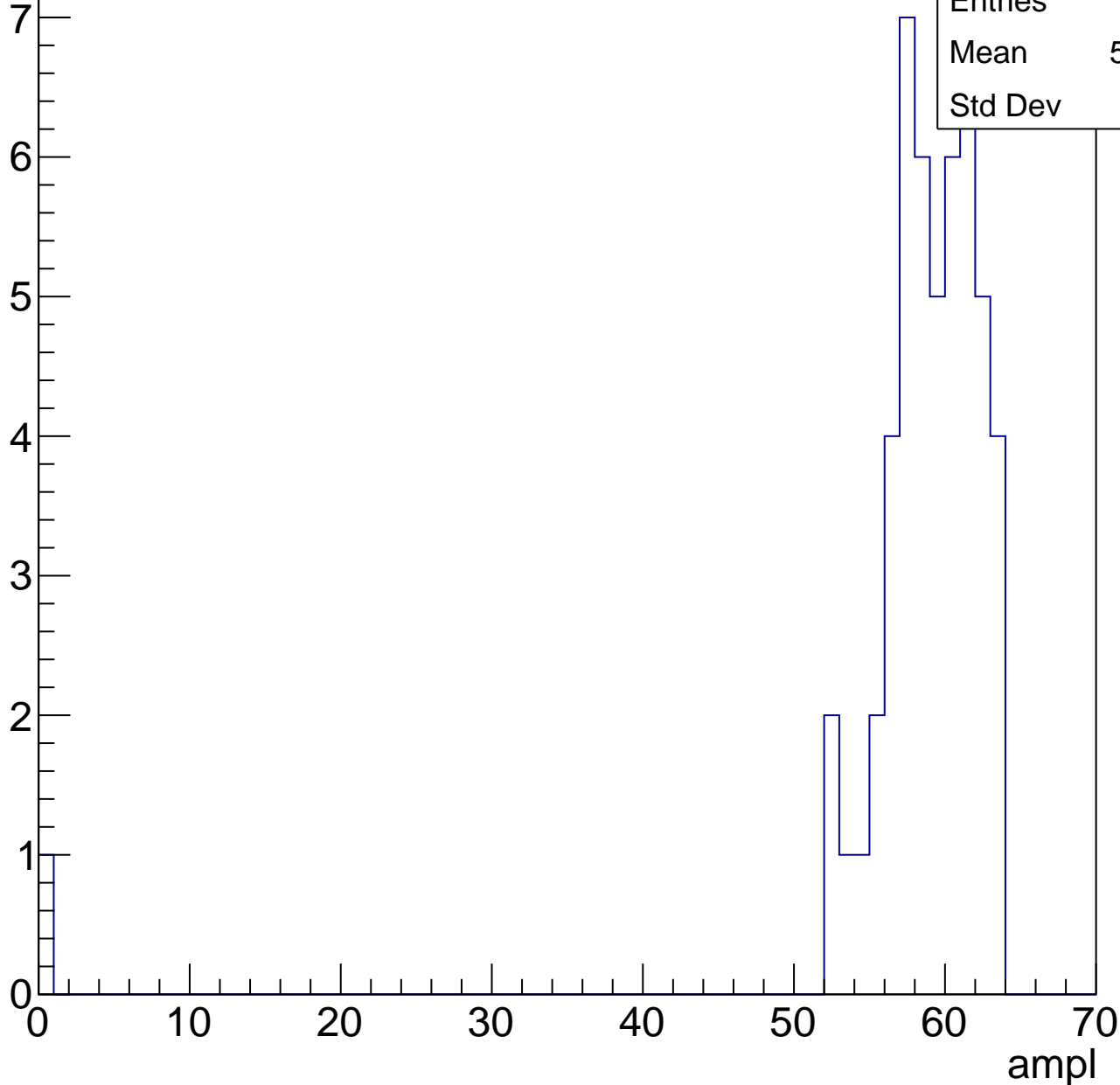


Entries	63
Mean	53.33
Std Dev	3.324

# B0L001S, U24-ch29, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

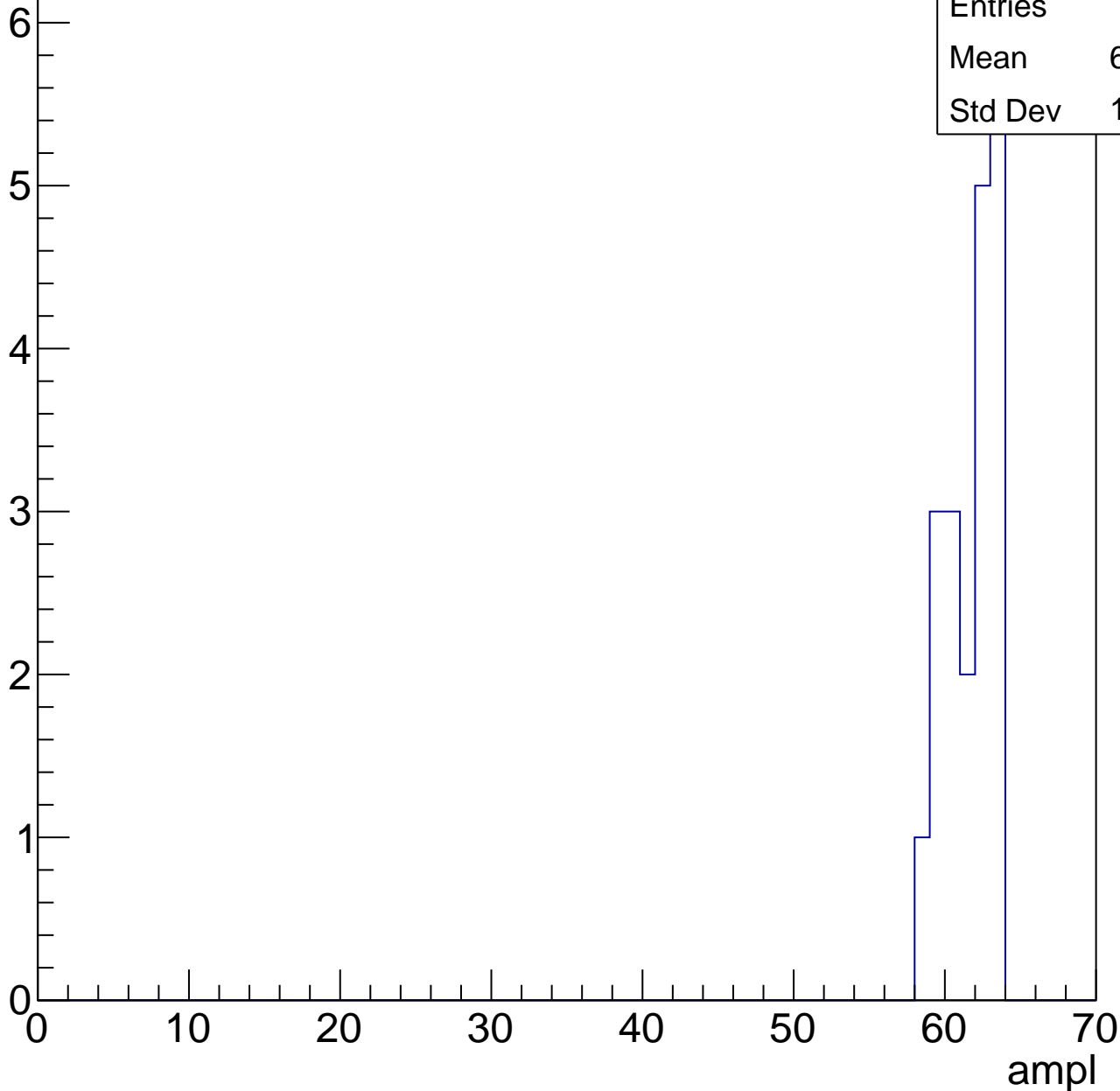


# B0L001S, U24-ch29, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	20
Mean	61.25
Std Dev	1.609



# B0L001S, U24-ch29, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U24-ch29, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U24-ch30, adc0

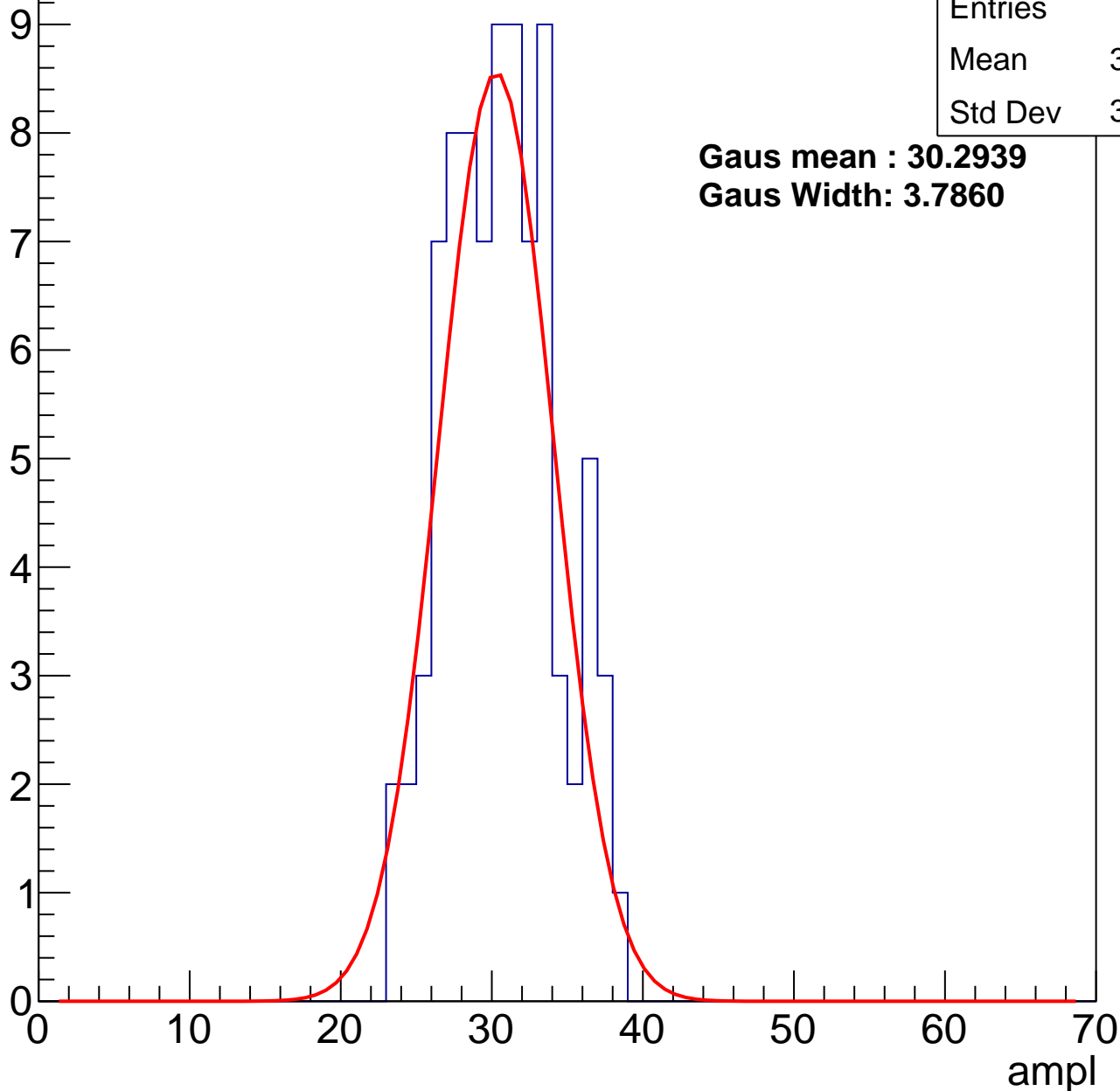
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	85
Mean	30.18
Std Dev	3.552

**Gaus mean : 30.2939**

**Gaus Width: 3.7860**



# B0L001S, U24-ch30, adc1

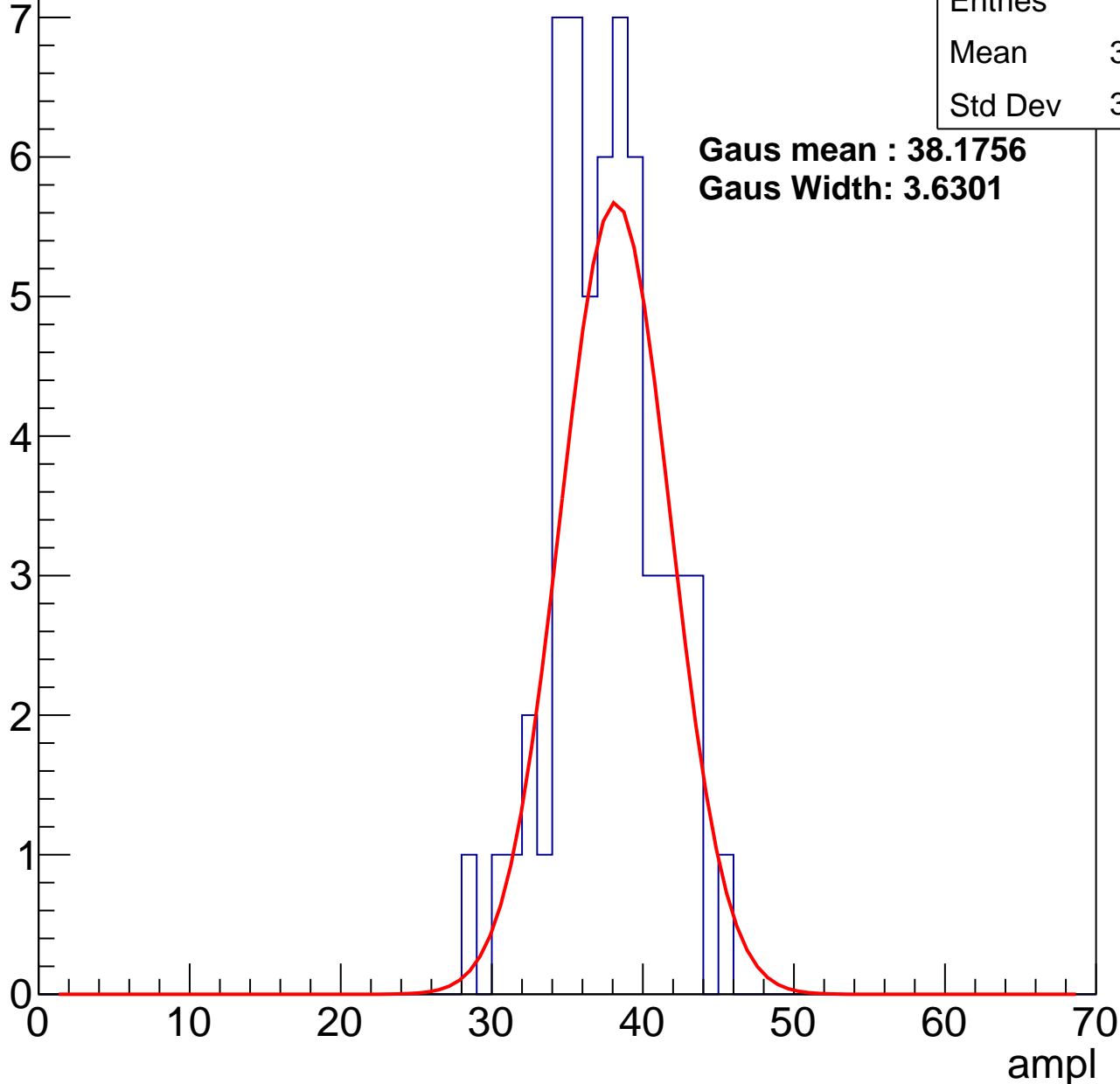
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	37.09
Std Dev	3.455

**Gaus mean : 38.1756**

**Gaus Width: 3.6301**



# B0L001S, U24-ch30, adc2

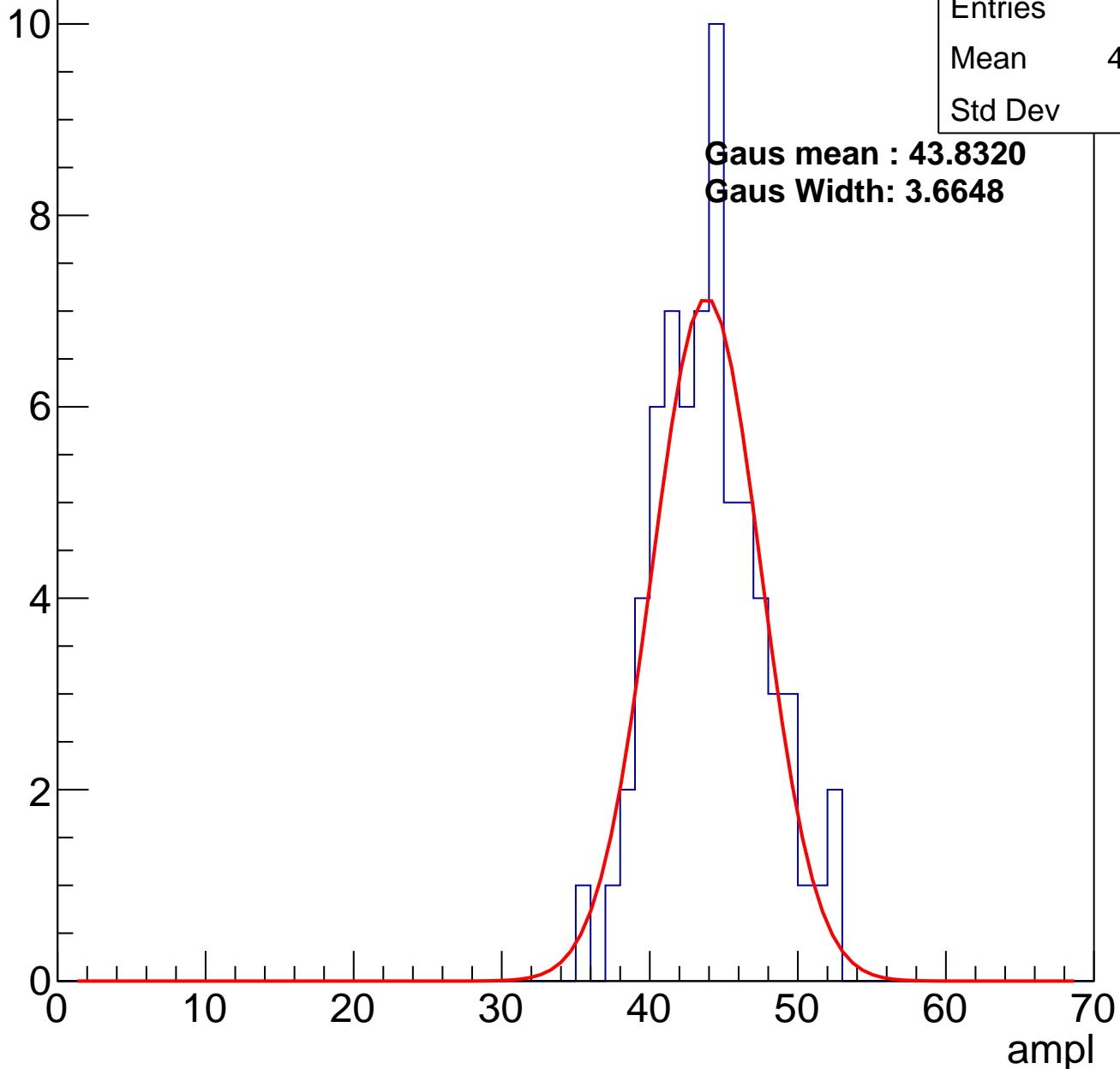
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	68
Mean	43.57
Std Dev	3.59

**Gaus mean : 43.8320**

**Gaus Width: 3.6648**

Entry

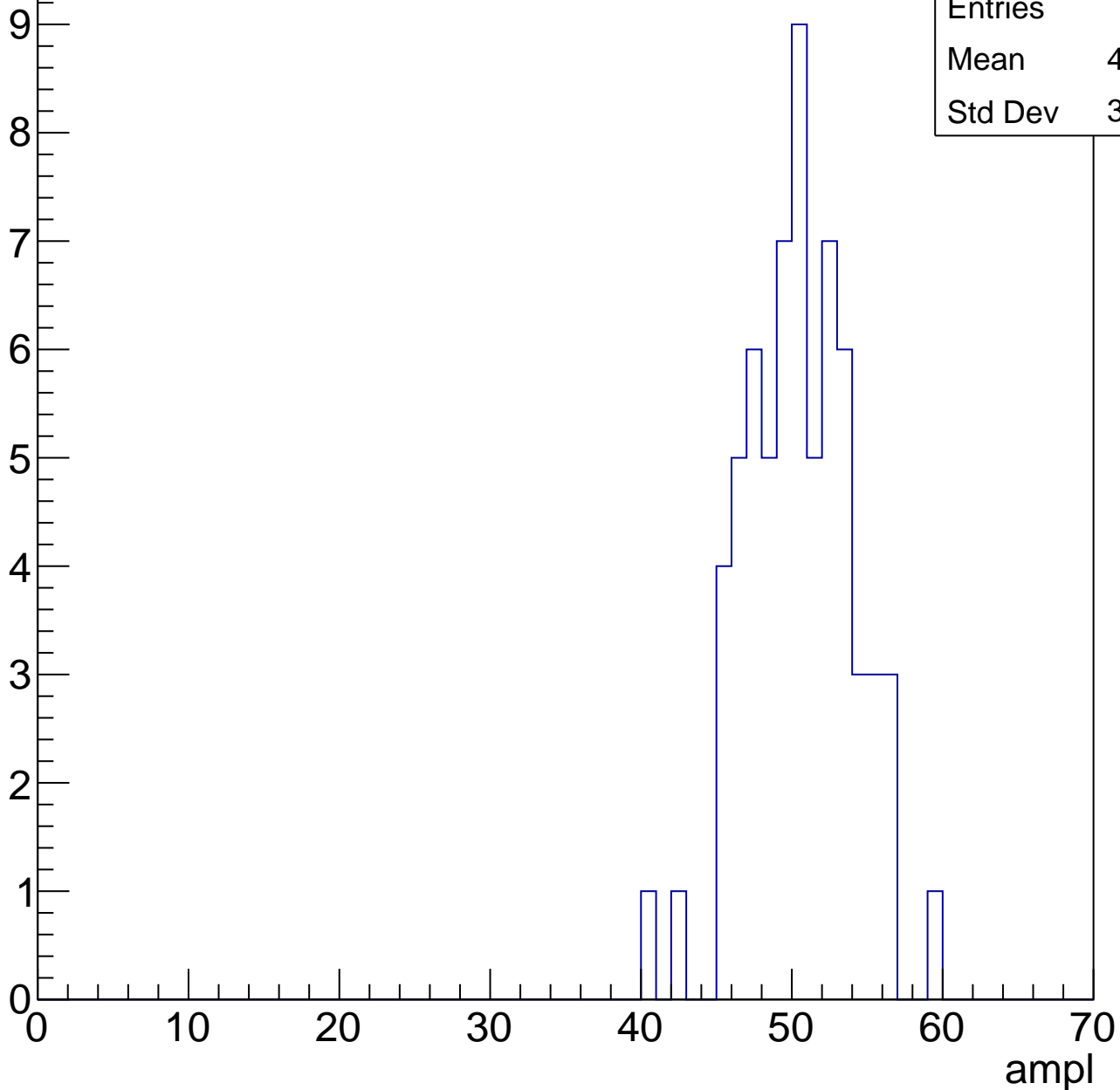


# B0L001S, U24-ch30, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

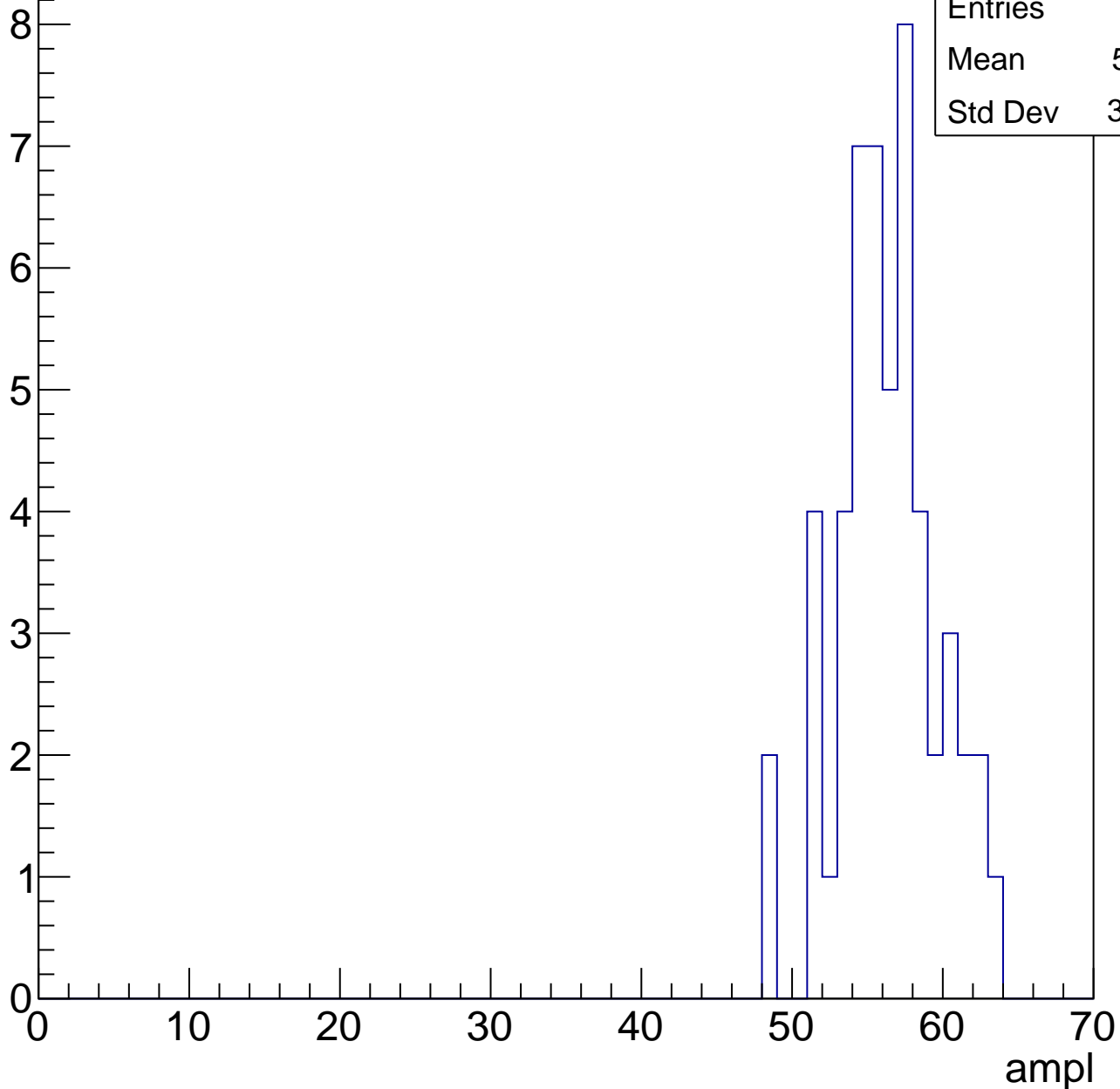
Entries	66
Mean	49.97
Std Dev	3.533



# B0L001S, U24-ch30, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

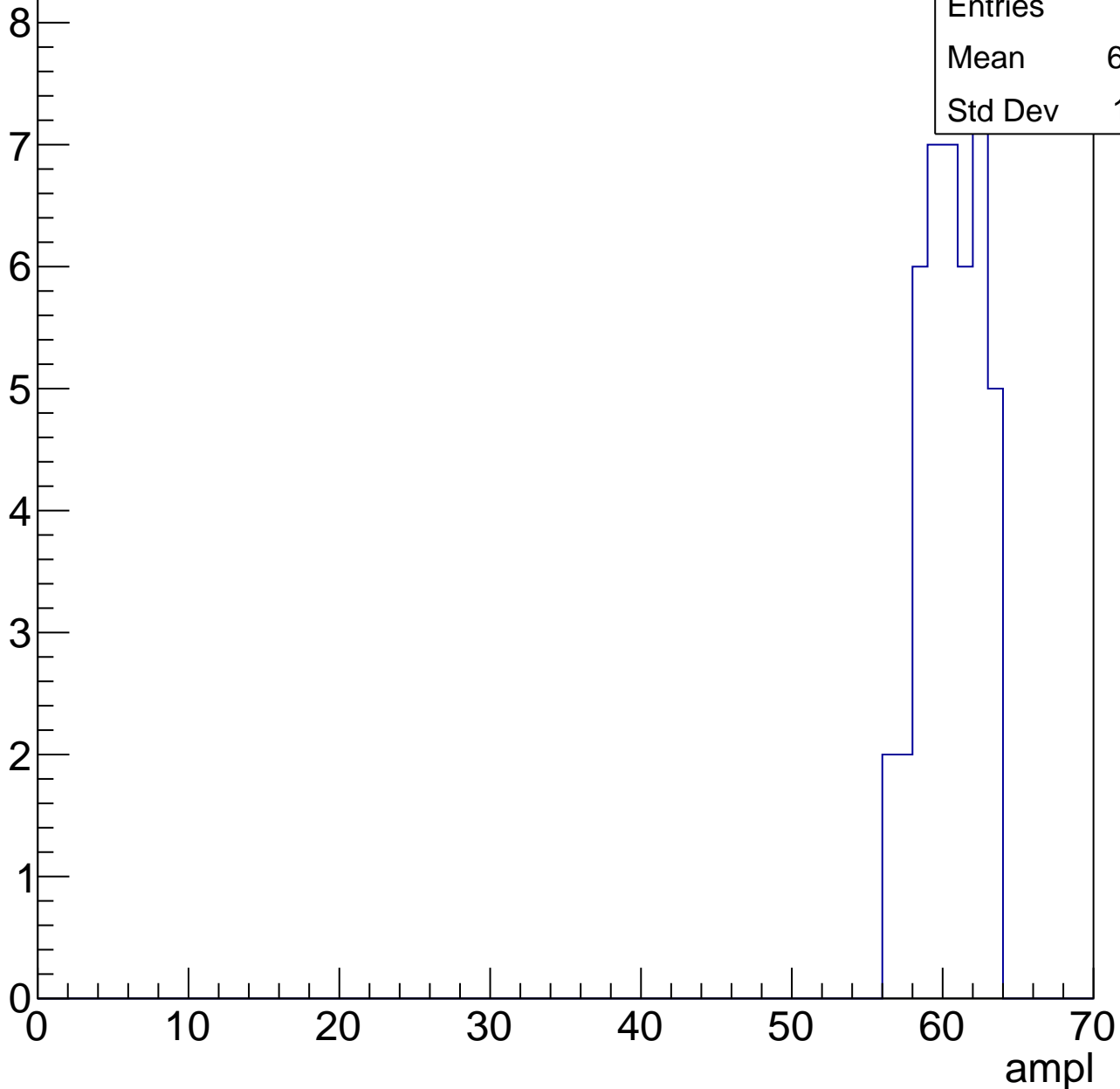


# B0L001S, U24-ch30, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

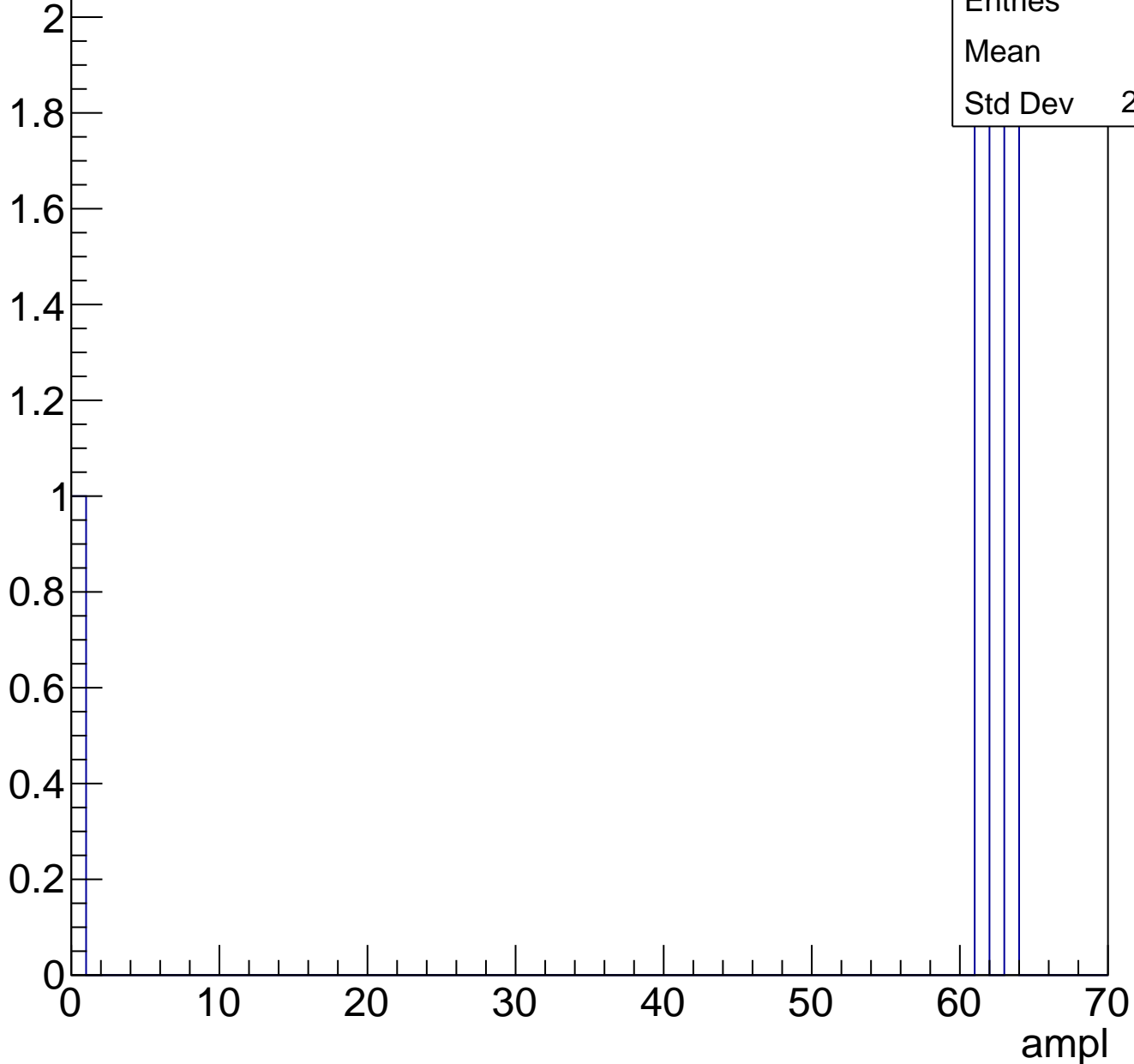
Entries	43
Mean	60.09
Std Dev	1.951



# B0L001S, U24-ch30, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



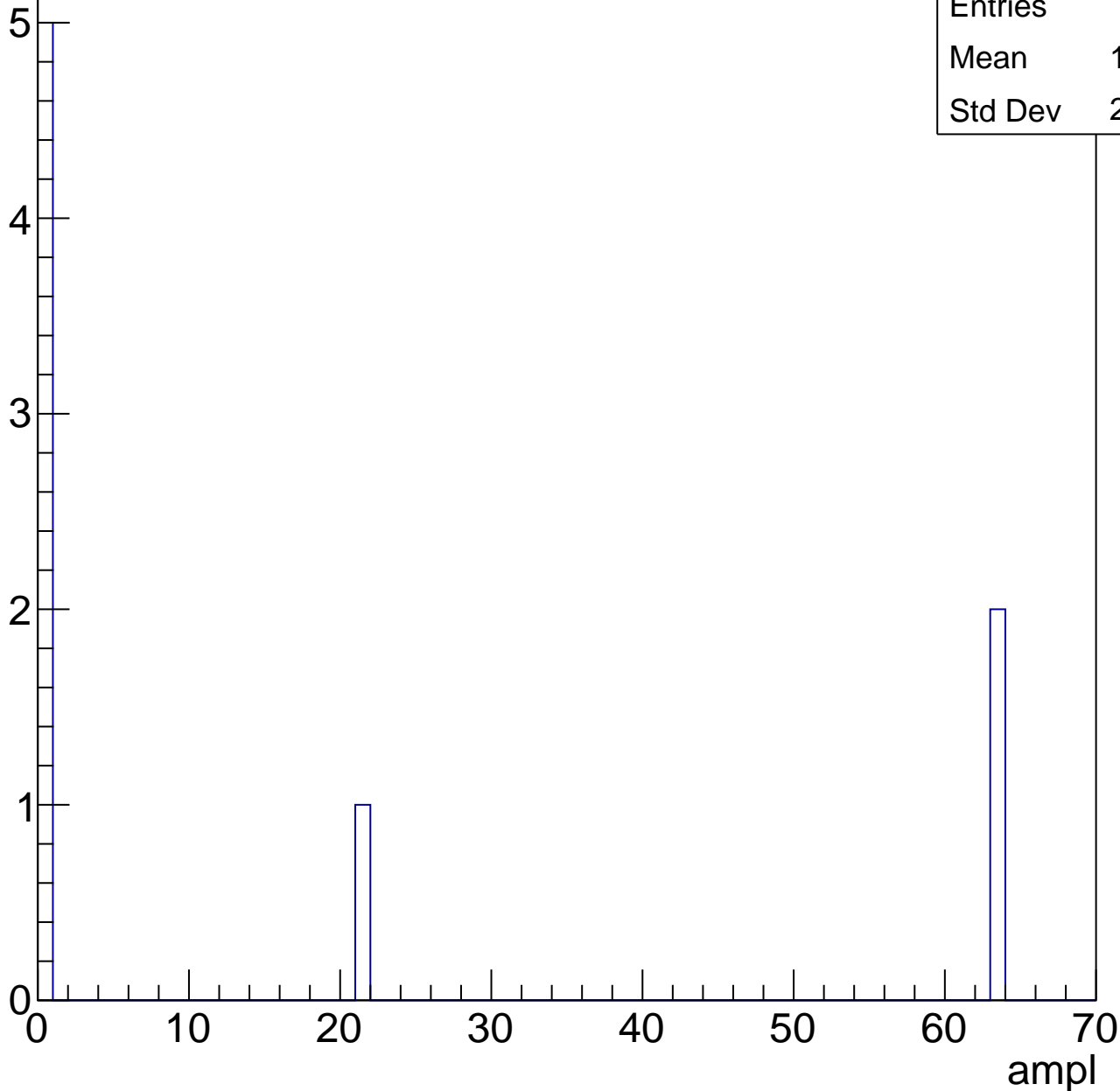


# B0L001S, U24-ch30, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	8
Mean	18.38
Std Dev	26.64



# B0L001S, U24-ch31, adc0

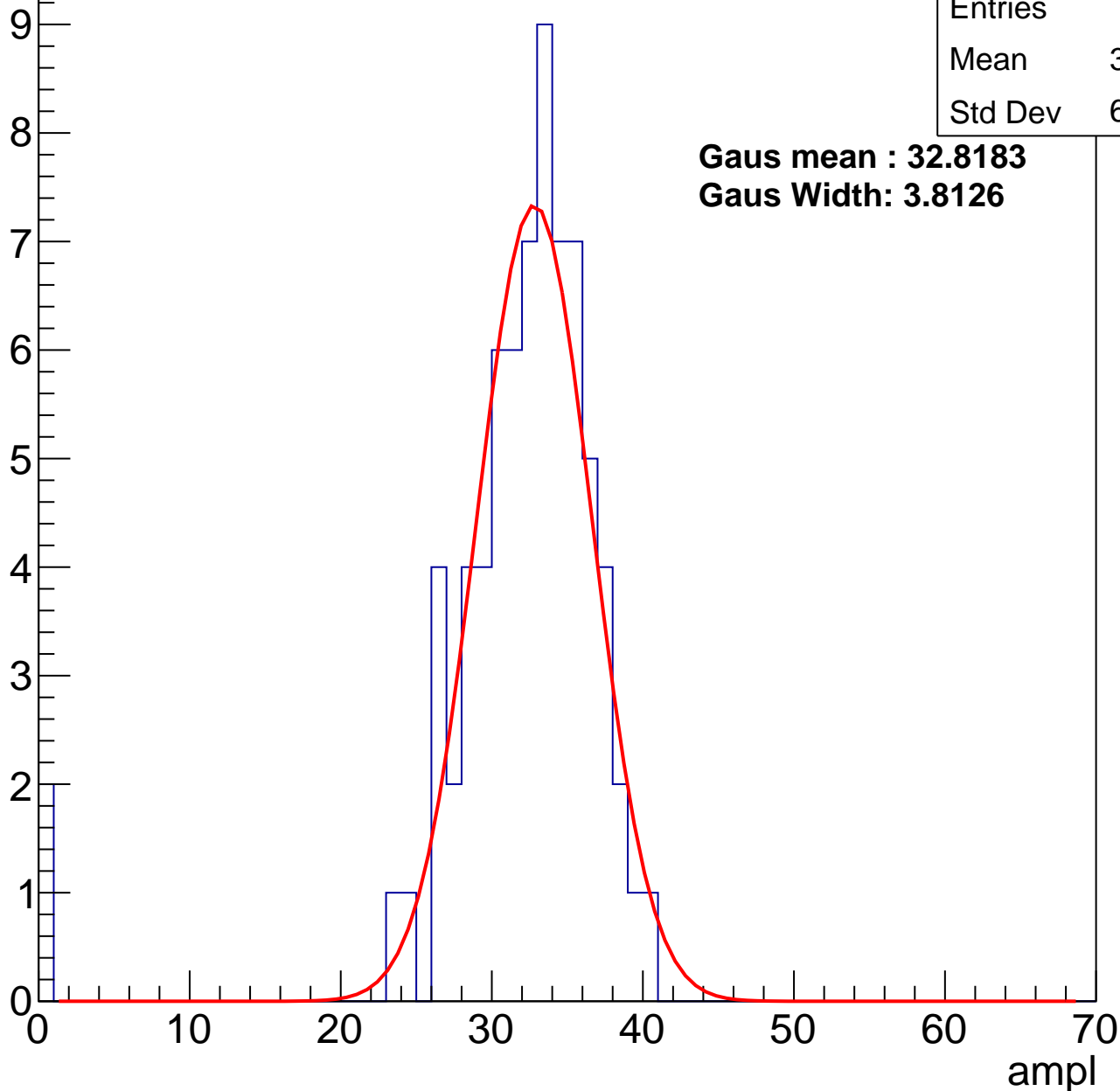
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	31.32
Std Dev	6.355

**Gaus mean : 32.8183**

**Gaus Width: 3.8126**



# B0L001S, U24-ch31, adc1

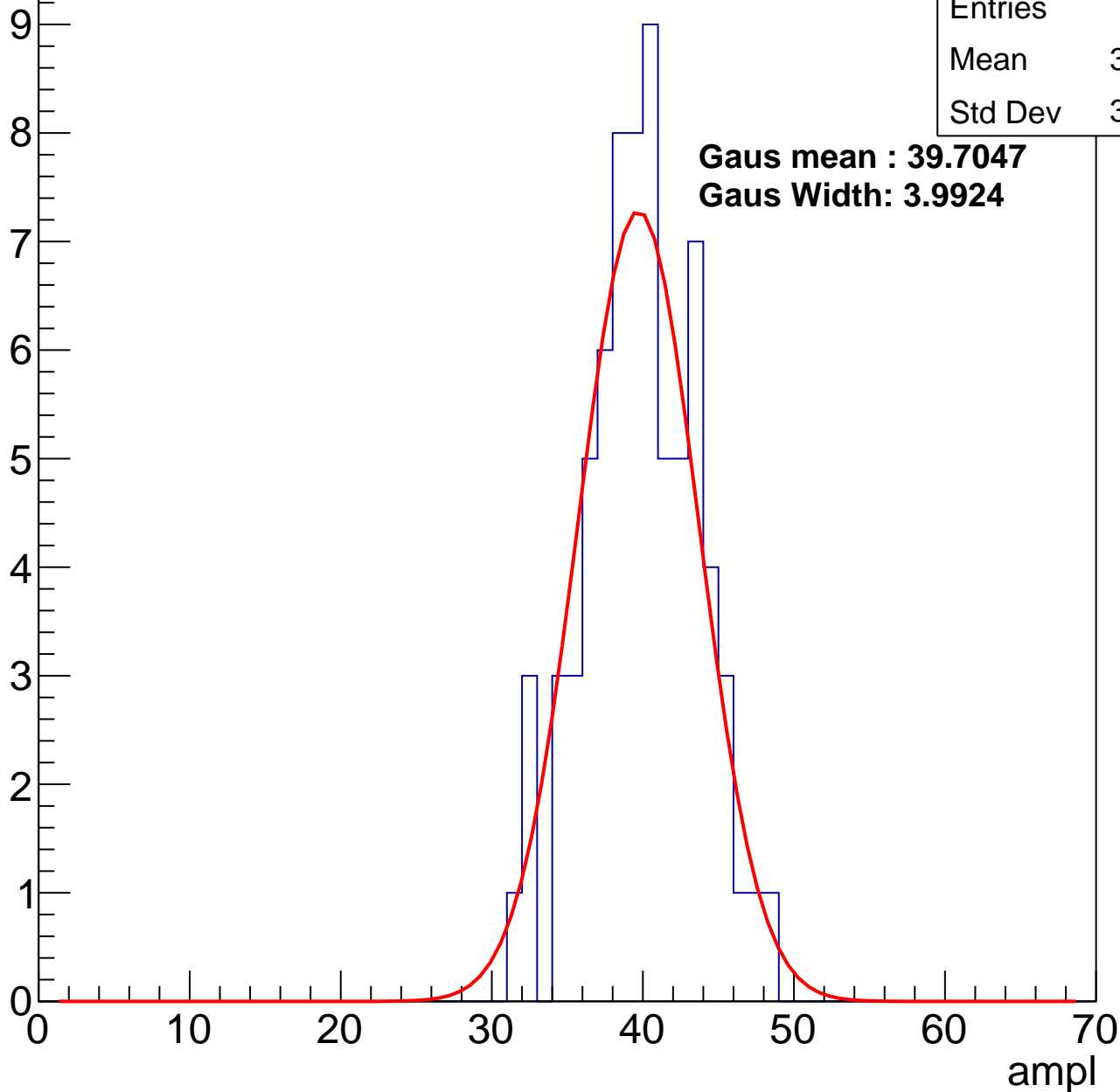
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	39.45
Std Dev	3.672

**Gaus mean : 39.7047**

**Gaus Width: 3.9924**



# B0L001S, U24-ch31, adc2

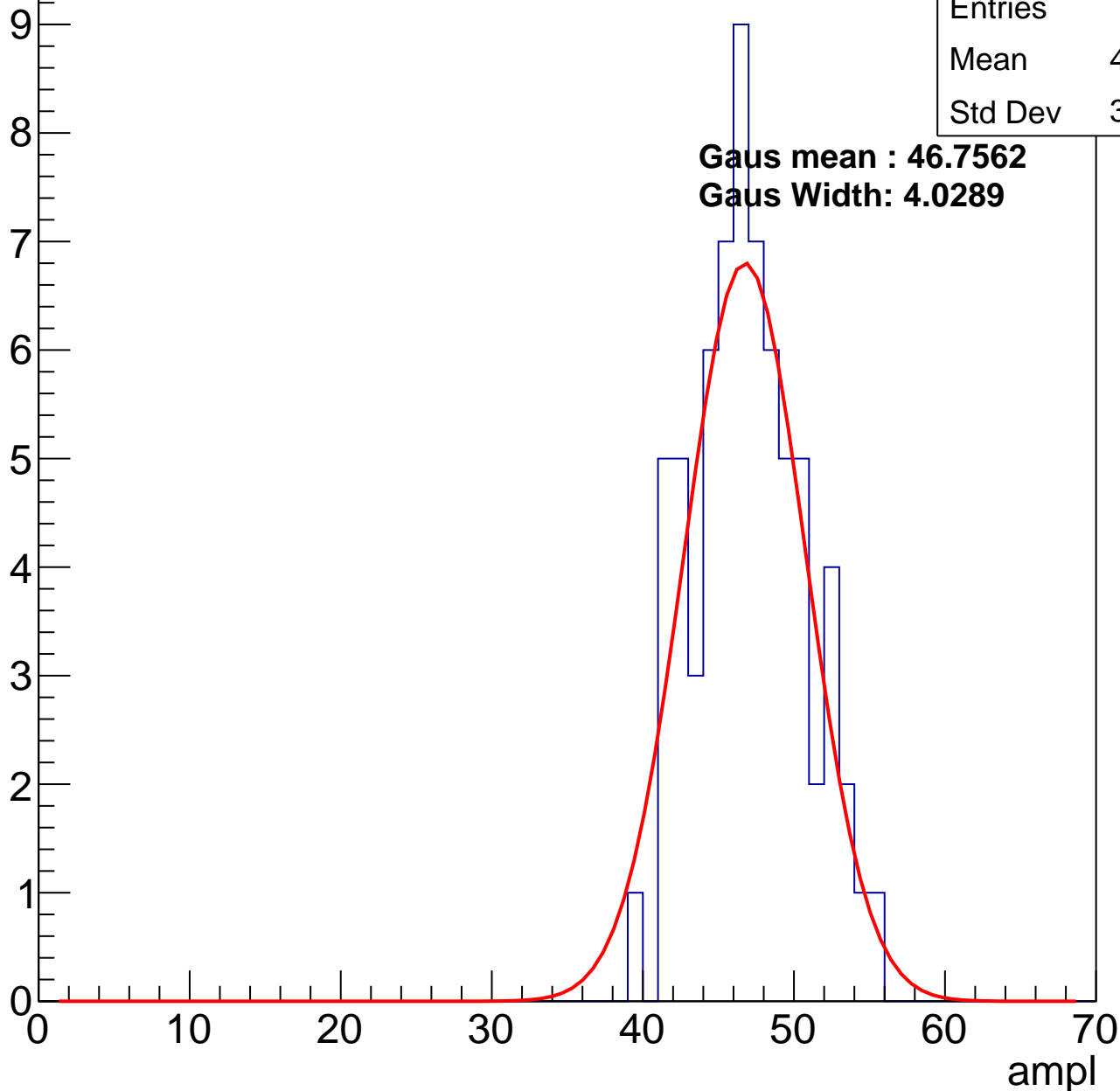
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	46.57
Std Dev	3.577

**Gaus mean : 46.7562**

**Gaus Width: 4.0289**

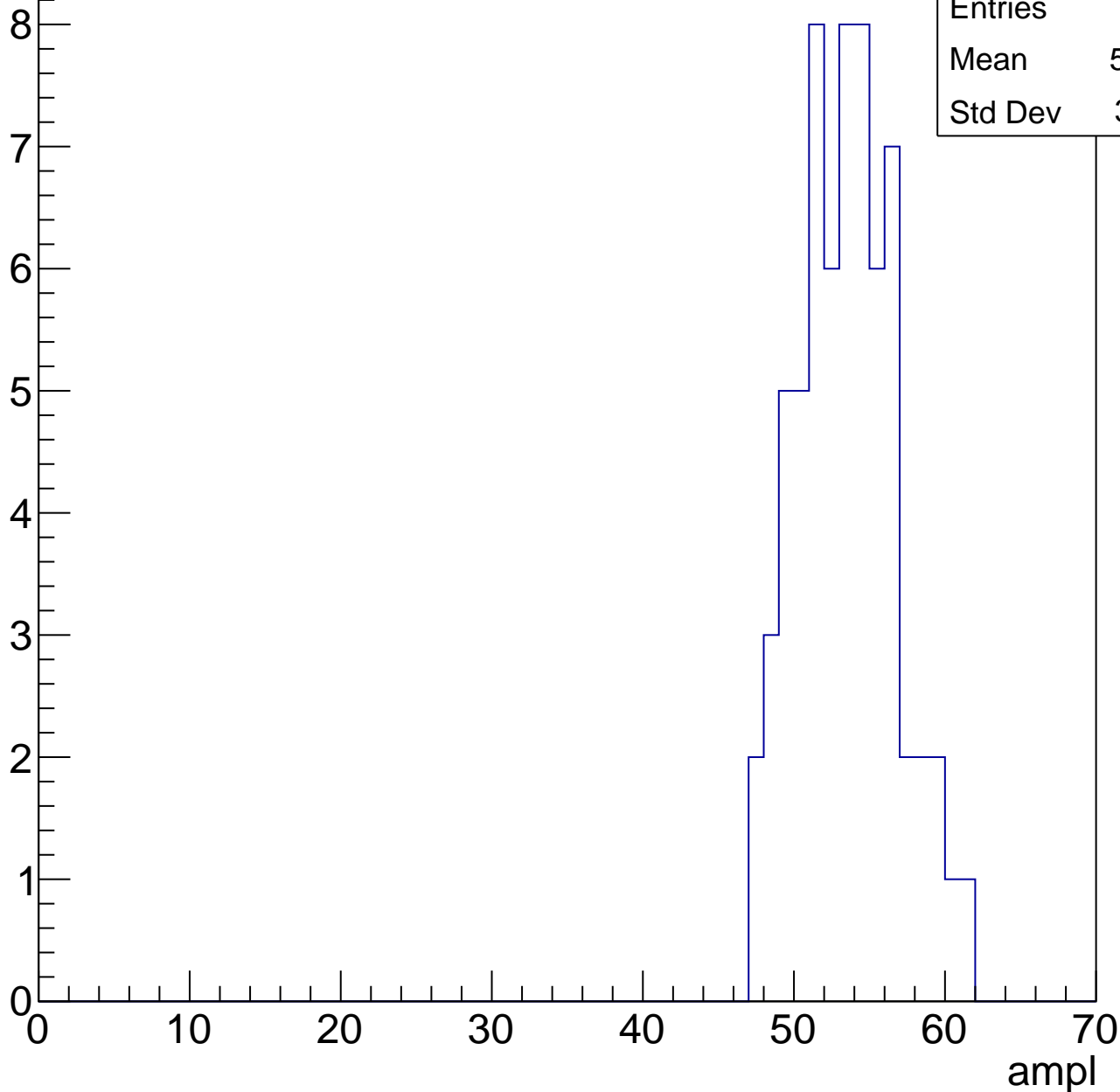


# B0L001S, U24-ch31, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	53.03
Std Dev	3.191

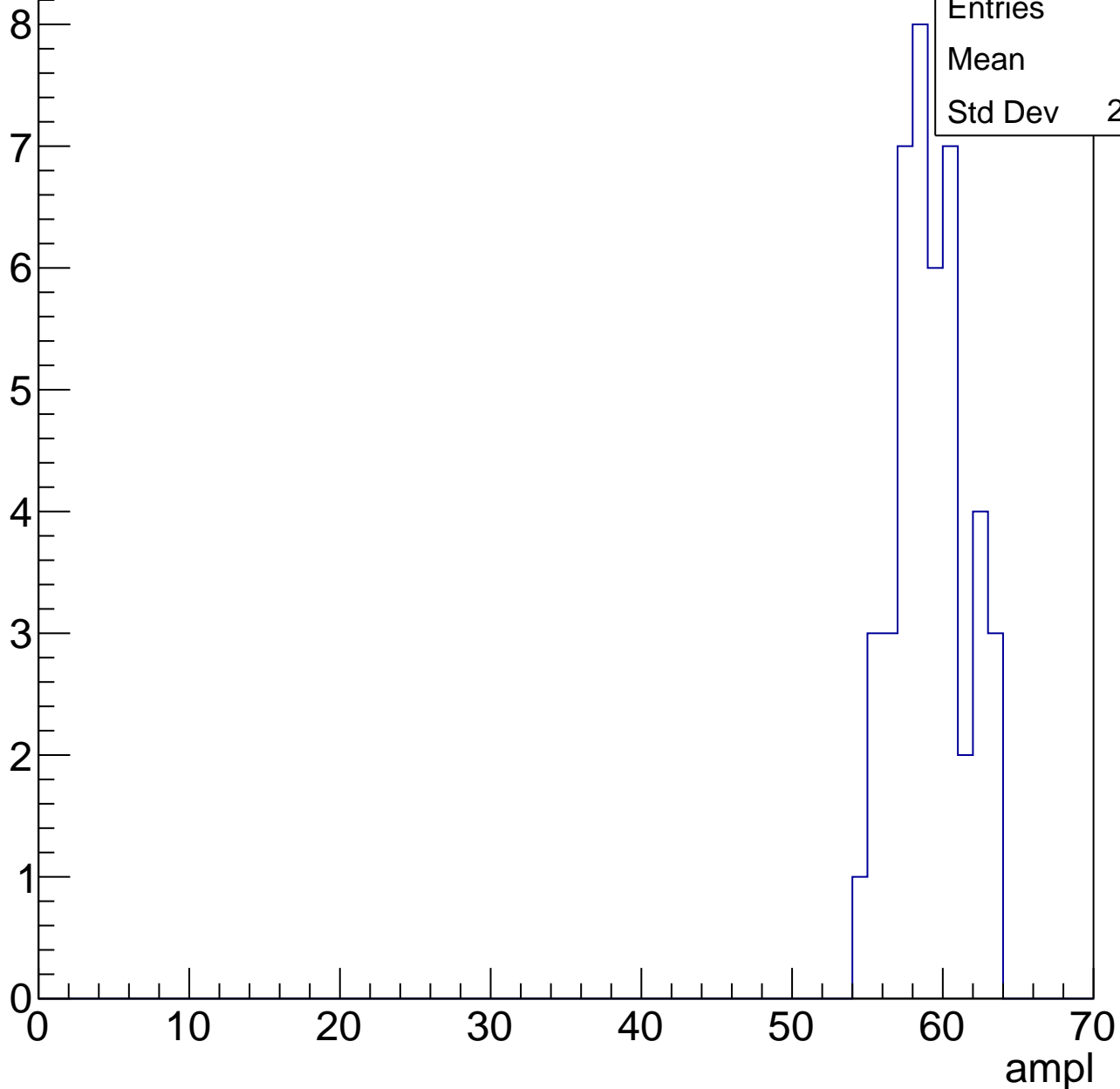


# B0L001S, U24-ch31, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	44
Mean	58.7
Std Dev	2.292

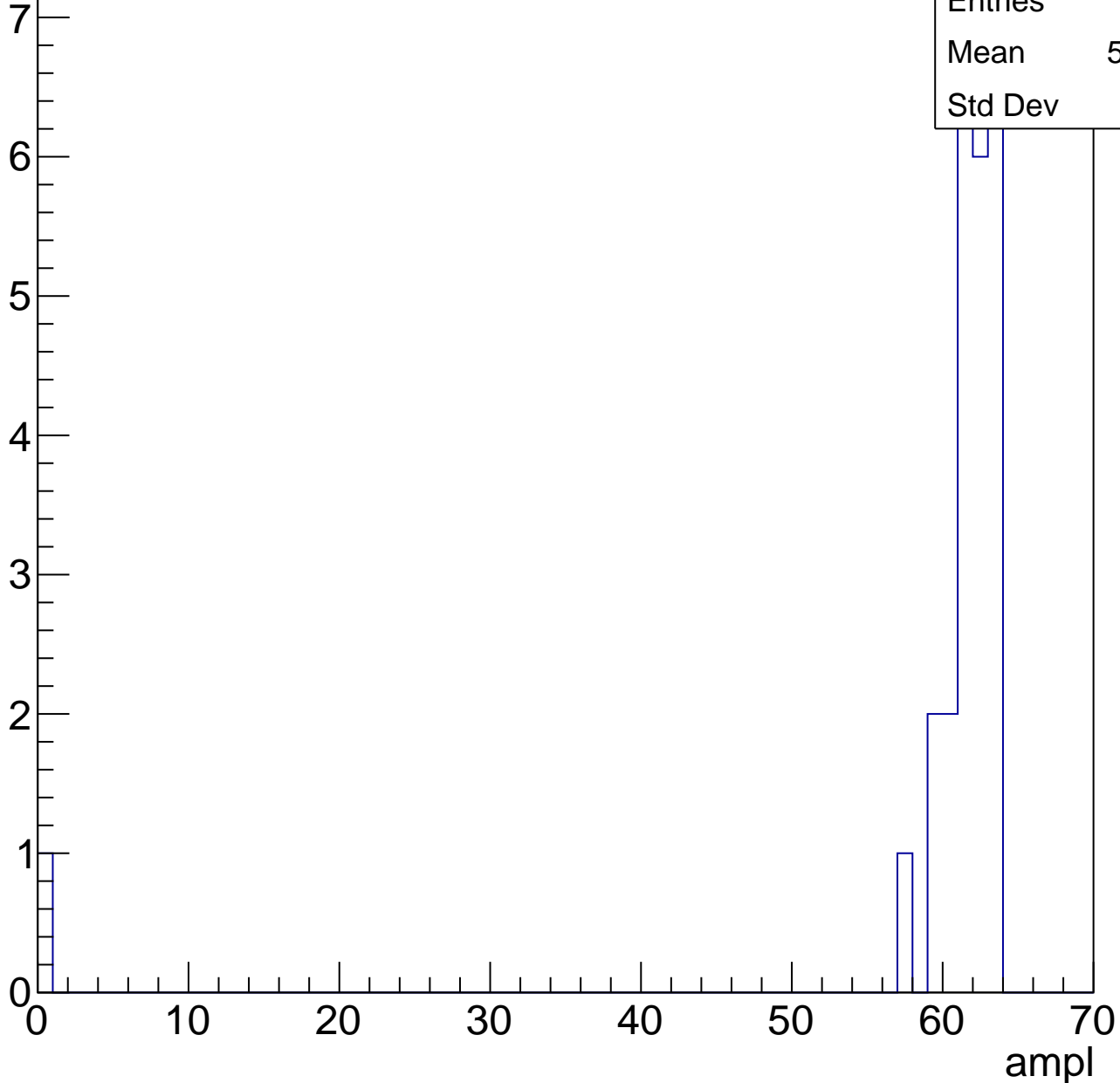


# B0L001S, U24-ch31, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	26
Mean	59.04
Std Dev	11.9



# B0L001S, U24-ch31, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U24-ch31, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U24-ch32, adc0

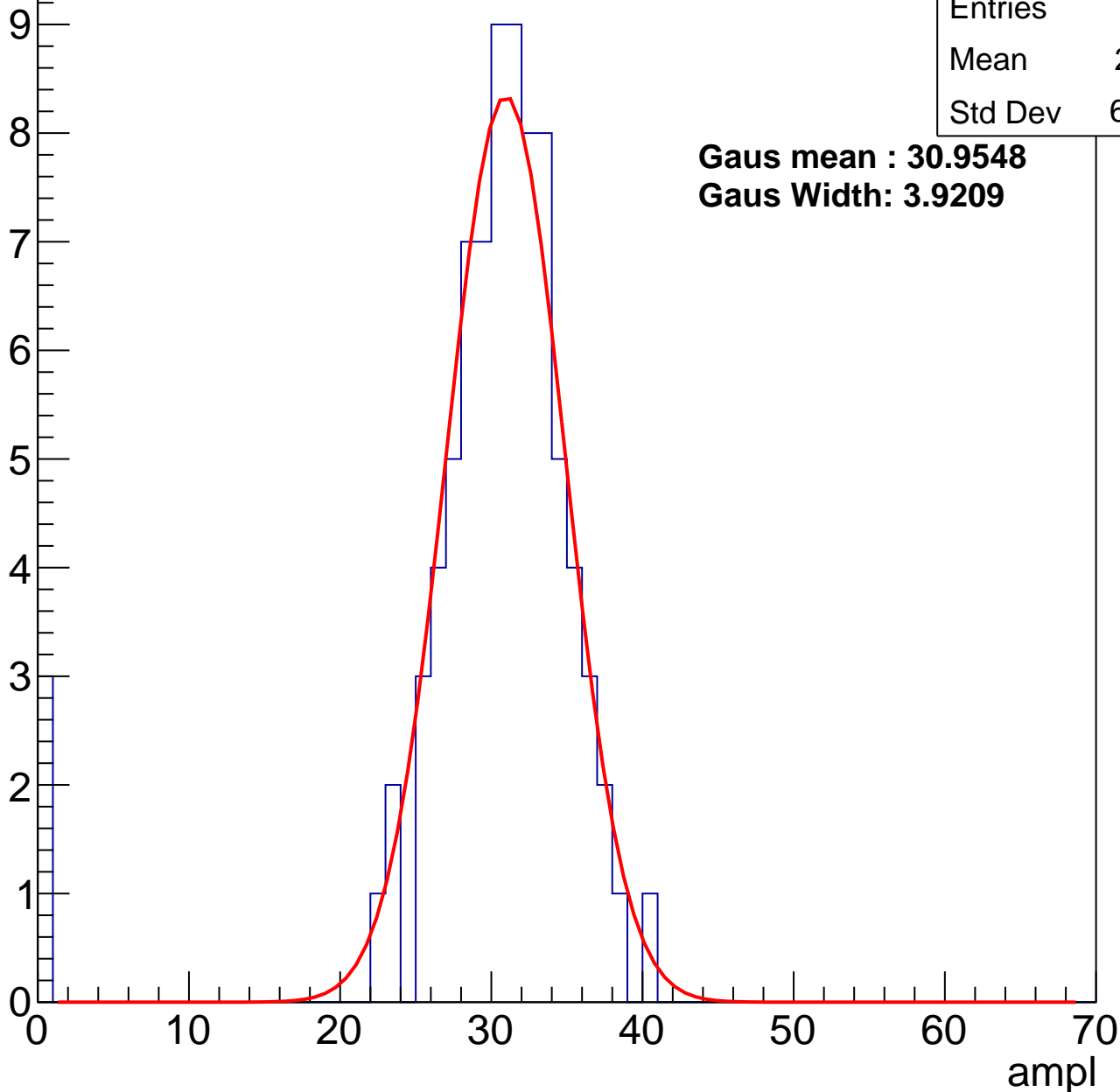
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	82
Mean	29.51
Std Dev	6.739

**Gaus mean : 30.9548**

**Gaus Width: 3.9209**



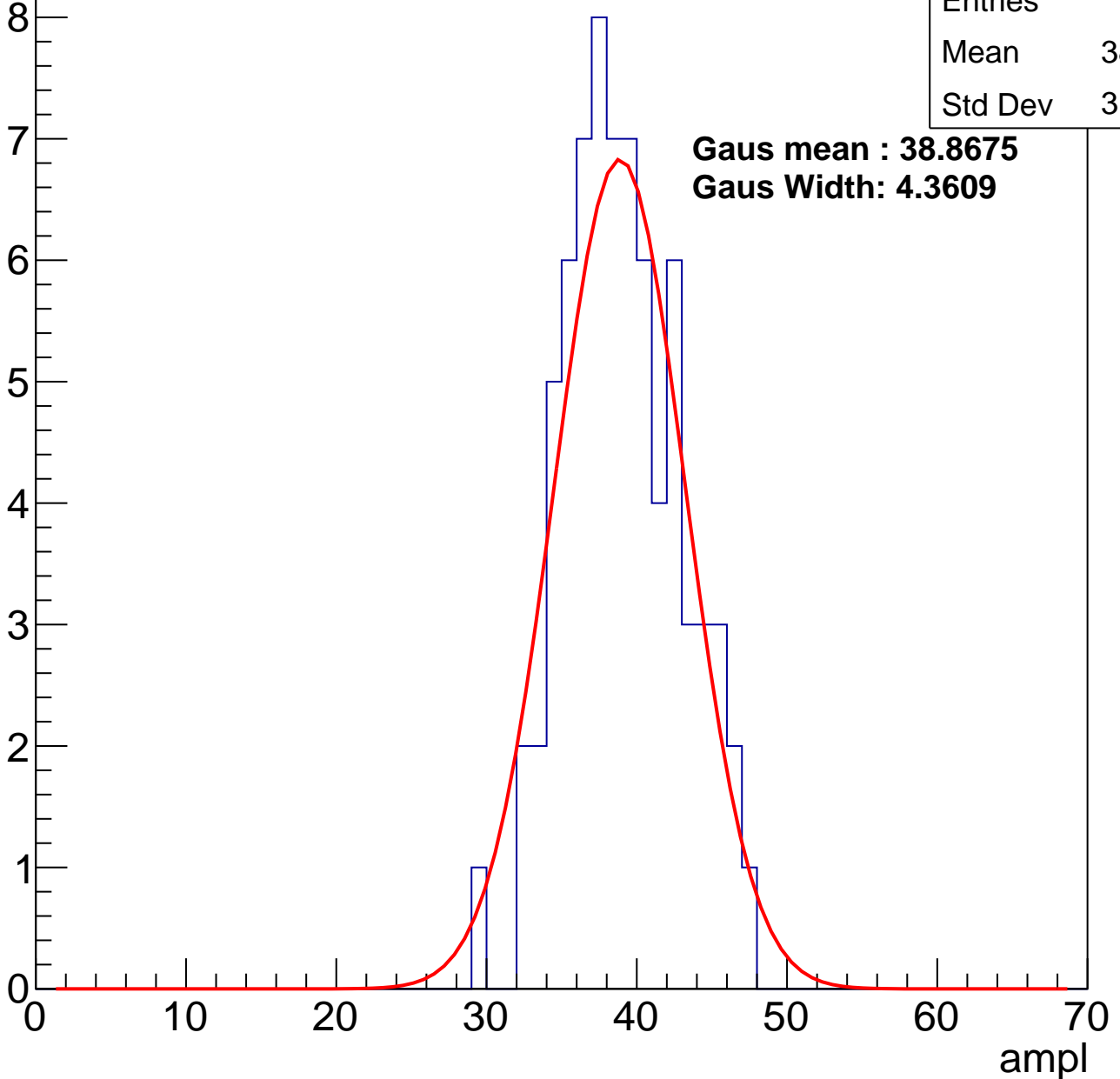
# B0L001S, U24-ch32, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	38.59
Std Dev	3.792

**Gaus mean : 38.8675**  
**Gaus Width: 4.3609**



# B0L001S, U24-ch32, adc2

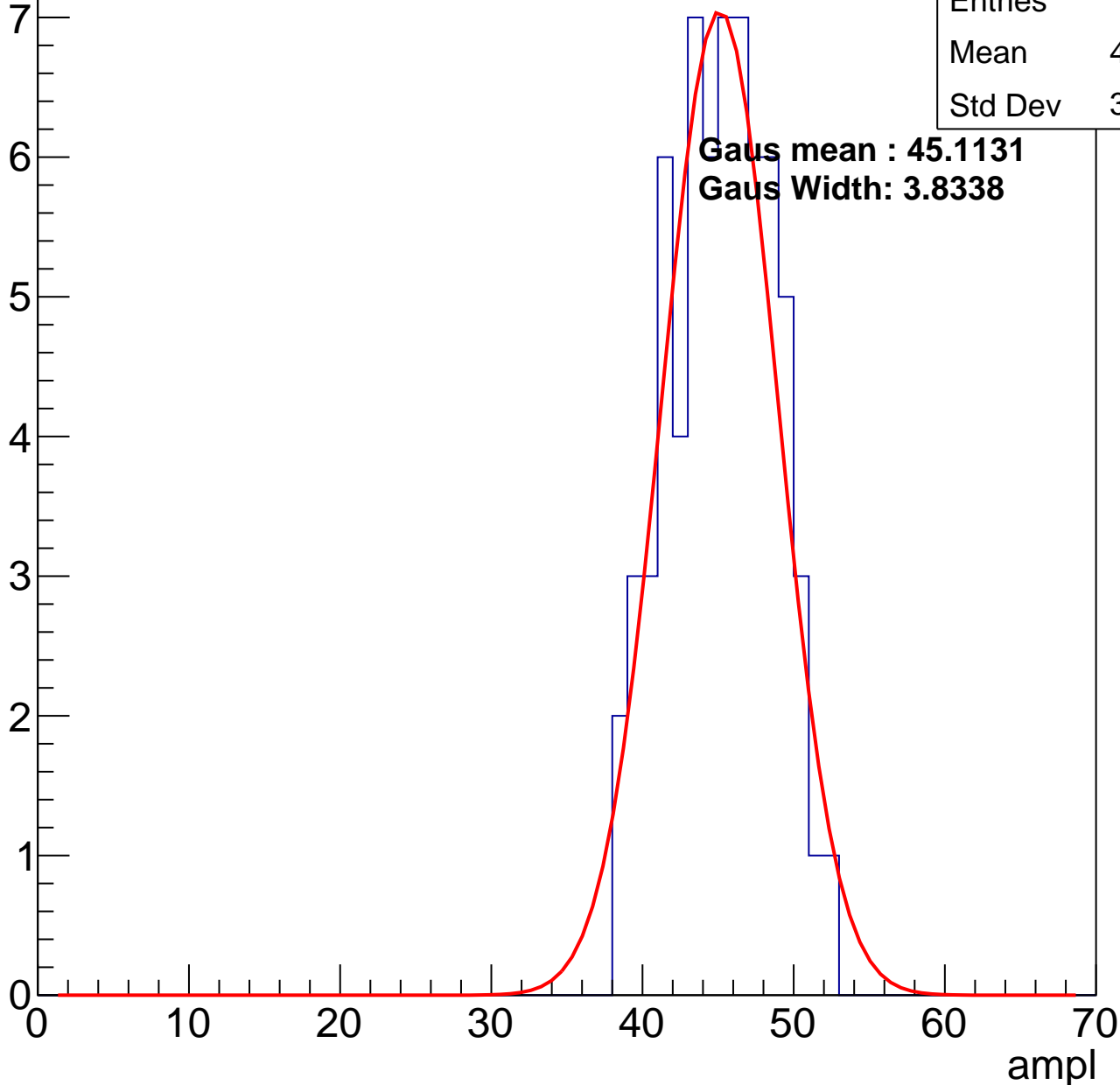
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	44.73
Std Dev	3.384

**Gaus mean : 45.1131**

**Gaus Width: 3.8338**

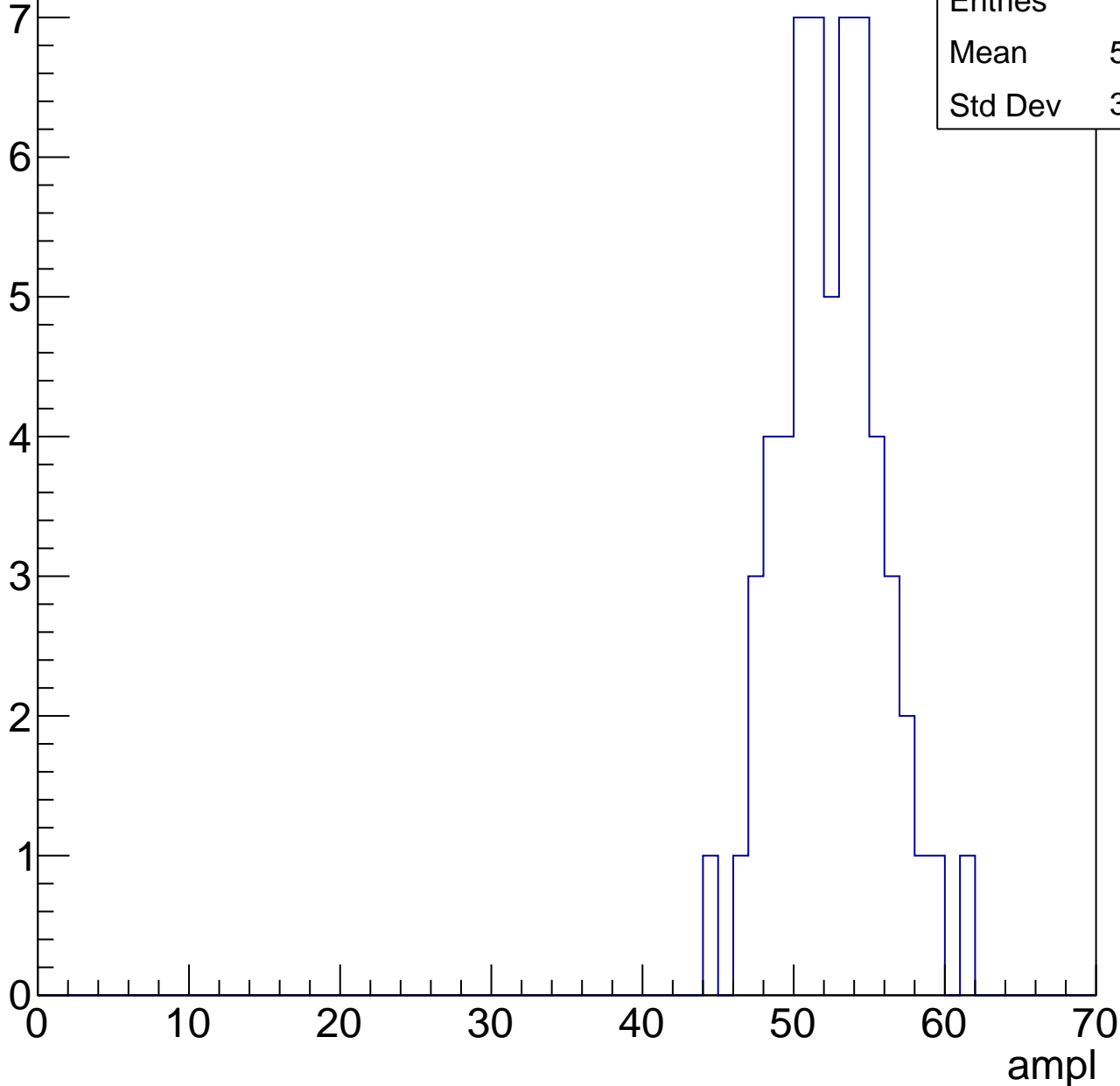


# B0L001S, U24-ch32, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

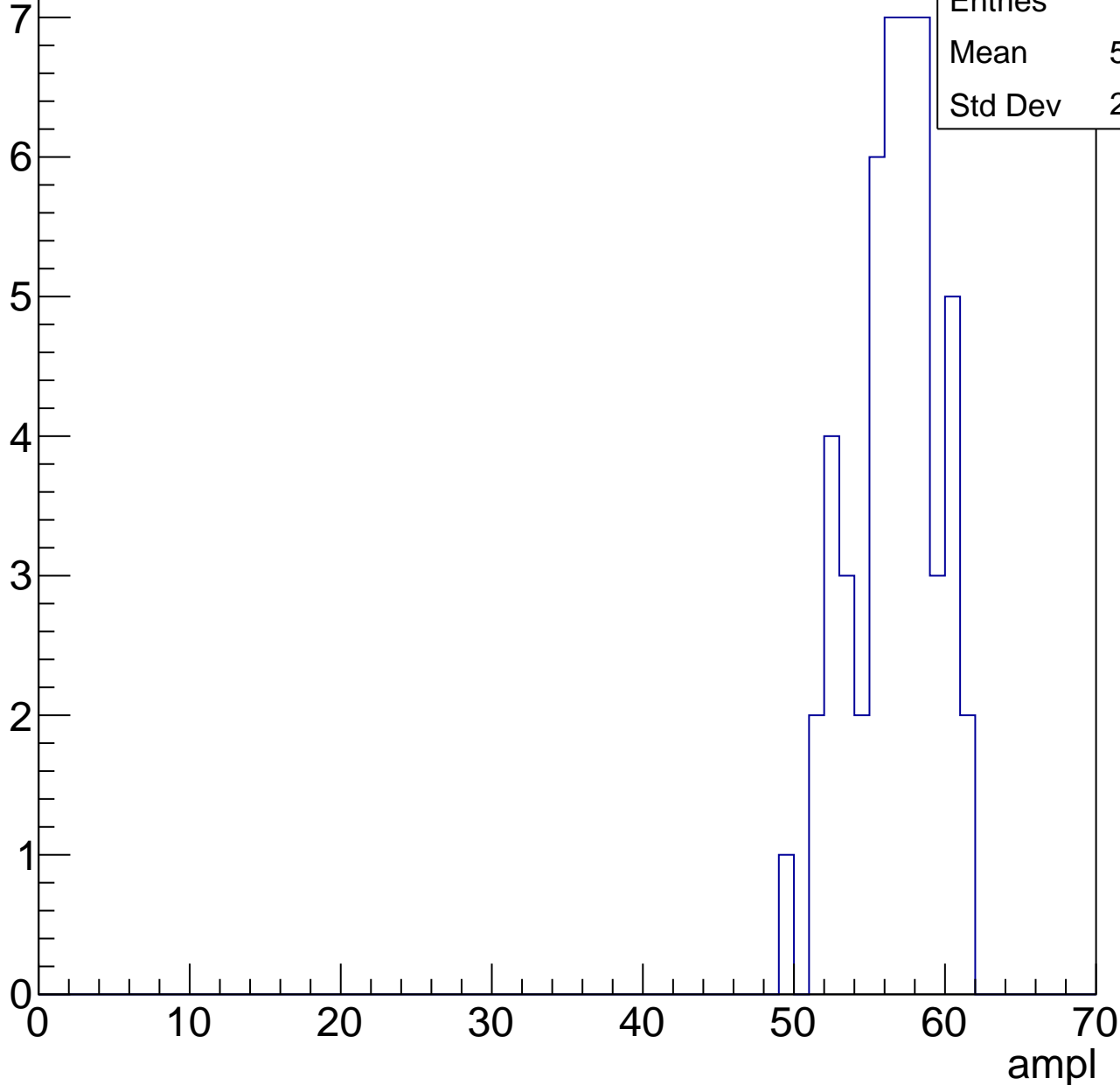
Entries	58
Mean	51.98
Std Dev	3.335



# B0L001S, U24-ch32, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

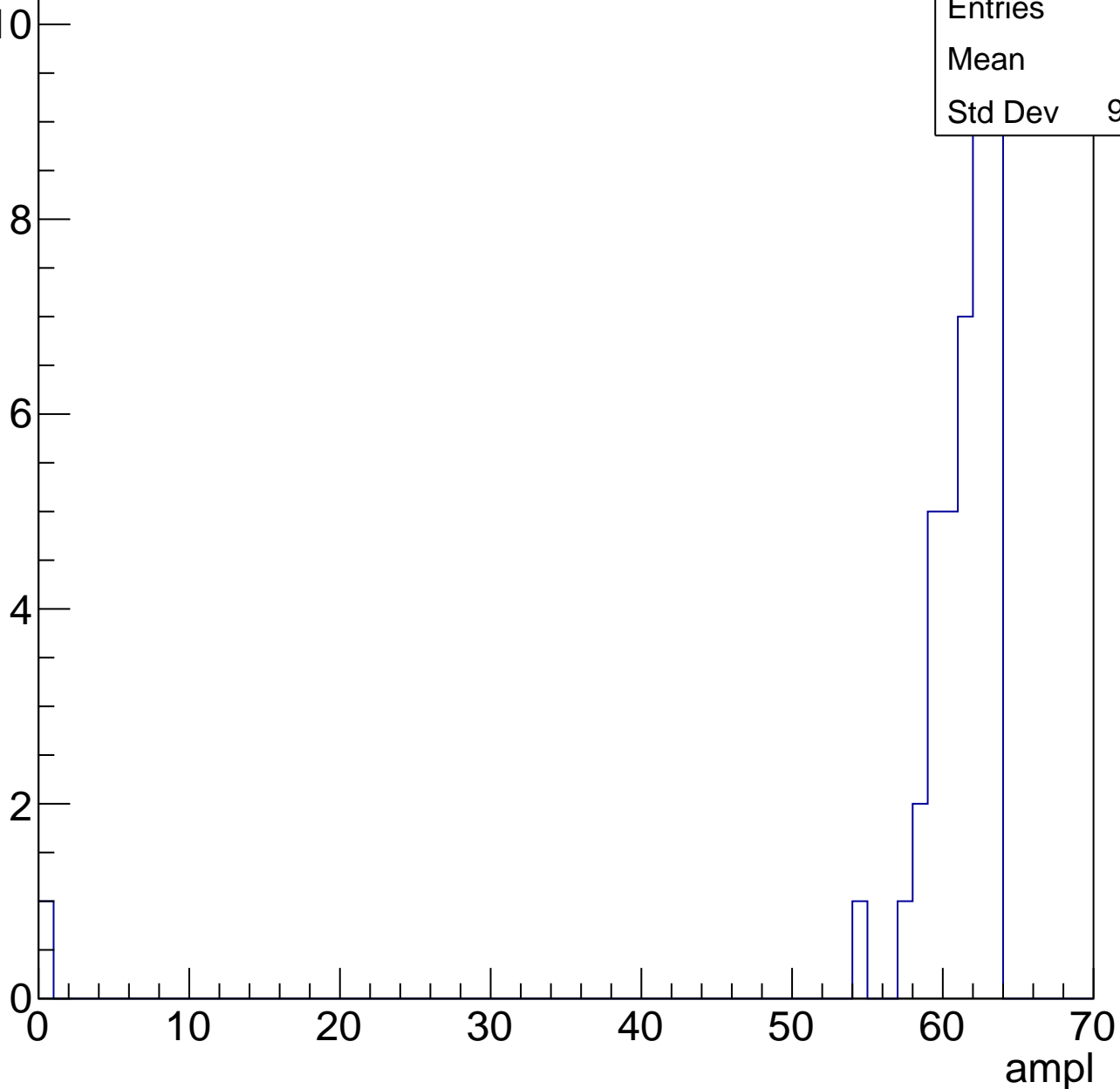


# B0L001S, U24-ch32, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	42
Mean	59.5
Std Dev	9.492



# B0L001S, U24-ch32, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch32, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U24-ch33, adc0

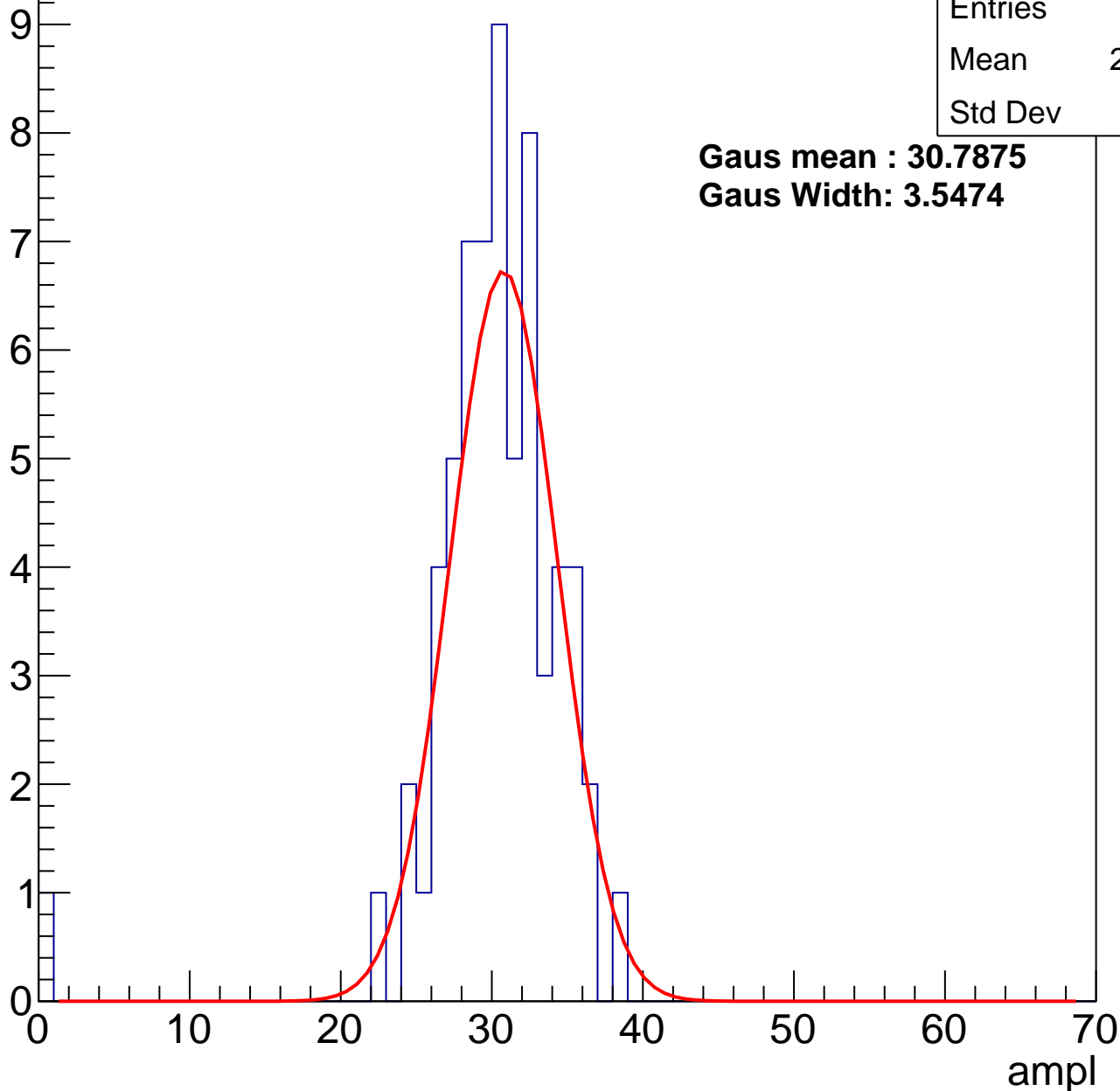
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	29.67
Std Dev	4.94

**Gaus mean : 30.7875**

**Gaus Width: 3.5474**



# B0L001S, U24-ch33, adc1

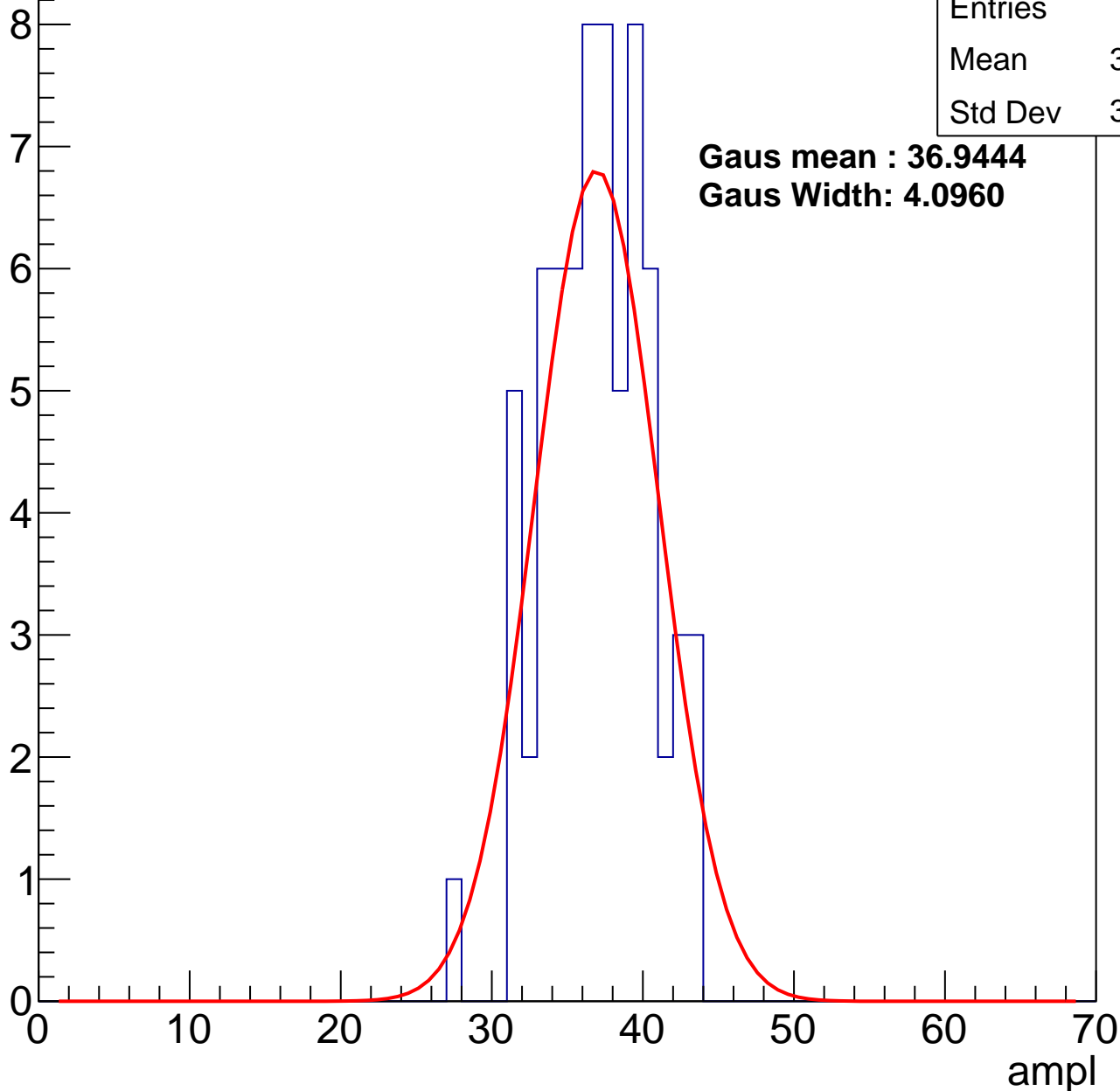
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	36.54
Std Dev	3.412

**Gaus mean : 36.9444**

**Gaus Width: 4.0960**



# B0L001S, U24-ch33, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	43.8
Std Dev	3.3

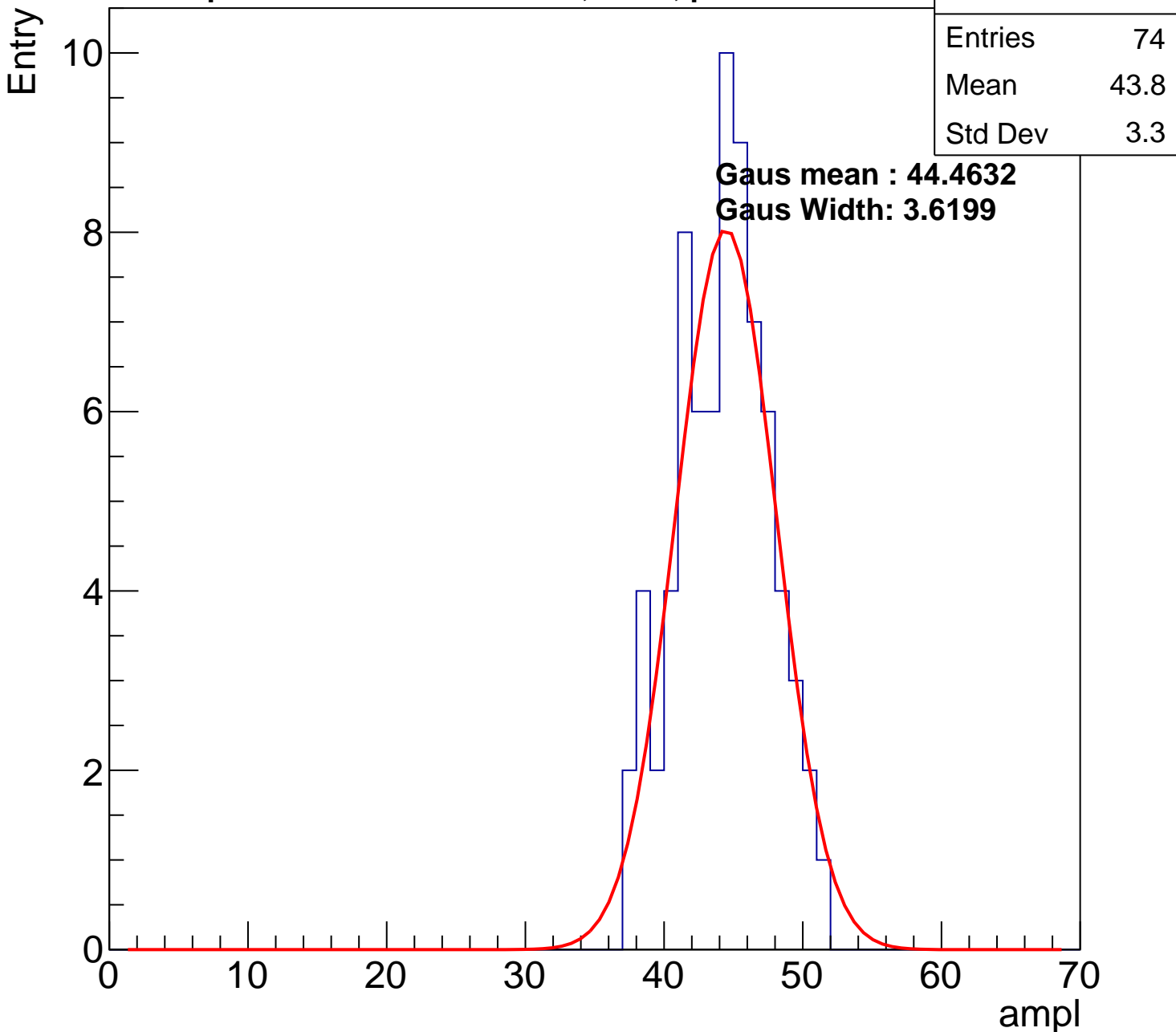
**Gaus mean : 44.4632**

**Gaus Width: 3.6199**

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

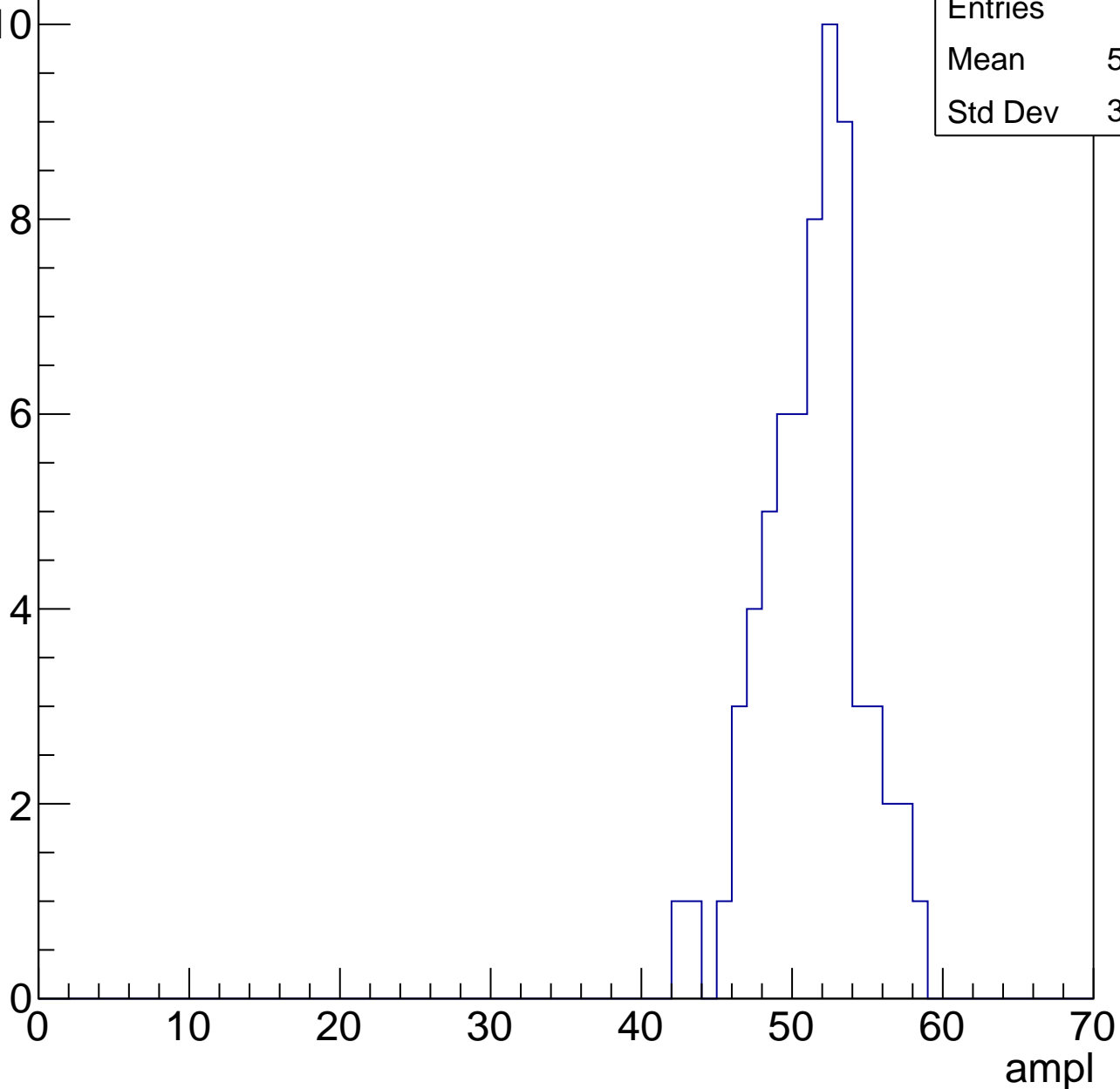


# B0L001S, U24-ch33, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	50.86
Std Dev	3.248

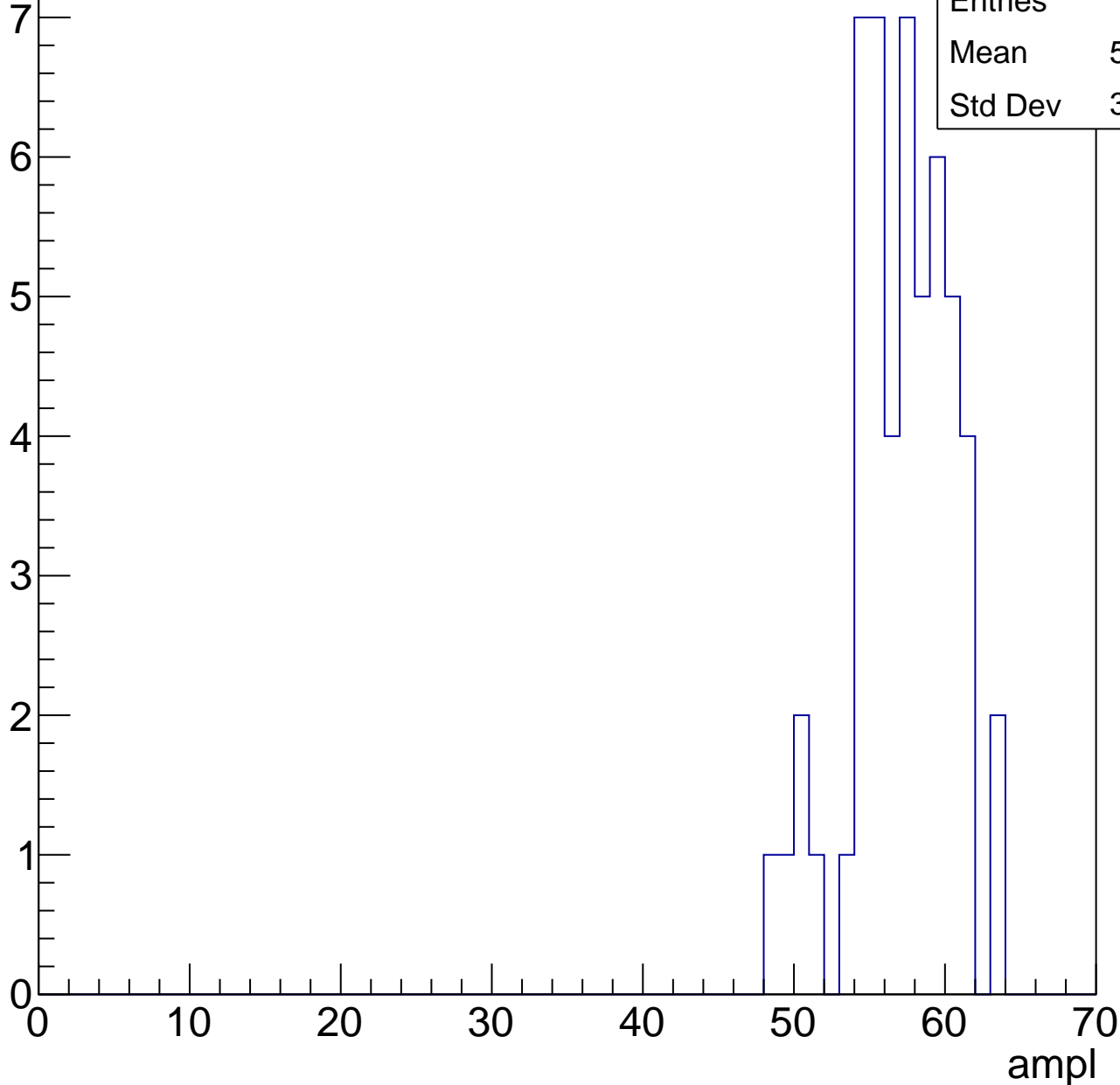


# B0L001S, U24-ch33, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	56.62
Std Dev	3.343

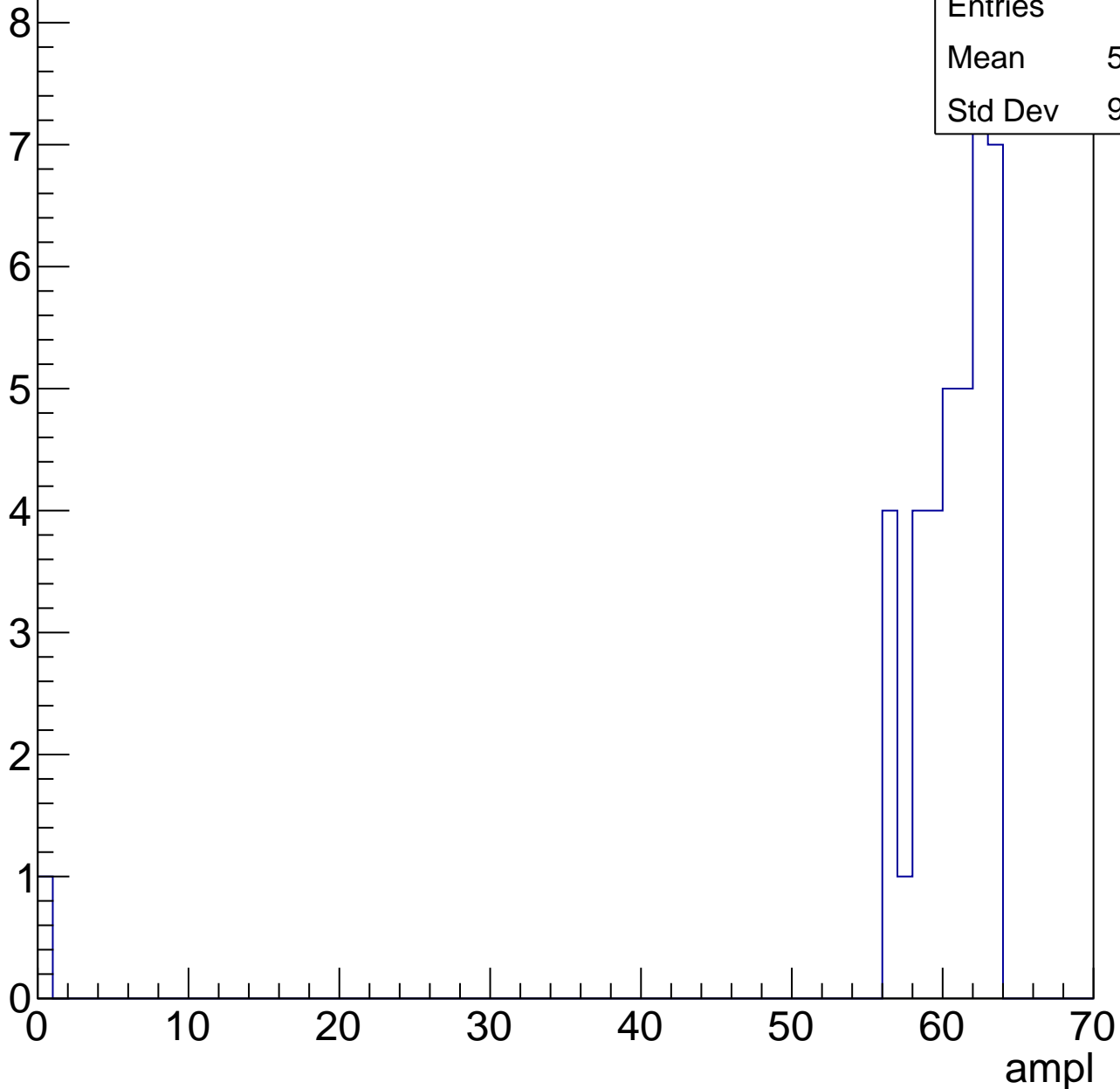


# B0L001S, U24-ch33, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	39
Mean	58.74
Std Dev	9.782



# B0L001S, U24-ch33, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

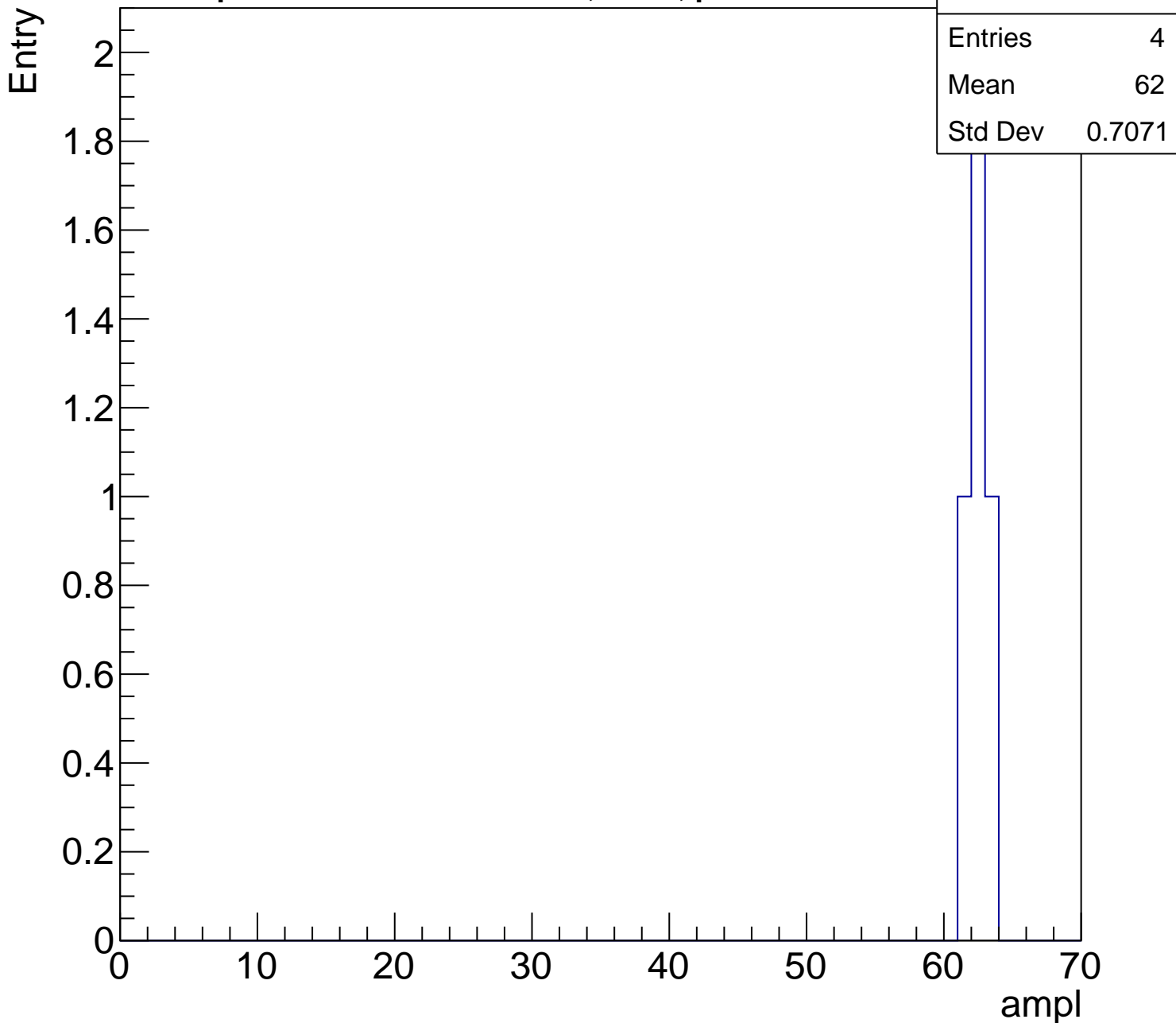
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	62
Std Dev	0.7071

ampl

0 10 20 30 40 50 60 70





# B0L001S, U24-ch33, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U24-ch34, adc0

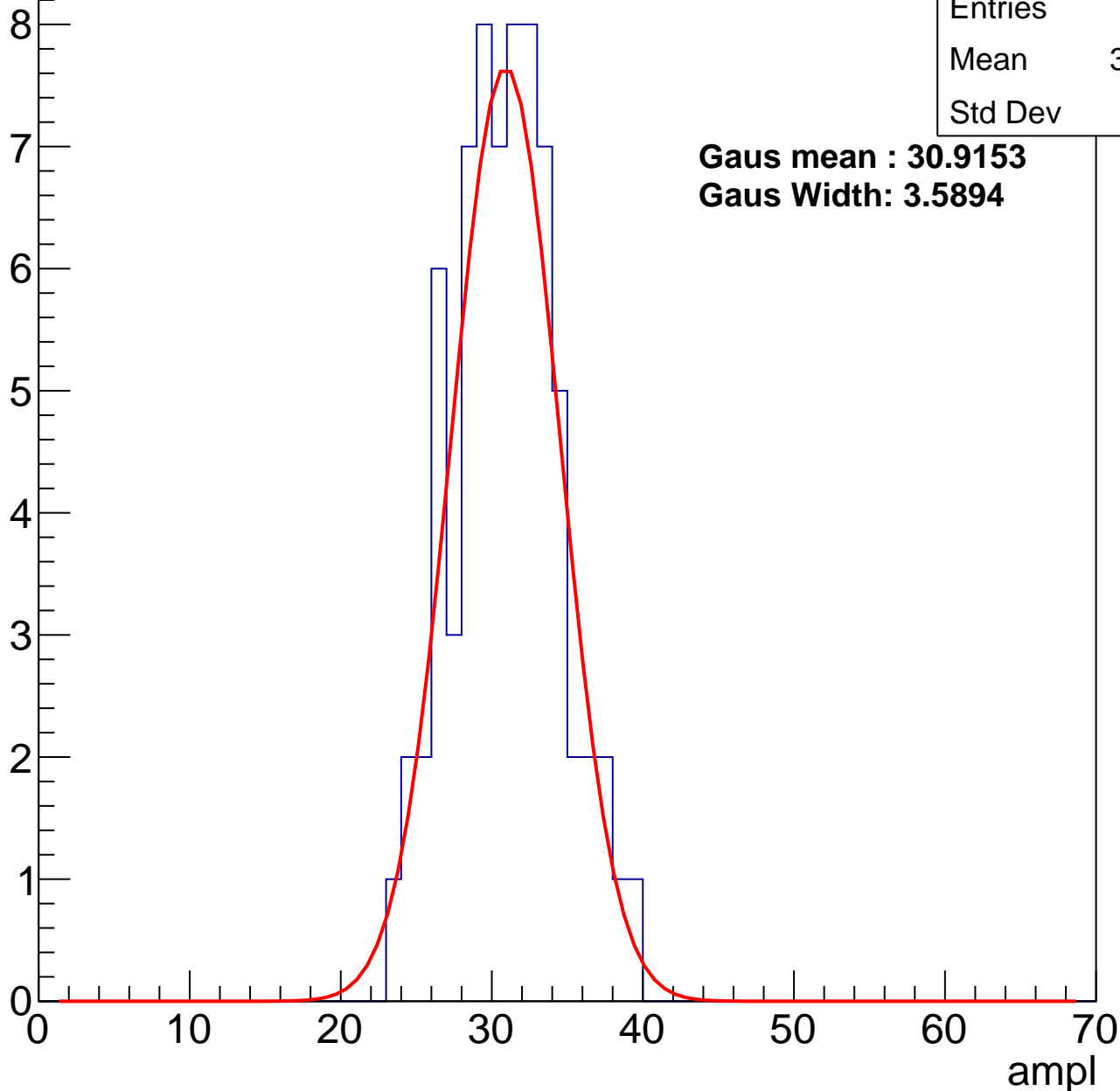
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	30.47
Std Dev	3.46

**Gaus mean : 30.9153**

**Gaus Width: 3.5894**



# B0L001S, U24-ch34, adc1

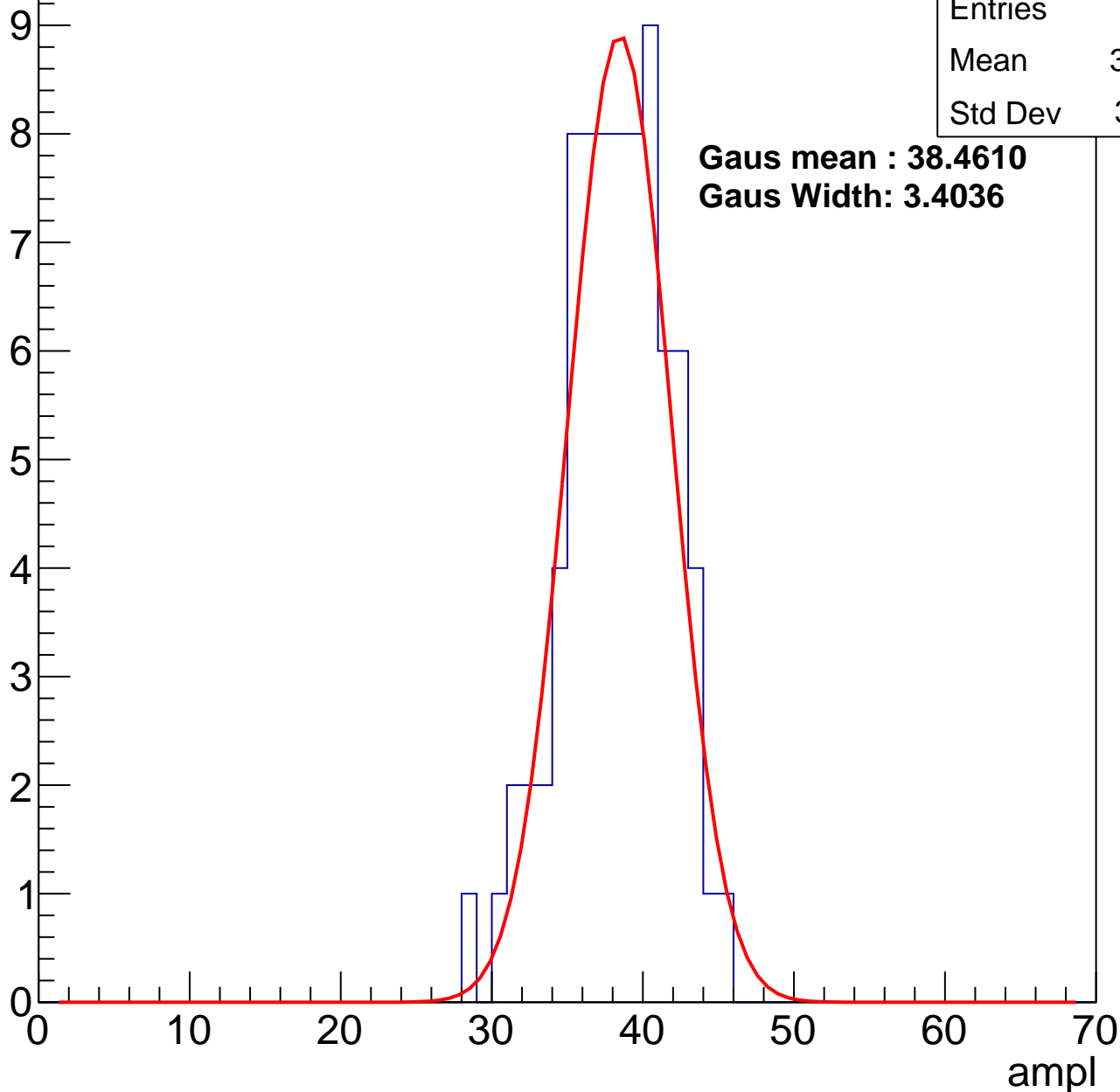
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	79
Mean	37.78
Std Dev	3.441

**Gaus mean : 38.4610**

**Gaus Width: 3.4036**



# B0L001S, U24-ch34, adc2

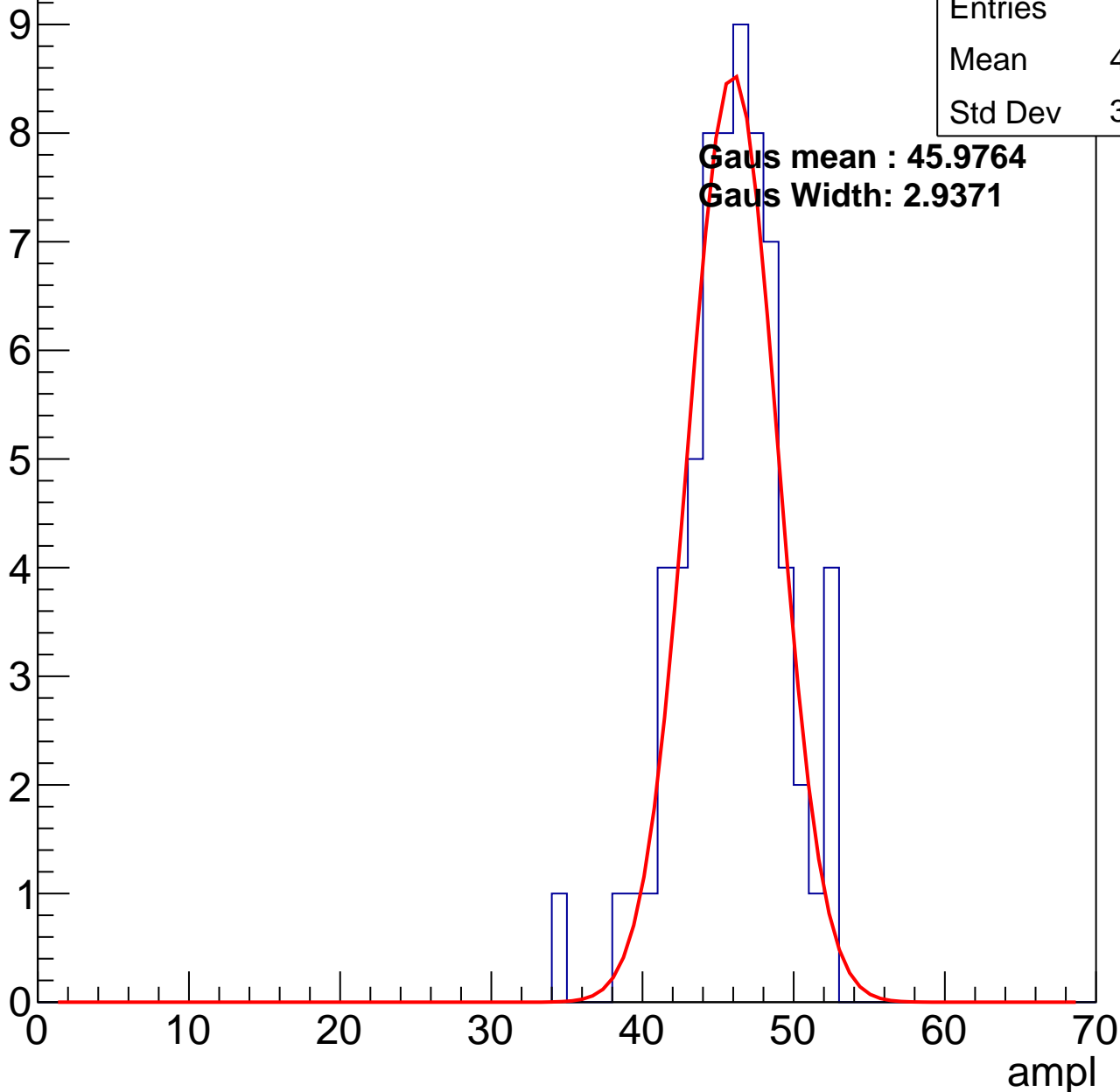
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	45.46
Std Dev	3.419

**Gaus mean : 45.9764**

**Gaus Width: 2.9371**



# B0L001S, U24-ch34, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	68
Mean	51.82
Std Dev	3.267

Entry

10

8

6

4

2

0

0

10

20

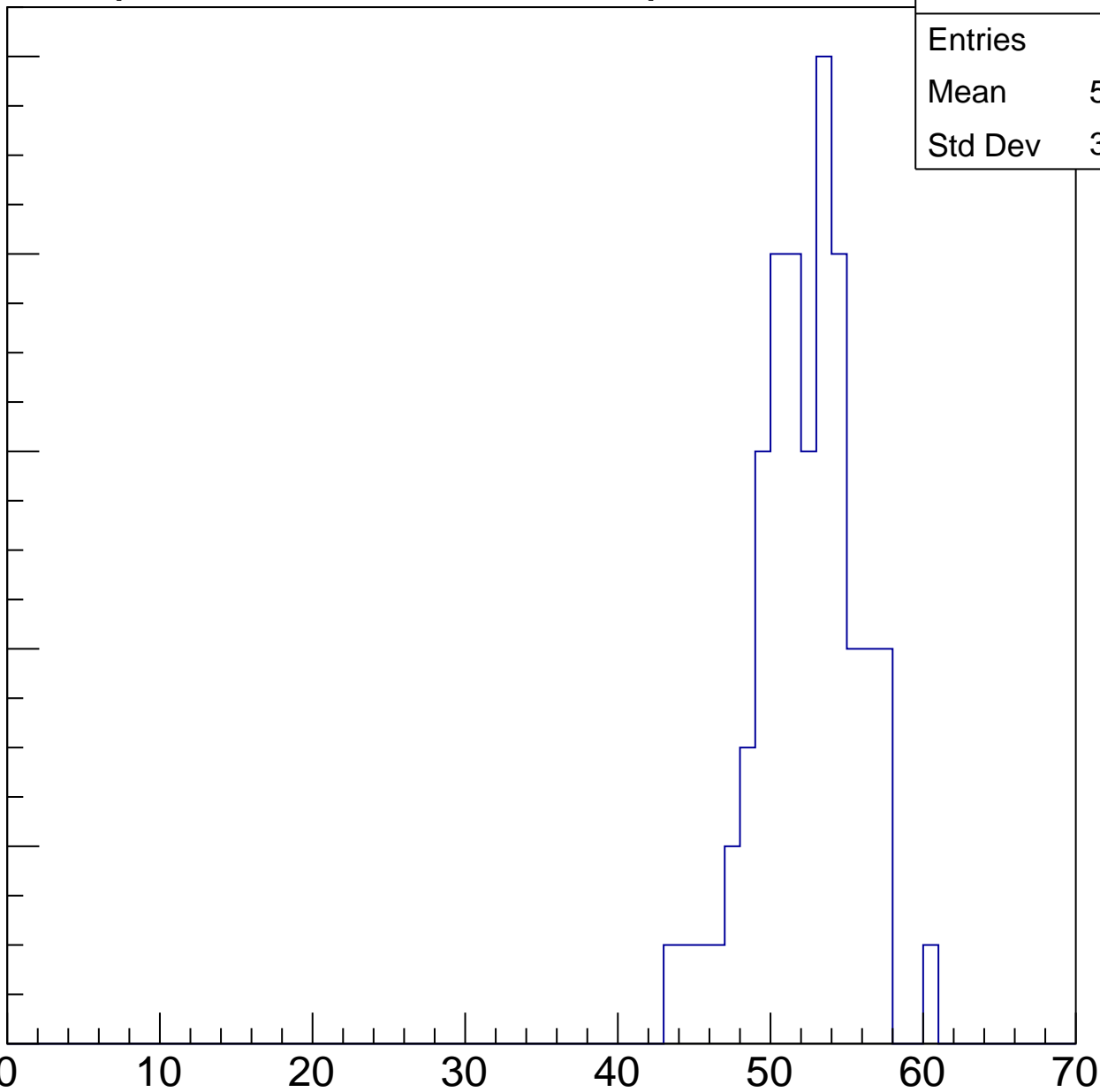
30

40

50

60

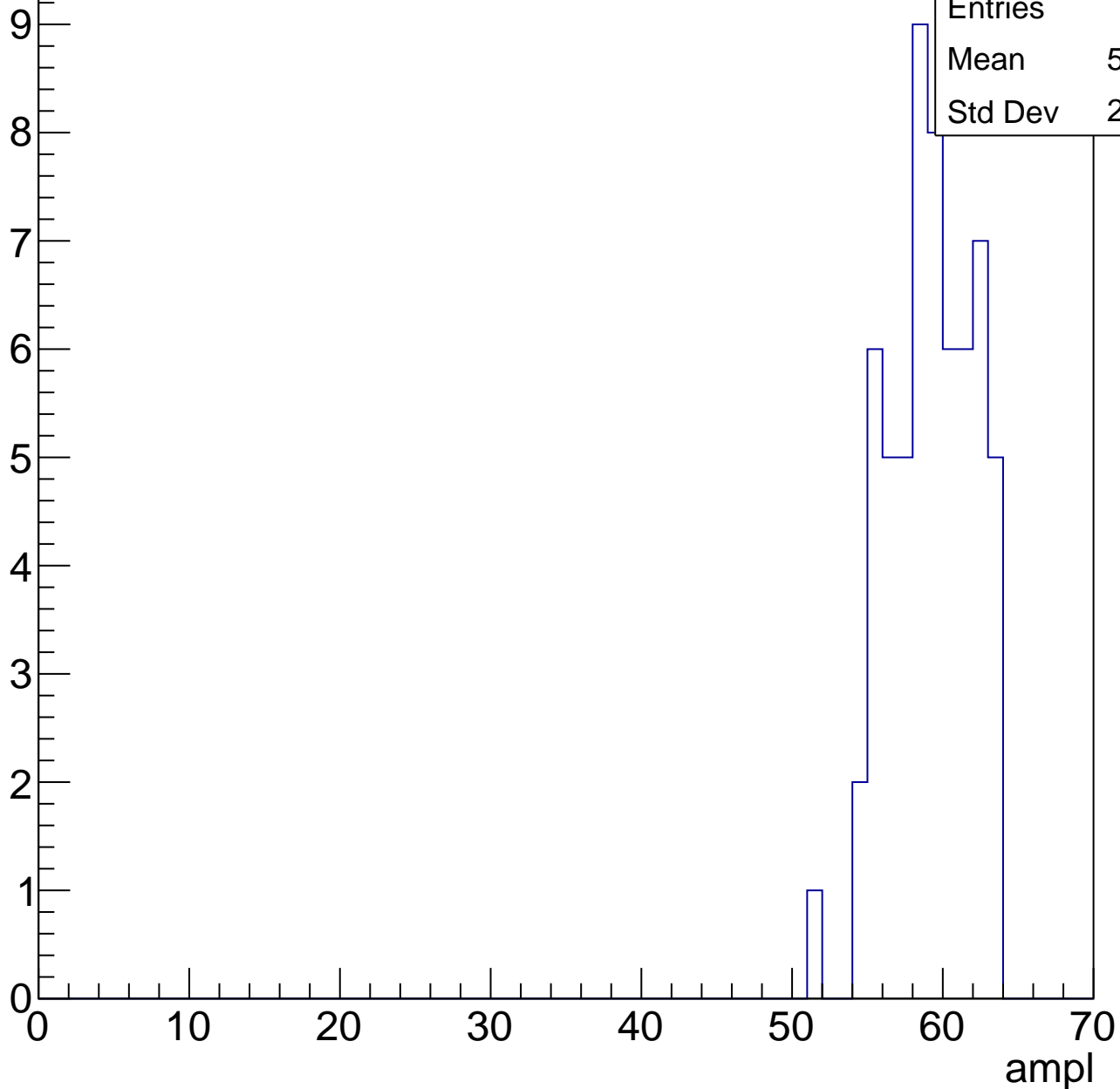
ampl



# B0L001S, U24-ch34, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

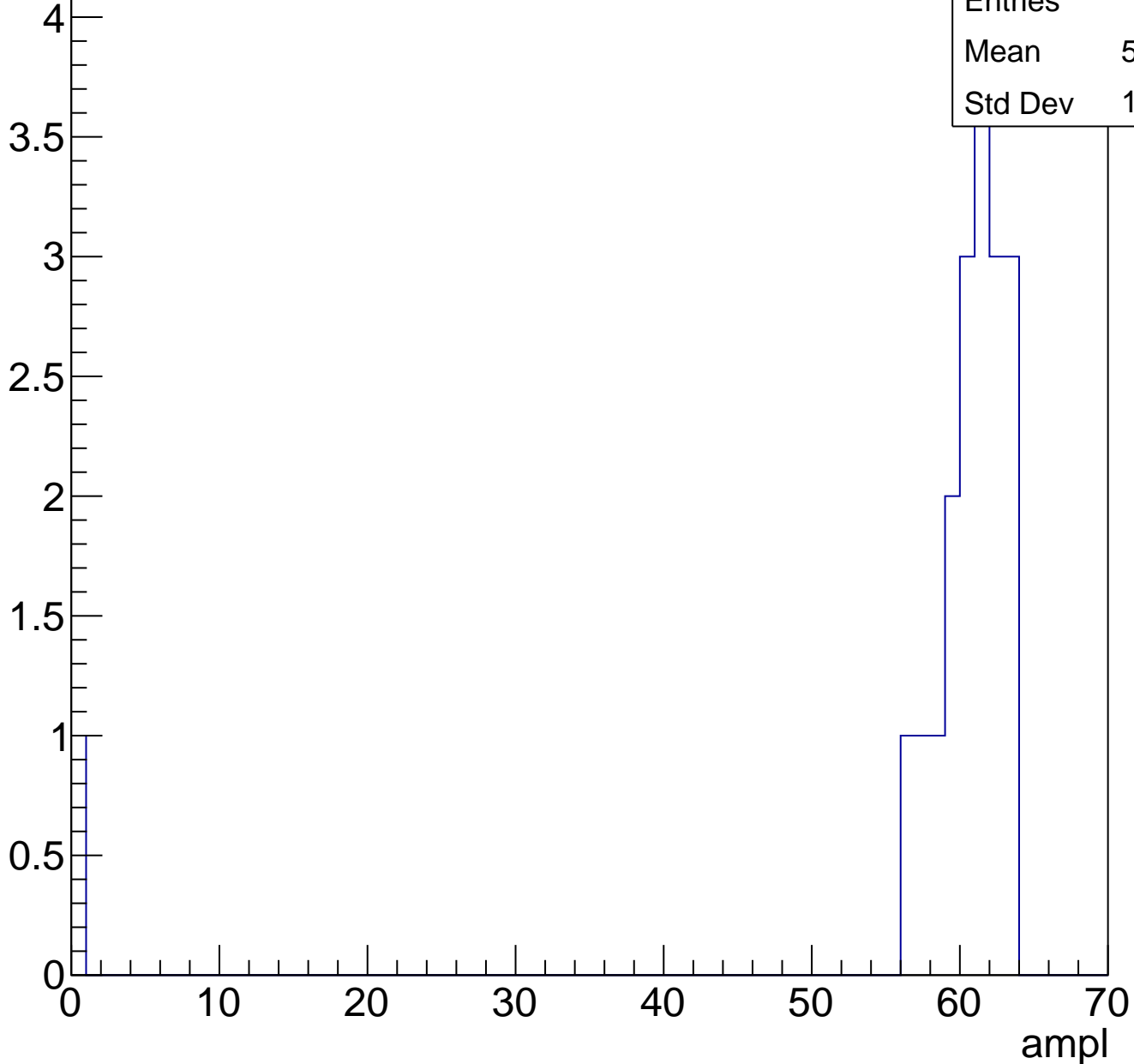
Entry



# B0L001S, U24-ch34, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U24-ch34, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch34, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U24-ch35, adc0

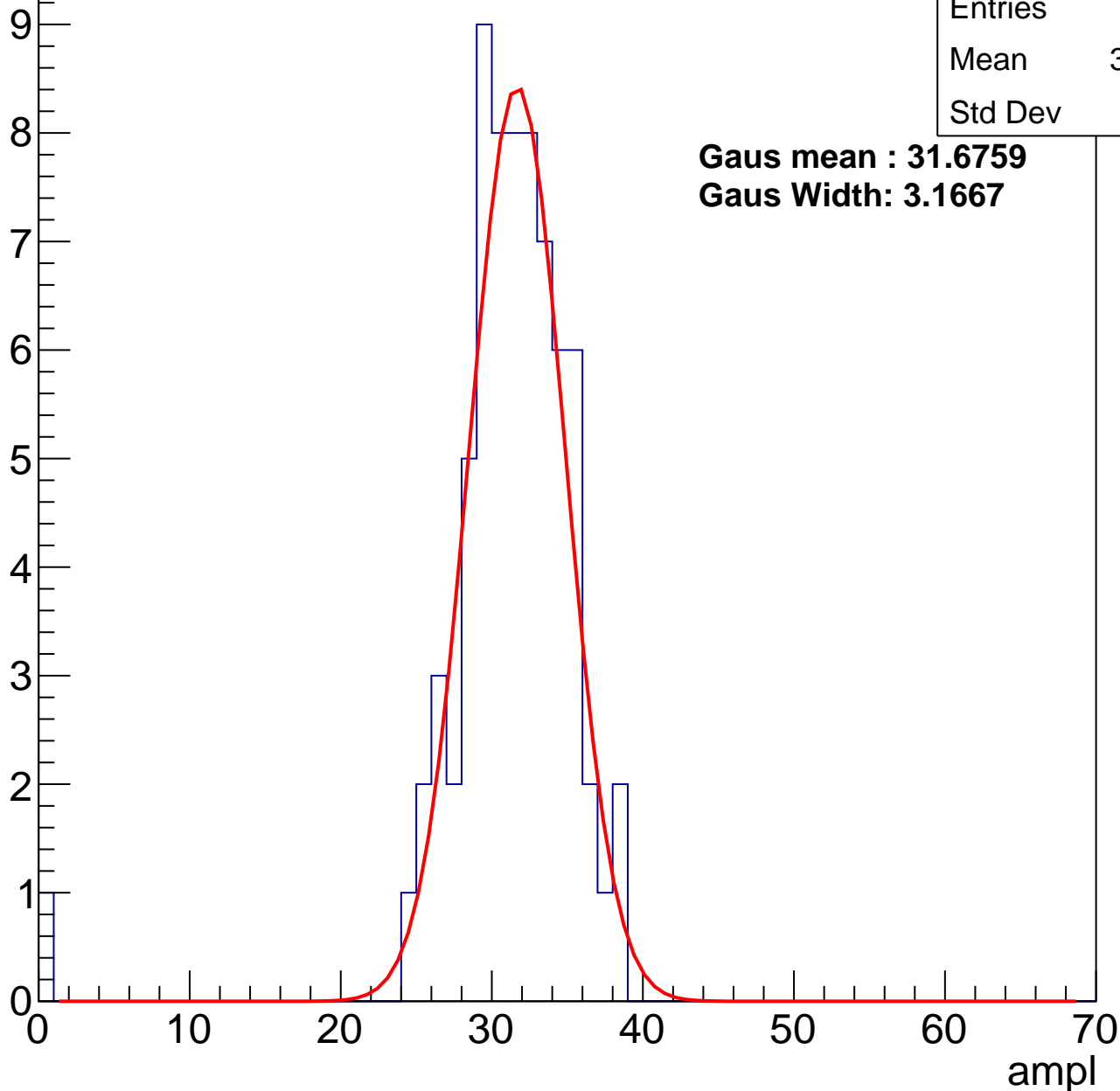
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	30.72
Std Dev	4.81

**Gaus mean : 31.6759**

**Gaus Width: 3.1667**



# B0L001S, U24-ch35, adc1

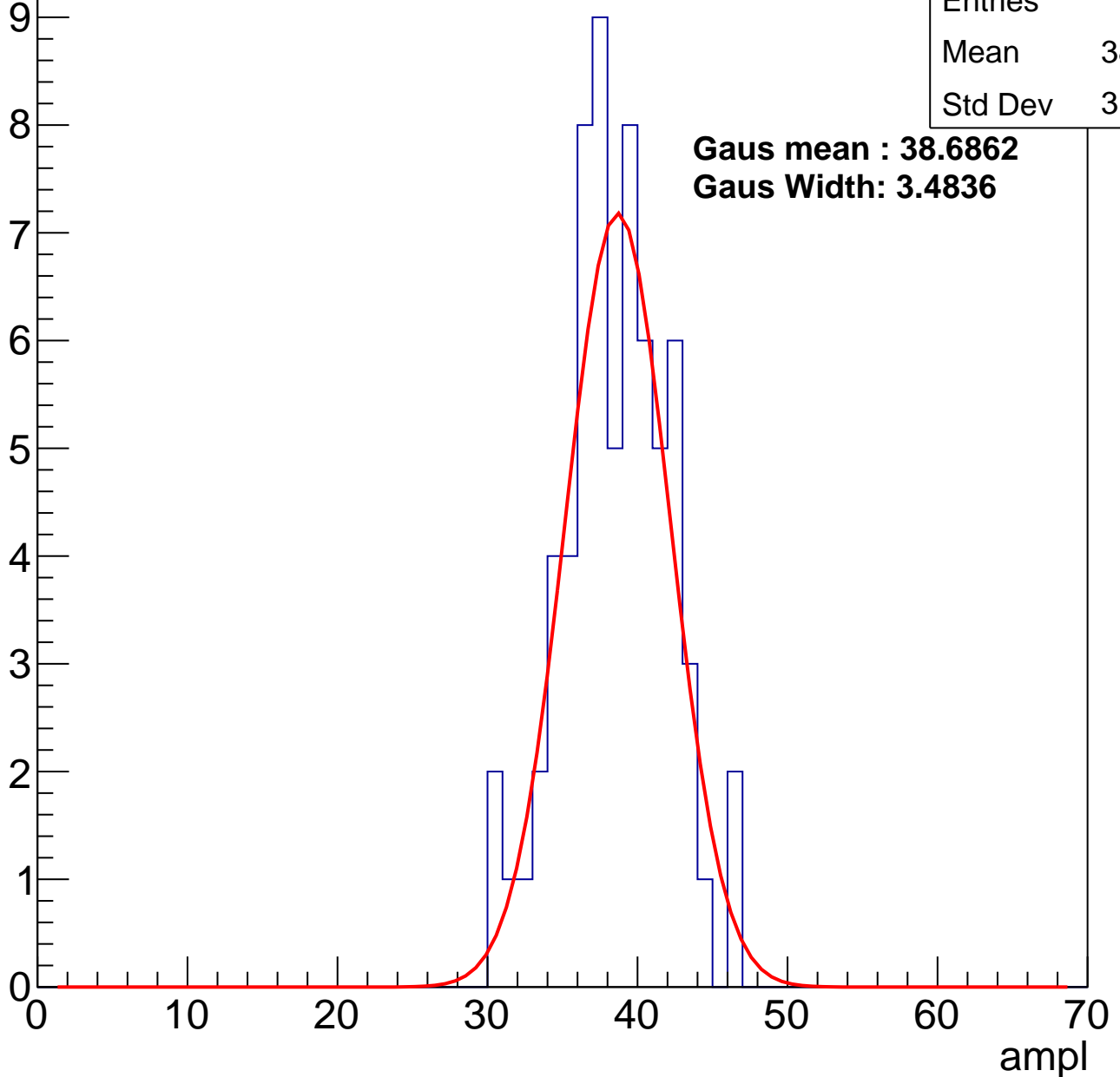
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	38.06
Std Dev	3.489

**Gaus mean : 38.6862**

**Gaus Width: 3.4836**



# B0L001S, U24-ch35, adc2

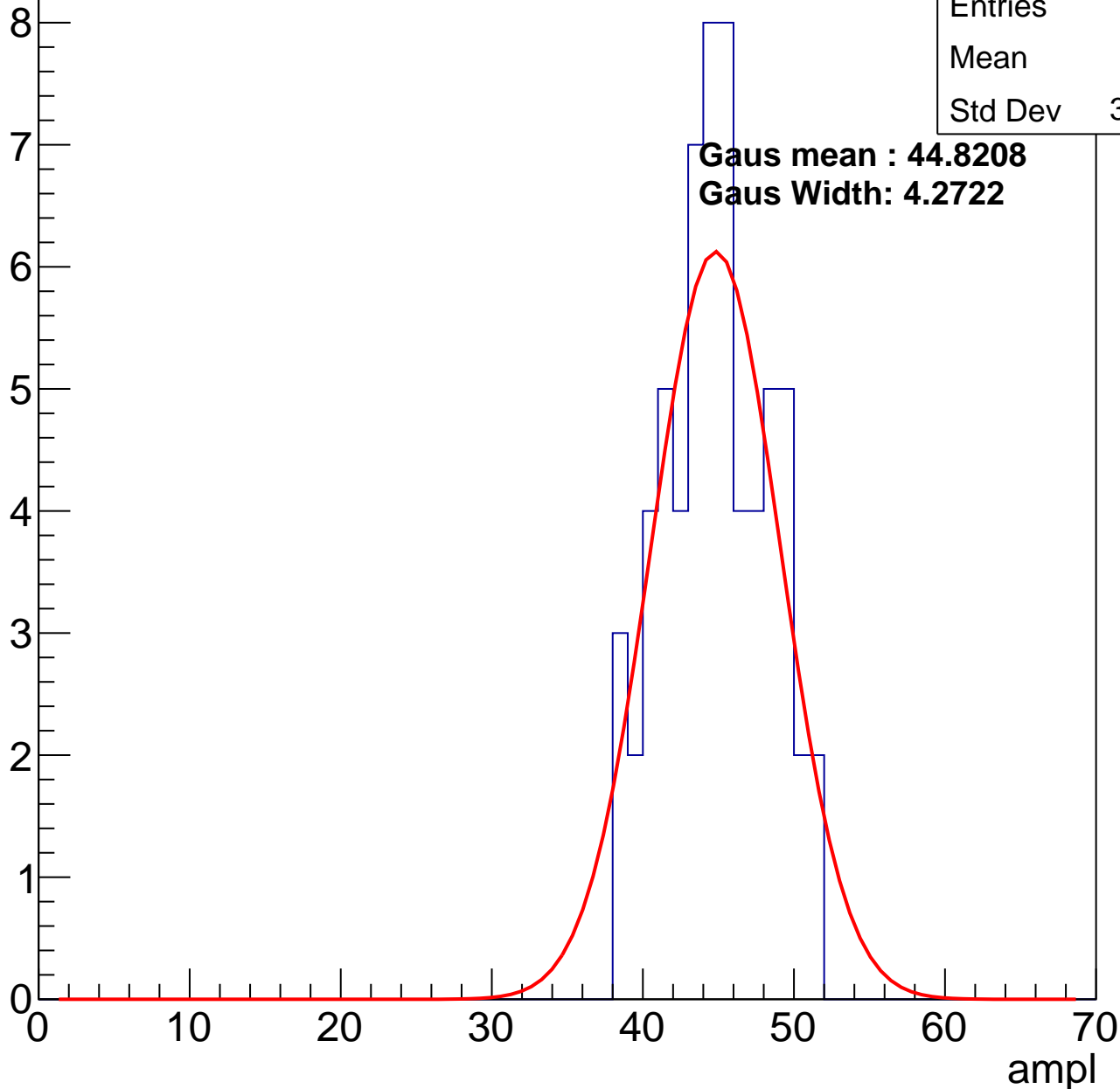
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	44.4
Std Dev	3.369

**Gaus mean : 44.8208**

**Gaus Width: 4.2722**

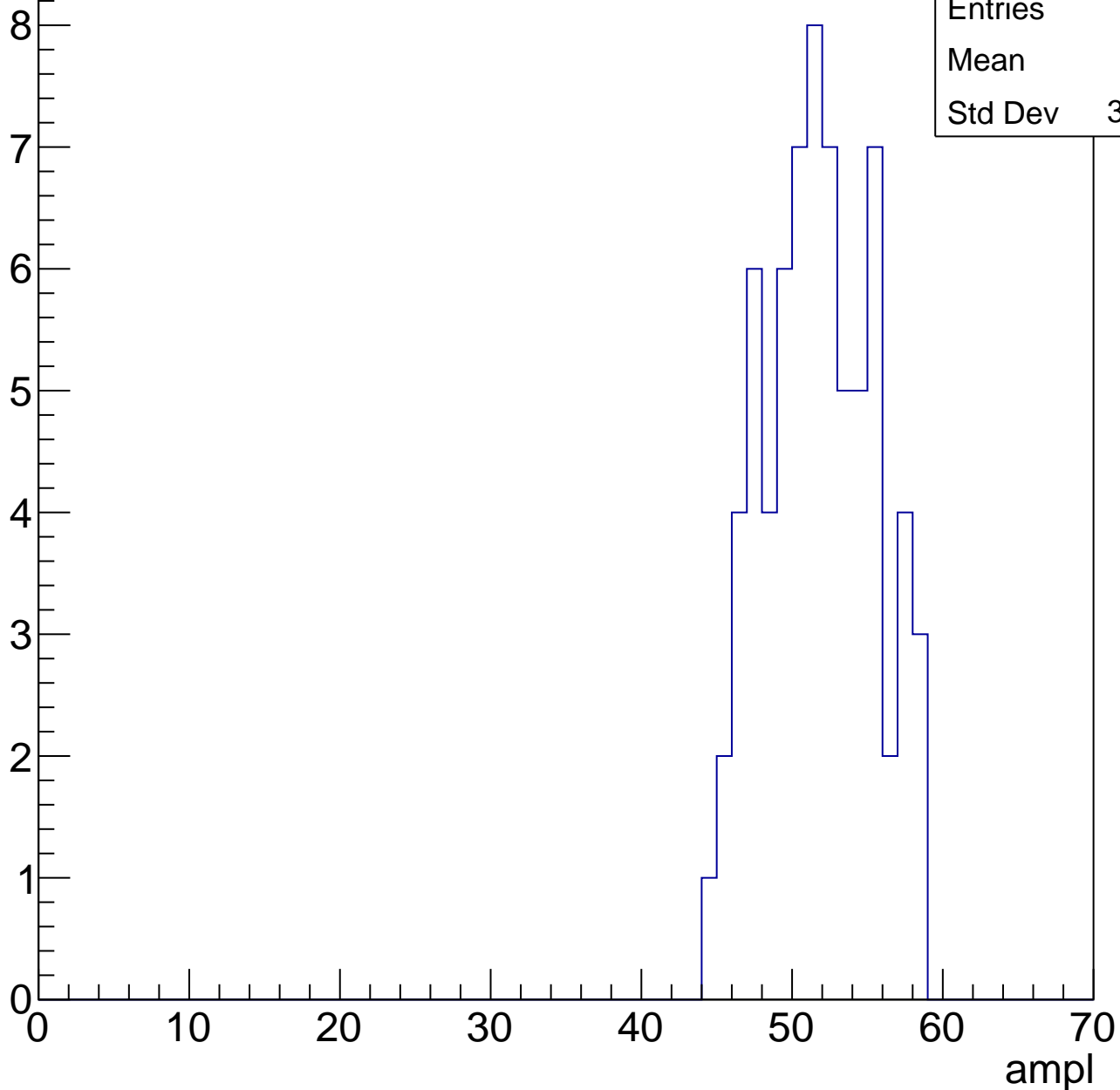


# B0L001S, U24-ch35, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	51.3
Std Dev	3.566

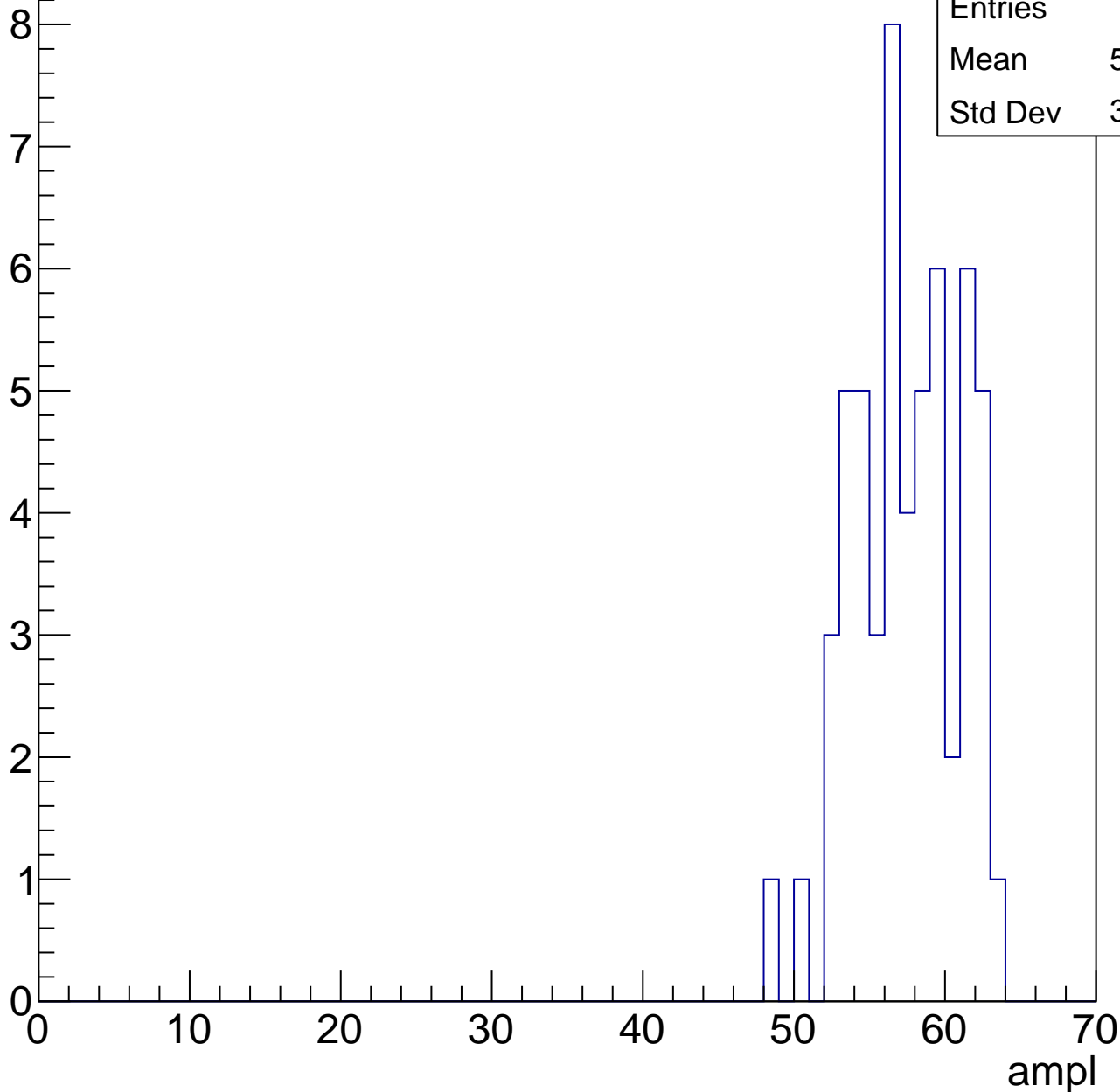


# B0L001S, U24-ch35, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

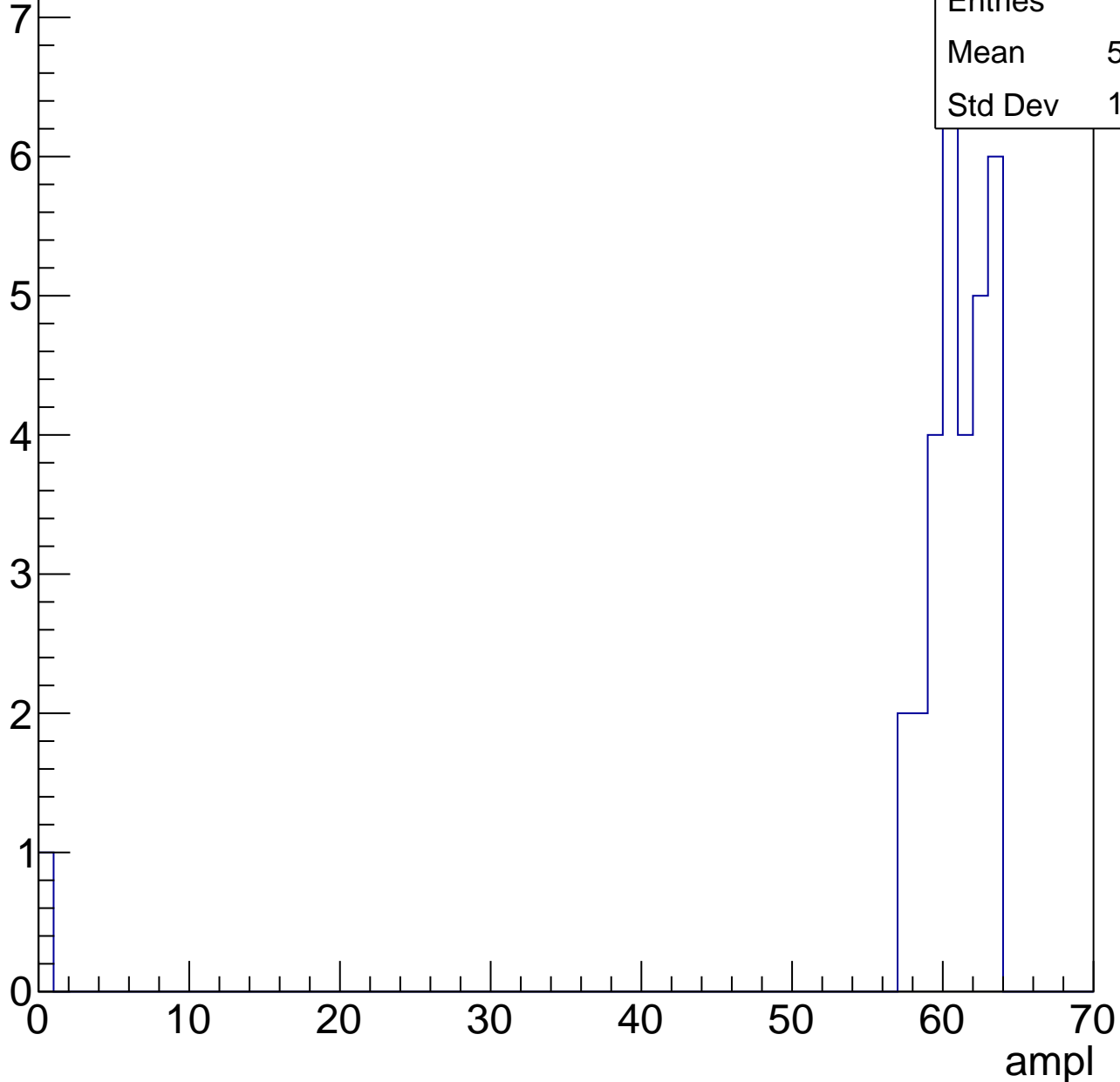
Entries	55
Mean	56.96
Std Dev	3.448



# B0L001S, U24-ch35, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U24-ch35, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch35, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U24-ch36, adc0

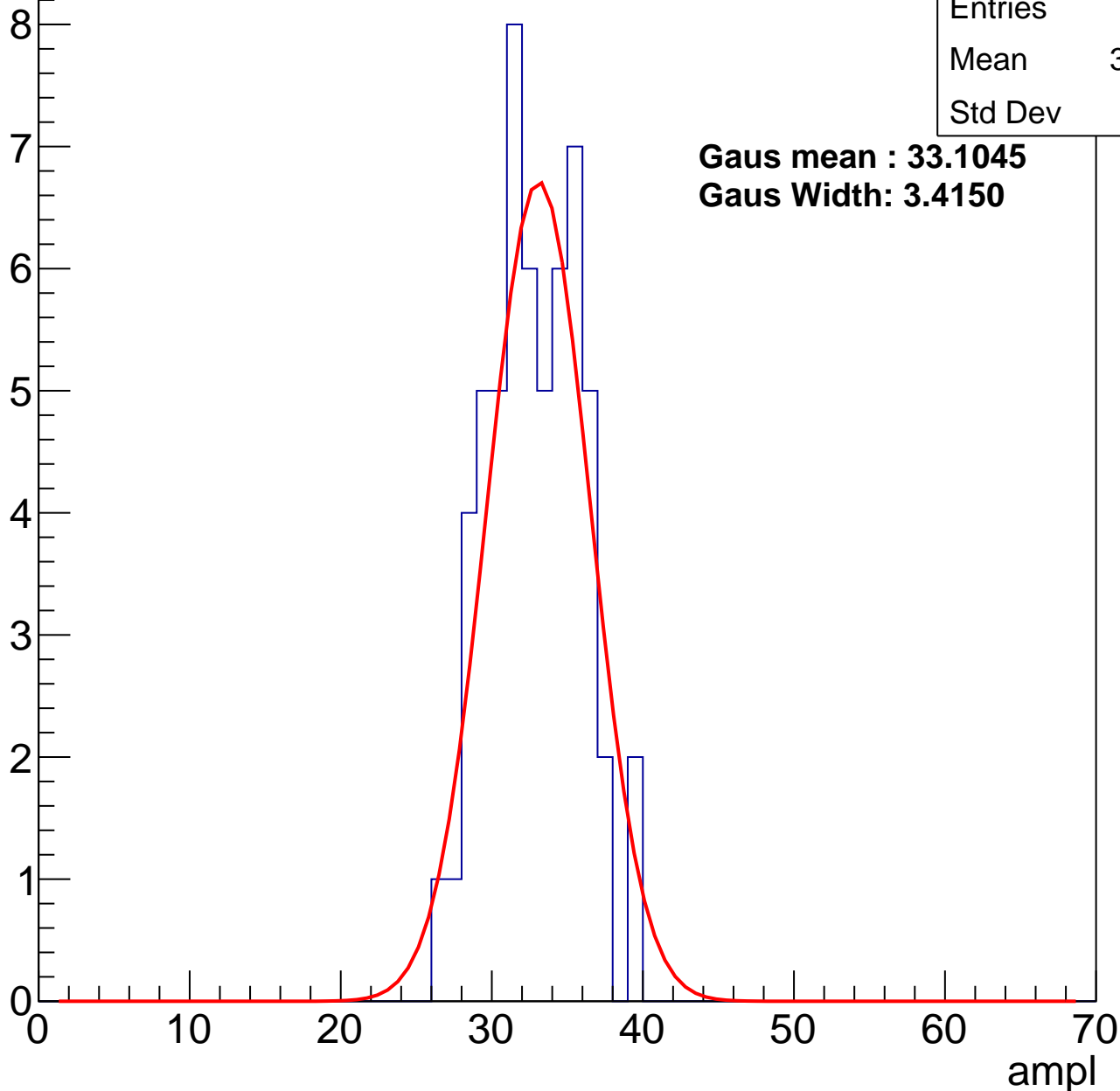
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	32.39
Std Dev	2.99

**Gaus mean : 33.1045**

**Gaus Width: 3.4150**



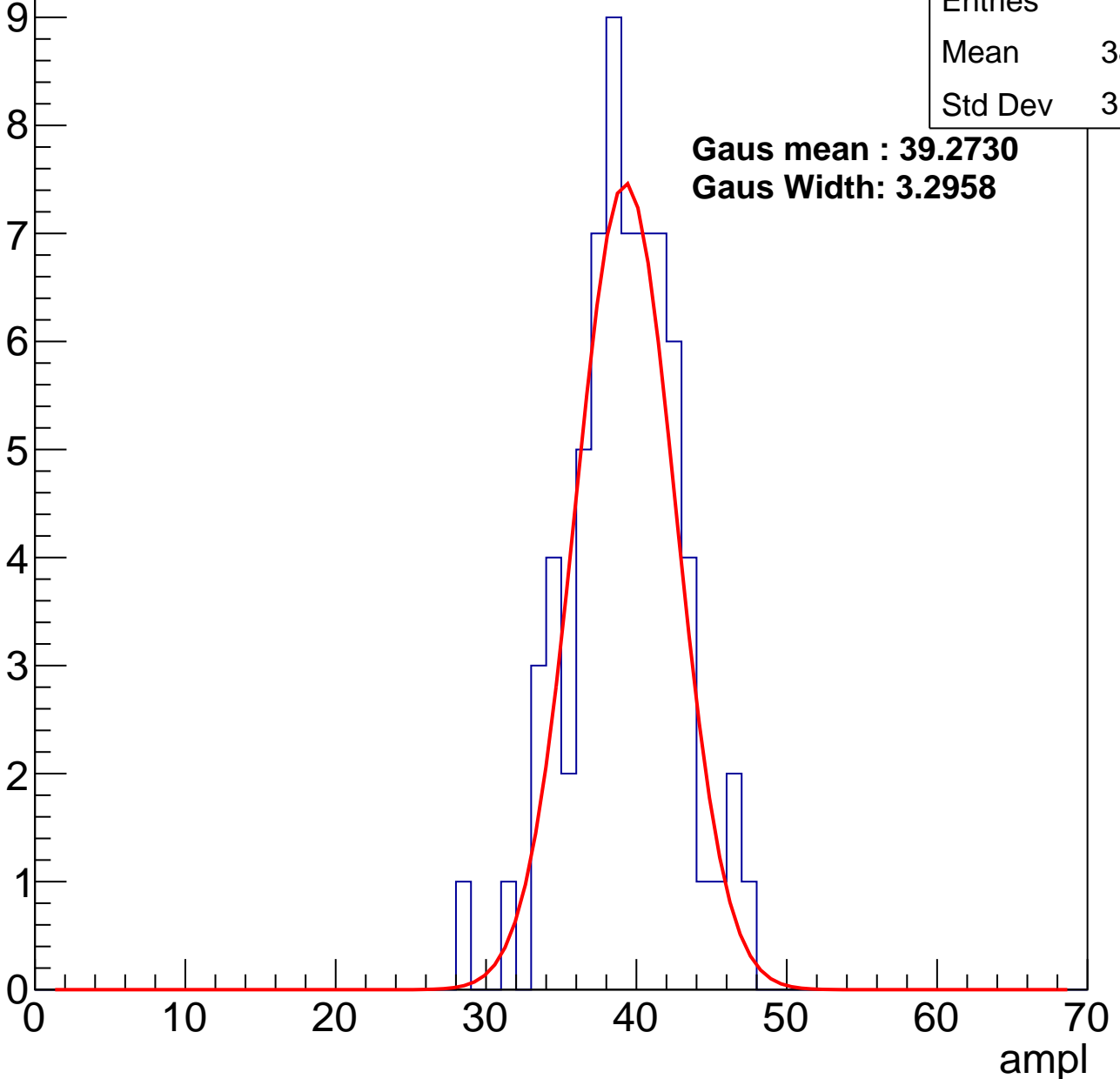
# B0L001S, U24-ch36, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	38.78
Std Dev	3.597

**Gaus mean : 39.2730**  
**Gaus Width: 3.2958**



# B0L001S, U24-ch36, adc2

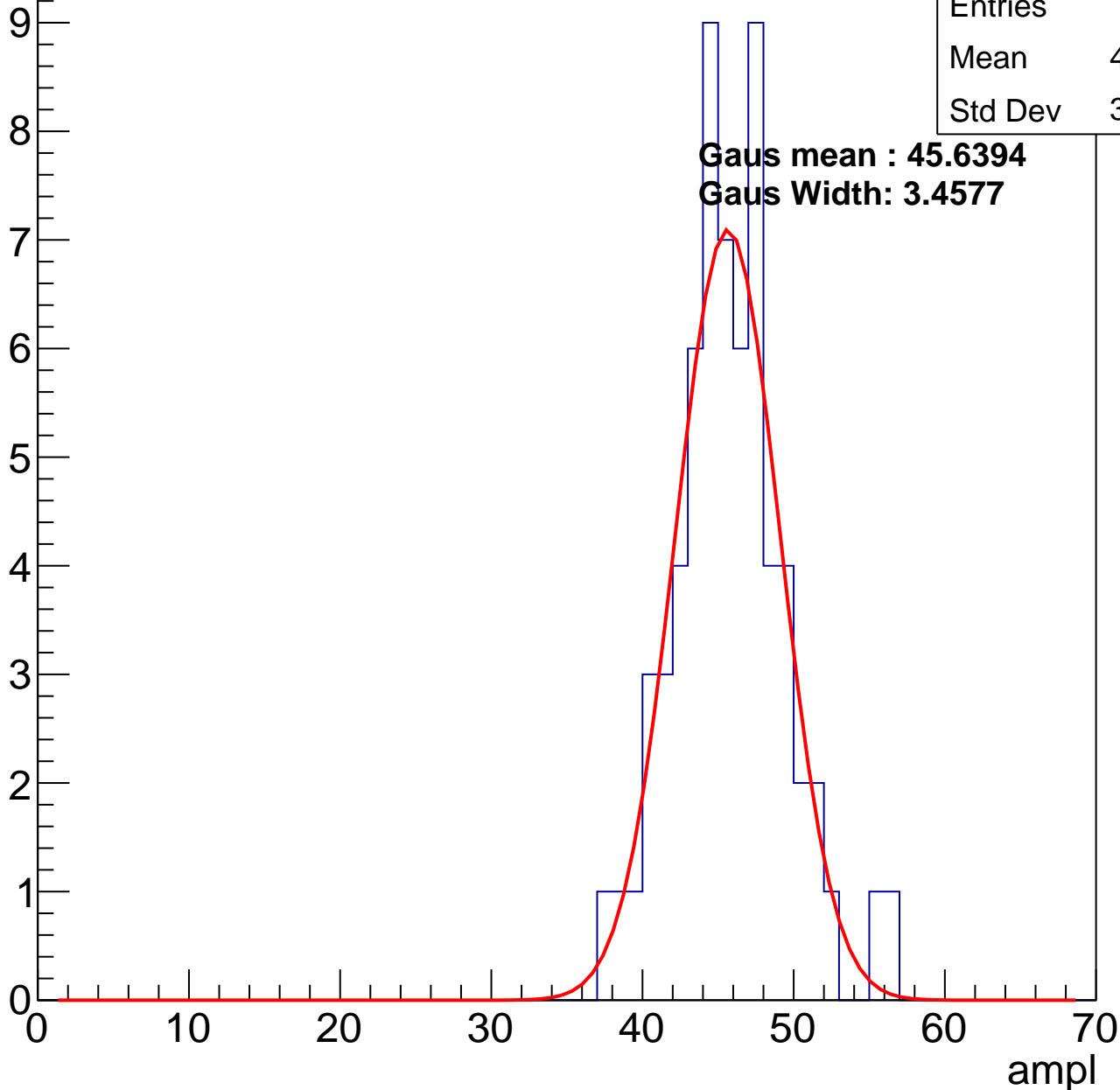
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	45.32
Std Dev	3.655

**Gaus mean : 45.6394**

**Gaus Width: 3.4577**

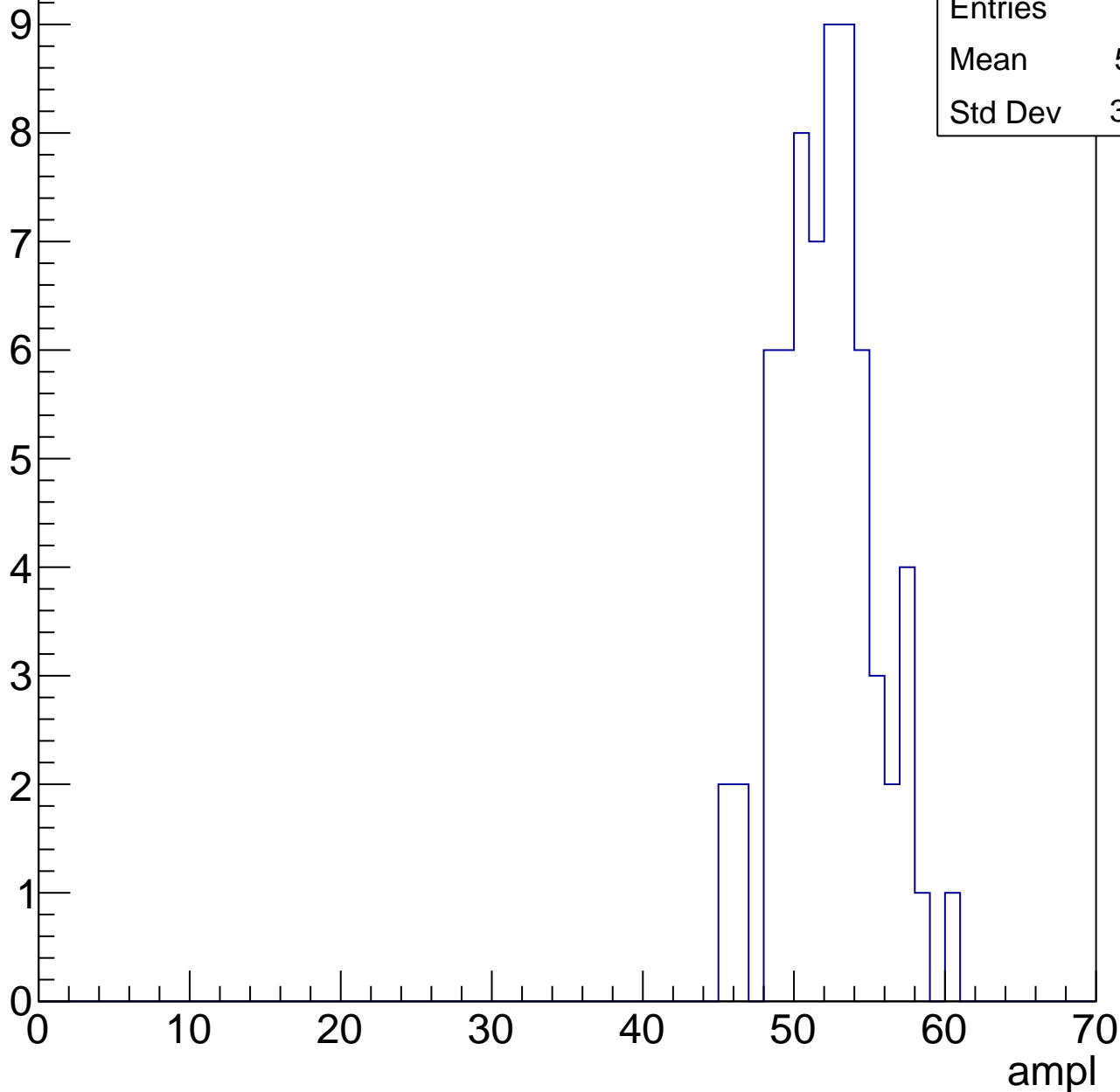


# B0L001S, U24-ch36, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	51.71
Std Dev	3.127

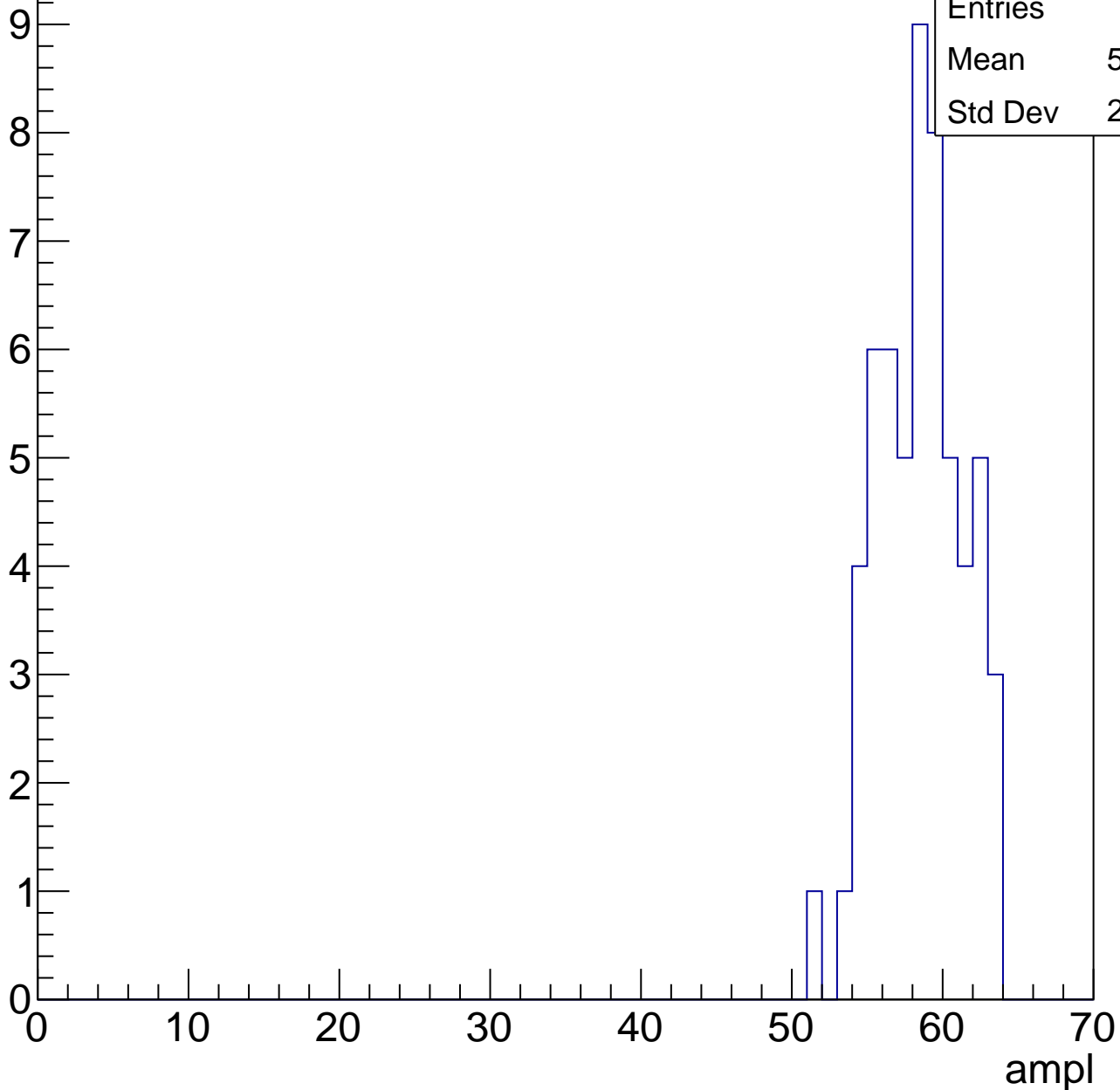


# B0L001S, U24-ch36, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	58.04
Std Dev	2.778

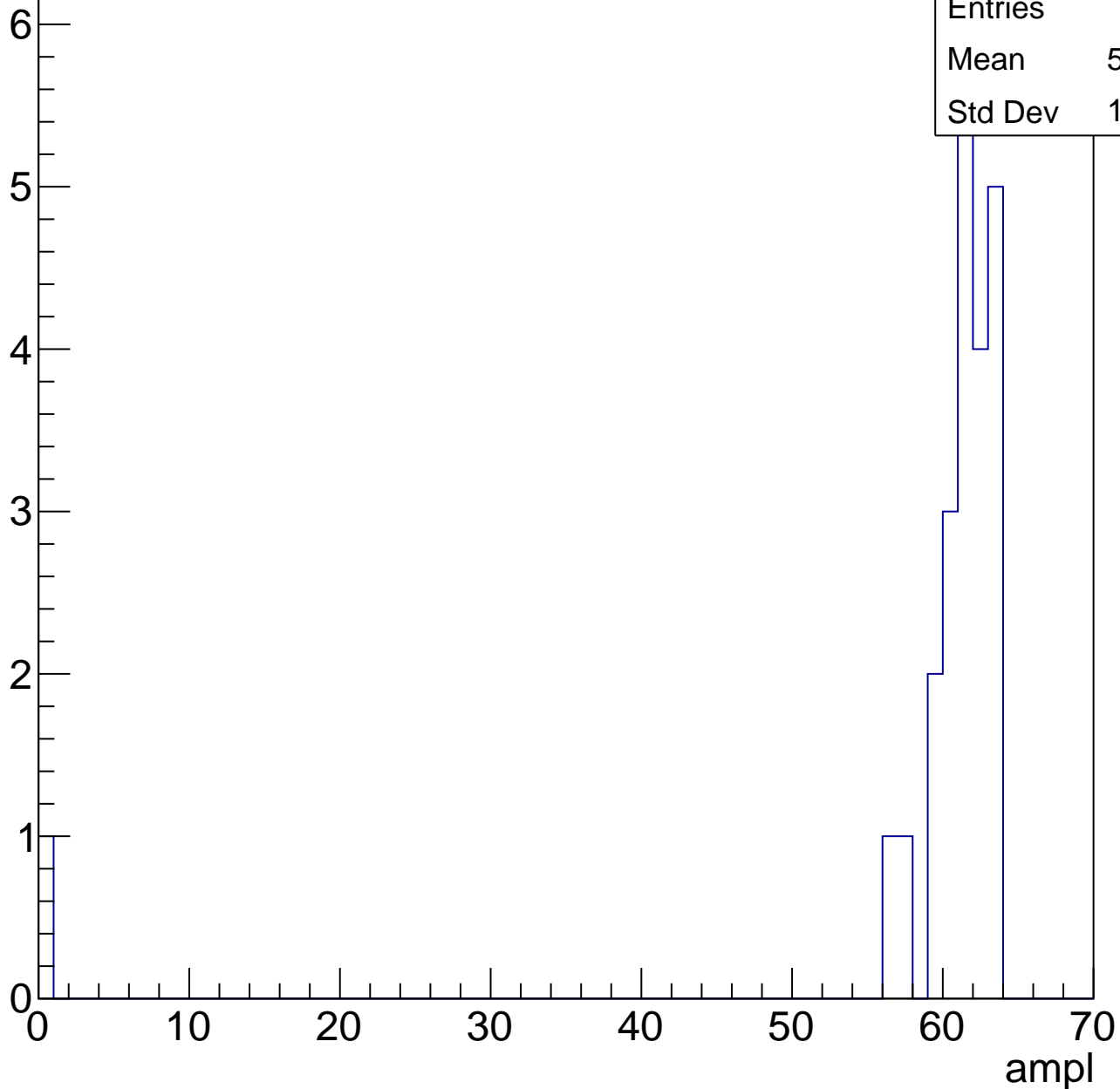


# B0L001S, U24-ch36, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	23
Mean	58.26
Std Dev	12.55



# B0L001S, U24-ch36, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch36, adc7

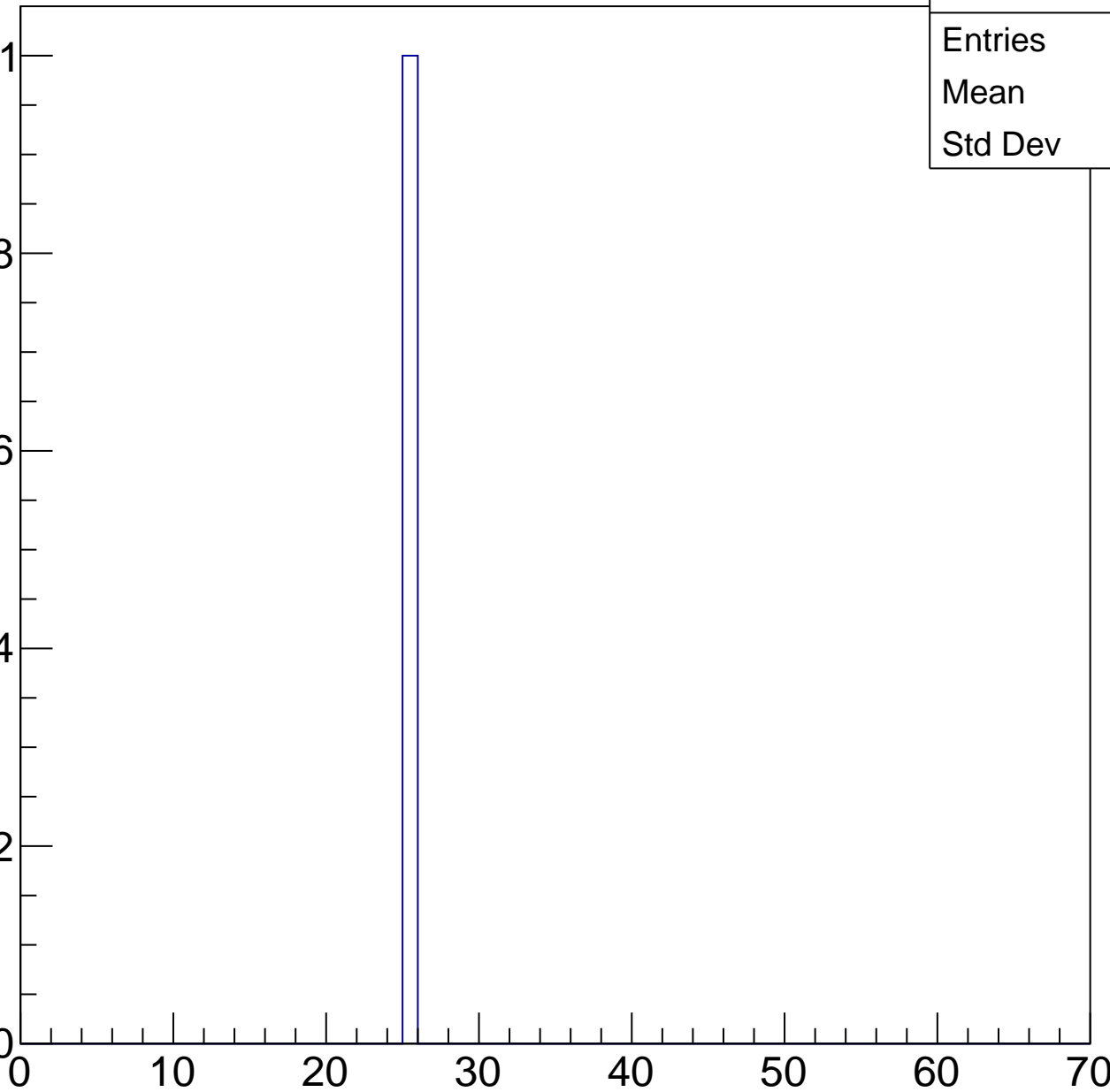
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	25
Std Dev	0

ampl



# B0L001S, U24-ch37, adc0

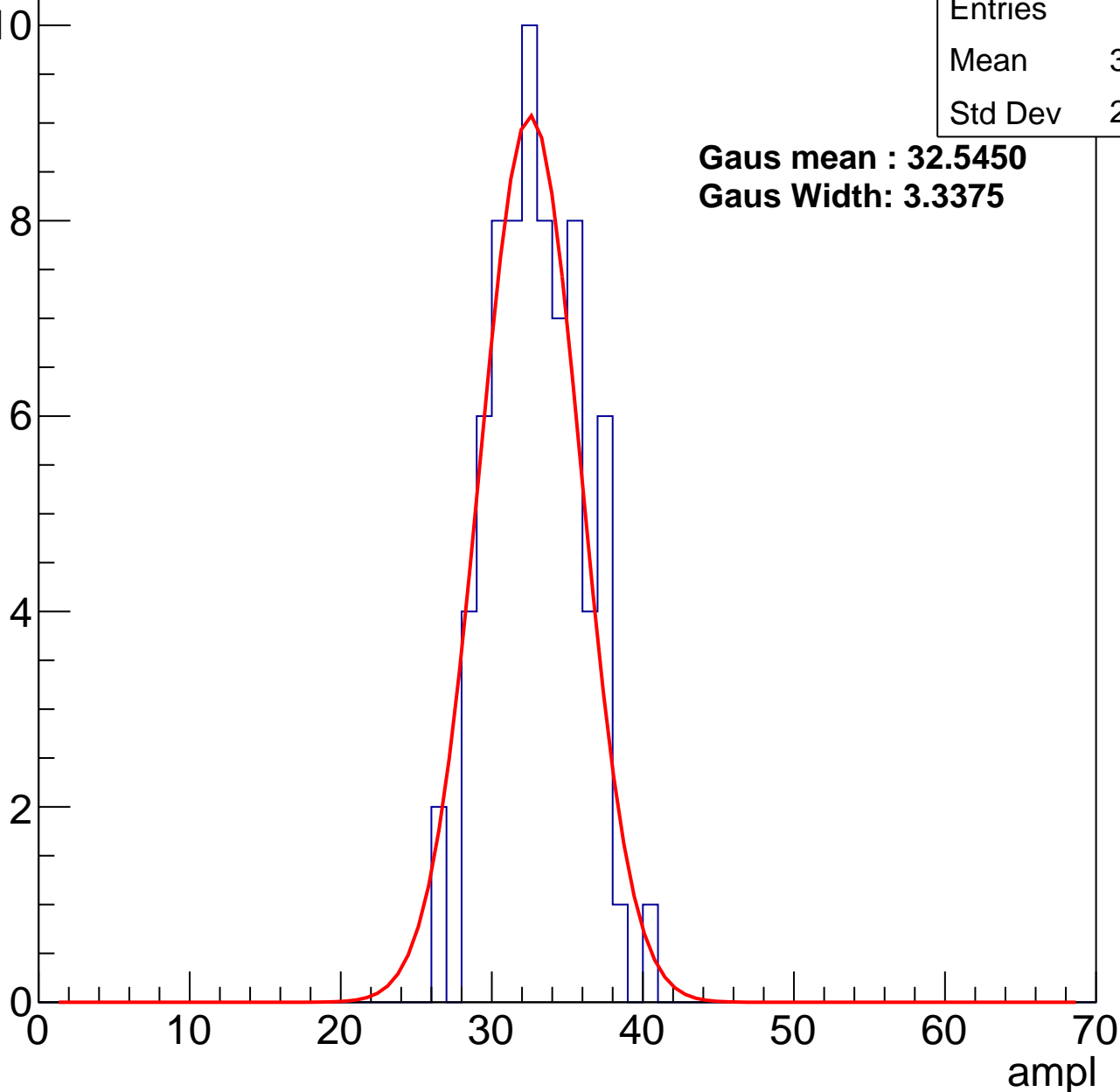
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	32.49
Std Dev	2.948

**Gaus mean : 32.5450**

**Gaus Width: 3.3375**



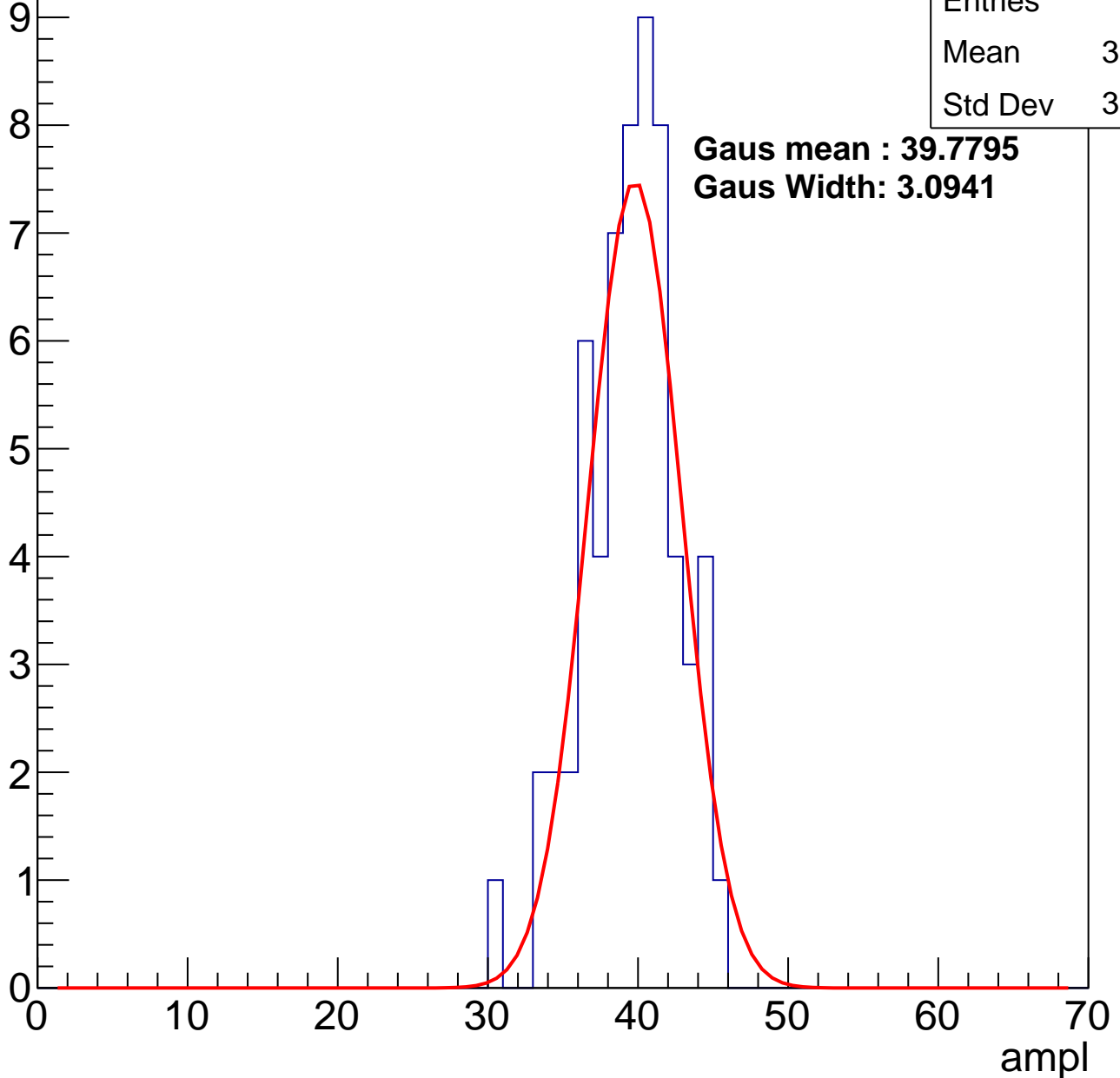
# B0L001S, U24-ch37, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	39.05
Std Dev	3.064

**Gaus mean : 39.7795**  
**Gaus Width: 3.0941**



# B0L001S, U24-ch37, adc2

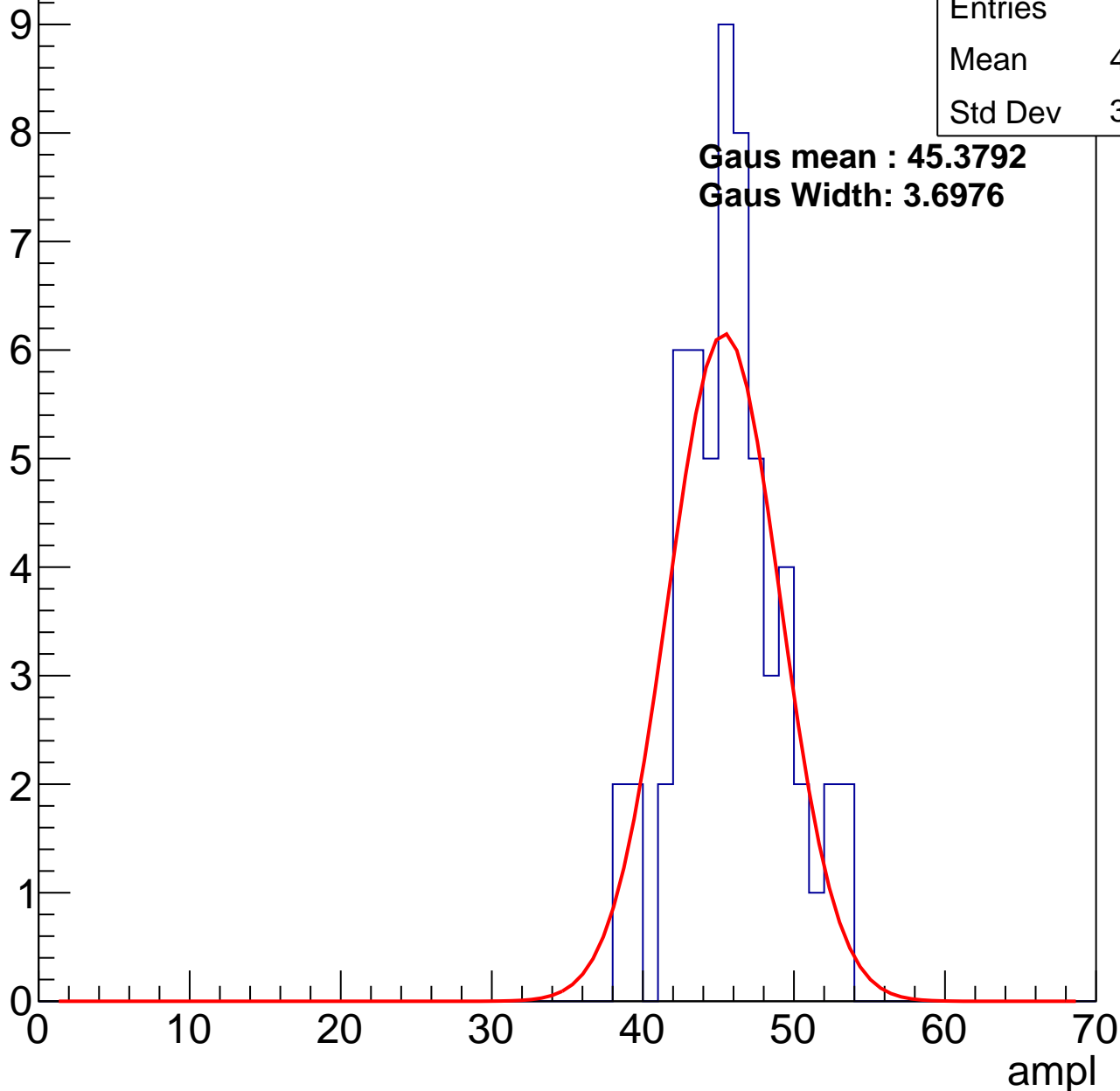
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	45.34
Std Dev	3.467

**Gaus mean : 45.3792**

**Gaus Width: 3.6976**

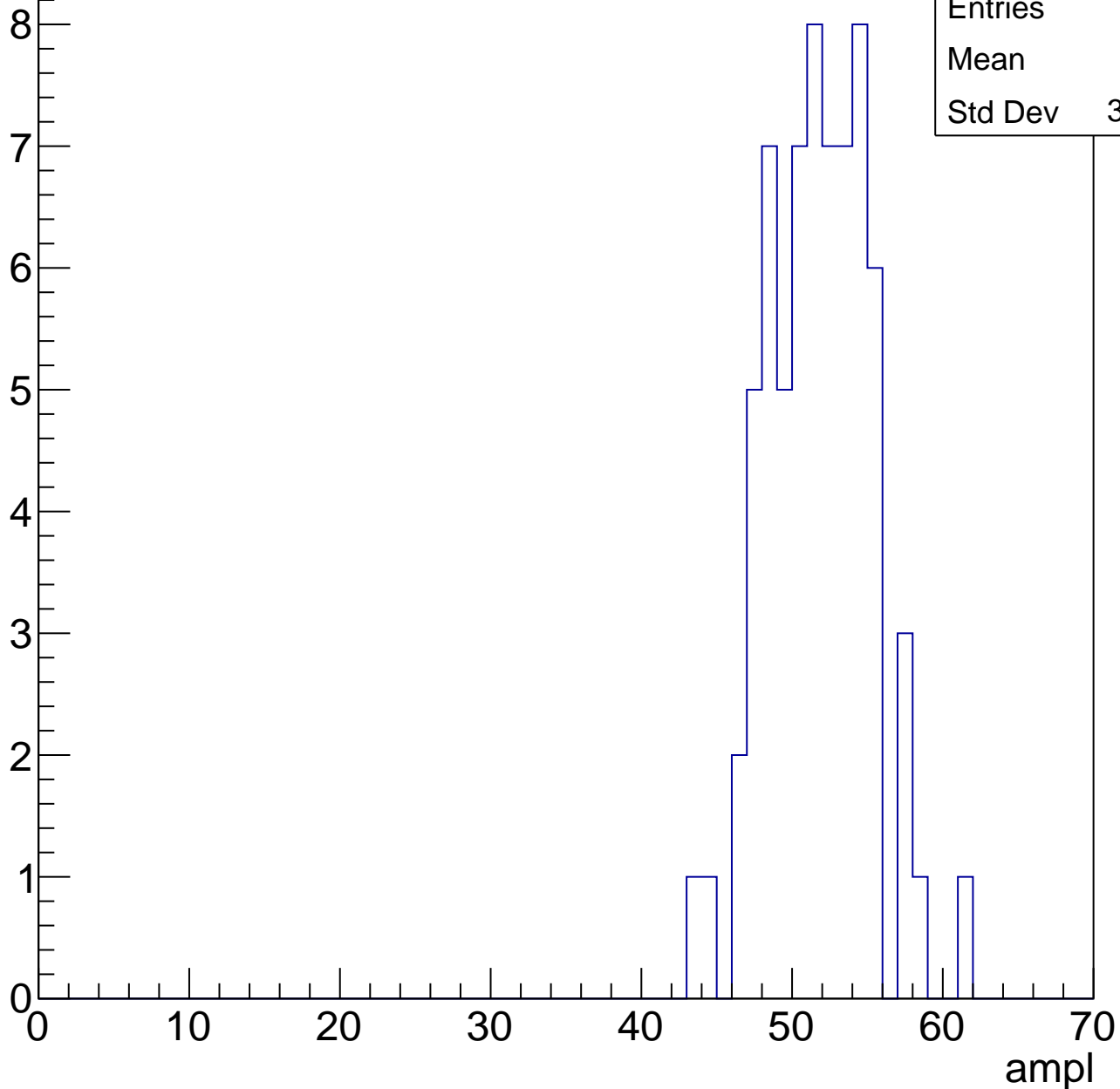


# B0L001S, U24-ch37, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	51.3
Std Dev	3.376



# B0L001S, U24-ch37, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

10

8

6

4

2

0

0

10

20

30

40

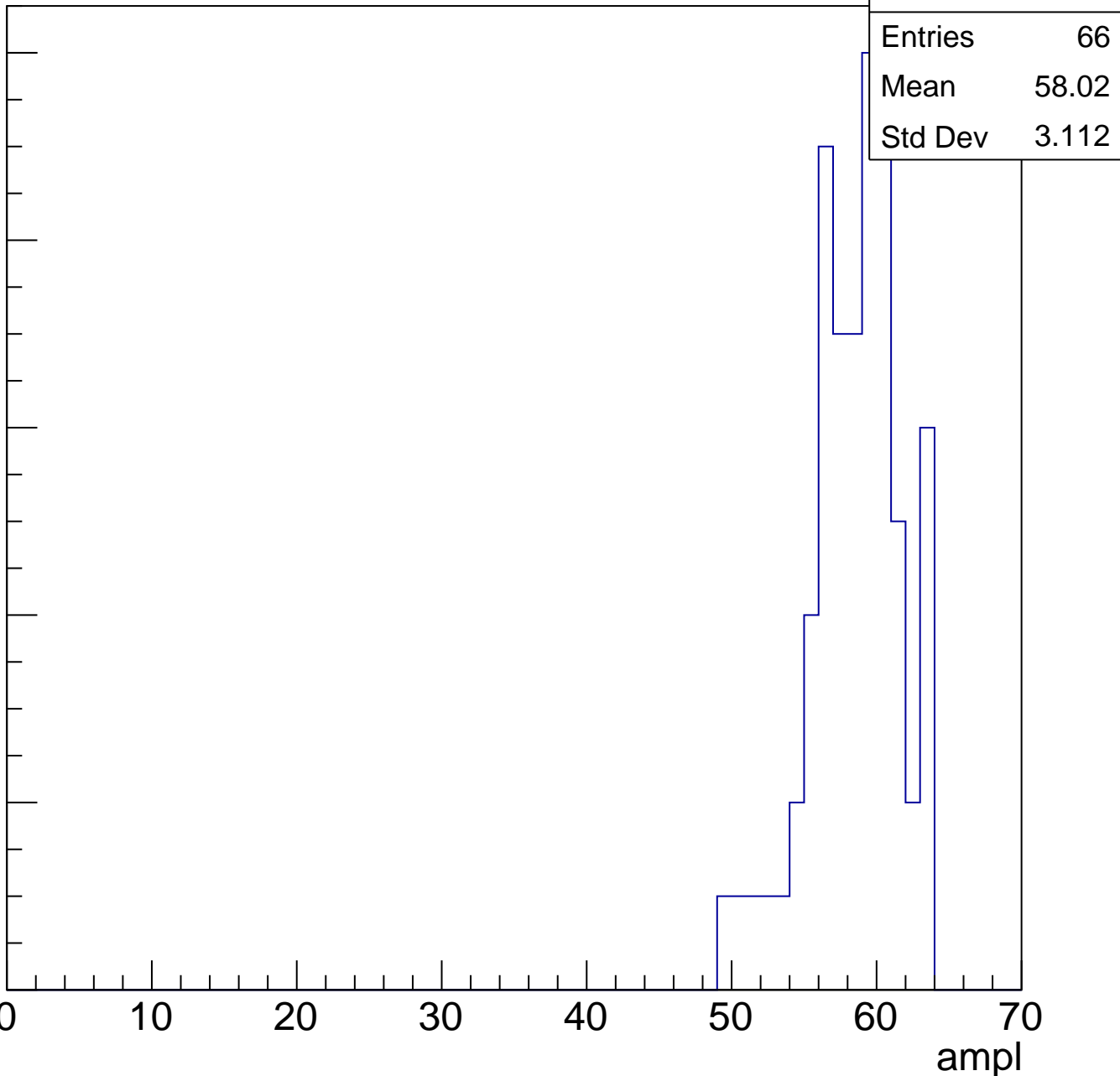
50

60

70

ampl

Entries	66
Mean	58.02
Std Dev	3.112

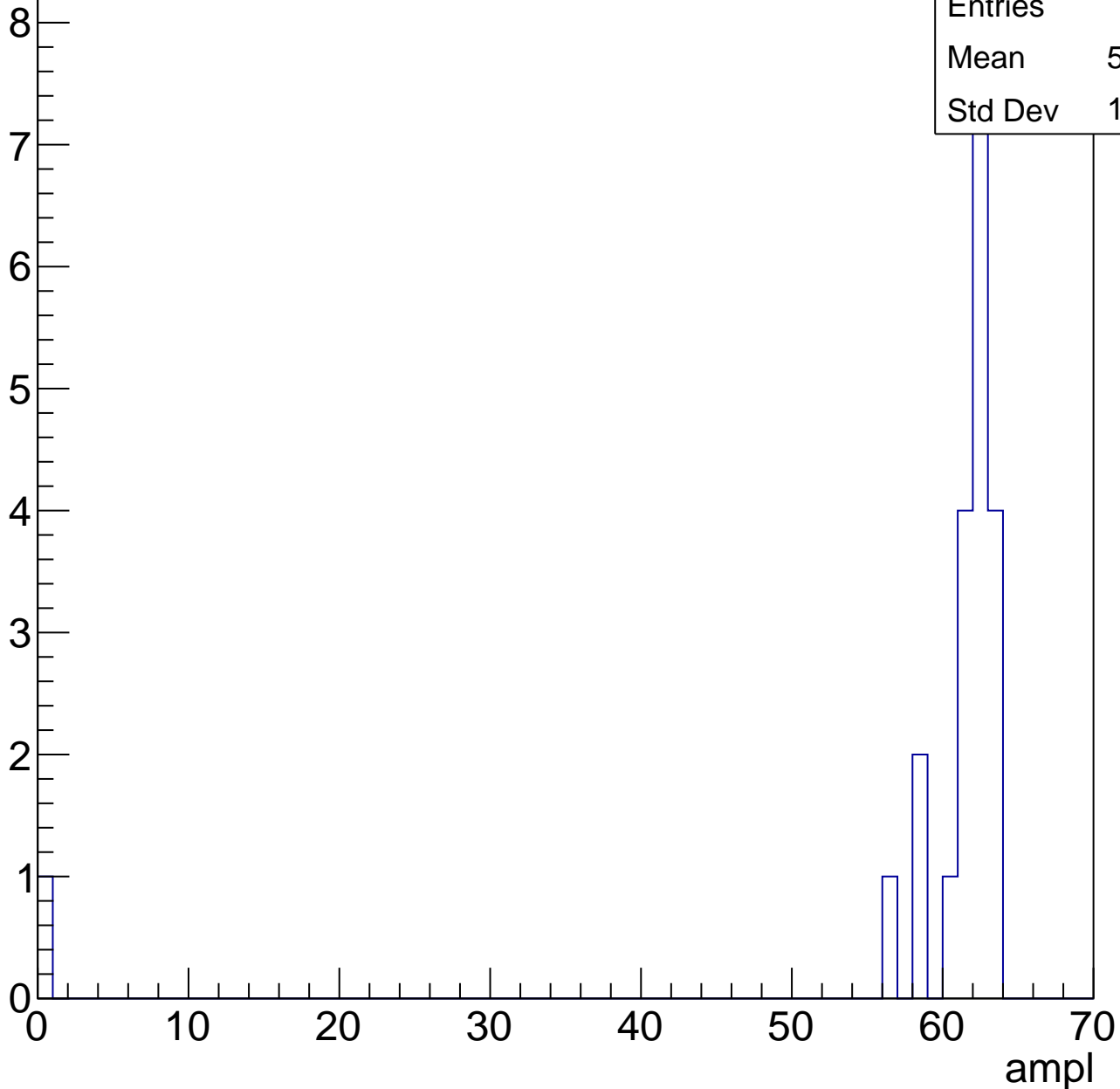


# B0L001S, U24-ch37, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	21
Mean	58.29
Std Dev	13.16



# B0L001S, U24-ch37, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U24-ch37, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U24-ch38, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	92
Mean	28.3
Std Dev	5.373

**Gaus mean : 29.4078**

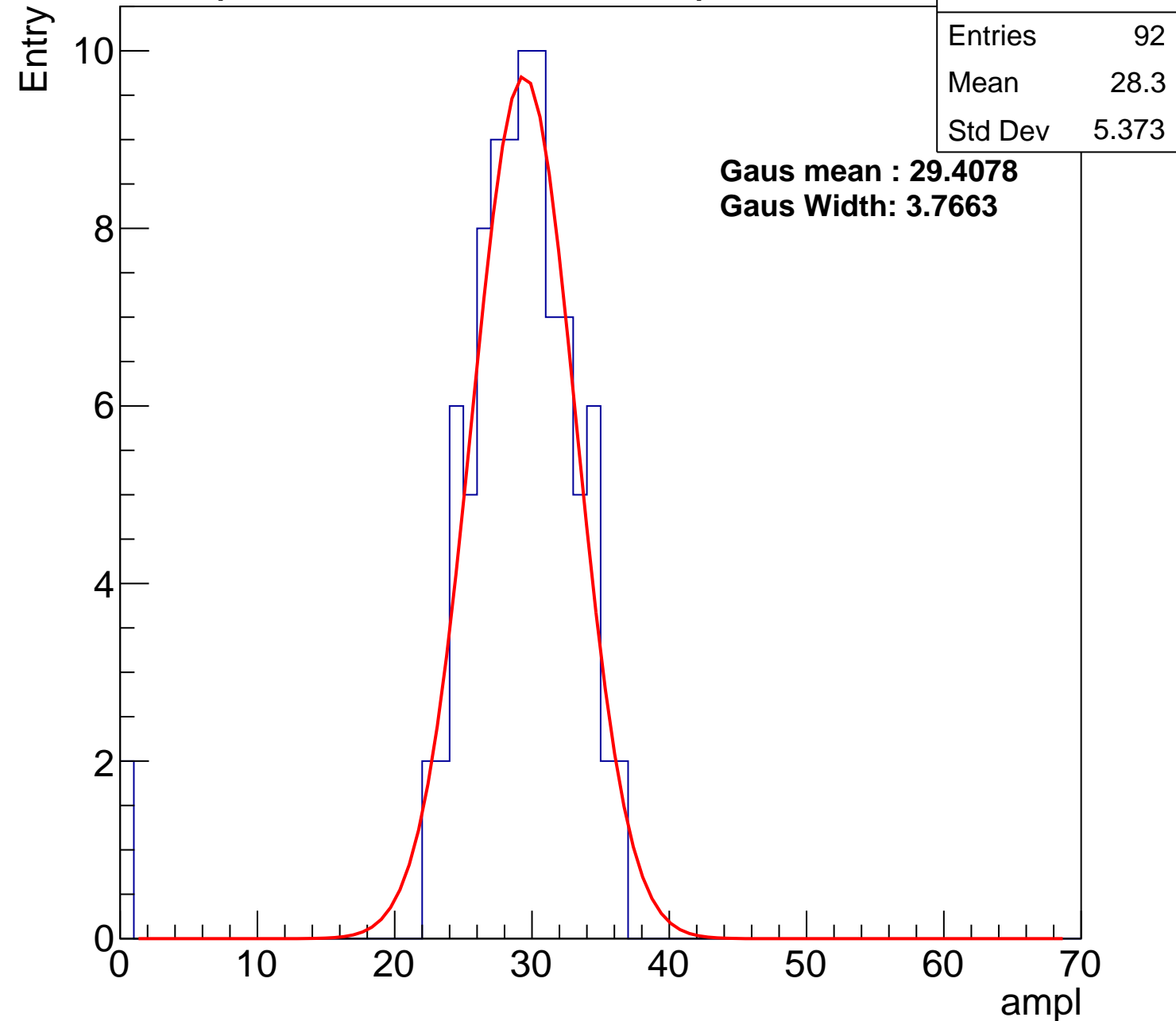
**Gaus Width: 3.7663**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U24-ch38, adc1

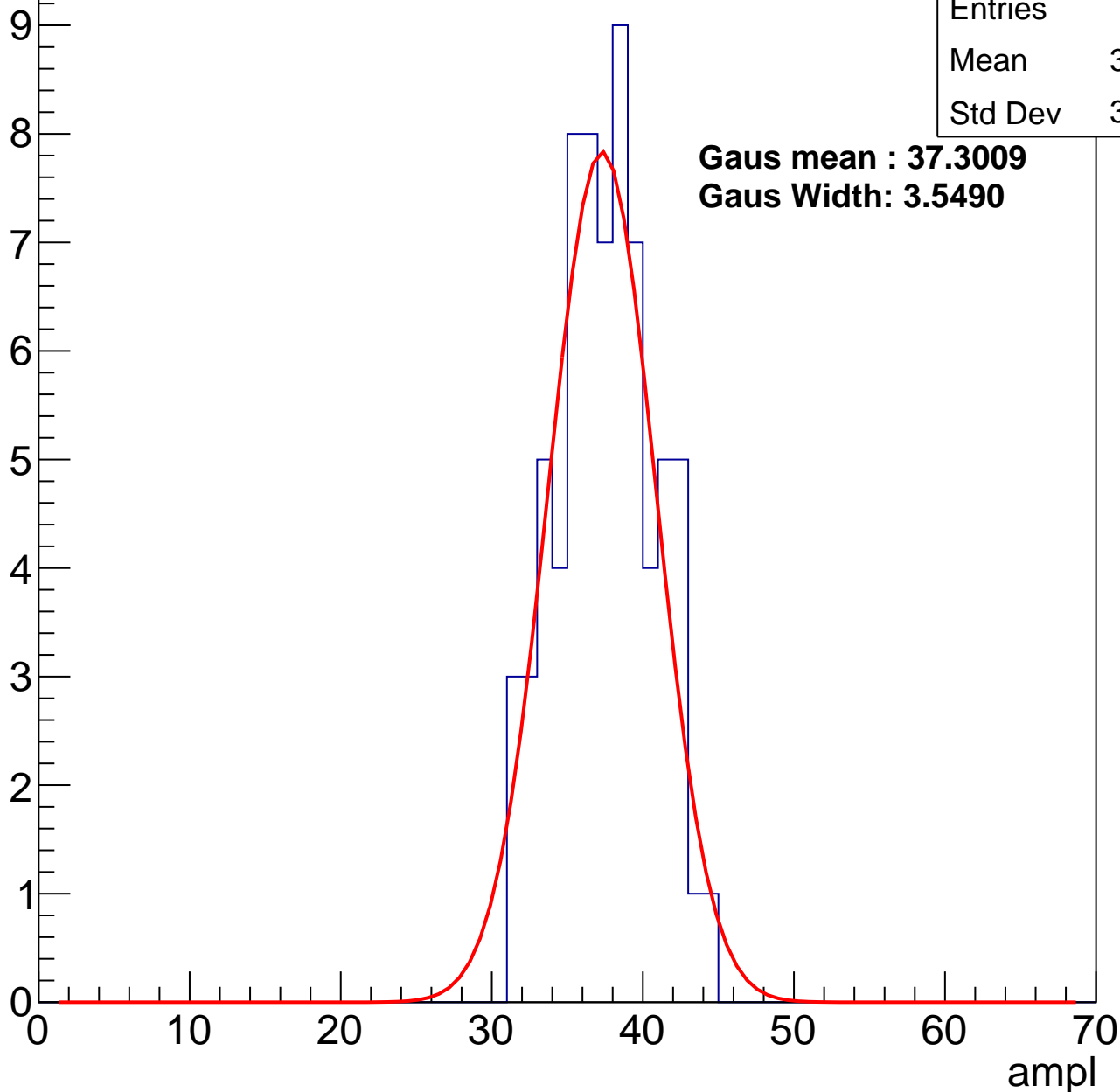
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	37.06
Std Dev	3.166

**Gaus mean : 37.3009**

**Gaus Width: 3.5490**



# B0L001S, U24-ch38, adc2

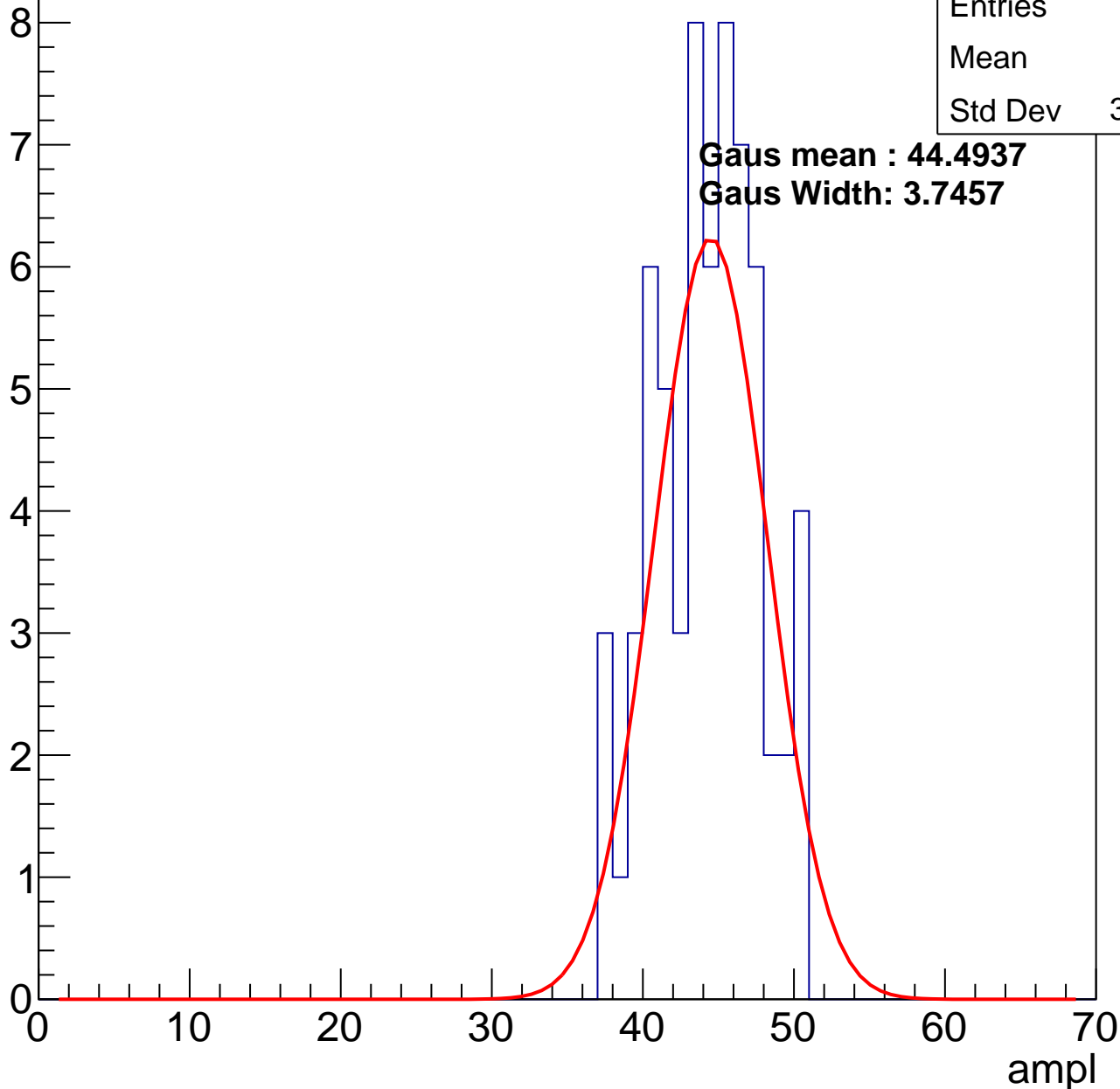
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	43.8
Std Dev	3.383

**Gaus mean : 44.4937**

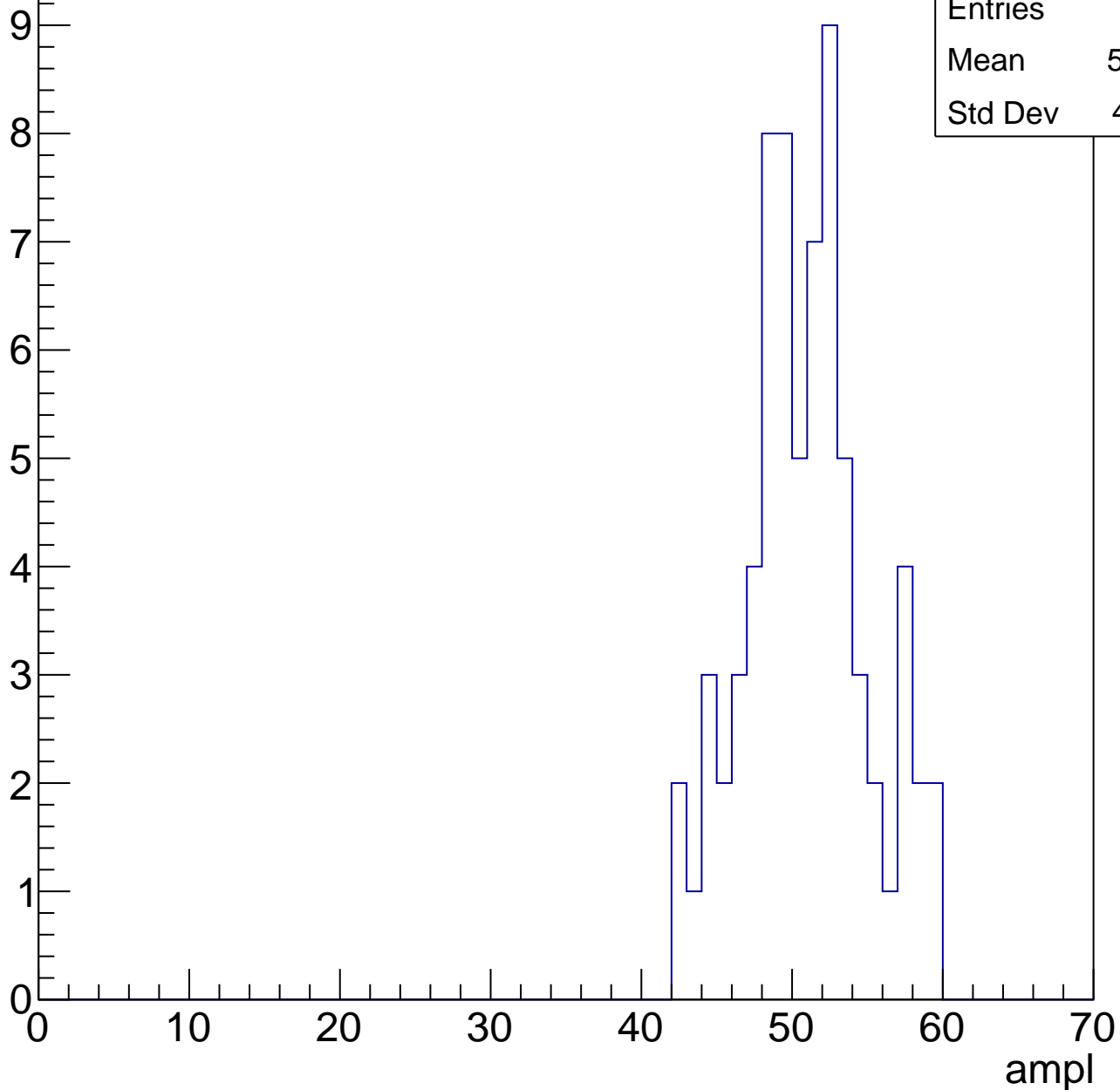
**Gaus Width: 3.7457**



# B0L001S, U24-ch38, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



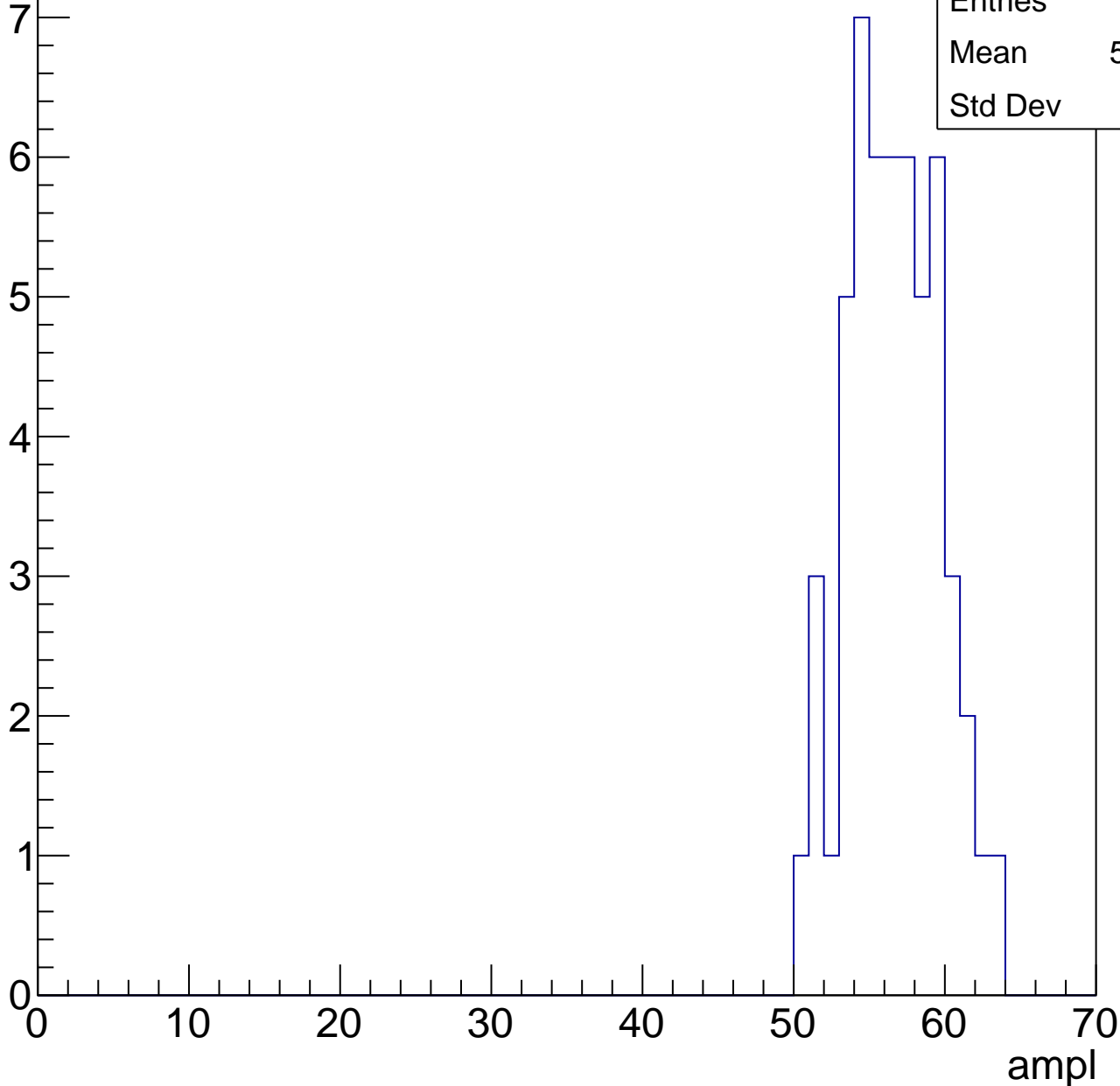
Entries	71
Mean	50.44
Std Dev	4.031

# B0L001S, U24-ch38, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

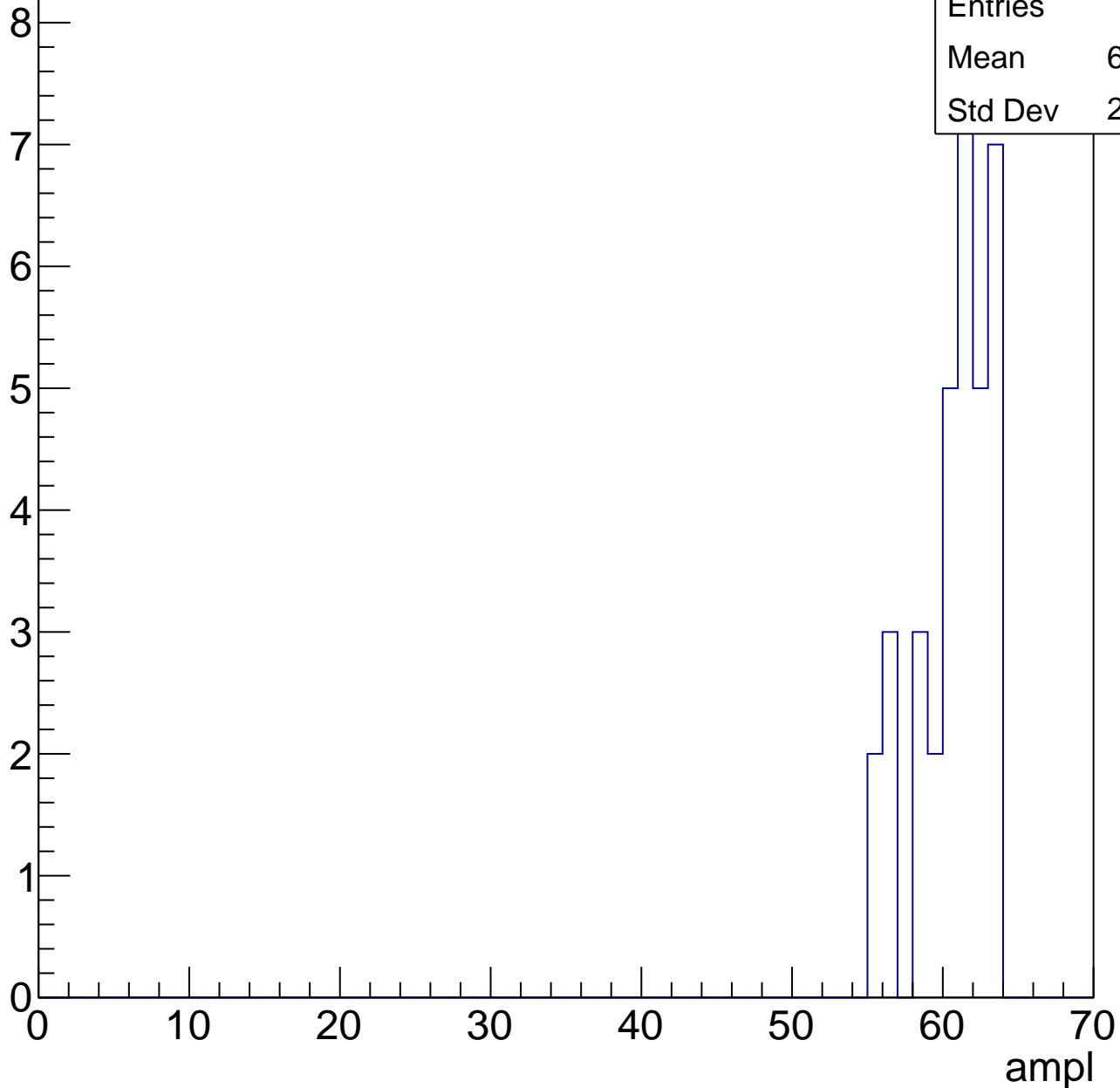
Entries	53
Mean	56.17
Std Dev	2.97



# B0L001S, U24-ch38, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

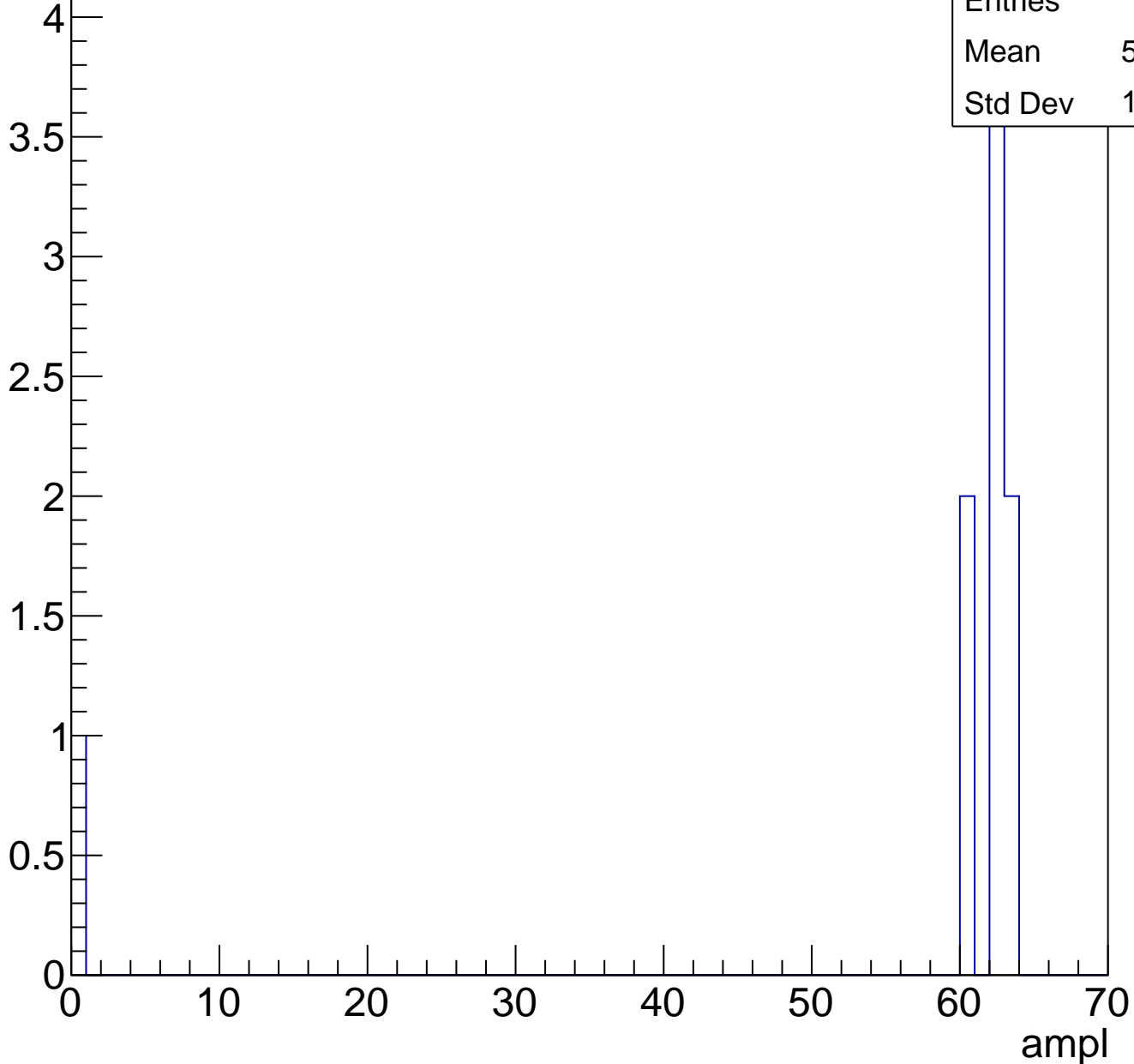
Entry



# B0L001S, U24-ch38, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

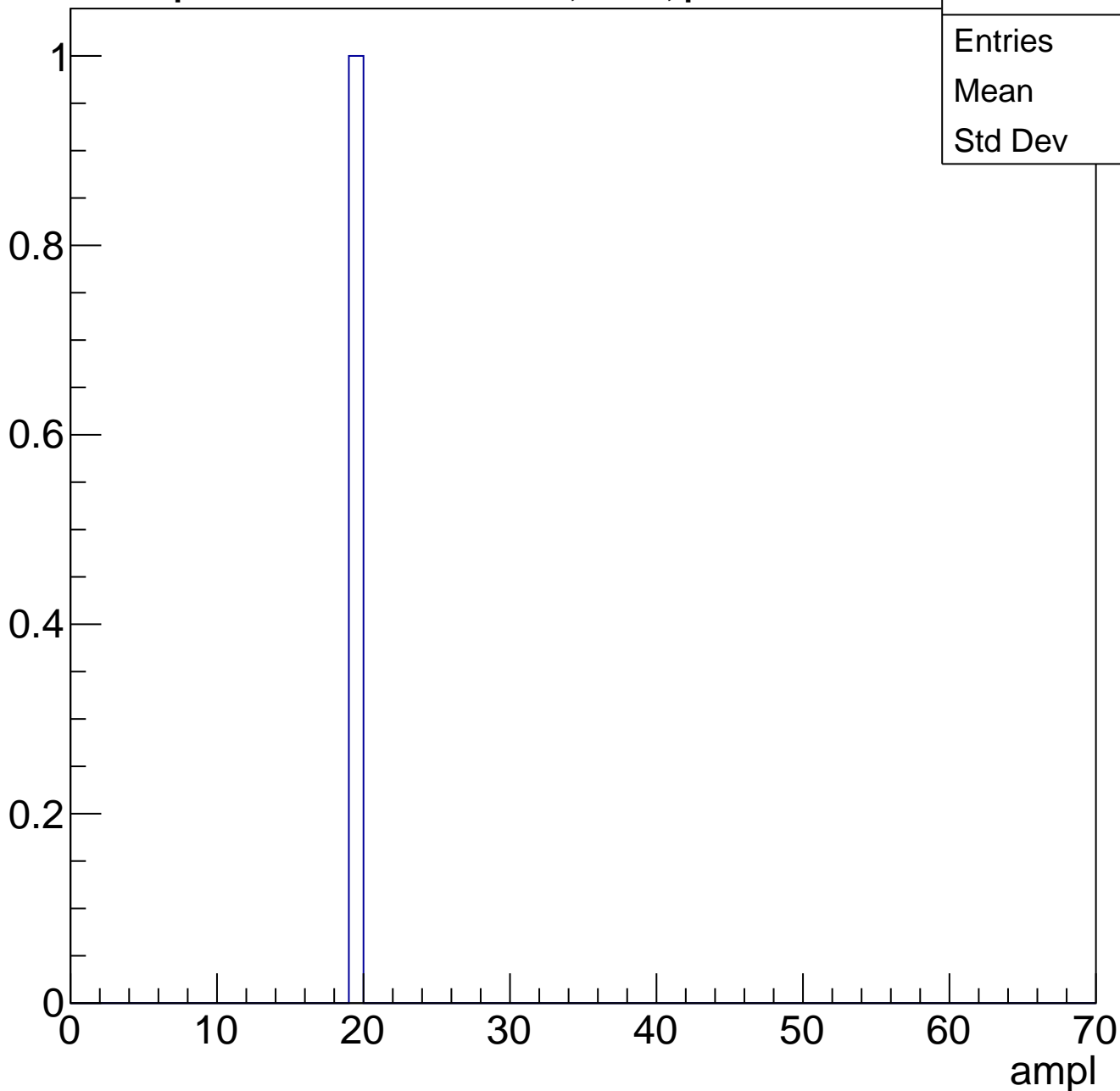




# B0L001S, U24-ch38, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U24-ch39, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	87
Mean	30.62
Std Dev	4.812

**Gaus mean : 31.7650**

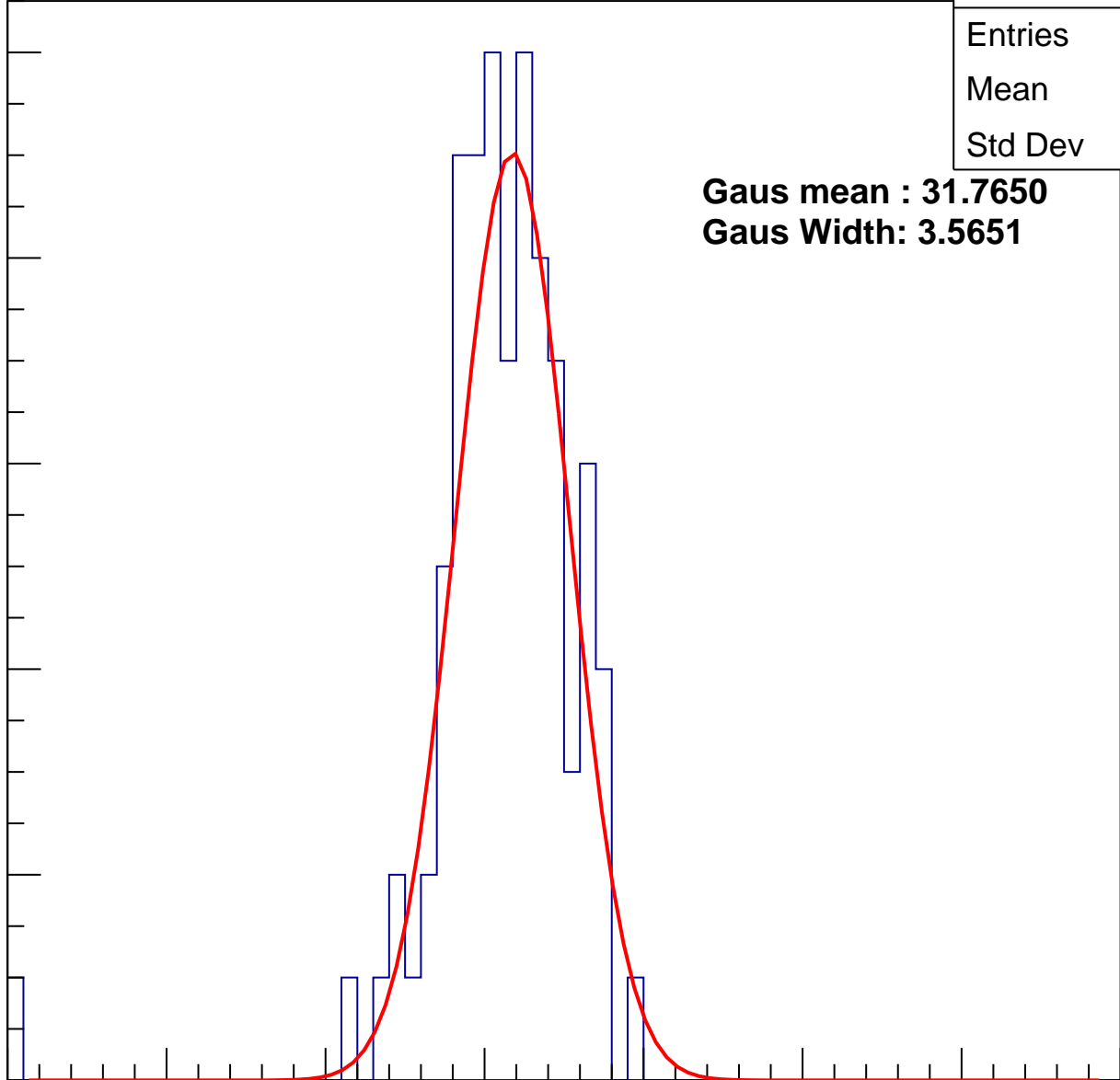
**Gaus Width: 3.5651**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U24-ch39, adc1

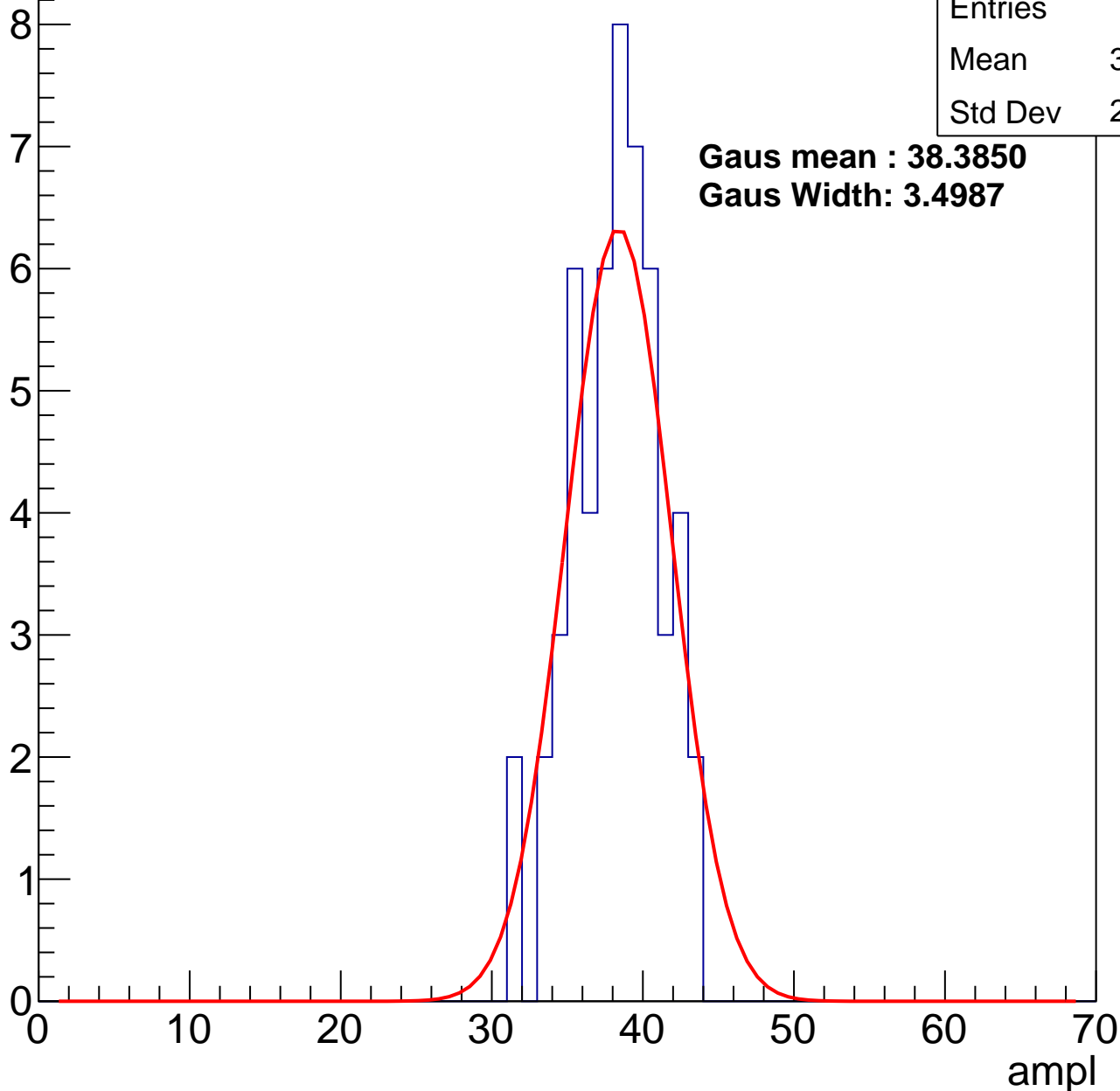
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	37.74
Std Dev	2.882

**Gaus mean : 38.3850**

**Gaus Width: 3.4987**



# B0L001S, U24-ch39, adc2

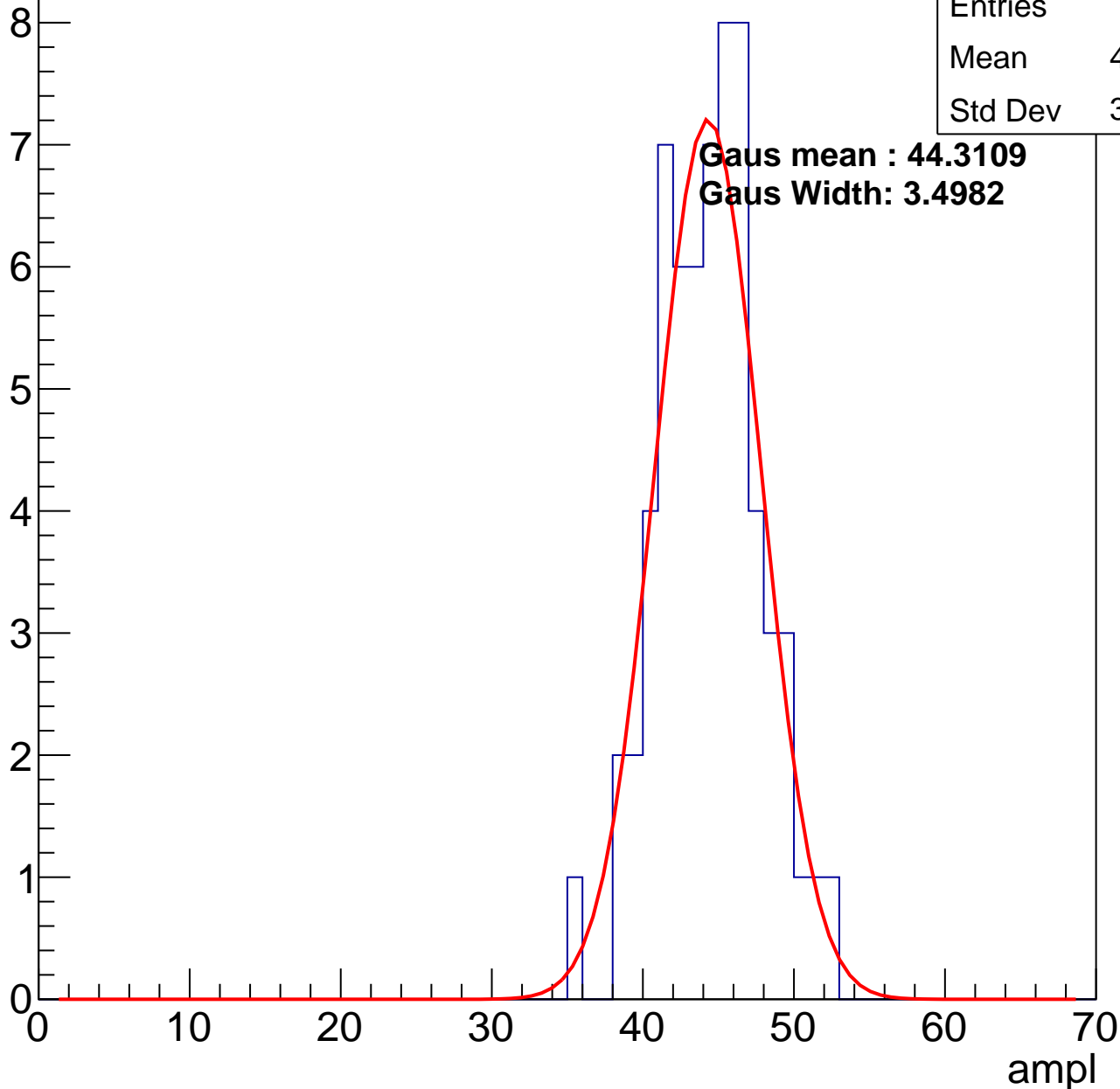
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	43.97
Std Dev	3.326

**Gaus mean : 44.3109**

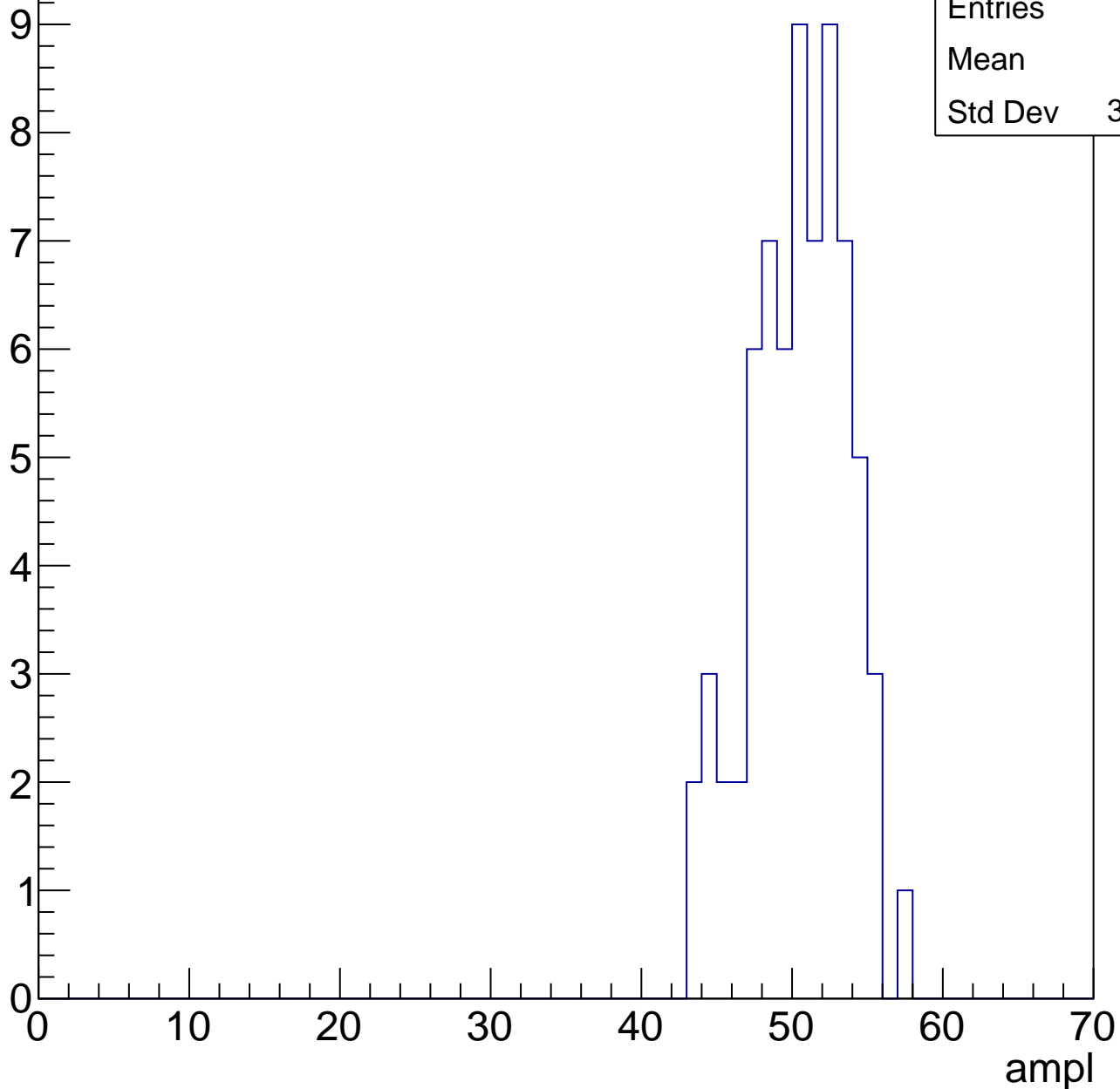
**Gaus Width: 3.4982**



# B0L001S, U24-ch39, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



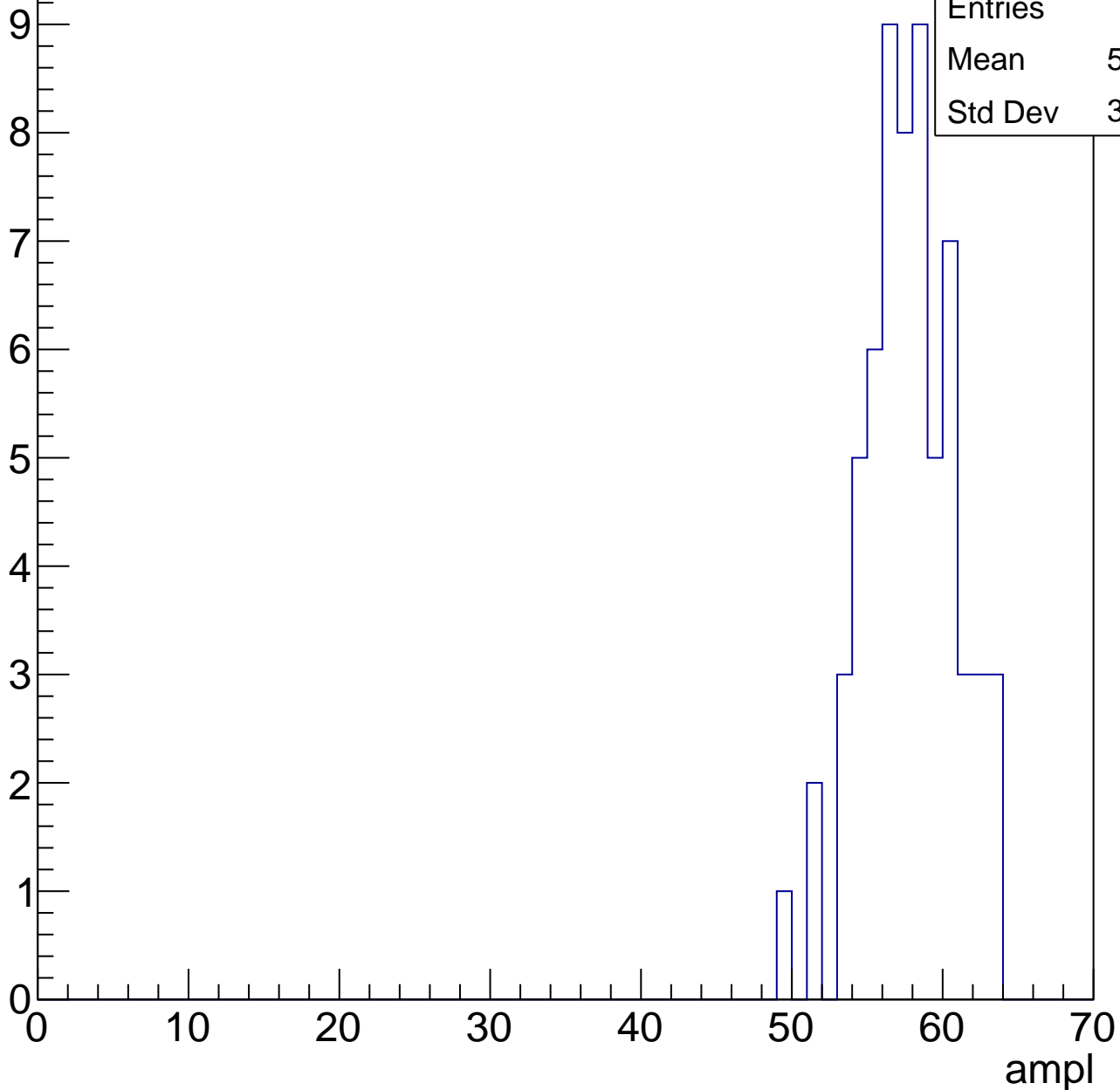
Entries	69
Mean	50
Std Dev	3.153

# B0L001S, U24-ch39, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	57.27
Std Dev	3.012

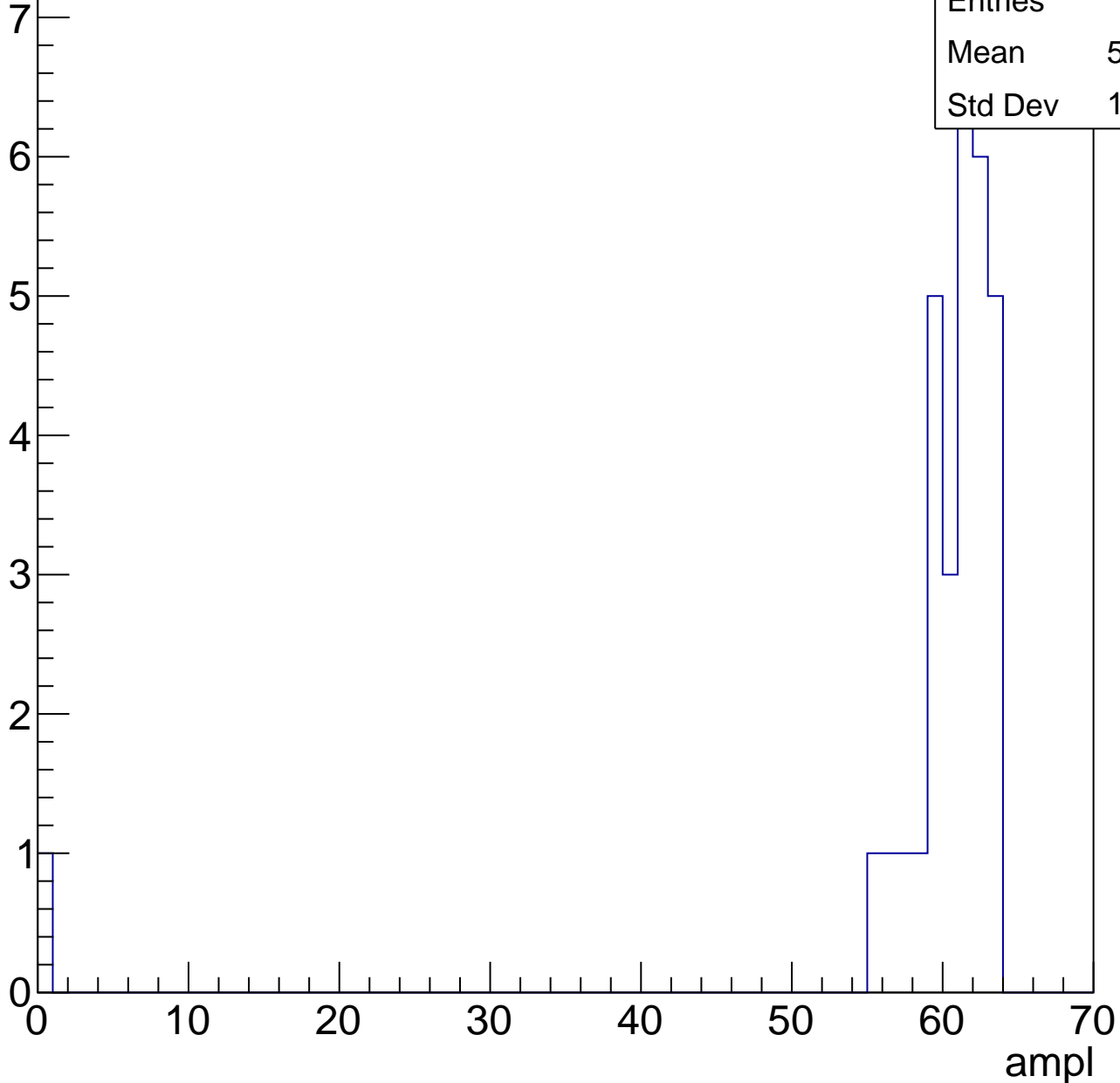


# B0L001S, U24-ch39, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	31
Mean	58.55
Std Dev	10.88



# B0L001S, U24-ch39, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.67
Std Dev	0.4714

ampl

0 10 20 30 40 50 60 70



# B0L001S, U24-ch39, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U24-ch40, adc0

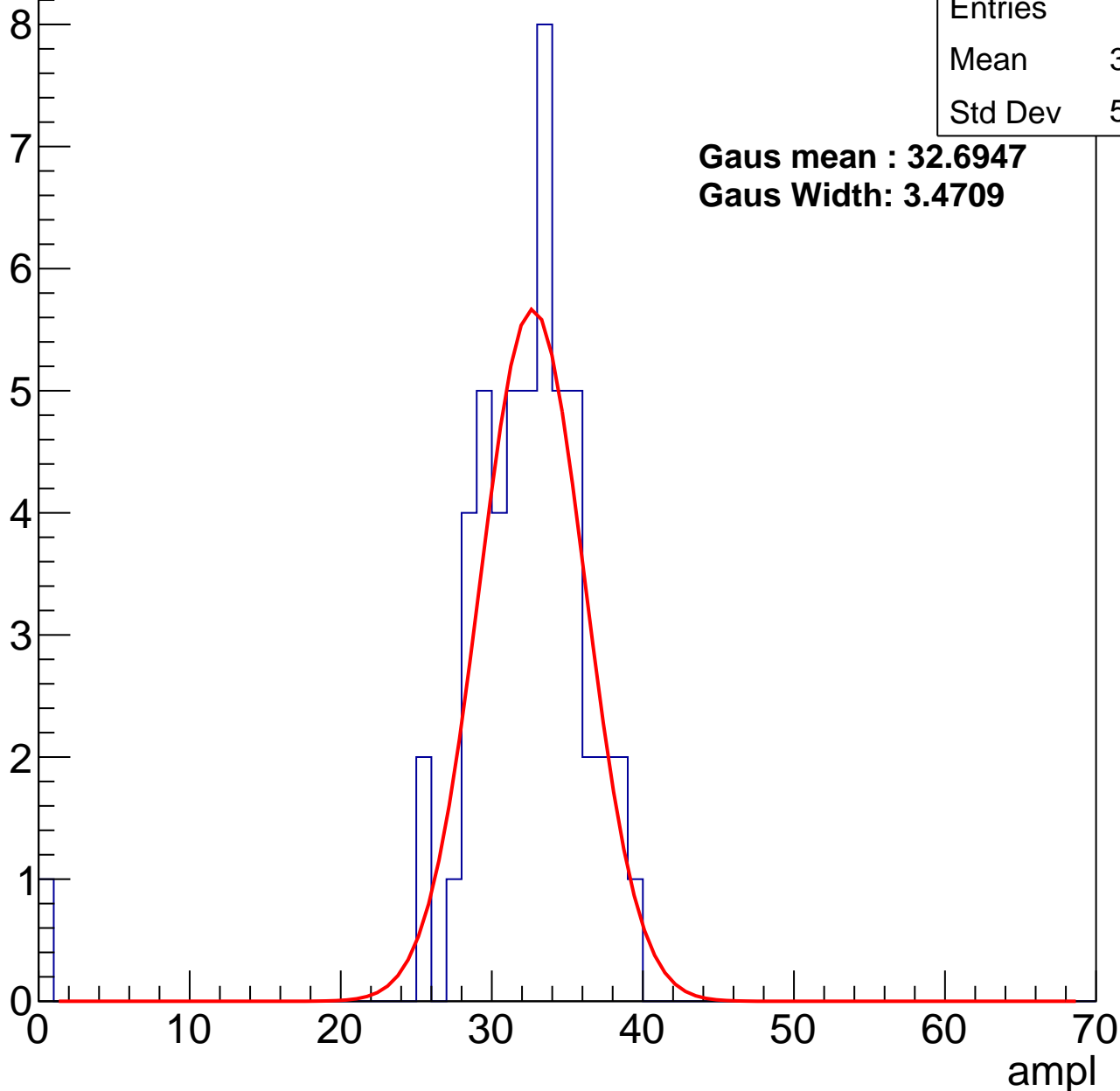
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	31.52
Std Dev	5.444

**Gaus mean : 32.6947**

**Gaus Width: 3.4709**



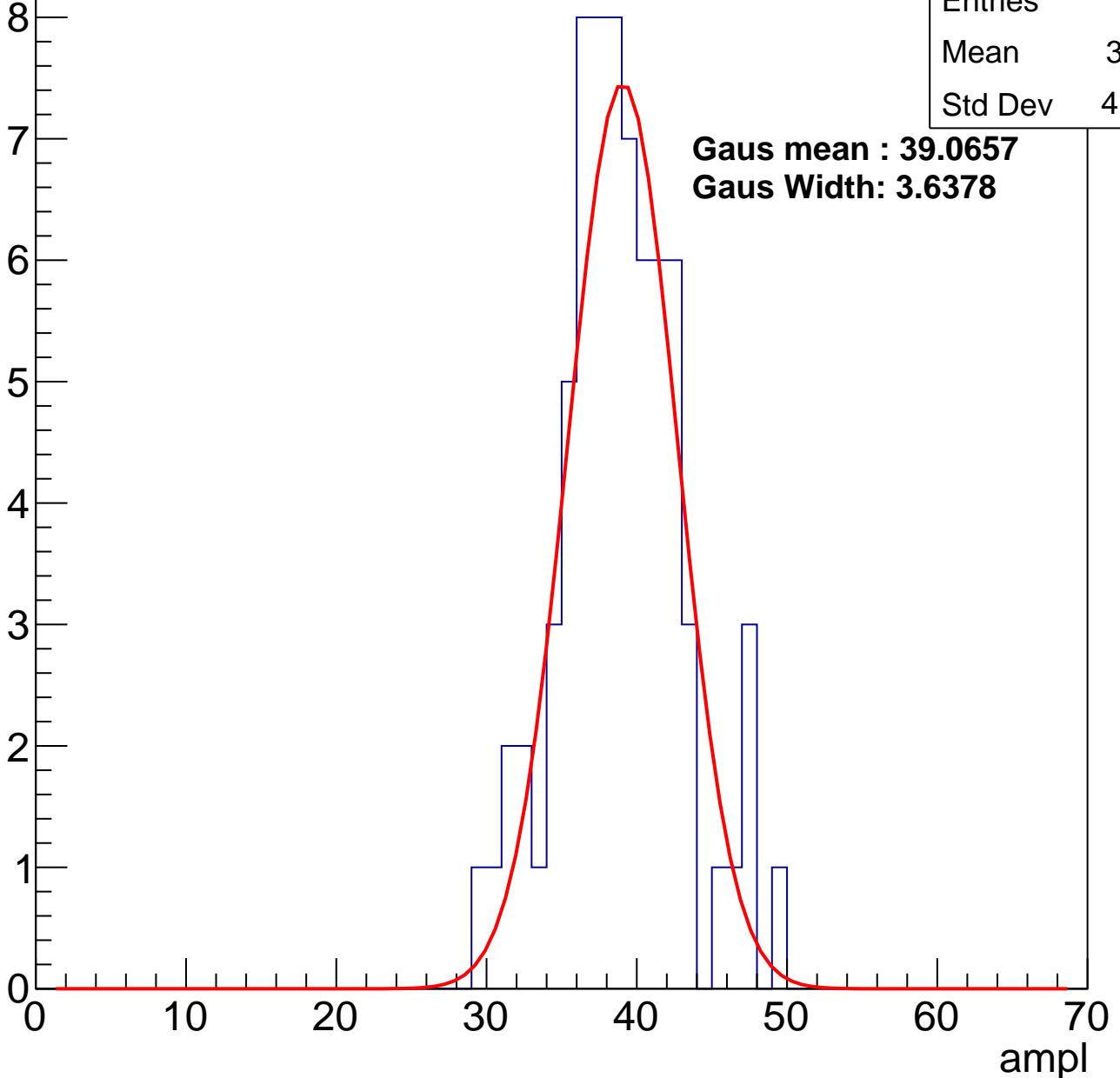
# B0L001S, U24-ch40, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	38.41
Std Dev	4.044

**Gaus mean : 39.0657**  
**Gaus Width: 3.6378**



# B0L001S, U24-ch40, adc2

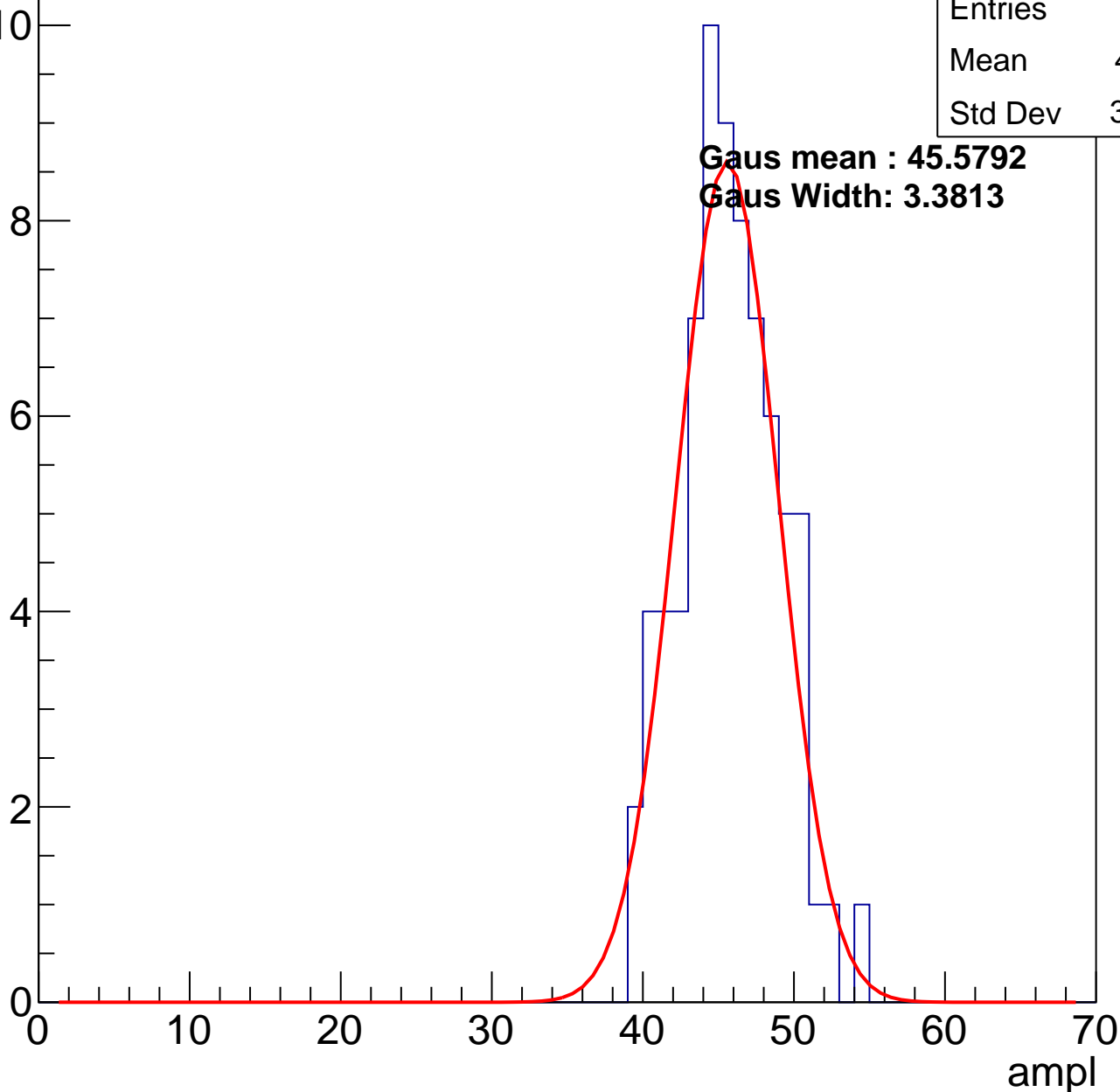
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	45.31
Std Dev	3.213

**Gaus mean : 45.5792**

**Gaus Width: 3.3813**

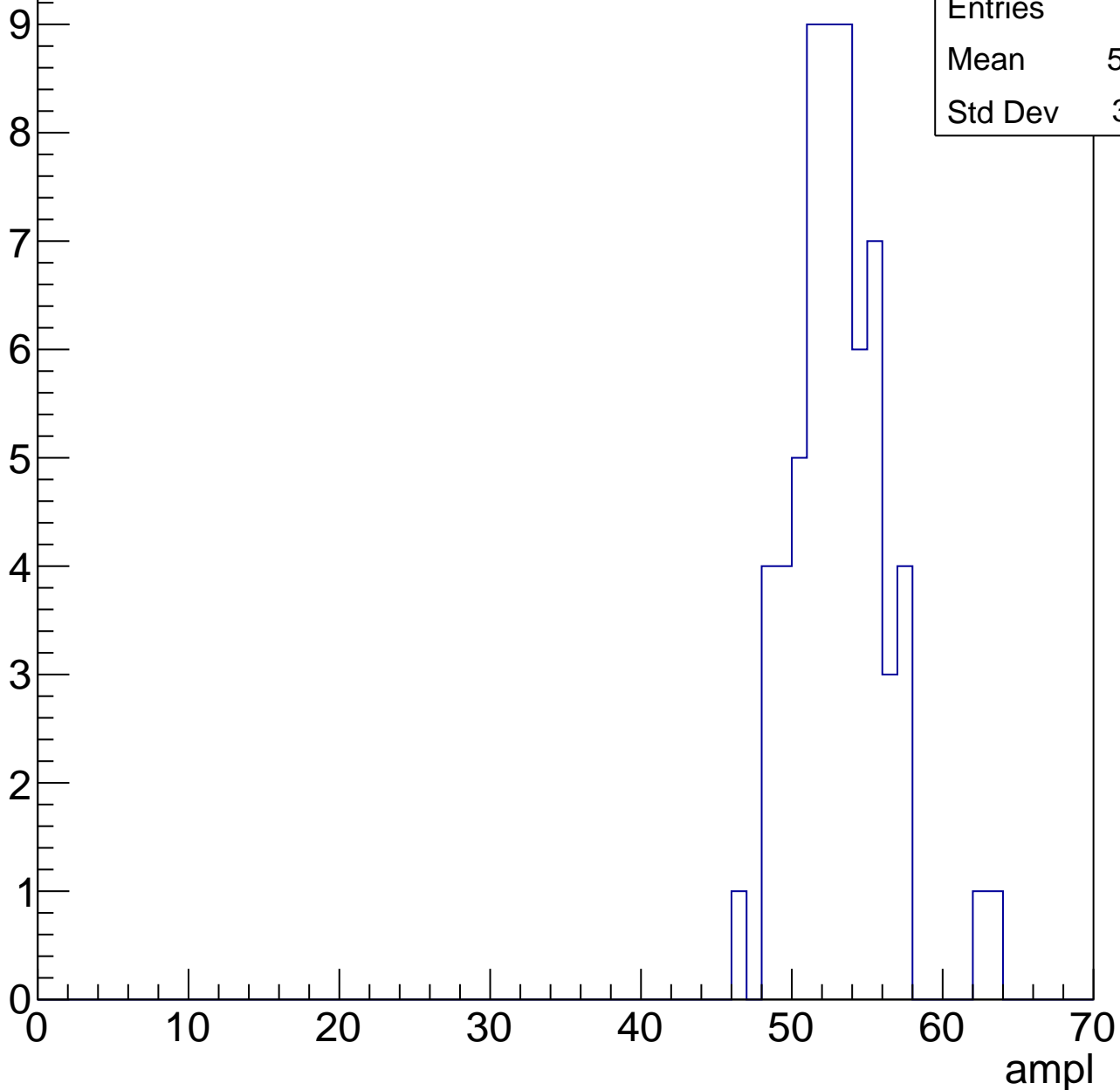


# B0L001S, U24-ch40, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	52.67
Std Dev	3.091



# B0L001S, U24-ch40, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

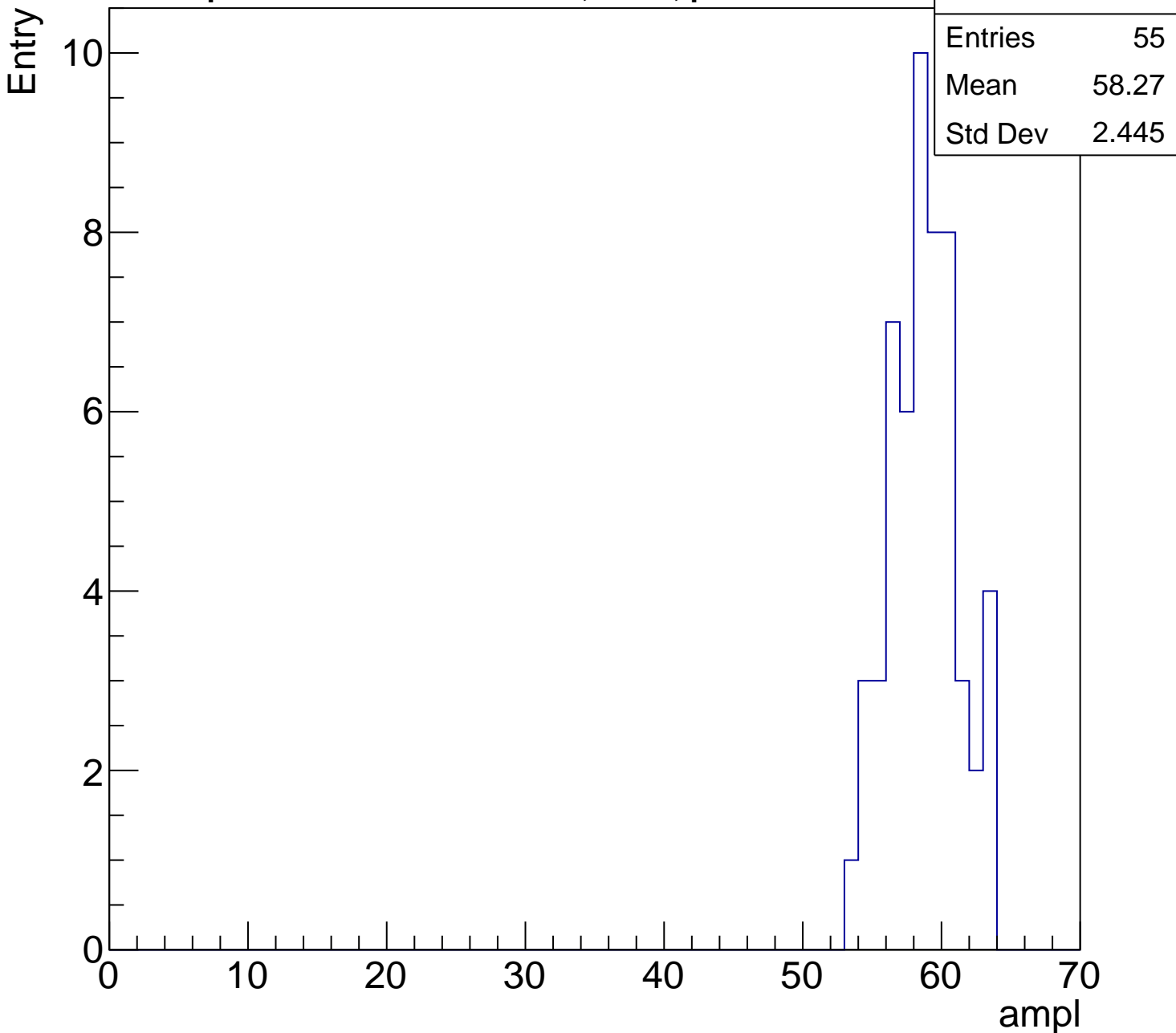
Entries	55
Mean	58.27
Std Dev	2.445

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

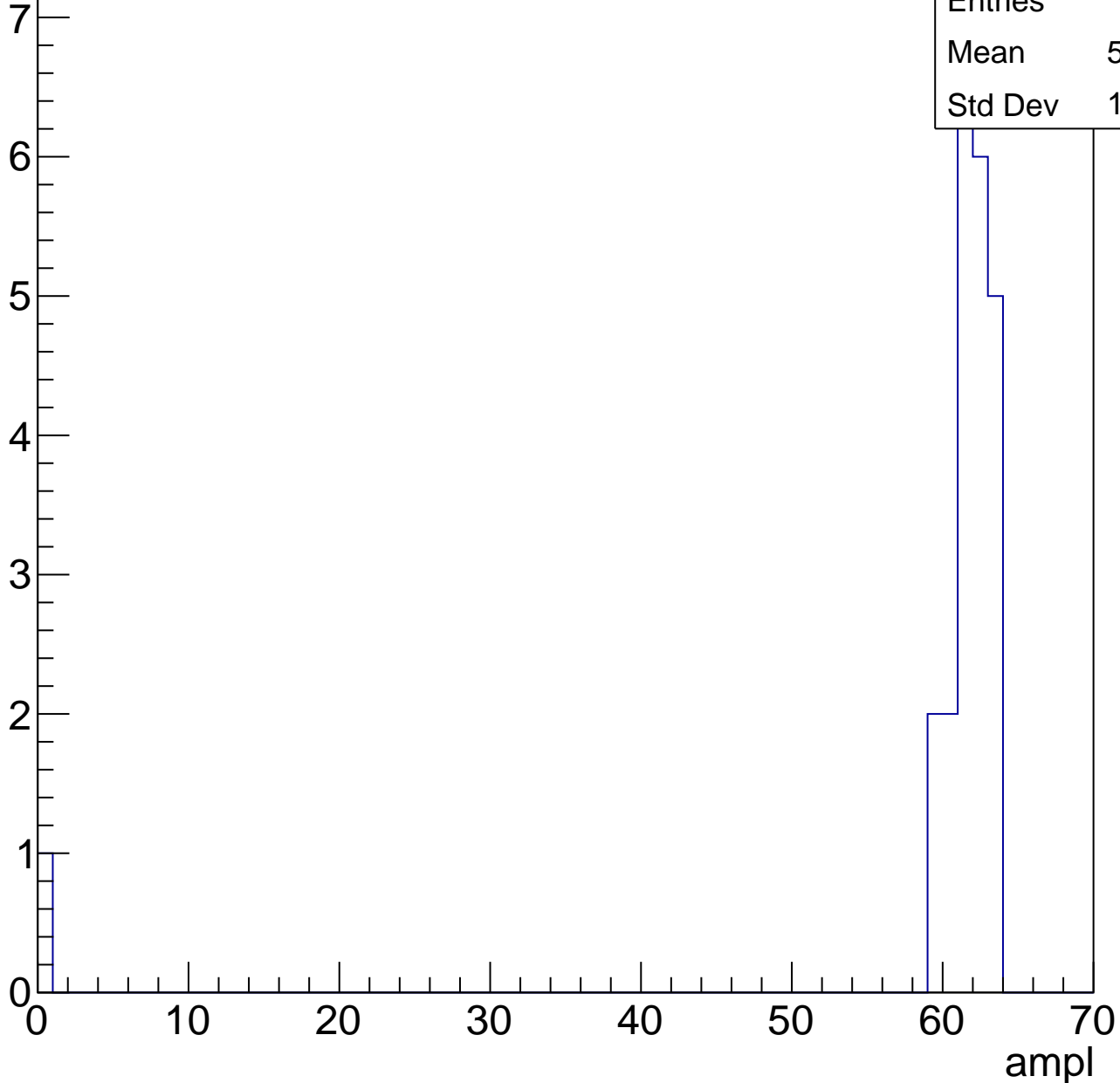


# B0L001S, U24-ch40, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	23
Mean	58.78
Std Dev	12.59



# B0L001S, U24-ch40, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	62
Std Dev	0

ampl



# B0L001S, U24-ch40, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U24-ch41, adc0

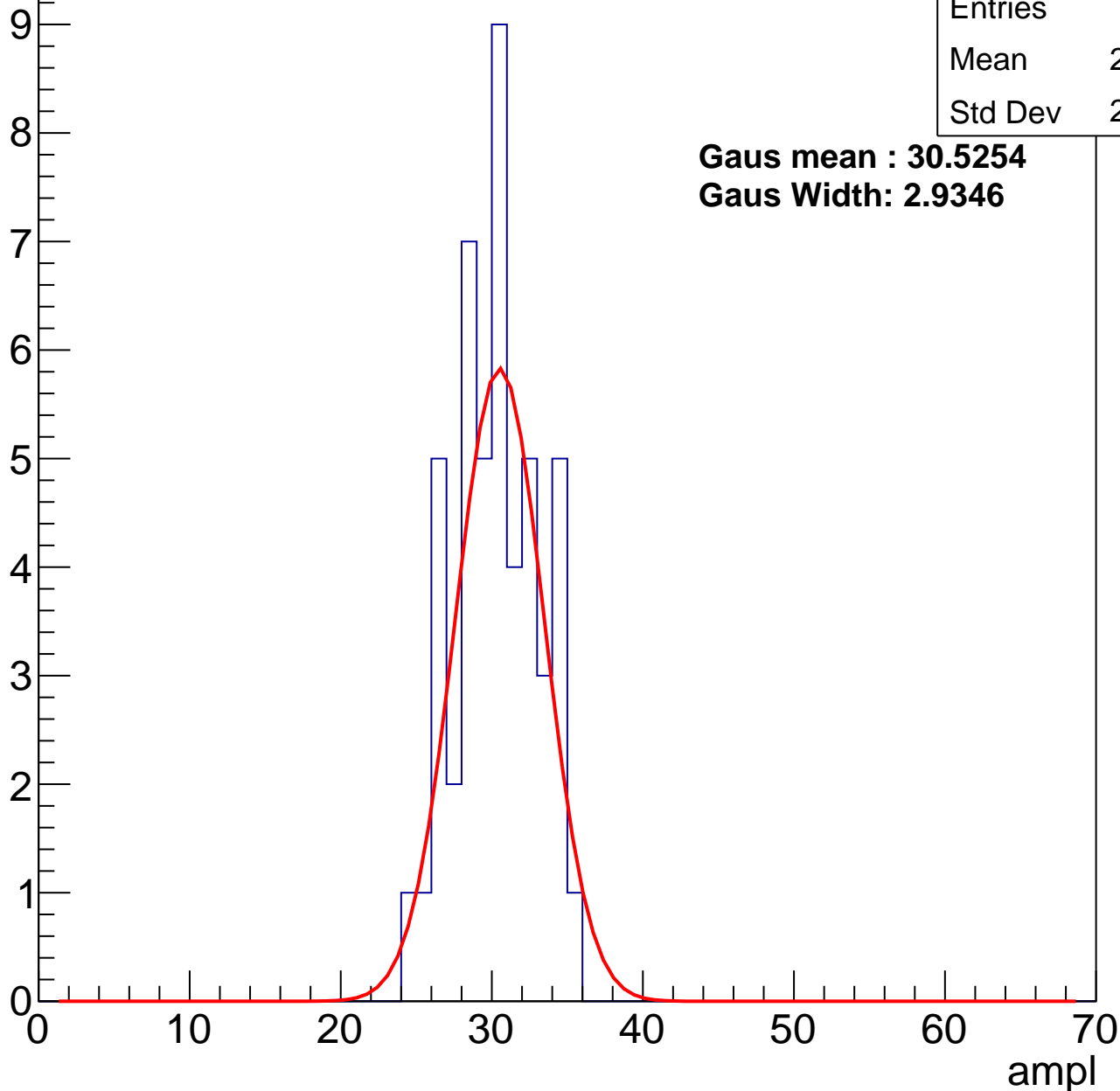
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	48
Mean	29.83
Std Dev	2.687

**Gaus mean : 30.5254**

**Gaus Width: 2.9346**



# B0L001S, U24-ch41, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	75
Mean	36.17
Std Dev	3.553

**Gaus mean : 36.1508**

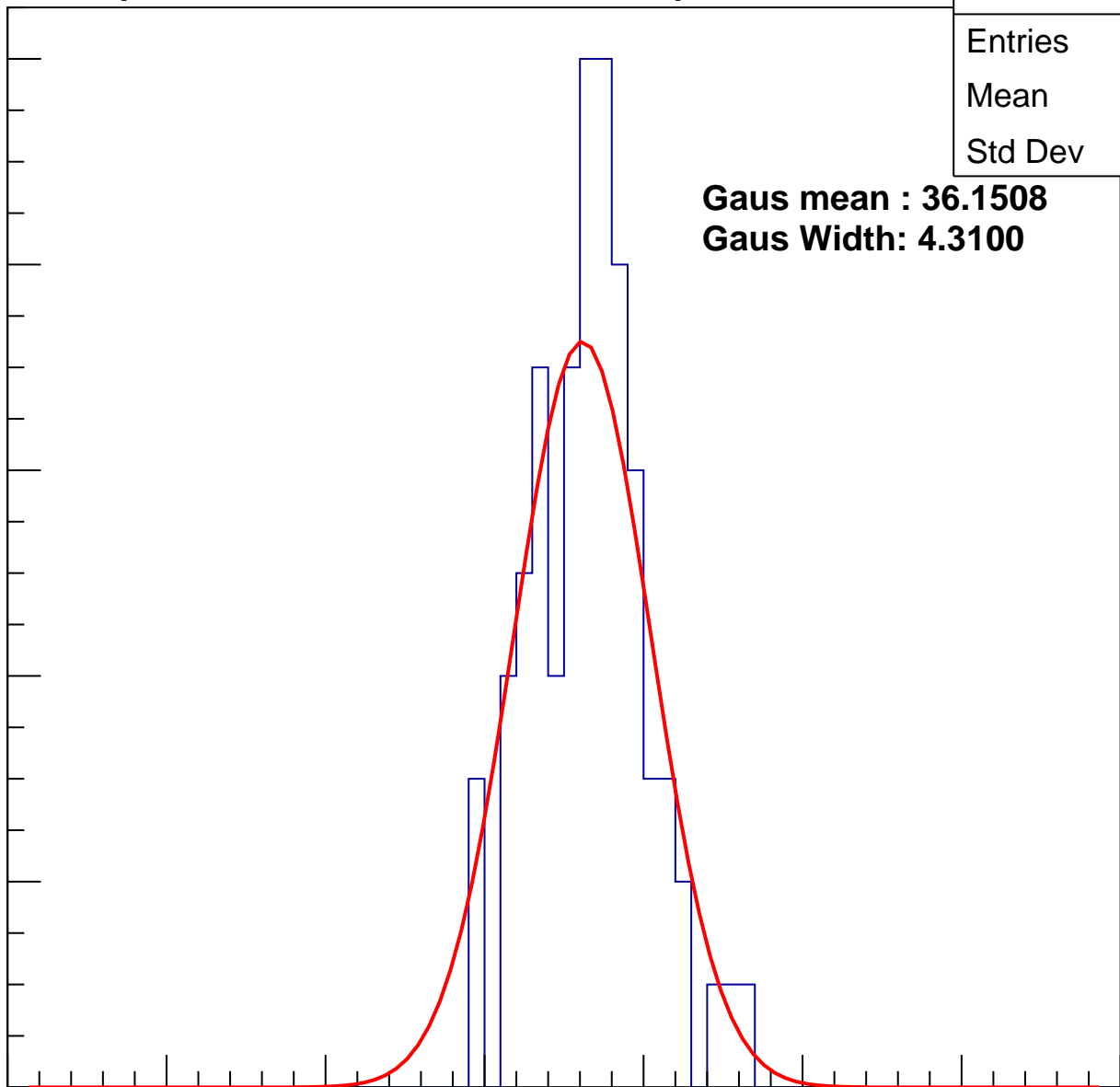
**Gaus Width: 4.3100**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U24-ch41, adc2

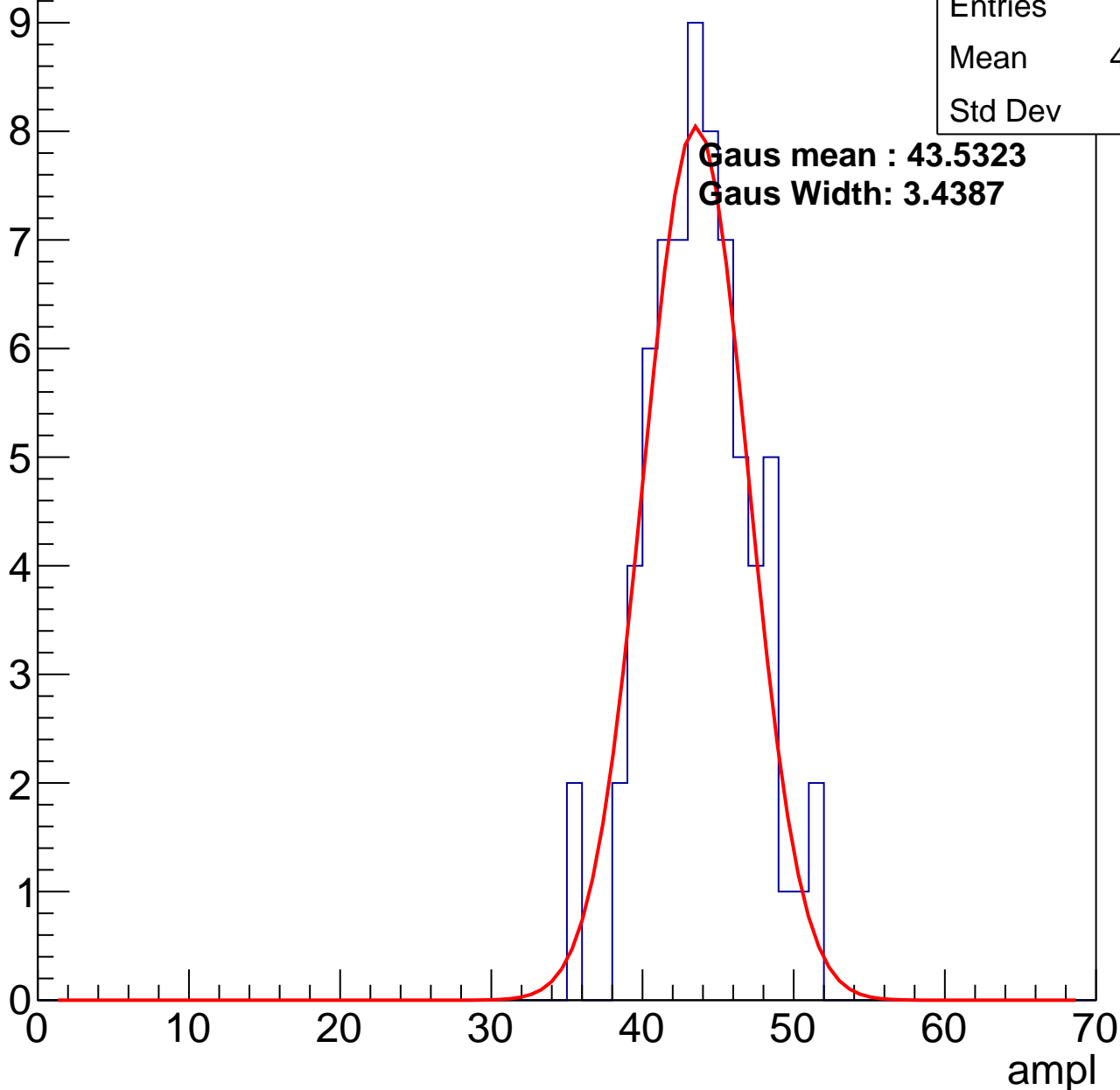
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	43.37
Std Dev	3.39

**Gaus mean : 43.5323**

**Gaus Width: 3.4387**

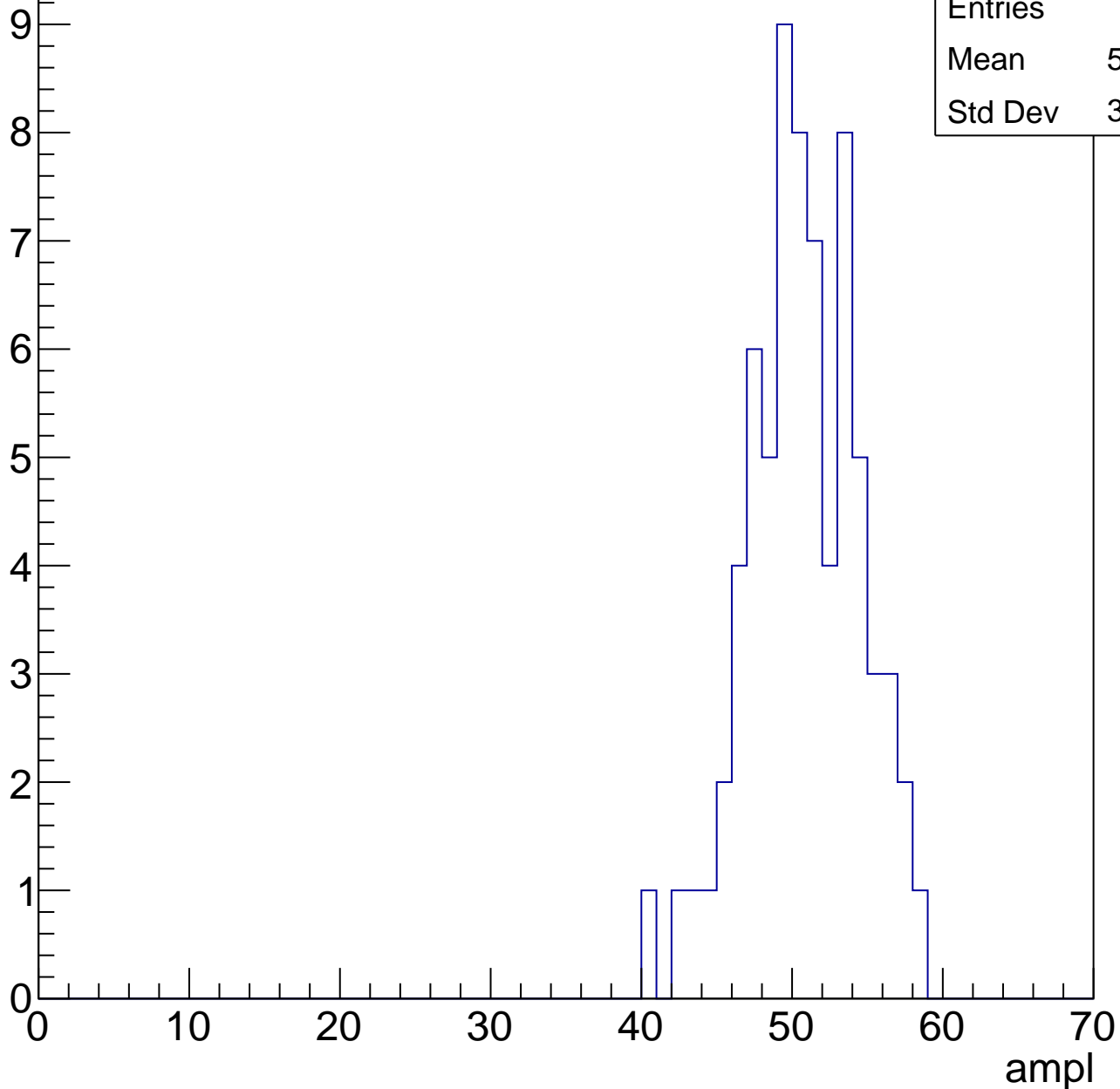


# B0L001S, U24-ch41, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	50.28
Std Dev	3.678

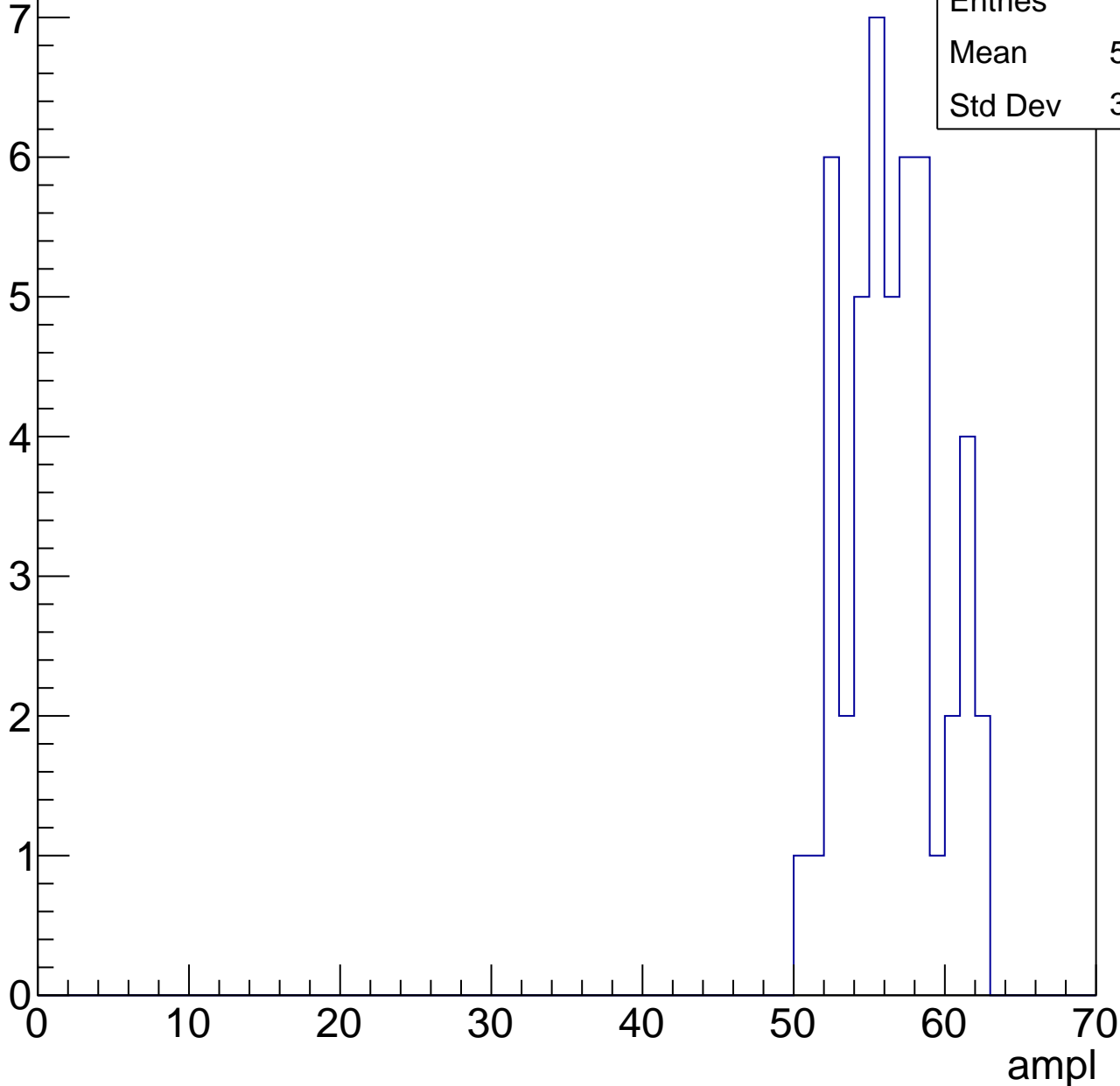


# B0L001S, U24-ch41, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

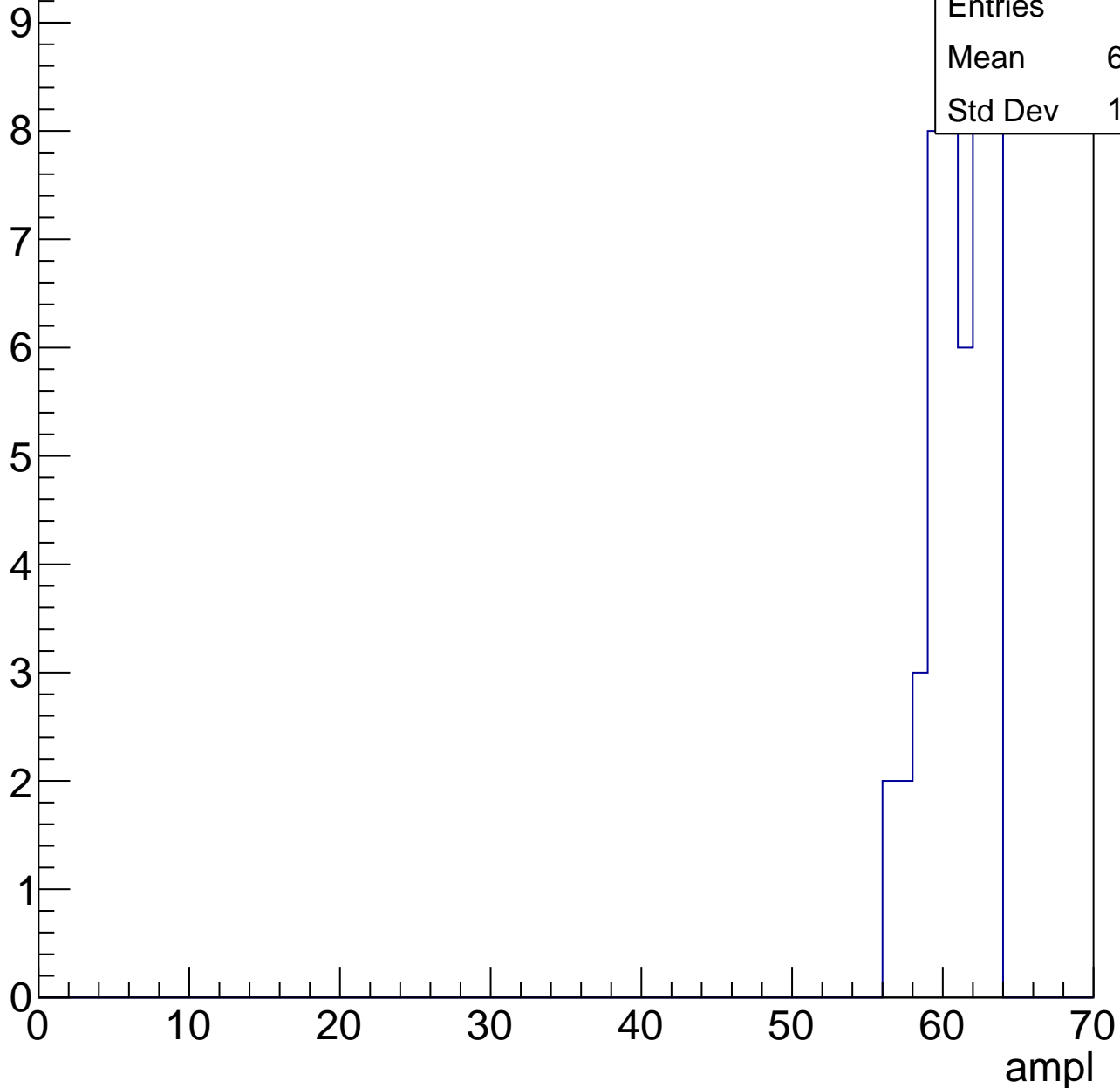
Entries	48
Mean	56.06
Std Dev	3.044



# B0L001S, U24-ch41, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

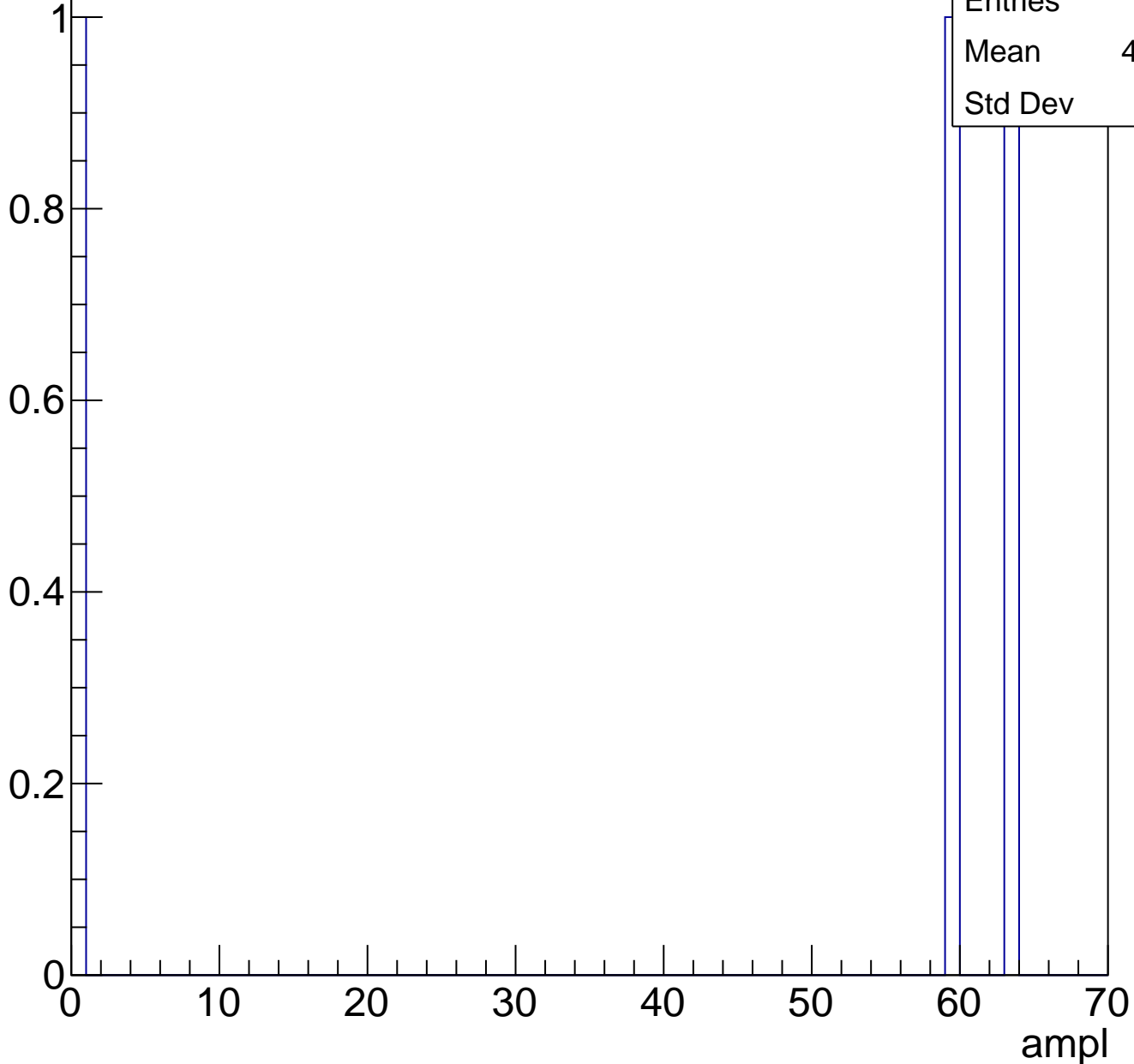


Entries	46
Mean	60.46
Std Dev	1.975

# B0L001S, U24-ch41, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch41, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U24-ch42, adc0

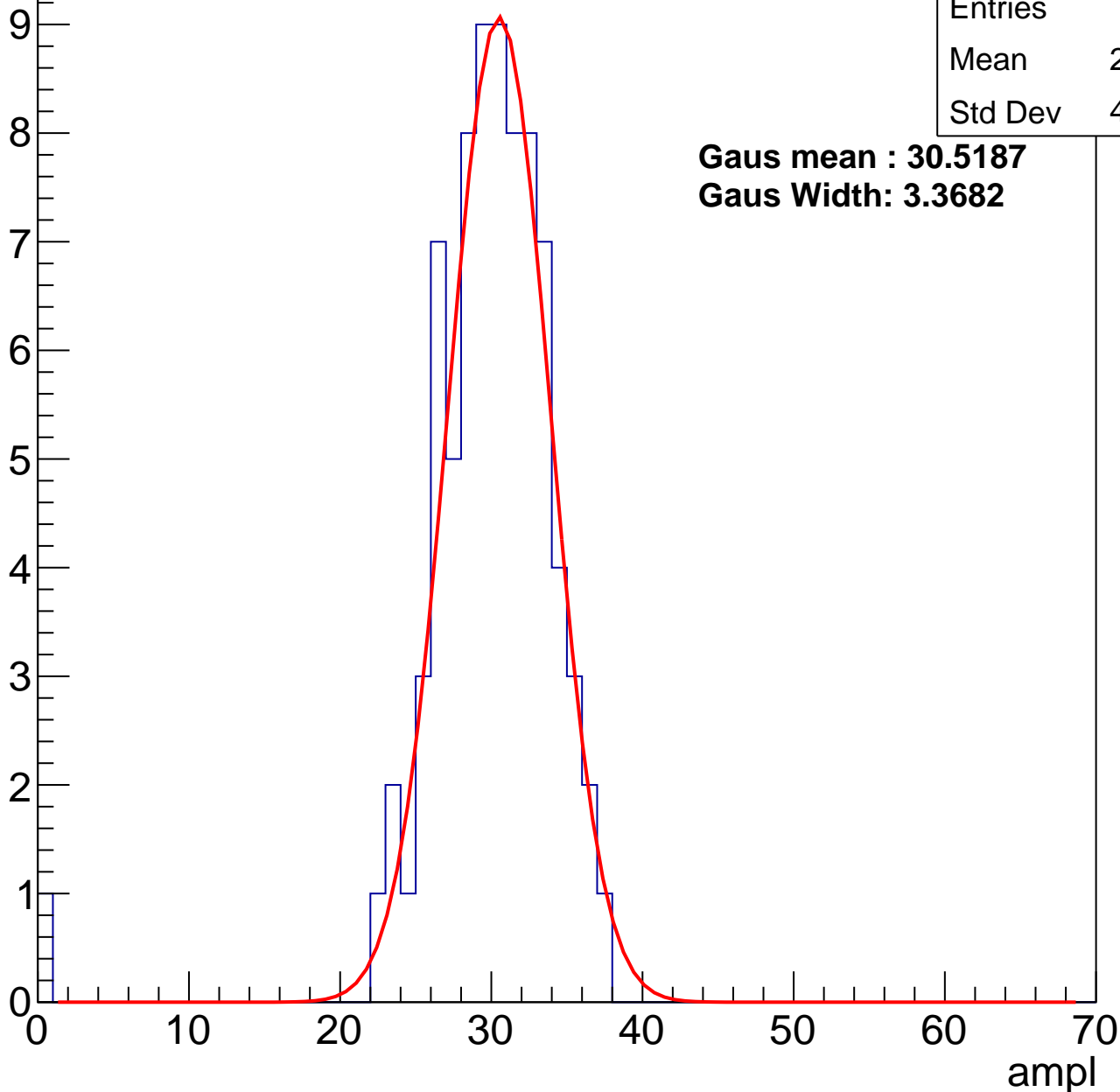
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	79
Mean	29.42
Std Dev	4.649

**Gaus mean : 30.5187**

**Gaus Width: 3.3682**



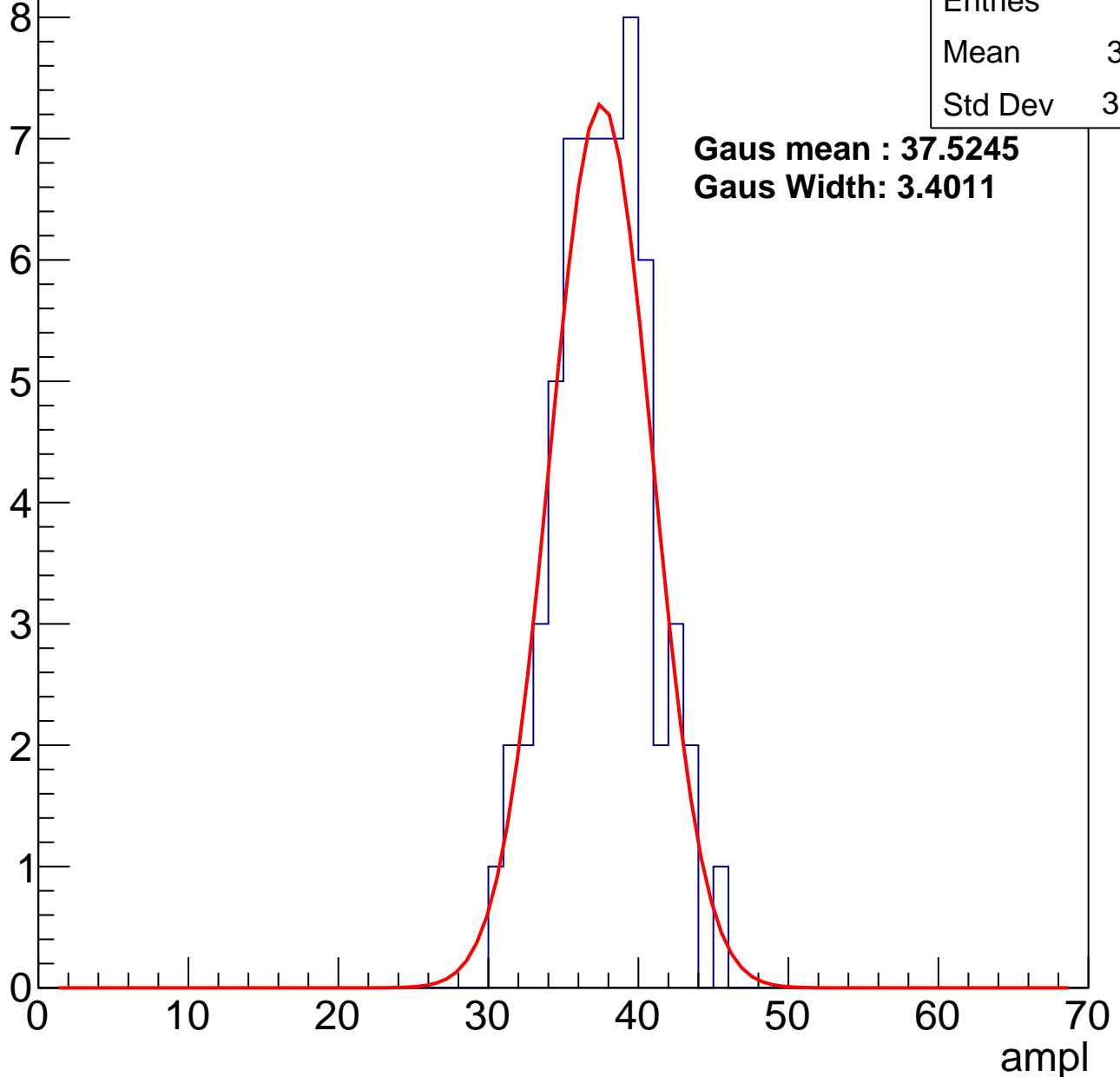
# B0L001S, U24-ch42, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	37.11
Std Dev	3.173

**Gaus mean : 37.5245**  
**Gaus Width: 3.4011**



# B0L001S, U24-ch42, adc2

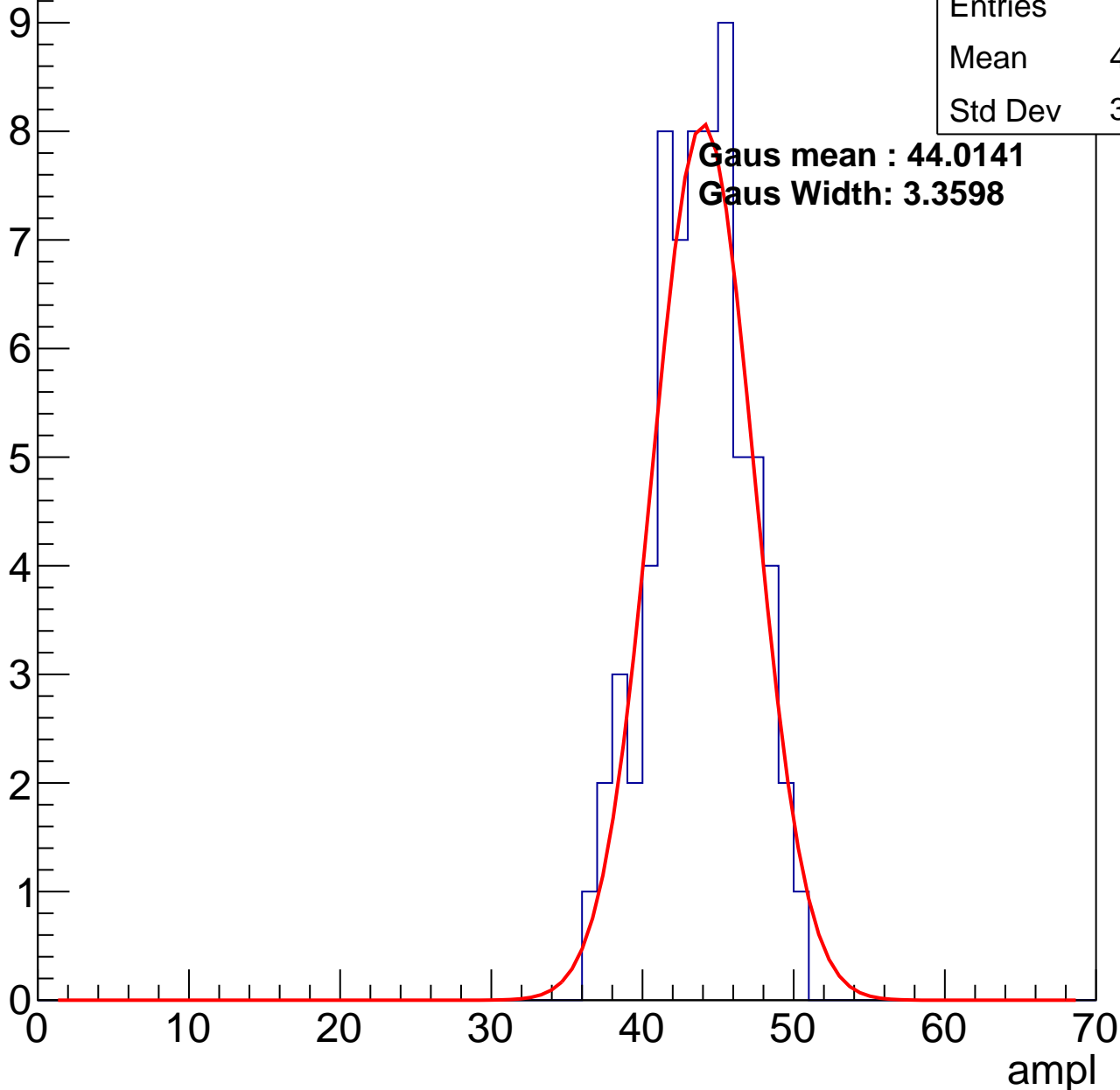
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	43.33
Std Dev	3.152

**Gaus mean : 44.0141**

**Gaus Width: 3.3598**



# B0L001S, U24-ch42, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

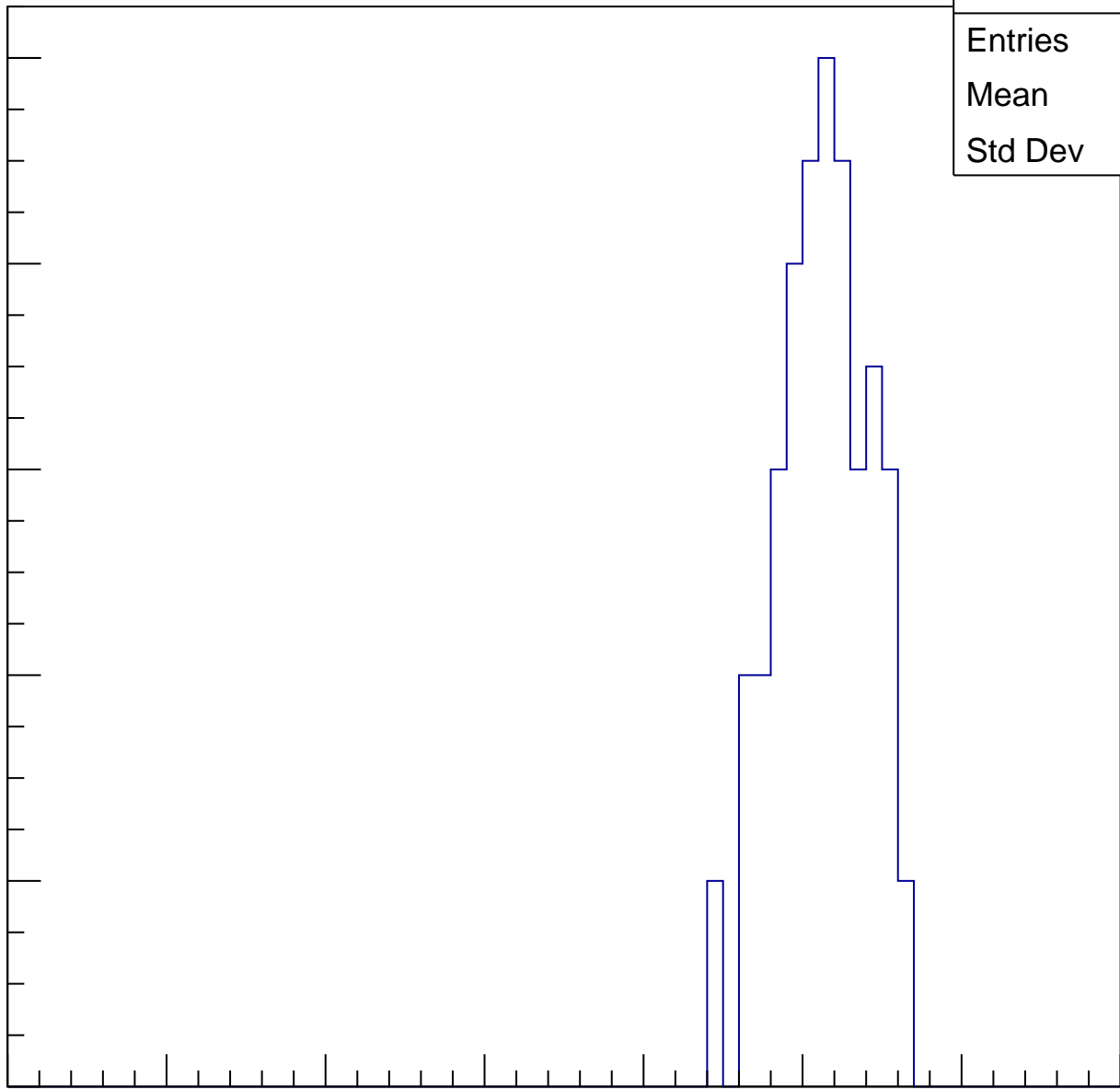
Entries	73
Mean	50.77
Std Dev	2.855

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

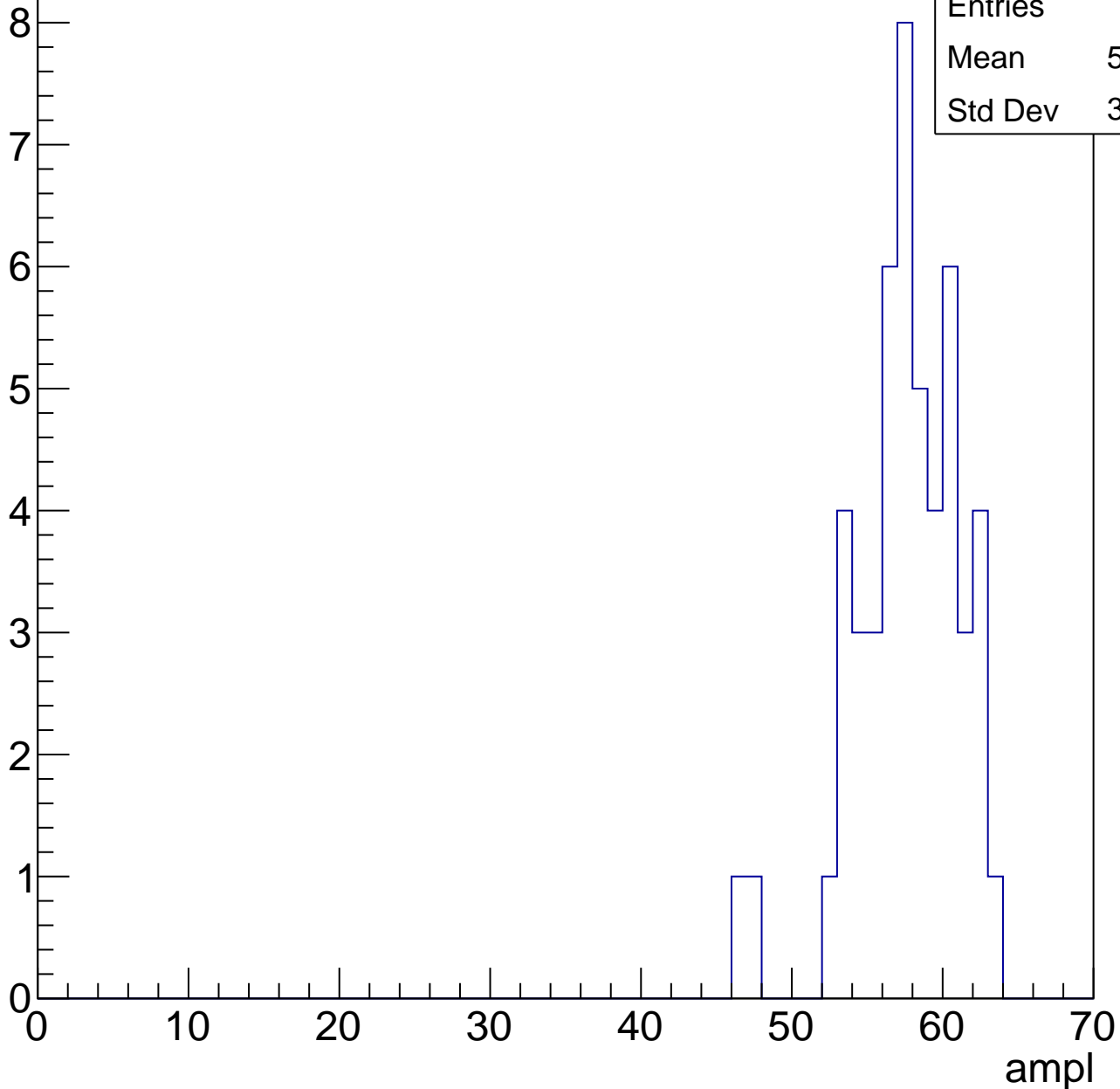


# B0L001S, U24-ch42, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

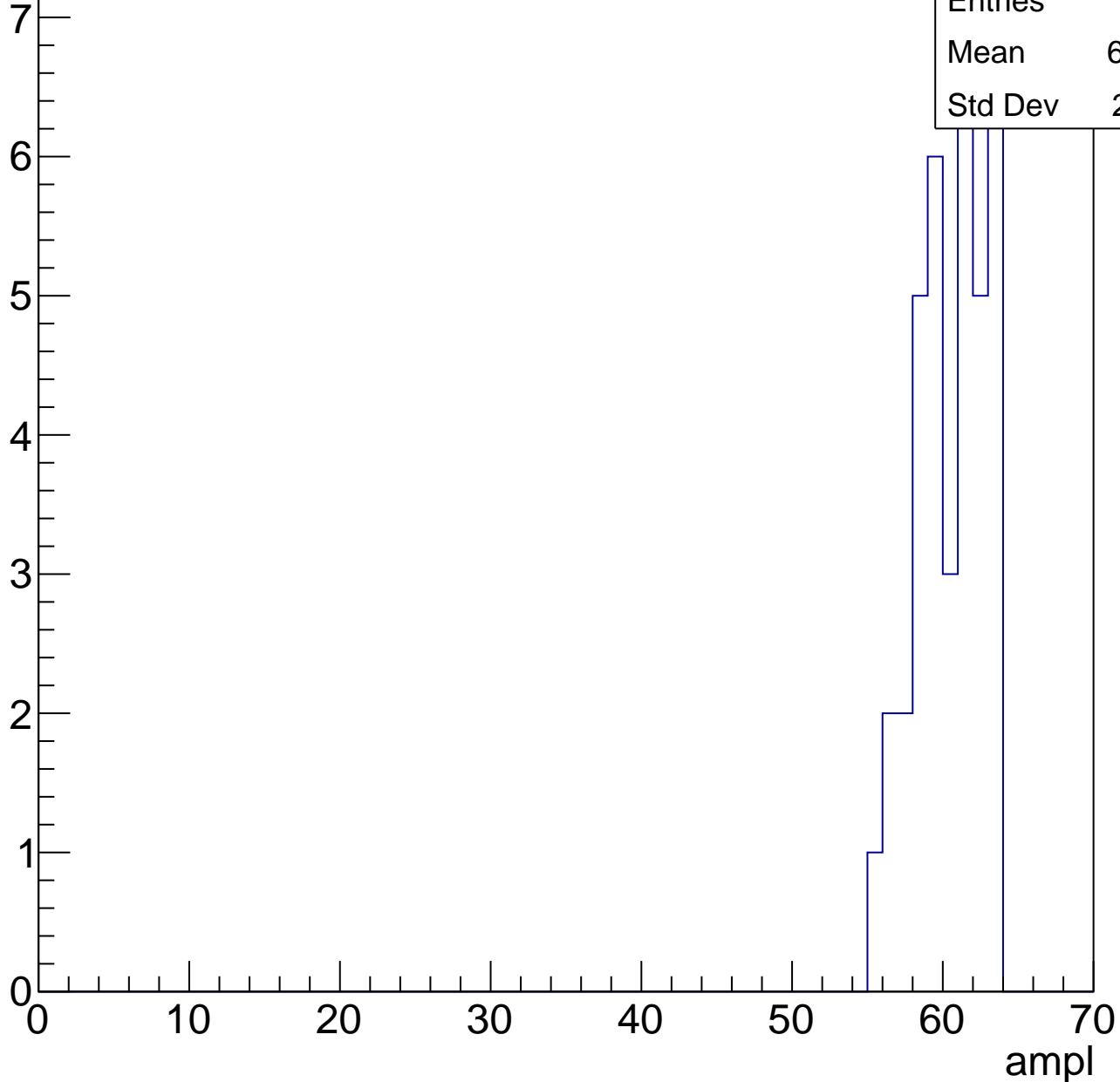
Entries	50
Mean	57.12
Std Dev	3.502



# B0L001S, U24-ch42, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U24-ch42, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

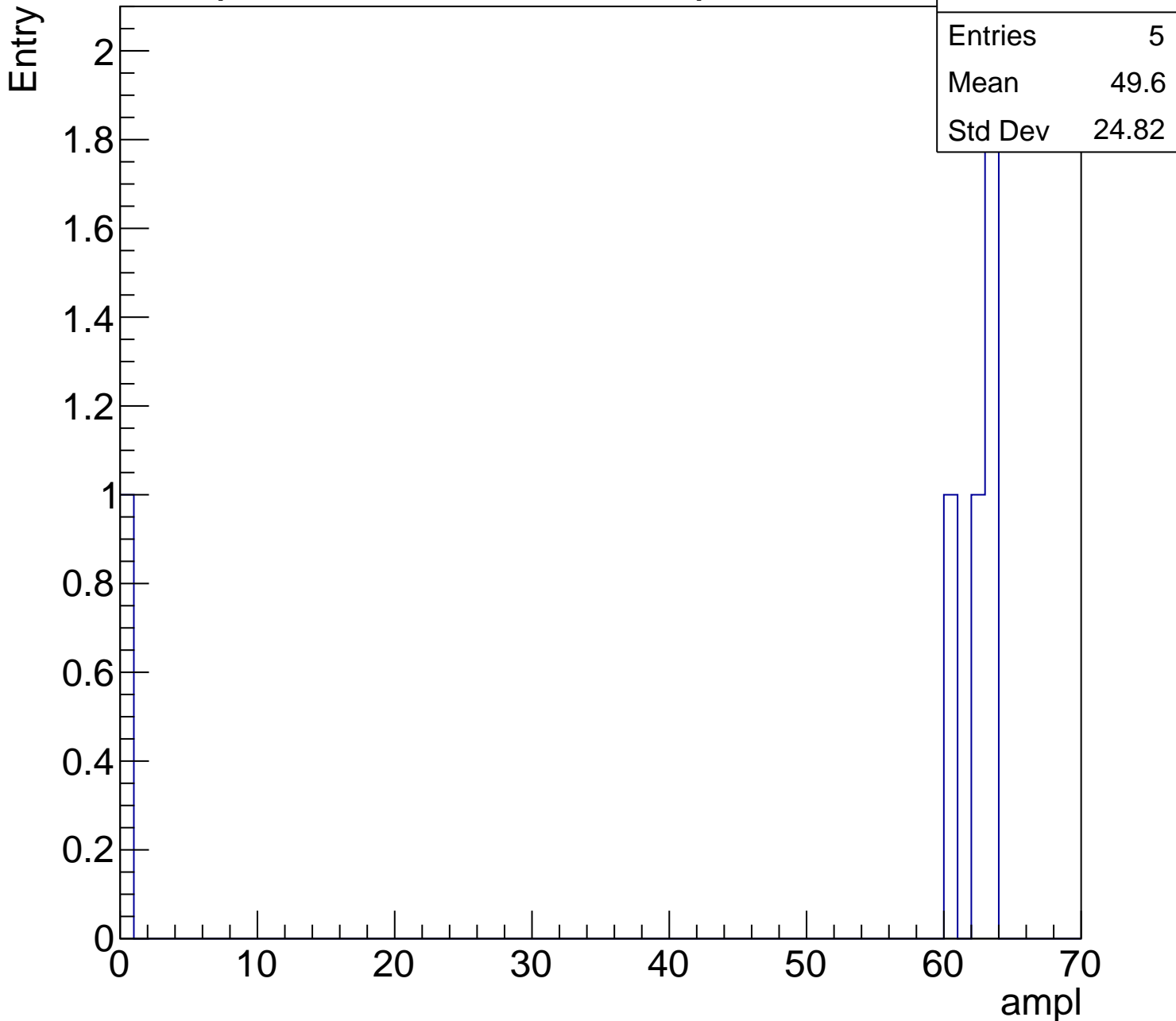
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	49.6
Std Dev	24.82

0 10 20 30 40 50 60 70

ampl





# B0L001S, U24-ch42, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U24-ch43, adc0

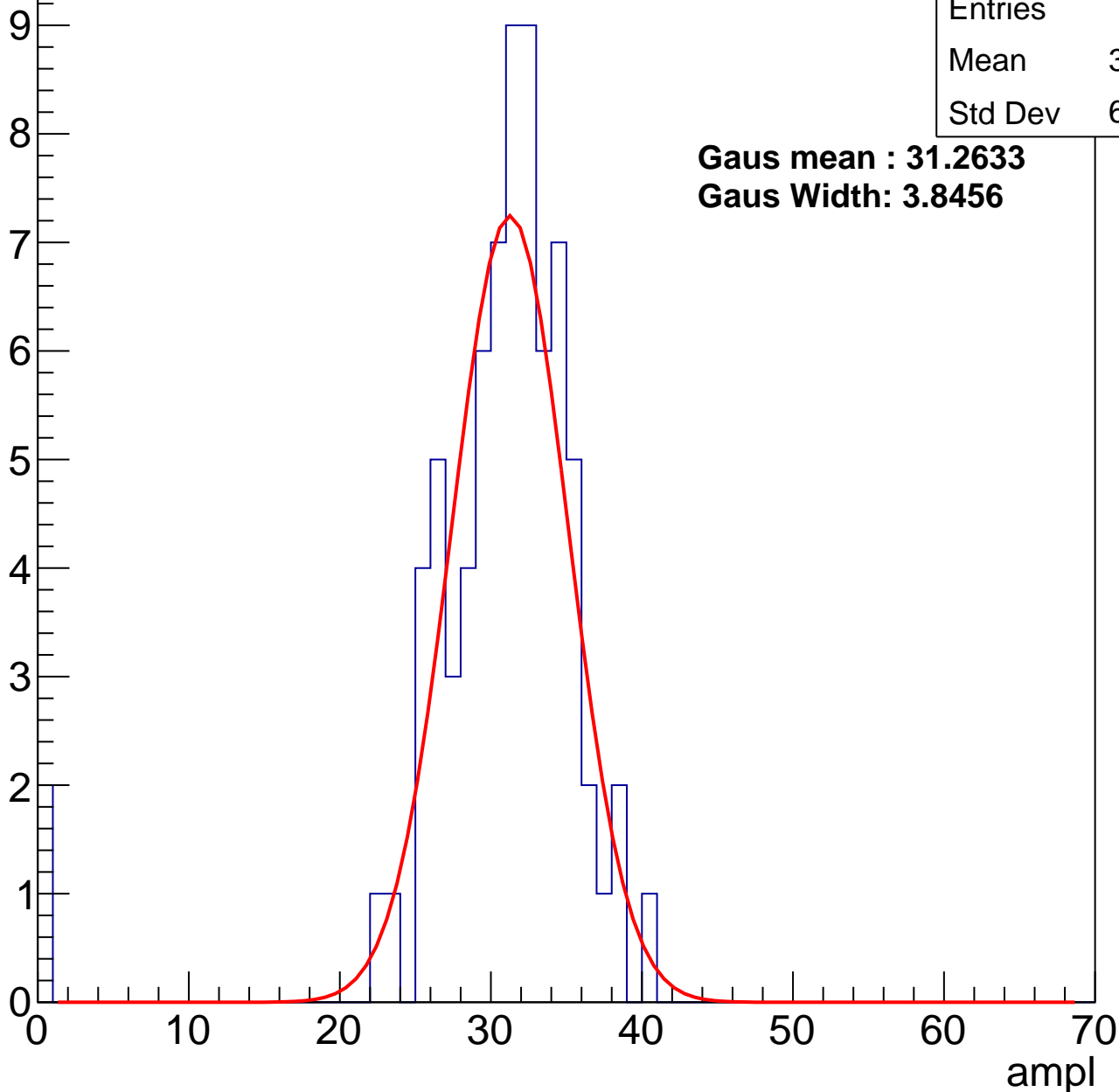
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	75
Mean	30.07
Std Dev	6.139

**Gaus mean : 31.2633**

**Gaus Width: 3.8456**



# B0L001S, U24-ch43, adc1

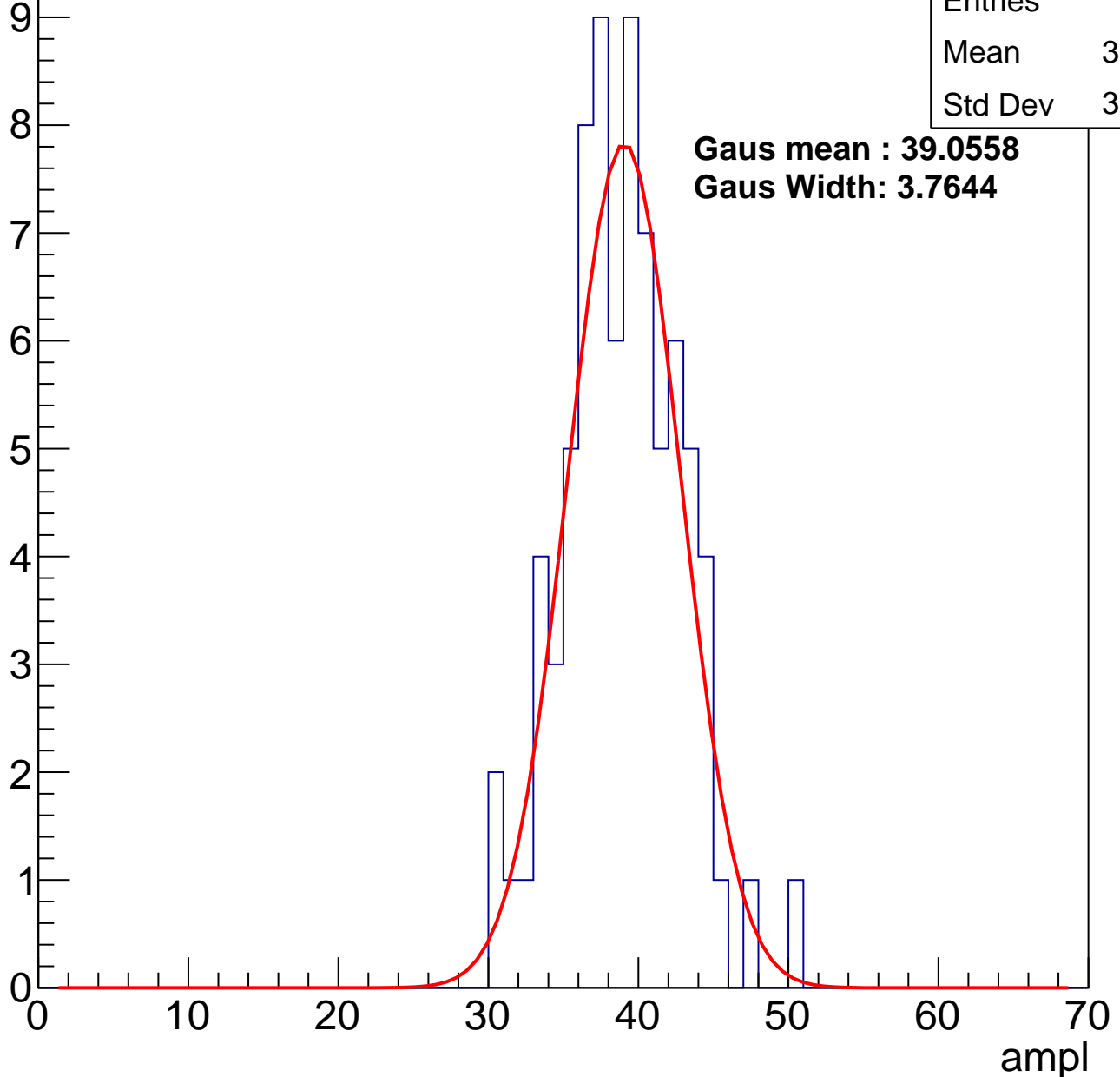
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	78
Mean	38.49
Std Dev	3.839

**Gaus mean : 39.0558**

**Gaus Width: 3.7644**



# B0L001S, U24-ch43, adc2

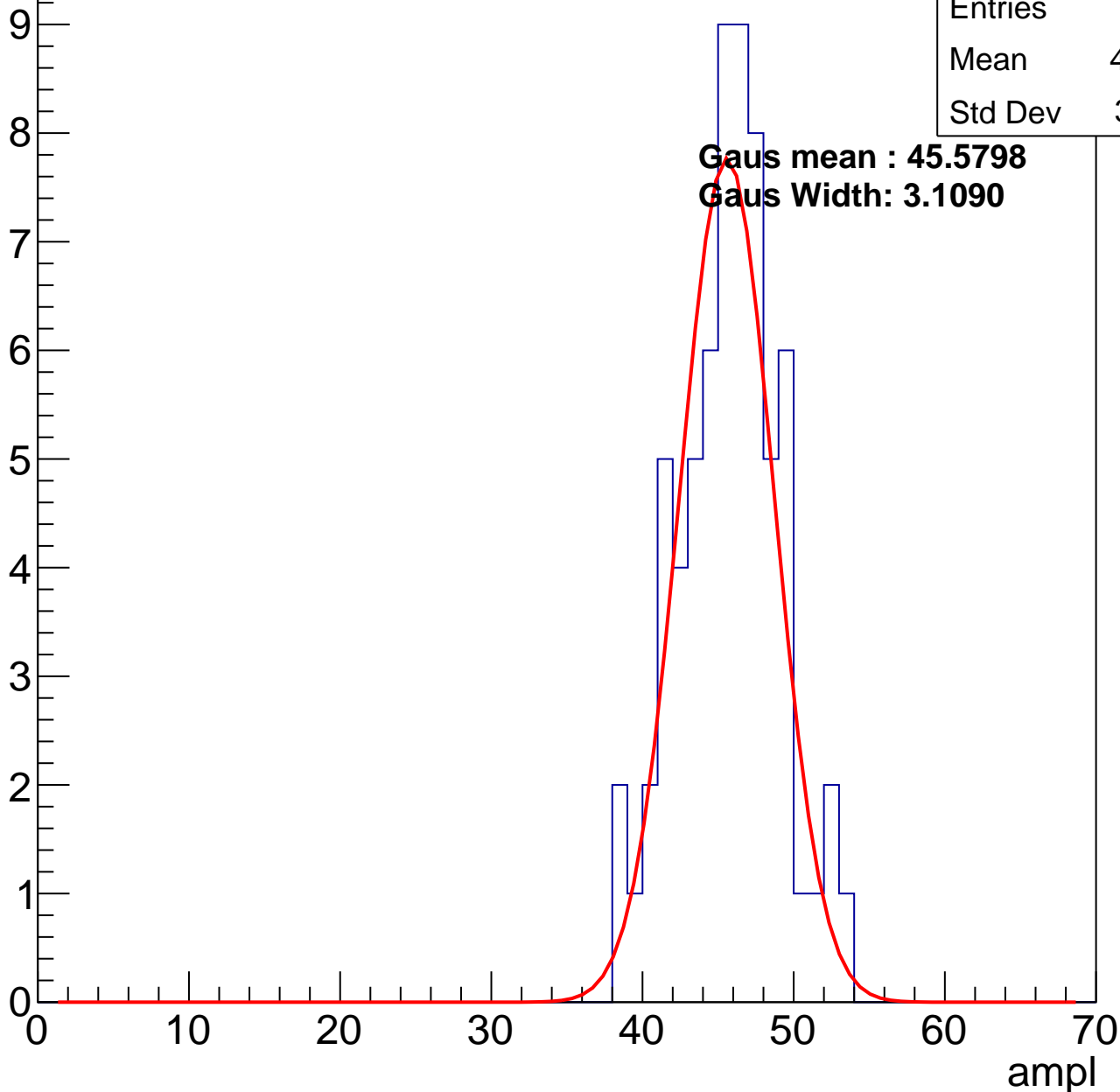
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	45.28
Std Dev	3.291

**Gaus mean : 45.5798**

**Gaus Width: 3.1090**

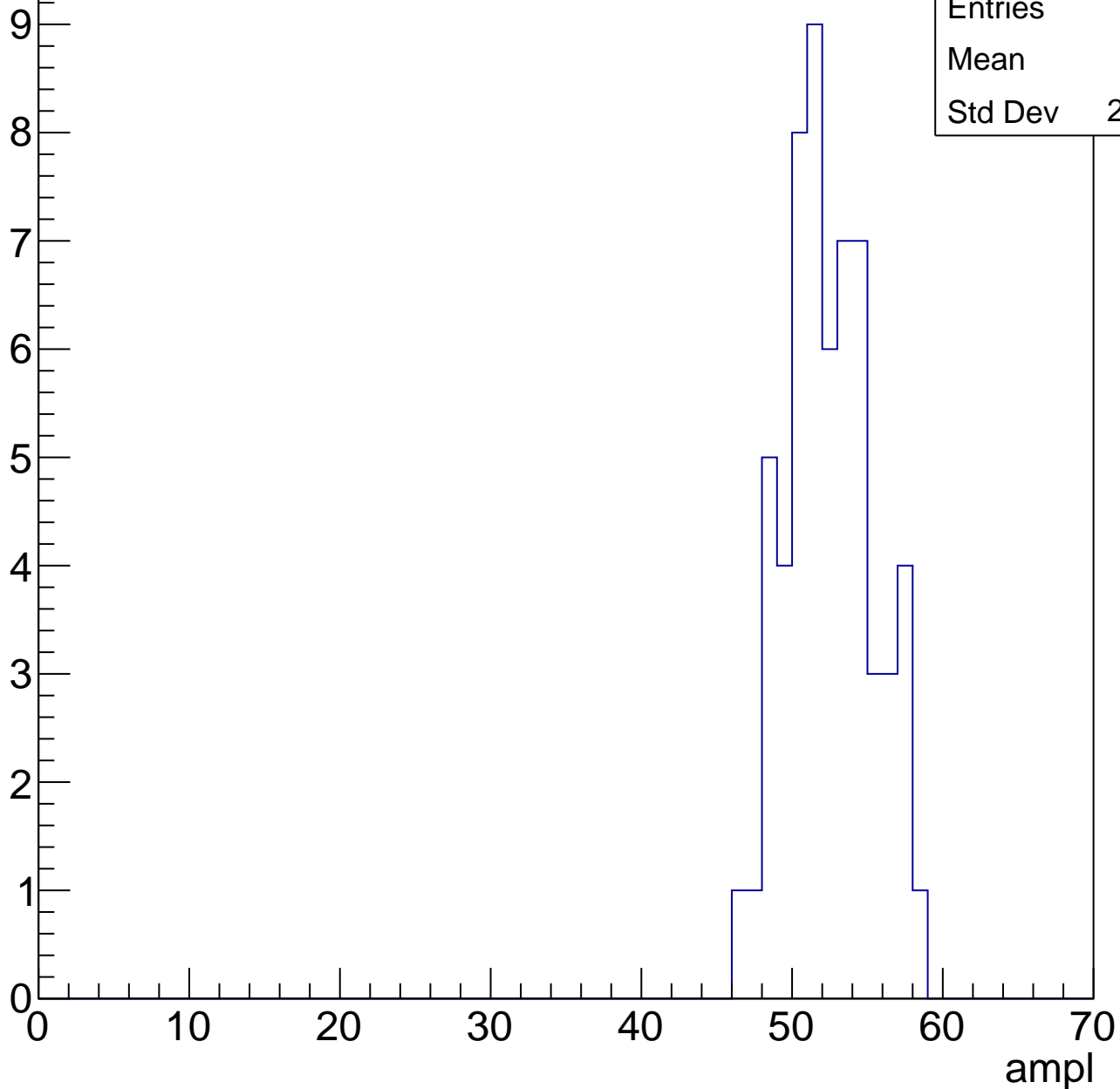


# B0L001S, U24-ch43, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

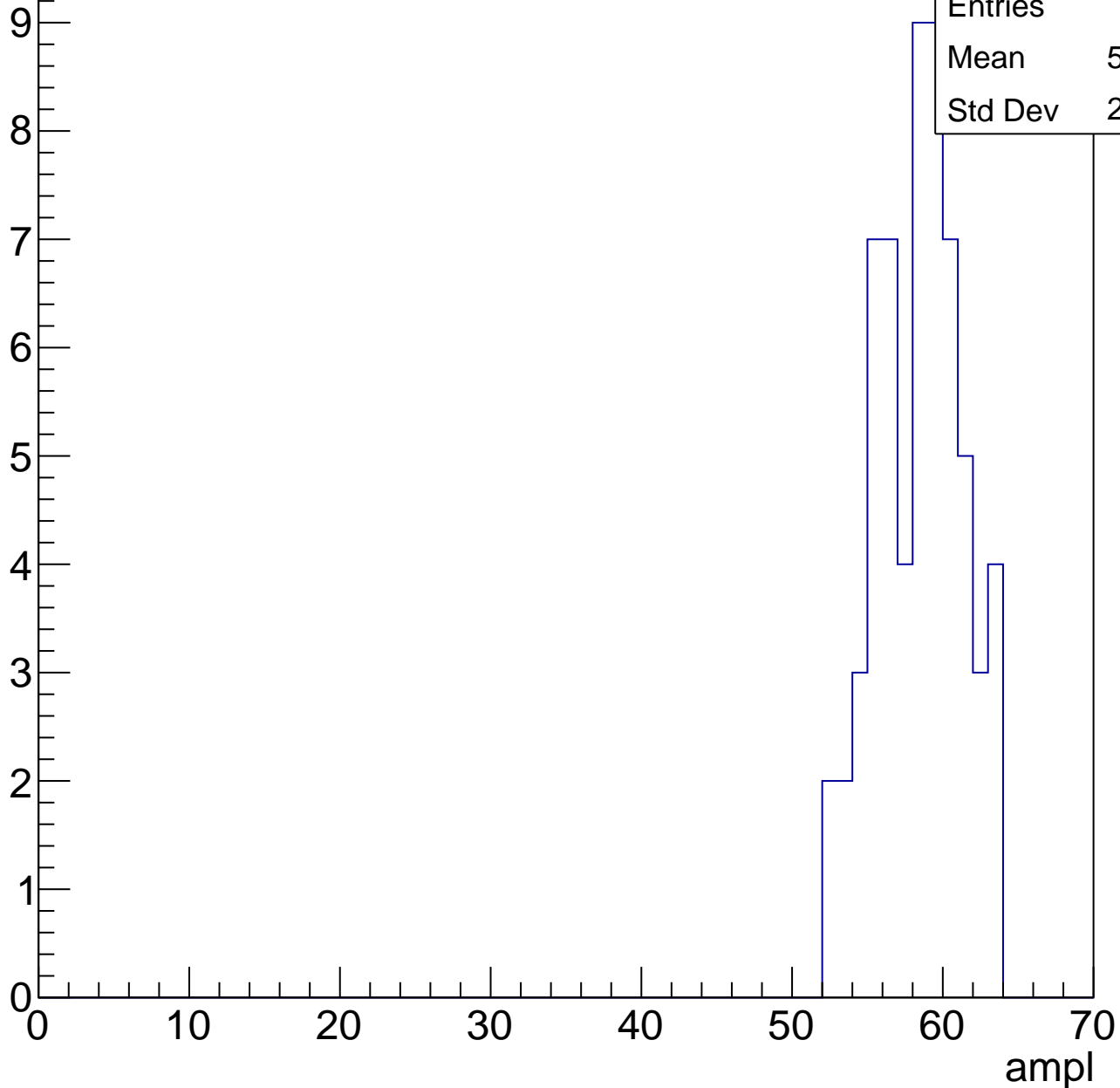
Entries	59
Mean	52
Std Dev	2.804



# B0L001S, U24-ch43, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

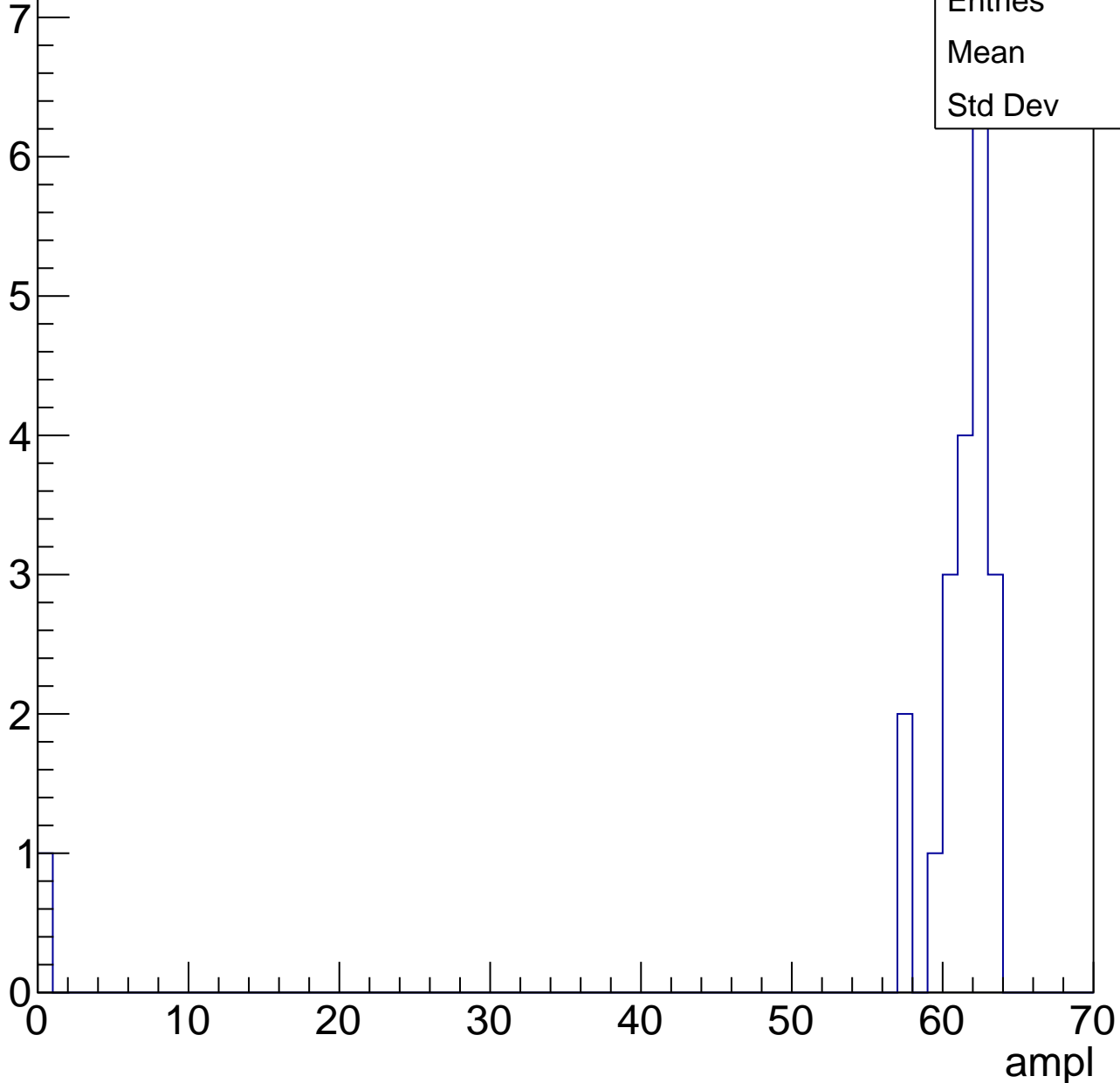


# B0L001S, U24-ch43, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	21
Mean	58.1
Std Dev	13.1



# B0L001S, U24-ch43, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch43, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U24-ch44, adc0

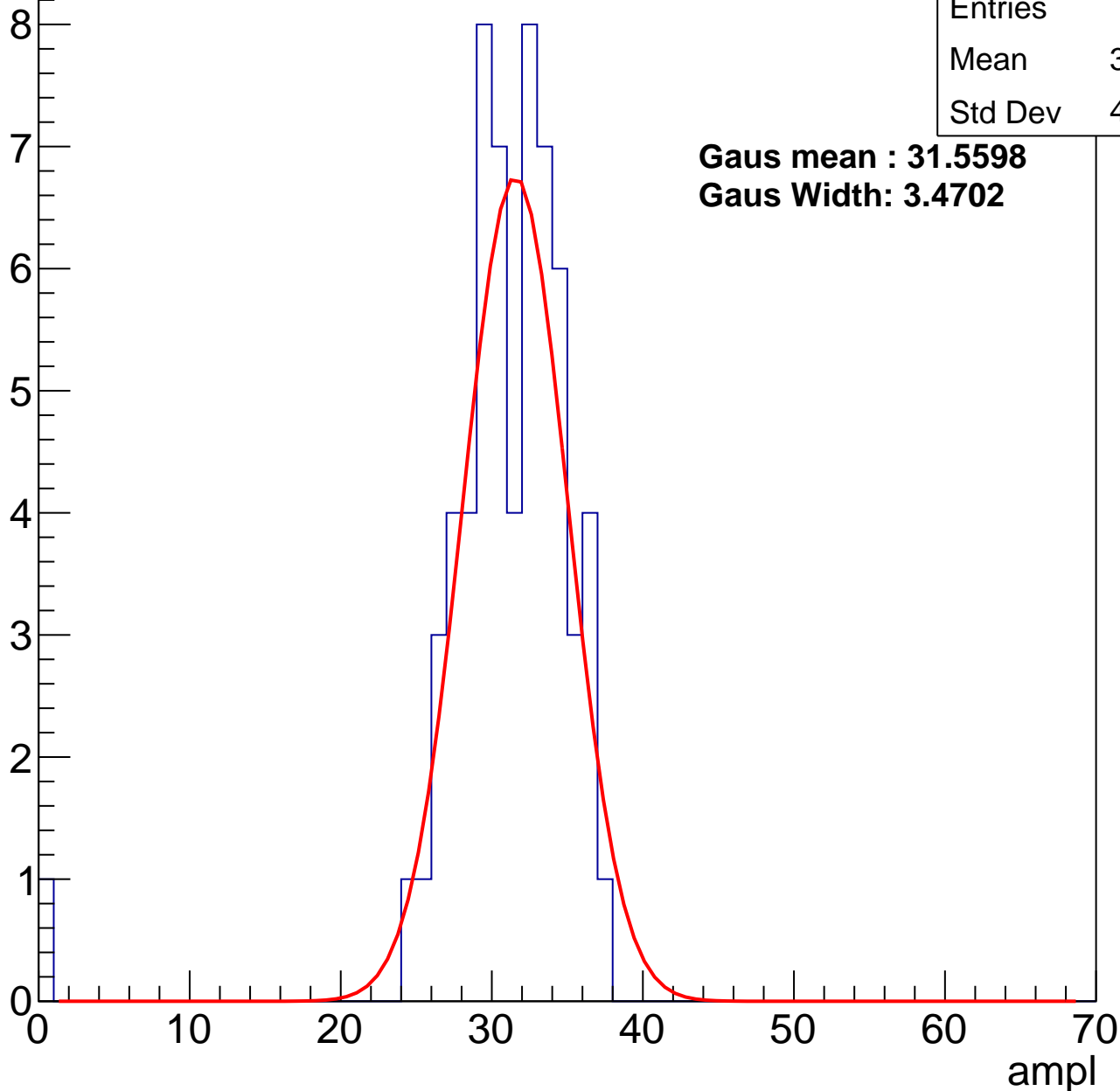
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	30.48
Std Dev	4.947

**Gaus mean : 31.5598**

**Gaus Width: 3.4702**



# B0L001S, U24-ch44, adc1

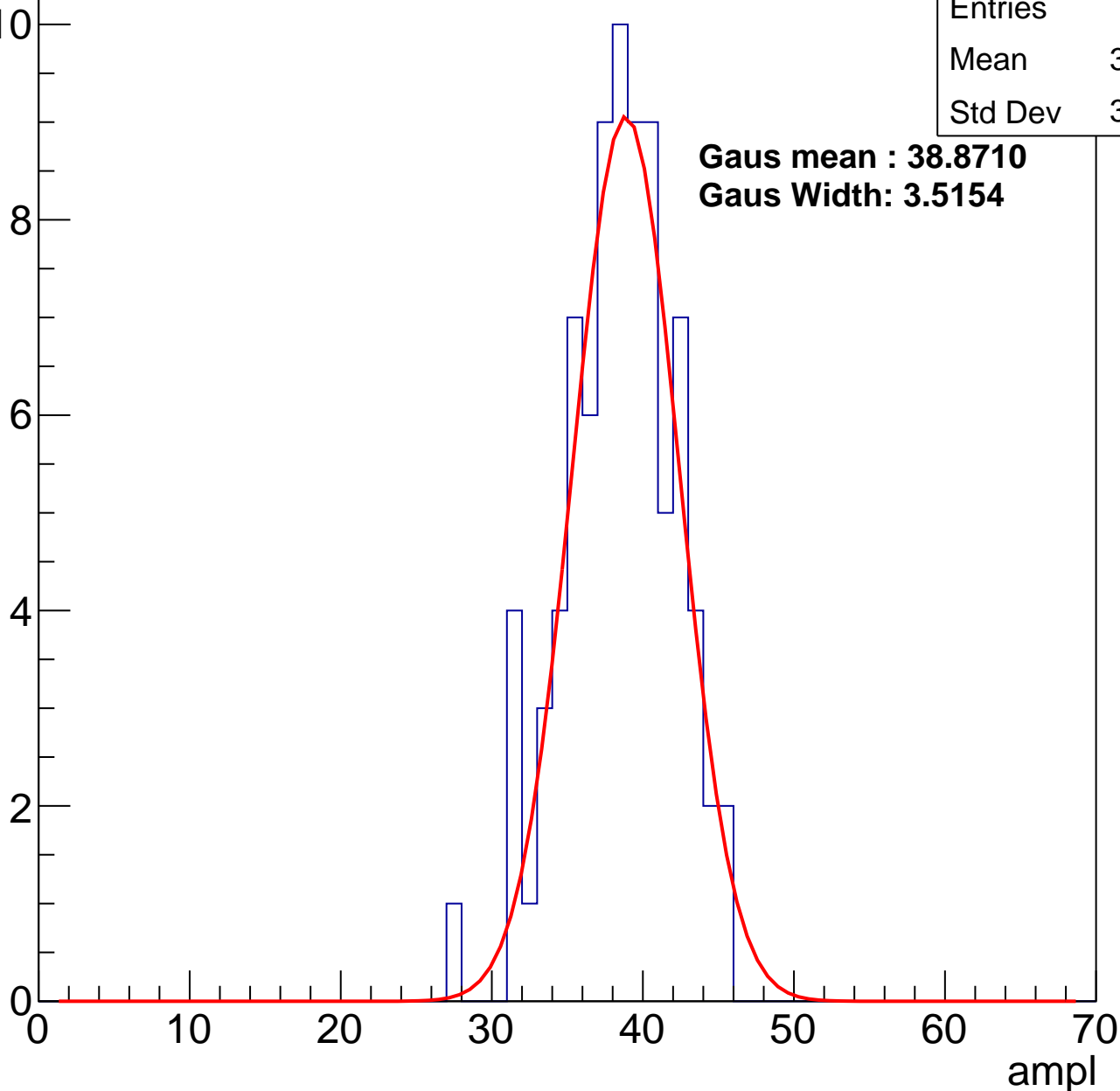
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	83
Mean	37.98
Std Dev	3.574

**Gaus mean : 38.8710**

**Gaus Width: 3.5154**



# B0L001S, U24-ch44, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	70
Mean	45.66
Std Dev	2.797

**Gaus mean : 46.2671**

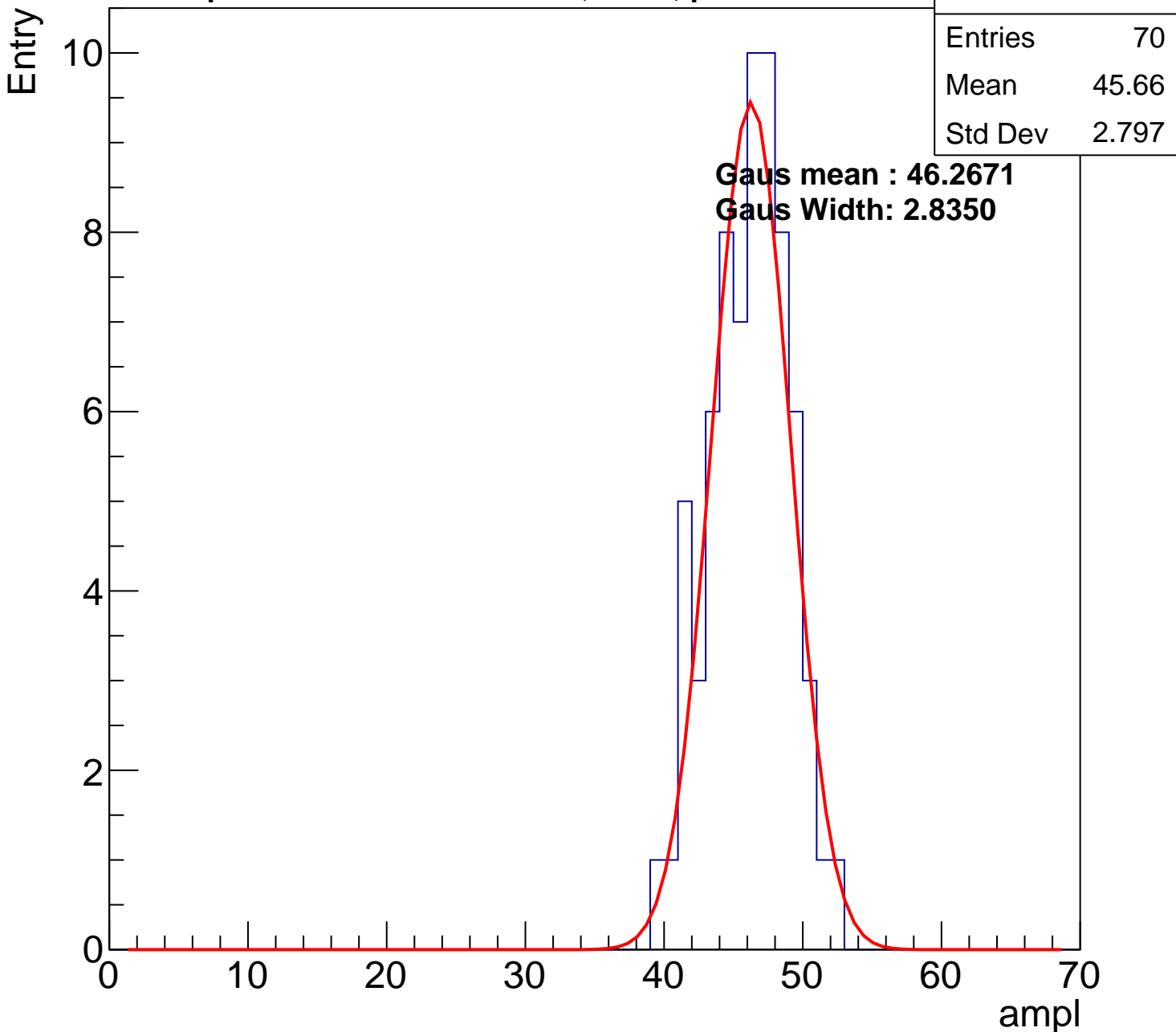
**Gaus Width: 2.8350**

Entry

10  
8  
6  
4  
2  
0

ampl

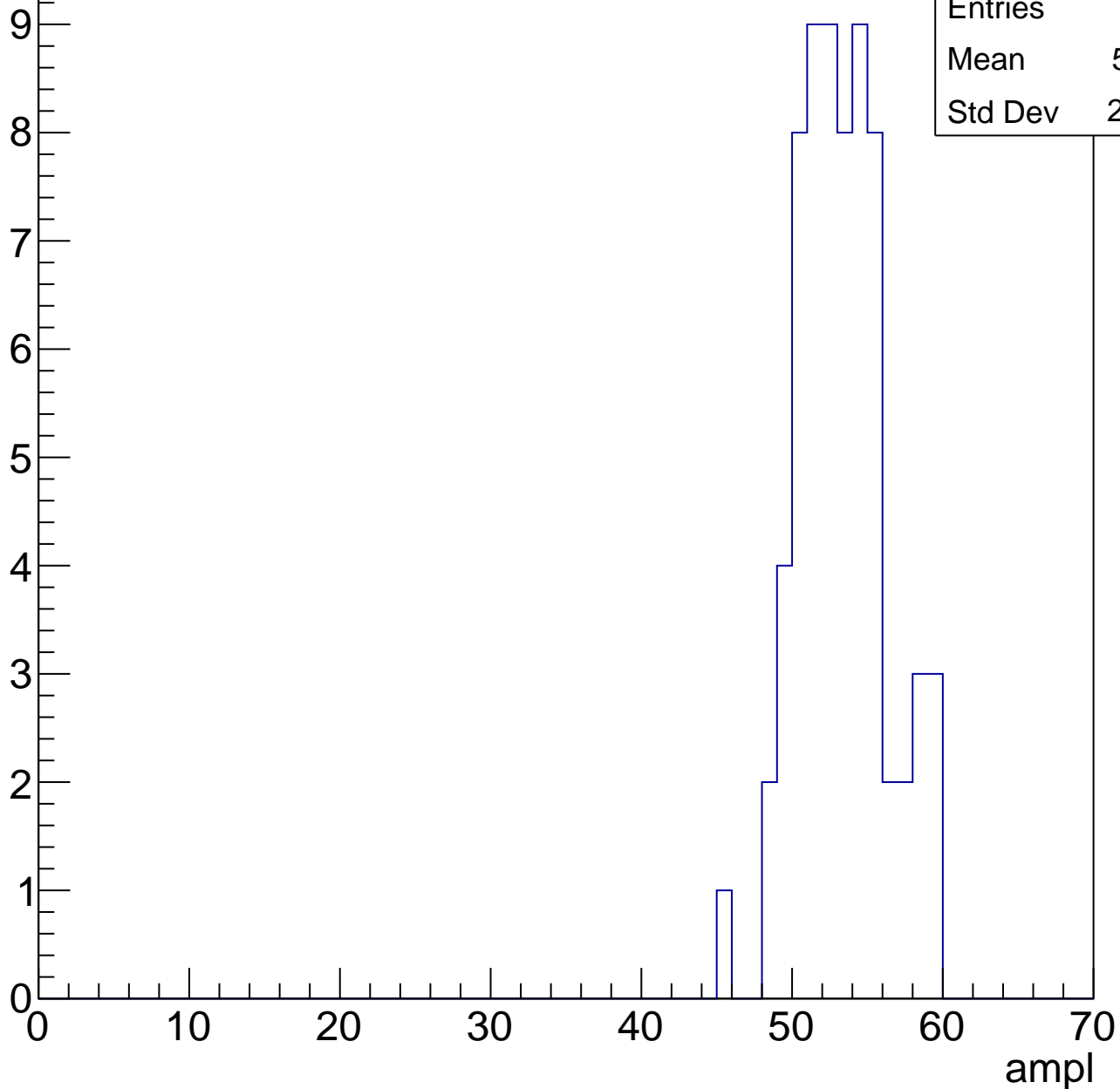
0 10 20 30 40 50 60 70



# B0L001S, U24-ch44, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



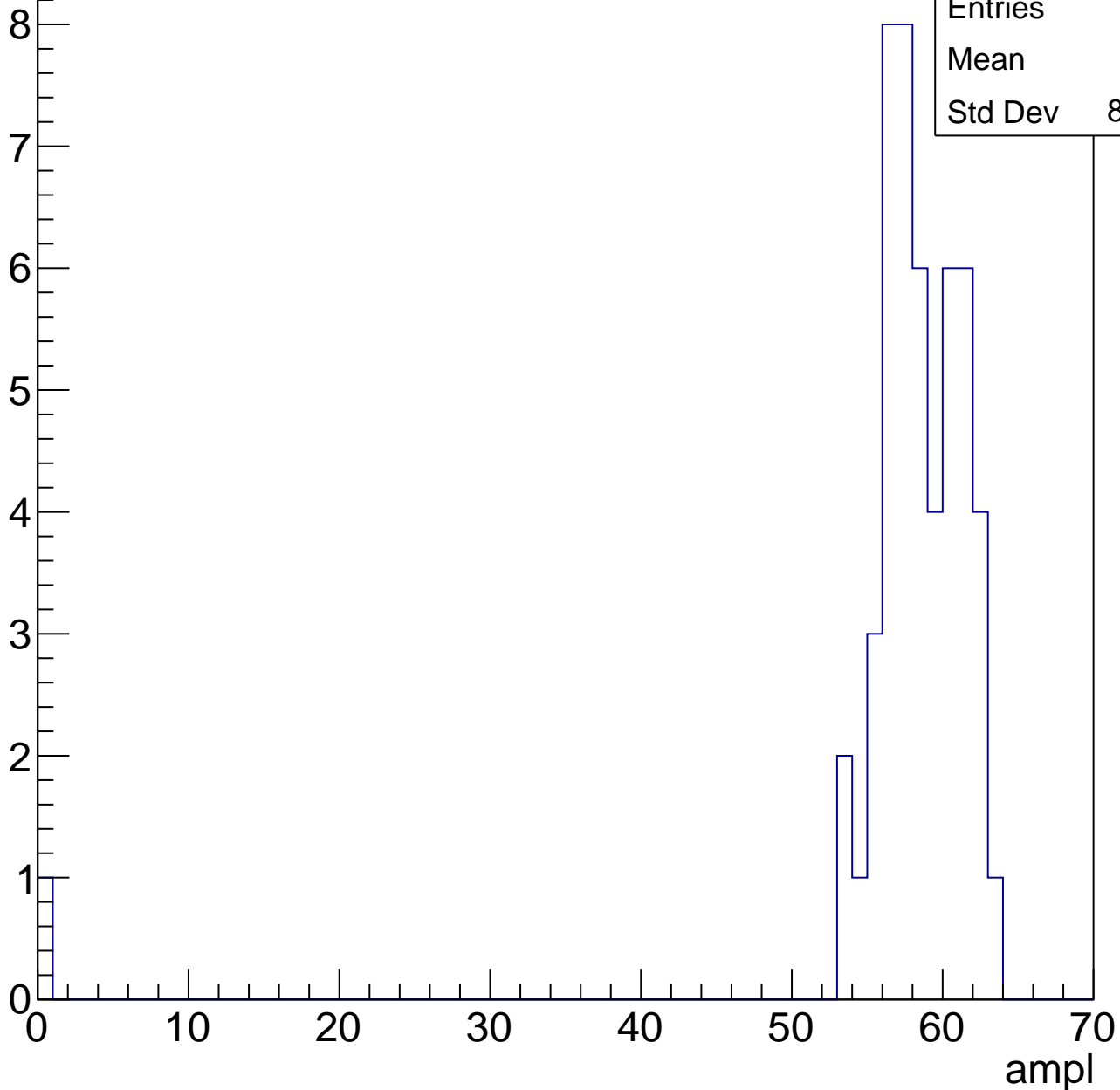
Entries	68
Mean	52.81
Std Dev	2.886

# B0L001S, U24-ch44, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	50
Mean	57
Std Dev	8.506

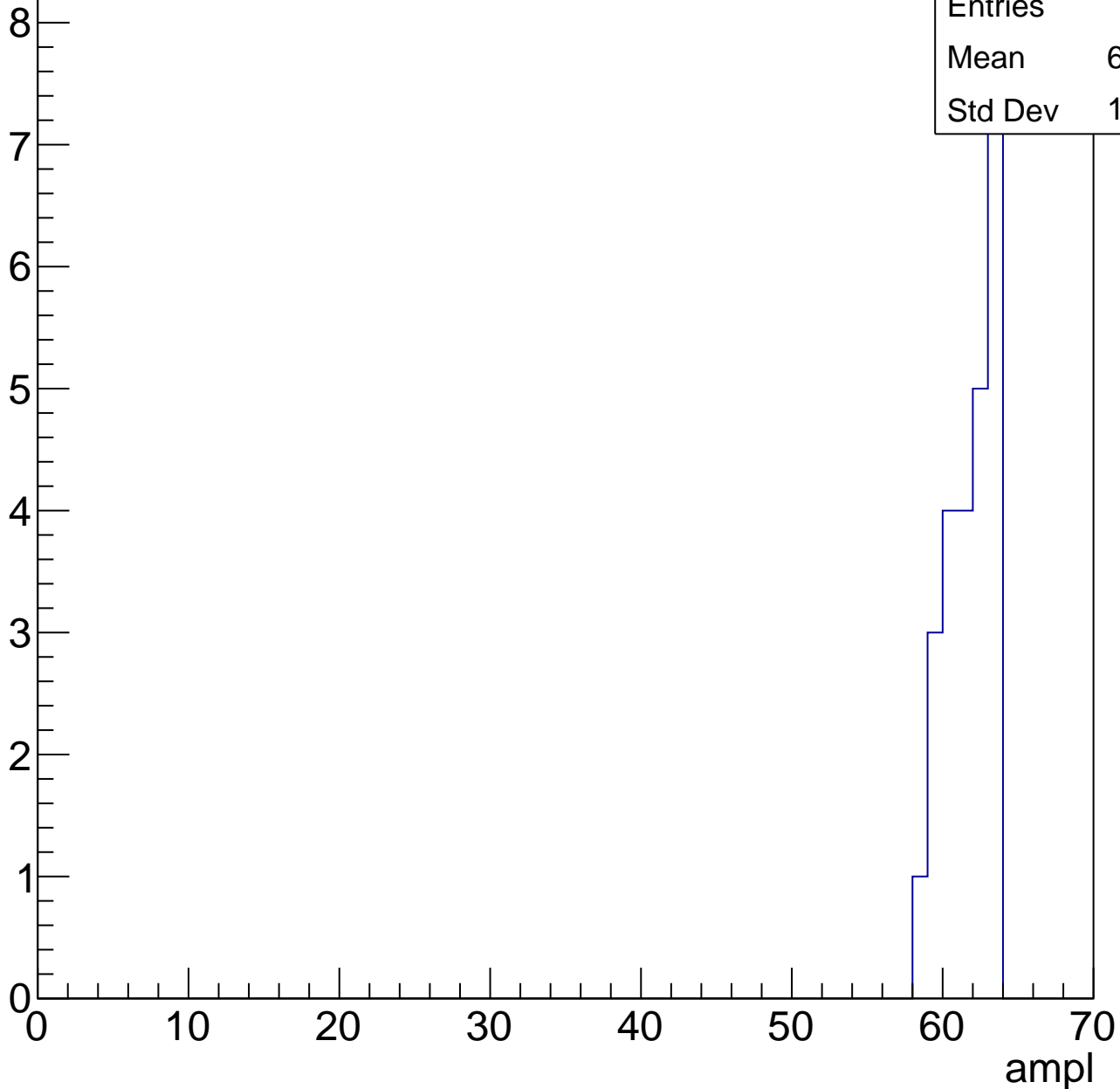


# B0L001S, U24-ch44, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	25
Mean	61.32
Std Dev	1.542



# B0L001S, U24-ch44, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch44, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U24-ch45, adc0

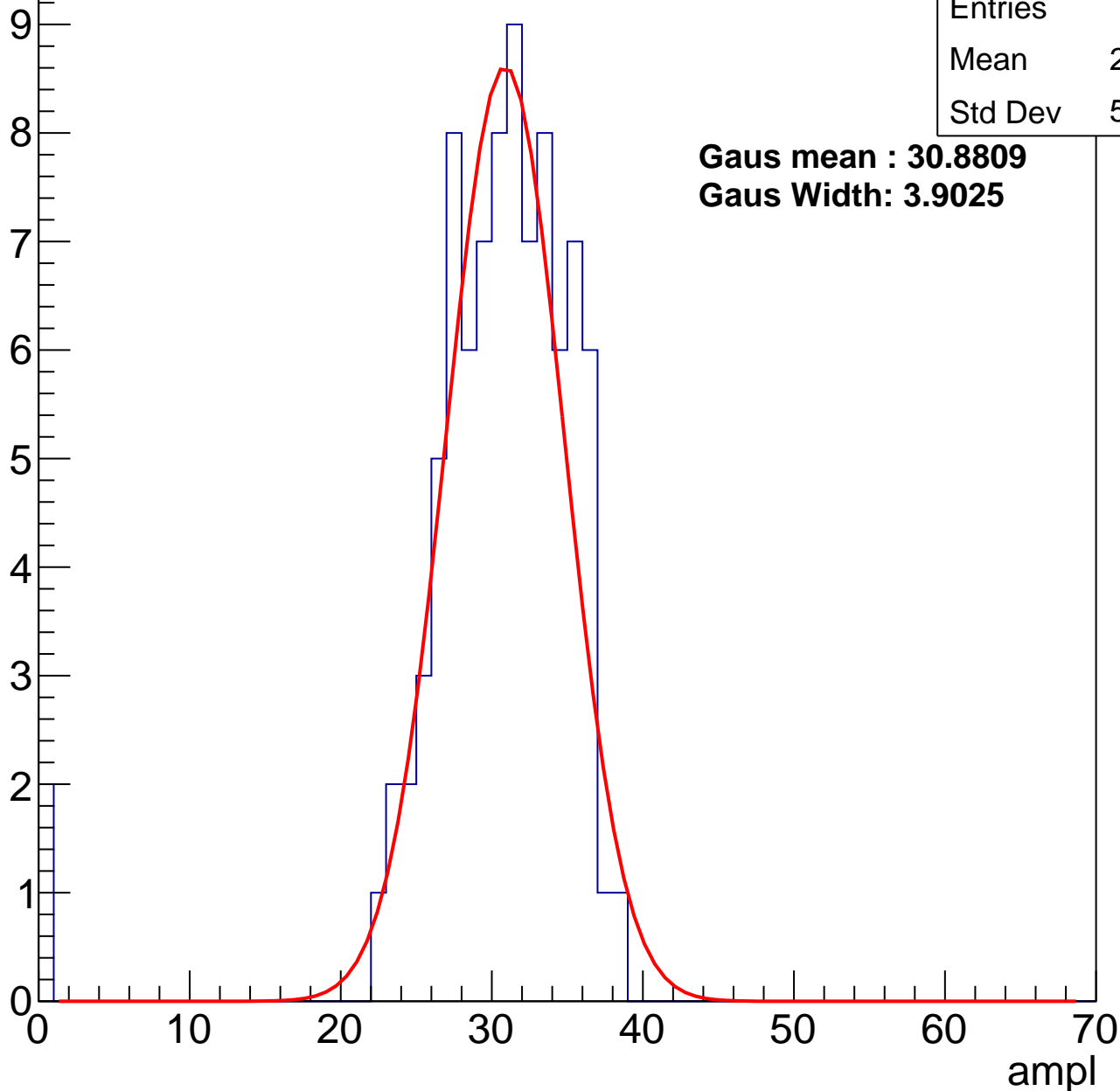
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	89
Mean	29.83
Std Dev	5.804

**Gaus mean : 30.8809**

**Gaus Width: 3.9025**



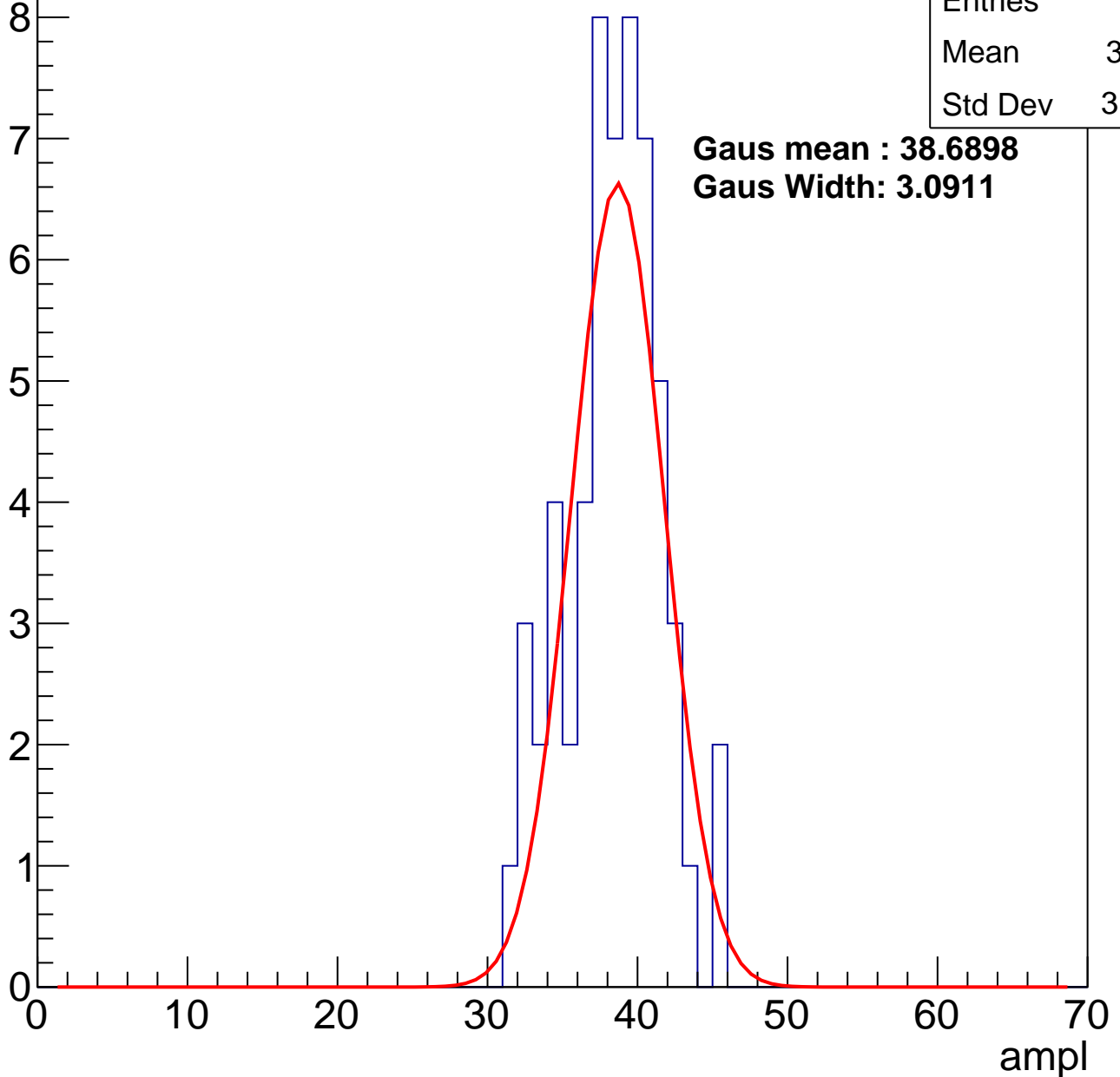
# B0L001S, U24-ch45, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	37.91
Std Dev	3.147

**Gaus mean : 38.6898**  
**Gaus Width: 3.0911**



# B0L001S, U24-ch45, adc2

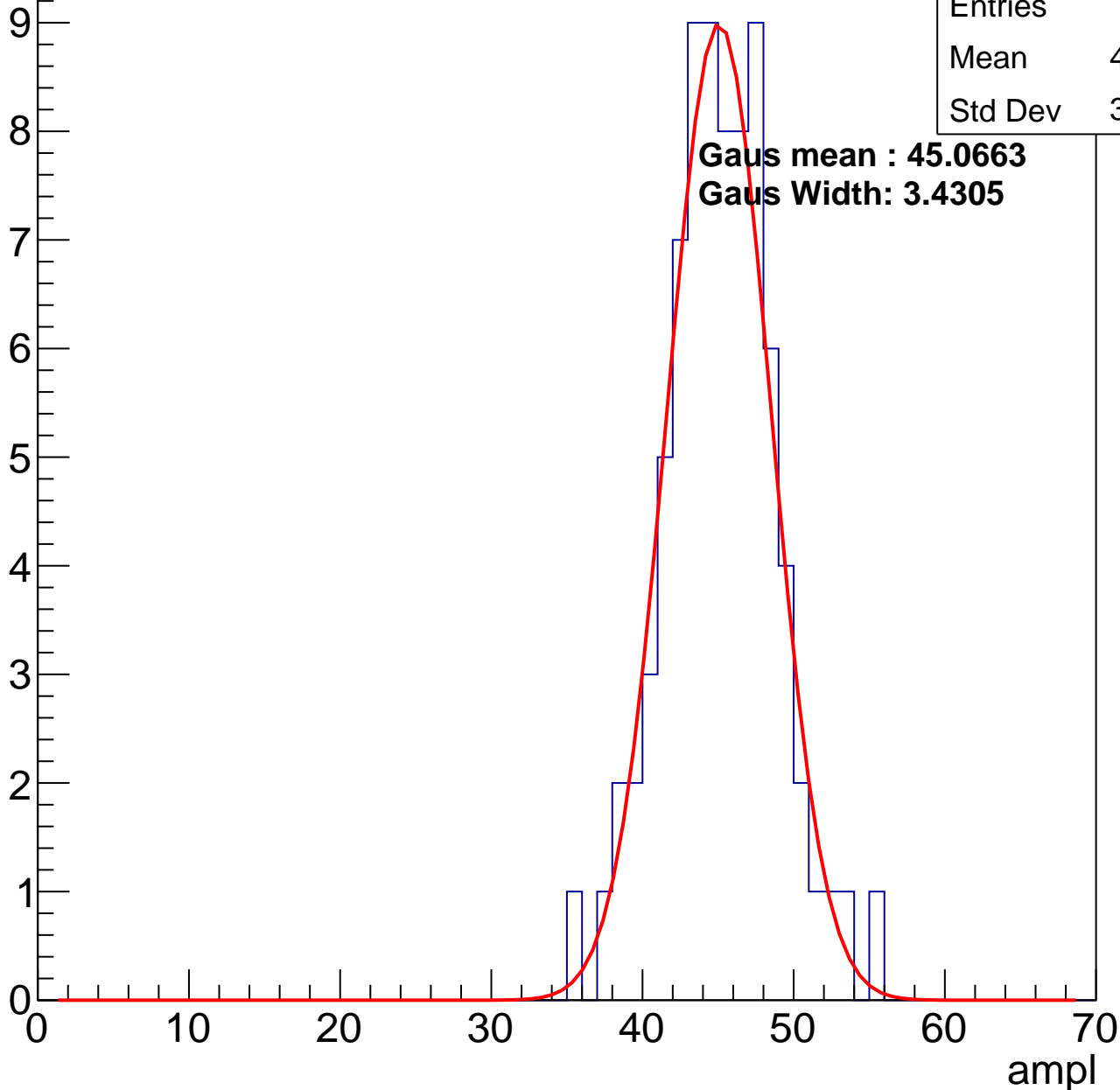
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	80
Mean	44.67
Std Dev	3.622

**Gaus mean : 45.0663**

**Gaus Width: 3.4305**

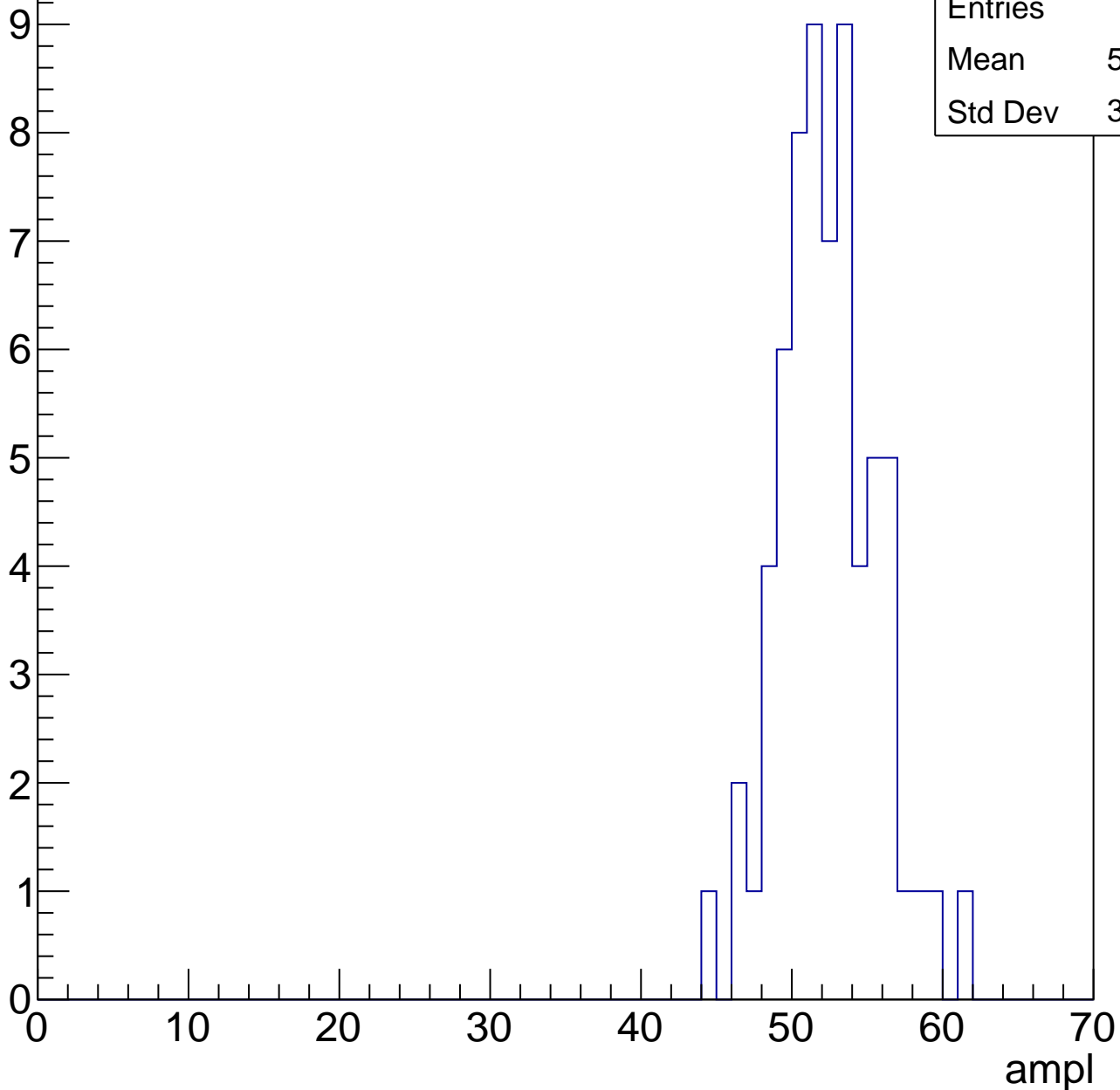


# B0L001S, U24-ch45, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

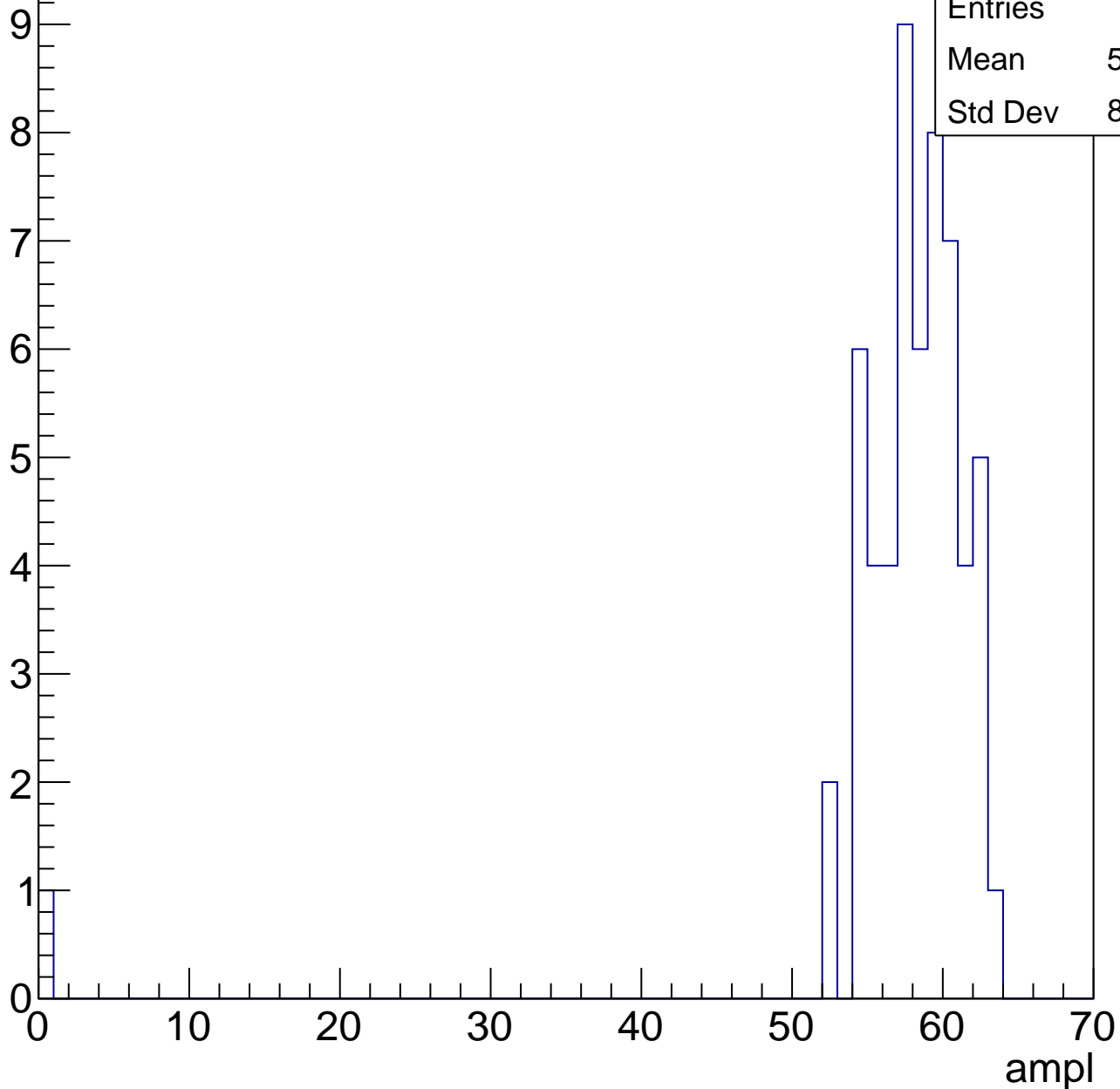
Entries	65
Mean	51.92
Std Dev	3.188



# B0L001S, U24-ch45, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

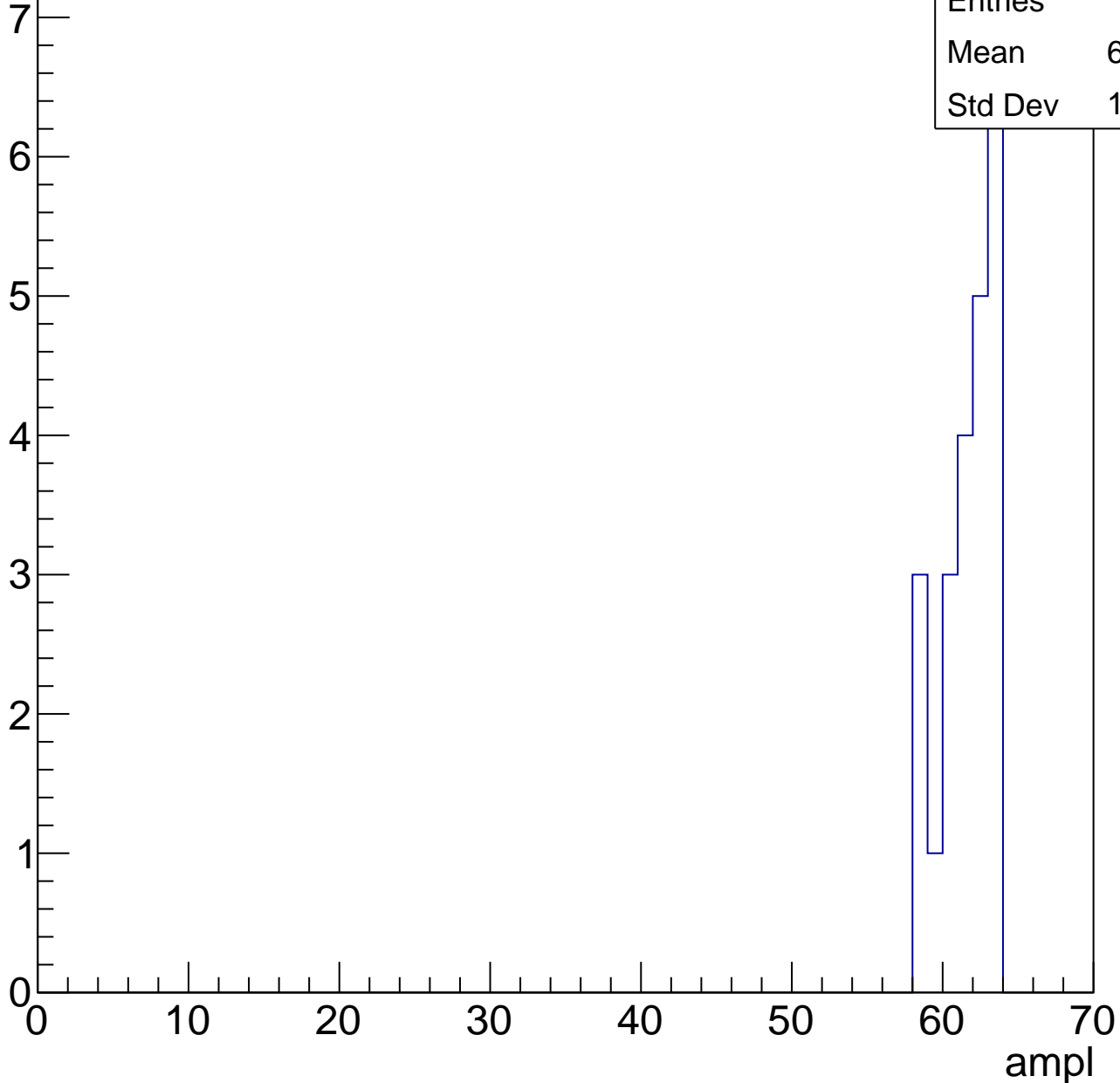


# B0L001S, U24-ch45, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

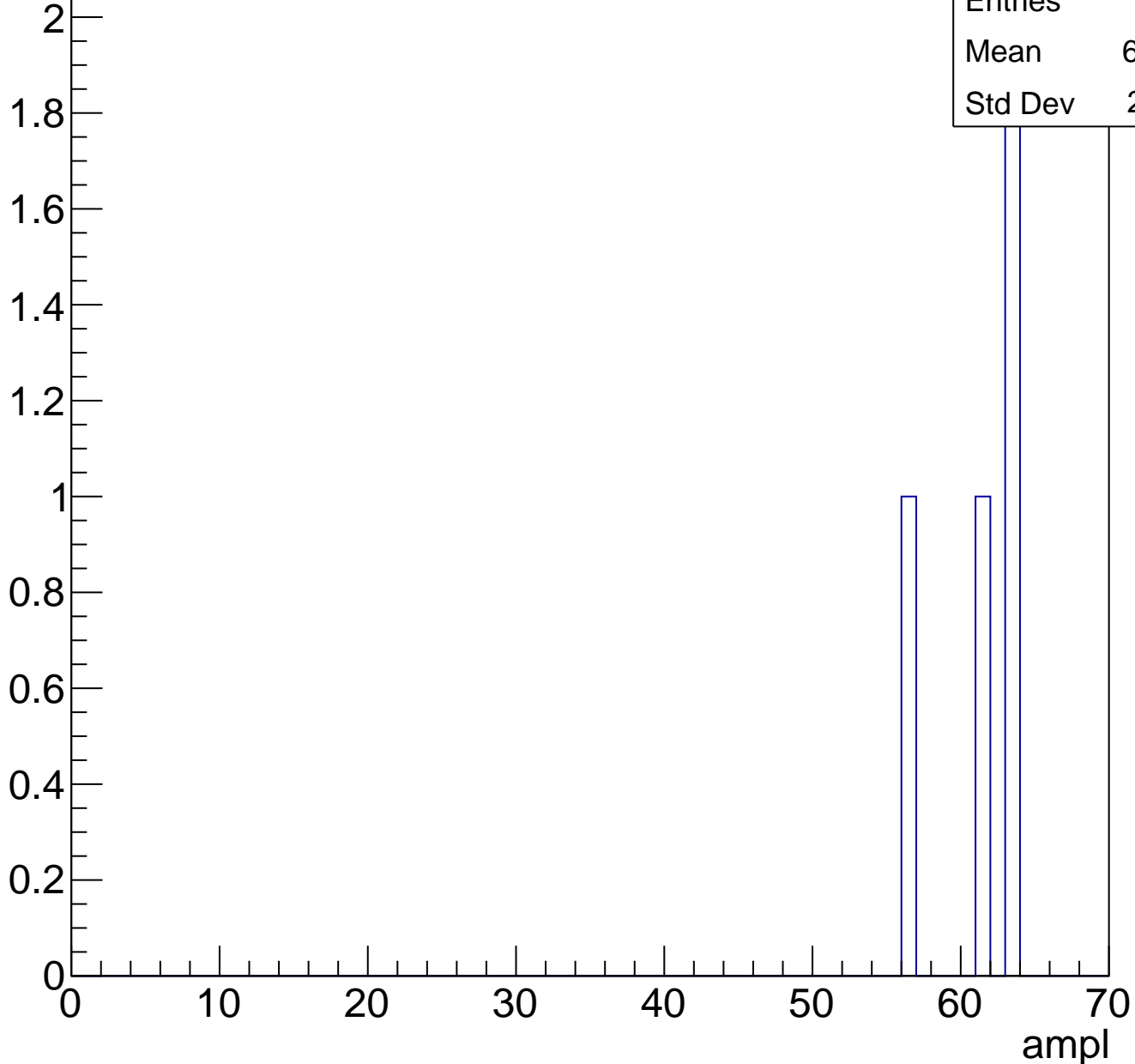
Entries	23
Mean	61.22
Std Dev	1.693



# B0L001S, U24-ch45, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch45, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U24-ch46, adc0

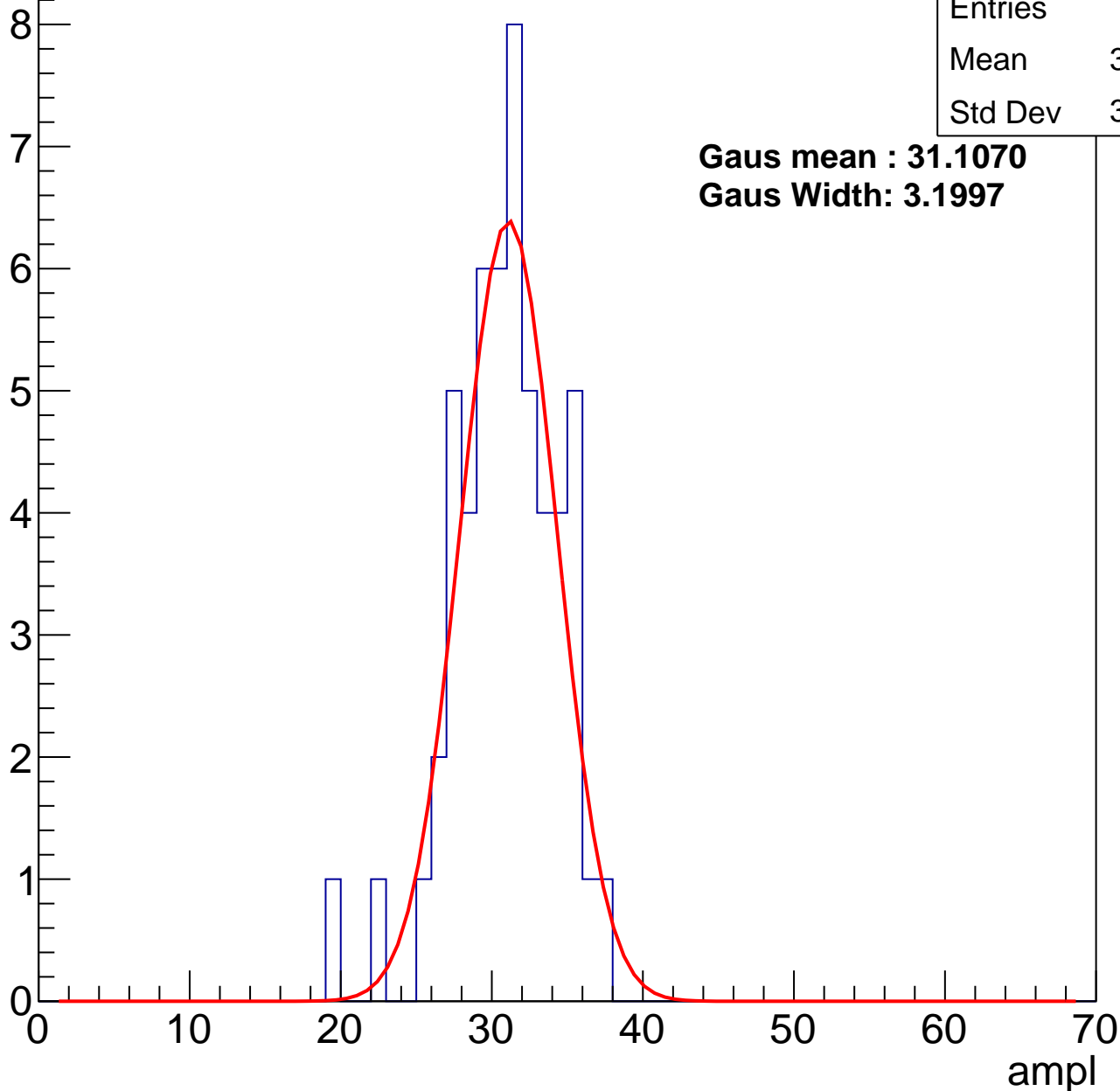
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	30.43
Std Dev	3.435

**Gaus mean : 31.1070**

**Gaus Width: 3.1997**



# B0L001S, U24-ch46, adc1

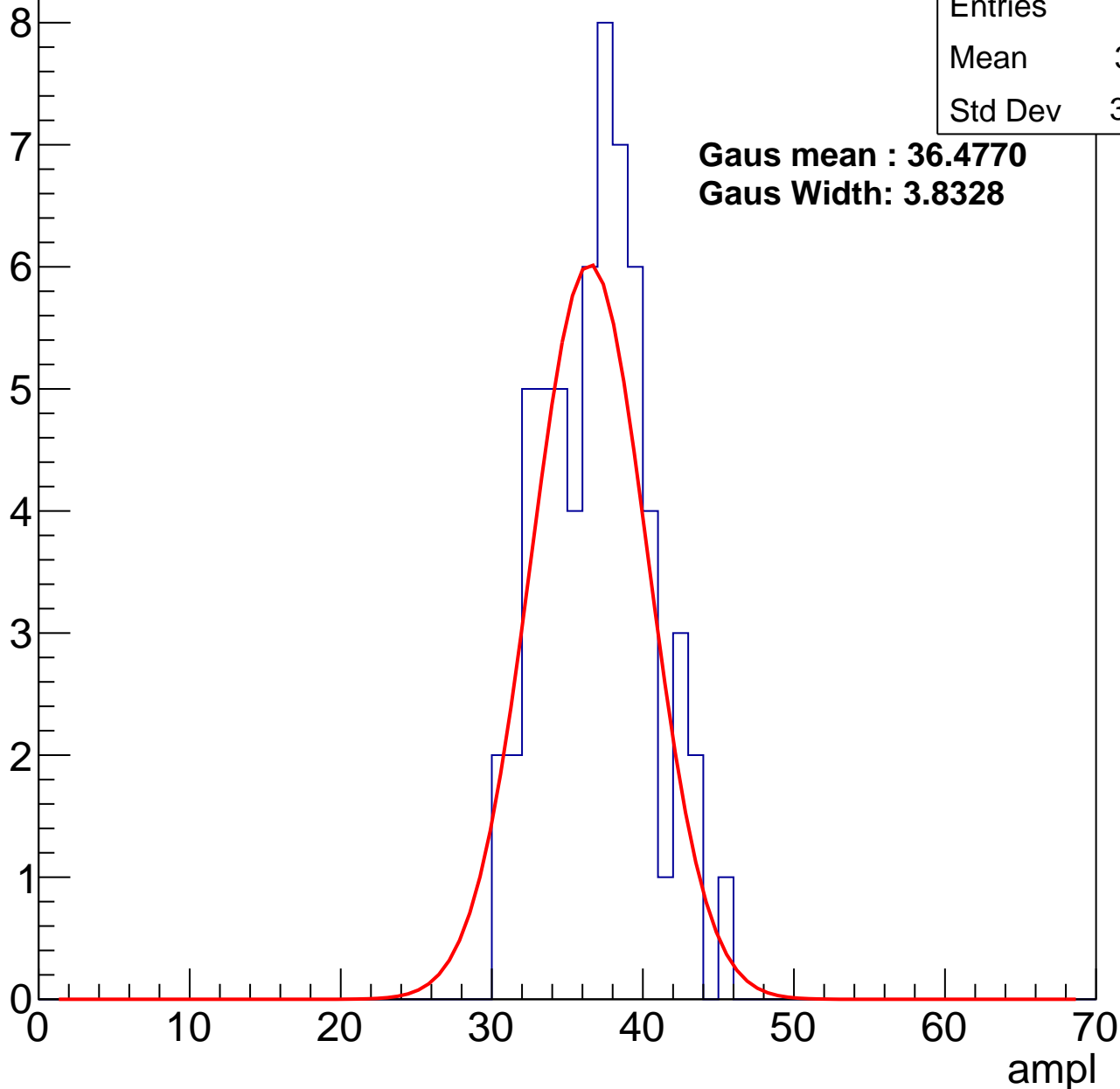
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	36.51
Std Dev	3.439

**Gaus mean : 36.4770**

**Gaus Width: 3.8328**



# B0L001S, U24-ch46, adc2

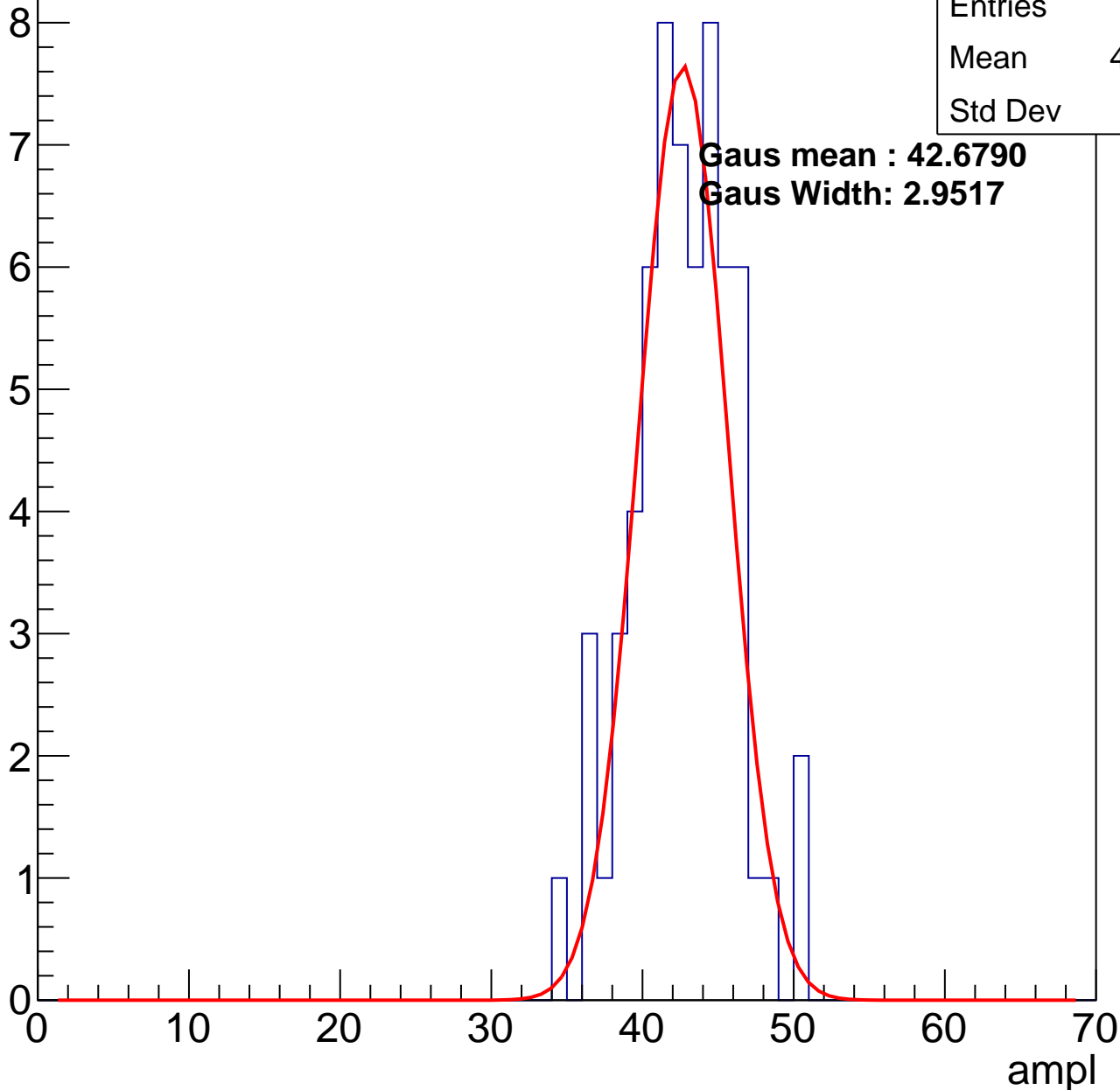
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	42.25
Std Dev	3.3

**Gaus mean : 42.6790**

**Gaus Width: 2.9517**



# B0L001S, U24-ch46, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

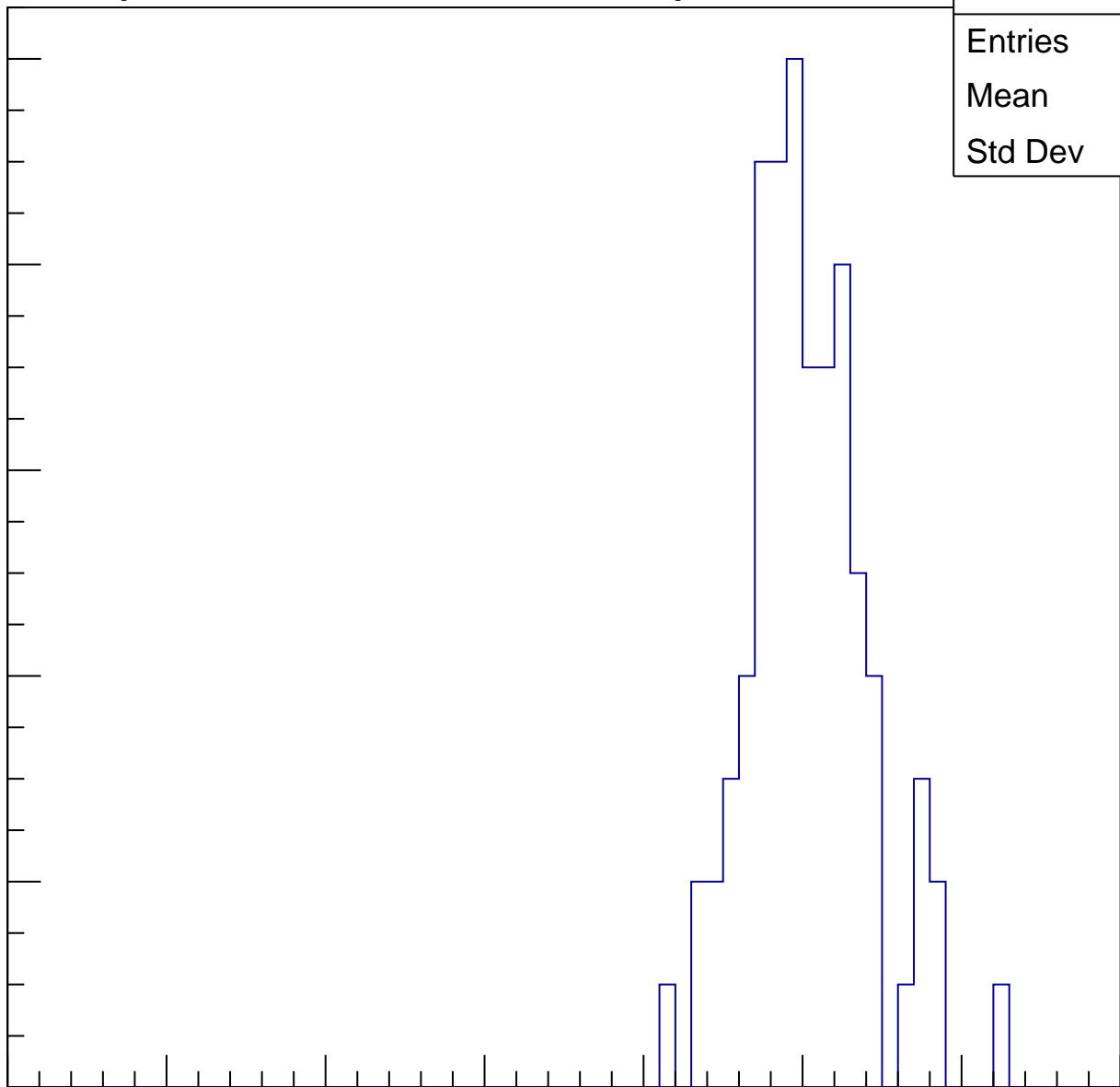
Entries	78
Mean	49.85
Std Dev	3.786

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

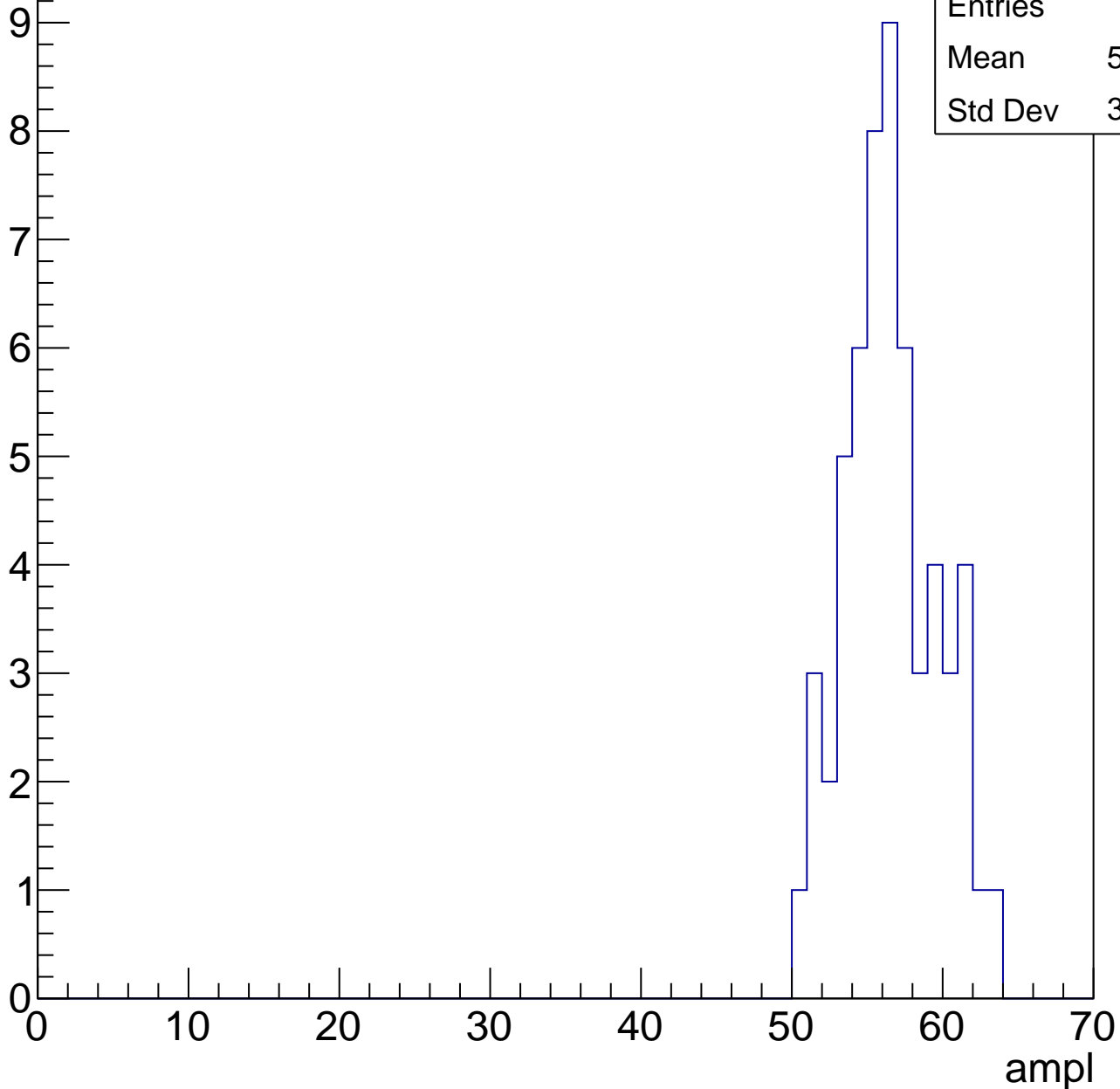


# B0L001S, U24-ch46, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	56.09
Std Dev	3.008

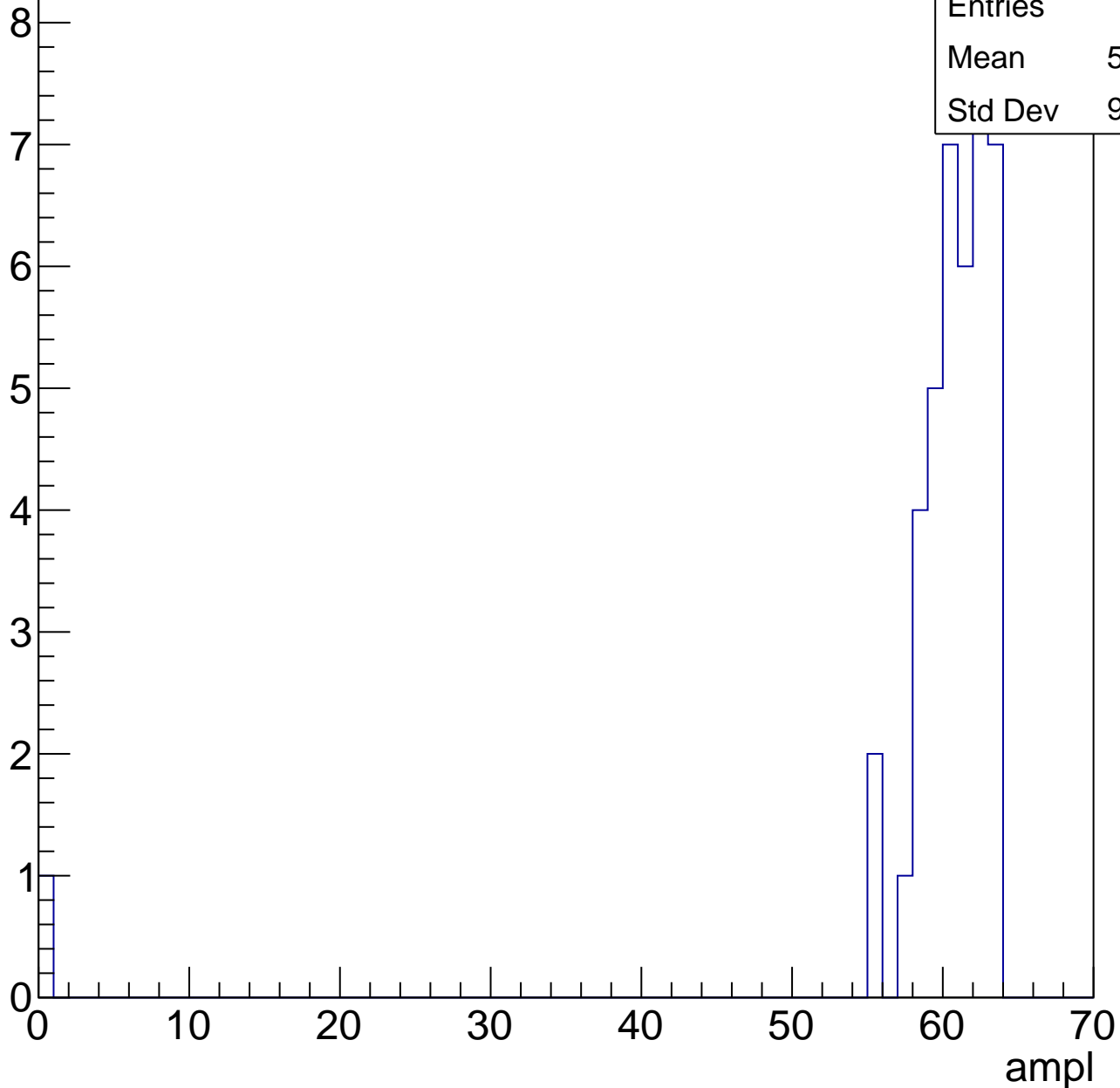


# B0L001S, U24-ch46, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

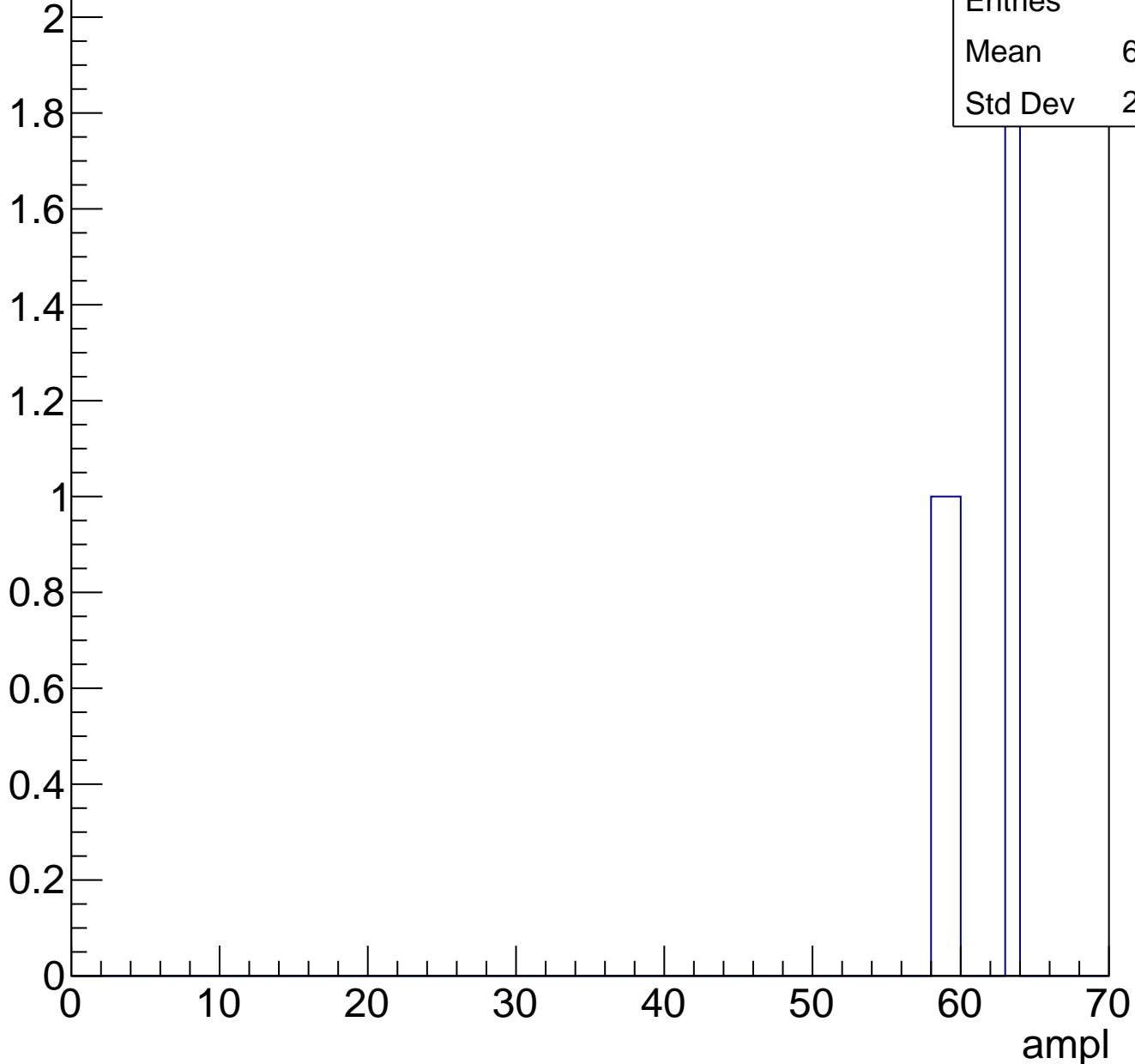
Entries	41
Mean	58.95
Std Dev	9.546



# B0L001S, U24-ch46, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch46, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U24-ch47, adc0

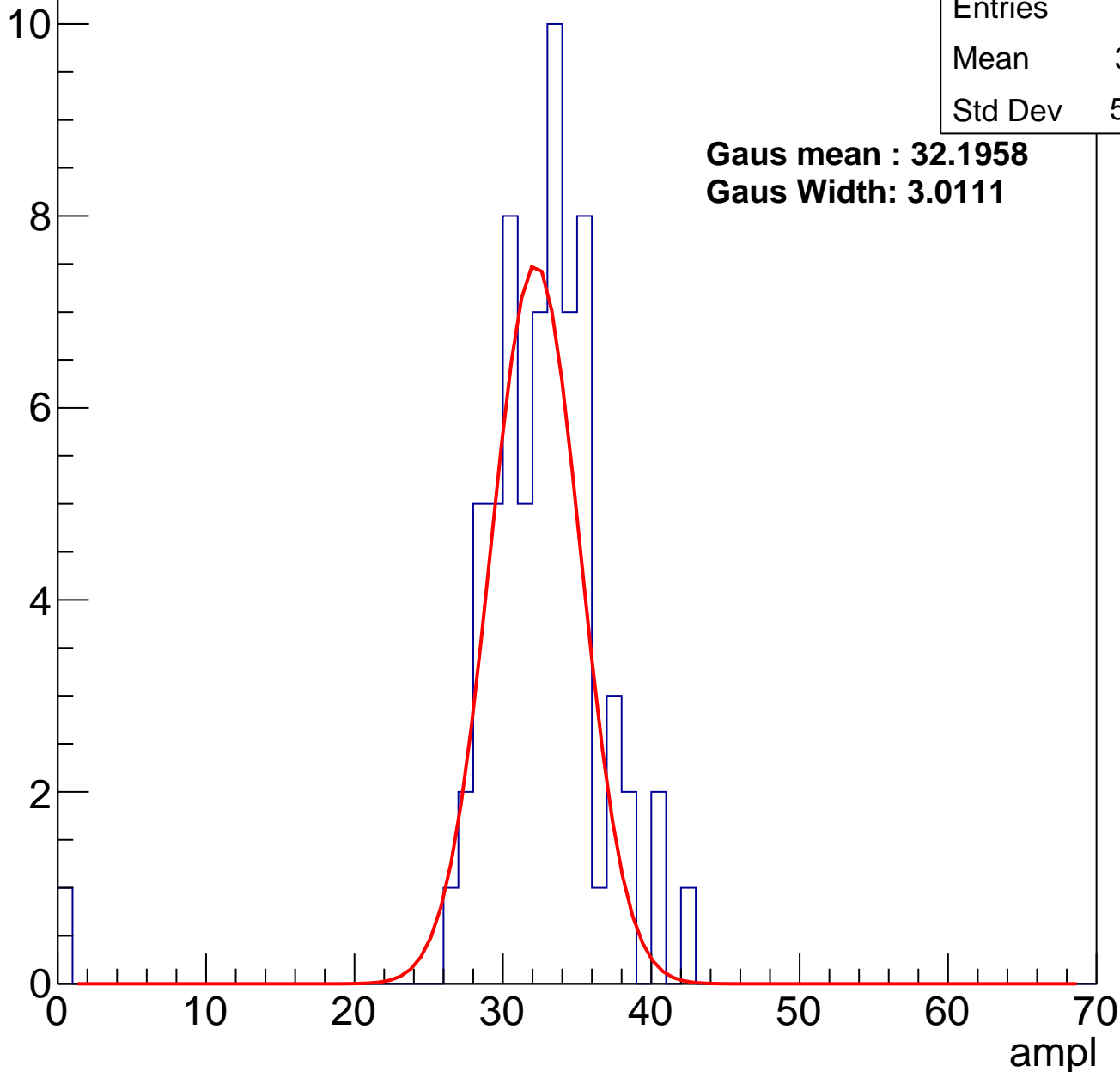
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	68
Mean	32.01
Std Dev	5.106

**Gaus mean : 32.1958**

**Gaus Width: 3.0111**

Entry



# B0L001S, U24-ch47, adc1

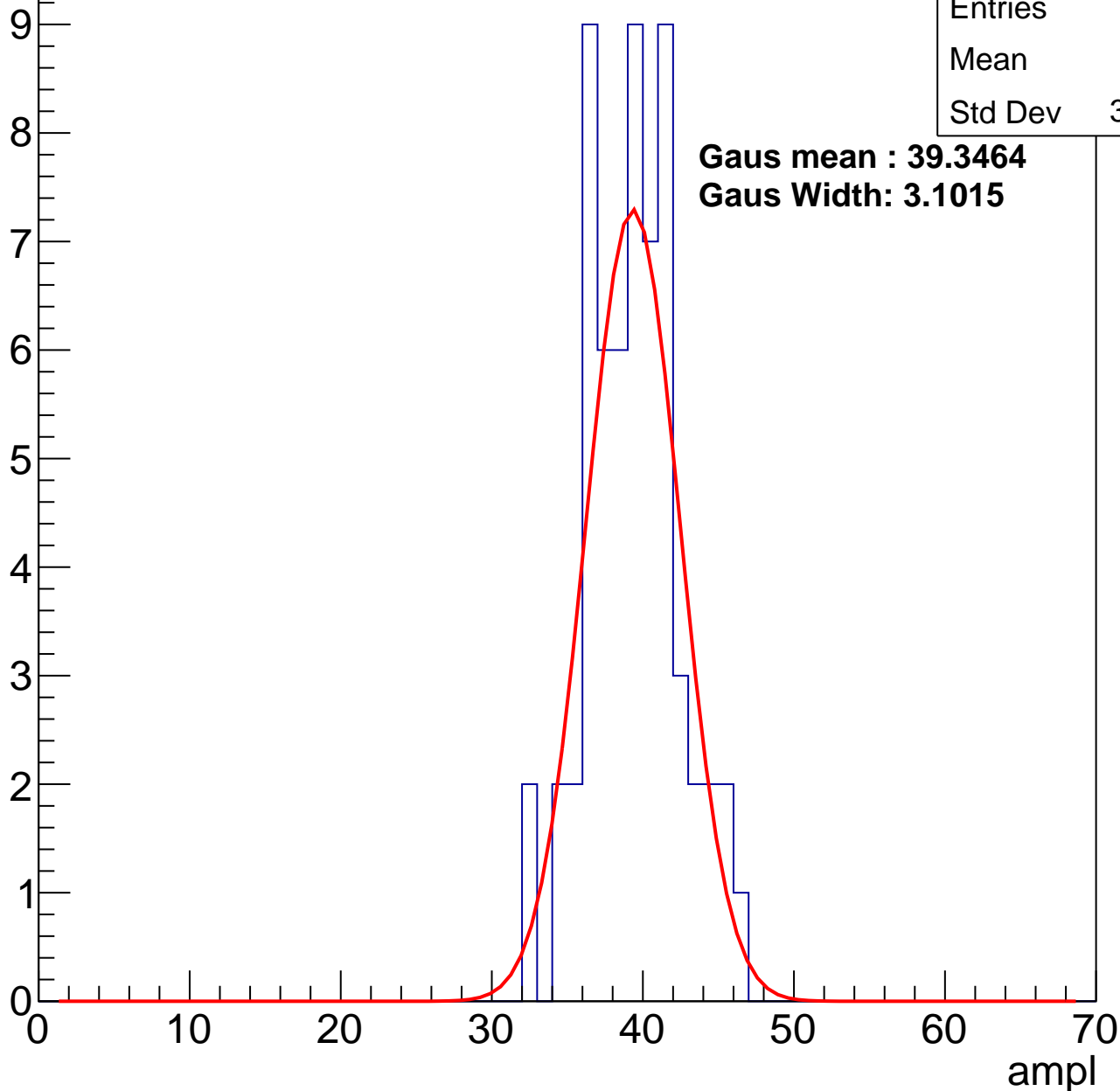
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	38.9
Std Dev	3.015

**Gaus mean : 39.3464**

**Gaus Width: 3.1015**



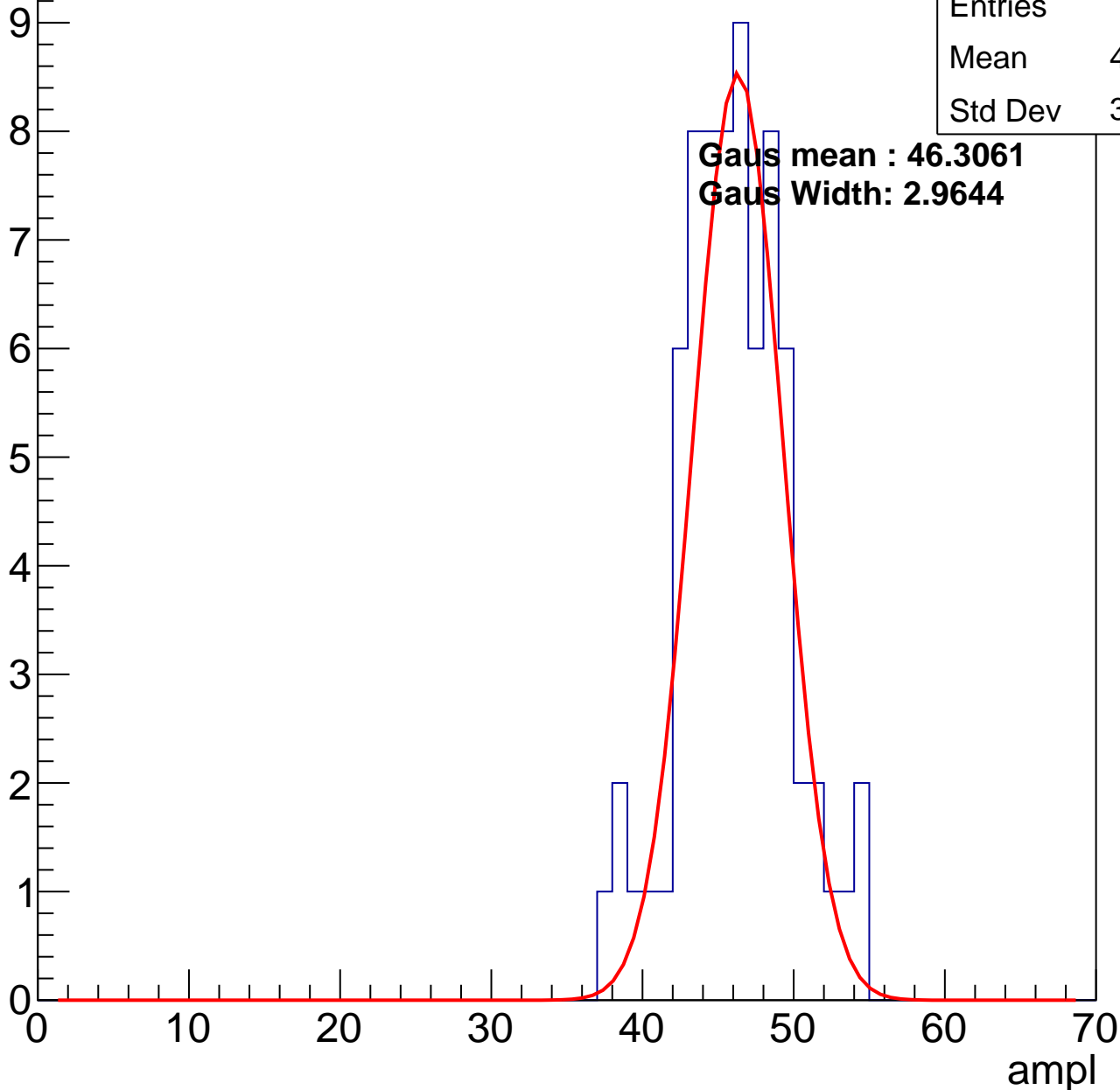
# B0L001S, U24-ch47, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	45.62
Std Dev	3.518

**Gaus mean : 46.3061**  
**Gaus Width: 2.9644**

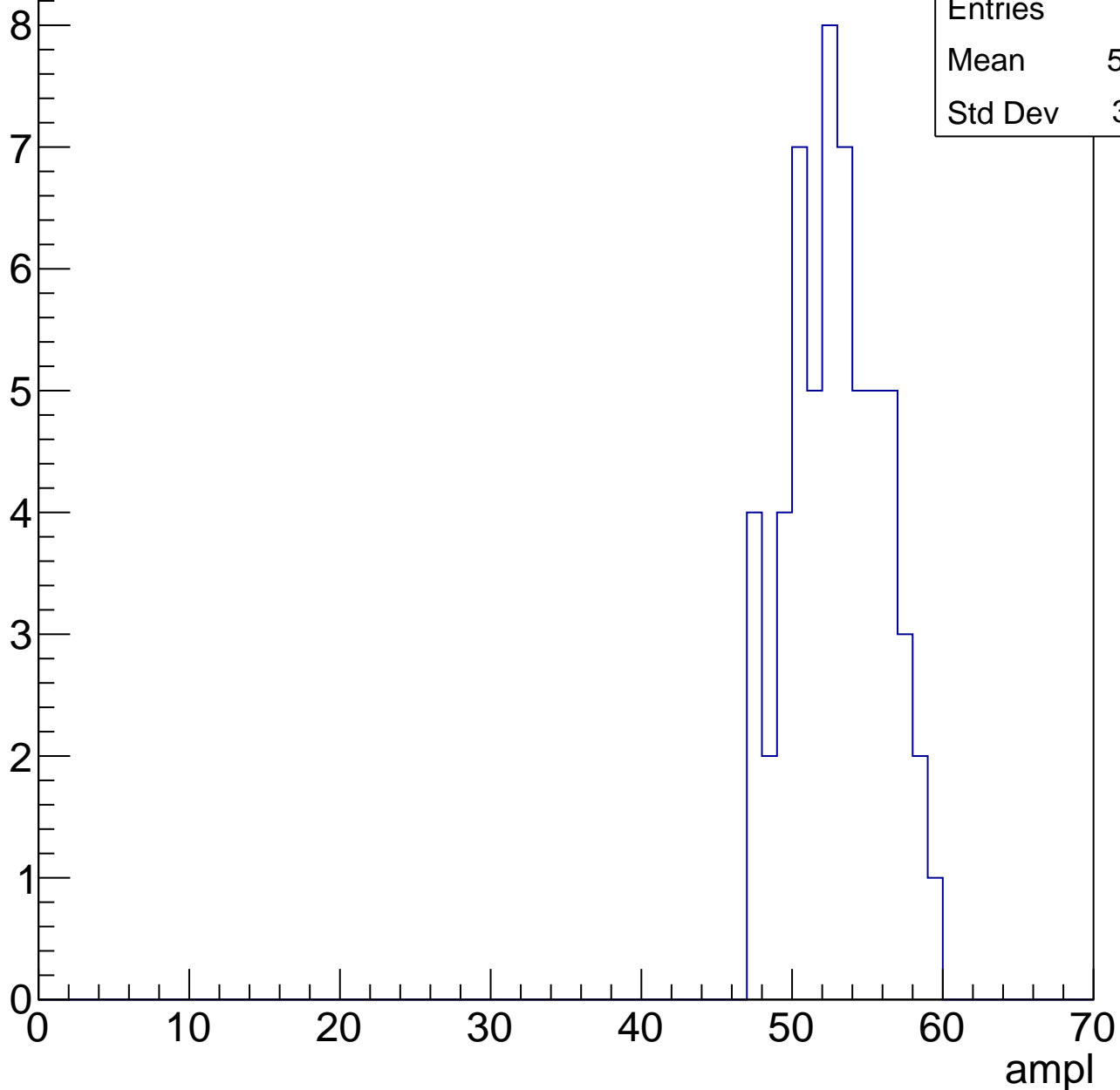


# B0L001S, U24-ch47, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

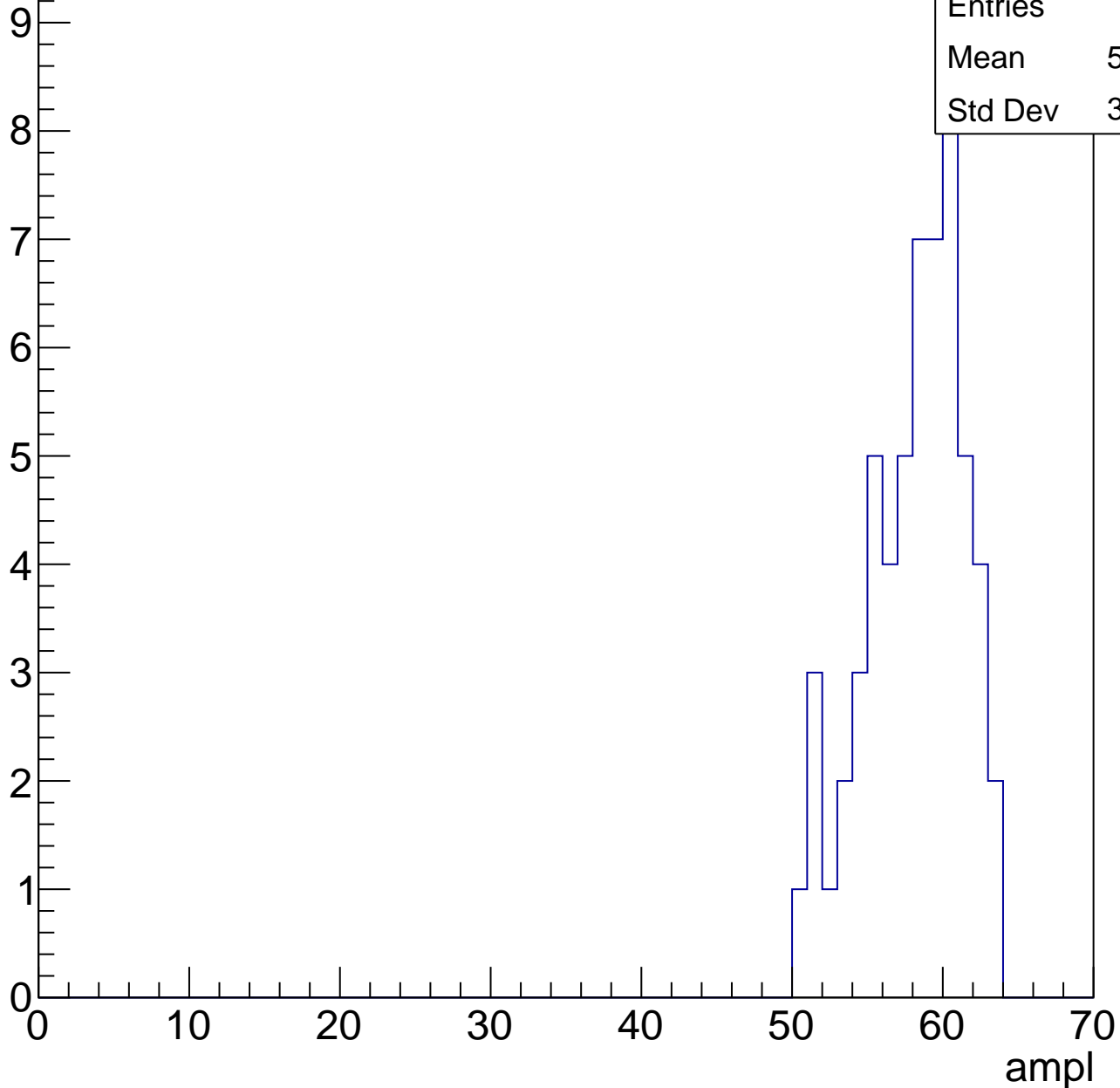
Entries	58
Mean	52.47
Std Dev	3.041



# B0L001S, U24-ch47, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

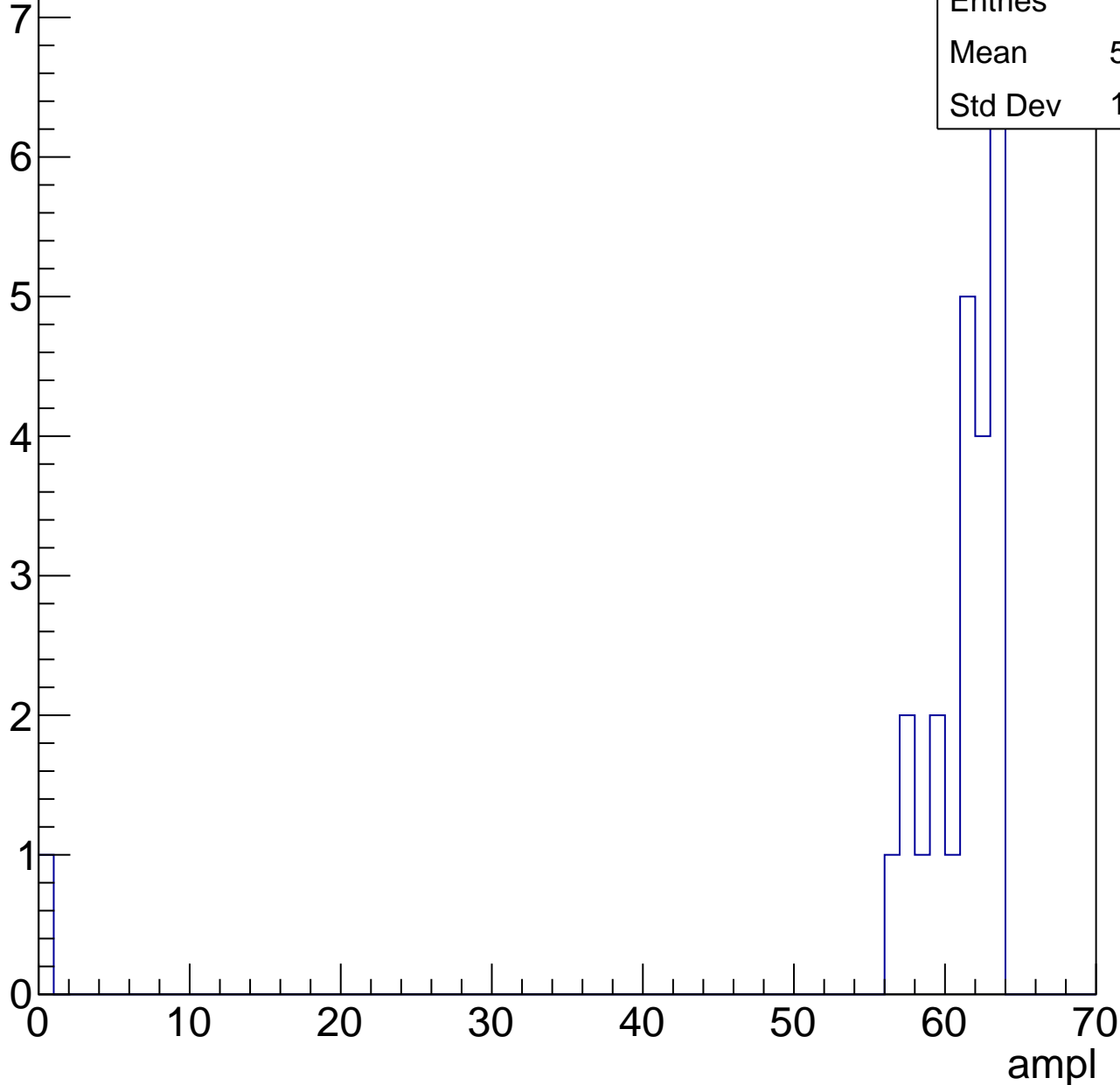


# B0L001S, U24-ch47, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	24
Mean	58.33
Std Dev	12.34



# B0L001S, U24-ch47, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.33
Std Dev	0.4714

ampl



# B0L001S, U24-ch47, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U24-ch48, adc0

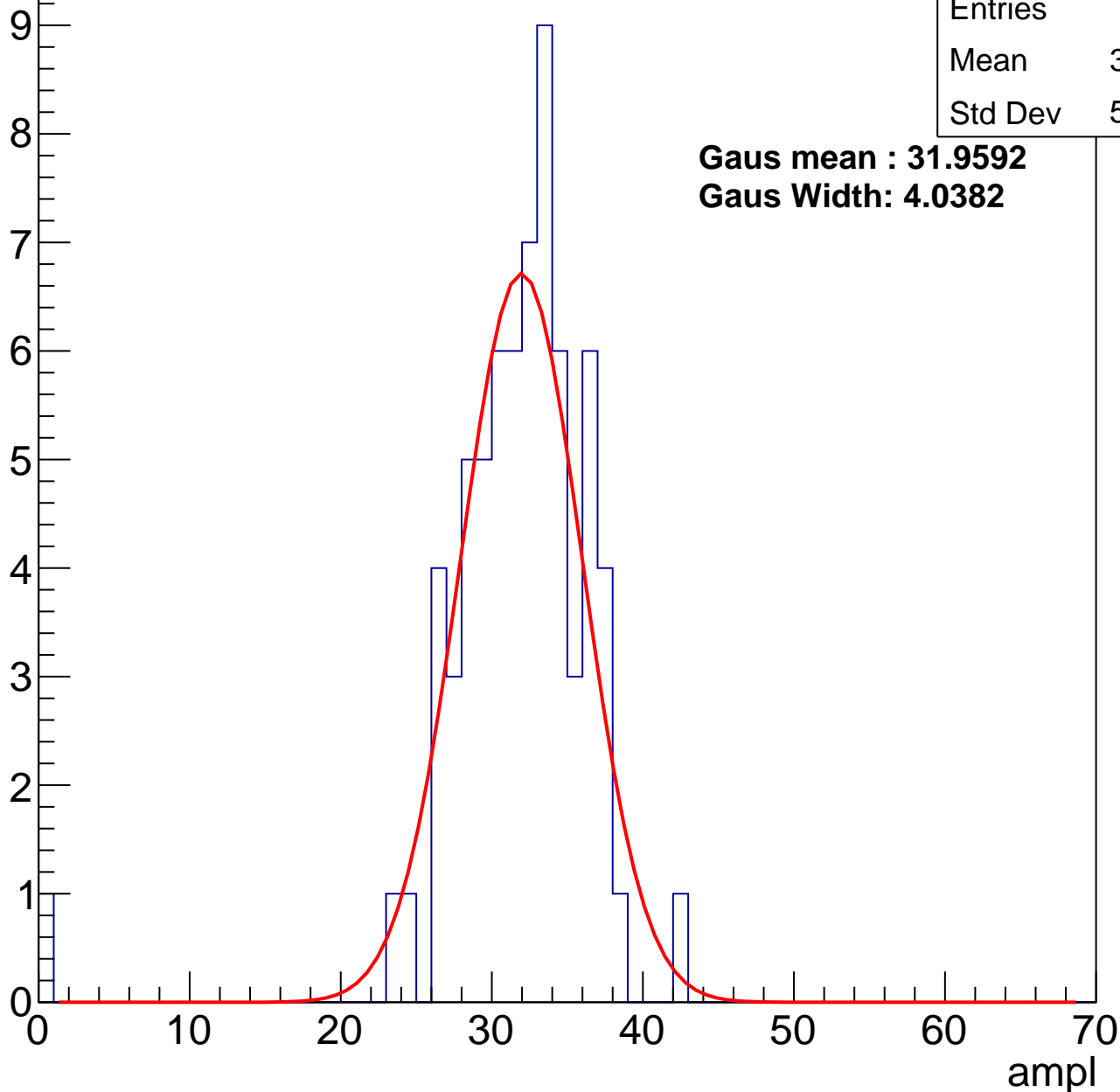
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	31.26
Std Dev	5.244

**Gaus mean : 31.9592**

**Gaus Width: 4.0382**



# B0L001S, U24-ch48, adc1

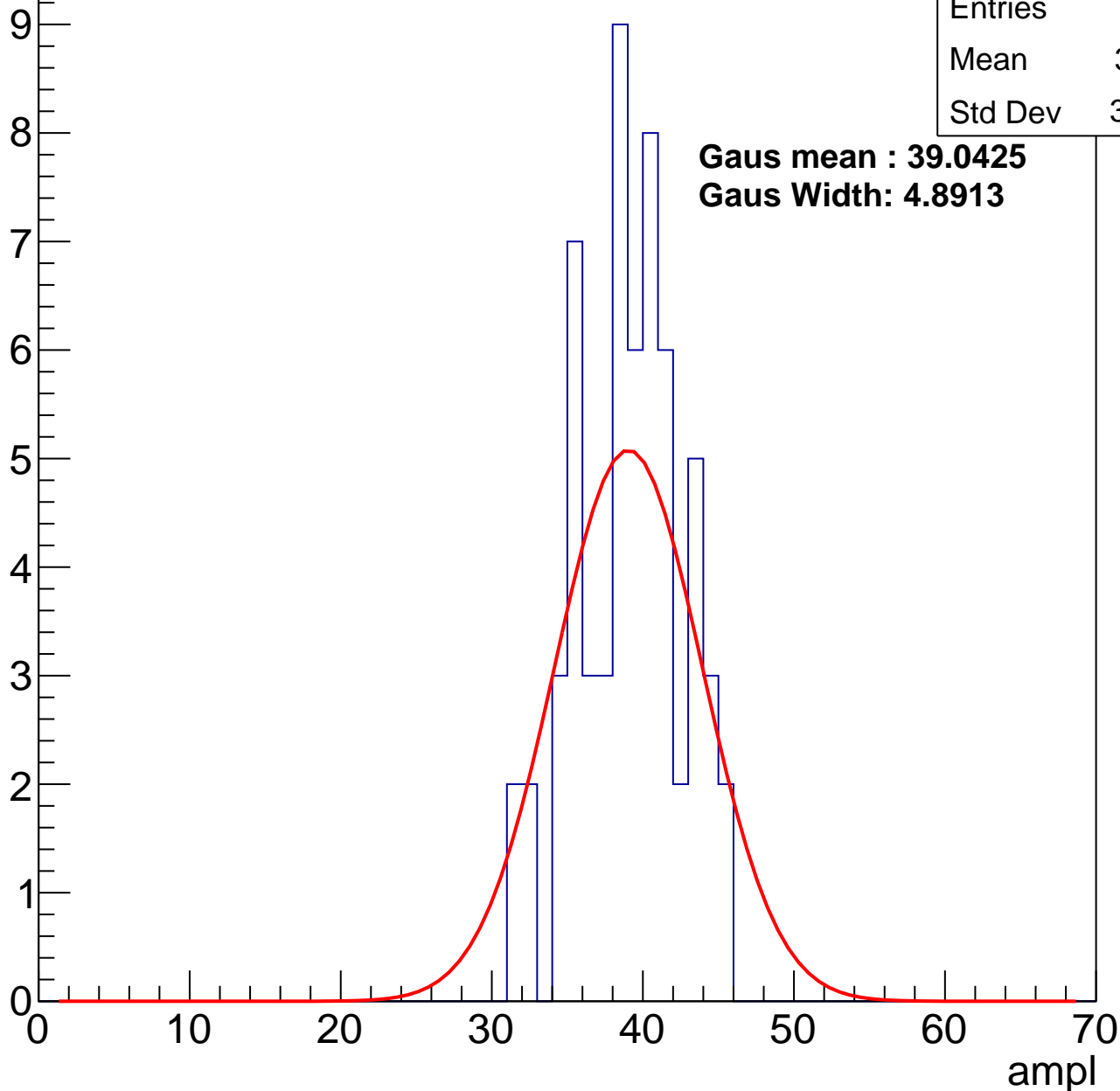
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	38.61
Std Dev	3.456

**Gaus mean : 39.0425**

**Gaus Width: 4.8913**

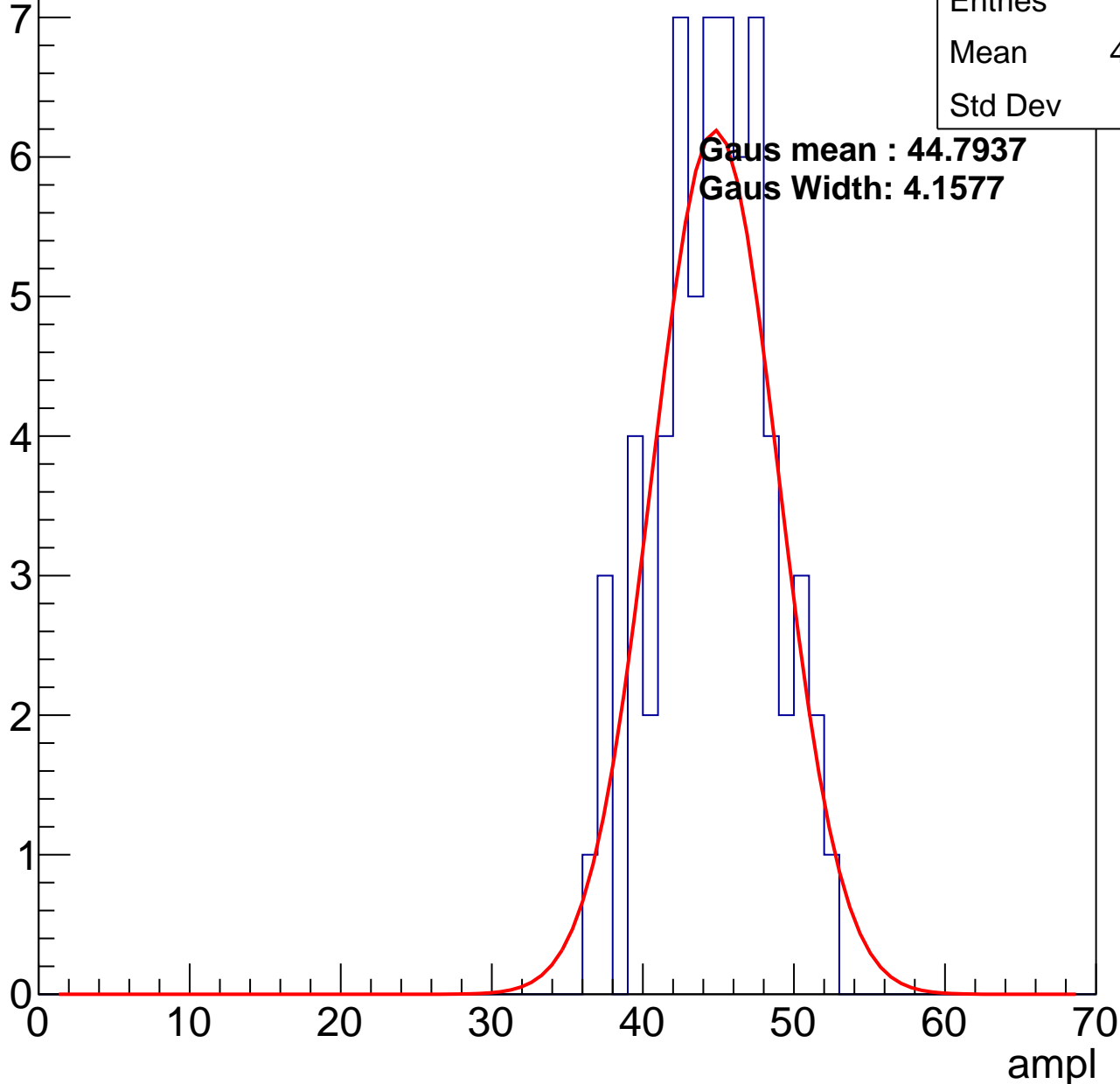


# B0L001S, U24-ch48, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	44.28
Std Dev	3.69

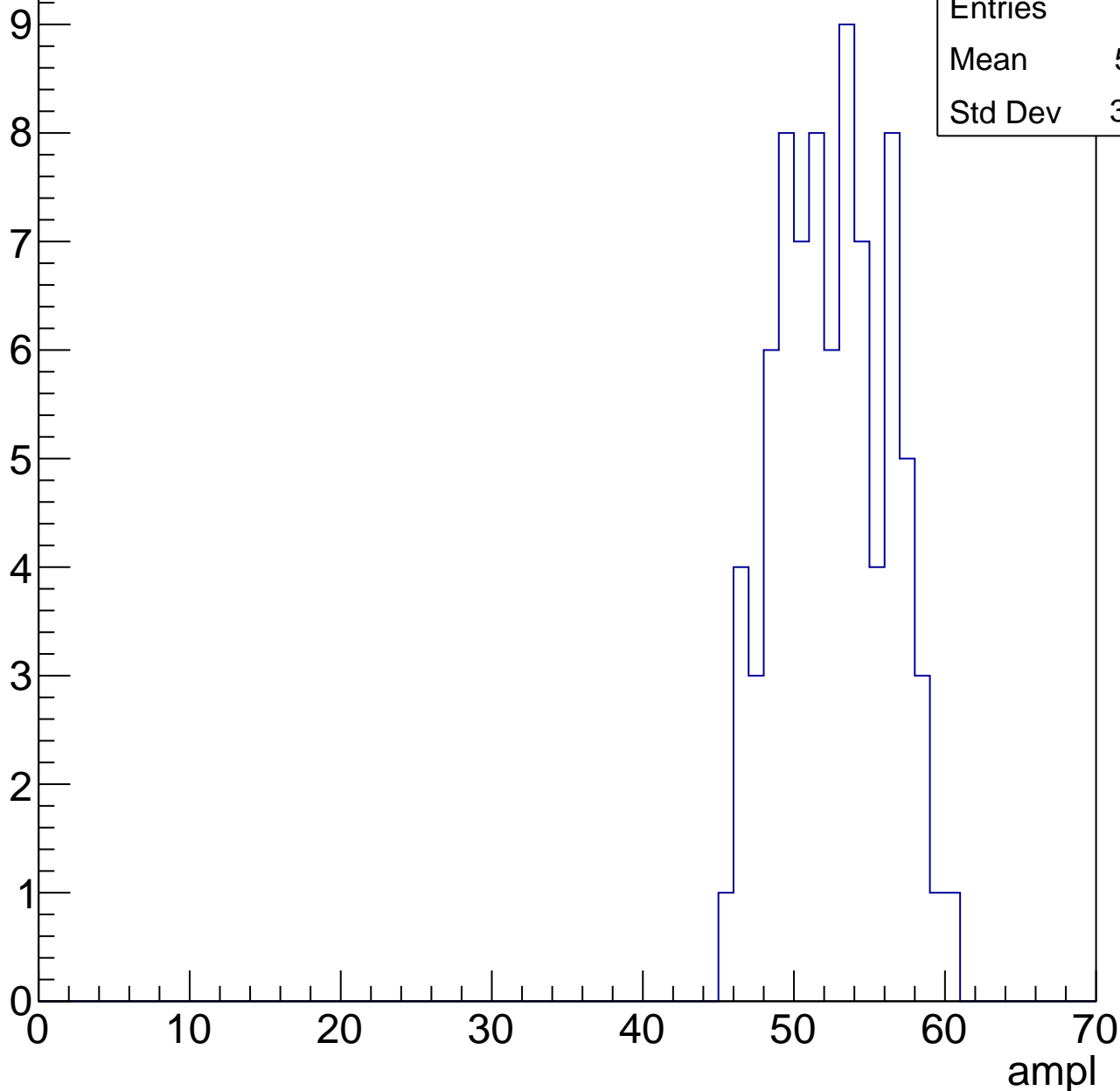


# B0L001S, U24-ch48, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

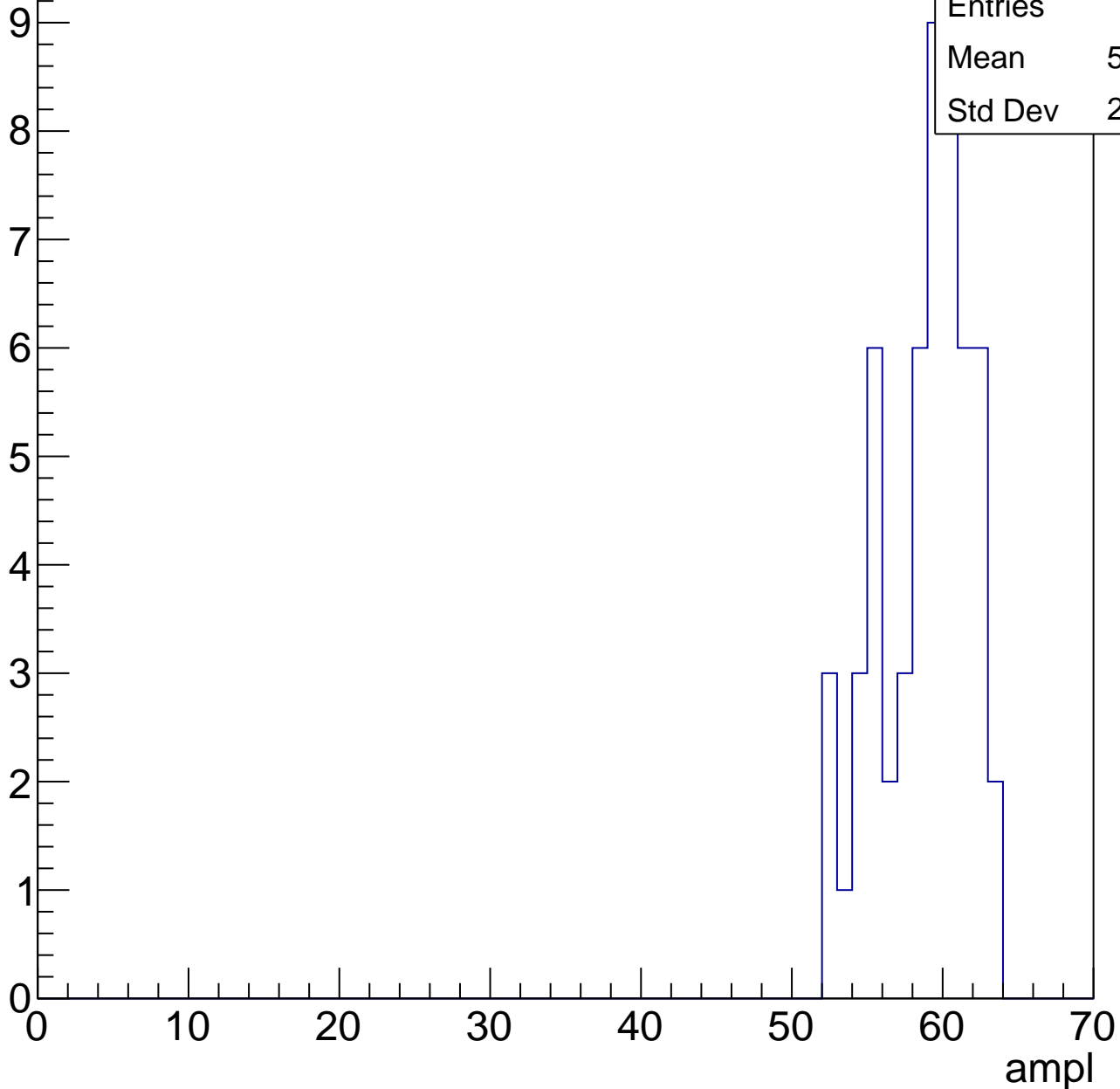
Entries	81
Mean	52.11
Std Dev	3.545



# B0L001S, U24-ch48, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

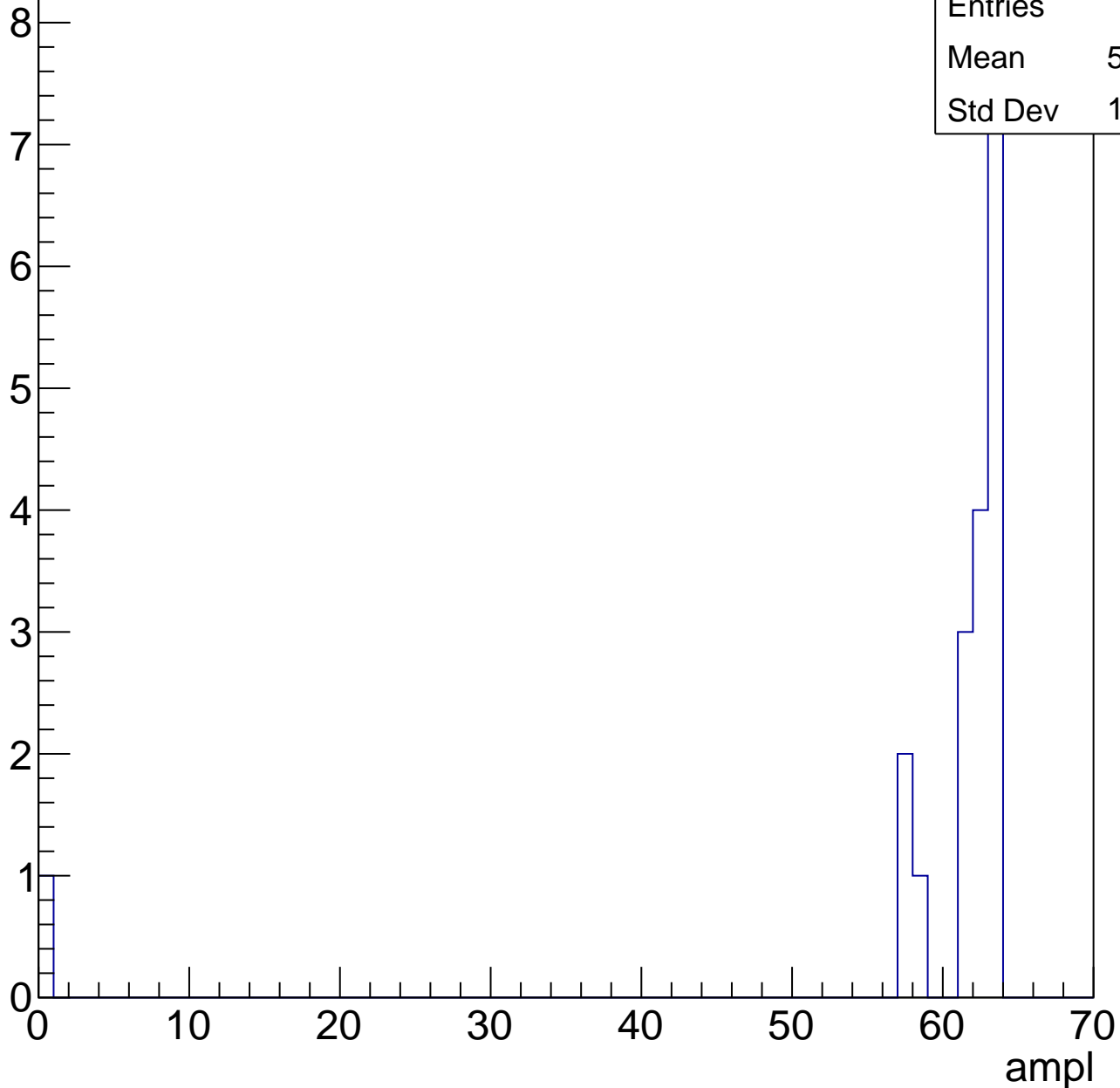


# B0L001S, U24-ch48, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	19
Mean	58.26
Std Dev	13.87



# B0L001S, U24-ch48, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch48, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U24-ch49, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	71
Mean	31.39
Std Dev	3.437

**Gaus mean : 31.9286**

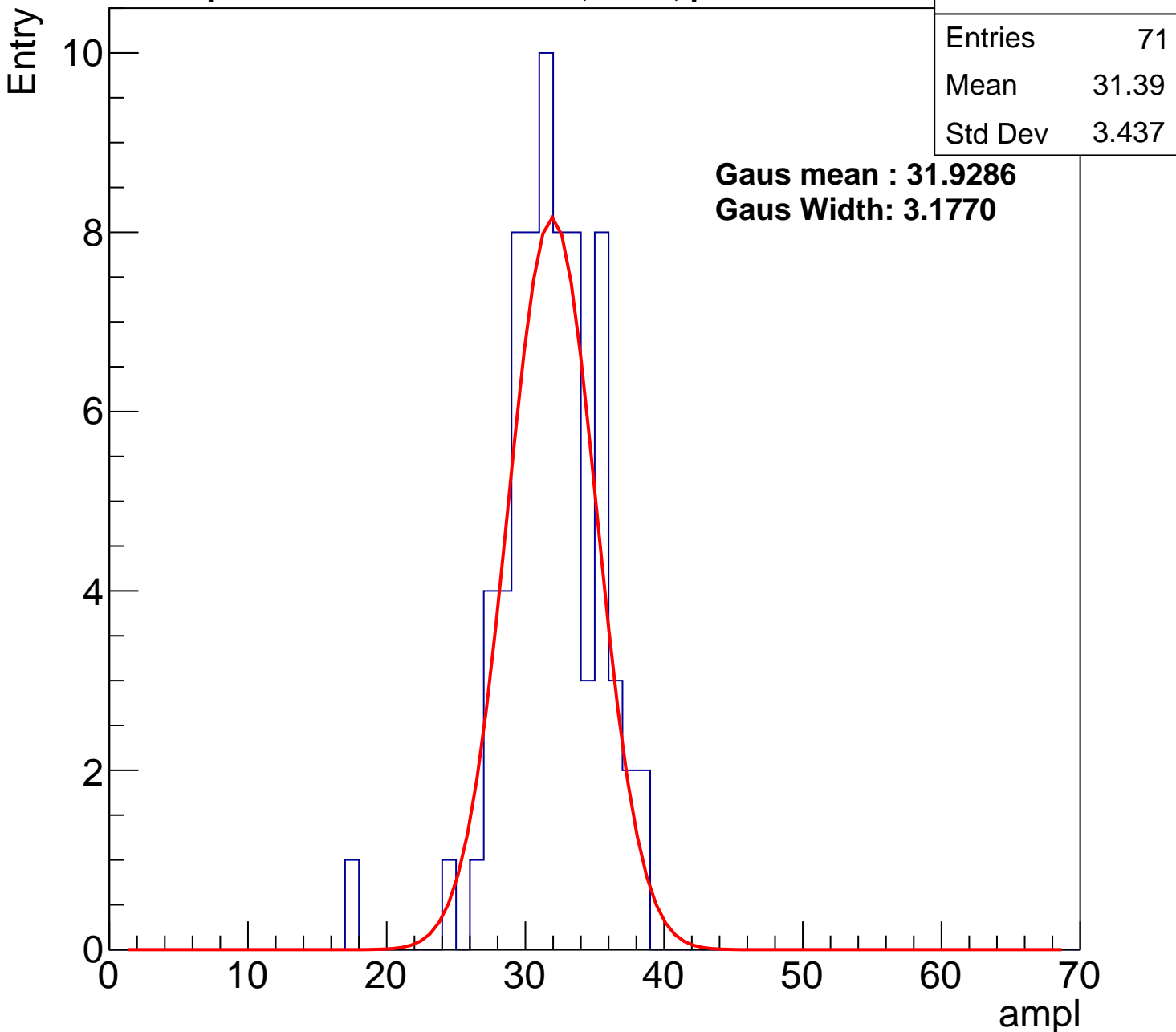
**Gaus Width: 3.1770**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U24-ch49, adc1

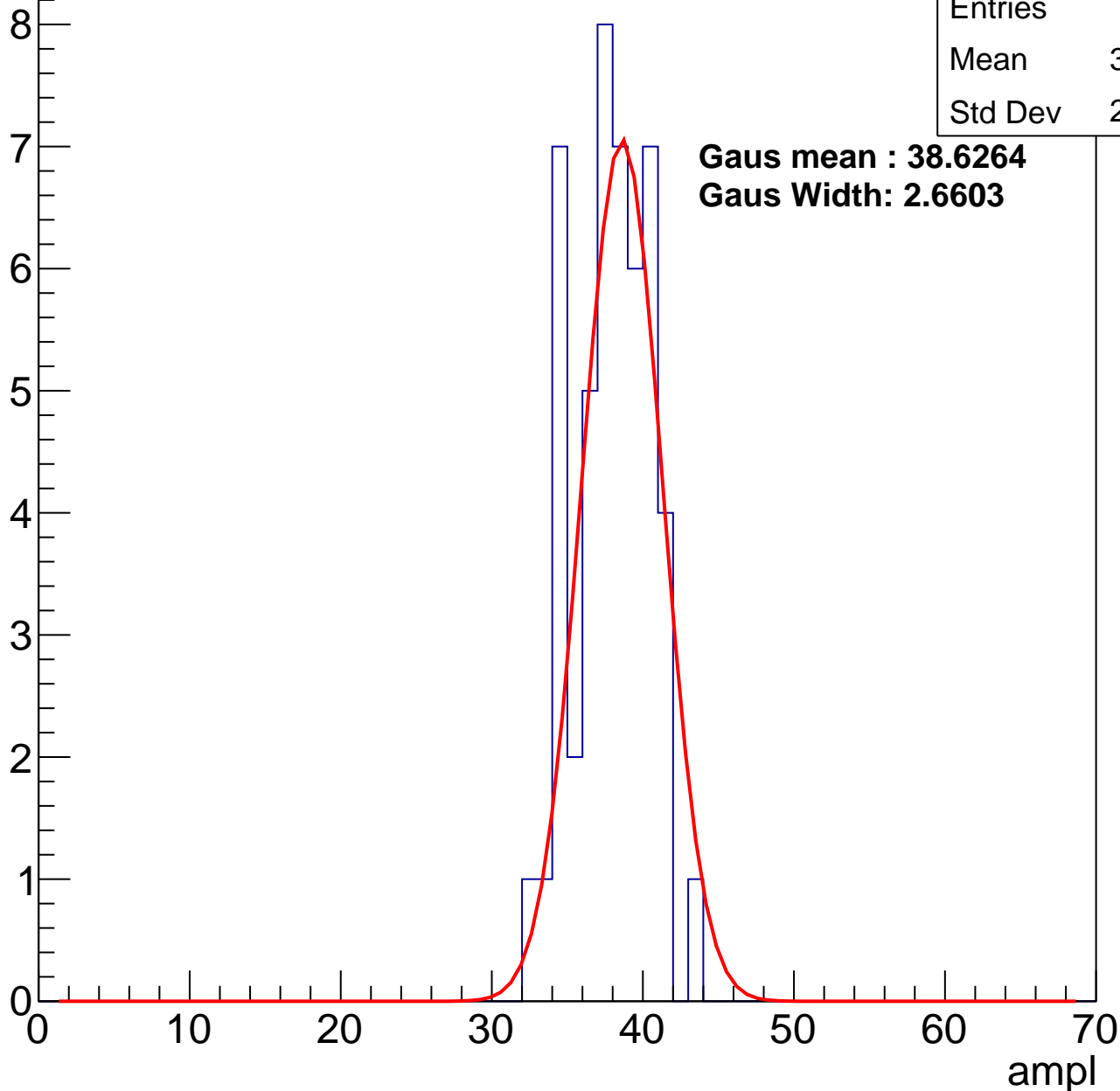
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	49
Mean	37.47
Std Dev	2.475

**Gaus mean : 38.6264**

**Gaus Width: 2.6603**



# B0L001S, U24-ch49, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	78
Mean	44.05
Std Dev	3.297

**Gaus mean : 44.6222**

**Gaus Width: 3.2847**

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

70

ampl

0

2

4

6

8

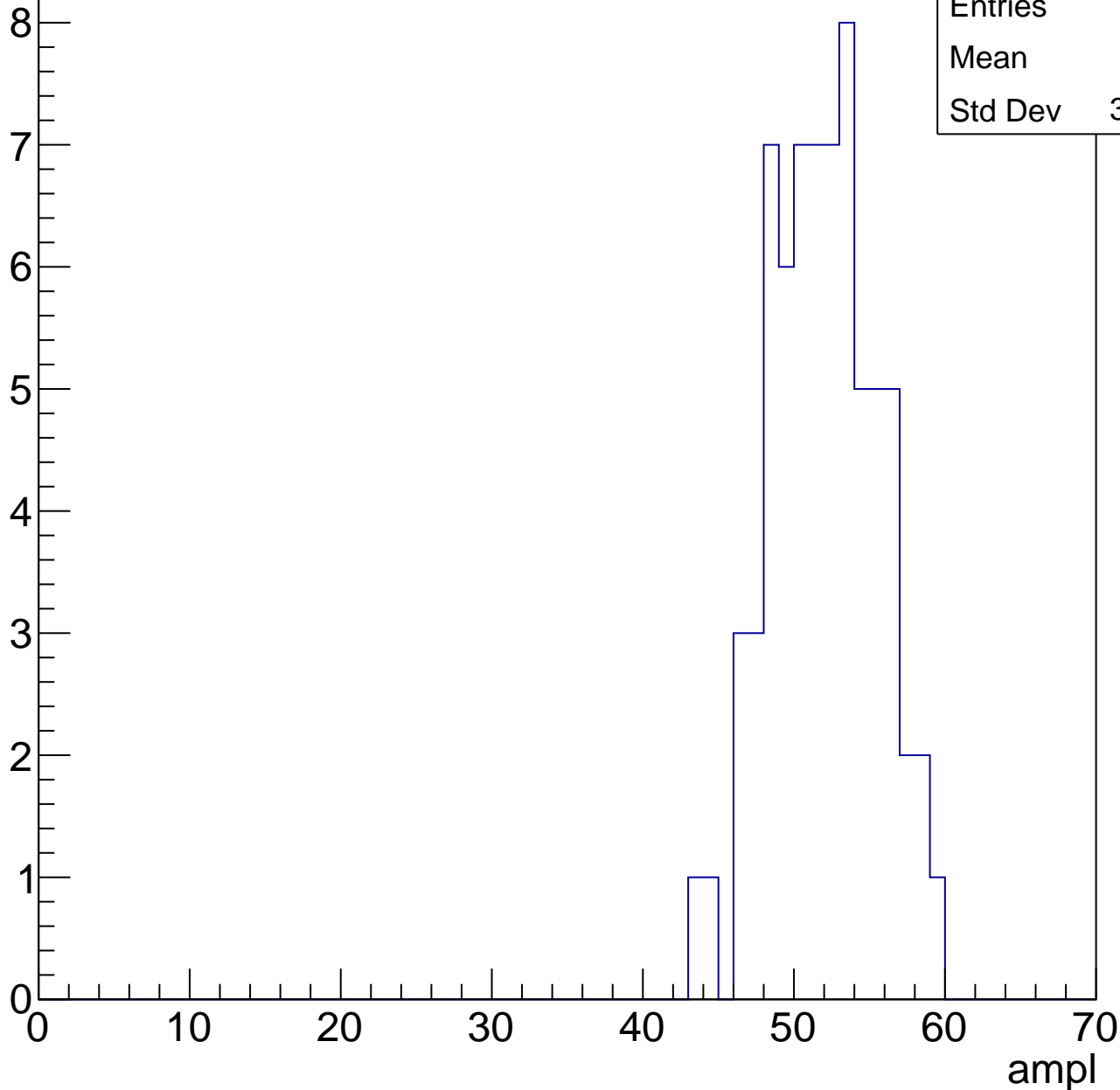
10

# B0L001S, U24-ch49, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	51.5
Std Dev	3.455

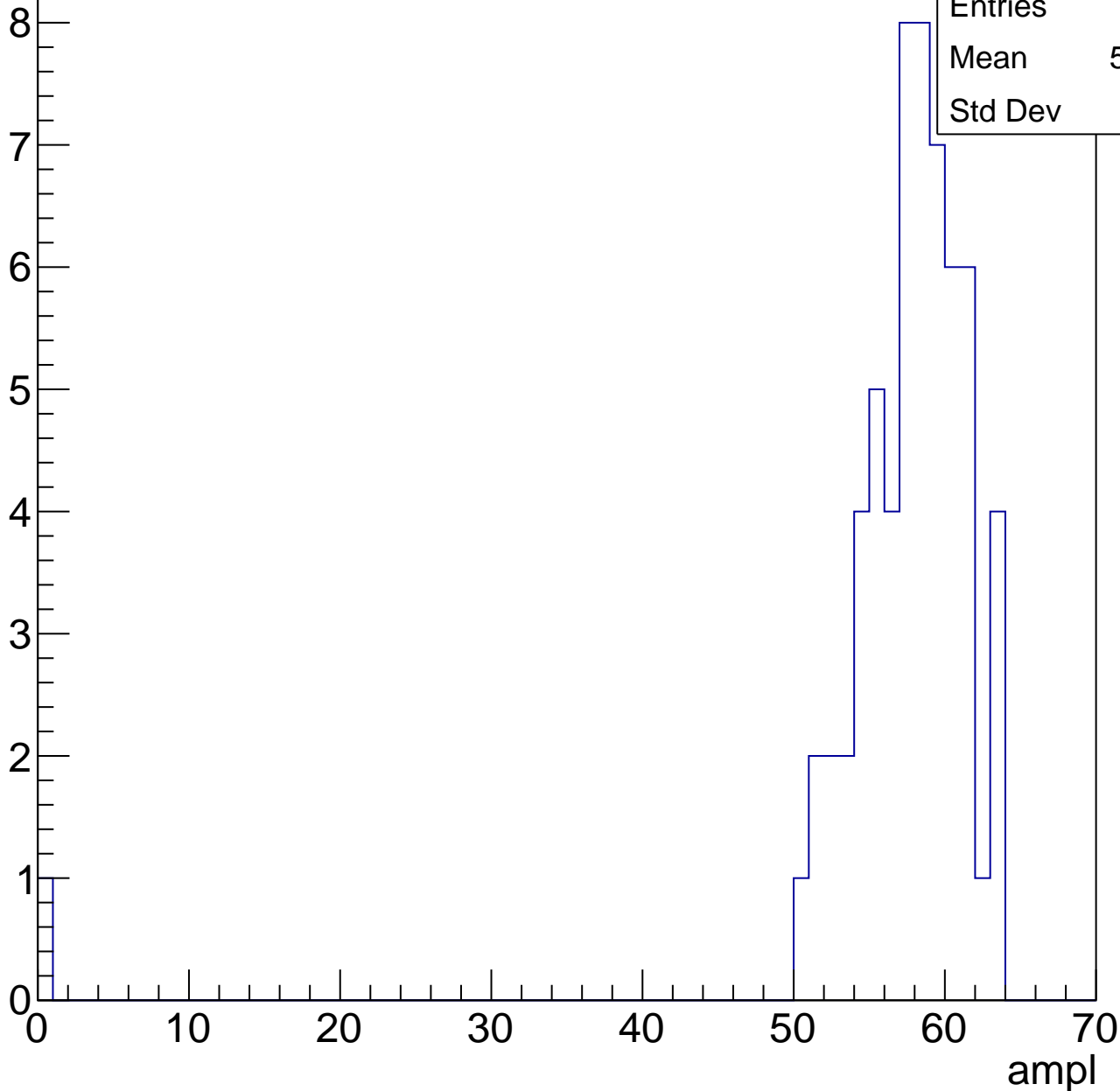


# B0L001S, U24-ch49, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	56.56
Std Dev	7.95

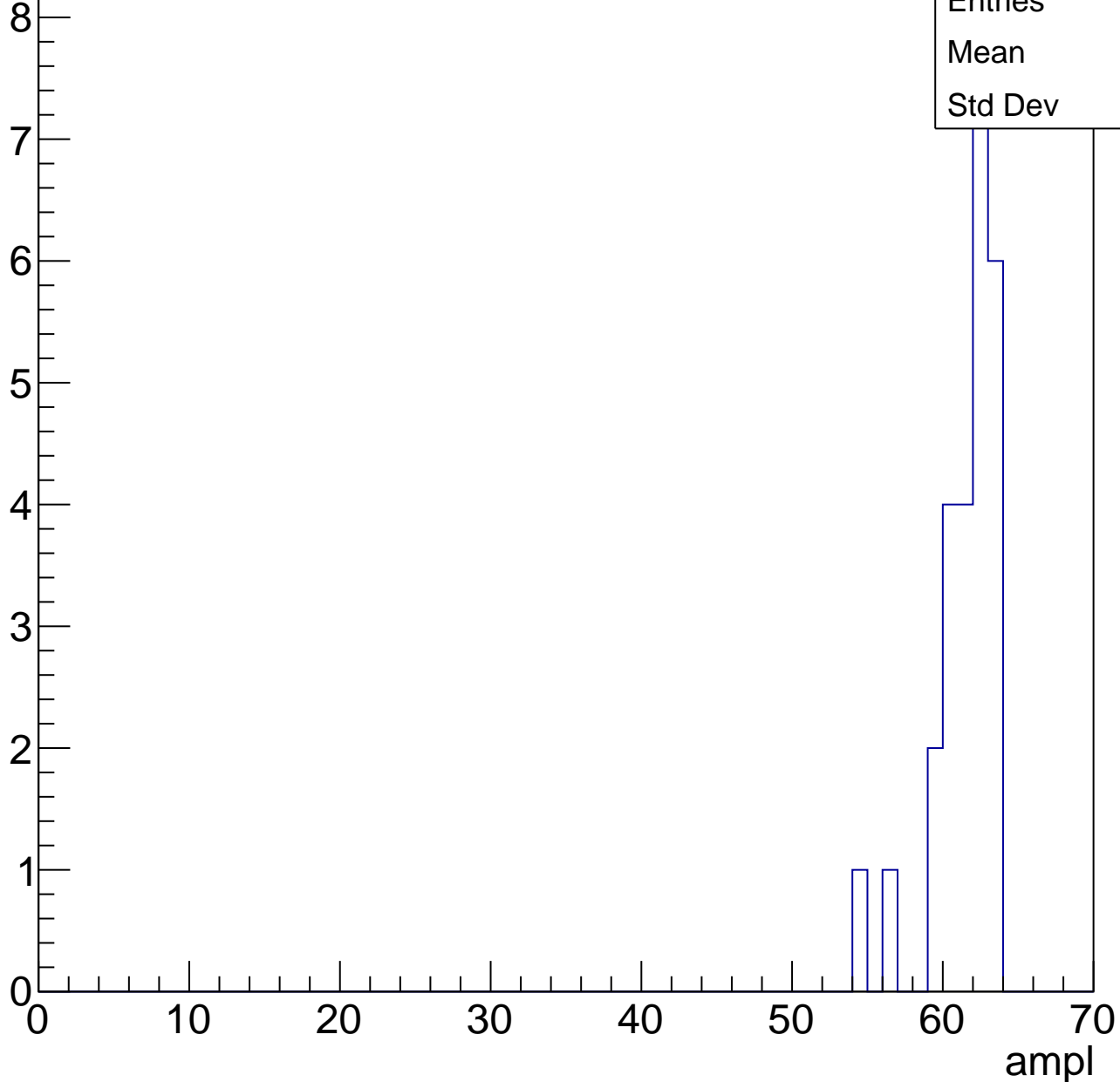


# B0L001S, U24-ch49, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	26
Mean	61
Std Dev	2.13



# B0L001S, U24-ch49, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch49, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U24-ch50, adc0

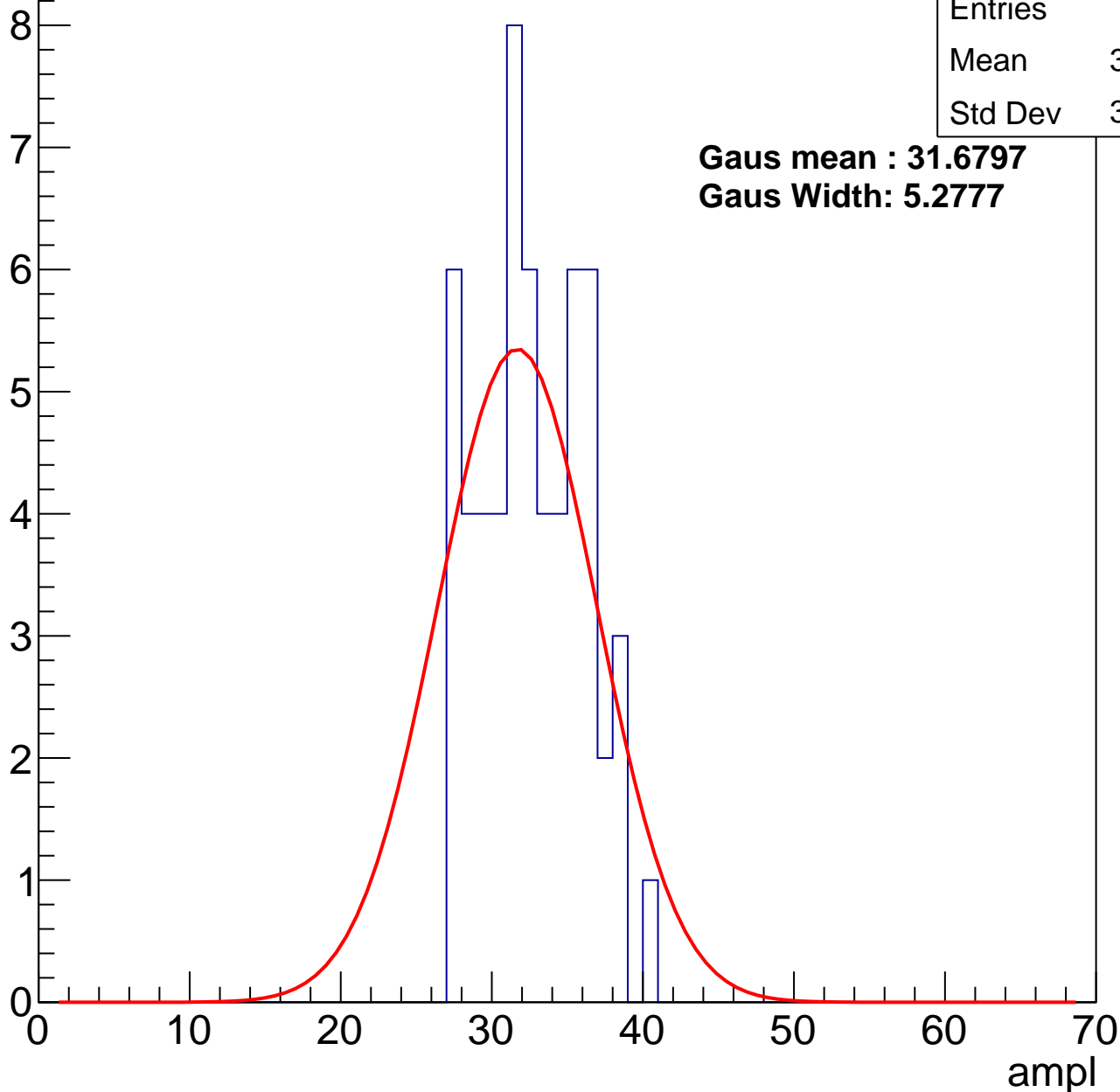
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	32.28
Std Dev	3.377

**Gaus mean : 31.6797**

**Gaus Width: 5.2777**



# B0L001S, U24-ch50, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	81
Mean	38.67
Std Dev	3.963

**Gaus mean : 39.6731**

**Gaus Width: 4.2711**

Entry

10

8

6

4

2

0

0

10

20

30

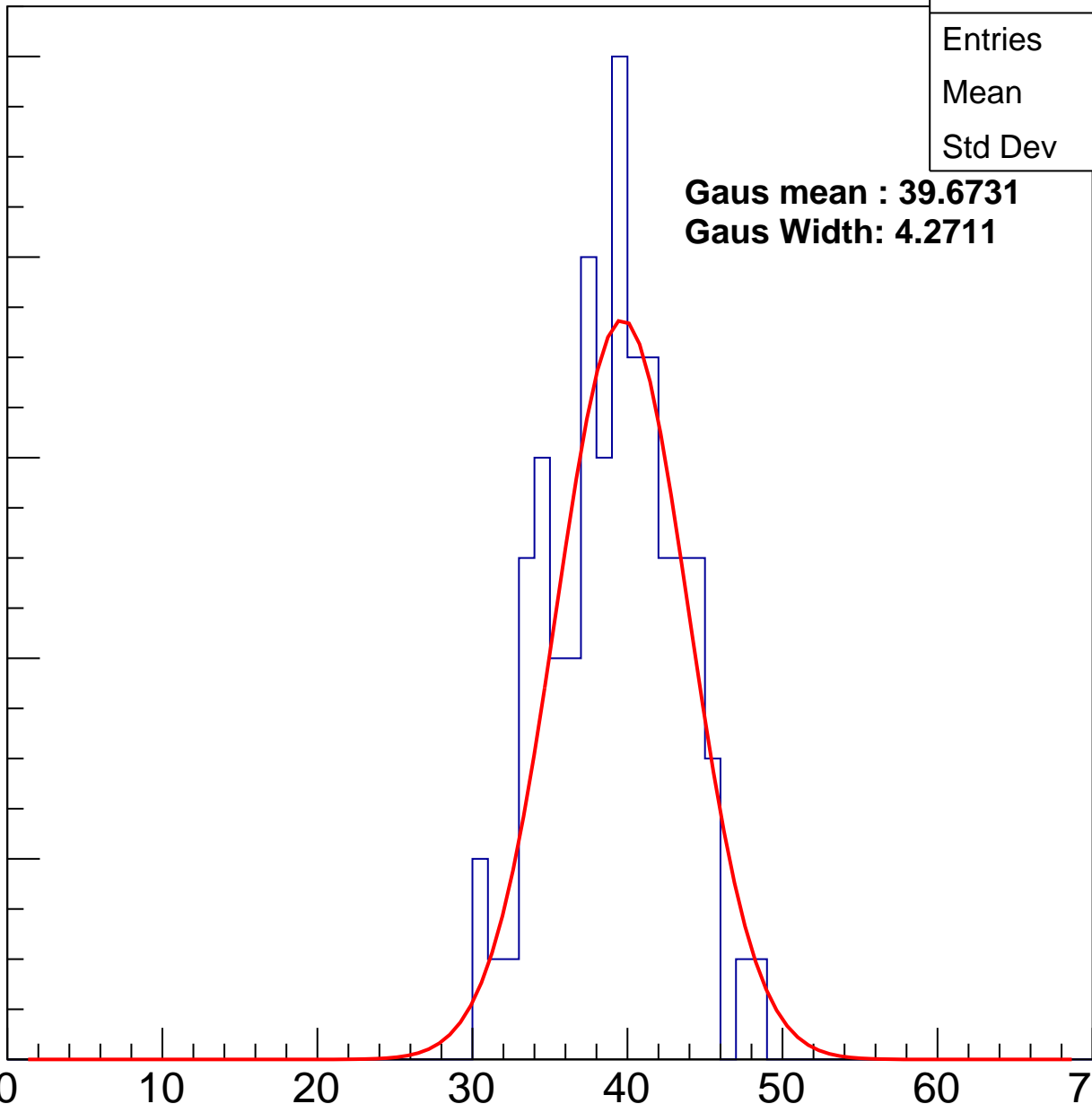
40

50

60

70

ampl



# B0L001S, U24-ch50, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	72
Mean	46.29
Std Dev	3.281

**Gaus mean : 46.8075**

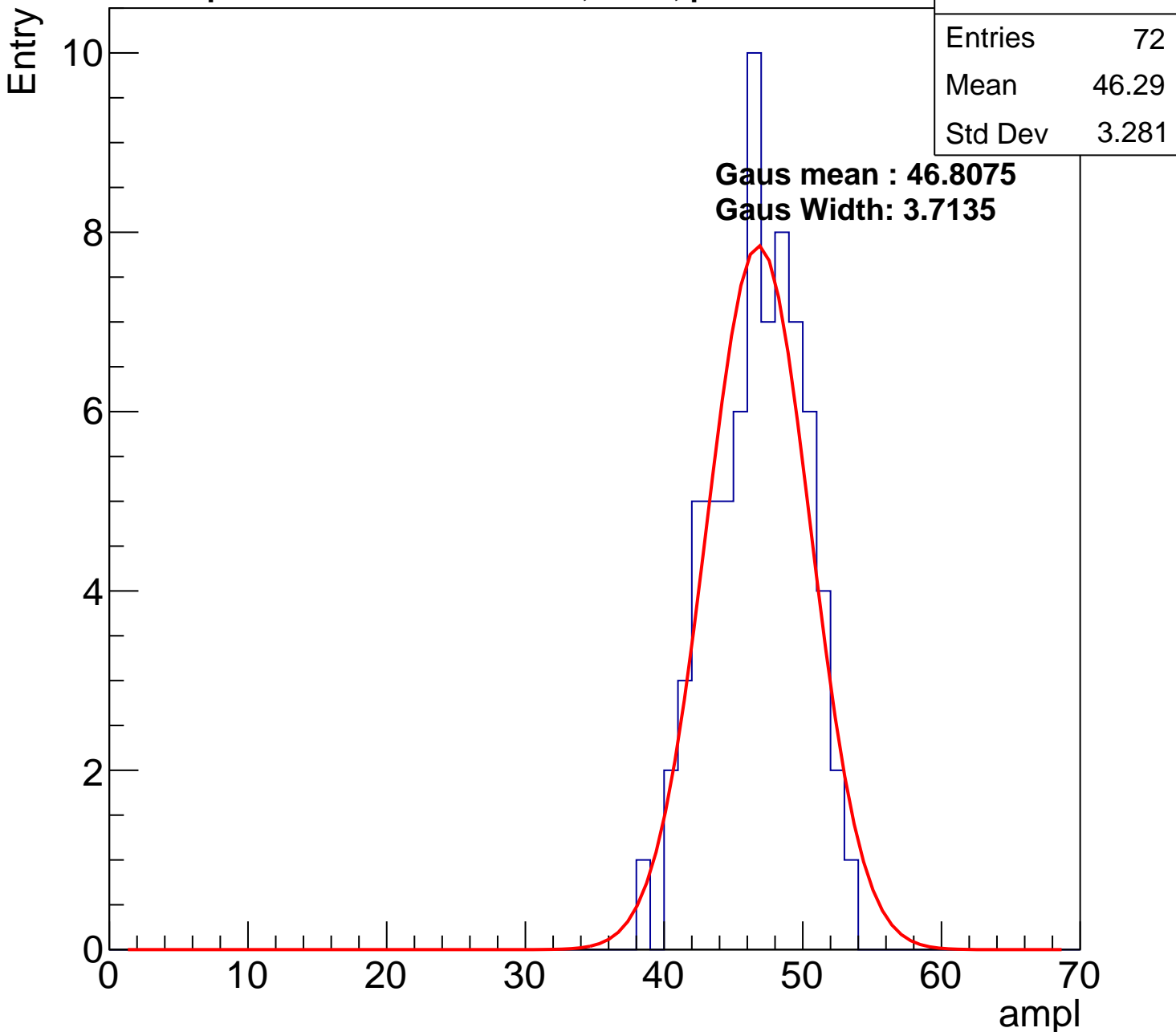
**Gaus Width: 3.7135**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

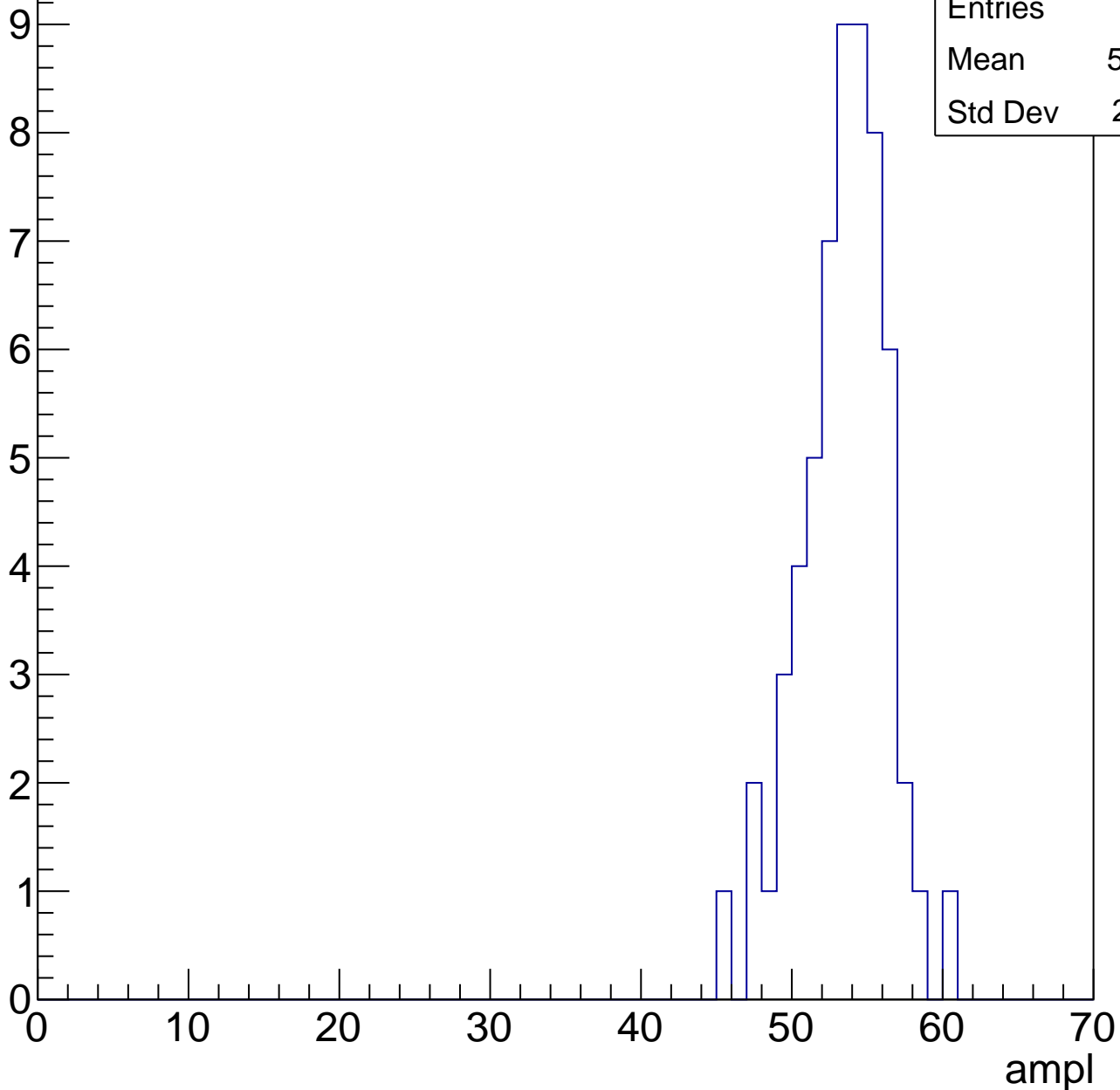


# B0L001S, U24-ch50, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	52.95
Std Dev	2.831

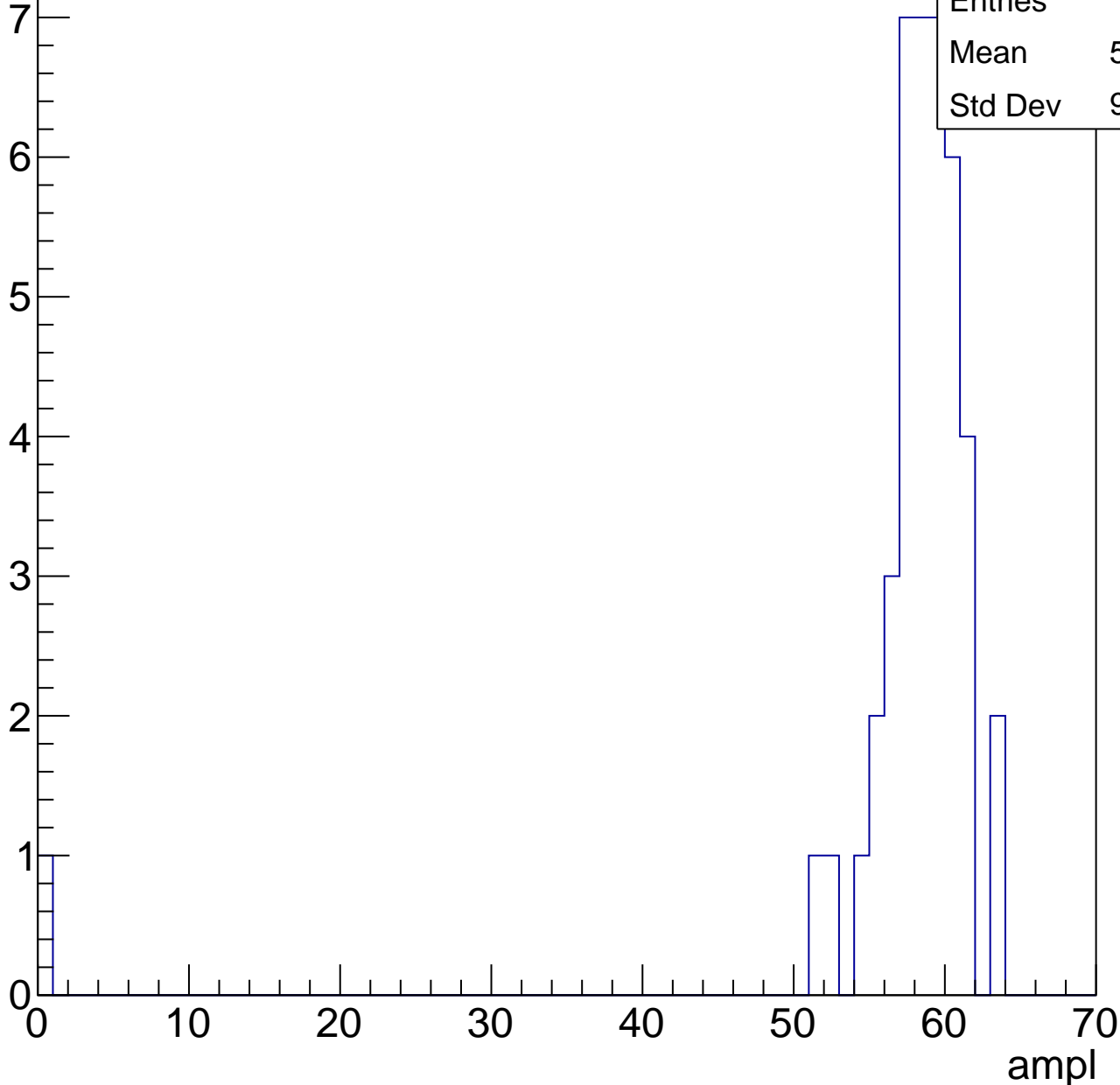


# B0L001S, U24-ch50, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	42
Mean	56.74
Std Dev	9.196

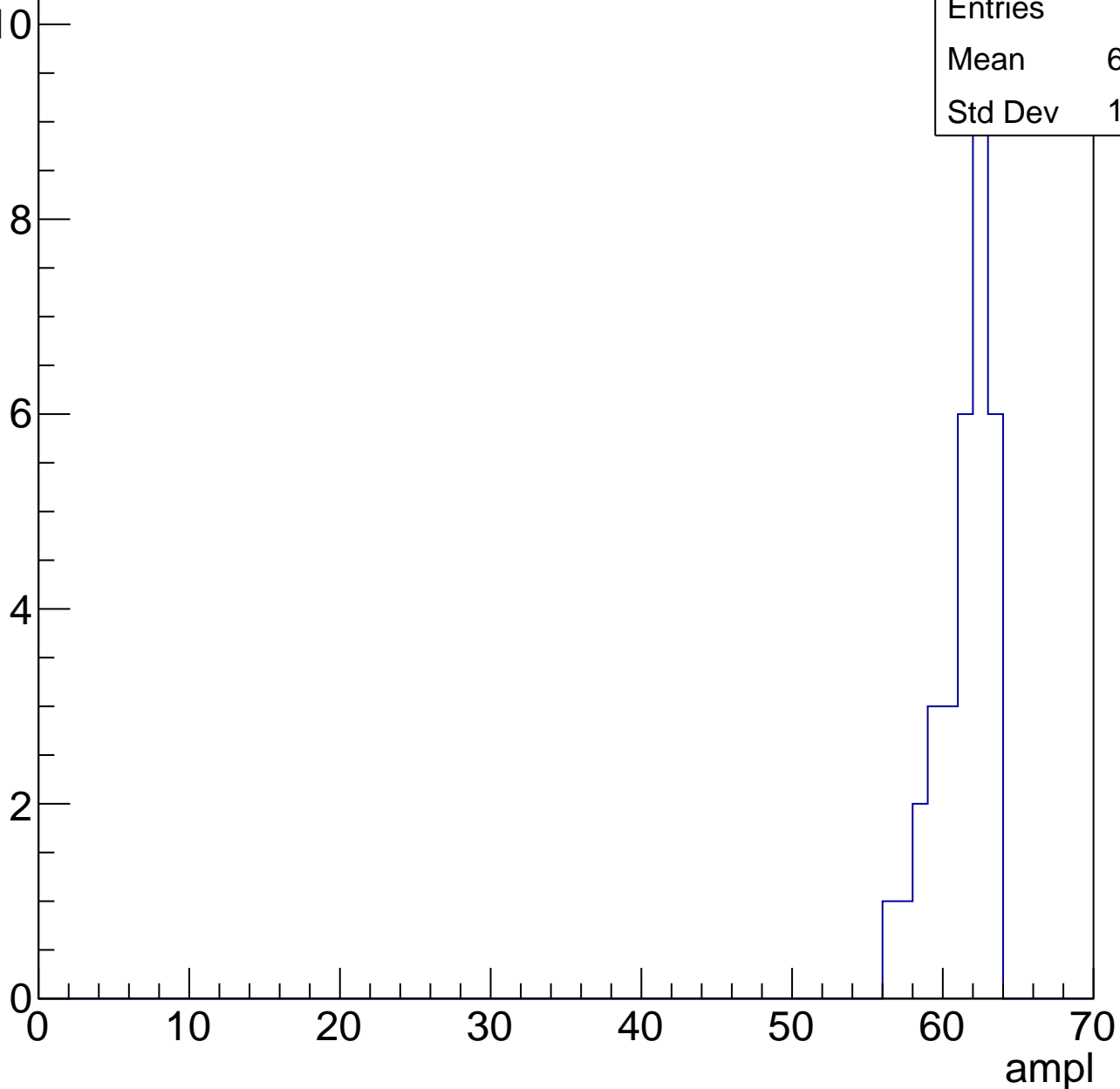


# B0L001S, U24-ch50, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	32
Mean	60.94
Std Dev	1.836



# B0L001S, U24-ch50, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	63
Std Dev	0

0 10 20 30 40 50 60 70

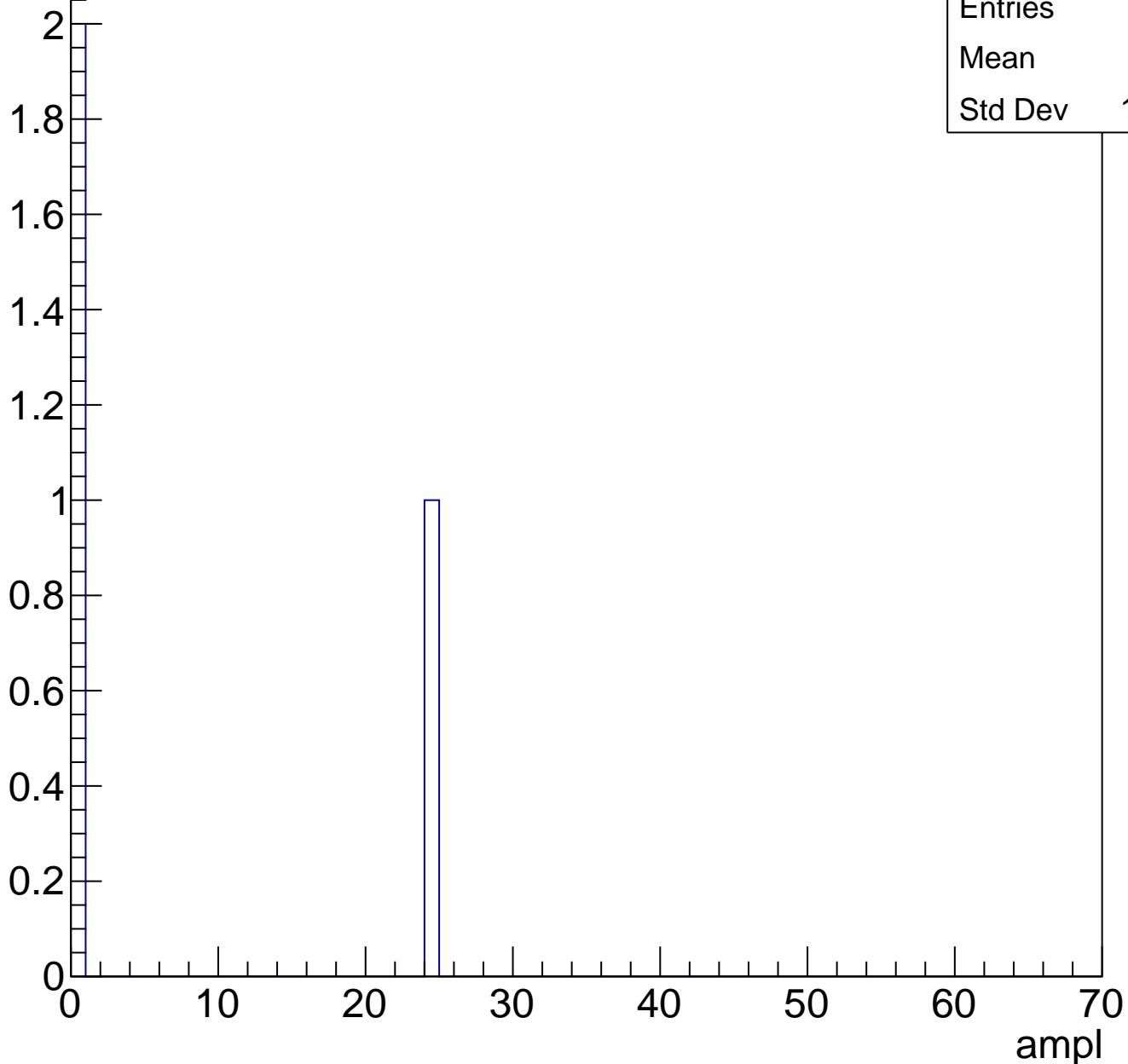
ampl



# B0L001S, U24-ch50, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	3
Mean	8
Std Dev	11.31

# B0L001S, U24-ch51, adc0

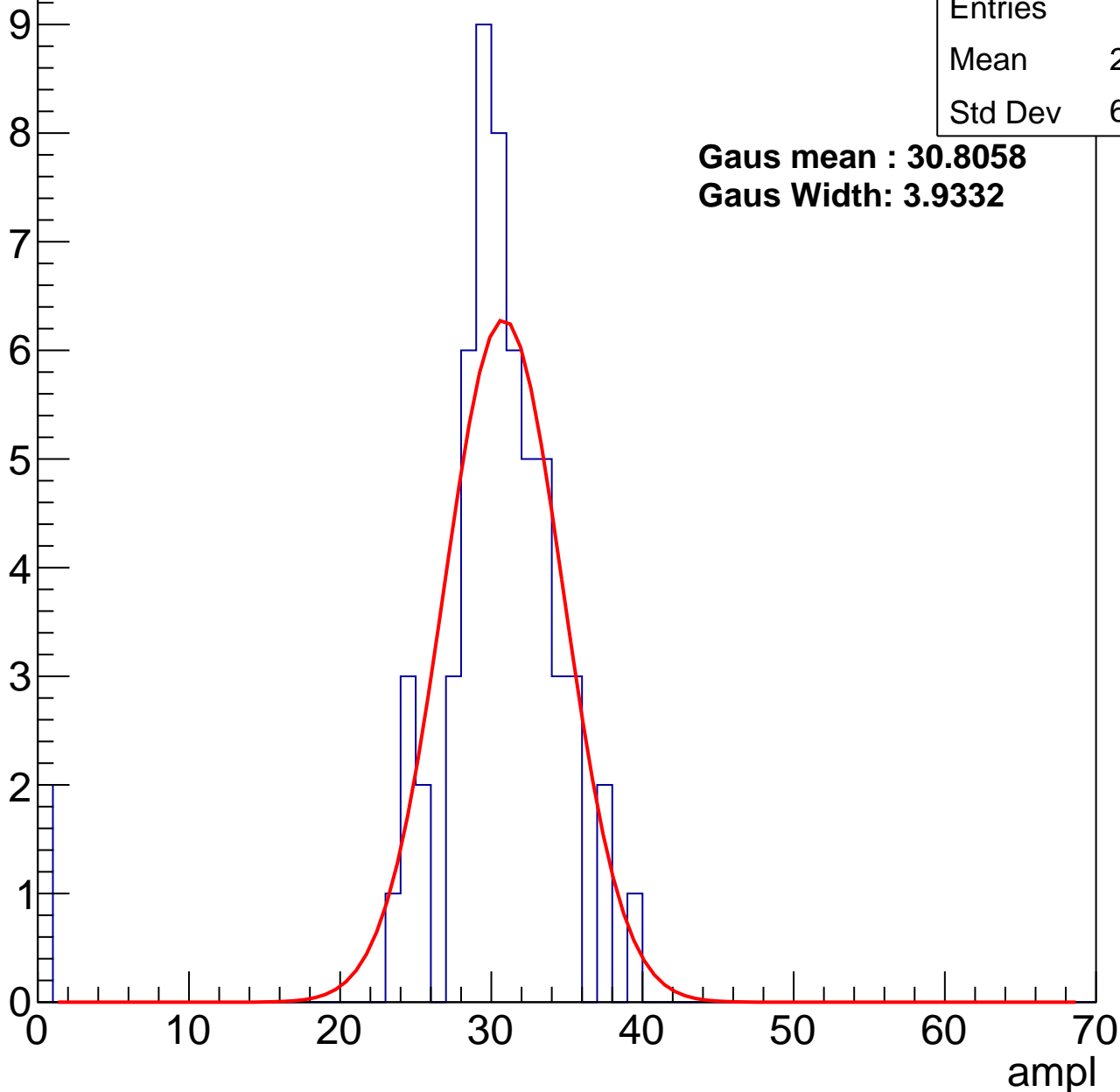
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	29.25
Std Dev	6.387

**Gaus mean : 30.8058**

**Gaus Width: 3.9332**



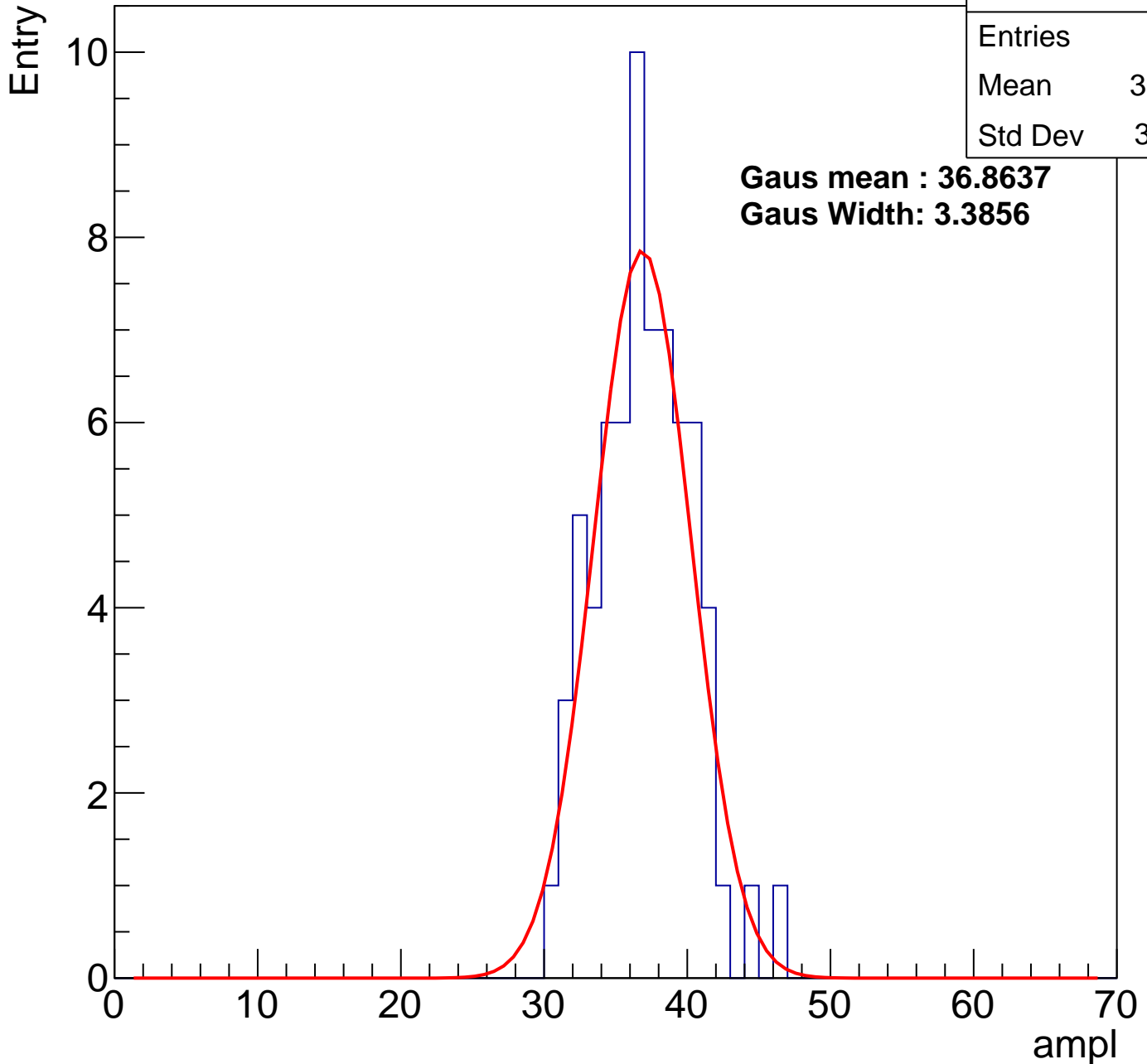
# B0L001S, U24-ch51, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	68
Mean	36.53
Std Dev	3.261

**Gaus mean : 36.8637**

**Gaus Width: 3.3856**



# B0L001S, U24-ch51, adc2

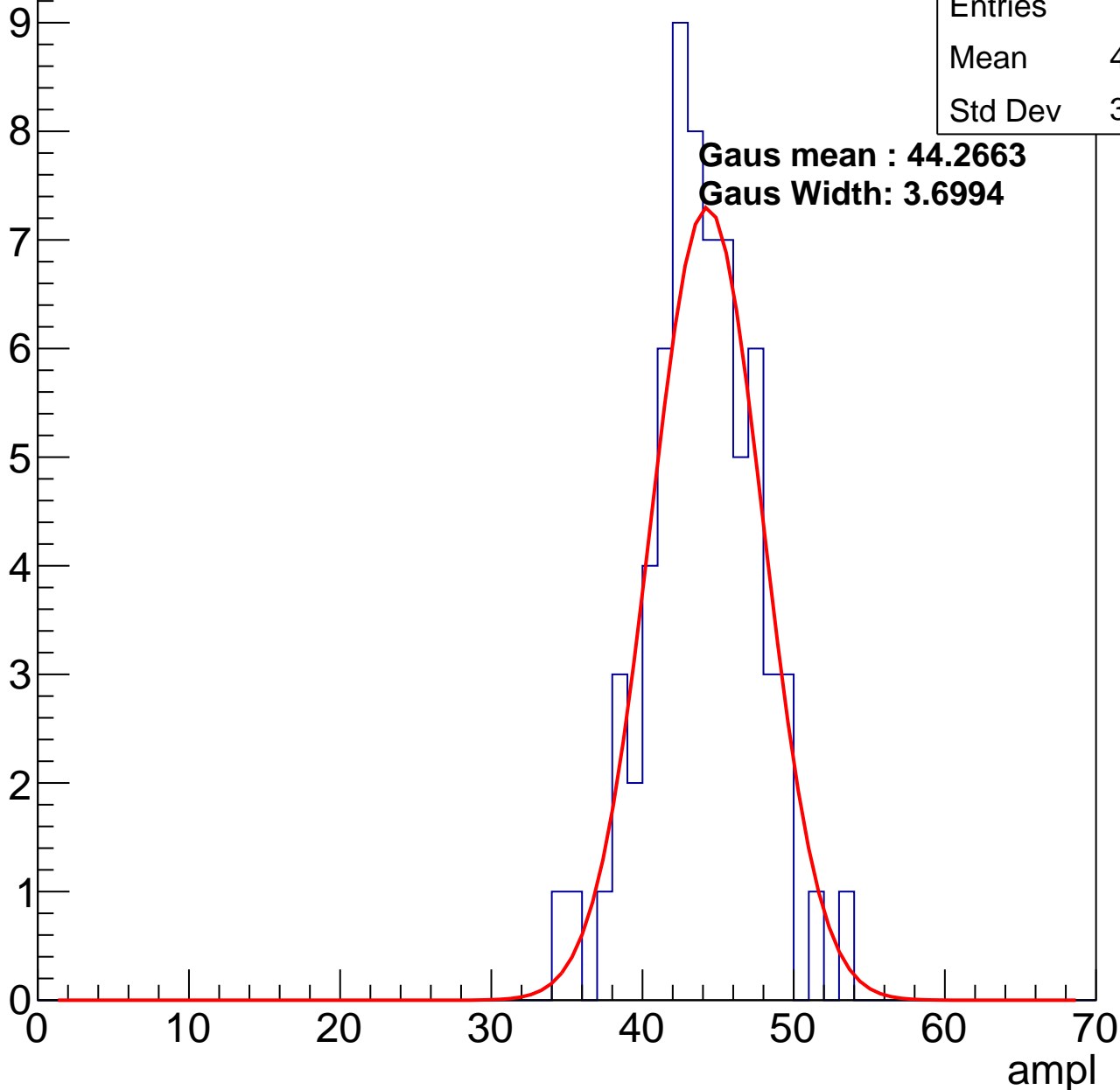
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	43.47
Std Dev	3.566

**Gaus mean : 44.2663**

**Gaus Width: 3.6994**

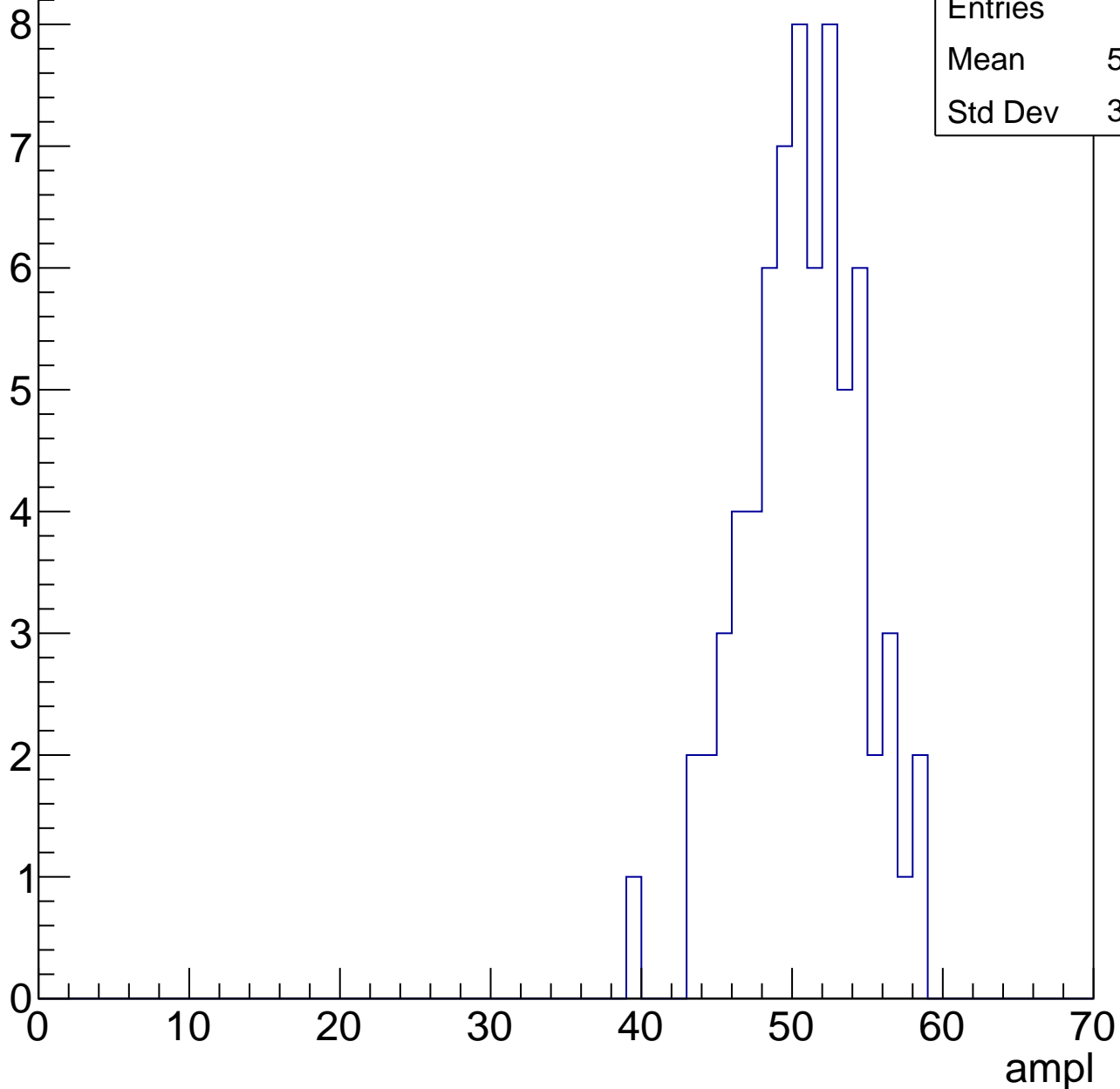


# B0L001S, U24-ch51, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	50.19
Std Dev	3.796

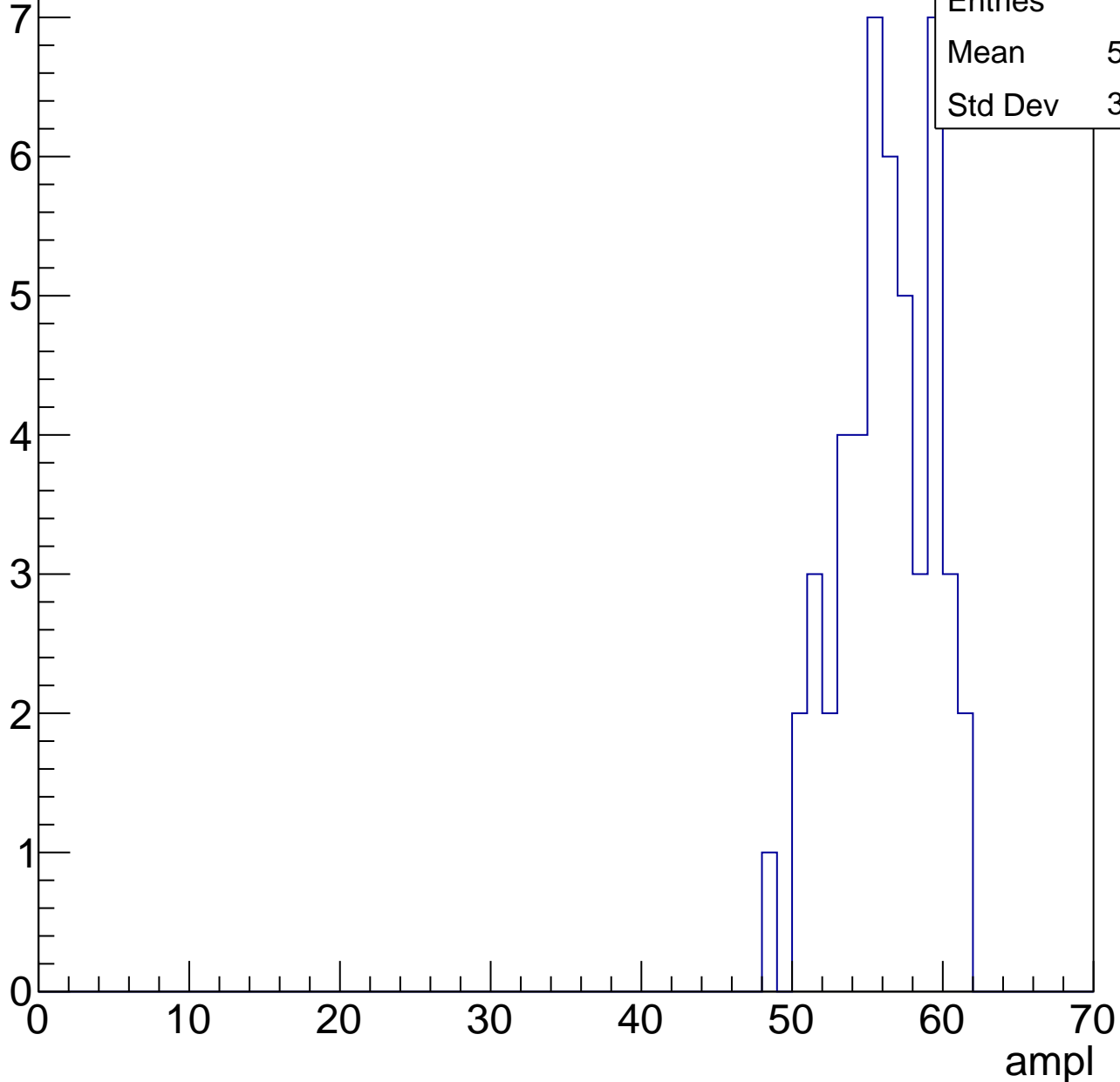


# B0L001S, U24-ch51, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	49
Mean	55.67
Std Dev	3.113

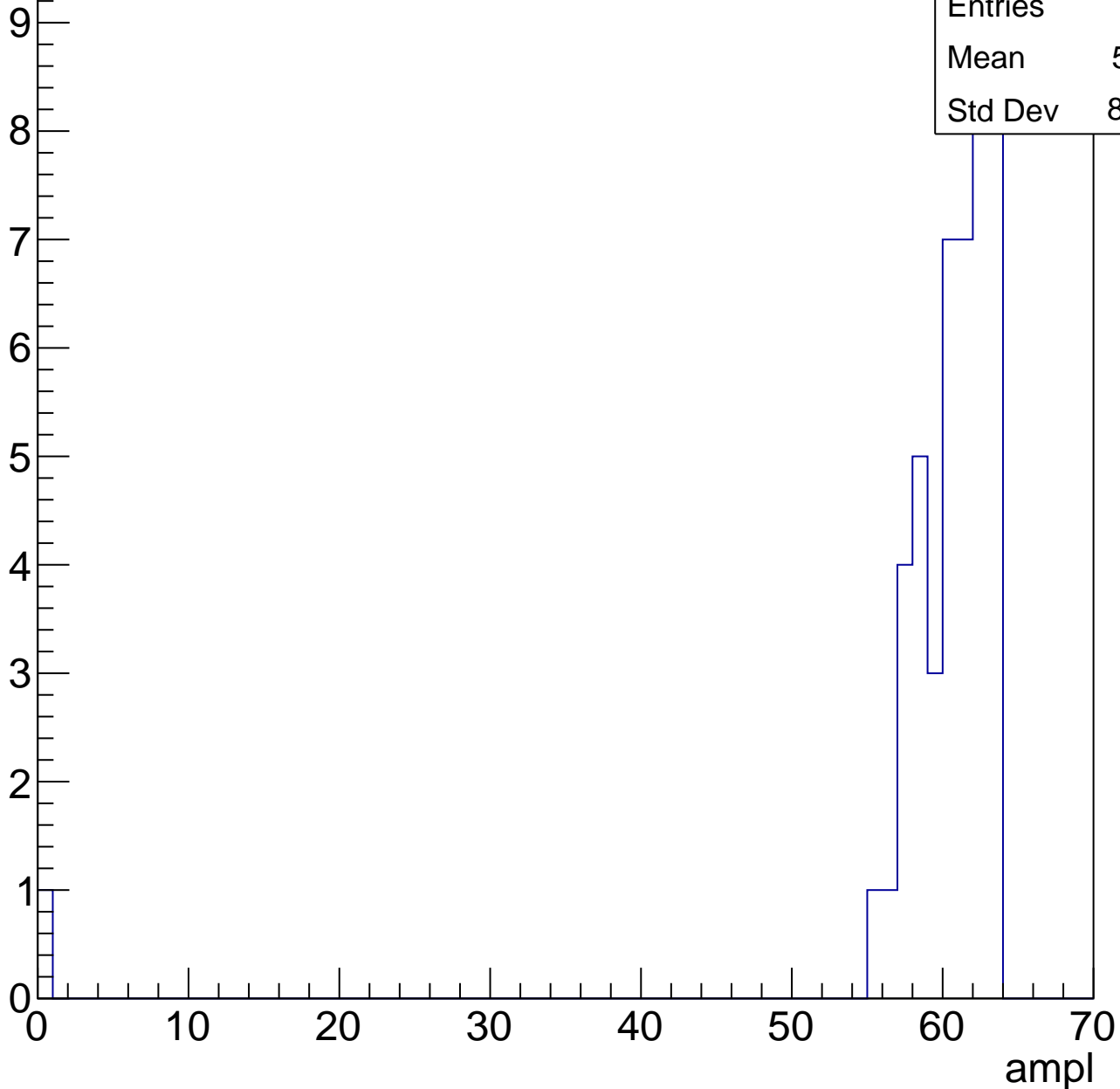


# B0L001S, U24-ch51, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	47
Mean	59.11
Std Dev	8.976



# B0L001S, U24-ch51, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch51, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	3
Mean	7.333
Std Dev	10.37

# B0L001S, U24-ch52, adc0

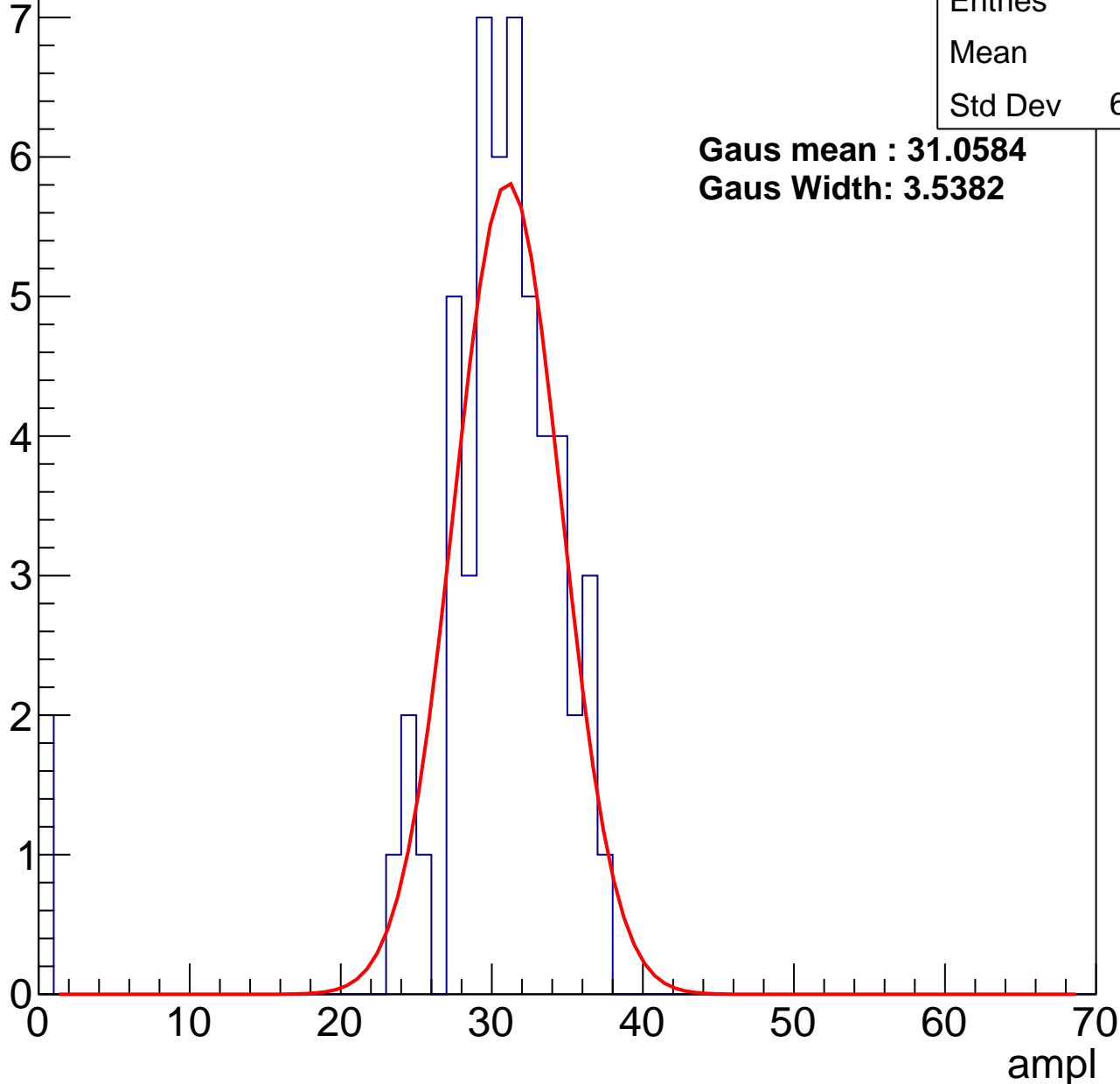
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	29.4
Std Dev	6.623

**Gaus mean : 31.0584**

**Gaus Width: 3.5382**



# B0L001S, U24-ch52, adc1

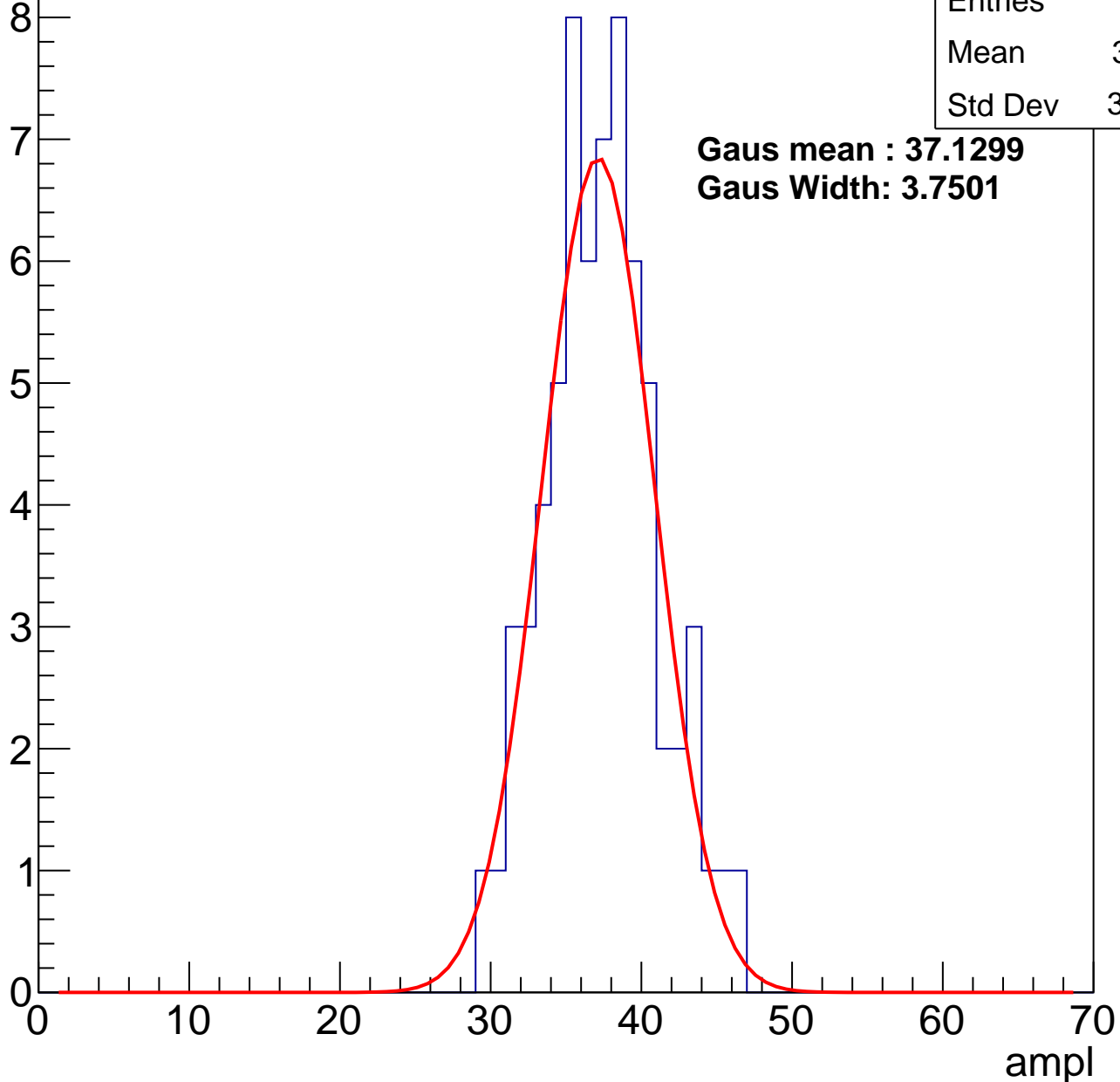
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	36.91
Std Dev	3.672

**Gaus mean : 37.1299**

**Gaus Width: 3.7501**



# B0L001S, U24-ch52, adc2

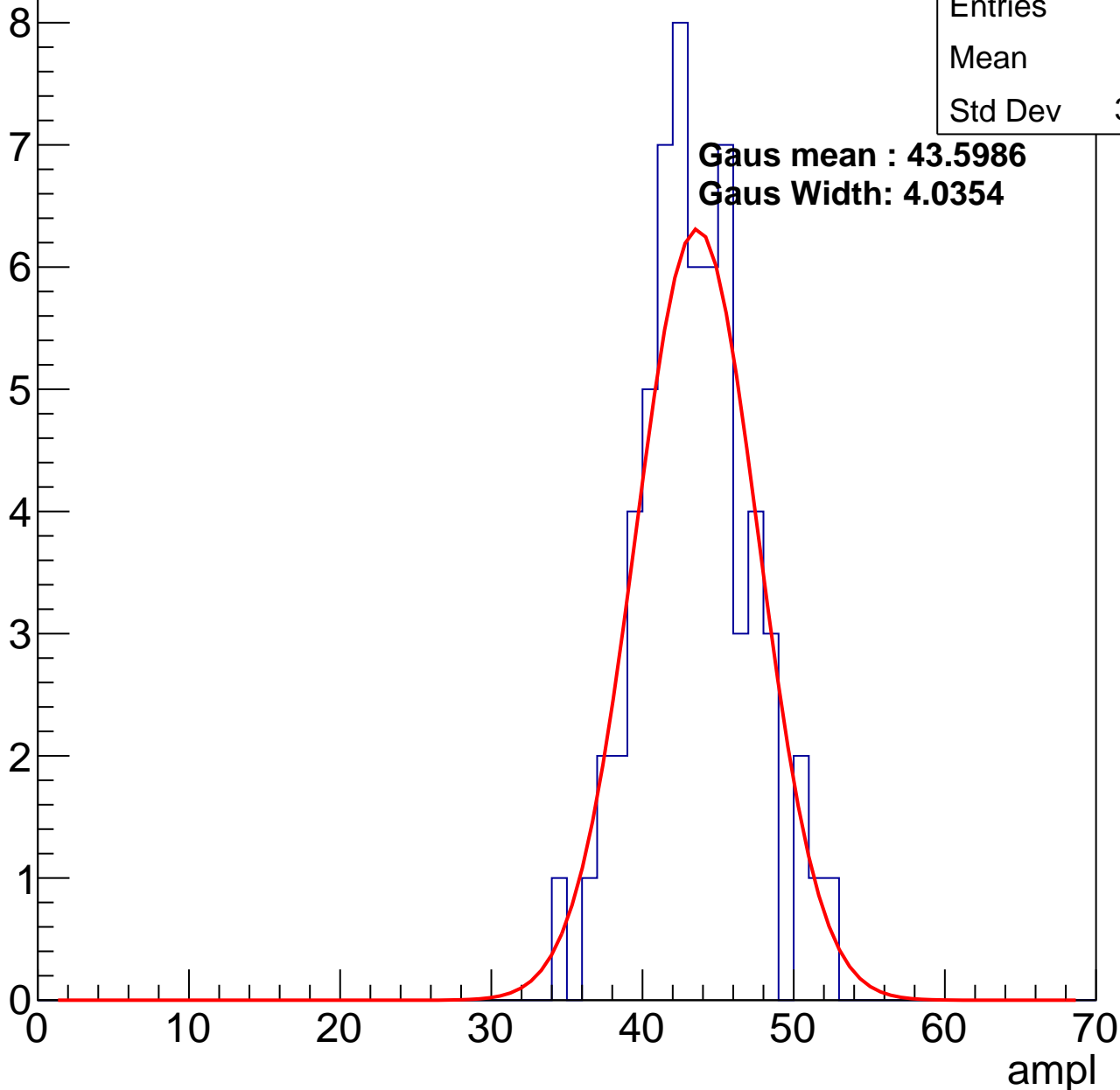
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	43
Std Dev	3.651

**Gaus mean : 43.5986**

**Gaus Width: 4.0354**

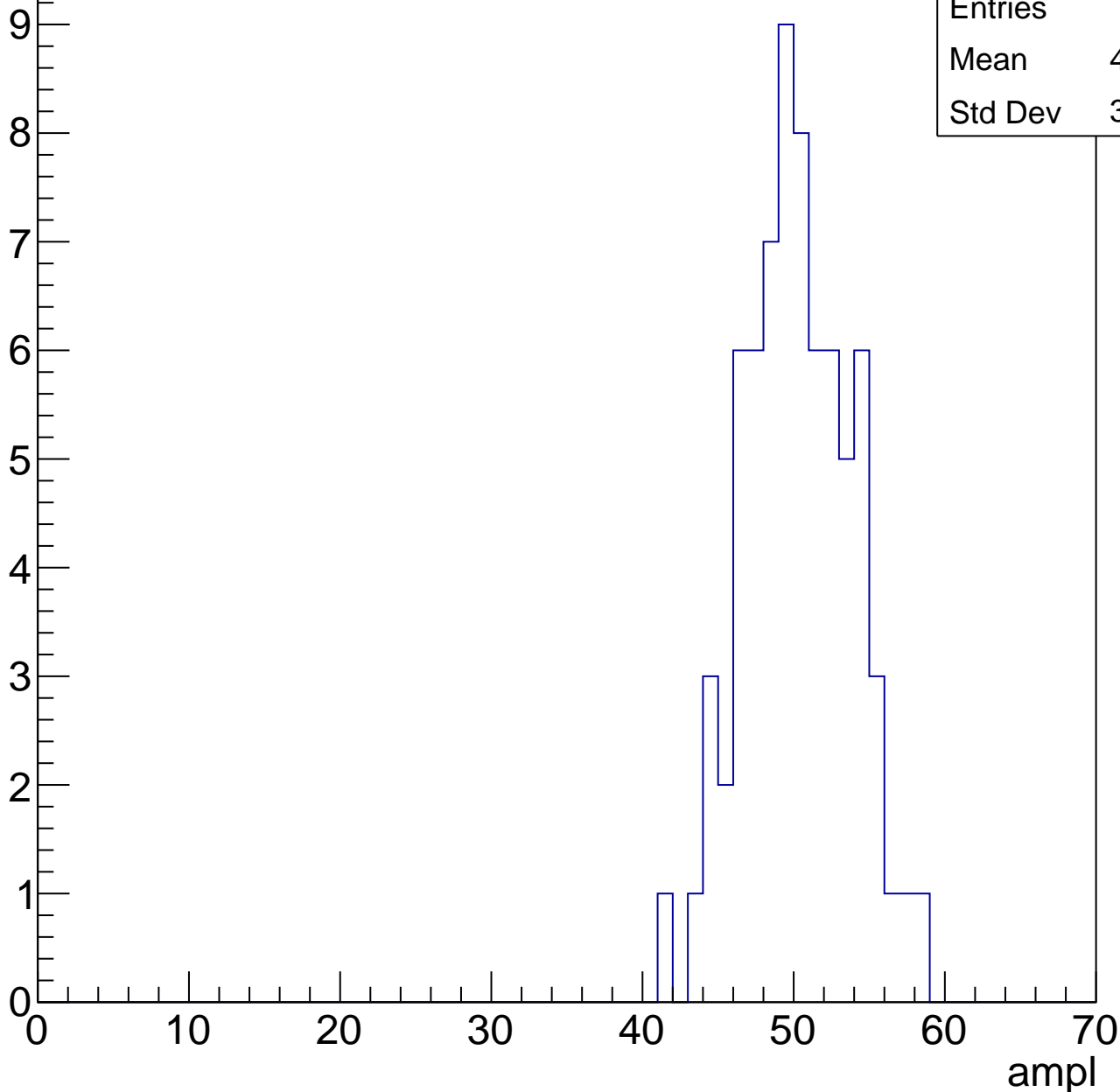


# B0L001S, U24-ch52, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	49.78
Std Dev	3.469

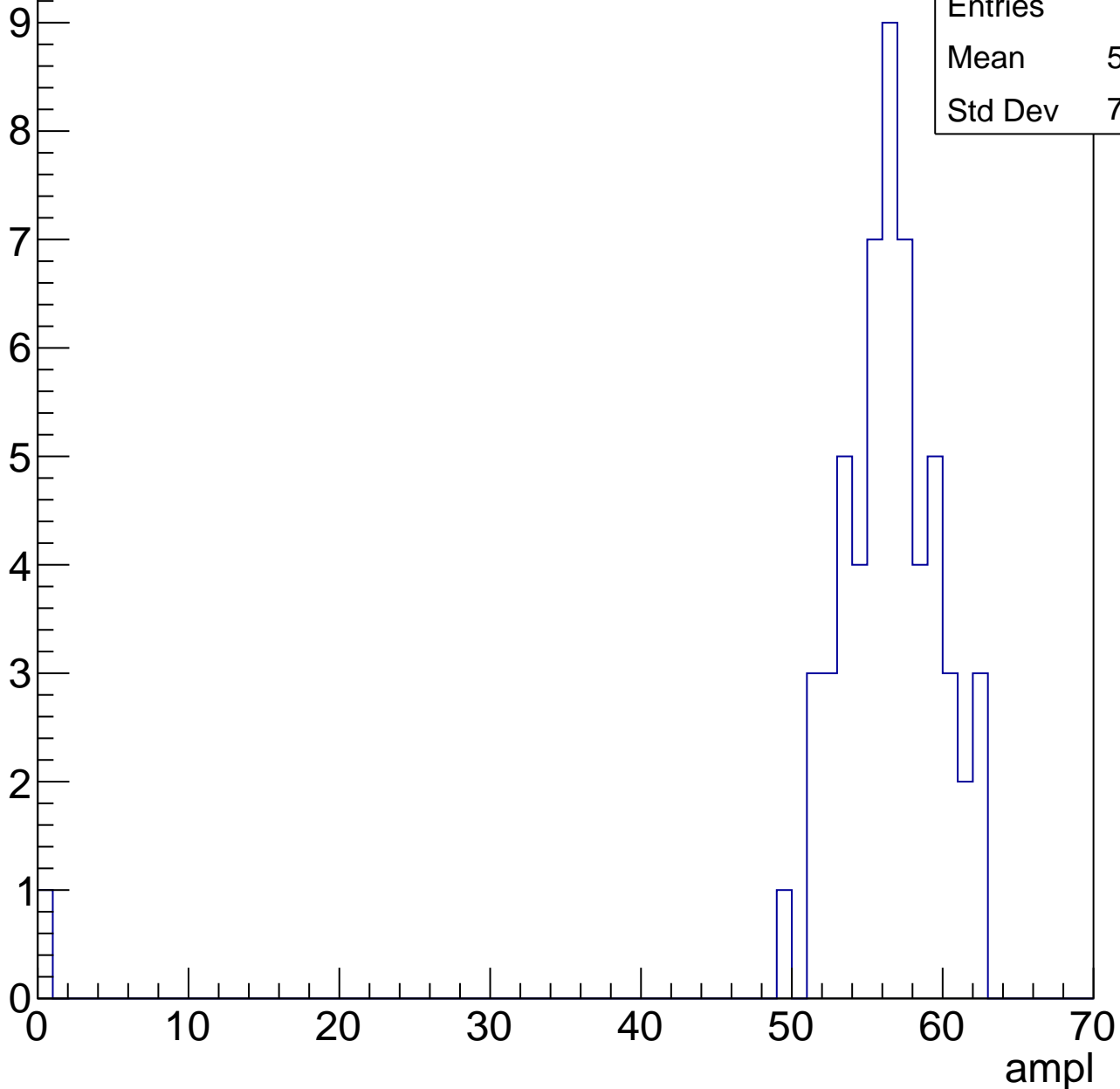


# B0L001S, U24-ch52, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

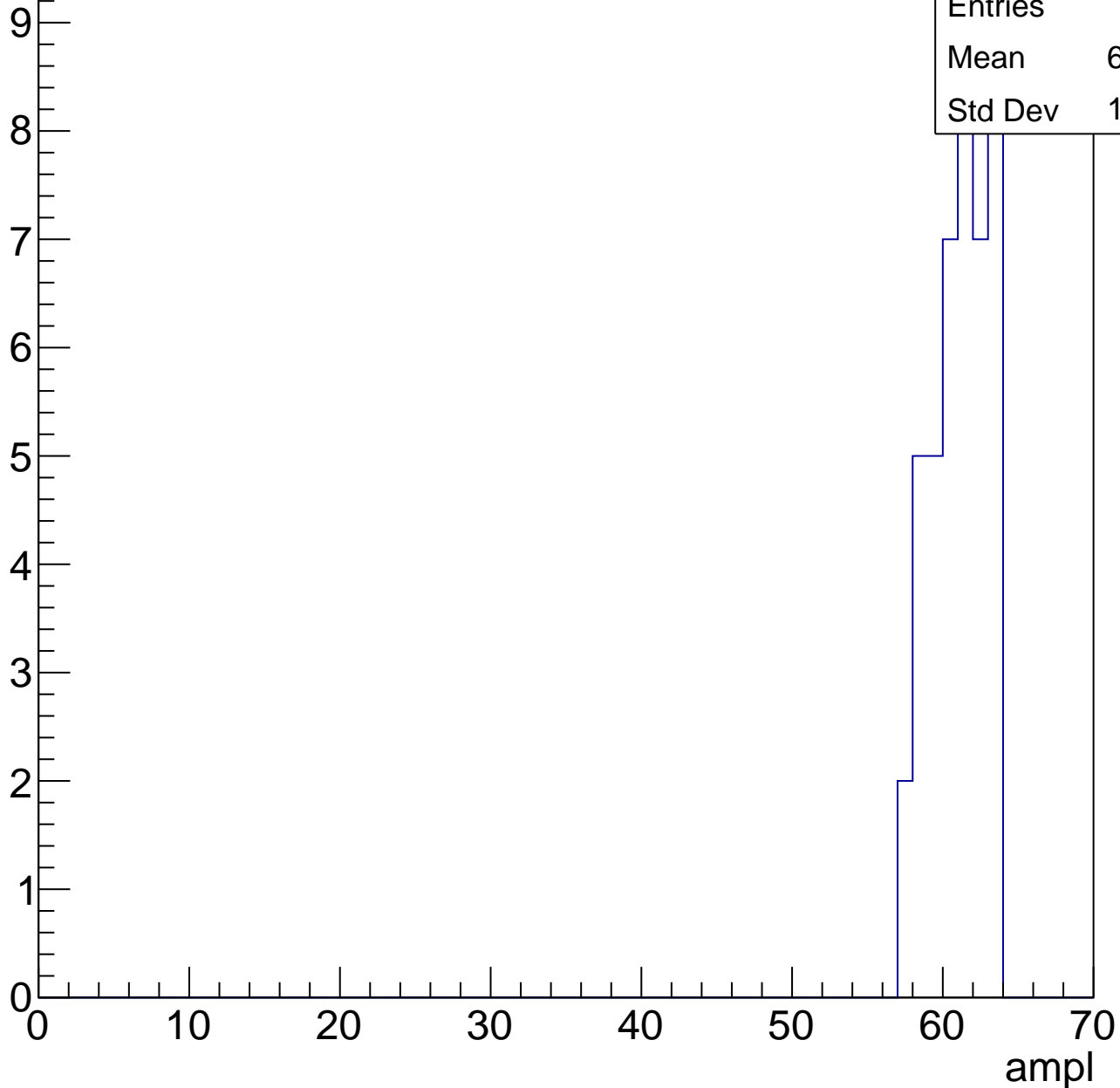
Entries	57
Mean	55.12
Std Dev	7.954



# B0L001S, U24-ch52, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U24-ch52, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U24-ch52, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	63
Std Dev	0

# B0L001S, U24-ch53, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	66
Mean	30.15
Std Dev	6.187

**Gaus mean : 31.2367**

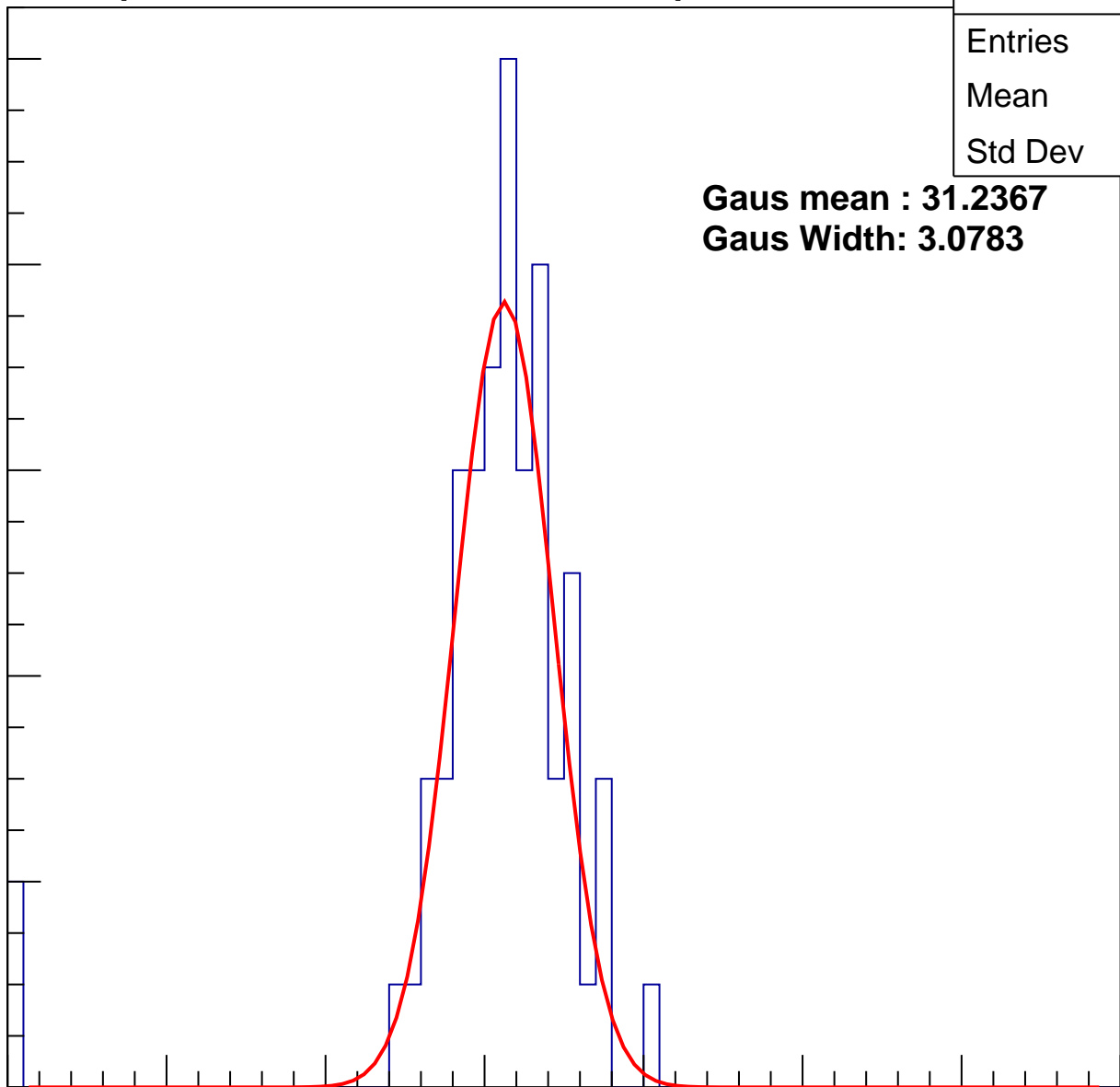
**Gaus Width: 3.0783**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U24-ch53, adc1

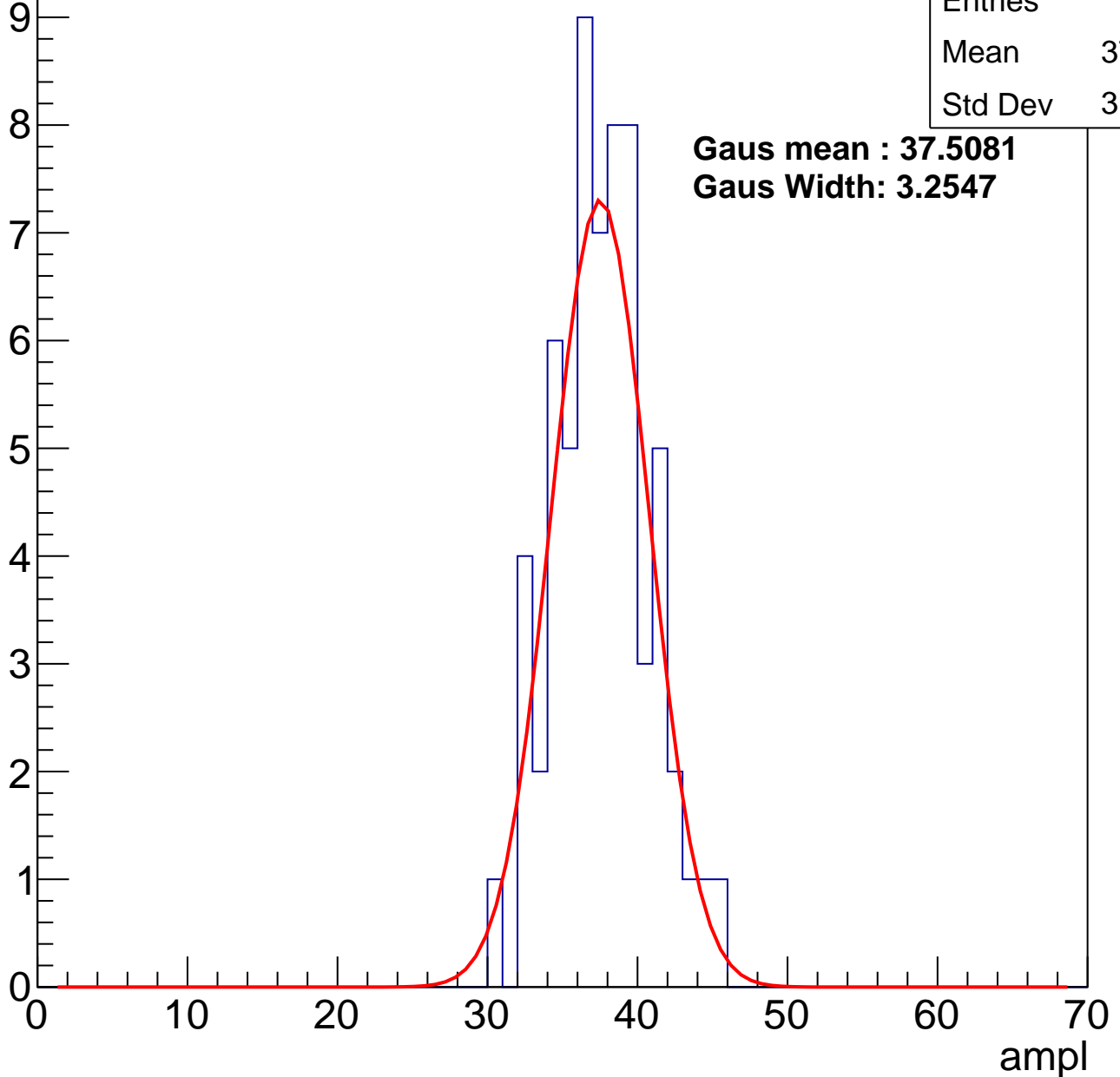
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	37.19
Std Dev	3.106

**Gaus mean : 37.5081**

**Gaus Width: 3.2547**



# B0L001S, U24-ch53, adc2

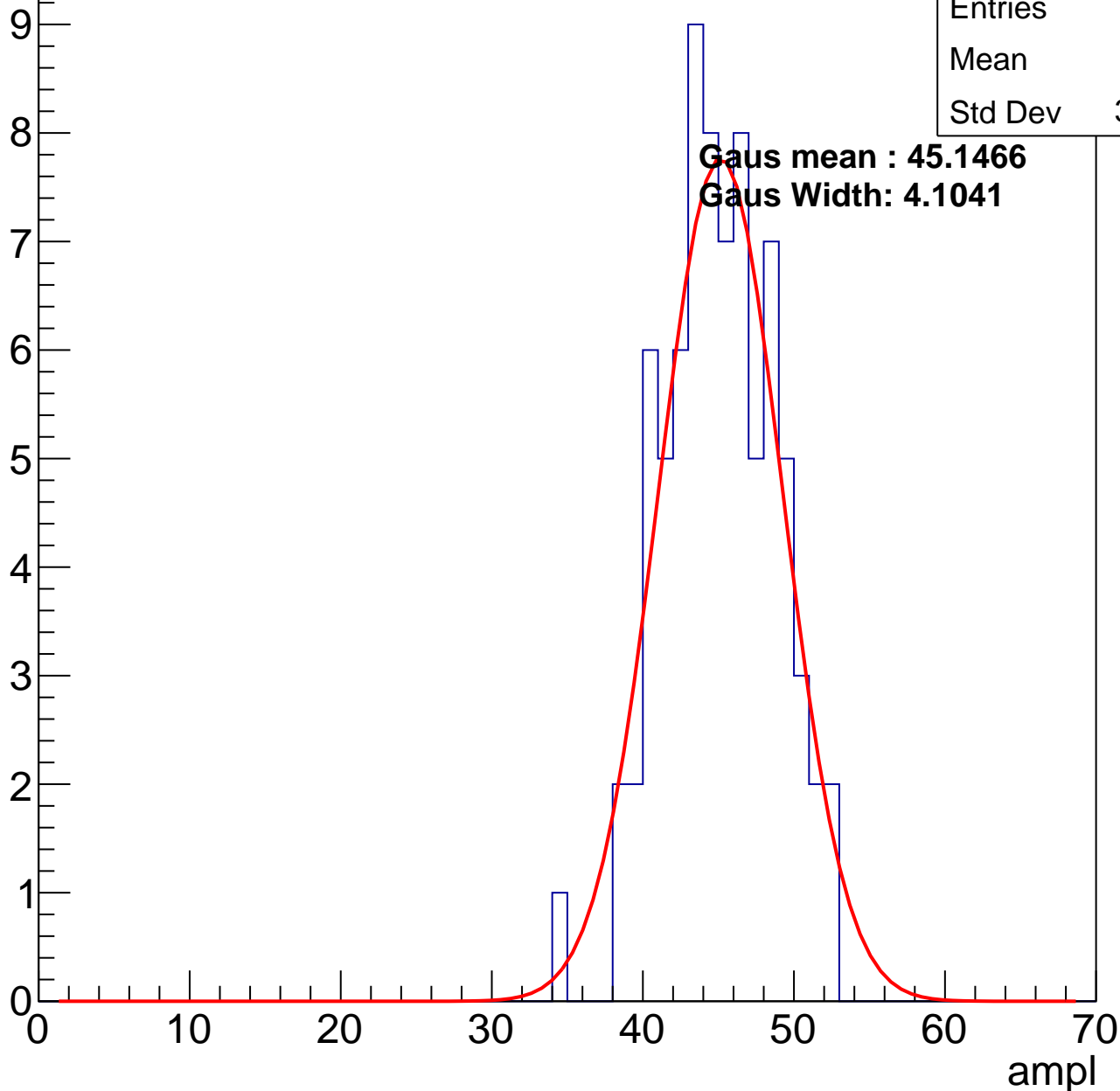
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	78
Mean	44.6
Std Dev	3.621

**Gaus mean : 45.1466**

**Gaus Width: 4.1041**

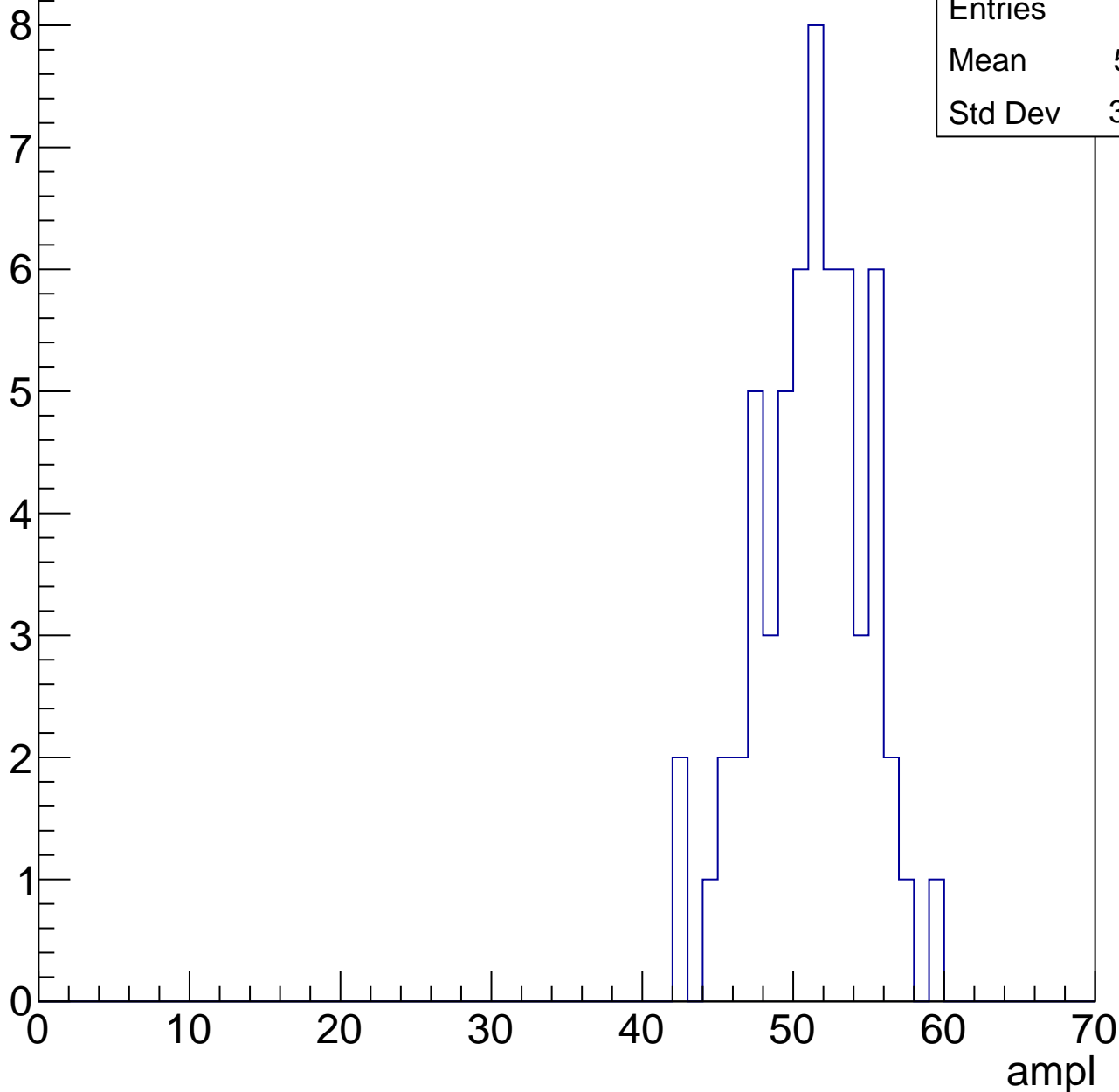


# B0L001S, U24-ch53, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

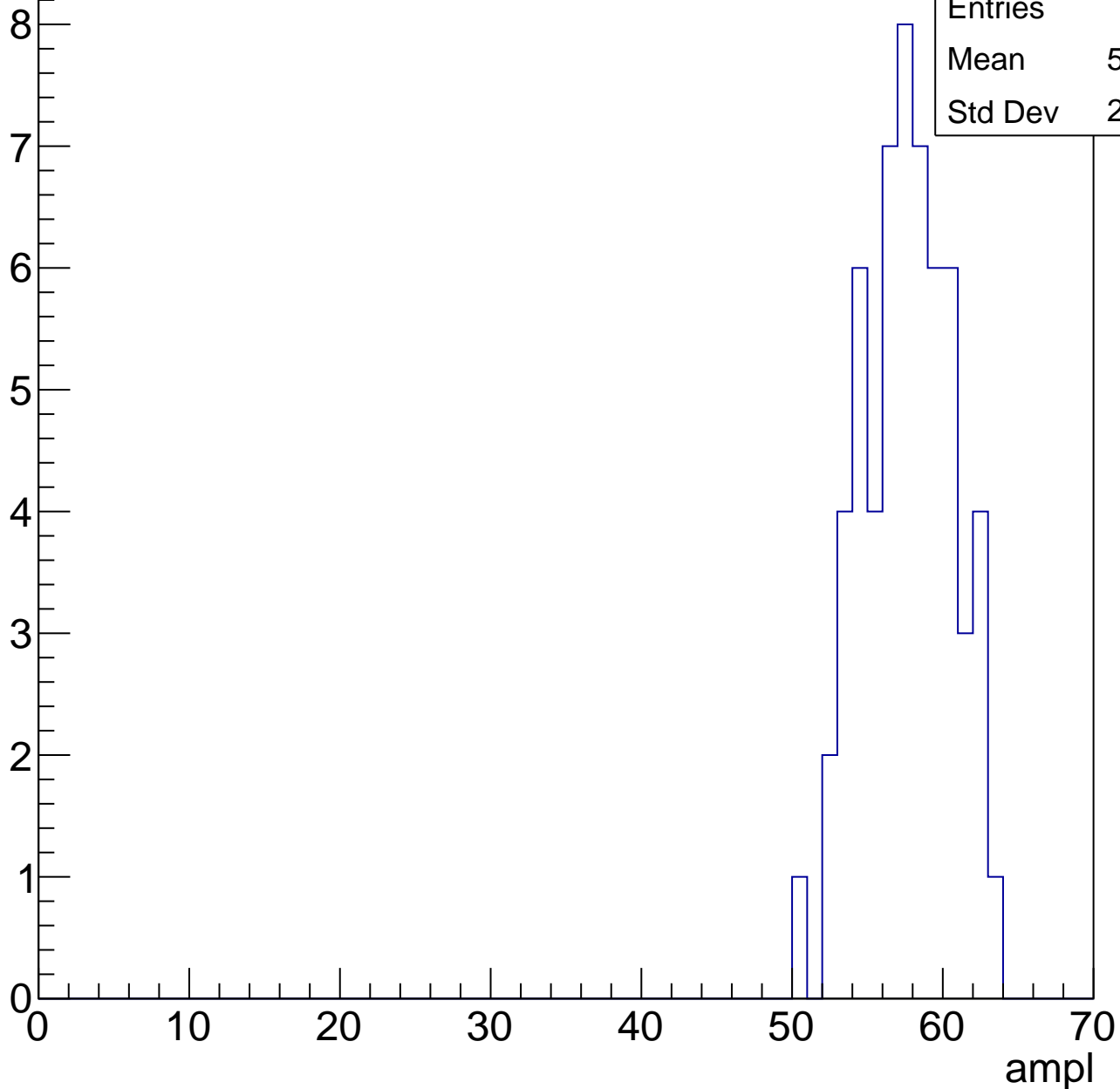
Entries	59
Mean	50.71
Std Dev	3.599



# B0L001S, U24-ch53, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



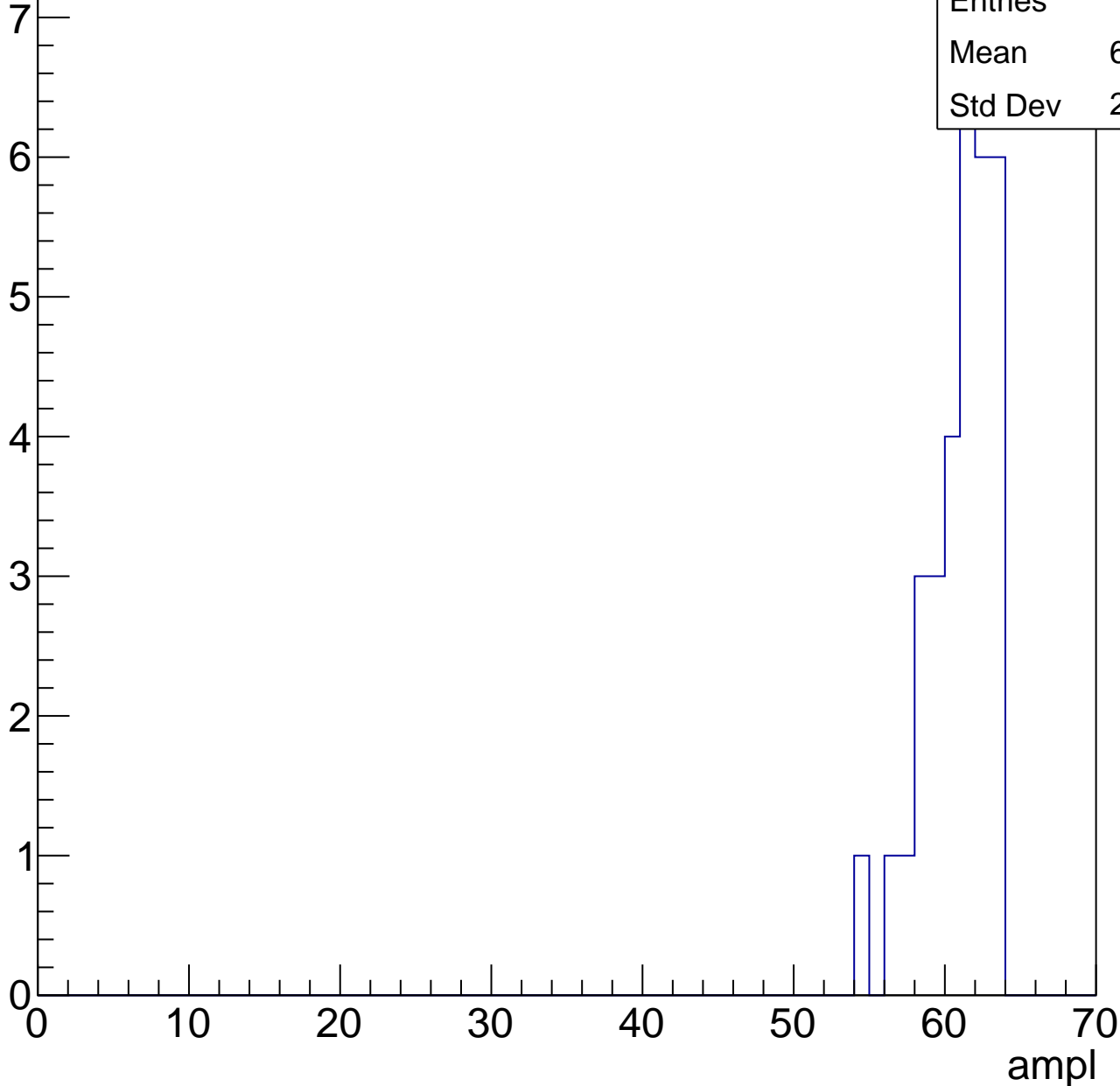
Entries	59
Mean	57.15
Std Dev	2.933

# B0L001S, U24-ch53, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

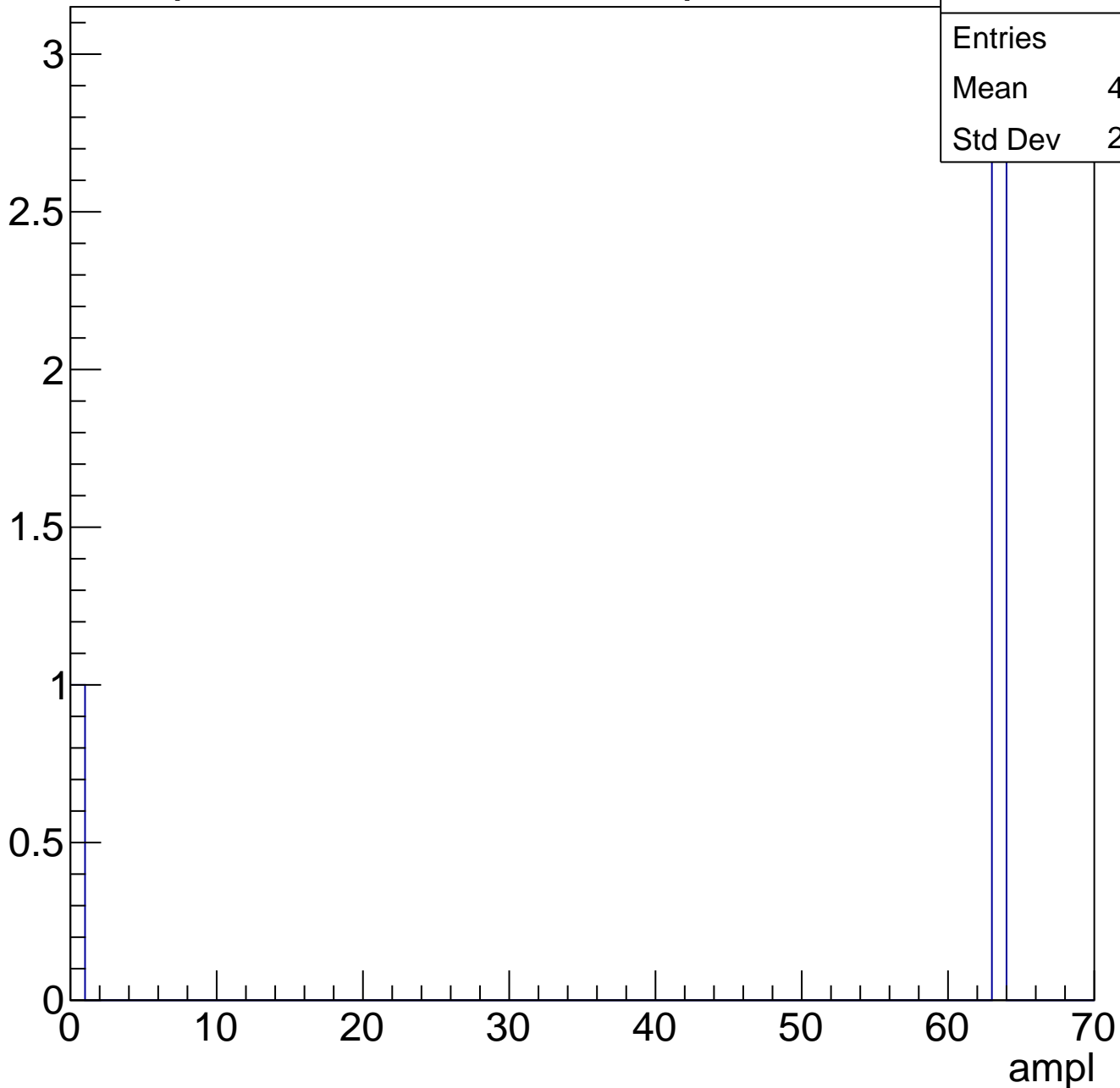
Entries	32
Mean	60.47
Std Dev	2.194



# B0L001S, U24-ch53, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch53, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U24-ch54, adc0

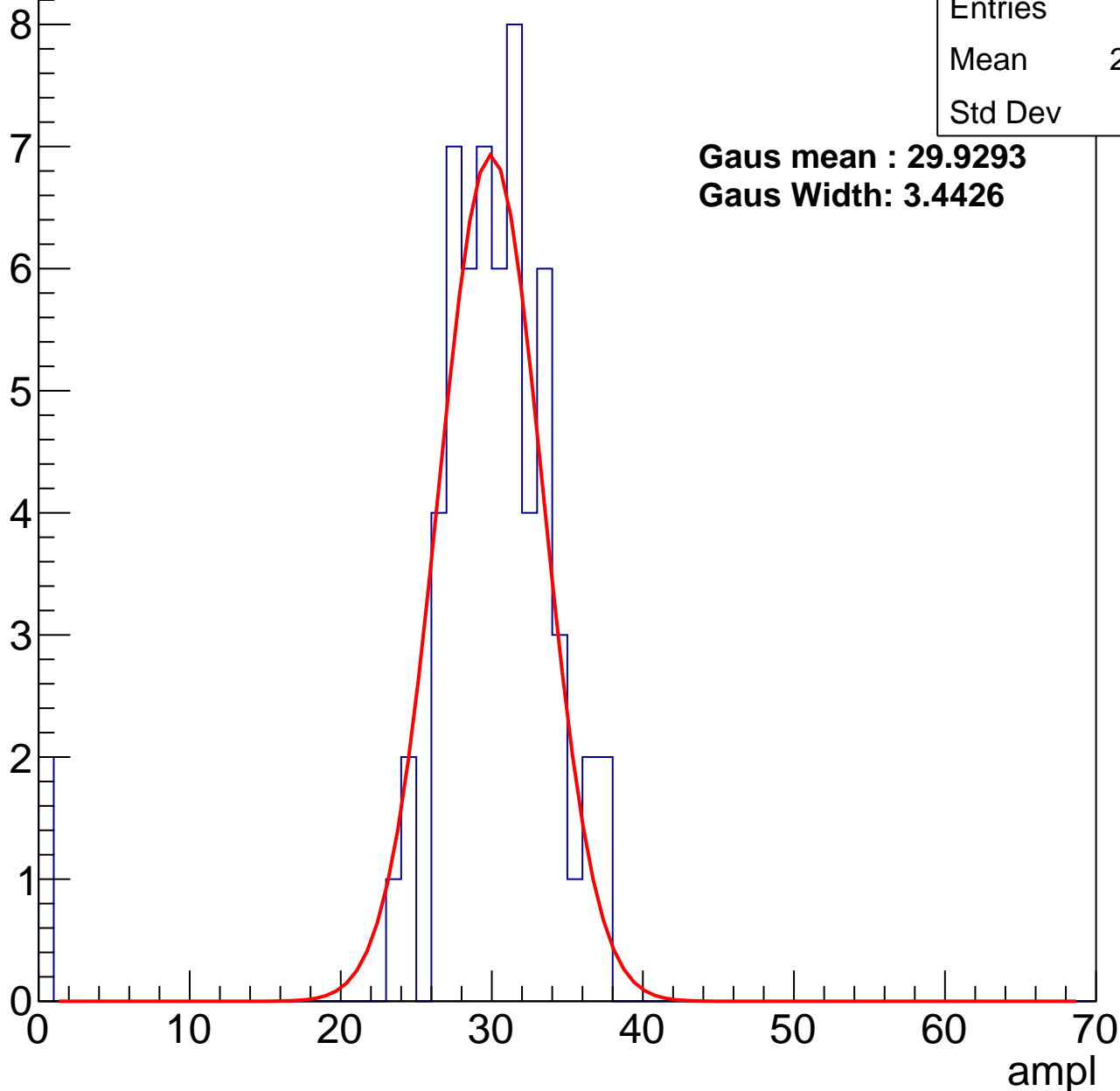
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	29.05
Std Dev	6.2

**Gaus mean : 29.9293**

**Gaus Width: 3.4426**



# B0L001S, U24-ch54, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	72
Mean	36.49
Std Dev	3.354

**Gaus mean : 36.7541**

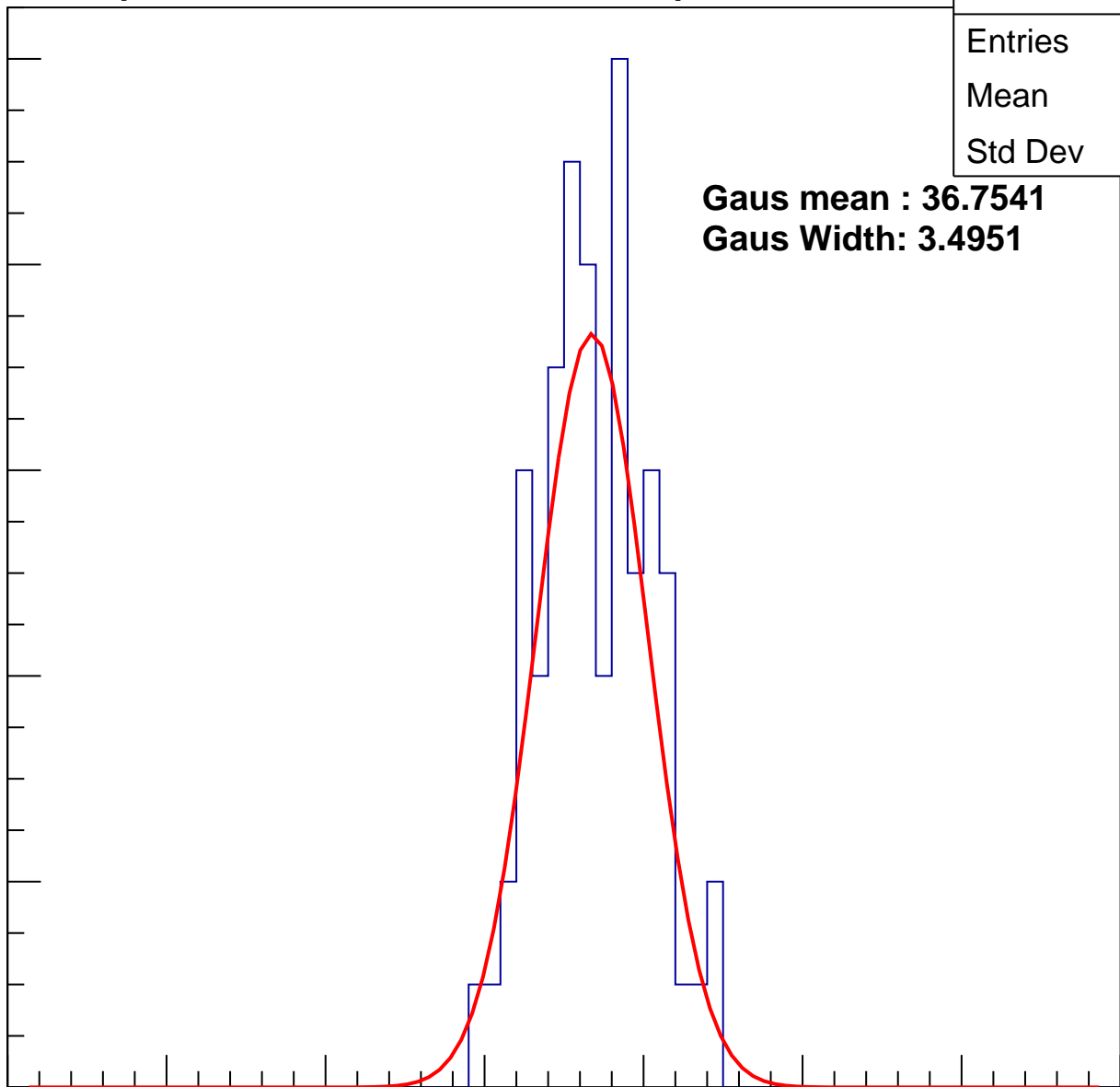
**Gaus Width: 3.4951**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B0L001S, U24-ch54, adc2

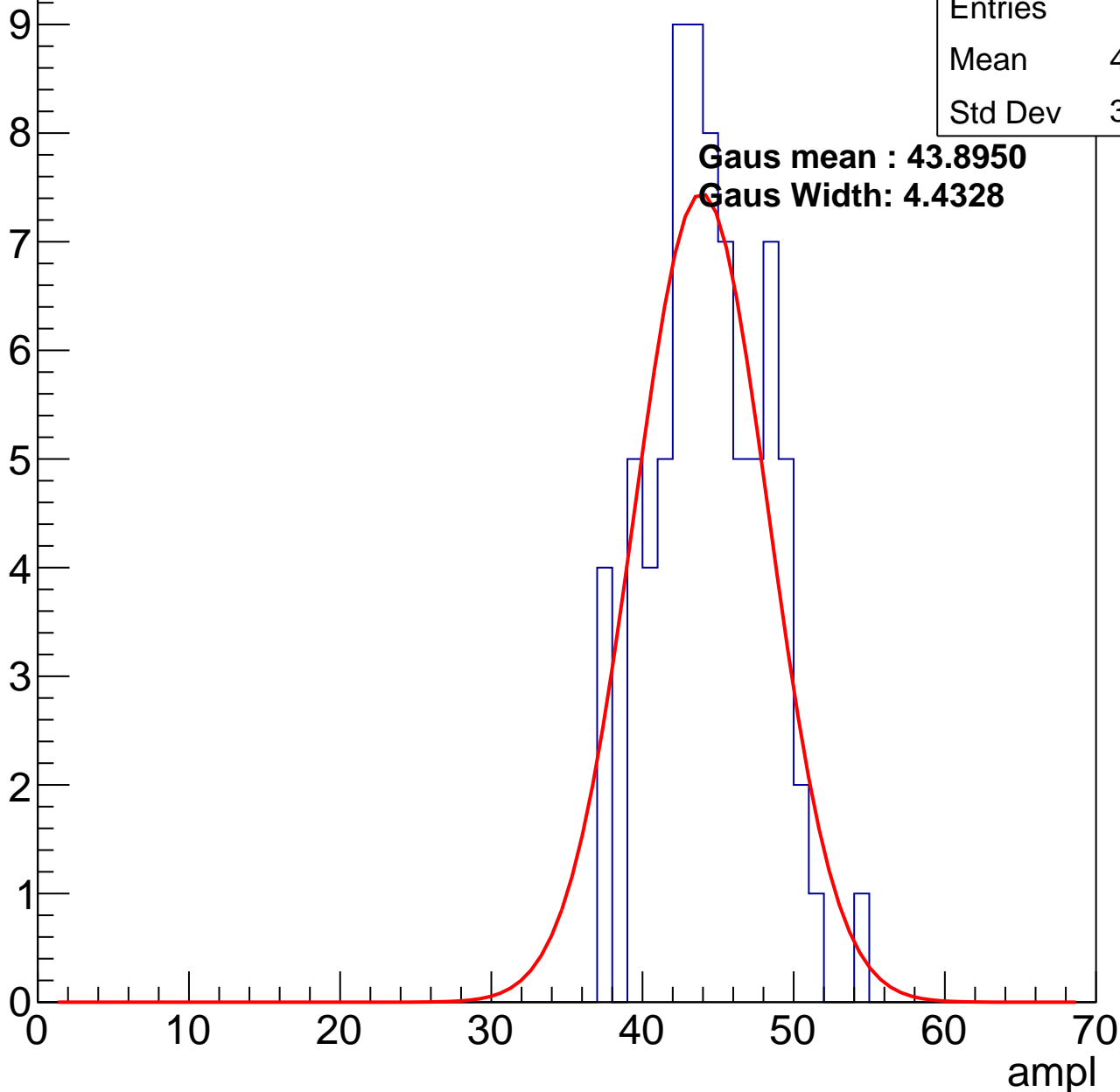
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	77
Mean	44.04
Std Dev	3.613

**Gaus mean : 43.8950**

**Gaus Width: 4.4328**

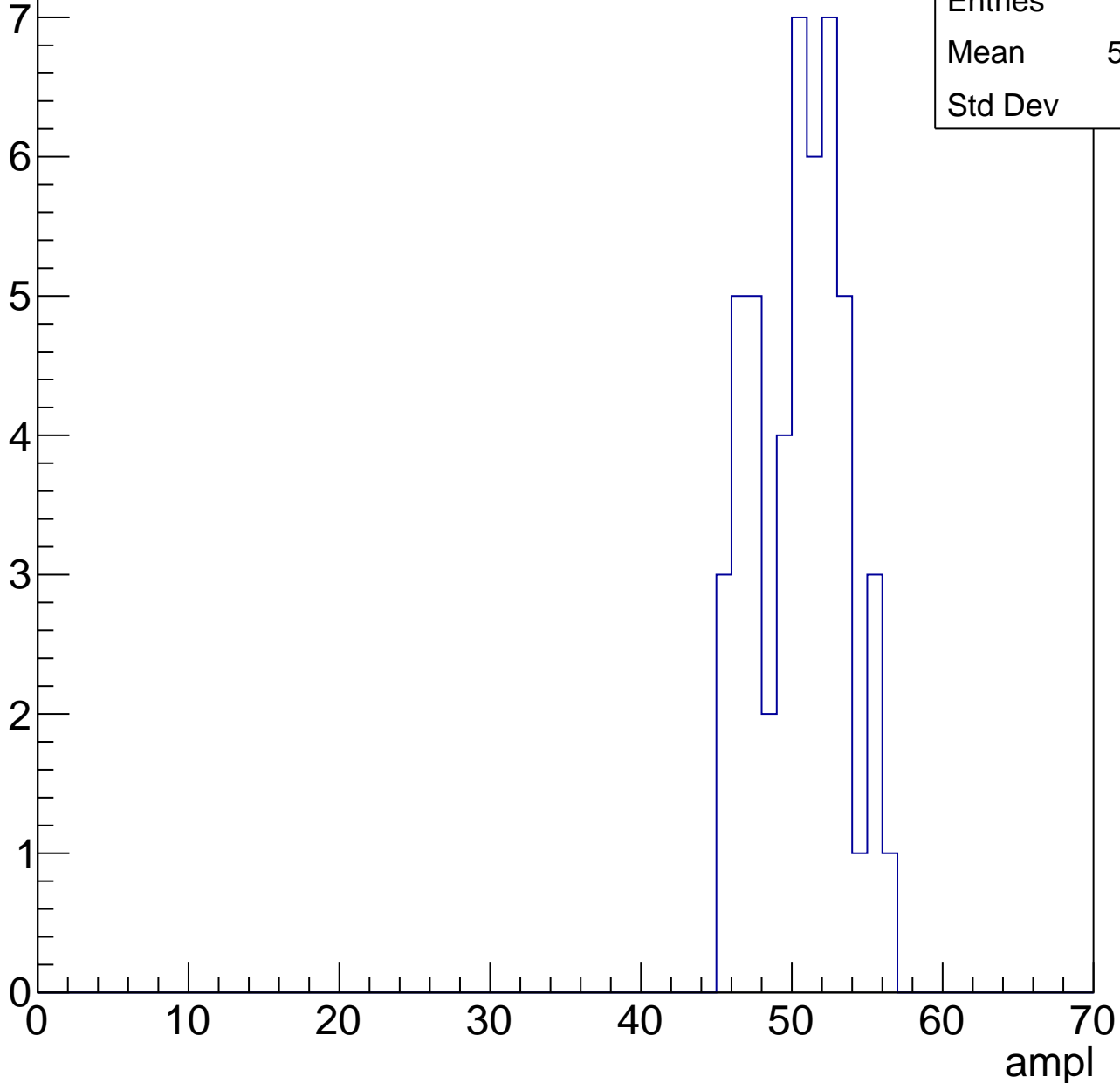


# B0L001S, U24-ch54, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	49
Mean	50.04
Std Dev	2.92

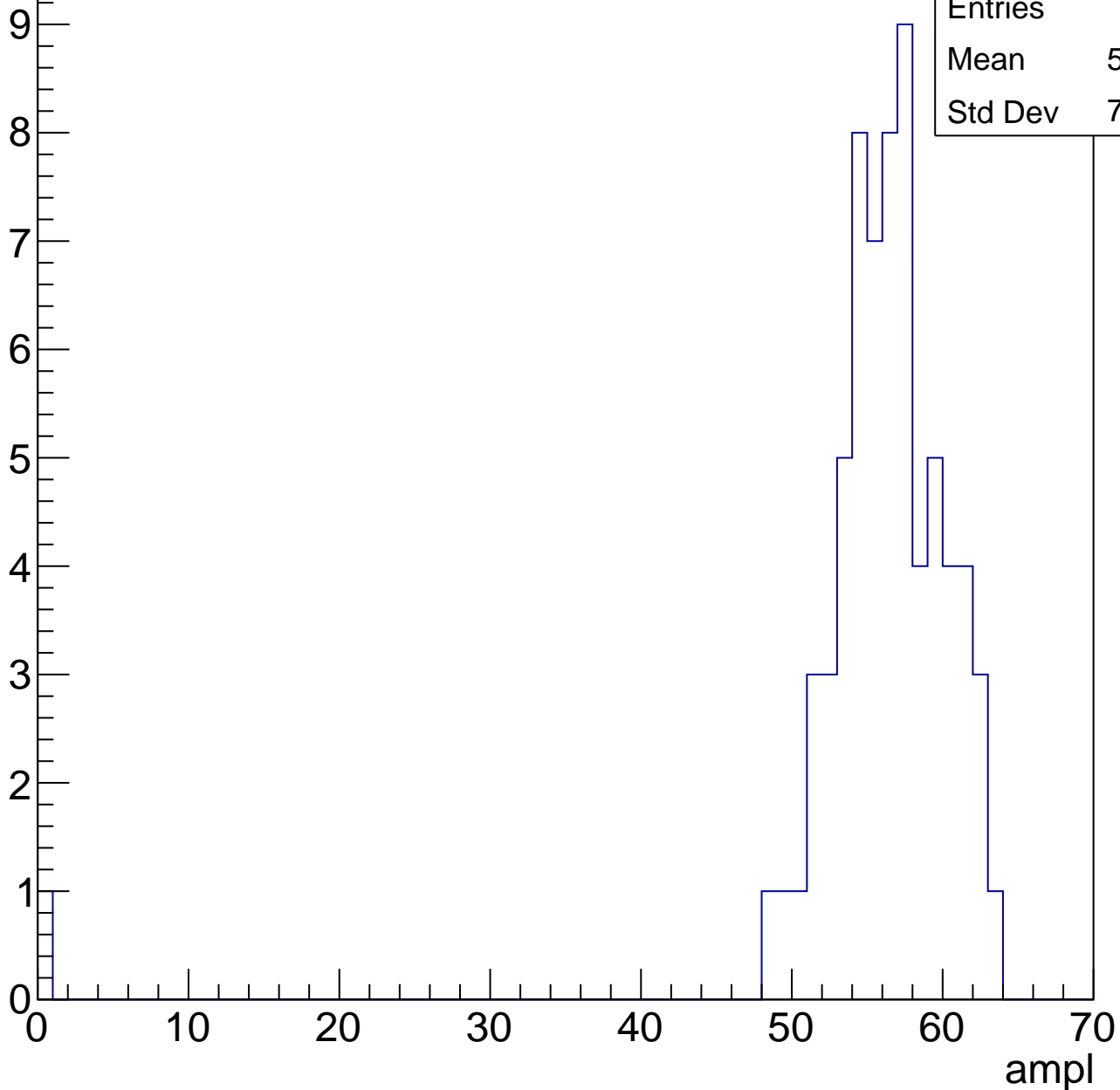


# B0L001S, U24-ch54, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	55.28
Std Dev	7.522

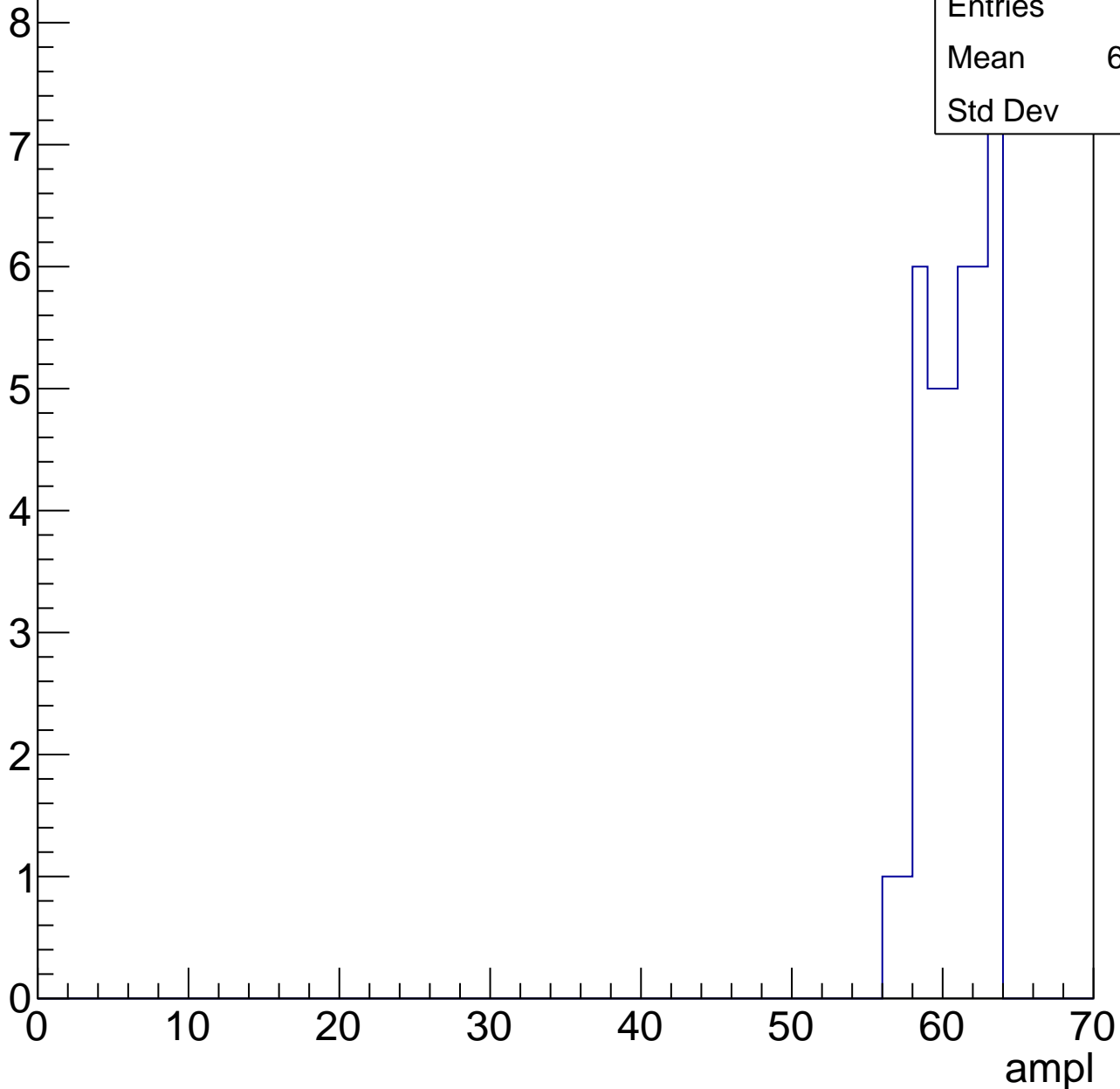


# B0L001S, U24-ch54, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	38
Mean	60.47
Std Dev	1.97



# B0L001S, U24-ch54, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch54, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

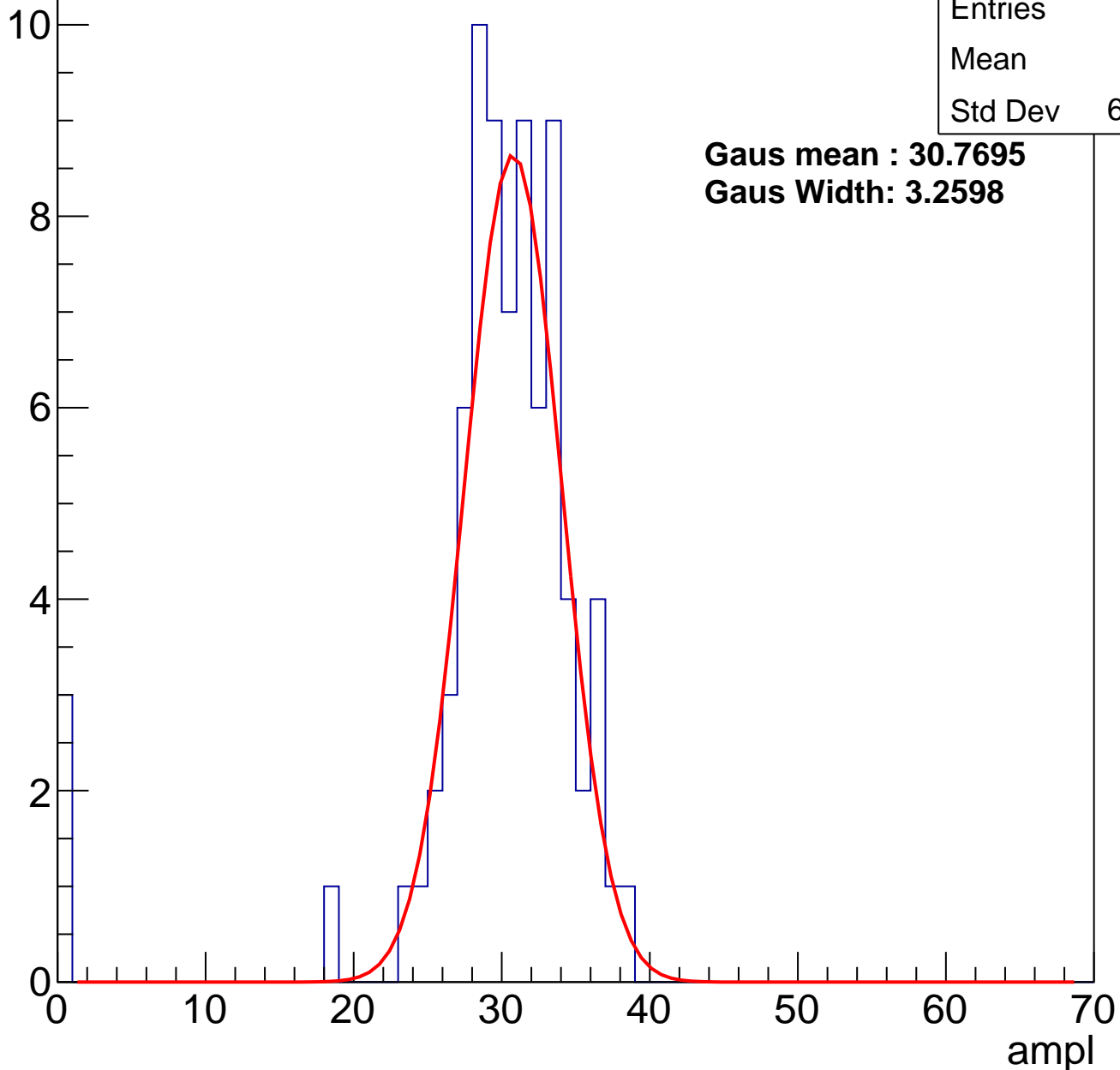
# B0L001S, U24-ch55, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	79
Mean	29.1
Std Dev	6.705

**Gaus mean : 30.7695**  
**Gaus Width: 3.2598**

Entry



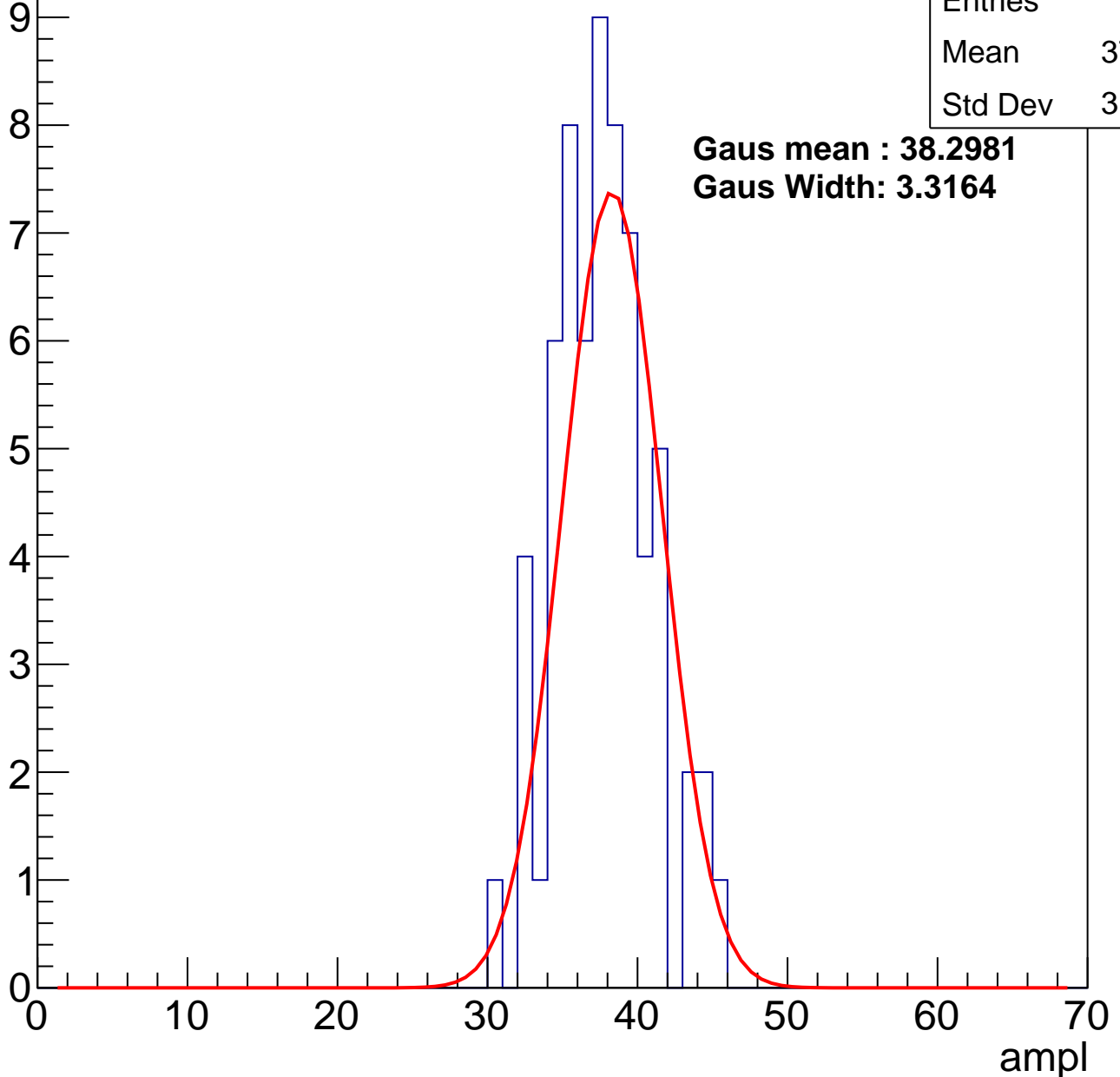
# B0L001S, U24-ch55, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	37.27
Std Dev	3.159

**Gaus mean : 38.2981**  
**Gaus Width: 3.3164**



# B0L001S, U24-ch55, adc2

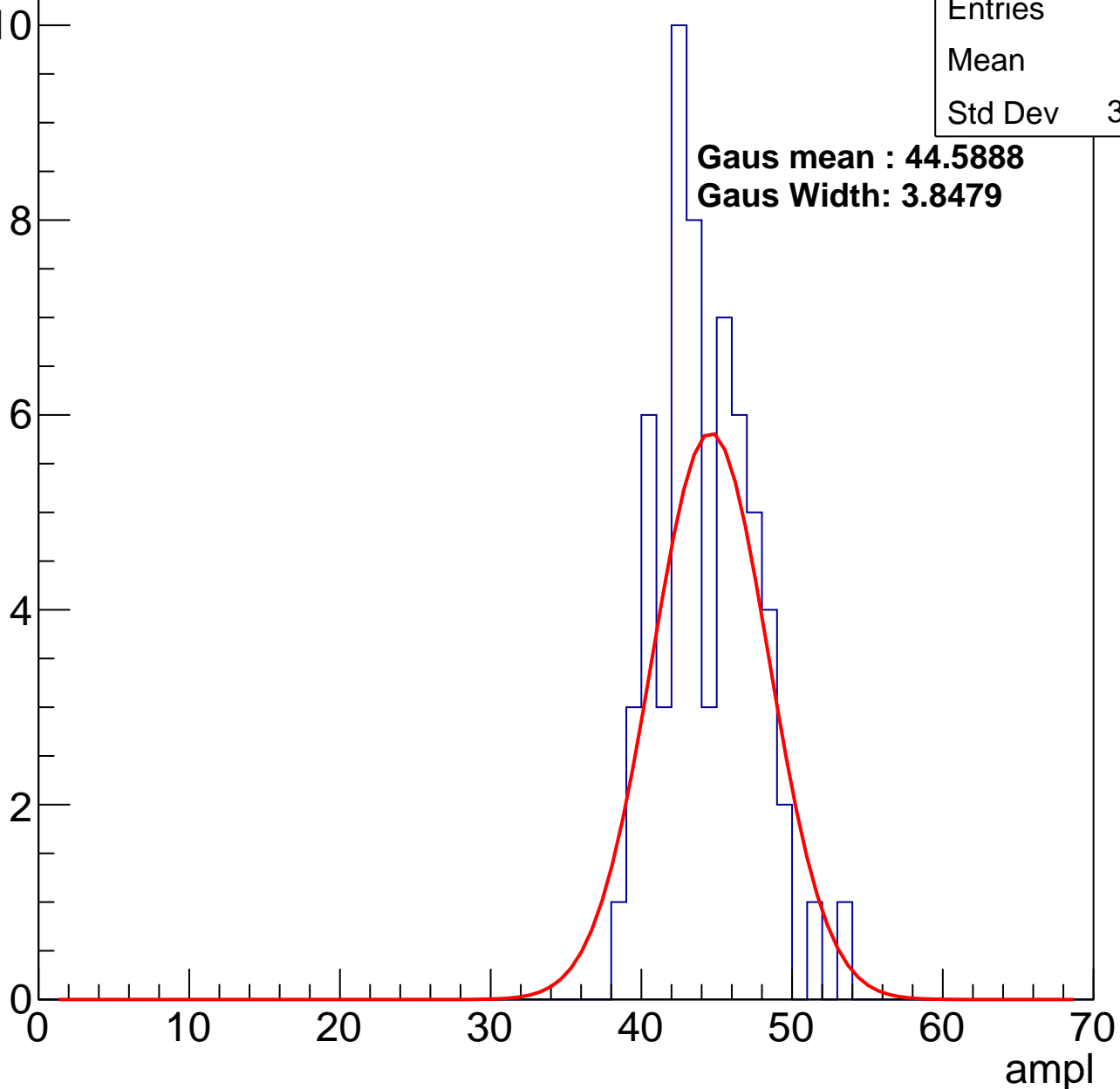
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	43.9
Std Dev	3.166

**Gaus mean : 44.5888**

**Gaus Width: 3.8479**



# B0L001S, U24-ch55, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

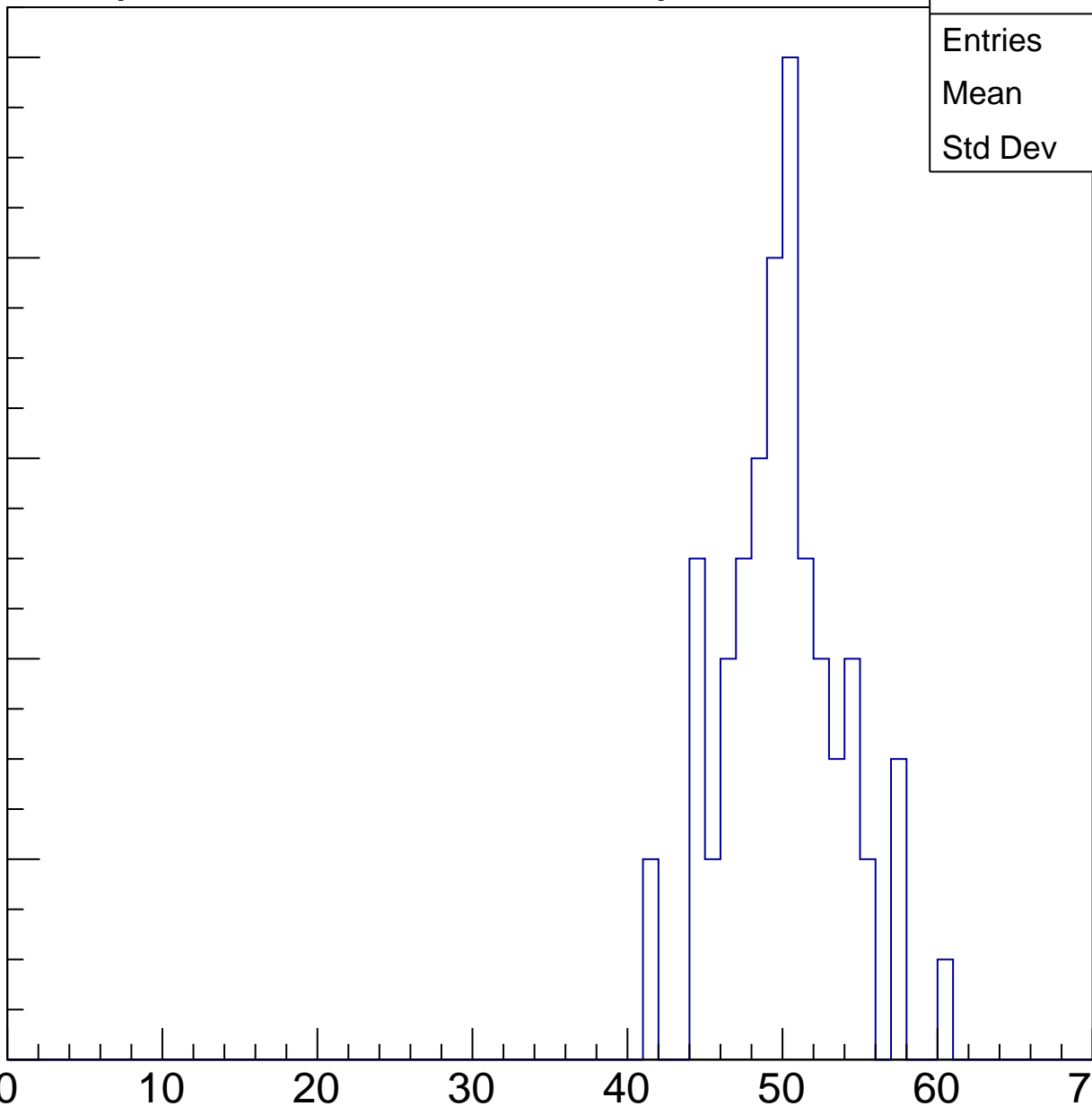
Entries	64
Mean	49.53
Std Dev	3.808

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

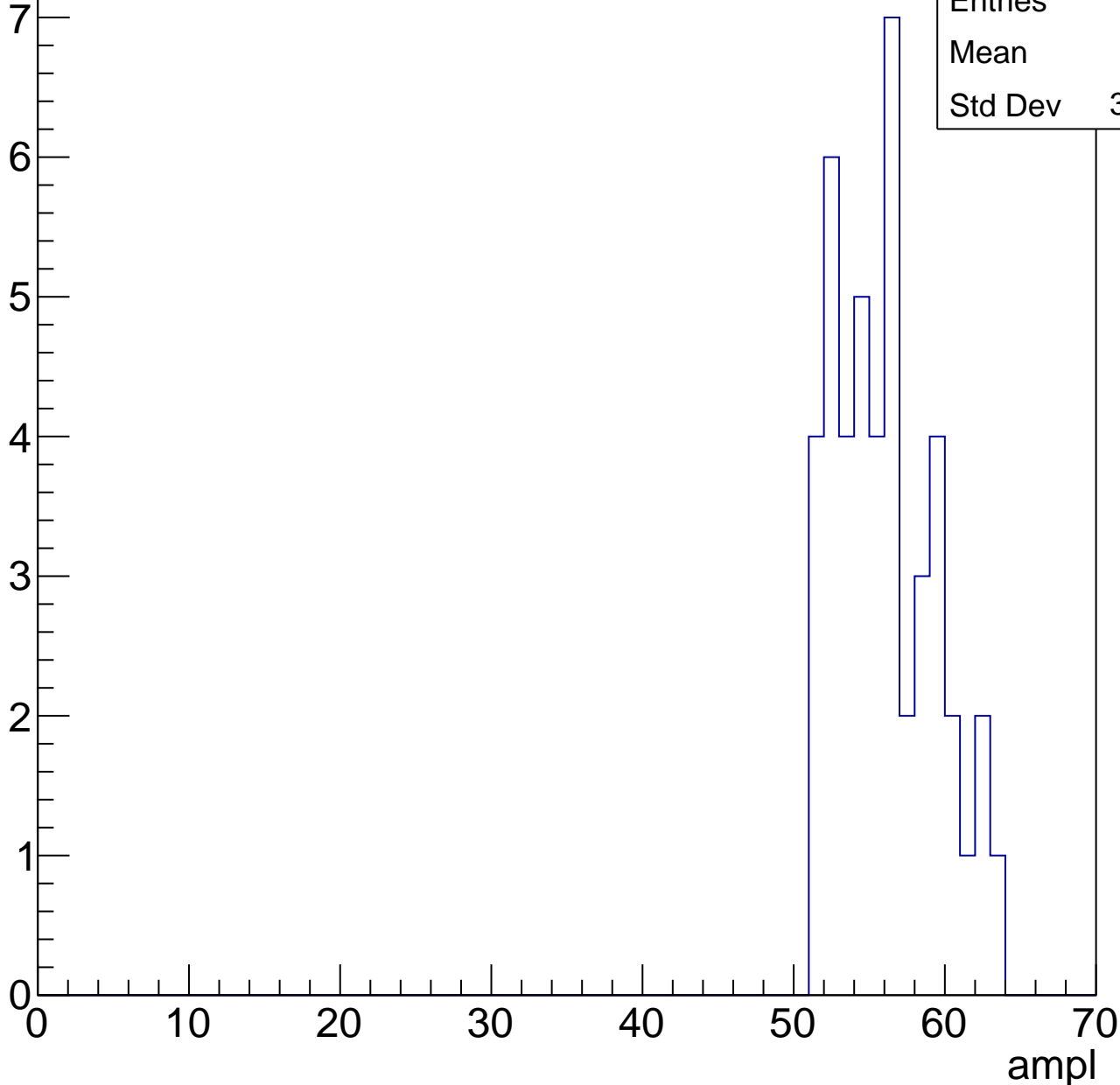


# B0L001S, U24-ch55, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	45
Mean	55.6
Std Dev	3.255

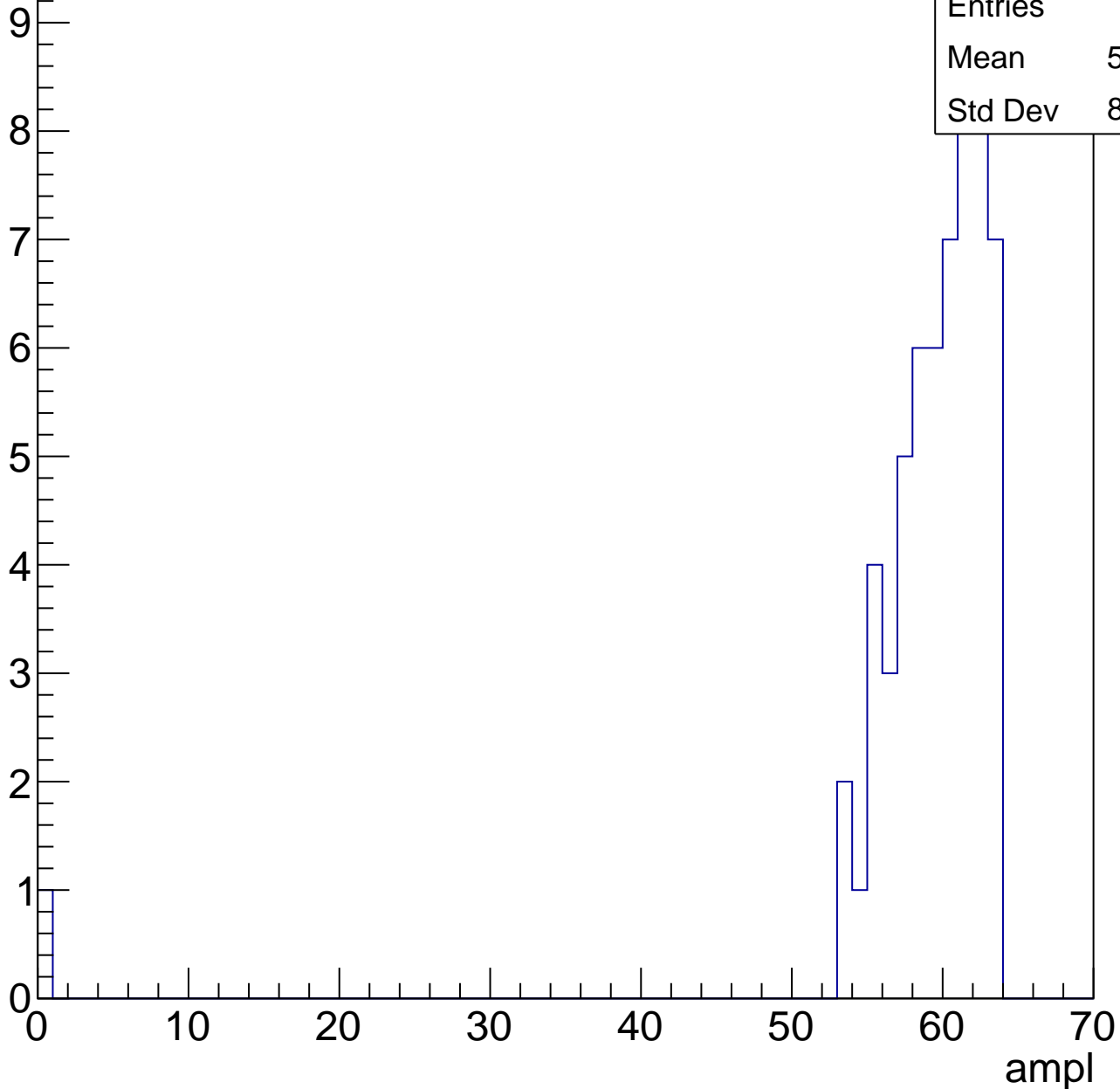


# B0L001S, U24-ch55, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

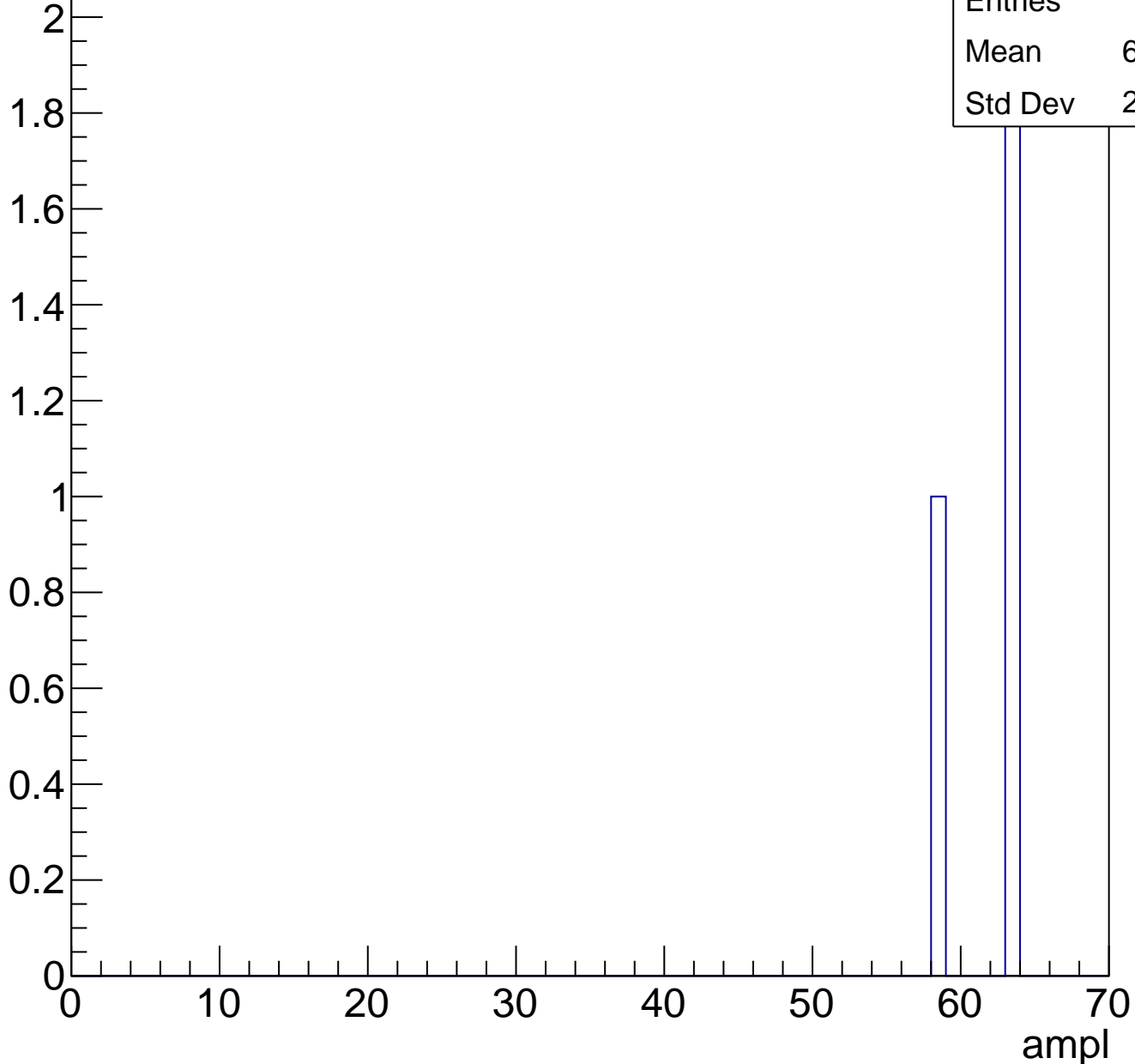
Entries	59
Mean	58.32
Std Dev	8.125



# B0L001S, U24-ch55, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	3
Mean	61.33
Std Dev	2.357



# B0L001S, U24-ch55, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L001S, U24-ch56, adc0

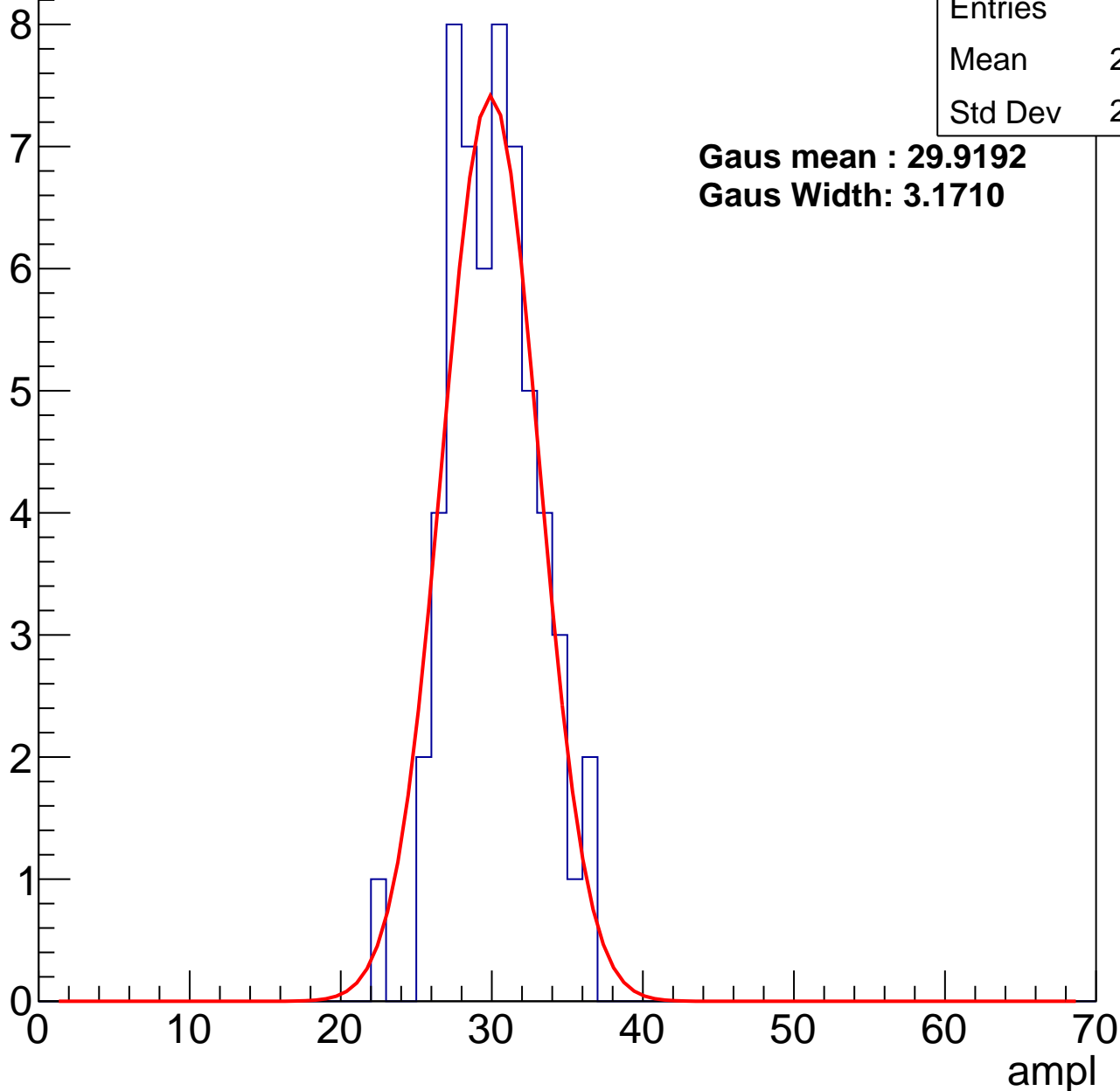
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	29.66
Std Dev	2.892

**Gaus mean : 29.9192**

**Gaus Width: 3.1710**



# B0L001S, U24-ch56, adc1

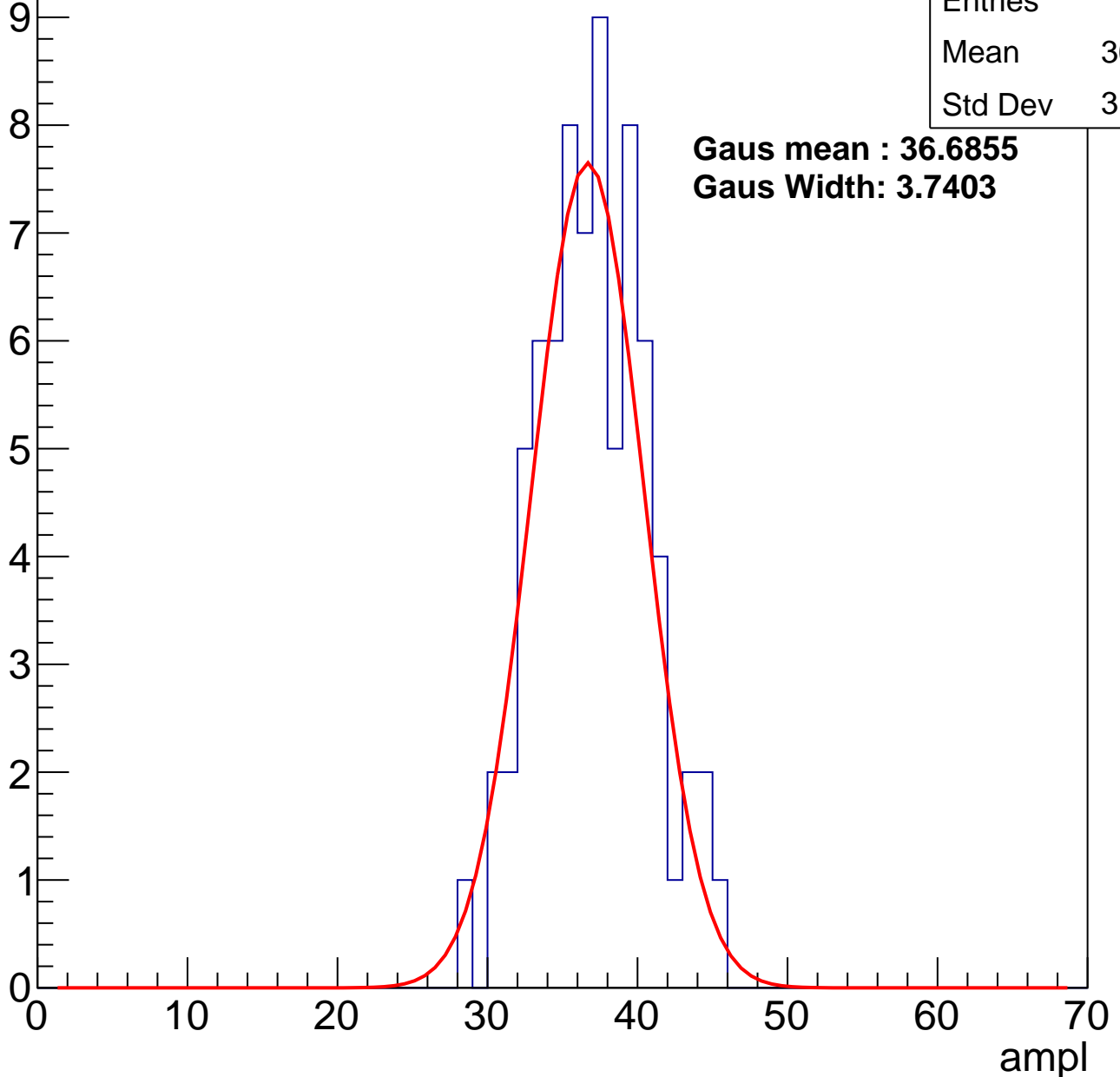
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	75
Mean	36.59
Std Dev	3.589

**Gaus mean : 36.6855**

**Gaus Width: 3.7403**



# B0L001S, U24-ch56, adc2

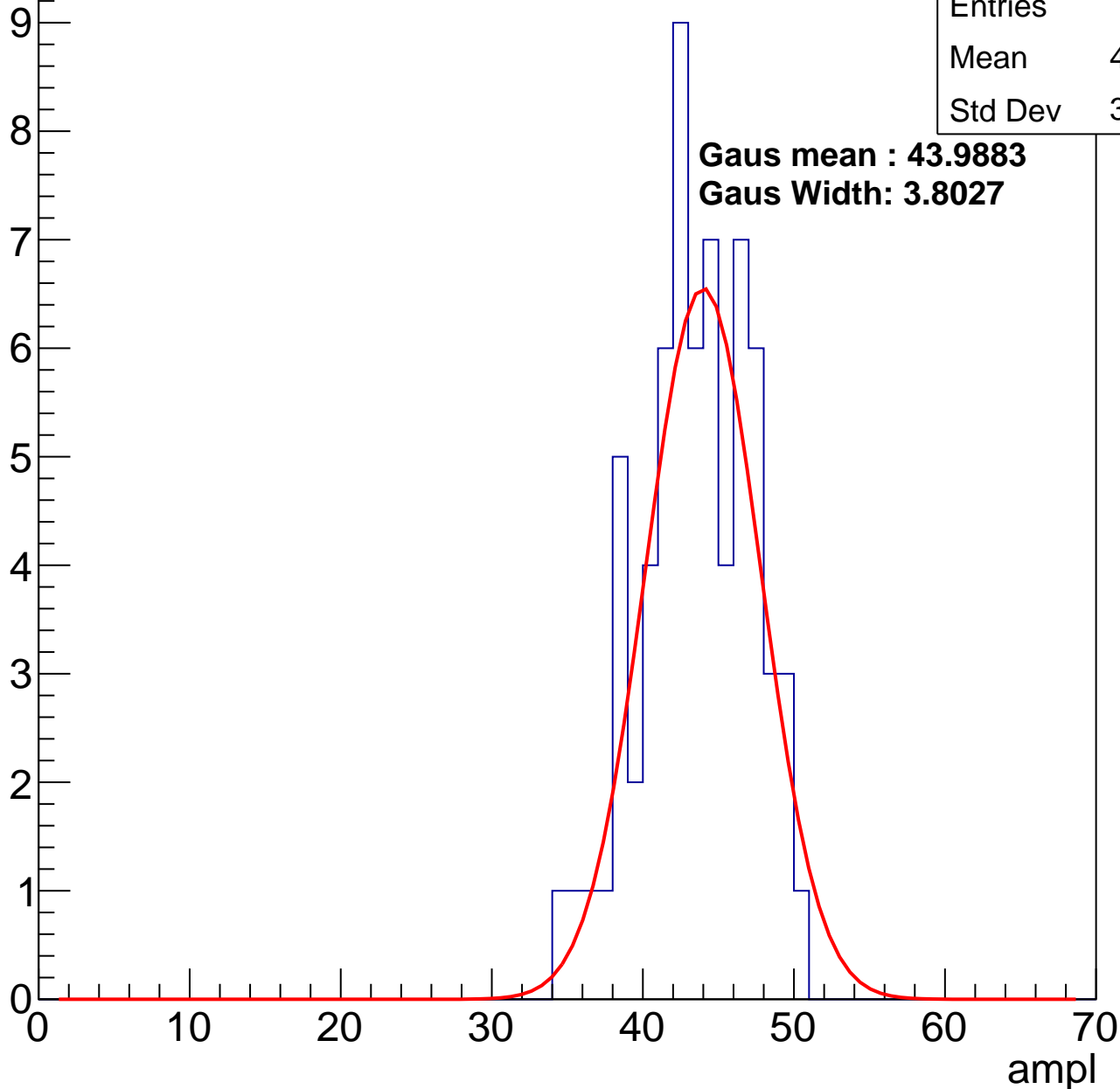
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	43.06
Std Dev	3.603

**Gaus mean : 43.9883**

**Gaus Width: 3.8027**

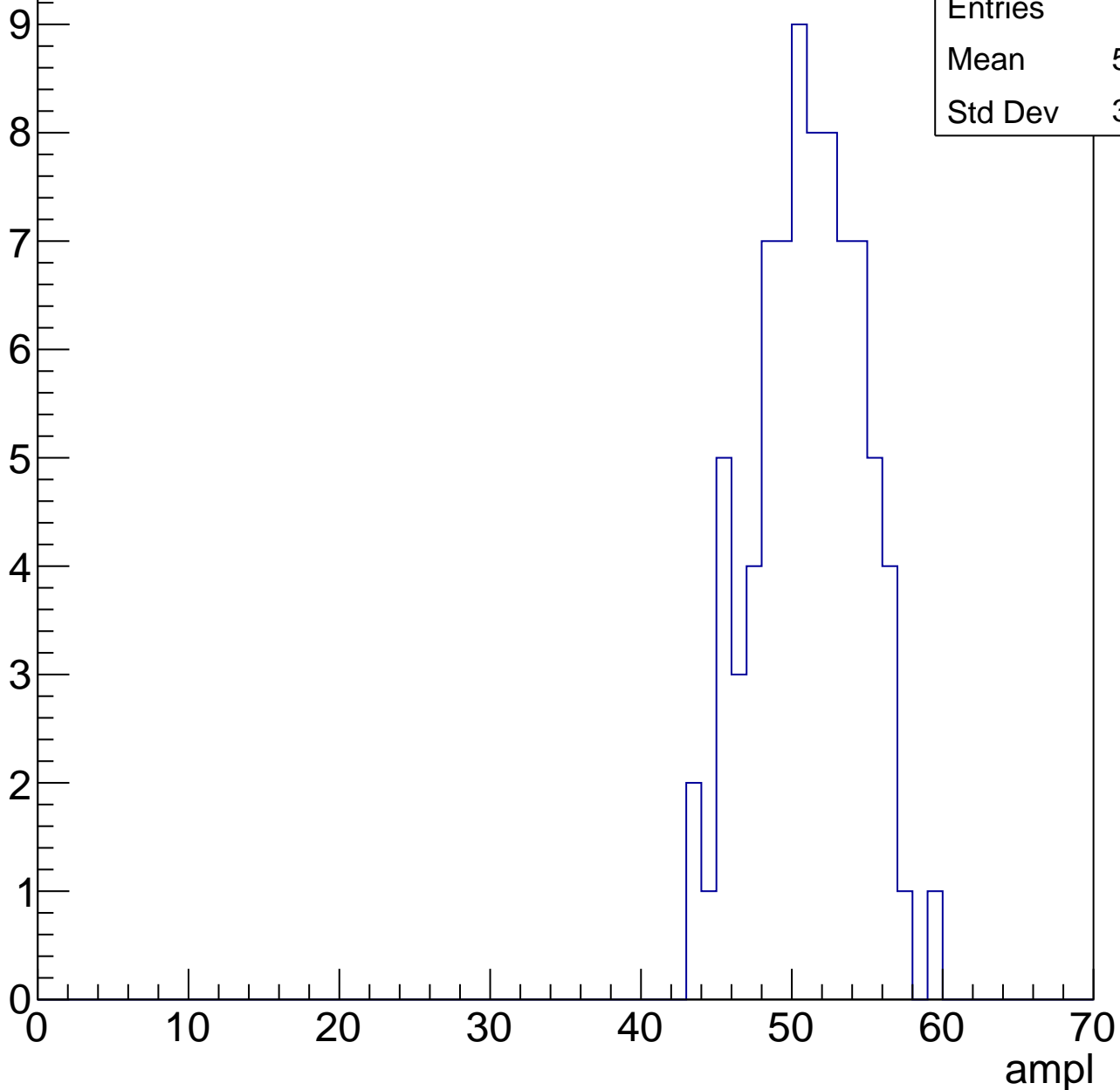


# B0L001S, U24-ch56, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	79
Mean	50.61
Std Dev	3.491

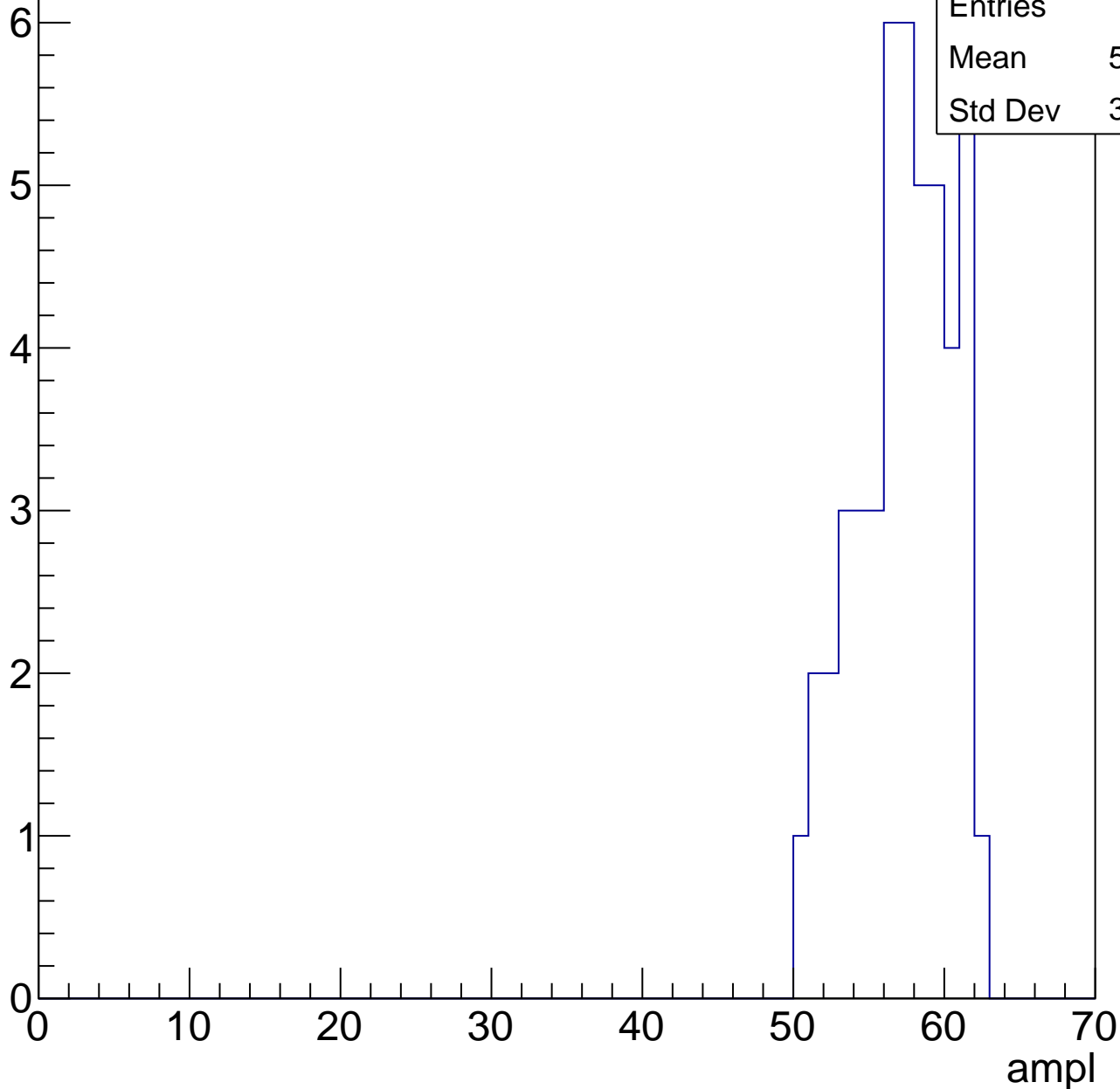


# B0L001S, U24-ch56, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	47
Mean	56.87
Std Dev	3.078

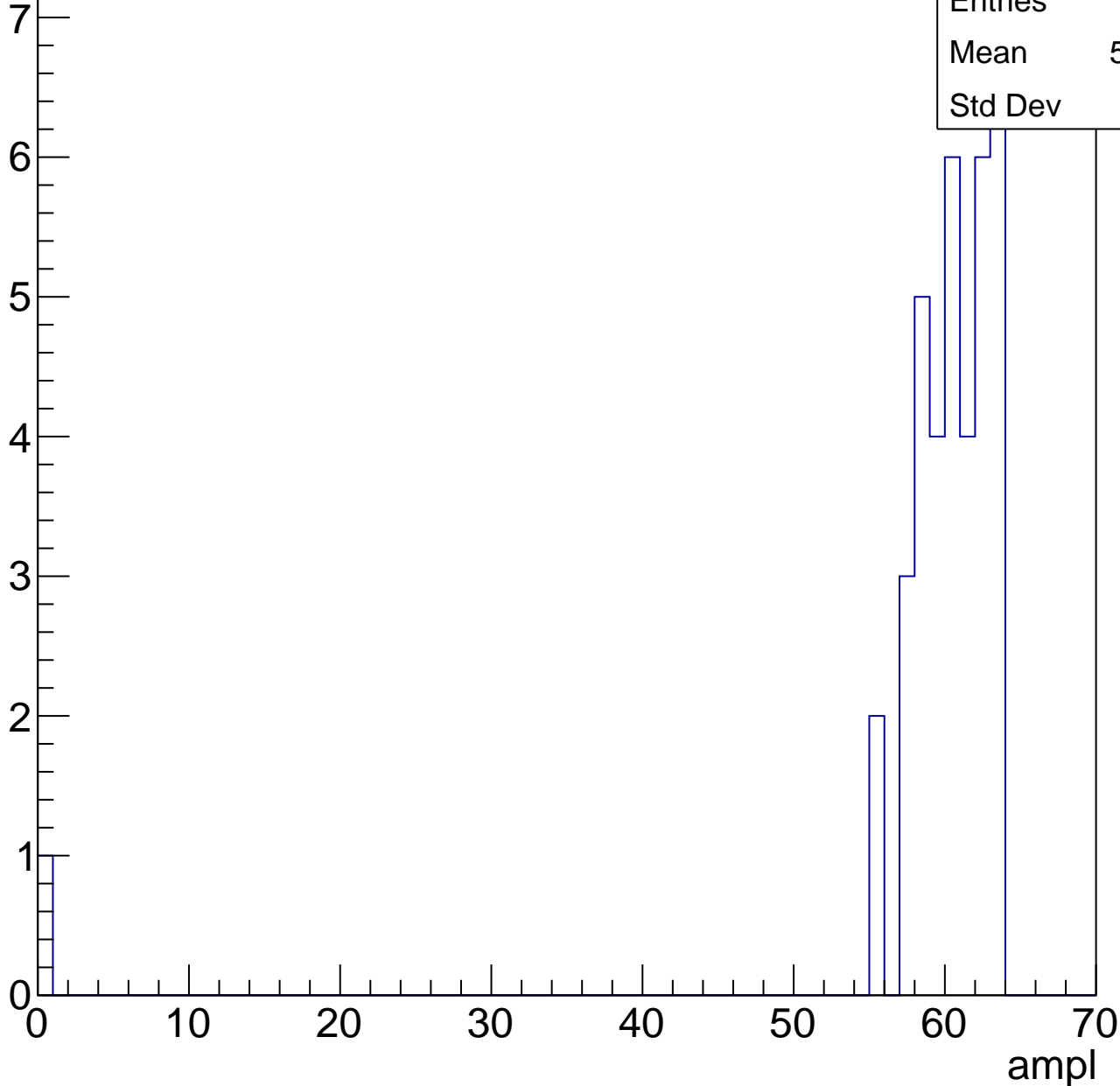


# B0L001S, U24-ch56, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	38
Mean	58.53
Std Dev	9.88



# B0L001S, U24-ch56, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch56, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U24-ch57, adc0

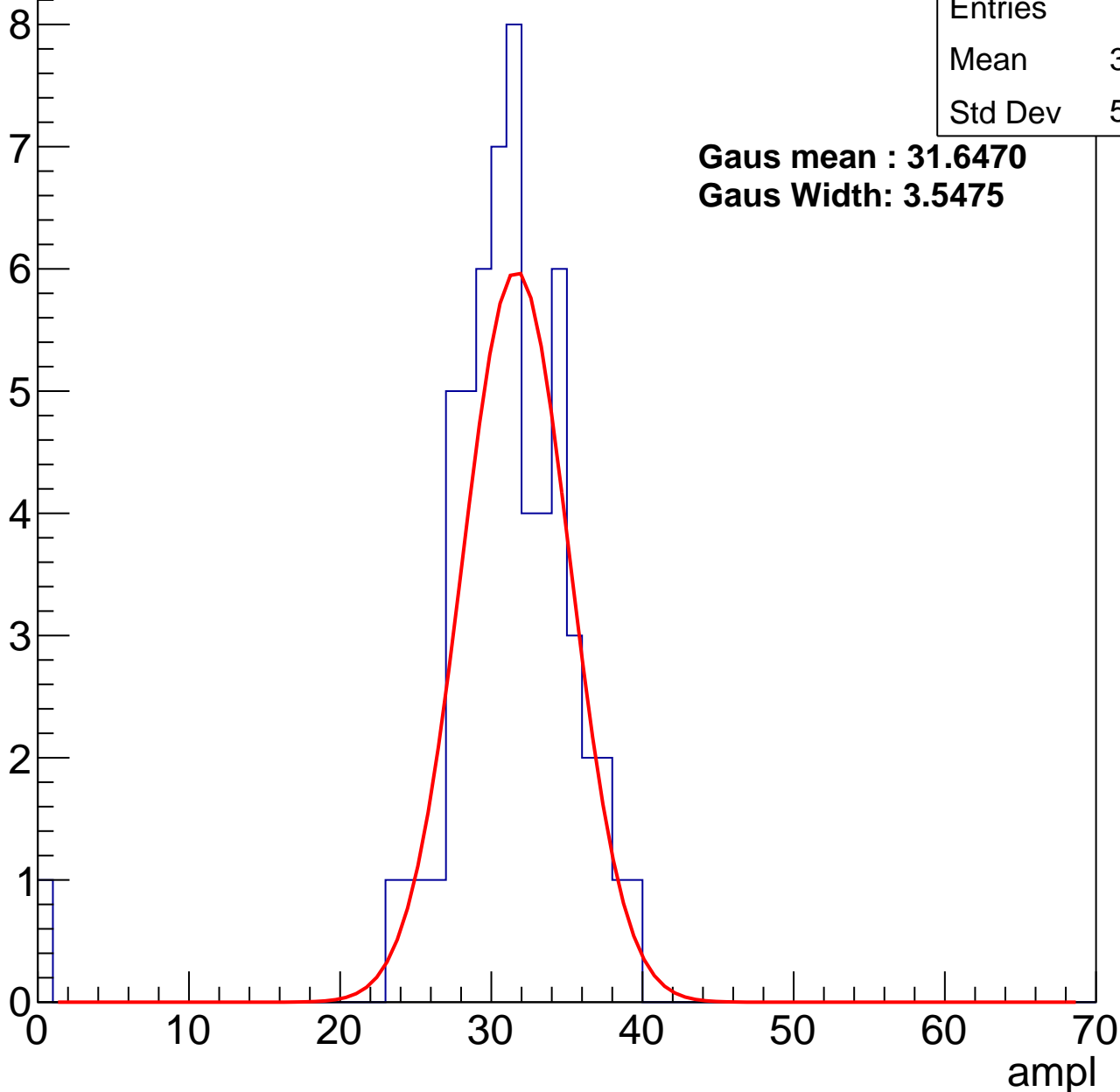
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	30.46
Std Dev	5.257

**Gaus mean : 31.6470**

**Gaus Width: 3.5475**



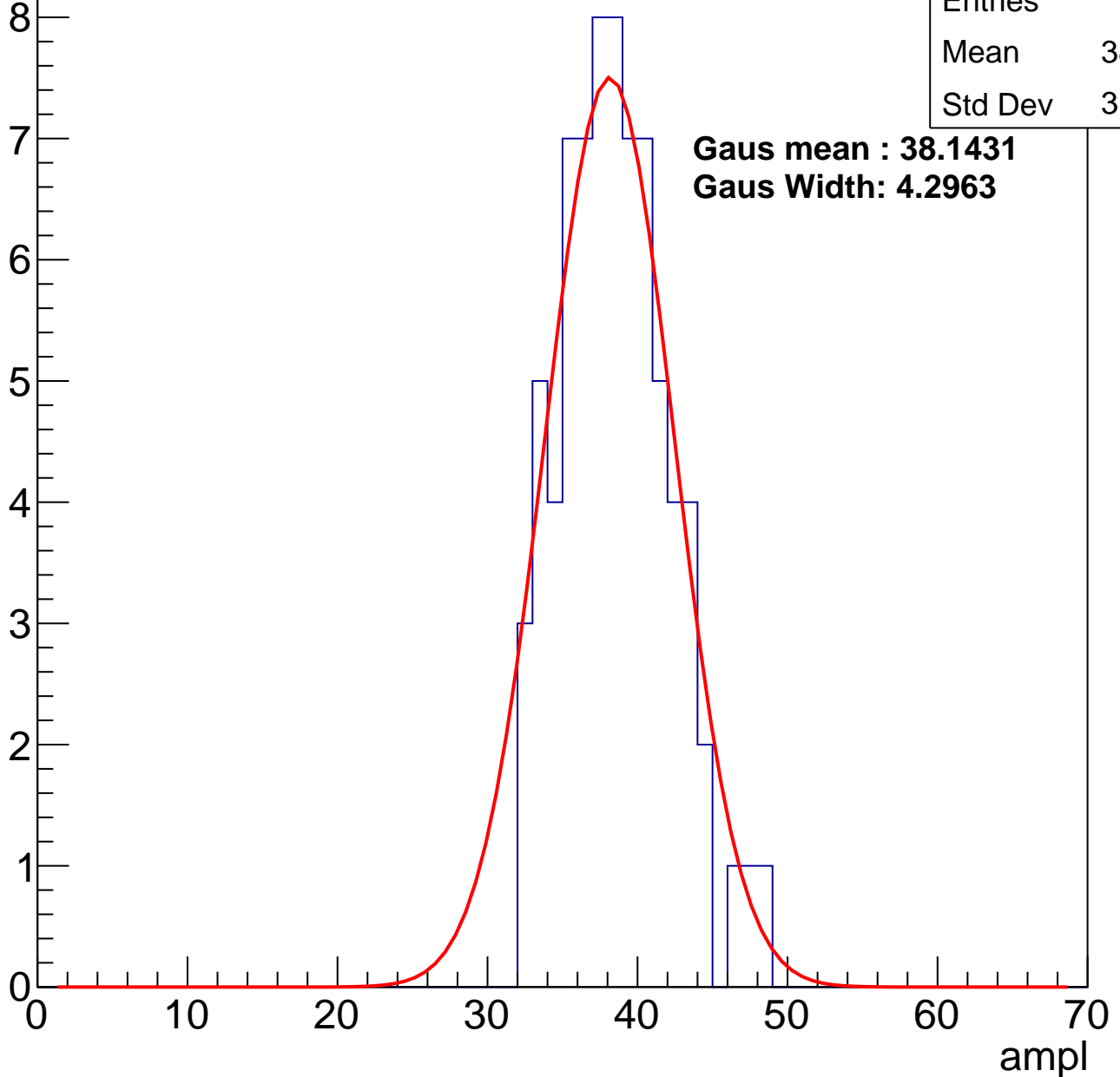
# B0L001S, U24-ch57, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	38.12
Std Dev	3.594

**Gaus mean : 38.1431**  
**Gaus Width: 4.2963**



# B0L001S, U24-ch57, adc2

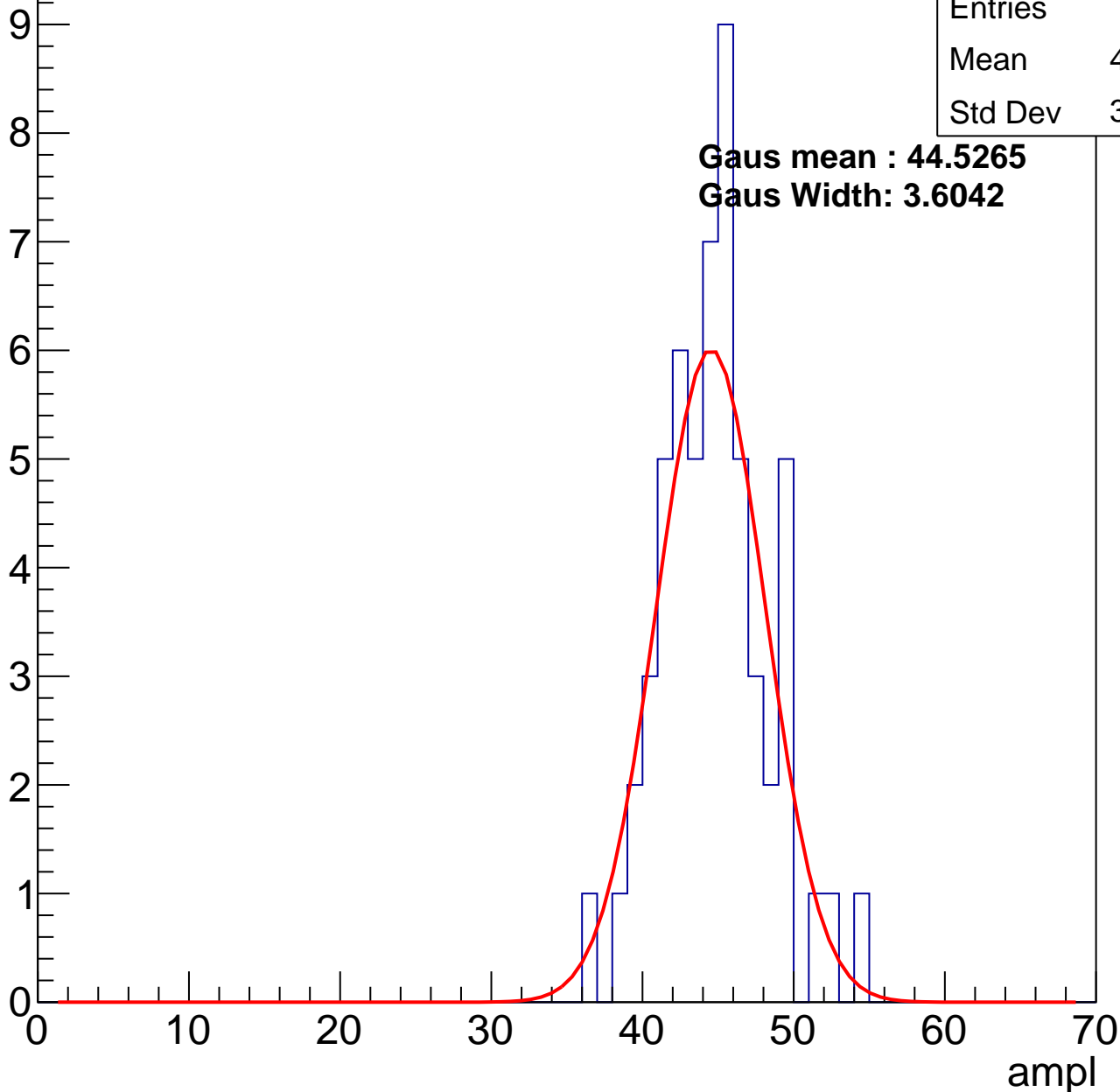
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	44.32
Std Dev	3.485

**Gaus mean : 44.5265**

**Gaus Width: 3.6042**

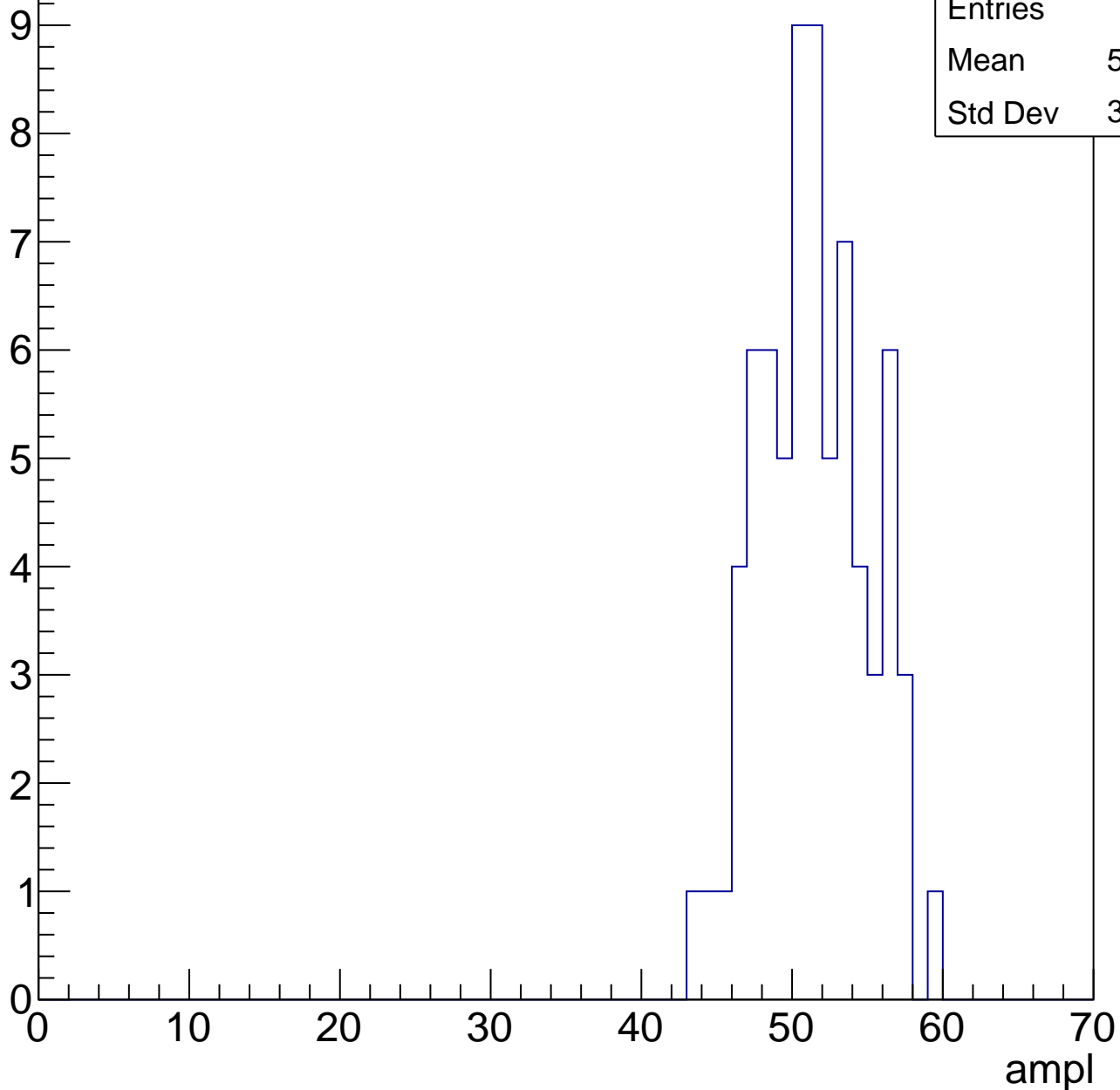


# B0L001S, U24-ch57, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	50.96
Std Dev	3.494

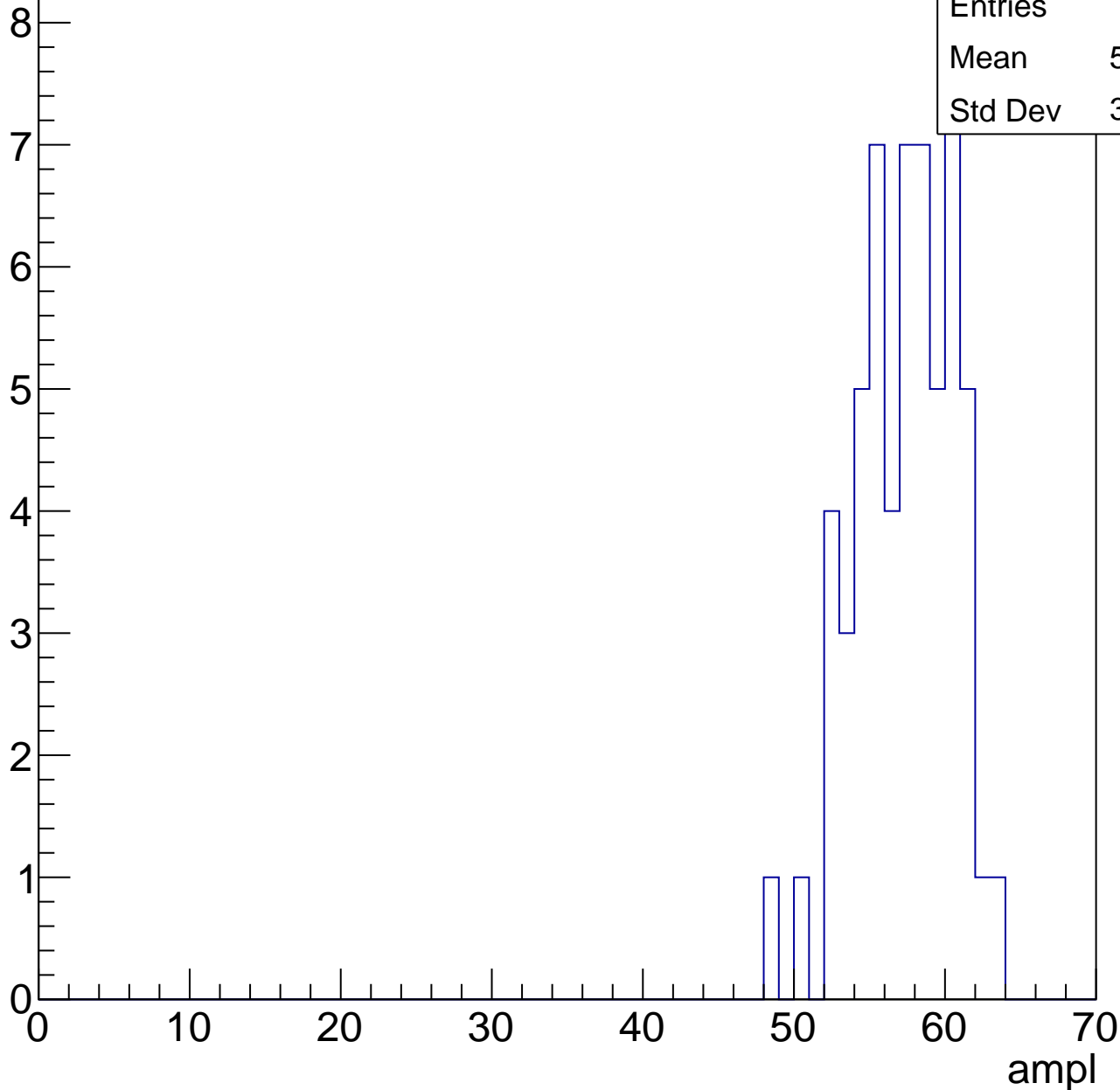


# B0L001S, U24-ch57, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	56.85
Std Dev	3.172

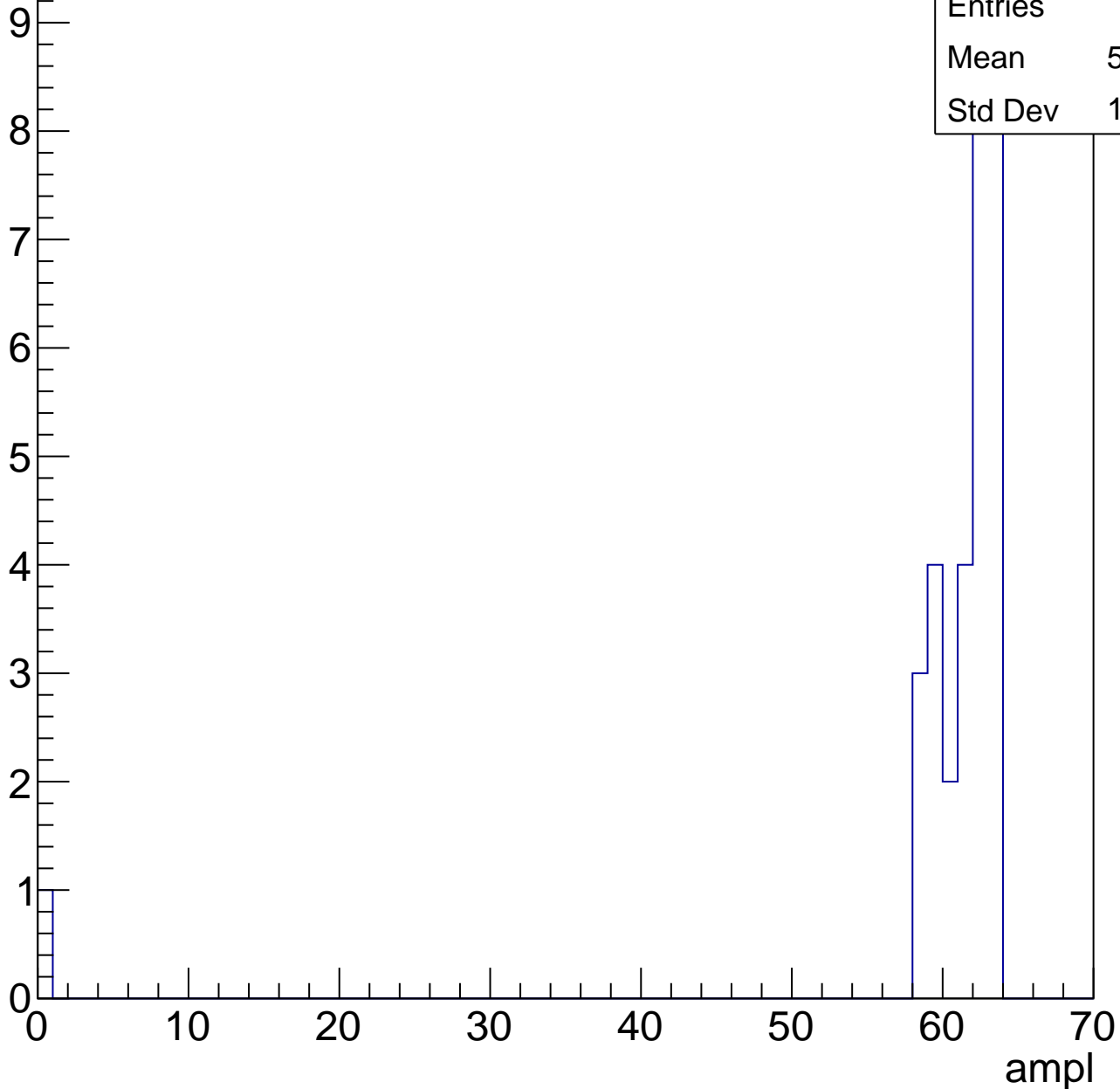


# B0L001S, U24-ch57, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	32
Mean	59.34
Std Dev	10.79



# B0L001S, U24-ch57, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch57, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U24-ch58, adc0

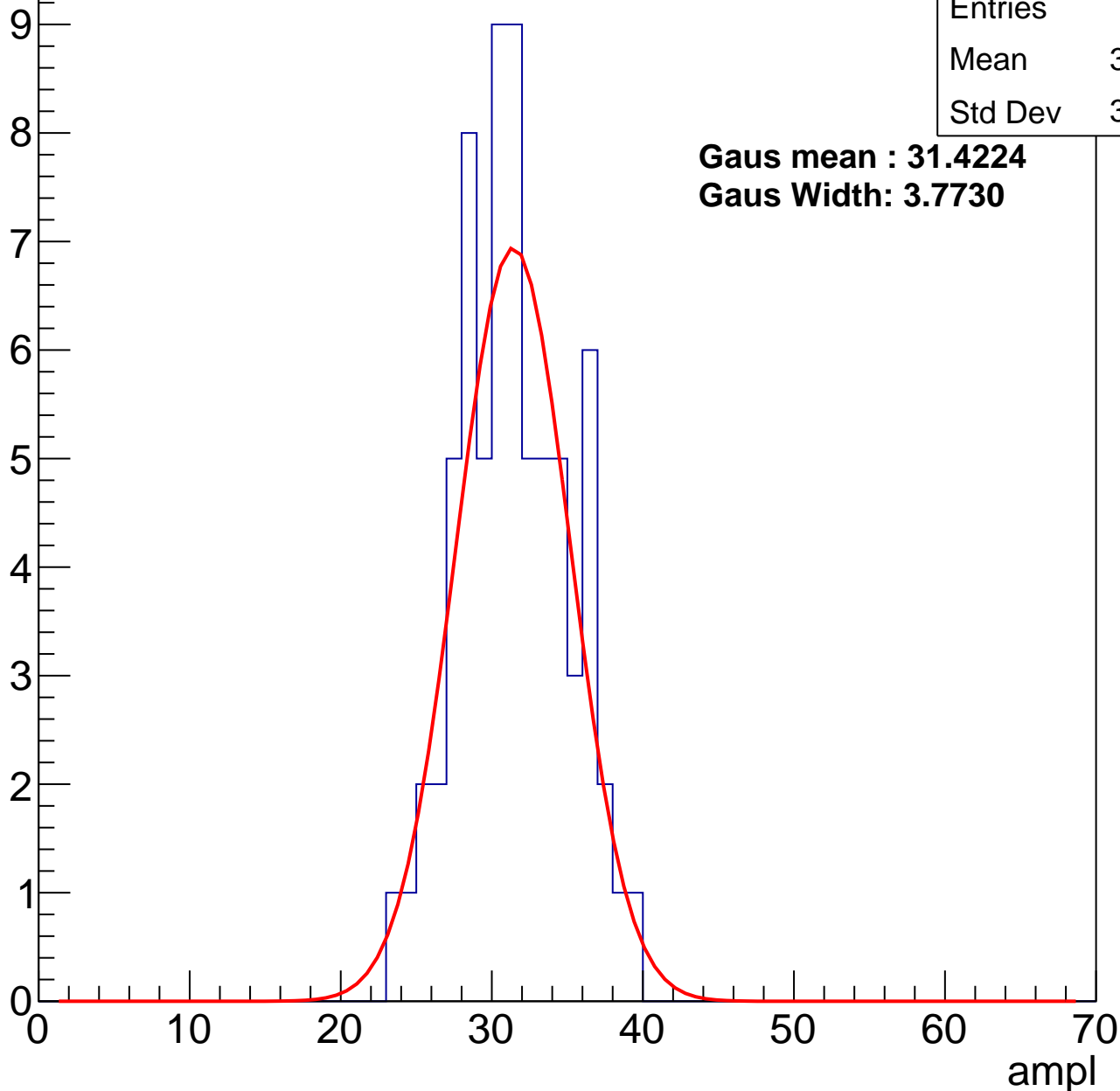
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	30.99
Std Dev	3.523

**Gaus mean : 31.4224**

**Gaus Width: 3.7730**



# B0L001S, U24-ch58, adc1

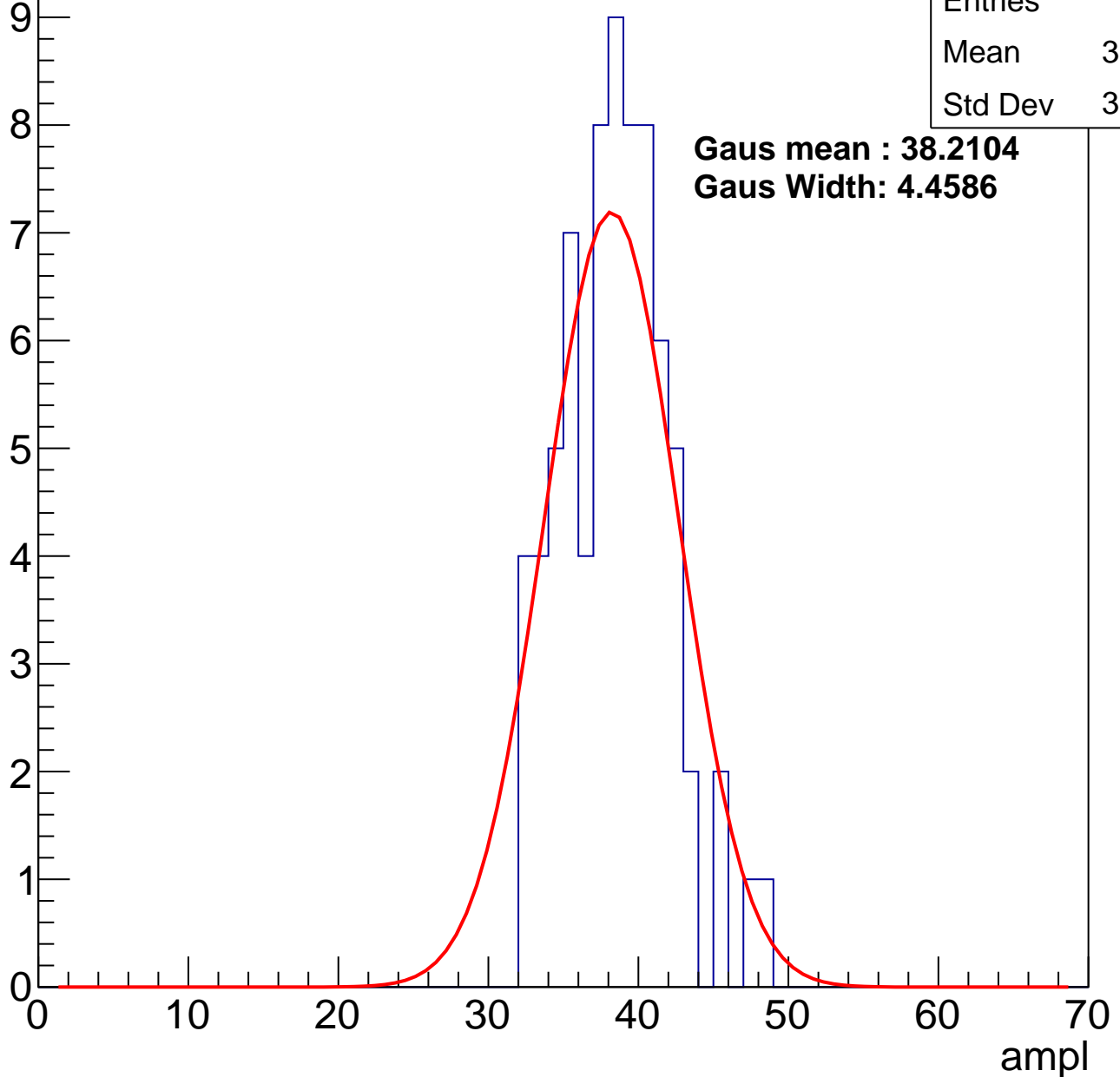
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	38.05
Std Dev	3.514

**Gaus mean : 38.2104**

**Gaus Width: 4.4586**



# B0L001S, U24-ch58, adc2

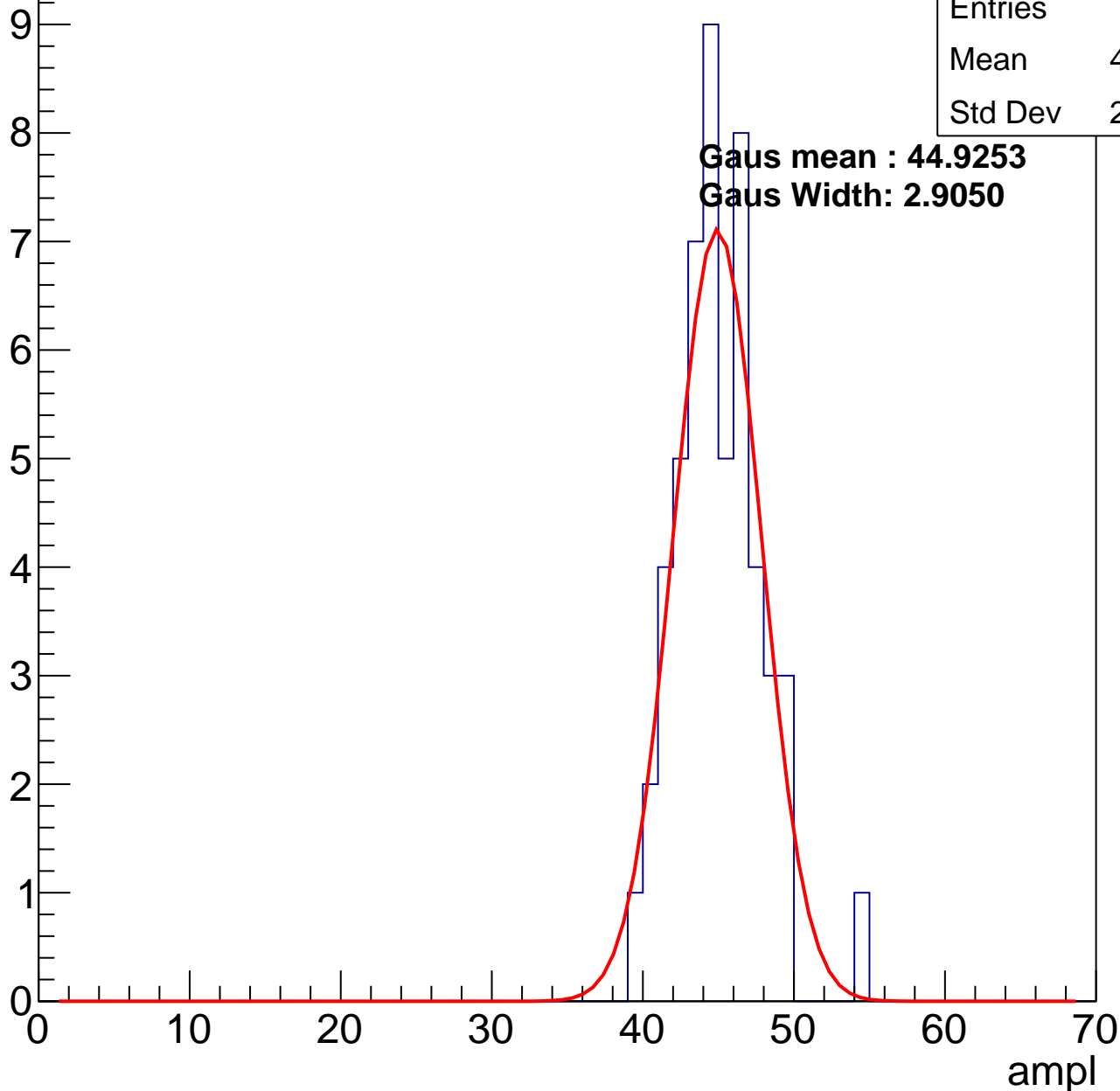
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	44.54
Std Dev	2.777

**Gaus mean : 44.9253**

**Gaus Width: 2.9050**



# B0L001S, U24-ch58, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

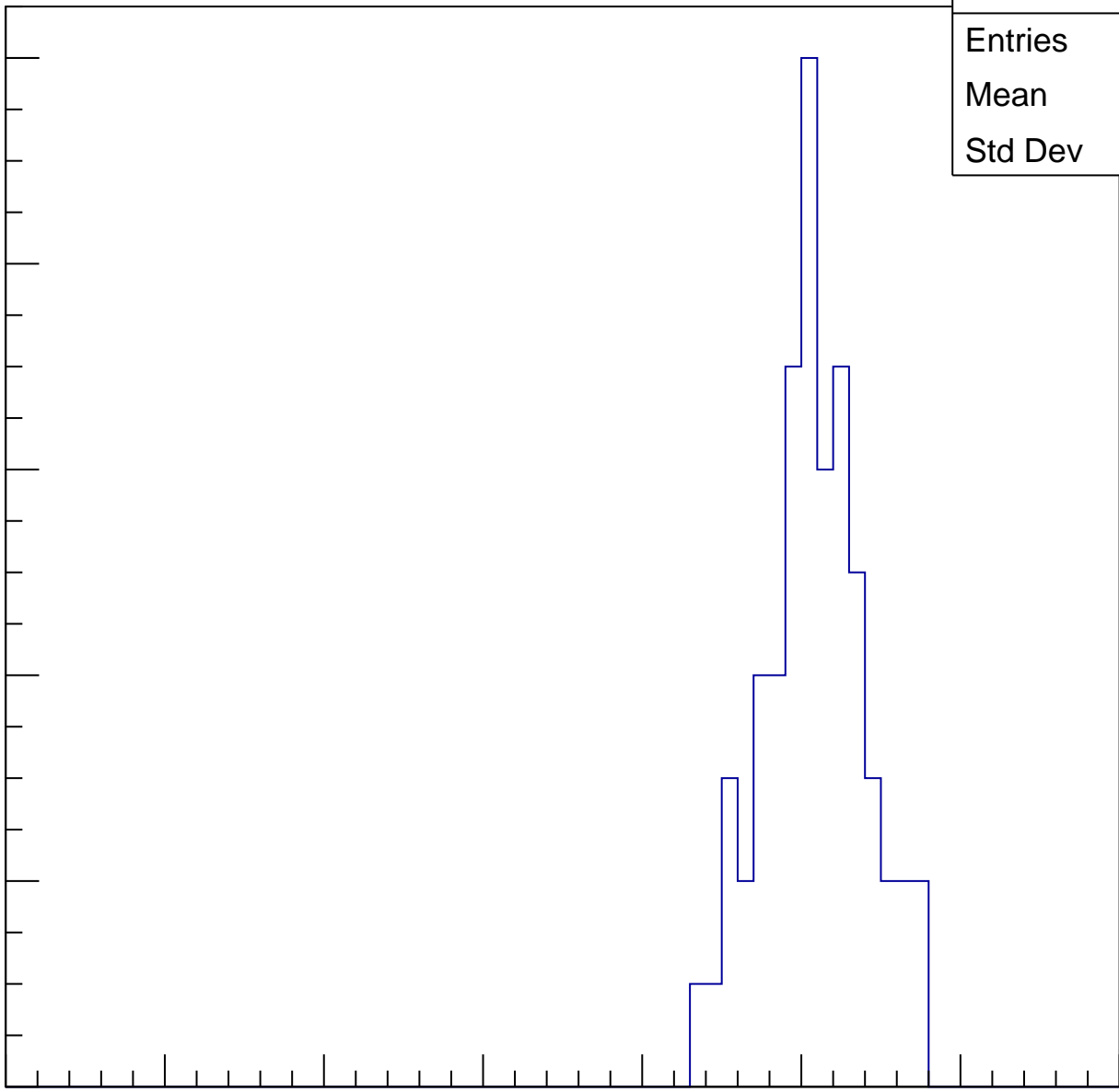
Entries	59
Mean	50.34
Std Dev	3.166

Entry

10  
8  
6  
4  
2  
0

ampl

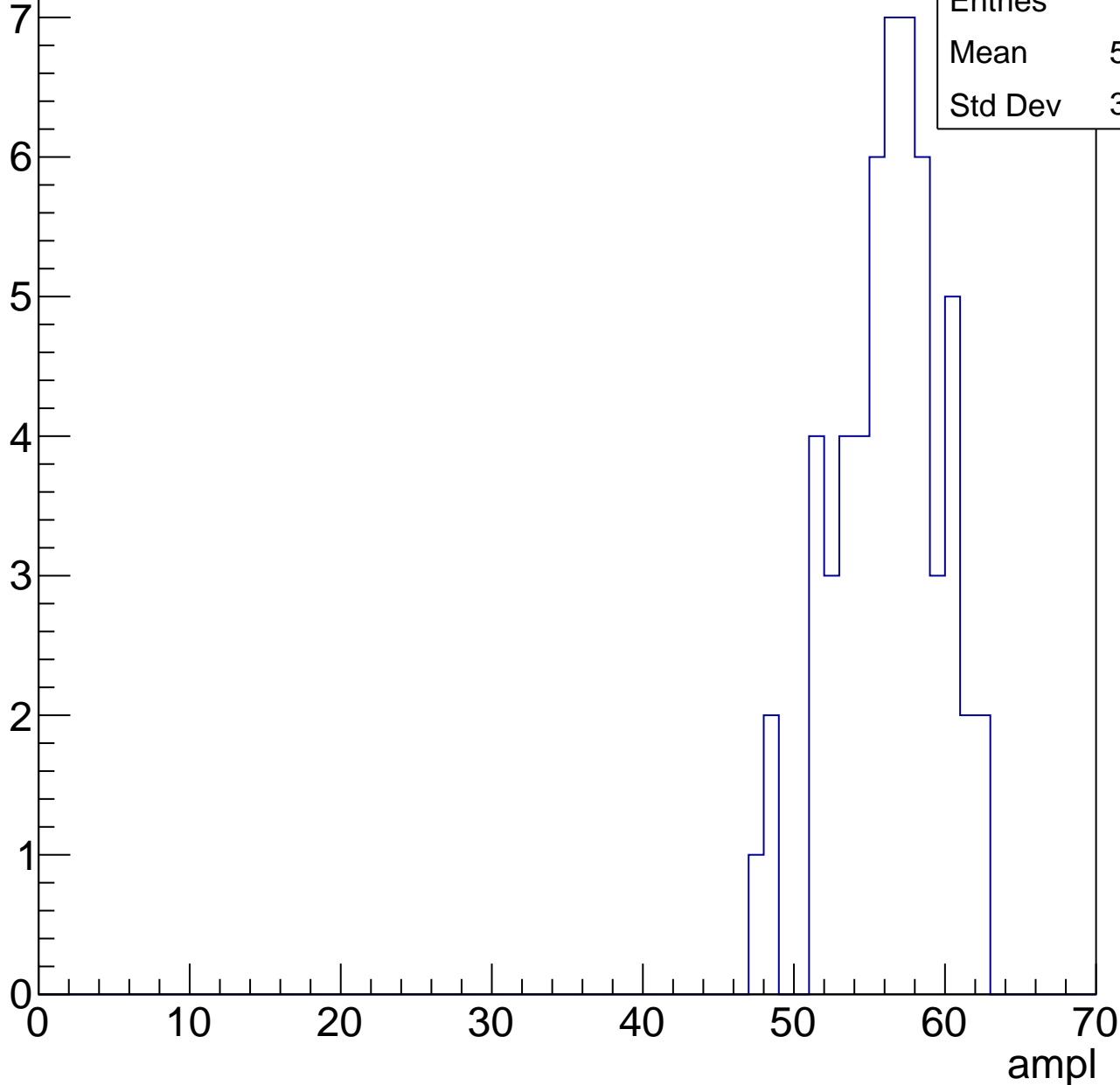
0 10 20 30 40 50 60 70



# B0L001S, U24-ch58, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

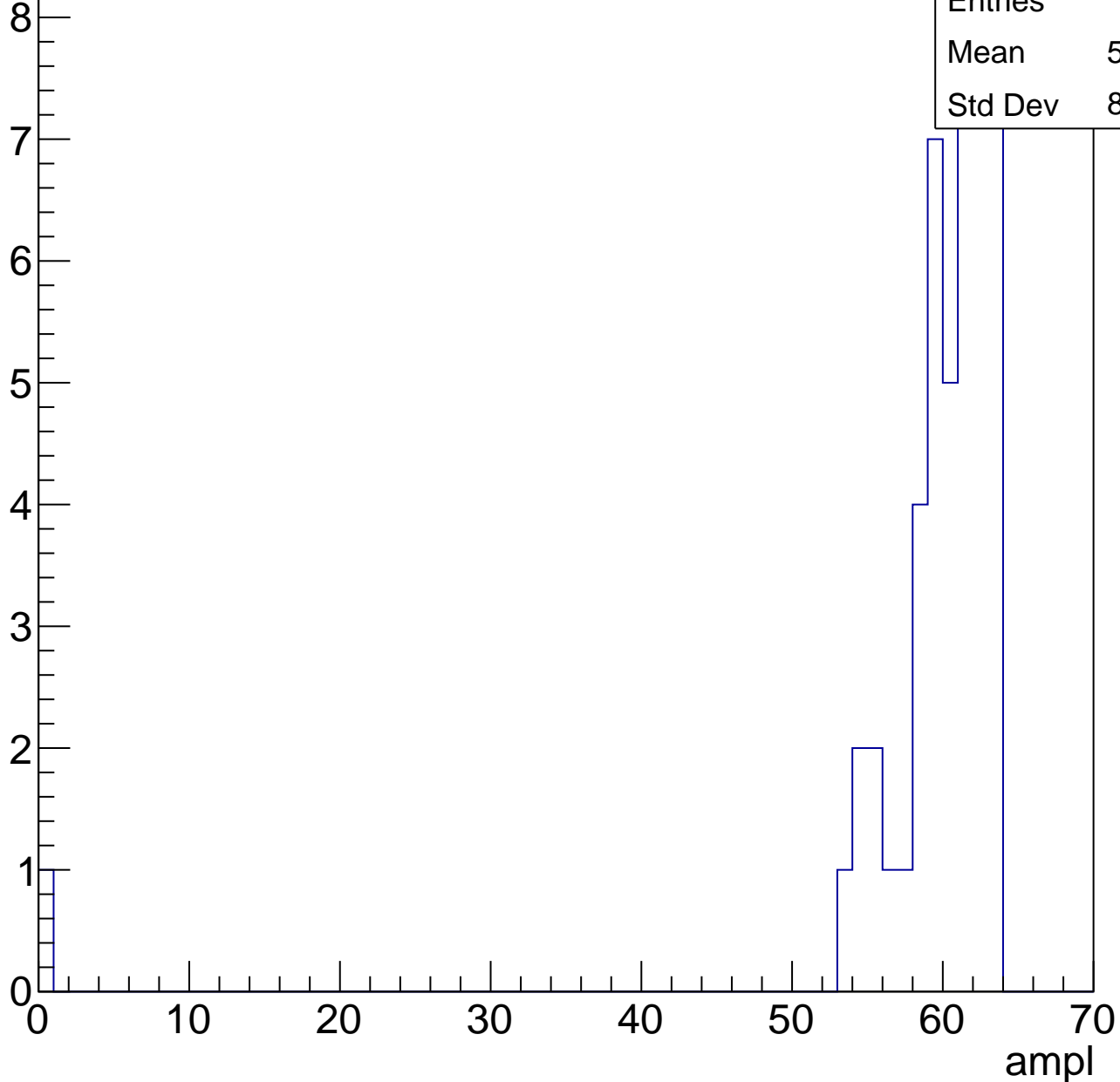


Entries	56
Mean	55.77
Std Dev	3.464

# B0L001S, U24-ch58, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U24-ch58, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch58, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U24-ch59, adc0

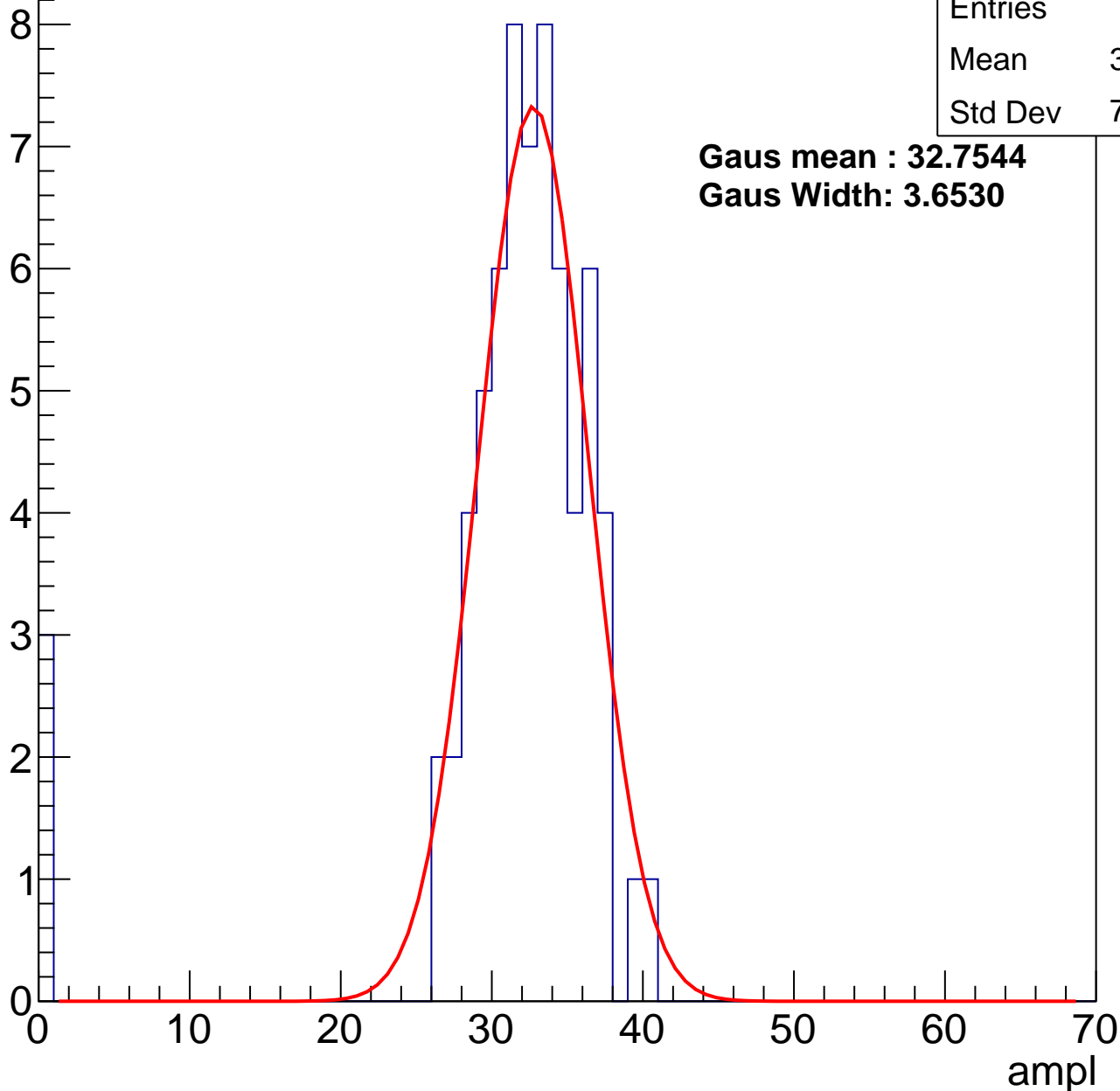
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	30.84
Std Dev	7.352

**Gaus mean : 32.7544**

**Gaus Width: 3.6530**



# B0L001S, U24-ch59, adc1

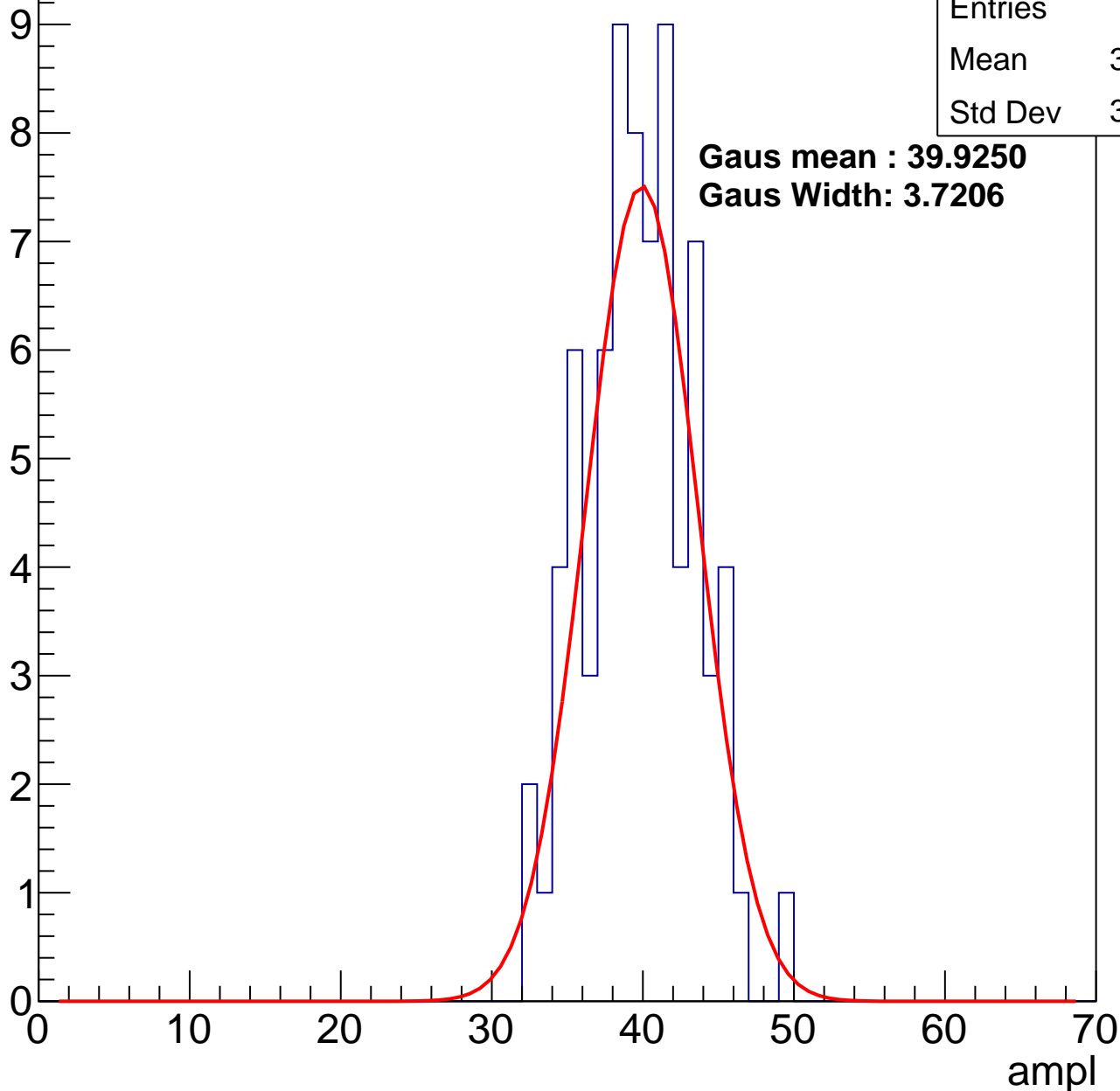
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	75
Mean	39.36
Std Dev	3.539

**Gaus mean : 39.9250**

**Gaus Width: 3.7206**



# B0L001S, U24-ch59, adc2

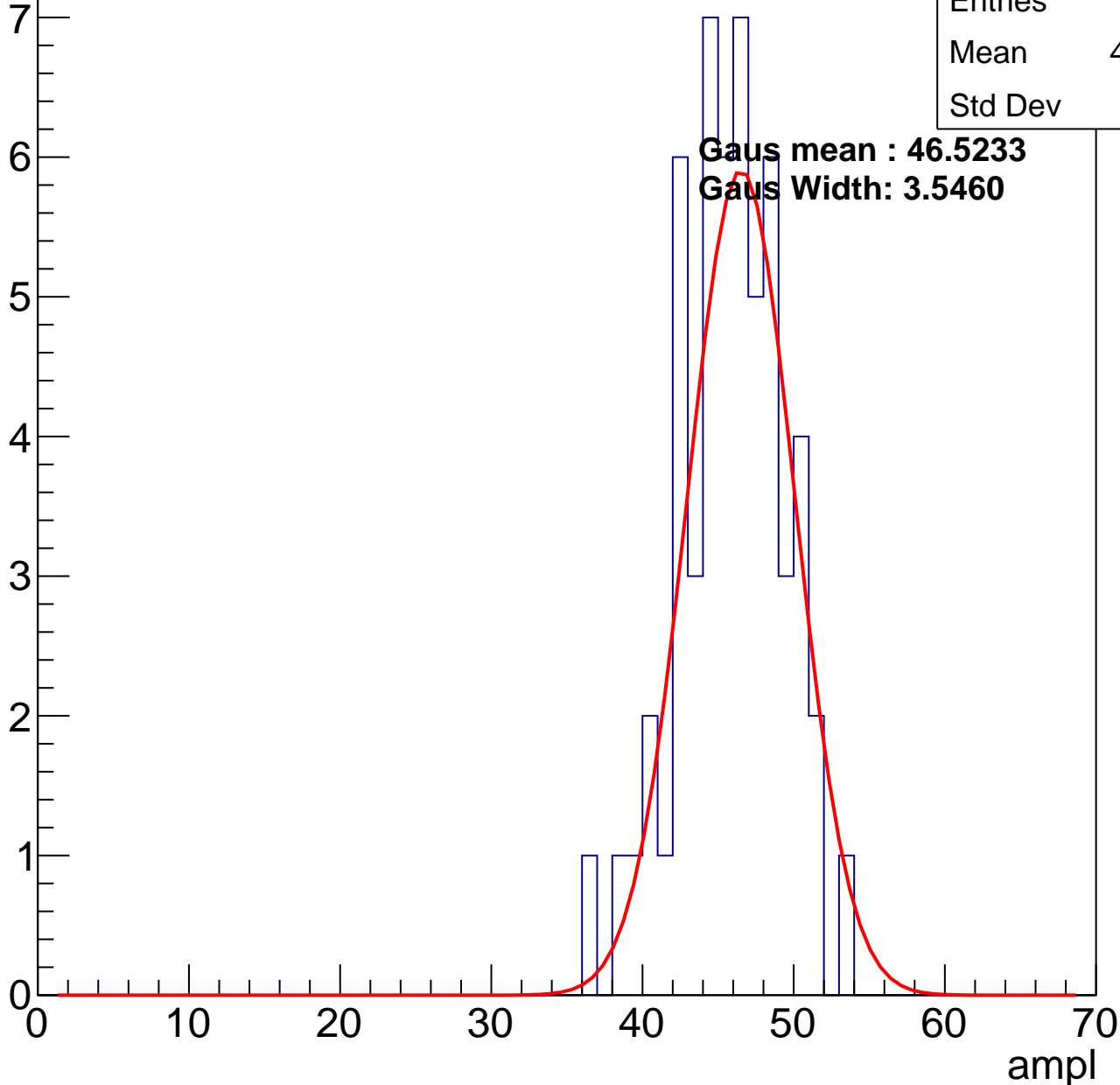
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	45.36
Std Dev	3.44

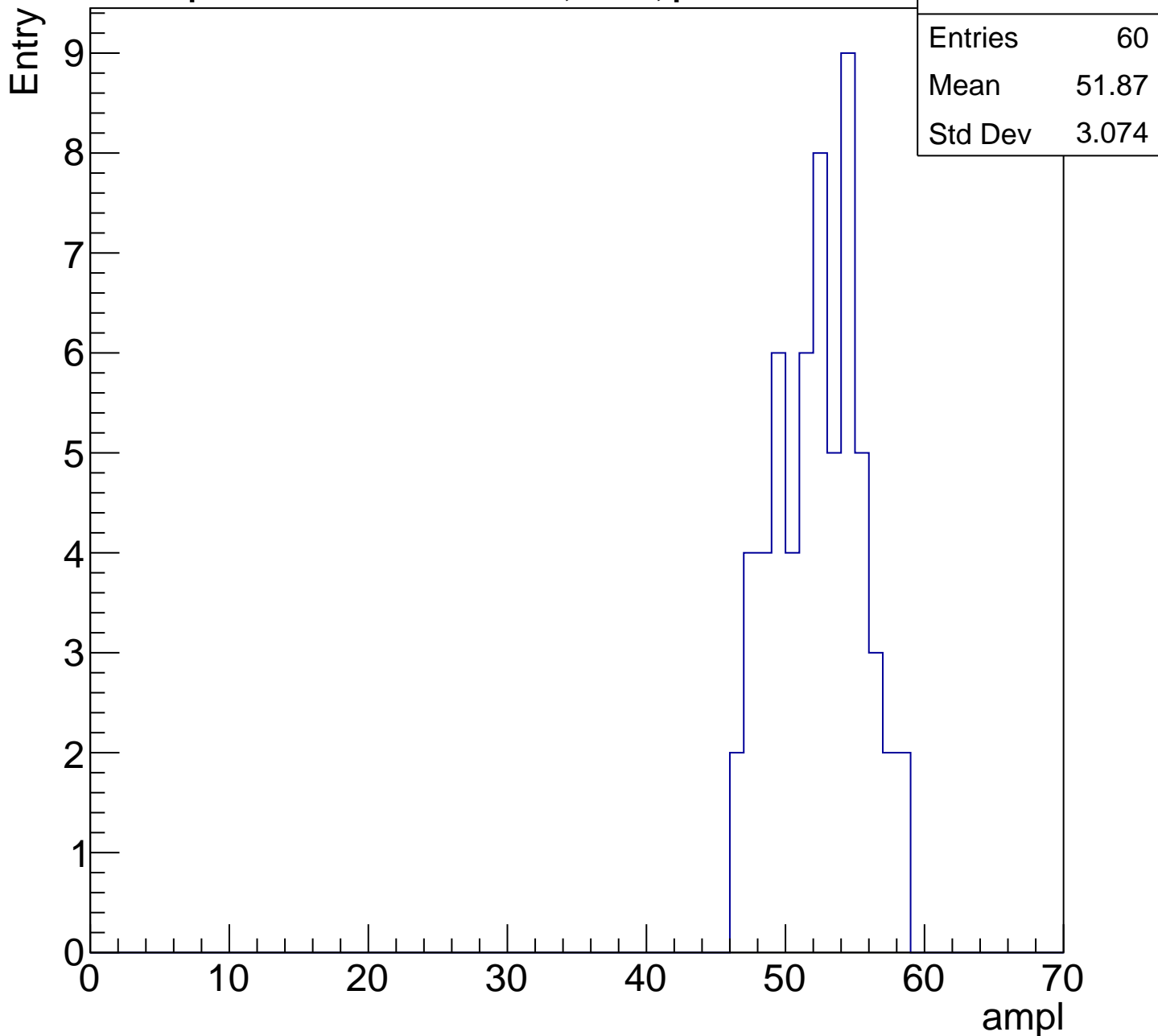
**Gaus mean : 46.5233**

**Gaus Width: 3.5460**



# B0L001S, U24-ch59, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

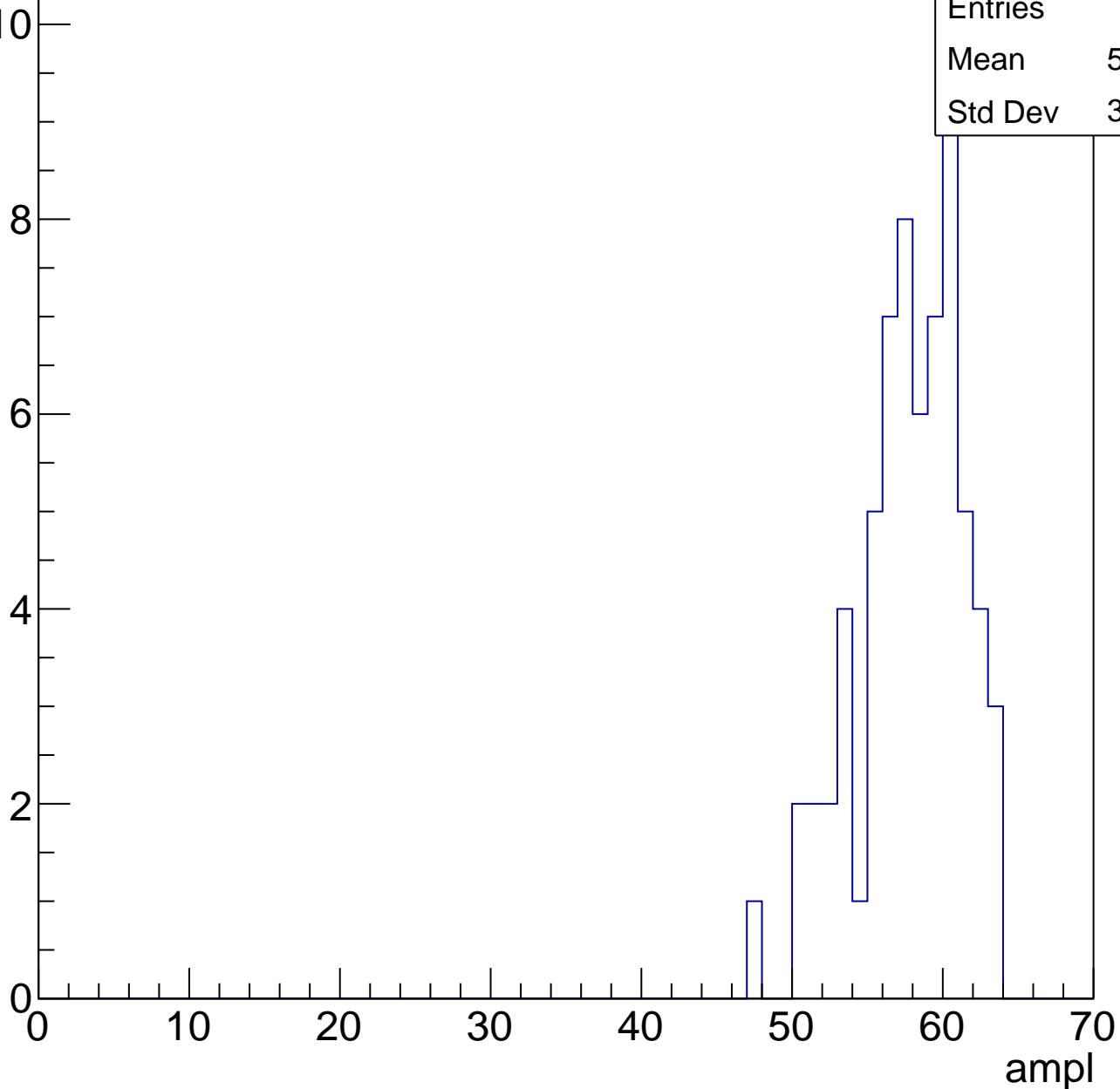


# B0L001S, U24-ch59, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	57.39
Std Dev	3.502

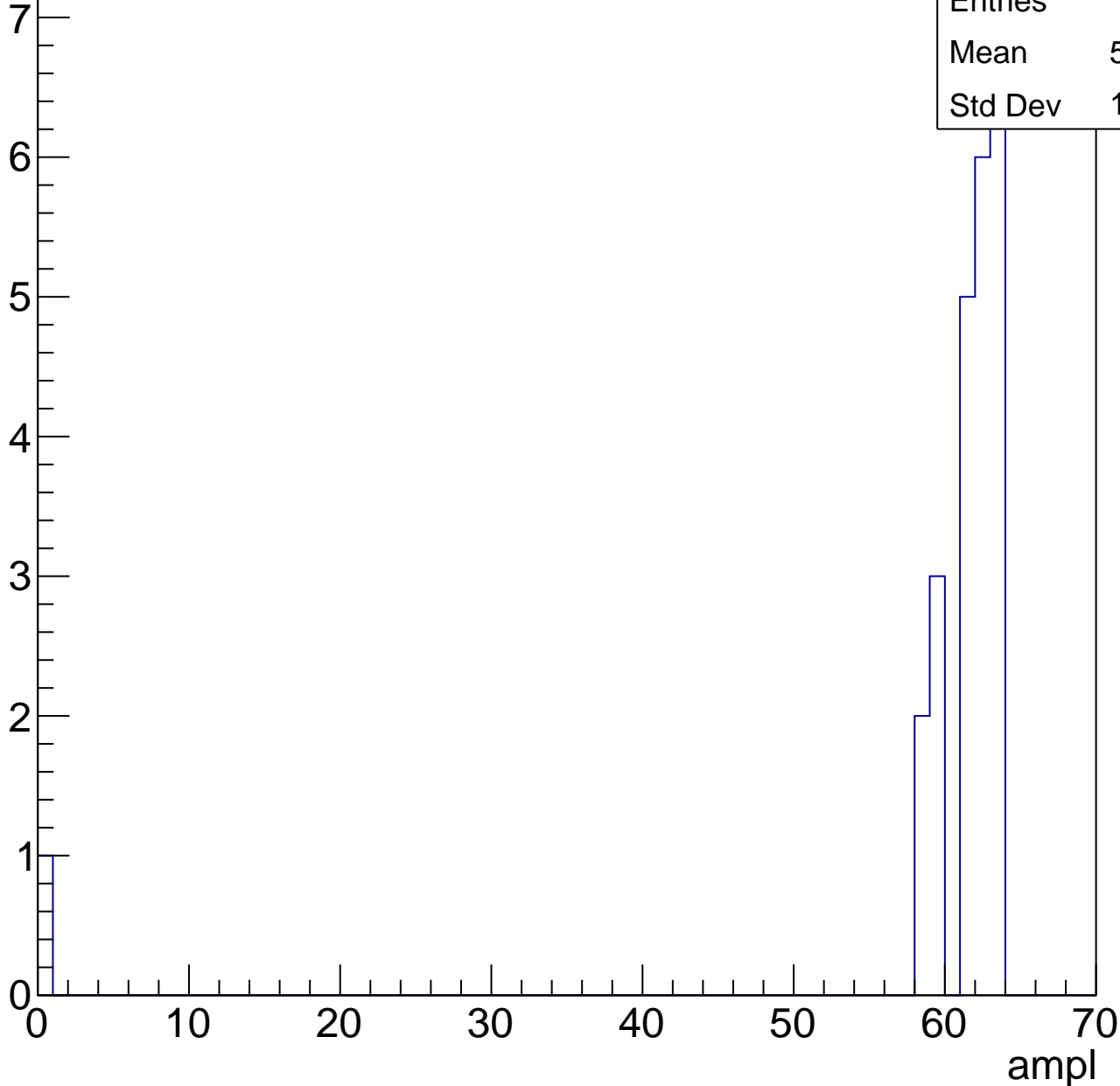


# B0L001S, U24-ch59, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	24
Mean	58.79
Std Dev	12.36



# B0L001S, U24-ch59, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U24-ch59, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U24-ch60, adc0

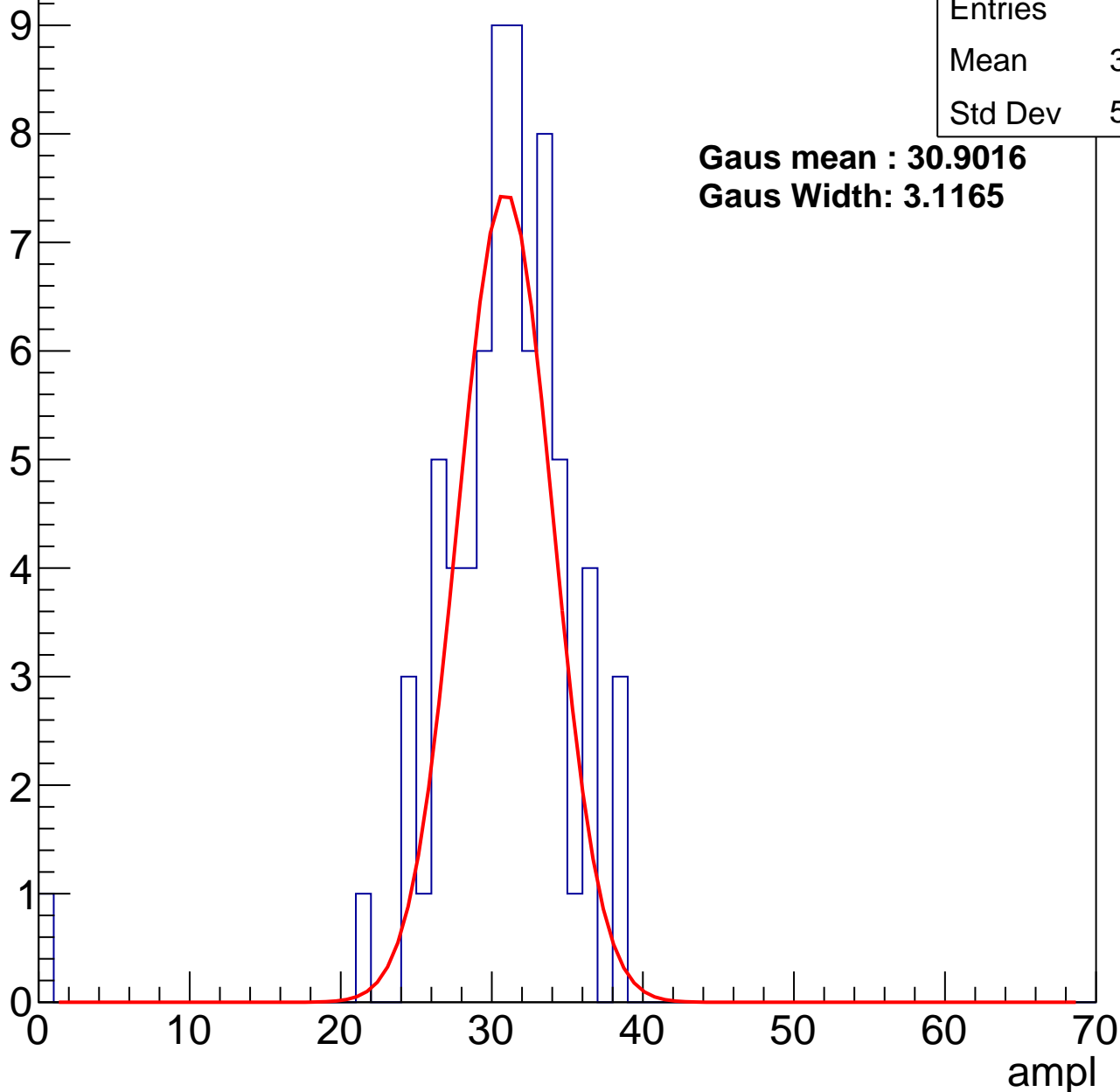
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	30.14
Std Dev	5.066

**Gaus mean : 30.9016**

**Gaus Width: 3.1165**



# B0L001S, U24-ch60, adc1

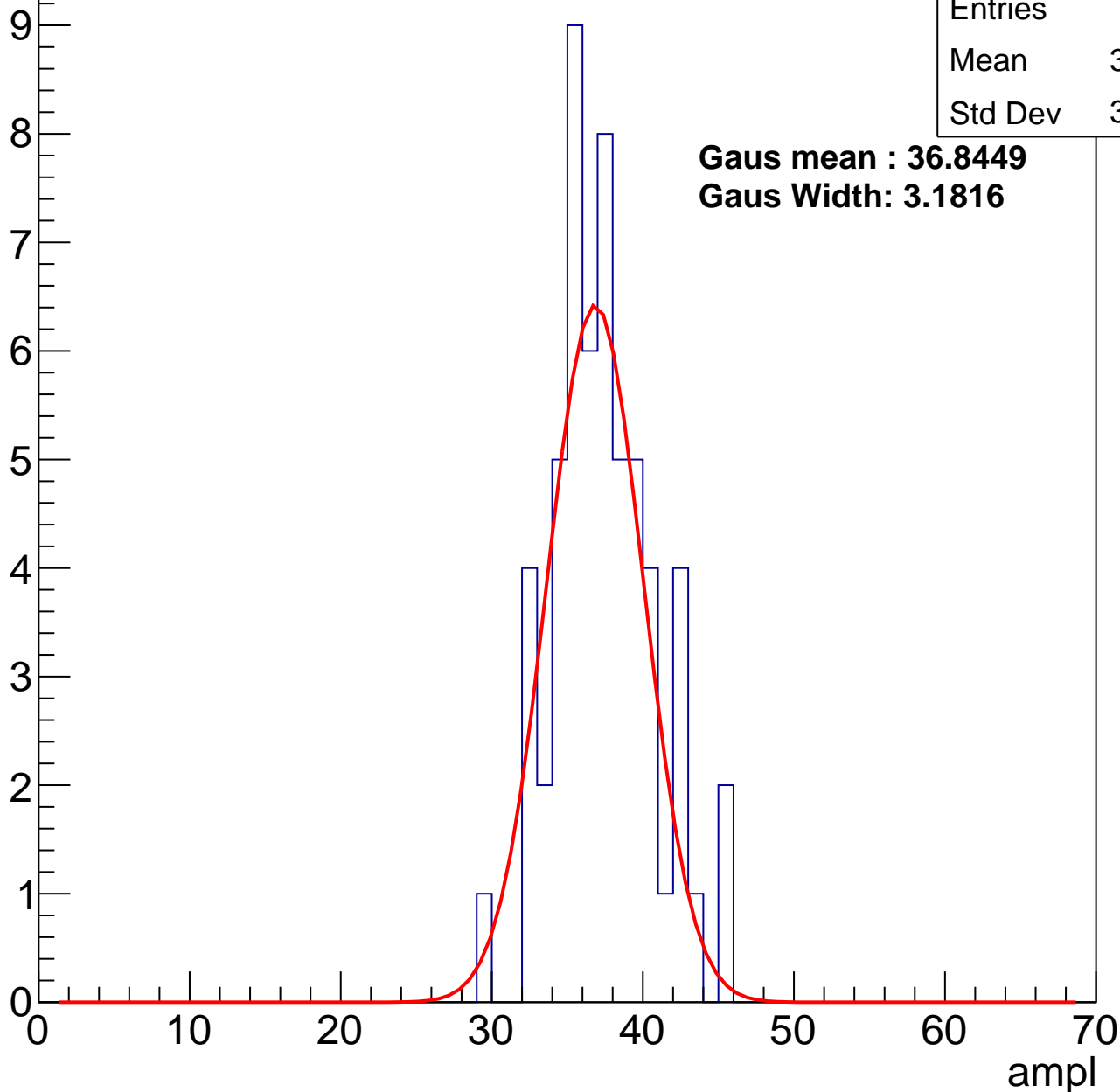
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	36.96
Std Dev	3.308

**Gaus mean : 36.8449**

**Gaus Width: 3.1816**



# B0L001S, U24-ch60, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	81
Mean	43.77
Std Dev	3.312

**Gaus mean : 44.6810**

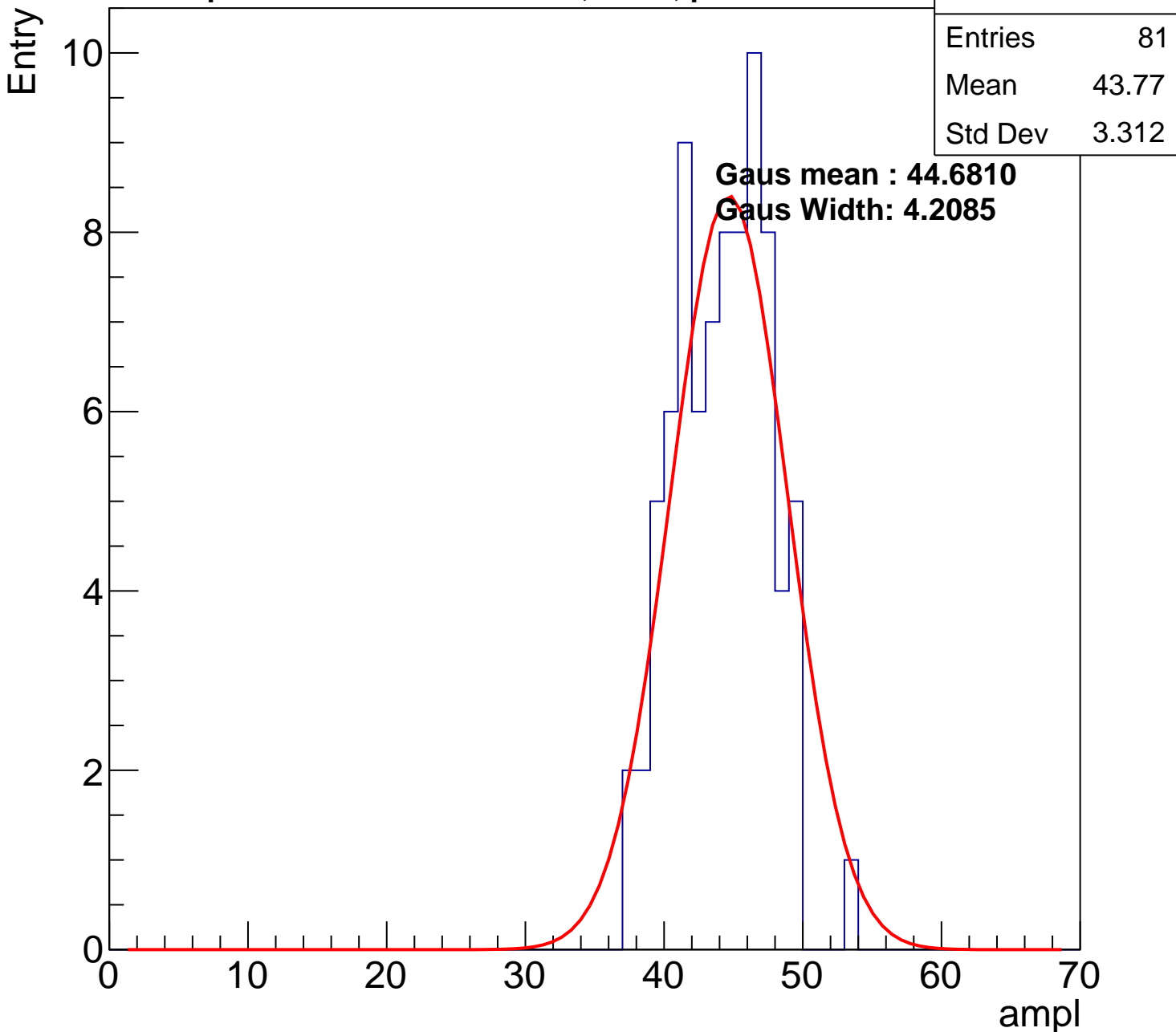
**Gaus Width: 4.2085**

Entry

10  
8  
6  
4  
2  
0

ampl

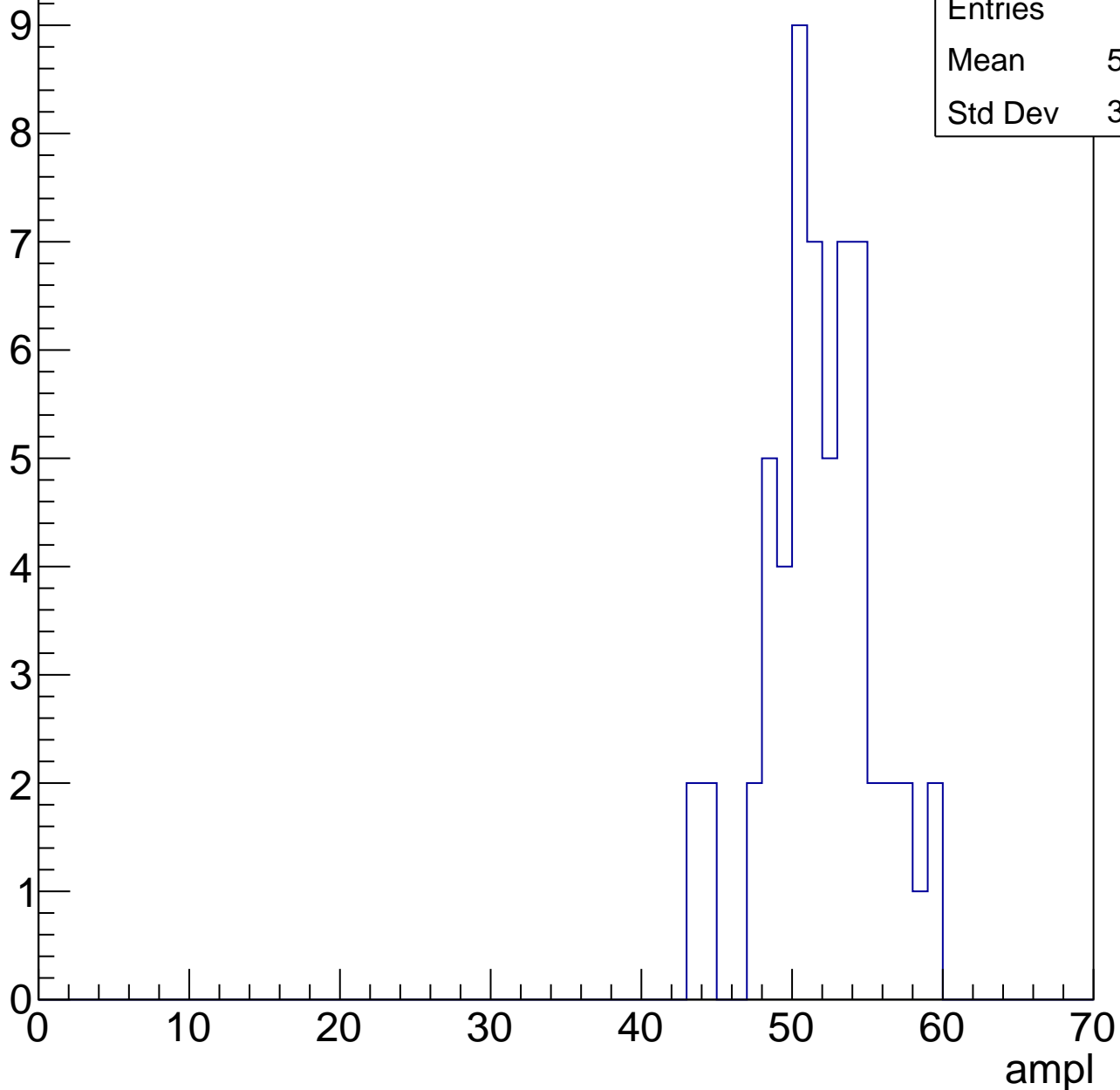
0 10 20 30 40 50 60 70



# B0L001S, U24-ch60, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

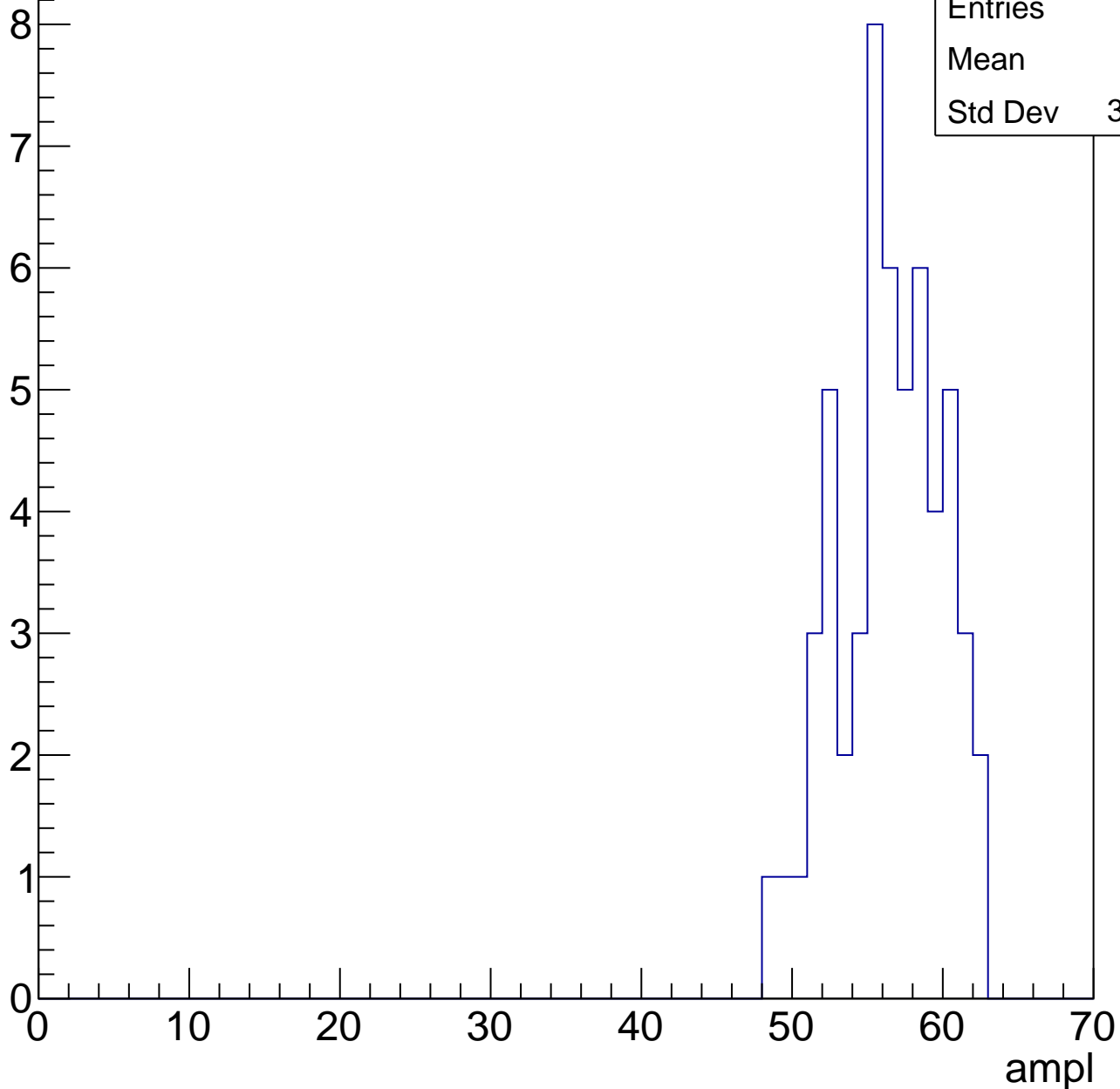


# B0L001S, U24-ch60, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	56
Std Dev	3.395

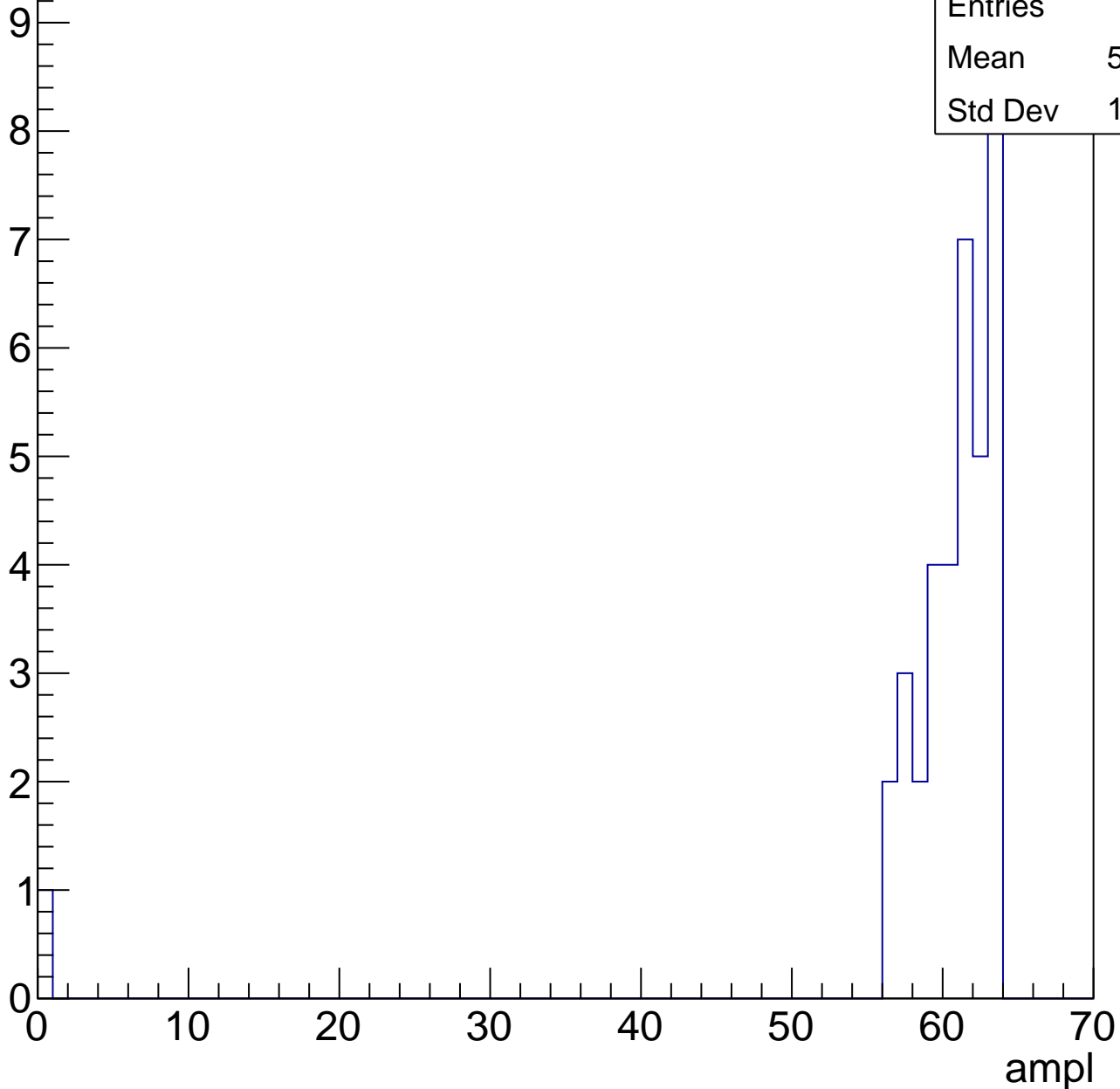


# B0L001S, U24-ch60, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

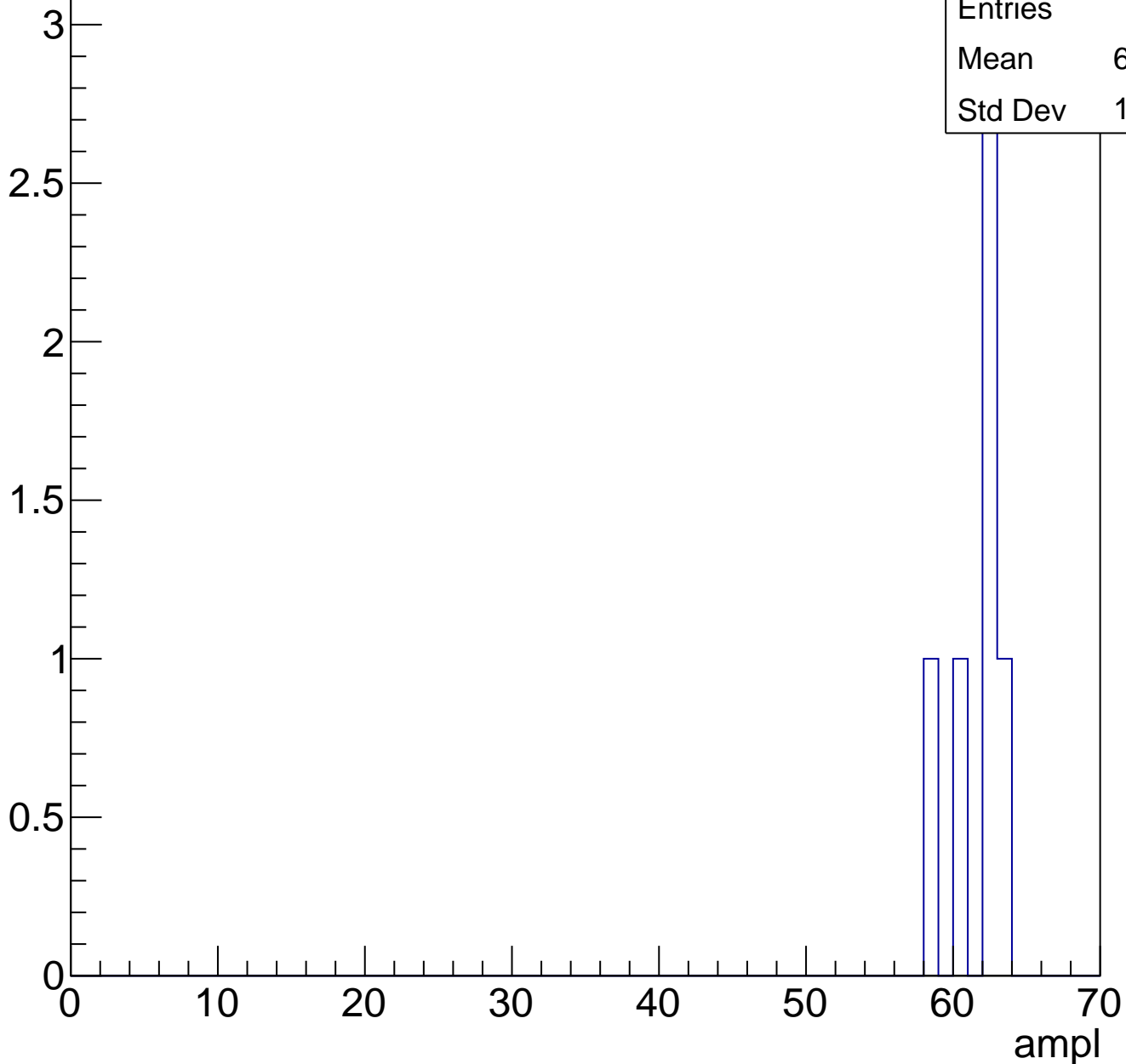
Entries	37
Mean	58.89
Std Dev	10.05



# B0L001S, U24-ch60, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch60, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U24-ch61, adc0

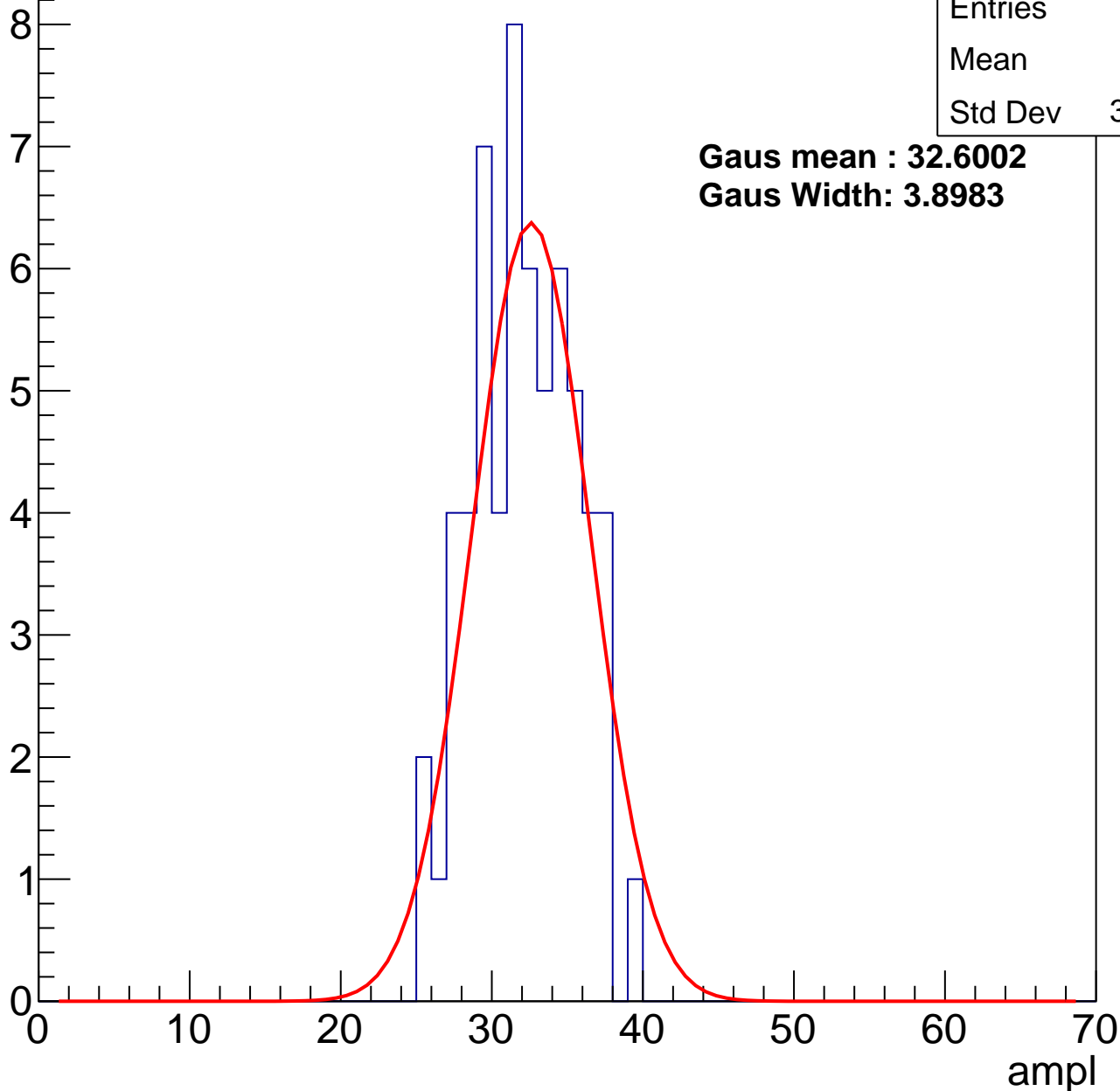
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	31.7
Std Dev	3.306

**Gaus mean : 32.6002**

**Gaus Width: 3.8983**

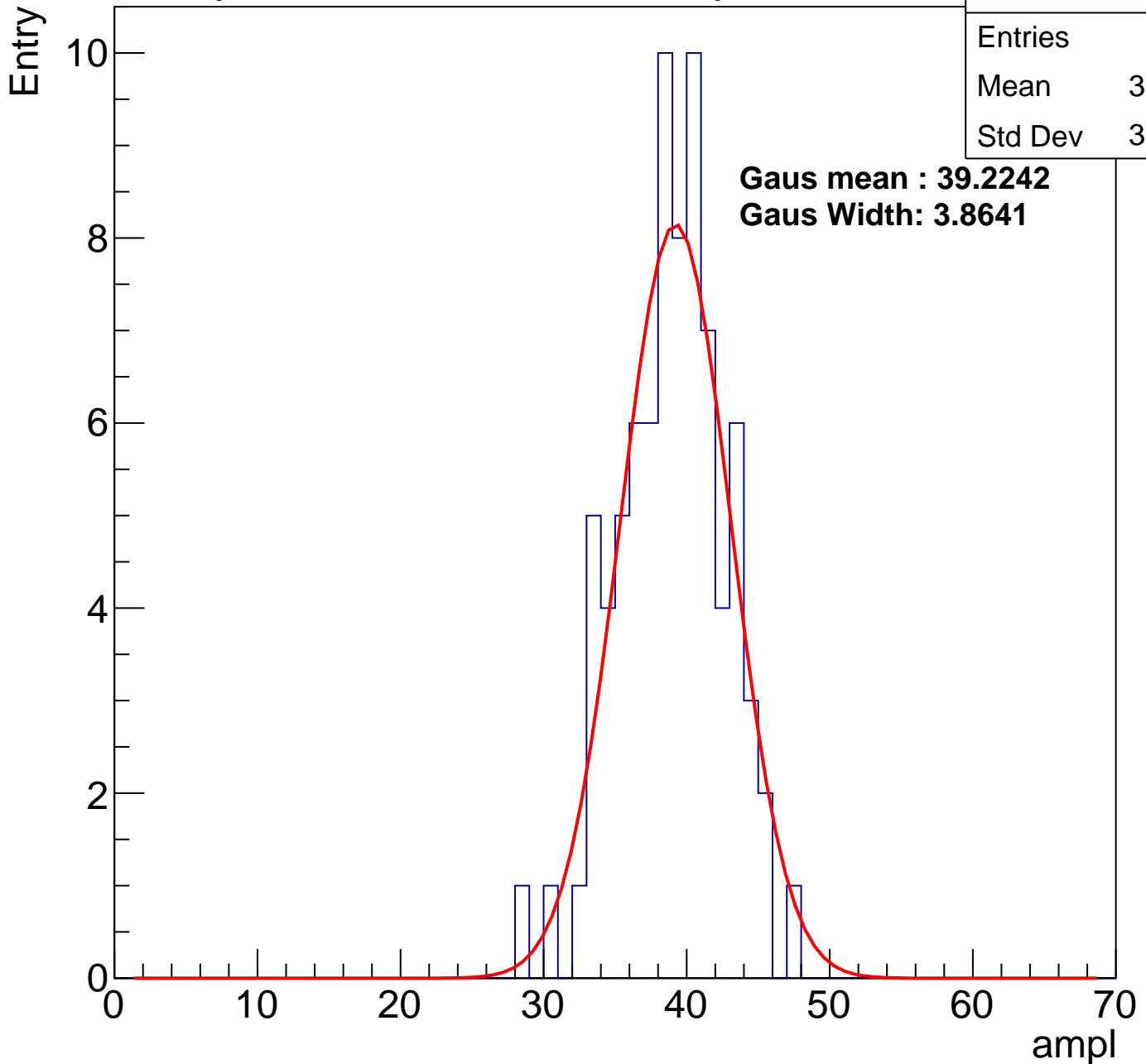


# B0L001S, U24-ch61, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	80
Mean	38.48
Std Dev	3.637

**Gaus mean : 39.2242**  
**Gaus Width: 3.8641**



# B0L001S, U24-ch61, adc2

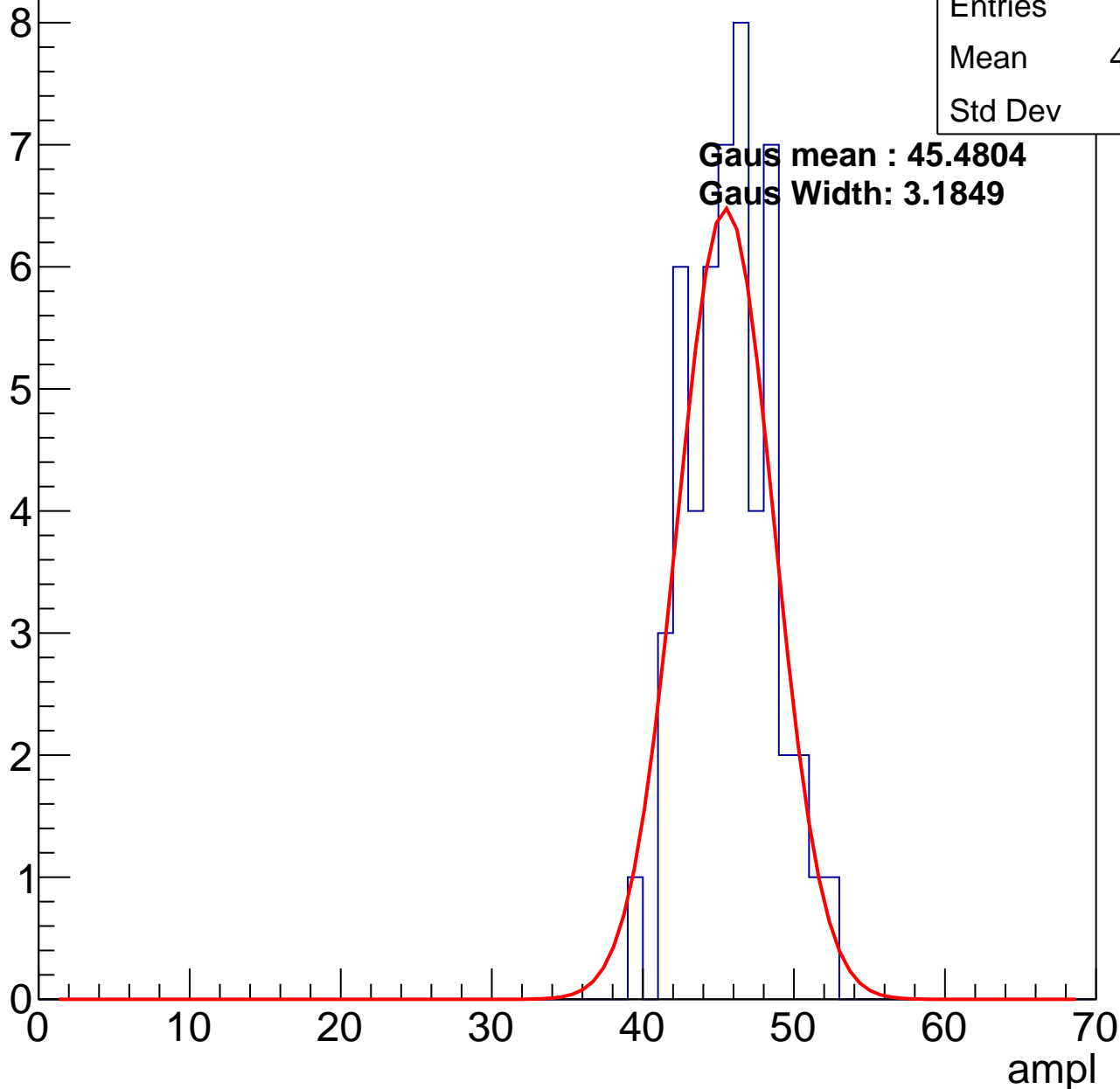
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	45.35
Std Dev	2.8

**Gaus mean : 45.4804**

**Gaus Width: 3.1849**

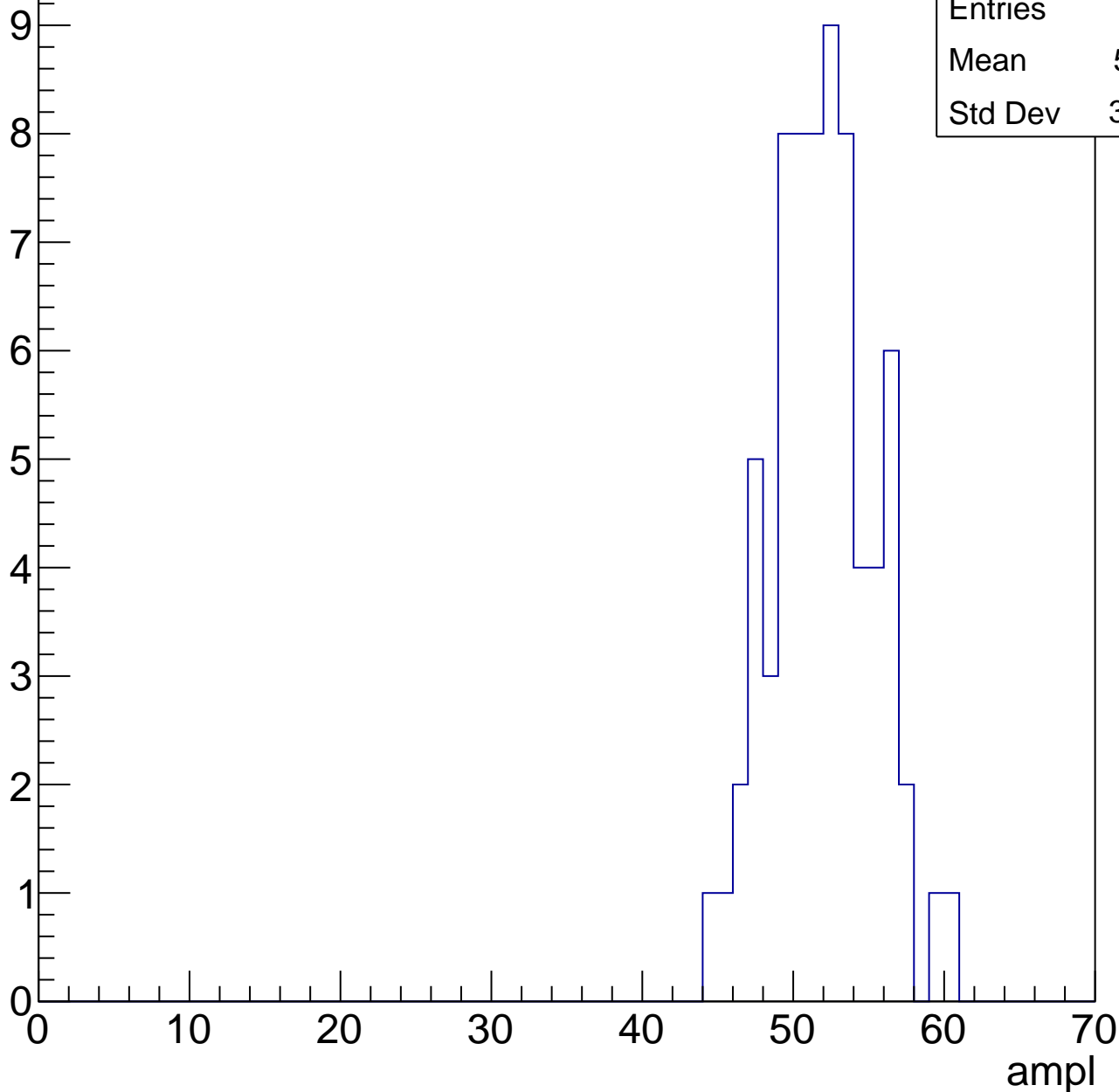


# B0L001S, U24-ch61, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	51.51
Std Dev	3.297

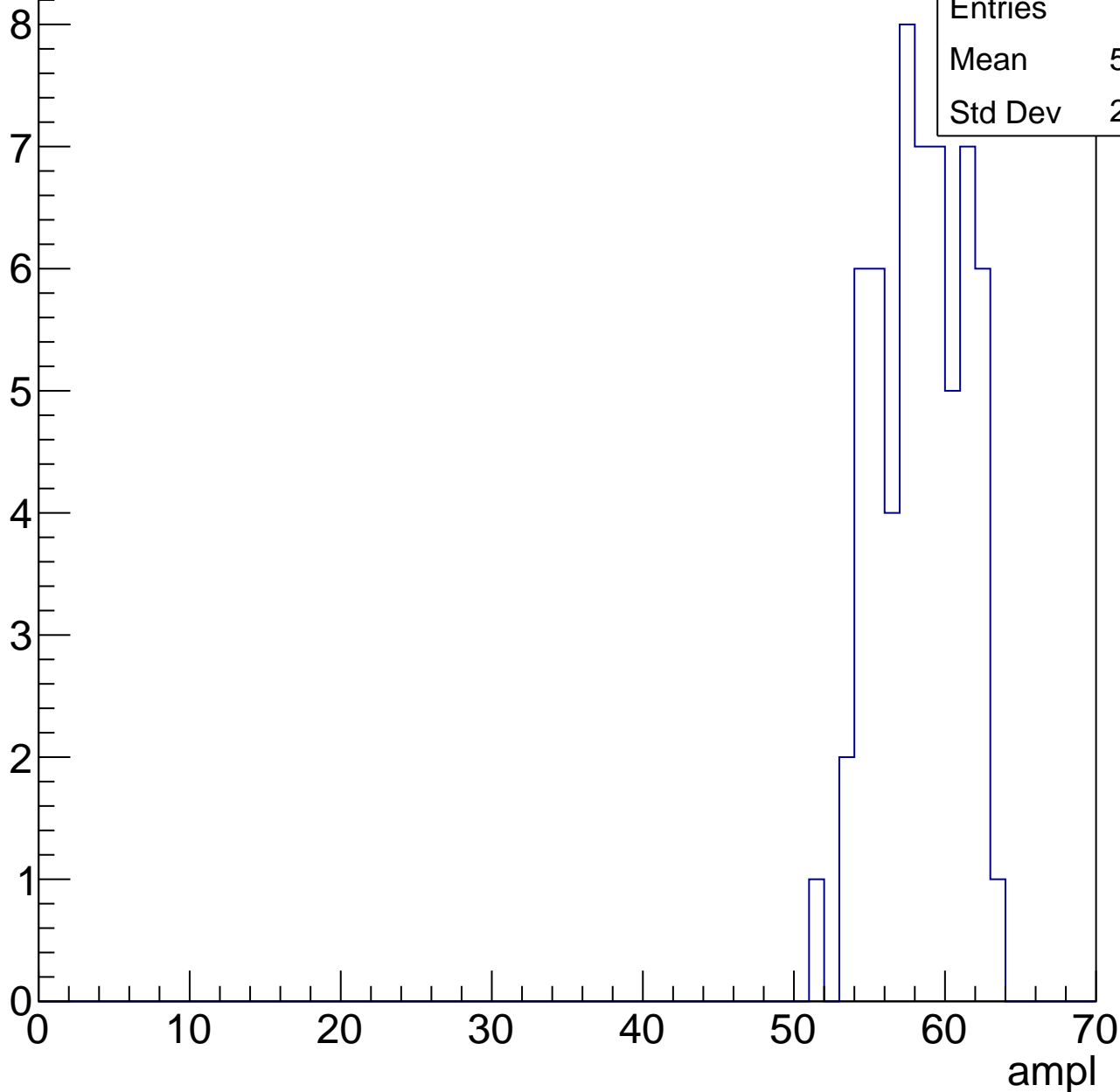


# B0L001S, U24-ch61, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	57.87
Std Dev	2.837

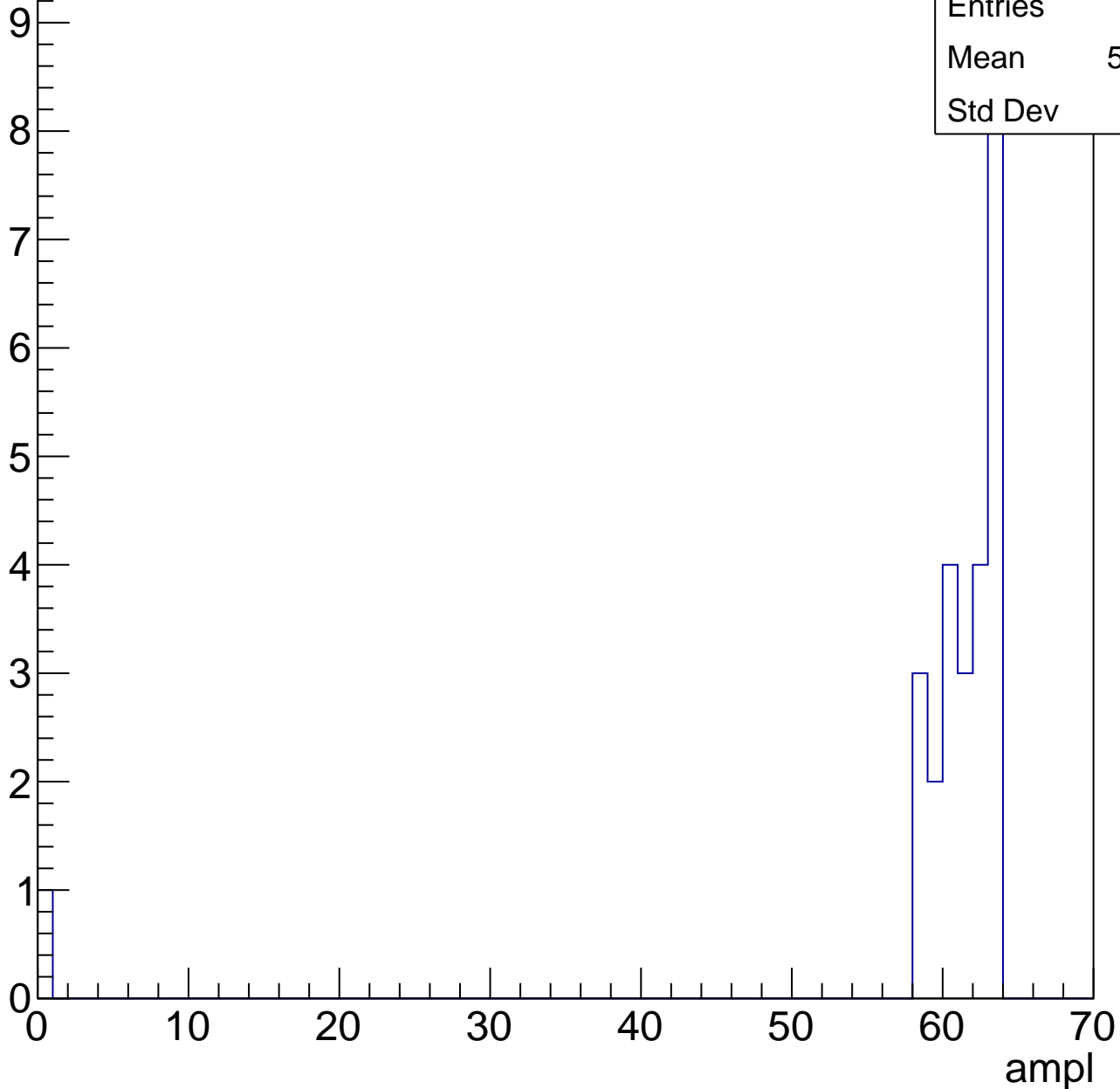


# B0L001S, U24-ch61, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	26
Mean	58.85
Std Dev	11.9



# B0L001S, U24-ch61, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U24-ch61, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L001S, U24-ch62, adc0

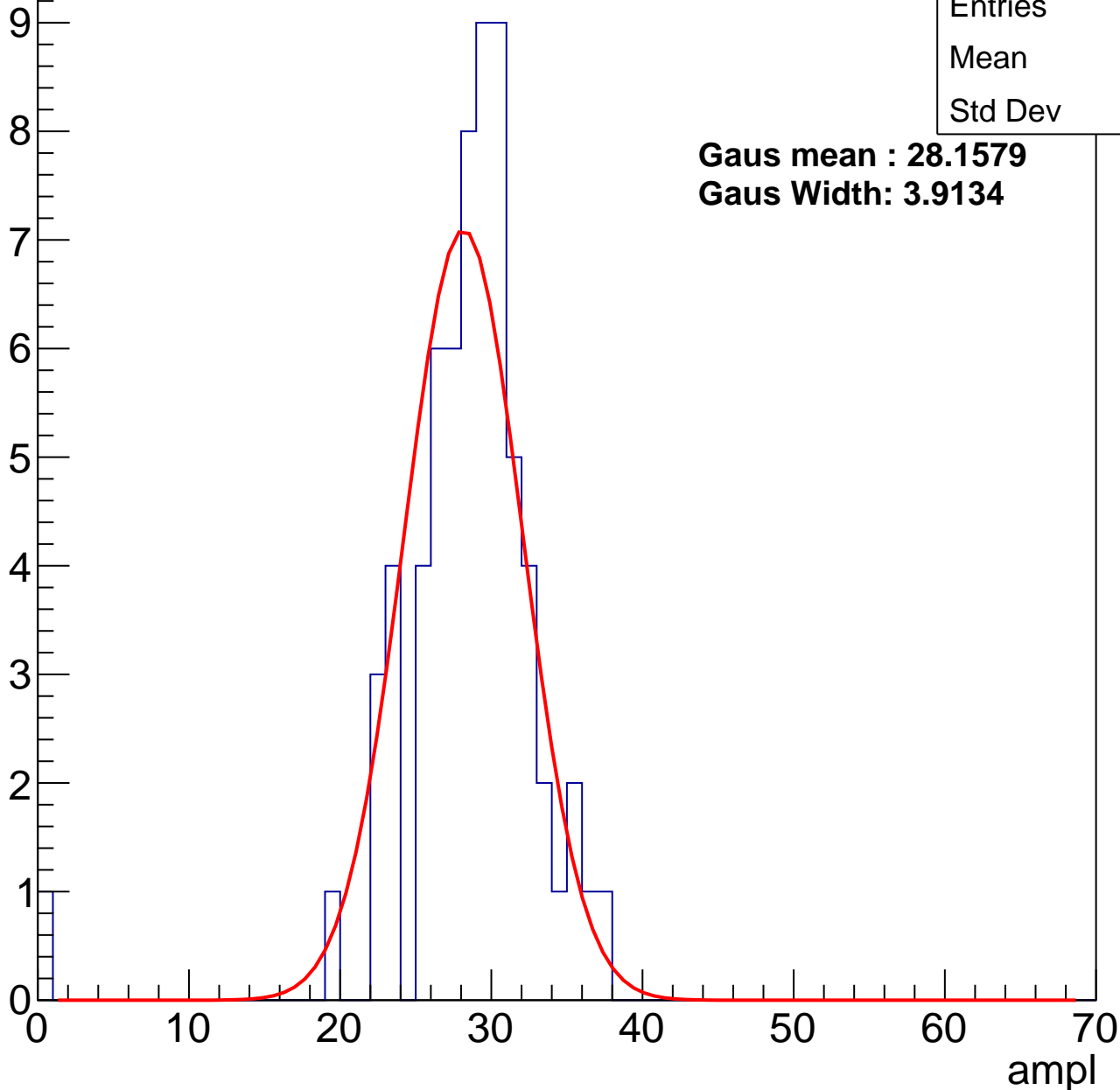
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	28
Std Dev	4.92

**Gaus mean : 28.1579**

**Gaus Width: 3.9134**



# B0L001S, U24-ch62, adc1

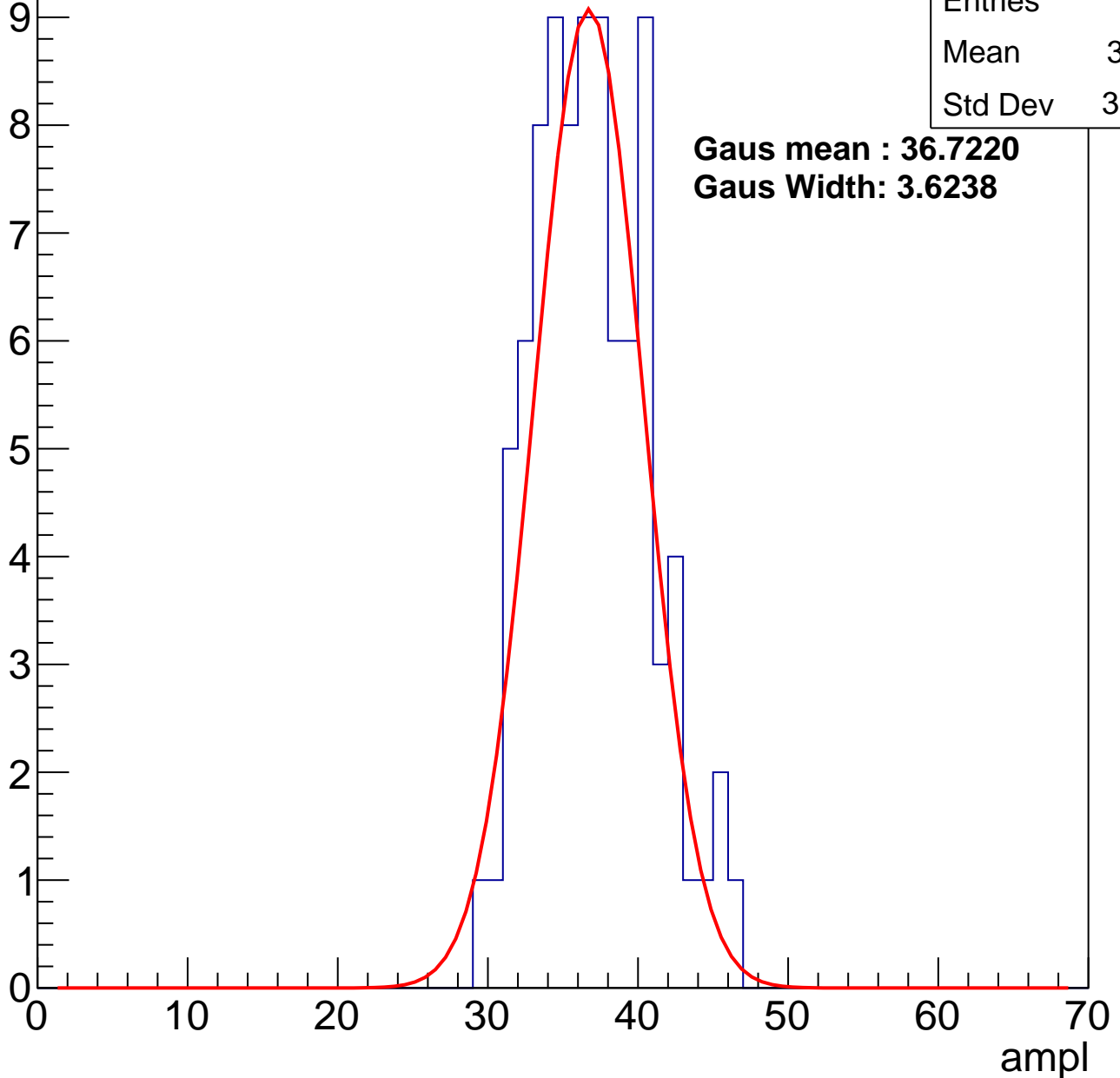
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	89
Mean	36.51
Std Dev	3.709

**Gaus mean : 36.7220**

**Gaus Width: 3.6238**

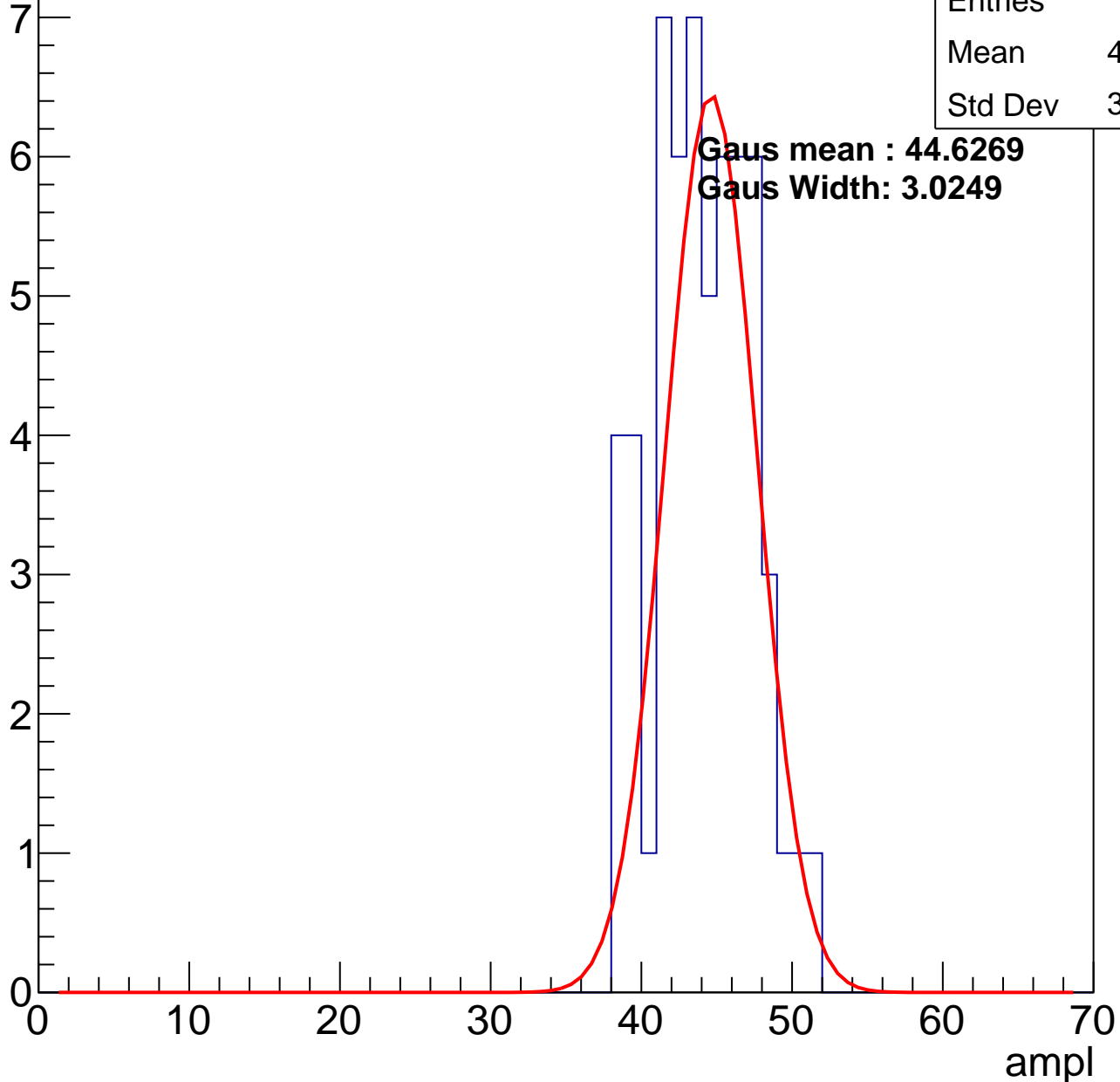


# B0L001S, U24-ch62, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	43.62
Std Dev	3.183

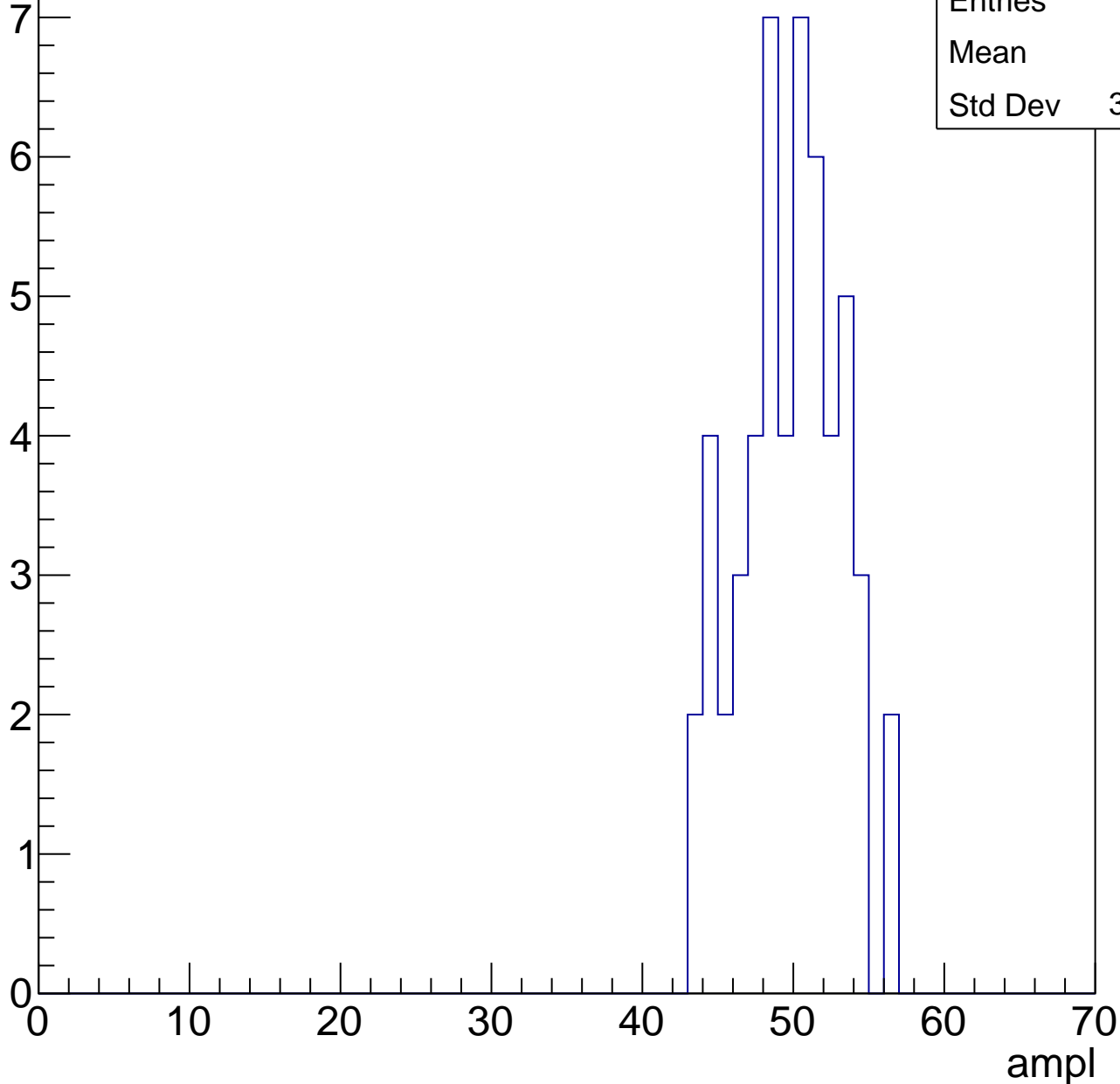


# B0L001S, U24-ch62, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

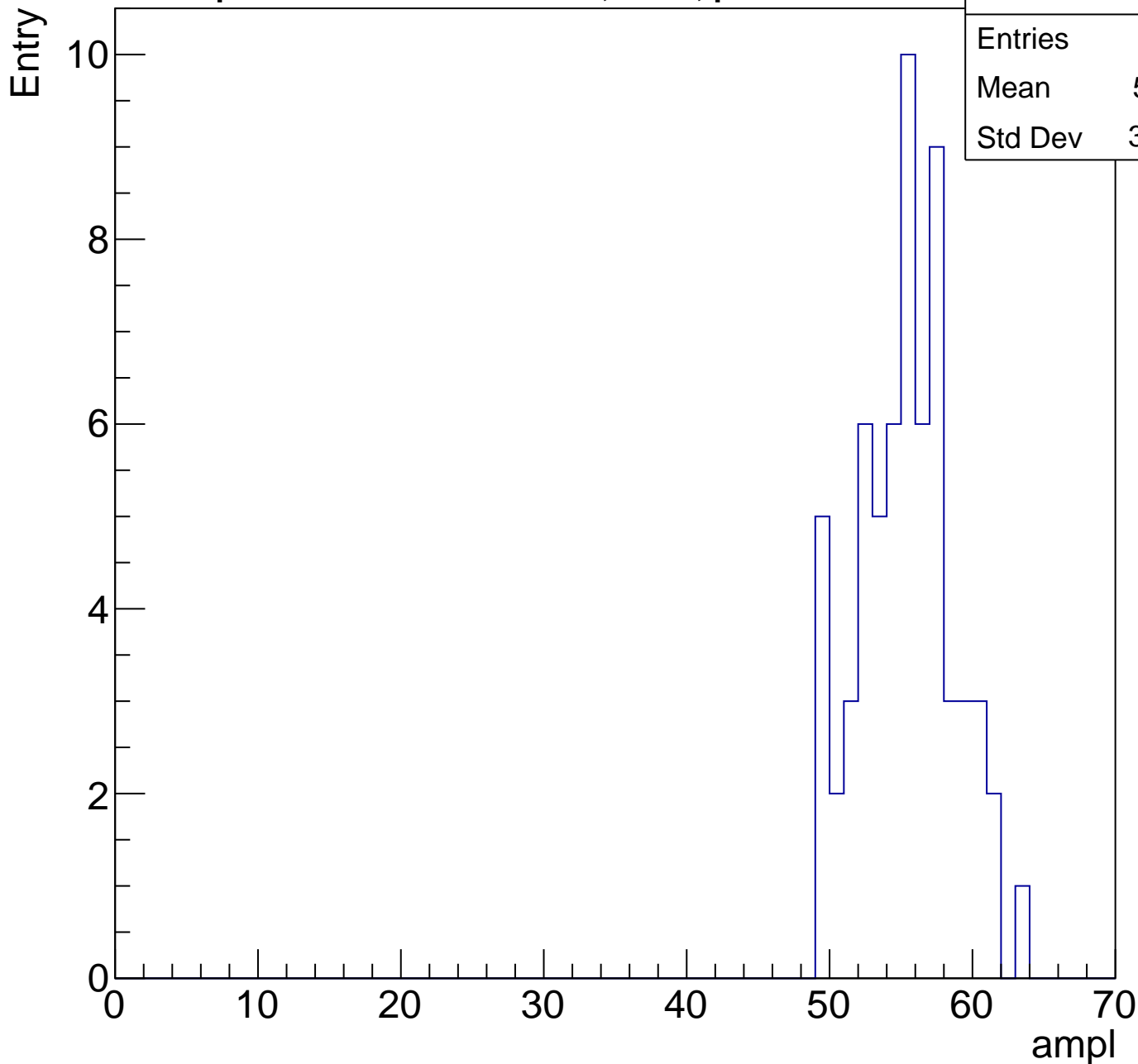
Entries	53
Mean	49.3
Std Dev	3.277



# B0L001S, U24-ch62, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	64
Mean	54.91
Std Dev	3.273

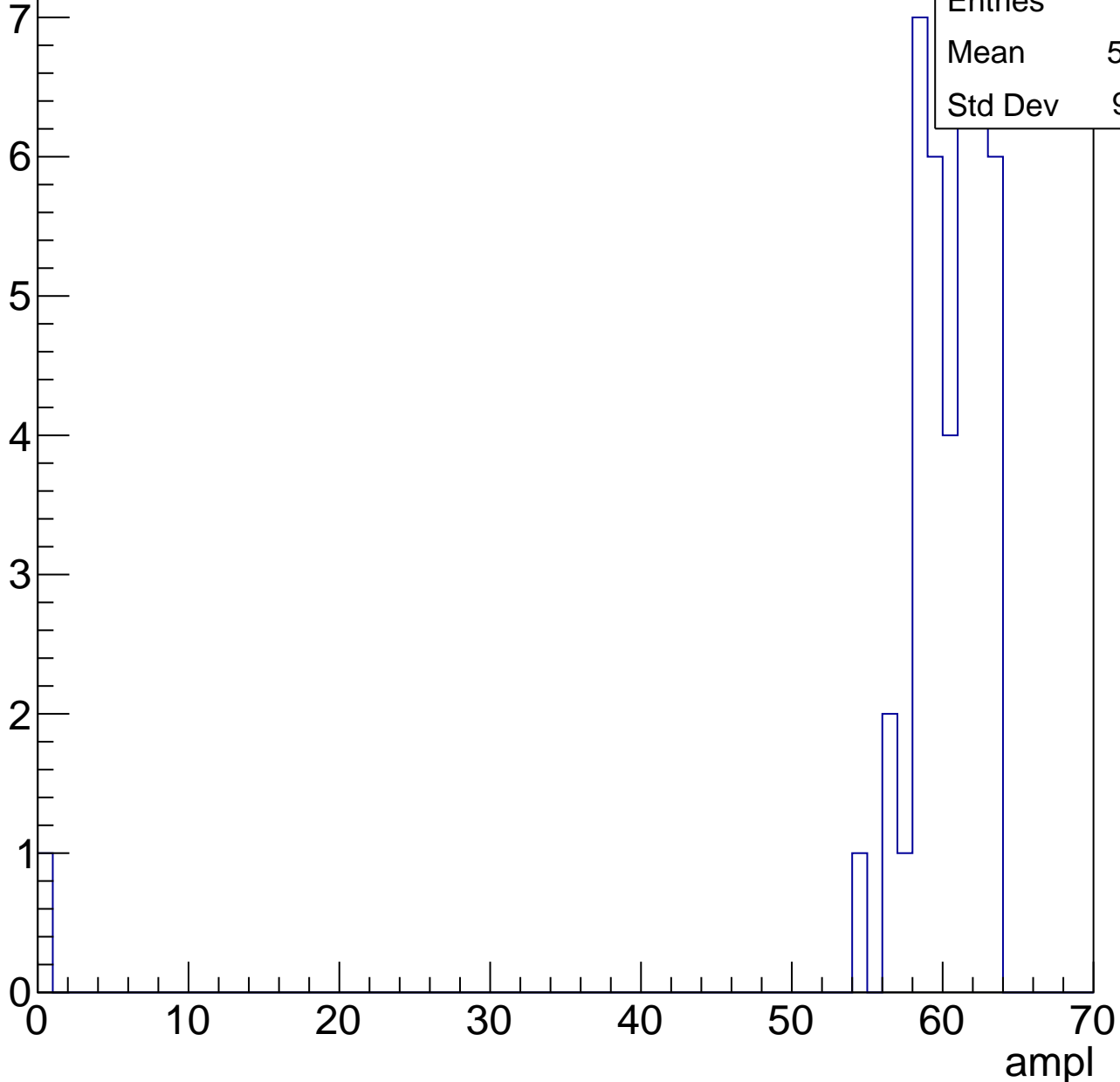


# B0L001S, U24-ch62, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

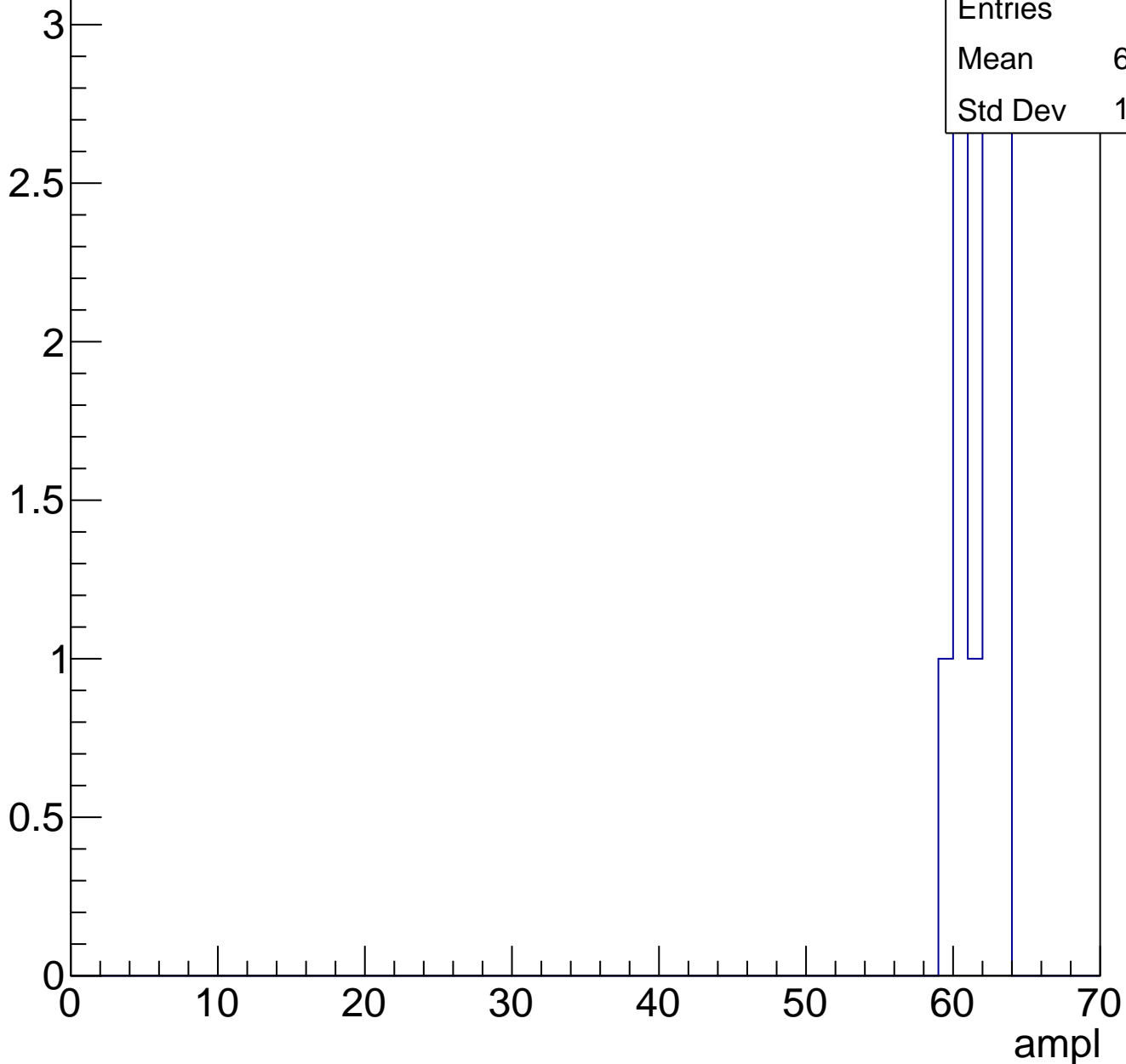
Entries	42
Mean	58.62
Std Dev	9.411



# B0L001S, U24-ch62, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch62, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U24-ch63, adc0

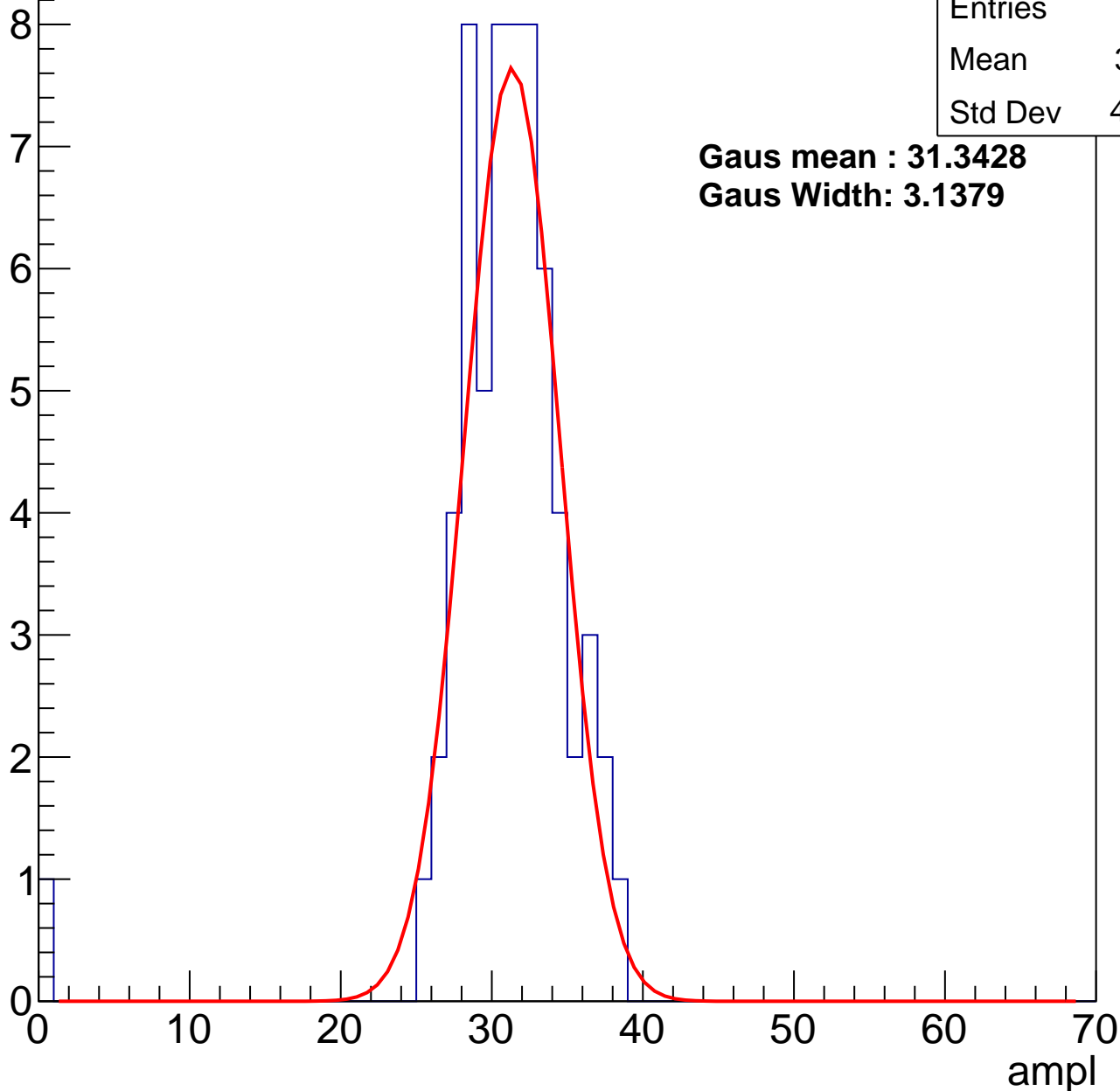
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	30.51
Std Dev	4.866

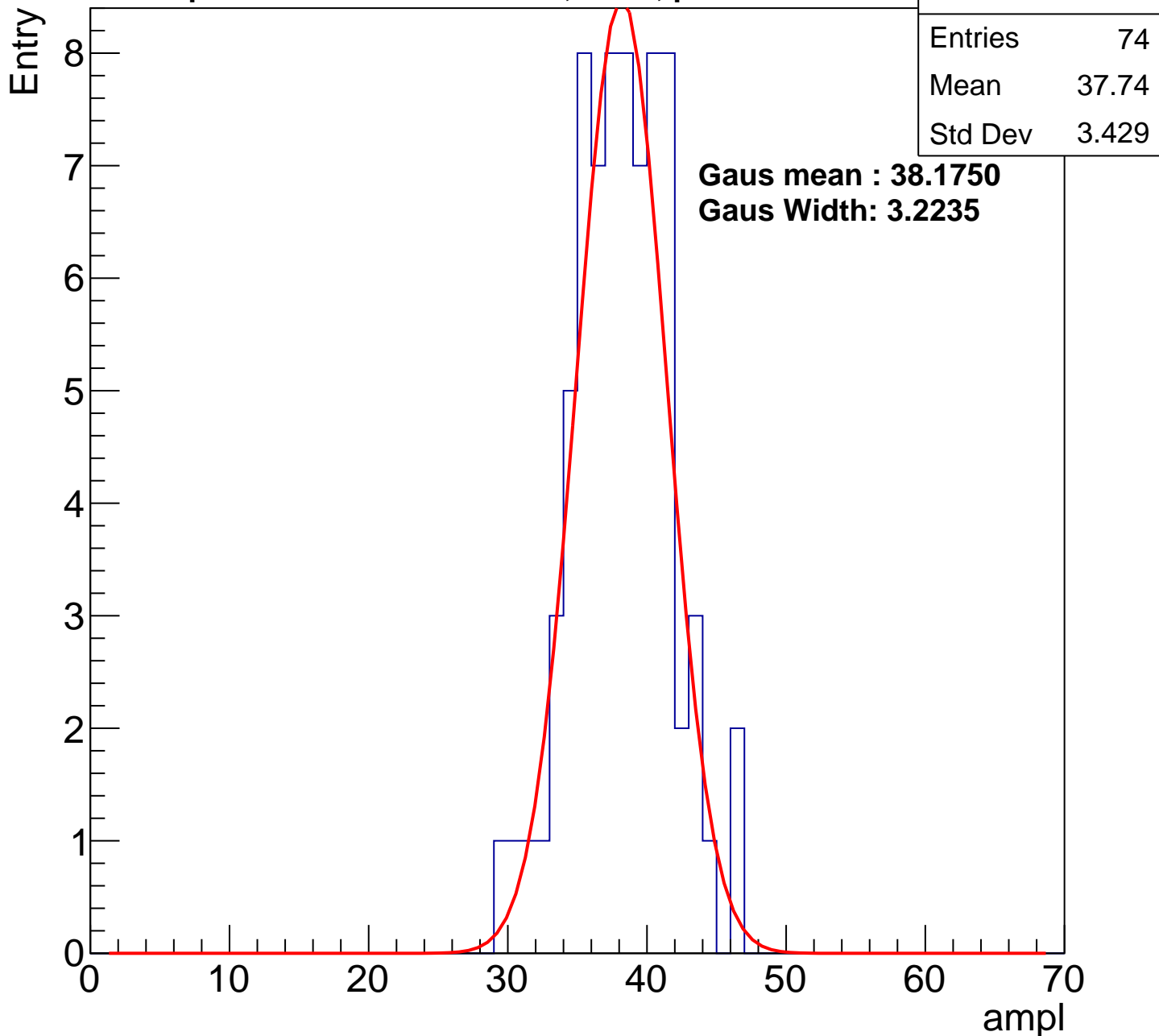
**Gaus mean : 31.3428**

**Gaus Width: 3.1379**



# B0L001S, U24-ch63, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U24-ch63, adc2

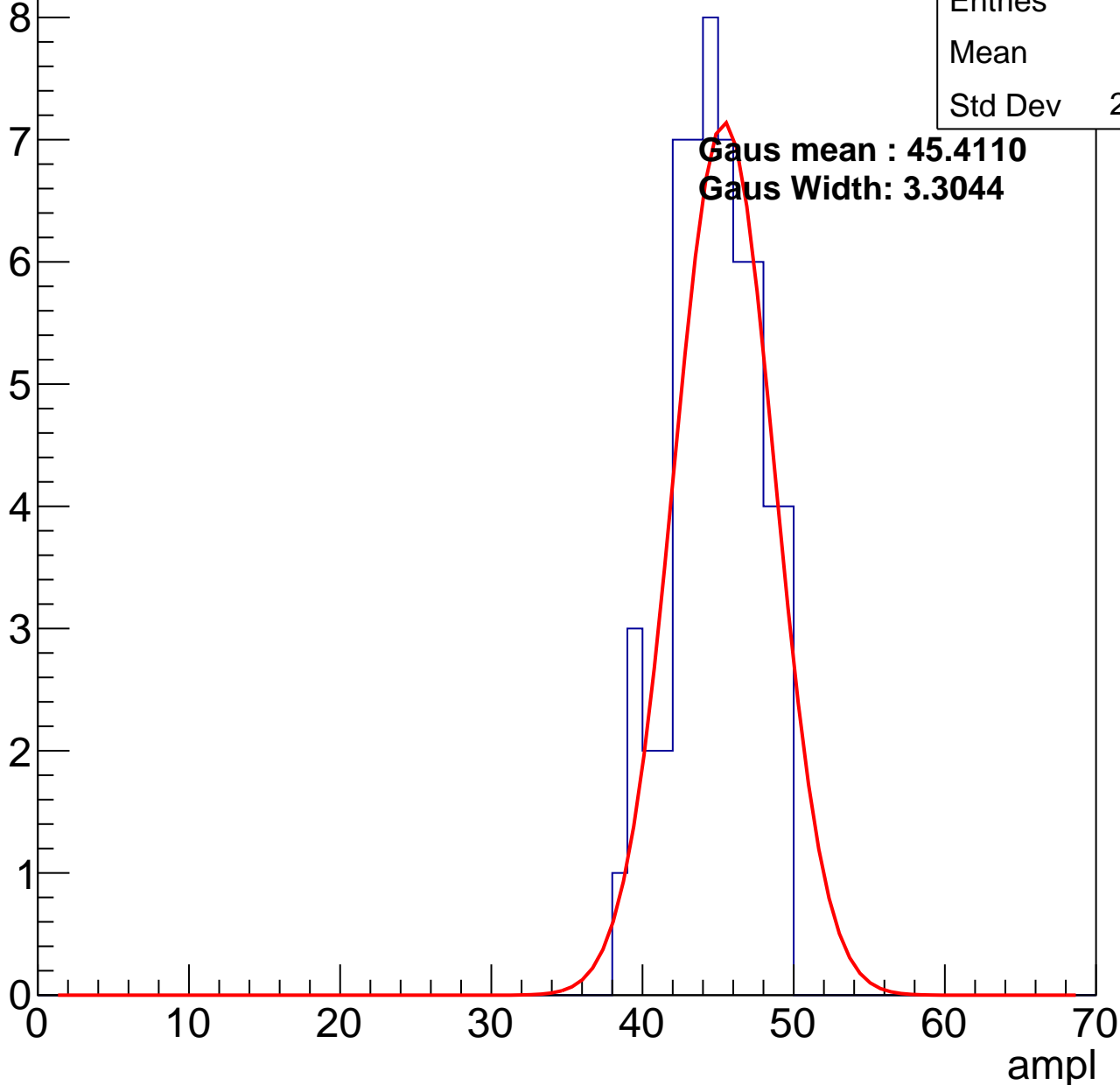
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	44.3
Std Dev	2.778

**Gaus mean : 45.4110**

**Gaus Width: 3.3044**



# B0L001S, U24-ch63, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

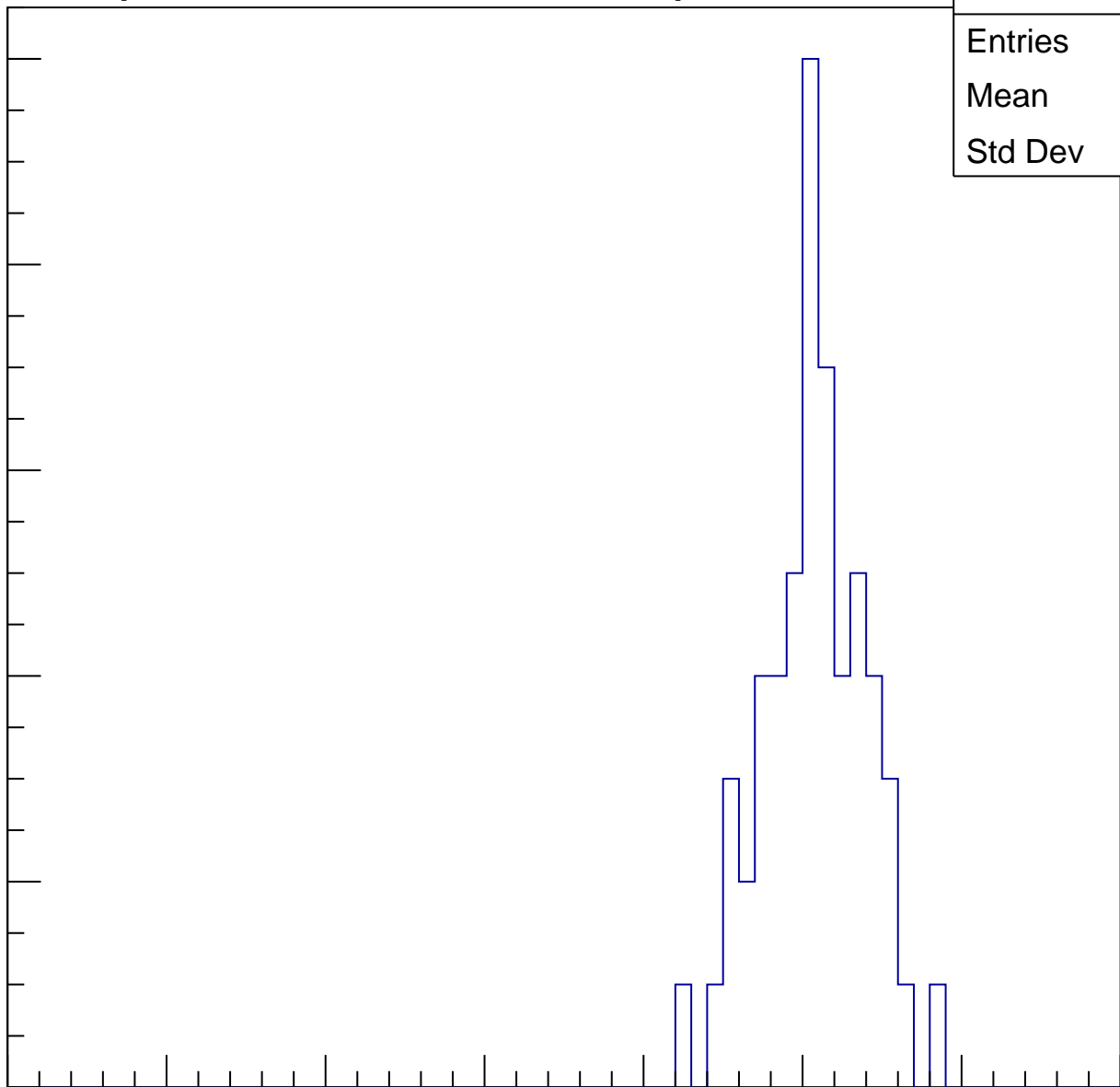
Entries	55
Mean	50.24
Std Dev	3.213

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

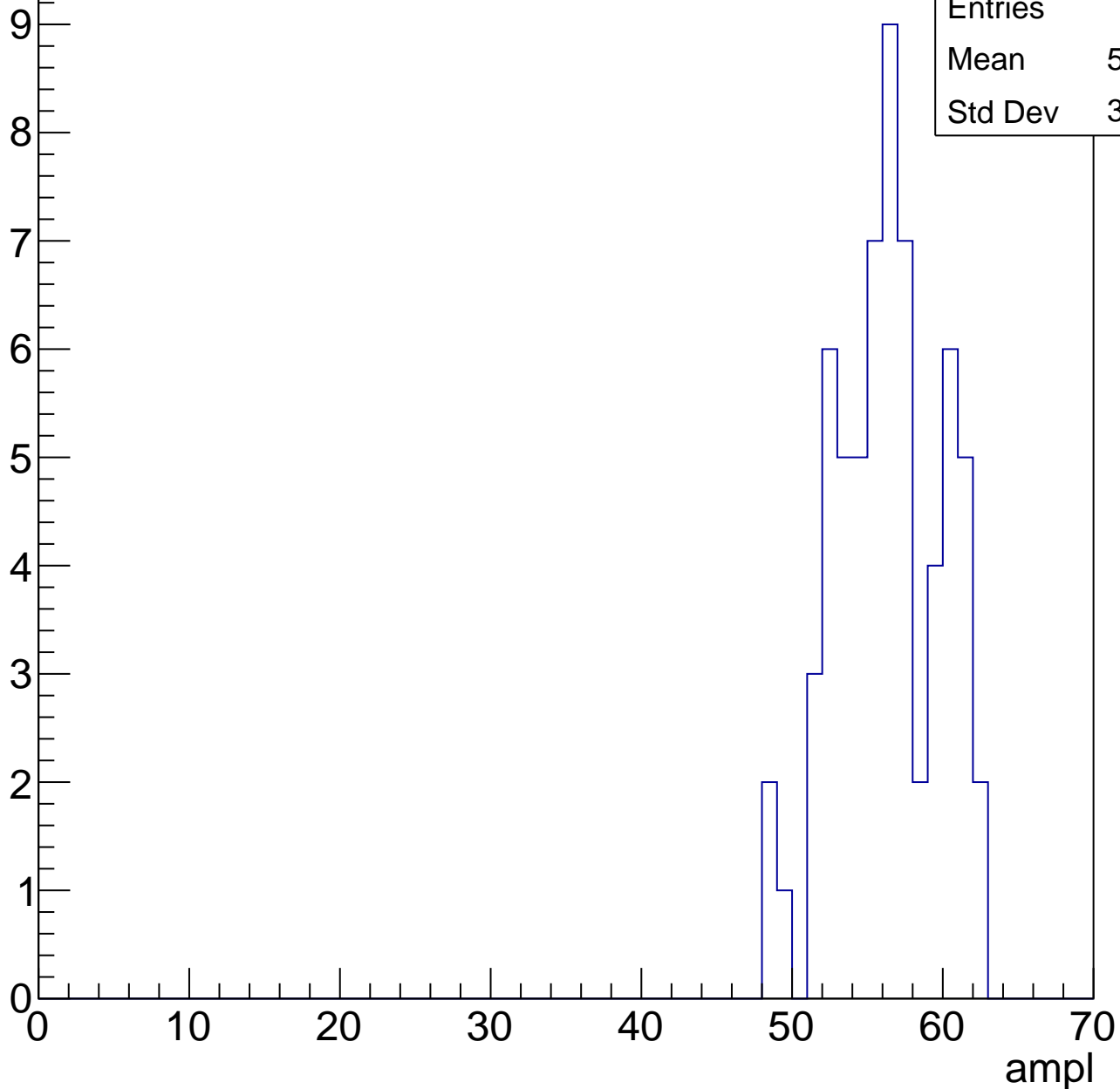
ampl



# B0L001S, U24-ch63, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

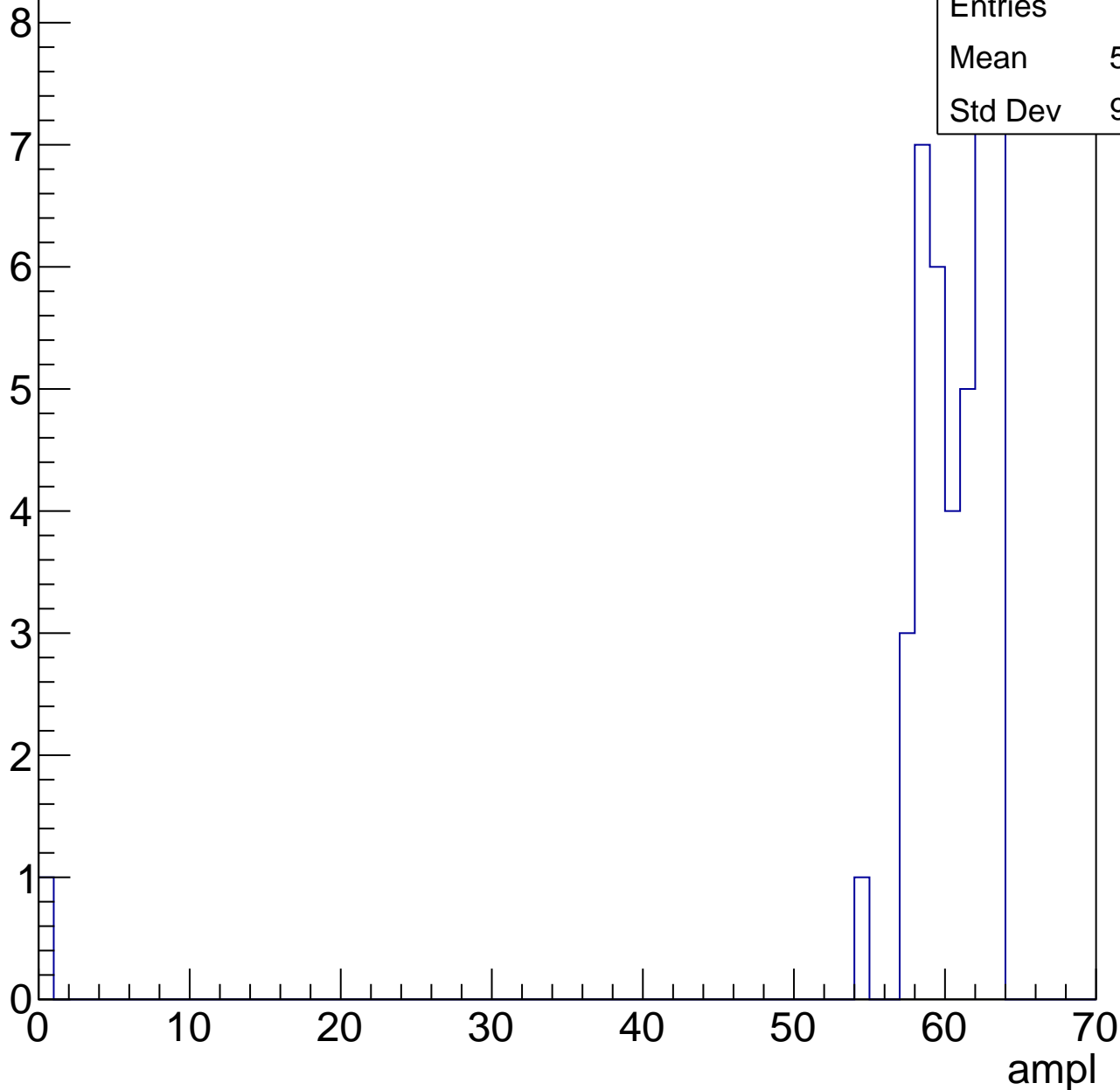


# B0L001S, U24-ch63, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	43
Mean	58.84
Std Dev	9.336



# B0L001S, U24-ch63, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	63
Std Dev	0

ampl



# B0L001S, U24-ch63, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	23
Std Dev	0

# B0L001S, U24-ch64, adc0

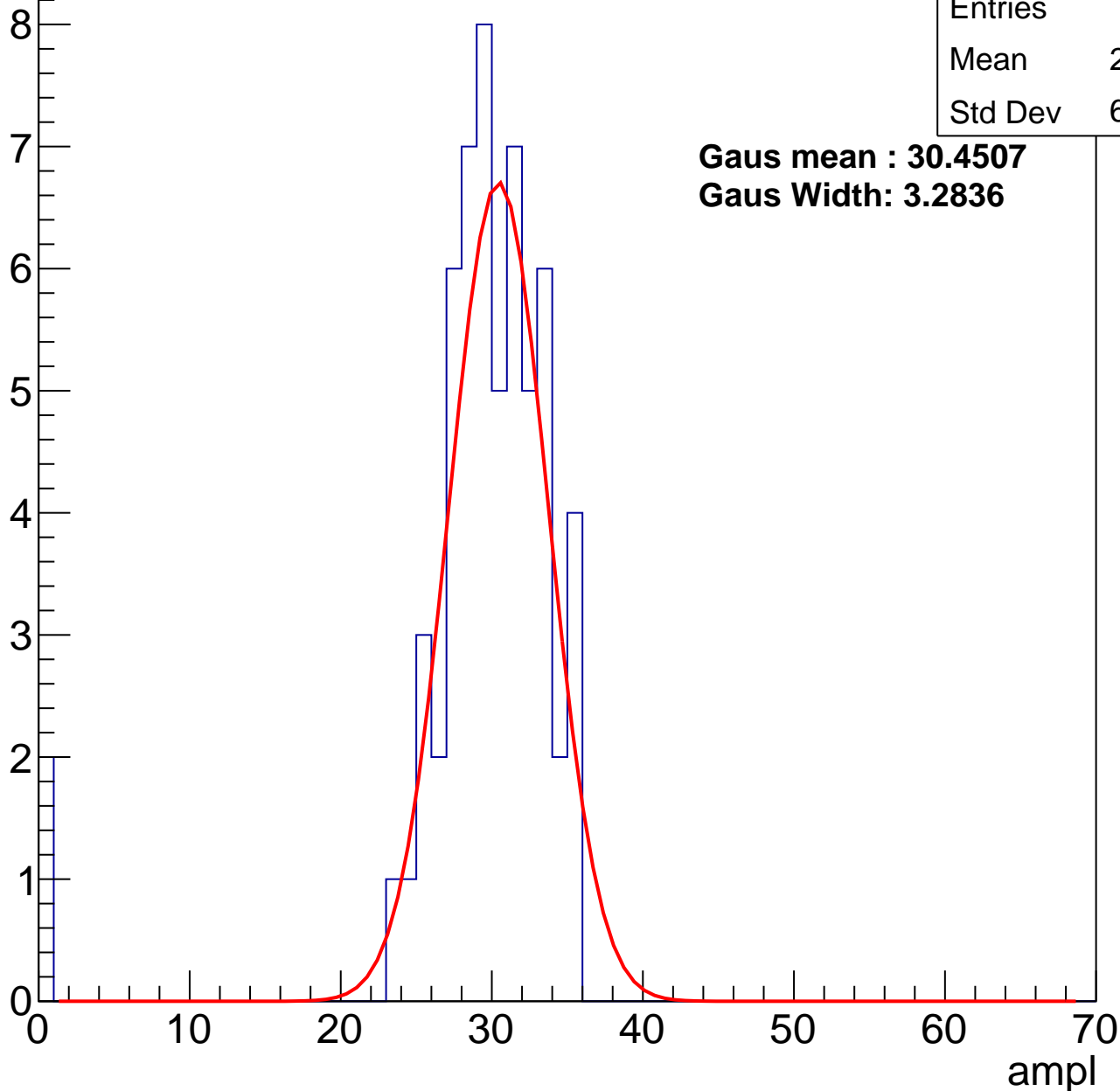
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	28.76
Std Dev	6.113

**Gaus mean : 30.4507**

**Gaus Width: 3.2836**



# B0L001S, U24-ch64, adc1

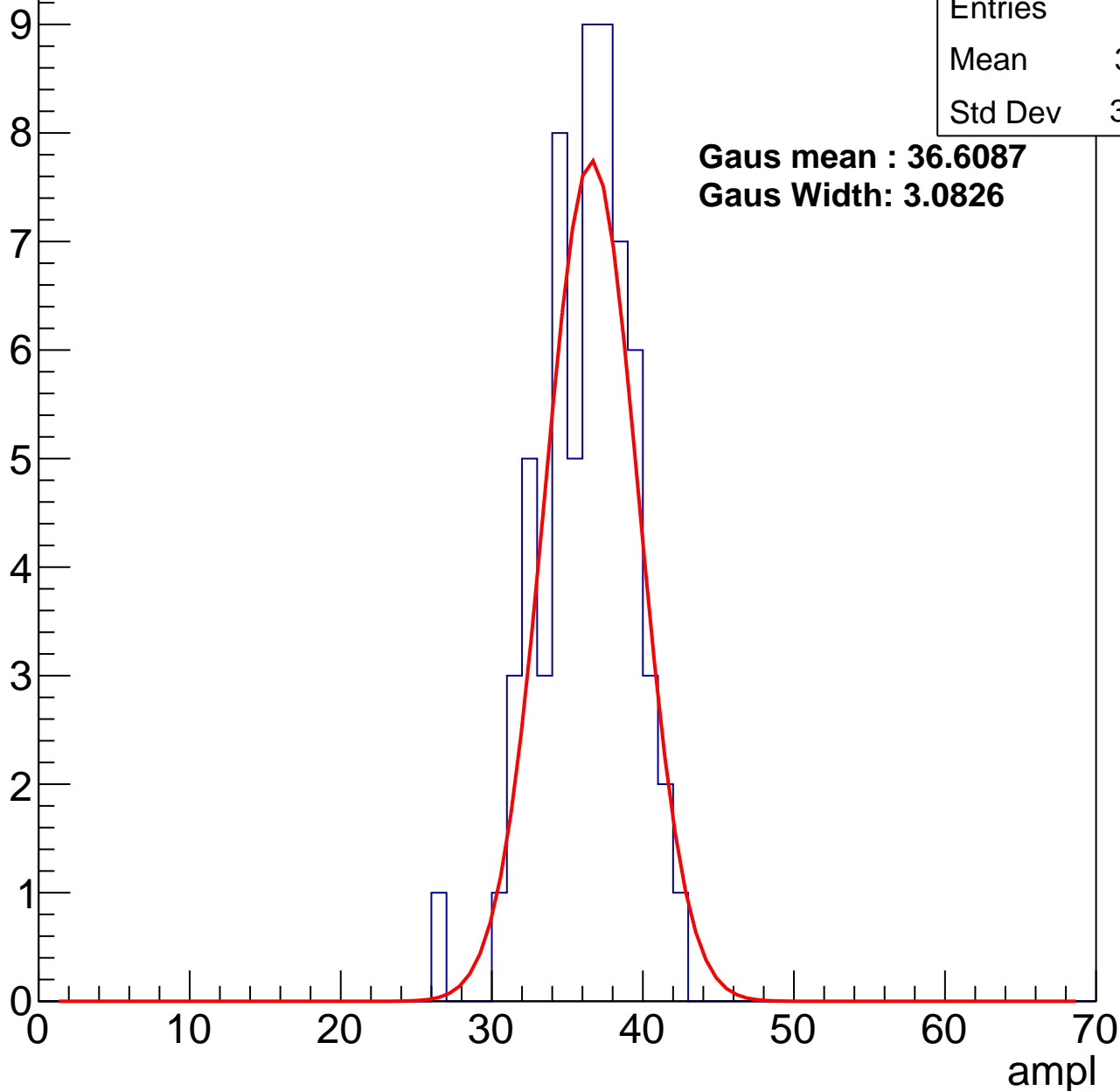
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	35.81
Std Dev	3.028

**Gaus mean : 36.6087**

**Gaus Width: 3.0826**



# B0L001S, U24-ch64, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	92
Mean	43.72
Std Dev	3.823

**Gaus mean : 44.2292**

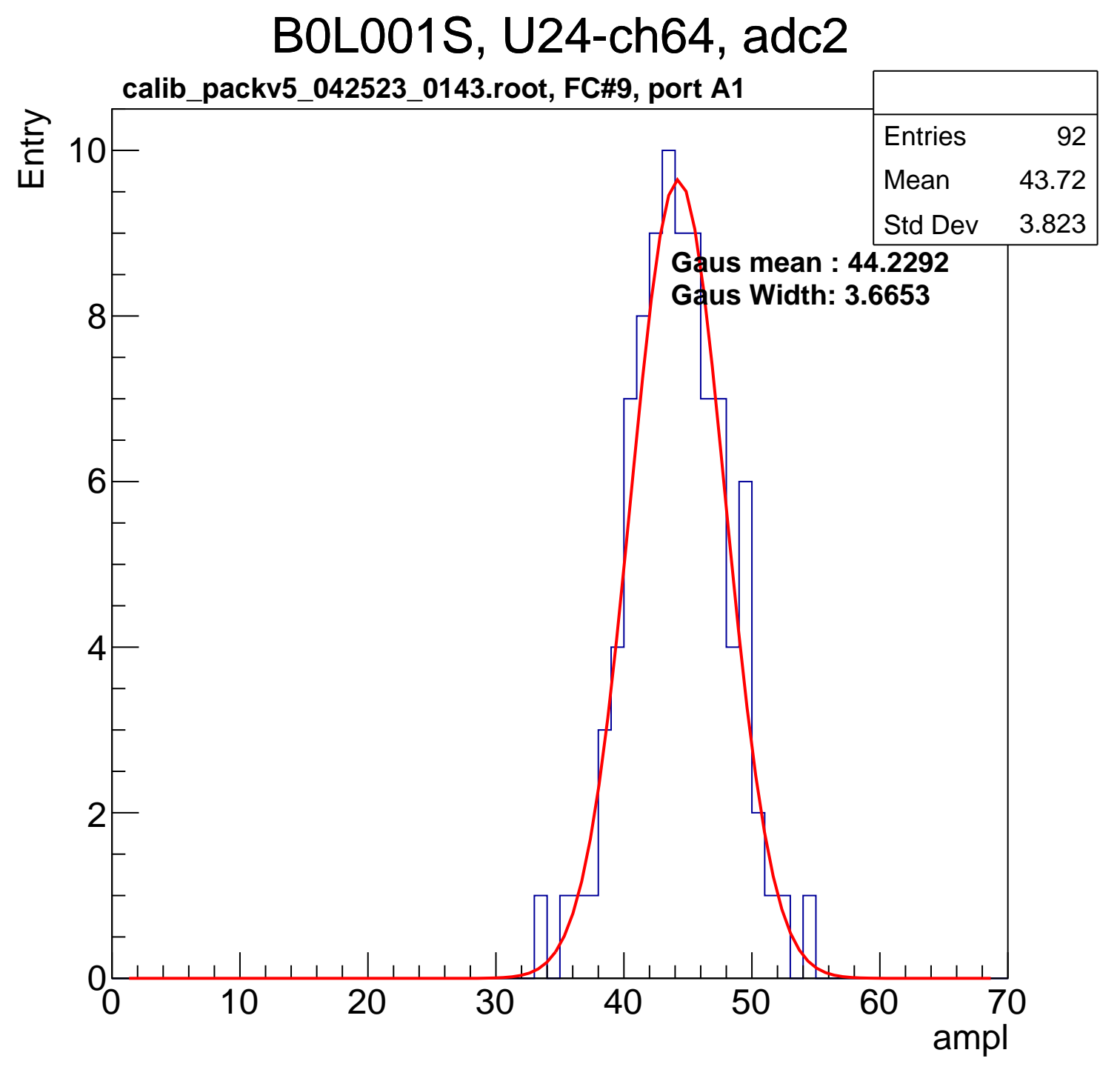
**Gaus Width: 3.6653**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

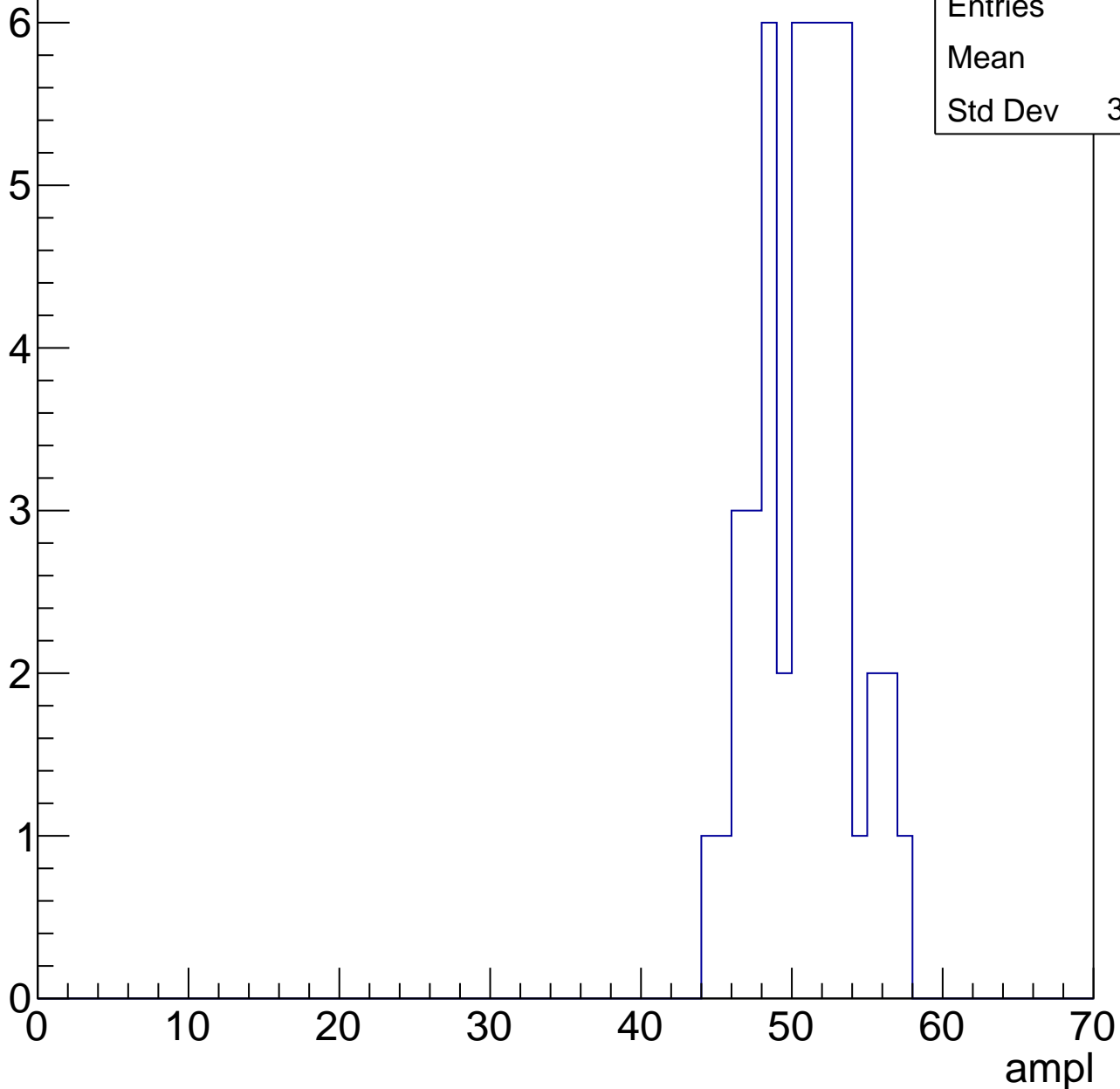


# B0L001S, U24-ch64, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

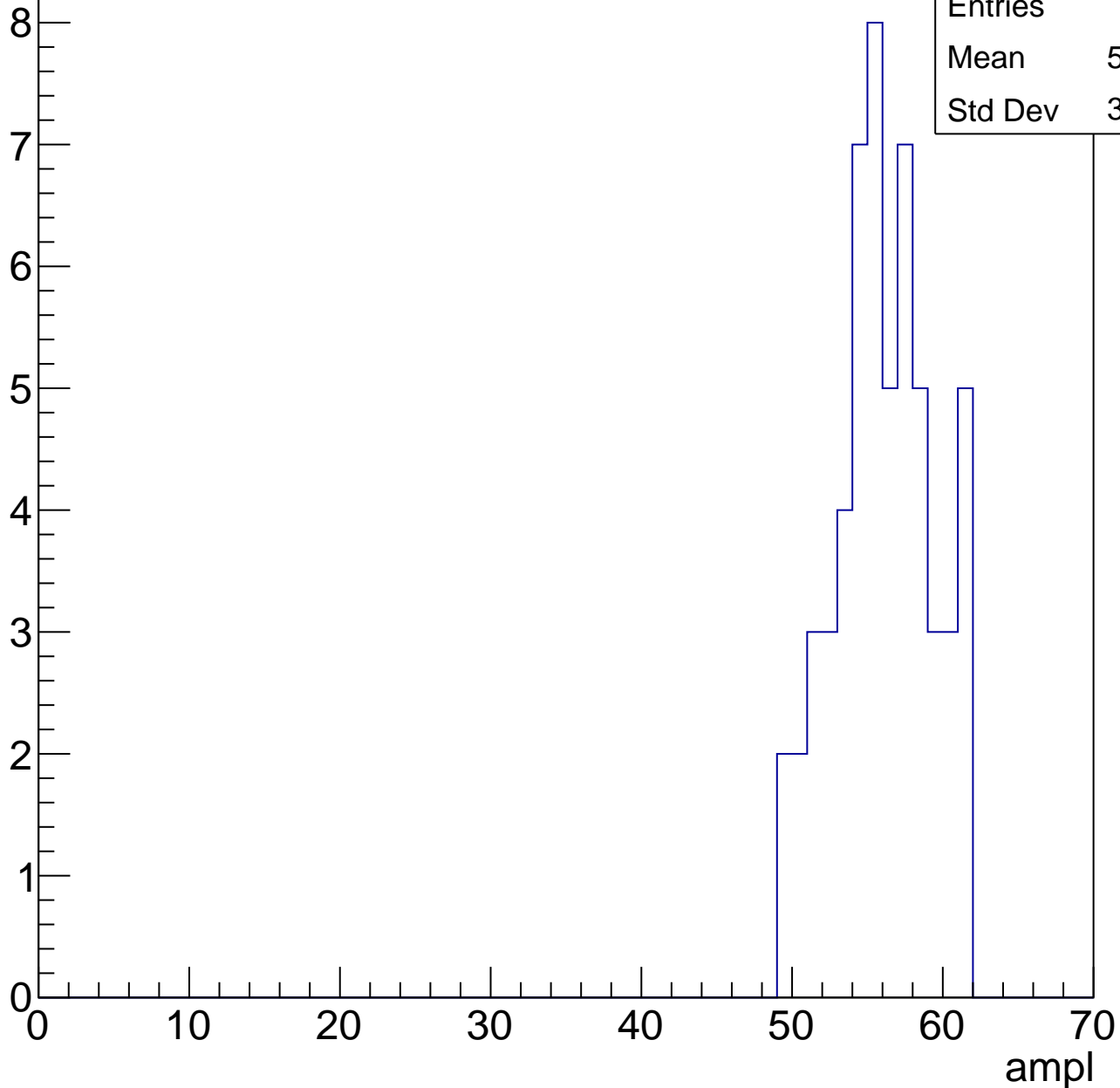
Entries	46
Mean	50.5
Std Dev	3.027



# B0L001S, U24-ch64, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



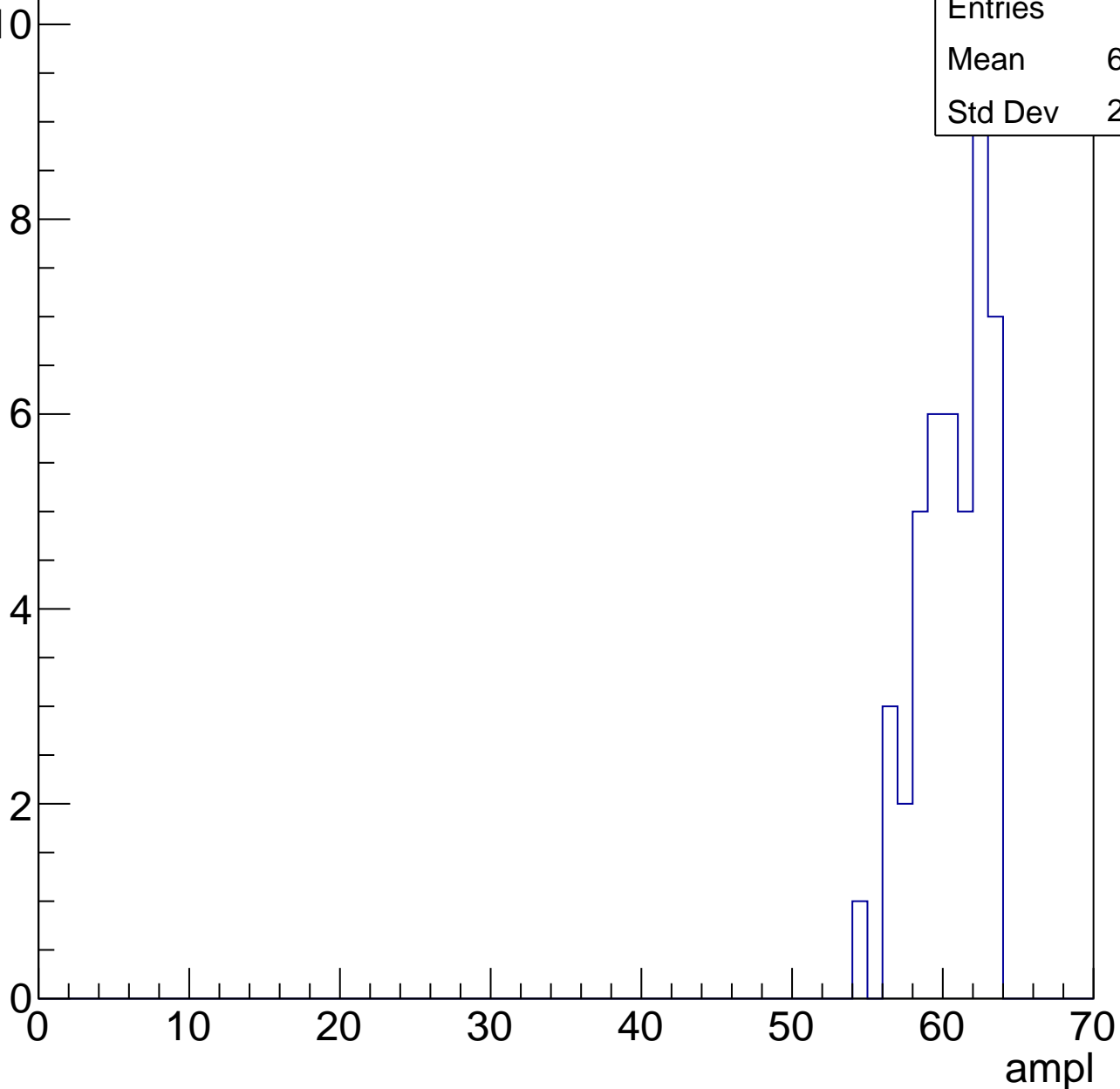
Entries	57
Mean	55.58
Std Dev	3.195

# B0L001S, U24-ch64, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

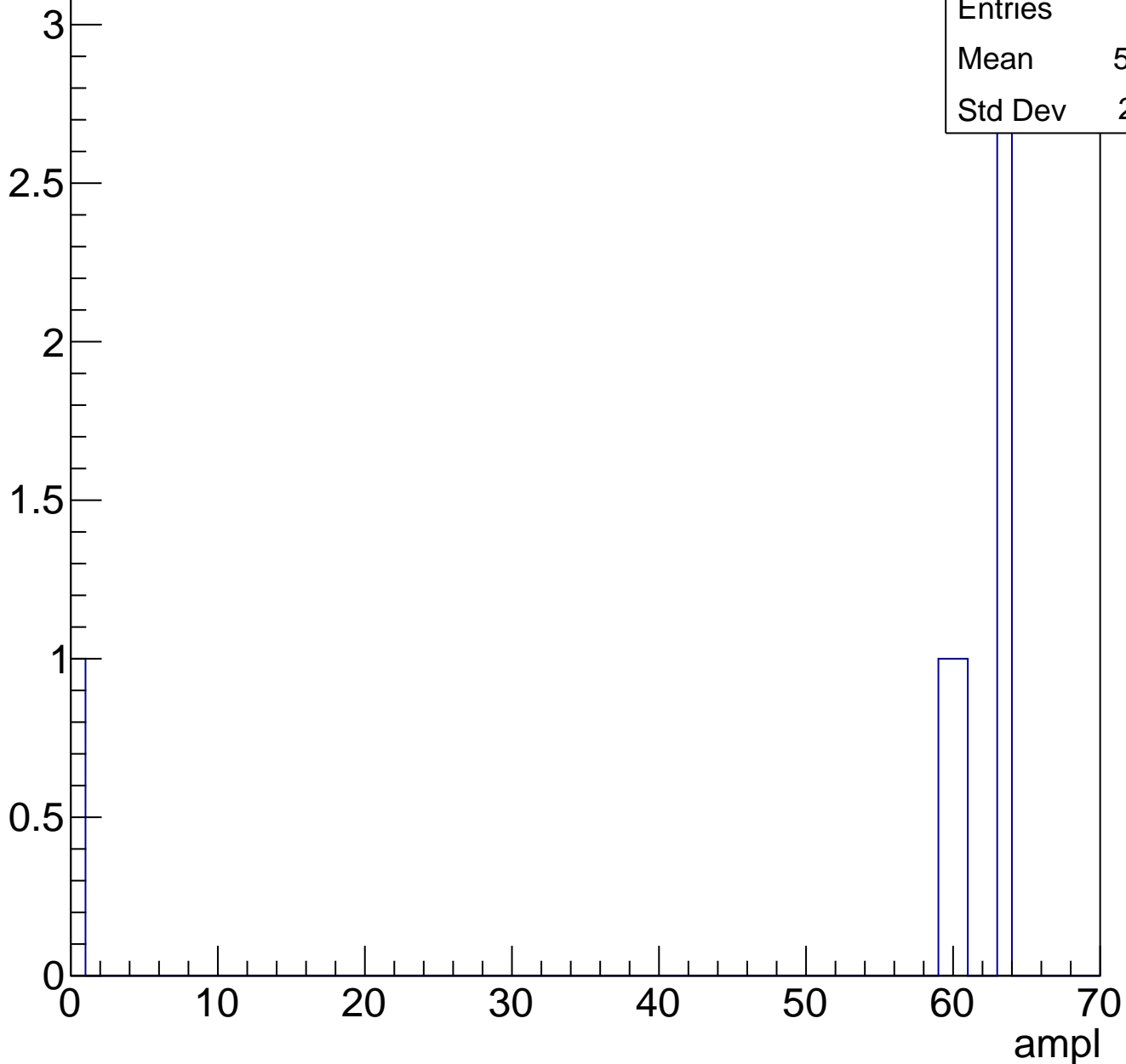
Entries	45
Mean	60.13
Std Dev	2.286



# B0L001S, U24-ch64, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch64, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U24-ch65, adc0

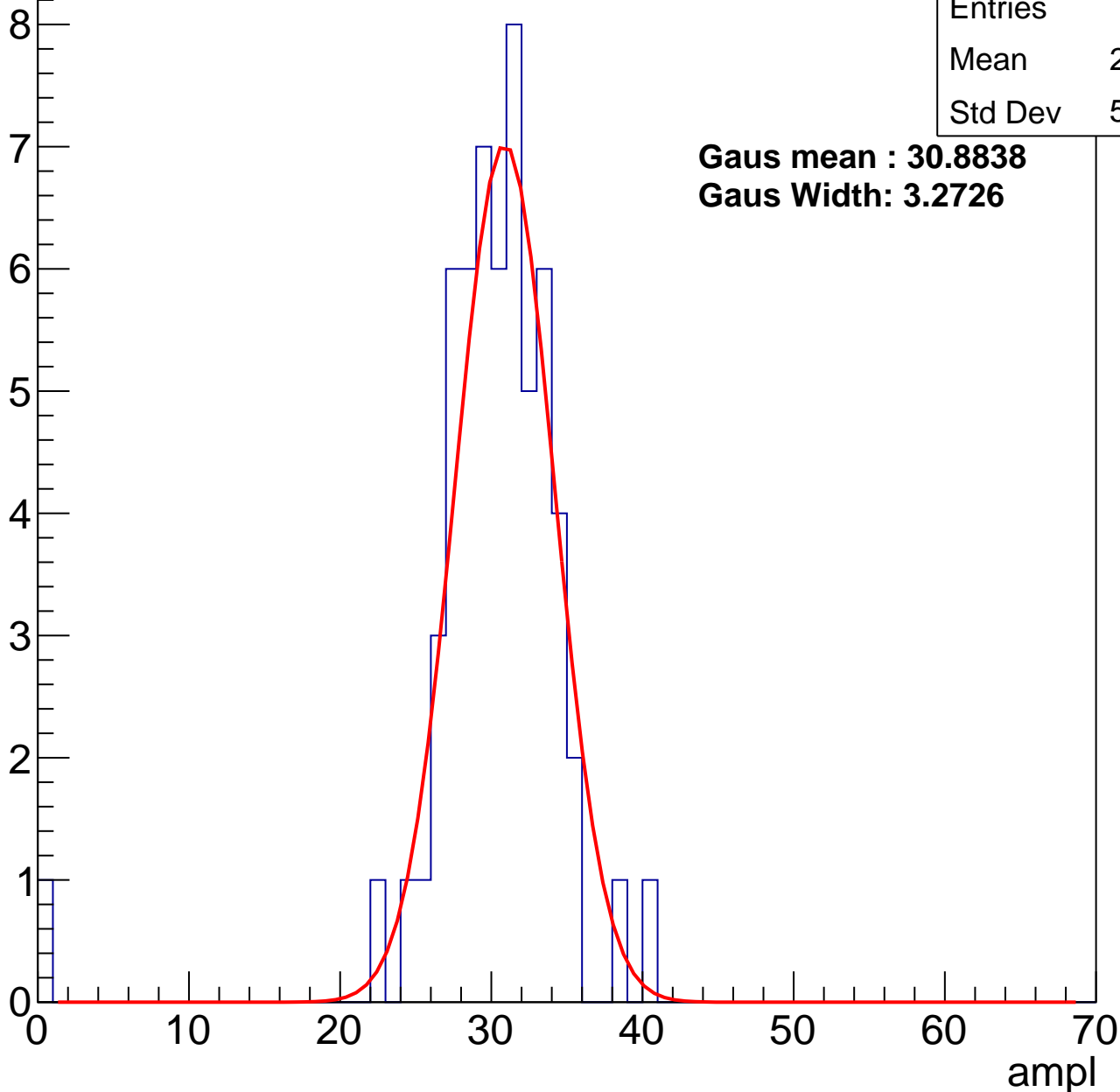
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	29.69
Std Dev	5.063

**Gaus mean : 30.8838**

**Gaus Width: 3.2726**



# B0L001S, U24-ch65, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	82
Mean	37.74
Std Dev	3.79

**Gaus mean : 37.8488**

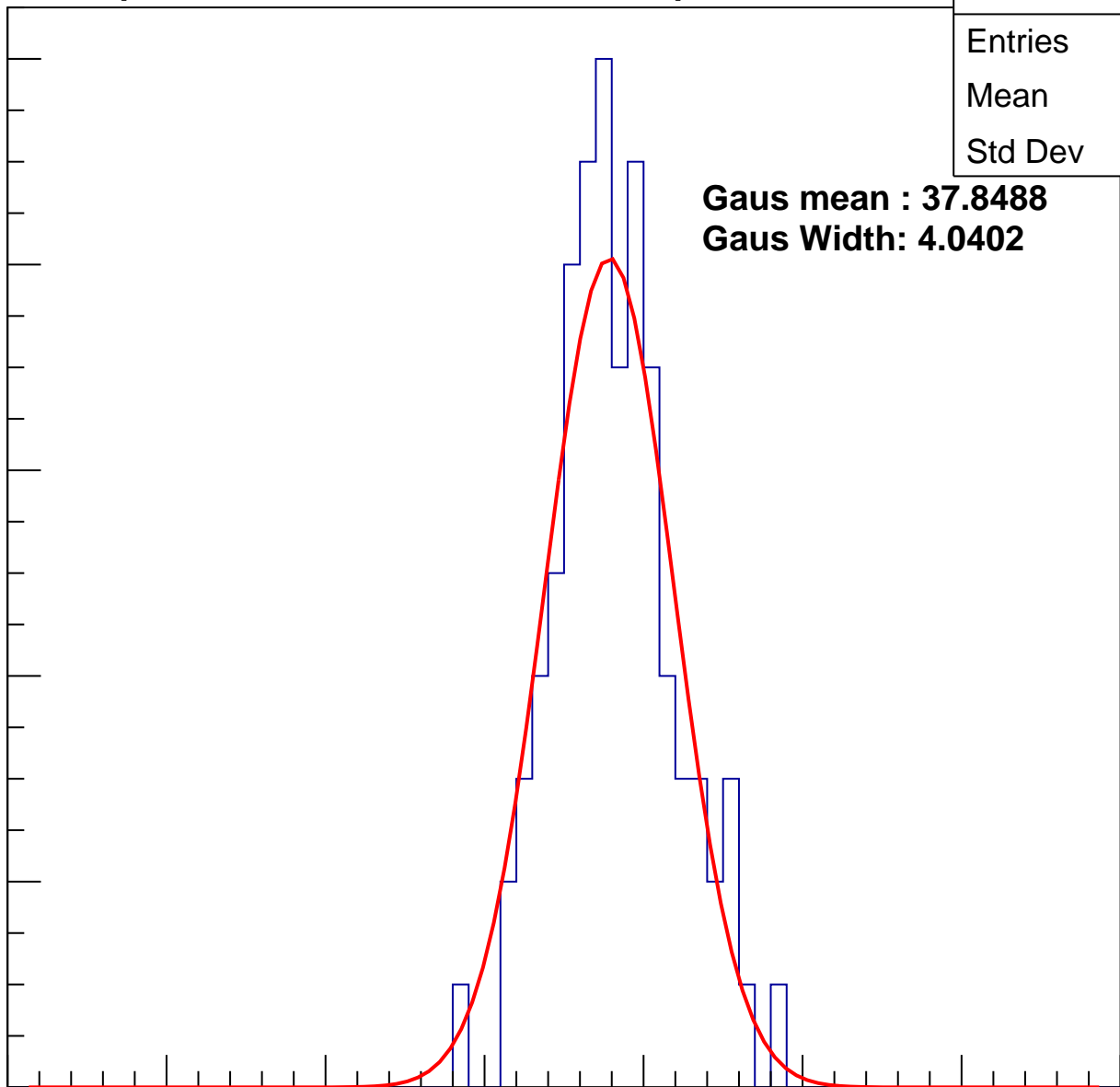
**Gaus Width: 4.0402**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B0L001S, U24-ch65, adc2

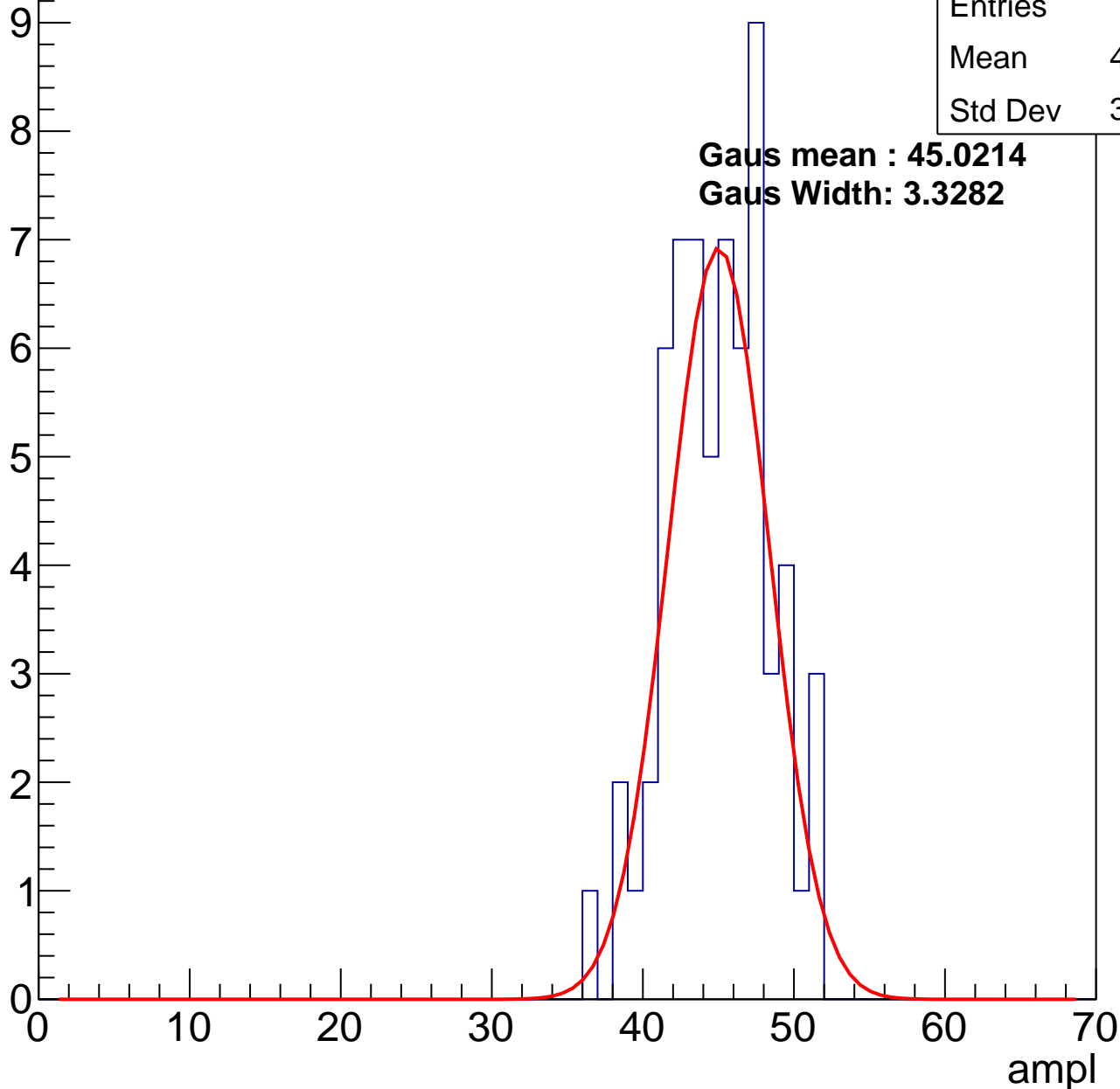
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	44.52
Std Dev	3.326

**Gaus mean : 45.0214**

**Gaus Width: 3.3282**

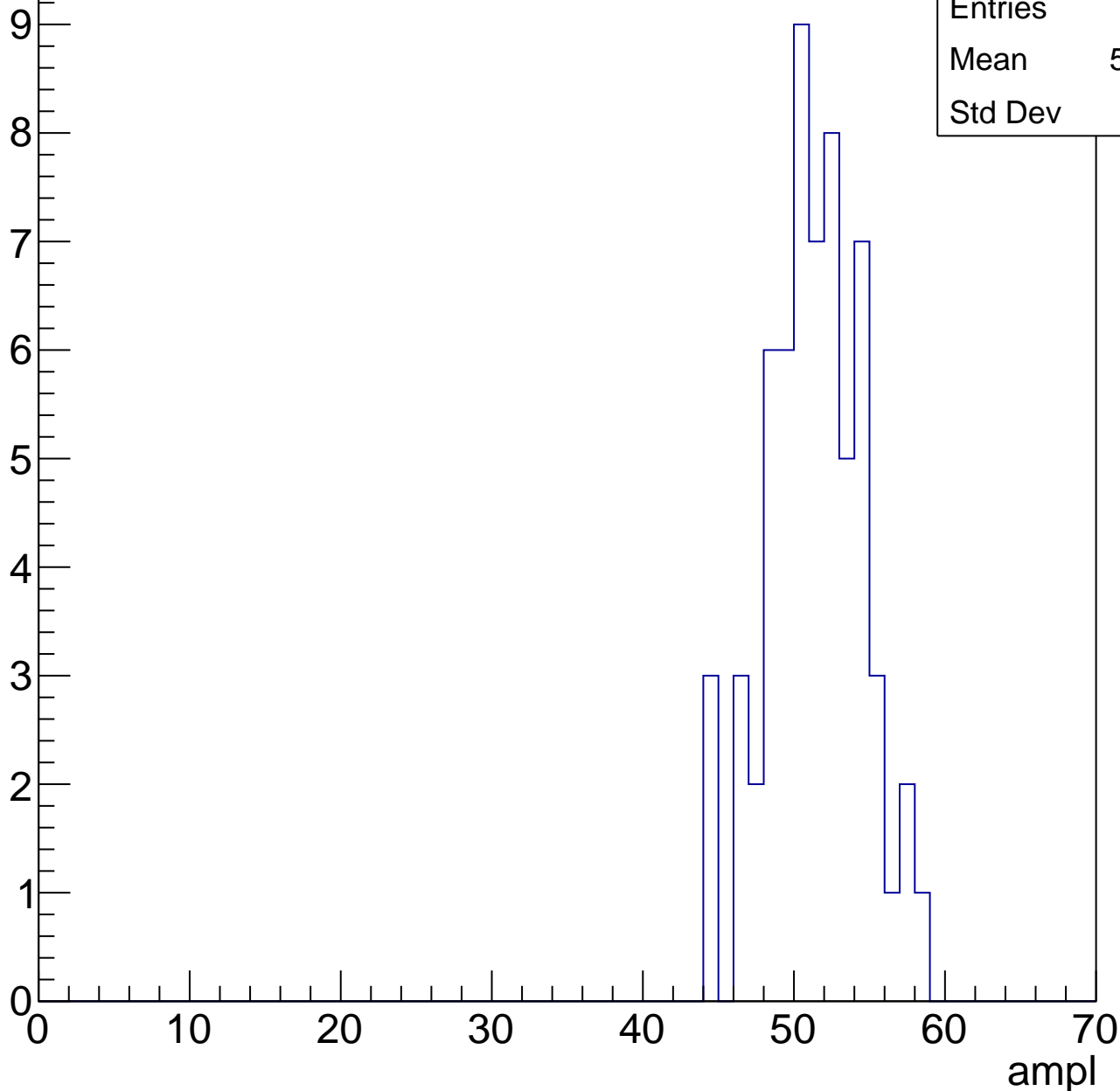


# B0L001S, U24-ch65, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	50.87
Std Dev	3.15

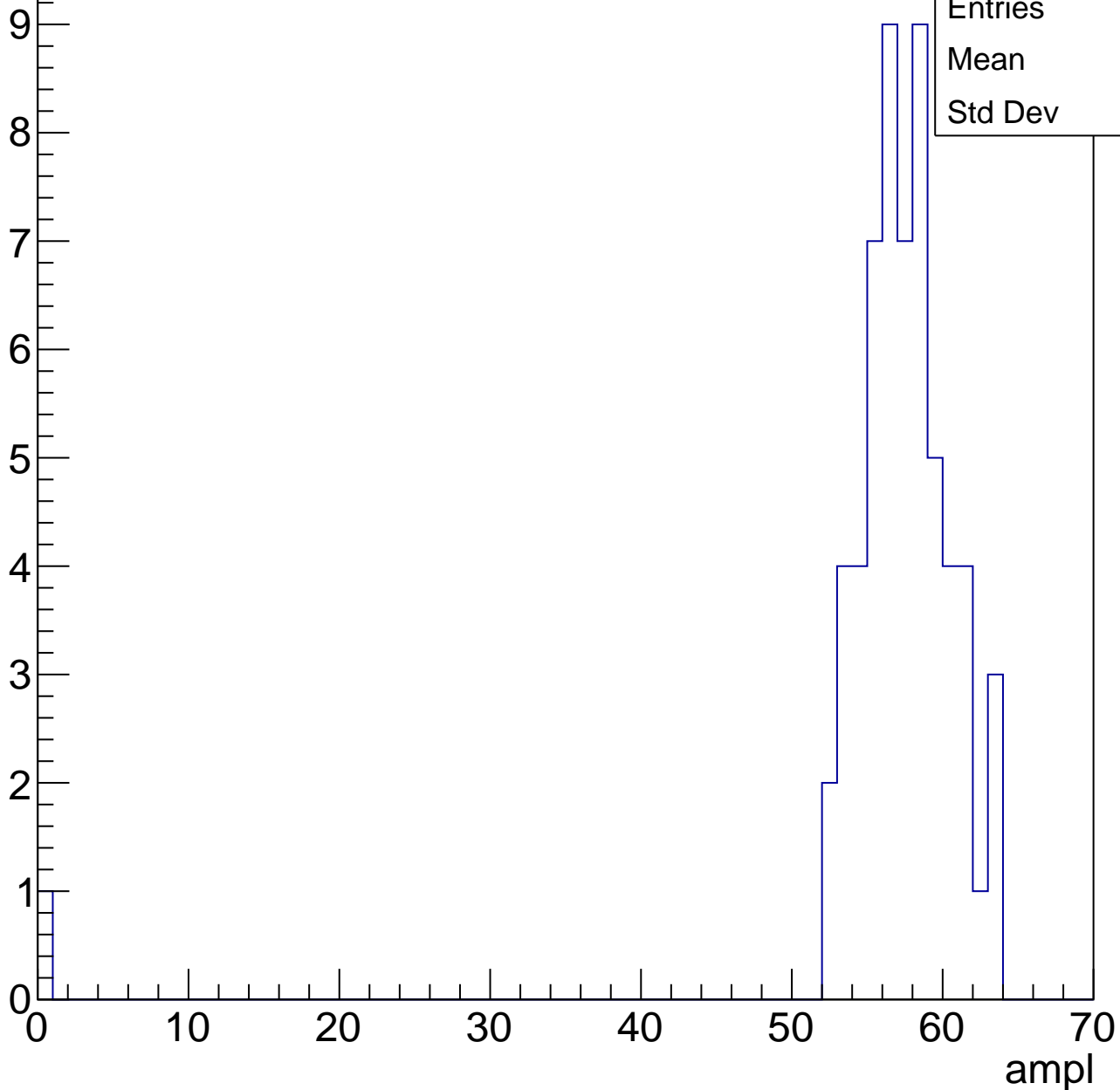


# B0L001S, U24-ch65, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	56.2
Std Dev	7.81

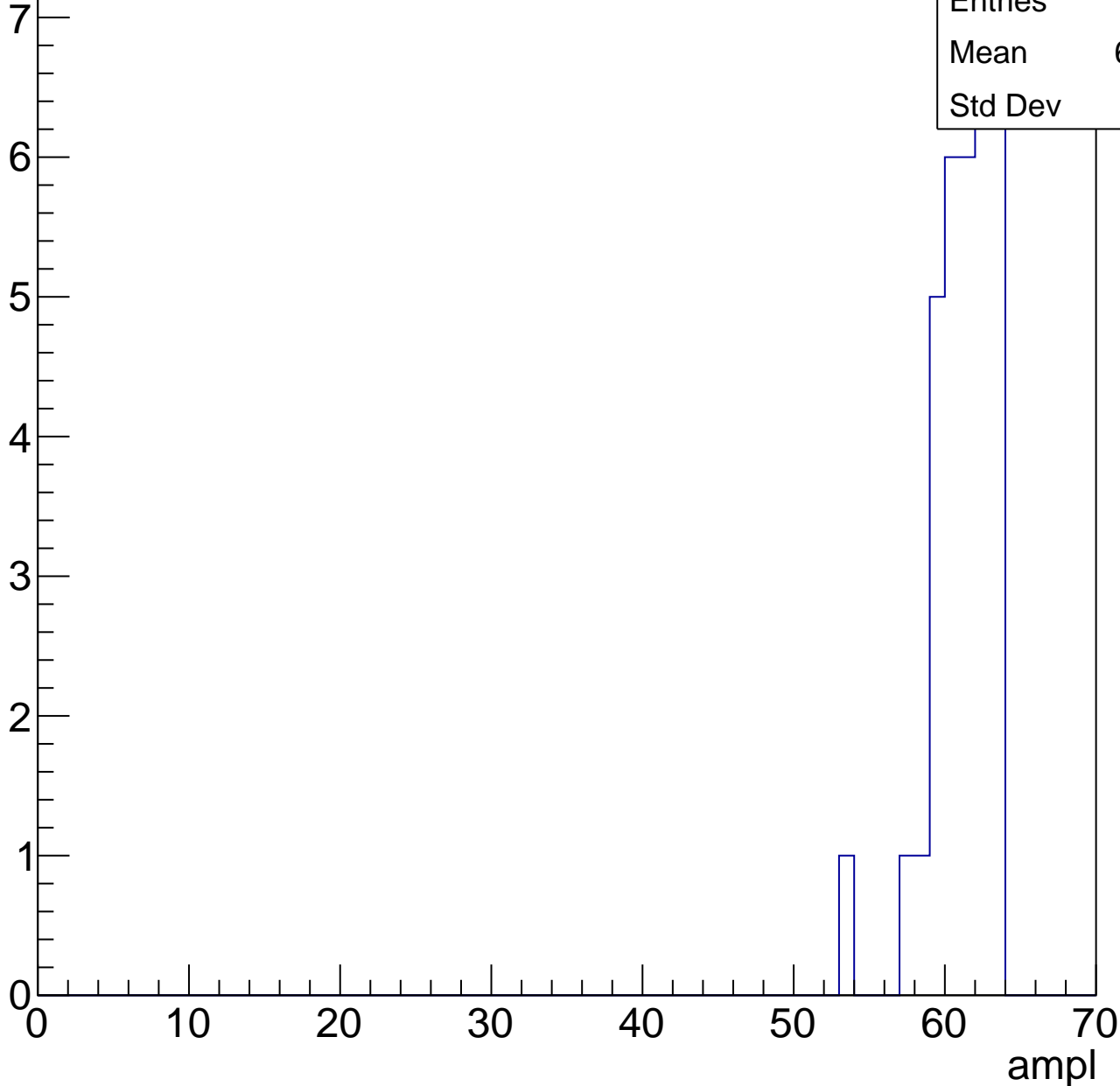


# B0L001S, U24-ch65, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	34
Mean	60.71
Std Dev	2.08



# B0L001S, U24-ch65, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	62
Std Dev	0

ampl



# B0L001S, U24-ch65, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U24-ch66, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	94
Mean	31.37
Std Dev	3.867

**Gaus mean : 31.6739**

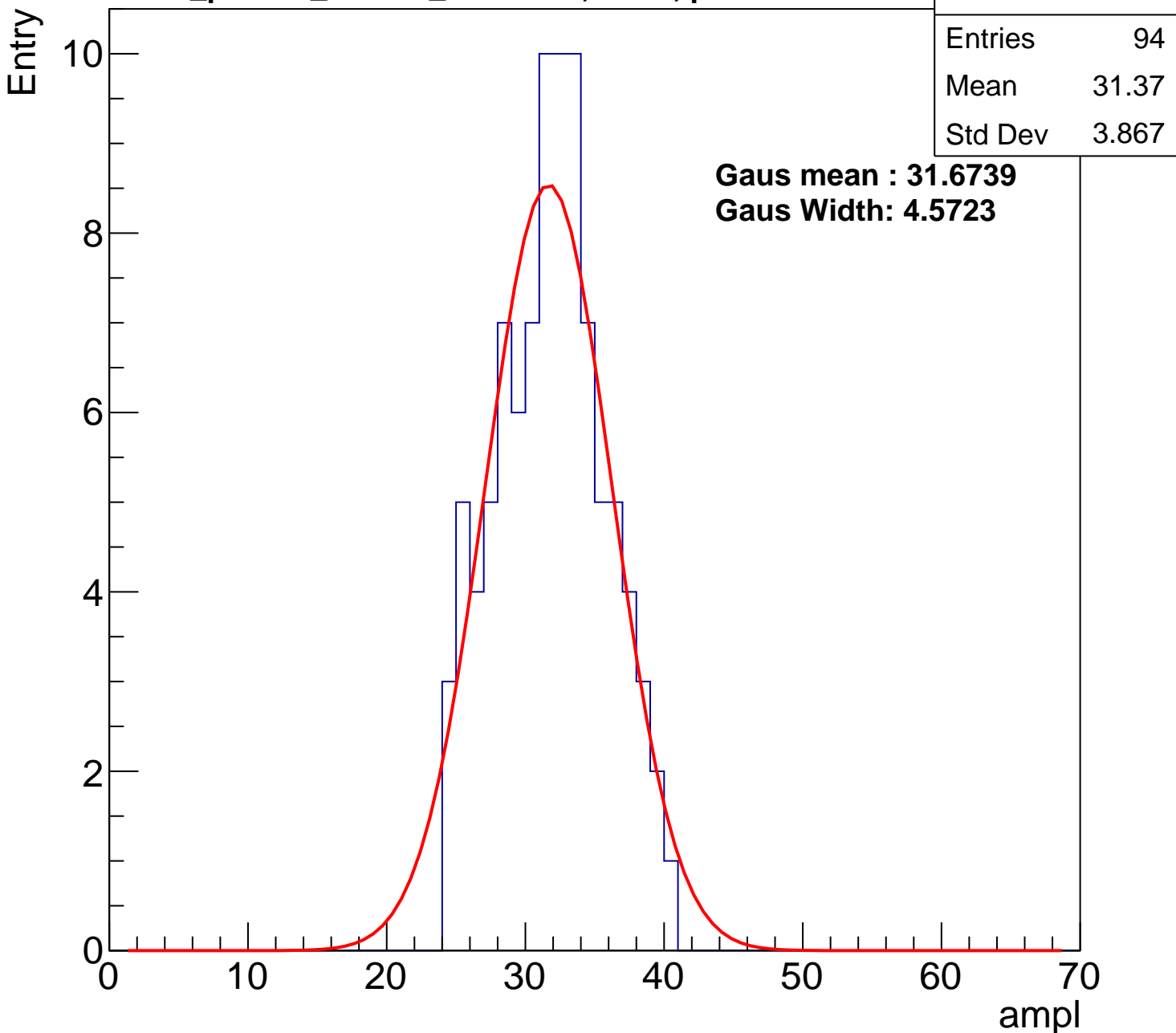
**Gaus Width: 4.5723**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U24-ch66, adc1

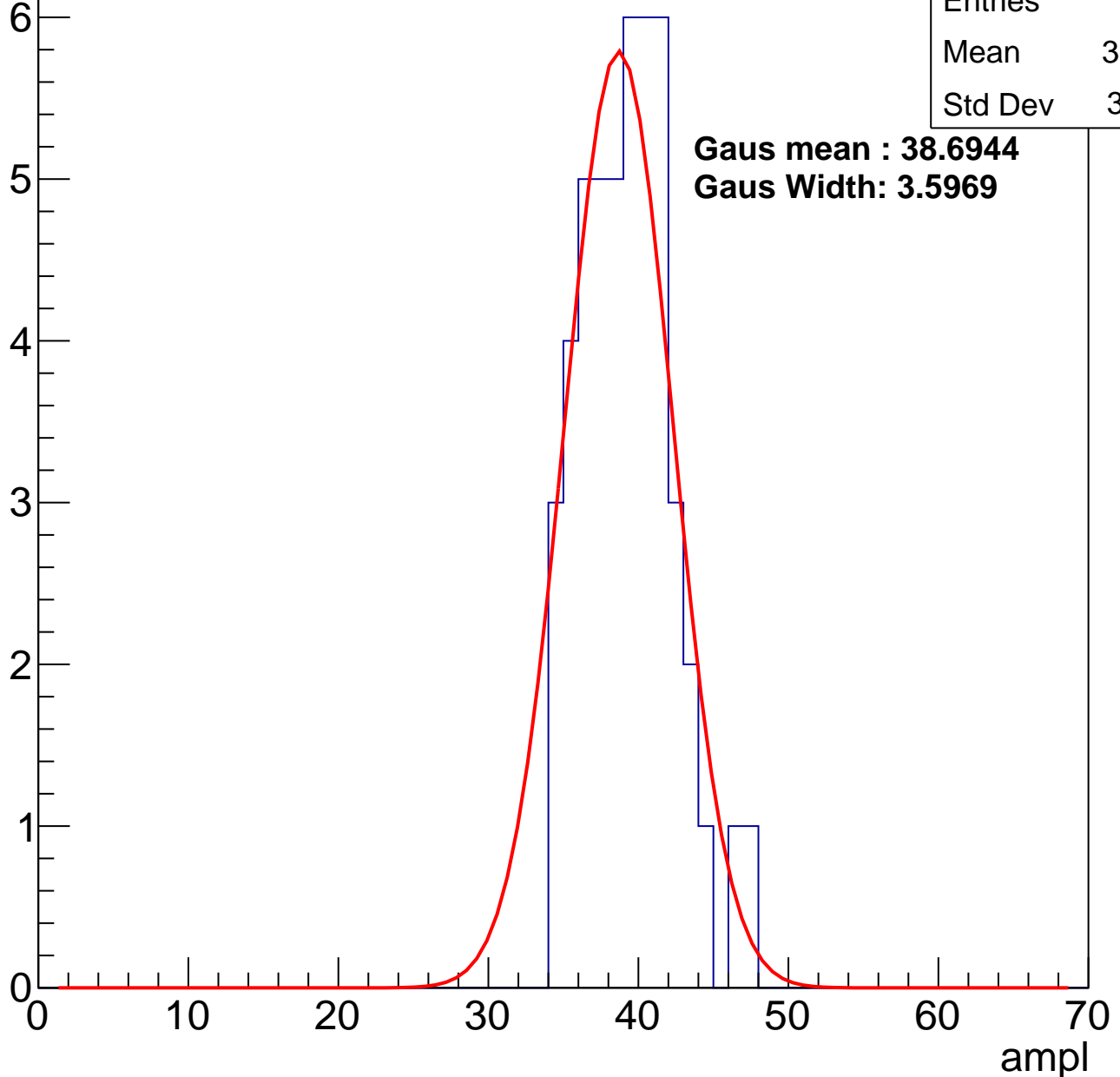
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	48
Mean	38.88
Std Dev	3.011

**Gaus mean : 38.6944**

**Gaus Width: 3.5969**

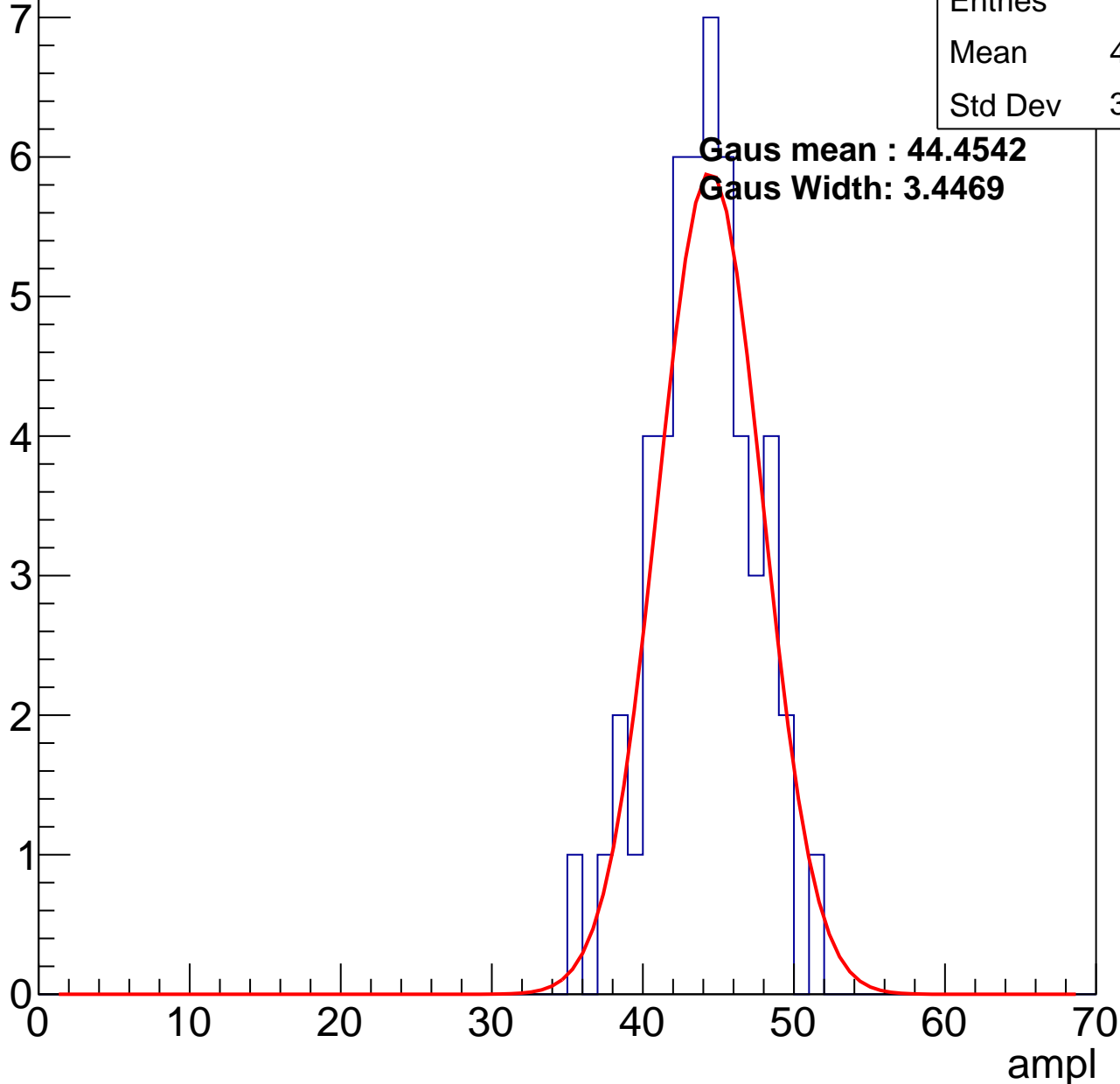


# B0L001S, U24-ch66, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

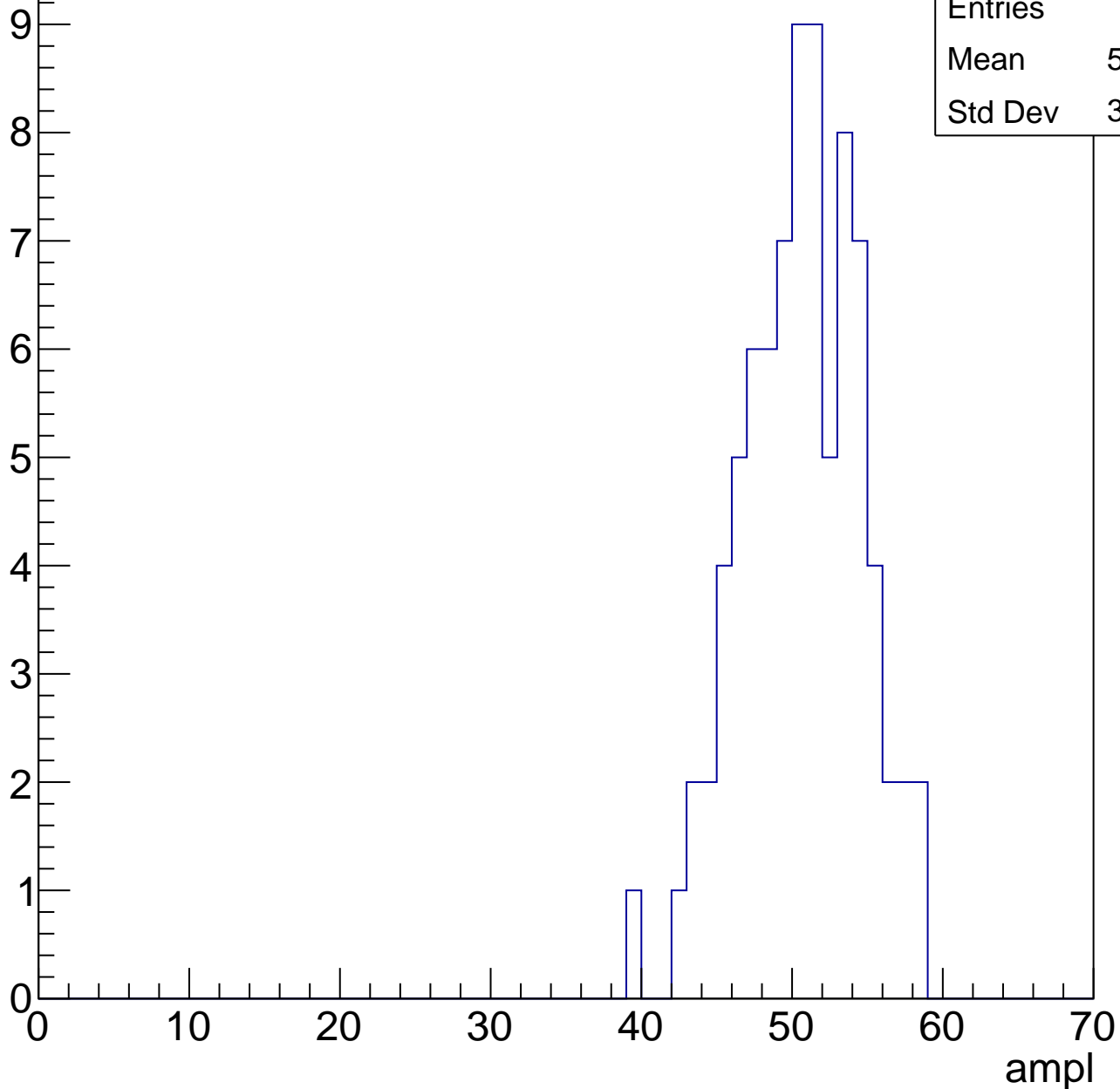
Entries	52
Mean	43.56
Std Dev	3.278



# B0L001S, U24-ch66, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



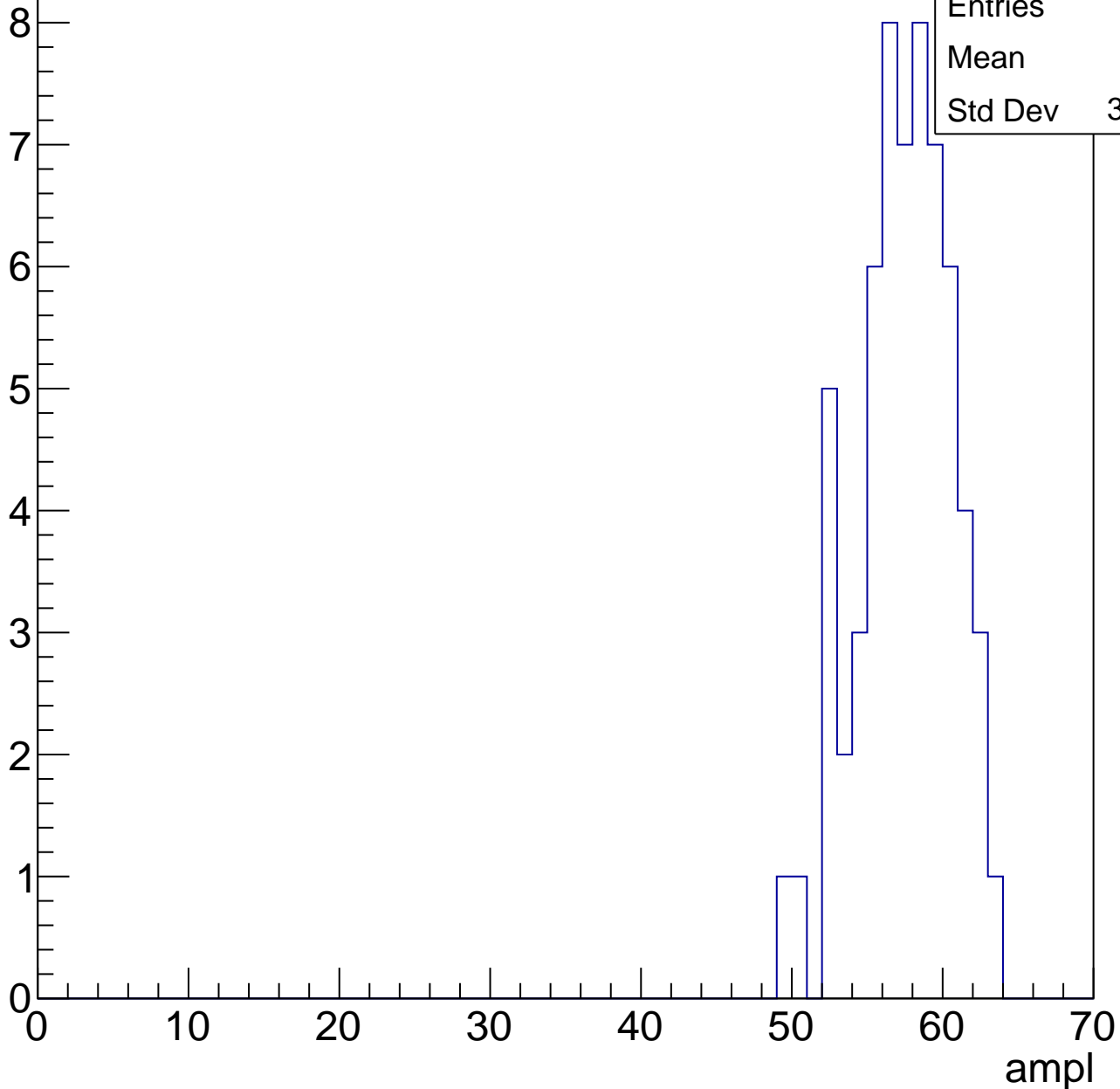
Entries	82
Mean	50.13
Std Dev	3.872

# B0L001S, U24-ch66, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	57
Std Dev	3.095

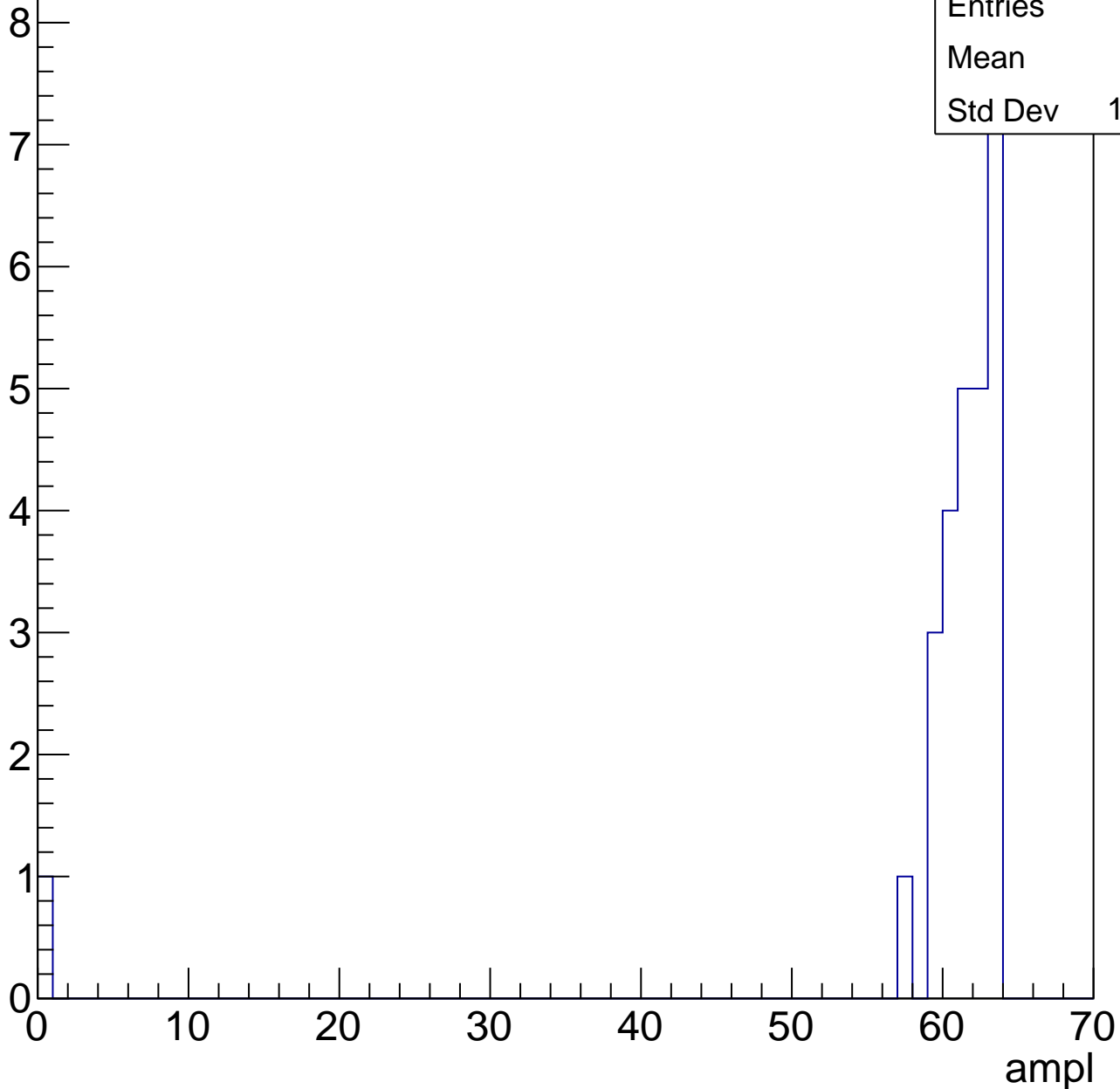


# B0L001S, U24-ch66, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

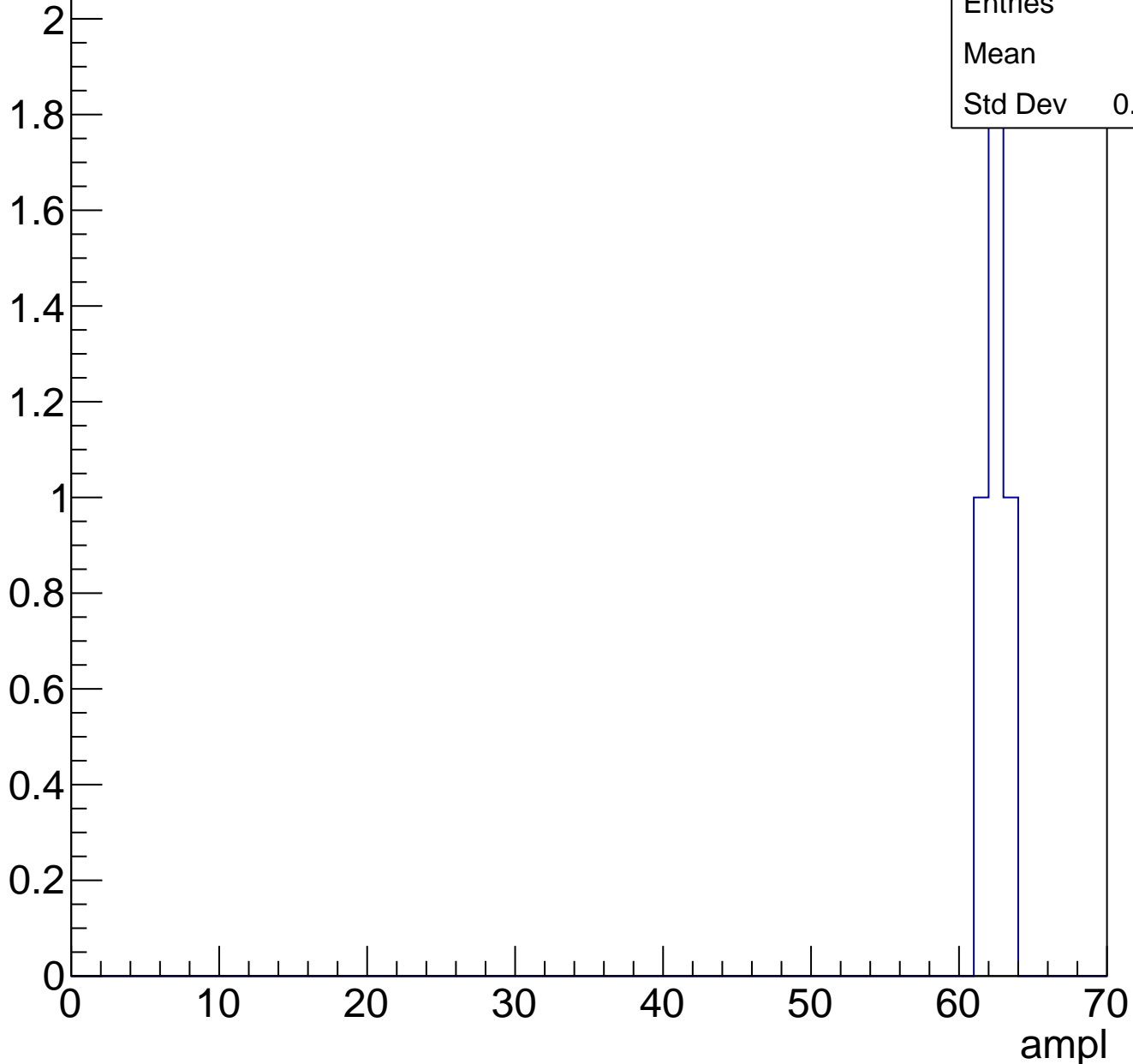
Entries	27
Mean	59
Std Dev	11.68



# B0L001S, U24-ch66, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch66, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L001S, U24-ch67, adc0

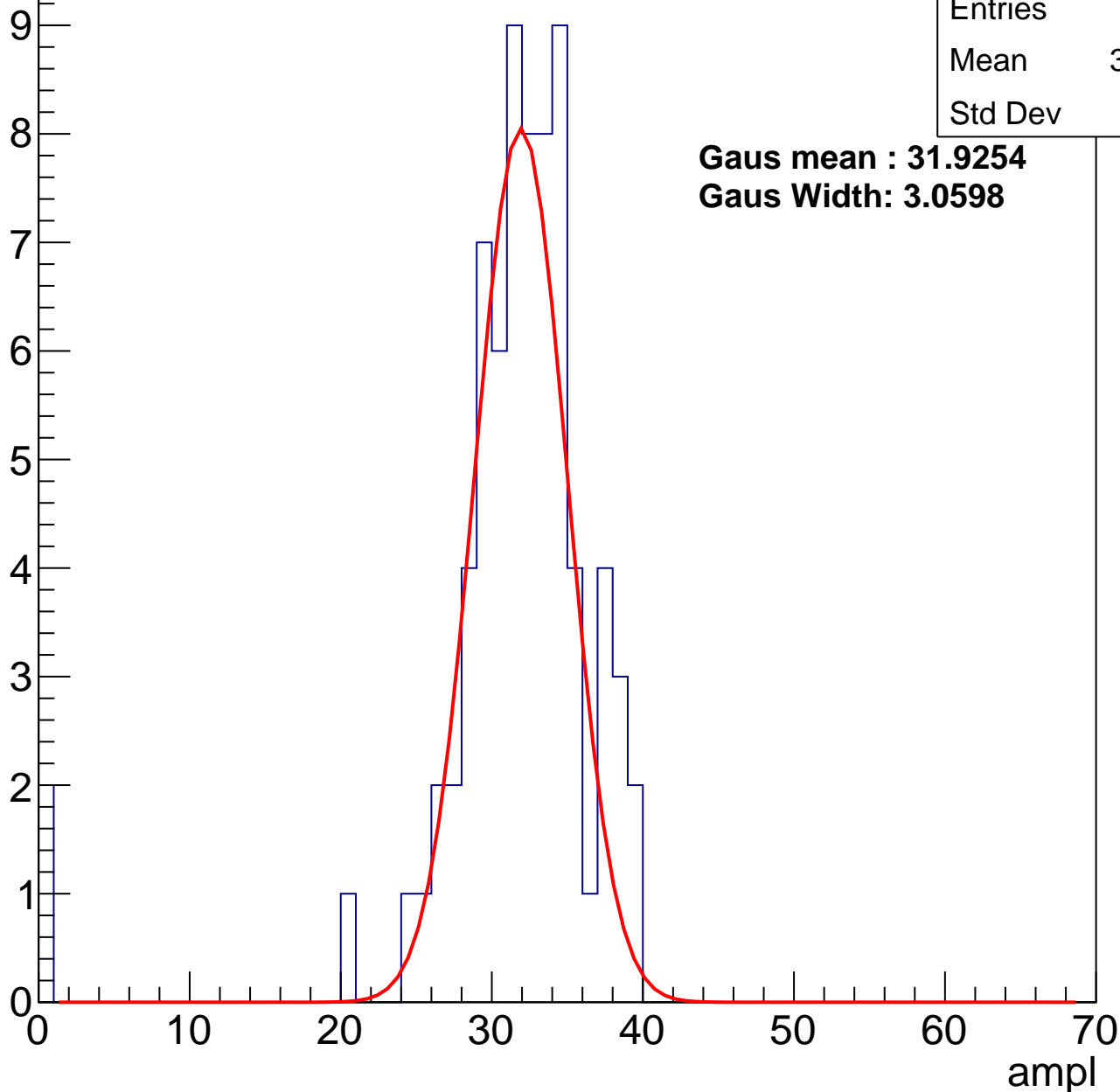
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	30.96
Std Dev	6.27

**Gaus mean : 31.9254**

**Gaus Width: 3.0598**



# B0L001S, U24-ch67, adc1

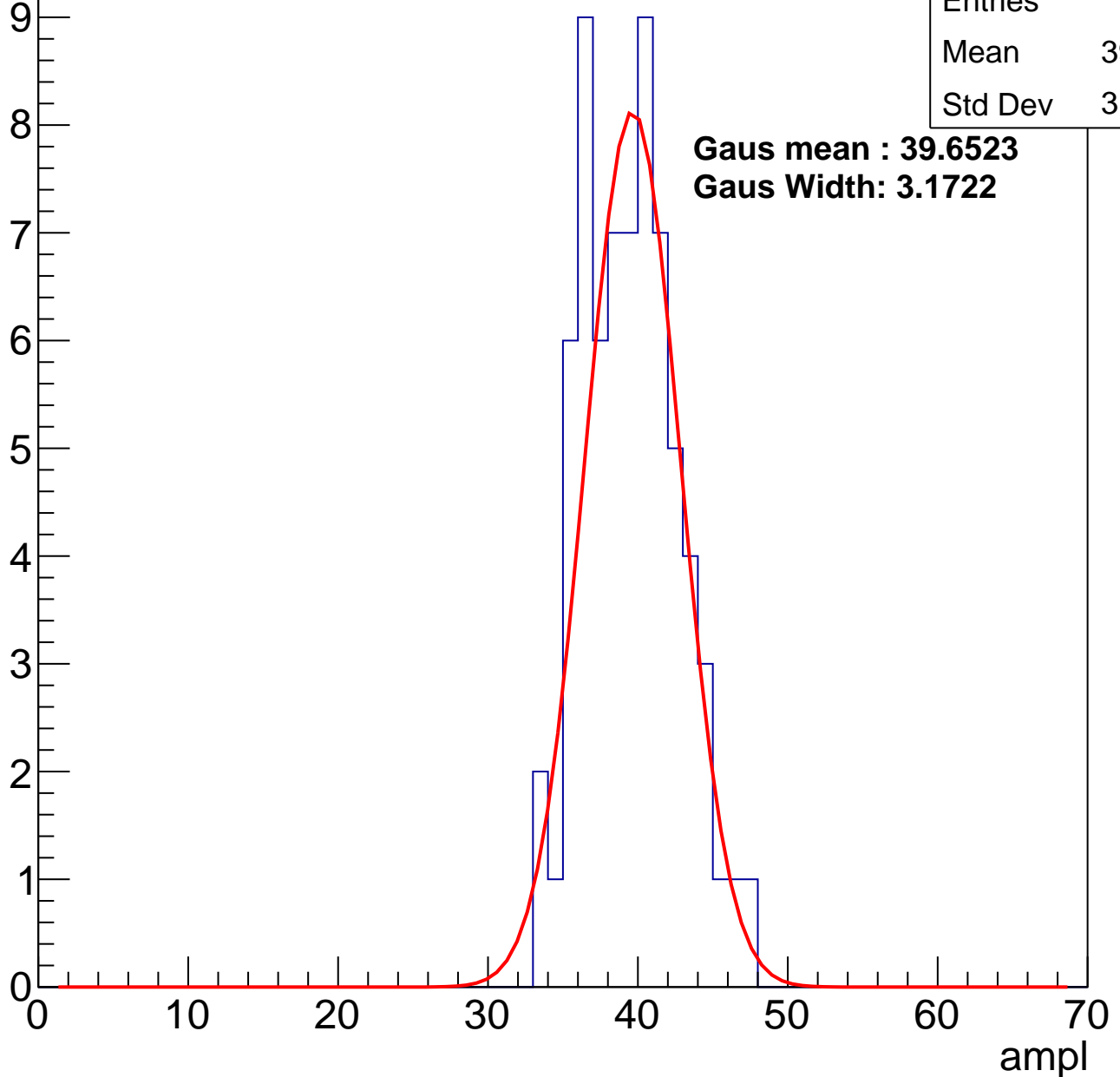
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	39.04
Std Dev	3.127

**Gaus mean : 39.6523**

**Gaus Width: 3.1722**



# B0L001S, U24-ch67, adc2

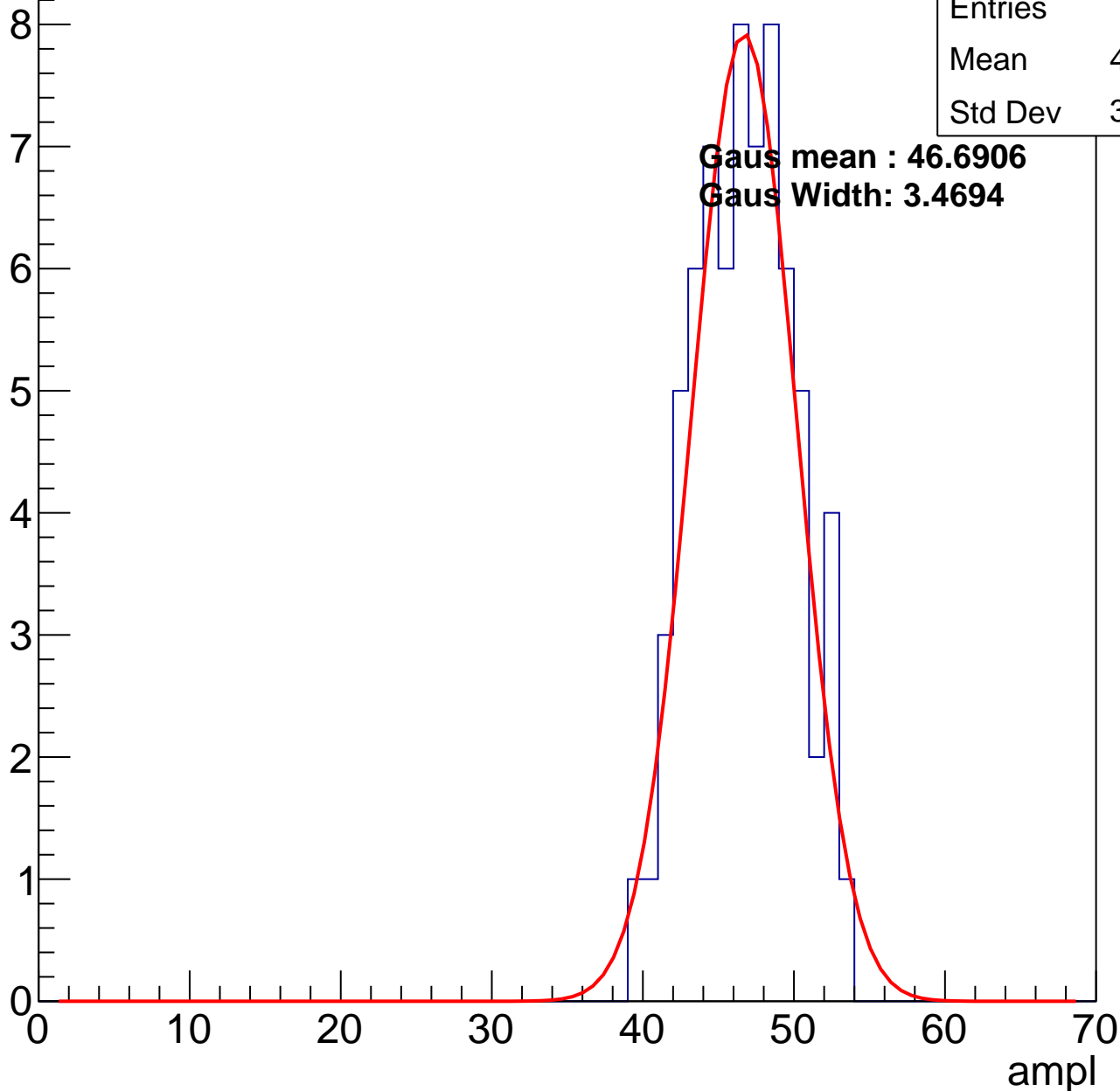
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	46.23
Std Dev	3.252

**Gaus mean : 46.6906**

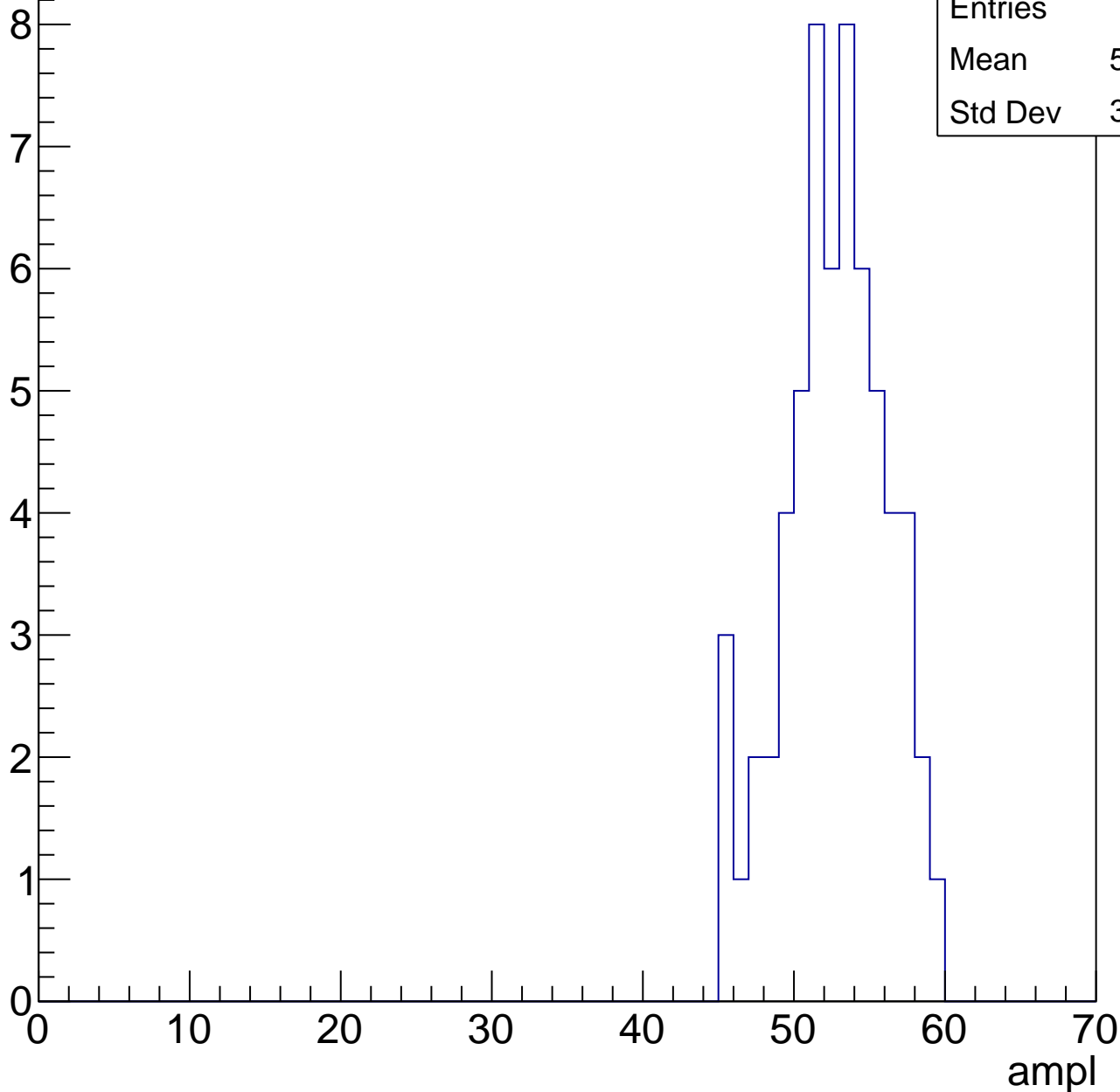
**Gaus Width: 3.4694**



# B0L001S, U24-ch67, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

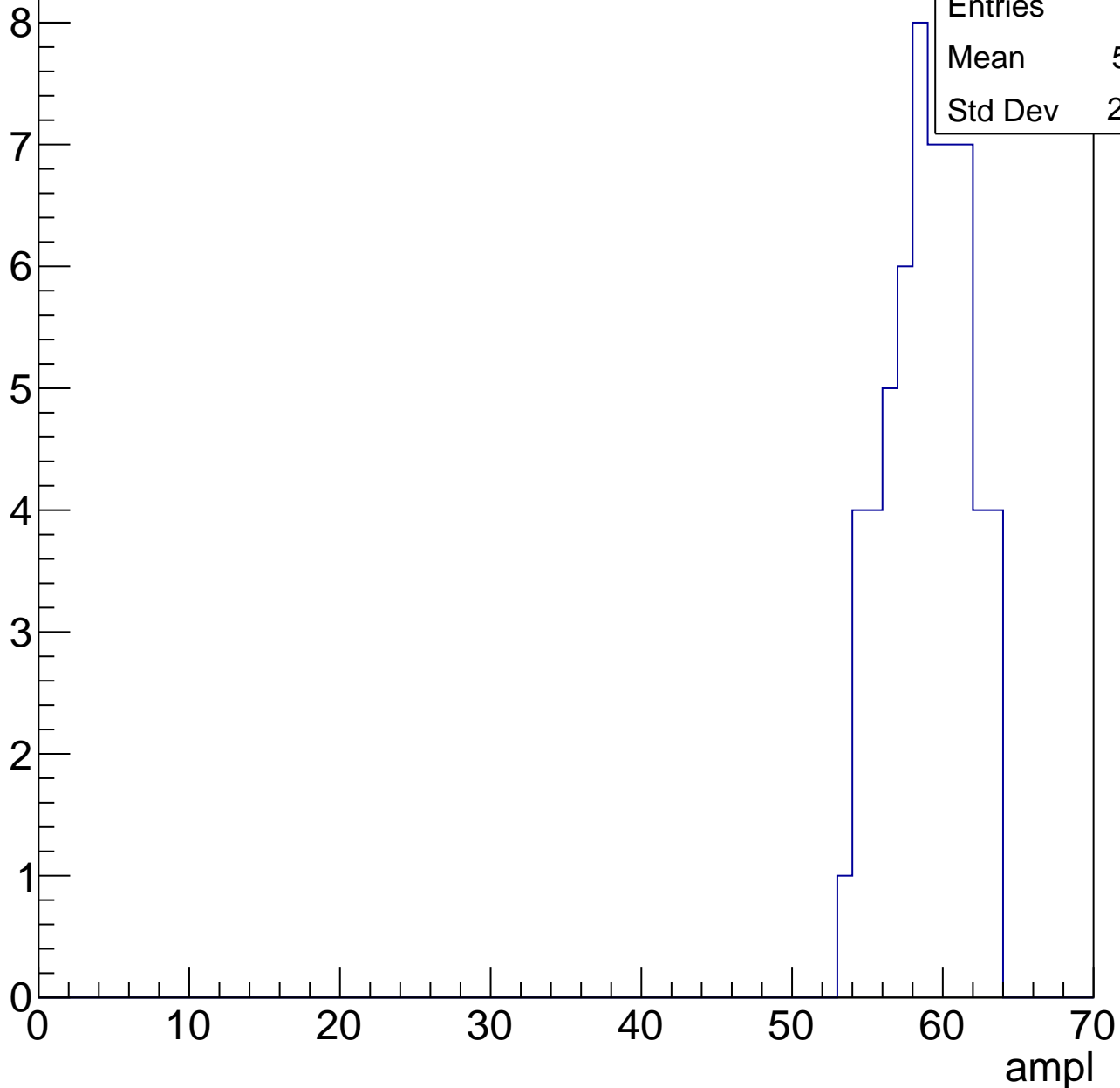
Entry



# B0L001S, U24-ch67, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

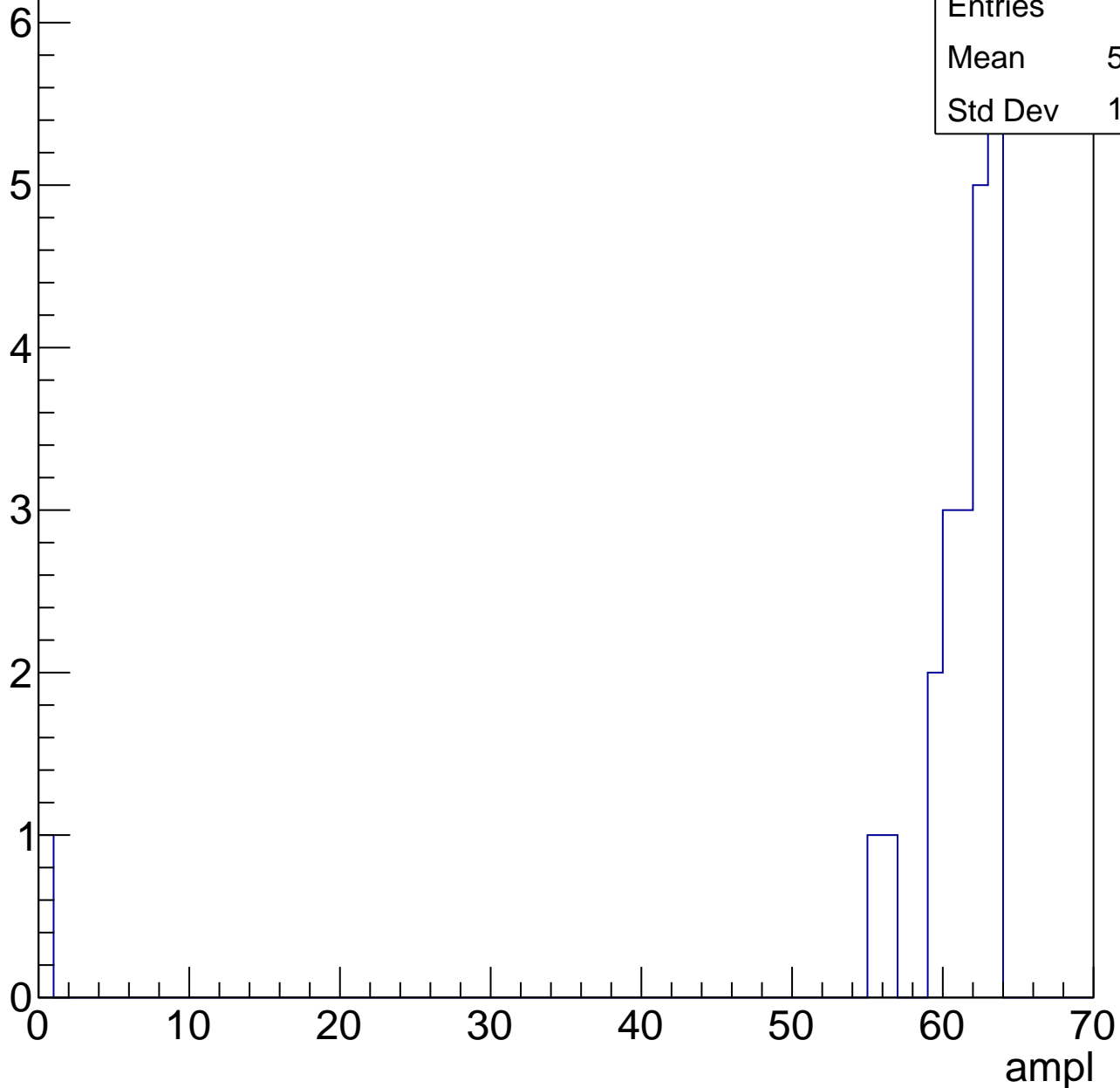


Entries	57
Mean	58.51
Std Dev	2.643

# B0L001S, U24-ch67, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U24-ch67, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	62
Std Dev	0



# B0L001S, U24-ch67, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U24-ch68, adc0

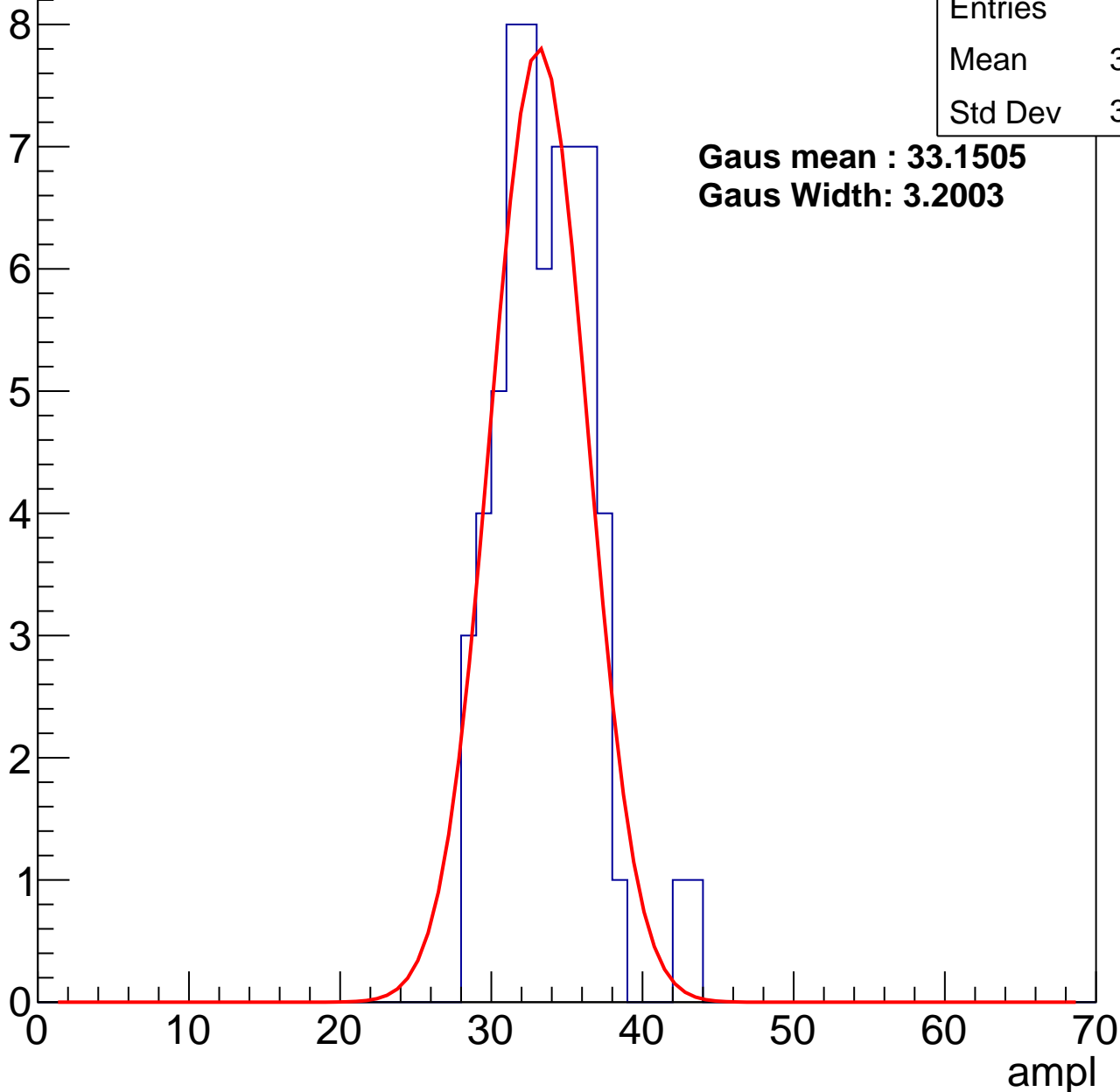
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	33.19
Std Dev	3.084

**Gaus mean : 33.1505**

**Gaus Width: 3.2003**



# B0L001S, U24-ch68, adc1

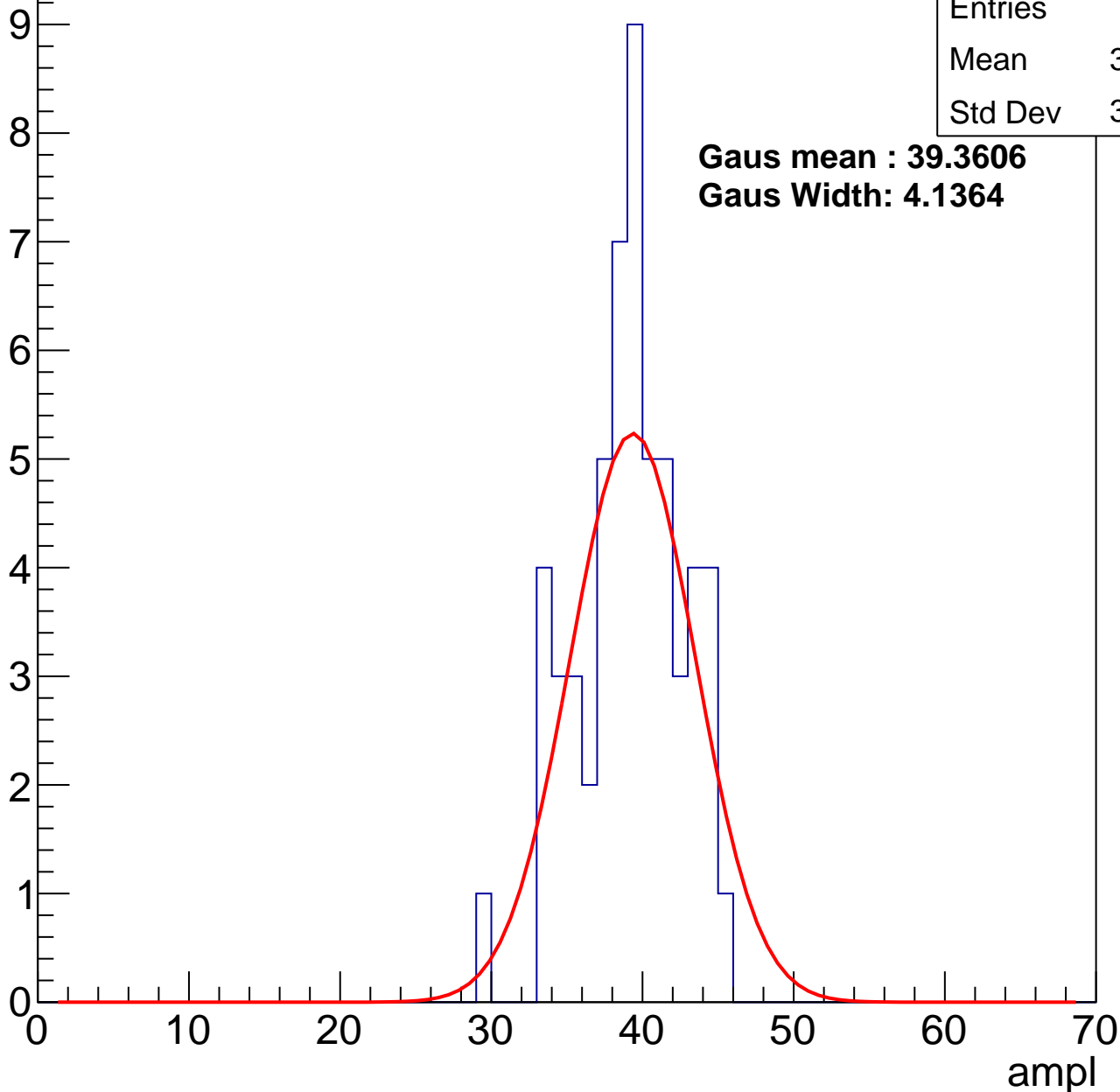
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	38.68
Std Dev	3.428

**Gaus mean : 39.3606**

**Gaus Width: 4.1364**



# B0L001S, U24-ch68, adc2

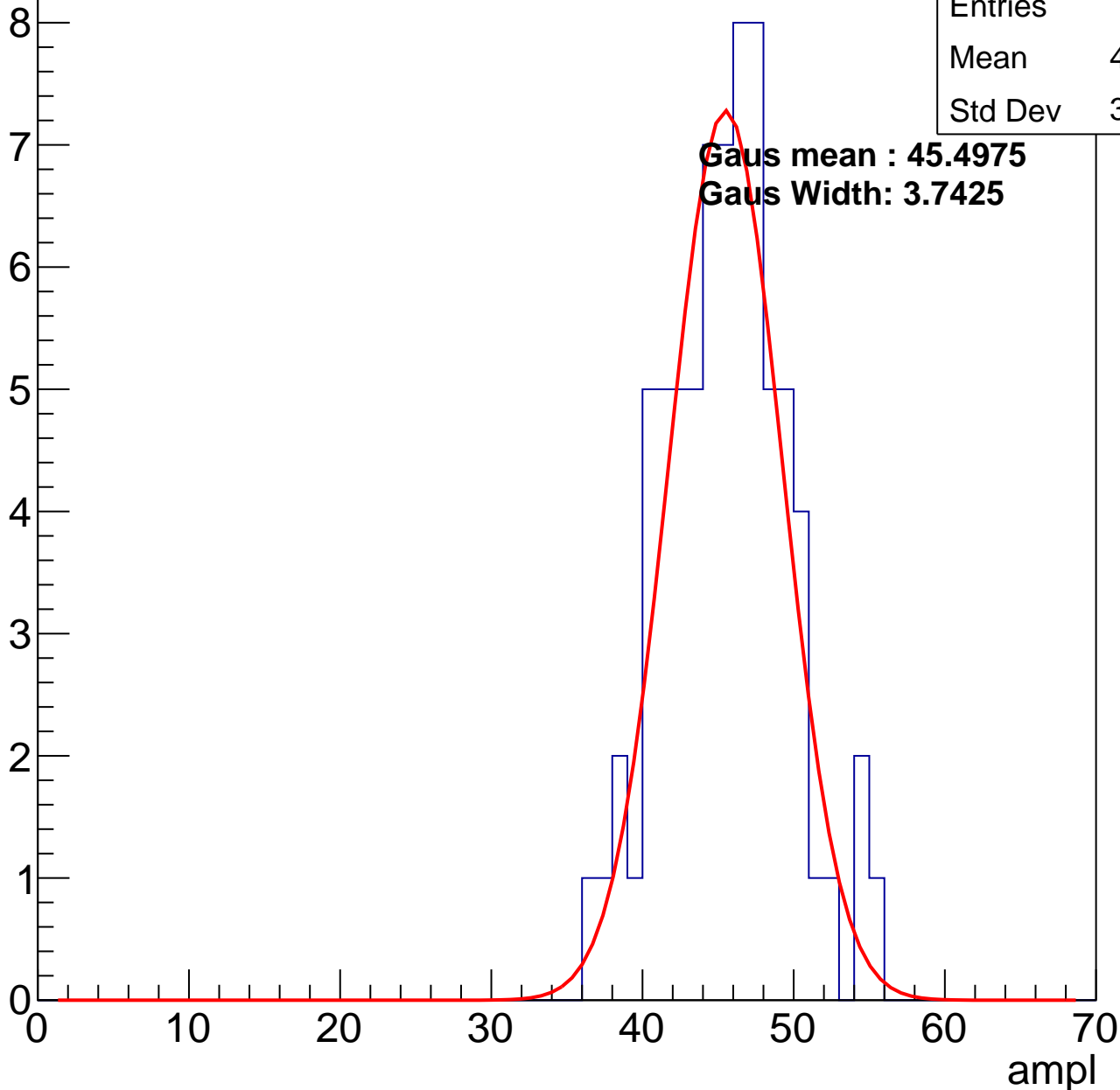
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	45.08
Std Dev	3.972

**Gaus mean : 45.4975**

**Gaus Width: 3.7425**

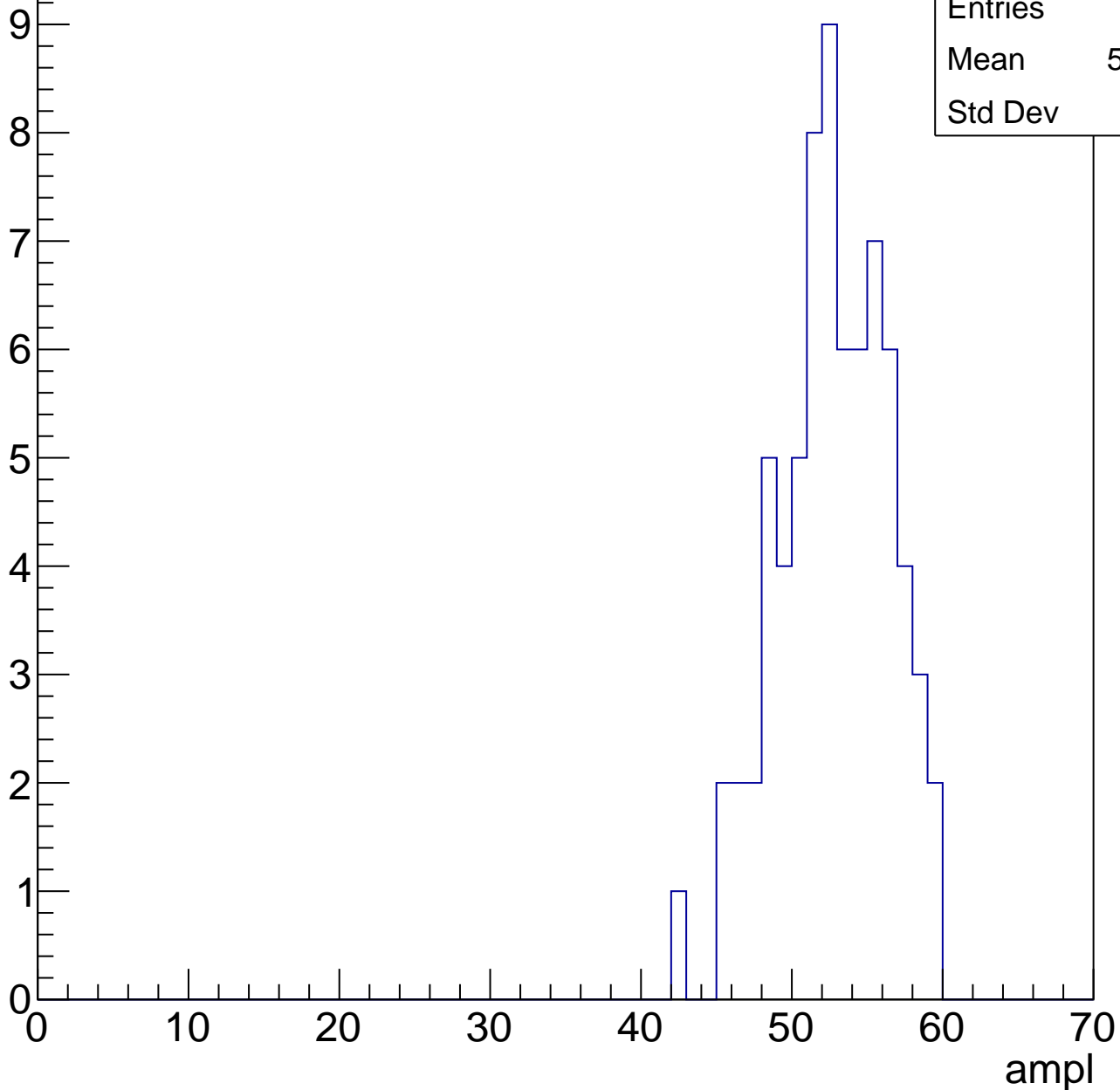


# B0L001S, U24-ch68, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

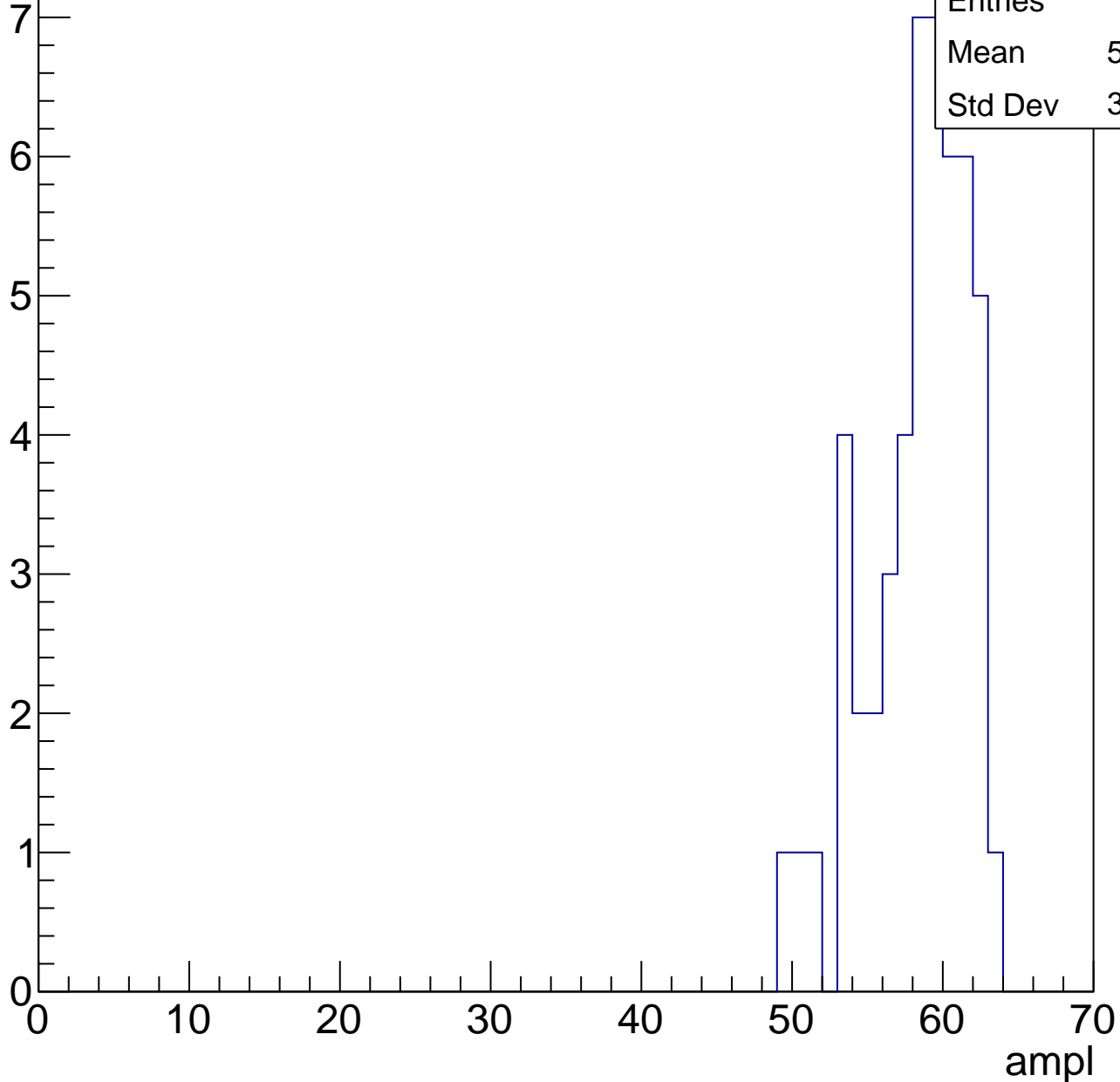
Entries	72
Mean	52.26
Std Dev	3.64



# B0L001S, U24-ch68, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

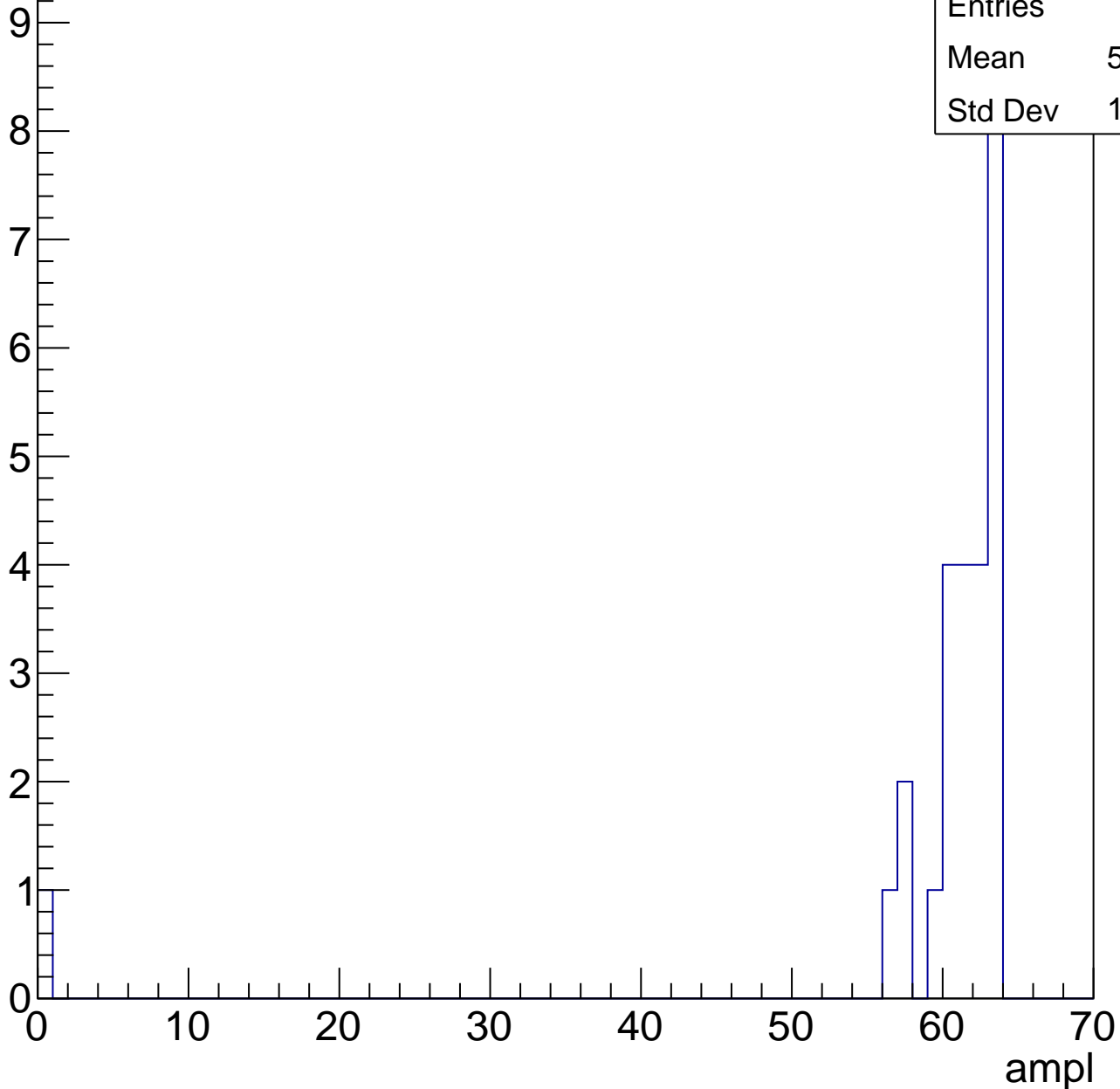


# B0L001S, U24-ch68, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	26
Mean	58.77
Std Dev	11.92



# B0L001S, U24-ch68, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

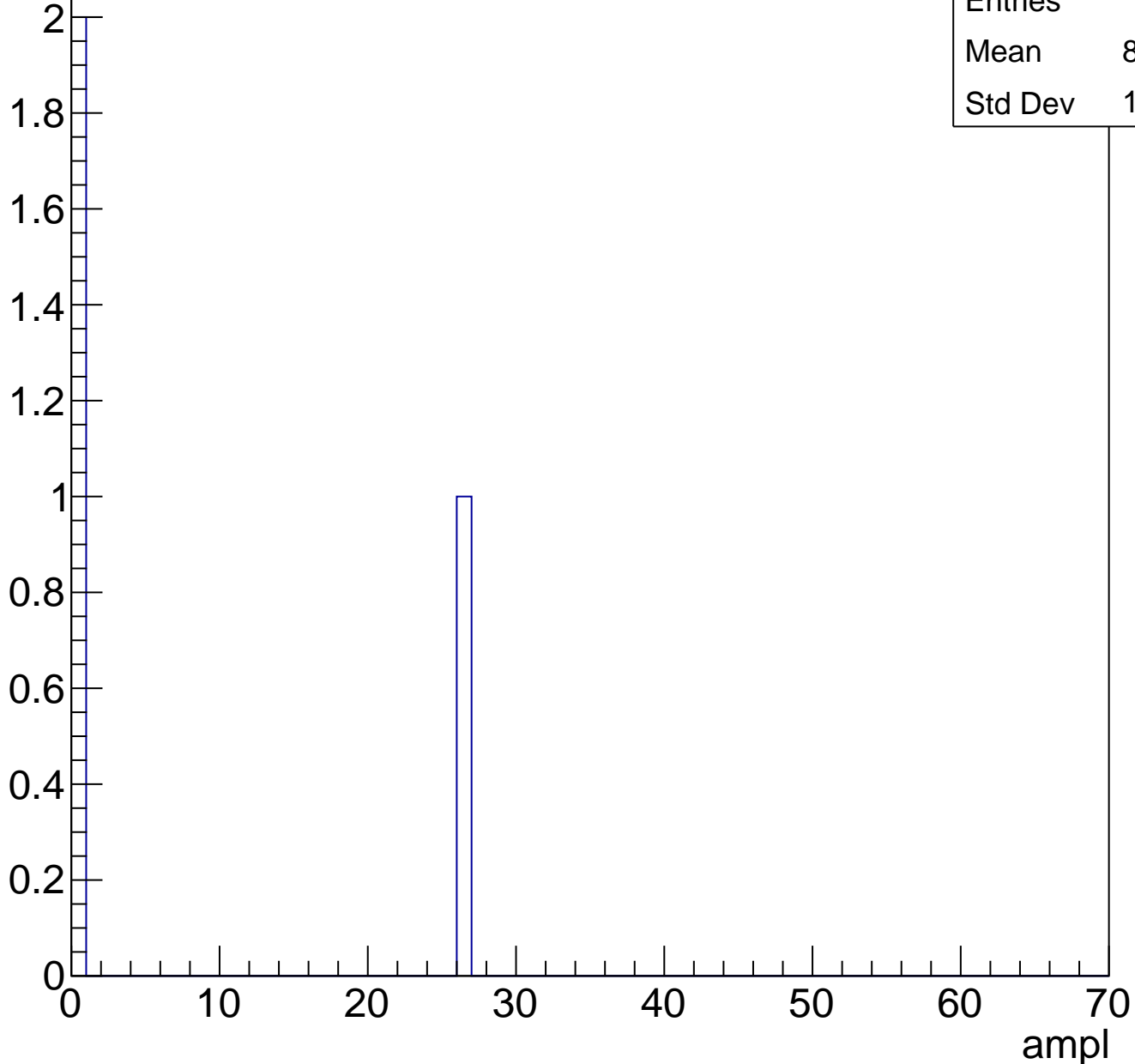




# B0L001S, U24-ch68, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	3
Mean	8.667
Std Dev	12.26

# B0L001S, U24-ch69, adc0

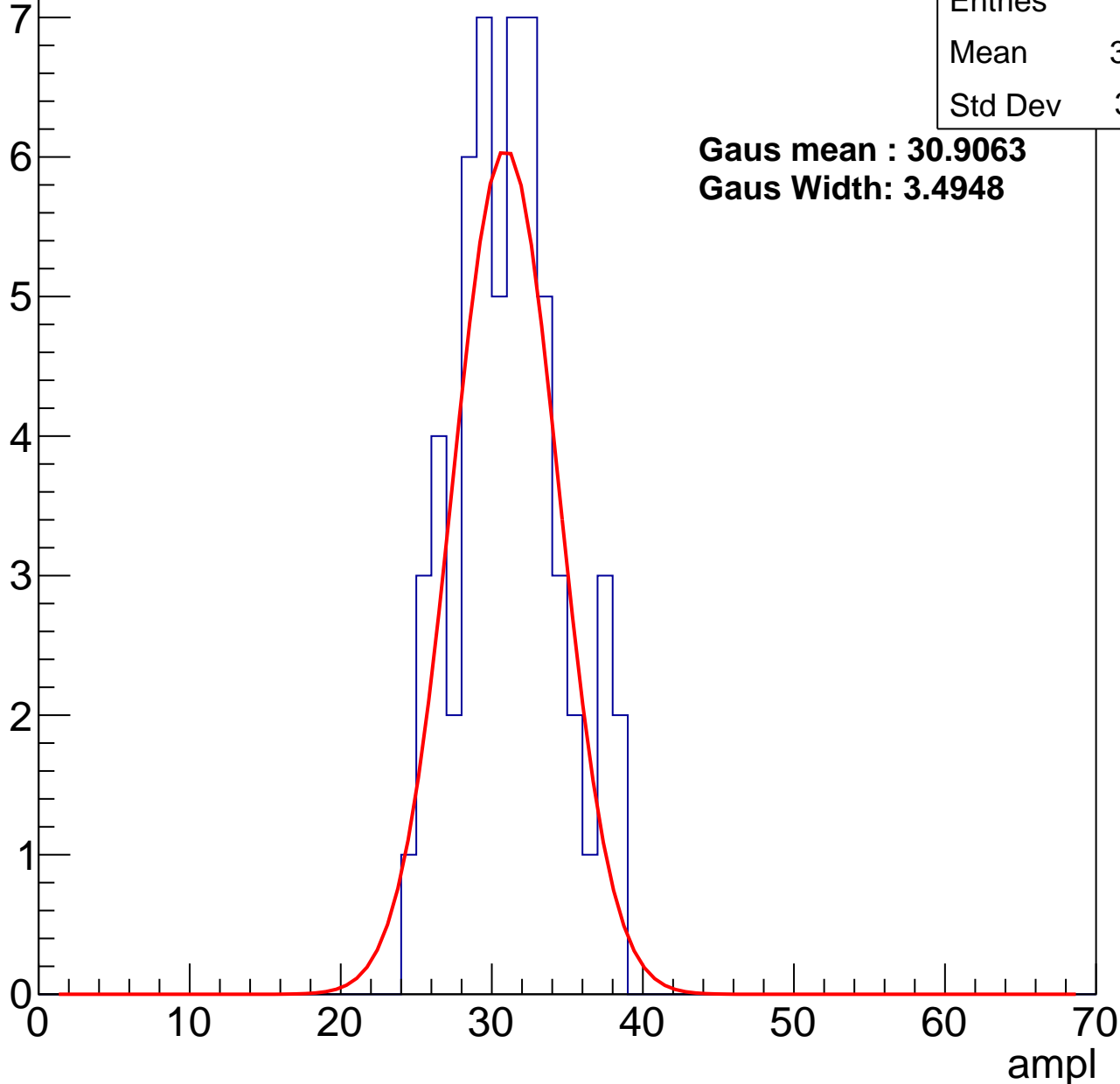
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	30.67
Std Dev	3.441

**Gaus mean : 30.9063**

**Gaus Width: 3.4948**



# B0L001S, U24-ch69, adc1

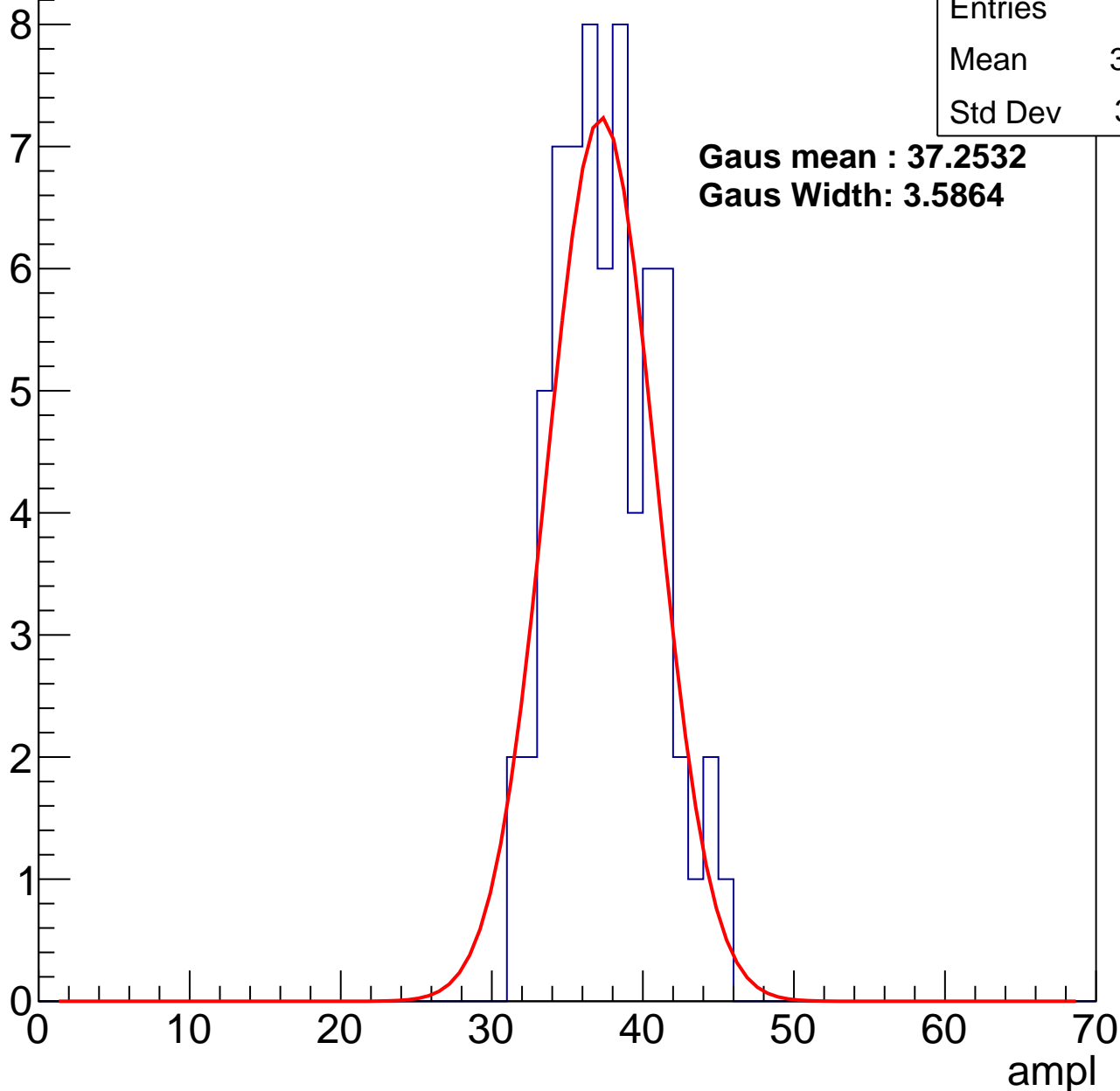
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	37.16
Std Dev	3.281

**Gaus mean : 37.2532**

**Gaus Width: 3.5864**



# B0L001S, U24-ch69, adc2

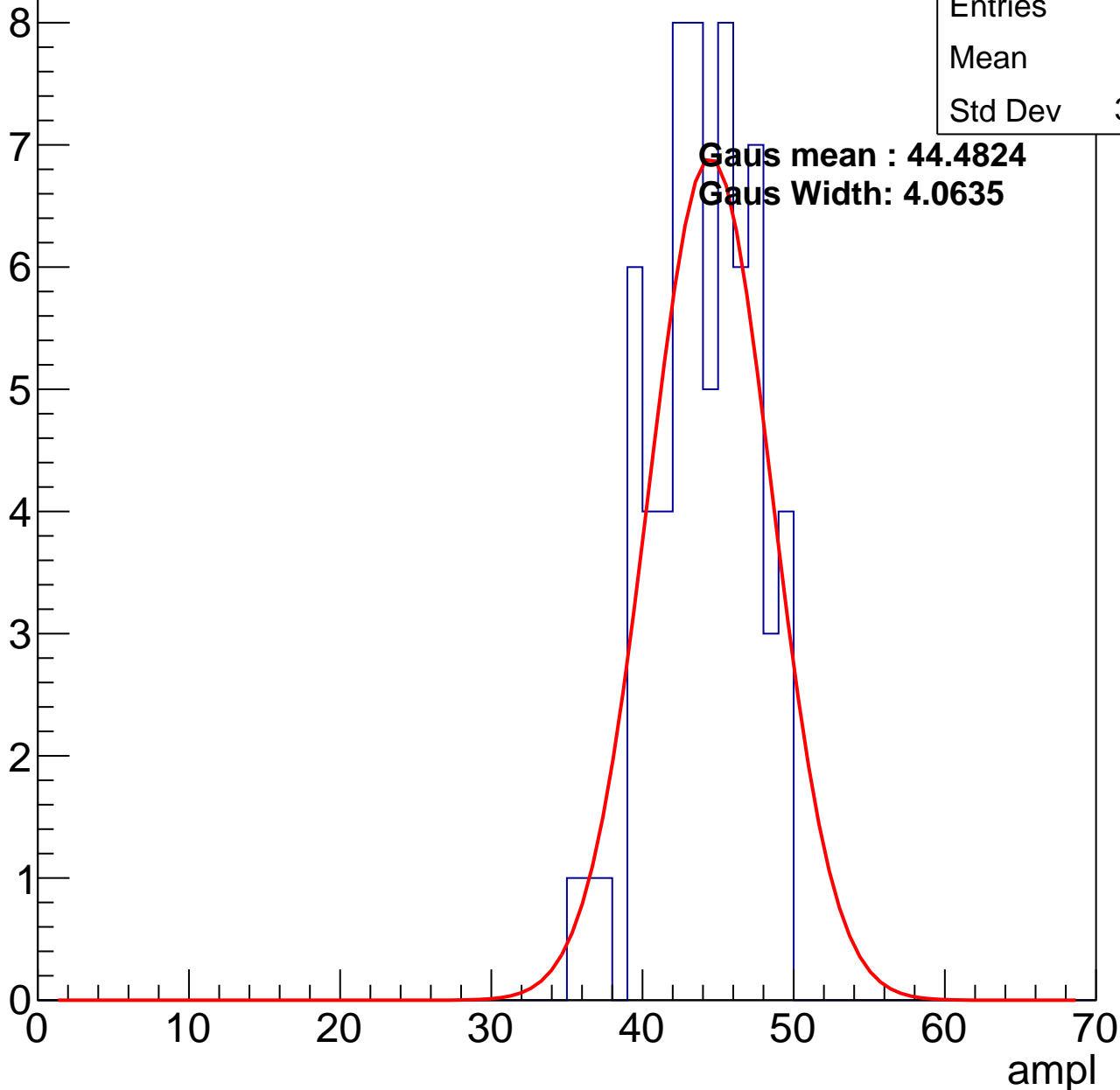
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	43.5
Std Dev	3.281

**Gaus mean : 44.4824**

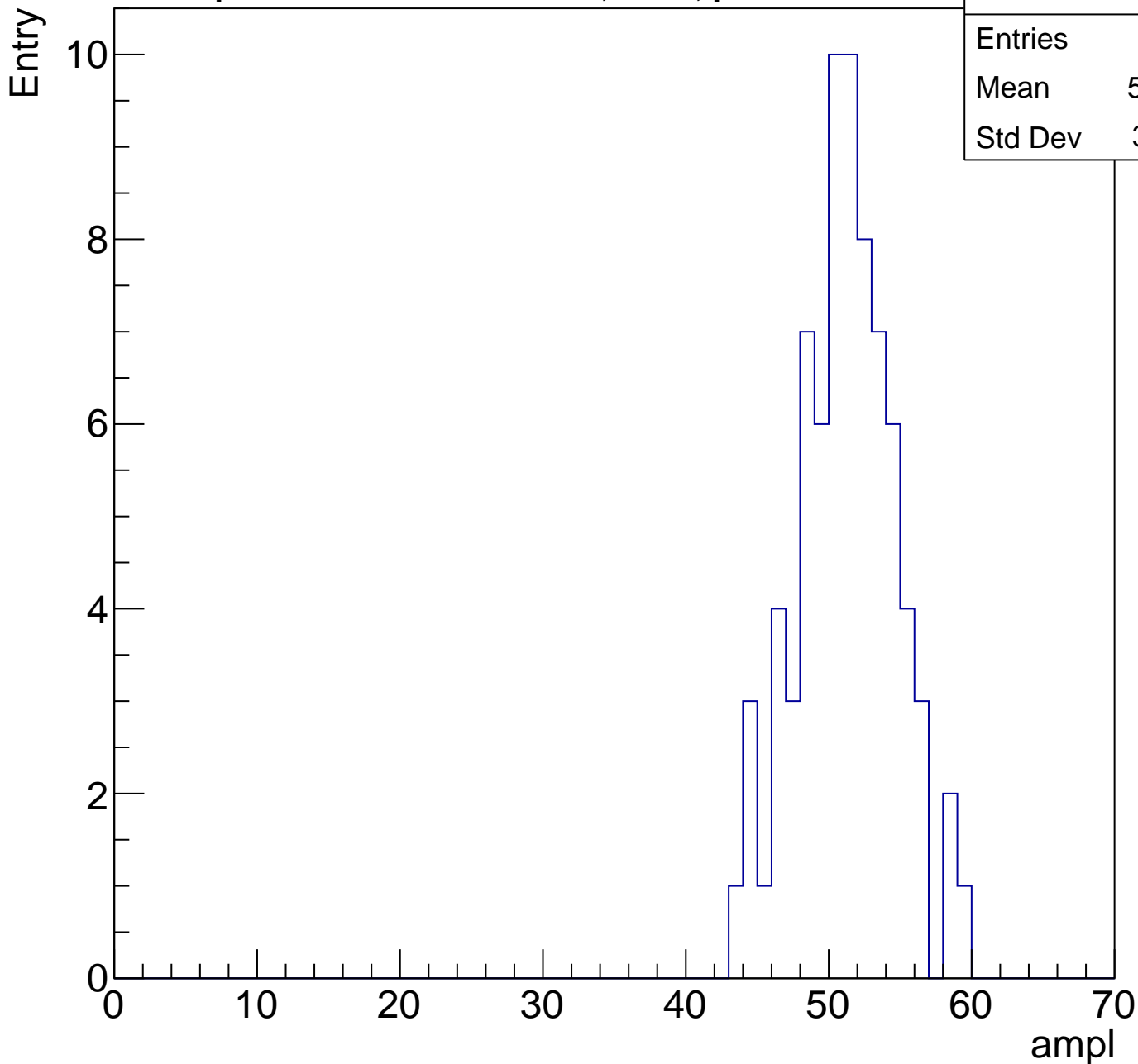
**Gaus Width: 4.0635**



# B0L001S, U24-ch69, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

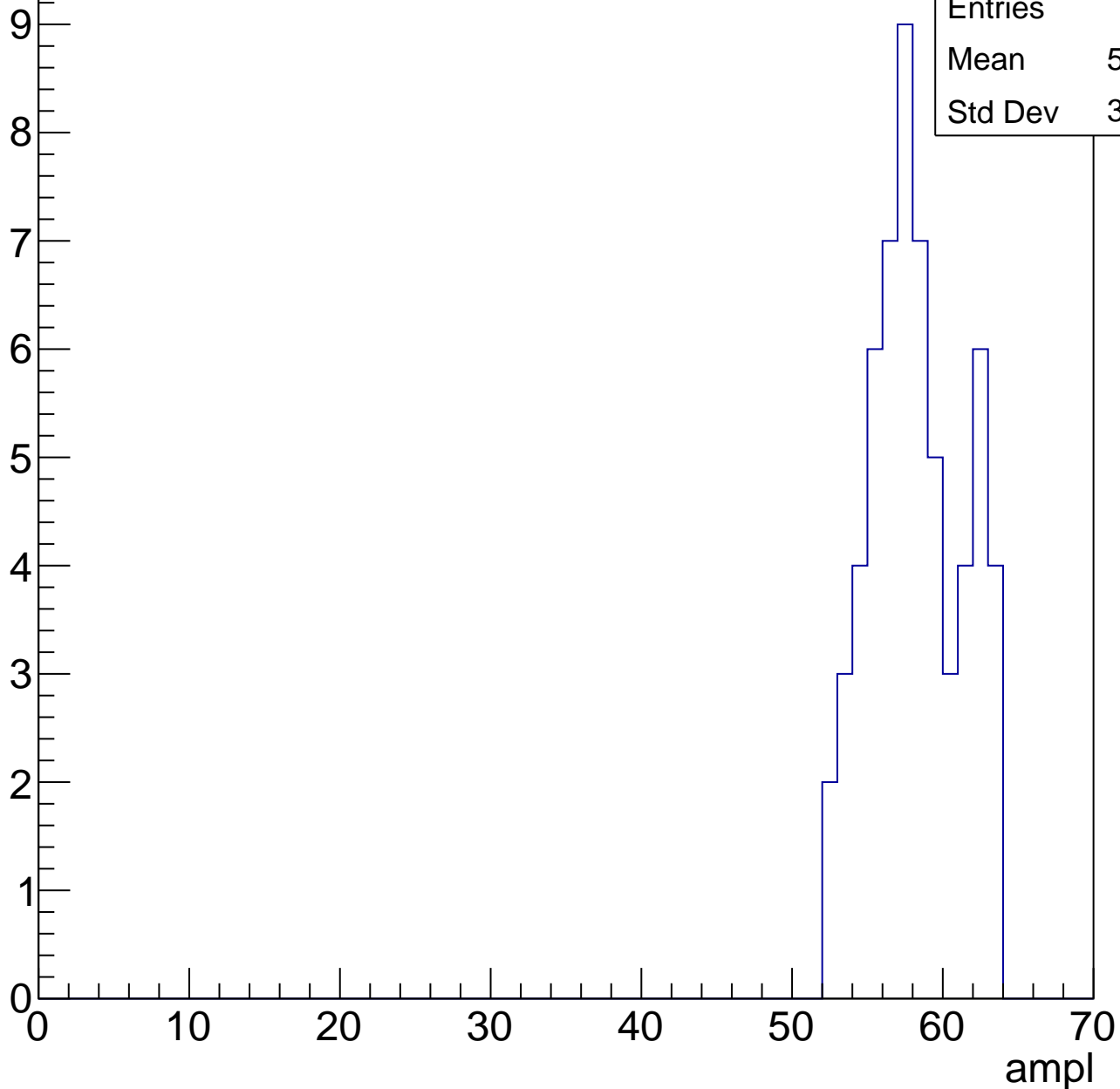
Entries	76
Mean	50.78
Std Dev	3.401



# B0L001S, U24-ch69, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

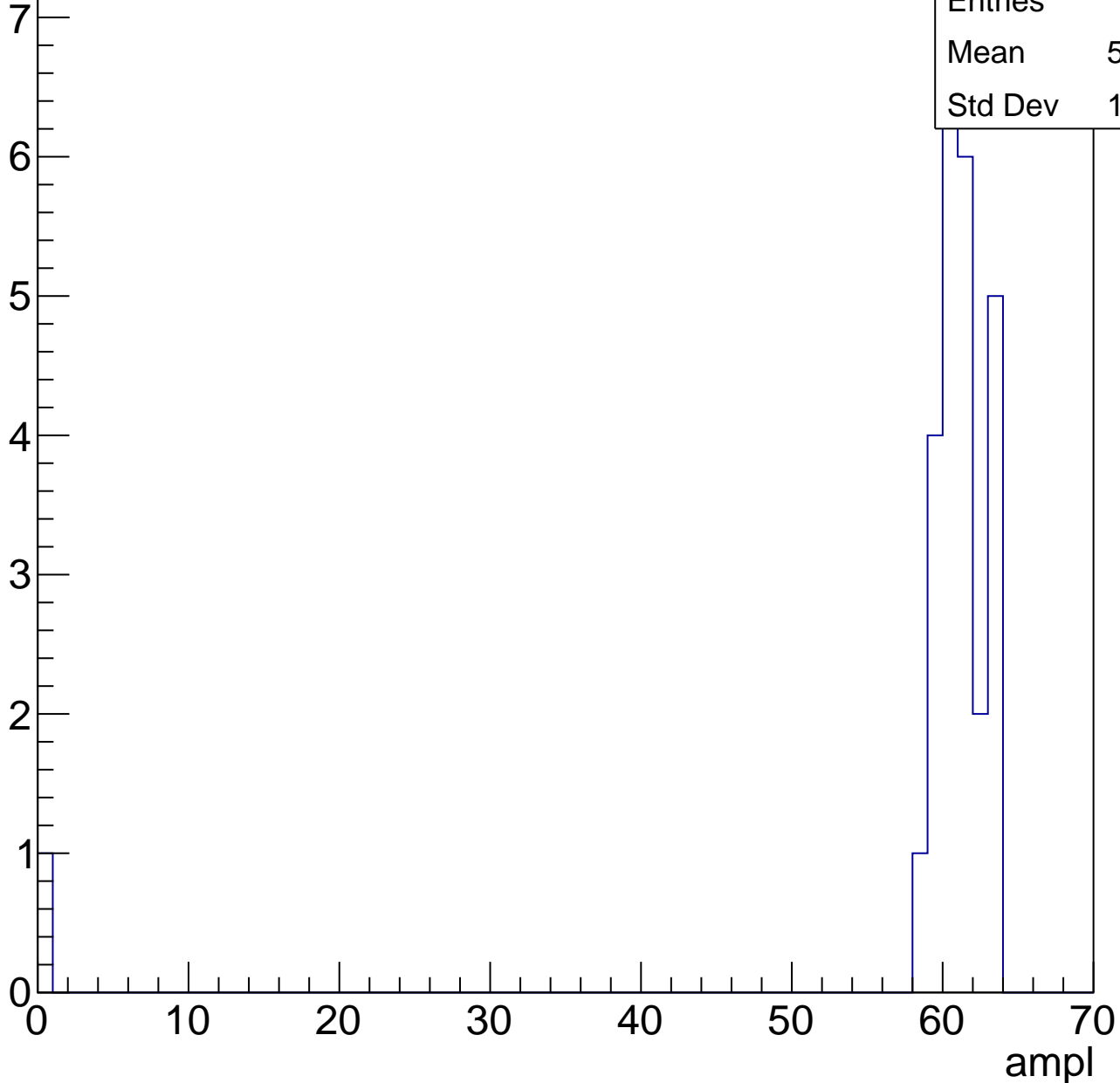


# B0L001S, U24-ch69, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

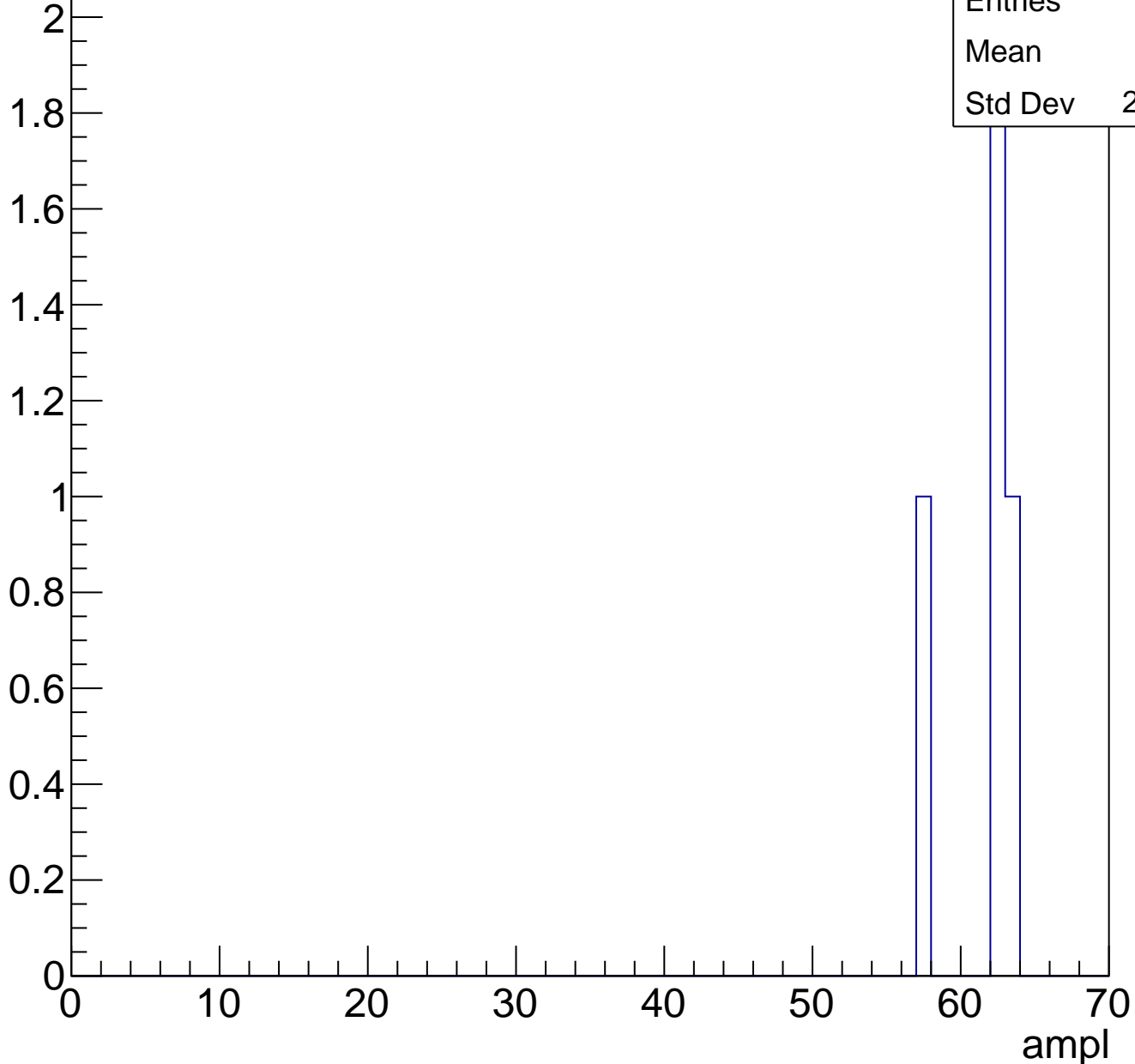
Entries	26
Mean	58.42
Std Dev	11.77



# B0L001S, U24-ch69, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch69, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U24-ch70, adc0

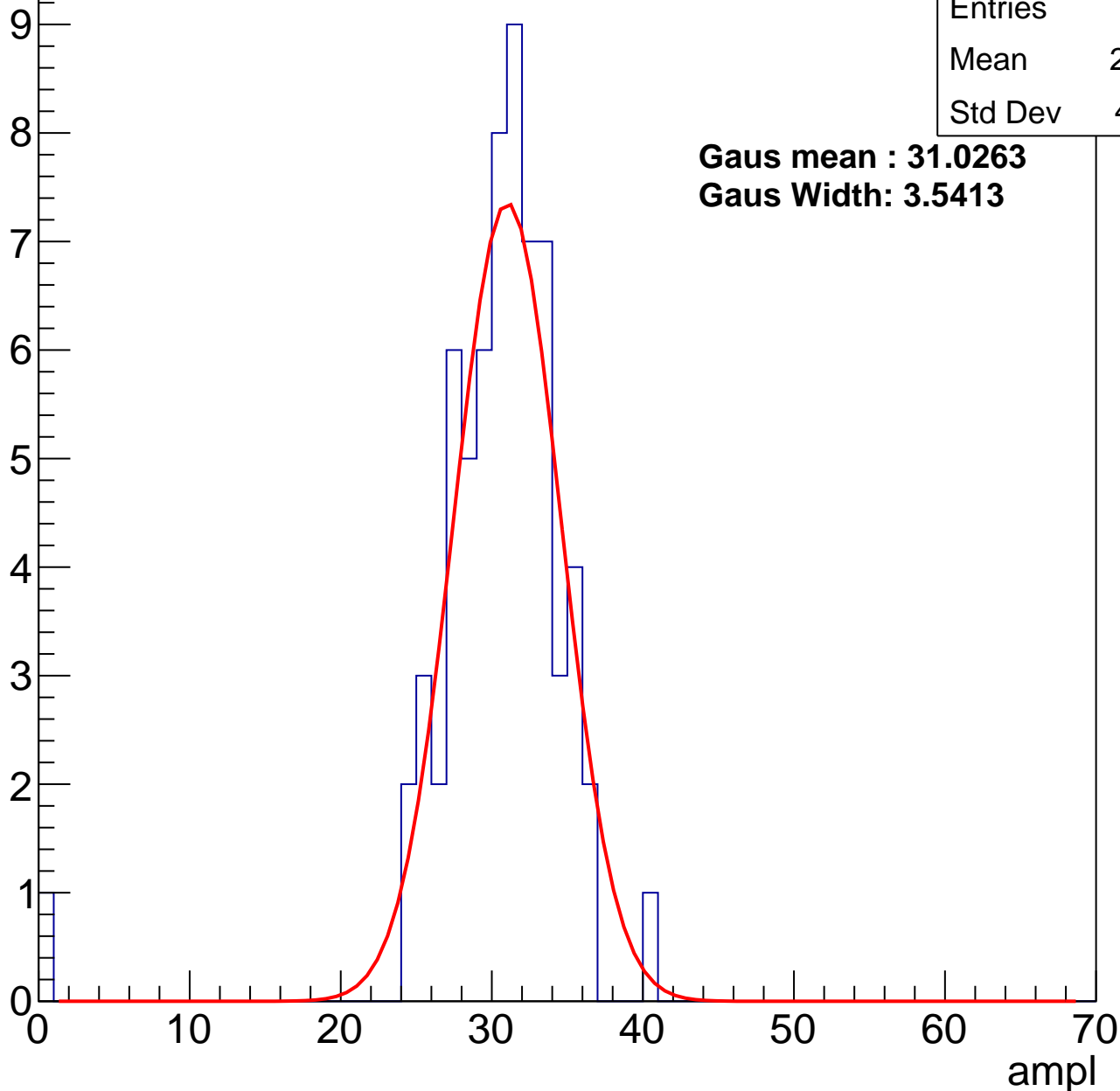
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	29.98
Std Dev	4.891

**Gaus mean : 31.0263**

**Gaus Width: 3.5413**



# B0L001S, U24-ch70, adc1

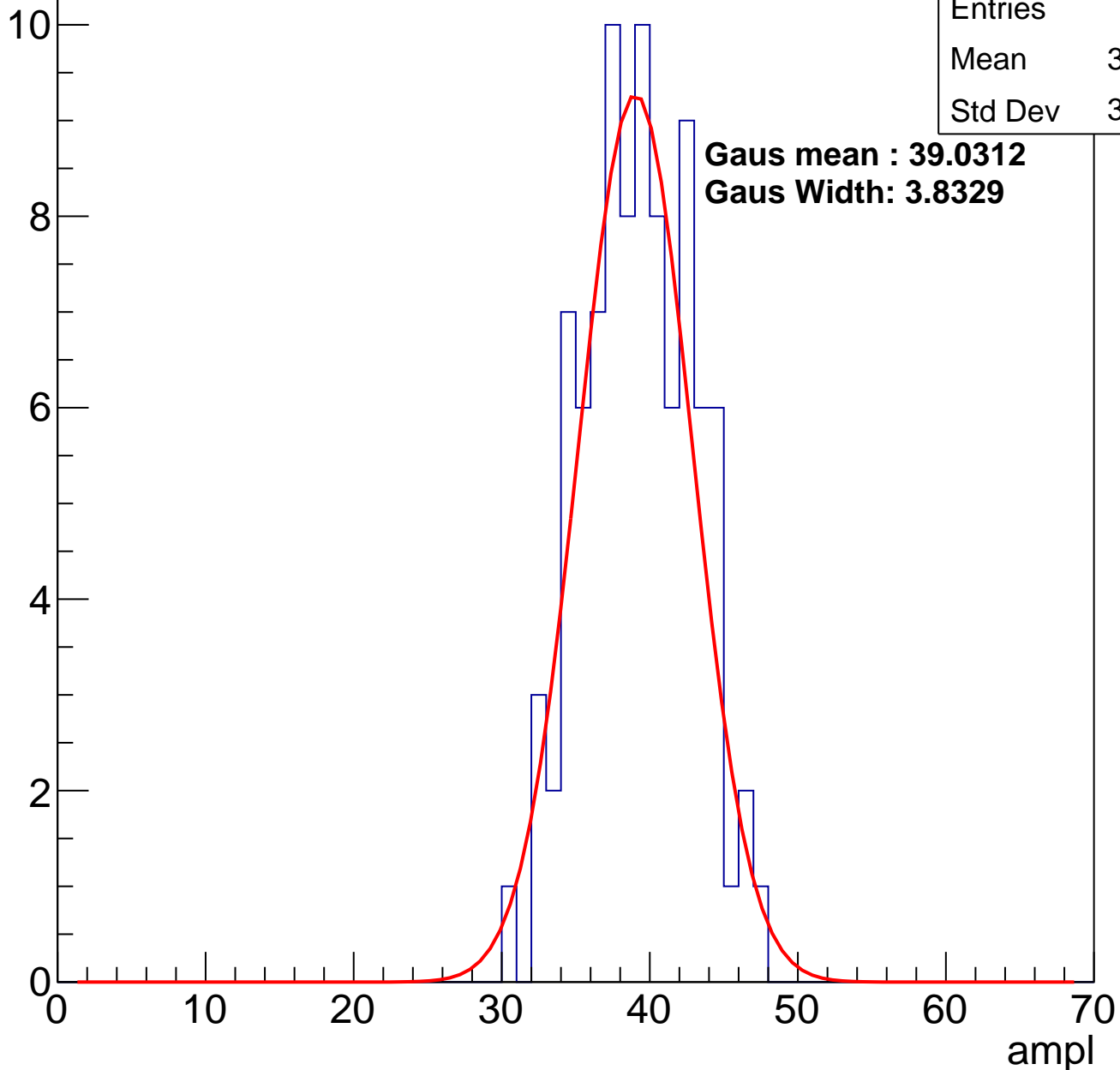
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	93
Mean	38.77
Std Dev	3.643

**Gaus mean : 39.0312**

**Gaus Width: 3.8329**

Entry



# B0L001S, U24-ch70, adc2

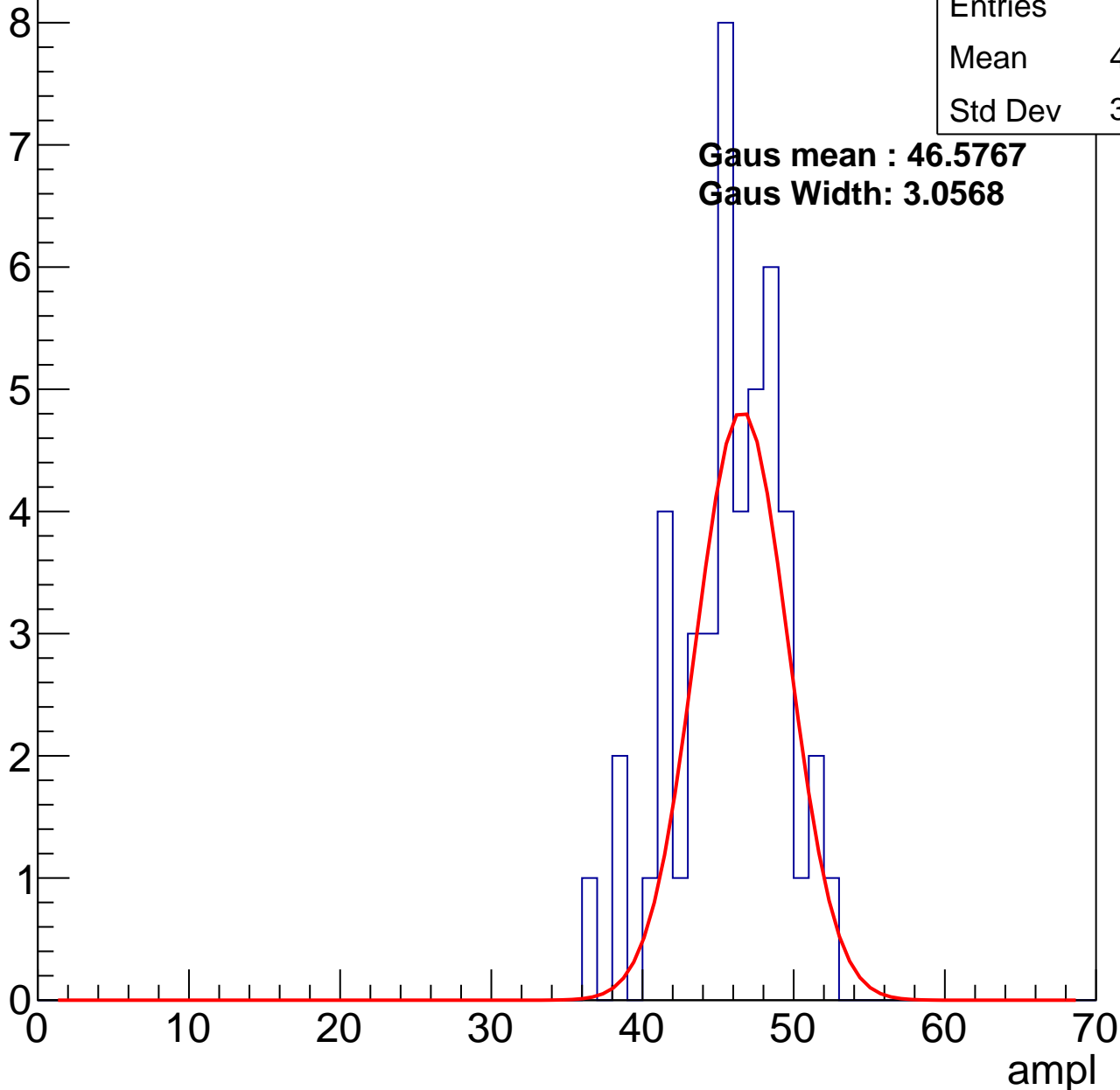
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	46
Mean	45.35
Std Dev	3.534

**Gaus mean : 46.5767**

**Gaus Width: 3.0568**

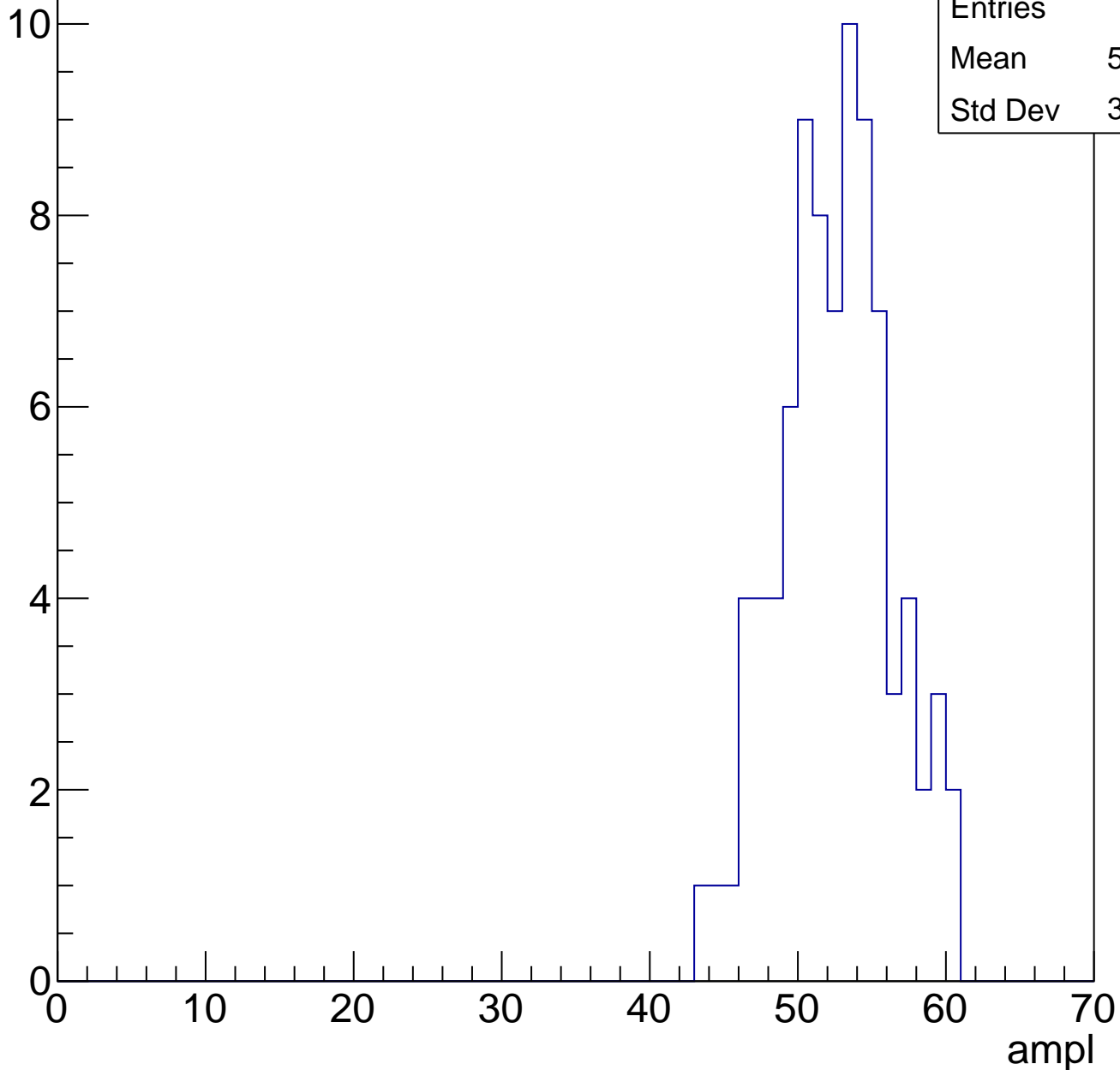


# B0L001S, U24-ch70, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	85
Mean	52.02
Std Dev	3.764

Entry

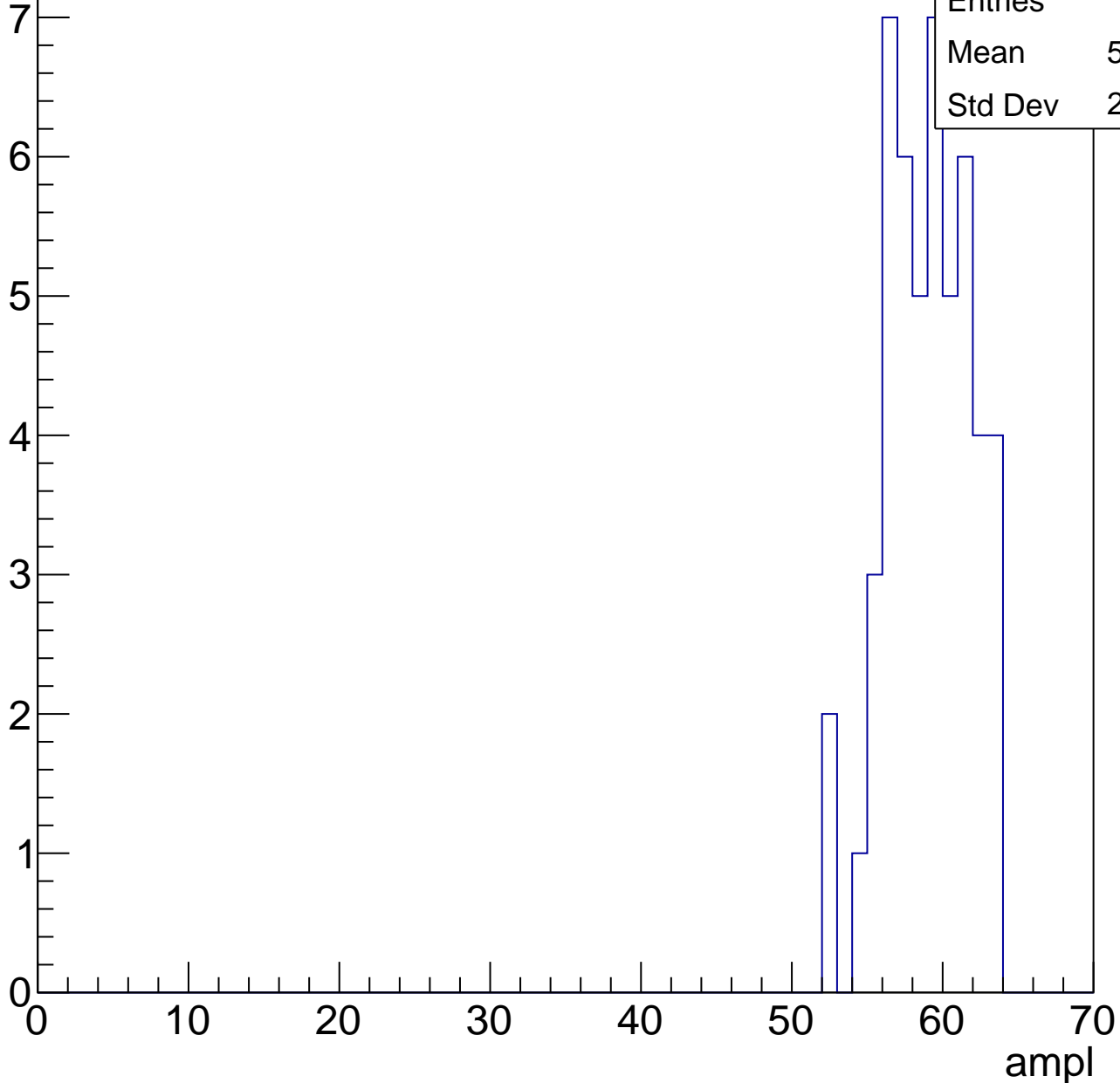


# B0L001S, U24-ch70, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	50
Mean	58.52
Std Dev	2.759

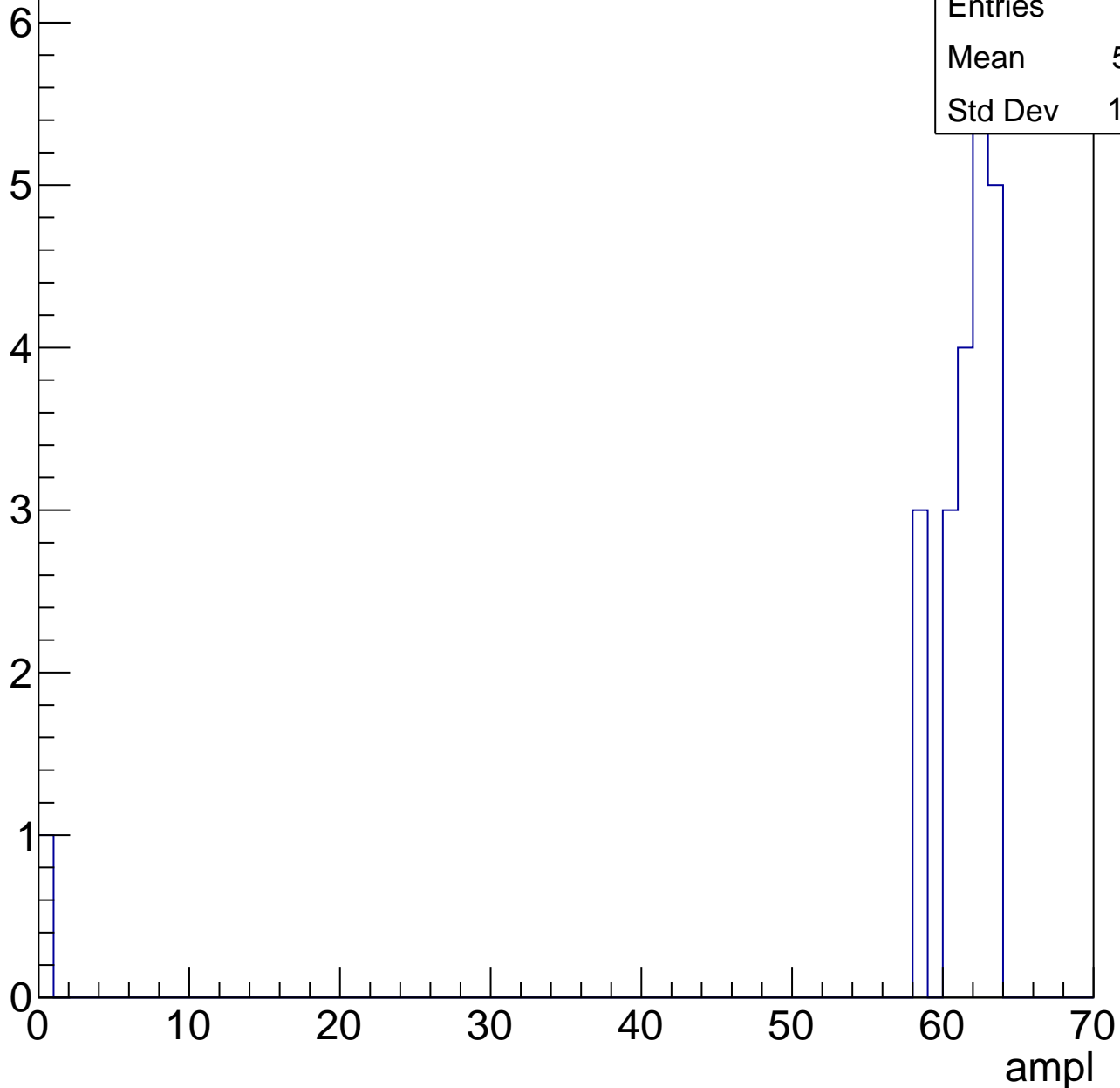


# B0L001S, U24-ch70, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	22
Mean	58.41
Std Dev	12.84



# B0L001S, U24-ch70, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch70, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	3
Mean	0
Std Dev	0

# B0L001S, U24-ch71, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	84
Mean	30.69
Std Dev	5.012

**Gaus mean : 31.3921**

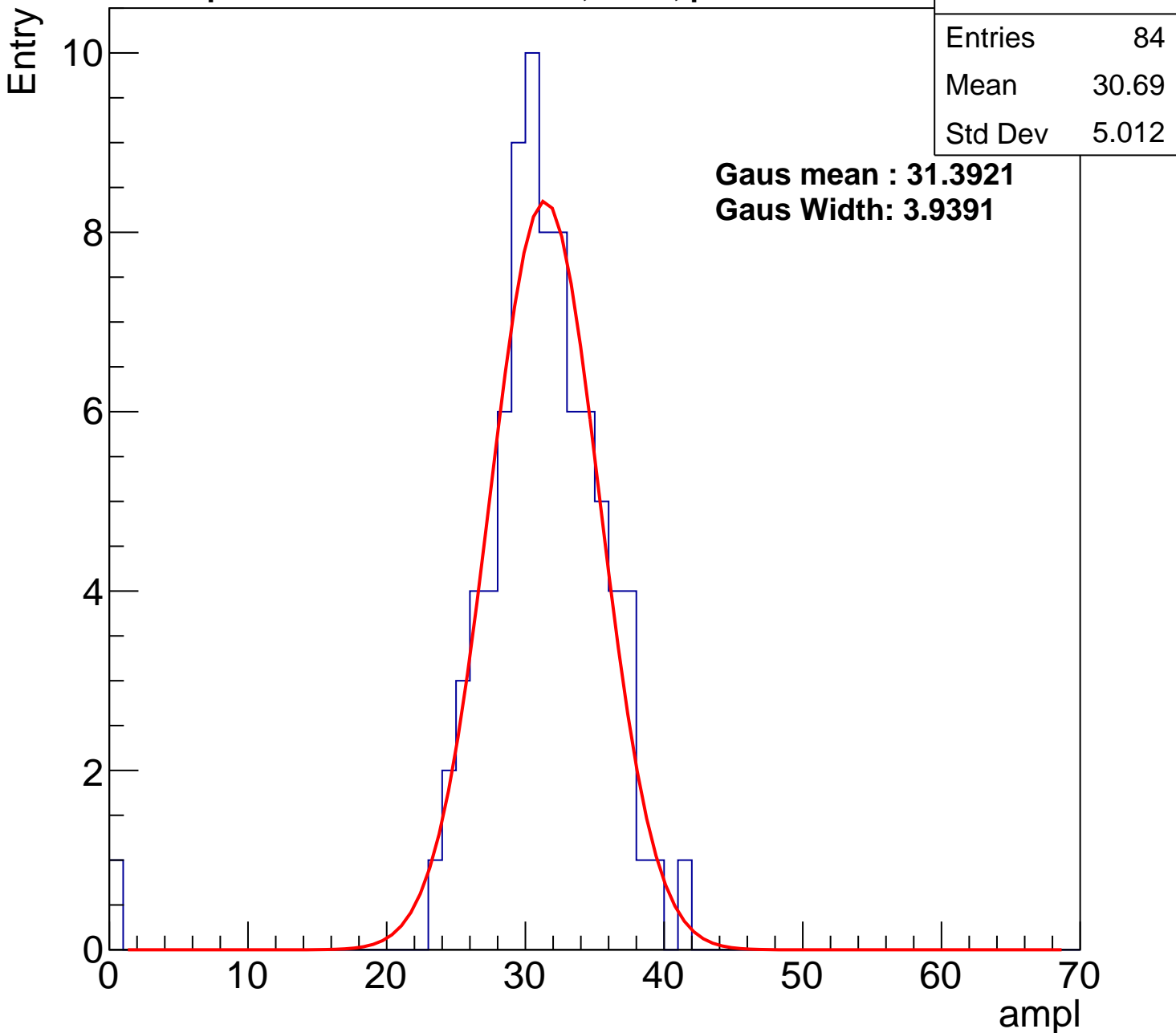
**Gaus Width: 3.9391**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U24-ch71, adc1

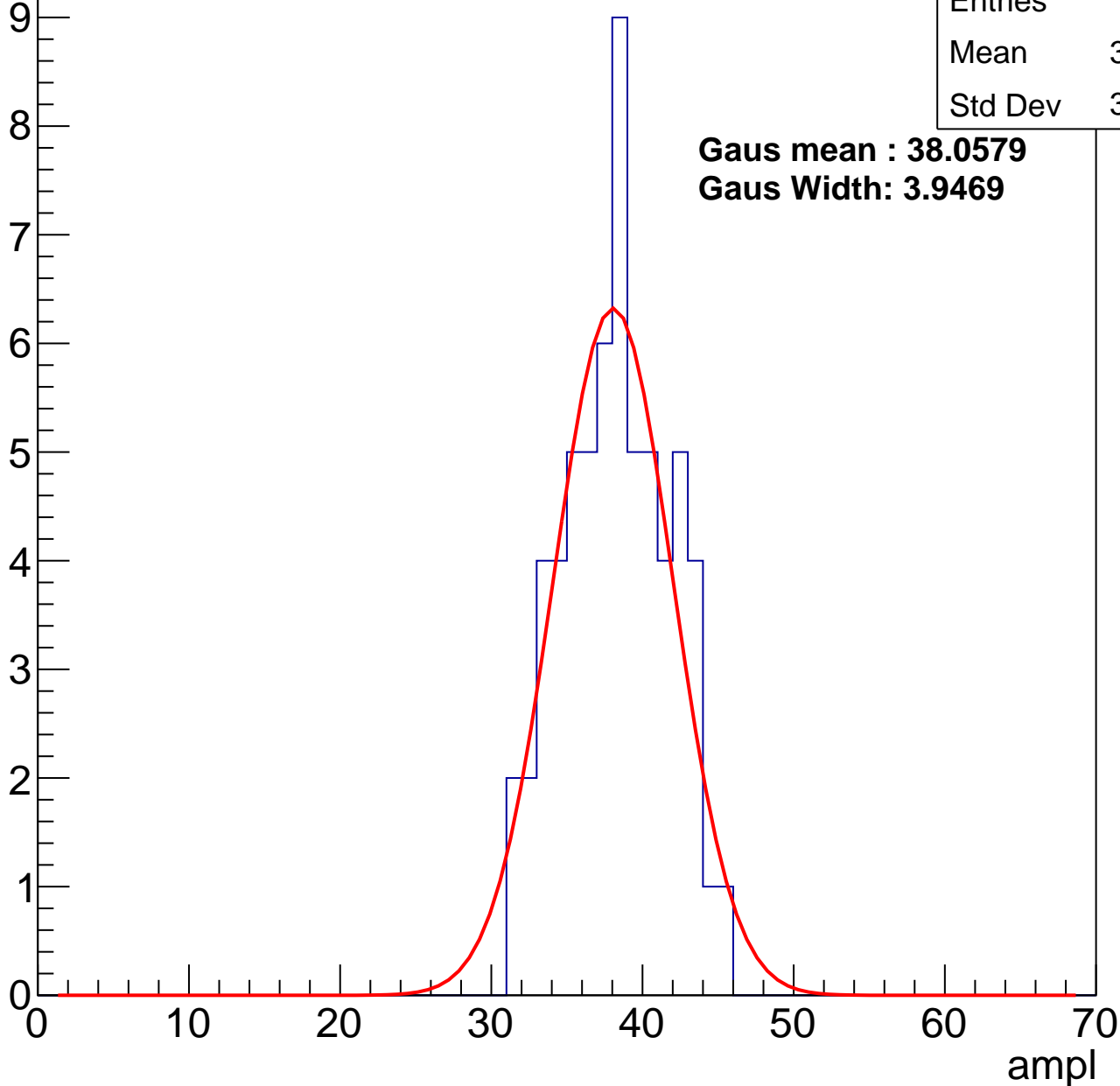
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	37.79
Std Dev	3.427

**Gaus mean : 38.0579**

**Gaus Width: 3.9469**



# B0L001S, U24-ch71, adc2

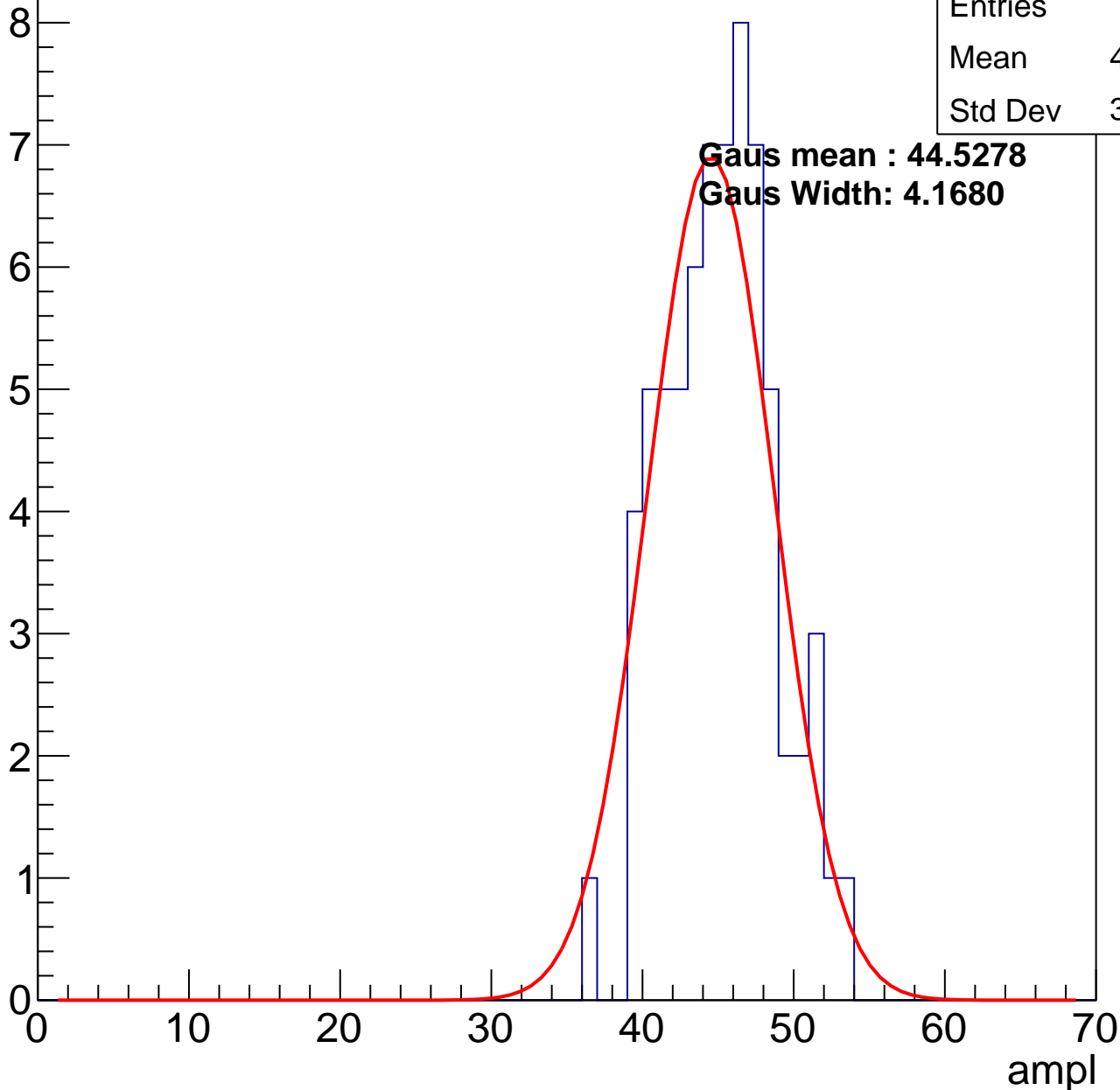
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	44.65
Std Dev	3.575

**Gaus mean : 44.5278**

**Gaus Width: 4.1680**

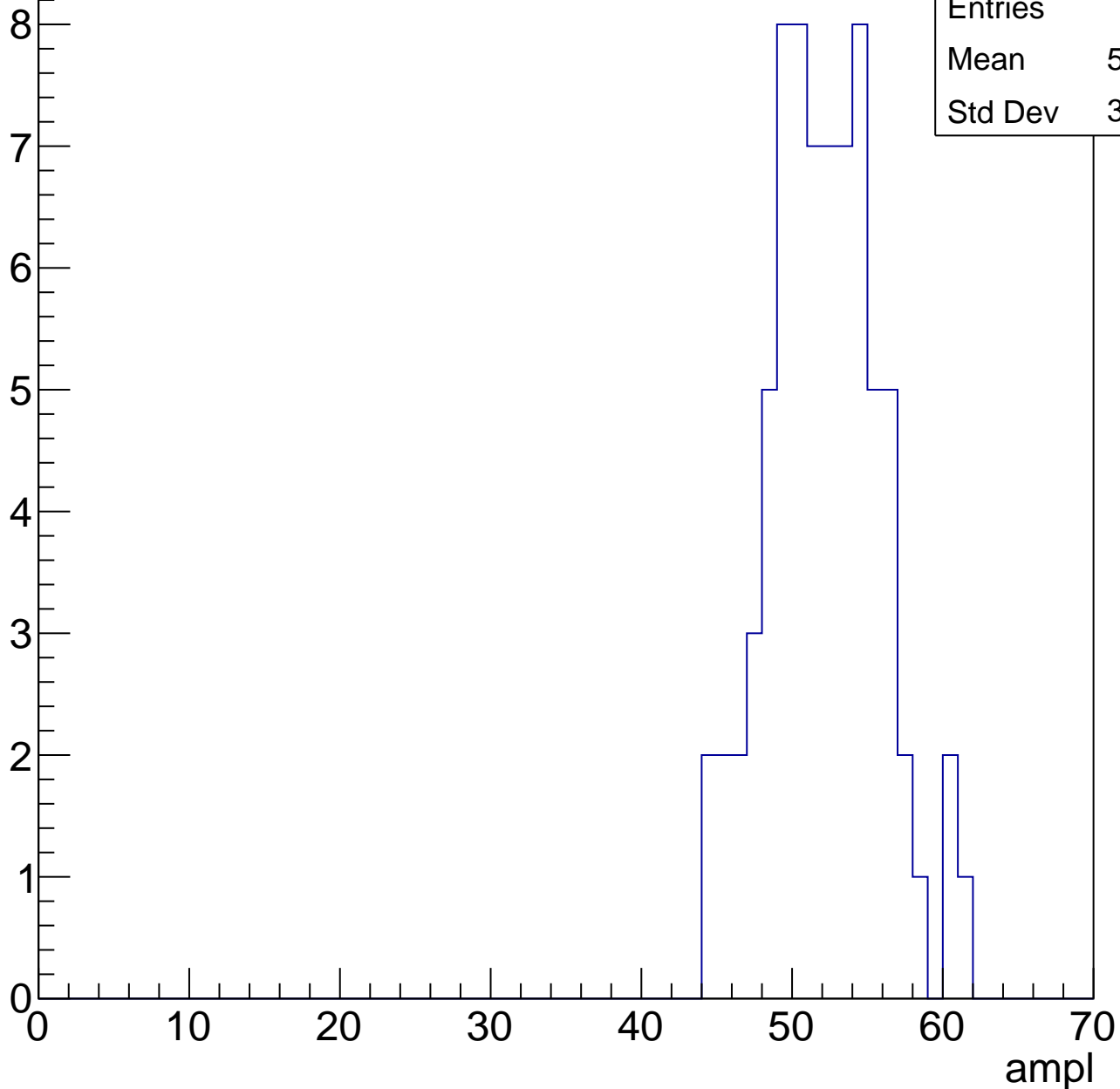


# B0L001S, U24-ch71, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	75
Mean	51.67
Std Dev	3.678

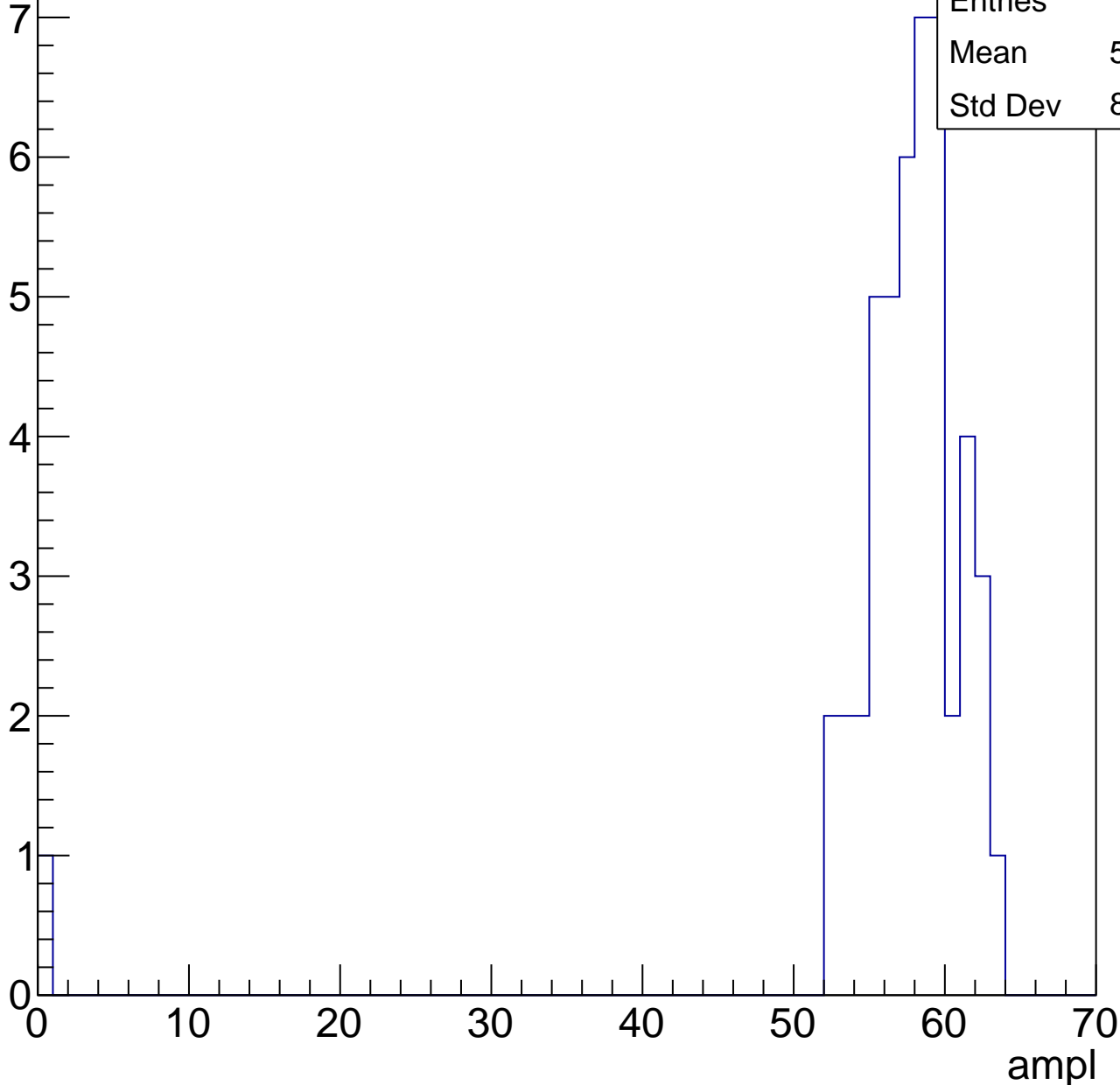


# B0L001S, U24-ch71, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	47
Mean	56.32
Std Dev	8.728

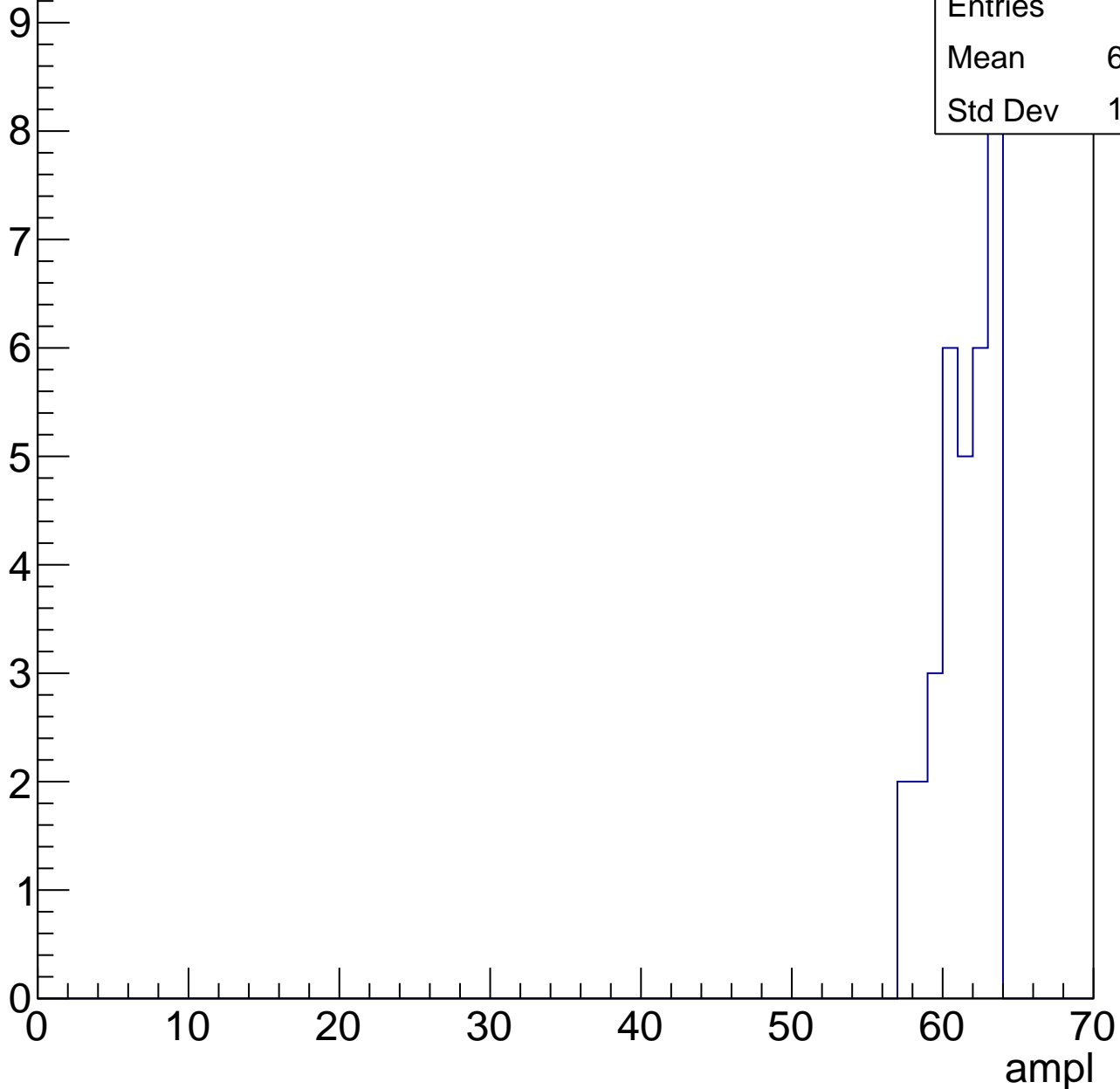


# B0L001S, U24-ch71, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	33
Mean	60.94
Std Dev	1.825



# B0L001S, U24-ch71, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch71, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	3
Mean	7.667
Std Dev	10.84

# B0L001S, U24-ch72, adc0

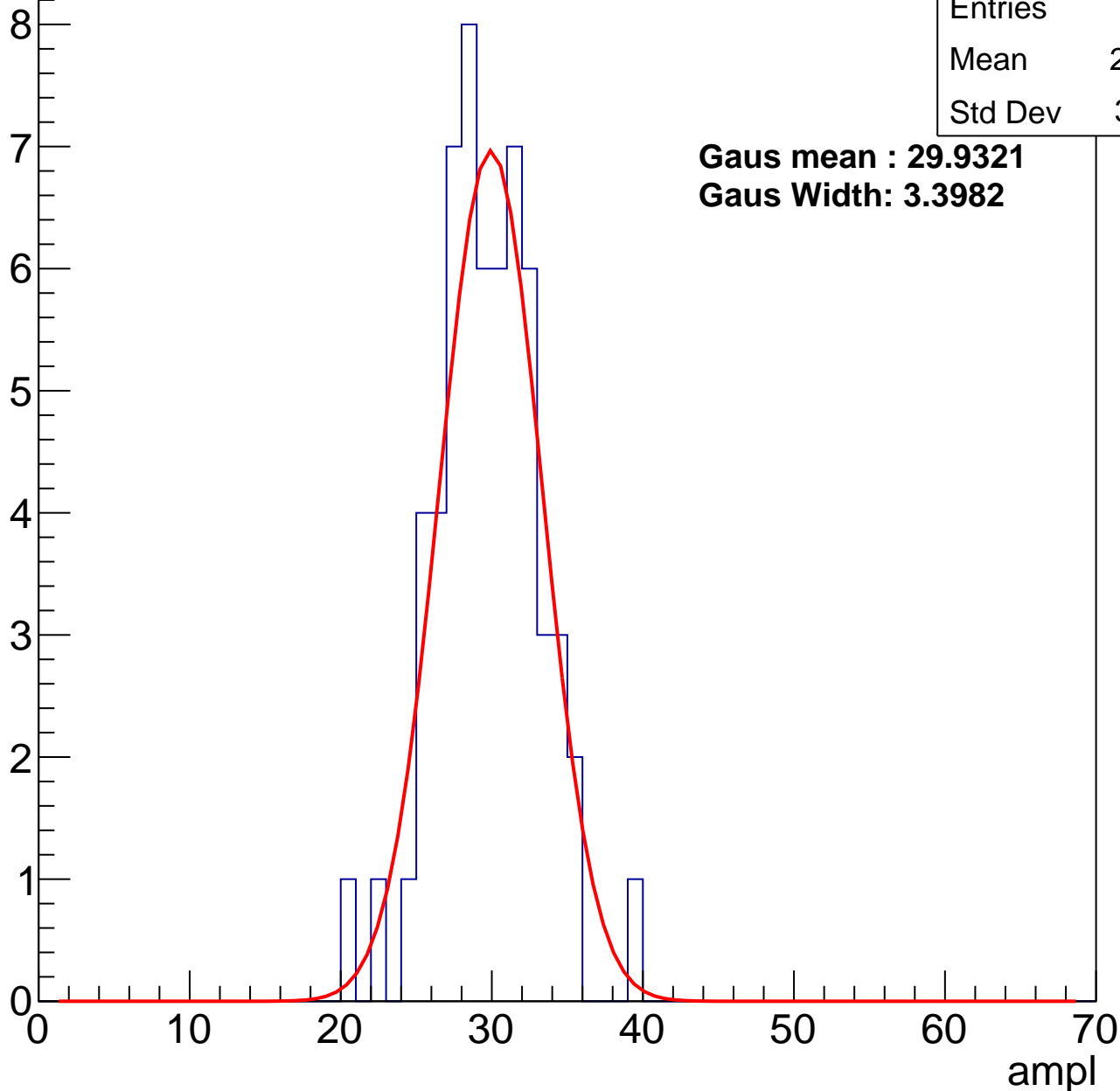
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	29.27
Std Dev	3.341

**Gaus mean : 29.9321**

**Gaus Width: 3.3982**



# B0L001S, U24-ch72, adc1

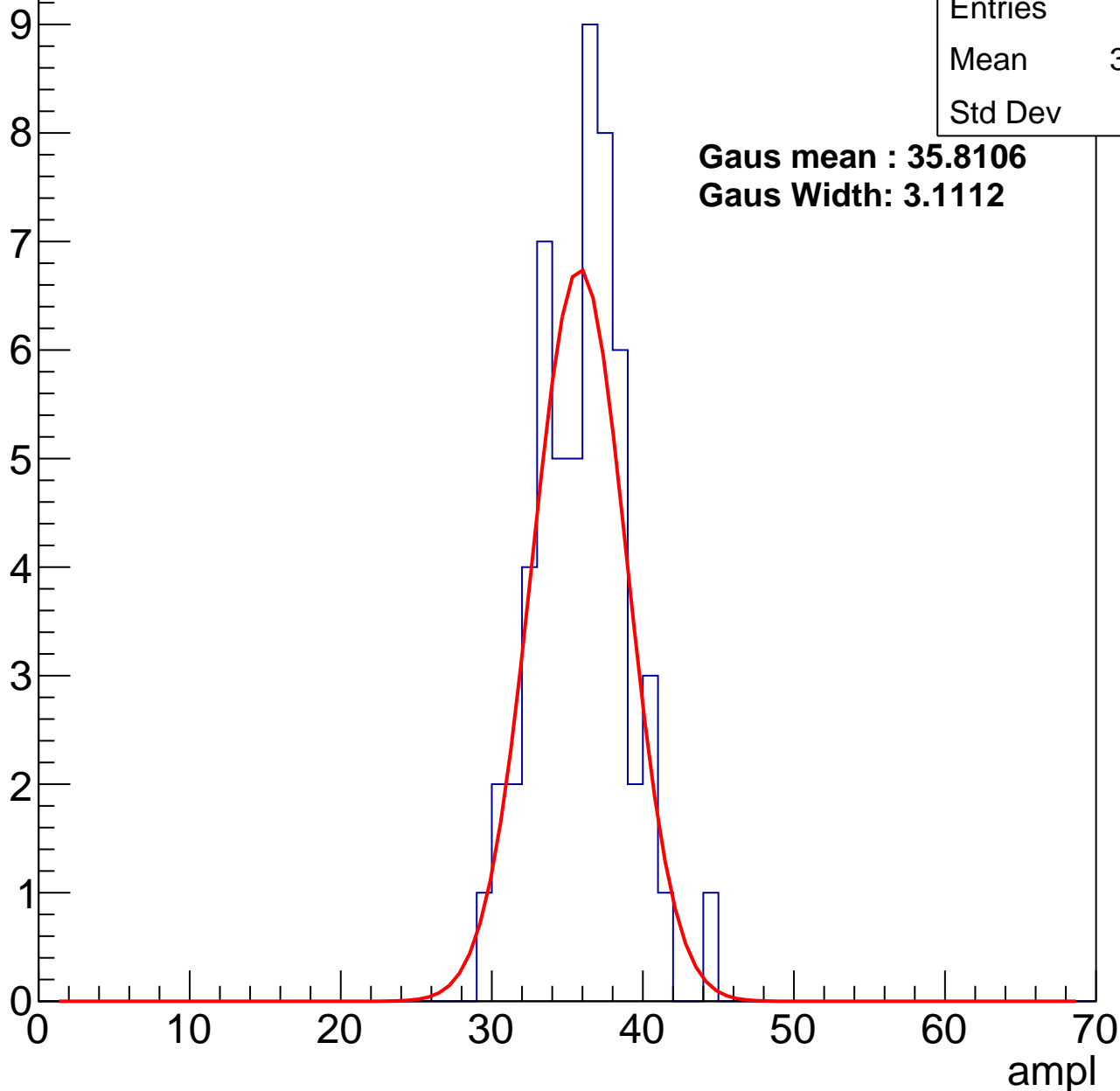
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	35.46
Std Dev	2.97

**Gaus mean : 35.8106**

**Gaus Width: 3.1112**



# B0L001S, U24-ch72, adc2

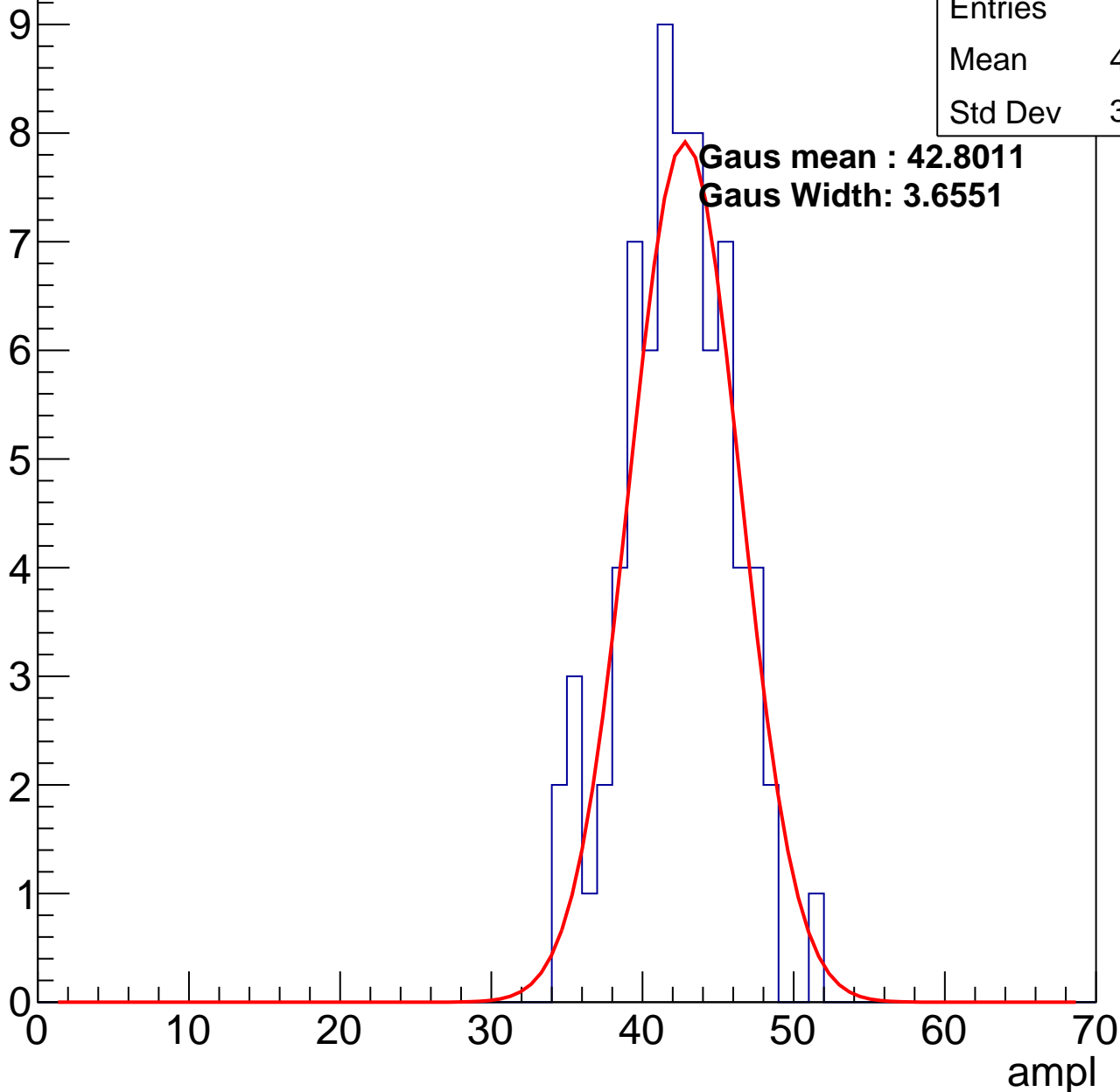
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	41.82
Std Dev	3.546

**Gaus mean : 42.8011**

**Gaus Width: 3.6551**

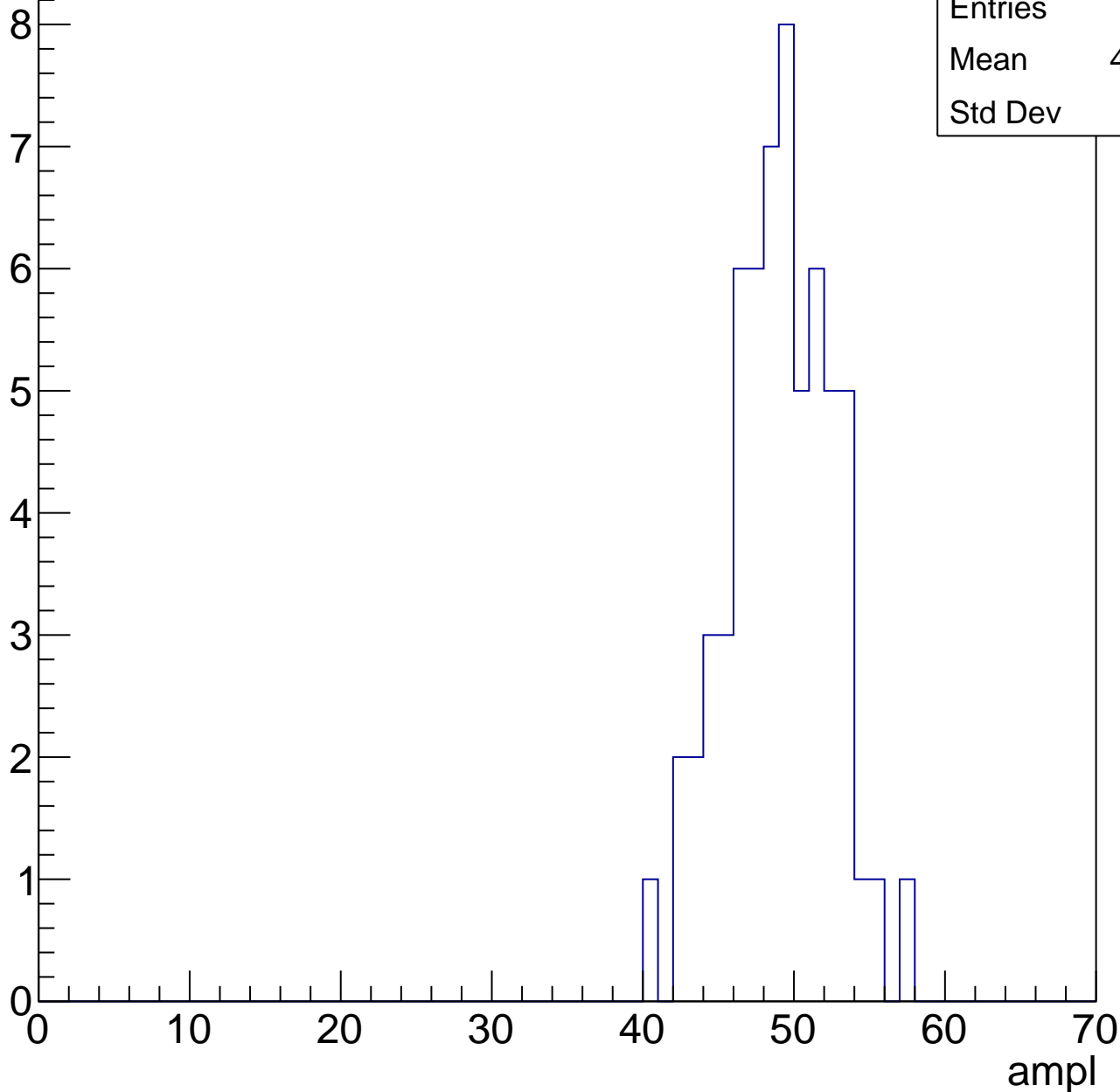


# B0L001S, U24-ch72, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

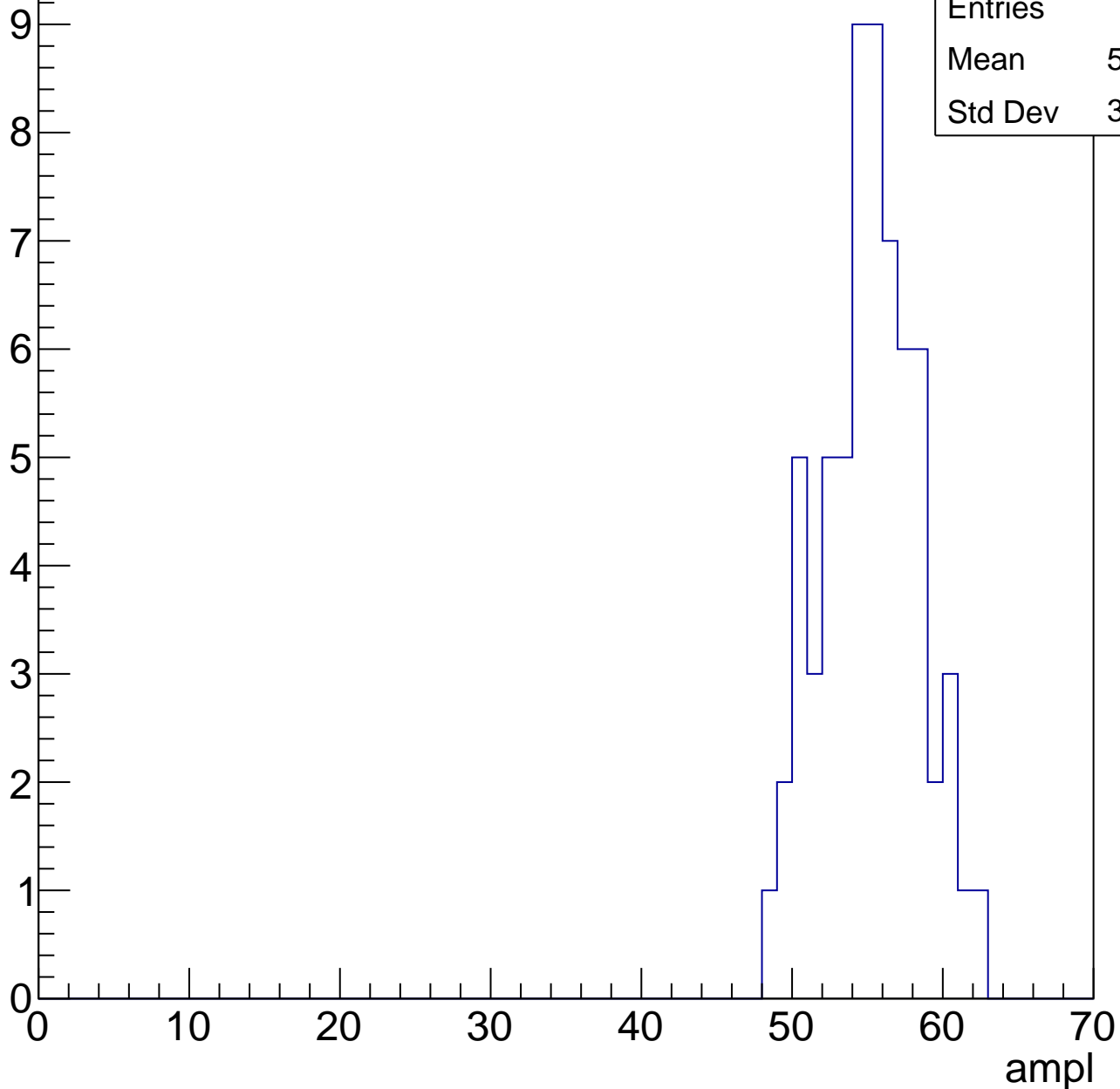
Entries	62
Mean	48.55
Std Dev	3.42



# B0L001S, U24-ch72, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U24-ch72, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

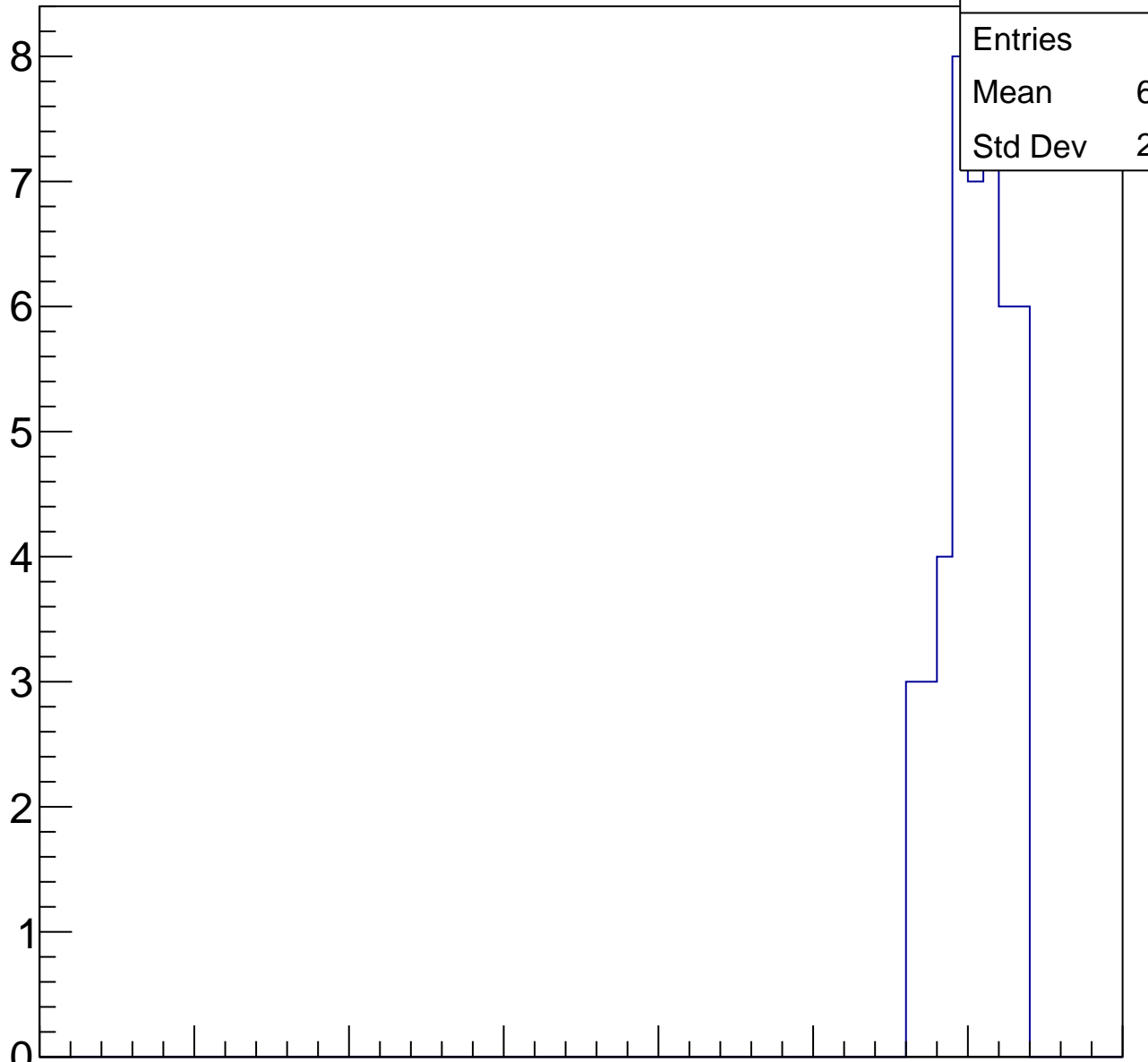
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	45
Mean	60.02
Std Dev	2.027

ampl

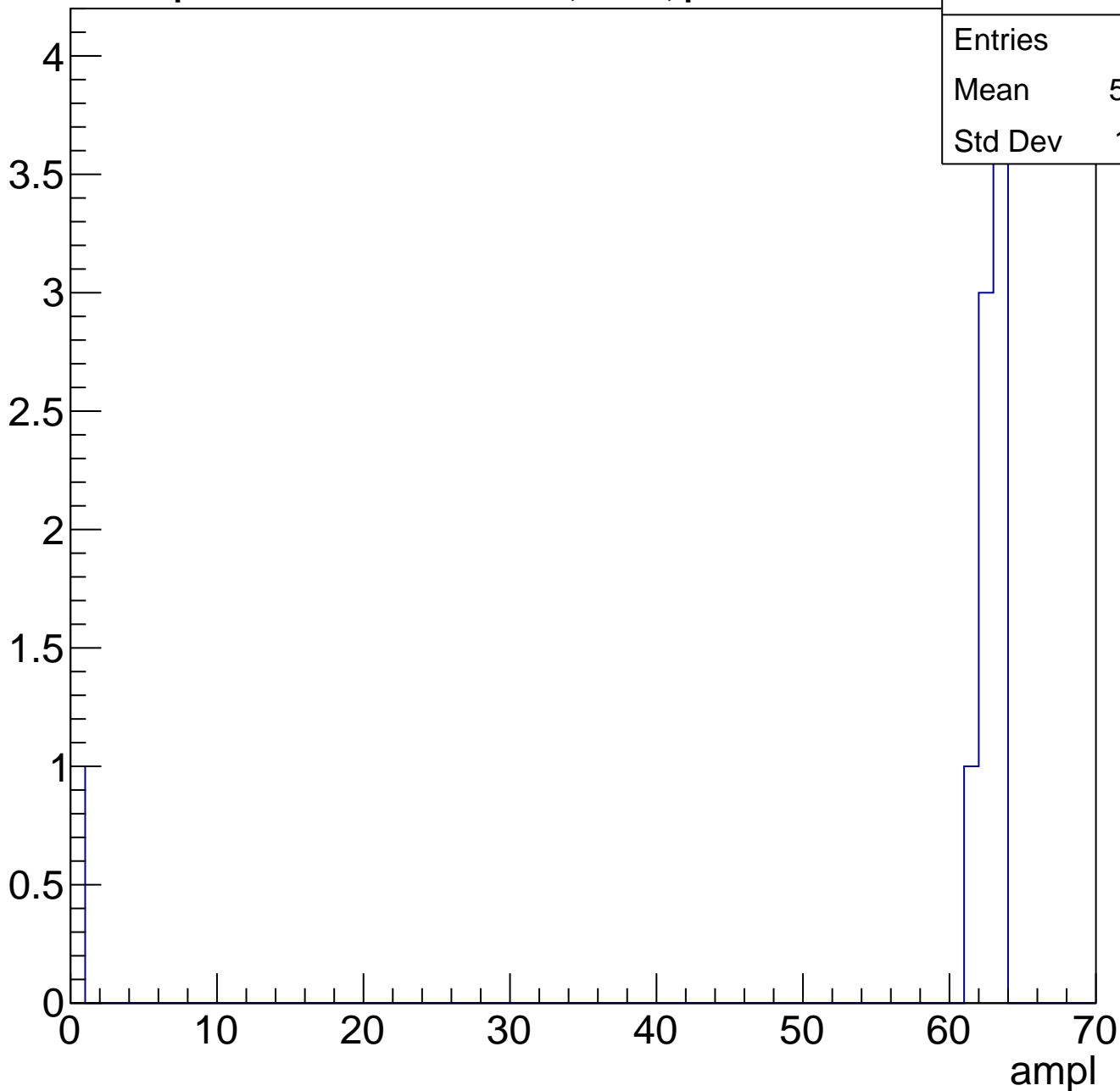
0 10 20 30 40 50 60 70



# B0L001S, U24-ch72, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch72, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U24-ch73, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	97
Mean	32.32
Std Dev	3.671

**Gaus mean : 32.8219**

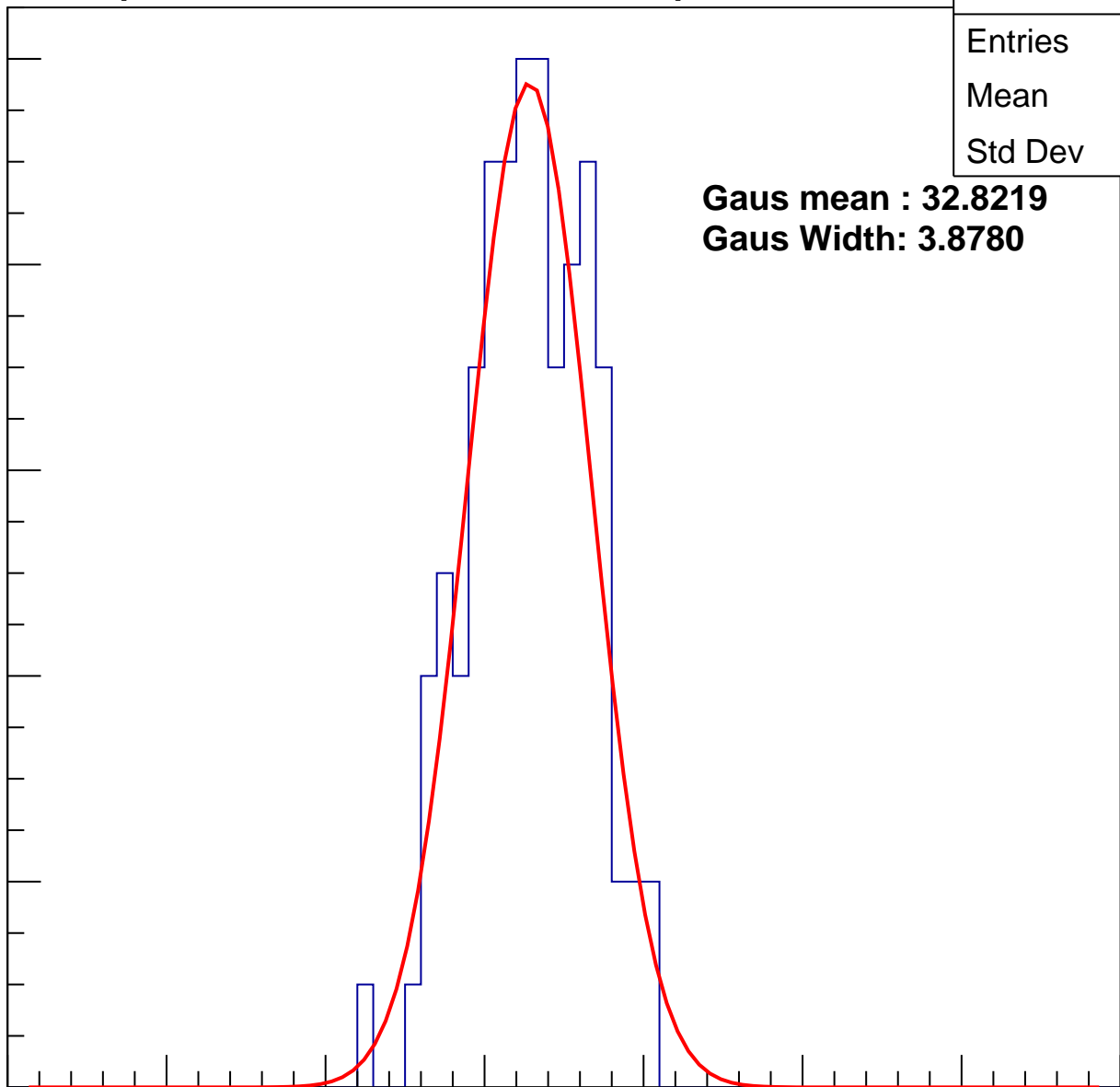
**Gaus Width: 3.8780**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U24-ch73, adc1

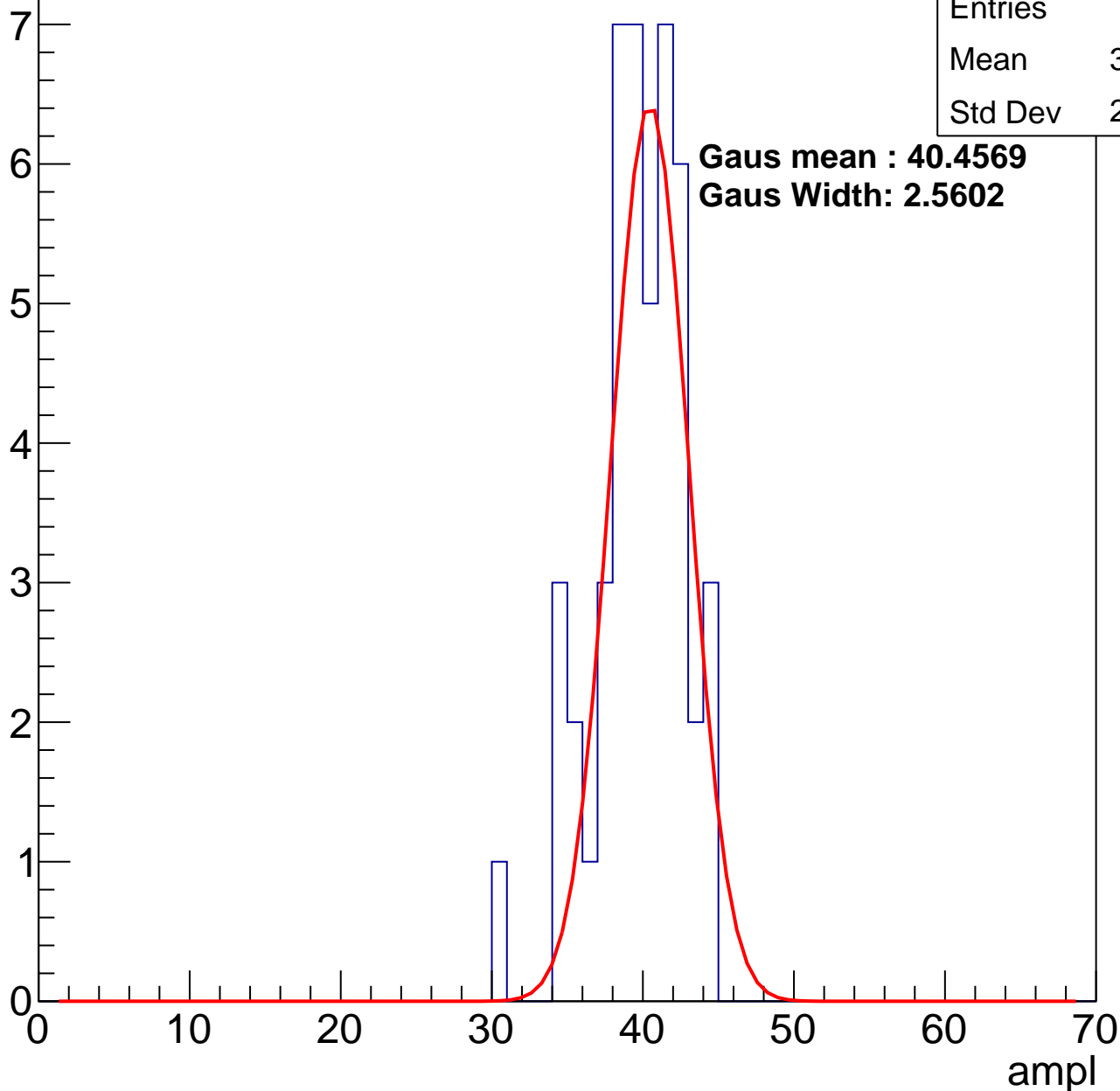
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	47
Mean	39.26
Std Dev	2.942

**Gaus mean : 40.4569**

**Gaus Width: 2.5602**



# B0L001S, U24-ch73, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	45.25
Std Dev	3.117

**Gaus mean : 45.7787**

**Gaus Width: 3.2280**

10

8

6

4

2

0

0

10

20

30

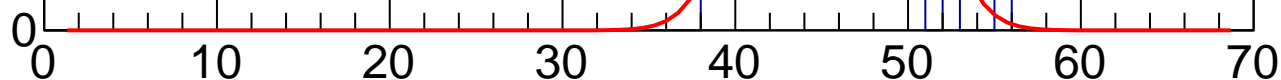
40

50

60

70

ampl

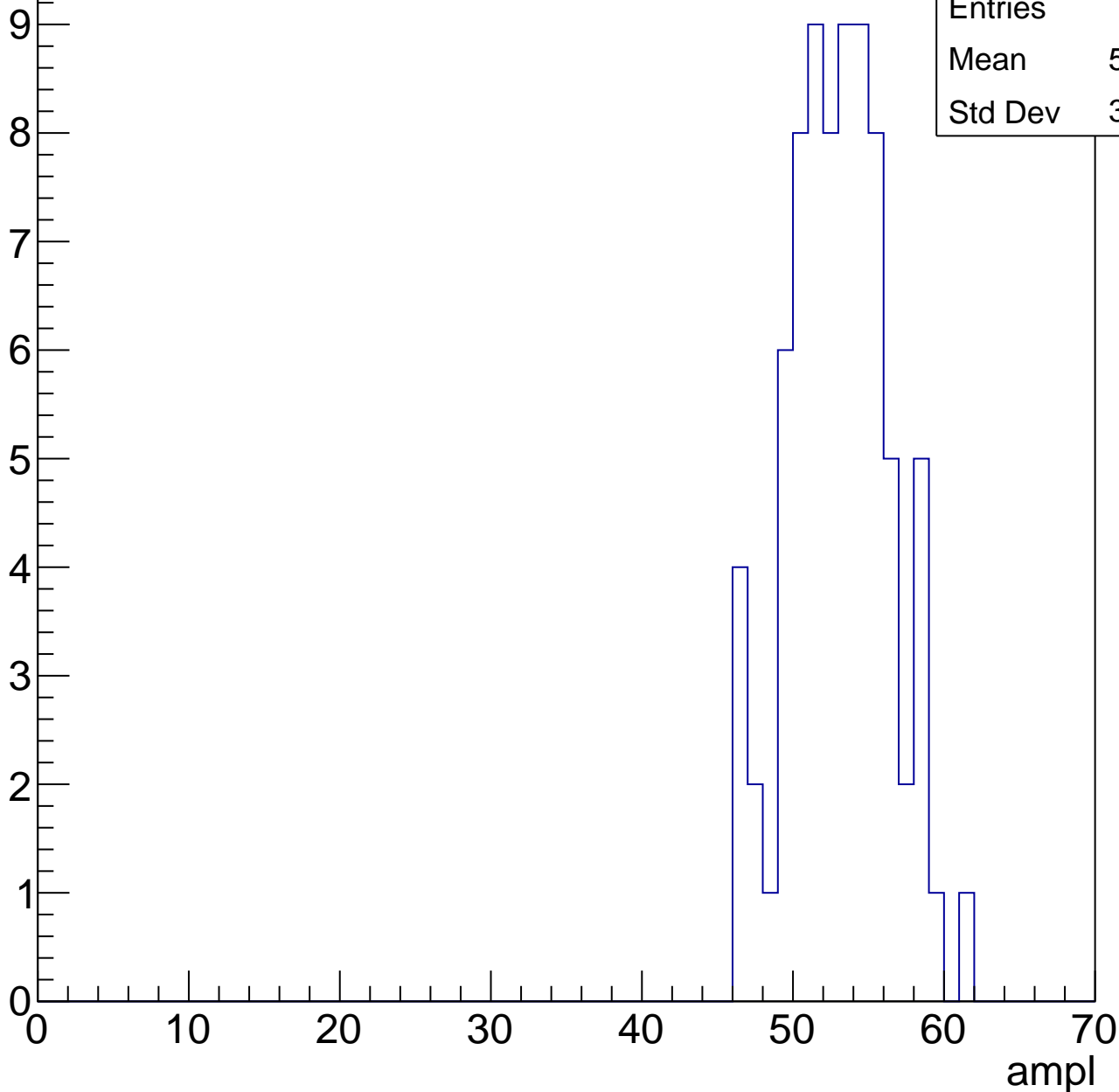


# B0L001S, U24-ch73, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

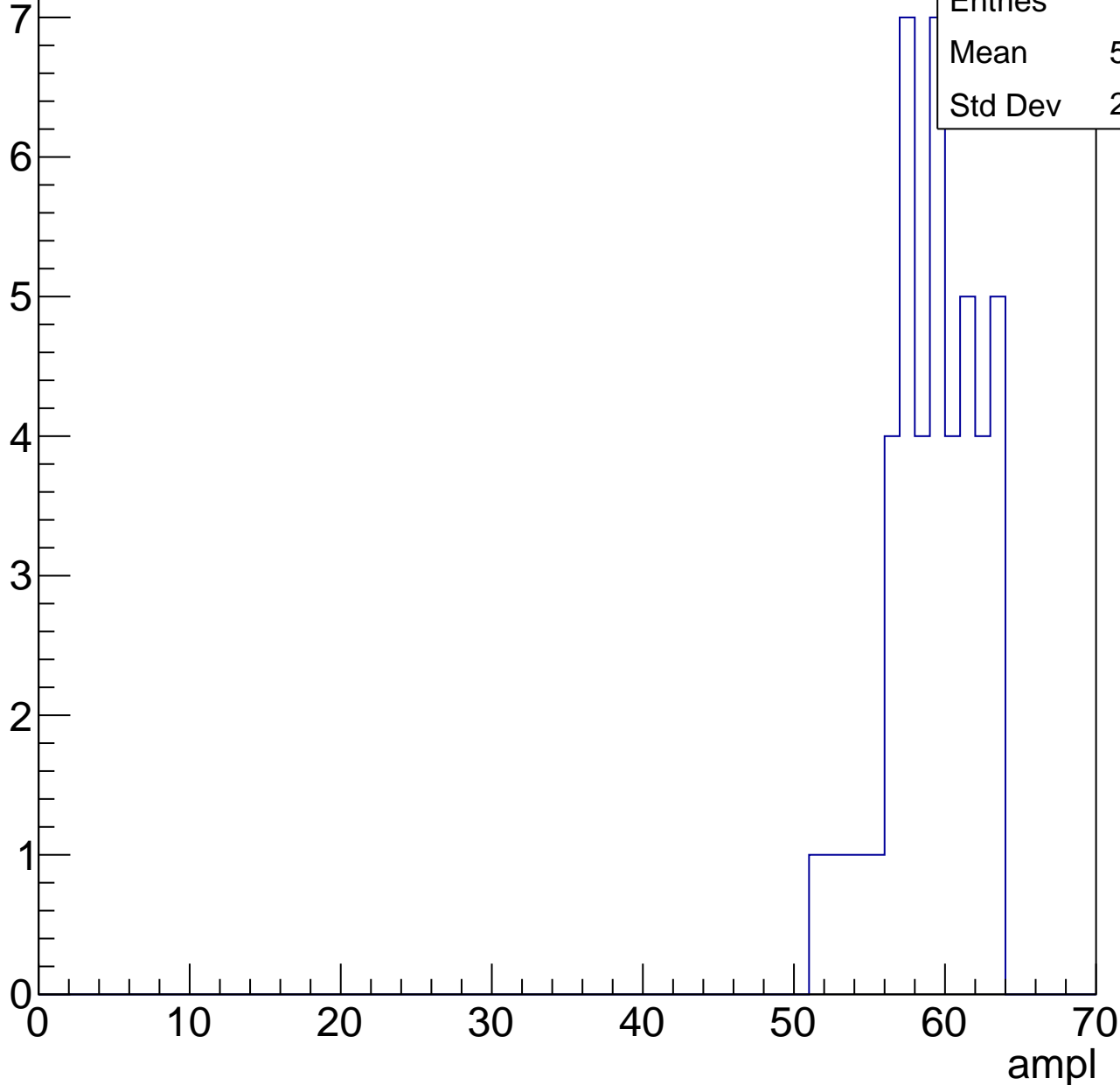
Entries	78
Mean	52.59
Std Dev	3.272



# B0L001S, U24-ch73, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

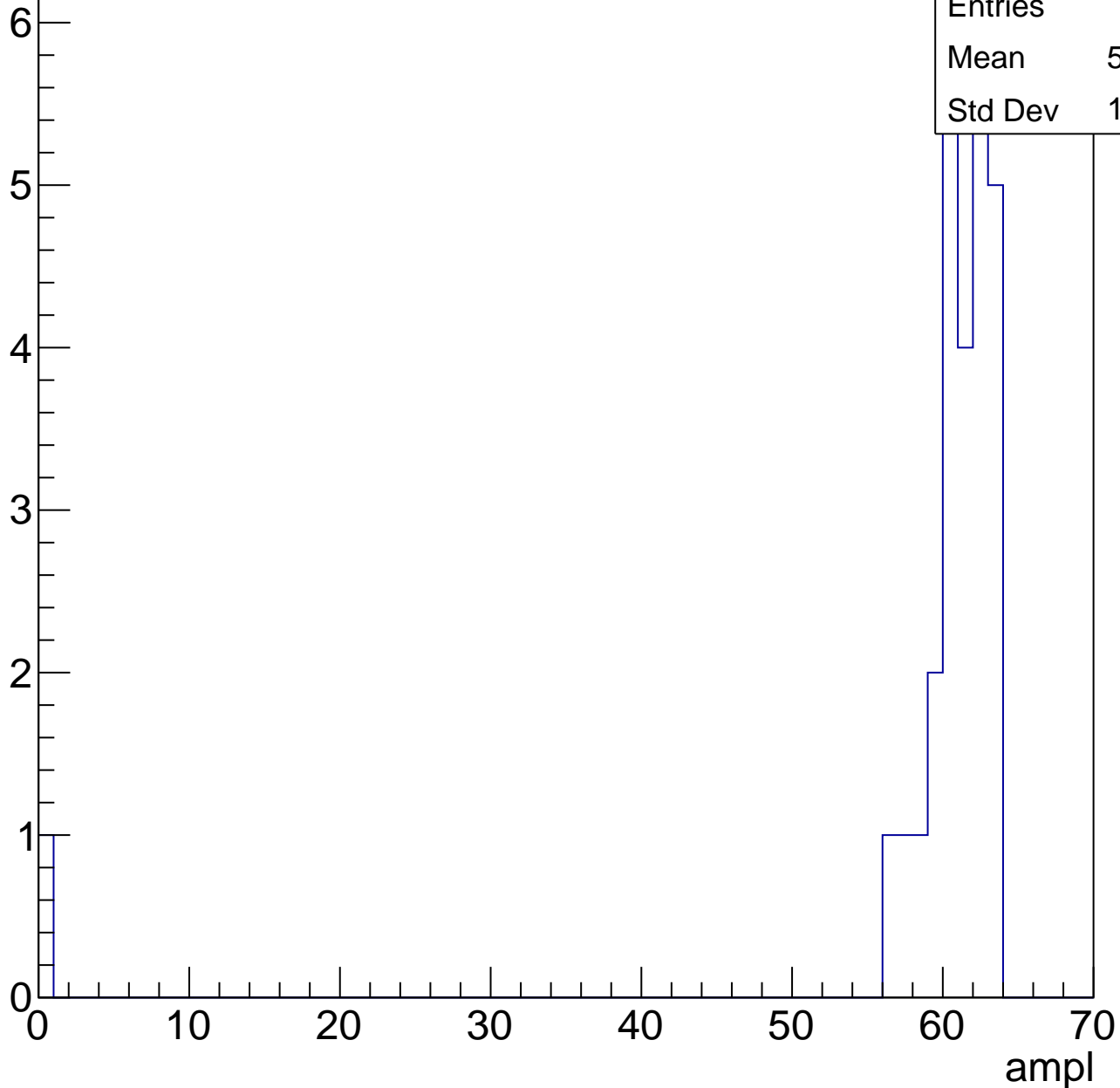
Entry



# B0L001S, U24-ch73, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U24-ch73, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U24-ch73, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U24-ch74, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	73
Mean	29.47
Std Dev	4.803

**Gaus mean : 30.4606**

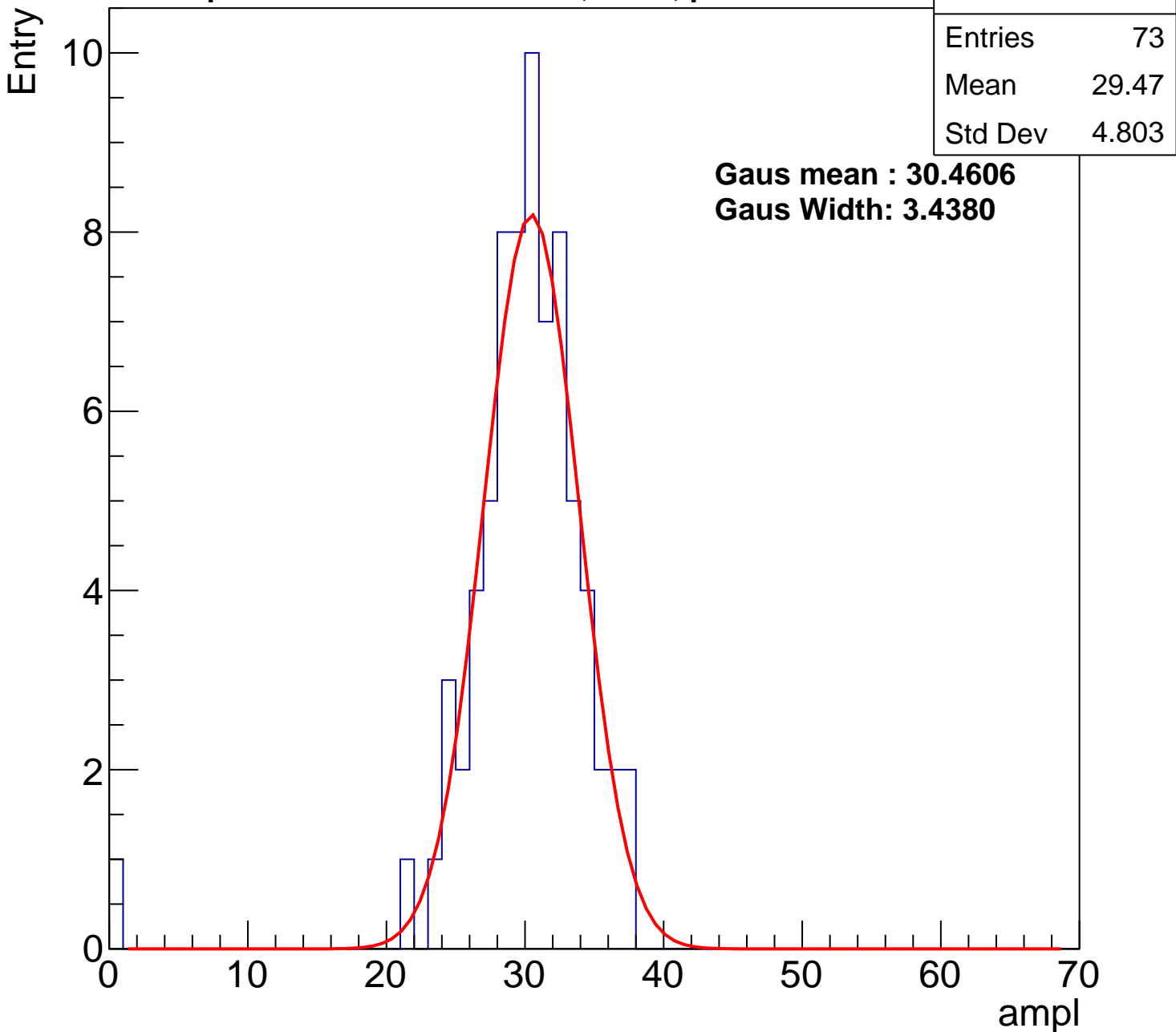
**Gaus Width: 3.4380**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U24-ch74, adc1

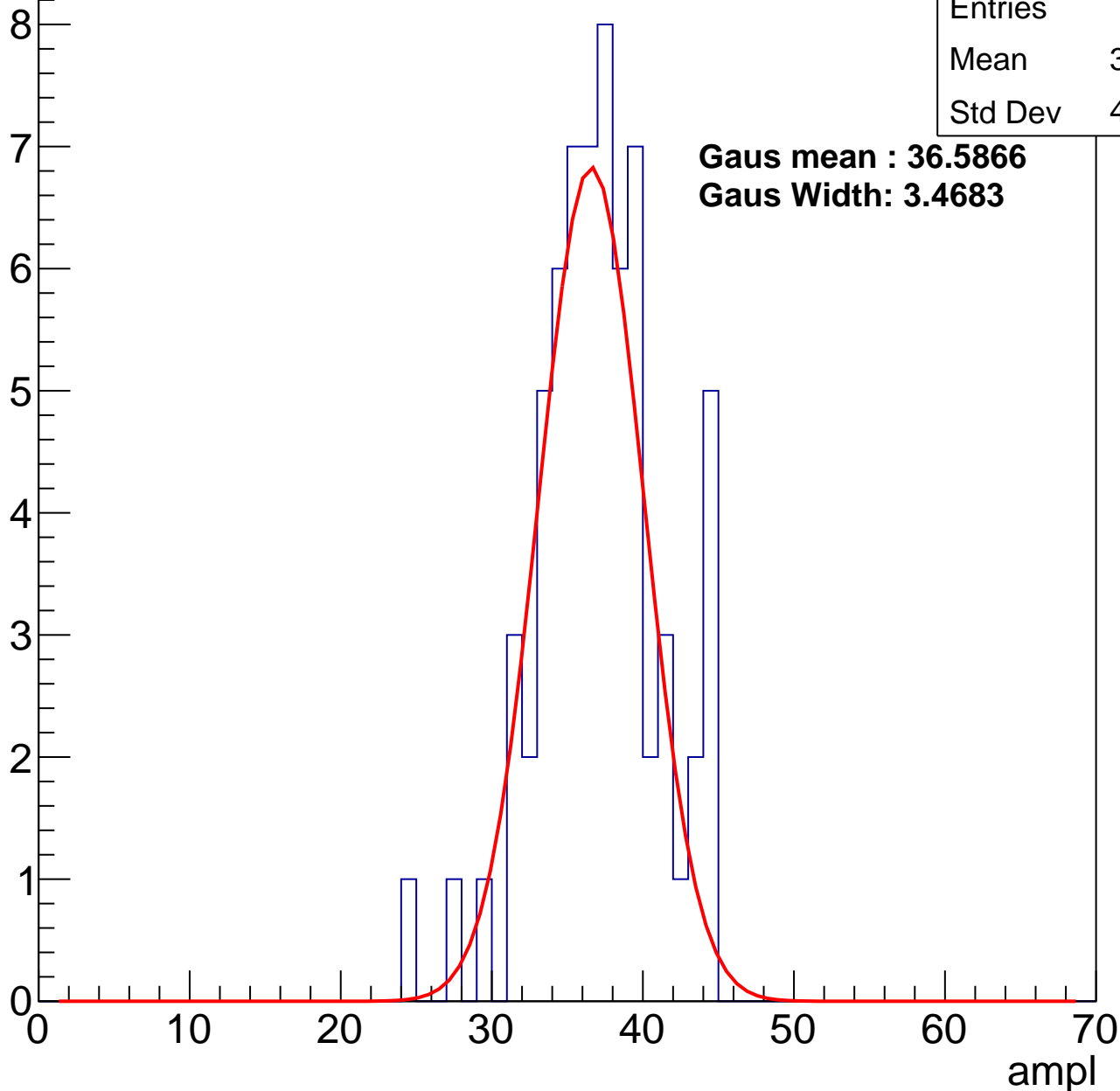
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	36.58
Std Dev	4.034

**Gaus mean : 36.5866**

**Gaus Width: 3.4683**



# B0L001S, U24-ch74, adc2

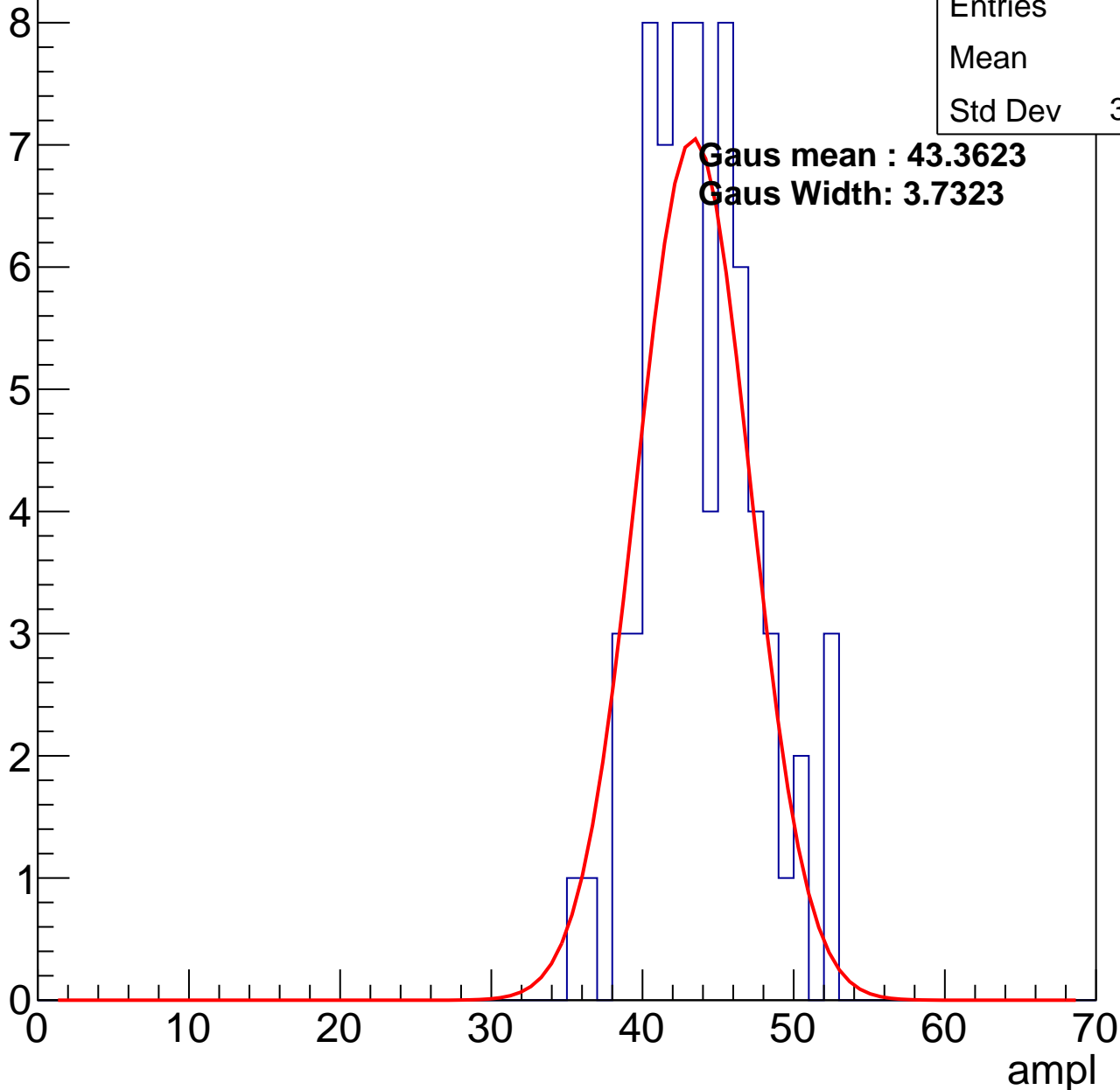
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	43.4
Std Dev	3.662

**Gaus mean : 43.3623**

**Gaus Width: 3.7323**

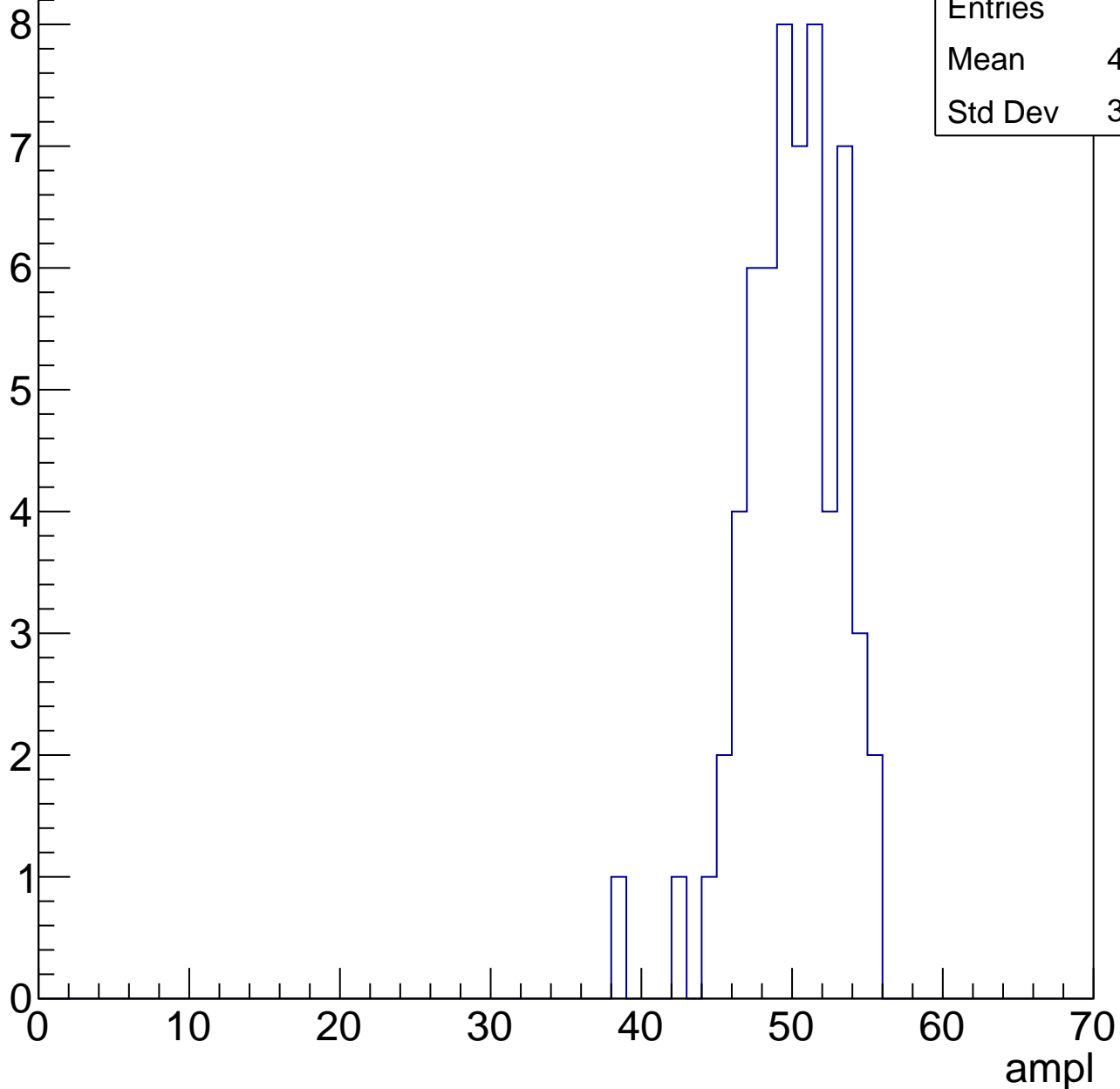


# B0L001S, U24-ch74, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	49.48
Std Dev	3.196

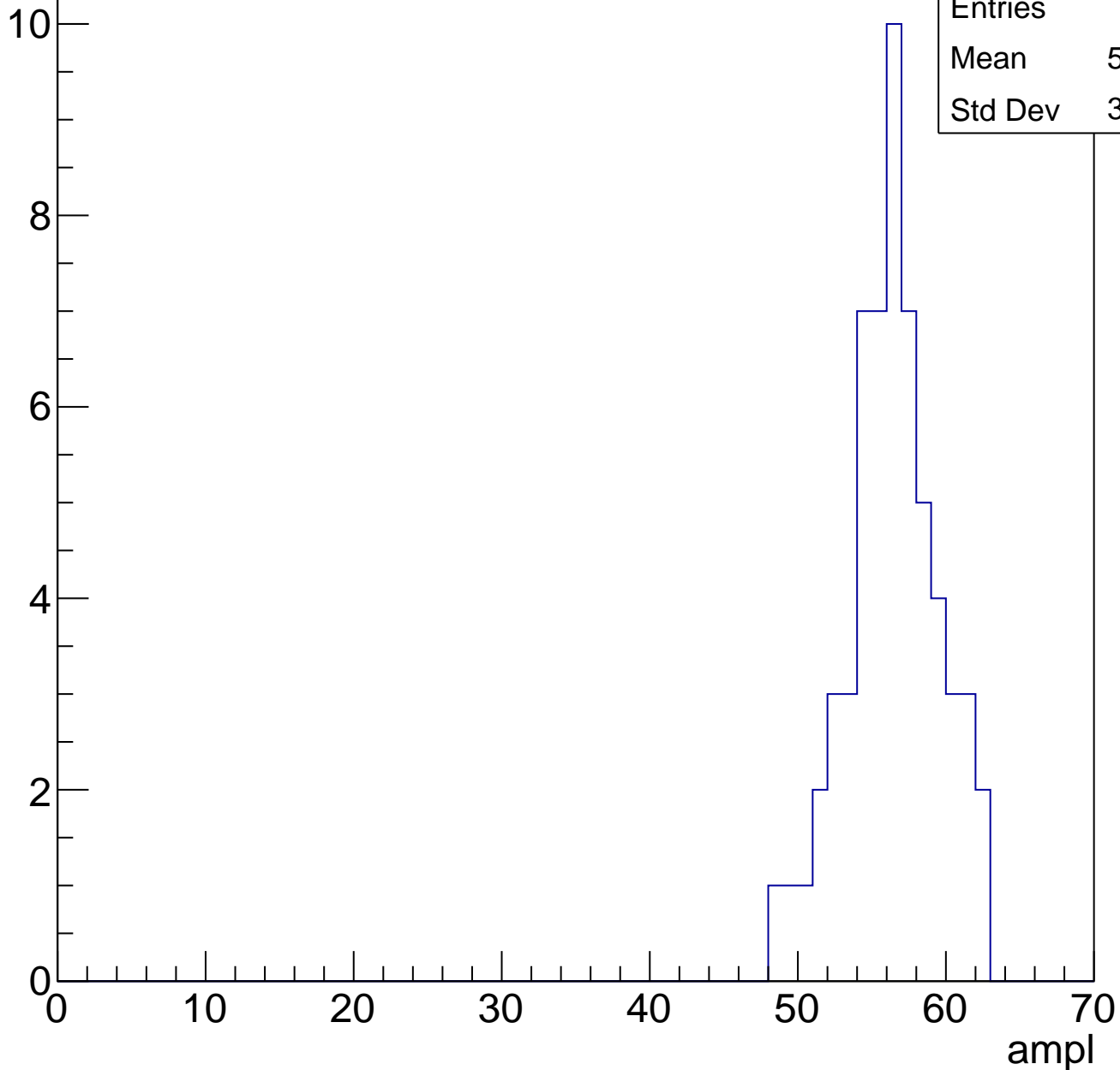


# B0L001S, U24-ch74, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	59
Mean	55.92
Std Dev	3.099

Entry

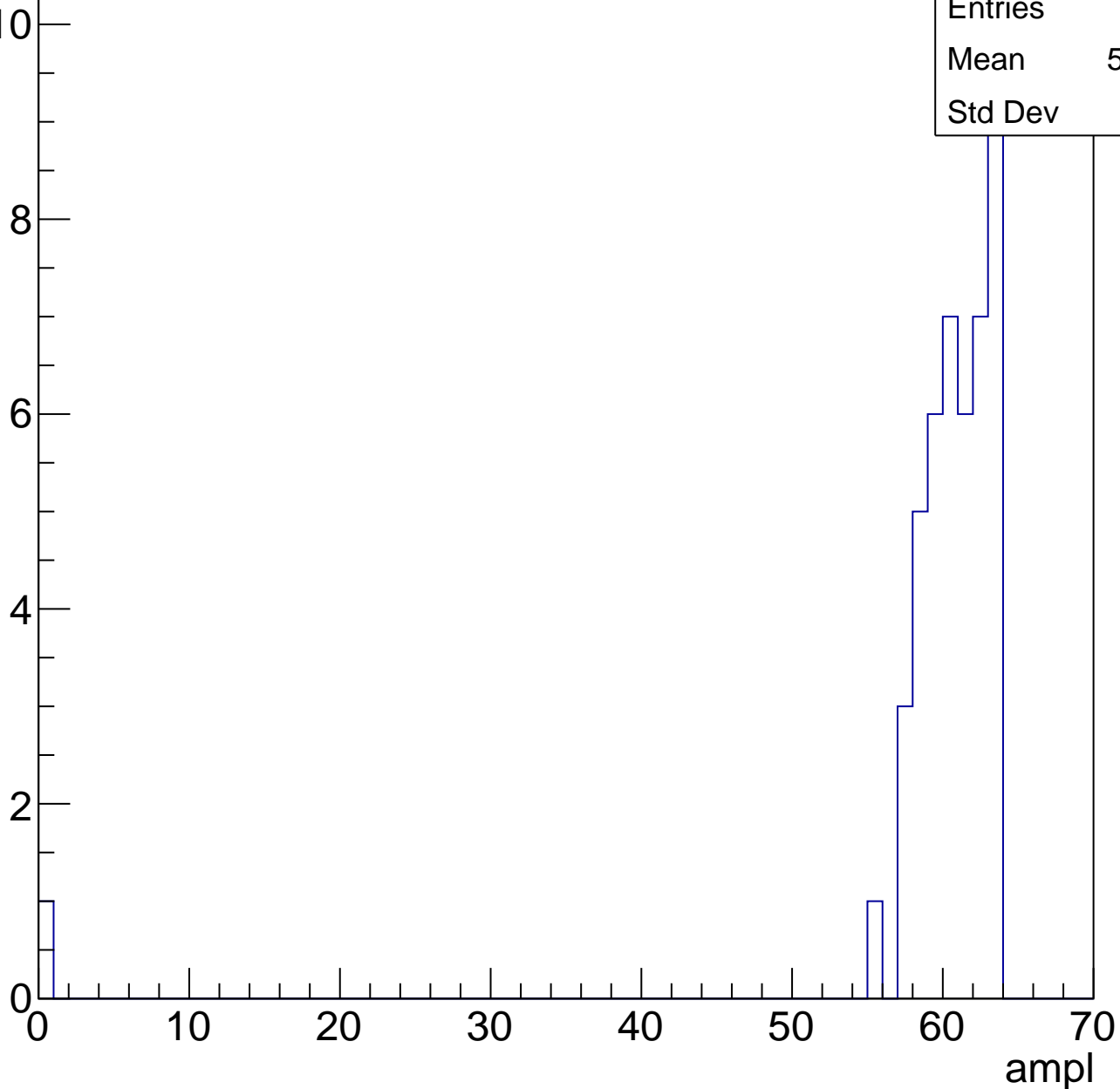


# B0L001S, U24-ch74, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	46
Mean	59.13
Std Dev	9.05



# B0L001S, U24-ch74, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch74, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	3
Mean	0
Std Dev	0

# B0L001S, U24-ch75, adc0

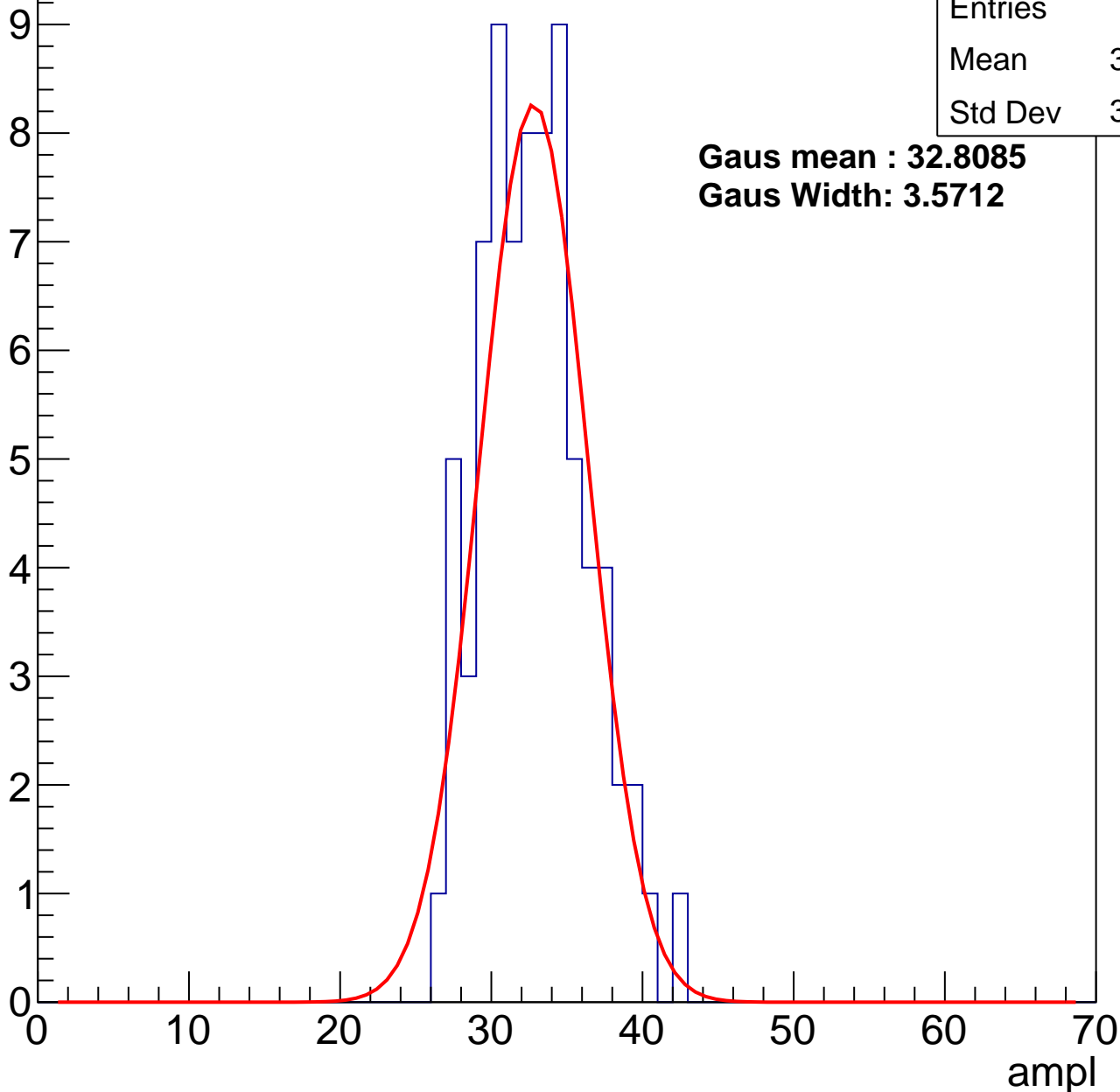
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	76
Mean	32.42
Std Dev	3.419

**Gaus mean : 32.8085**

**Gaus Width: 3.5712**



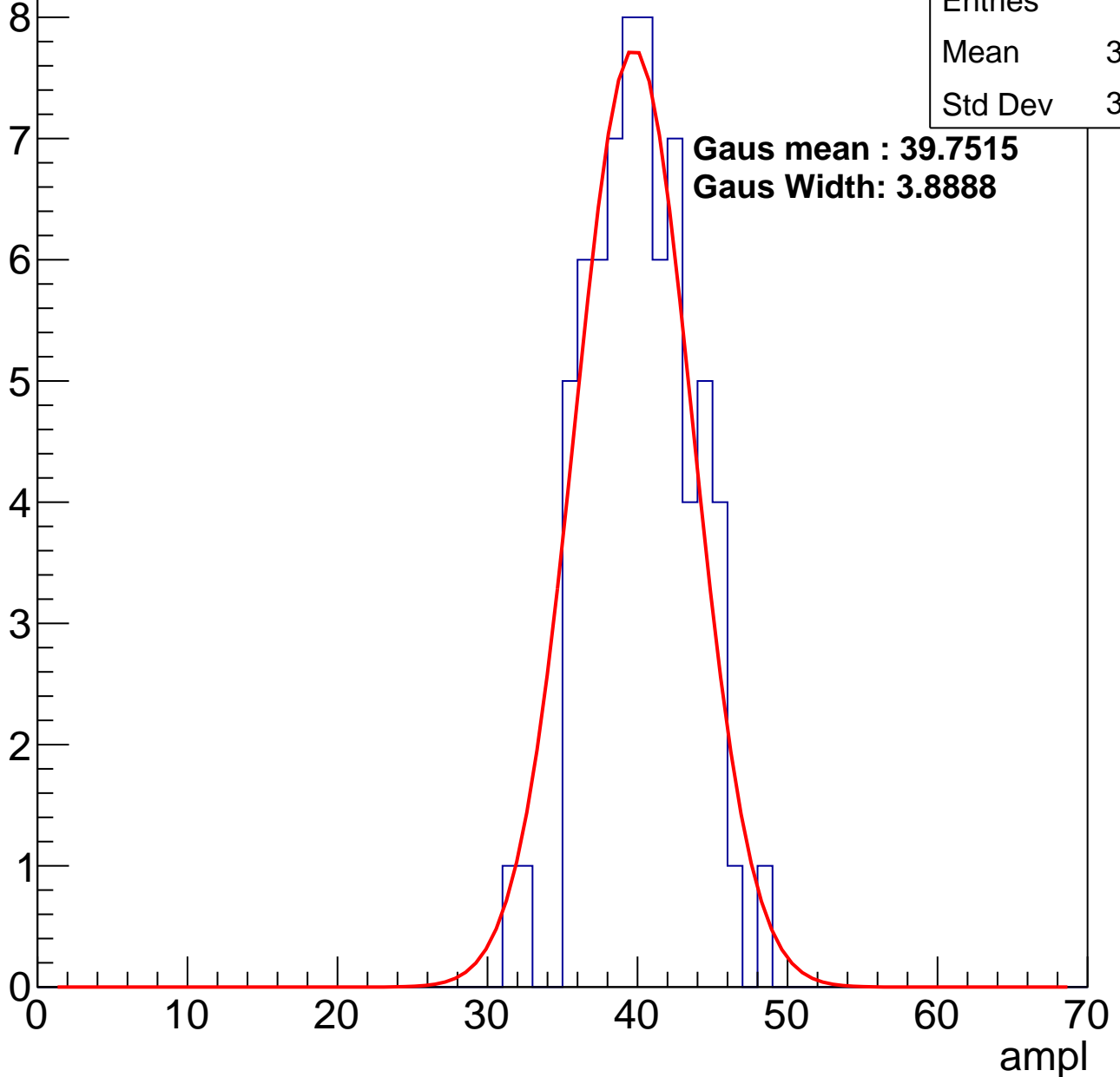
# B0L001S, U24-ch75, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	39.71
Std Dev	3.381

**Gaus mean : 39.7515**  
**Gaus Width: 3.8888**



# B0L001S, U24-ch75, adc2

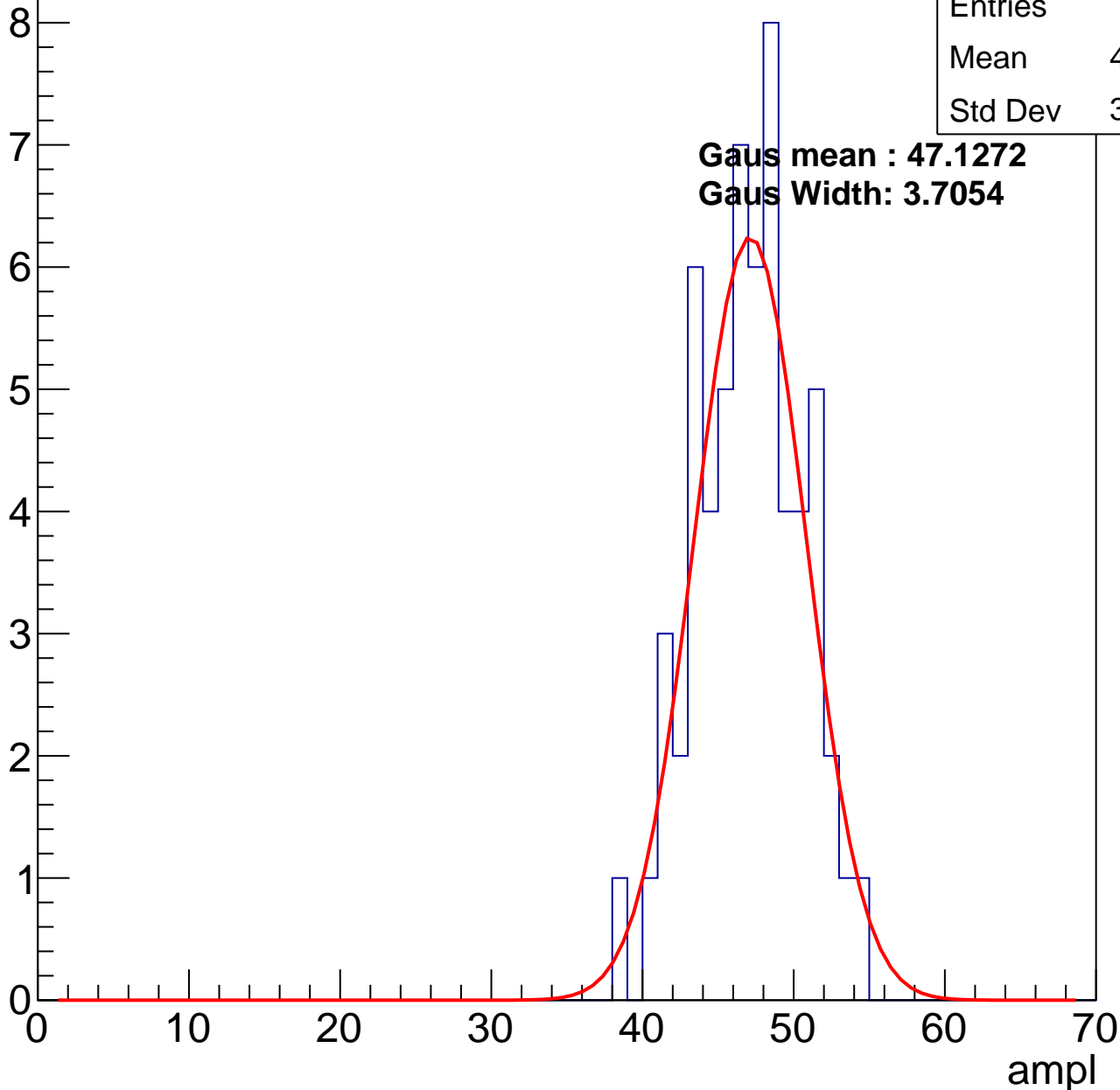
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	46.57
Std Dev	3.442

**Gaus mean : 47.1272**

**Gaus Width: 3.7054**

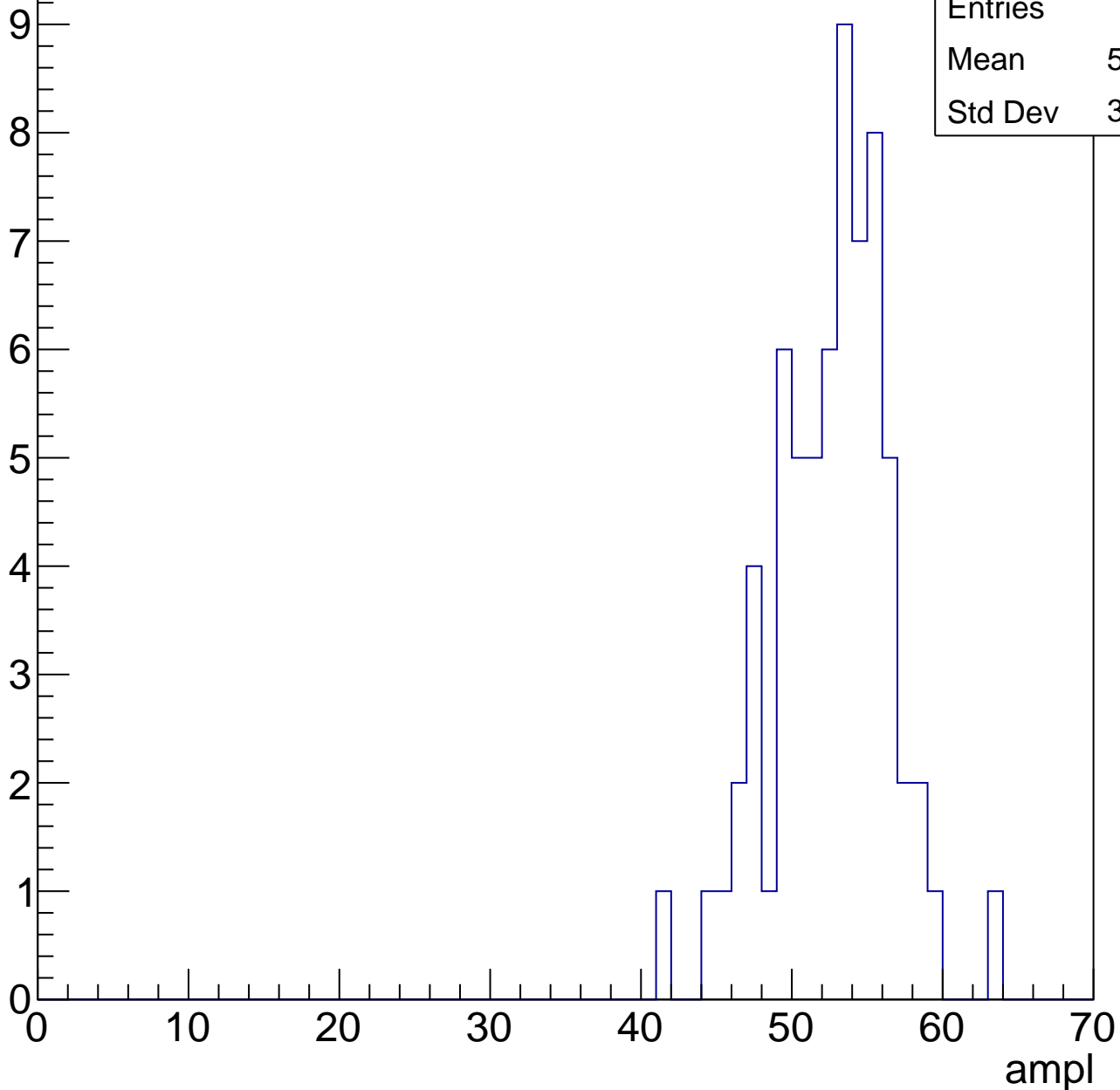


# B0L001S, U24-ch75, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	52.18
Std Dev	3.824

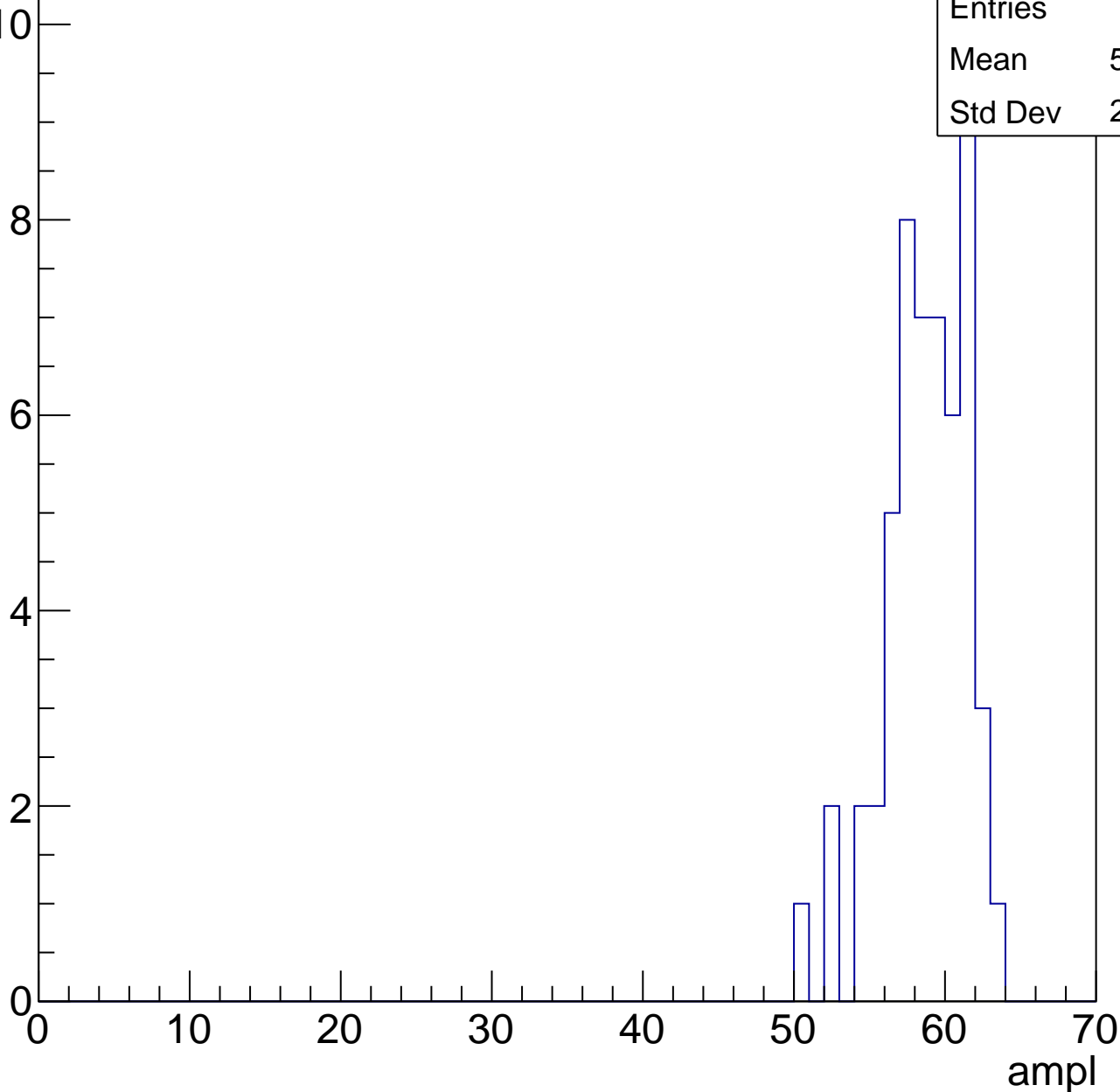


# B0L001S, U24-ch75, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	58.26
Std Dev	2.736

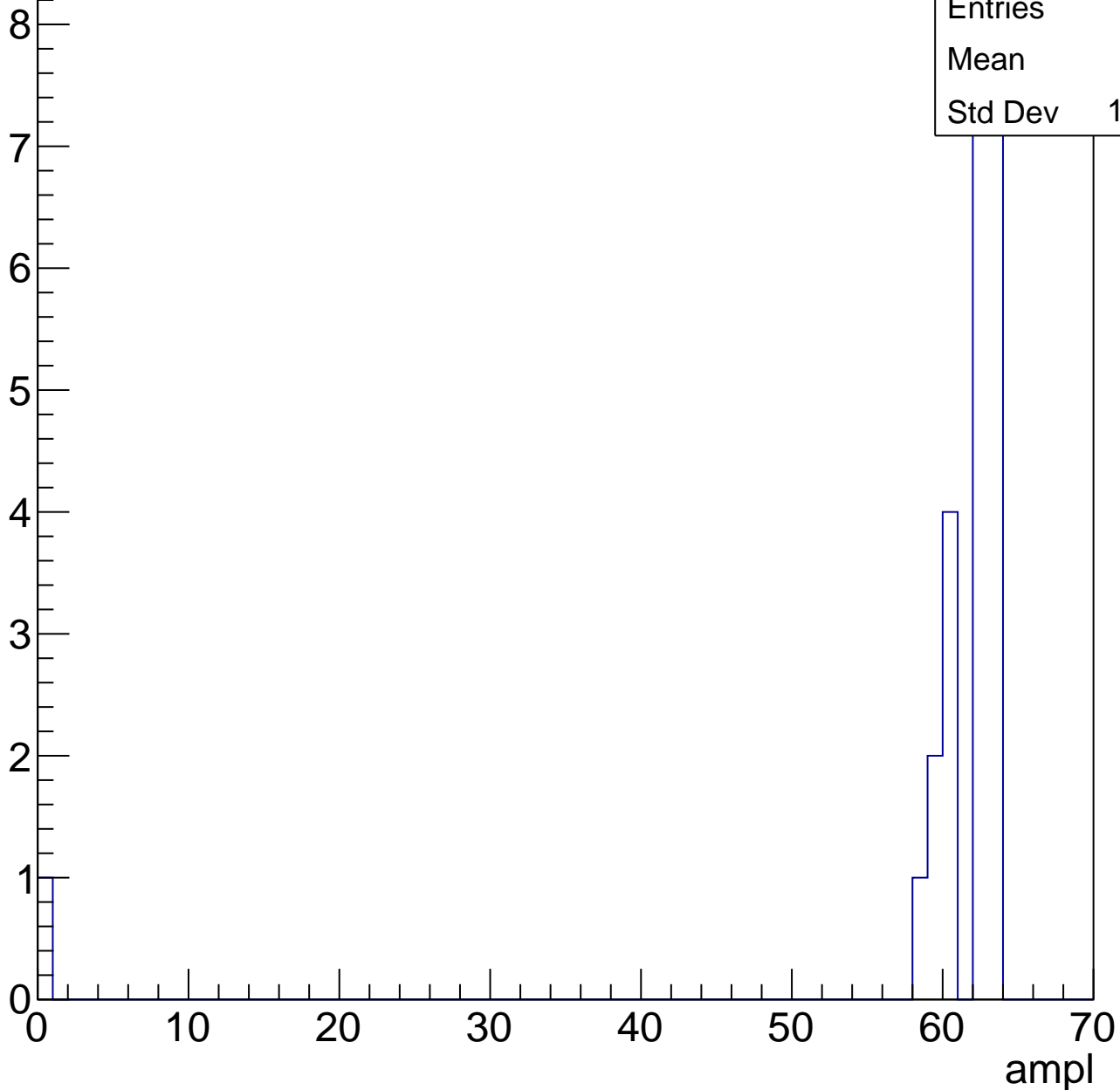


# B0L001S, U24-ch75, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	24
Mean	59
Std Dev	12.39



# B0L001S, U24-ch75, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

0

Mean

0

Std Dev

0



# B0L001S, U24-ch75, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U24-ch76, adc0

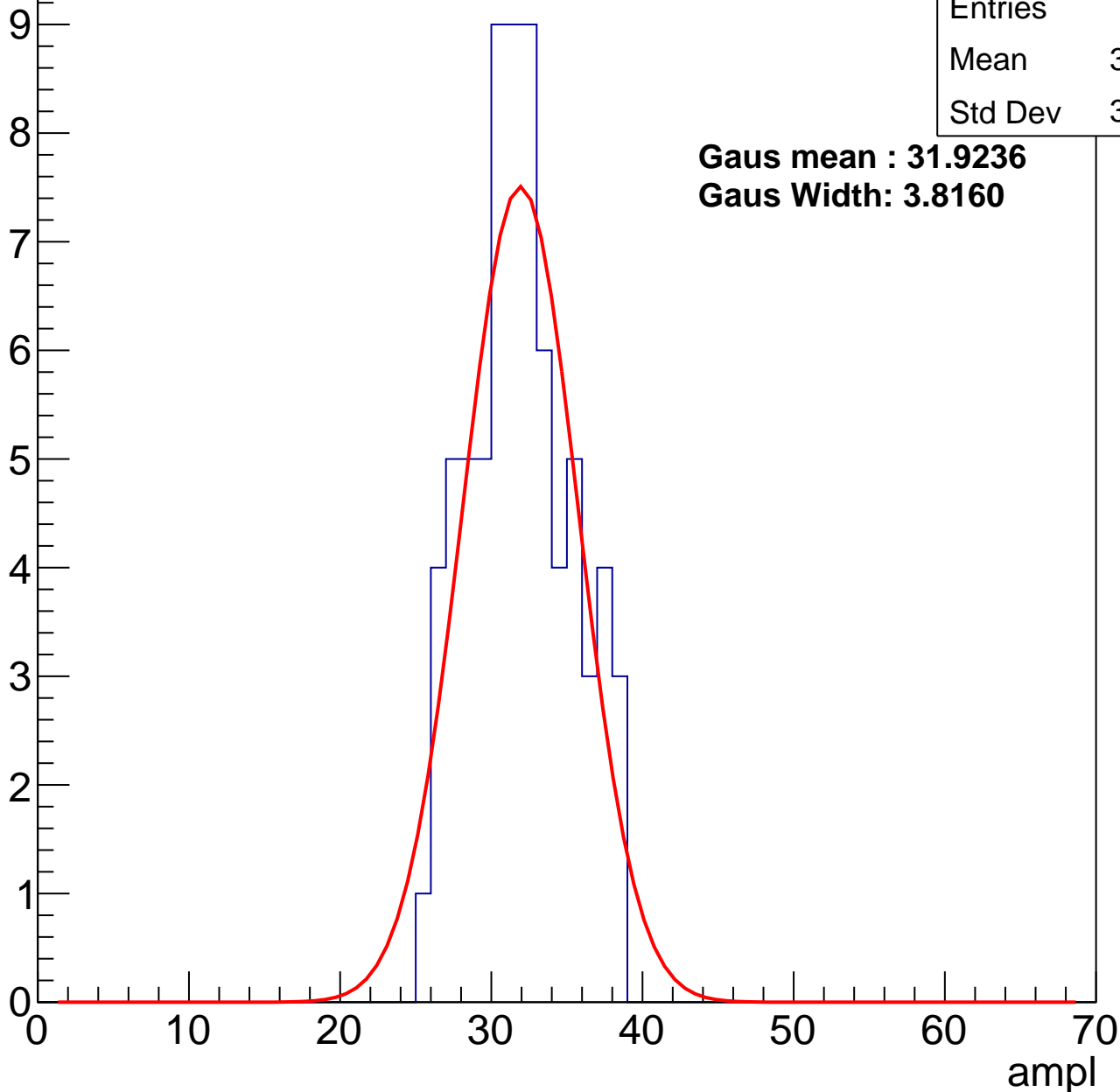
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	31.46
Std Dev	3.312

**Gaus mean : 31.9236**

**Gaus Width: 3.8160**



# B0L001S, U24-ch76, adc1

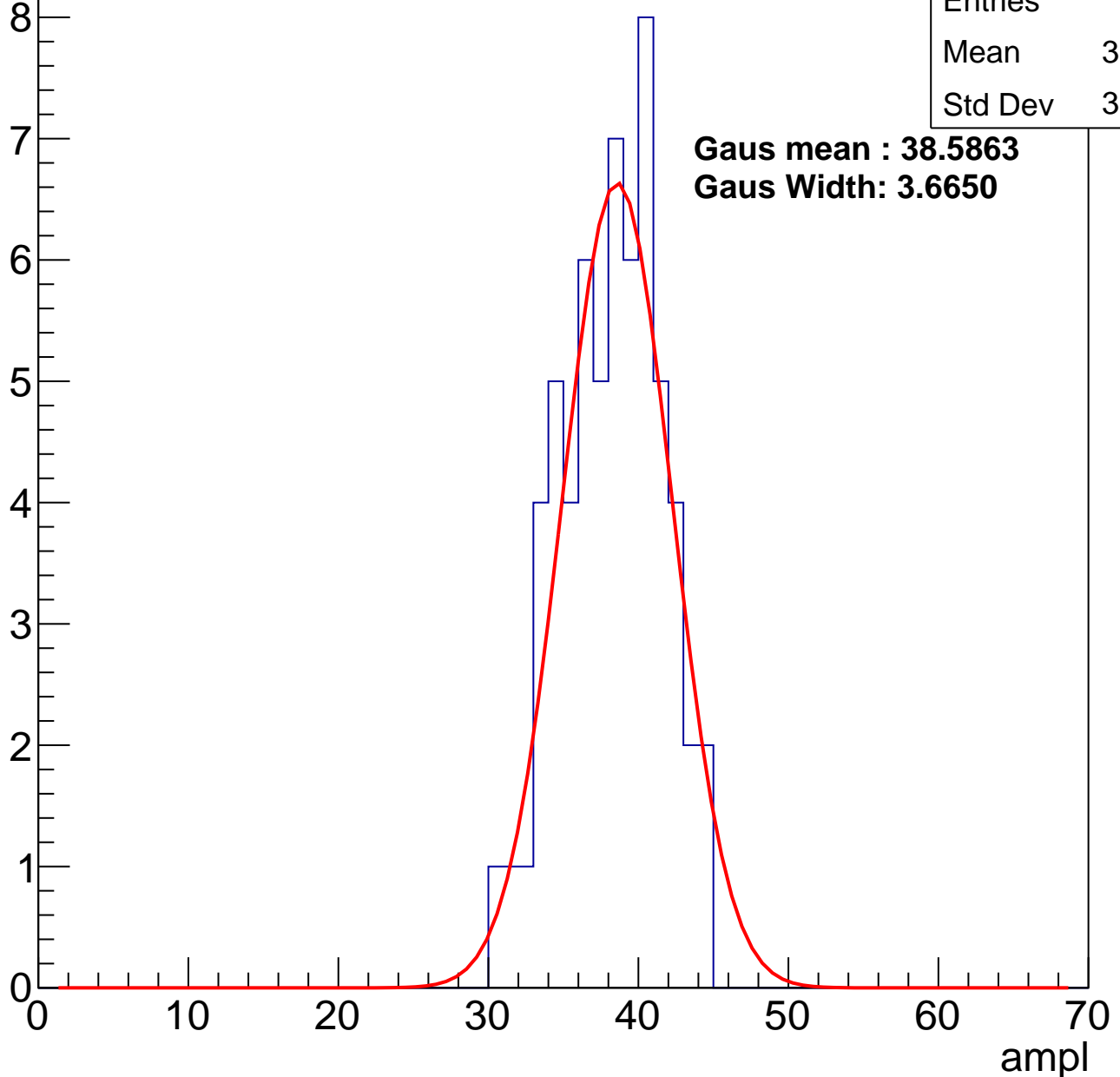
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	37.75
Std Dev	3.288

**Gaus mean : 38.5863**

**Gaus Width: 3.6650**



# B0L001S, U24-ch76, adc2

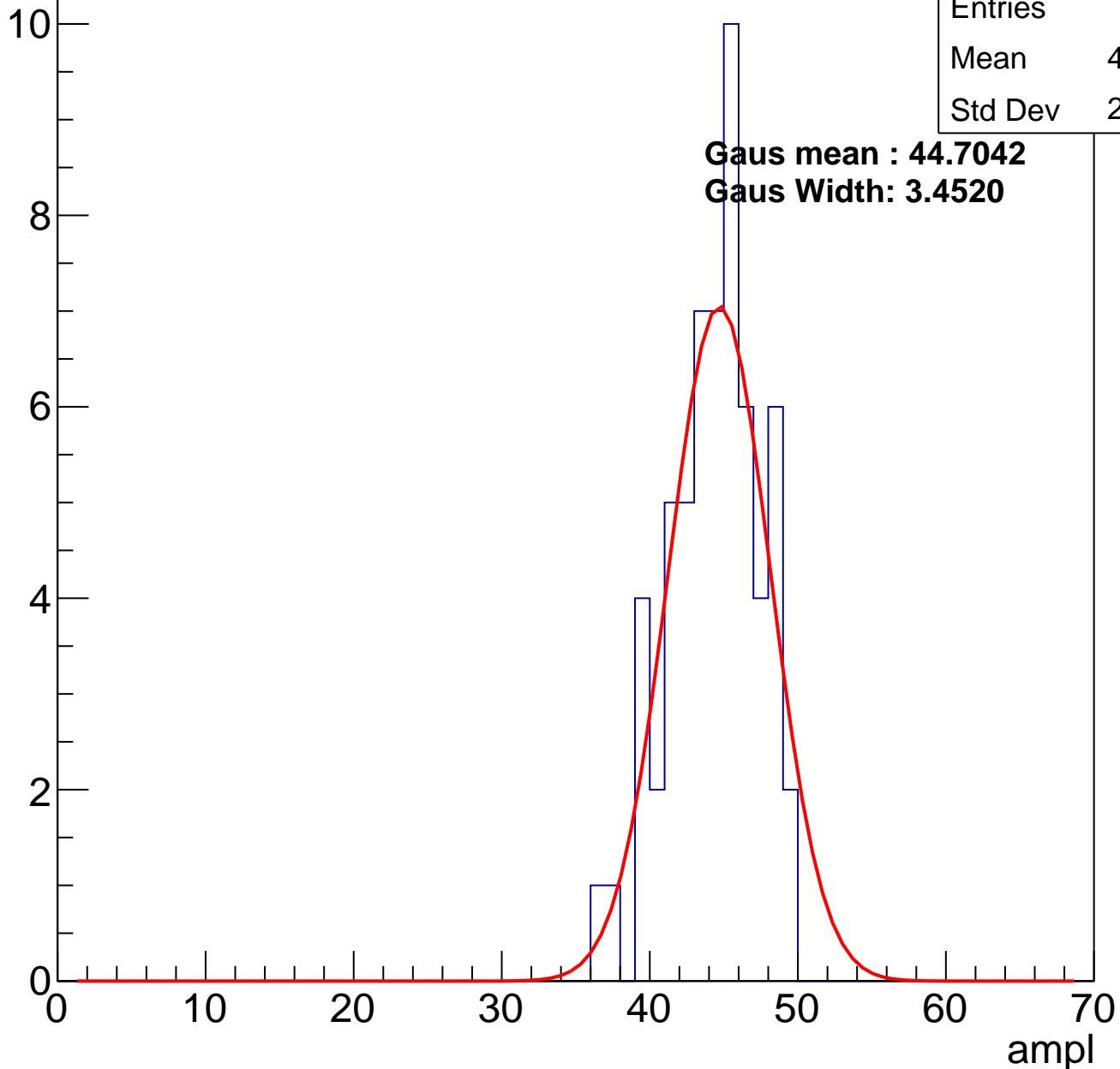
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	60
Mean	43.88
Std Dev	2.978

**Gaus mean : 44.7042**

**Gaus Width: 3.4520**

Entry

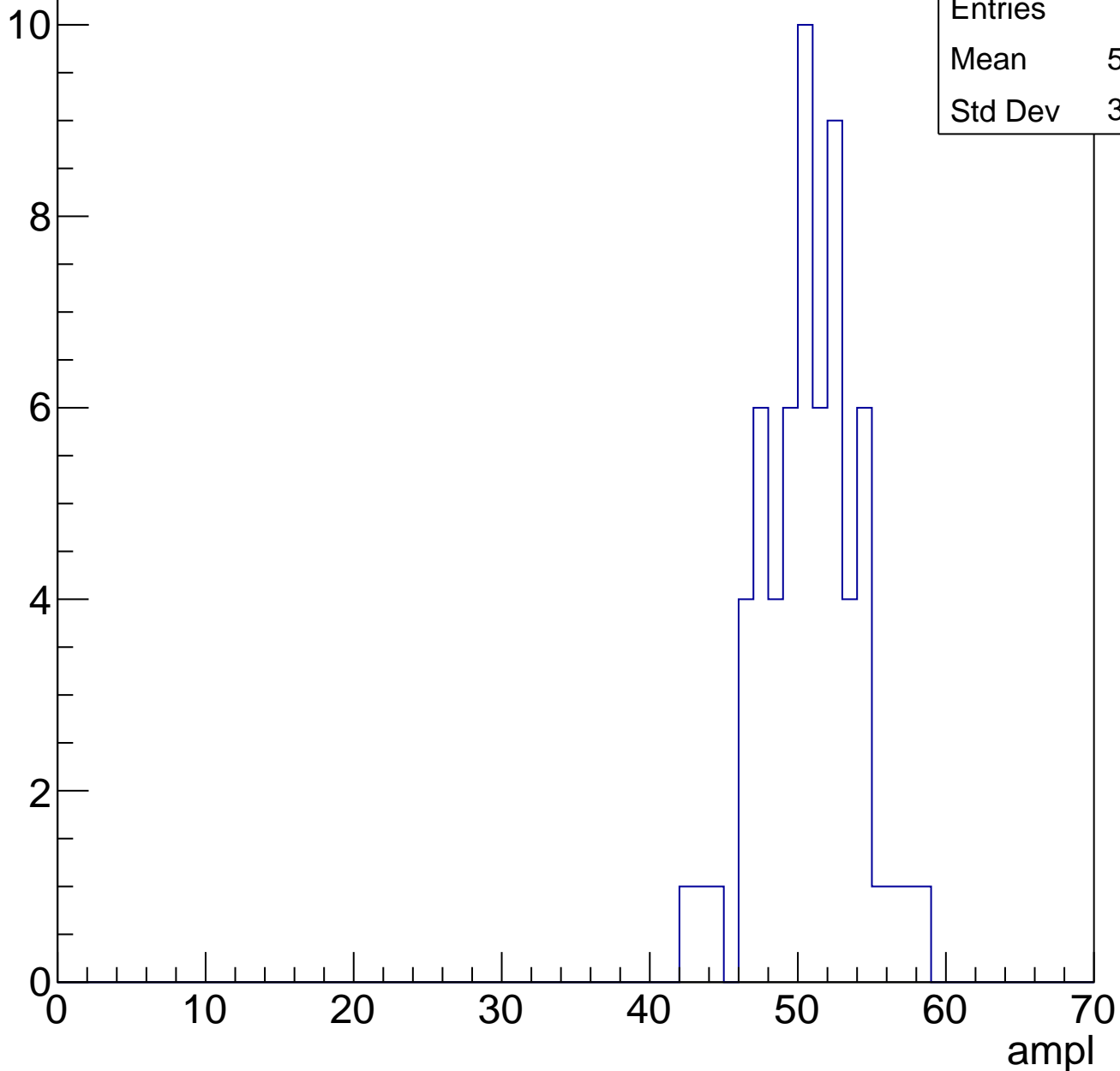


# B0L001S, U24-ch76, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

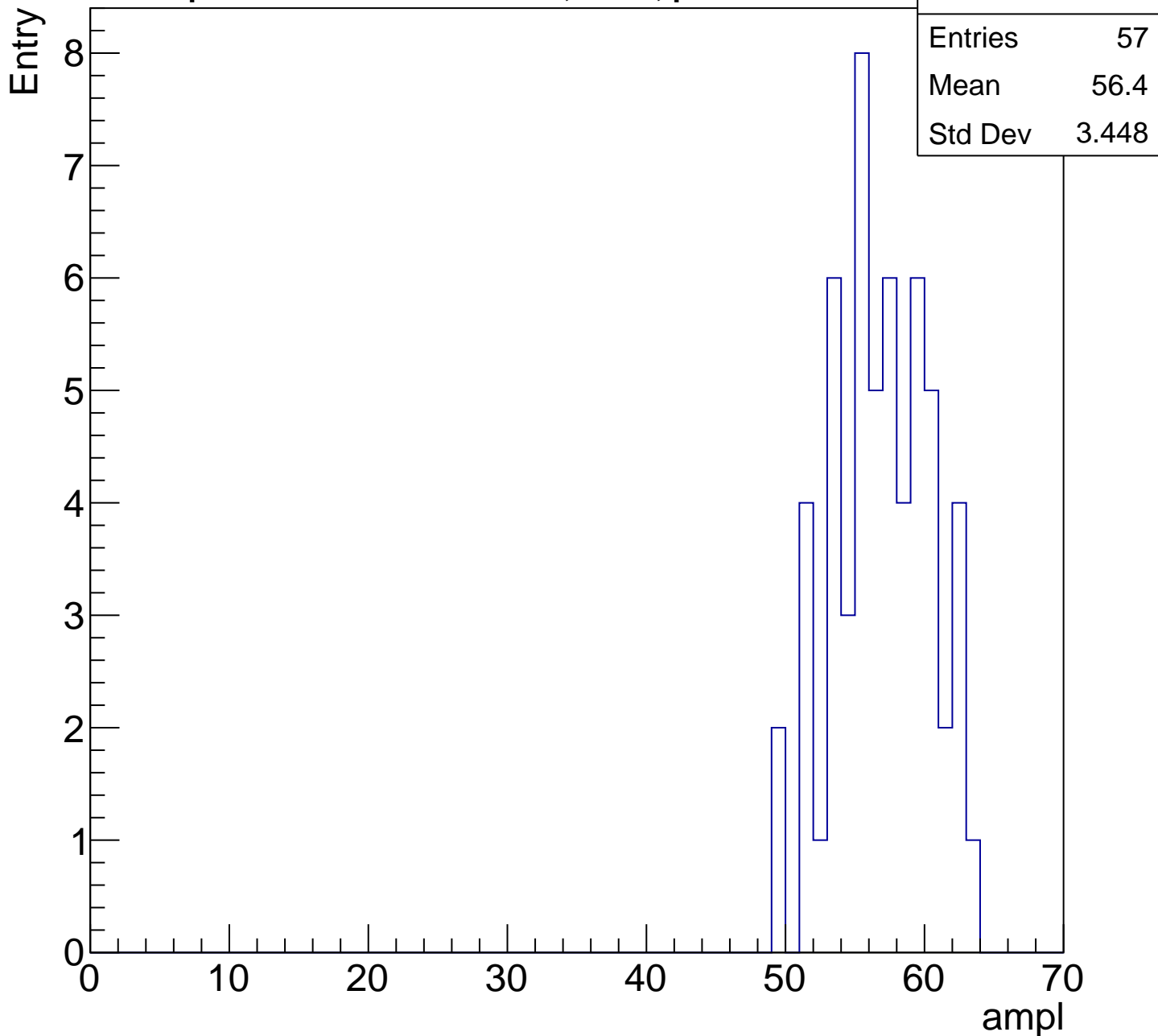
Entries	62
Mean	50.27
Std Dev	3.194

Entry



# B0L001S, U24-ch76, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

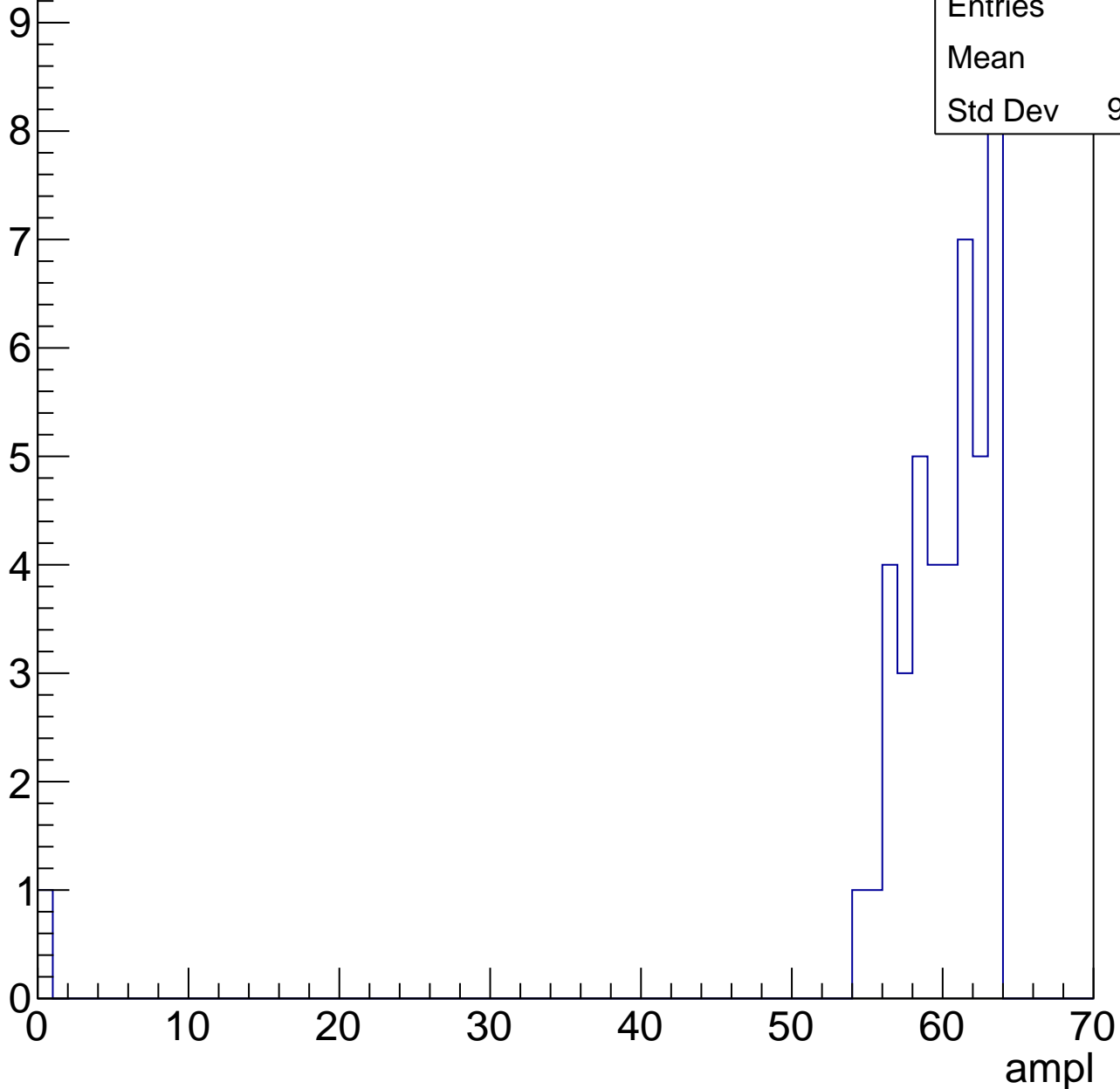


# B0L001S, U24-ch76, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	44
Mean	58.5
Std Dev	9.275



# B0L001S, U24-ch76, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch76, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U24-ch77, adc0

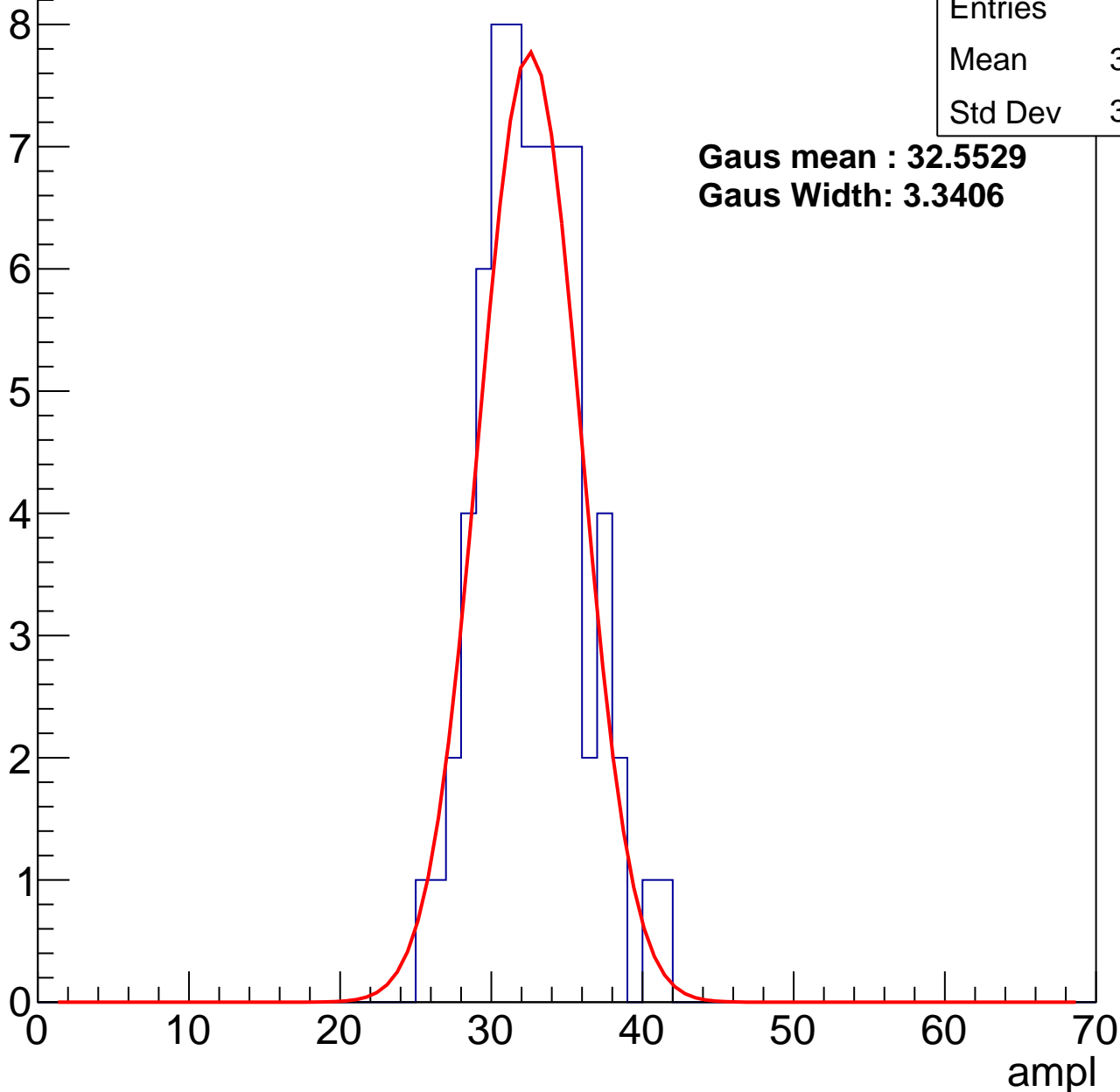
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	32.26
Std Dev	3.288

**Gaus mean : 32.5529**

**Gaus Width: 3.3406**



# B0L001S, U24-ch77, adc1

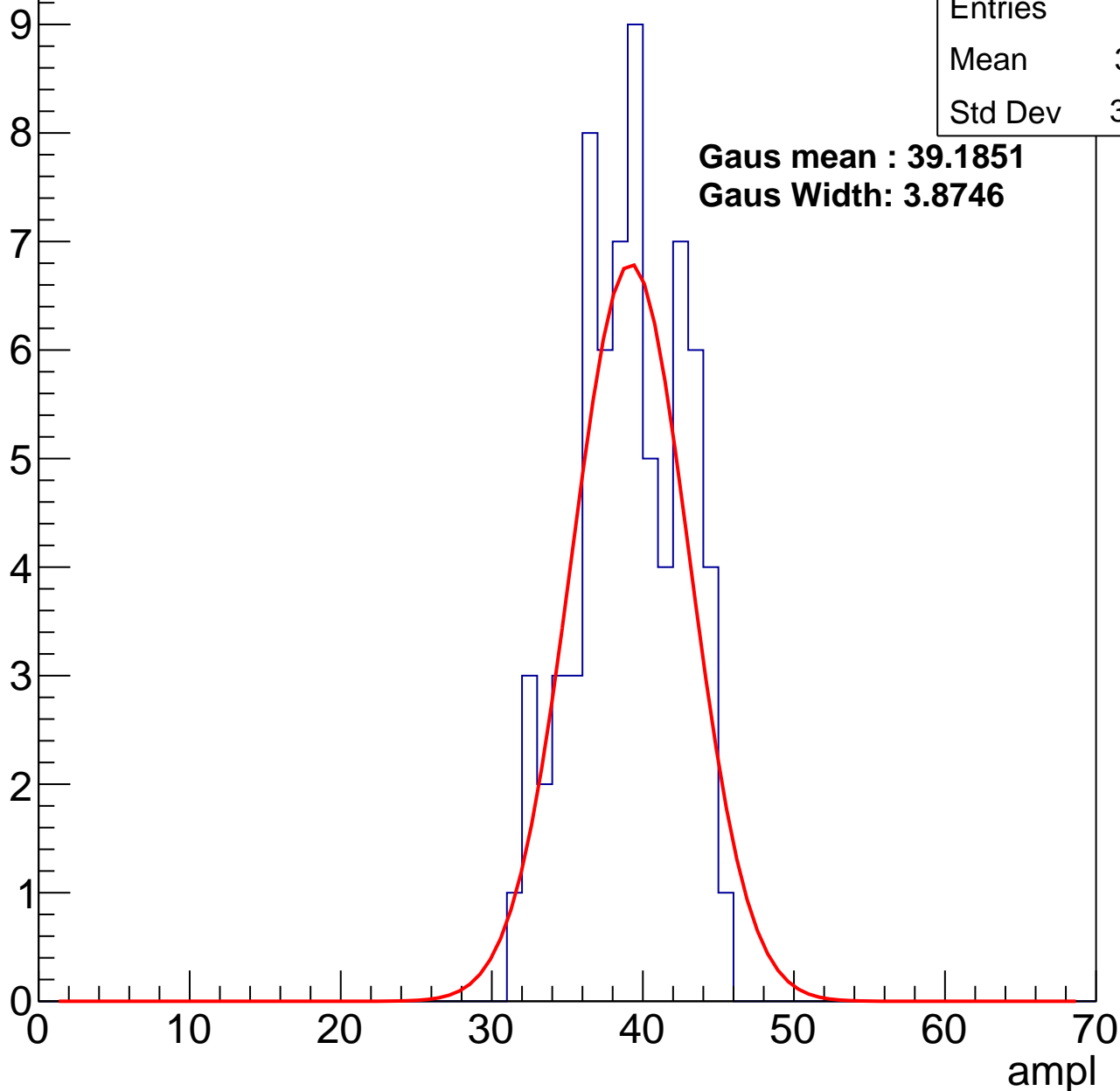
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	38.61
Std Dev	3.436

**Gaus mean : 39.1851**

**Gaus Width: 3.8746**



# B0L001S, U24-ch77, adc2

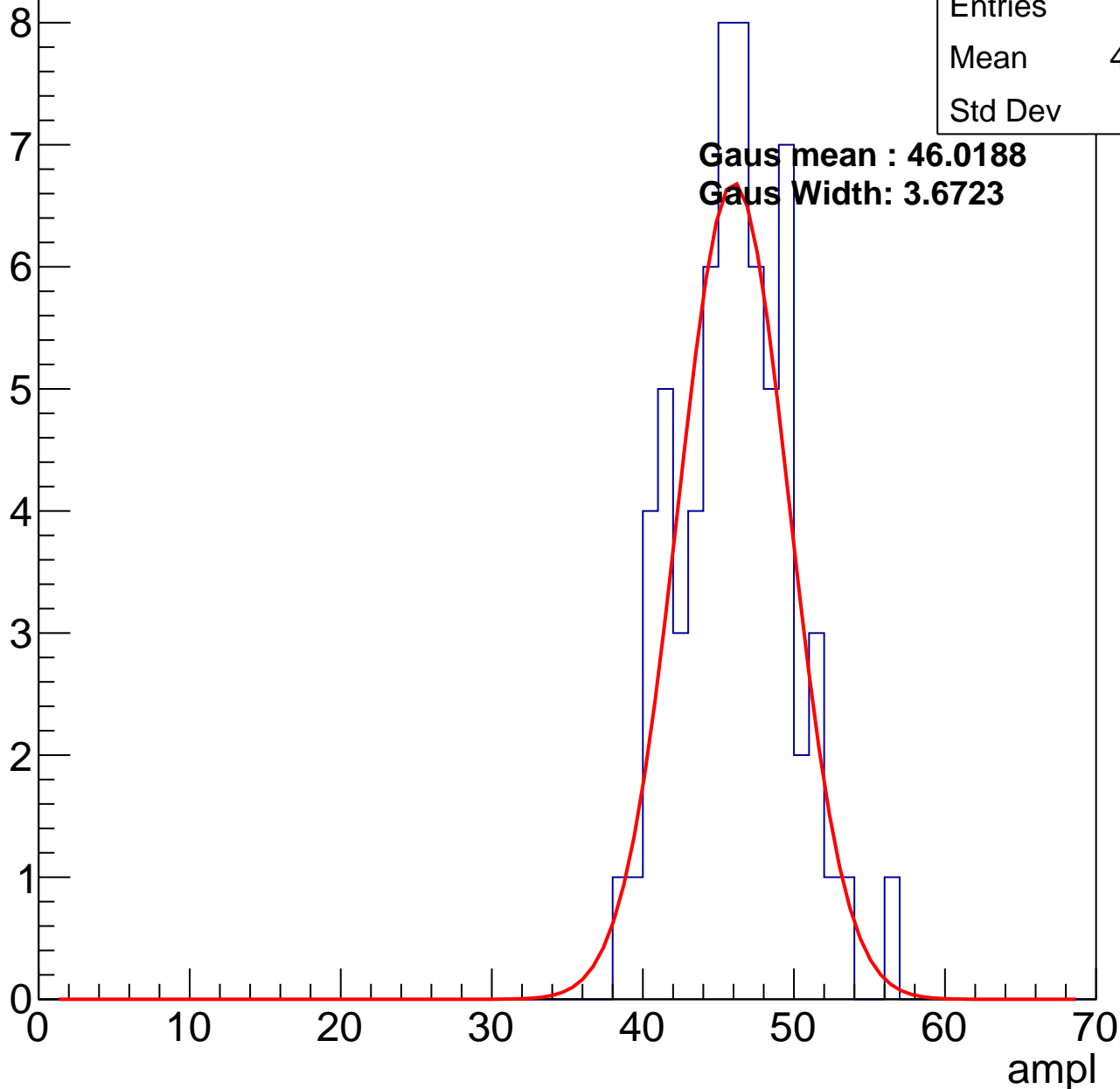
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	45.62
Std Dev	3.63

Gaus mean : 46.0188

Gaus Width: 3.6723

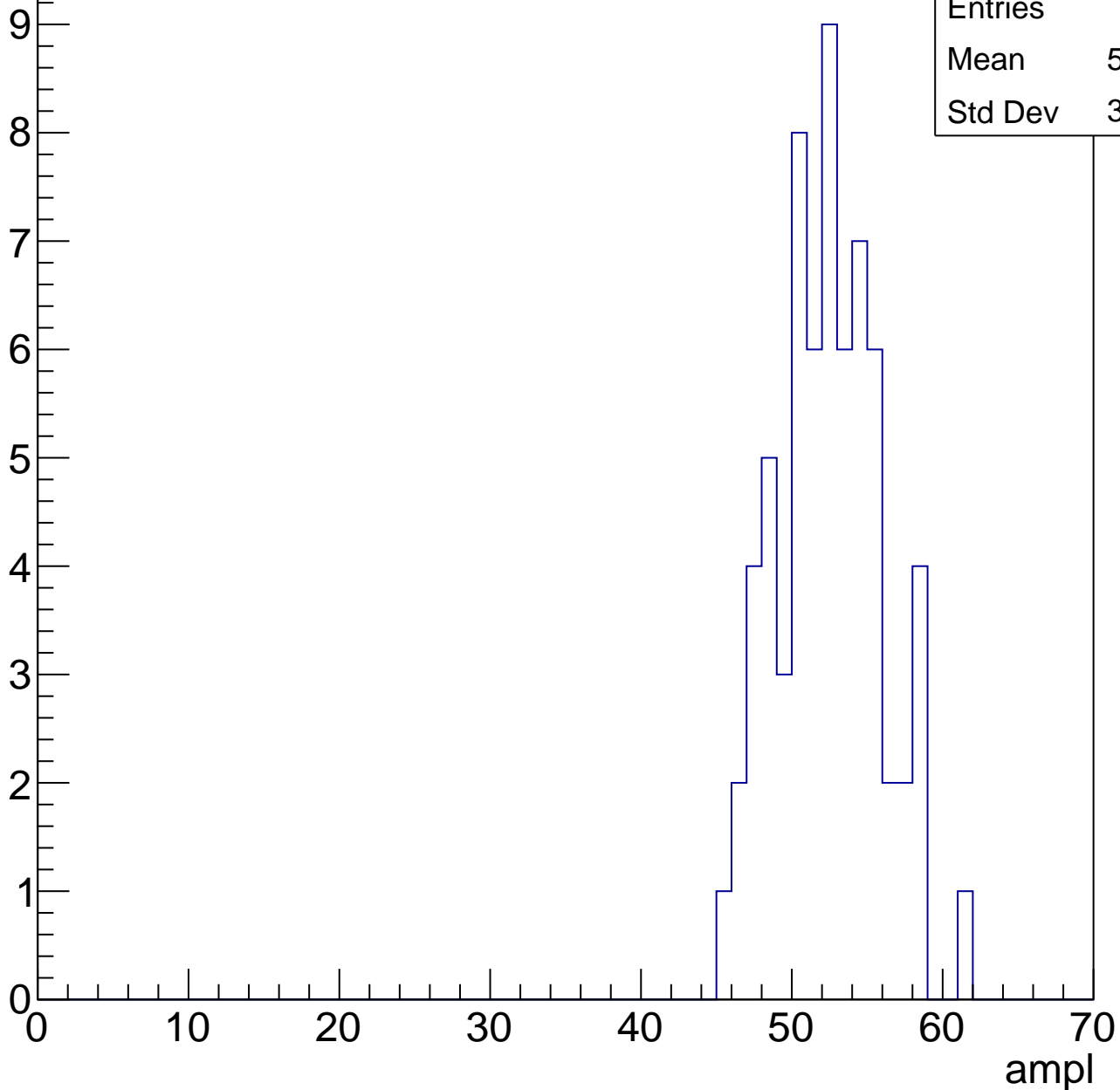


# B0L001S, U24-ch77, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

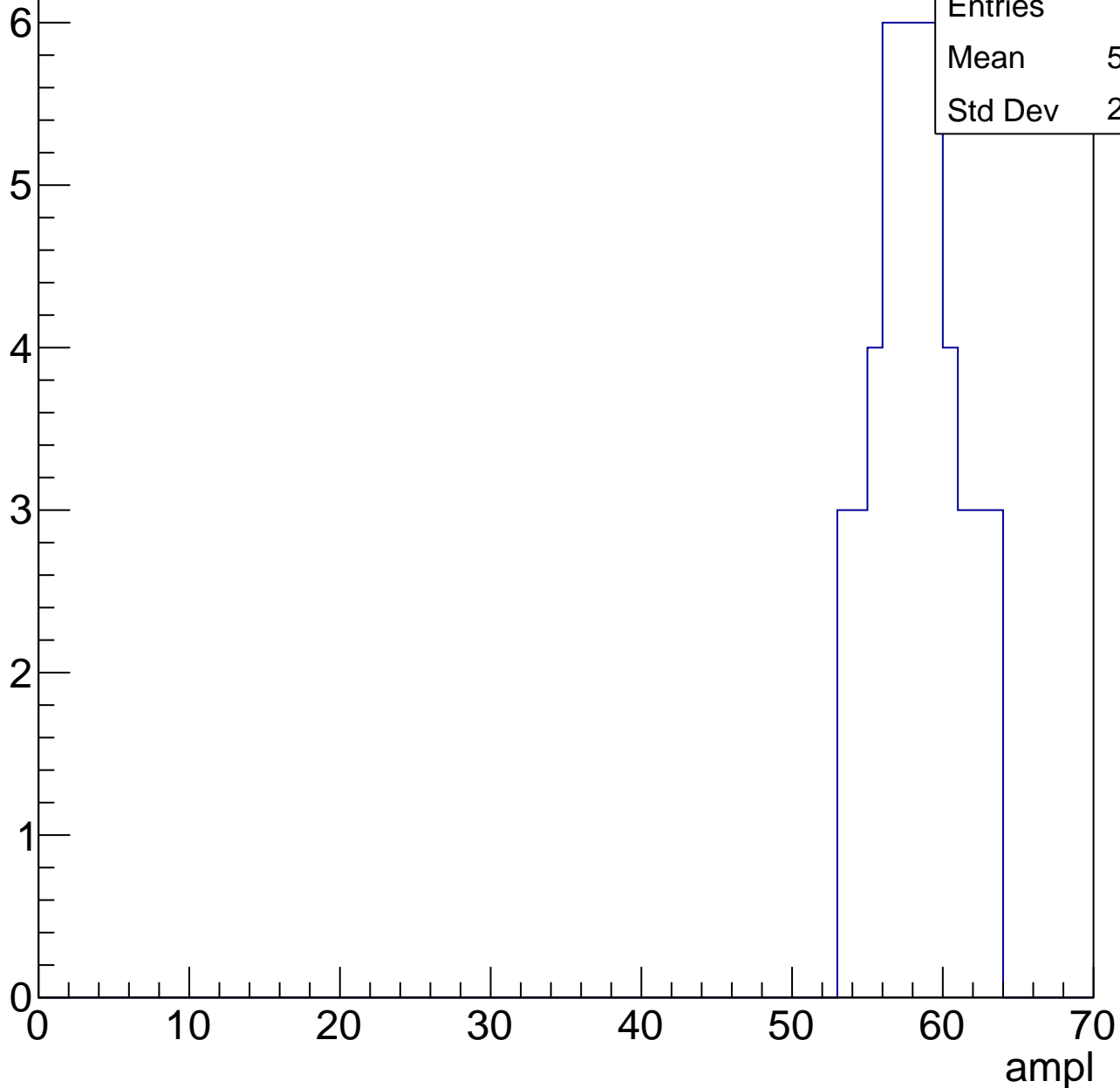
Entries	66
Mean	51.98
Std Dev	3.396



# B0L001S, U24-ch77, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

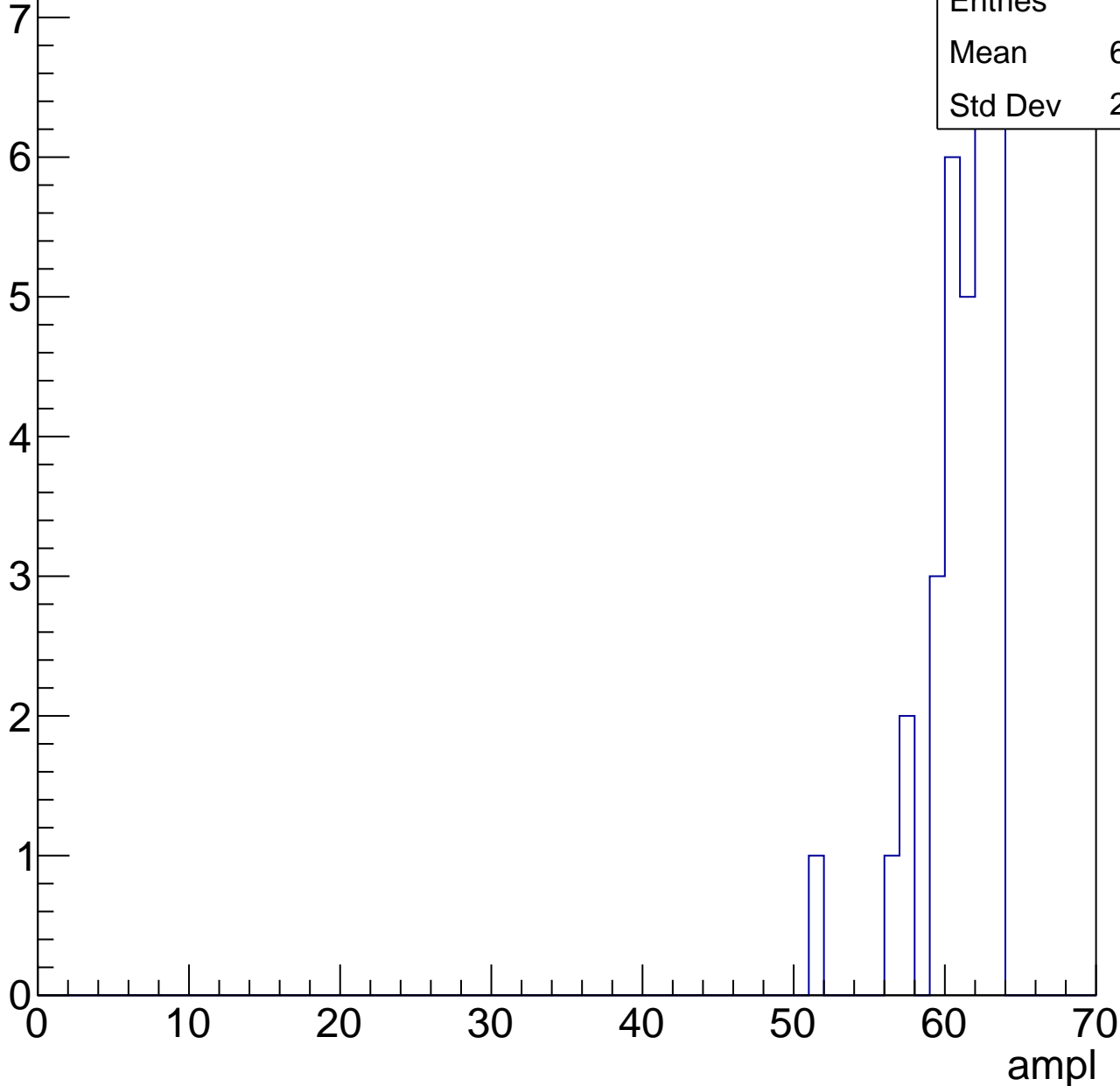


# B0L001S, U24-ch77, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

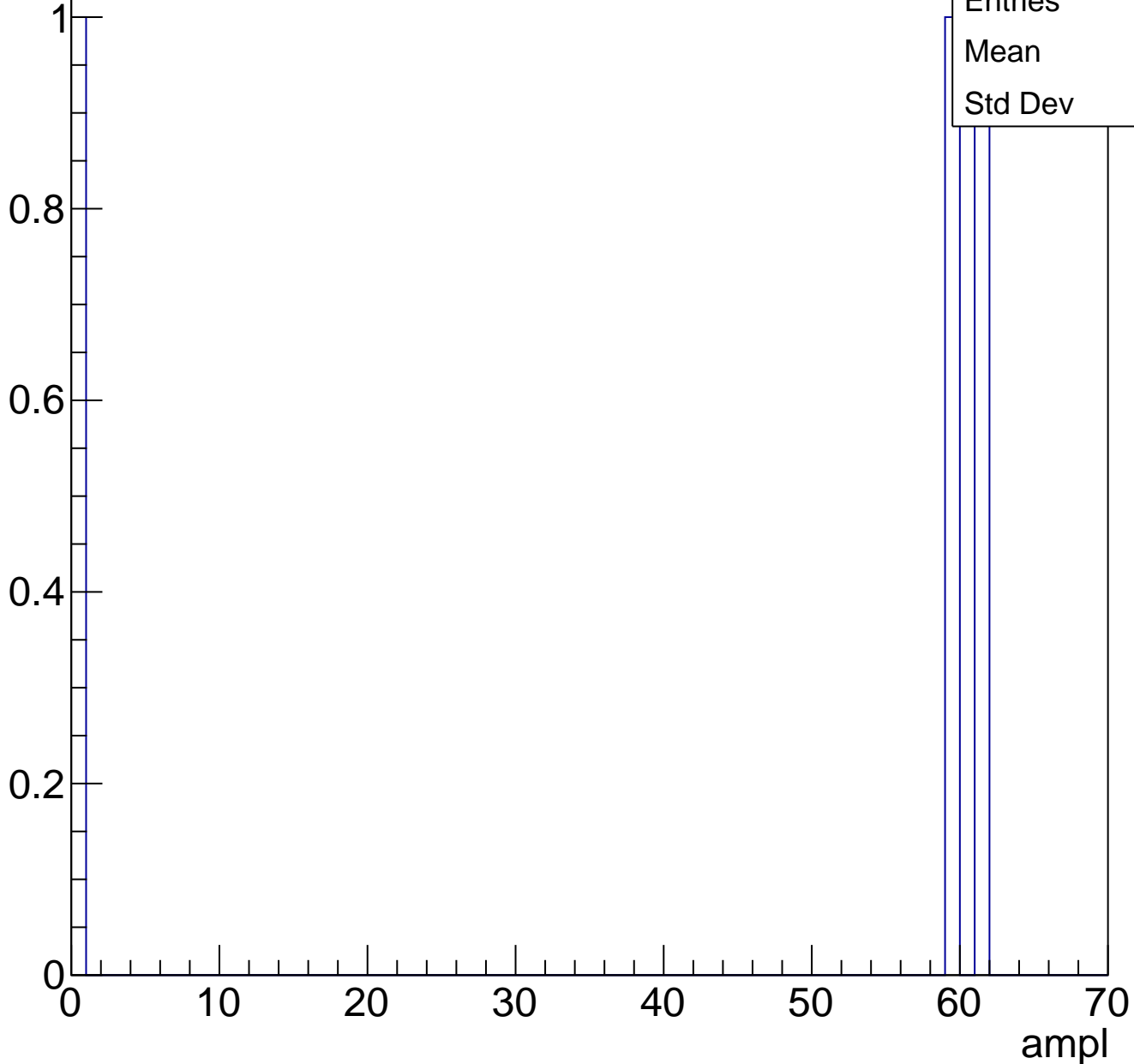
Entries	32
Mean	60.56
Std Dev	2.524



# B0L001S, U24-ch77, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch77, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U24-ch78, adc0

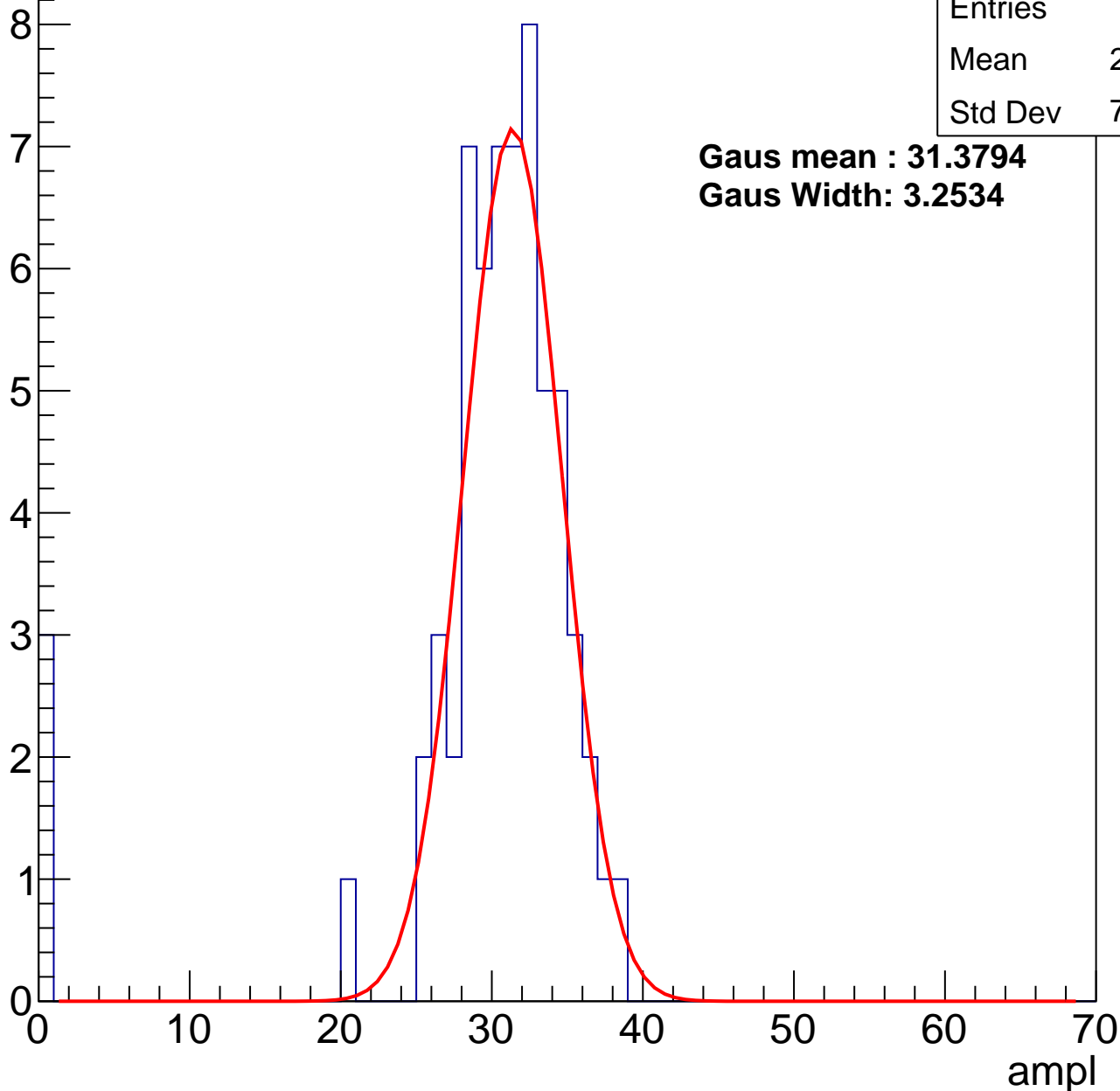
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	29.24
Std Dev	7.278

**Gaus mean : 31.3794**

**Gaus Width: 3.2534**



# B0L001S, U24-ch78, adc1

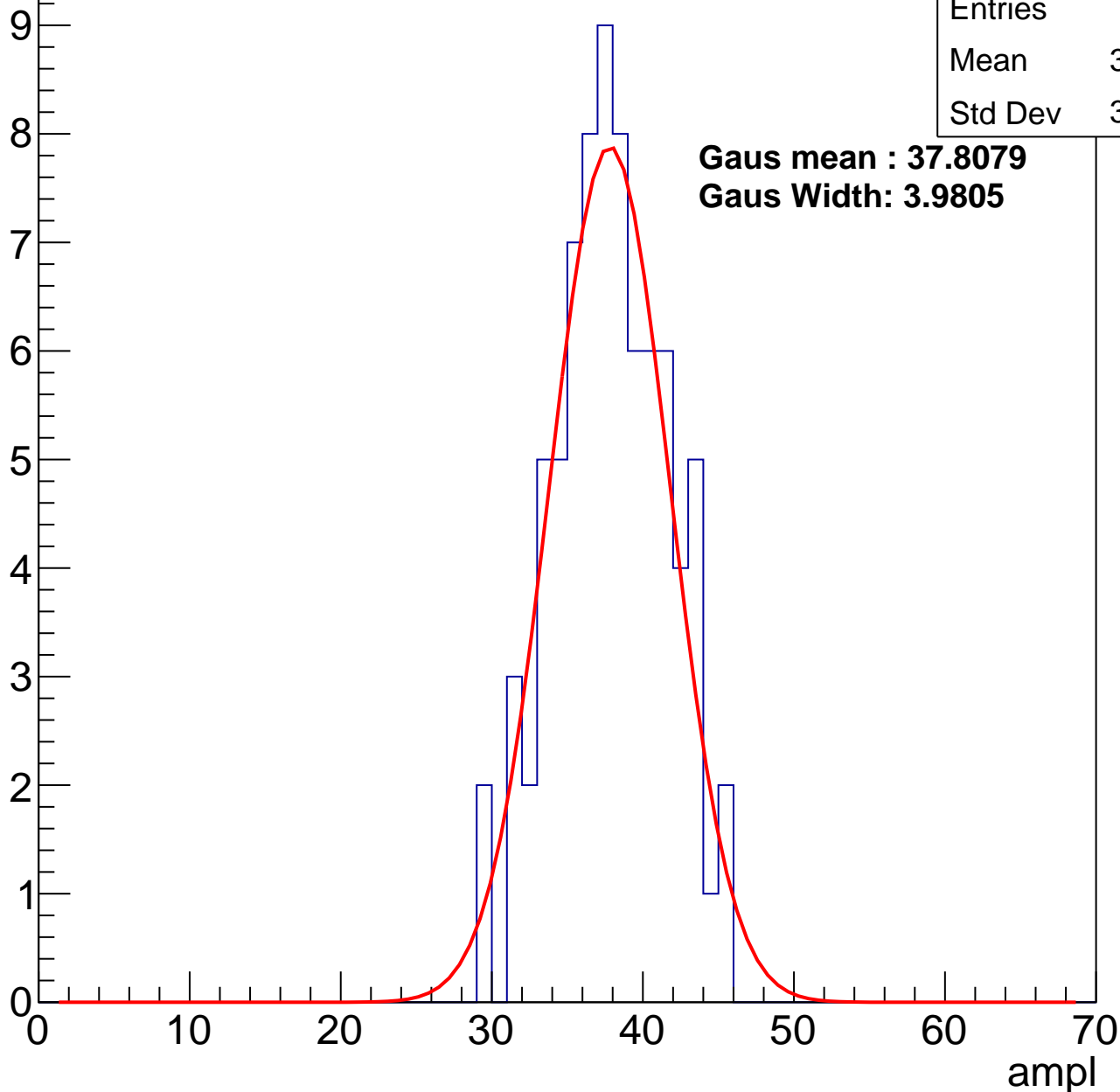
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	79
Mean	37.43
Std Dev	3.683

**Gaus mean : 37.8079**

**Gaus Width: 3.9805**



# B0L001S, U24-ch78, adc2

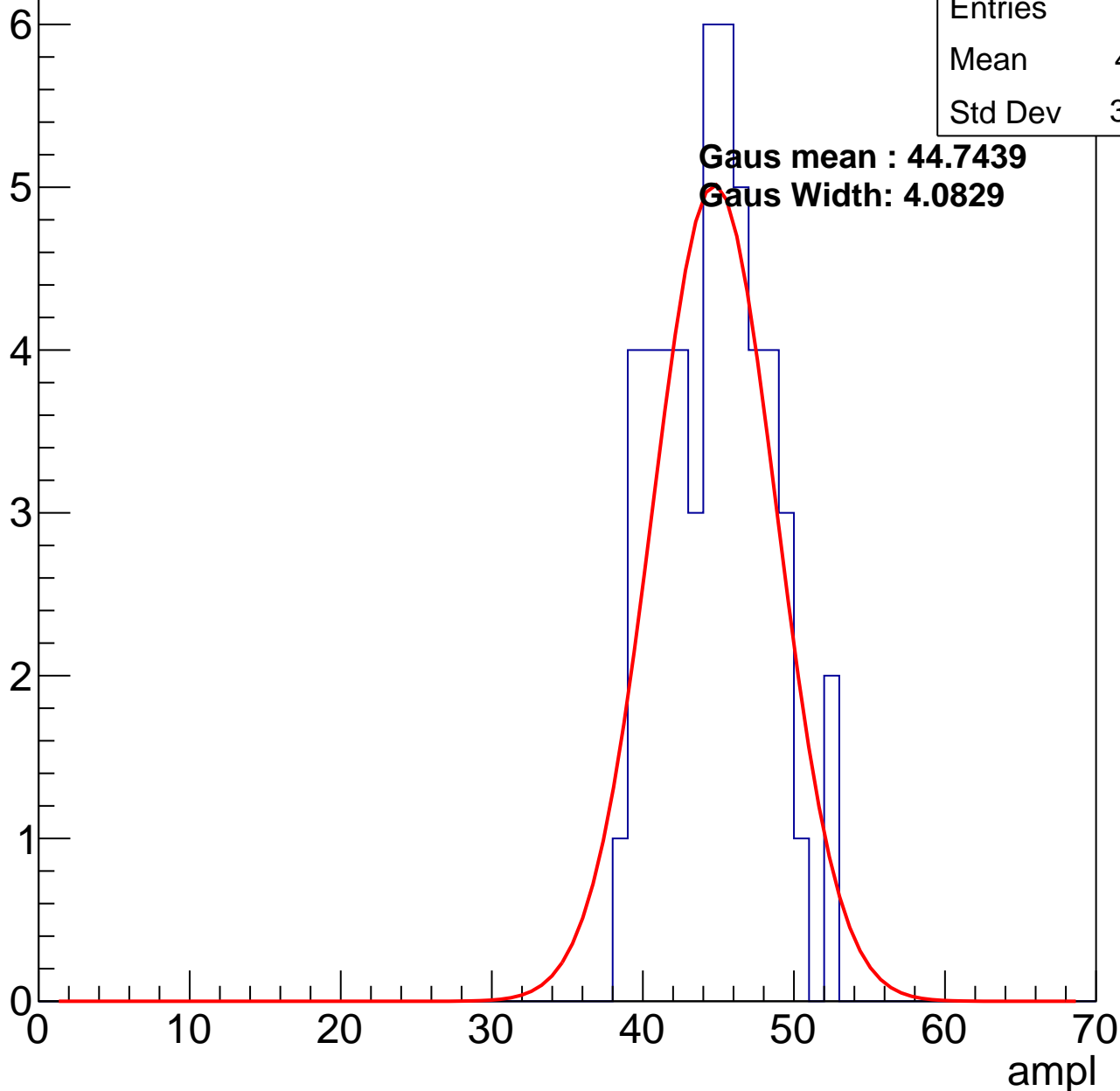
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	51
Mean	44.31
Std Dev	3.473

**Gaus mean : 44.7439**

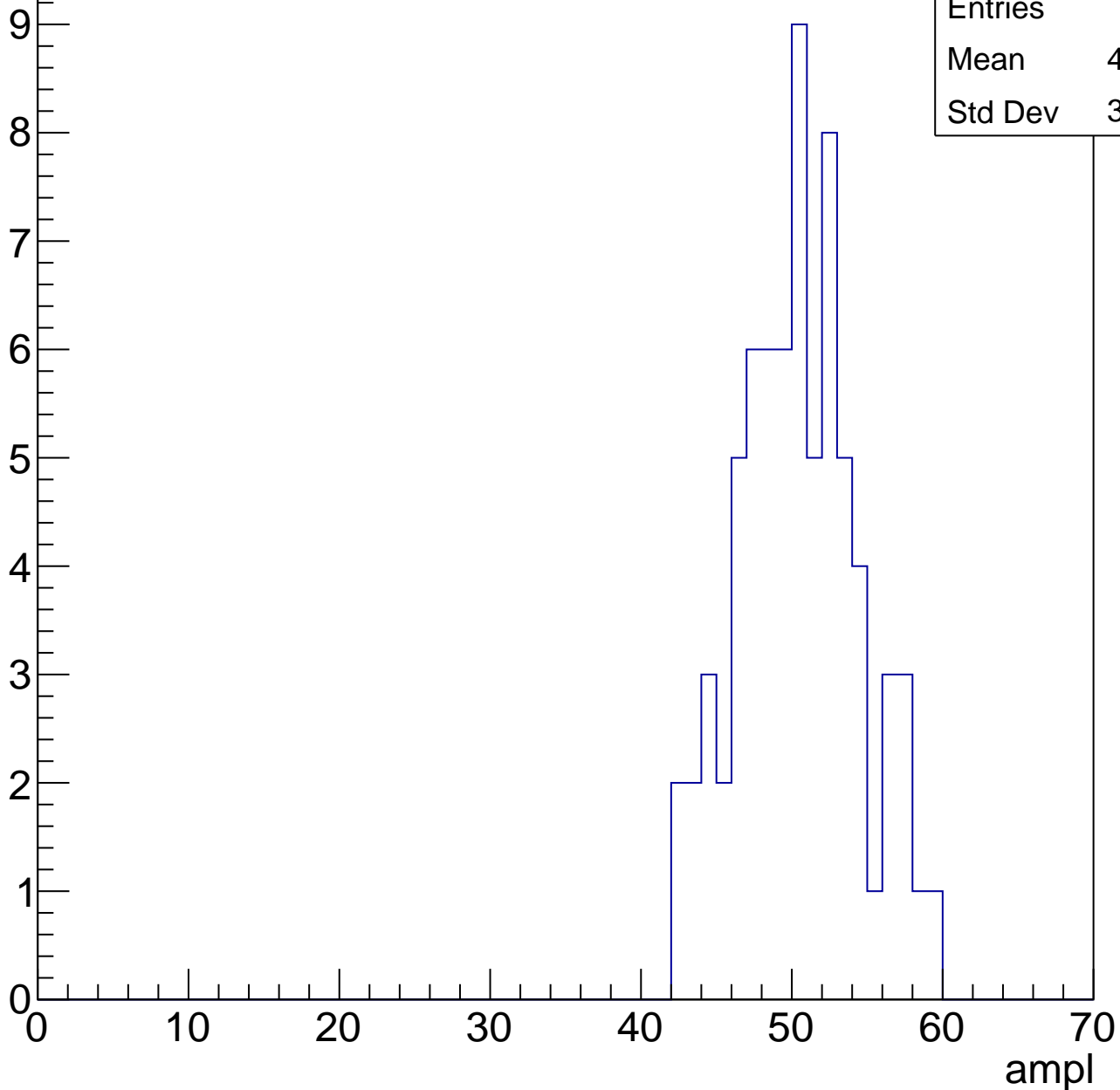
**Gaus Width: 4.0829**



# B0L001S, U24-ch78, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

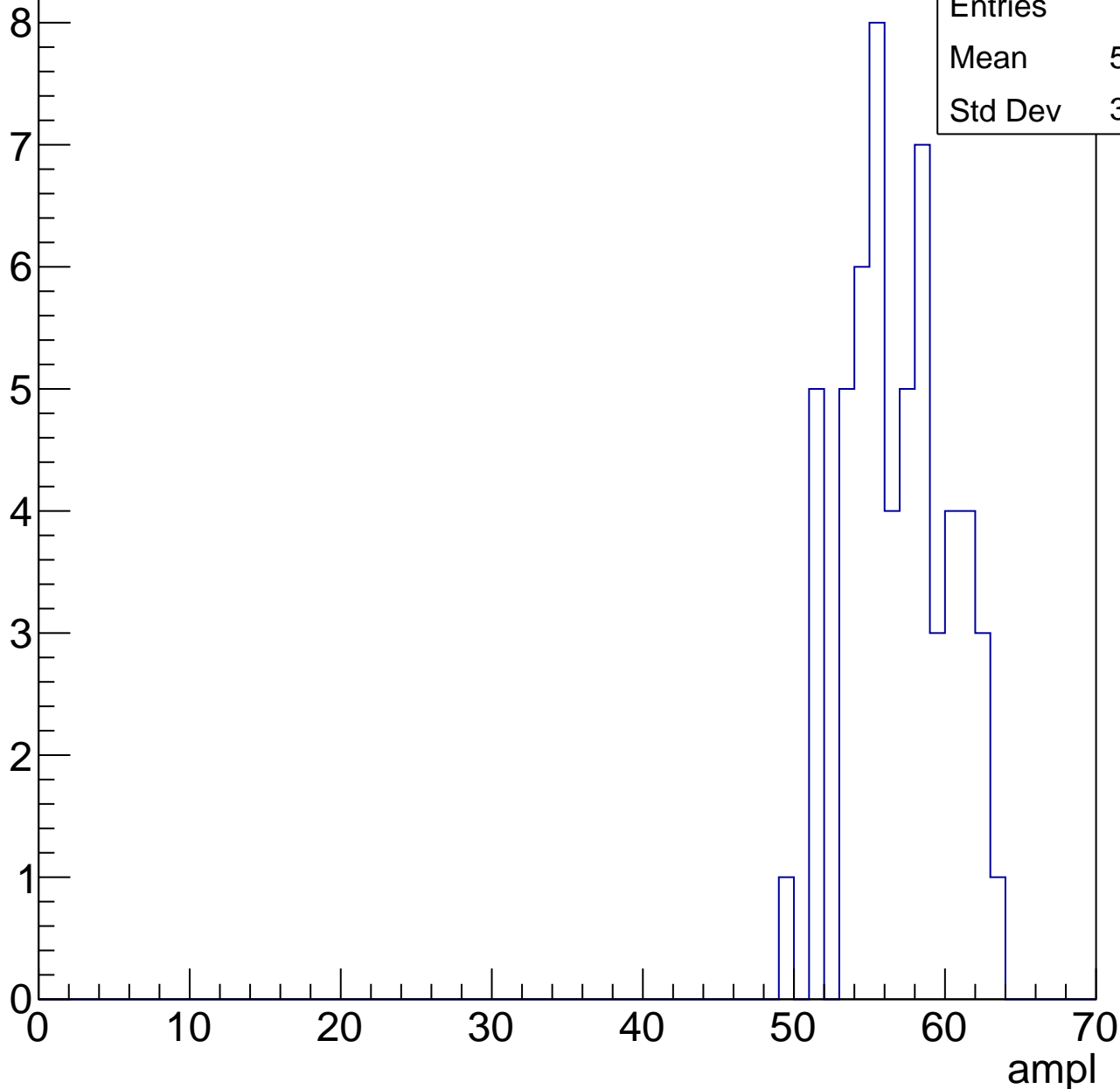


# B0L001S, U24-ch78, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	56.39
Std Dev	3.336

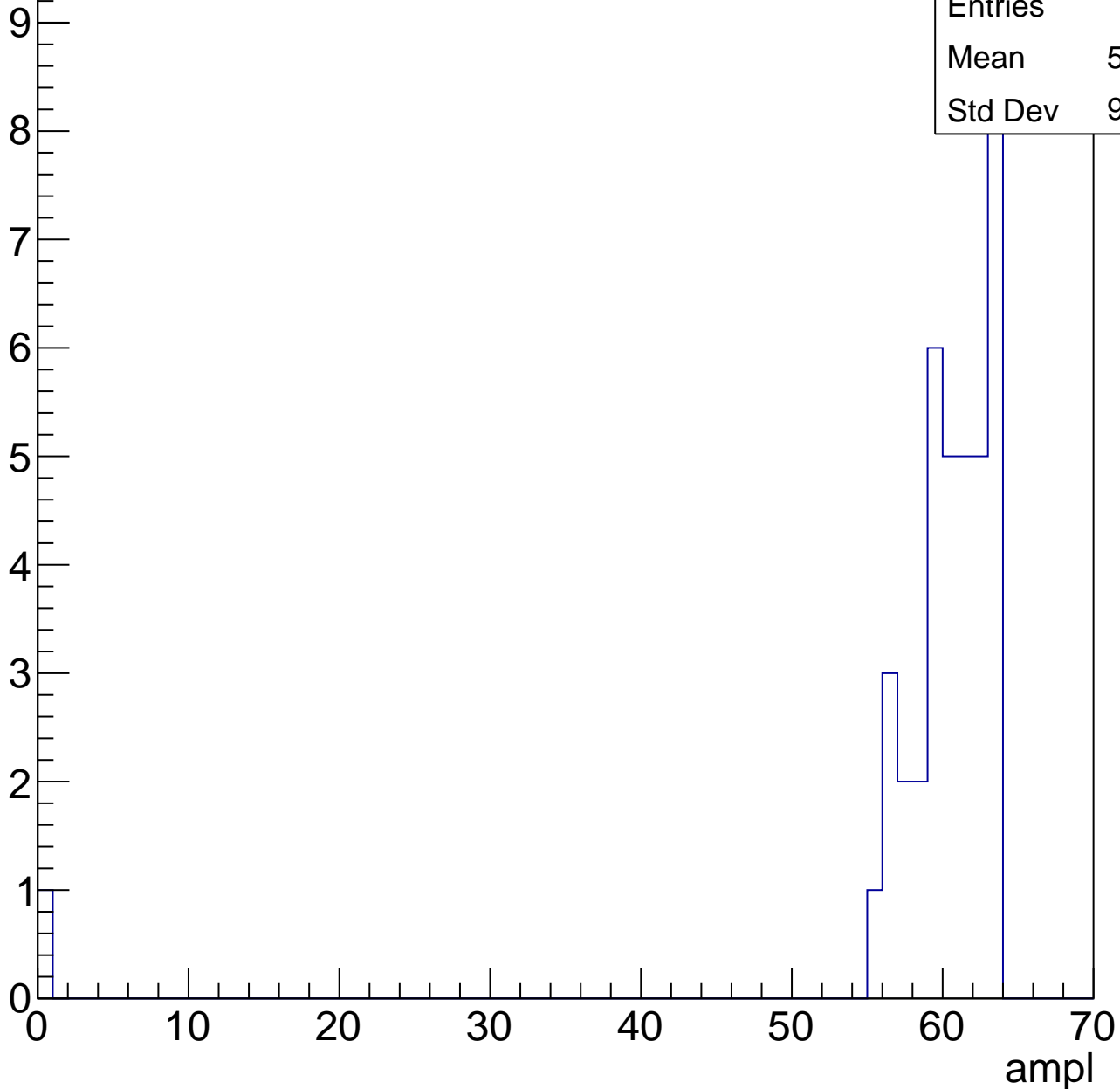


# B0L001S, U24-ch78, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	39
Mean	58.69
Std Dev	9.798



# B0L001S, U24-ch78, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

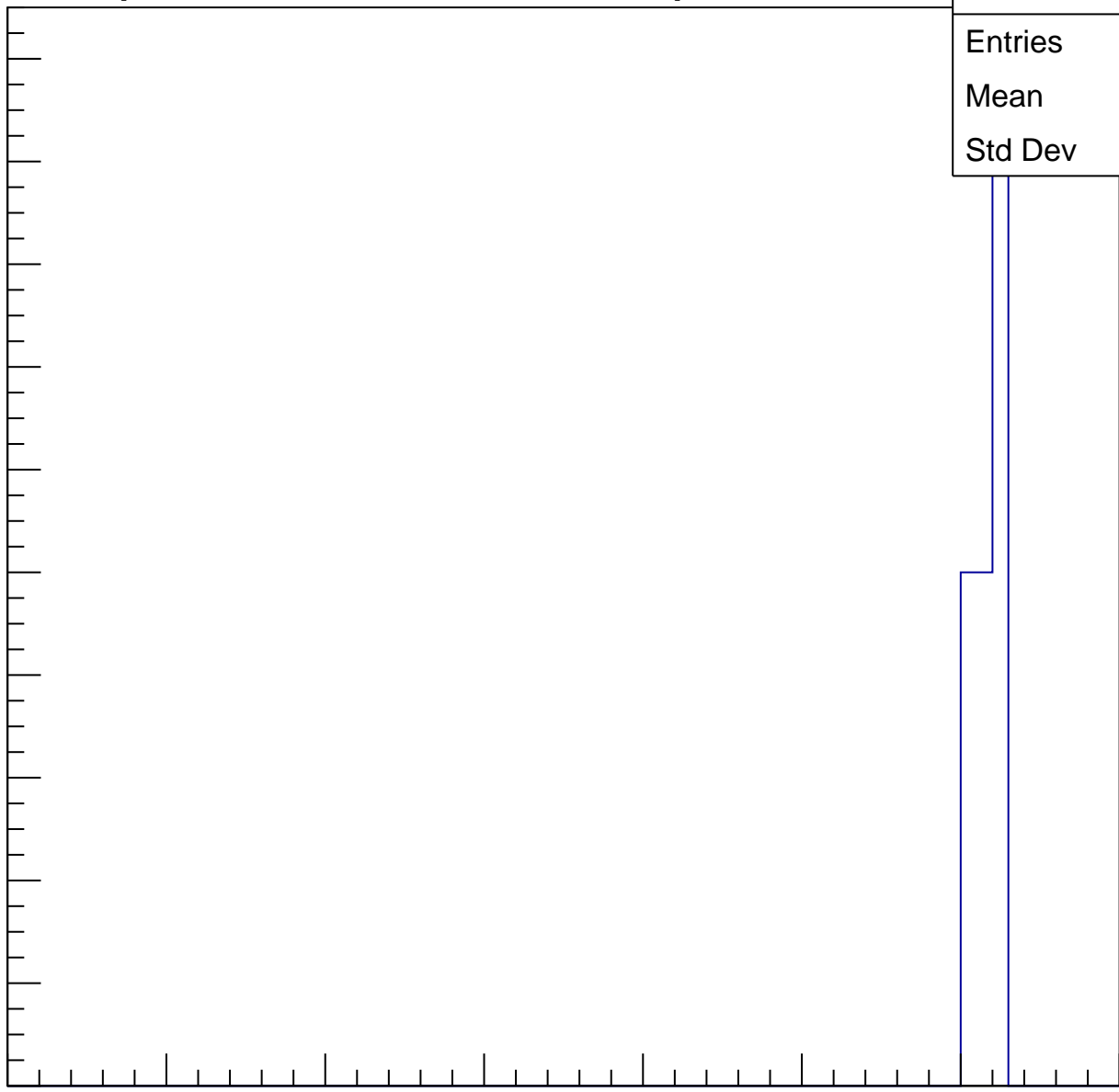
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	61.25
Std Dev	0.8292

ampl

0 10 20 30 40 50 60 70





# B0L001S, U24-ch78, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U24-ch79, adc0

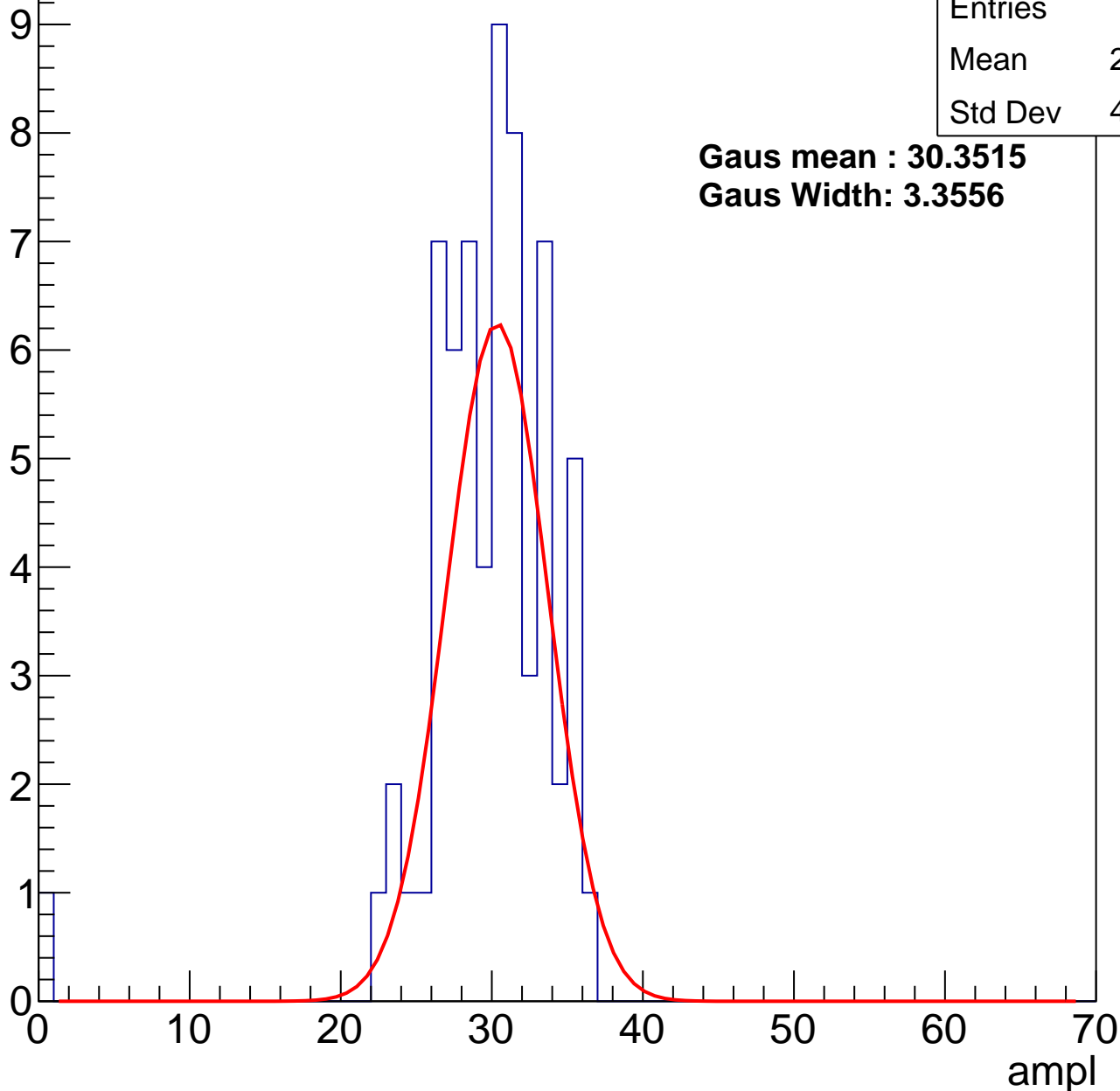
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	29.18
Std Dev	4.889

**Gaus mean : 30.3515**

**Gaus Width: 3.3556**



# B0L001S, U24-ch79, adc1

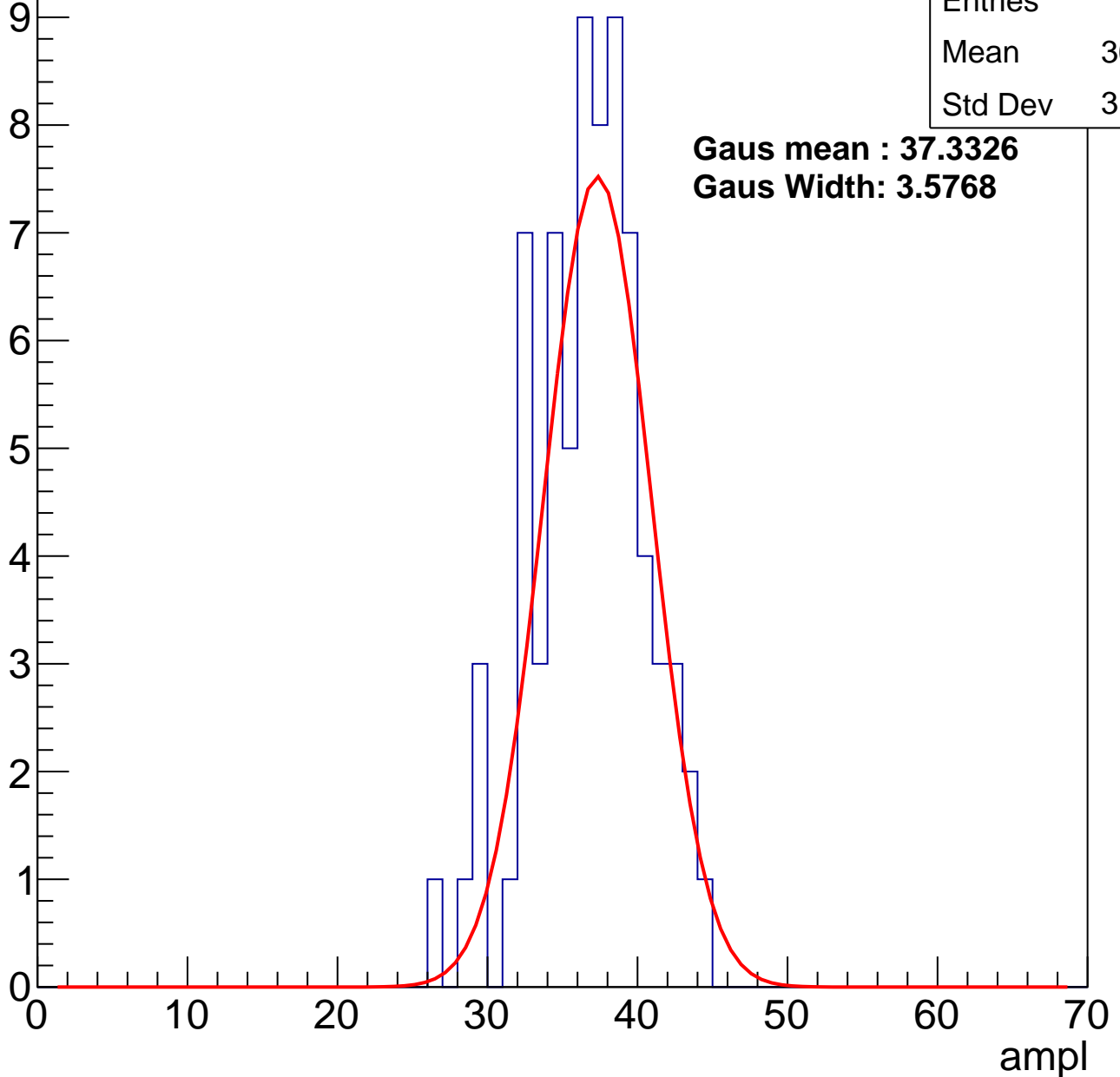
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	36.24
Std Dev	3.712

**Gaus mean : 37.3326**

**Gaus Width: 3.5768**



# B0L001S, U24-ch79, adc2

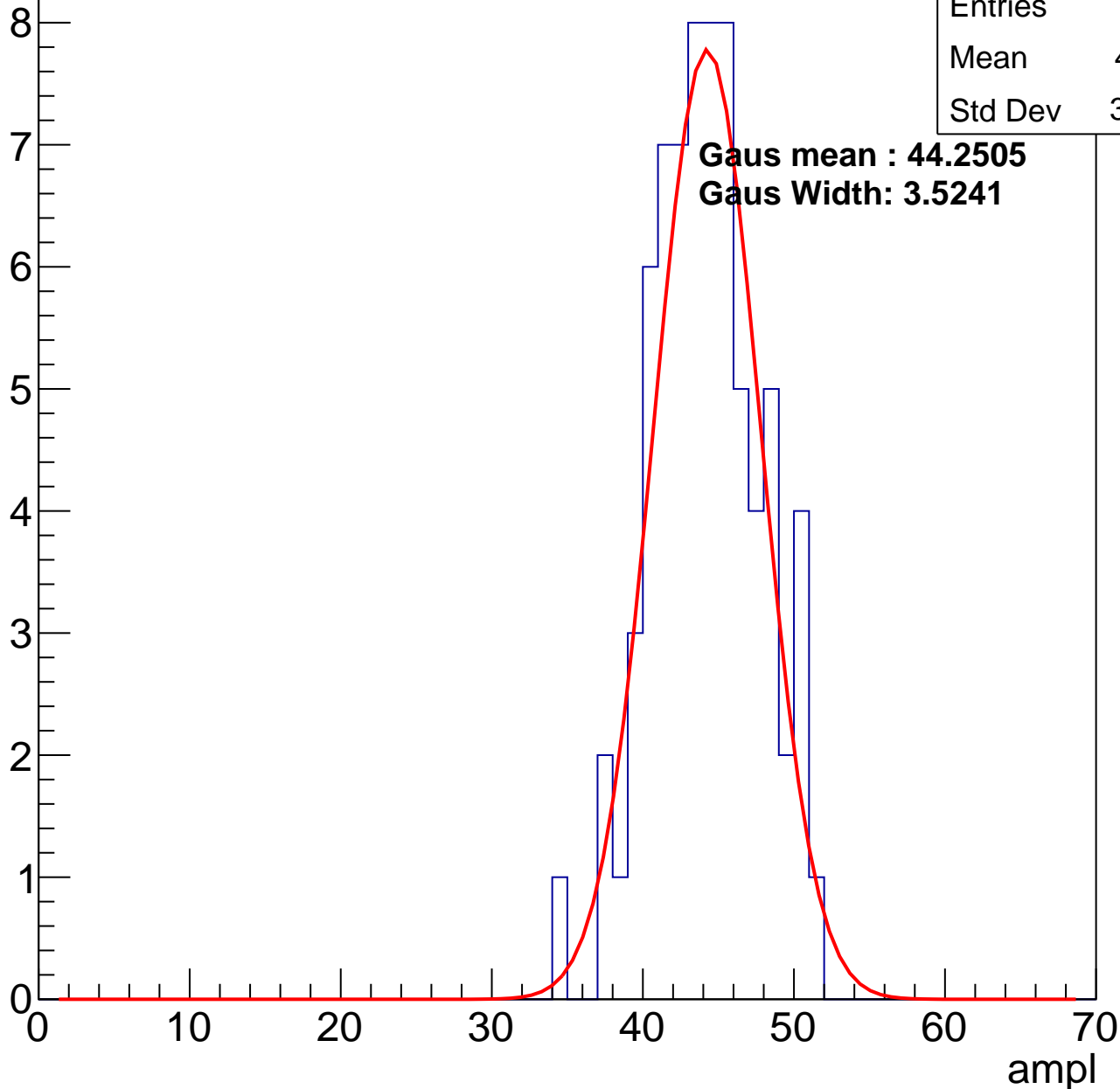
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	43.71
Std Dev	3.506

**Gaus mean : 44.2505**

**Gaus Width: 3.5241**

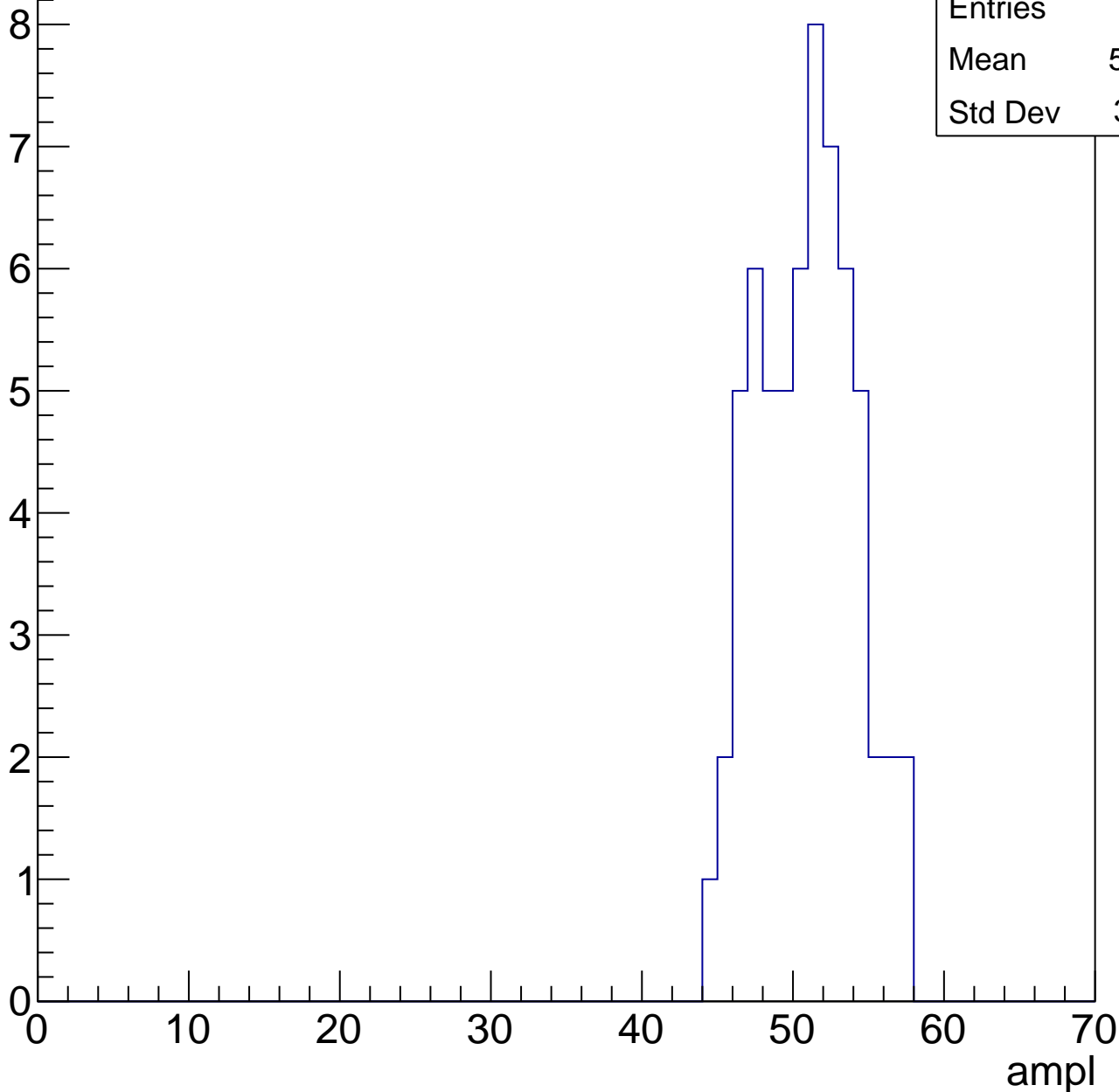


# B0L001S, U24-ch79, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	50.44
Std Dev	3.171

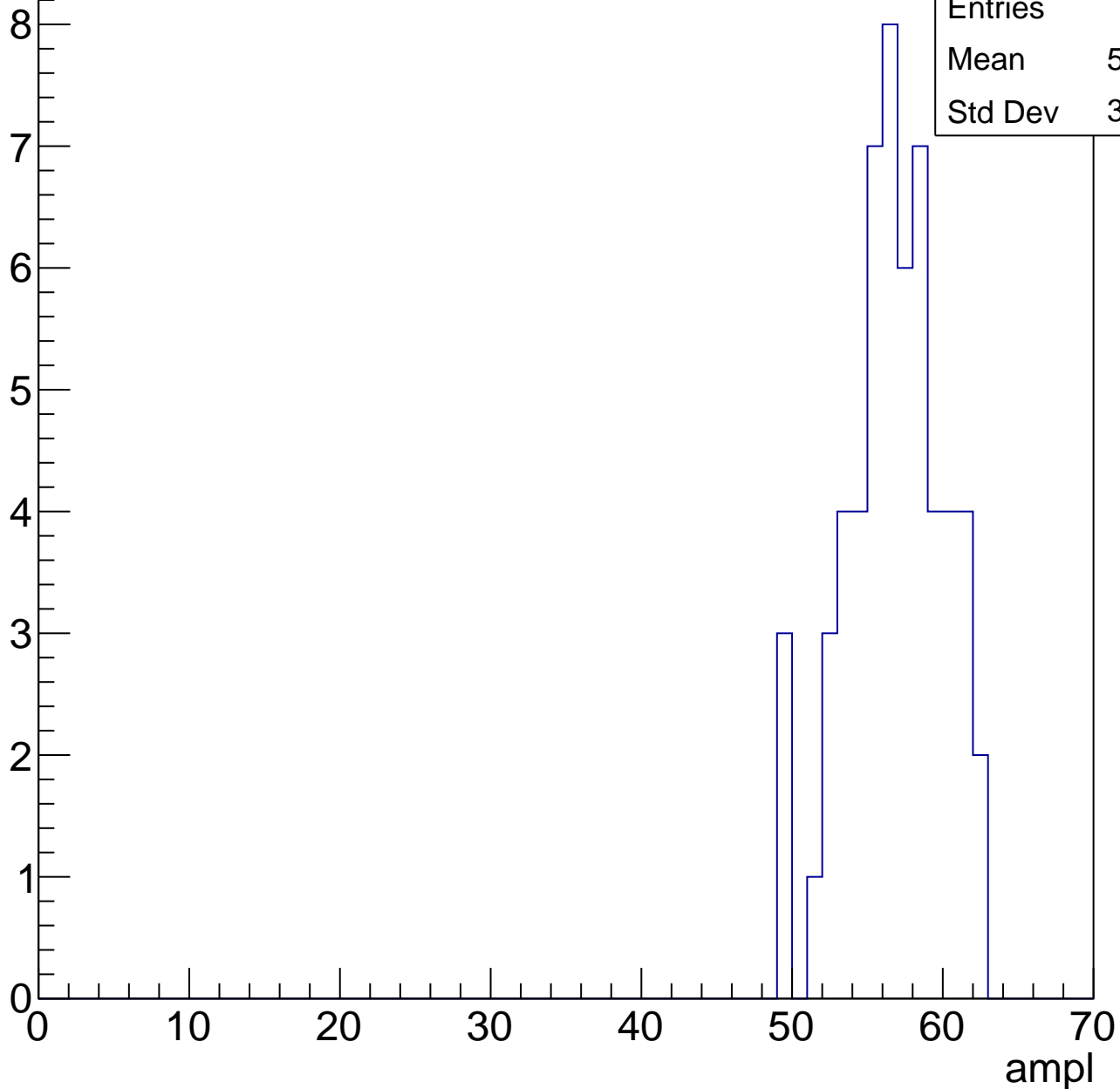


# B0L001S, U24-ch79, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	56.26
Std Dev	3.193

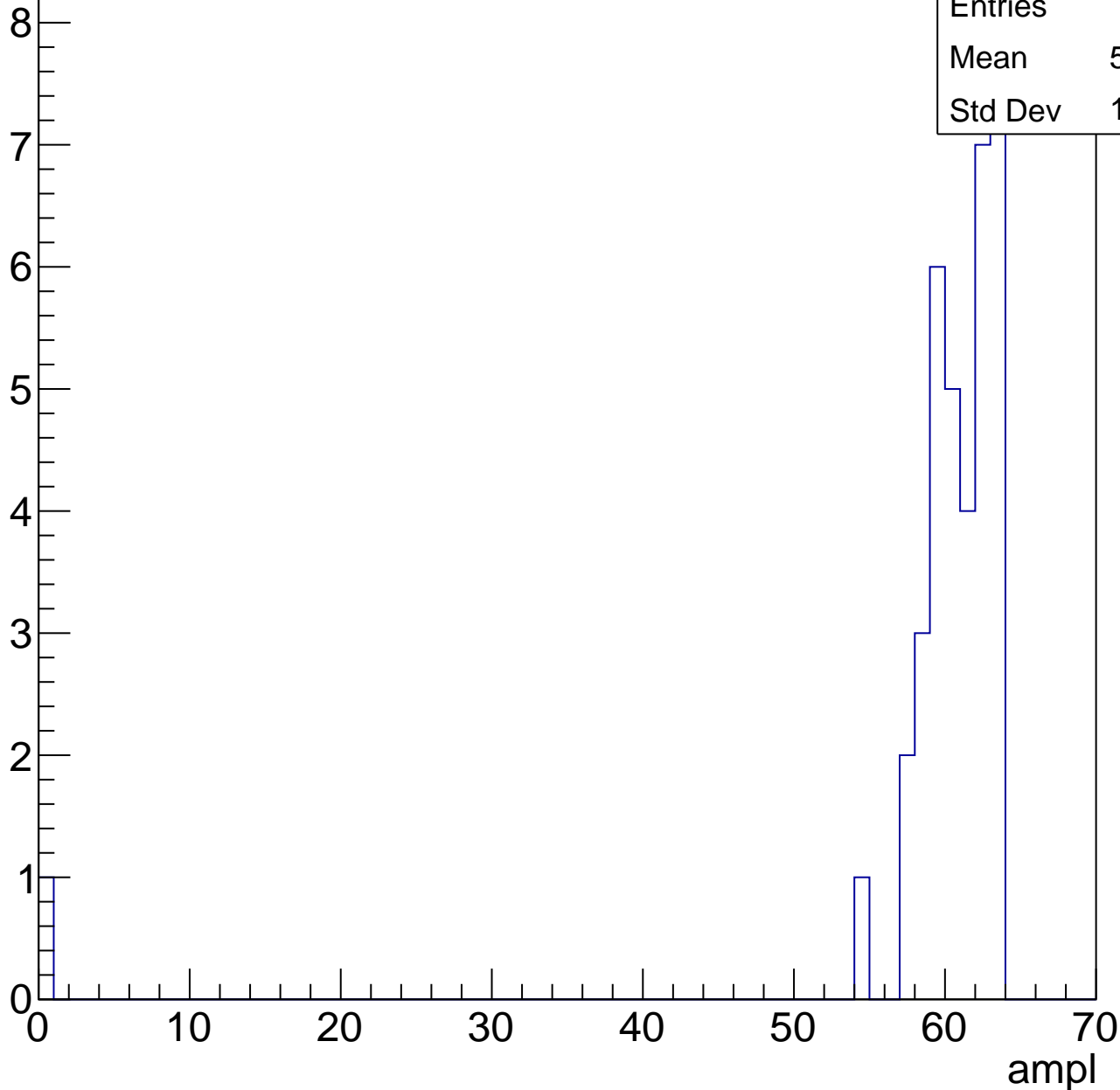


# B0L001S, U24-ch79, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

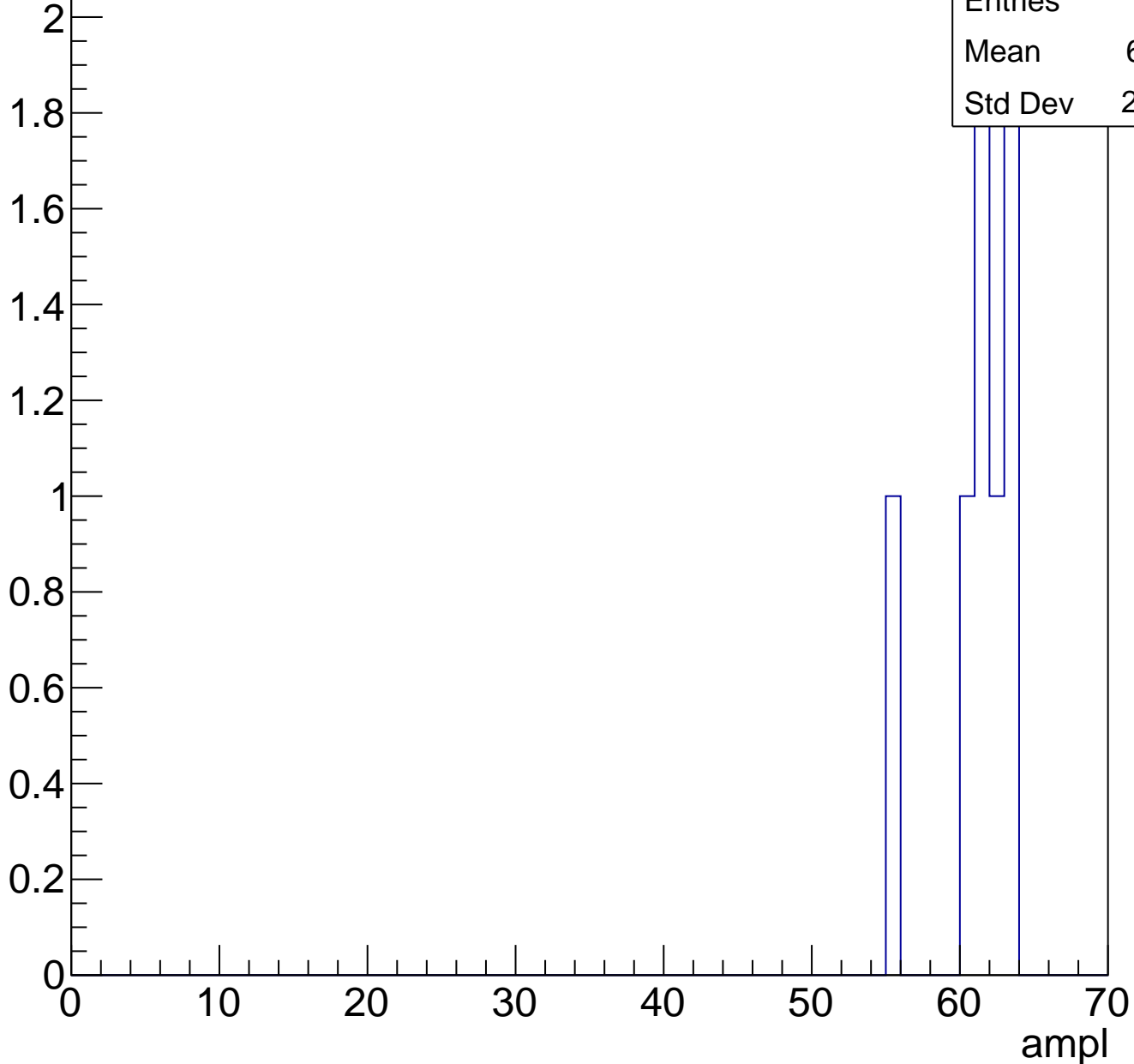
Entries	37
Mean	58.86
Std Dev	10.04



# B0L001S, U24-ch79, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch79, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U24-ch80, adc0

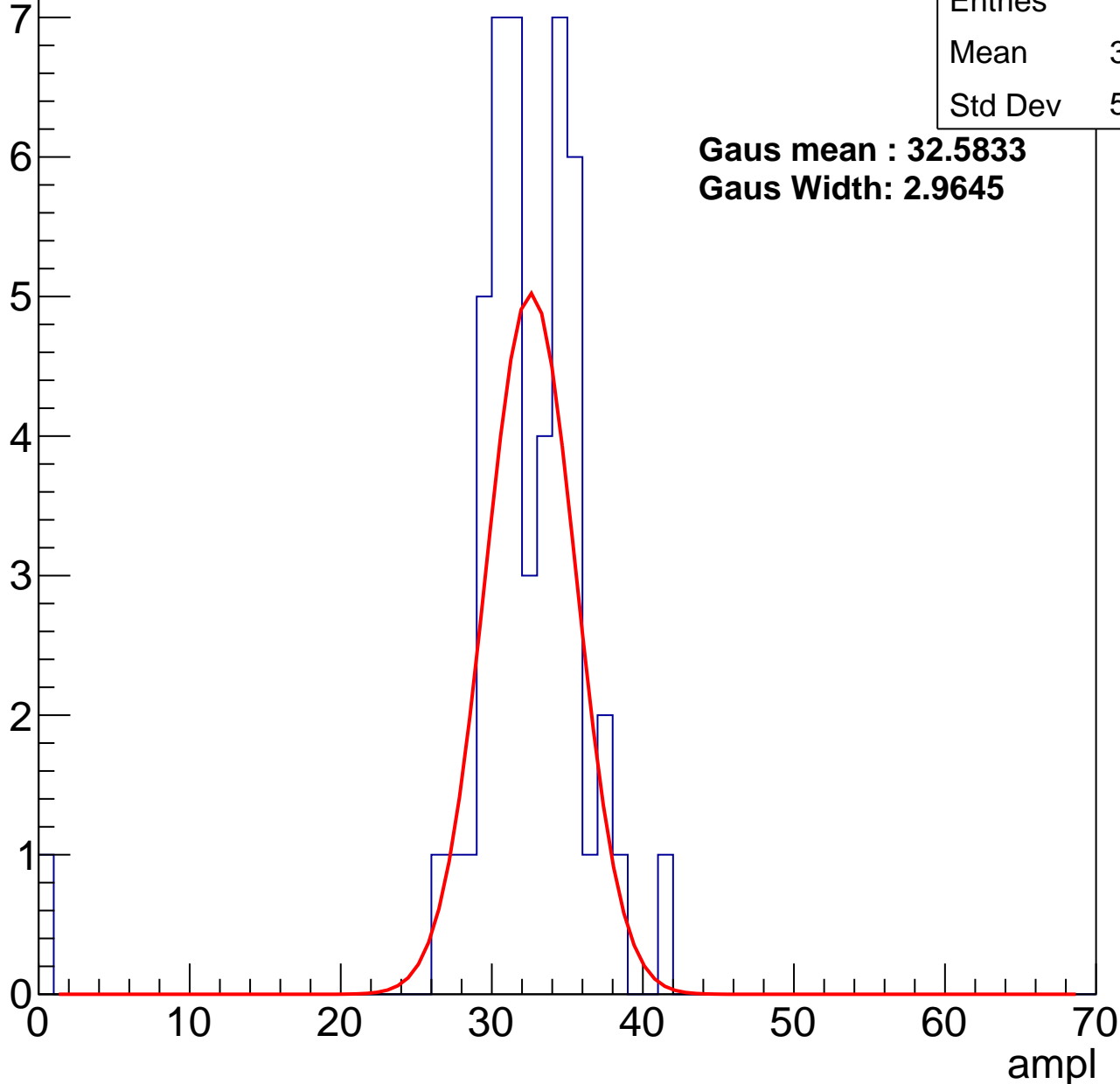
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	48
Mean	31.62
Std Dev	5.483

**Gaus mean : 32.5833**

**Gaus Width: 2.9645**



# B0L001S, U24-ch80, adc1

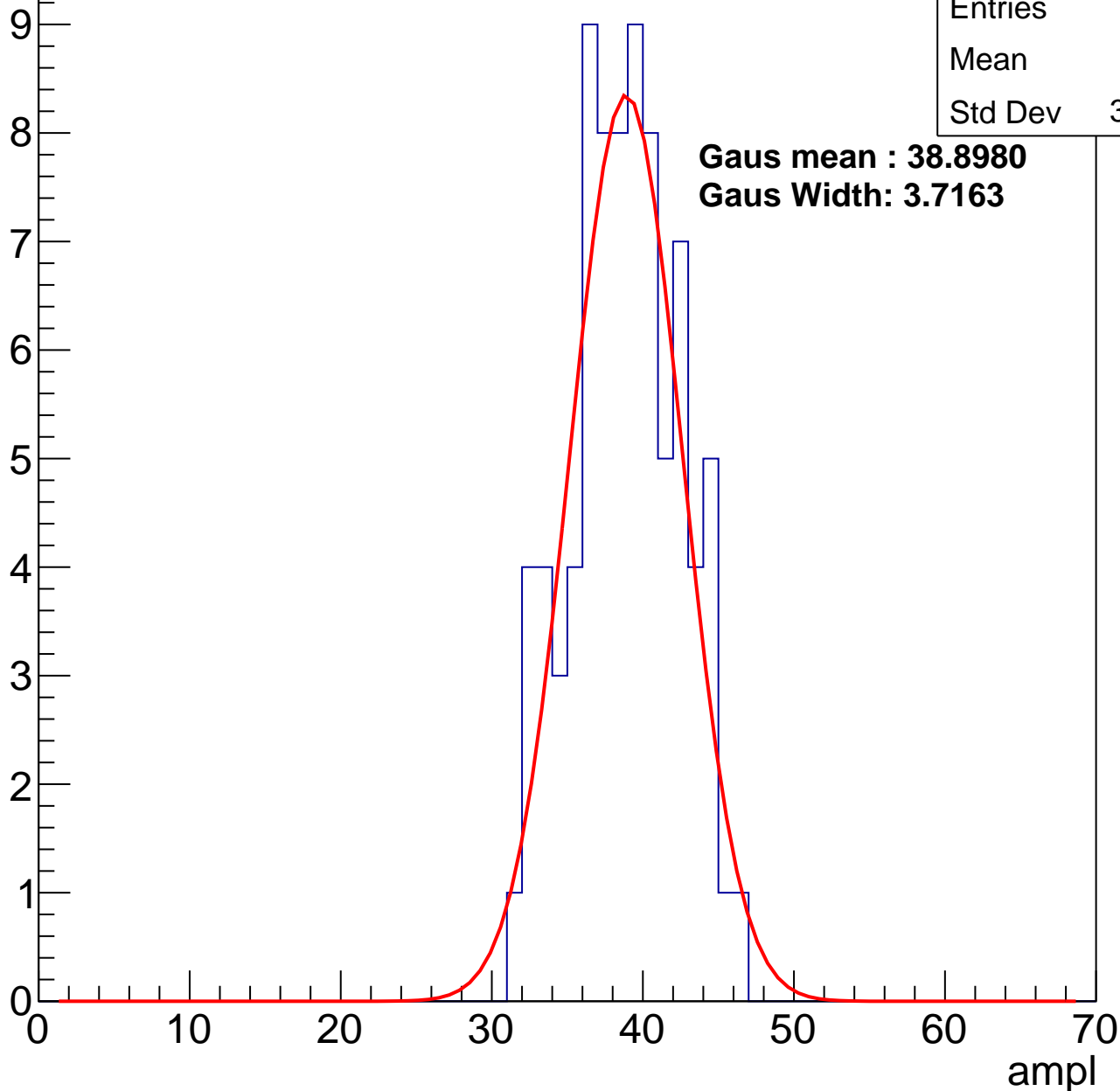
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	81
Mean	38.4
Std Dev	3.513

**Gaus mean : 38.8980**

**Gaus Width: 3.7163**



# B0L001S, U24-ch80, adc2

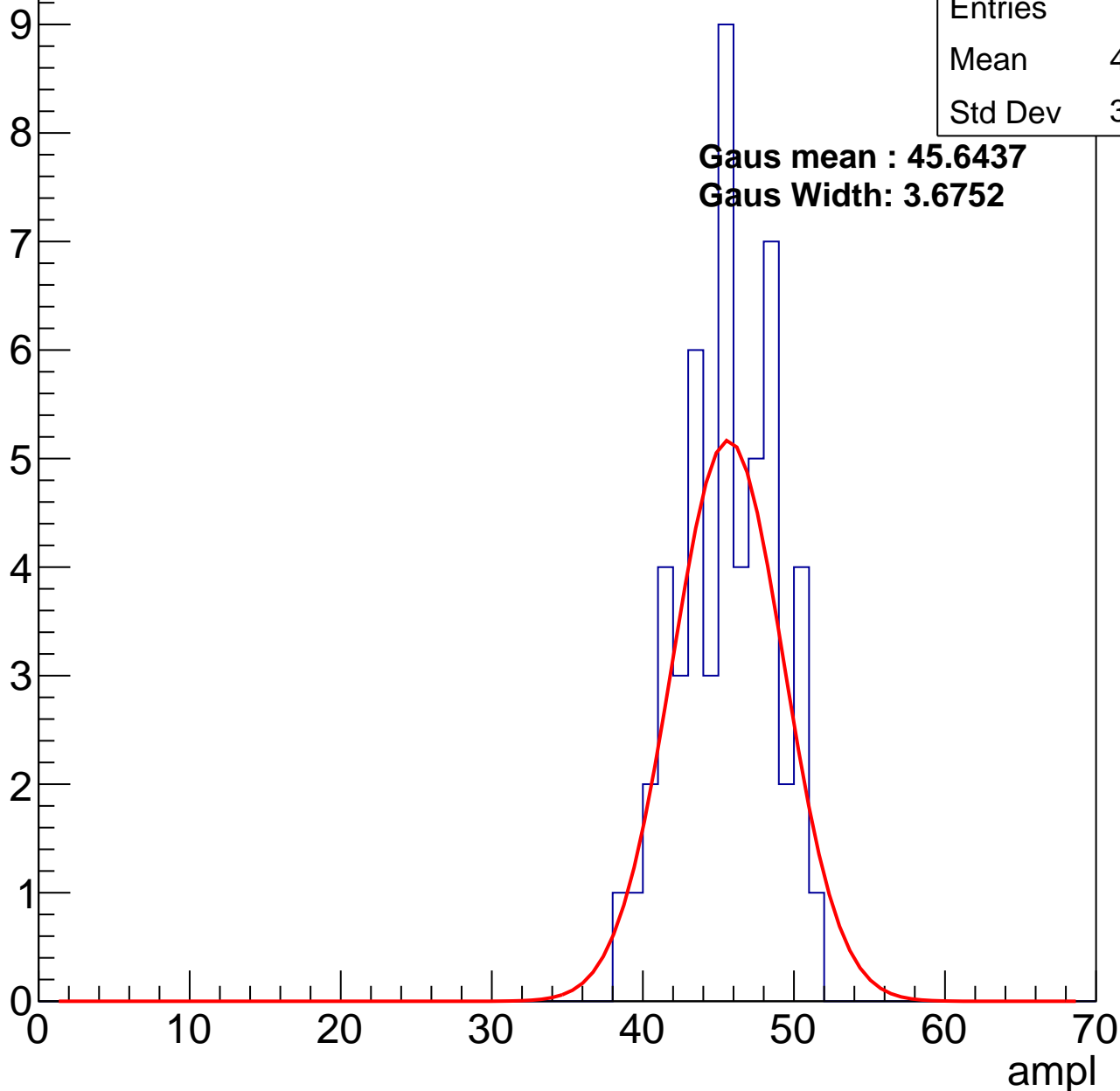
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	45.12
Std Dev	3.123

**Gaus mean : 45.6437**

**Gaus Width: 3.6752**

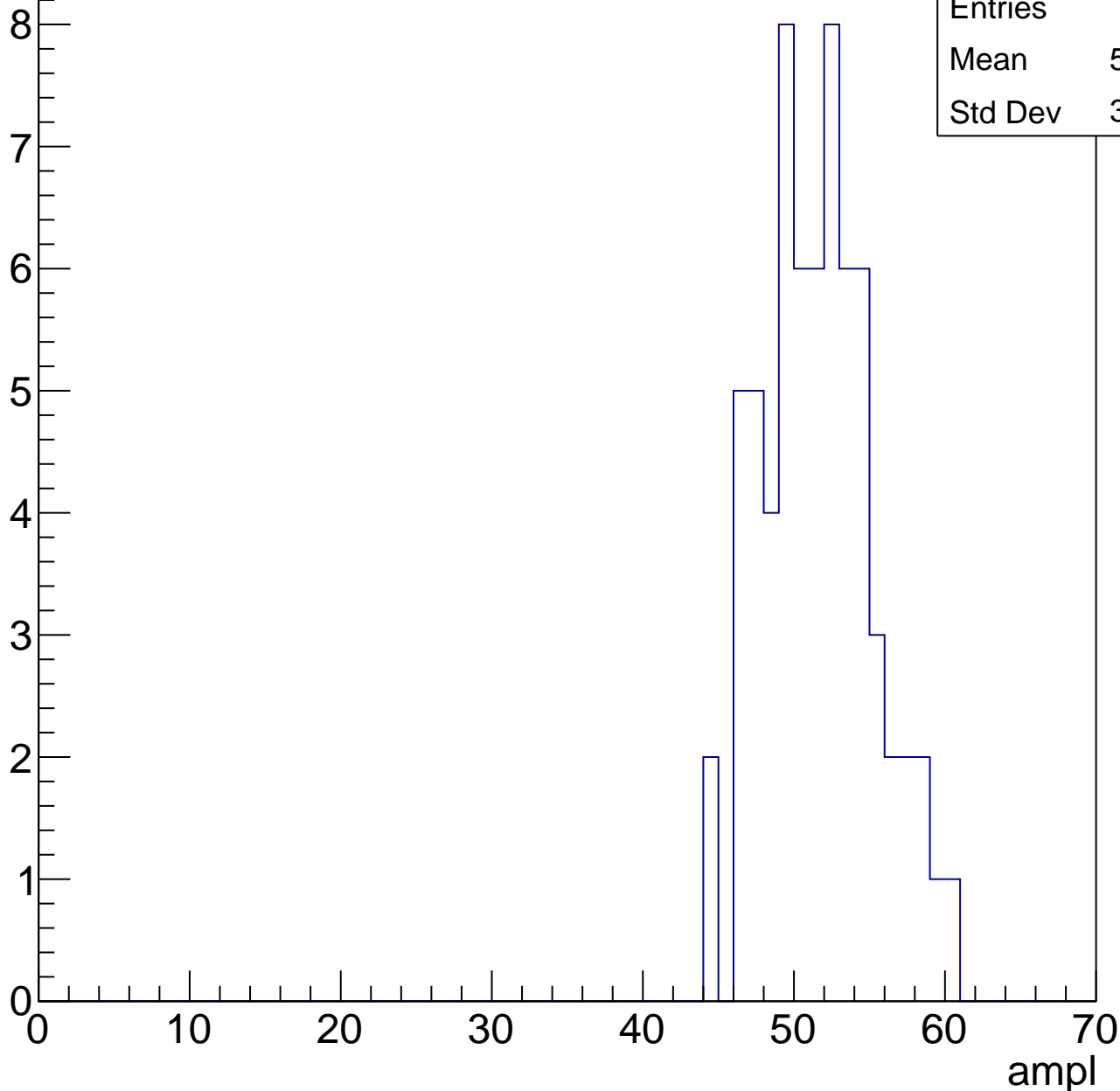


# B0L001S, U24-ch80, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

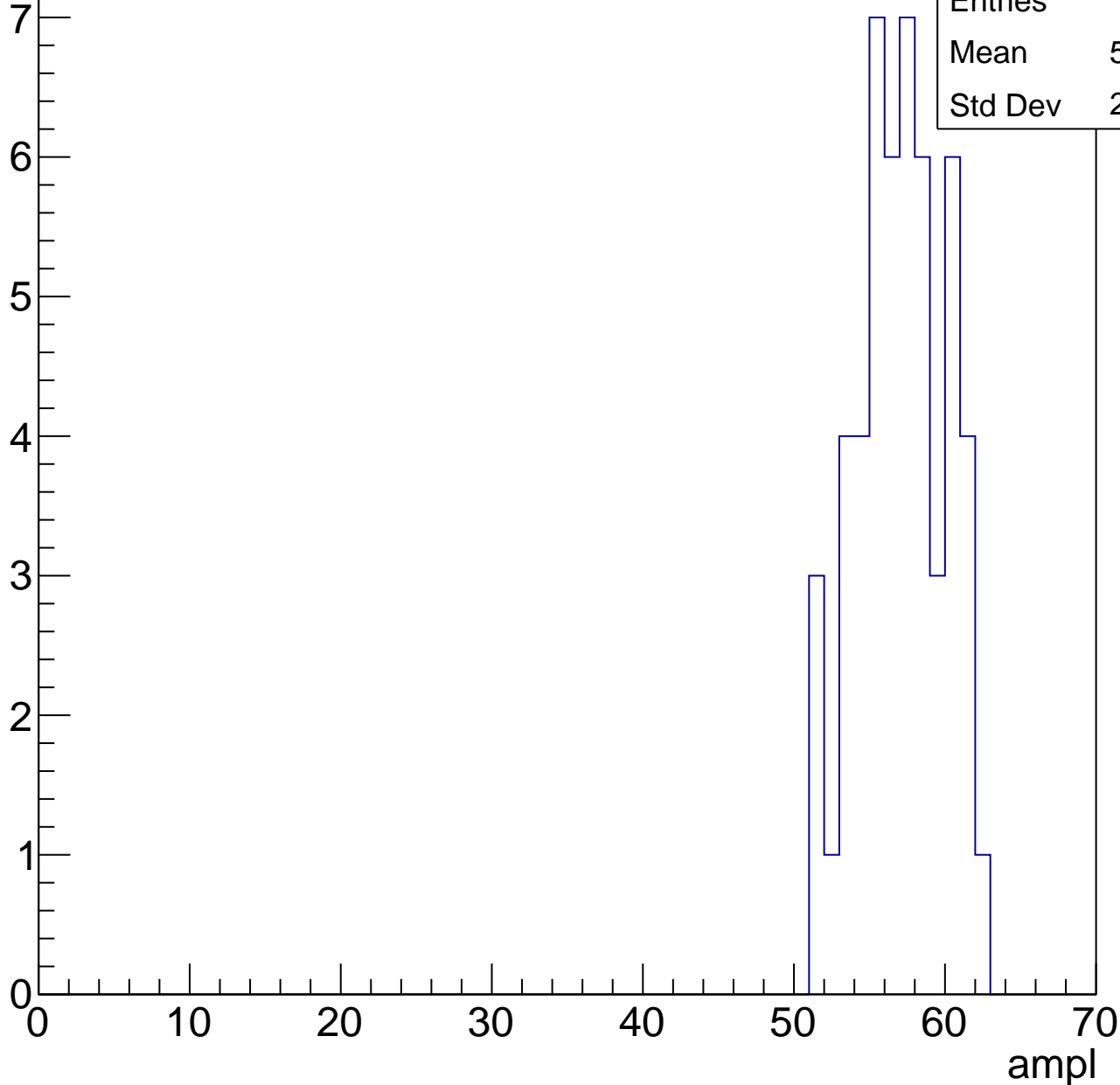
Entries	67
Mean	51.15
Std Dev	3.613



# B0L001S, U24-ch80, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



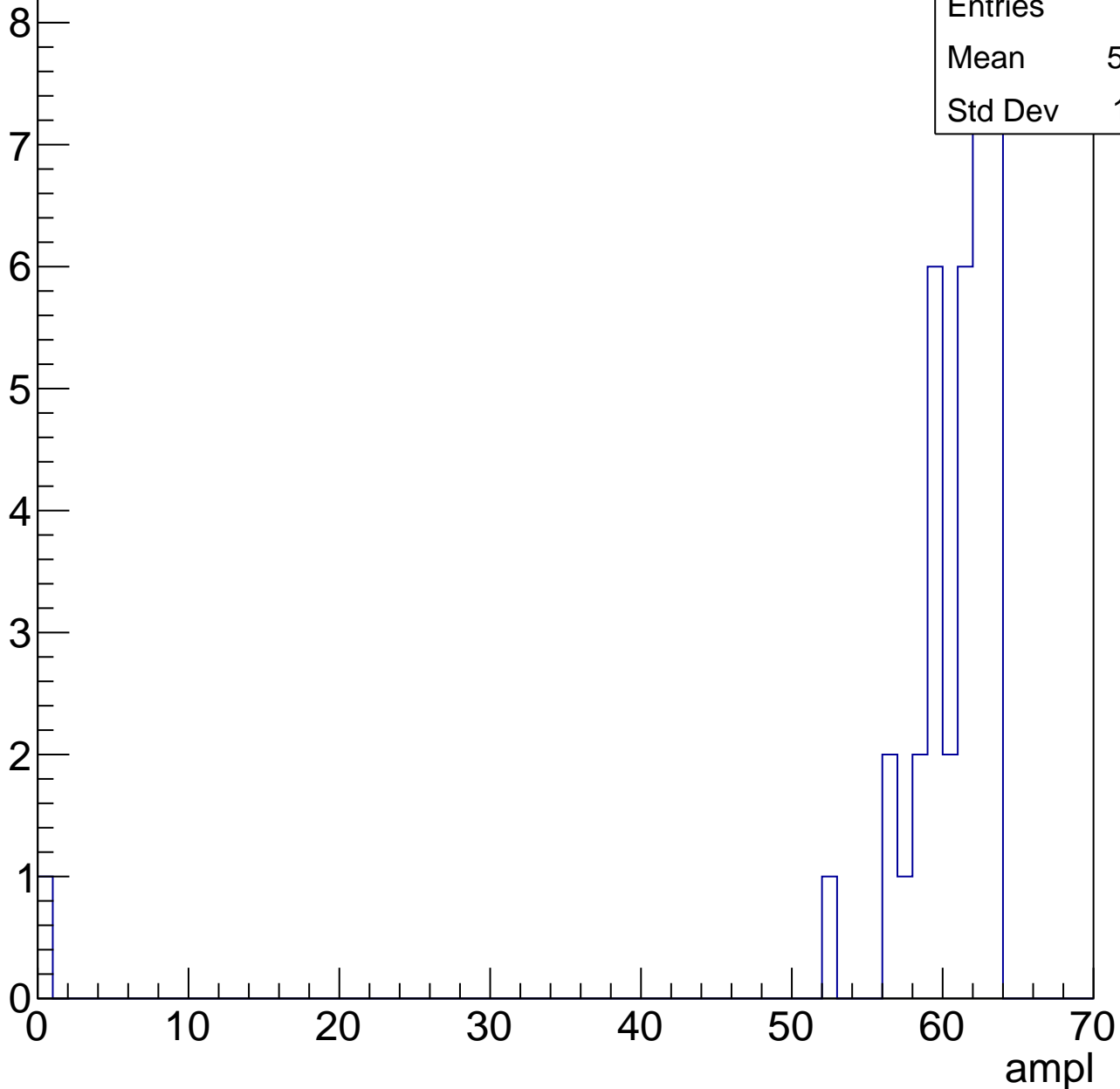
Entries	52
Mean	56.62
Std Dev	2.843

# B0L001S, U24-ch80, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	37
Mean	58.84
Std Dev	10.11



# B0L001S, U24-ch80, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

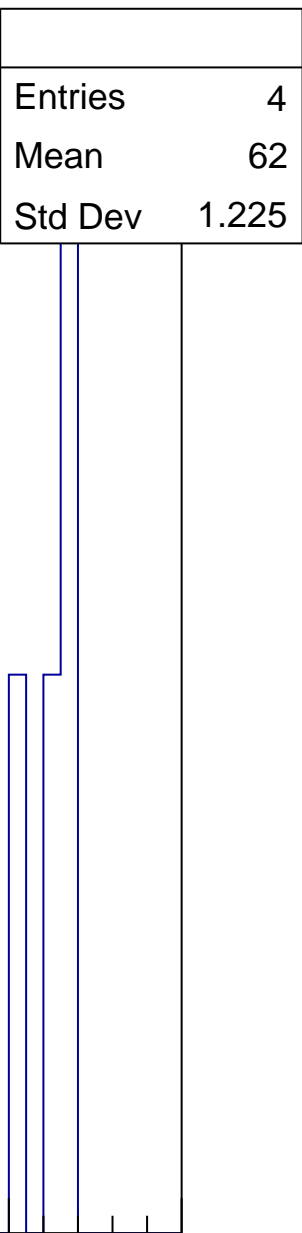
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	62
Std Dev	1.225

0 10 20 30 40 50 60 70

ampl





# B0L001S, U24-ch80, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U24-ch81, adc0

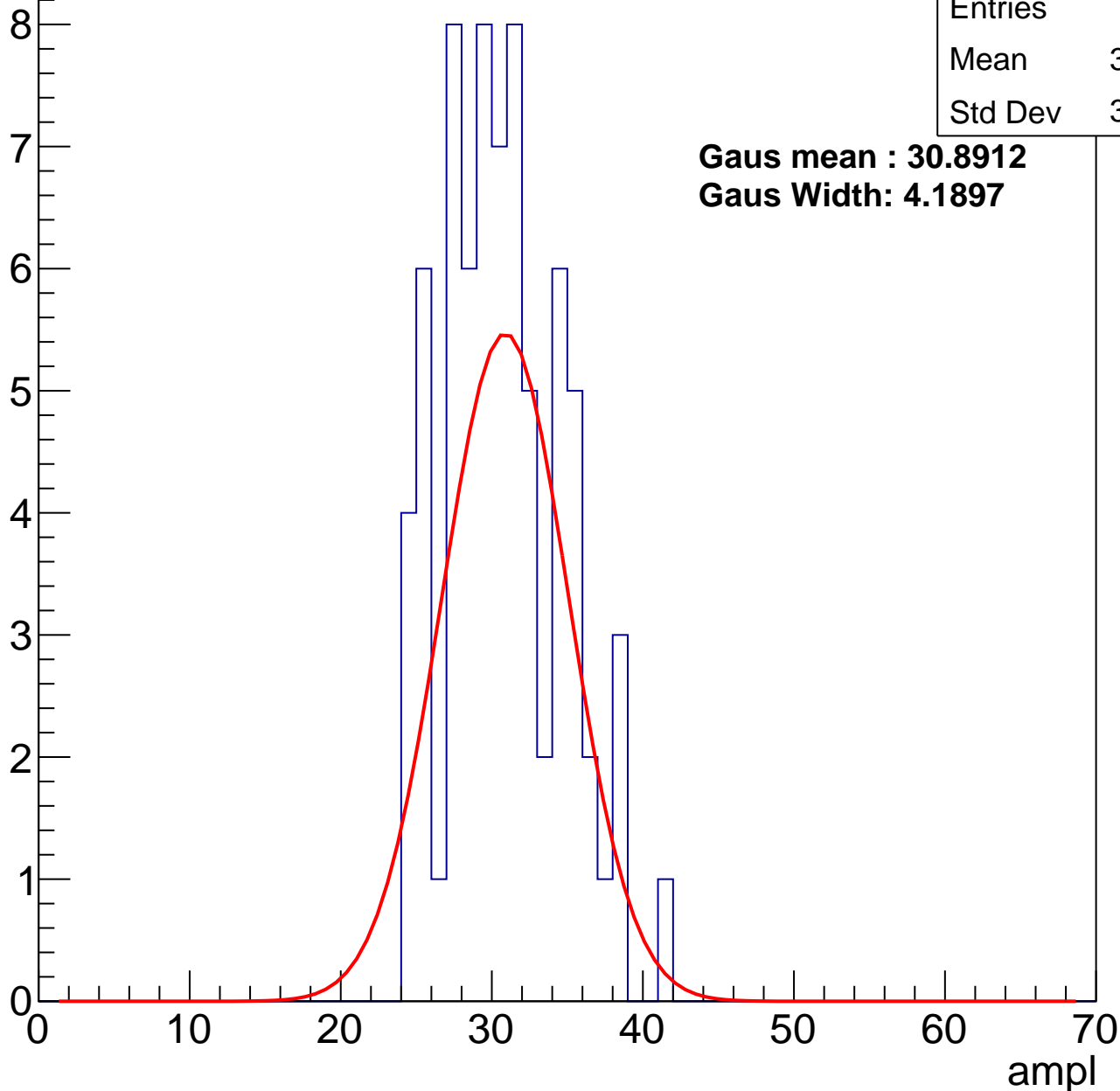
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	30.34
Std Dev	3.893

**Gaus mean : 30.8912**

**Gaus Width: 4.1897**



# B0L001S, U24-ch81, adc1

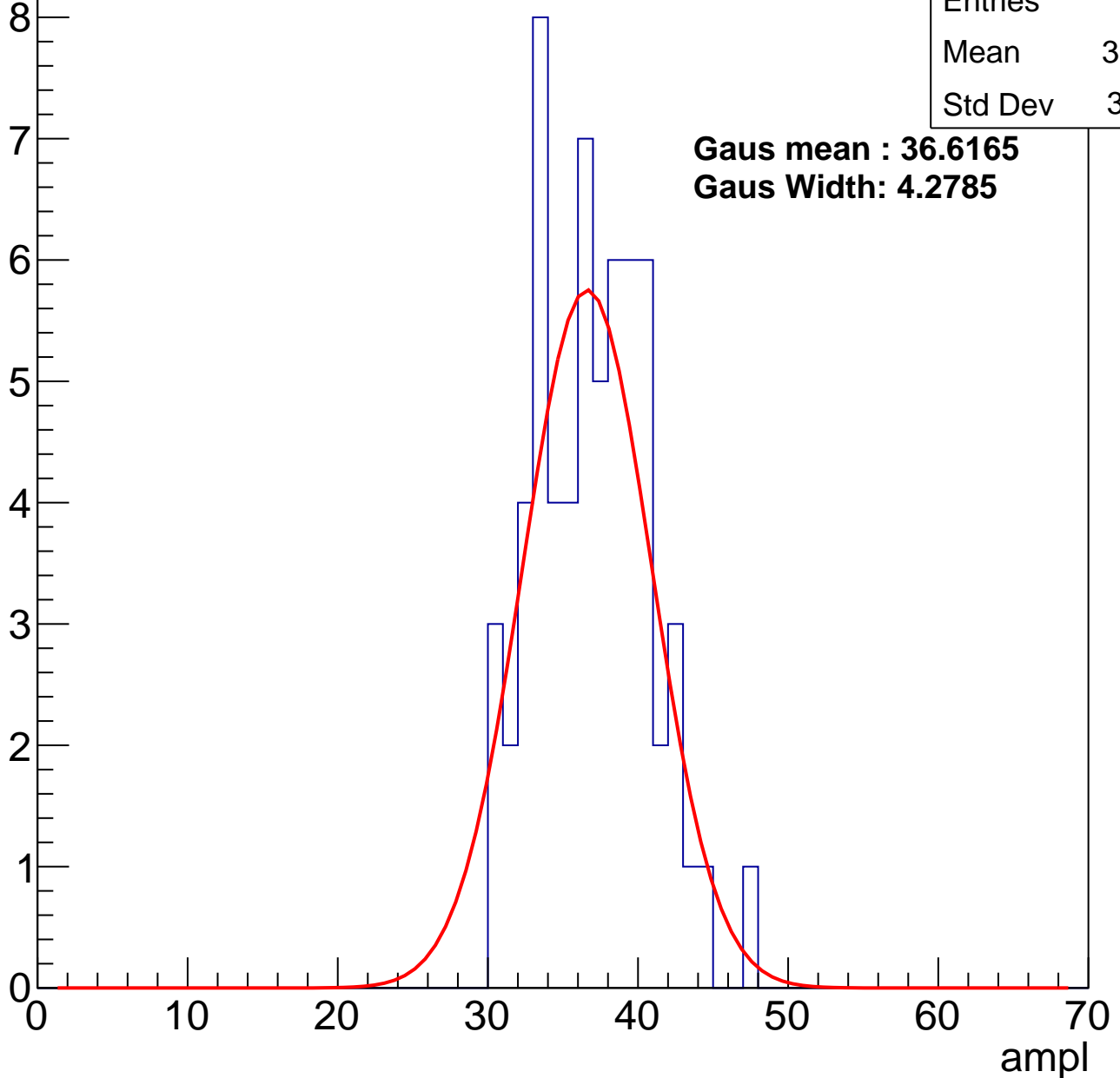
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	36.52
Std Dev	3.711

**Gaus mean : 36.6165**

**Gaus Width: 4.2785**



# B0L001S, U24-ch81, adc2

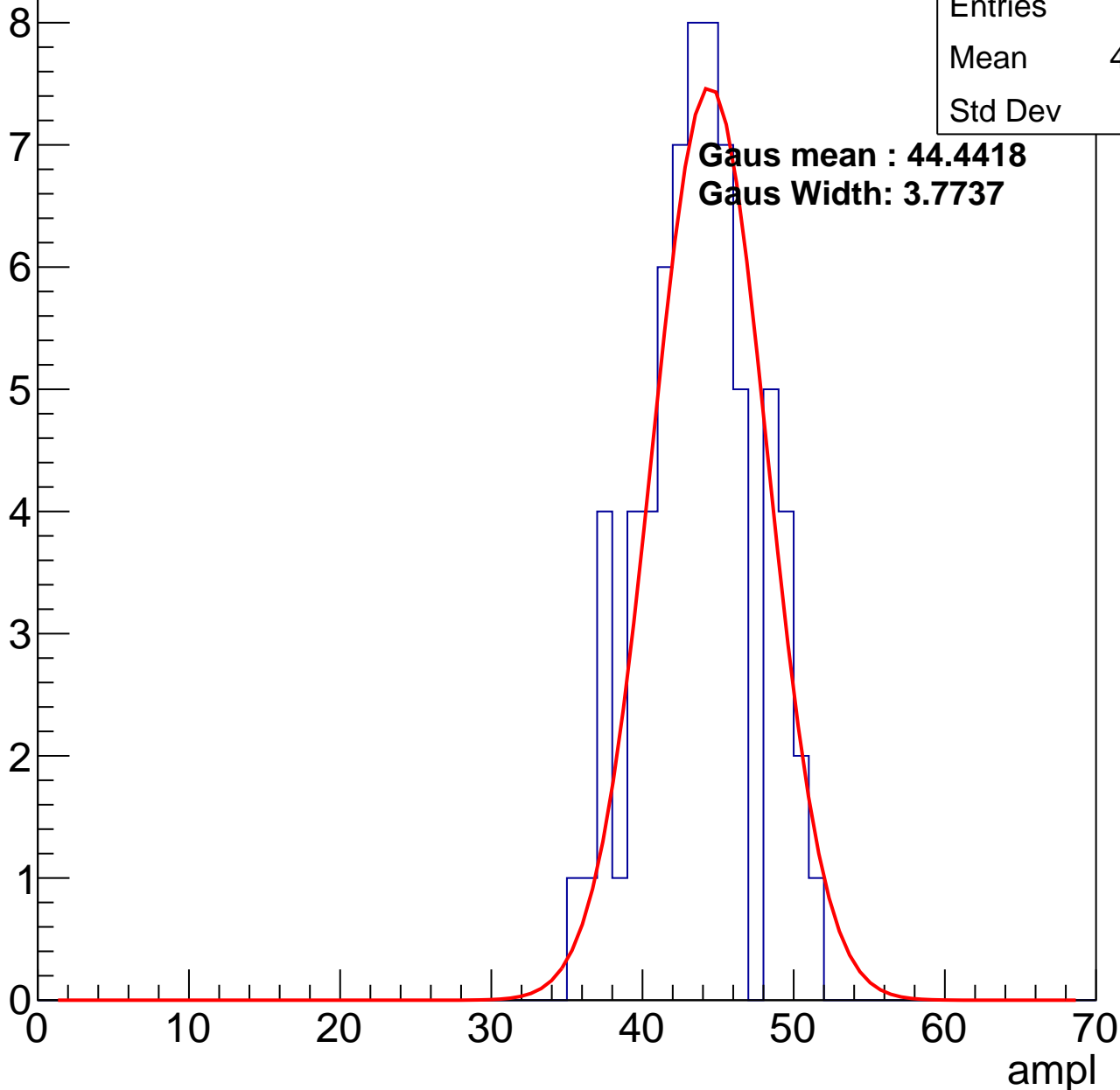
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	43.25
Std Dev	3.68

**Gaus mean : 44.4418**

**Gaus Width: 3.7737**

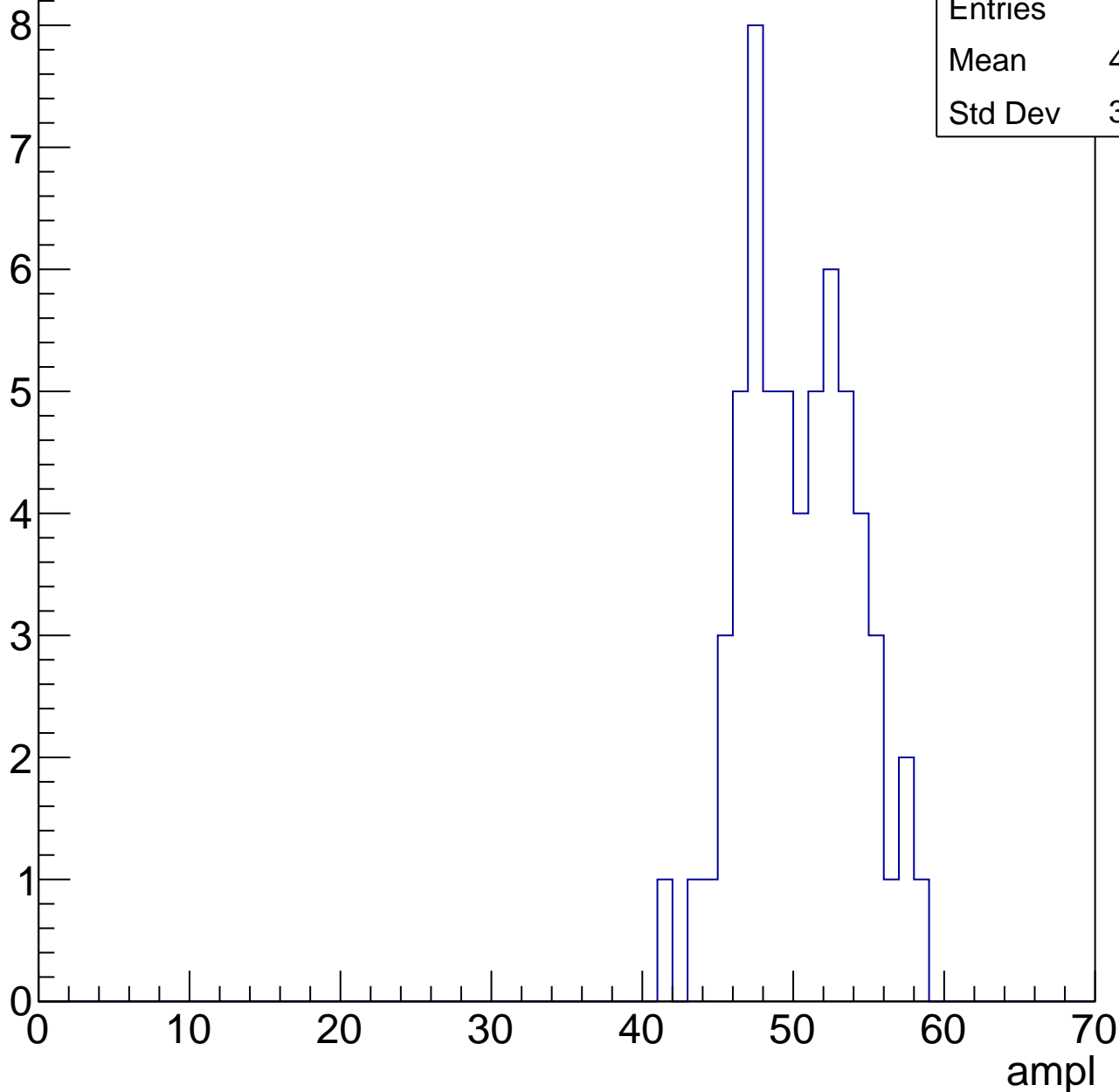


# B0L001S, U24-ch81, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	49.92
Std Dev	3.716

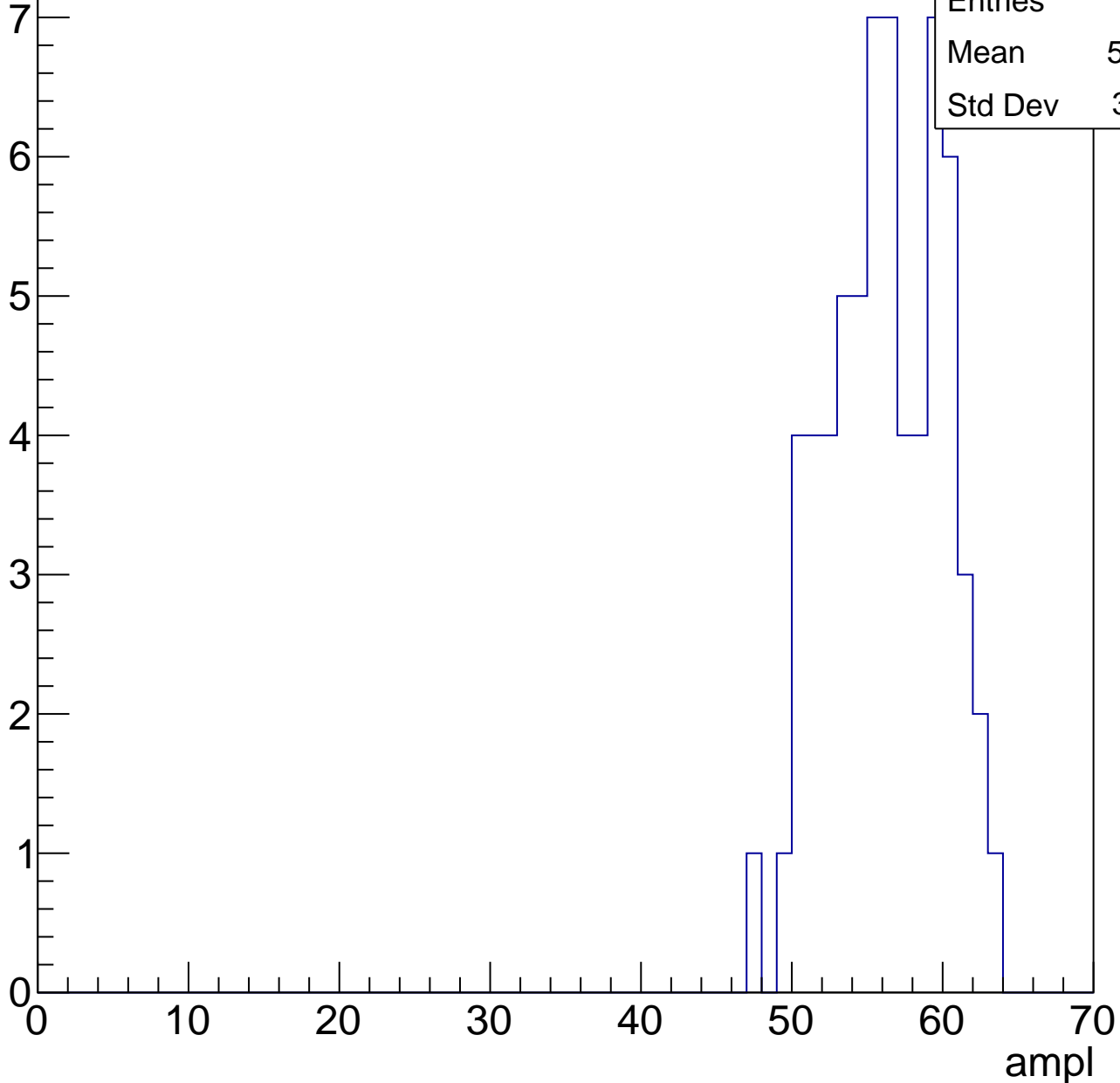


# B0L001S, U24-ch81, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	55.74
Std Dev	3.681

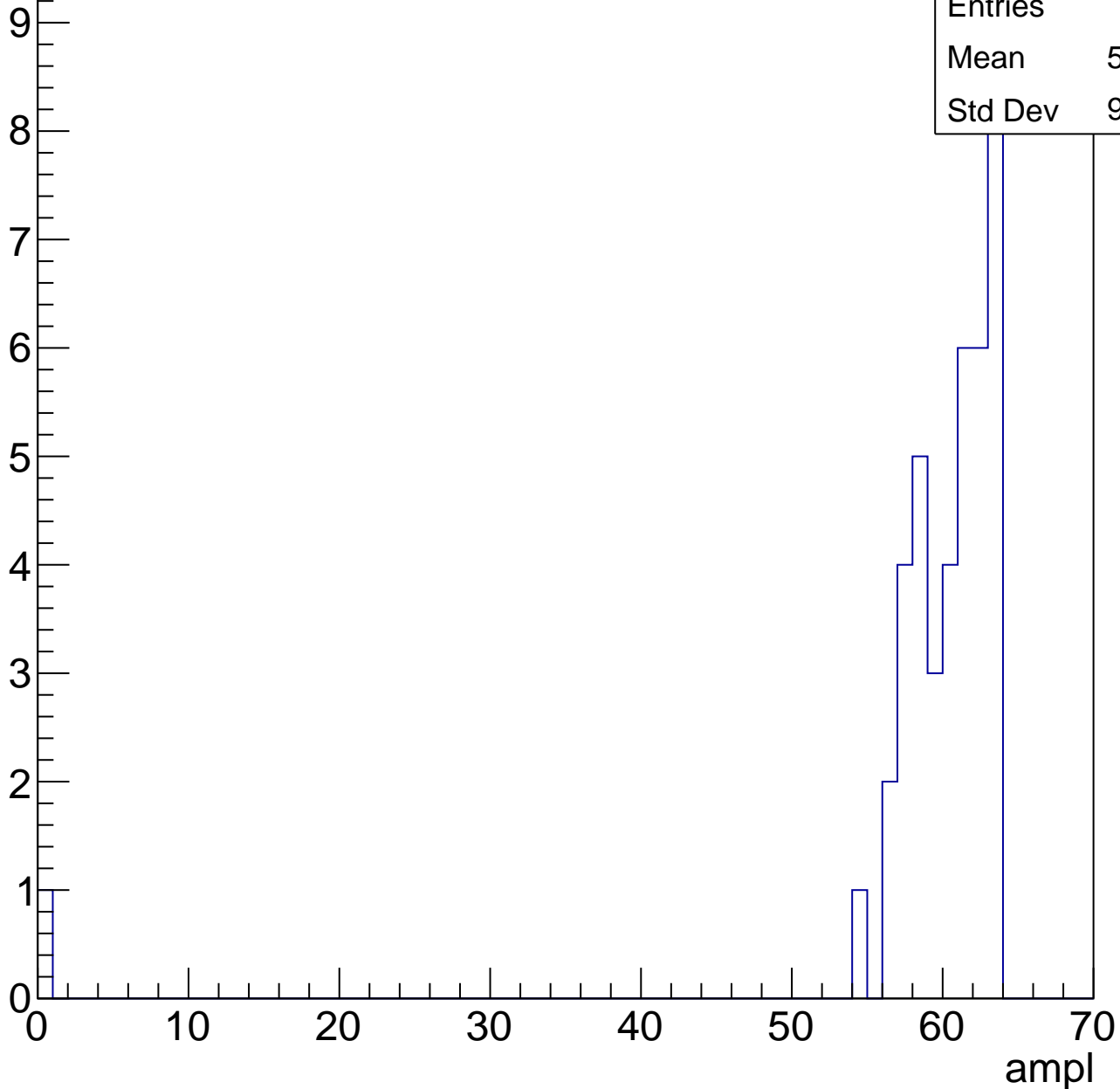


# B0L001S, U24-ch81, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	41
Mean	58.68
Std Dev	9.585



# B0L001S, U24-ch81, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	61.67
Std Dev	0.4714

ampl

0 10 20 30 40 50 60 70



# B0L001S, U24-ch81, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	3
Mean	7.667
Std Dev	10.84

# B0L001S, U24-ch82, adc0

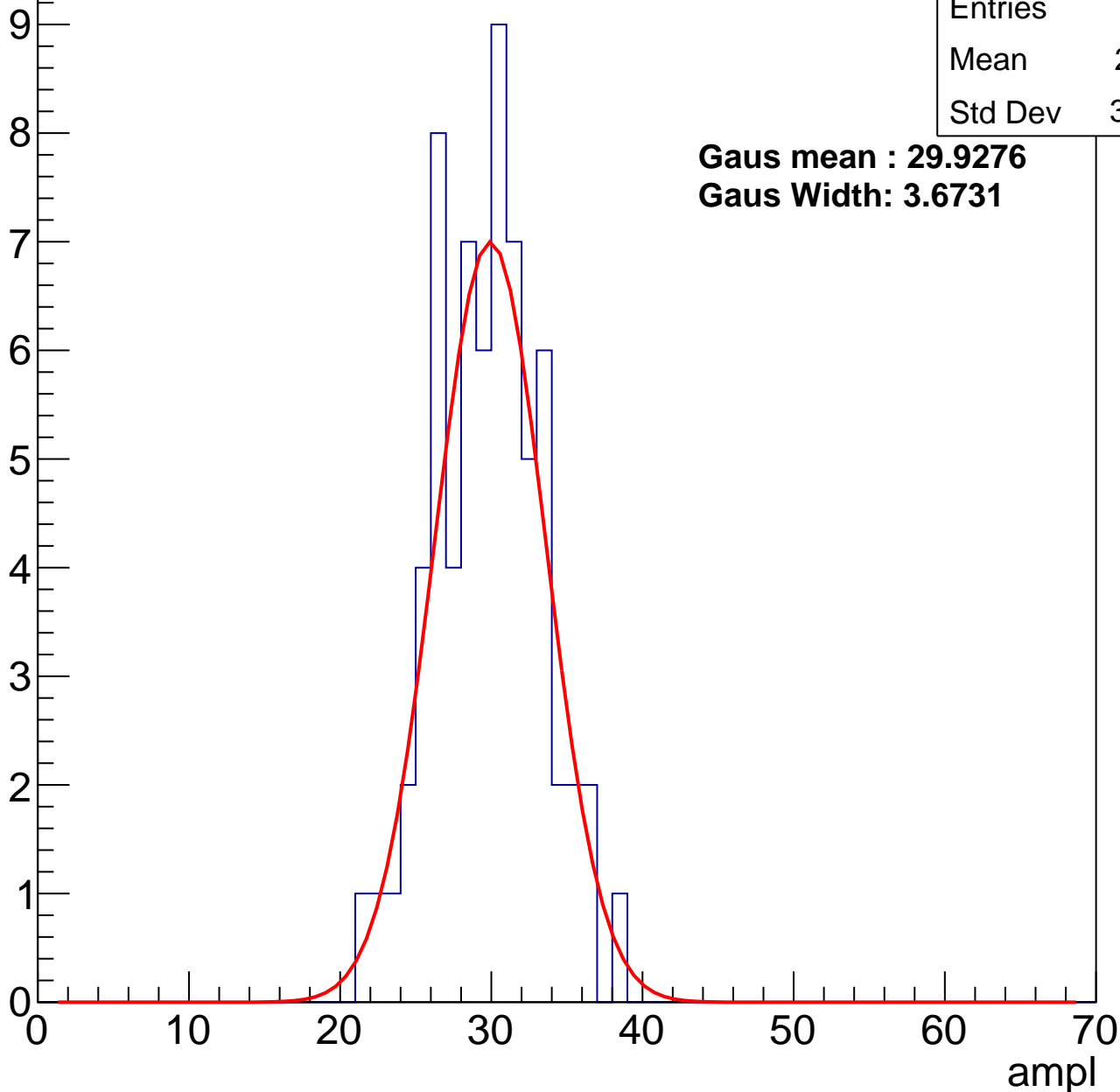
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	29.31
Std Dev	3.495

**Gaus mean : 29.9276**

**Gaus Width: 3.6731**



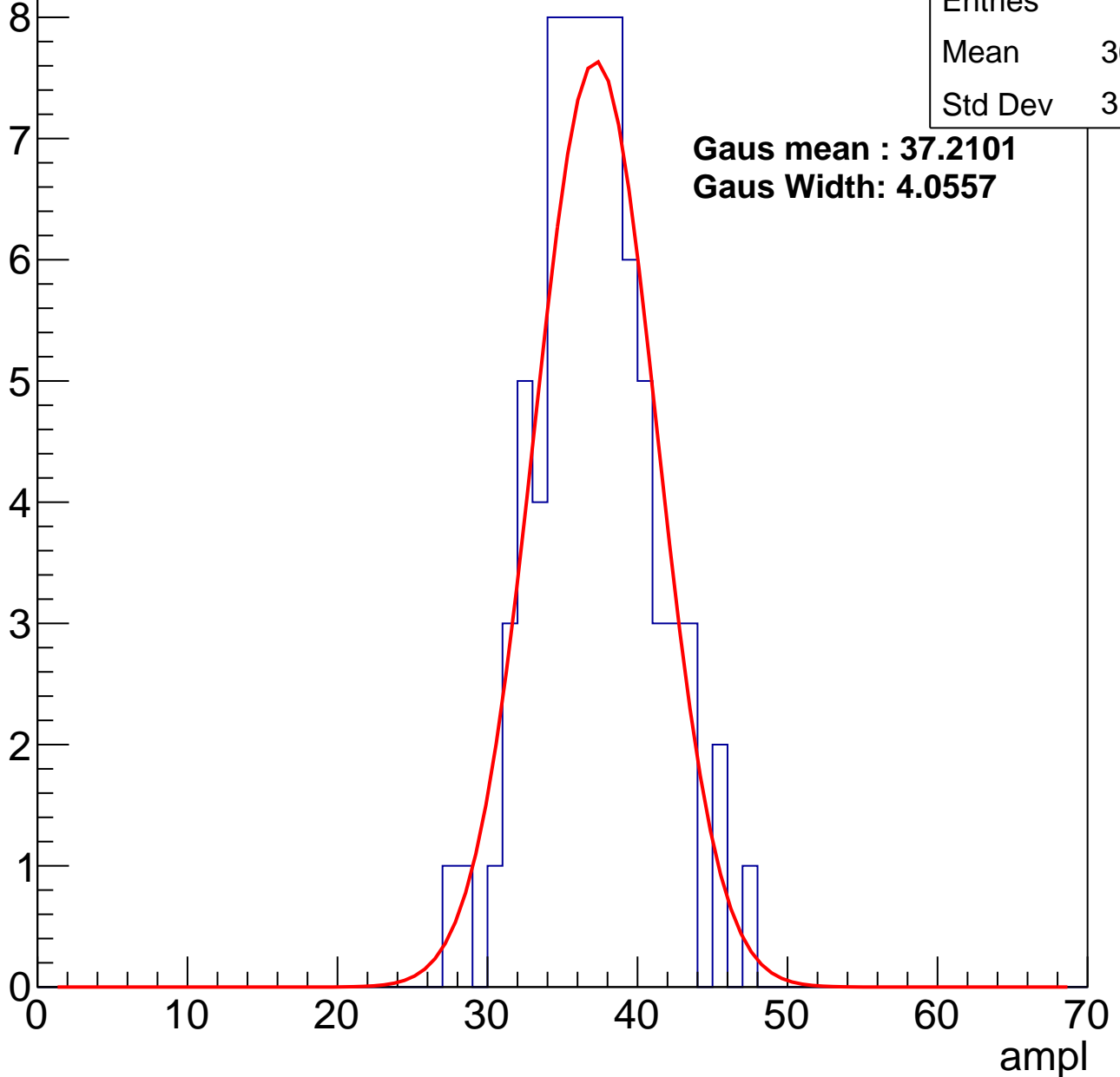
# B0L001S, U24-ch82, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	78
Mean	36.65
Std Dev	3.866

**Gaus mean : 37.2101**  
**Gaus Width: 4.0557**



# B0L001S, U24-ch82, adc2

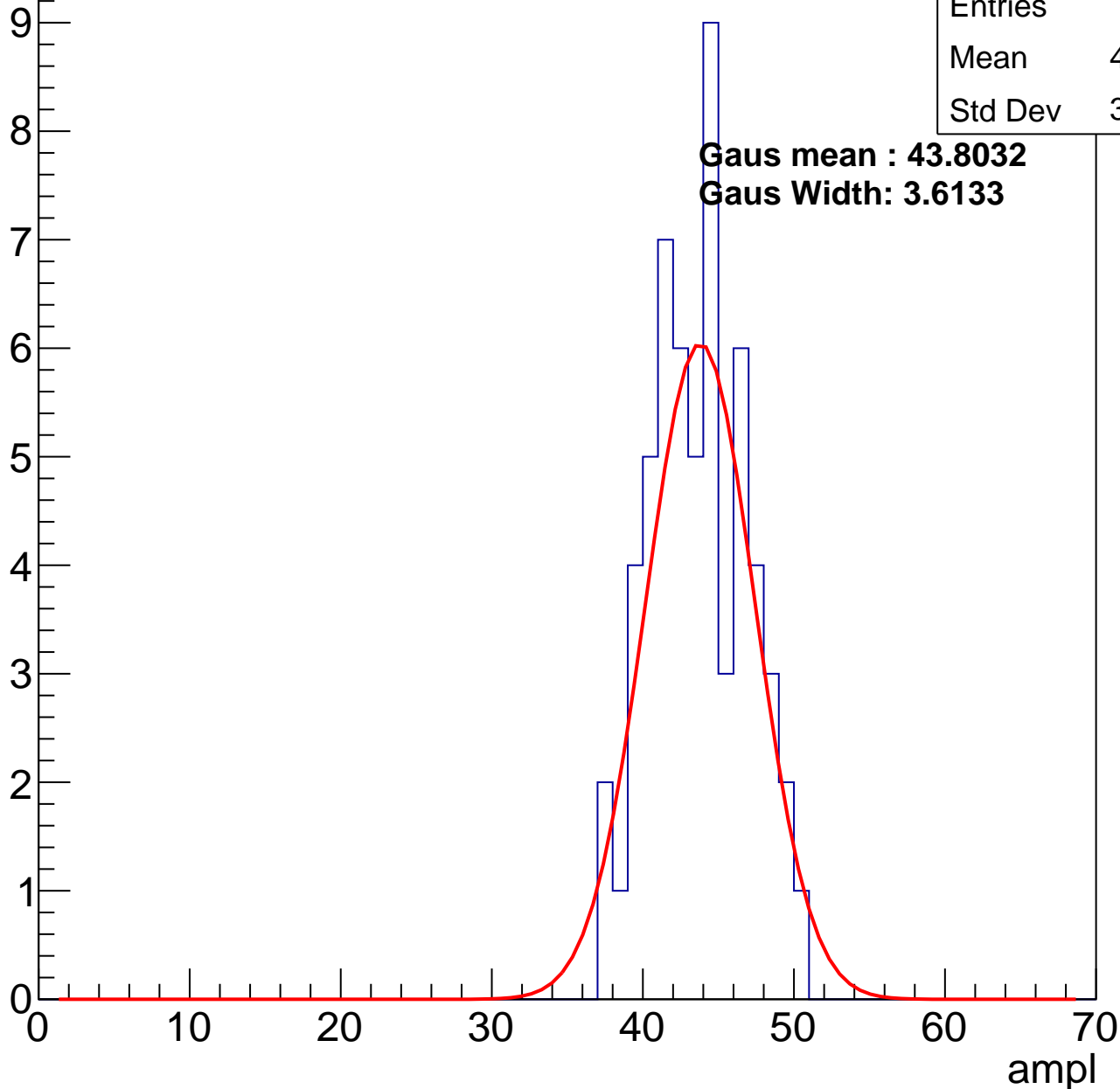
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	43.26
Std Dev	3.138

**Gaus mean : 43.8032**

**Gaus Width: 3.6133**

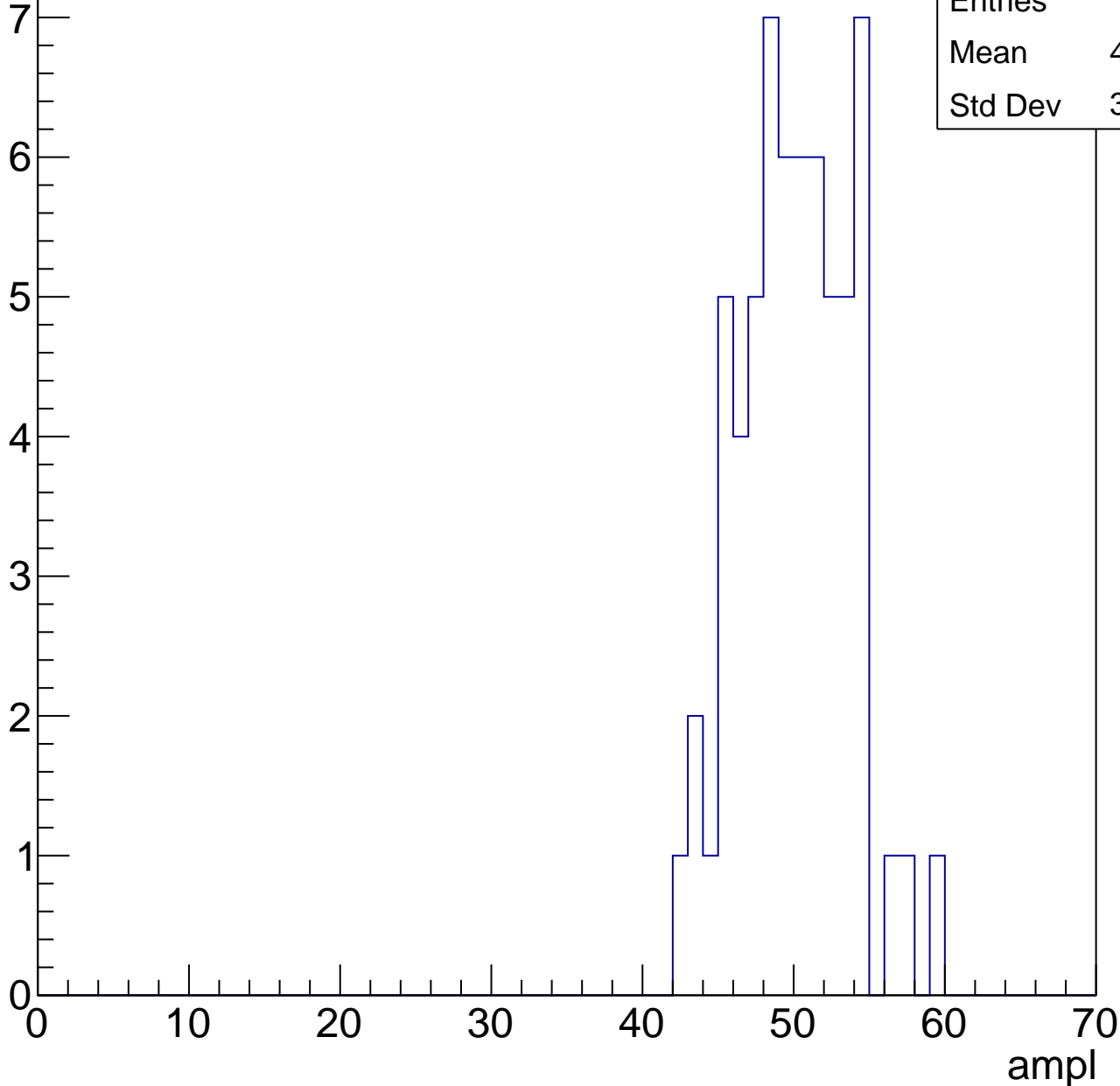


# B0L001S, U24-ch82, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	49.63
Std Dev	3.578

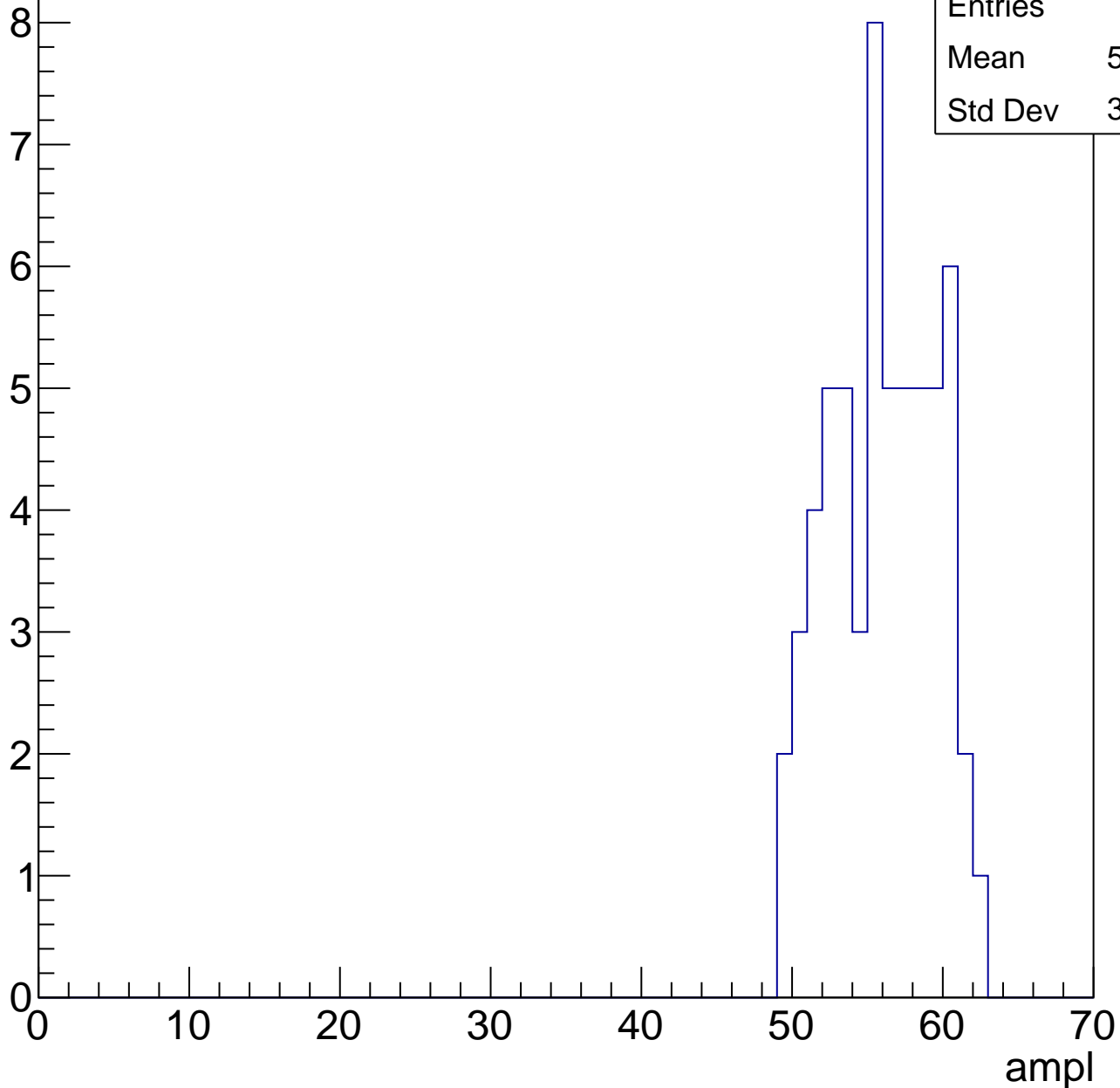


# B0L001S, U24-ch82, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	55.47
Std Dev	3.412

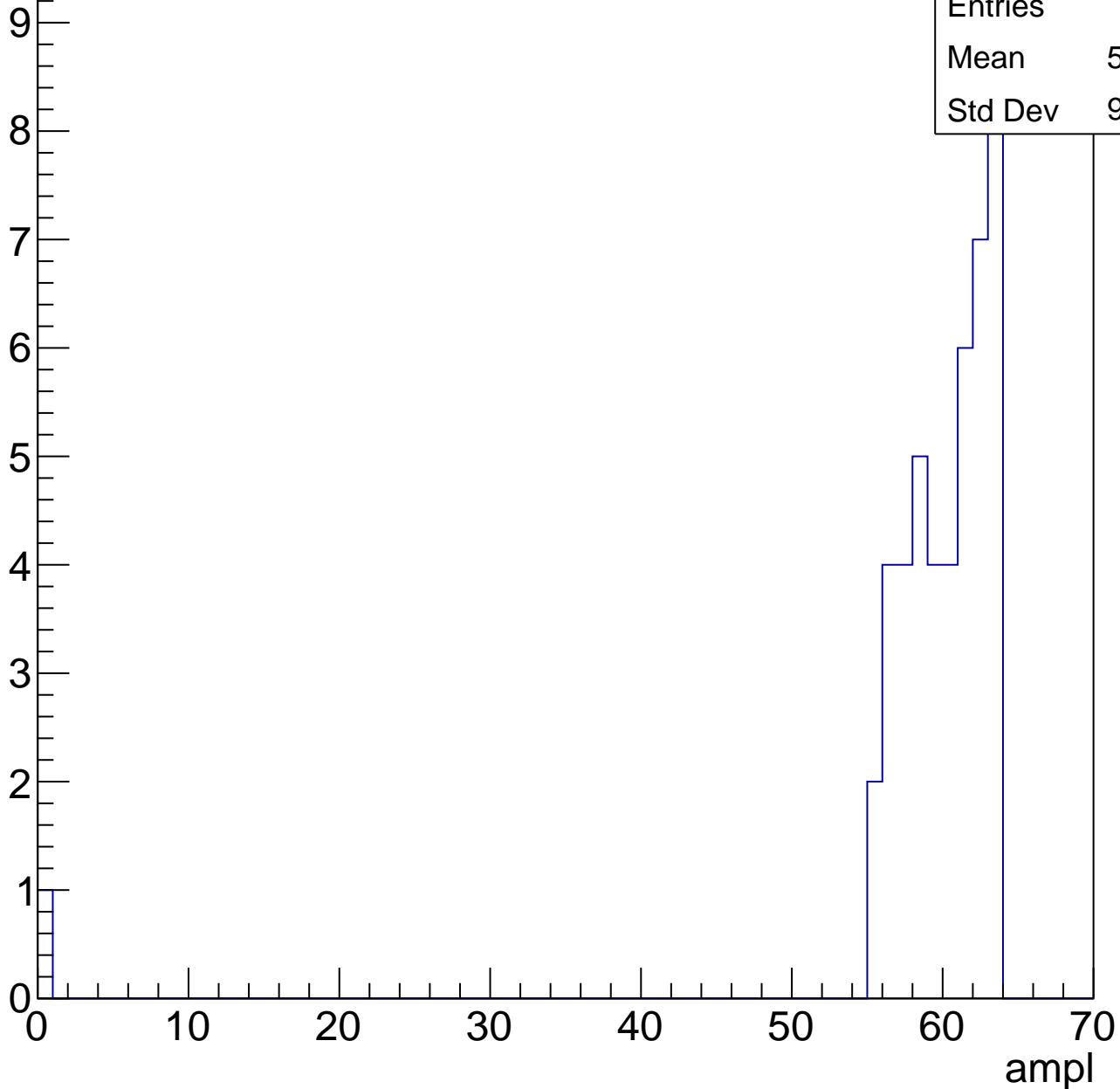


# B0L001S, U24-ch82, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	46
Mean	58.59
Std Dev	9.086



# B0L001S, U24-ch82, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	61.8
Std Dev	0.7483

ampl

0 10 20 30 40 50 60 70



# B0L001S, U24-ch82, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L001S, U24-ch83, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	71
Mean	30.32
Std Dev	7.193

**Gaus mean : 32.2237**

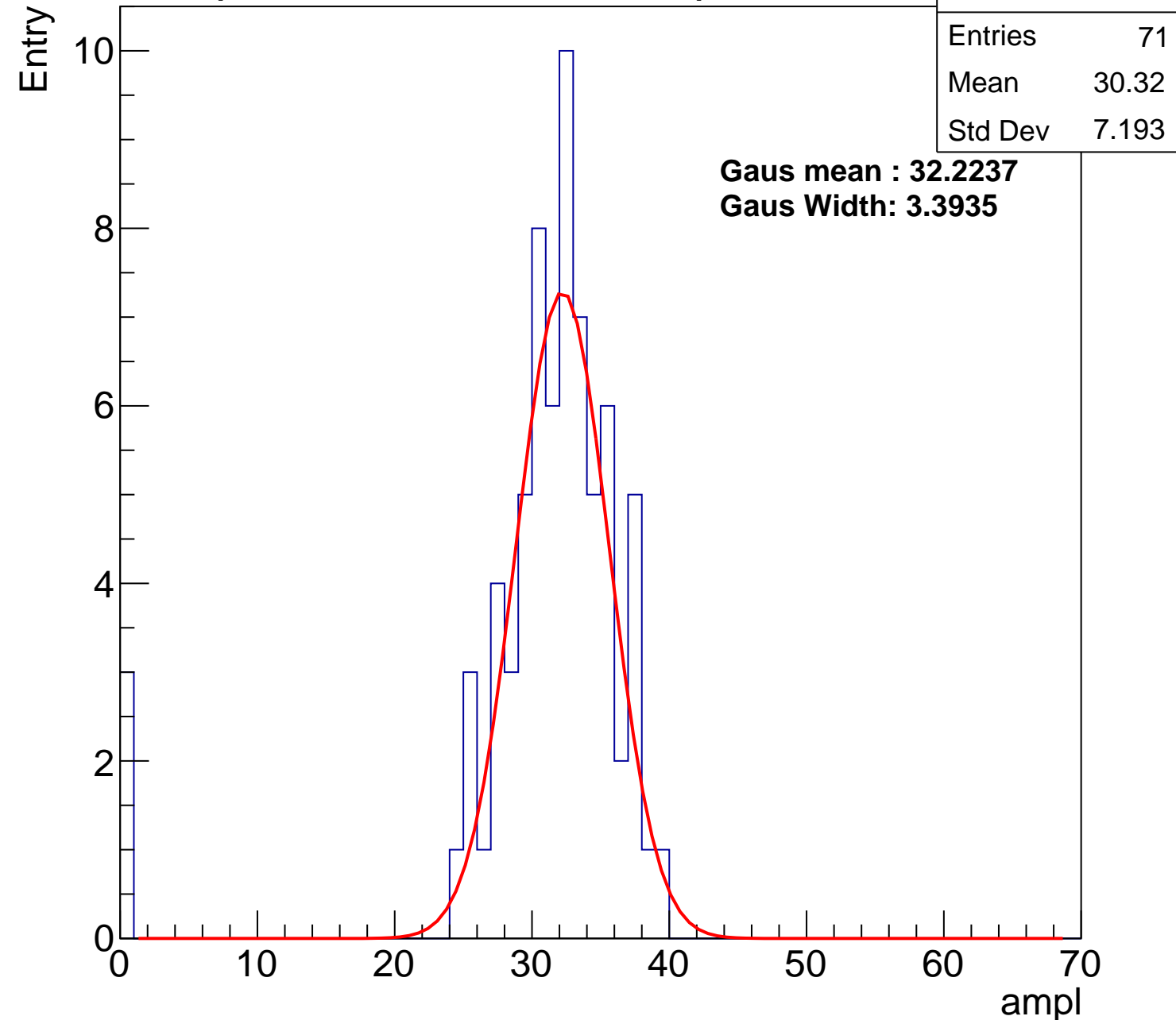
**Gaus Width: 3.3935**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U24-ch83, adc1

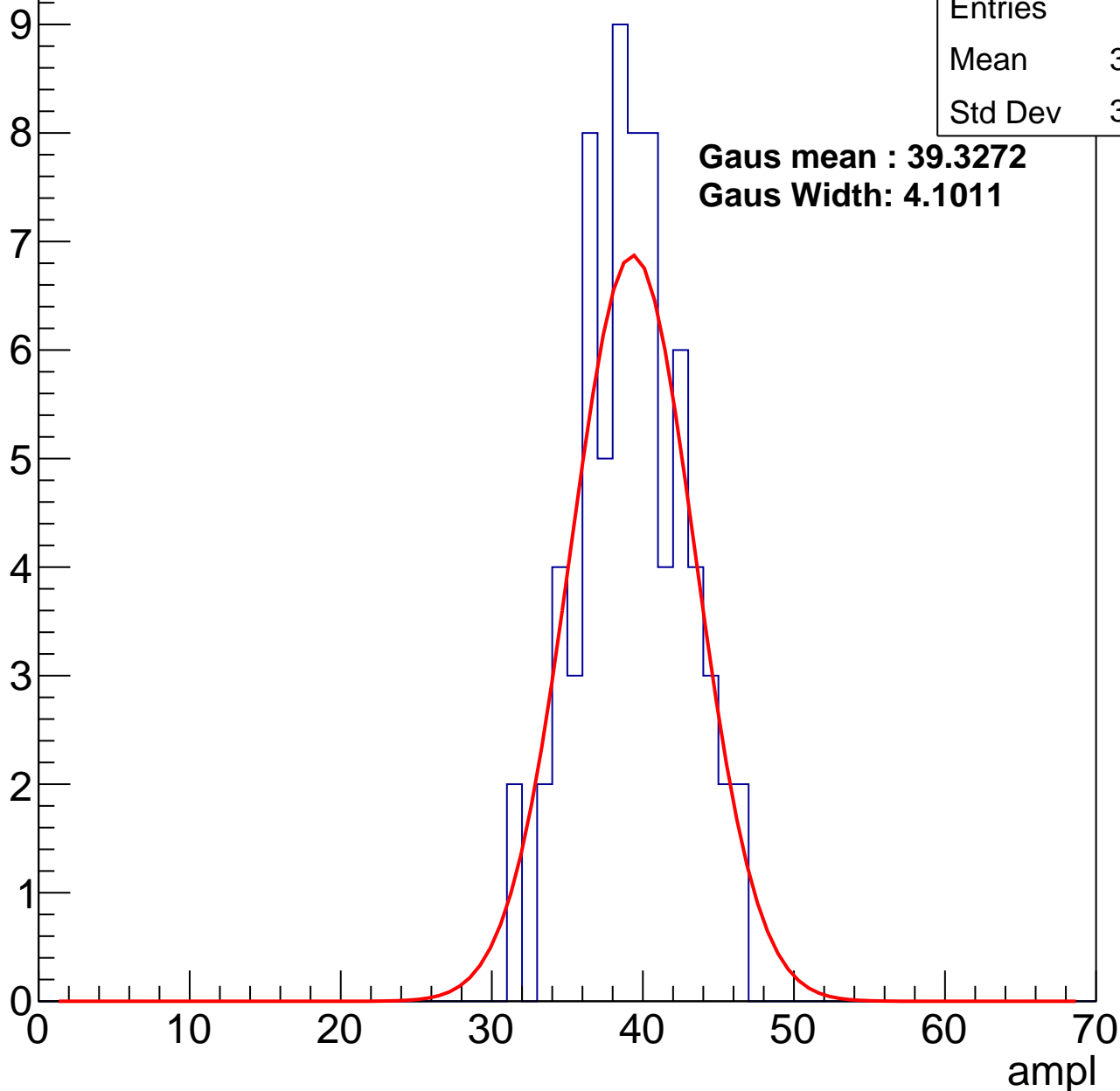
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	38.83
Std Dev	3.452

**Gaus mean : 39.3272**

**Gaus Width: 4.1011**



# B0L001S, U24-ch83, adc2

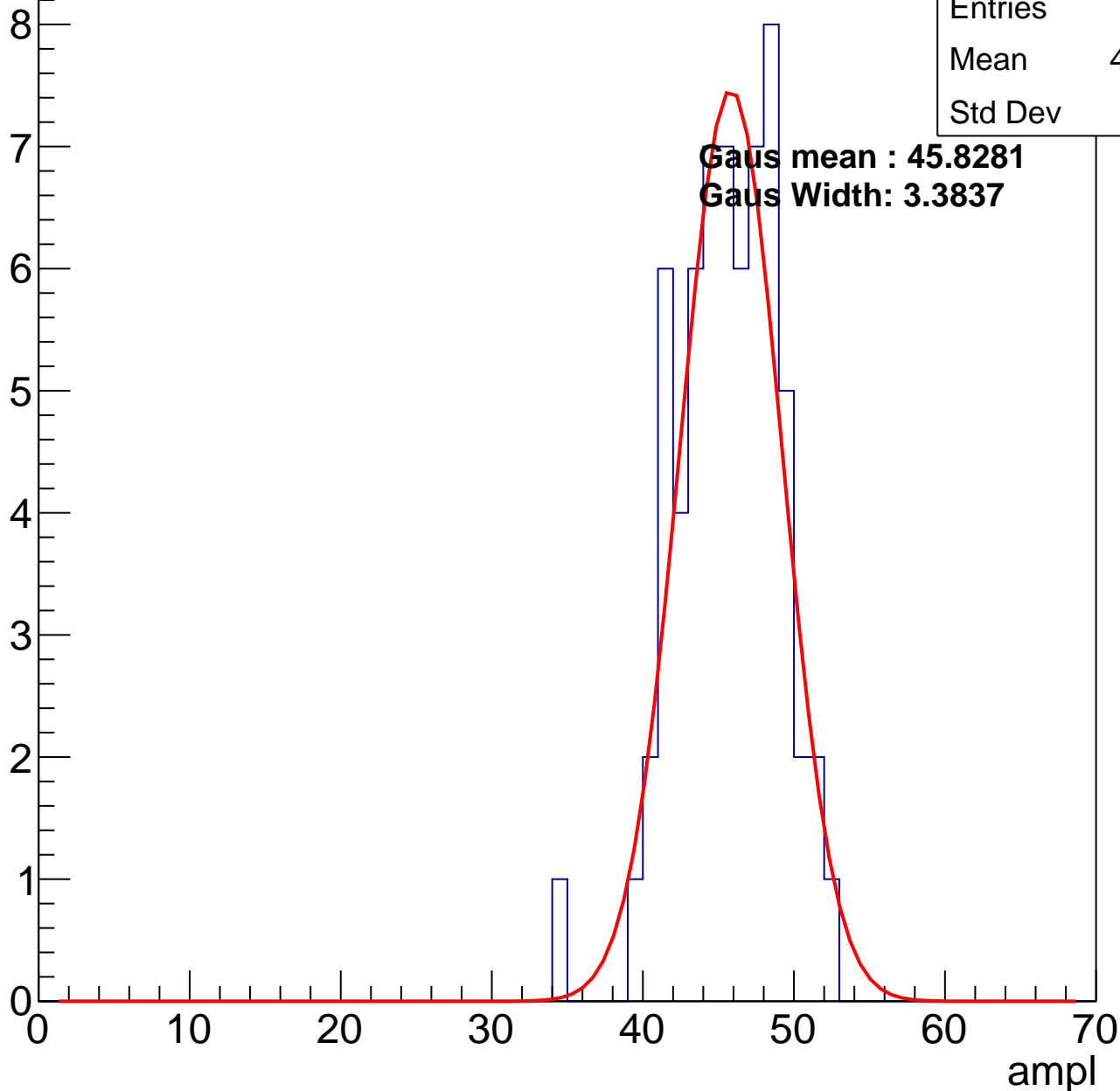
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	45.17
Std Dev	3.34

**Gaus mean : 45.8281**

**Gaus Width: 3.3837**

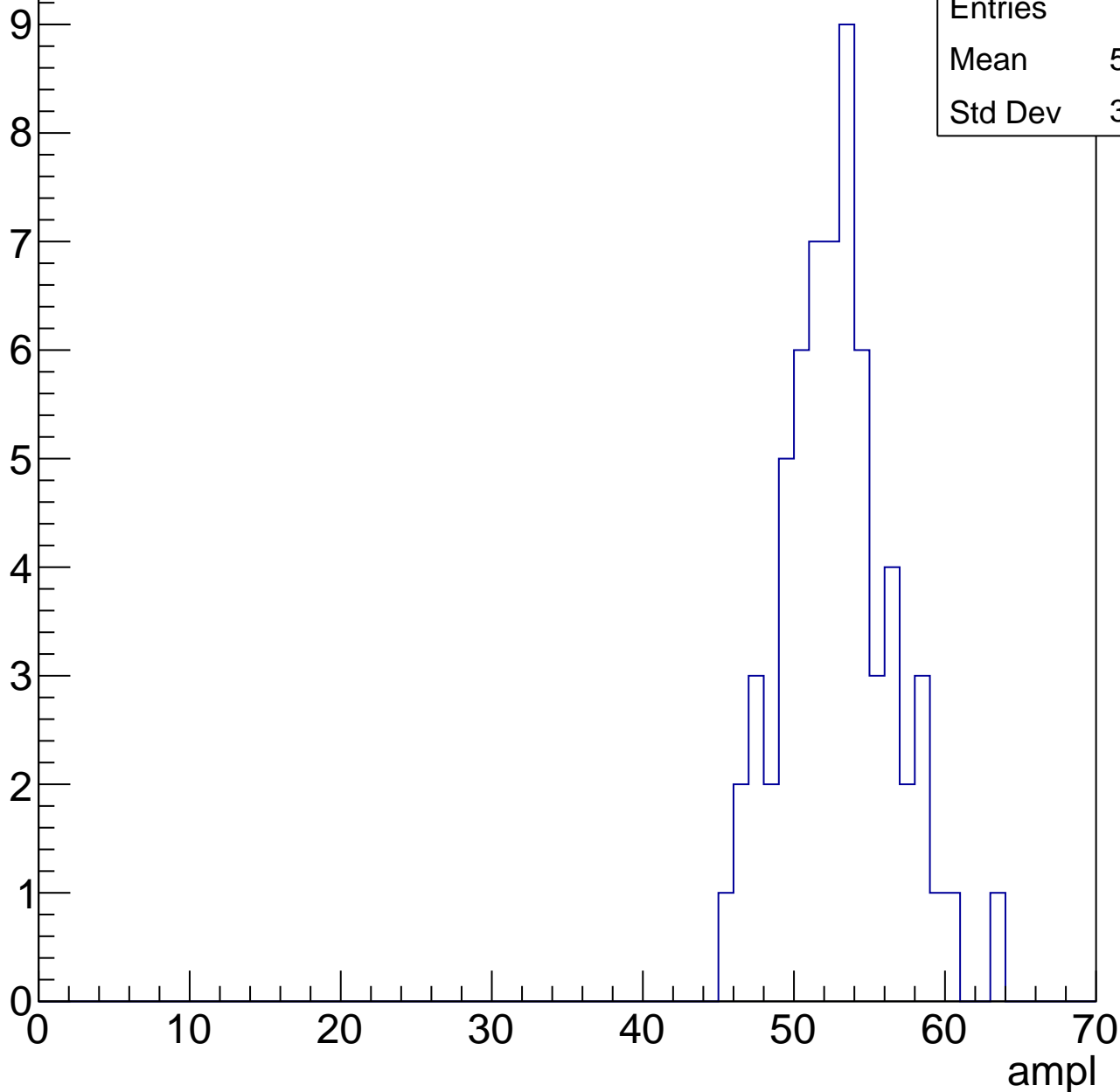


# B0L001S, U24-ch83, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	52.38
Std Dev	3.588

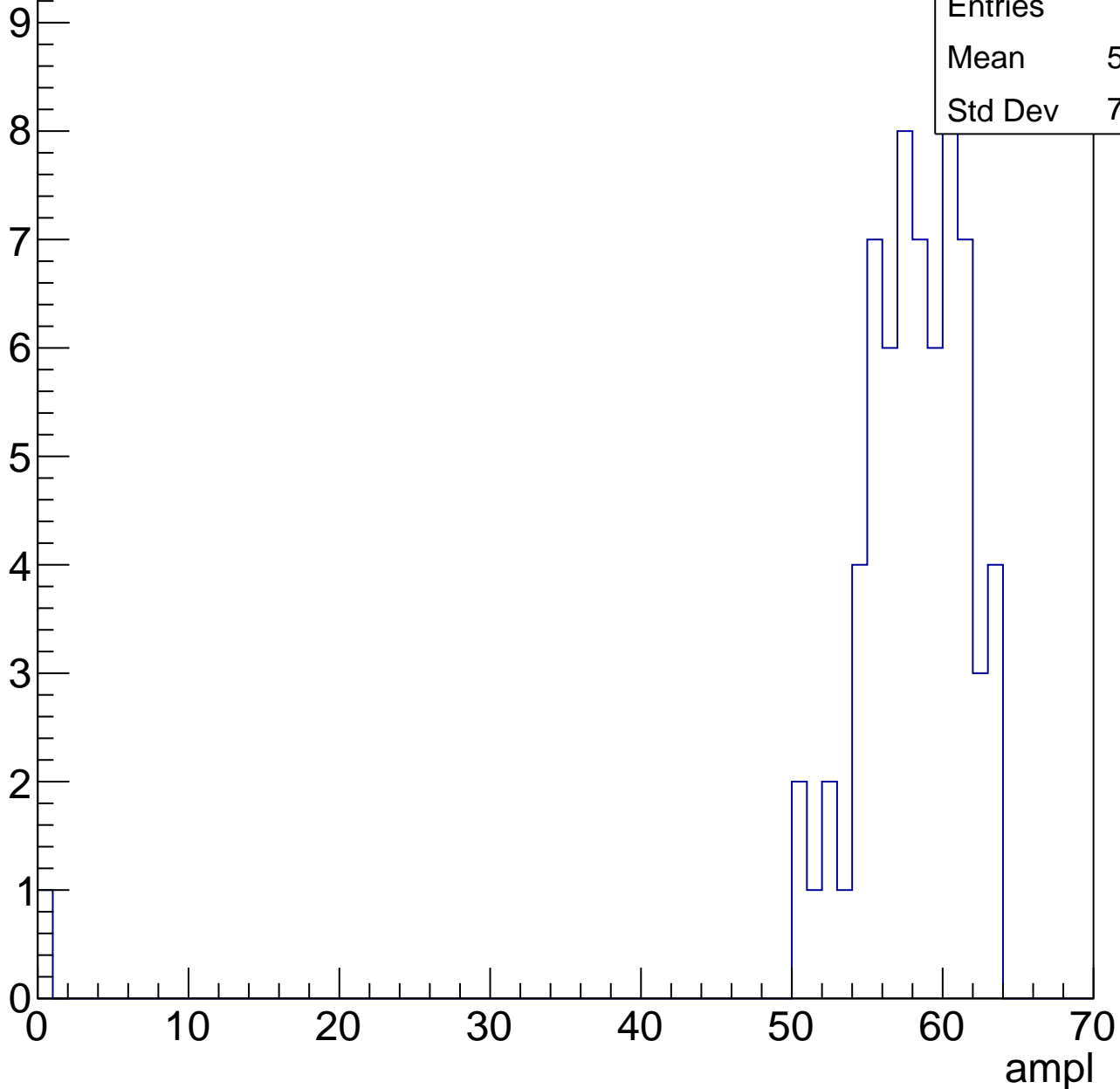


# B0L001S, U24-ch83, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	56.85
Std Dev	7.632

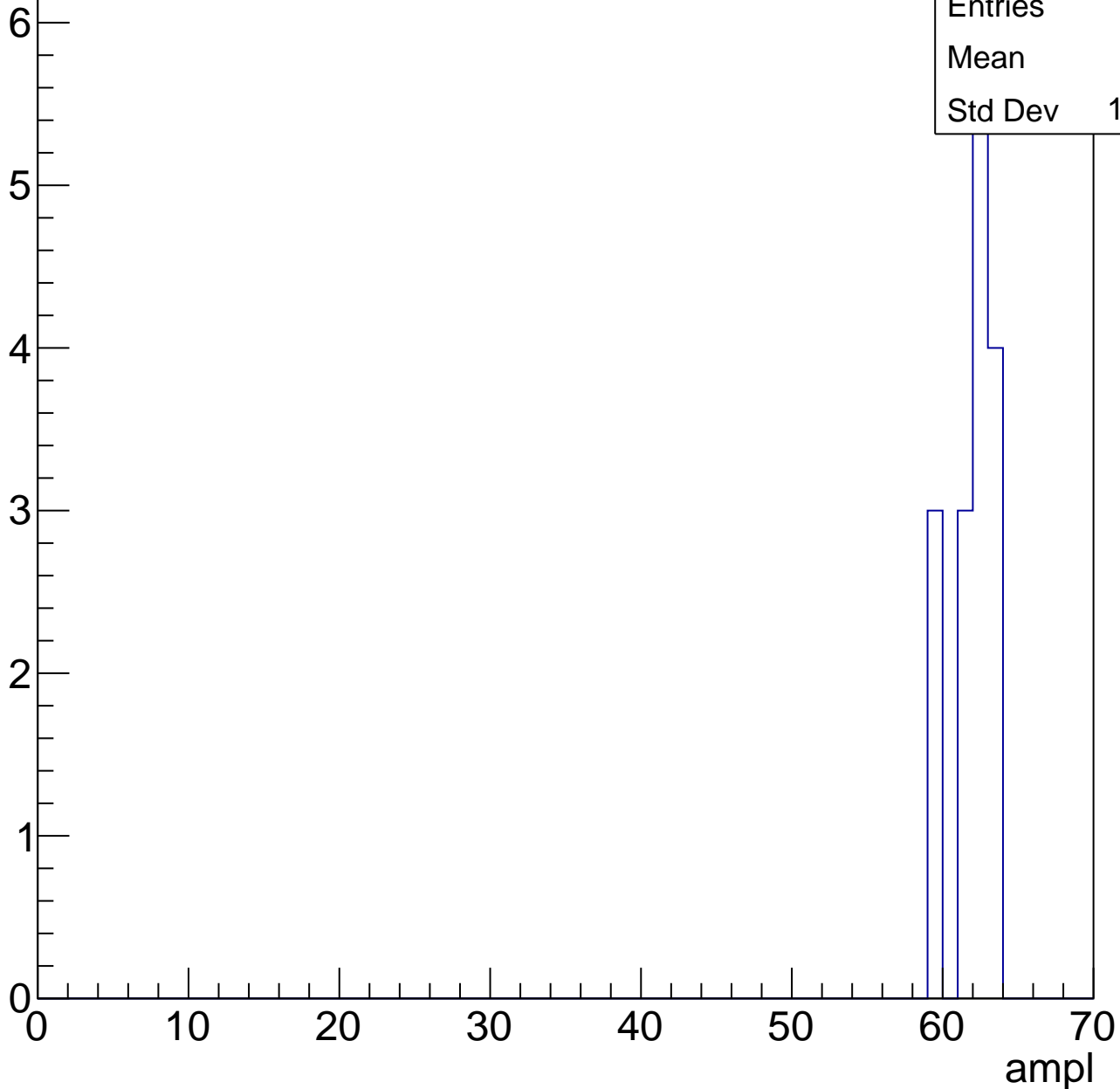


# B0L001S, U24-ch83, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	16
Mean	61.5
Std Dev	1.369



# B0L001S, U24-ch83, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch83, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U24-ch84, adc0

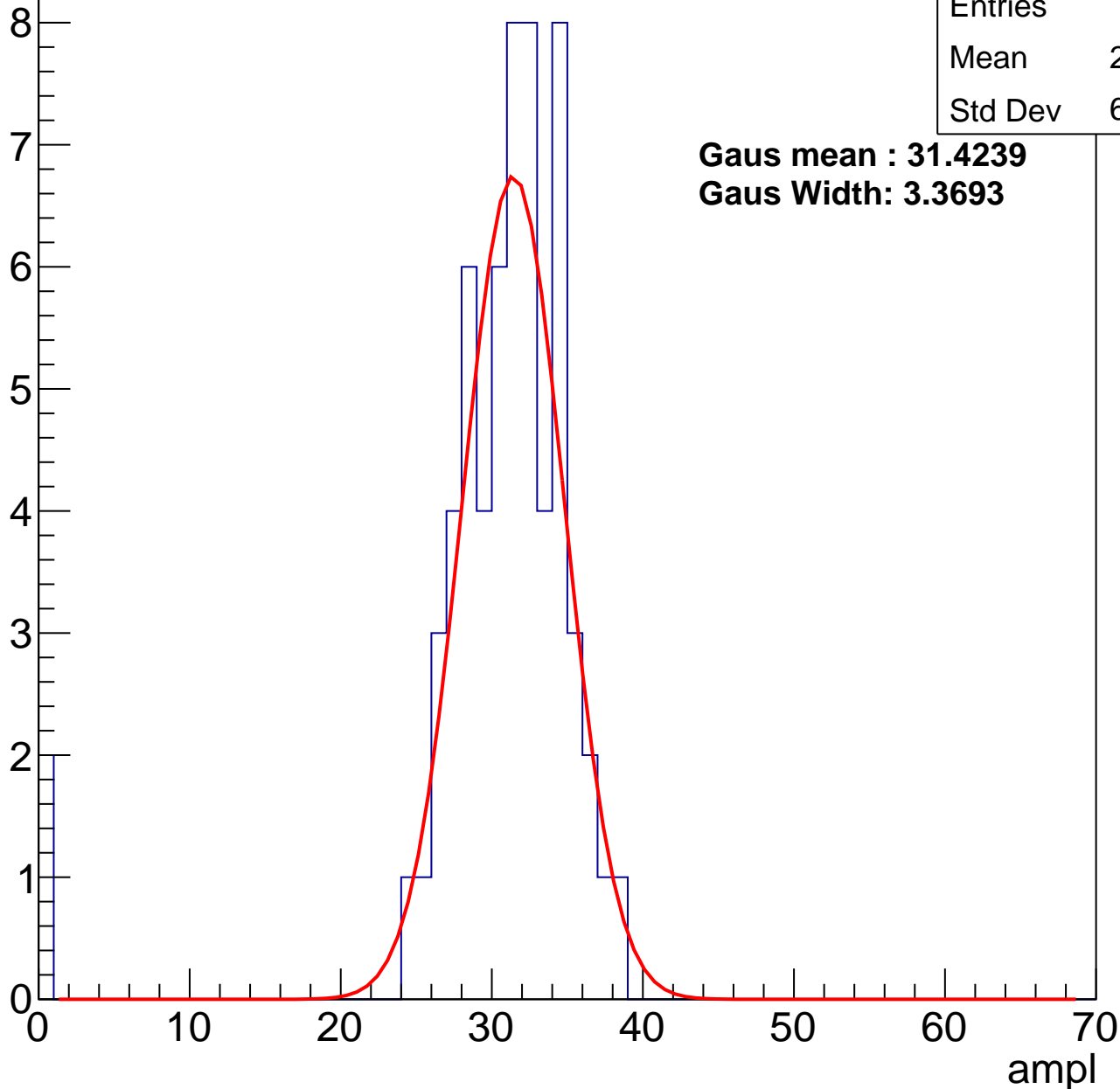
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	29.98
Std Dev	6.269

**Gaus mean : 31.4239**

**Gaus Width: 3.3693**



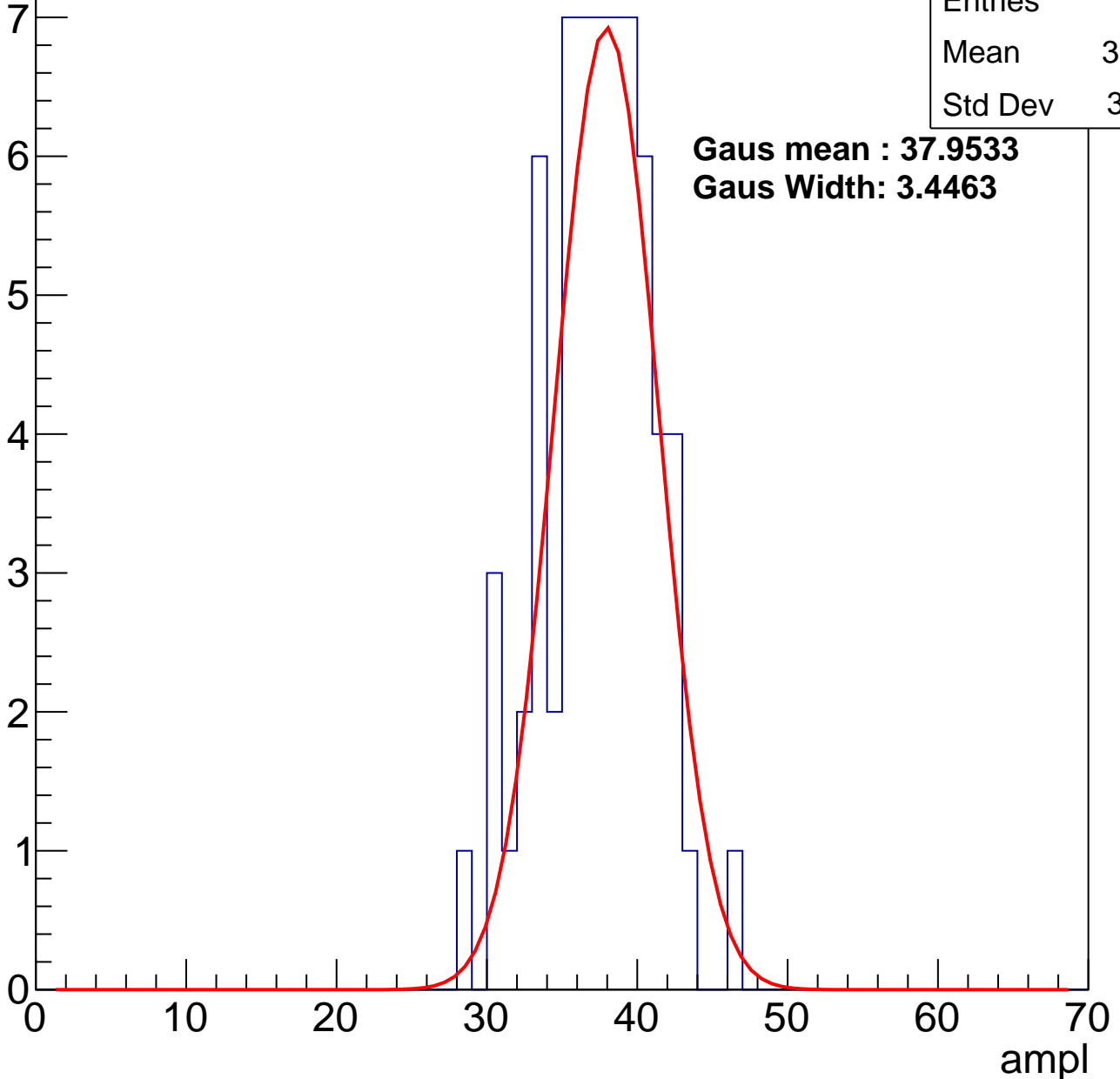
# B0L001S, U24-ch84, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	36.89
Std Dev	3.551

**Gaus mean : 37.9533**  
**Gaus Width: 3.4463**



# B0L001S, U24-ch84, adc2

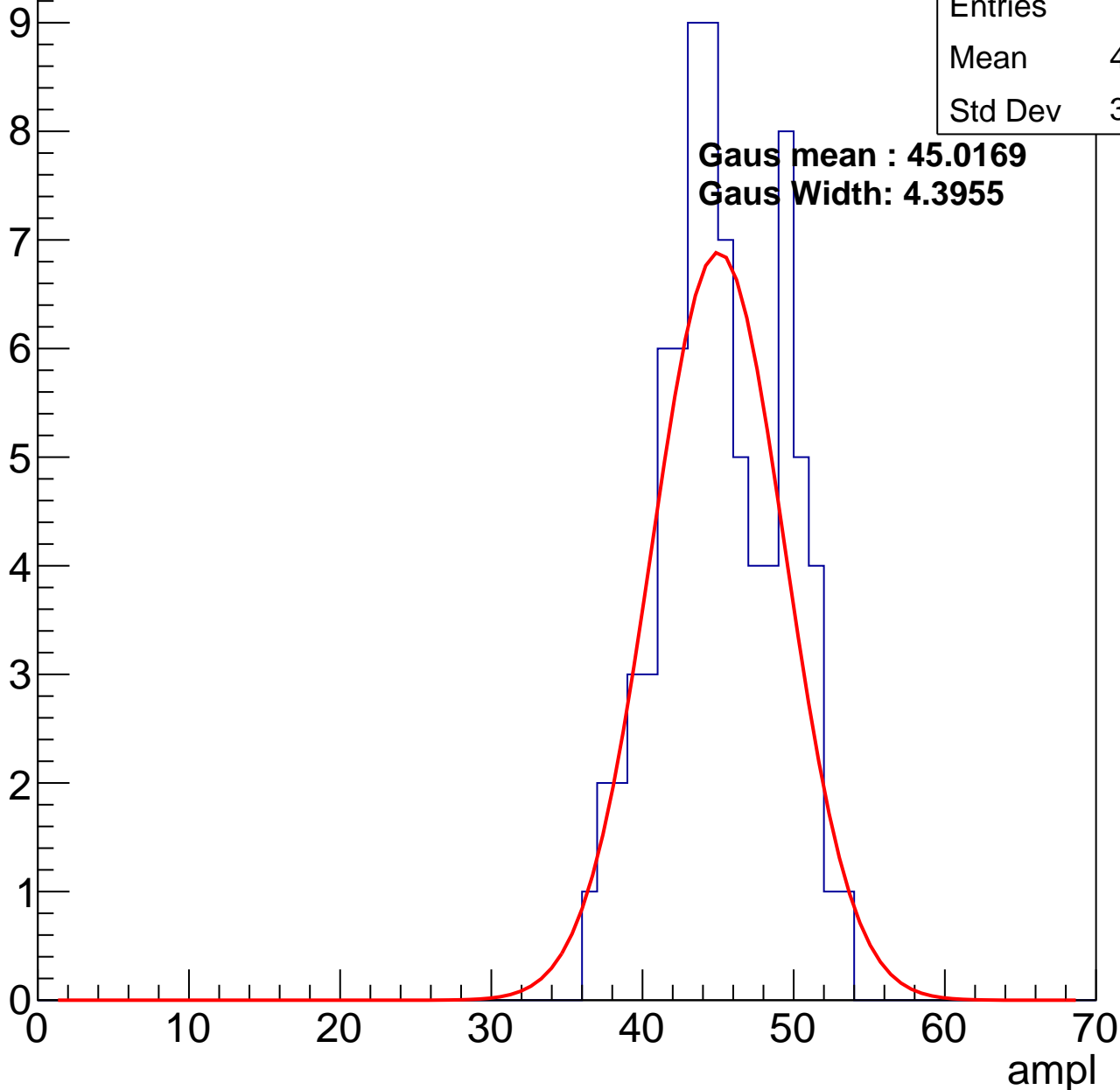
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	80
Mean	44.75
Std Dev	3.948

**Gaus mean : 45.0169**

**Gaus Width: 4.3955**

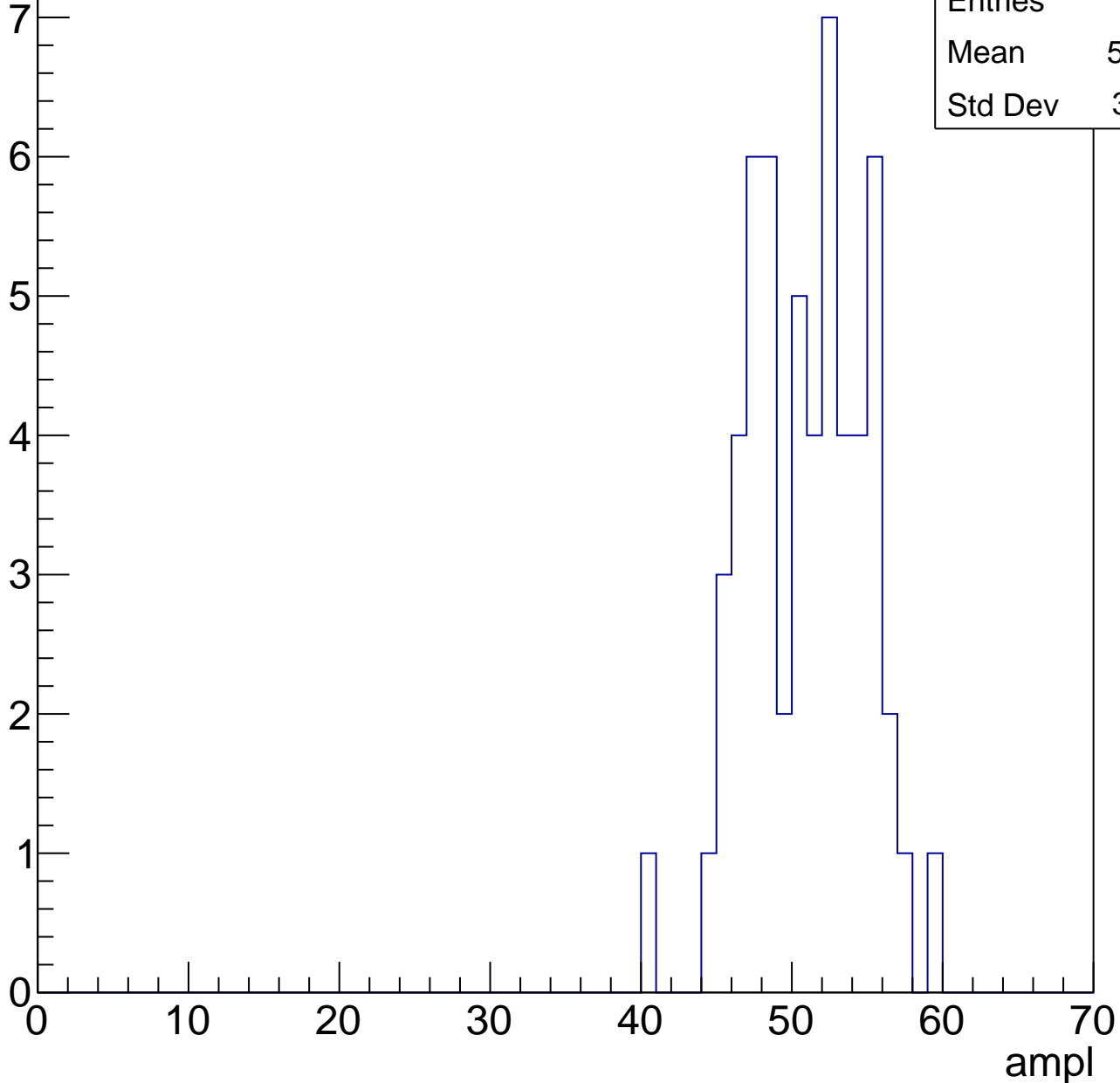


# B0L001S, U24-ch84, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

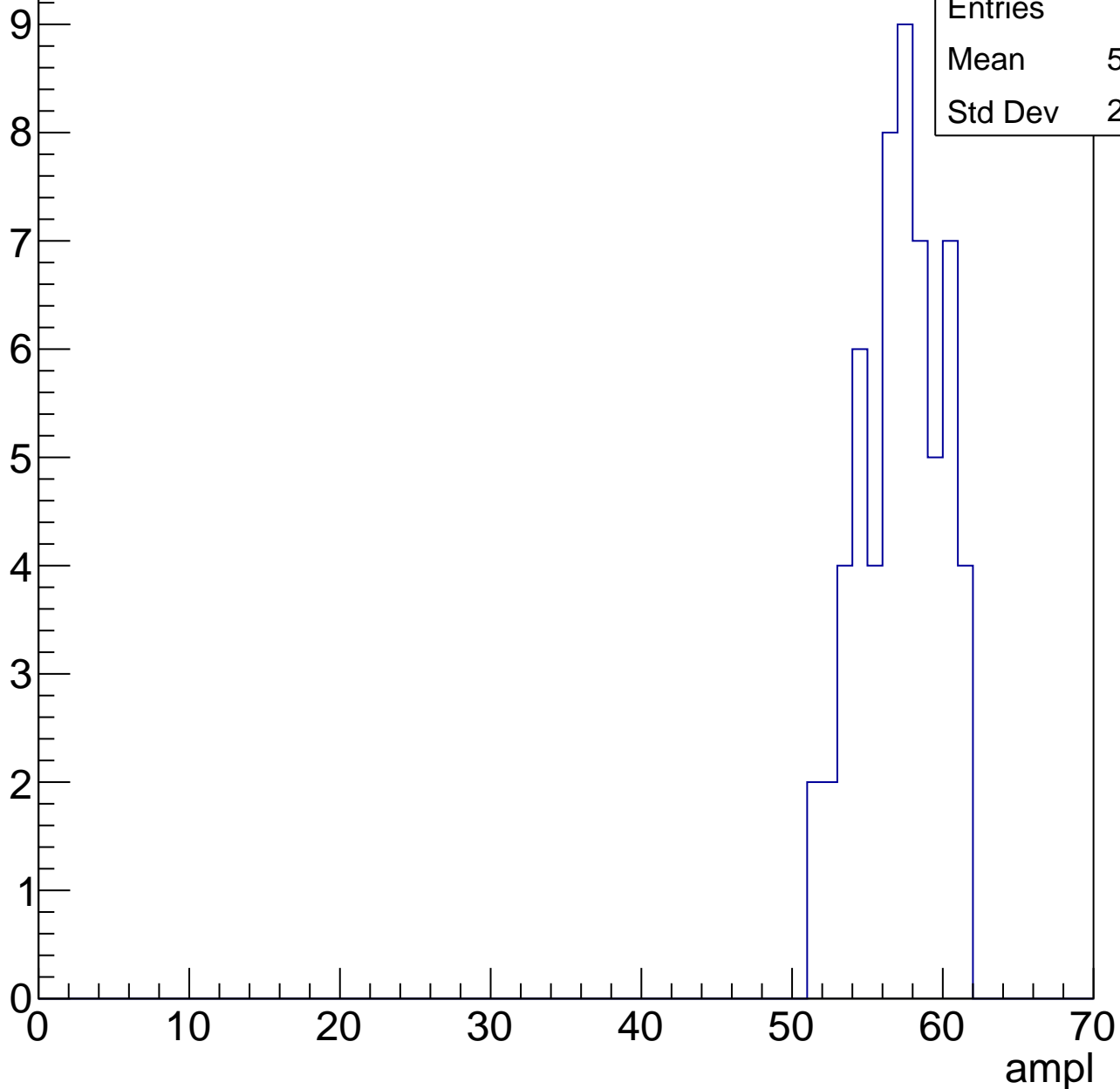
Entries	57
Mean	50.44
Std Dev	3.811



# B0L001S, U24-ch84, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



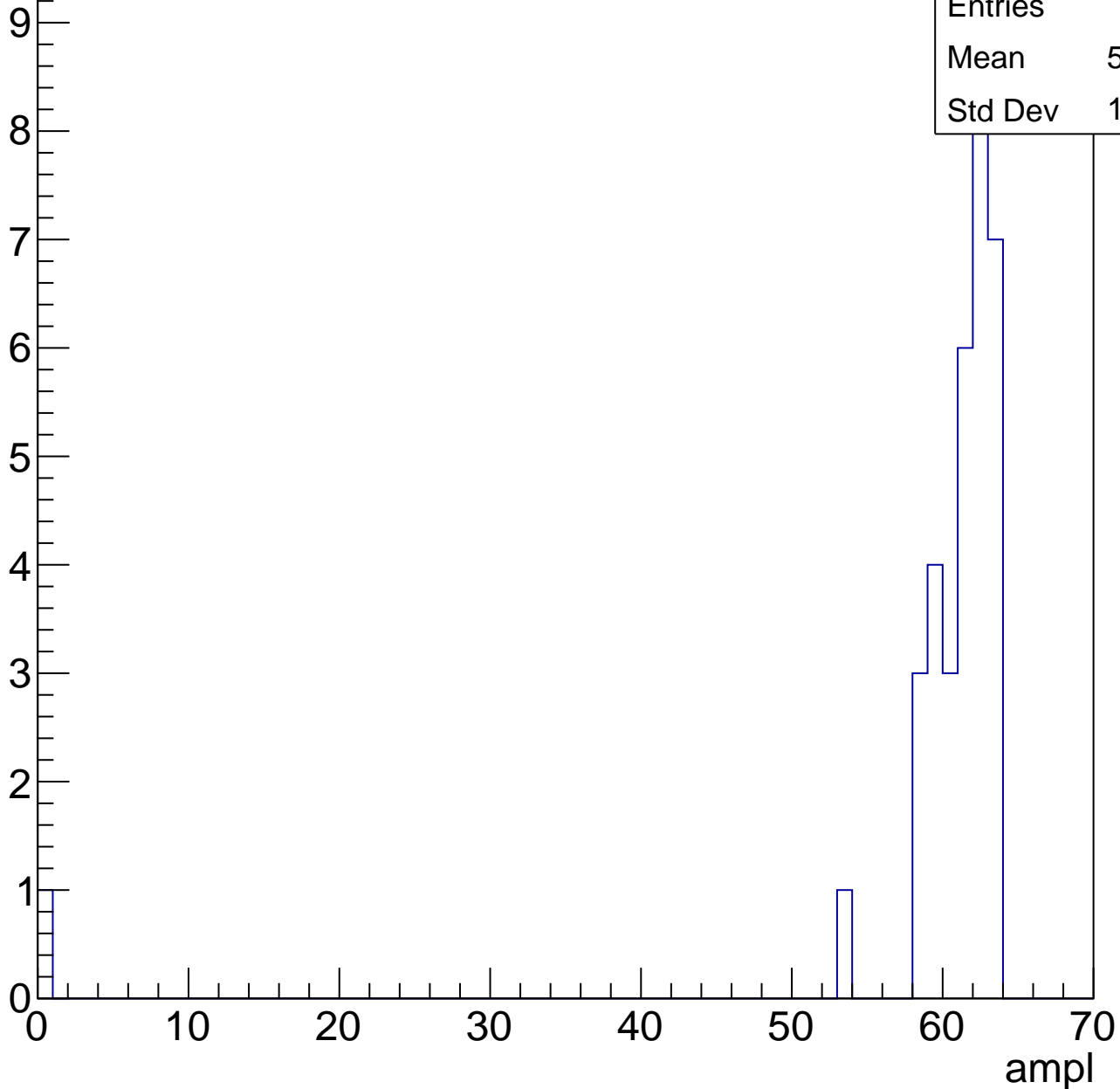
Entries	58
Mean	56.69
Std Dev	2.667

# B0L001S, U24-ch84, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	34
Mean	59.06
Std Dev	10.49



# B0L001S, U24-ch84, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch84, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L001S, U24-ch85, adc0

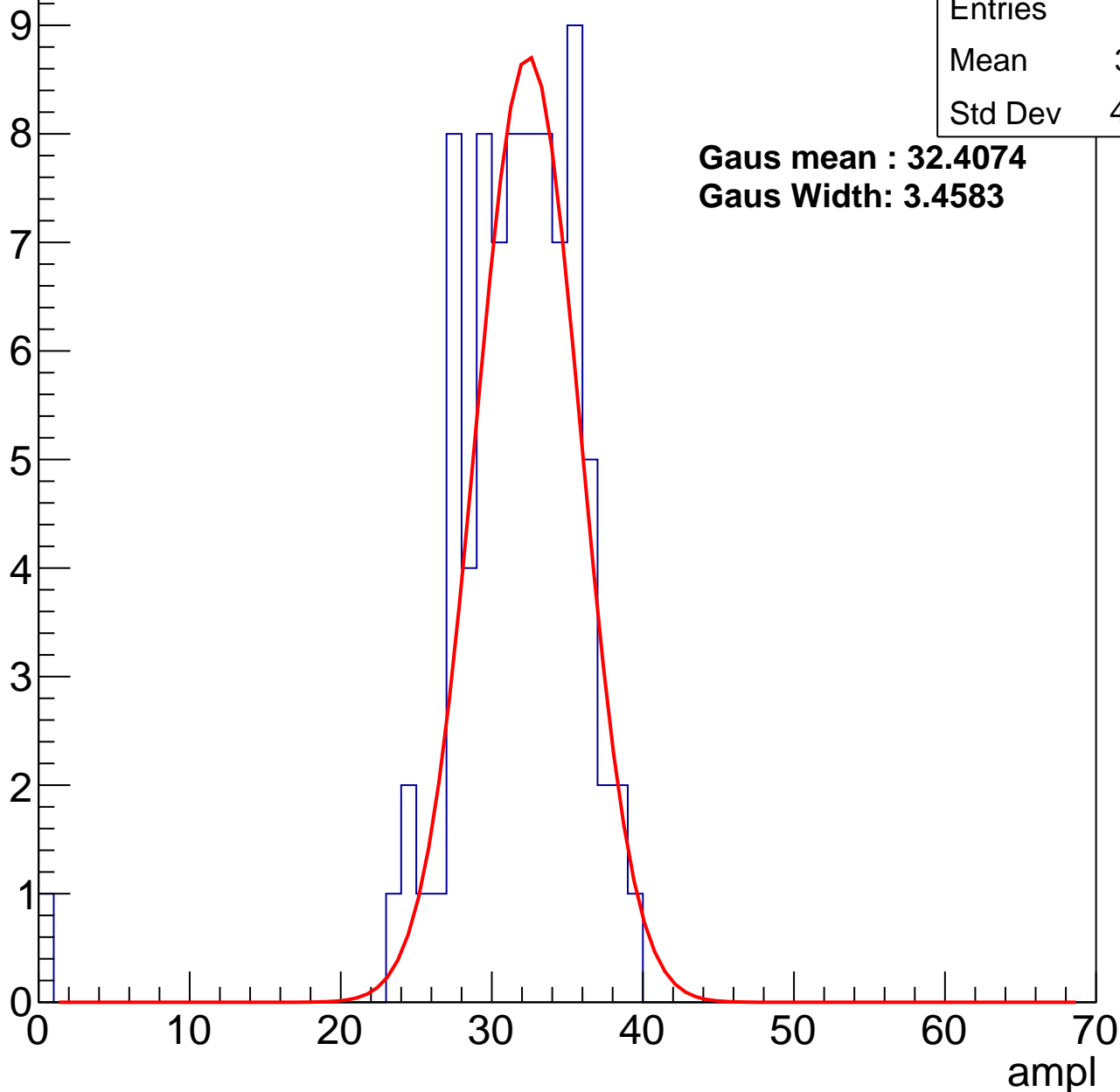
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	83
Mean	31.11
Std Dev	4.899

**Gaus mean : 32.4074**

**Gaus Width: 3.4583**



# B0L001S, U24-ch85, adc1

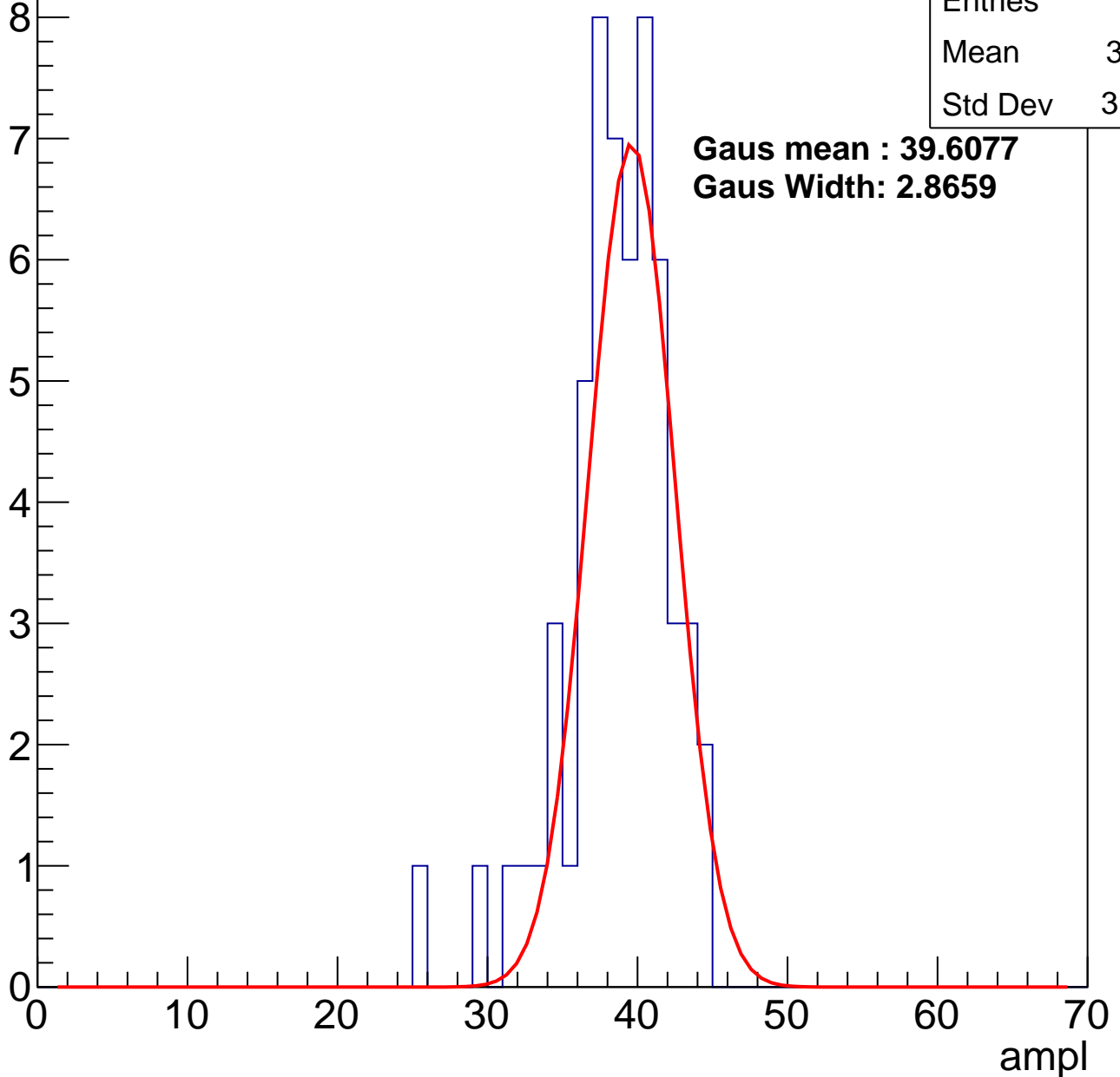
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	38.11
Std Dev	3.582

**Gaus mean : 39.6077**

**Gaus Width: 2.8659**



# B0L001S, U24-ch85, adc2

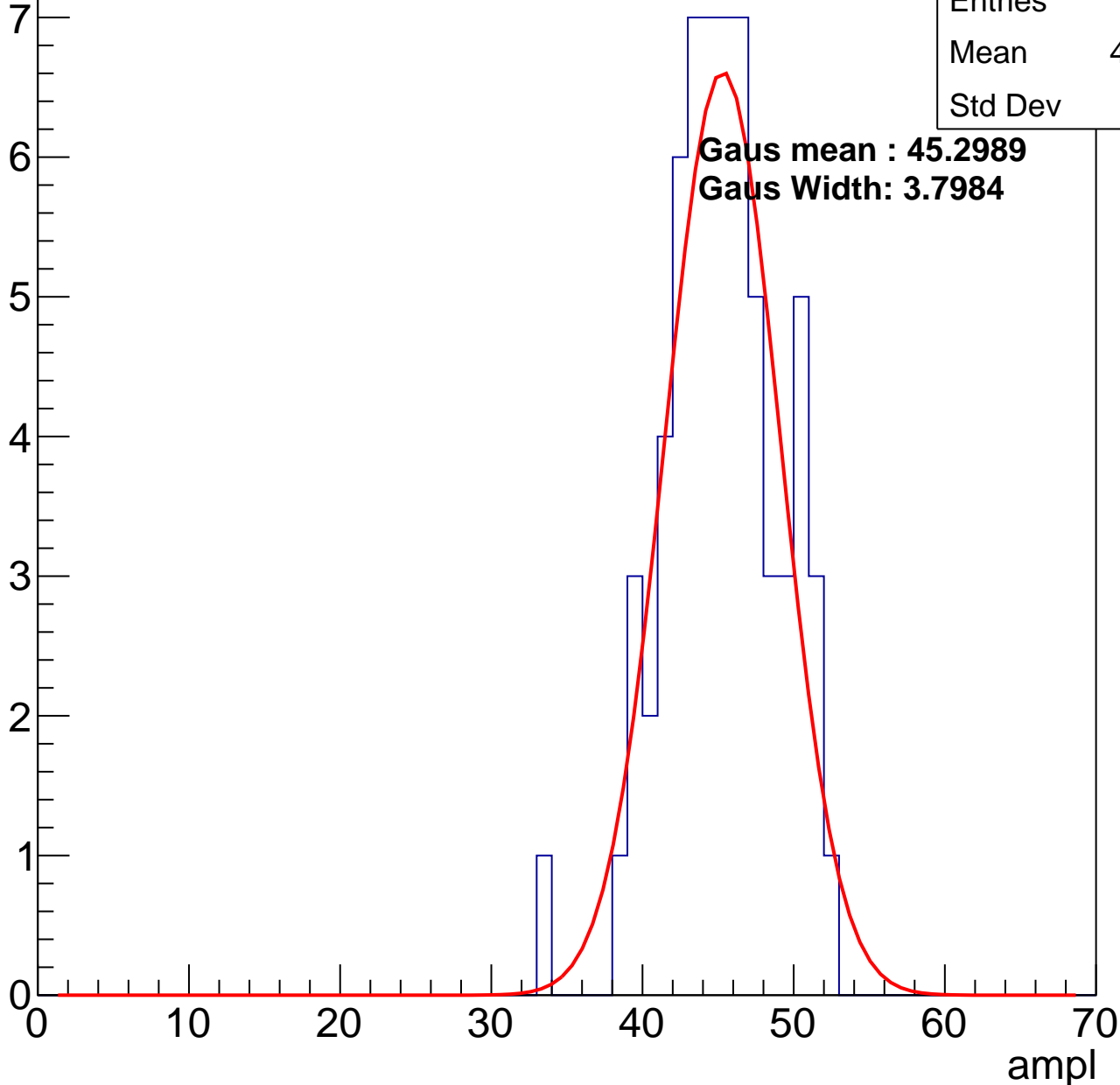
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	44.78
Std Dev	3.69

**Gaus mean : 45.2989**

**Gaus Width: 3.7984**

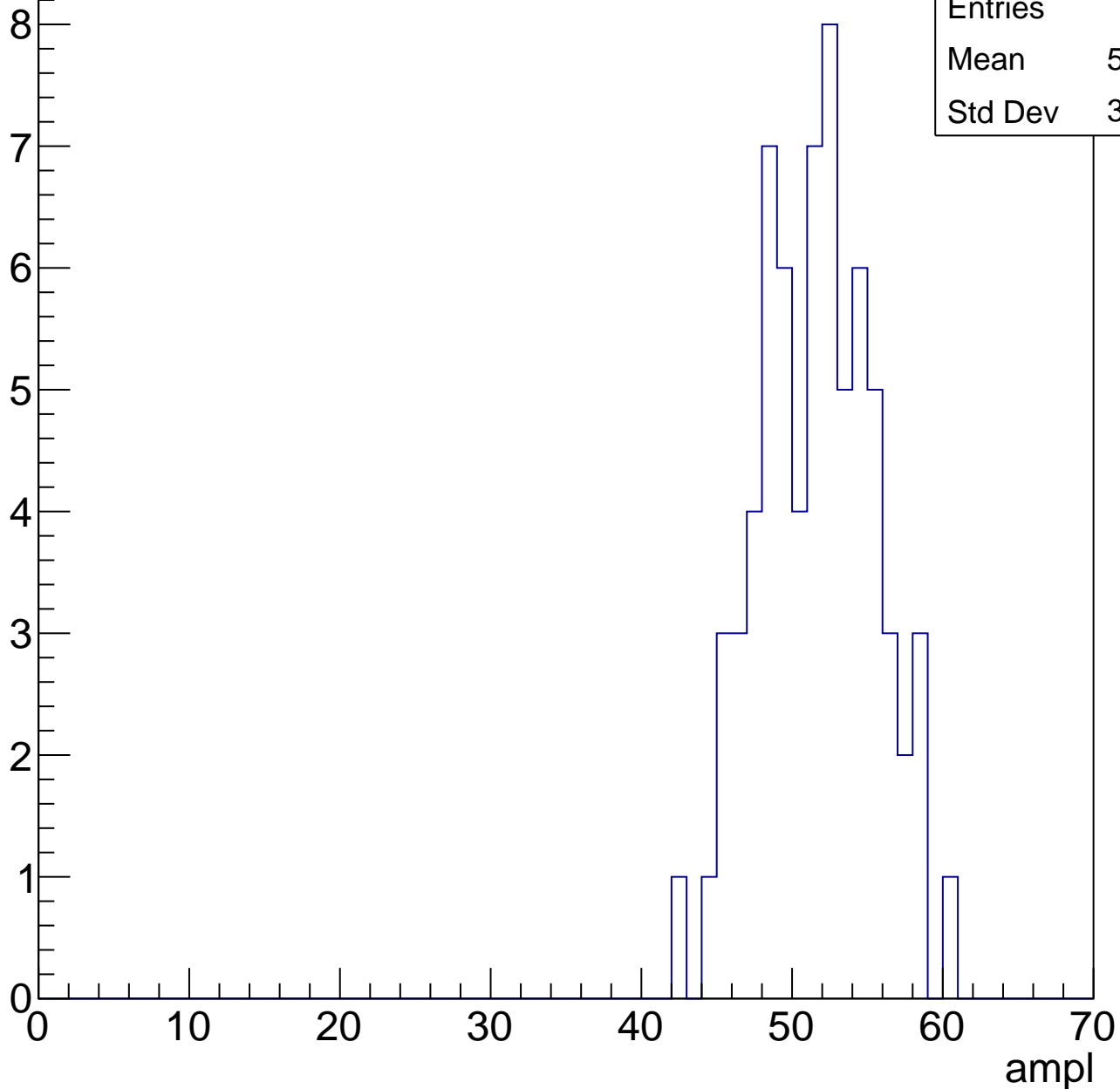


# B0L001S, U24-ch85, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	51.16
Std Dev	3.813

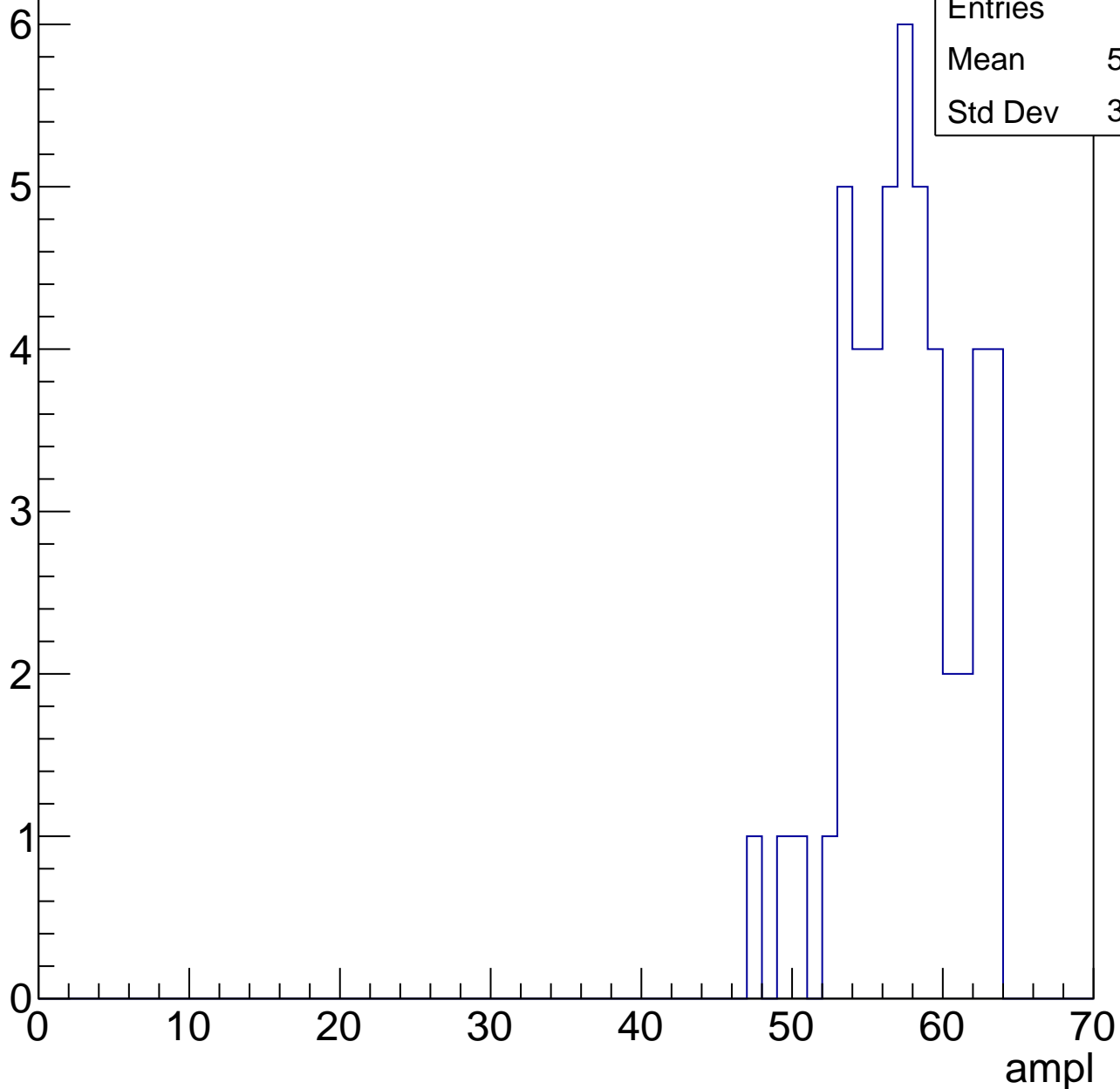


# B0L001S, U24-ch85, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	49
Mean	56.92
Std Dev	3.752

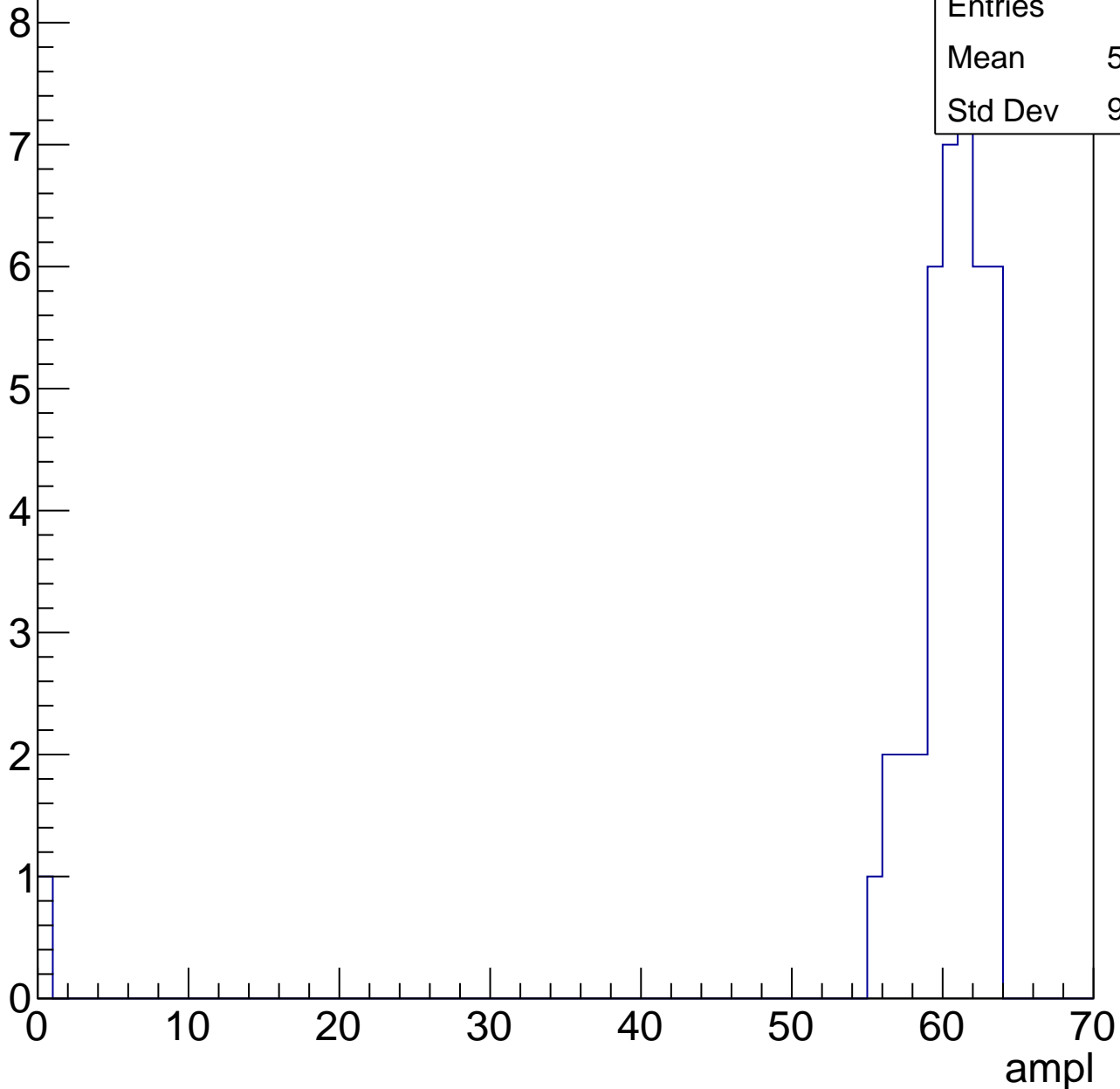


# B0L001S, U24-ch85, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	41
Mean	58.76
Std Dev	9.515



# B0L001S, U24-ch85, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U24-ch85, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U24-ch86, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	82
Mean	30.12
Std Dev	3.934

**Gaus mean : 31.2006**

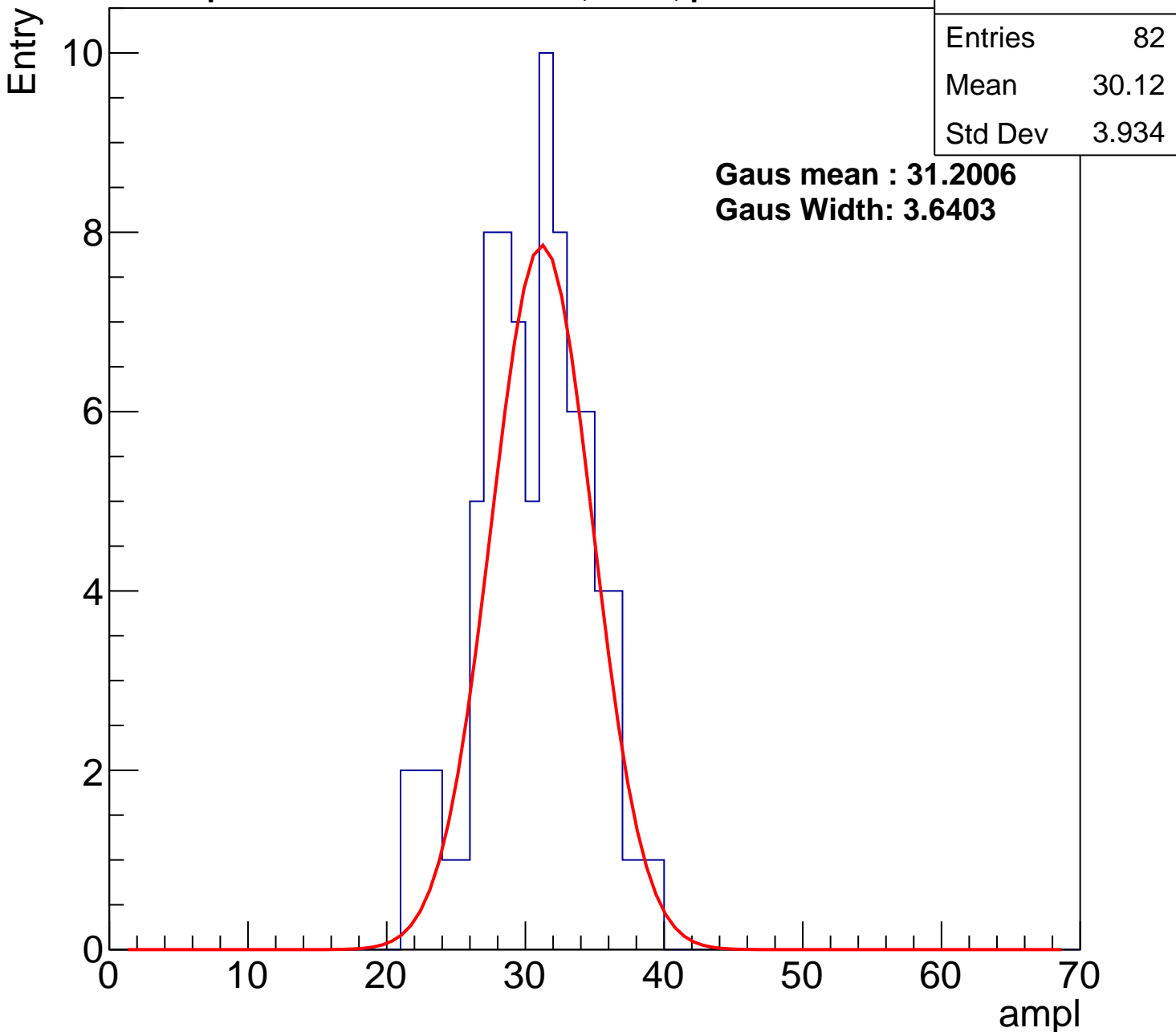
**Gaus Width: 3.6403**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U24-ch86, adc1

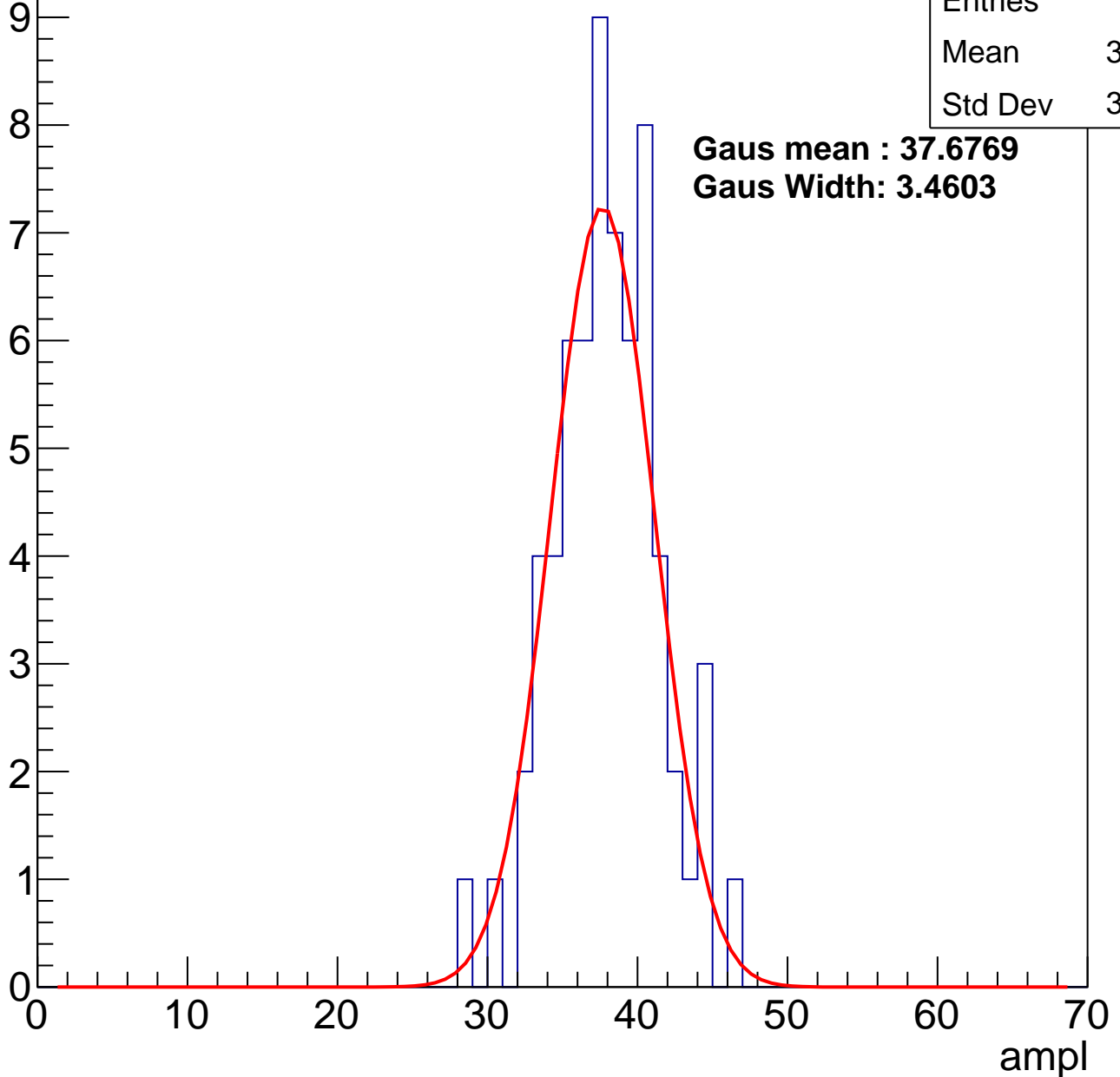
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	37.51
Std Dev	3.451

**Gaus mean : 37.6769**

**Gaus Width: 3.4603**



# B0L001S, U24-ch86, adc2

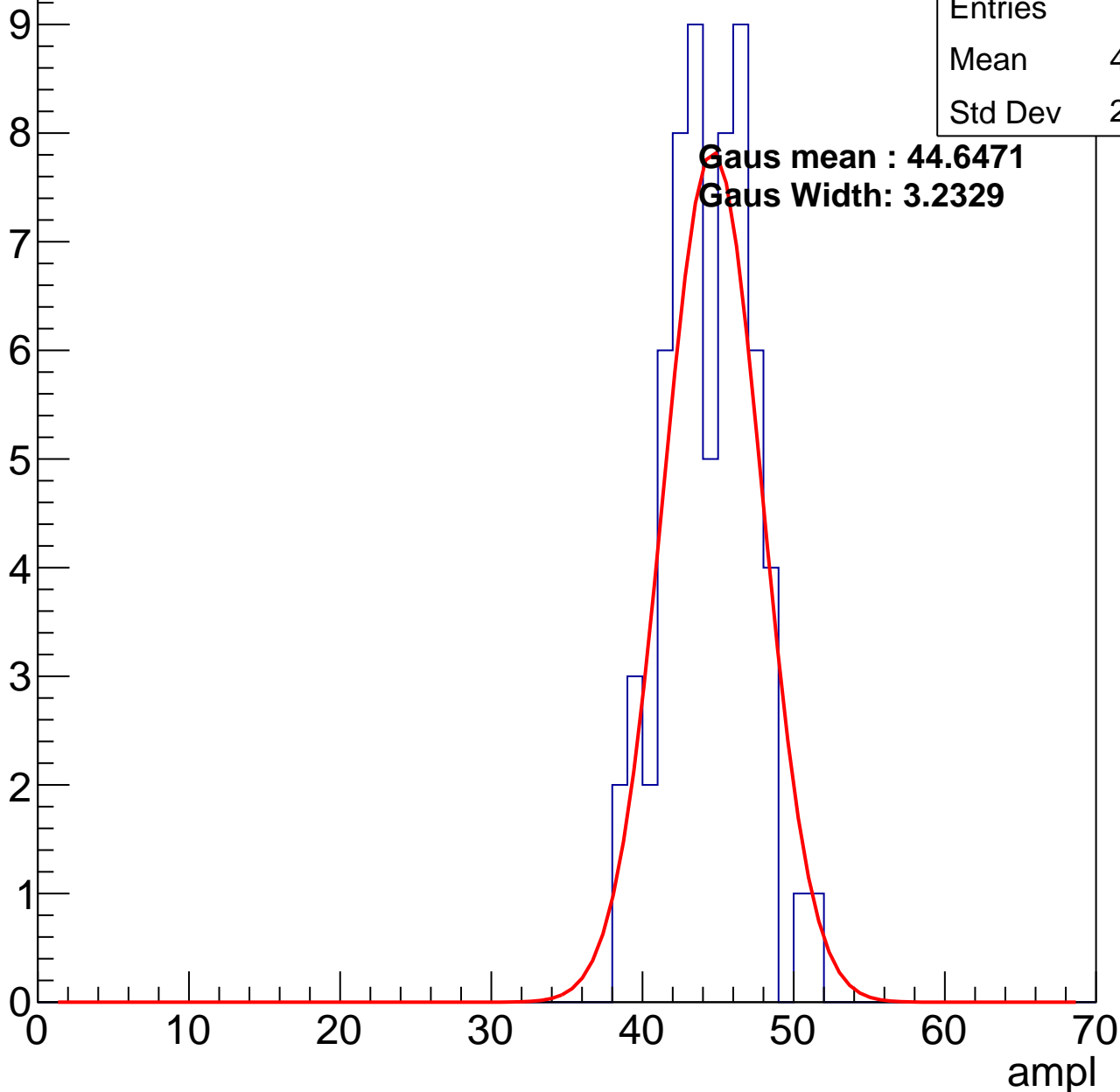
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	43.92
Std Dev	2.852

**Gaus mean : 44.6471**

**Gaus Width: 3.2329**



# B0L001S, U24-ch86, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

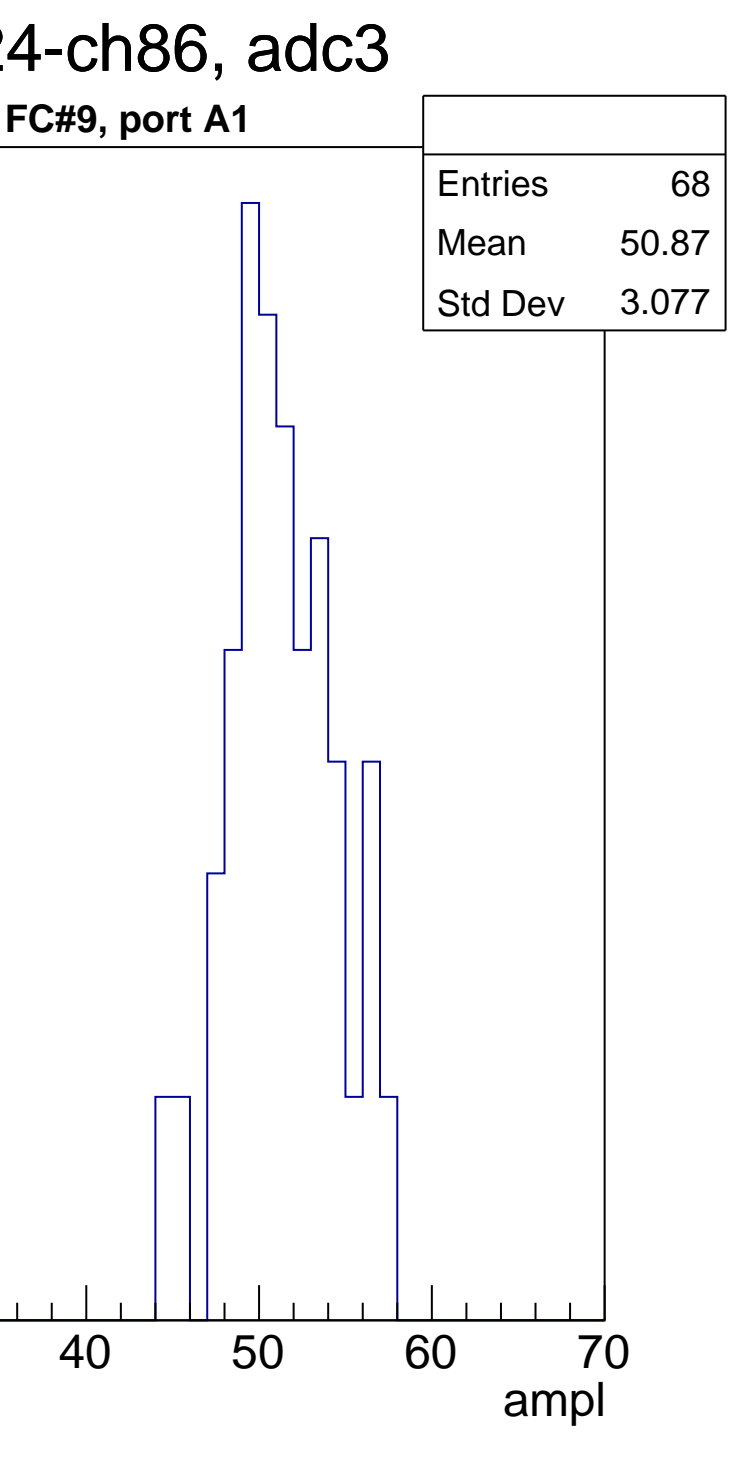
Entries	68
Mean	50.87
Std Dev	3.077

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

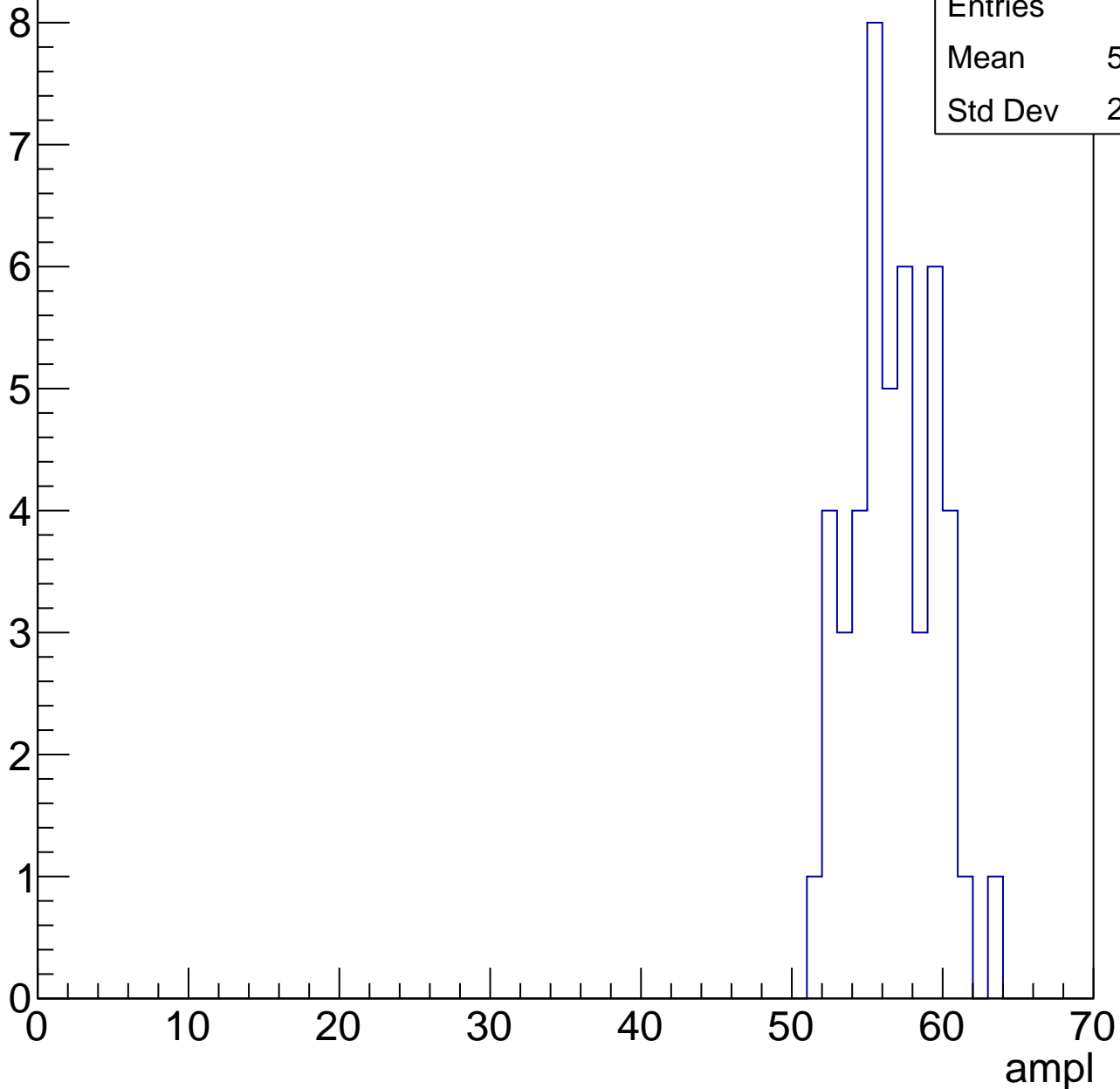


# B0L001S, U24-ch86, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	46
Mean	56.26
Std Dev	2.746

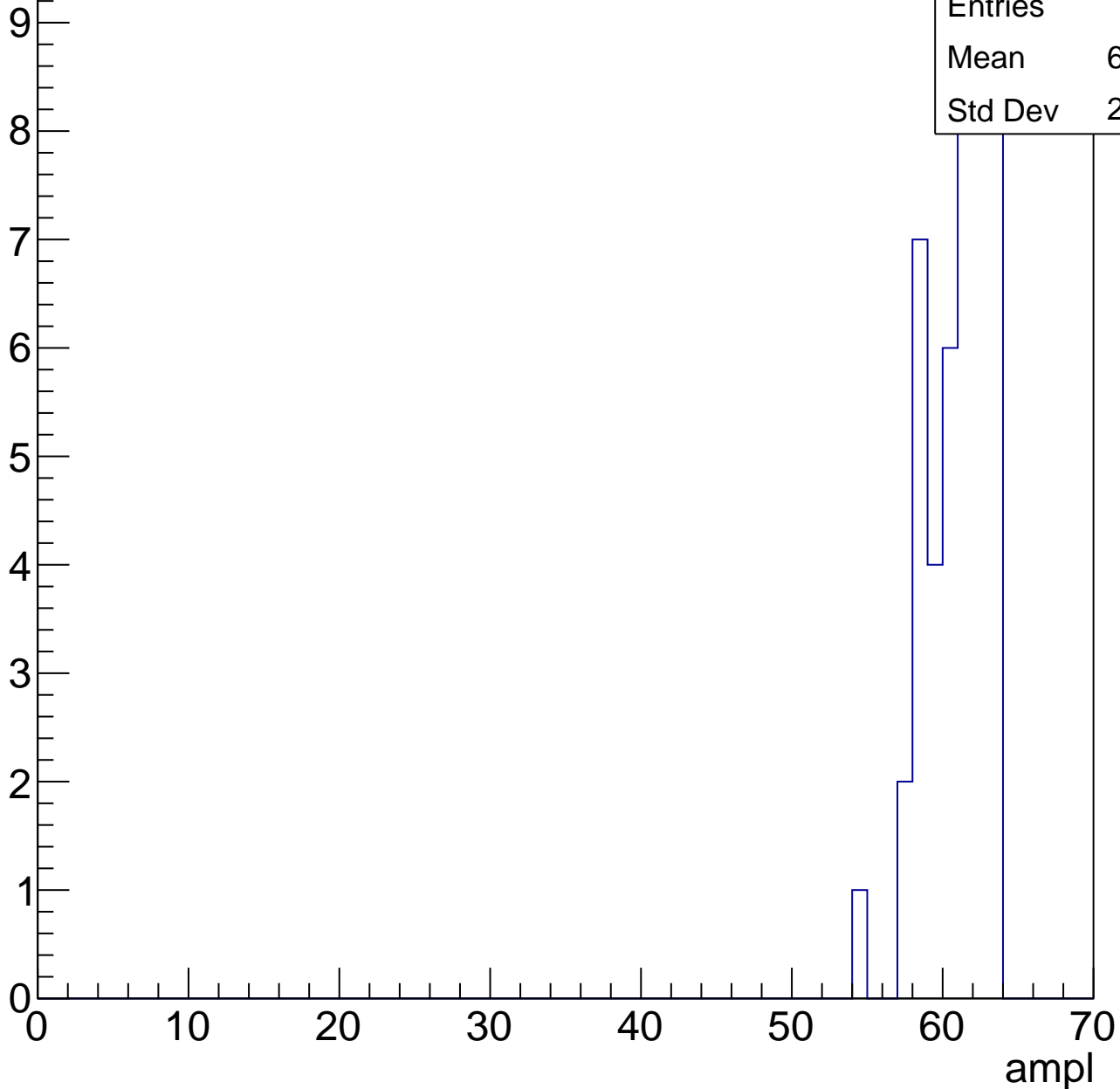


# B0L001S, U24-ch86, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

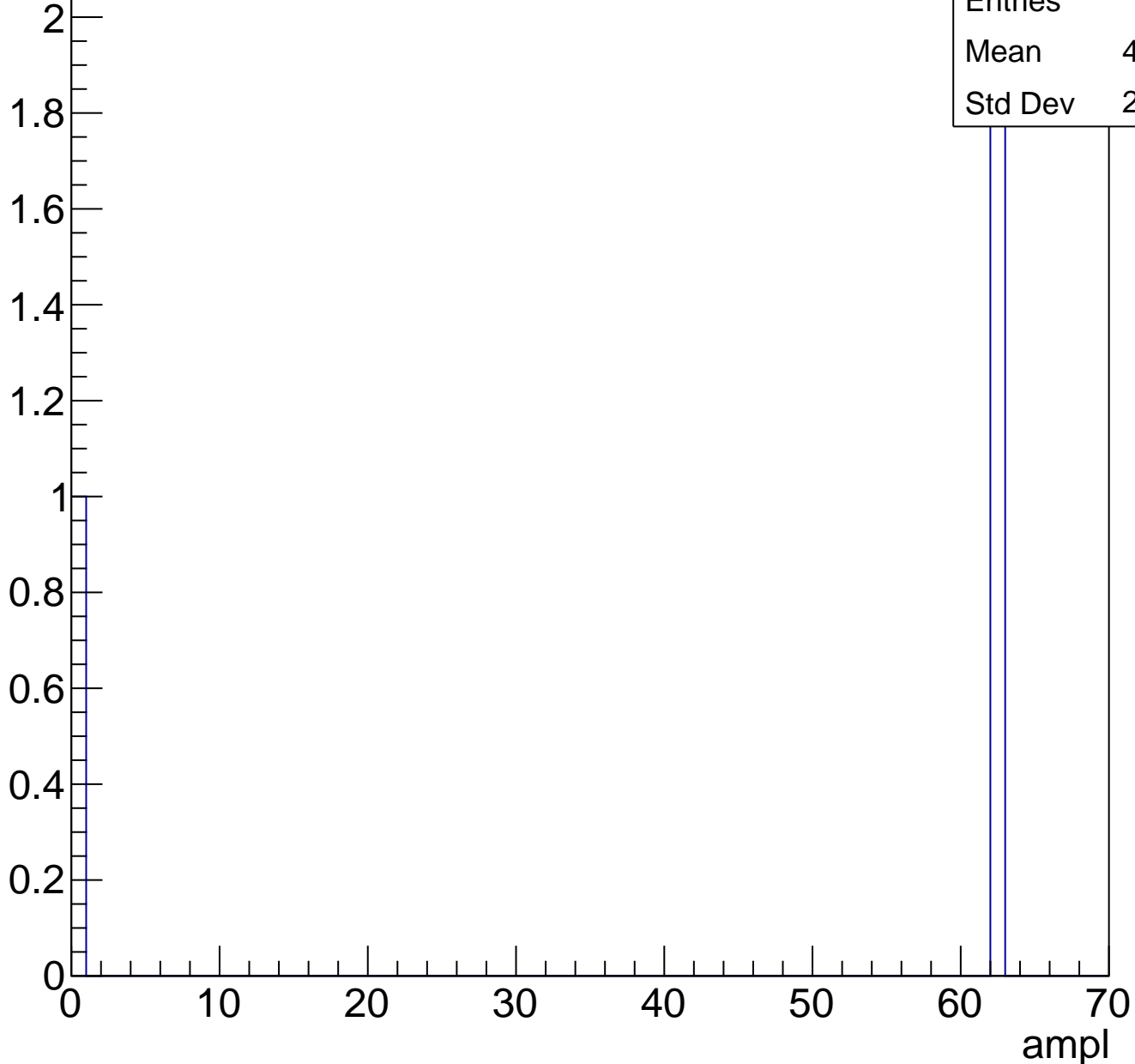
Entries	46
Mean	60.48
Std Dev	2.072



# B0L001S, U24-ch86, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch86, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U24-ch87, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	80
Mean	31.05
Std Dev	3.721

**Gaus mean : 31.8142**

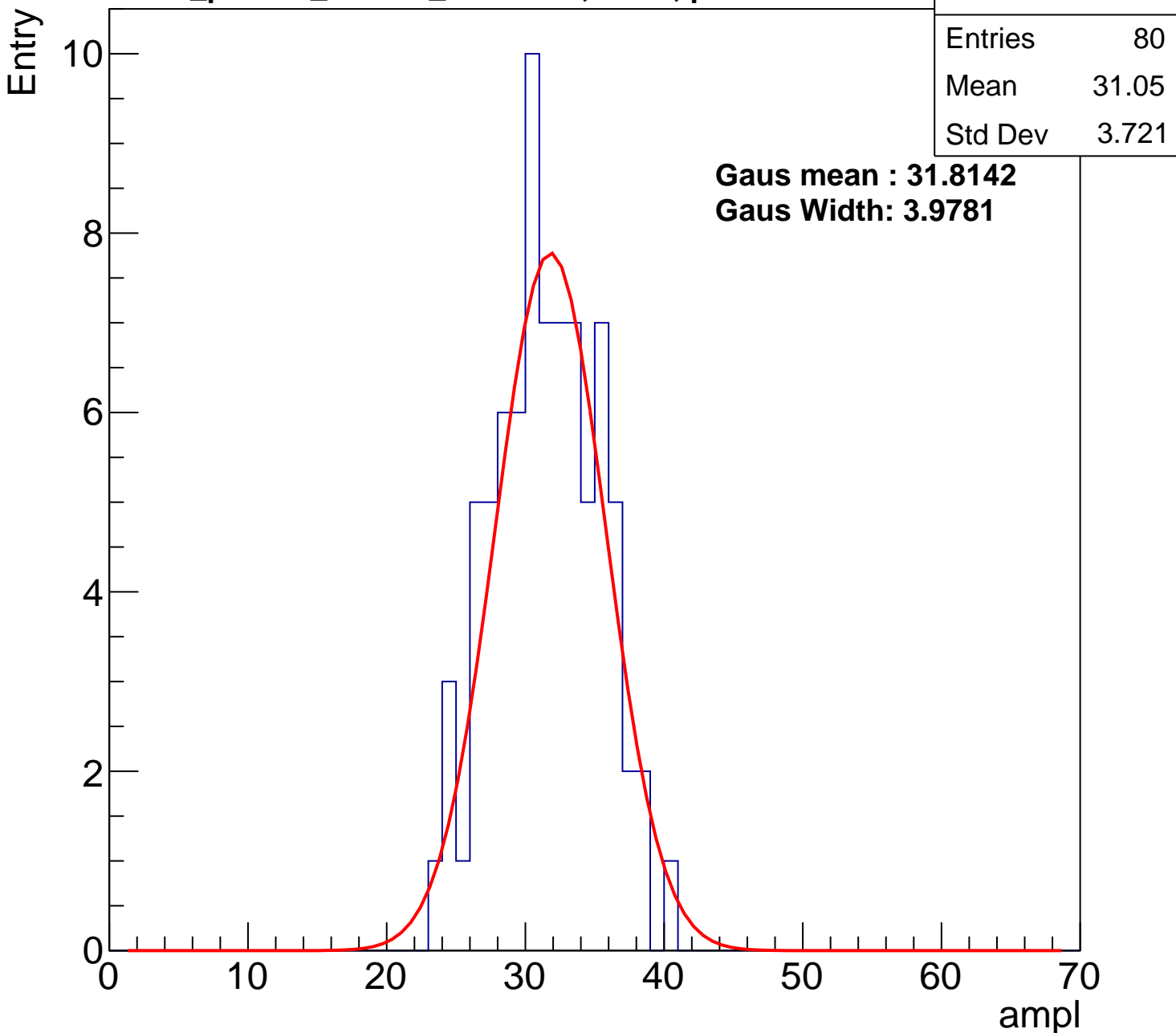
**Gaus Width: 3.9781**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



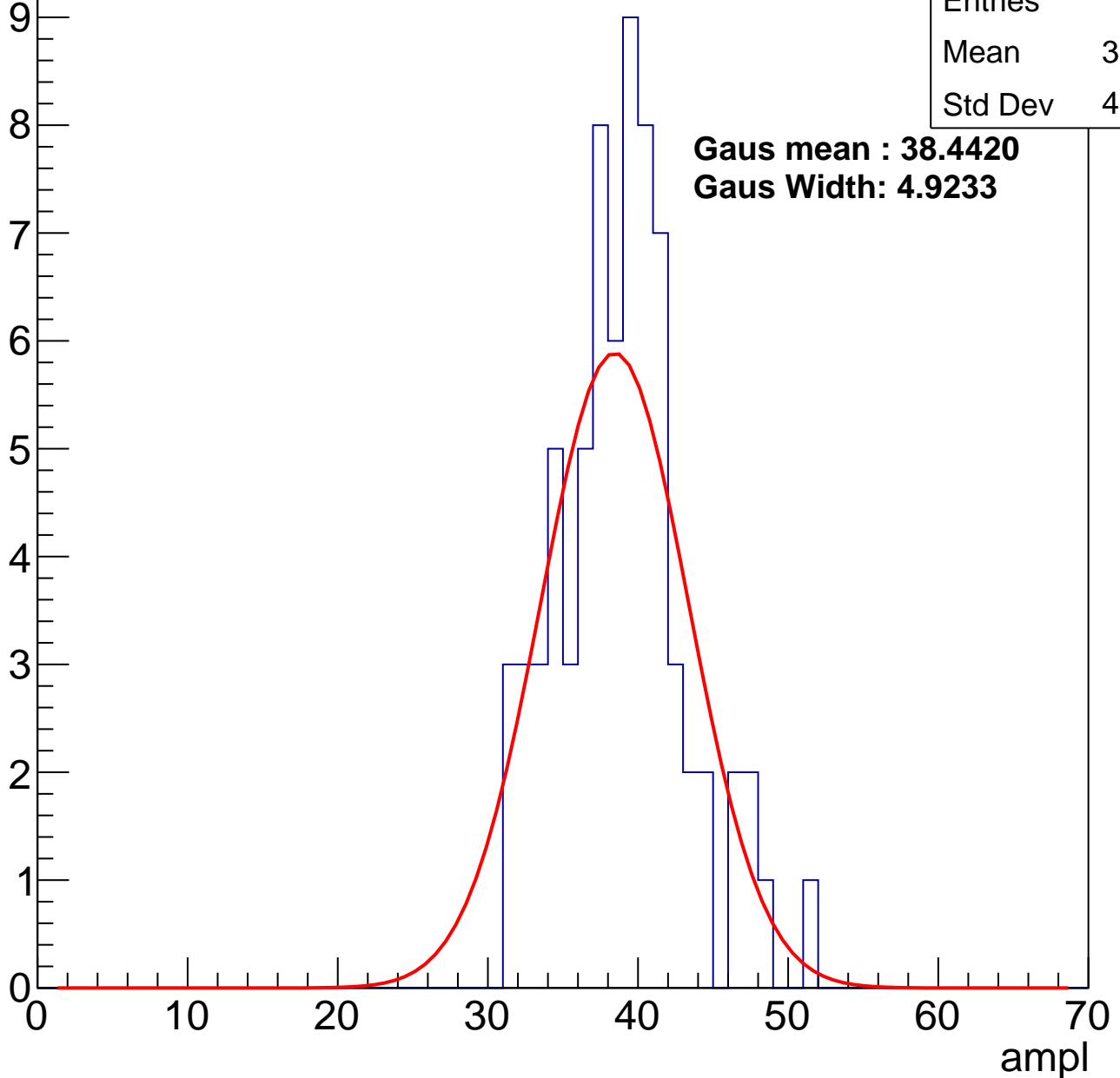
# B0L001S, U24-ch87, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	38.49
Std Dev	4.188

**Gaus mean : 38.4420**  
**Gaus Width: 4.9233**



# B0L001S, U24-ch87, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	77
Mean	45.97
Std Dev	3.622

**Gaus mean : 46.4195**

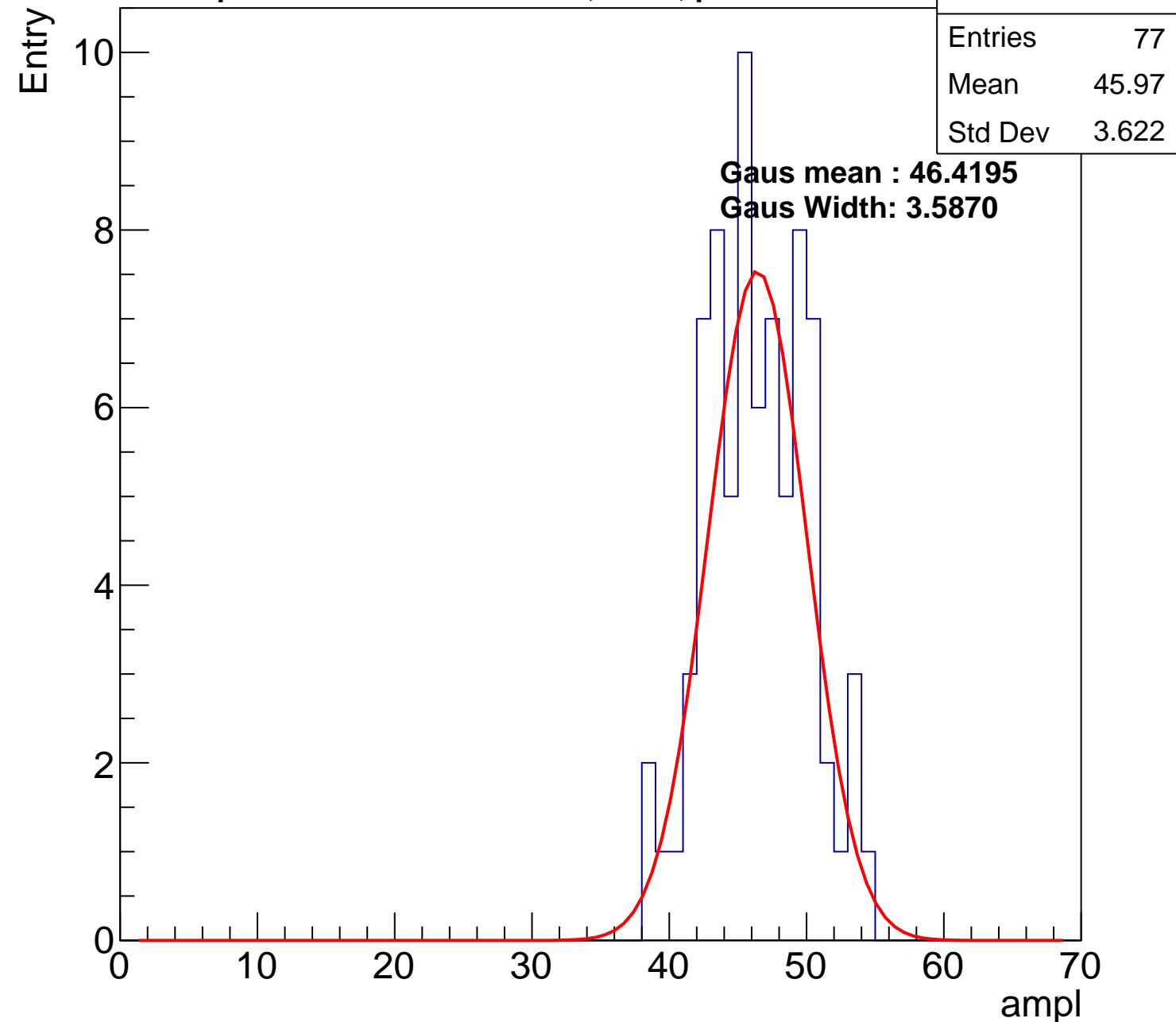
**Gaus Width: 3.5870**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

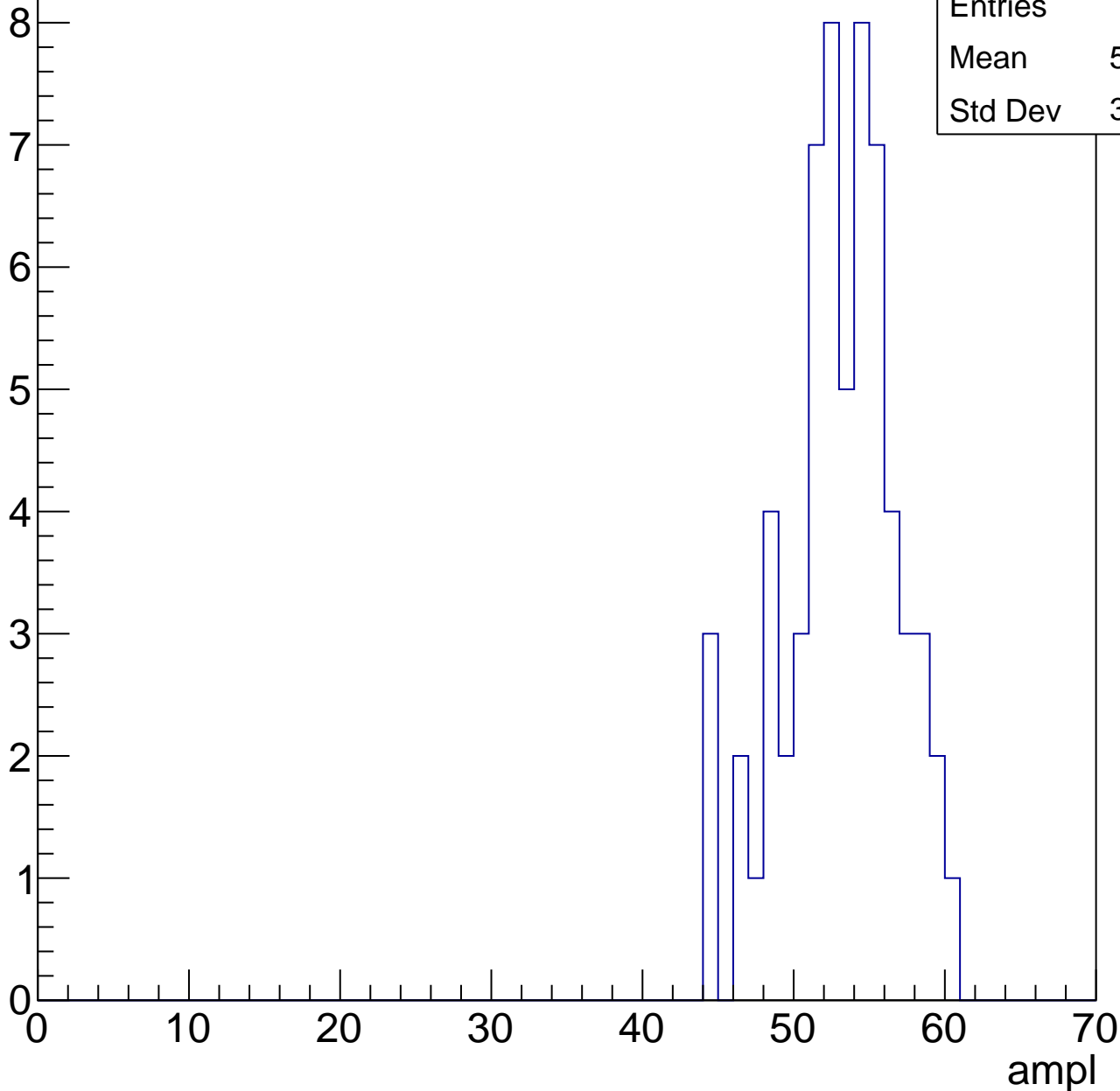


# B0L001S, U24-ch87, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

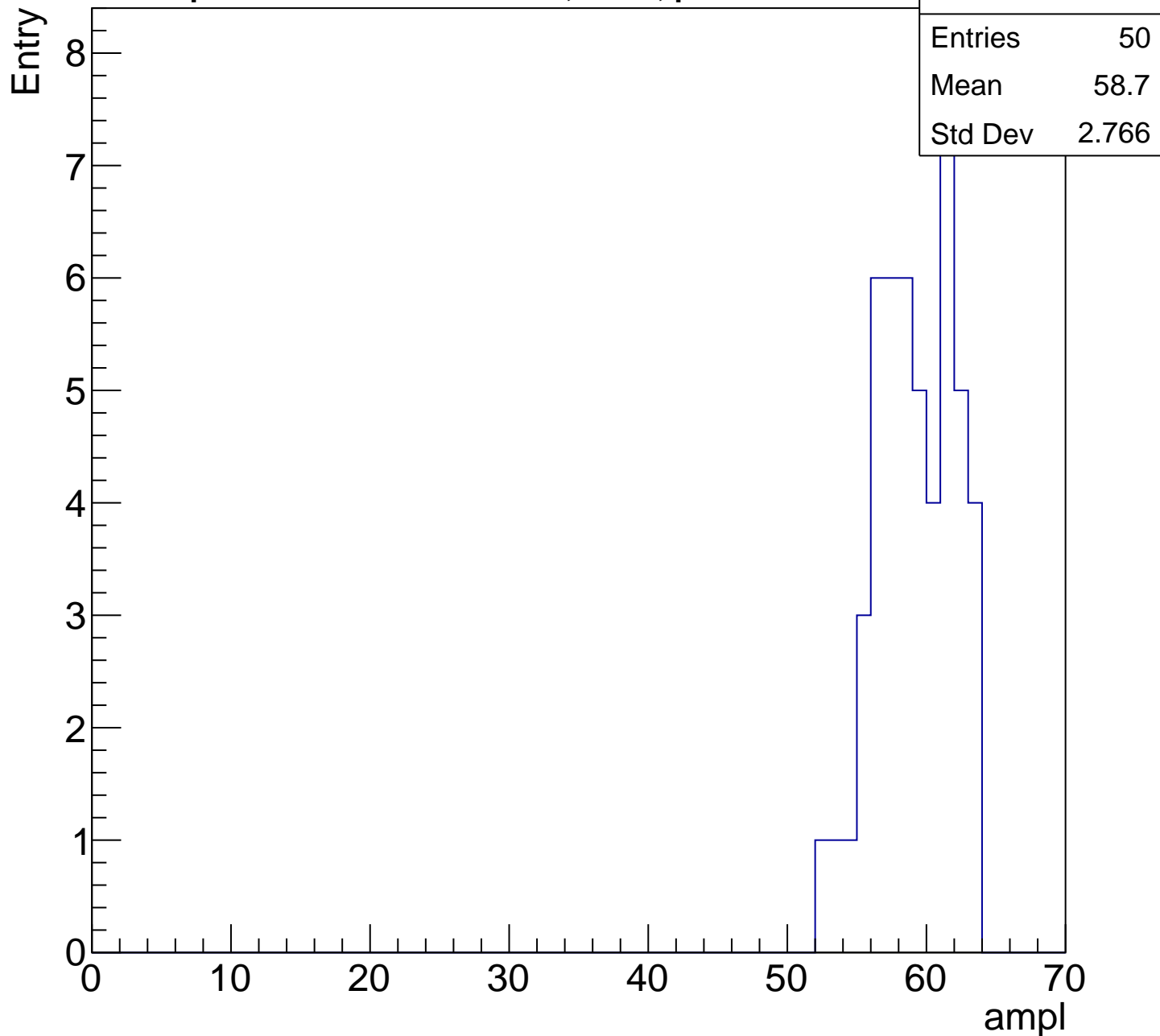
Entry

Entries	63
Mean	52.59
Std Dev	3.732



# B0L001S, U24-ch87, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

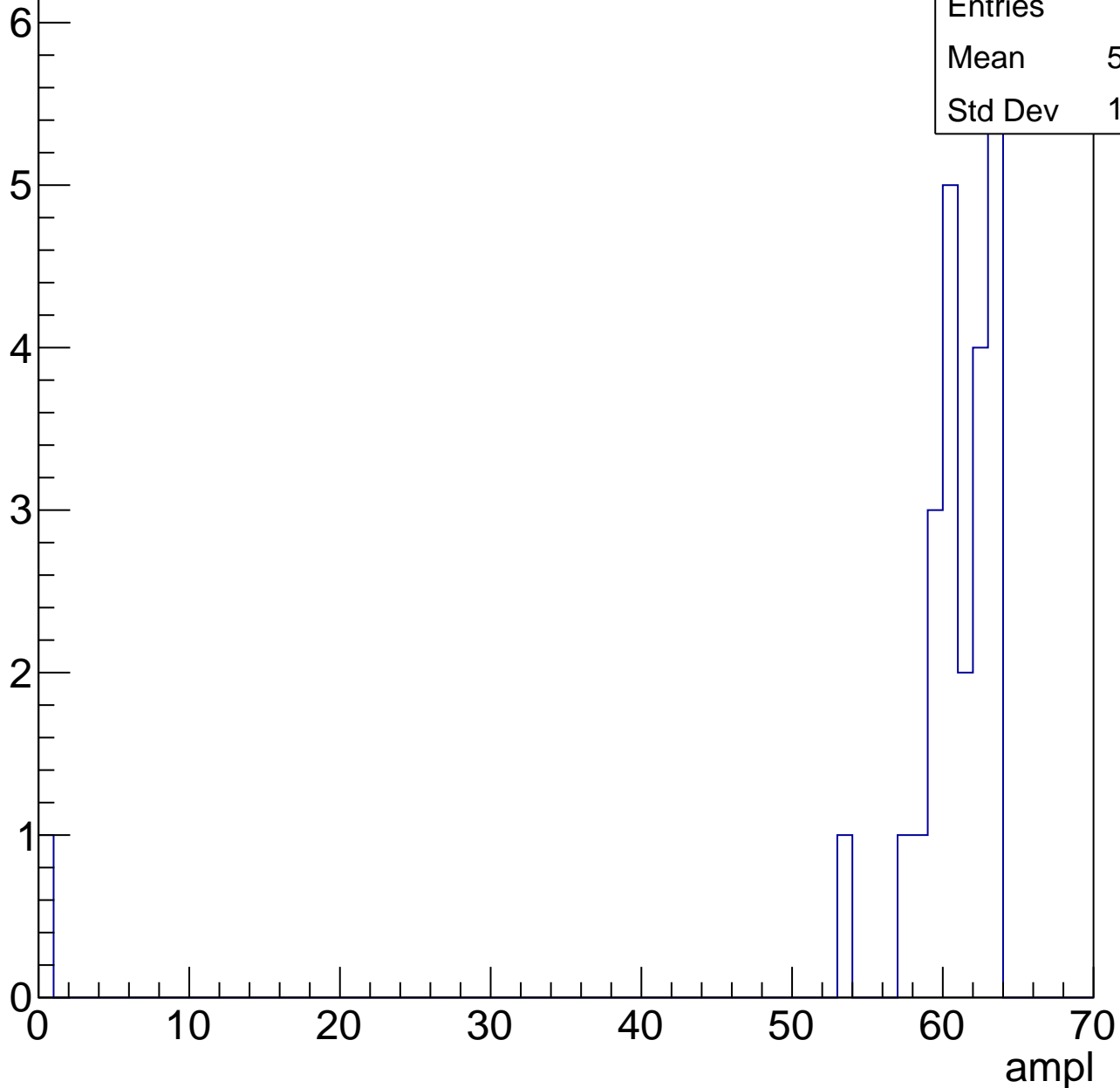


# B0L001S, U24-ch87, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	24
Mean	58.04
Std Dev	12.32



# B0L001S, U24-ch87, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch87, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U24-ch88, adc0

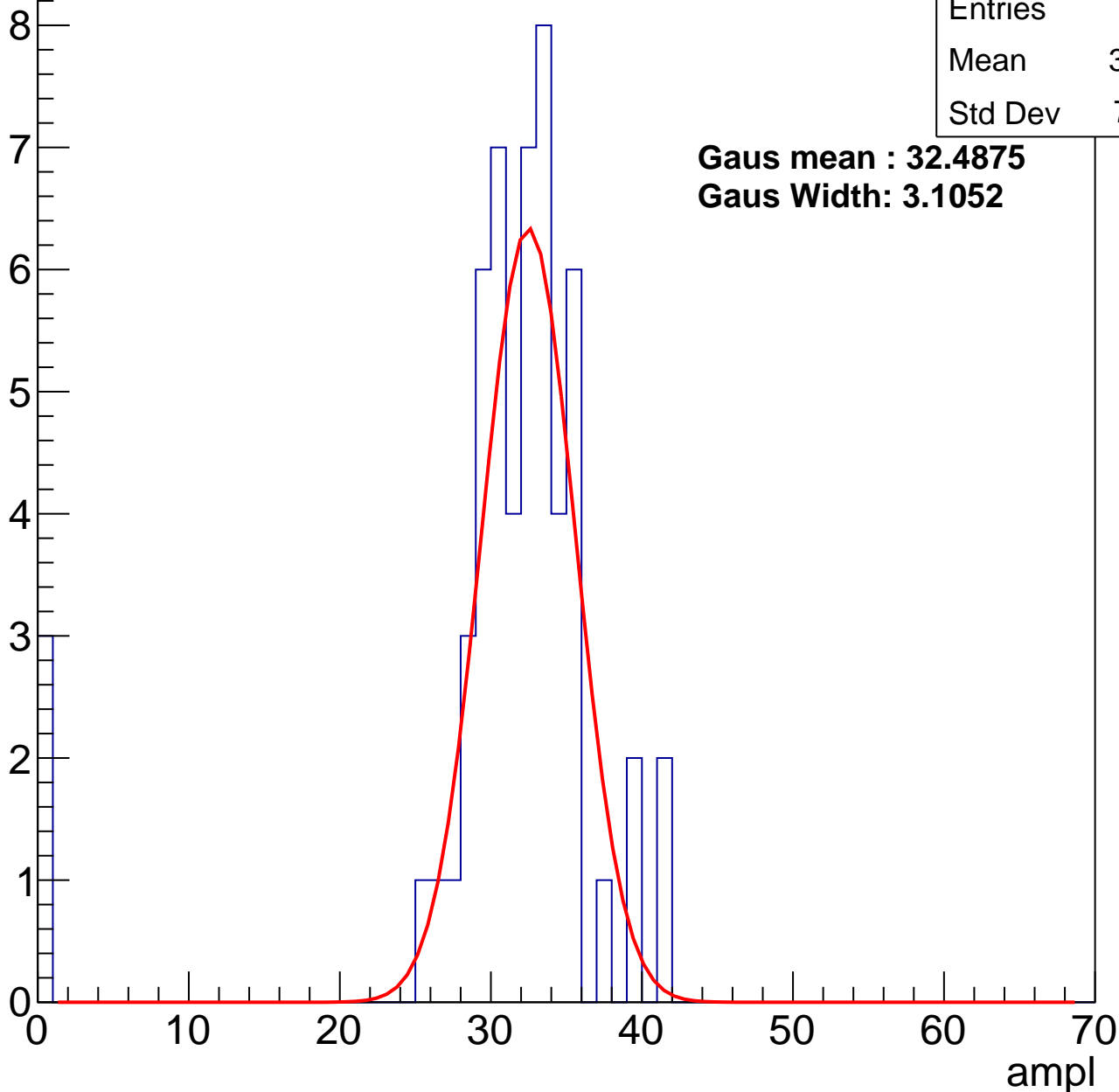
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	30.38
Std Dev	7.941

**Gaus mean : 32.4875**

**Gaus Width: 3.1052**



# B0L001S, U24-ch88, adc1

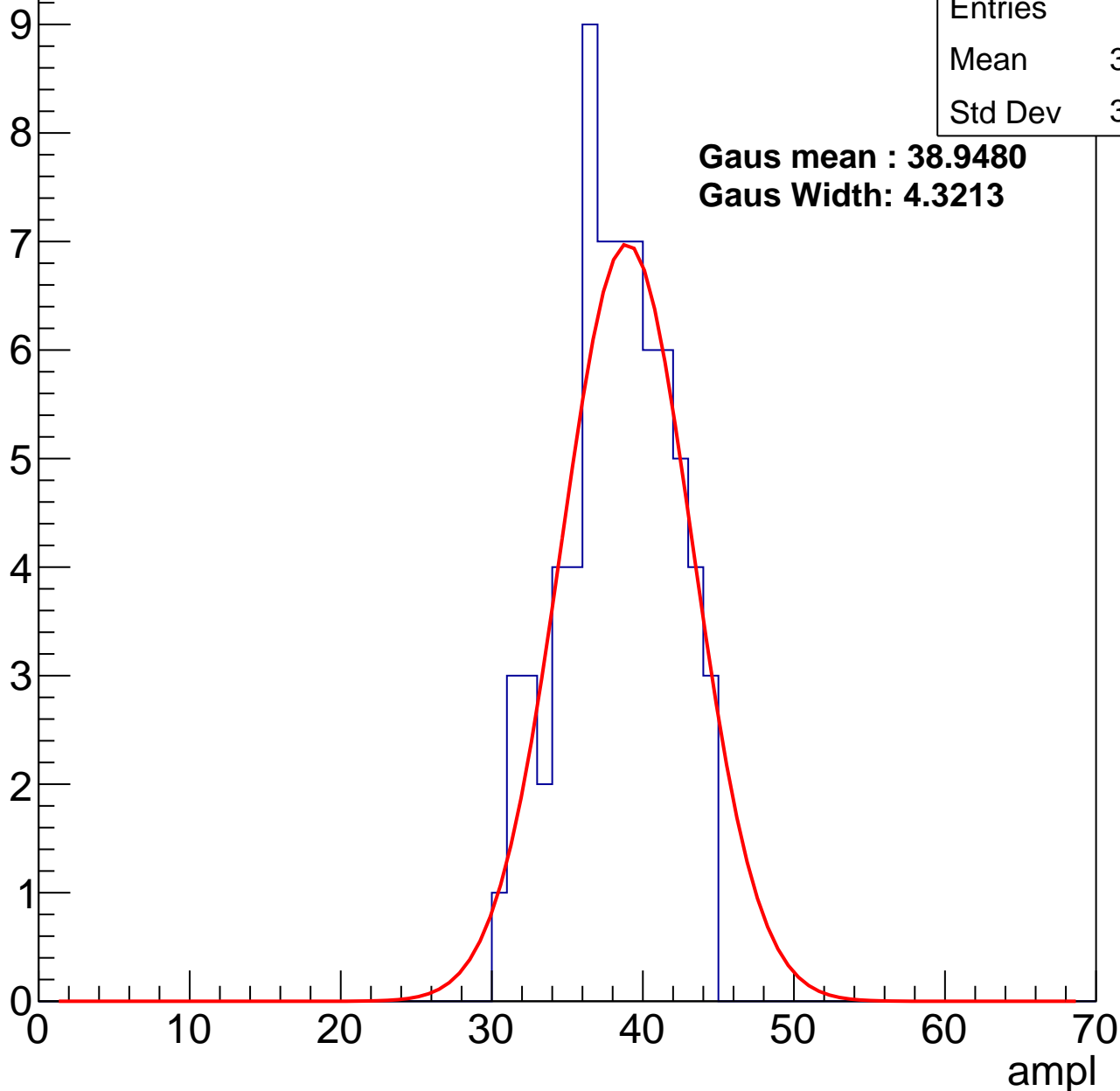
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	37.79
Std Dev	3.524

**Gaus mean : 38.9480**

**Gaus Width: 4.3213**



# B0L001S, U24-ch88, adc2

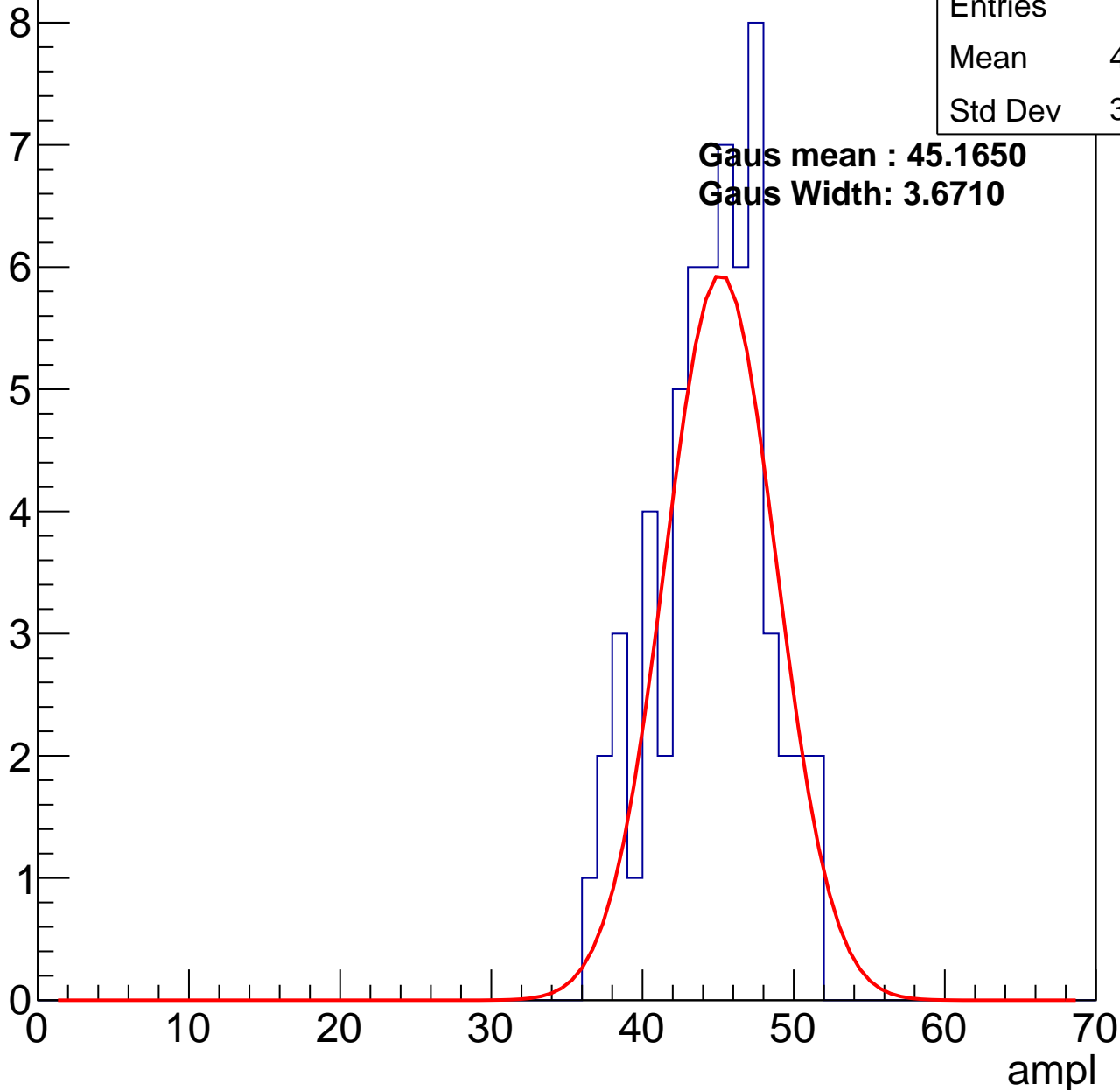
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	44.13
Std Dev	3.589

**Gaus mean : 45.1650**

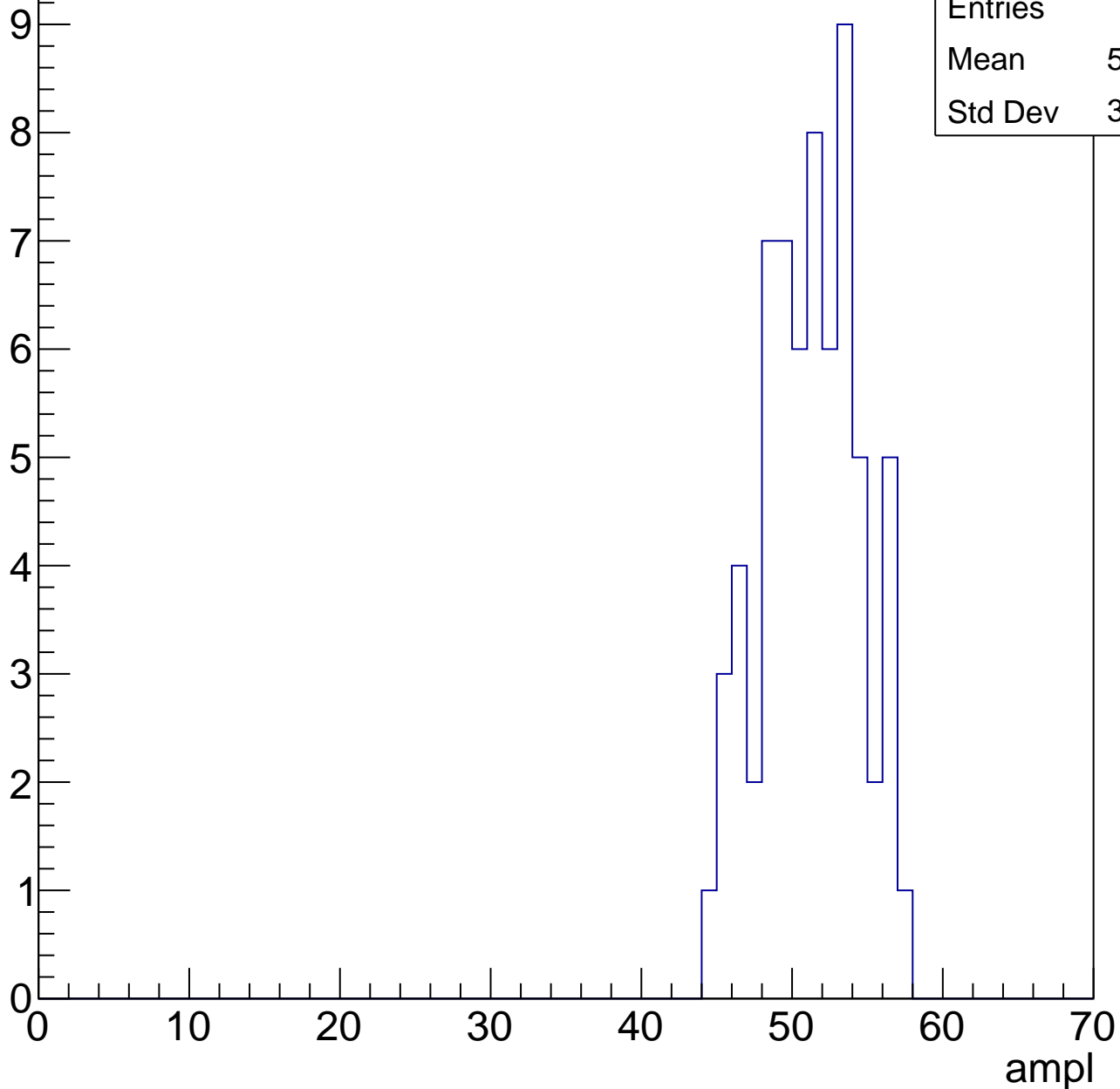
**Gaus Width: 3.6710**



# B0L001S, U24-ch88, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

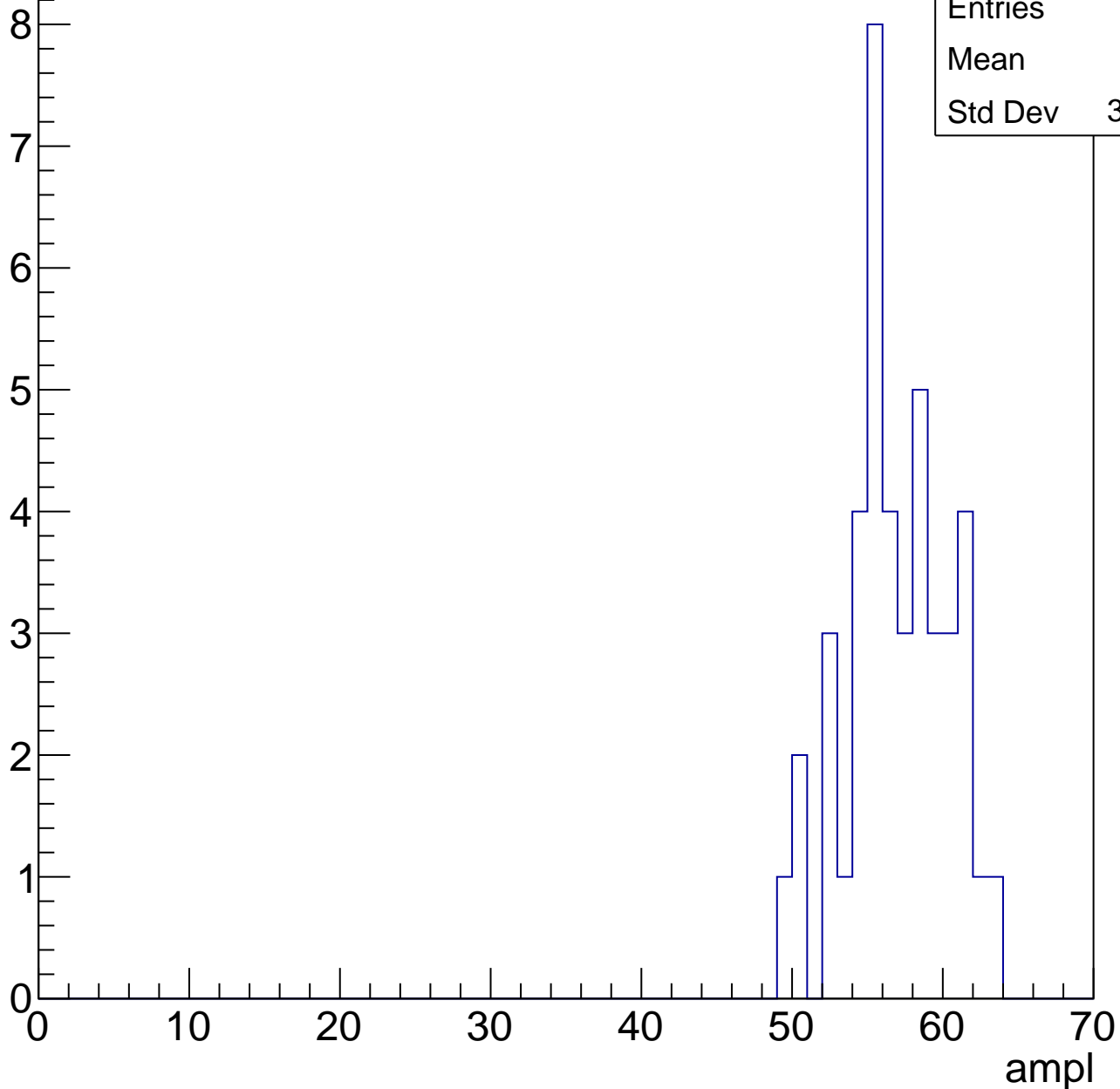


# B0L001S, U24-ch88, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	43
Mean	56.4
Std Dev	3.335



# B0L001S, U24-ch88, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

7

6

5

4

3

2

1

0

Entries 46

Mean 59.7

Std Dev 2.492

ampl

0

10

20

30

40

50

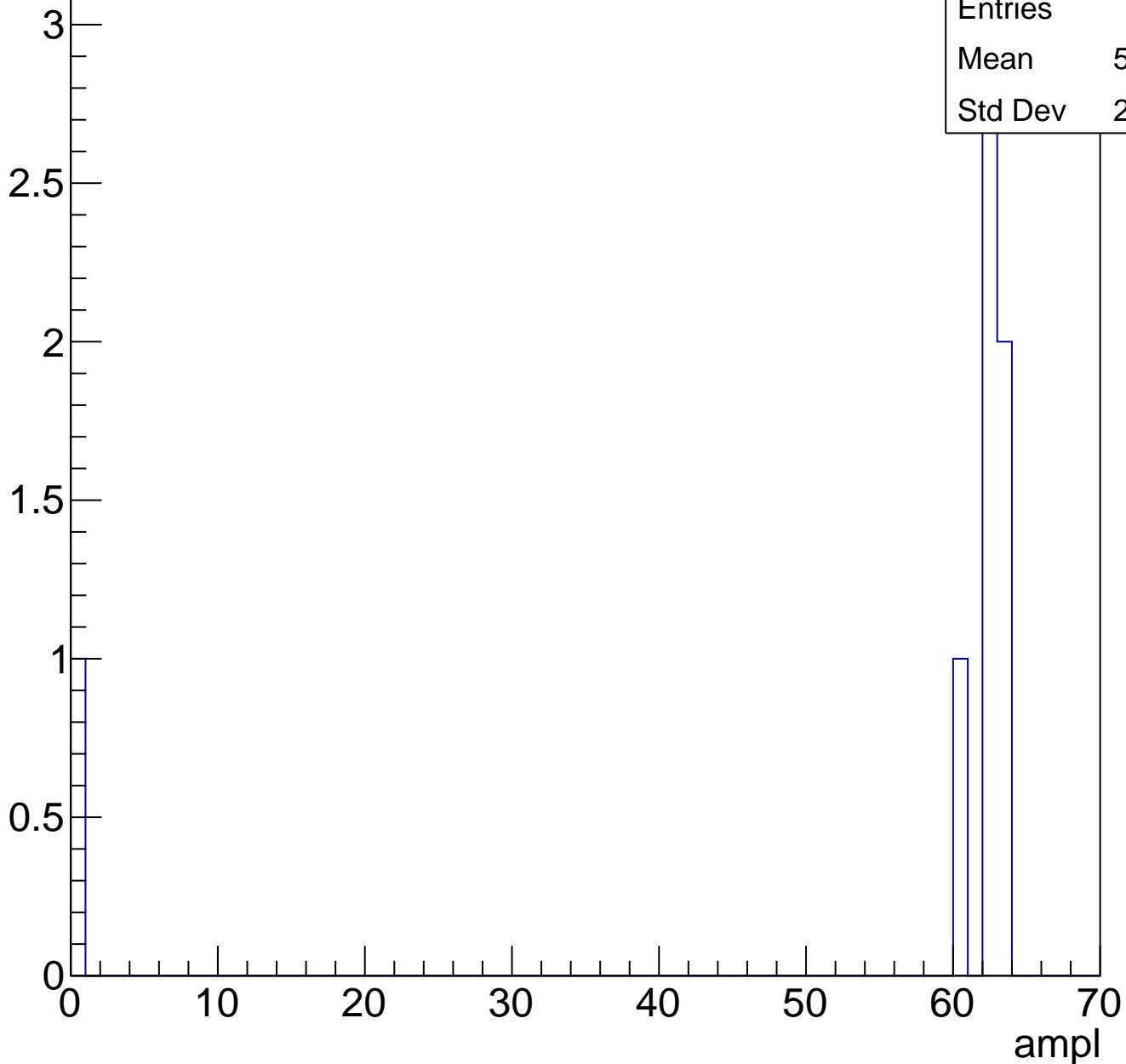
60

70

# B0L001S, U24-ch88, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch88, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

0

Mean

0

Std Dev

0

# B0L001S, U24-ch89, adc0

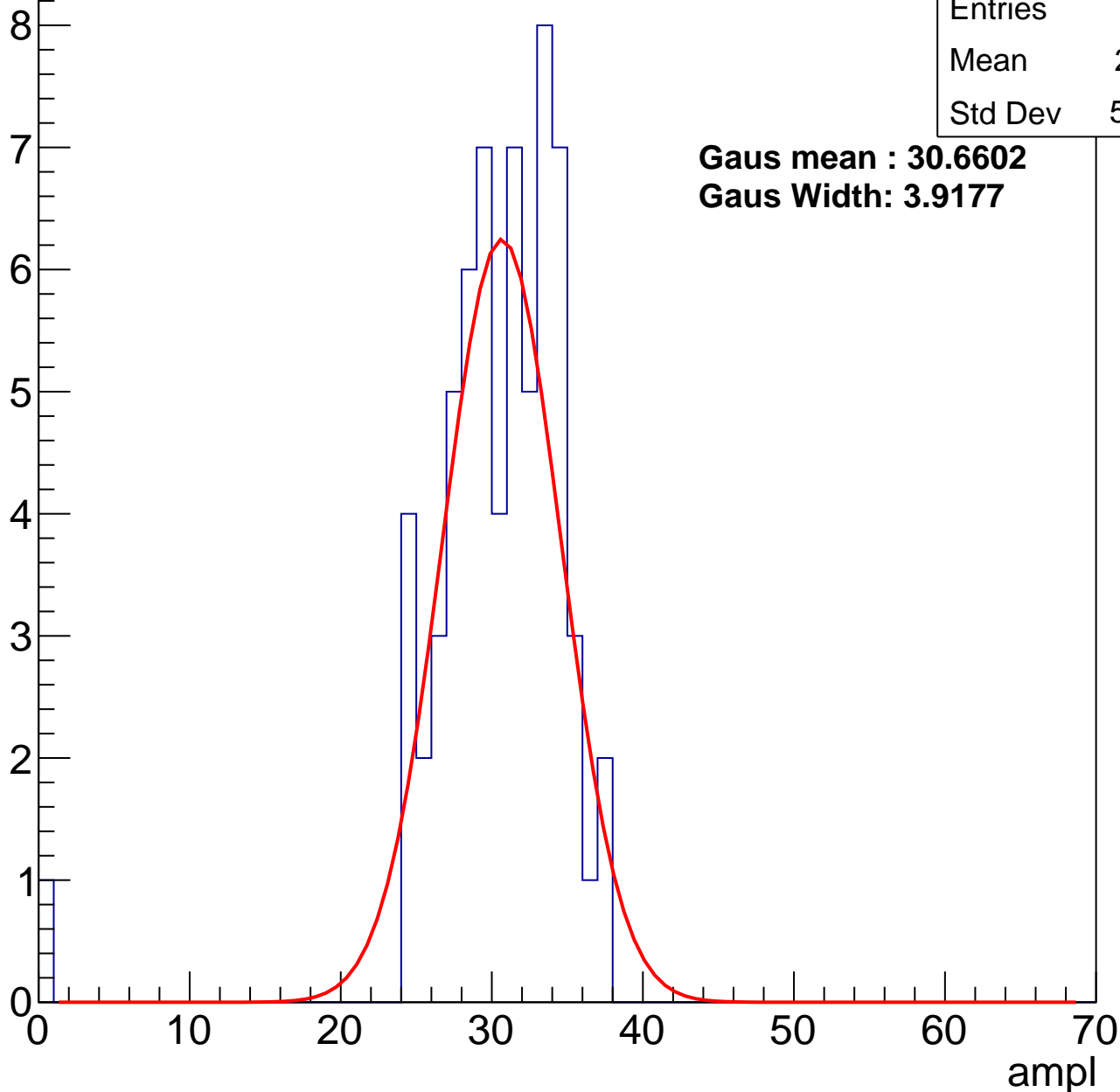
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	29.91
Std Dev	5.019

**Gaus mean : 30.6602**

**Gaus Width: 3.9177**



# B0L001S, U24-ch89, adc1

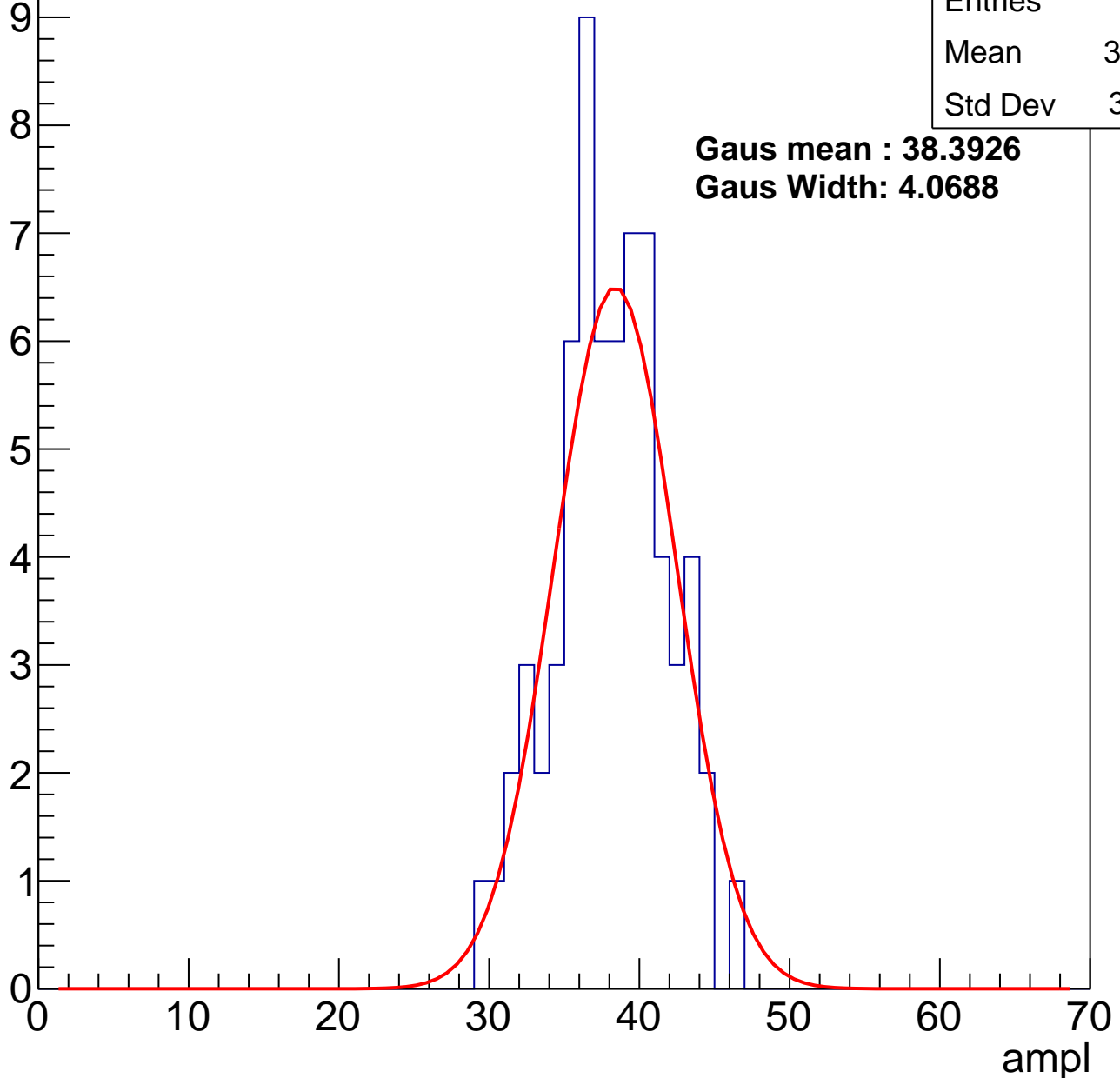
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	37.58
Std Dev	3.641

**Gaus mean : 38.3926**

**Gaus Width: 4.0688**



# B0L001S, U24-ch89, adc2

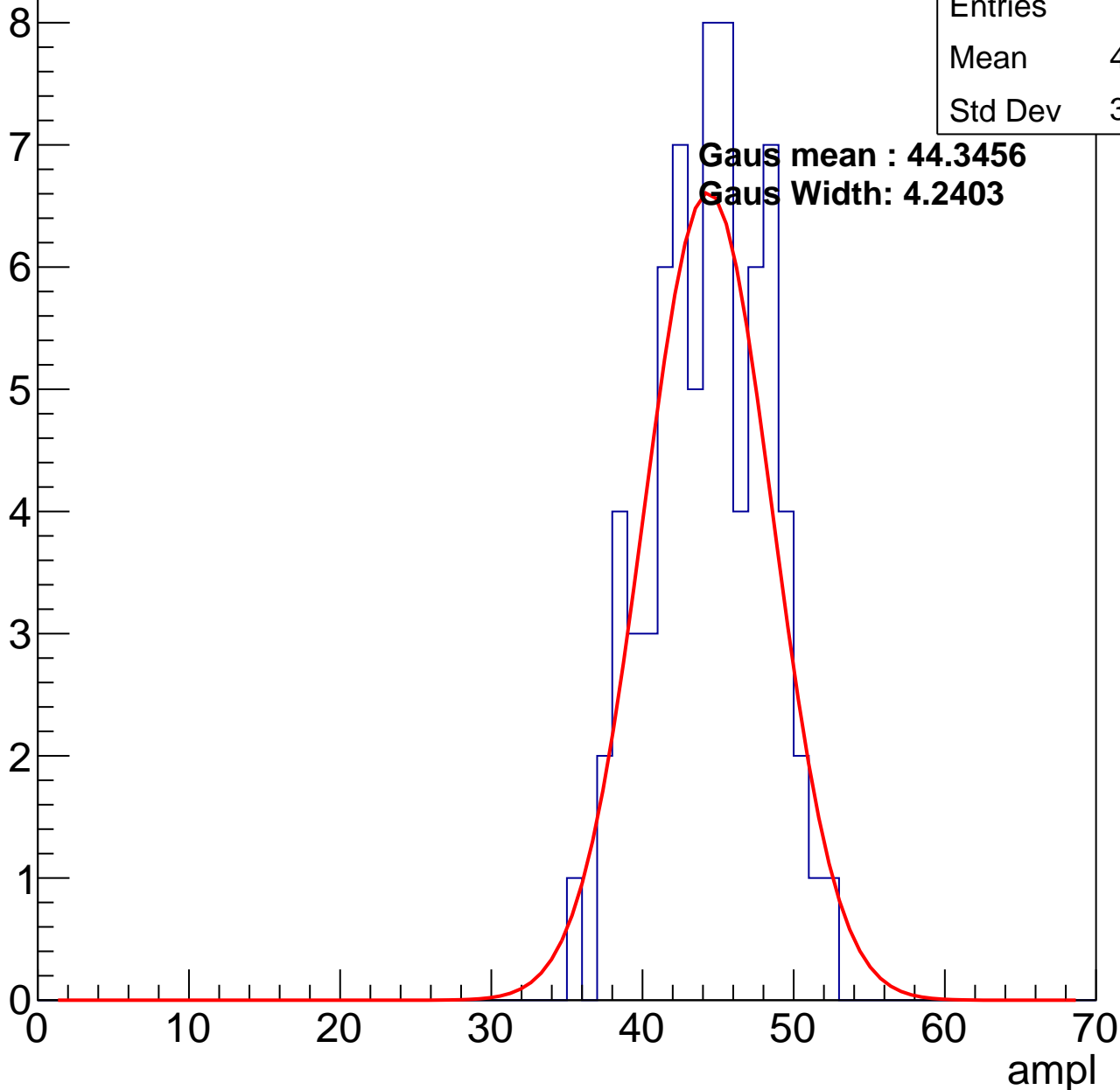
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	43.97
Std Dev	3.742

**Gaus mean : 44.3456**

**Gaus Width: 4.2403**

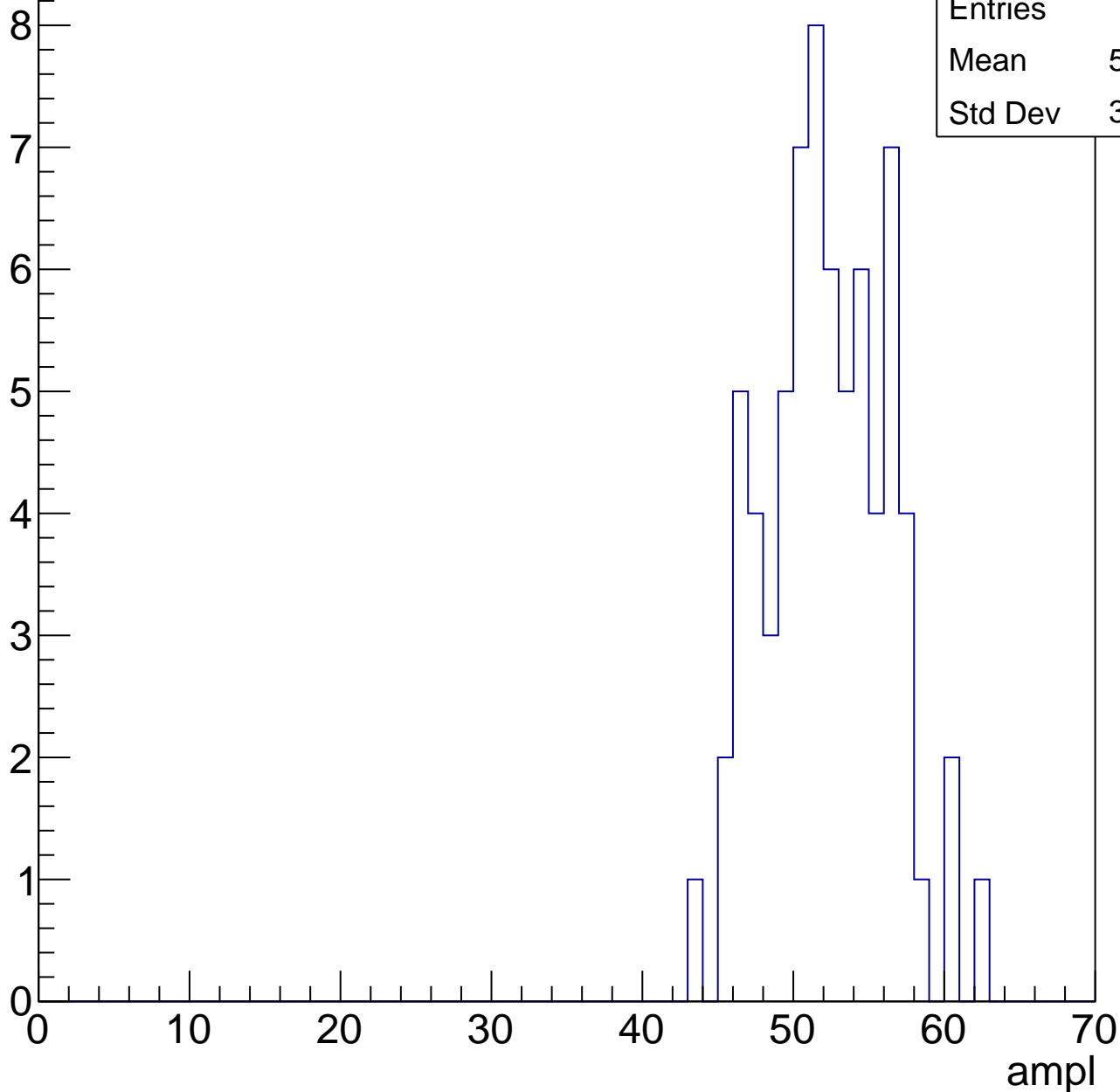


# B0L001S, U24-ch89, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	51.82
Std Dev	3.983

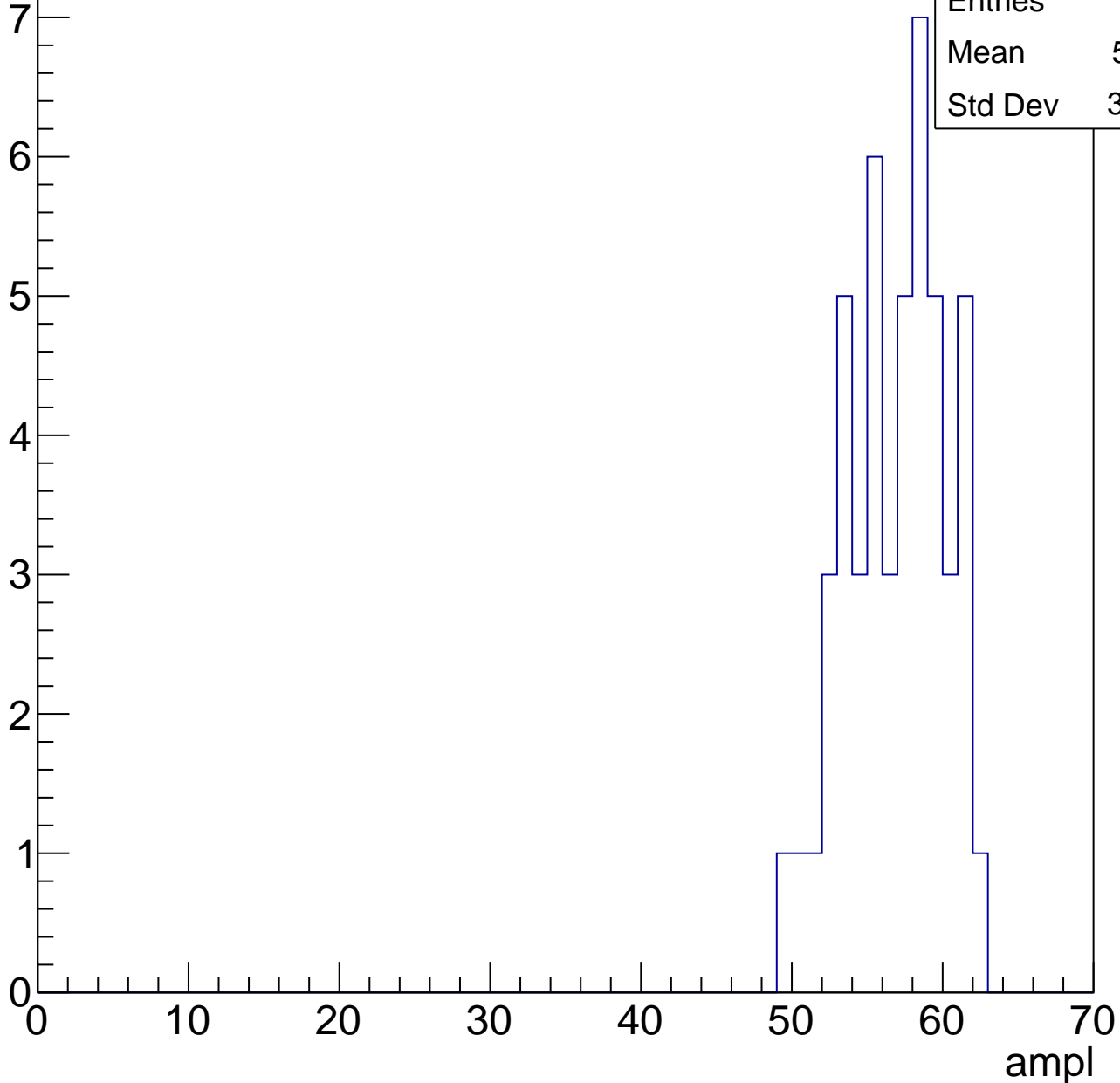


# B0L001S, U24-ch89, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	49
Mean	56.41
Std Dev	3.194

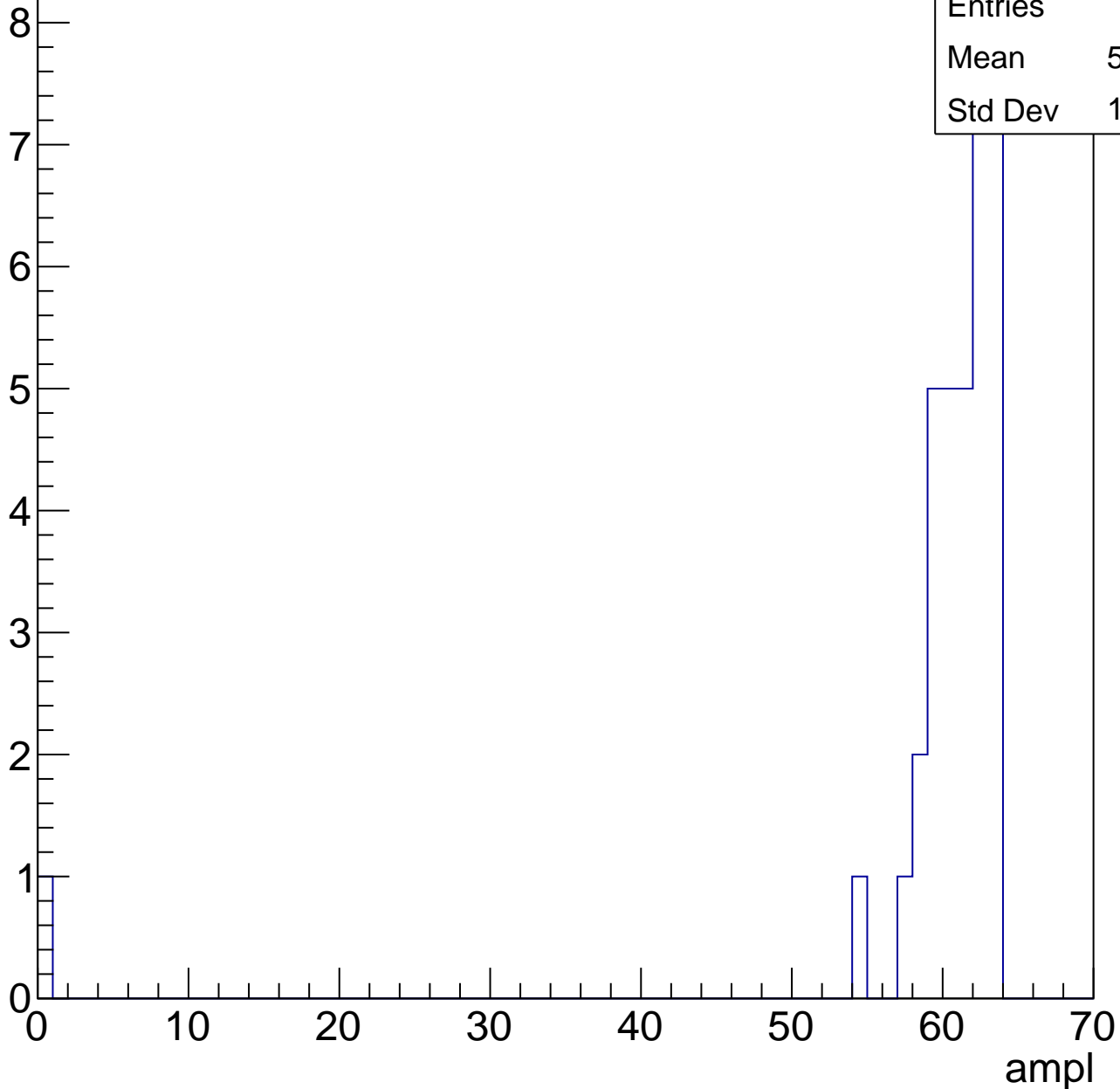


# B0L001S, U24-ch89, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	36
Mean	59.08
Std Dev	10.19



# B0L001S, U24-ch89, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch89, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U24-ch90, adc0

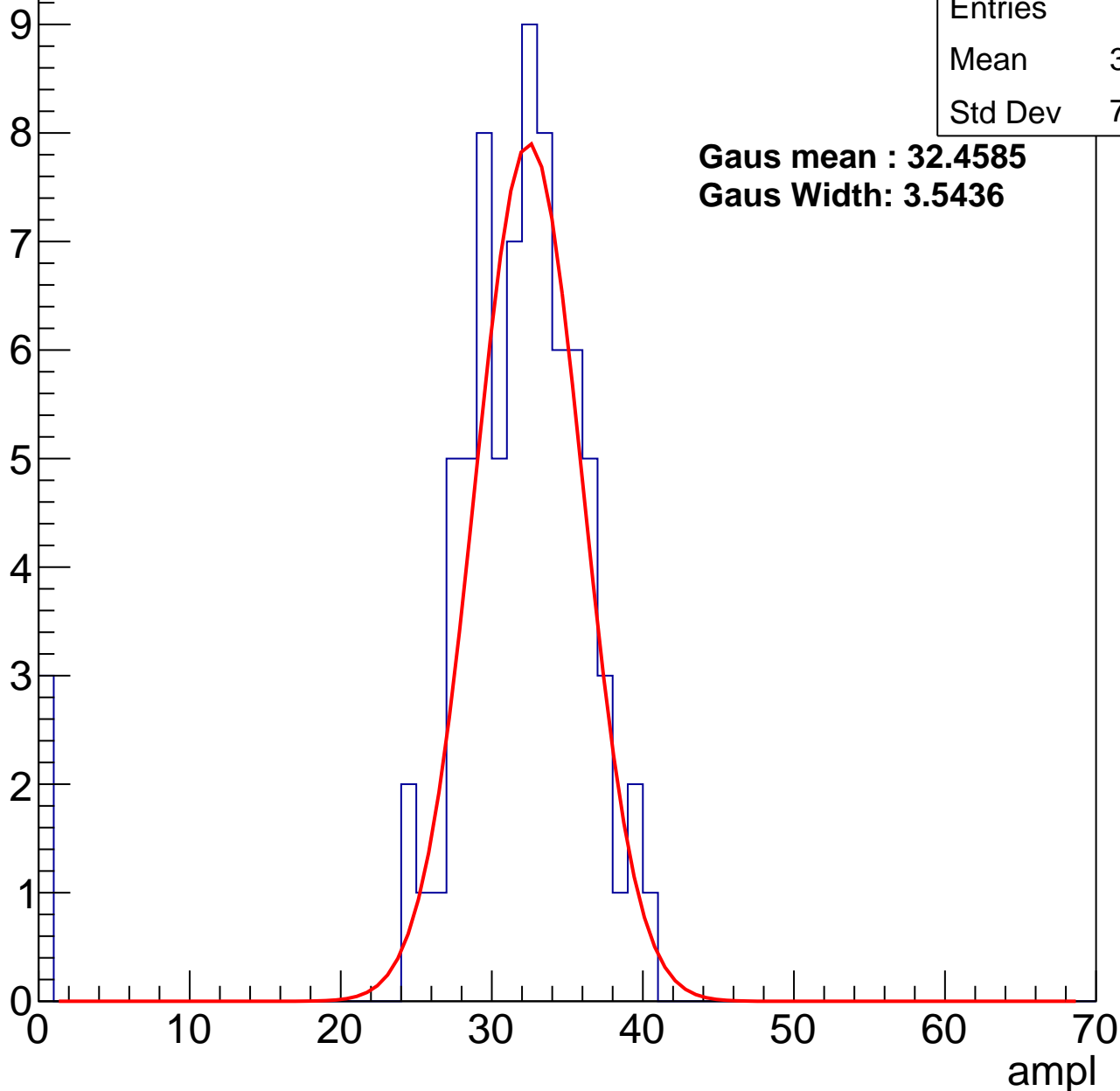
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	78
Mean	30.59
Std Dev	7.046

**Gaus mean : 32.4585**

**Gaus Width: 3.5436**



# B0L001S, U24-ch90, adc1

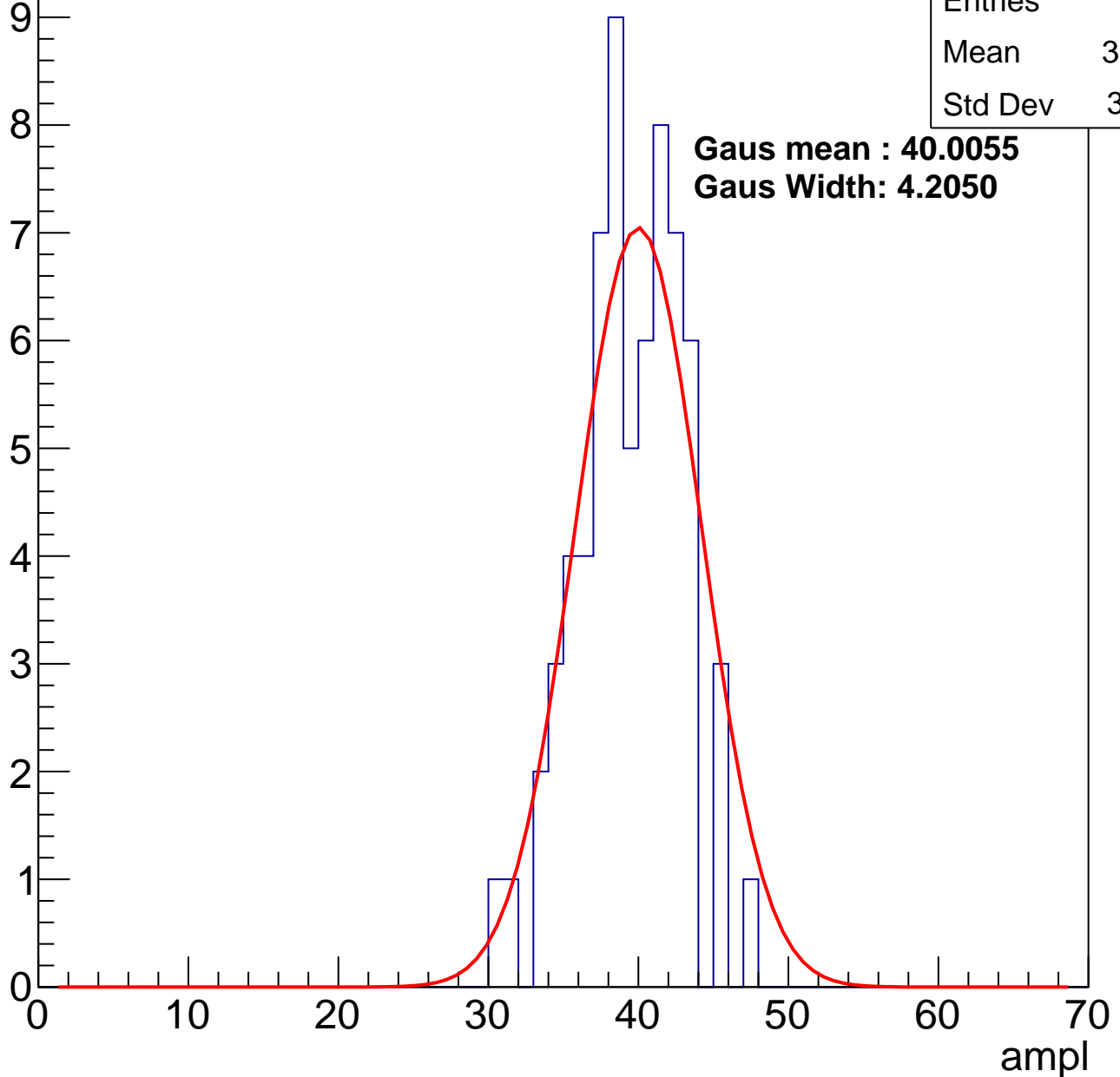
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	38.97
Std Dev	3.451

**Gaus mean : 40.0055**

**Gaus Width: 4.2050**



# B0L001S, U24-ch90, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	52
Mean	44.6
Std Dev	3.794

**Gaus mean : 45.1641**

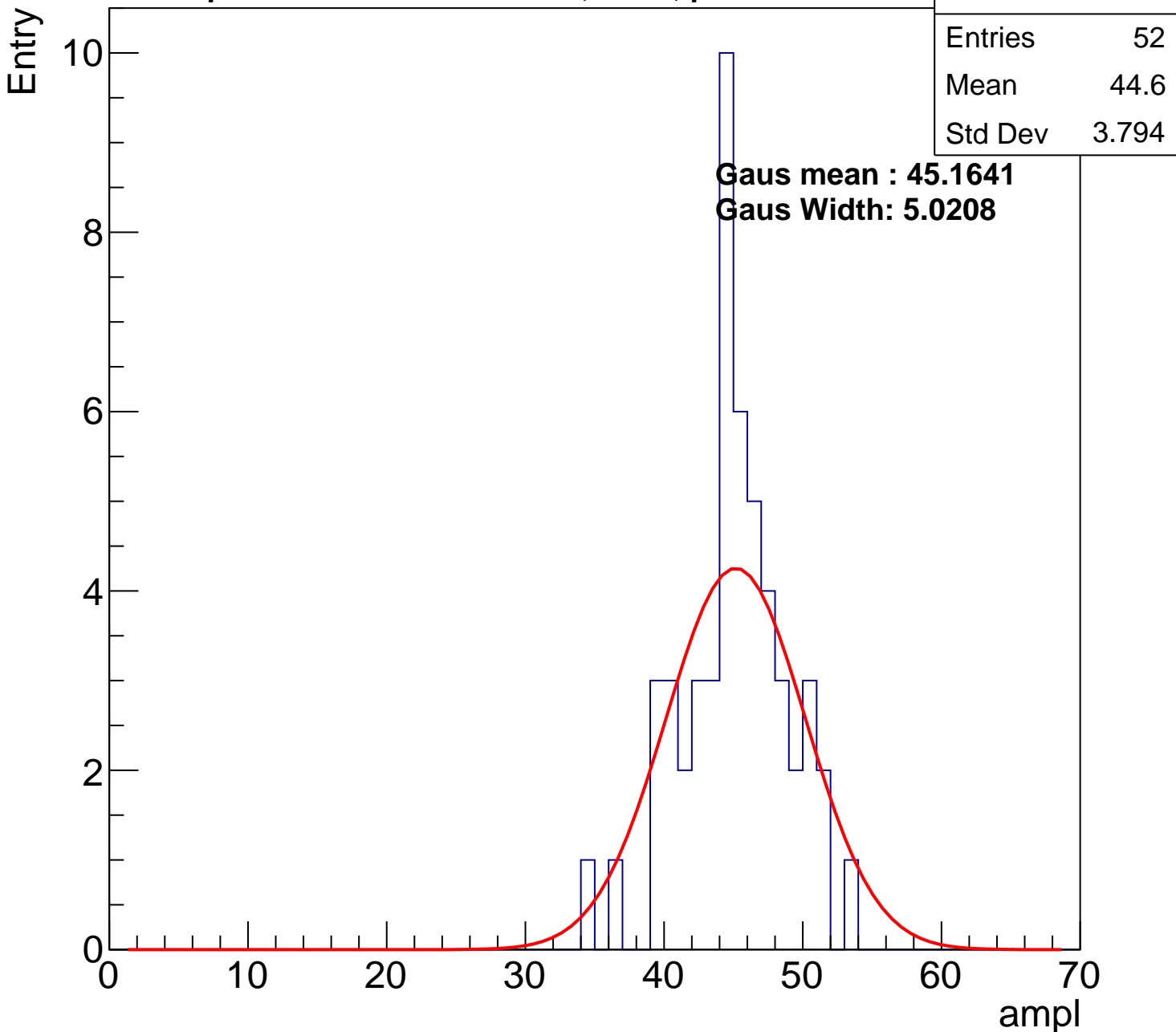
**Gaus Width: 5.0208**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

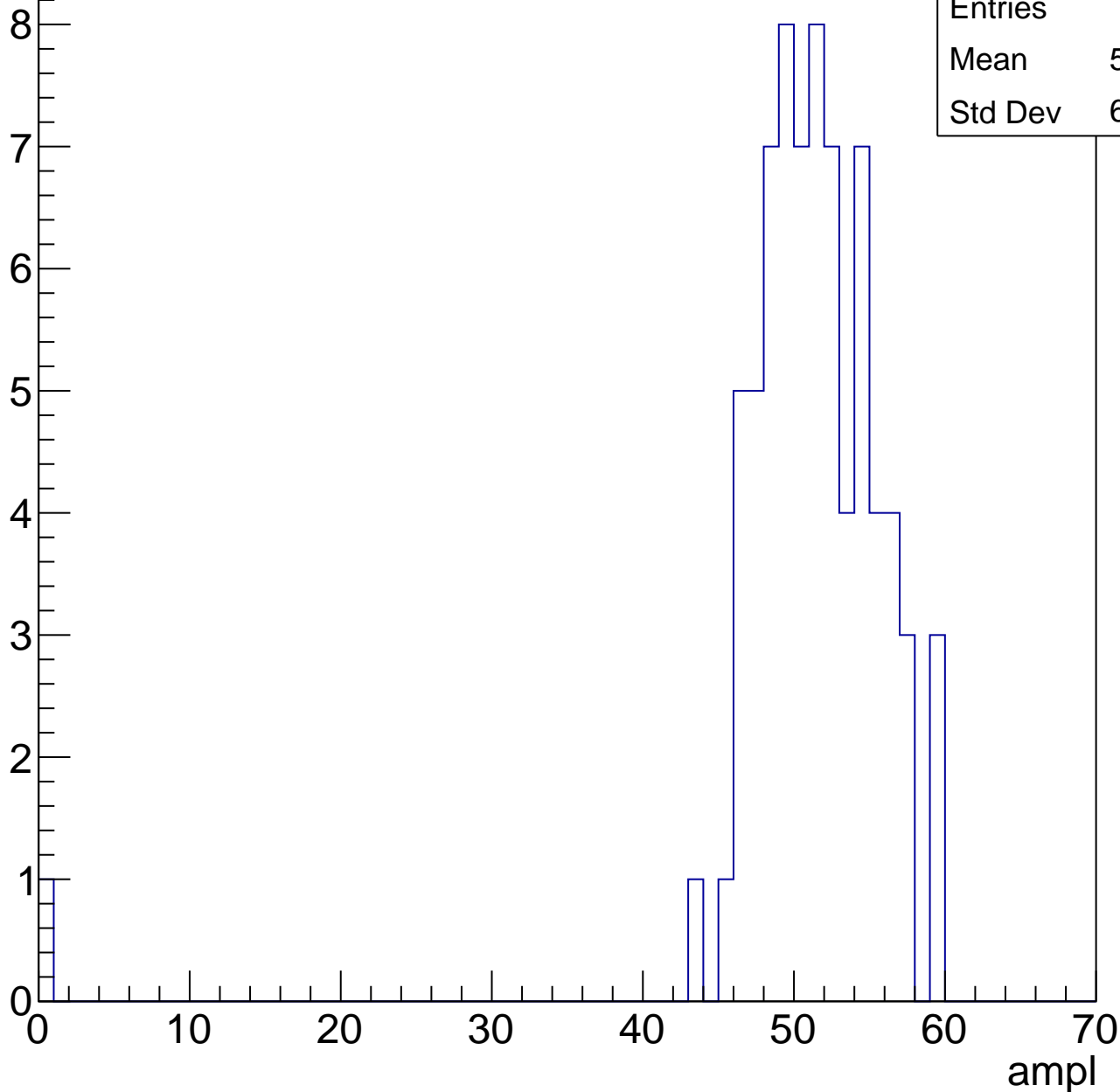


# B0L001S, U24-ch90, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	75
Mean	50.47
Std Dev	6.867

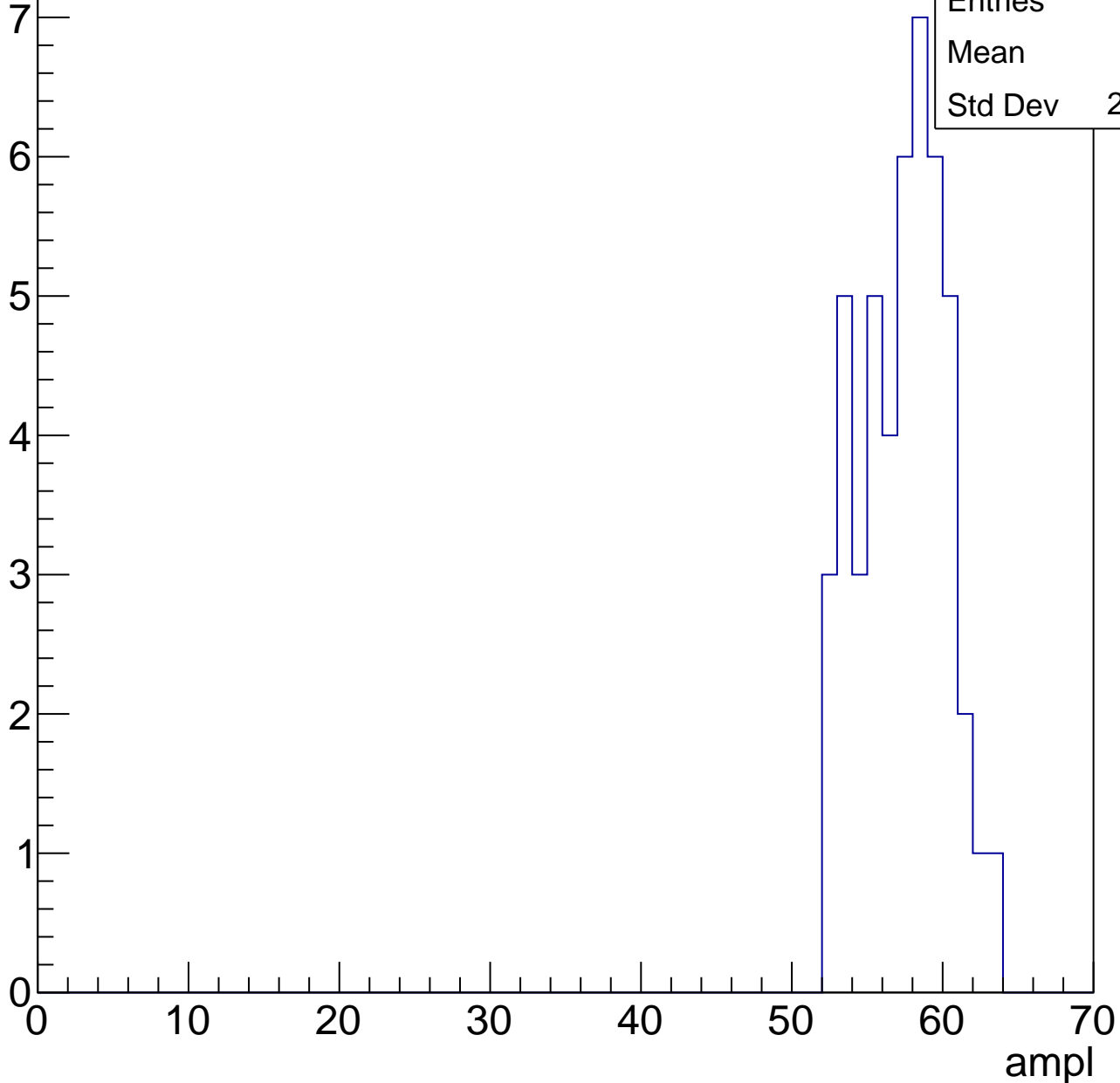


# B0L001S, U24-ch90, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	48
Mean	56.9
Std Dev	2.793

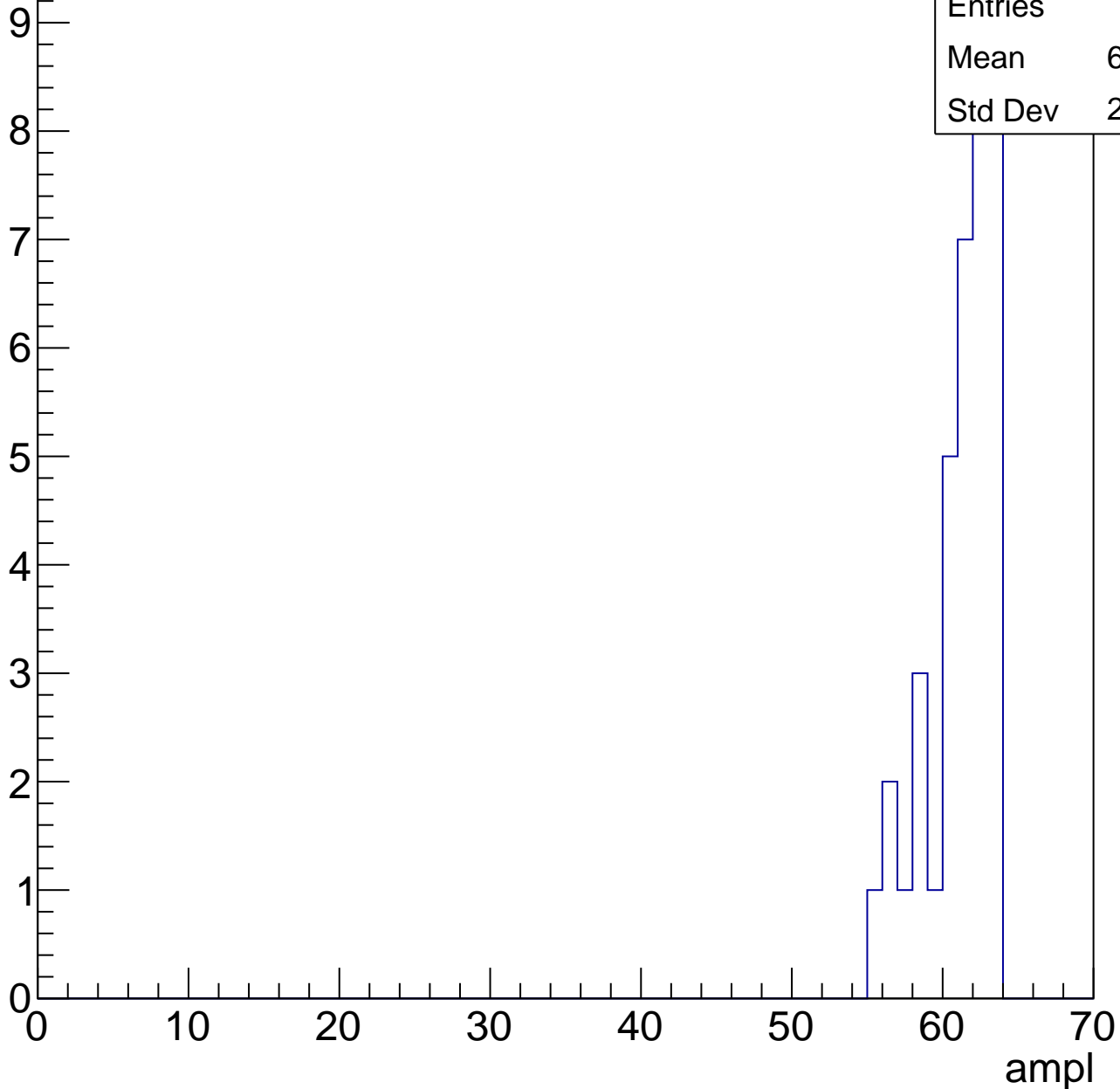


# B0L001S, U24-ch90, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	38
Mean	60.76
Std Dev	2.182



# B0L001S, U24-ch90, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch90, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U24-ch91, adc0

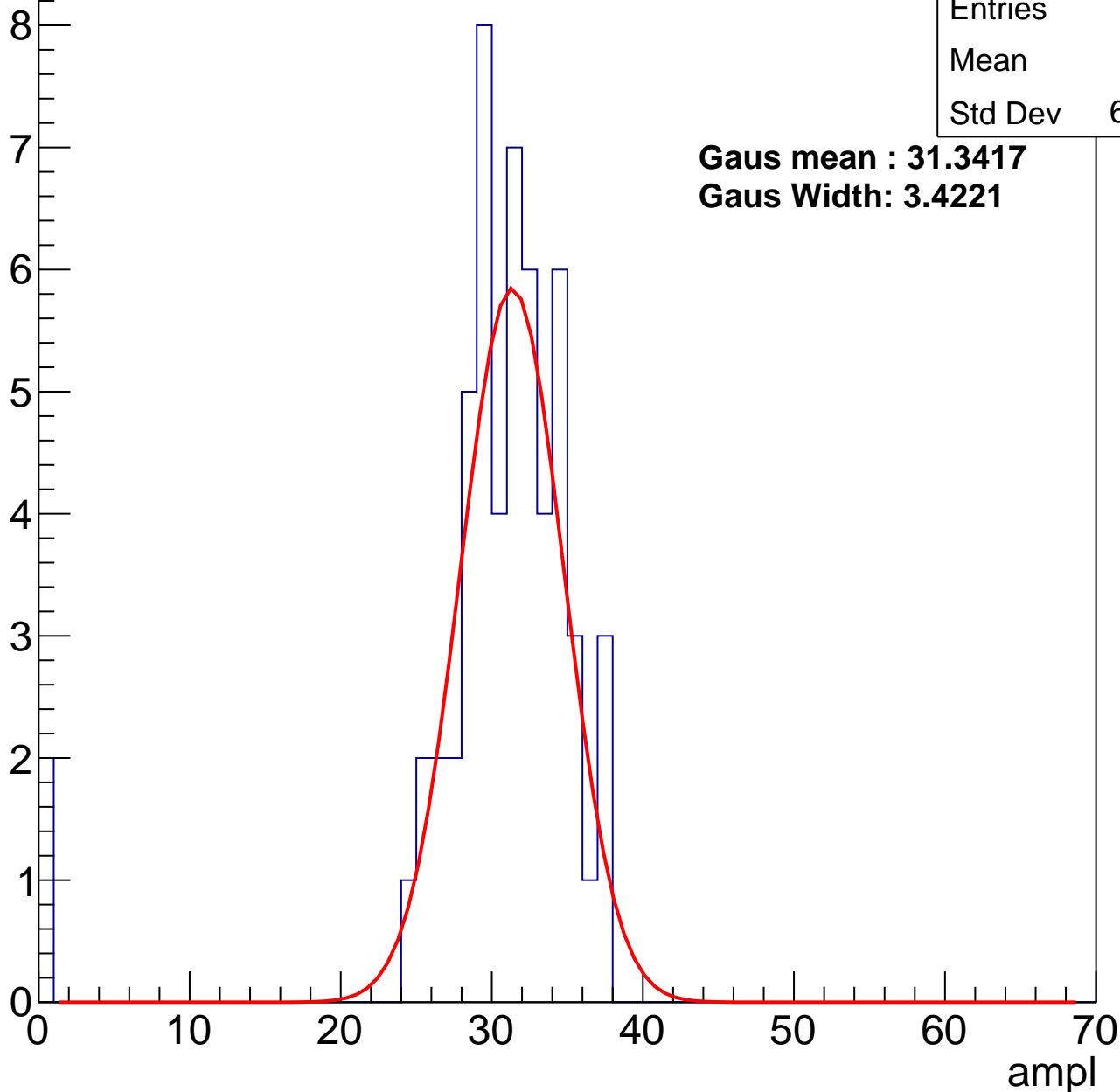
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	29.8
Std Dev	6.523

**Gaus mean : 31.3417**

**Gaus Width: 3.4221**



# B0L001S, U24-ch91, adc1

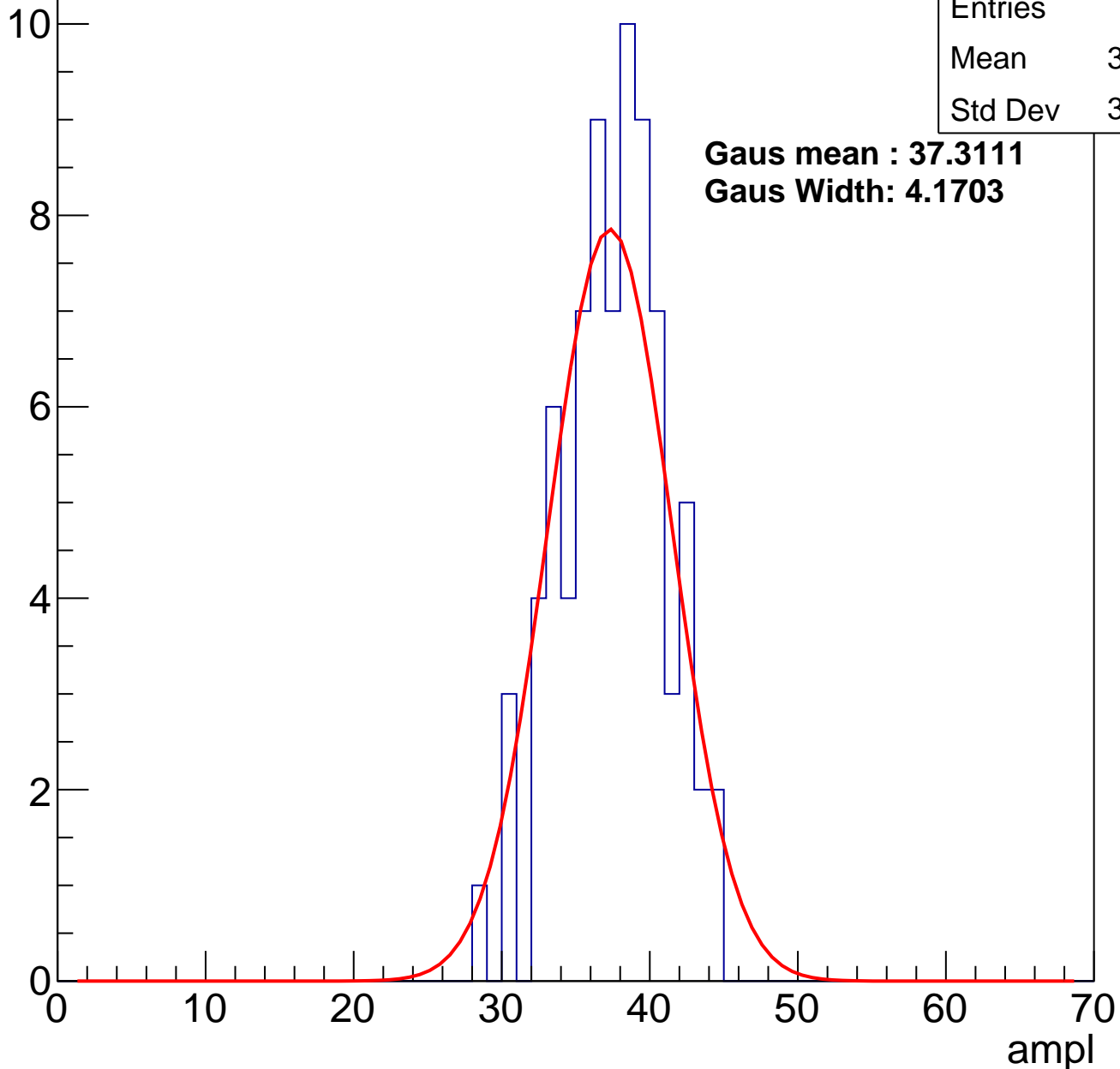
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	79
Mean	37.04
Std Dev	3.466

**Gaus mean : 37.3111**

**Gaus Width: 4.1703**

Entry



# B0L001S, U24-ch91, adc2

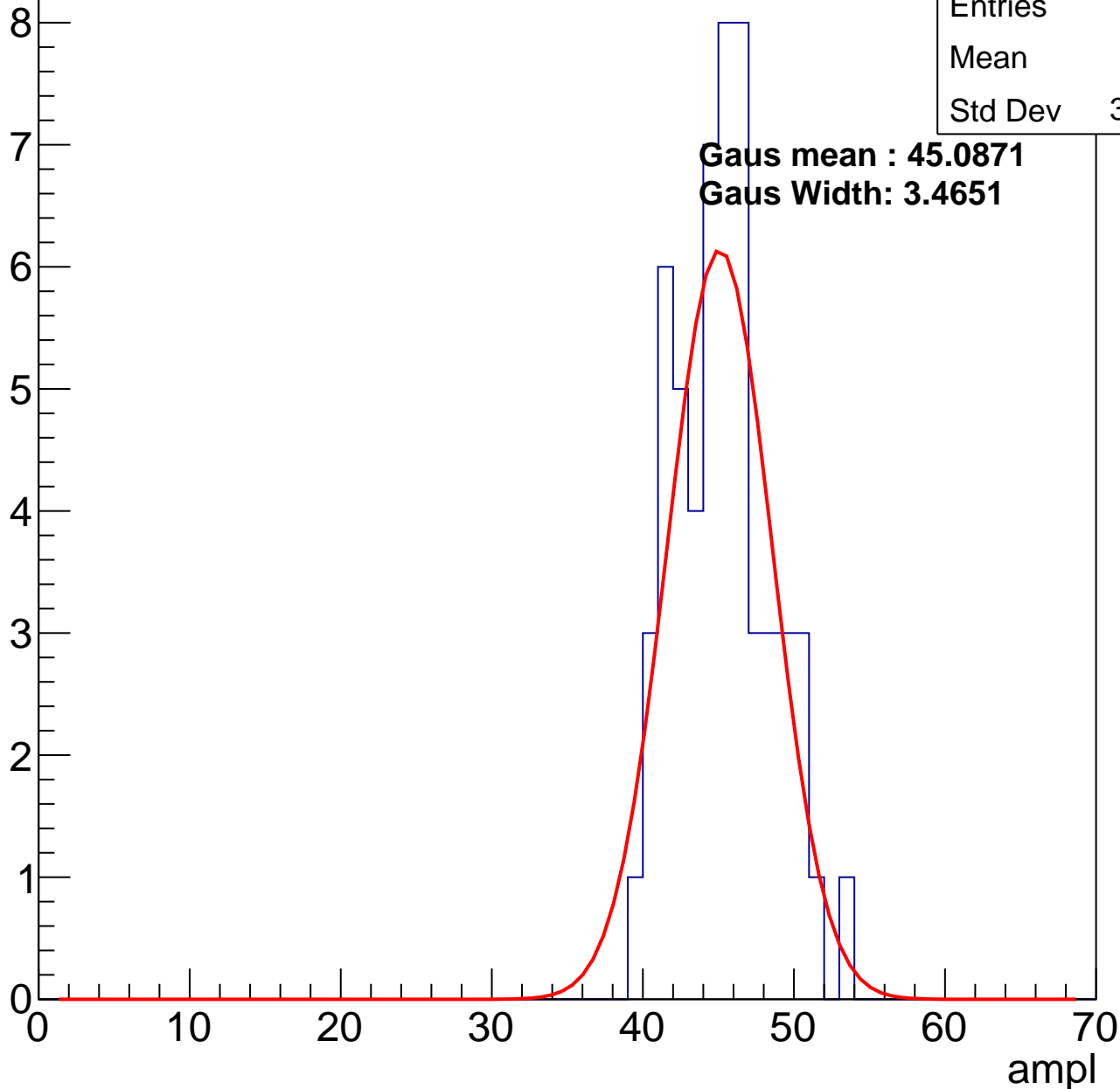
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	44.8
Std Dev	3.113

**Gaus mean : 45.0871**

**Gaus Width: 3.4651**

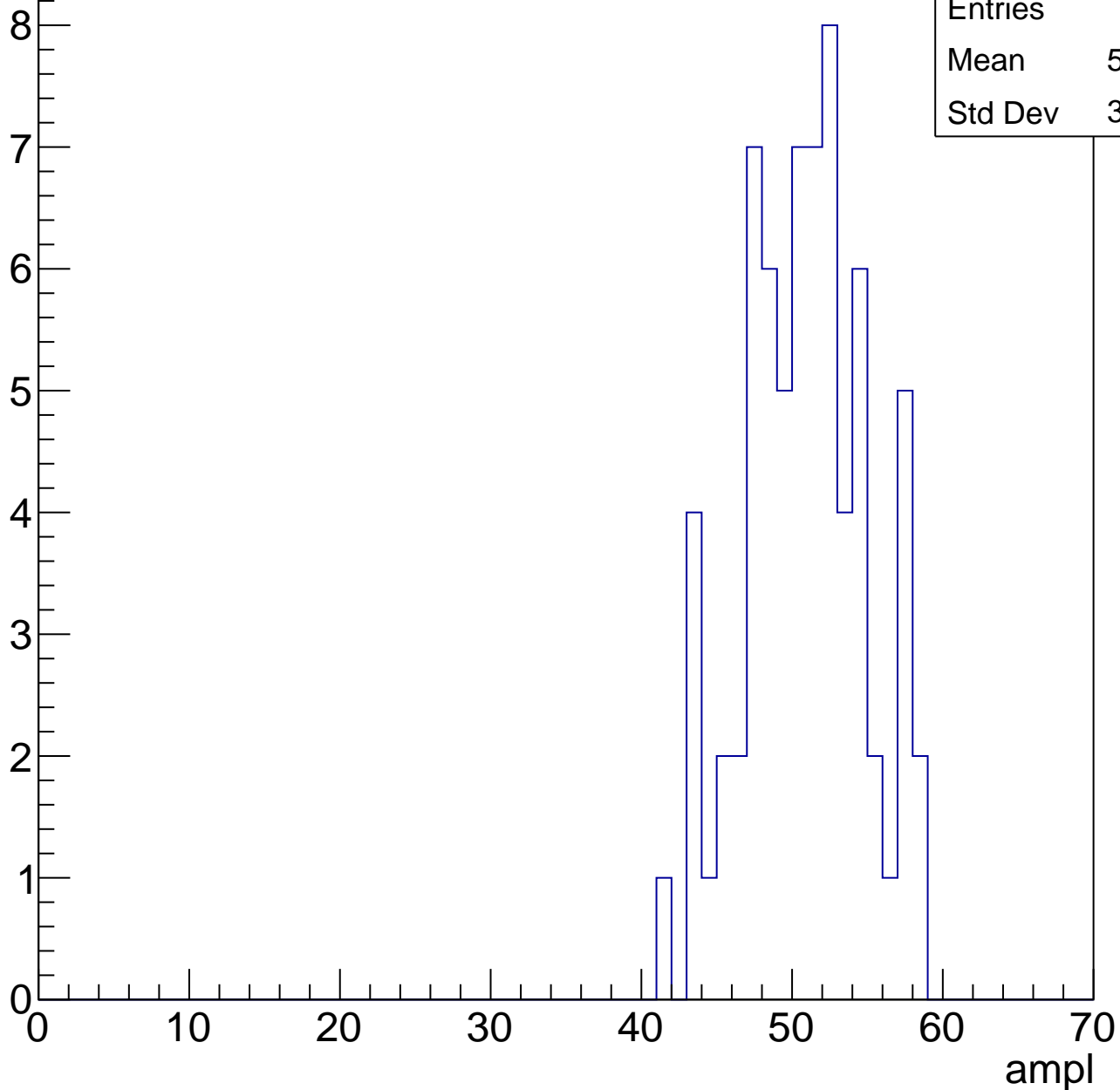


# B0L001S, U24-ch91, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

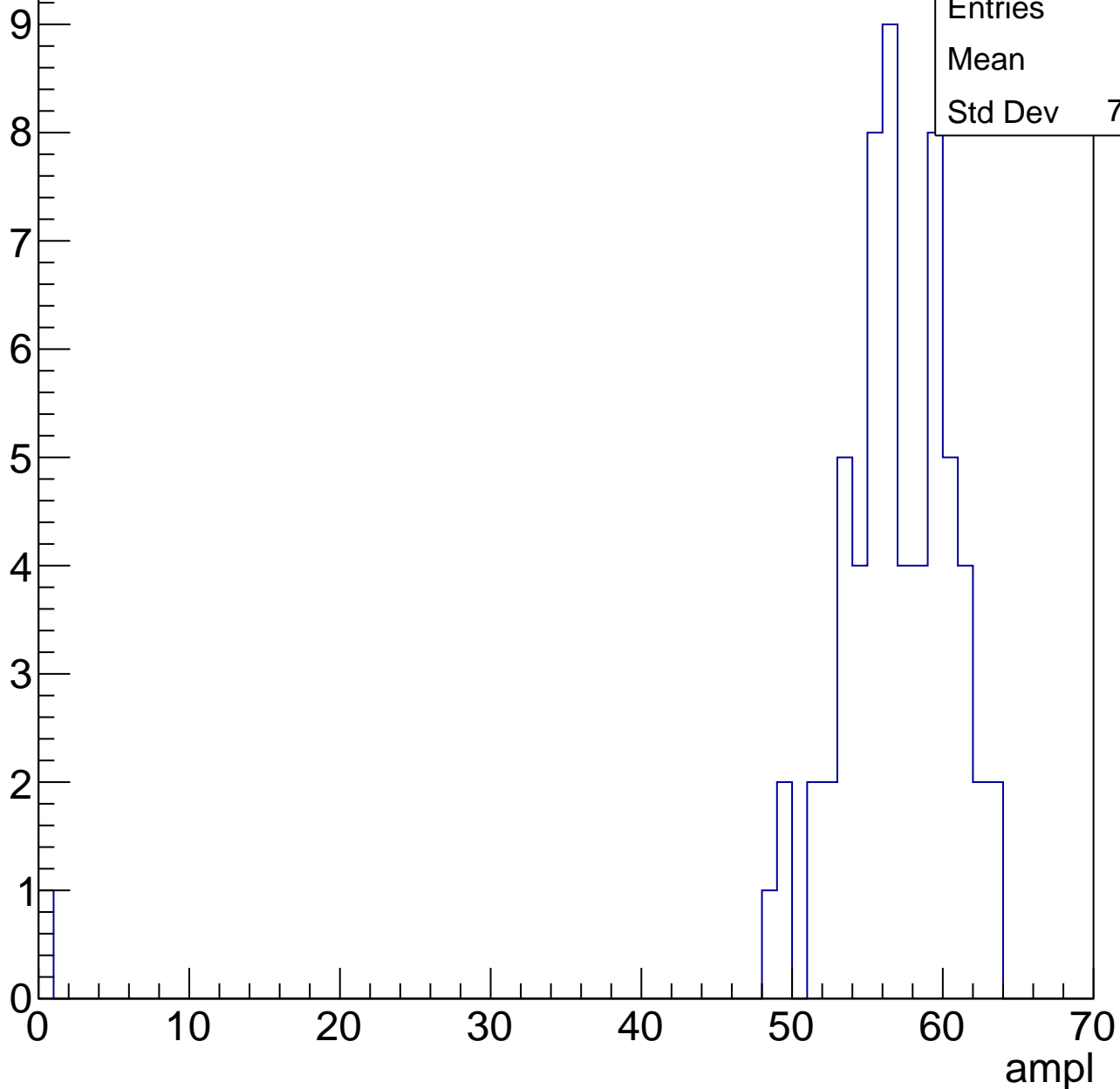
Entries	70
Mean	50.39
Std Dev	3.976



# B0L001S, U24-ch91, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

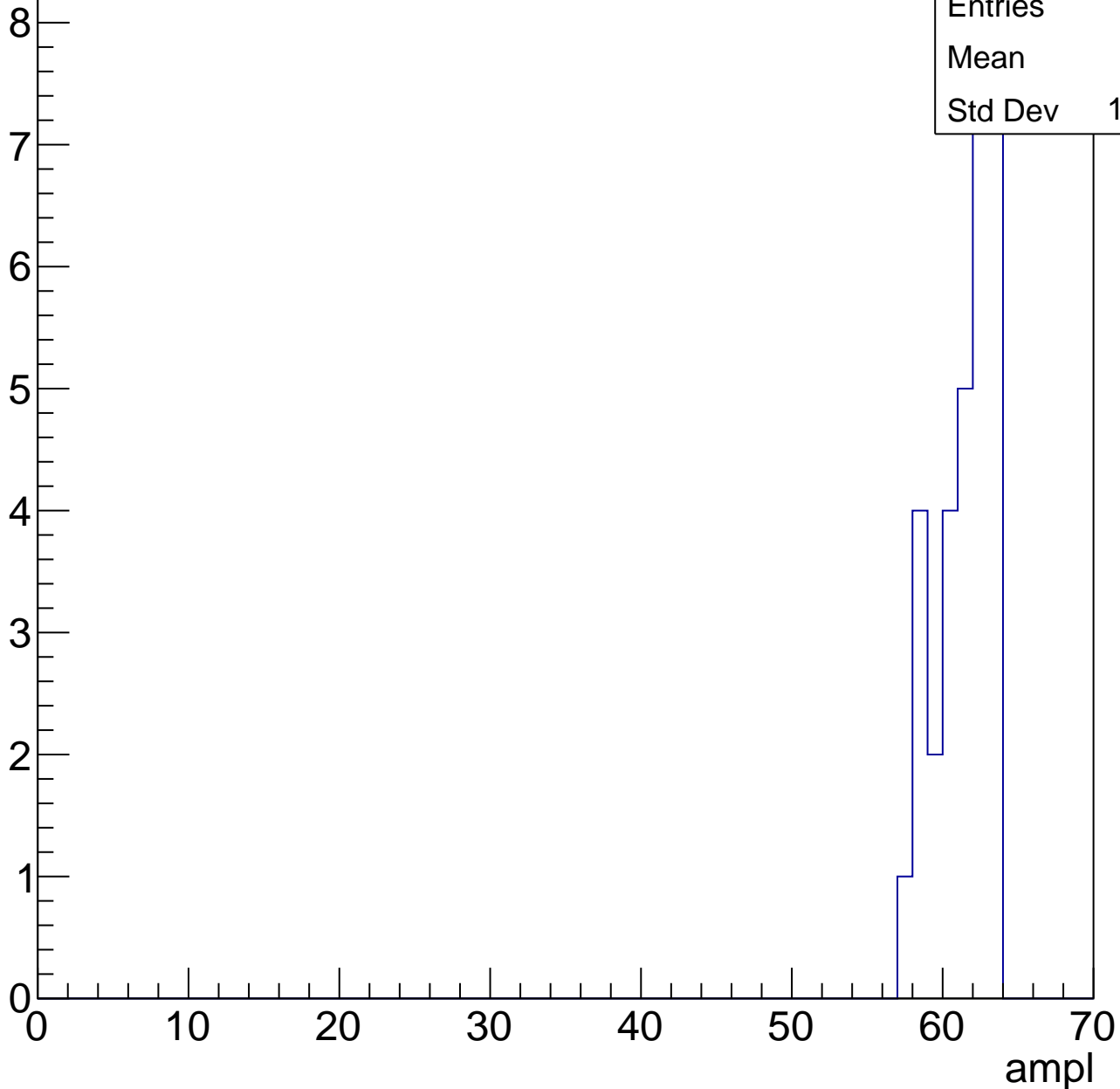


# B0L001S, U24-ch91, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

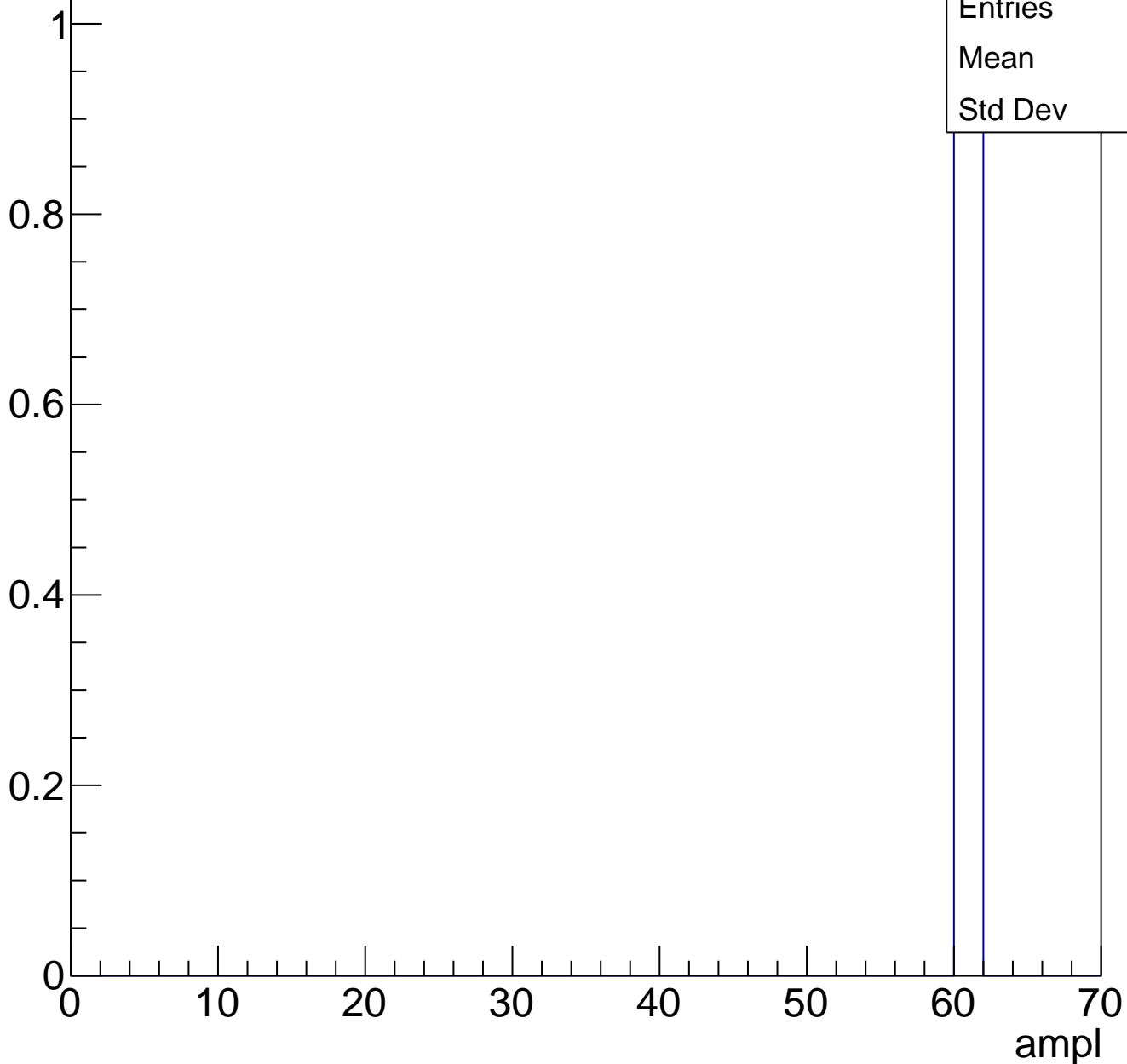
Entries	32
Mean	61
Std Dev	1.803



# B0L001S, U24-ch91, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch91, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U24-ch92, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	67
Mean	29.85
Std Dev	3.563

**Gaus mean : 29.8574**

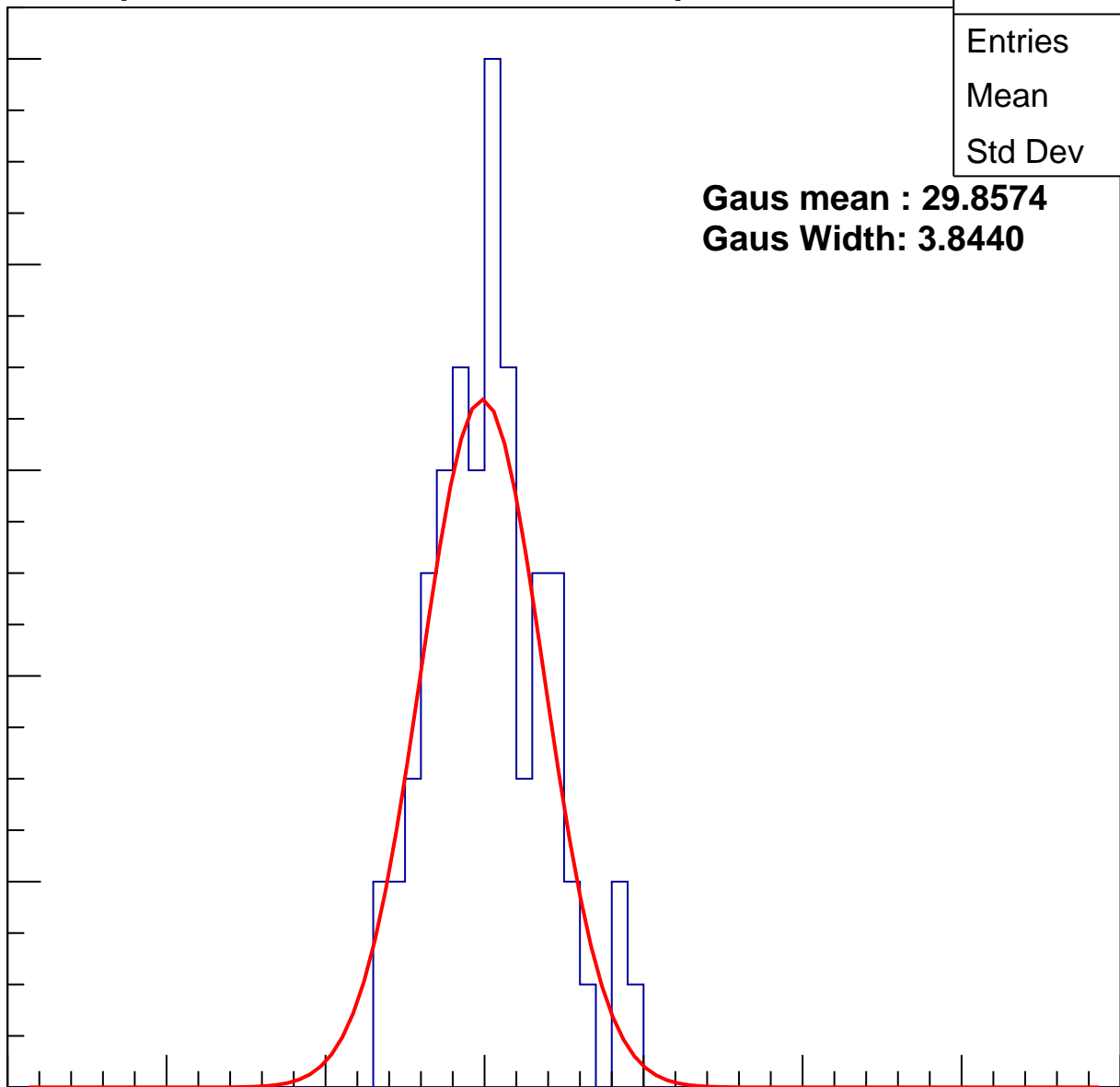
**Gaus Width: 3.8440**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U24-ch92, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	73
Mean	36.14
Std Dev	3.669

**Gaus mean : 36.1396**

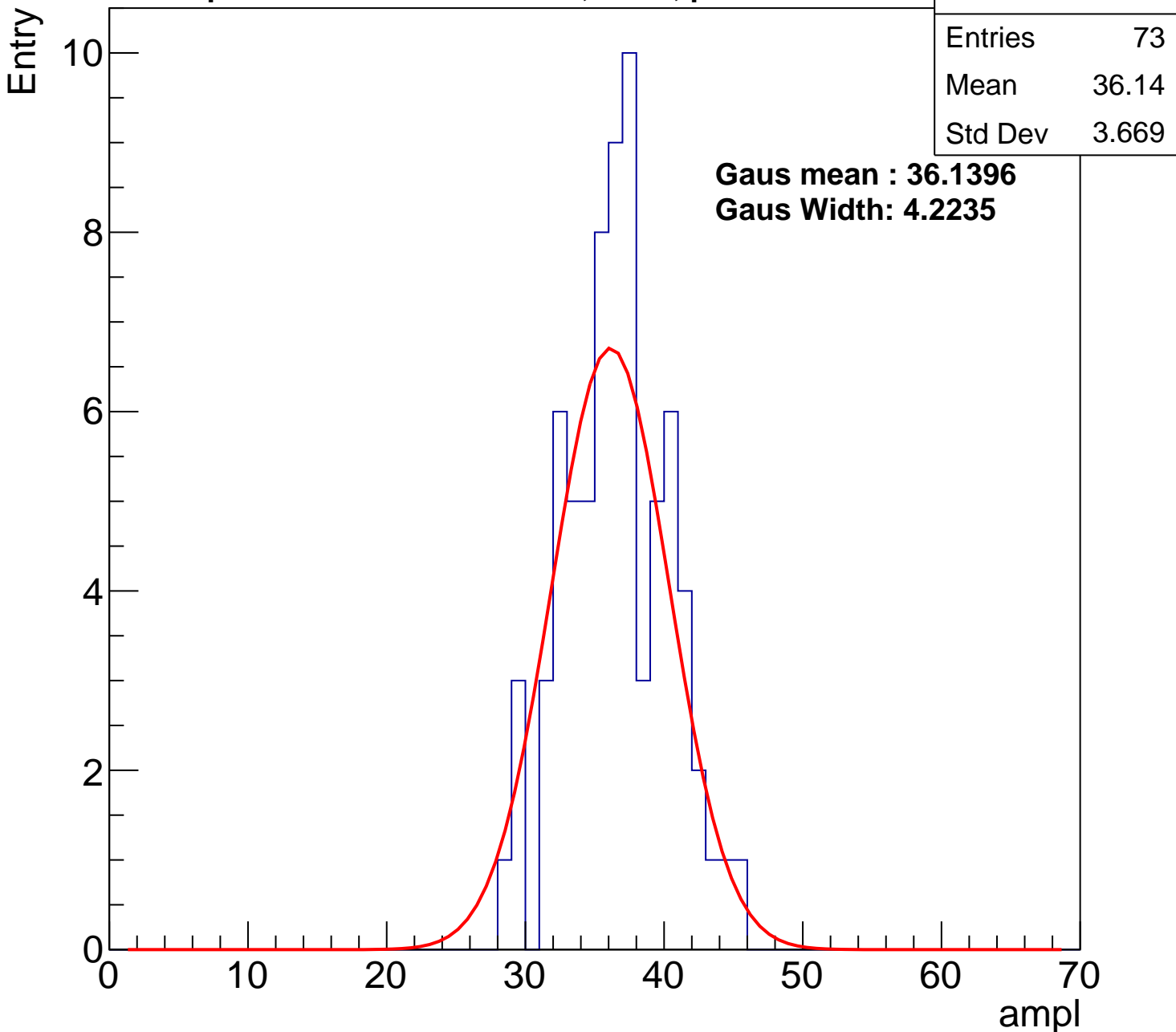
**Gaus Width: 4.2235**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B0L001S, U24-ch92, adc2

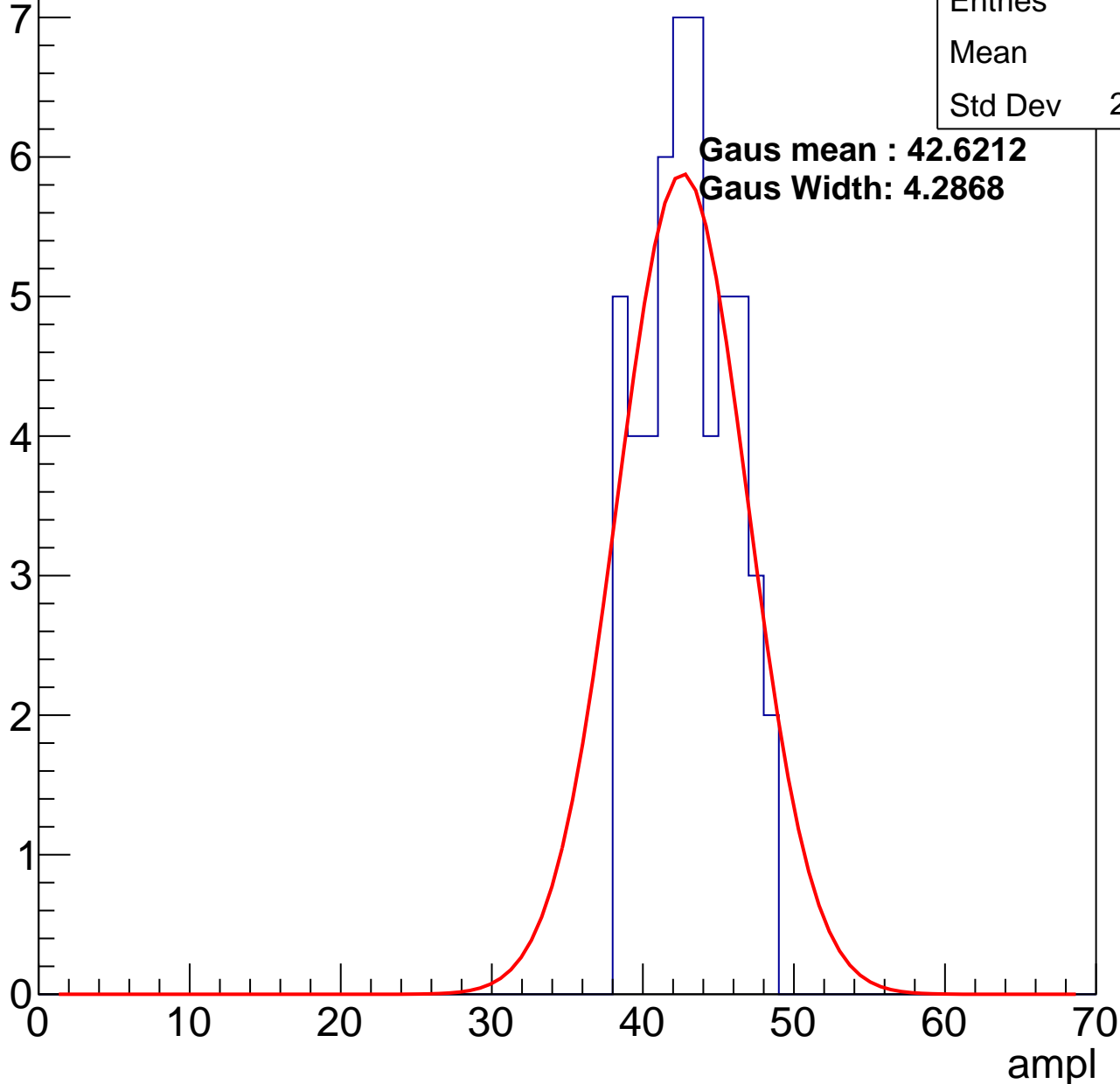
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	42.6
Std Dev	2.823

**Gaus mean : 42.6212**

**Gaus Width: 4.2868**

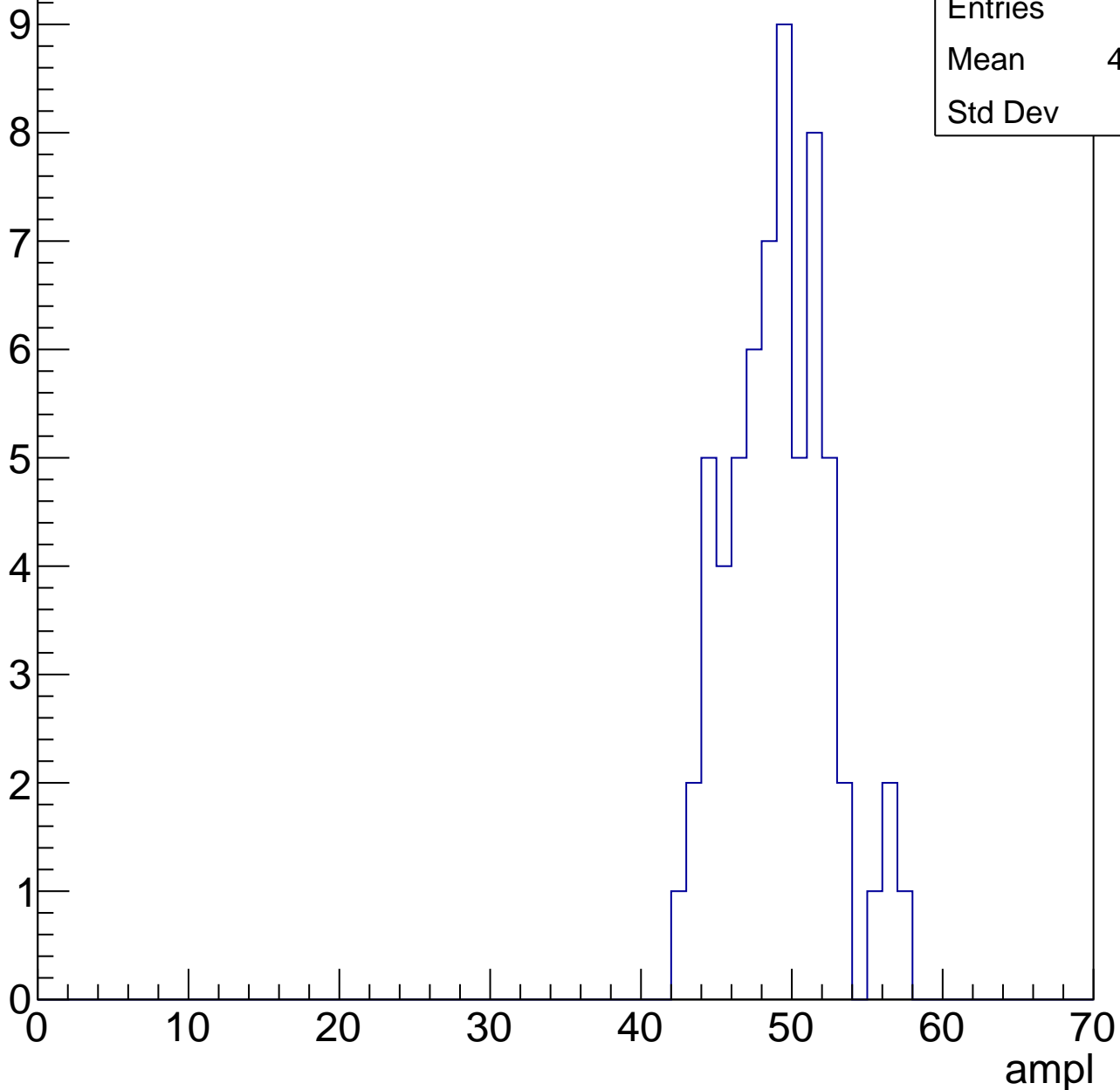


# B0L001S, U24-ch92, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	48.65
Std Dev	3.31

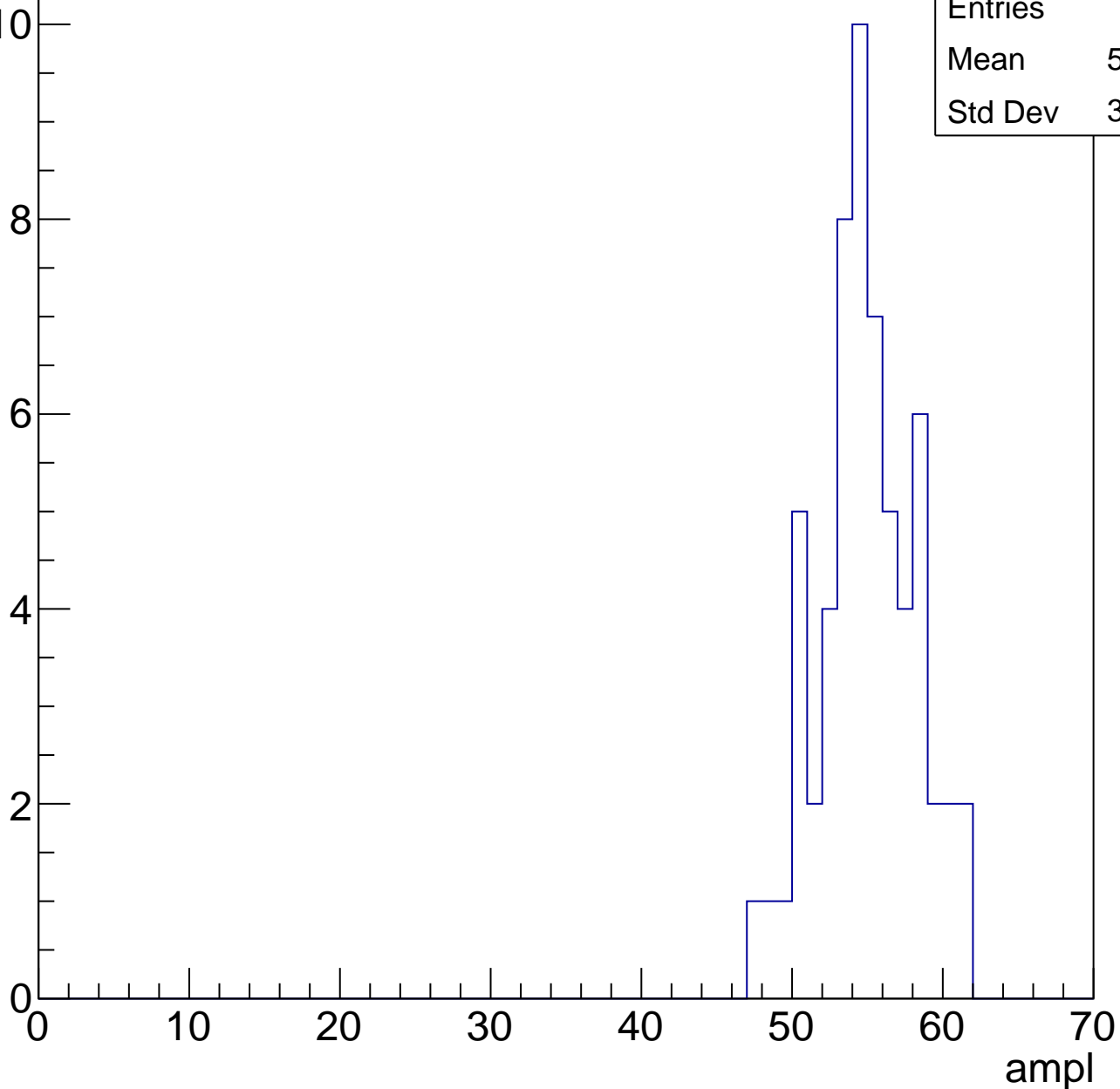


# B0L001S, U24-ch92, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	54.48
Std Dev	3.154

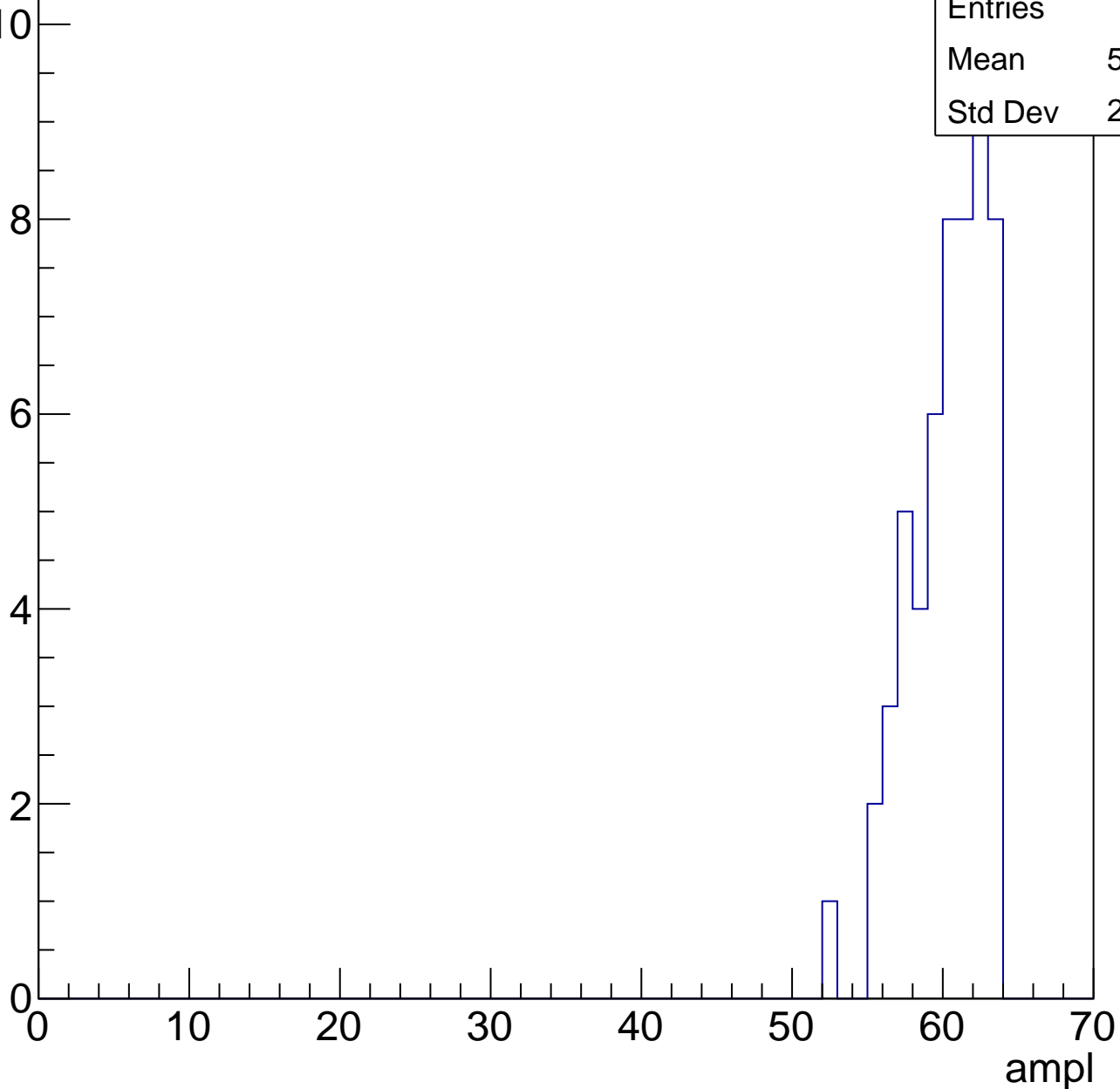


# B0L001S, U24-ch92, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	59.87
Std Dev	2.516



# B0L001S, U24-ch92, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

0 10 20 30 40 50 60 70

ampl

Entries	5
Mean	48.8
Std Dev	24.47



# B0L001S, U24-ch92, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U24-ch93, adc0

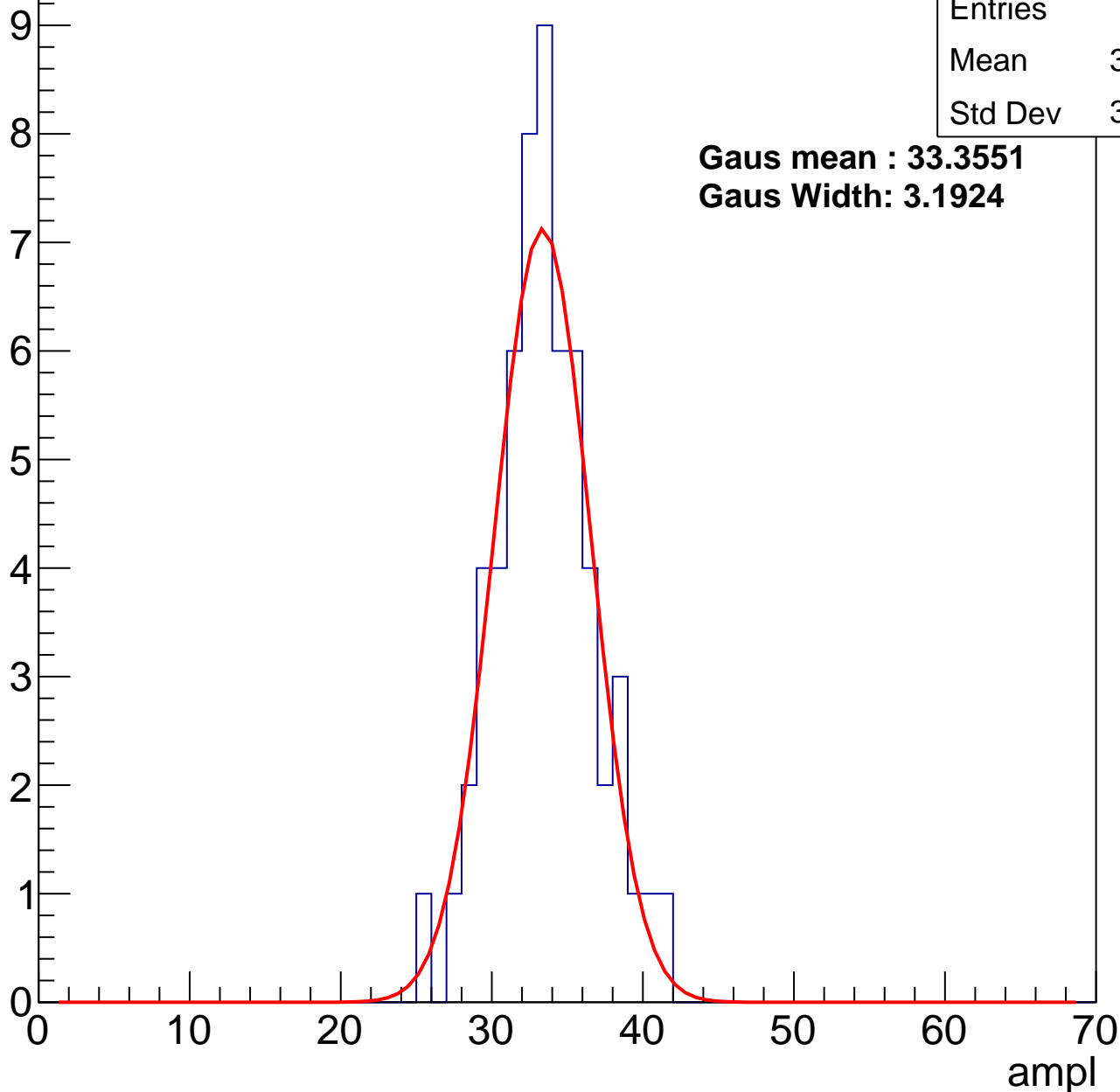
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	33.03
Std Dev	3.199

**Gaus mean : 33.3551**

**Gaus Width: 3.1924**



# B0L001S, U24-ch93, adc1

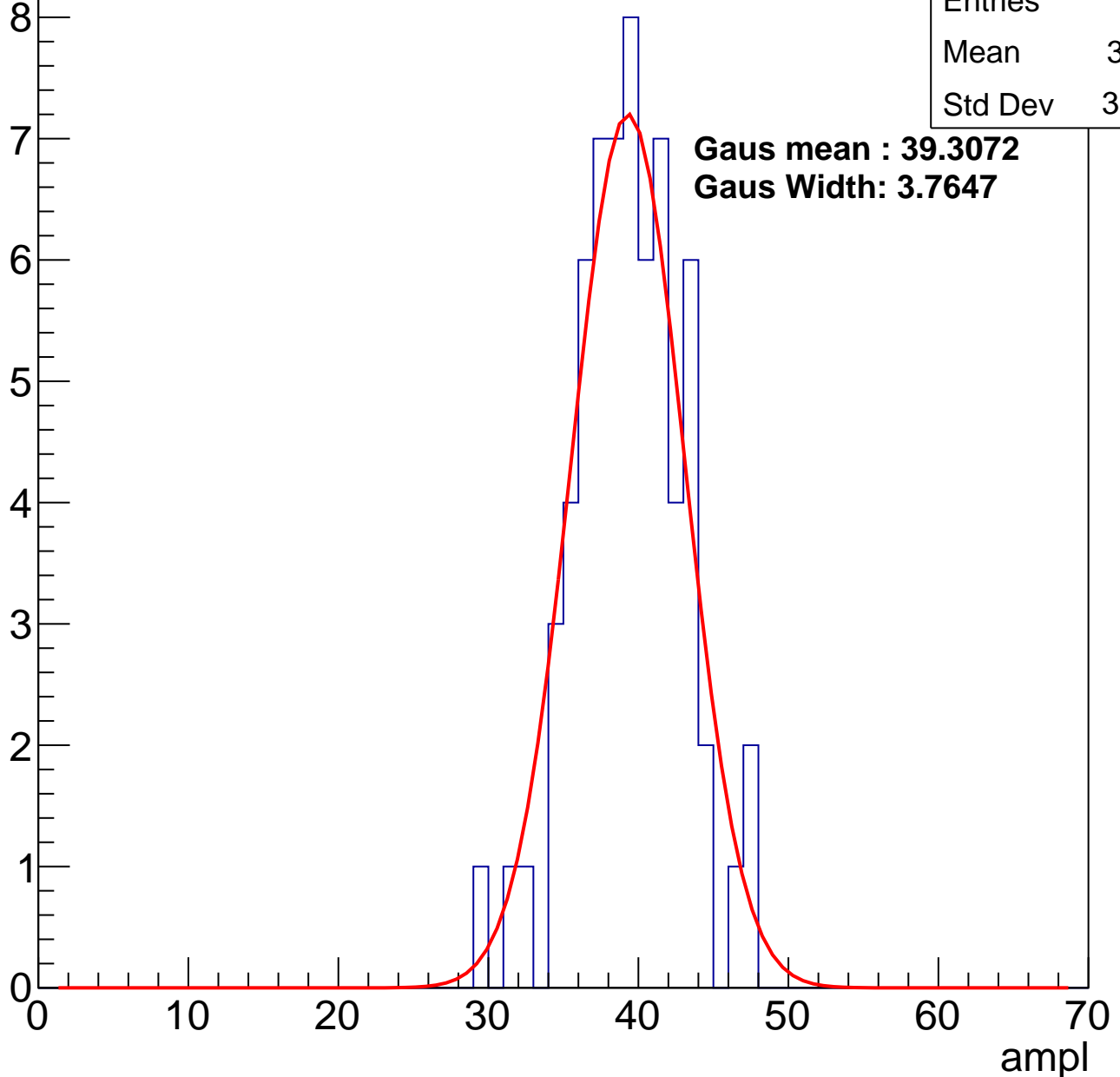
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	38.91
Std Dev	3.554

**Gaus mean : 39.3072**

**Gaus Width: 3.7647**



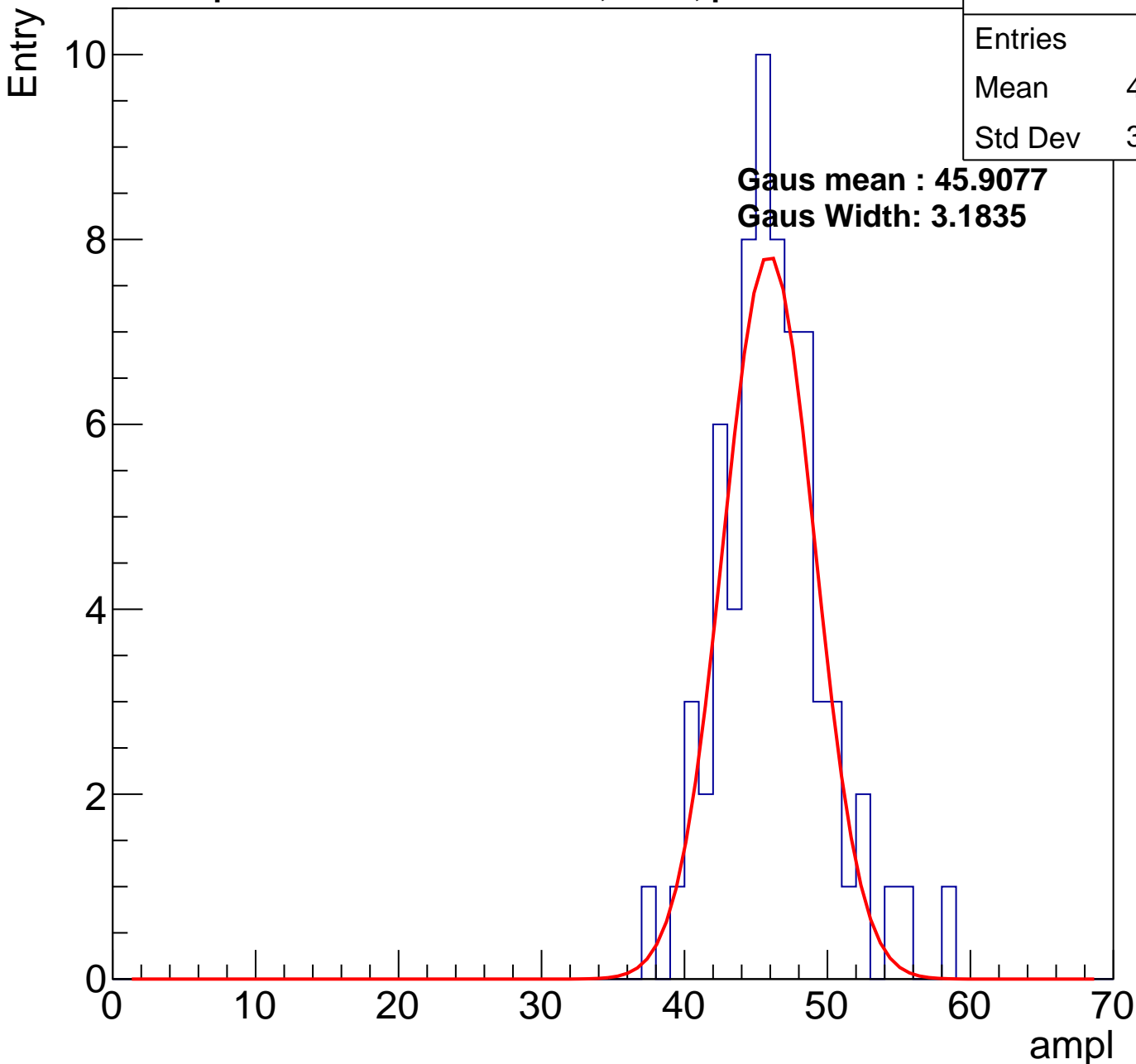
# B0L001S, U24-ch93, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	69
Mean	45.74
Std Dev	3.717

**Gaus mean : 45.9077**

**Gaus Width: 3.1835**

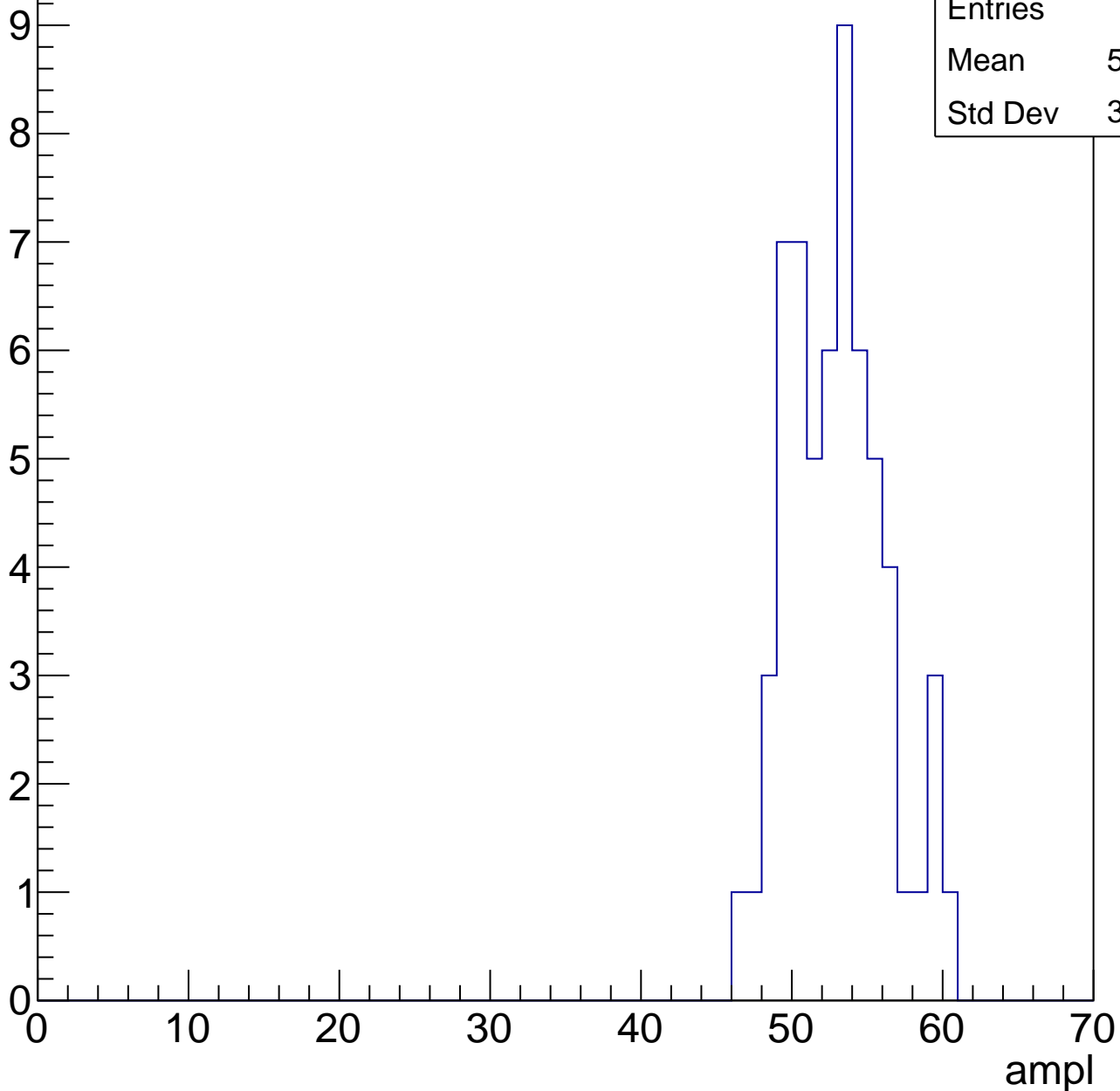


# B0L001S, U24-ch93, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	52.48
Std Dev	3.175

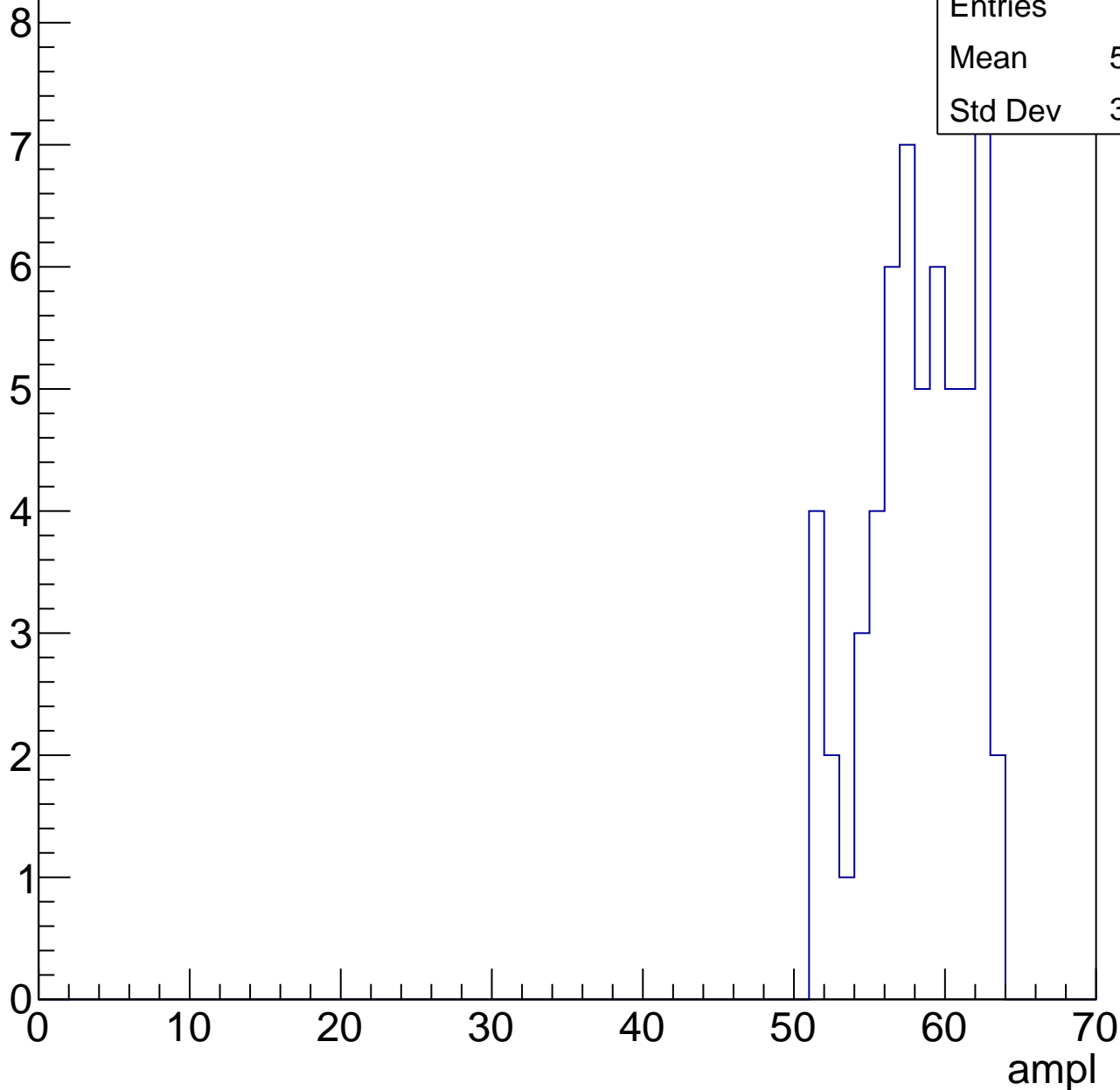


# B0L001S, U24-ch93, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	57.74
Std Dev	3.356

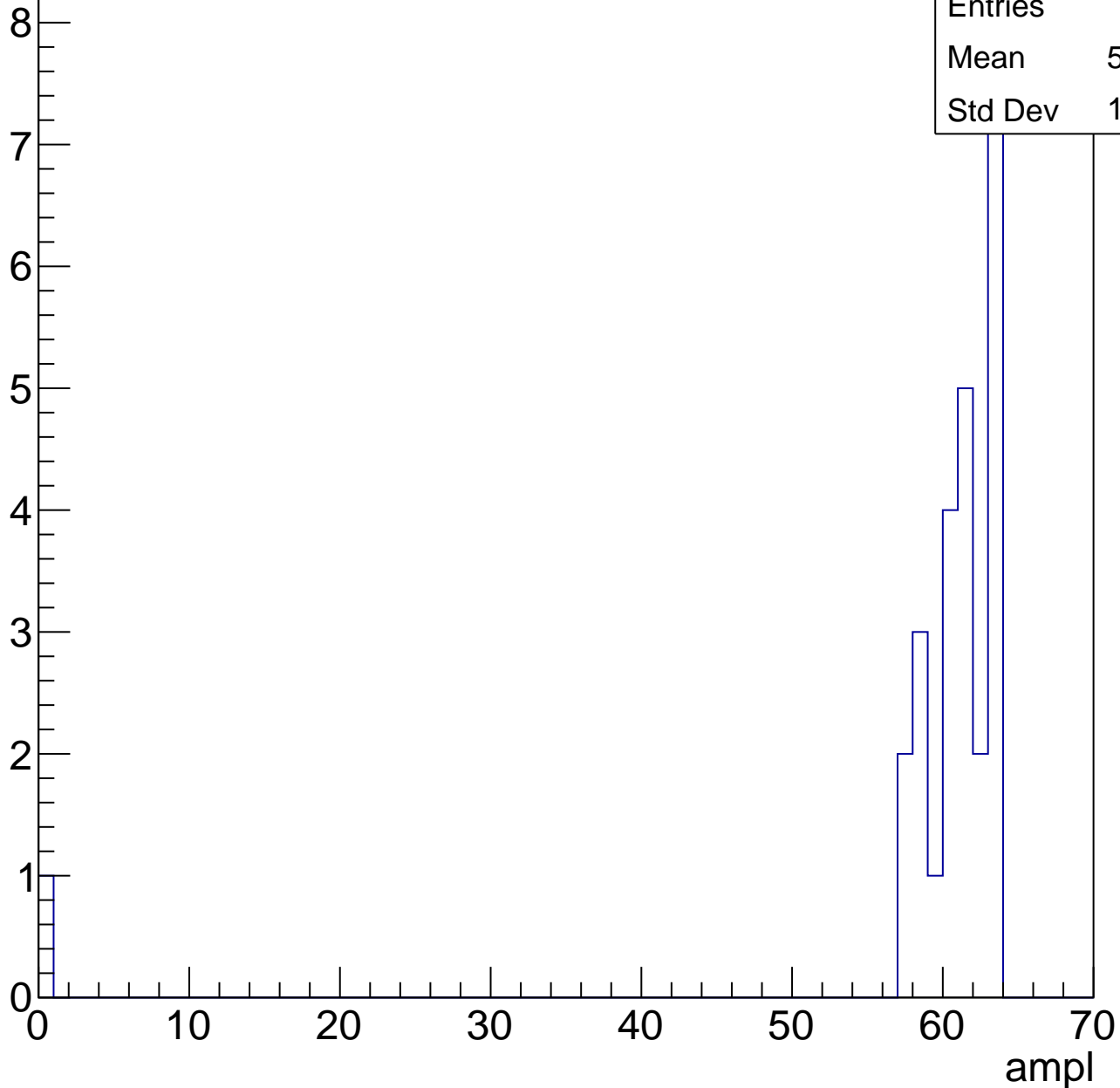


# B0L001S, U24-ch93, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	26
Mean	58.46
Std Dev	11.86



# B0L001S, U24-ch93, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U24-ch93, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U24-ch94, adc0

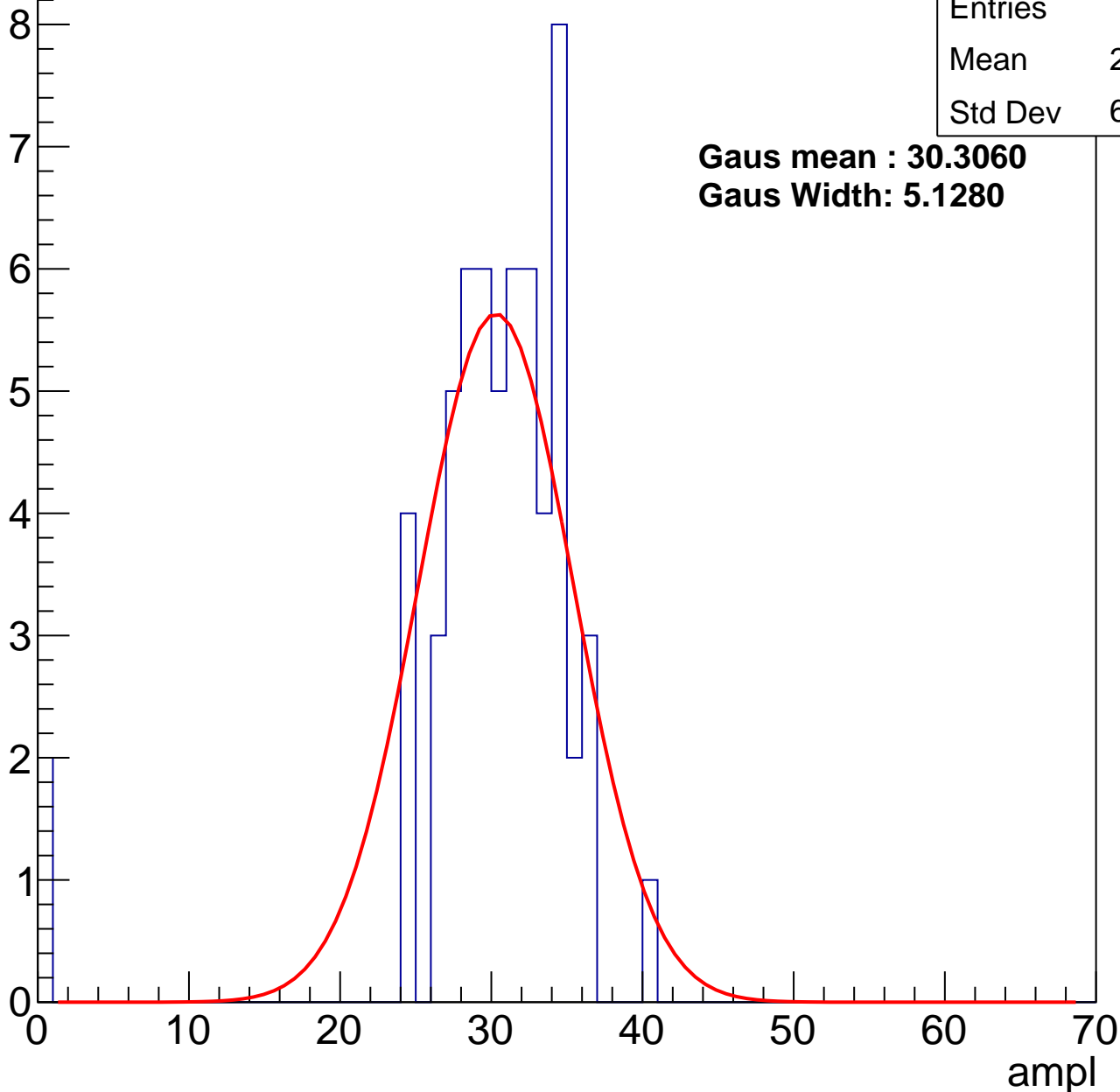
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	29.52
Std Dev	6.409

**Gaus mean : 30.3060**

**Gaus Width: 5.1280**



# B0L001S, U24-ch94, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	58
Mean	37.02
Std Dev	3.411

**Gaus mean : 37.5723**

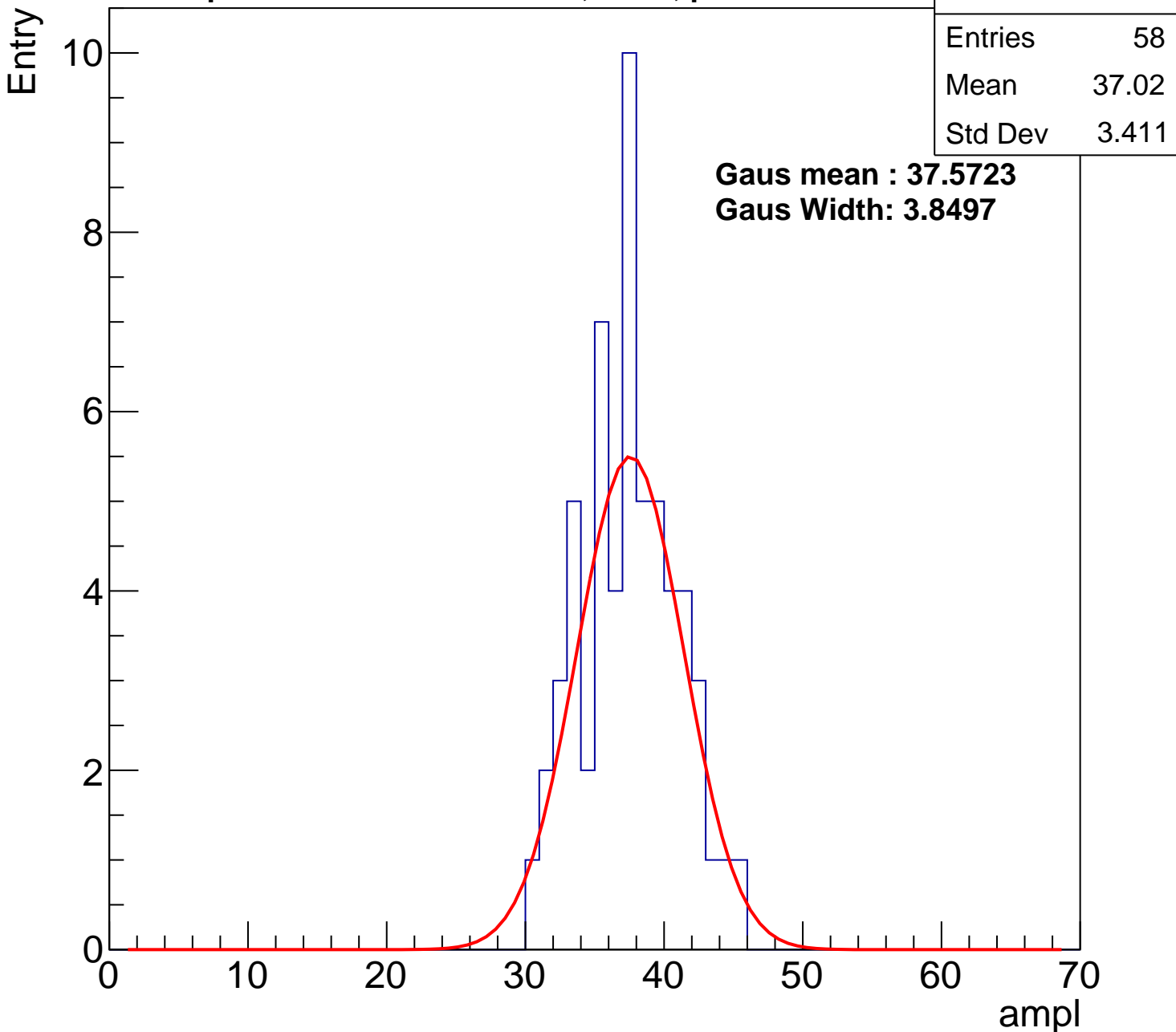
**Gaus Width: 3.8497**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U24-ch94, adc2

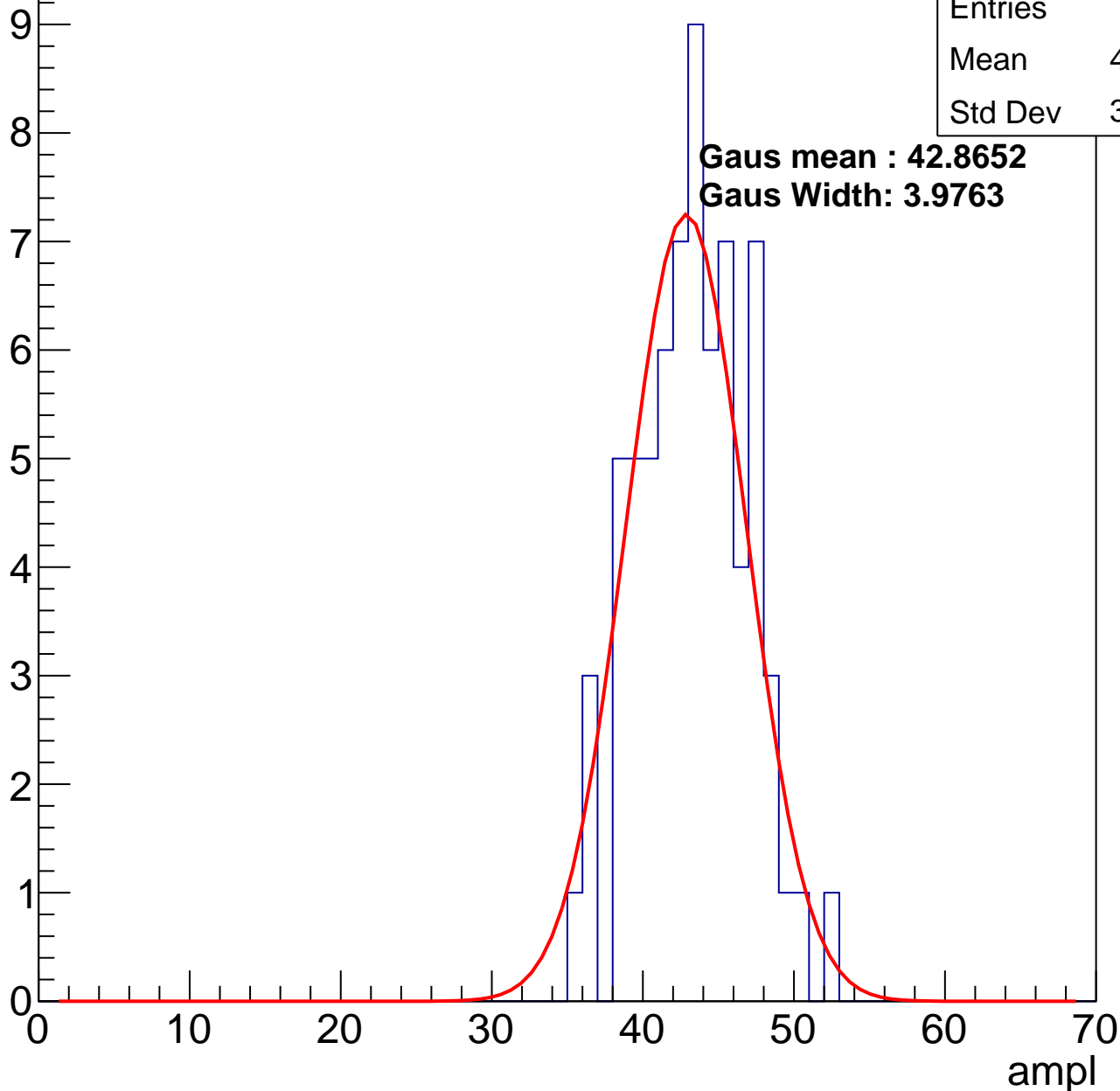
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	42.85
Std Dev	3.587

**Gaus mean : 42.8652**

**Gaus Width: 3.9763**

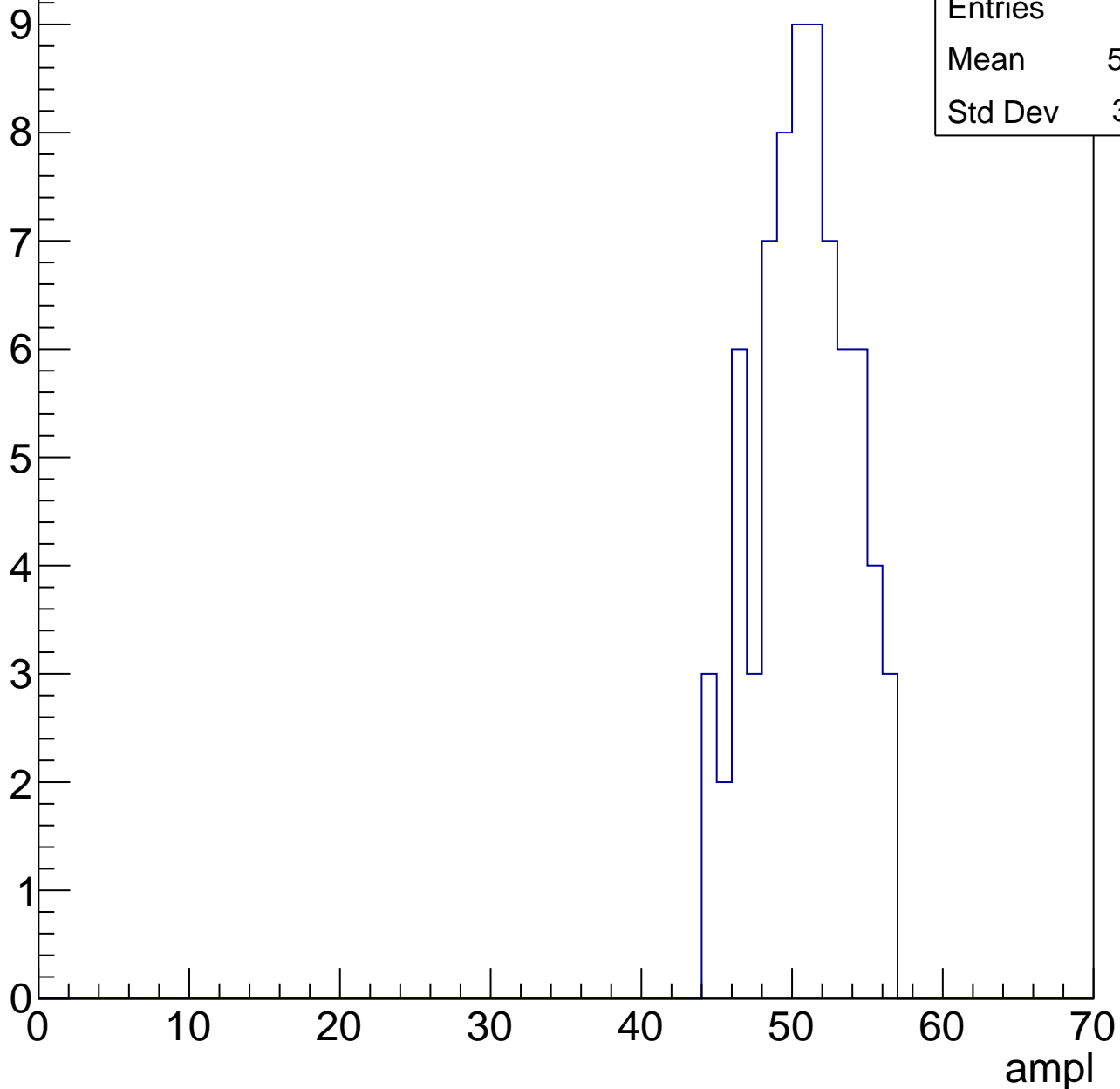


# B0L001S, U24-ch94, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	50.27
Std Dev	3.111

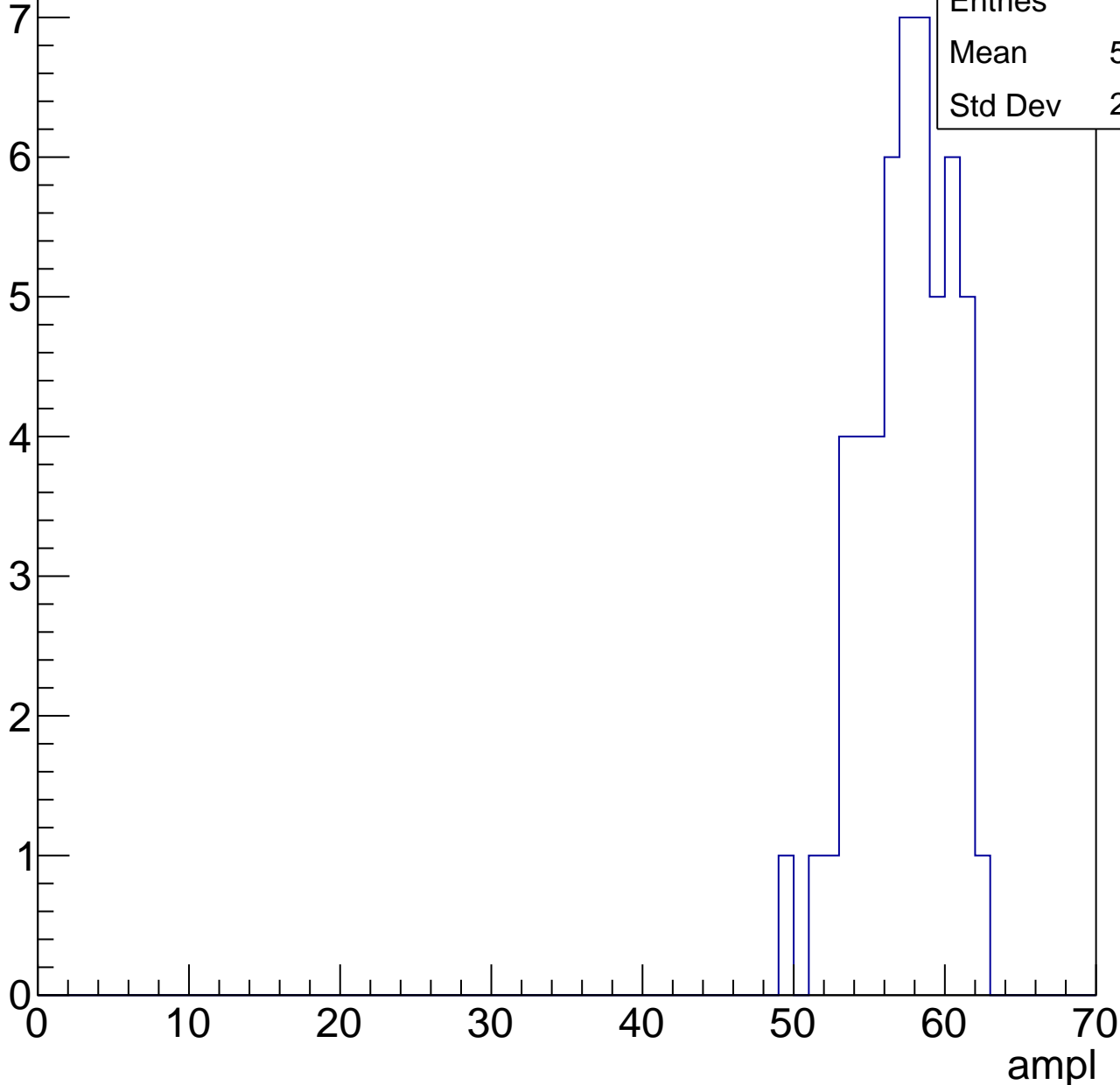


# B0L001S, U24-ch94, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	56.98
Std Dev	2.886

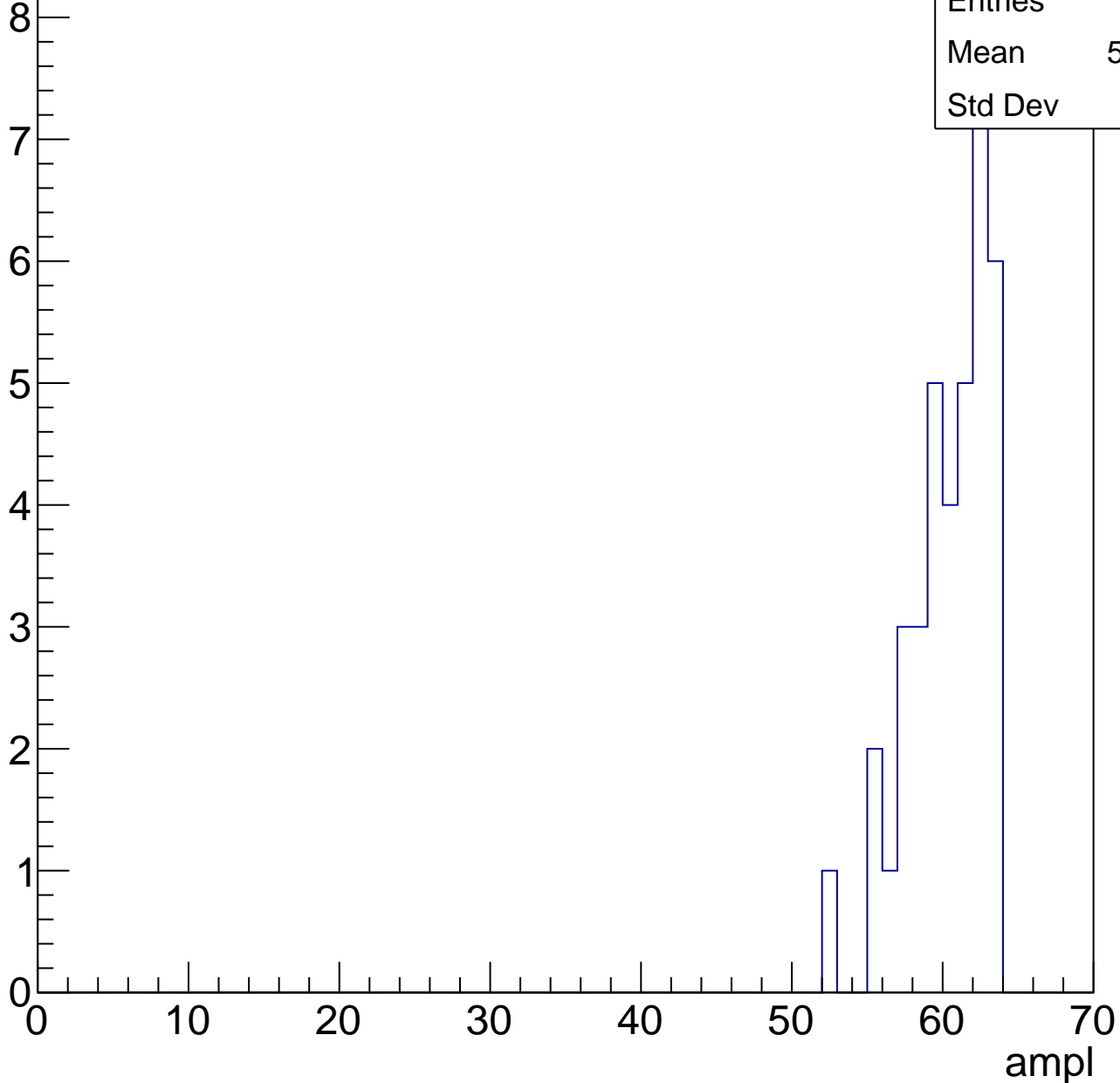


# B0L001S, U24-ch94, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

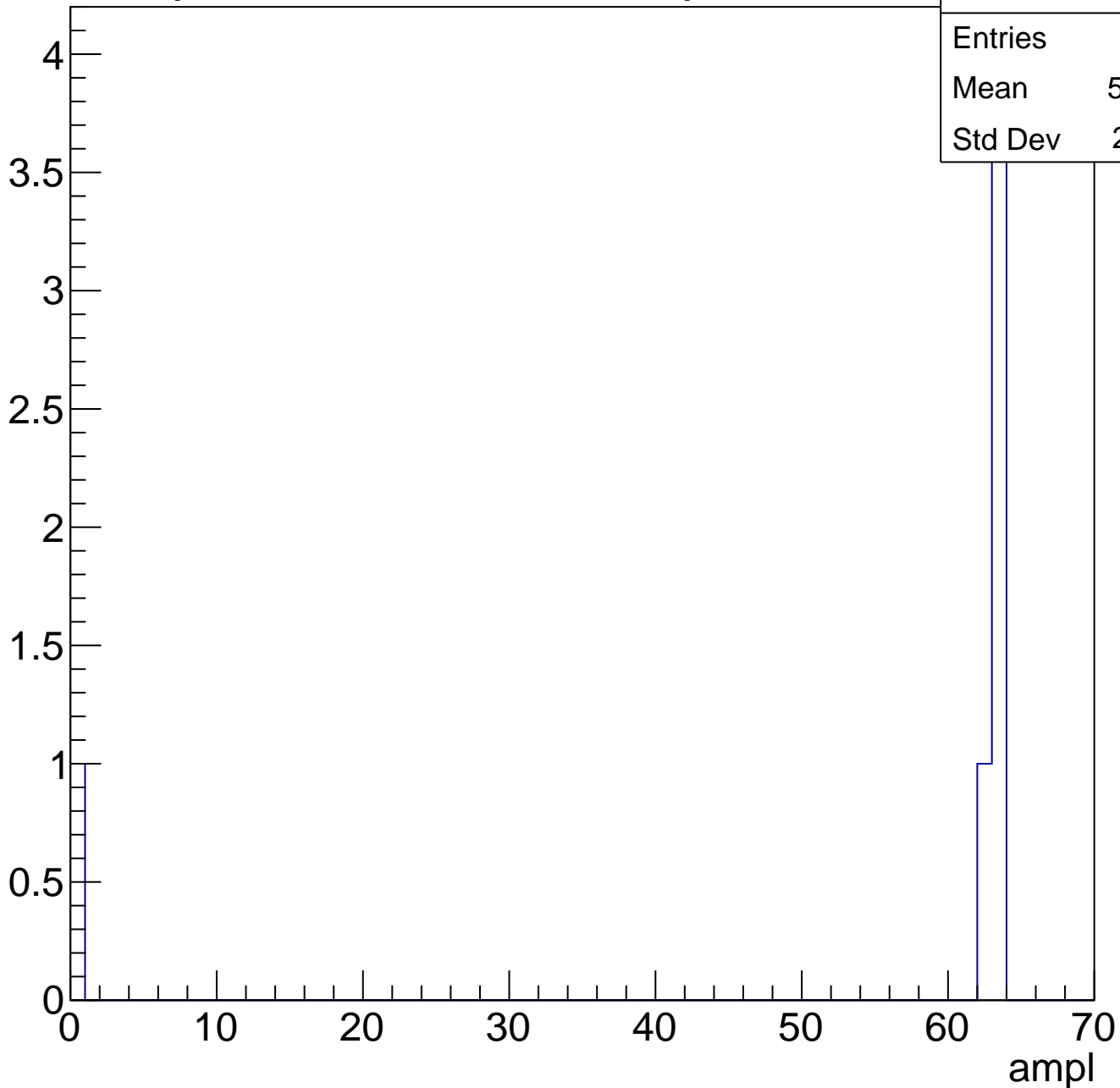
Entries	38
Mean	59.92
Std Dev	2.64



# B0L001S, U24-ch94, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	6
Mean	52.33
Std Dev	23.41



# B0L001S, U24-ch94, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U24-ch95, adc0

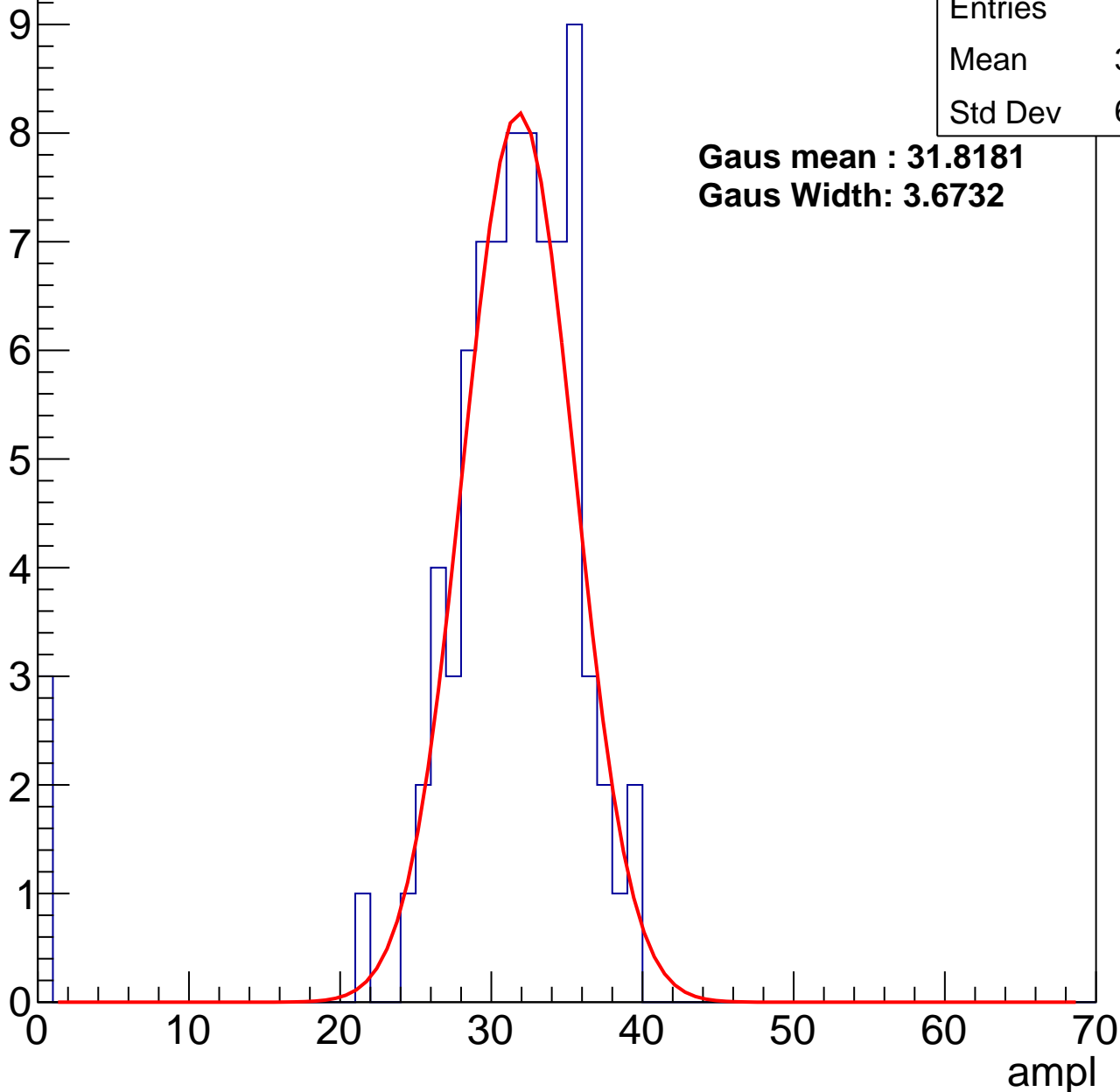
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	81
Mean	30.21
Std Dev	6.901

**Gaus mean : 31.8181**

**Gaus Width: 3.6732**



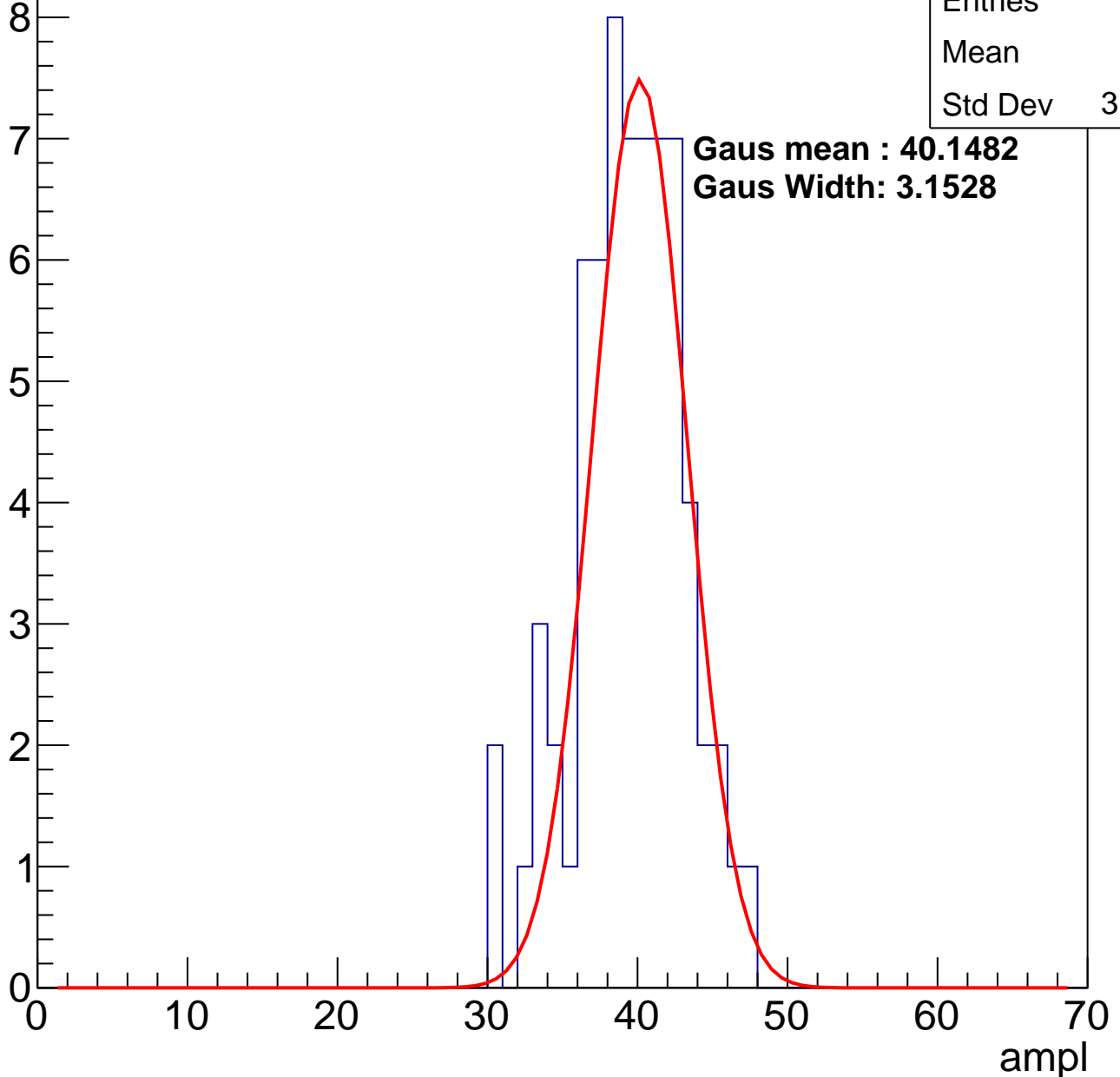
# B0L001S, U24-ch95, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	39
Std Dev	3.599

**Gaus mean : 40.1482**  
**Gaus Width: 3.1528**



# B0L001S, U24-ch95, adc2

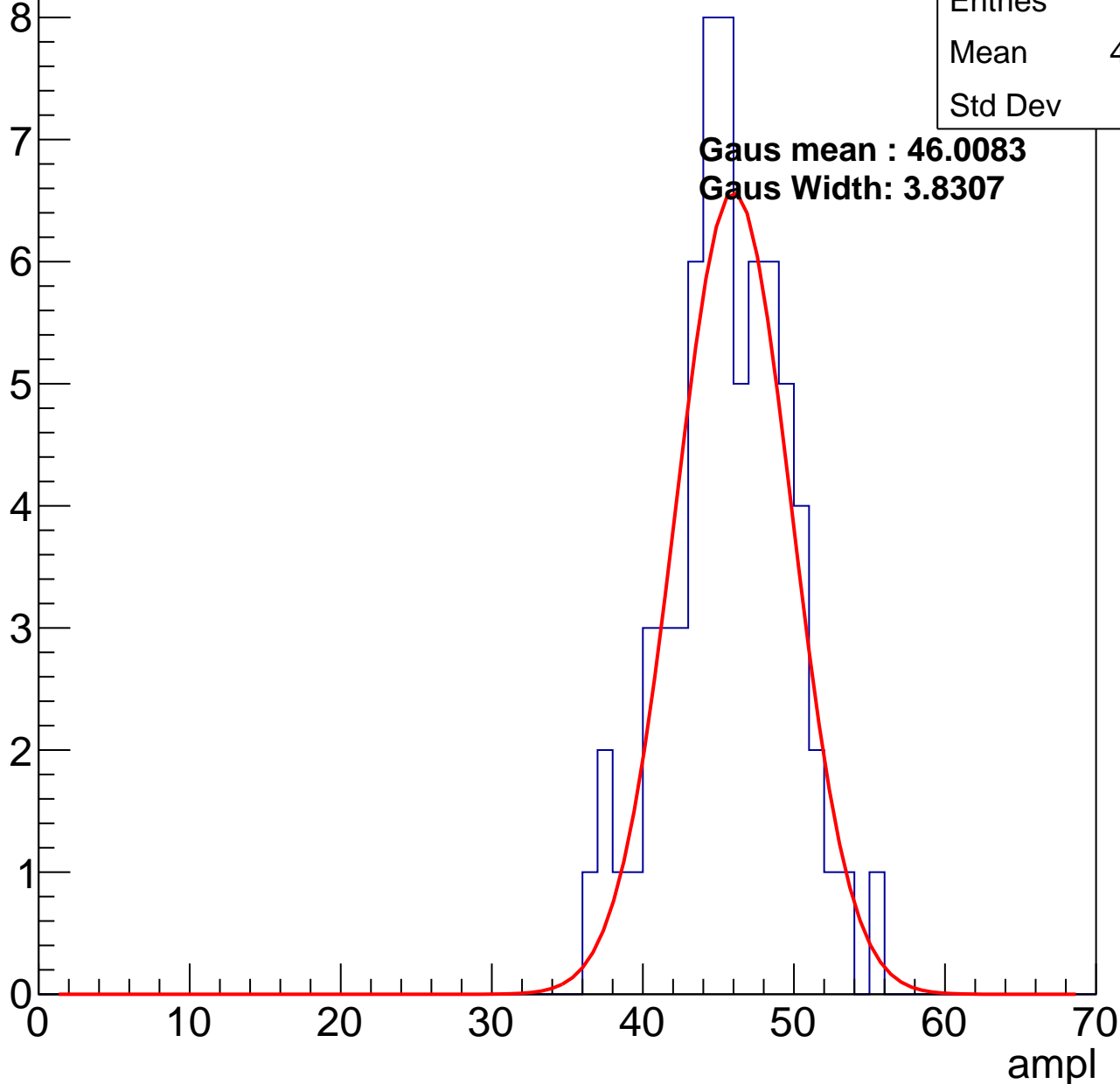
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	45.27
Std Dev	3.9

**Gaus mean : 46.0083**

**Gaus Width: 3.8307**

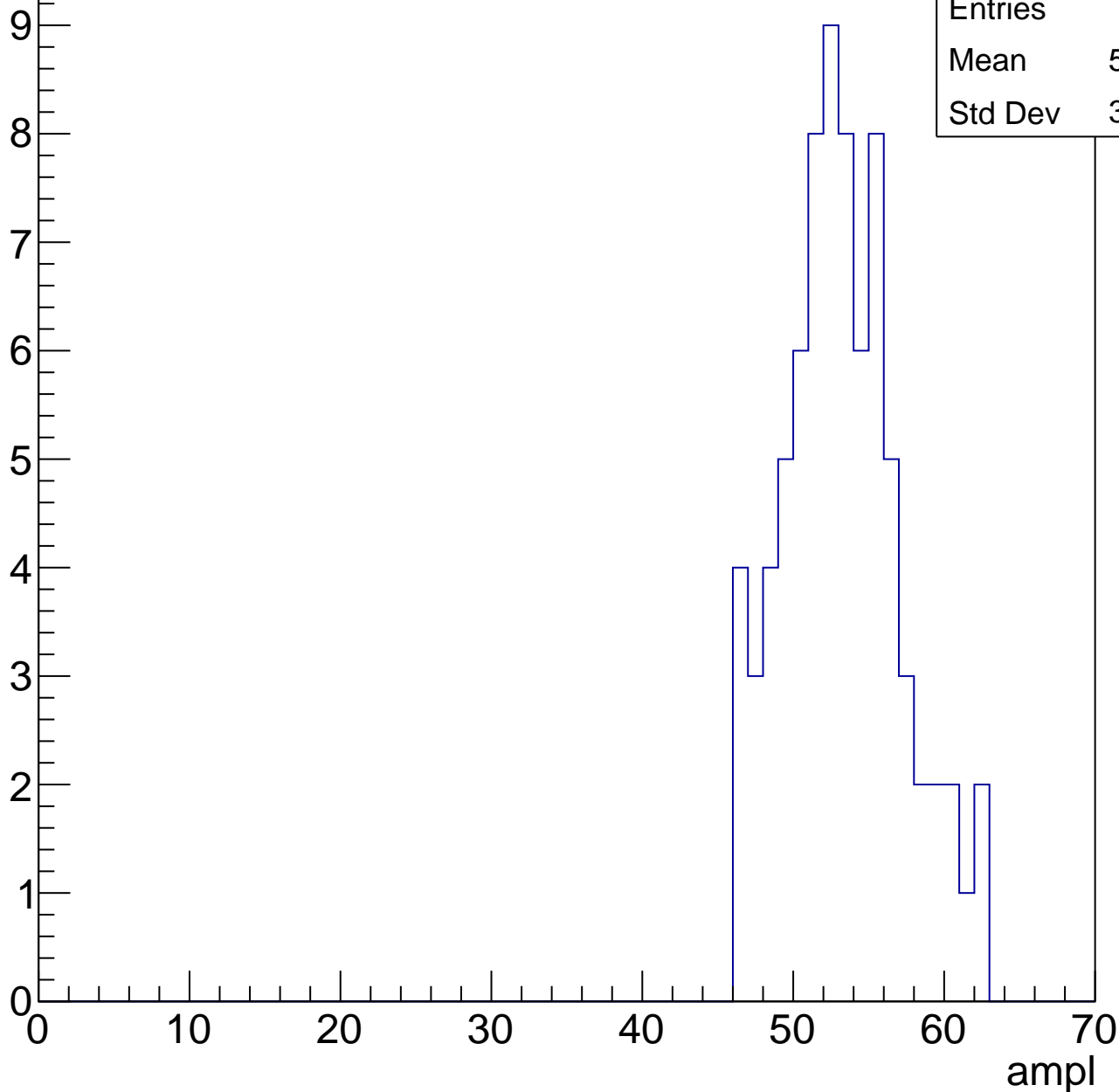


# B0L001S, U24-ch95, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	78
Mean	52.77
Std Dev	3.843

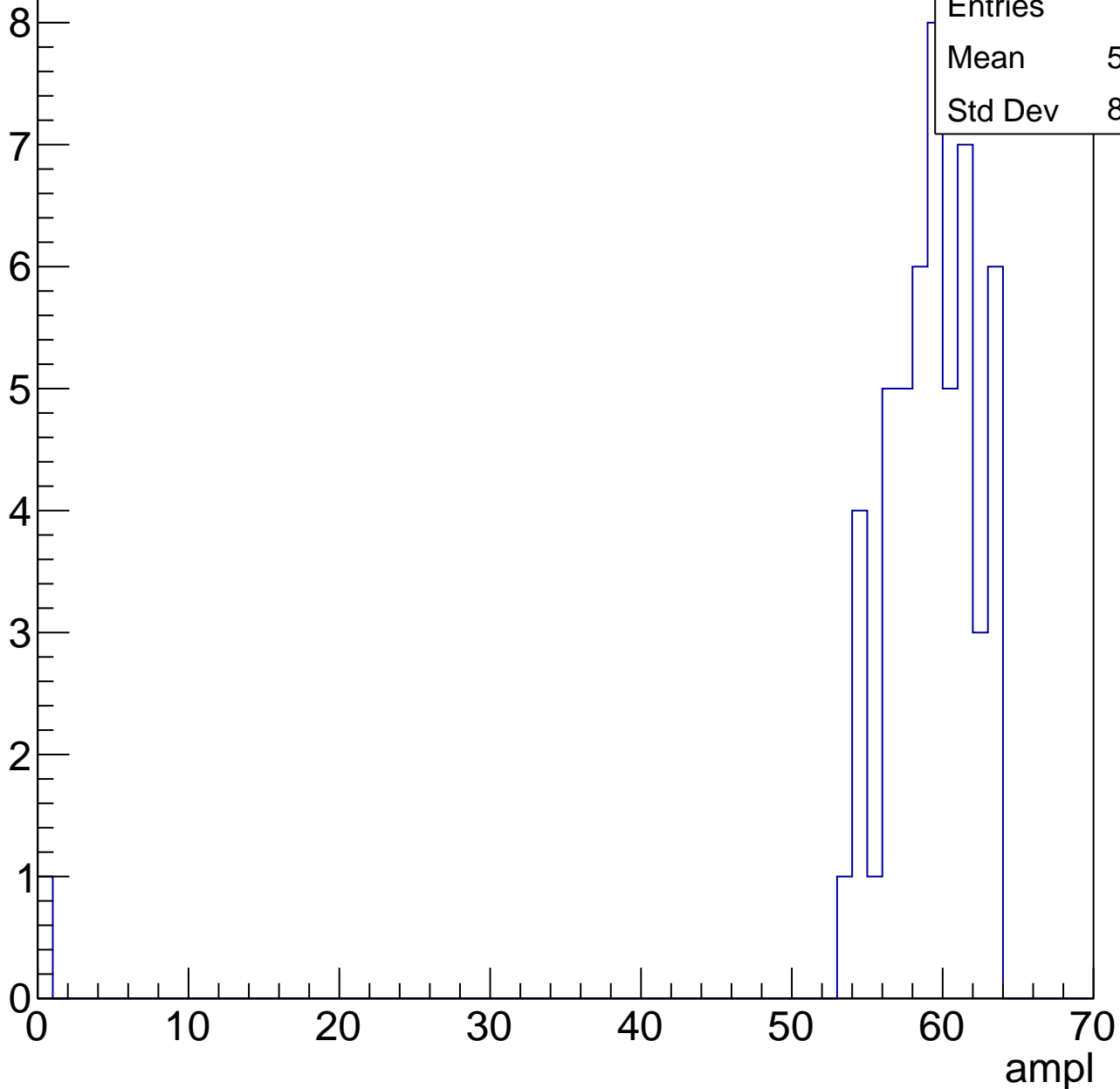


# B0L001S, U24-ch95, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	57.69
Std Dev	8.516

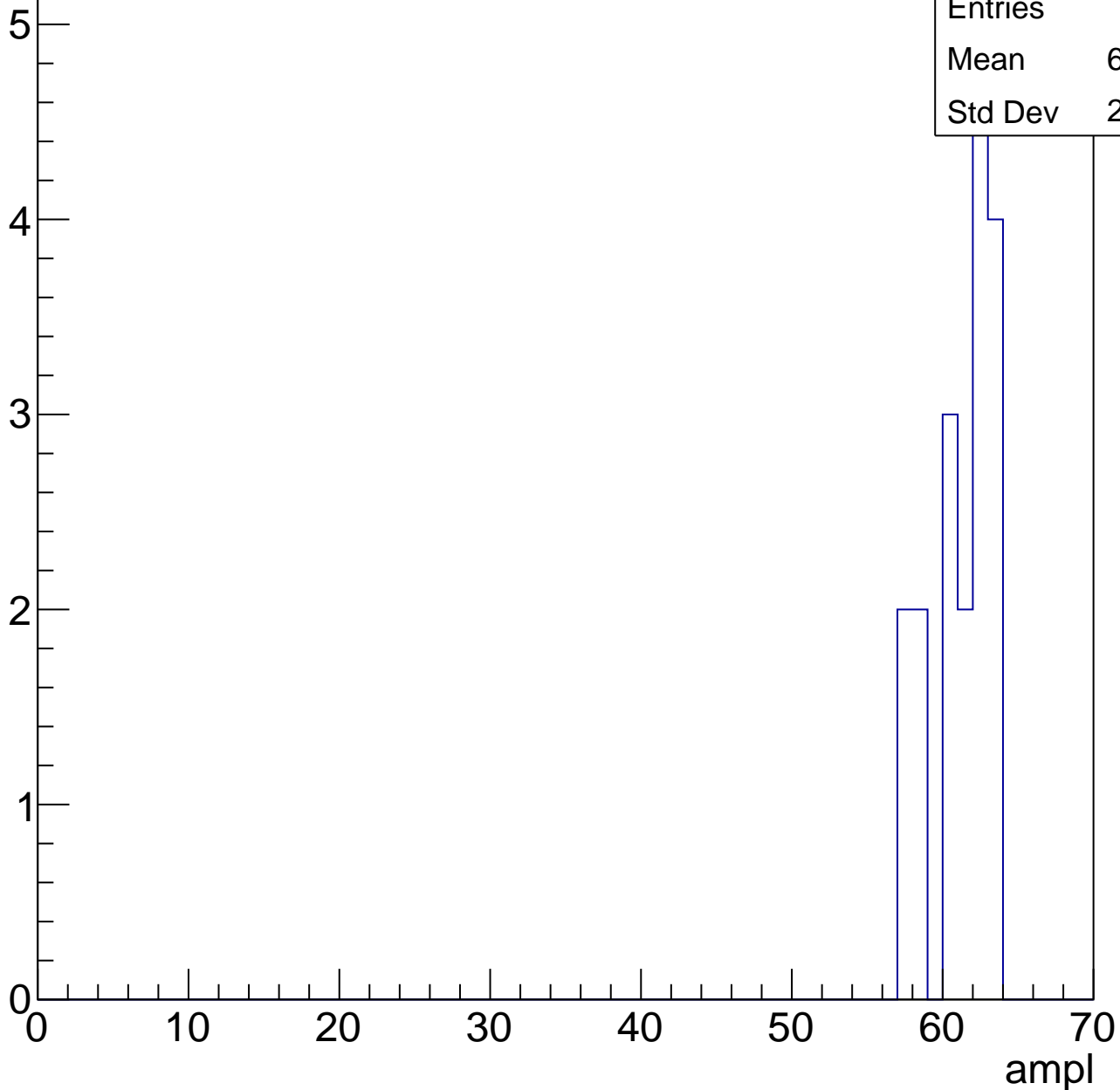


# B0L001S, U24-ch95, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	18
Mean	60.78
Std Dev	2.015



# B0L001S, U24-ch95, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U24-ch95, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L001S, U24-ch96, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	72
Mean	32.04
Std Dev	3.352

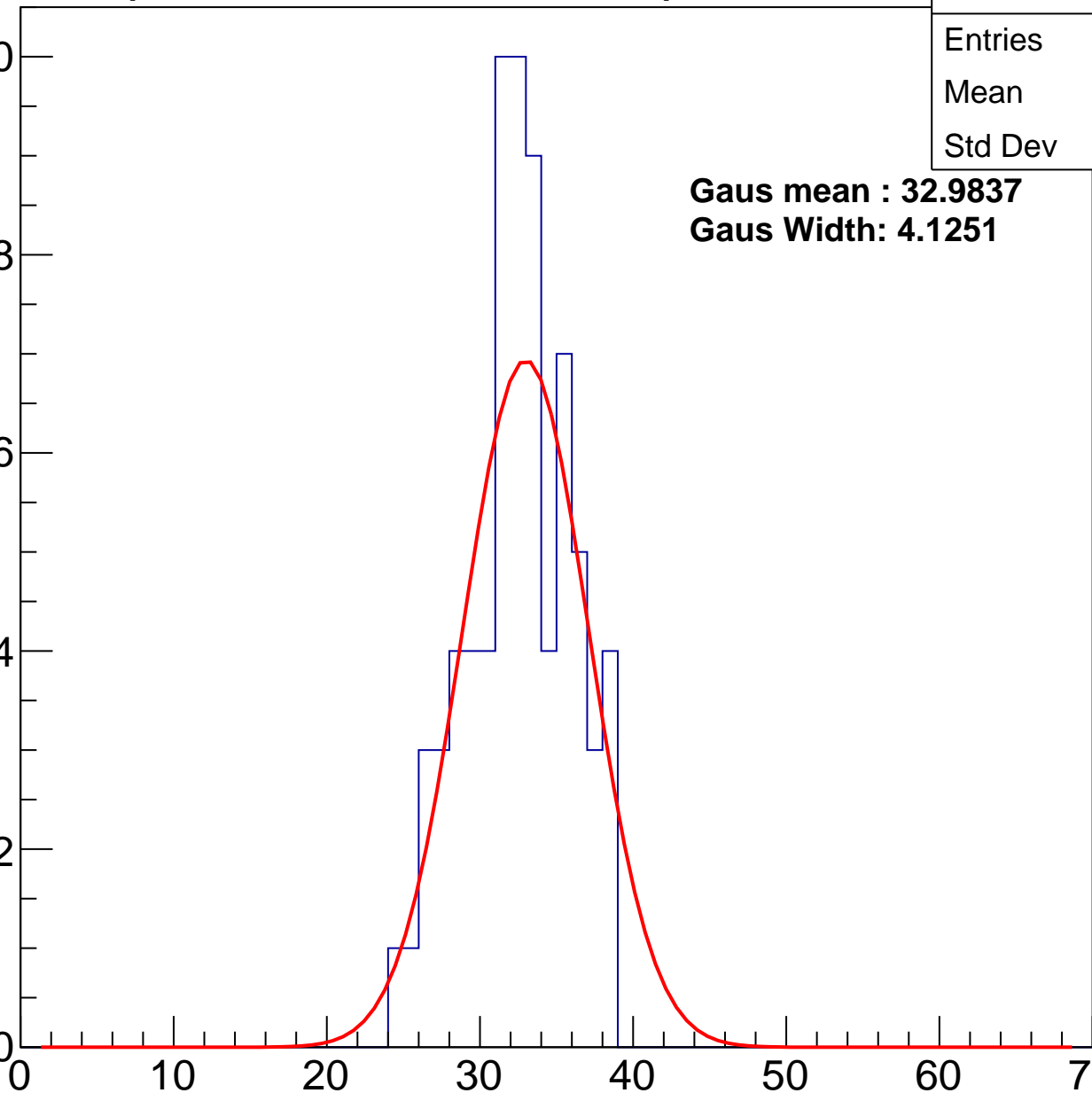
**Gaus mean : 32.9837**

**Gaus Width: 4.1251**

Entry

10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch96, adc1

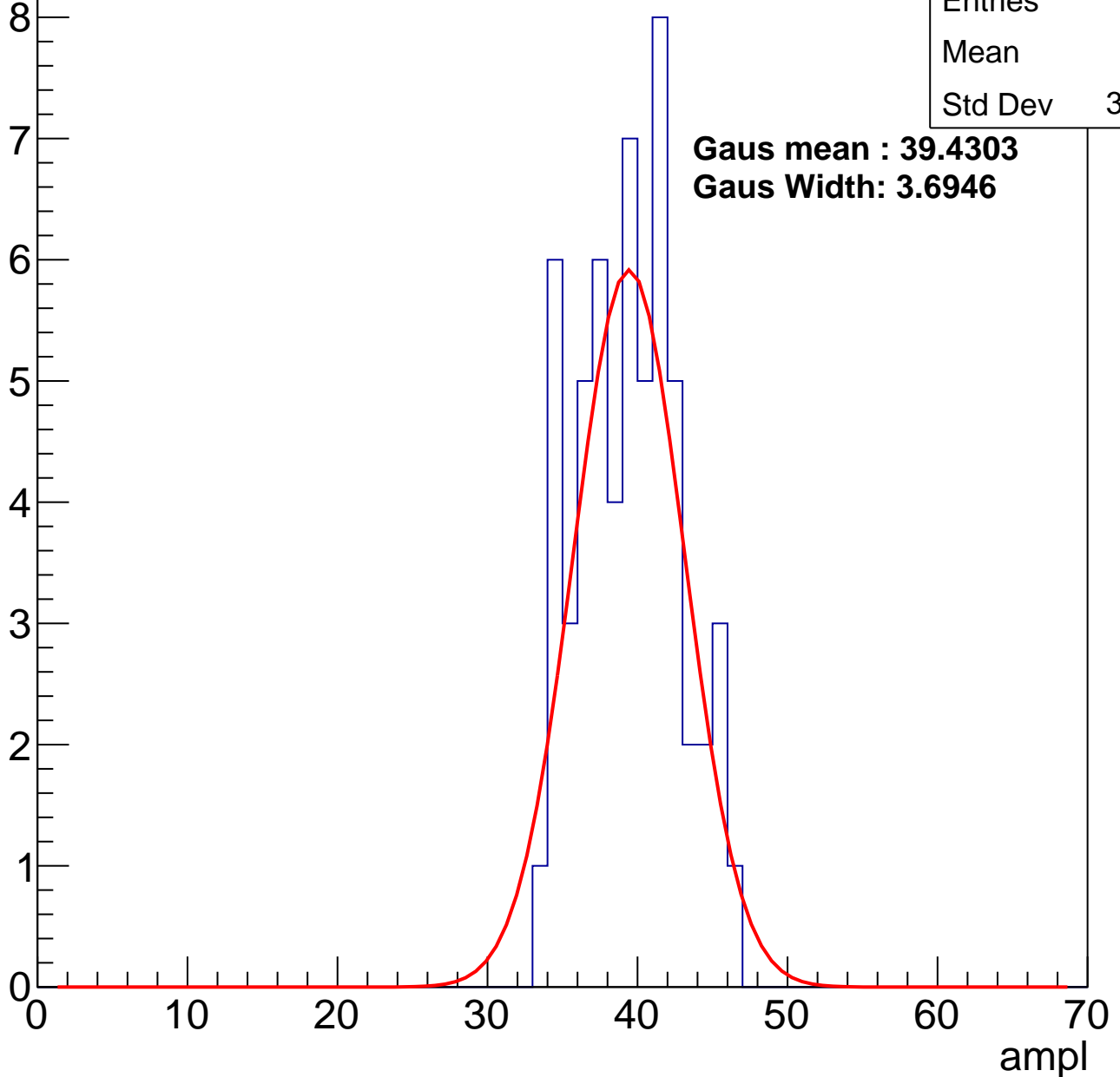
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	39
Std Dev	3.291

**Gaus mean : 39.4303**

**Gaus Width: 3.6946**



# B0L001S, U24-ch96, adc2

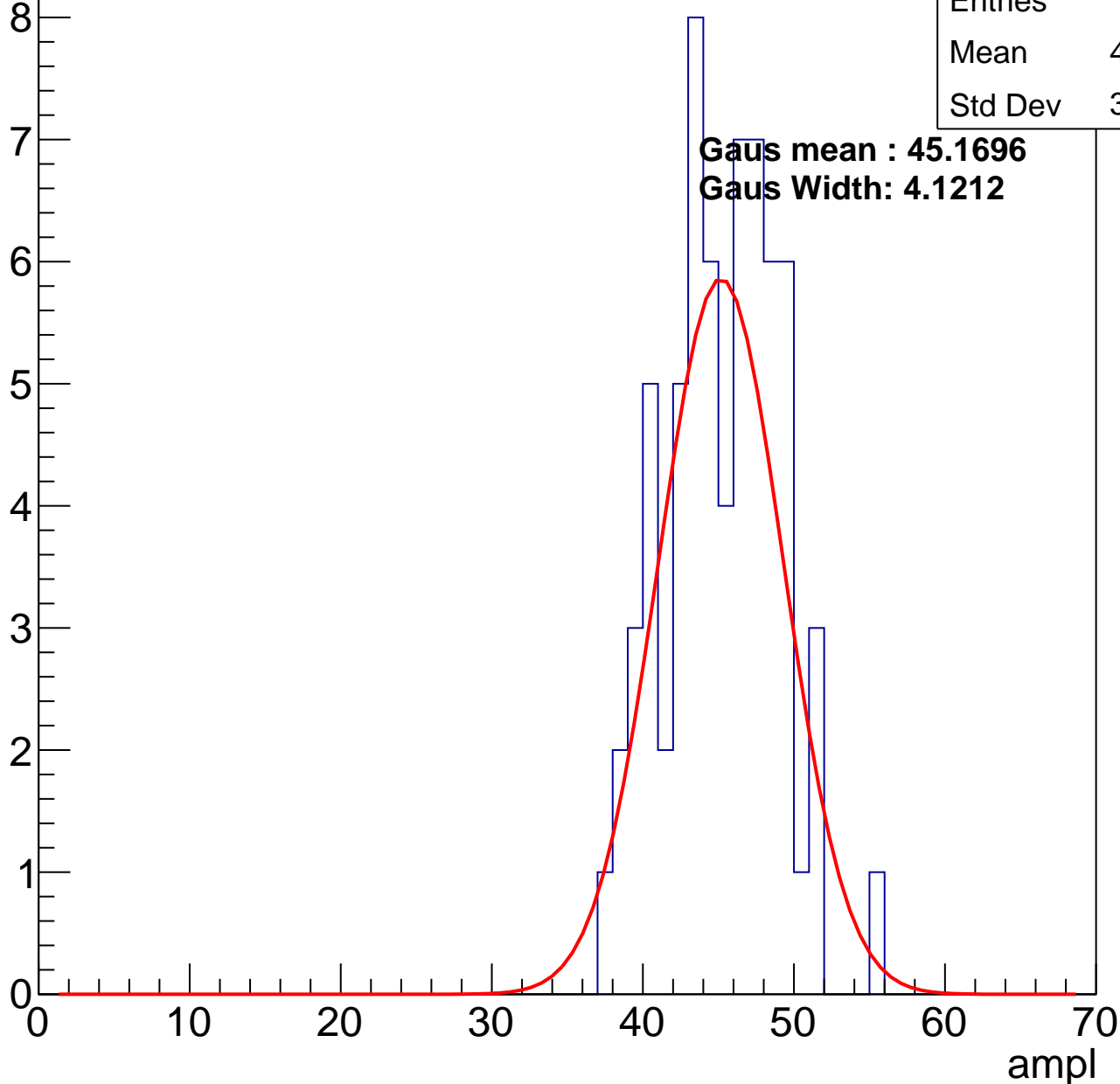
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	44.79
Std Dev	3.716

**Gaus mean : 45.1696**

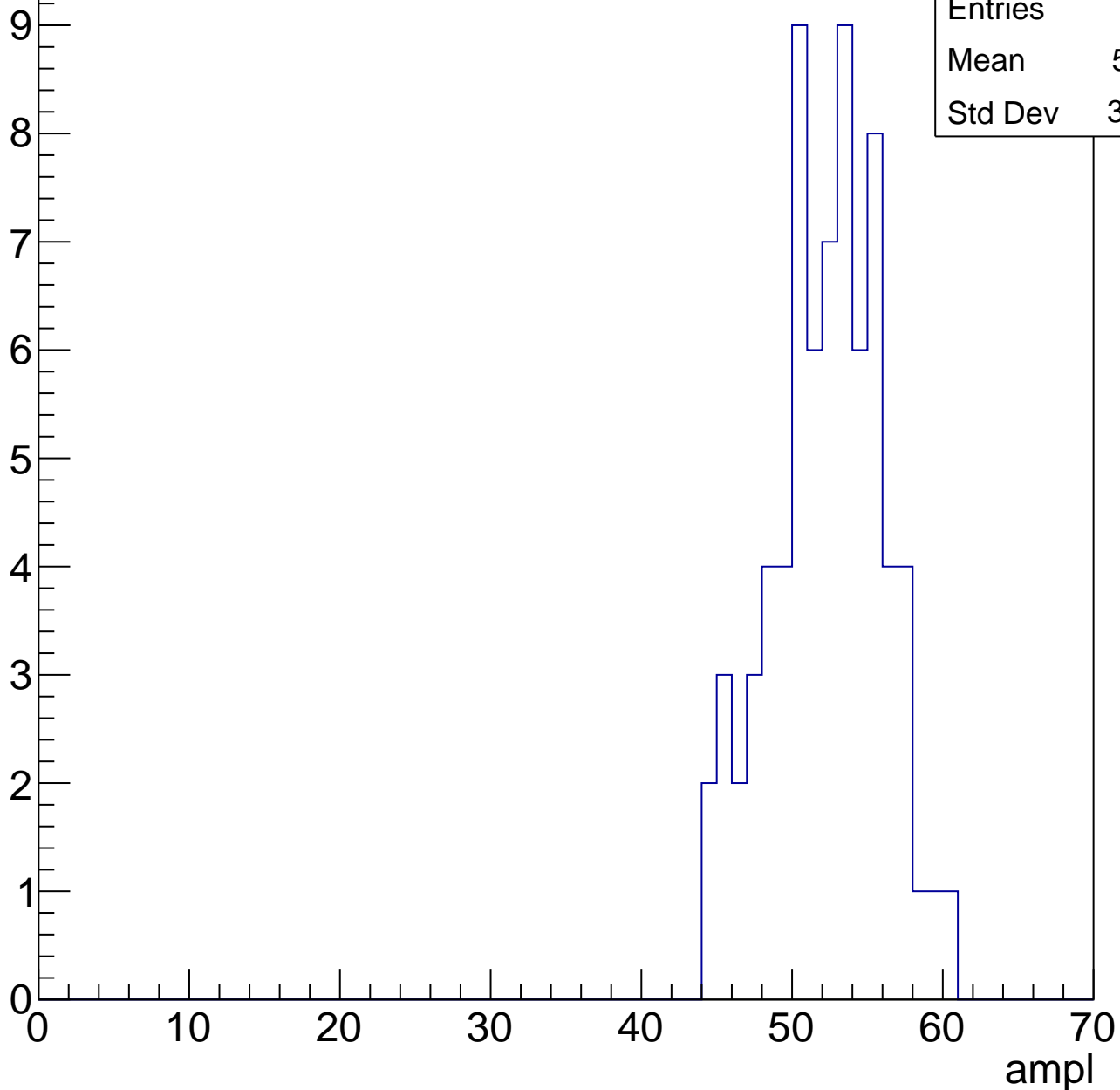
**Gaus Width: 4.1212**



# B0L001S, U24-ch96, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



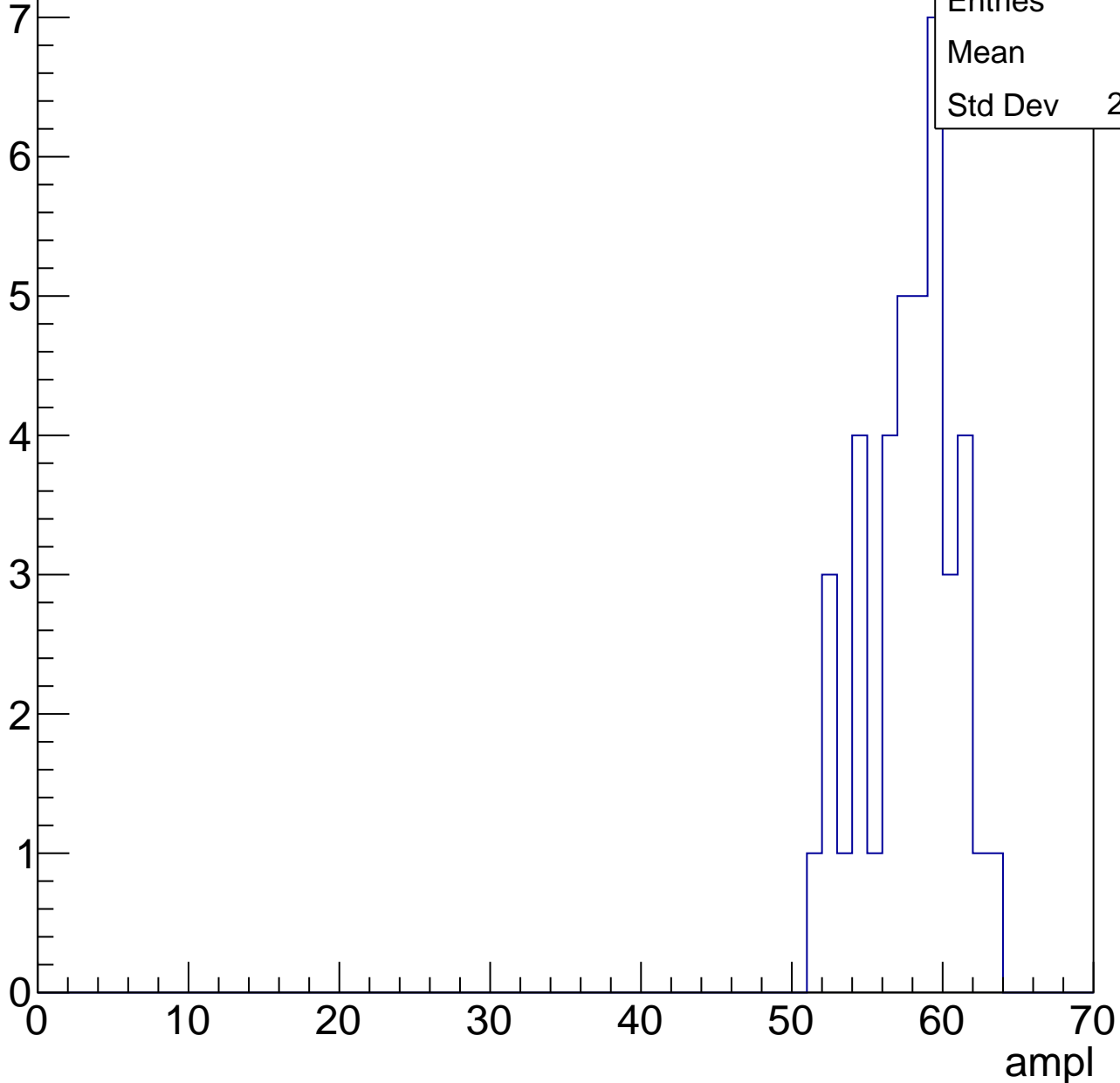
Entries	74
Mean	51.81
Std Dev	3.638

# B0L001S, U24-ch96, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	40
Mean	57.3
Std Dev	2.968

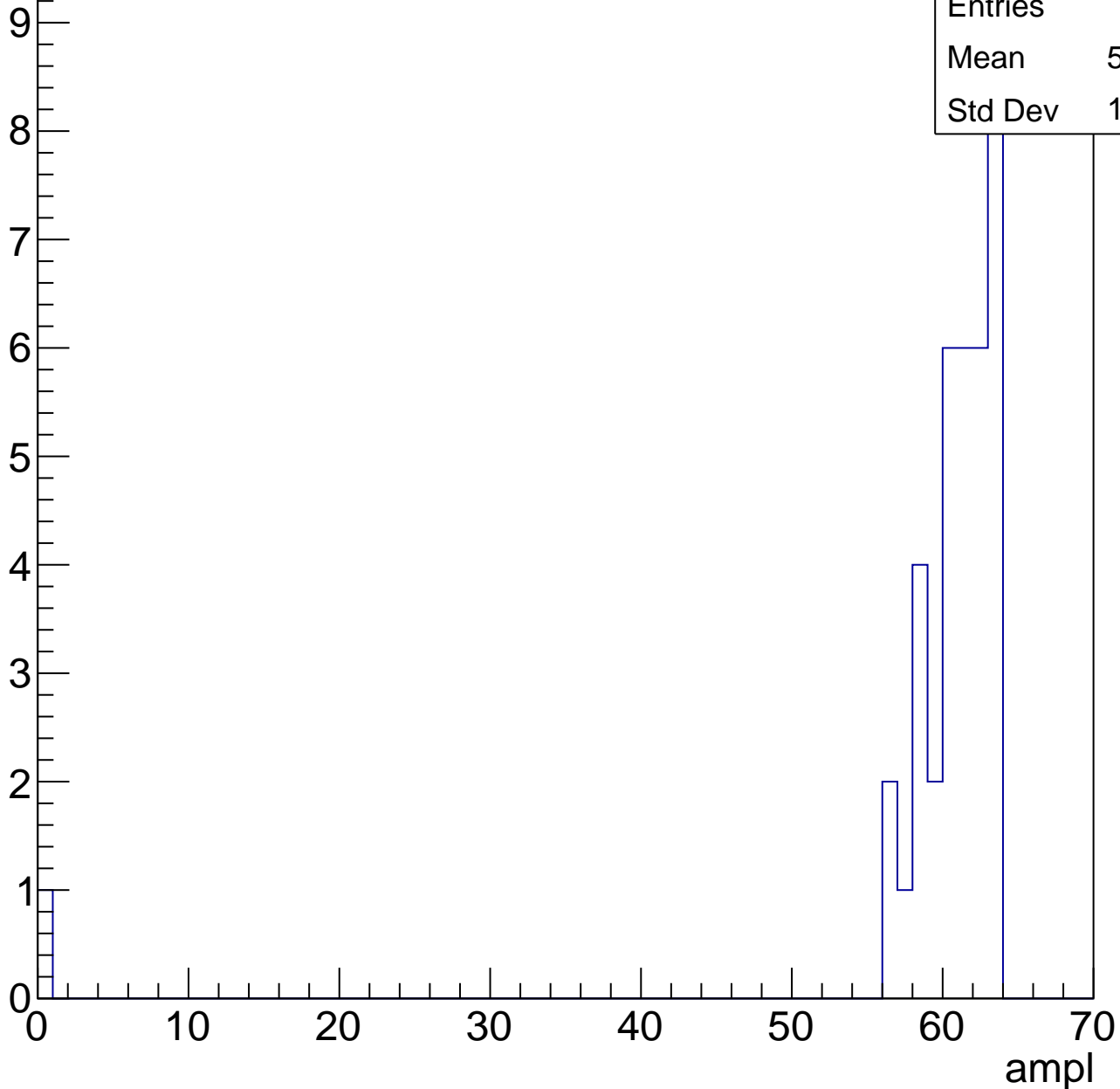


# B0L001S, U24-ch96, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	37
Mean	59.03
Std Dev	10.05



# B0L001S, U24-ch96, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch96, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U24-ch97, adc0

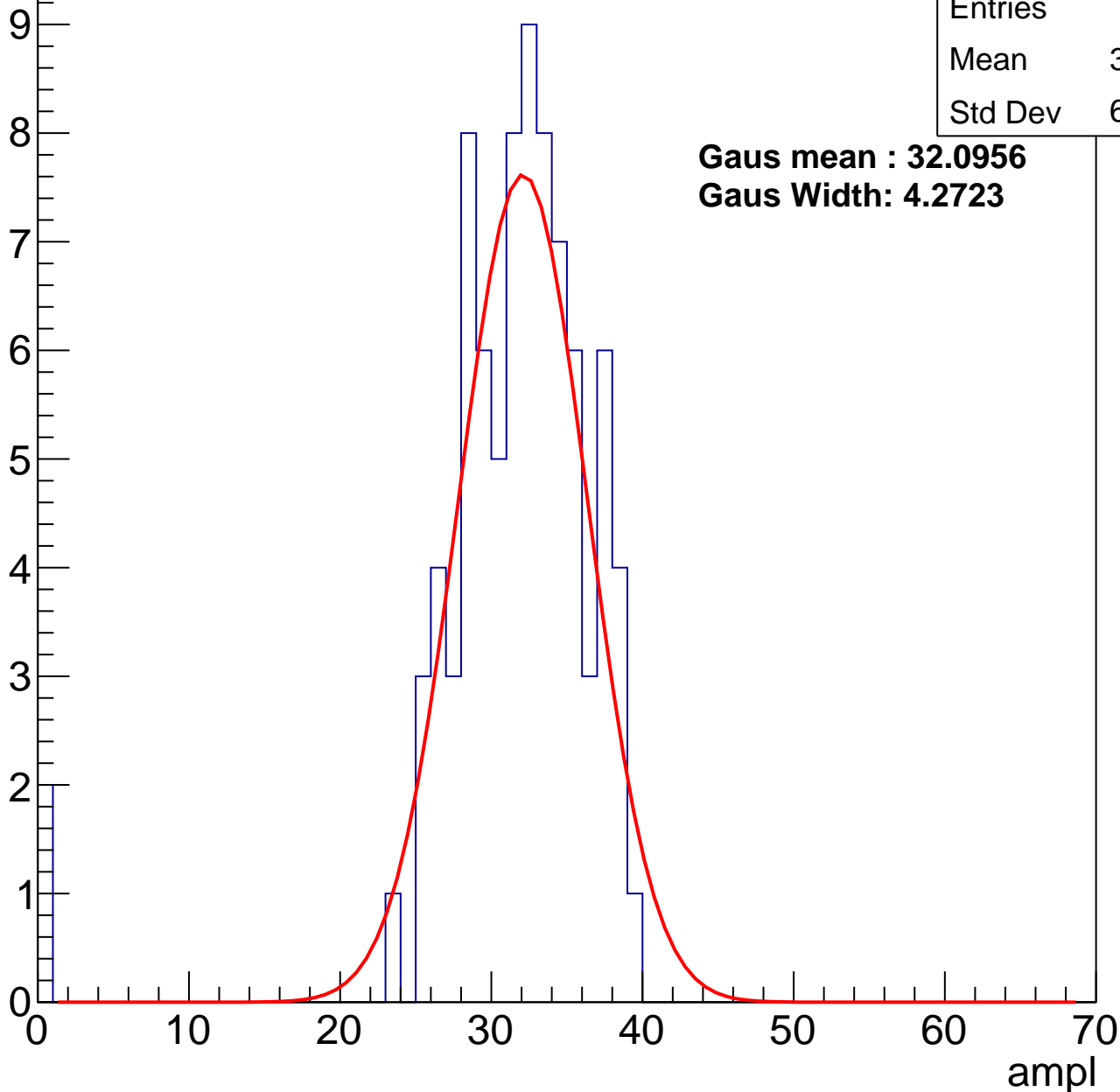
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	84
Mean	30.95
Std Dev	6.069

**Gaus mean : 32.0956**

**Gaus Width: 4.2723**



# B0L001S, U24-ch97, adc1

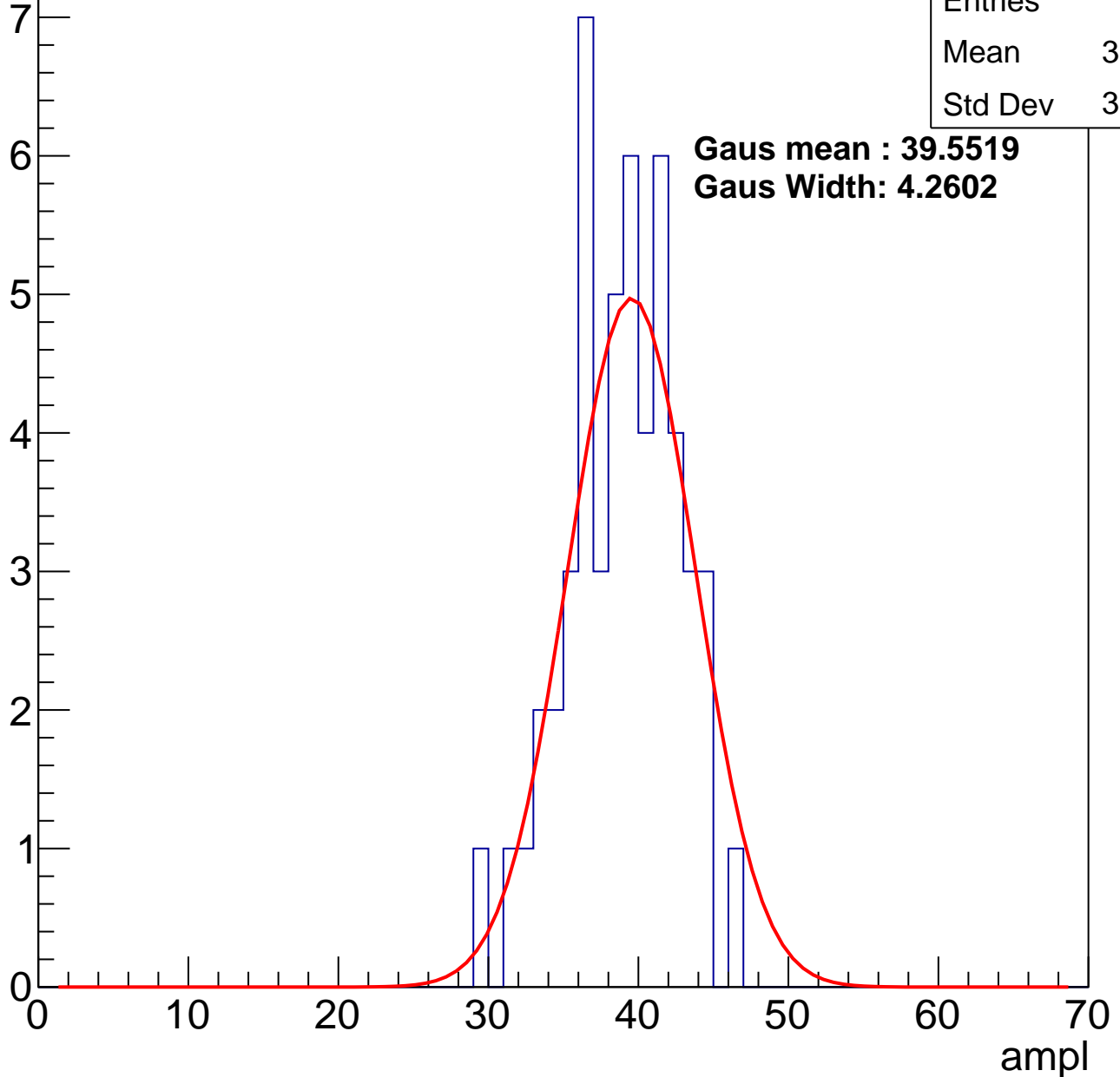
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	38.44
Std Dev	3.624

**Gaus mean : 39.5519**

**Gaus Width: 4.2602**



# B0L001S, U24-ch97, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	44.44
Std Dev	3.274

**Gaus mean : 45.1083**

**Gaus Width: 3.5954**

10

8

6

4

2

0

0

10

20

30

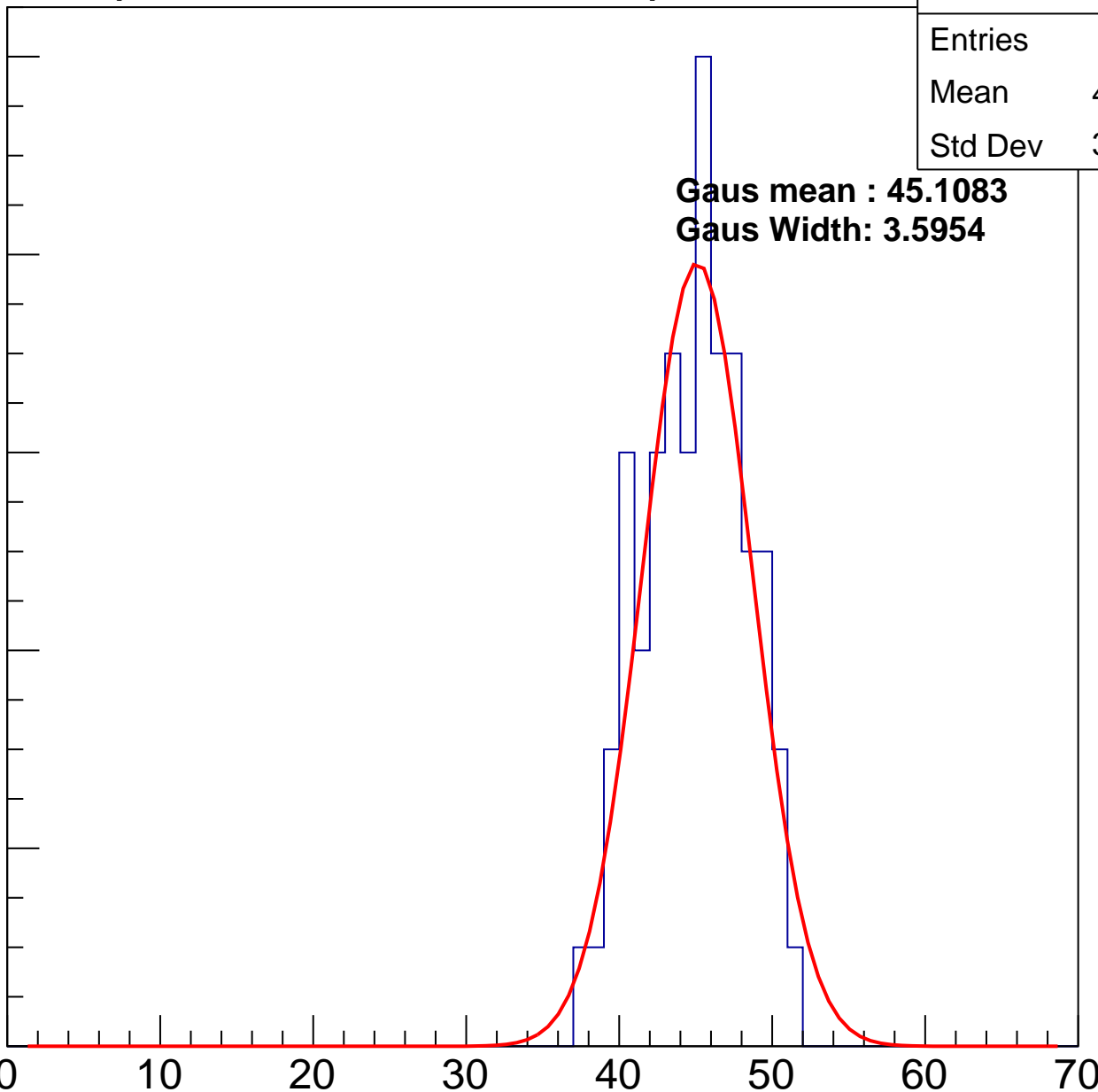
40

50

60

70

ampl

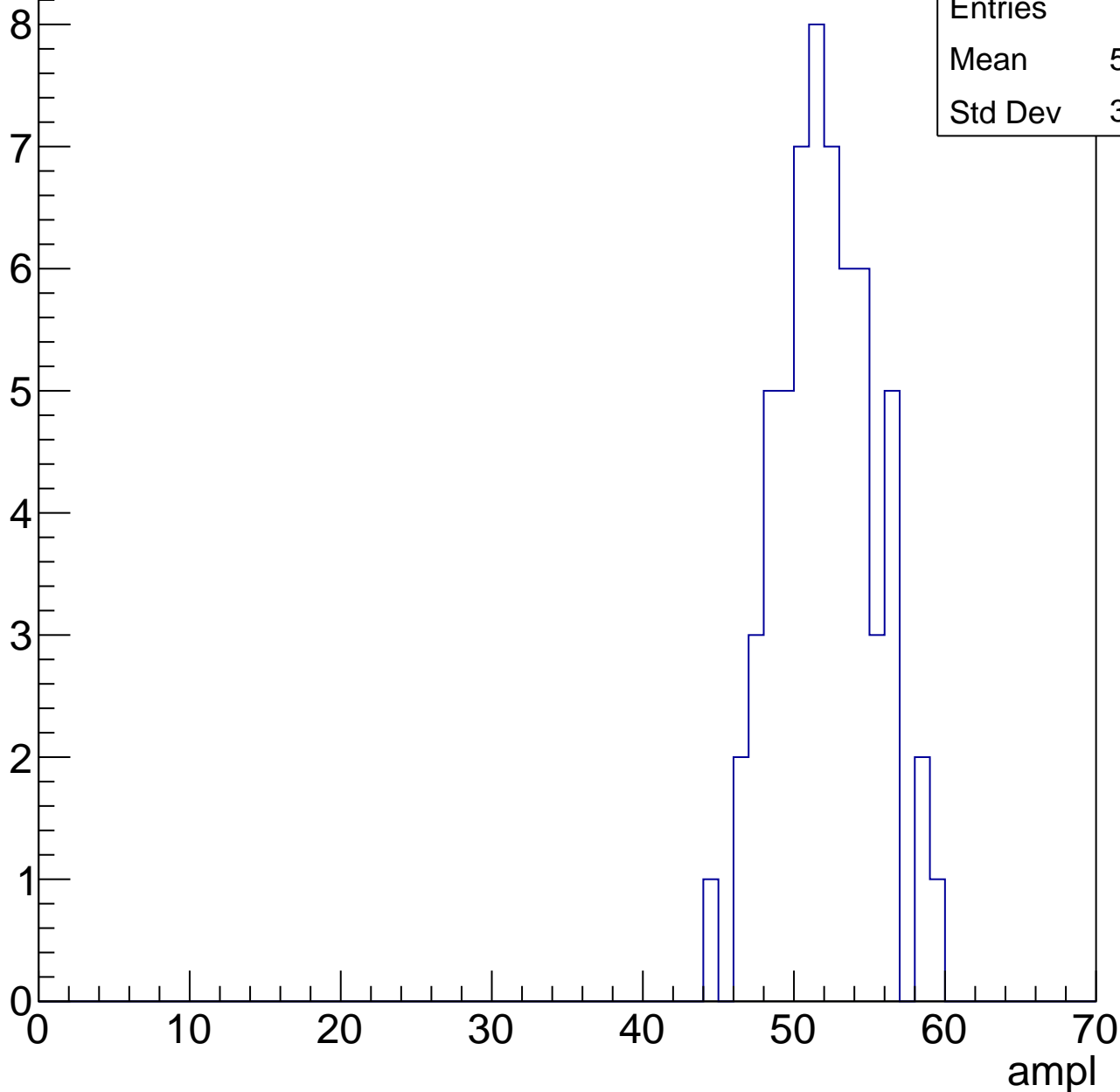


# B0L001S, U24-ch97, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	51.57
Std Dev	3.185

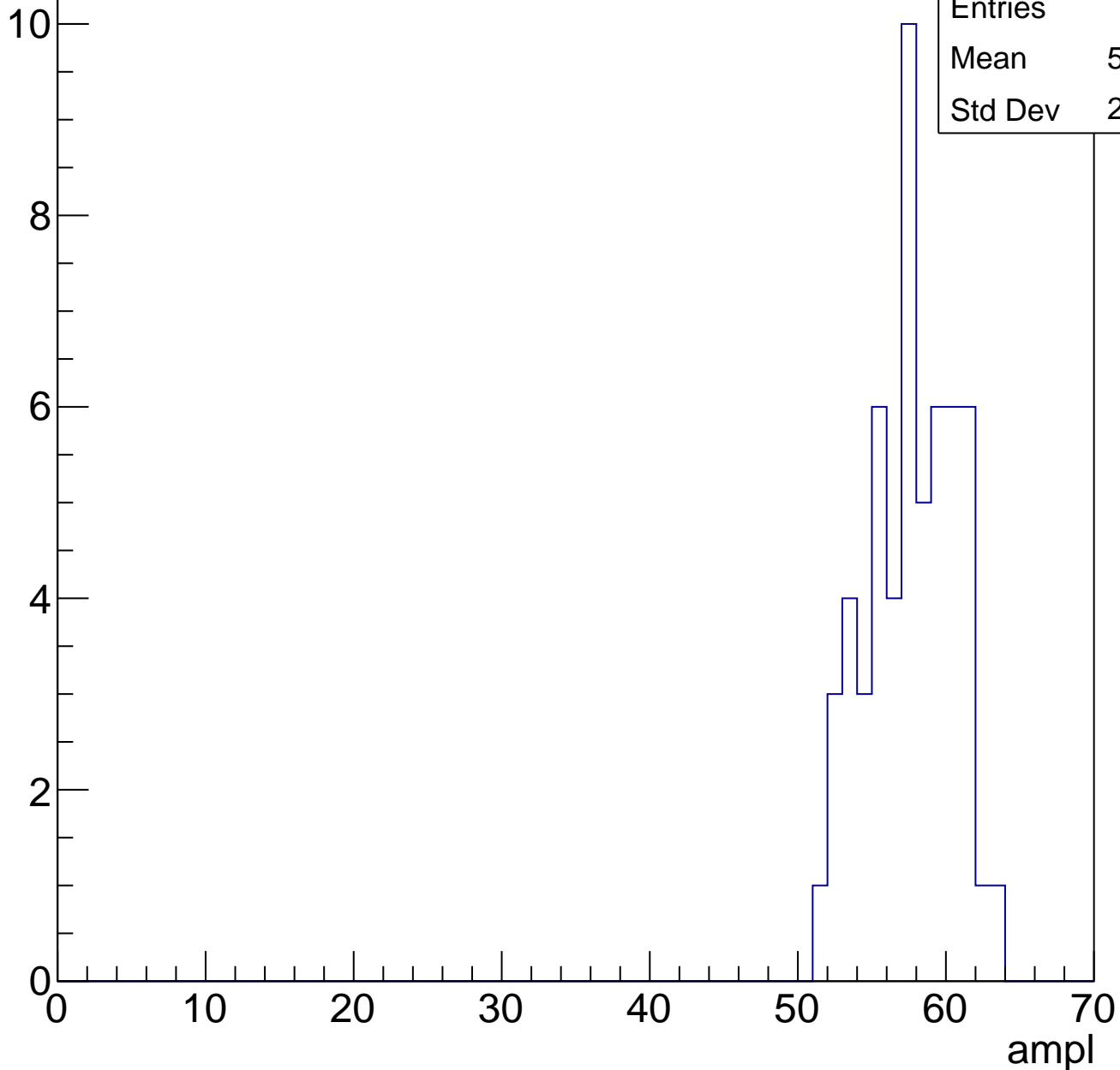


# B0L001S, U24-ch97, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	56
Mean	57.14
Std Dev	2.894

Entry

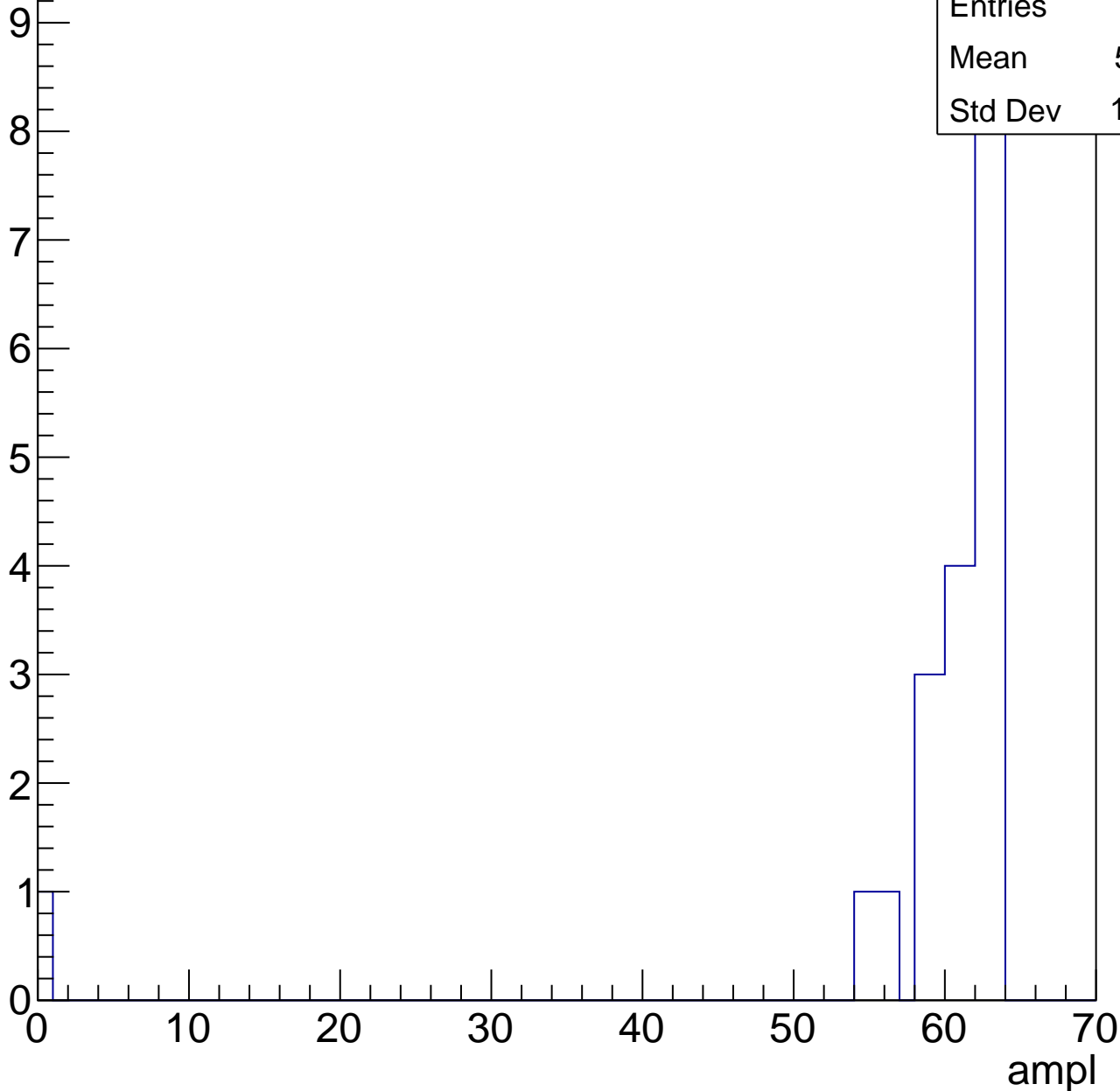


# B0L001S, U24-ch97, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	35
Mean	58.91
Std Dev	10.37



# B0L001S, U24-ch97, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch97, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U24-ch98, adc0

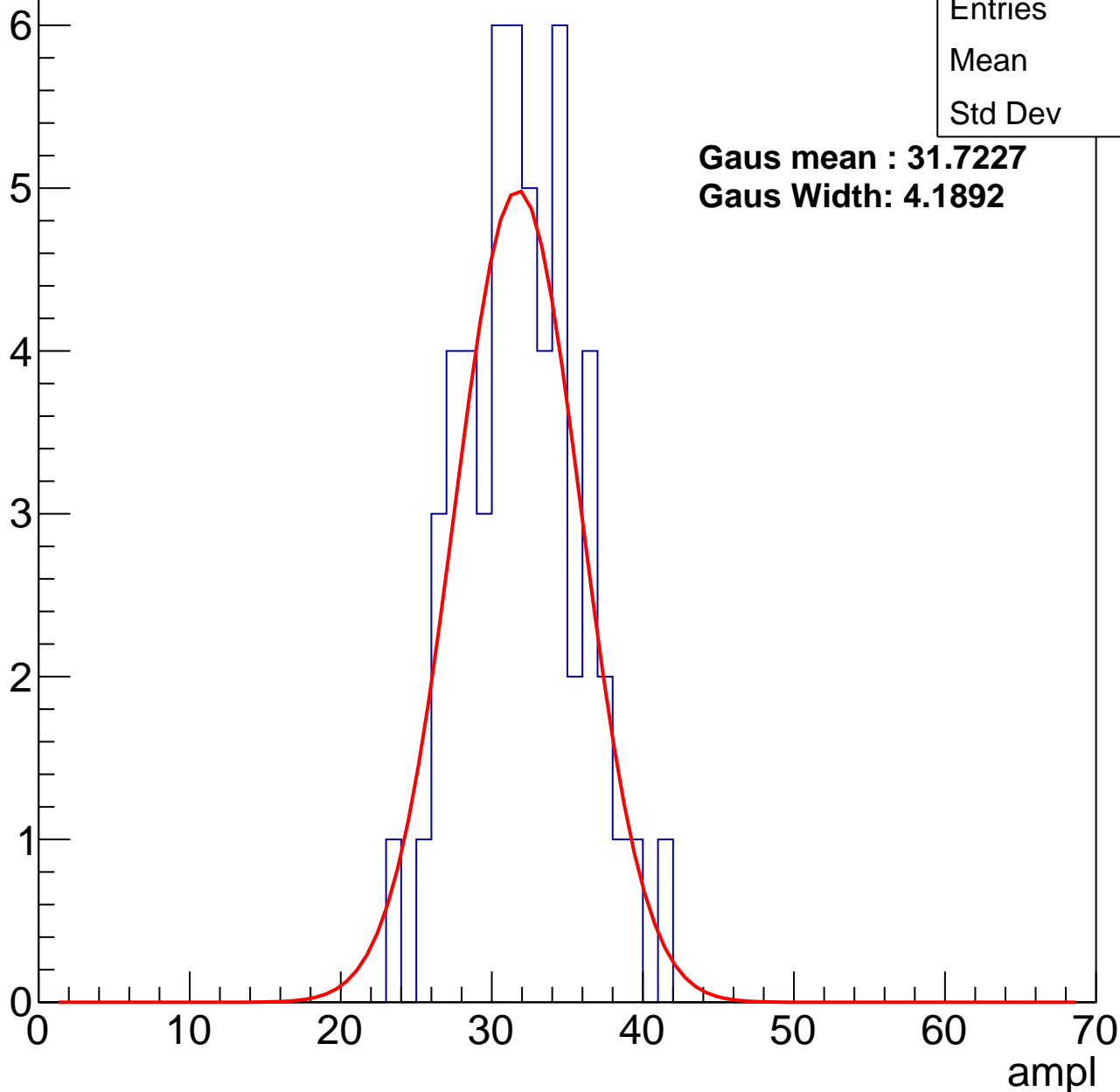
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	31.5
Std Dev	3.78

**Gaus mean : 31.7227**

**Gaus Width: 4.1892**



# B0L001S, U24-ch98, adc1

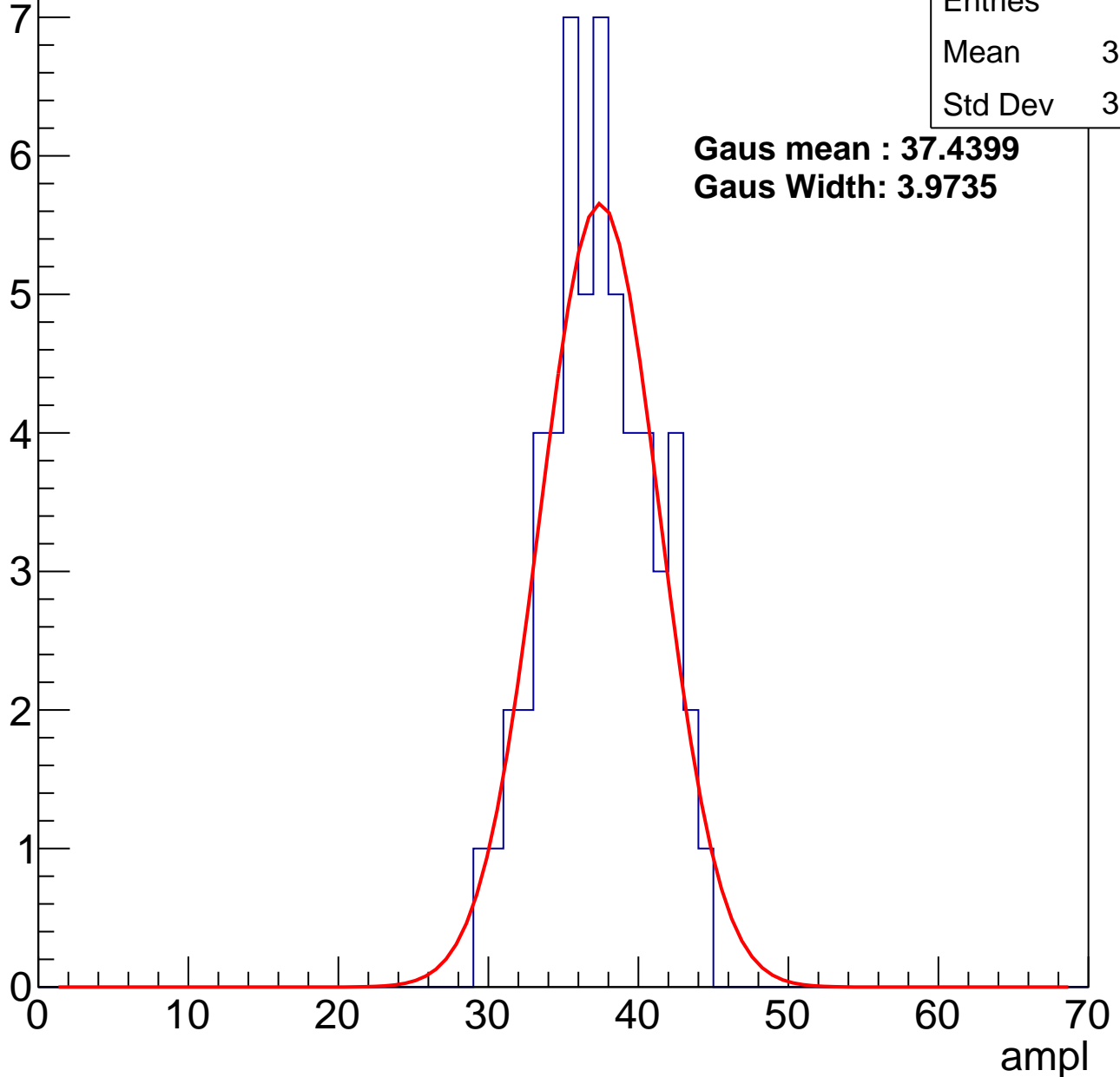
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	36.86
Std Dev	3.517

**Gaus mean : 37.4399**

**Gaus Width: 3.9735**



# B0L001S, U24-ch98, adc2

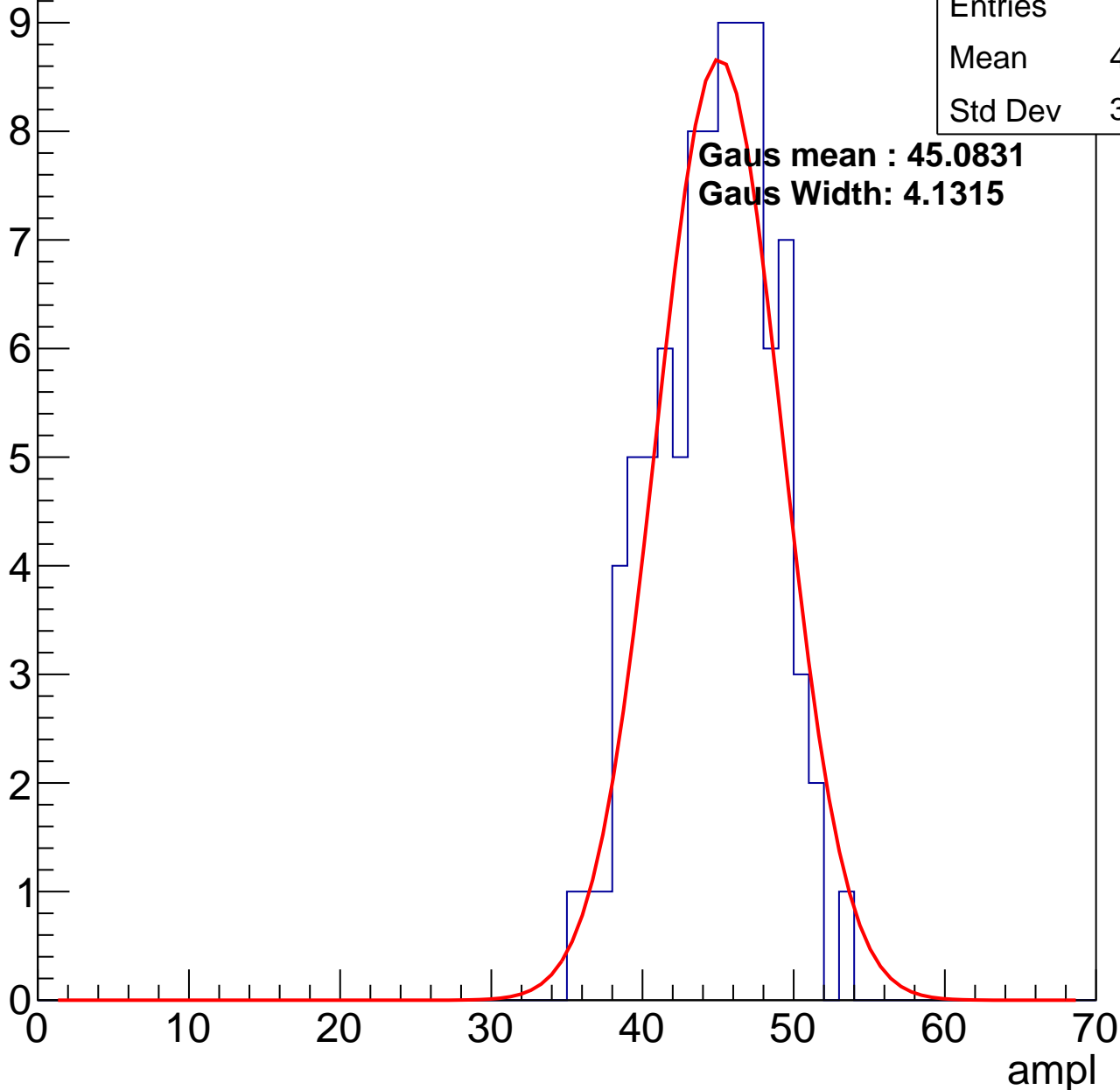
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	90
Mean	44.28
Std Dev	3.804

**Gaus mean : 45.0831**

**Gaus Width: 4.1315**

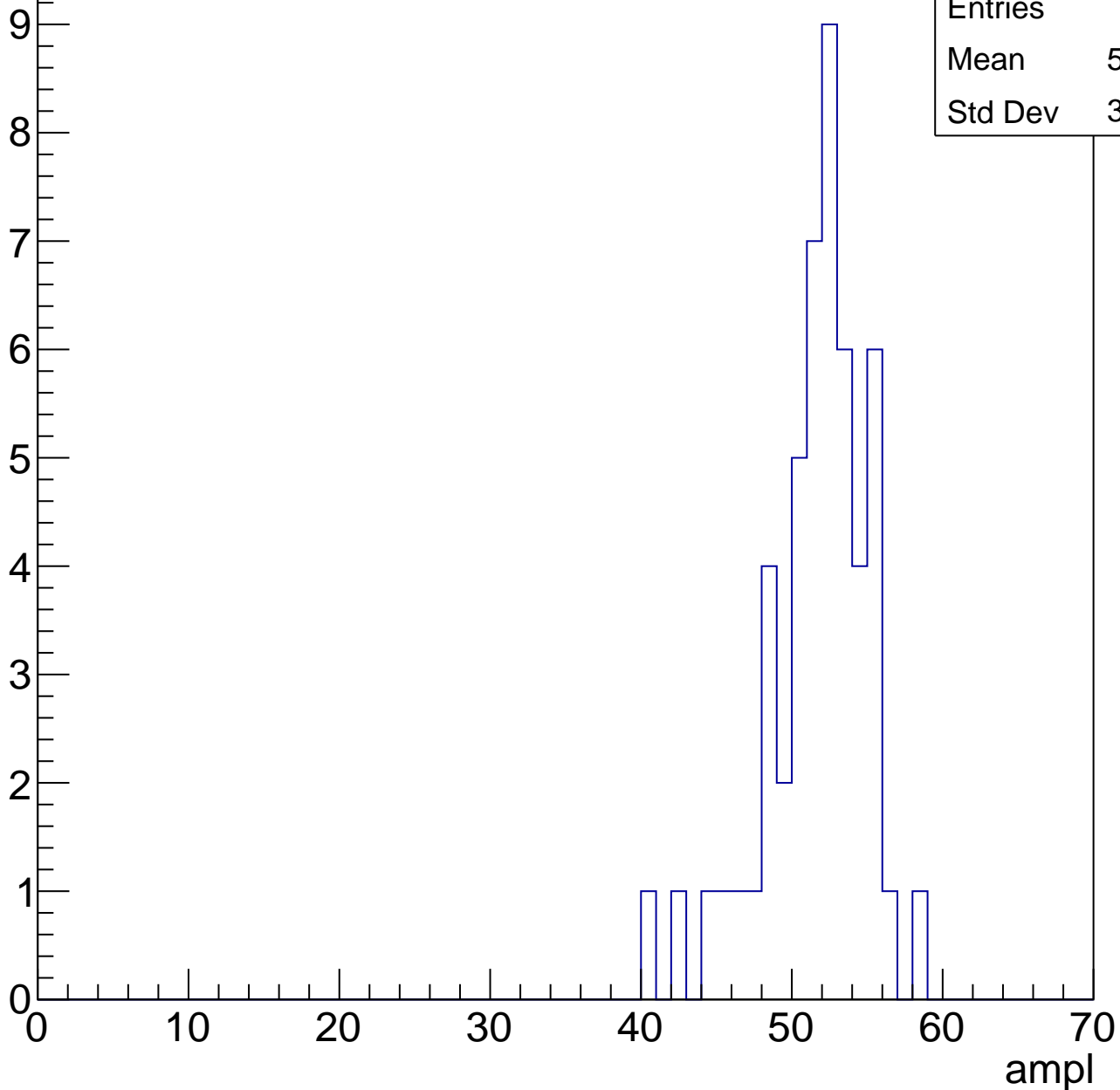


# B0L001S, U24-ch98, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	51
Mean	51.12
Std Dev	3.473

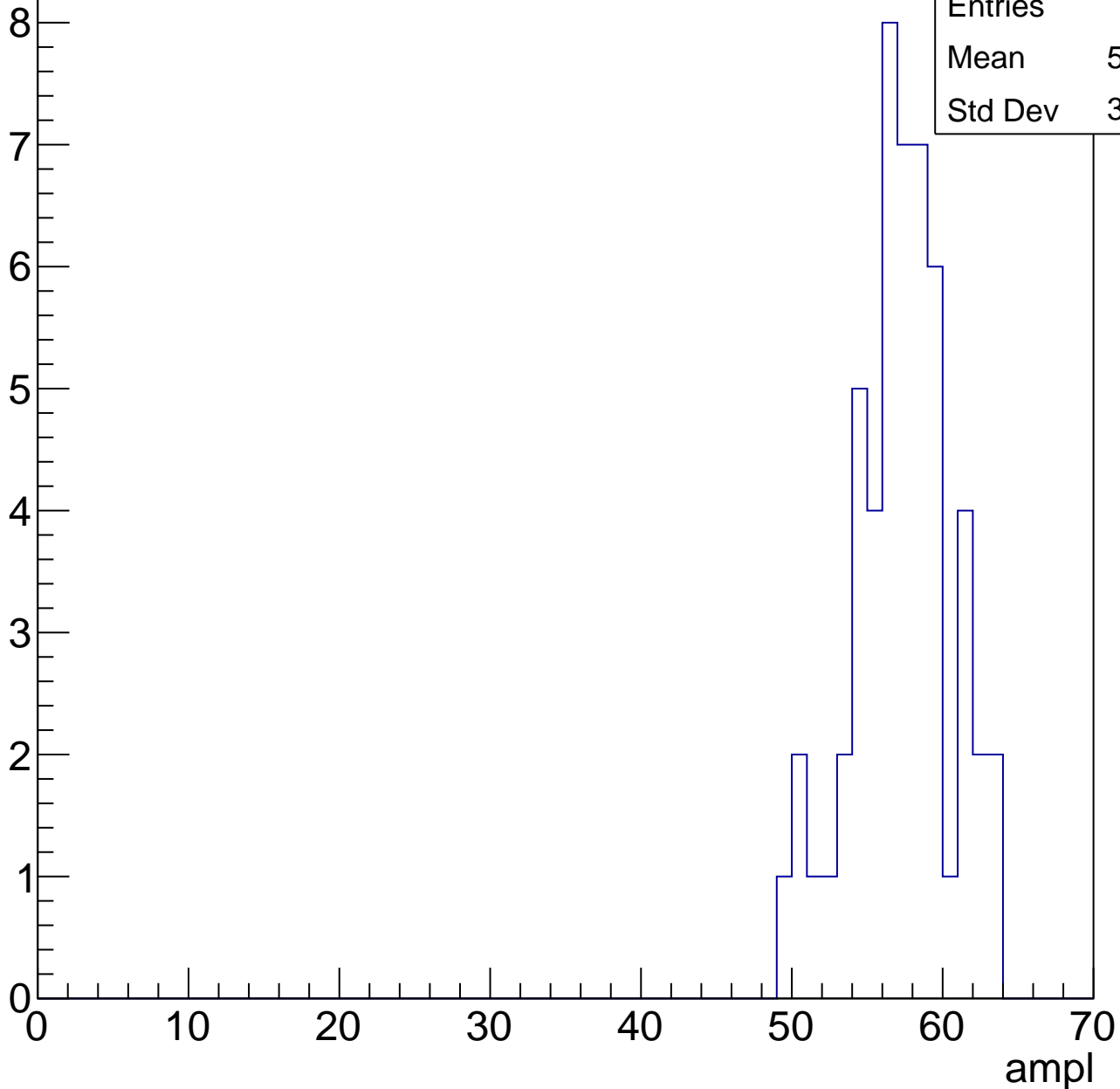


# B0L001S, U24-ch98, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

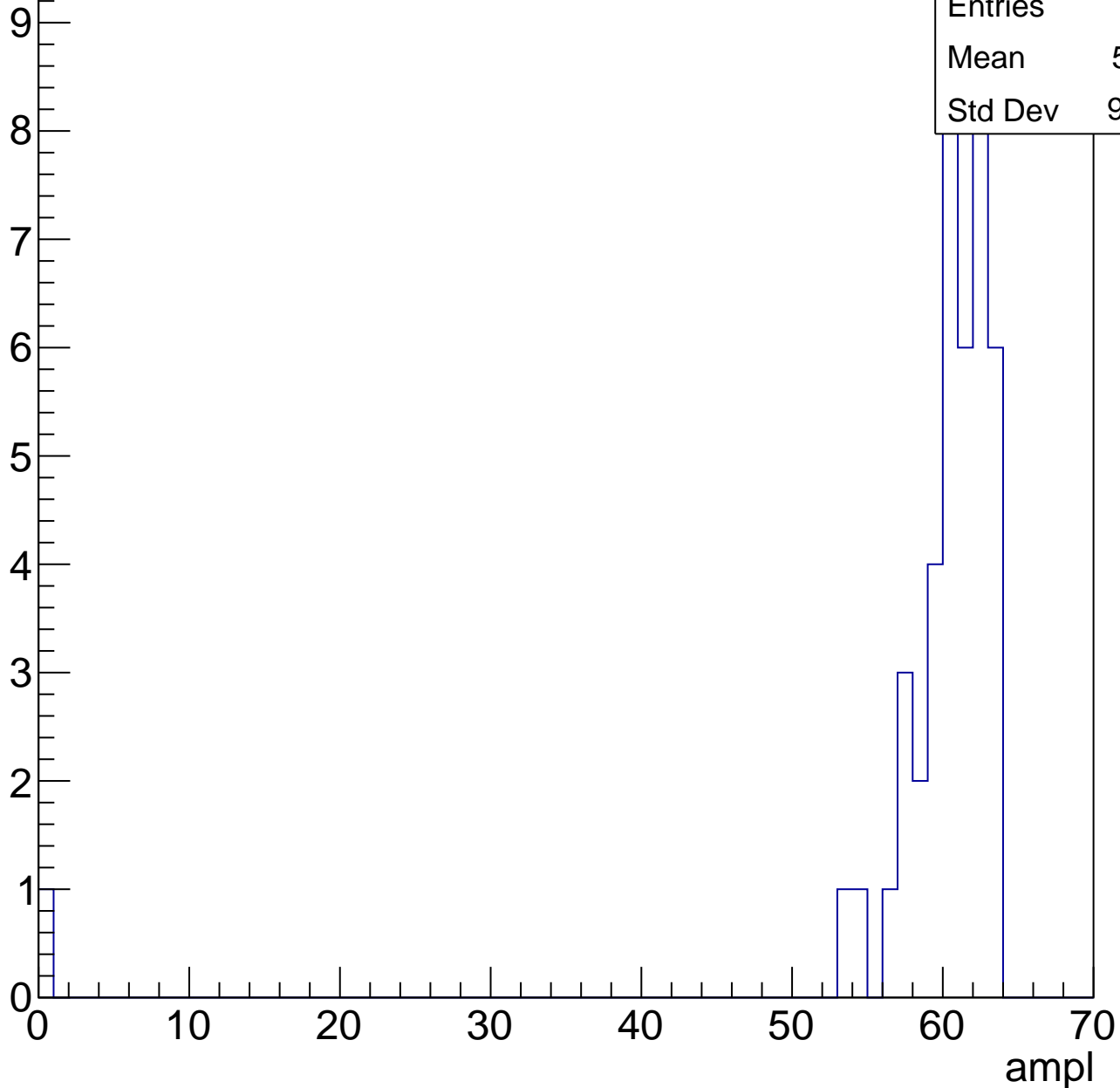
Entries	53
Mean	56.77
Std Dev	3.213



# B0L001S, U24-ch98, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U24-ch98, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch98, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L001S, U24-ch99, adc0

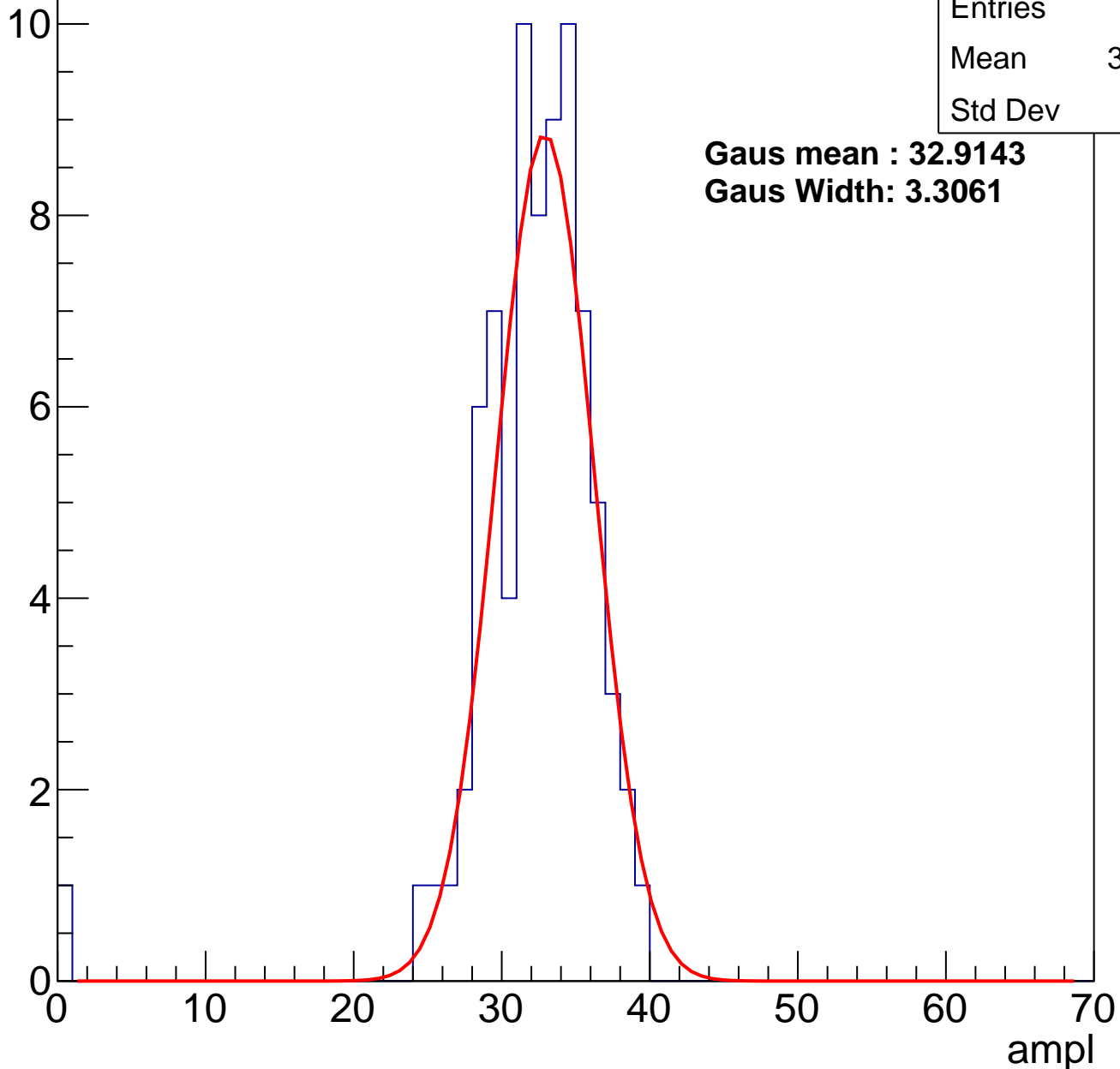
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	78
Mean	31.72
Std Dev	4.79

**Gaus mean : 32.9143**

**Gaus Width: 3.3061**

Entry



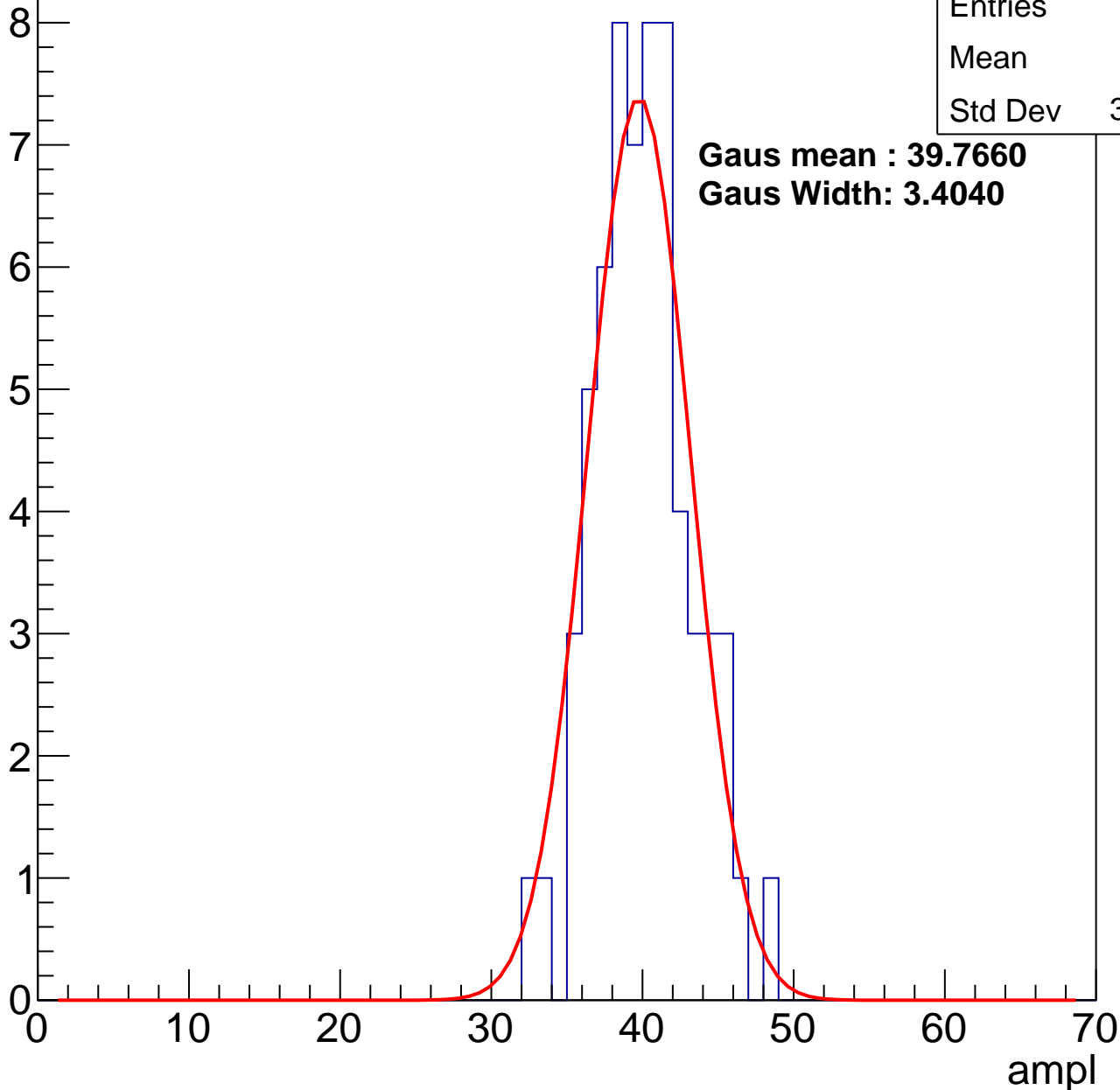
# B0L001S, U24-ch99, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	39.6
Std Dev	3.175

**Gaus mean : 39.7660**  
**Gaus Width: 3.4040**



# B0L001S, U24-ch99, adc2

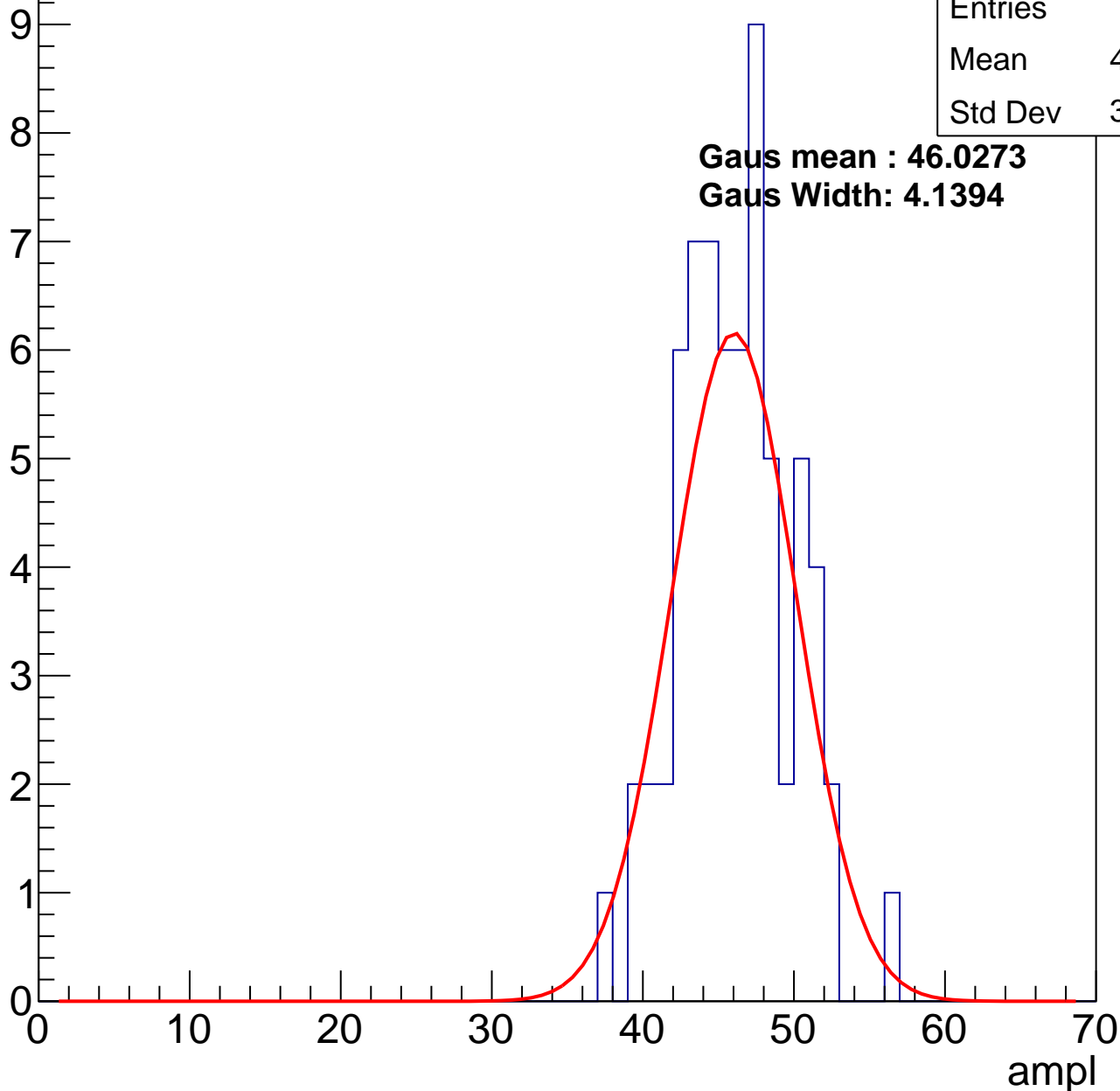
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	45.66
Std Dev	3.635

**Gaus mean : 46.0273**

**Gaus Width: 4.1394**

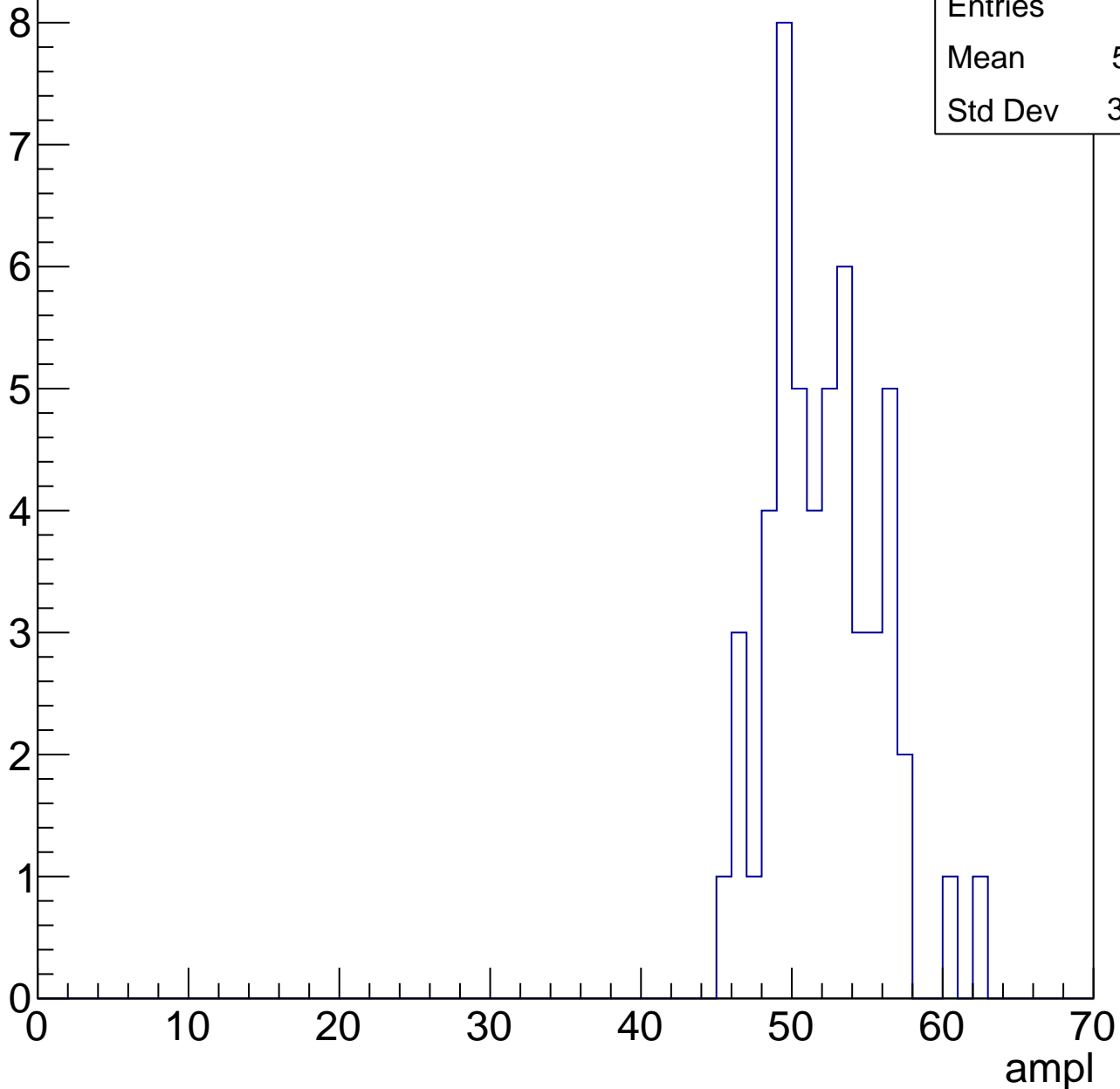


# B0L001S, U24-ch99, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	51.71
Std Dev	3.607

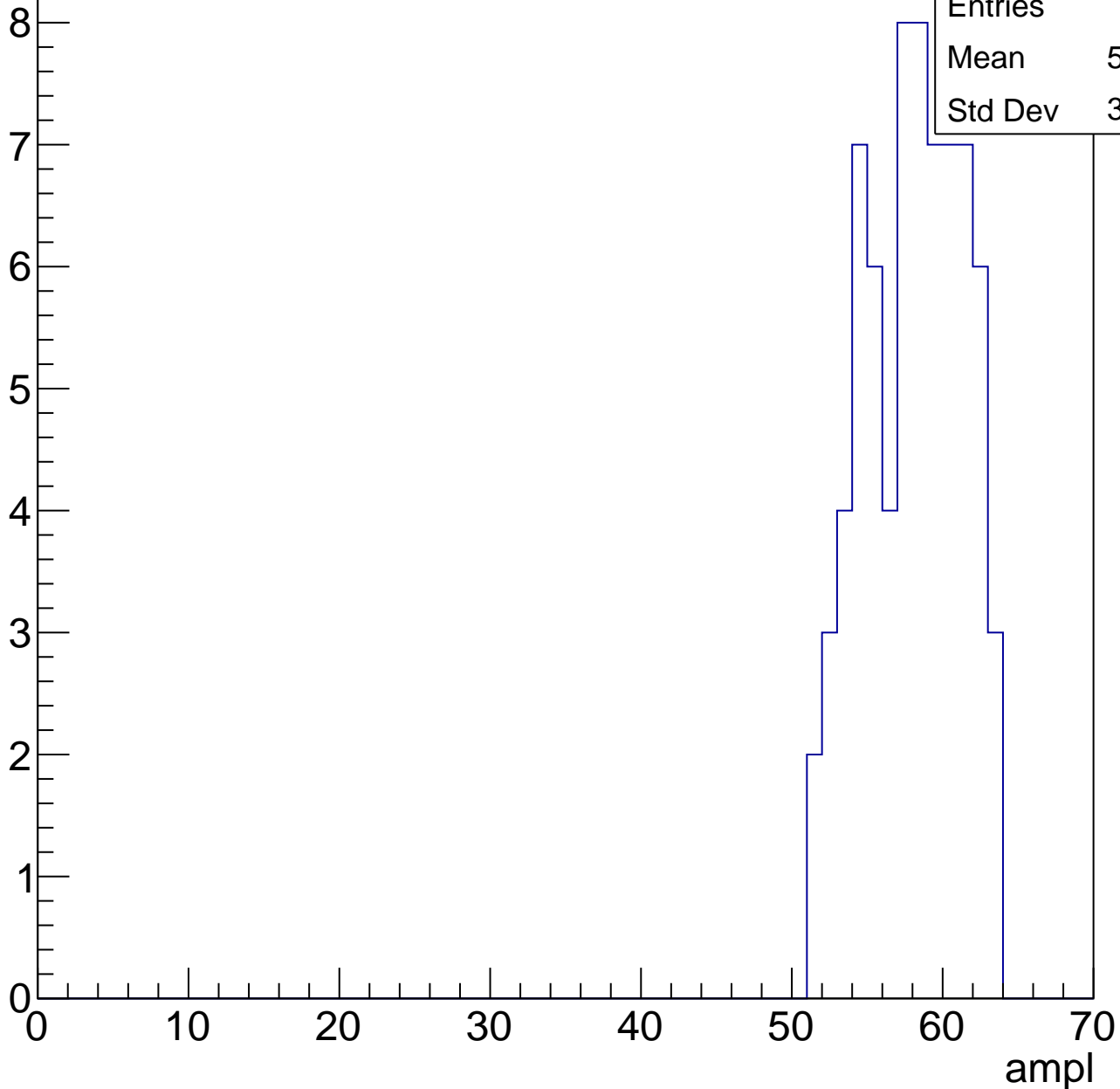


# B0L001S, U24-ch99, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	57.54
Std Dev	3.227

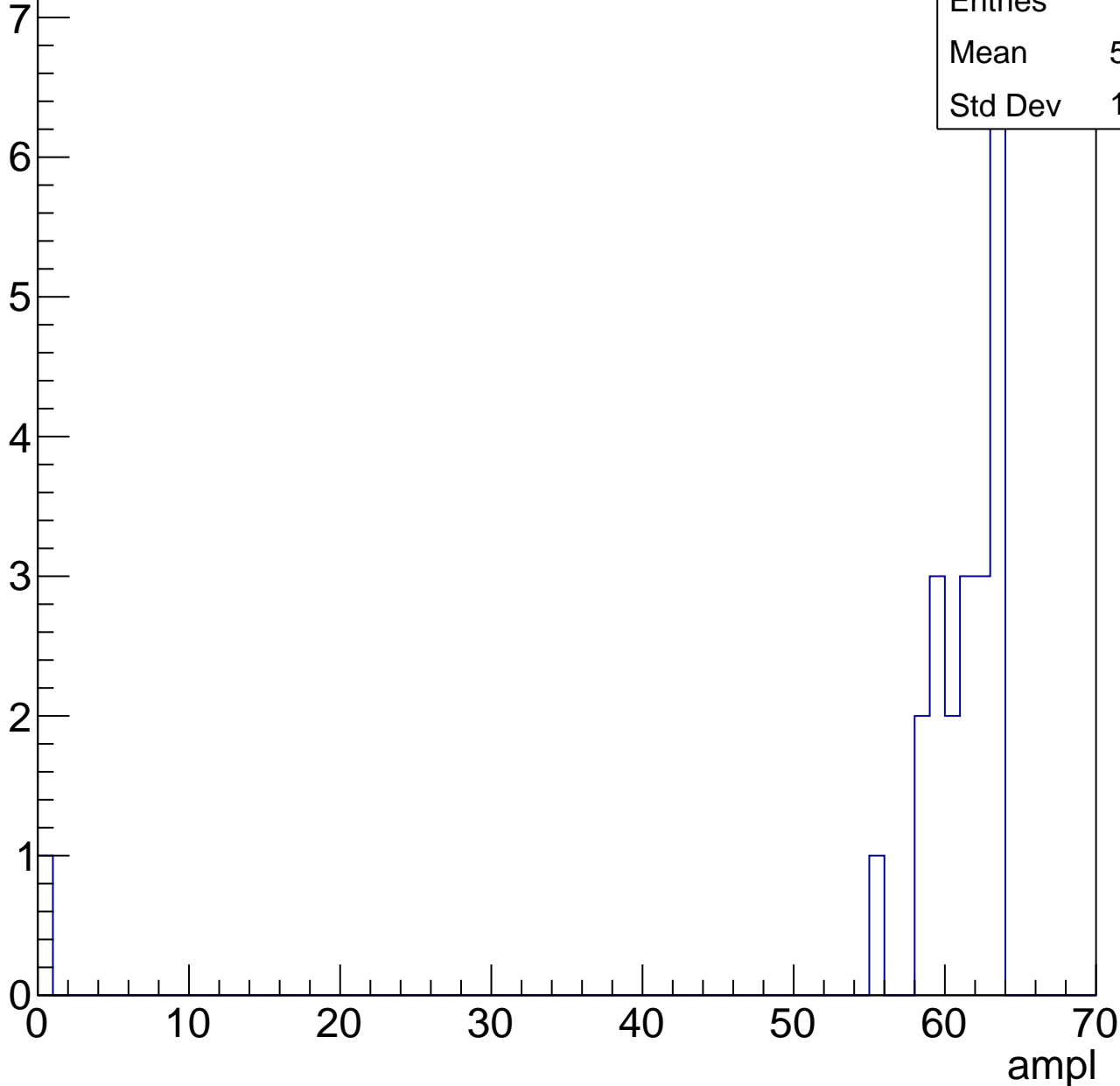


# B0L001S, U24-ch99, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	22
Mean	58.09
Std Dev	12.85



# B0L001S, U24-ch99, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U24-ch99, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U24-ch100, adc0

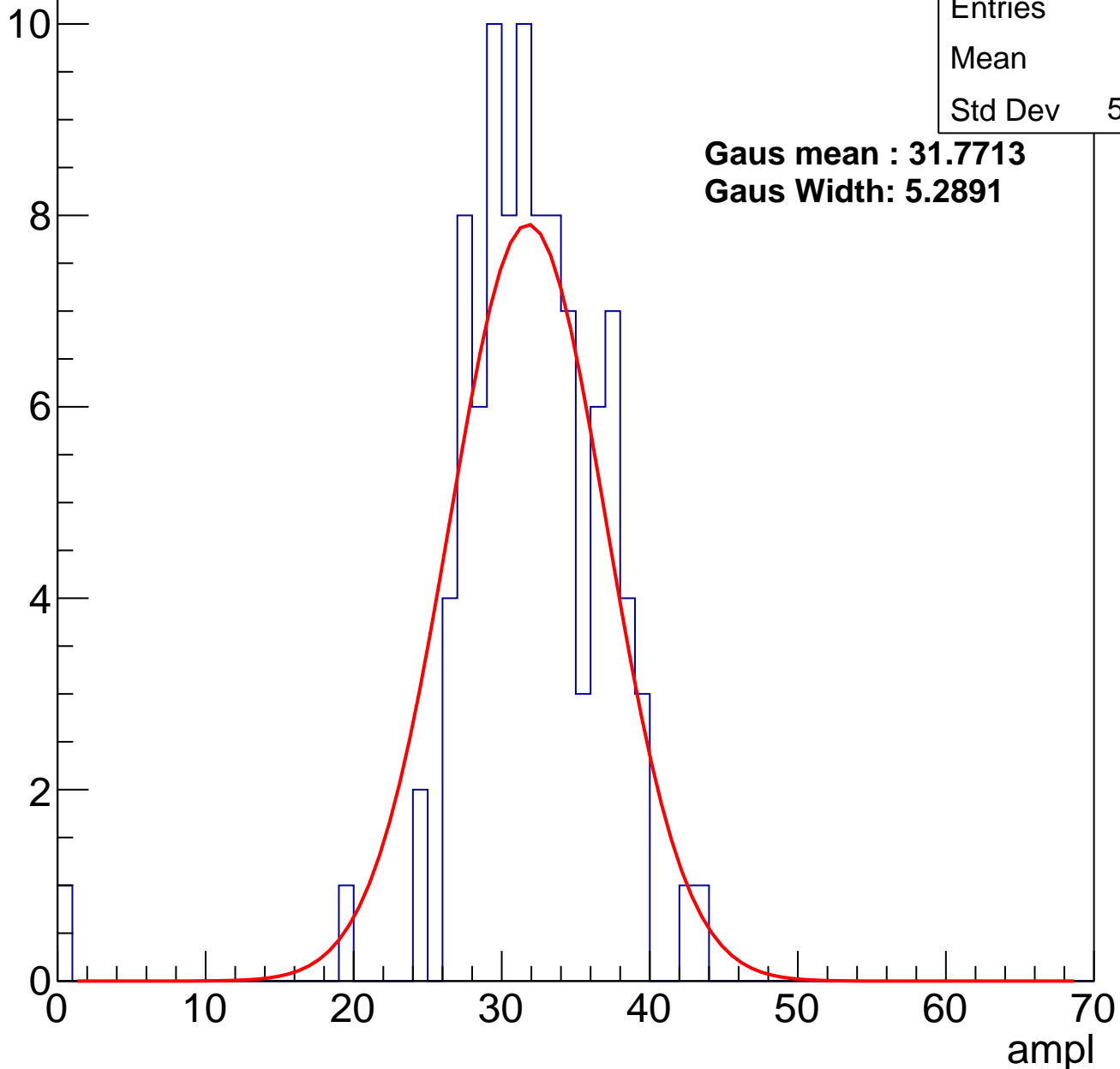
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	98
Mean	31.5
Std Dev	5.263

**Gaus mean : 31.7713**

**Gaus Width: 5.2891**

Entry



# B0L001S, U24-ch100, adc1

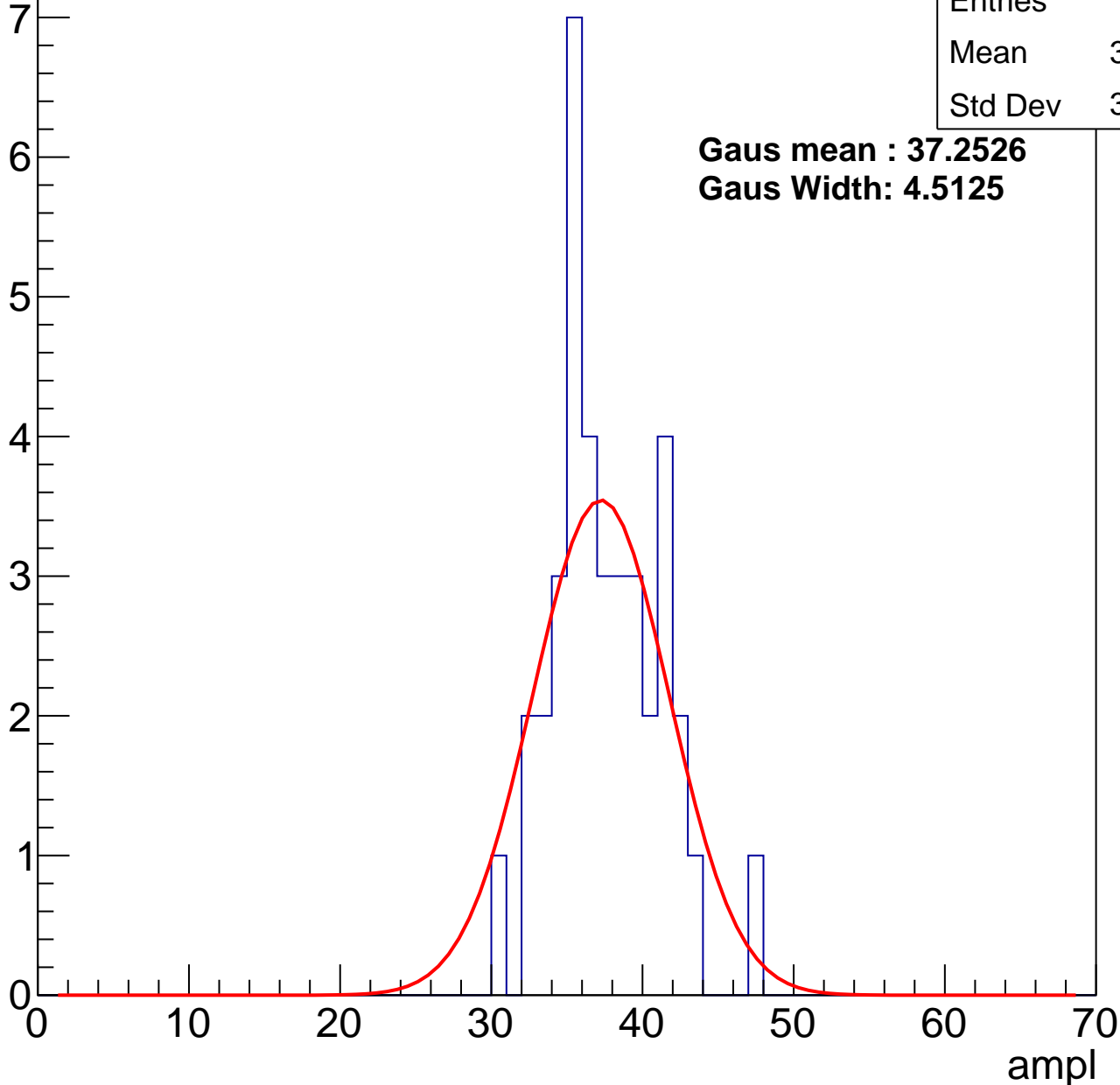
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	38
Mean	37.13
Std Dev	3.526

**Gaus mean : 37.2526**

**Gaus Width: 4.5125**



# B0L001S, U24-ch100, adc2

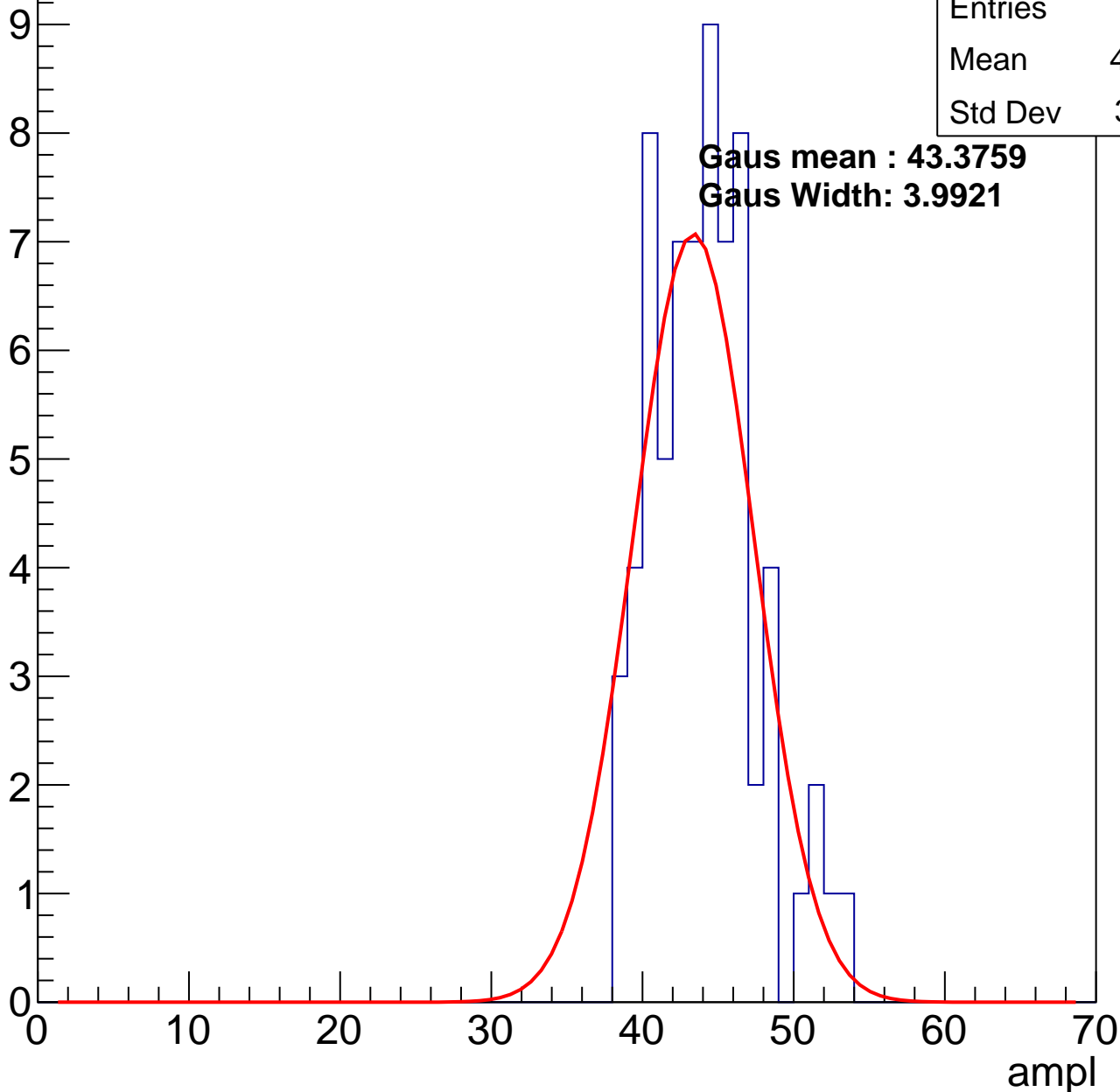
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	43.65
Std Dev	3.421

**Gaus mean : 43.3759**

**Gaus Width: 3.9921**



# B0L001S, U24-ch100, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

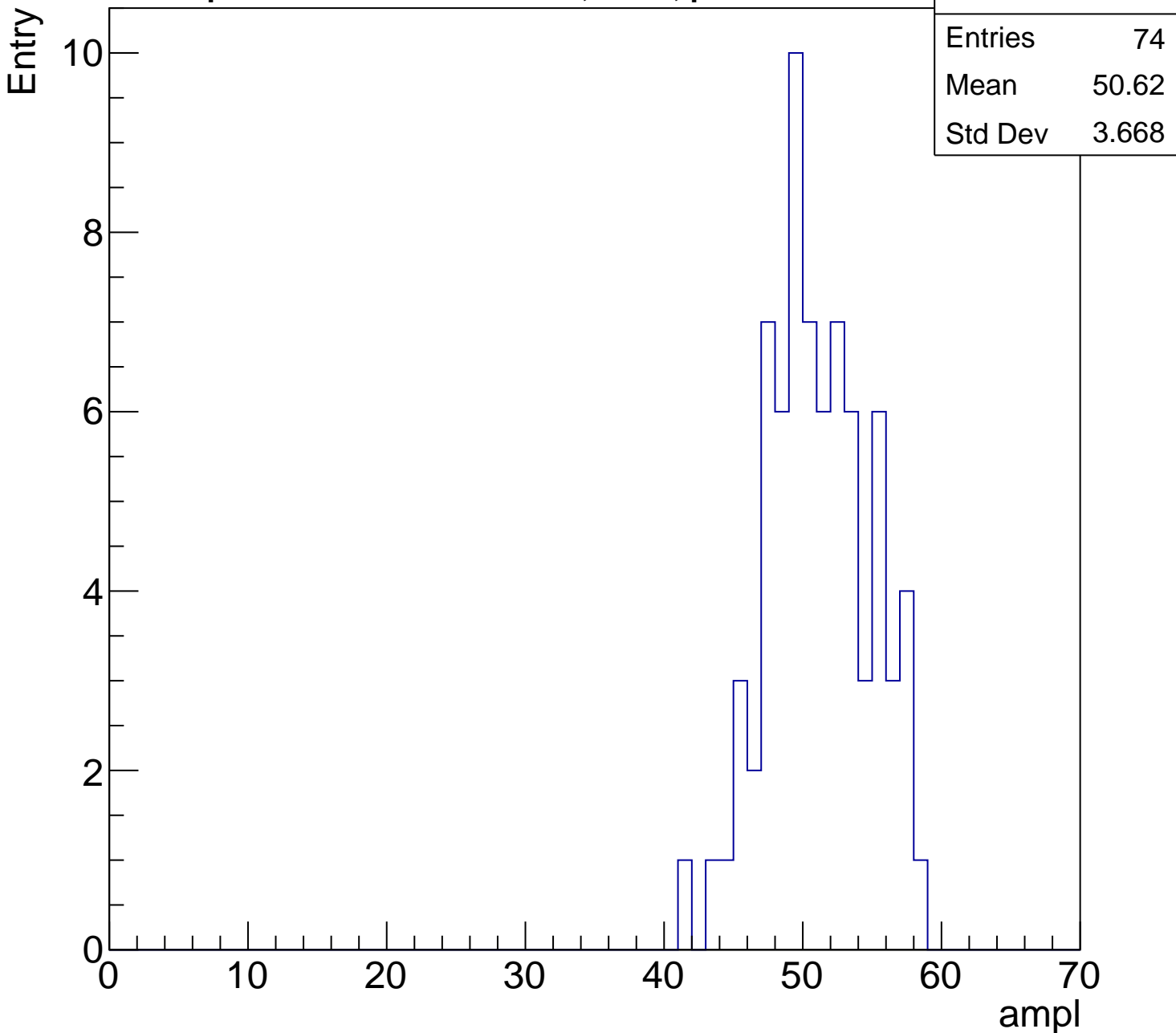
Entries	74
Mean	50.62
Std Dev	3.668

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

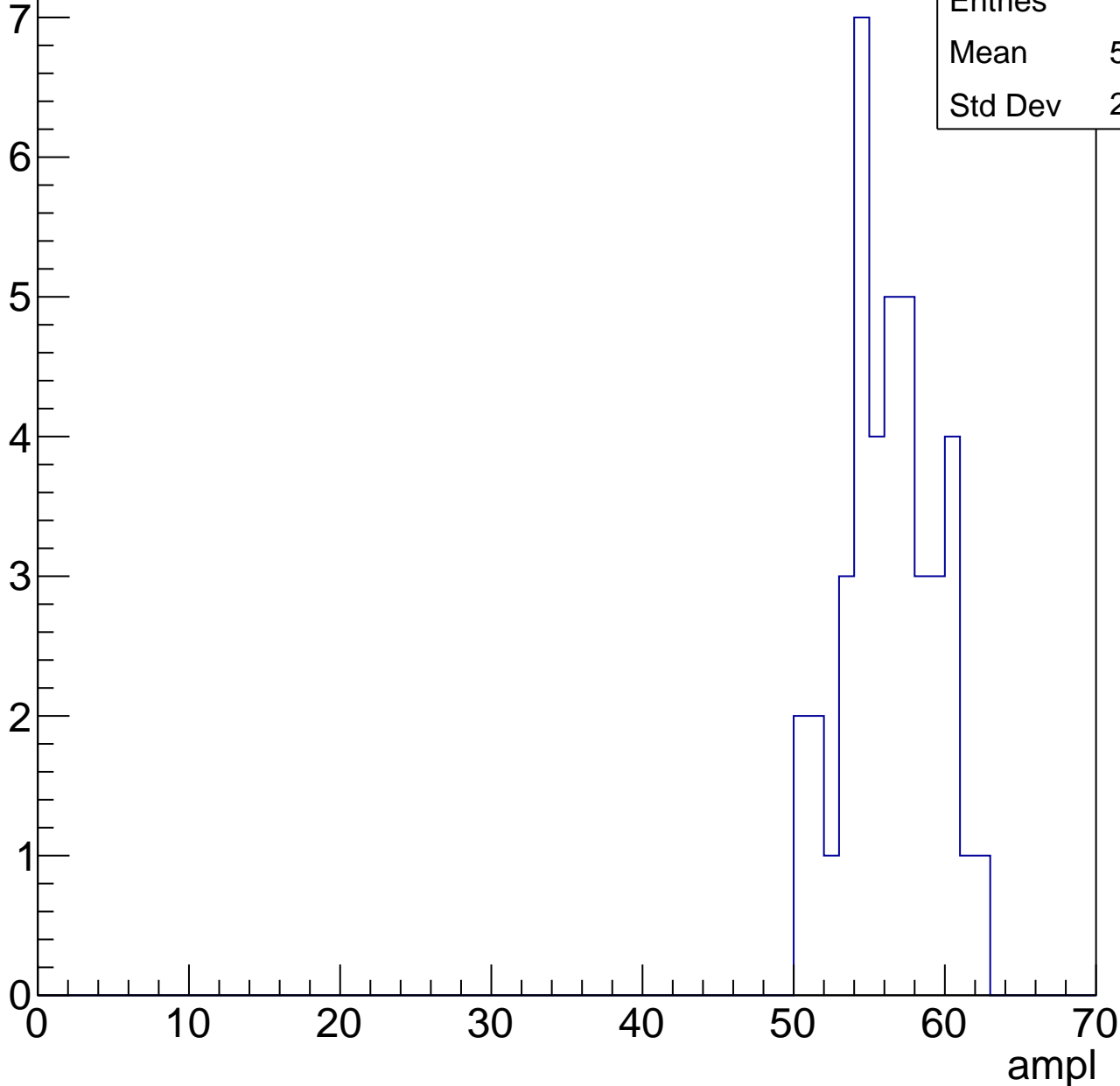


# B0L001S, U24-ch100, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	41
Mean	55.85
Std Dev	2.984

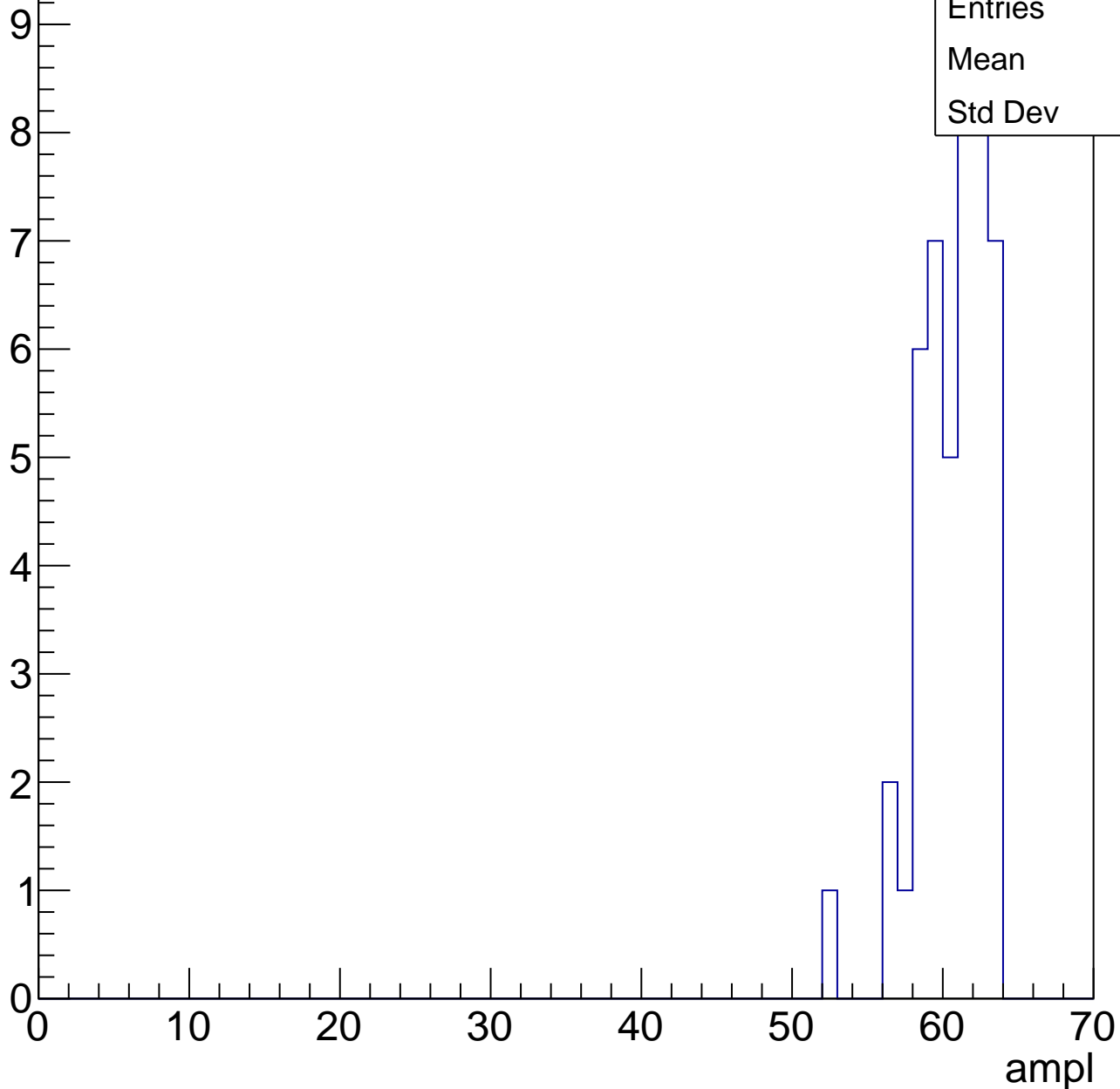


# B0L001S, U24-ch100, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

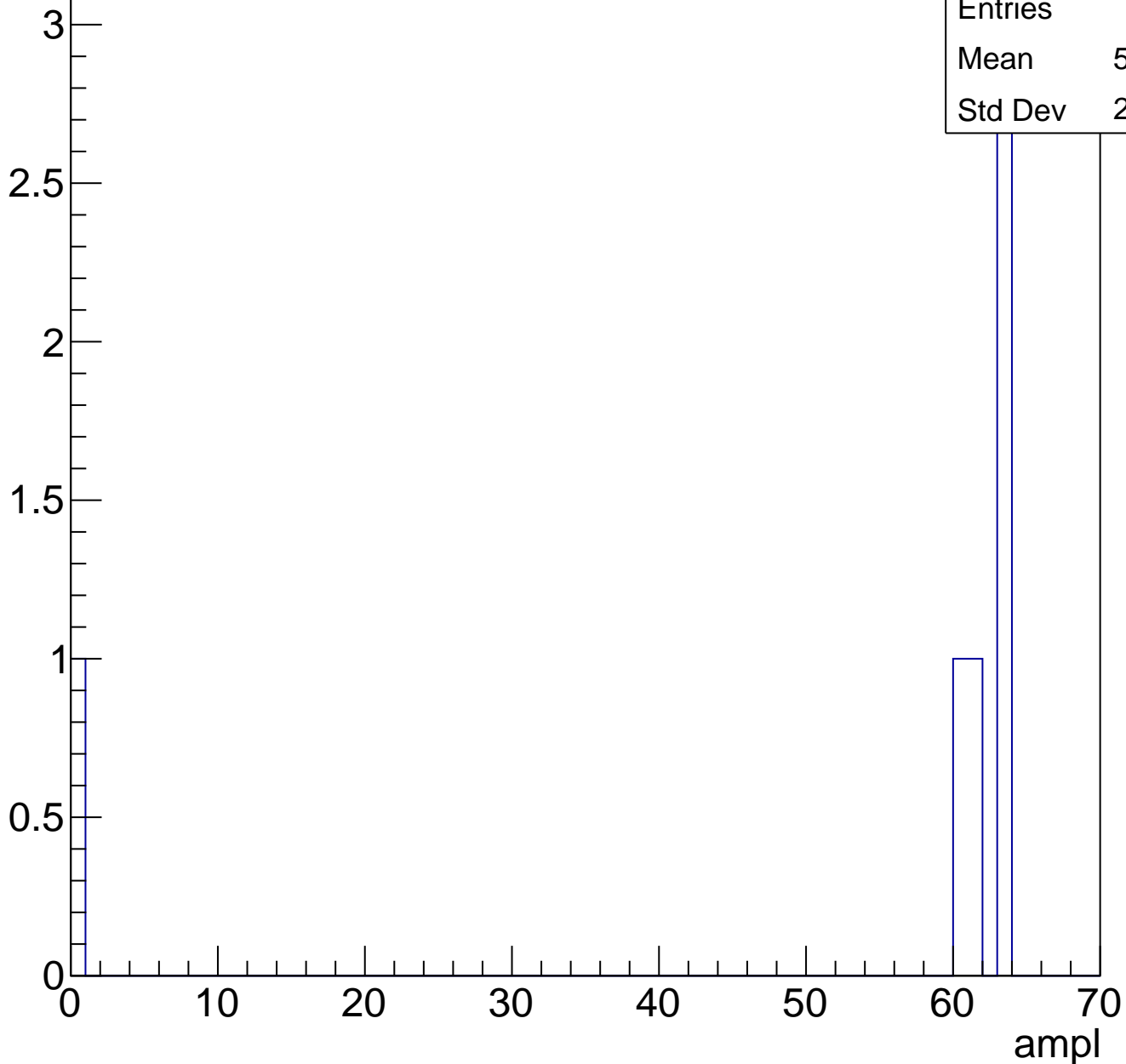
Entries	46
Mean	60.2
Std Dev	2.29



# B0L001S, U24-ch100, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch100, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L001S, U24-ch101, adc0

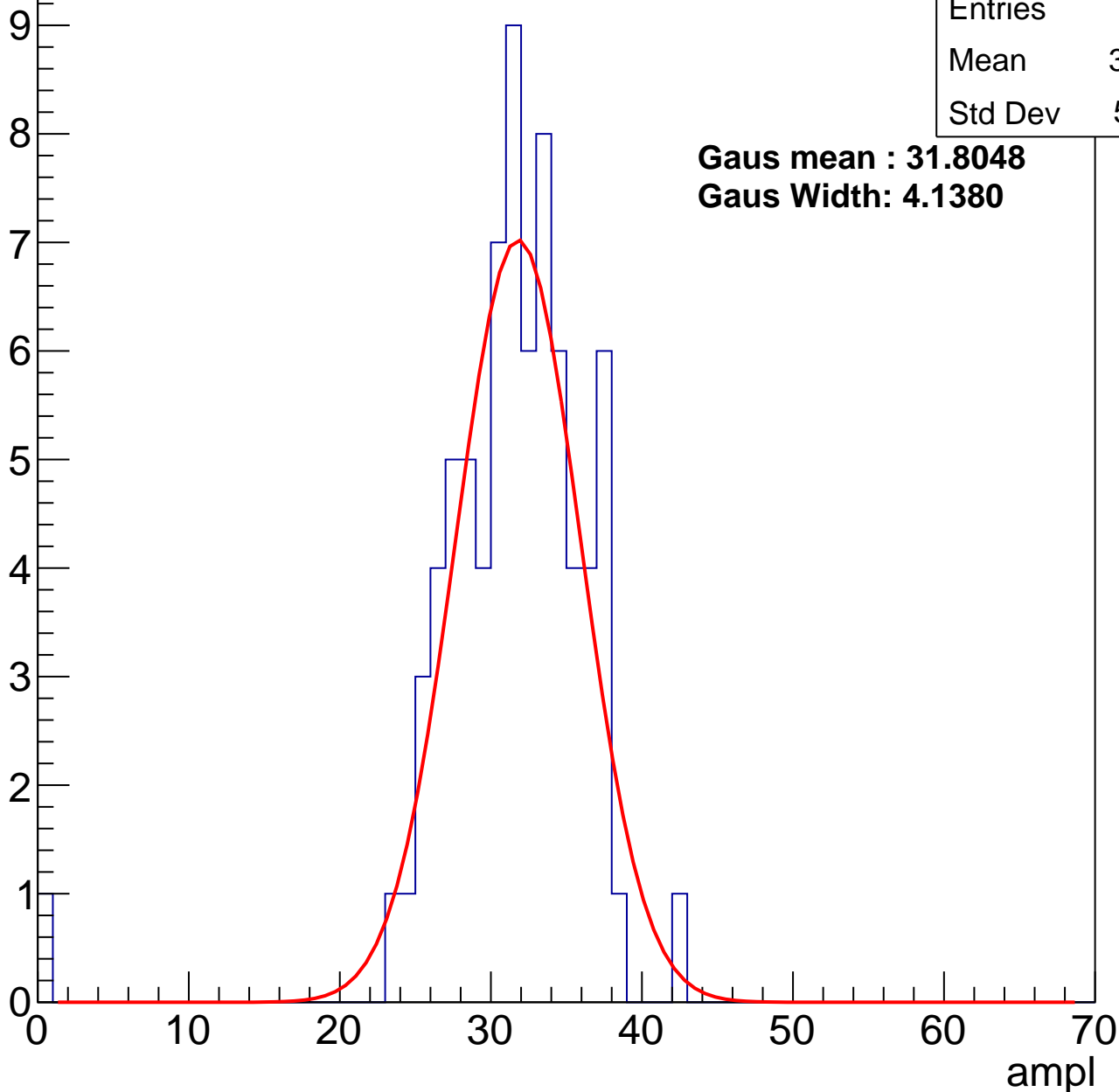
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	76
Mean	30.95
Std Dev	5.221

**Gaus mean : 31.8048**

**Gaus Width: 4.1380**



# B0L001S, U24-ch101, adc1

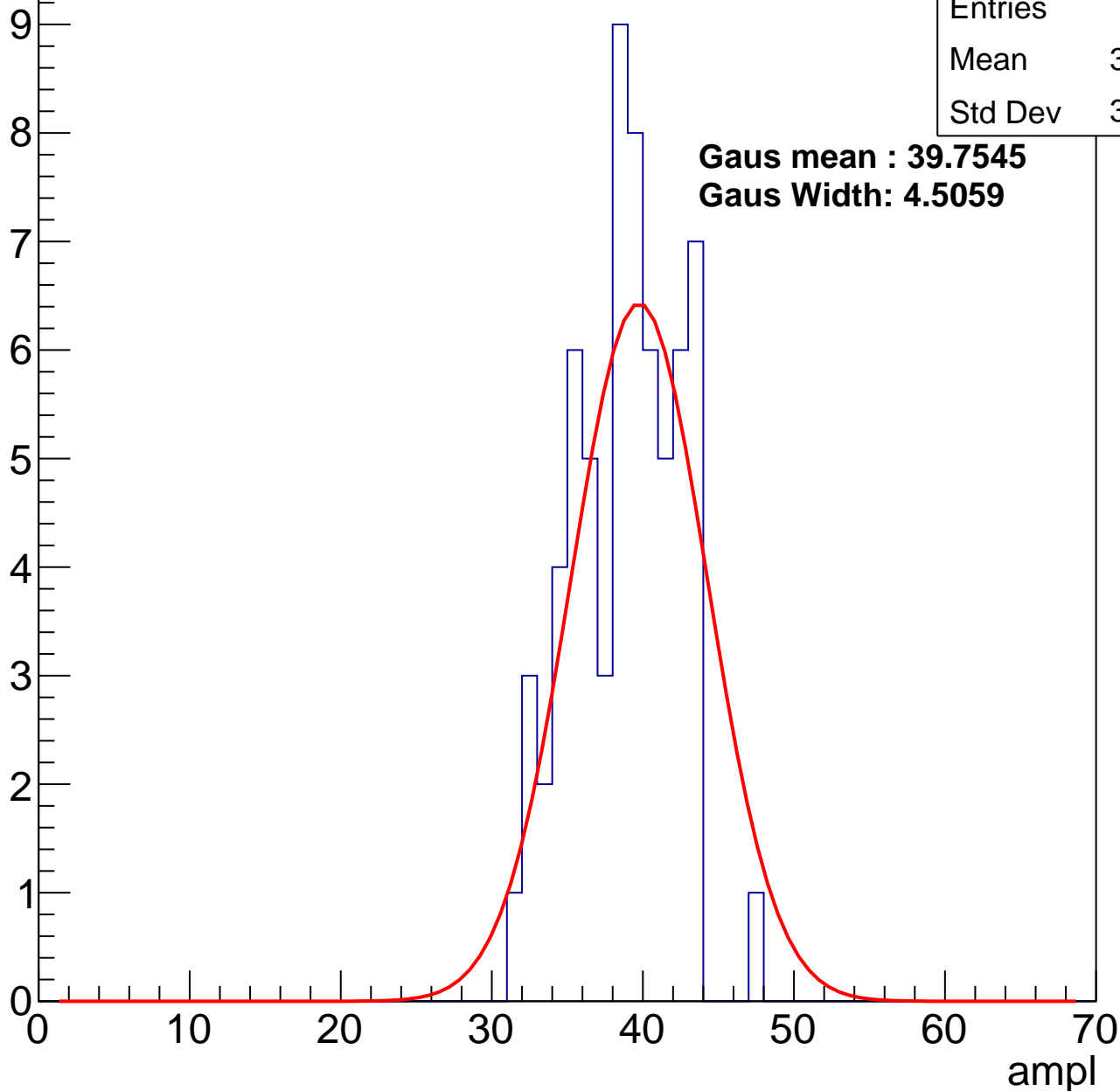
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	38.32
Std Dev	3.416

**Gaus mean : 39.7545**

**Gaus Width: 4.5059**



# B0L001S, U24-ch101, adc2

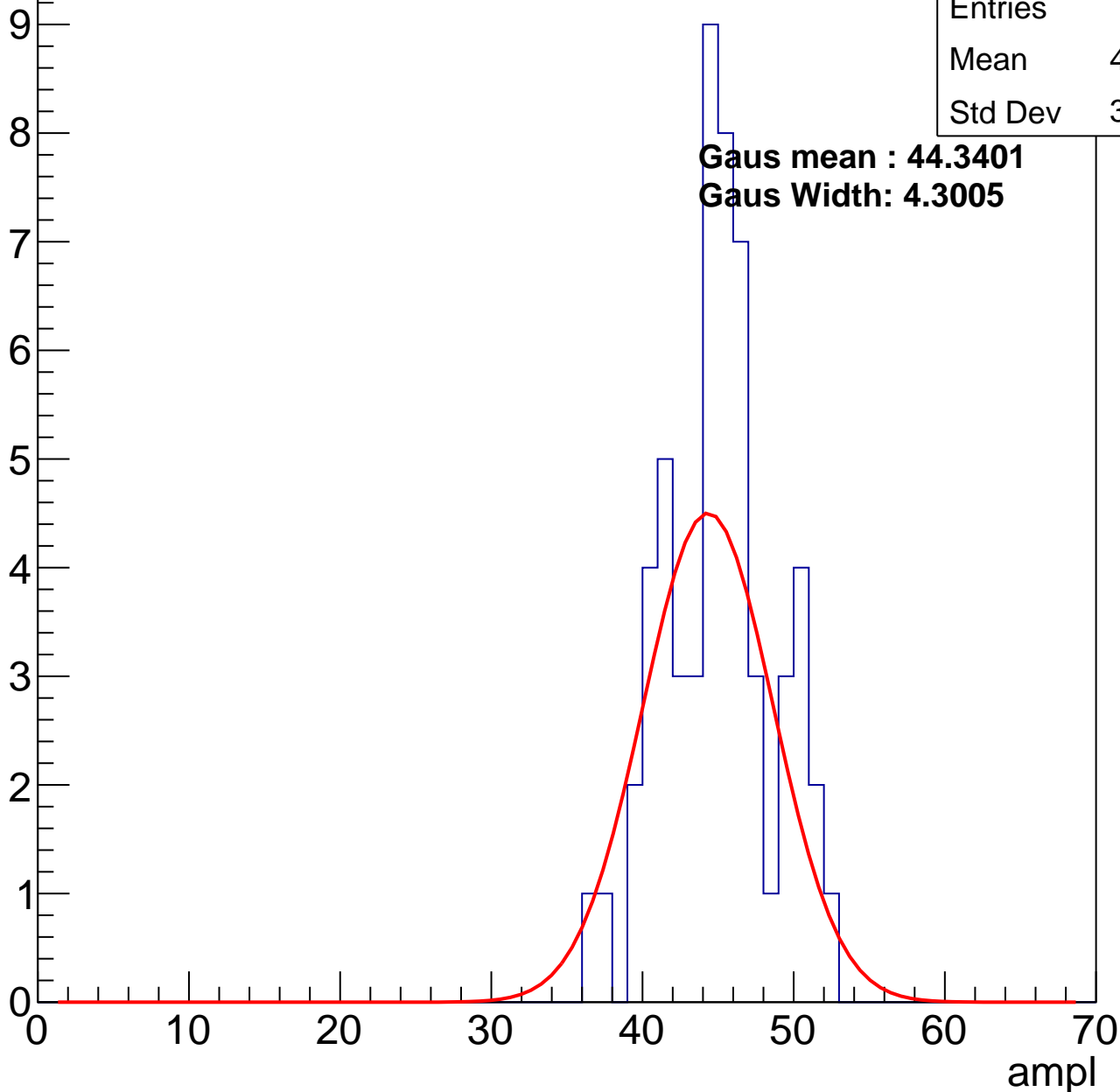
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	44.54
Std Dev	3.579

**Gaus mean : 44.3401**

**Gaus Width: 4.3005**

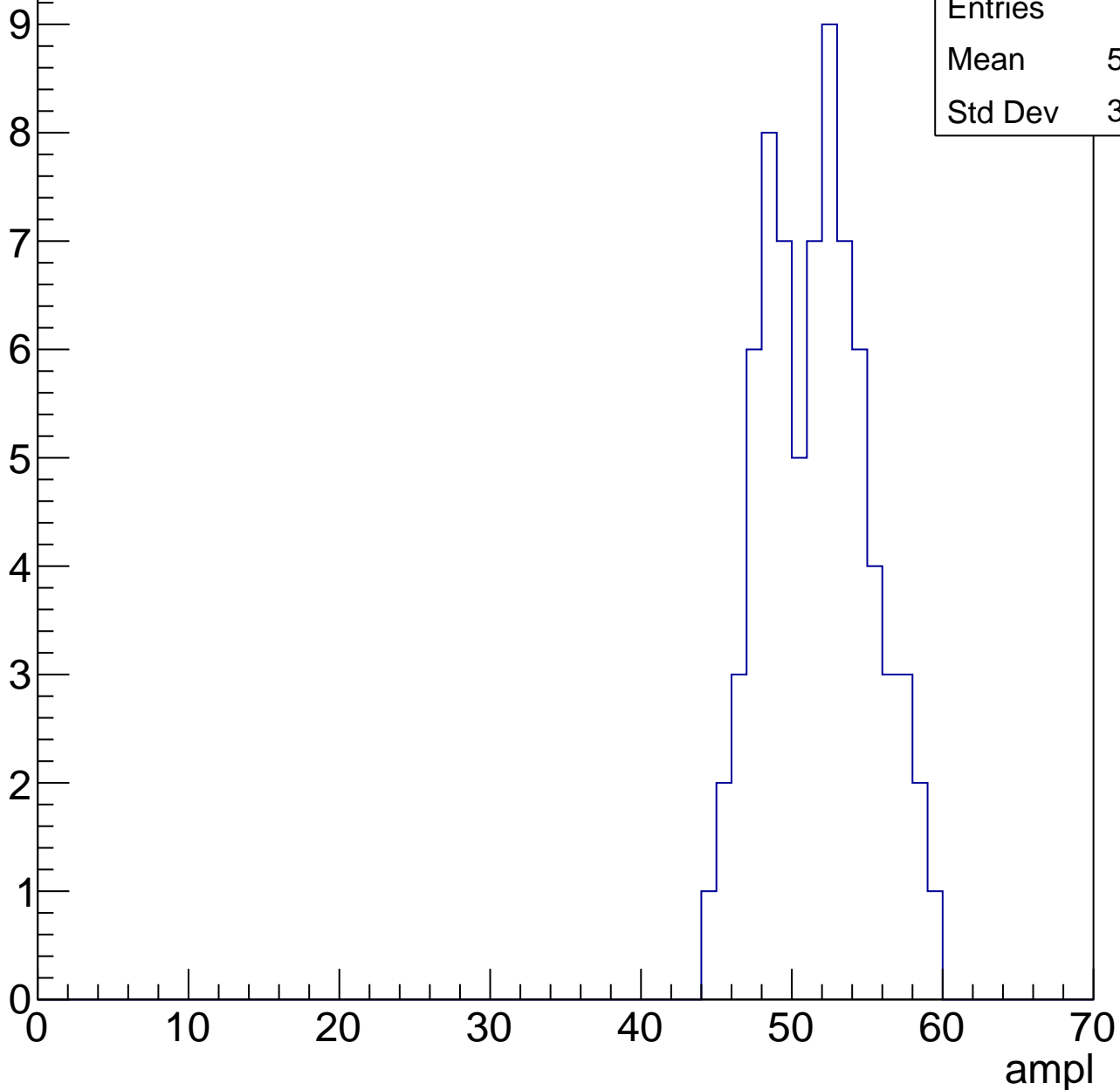


# B0L001S, U24-ch101, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	51.15
Std Dev	3.478

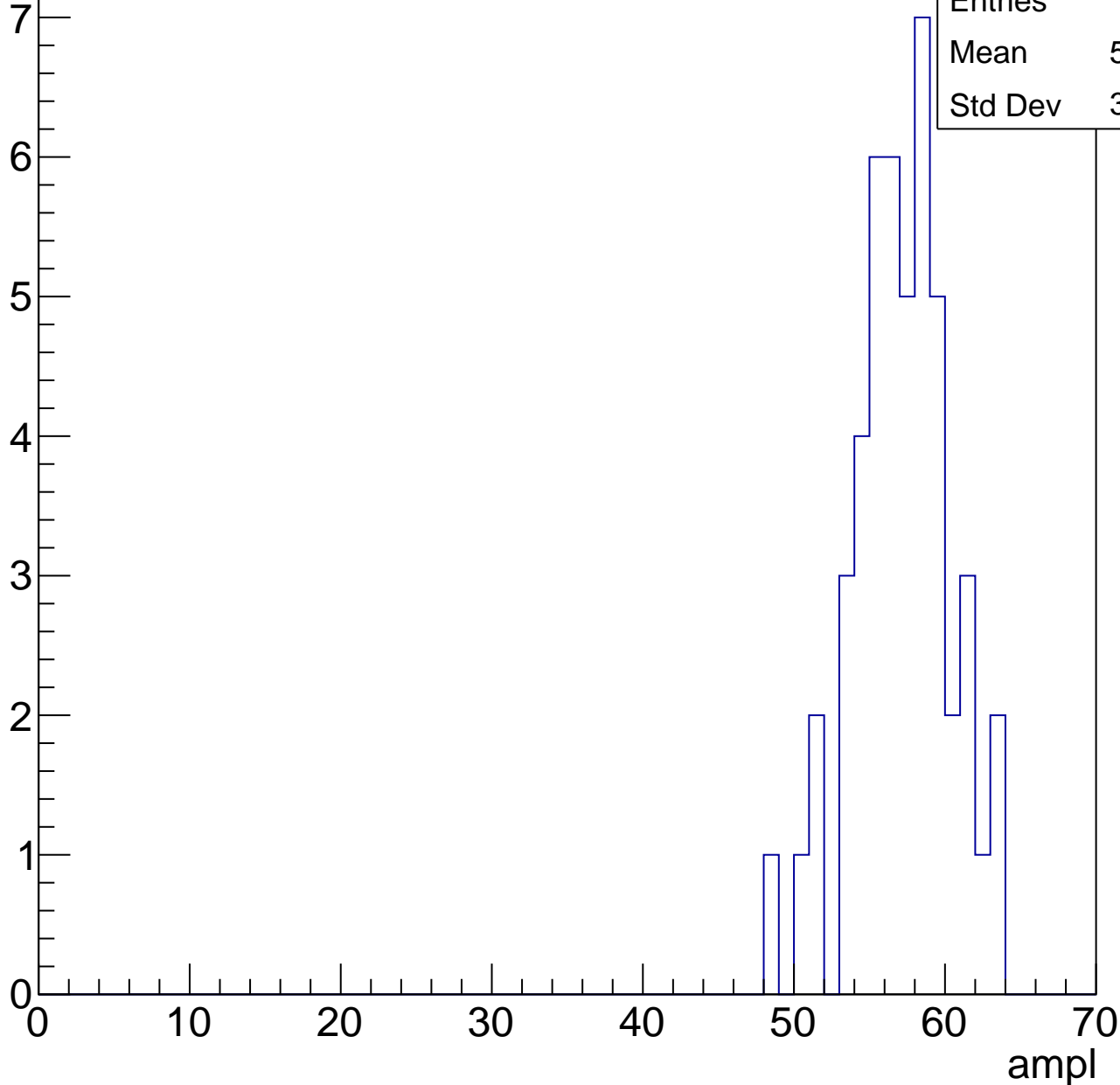


# B0L001S, U24-ch101, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

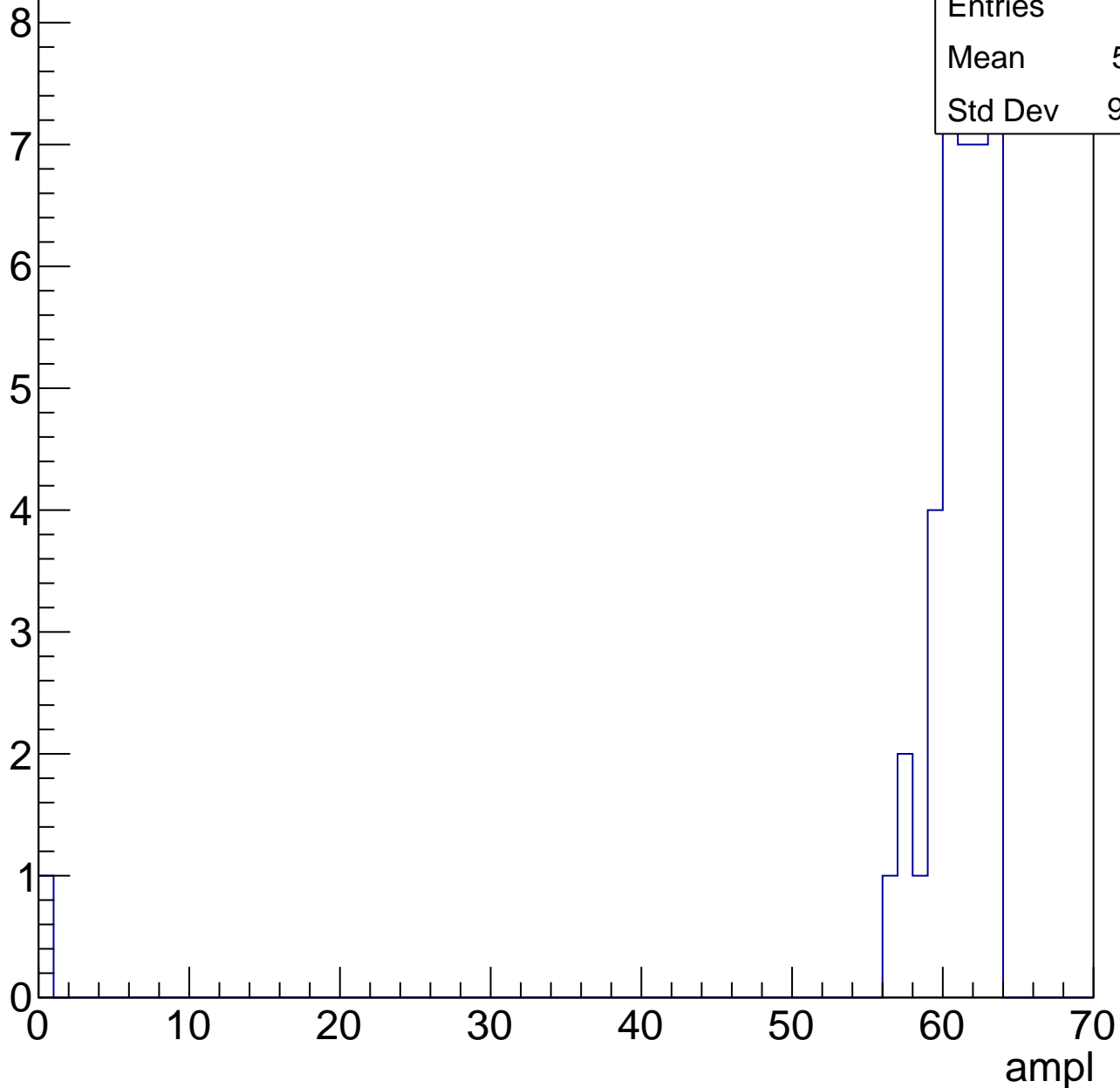
Entries	48
Mean	56.62
Std Dev	3.225



# B0L001S, U24-ch101, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U24-ch101, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch101, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L001S, U24-ch102, adc0

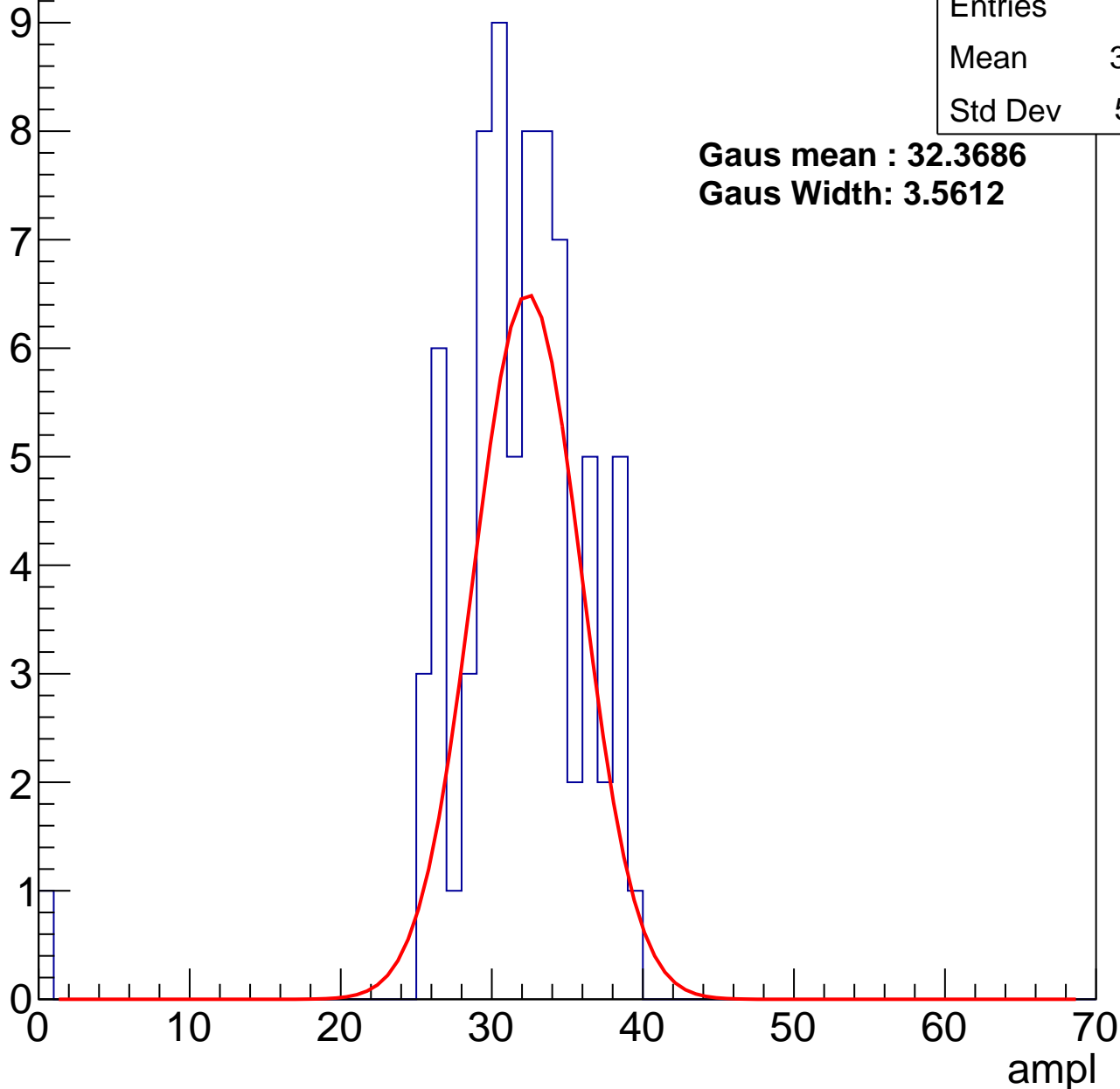
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	31.22
Std Dev	5.121

**Gaus mean : 32.3686**

**Gaus Width: 3.5612**



# B0L001S, U24-ch102, adc1

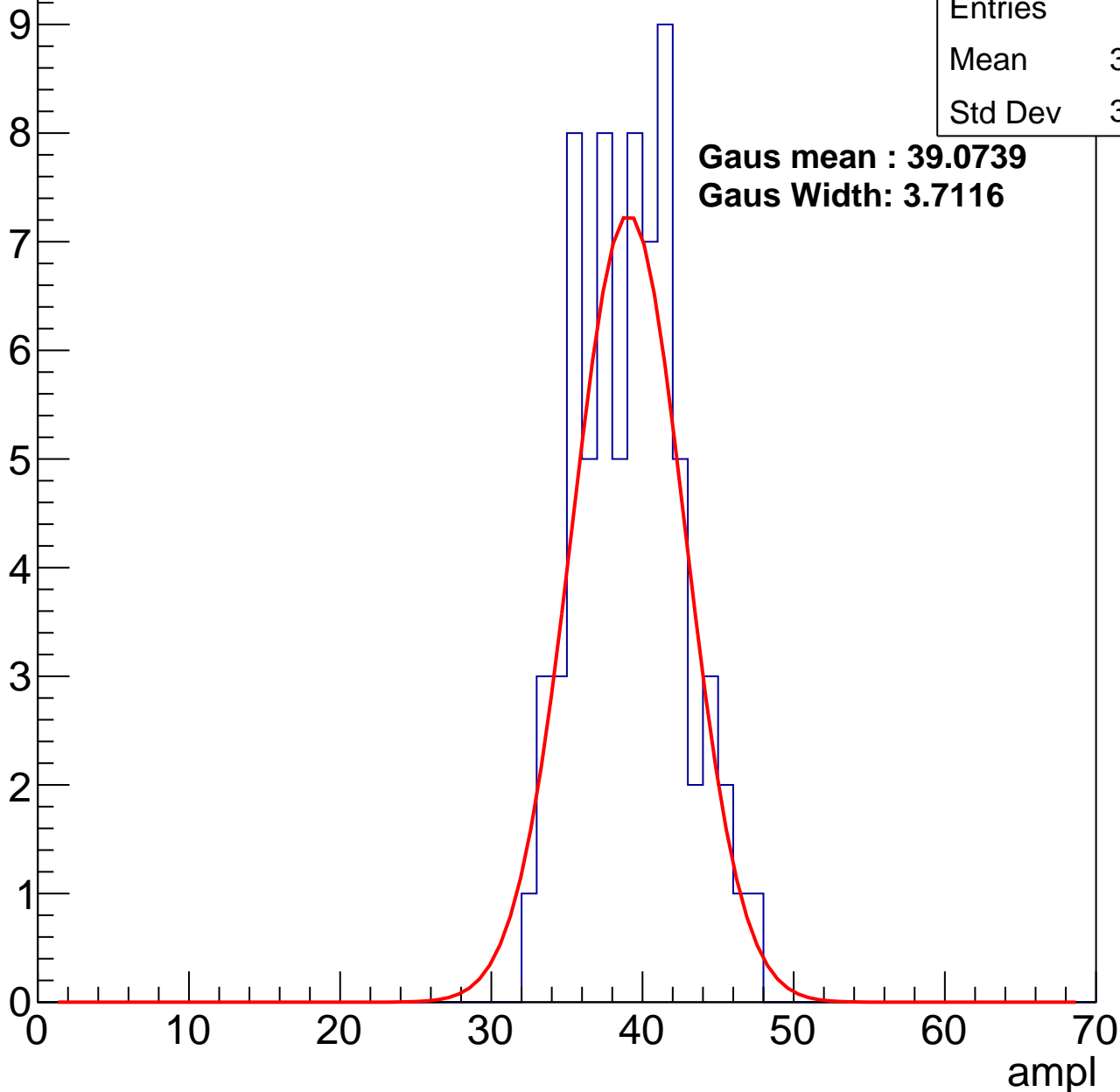
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	38.75
Std Dev	3.393

**Gaus mean : 39.0739**

**Gaus Width: 3.7116**



# B0L001S, U24-ch102, adc2

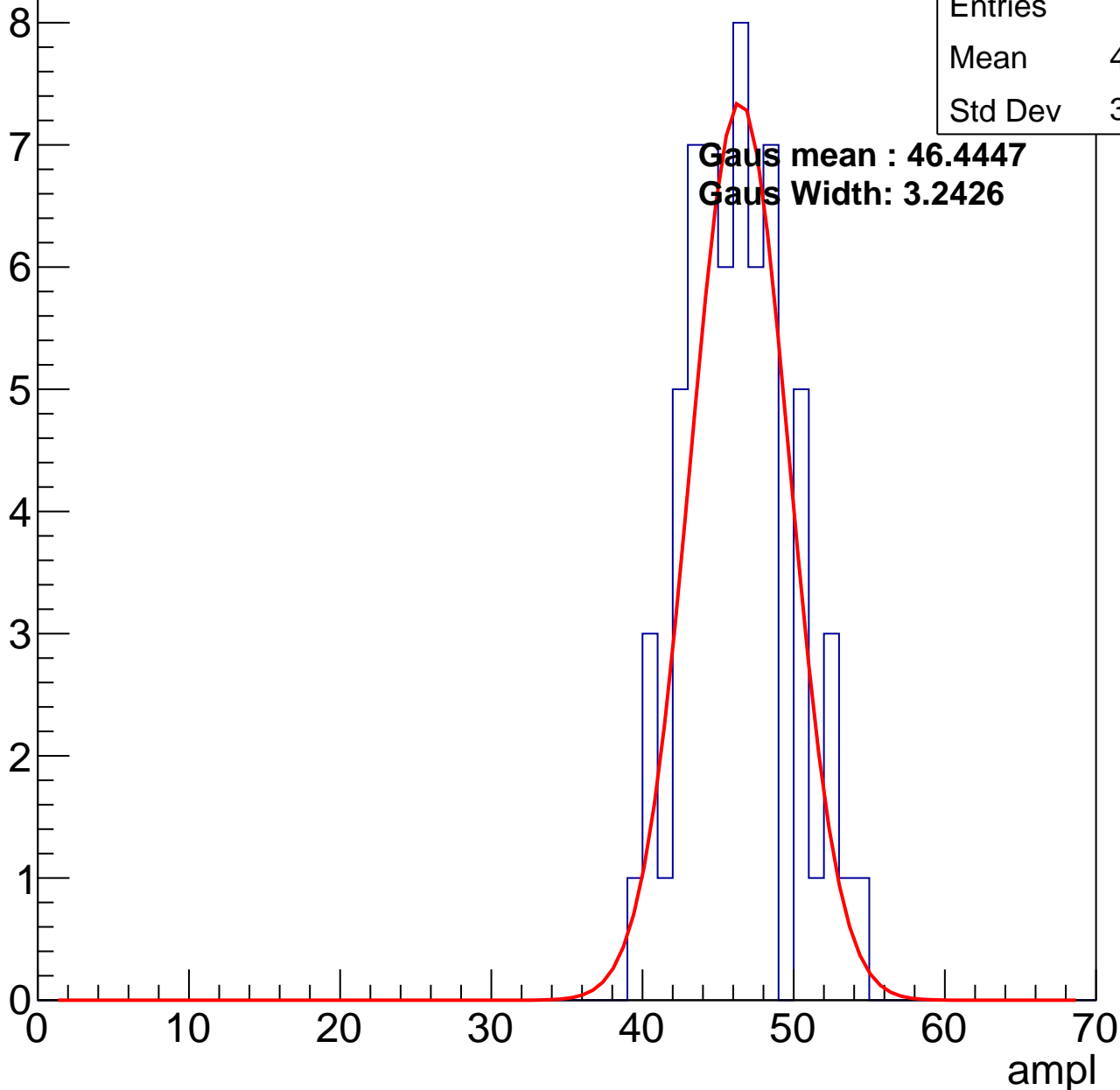
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	45.79
Std Dev	3.399

**Gaus mean : 46.4447**

**Gaus Width: 3.2426**



# B0L001S, U24-ch102, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

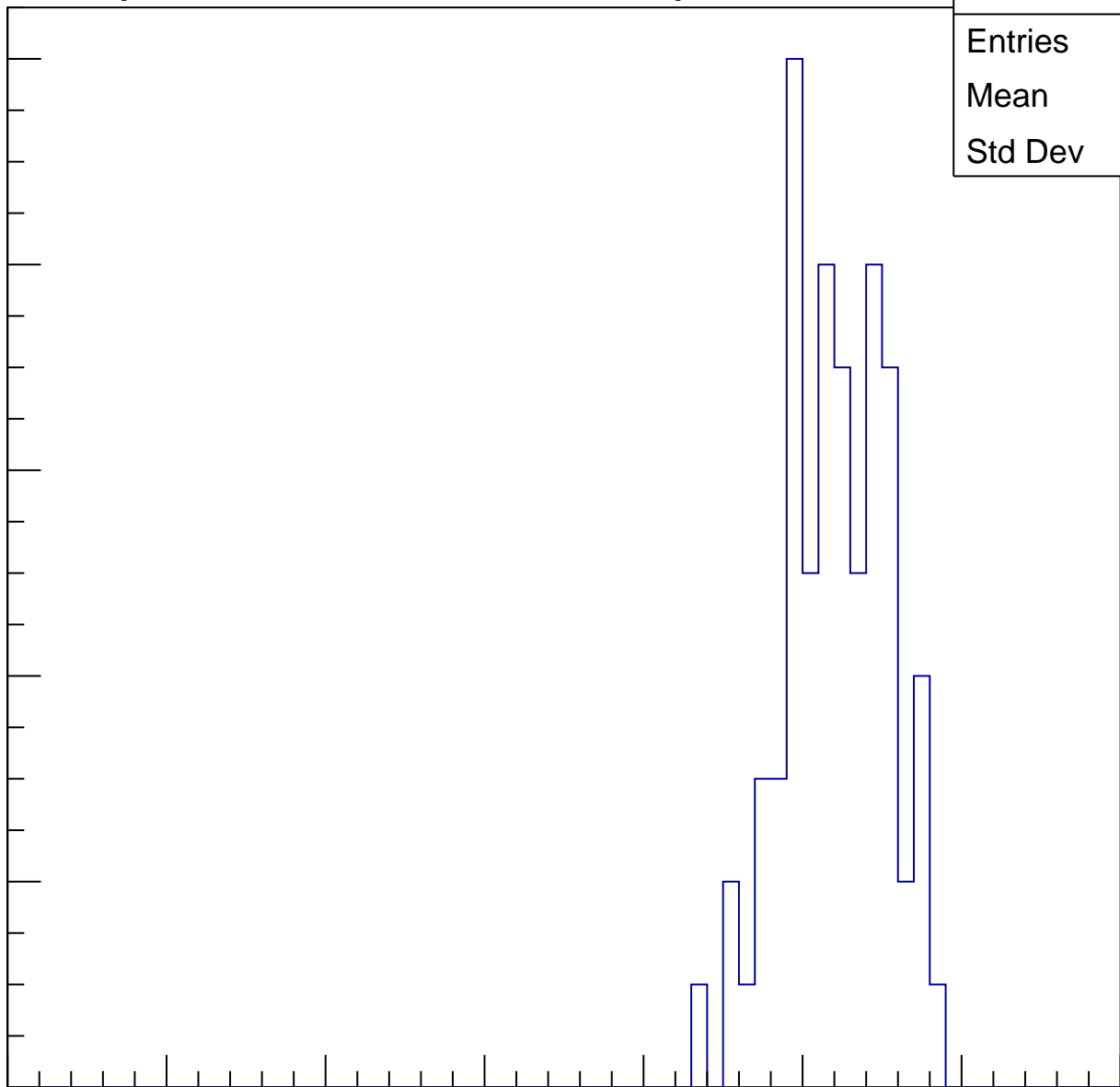
Entries	67
Mean	51.58
Std Dev	3.261

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

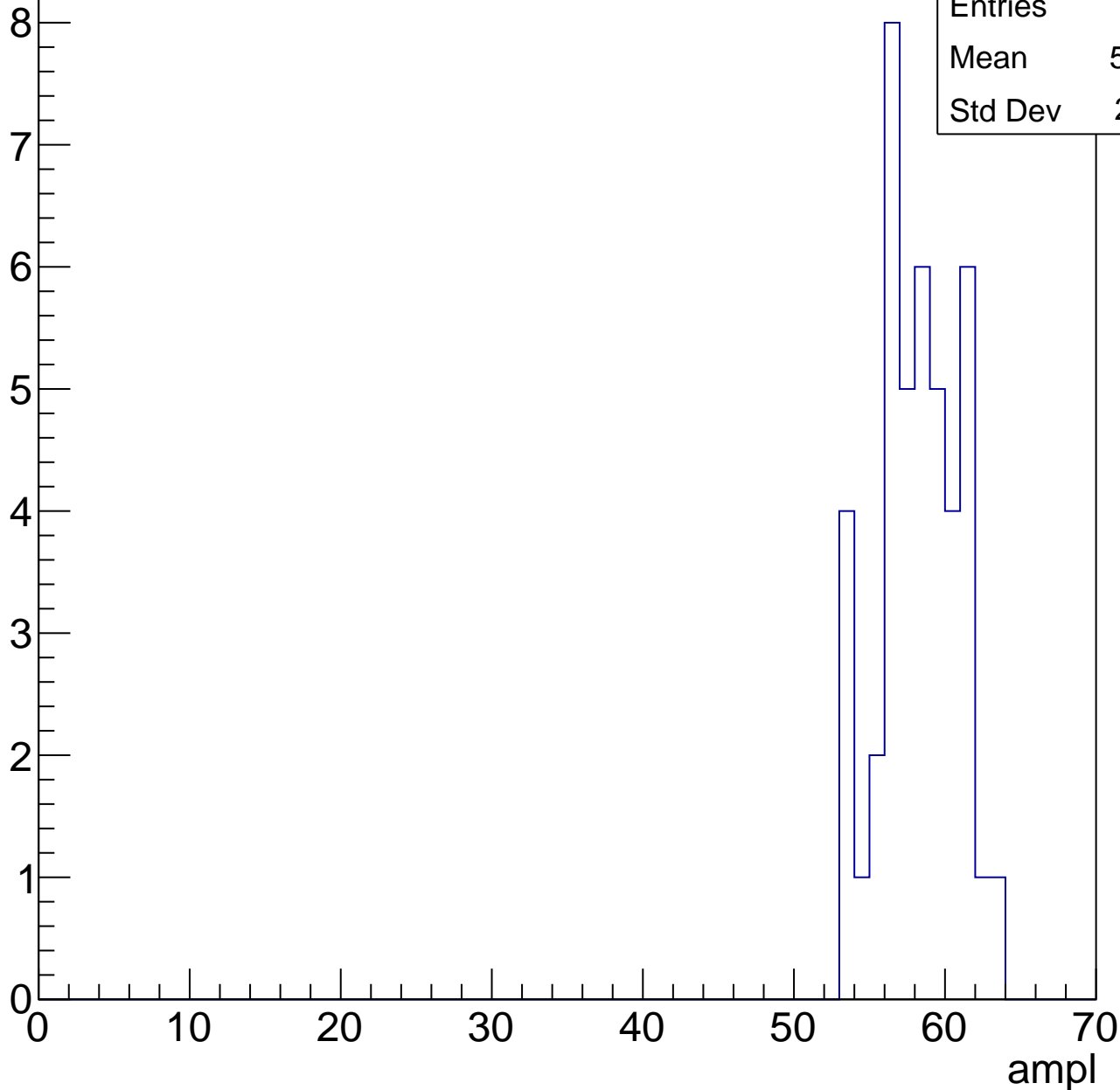


# B0L001S, U24-ch102, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	43
Mean	57.74
Std Dev	2.571

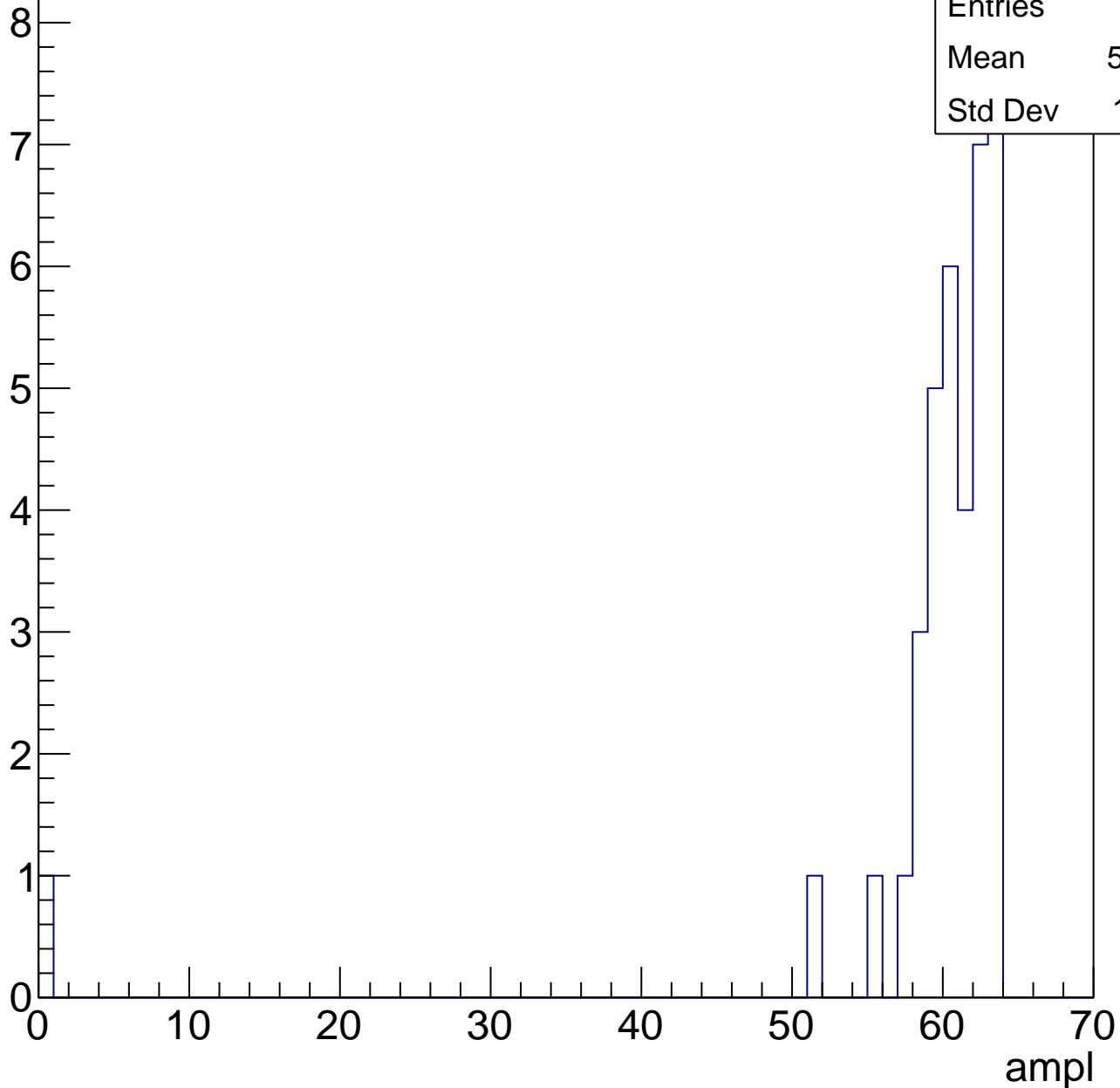


# B0L001S, U24-ch102, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	37
Mean	58.76
Std Dev	10.11



# B0L001S, U24-ch102, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

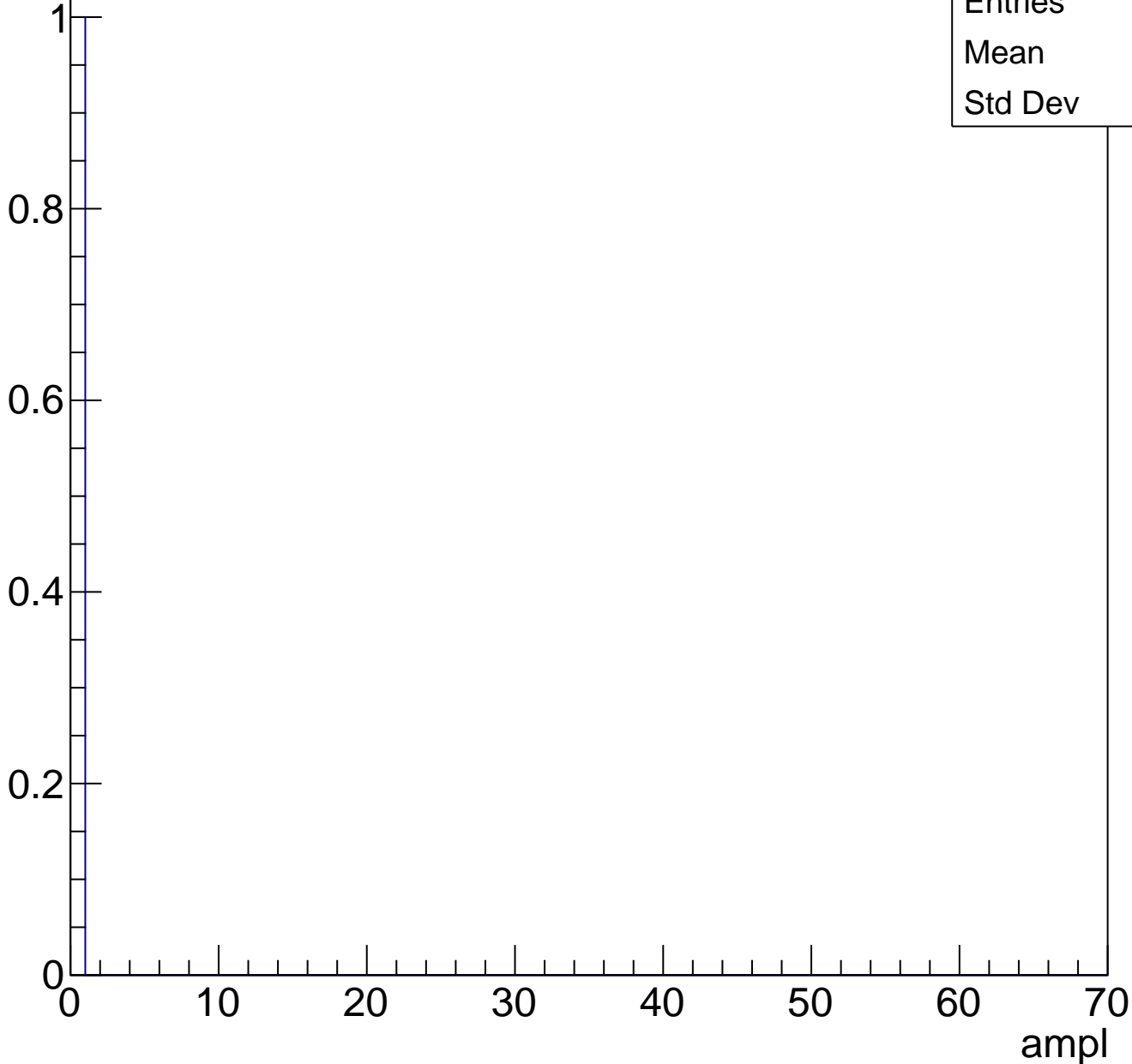




# B0L001S, U24-ch102, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U24-ch103, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	79
Mean	32.04
Std Dev	4.193

**Gaus mean : 32.7754**

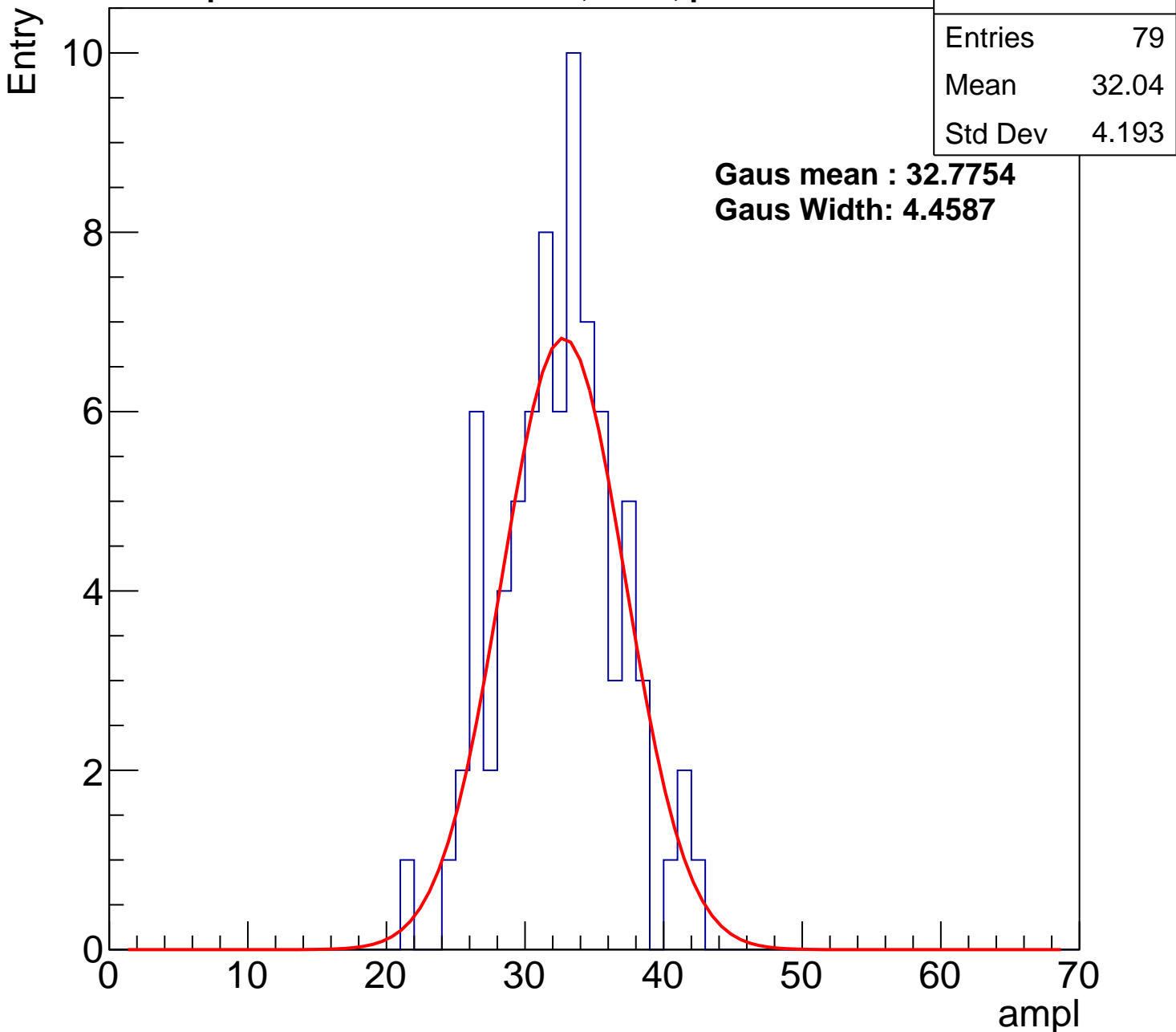
**Gaus Width: 4.4587**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U24-ch103, adc1

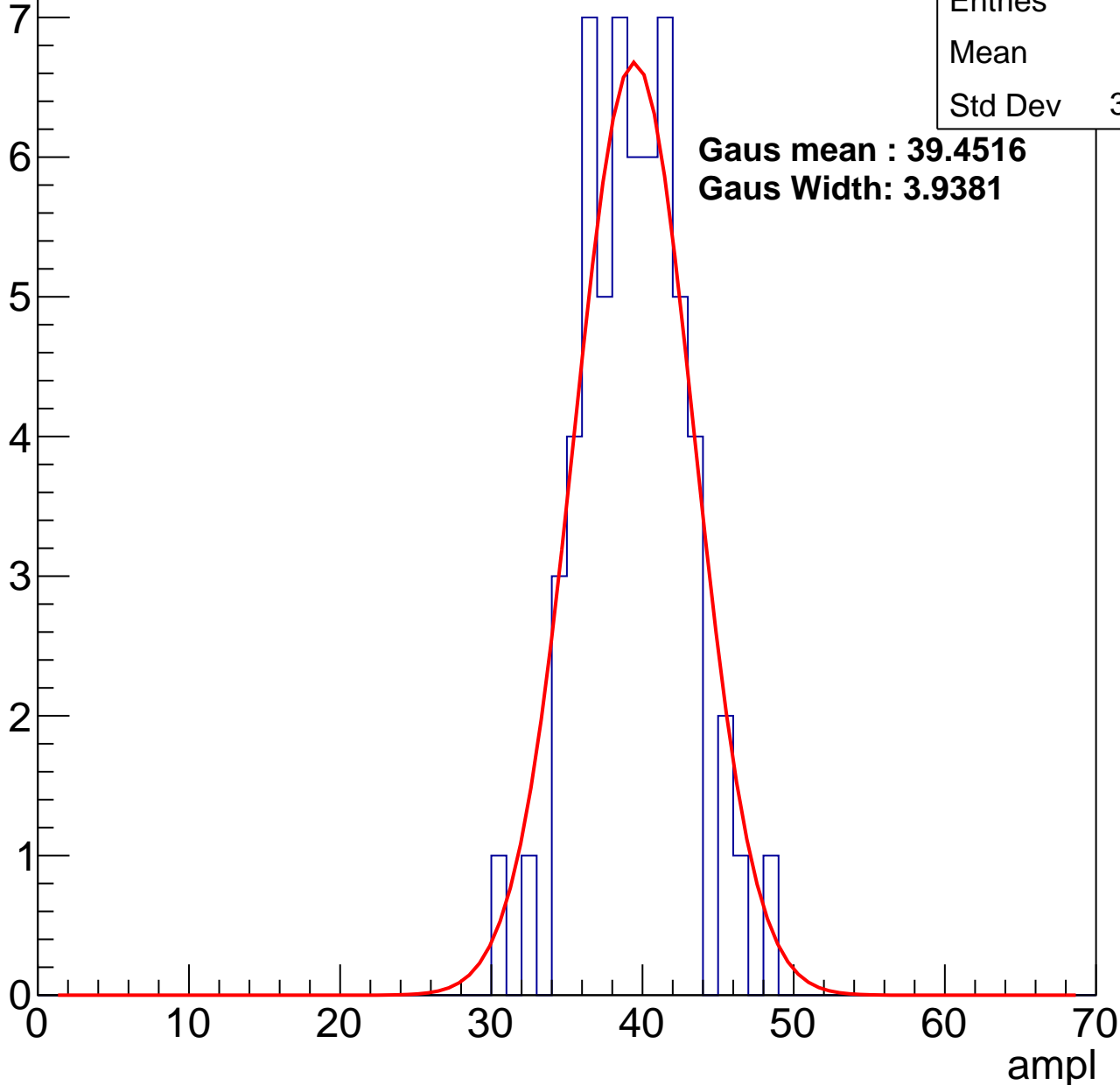
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	38.9
Std Dev	3.424

**Gaus mean : 39.4516**

**Gaus Width: 3.9381**



# B0L001S, U24-ch103, adc2

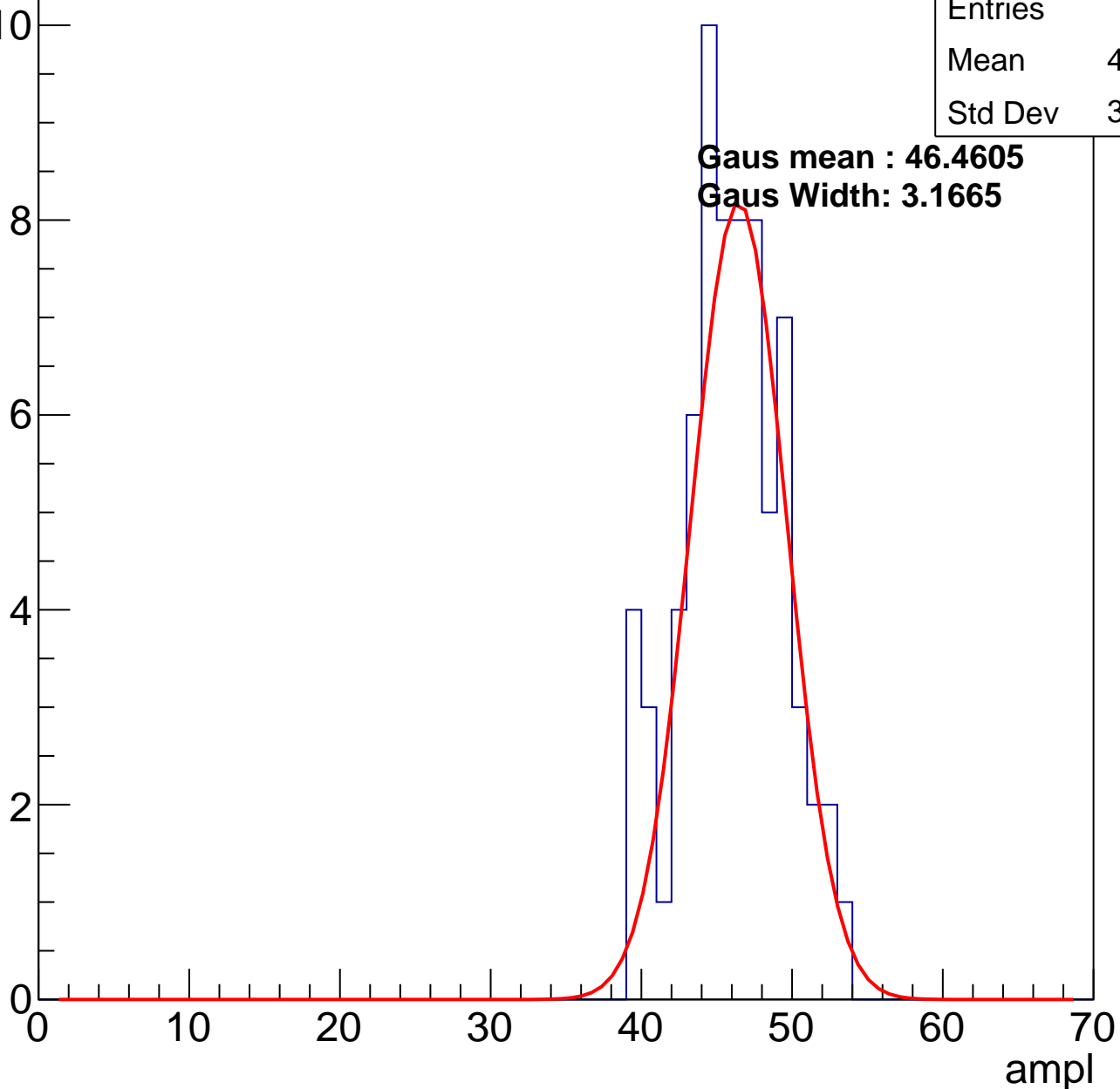
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	45.54
Std Dev	3.312

**Gaus mean : 46.4605**

**Gaus Width: 3.1665**

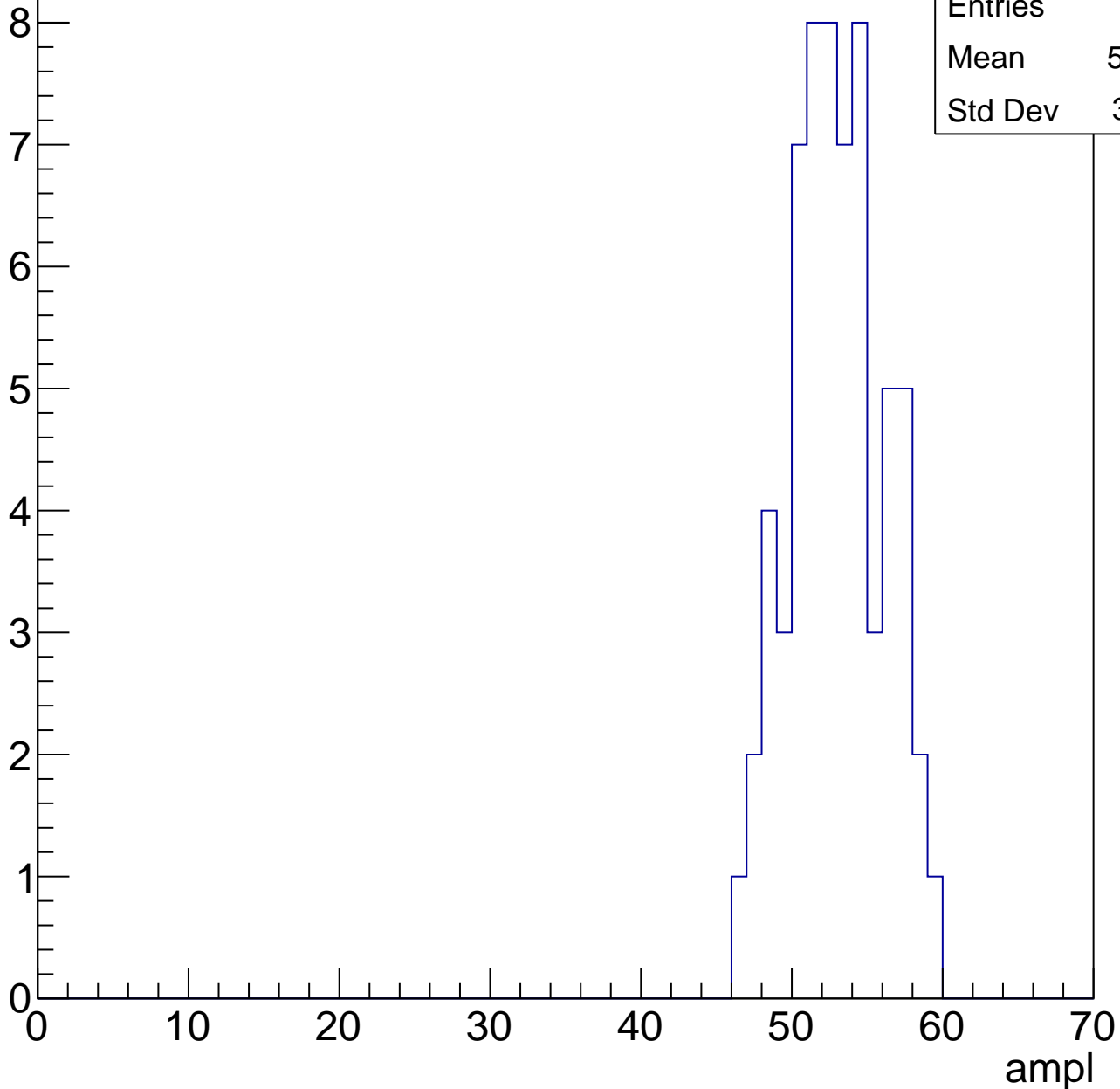


# B0L001S, U24-ch103, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

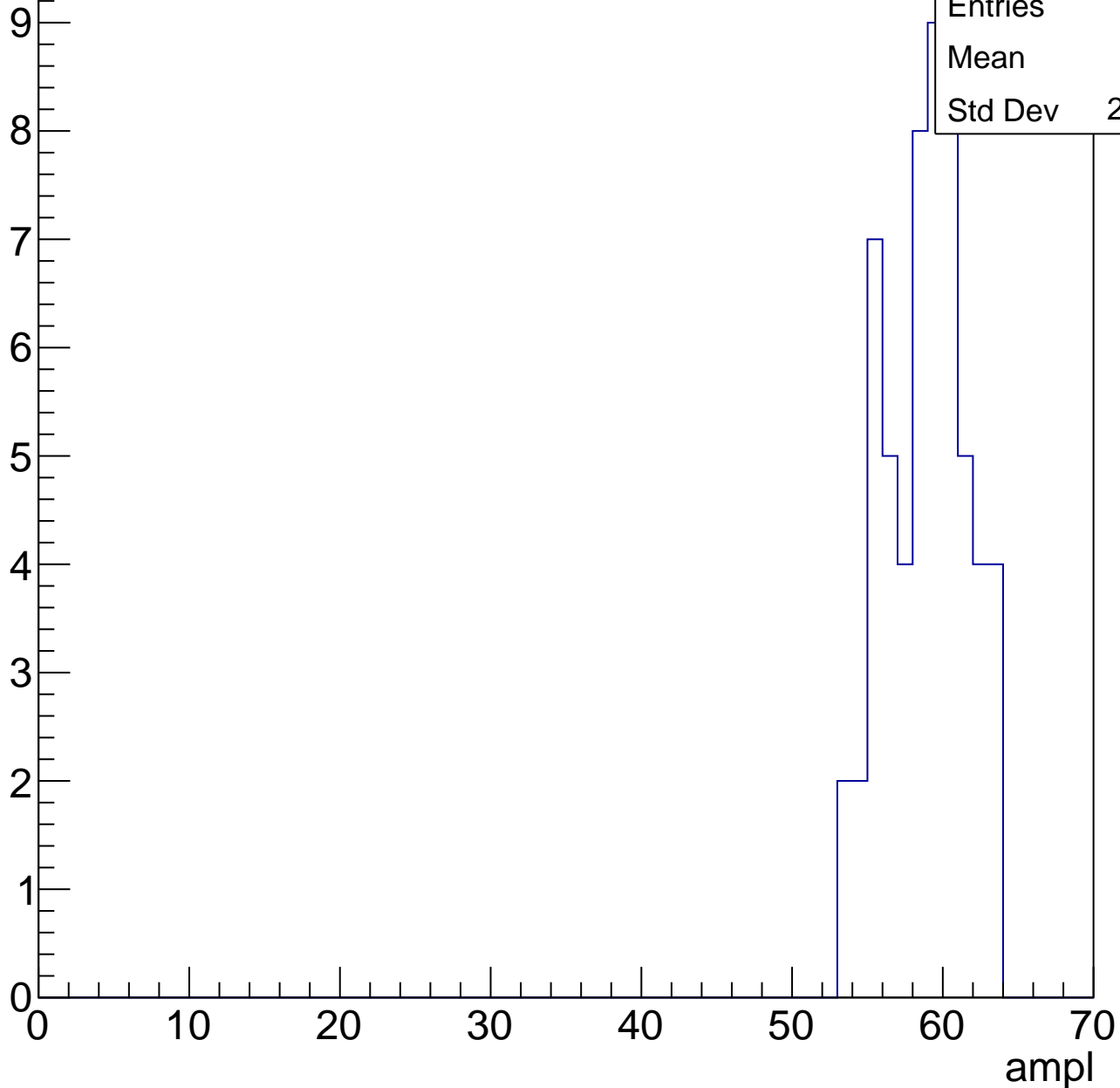
Entries	64
Mean	52.52
Std Dev	3.031



# B0L001S, U24-ch103, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

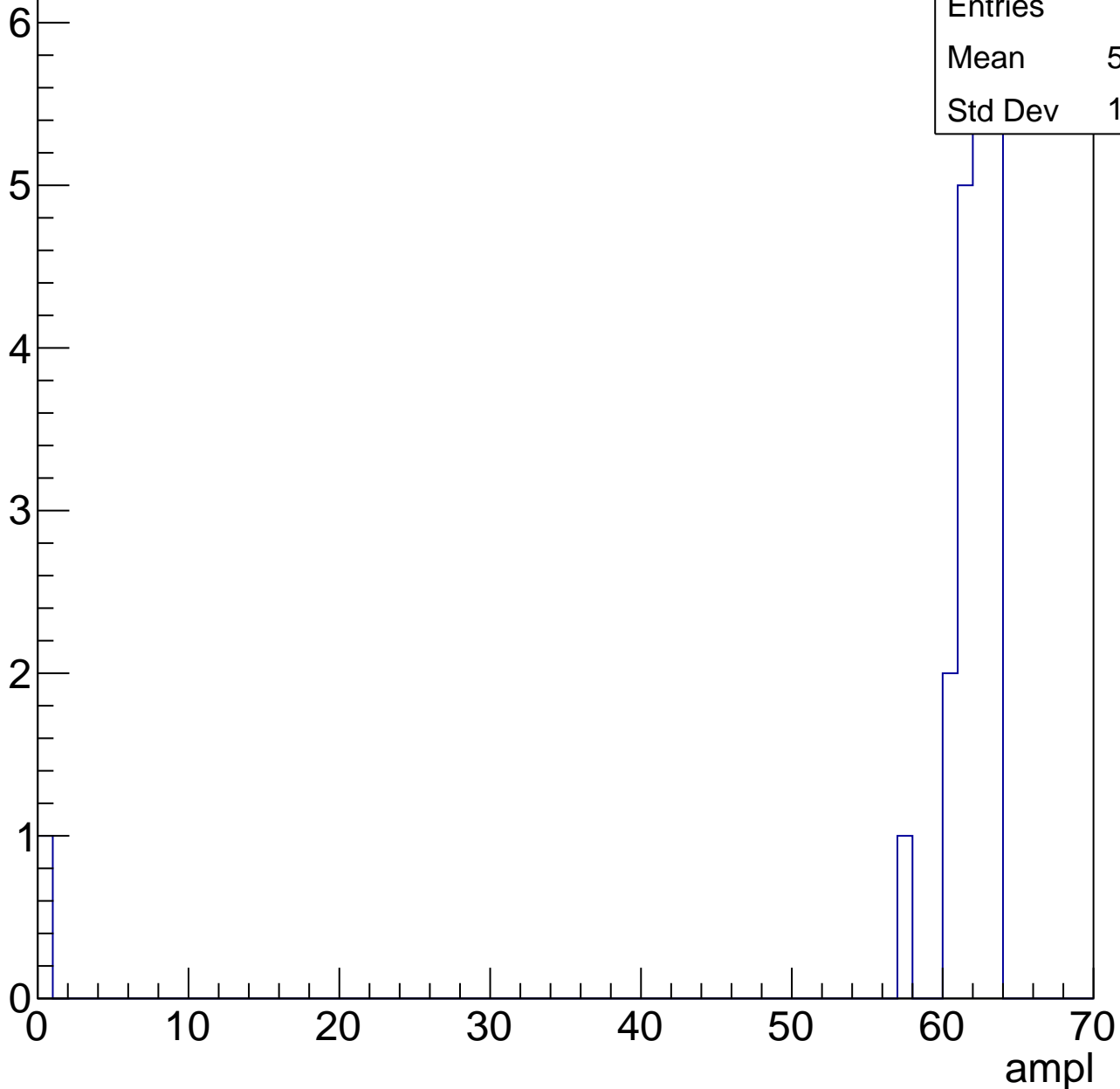


# B0L001S, U24-ch103, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	21
Mean	58.67
Std Dev	13.19



# B0L001S, U24-ch103, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U24-ch103, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U24-ch104, adc0

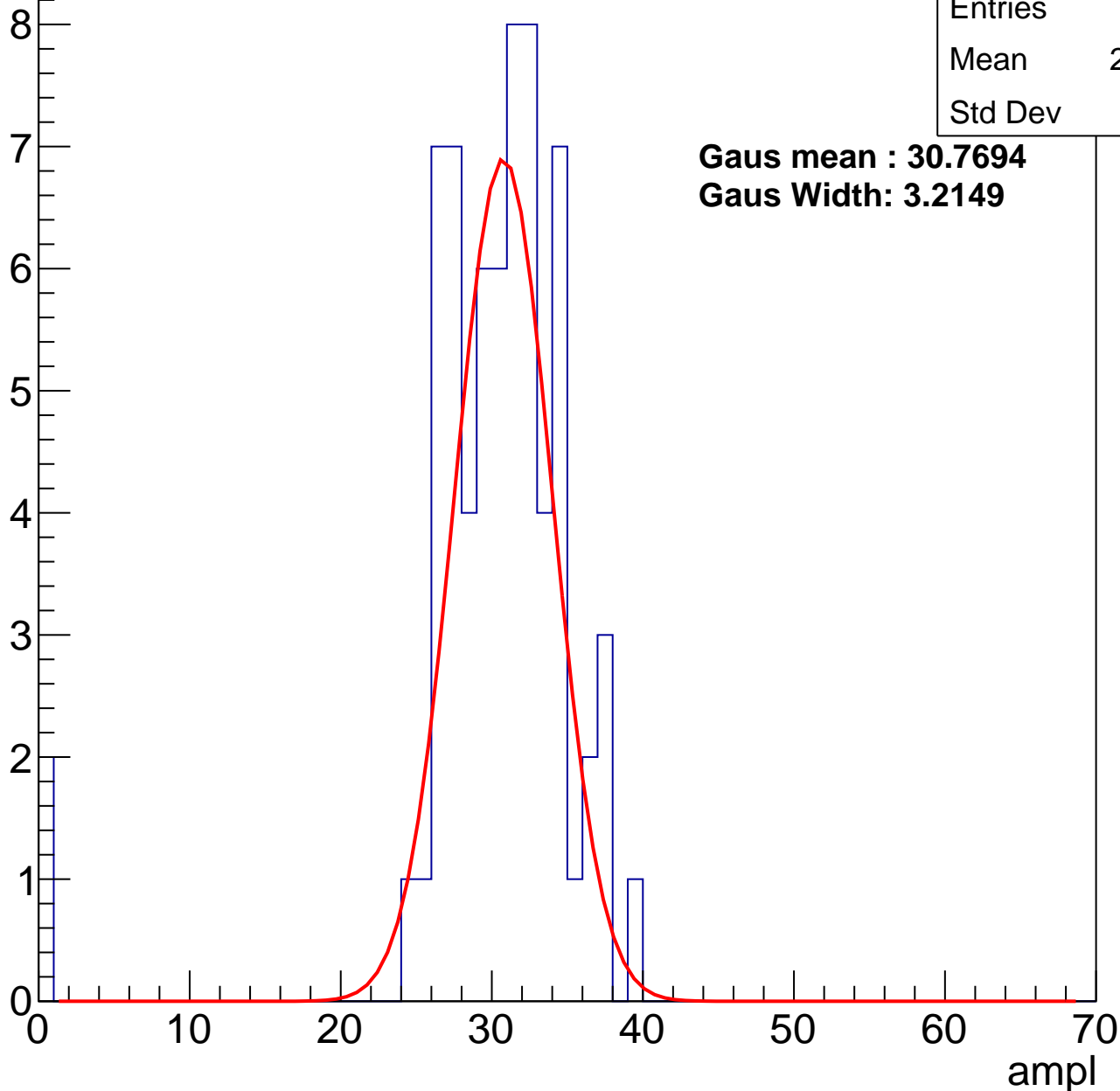
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	29.66
Std Dev	6.14

**Gaus mean : 30.7694**

**Gaus Width: 3.2149**



# B0L001S, U24-ch104, adc1

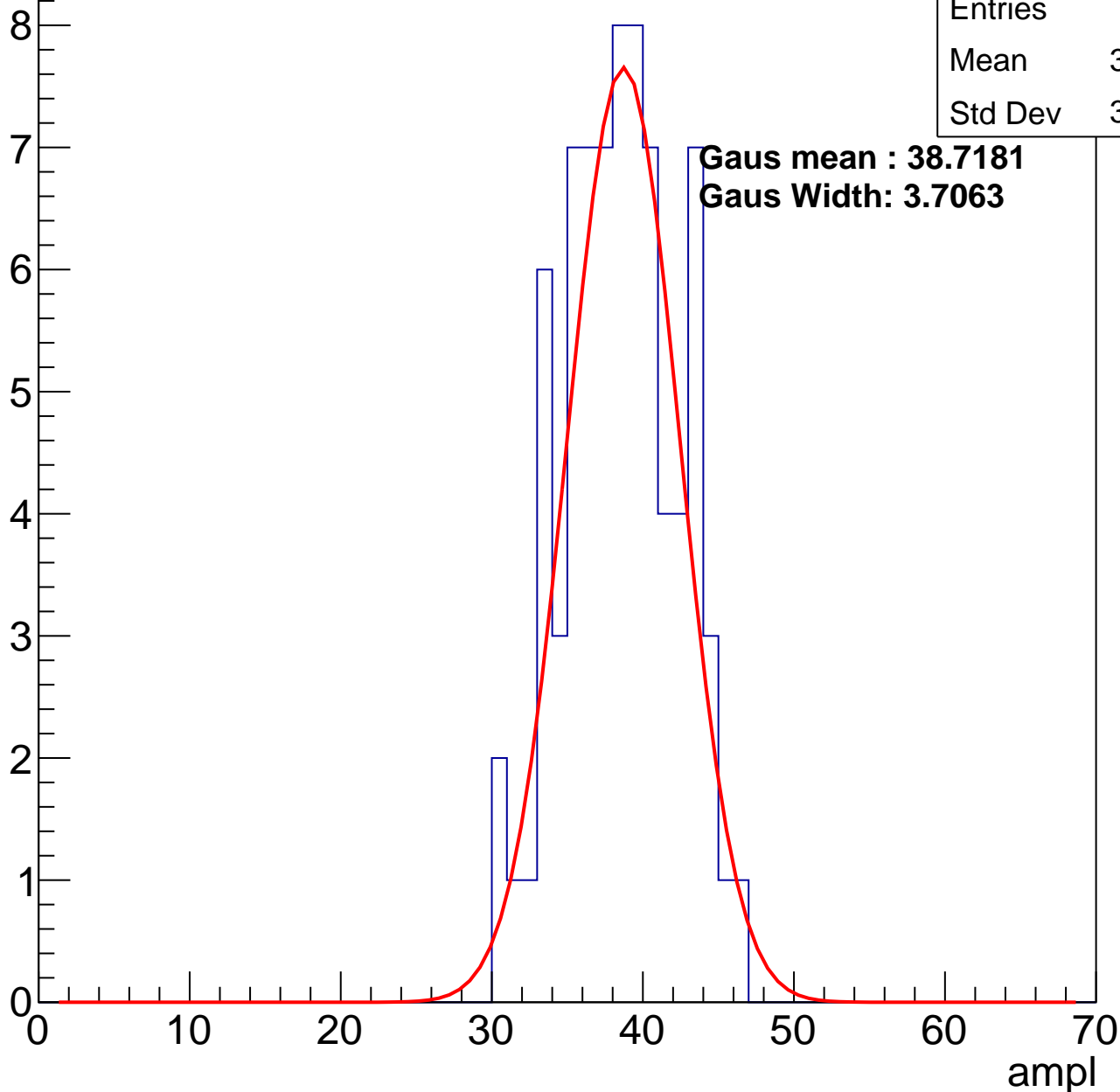
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	77
Mean	38.06
Std Dev	3.676

**Gaus mean : 38.7181**

**Gaus Width: 3.7063**



# B0L001S, U24-ch104, adc2

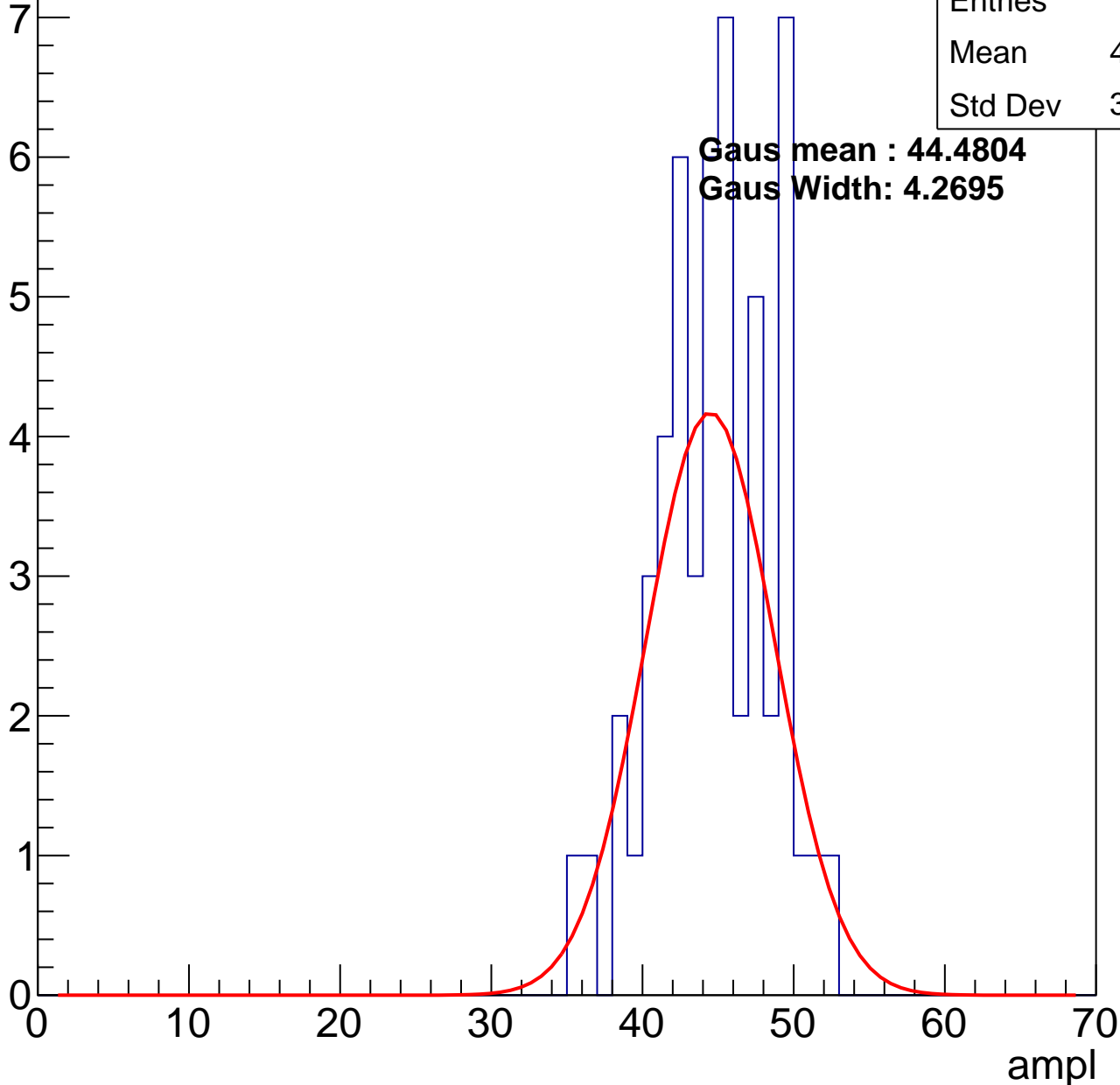
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	44.32
Std Dev	3.796

**Gaus mean : 44.4804**

**Gaus Width: 4.2695**



# B0L001S, U24-ch104, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	73
Mean	50.52
Std Dev	3.753

Entry

10

8

6

4

2

0

0

10

20

30

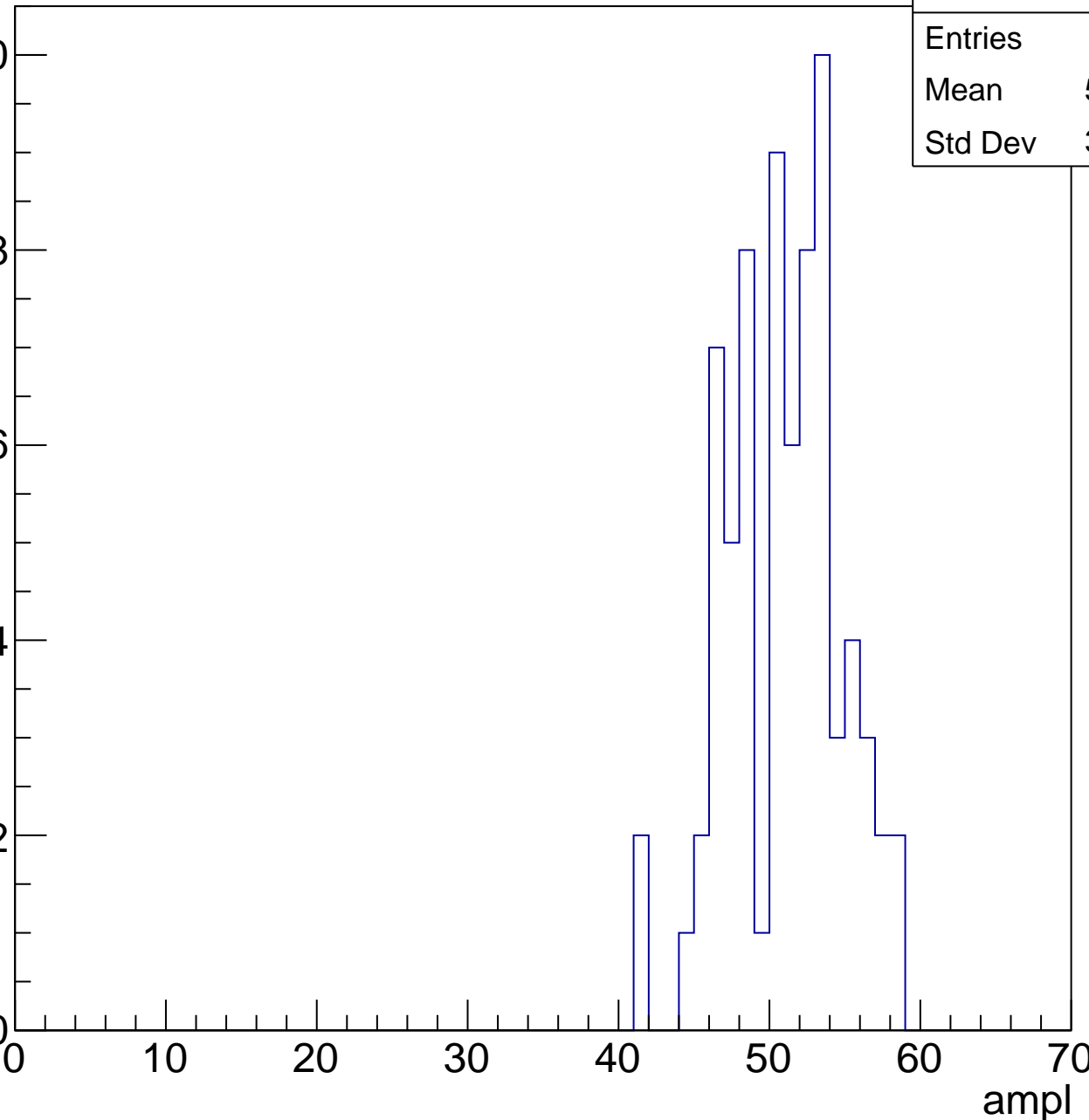
40

50

60

ampl

70

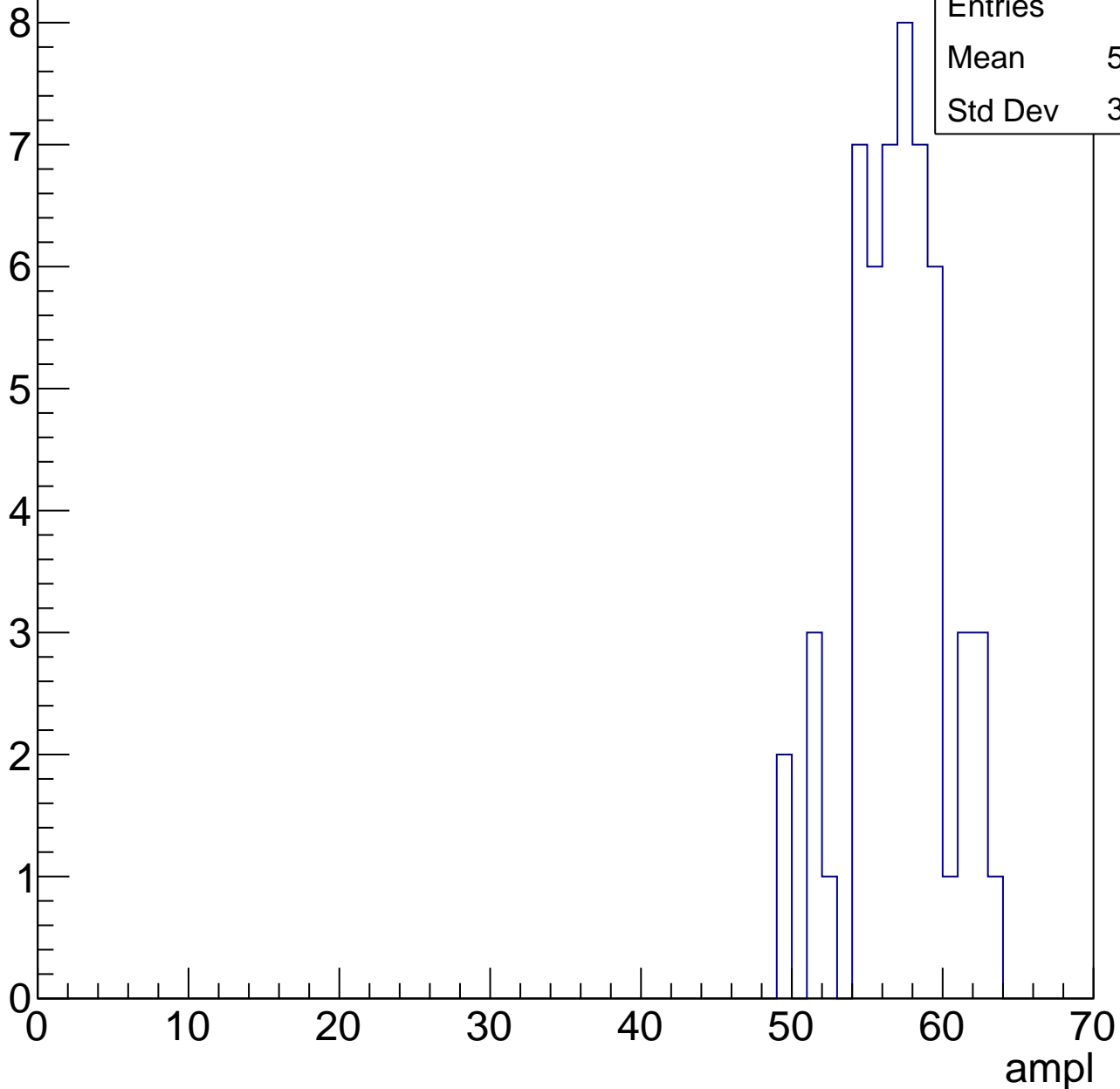


# B0L001S, U24-ch104, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	56.56
Std Dev	3.144

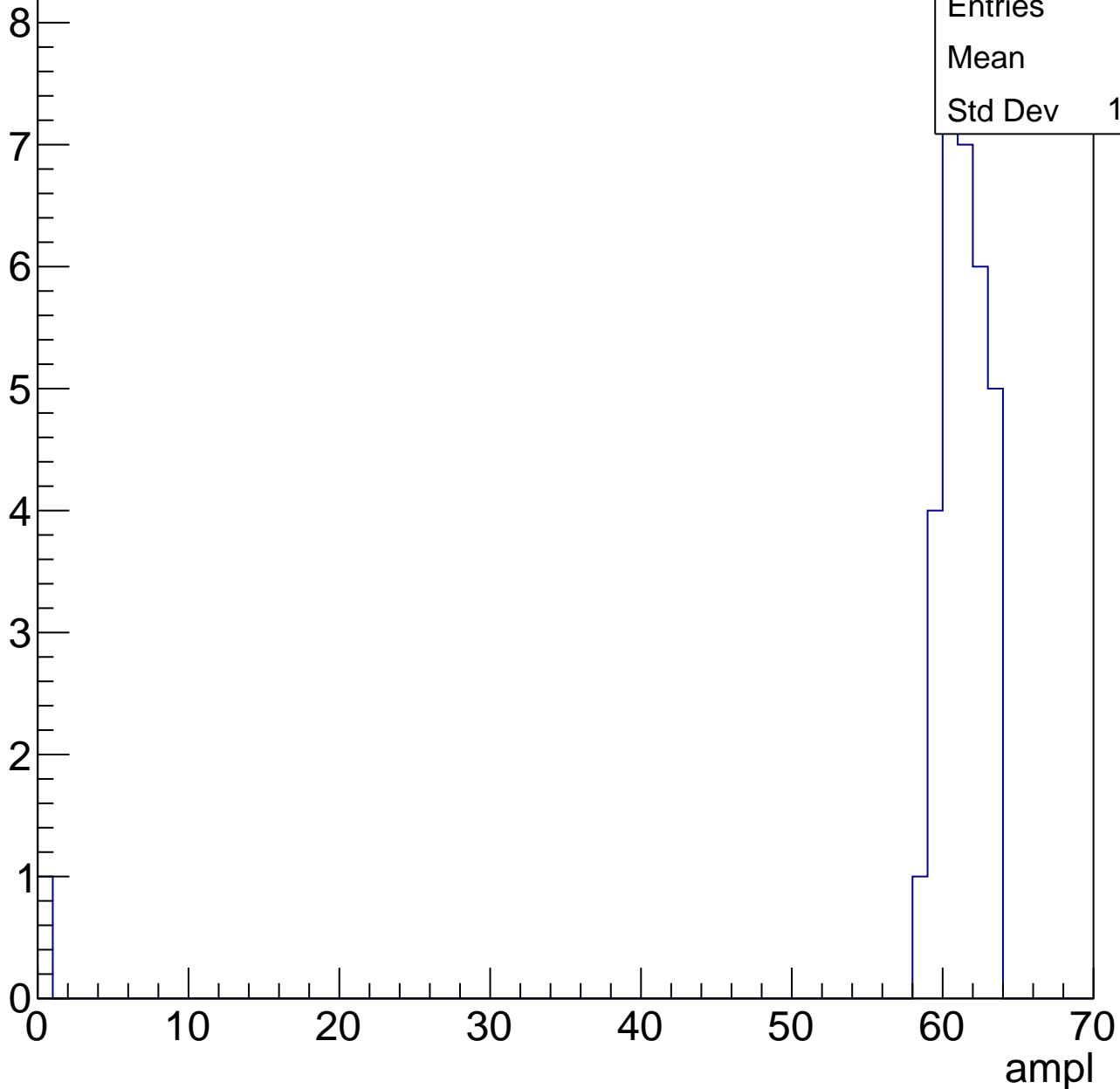


# B0L001S, U24-ch104, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

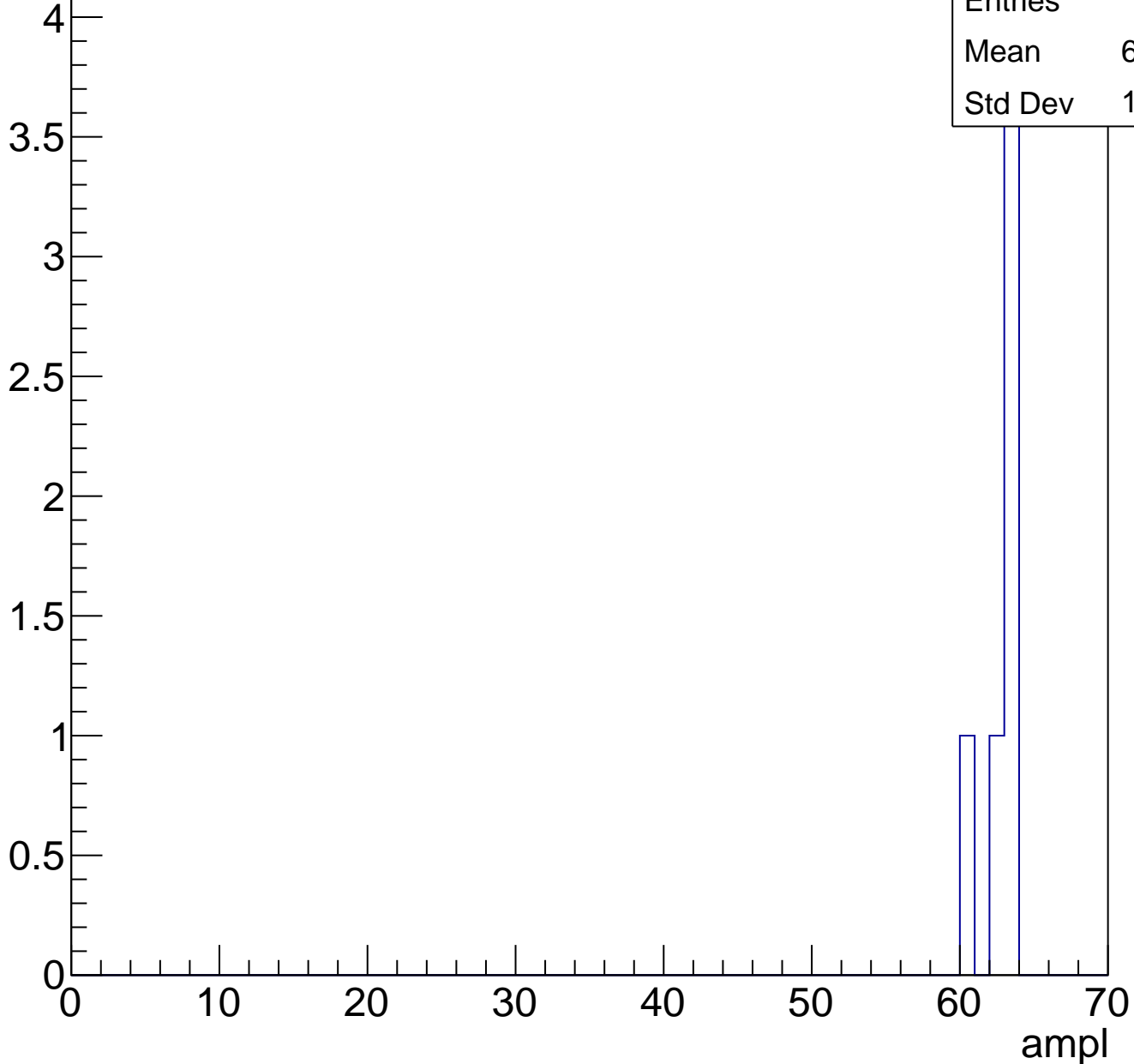
Entries	32
Mean	59
Std Dev	10.68



# B0L001S, U24-ch104, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch104, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U24-ch105, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	93
Mean	29.88
Std Dev	4.042

**Gaus mean : 29.9523**

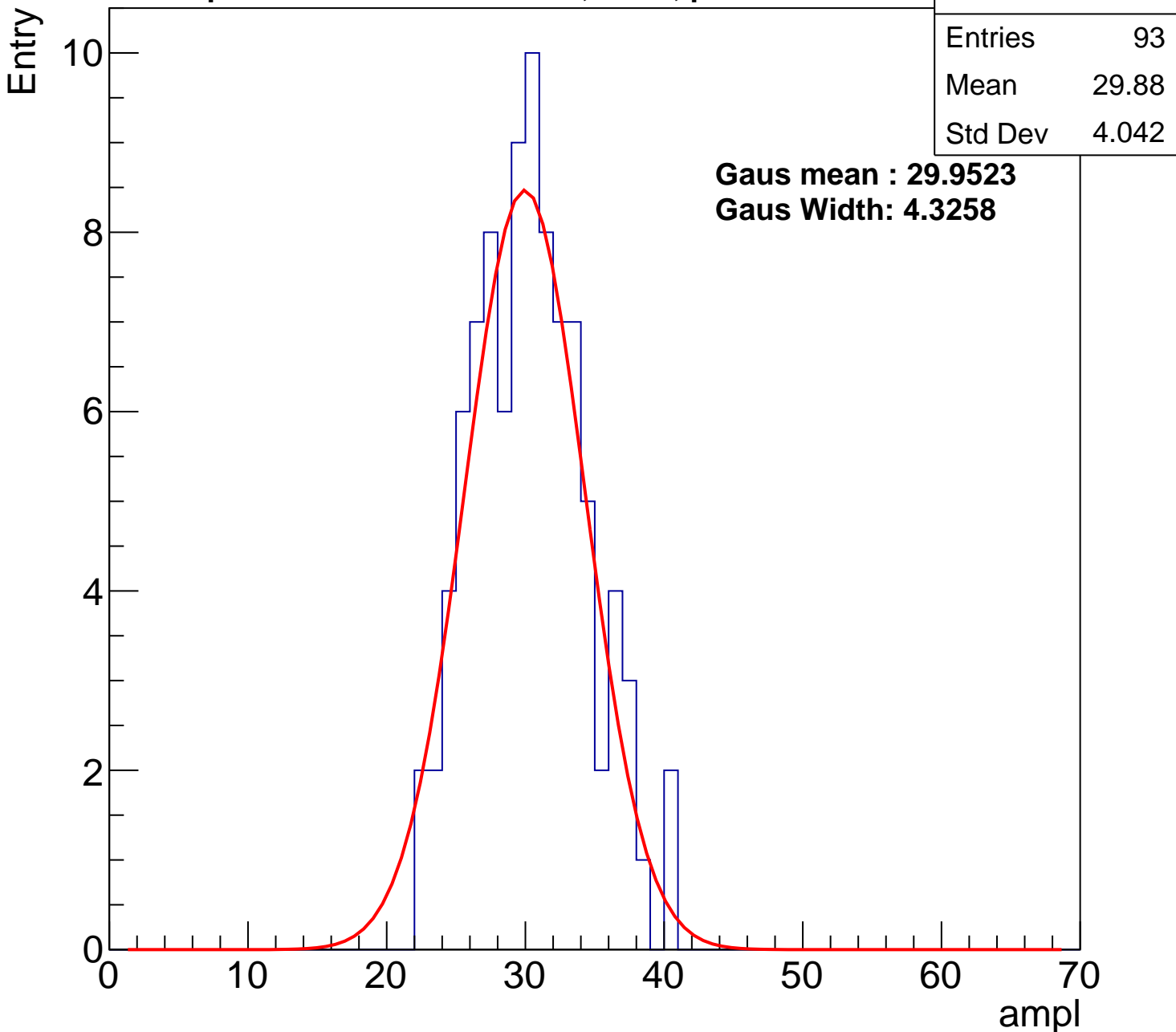
**Gaus Width: 4.3258**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U24-ch105, adc1

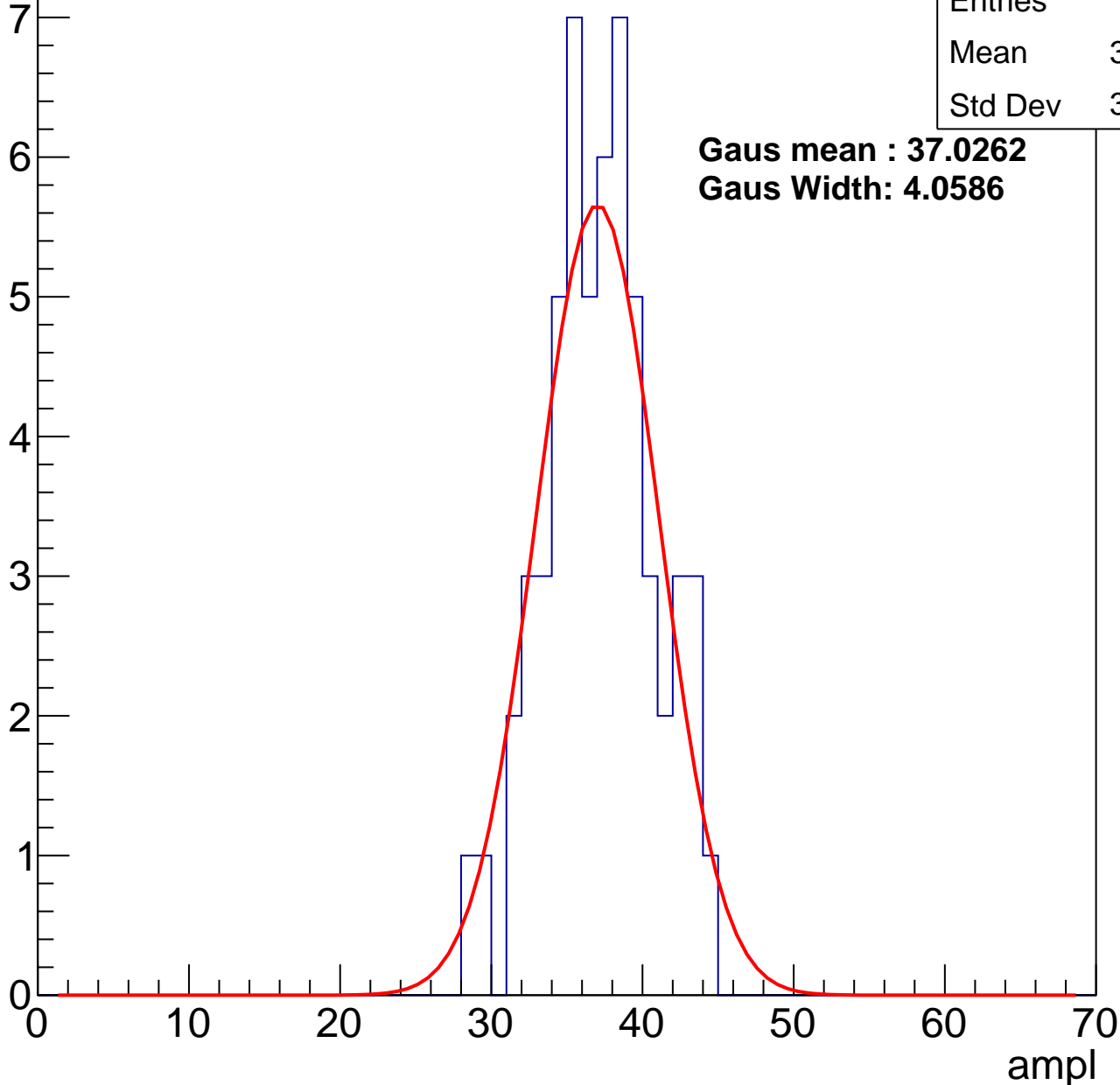
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	36.72
Std Dev	3.582

**Gaus mean : 37.0262**

**Gaus Width: 4.0586**



# B0L001S, U24-ch105, adc2

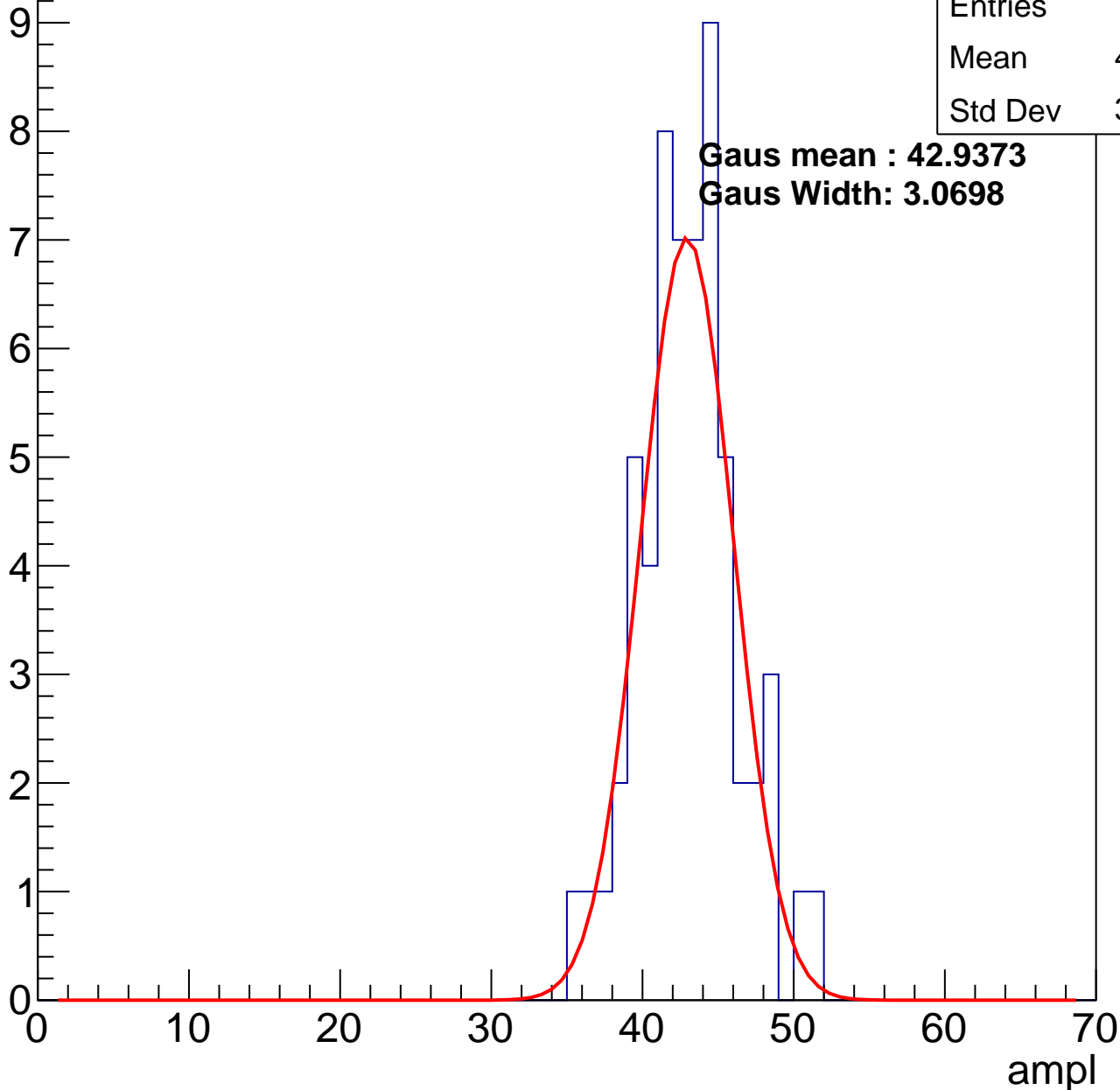
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	42.61
Std Dev	3.221

**Gaus mean : 42.9373**

**Gaus Width: 3.0698**

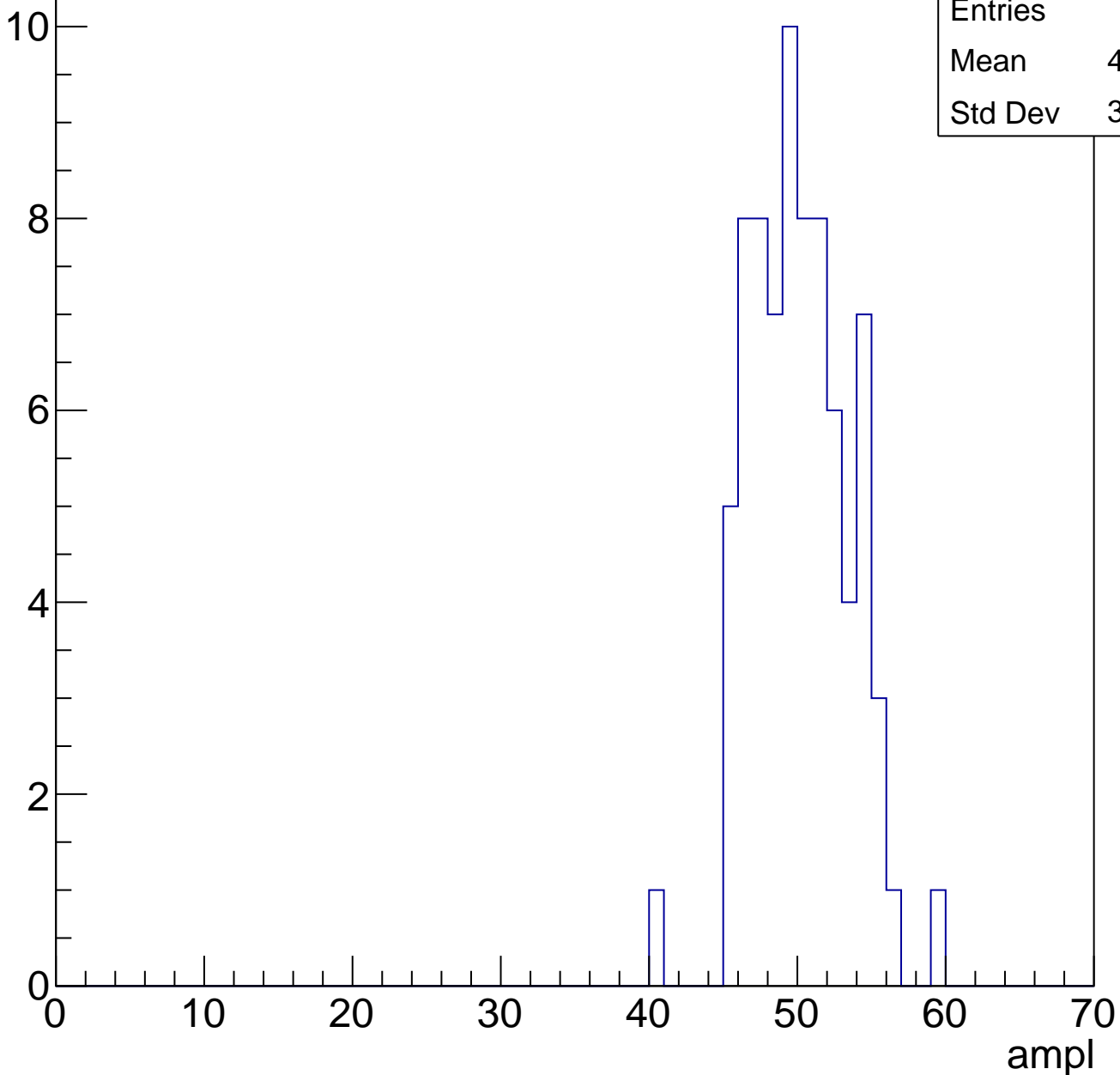


# B0L001S, U24-ch105, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	77
Mean	49.68
Std Dev	3.277

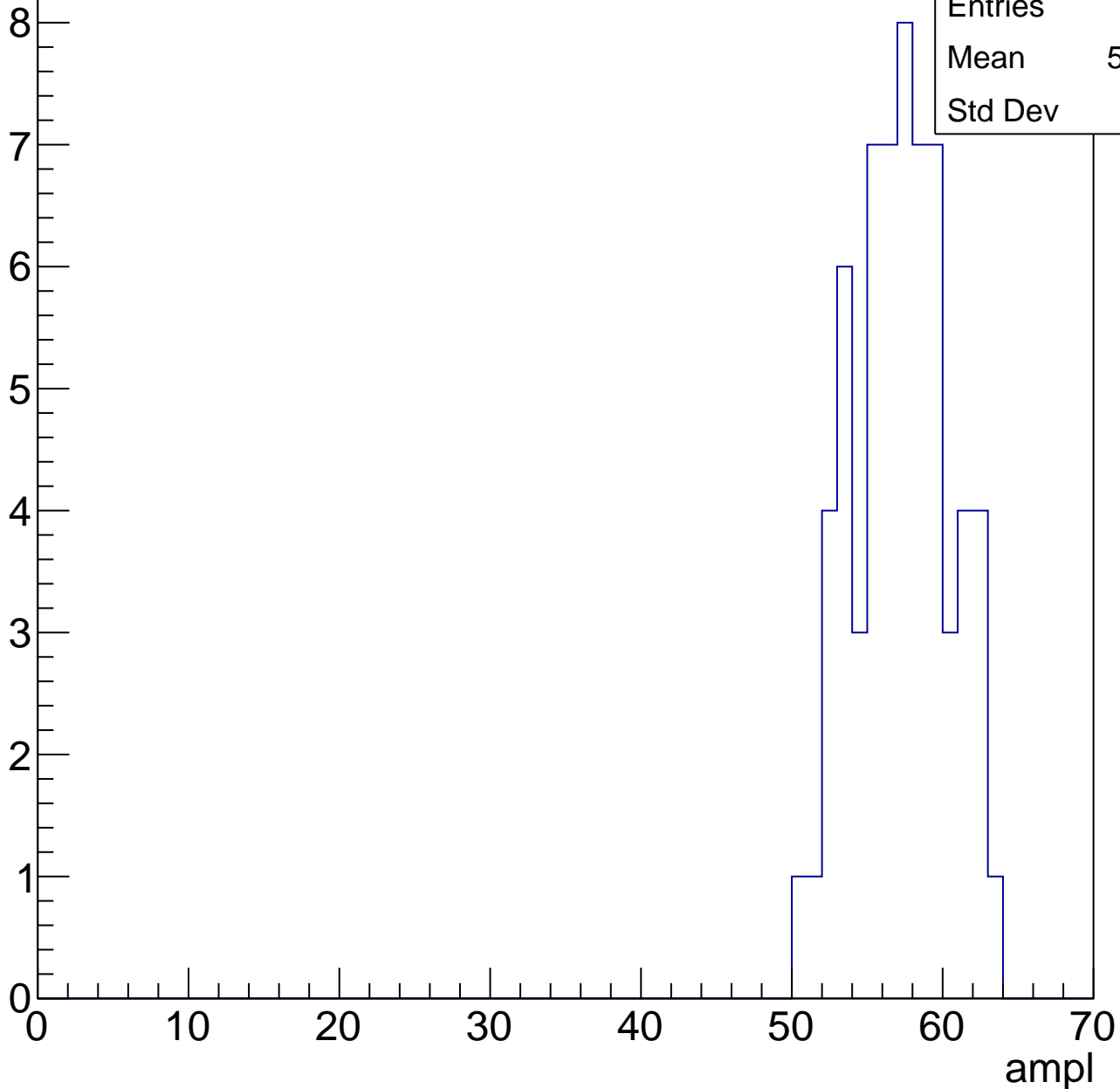


# B0L001S, U24-ch105, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	56.76
Std Dev	3.09

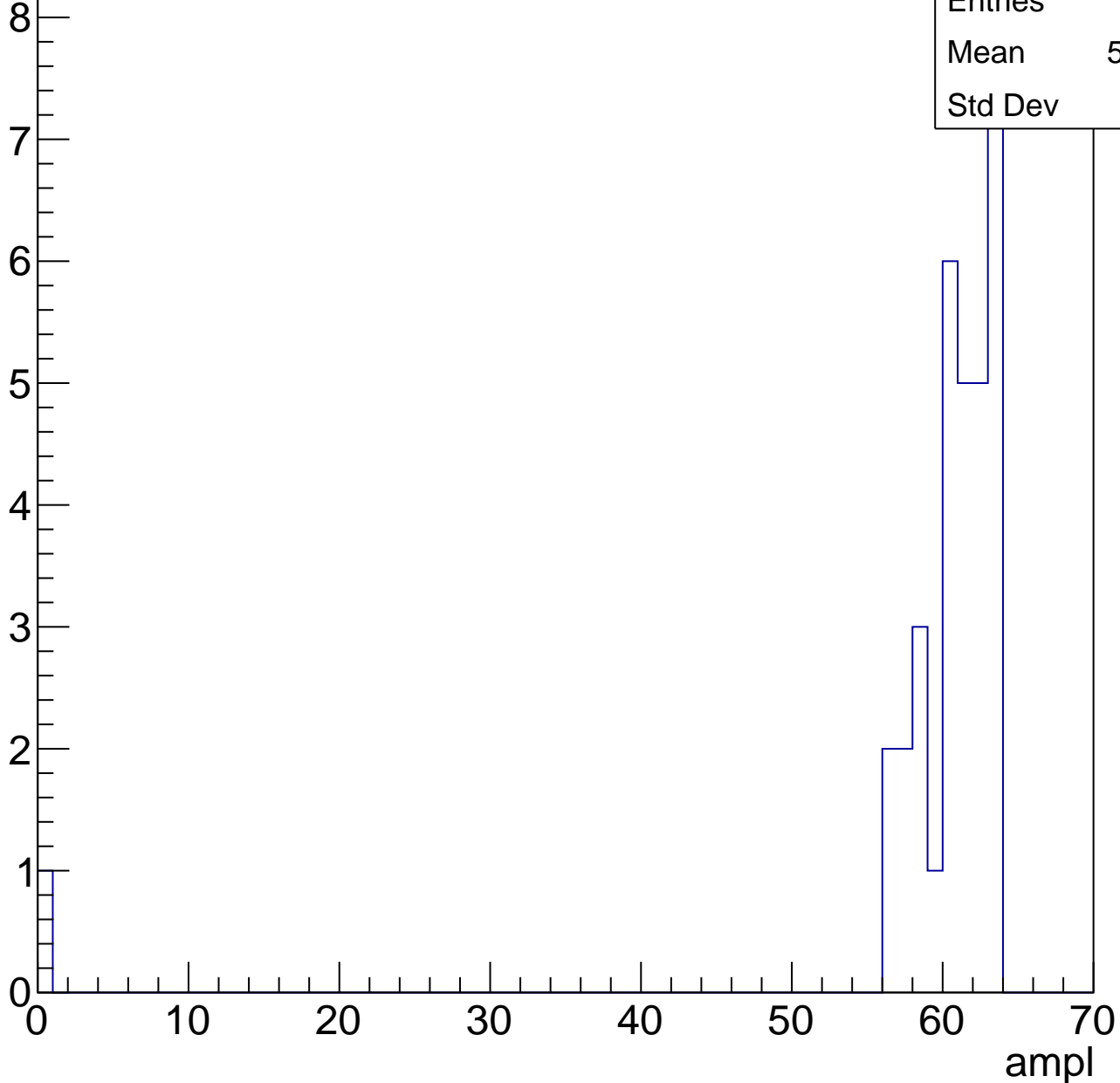


# B0L001S, U24-ch105, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

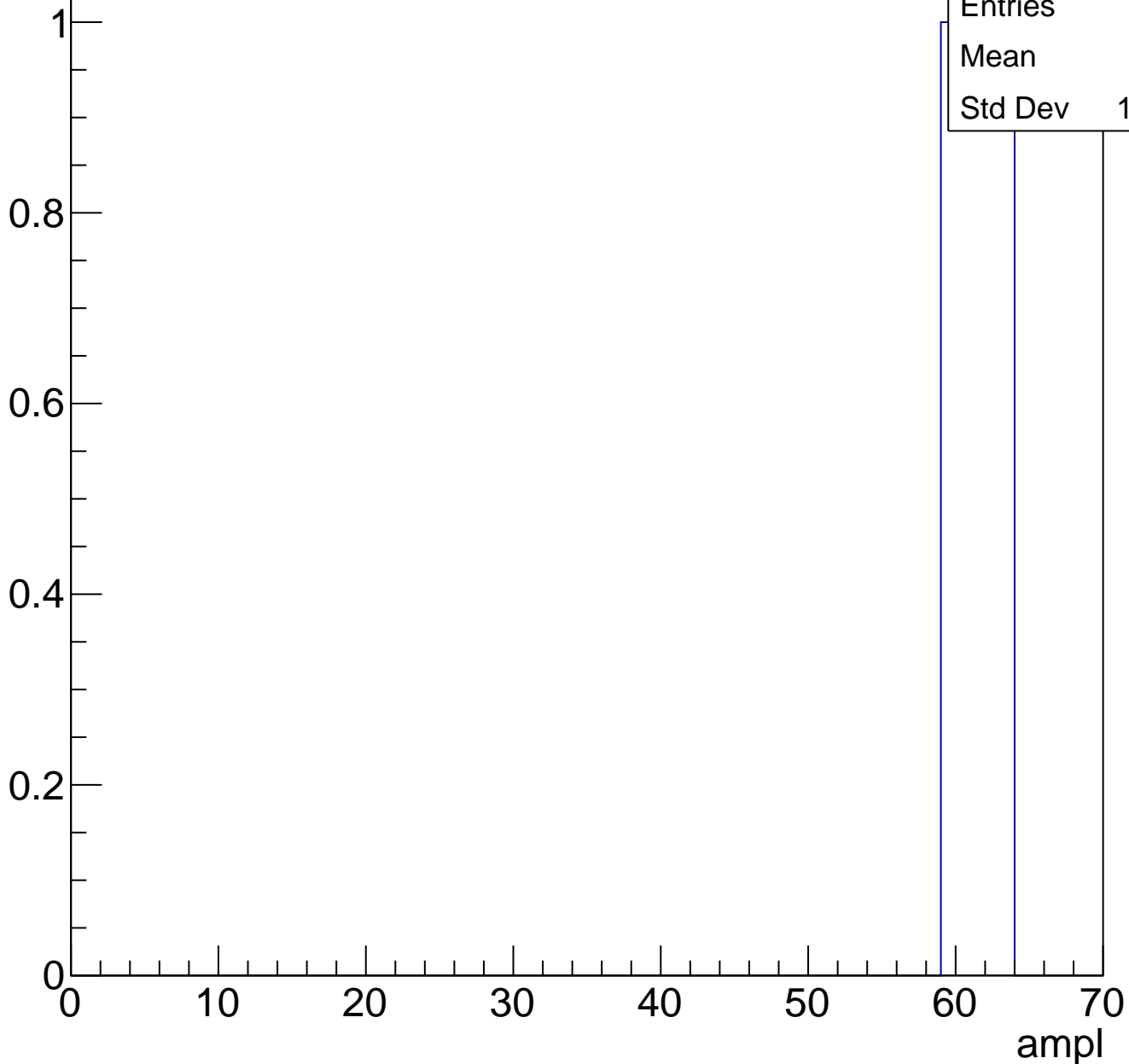
Entries	33
Mean	58.73
Std Dev	10.6



# B0L001S, U24-ch105, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch105, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U24-ch106, adc0

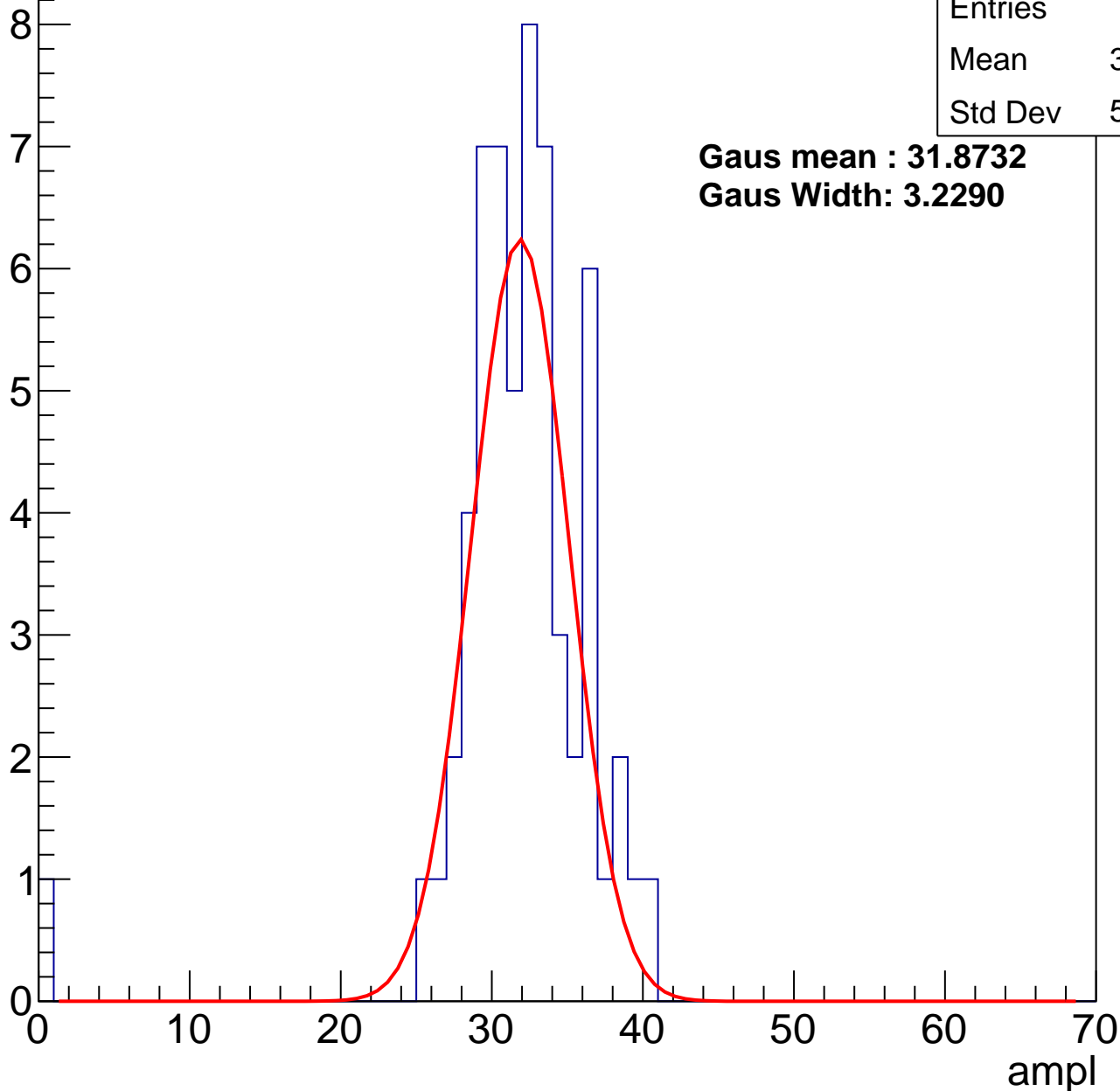
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	31.39
Std Dev	5.272

**Gaus mean : 31.8732**

**Gaus Width: 3.2290**



# B0L001S, U24-ch106, adc1

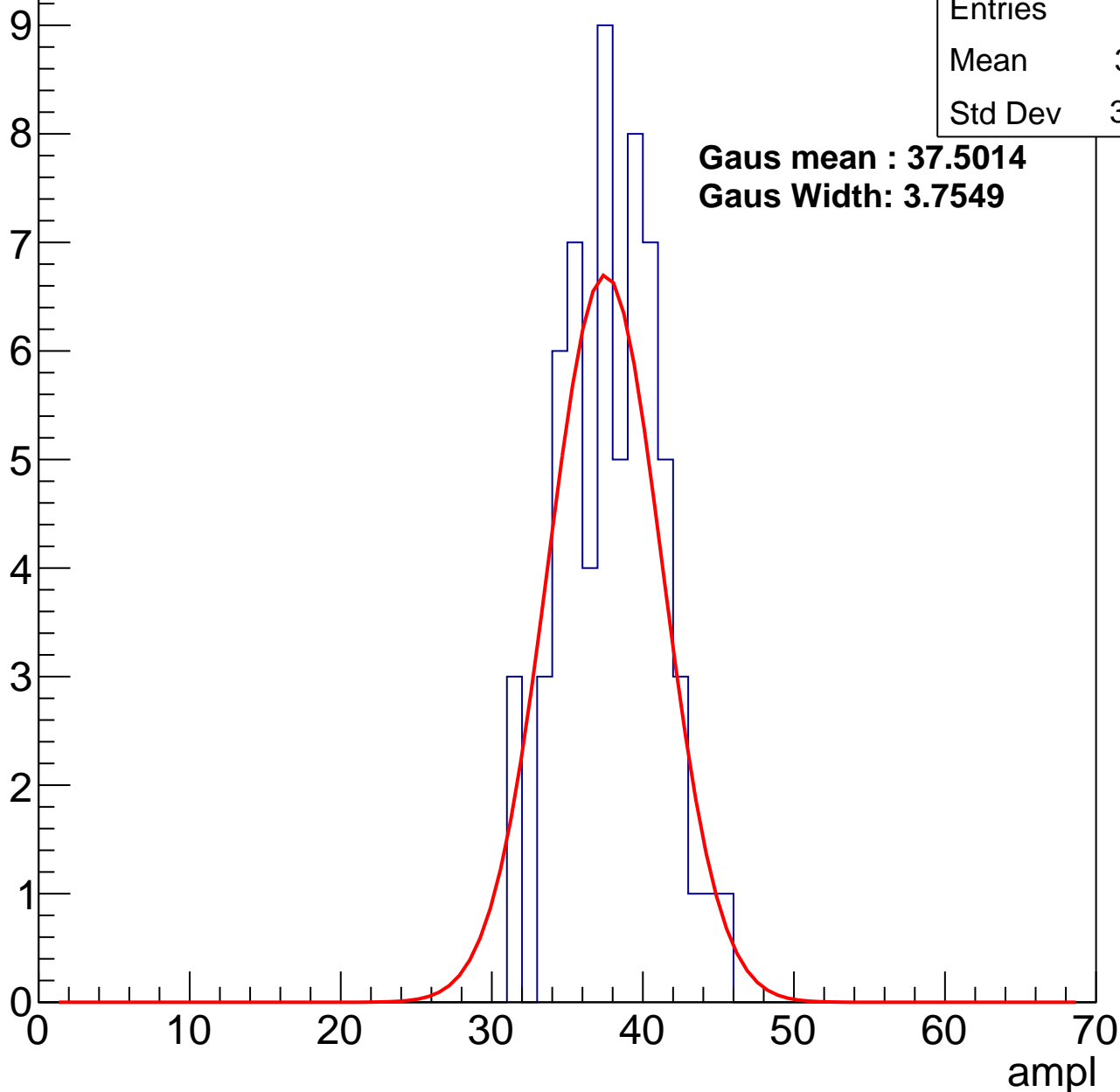
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	37.51
Std Dev	3.162

**Gaus mean : 37.5014**

**Gaus Width: 3.7549**



# B0L001S, U24-ch106, adc2

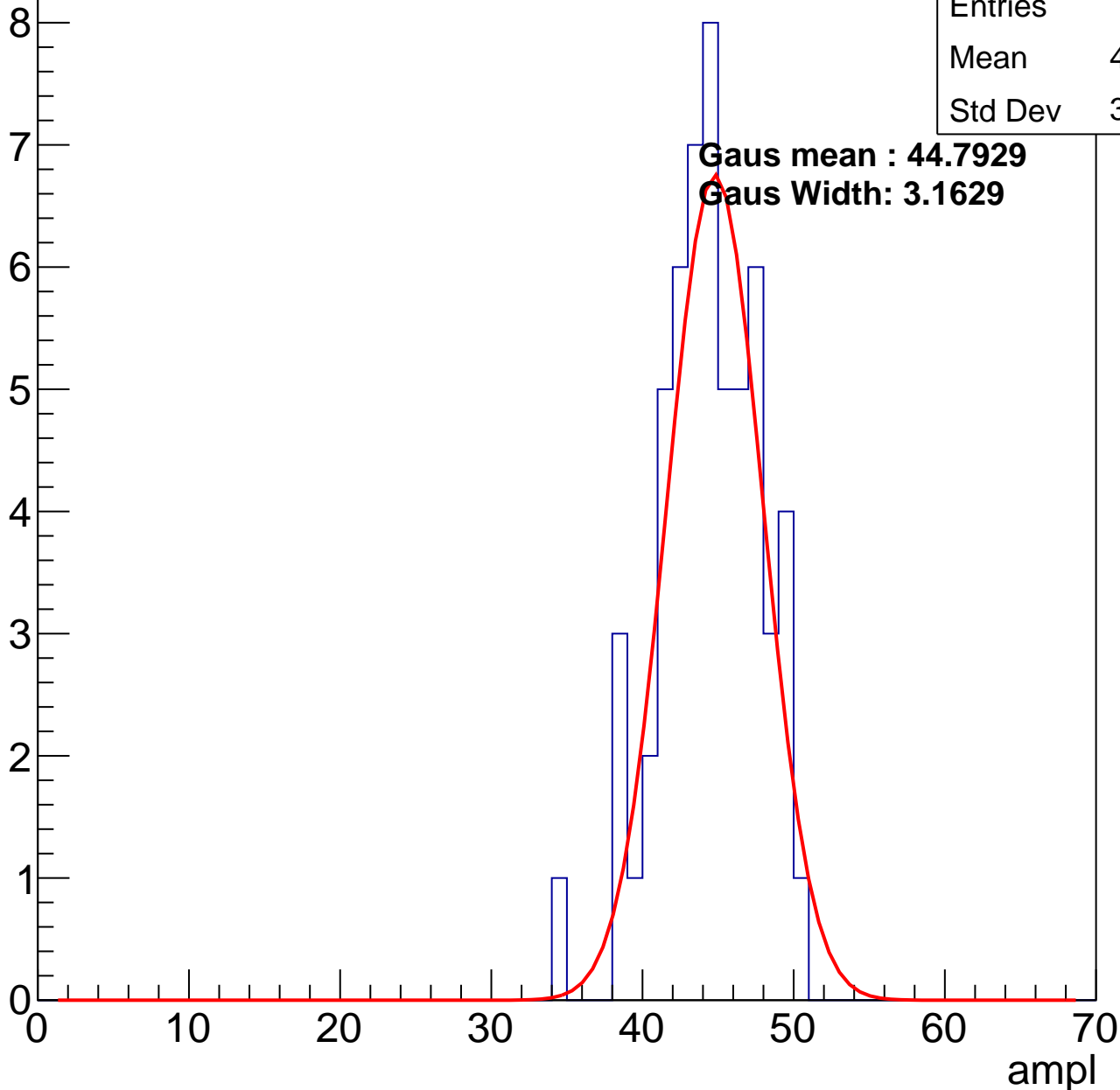
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	43.93
Std Dev	3.254

**Gaus mean : 44.7929**

**Gaus Width: 3.1629**

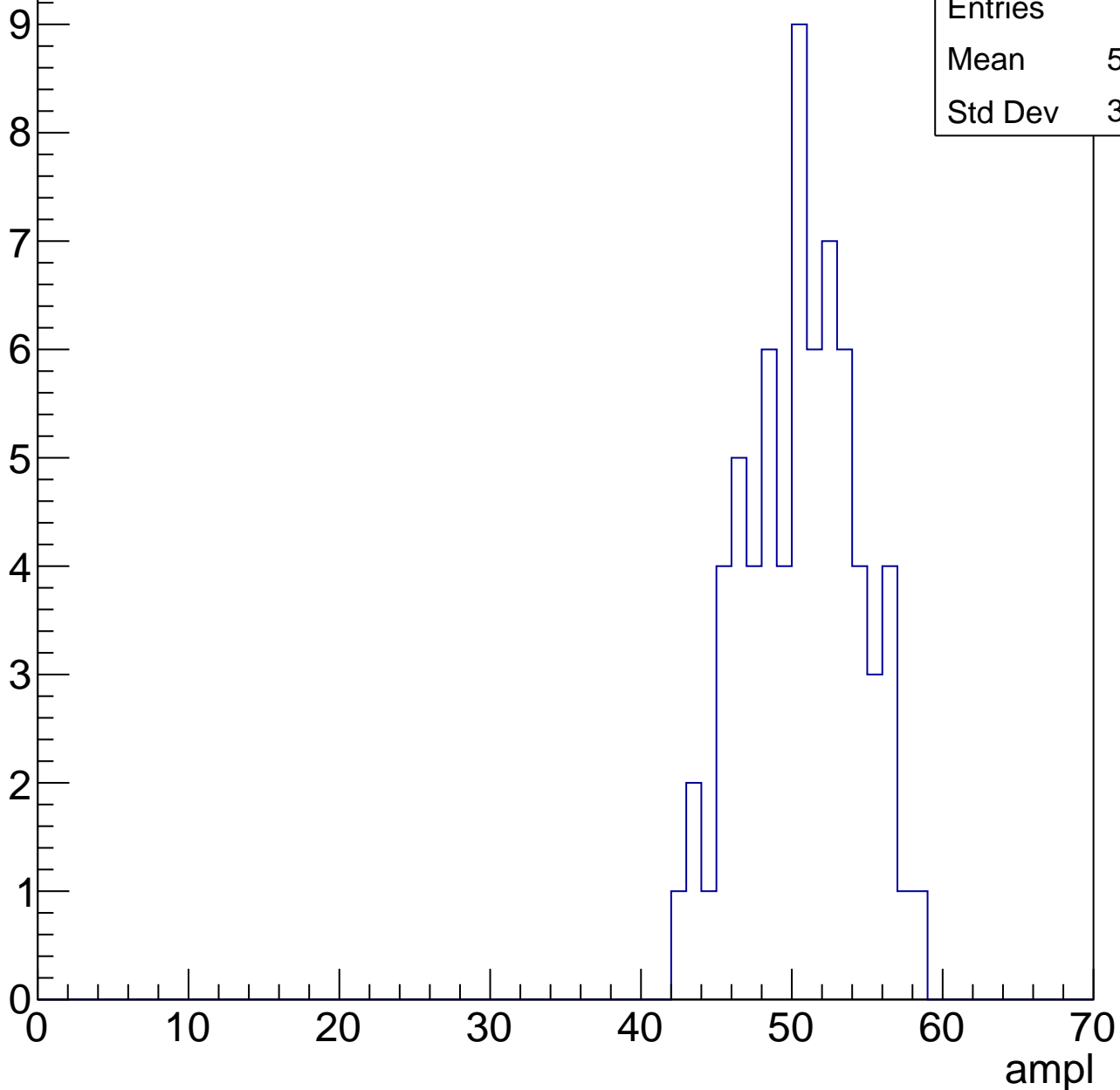


# B0L001S, U24-ch106, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	50.18
Std Dev	3.686

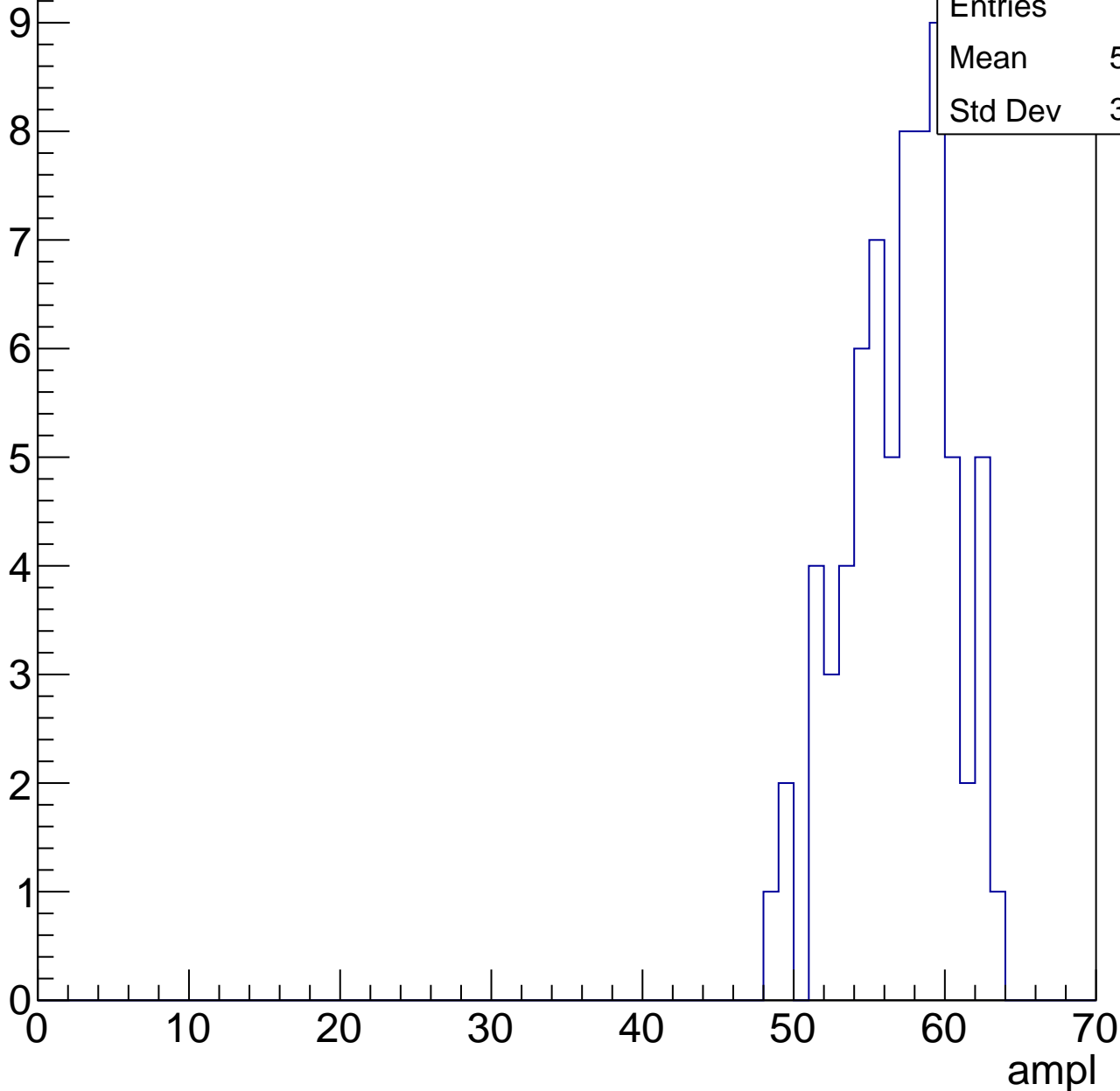


# B0L001S, U24-ch106, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	56.47
Std Dev	3.467

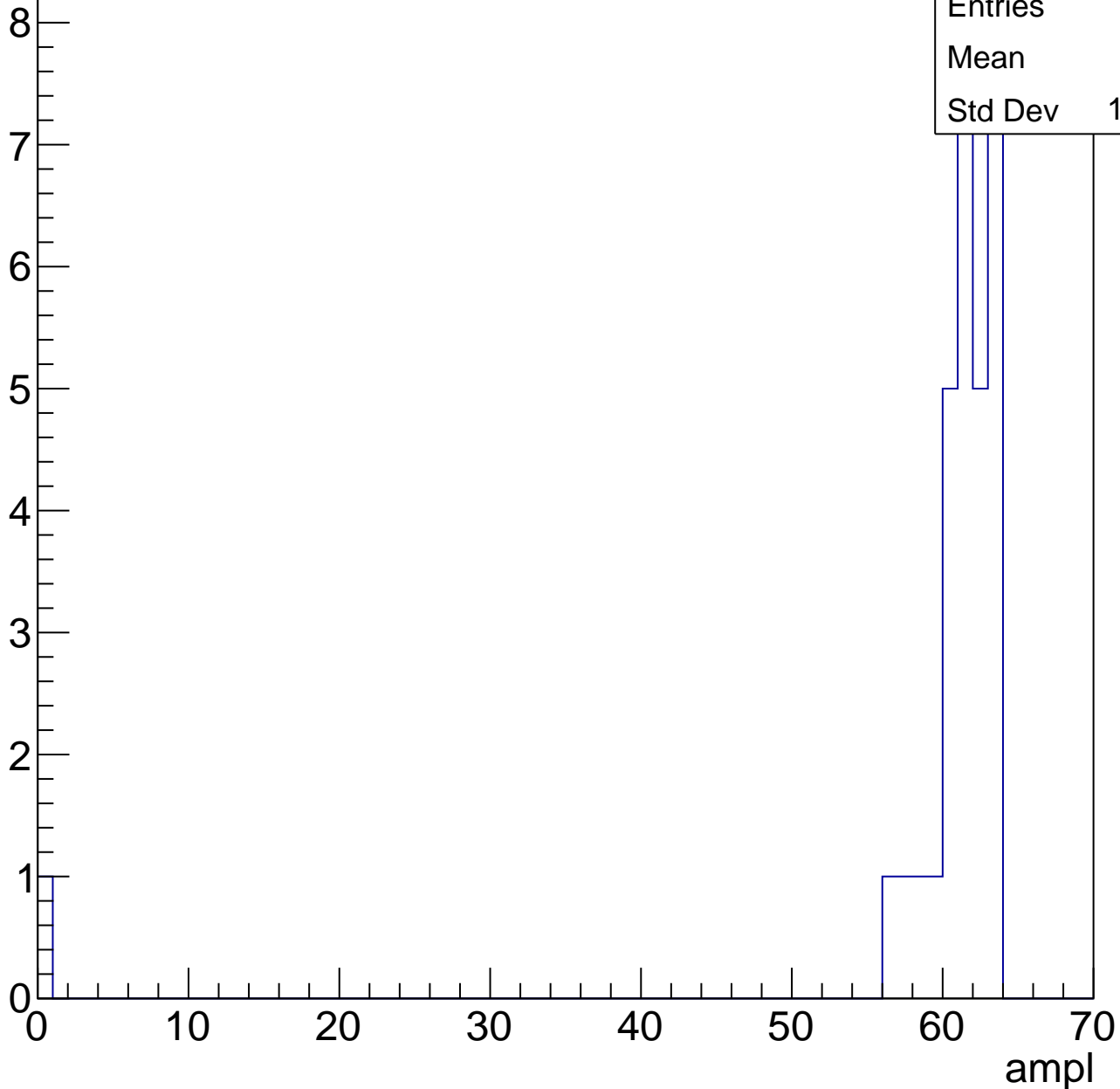


# B0L001S, U24-ch106, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	31
Mean	59.1
Std Dev	10.93



# B0L001S, U24-ch106, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch106, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U24-ch107, adc0

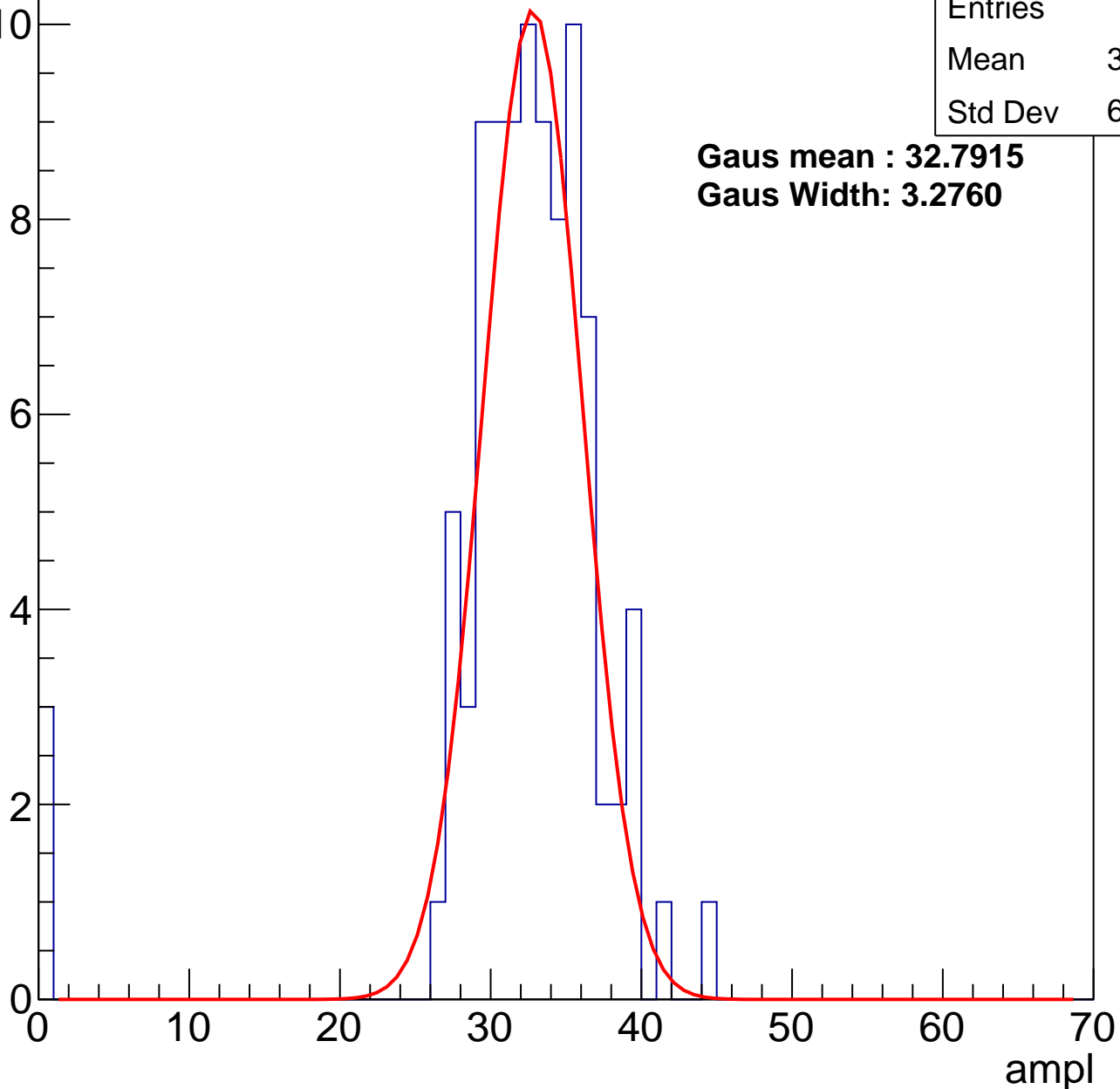
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	93
Mean	31.58
Std Dev	6.702

**Gaus mean : 32.7915**

**Gaus Width: 3.2760**

Entry



# B0L001S, U24-ch107, adc1

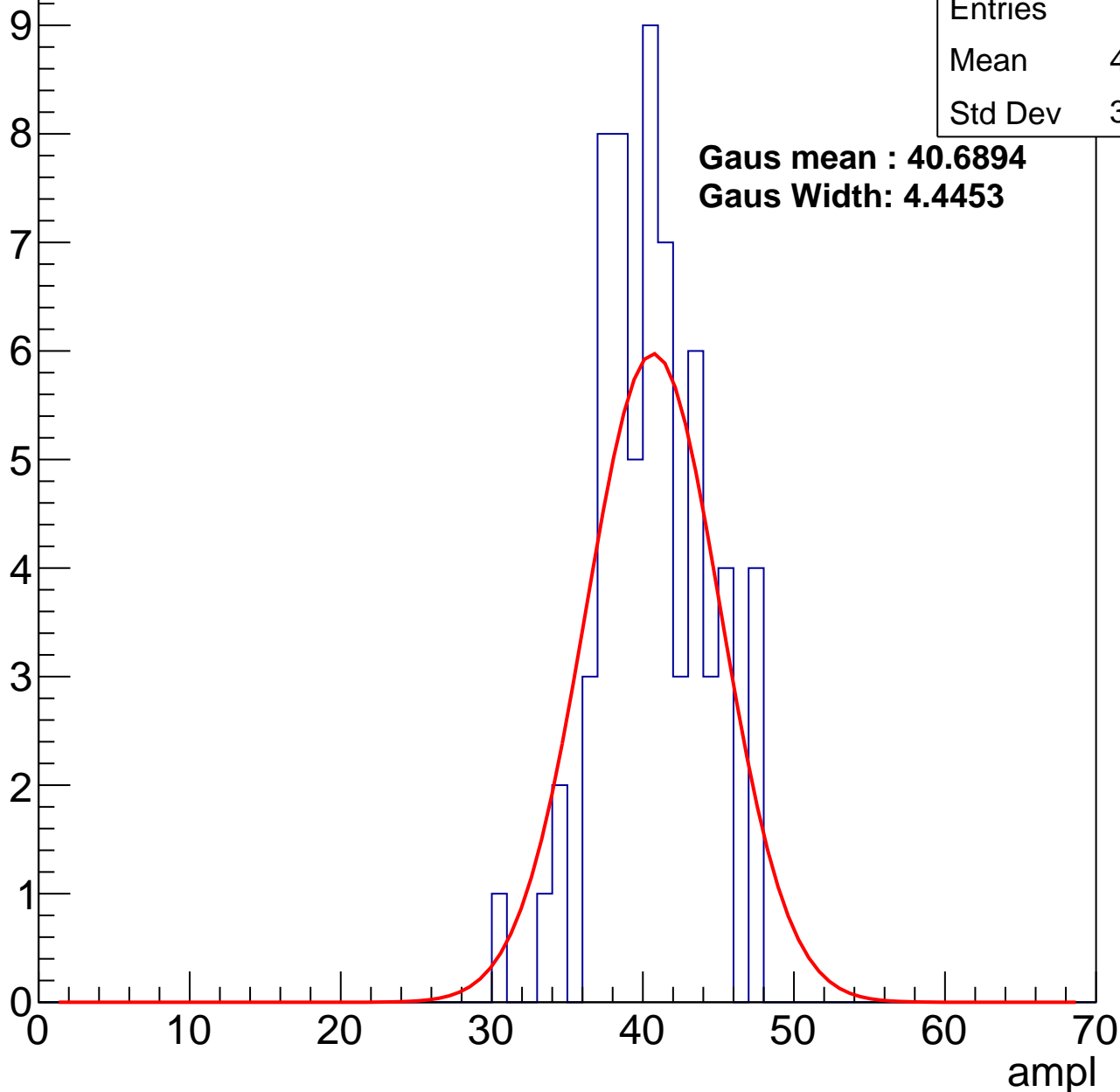
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	40.08
Std Dev	3.524

**Gaus mean : 40.6894**

**Gaus Width: 4.4453**



# B0L001S, U24-ch107, adc2

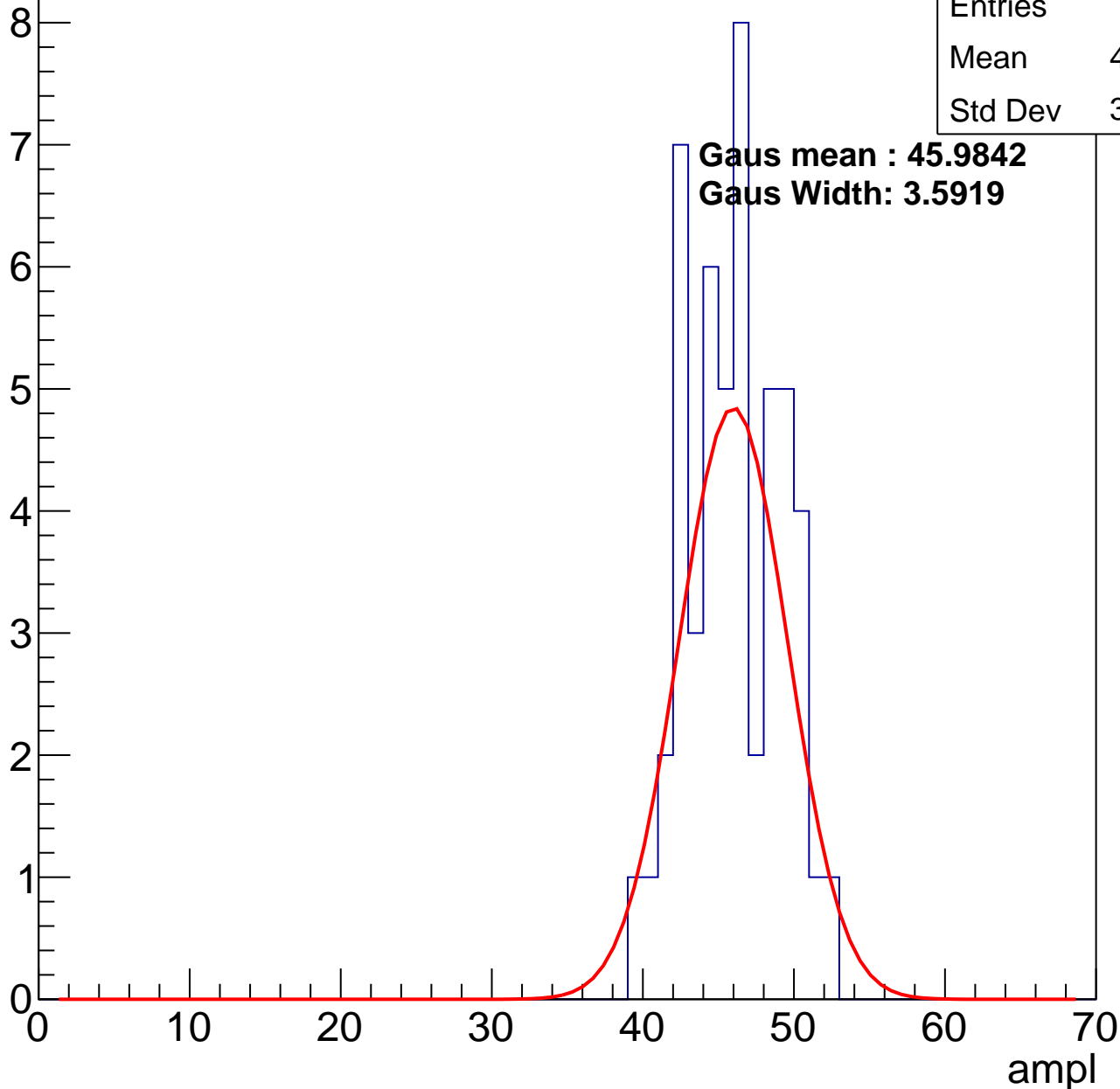
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	51
Mean	45.55
Std Dev	3.083

**Gaus mean : 45.9842**

**Gaus Width: 3.5919**

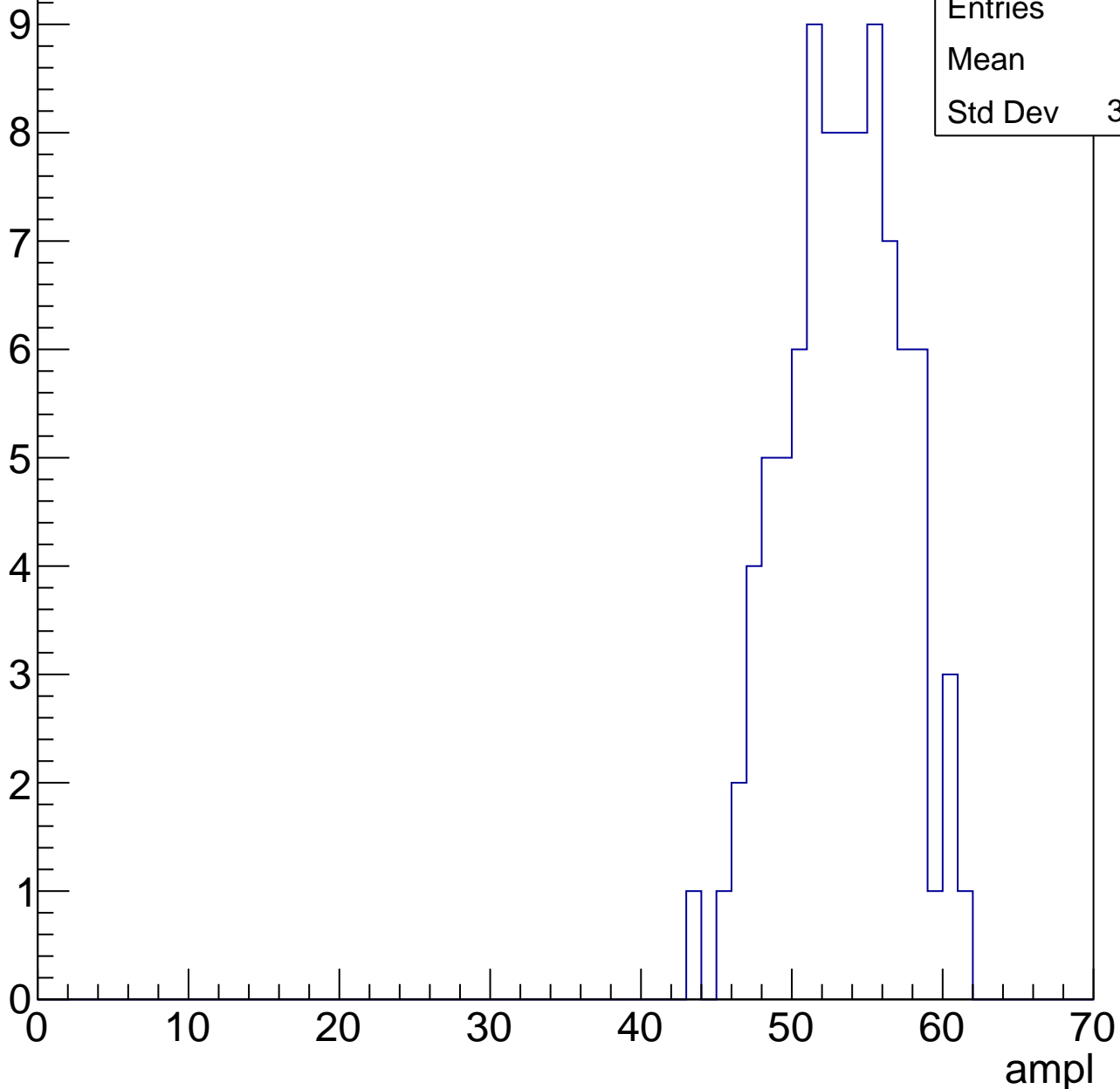


# B0L001S, U24-ch107, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	90
Mean	52.9
Std Dev	3.812

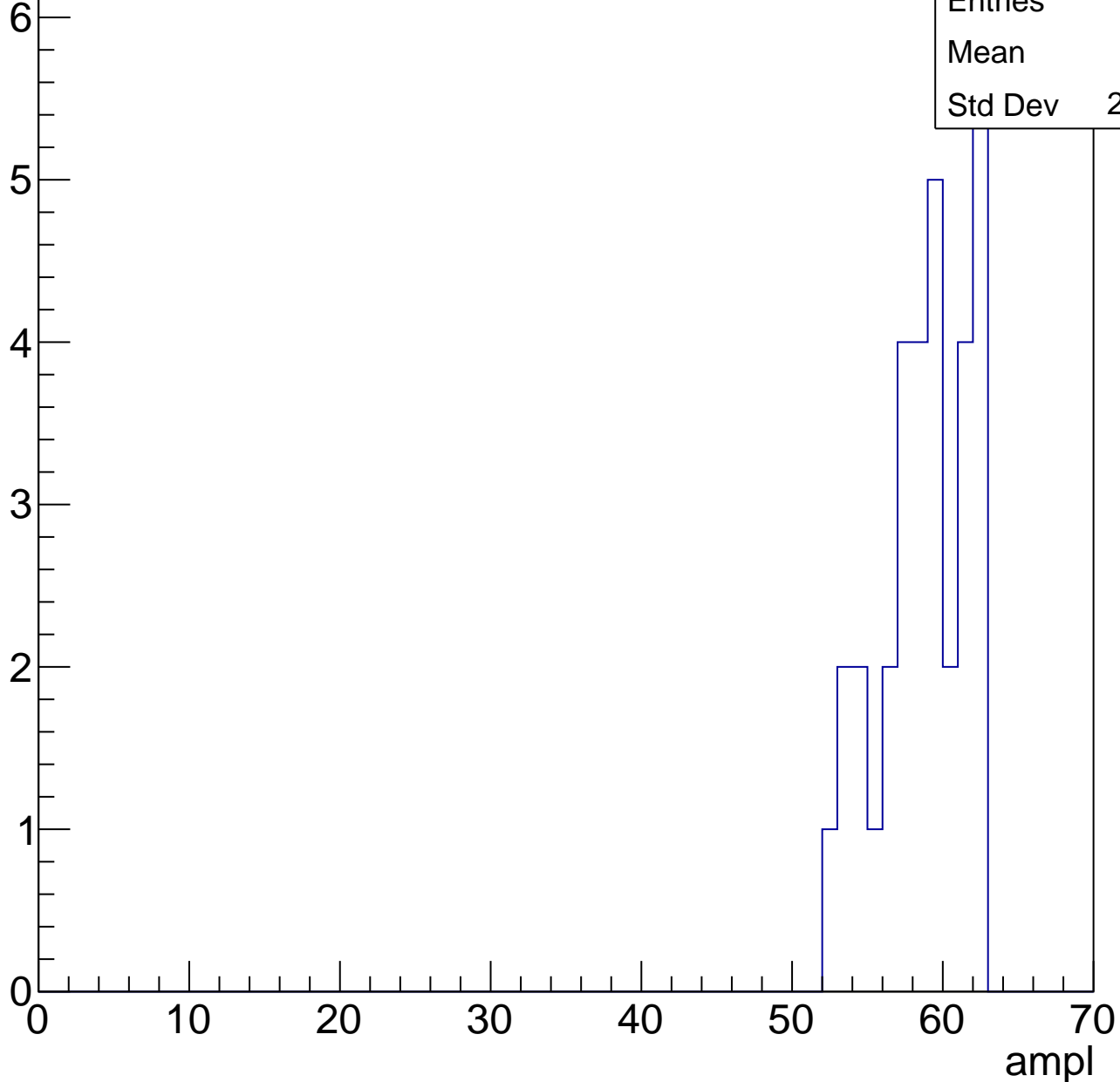


# B0L001S, U24-ch107, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	33
Mean	58.3
Std Dev	2.918

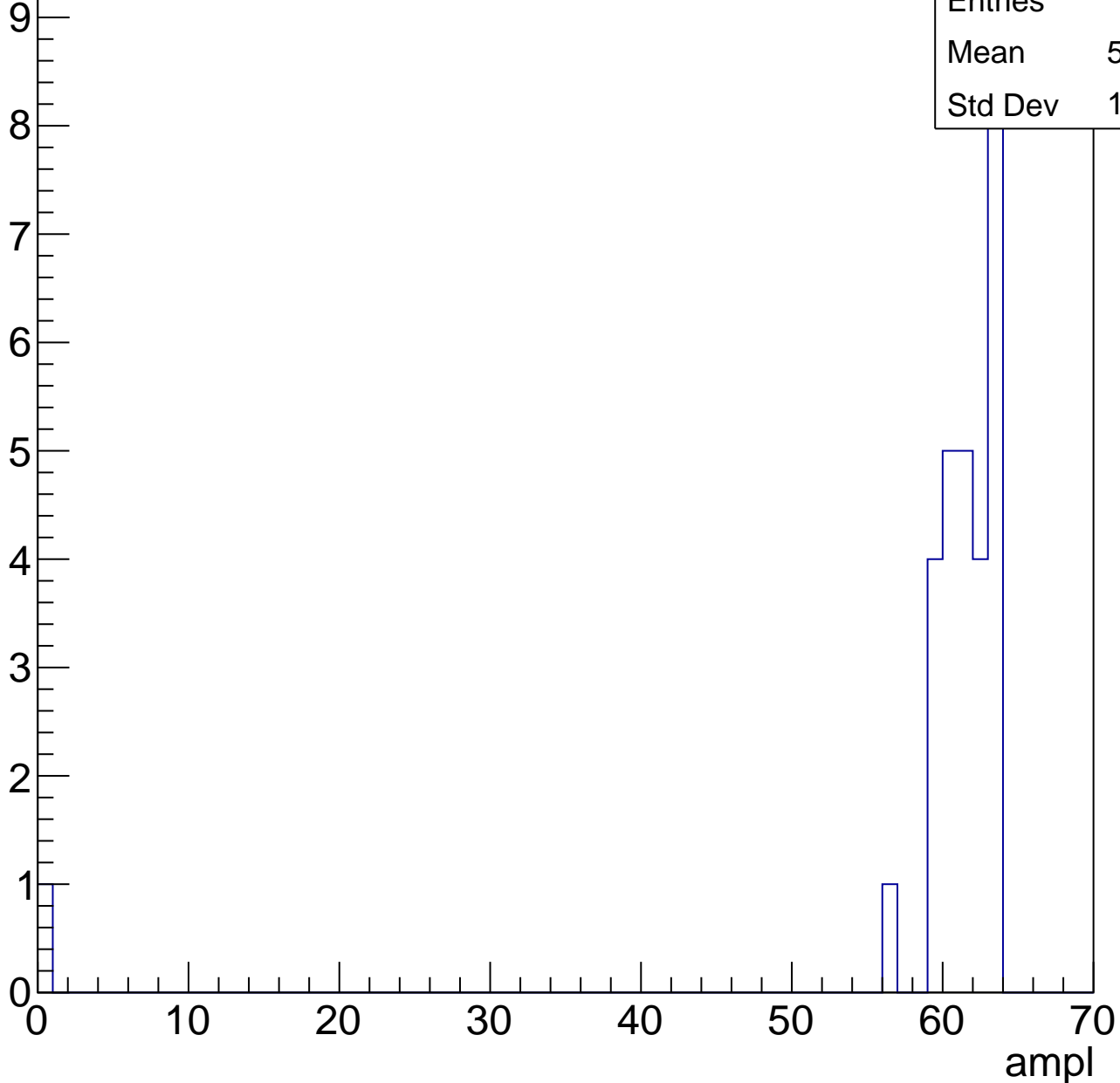


# B0L001S, U24-ch107, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	29
Mean	59.03
Std Dev	11.29



# B0L001S, U24-ch107, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch107, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U24-ch108, adc0

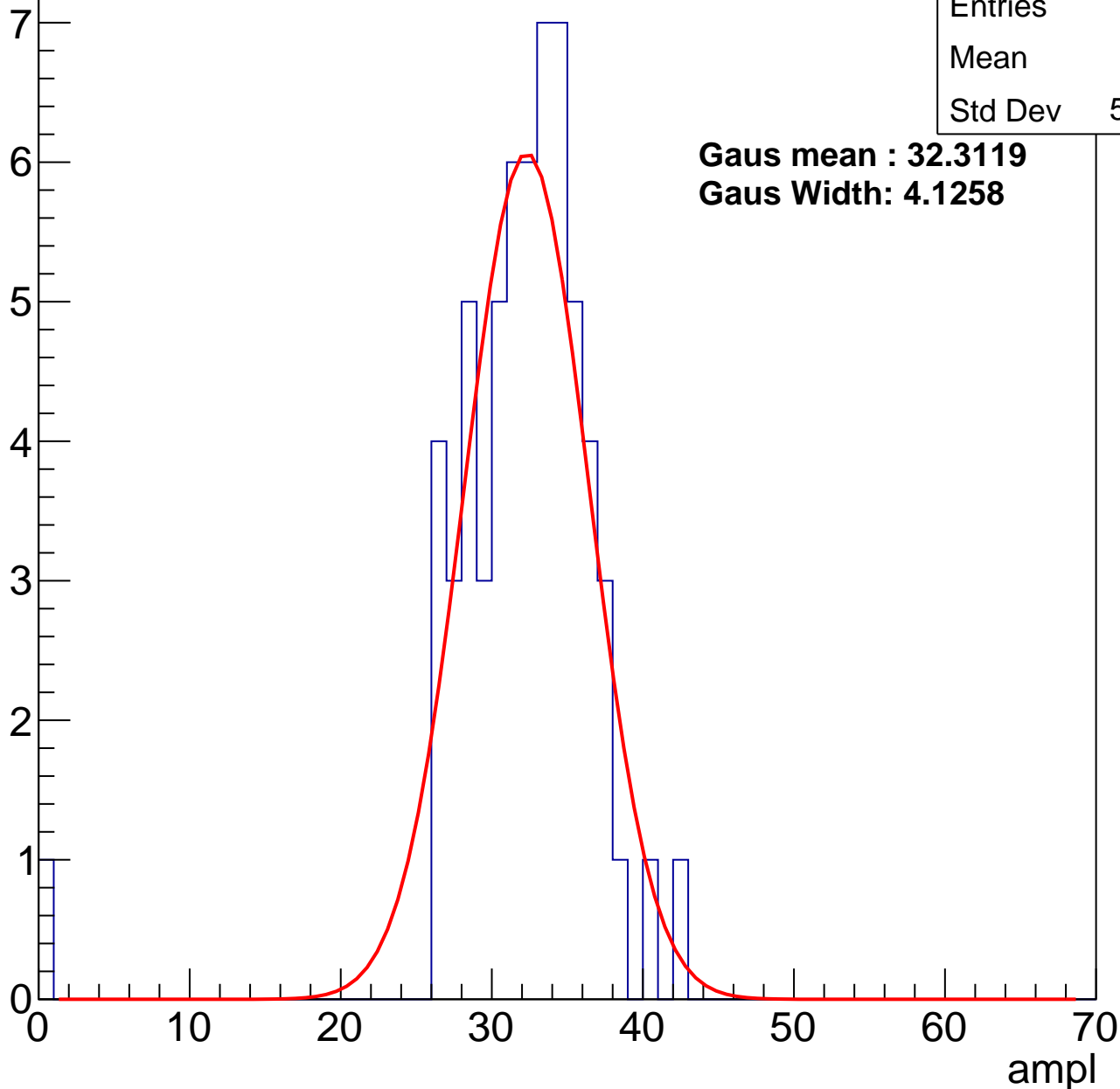
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	31.6
Std Dev	5.366

**Gaus mean : 32.3119**

**Gaus Width: 4.1258**



# B0L001S, U24-ch108, adc1

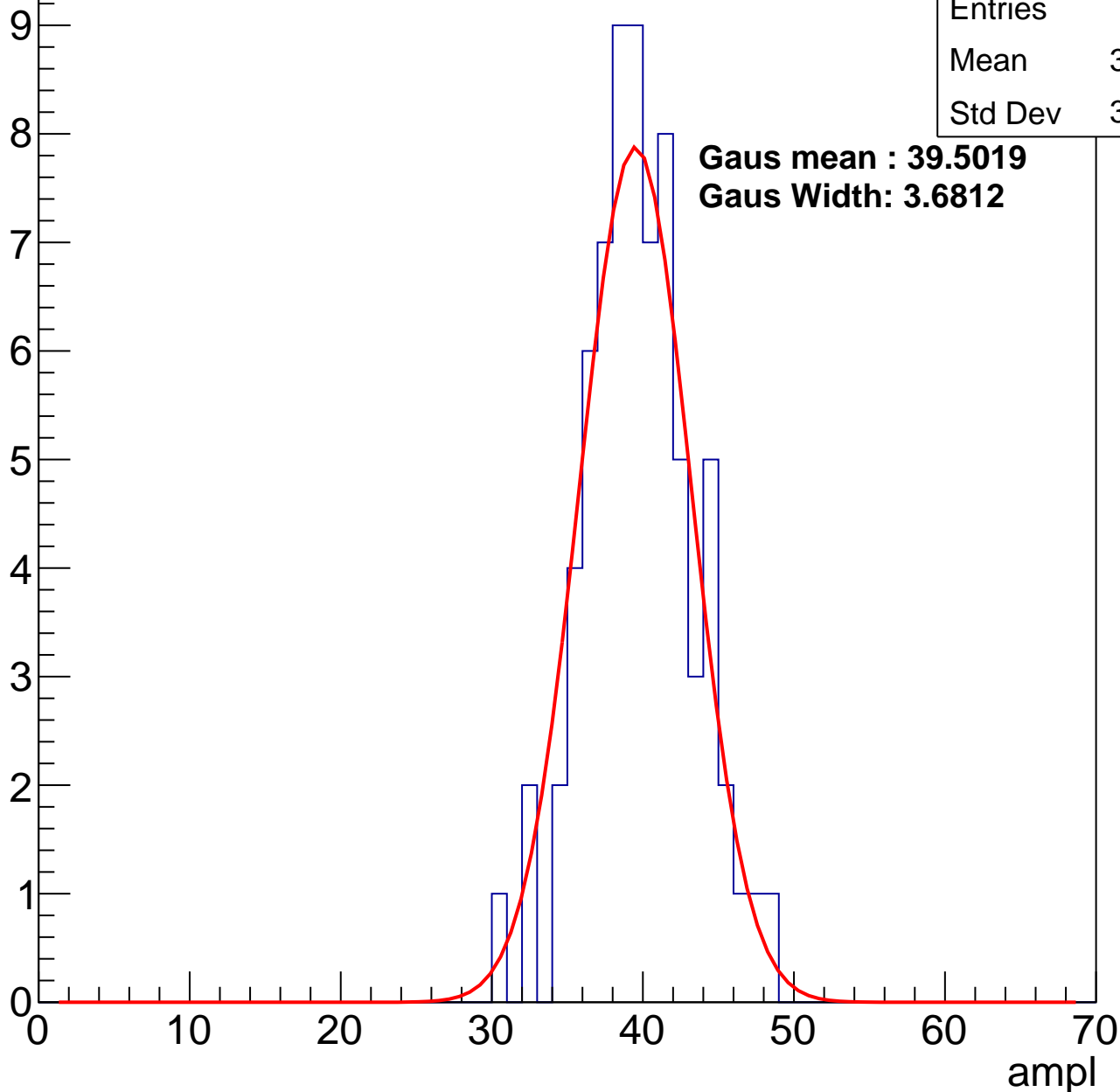
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	39.29
Std Dev	3.513

**Gaus mean : 39.5019**

**Gaus Width: 3.6812**



# B0L001S, U24-ch108, adc2

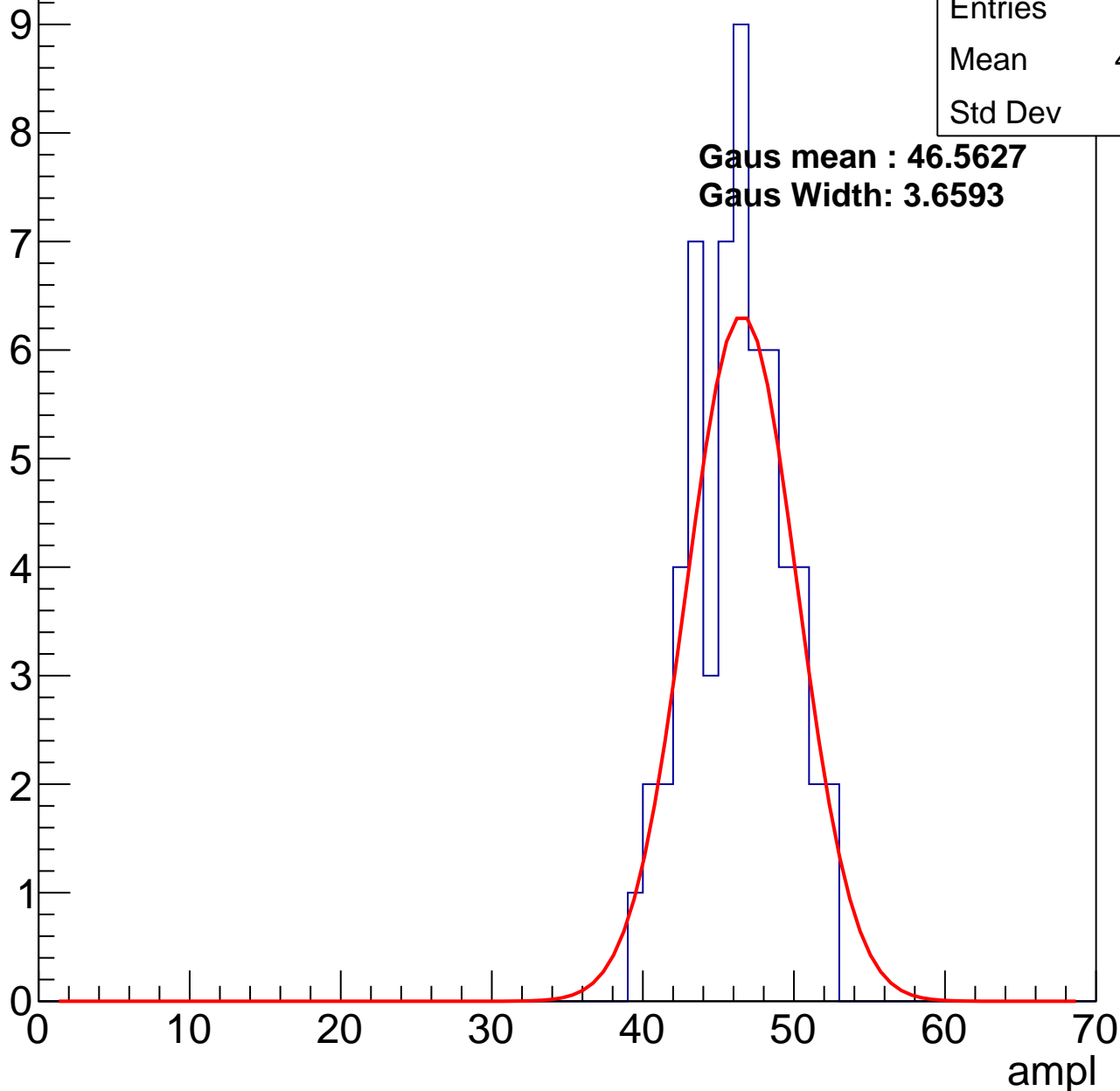
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	45.81
Std Dev	3.1

**Gaus mean : 46.5627**

**Gaus Width: 3.6593**

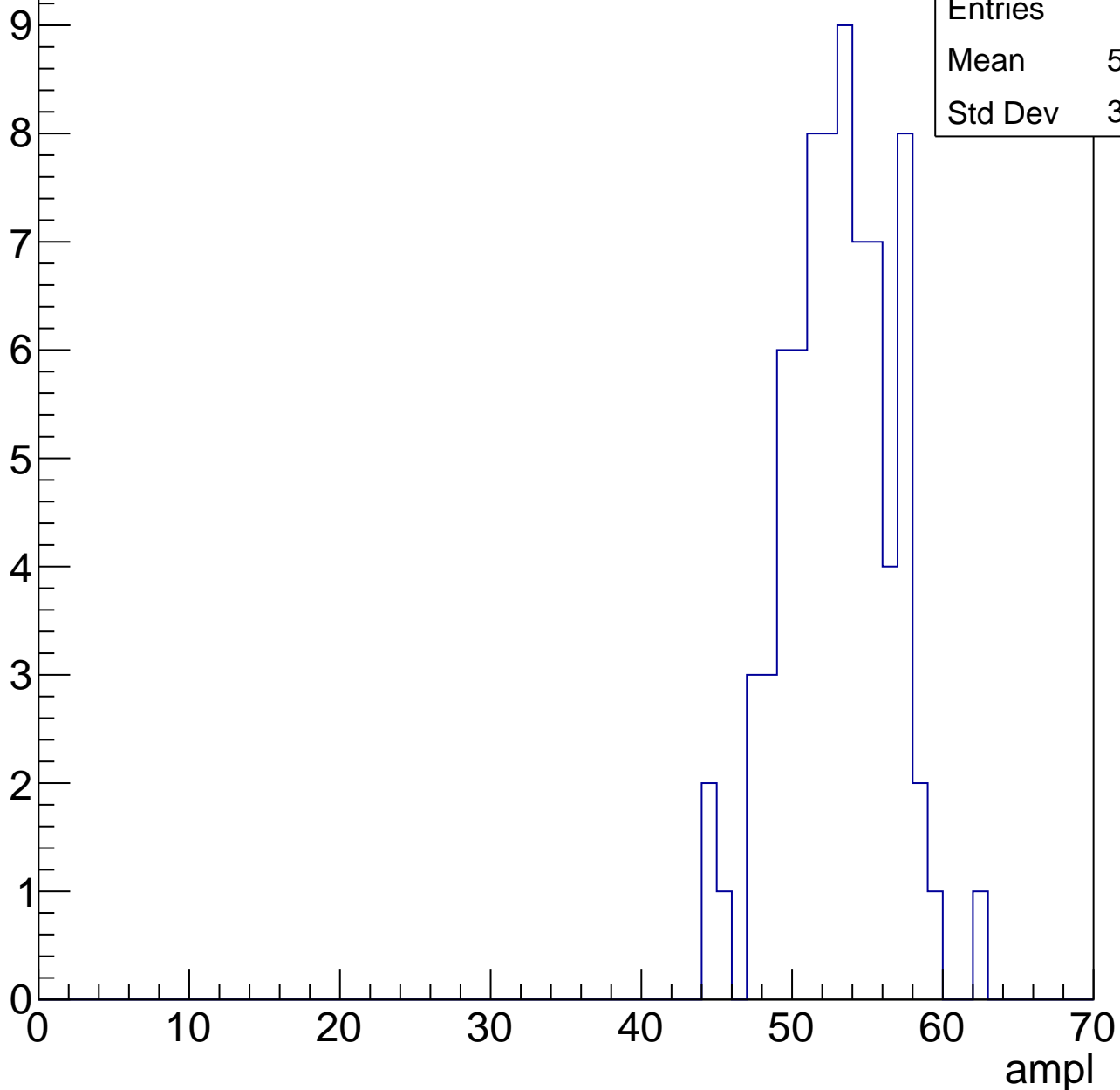


# B0L001S, U24-ch108, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	76
Mean	52.54
Std Dev	3.533

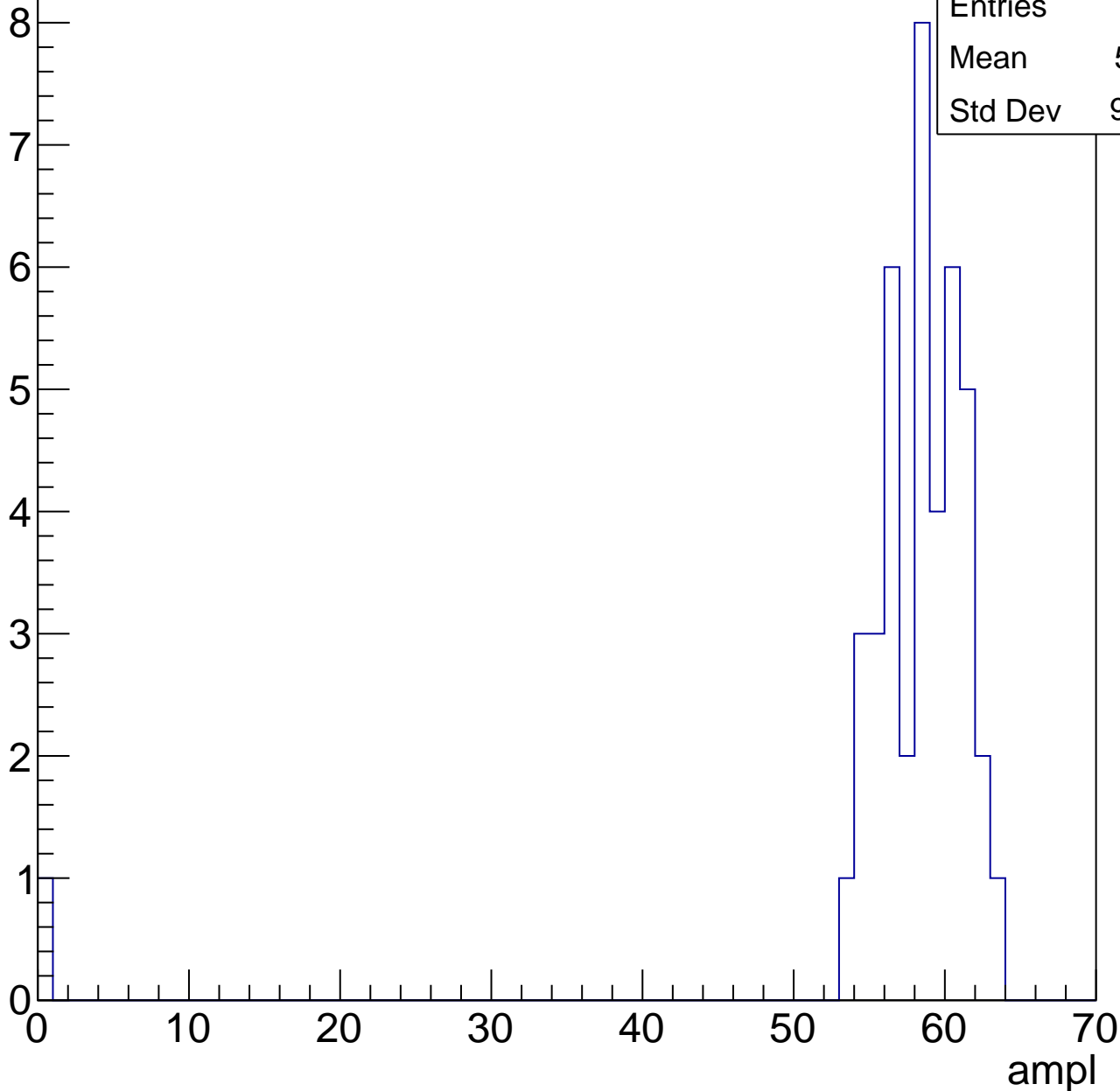


# B0L001S, U24-ch108, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	42
Mean	56.71
Std Dev	9.194

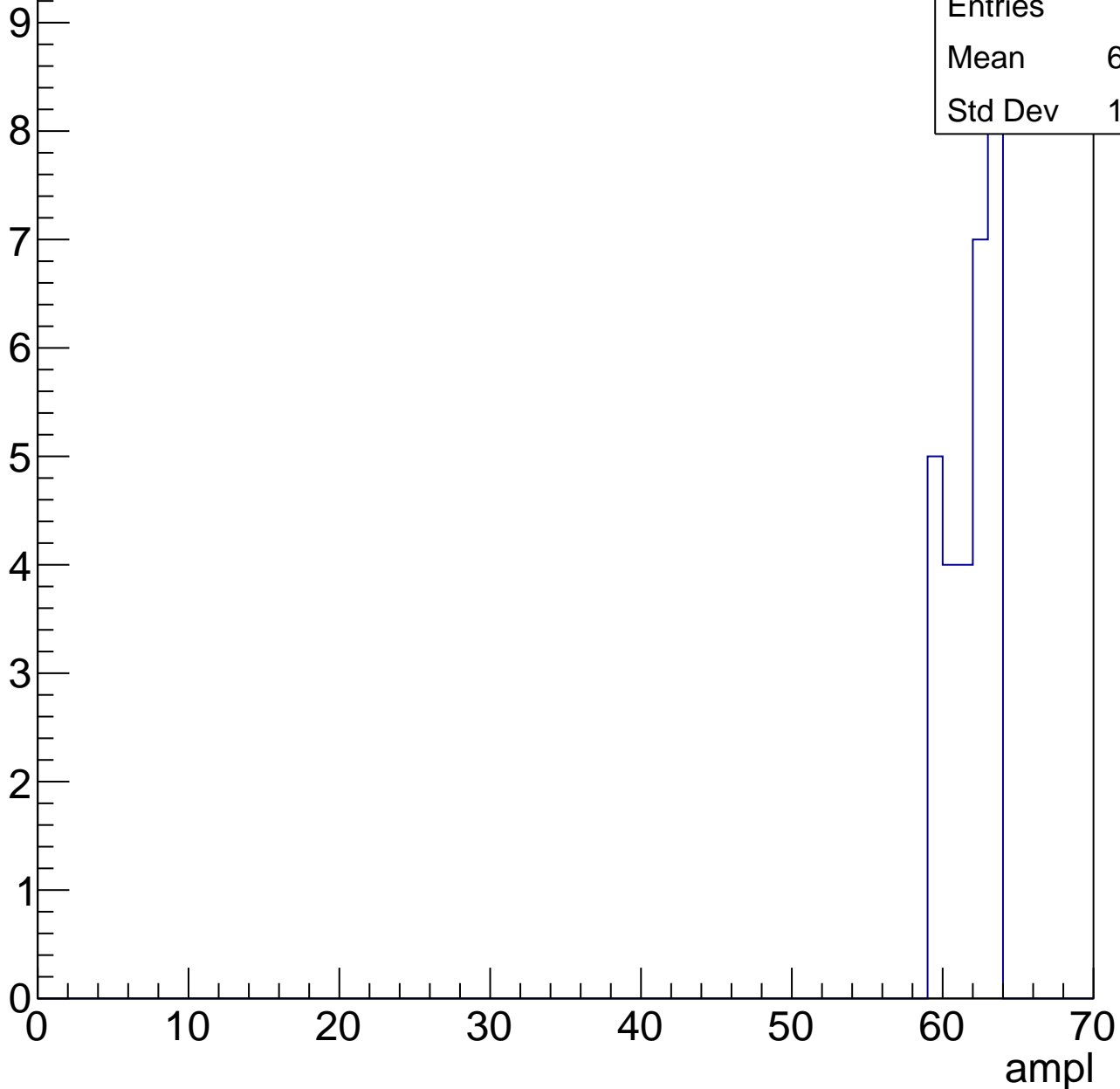


# B0L001S, U24-ch108, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

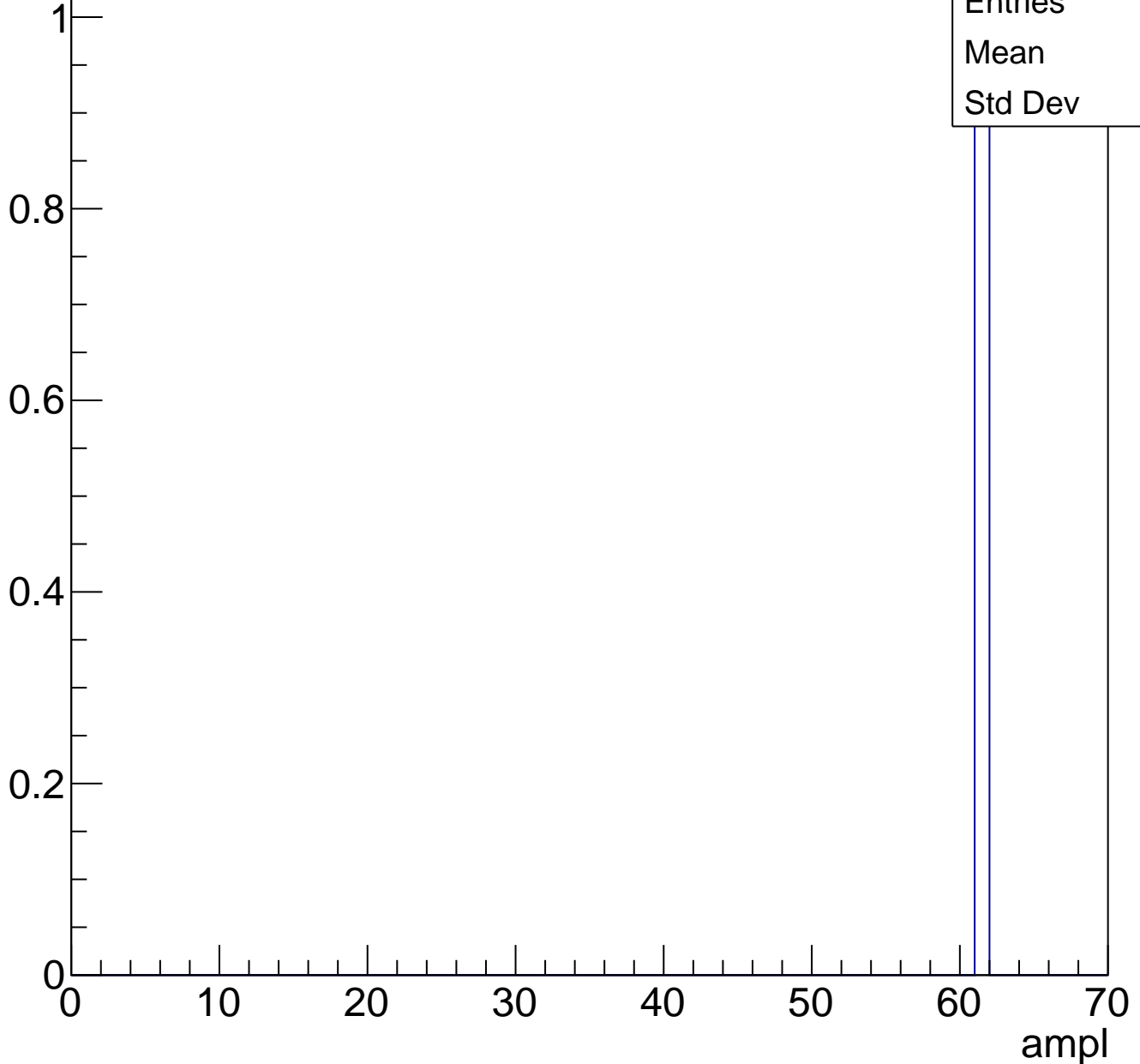
Entries	29
Mean	61.38
Std Dev	1.472



# B0L001S, U24-ch108, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch108, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	3
Mean	0
Std Dev	0

# B0L001S, U24-ch109, adc0

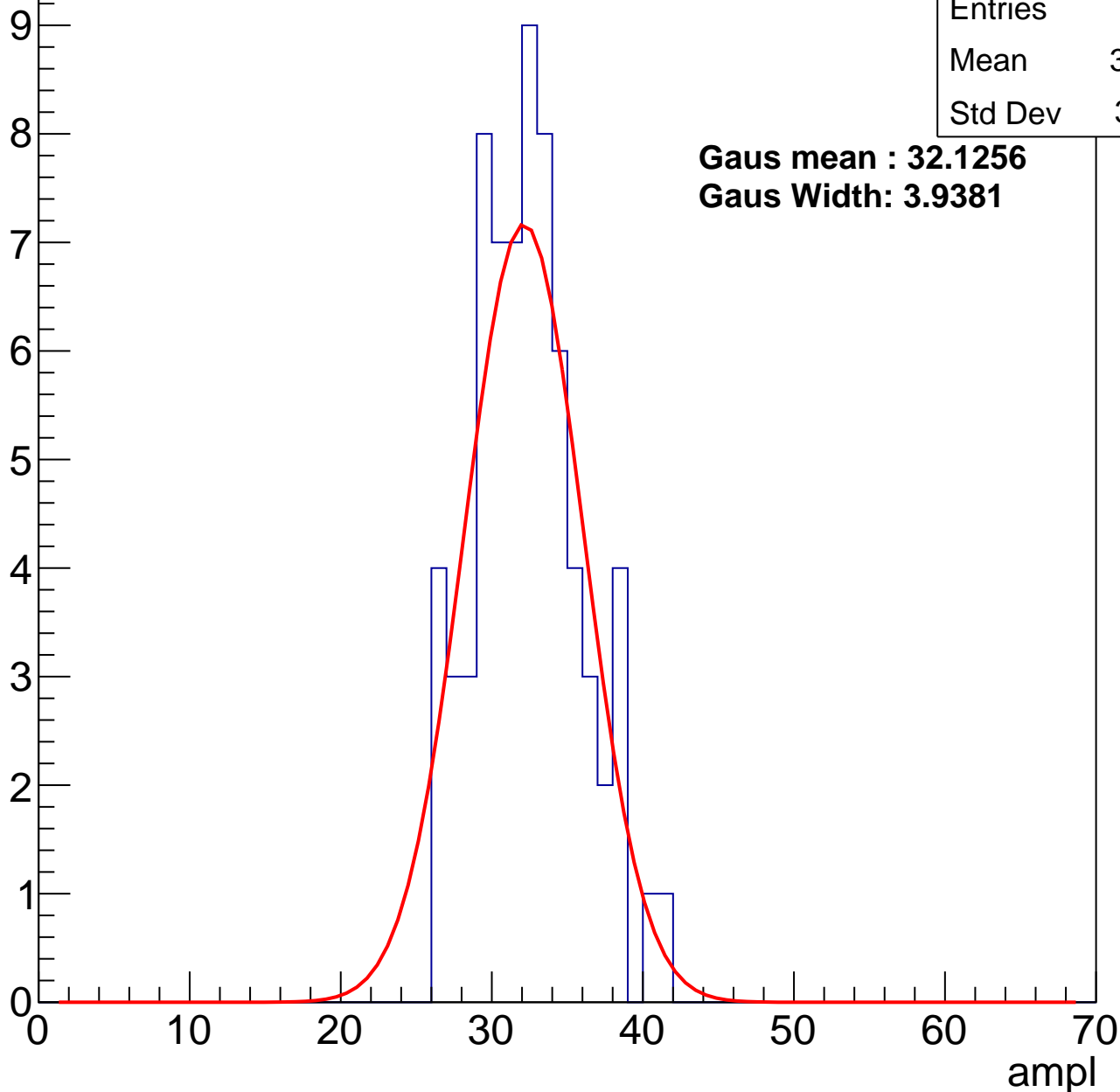
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	31.99
Std Dev	3.441

**Gaus mean : 32.1256**

**Gaus Width: 3.9381**



# B0L001S, U24-ch109, adc1

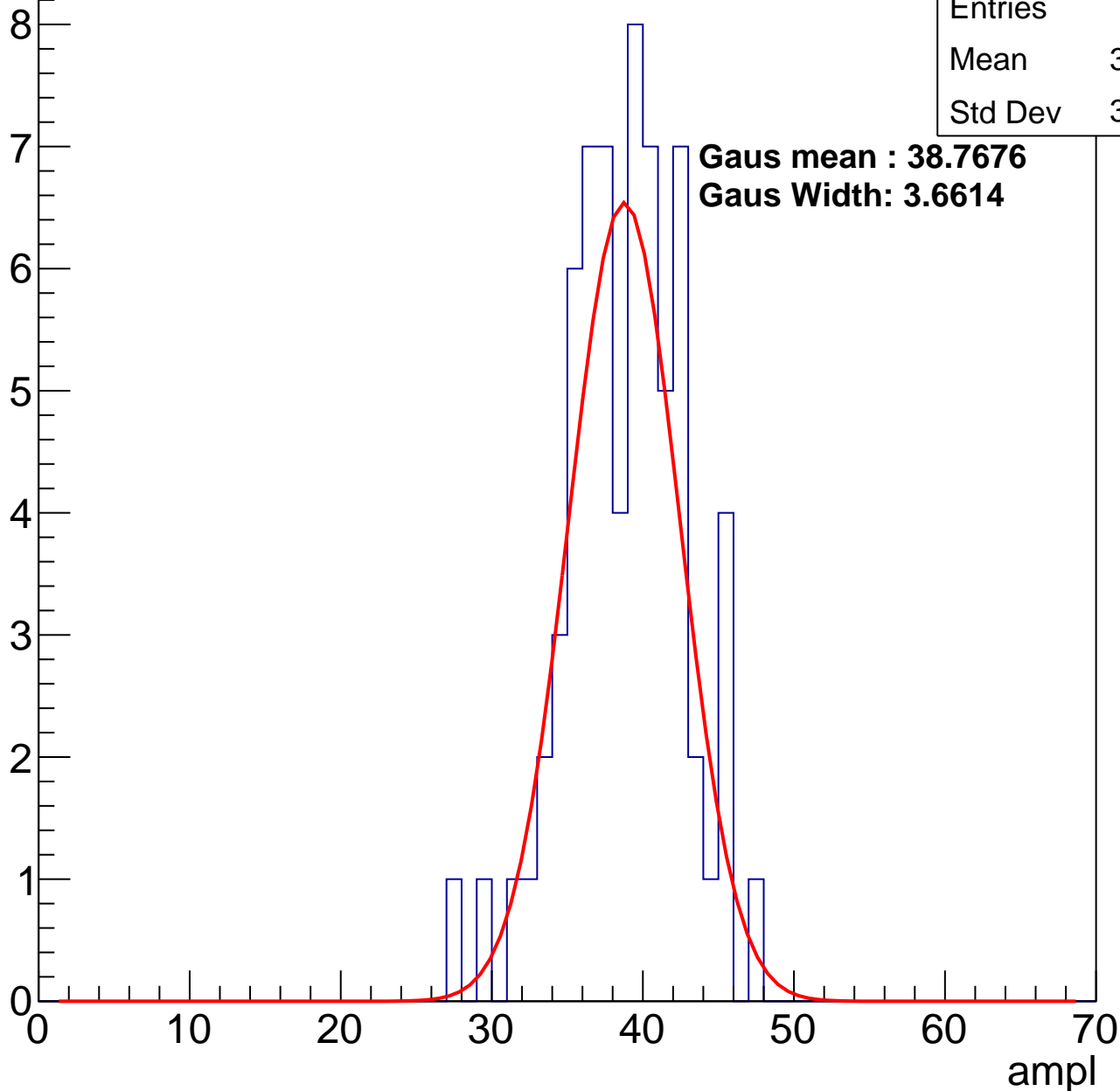
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	38.35
Std Dev	3.876

**Gaus mean : 38.7676**

**Gaus Width: 3.6614**



# B0L001S, U24-ch109, adc2

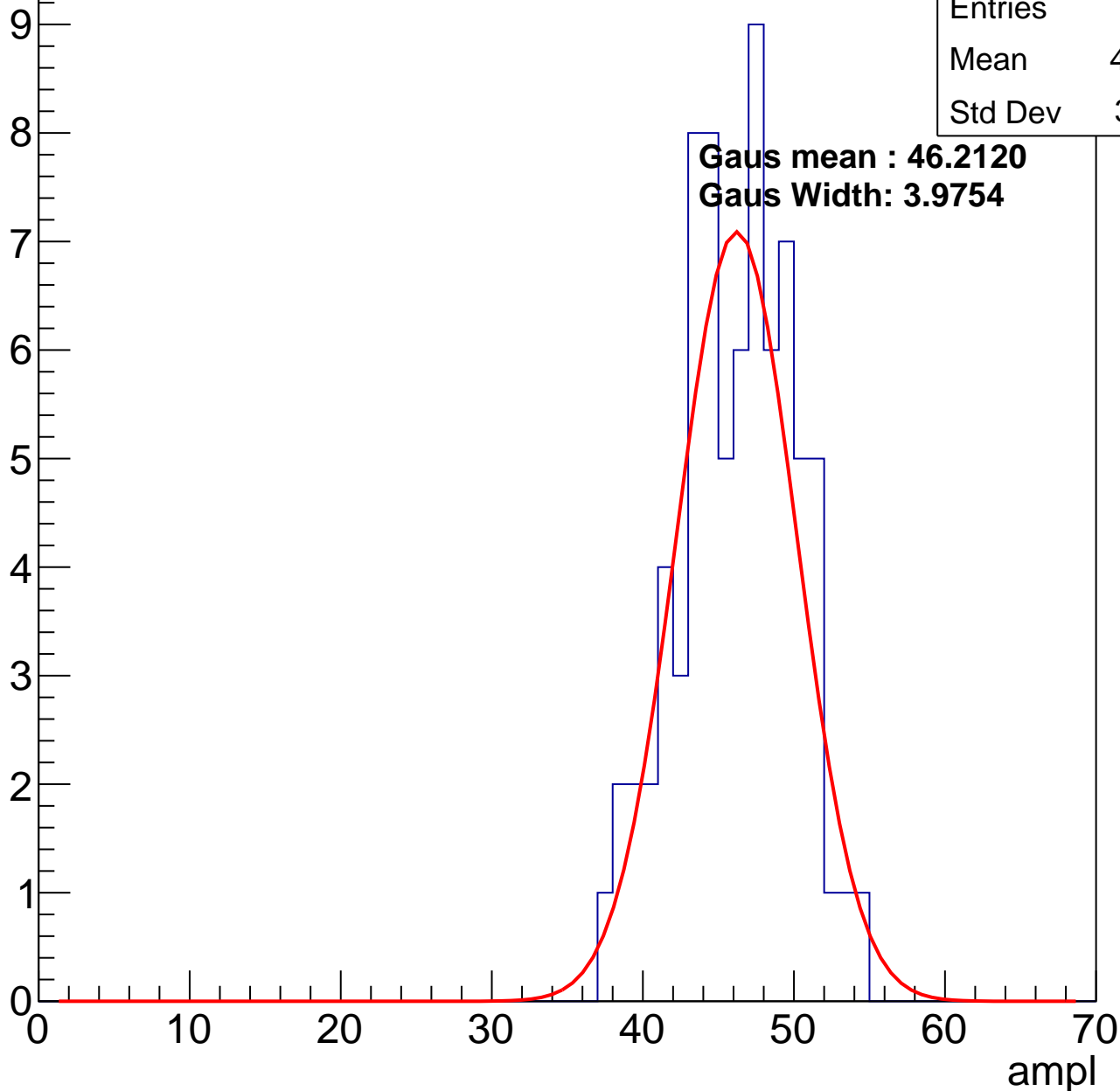
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	76
Mean	45.74
Std Dev	3.771

**Gaus mean : 46.2120**

**Gaus Width: 3.9754**

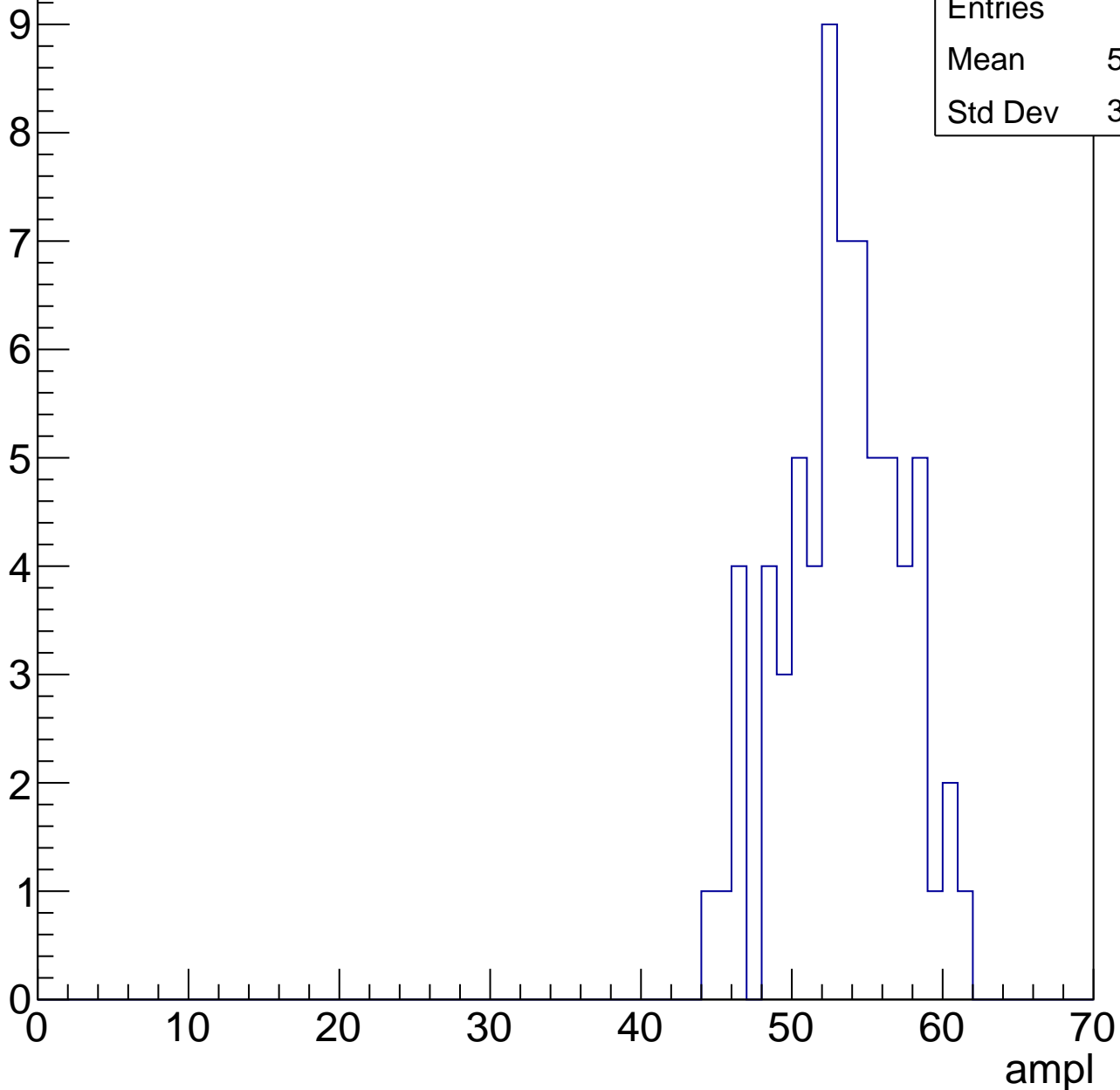


# B0L001S, U24-ch109, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	52.88
Std Dev	3.867

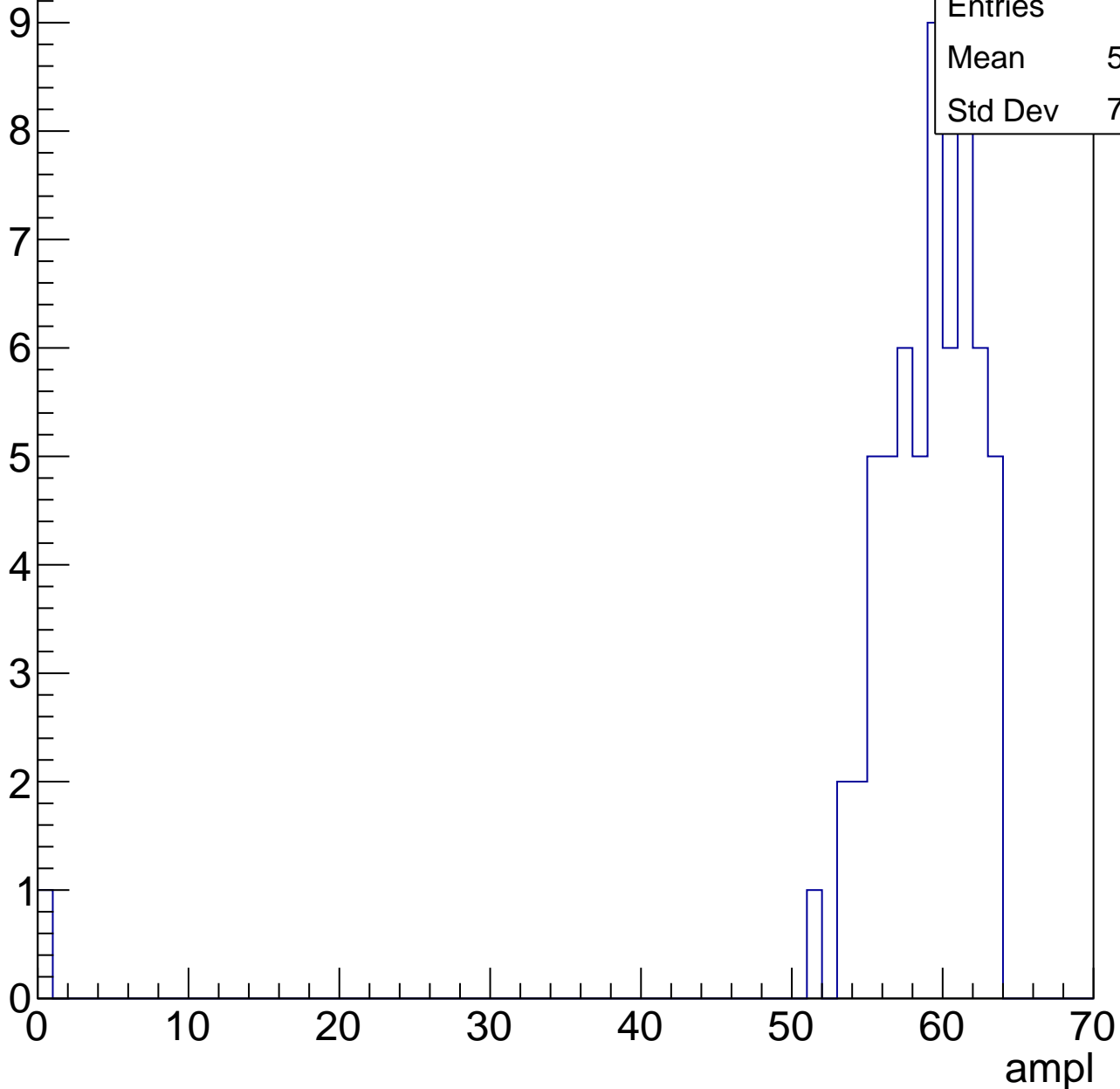


# B0L001S, U24-ch109, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	57.73
Std Dev	7.927

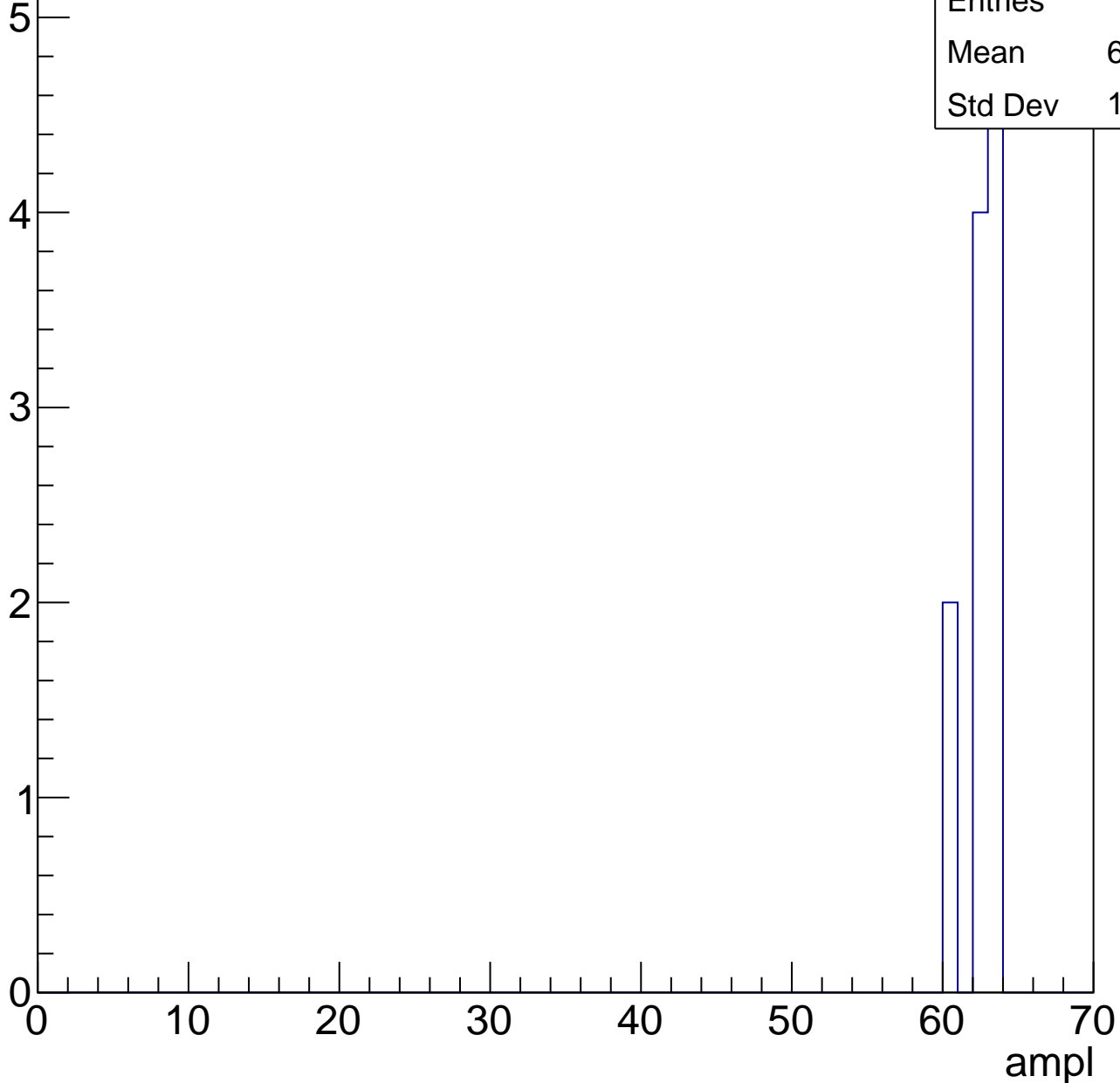


# B0L001S, U24-ch109, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	11
Mean	62.09
Std Dev	1.083



# B0L001S, U24-ch109, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



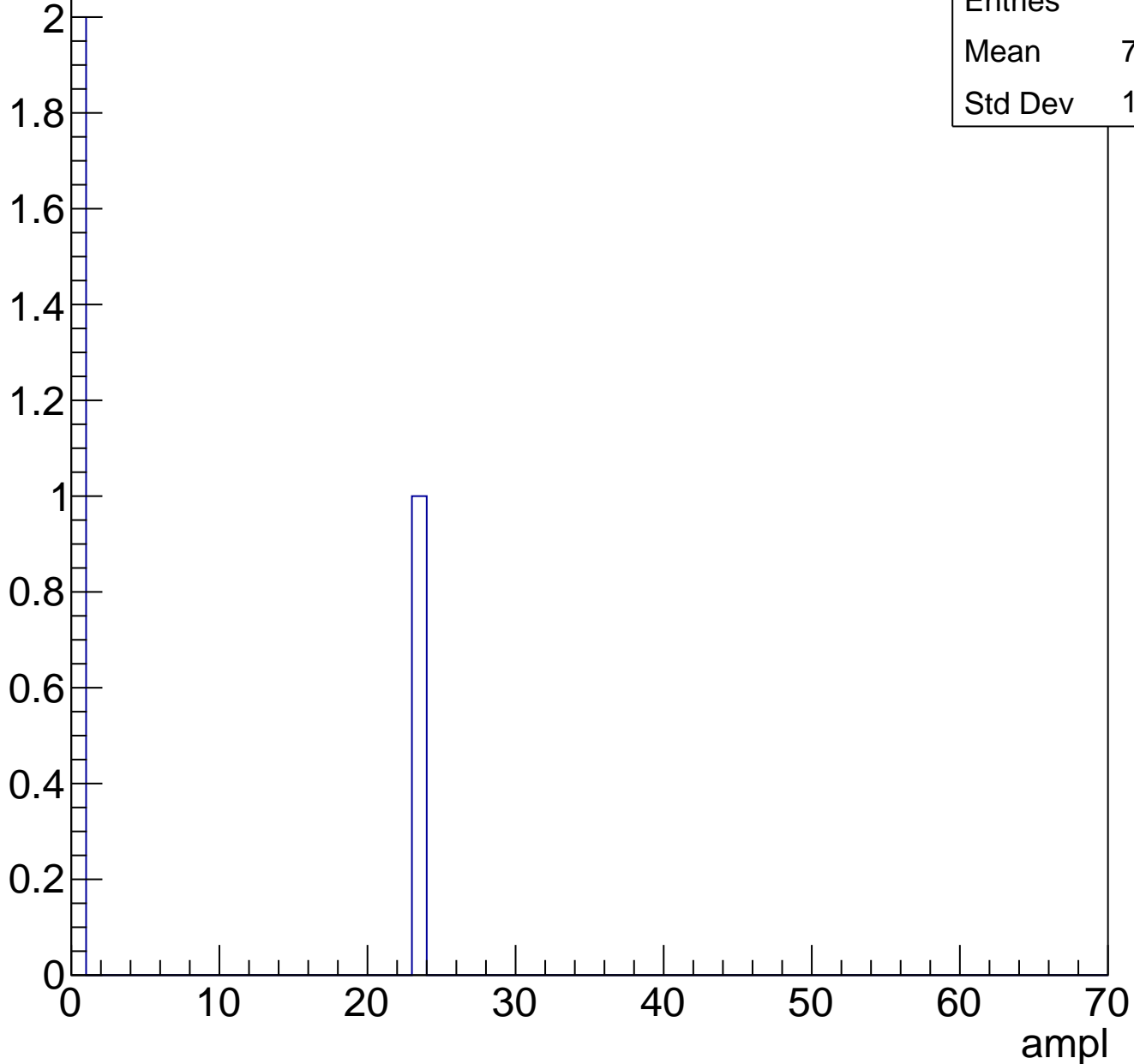
Entries	0
Mean	0
Std Dev	0



# B0L001S, U24-ch109, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U24-ch110, adc0

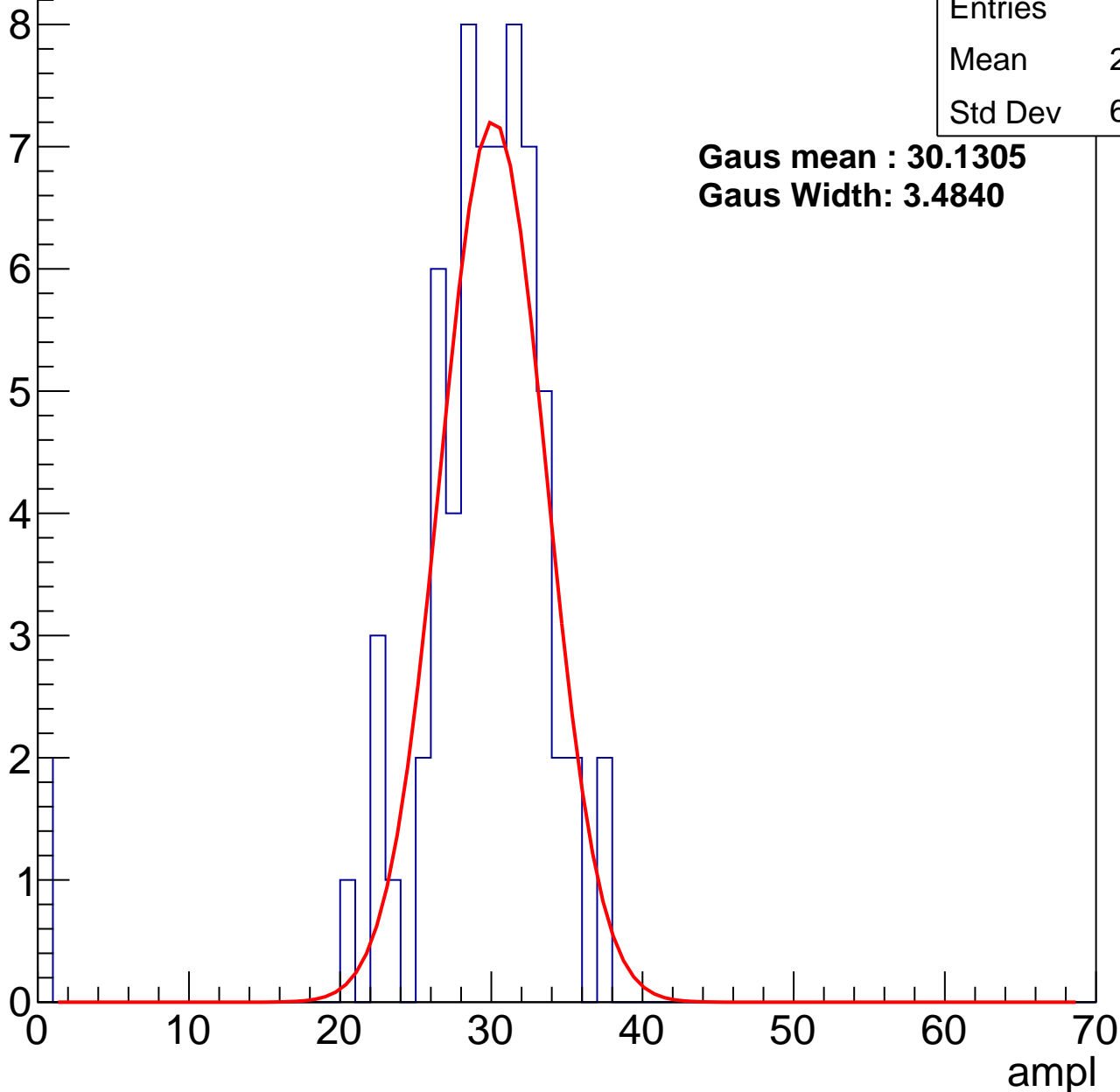
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	28.49
Std Dev	6.073

**Gaus mean : 30.1305**

**Gaus Width: 3.4840**



# B0L001S, U24-ch110, adc1

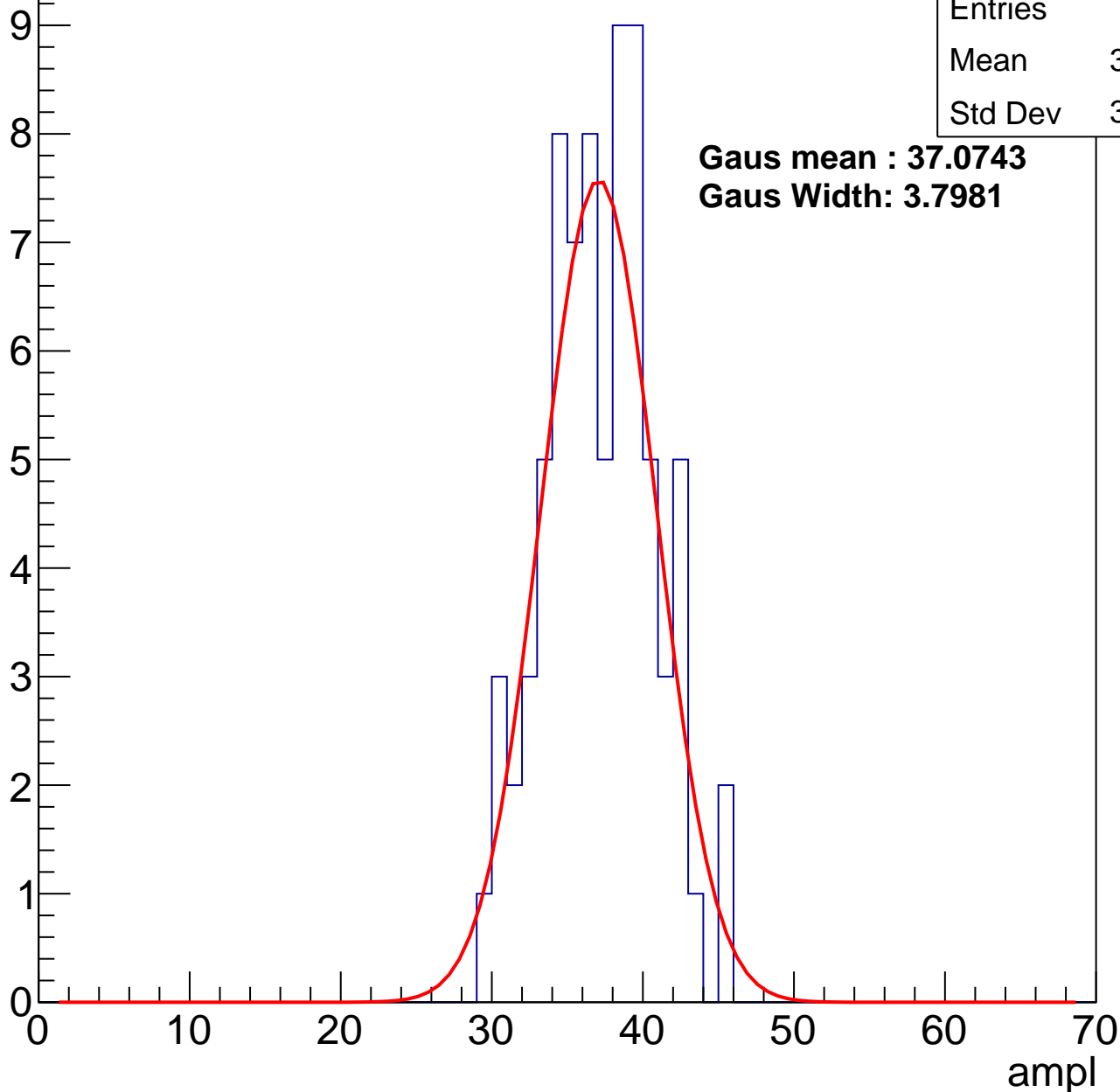
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	76
Mean	36.72
Std Dev	3.567

**Gaus mean : 37.0743**

**Gaus Width: 3.7981**



# B0L001S, U24-ch110, adc2

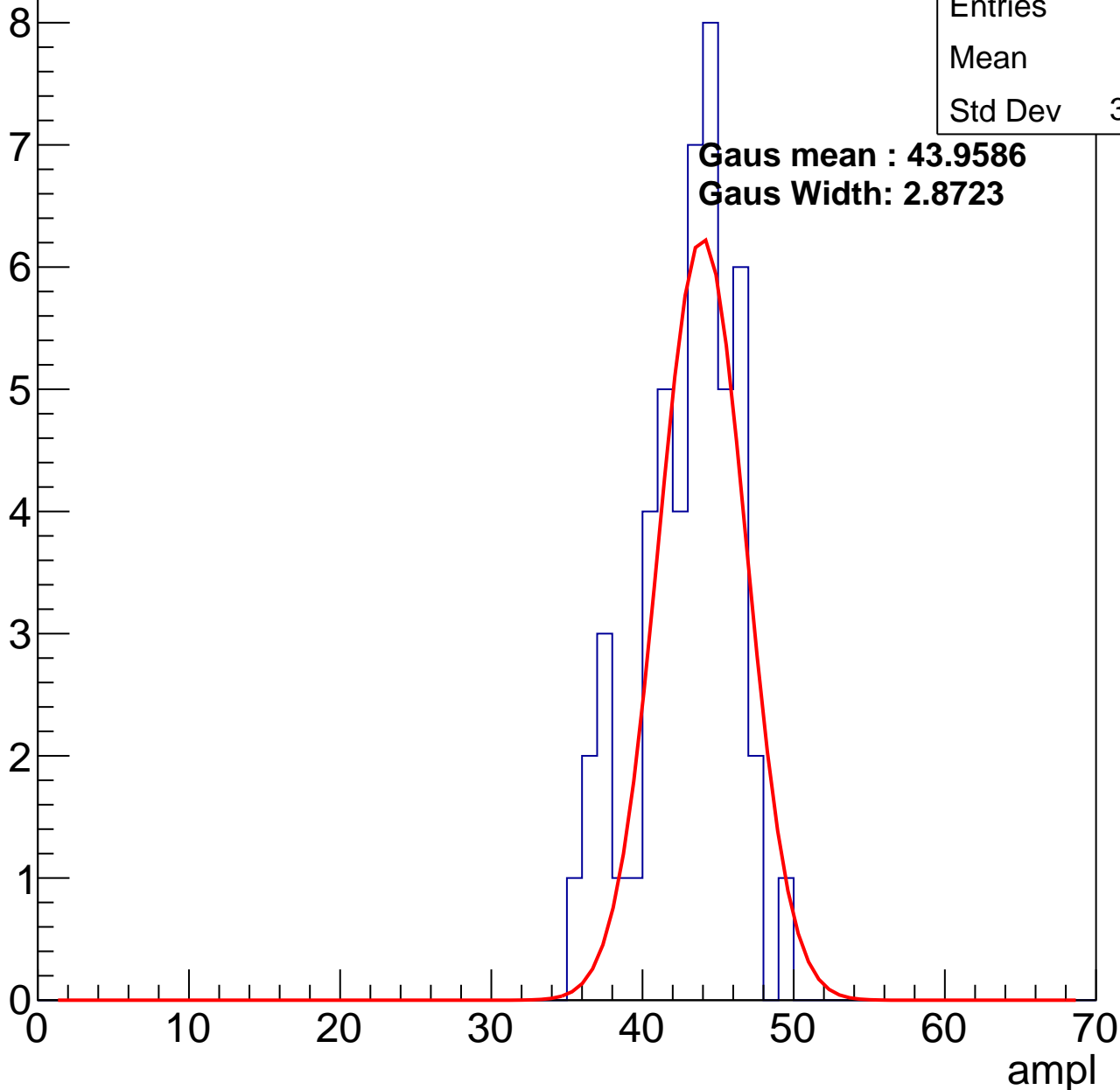
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	50
Mean	42.5
Std Dev	3.189

**Gaus mean : 43.9586**

**Gaus Width: 2.8723**

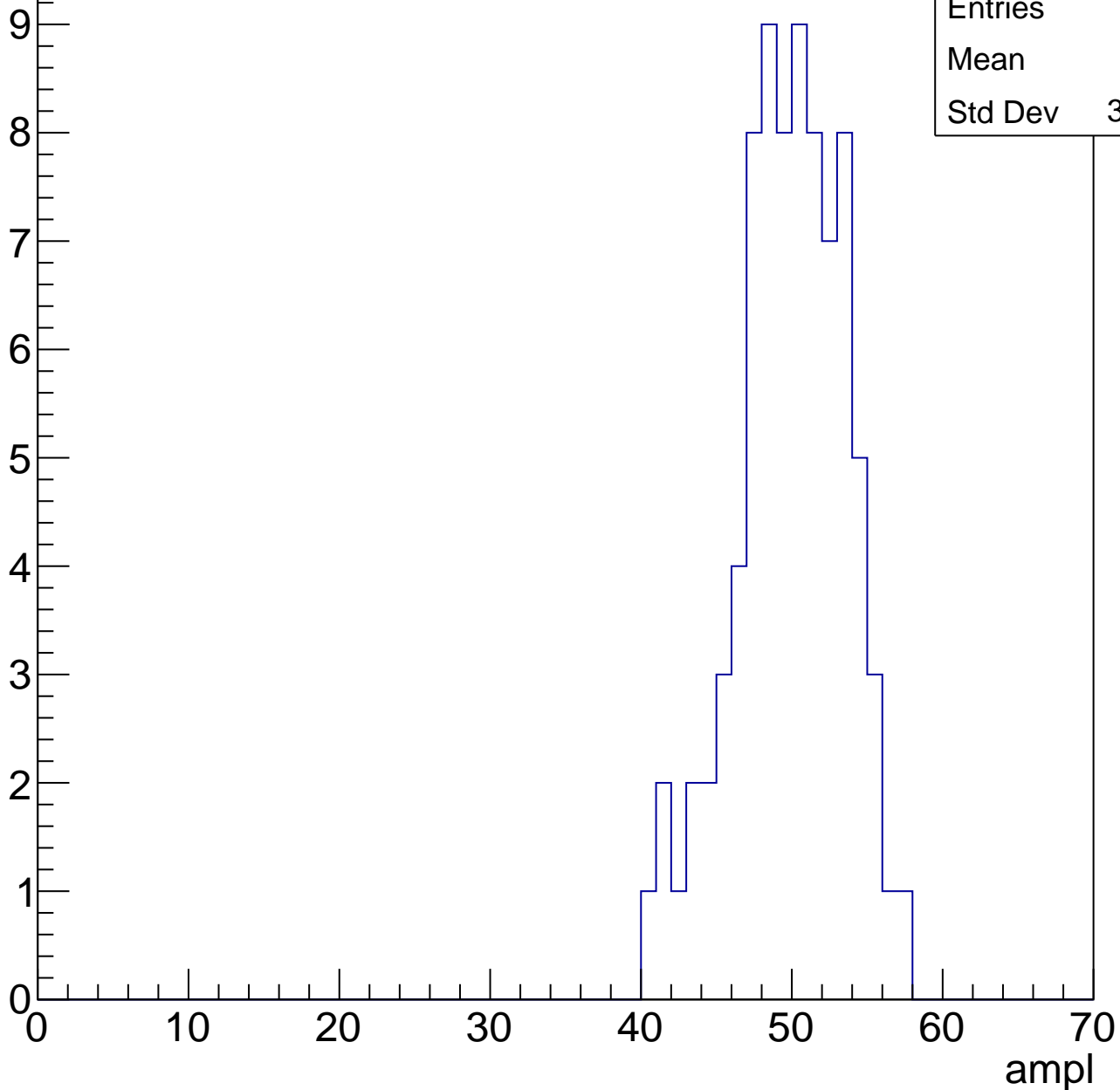


# B0L001S, U24-ch110, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	82
Mean	49.4
Std Dev	3.612

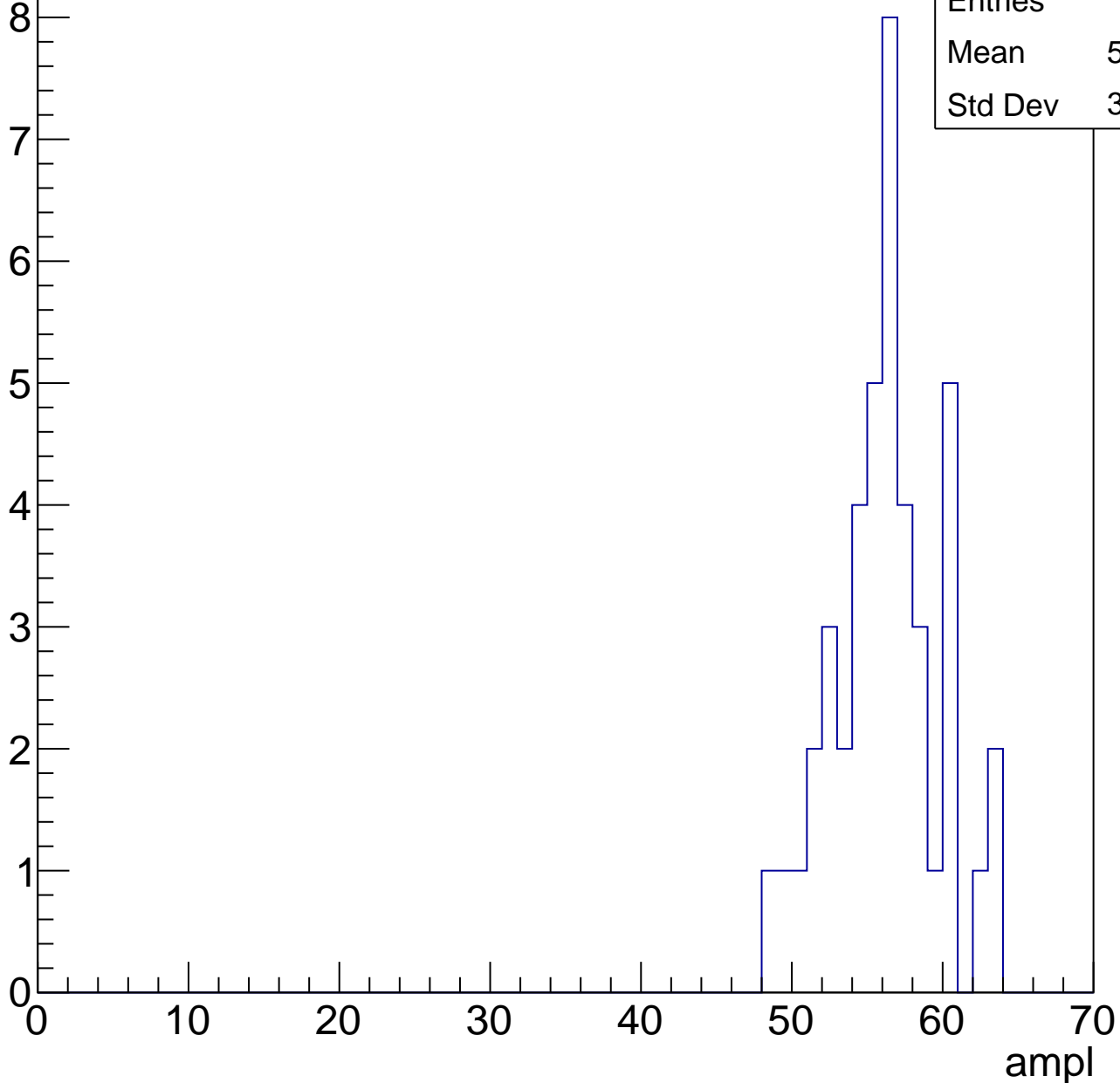


# B0L001S, U24-ch110, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

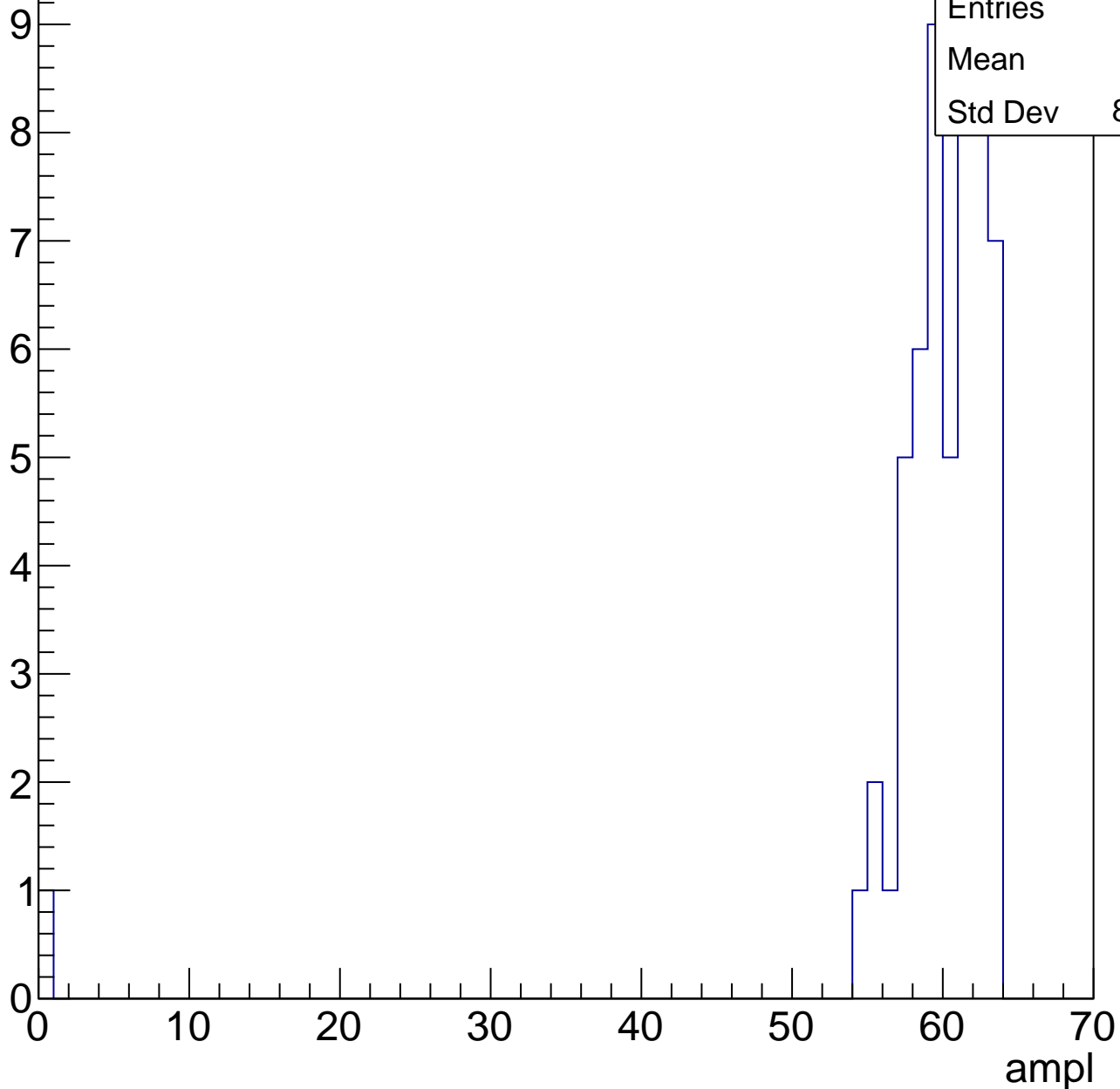
Entries	43
Mean	55.79
Std Dev	3.488



# B0L001S, U24-ch110, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

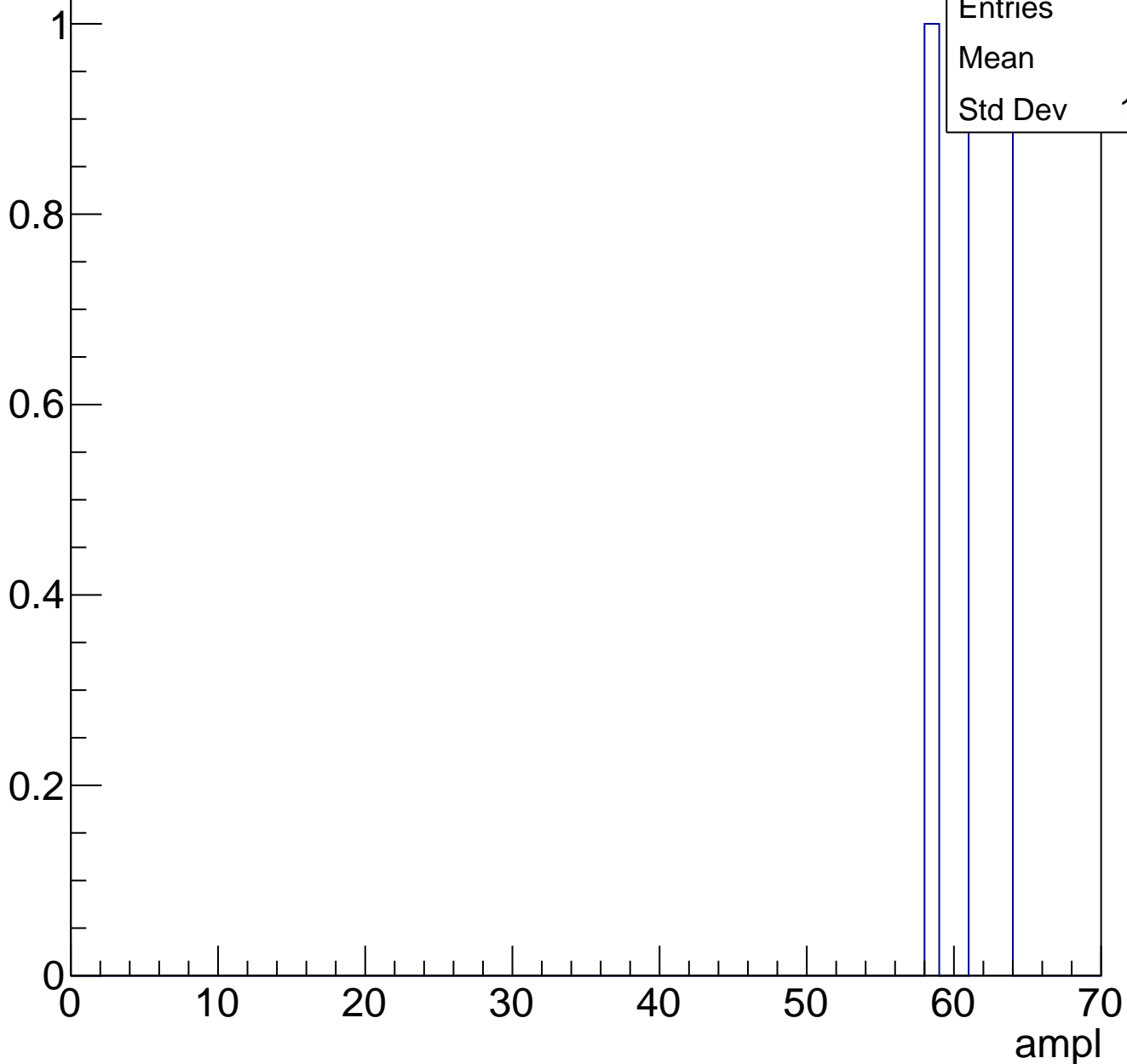
Entry



# B0L001S, U24-ch110, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch110, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U24-ch111, adc0

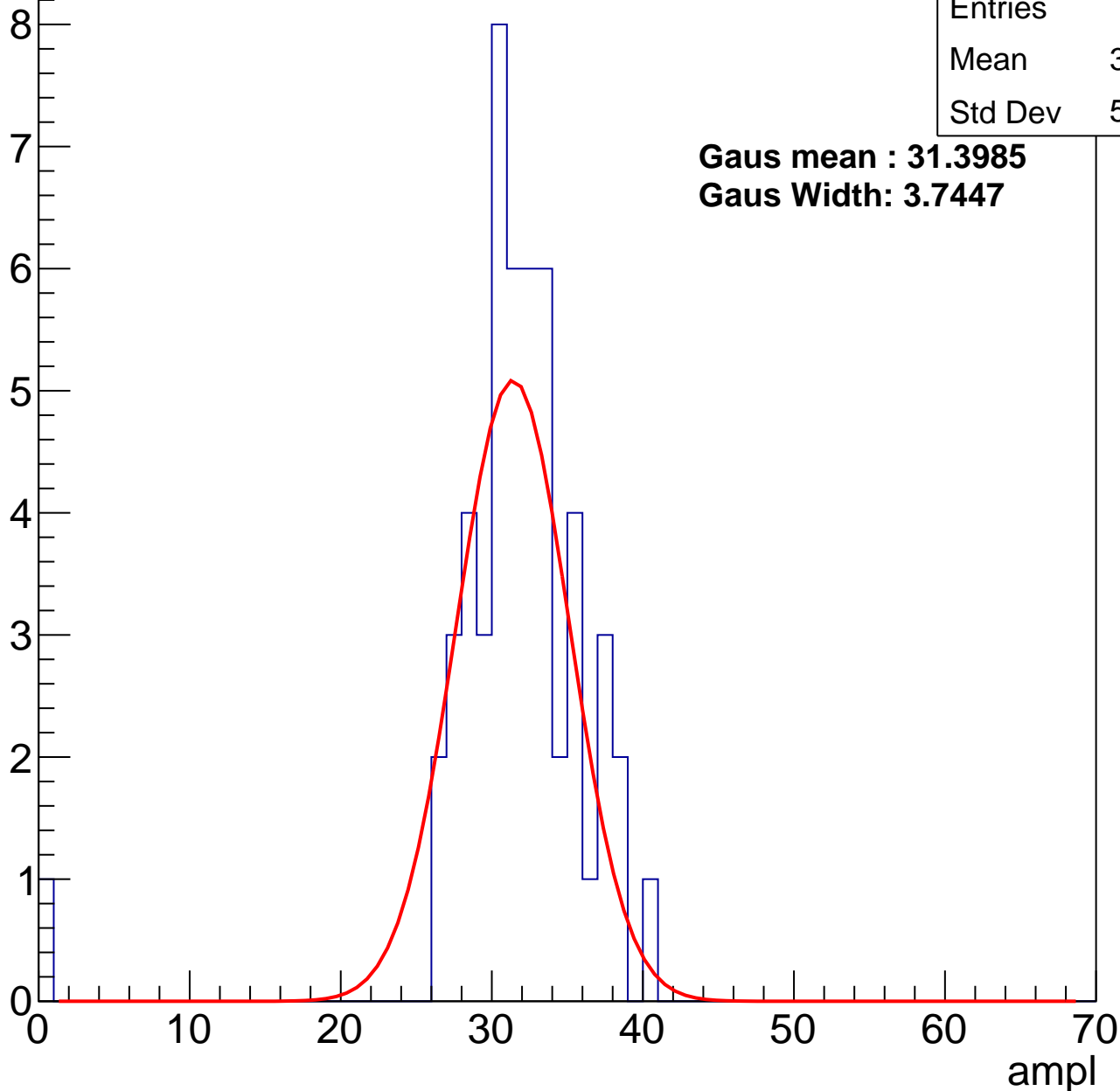
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	31.13
Std Dev	5.439

**Gaus mean : 31.3985**

**Gaus Width: 3.7447**



# B0L001S, U24-ch111, adc1

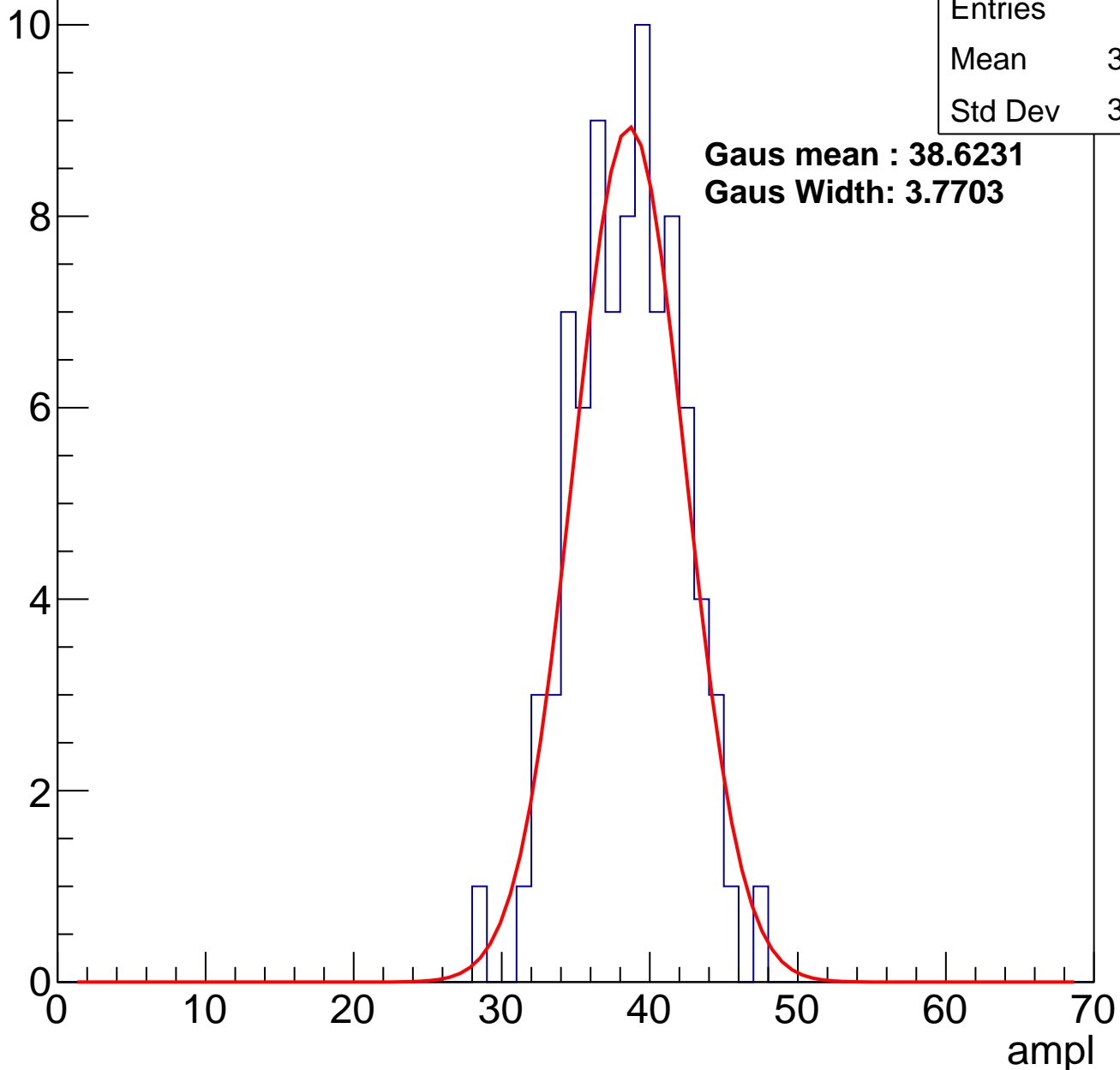
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	85
Mean	38.06
Std Dev	3.572

**Gaus mean : 38.6231**

**Gaus Width: 3.7703**

Entry



# B0L001S, U24-ch111, adc2

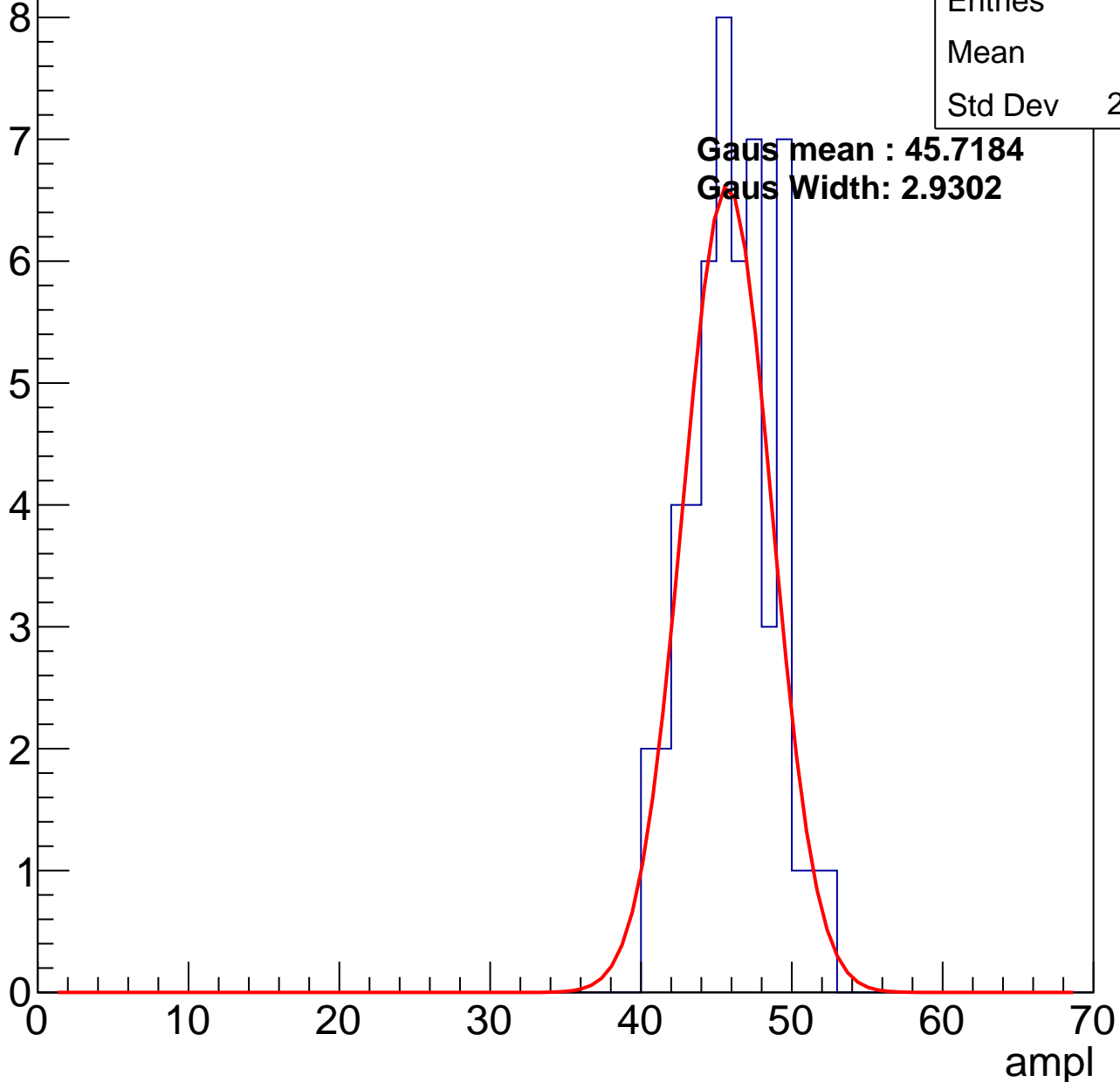
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	45.6
Std Dev	2.789

Gaus mean : 45.7184

Gaus Width: 2.9302

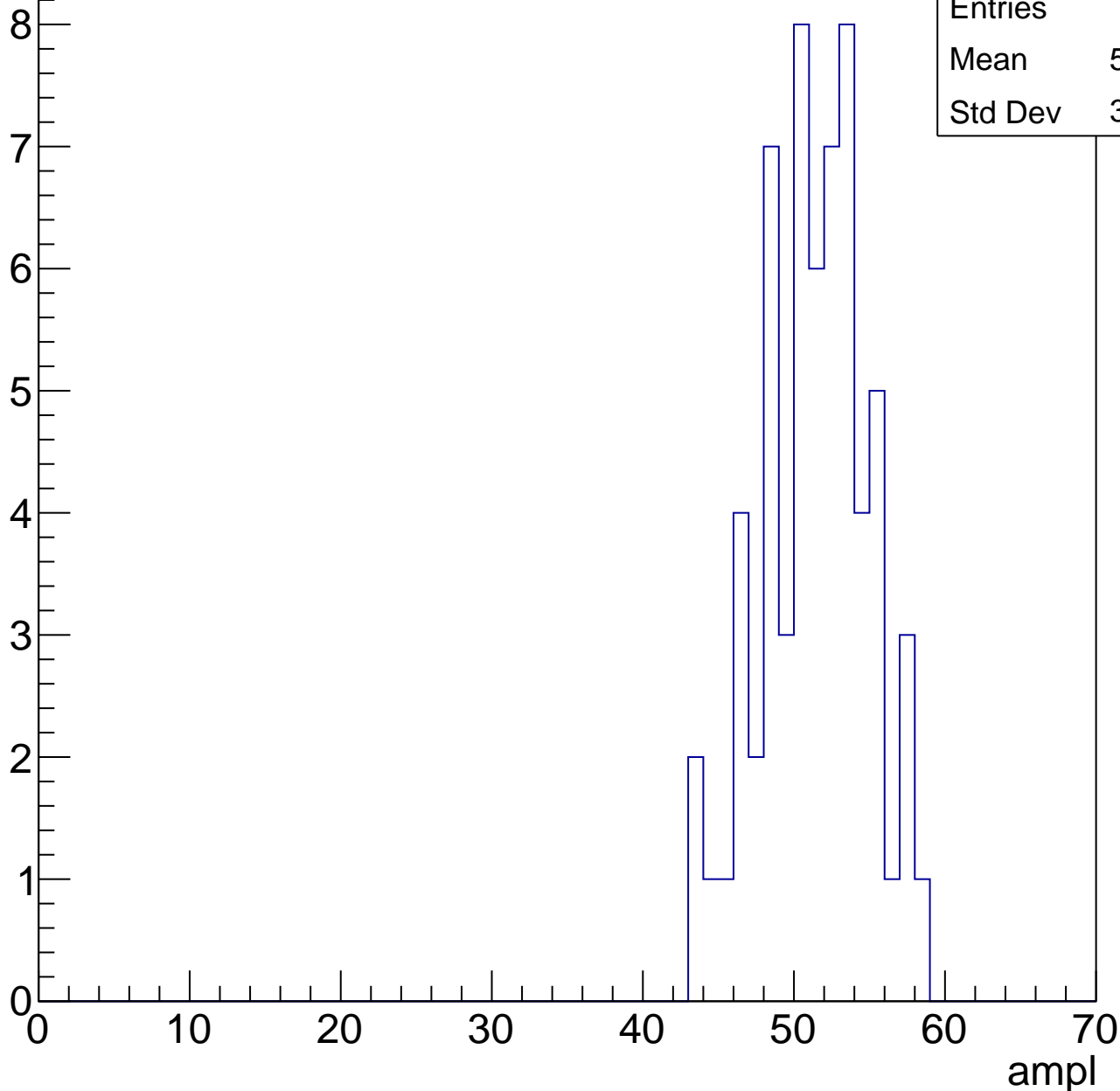


# B0L001S, U24-ch111, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	50.89
Std Dev	3.483



# B0L001S, U24-ch111, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	65
Mean	57.12
Std Dev	3.061

Entry

10

8

6

4

2

0

0

10

20

30

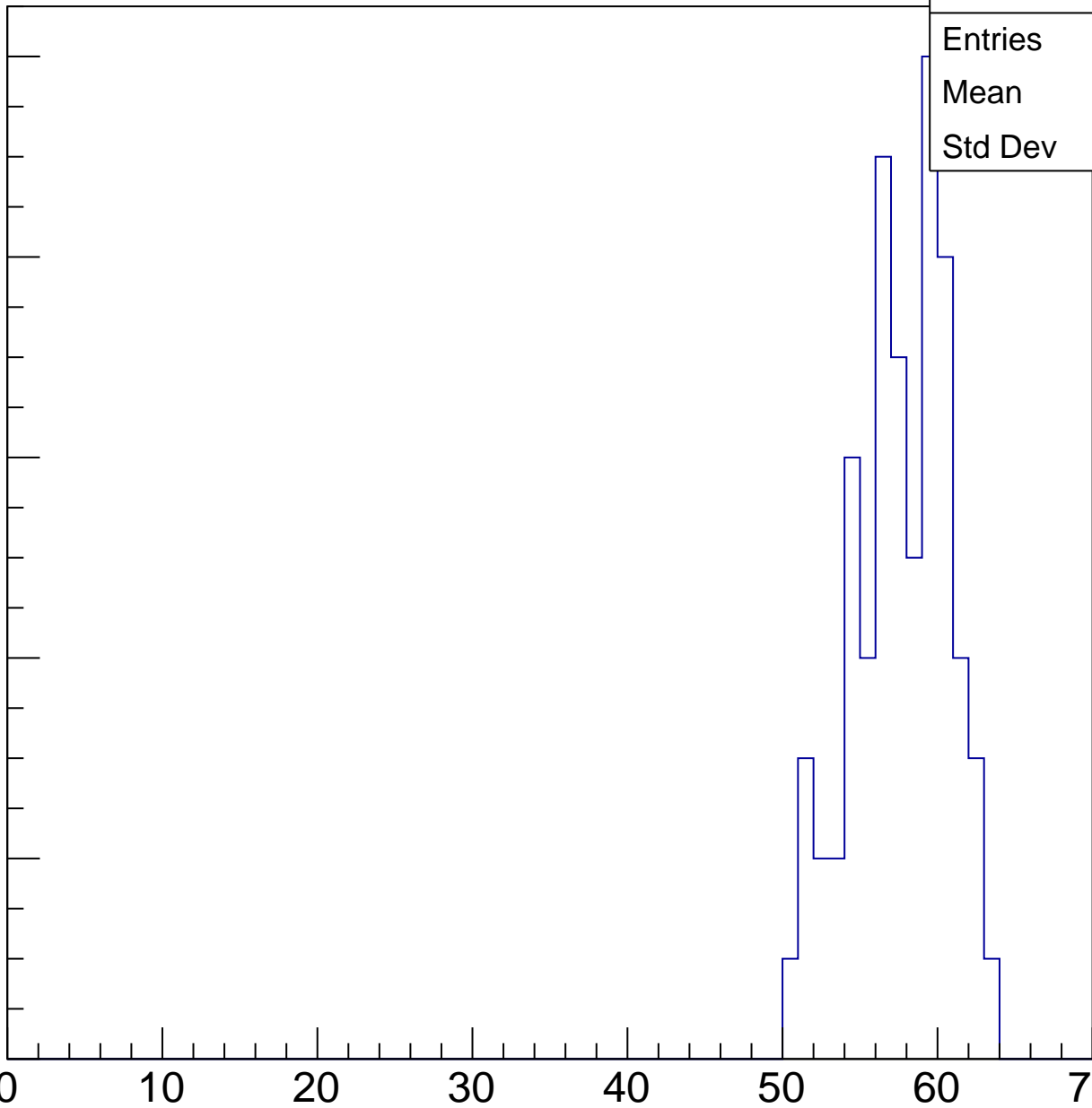
40

50

60

70

ampl

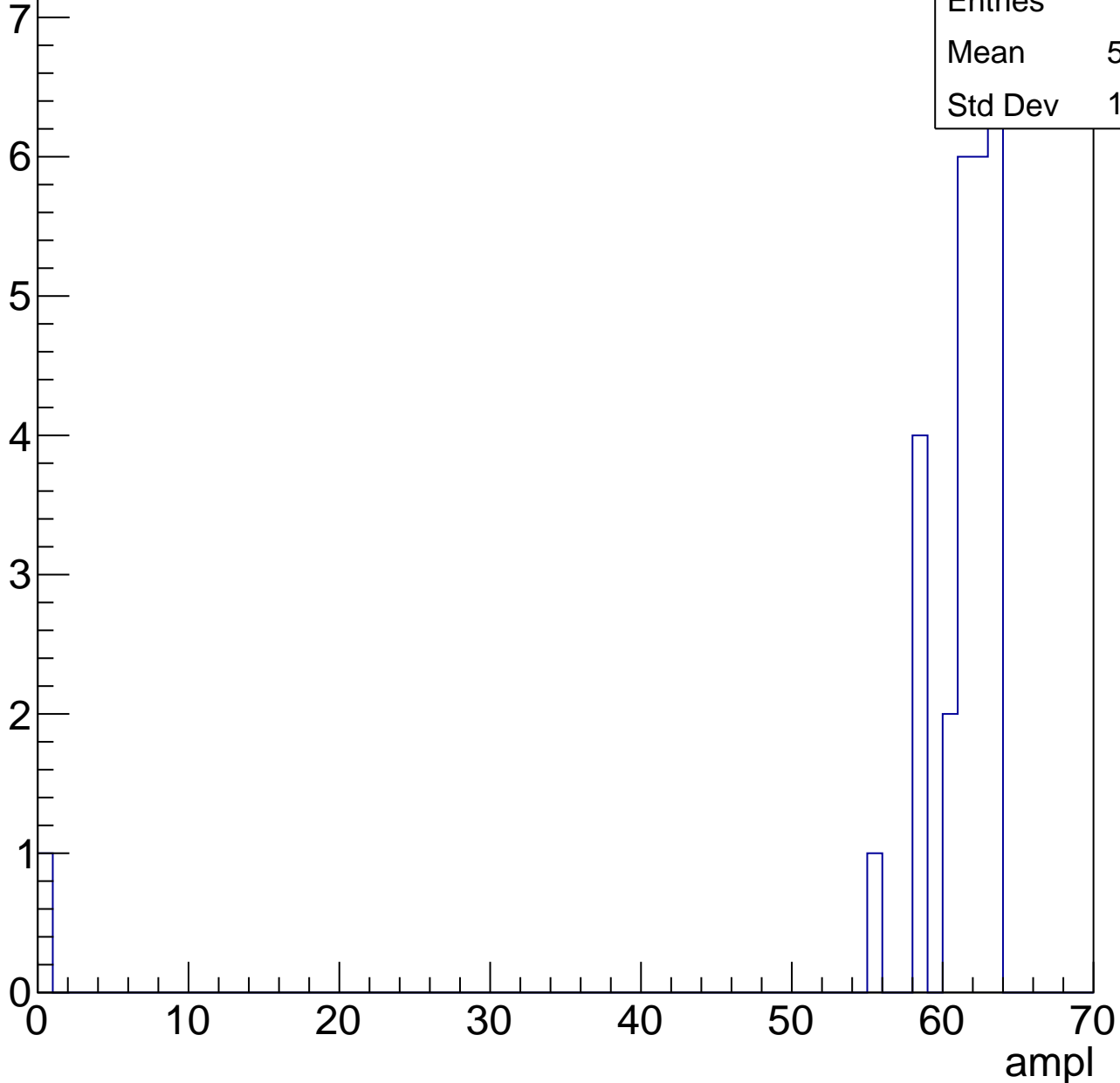


# B0L001S, U24-ch111, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	27
Mean	58.74
Std Dev	11.69



# B0L001S, U24-ch111, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

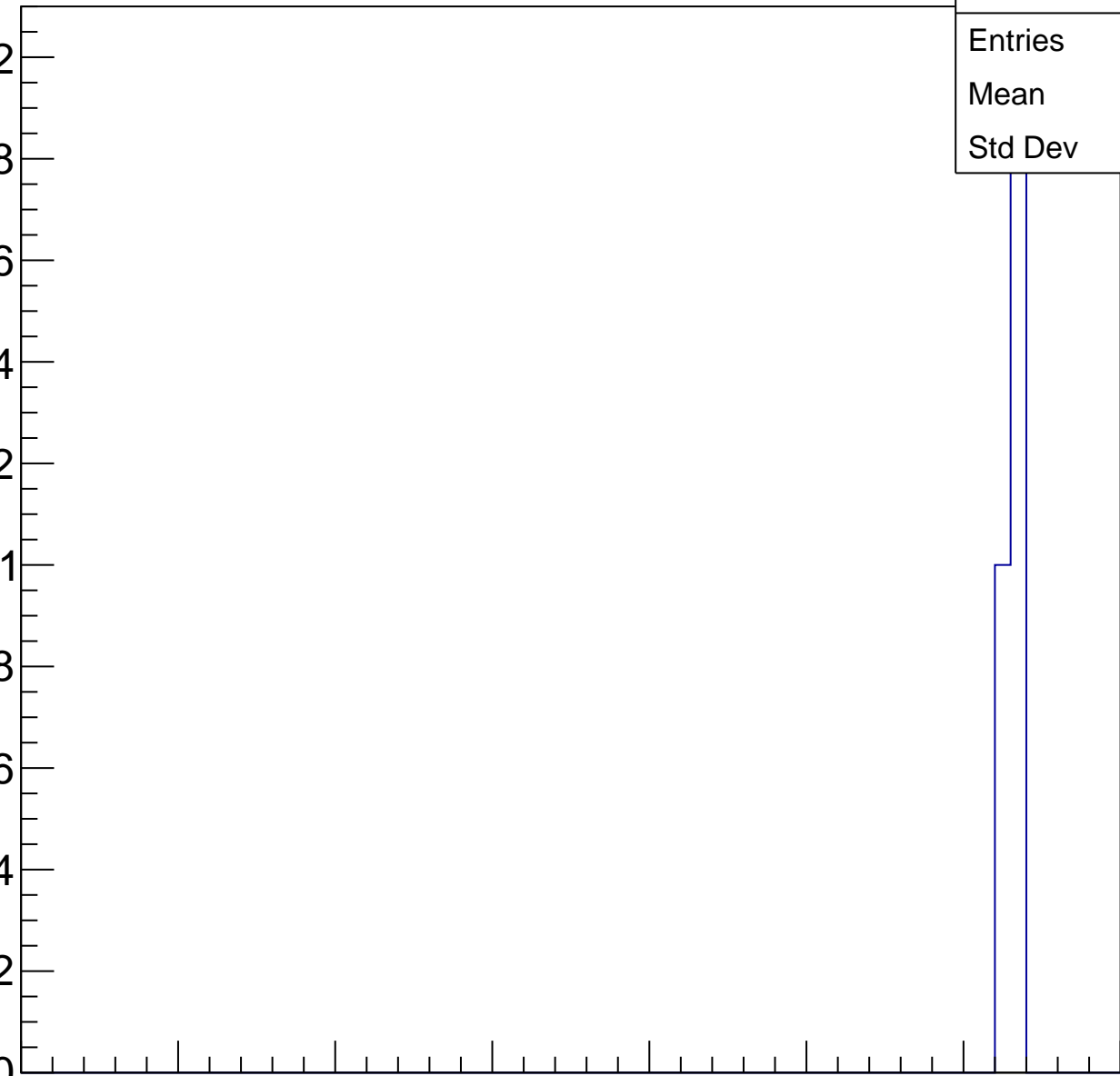
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.67
Std Dev	0.4714

ampl

0 10 20 30 40 50 60 70





# B0L001S, U24-ch111, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U24-ch112, adc0

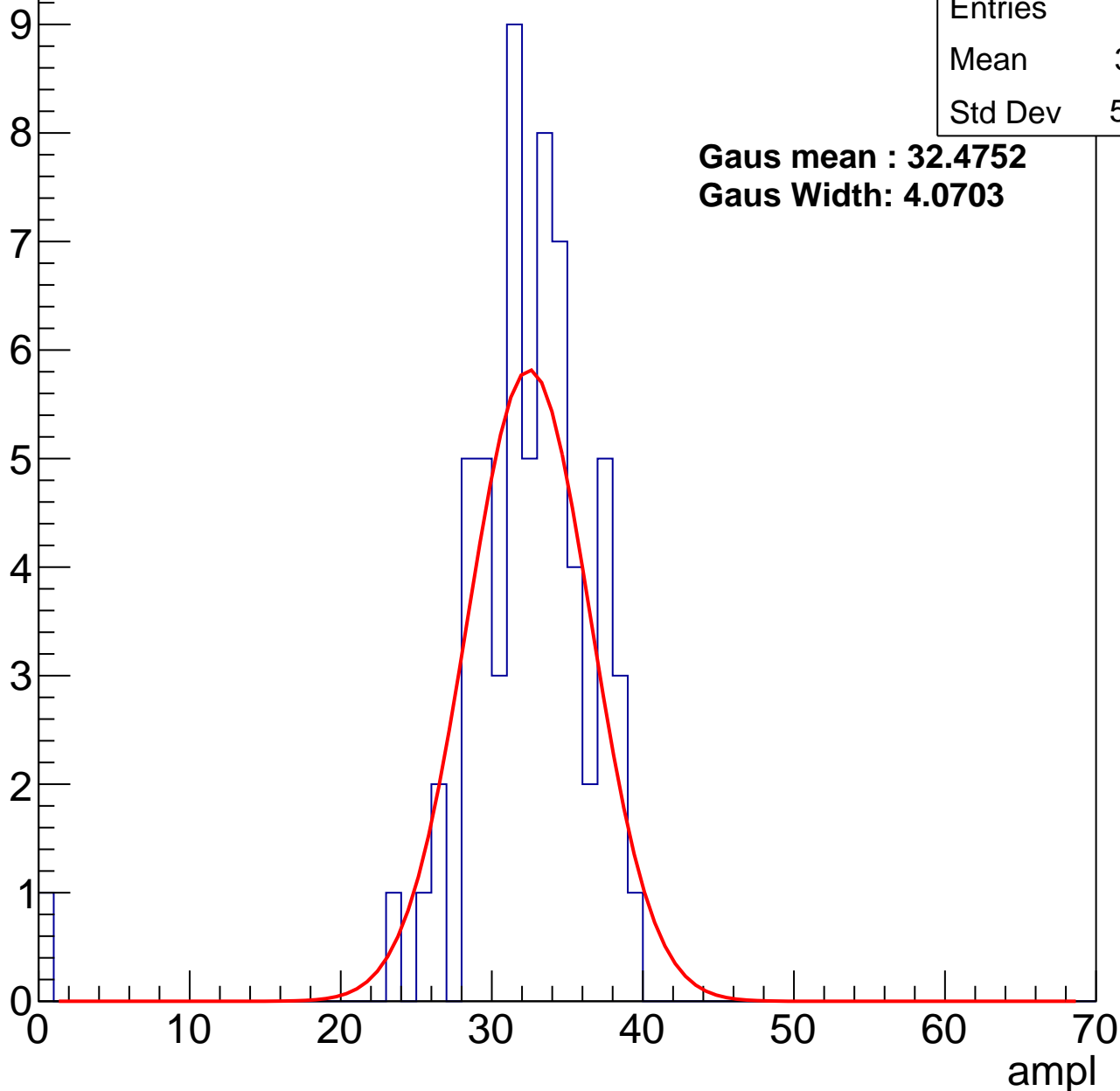
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	31.71
Std Dev	5.317

**Gaus mean : 32.4752**

**Gaus Width: 4.0703**



# B0L001S, U24-ch112, adc1

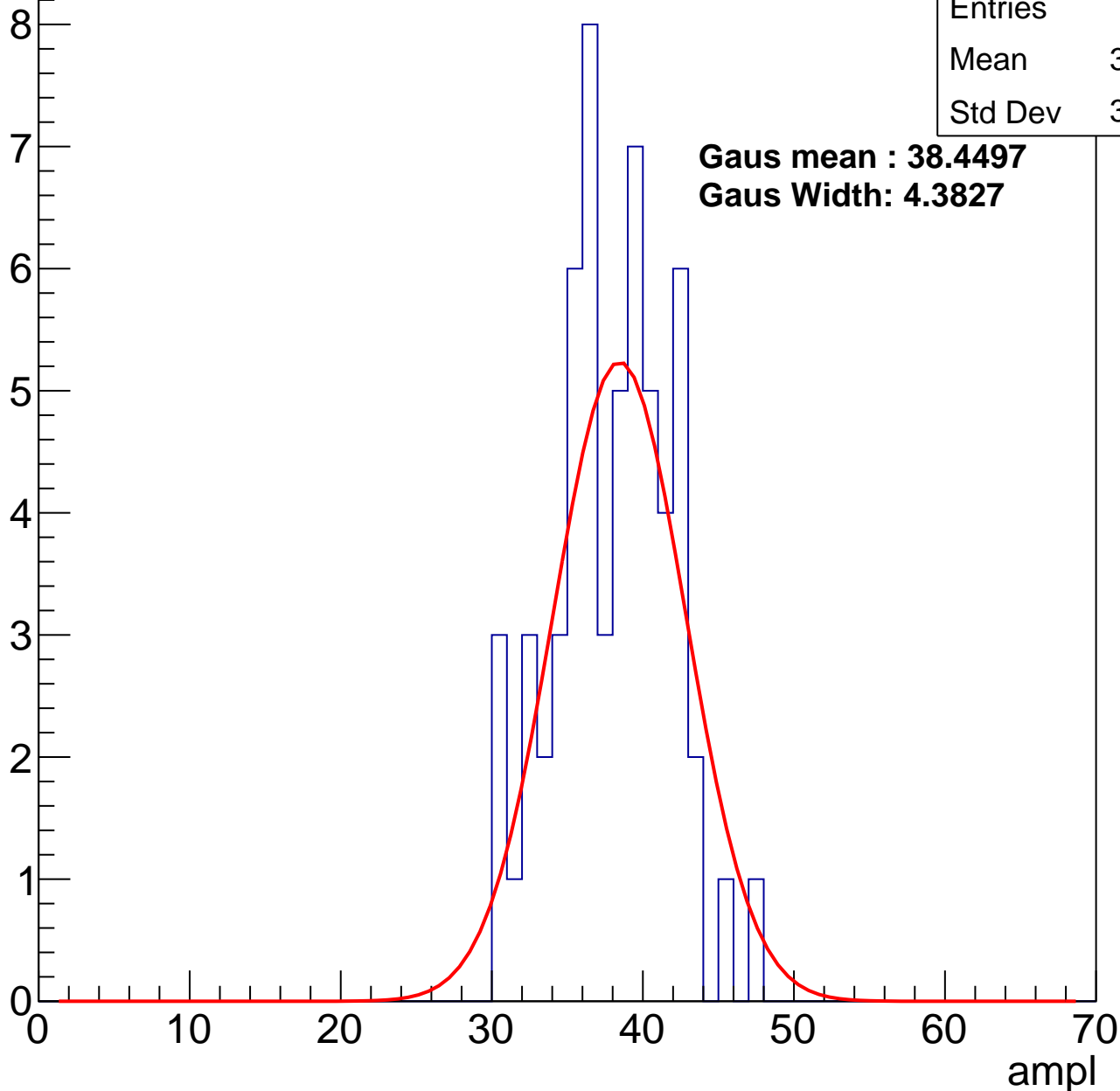
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	37.52
Std Dev	3.788

**Gaus mean : 38.4497**

**Gaus Width: 4.3827**



# B0L001S, U24-ch112, adc2

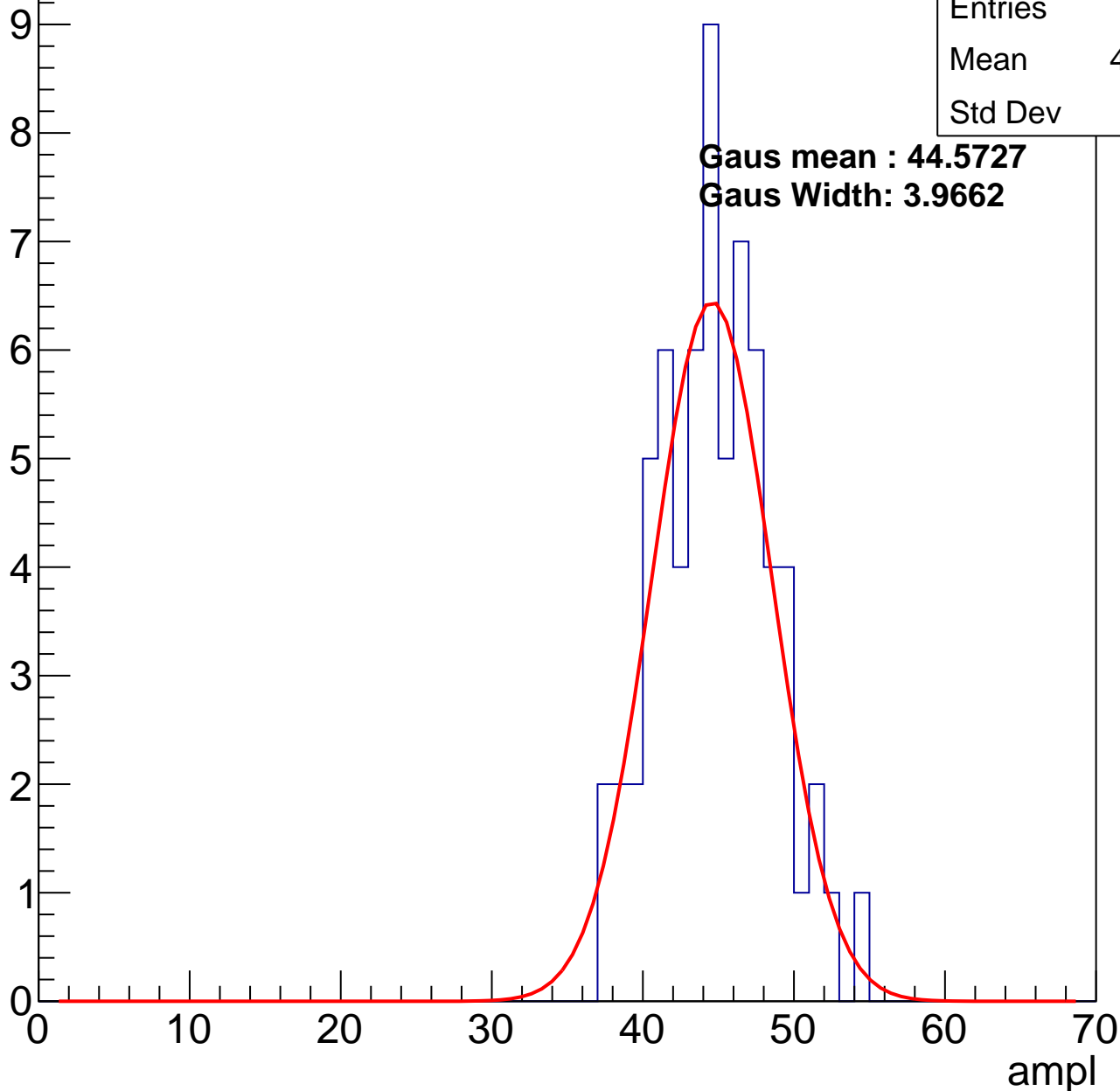
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	44.34
Std Dev	3.7

**Gaus mean : 44.5727**

**Gaus Width: 3.9662**

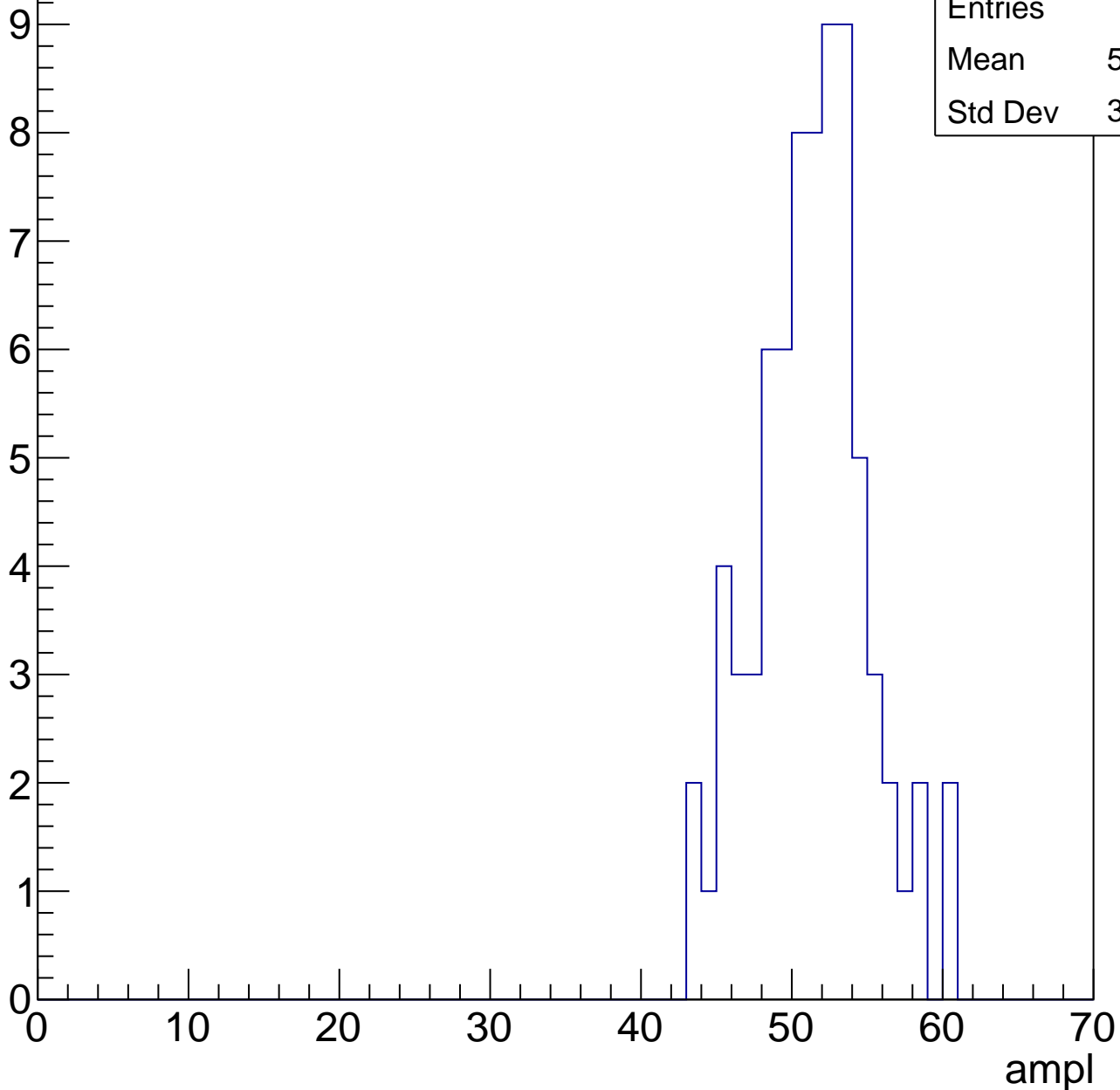


# B0L001S, U24-ch112, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	50.86
Std Dev	3.699

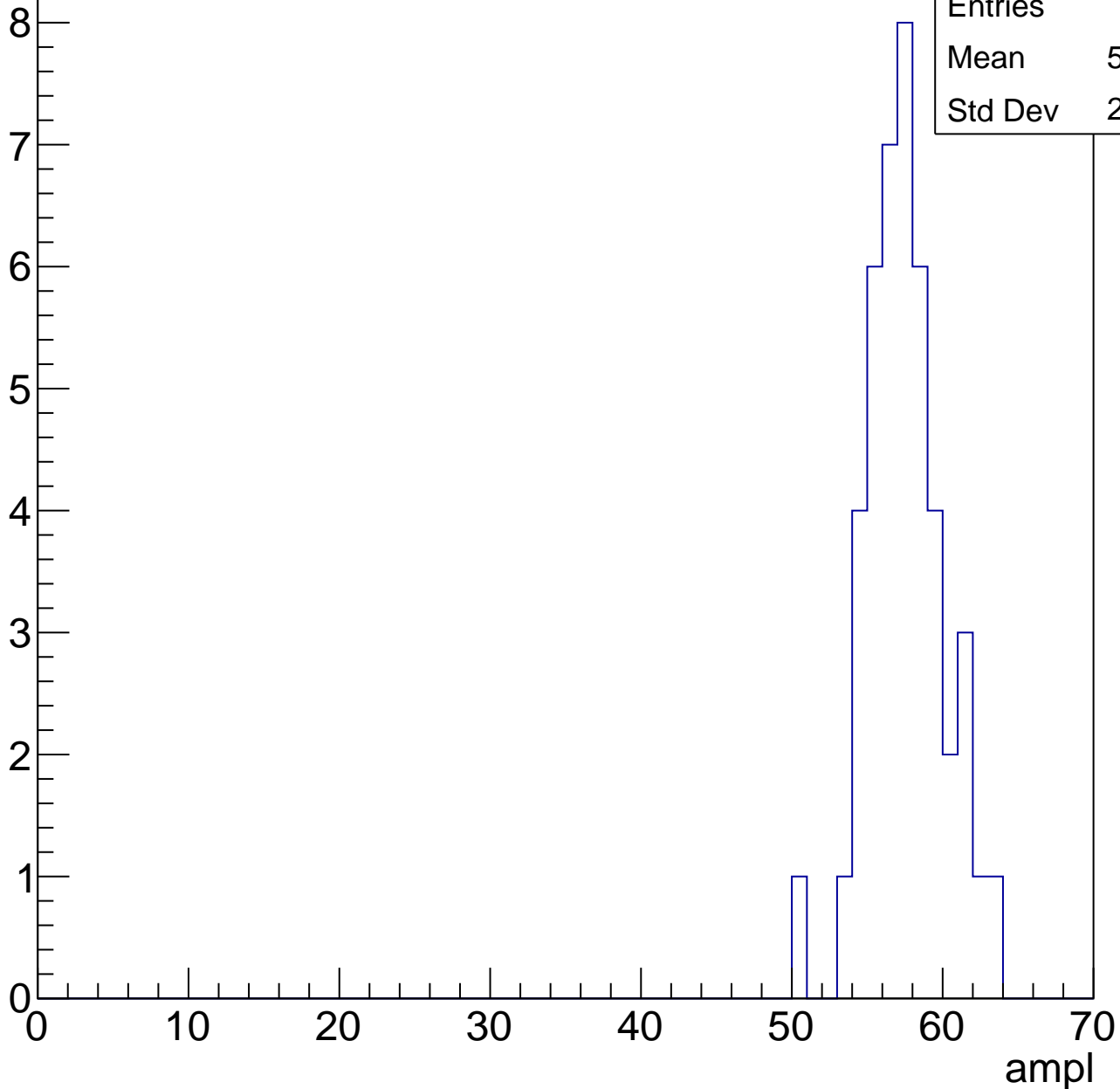


# B0L001S, U24-ch112, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	44
Mean	57.02
Std Dev	2.527

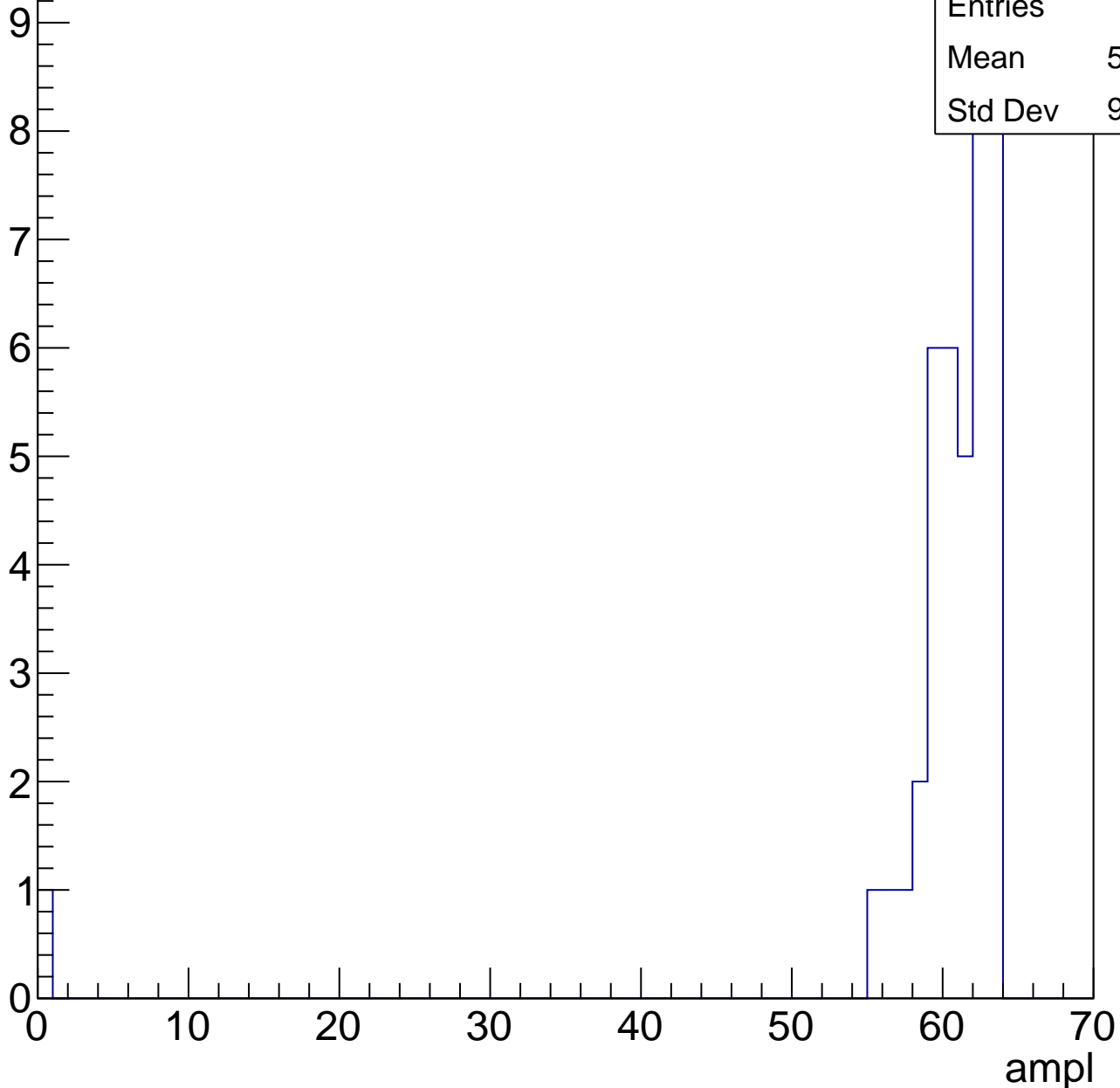


# B0L001S, U24-ch112, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	40
Mean	59.12
Std Dev	9.678



# B0L001S, U24-ch112, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

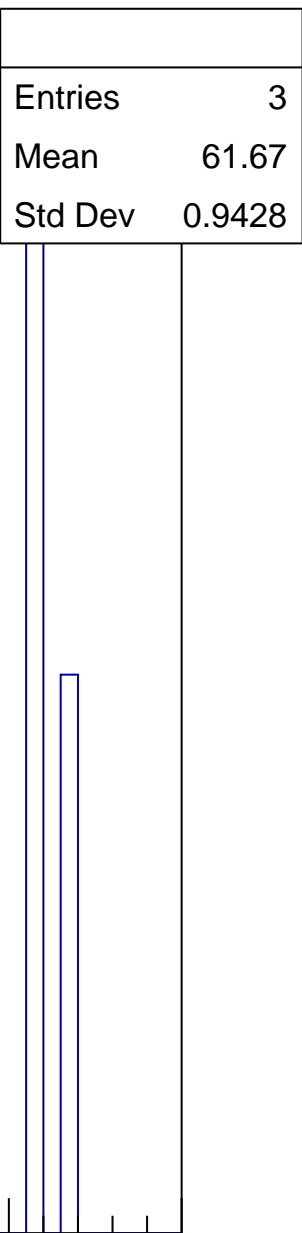
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	61.67
Std Dev	0.9428

0 10 20 30 40 50 60 70

ampl





# B0L001S, U24-ch112, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L001S, U24-ch113, adc0

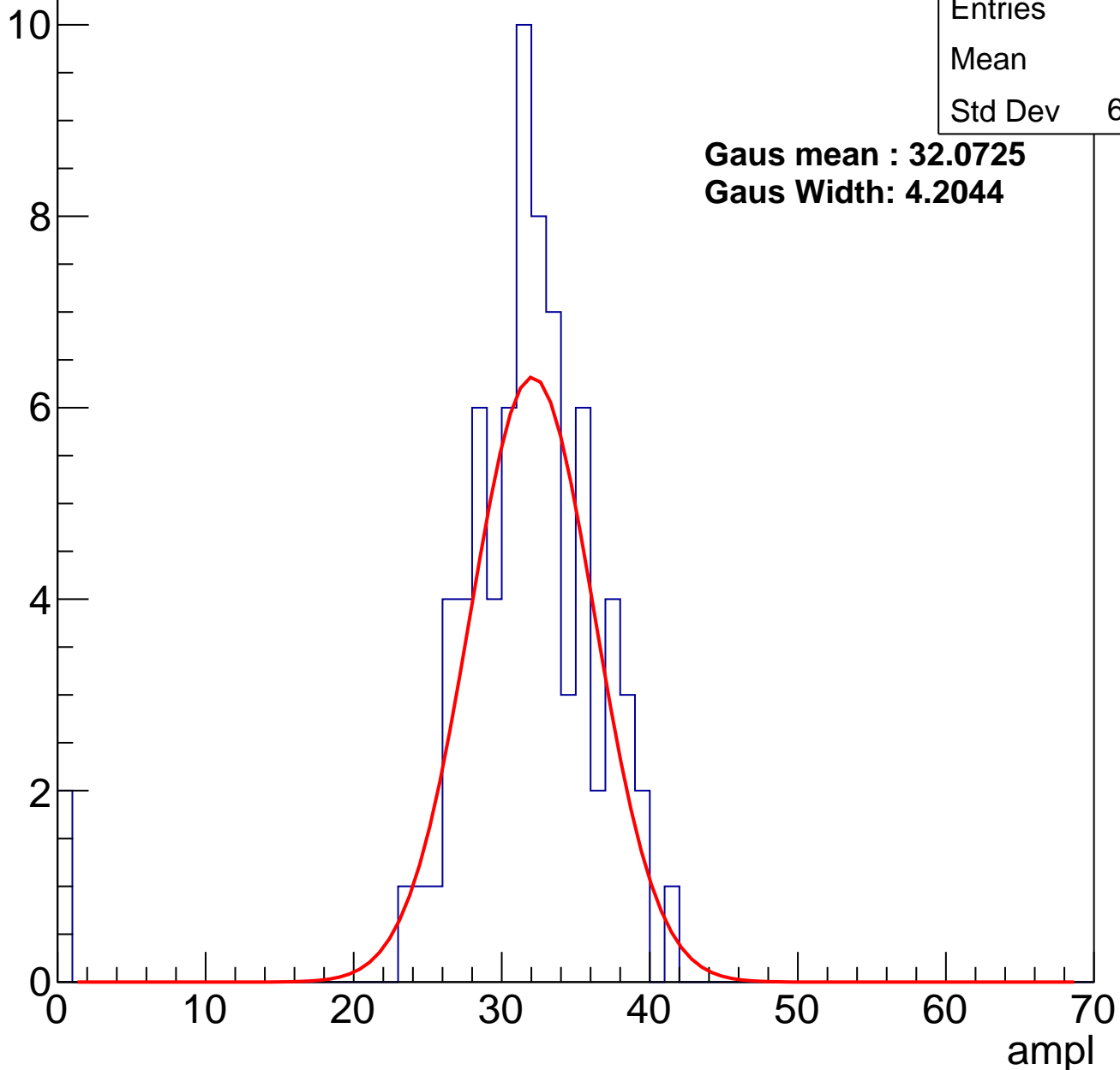
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	75
Mean	30.8
Std Dev	6.362

**Gaus mean : 32.0725**

**Gaus Width: 4.2044**

Entry



# B0L001S, U24-ch113, adc1

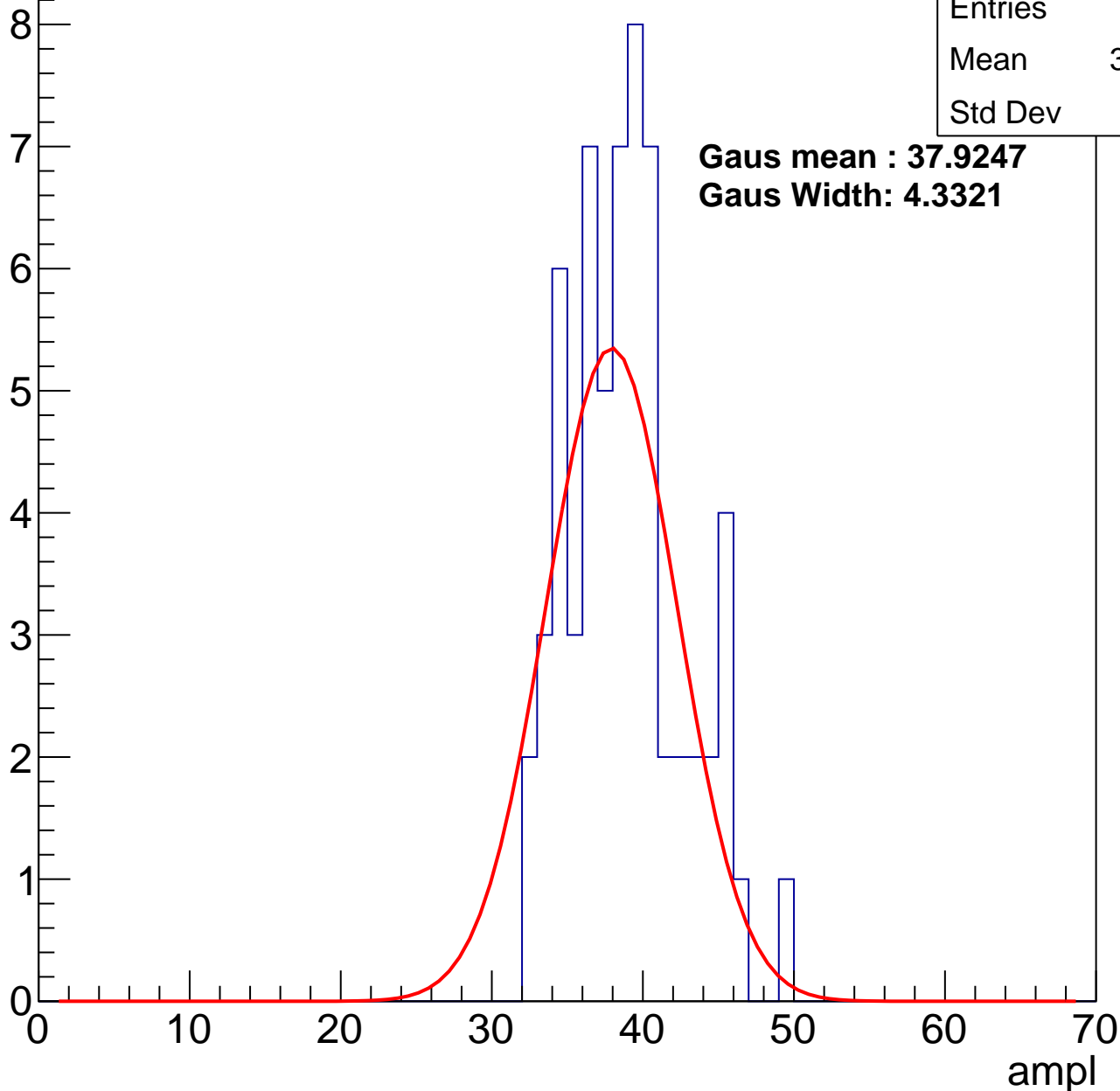
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	38.42
Std Dev	3.77

**Gaus mean : 37.9247**

**Gaus Width: 4.3321**



# B0L001S, U24-ch113, adc2

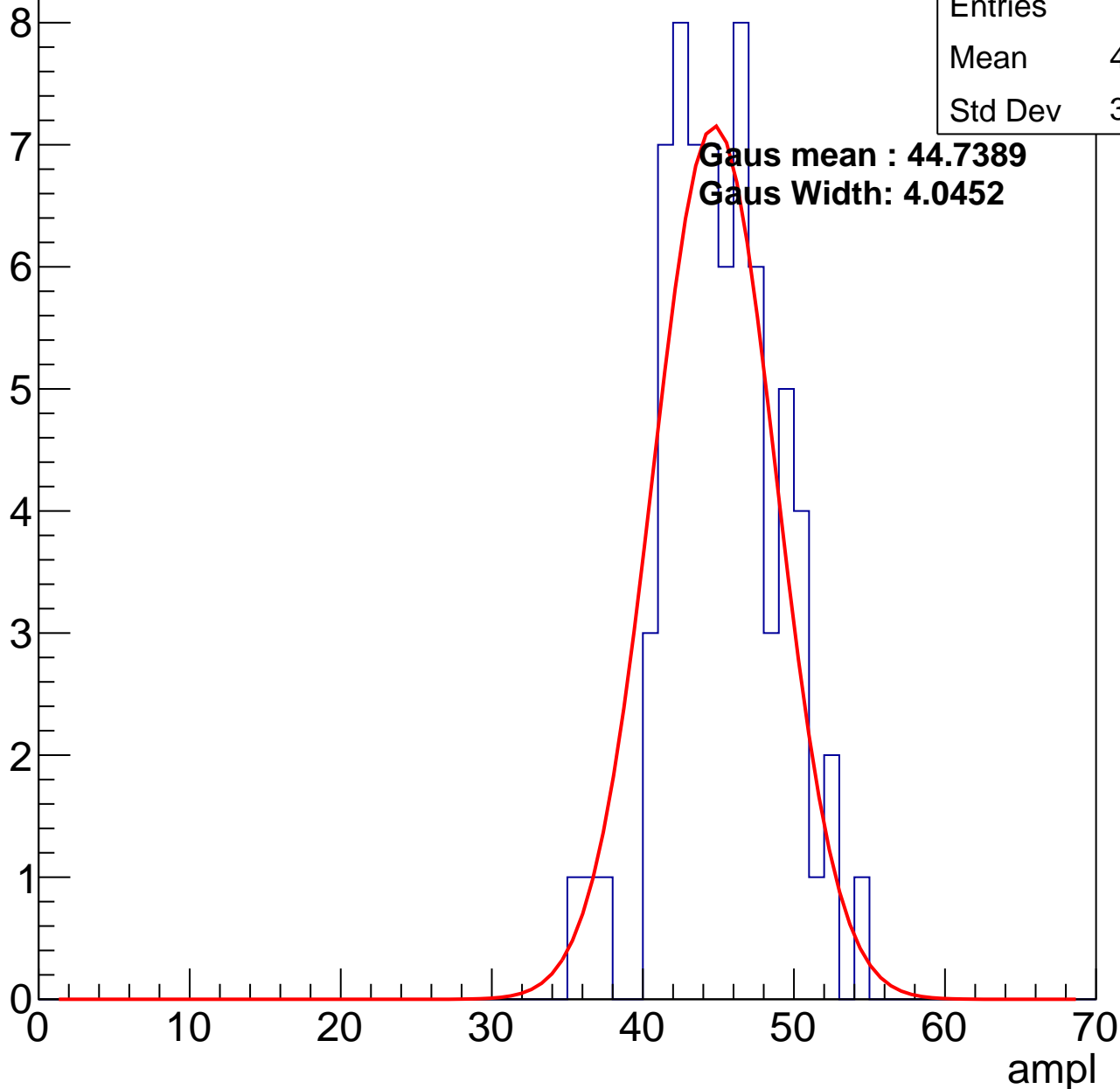
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	44.76
Std Dev	3.732

**Gaus mean : 44.7389**

**Gaus Width: 4.0452**

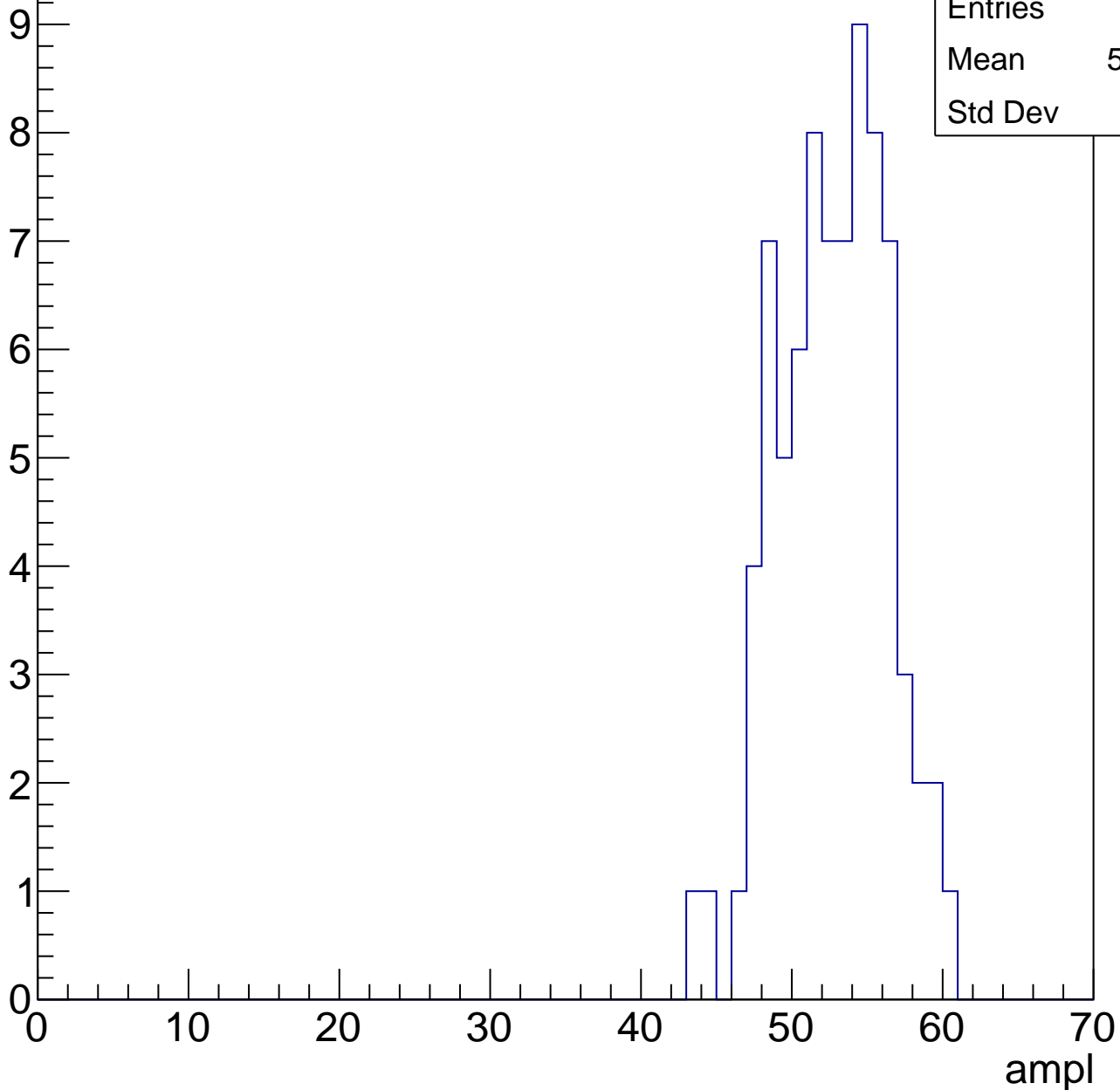


# B0L001S, U24-ch113, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	79
Mean	52.25
Std Dev	3.56

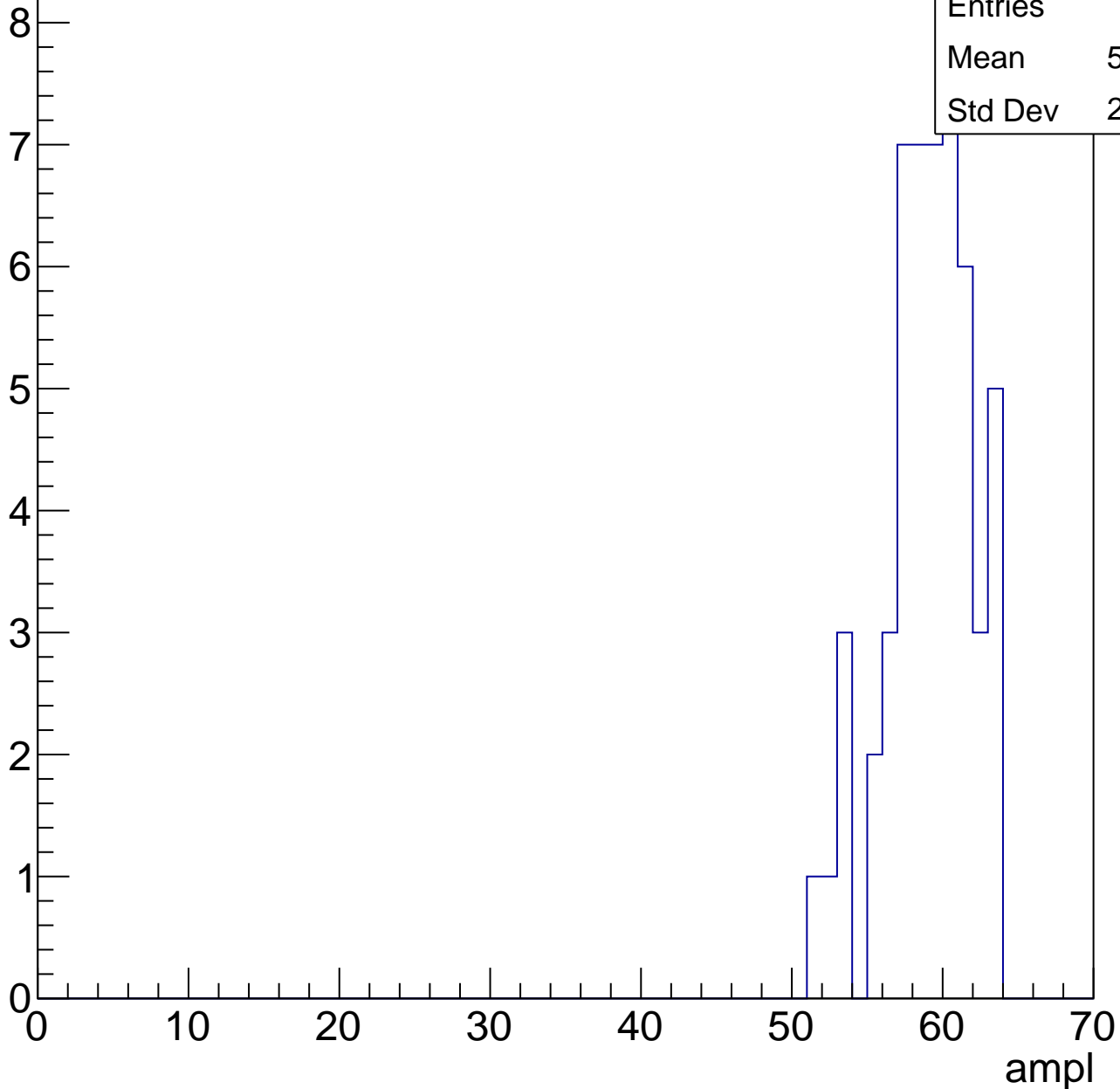


# B0L001S, U24-ch113, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	58.58
Std Dev	2.897

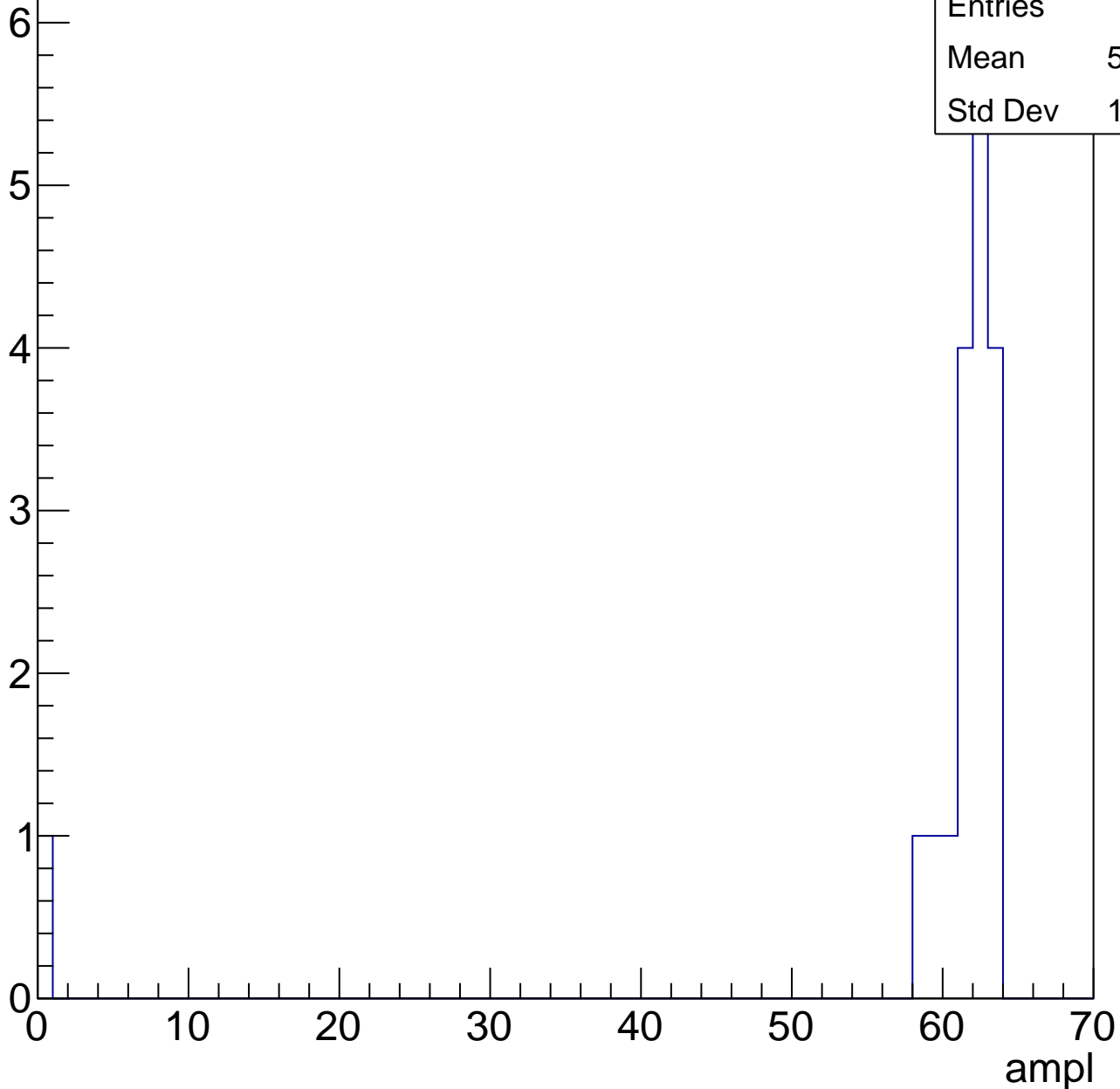


# B0L001S, U24-ch113, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	18
Mean	58.06
Std Dev	14.14



# B0L001S, U24-ch113, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch113, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U24-ch114, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	89
Mean	28.84
Std Dev	7.322

**Gaus mean : 30.7325**

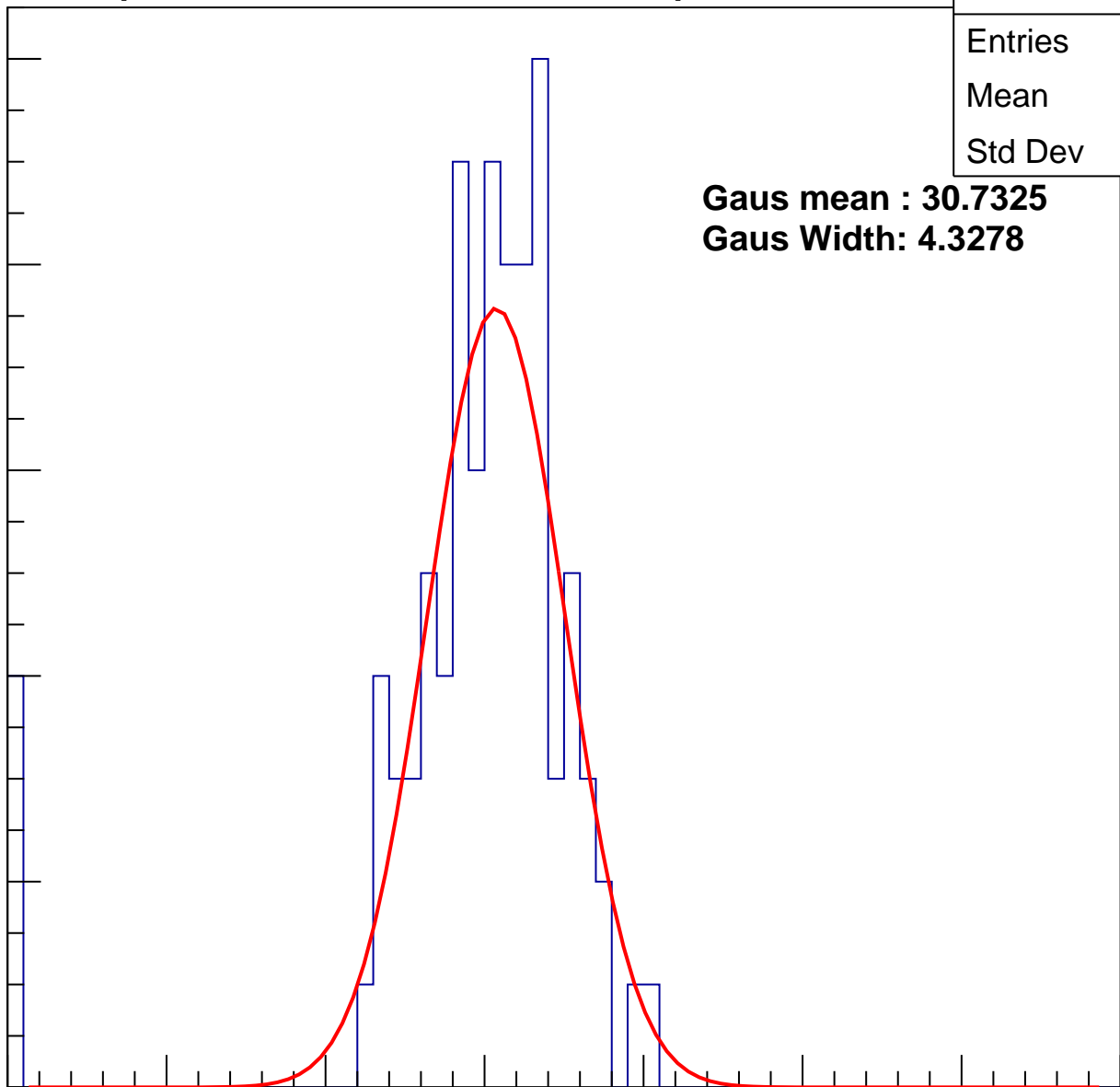
**Gaus Width: 4.3278**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U24-ch114, adc1

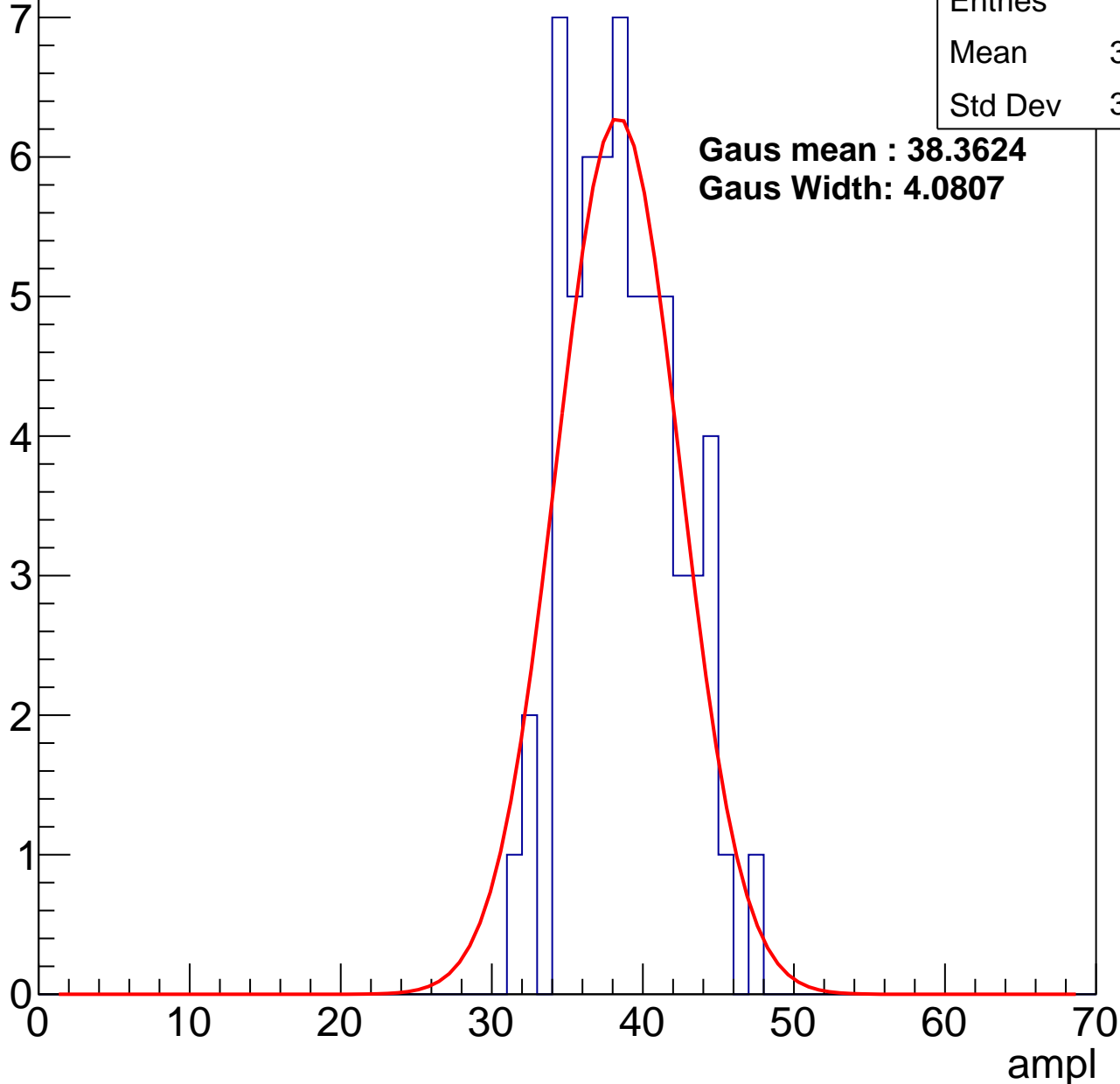
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	38.28
Std Dev	3.553

**Gaus mean : 38.3624**

**Gaus Width: 4.0807**



# B0L001S, U24-ch114, adc2

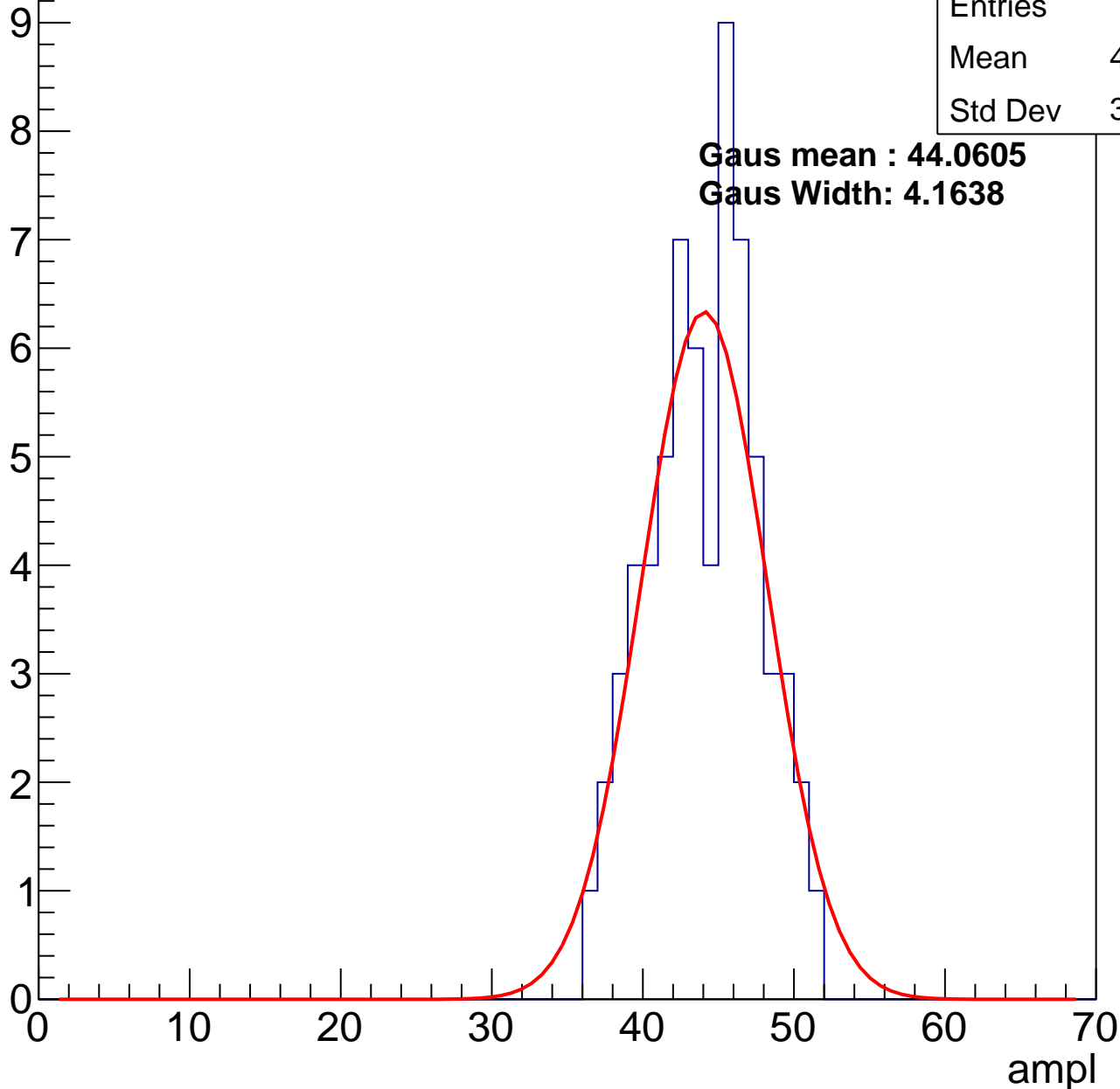
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	43.59
Std Dev	3.542

**Gaus mean : 44.0605**

**Gaus Width: 4.1638**

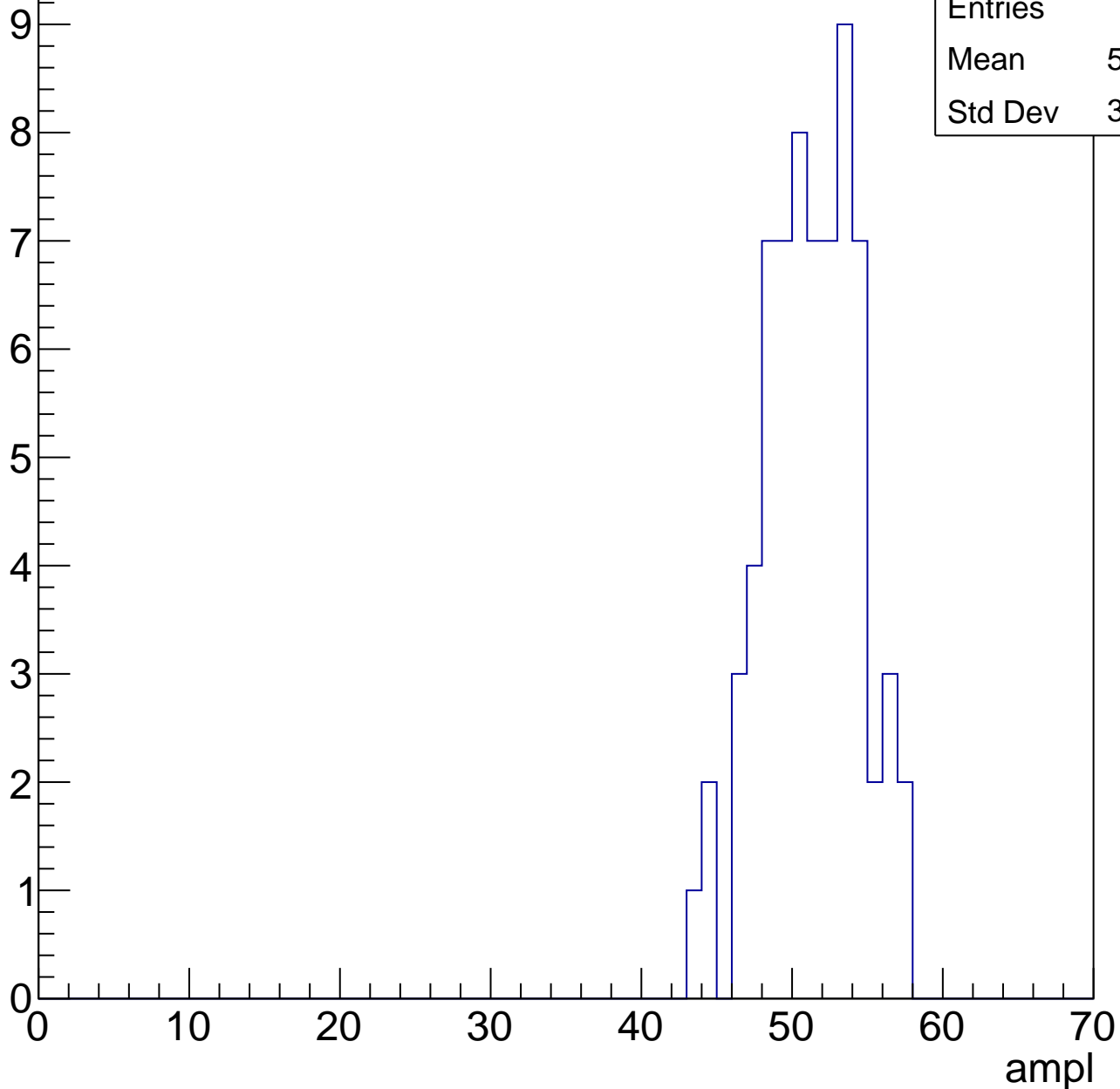


# B0L001S, U24-ch114, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	50.78
Std Dev	3.143

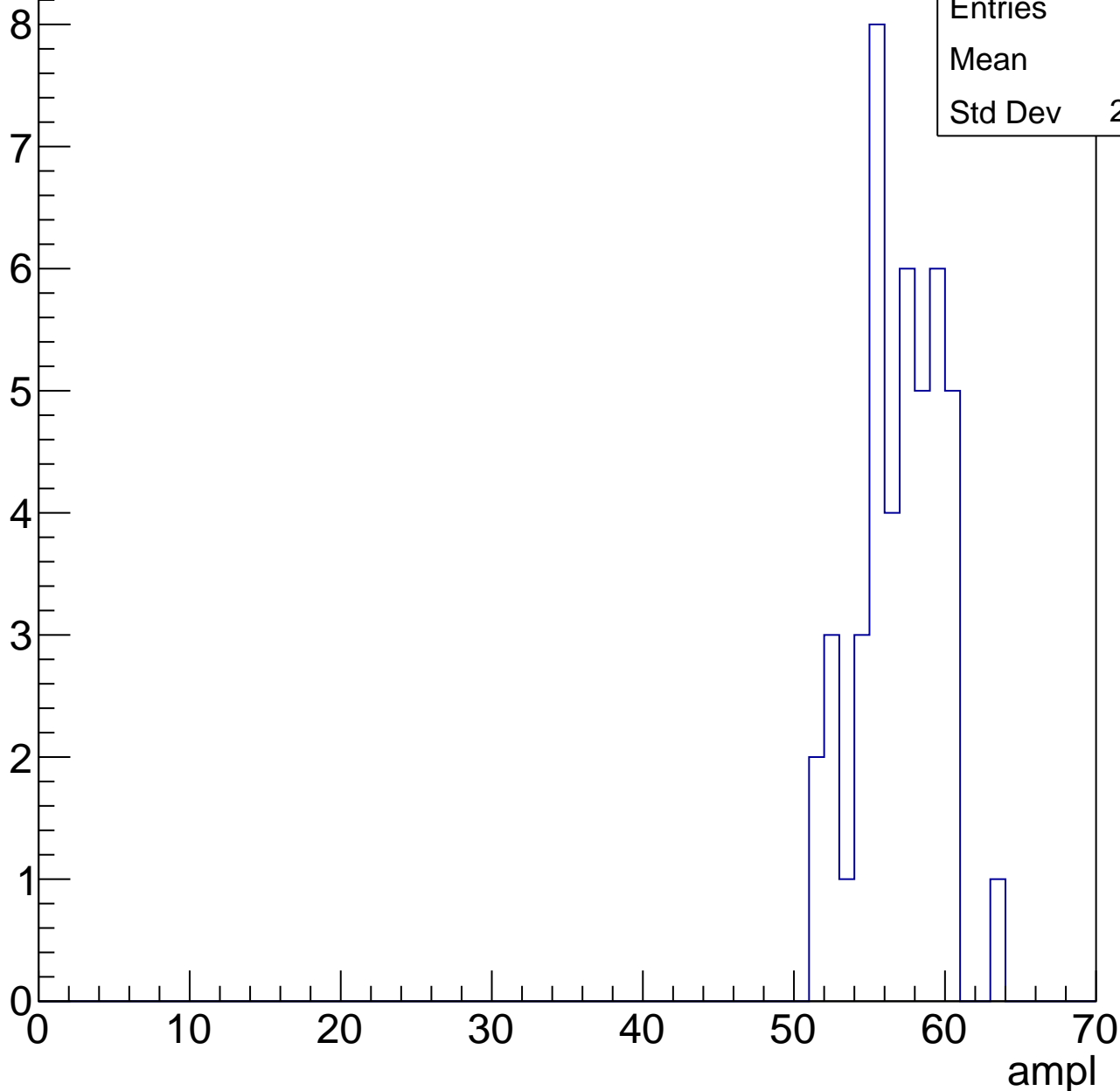


# B0L001S, U24-ch114, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	44
Mean	56.5
Std Dev	2.718



# B0L001S, U24-ch114, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

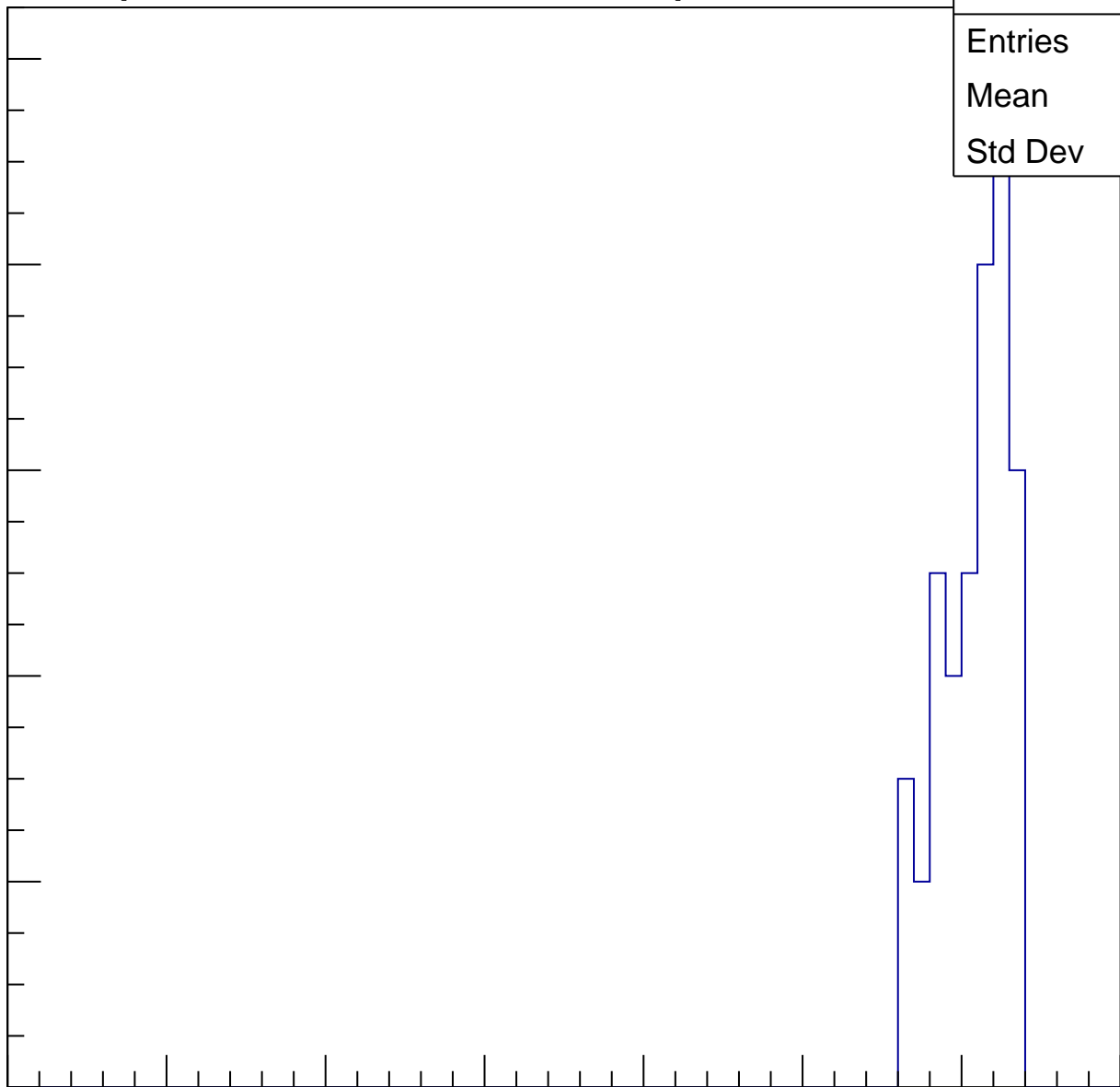
Entries	43
Mean	60.33
Std Dev	2.088

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

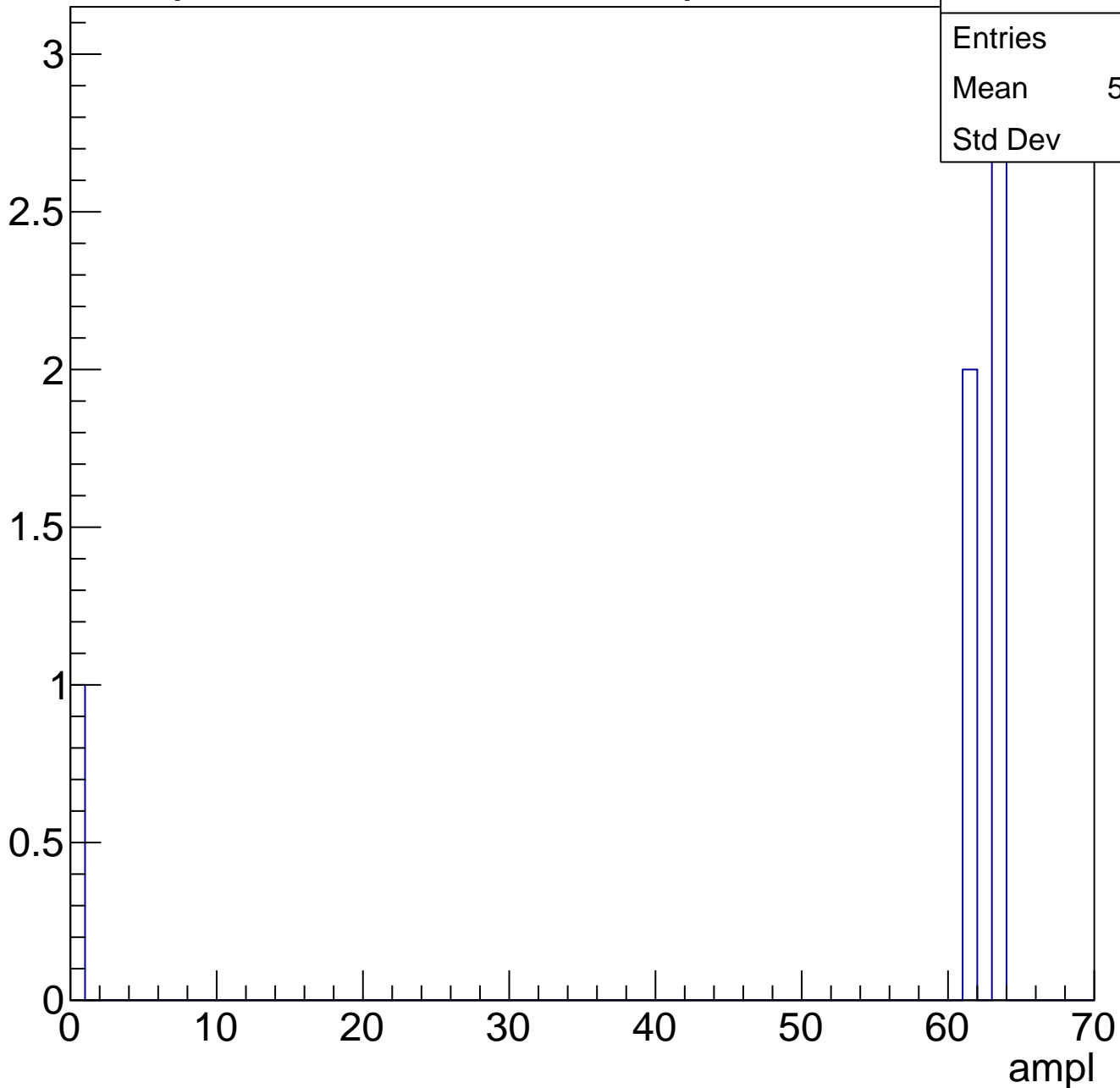
ampl



# B0L001S, U24-ch114, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



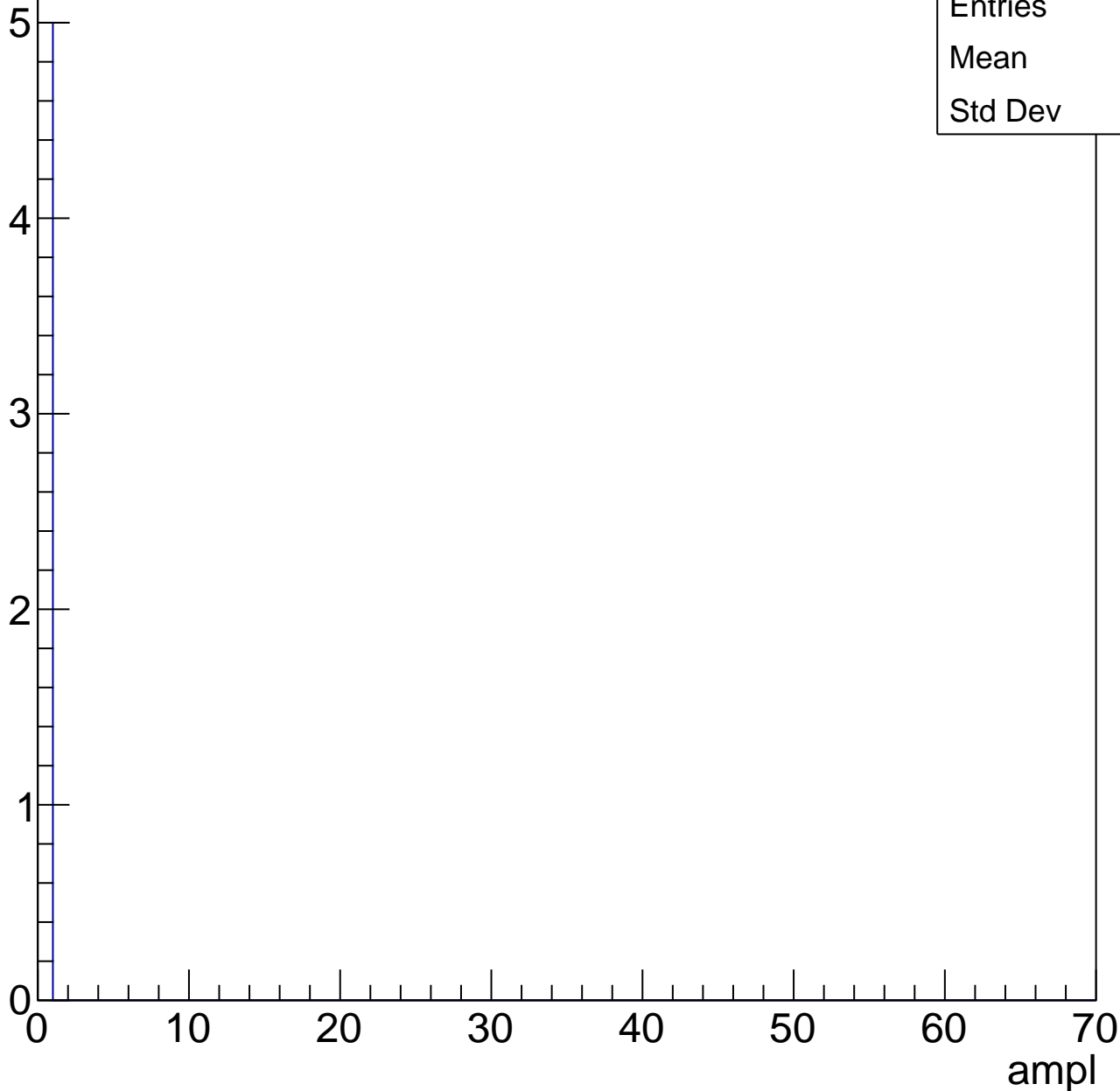


# B0L001S, U24-ch114, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	5
Mean	0
Std Dev	0



# B0L001S, U24-ch115, adc0

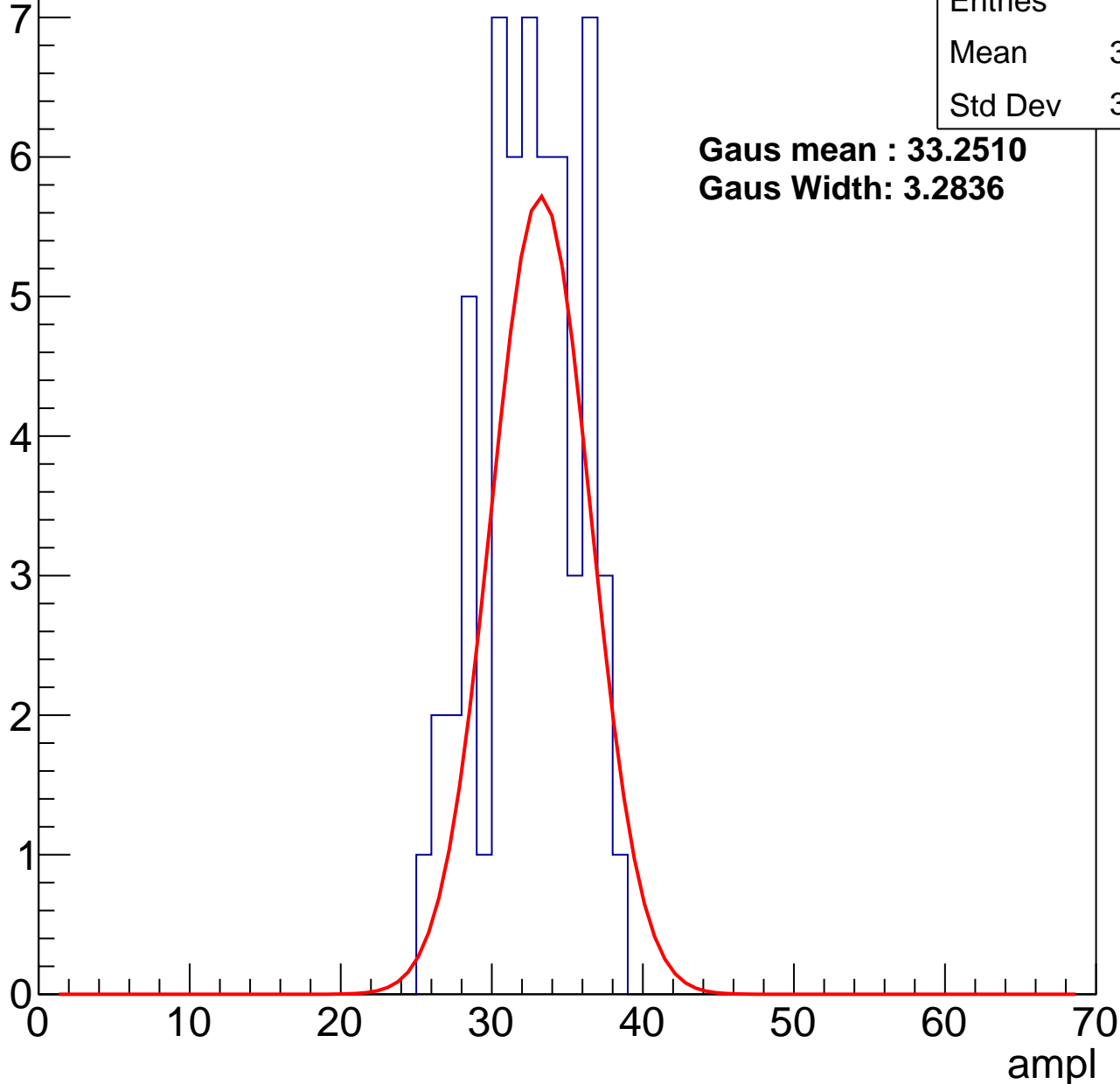
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	32.07
Std Dev	3.173

**Gaus mean : 33.2510**

**Gaus Width: 3.2836**



# B0L001S, U24-ch115, adc1

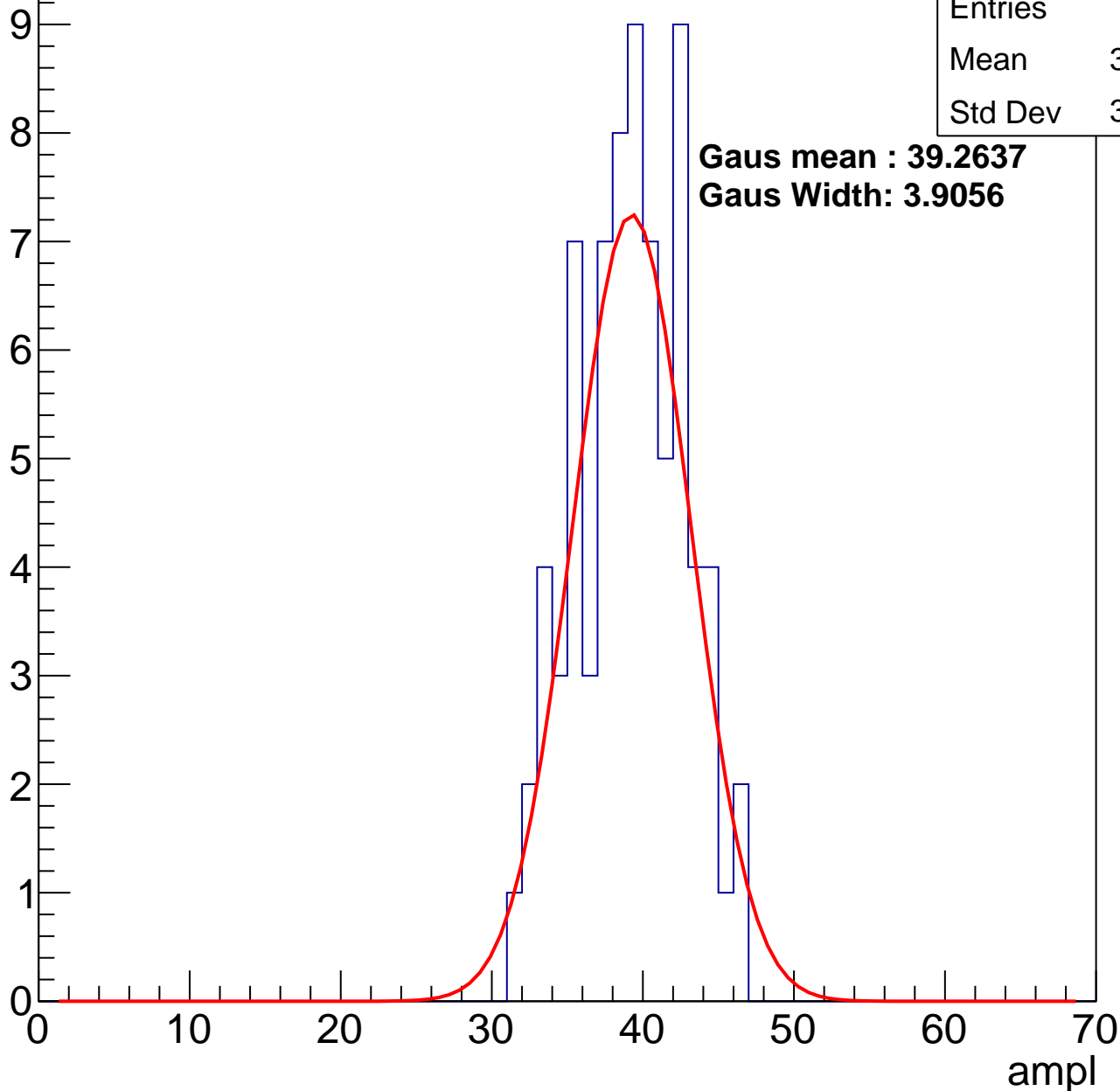
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	76
Mean	38.74
Std Dev	3.548

**Gaus mean : 39.2637**

**Gaus Width: 3.9056**



# B0L001S, U24-ch115, adc2

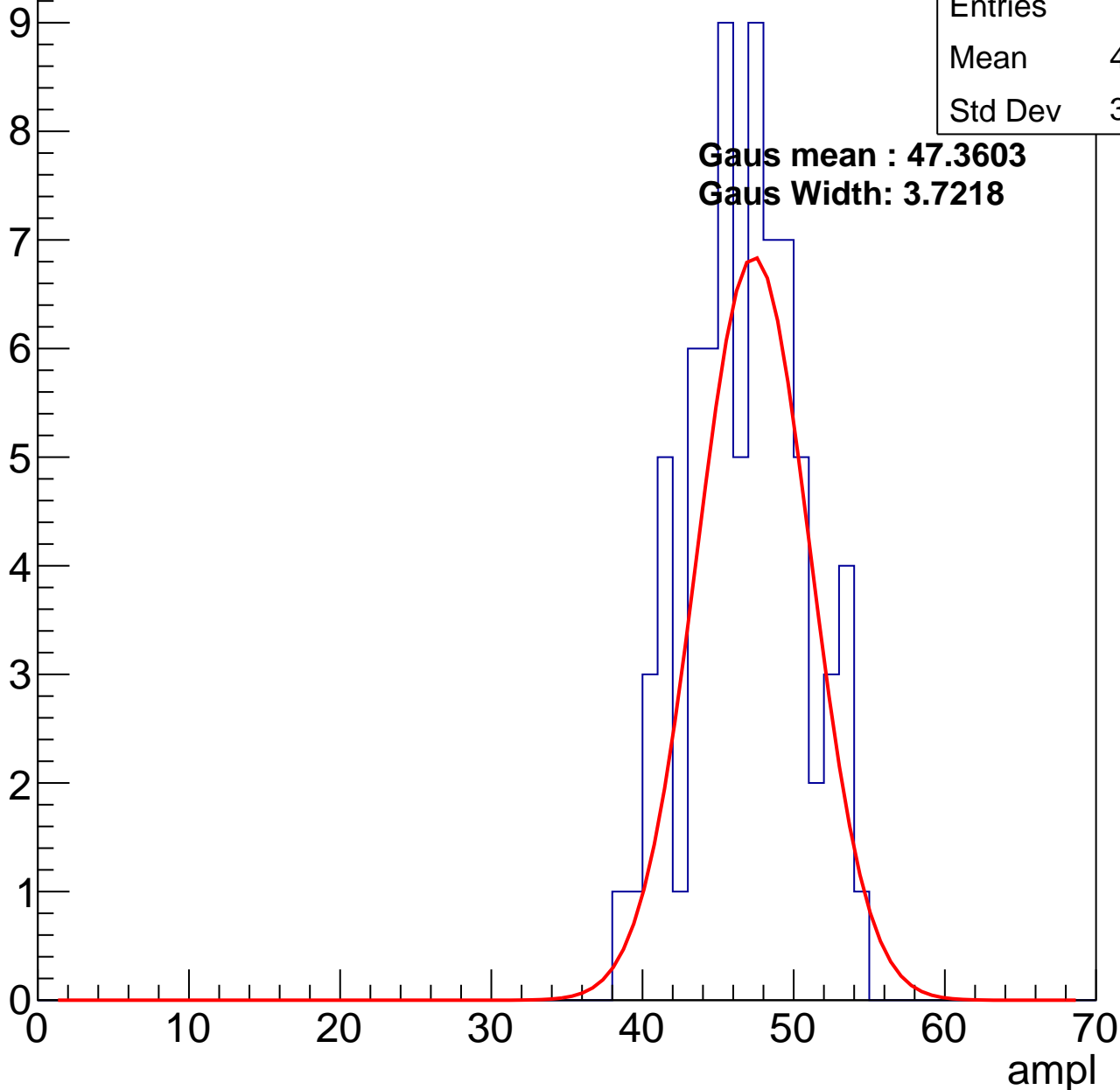
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	75
Mean	46.36
Std Dev	3.719

**Gaus mean : 47.3603**

**Gaus Width: 3.7218**

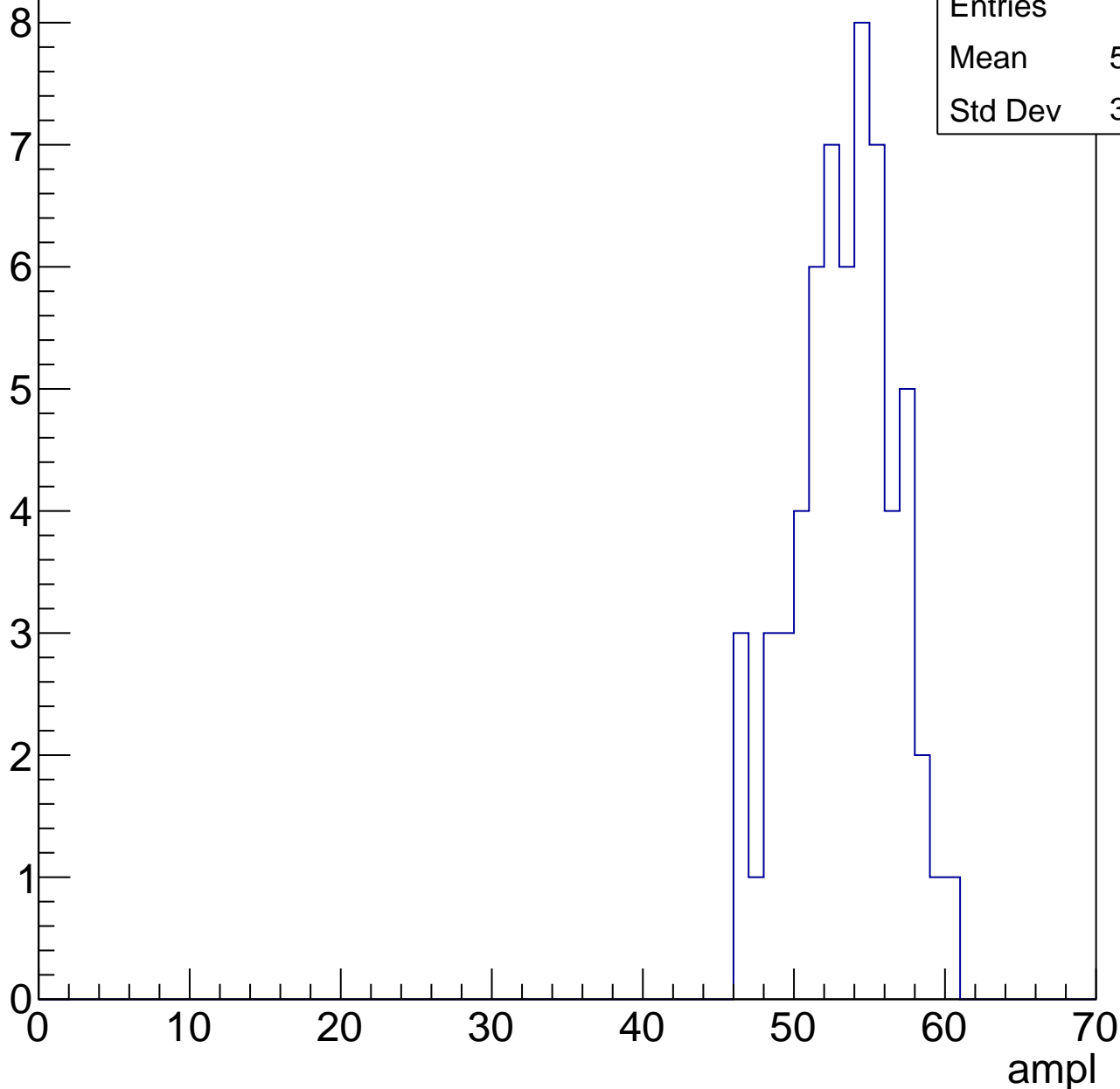


# B0L001S, U24-ch115, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	52.87
Std Dev	3.287

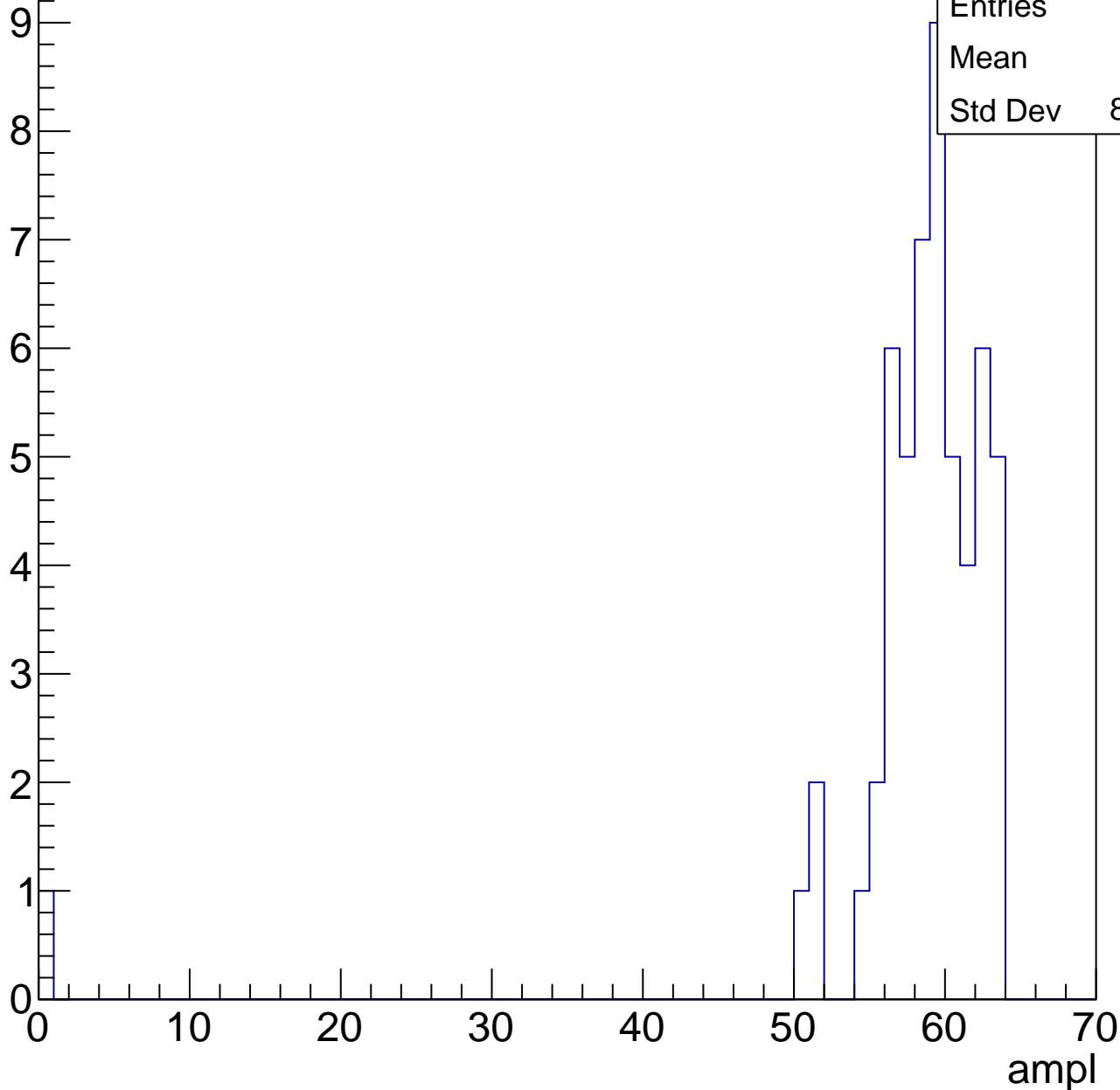


# B0L001S, U24-ch115, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	57.5
Std Dev	8.456

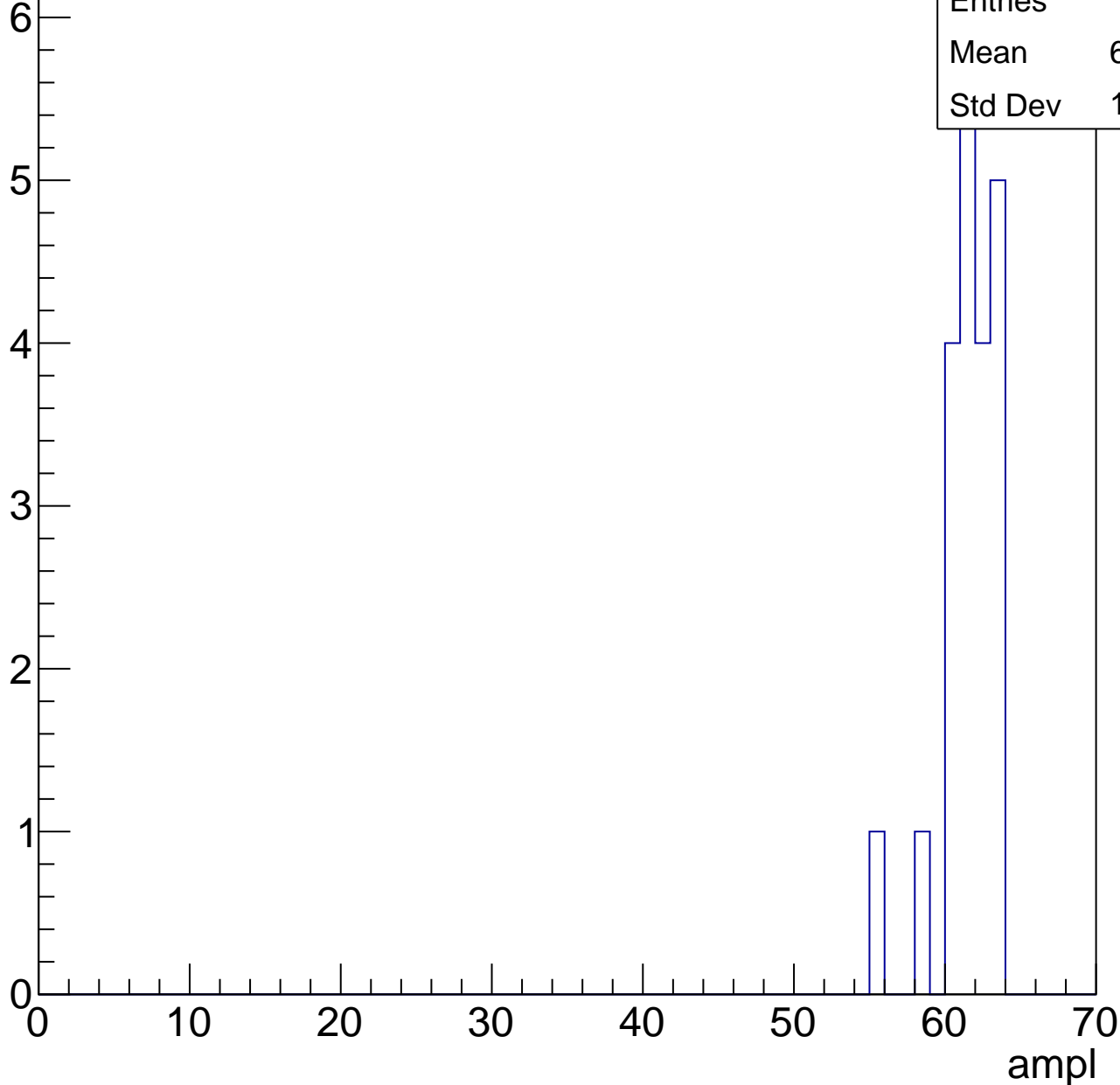


# B0L001S, U24-ch115, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	21
Mean	61.05
Std Dev	1.864



# B0L001S, U24-ch115, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U24-ch115, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U24-ch116, adc0

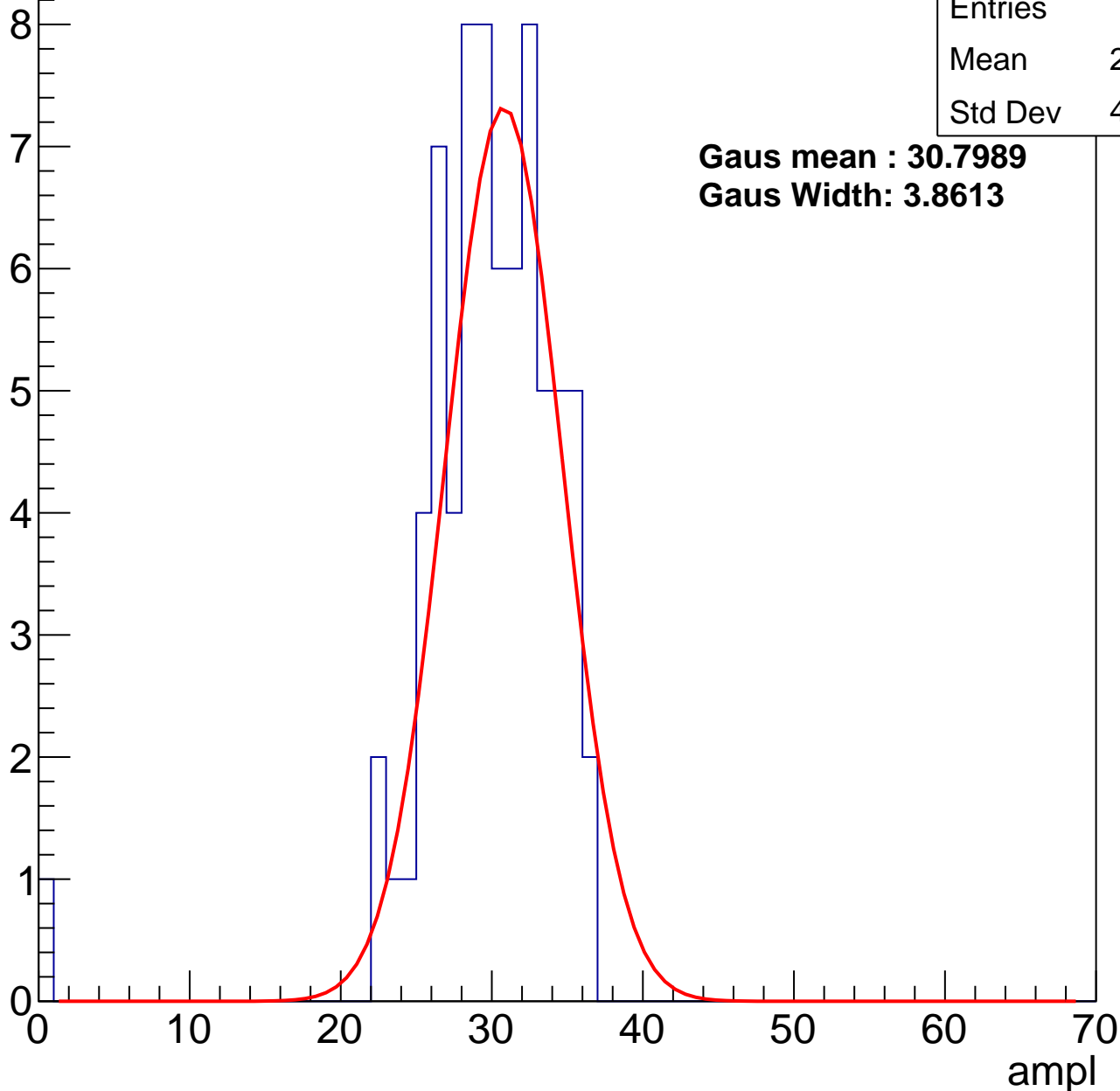
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	29.33
Std Dev	4.865

**Gaus mean : 30.7989**

**Gaus Width: 3.8613**



# B0L001S, U24-ch116, adc1

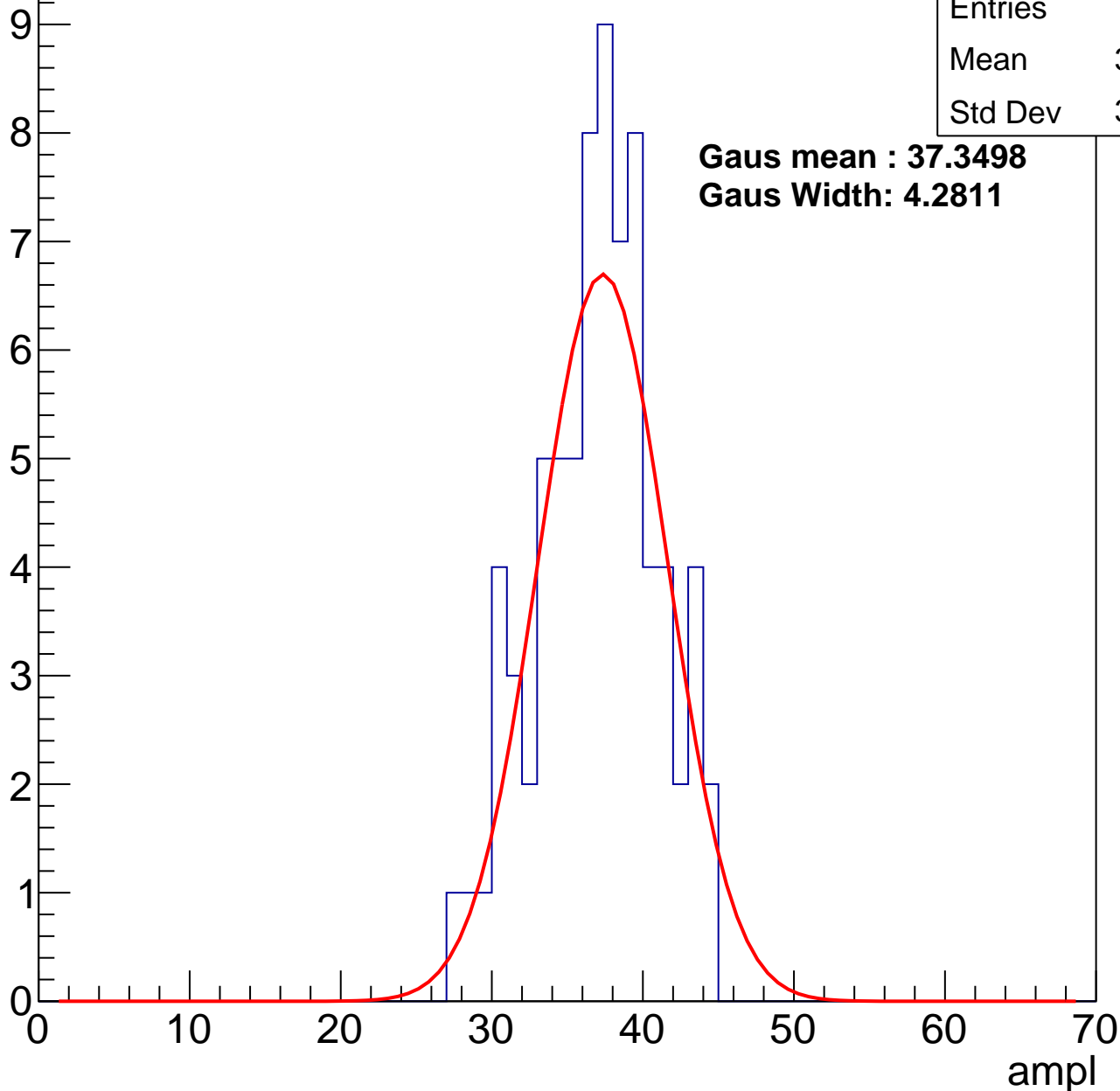
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	75
Mean	36.51
Std Dev	3.941

**Gaus mean : 37.3498**

**Gaus Width: 4.2811**



# B0L001S, U24-ch116, adc2

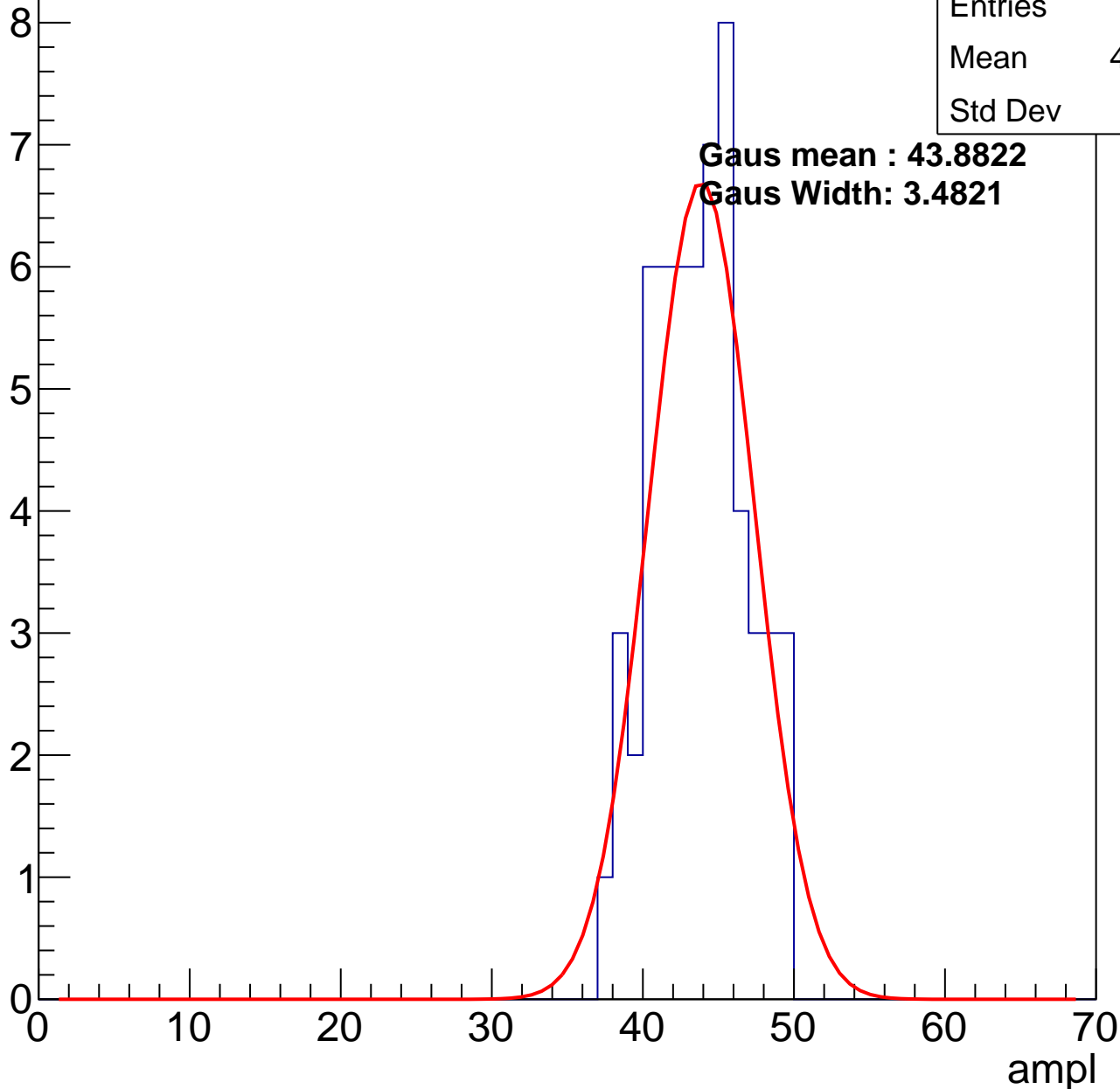
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	43.26
Std Dev	3.02

**Gaus mean : 43.8822**

**Gaus Width: 3.4821**

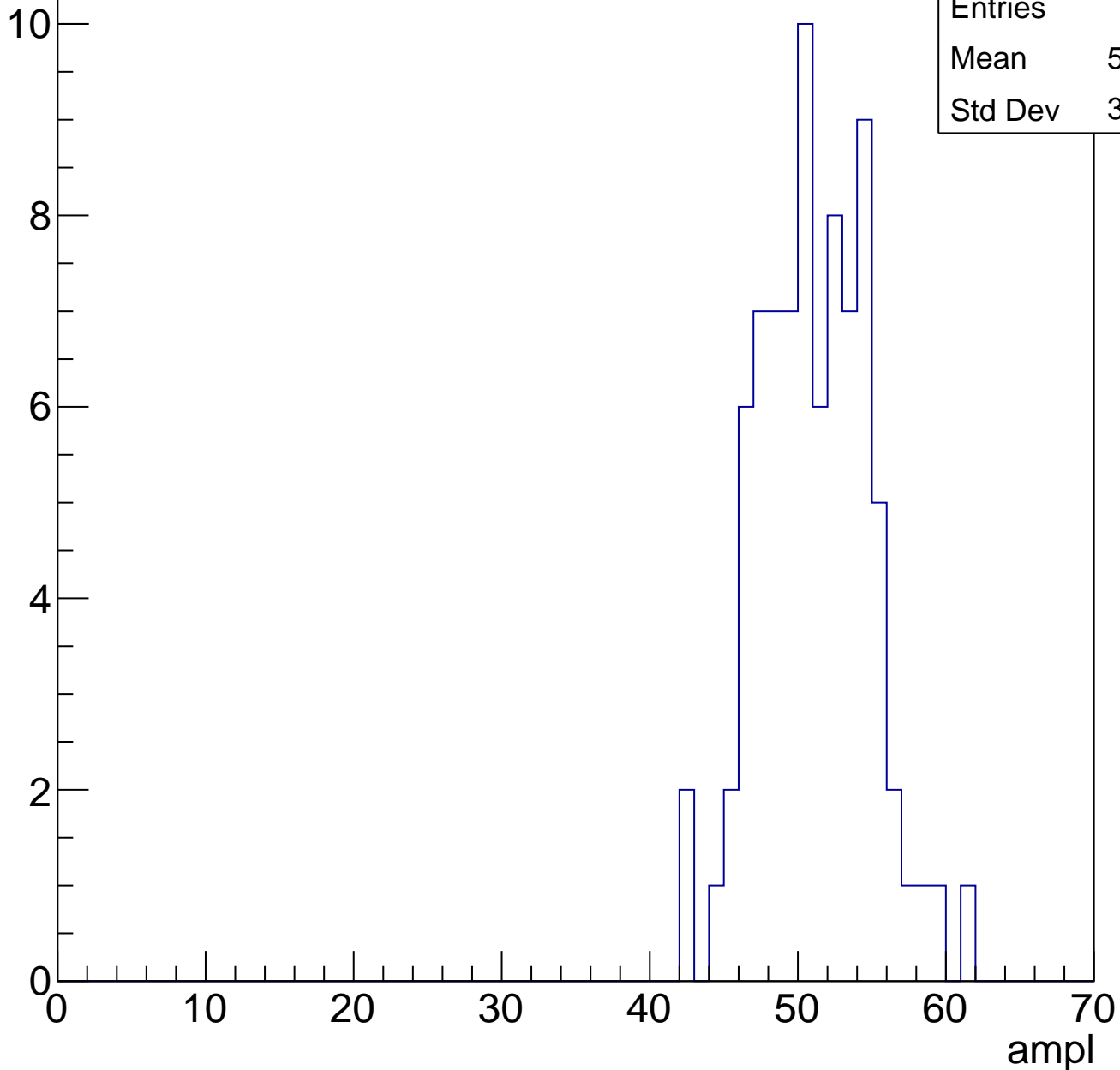


# B0L001S, U24-ch116, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	83
Mean	50.64
Std Dev	3.692

Entry

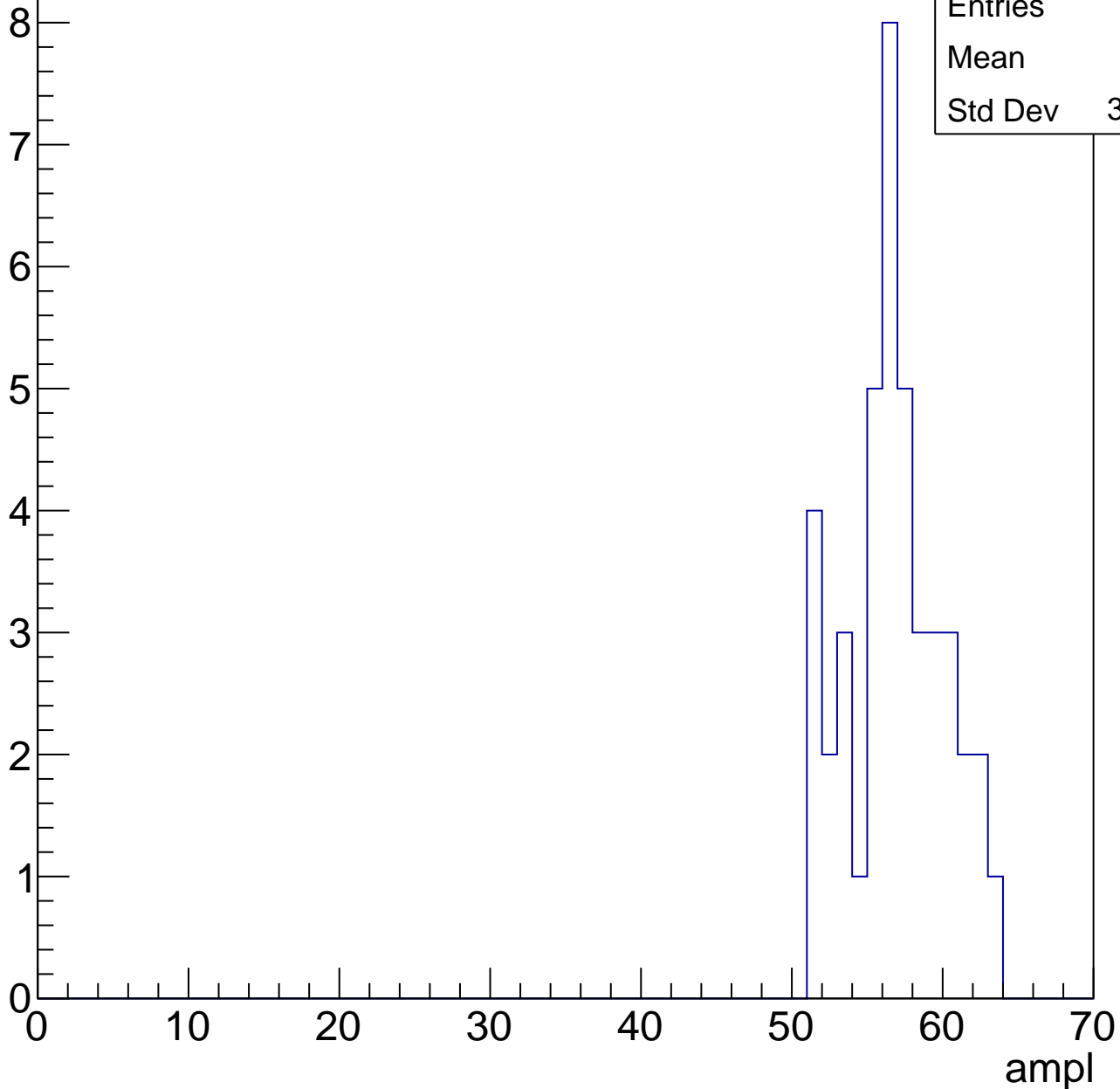


# B0L001S, U24-ch116, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	42
Mean	56.4
Std Dev	3.178

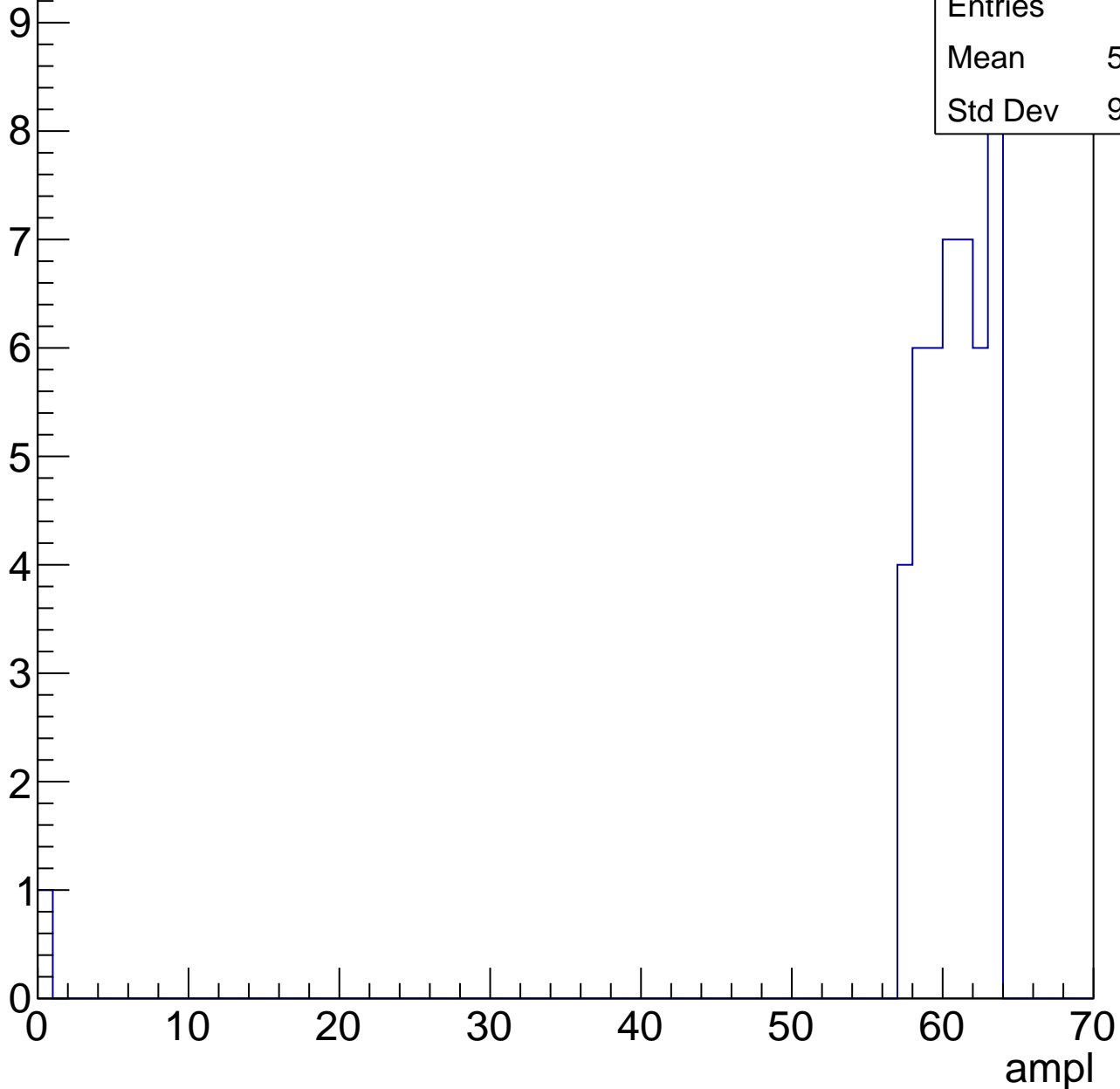


# B0L001S, U24-ch116, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	46
Mean	59.04
Std Dev	9.012



# B0L001S, U24-ch116, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch116, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U24-ch117, adc0

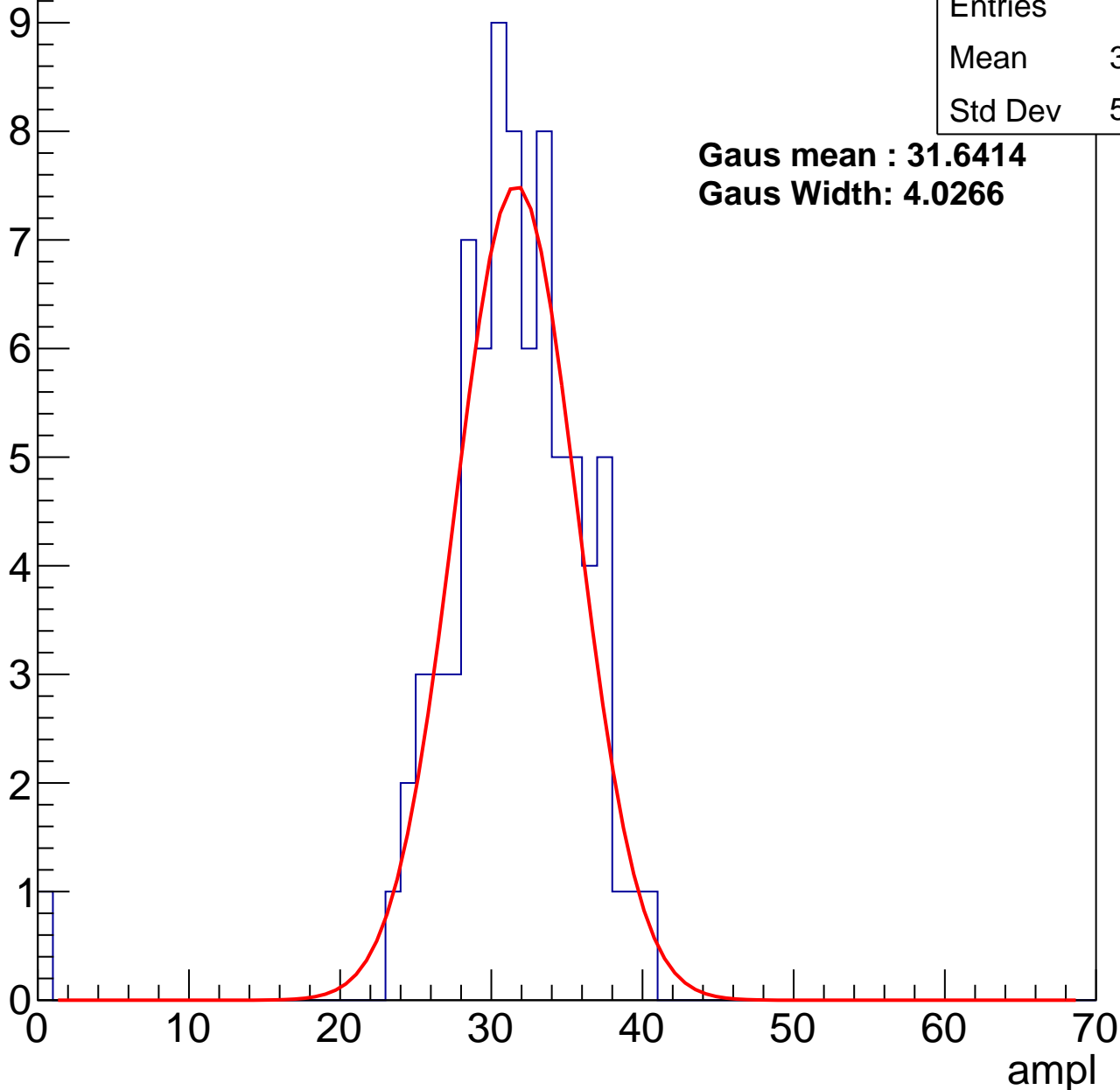
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	79
Mean	30.89
Std Dev	5.139

**Gaus mean : 31.6414**

**Gaus Width: 4.0266**



# B0L001S, U24-ch117, adc1

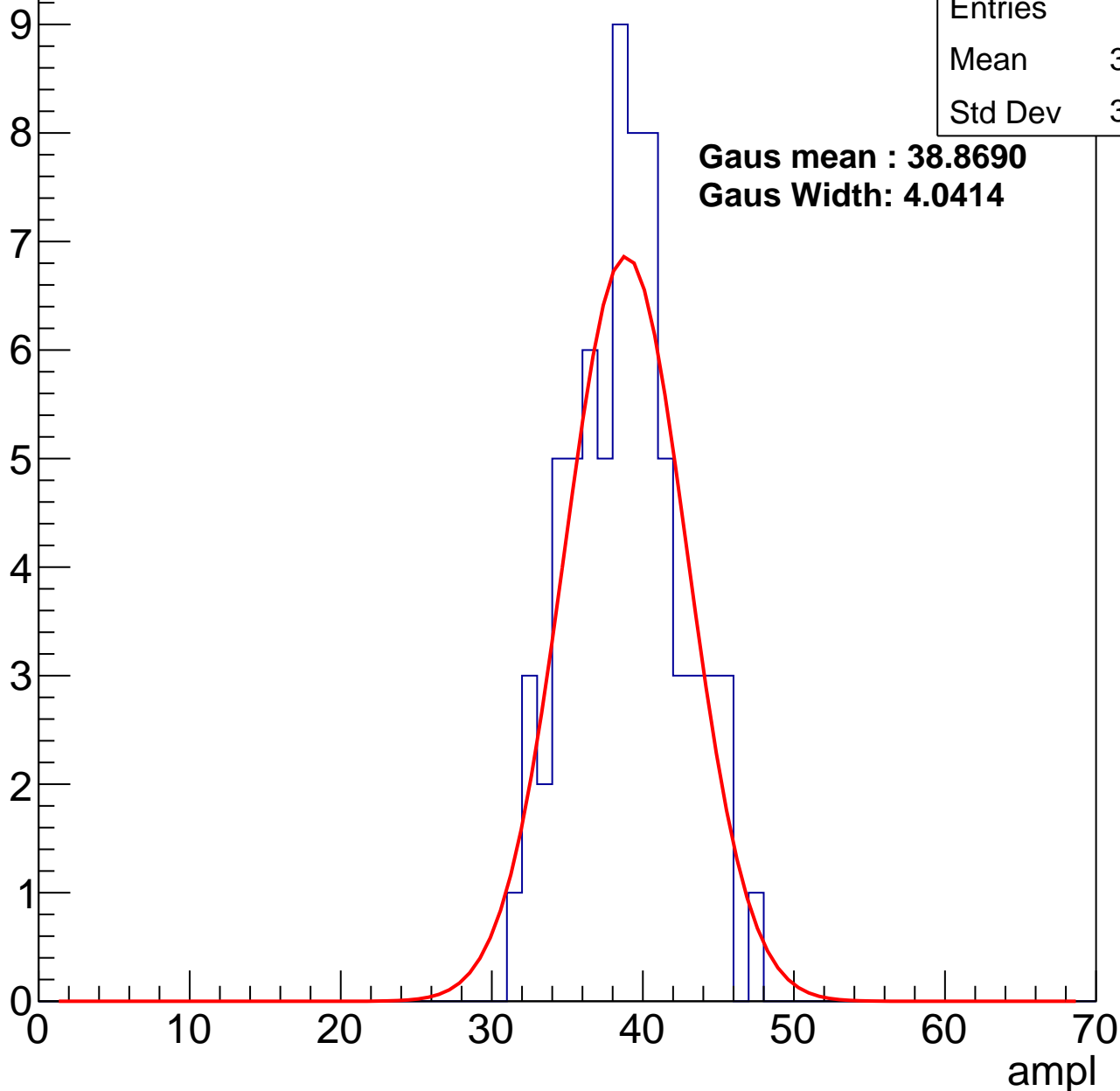
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	38.39
Std Dev	3.575

**Gaus mean : 38.8690**

**Gaus Width: 4.0414**



# B0L001S, U24-ch117, adc2

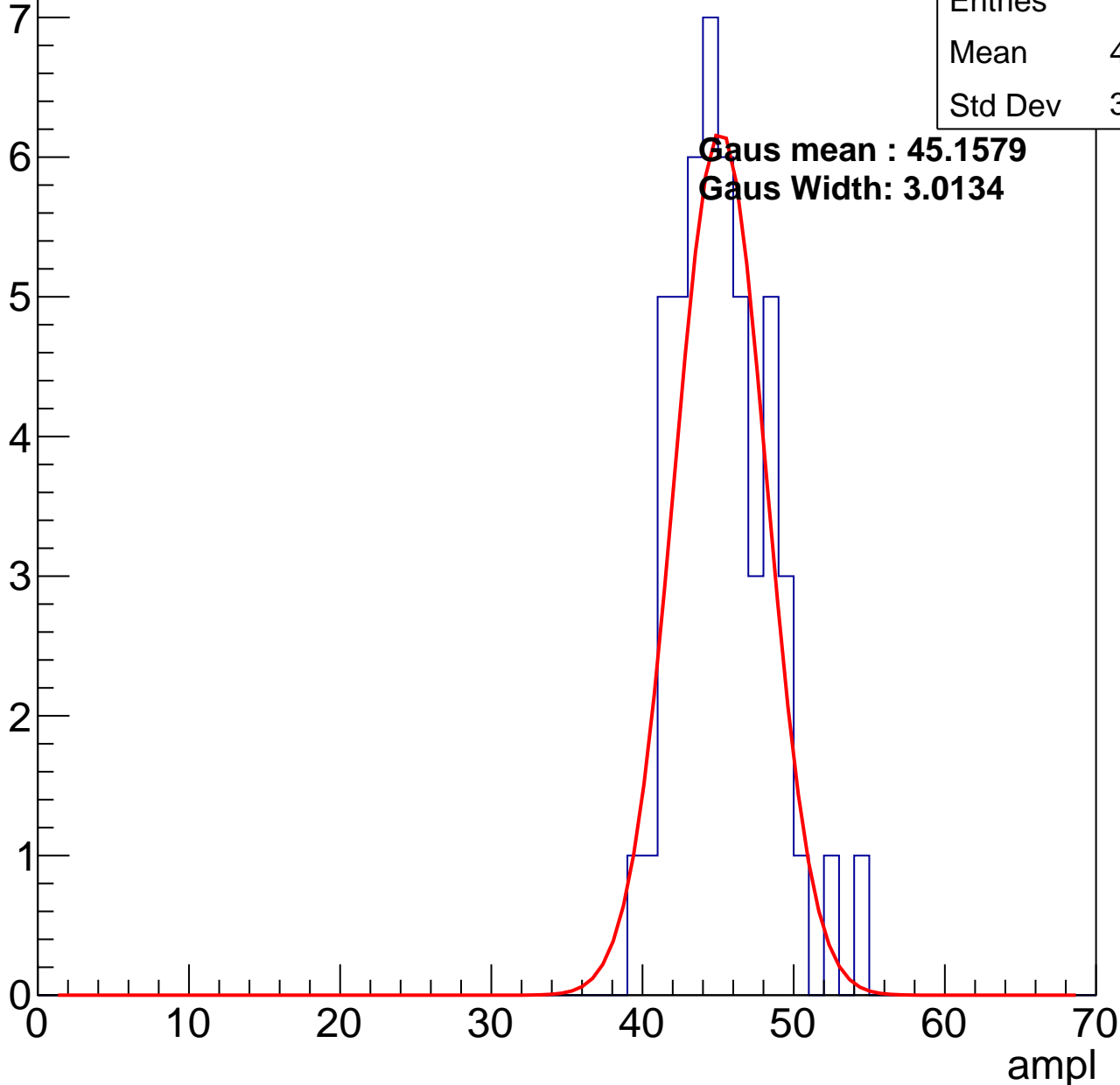
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	50
Mean	44.88
Std Dev	3.103

**Gaus mean : 45.1579**

**Gaus Width: 3.0134**

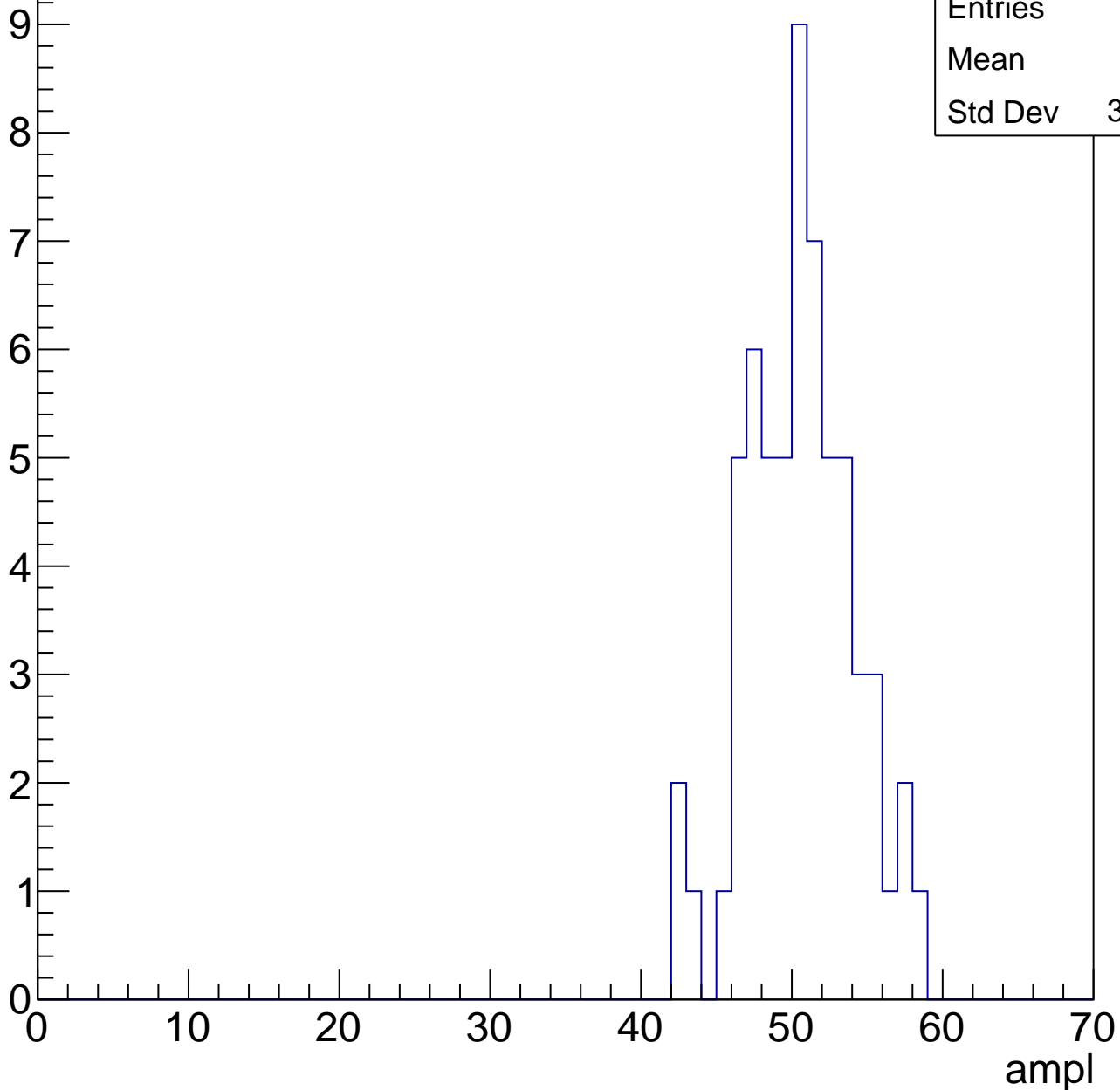


# B0L001S, U24-ch117, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	50.1
Std Dev	3.514



# B0L001S, U24-ch117, adc4

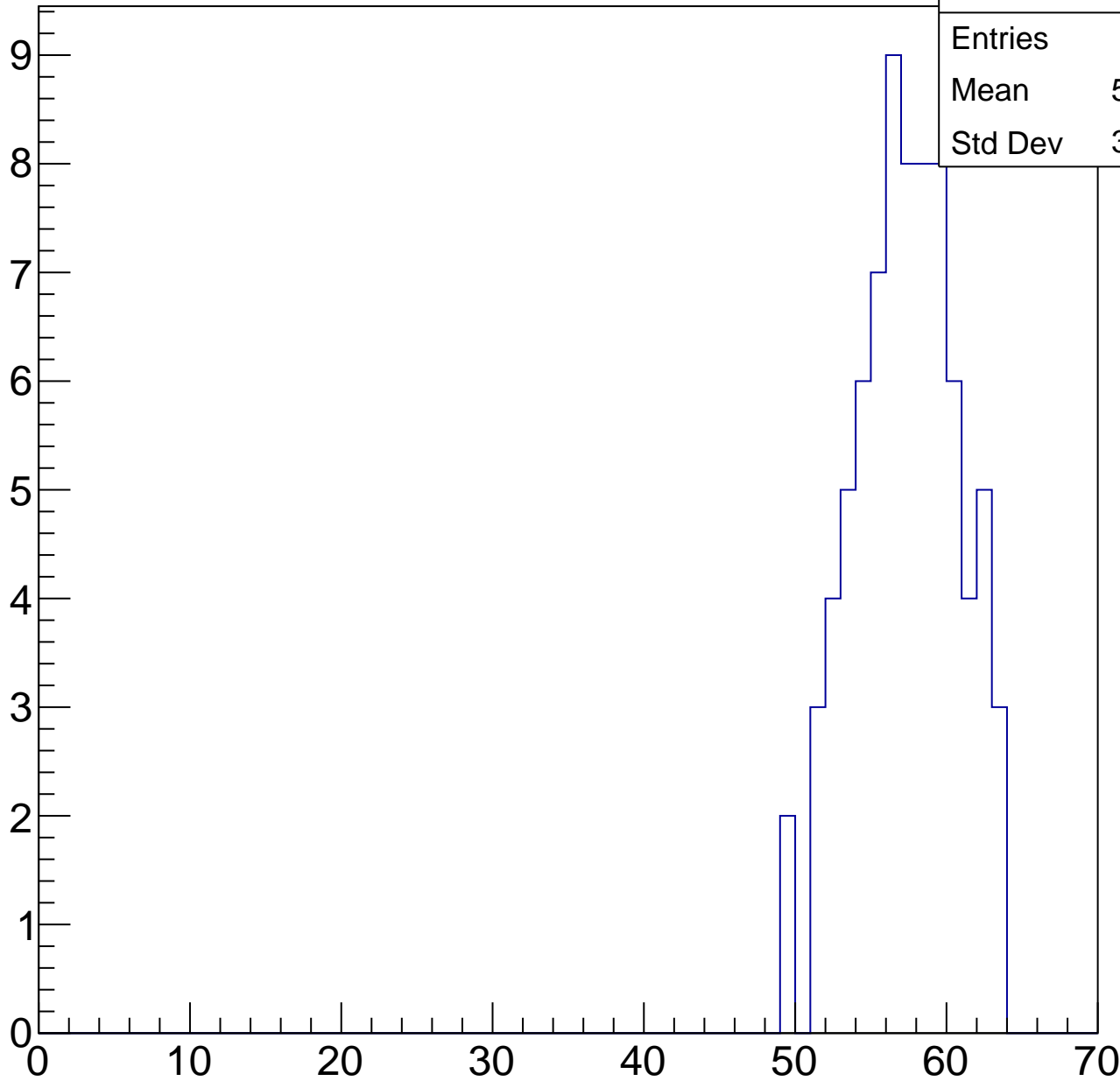
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	78
Mean	56.82
Std Dev	3.388

ampl

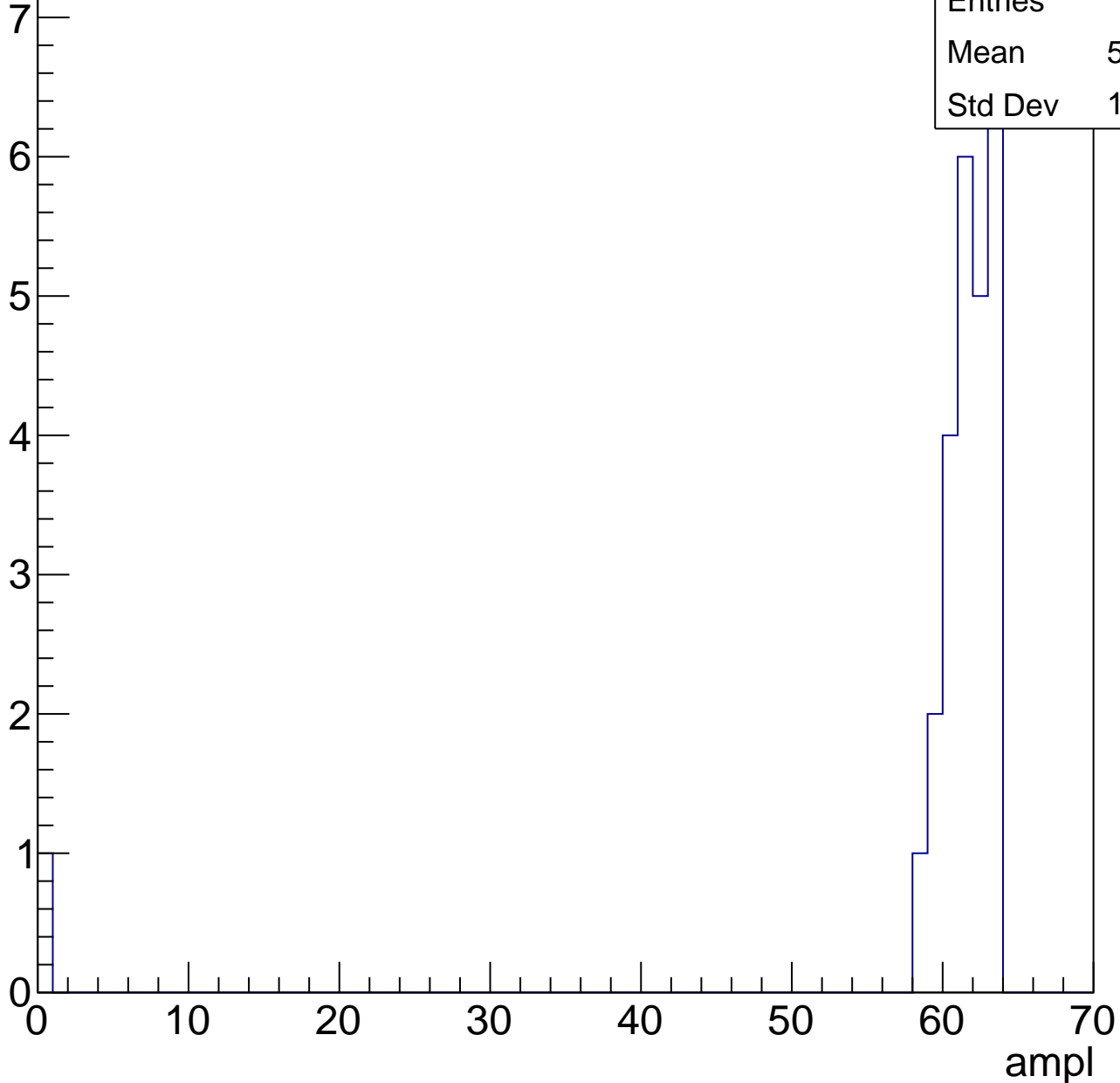


# B0L001S, U24-ch117, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	26
Mean	58.96
Std Dev	11.88



# B0L001S, U24-ch117, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



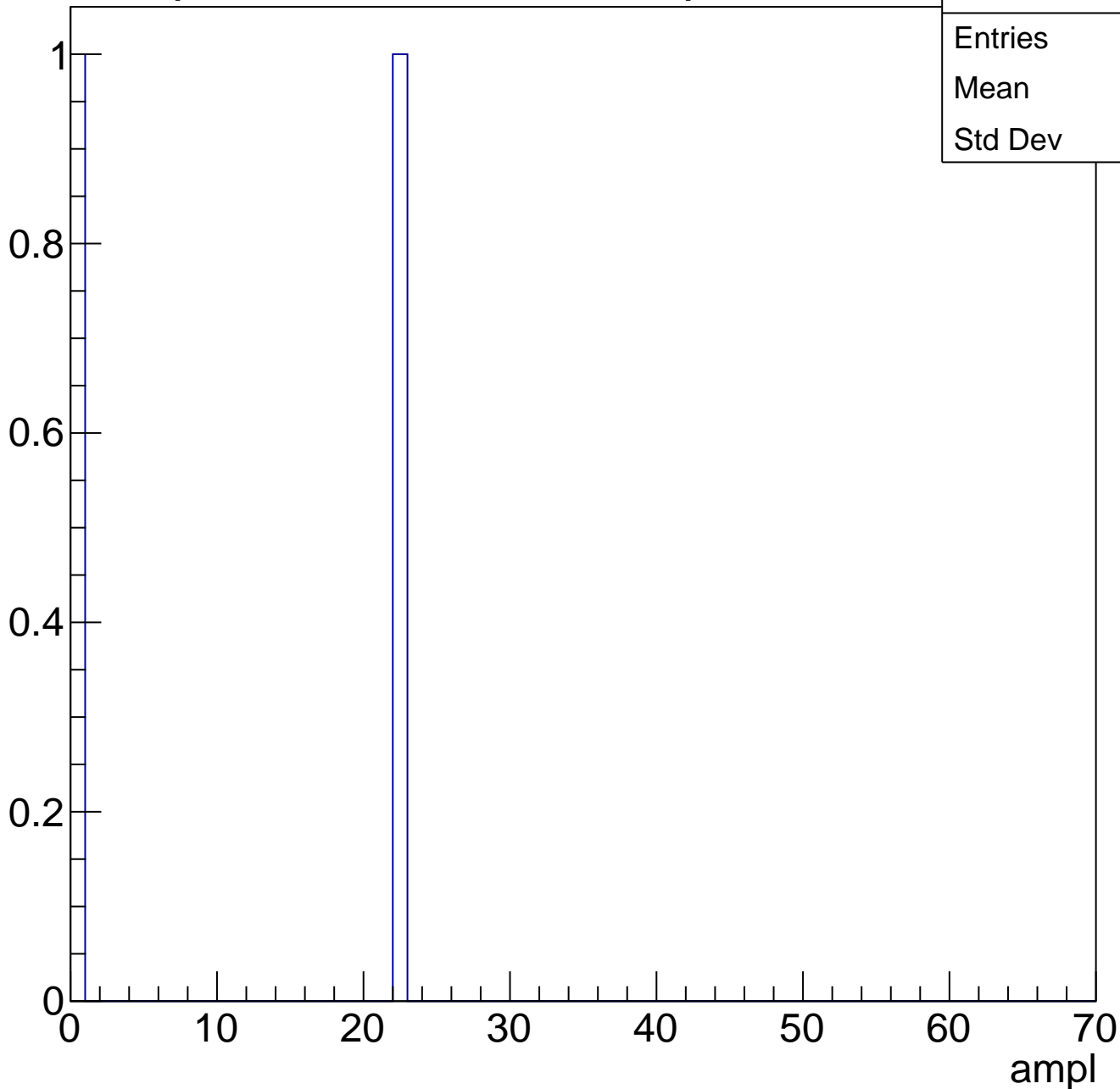
Entries	0
Mean	0
Std Dev	0



# B0L001S, U24-ch117, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U24-ch118, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	76
Mean	29.68
Std Dev	5.989

**Gaus mean : 31.1025**

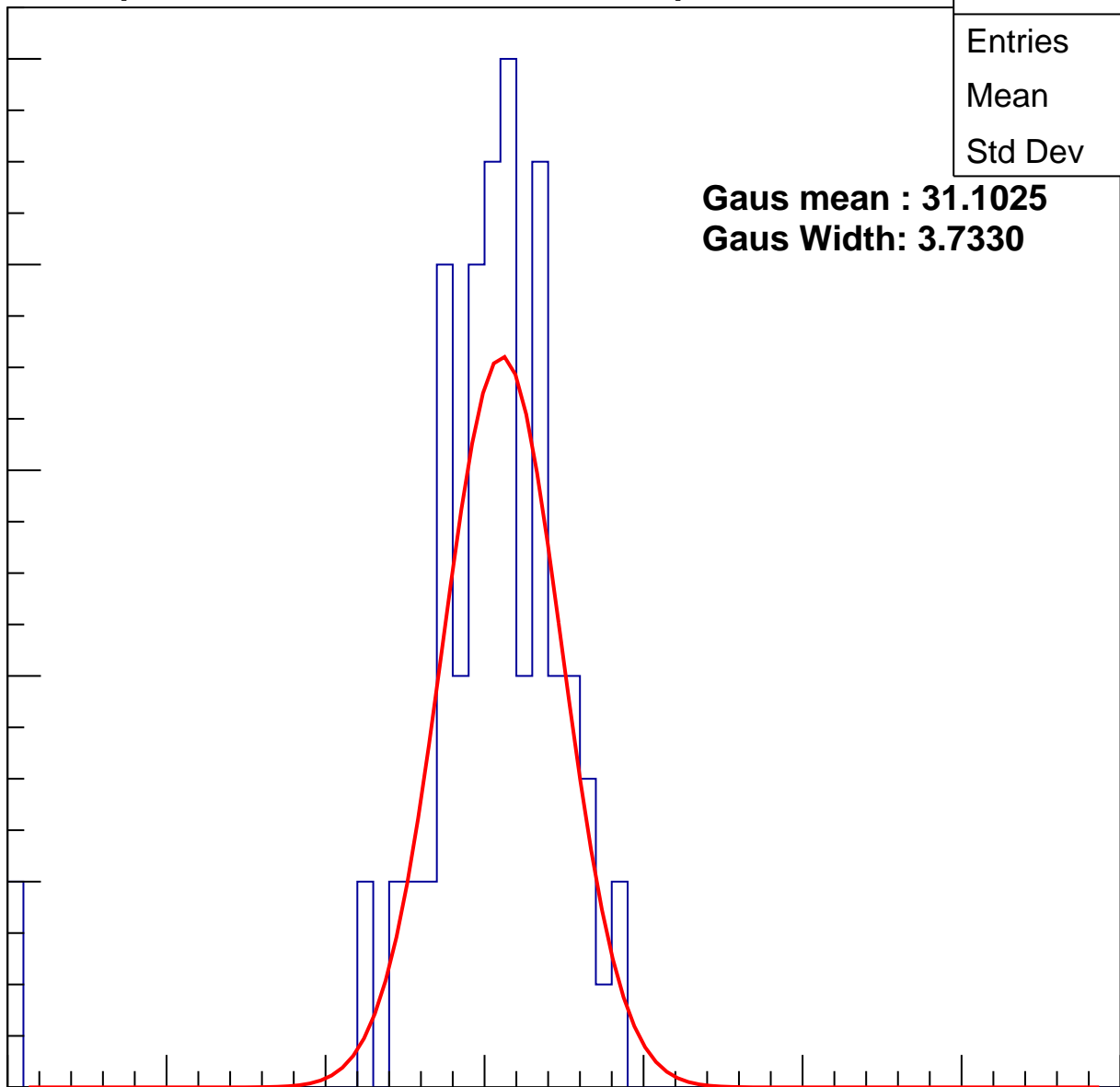
**Gaus Width: 3.7330**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U24-ch118, adc1

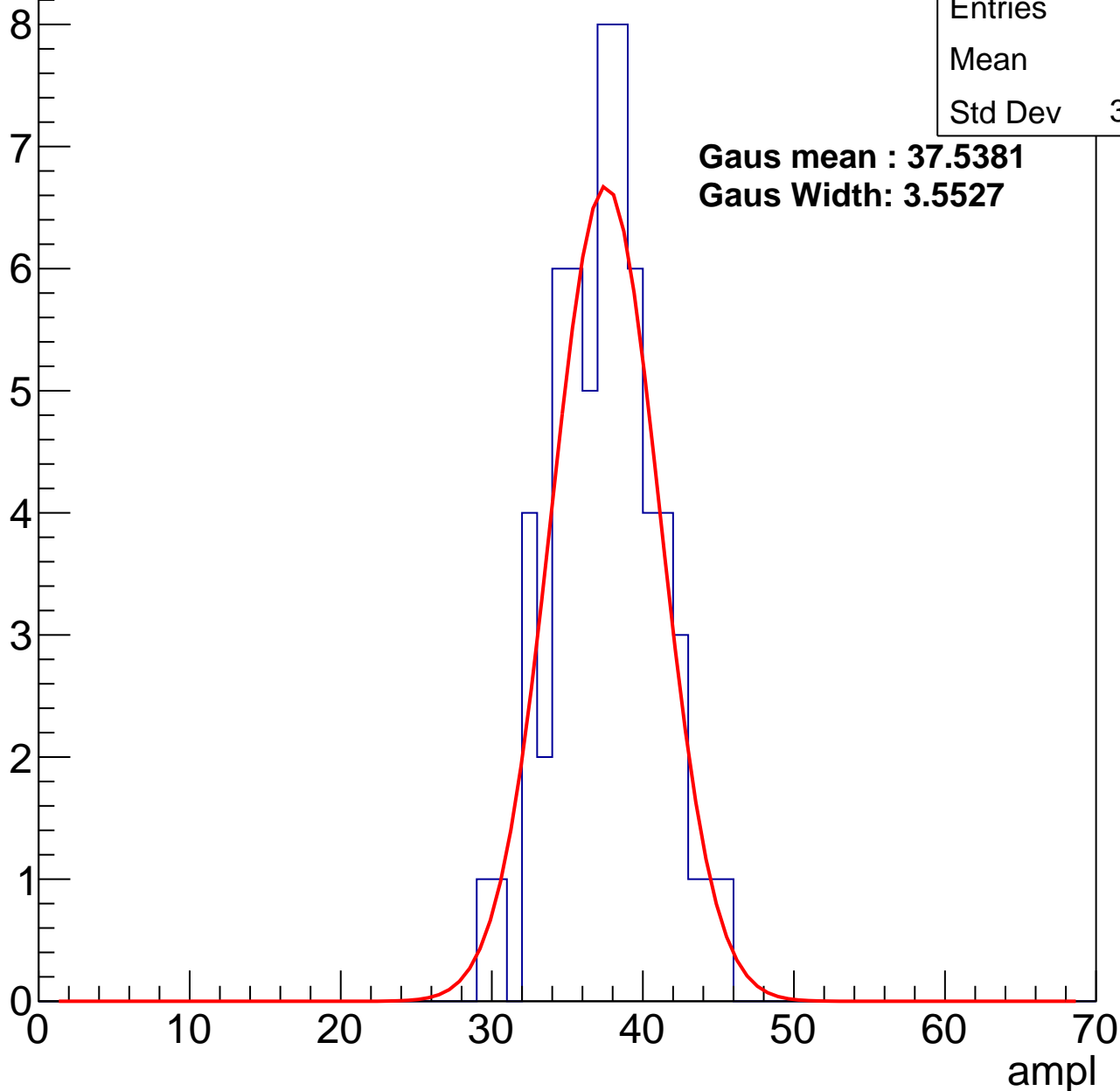
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	37.1
Std Dev	3.347

**Gaus mean : 37.5381**

**Gaus Width: 3.5527**



# B0L001S, U24-ch118, adc2

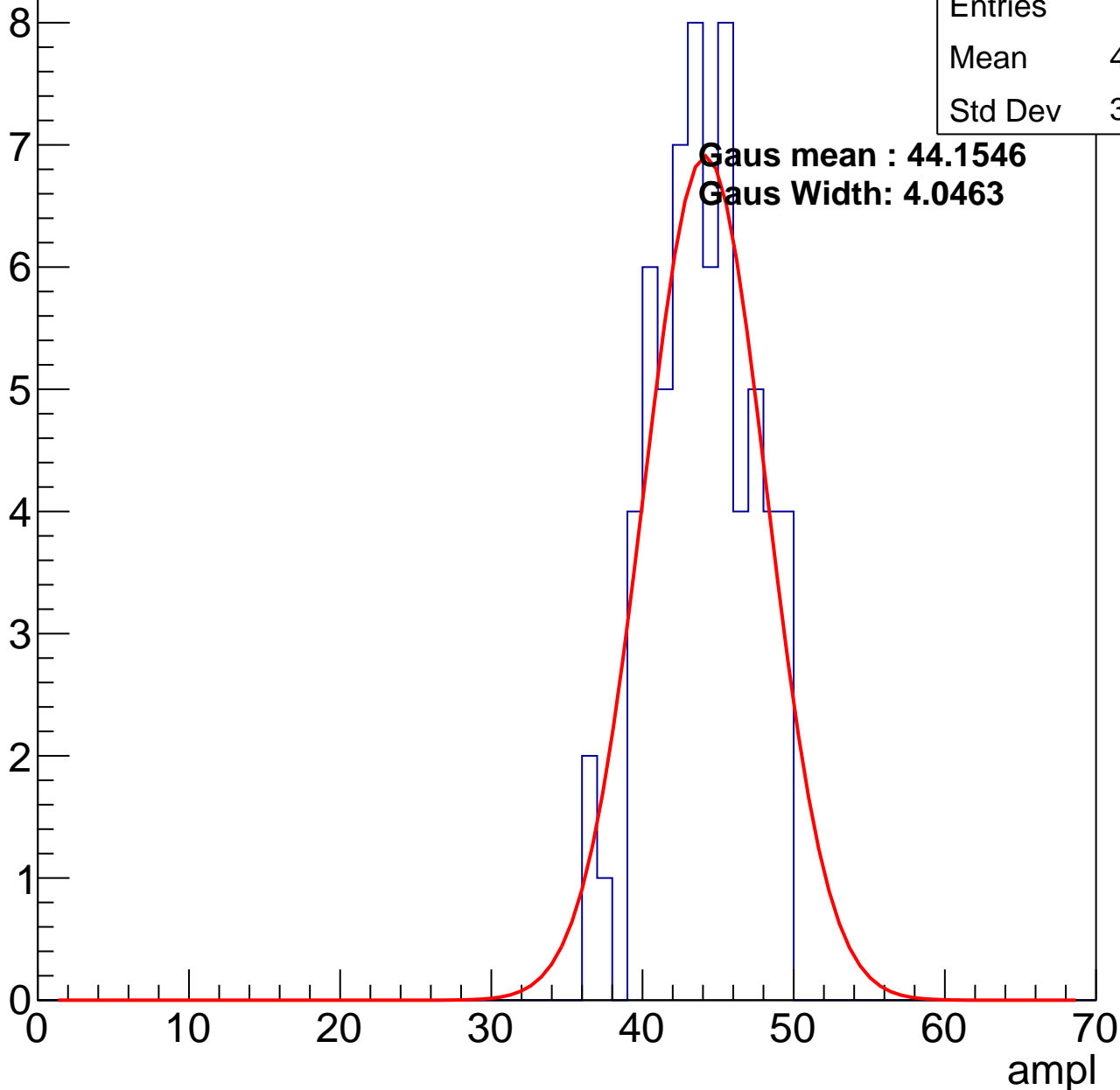
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	43.42
Std Dev	3.225

**Gaus mean : 44.1546**

**Gaus Width: 4.0463**

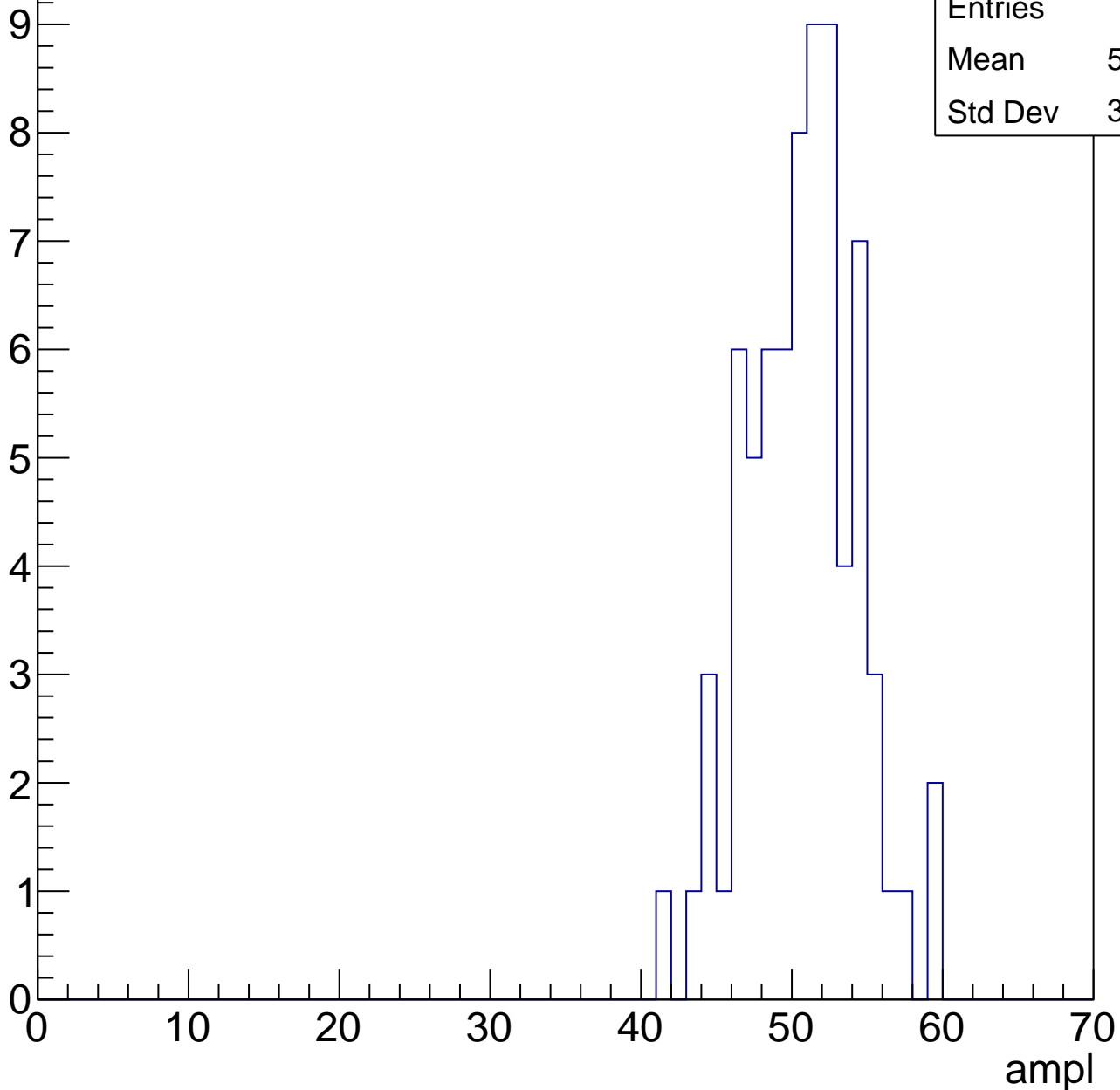


# B0L001S, U24-ch118, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	50.23
Std Dev	3.598

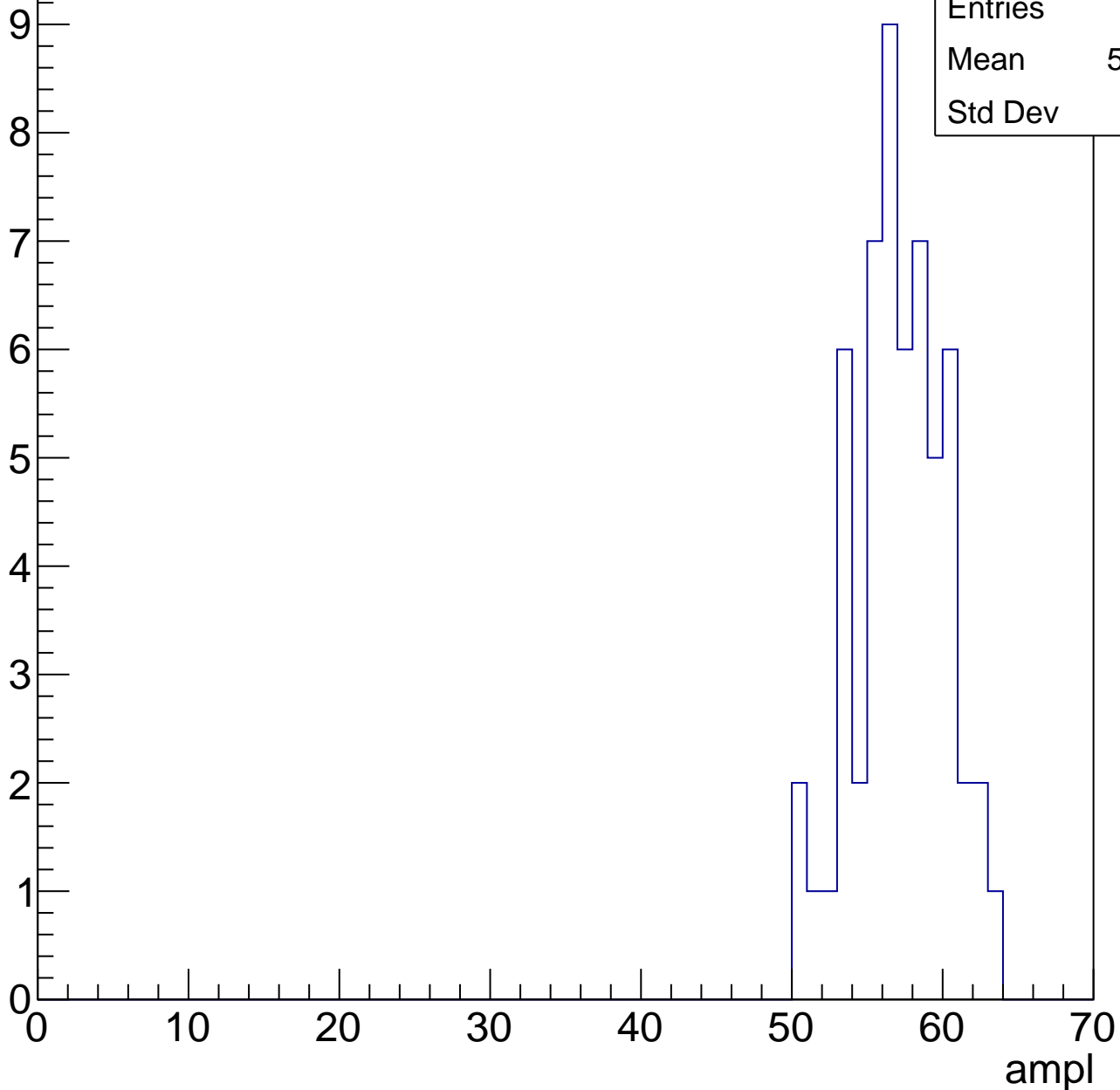


# B0L001S, U24-ch118, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	56.67
Std Dev	2.97

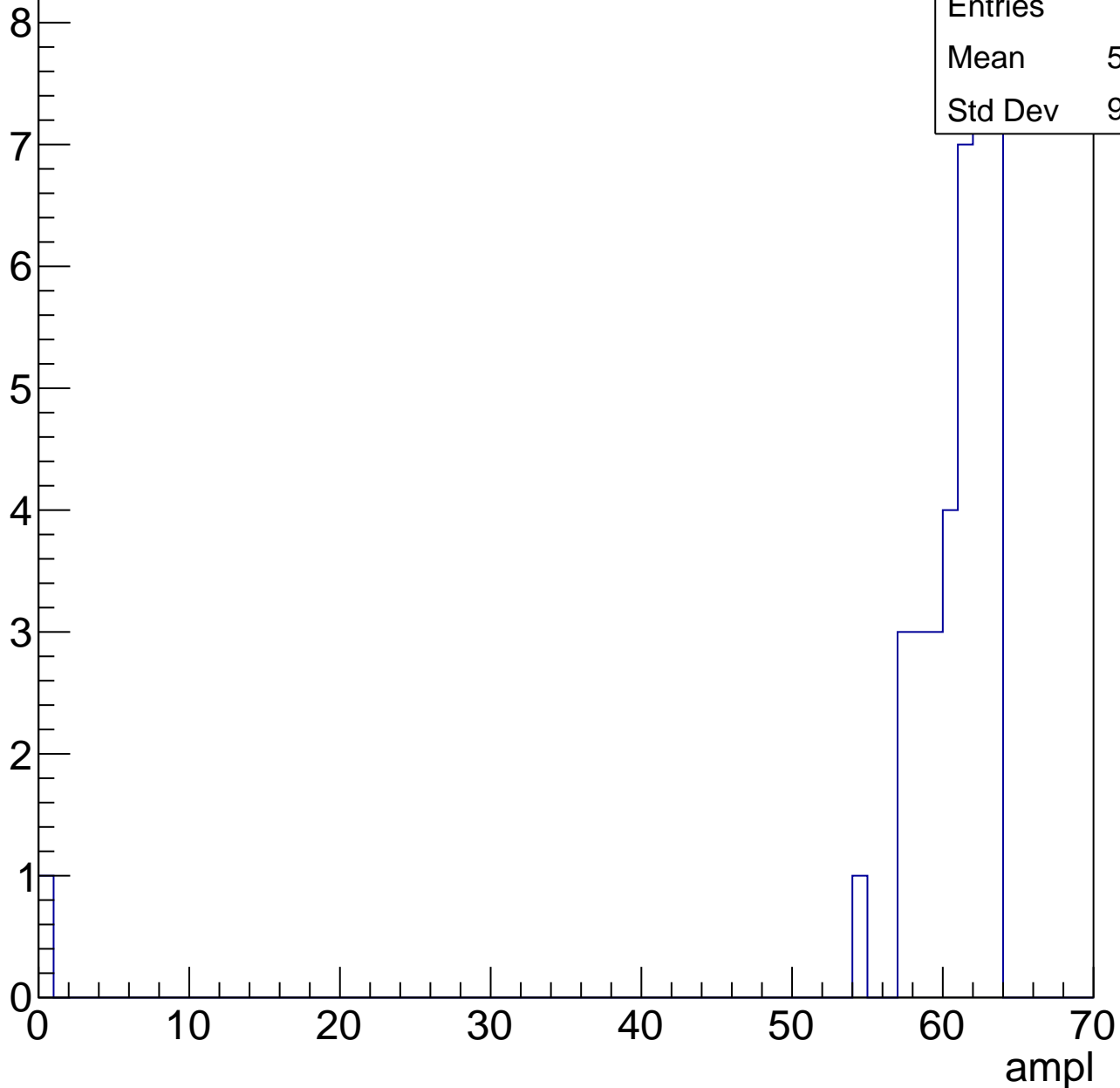


# B0L001S, U24-ch118, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	38
Mean	59.03
Std Dev	9.938



# B0L001S, U24-ch118, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch118, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U24-ch119, adc0

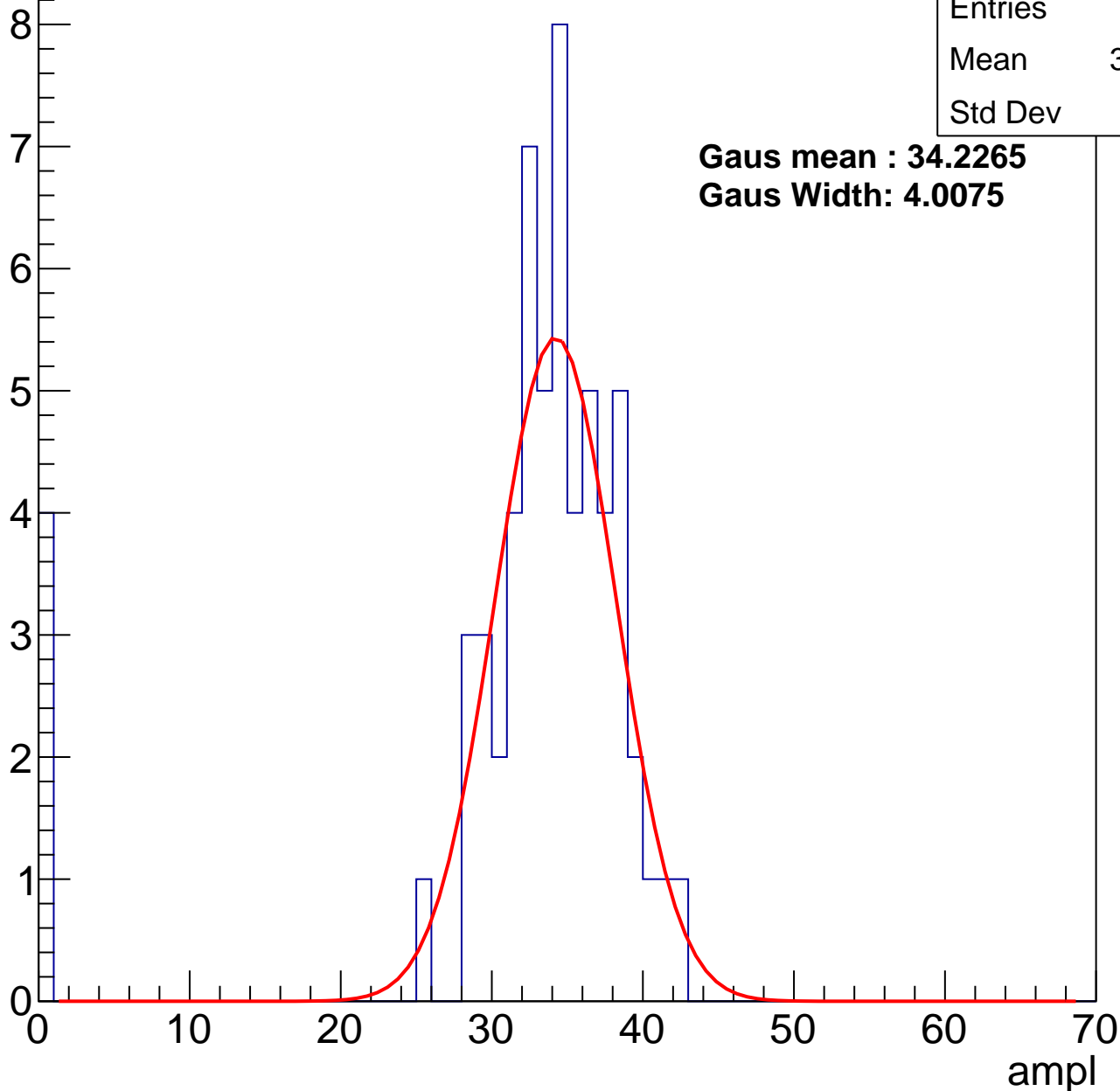
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	31.67
Std Dev	9.13

**Gaus mean : 34.2265**

**Gaus Width: 4.0075**



# B0L001S, U24-ch119, adc1

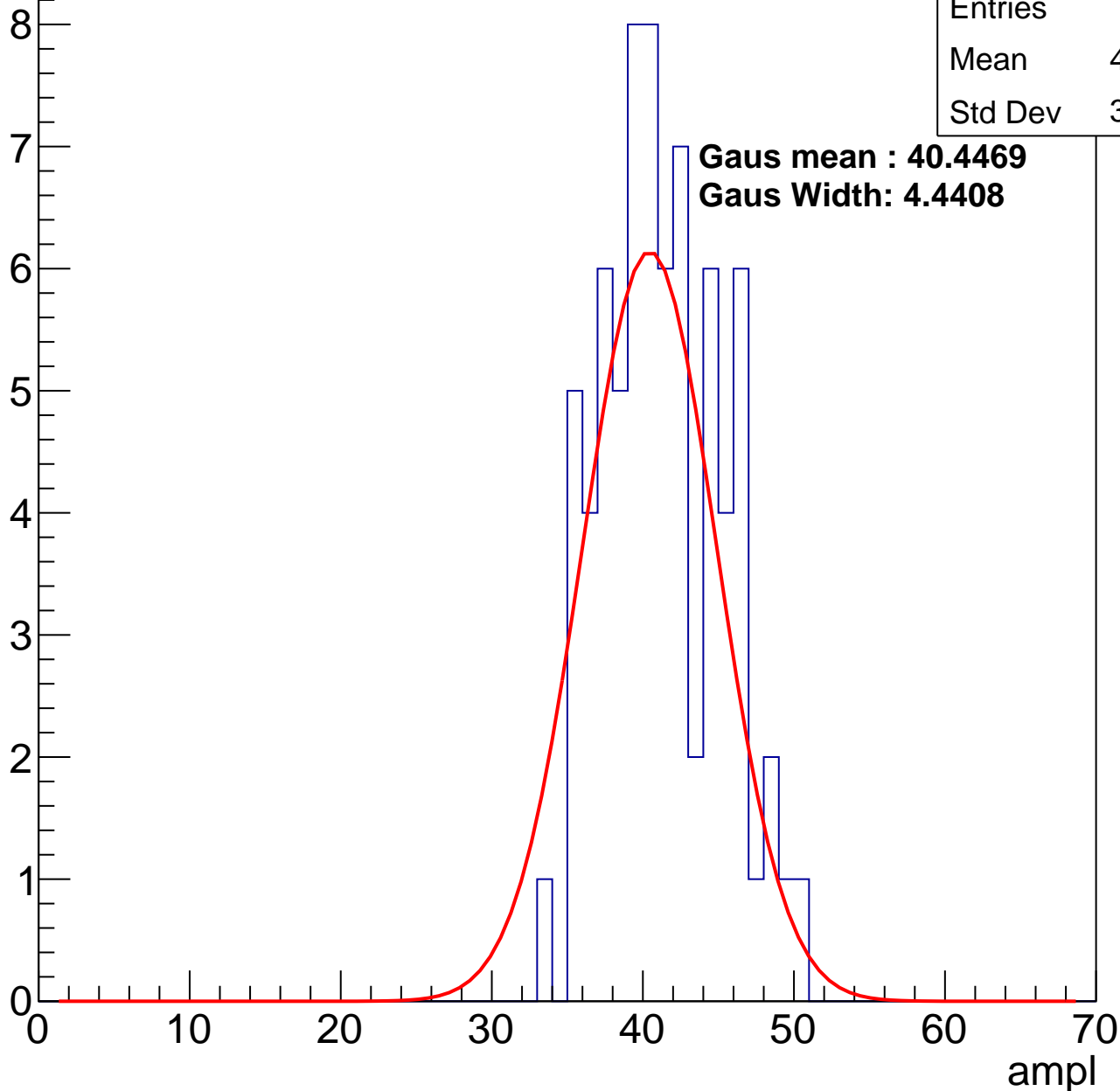
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	40.88
Std Dev	3.857

**Gaus mean : 40.4469**

**Gaus Width: 4.4408**



# B0L001S, U24-ch119, adc2

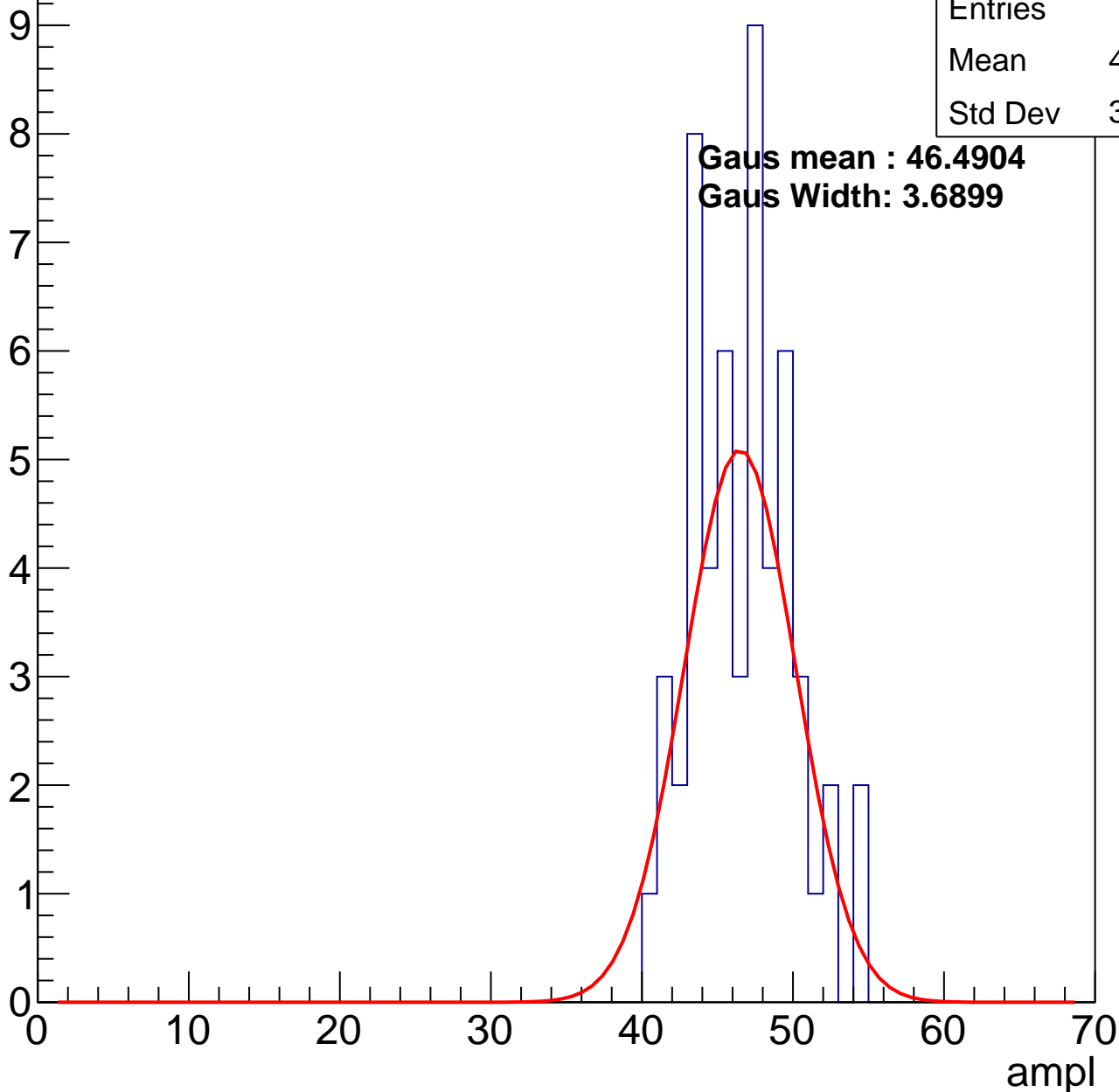
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	46.24
Std Dev	3.294

**Gaus mean : 46.4904**

**Gaus Width: 3.6899**

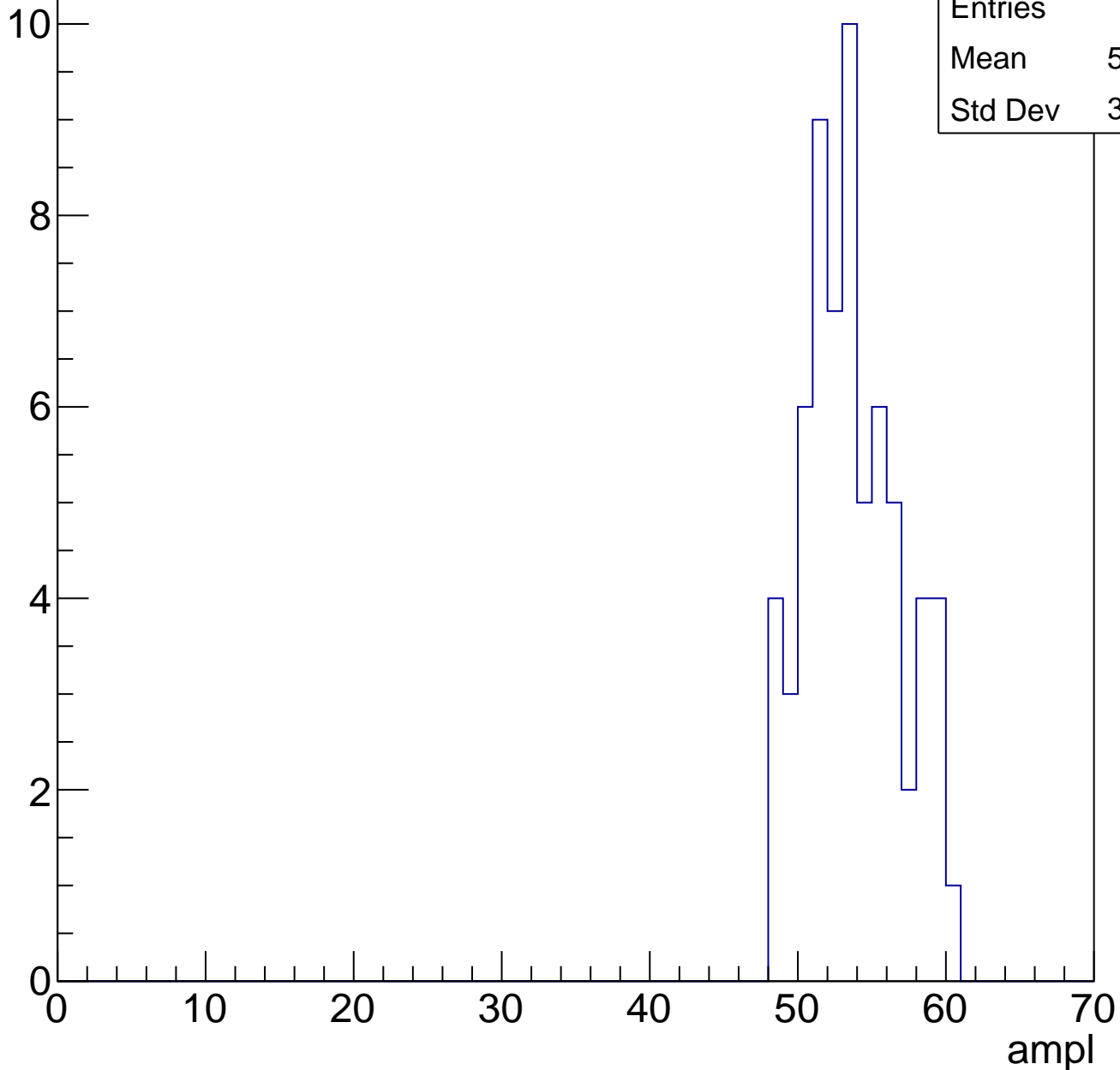


# B0L001S, U24-ch119, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	66
Mean	53.24
Std Dev	3.114

Entry

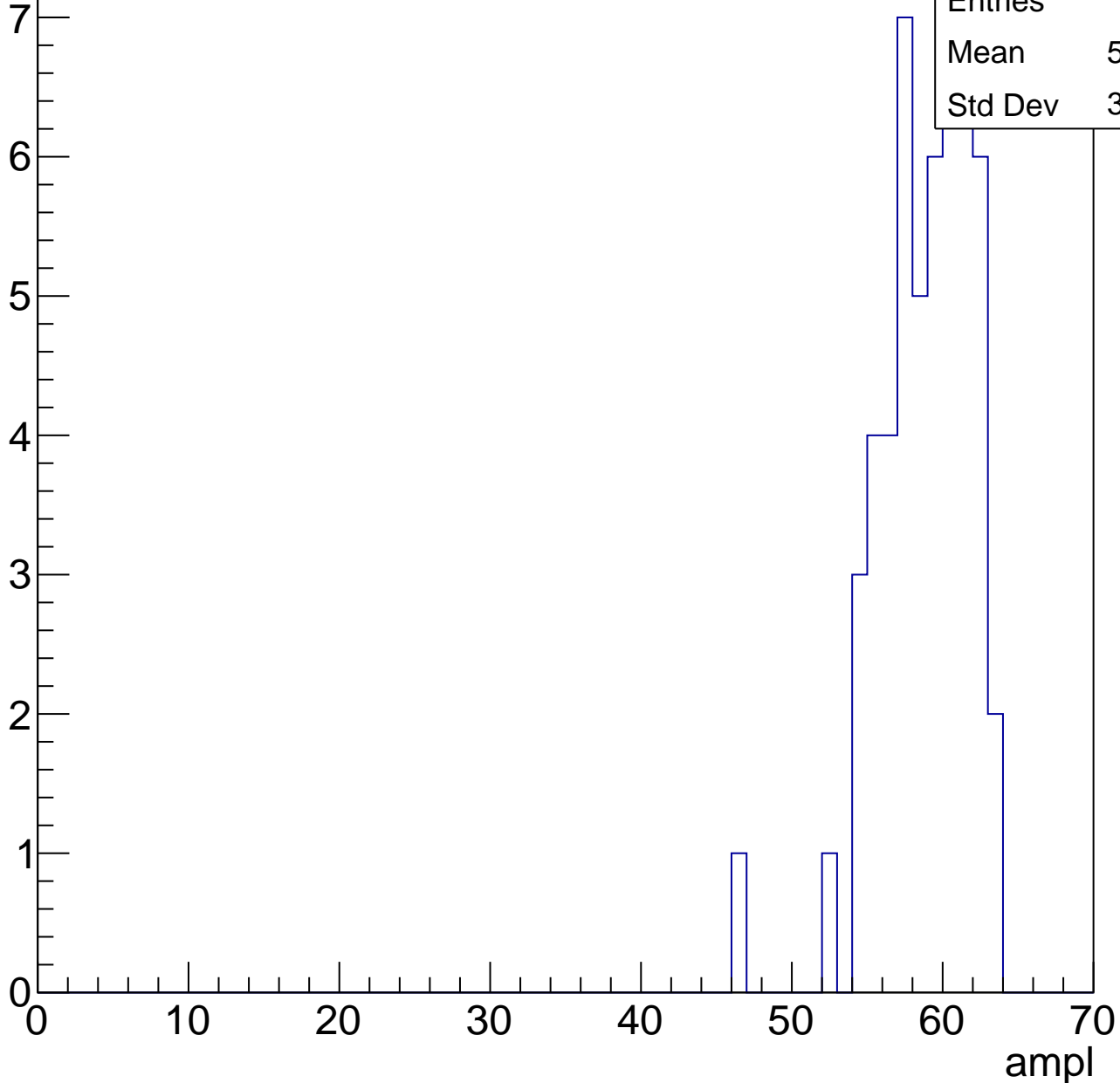


# B0L001S, U24-ch119, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	58.34
Std Dev	3.144

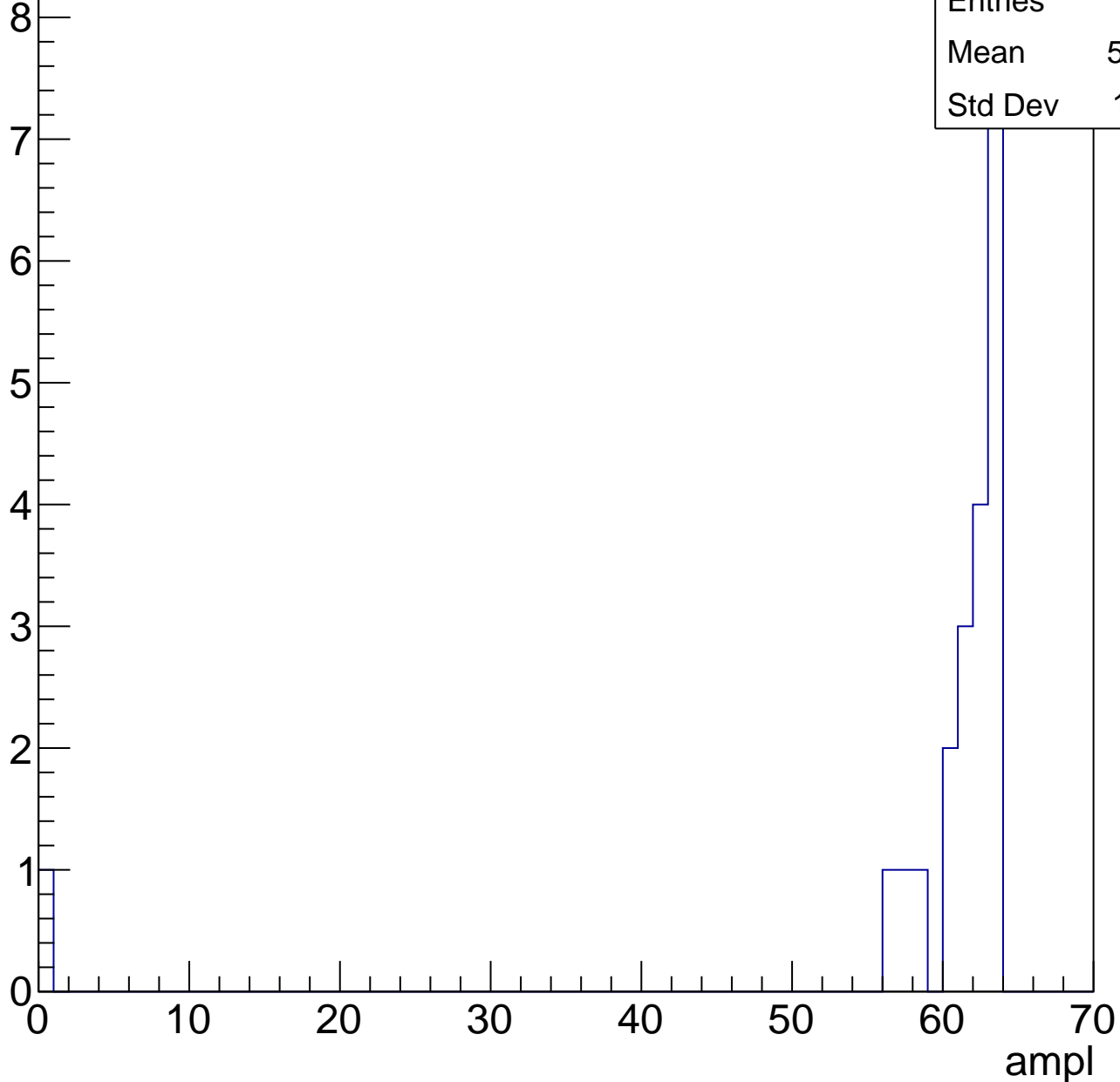


# B0L001S, U24-ch119, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	21
Mean	58.38
Std Dev	13.21



# B0L001S, U24-ch119, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U24-ch119, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U24-ch120, adc0

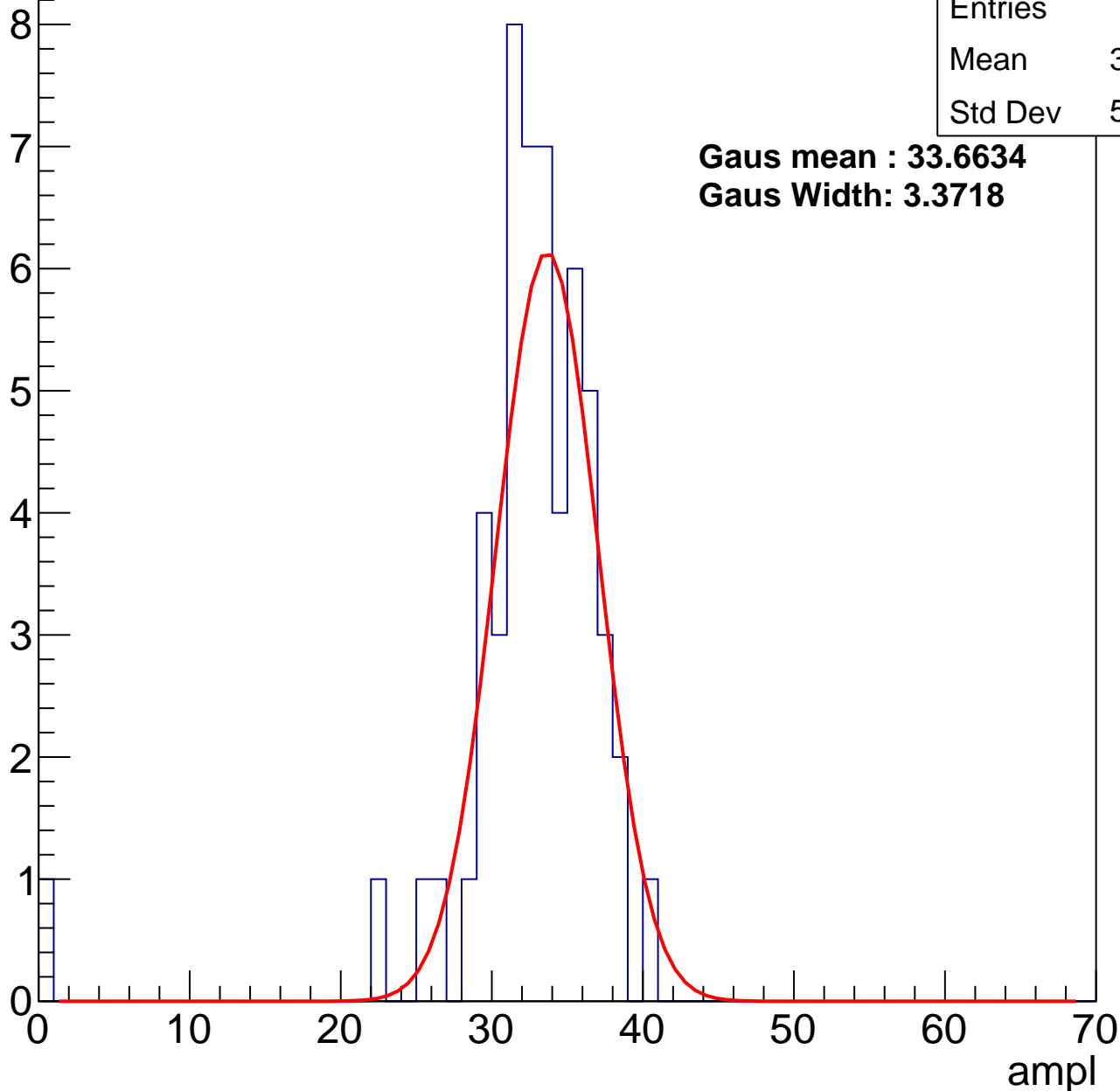
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	32.05
Std Dev	5.475

**Gaus mean : 33.6634**

**Gaus Width: 3.3718**



# B0L001S, U24-ch120, adc1

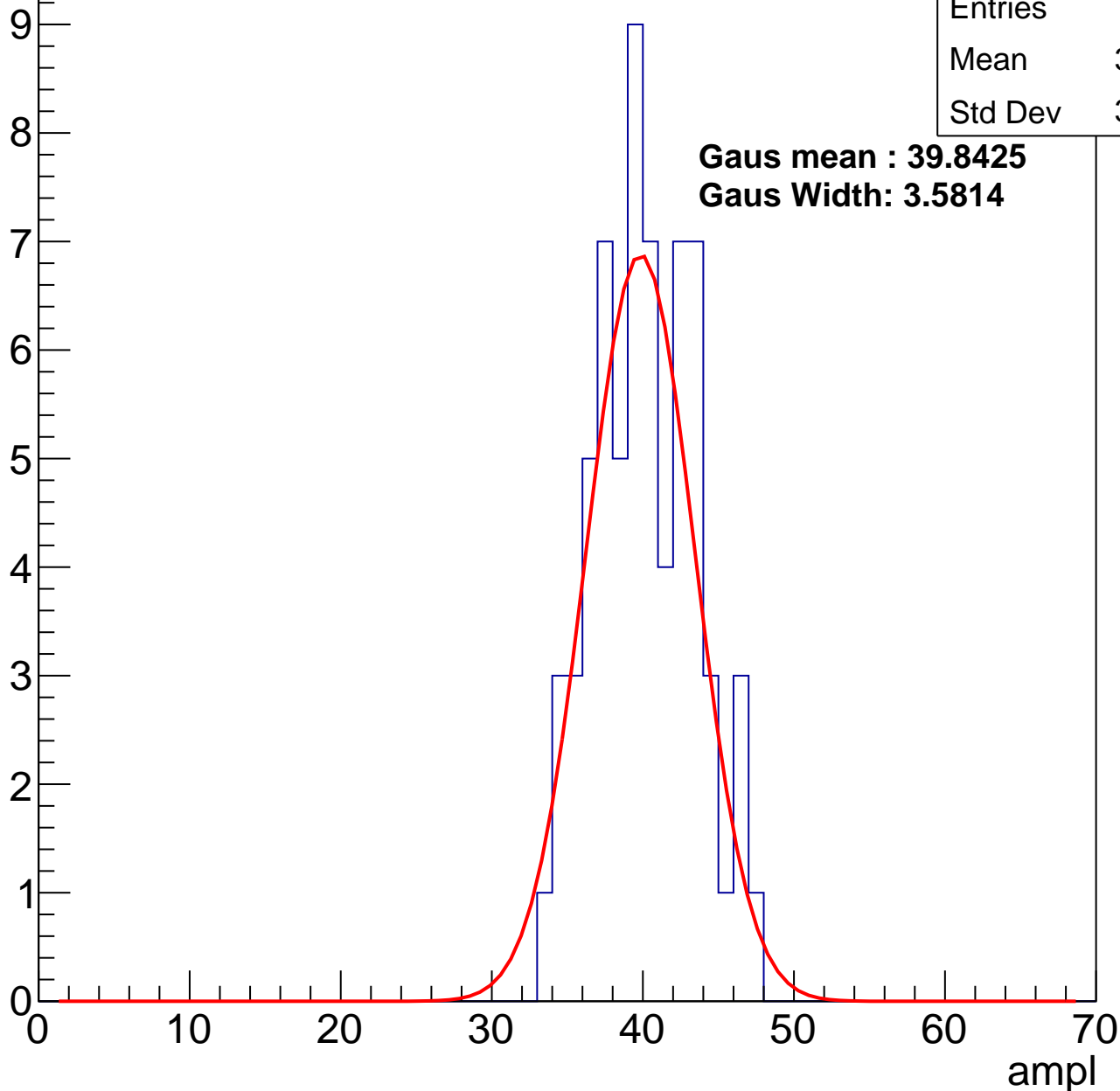
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	39.71
Std Dev	3.311

**Gaus mean : 39.8425**

**Gaus Width: 3.5814**



# B0L001S, U24-ch120, adc2

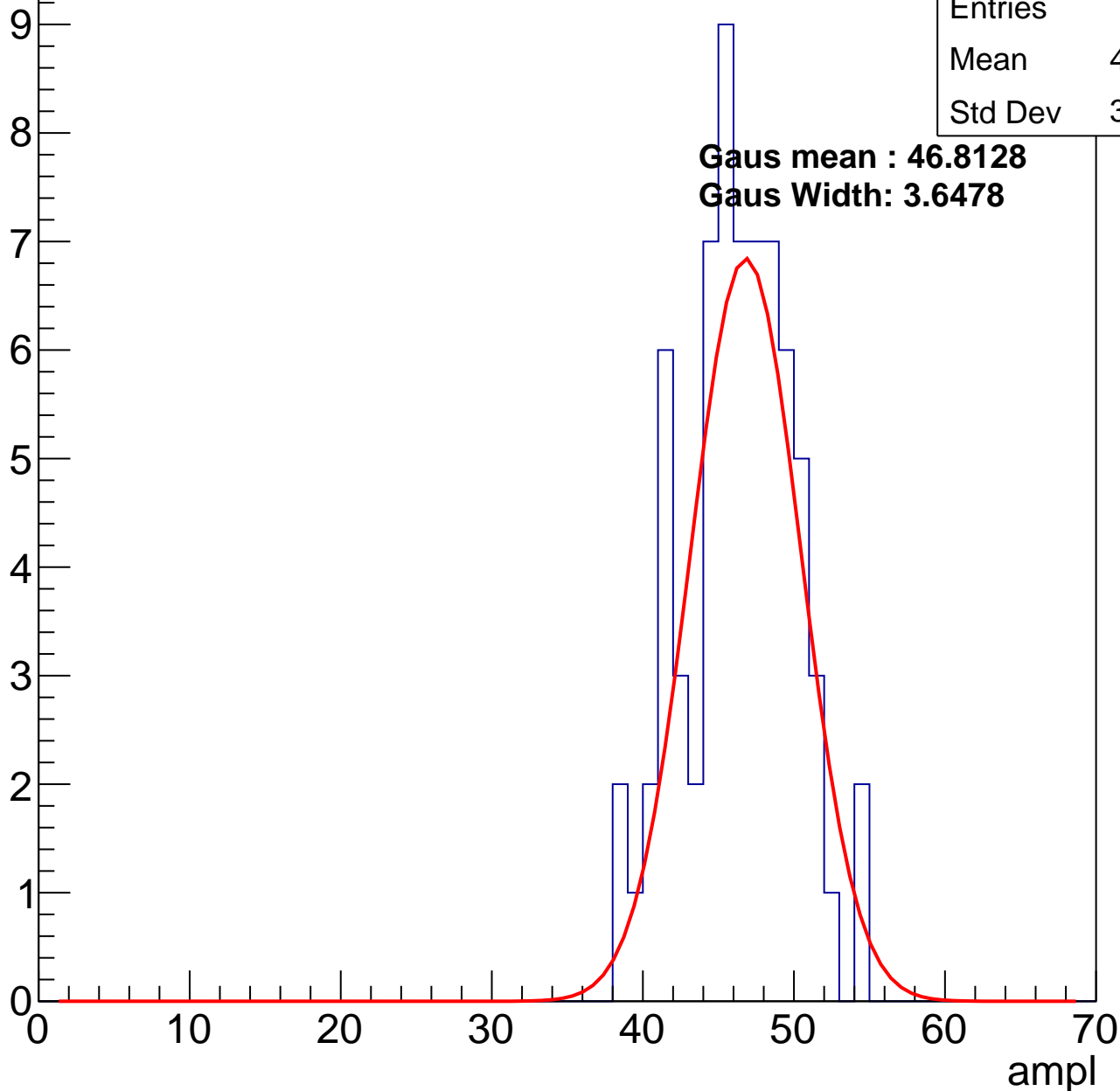
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	45.86
Std Dev	3.603

**Gaus mean : 46.8128**

**Gaus Width: 3.6478**

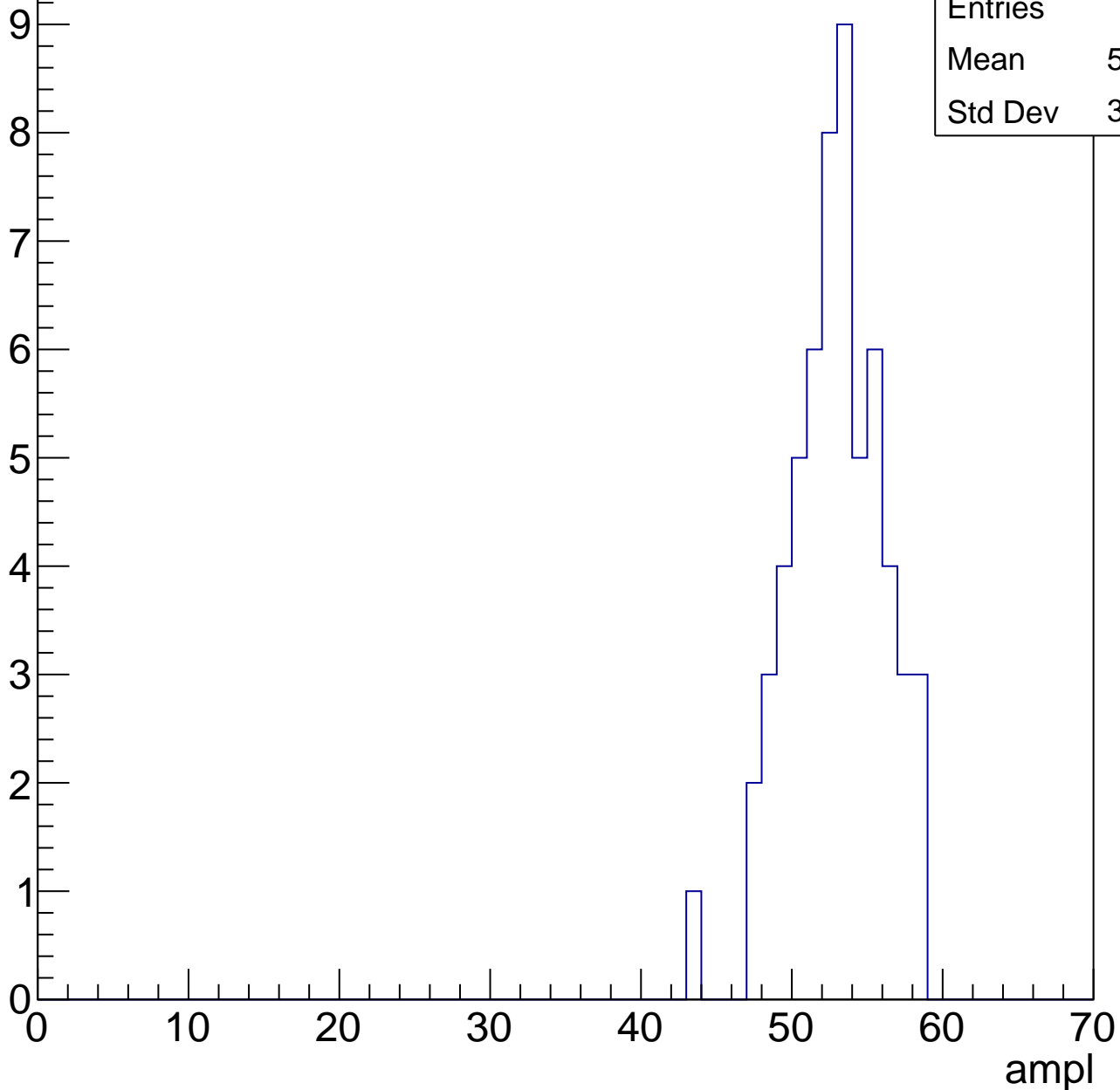


# B0L001S, U24-ch120, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	52.46
Std Dev	3.077

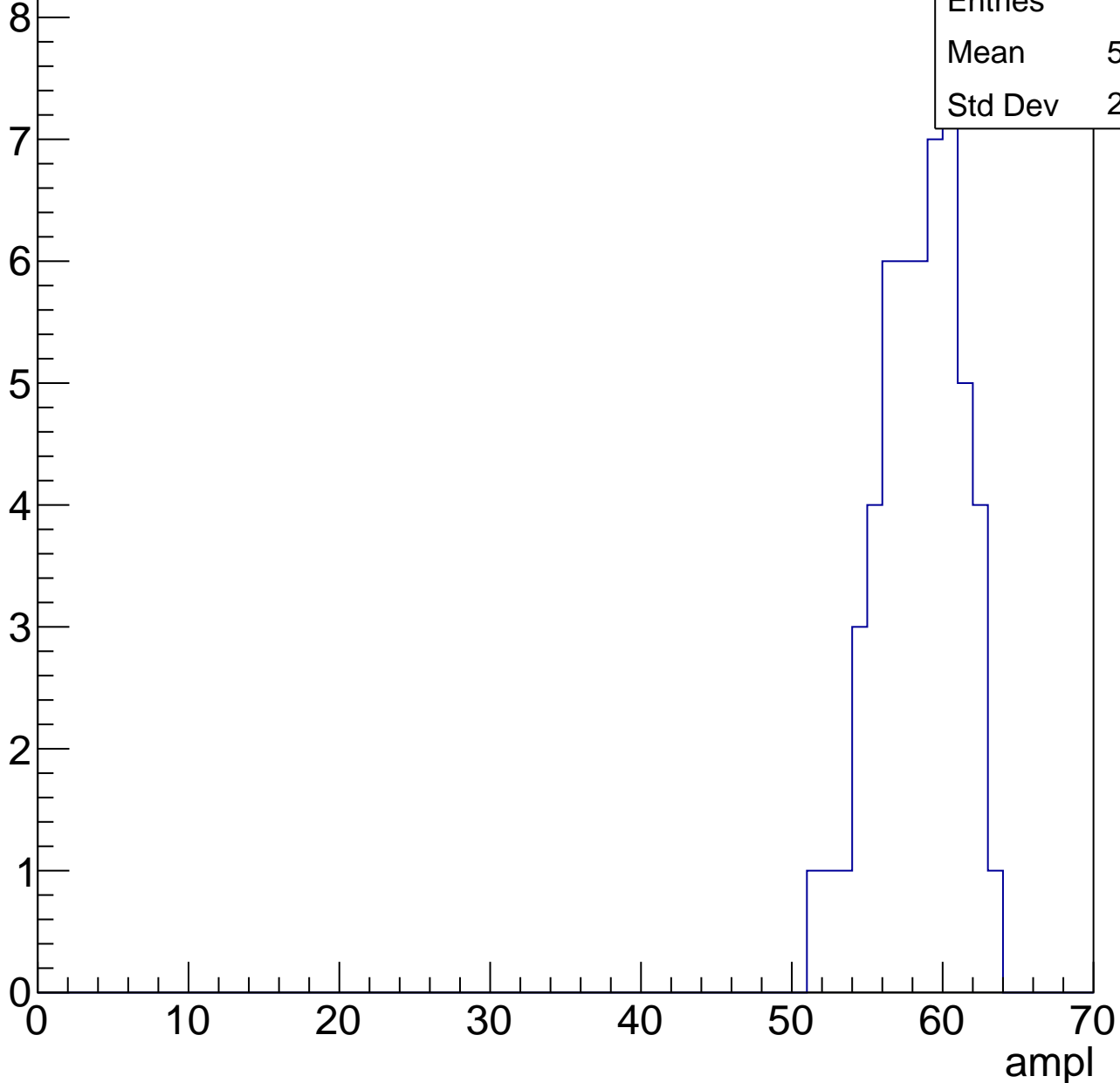


# B0L001S, U24-ch120, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	57.98
Std Dev	2.737

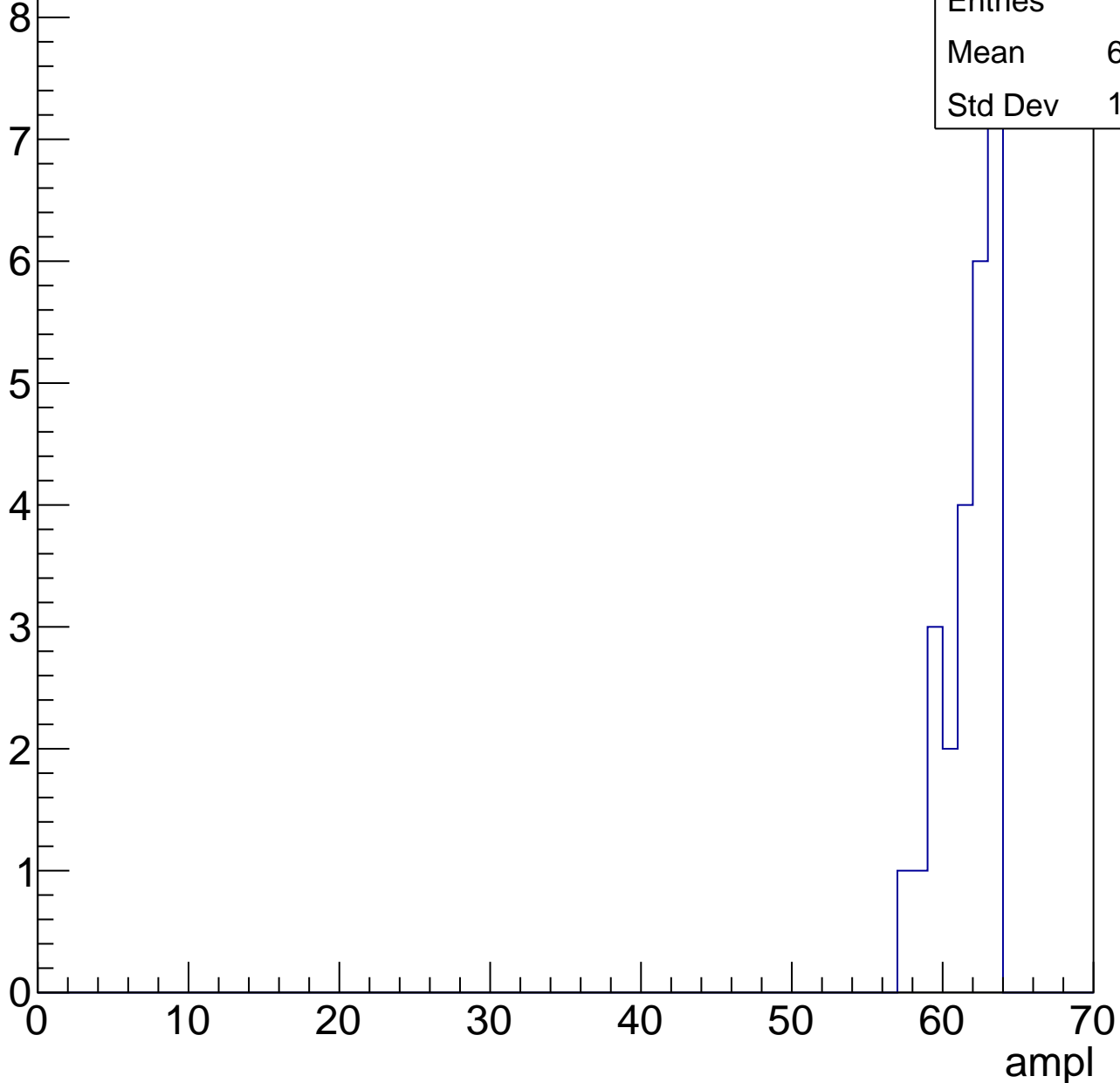


# B0L001S, U24-ch120, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

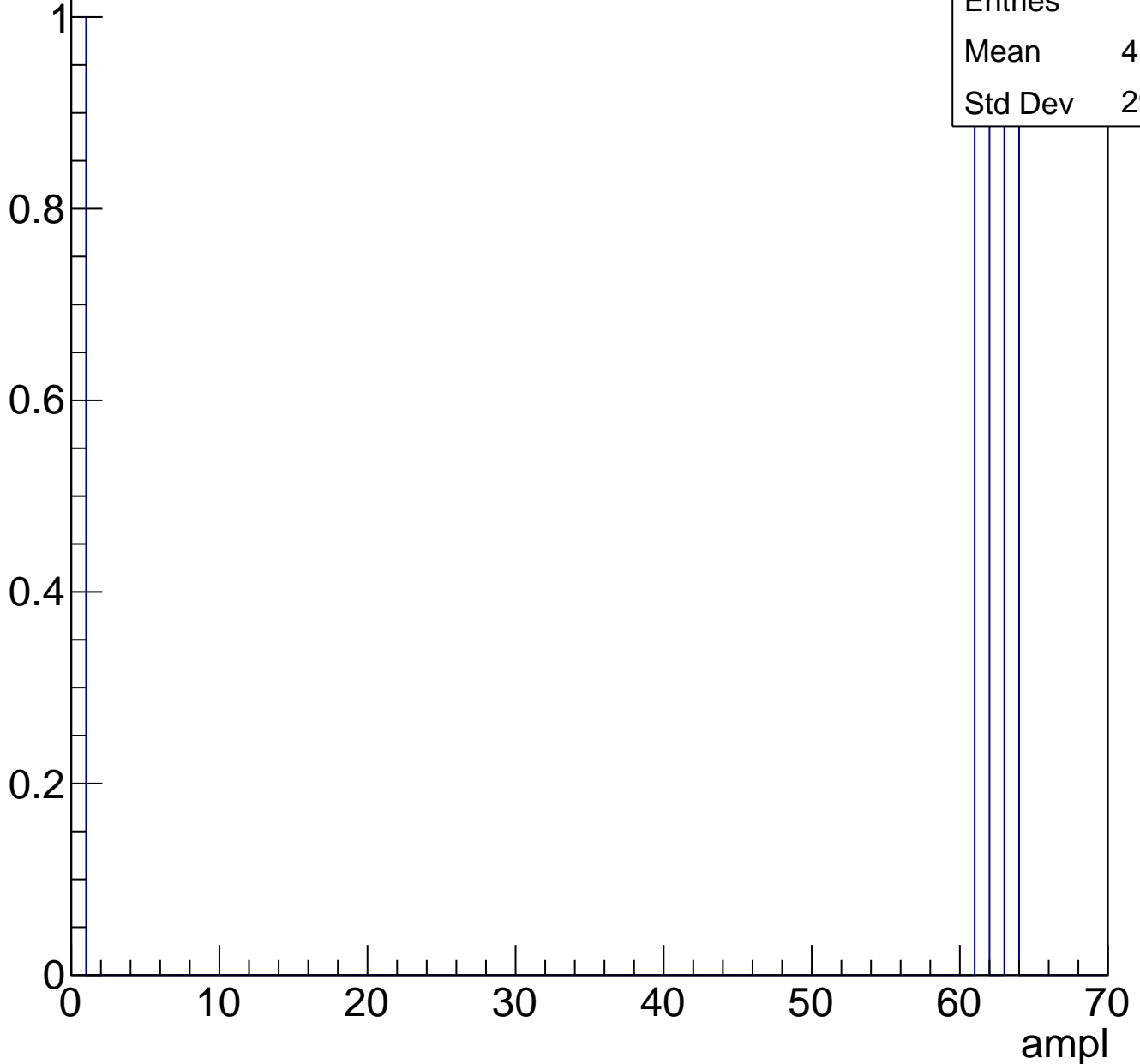
Entries	25
Mean	61.28
Std Dev	1.733



# B0L001S, U24-ch120, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch120, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U24-ch121, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	70
Mean	29.4
Std Dev	7.108

**Gaus mean : 31.0675**

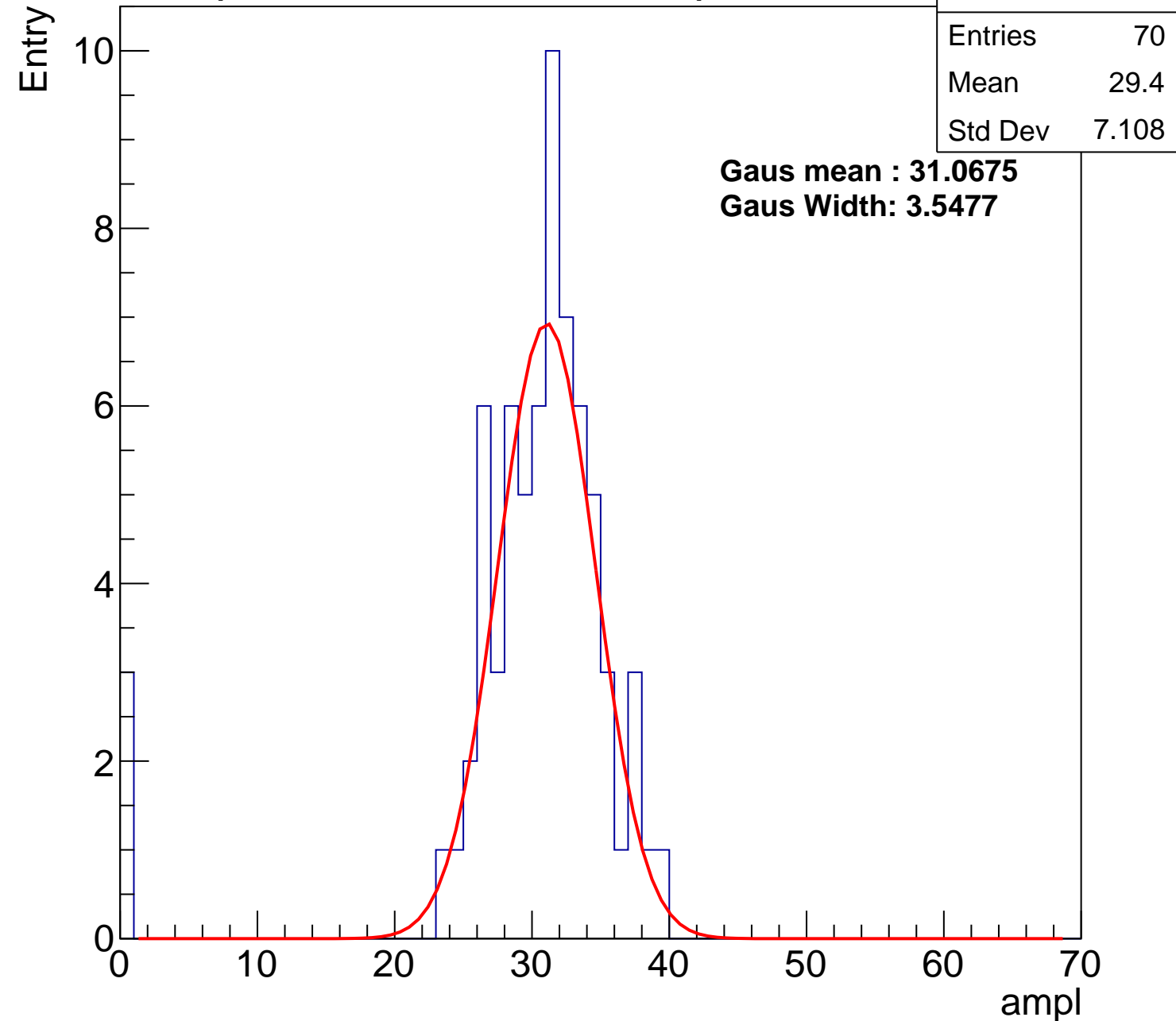
**Gaus Width: 3.5477**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U24-ch121, adc1

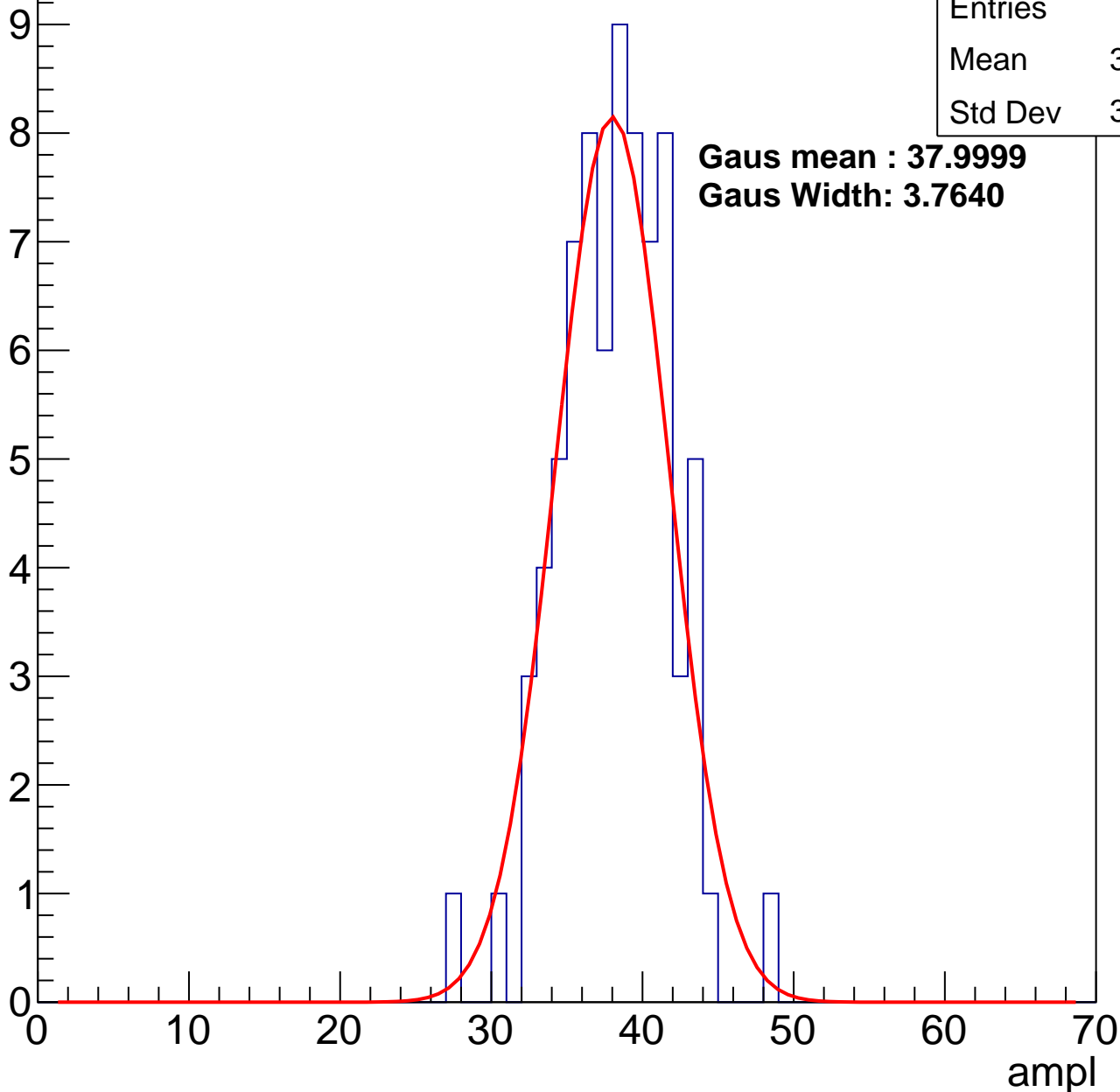
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	77
Mean	37.73
Std Dev	3.577

**Gaus mean : 37.9999**

**Gaus Width: 3.7640**



# B0L001S, U24-ch121, adc2

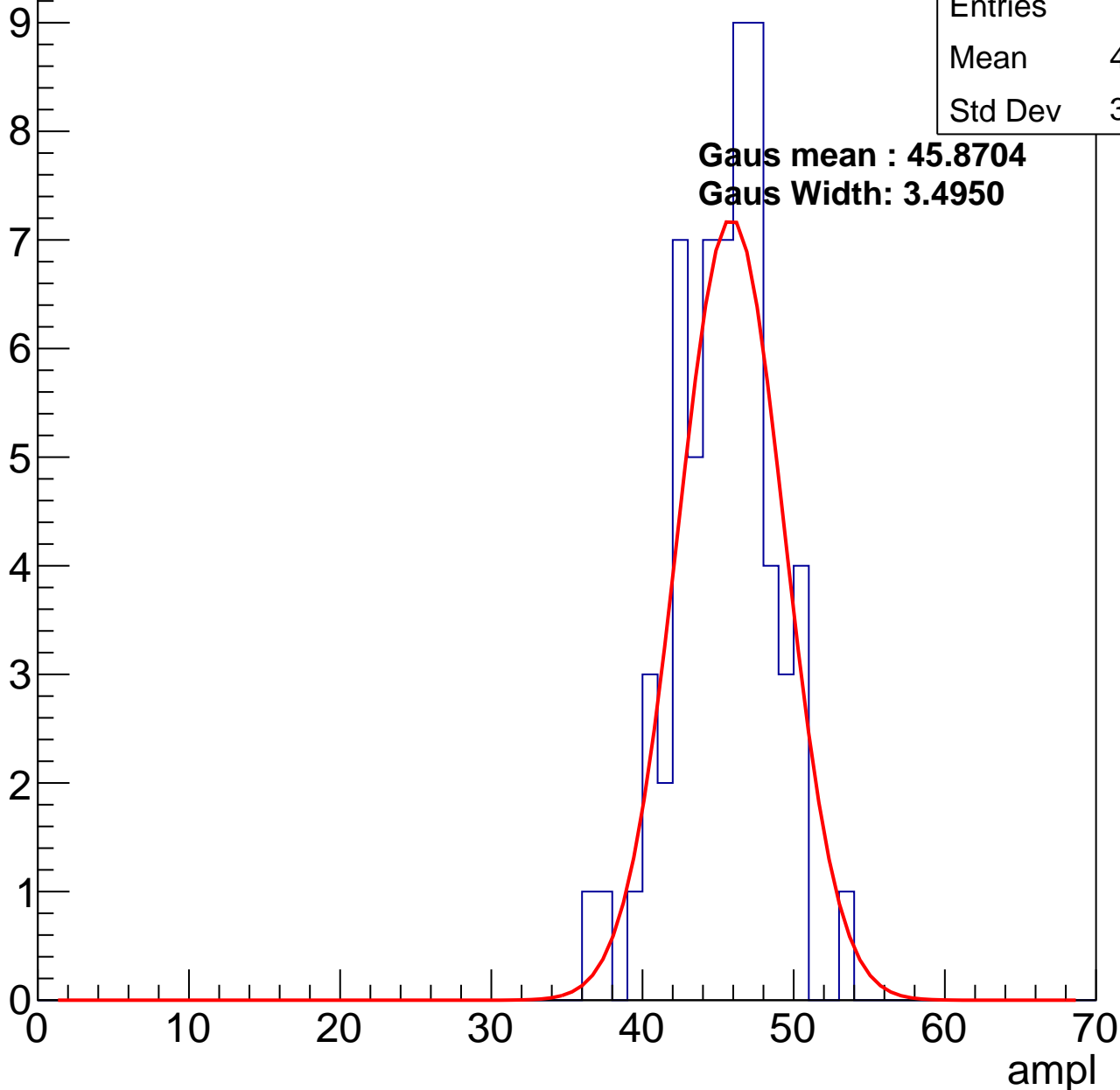
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	44.92
Std Dev	3.237

**Gaus mean : 45.8704**

**Gaus Width: 3.4950**

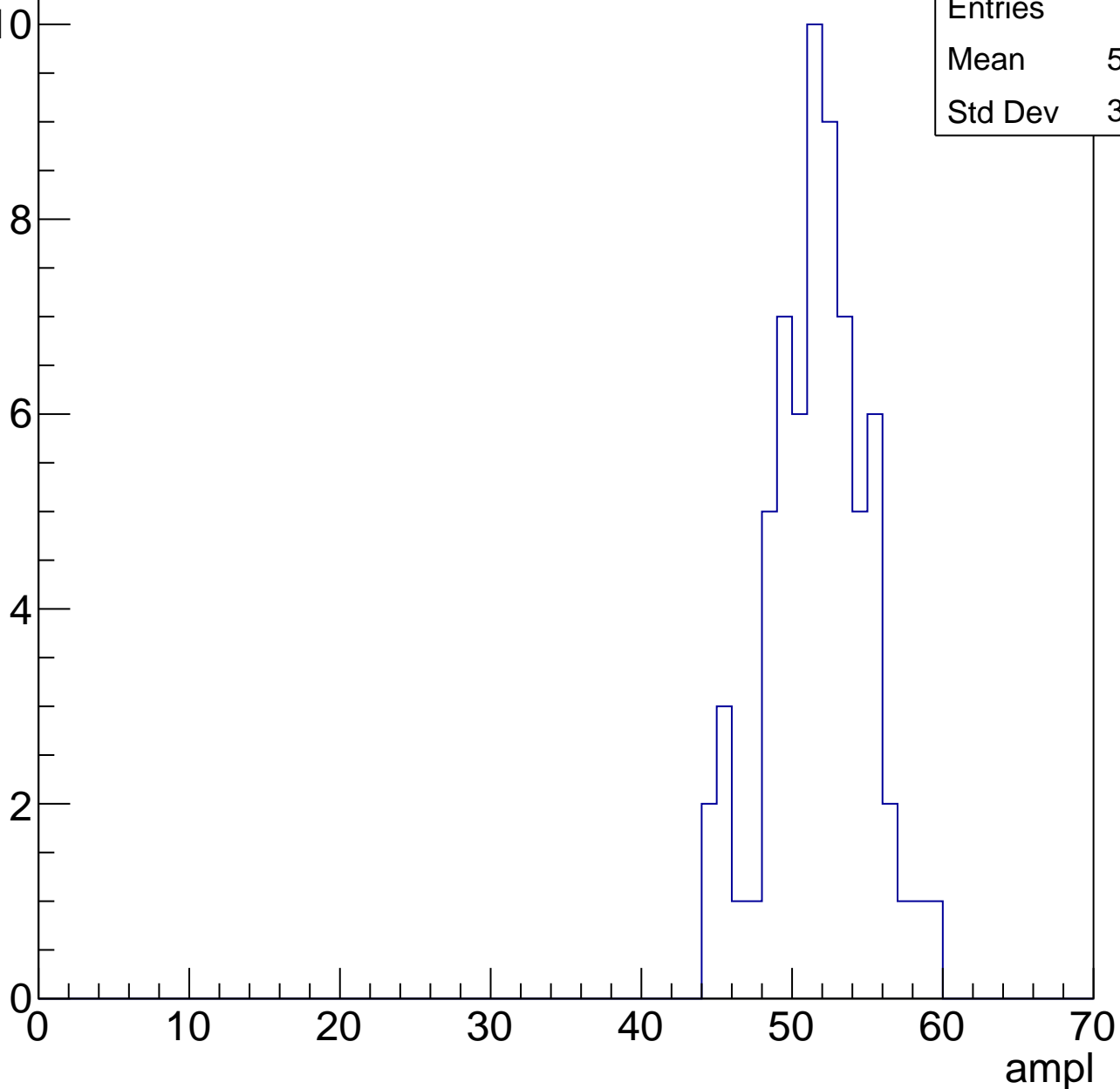


# B0L001S, U24-ch121, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	51.25
Std Dev	3.229

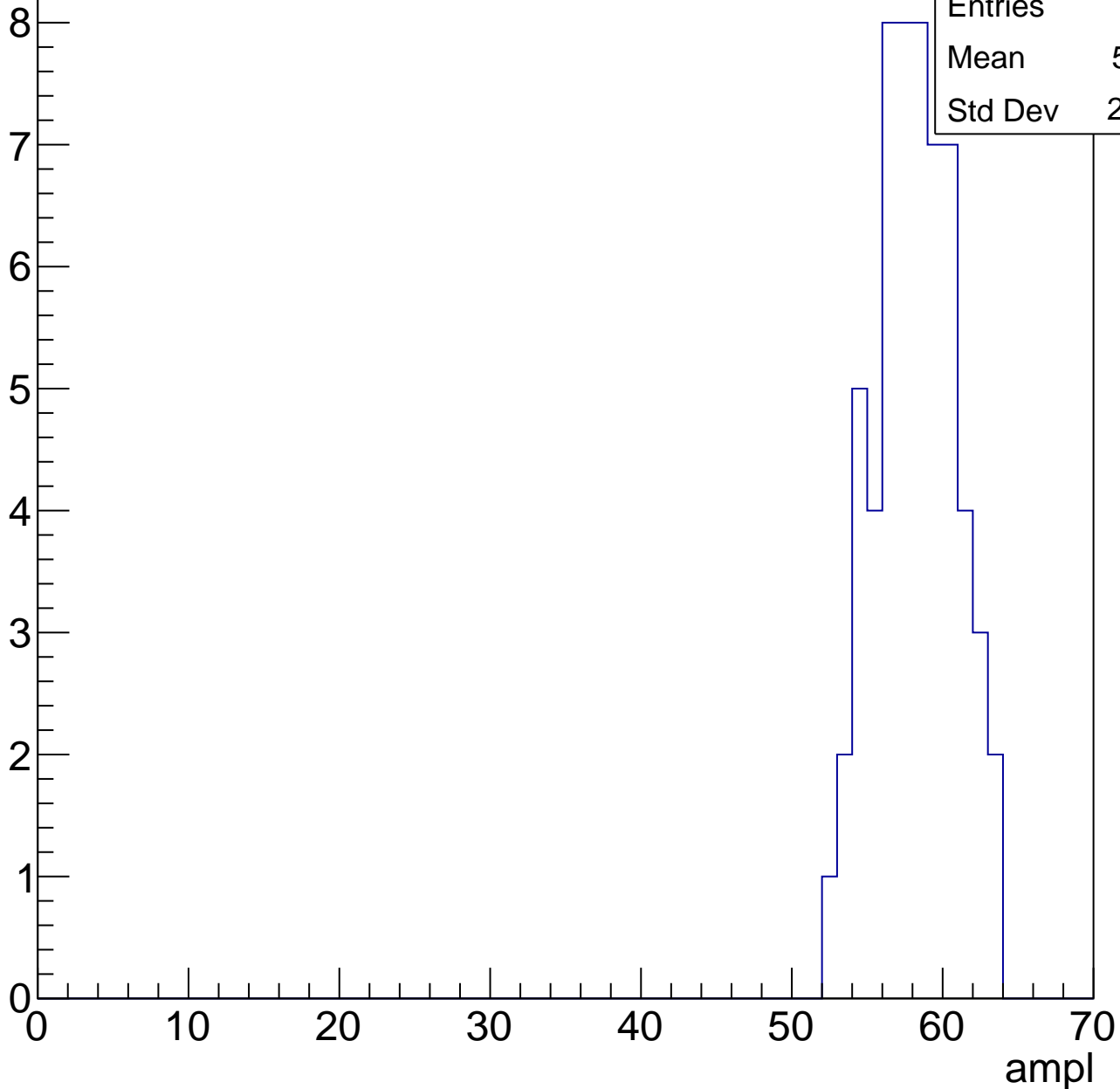


# B0L001S, U24-ch121, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	57.71
Std Dev	2.624

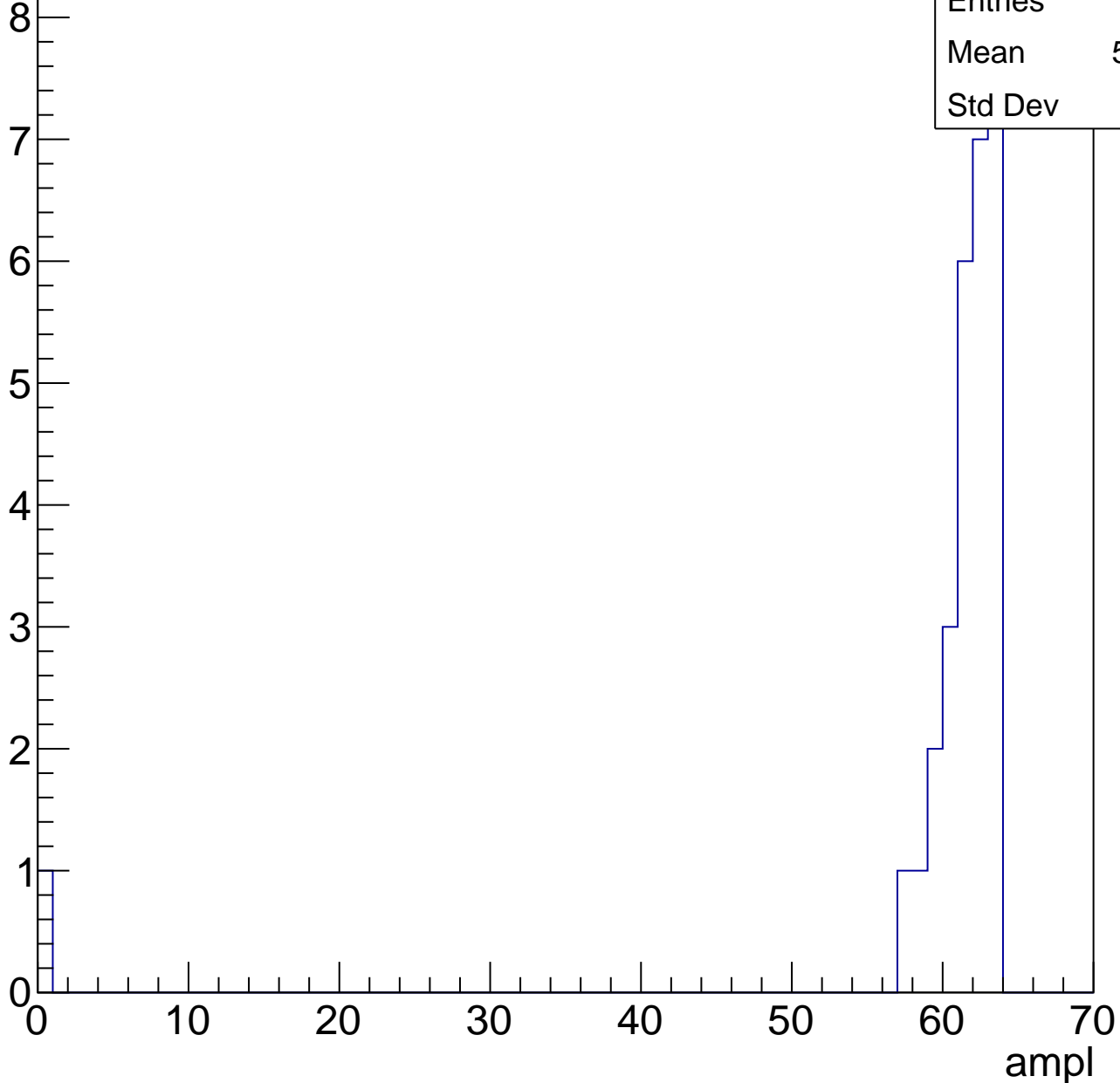


# B0L001S, U24-ch121, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	29
Mean	59.21
Std Dev	11.3



# B0L001S, U24-ch121, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U24-ch121, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U24-ch122, adc0

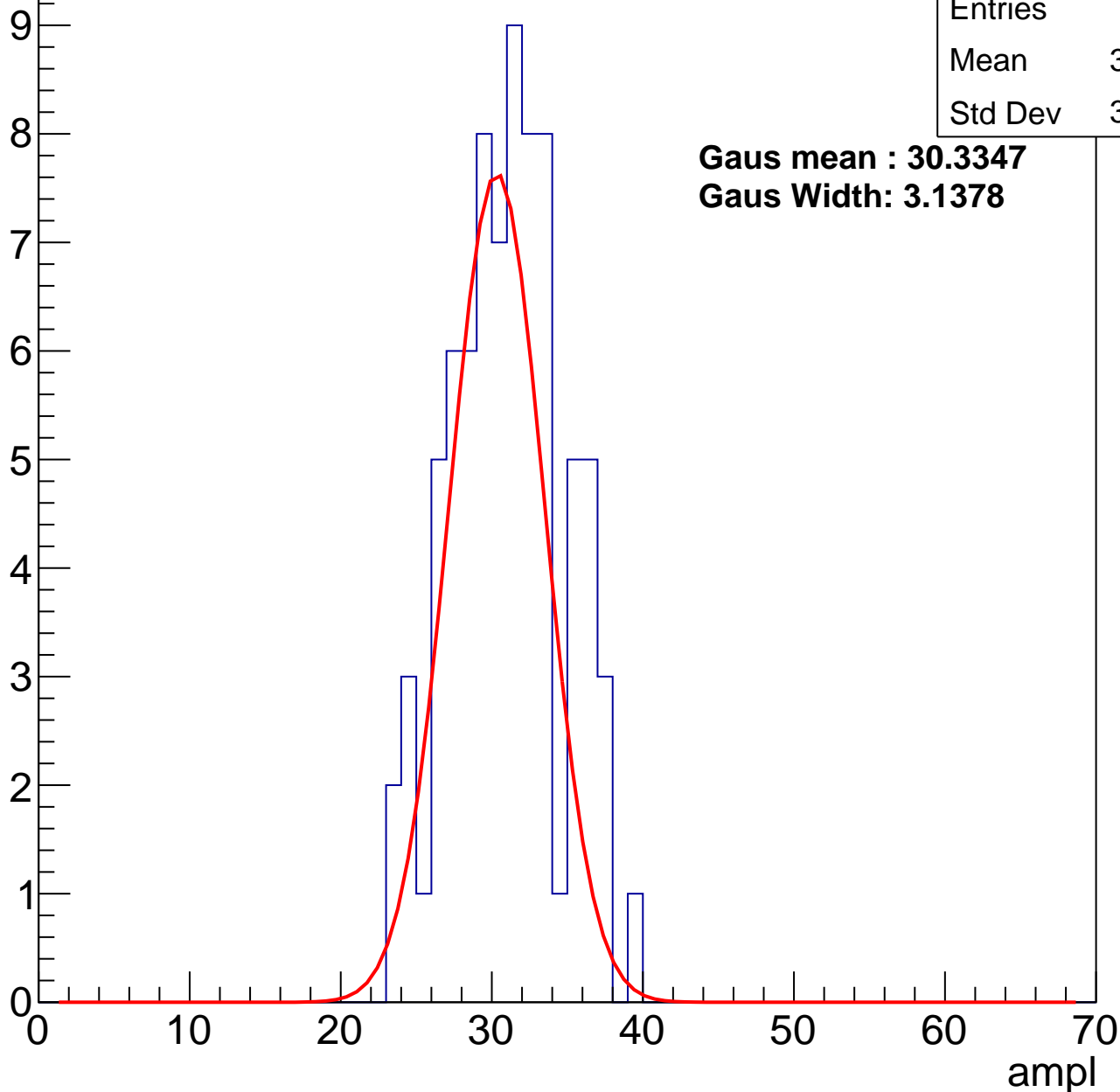
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	78
Mean	30.55
Std Dev	3.643

**Gaus mean : 30.3347**

**Gaus Width: 3.1378**



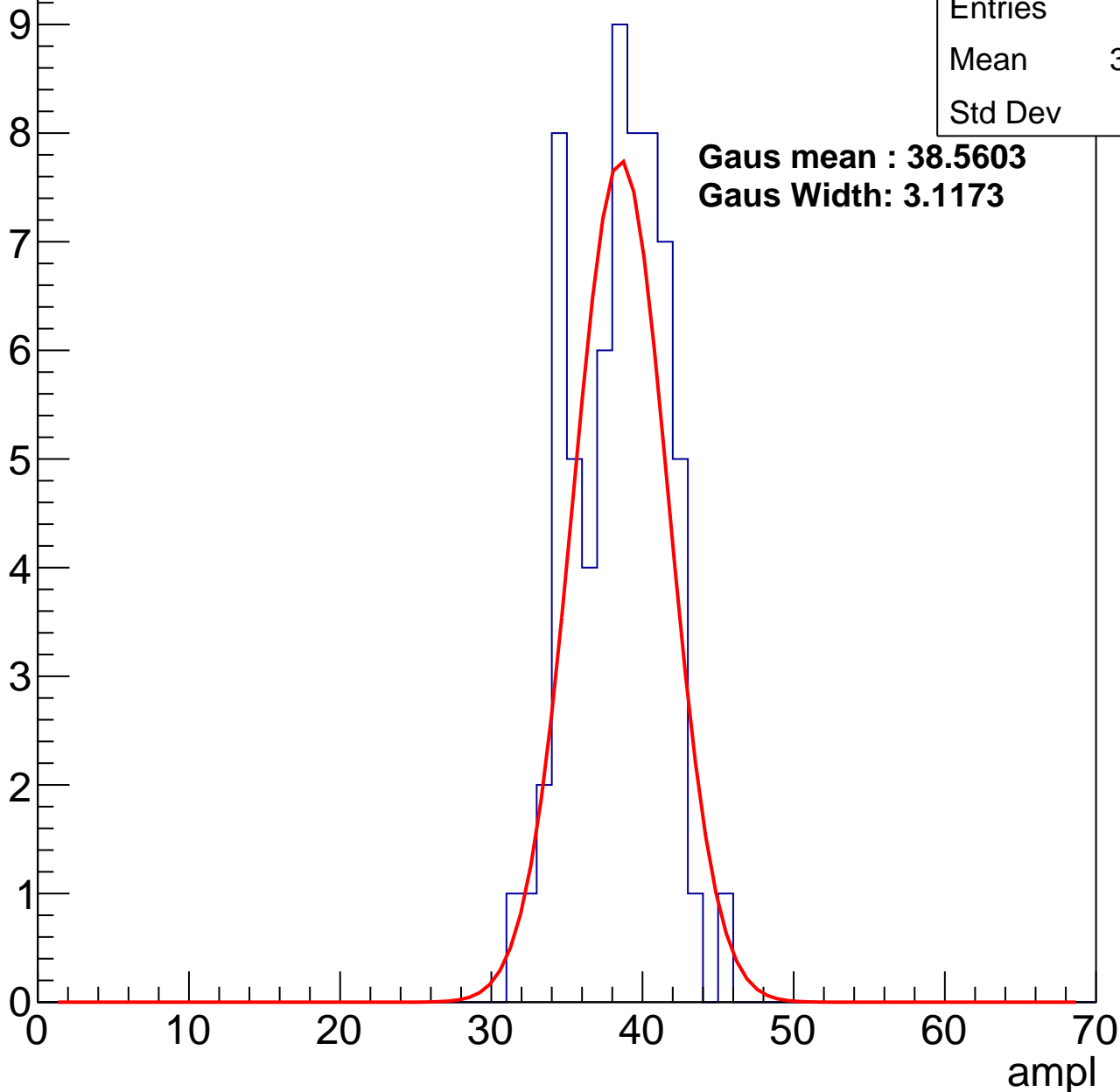
# B0L001S, U24-ch122, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	37.89
Std Dev	2.98

**Gaus mean : 38.5603**  
**Gaus Width: 3.1173**



# B0L001S, U24-ch122, adc2

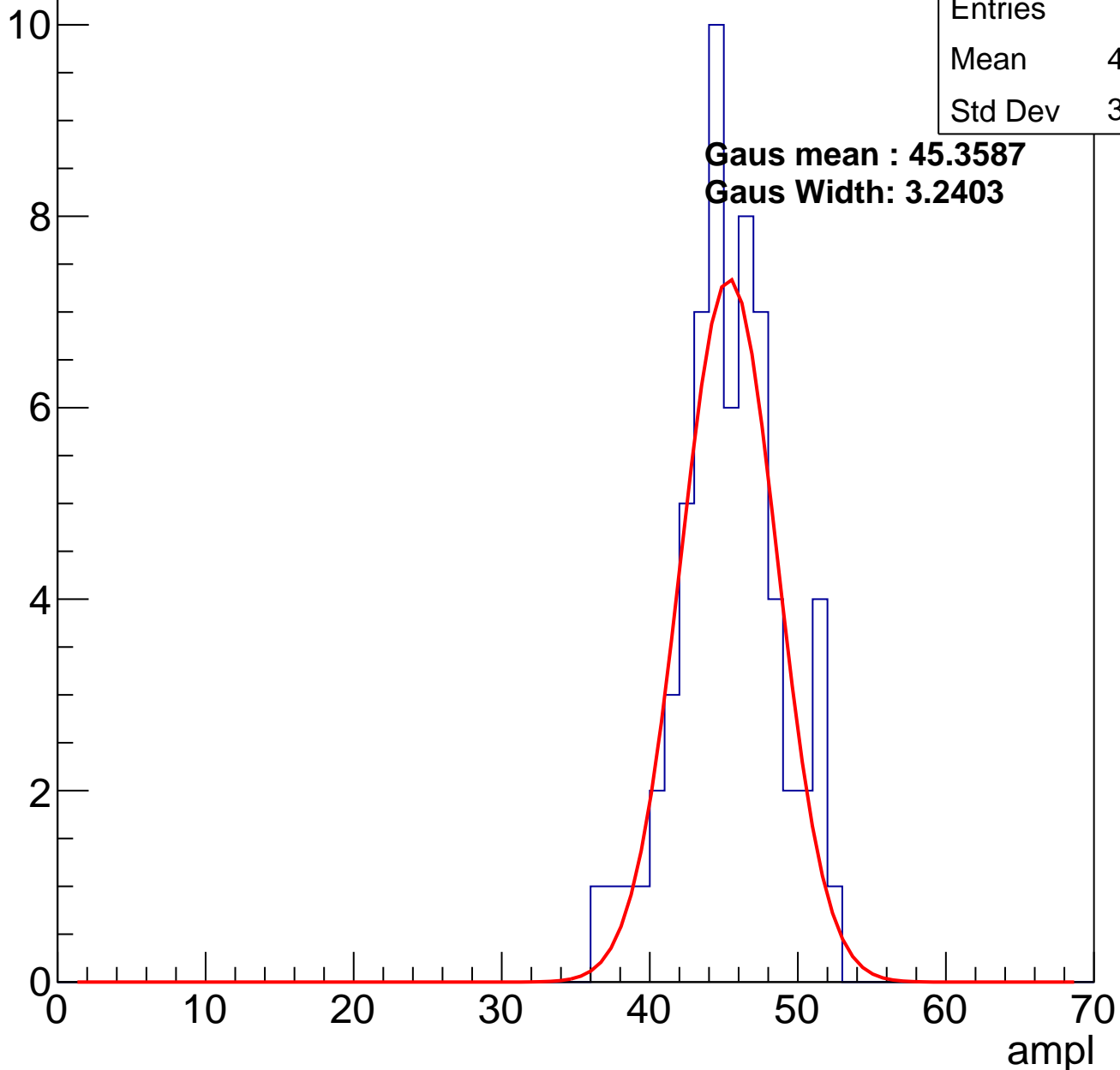
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	65
Mean	44.88
Std Dev	3.413

**Gaus mean : 45.3587**

**Gaus Width: 3.2403**

Entry

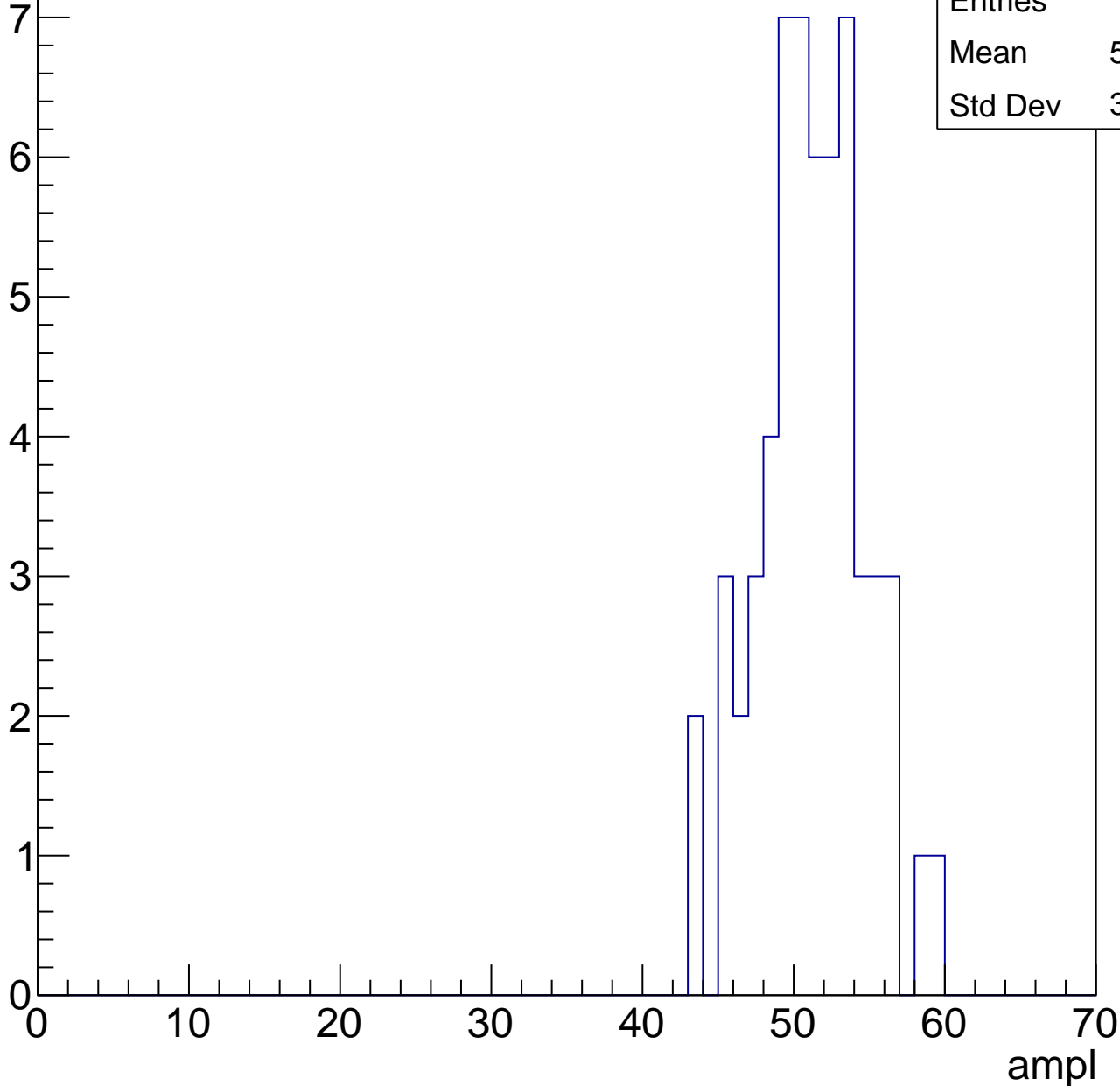


# B0L001S, U24-ch122, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	50.69
Std Dev	3.465

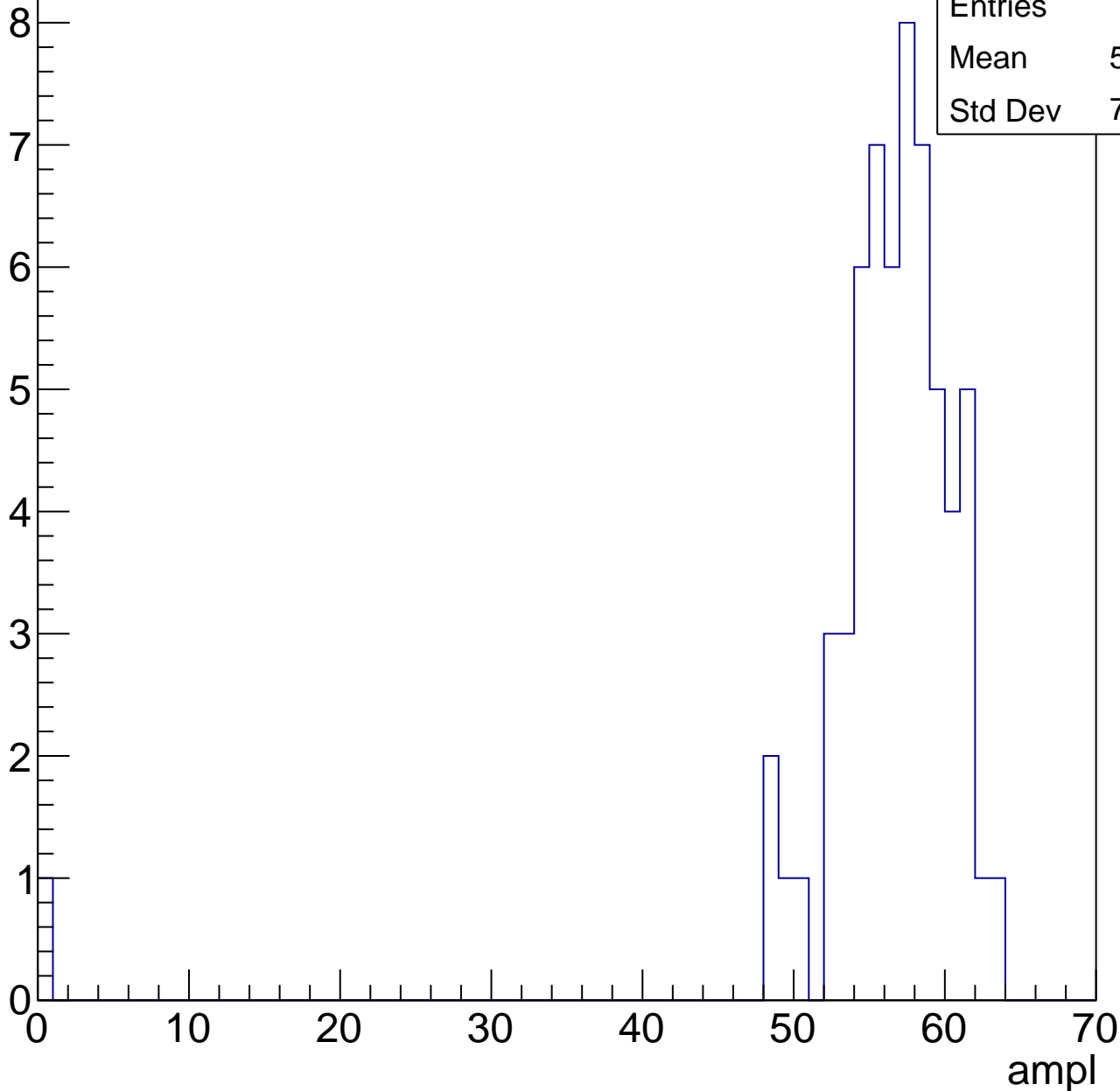


# B0L001S, U24-ch122, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	55.44
Std Dev	7.883

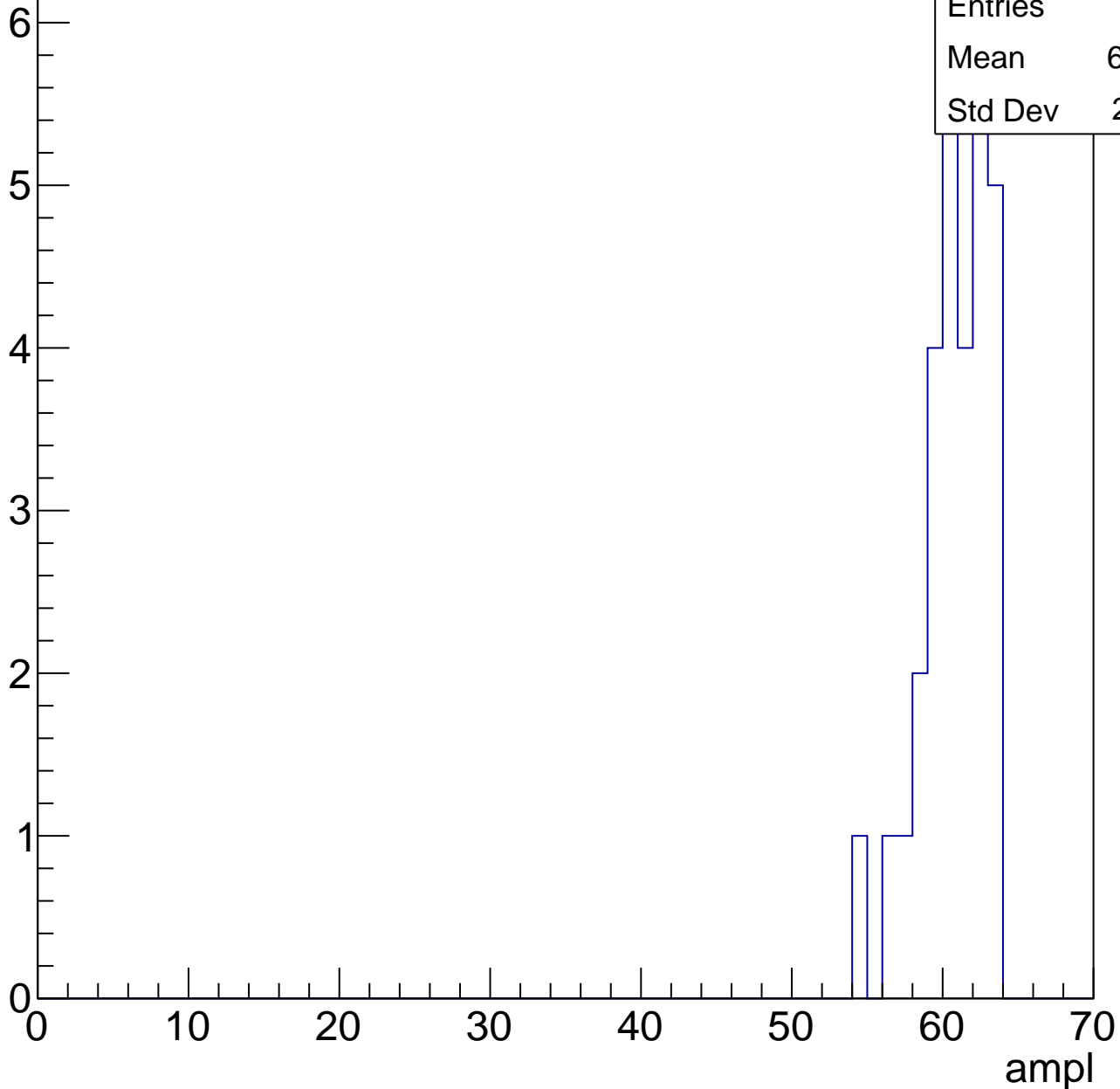


# B0L001S, U24-ch122, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

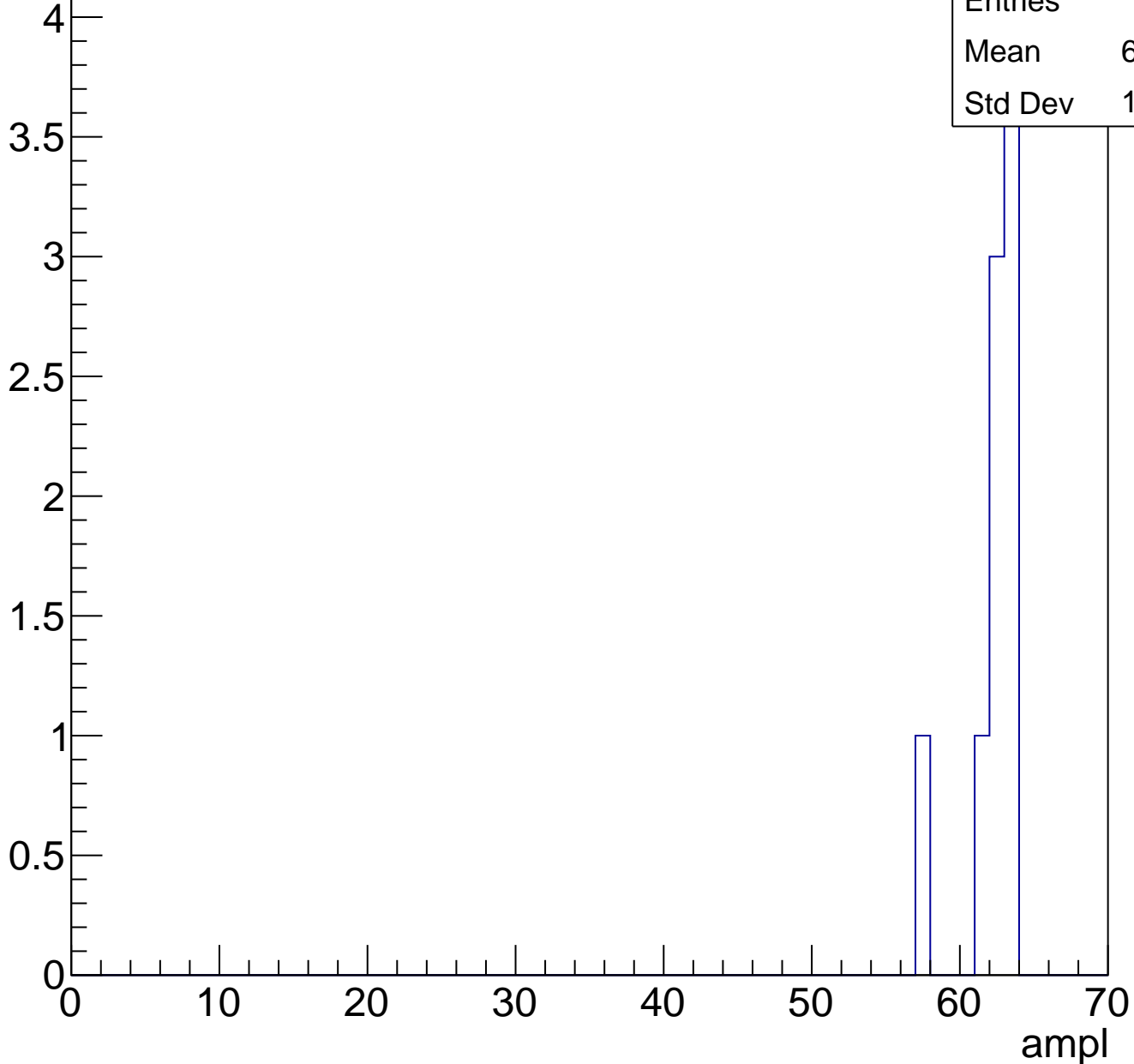
Entries	30
Mean	60.33
Std Dev	2.181



# B0L001S, U24-ch122, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch122, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U24-ch123, adc0

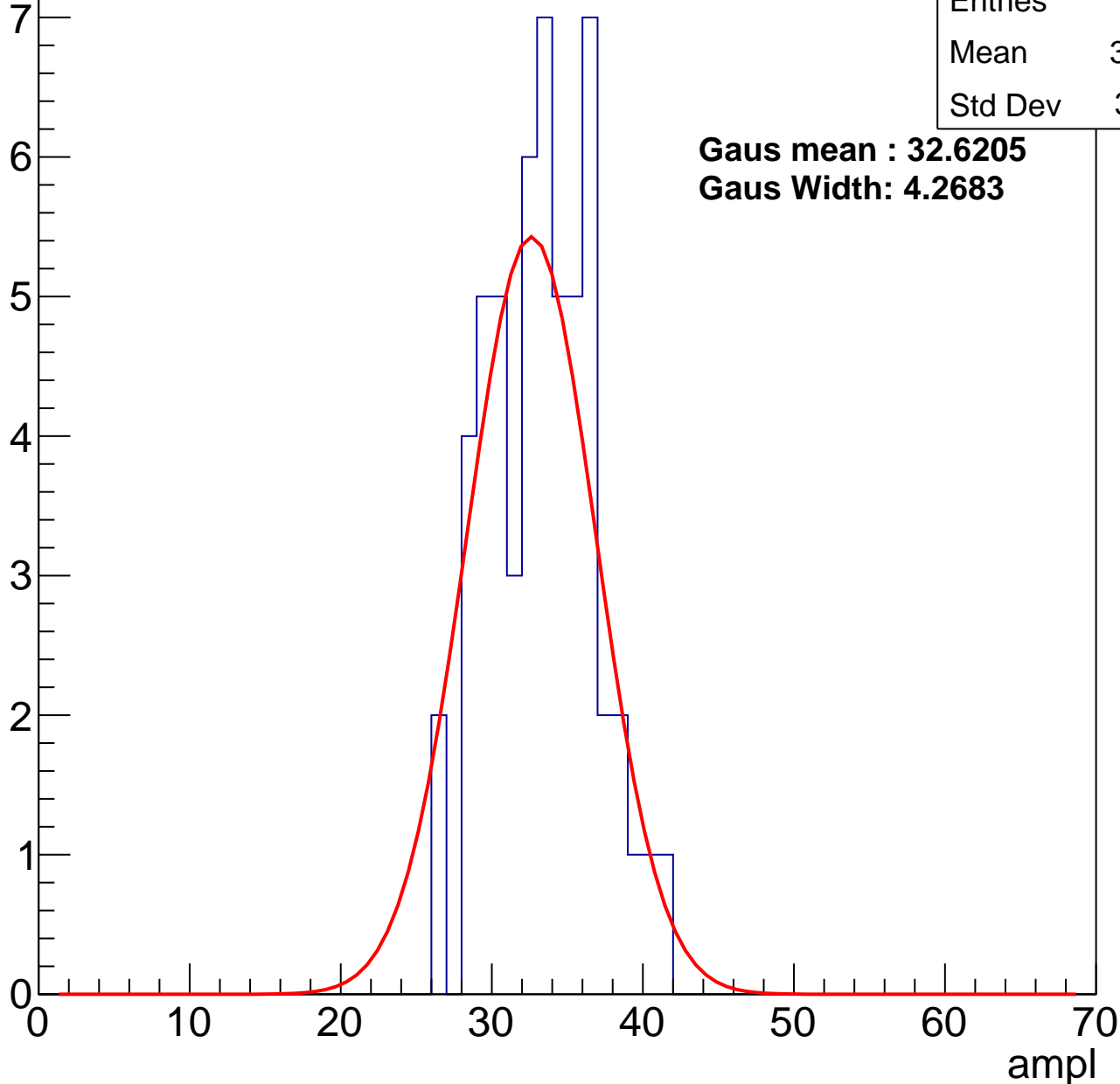
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	32.89
Std Dev	3.431

**Gaus mean : 32.6205**

**Gaus Width: 4.2683**



# B0L001S, U24-ch123, adc1

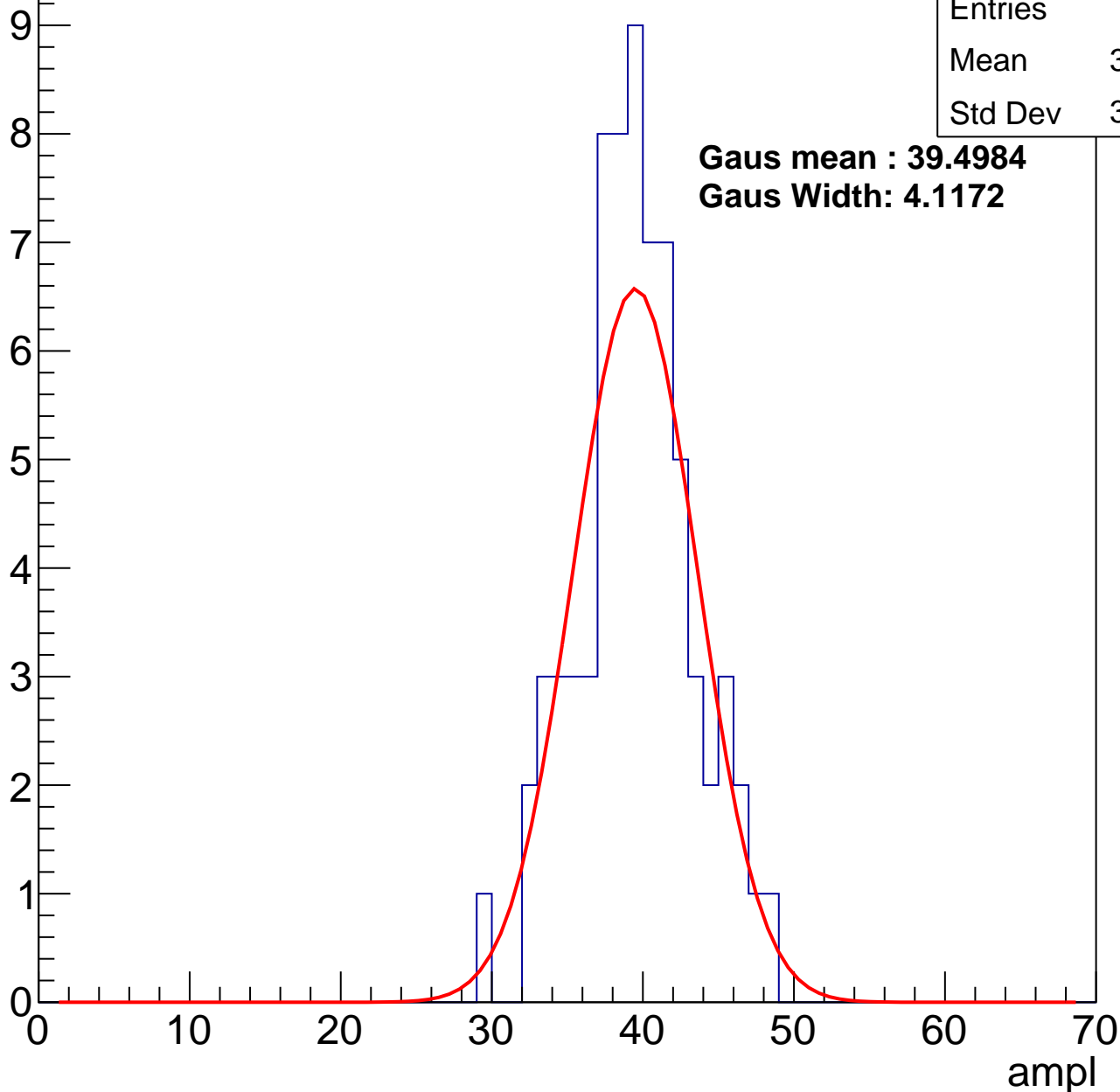
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	39.07
Std Dev	3.799

**Gaus mean : 39.4984**

**Gaus Width: 4.1172**



# B0L001S, U24-ch123, adc2

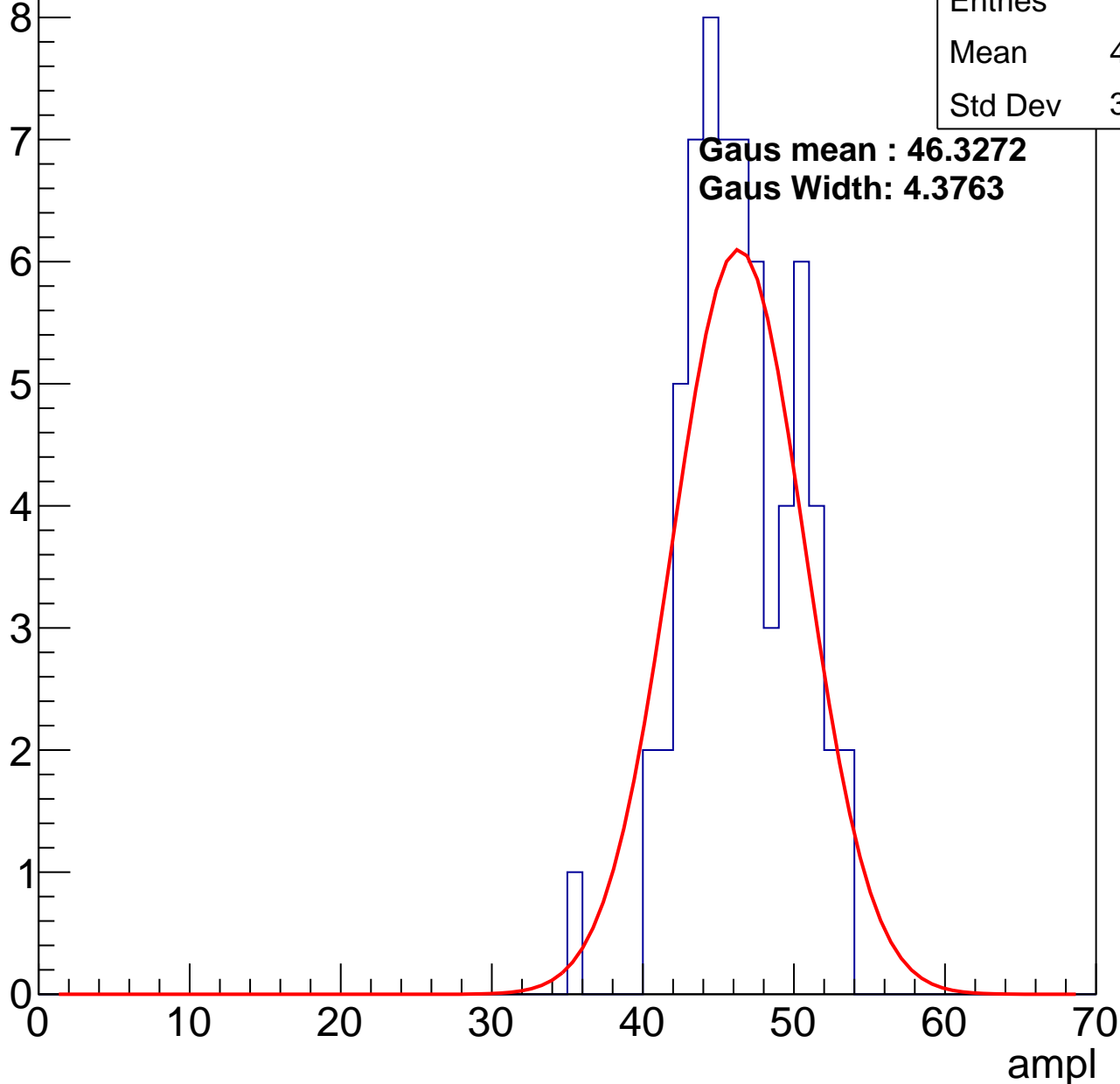
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	45.95
Std Dev	3.578

**Gaus mean : 46.3272**

**Gaus Width: 4.3763**

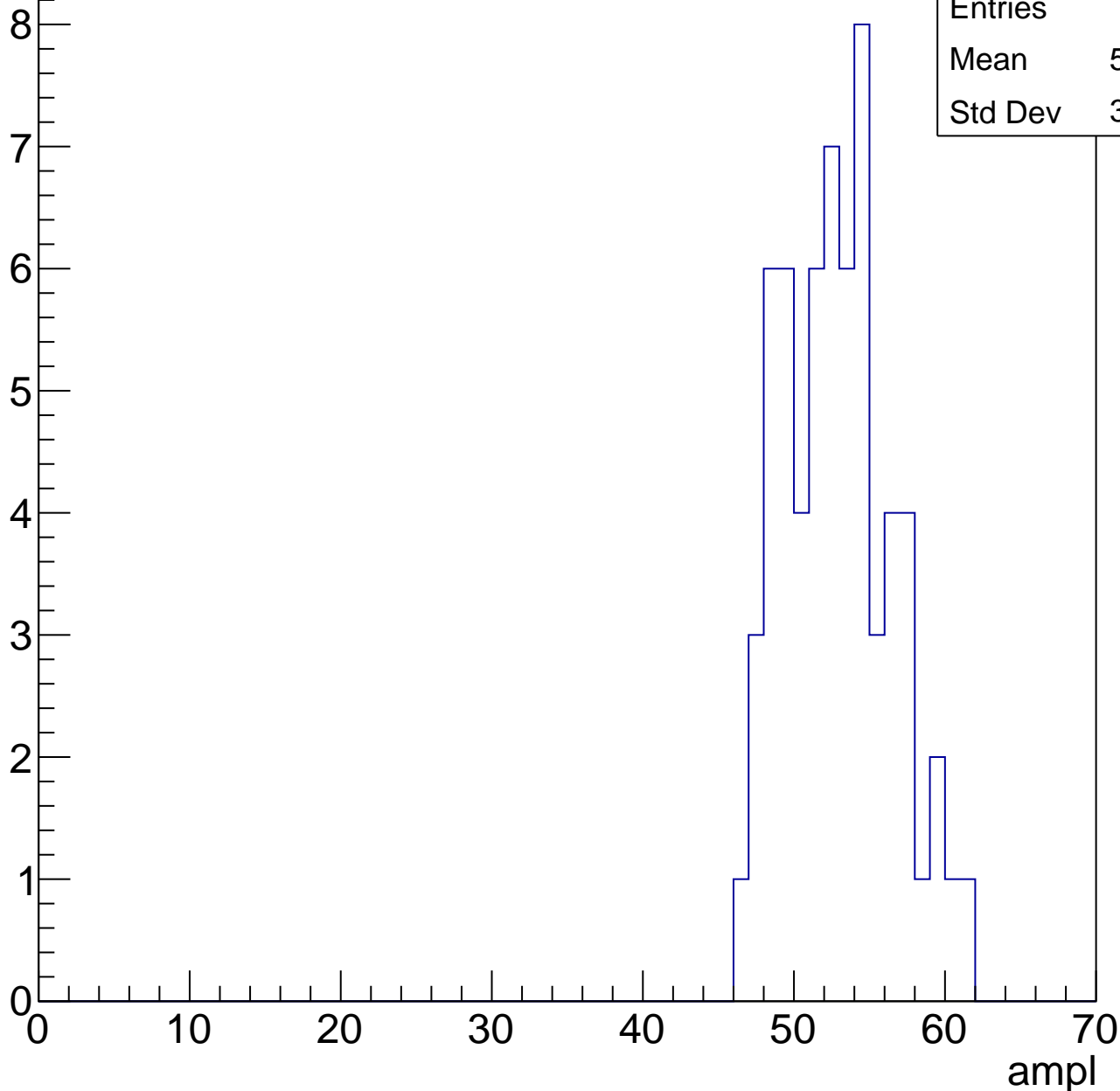


# B0L001S, U24-ch123, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	52.43
Std Dev	3.517

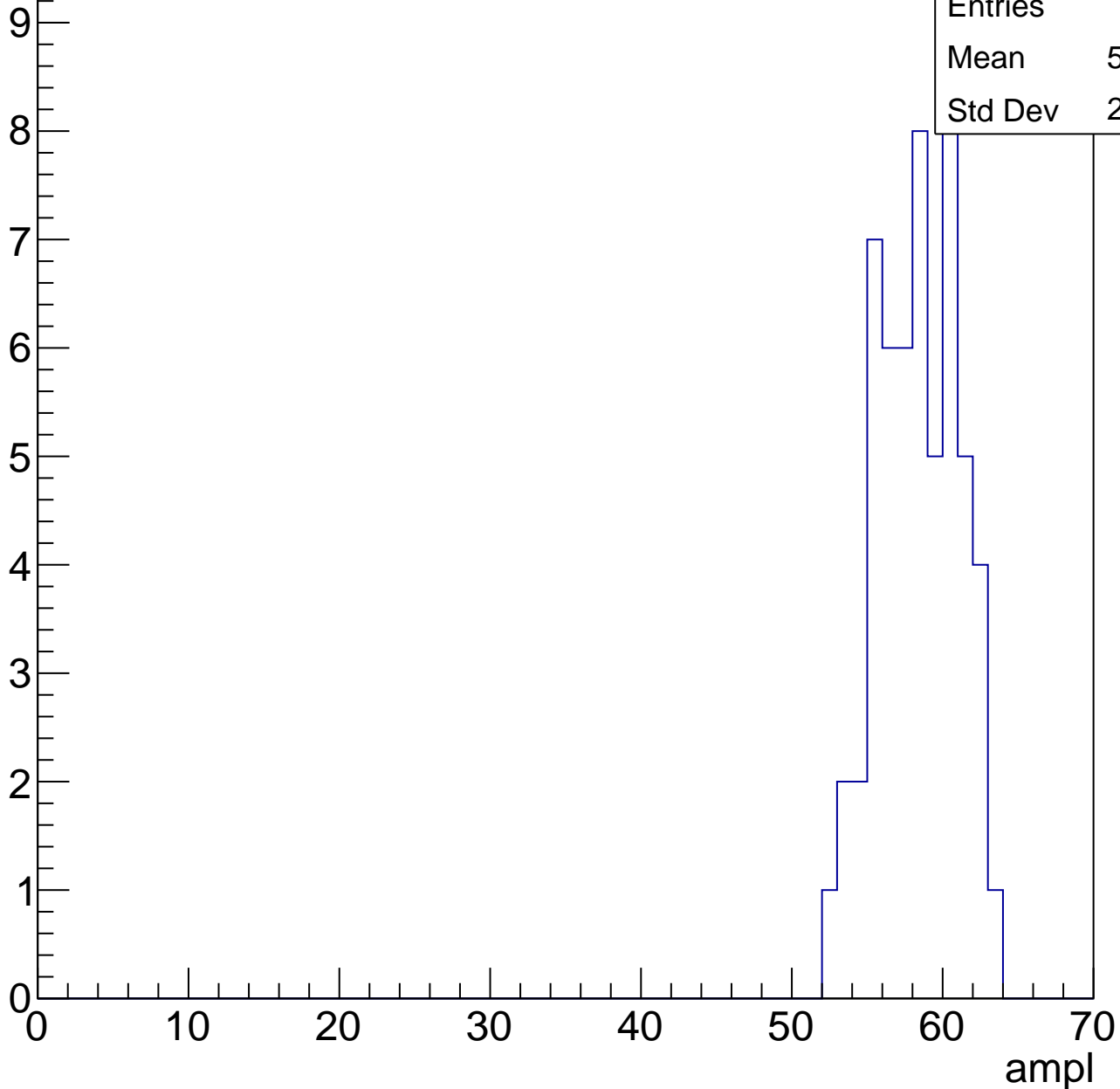


# B0L001S, U24-ch123, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	57.93
Std Dev	2.624

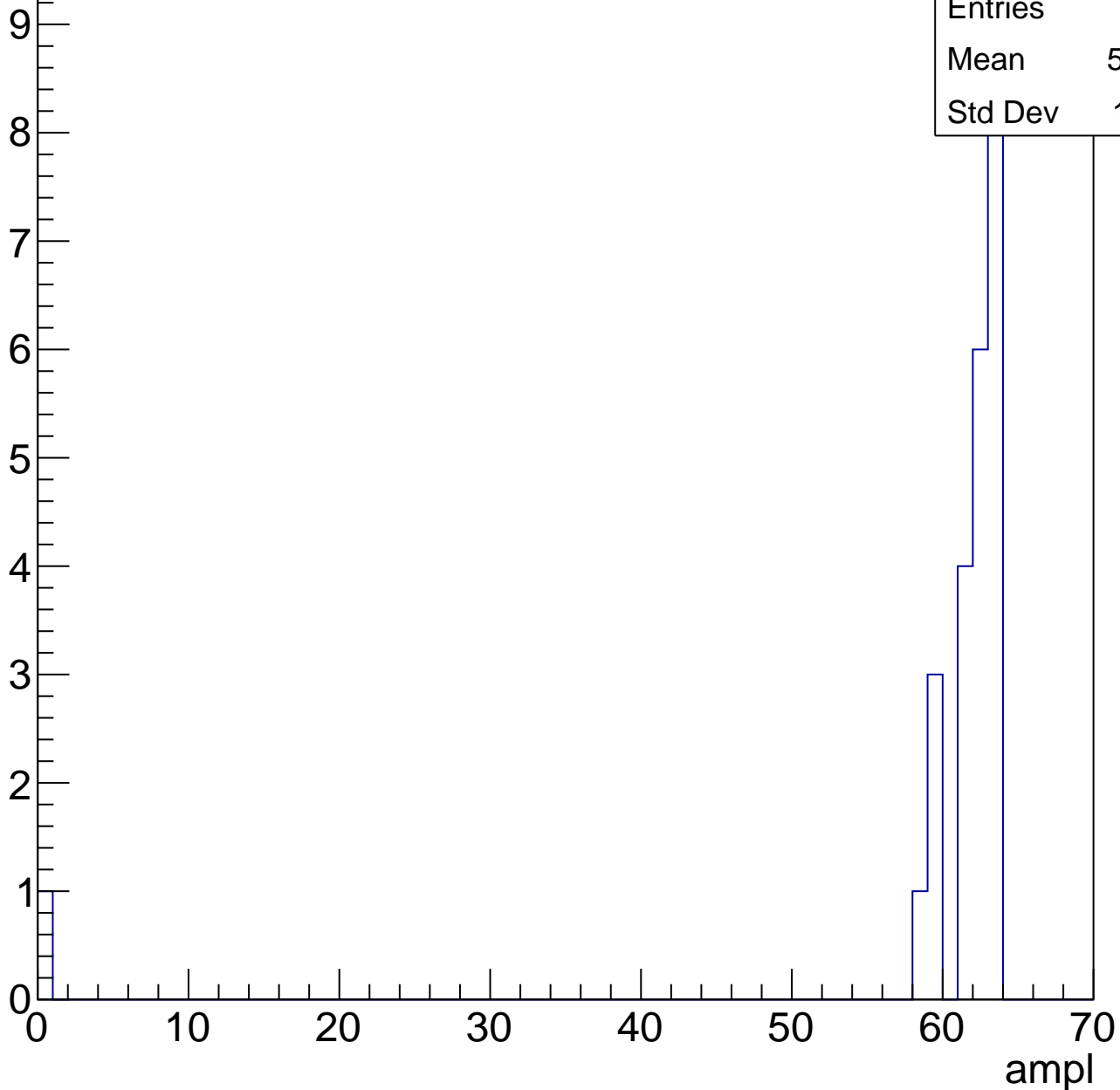


# B0L001S, U24-ch123, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	24
Mean	59.08
Std Dev	12.41



# B0L001S, U24-ch123, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U24-ch123, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	3
Mean	0
Std Dev	0

# B0L001S, U24-ch124, adc0

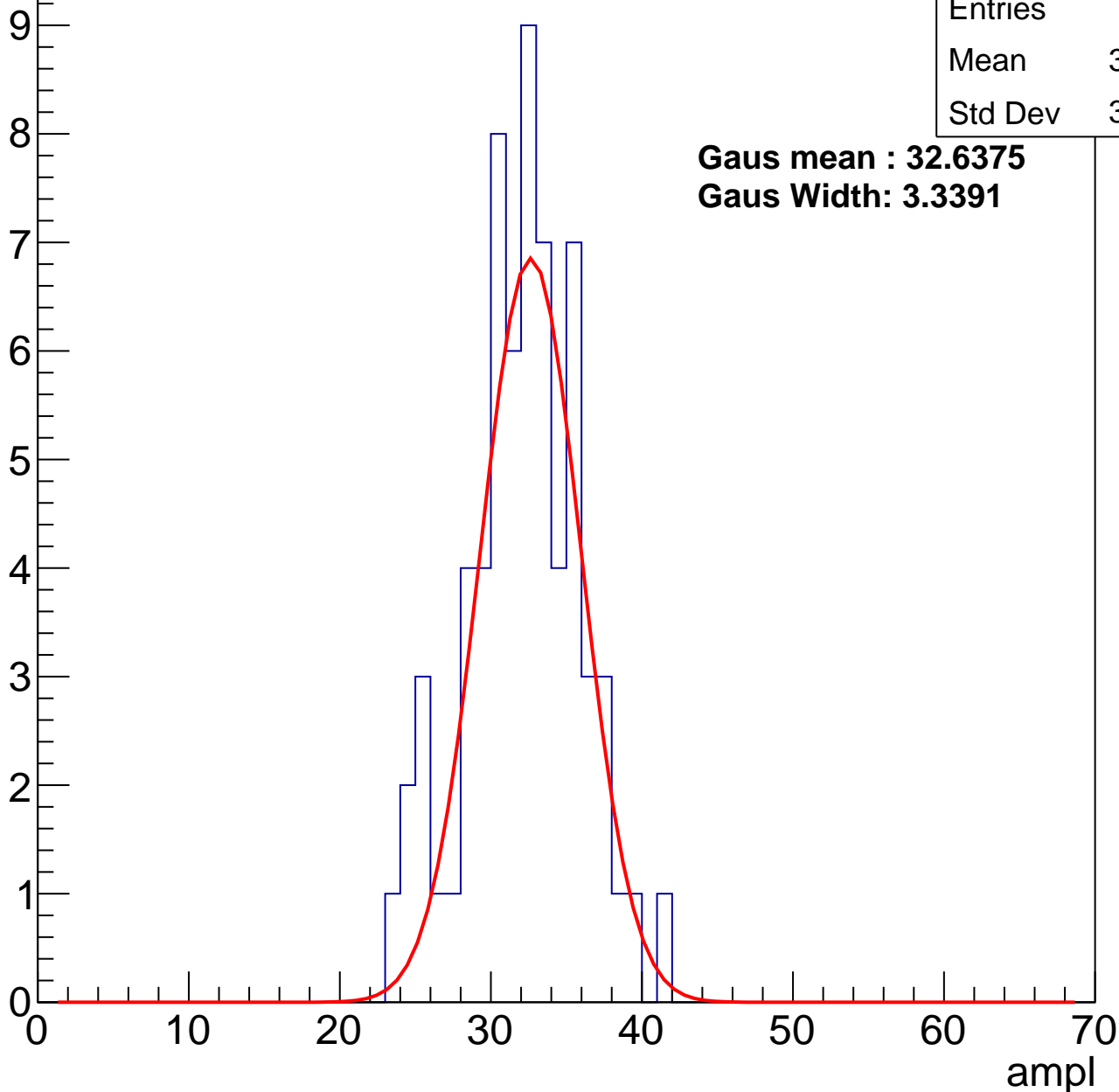
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	31.67
Std Dev	3.739

**Gaus mean : 32.6375**

**Gaus Width: 3.3391**



# B0L001S, U24-ch124, adc1

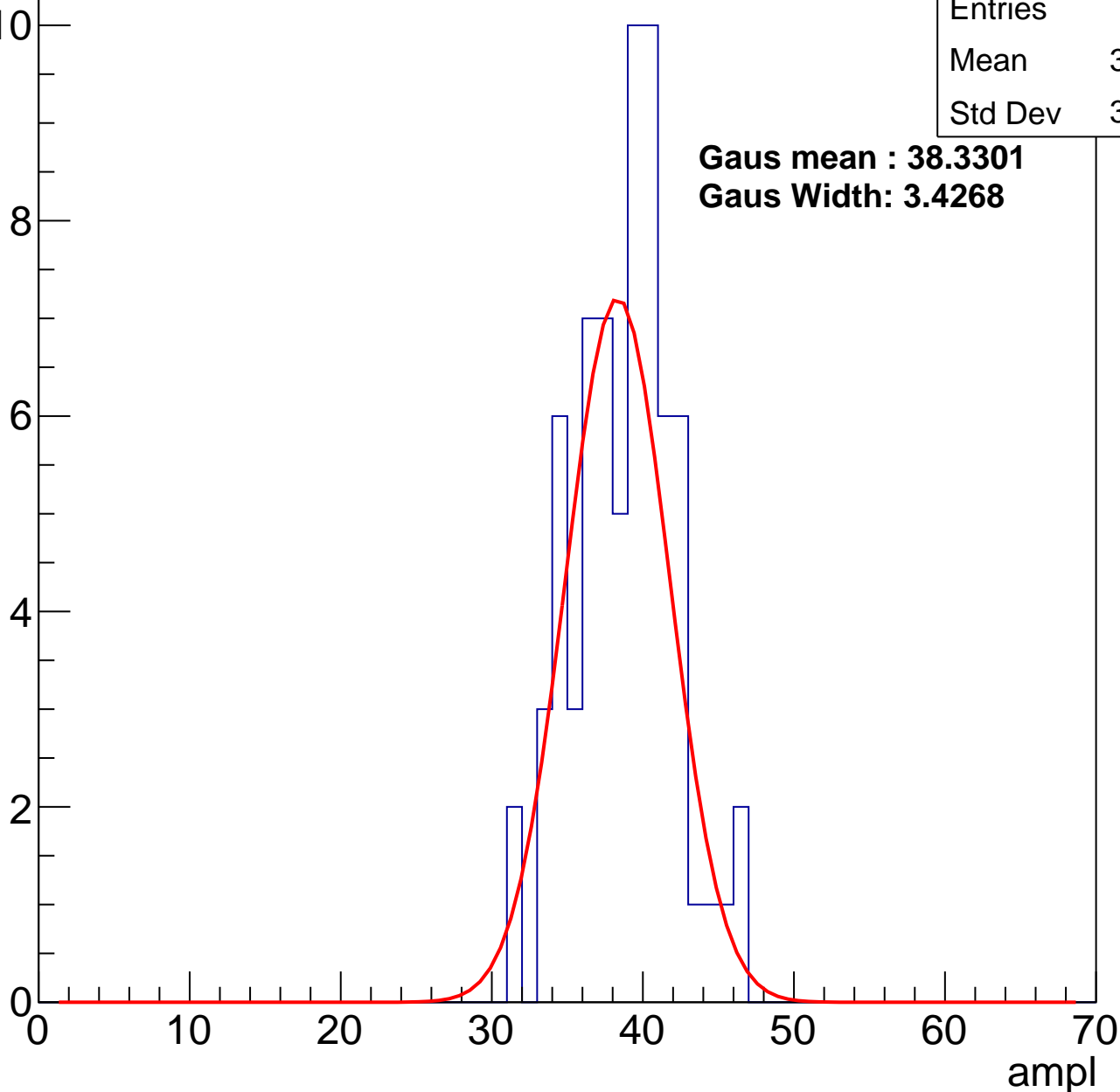
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	38.33
Std Dev	3.298

**Gaus mean : 38.3301**

**Gaus Width: 3.4268**



# B0L001S, U24-ch124, adc2

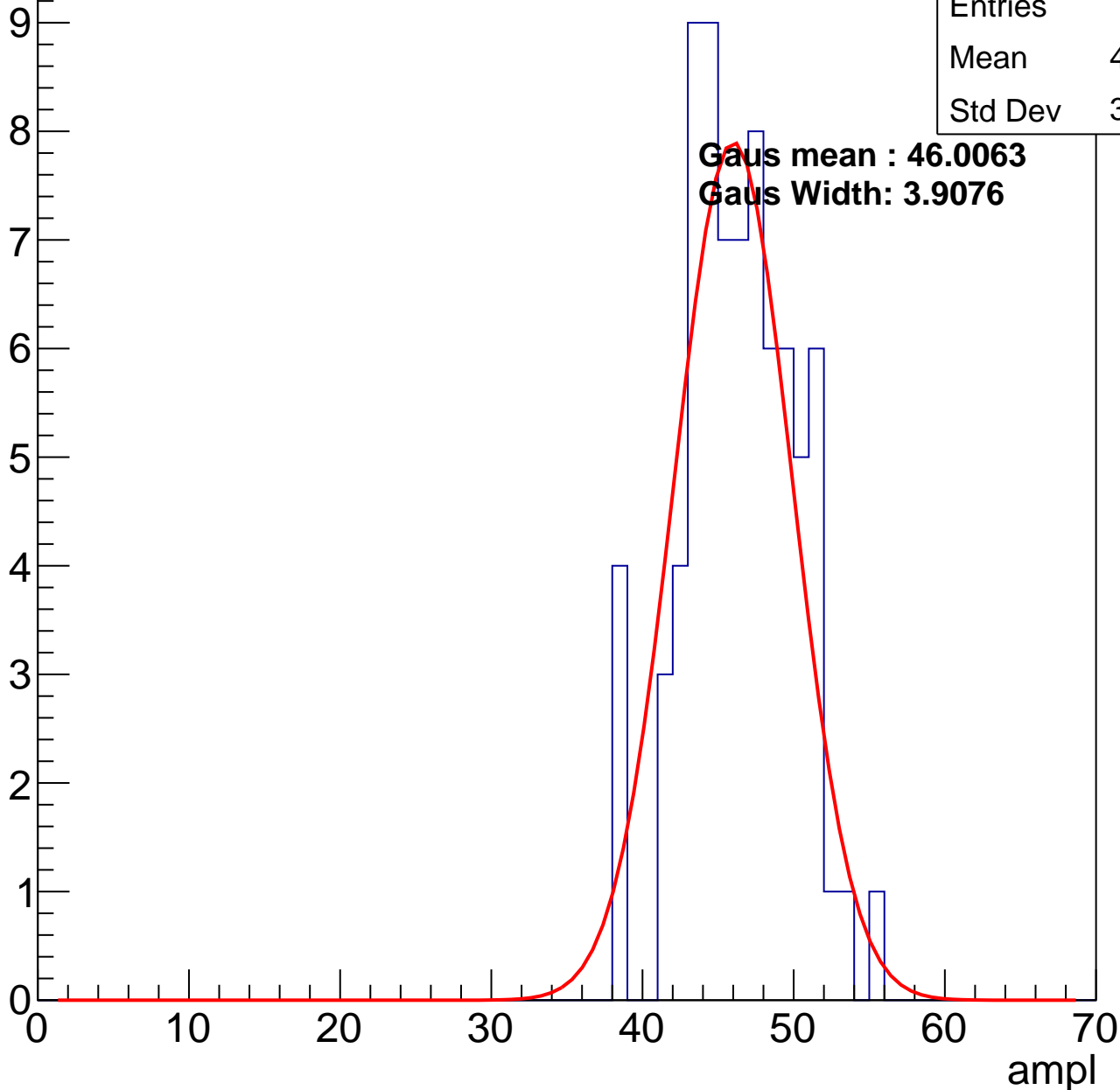
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	77
Mean	45.94
Std Dev	3.605

**Gaus mean : 46.0063**

**Gaus Width: 3.9076**

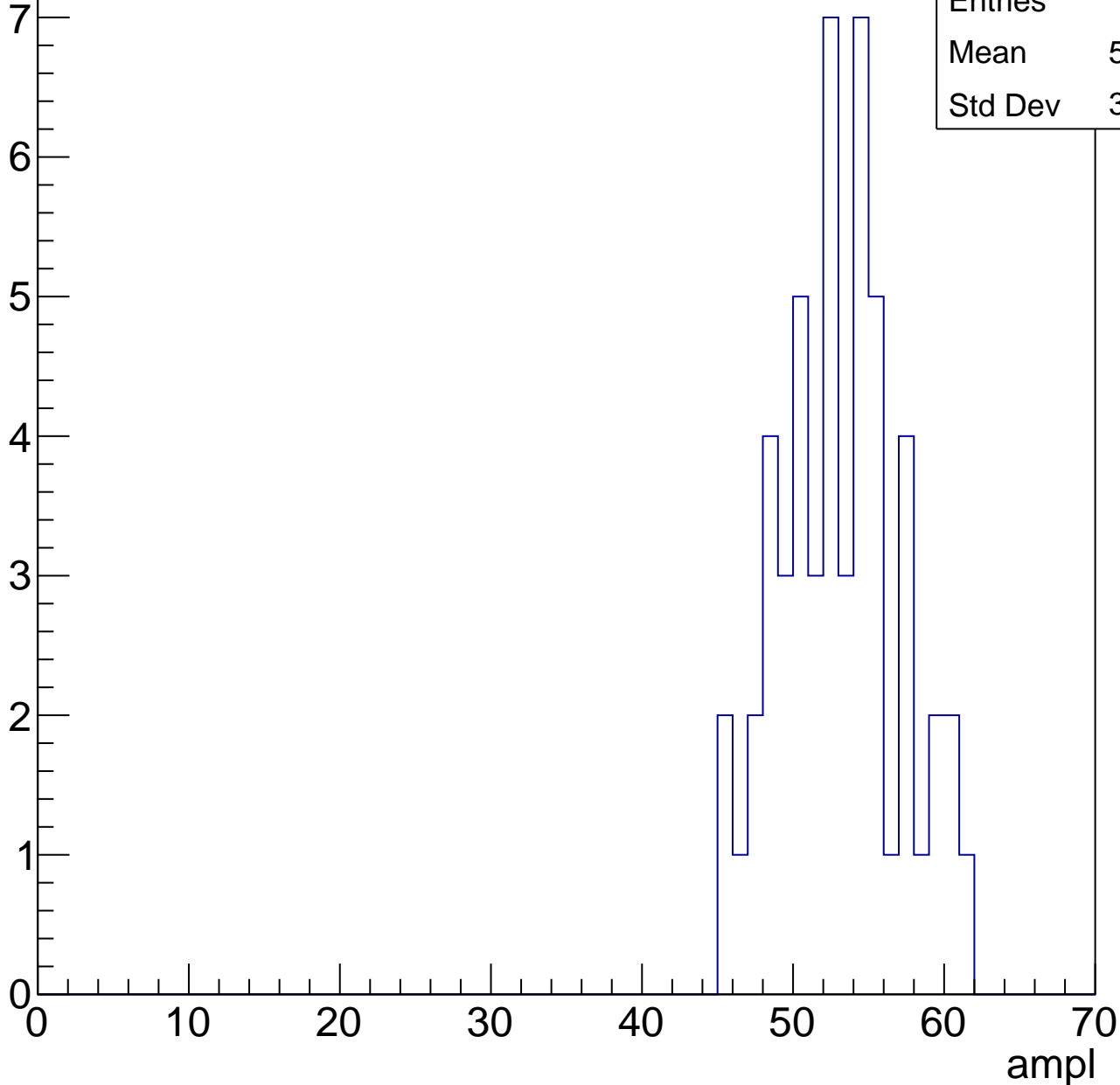


# B0L001S, U24-ch124, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	52.62
Std Dev	3.915

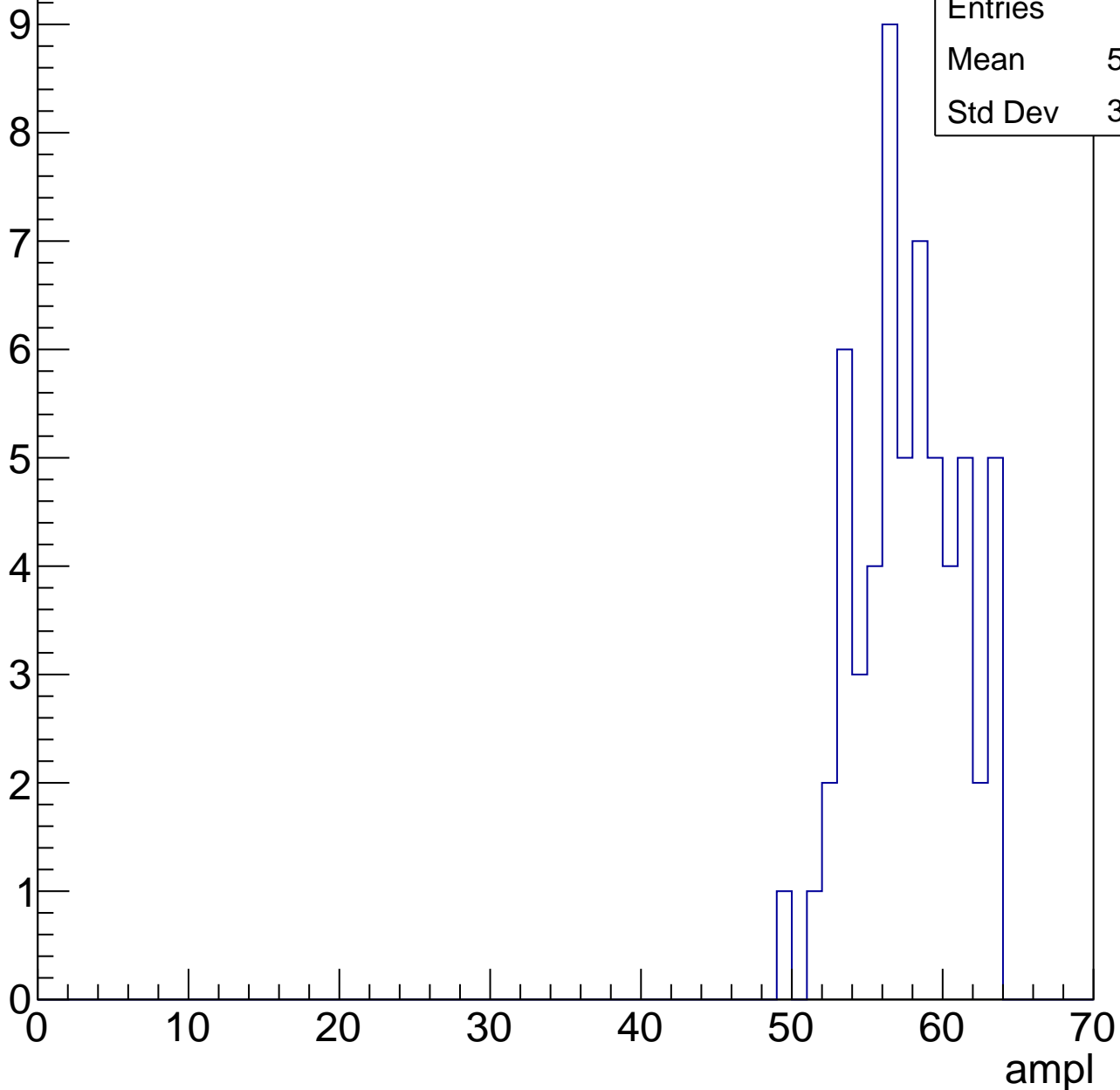


# B0L001S, U24-ch124, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	57.25
Std Dev	3.363

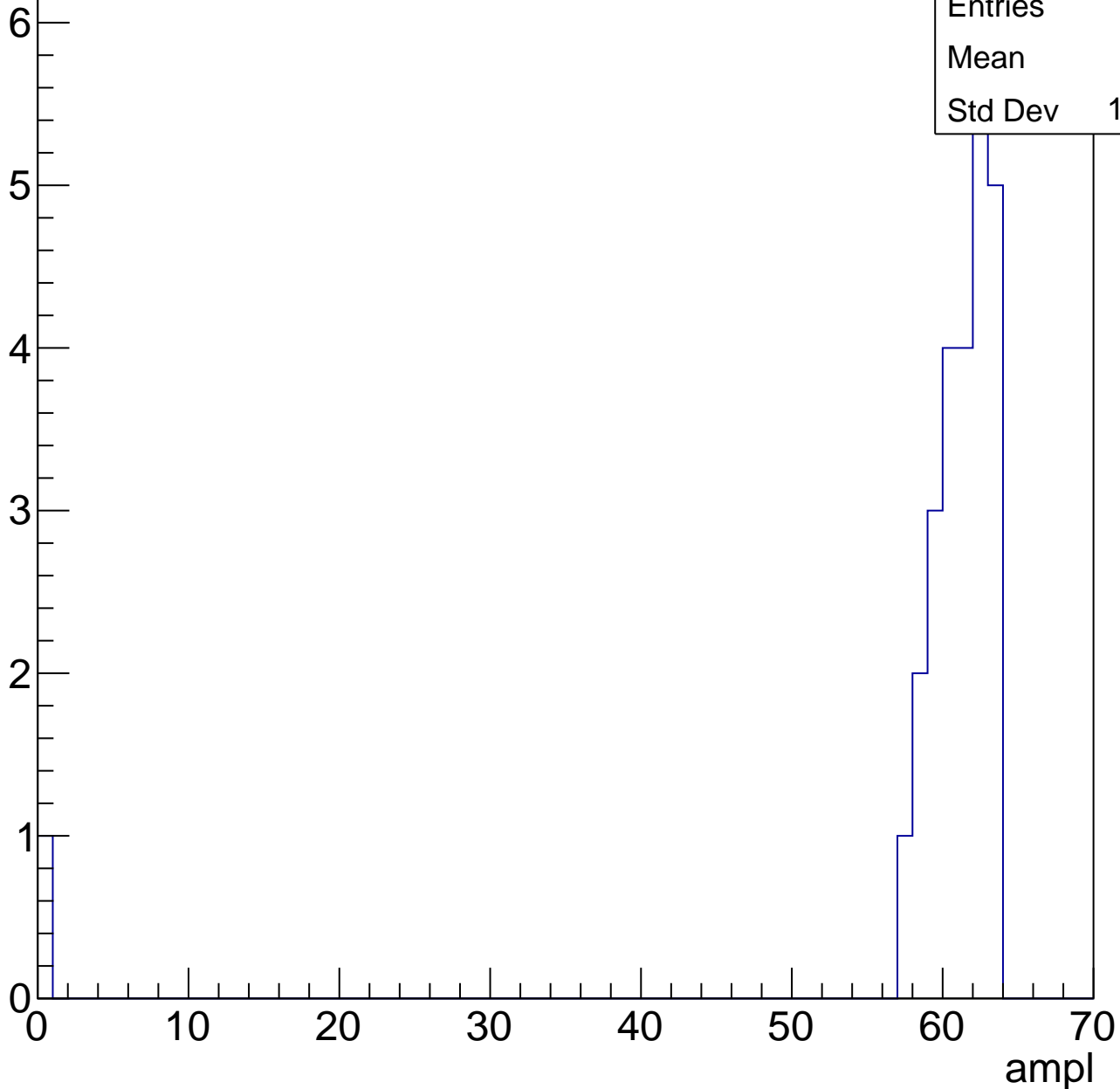


# B0L001S, U24-ch124, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	26
Mean	58.5
Std Dev	11.82



# B0L001S, U24-ch124, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch124, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U24-ch125, adc0

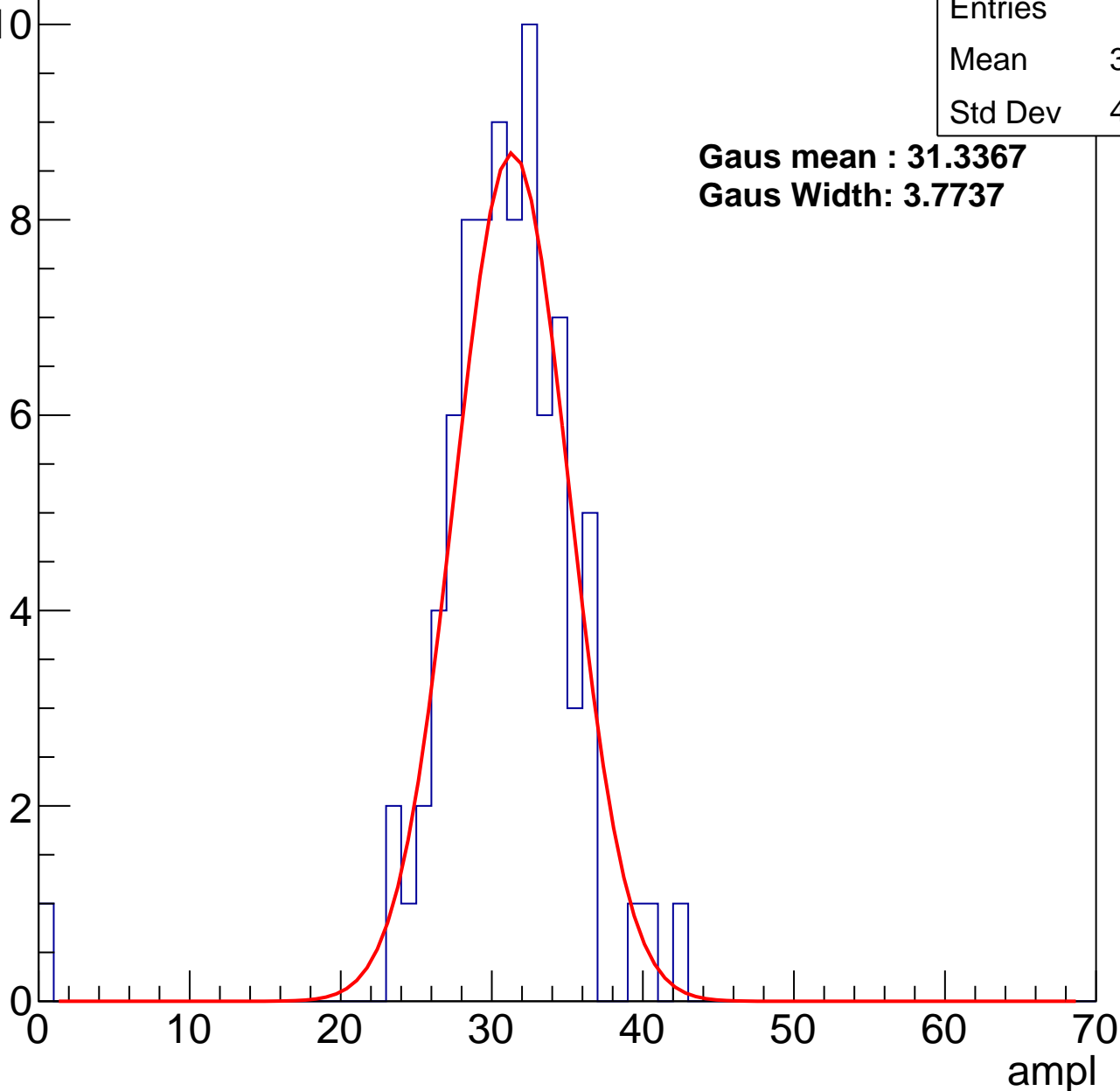
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	83
Mean	30.39
Std Dev	4.938

**Gaus mean : 31.3367**

**Gaus Width: 3.7737**



# B0L001S, U24-ch125, adc1

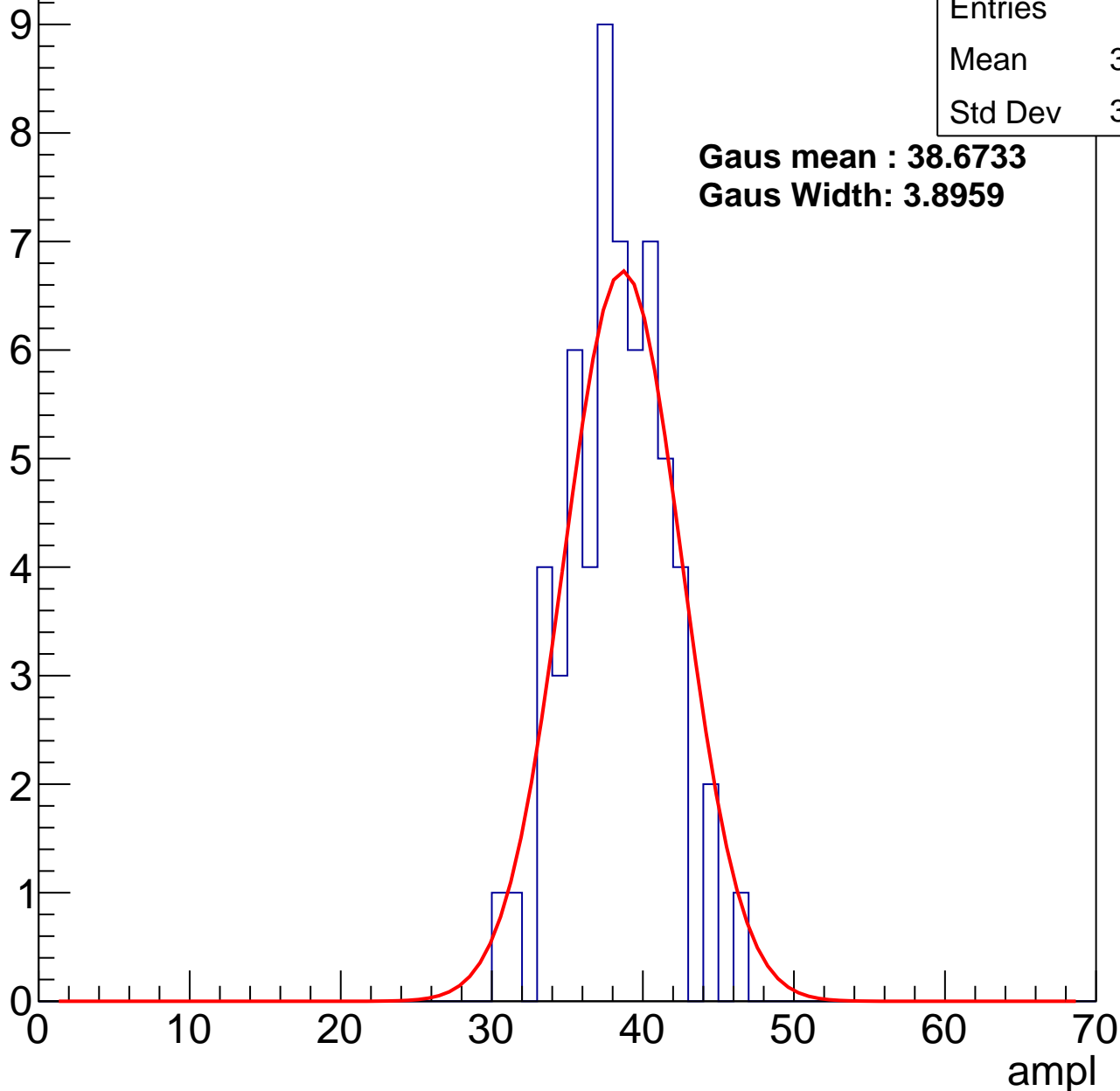
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	37.82
Std Dev	3.207

**Gaus mean : 38.6733**

**Gaus Width: 3.8959**



# B0L001S, U24-ch125, adc2

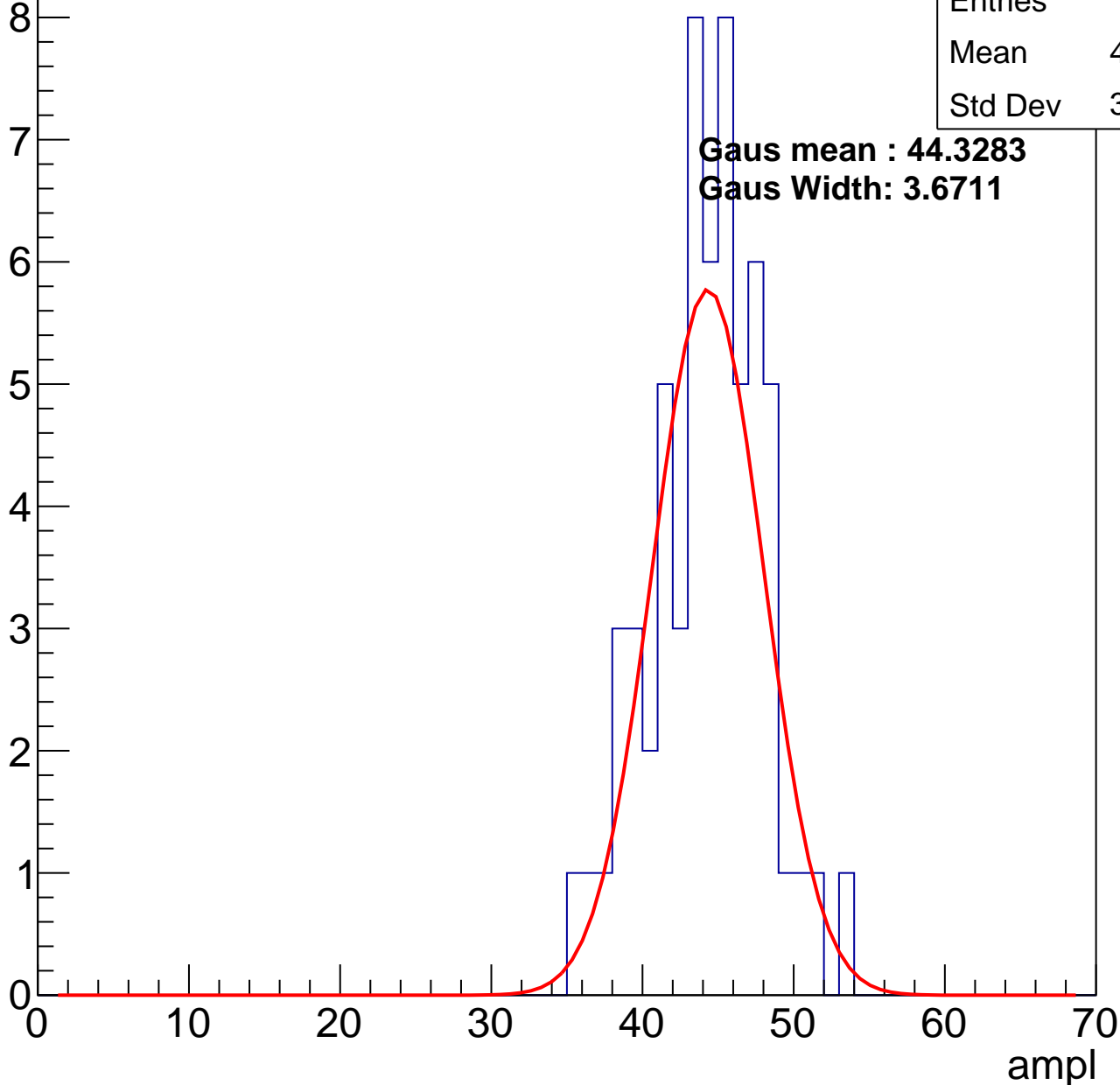
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	43.82
Std Dev	3.678

**Gaus mean : 44.3283**

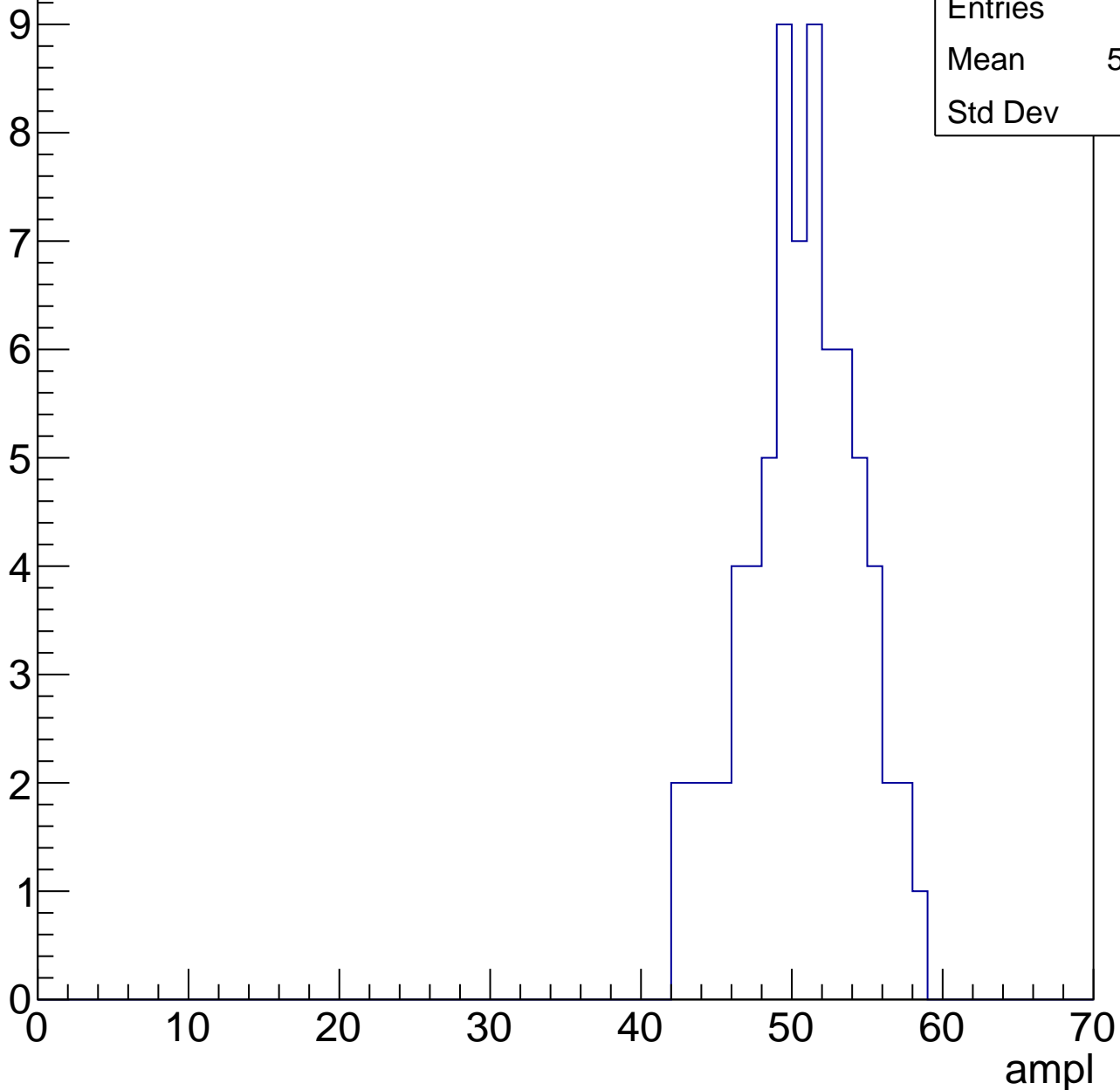
**Gaus Width: 3.6711**



# B0L001S, U24-ch125, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

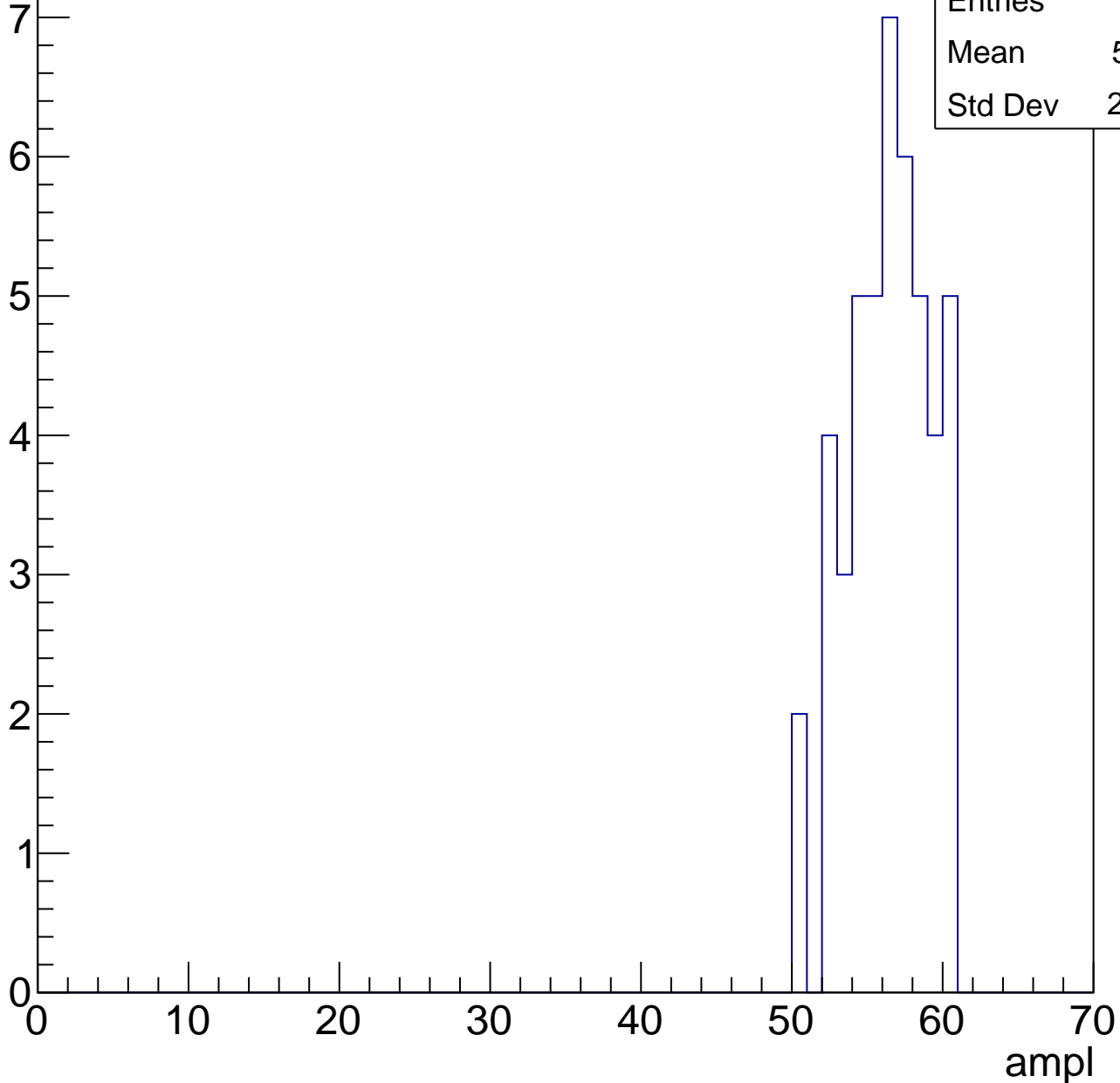


# B0L001S, U24-ch125, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	46
Mean	55.91
Std Dev	2.677

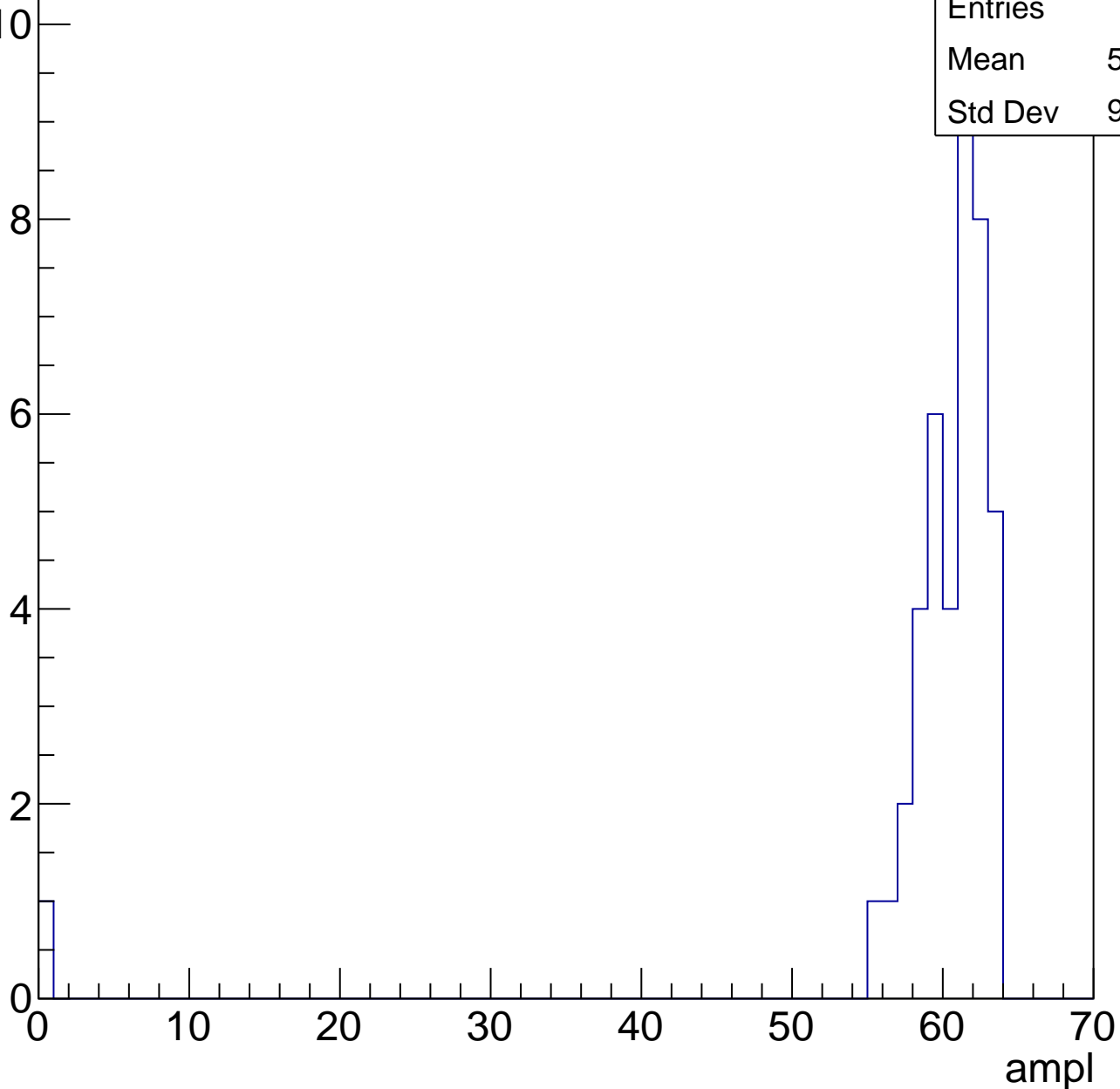


# B0L001S, U24-ch125, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	42
Mean	58.86
Std Dev	9.403

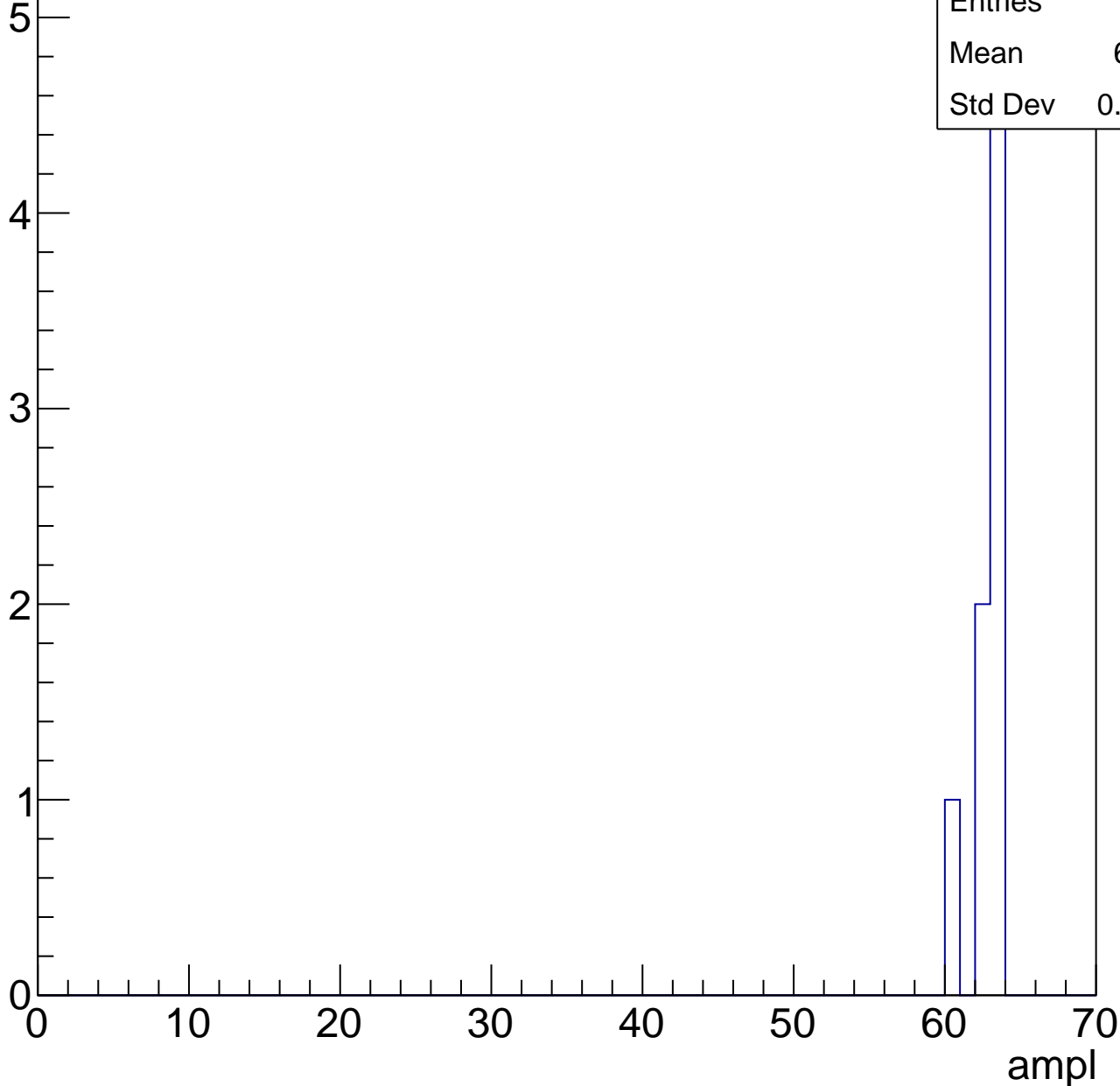


# B0L001S, U24-ch125, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	8
Mean	62.38
Std Dev	0.9922





# B0L001S, U24-ch125, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U24-ch126, adc0

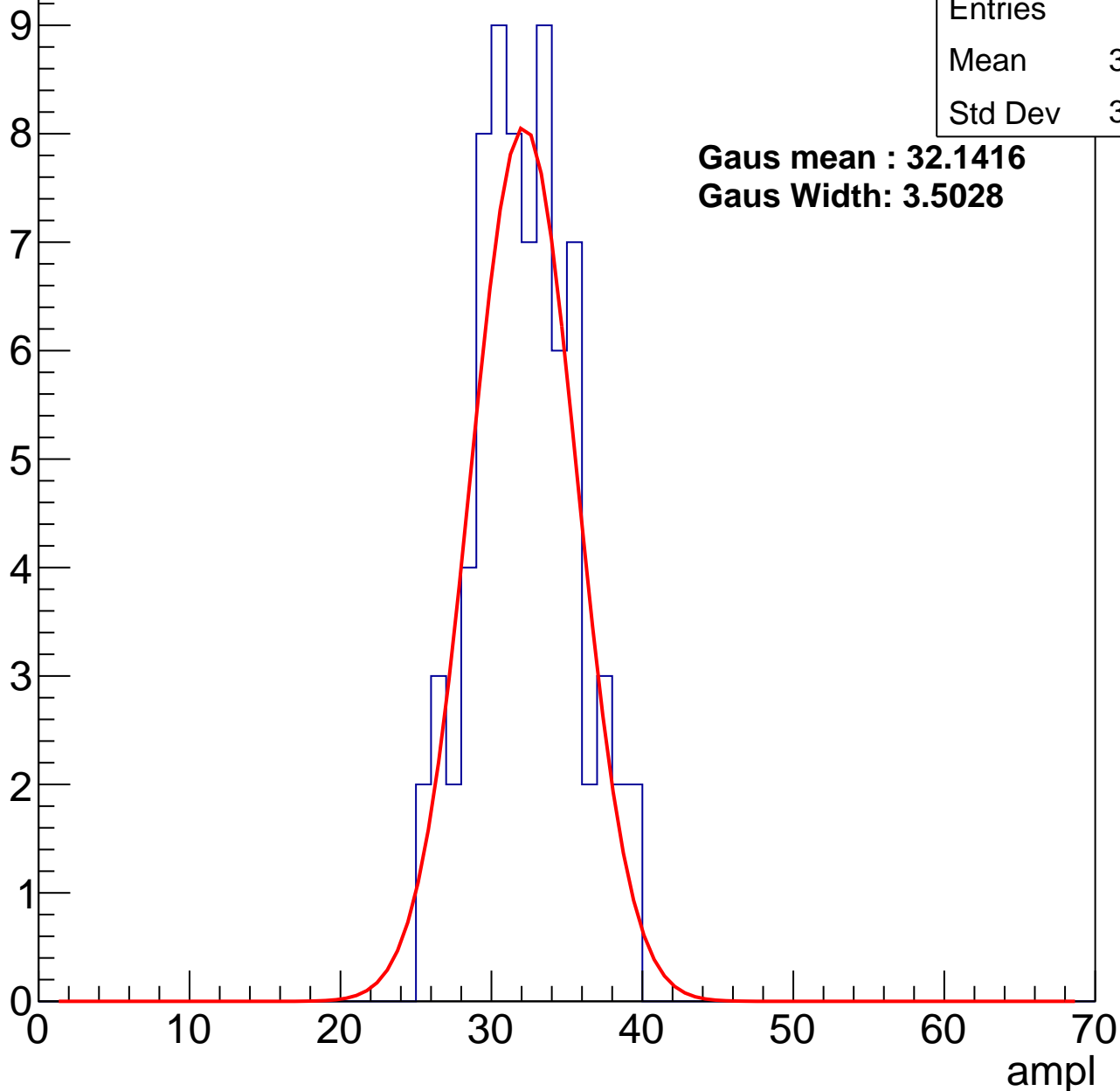
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	31.77
Std Dev	3.298

**Gaus mean : 32.1416**

**Gaus Width: 3.5028**



# B0L001S, U24-ch126, adc1

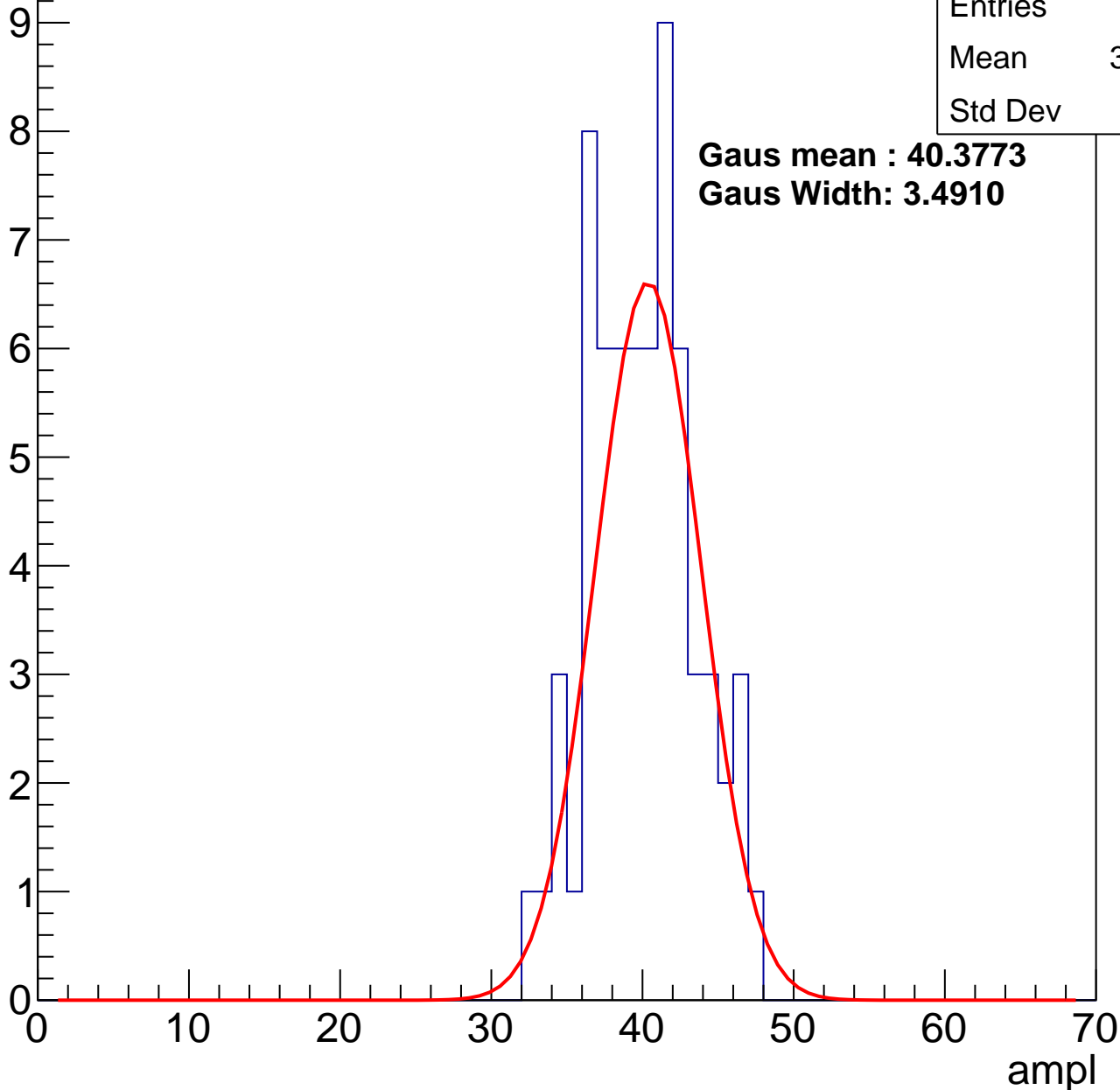
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	39.55
Std Dev	3.42

**Gaus mean : 40.3773**

**Gaus Width: 3.4910**



# B0L001S, U24-ch126, adc2

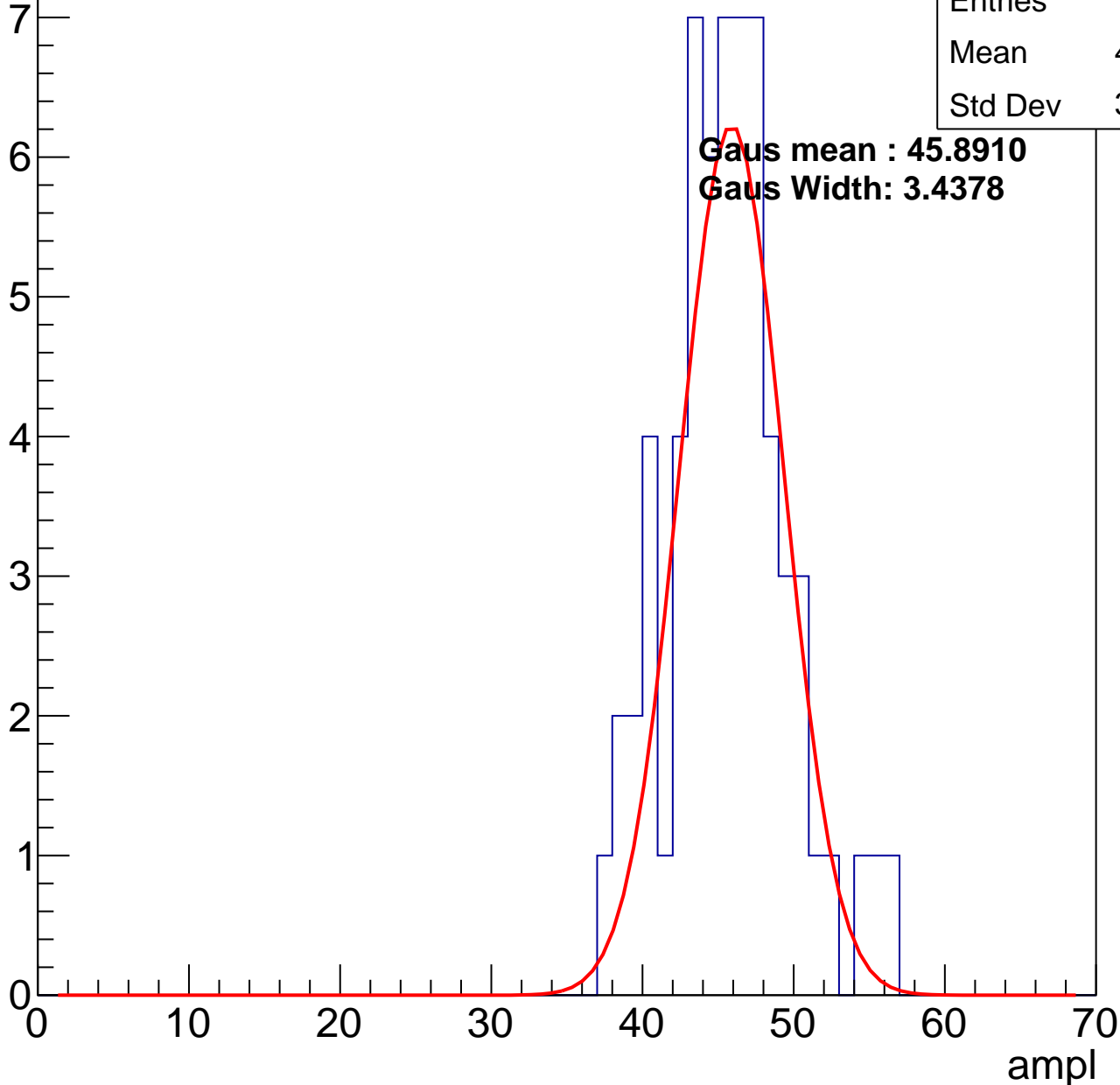
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	45.21
Std Dev	3.981

**Gaus mean : 45.8910**

**Gaus Width: 3.4378**

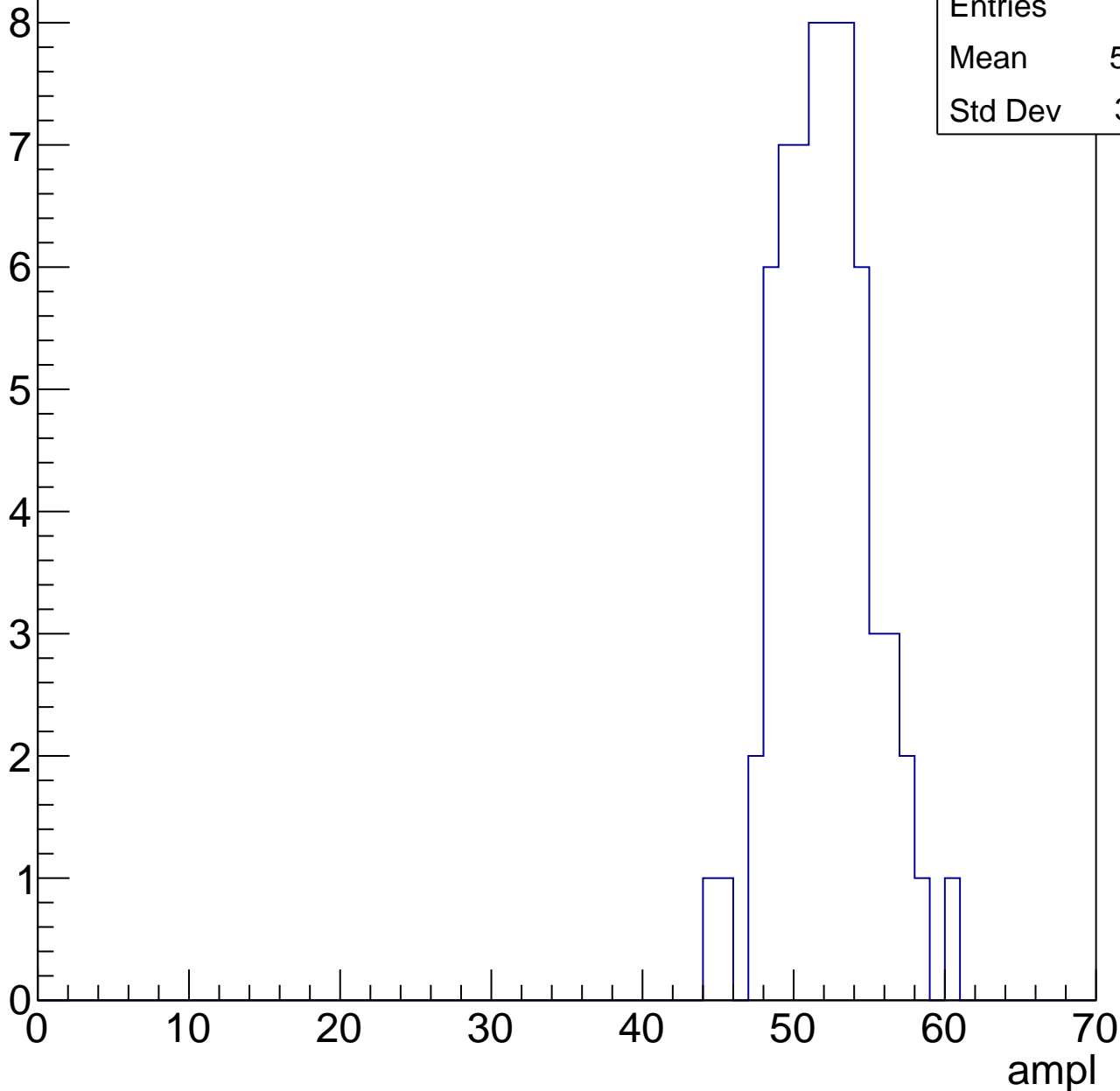


# B0L001S, U24-ch126, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	51.58
Std Dev	3.071

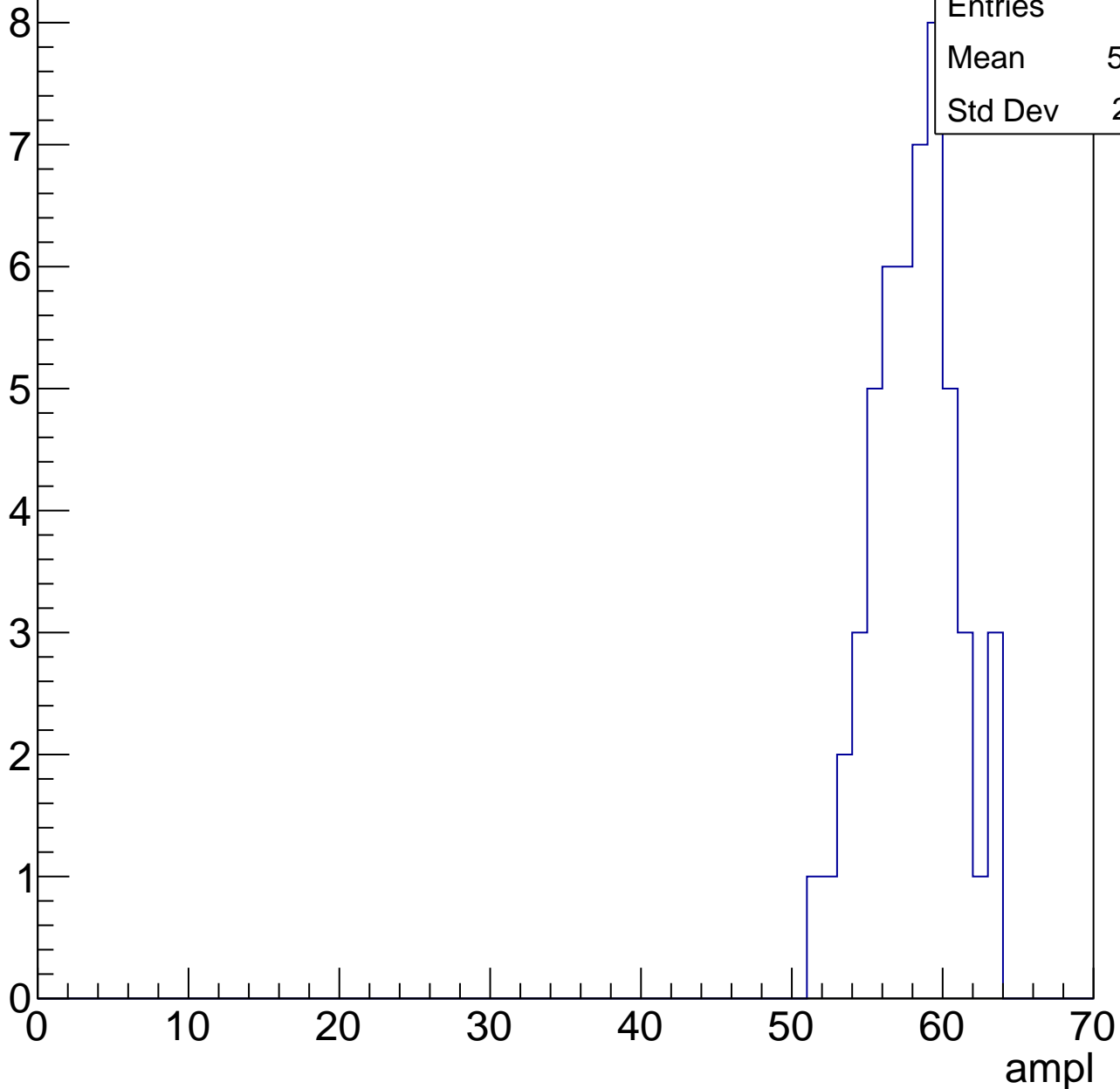


# B0L001S, U24-ch126, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	51
Mean	57.57
Std Dev	2.781

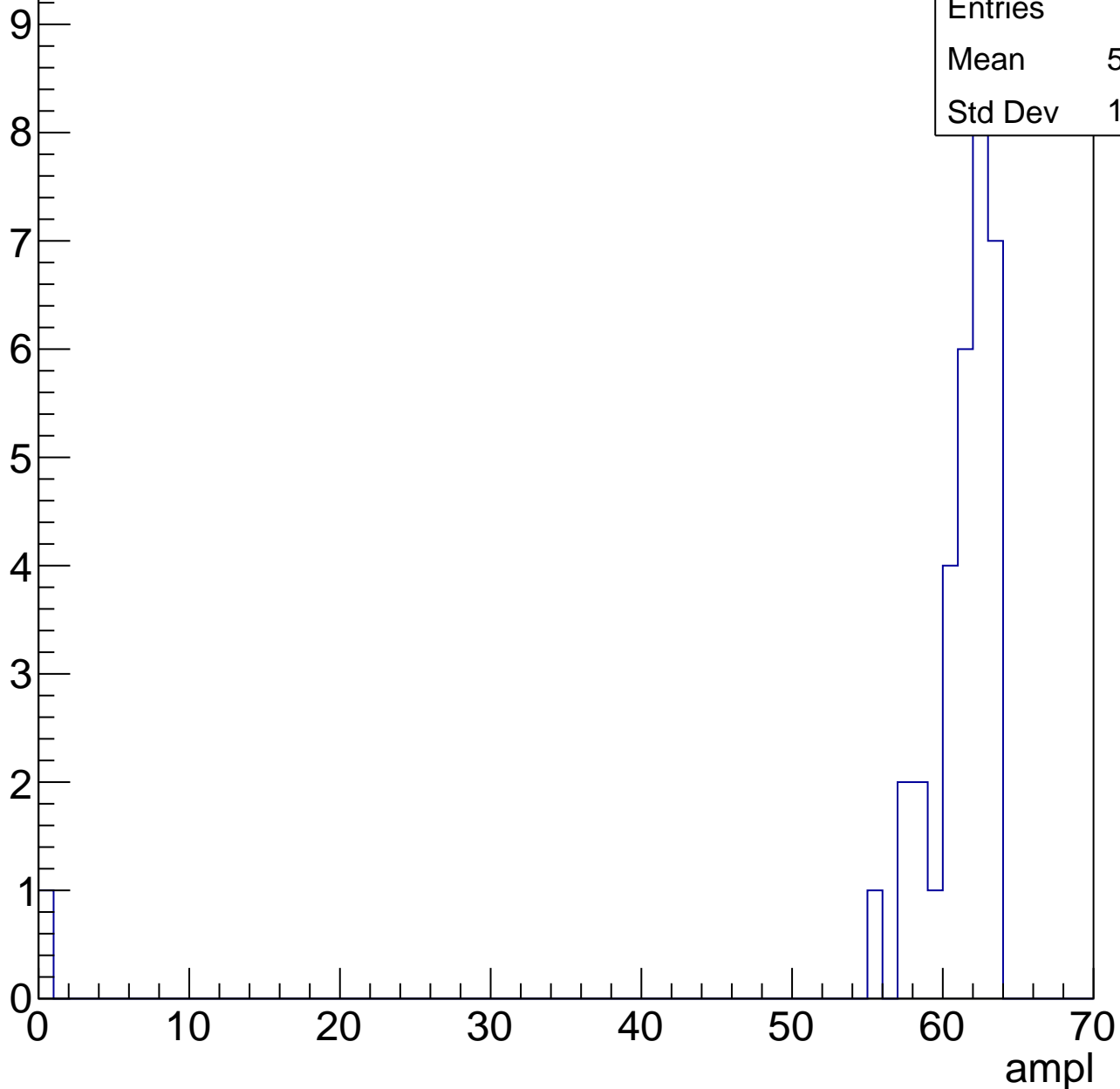


# B0L001S, U24-ch126, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

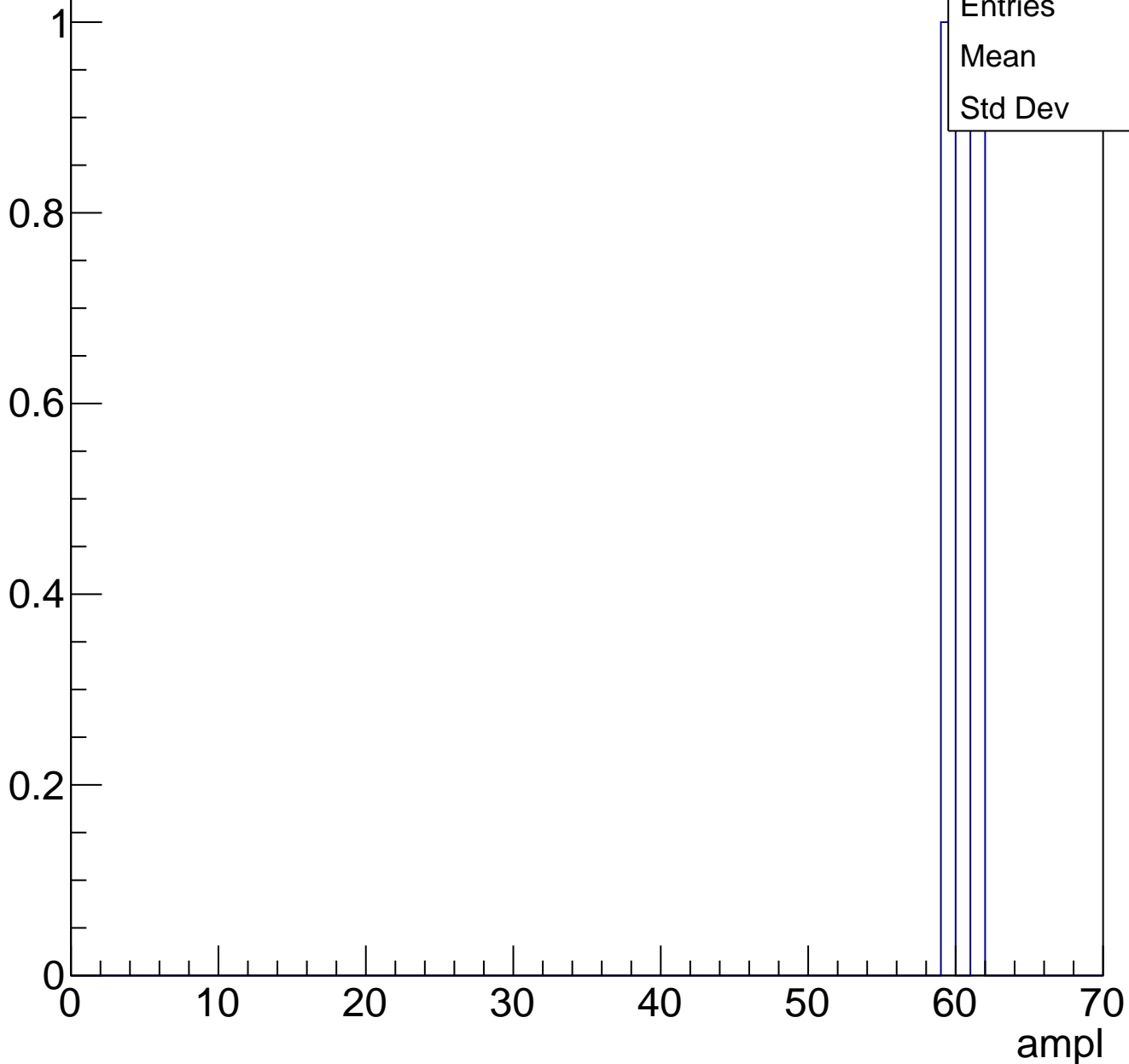
Entries	33
Mean	59.06
Std Dev	10.63



# B0L001S, U24-ch126, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

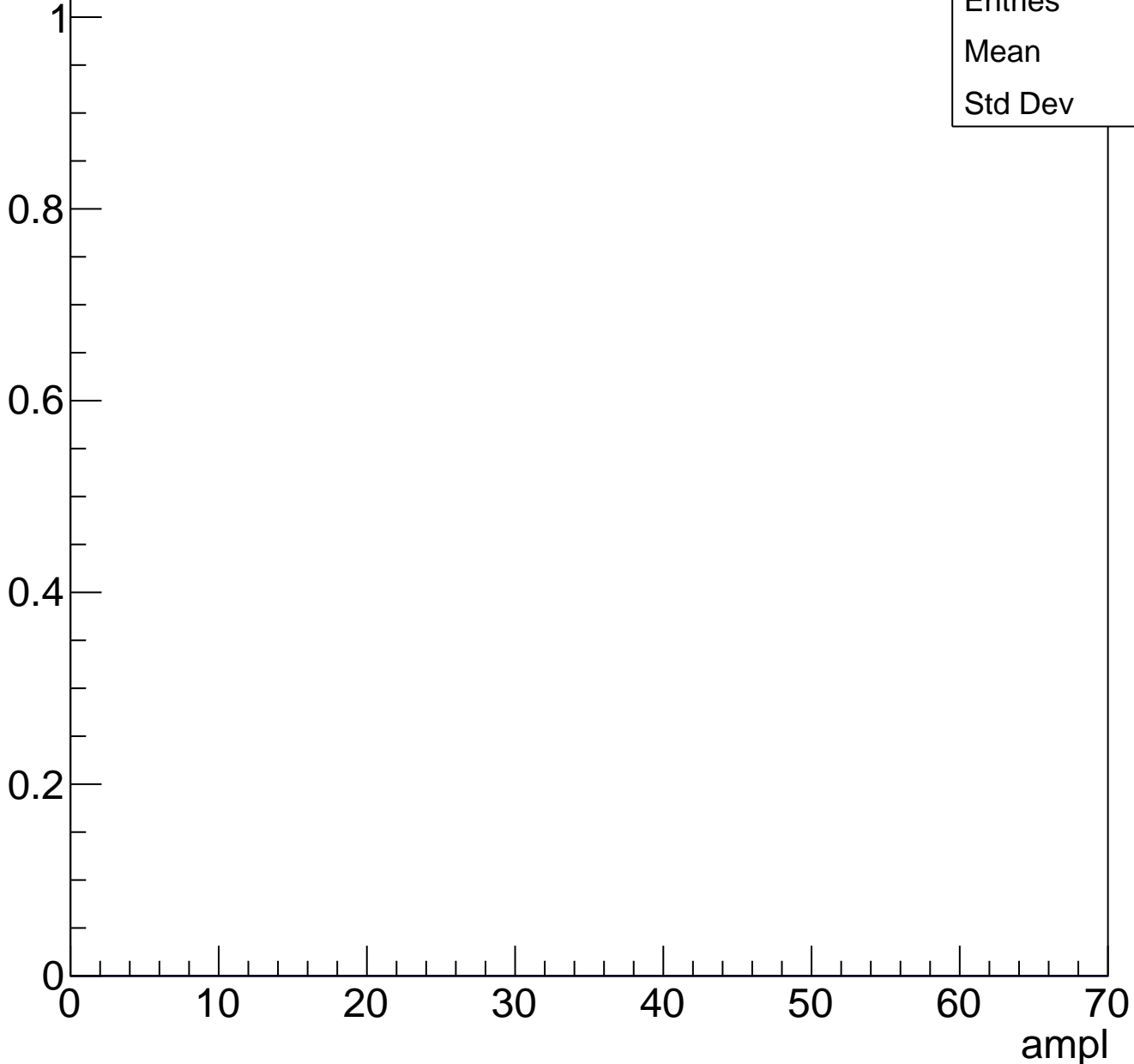




# B0L001S, U24-ch126, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U24-ch127, adc0

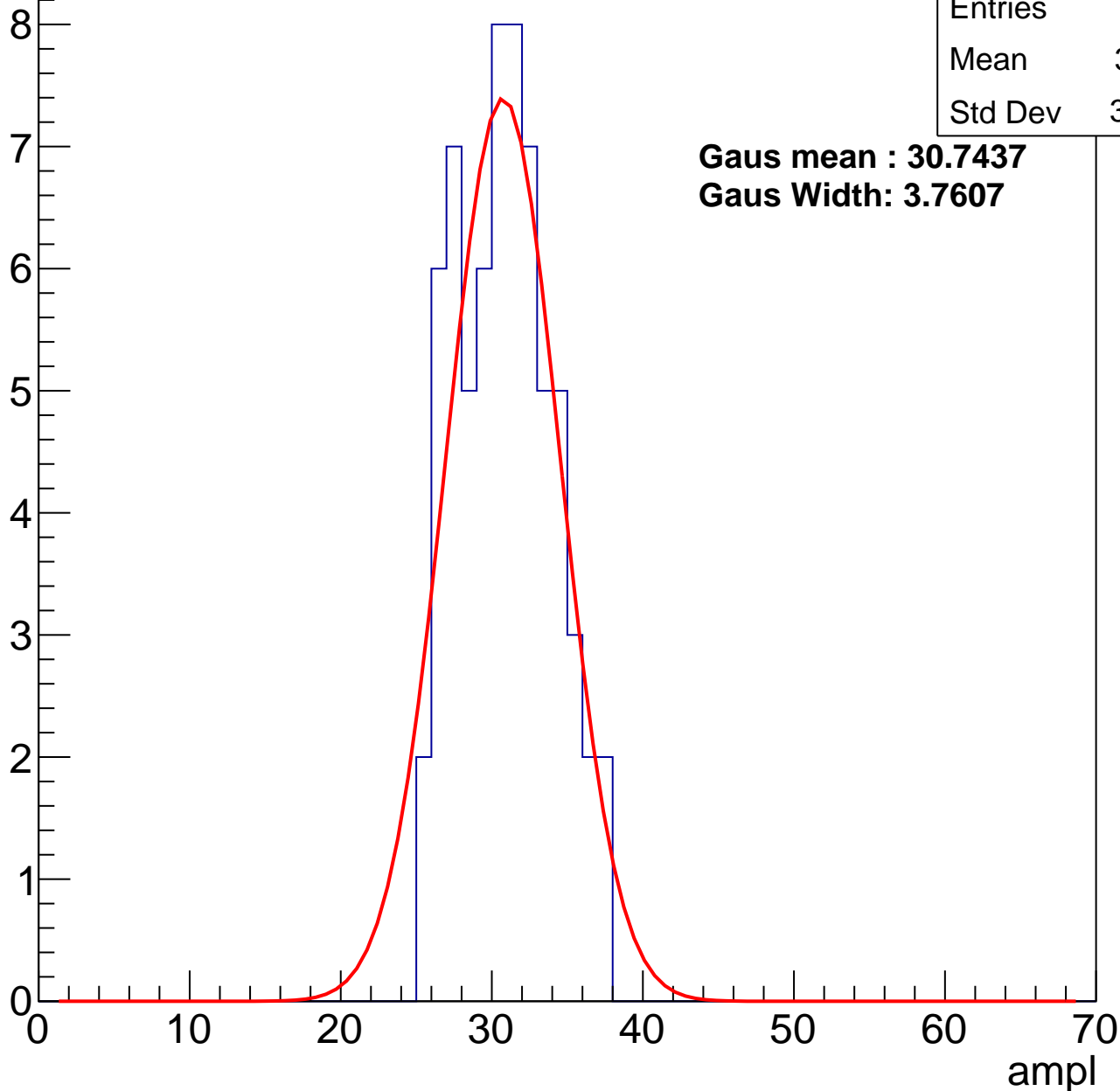
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	30.41
Std Dev	3.089

**Gaus mean : 30.7437**

**Gaus Width: 3.7607**



# B0L001S, U24-ch127, adc1

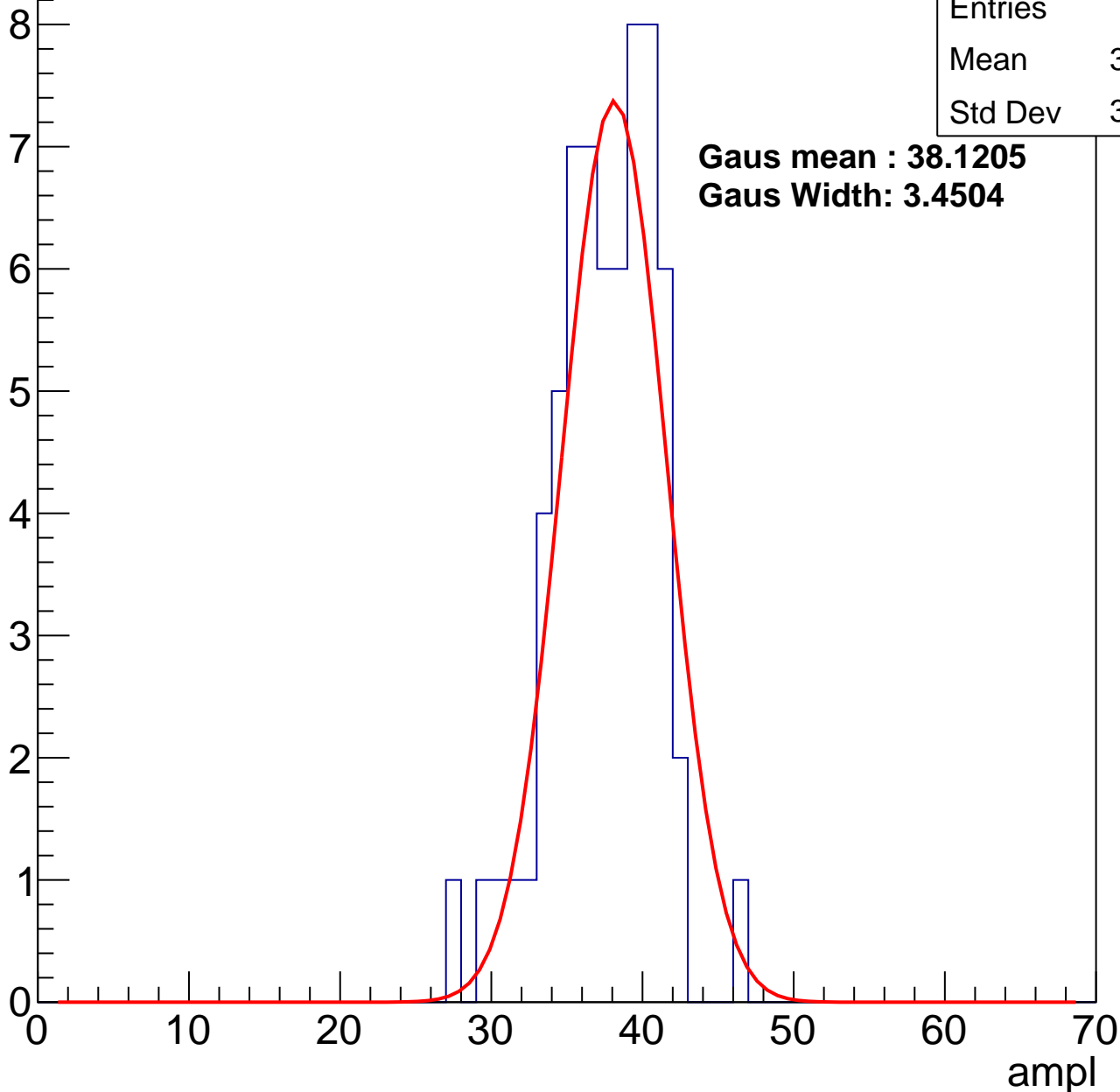
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	37.02
Std Dev	3.408

**Gaus mean : 38.1205**

**Gaus Width: 3.4504**



# B0L001S, U24-ch127, adc2

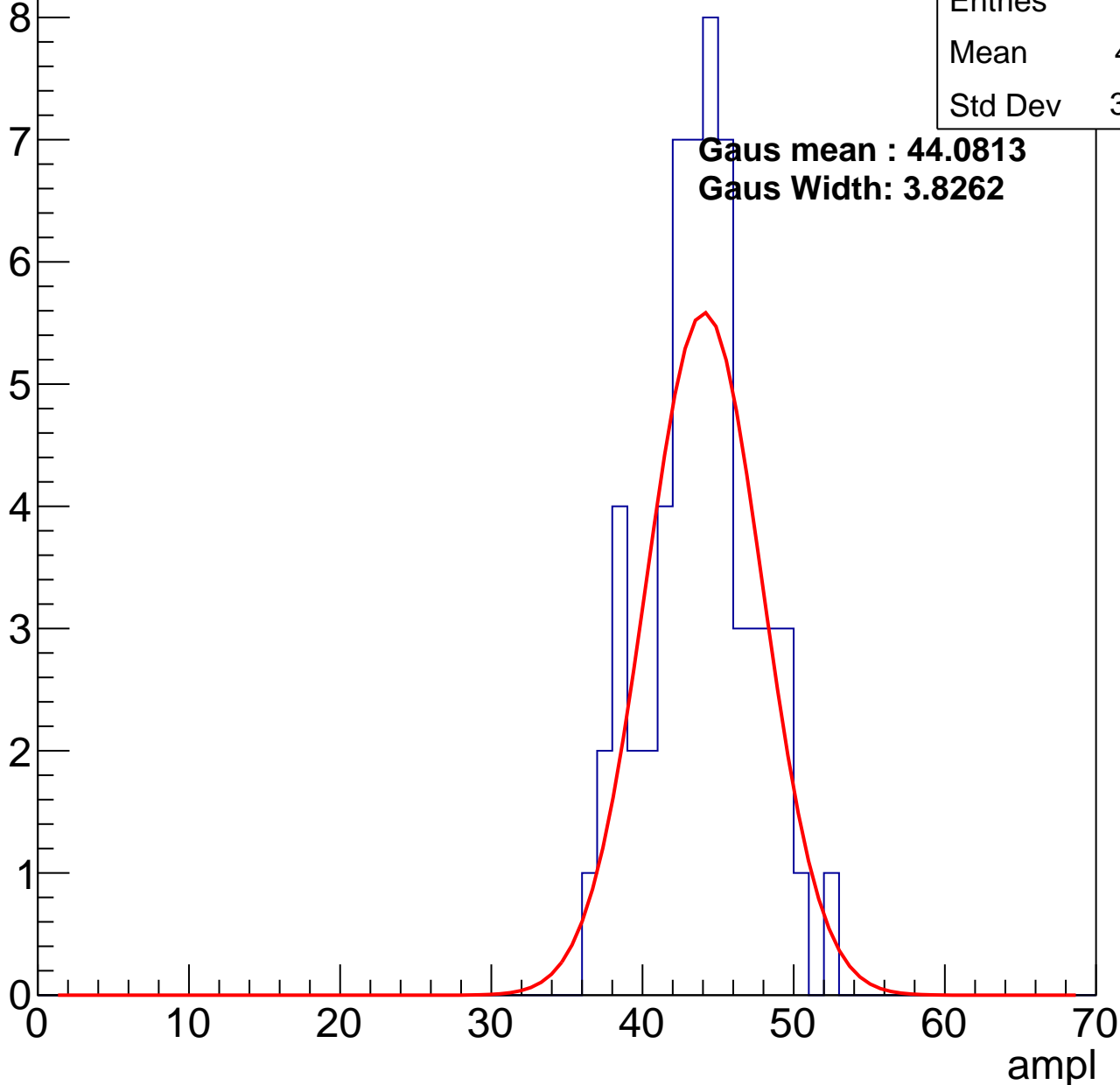
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	43.41
Std Dev	3.494

**Gaus mean : 44.0813**

**Gaus Width: 3.8262**

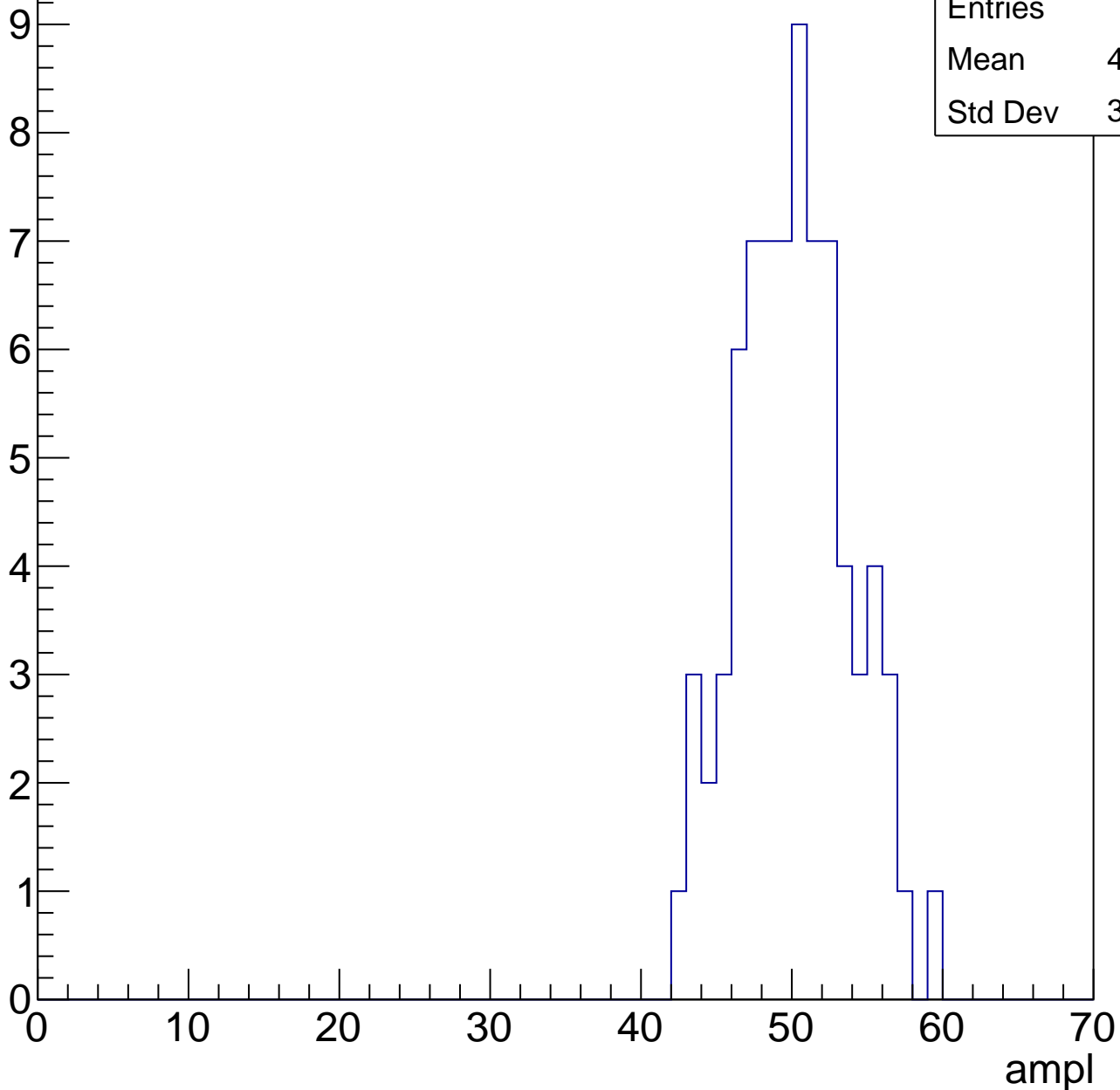


# B0L001S, U24-ch127, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	75
Mean	49.69
Std Dev	3.655

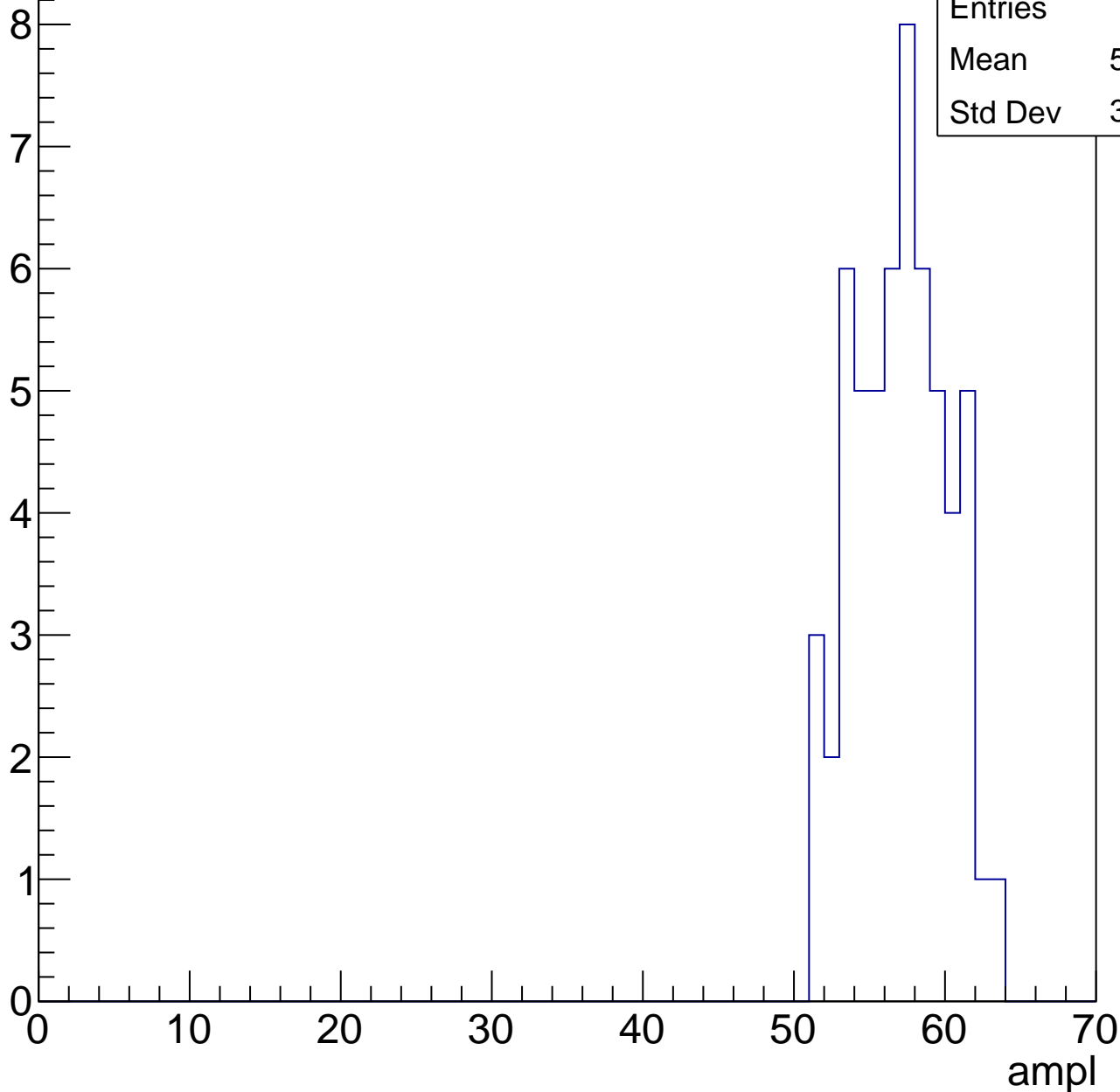


# B0L001S, U24-ch127, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	56.58
Std Dev	3.014

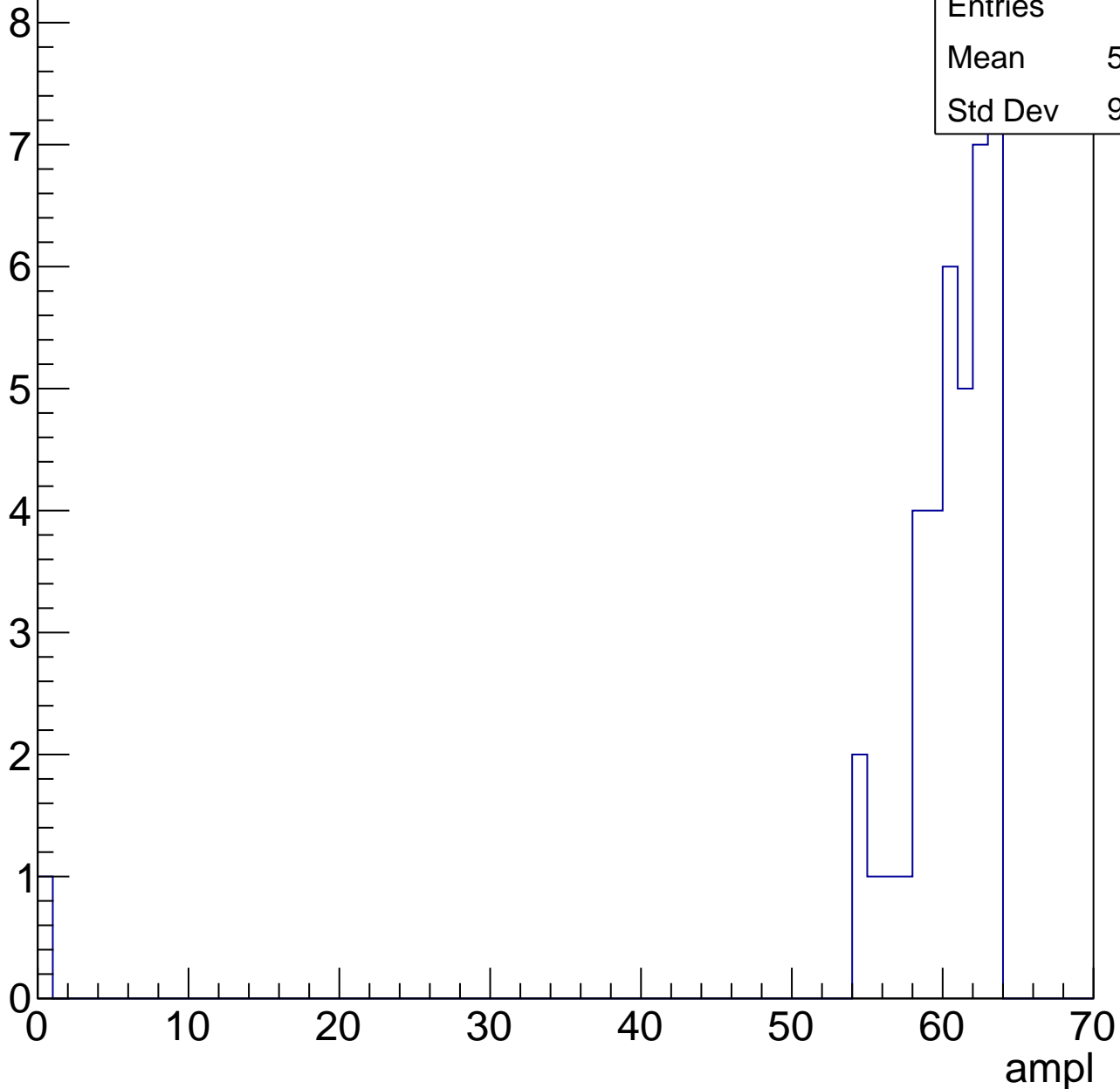


# B0L001S, U24-ch127, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	40
Mean	58.67
Std Dev	9.717



# B0L001S, U24-ch127, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U24-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U24-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

