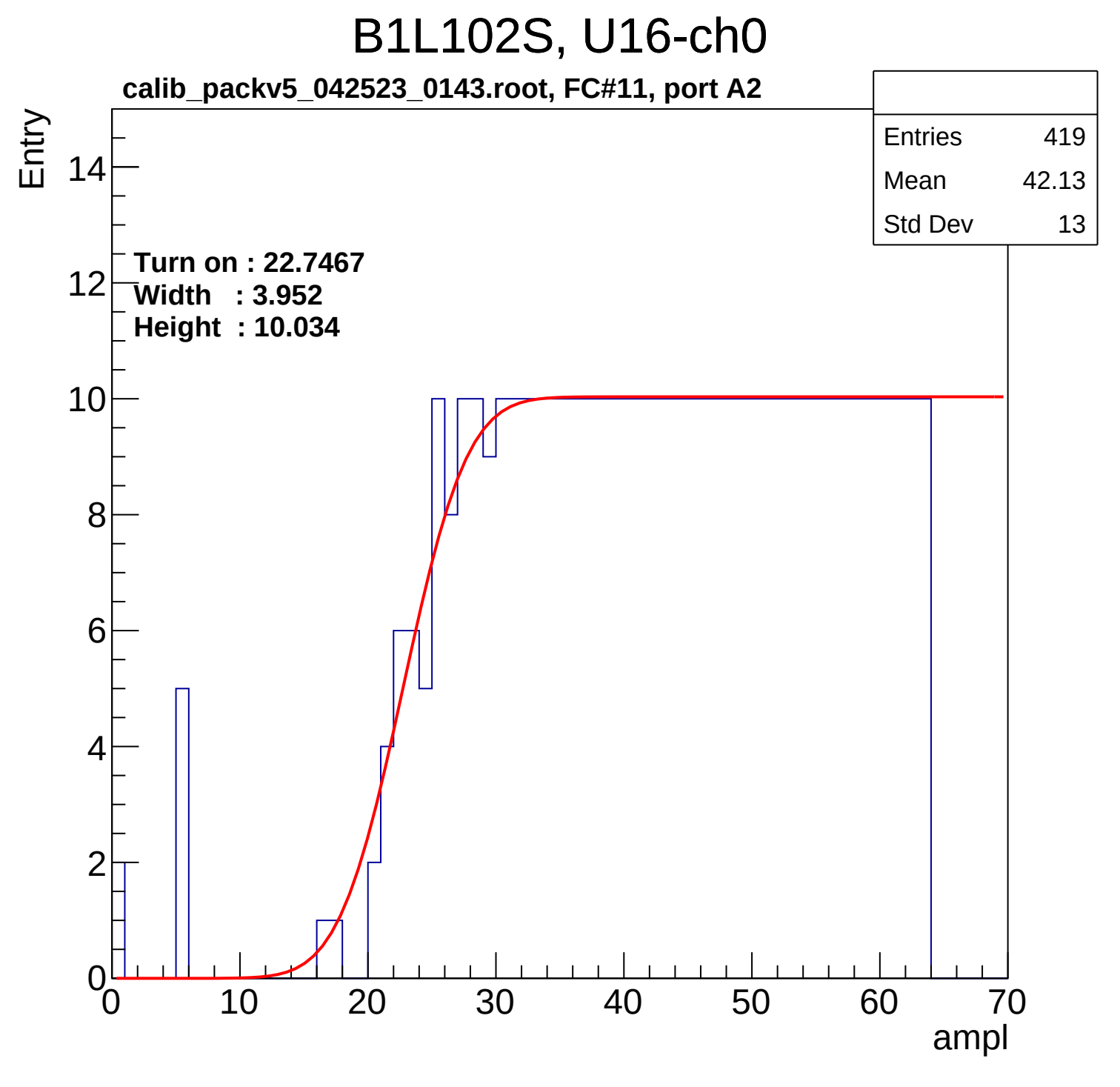
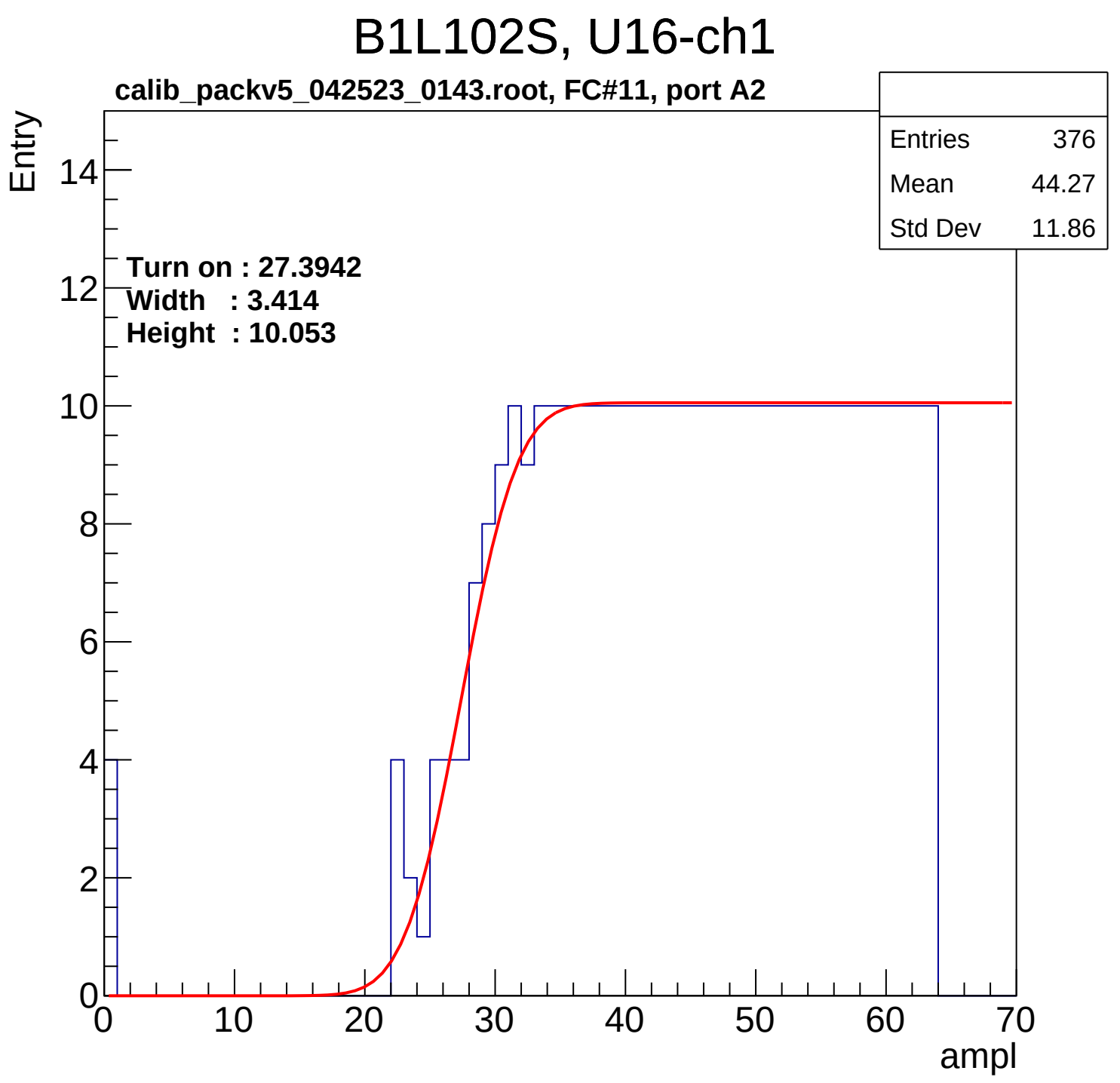
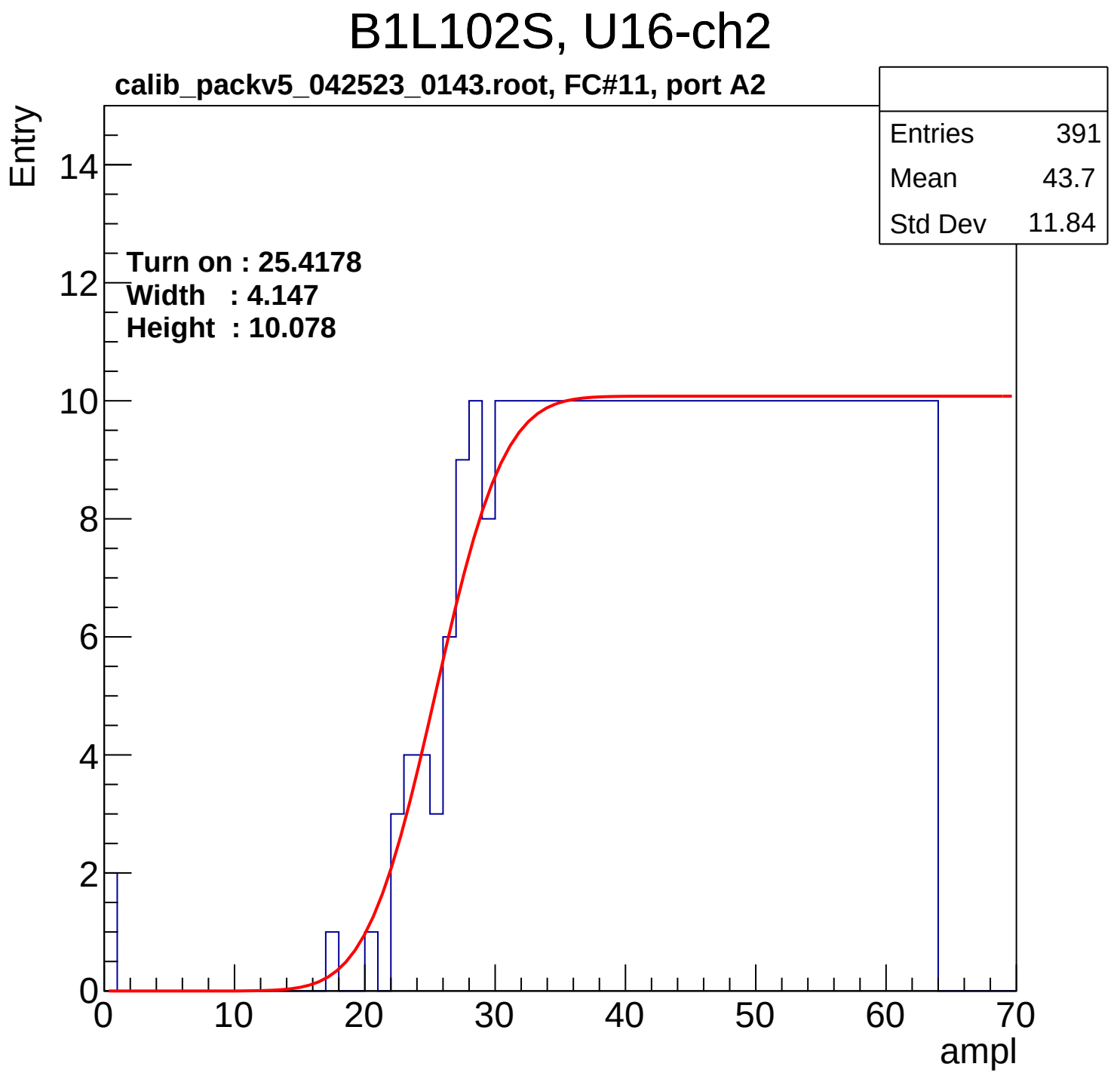
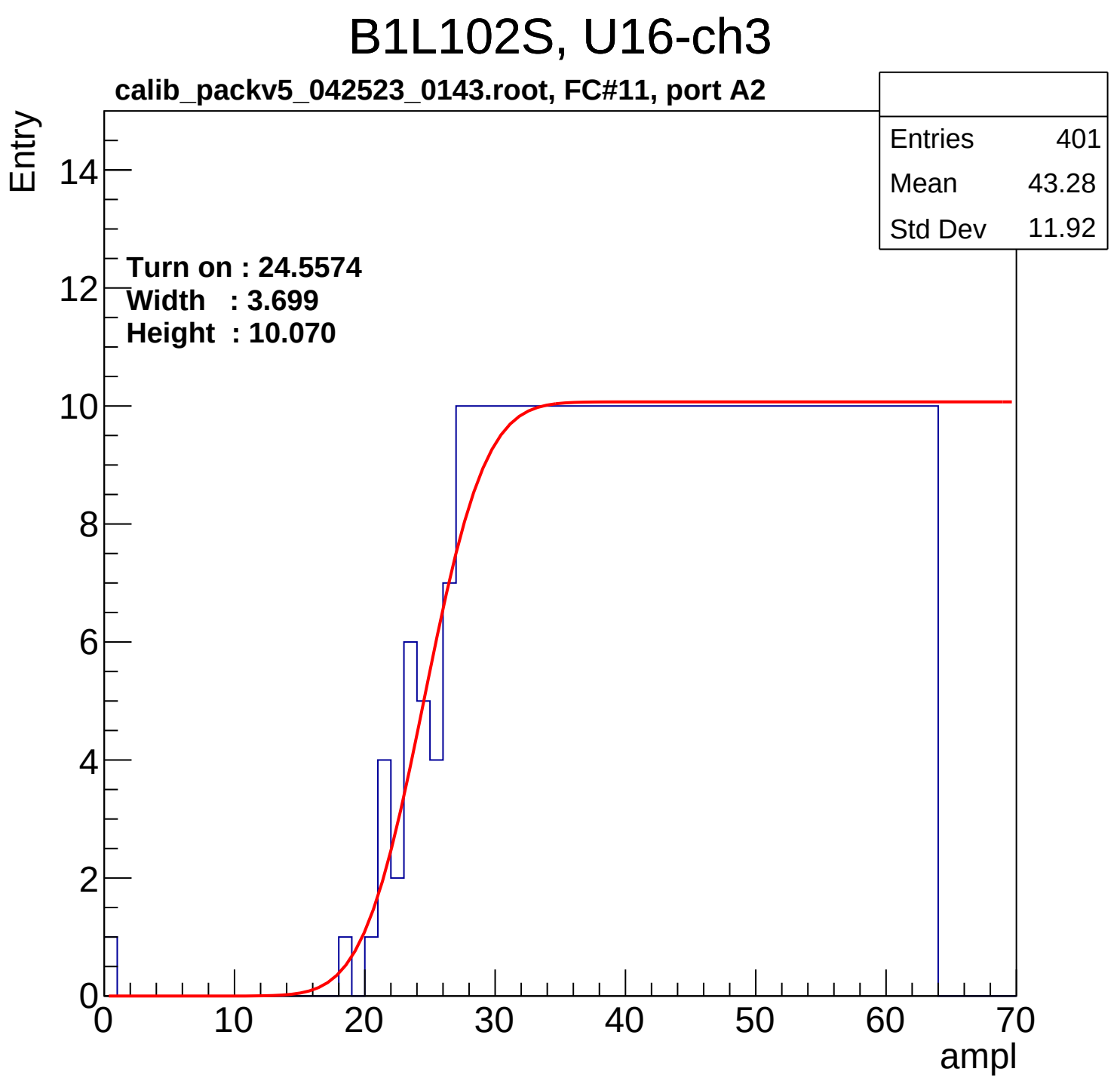
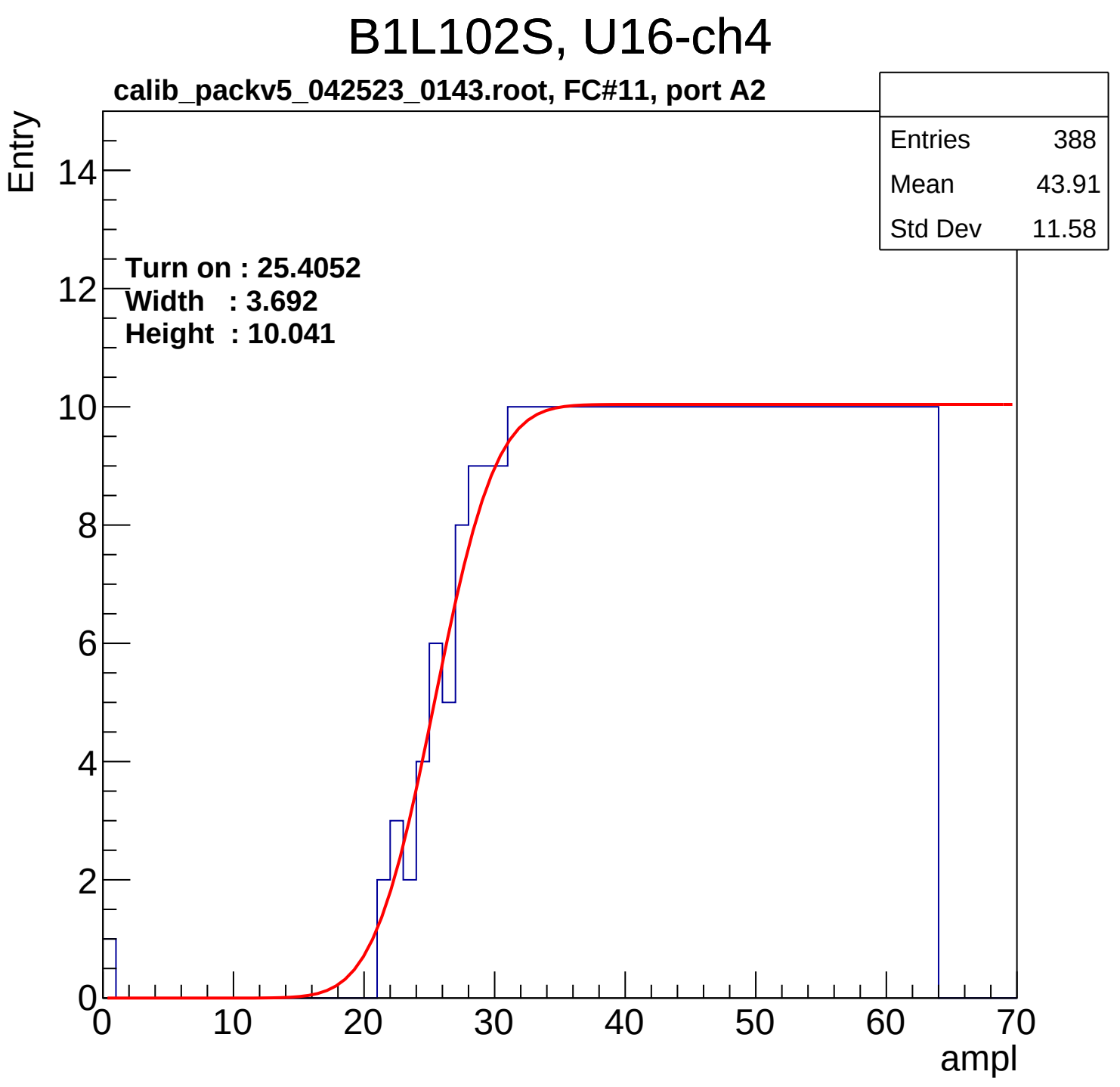
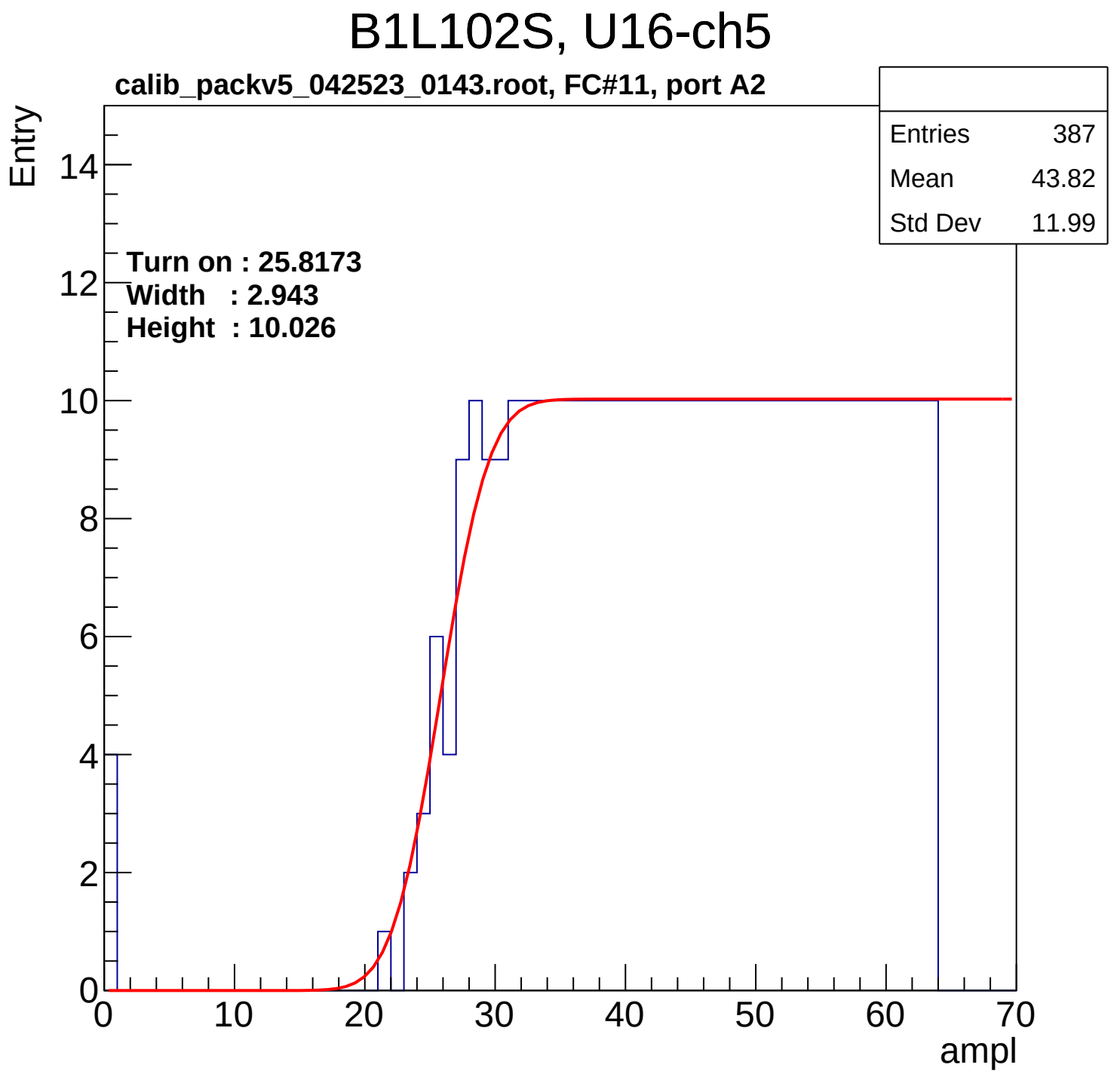

B1L102S, U16-ch0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 419
Mean 42.13
Std Dev 13
Turn on : 22.7467
Width : 3.952
Height : 10.034
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

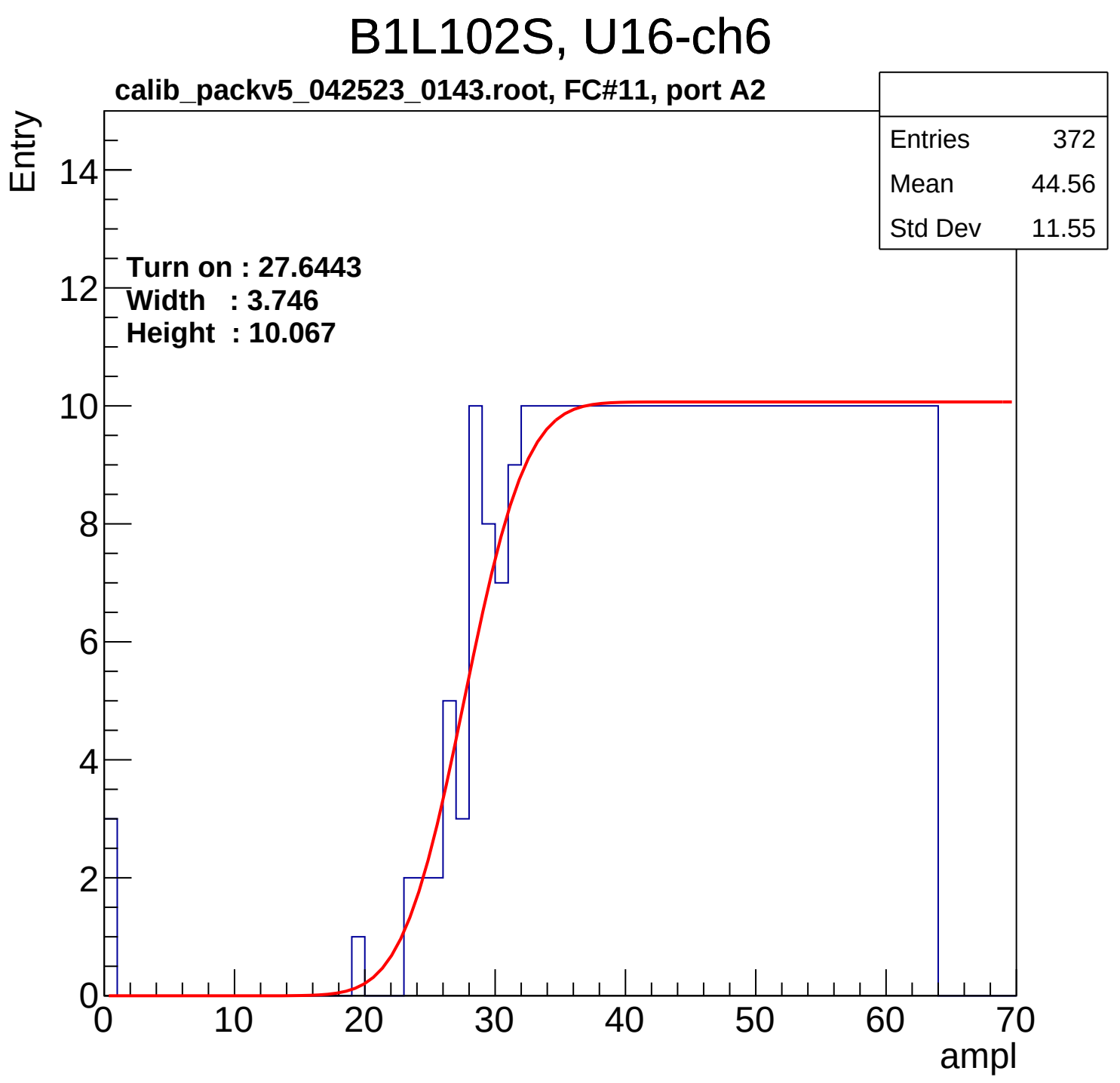

B1L102S, U16-ch1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 376
Mean 44.27
Std Dev 11.86
Turn on : 27.3942
Width : 3.414
Height : 10.053
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

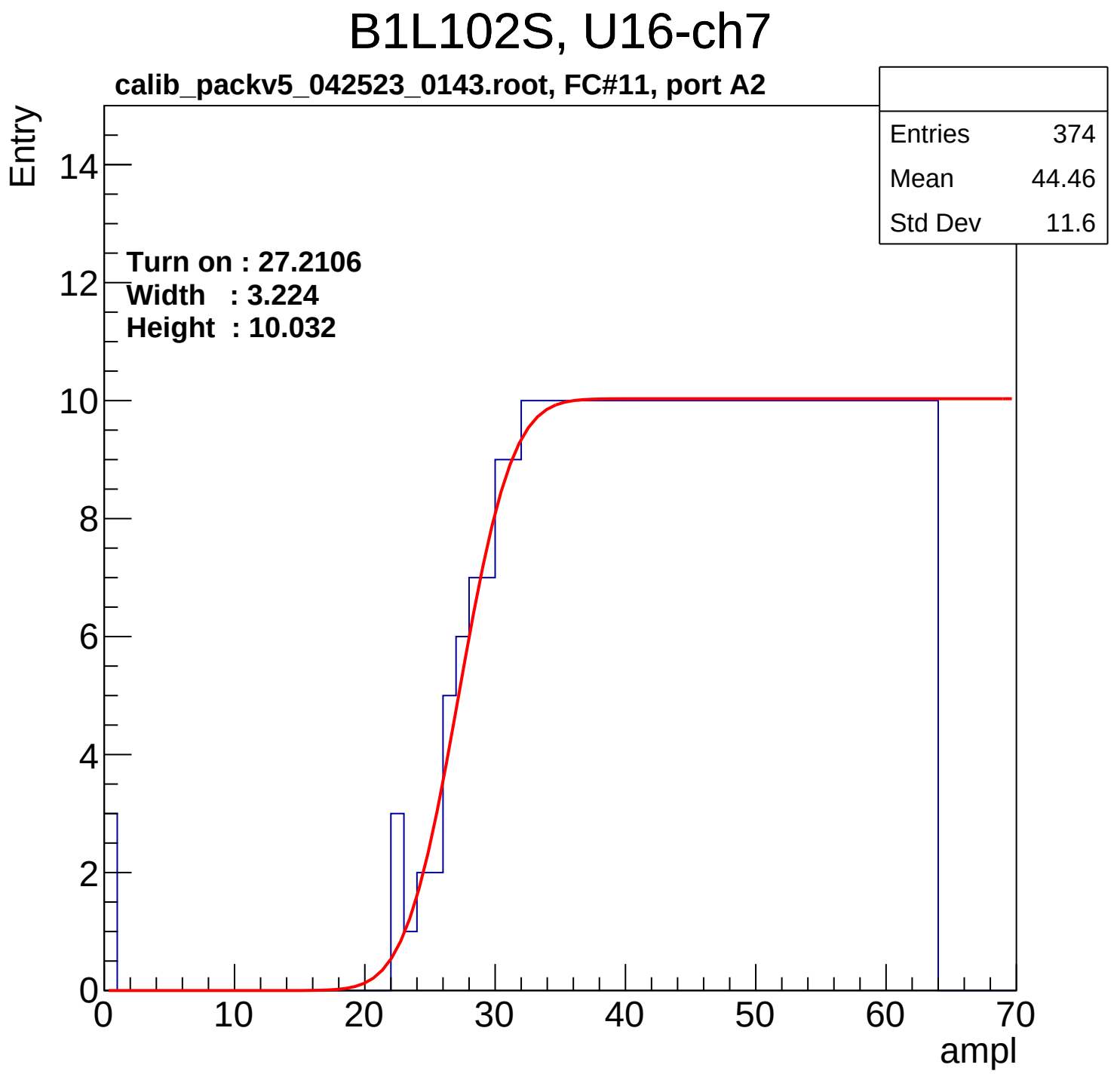

B1L102S, U16-ch2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 391
Mean 43.7
Std Dev 11.84
Turn on : 25.4178
Width : 4.147
Height : 10.078
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

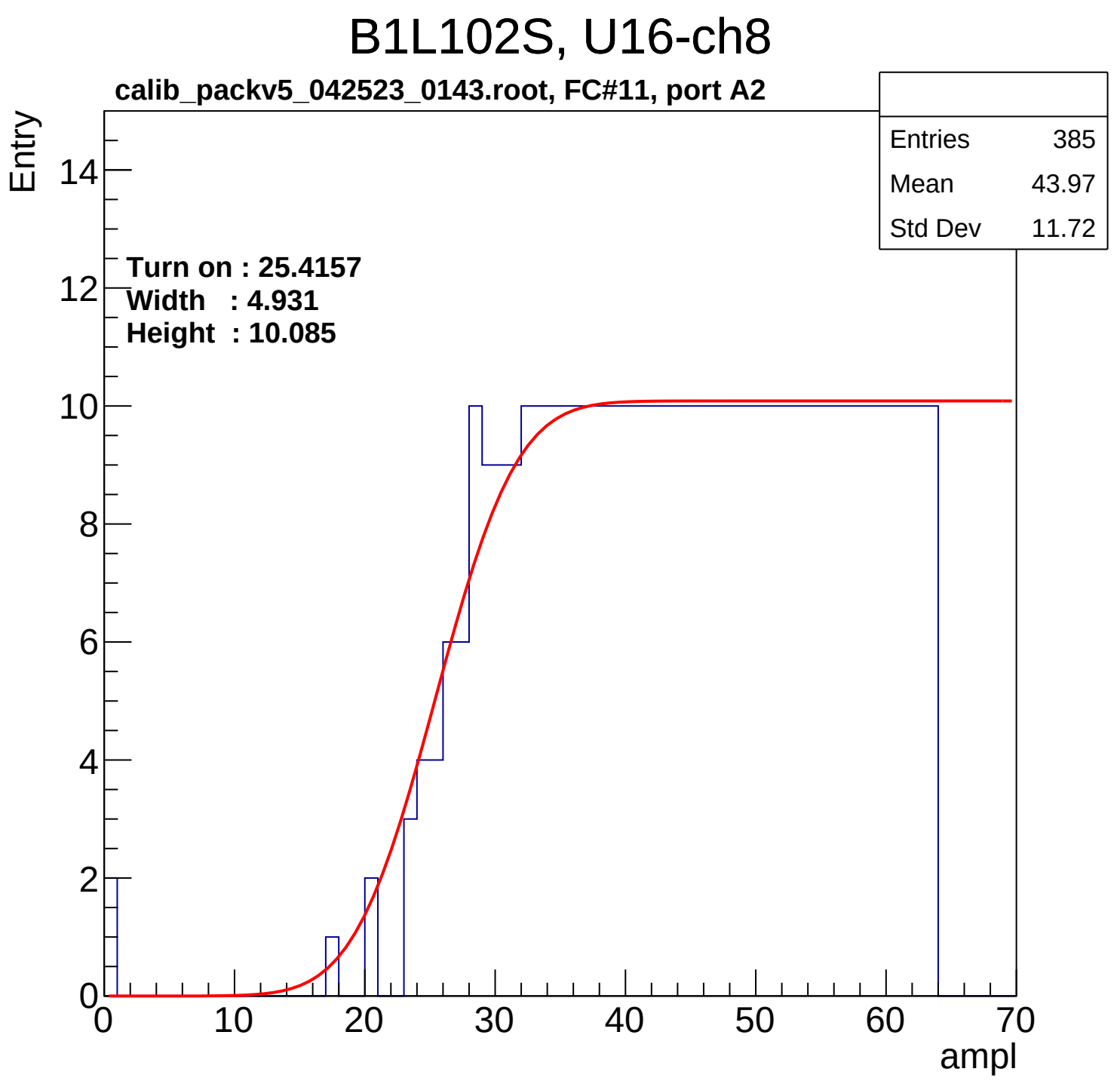

B1L102S, U16-ch3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 401
Mean 43.28
Std Dev 11.92
Turn on : 24.5574
Width : 3.699
Height : 10.070
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

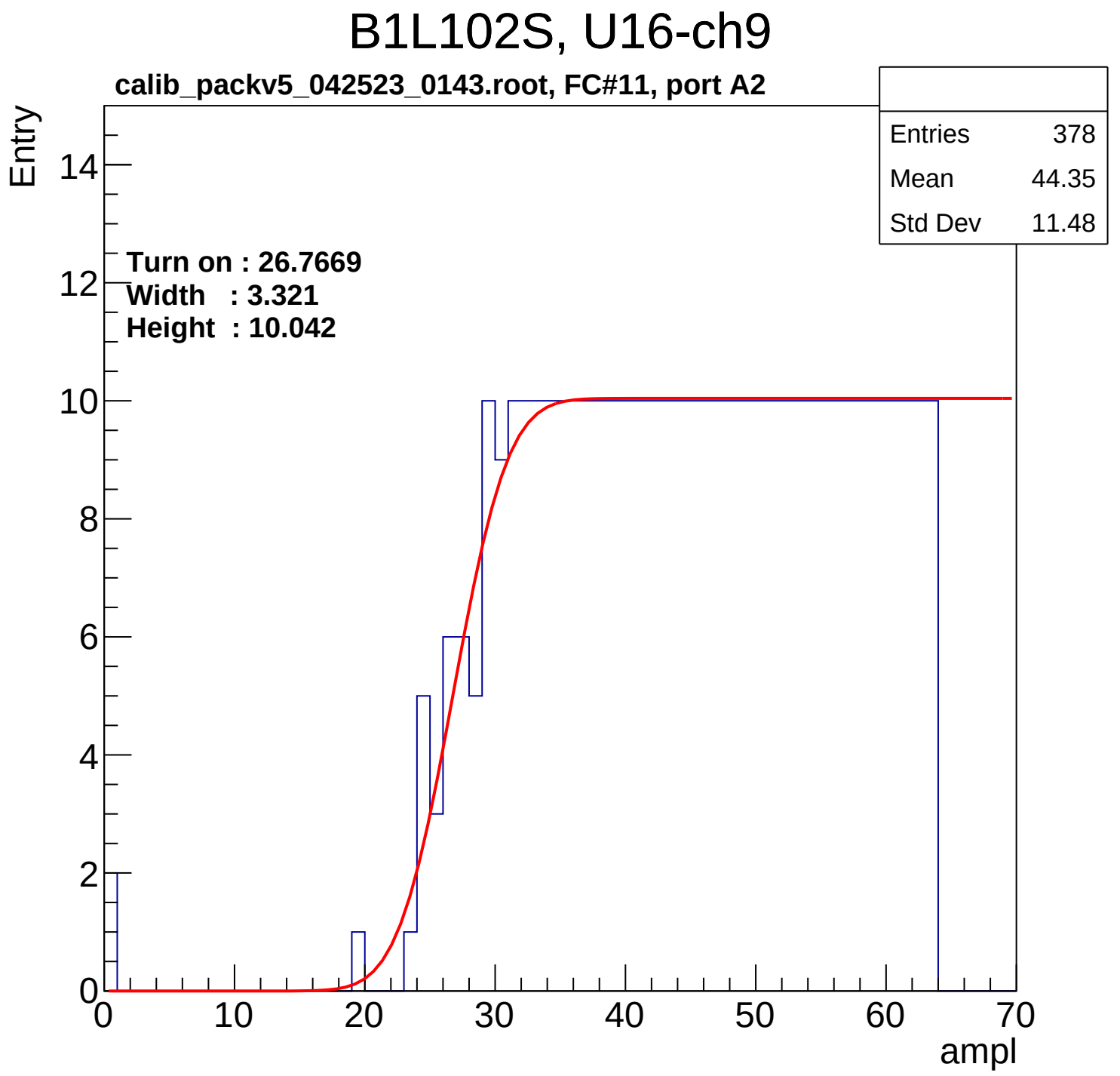

B1L102S, U16-ch4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 388
Mean 43.91
Std Dev 11.58
Turn on : 25.4052
Width : 3.692
Height : 10.041
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

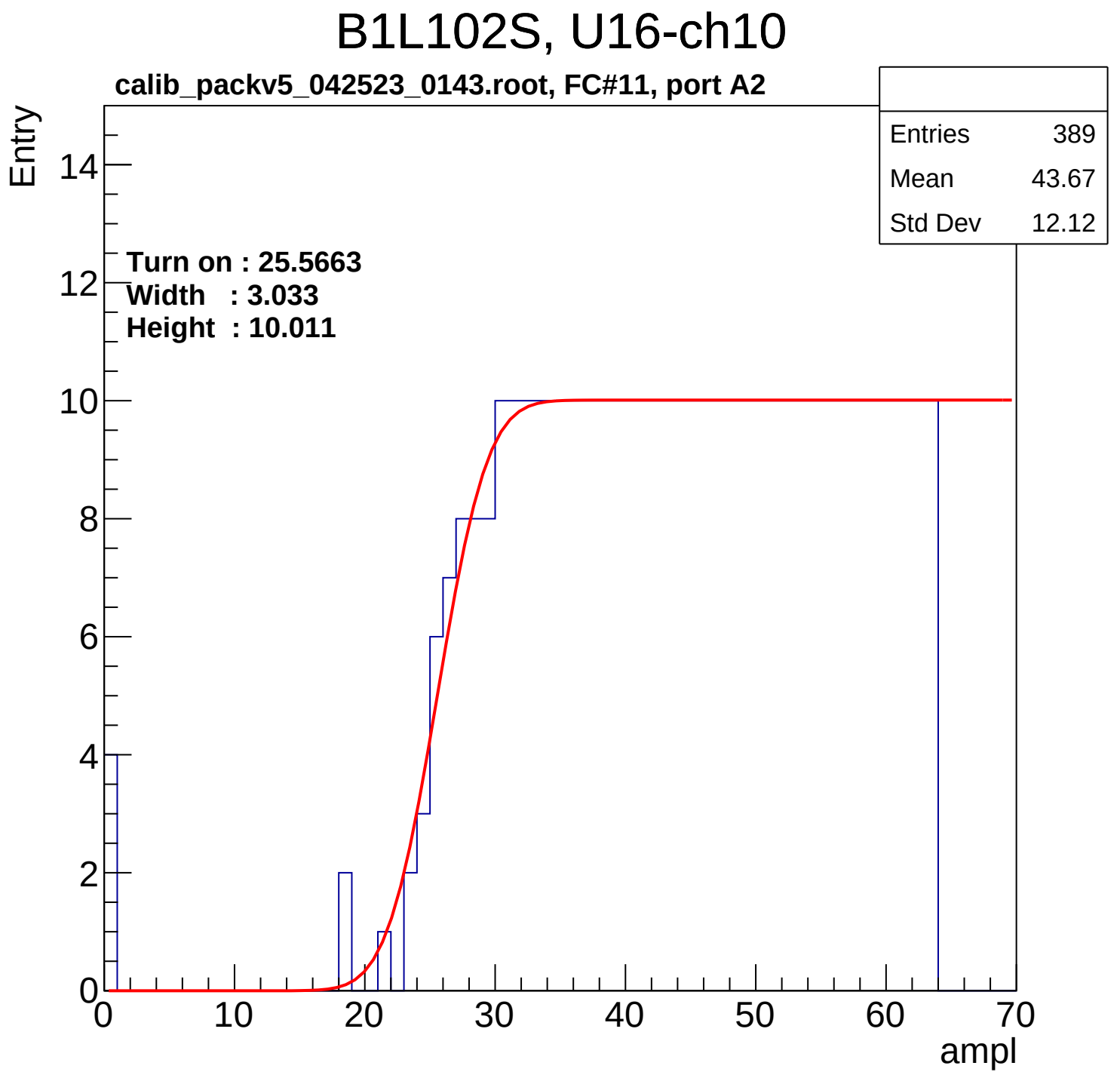

B1L102S, U16-ch5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 43.82
Std Dev 11.99
Turn on : 25.8173
Width : 2.943
Height : 10.026
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

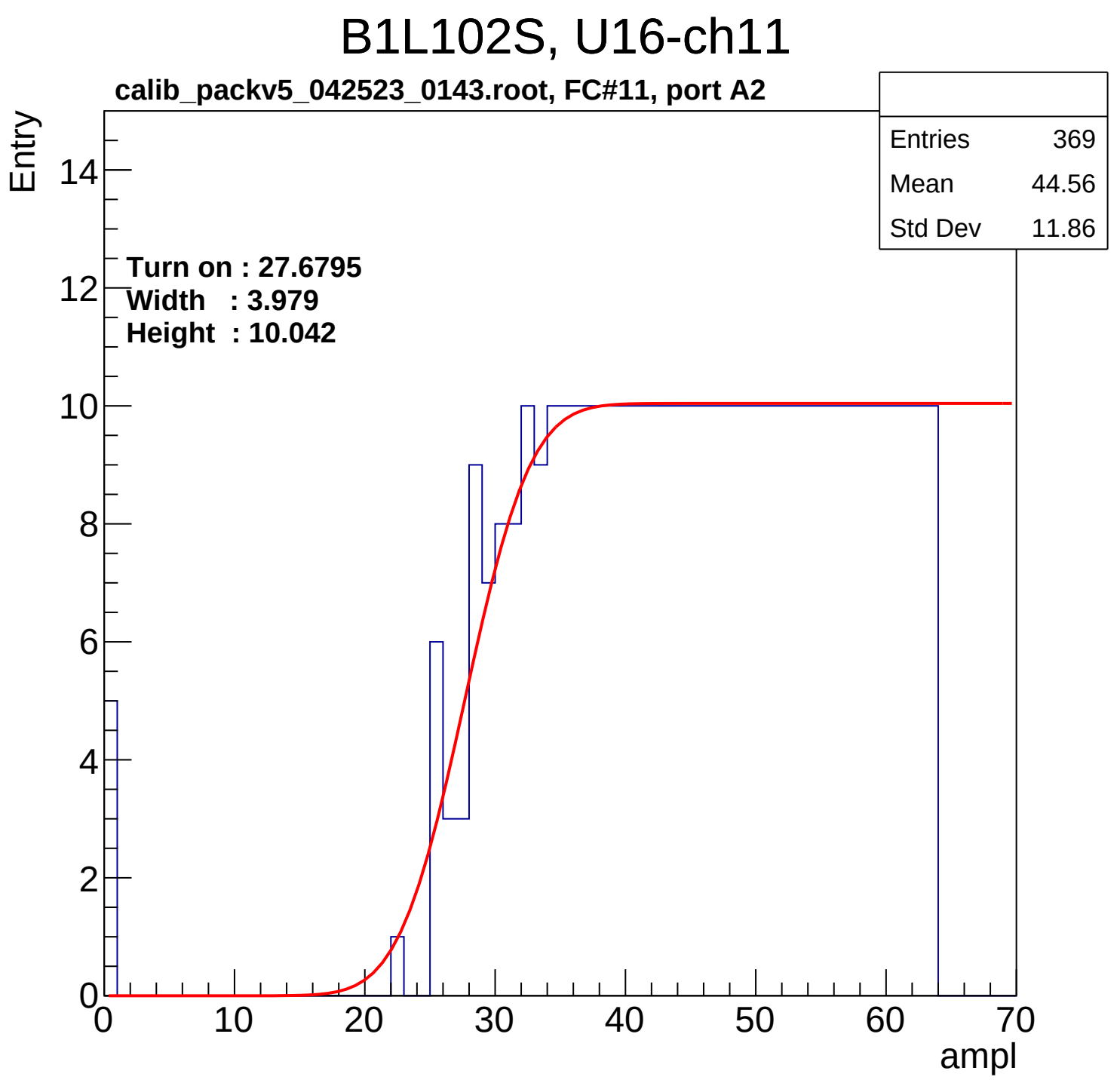

B1L102S, U16-ch6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 372
Mean 44.56
Std Dev 11.55
Turn on : 27.6443
Width : 3.746
Height : 10.067
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

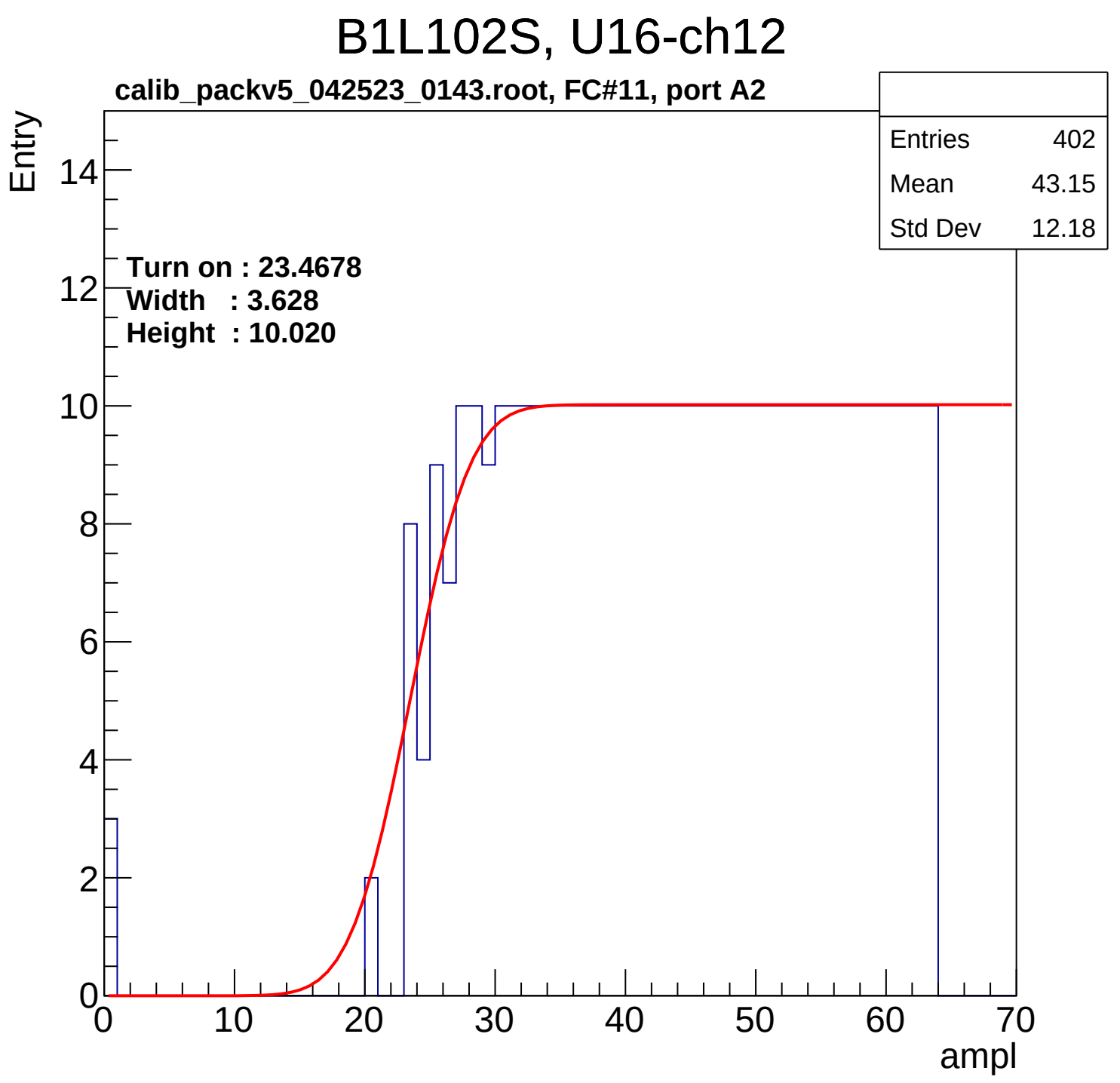

B1L102S, U16-ch7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 374
Mean 44.46
Std Dev 11.6
Turn on : 27.2106
Width : 3.224
Height : 10.032
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

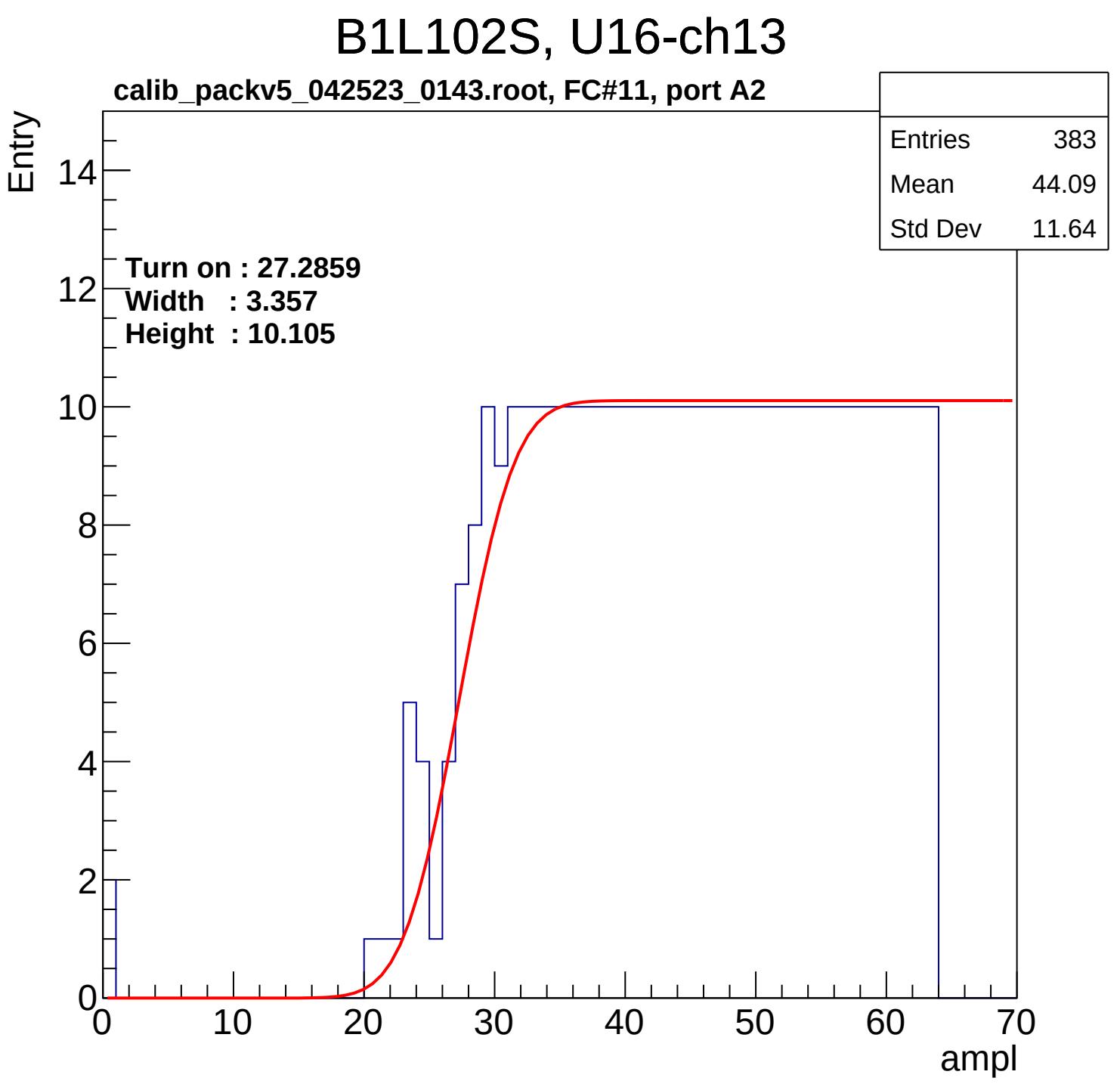

B1L102S, U16-ch8
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 43.97
Std Dev 11.72
Turn on : 25.4157
Width : 4.931
Height : 10.085
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

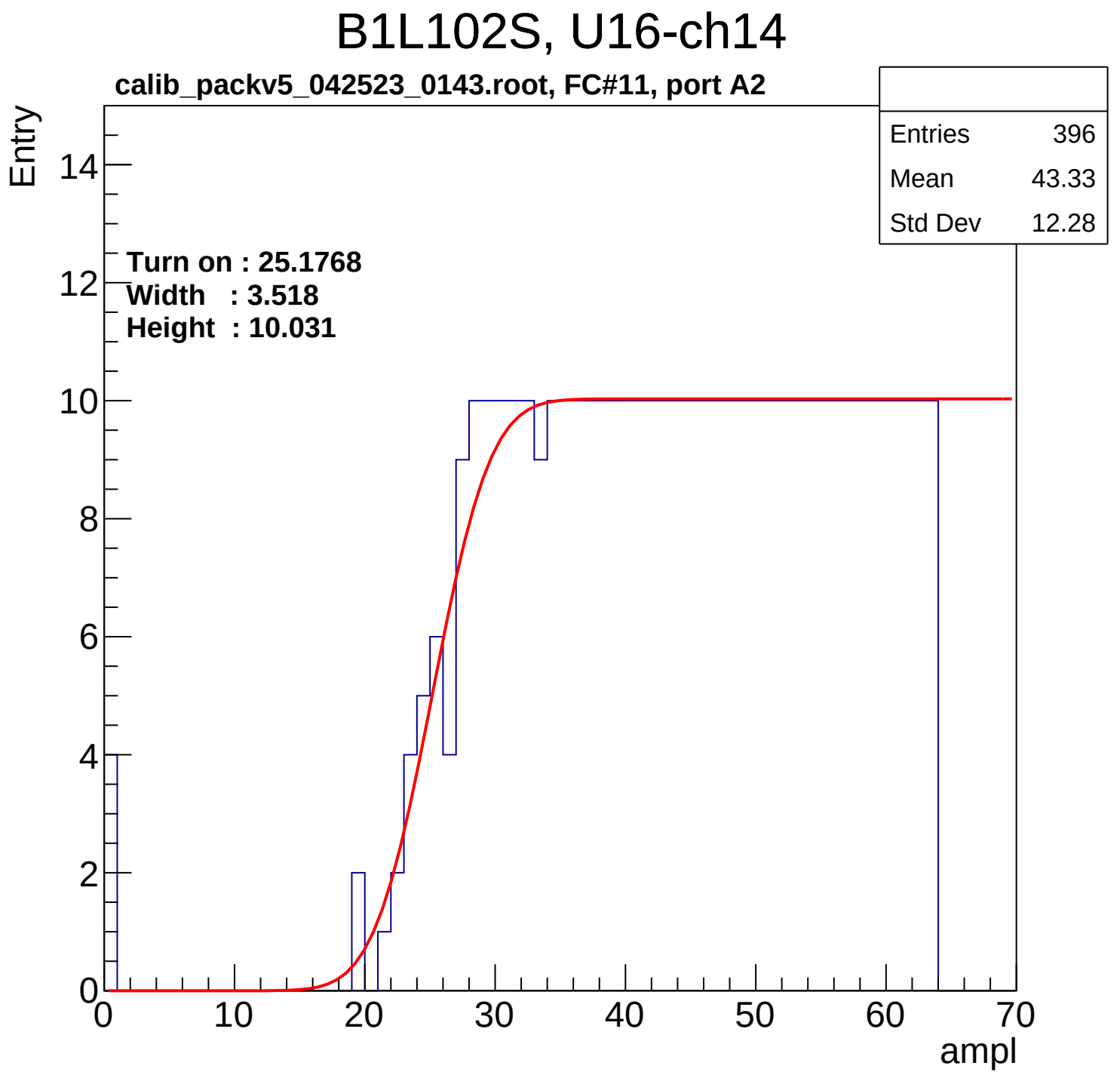

B1L102S, U16-ch9
calib_packv5_042523_0143.root, FC#11, port A2
Entries 378
Mean 44.35
Std Dev 11.48
Turn on : 26.7669
Width : 3.321
Height : 10.042
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

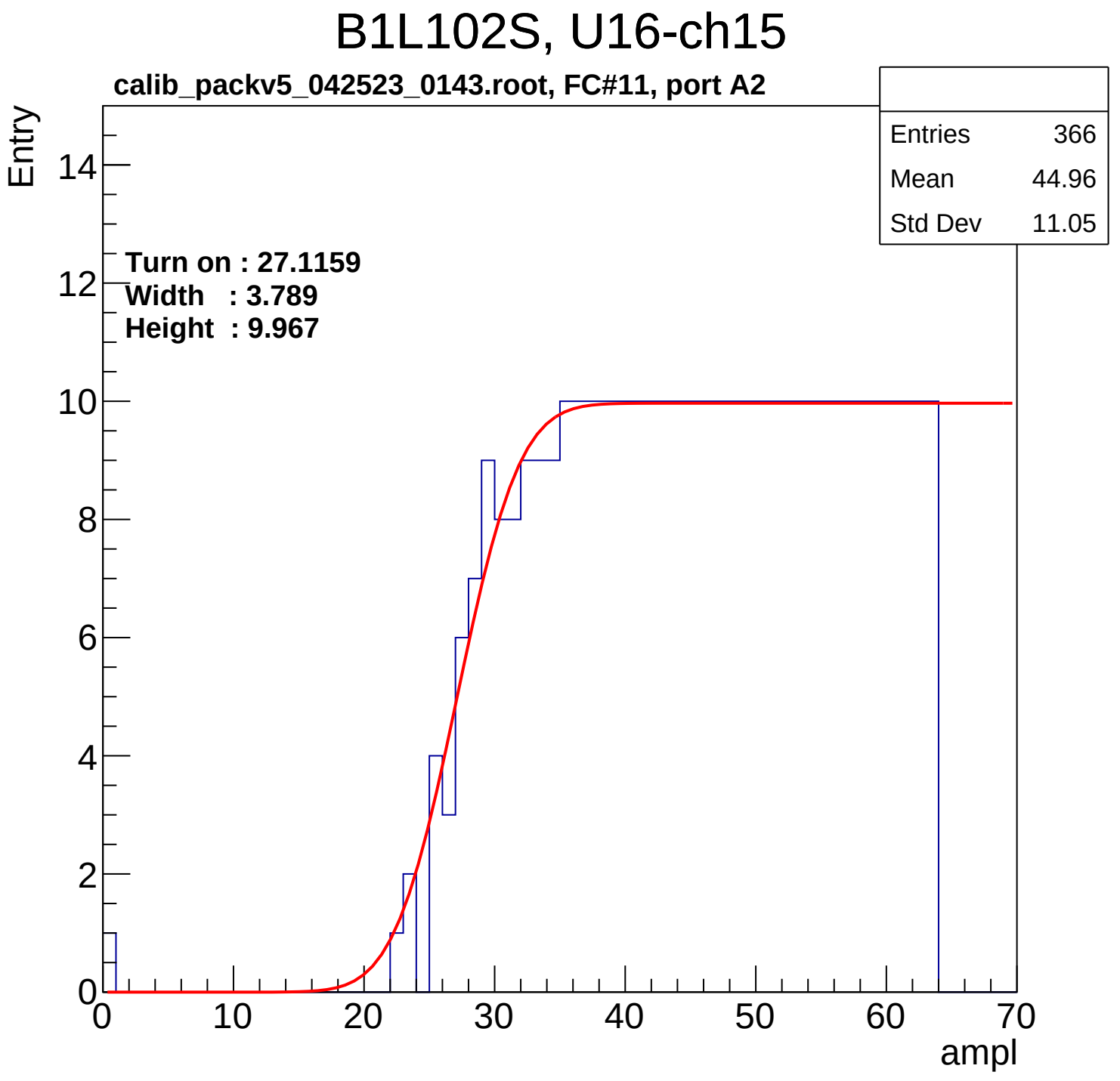

B1L102S, U16-ch10
calib_packv5_042523_0143.root, FC#11, port A2
Entries 389
Mean 43.67
Std Dev 12.12
Turn on : 25.5663
Width : 3.033
Height : 10.011
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

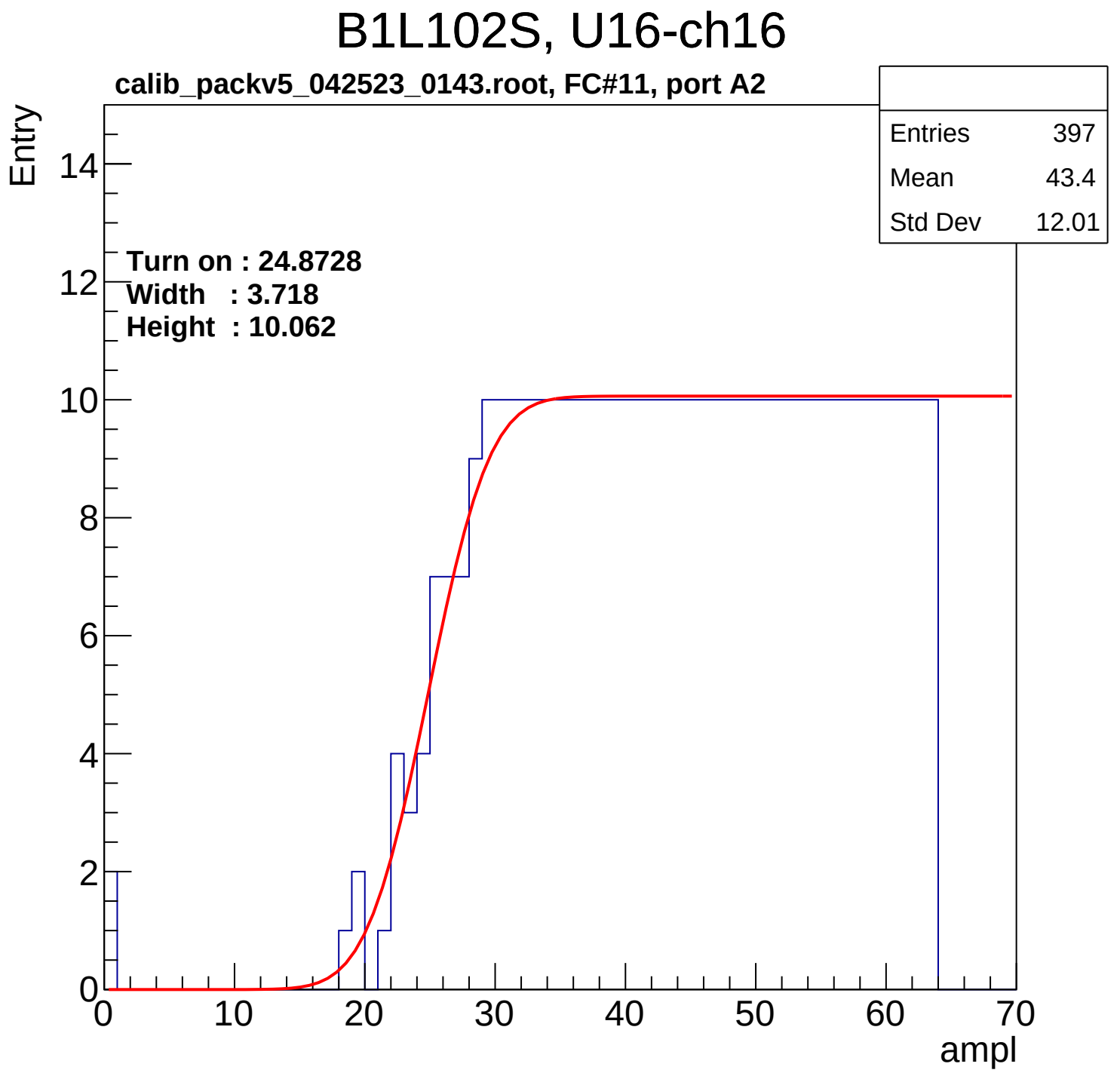

B1L102S, U16-ch11
calib_packv5_042523_0143.root, FC#11, port A2
Entries 369
Mean 44.56
Std Dev 11.86
Turn on : 27.6795
Width : 3.979
Height : 10.042
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

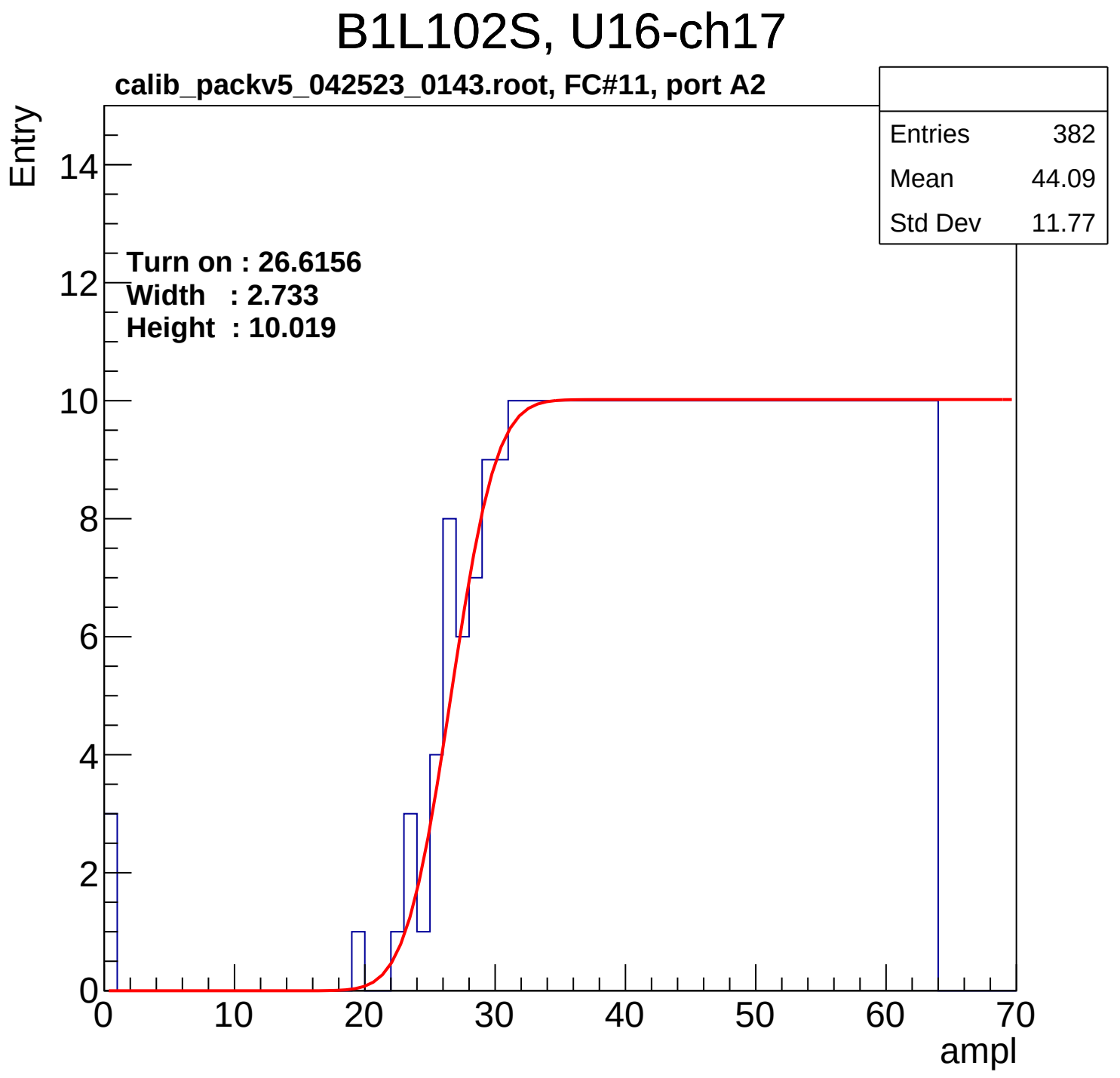

B1L102S, U16-ch12
calib_packv5_042523_0143.root, FC#11, port A2
Entries 402
Mean 43.15
Std Dev 12.18
Turn on : 23.4678
Width : 3.628
Height : 10.020
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

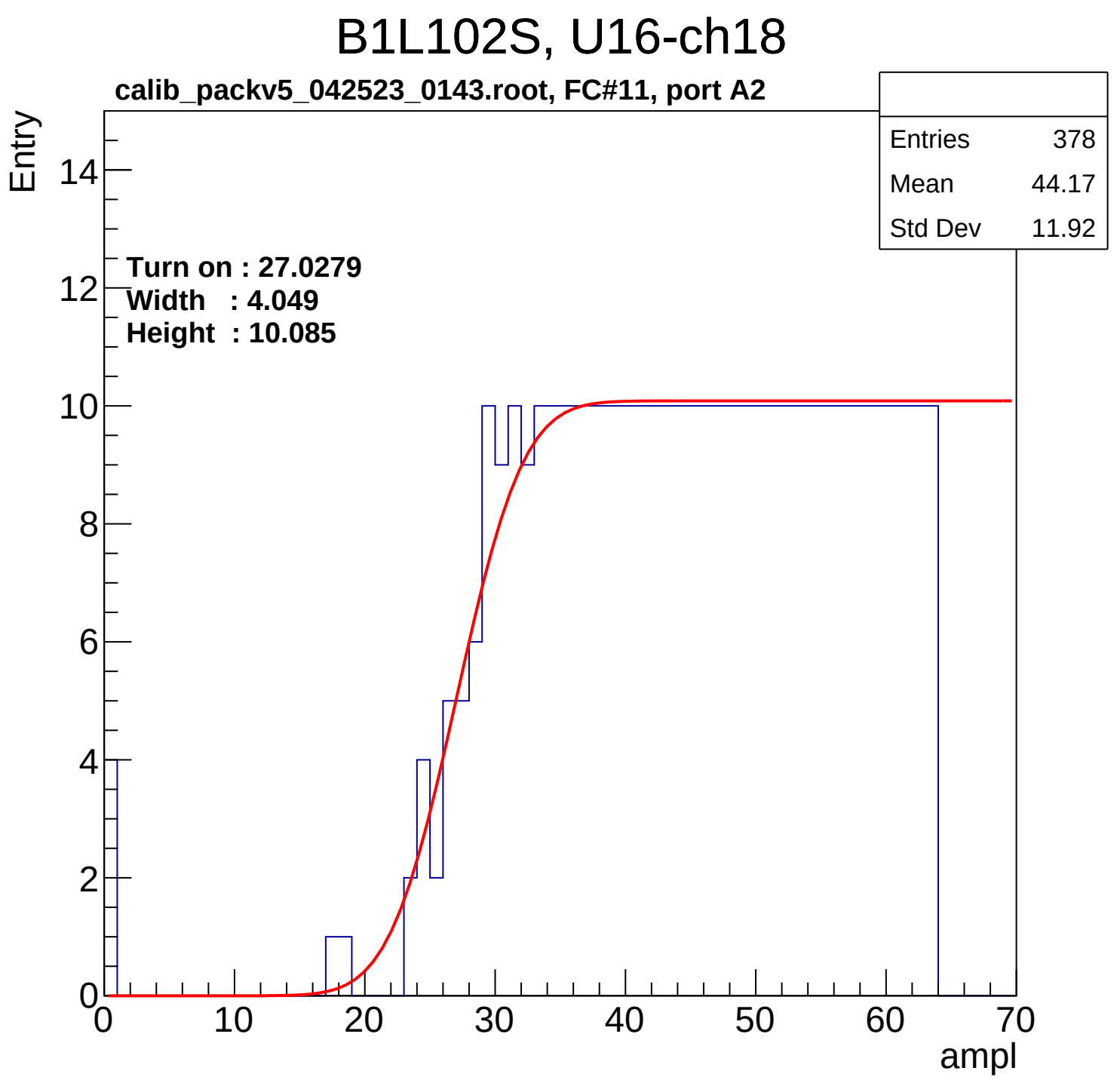

B1L102S, U16-ch13
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 44.09
Std Dev 11.64
Turn on : 27.2859
Width : 3.357
Height : 10.105
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

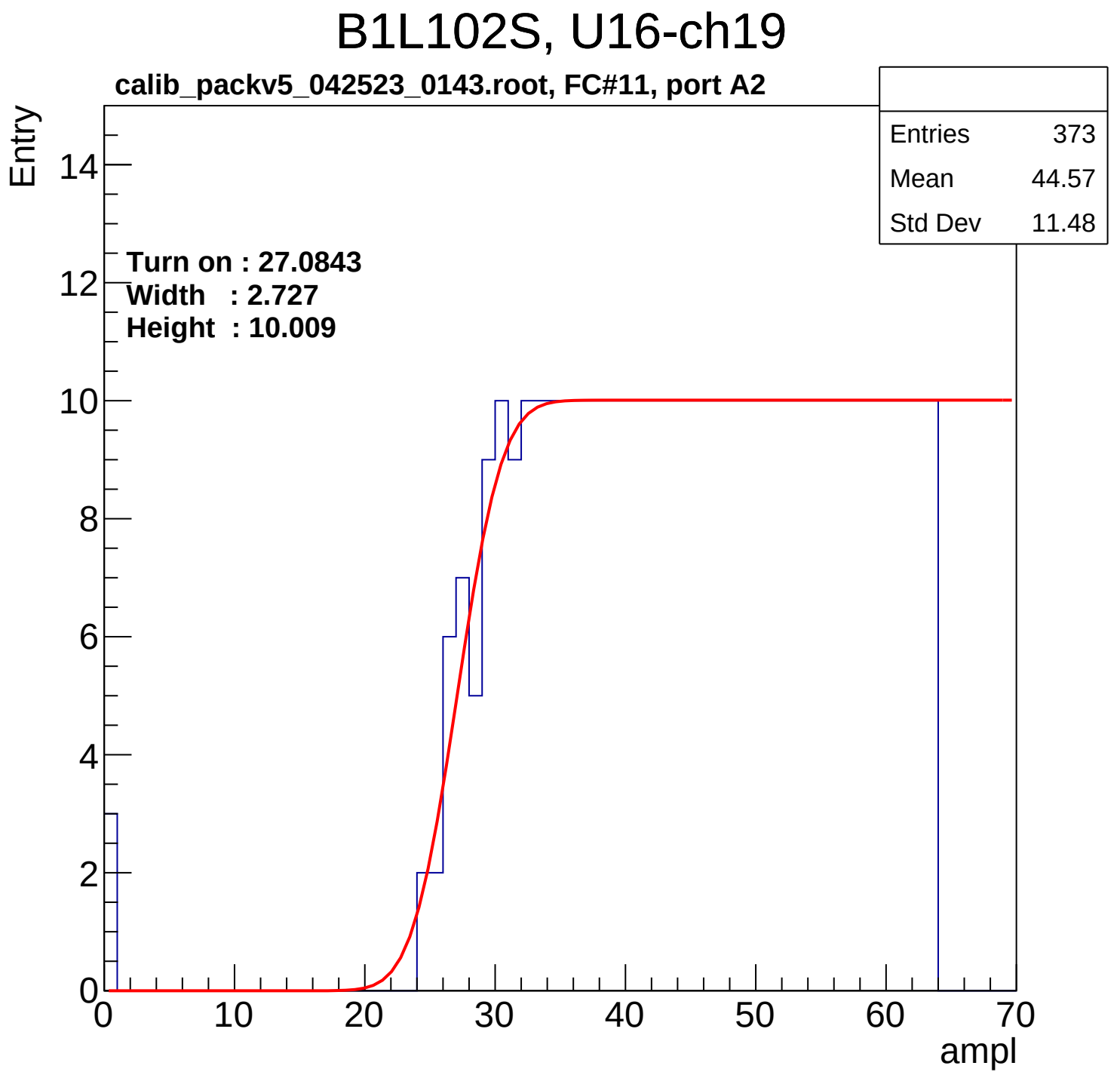

B1L102S, U16-ch14
calib_packv5_042523_0143.root, FC#11, port A2
Entries 396
Mean 43.33
Std Dev 12.28
Turn on : 25.1768
Width : 3.518
Height : 10.031
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

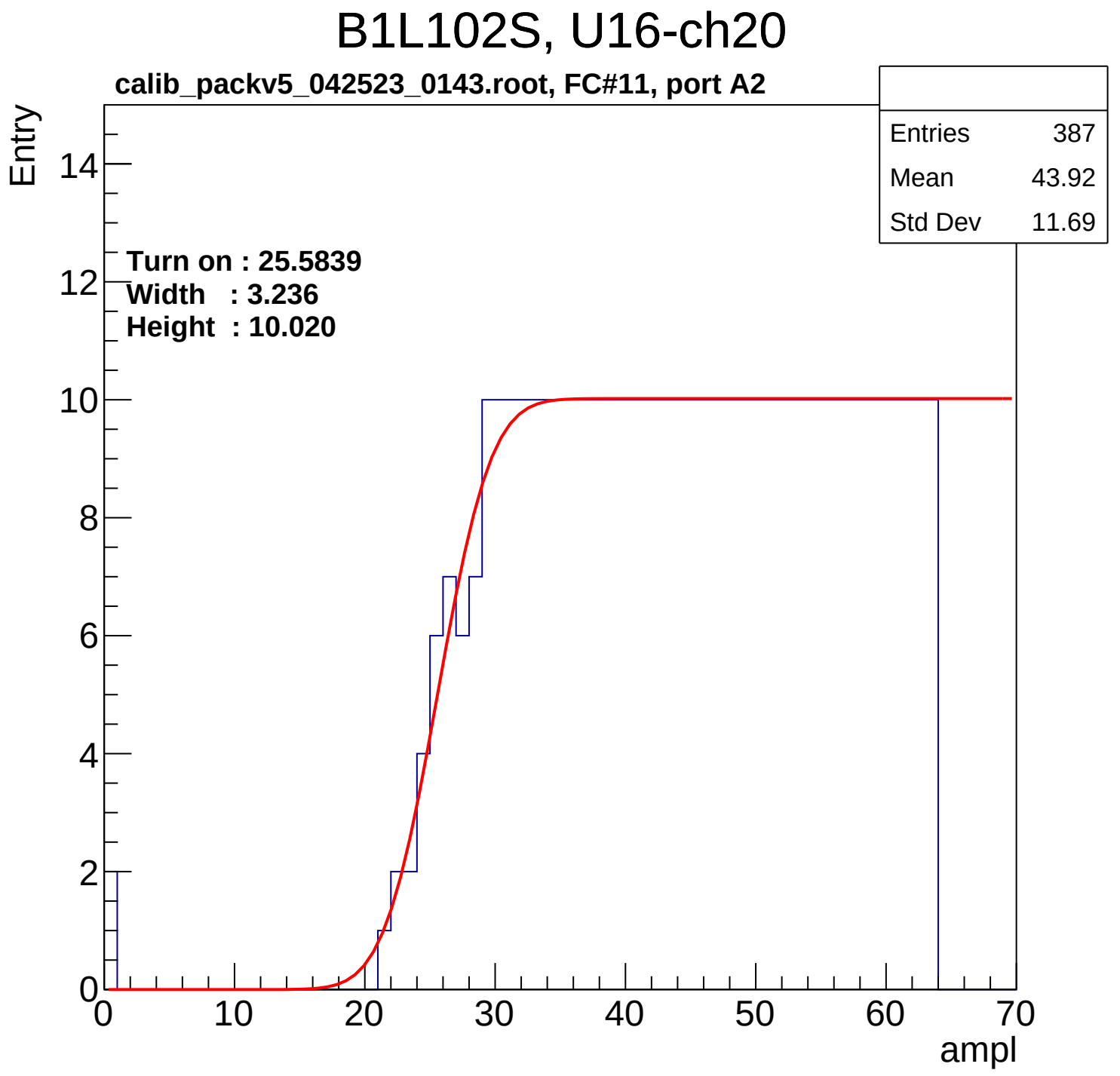

B1L102S, U16-ch15
calib_packv5_042523_0143.root, FC#11, port A2
Entries 366
Mean 44.96
Std Dev 11.05
Turn on : 27.1159
Width : 3.789
Height : 9.967
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

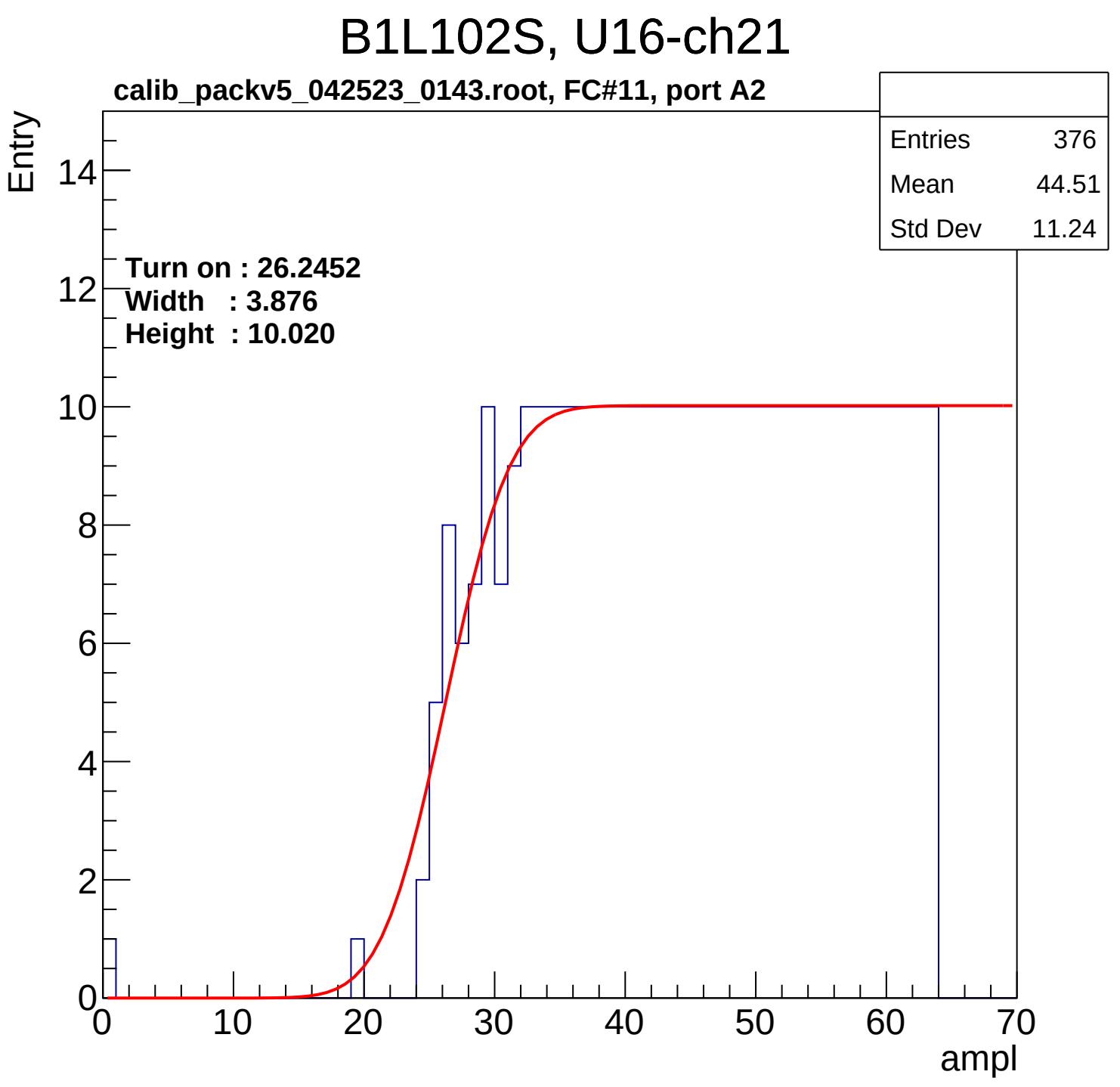

B1L102S, U16-ch16
calib_packv5_042523_0143.root, FC#11, port A2
Entries 397
Mean 43.4
Std Dev 12.01
Turn on : 24.8728
Width : 3.718
Height : 10.062
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

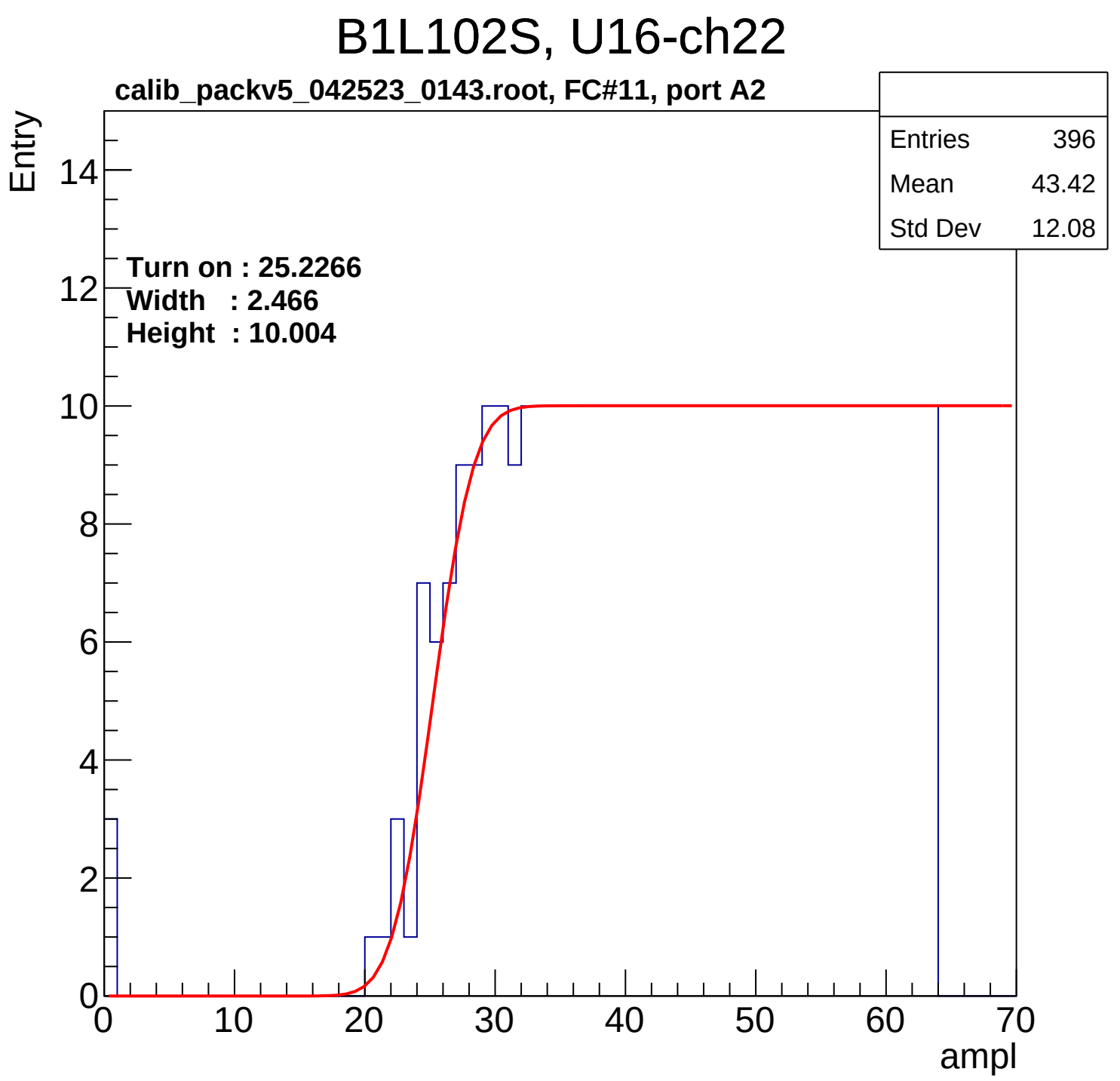

B1L102S, U16-ch17
calib_packv5_042523_0143.root, FC#11, port A2
Entries 382
Mean 44.09
Std Dev 11.77
Turn on : 26.6156
Width : 2.733
Height : 10.019
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

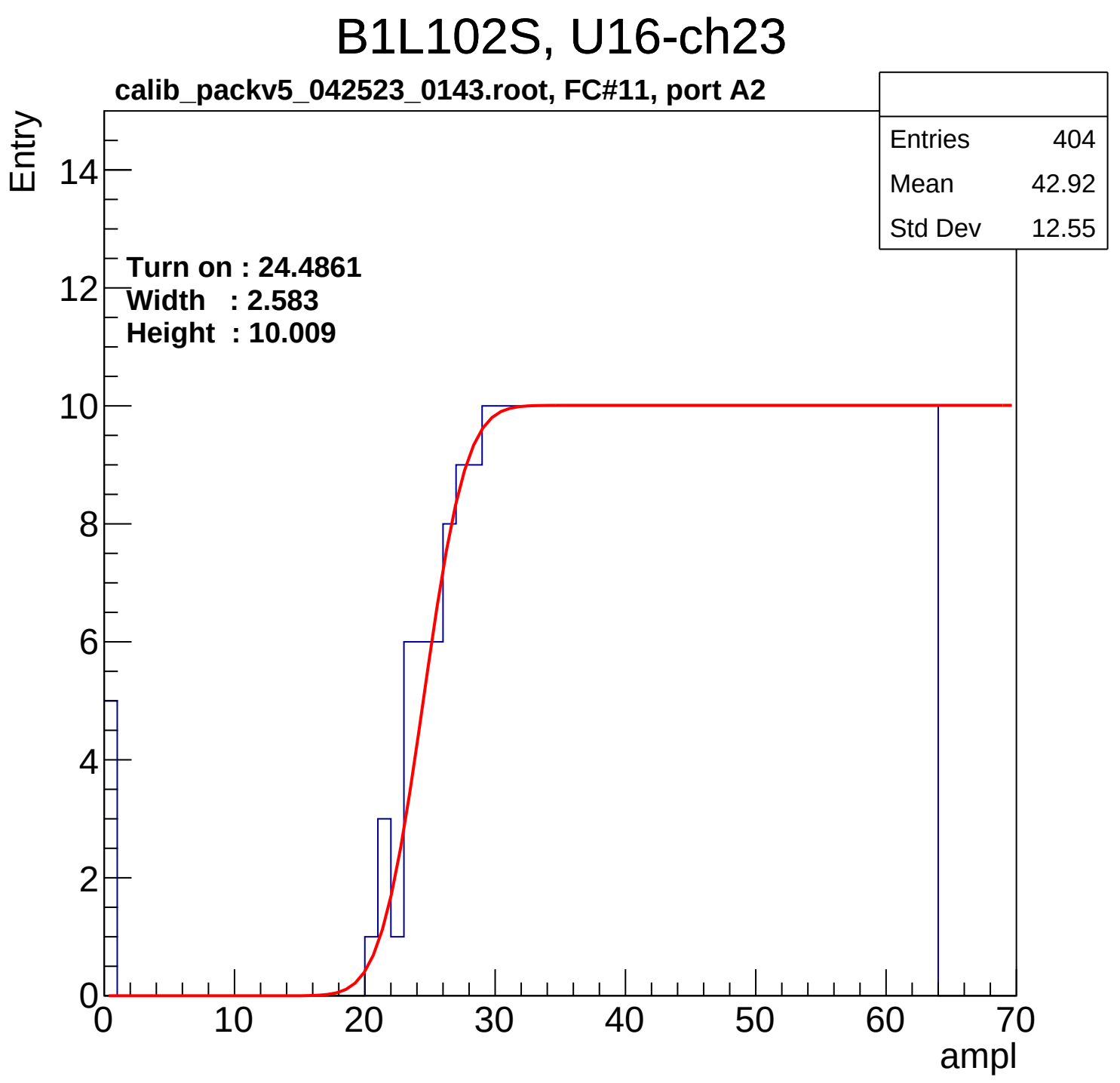

B1L102S, U16-ch18
calib_packv5_042523_0143.root, FC#11, port A2
Entries 378
Mean 44.17
Std Dev 11.92
Turn on : 27.0279
Width : 4.049
Height : 10.085
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

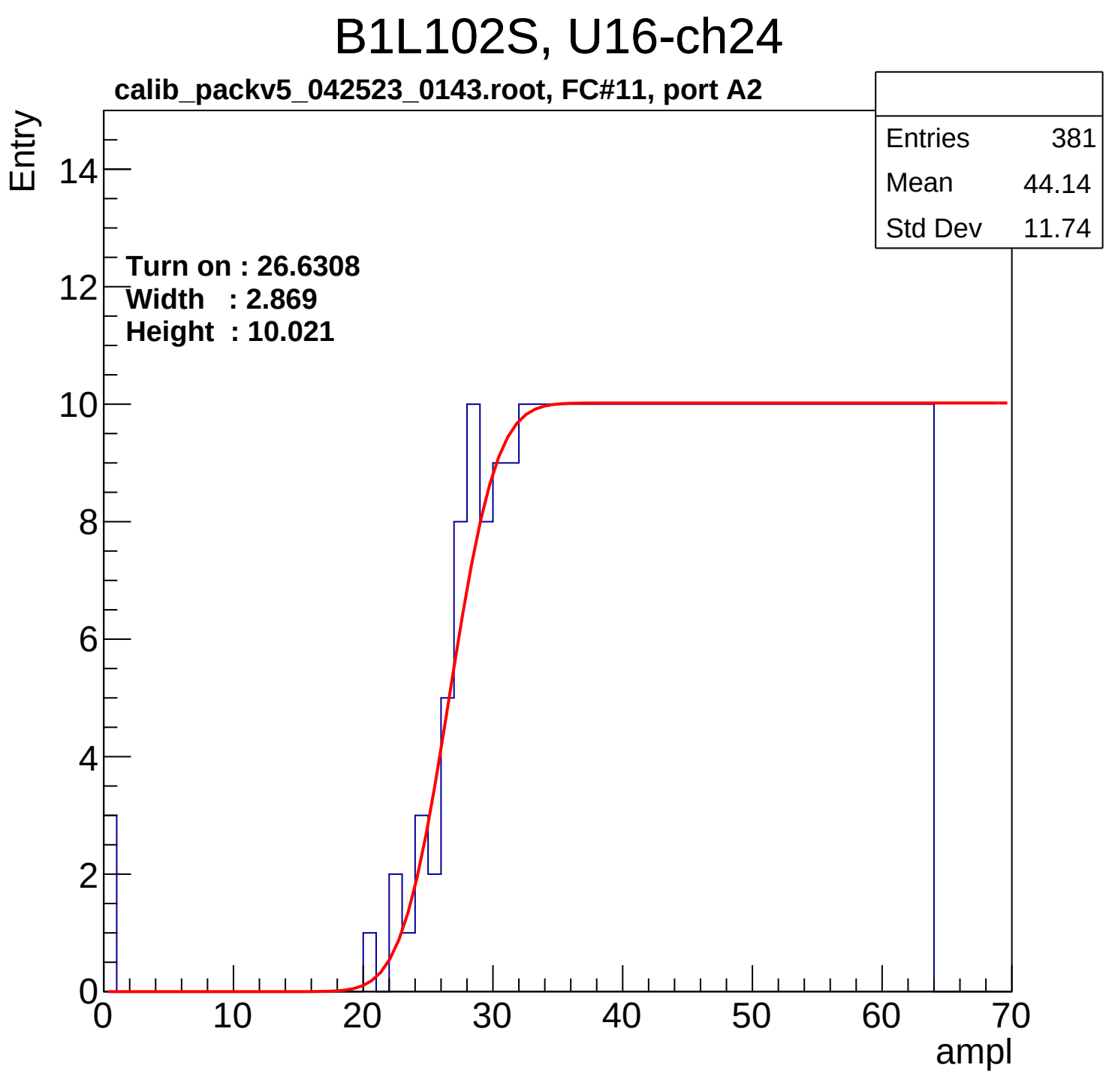

B1L102S, U16-ch19
calib_packv5_042523_0143.root, FC#11, port A2
Entries 373
Mean 44.57
Std Dev 11.48
Turn on : 27.0843
Width : 2.727
Height : 10.009
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

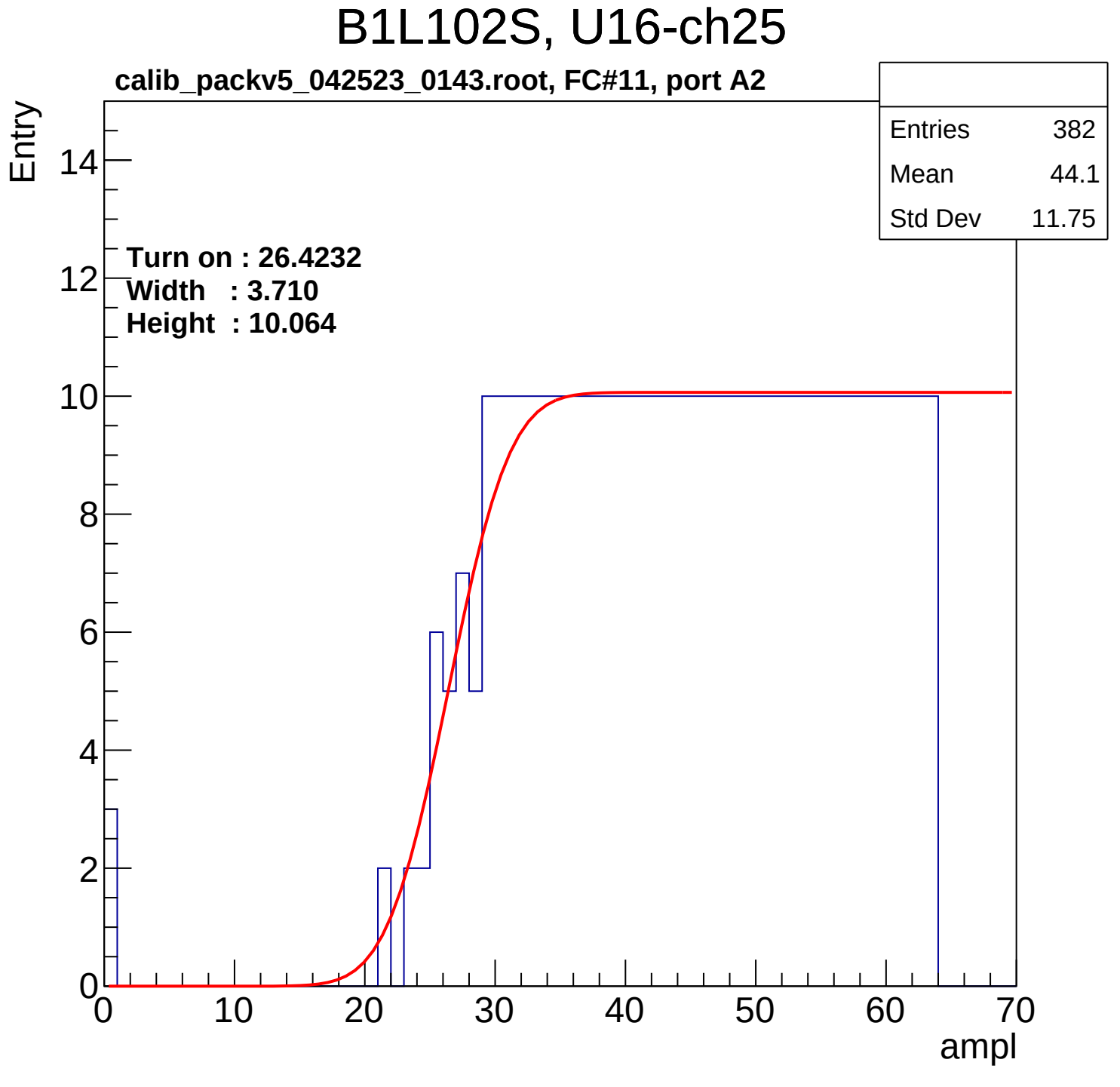

B1L102S, U16-ch20
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 43.92
Std Dev 11.69
Turn on : 25.5839
Width : 3.236
Height : 10.020
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

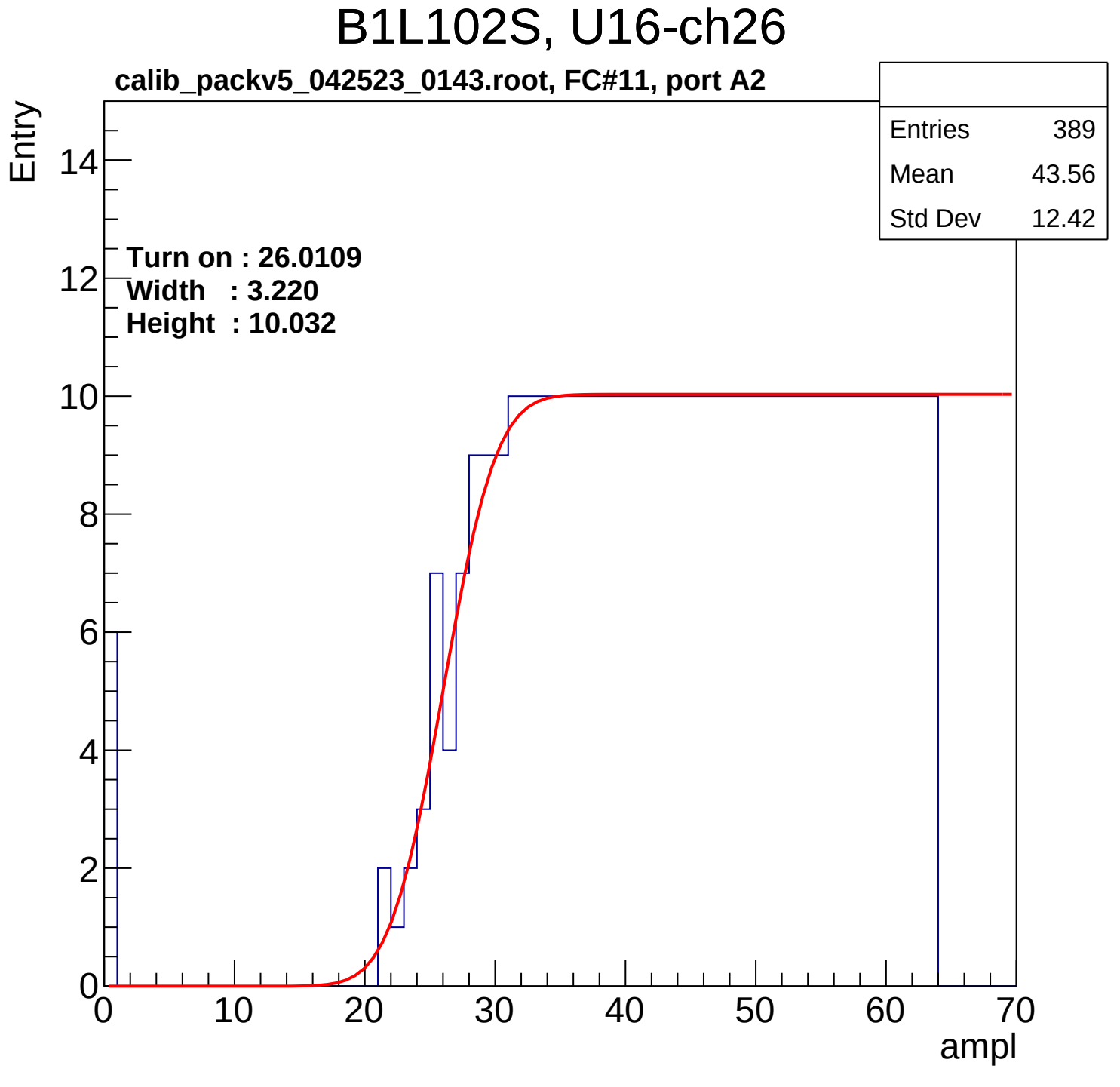

B1L102S, U16-ch21
calib_packv5_042523_0143.root, FC#11, port A2
Entries 376
Mean 44.51
Std Dev 11.24
Turn on : 26.2452
Width : 3.876
Height : 10.020
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

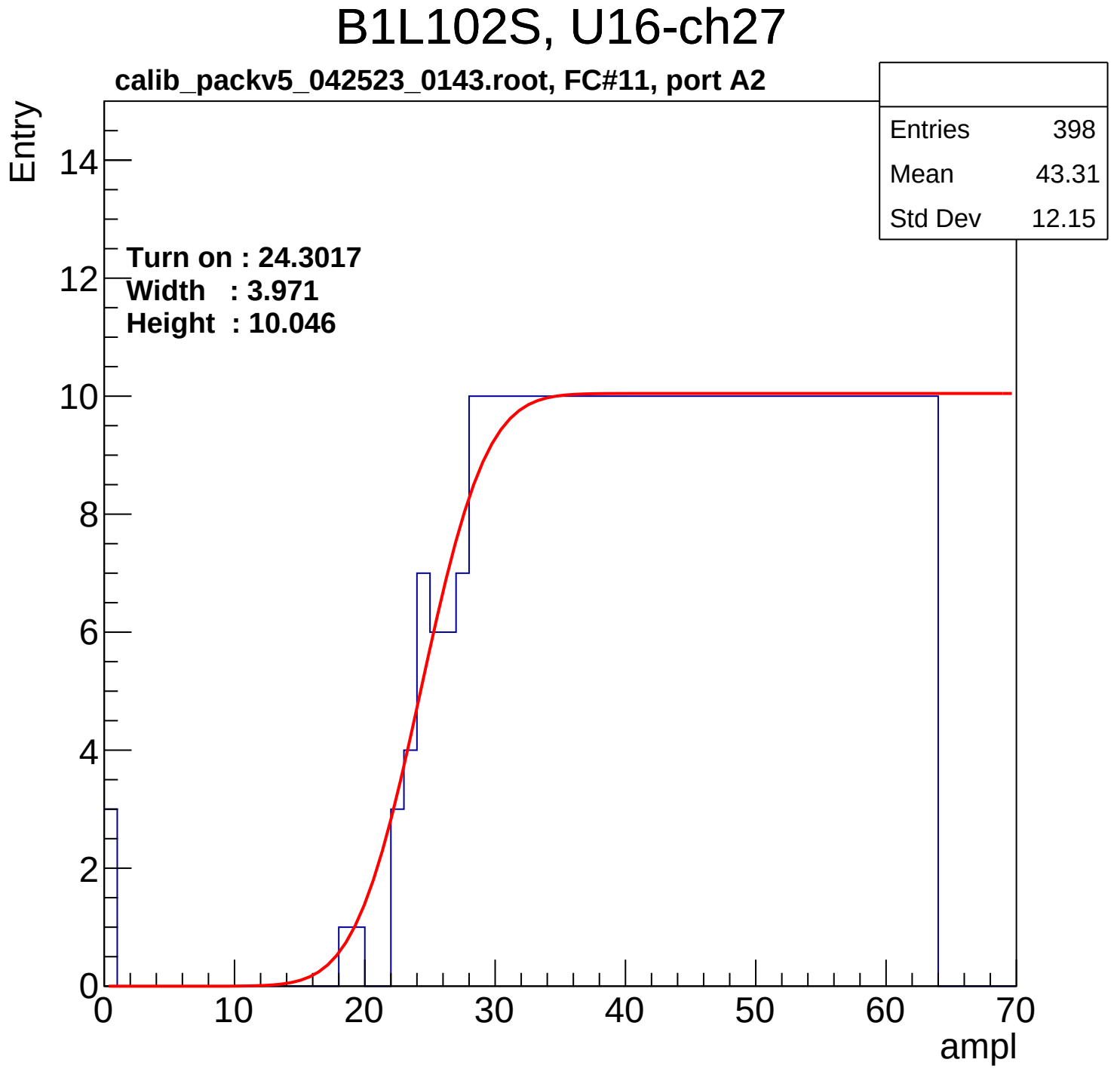

B1L102S, U16-ch22
calib_packv5_042523_0143.root, FC#11, port A2
Entries 396
Mean 43.42
Std Dev 12.08
Turn on : 25.2266
Width : 2.466
Height : 10.004
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

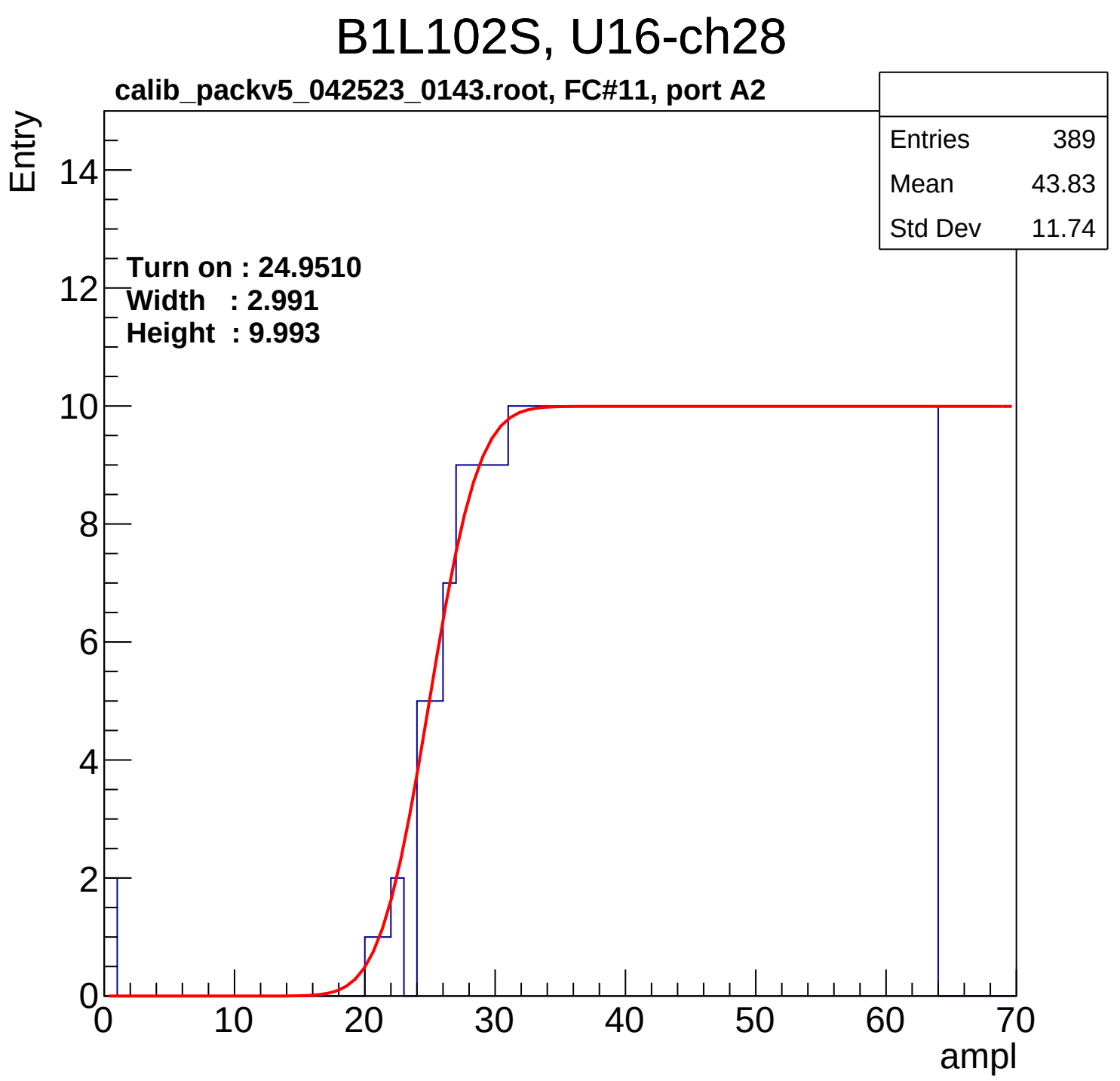

B1L102S, U16-ch23
calib_packv5_042523_0143.root, FC#11, port A2
Entries 404
Mean 42.92
Std Dev 12.55
Turn on : 24.4861
Width : 2.583
Height : 10.009
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

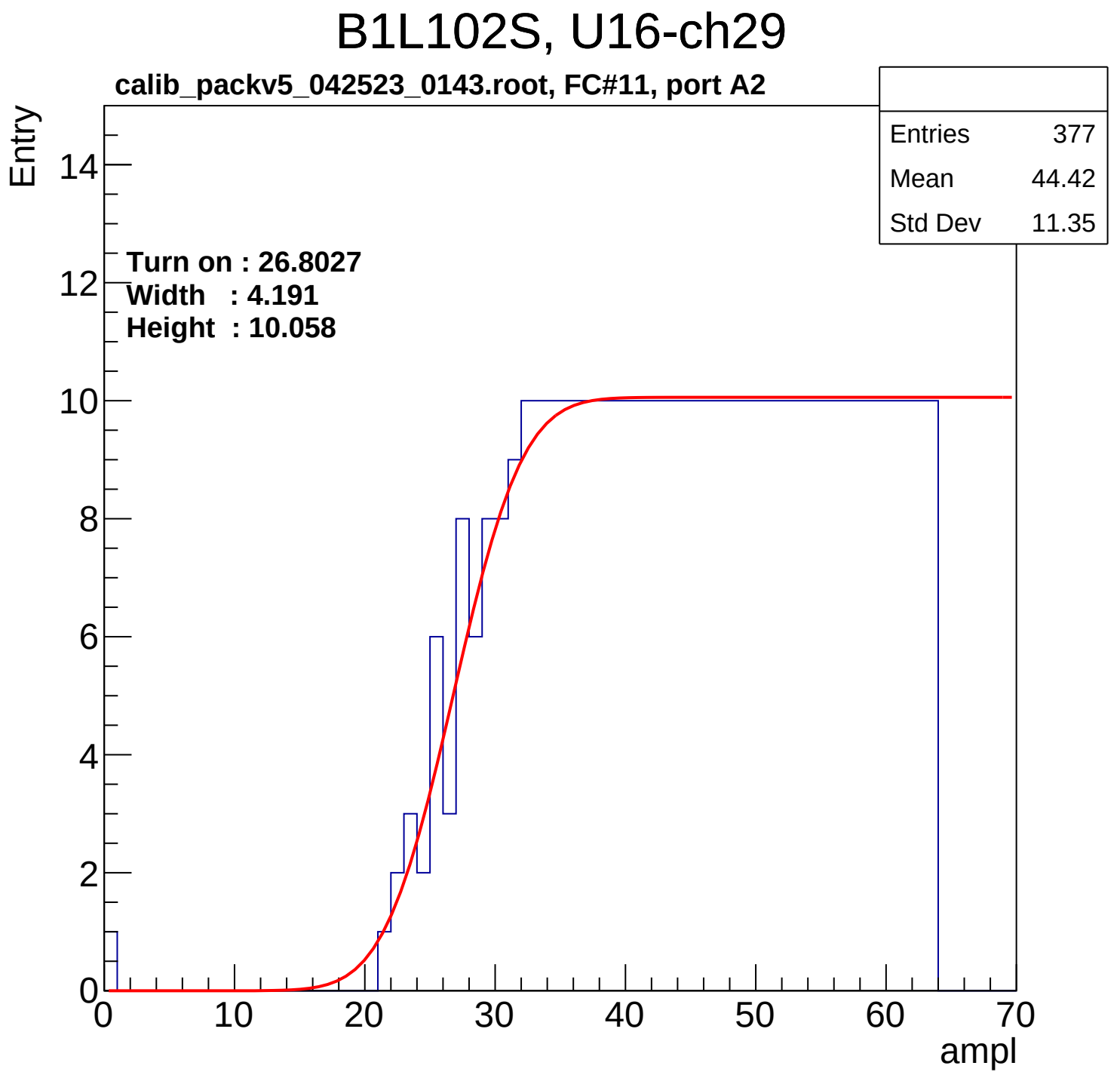

B1L102S, U16-ch24
calib_packv5_042523_0143.root, FC#11, port A2
Entries 381
Mean 44.14
Std Dev 11.74
Turn on : 26.6308
Width : 2.869
Height : 10.021
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

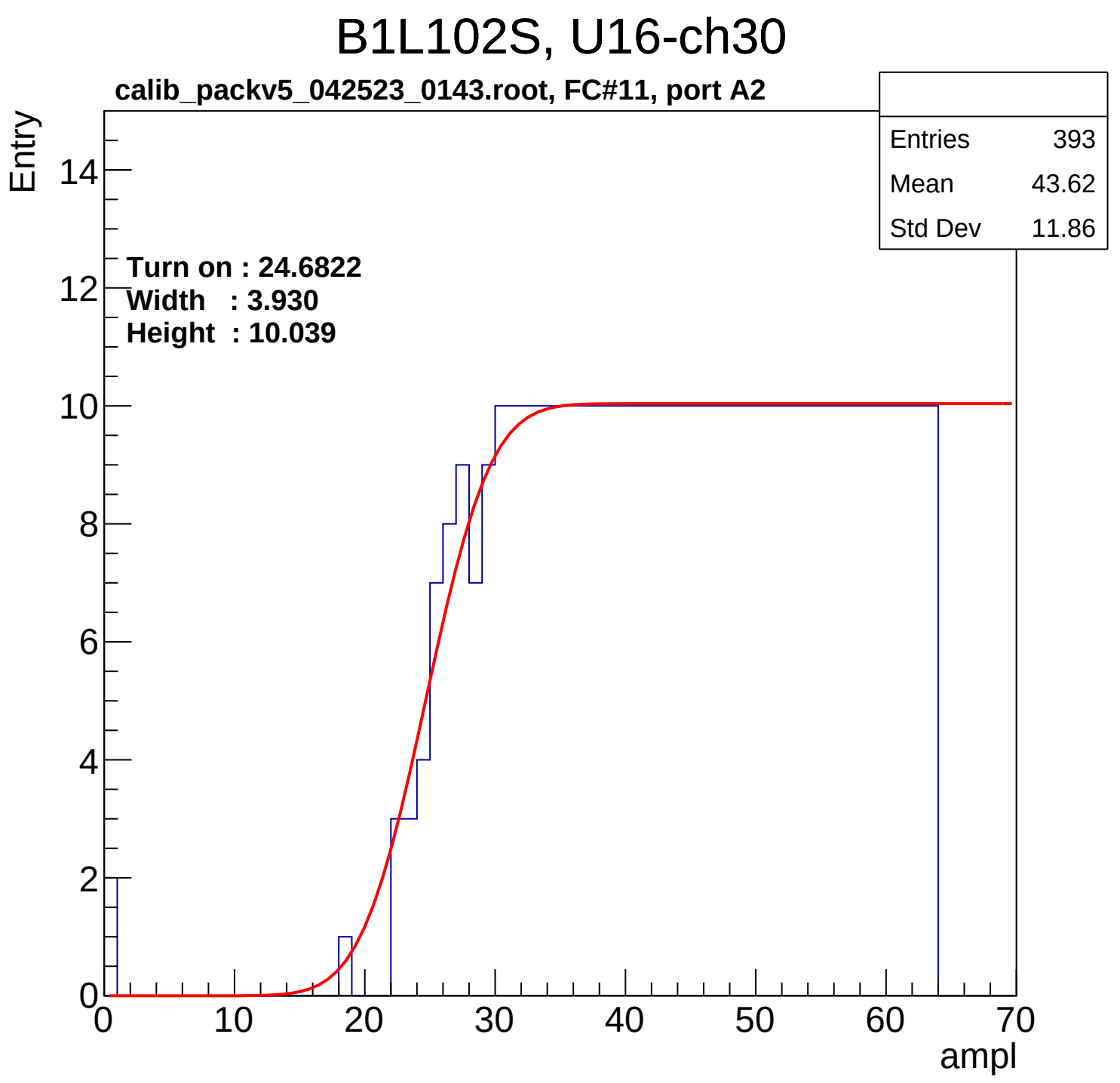

B1L102S, U16-ch25
calib_packv5_042523_0143.root, FC#11, port A2
Entries 382
Mean 44.1
Std Dev 11.75
Turn on : 26.4232
Width : 3.710
Height : 10.064
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

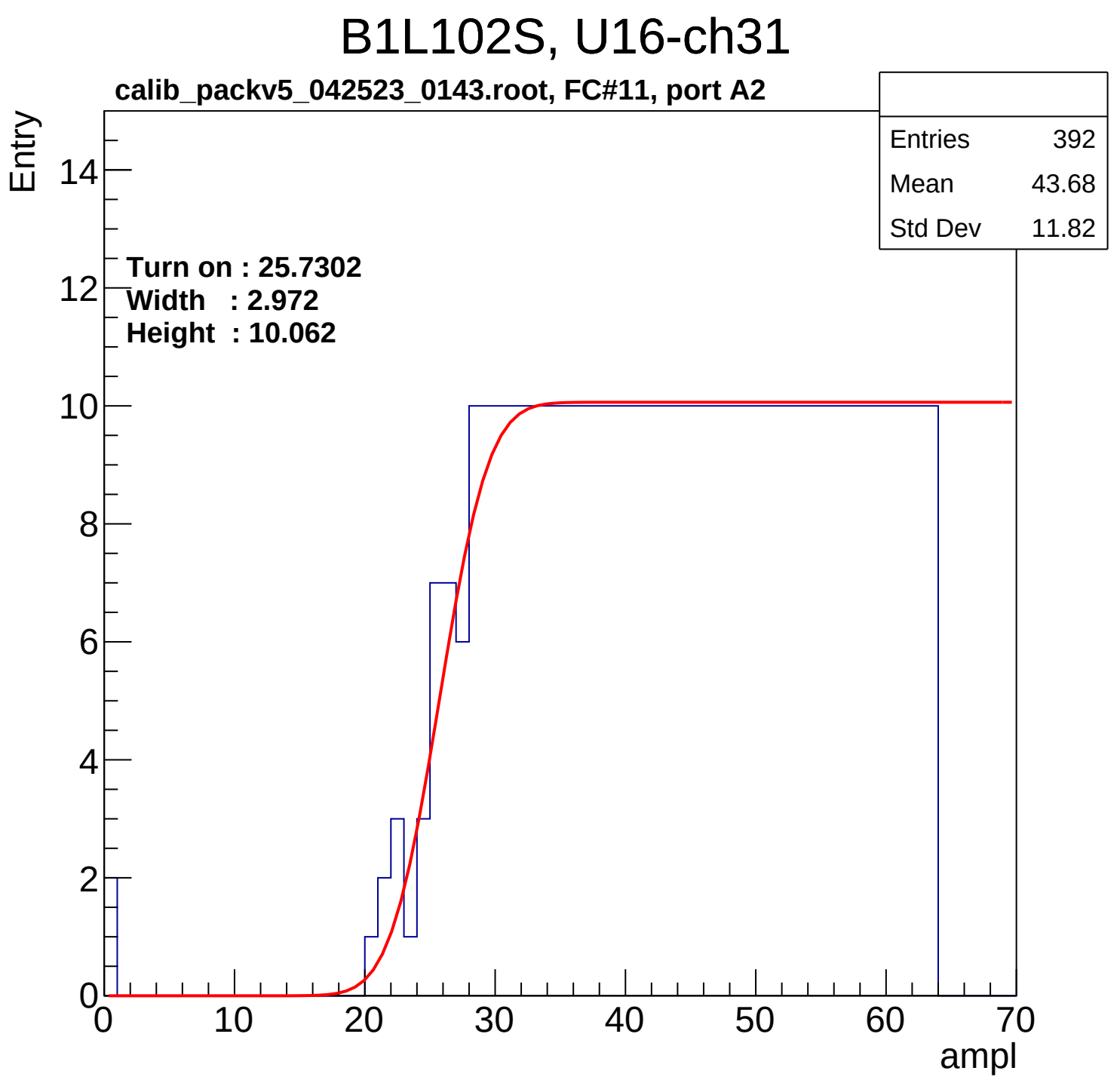

B1L102S, U16-ch26
calib_packv5_042523_0143.root, FC#11, port A2
Entries 389
Mean 43.56
Std Dev 12.42
Turn on : 26.0109
Width : 3.220
Height : 10.032
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

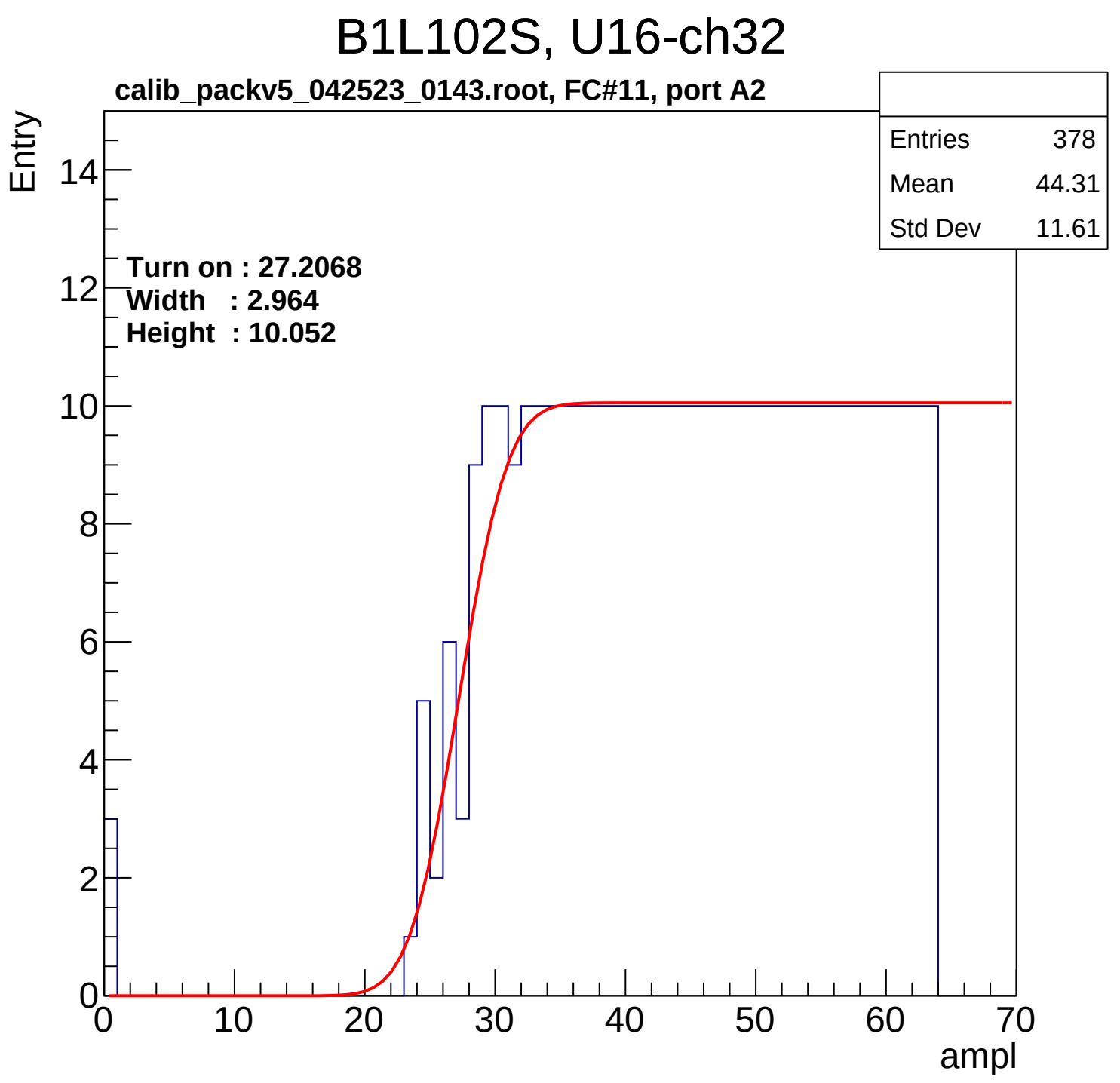

B1L102S, U16-ch27
calib_packv5_042523_0143.root, FC#11, port A2
Entries 398
Mean 43.31
Std Dev 12.15
Turn on : 24.3017
Width : 3.971
Height : 10.046
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

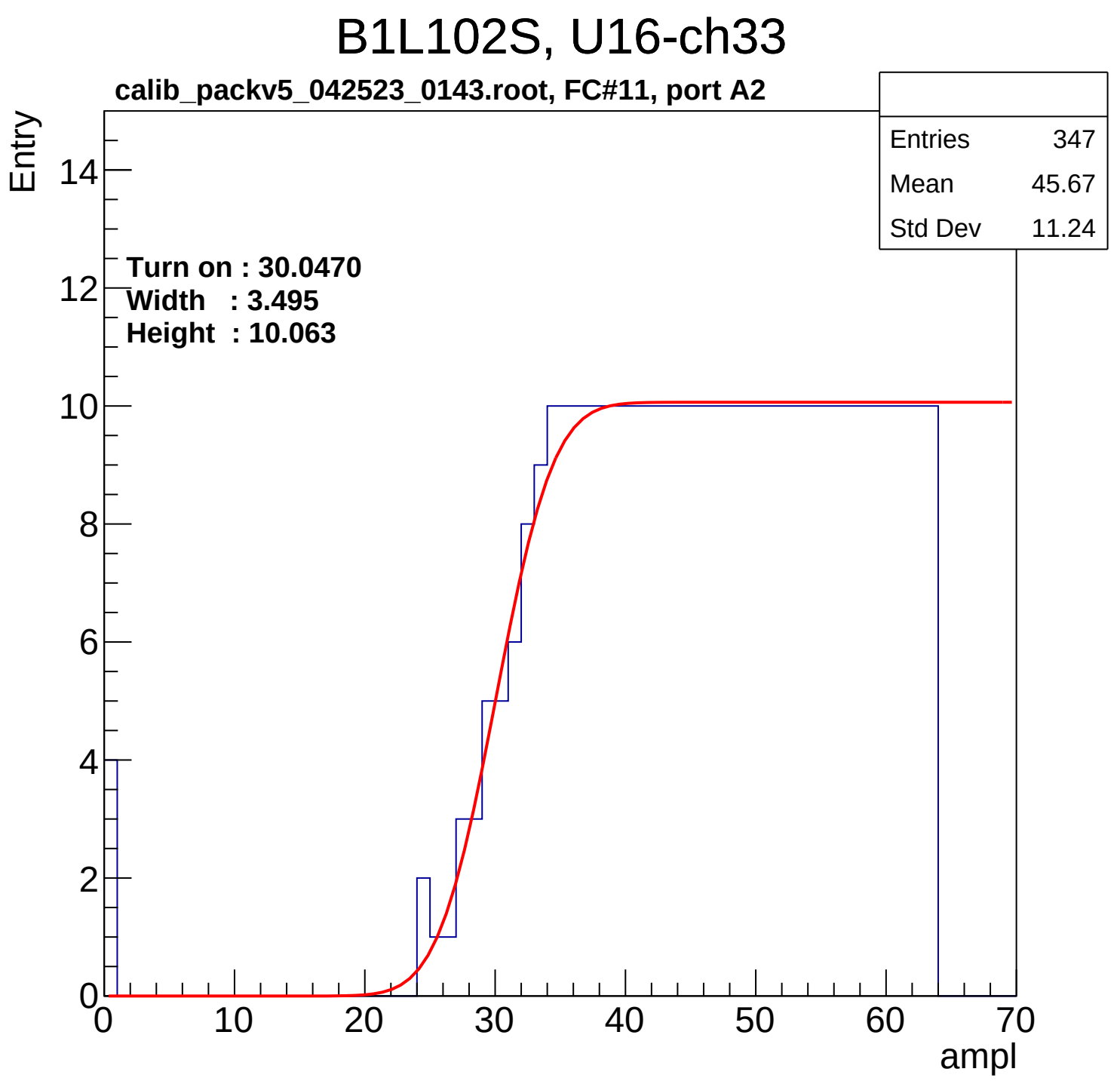

B1L102S, U16-ch28
calib_packv5_042523_0143.root, FC#11, port A2
Entries 389
Mean 43.83
Std Dev 11.74
Turn on : 24.9510
Width : 2.991
Height : 9.993
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

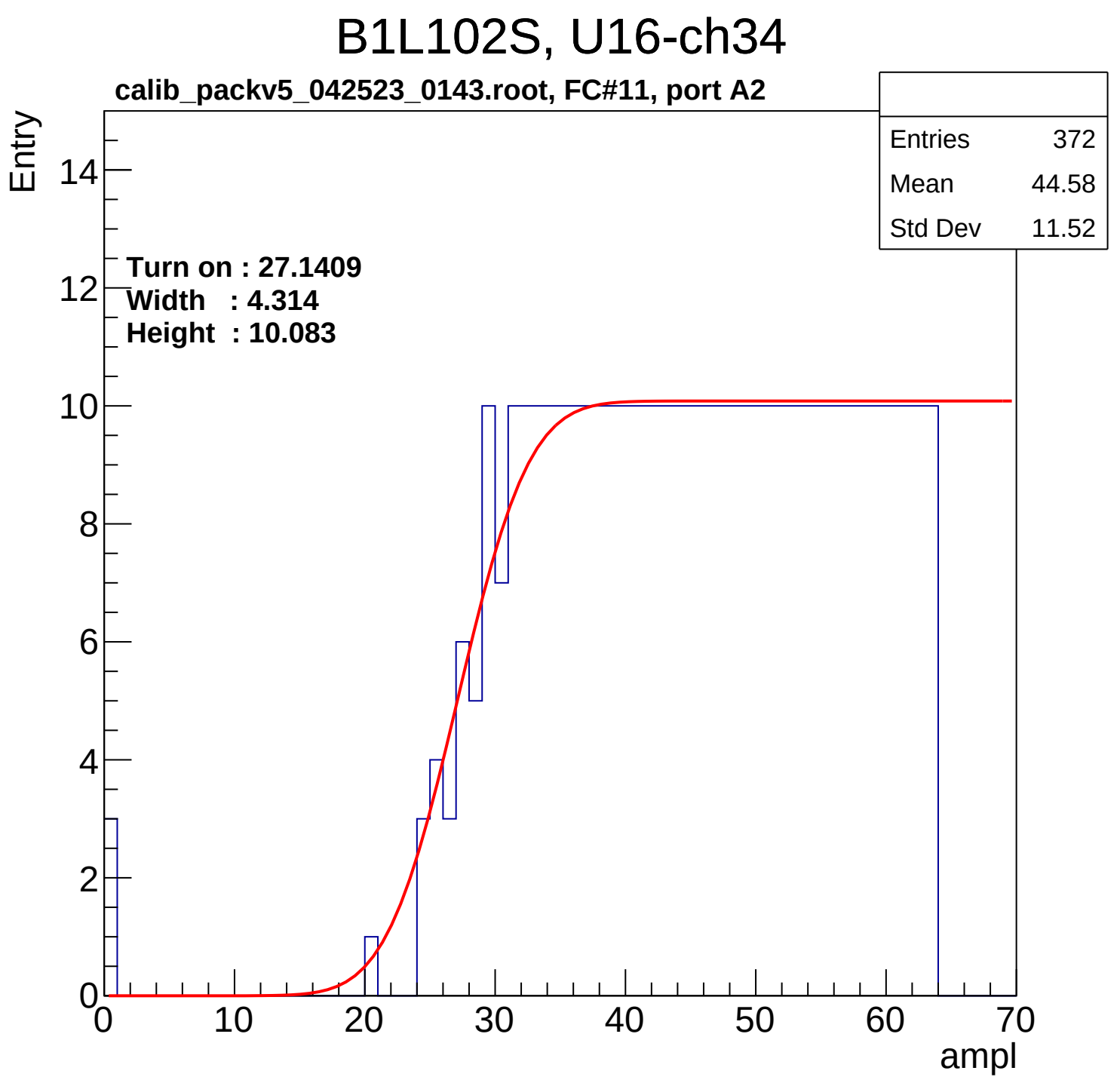

B1L102S, U16-ch29
calib_packv5_042523_0143.root, FC#11, port A2
Entries 377
Mean 44.42
Std Dev 11.35
Turn on : 26.8027
Width : 4.191
Height : 10.058
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

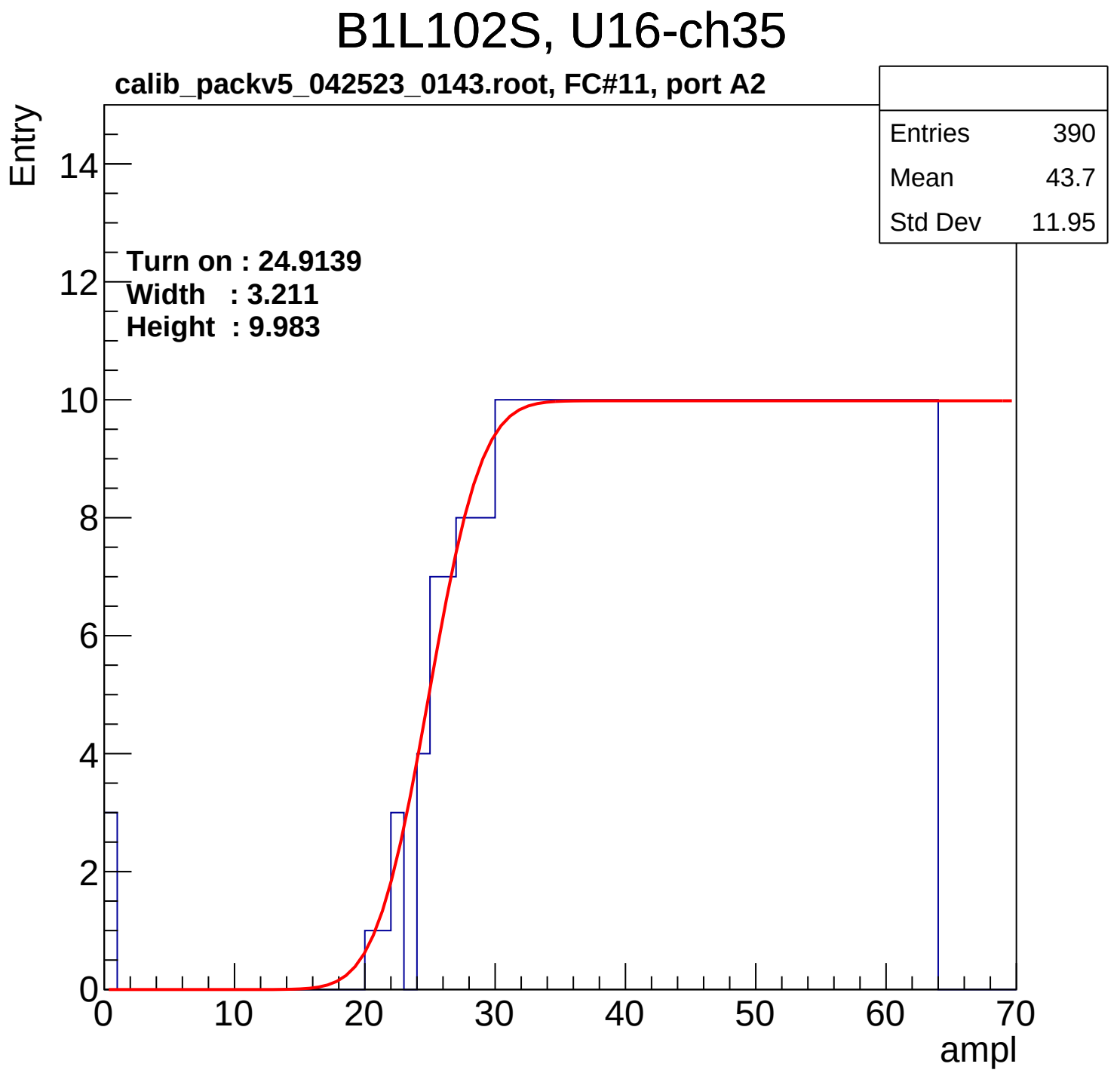

B1L102S, U16-ch30
calib_packv5_042523_0143.root, FC#11, port A2
Entries 393
Mean 43.62
Std Dev 11.86
Turn on : 24.6822
Width : 3.930
Height : 10.039
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

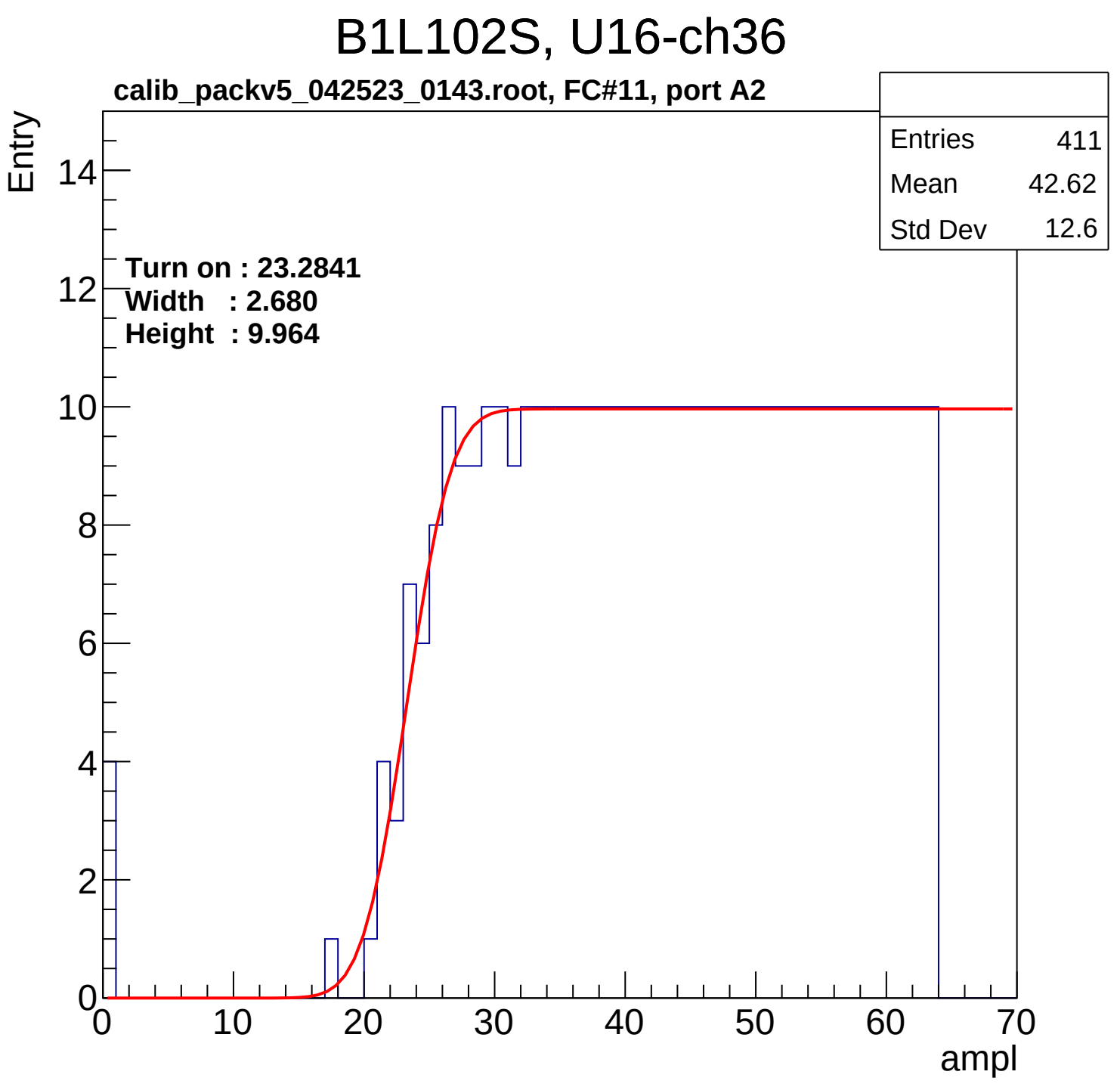

B1L102S, U16-ch31
calib_packv5_042523_0143.root, FC#11, port A2
Entries 392
Mean 43.68
Std Dev 11.82
Turn on : 25.7302
Width : 2.972
Height : 10.062
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

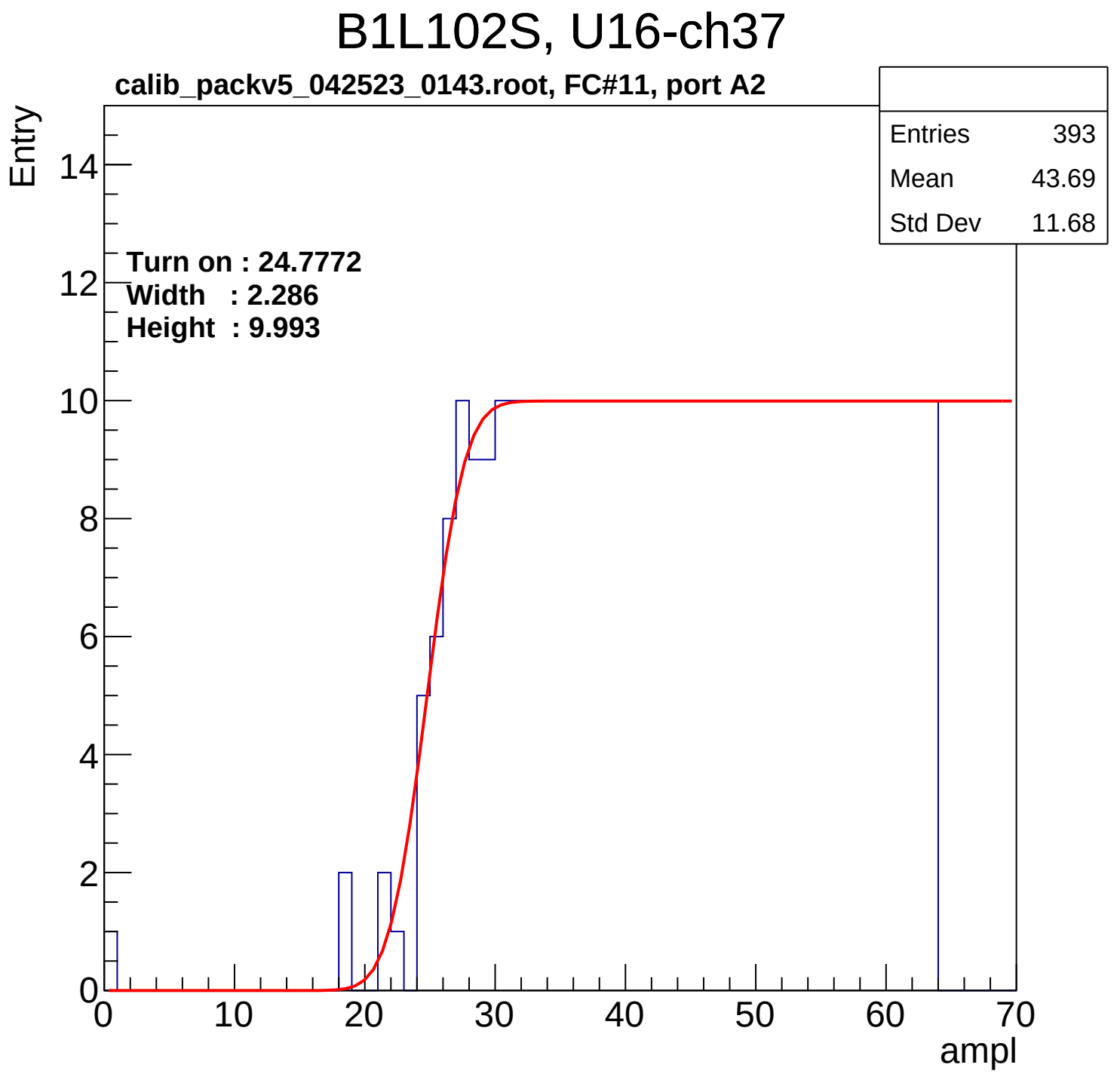

B1L102S, U16-ch32
calib_packv5_042523_0143.root, FC#11, port A2
Entries 378
Mean 44.31
Std Dev 11.61
Turn on : 27.2068
Width : 2.964
Height : 10.052
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

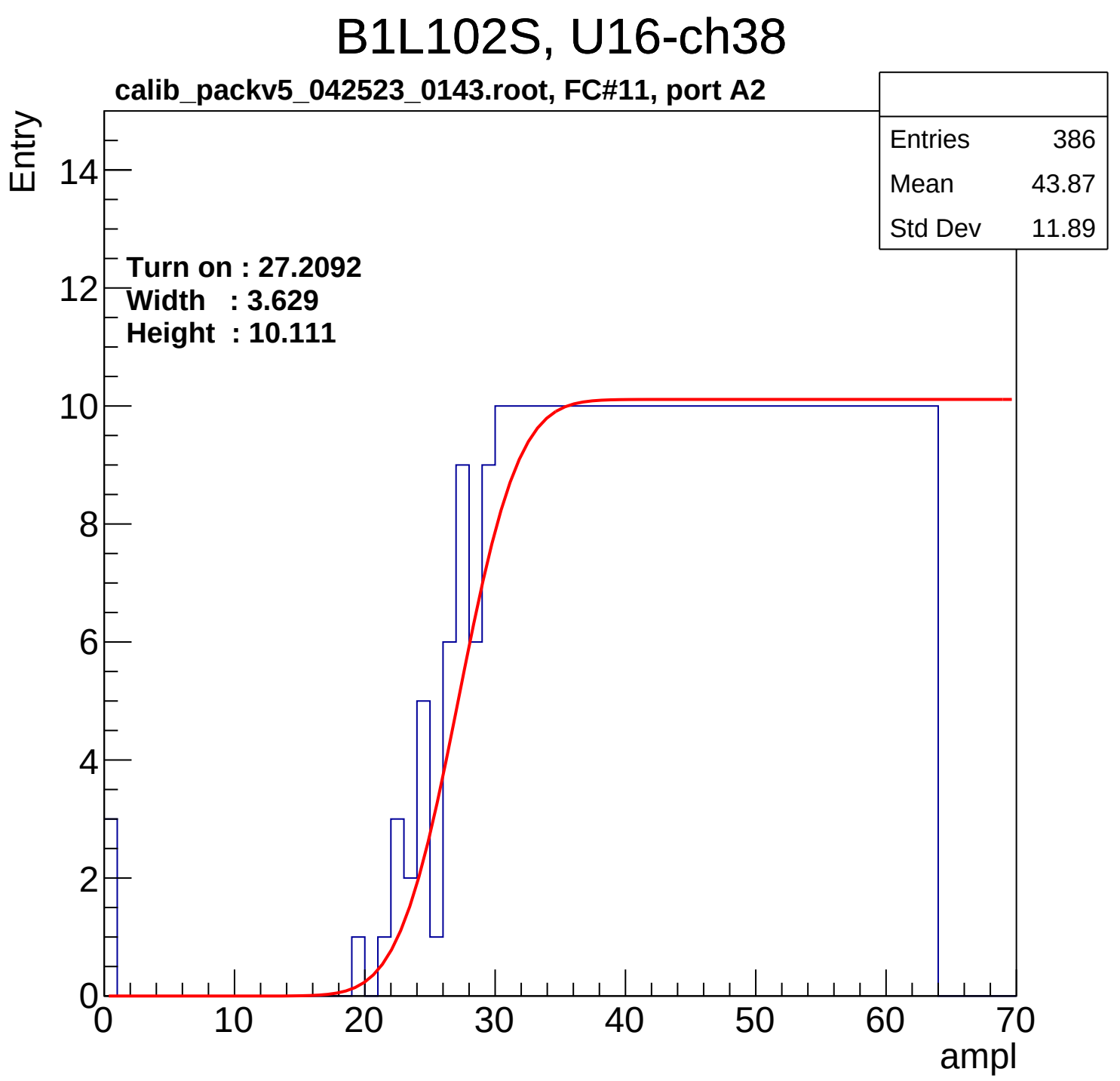

B1L102S, U16-ch33
calib_packv5_042523_0143.root, FC#11, port A2
Entries 347
Mean 45.67
Std Dev 11.24
Turn on : 30.0470
Width : 3.495
Height : 10.063
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

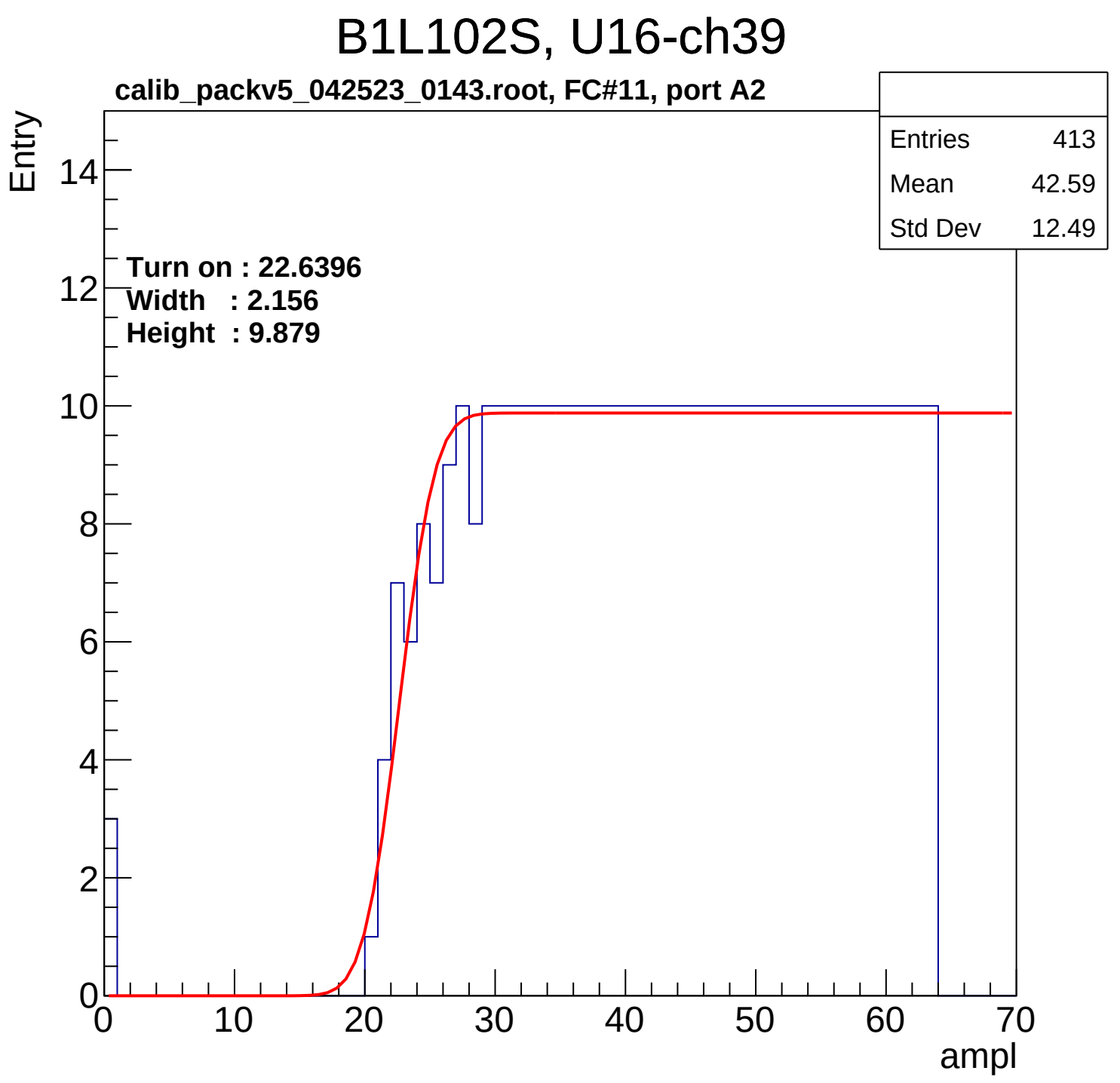

B1L102S, U16-ch34
calib_packv5_042523_0143.root, FC#11, port A2
Entries 372
Mean 44.58
Std Dev 11.52
Turn on : 27.1409
Width : 4.314
Height : 10.083
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

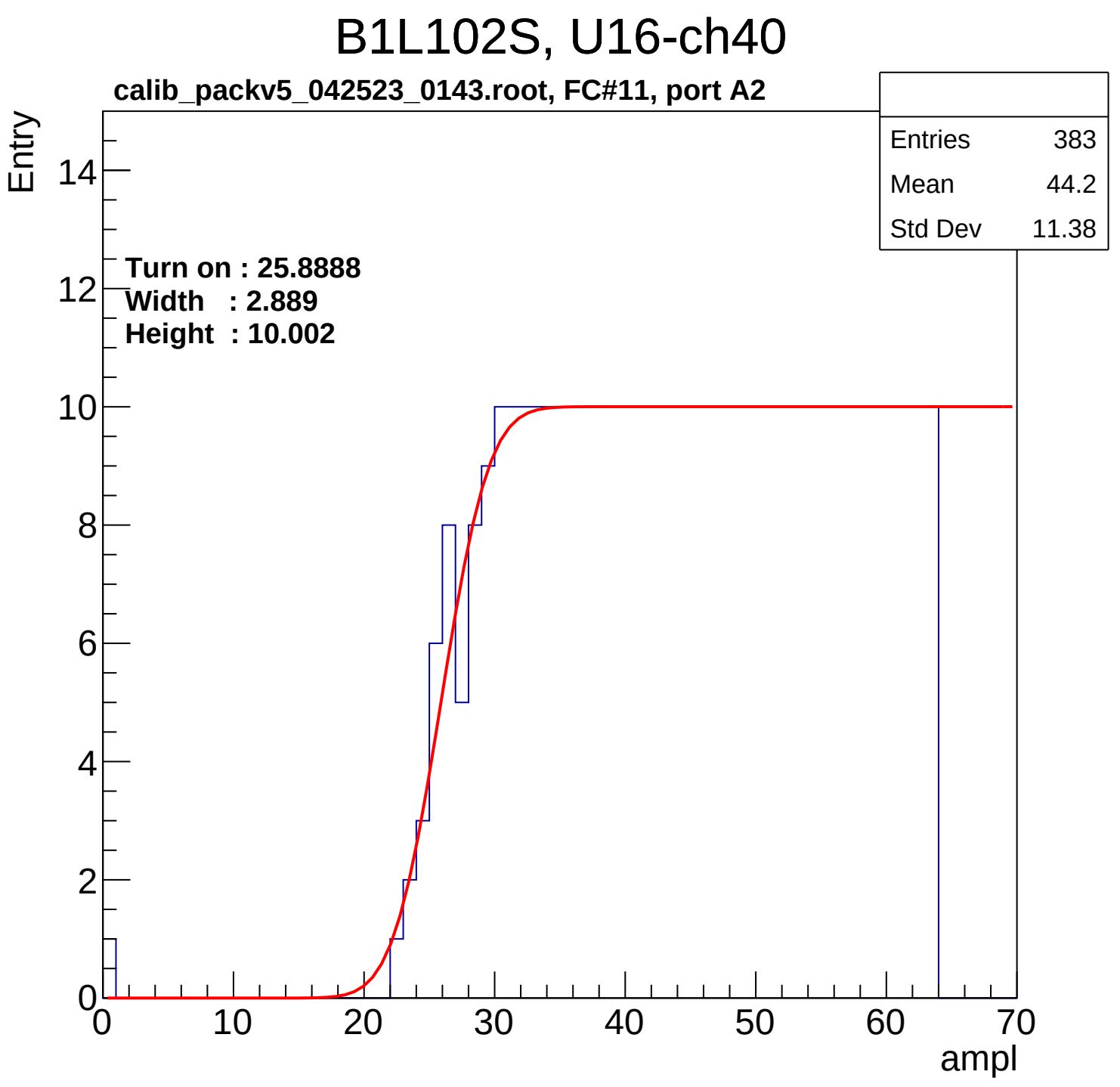

B1L102S, U16-ch35
calib_packv5_042523_0143.root, FC#11, port A2
Entries 390
Mean 43.7
Std Dev 11.95
Turn on : 24.9139
Width : 3.211
Height : 9.983
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

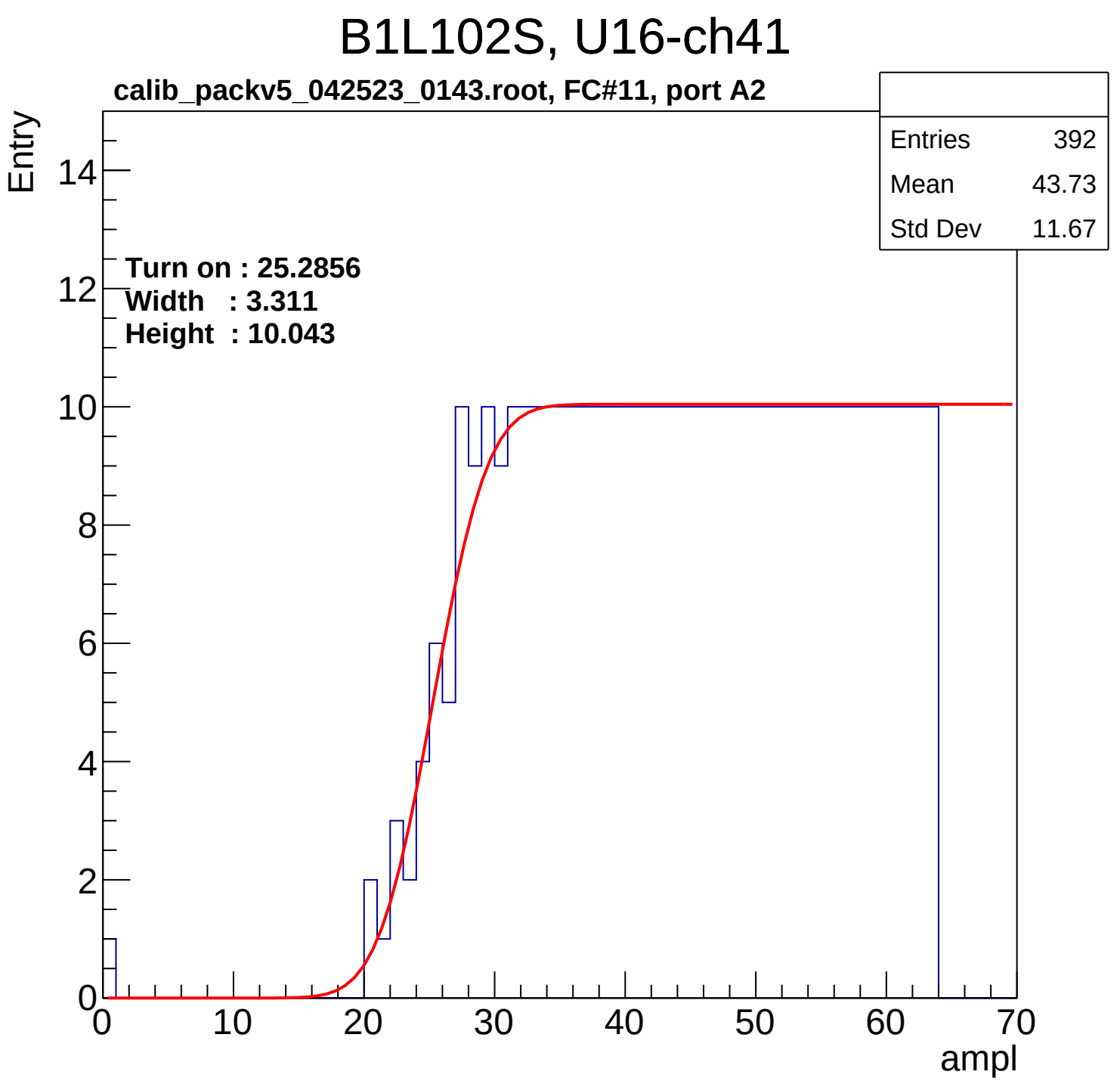

B1L102S, U16-ch36
calib_packv5_042523_0143.root, FC#11, port A2
Entries 411
Mean 42.62
Std Dev 12.6
Turn on : 23.2841
Width : 2.680
Height : 9.964
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

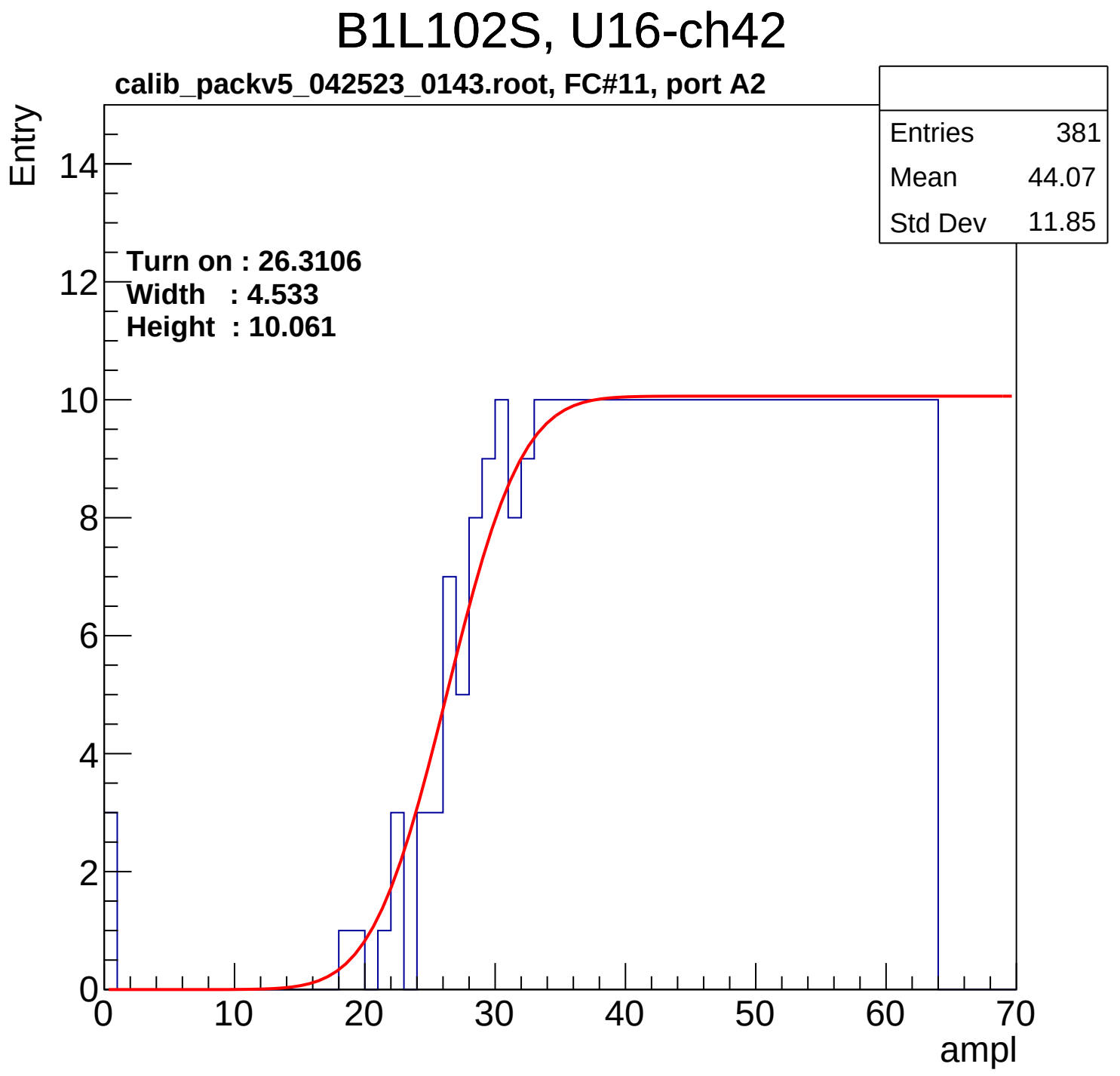

B1L102S, U16-ch37
calib_packv5_042523_0143.root, FC#11, port A2
Entries 393
Mean 43.69
Std Dev 11.68
Turn on : 24.7772
Width : 2.286
Height : 9.993
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

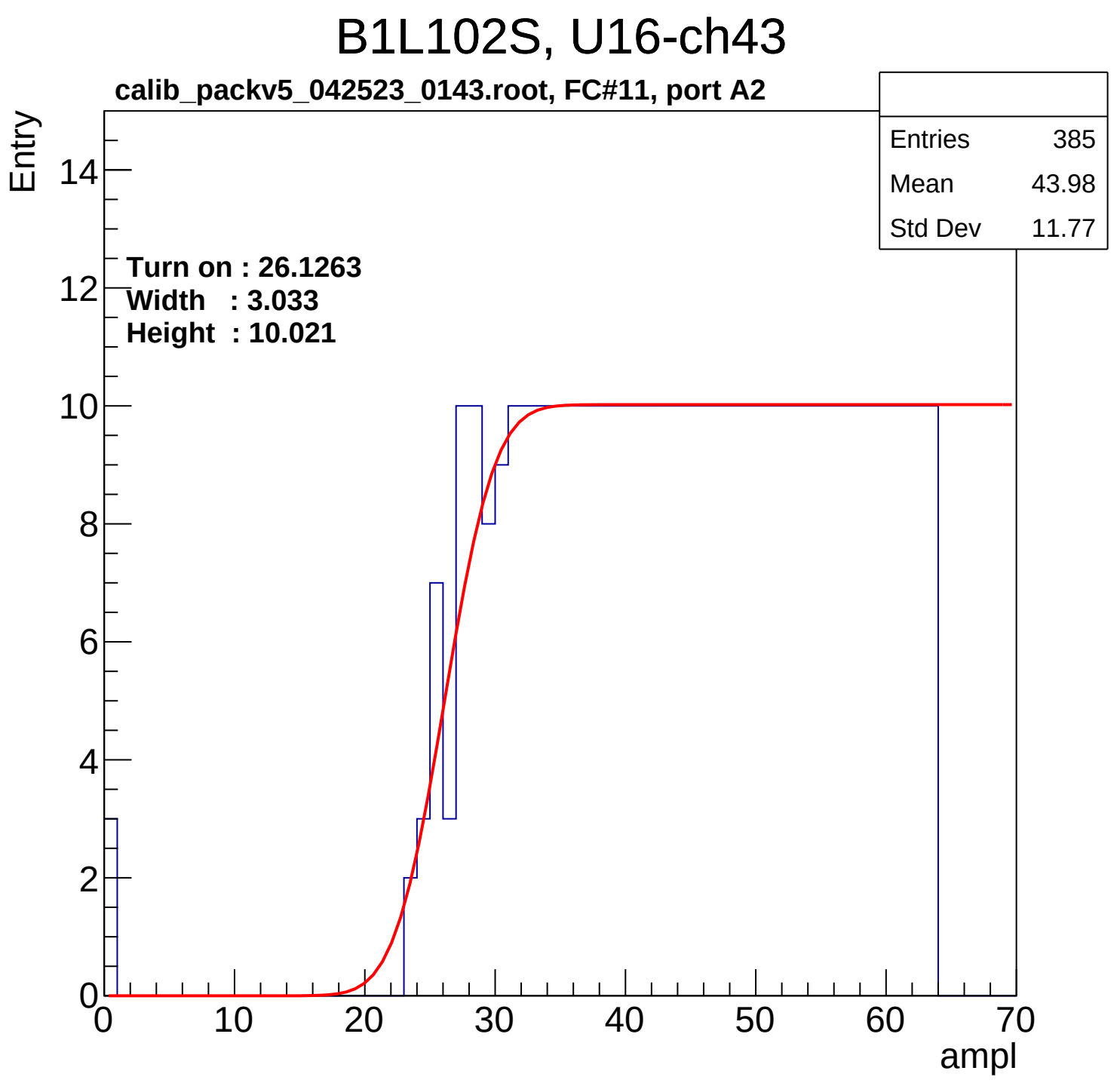

B1L102S, U16-ch38
calib_packv5_042523_0143.root, FC#11, port A2
Entries 386
Mean 43.87
Std Dev 11.89
Turn on : 27.2092
Width : 3.629
Height : 10.111
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

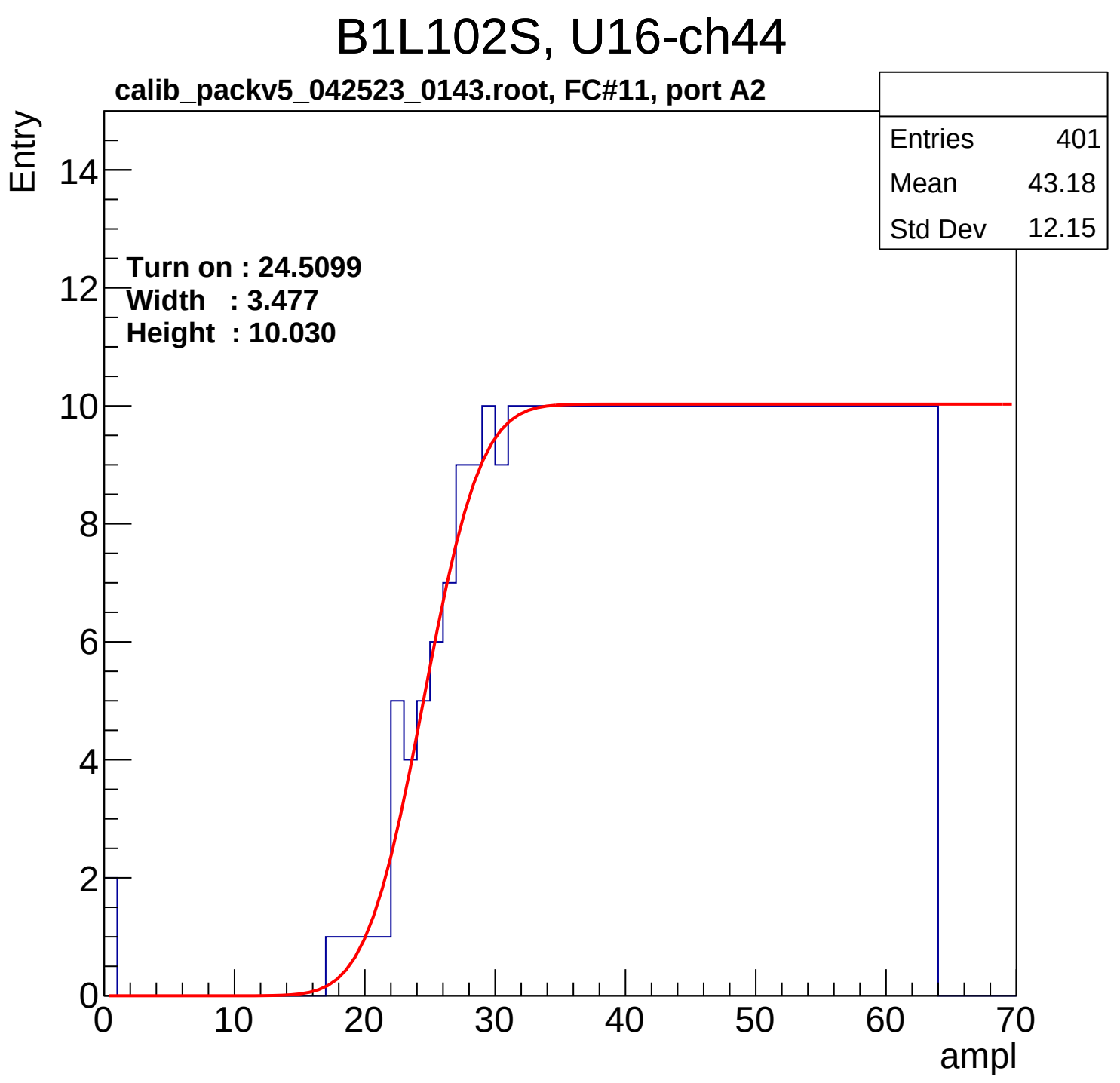

B1L102S, U16-ch39
calib_packv5_042523_0143.root, FC#11, port A2
Entries 413
Mean 42.59
Std Dev 12.49
Turn on : 22.6396
Width : 2.156
Height : 9.879
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

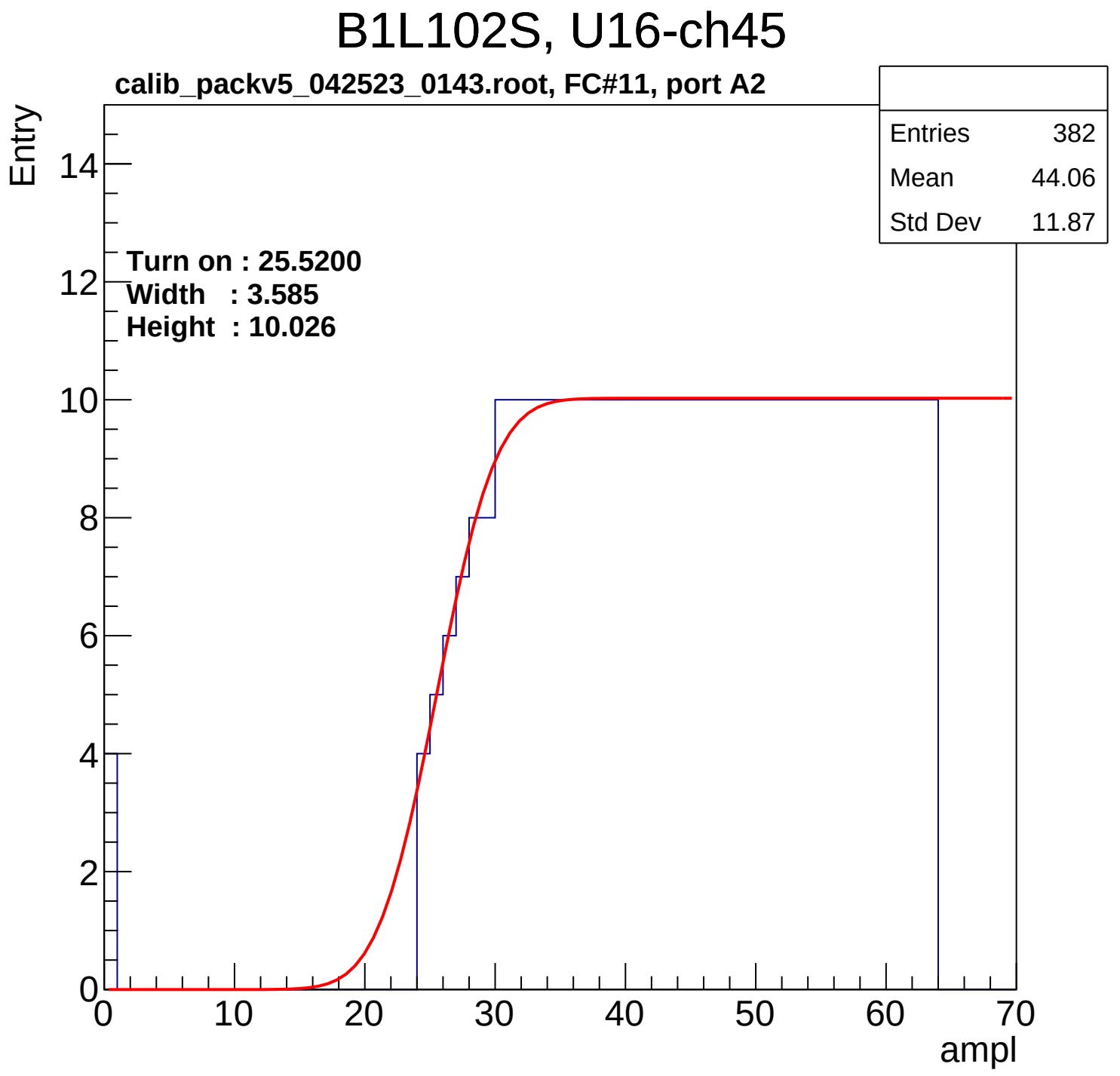

B1L102S, U16-ch40
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 44.2
Std Dev 11.38
Turn on : 25.8888
Width : 2.889
Height : 10.002
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

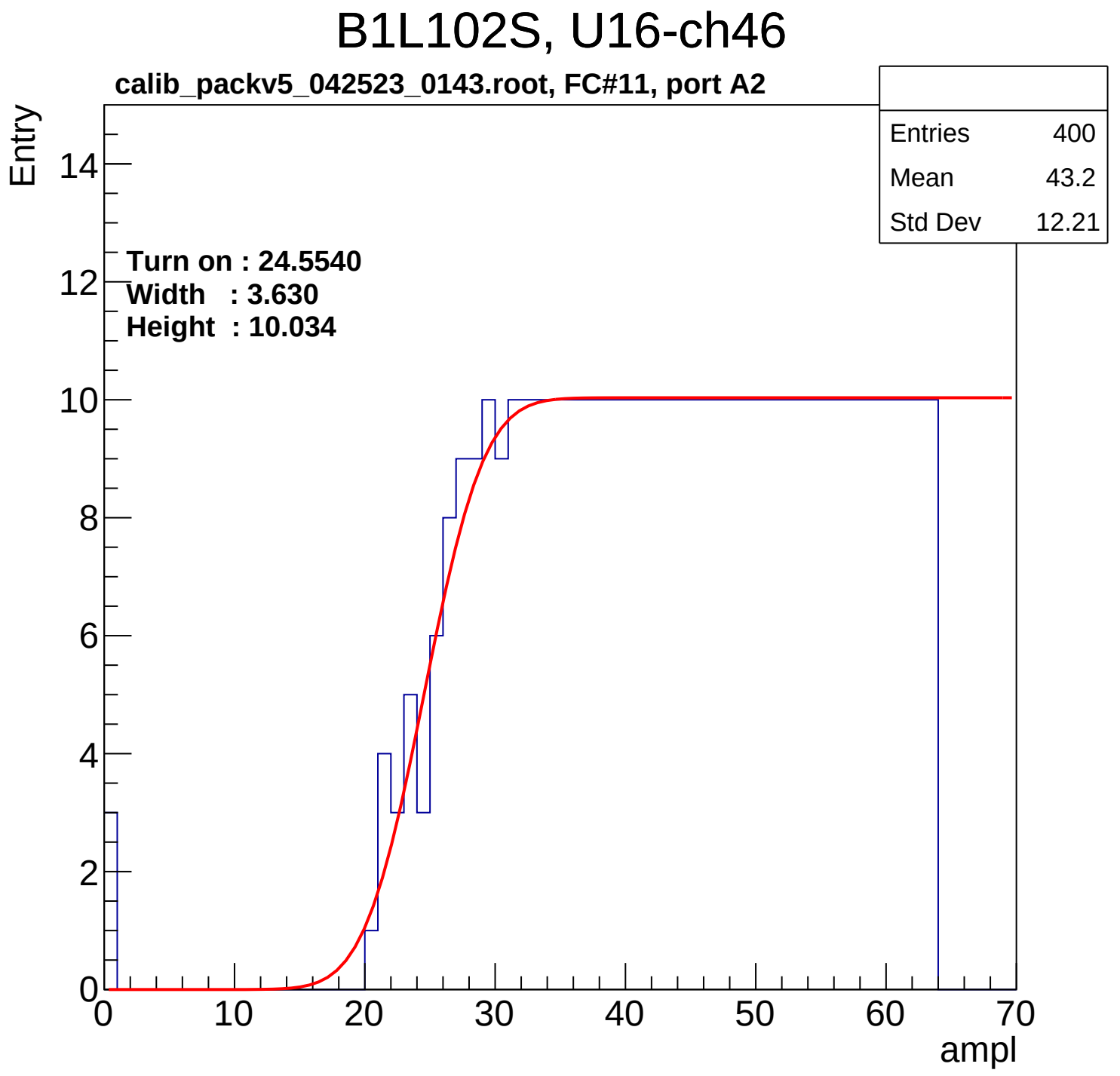

B1L102S, U16-ch41
calib_packv5_042523_0143.root, FC#11, port A2
Entries 392
Mean 43.73
Std Dev 11.67
Turn on : 25.2856
Width : 3.311
Height : 10.043
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

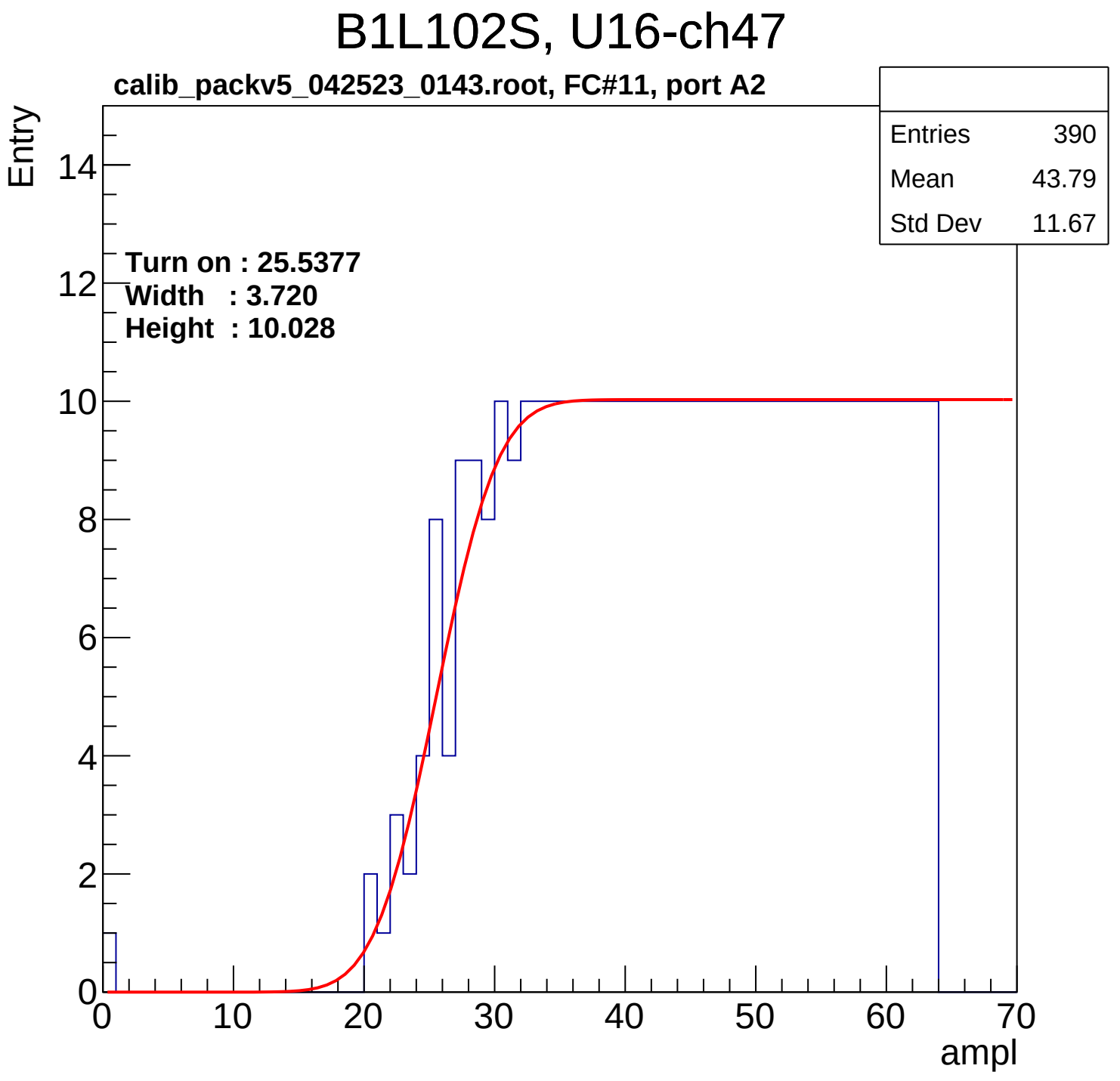

B1L102S, U16-ch42
calib_packv5_042523_0143.root, FC#11, port A2
Entries 381
Mean 44.07
Std Dev 11.85
Turn on : 26.3106
Width : 4.533
Height : 10.061
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

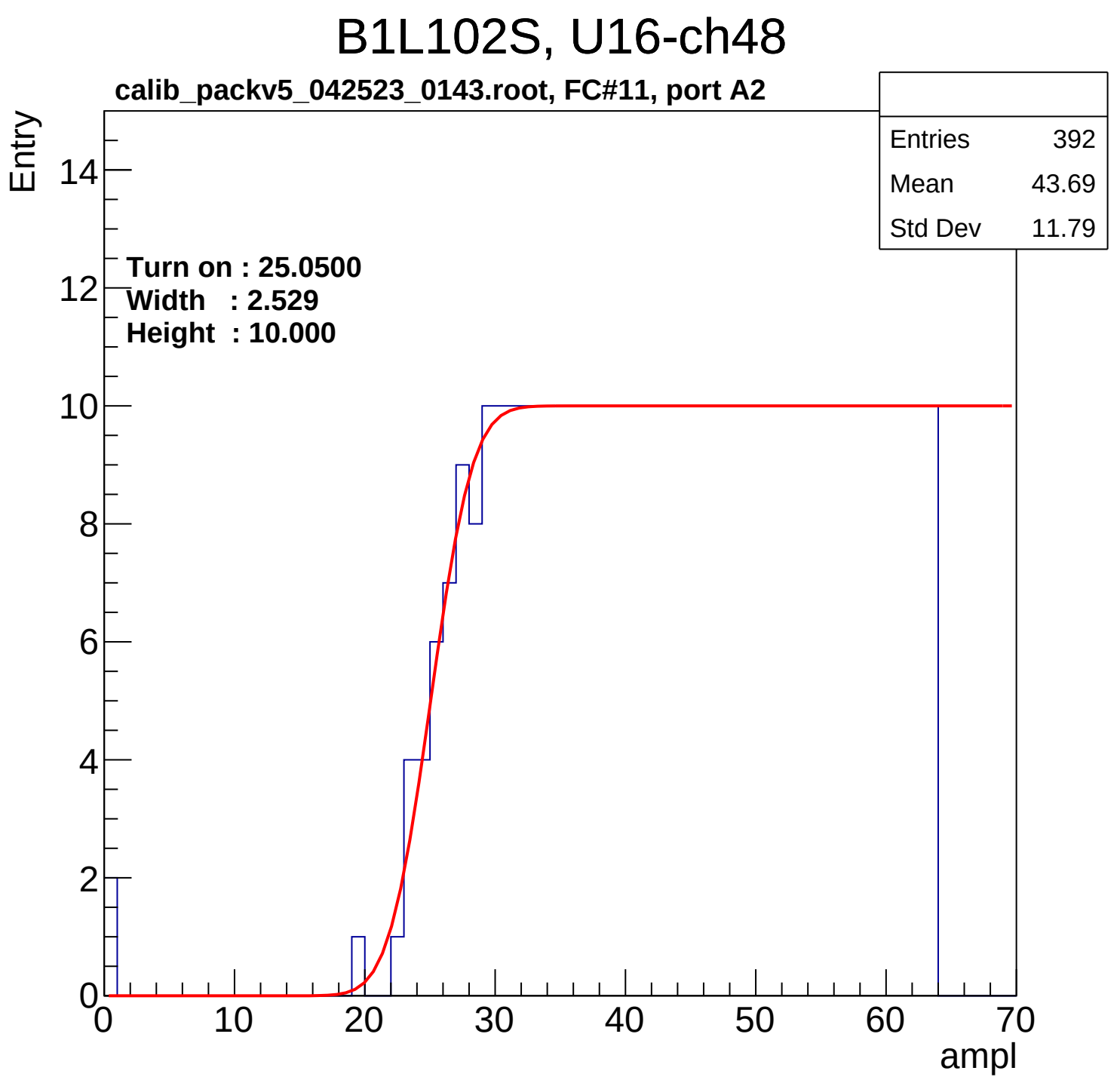

B1L102S, U16-ch43
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 43.98
Std Dev 11.77
Turn on : 26.1263
Width : 3.033
Height : 10.021
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

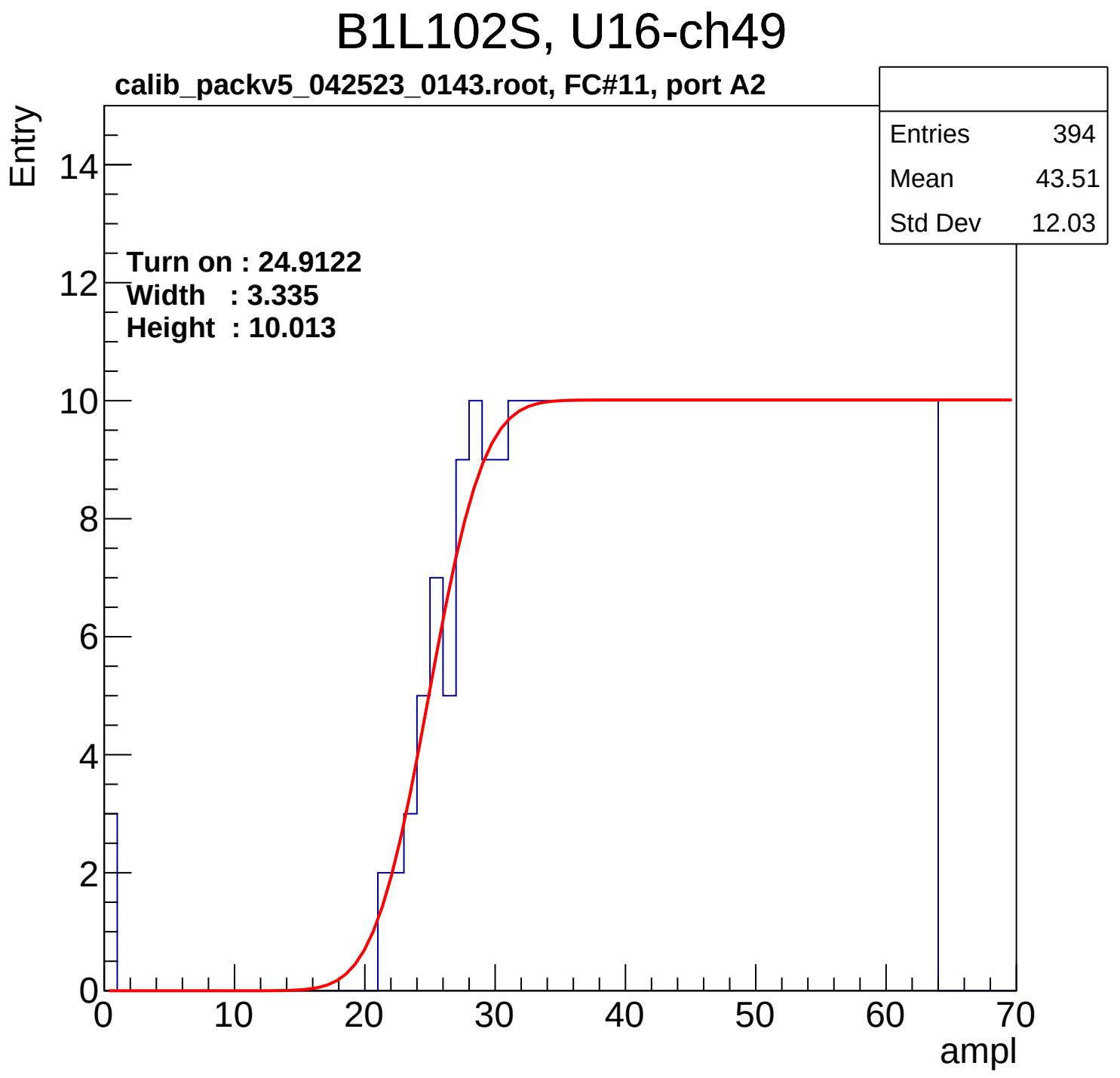

B1L102S, U16-ch44
calib_packv5_042523_0143.root, FC#11, port A2
Entries 401
Mean 43.18
Std Dev 12.15
Turn on : 24.5099
Width : 3.477
Height : 10.030
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

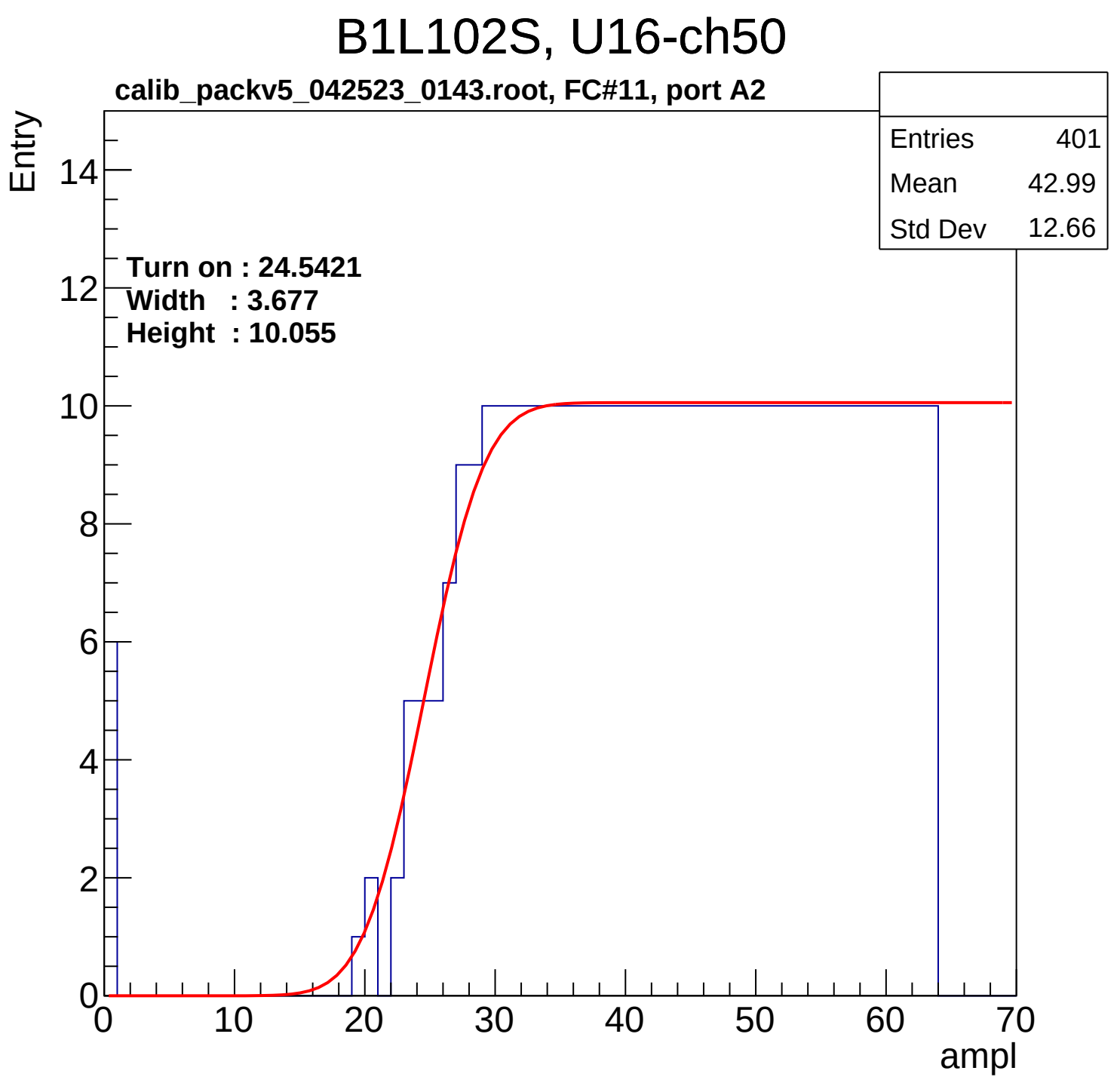

B1L102S, U16-ch45
calib_packv5_042523_0143.root, FC#11, port A2
Entries 382
Mean 44.06
Std Dev 11.87
Turn on : 25.5200
Width : 3.585
Height : 10.026
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

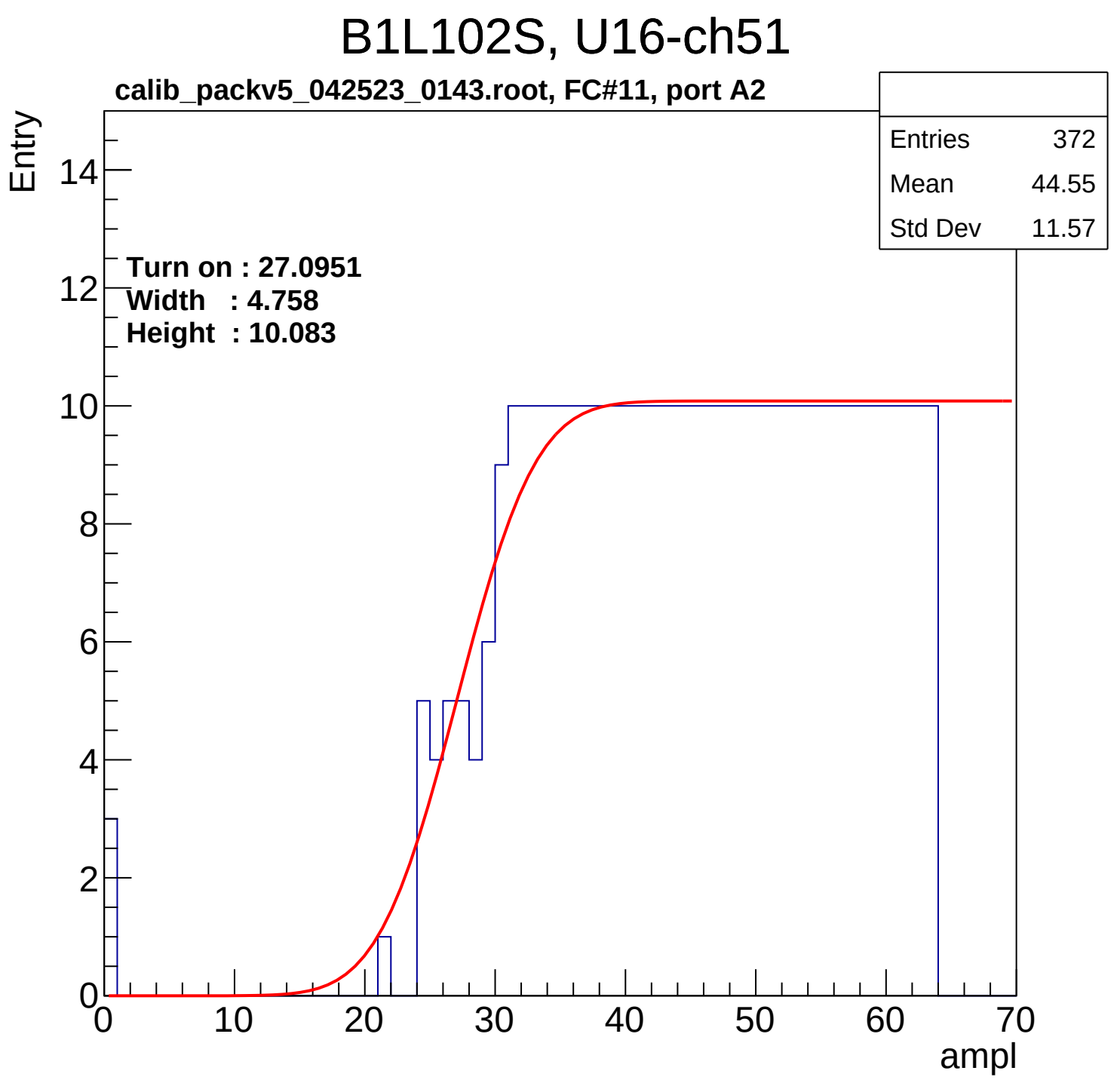

B1L102S, U16-ch46
calib_packv5_042523_0143.root, FC#11, port A2
Entries 400
Mean 43.2
Std Dev 12.21
Turn on : 24.5540
Width : 3.630
Height : 10.034
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

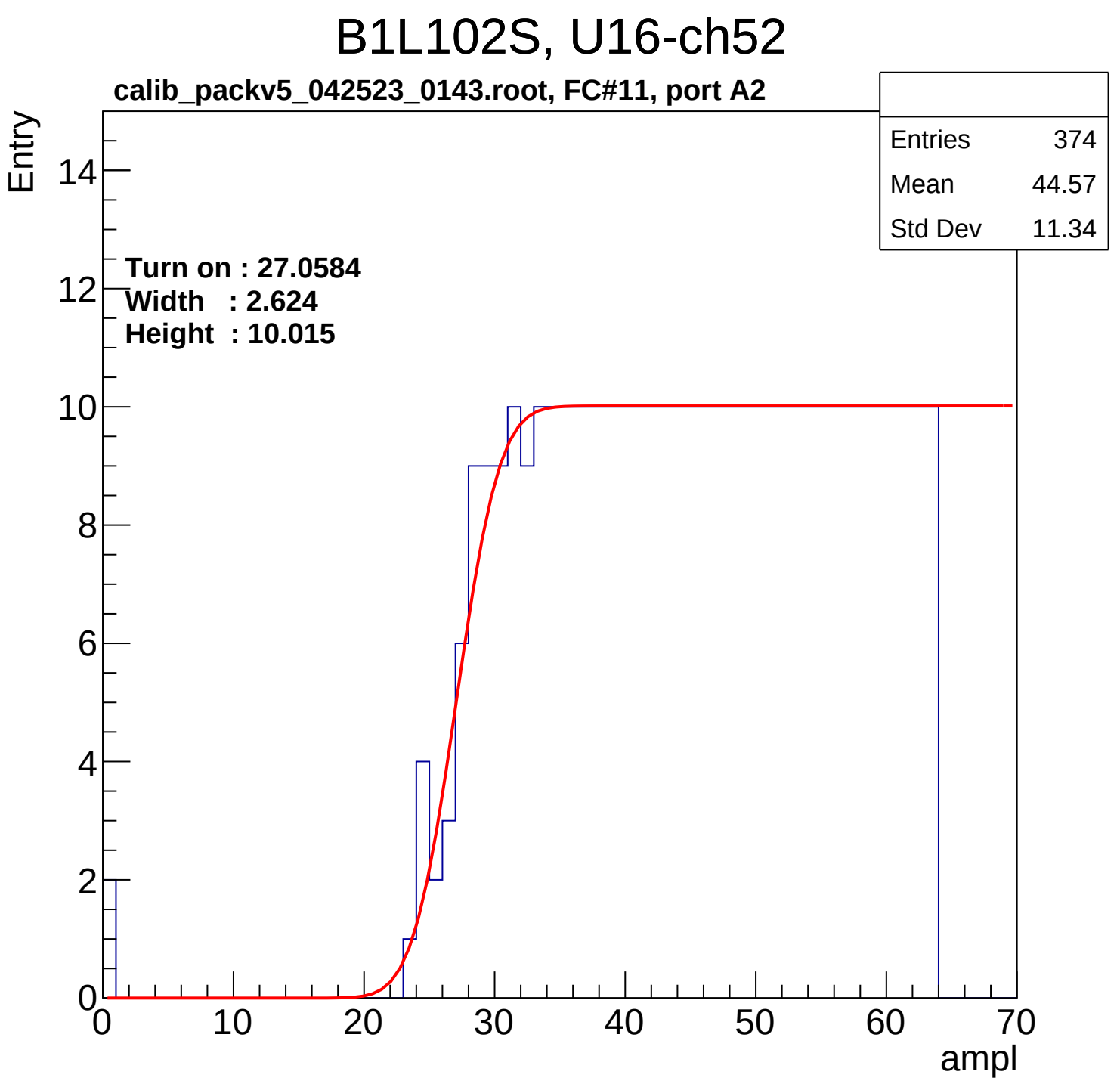

B1L102S, U16-ch47
calib_packv5_042523_0143.root, FC#11, port A2
Entries 390
Mean 43.79
Std Dev 11.67
Turn on : 25.5377
Width : 3.720
Height : 10.028
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

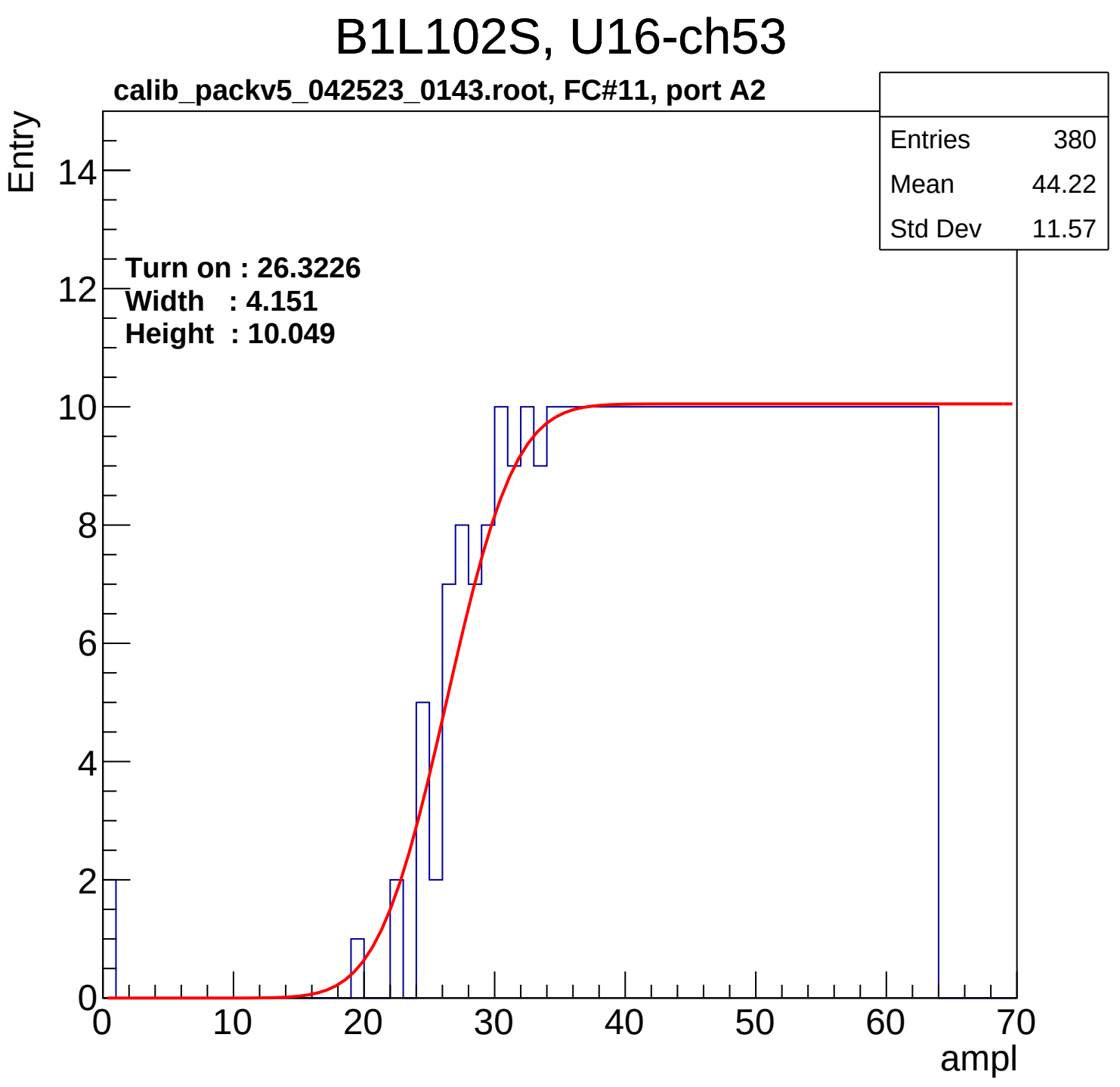

B1L102S, U16-ch48
calib_packv5_042523_0143.root, FC#11, port A2
Entries 392
Mean 43.69
Std Dev 11.79
Turn on : 25.0500
Width : 2.529
Height : 10.000
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

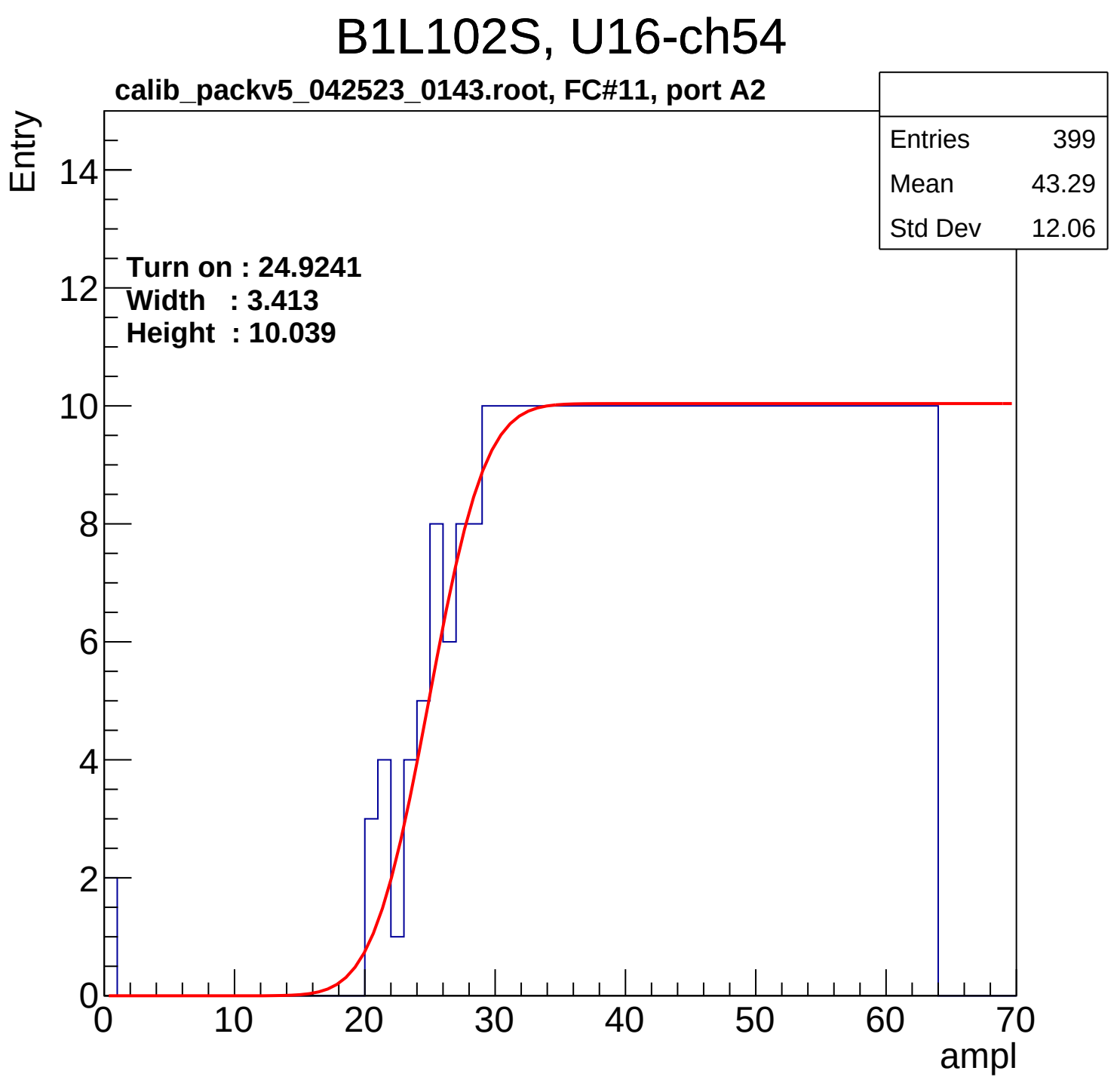

B1L102S, U16-ch49
calib_packv5_042523_0143.root, FC#11, port A2
Entries 394
Mean 43.51
Std Dev 12.03
Turn on : 24.9122
Width : 3.335
Height : 10.013
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

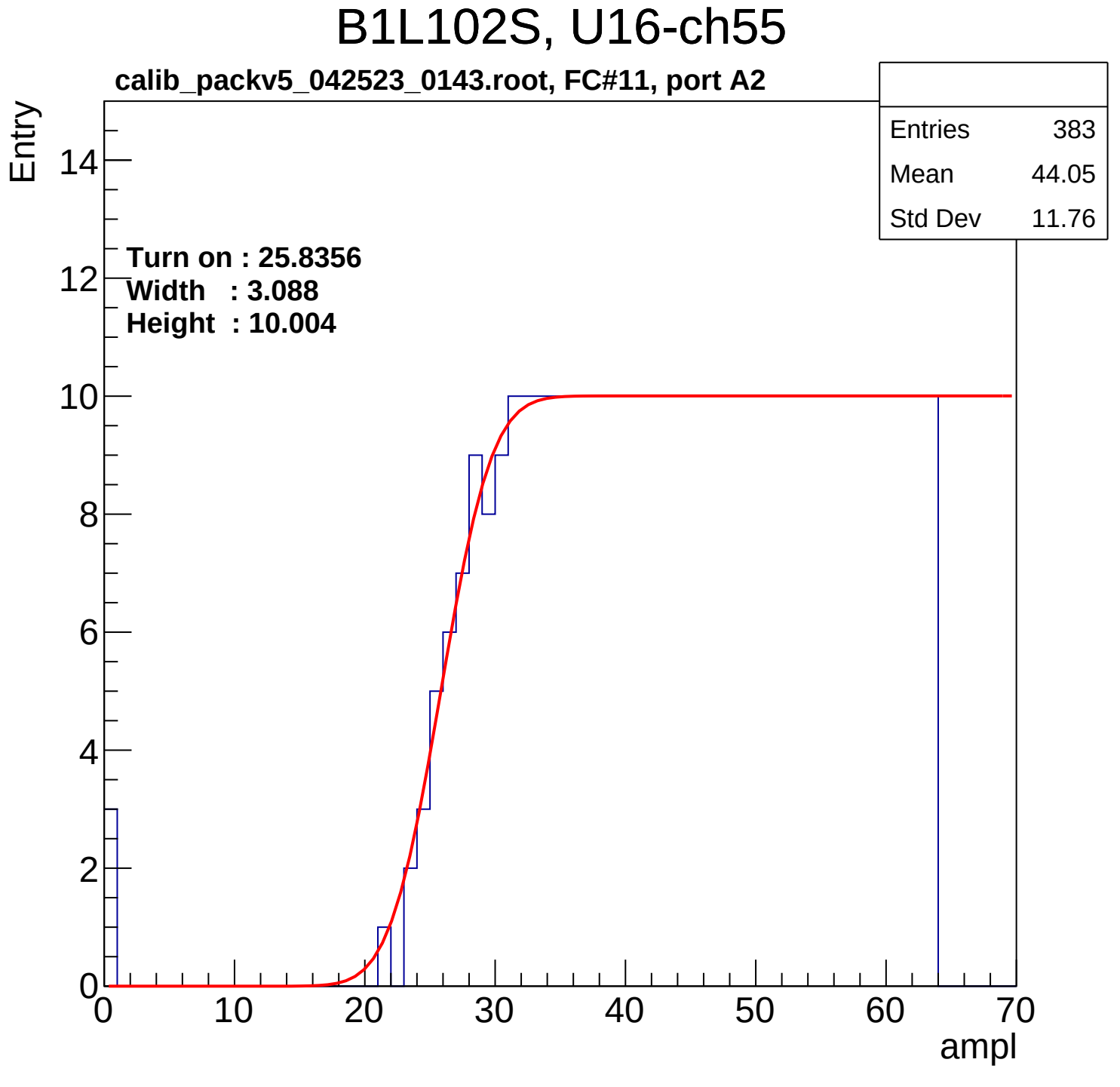

B1L102S, U16-ch50
calib_packv5_042523_0143.root, FC#11, port A2
Entries 401
Mean 42.99
Std Dev 12.66
Turn on : 24.5421
Width : 3.677
Height : 10.055
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

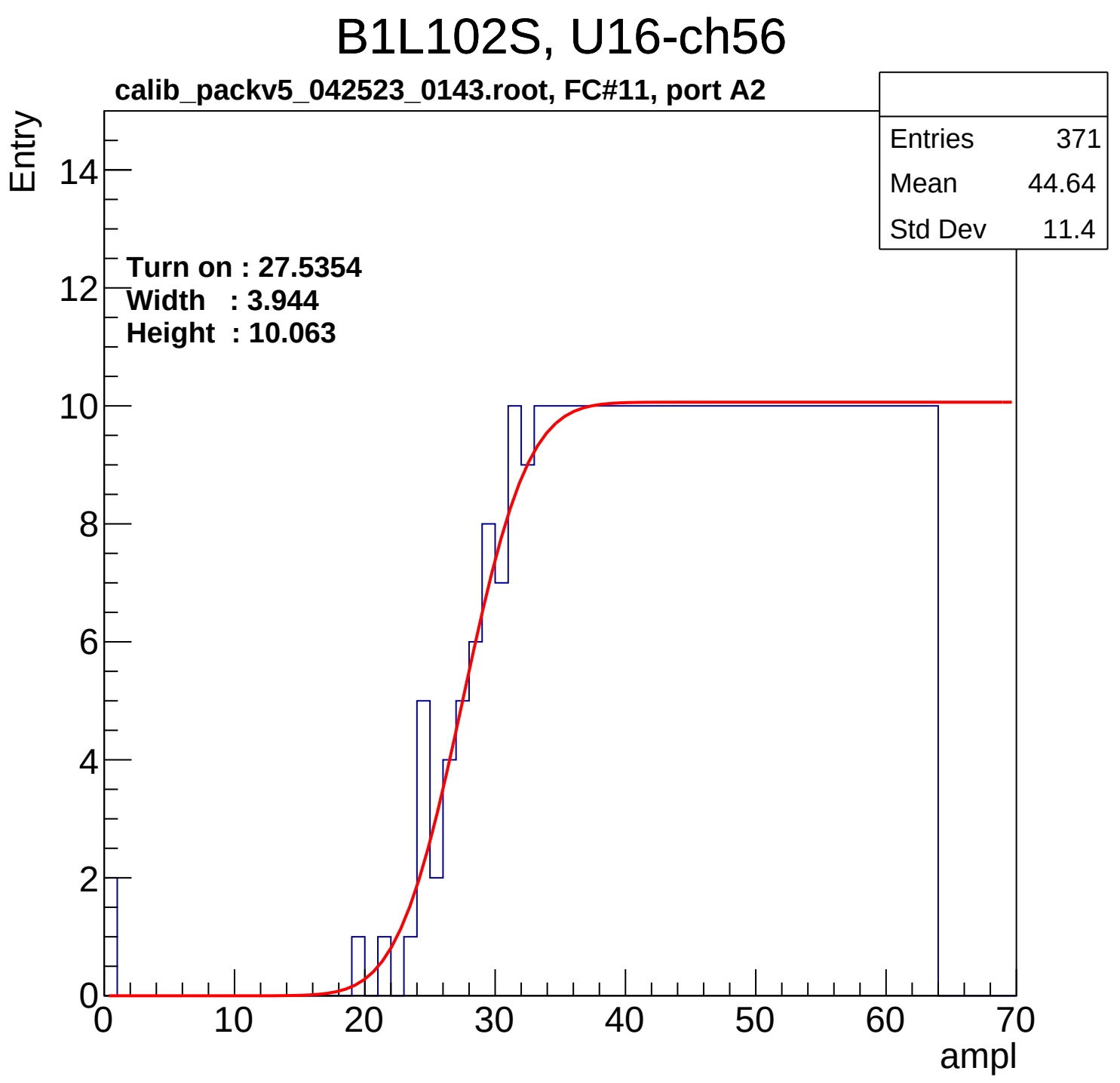

B1L102S, U16-ch51
calib_packv5_042523_0143.root, FC#11, port A2
Entries 372
Mean 44.55
Std Dev 11.57
Turn on : 27.0951
Width : 4.758
Height : 10.083
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

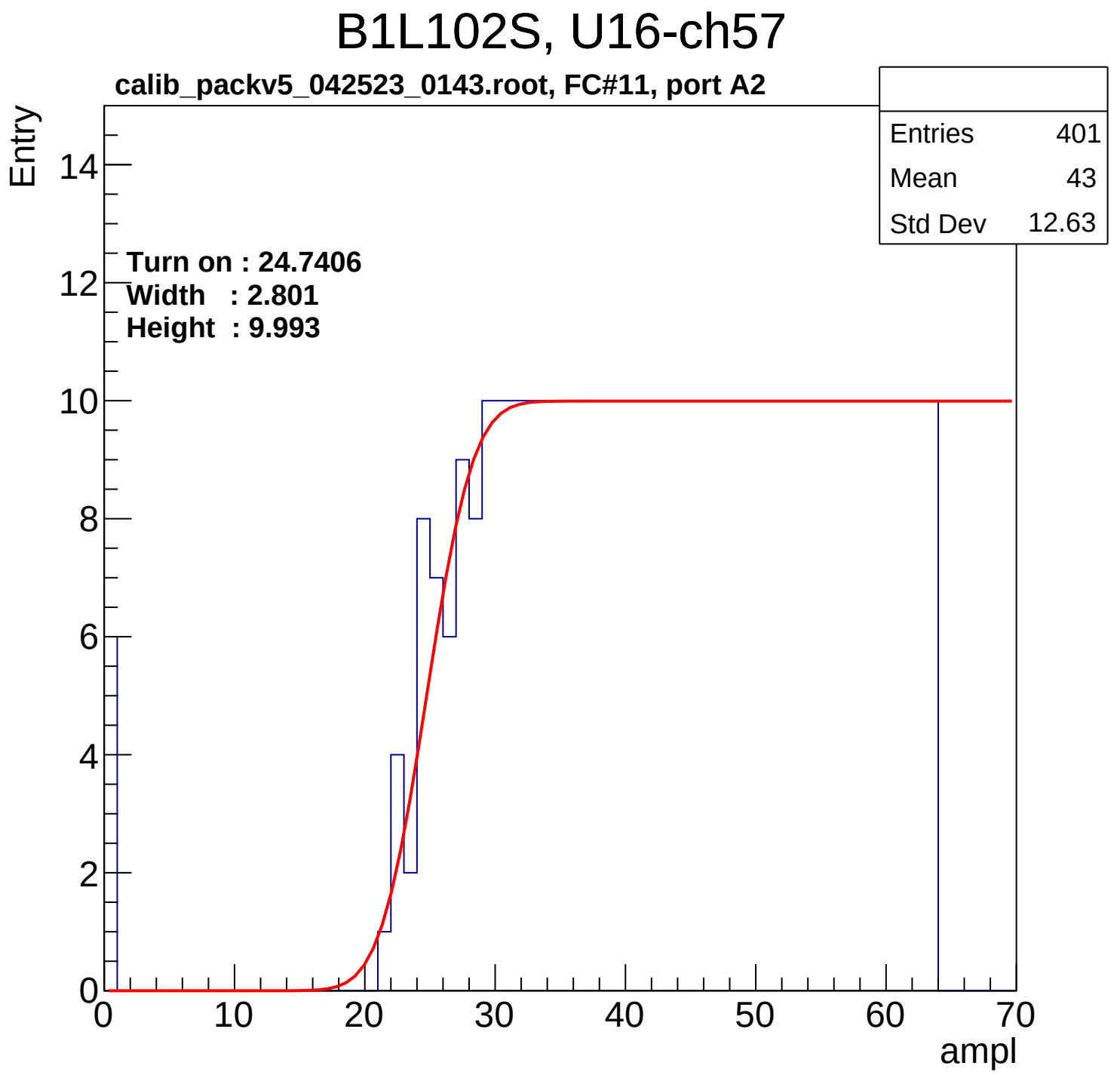

B1L102S, U16-ch52
calib_packv5_042523_0143.root, FC#11, port A2
Entries 374
Mean 44.57
Std Dev 11.34
Turn on : 27.0584
Width : 2.624
Height : 10.015
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

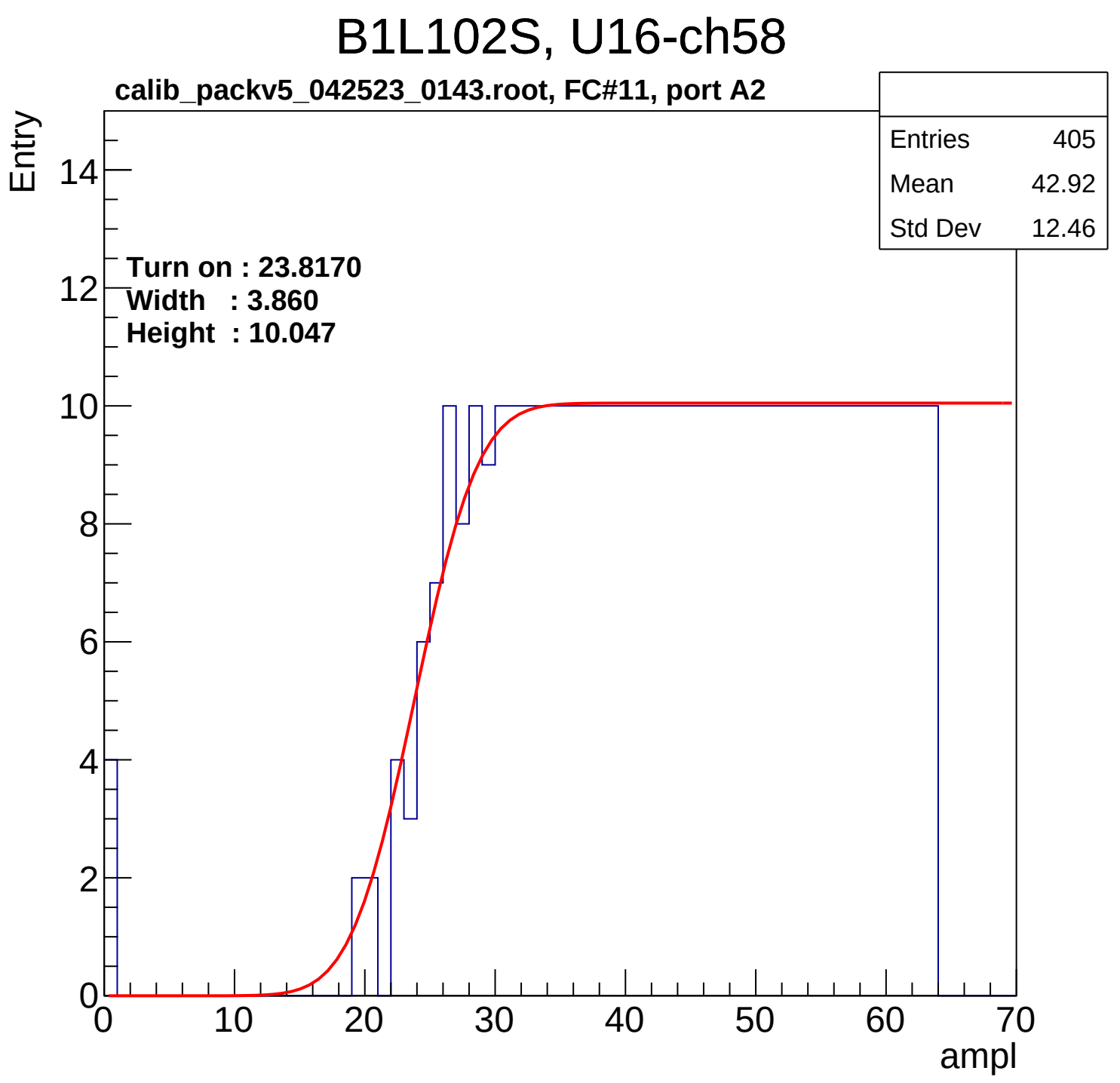

B1L102S, U16-ch53
calib_packv5_042523_0143.root, FC#11, port A2
Entries 380
Mean 44.22
Std Dev 11.57
Turn on : 26.3226
Width : 4.151
Height : 10.049
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

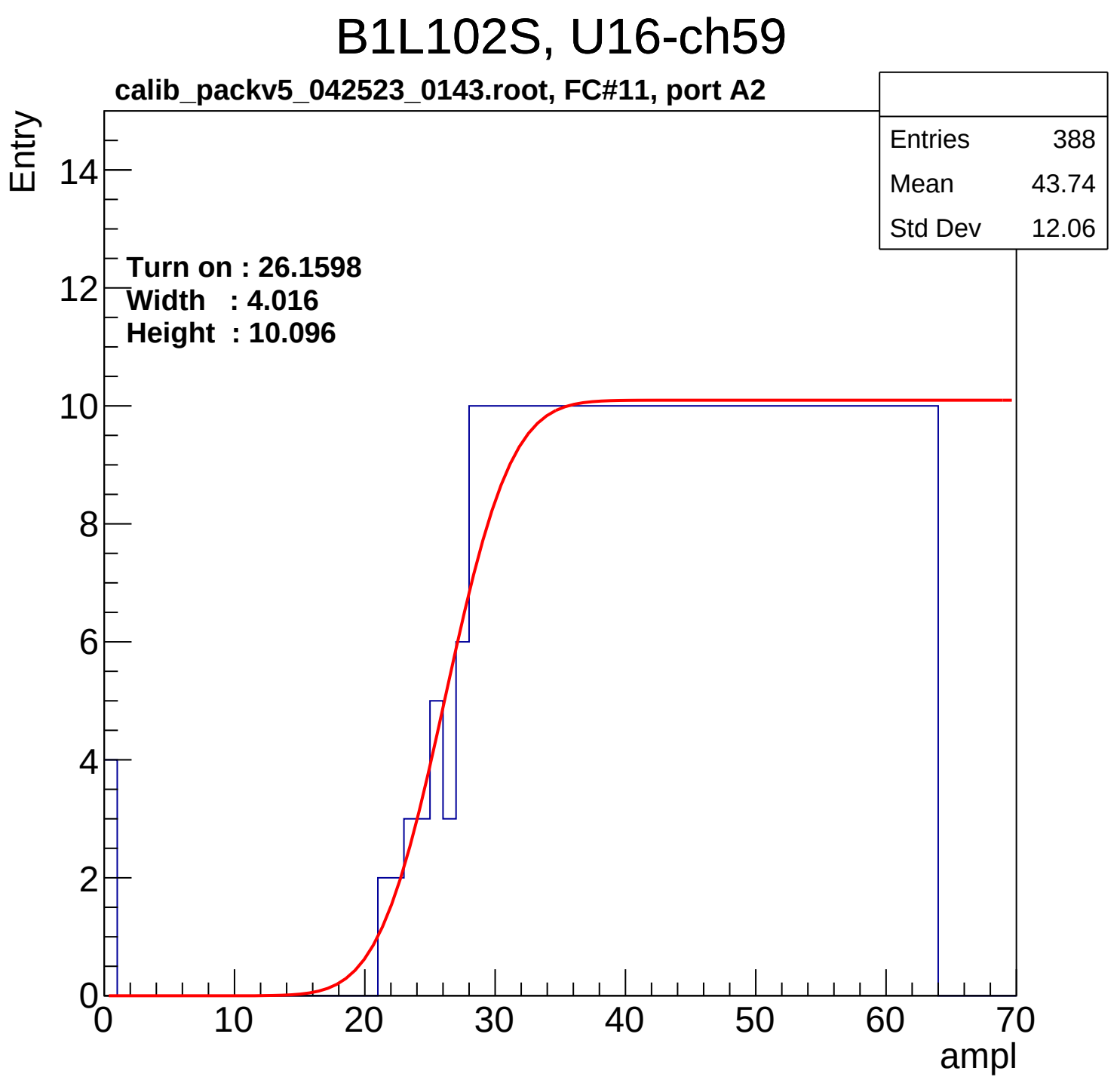

B1L102S, U16-ch54
calib_packv5_042523_0143.root, FC#11, port A2
Entries 399
Mean 43.29
Std Dev 12.06
Turn on : 24.9241
Width : 3.413
Height : 10.039
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

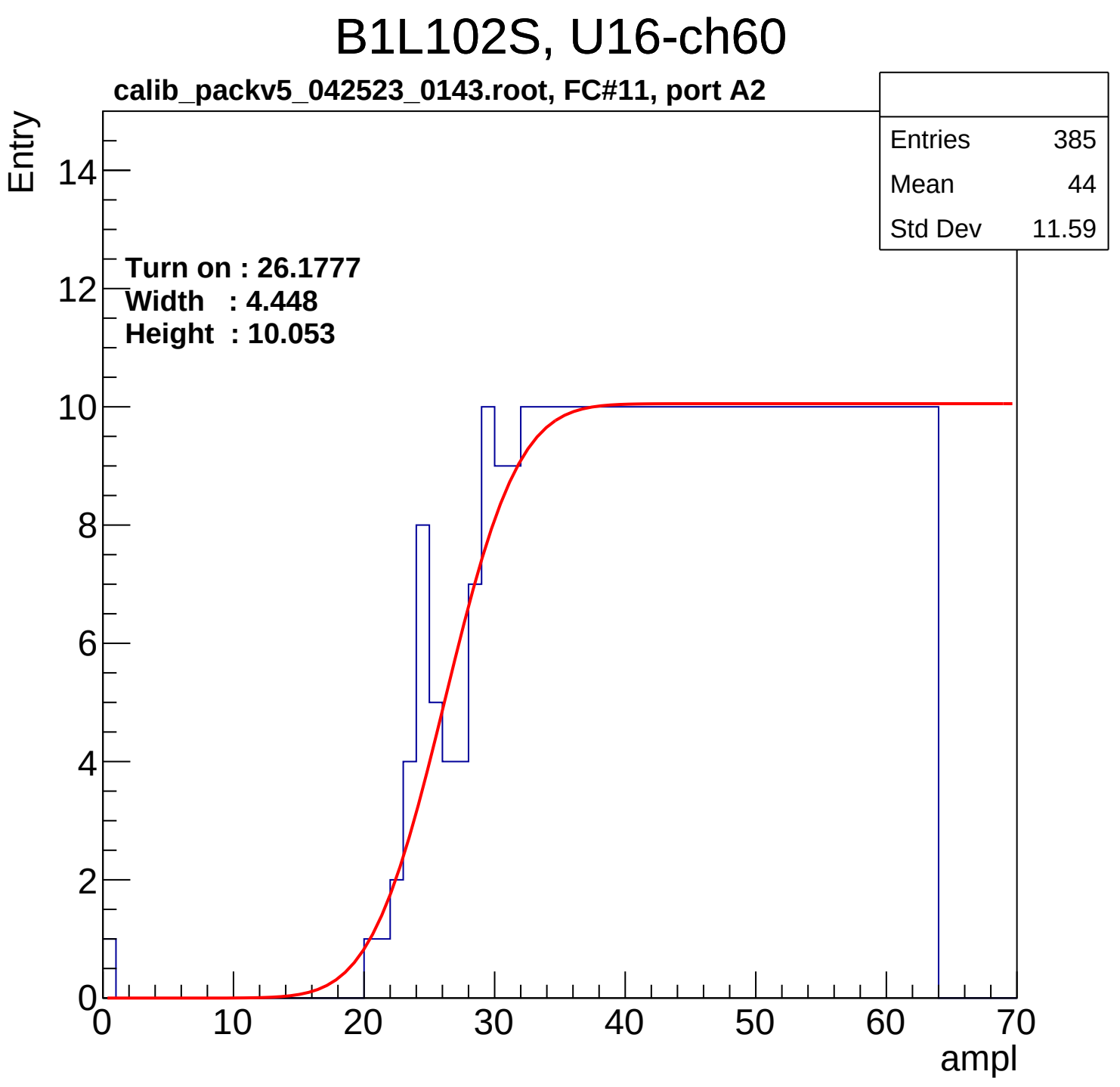

B1L102S, U16-ch55
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 44.05
Std Dev 11.76
Turn on : 25.8356
Width : 3.088
Height : 10.004
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

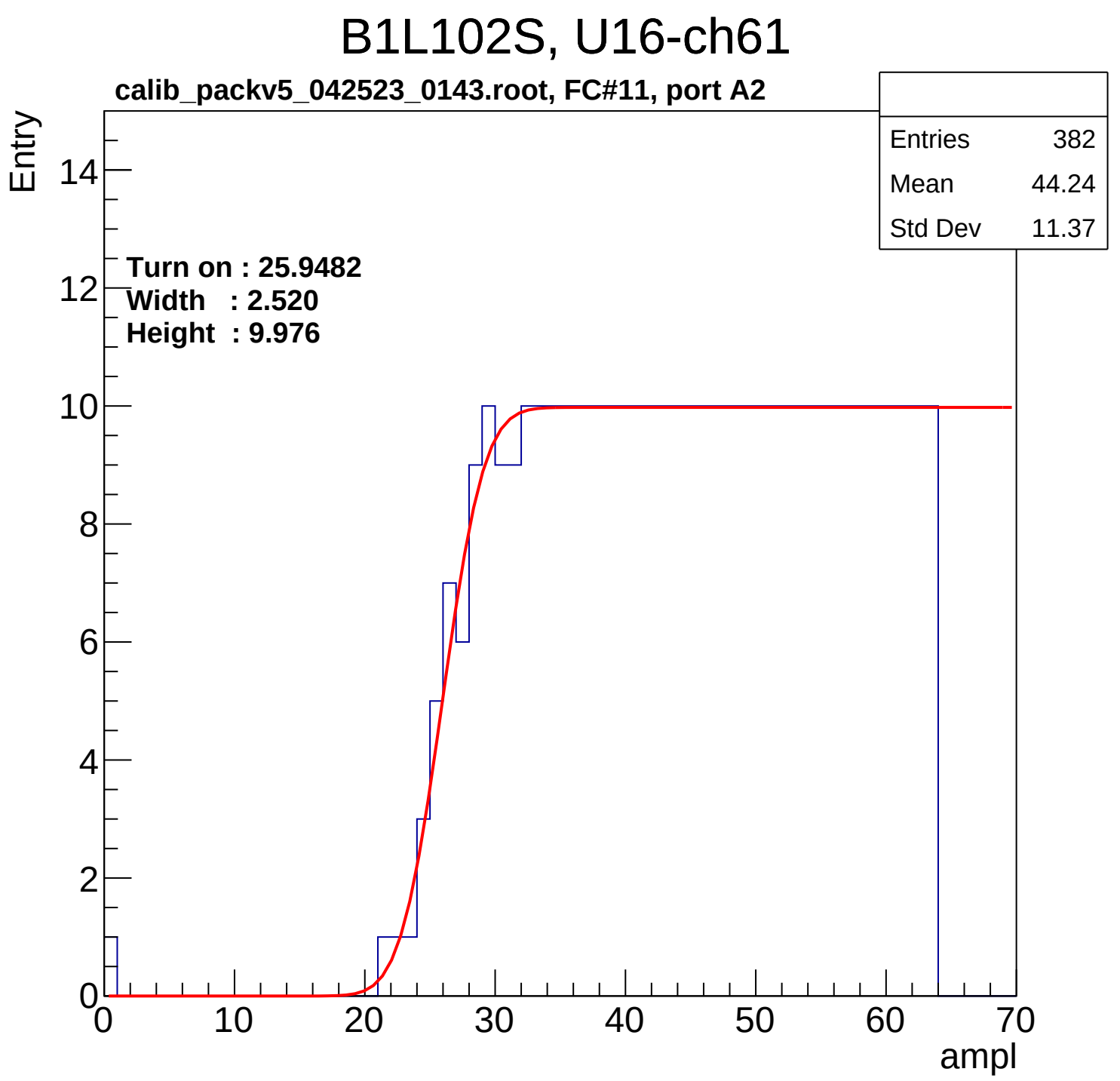

B1L102S, U16-ch56
calib_packv5_042523_0143.root, FC#11, port A2
Entries 371
Mean 44.64
Std Dev 11.4
Turn on : 27.5354
Width : 3.944
Height : 10.063
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

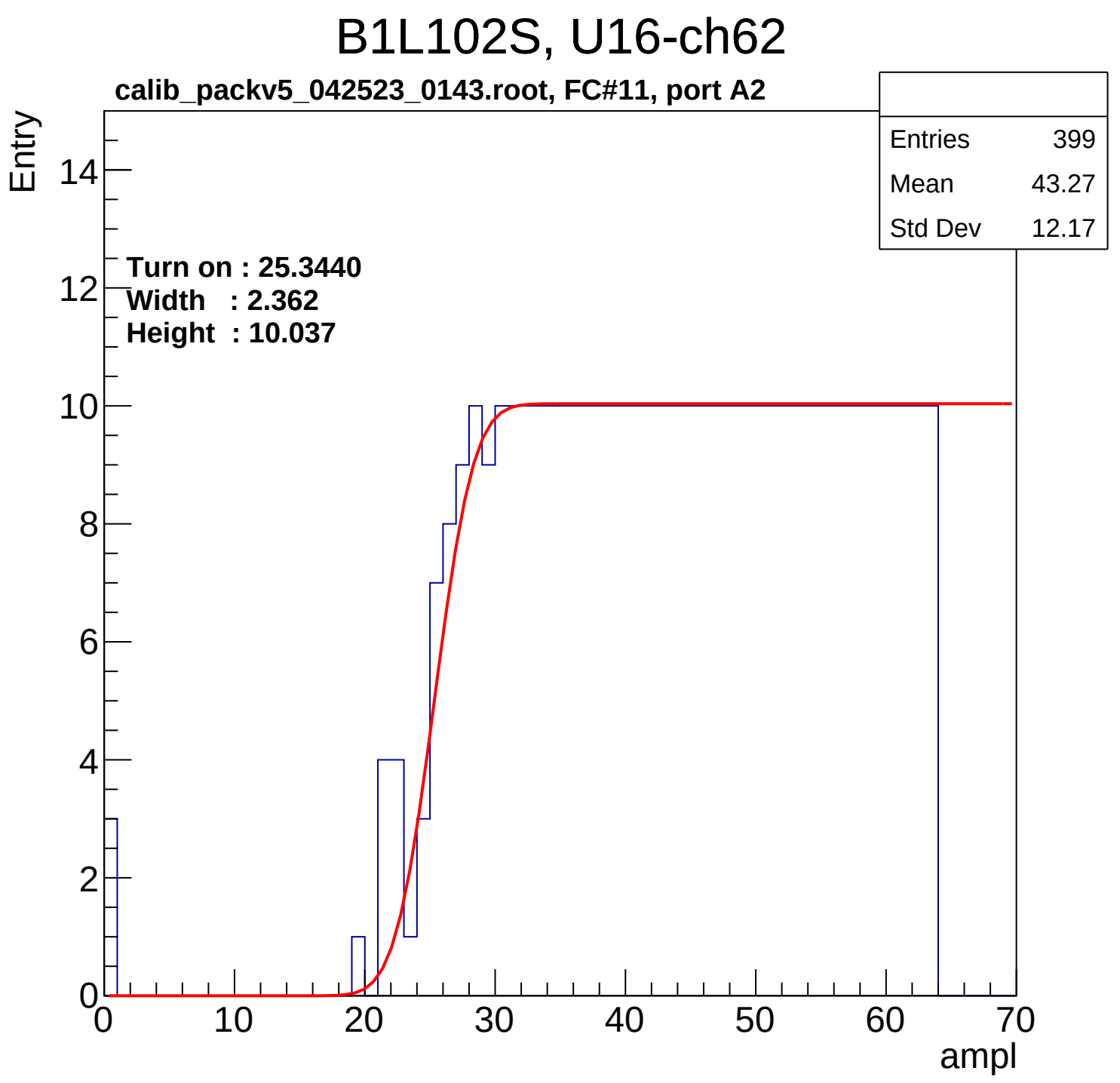

B1L102S, U16-ch57
calib_packv5_042523_0143.root, FC#11, port A2
Entries 401
Mean 43
Std Dev 12.63
Turn on : 24.7406
Width : 2.801
Height : 9.993
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

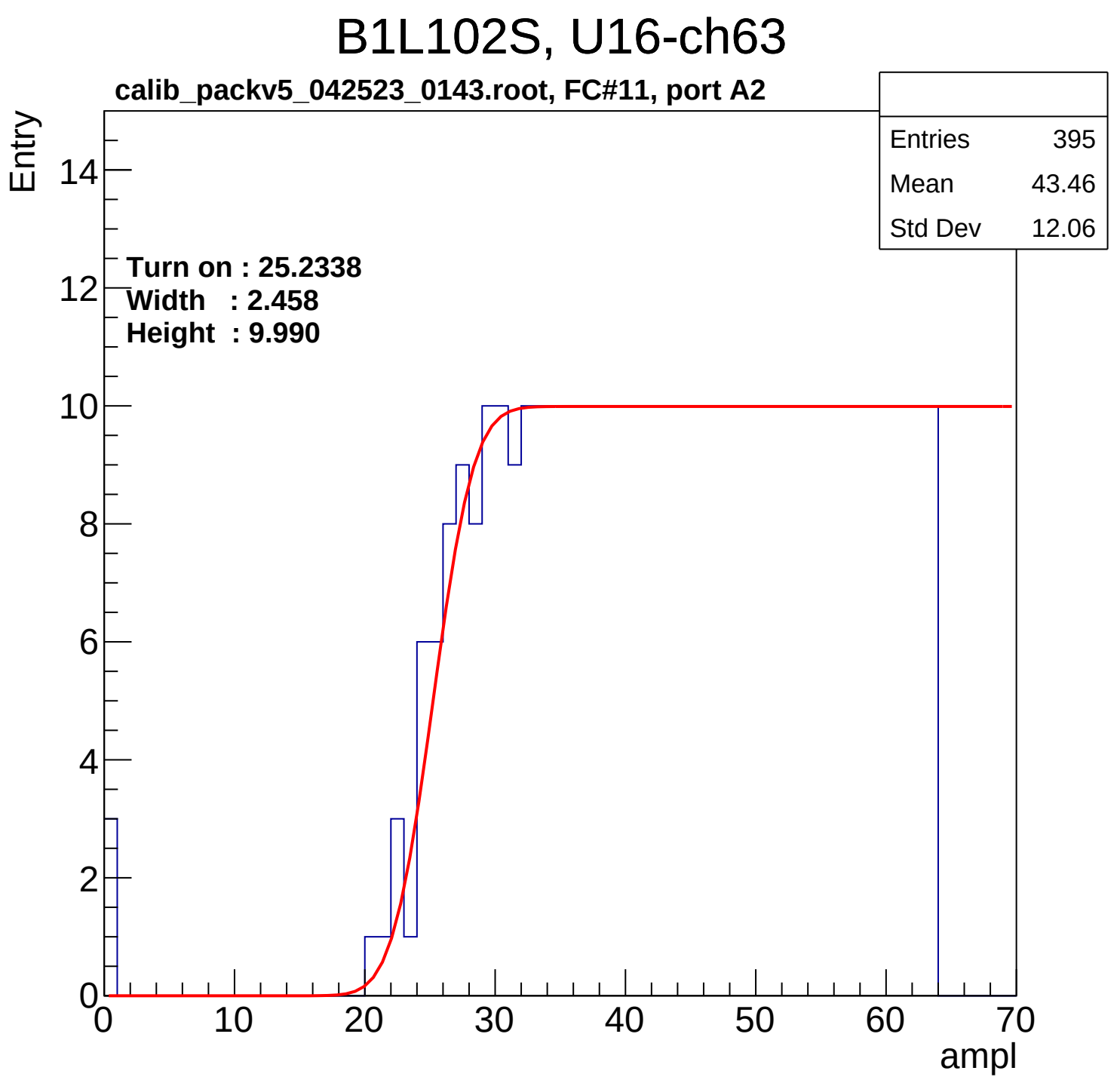

B1L102S, U16-ch58
calib_packv5_042523_0143.root, FC#11, port A2
Entries 405
Mean 42.92
Std Dev 12.46
Turn on : 23.8170
Width : 3.860
Height : 10.047
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

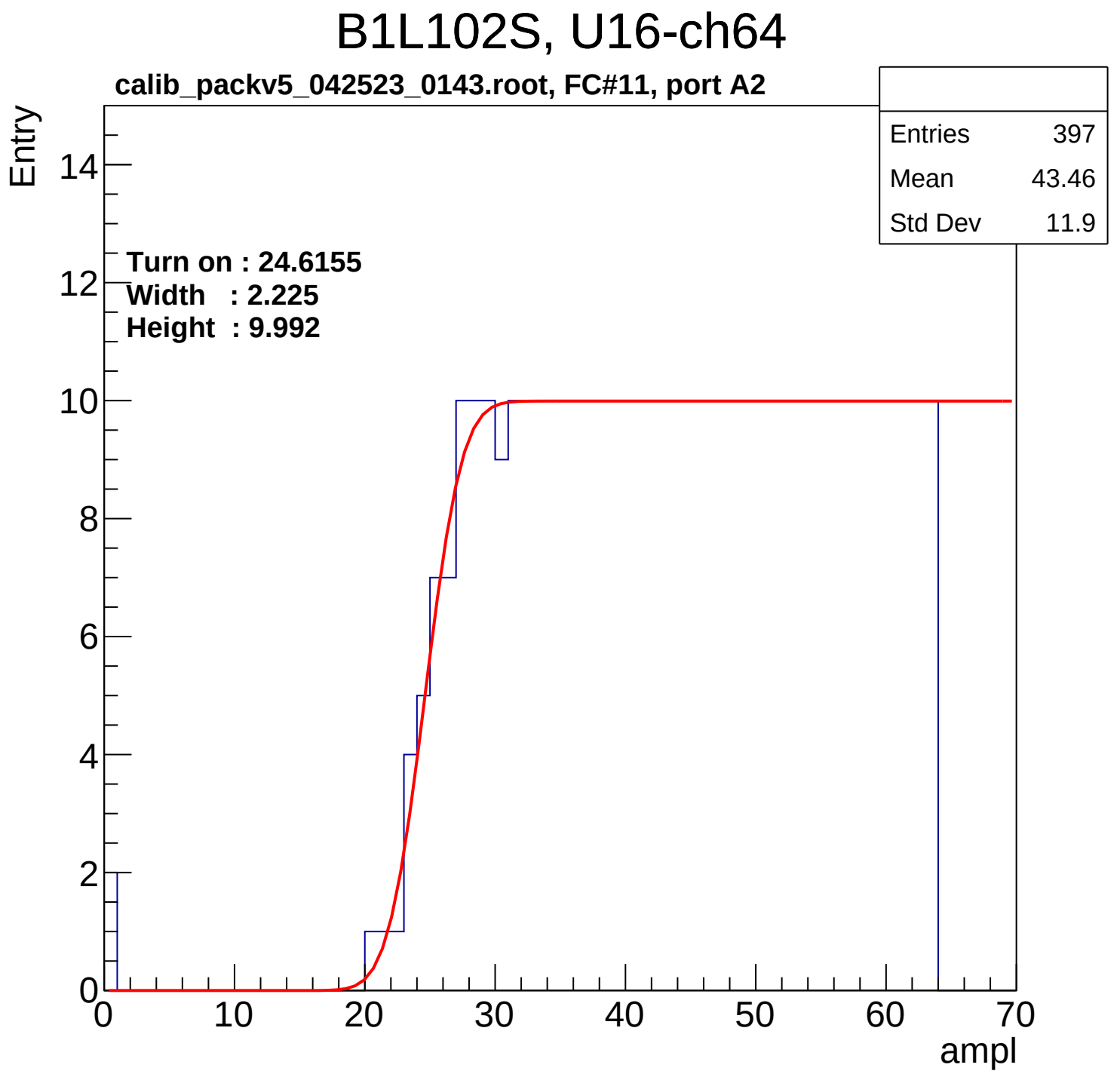

B1L102S, U16-ch59
calib_packv5_042523_0143.root, FC#11, port A2
Entries 388
Mean 43.74
Std Dev 12.06
Turn on : 26.1598
Width : 4.016
Height : 10.096
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

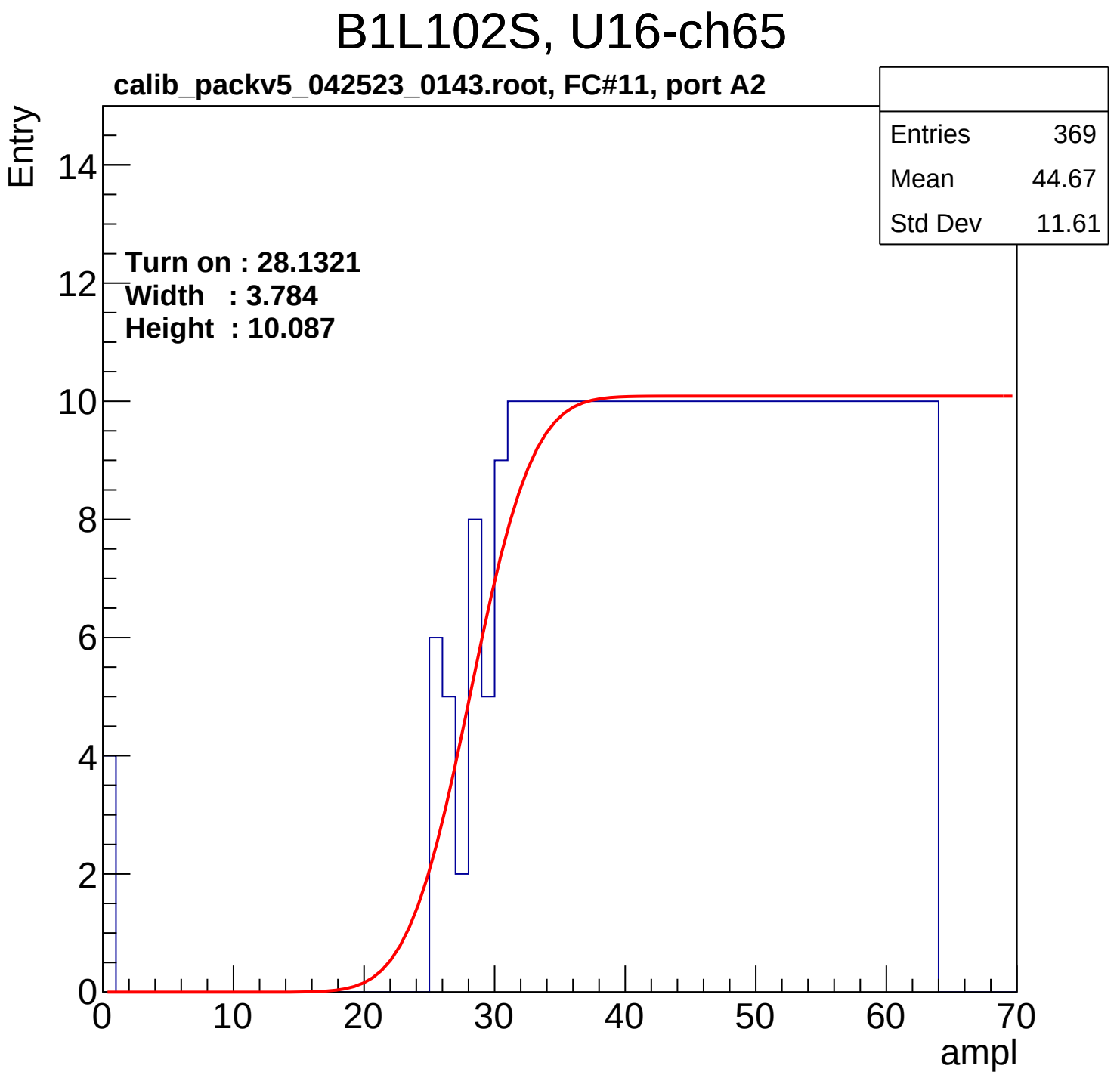

B1L102S, U16-ch60
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 44
Std Dev 11.59
Turn on : 26.1777
Width : 4.448
Height : 10.053
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

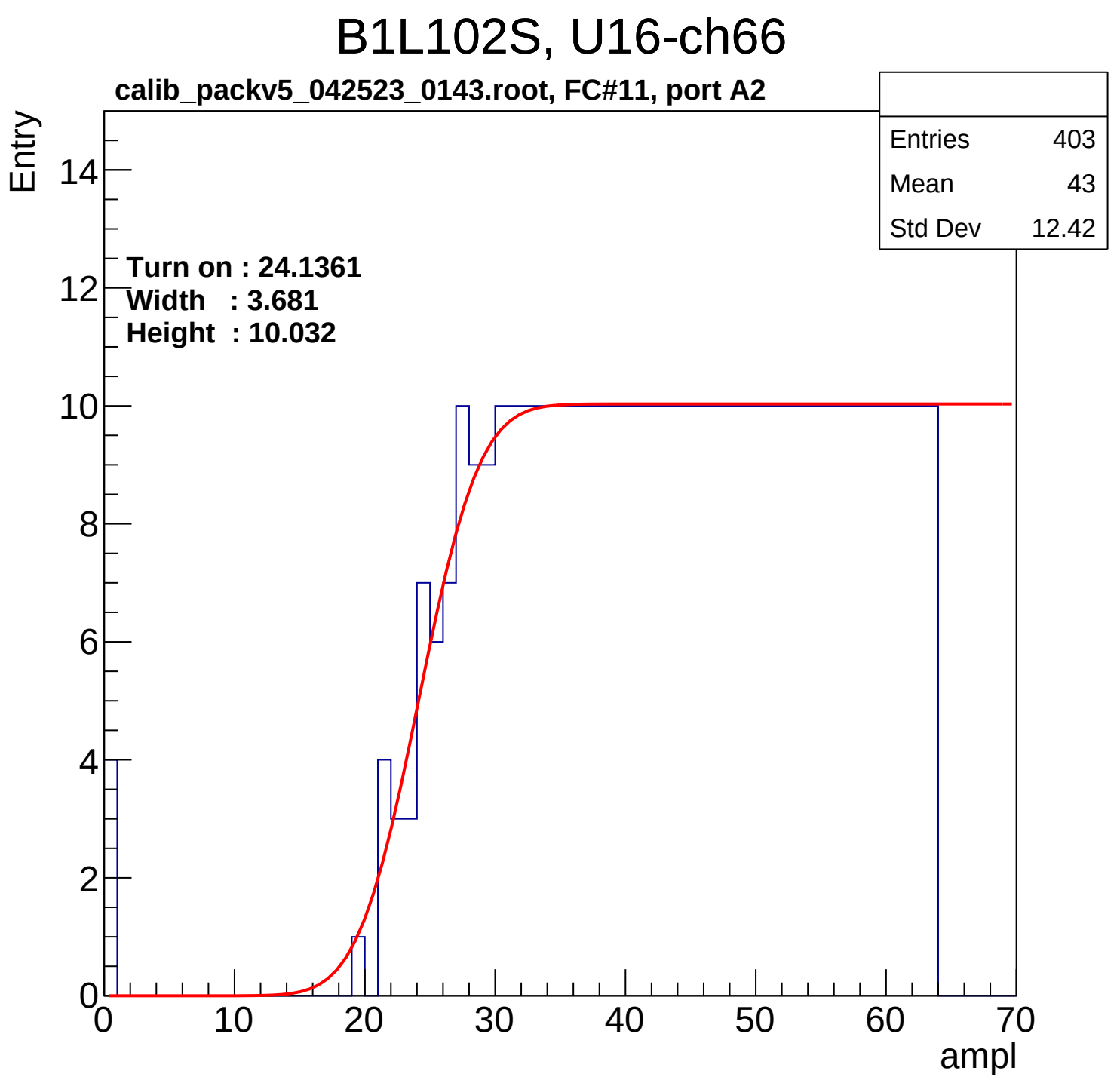

B1L102S, U16-ch61
calib_packv5_042523_0143.root, FC#11, port A2
Entries 382
Mean 44.24
Std Dev 11.37
Turn on : 25.9482
Width : 2.520
Height : 9.976
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

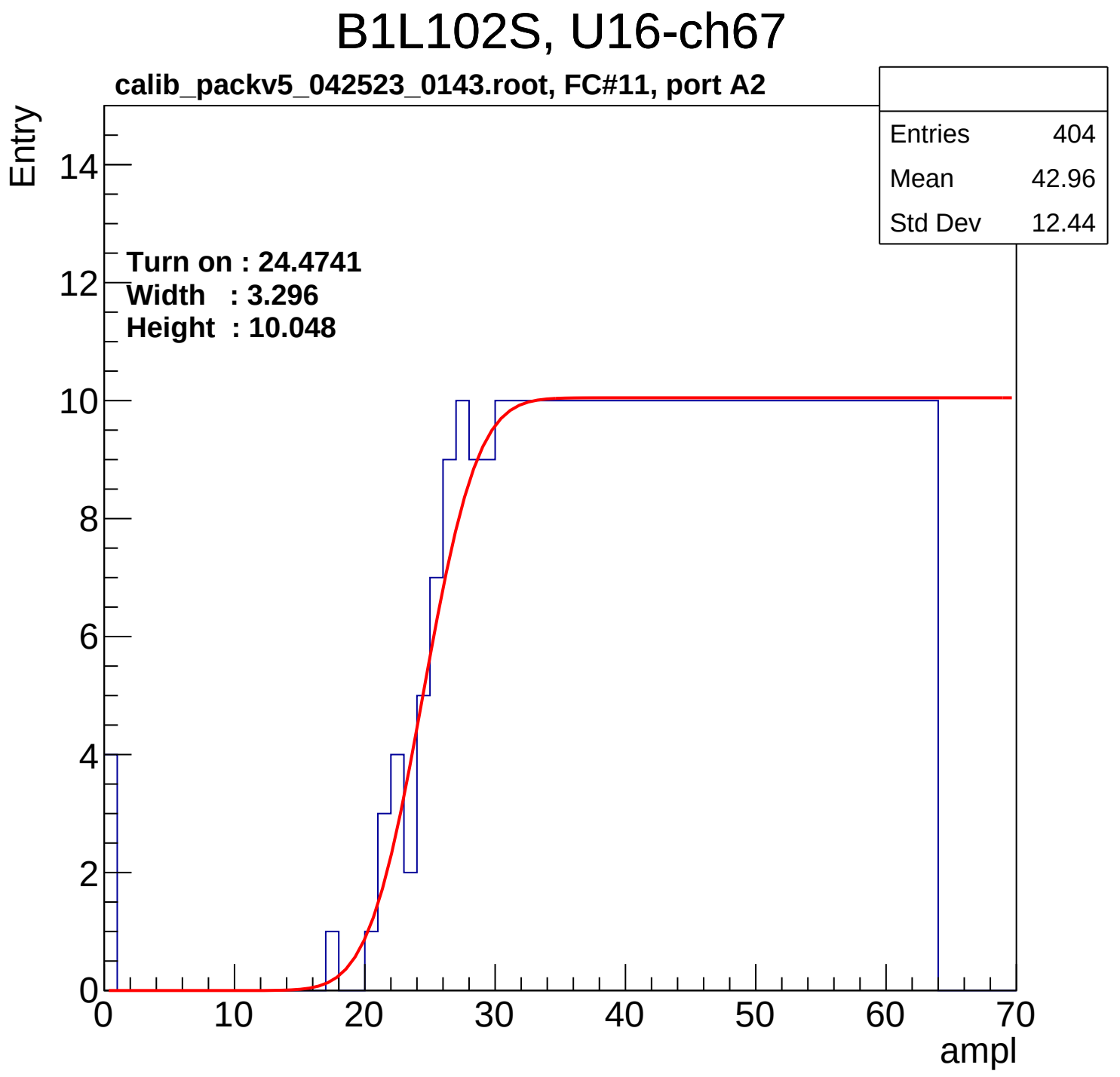

B1L102S, U16-ch62
calib_packv5_042523_0143.root, FC#11, port A2
Entries 399
Mean 43.27
Std Dev 12.17
Turn on : 25.3440
Width : 2.362
Height : 10.037
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

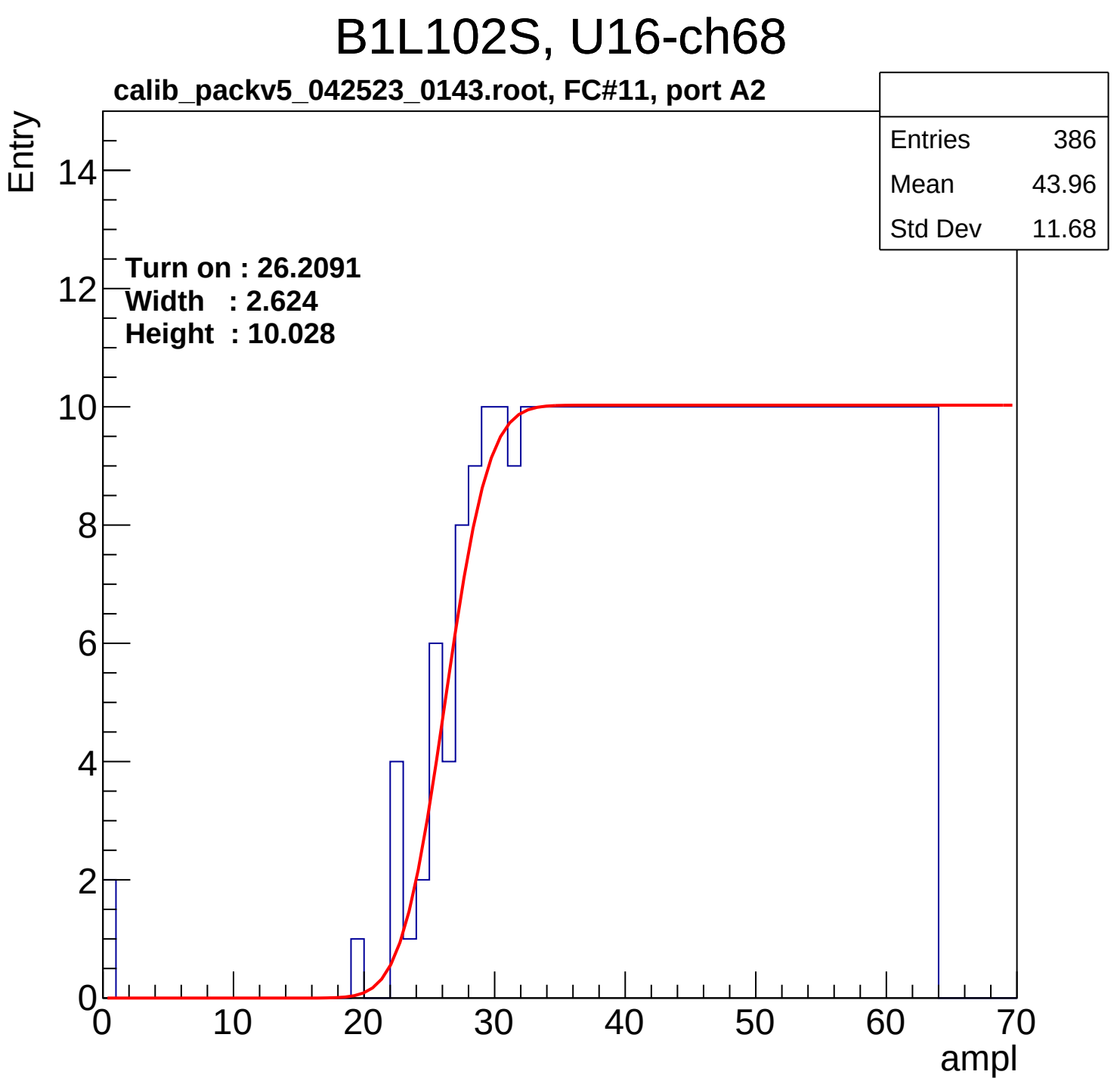

B1L102S, U16-ch63
calib_packv5_042523_0143.root, FC#11, port A2
Entries 395
Mean 43.46
Std Dev 12.06
Turn on : 25.2338
Width : 2.458
Height : 9.990
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

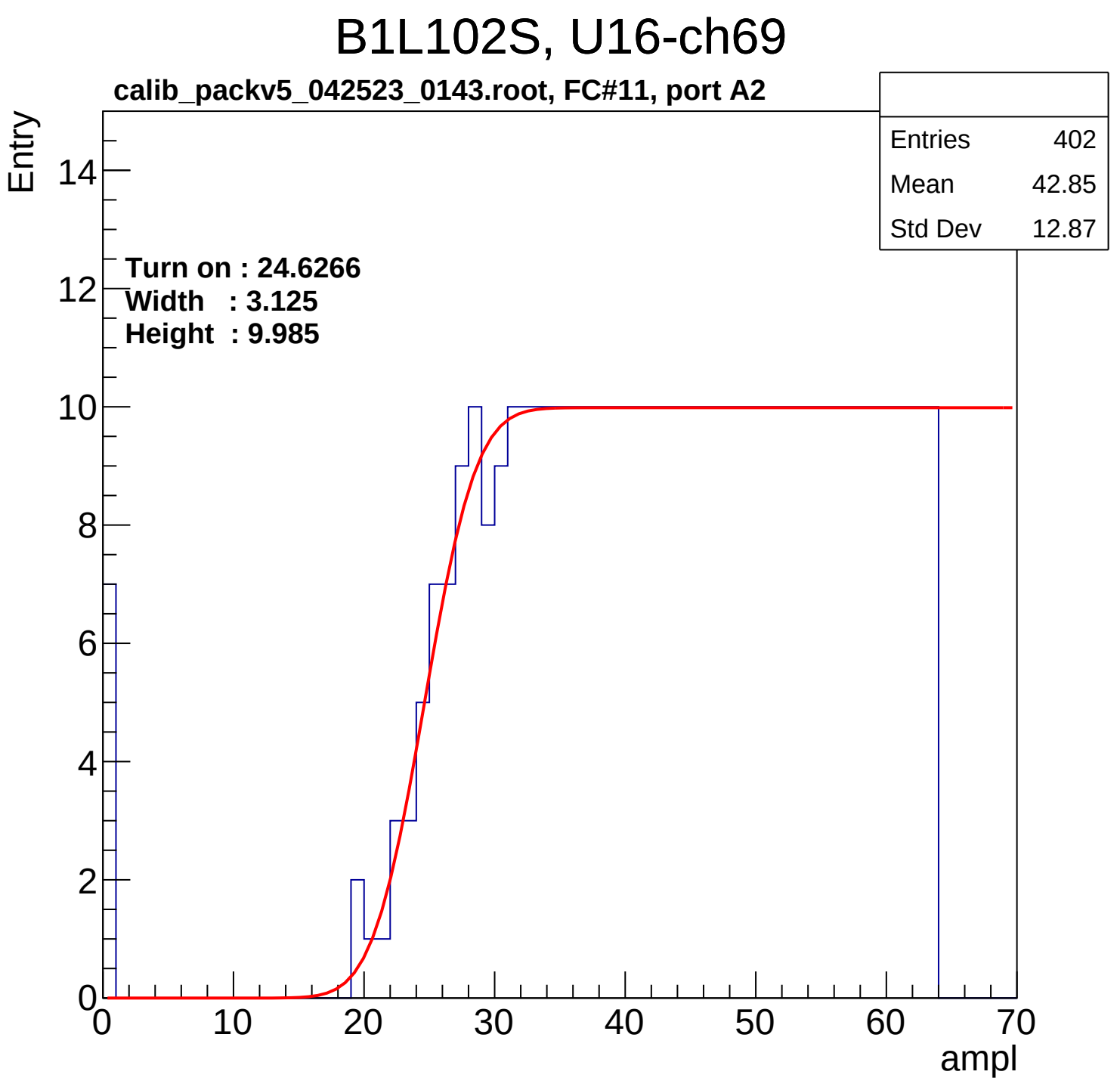

B1L102S, U16-ch64
calib_packv5_042523_0143.root, FC#11, port A2
Entries 397
Mean 43.46
Std Dev 11.9
Turn on : 24.6155
Width : 2.225
Height : 9.992
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

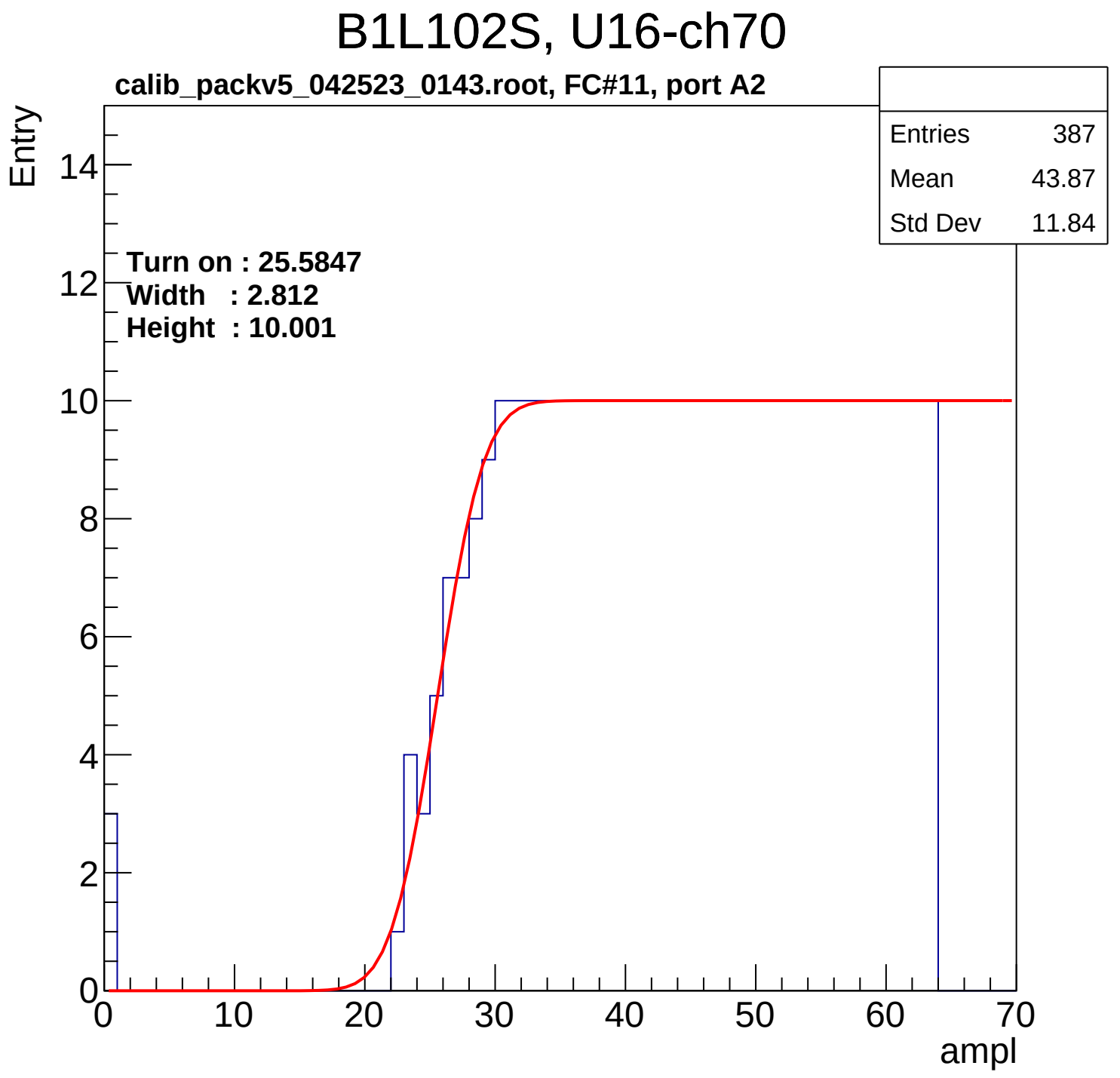

B1L102S, U16-ch65
calib_packv5_042523_0143.root, FC#11, port A2
Entries 369
Mean 44.67
Std Dev 11.61
Turn on : 28.1321
Width : 3.784
Height : 10.087
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

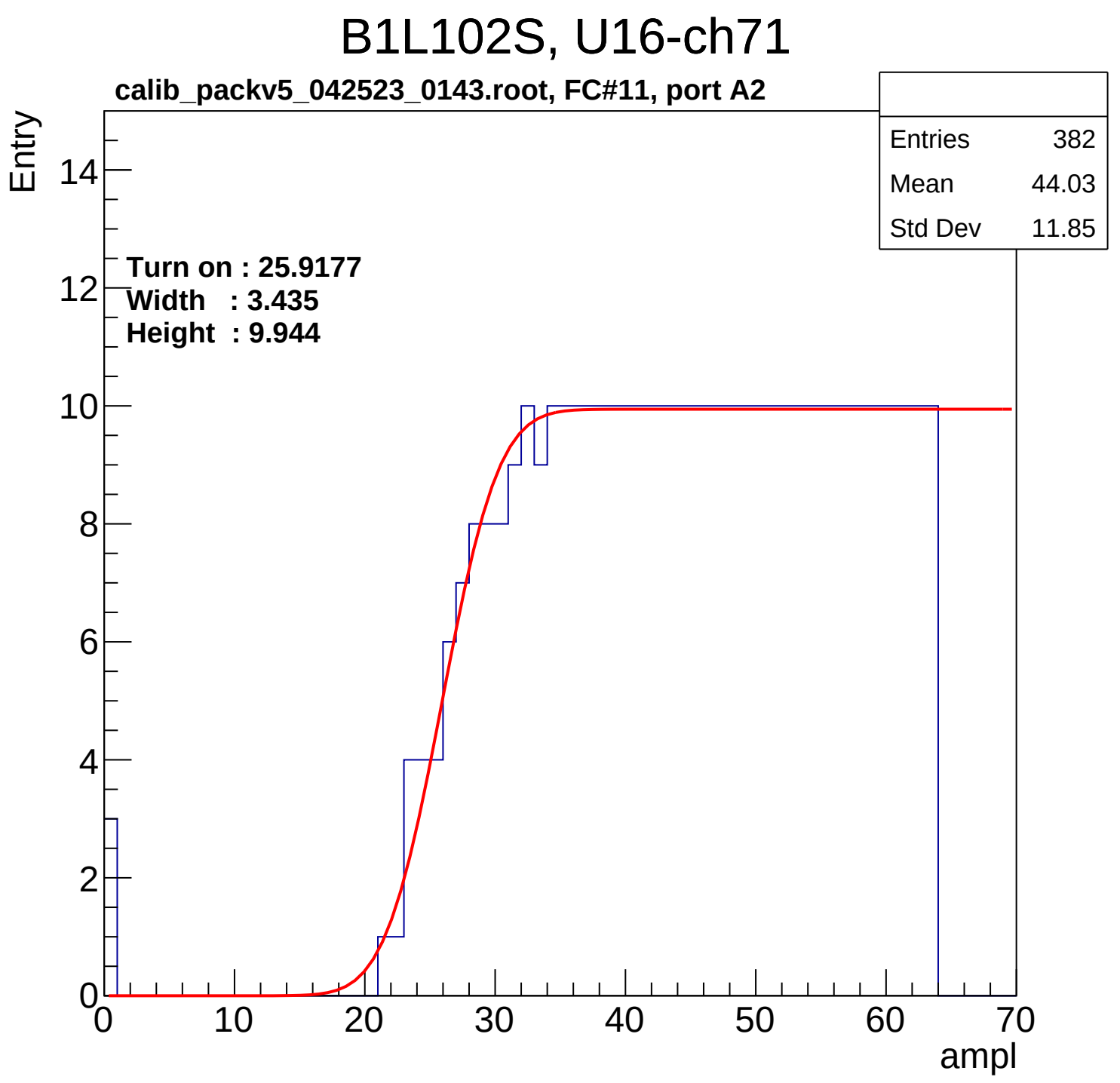

B1L102S, U16-ch66
calib_packv5_042523_0143.root, FC#11, port A2
Entries 403
Mean 43
Std Dev 12.42
Turn on : 24.1361
Width : 3.681
Height : 10.032
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

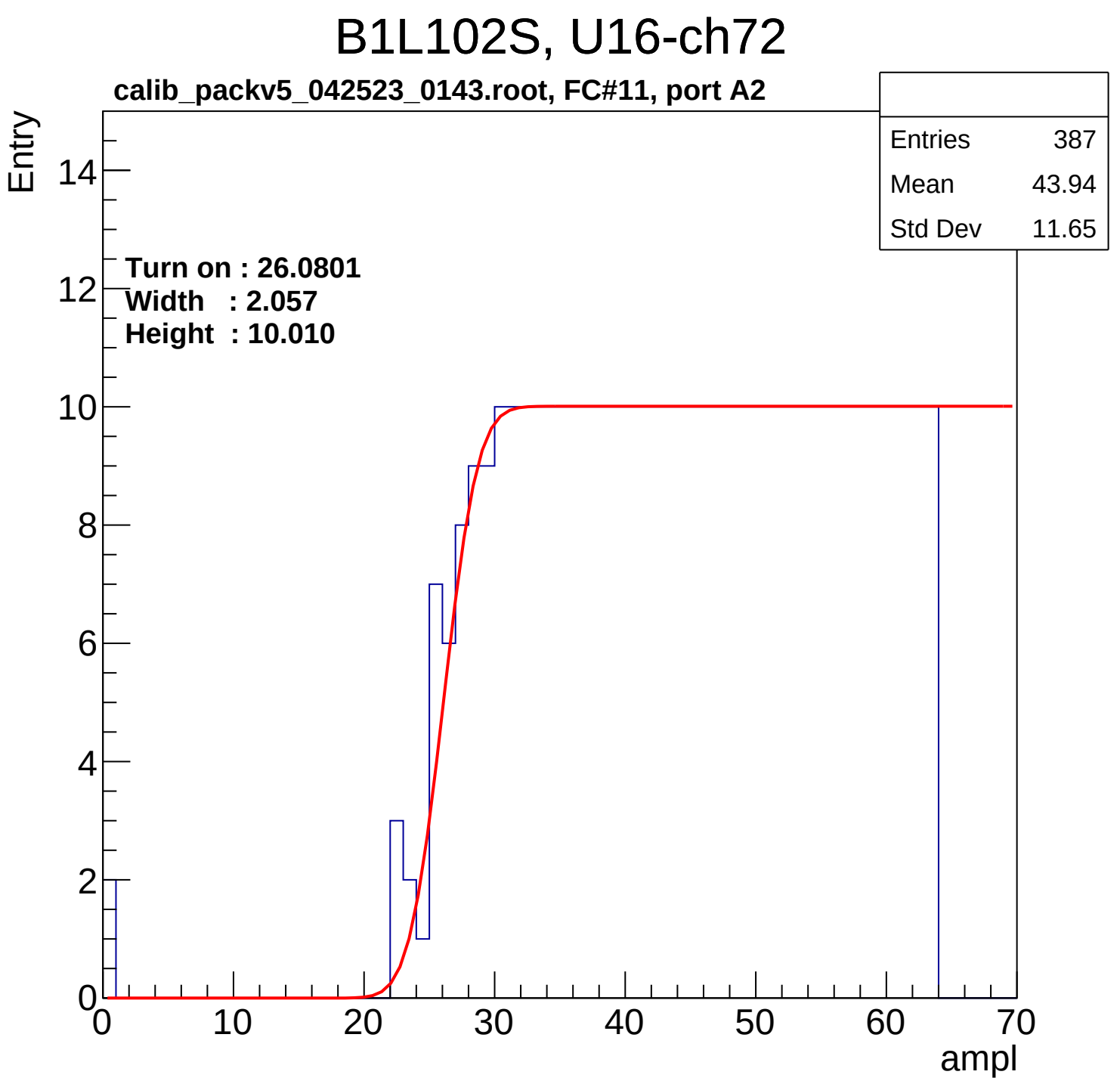

B1L102S, U16-ch67
calib_packv5_042523_0143.root, FC#11, port A2
Entries 404
Mean 42.96
Std Dev 12.44
Turn on : 24.4741
Width : 3.296
Height : 10.048
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

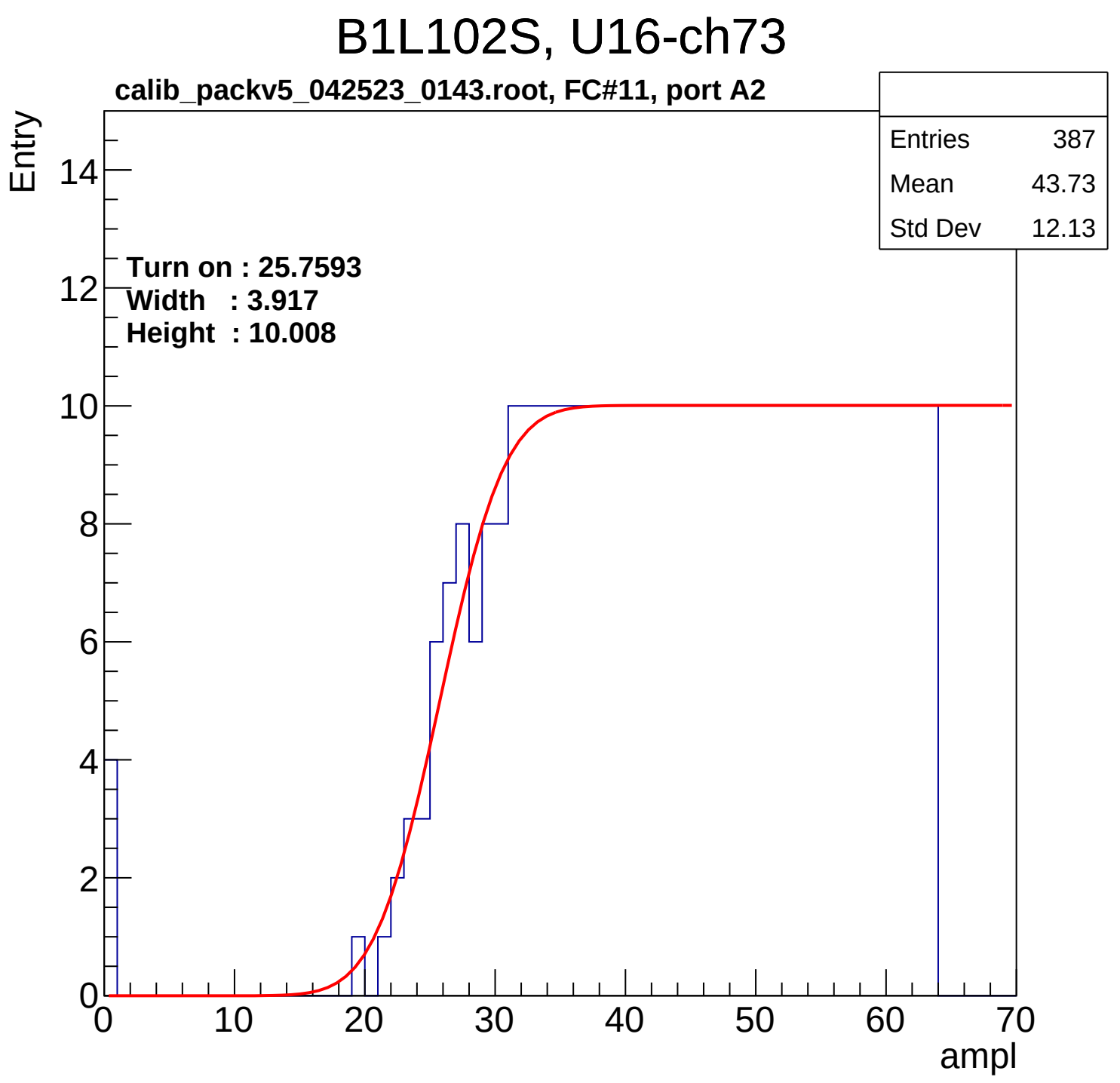

B1L102S, U16-ch68
calib_packv5_042523_0143.root, FC#11, port A2
Entries 386
Mean 43.96
Std Dev 11.68
Turn on : 26.2091
Width : 2.624
Height : 10.028
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

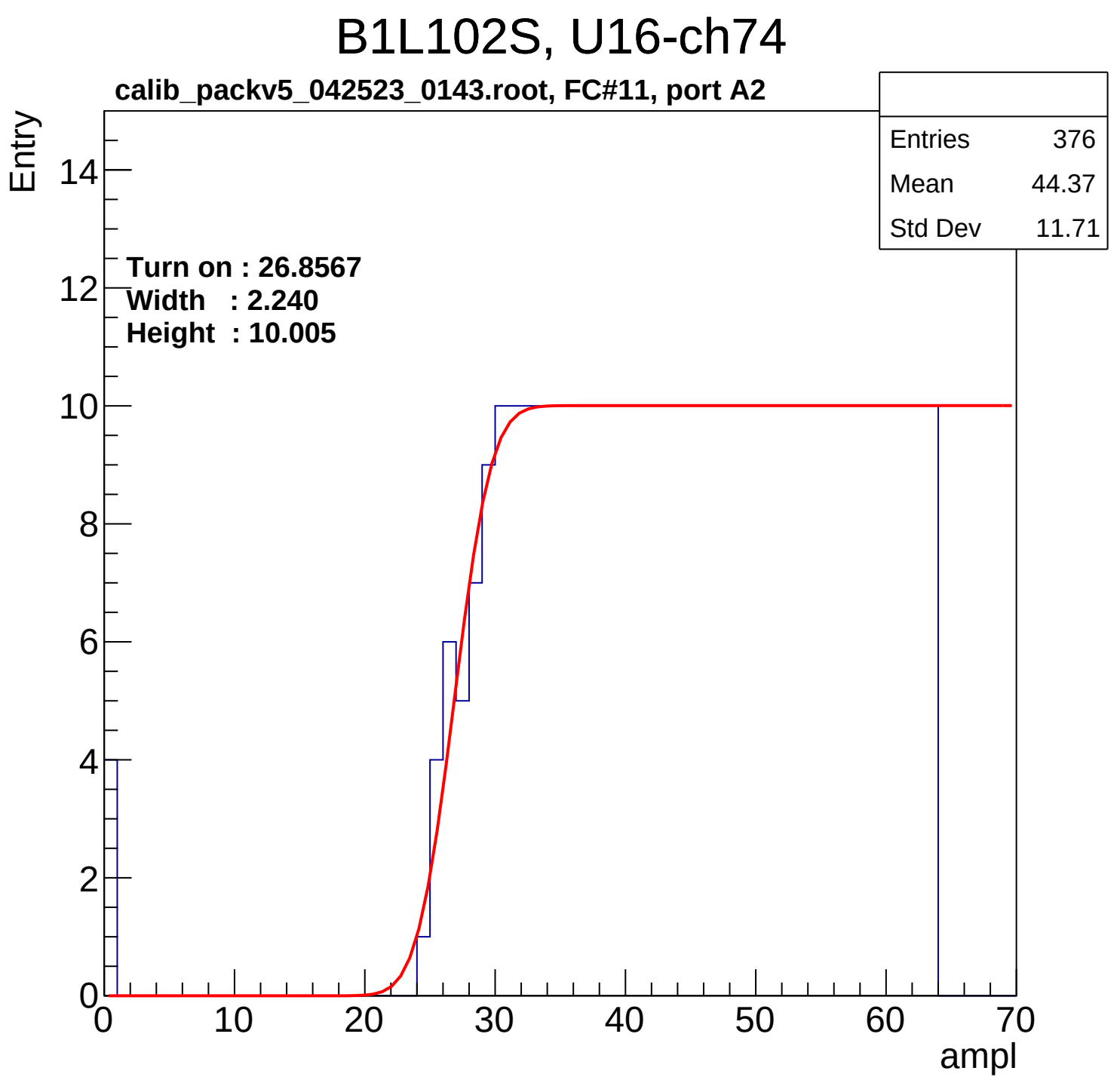

B1L102S, U16-ch69
calib_packv5_042523_0143.root, FC#11, port A2
Entries 402
Mean 42.85
Std Dev 12.87
Turn on : 24.6266
Width : 3.125
Height : 9.985
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

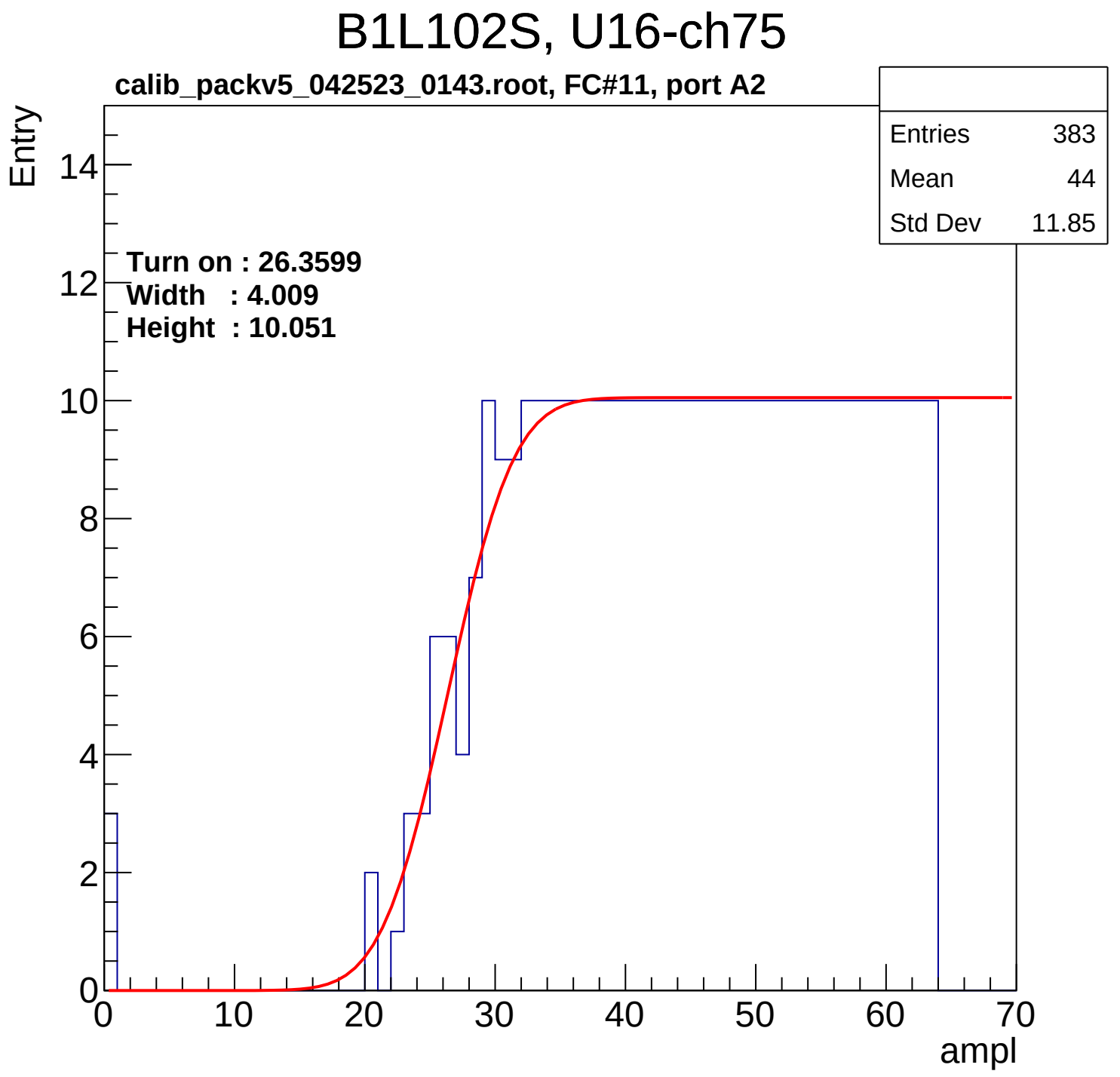

B1L102S, U16-ch70
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 43.87
Std Dev 11.84
Turn on : 25.5847
Width : 2.812
Height : 10.001
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

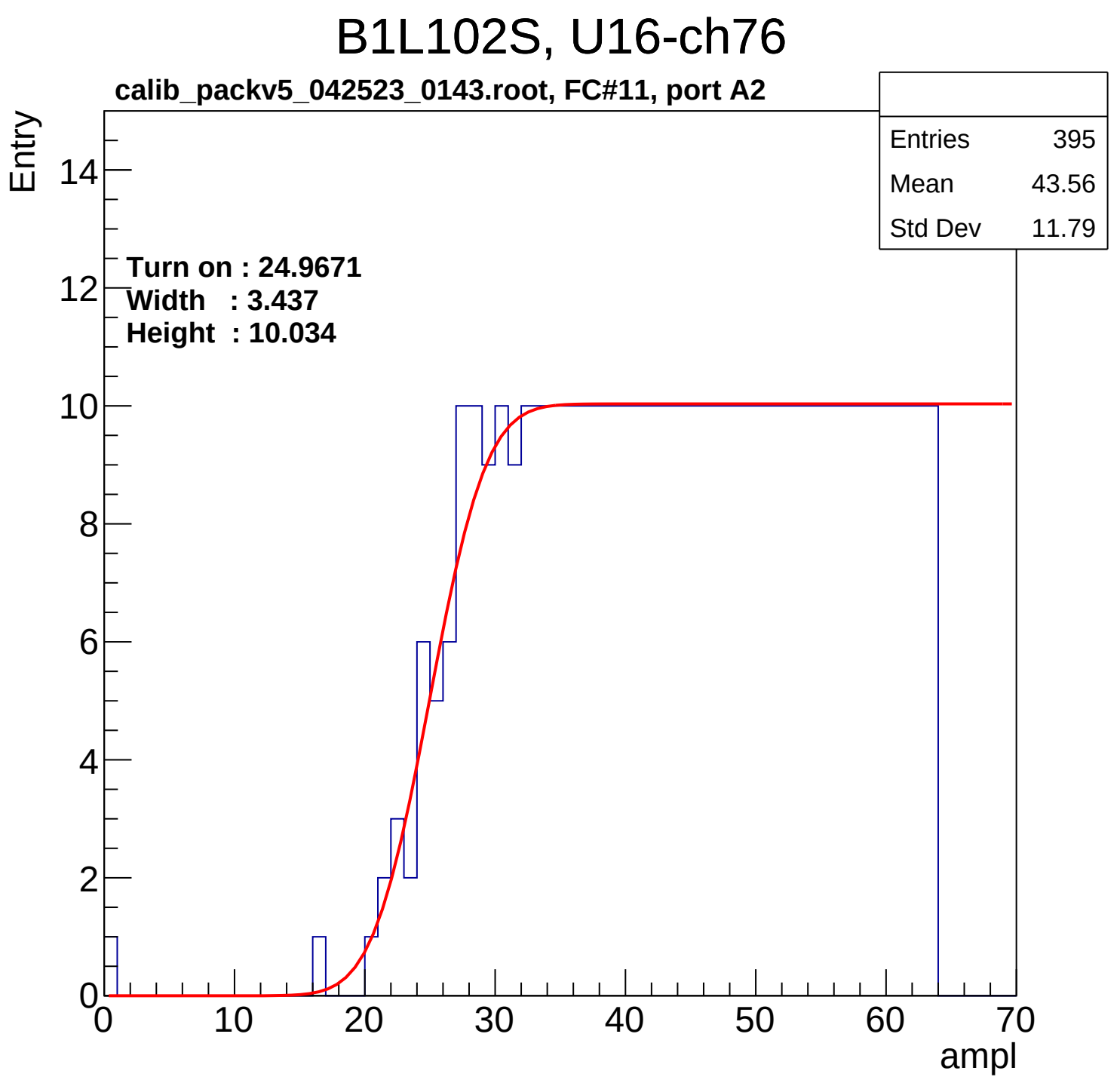

B1L102S, U16-ch71
calib_packv5_042523_0143.root, FC#11, port A2
Entries 382
Mean 44.03
Std Dev 11.85
Turn on : 25.9177
Width : 3.435
Height : 9.944
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

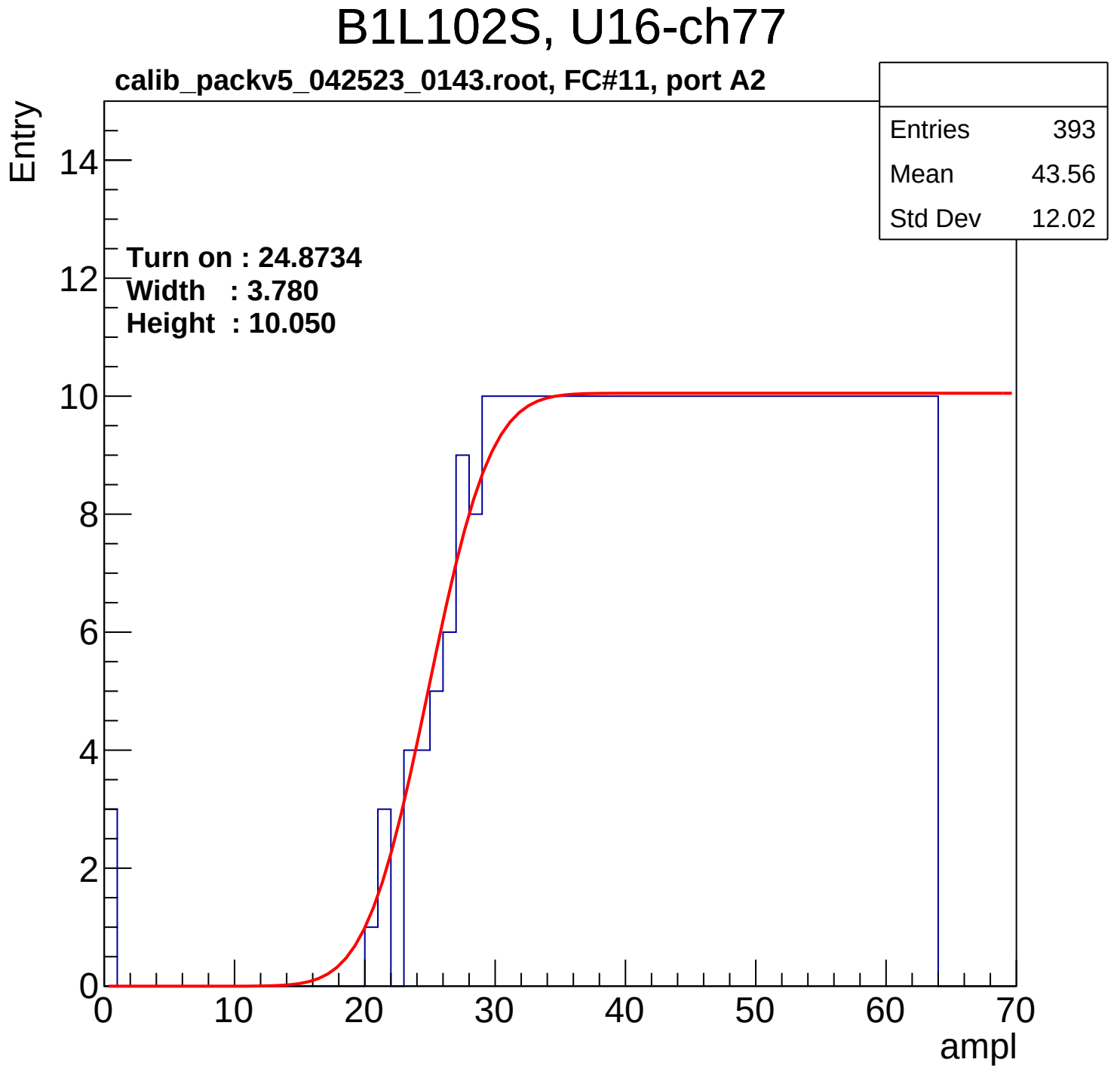

B1L102S, U16-ch72
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 43.94
Std Dev 11.65
Turn on : 26.0801
Width : 2.057
Height : 10.010
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

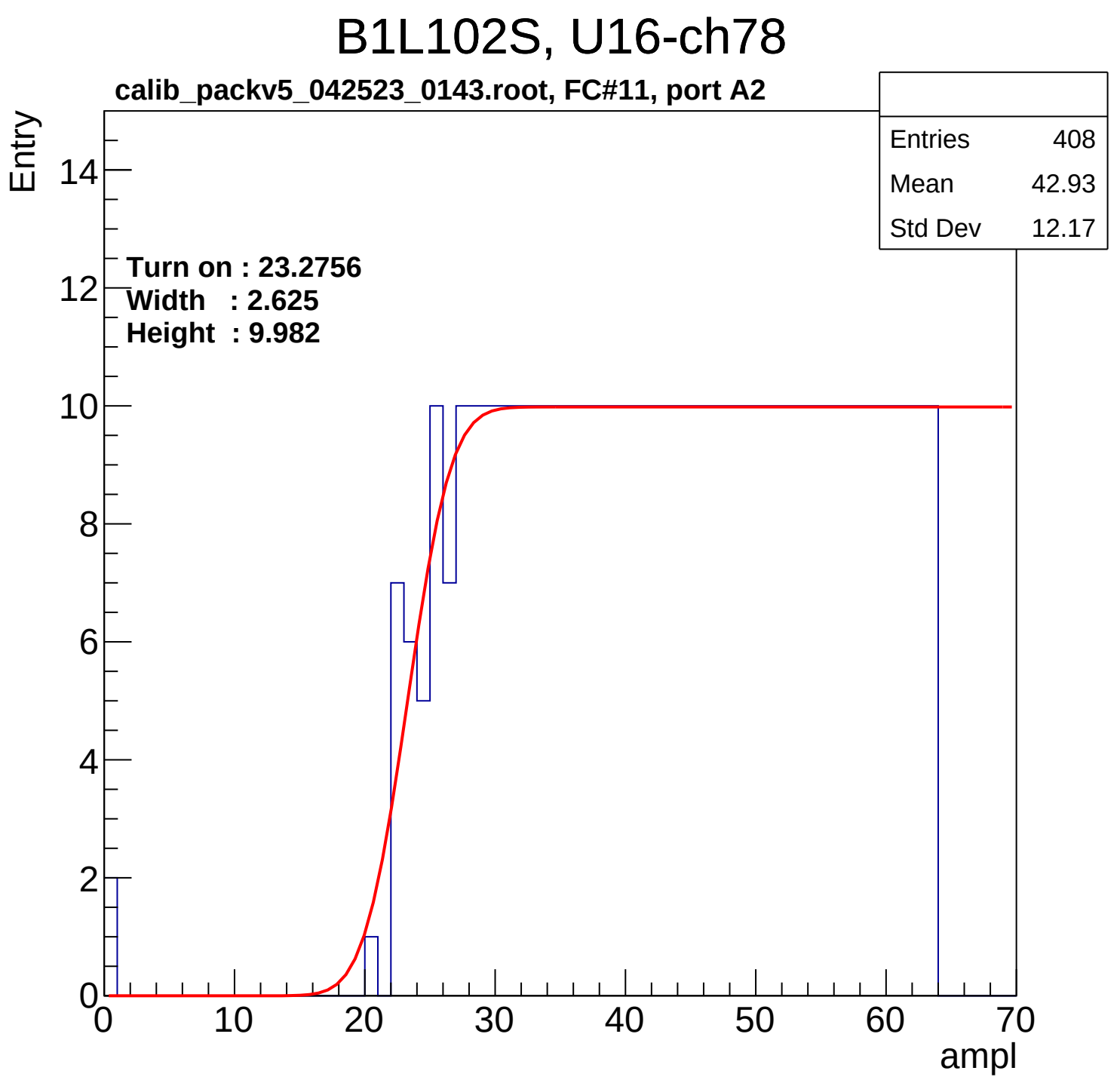

B1L102S, U16-ch73
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 43.73
Std Dev 12.13
Turn on : 25.7593
Width : 3.917
Height : 10.008
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

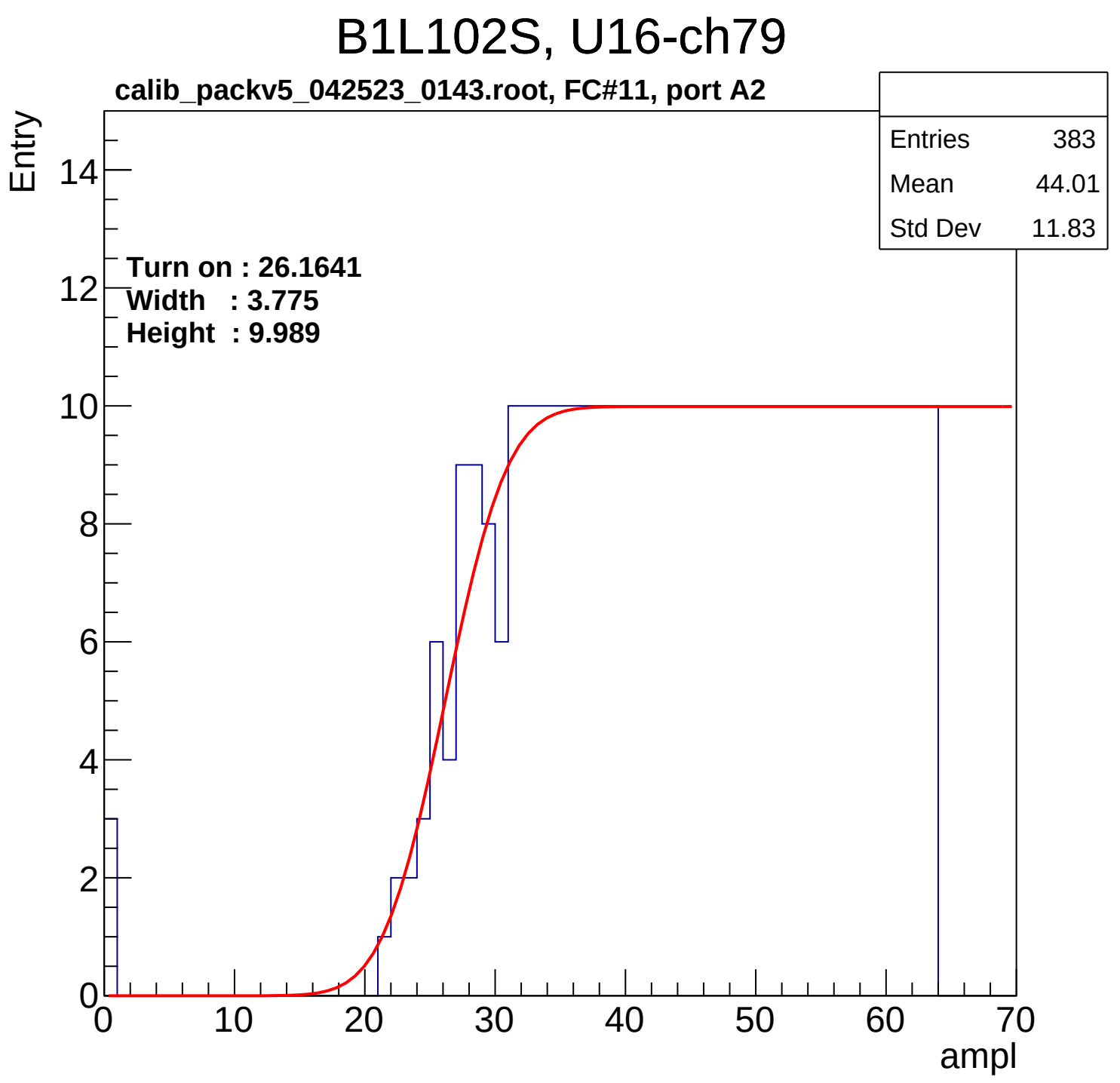

B1L102S, U16-ch74
calib_packv5_042523_0143.root, FC#11, port A2
Entries 376
Mean 44.37
Std Dev 11.71
Turn on : 26.8567
Width : 2.240
Height : 10.005
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

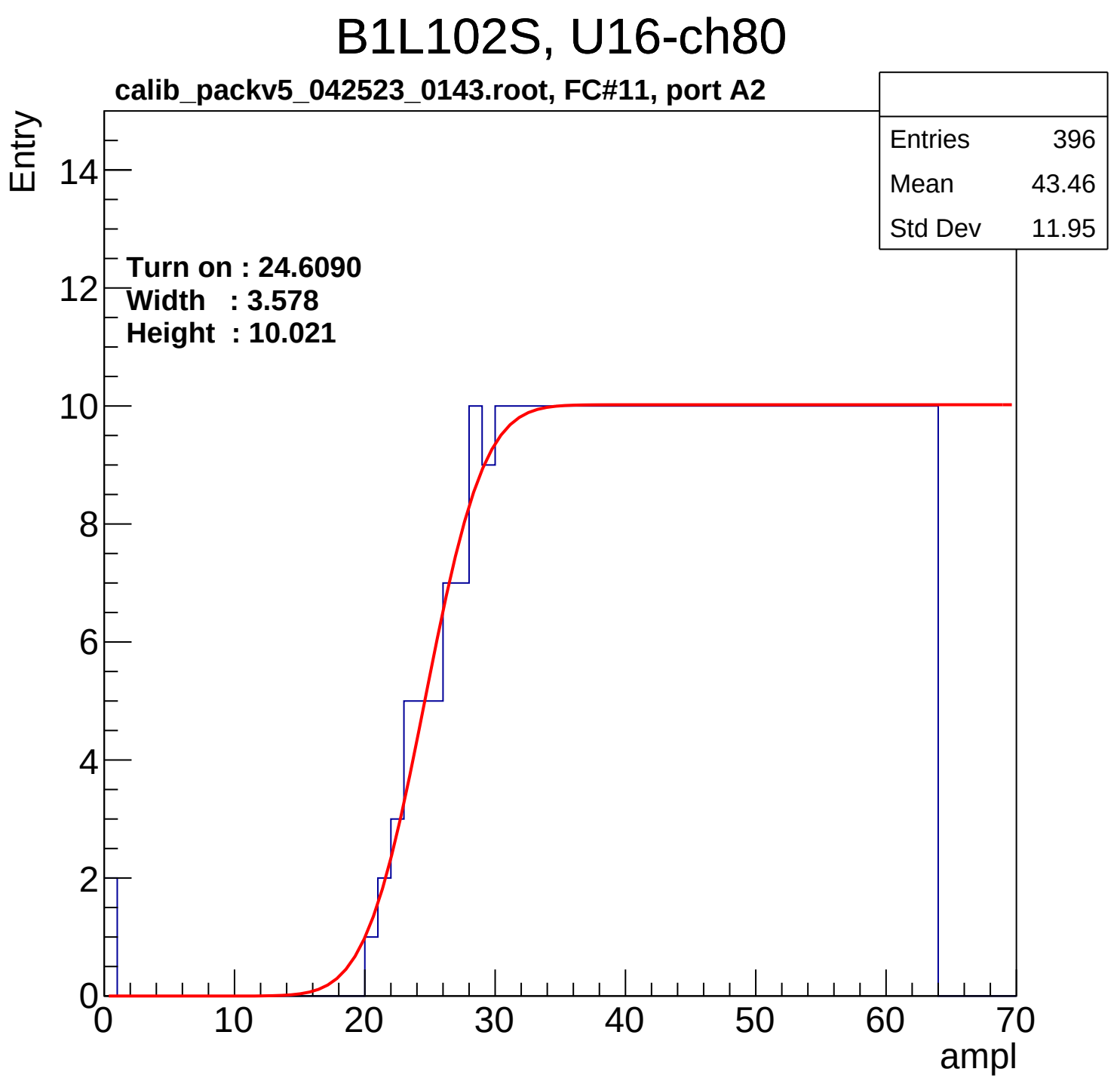

B1L102S, U16-ch75
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 44
Std Dev 11.85
Turn on : 26.3599
Width : 4.009
Height : 10.051
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

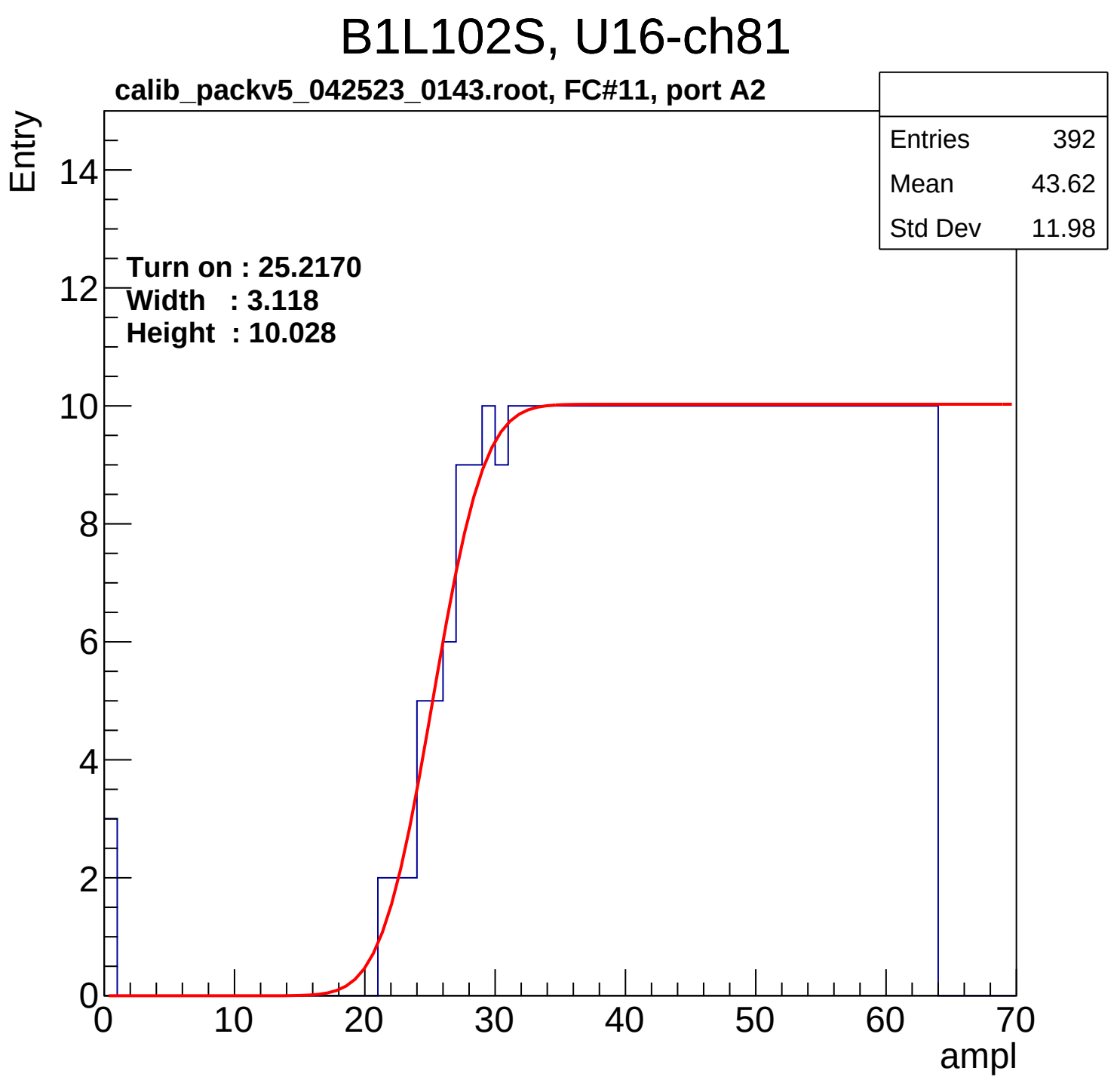

B1L102S, U16-ch76
calib_packv5_042523_0143.root, FC#11, port A2
Entries 395
Mean 43.56
Std Dev 11.79
Turn on : 24.9671
Width : 3.437
Height : 10.034
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

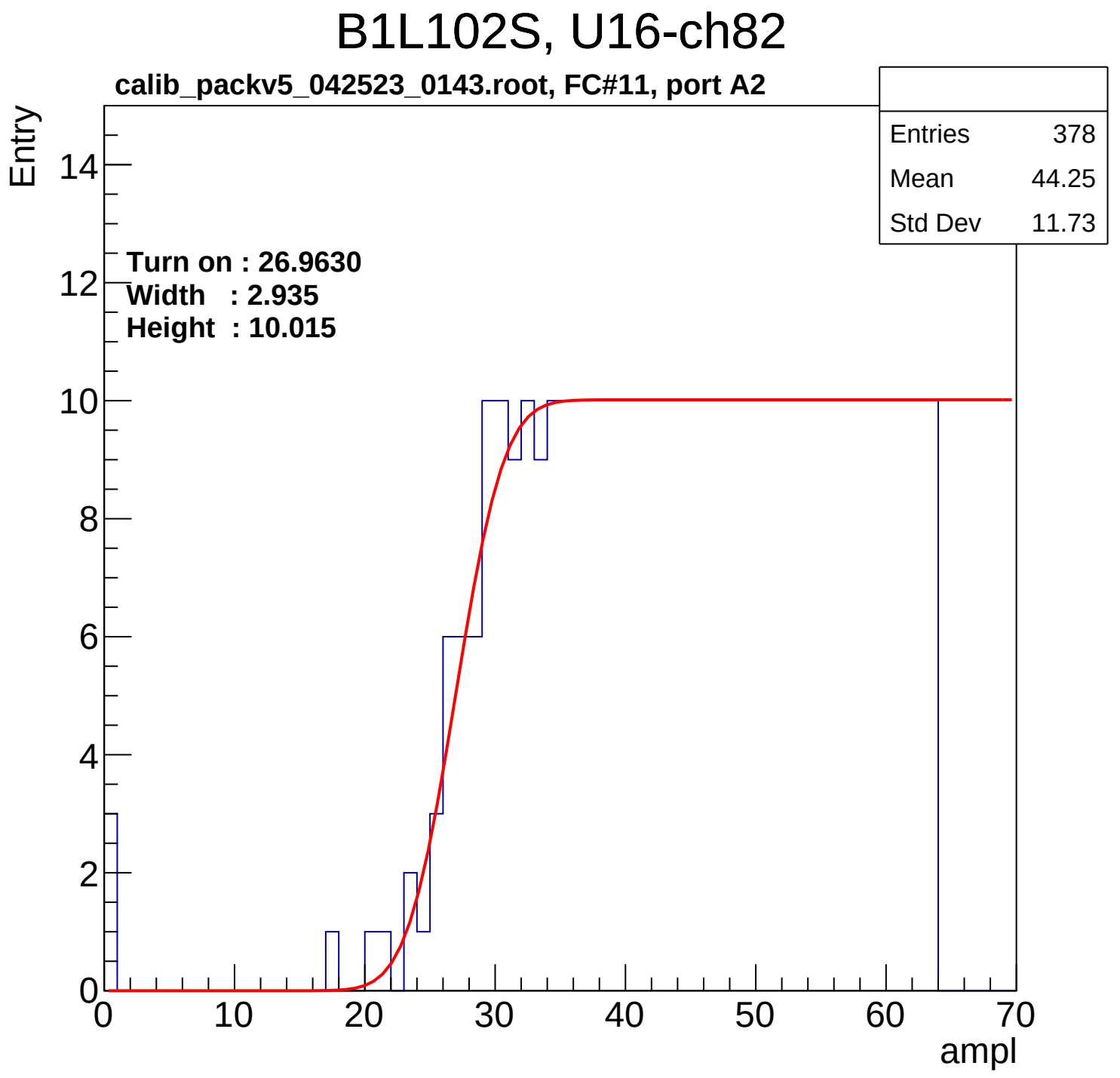

B1L102S, U16-ch77
calib_packv5_042523_0143.root, FC#11, port A2
Entries 393
Mean 43.56
Std Dev 12.02
Turn on : 24.8734
Width : 3.780
Height : 10.050
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

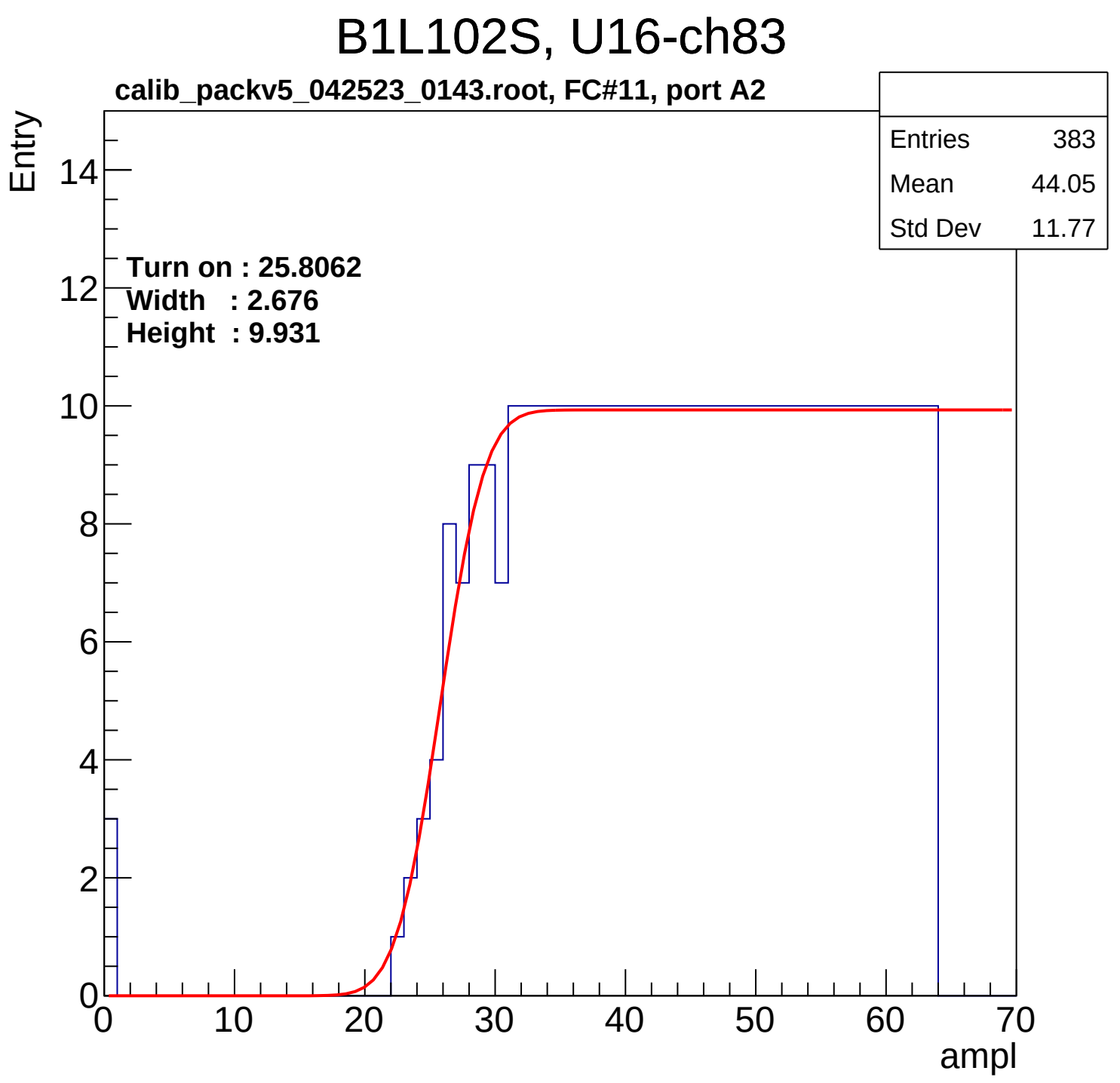

B1L102S, U16-ch78
calib_packv5_042523_0143.root, FC#11, port A2
Entries 408
Mean 42.93
Std Dev 12.17
Turn on : 23.2756
Width : 2.625
Height : 9.982
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

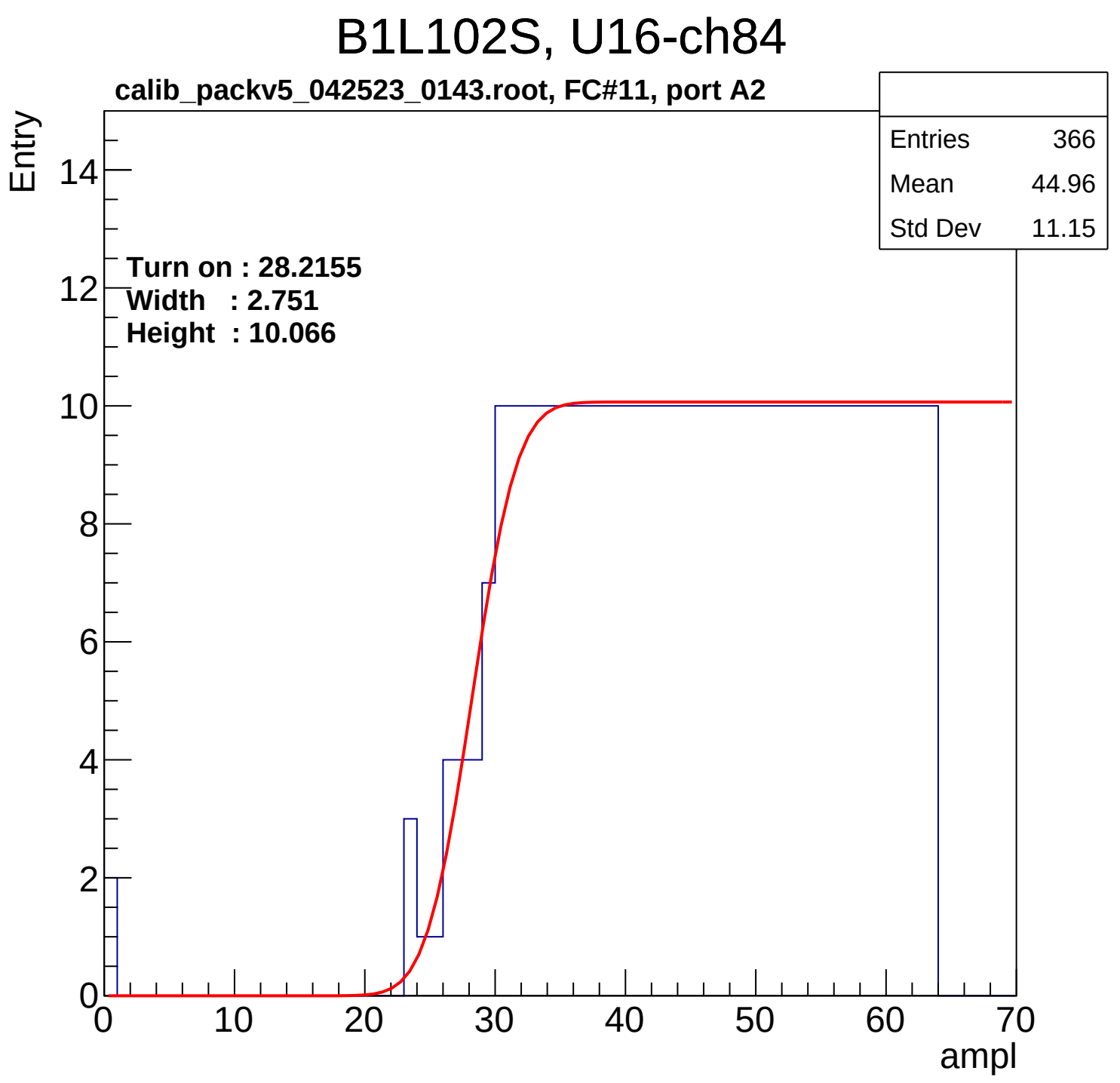

B1L102S, U16-ch79
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 44.01
Std Dev 11.83
Turn on : 26.1641
Width : 3.775
Height : 9.989
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

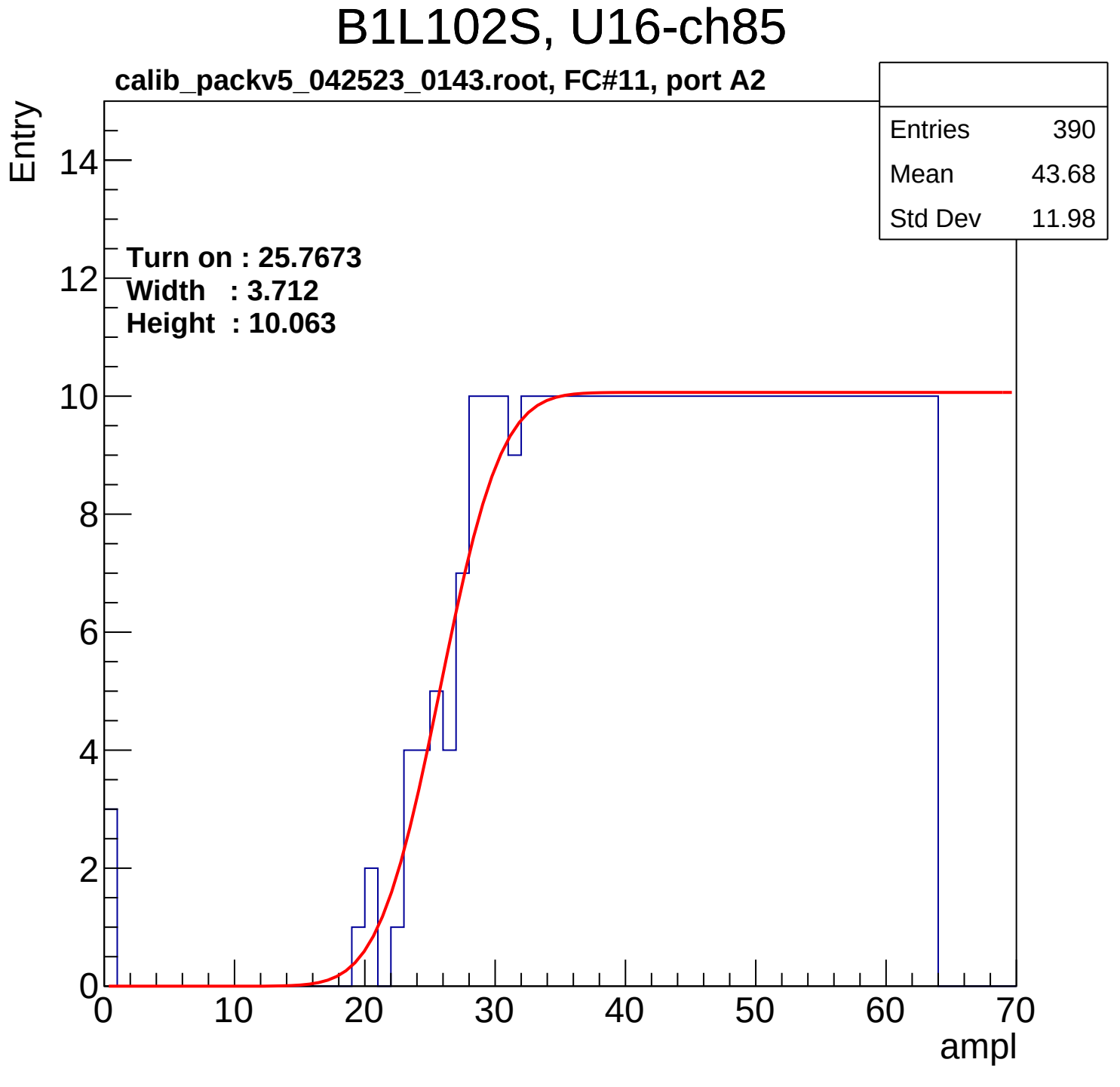

B1L102S, U16-ch80
calib_packv5_042523_0143.root, FC#11, port A2
Entries 396
Mean 43.46
Std Dev 11.95
Turn on : 24.6090
Width : 3.578
Height : 10.021
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

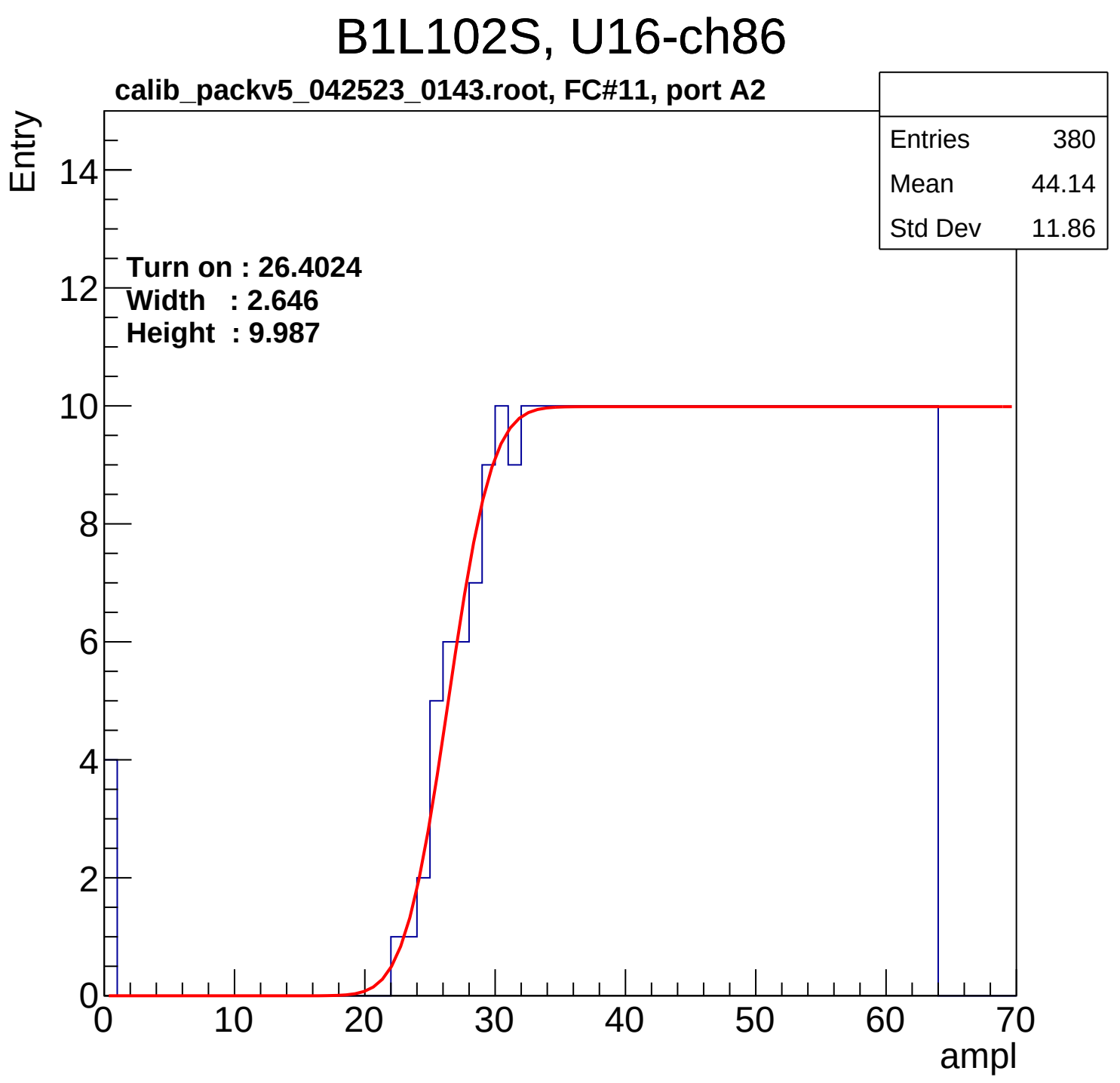

B1L102S, U16-ch81
calib_packv5_042523_0143.root, FC#11, port A2
Entries 392
Mean 43.62
Std Dev 11.98
Turn on : 25.2170
Width : 3.118
Height : 10.028
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

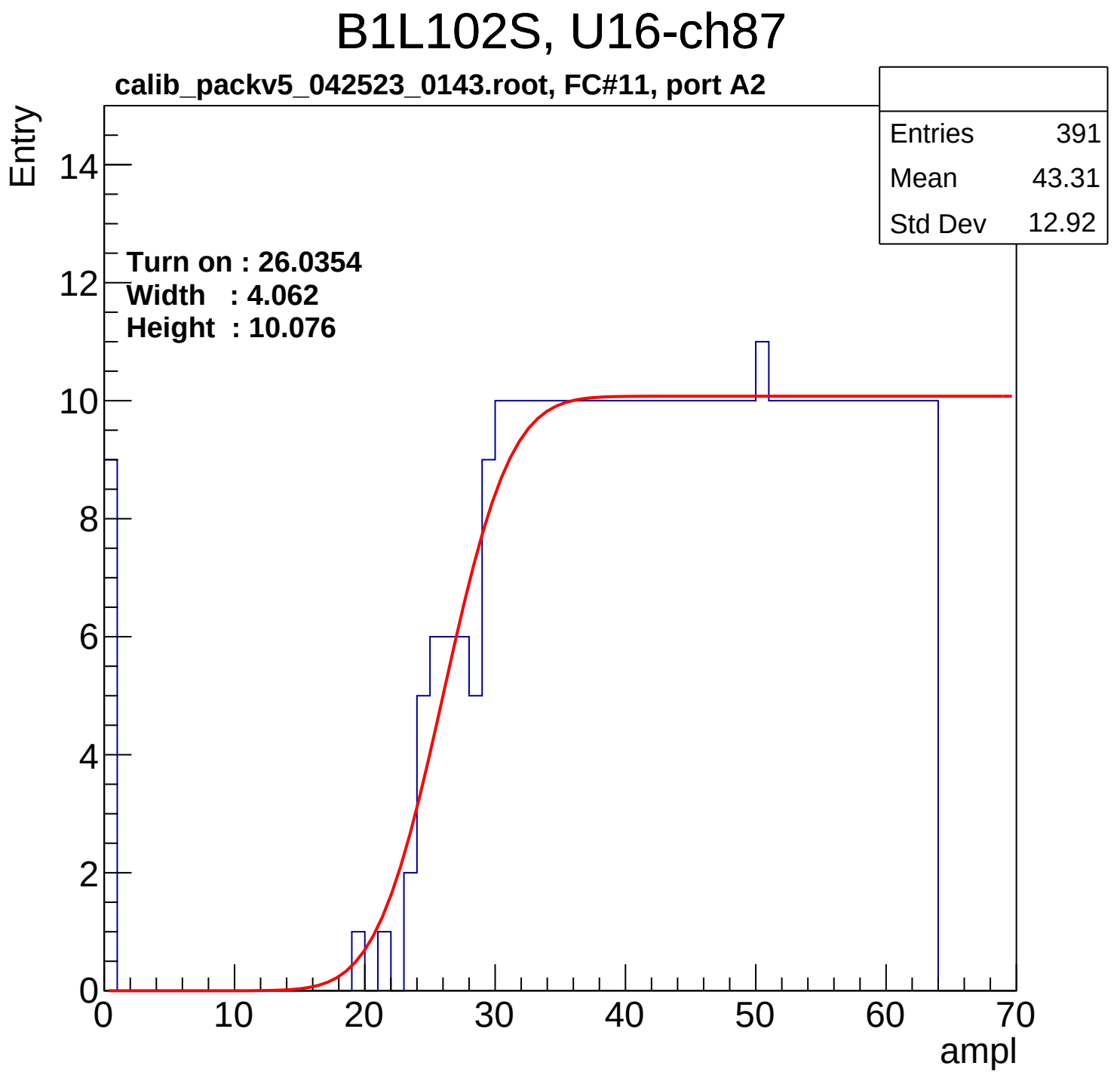

B1L102S, U16-ch82
calib_packv5_042523_0143.root, FC#11, port A2
Entries 378
Mean 44.25
Std Dev 11.73
Turn on : 26.9630
Width : 2.935
Height : 10.015
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

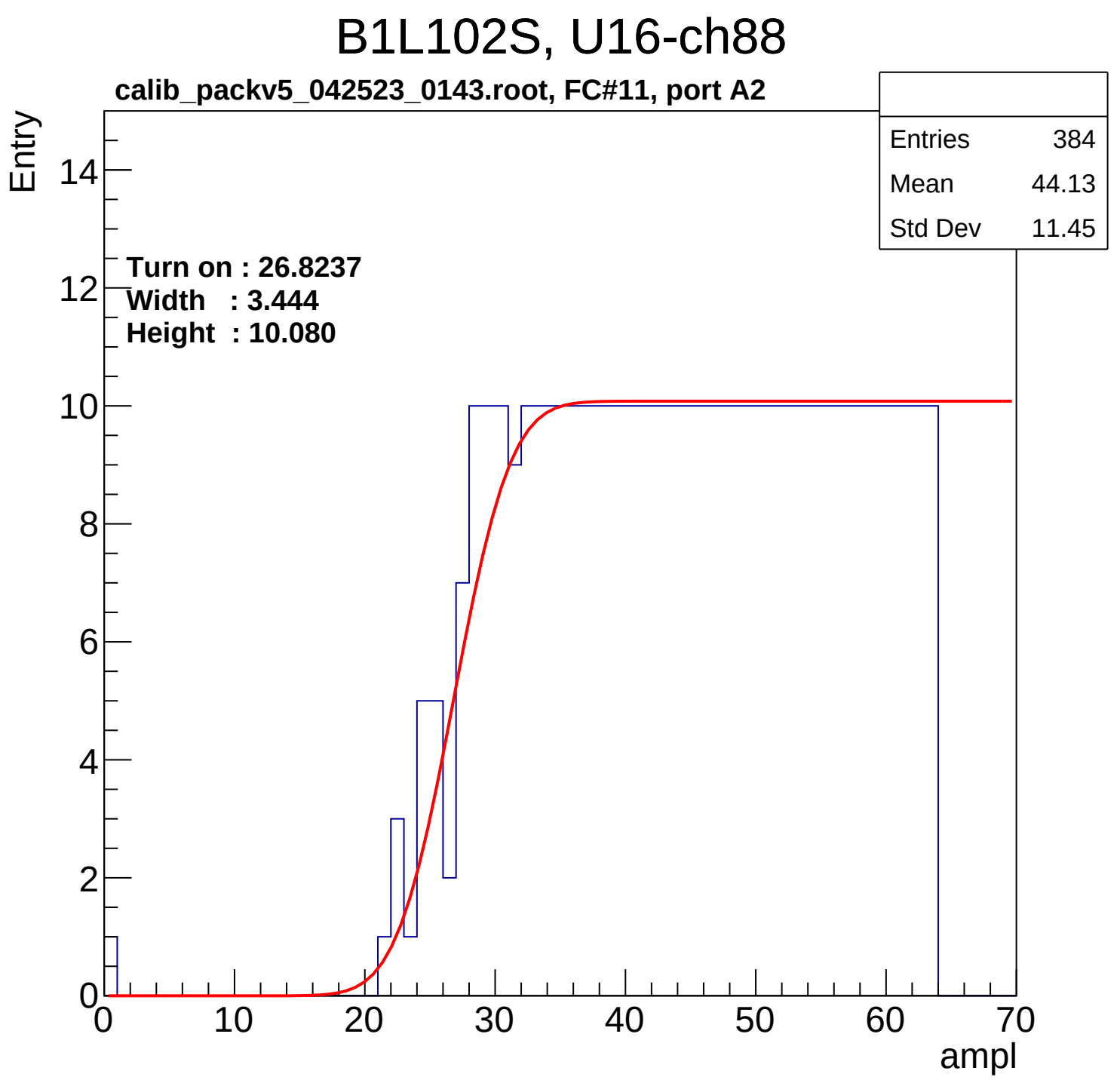

B1L102S, U16-ch83
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 44.05
Std Dev 11.77
Turn on : 25.8062
Width : 2.676
Height : 9.931
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

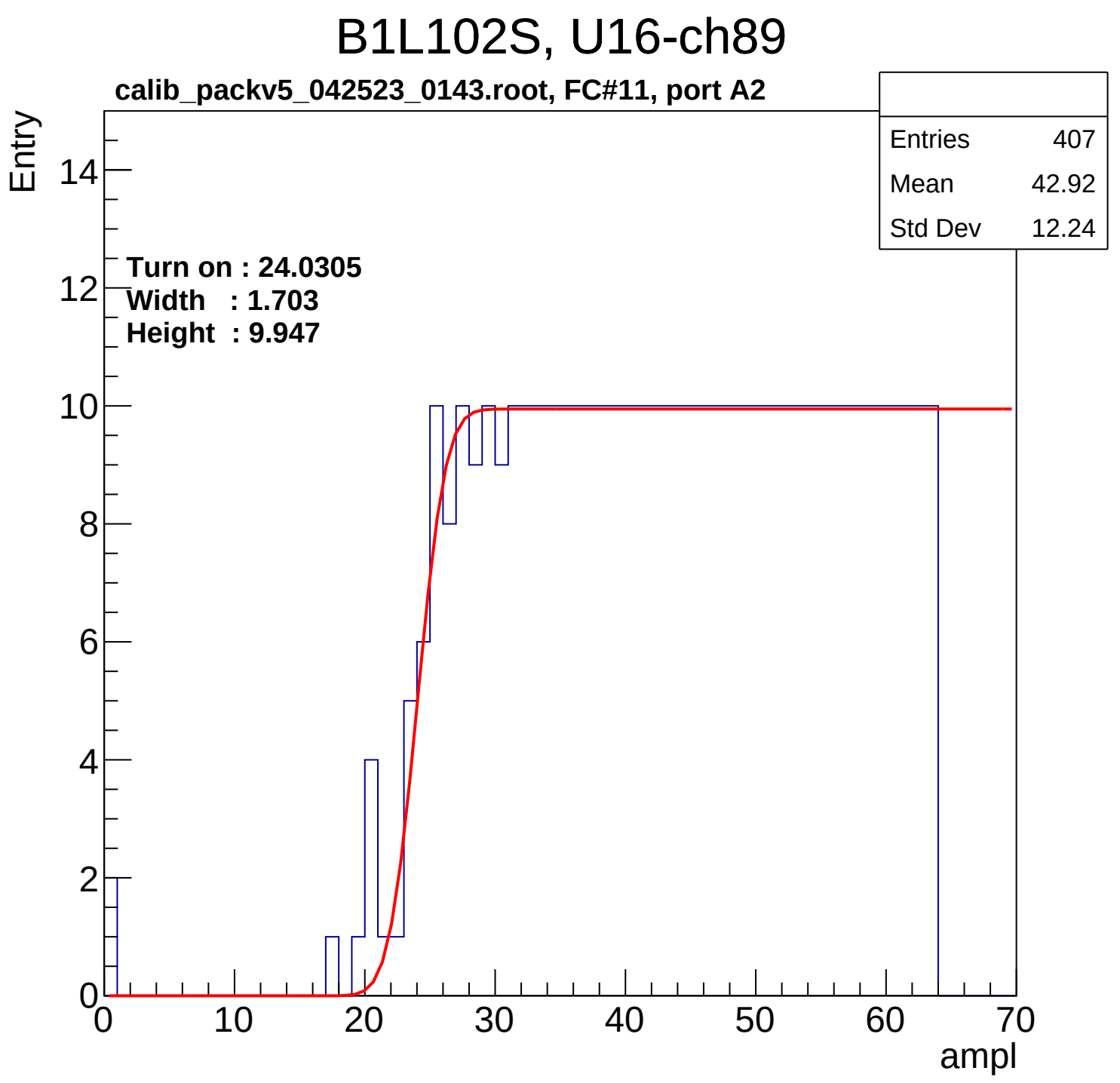

B1L102S, U16-ch84
calib_packv5_042523_0143.root, FC#11, port A2
Entries 366
Mean 44.96
Std Dev 11.15
Turn on : 28.2155
Width : 2.751
Height : 10.066
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

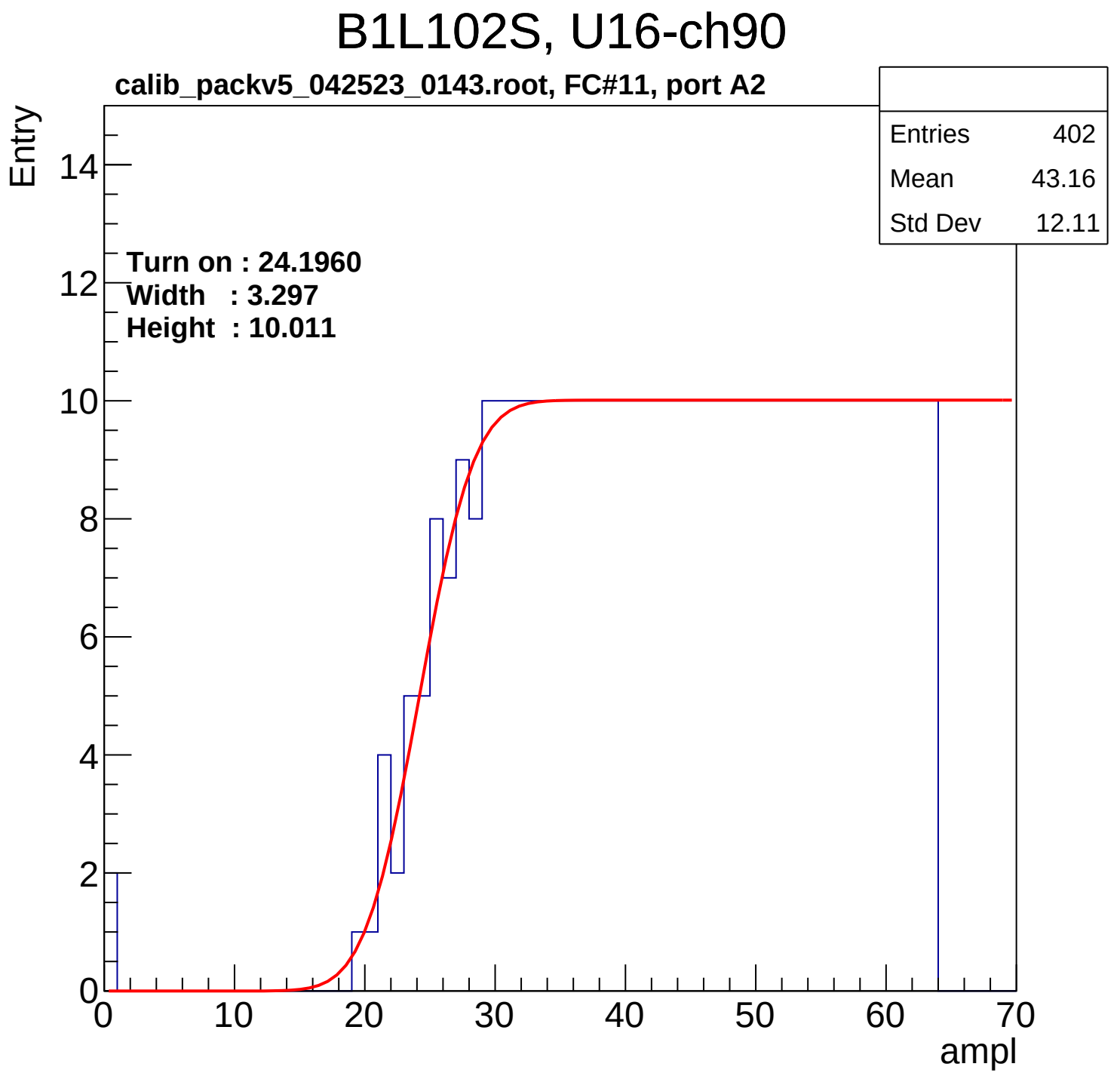

B1L102S, U16-ch85
calib_packv5_042523_0143.root, FC#11, port A2
Entries 390
Mean 43.68
Std Dev 11.98
Turn on : 25.7673
Width : 3.712
Height : 10.063
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

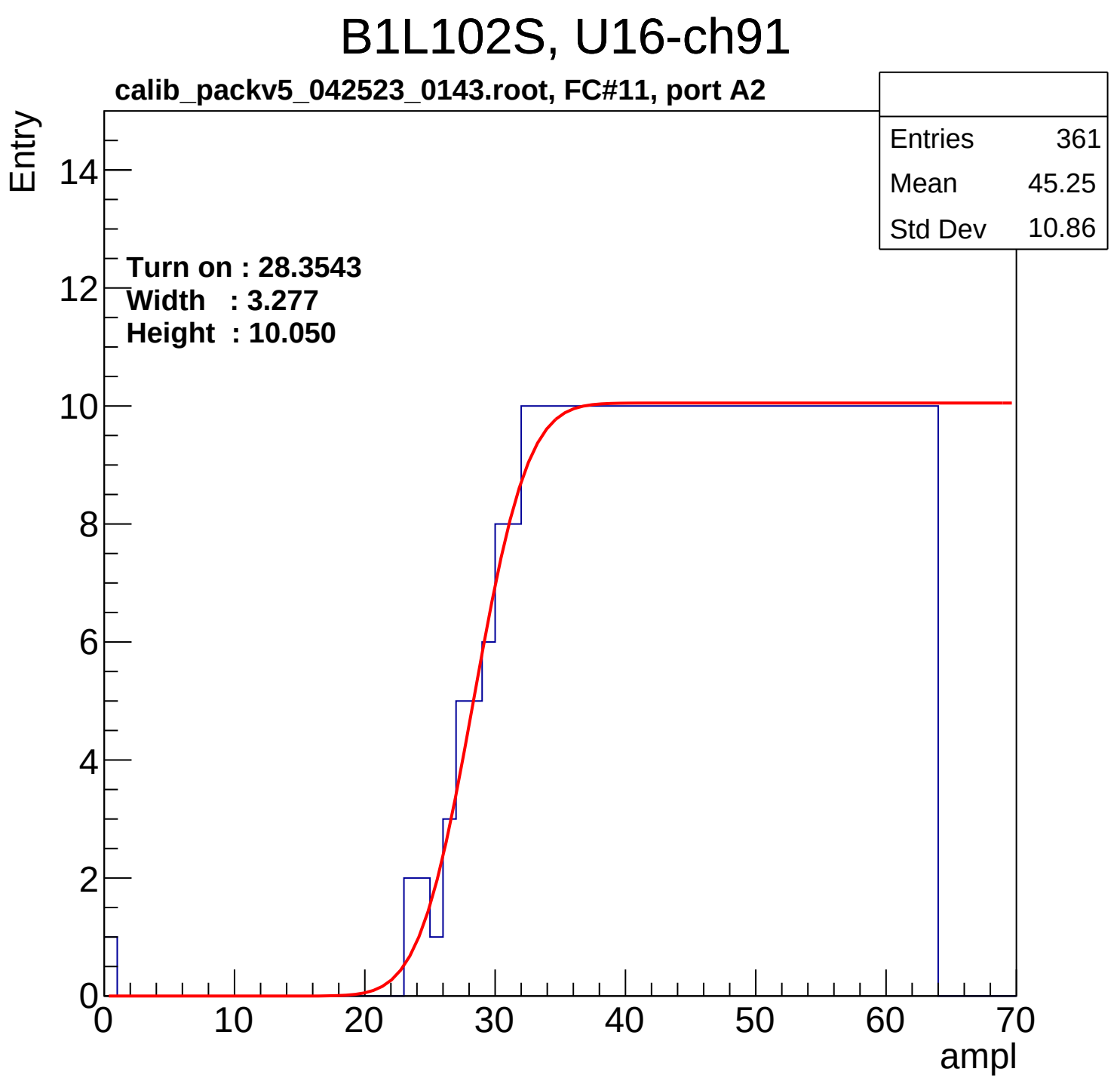

B1L102S, U16-ch86
calib_packv5_042523_0143.root, FC#11, port A2
Entries 380
Mean 44.14
Std Dev 11.86
Turn on : 26.4024
Width : 2.646
Height : 9.987
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

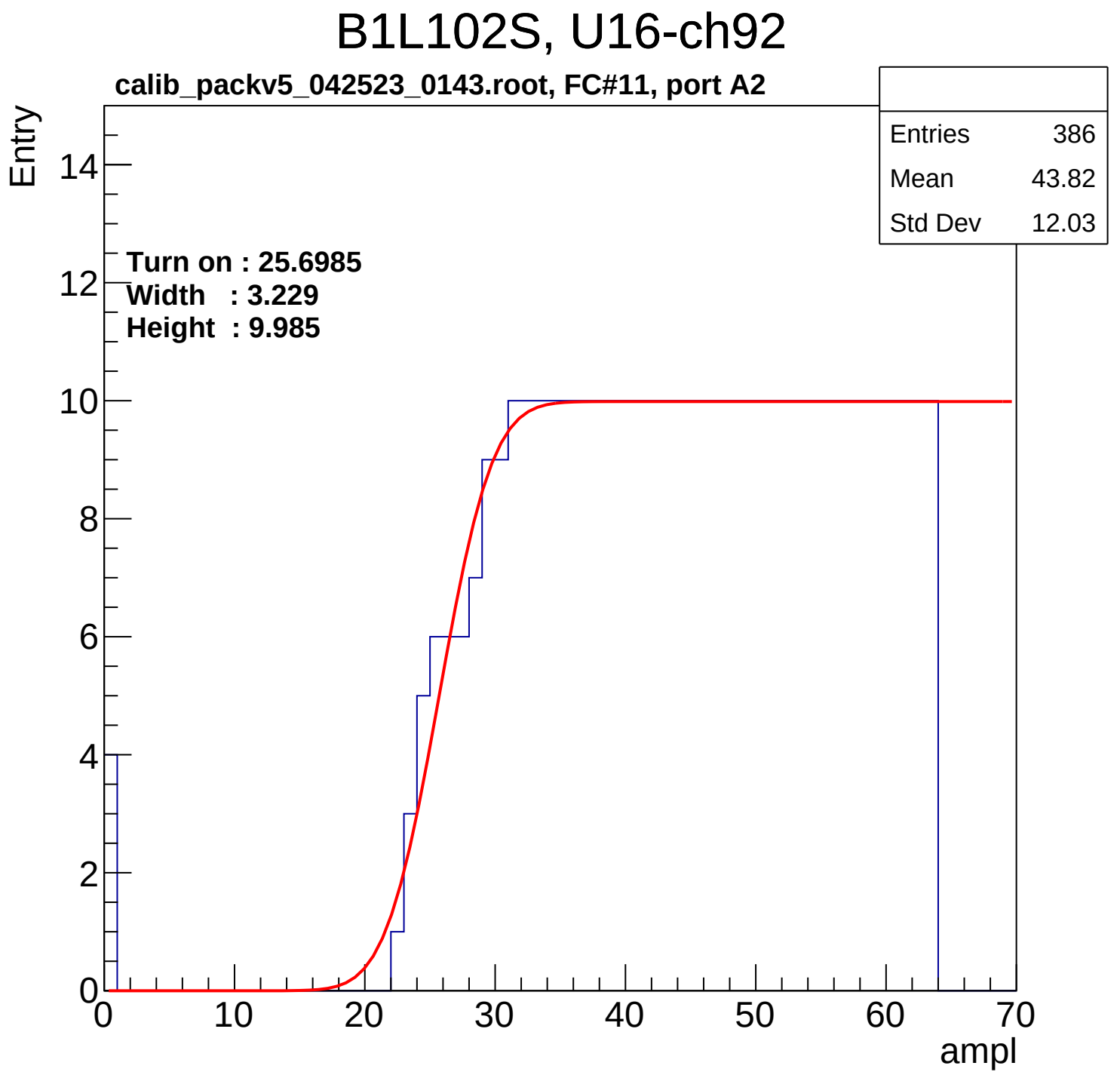

B1L102S, U16-ch87
calib_packv5_042523_0143.root, FC#11, port A2
Entries 391
Mean 43.31
Std Dev 12.92
Turn on : 26.0354
Width : 4.062
Height : 10.076
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

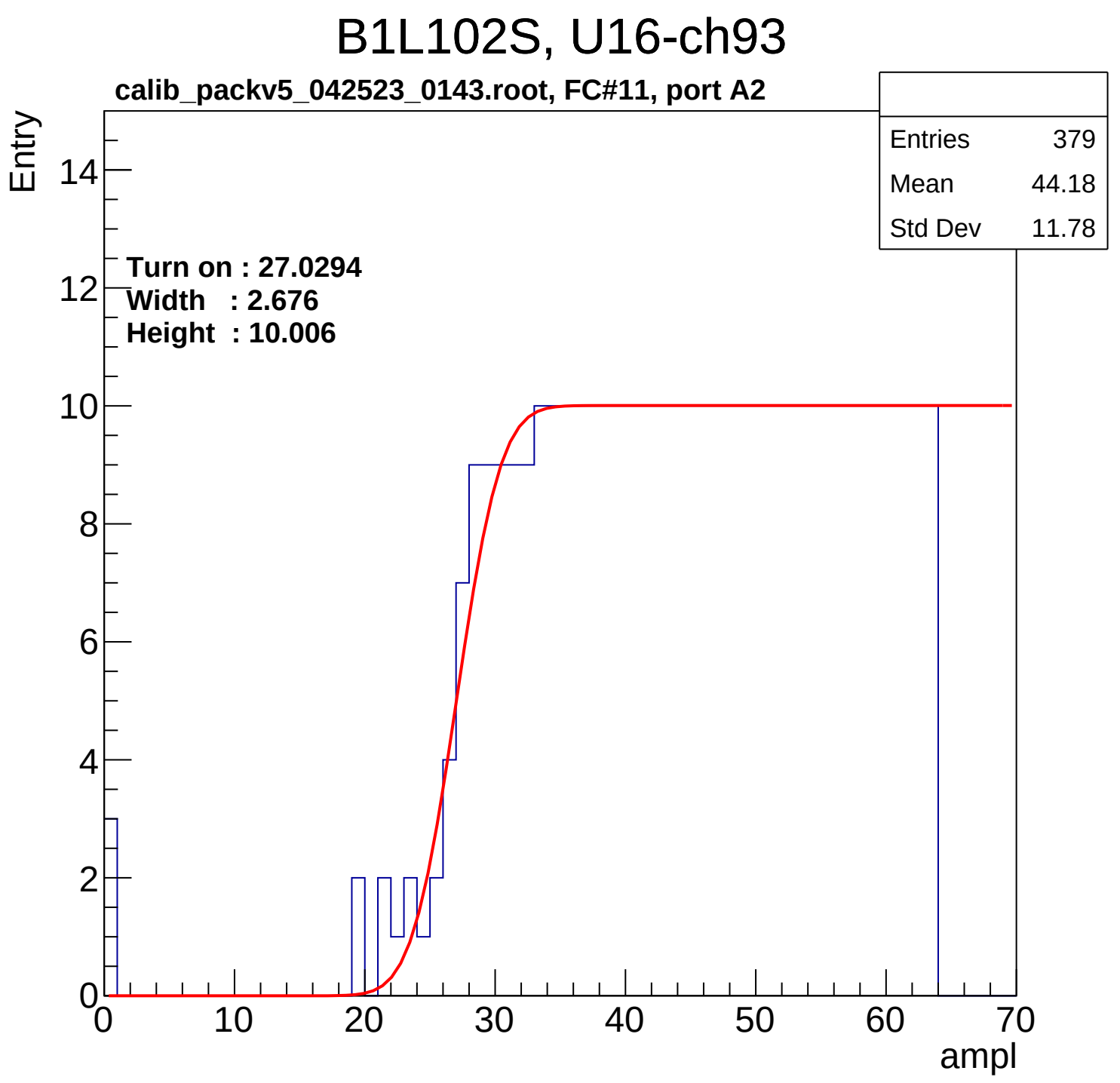

B1L102S, U16-ch88
calib_packv5_042523_0143.root, FC#11, port A2
Entries 384
Mean 44.13
Std Dev 11.45
Turn on : 26.8237
Width : 3.444
Height : 10.080
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

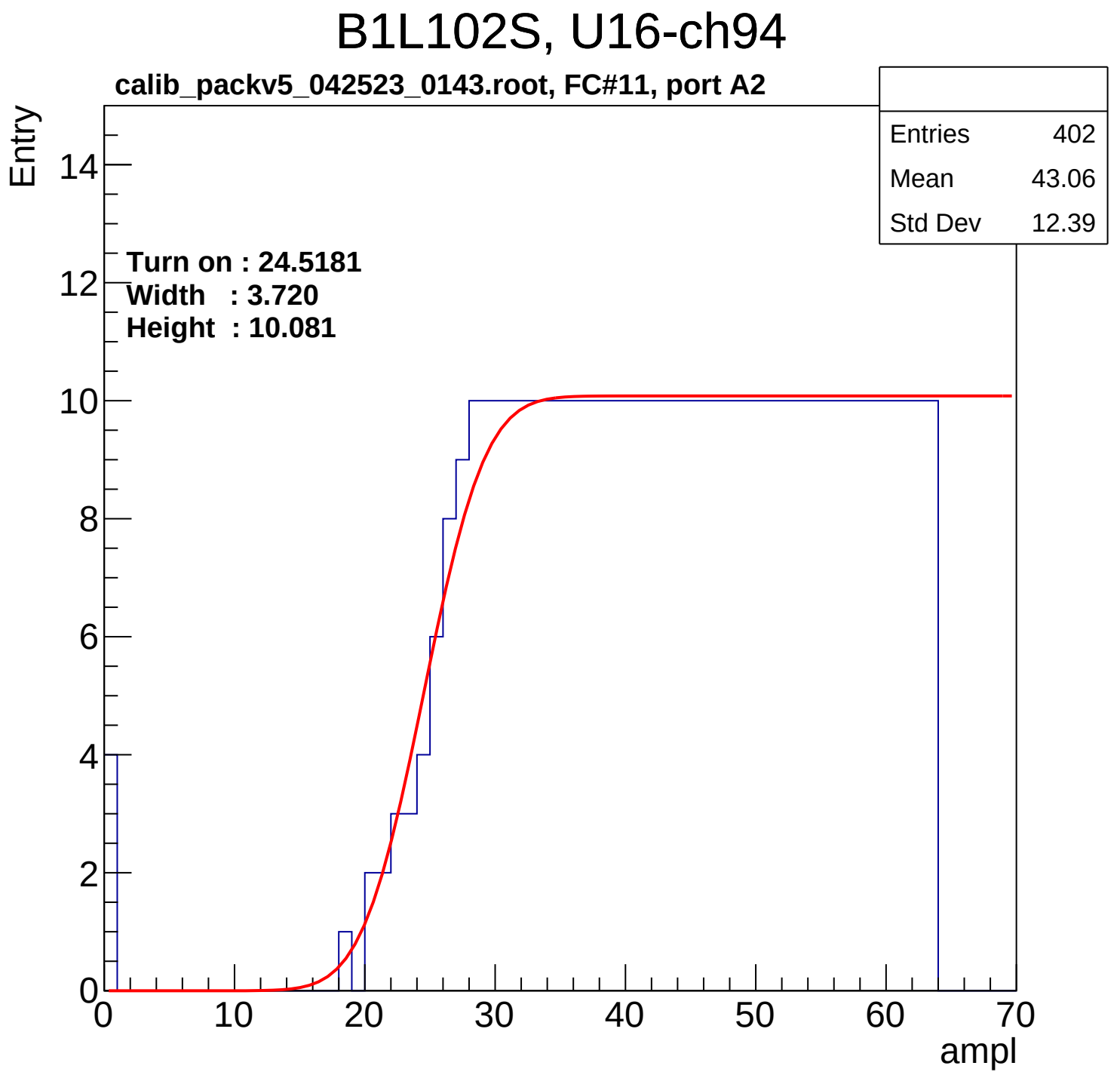

B1L102S, U16-ch89
calib_packv5_042523_0143.root, FC#11, port A2
Entries 407
Mean 42.92
Std Dev 12.24
Turn on : 24.0305
Width : 1.703
Height : 9.947
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

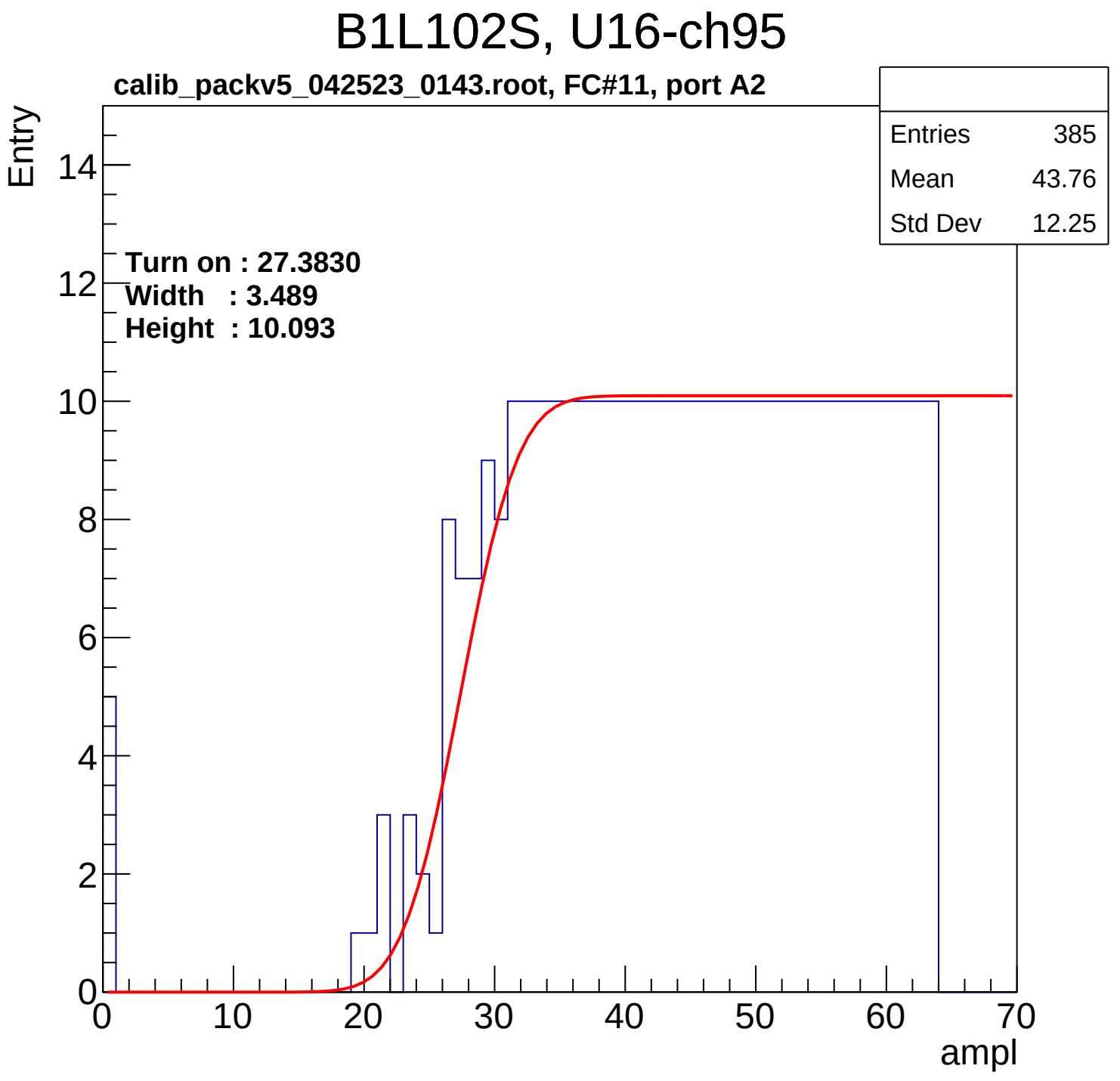

B1L102S, U16-ch90
calib_packv5_042523_0143.root, FC#11, port A2
Entries 402
Mean 43.16
Std Dev 12.11
Turn on : 24.1960
Width : 3.297
Height : 10.011
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

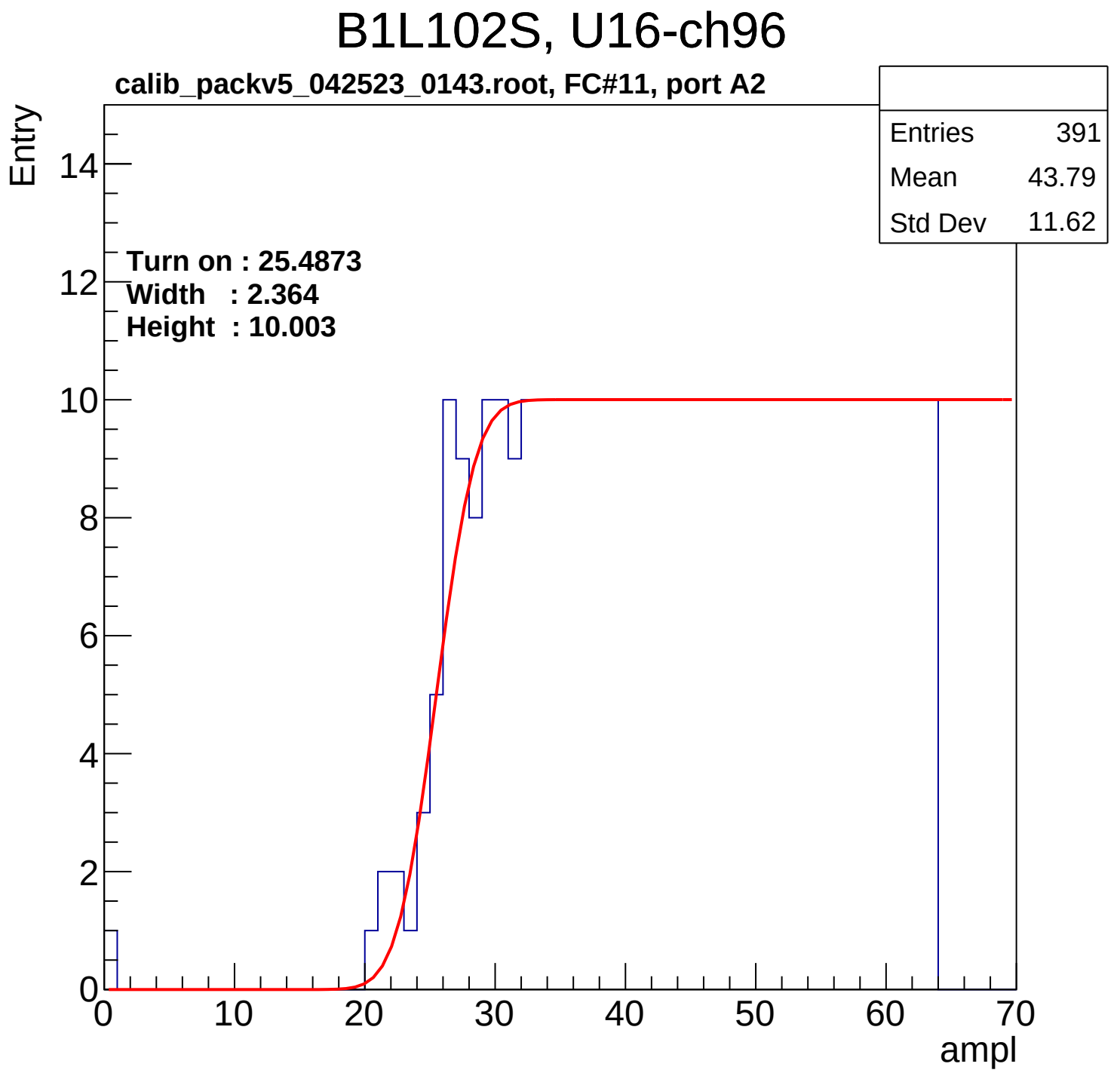

B1L102S, U16-ch91
calib_packv5_042523_0143.root, FC#11, port A2
Entries 361
Mean 45.25
Std Dev 10.86
Turn on : 28.3543
Width : 3.277
Height : 10.050
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

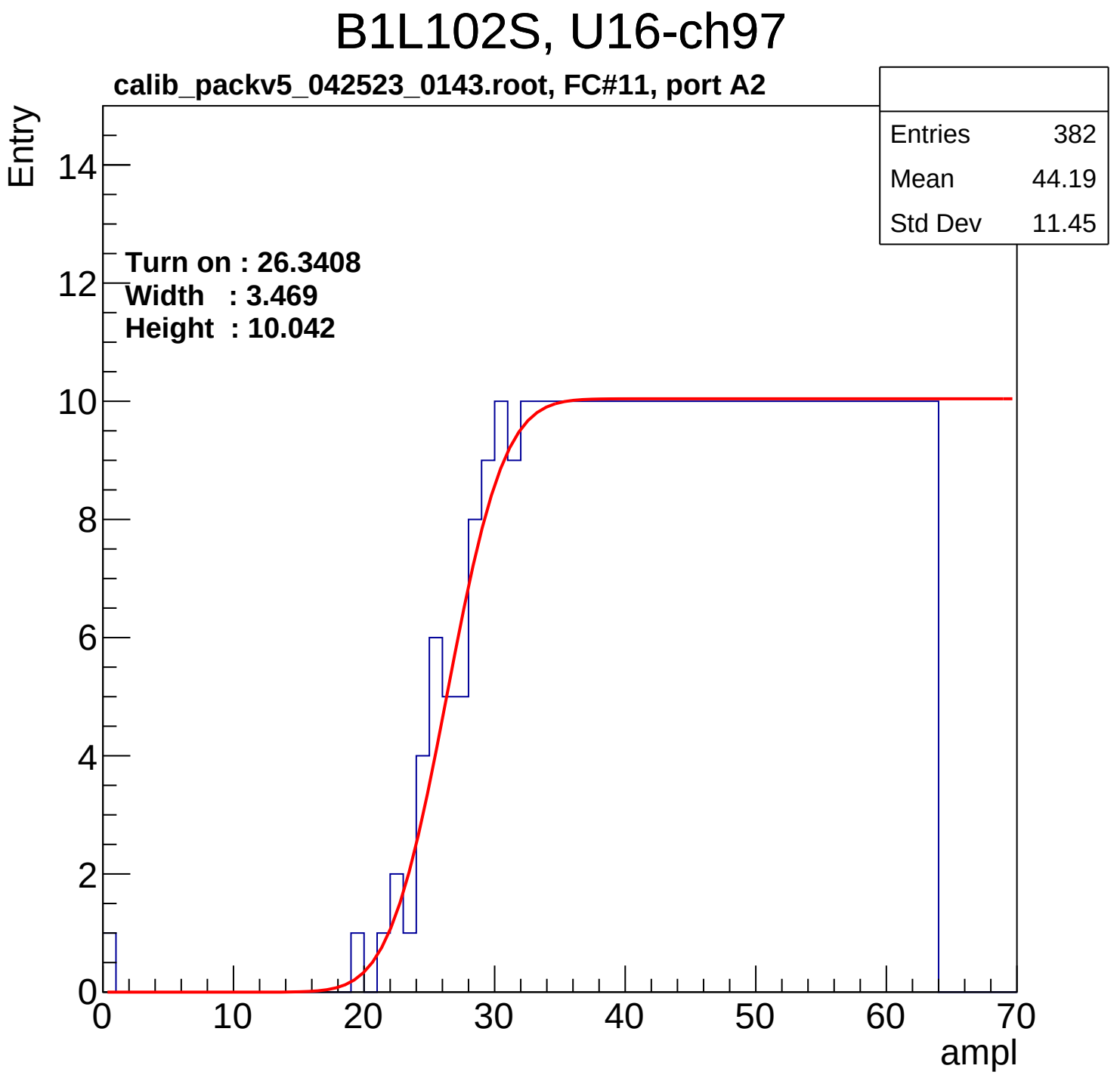

B1L102S, U16-ch92
calib_packv5_042523_0143.root, FC#11, port A2
Entries 386
Mean 43.82
Std Dev 12.03
Turn on : 25.6985
Width : 3.229
Height : 9.985
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

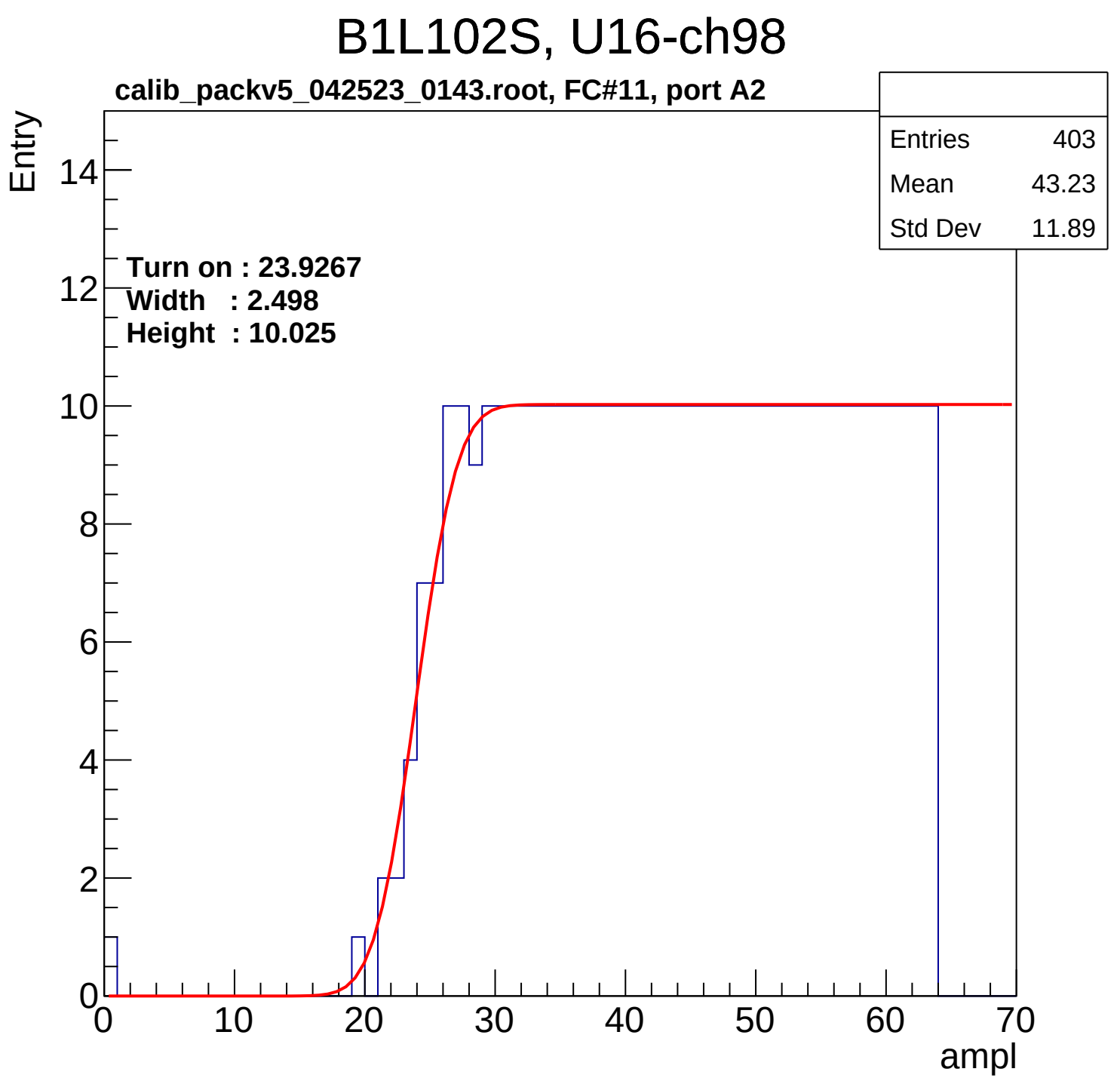

B1L102S, U16-ch93
calib_packv5_042523_0143.root, FC#11, port A2
Entries 379
Mean 44.18
Std Dev 11.78
Turn on : 27.0294
Width : 2.676
Height : 10.006
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

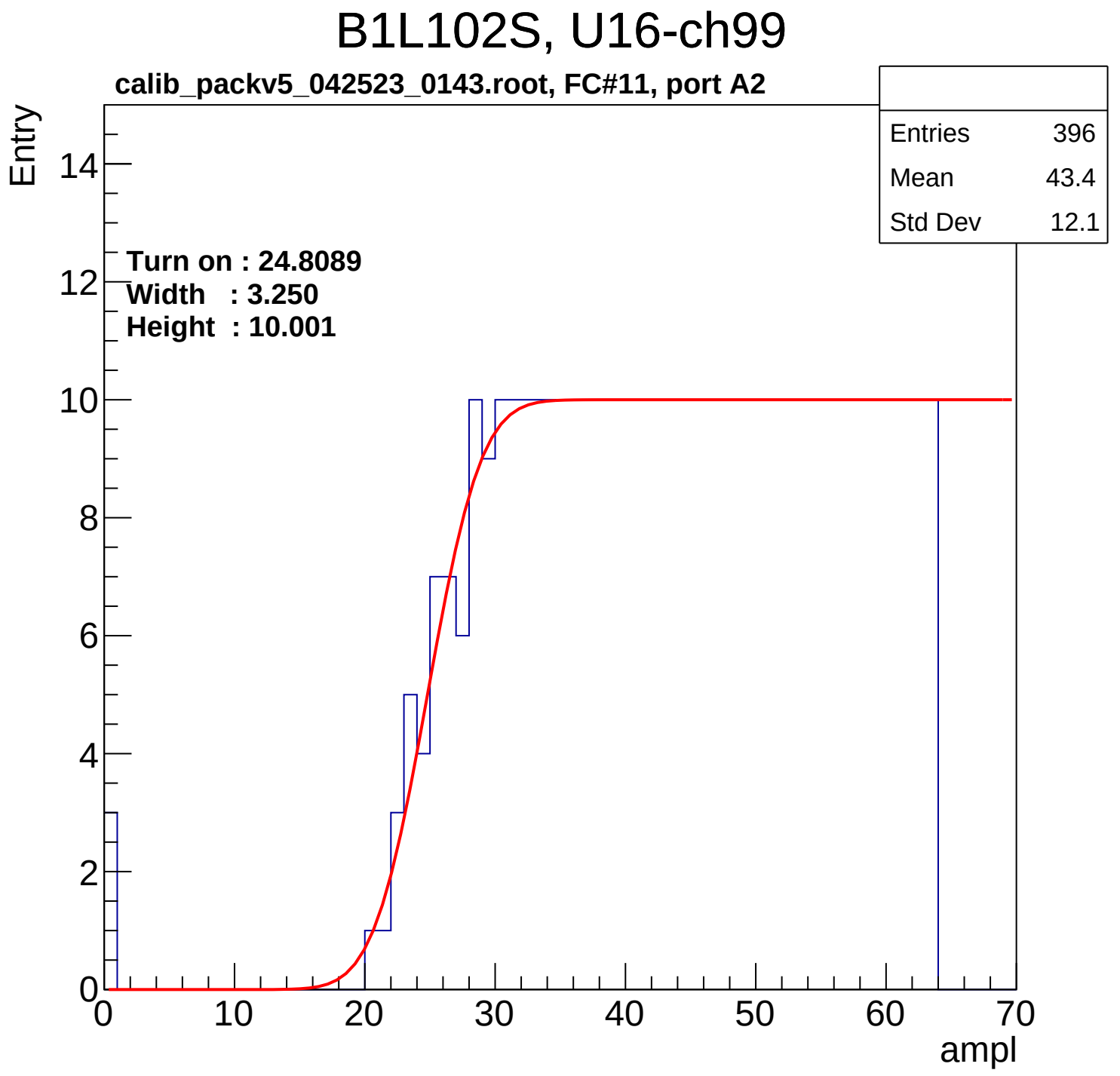

B1L102S, U16-ch94
calib_packv5_042523_0143.root, FC#11, port A2
Entries 402
Mean 43.06
Std Dev 12.39
Turn on : 24.5181
Width : 3.720
Height : 10.081
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

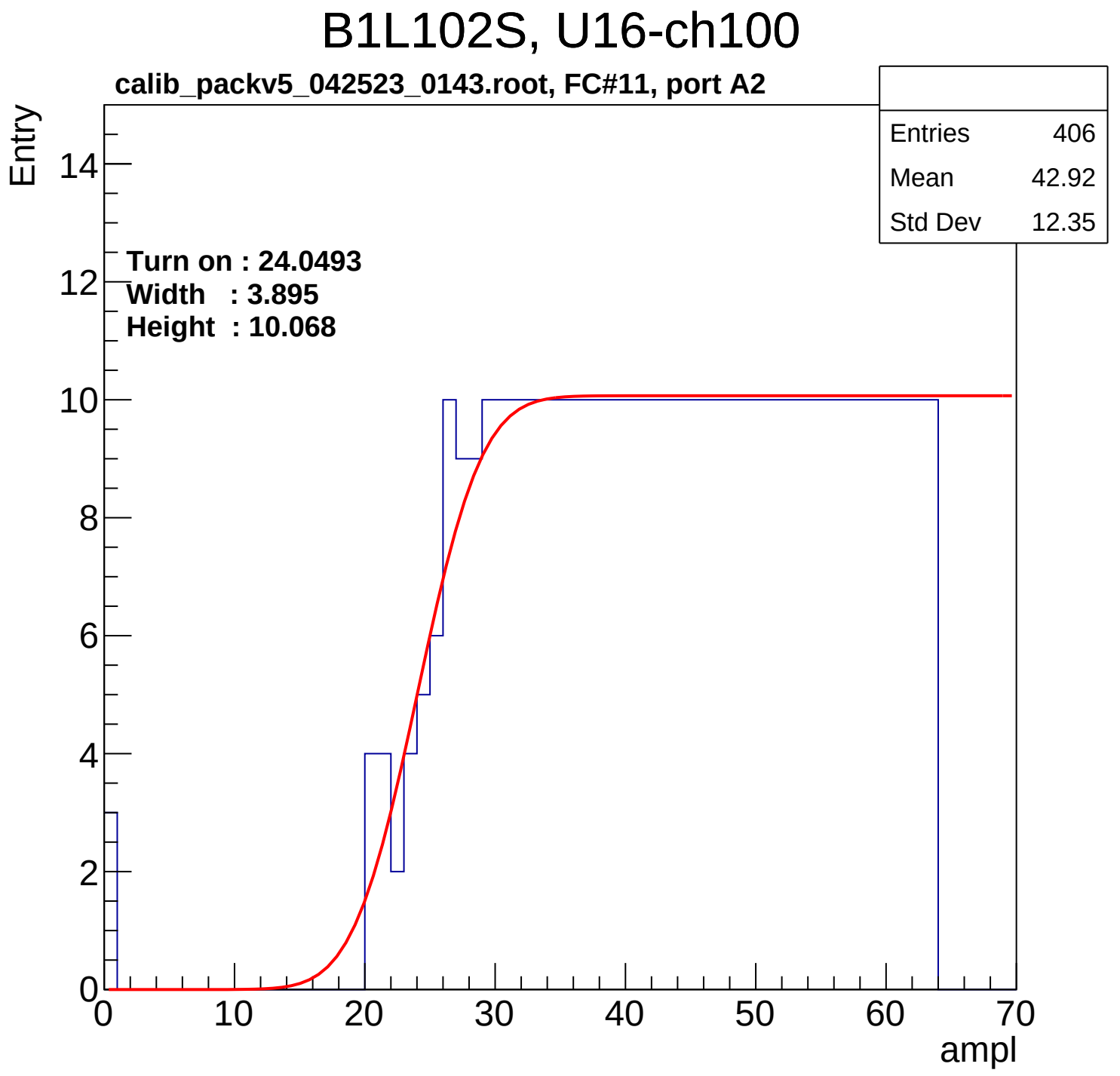

B1L102S, U16-ch95
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 43.76
Std Dev 12.25
Turn on : 27.3830
Width : 3.489
Height : 10.093
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

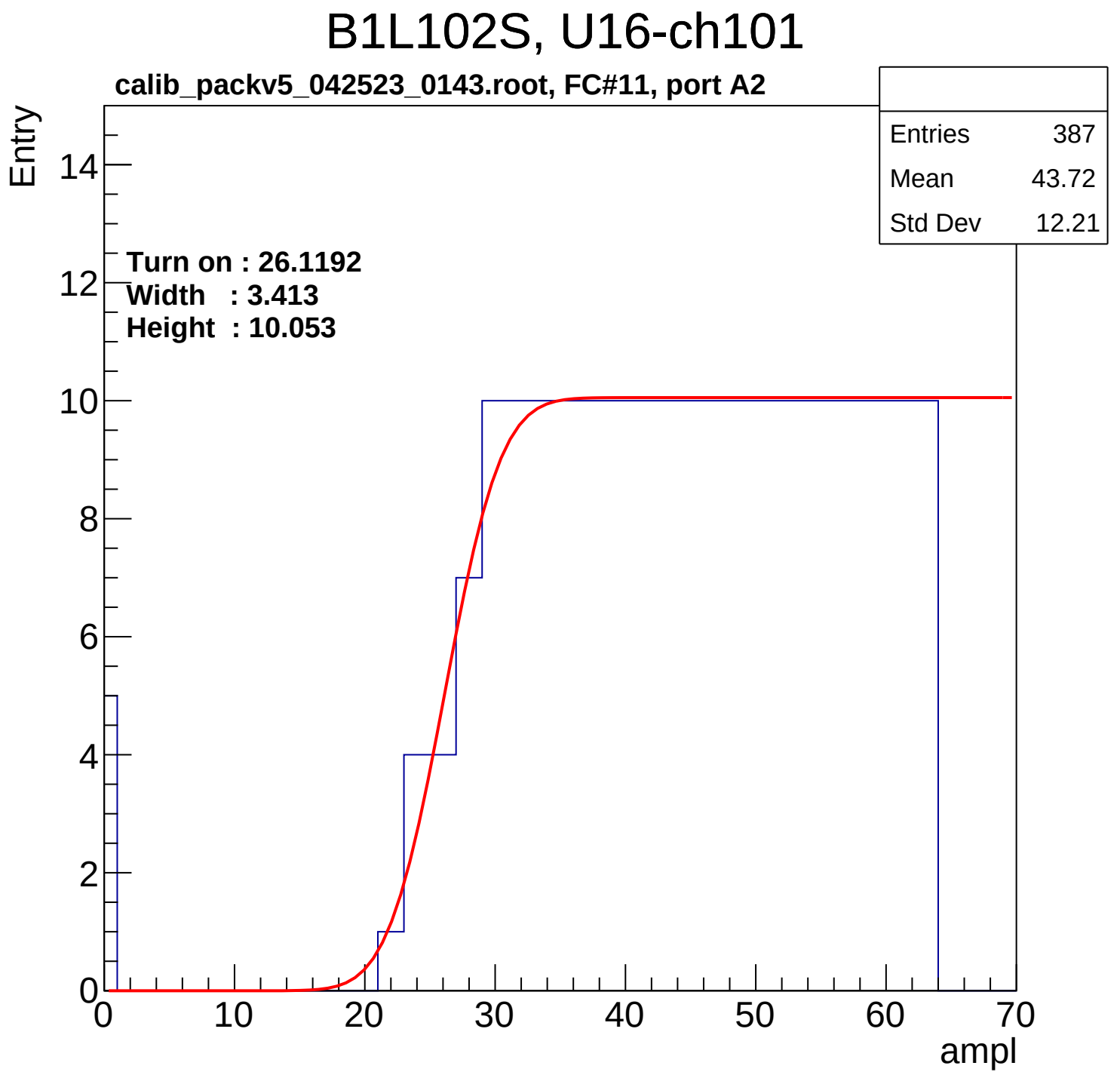

B1L102S, U16-ch96
calib_packv5_042523_0143.root, FC#11, port A2
Entries 391
Mean 43.79
Std Dev 11.62
Turn on : 25.4873
Width : 2.364
Height : 10.003
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

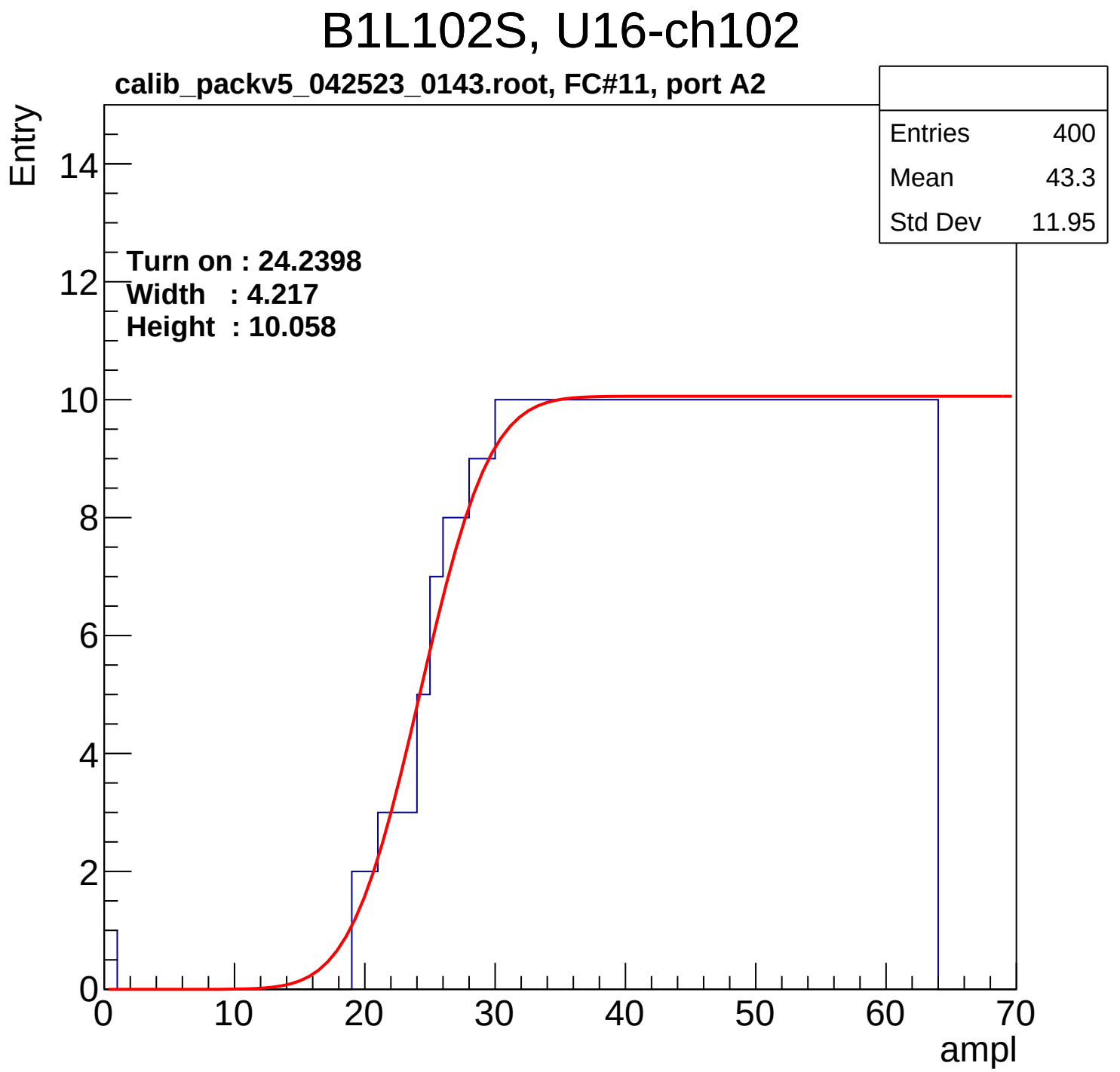

B1L102S, U16-ch97
calib_packv5_042523_0143.root, FC#11, port A2
Entries 382
Mean 44.19
Std Dev 11.45
Turn on : 26.3408
Width : 3.469
Height : 10.042
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

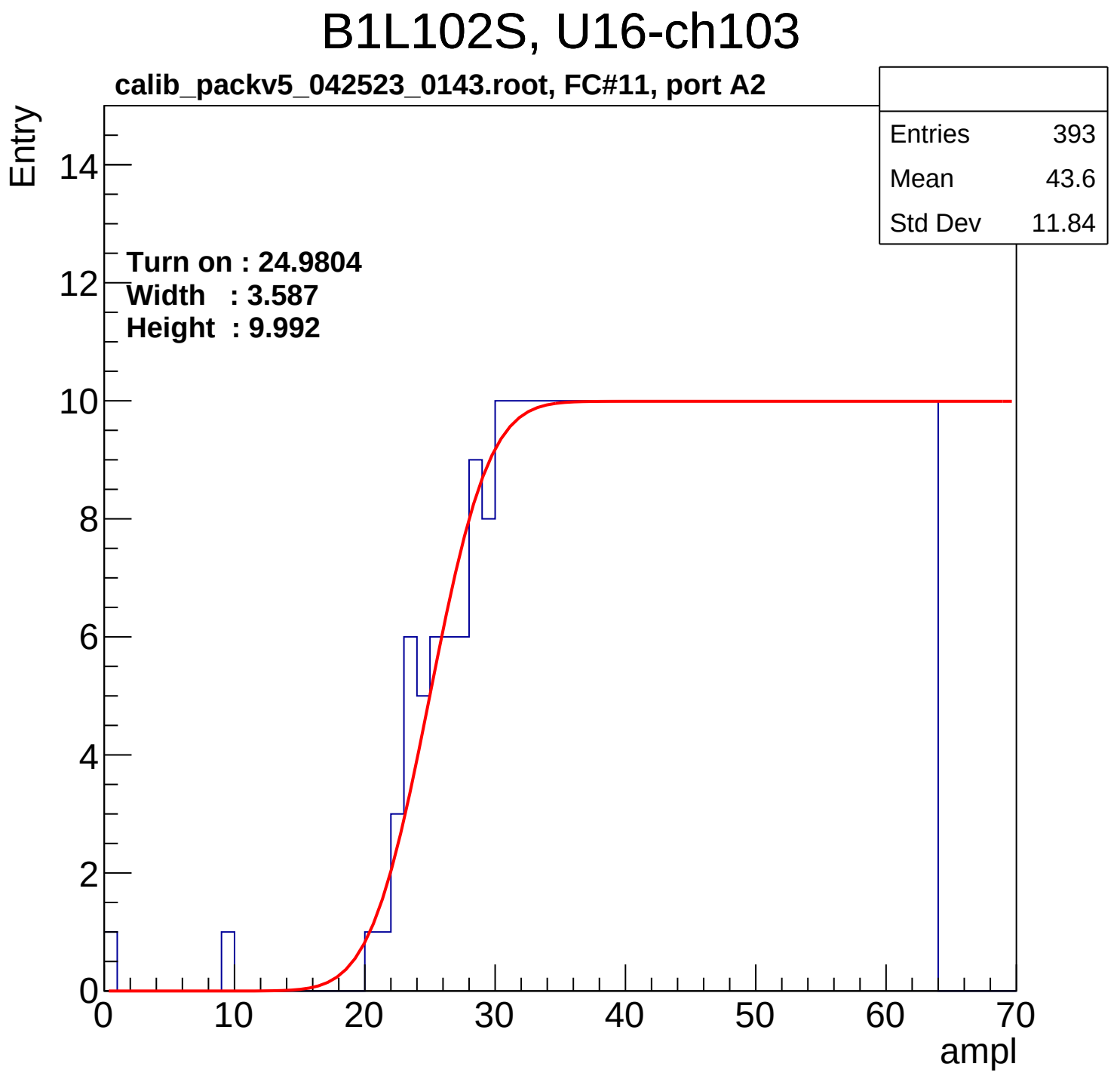

B1L102S, U16-ch98
calib_packv5_042523_0143.root, FC#11, port A2
Entries 403
Mean 43.23
Std Dev 11.89
Turn on : 23.9267
Width : 2.498
Height : 10.025
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

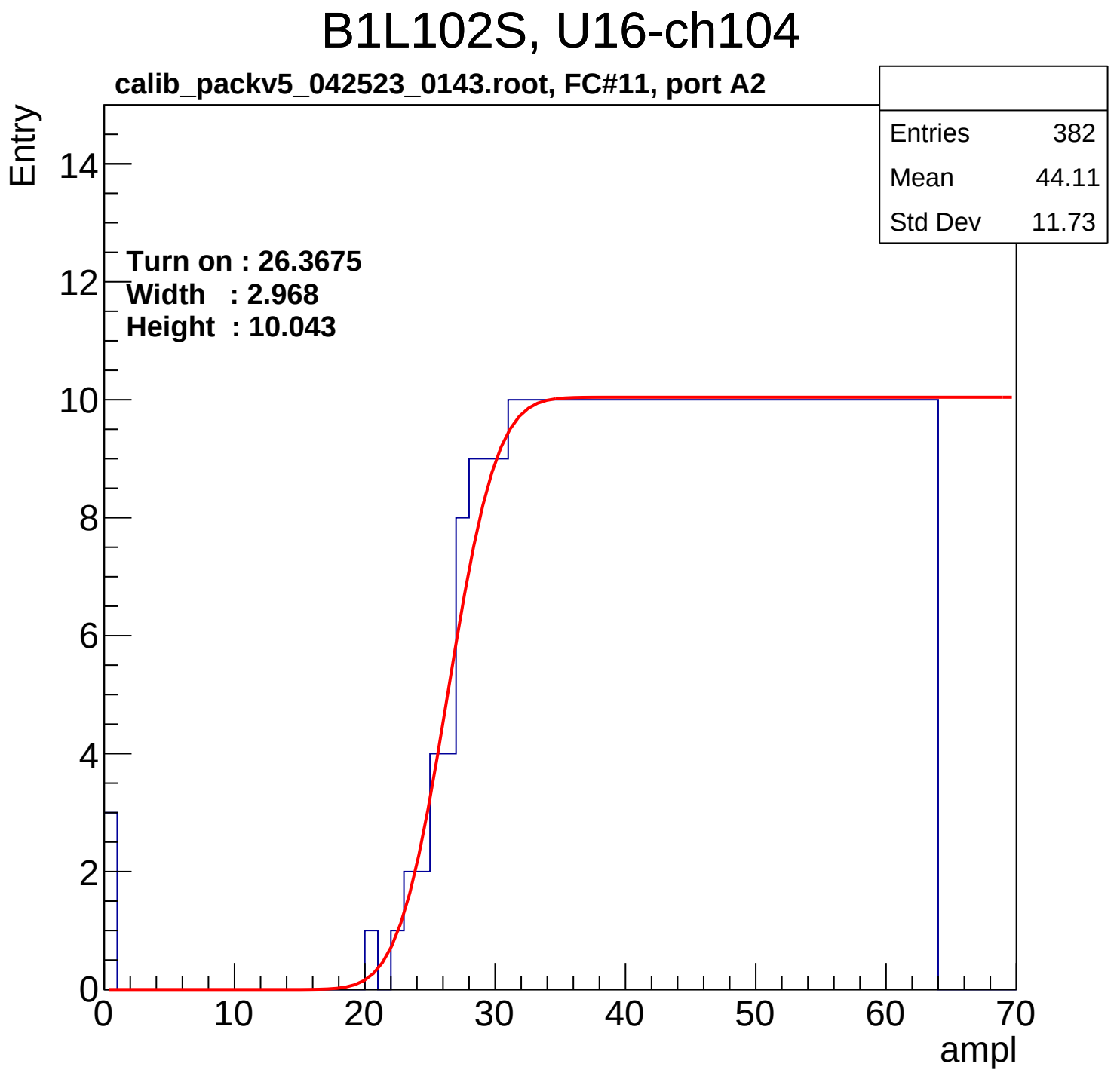

B1L102S, U16-ch99
calib_packv5_042523_0143.root, FC#11, port A2
Entries 396
Mean 43.4
Std Dev 12.1
Turn on : 24.8089
Width : 3.250
Height : 10.001
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

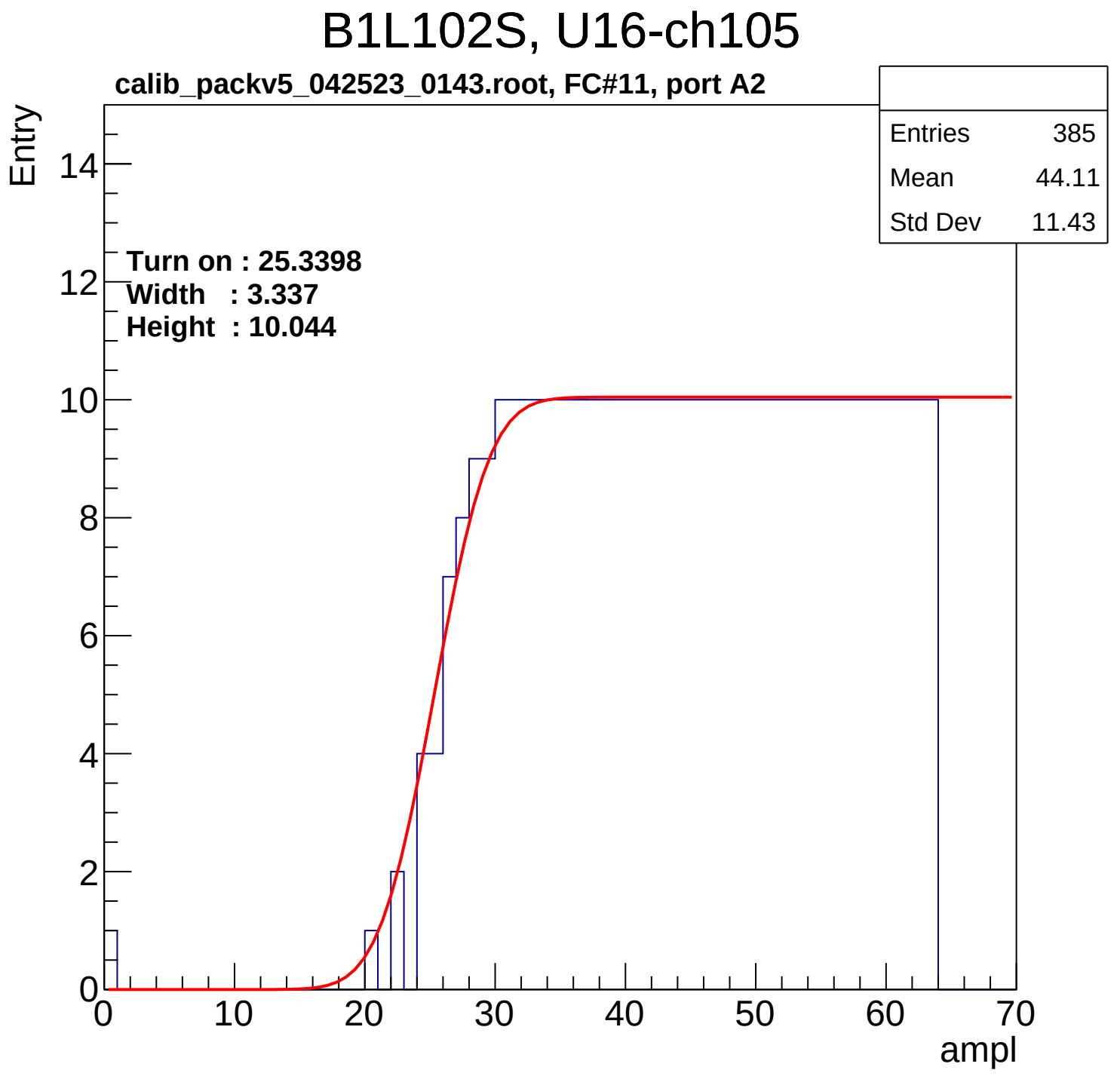

B1L102S, U16-ch100
calib_packv5_042523_0143.root, FC#11, port A2
Entries 406
Mean 42.92
Std Dev 12.35
Turn on : 24.0493
Width : 3.895
Height : 10.068
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

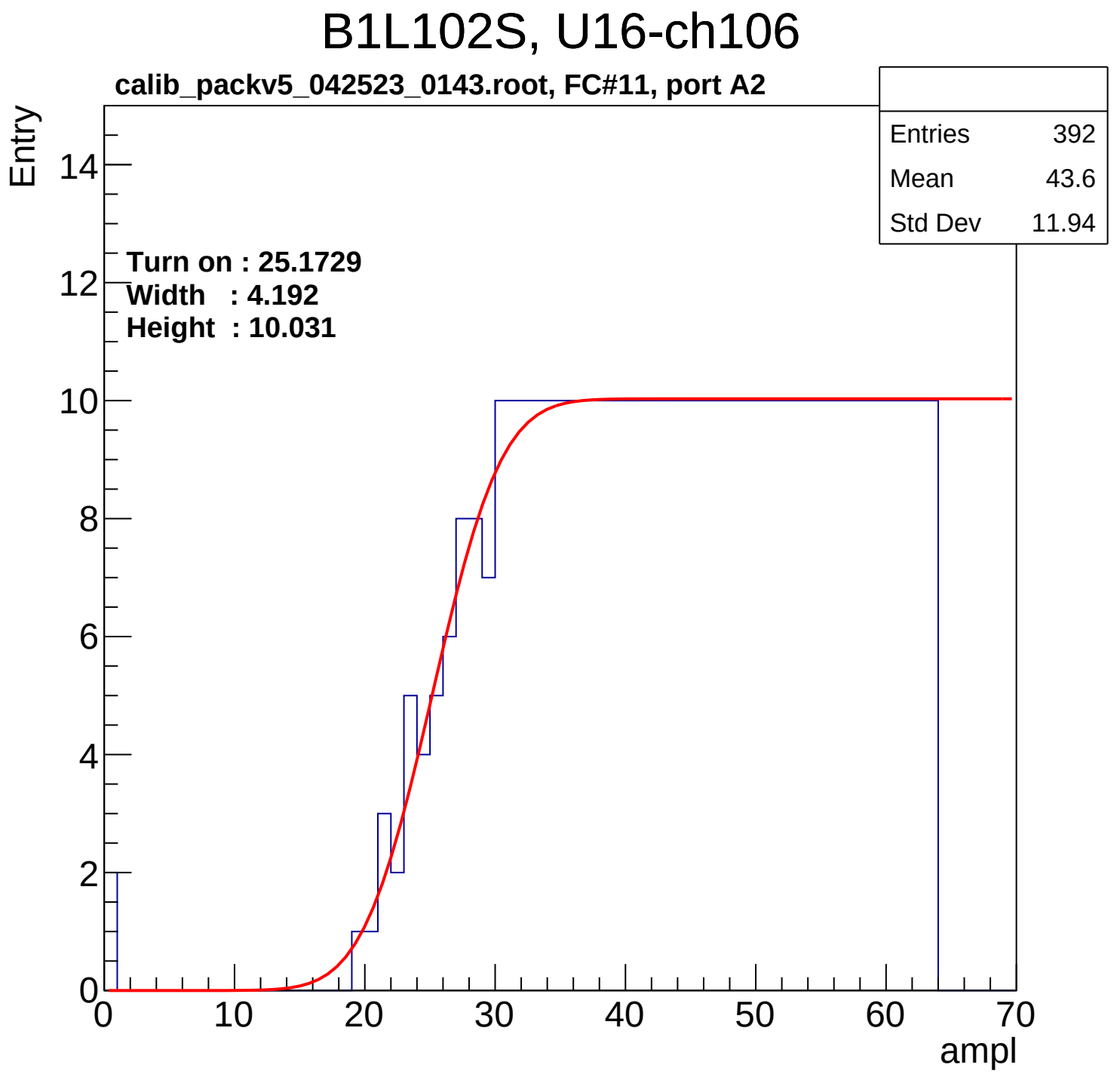

B1L102S, U16-ch101
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 43.72
Std Dev 12.21
Turn on : 26.1192
Width : 3.413
Height : 10.053
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

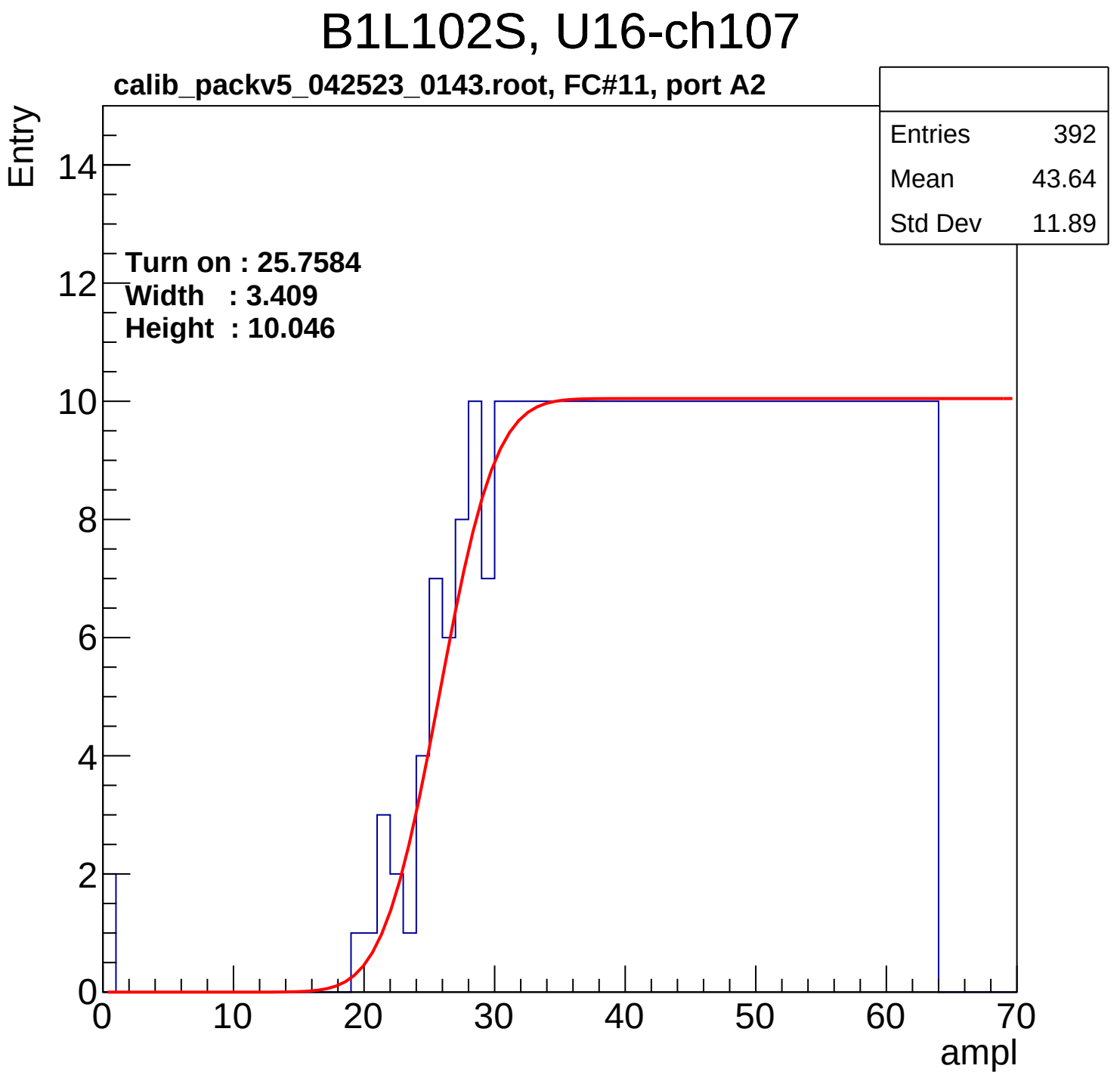

B1L102S, U16-ch102
calib_packv5_042523_0143.root, FC#11, port A2
Entries 400
Mean 43.3
Std Dev 11.95
Turn on : 24.2398
Width : 4.217
Height : 10.058
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

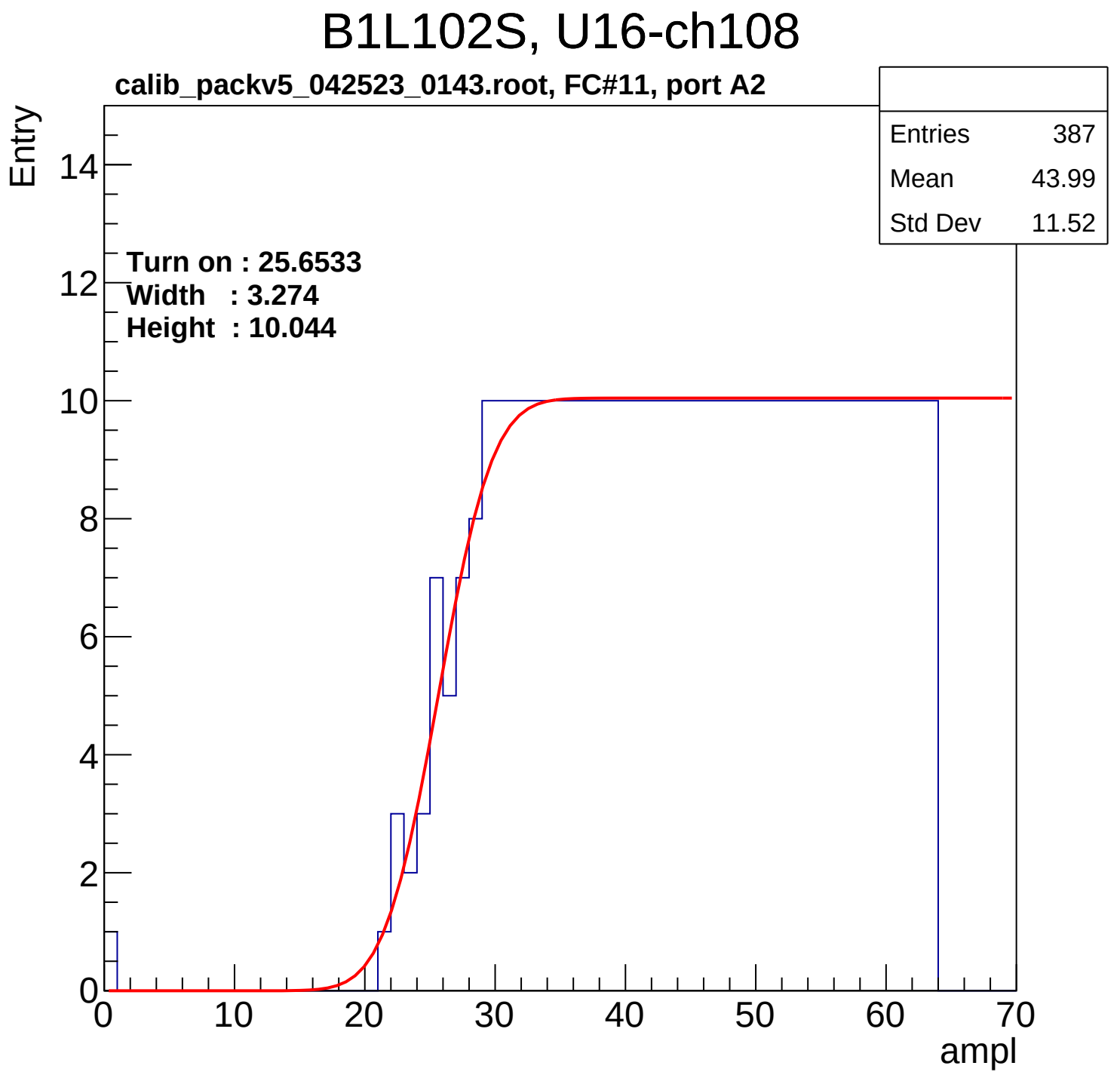

B1L102S, U16-ch103
calib_packv5_042523_0143.root, FC#11, port A2
Entries 393
Mean 43.6
Std Dev 11.84
Turn on : 24.9804
Width : 3.587
Height : 9.992
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

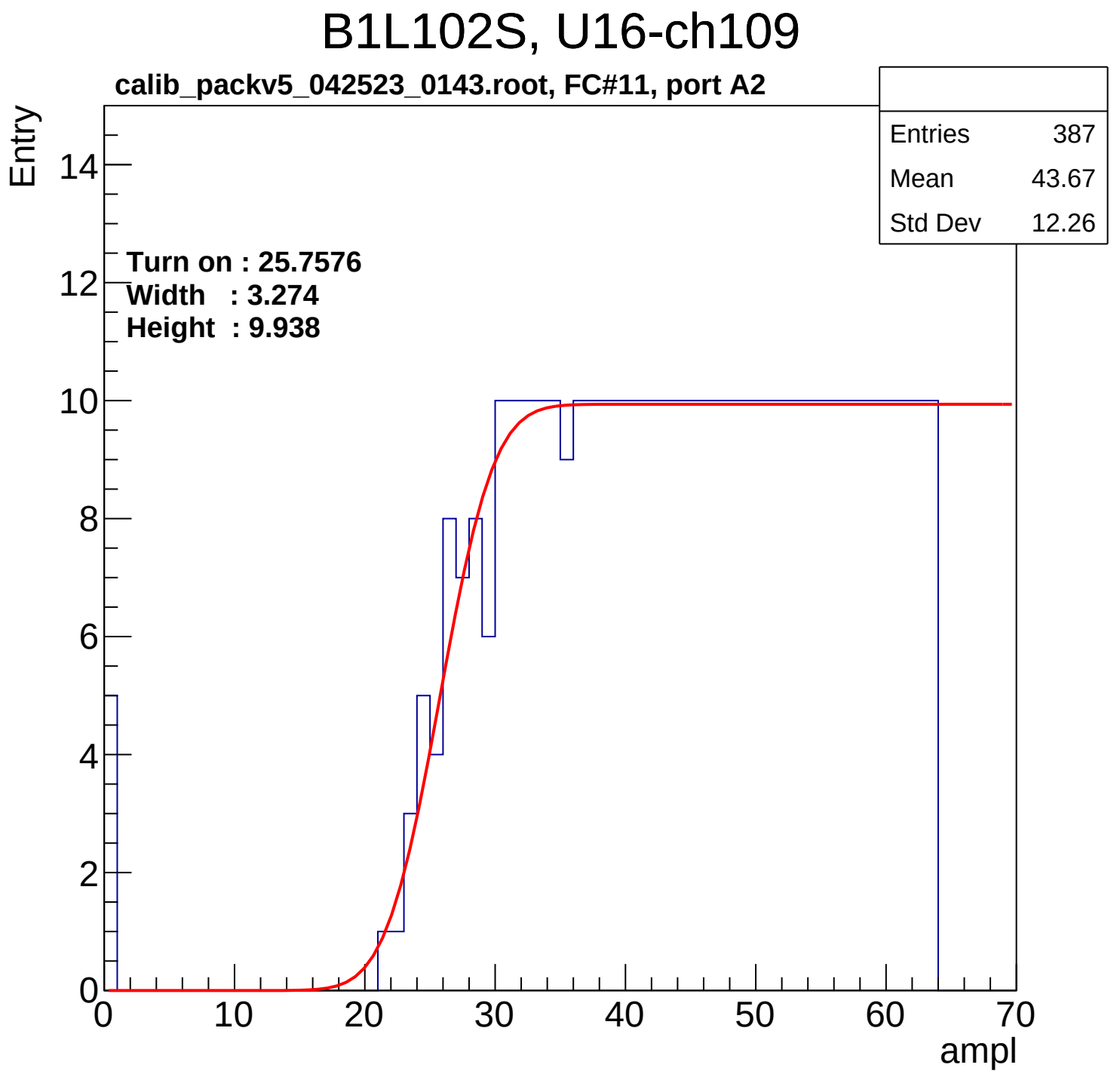

B1L102S, U16-ch104
calib_packv5_042523_0143.root, FC#11, port A2
Entries 382
Mean 44.11
Std Dev 11.73
Turn on : 26.3675
Width : 2.968
Height : 10.043
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

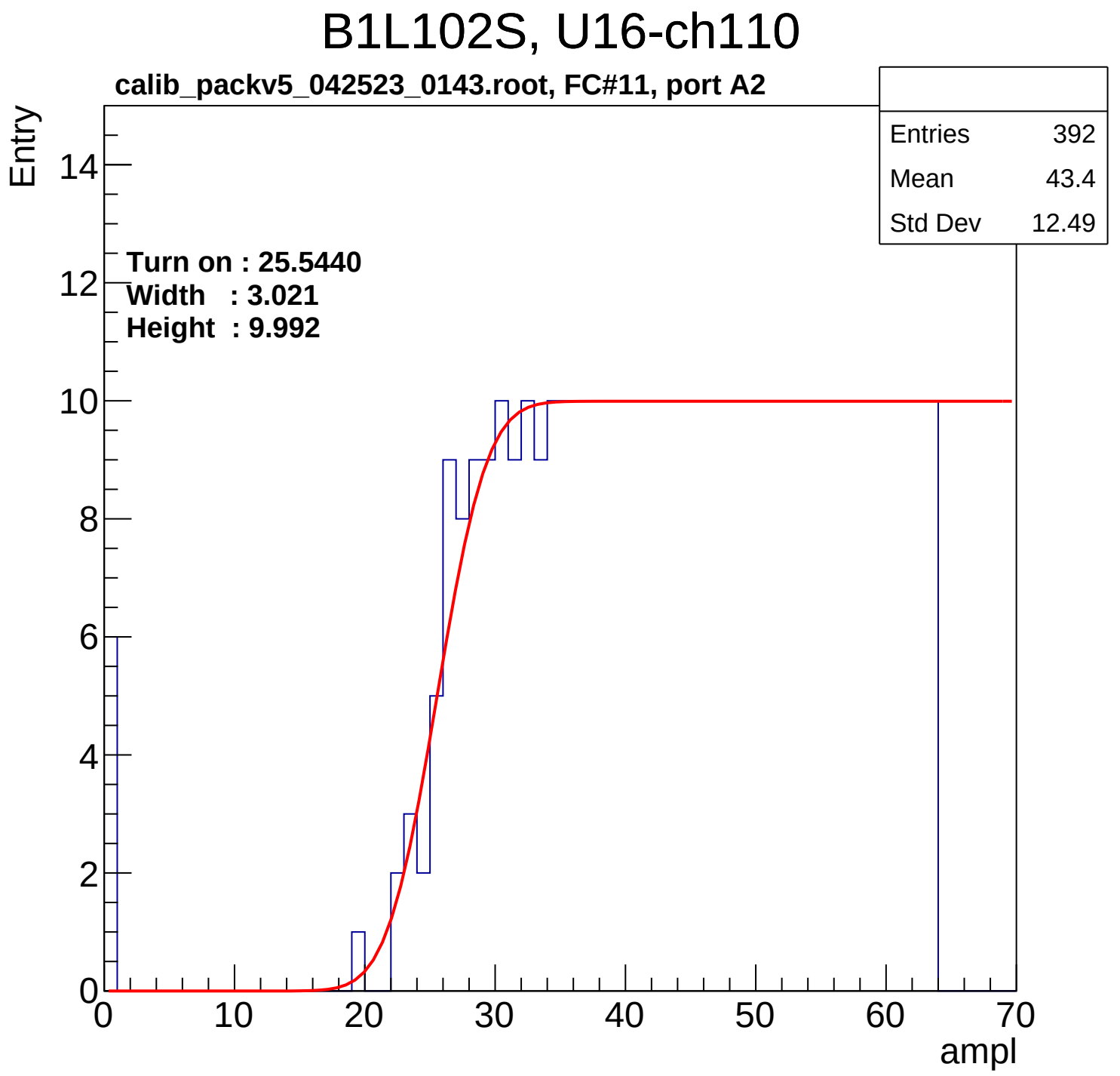

B1L102S, U16-ch105
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 44.11
Std Dev 11.43
Turn on : 25.3398
Width : 3.337
Height : 10.044
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

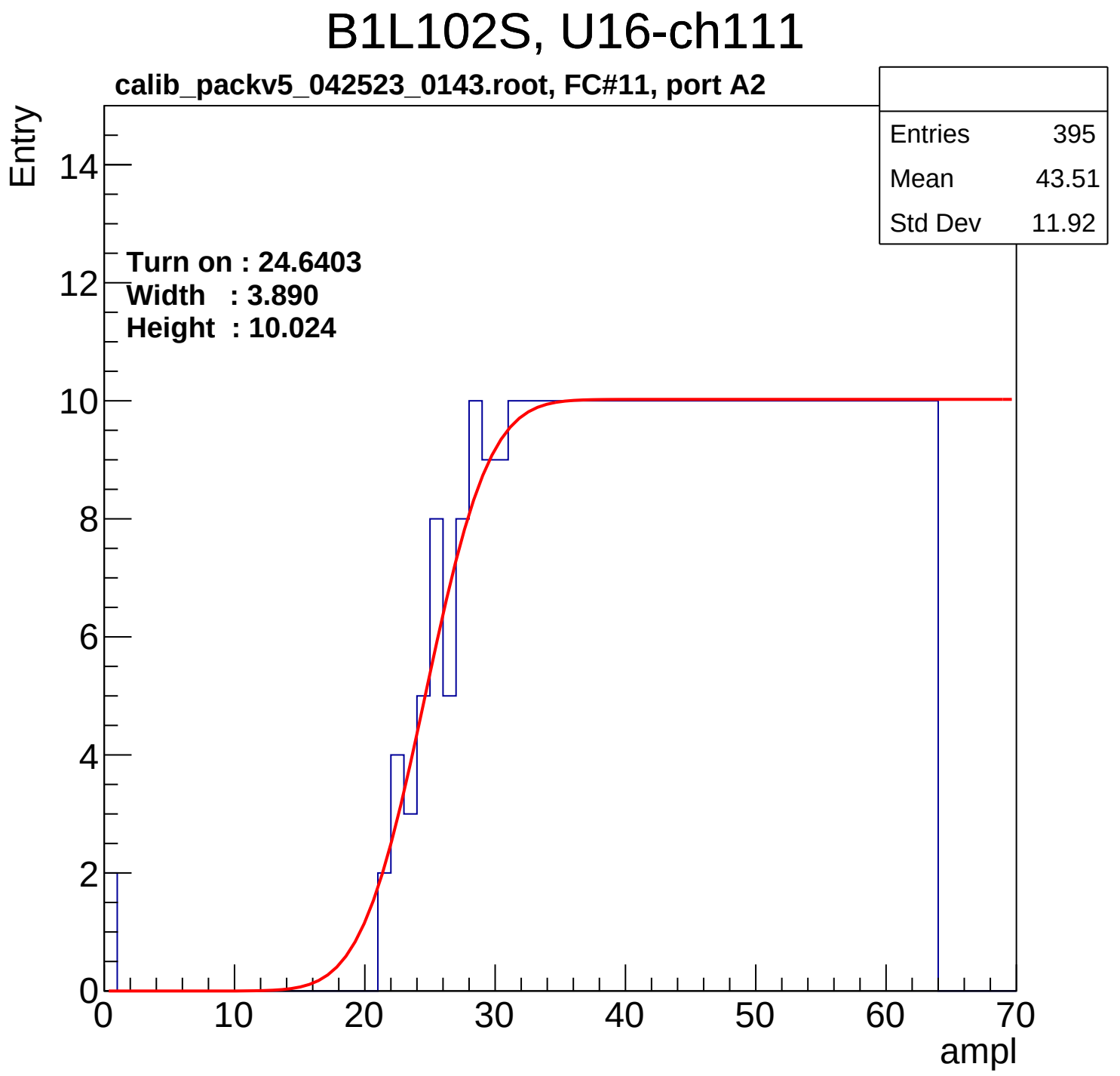

B1L102S, U16-ch106
calib_packv5_042523_0143.root, FC#11, port A2
Entries 392
Mean 43.6
Std Dev 11.94
Turn on : 25.1729
Width : 4.192
Height : 10.031
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

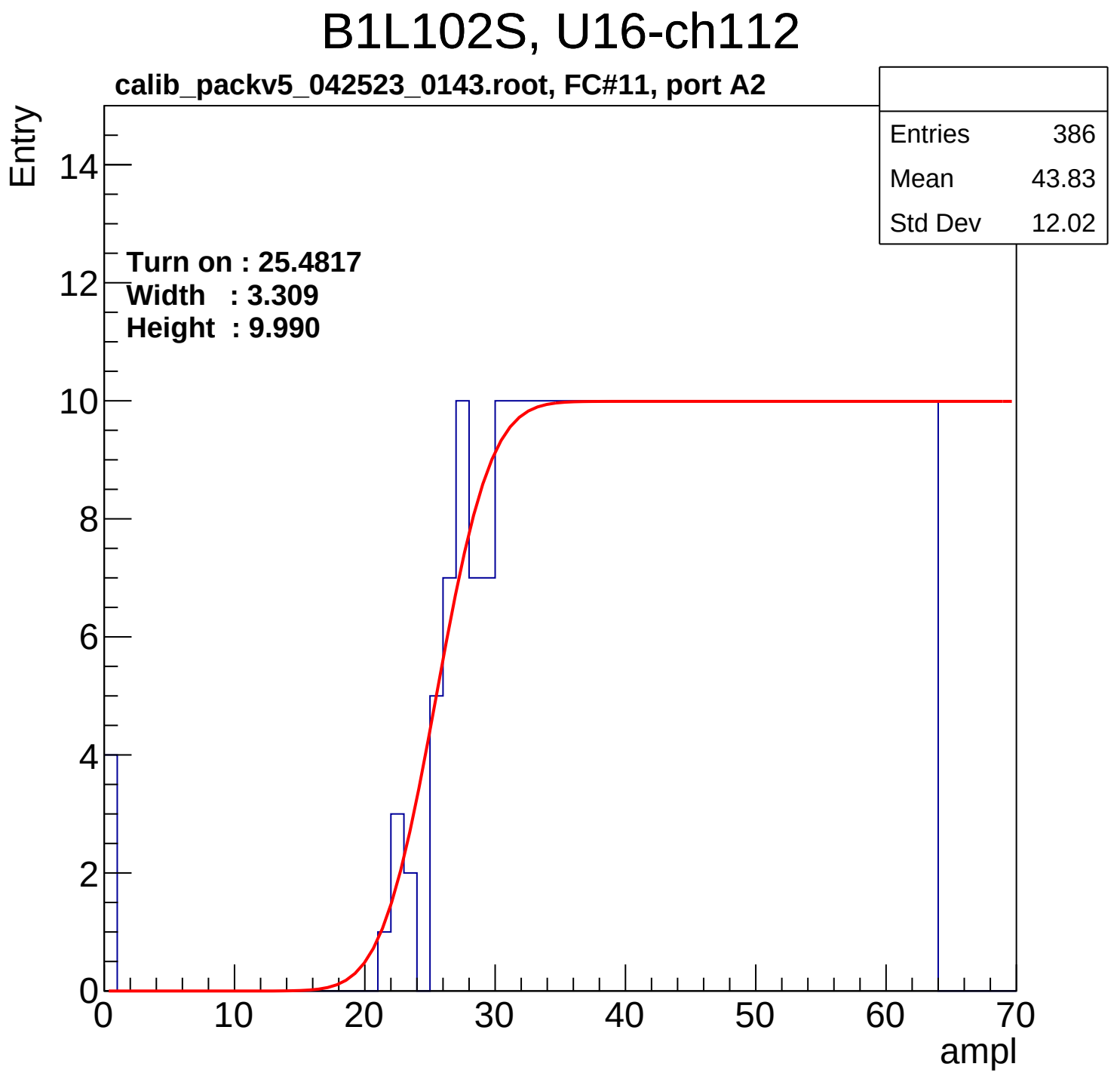

B1L102S, U16-ch107
calib_packv5_042523_0143.root, FC#11, port A2
Entries 392
Mean 43.64
Std Dev 11.89
Turn on : 25.7584
Width : 3.409
Height : 10.046
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

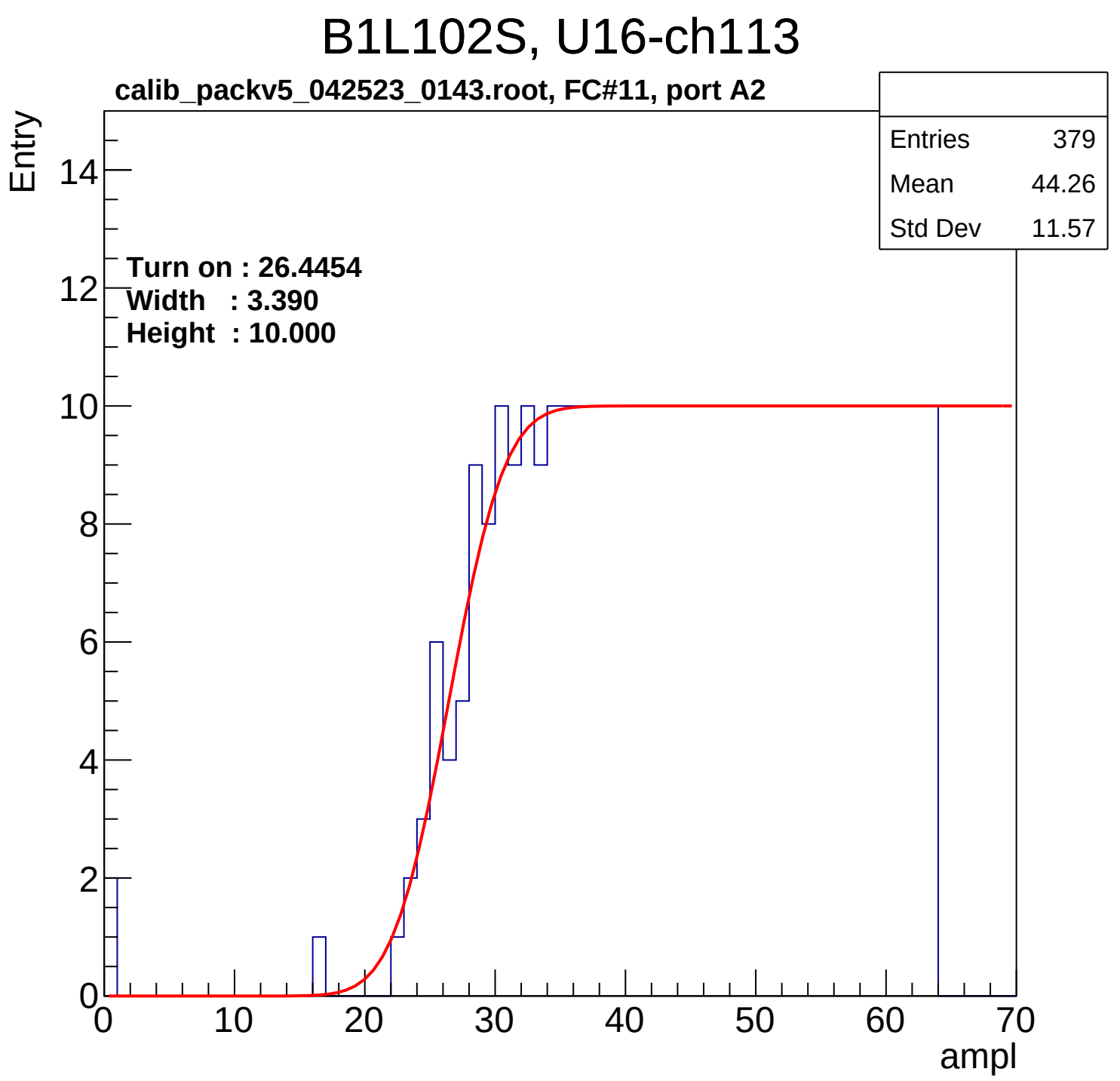

B1L102S, U16-ch108
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 43.99
Std Dev 11.52
Turn on : 25.6533
Width : 3.274
Height : 10.044
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

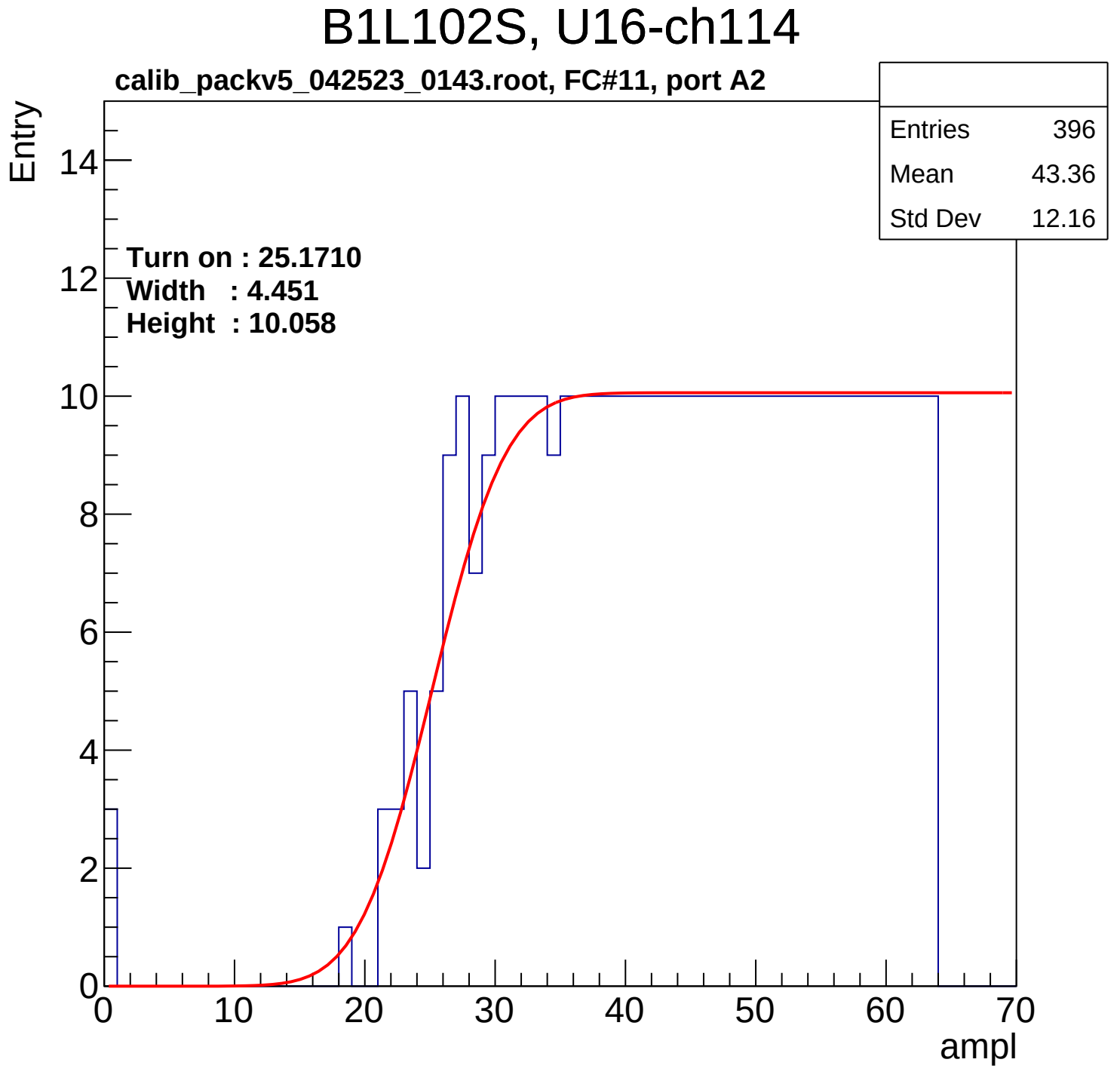

B1L102S, U16-ch109
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 43.67
Std Dev 12.26
Turn on : 25.7576
Width : 3.274
Height : 9.938
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

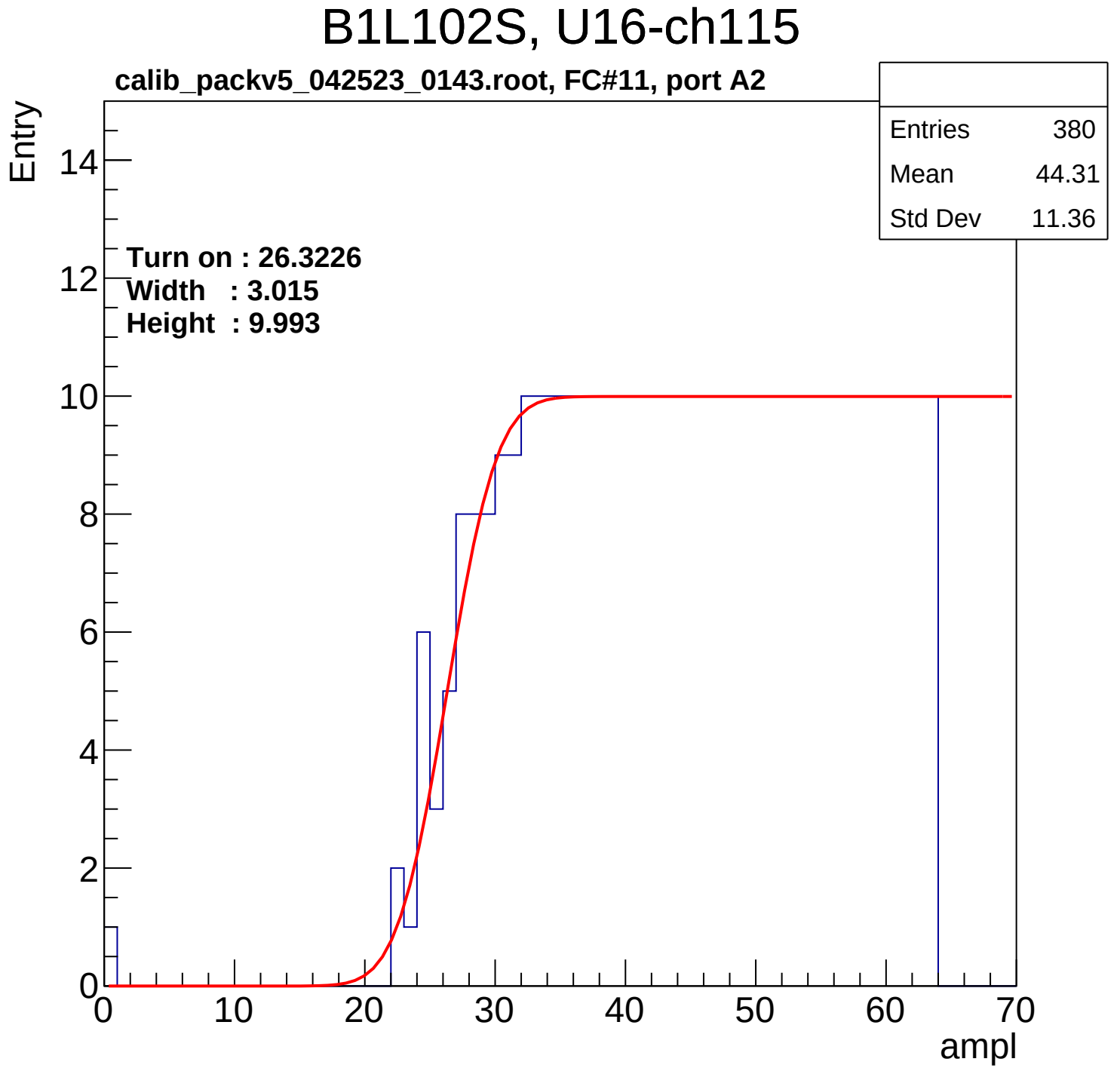

B1L102S, U16-ch110
calib_packv5_042523_0143.root, FC#11, port A2
Entries 392
Mean 43.4
Std Dev 12.49
Turn on : 25.5440
Width : 3.021
Height : 9.992
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

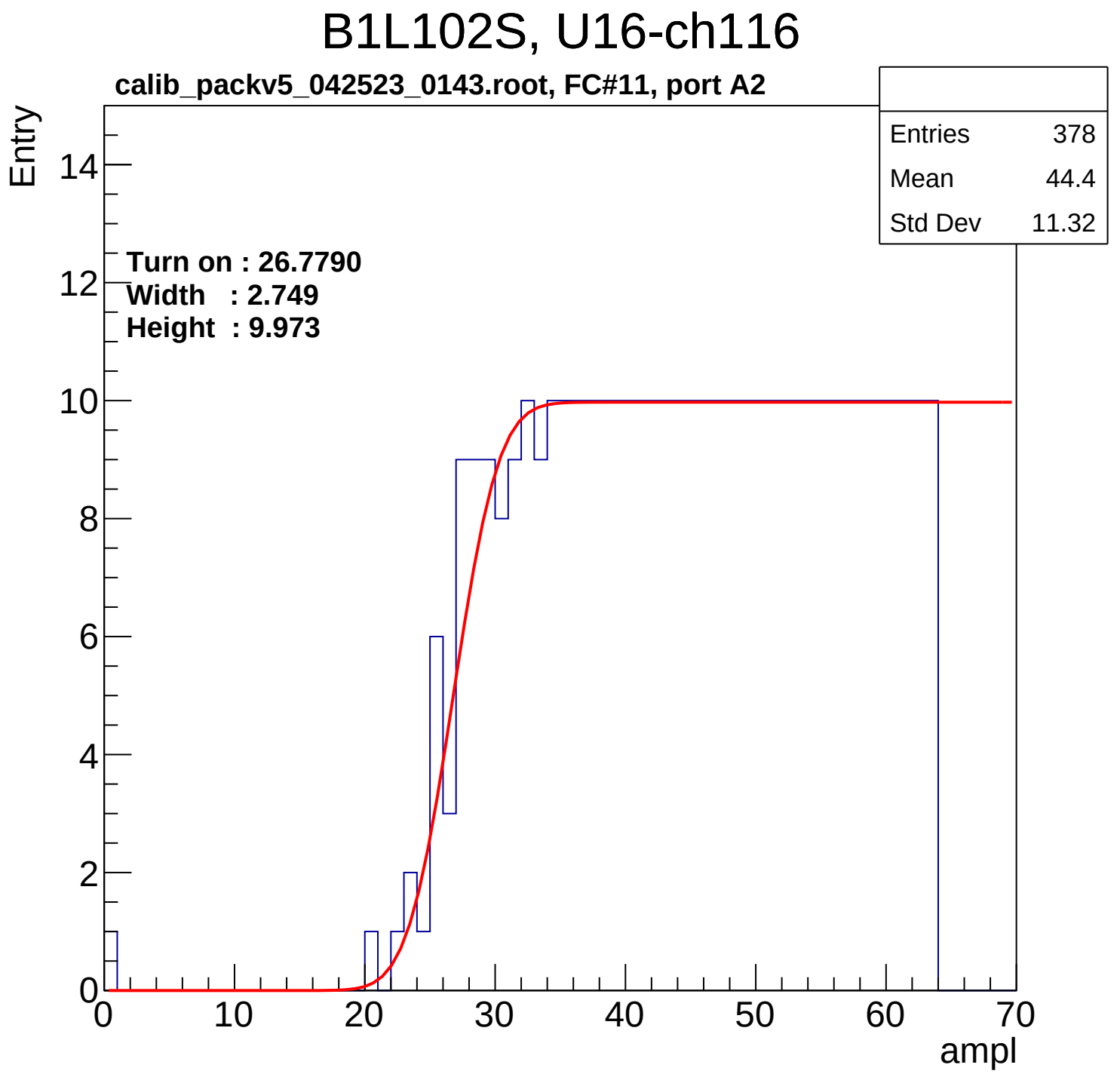

B1L102S, U16-ch111
calib_packv5_042523_0143.root, FC#11, port A2
Entries 395
Mean 43.51
Std Dev 11.92
Turn on : 24.6403
Width : 3.890
Height : 10.024
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

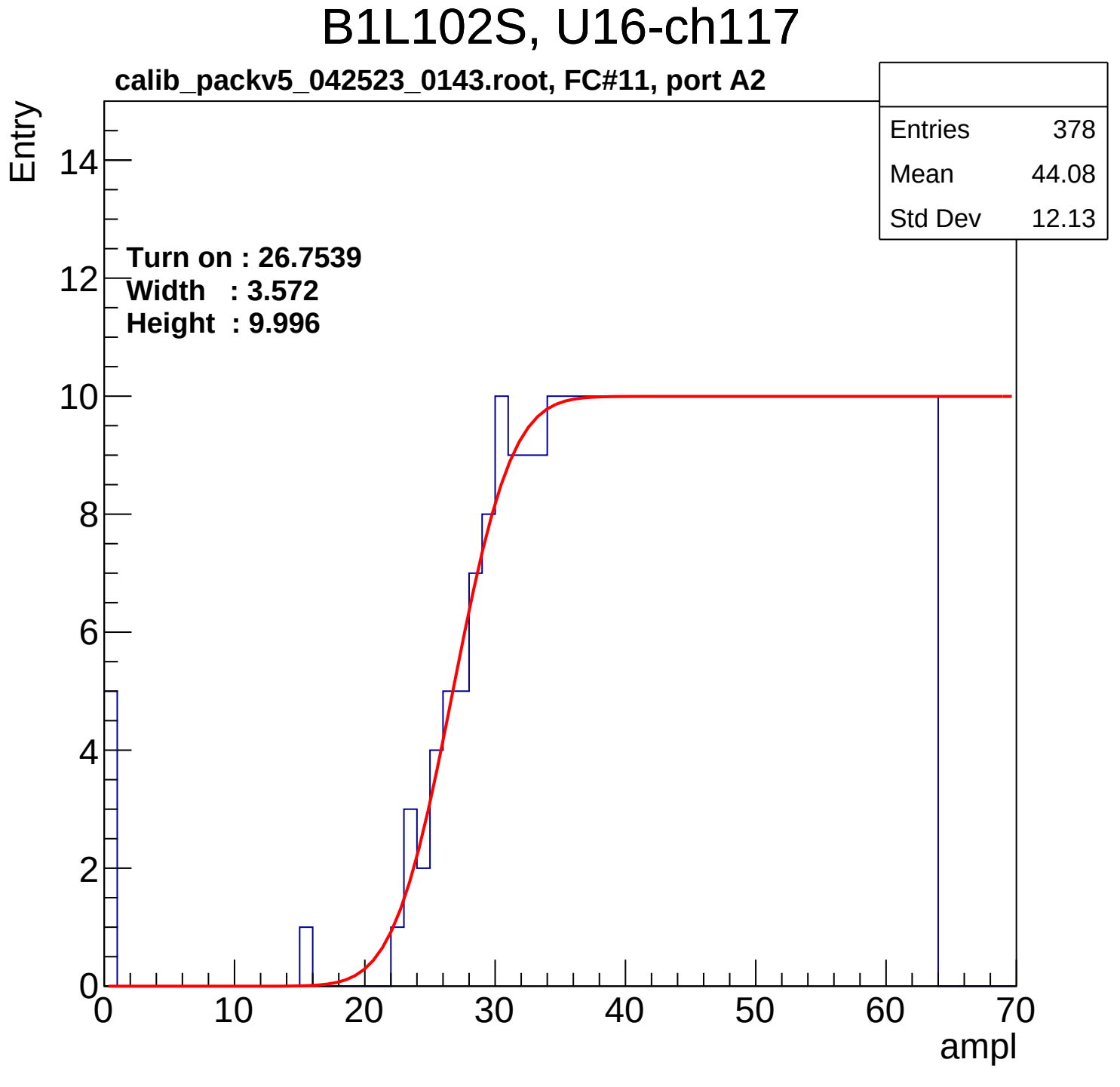

B1L102S, U16-ch112
calib_packv5_042523_0143.root, FC#11, port A2
Entries 386
Mean 43.83
Std Dev 12.02
Turn on : 25.4817
Width : 3.309
Height : 9.990
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

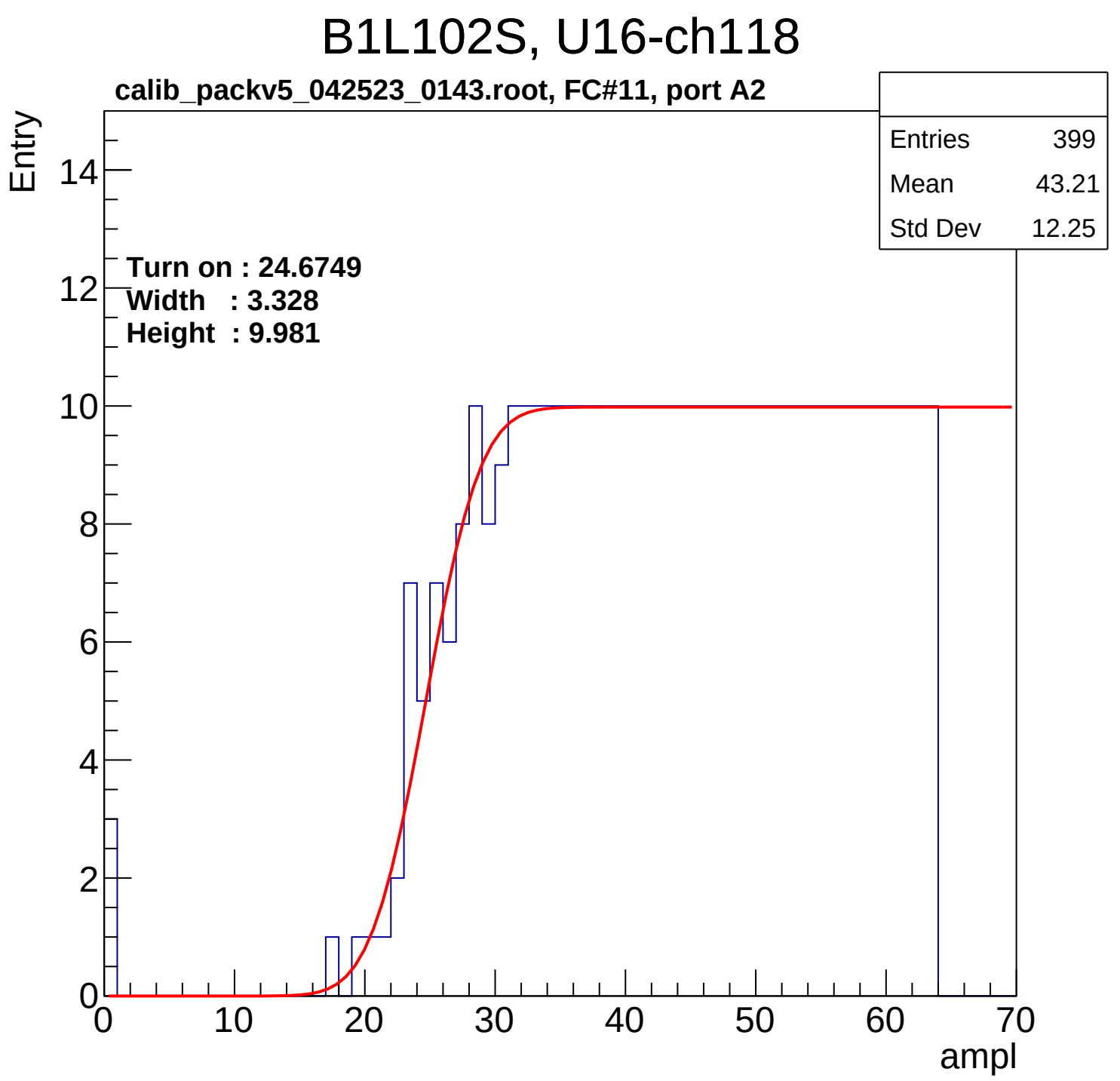

B1L102S, U16-ch113
calib_packv5_042523_0143.root, FC#11, port A2
Entries 379
Mean 44.26
Std Dev 11.57
Turn on : 26.4454
Width : 3.390
Height : 10.000
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

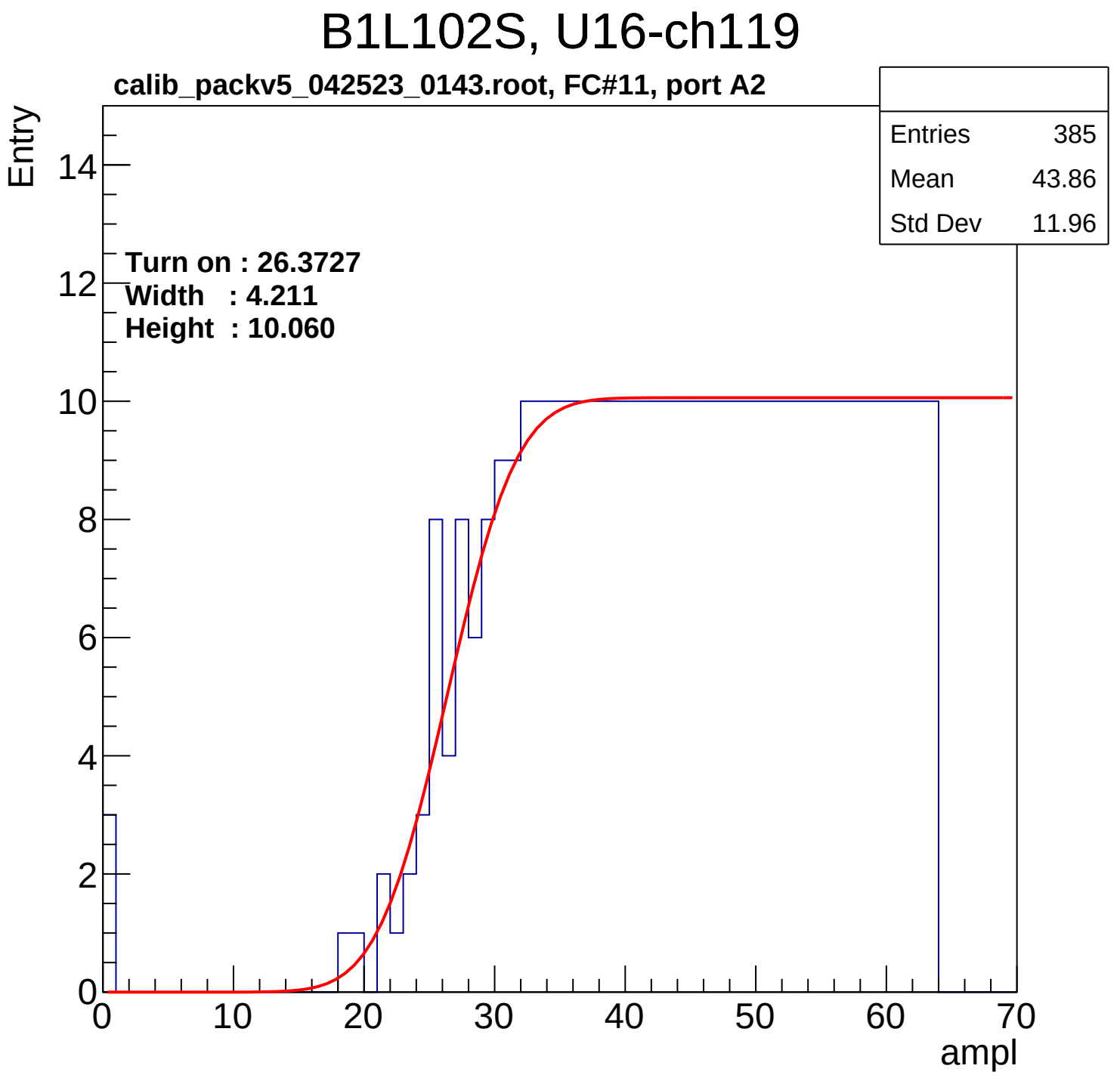

B1L102S, U16-ch114
calib_packv5_042523_0143.root, FC#11, port A2
Entries 396
Mean 43.36
Std Dev 12.16
Turn on : 25.1710
Width : 4.451
Height : 10.058
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

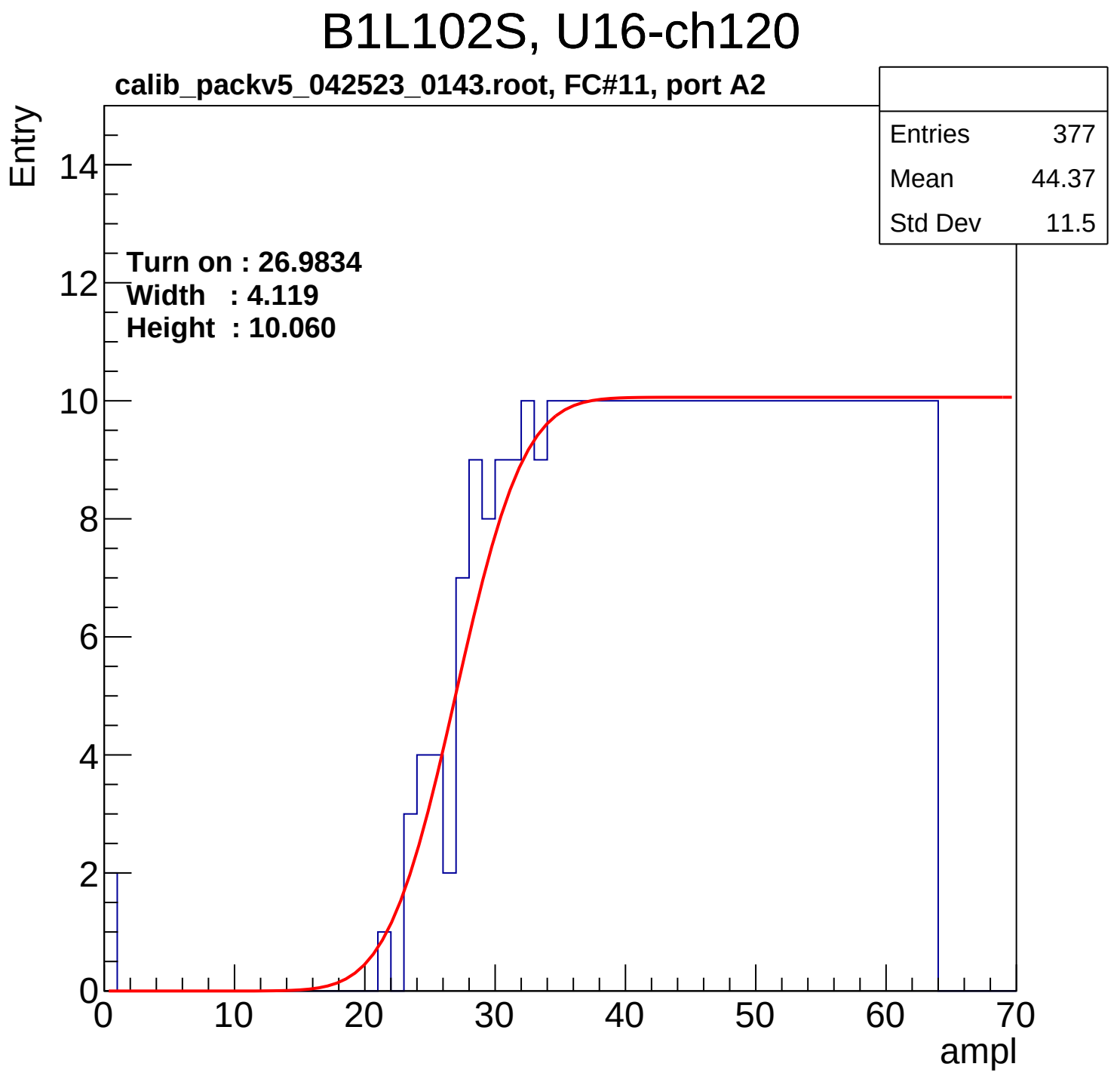

B1L102S, U16-ch115
calib_packv5_042523_0143.root, FC#11, port A2
Entries 380
Mean 44.31
Std Dev 11.36
Turn on : 26.3226
Width : 3.015
Height : 9.993
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

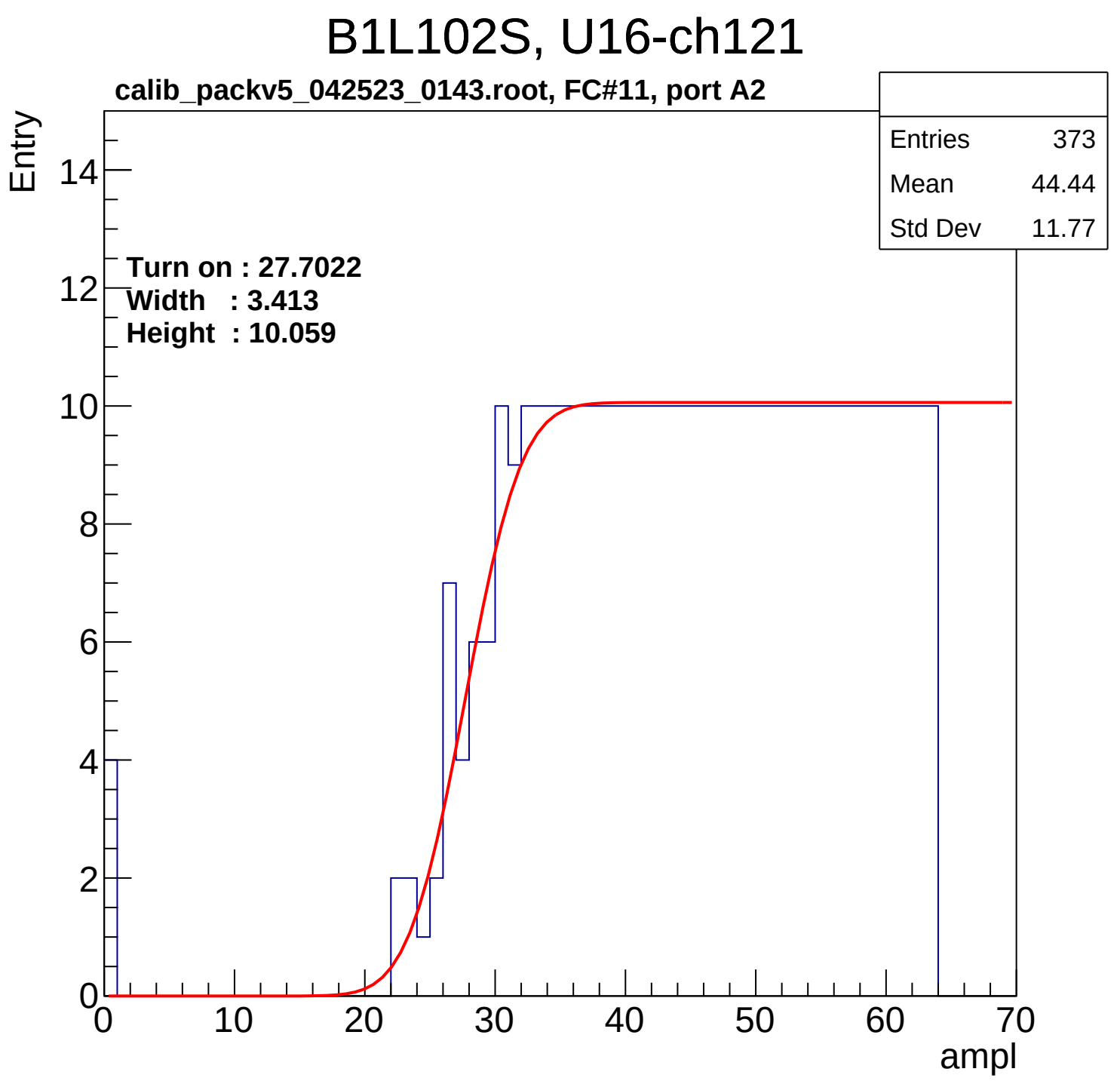

B1L102S, U16-ch116
calib_packv5_042523_0143.root, FC#11, port A2
Entries 378
Mean 44.4
Std Dev 11.32
Turn on : 26.7790
Width : 2.749
Height : 9.973
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

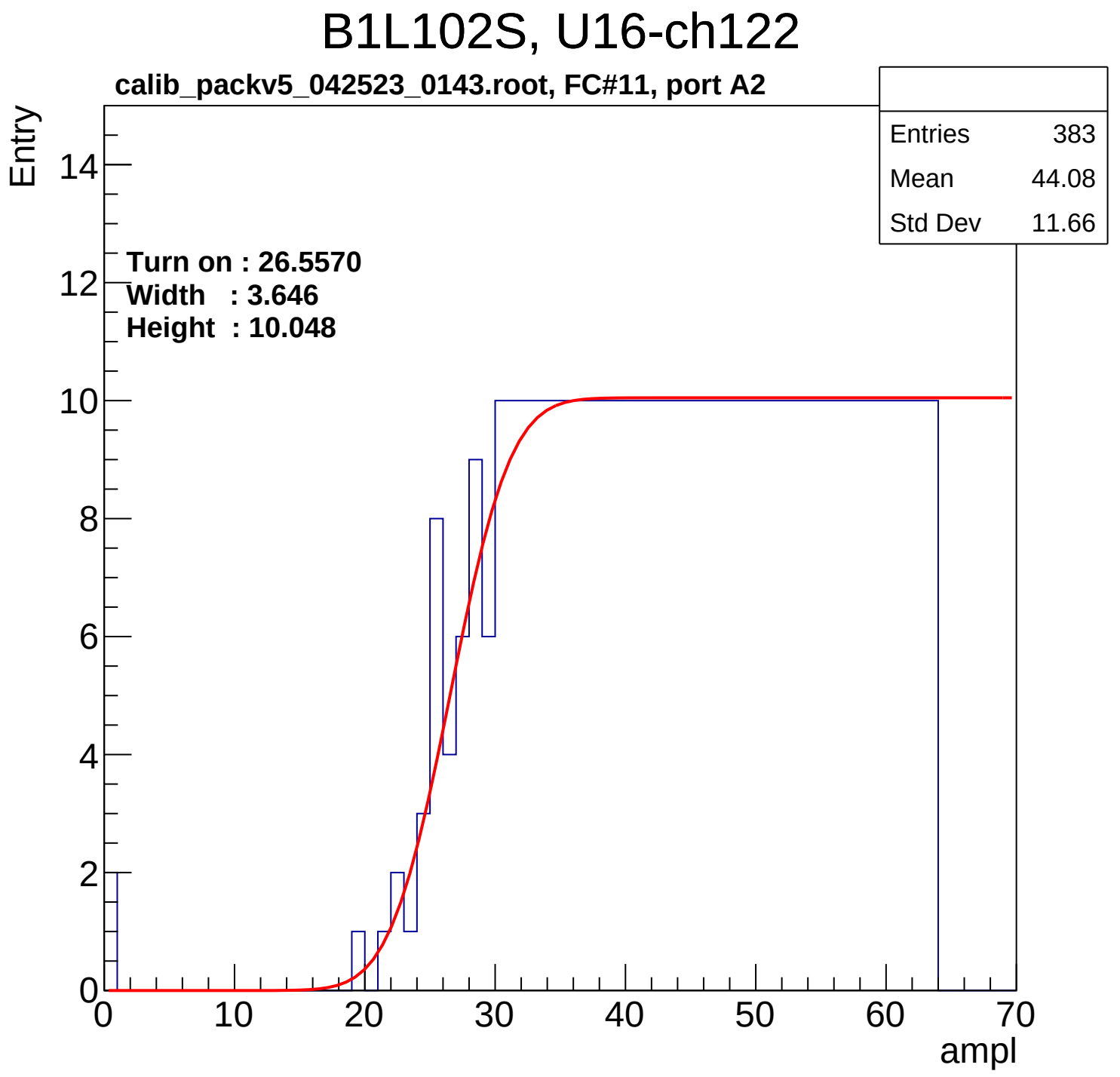

B1L102S, U16-ch117
calib_packv5_042523_0143.root, FC#11, port A2
Entries 378
Mean 44.08
Std Dev 12.13
Turn on : 26.7539
Width : 3.572
Height : 9.996
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

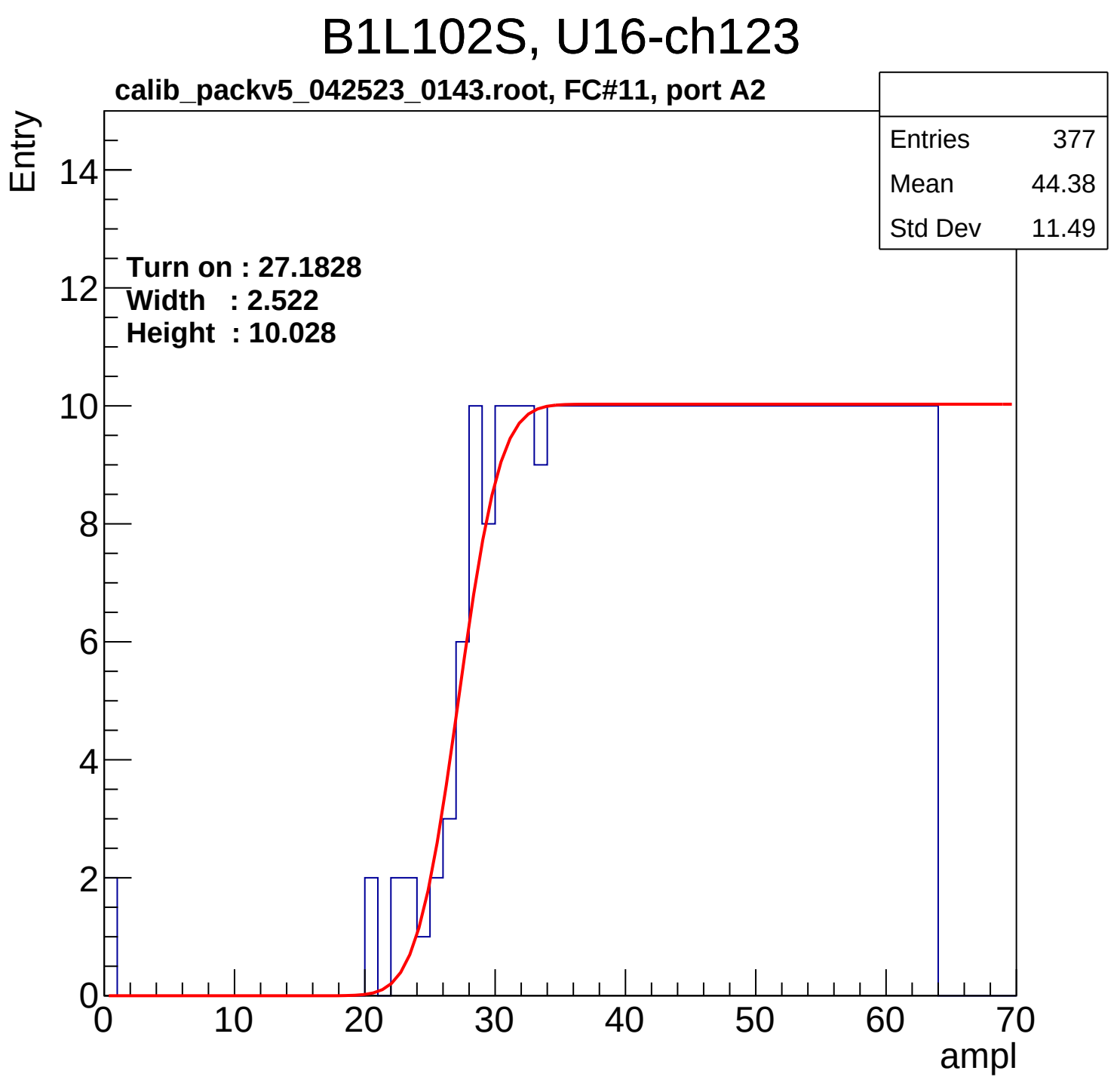

B1L102S, U16-ch118
calib_packv5_042523_0143.root, FC#11, port A2
Entries 399
Mean 43.21
Std Dev 12.25
Turn on : 24.6749
Width : 3.328
Height : 9.981
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

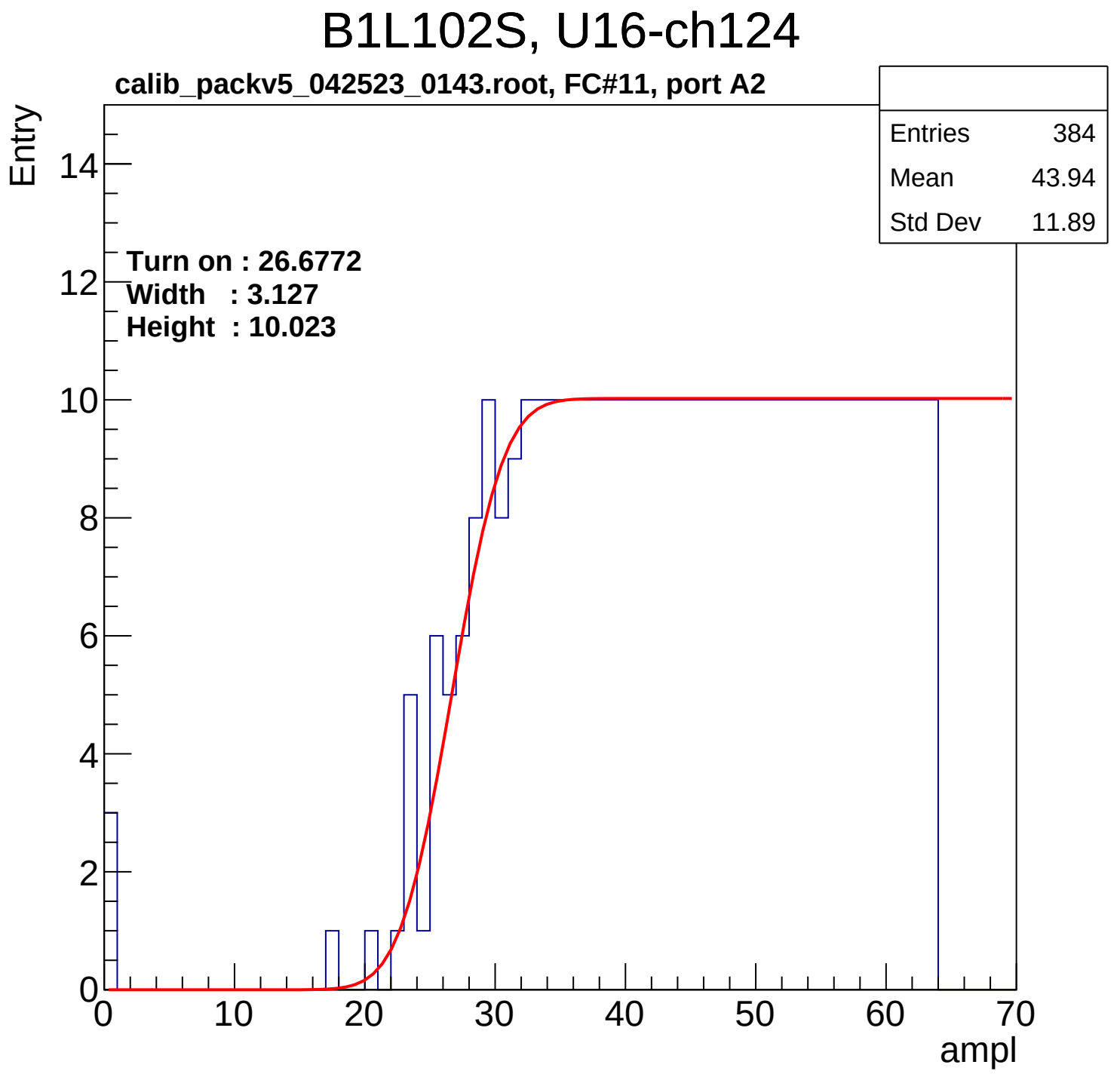

B1L102S, U16-ch119
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 43.86
Std Dev 11.96
Turn on : 26.3727
Width : 4.211
Height : 10.060
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

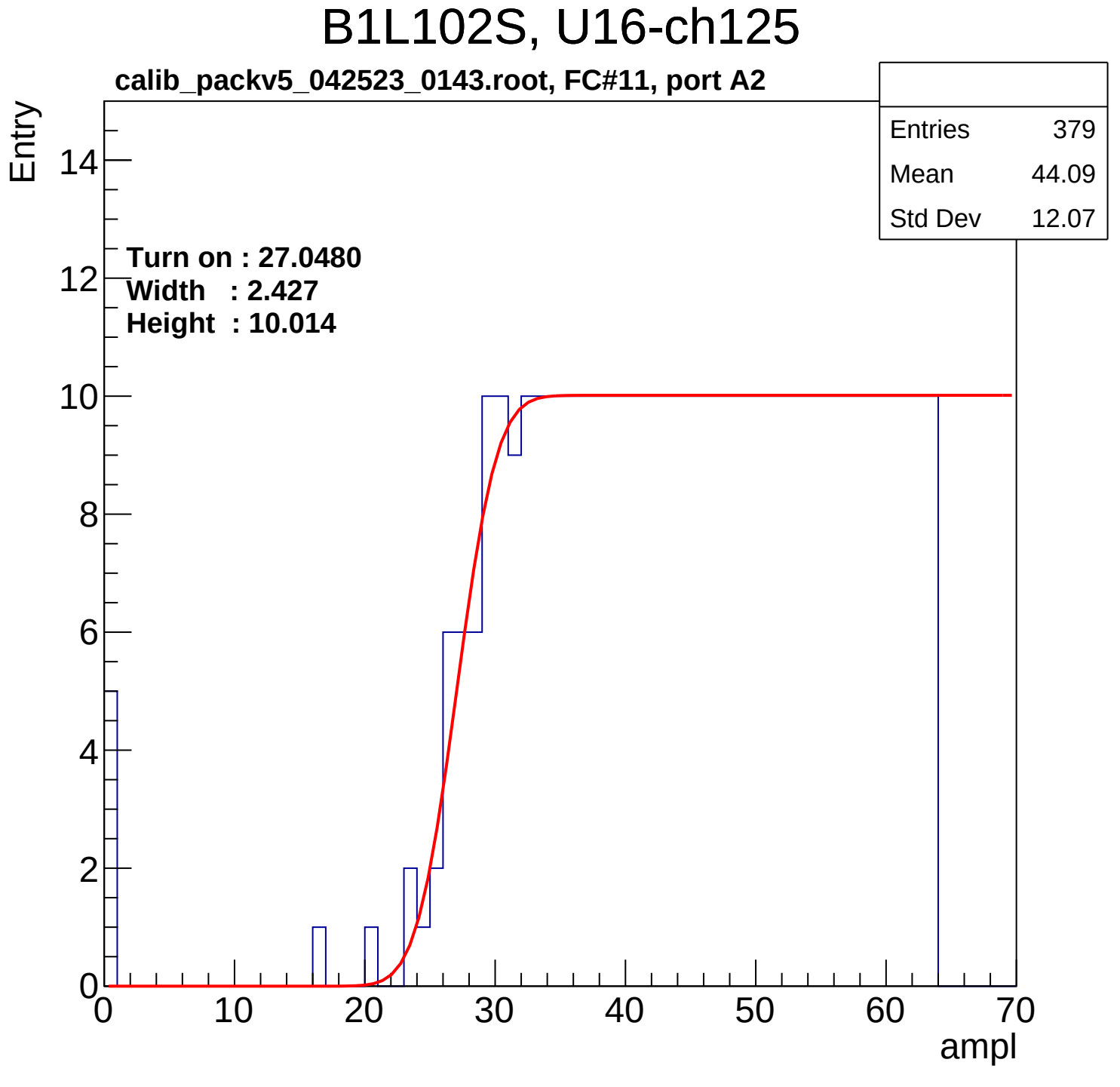

B1L102S, U16-ch120
calib_packv5_042523_0143.root, FC#11, port A2
Entries 377
Mean 44.37
Std Dev 11.5
Turn on : 26.9834
Width : 4.119
Height : 10.060
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

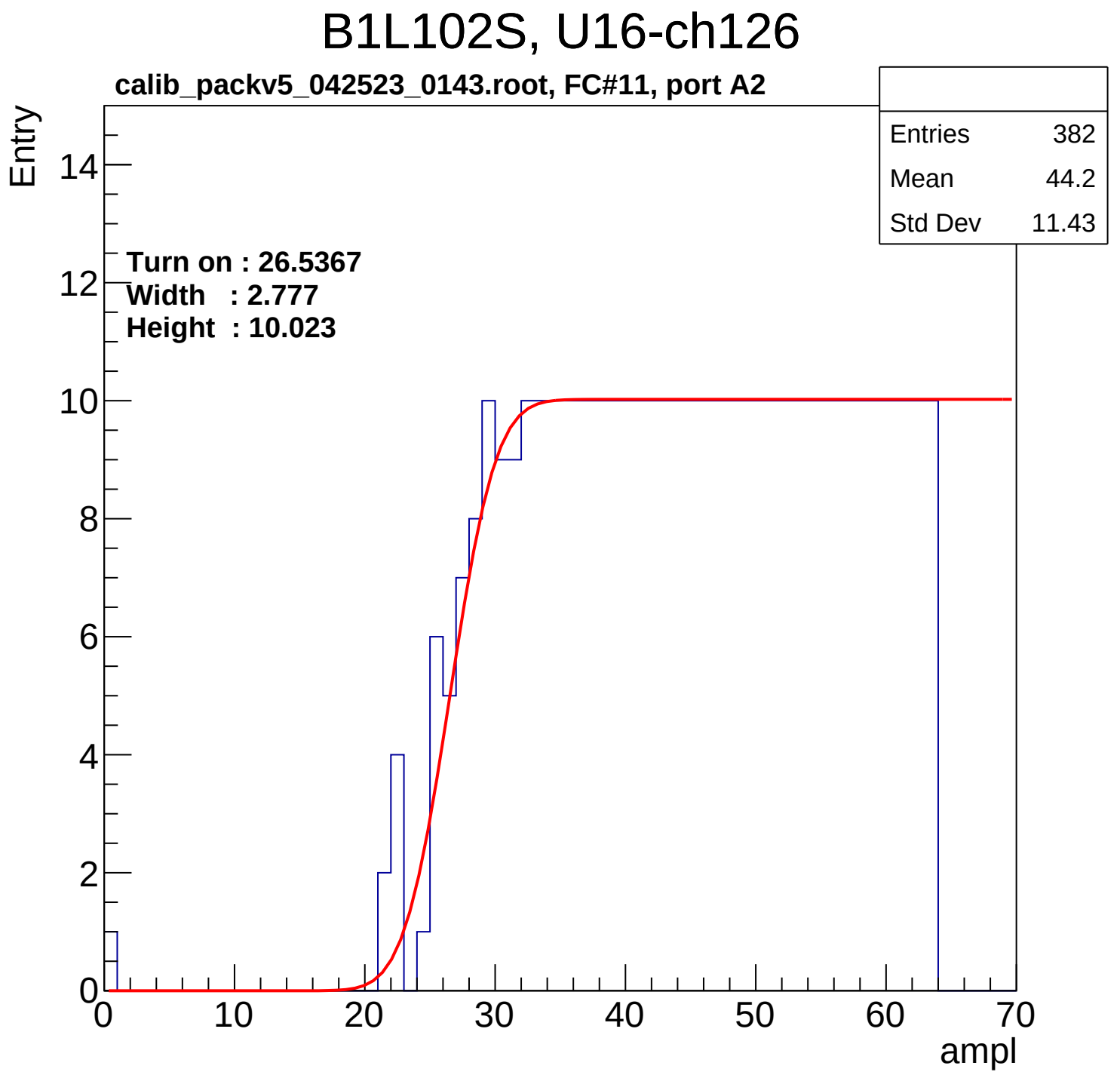

B1L102S, U16-ch121
calib_packv5_042523_0143.root, FC#11, port A2
Entries 373
Mean 44.44
Std Dev 11.77
Turn on : 27.7022
Width : 3.413
Height : 10.059
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

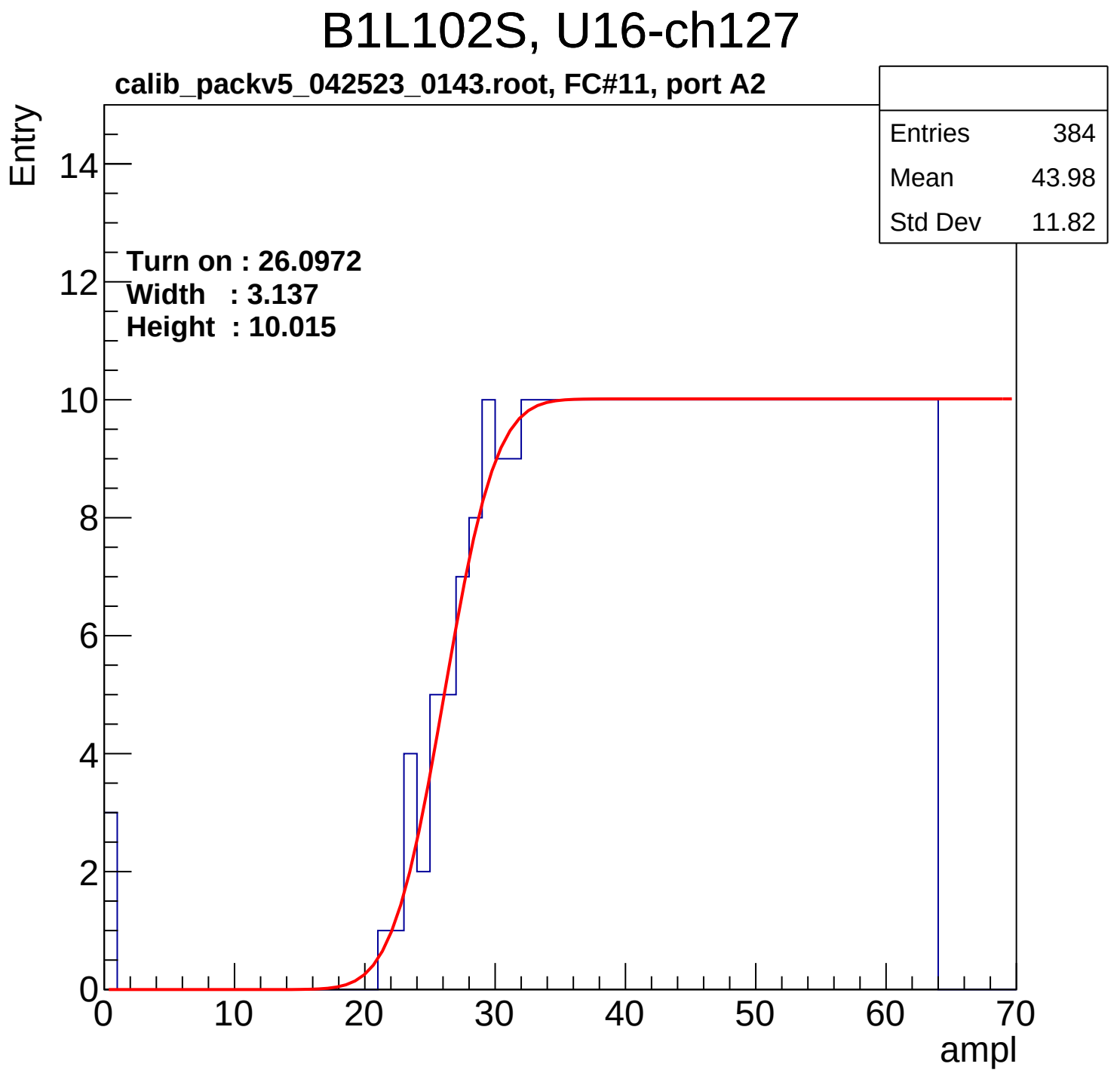

B1L102S, U16-ch122
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 44.08
Std Dev 11.66
Turn on : 26.5570
Width : 3.646
Height : 10.048
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

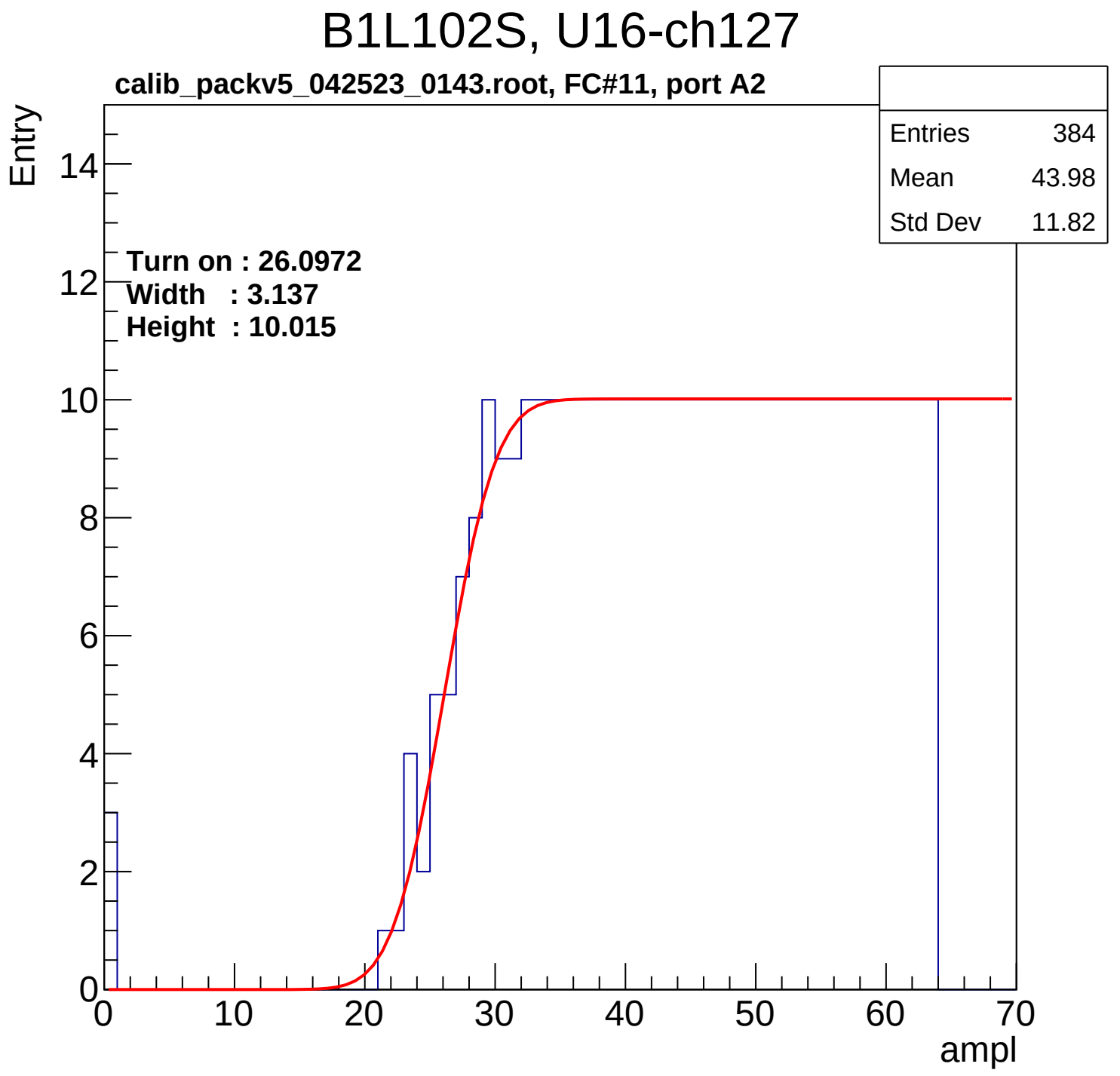

B1L102S, U16-ch123
calib_packv5_042523_0143.root, FC#11, port A2
Entries 377
Mean 44.38
Std Dev 11.49
Turn on : 27.1828
Width : 2.522
Height : 10.028
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L102S, U16-ch124
calib_packv5_042523_0143.root, FC#11, port A2
Entries 384
Mean 43.94
Std Dev 11.89
Turn on : 26.6772
Width : 3.127
Height : 10.023
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L102S, U16-ch125
calib_packv5_042523_0143.root, FC#11, port A2
Entries 379
Mean 44.09
Std Dev 12.07
Turn on : 27.0480
Width : 2.427
Height : 10.014
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L102S, U16-ch126
calib_packv5_042523_0143.root, FC#11, port A2
Entries 382
Mean 44.2
Std Dev 11.43
Turn on : 26.5367
Width : 2.777
Height : 10.023
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L102S, U16-ch127
calib_packv5_042523_0143.root, FC#11, port A2
Entries 384
Mean 43.98
Std Dev 11.82
Turn on : 26.0972
Width : 3.137
Height : 10.015
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L102S, U16-ch127
calib_packv5_042523_0143.root, FC#11, port A2
Entries 384
Mean 43.98
Std Dev 11.82
Turn on : 26.0972
Width : 3.137
Height : 10.015
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70