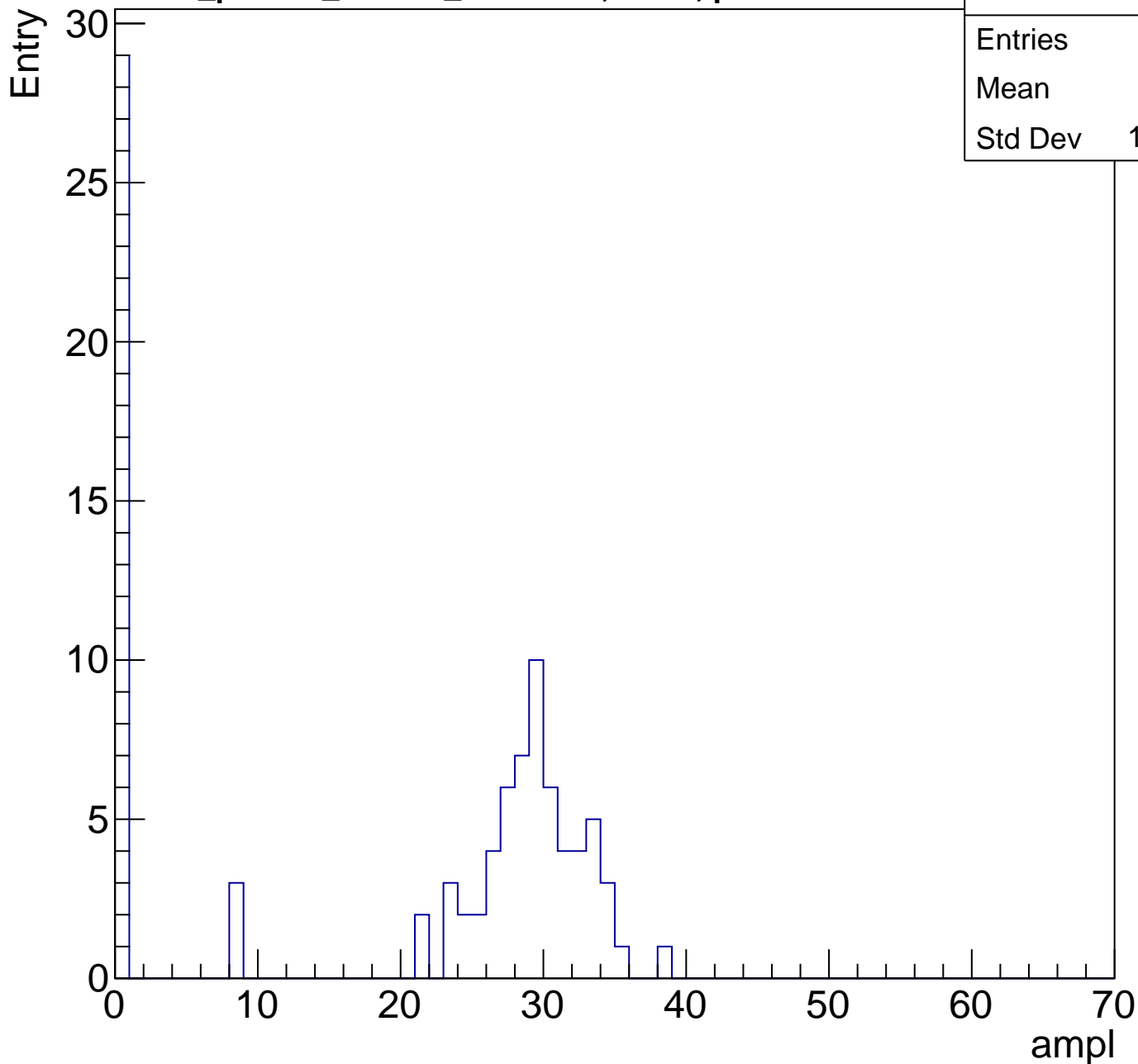




# B1L103S, U4-ch0, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 92    |
| Mean    | 19.1  |
| Std Dev | 13.75 |

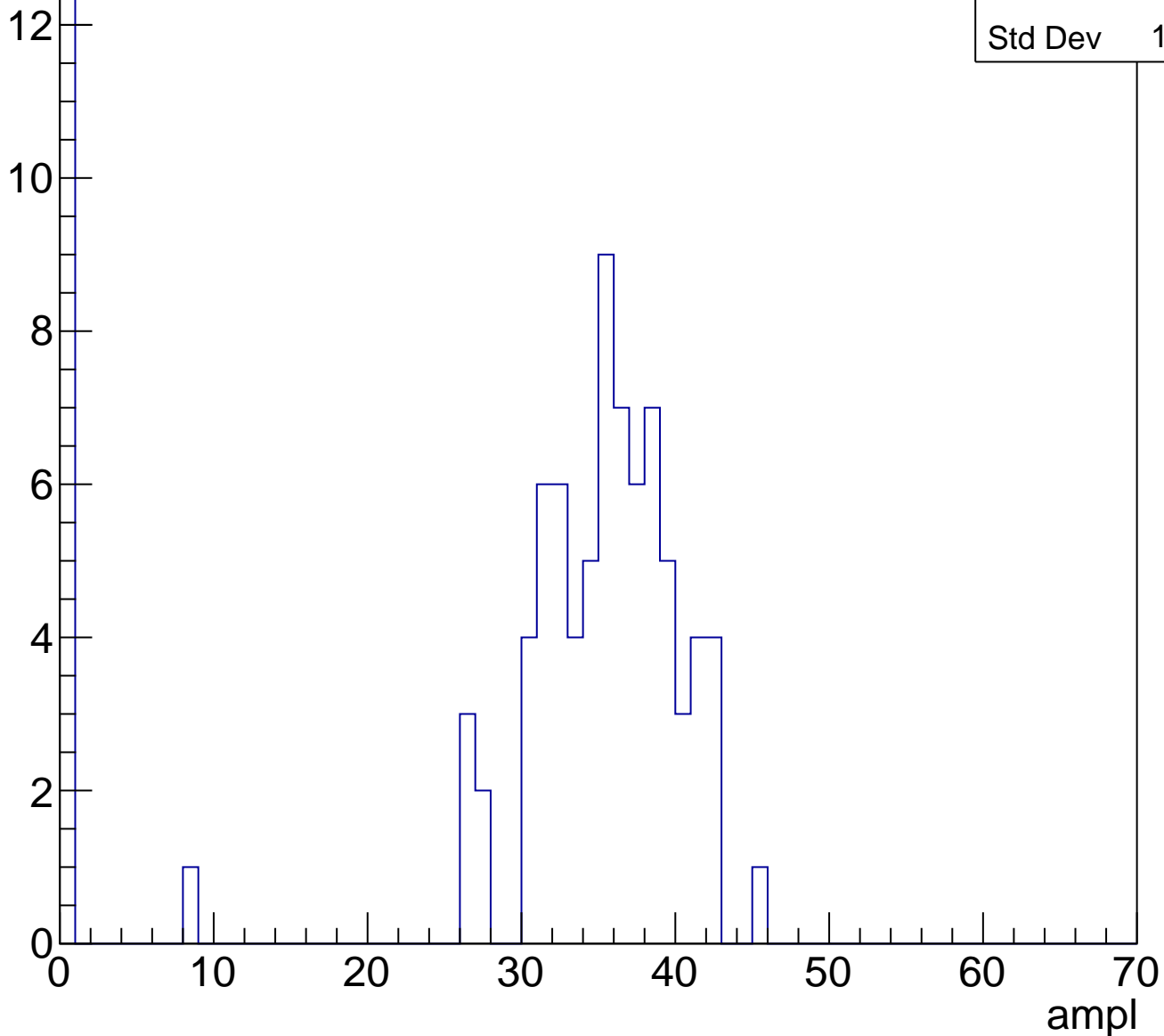


# B1L103S, U4-ch0, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 90    |
| Mean    | 29.86 |
| Std Dev | 13.17 |

Entry

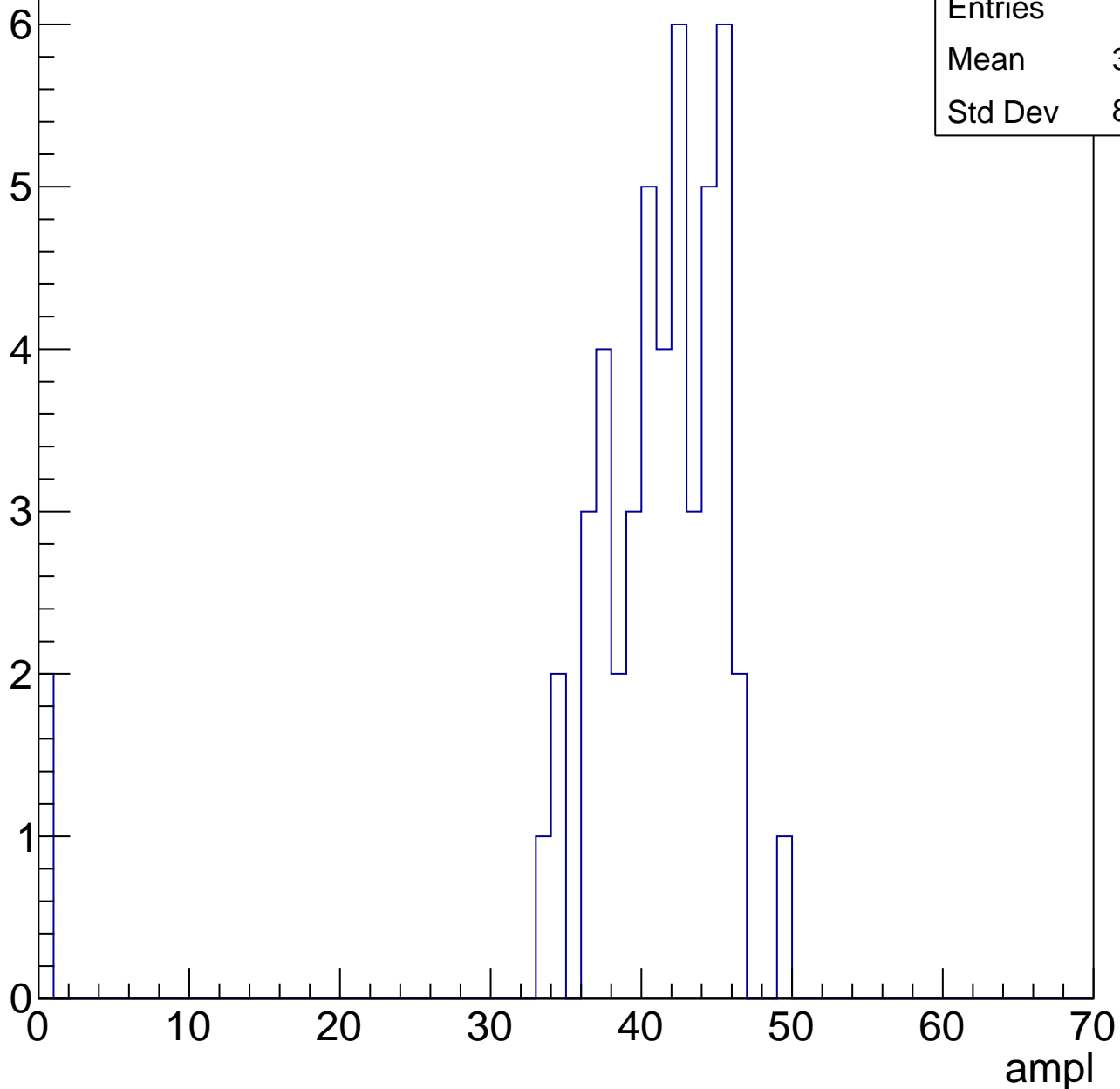


# B1L103S, U4-ch0, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 49    |
| Mean    | 39.31 |
| Std Dev | 8.841 |

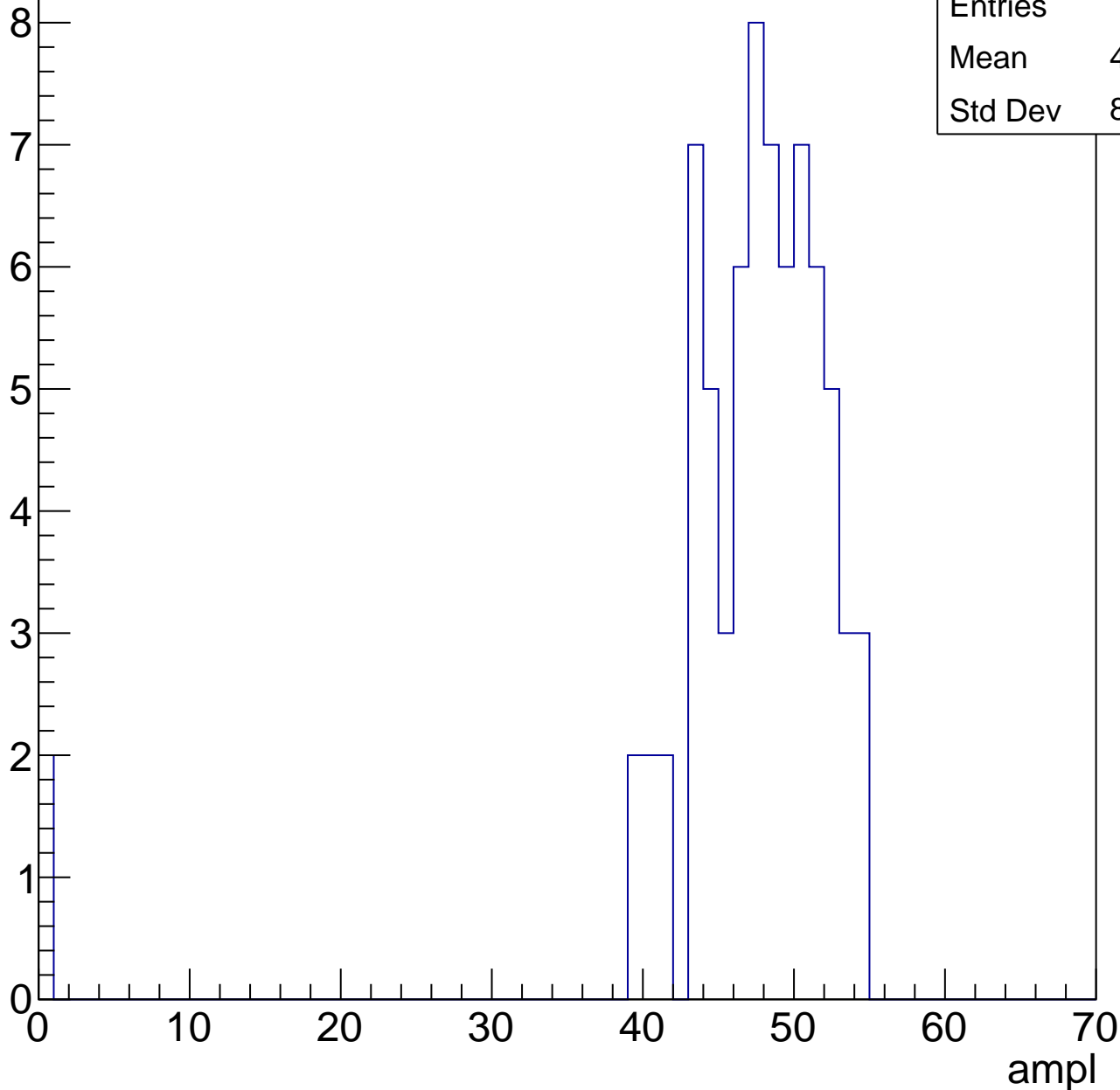


# B1L103S, U4-ch0, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

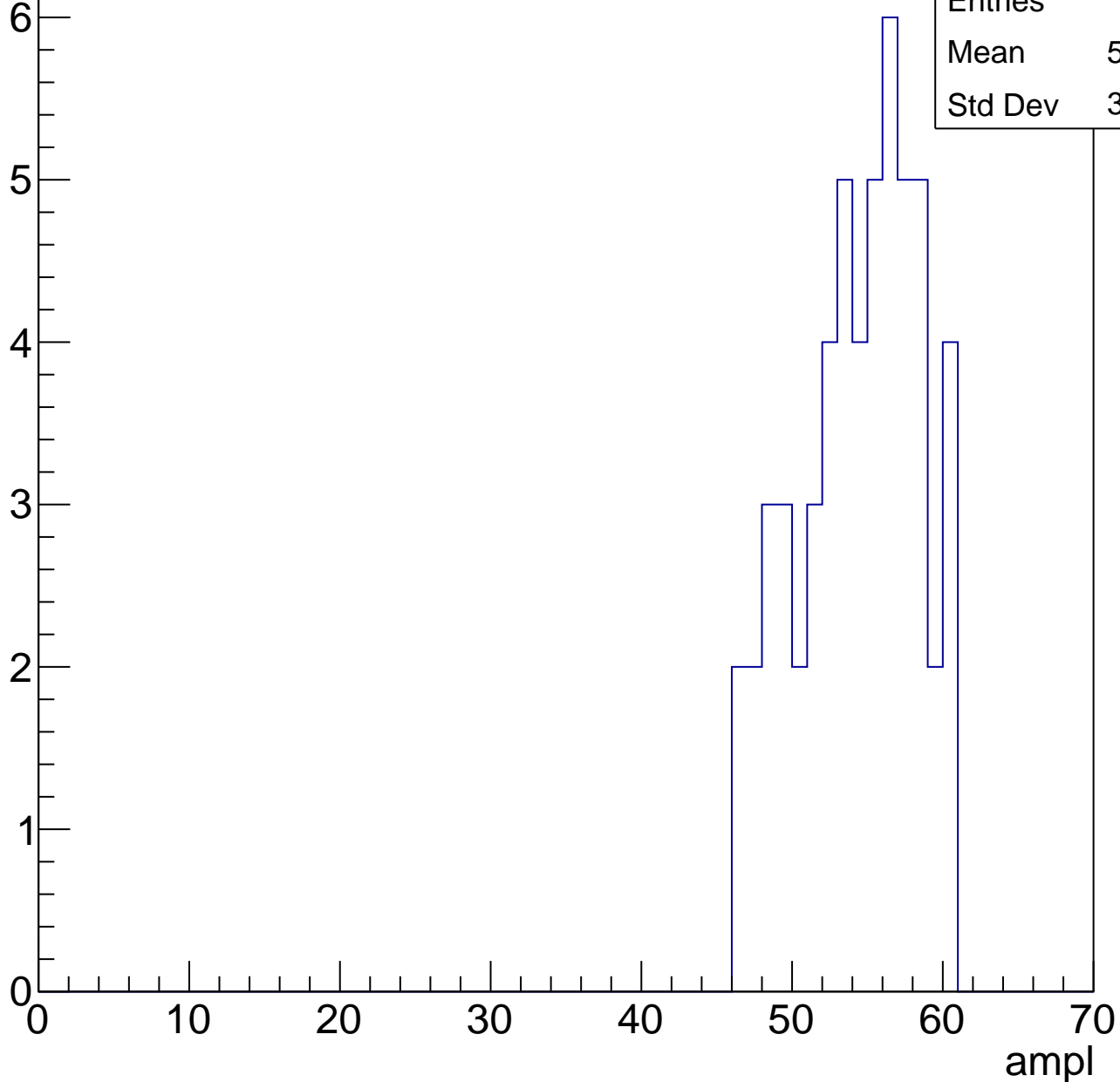
|         |       |
|---------|-------|
| Entries | 74    |
| Mean    | 46.15 |
| Std Dev | 8.548 |



# B1L103S, U4-ch0, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



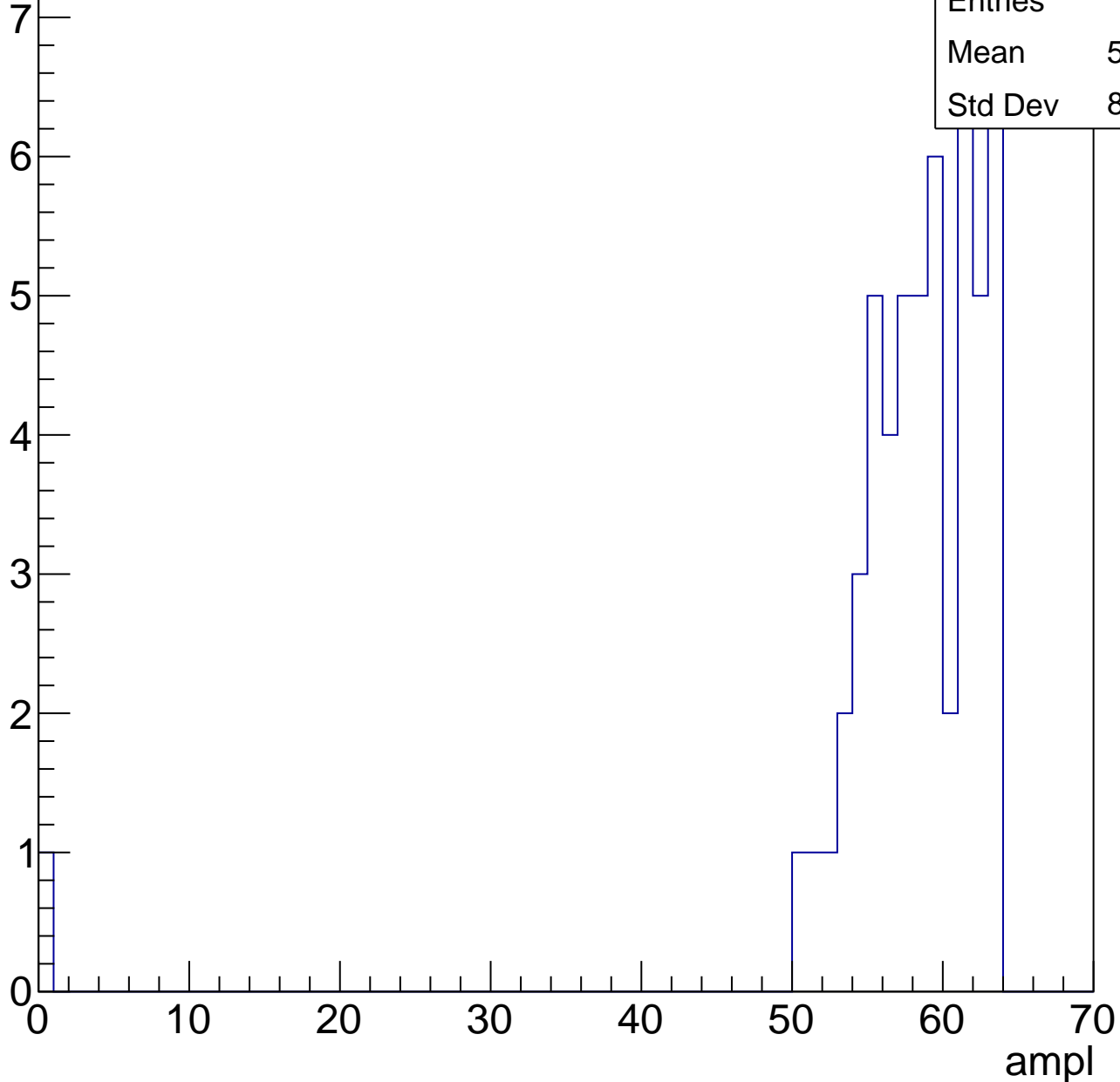
|         |       |
|---------|-------|
| Entries | 55    |
| Mean    | 53.87 |
| Std Dev | 3.899 |

# B1L103S, U4-ch0, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

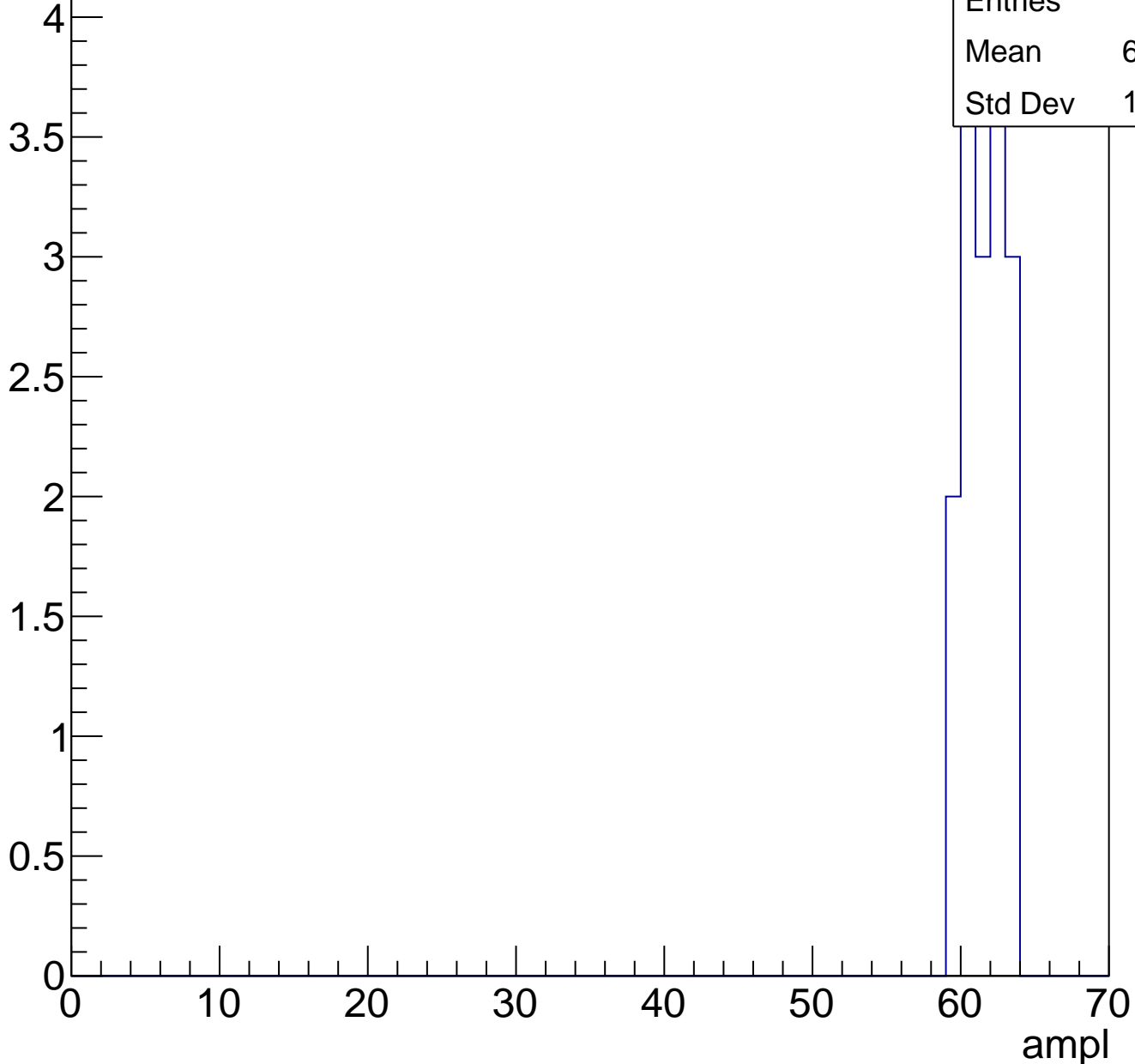
|         |       |
|---------|-------|
| Entries | 55    |
| Mean    | 57.22 |
| Std Dev | 8.502 |



# B1L103S, U4-ch0, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



|         |       |
|---------|-------|
| Entries | 16    |
| Mean    | 61.12 |
| Std Dev | 1.317 |



# B1L103S, U4-ch0, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 20    |
| Mean    | 3.1   |
| Std Dev | 13.51 |

Entry



# B1L103S, U4-ch1, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

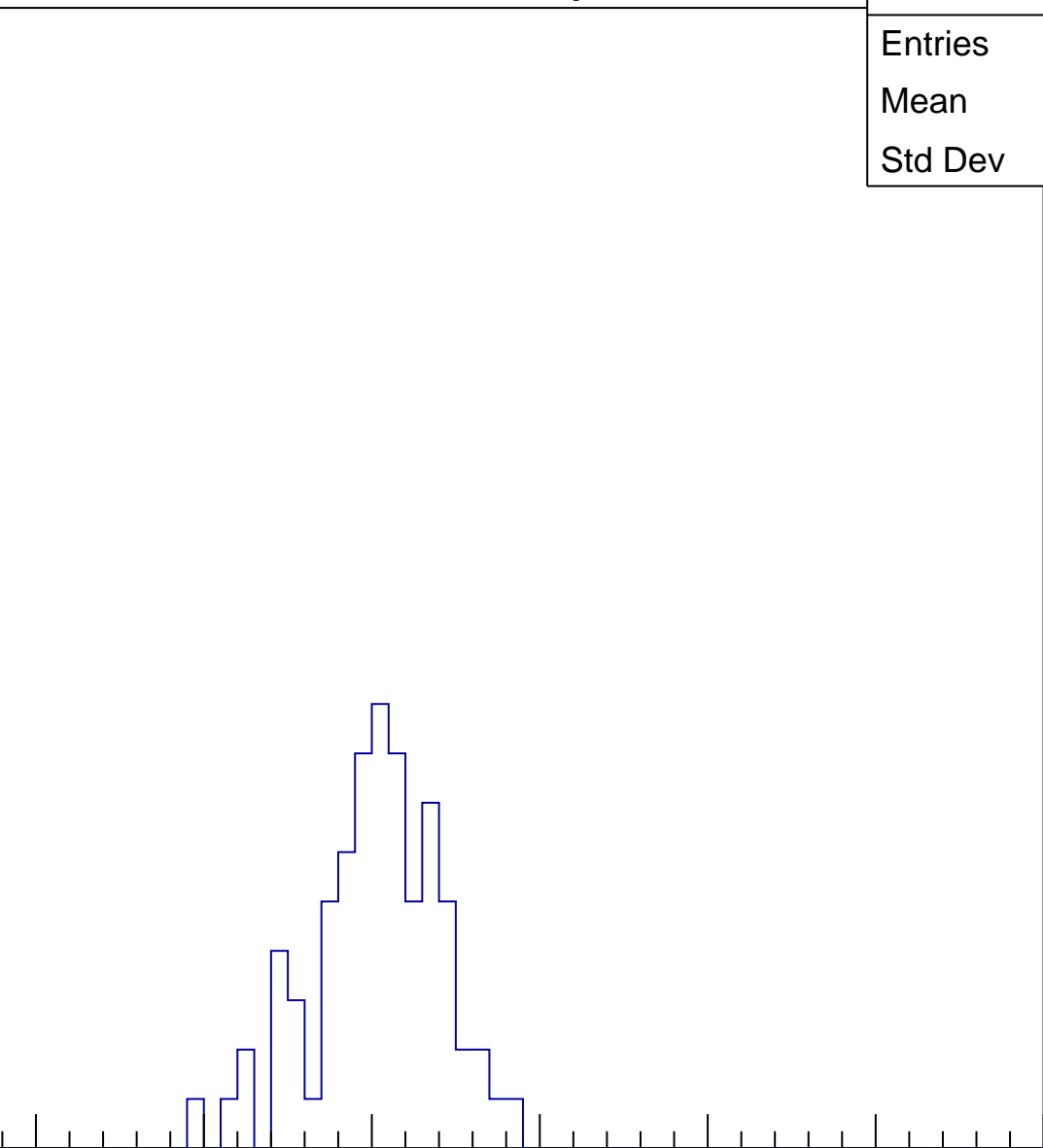
|         |       |
|---------|-------|
| Entries | 93    |
| Mean    | 22.71 |
| Std Dev | 13.08 |

Entry

22  
20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

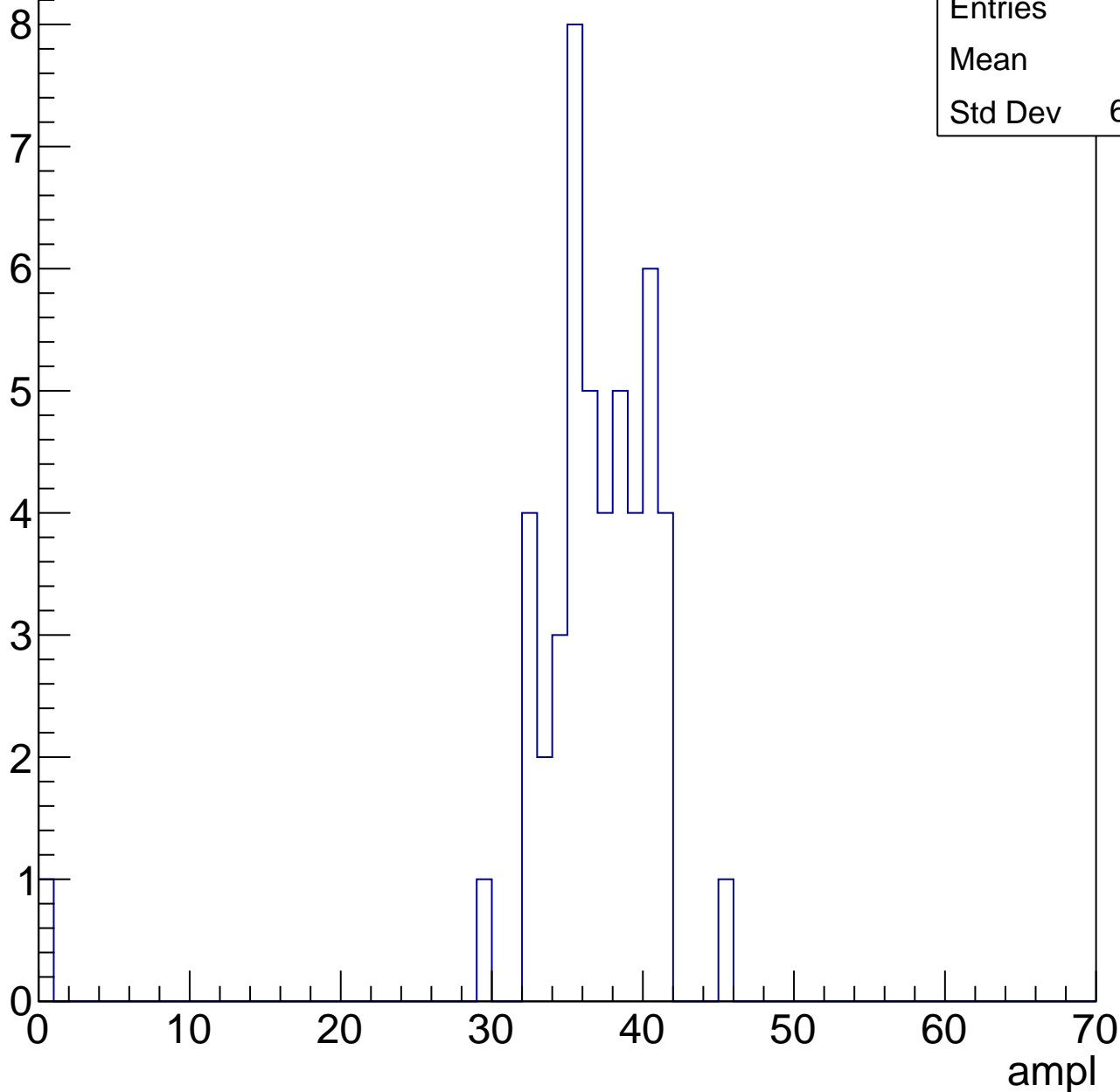


# B1L103S, U4-ch1, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 48    |
| Mean    | 36    |
| Std Dev | 6.096 |



# B1L103S, U4-ch1, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 85    |
| Mean    | 36.69 |
| Std Dev | 14.55 |

Entry

10

8

6

4

2

0

ampl

0

10

20

30

40

50

60

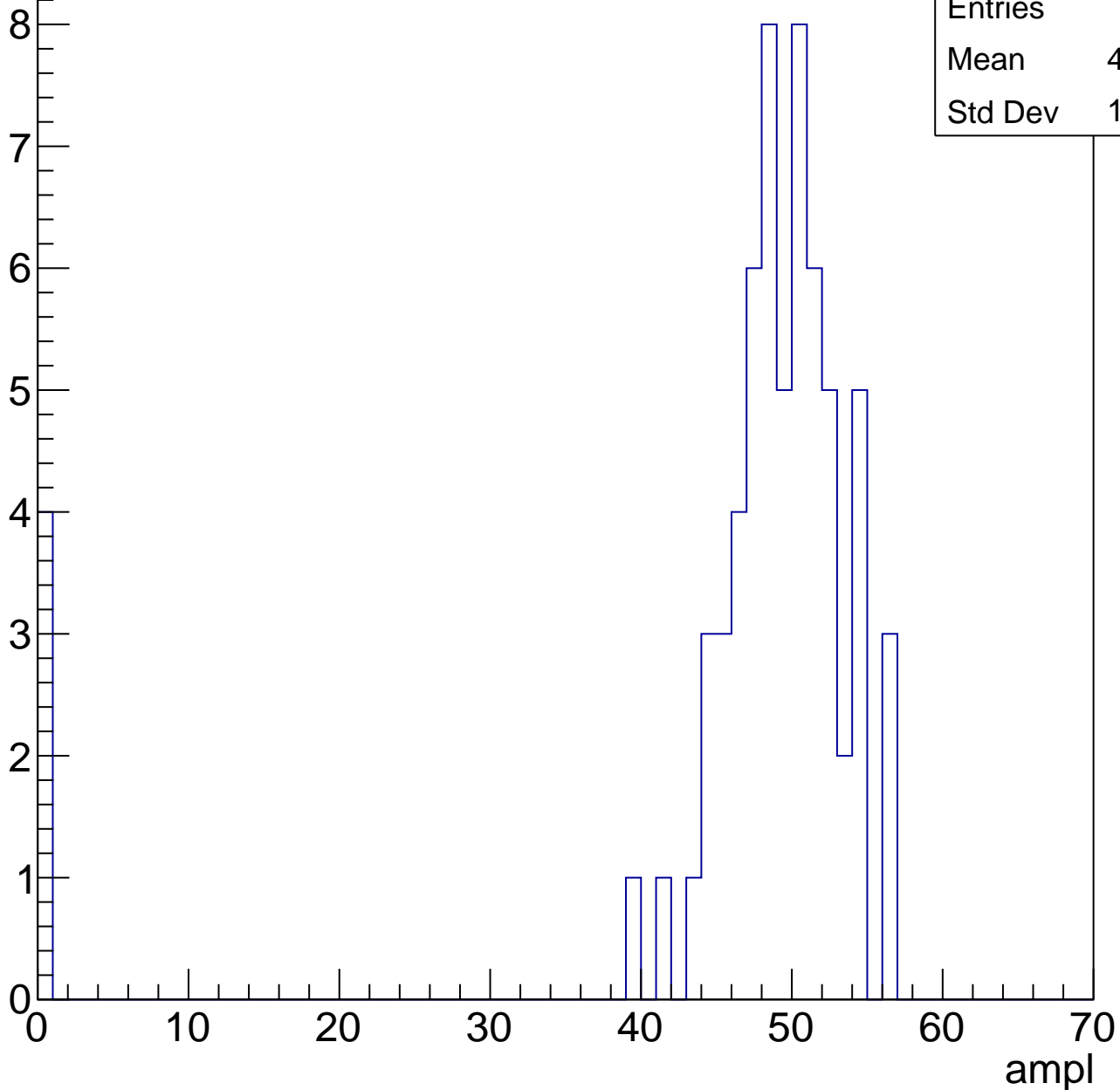
70

# B1L103S, U4-ch1, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 65    |
| Mean    | 46.08 |
| Std Dev | 12.29 |

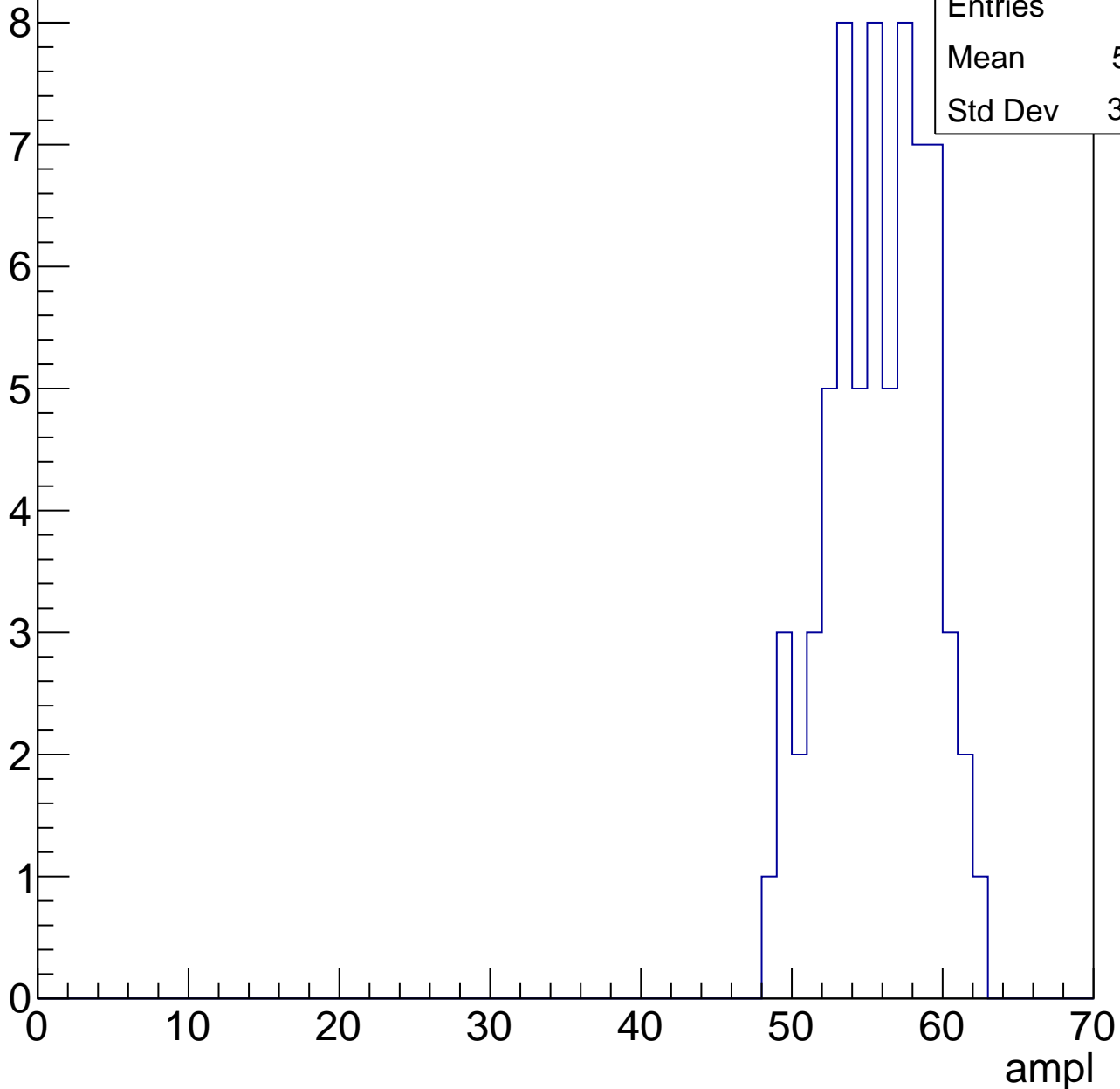


# B1L103S, U4-ch1, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 68    |
| Mean    | 55.31 |
| Std Dev | 3.296 |

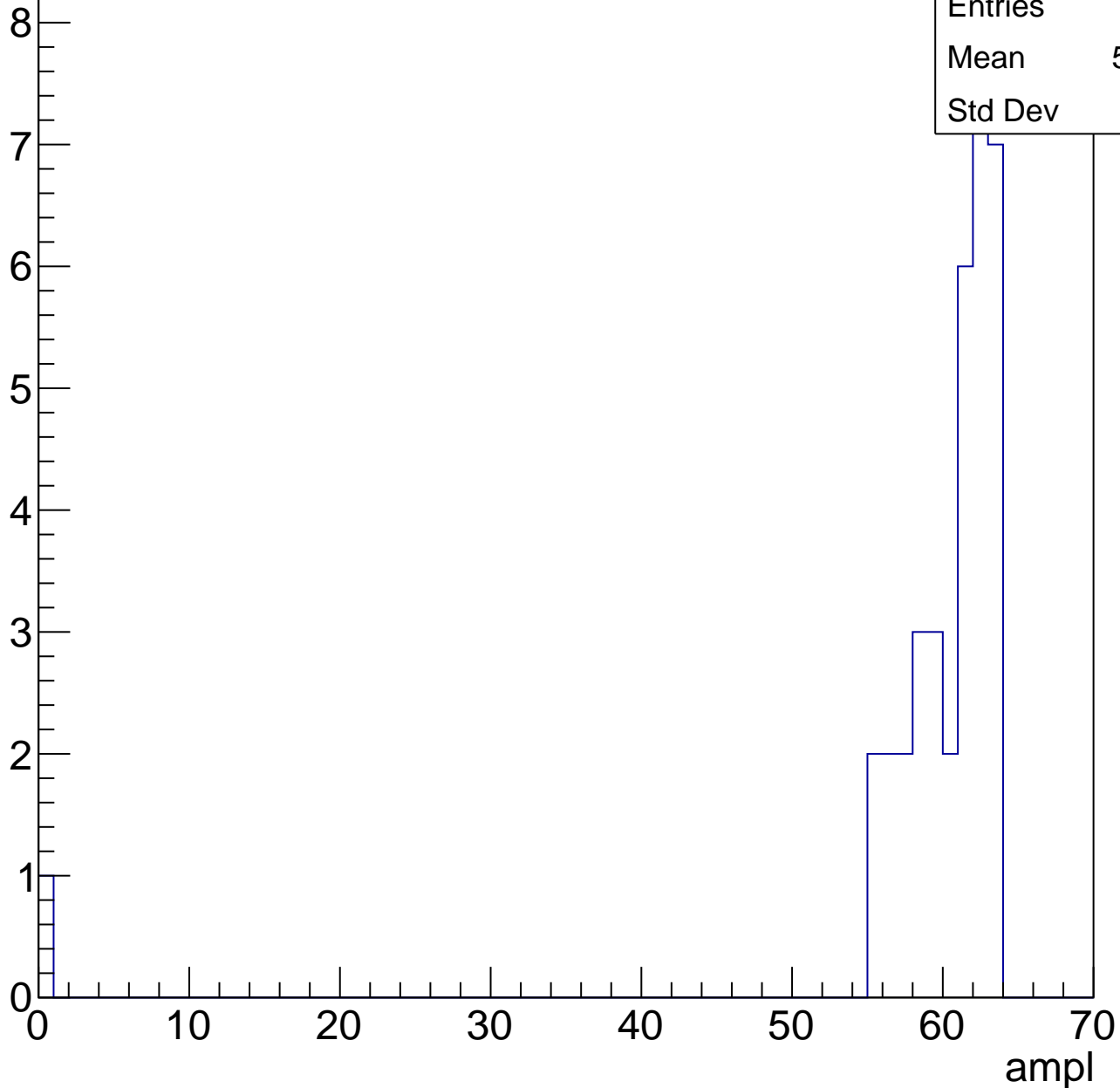


# B1L103S, U4-ch1, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

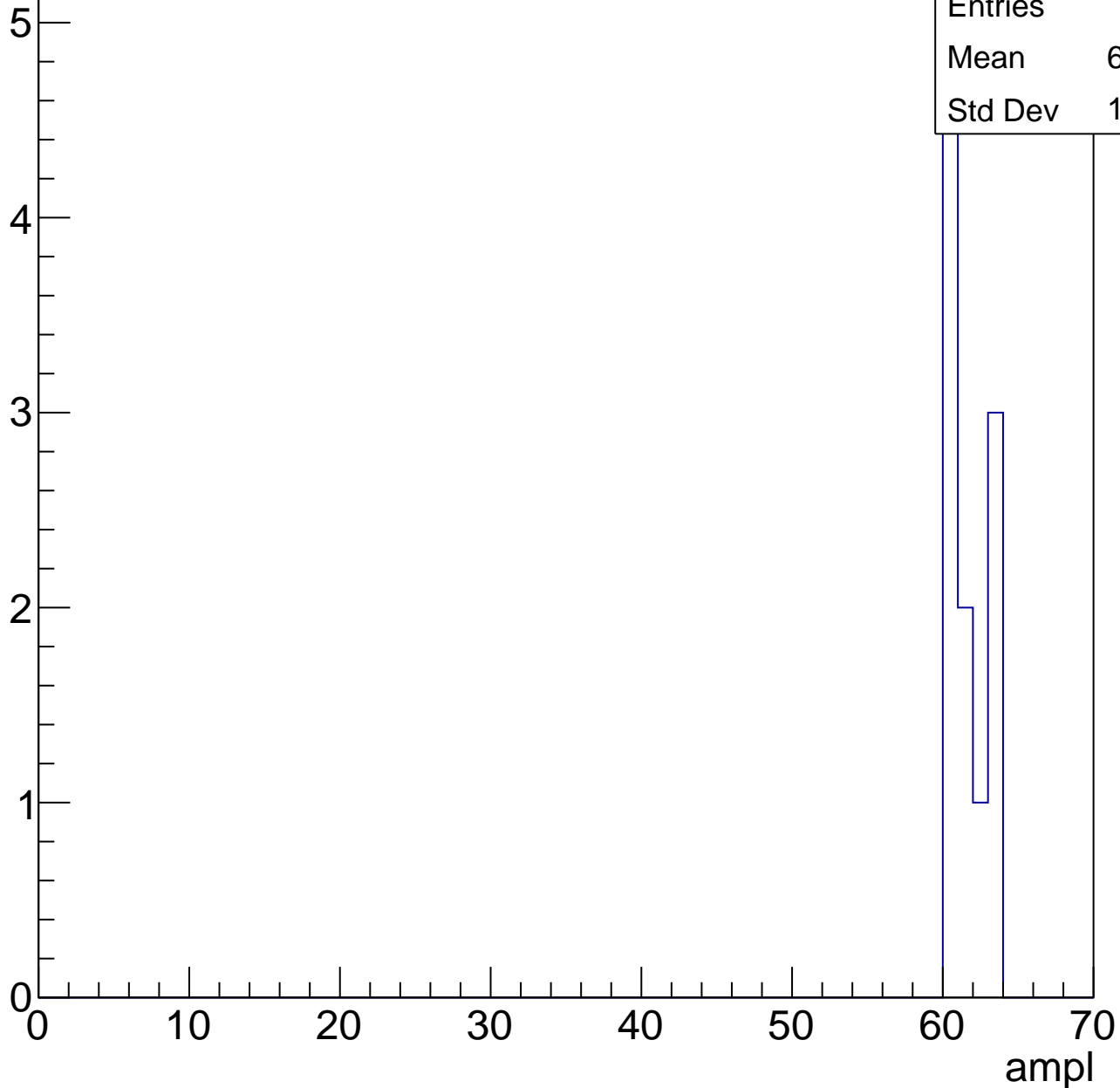
|         |       |
|---------|-------|
| Entries | 36    |
| Mean    | 58.61 |
| Std Dev | 10.2  |



# B1L103S, U4-ch1, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U4-ch1, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |    |
|---------|----|
| Entries | 19 |
| Mean    | 0  |
| Std Dev | 0  |



# B1L103S, U4-ch2, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 80    |
| Mean    | 22.62 |
| Std Dev | 11.76 |

Entry

16  
14  
12  
10  
8  
6  
4  
2  
0

0

10

20

30

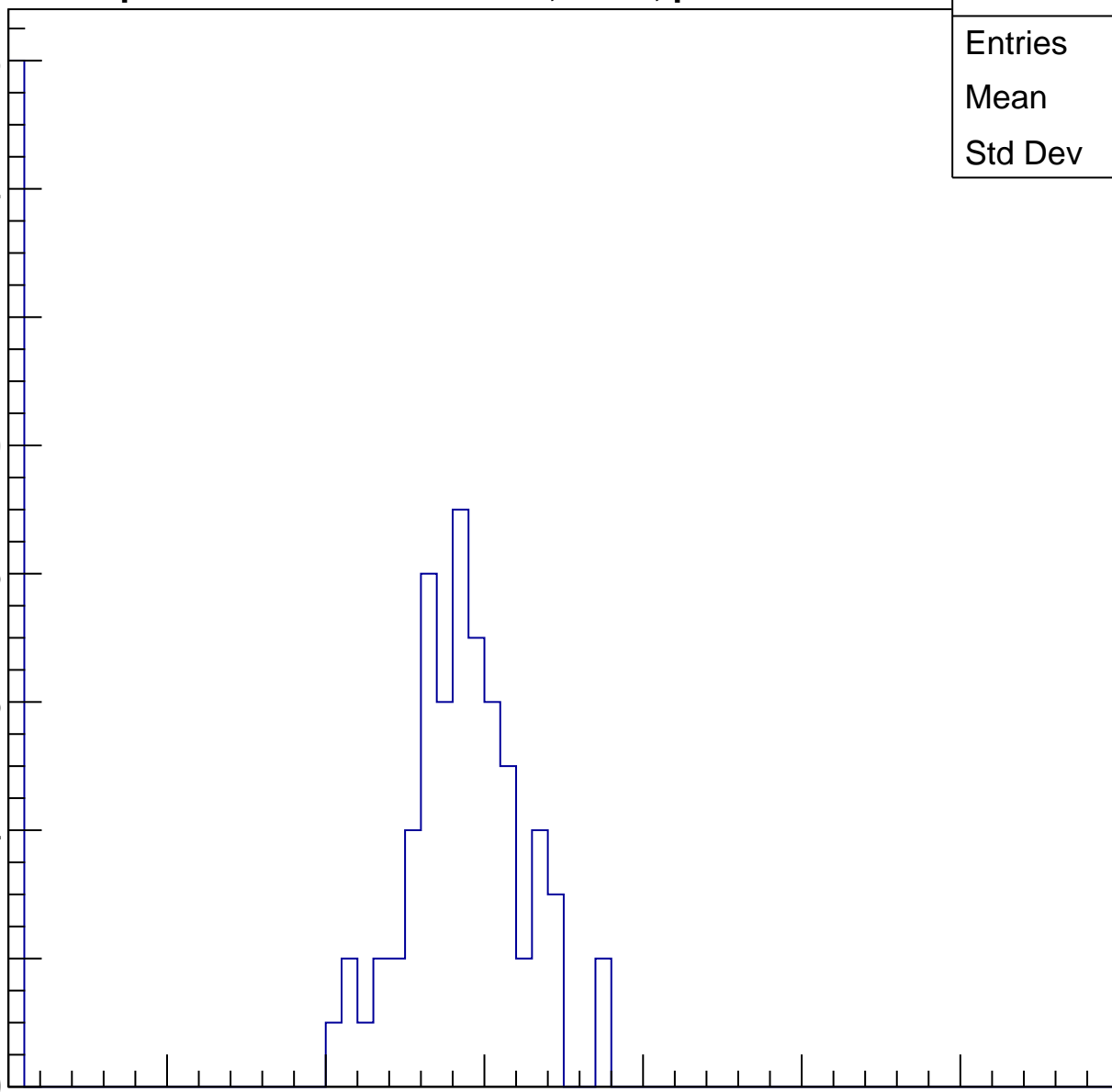
40

50

60

70

ampl



# B1L103S, U4-ch2, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 71    |
| Mean    | 34.48 |
| Std Dev | 3.472 |

Entry

10

8

6

4

2

0

0

10

20

30

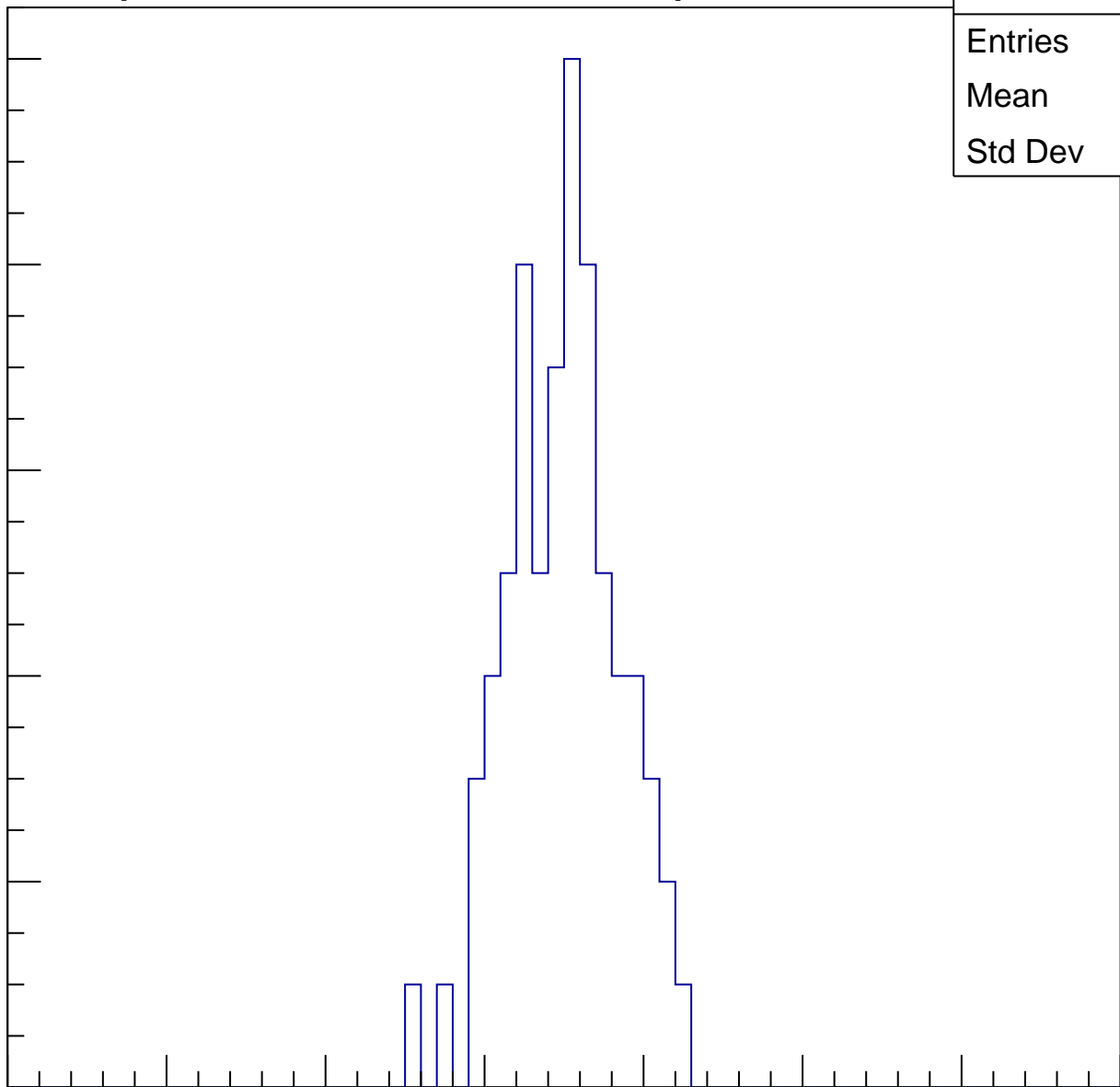
40

50

60

70

ampl

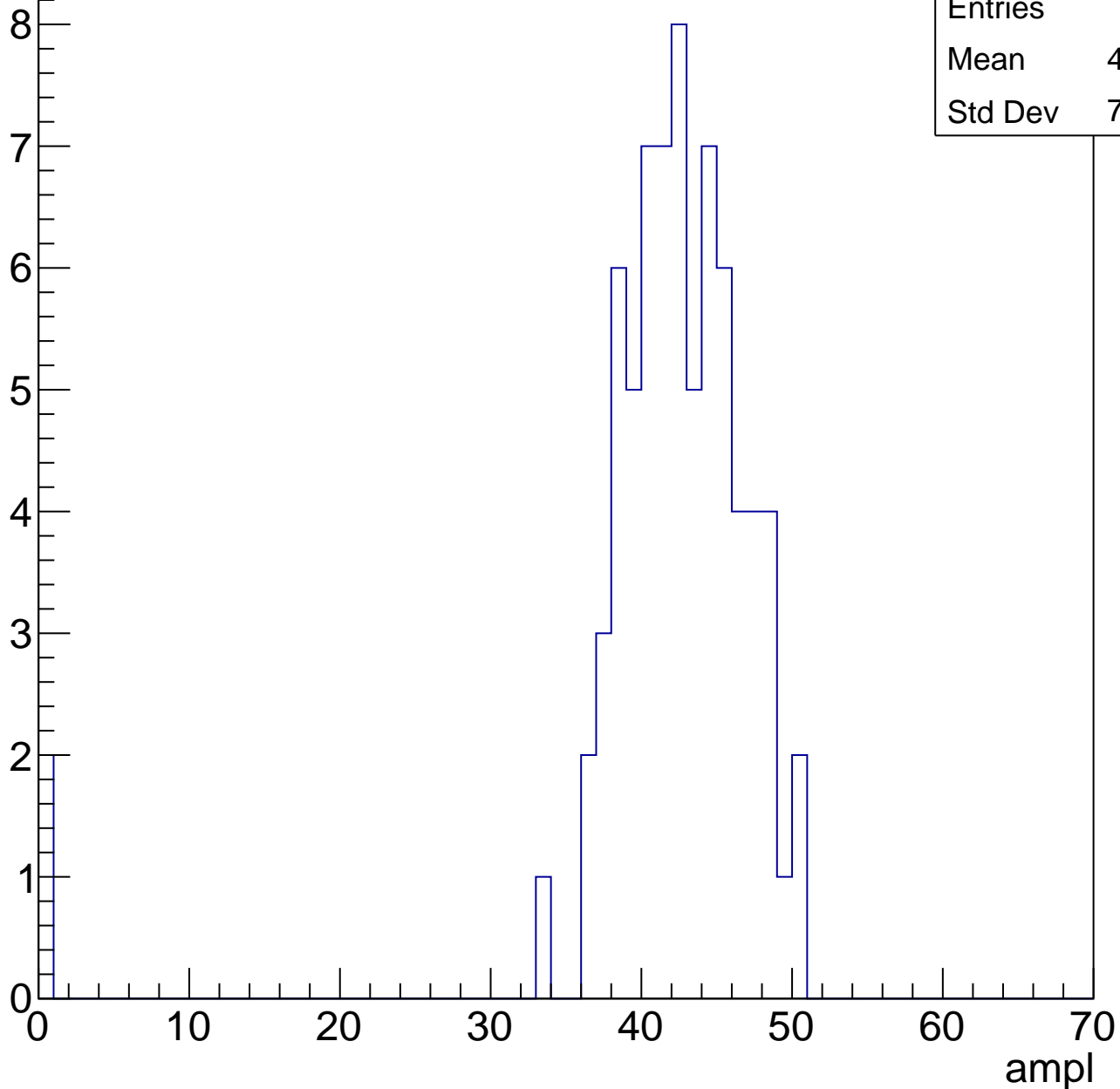


# B1L103S, U4-ch2, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

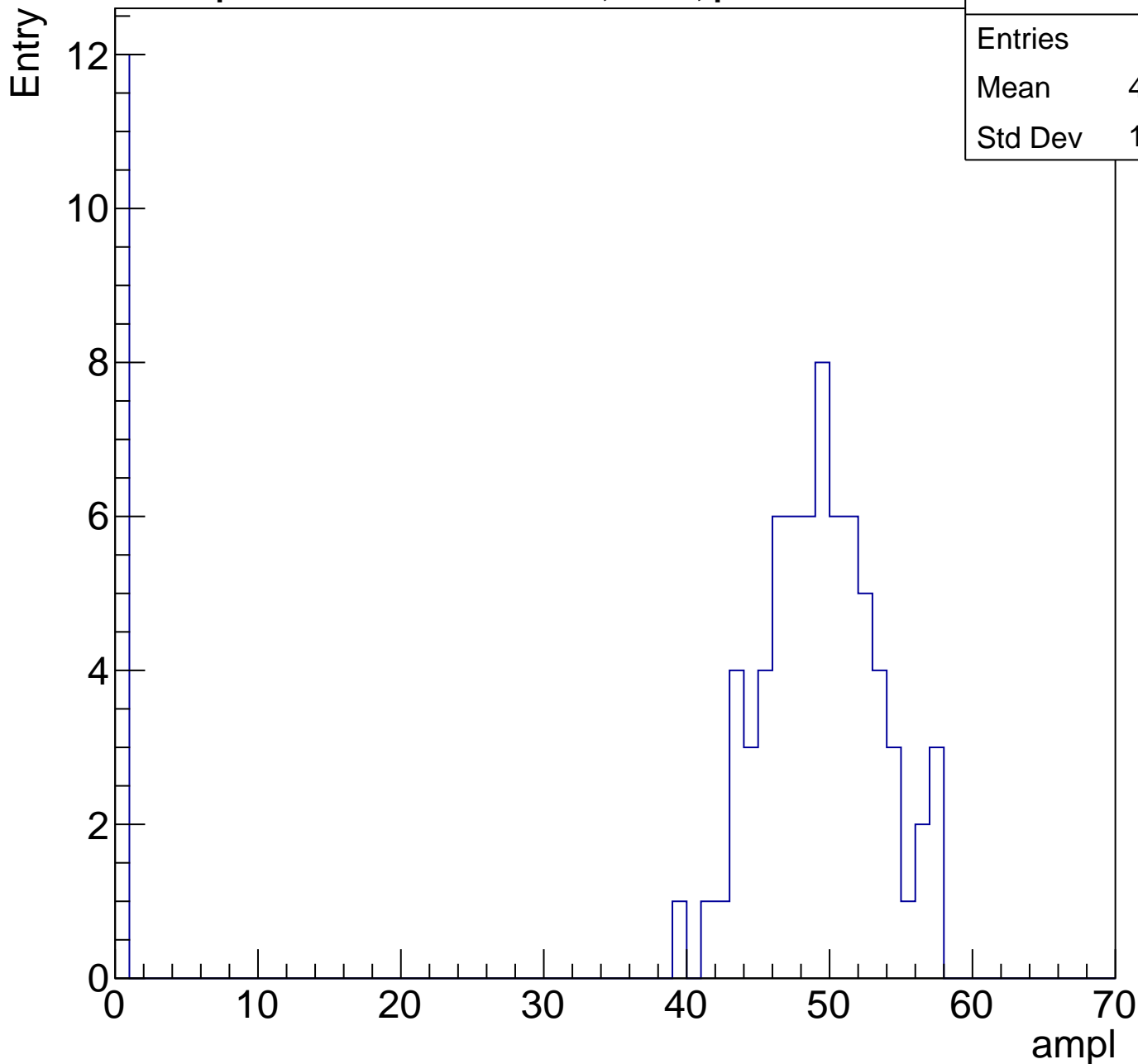
|         |       |
|---------|-------|
| Entries | 74    |
| Mean    | 41.19 |
| Std Dev | 7.759 |



# B1L103S, U4-ch2, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 82    |
| Mean    | 41.73 |
| Std Dev | 17.67 |

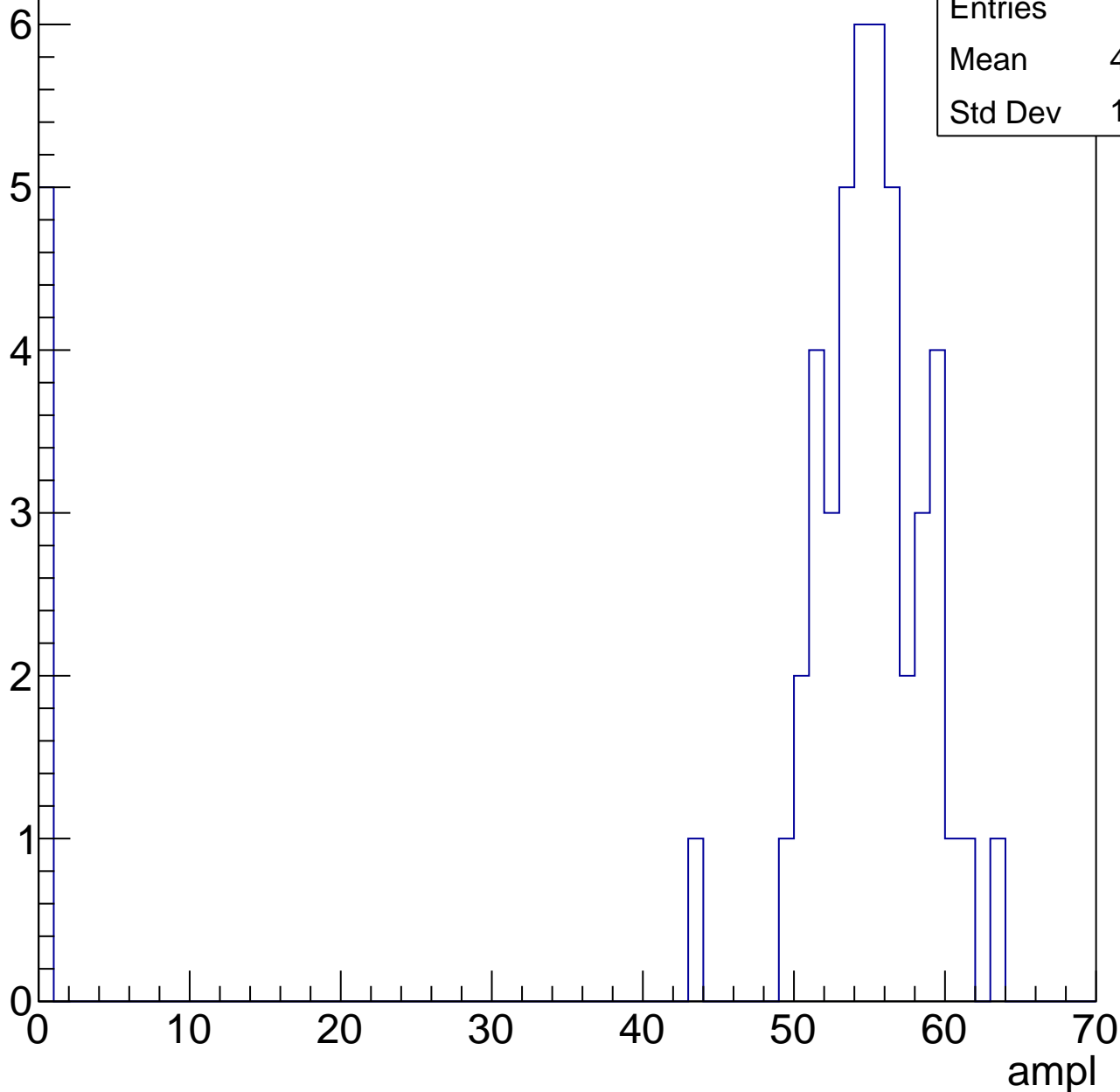


# B1L103S, U4-ch2, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 50    |
| Mean    | 49.18 |
| Std Dev | 16.74 |

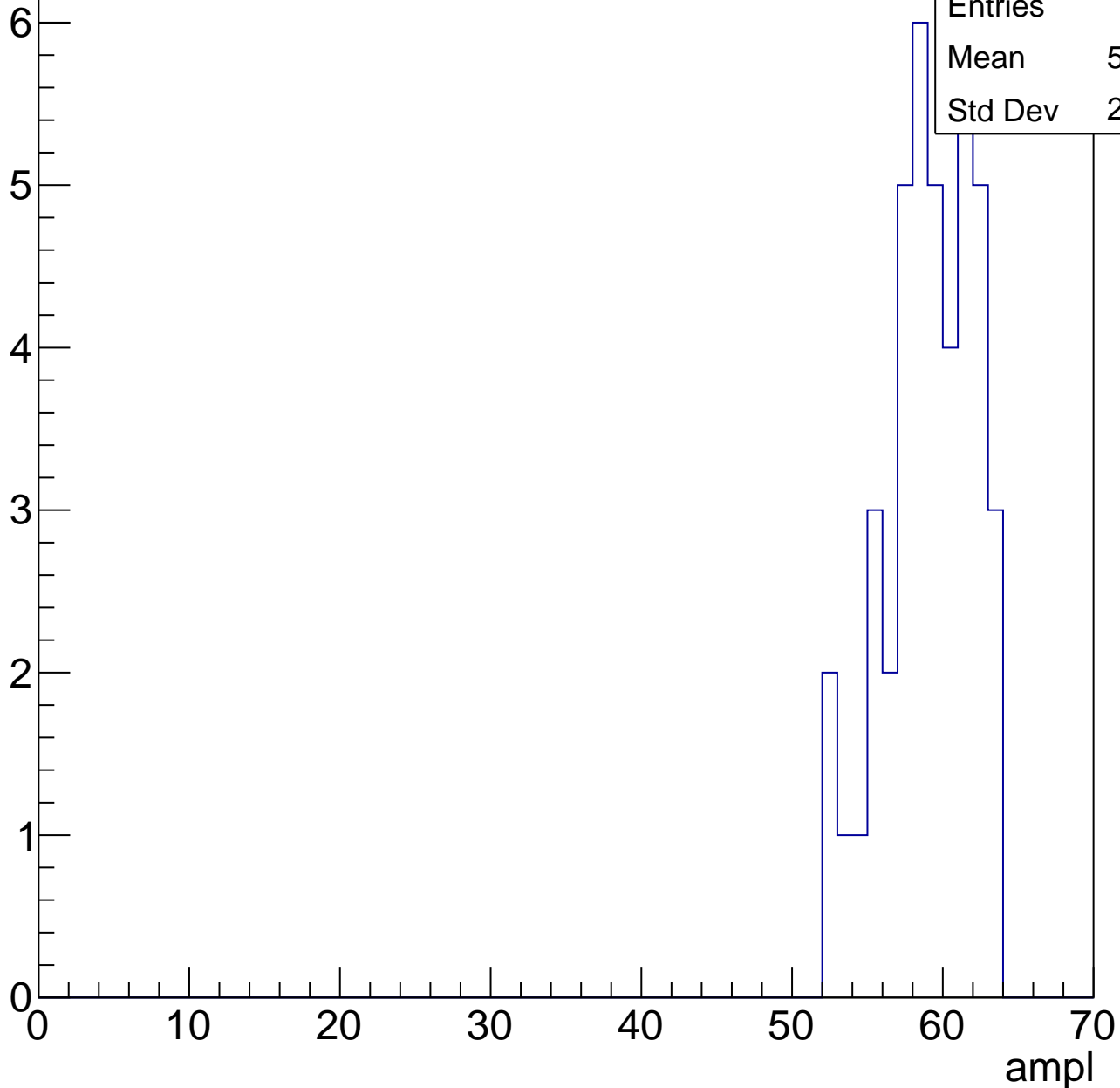


# B1L103S, U4-ch2, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

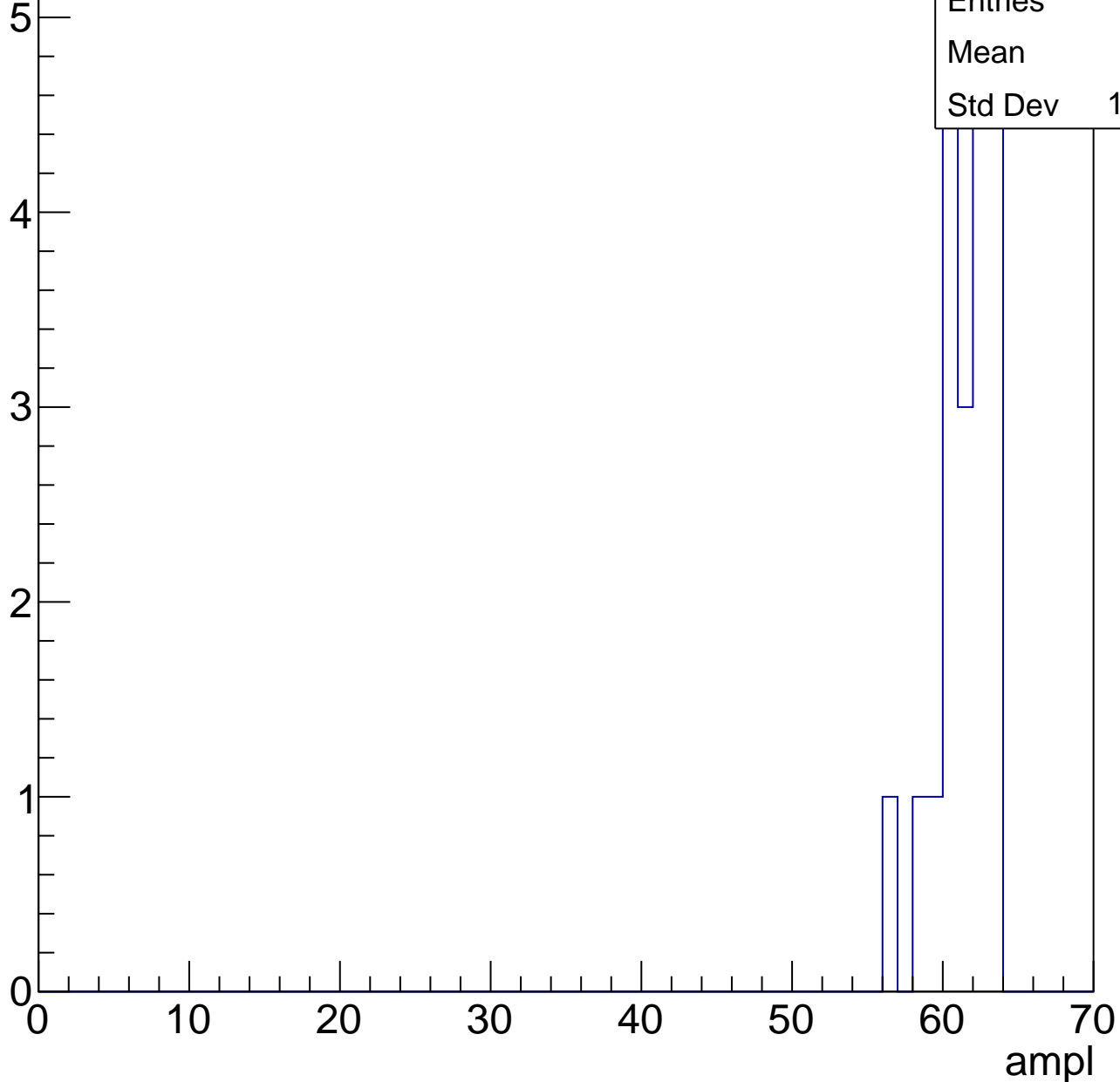
|         |       |
|---------|-------|
| Entries | 43    |
| Mean    | 58.63 |
| Std Dev | 2.918 |



# B1L103S, U4-ch2, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



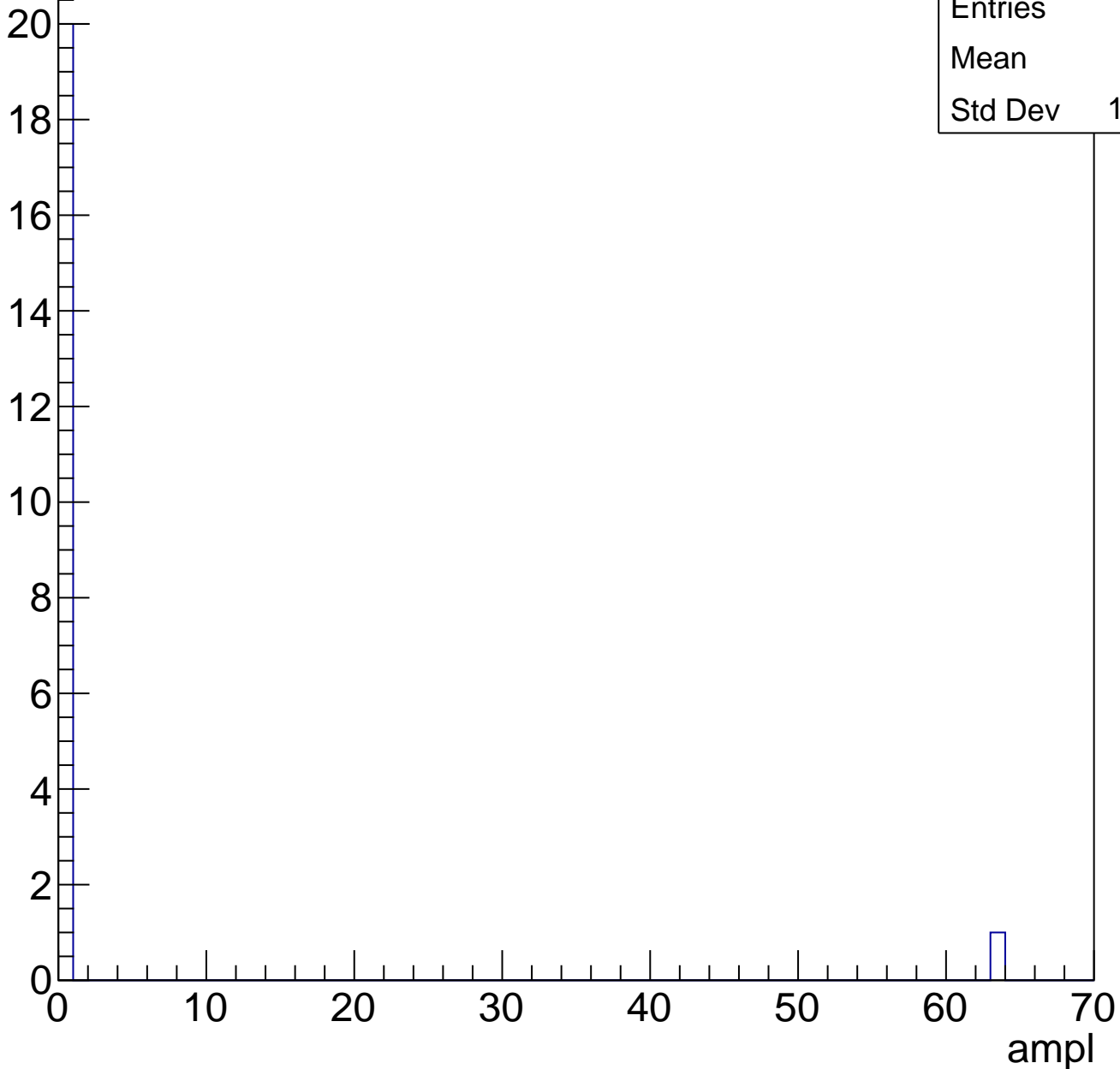


# B1L103S, U4-ch2, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 21    |
| Mean    | 3     |
| Std Dev | 13.42 |

Entry

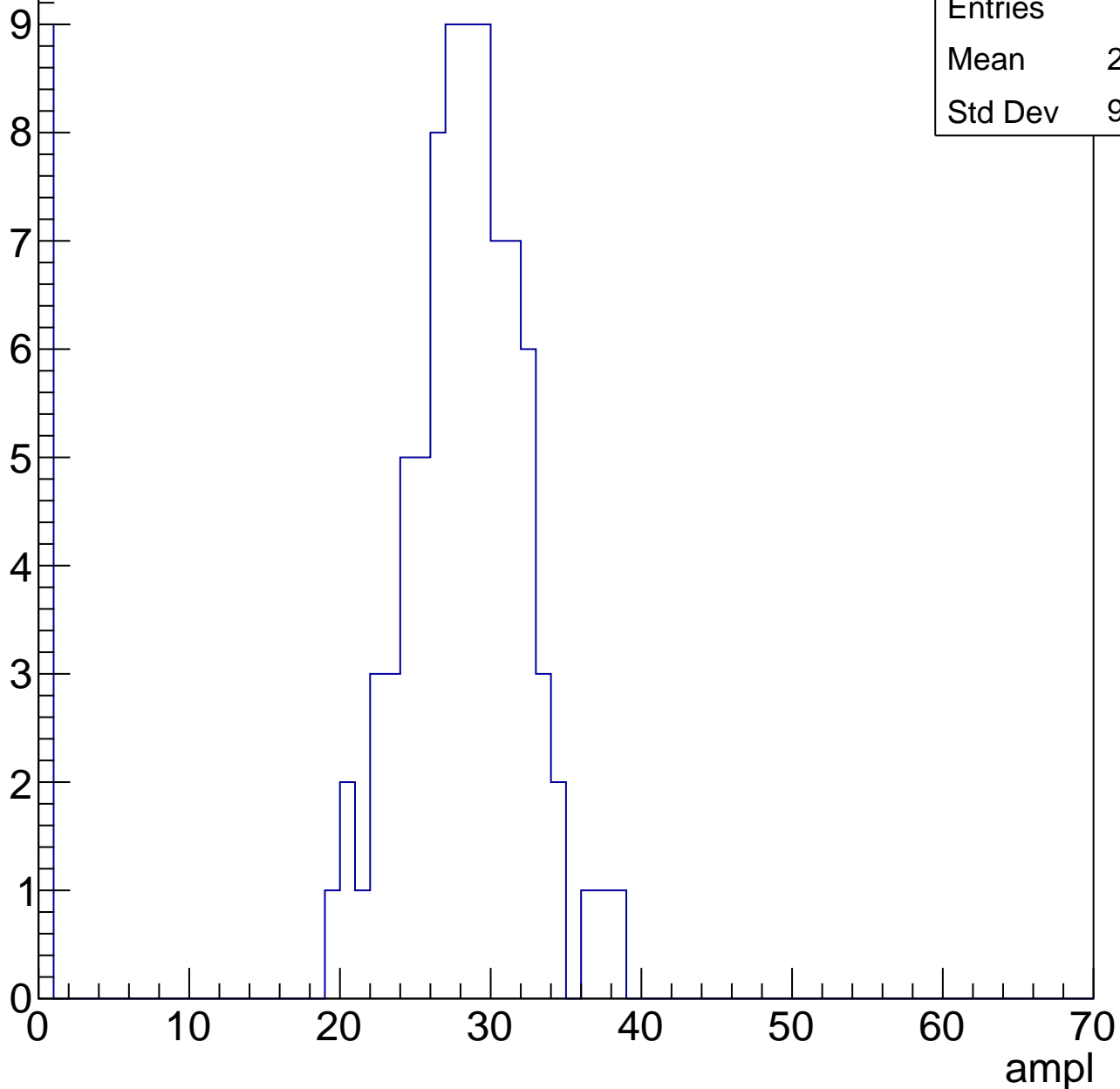


# B1L103S, U4-ch3, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 92    |
| Mean    | 25.23 |
| Std Dev | 9.056 |

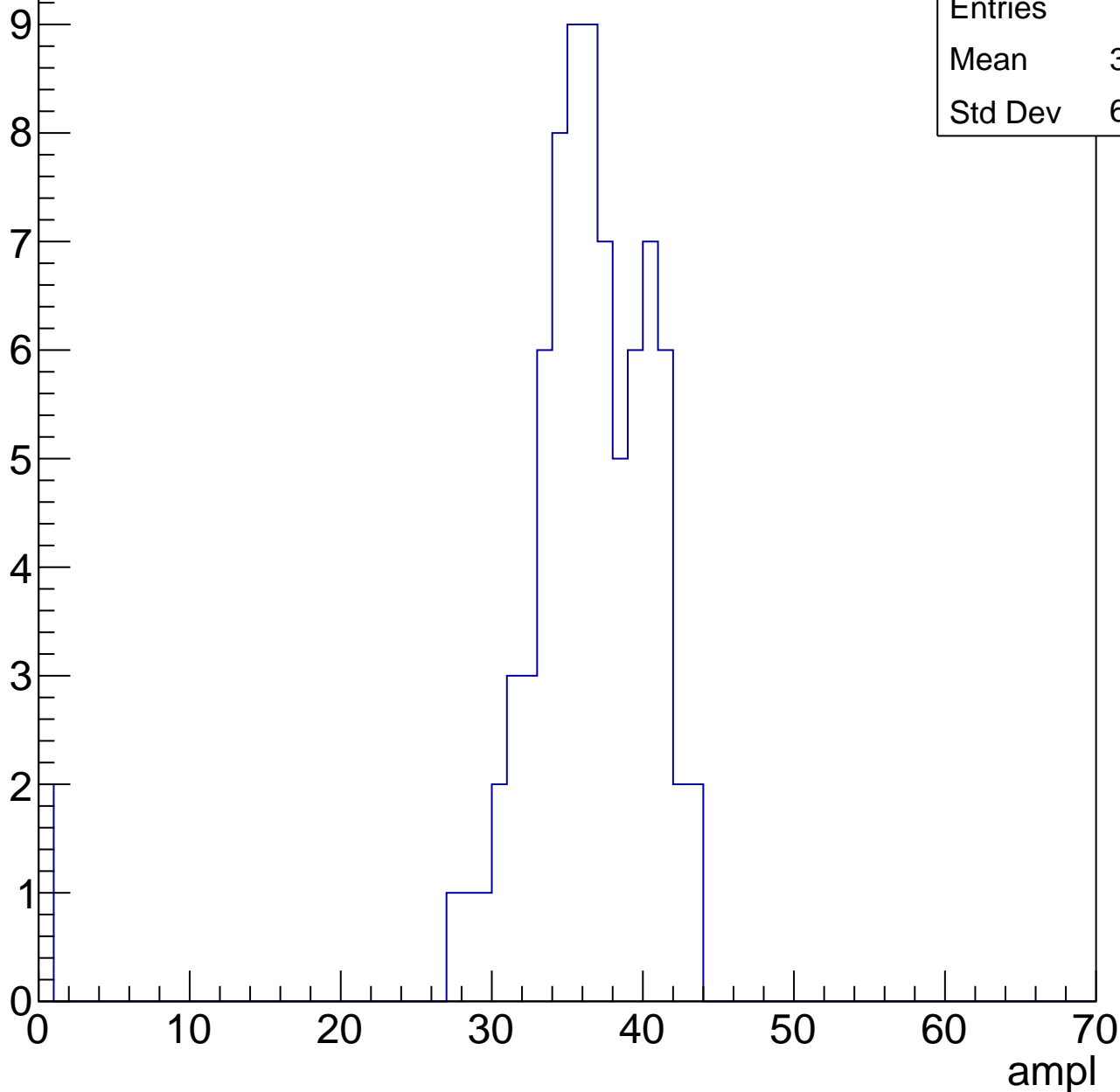


# B1L103S, U4-ch3, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 80    |
| Mean    | 35.26 |
| Std Dev | 6.657 |

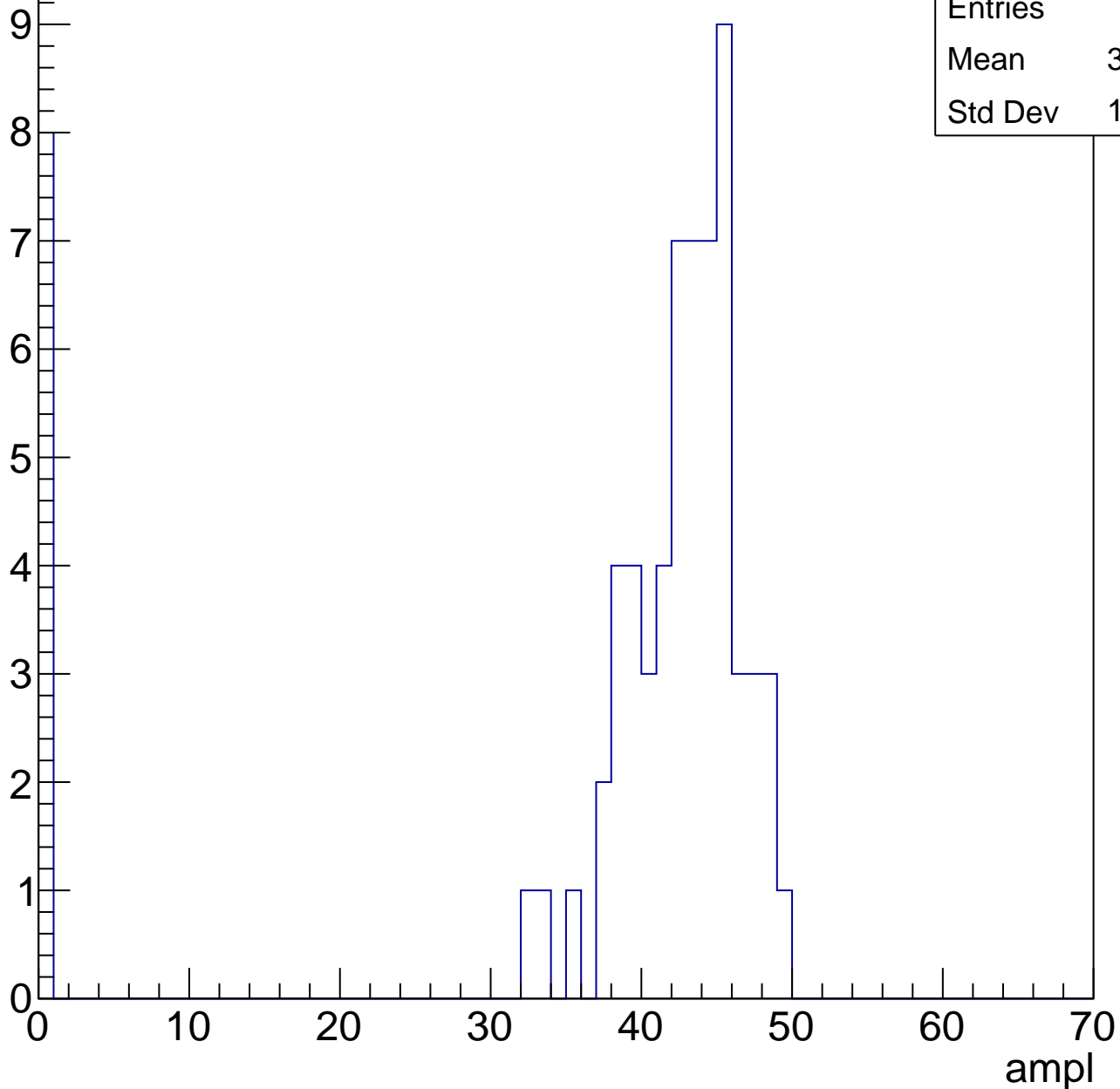


# B1L103S, U4-ch3, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 68    |
| Mean    | 37.44 |
| Std Dev | 14.09 |

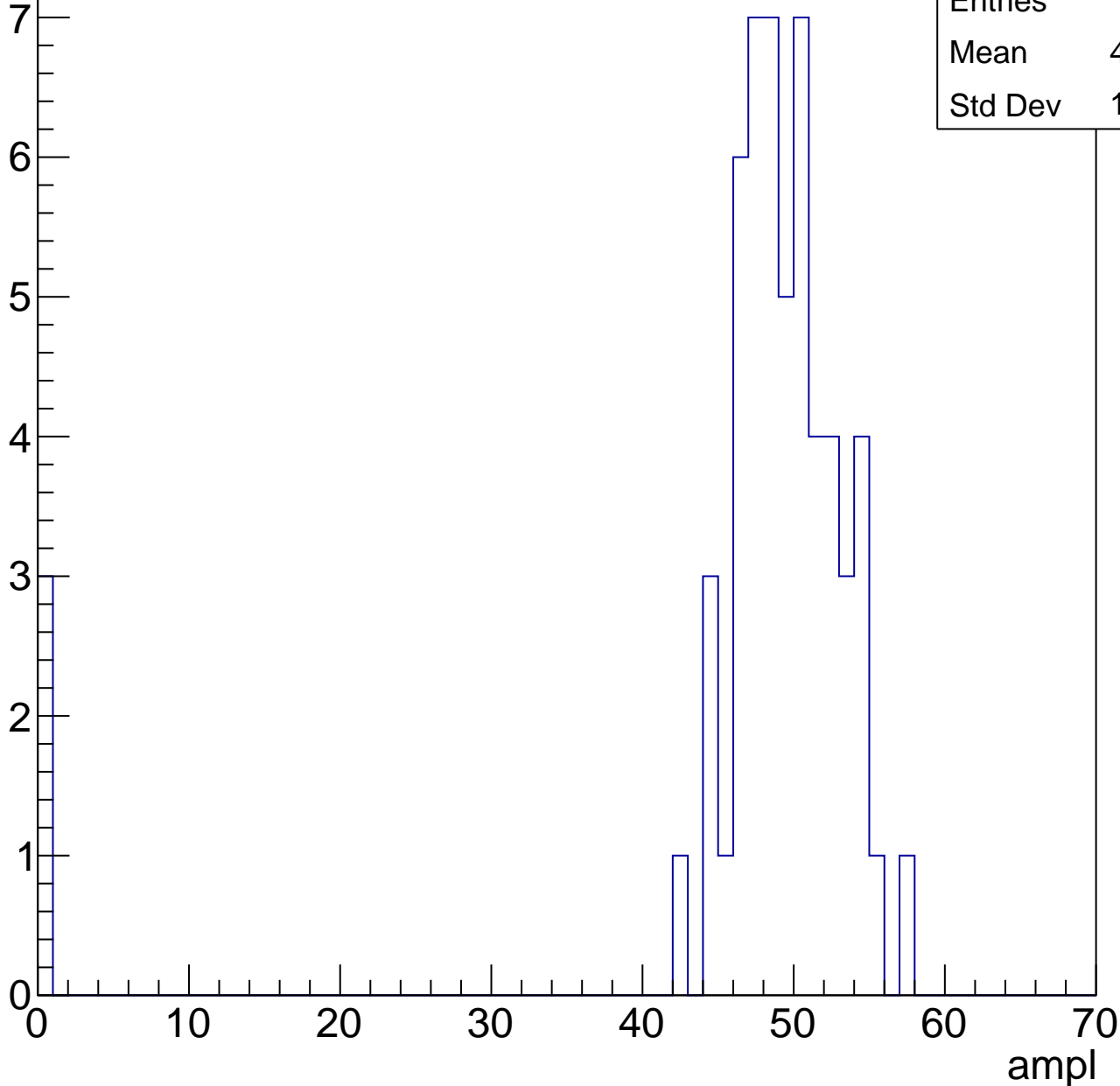


# B1L103S, U4-ch3, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 57    |
| Mean    | 46.56 |
| Std Dev | 11.39 |

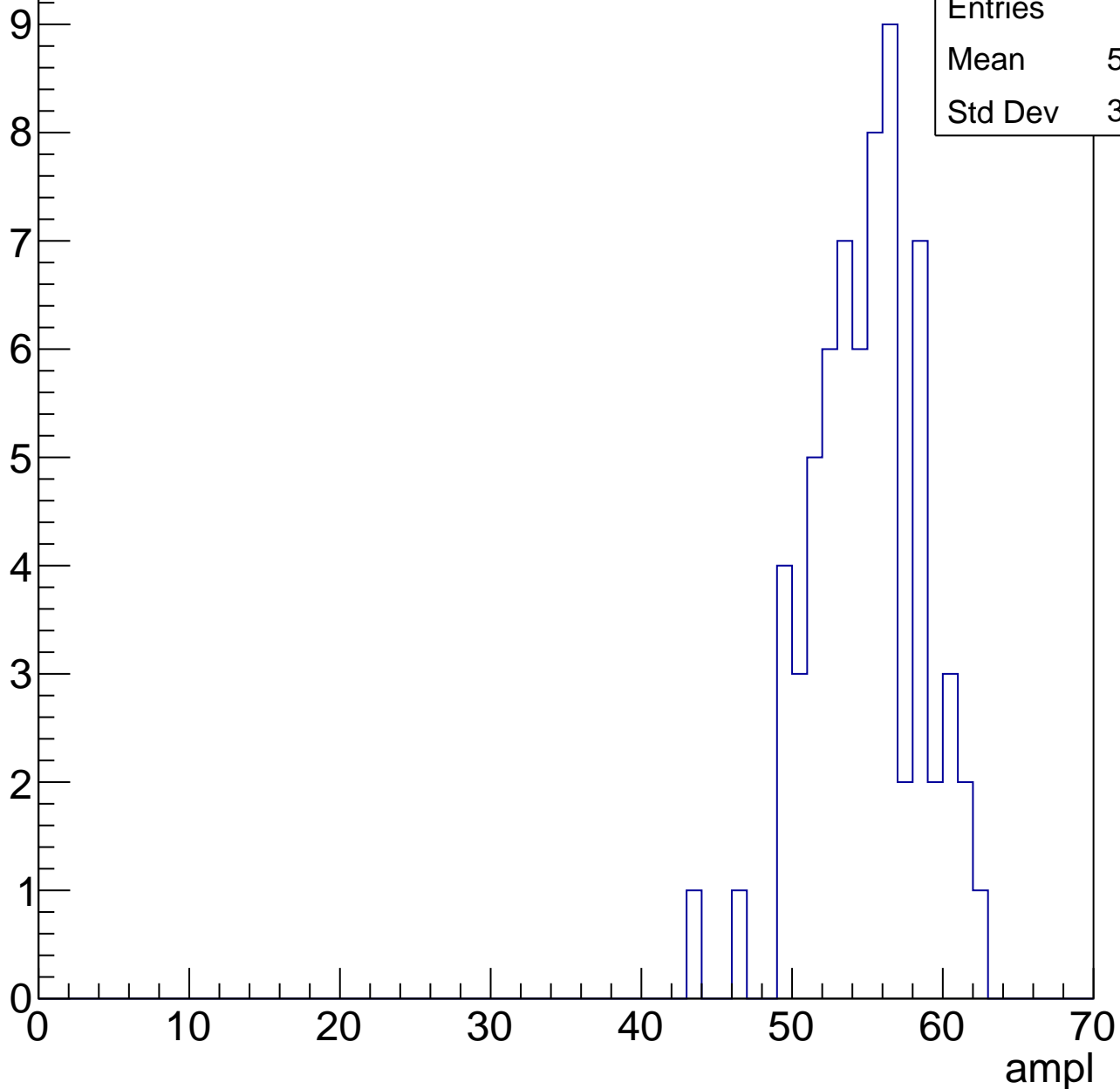


# B1L103S, U4-ch3, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 67    |
| Mean    | 54.37 |
| Std Dev | 3.652 |

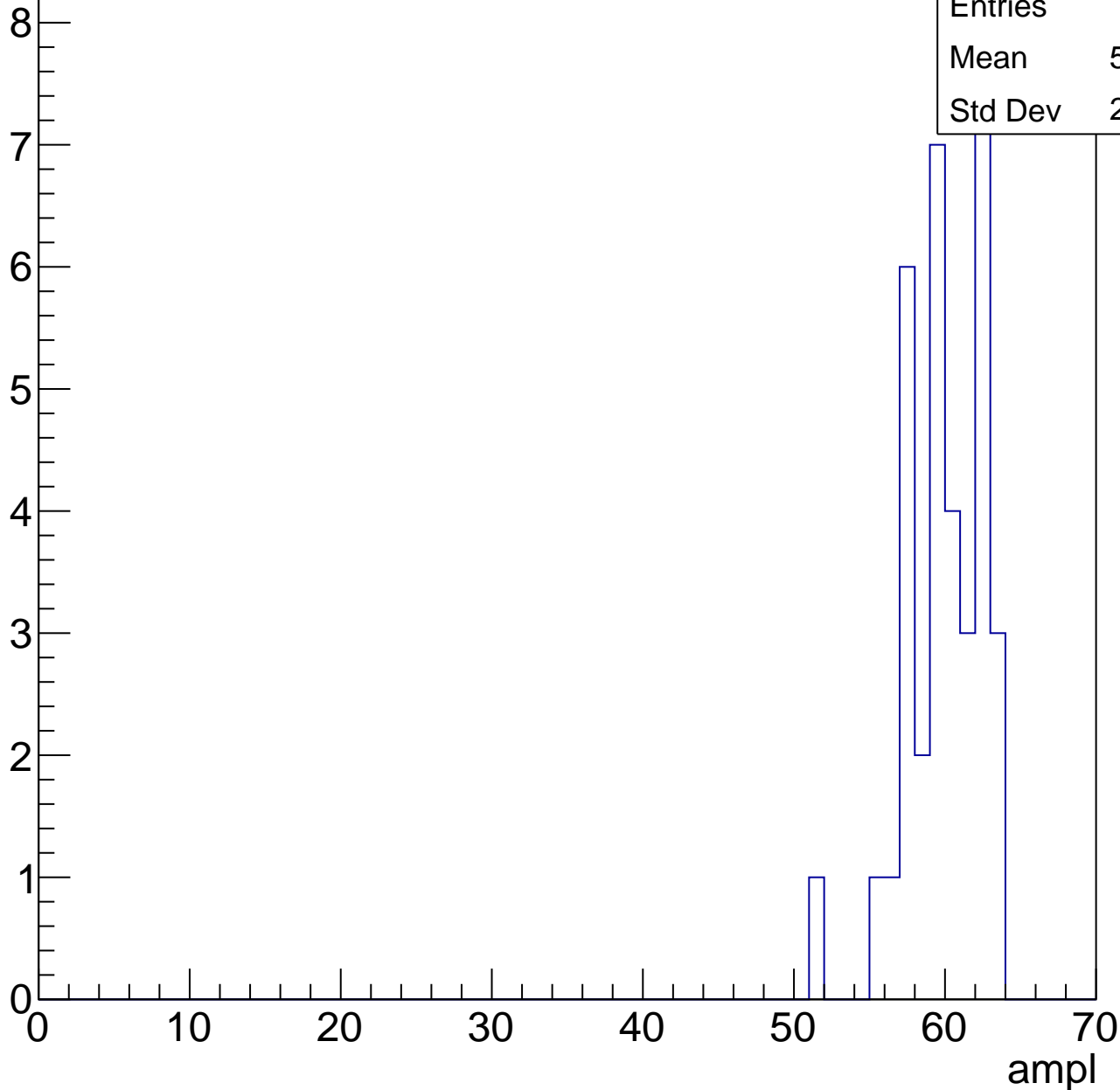


# B1L103S, U4-ch3, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 36    |
| Mean    | 59.47 |
| Std Dev | 2.598 |

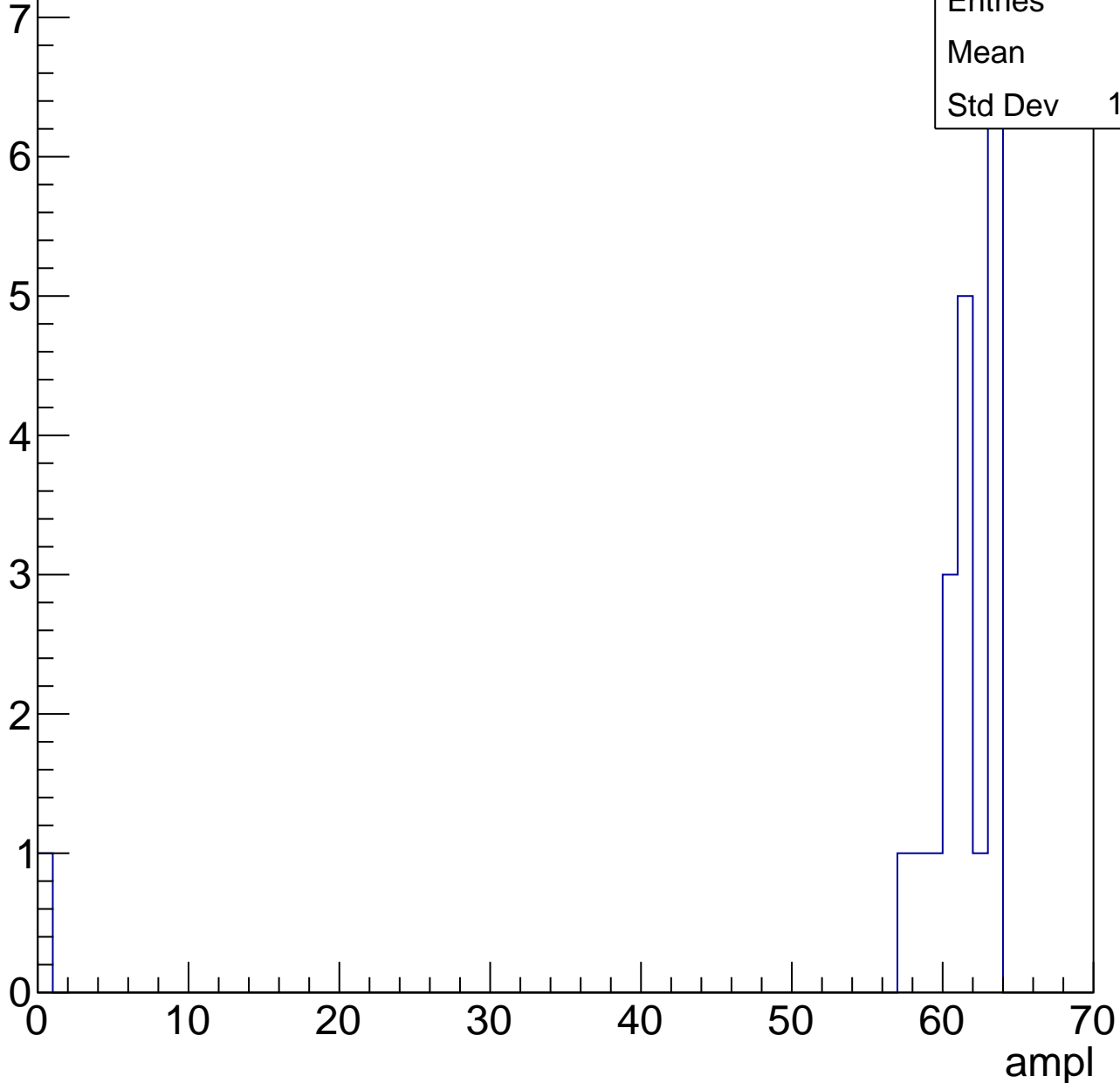


# B1L103S, U4-ch3, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 20    |
| Mean    | 58.1  |
| Std Dev | 13.44 |





# B1L103S, U4-ch3, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

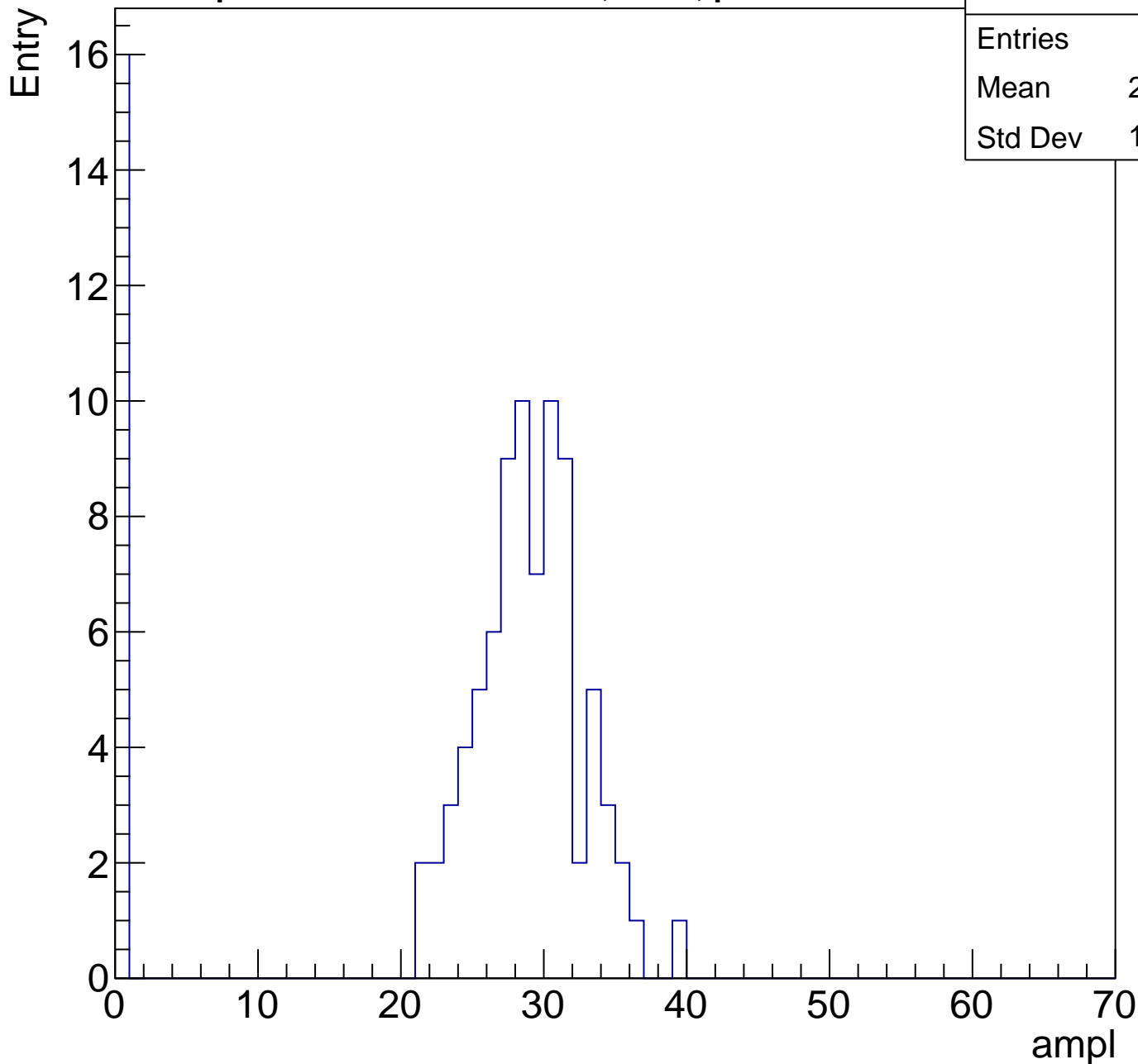
|         |    |
|---------|----|
| Entries | 19 |
| Mean    | 0  |
| Std Dev | 0  |



# B1L103S, U4-ch4, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

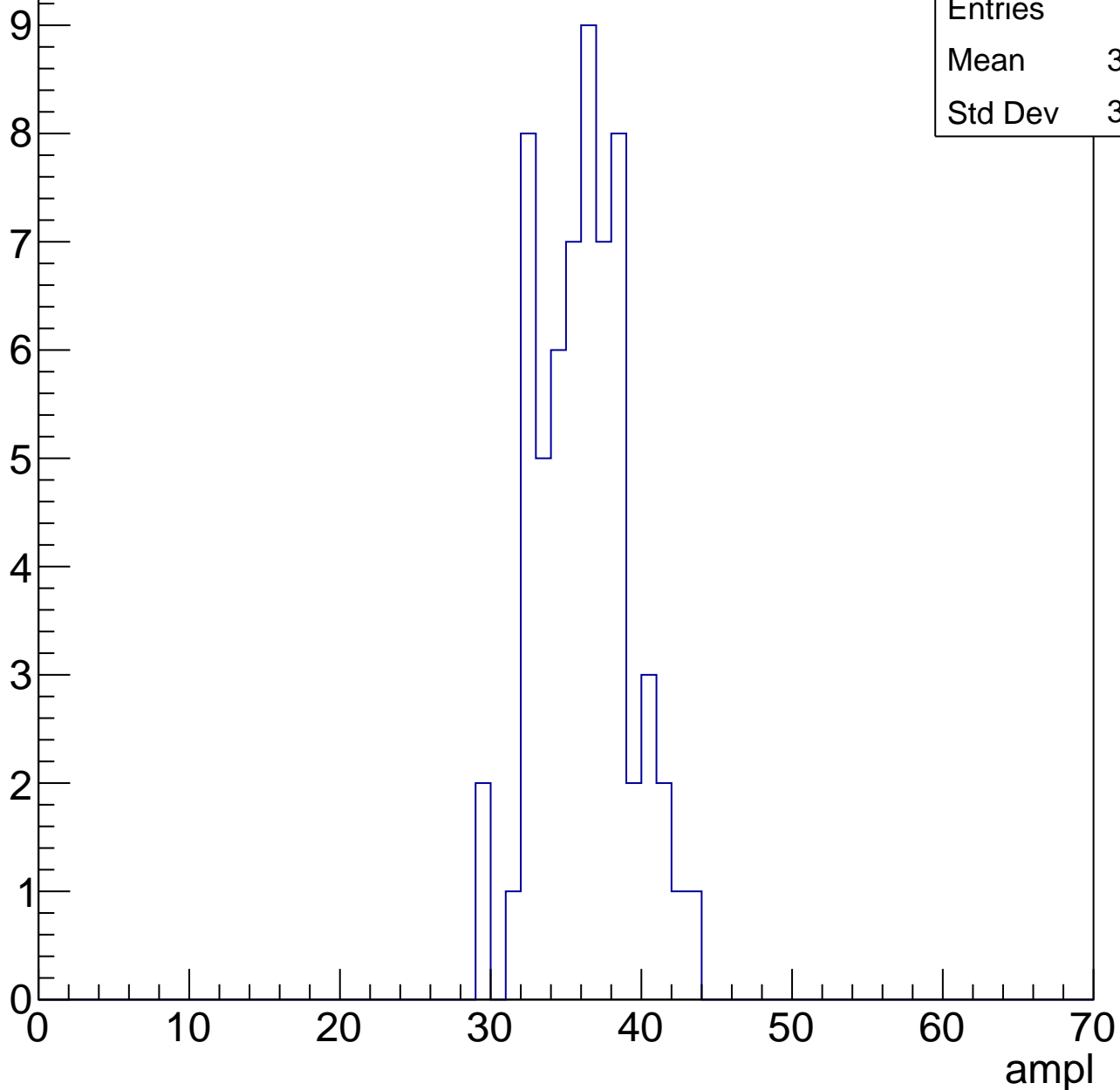
|         |       |
|---------|-------|
| Entries | 97    |
| Mean    | 23.85 |
| Std Dev | 11.09 |



# B1L103S, U4-ch4, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

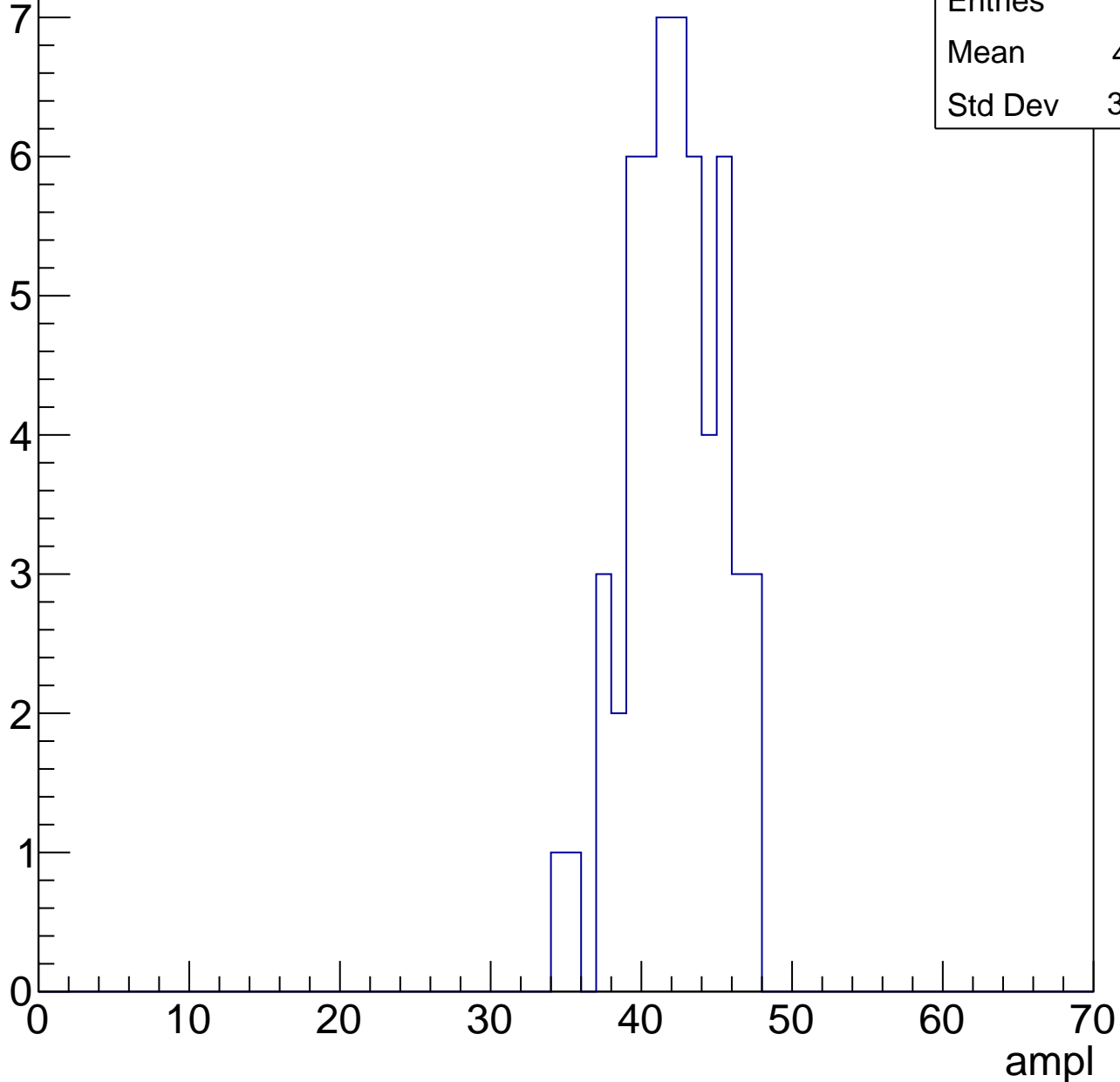


# B1L103S, U4-ch4, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 55    |
| Mean    | 41.71 |
| Std Dev | 3.013 |



# B1L103S, U4-ch4, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

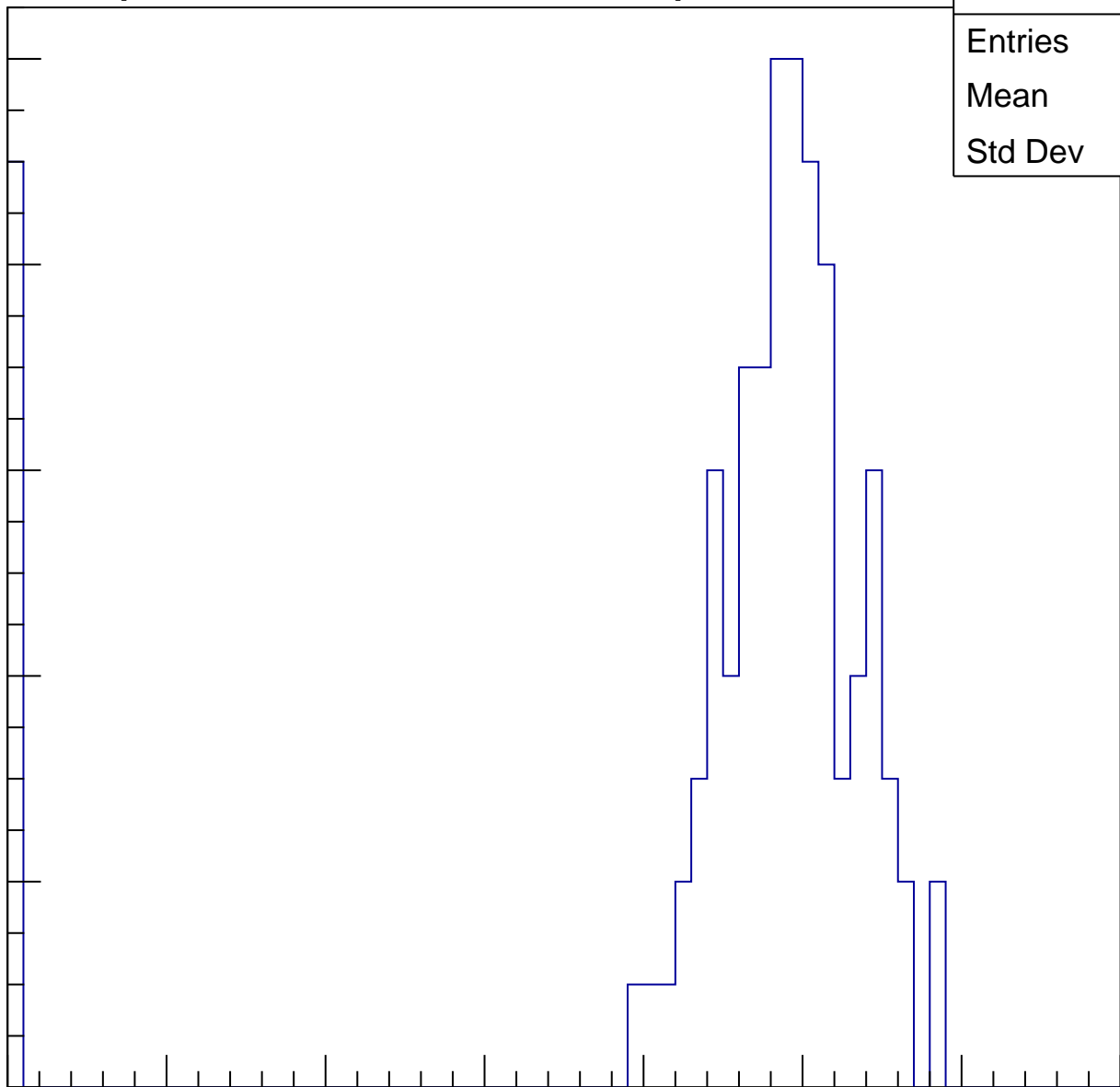
|         |       |
|---------|-------|
| Entries | 98    |
| Mean    | 44.3  |
| Std Dev | 14.59 |

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

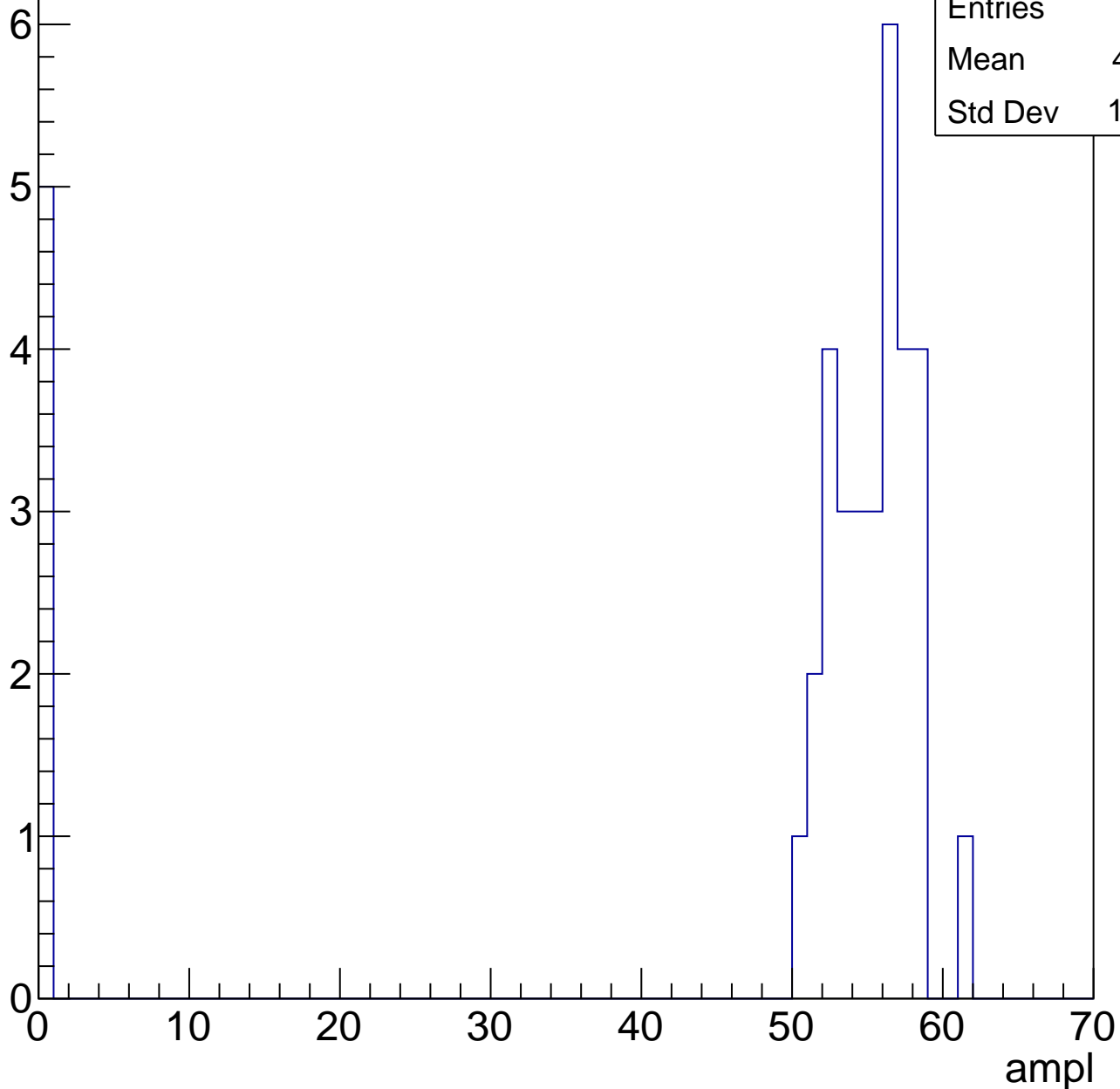


# B1L103S, U4-ch4, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 36    |
| Mean    | 47.31 |
| Std Dev | 19.15 |

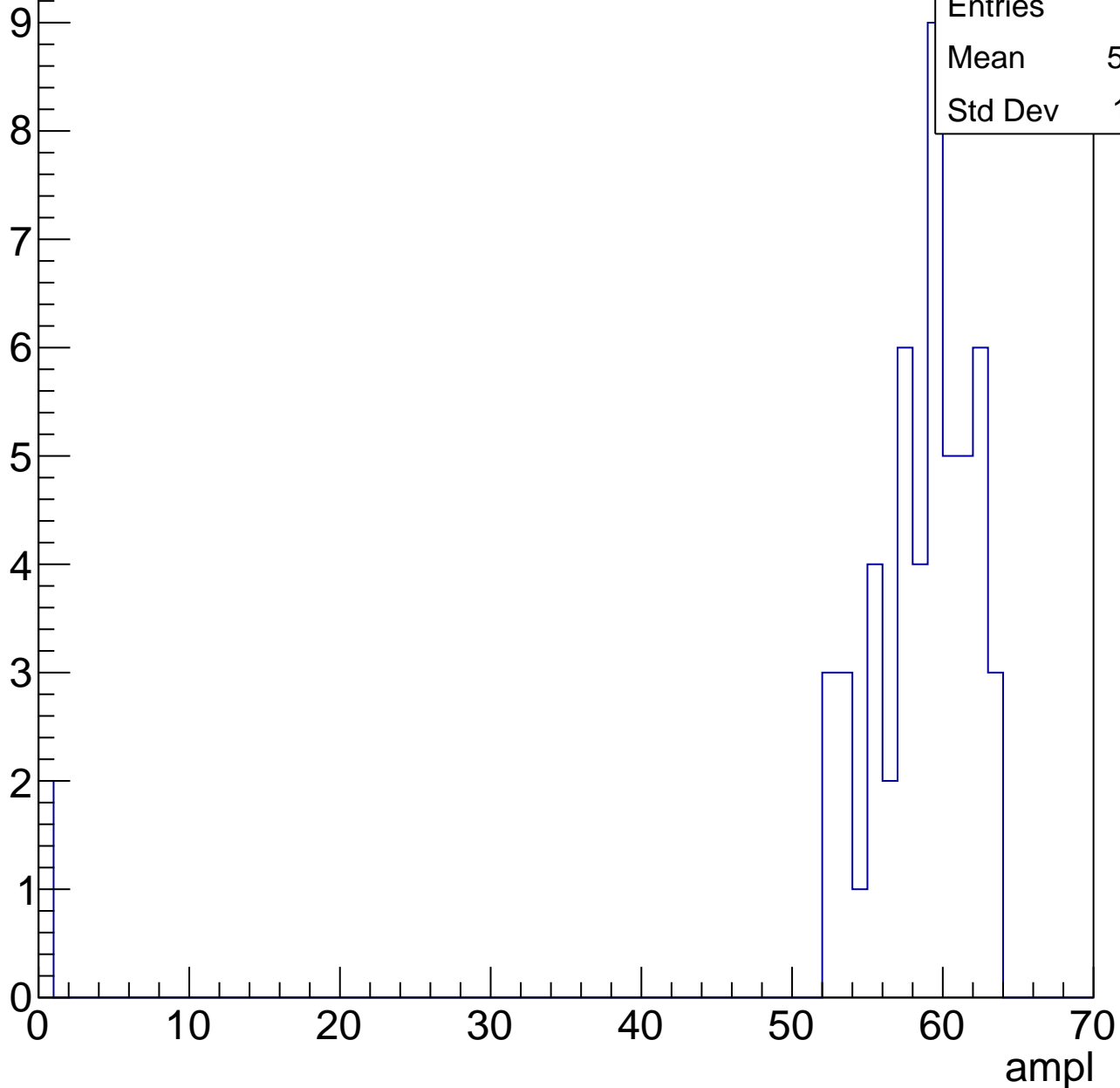


# B1L103S, U4-ch4, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 53    |
| Mean    | 56.08 |
| Std Dev | 11.51 |

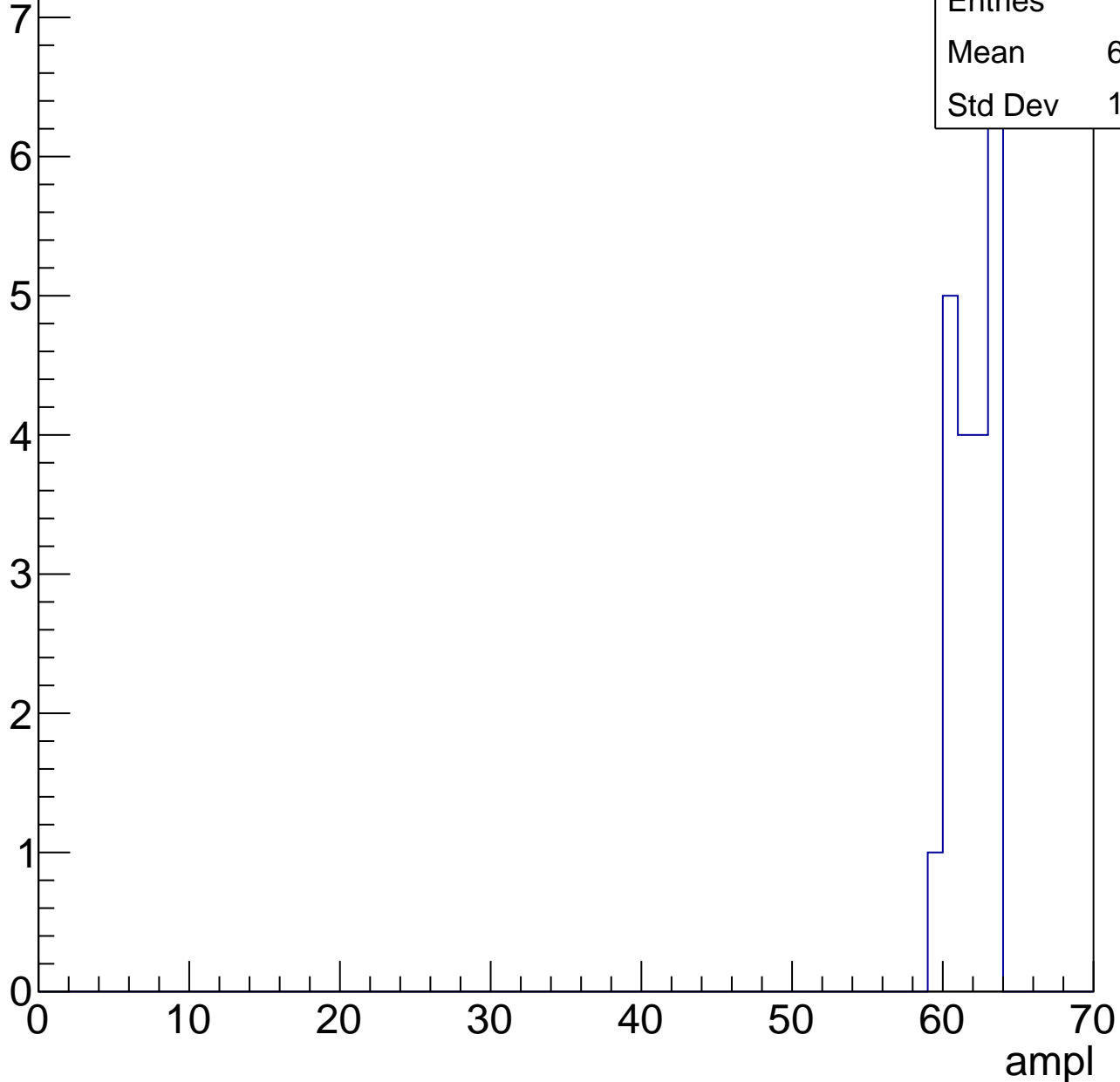


# B1L103S, U4-ch4, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 21    |
| Mean    | 61.52 |
| Std Dev | 1.295 |



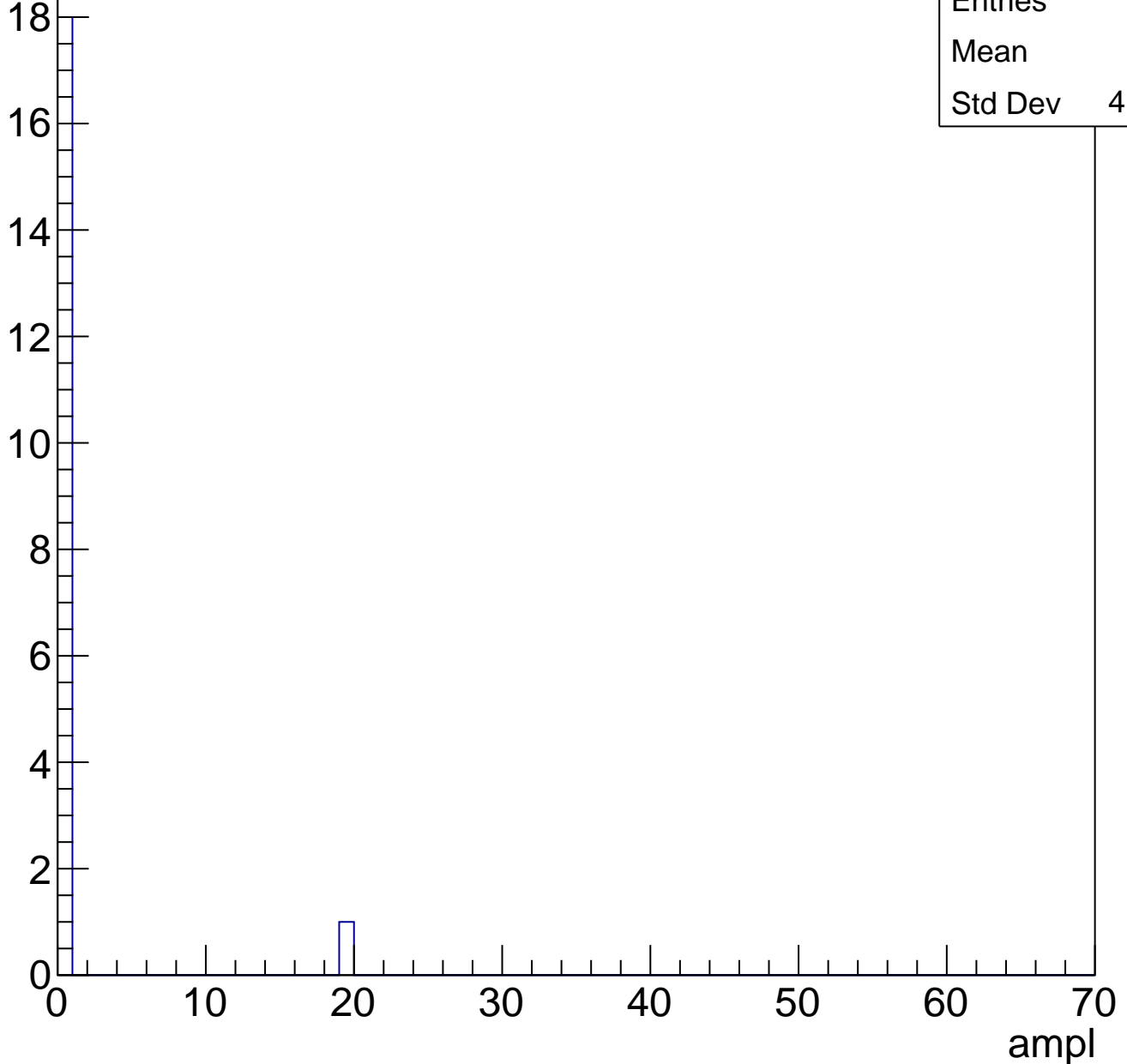


# B1L103S, U4-ch4, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 19    |
| Mean    | 1     |
| Std Dev | 4.243 |

Entry



# B1L103S, U4-ch5, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 66    |
| Mean    | 20.7  |
| Std Dev | 12.39 |

Entry

16  
14  
12  
10  
8  
6  
4  
2  
0

0

10

20

30

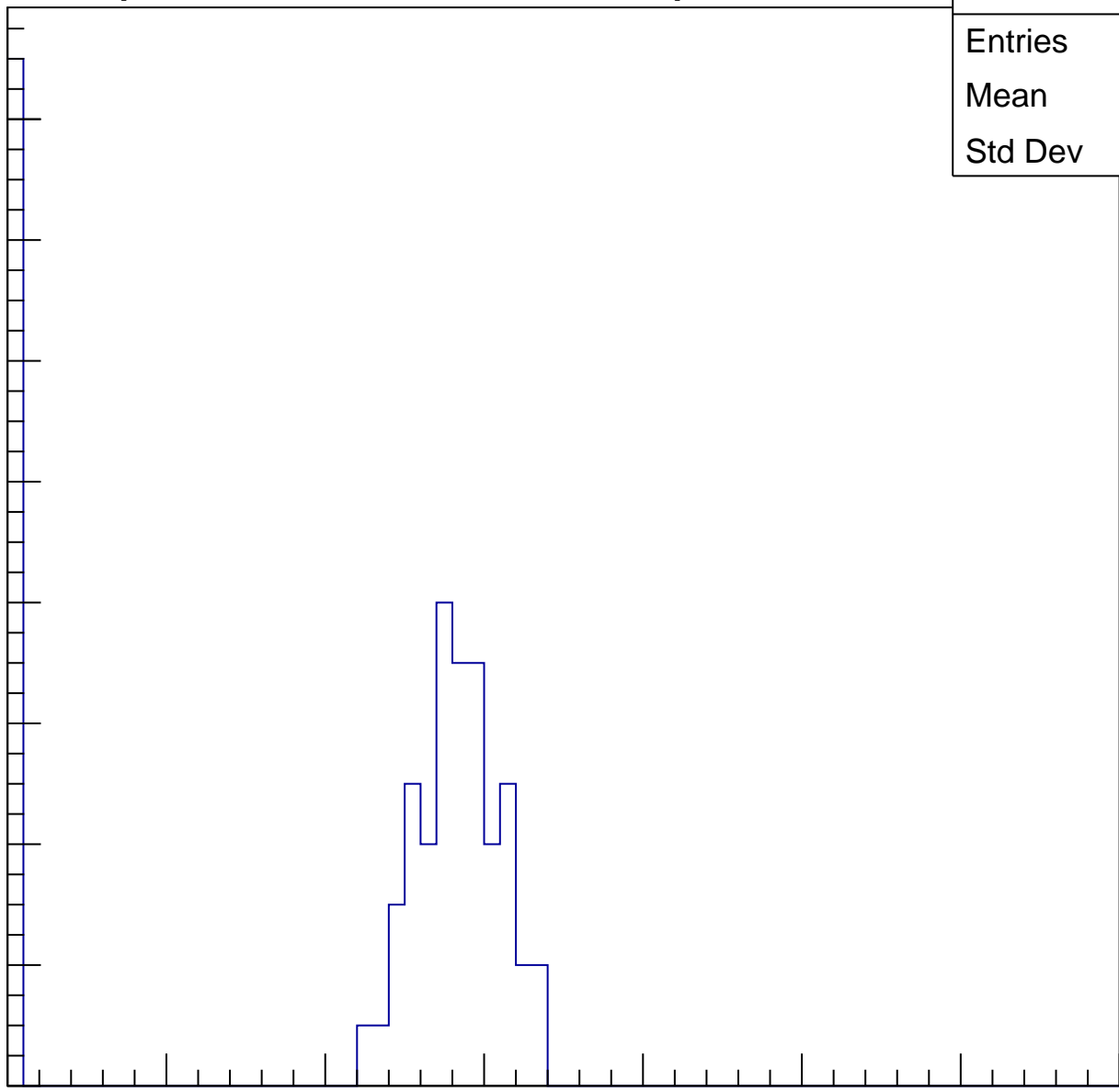
40

50

60

70

ampl

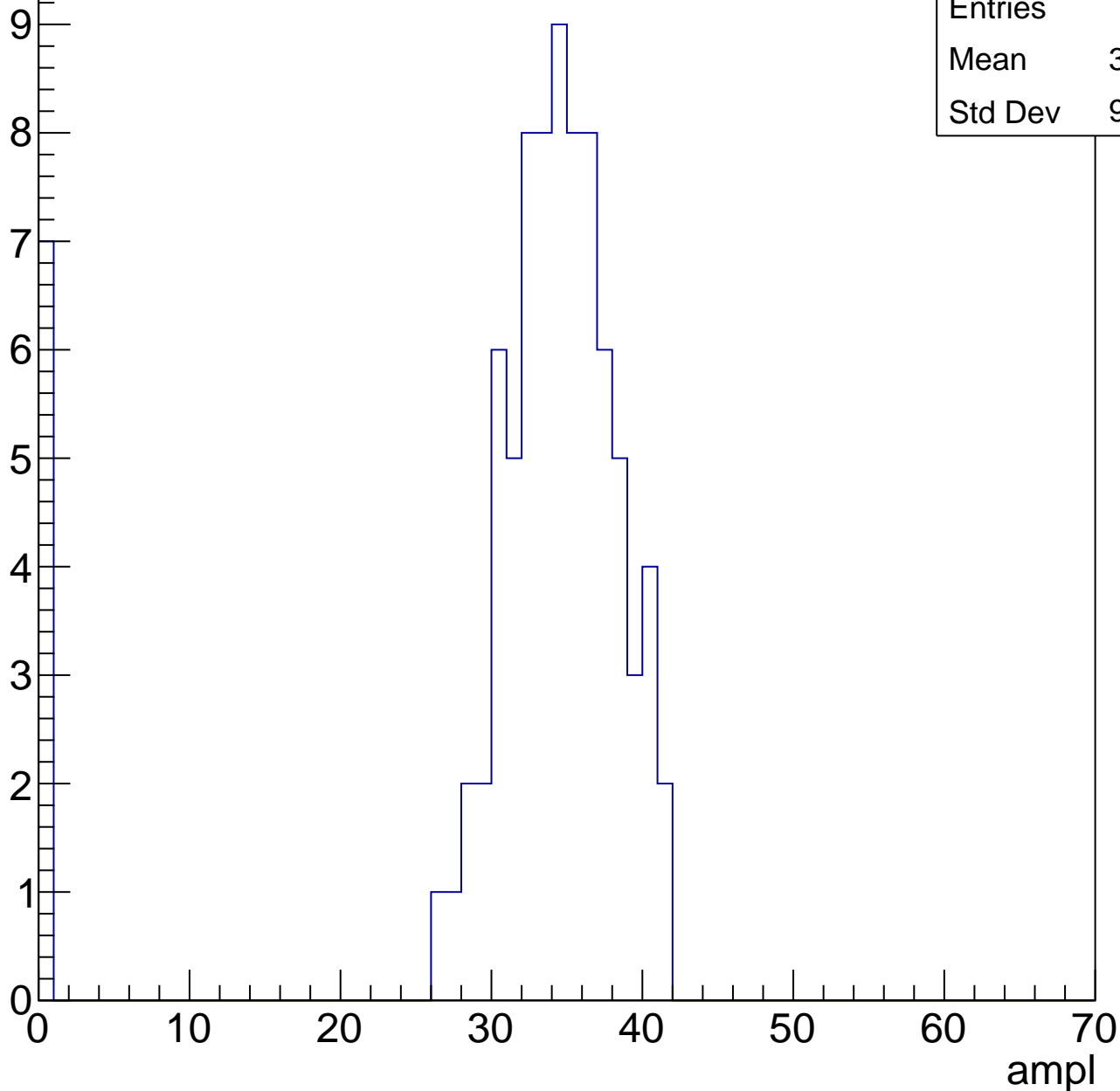


# B1L103S, U4-ch5, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 85    |
| Mean    | 31.38 |
| Std Dev | 9.949 |

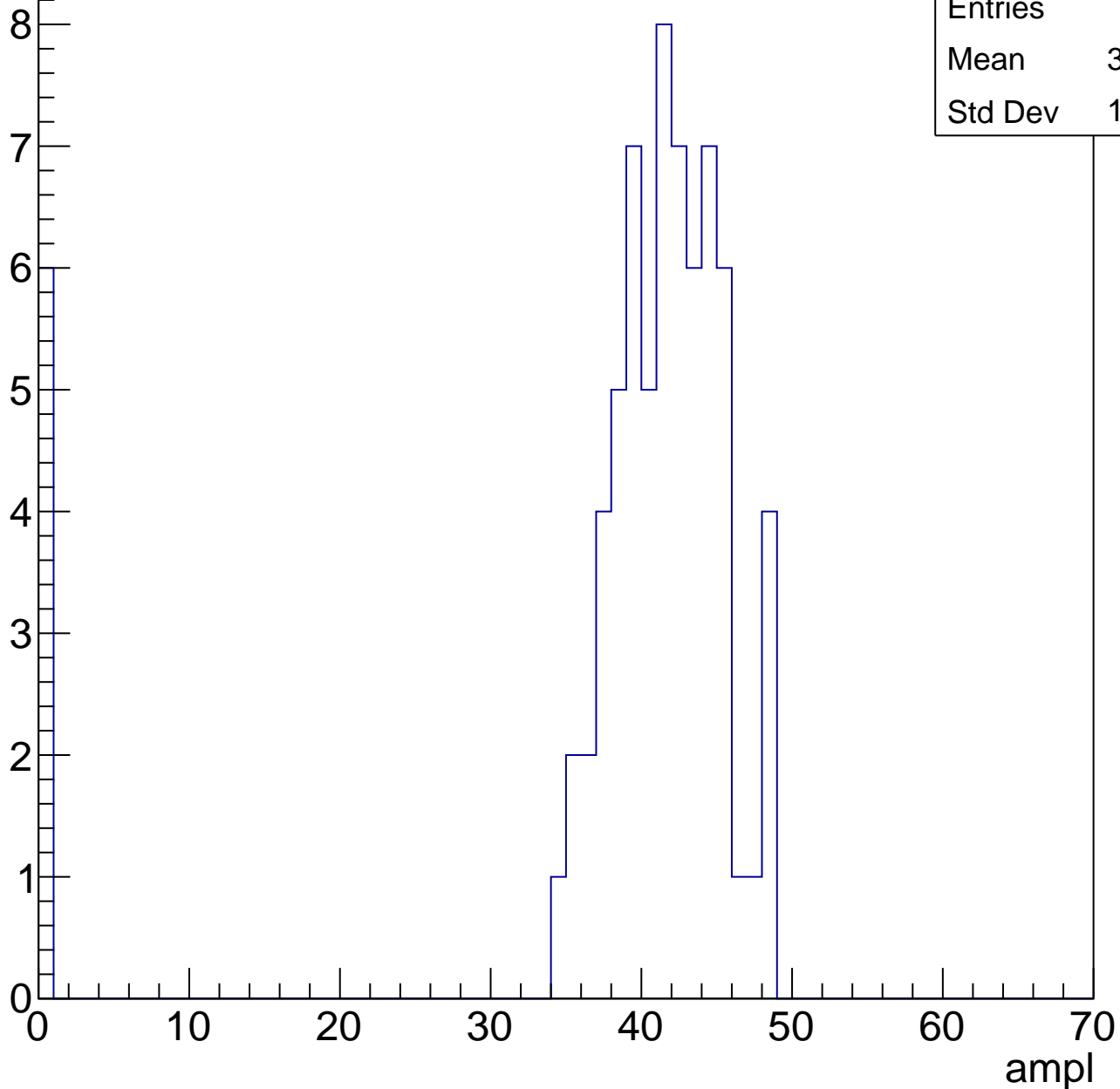


# B1L103S, U4-ch5, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 72    |
| Mean    | 37.92 |
| Std Dev | 11.88 |

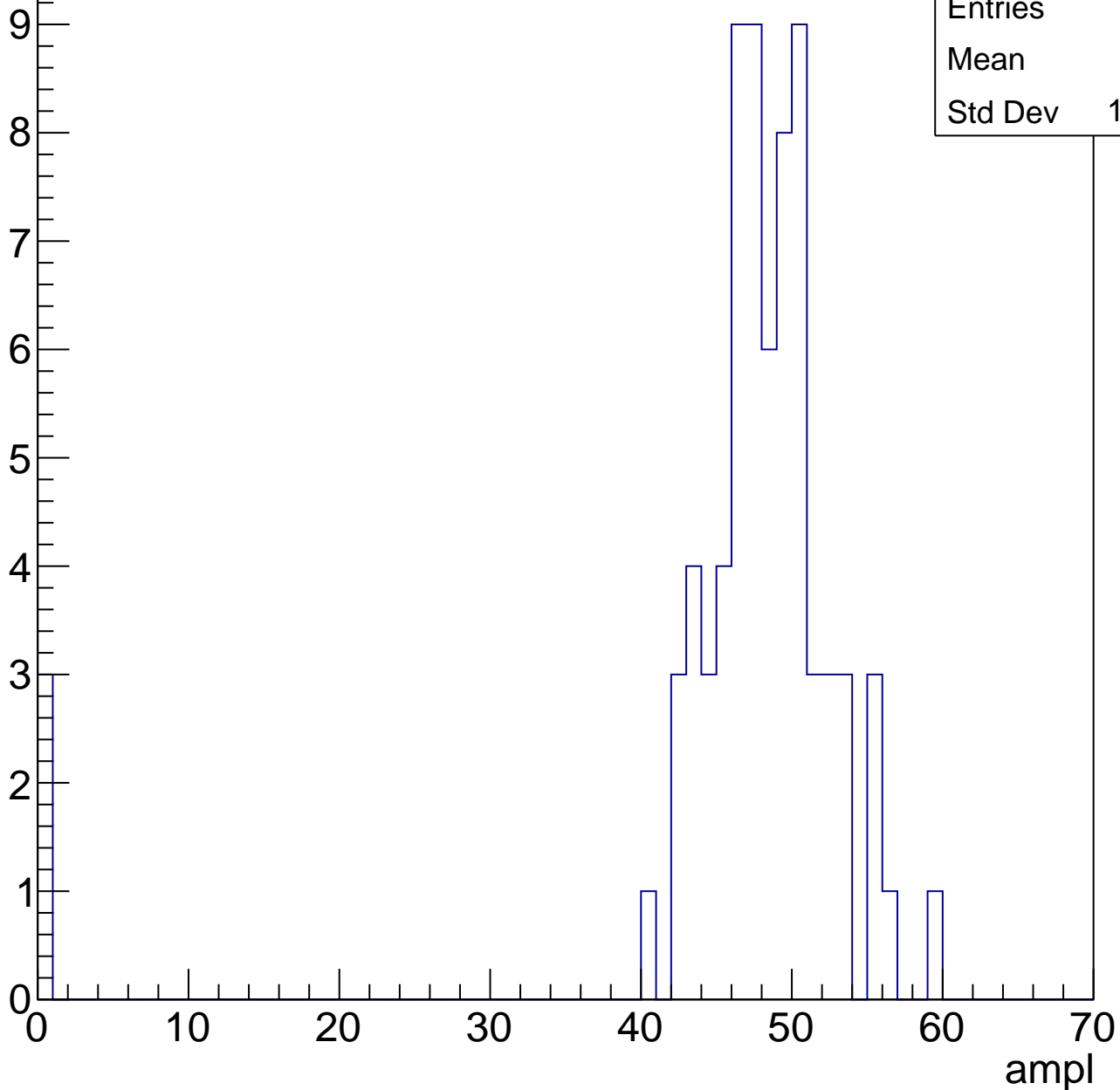


# B1L103S, U4-ch5, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

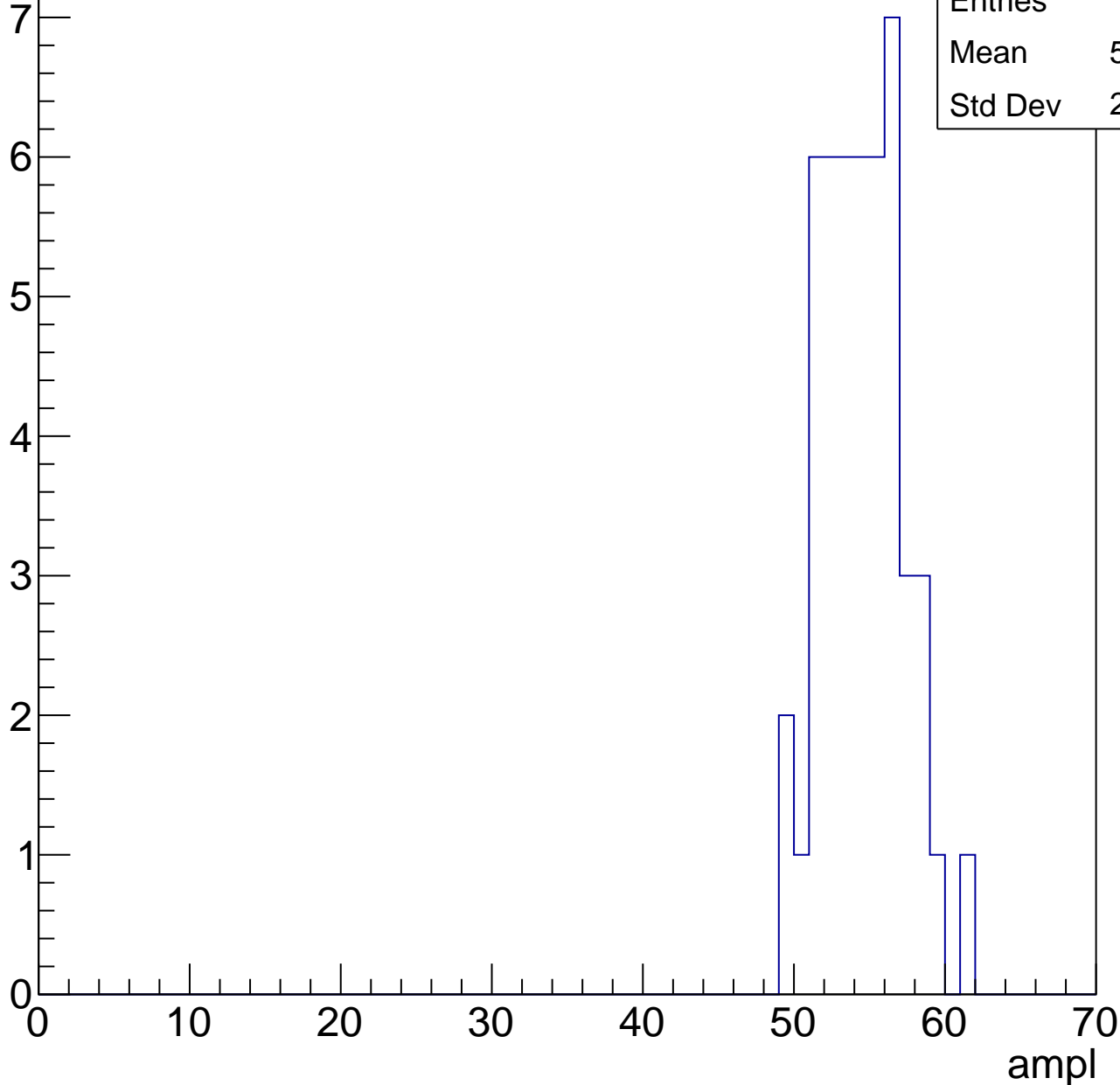
|         |       |
|---------|-------|
| Entries | 73    |
| Mean    | 46.1  |
| Std Dev | 10.19 |



# B1L103S, U4-ch5, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



|         |       |
|---------|-------|
| Entries | 48    |
| Mean    | 54.06 |
| Std Dev | 2.633 |

# B1L103S, U4-ch5, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 64    |
| Mean    | 58.17 |
| Std Dev | 7.879 |

Entry

10

8

6

4

2

0

0

10

20

30

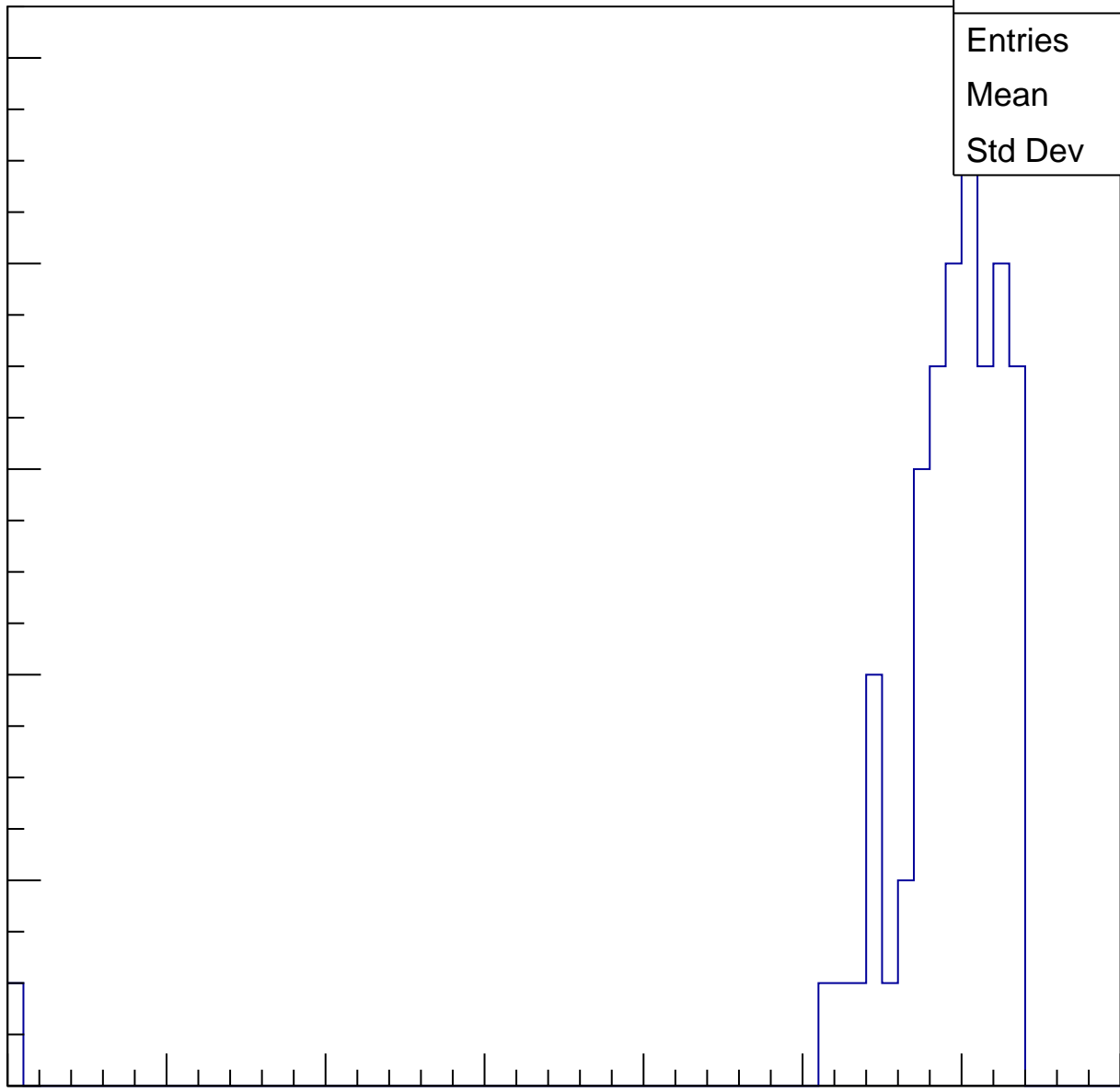
40

50

60

70

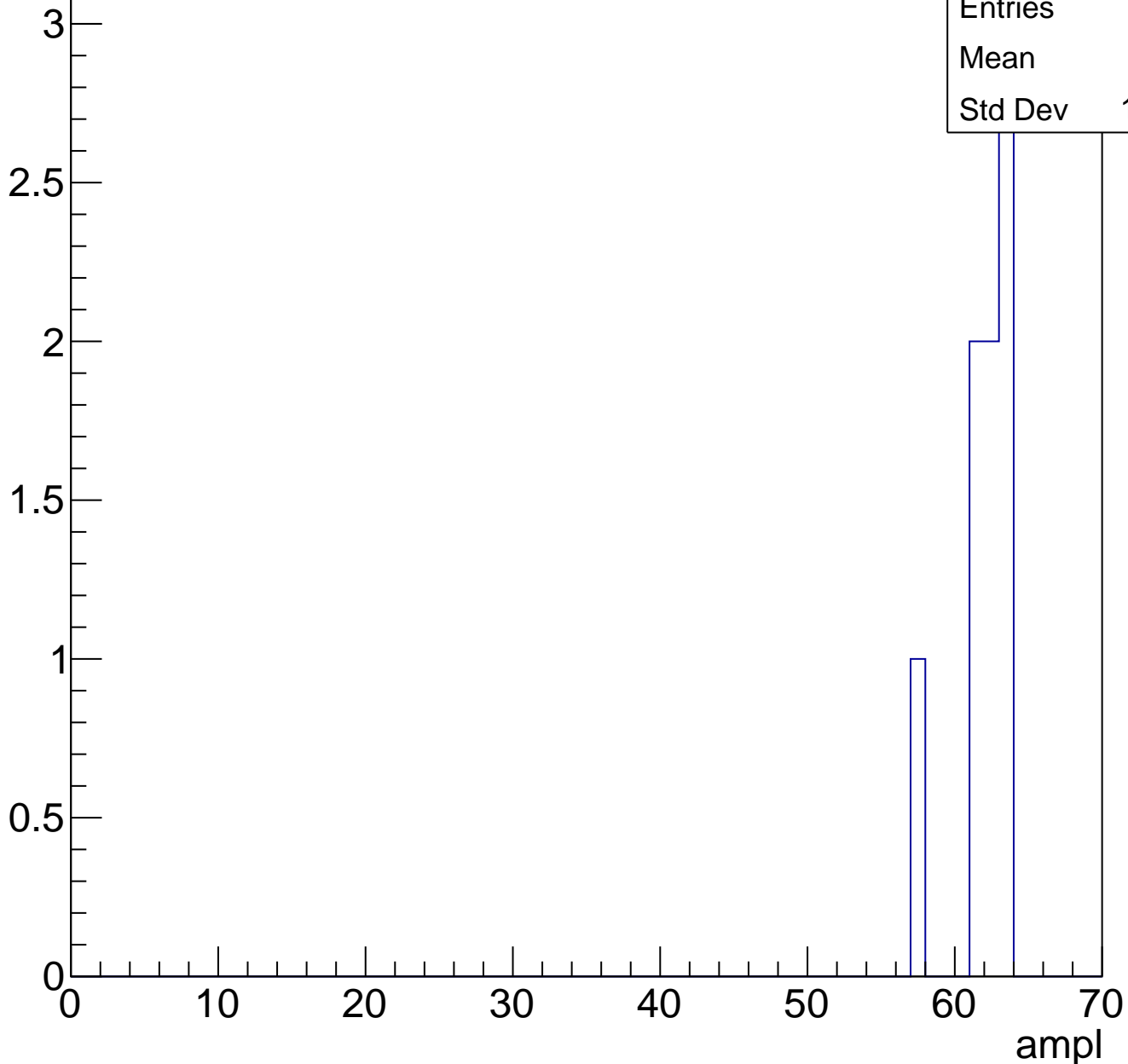
ampl



# B1L103S, U4-ch5, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



|         |       |
|---------|-------|
| Entries | 8     |
| Mean    | 61.5  |
| Std Dev | 1.871 |



# B1L103S, U4-ch5, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

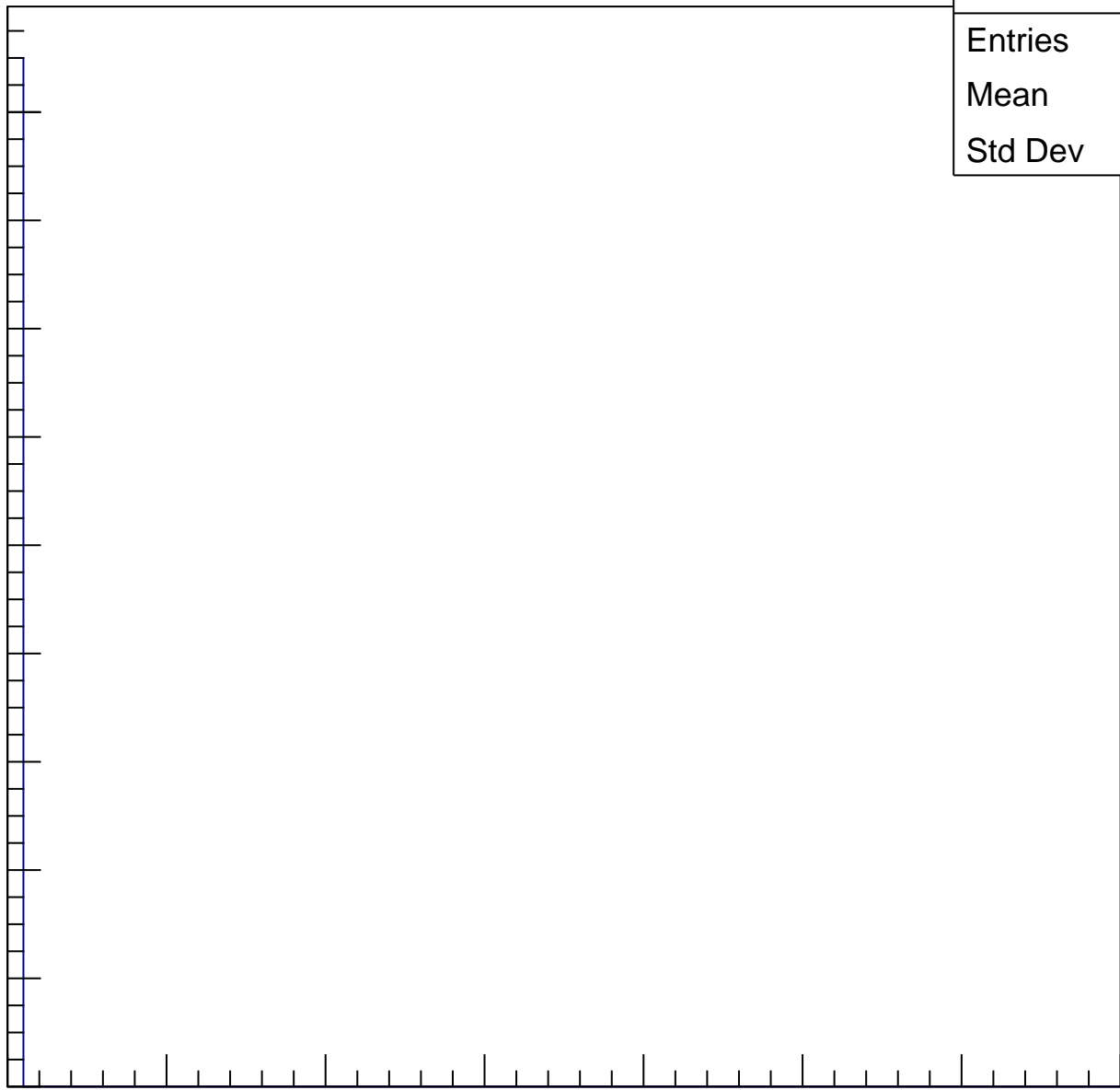
|         |    |
|---------|----|
| Entries | 19 |
| Mean    | 0  |
| Std Dev | 0  |

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L103S, U4-ch6, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

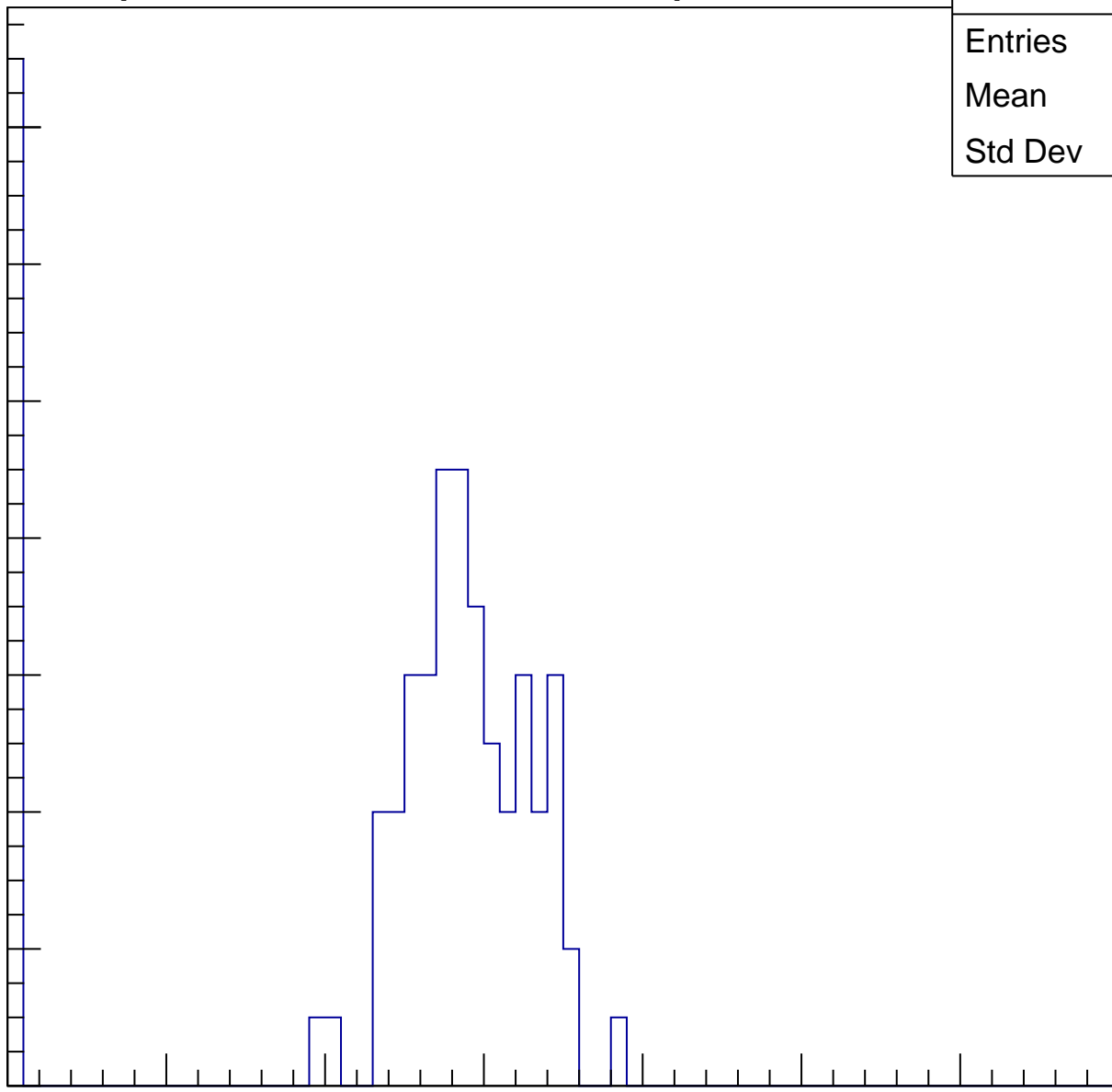
|         |       |
|---------|-------|
| Entries | 90    |
| Mean    | 23.79 |
| Std Dev | 11.17 |

Entry

14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

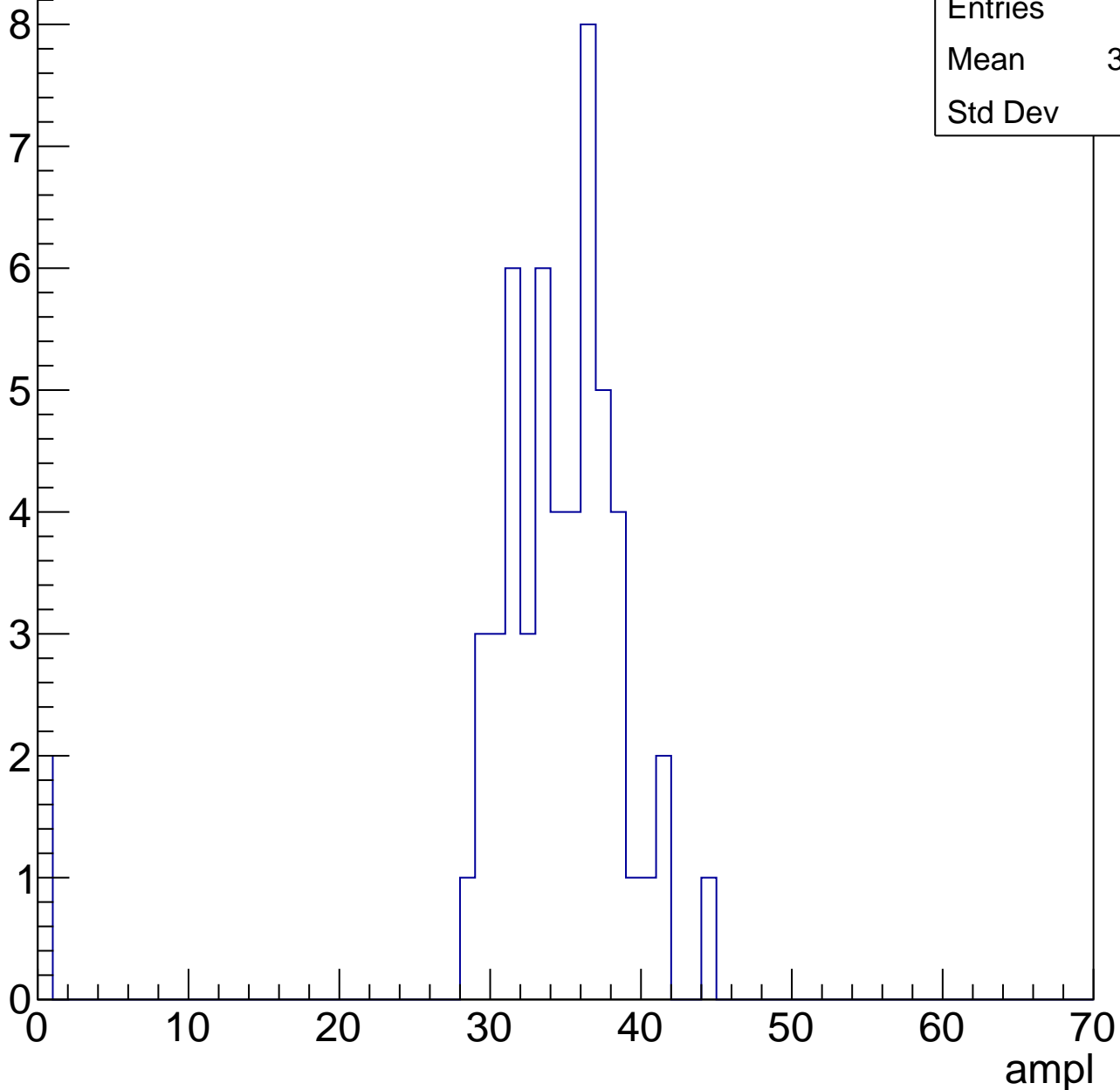


# B1L103S, U4-ch6, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 54    |
| Mean    | 33.17 |
| Std Dev | 7.34  |



# B1L103S, U4-ch6, adc2

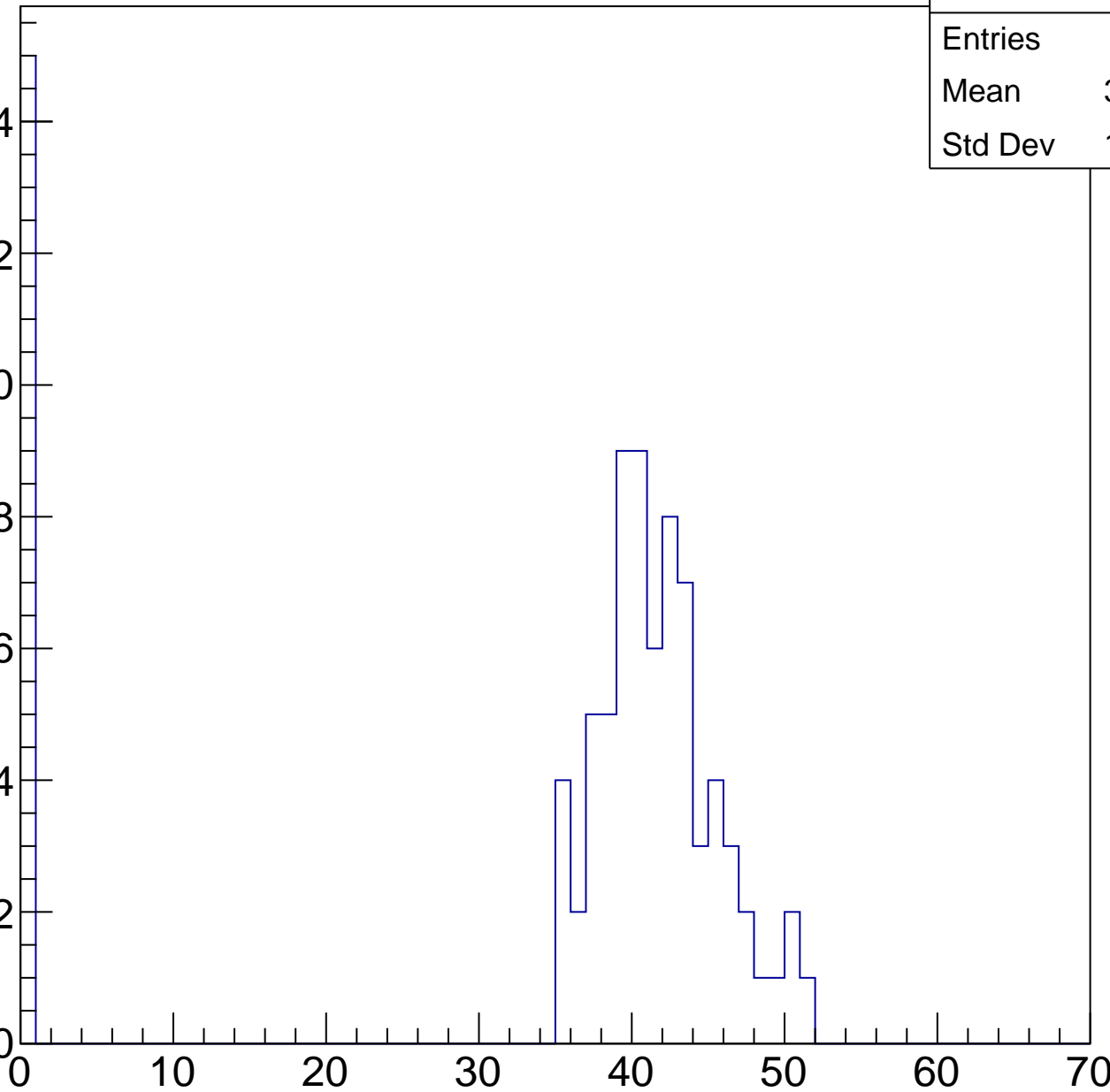
calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 87    |
| Mean    | 34.17 |
| Std Dev | 15.96 |

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl

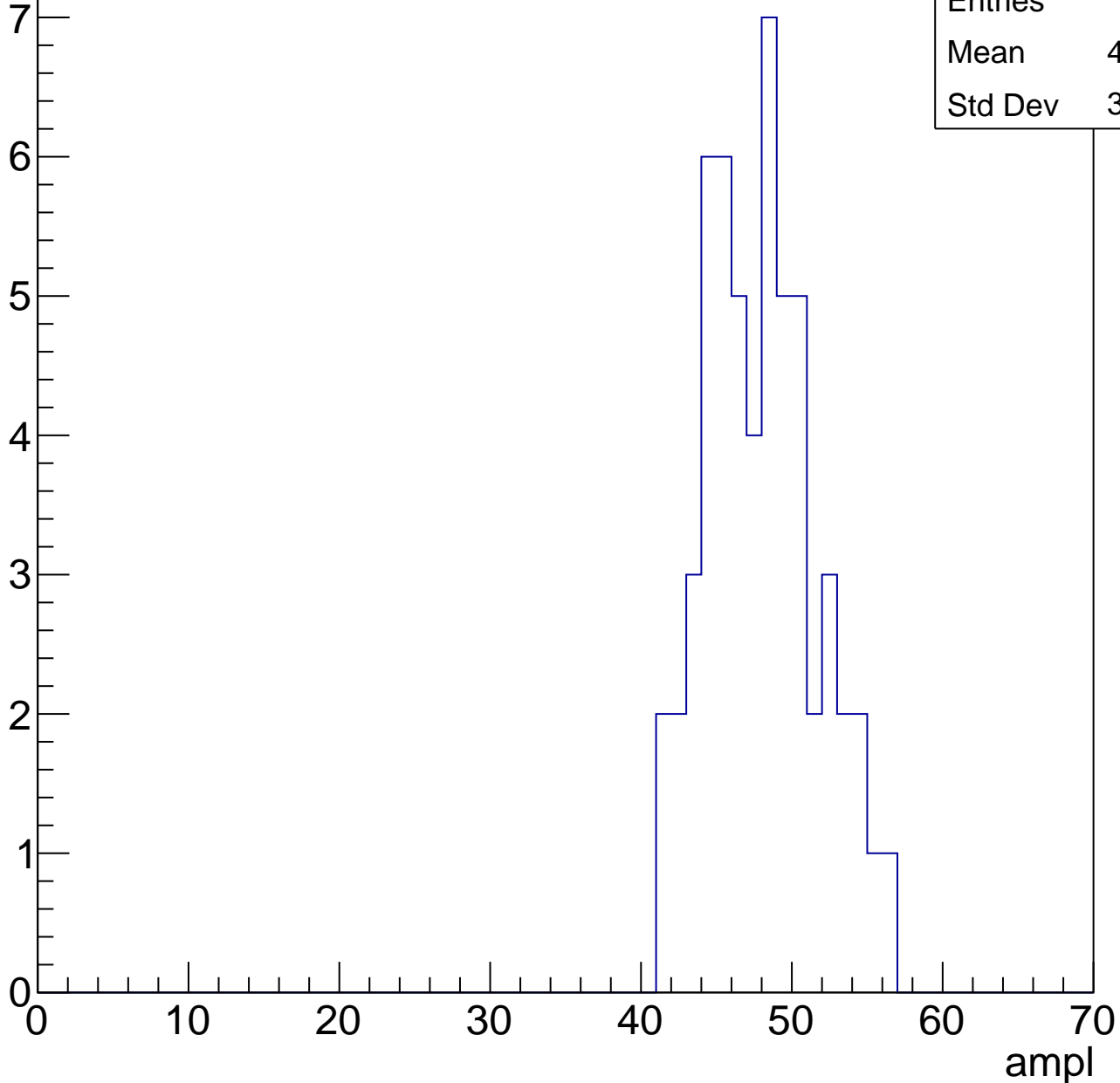


# B1L103S, U4-ch6, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 56    |
| Mean    | 47.52 |
| Std Dev | 3.615 |

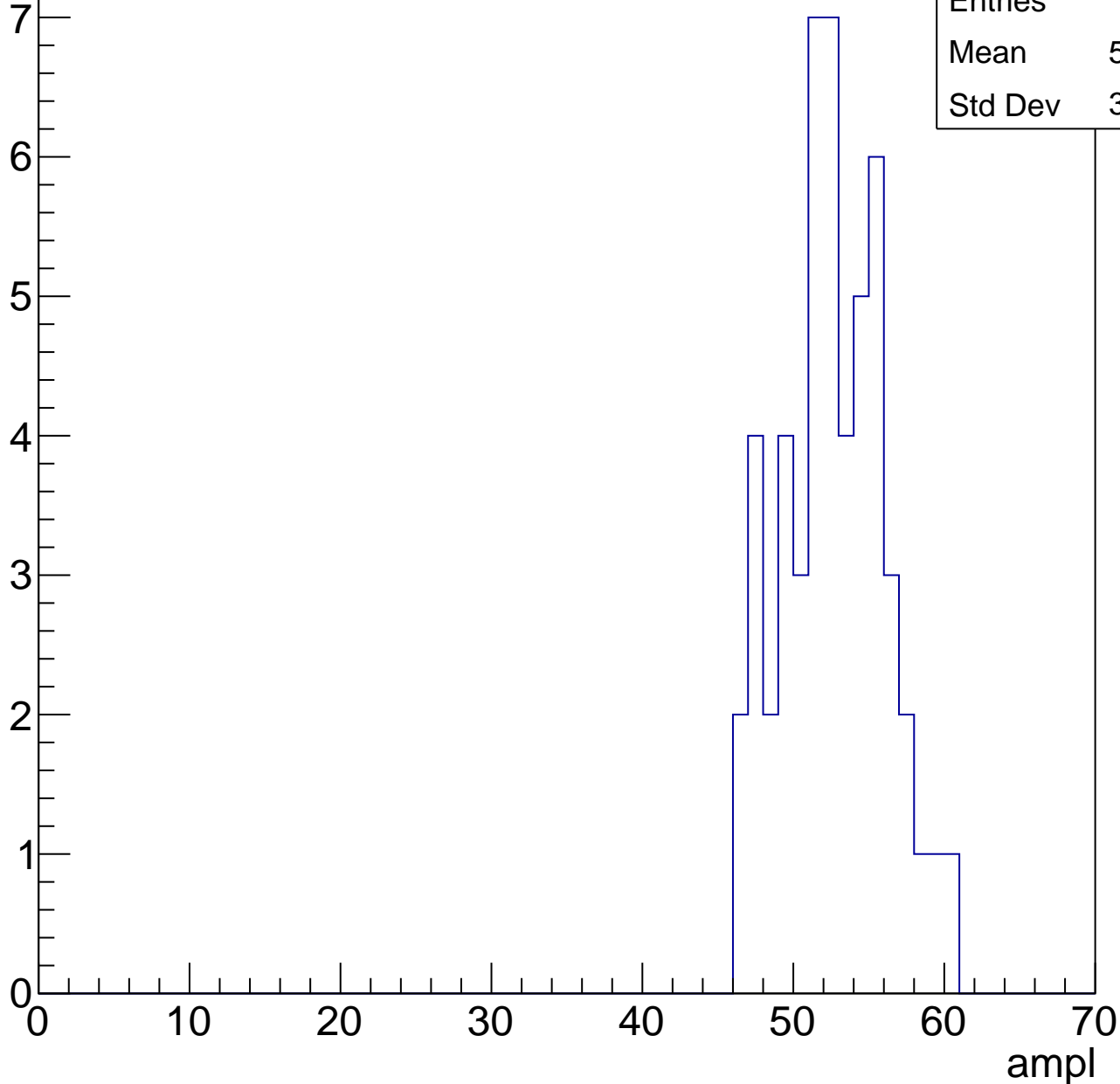


# B1L103S, U4-ch6, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 52    |
| Mean    | 52.19 |
| Std Dev | 3.346 |



# B1L103S, U4-ch6, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

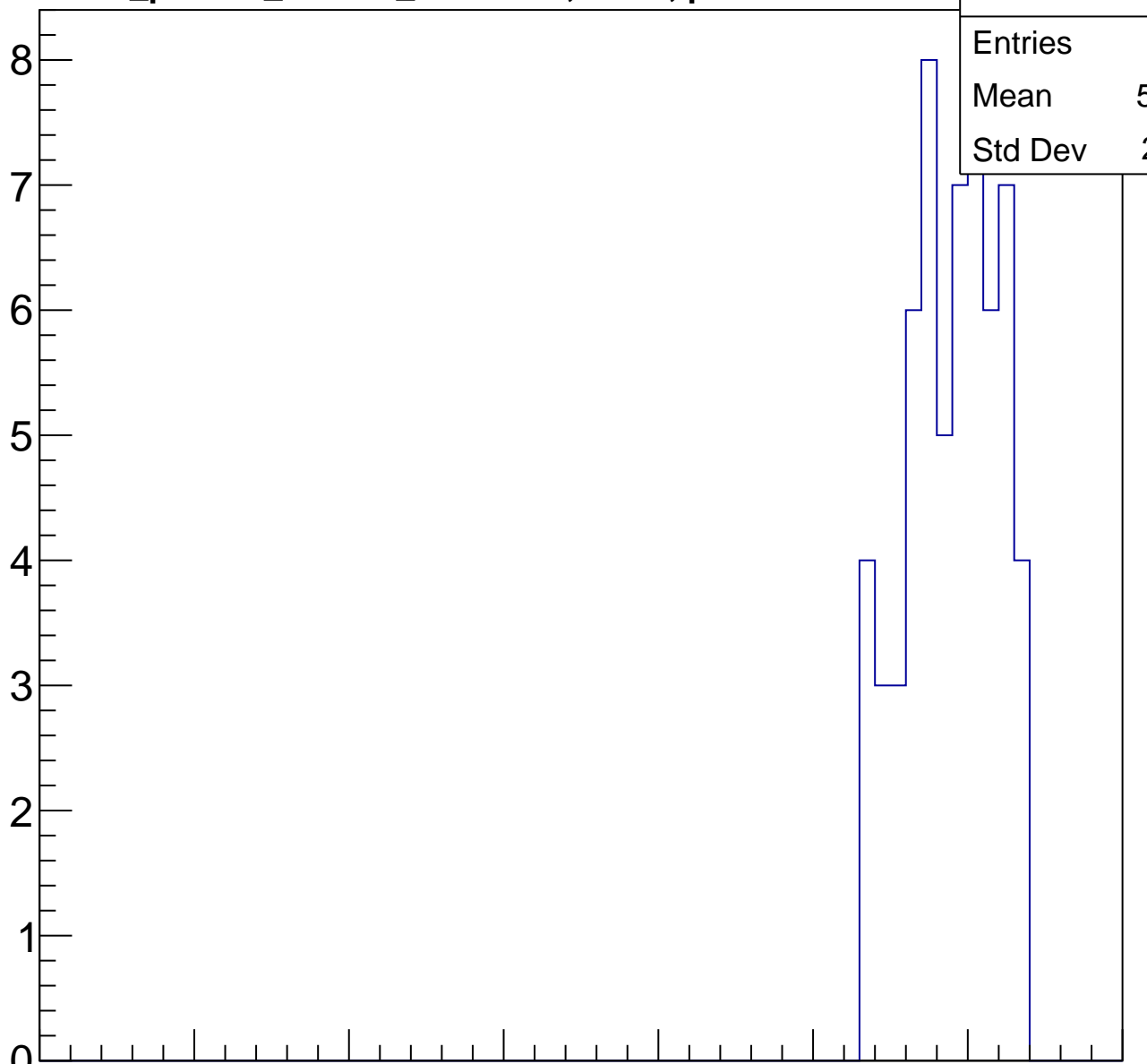
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

|         |       |
|---------|-------|
| Entries | 61    |
| Mean    | 58.46 |
| Std Dev | 2.861 |

ampl

0 10 20 30 40 50 60 70

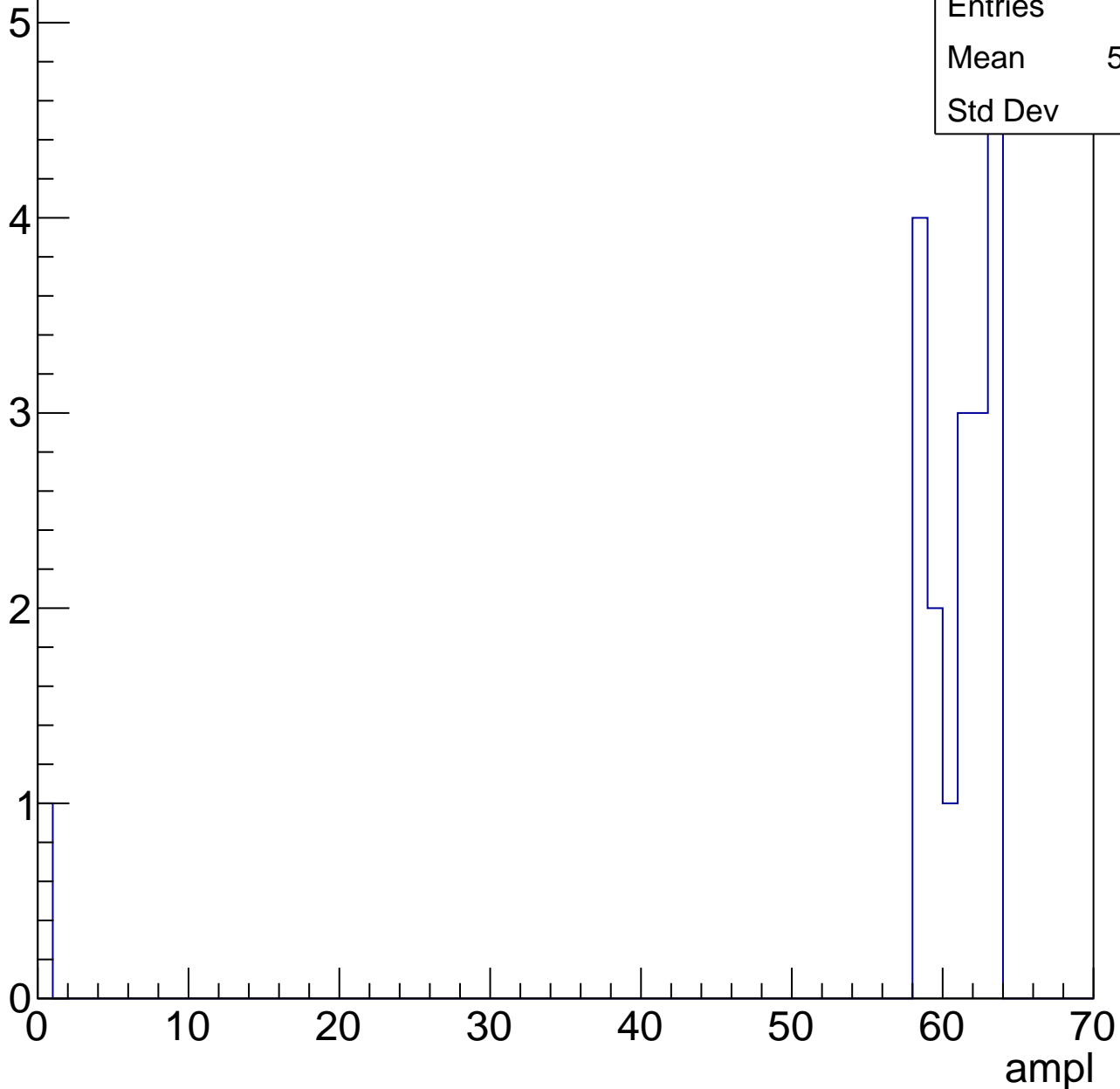


# B1L103S, U4-ch6, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 19    |
| Mean    | 57.58 |
| Std Dev | 13.7  |

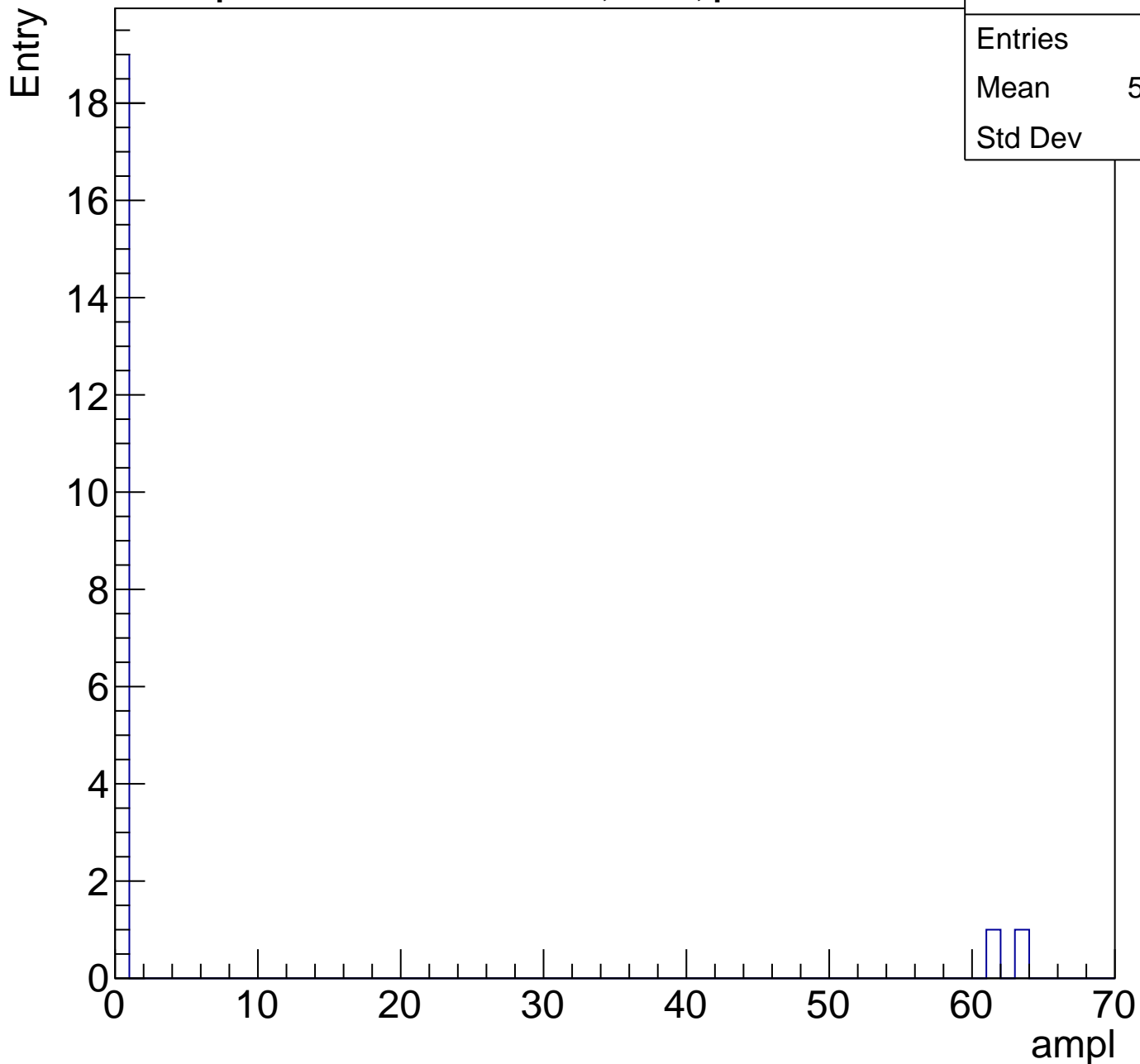




# B1L103S, U4-ch6, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

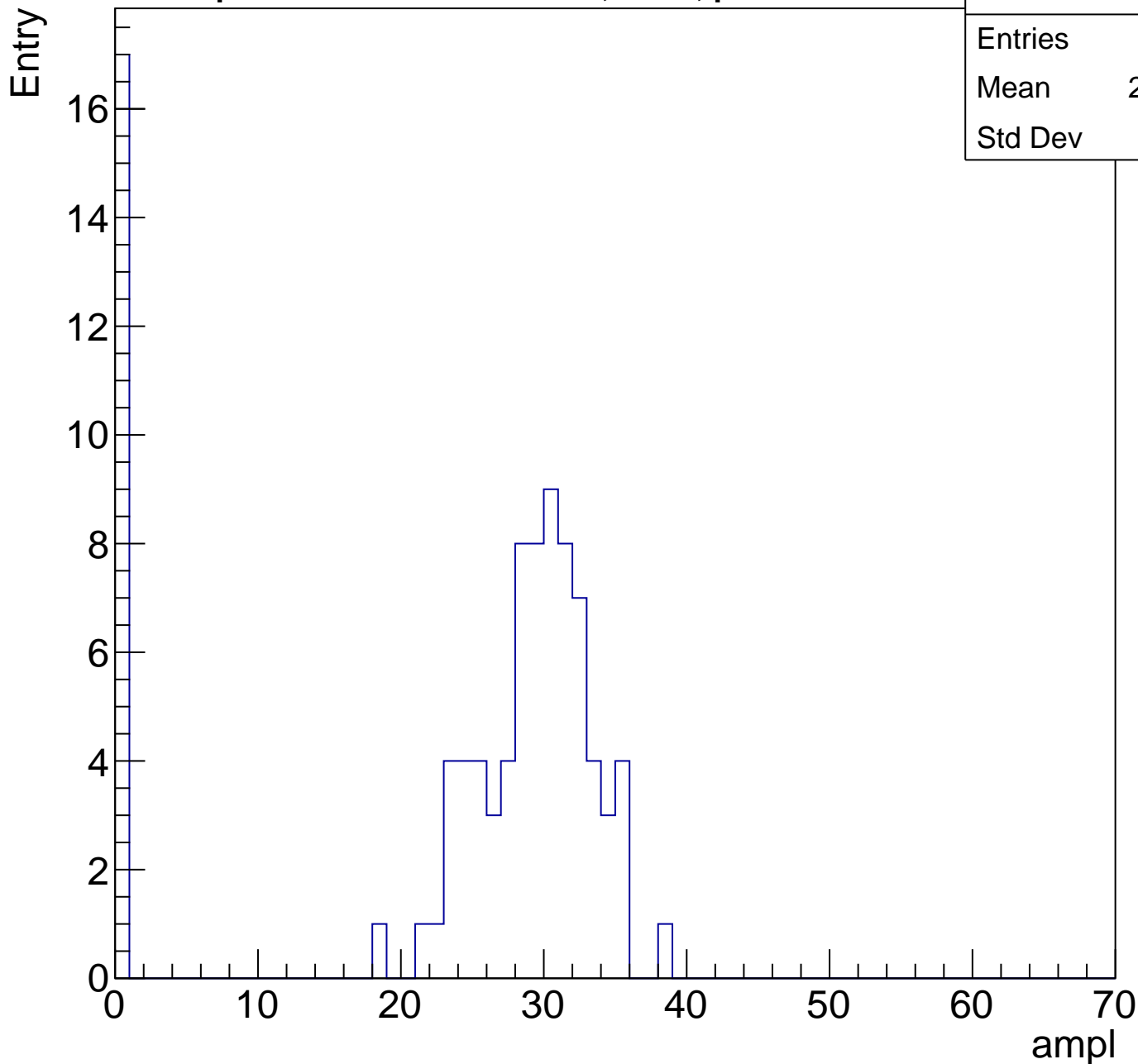
|         |       |
|---------|-------|
| Entries | 21    |
| Mean    | 5.905 |
| Std Dev | 18.2  |



# B1L103S, U4-ch7, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 91    |
| Mean    | 23.57 |
| Std Dev | 11.8  |

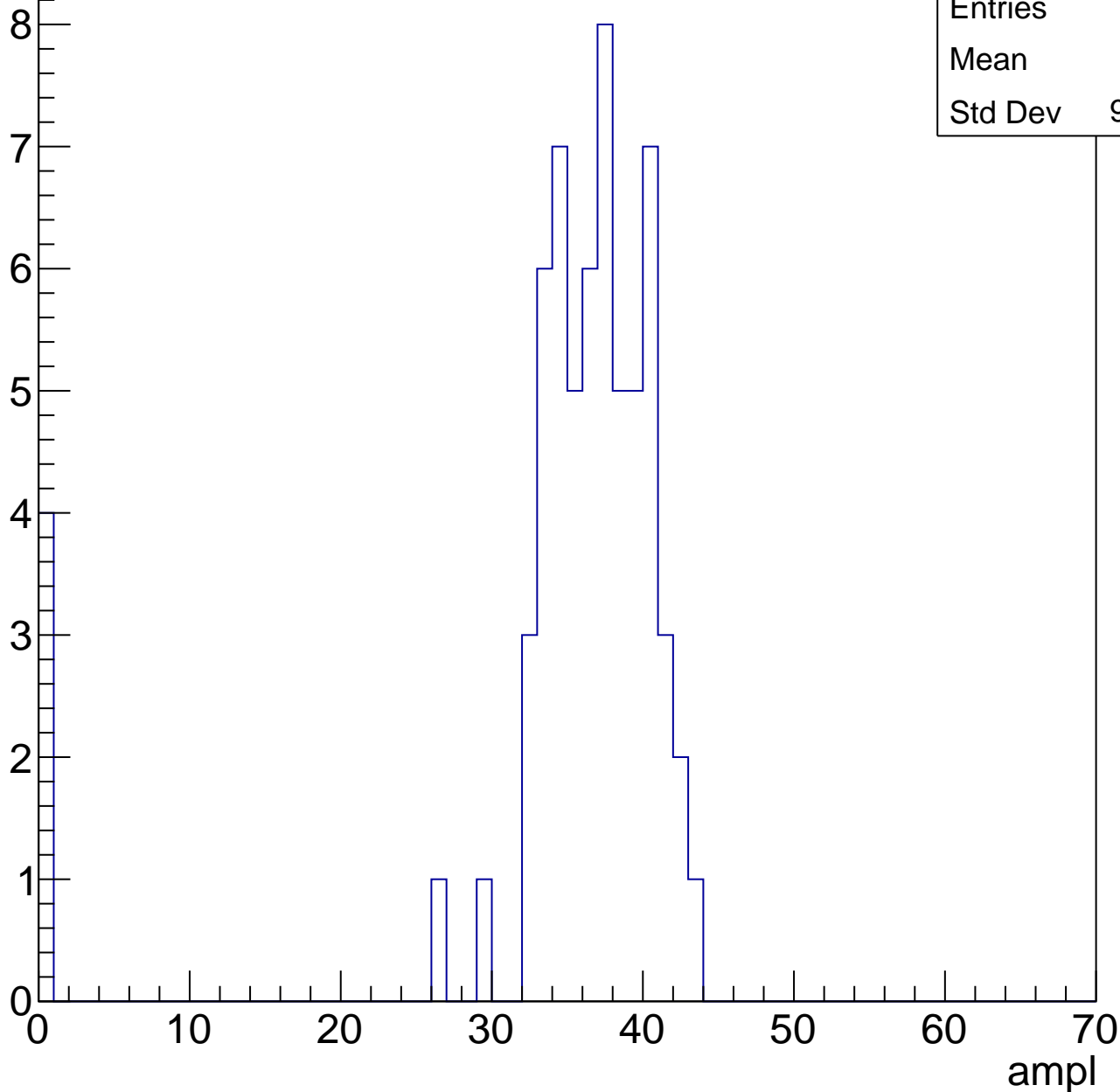


# B1L103S, U4-ch7, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 64    |
| Mean    | 34.2  |
| Std Dev | 9.389 |



# B1L103S, U4-ch7, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 82    |
| Mean    | 36.91 |
| Std Dev | 14.95 |

Entry

10

8

6

4

2

0

0

10

20

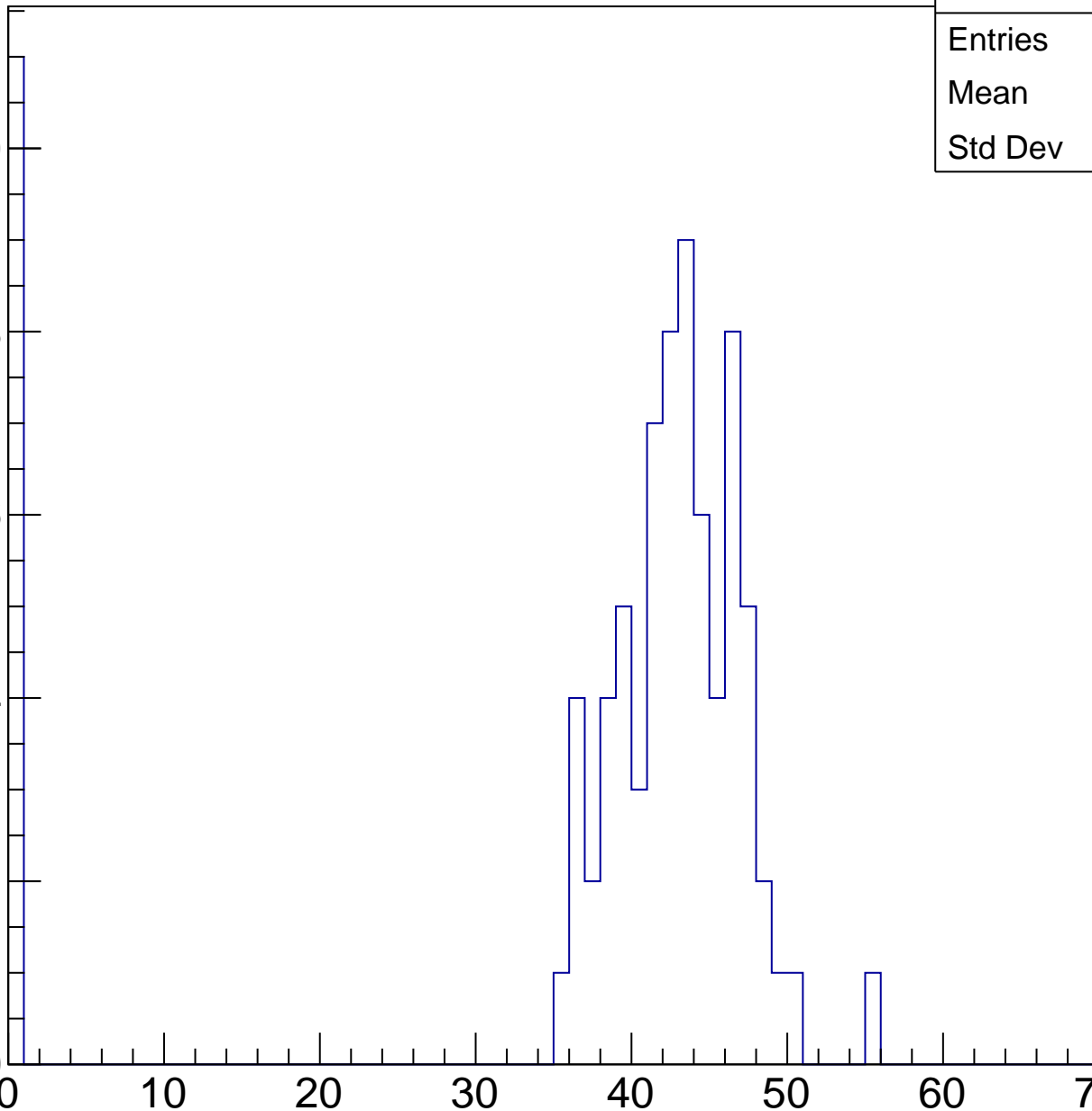
30

40

50

60

ampl

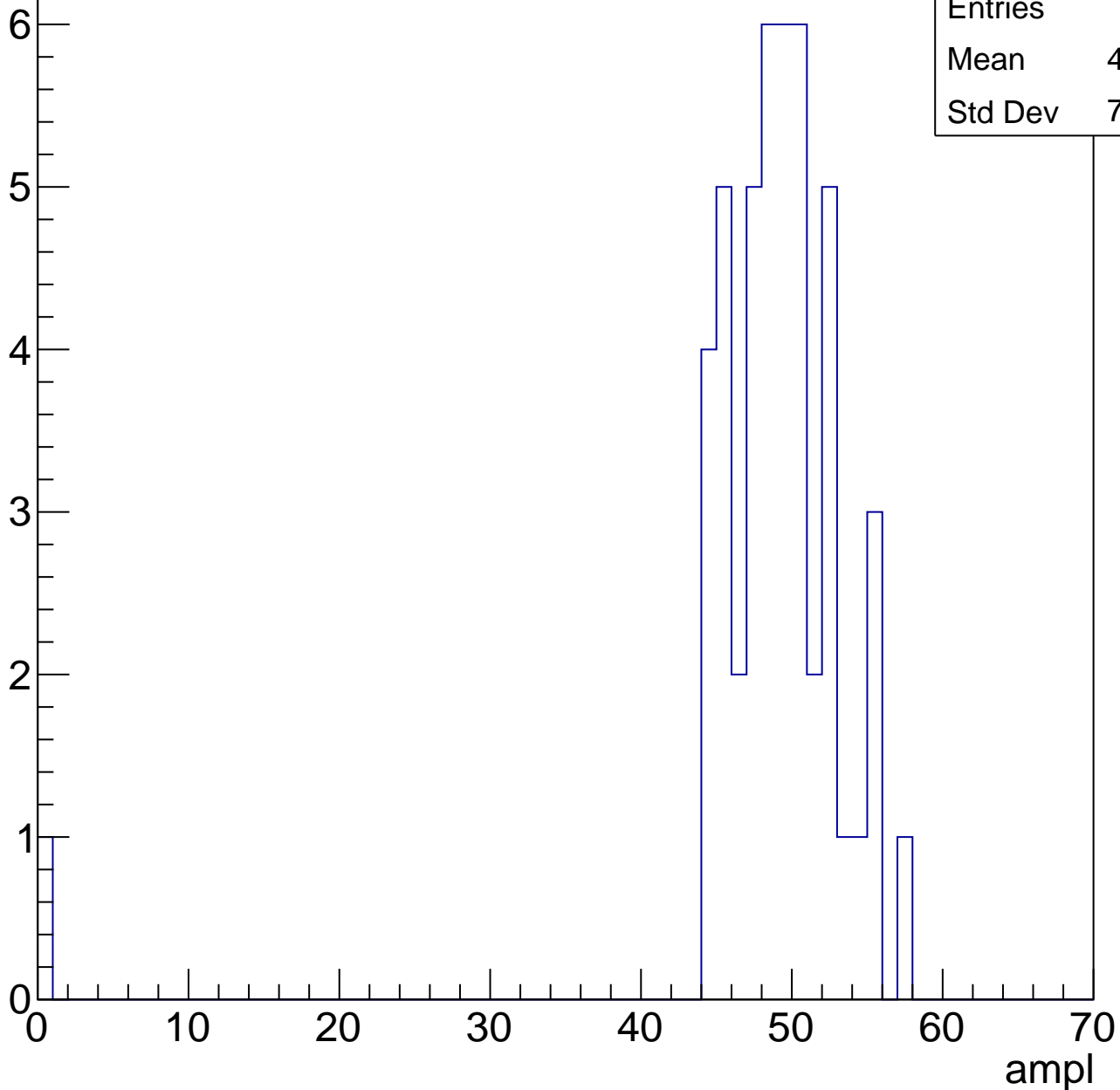


# B1L103S, U4-ch7, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

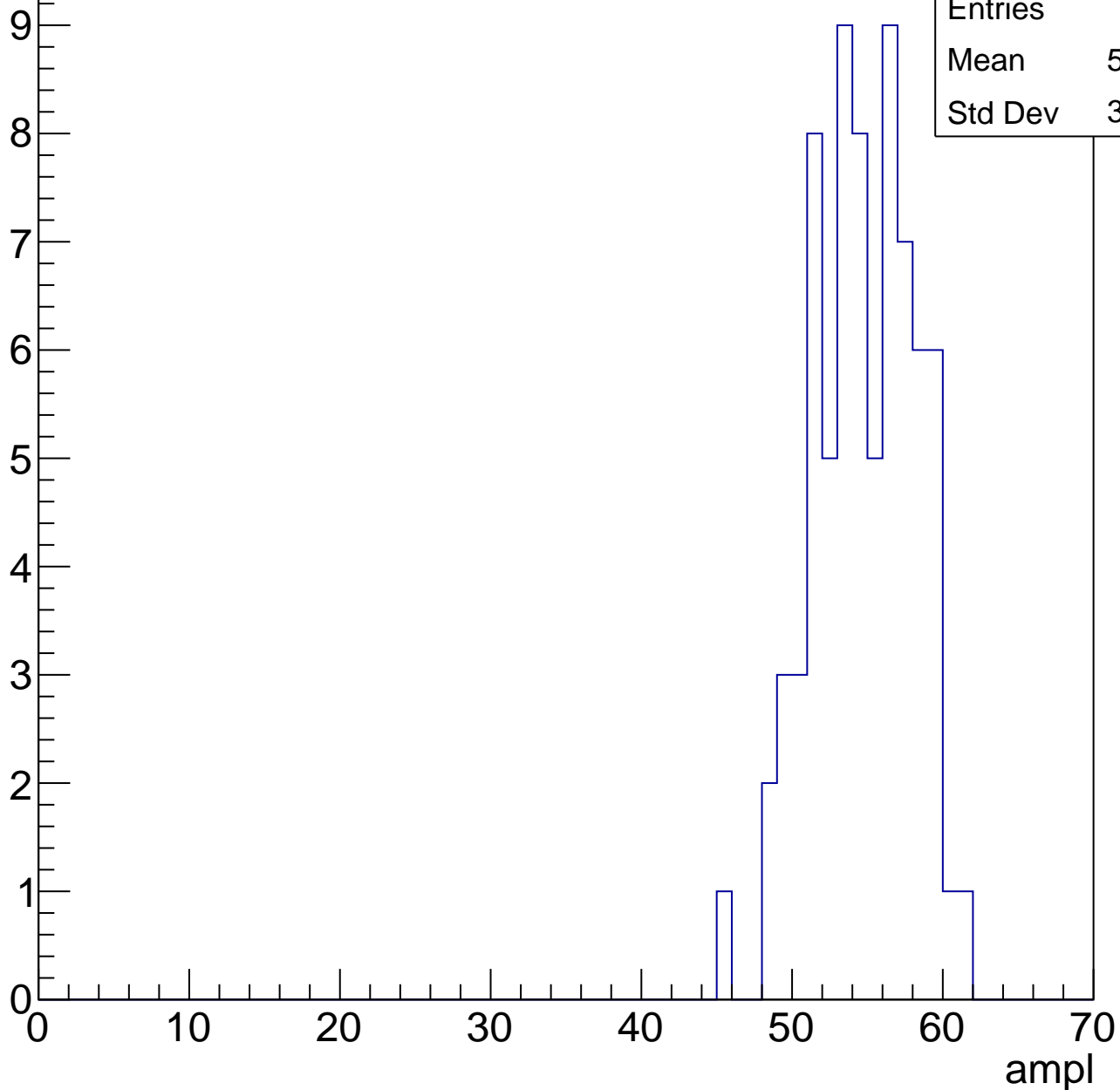
|         |       |
|---------|-------|
| Entries | 48    |
| Mean    | 47.94 |
| Std Dev | 7.696 |



# B1L103S, U4-ch7, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

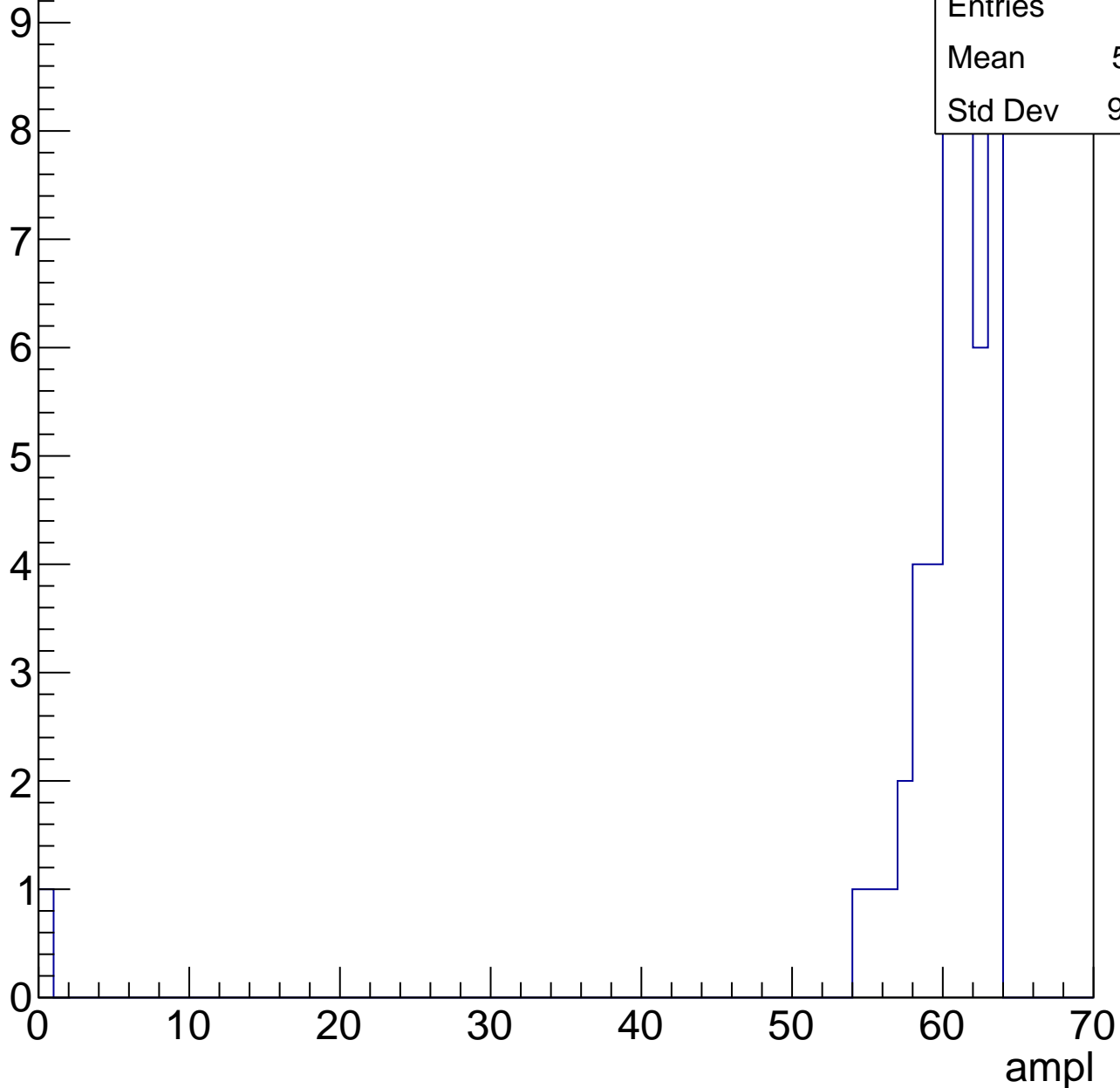


|         |       |
|---------|-------|
| Entries | 74    |
| Mean    | 54.27 |
| Std Dev | 3.302 |

# B1L103S, U4-ch7, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U4-ch7, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



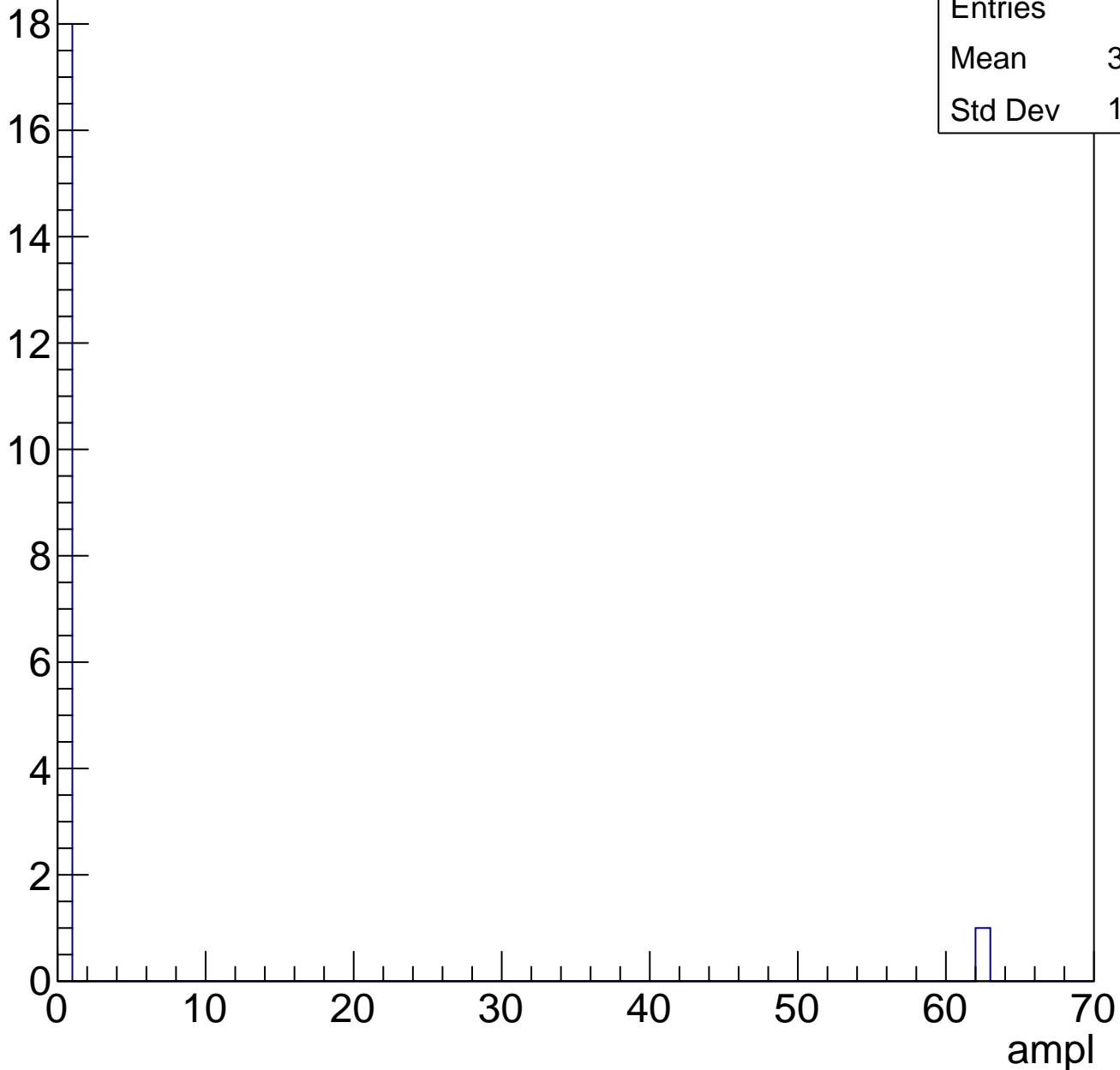


# B1L103S, U4-ch7, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 19    |
| Mean    | 3.263 |
| Std Dev | 13.84 |

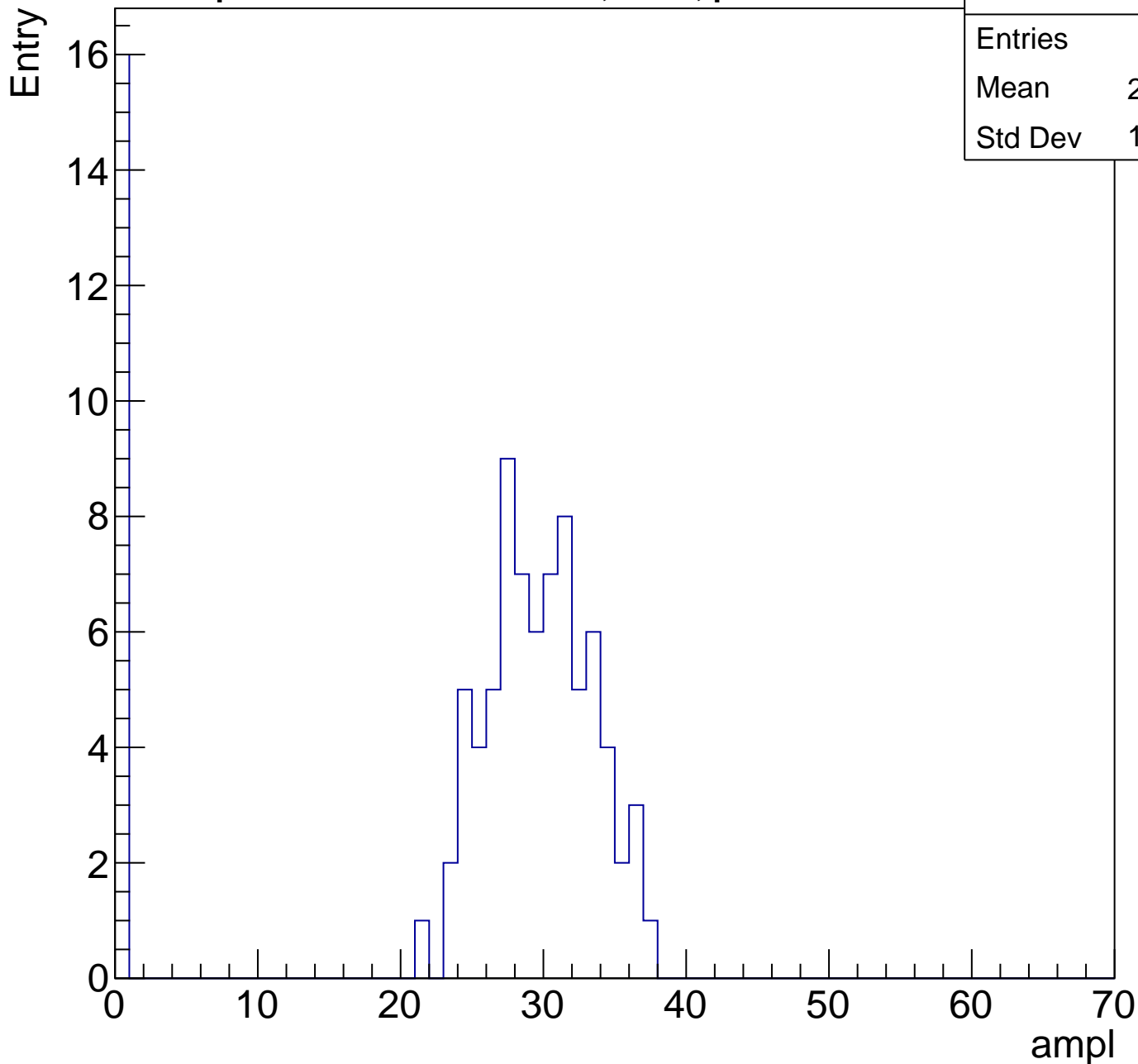
Entry



# B1L103S, U4-ch8, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 91    |
| Mean    | 24.14 |
| Std Dev | 11.62 |

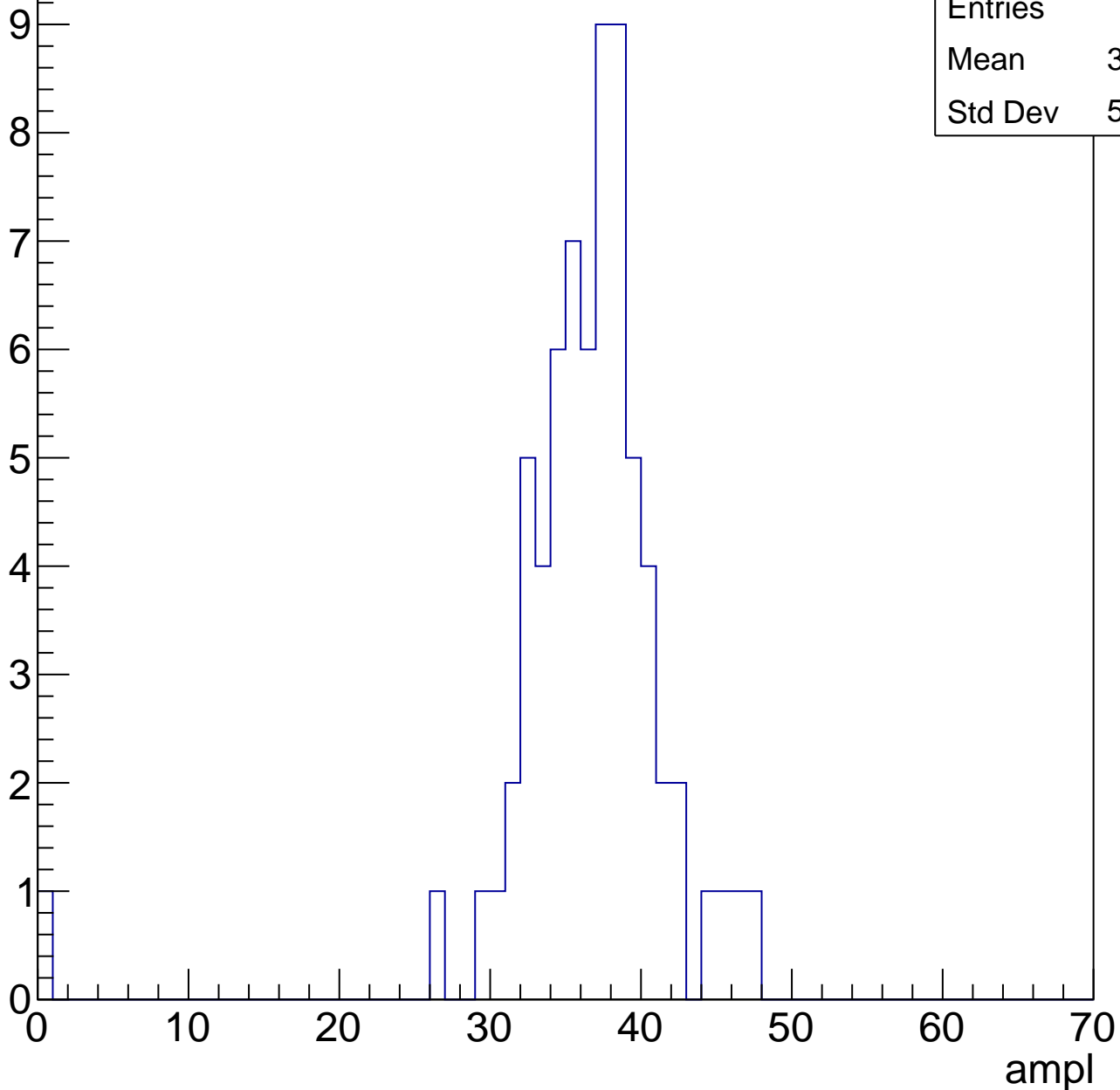


# B1L103S, U4-ch8, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 69    |
| Mean    | 35.97 |
| Std Dev | 5.798 |

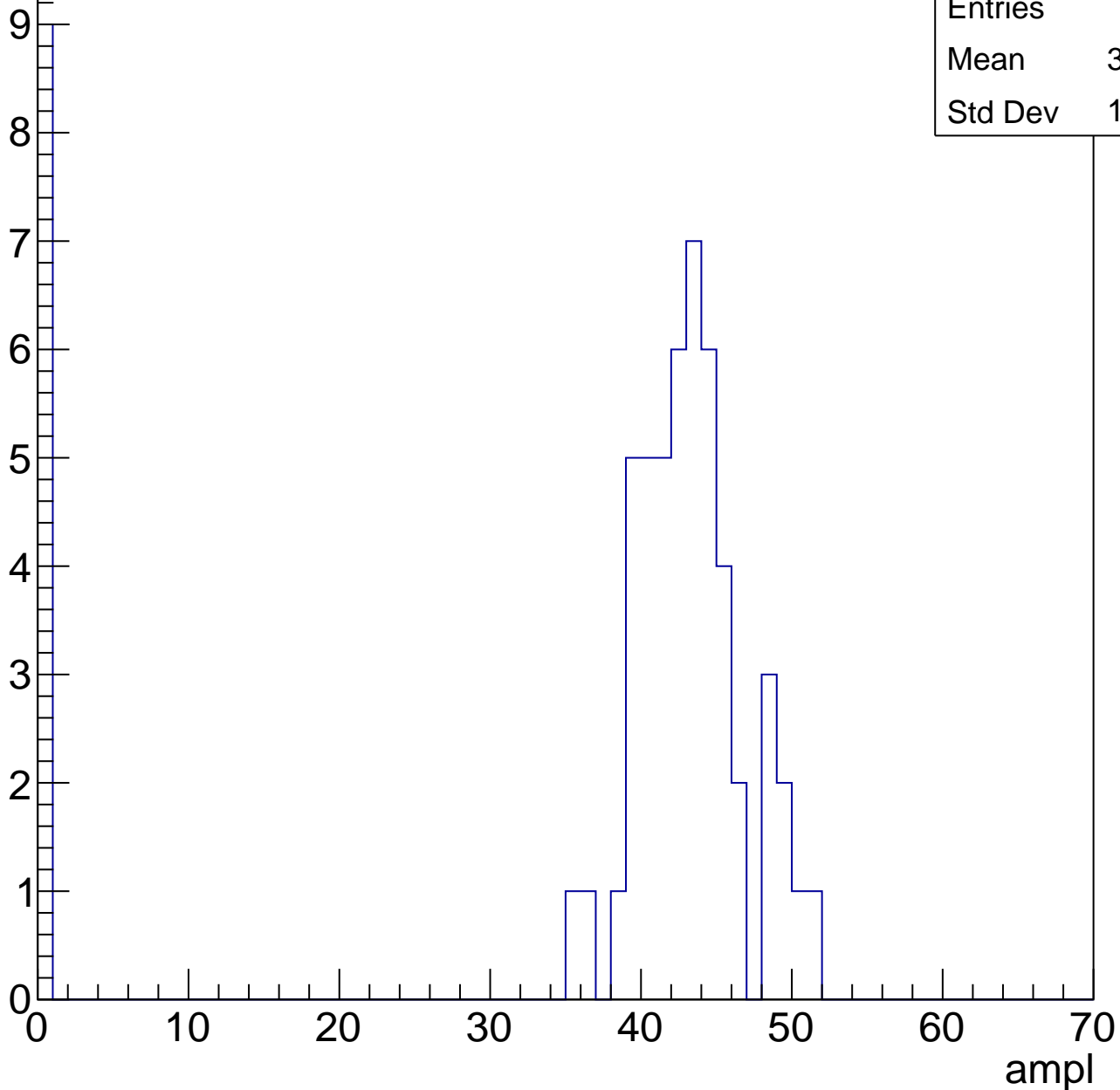


# B1L103S, U4-ch8, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 59    |
| Mean    | 36.29 |
| Std Dev | 15.72 |

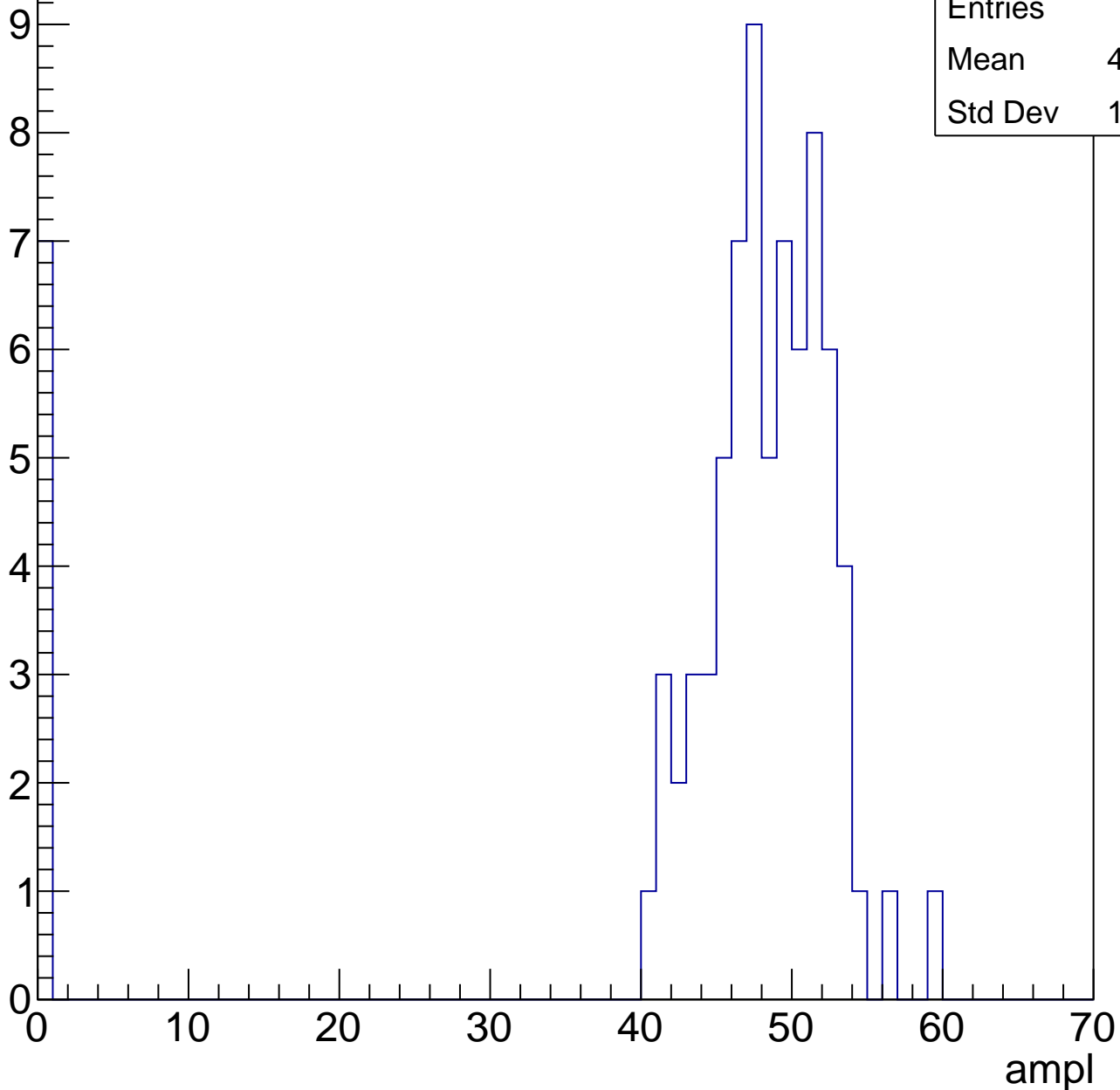


# B1L103S, U4-ch8, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 79    |
| Mean    | 43.82 |
| Std Dev | 14.12 |

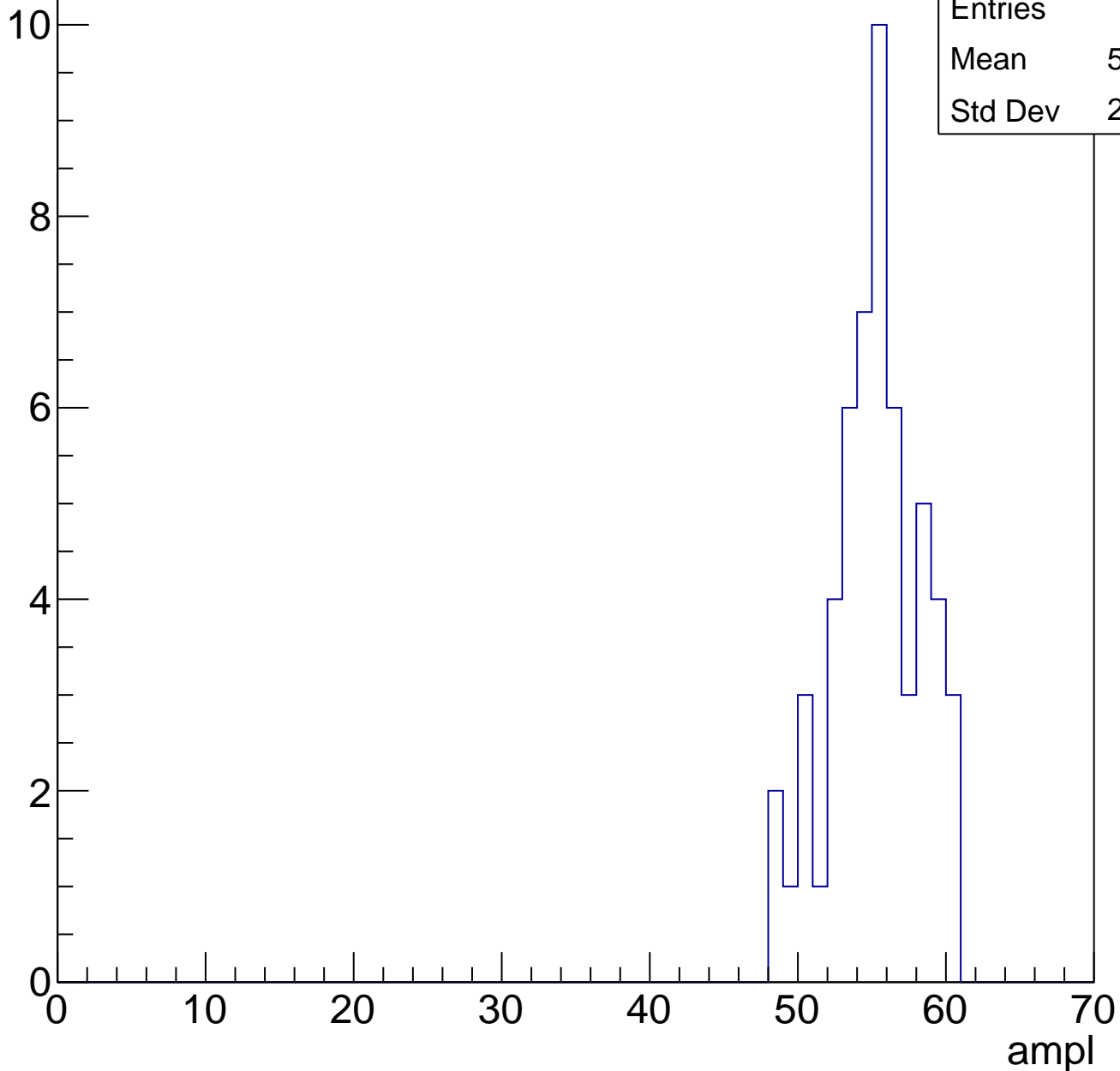


# B1L103S, U4-ch8, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 55    |
| Mean    | 54.78 |
| Std Dev | 2.989 |

Entry

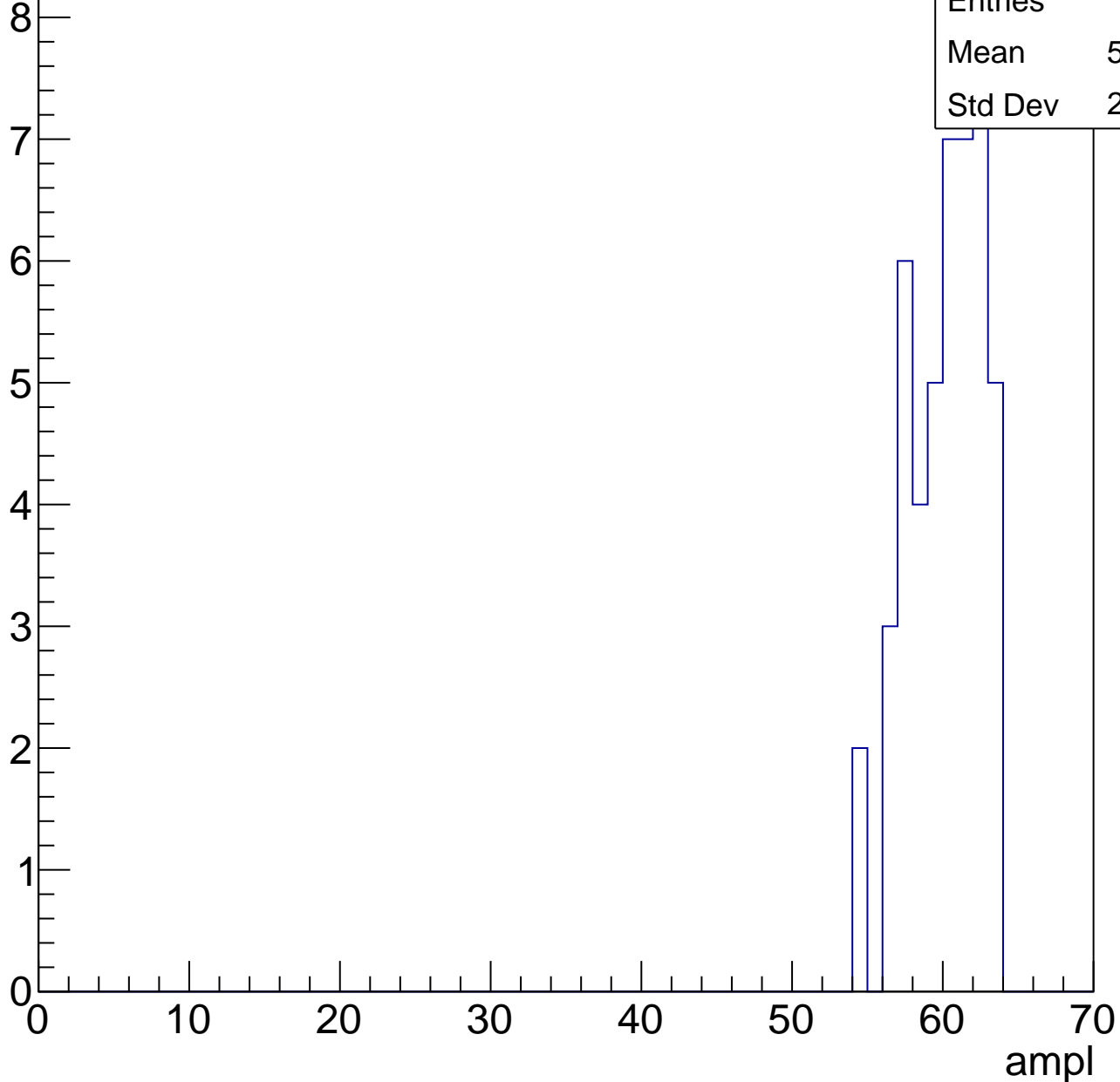


# B1L103S, U4-ch8, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 47    |
| Mean    | 59.64 |
| Std Dev | 2.409 |







# B1L103S, U4-ch8, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

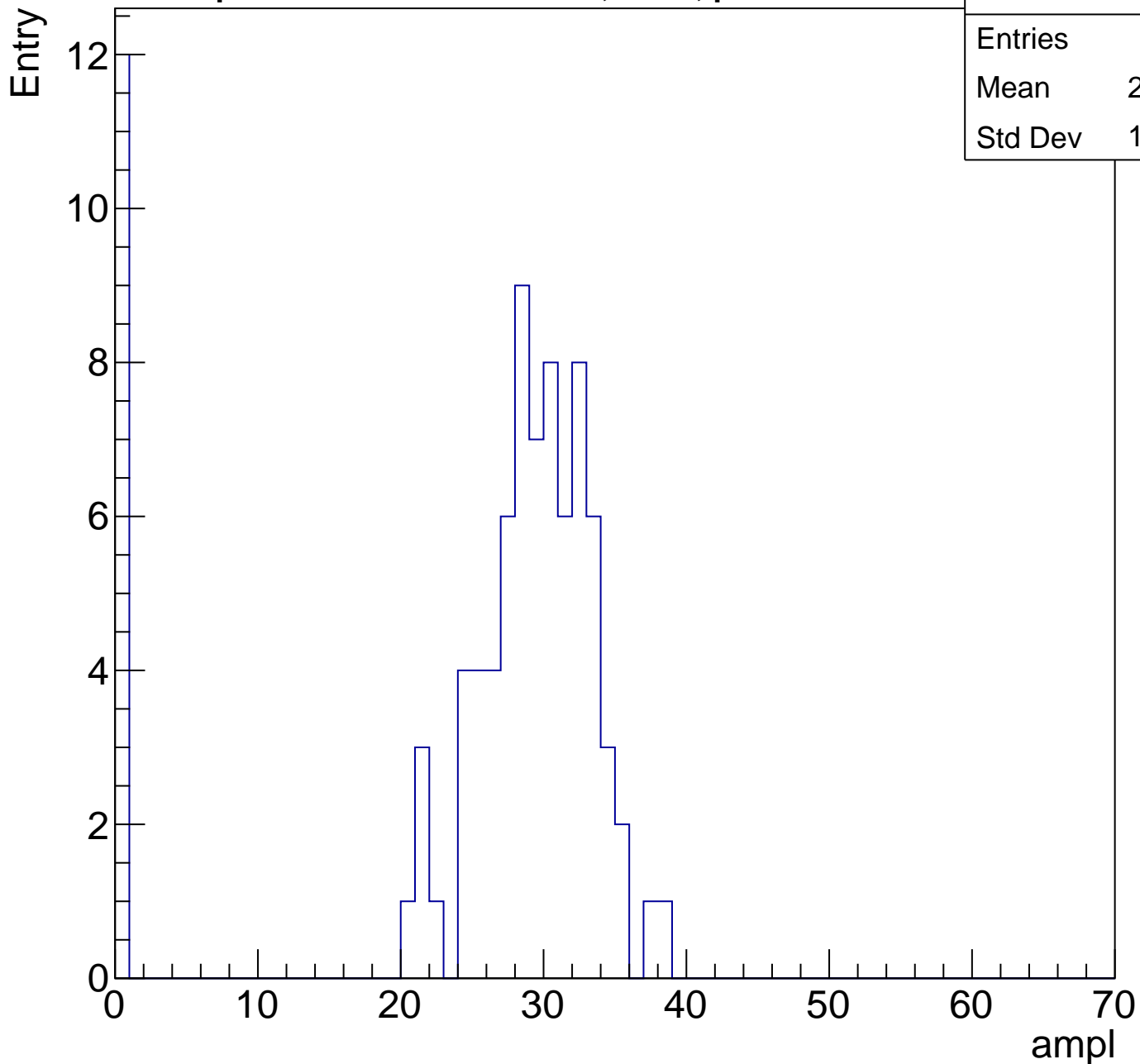
|         |    |
|---------|----|
| Entries | 19 |
| Mean    | 0  |
| Std Dev | 0  |



# B1L103S, U4-ch9, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 86    |
| Mean    | 24.99 |
| Std Dev | 10.65 |



# B1L103S, U4-ch9, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

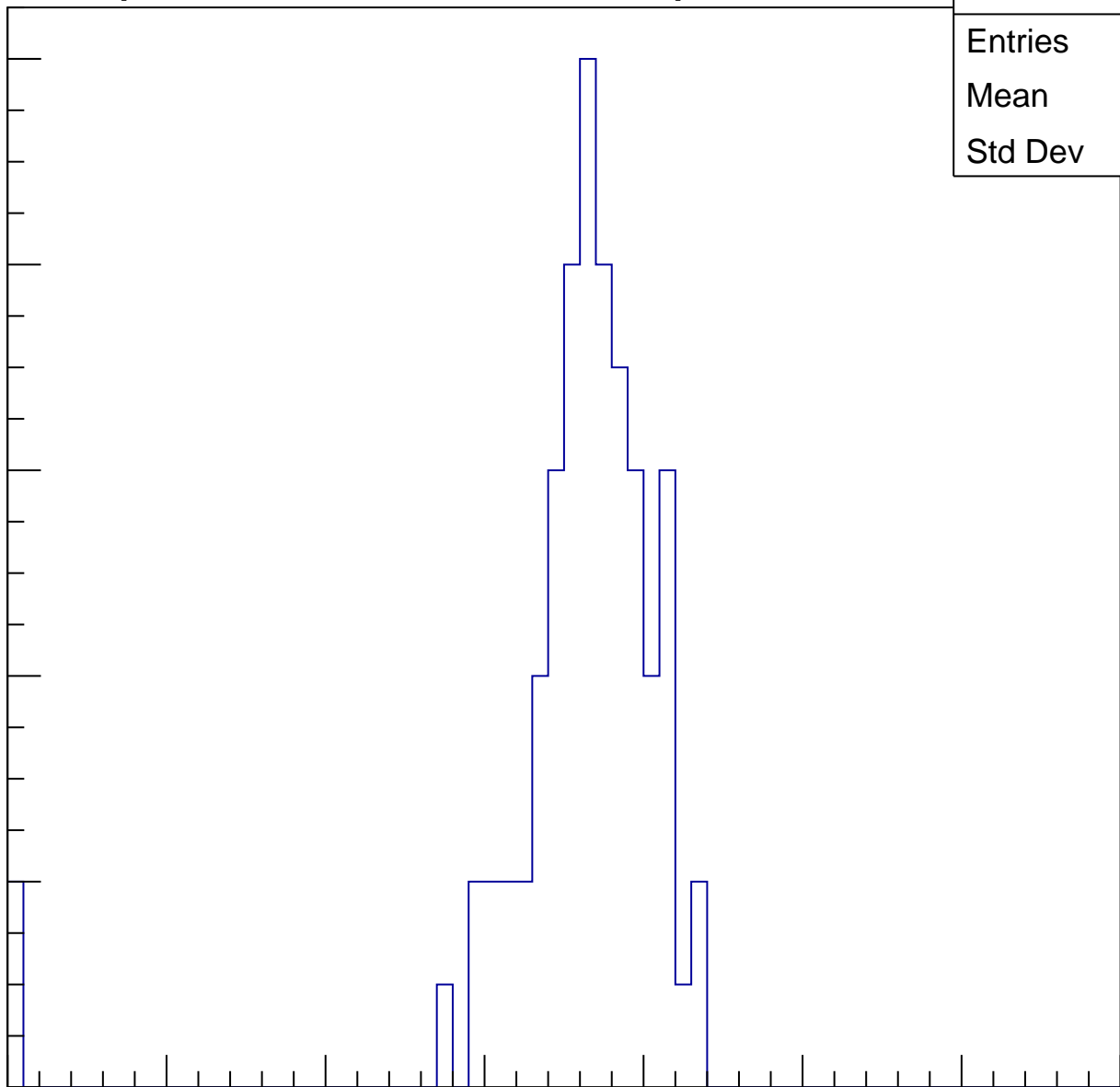
|         |      |
|---------|------|
| Entries | 73   |
| Mean    | 35.3 |
| Std Dev | 6.82 |

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

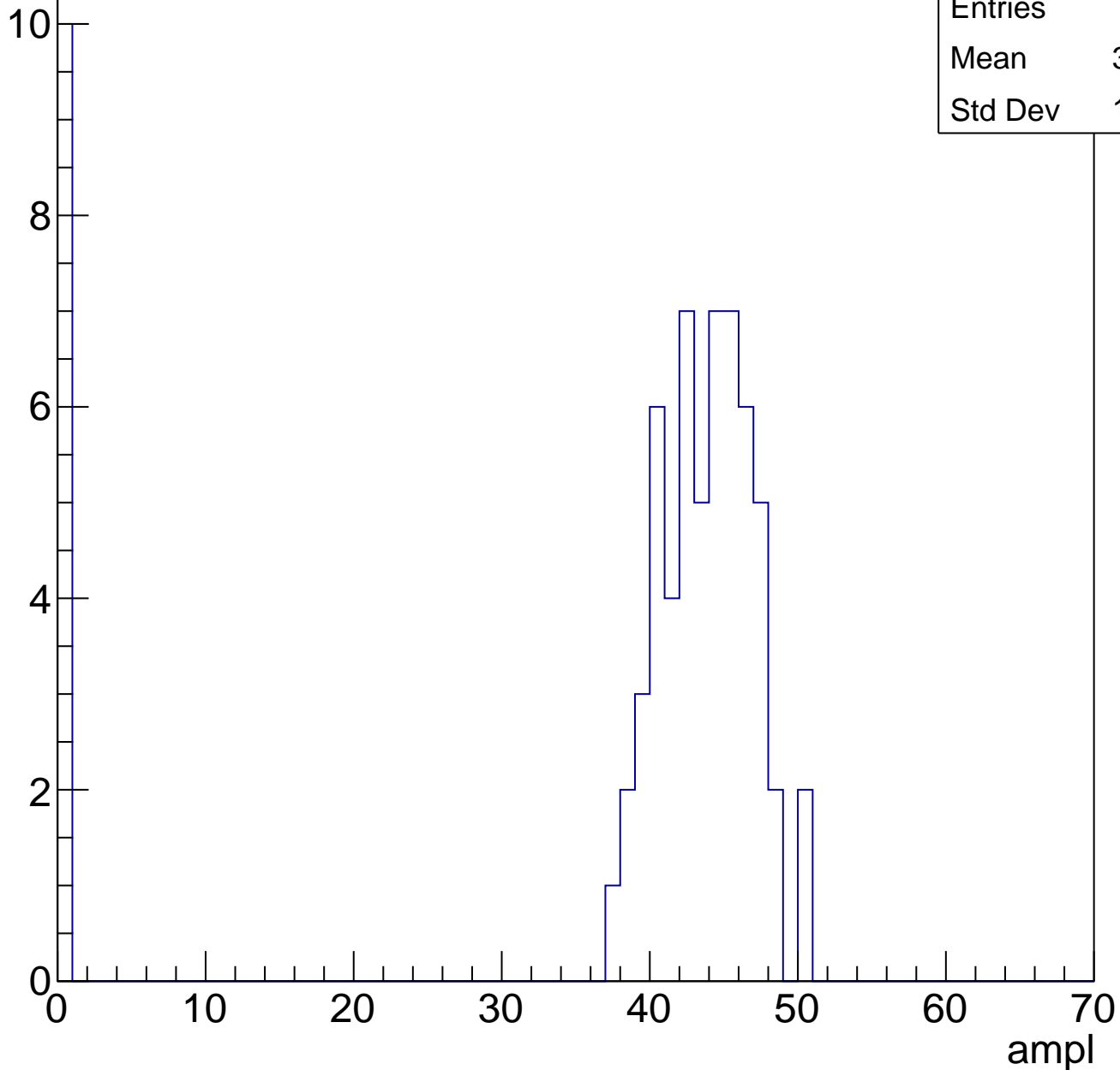


# B1L103S, U4-ch9, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 67    |
| Mean    | 36.91 |
| Std Dev | 15.71 |

Entry

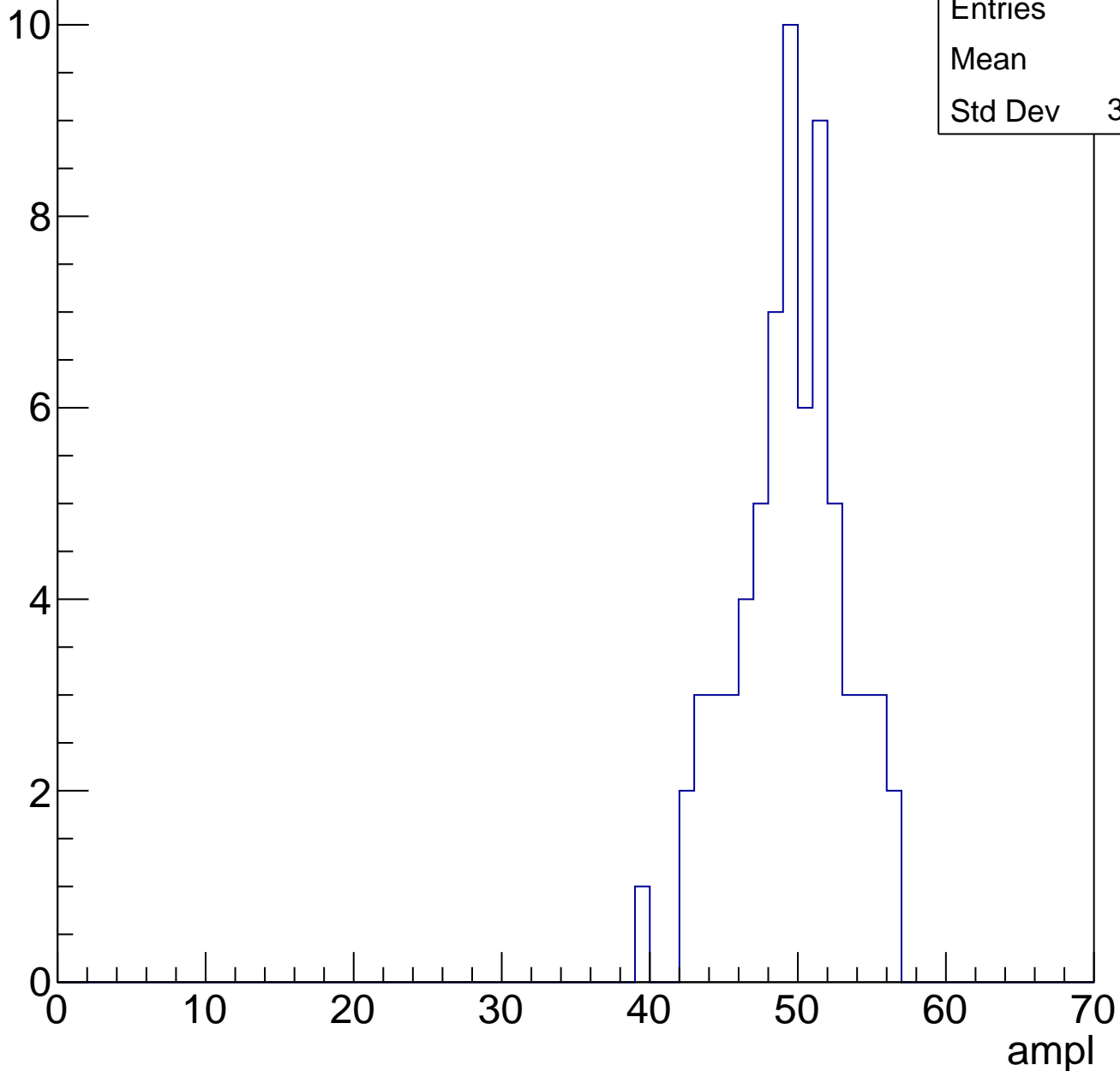


# B1L103S, U4-ch9, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 69    |
| Mean    | 49    |
| Std Dev | 3.628 |

Entry



# B1L103S, U4-ch9, adc4

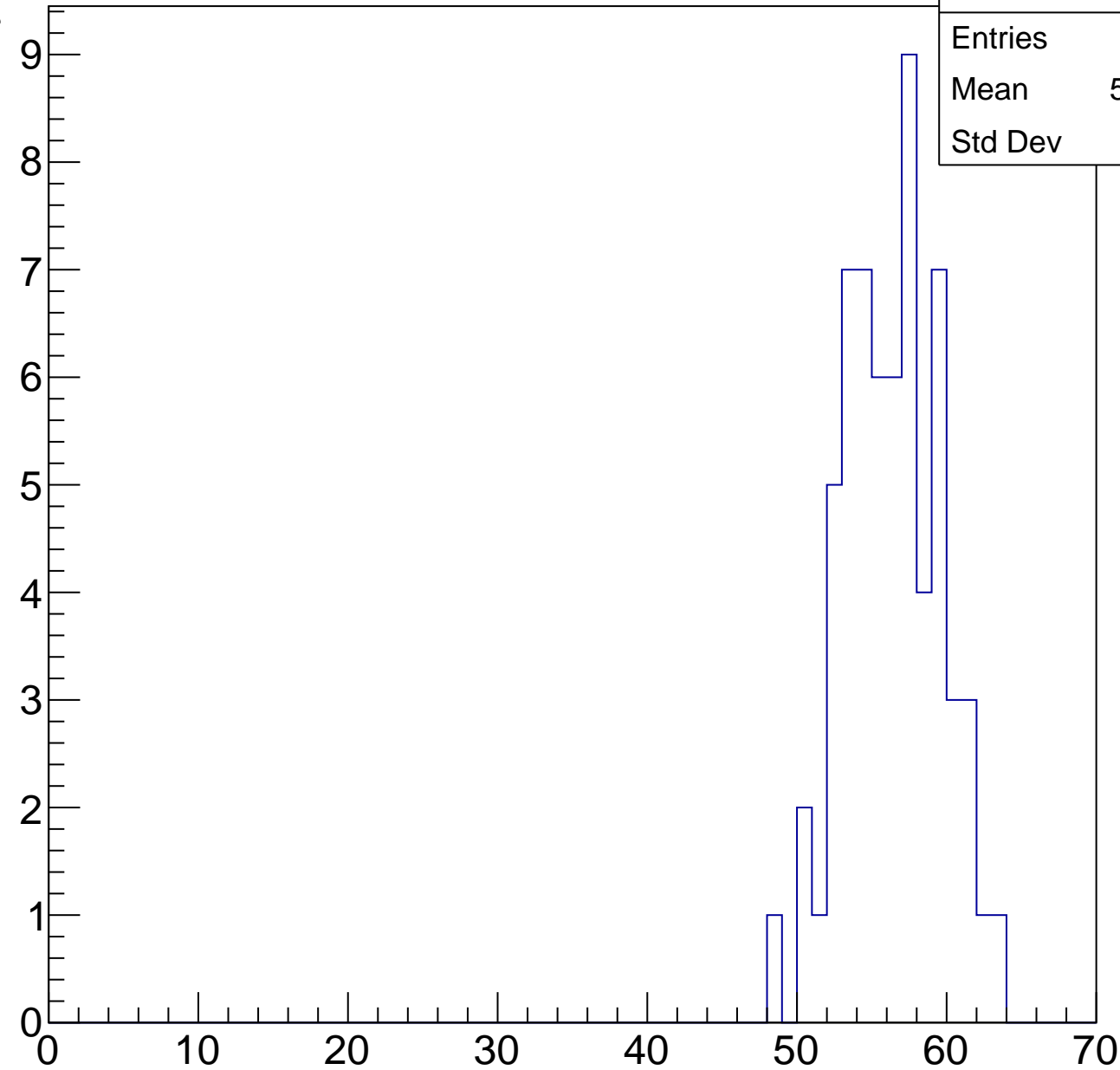
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

|         |       |
|---------|-------|
| Entries | 63    |
| Mean    | 55.87 |
| Std Dev | 3.17  |

ampl

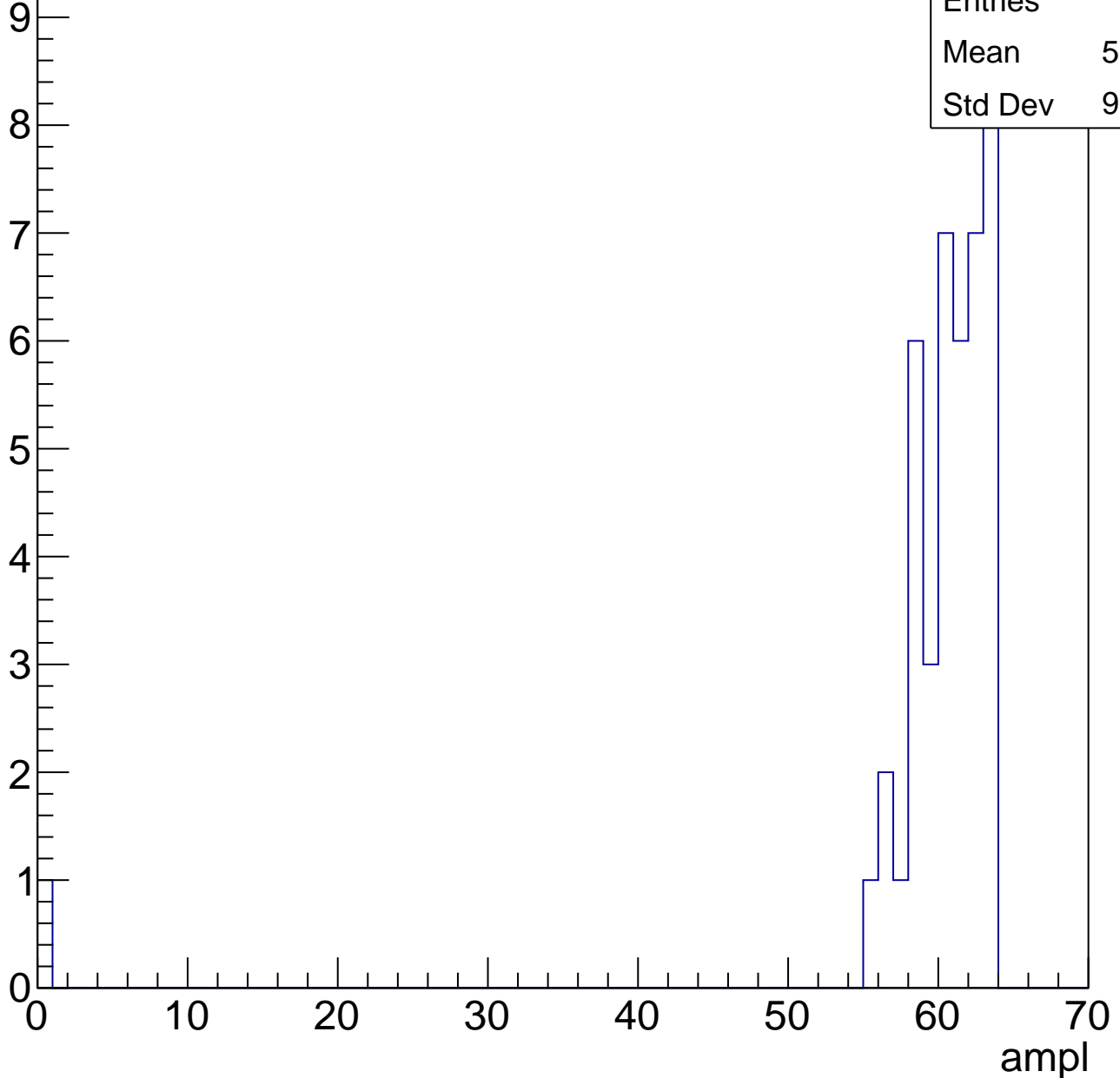


# B1L103S, U4-ch9, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 43    |
| Mean    | 58.98 |
| Std Dev | 9.355 |



# B1L103S, U4-ch9, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

|         |        |
|---------|--------|
| Entries | 3      |
| Mean    | 61.67  |
| Std Dev | 0.4714 |

ampl

0 10 20 30 40 50 60 70



# B1L103S, U4-ch9, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |    |
|---------|----|
| Entries | 19 |
| Mean    | 0  |
| Std Dev | 0  |



# B1L103S, U4-ch10, adc0

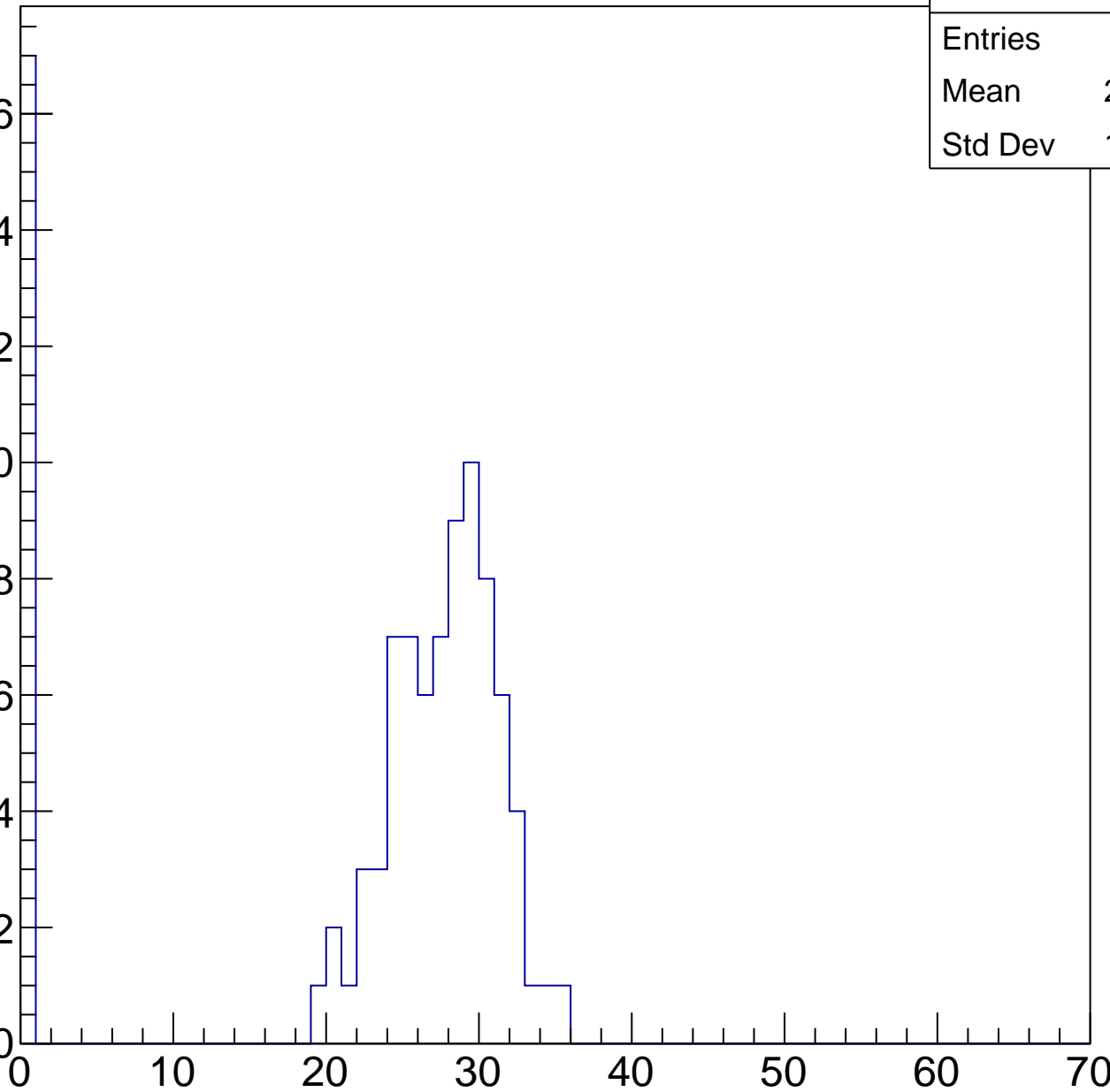
calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 94    |
| Mean    | 22.35 |
| Std Dev | 10.94 |

Entry

16  
14  
12  
10  
8  
6  
4  
2  
0

ampl

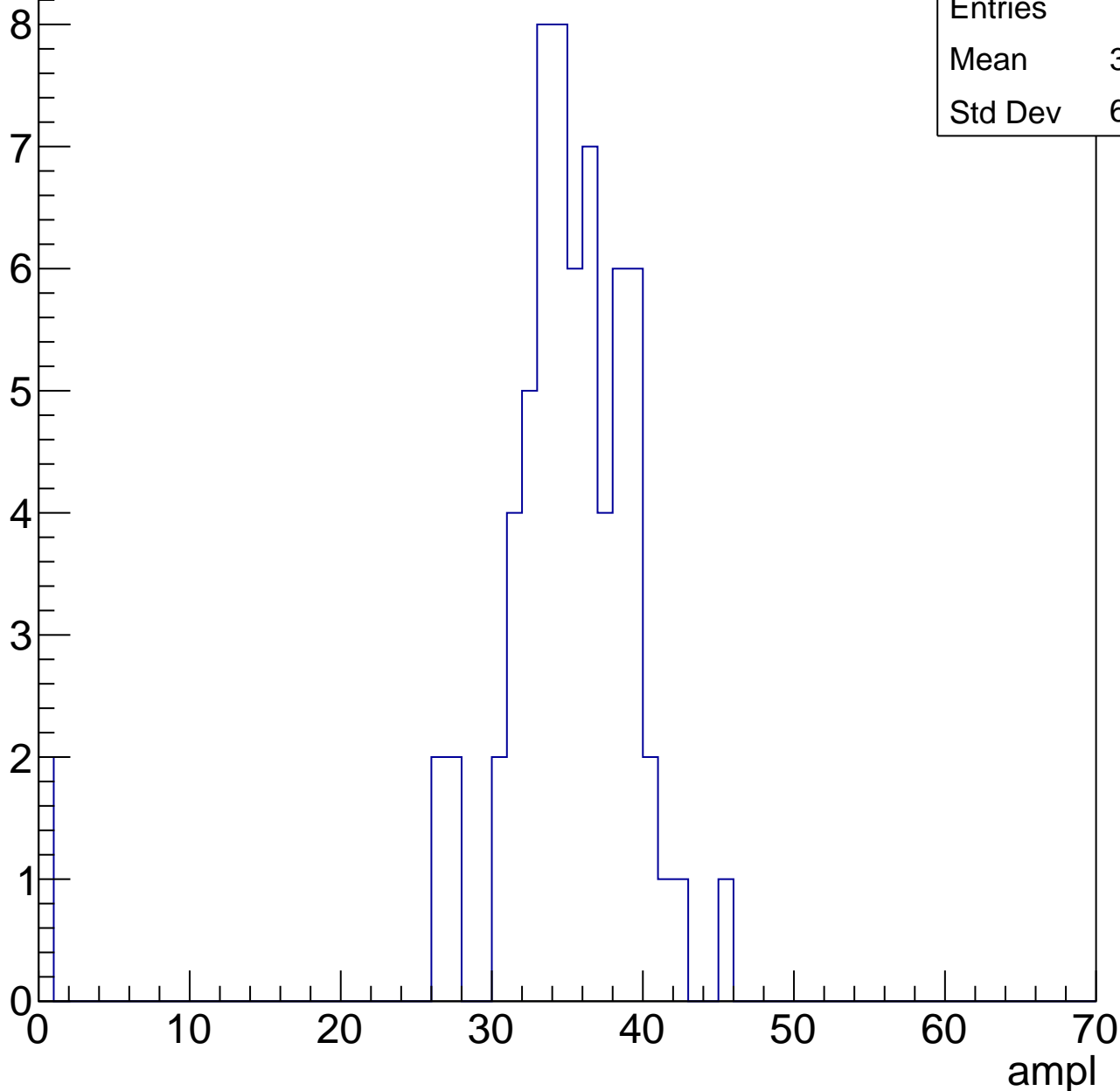


# B1L103S, U4-ch10, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 67    |
| Mean    | 33.82 |
| Std Dev | 6.969 |

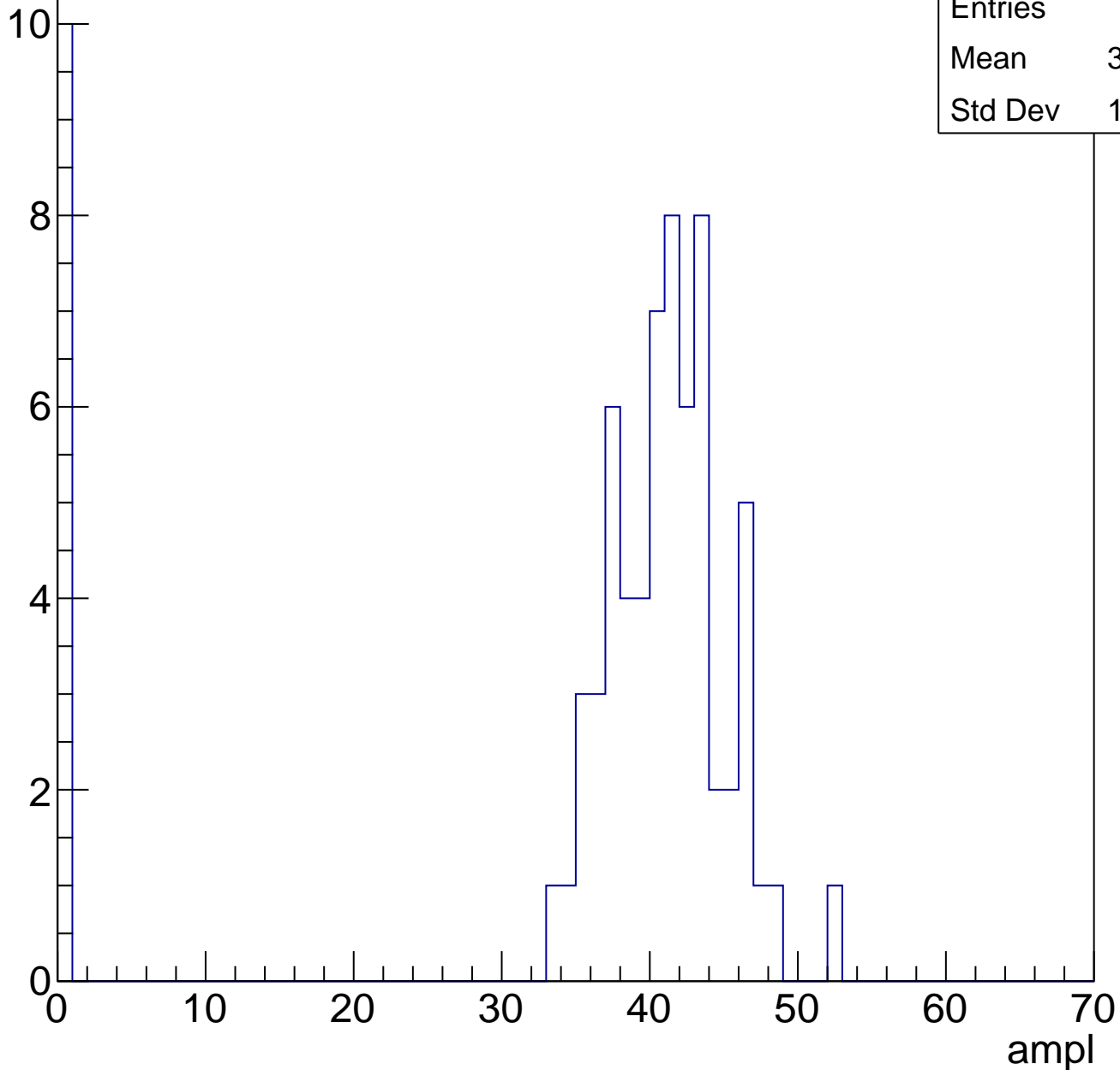


# B1L103S, U4-ch10, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 73    |
| Mean    | 35.19 |
| Std Dev | 14.44 |

Entry

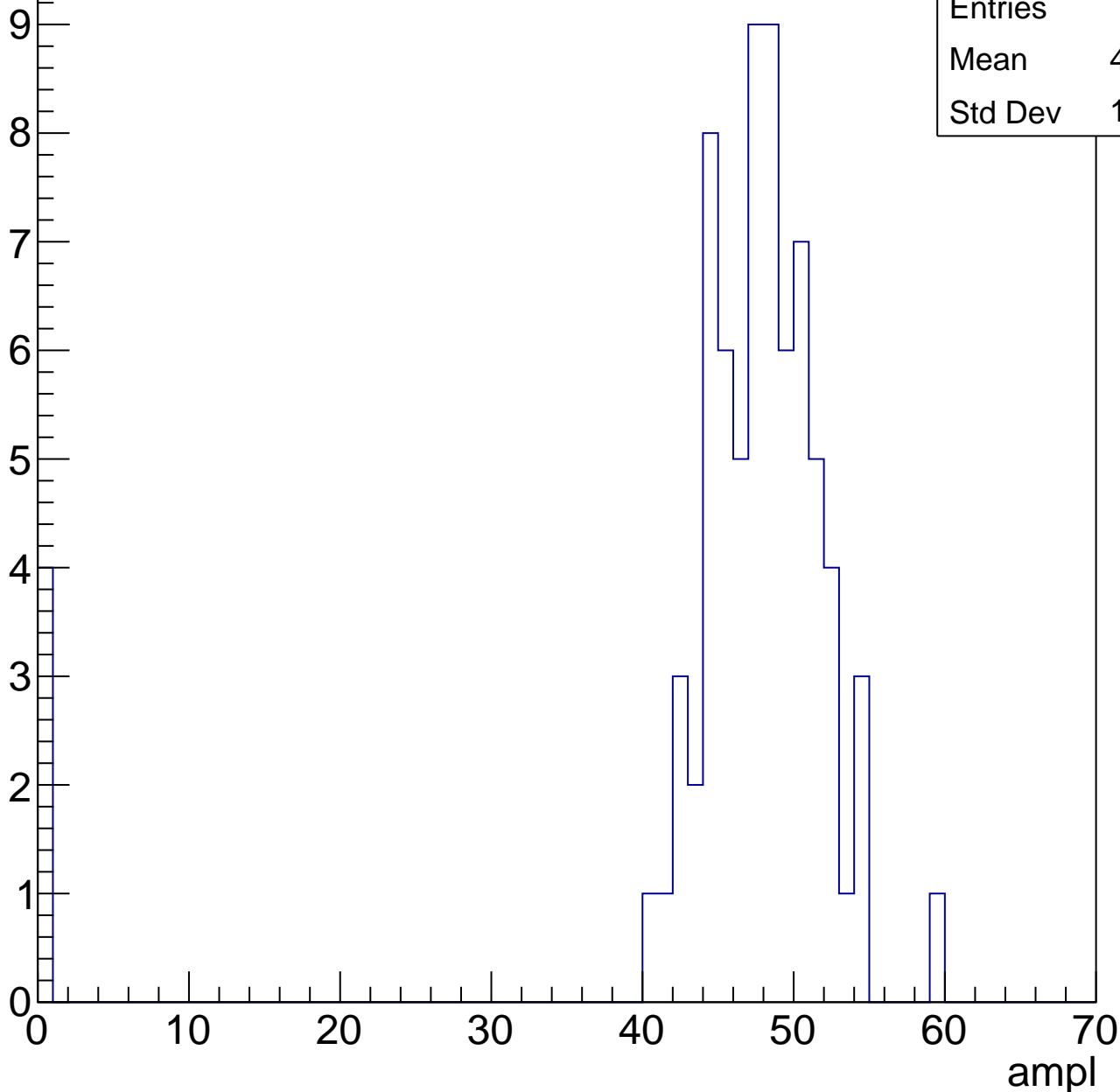


# B1L103S, U4-ch10, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 75    |
| Mean    | 45.08 |
| Std Dev | 11.23 |

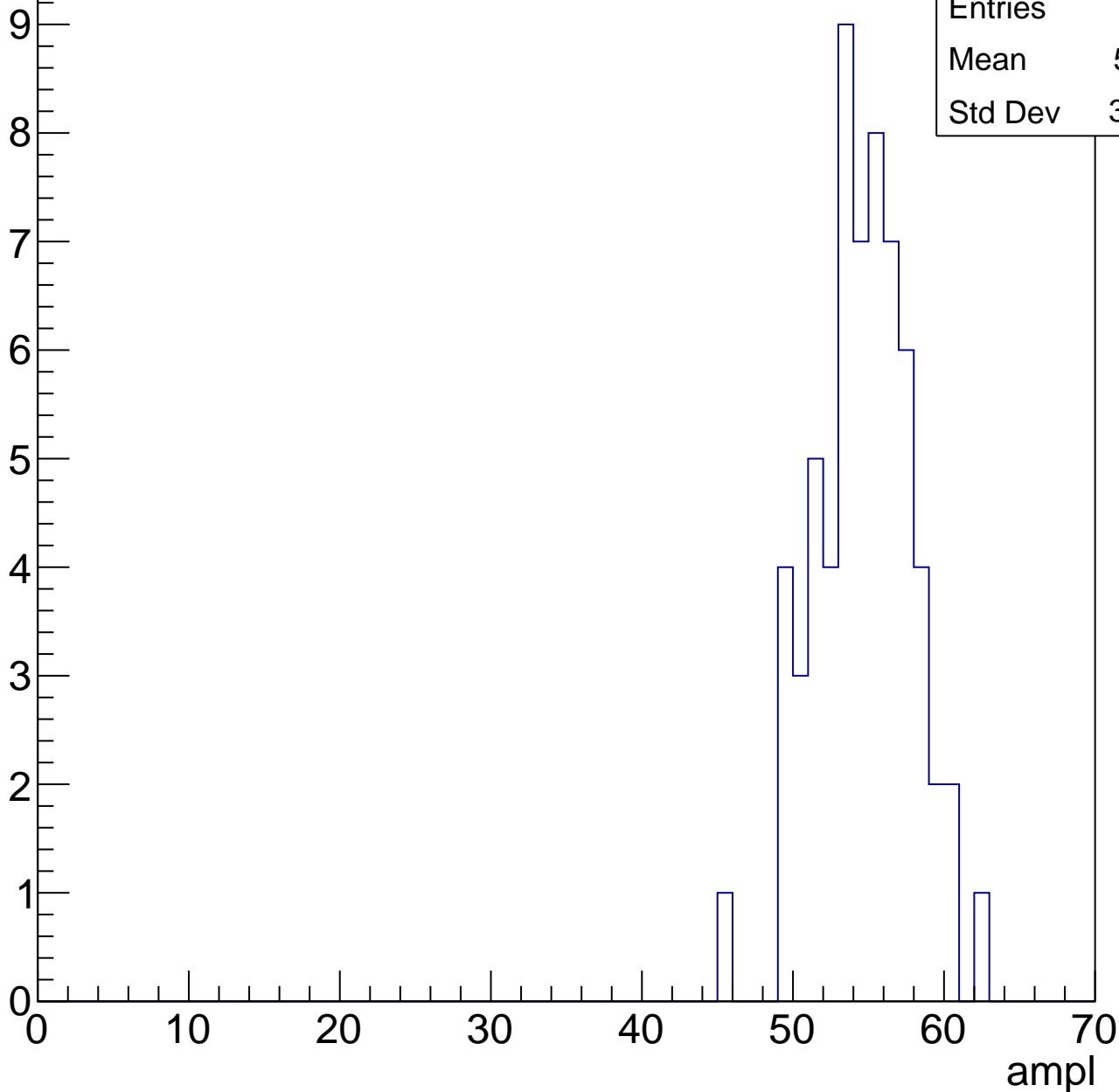


# B1L103S, U4-ch10, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 63    |
| Mean    | 54.21 |
| Std Dev | 3.178 |

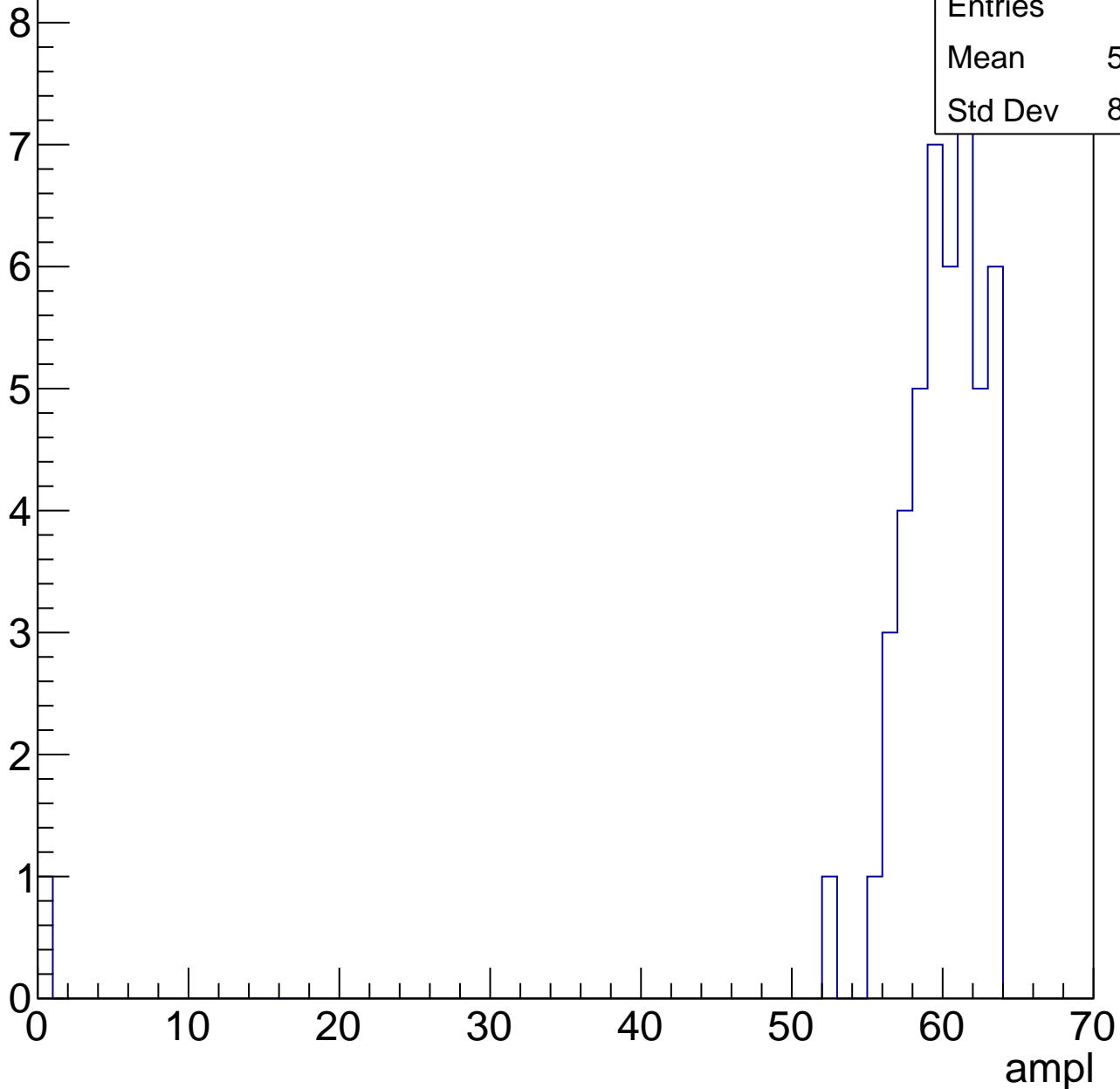


# B1L103S, U4-ch10, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 47    |
| Mean    | 58.34 |
| Std Dev | 8.935 |



# B1L103S, U4-ch10, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

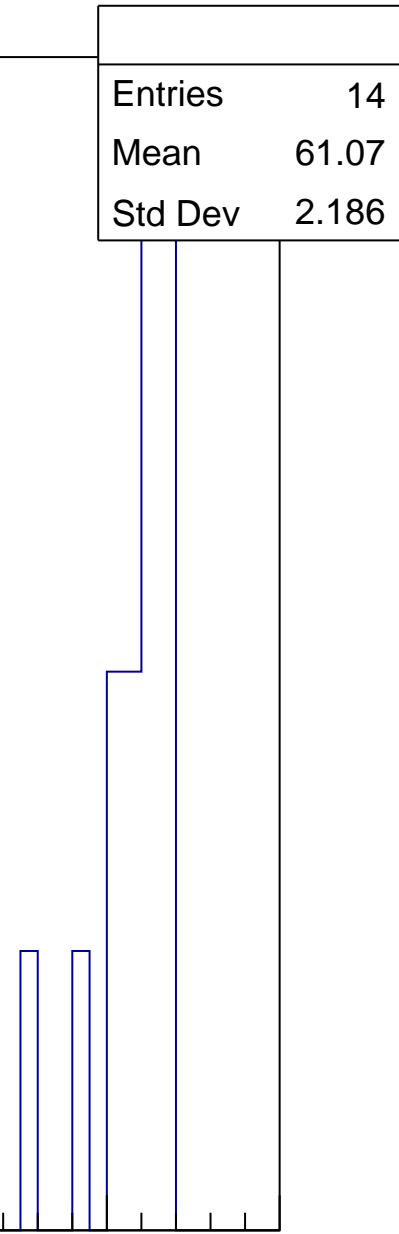
Entry

4  
3.5  
3  
2.5  
2  
1.5  
1  
0.5  
0

|         |       |
|---------|-------|
| Entries | 14    |
| Mean    | 61.07 |
| Std Dev | 2.186 |

ampl

0 10 20 30 40 50 60 70

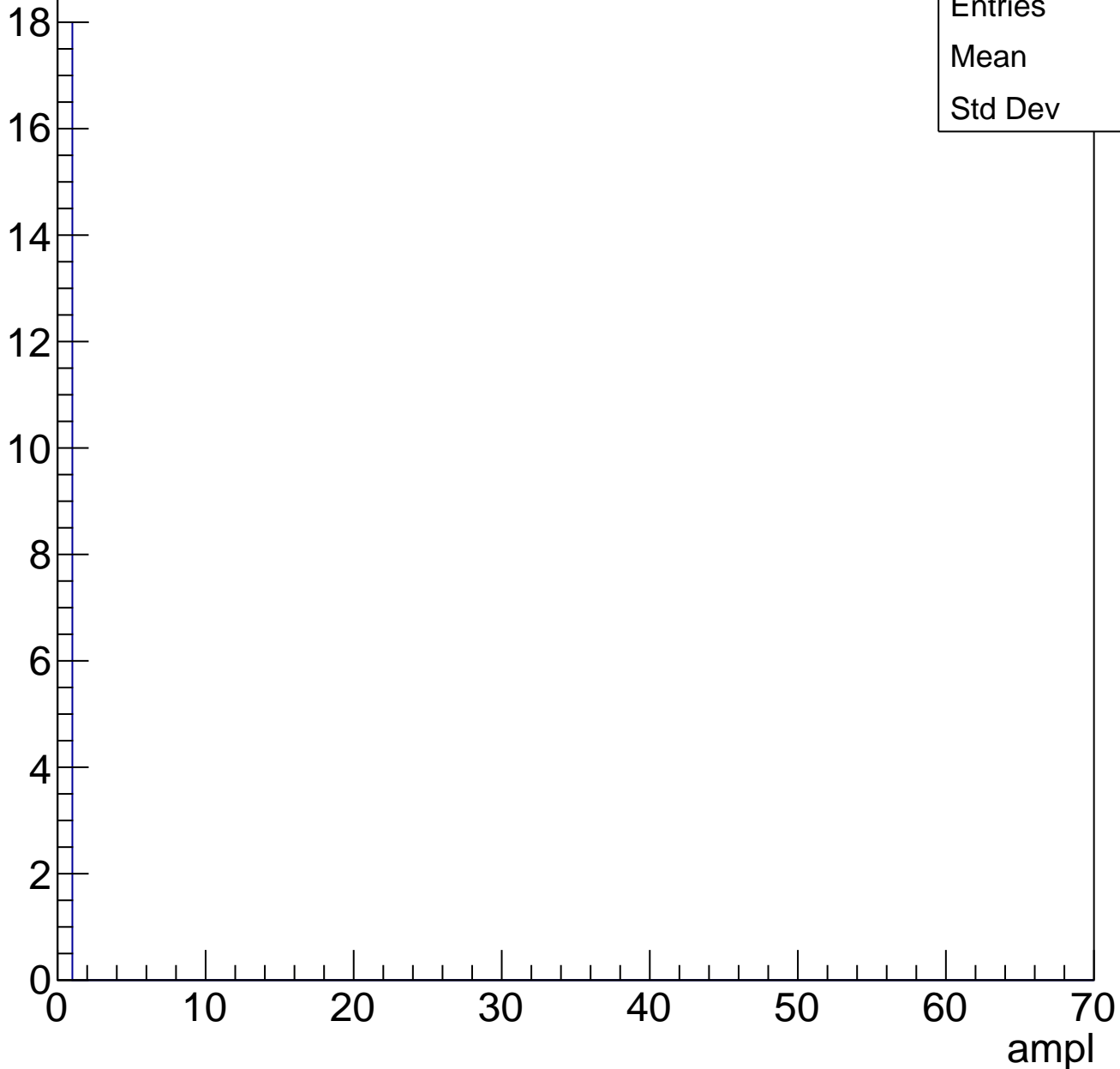




# B1L103S, U4-ch10, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

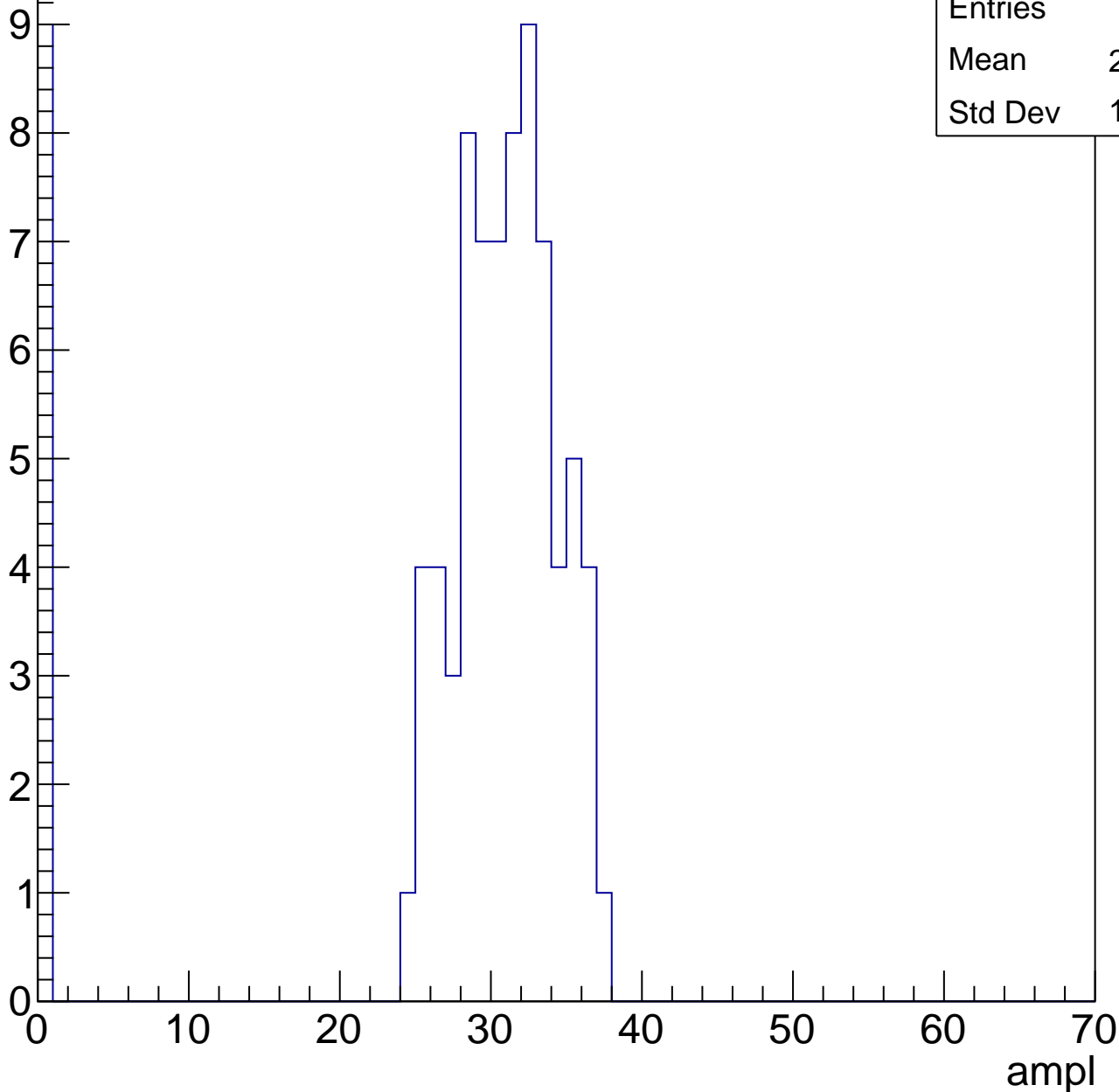


# B1L103S, U4-ch11, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 81    |
| Mean    | 27.22 |
| Std Dev | 10.08 |

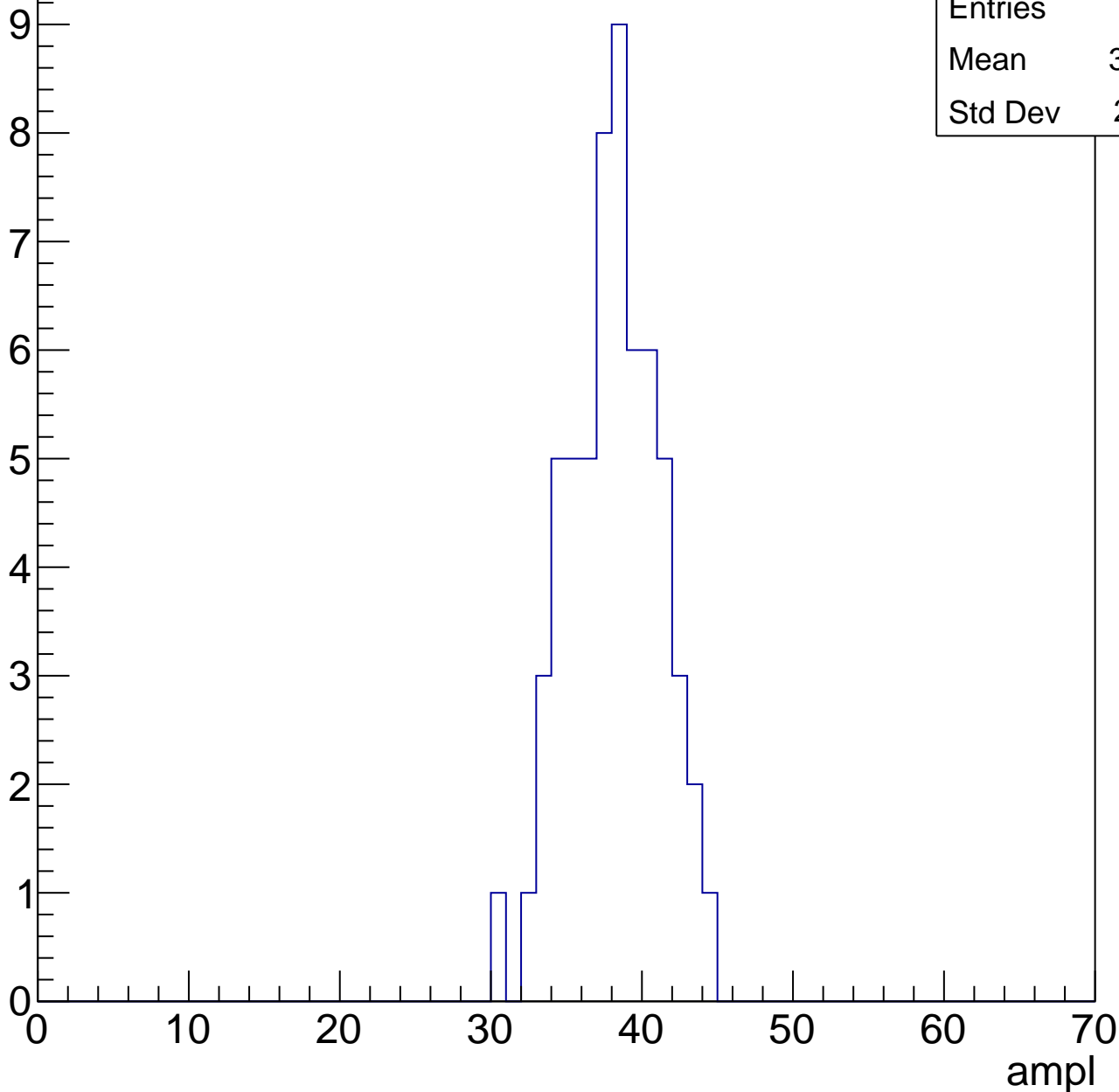


# B1L103S, U4-ch11, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 60    |
| Mean    | 37.65 |
| Std Dev | 2.971 |

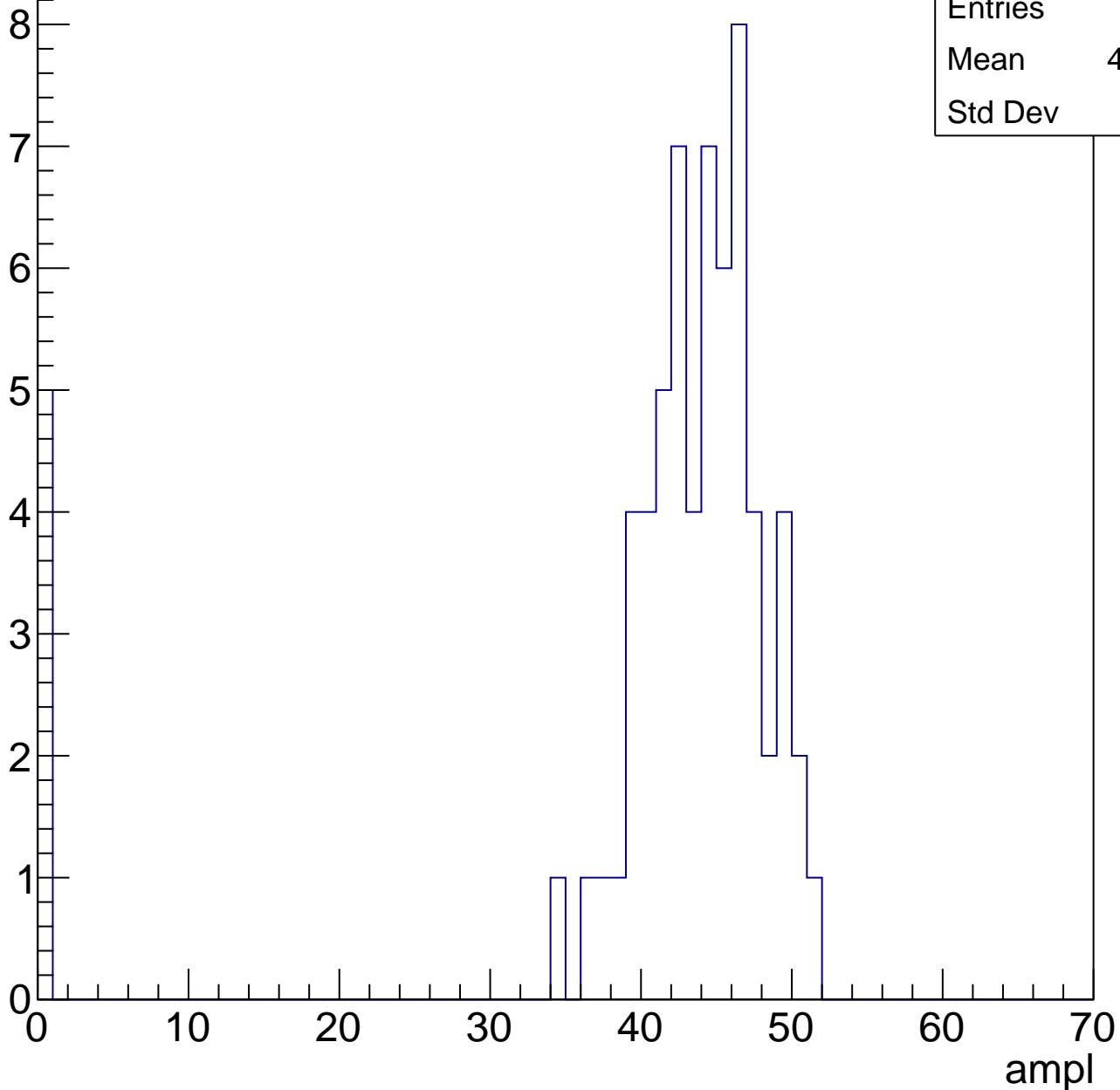


# B1L103S, U4-ch11, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

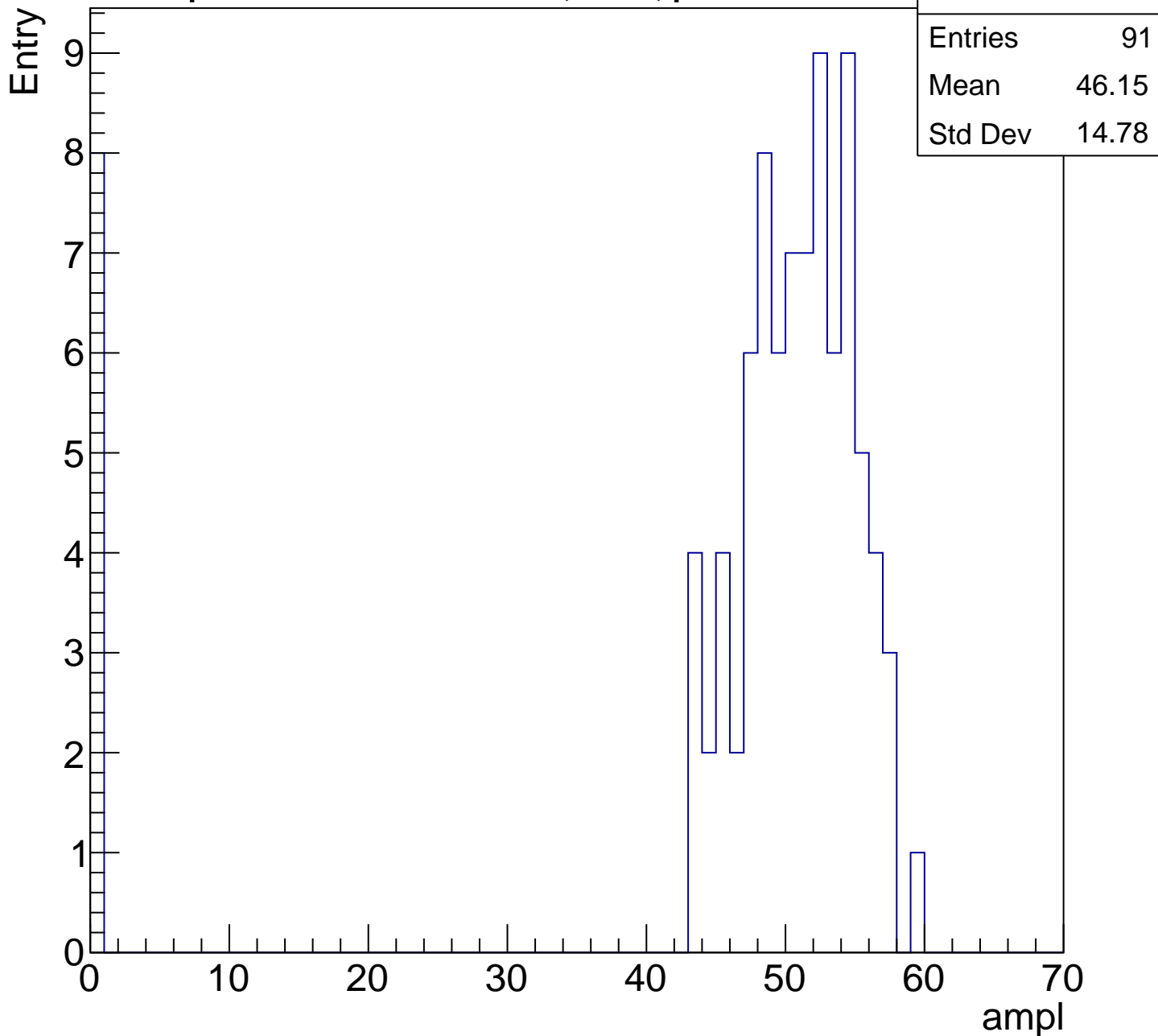
Entry

|         |       |
|---------|-------|
| Entries | 67    |
| Mean    | 40.43 |
| Std Dev | 12    |



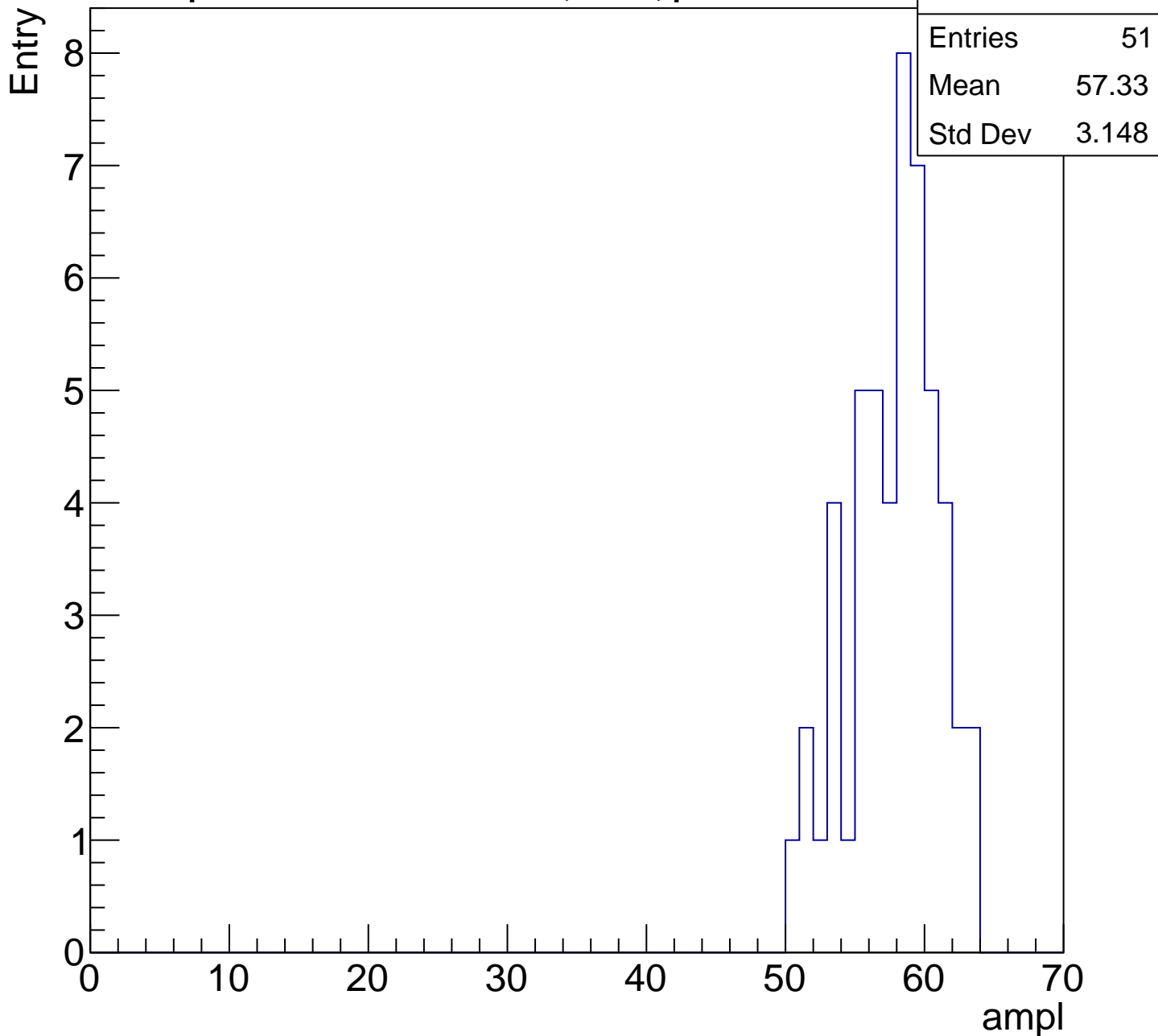
# B1L103S, U4-ch11, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2



# B1L103S, U4-ch11, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

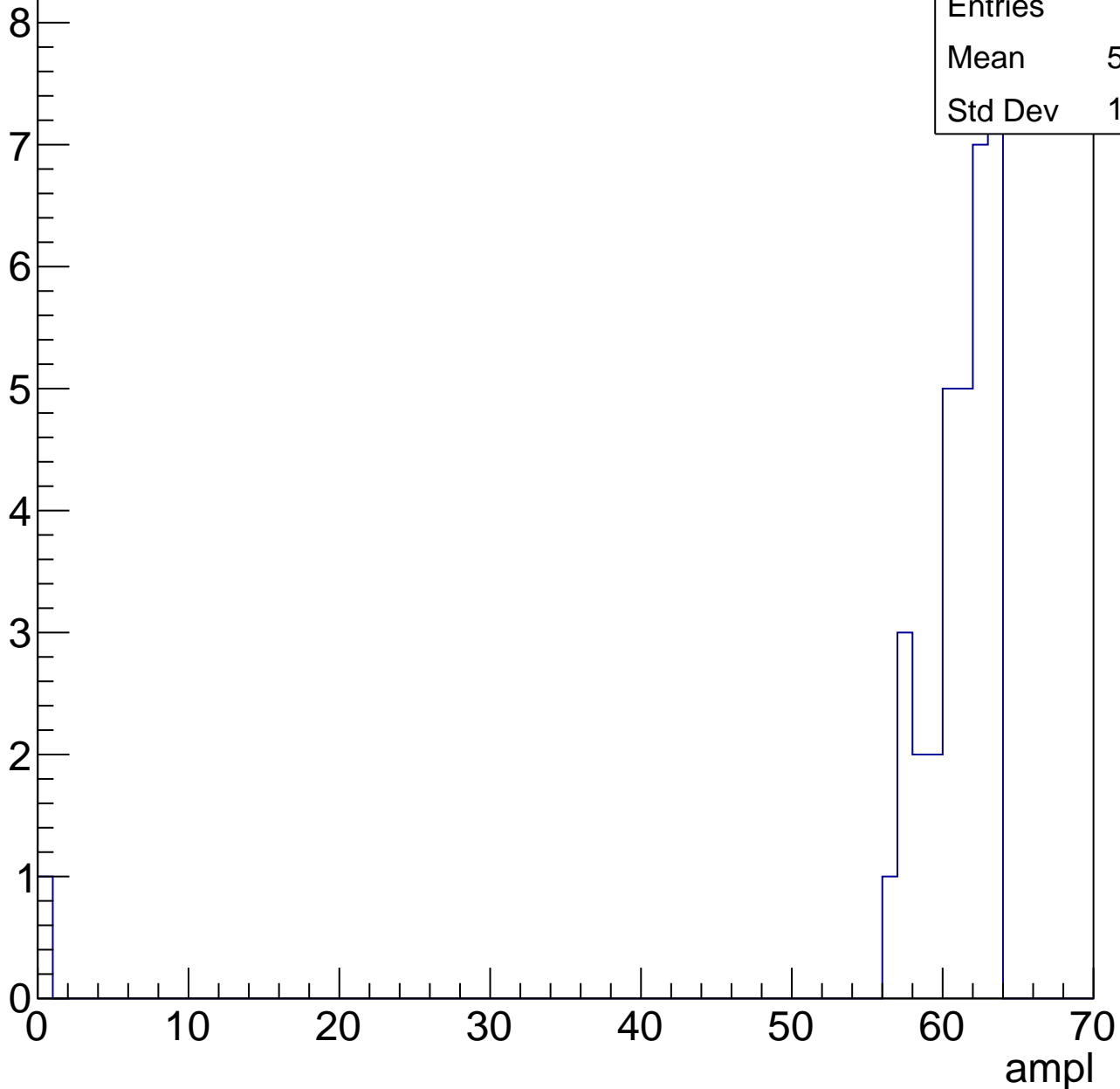


# B1L103S, U4-ch11, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 34    |
| Mean    | 58.94 |
| Std Dev | 10.46 |



# B1L103S, U4-ch11, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U4-ch11, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

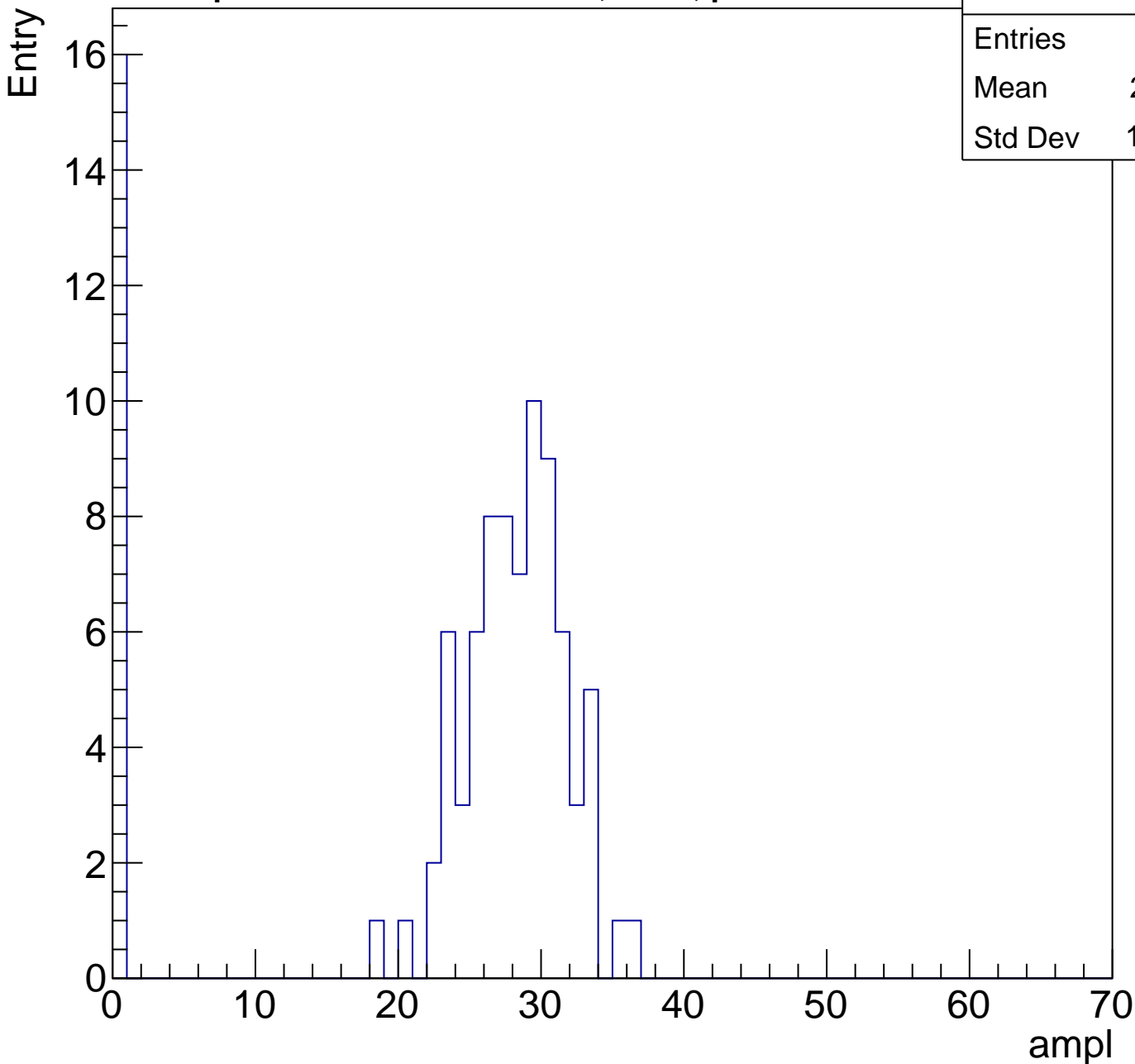
ampl

|         |    |
|---------|----|
| Entries | 19 |
| Mean    | 0  |
| Std Dev | 0  |

# B1L103S, U4-ch12, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 93    |
| Mean    | 23.01 |
| Std Dev | 10.95 |

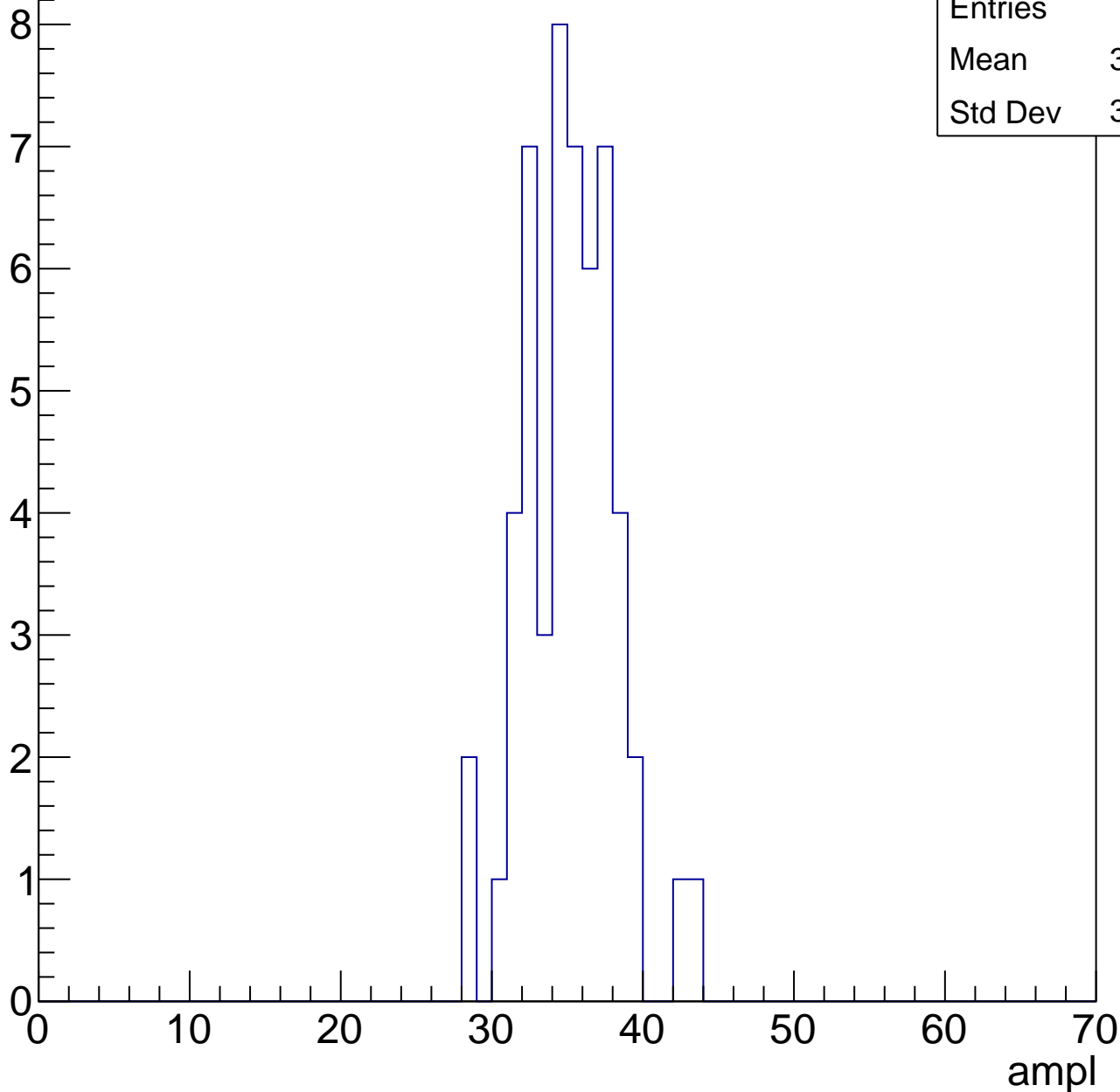


# B1L103S, U4-ch12, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 53    |
| Mean    | 34.72 |
| Std Dev | 3.012 |



# B1L103S, U4-ch12, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 93    |
| Mean    | 35.74 |
| Std Dev | 14.92 |

Entry

12

10

8

6

4

2

0

0

10

20

30

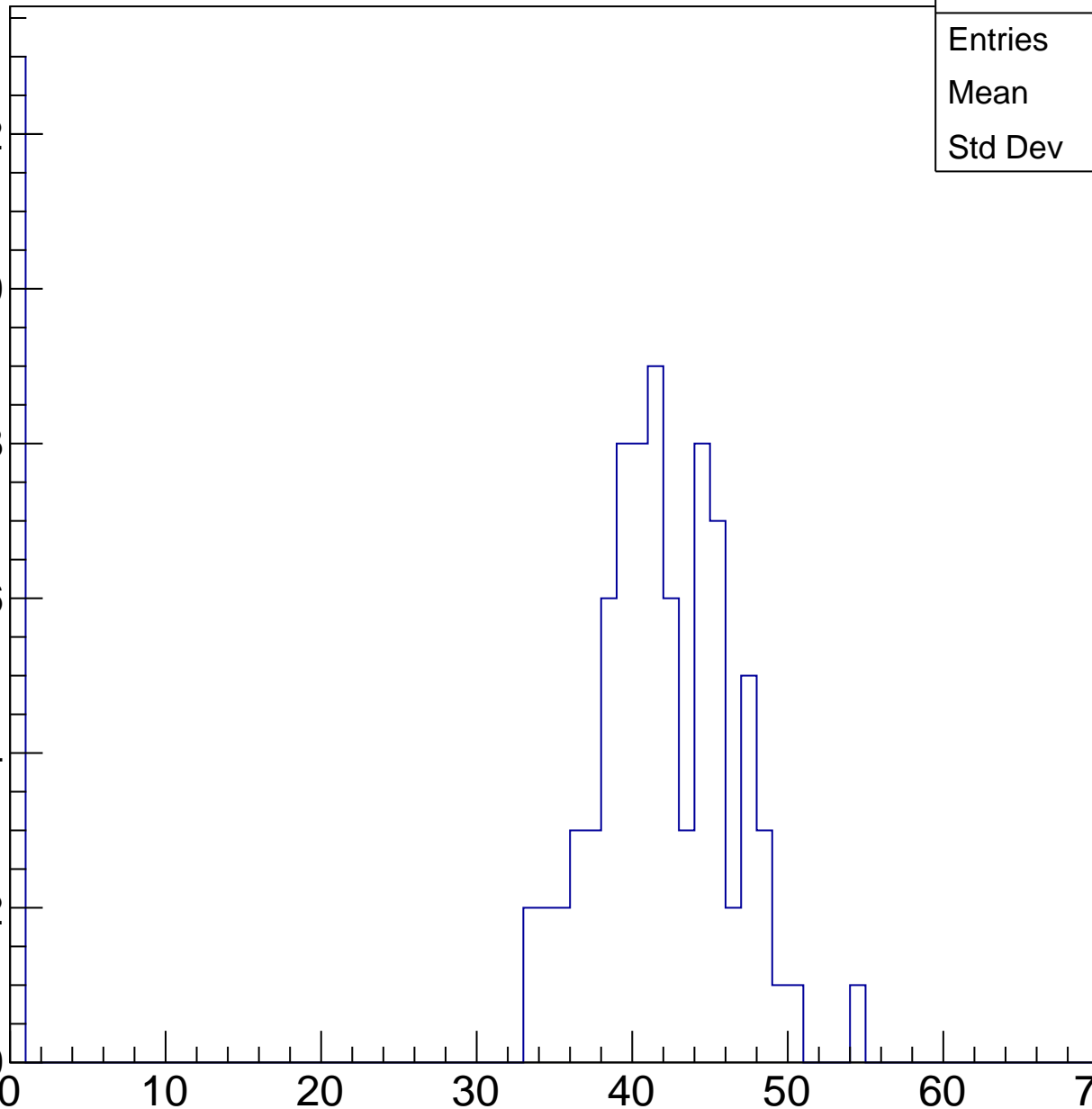
40

50

60

70

ampl

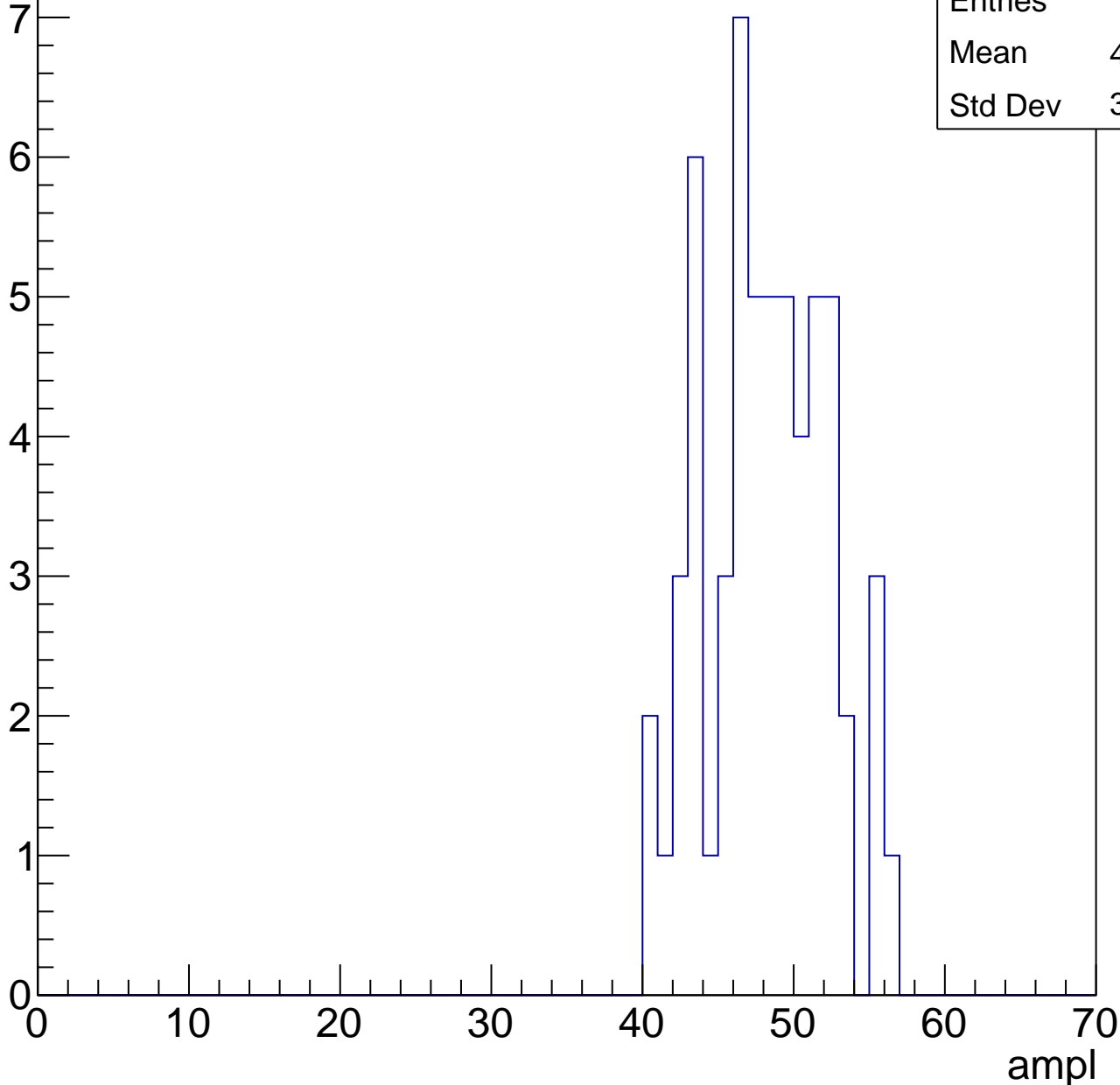


# B1L103S, U4-ch12, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 58    |
| Mean    | 47.72 |
| Std Dev | 3.969 |

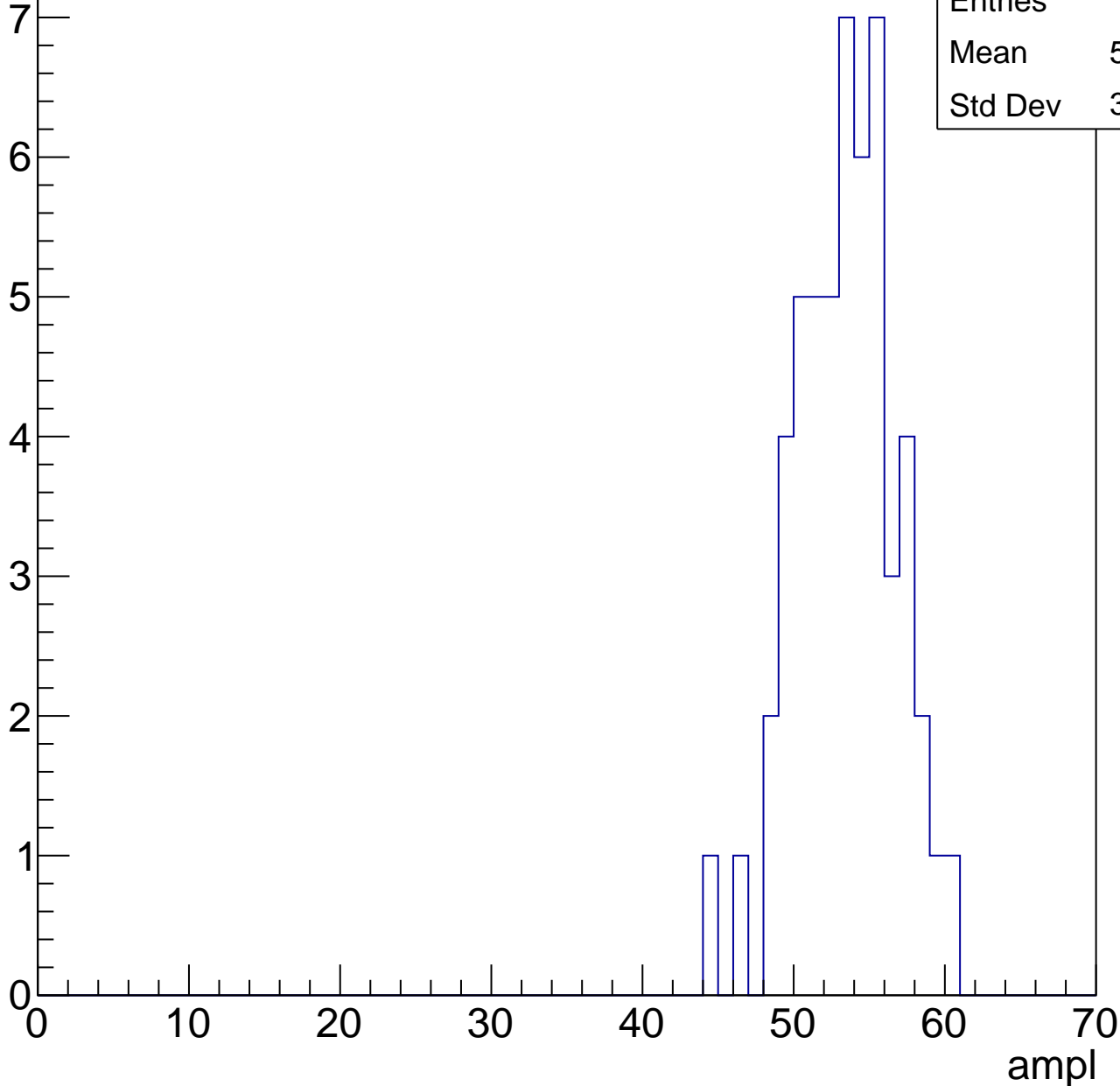


# B1L103S, U4-ch12, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 54    |
| Mean    | 52.93 |
| Std Dev | 3.259 |



# B1L103S, U4-ch12, adc5

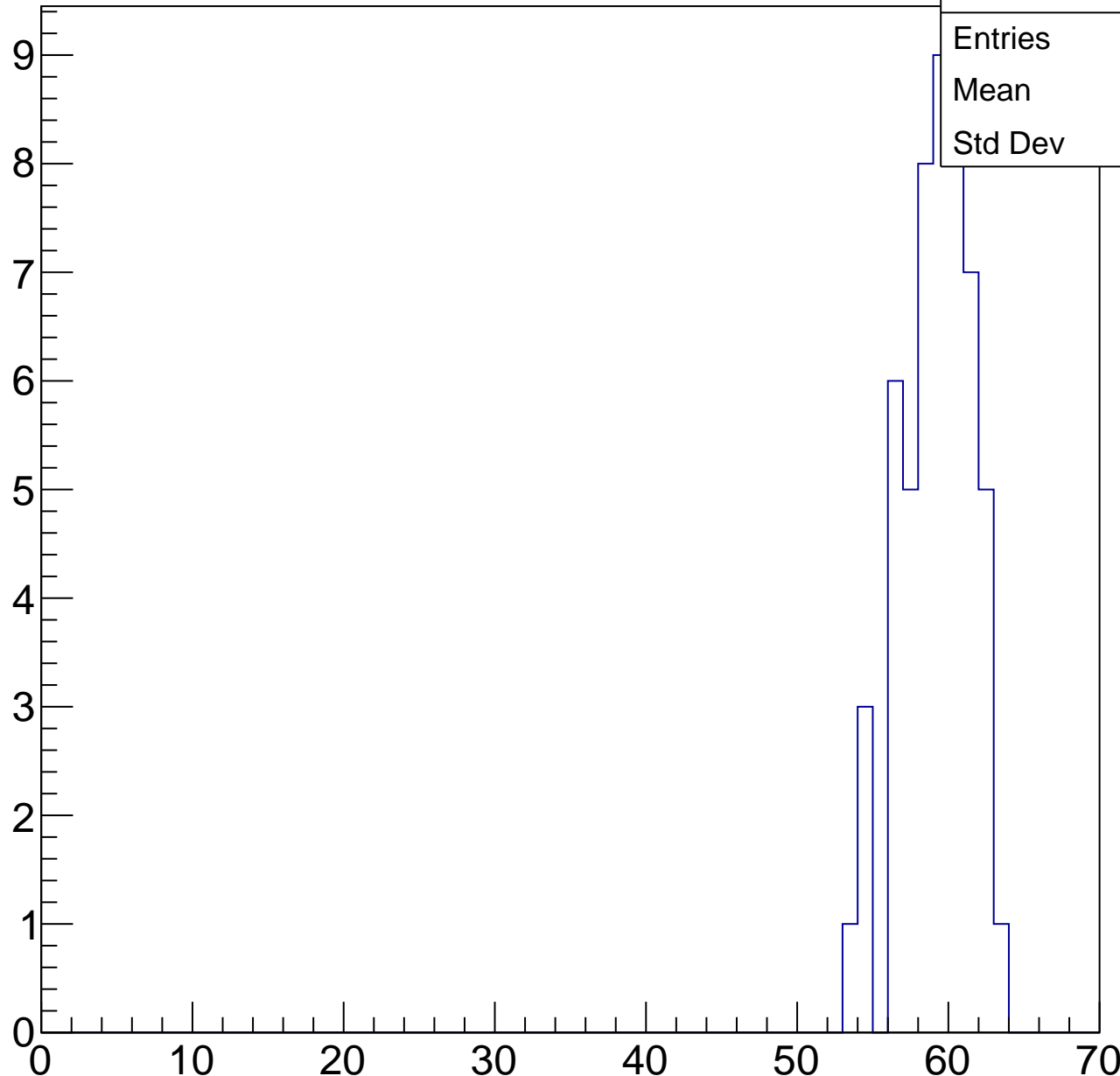
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

|         |      |
|---------|------|
| Entries | 53   |
| Mean    | 58.7 |
| Std Dev | 2.32 |

ampl

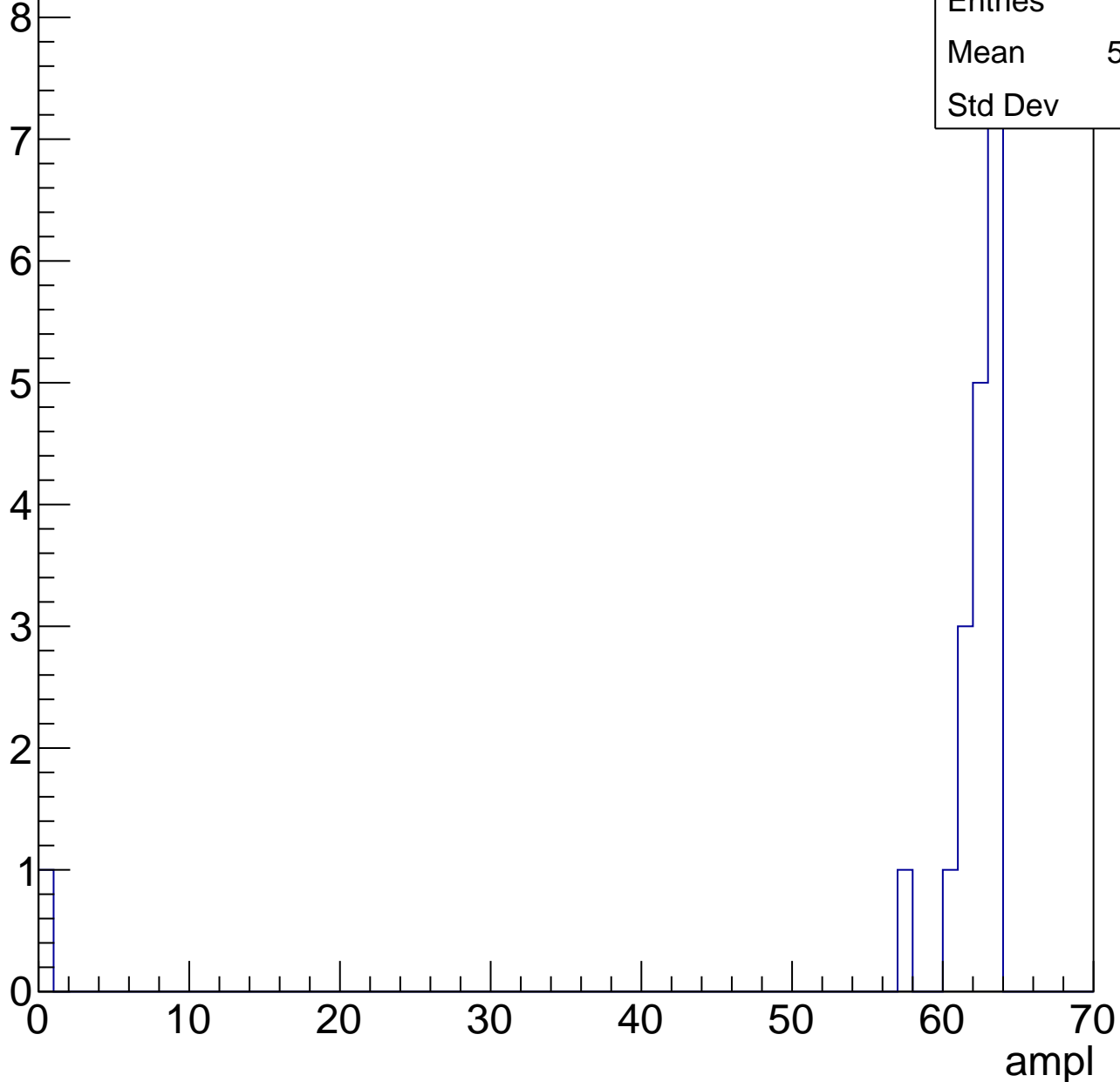


# B1L103S, U4-ch12, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 19    |
| Mean    | 58.63 |
| Std Dev | 13.9  |





# B1L103S, U4-ch12, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



|         |       |
|---------|-------|
| Entries | 20    |
| Mean    | 3.15  |
| Std Dev | 13.73 |

# B1L103S, U4-ch13, adc0

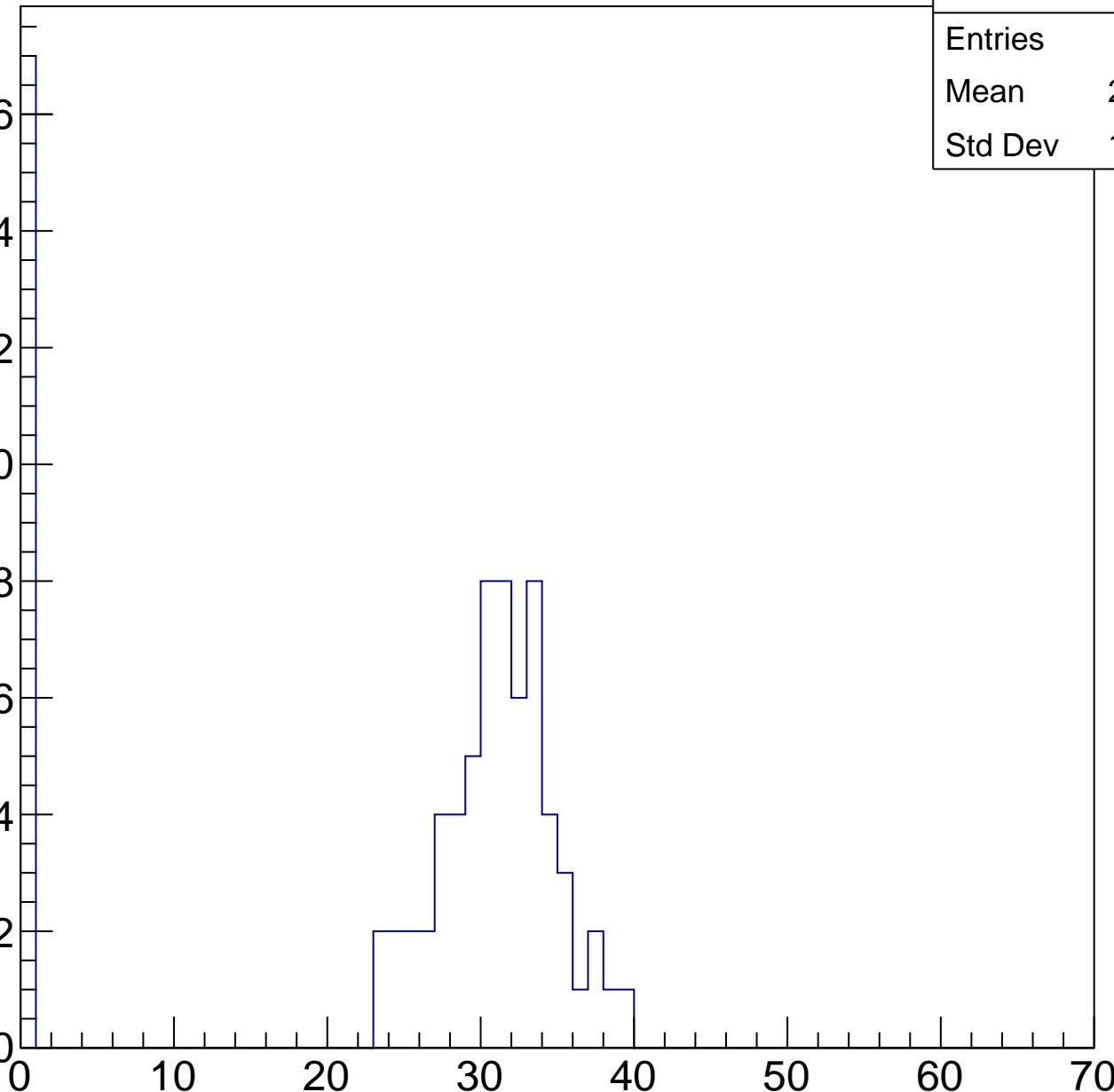
calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 80    |
| Mean    | 24.16 |
| Std Dev | 12.94 |

Entry

16  
14  
12  
10  
8  
6  
4  
2  
0

ampl

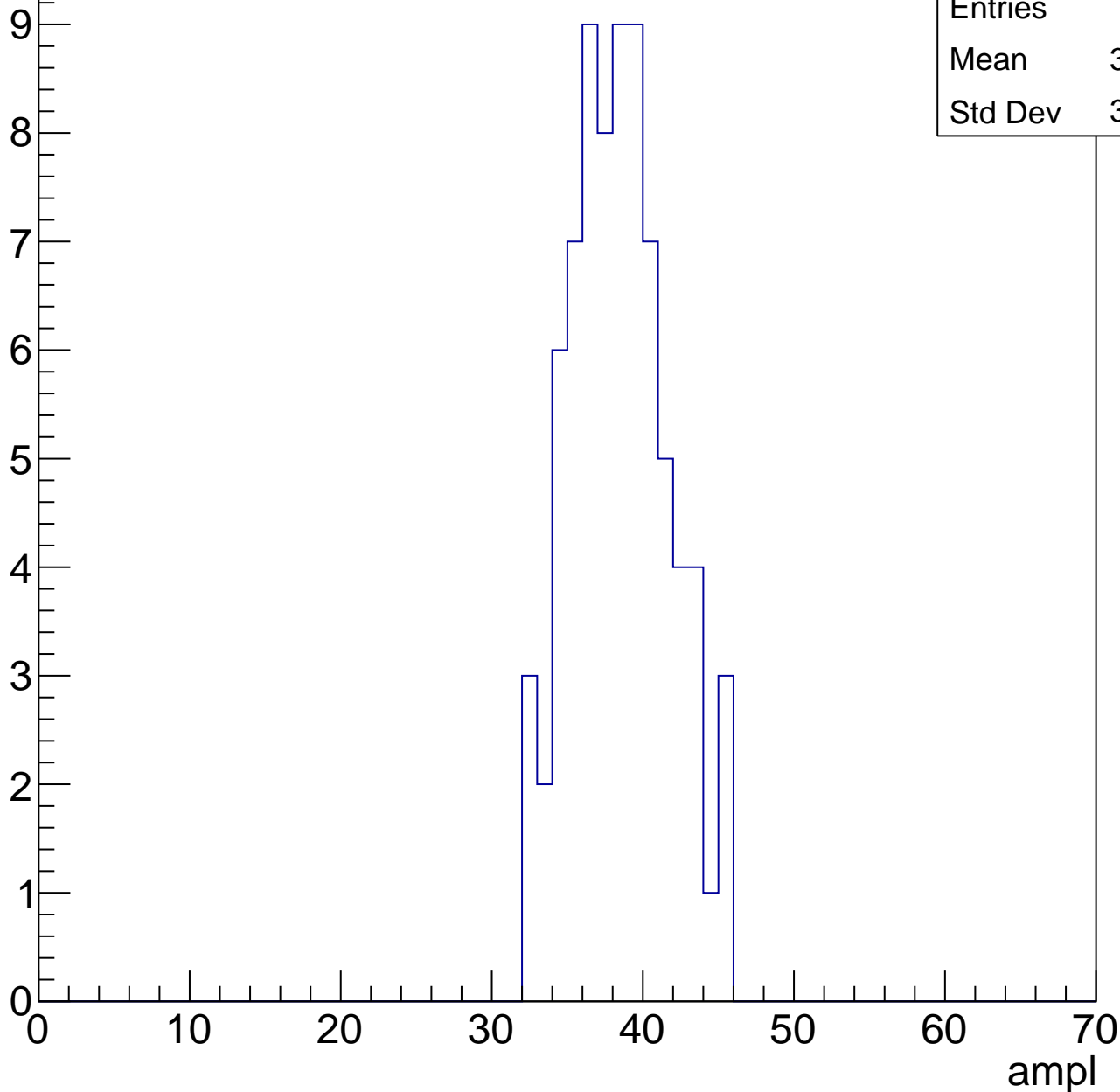


# B1L103S, U4-ch13, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 77    |
| Mean    | 38.03 |
| Std Dev | 3.203 |



# B1L103S, U4-ch13, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

10

8

6

4

2

0

Entries 72

Mean 38.4

Std Dev 16.61

ampl

0

10

20

30

40

50

60

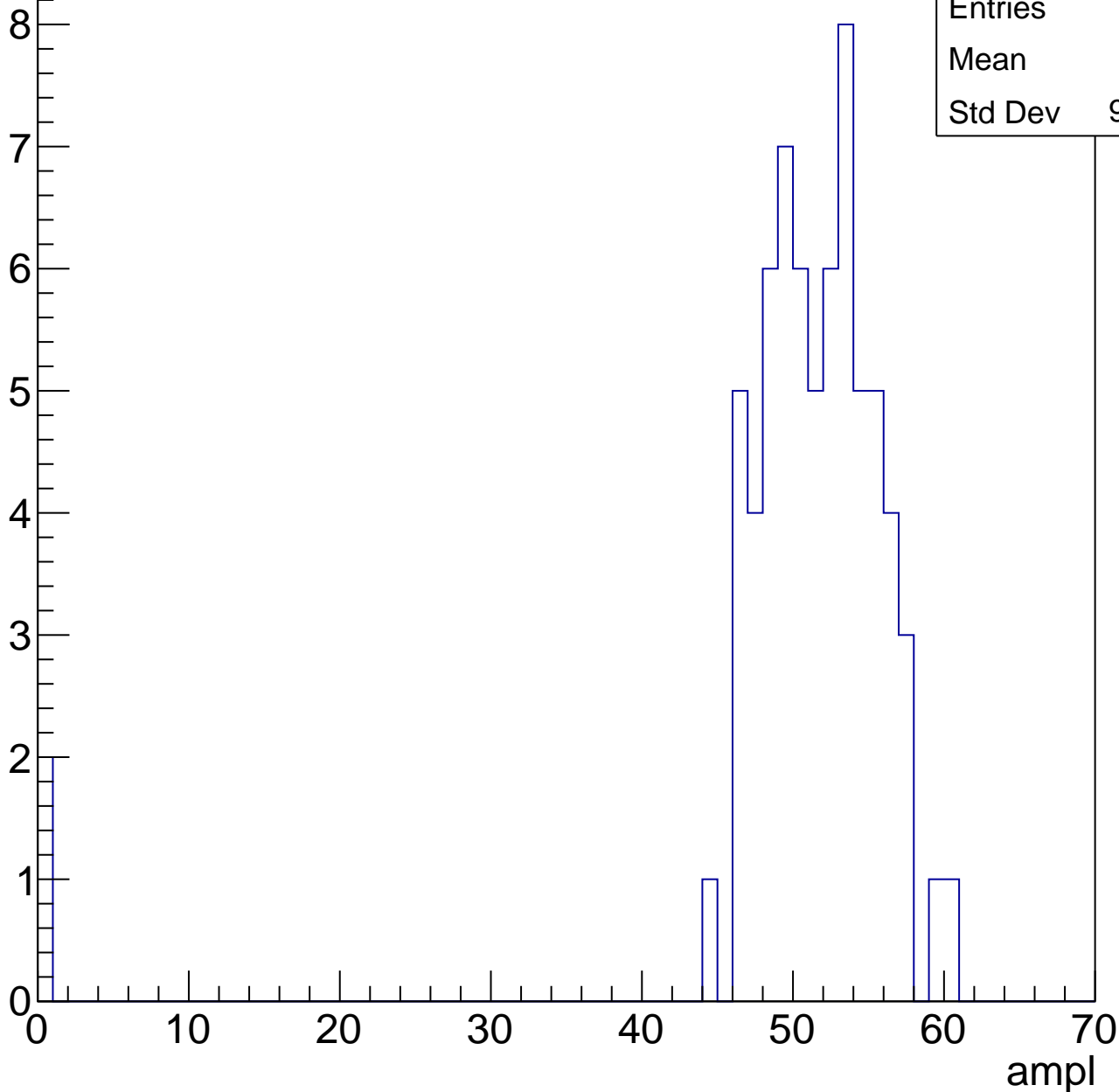
70

# B1L103S, U4-ch13, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 69    |
| Mean    | 49.9  |
| Std Dev | 9.294 |

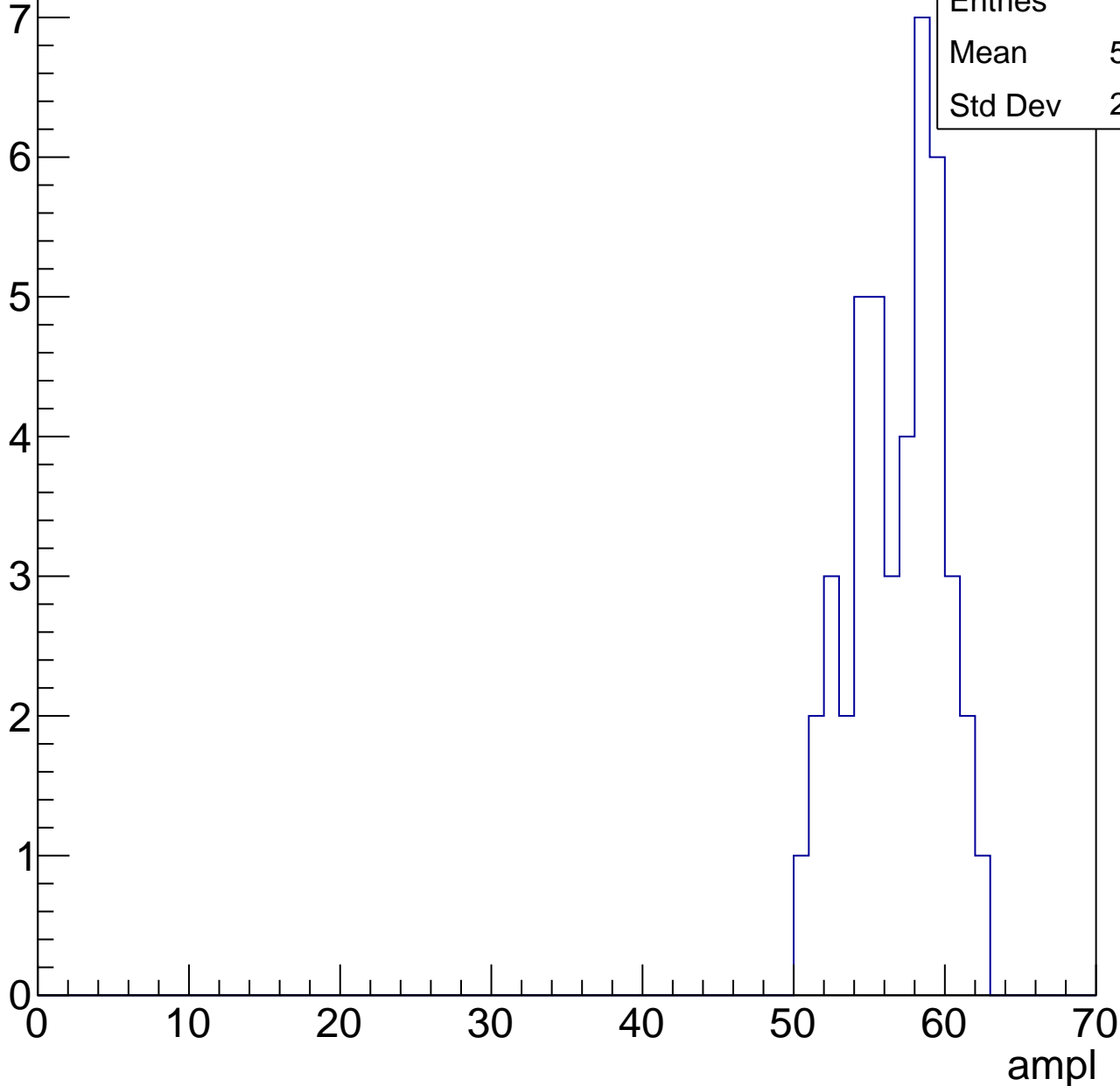


# B1L103S, U4-ch13, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 44    |
| Mean    | 56.34 |
| Std Dev | 2.984 |

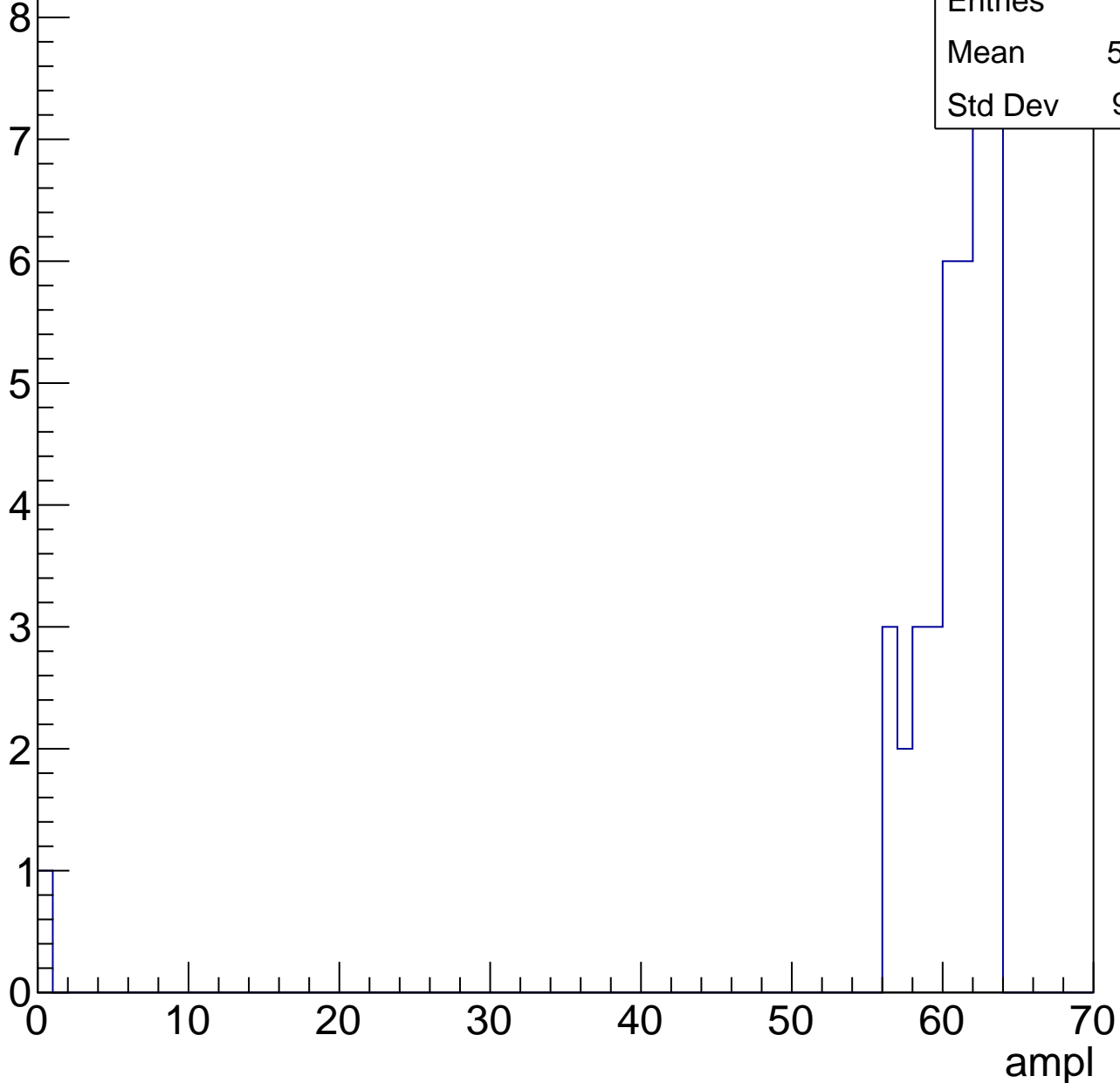


# B1L103S, U4-ch13, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 40    |
| Mean    | 58.98 |
| Std Dev | 9.681 |



# B1L103S, U4-ch13, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

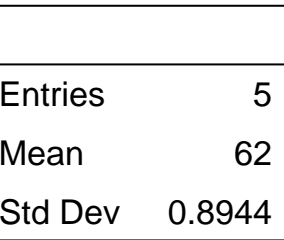
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

|         |        |
|---------|--------|
| Entries | 5      |
| Mean    | 62     |
| Std Dev | 0.8944 |

0 10 20 30 40 50 60 70

ampl





# B1L103S, U4-ch13, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

|         |    |
|---------|----|
| Entries | 19 |
| Mean    | 0  |
| Std Dev | 0  |

# B1L103S, U4-ch14, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 108   |
| Mean    | 21.33 |
| Std Dev | 12.93 |

Entry

25

20

15

10

5

0

0

10

20

30

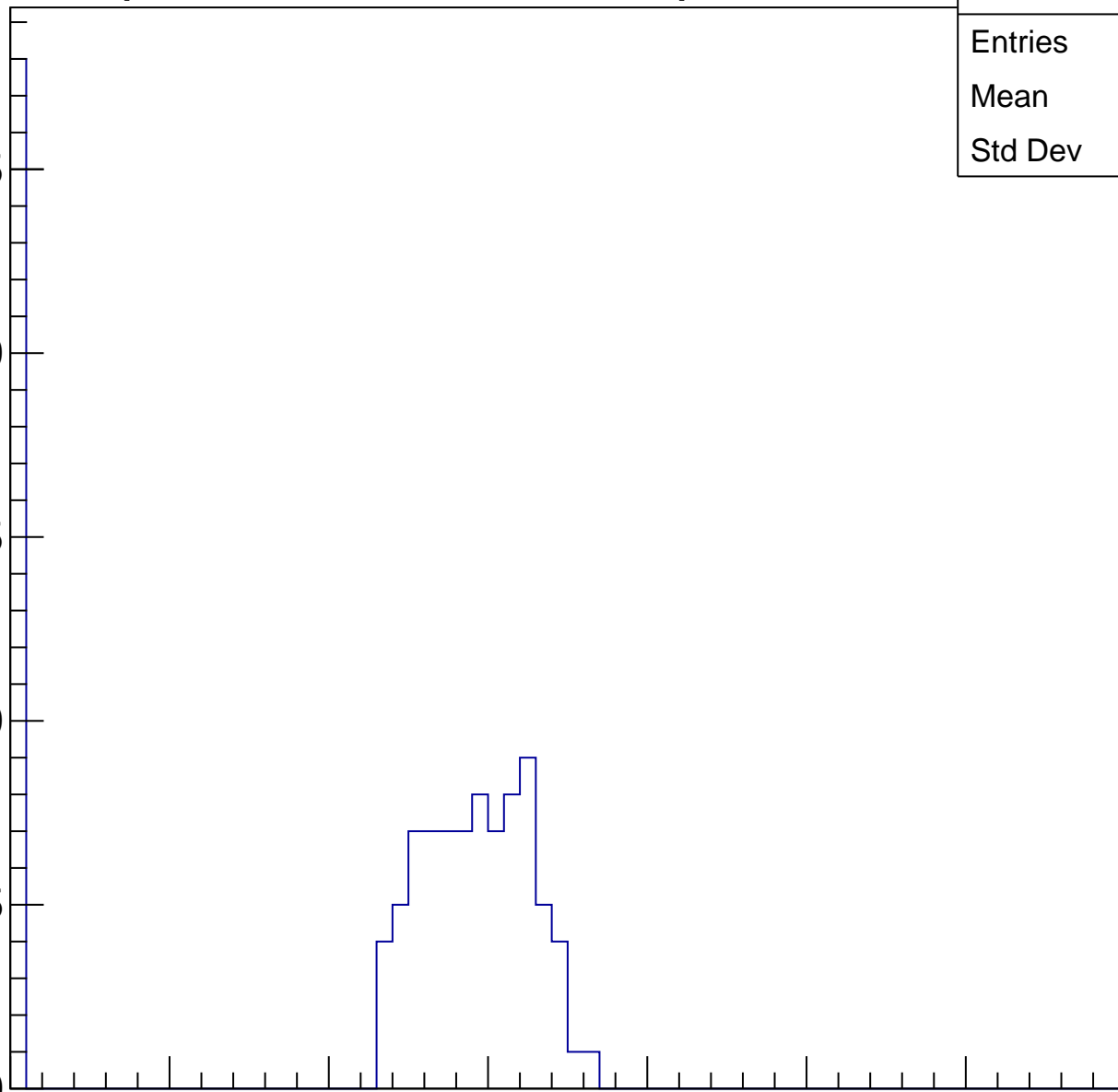
40

50

60

70

ampl

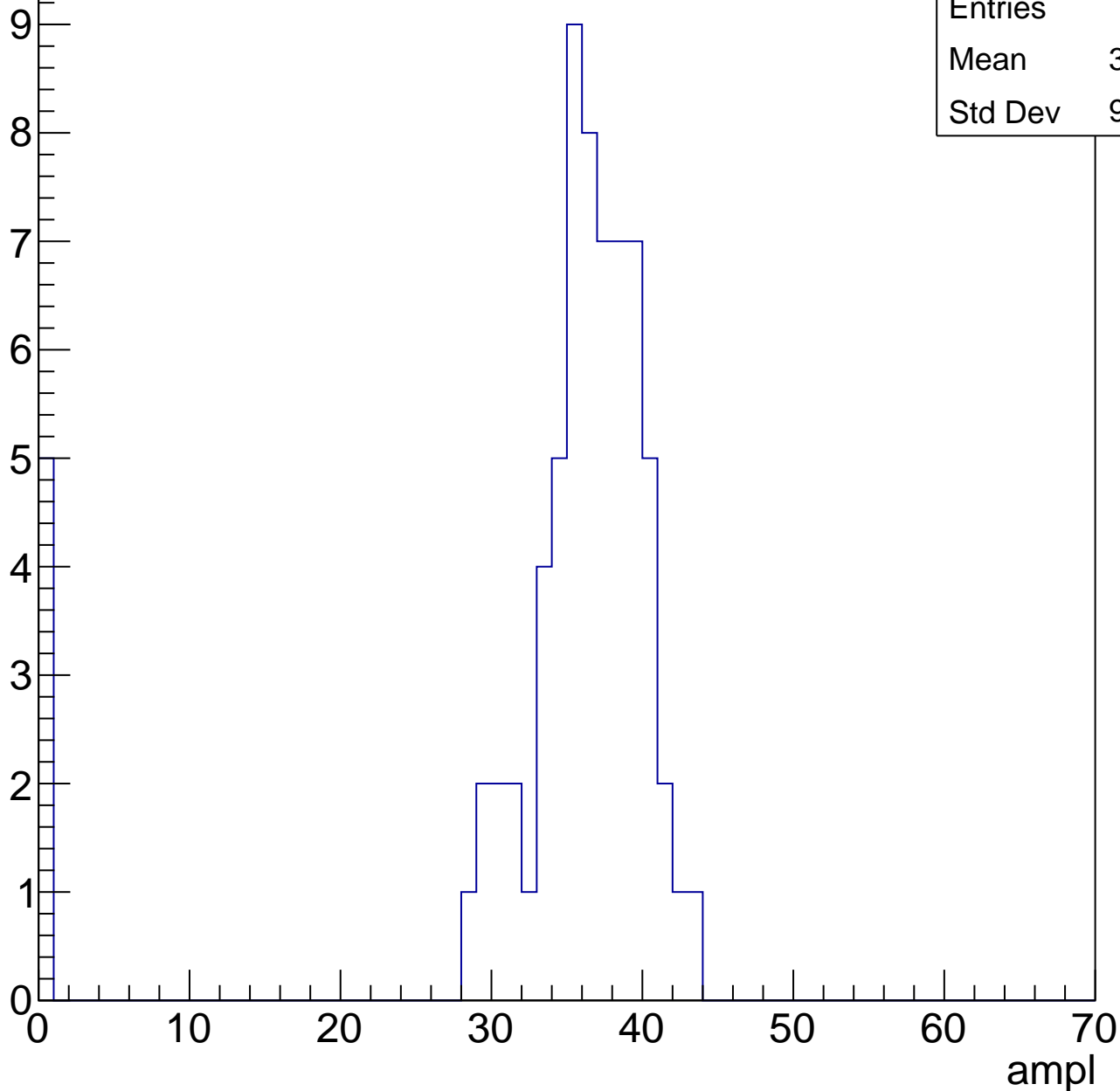


# B1L103S, U4-ch14, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 69    |
| Mean    | 33.48 |
| Std Dev | 9.868 |

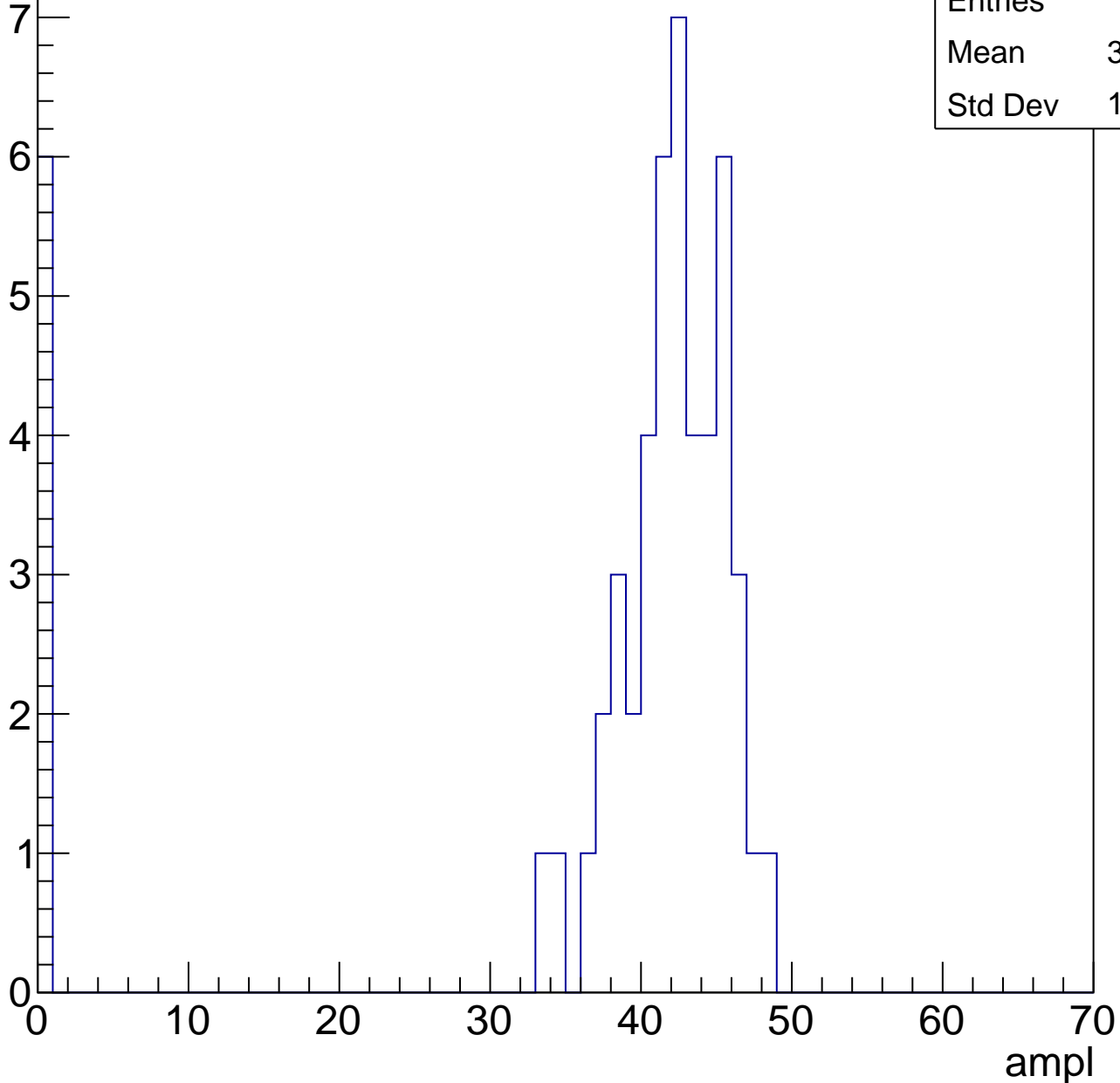


# B1L103S, U4-ch14, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 52    |
| Mean    | 36.92 |
| Std Dev | 13.69 |

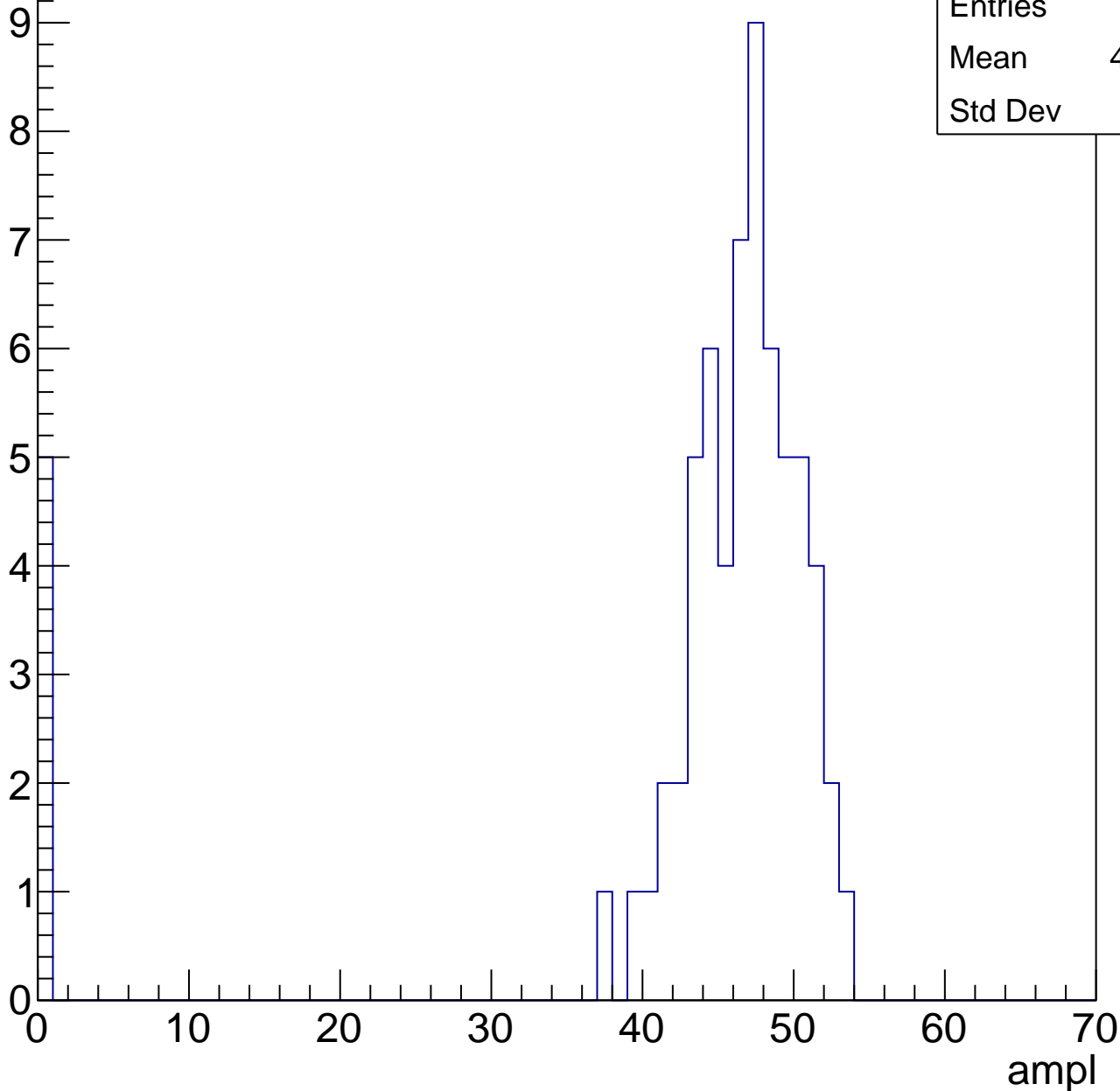


# B1L103S, U4-ch14, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

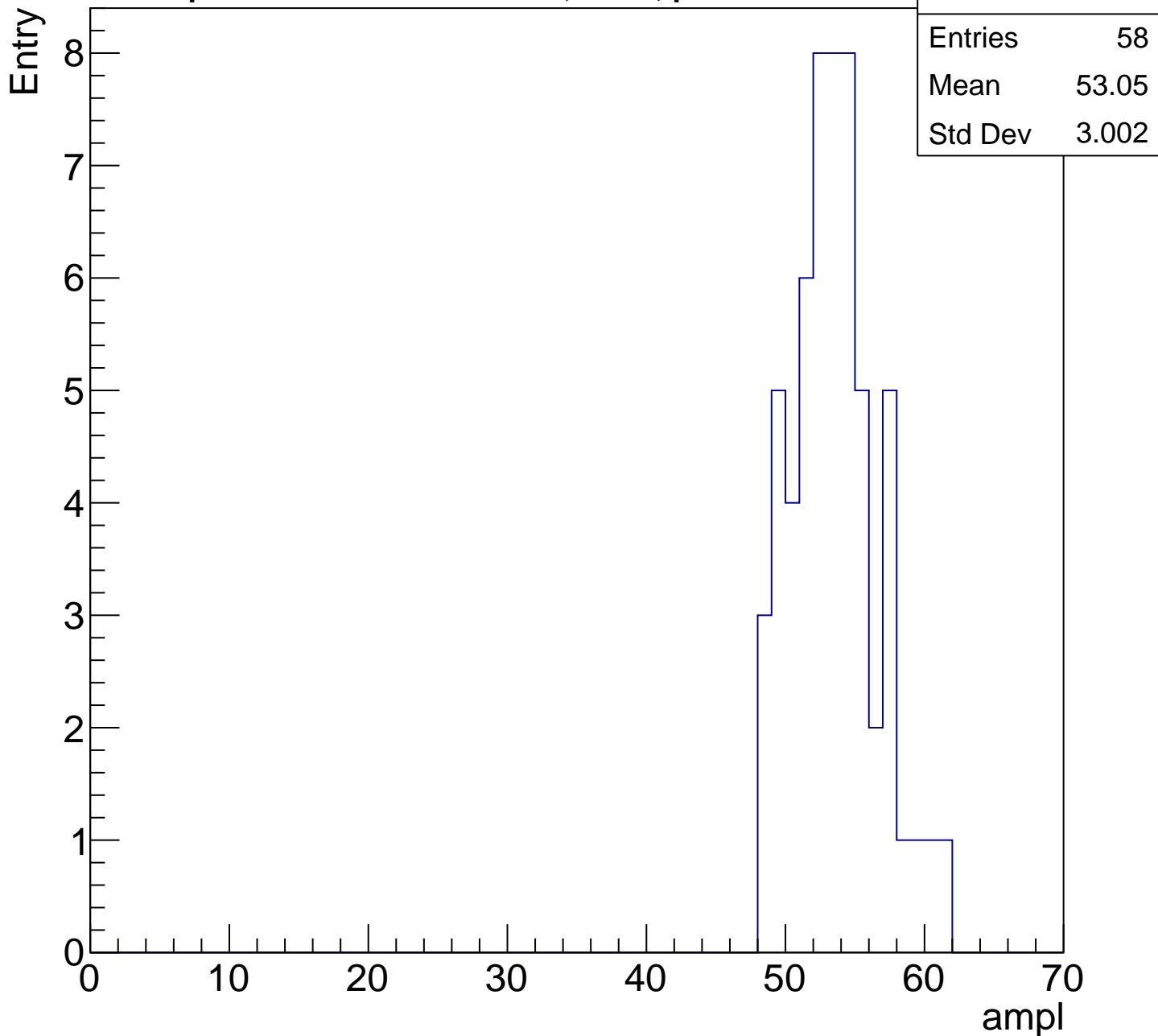
Entry

|         |       |
|---------|-------|
| Entries | 66    |
| Mean    | 42.88 |
| Std Dev | 12.7  |



# B1L103S, U4-ch14, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

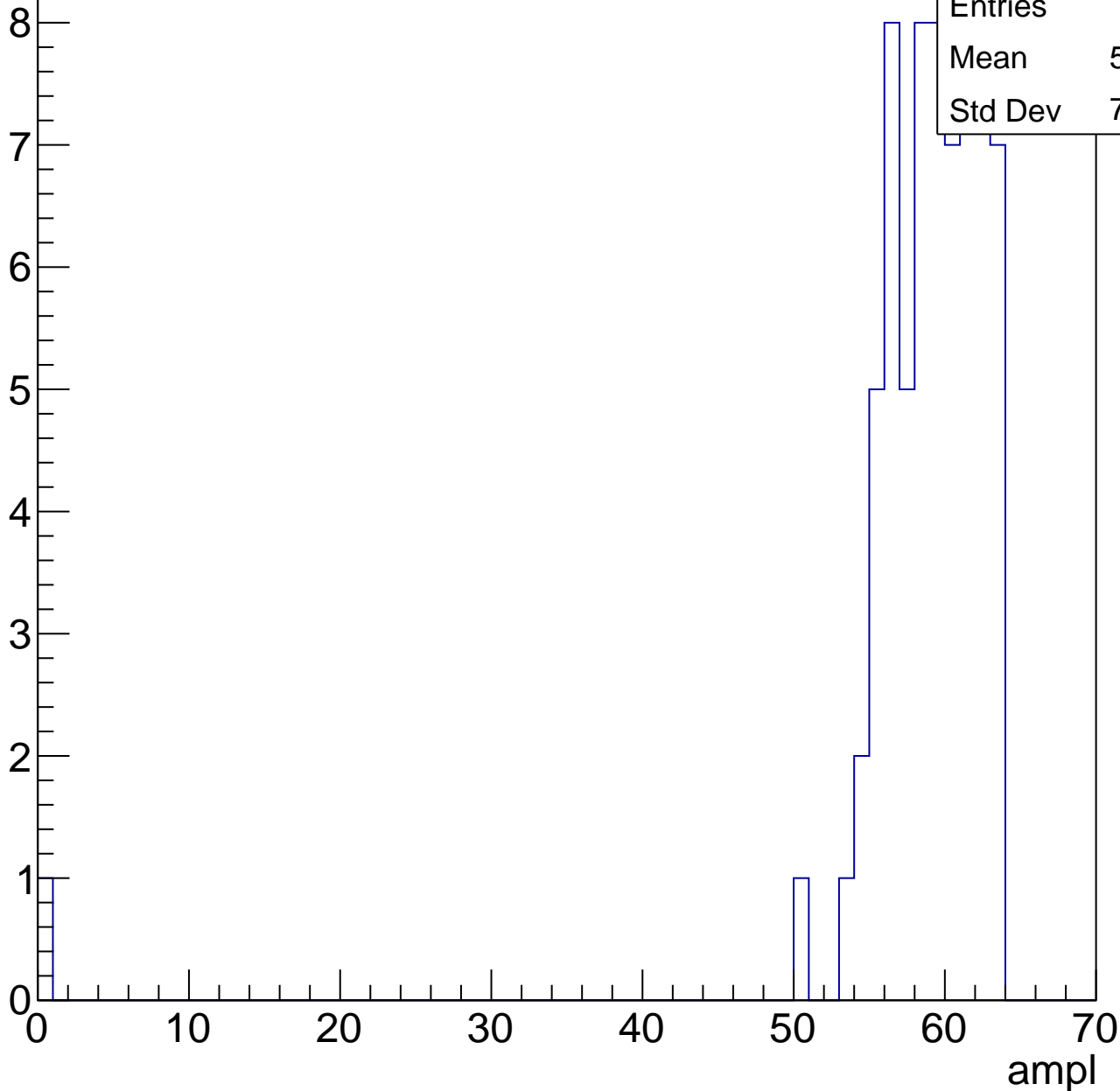


# B1L103S, U4-ch14, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

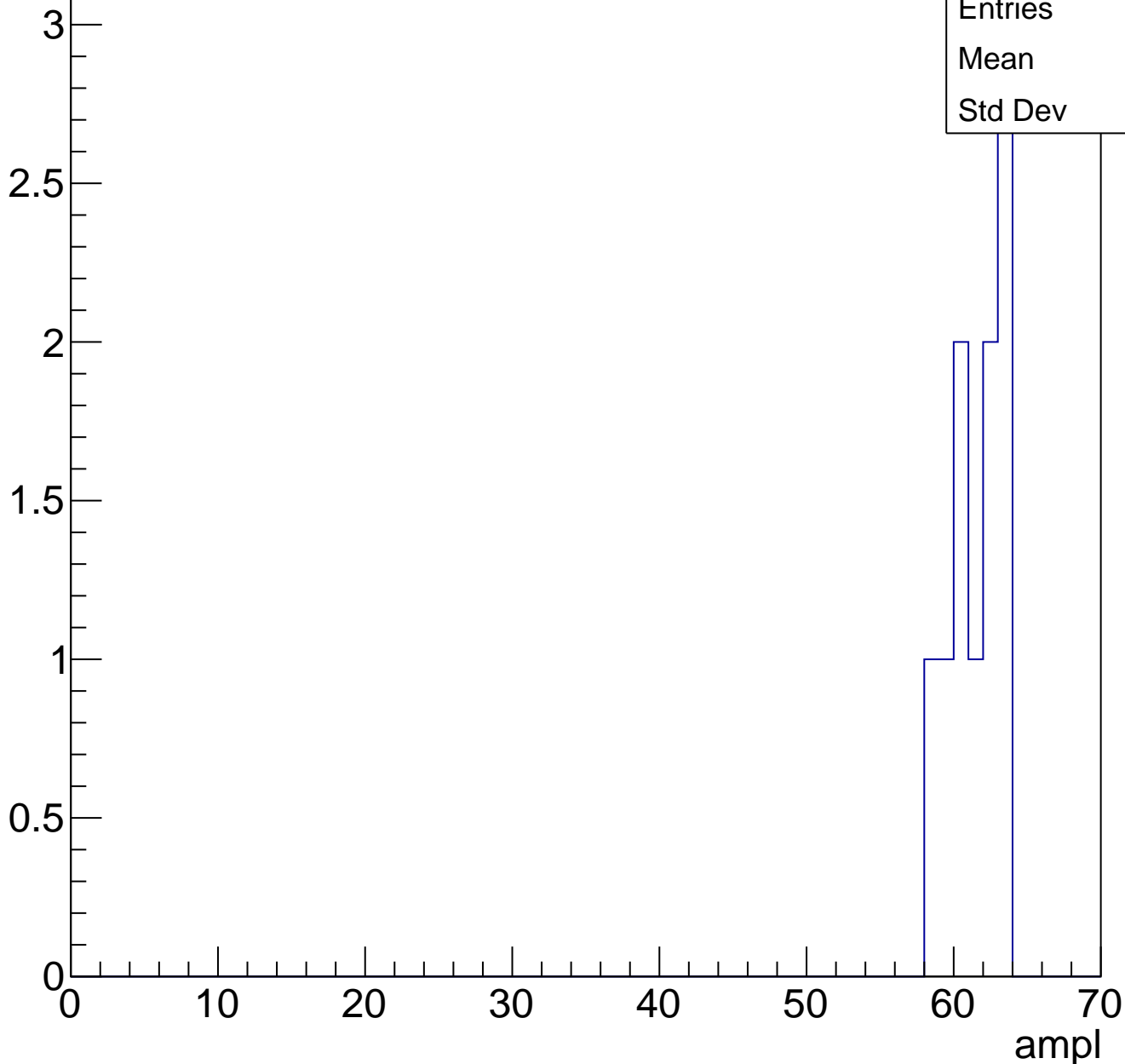
|         |       |
|---------|-------|
| Entries | 69    |
| Mean    | 57.97 |
| Std Dev | 7.593 |



# B1L103S, U4-ch14, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U4-ch14, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



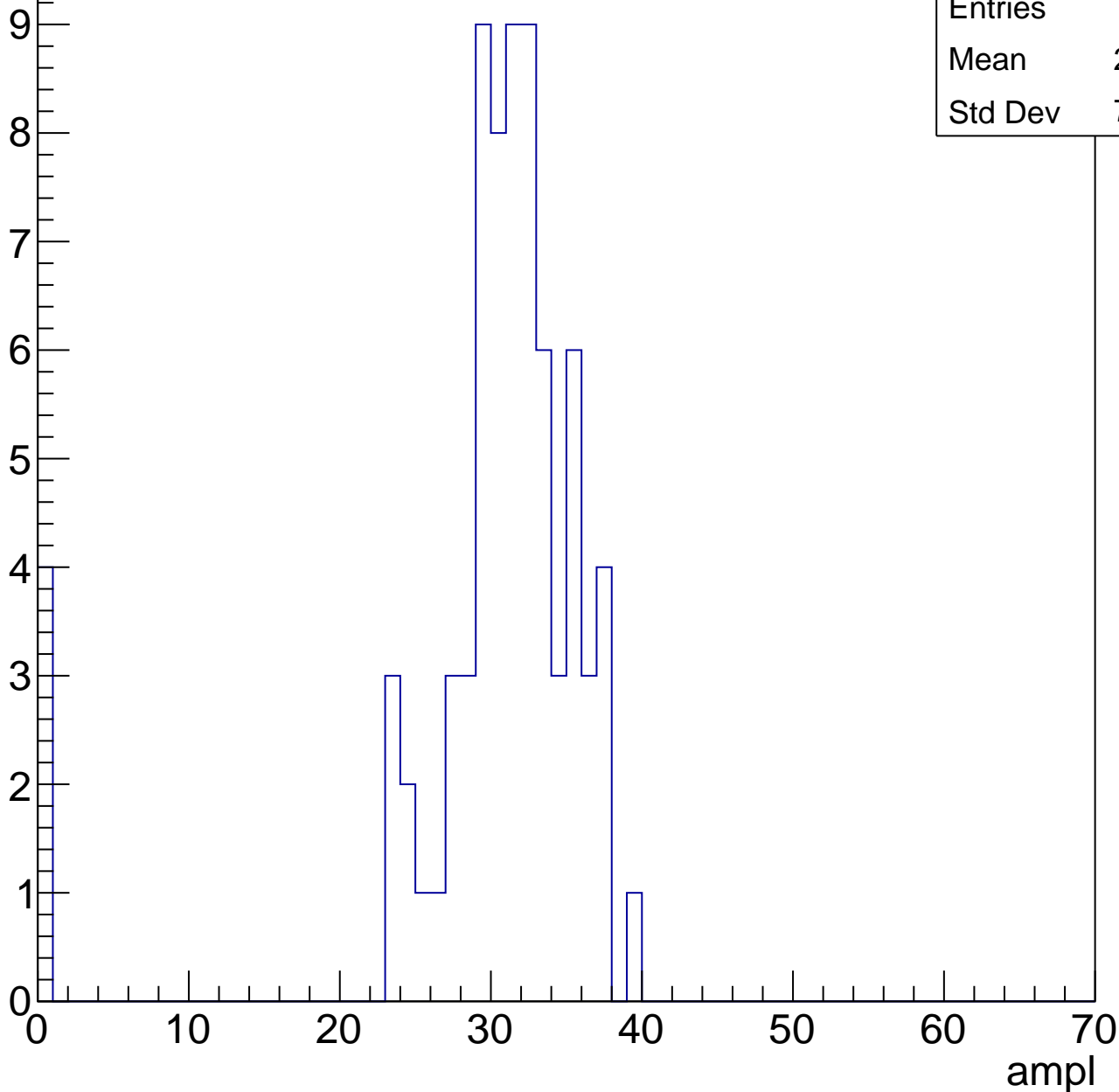
|         |    |
|---------|----|
| Entries | 19 |
| Mean    | 0  |
| Std Dev | 0  |

# B1L103S, U4-ch15, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 75    |
| Mean    | 29.41 |
| Std Dev | 7.801 |

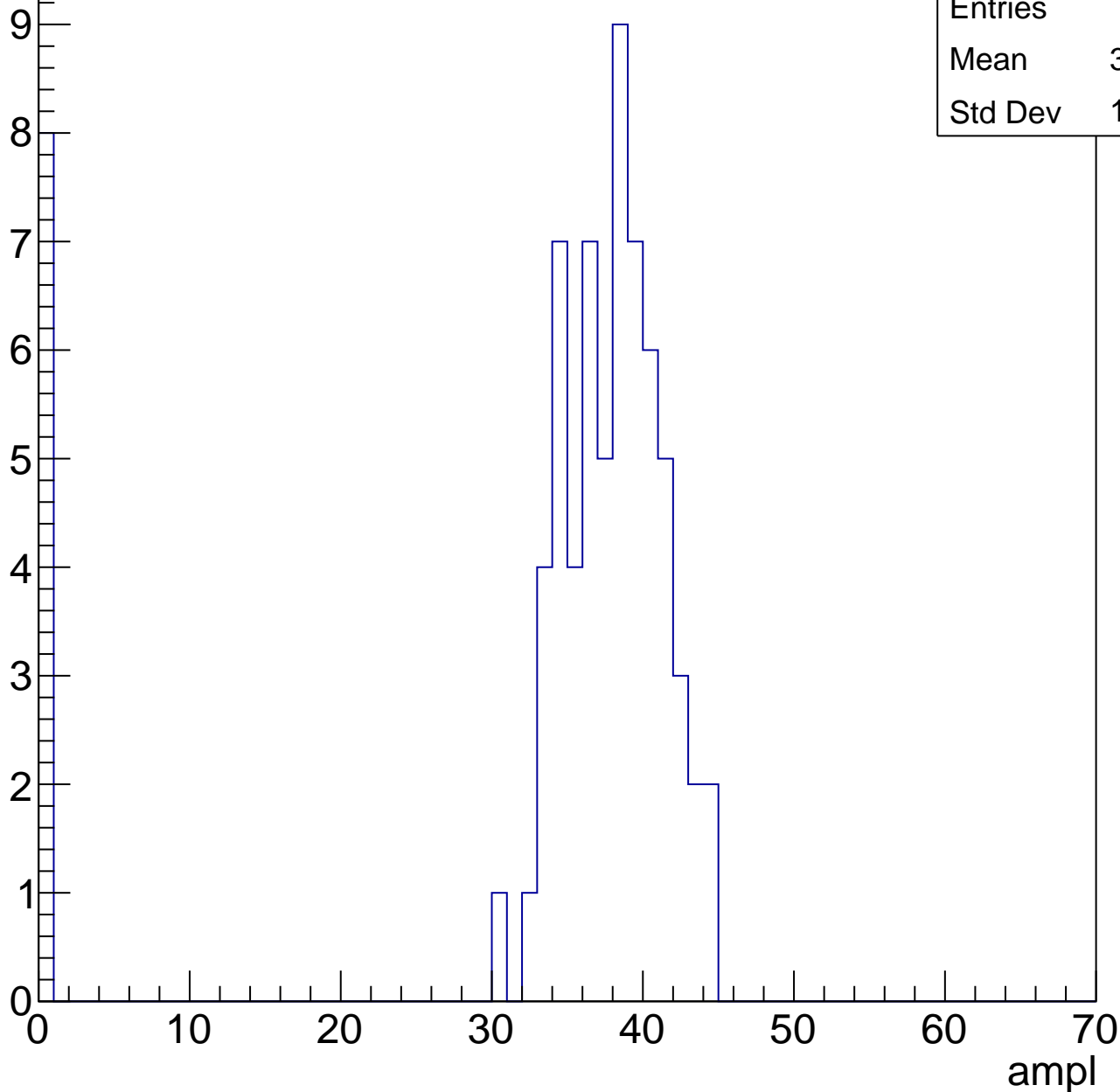


# B1L103S, U4-ch15, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 71    |
| Mean    | 33.37 |
| Std Dev | 12.25 |



# B1L103S, U4-ch15, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 78    |
| Mean    | 42.96 |
| Std Dev | 9.194 |

Entry

10

8

6

4

2

0

0

10

20

30

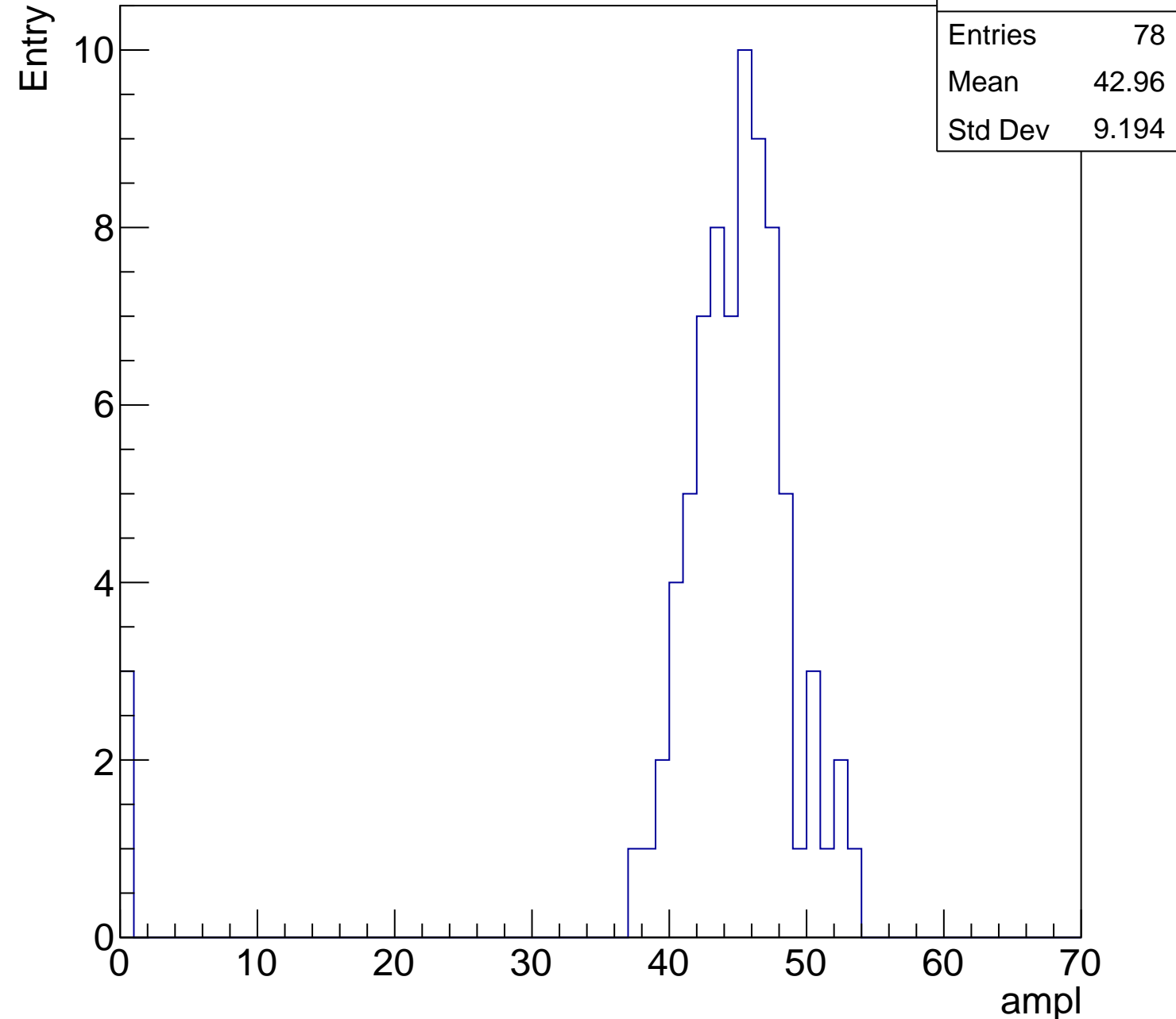
40

50

60

70

ampl

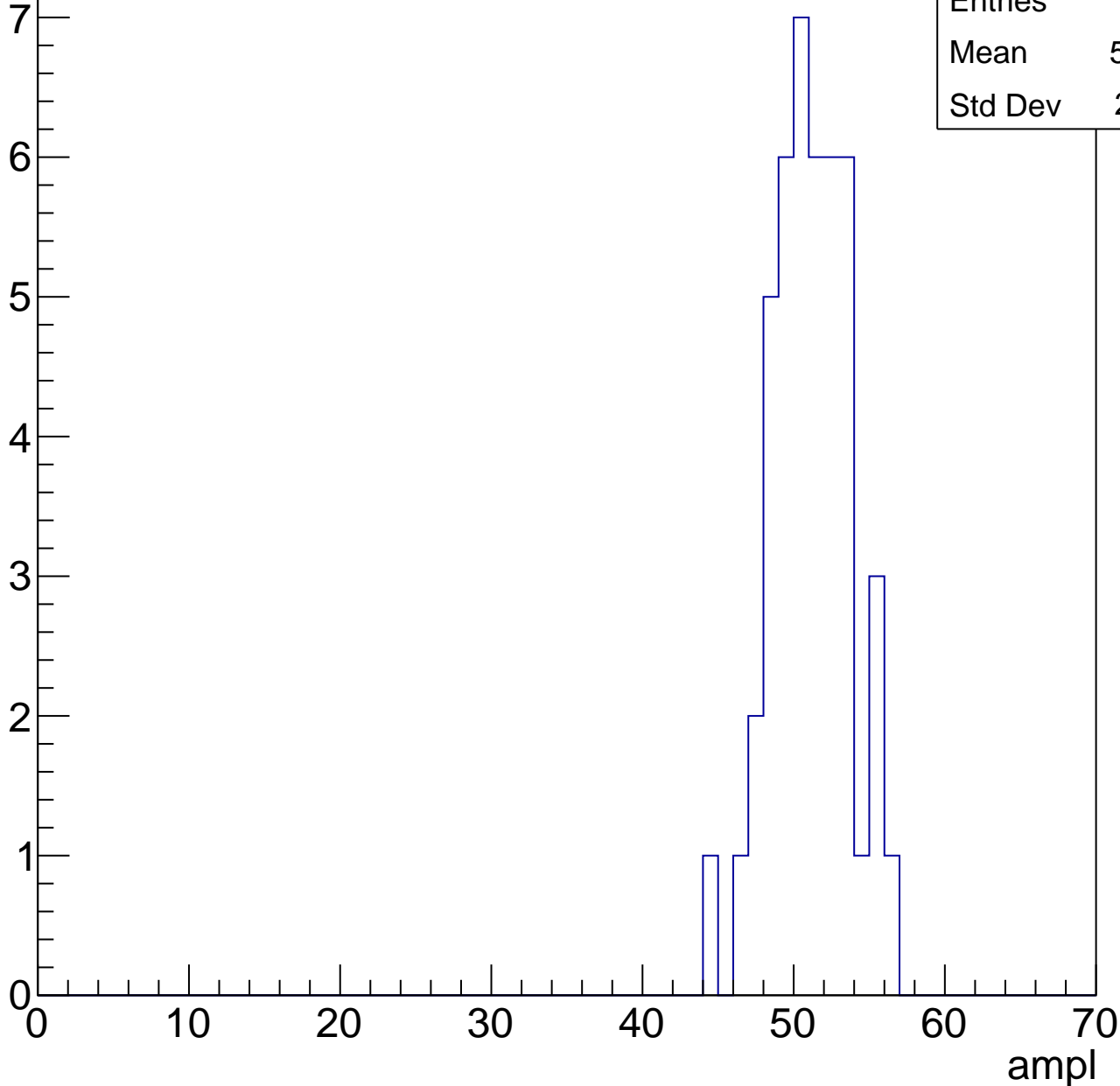


# B1L103S, U4-ch15, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 45    |
| Mean    | 50.64 |
| Std Dev | 2.531 |

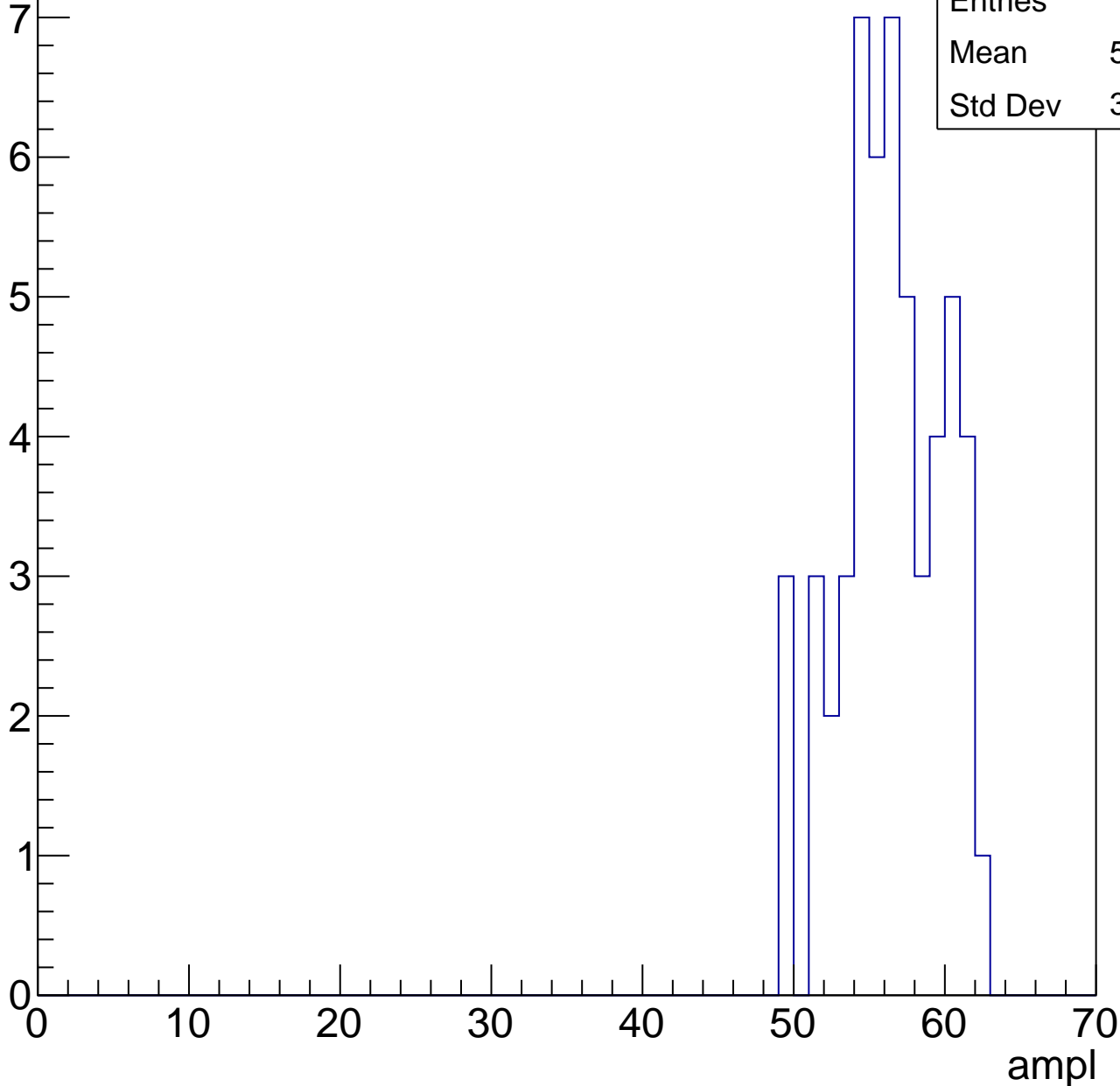


# B1L103S, U4-ch15, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 53    |
| Mean    | 55.92 |
| Std Dev | 3.319 |

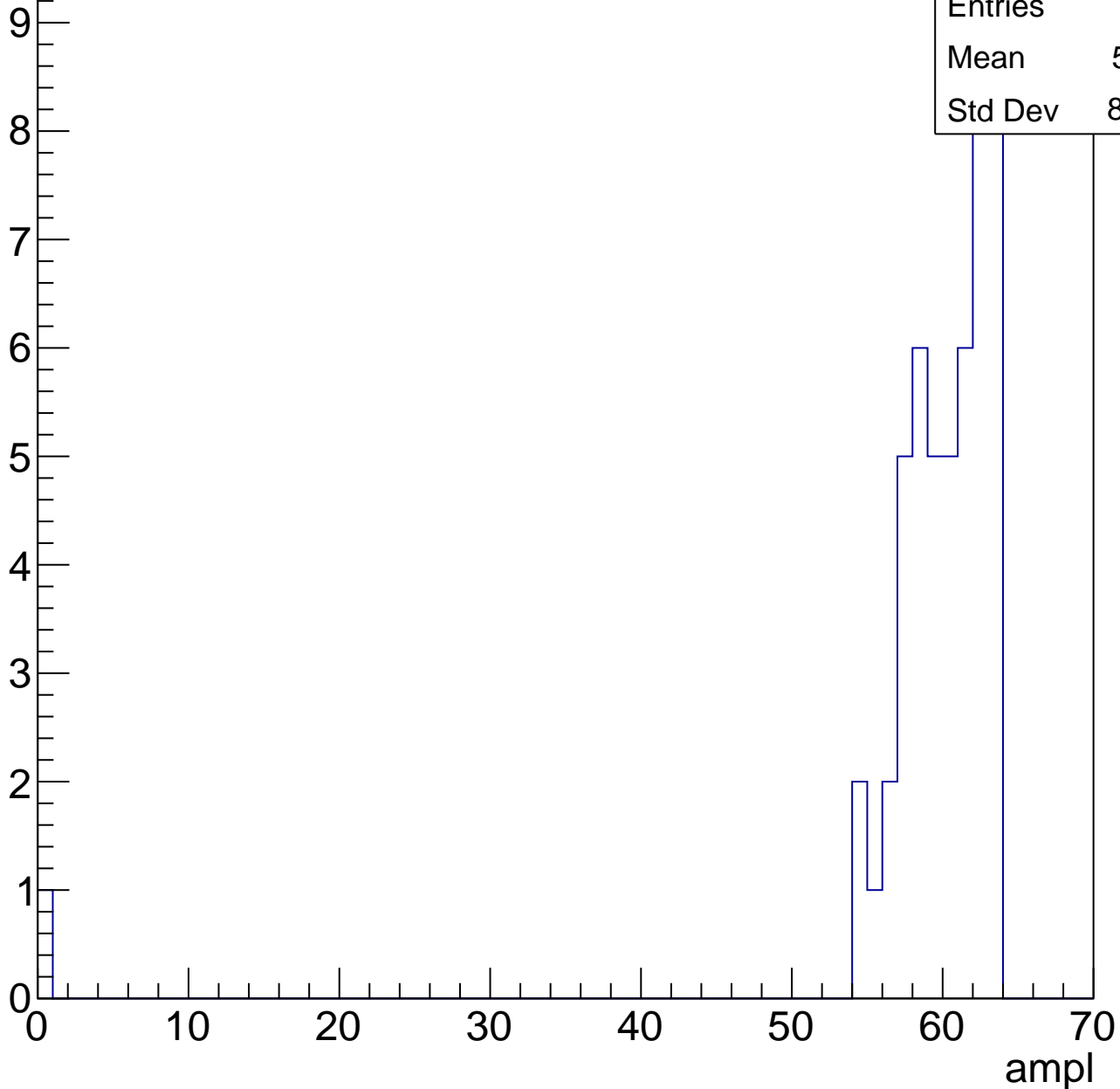


# B1L103S, U4-ch15, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

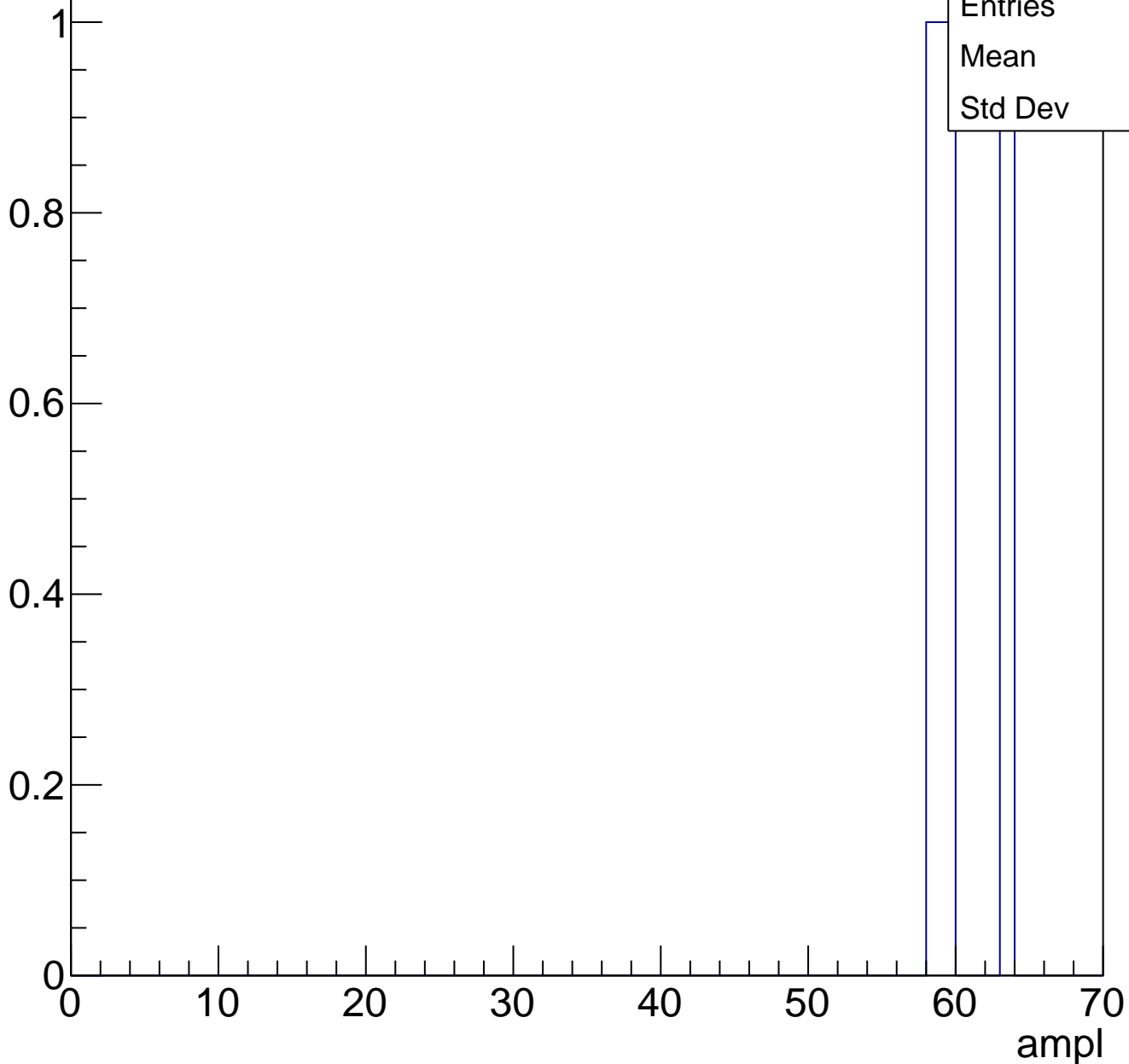
|         |       |
|---------|-------|
| Entries | 51    |
| Mean    | 58.71 |
| Std Dev | 8.678 |



# B1L103S, U4-ch15, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

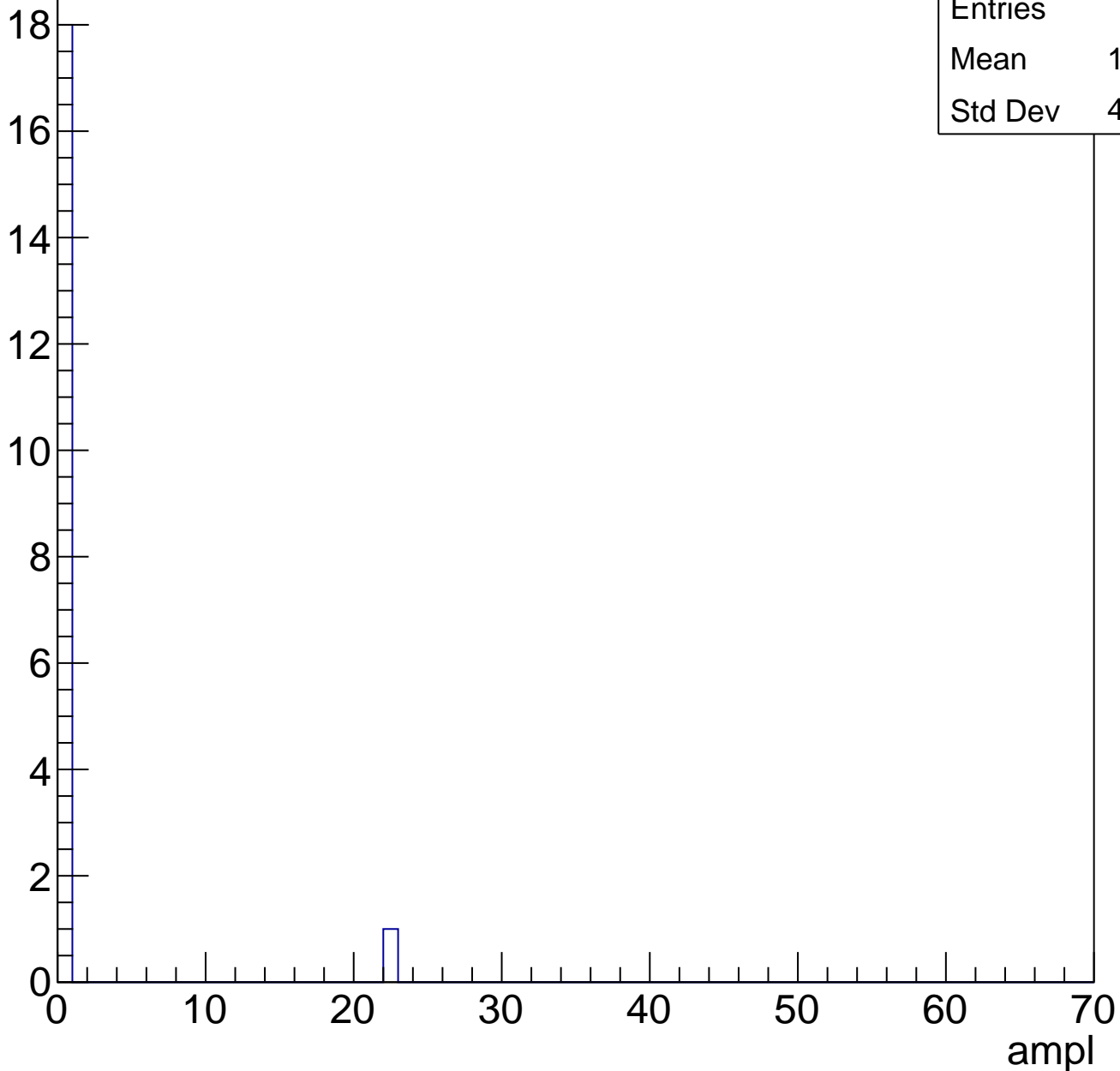




# B1L103S, U4-ch15, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



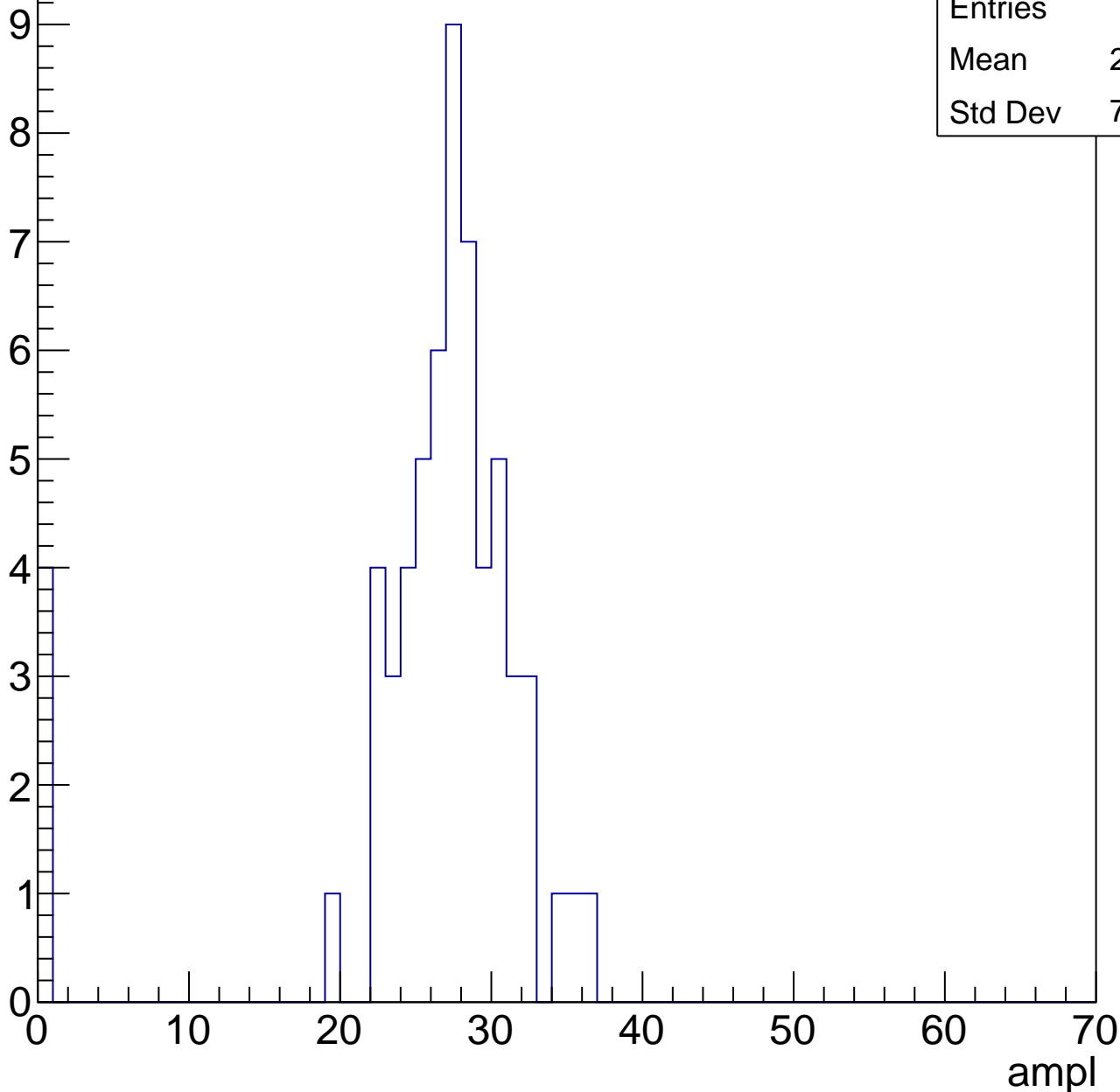
|         |       |
|---------|-------|
| Entries | 19    |
| Mean    | 1.158 |
| Std Dev | 4.913 |

# B1L103S, U4-ch16, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 61    |
| Mean    | 25.44 |
| Std Dev | 7.495 |



# B1L103S, U4-ch16, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 88    |
| Mean    | 29.18 |
| Std Dev | 11.49 |

Entry

10

8

6

4

2

0

0

10

20

30

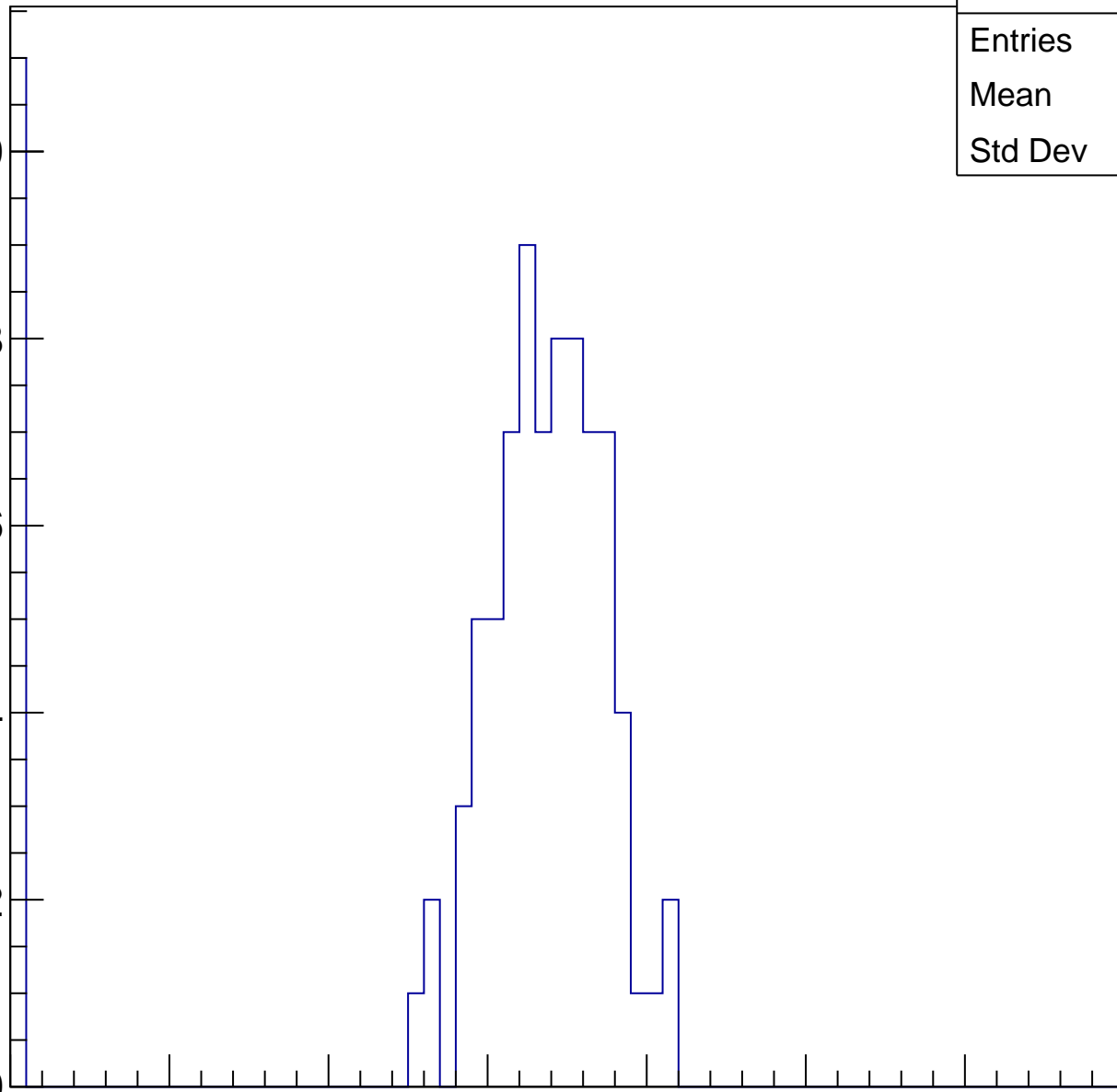
40

50

60

70

ampl

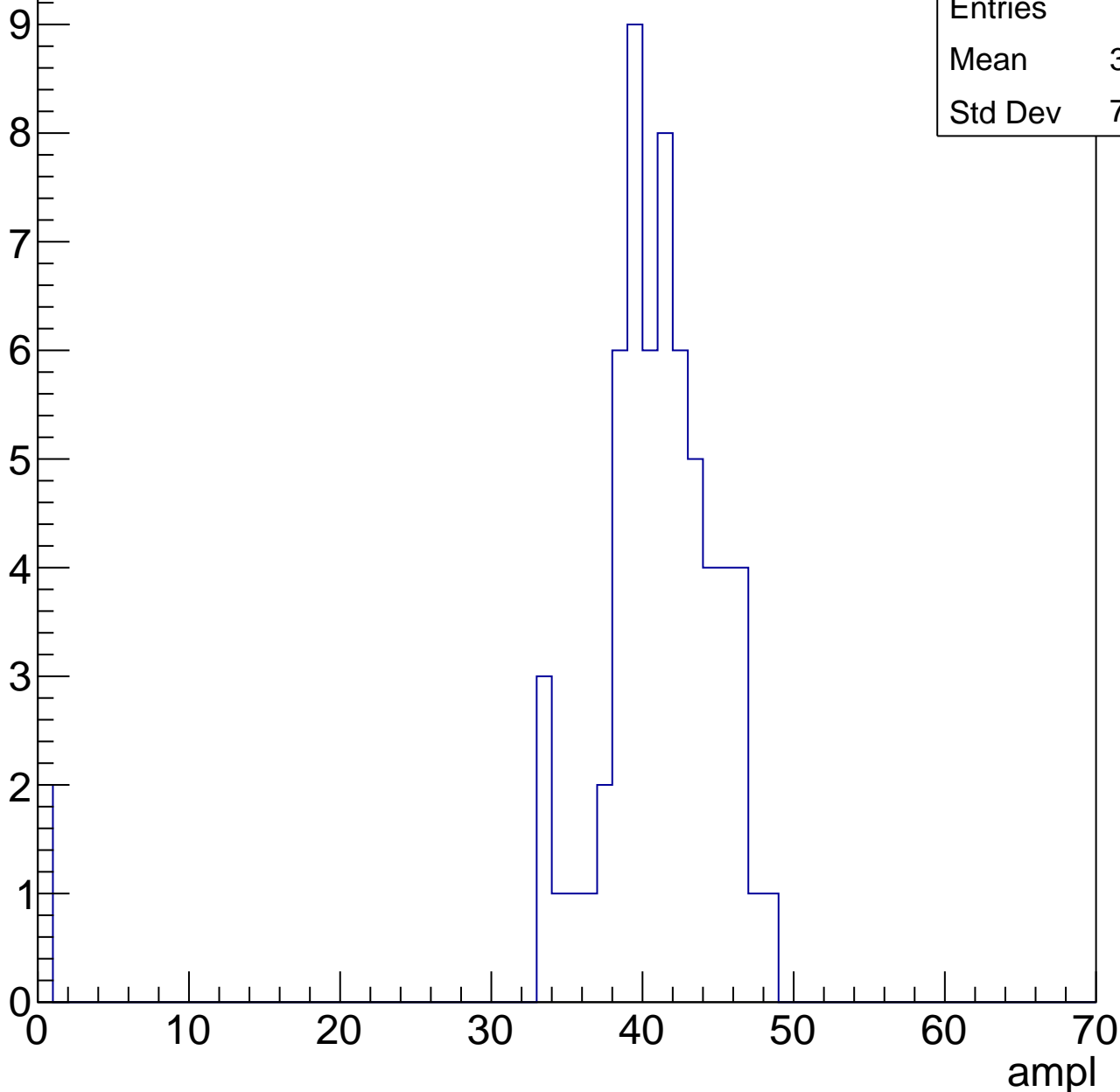


# B1L103S, U4-ch16, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 64    |
| Mean    | 39.48 |
| Std Dev | 7.862 |

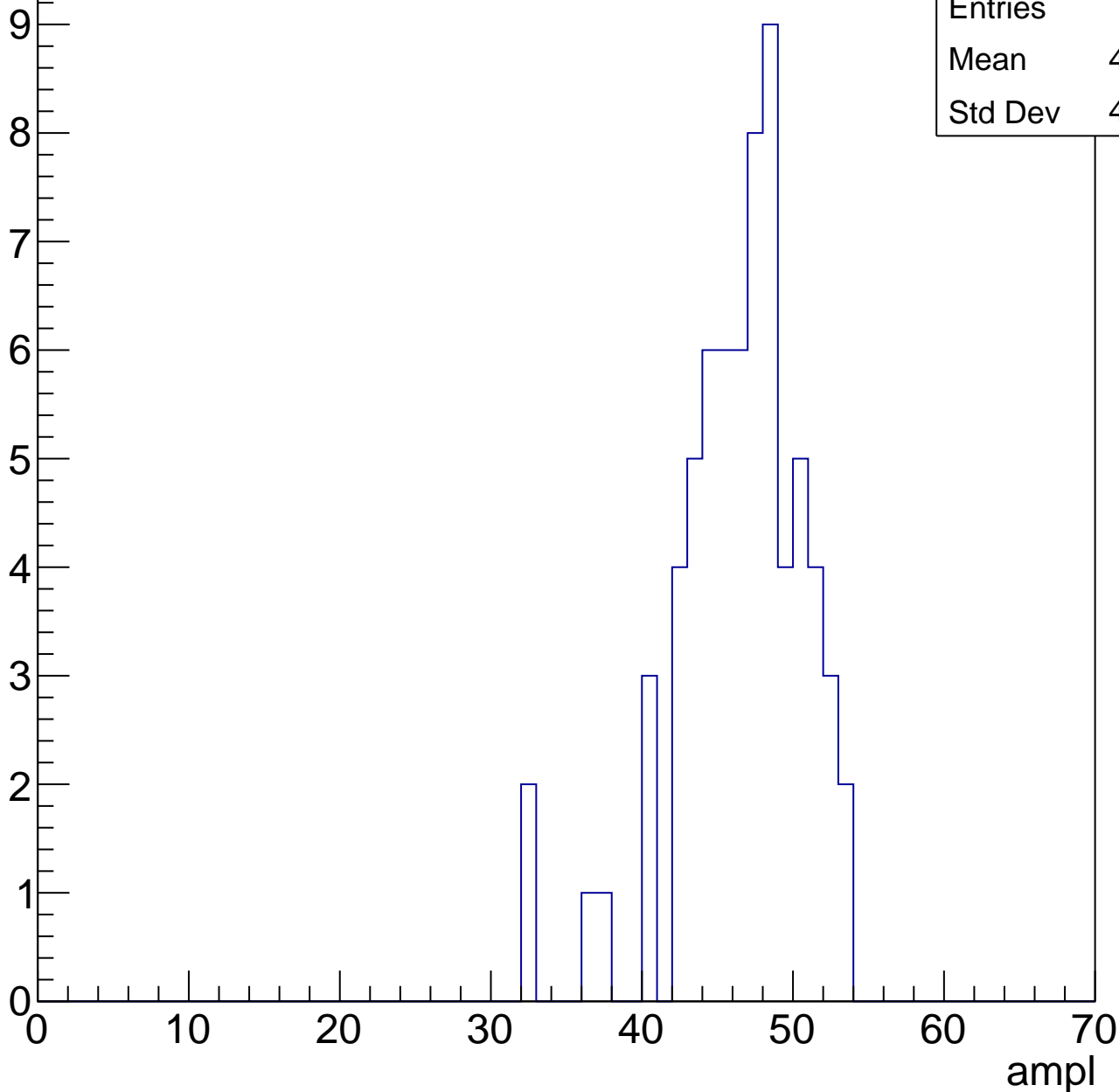


# B1L103S, U4-ch16, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

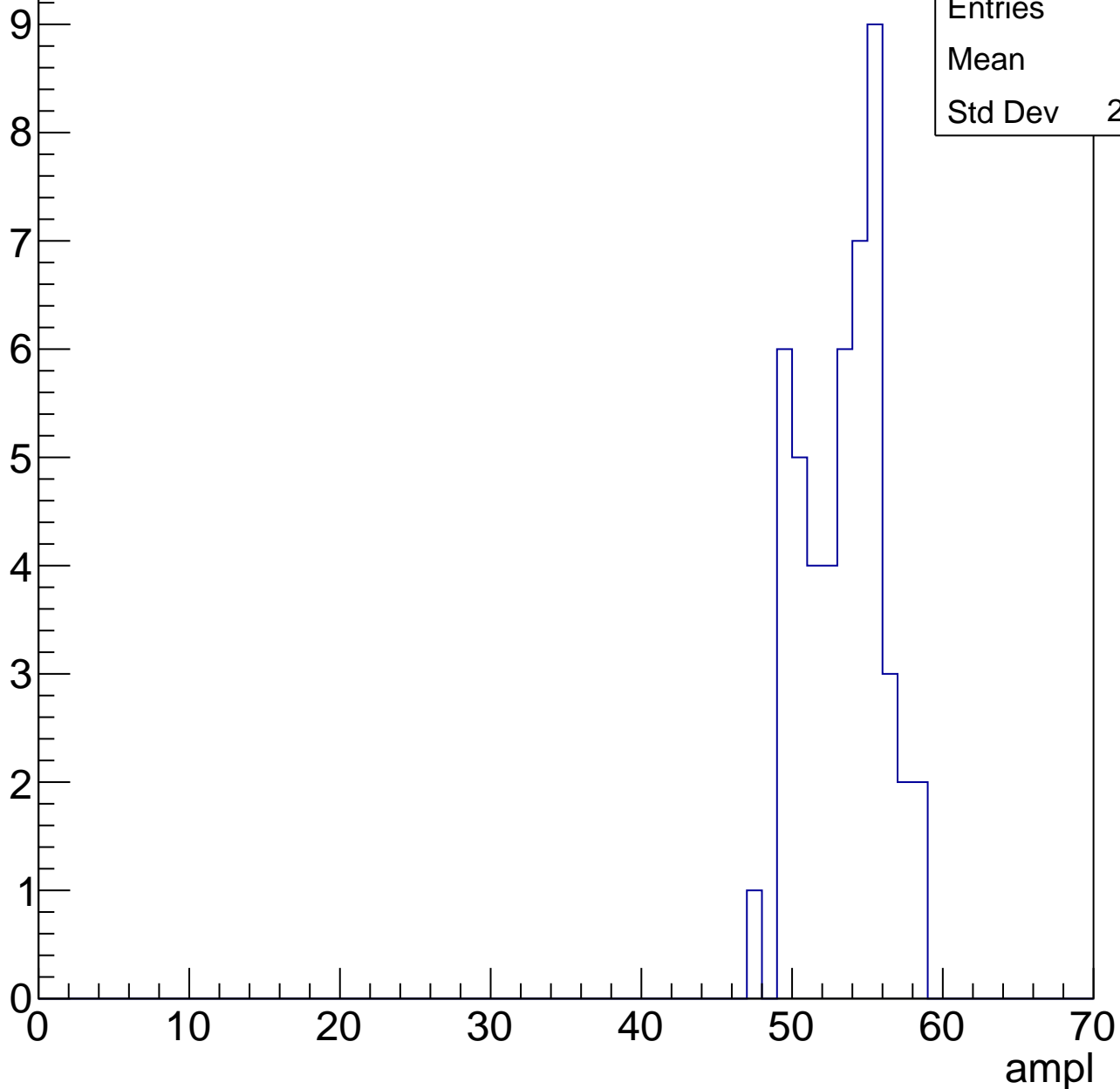
|         |       |
|---------|-------|
| Entries | 69    |
| Mean    | 45.94 |
| Std Dev | 4.317 |



# B1L103S, U4-ch16, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

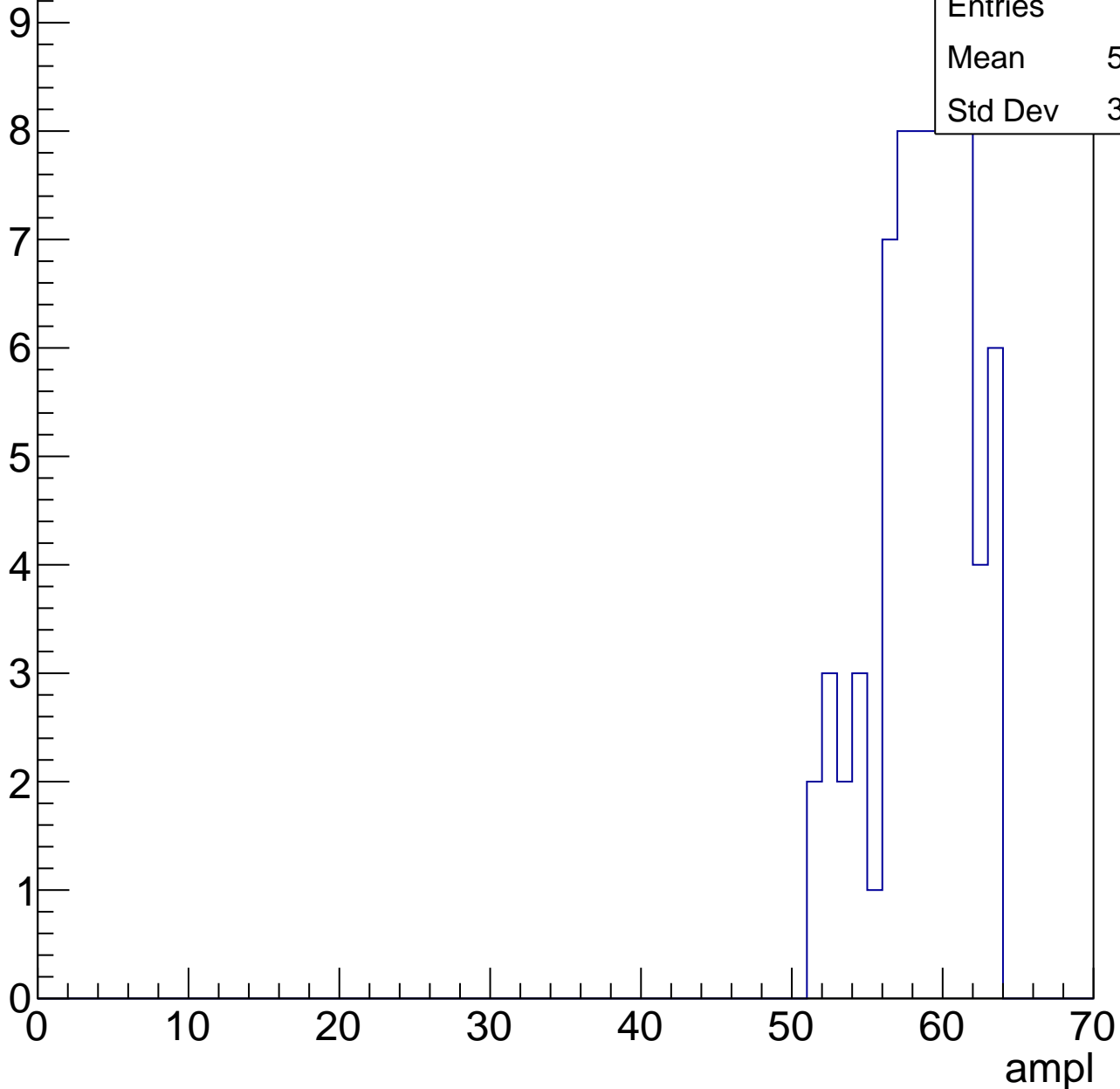


# B1L103S, U4-ch16, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

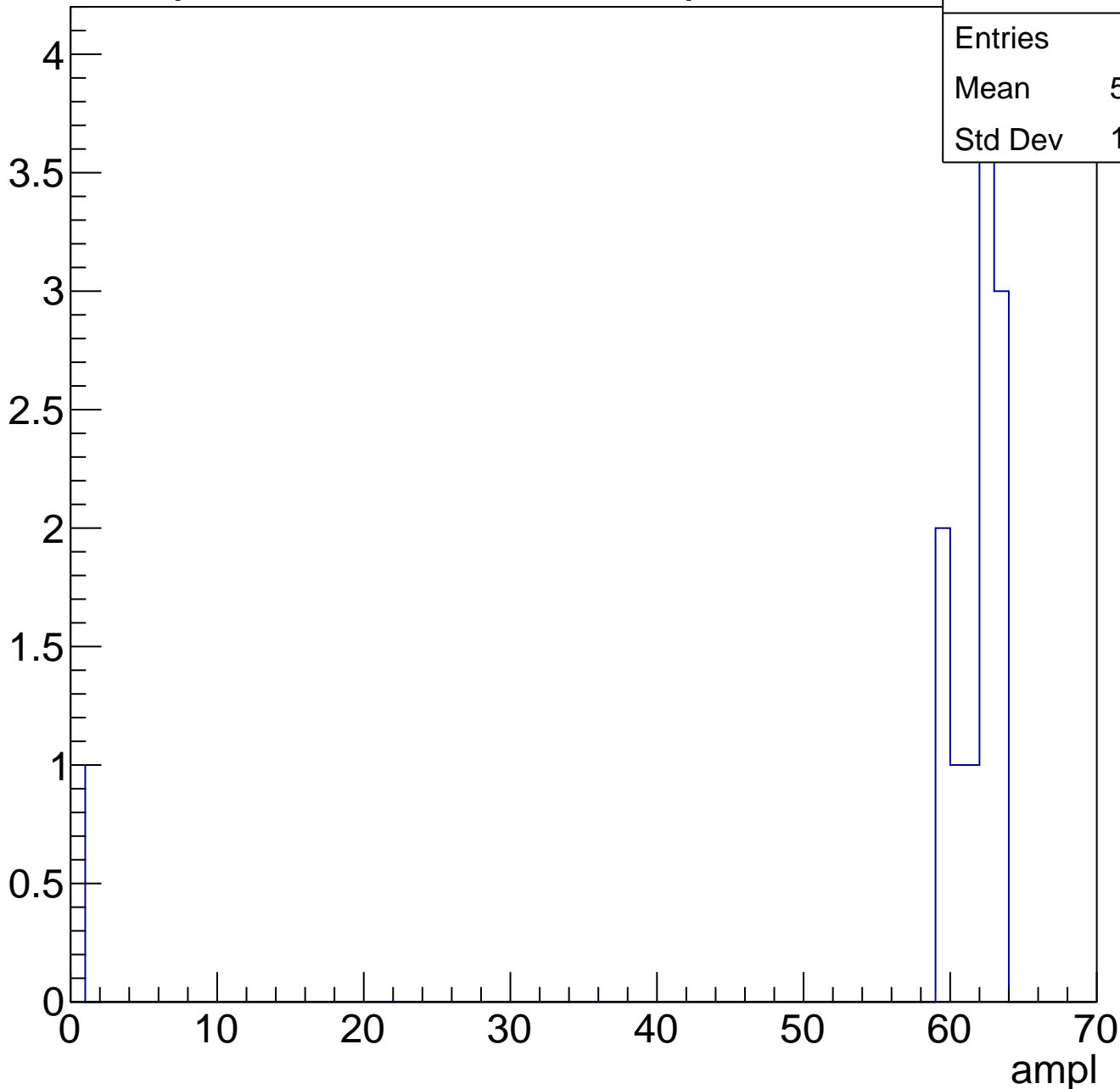
|         |       |
|---------|-------|
| Entries | 70    |
| Mean    | 58.29 |
| Std Dev | 3.122 |



# B1L103S, U4-ch16, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



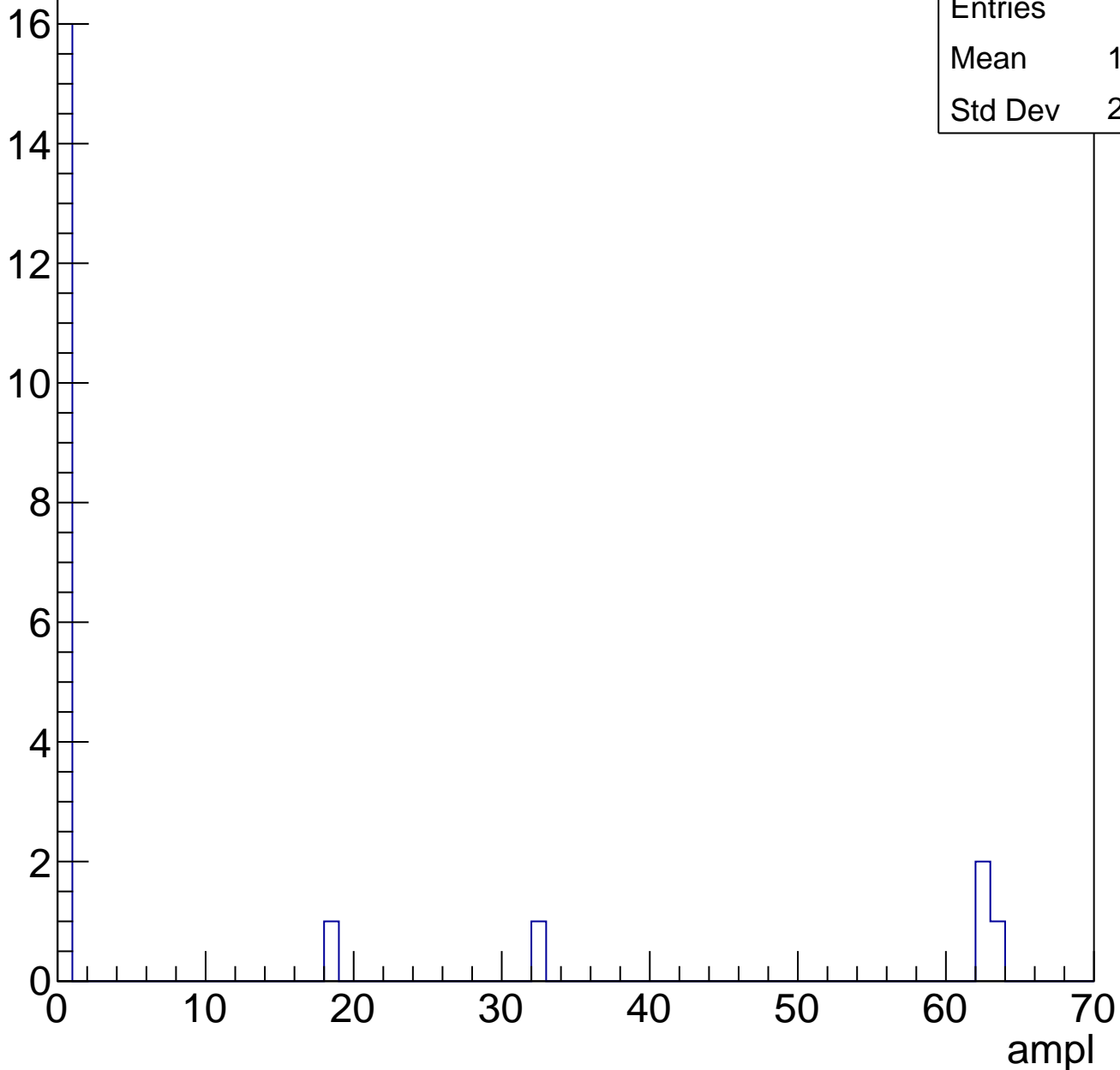


# B1L103S, U4-ch16, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 21    |
| Mean    | 11.29 |
| Std Dev | 22.18 |

Entry

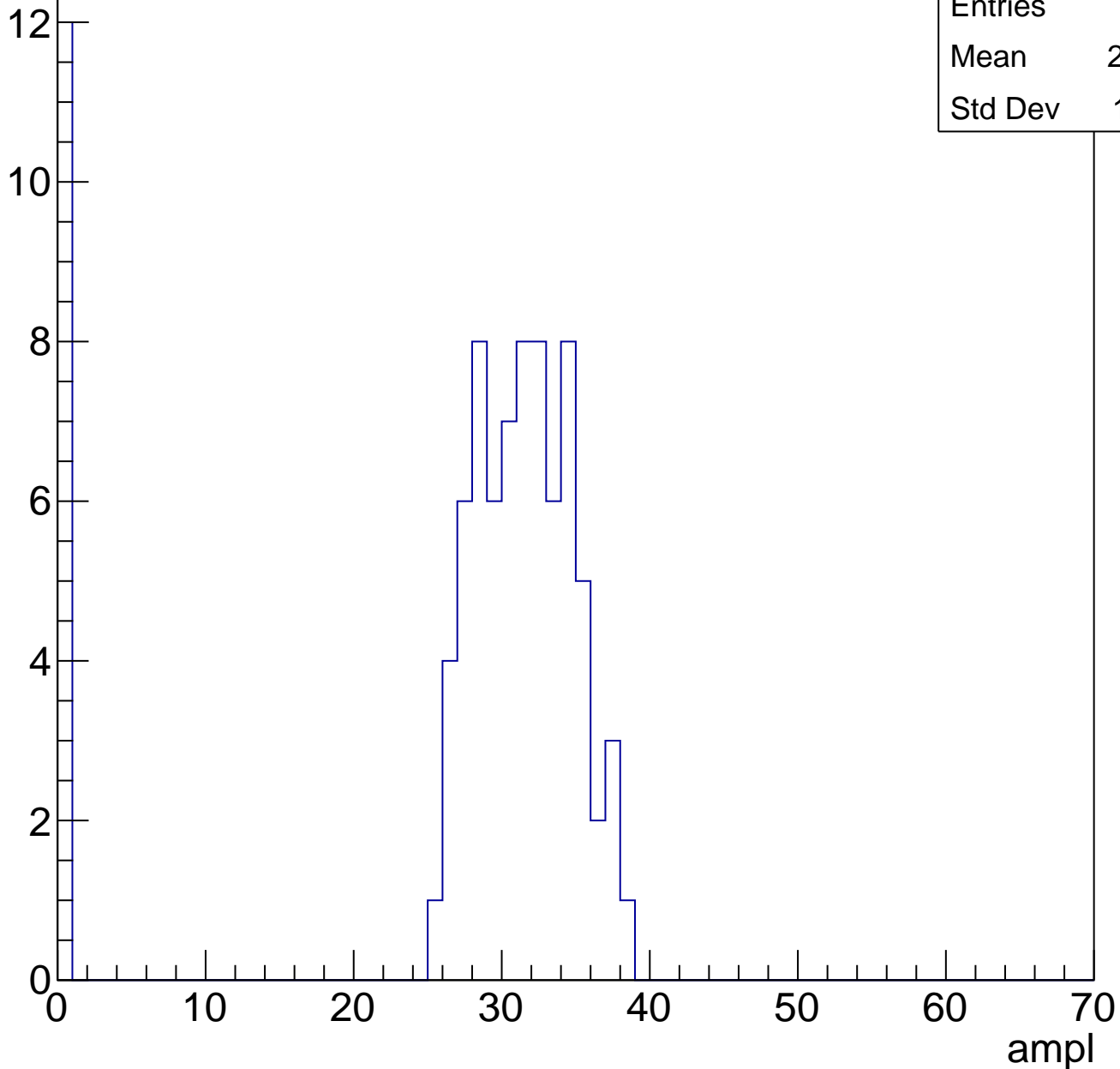


# B1L103S, U4-ch17, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 85    |
| Mean    | 26.69 |
| Std Dev | 11.21 |

Entry

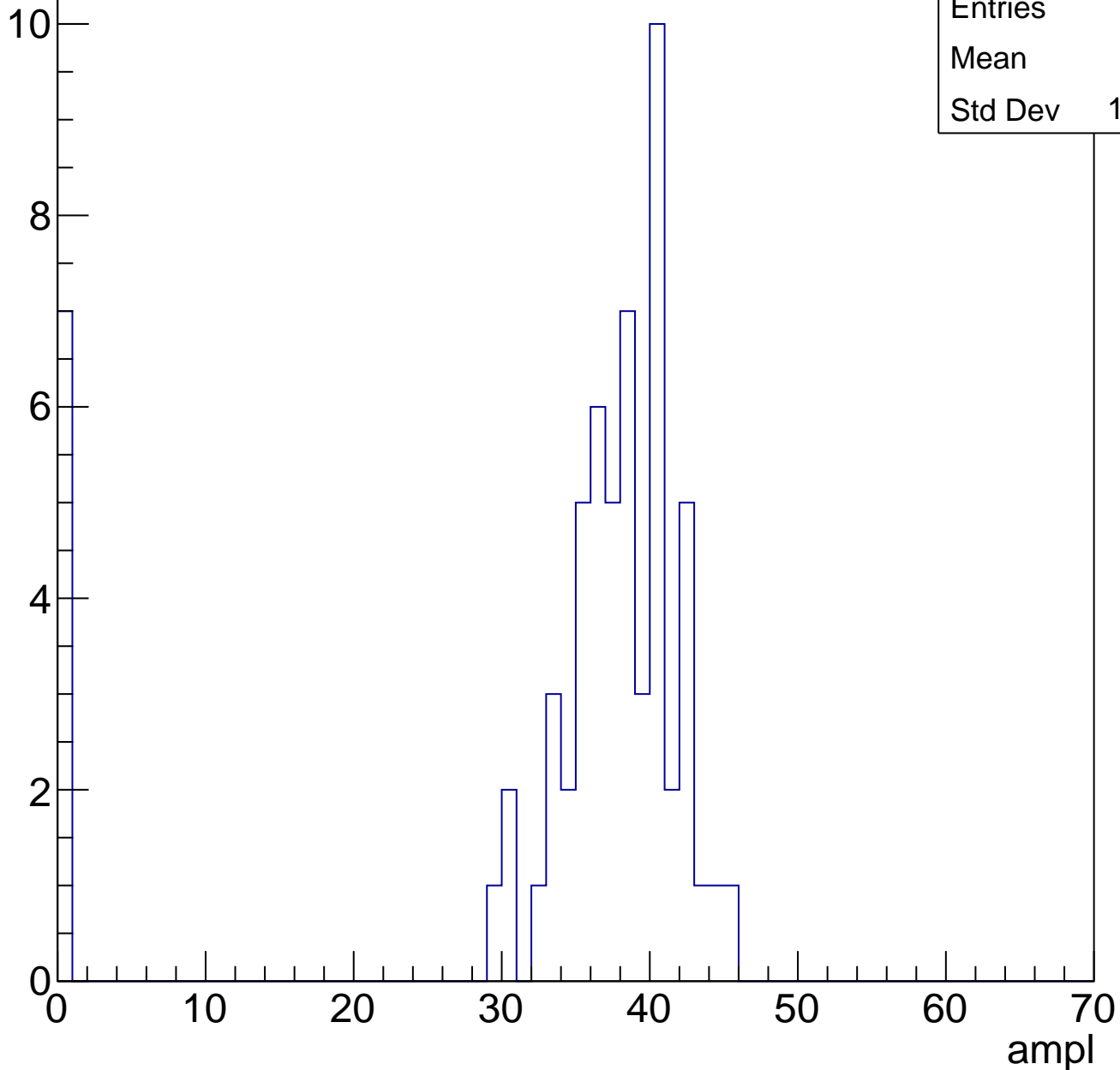


# B1L103S, U4-ch17, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 62    |
| Mean    | 33.4  |
| Std Dev | 12.36 |

Entry

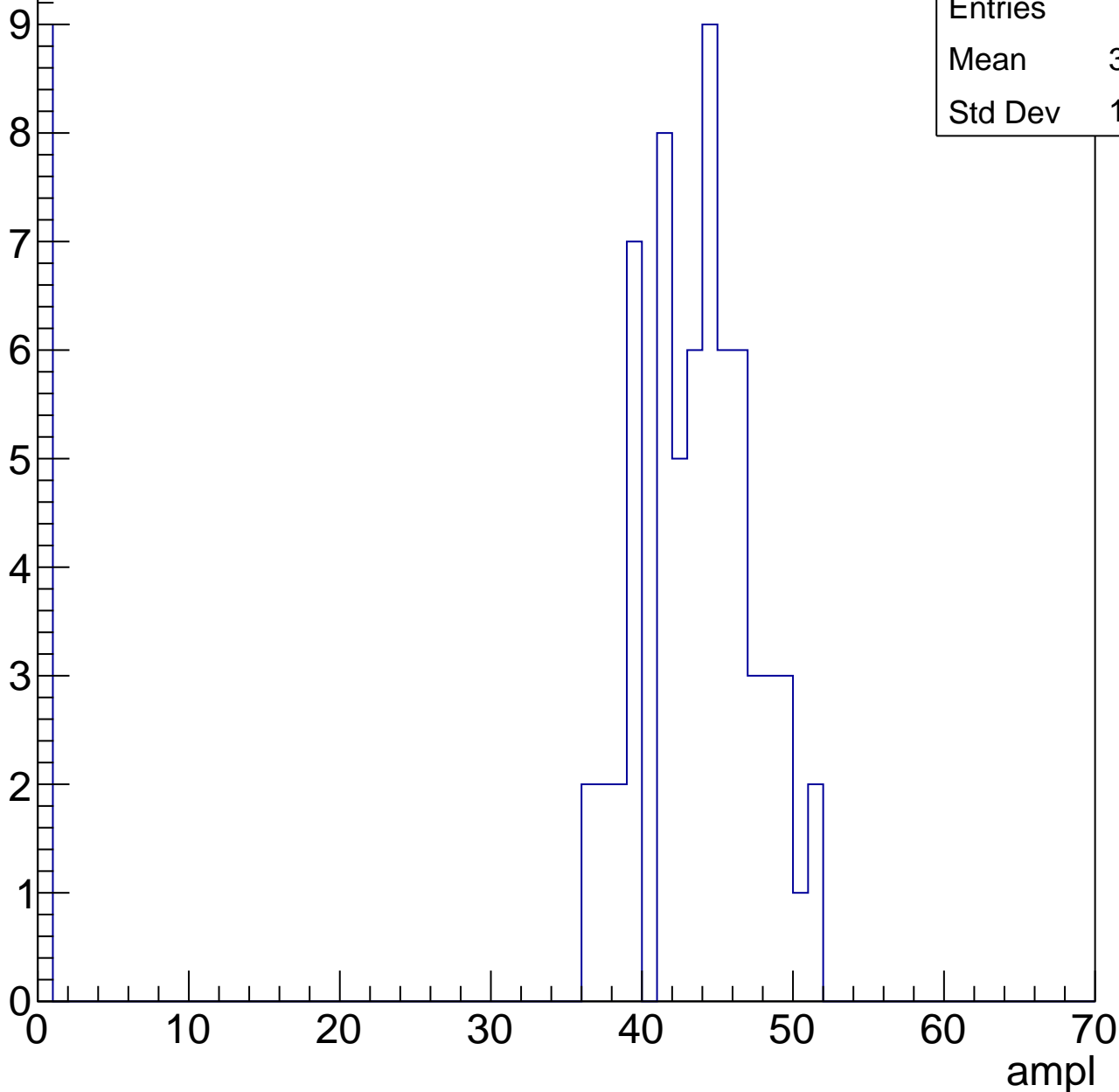


# B1L103S, U4-ch17, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

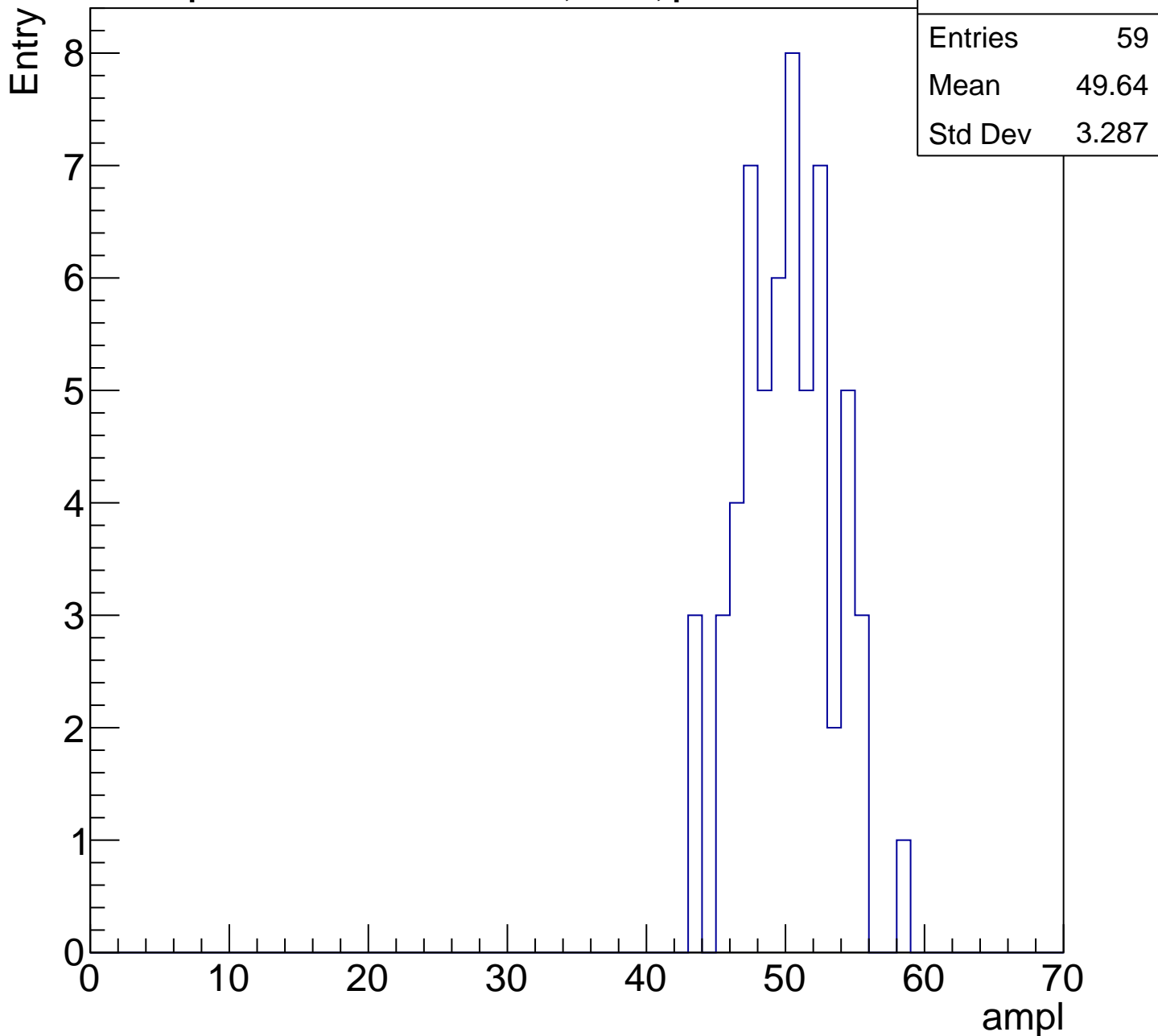
Entry

|         |       |
|---------|-------|
| Entries | 74    |
| Mean    | 38.07 |
| Std Dev | 14.57 |



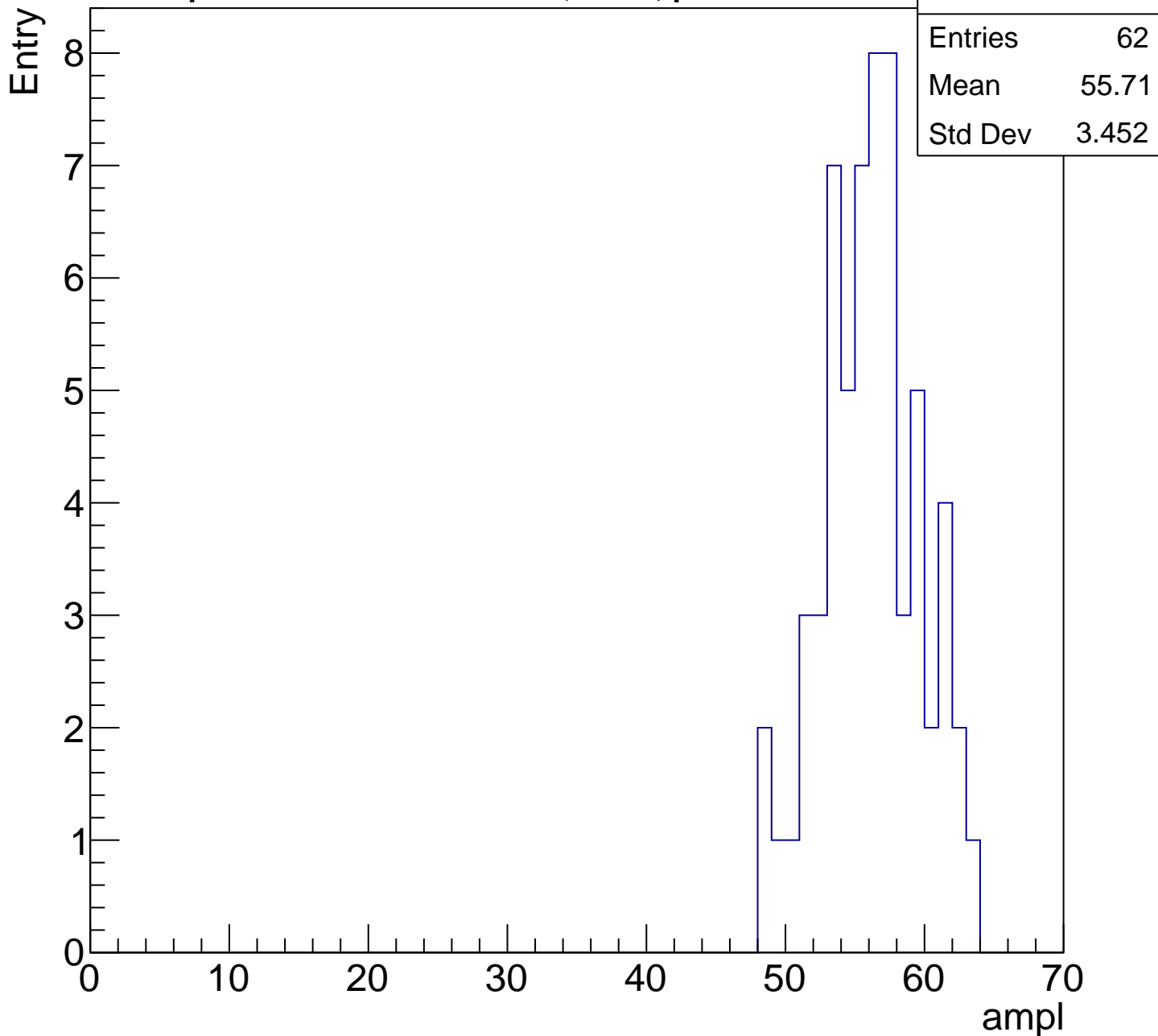
# B1L103S, U4-ch17, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2



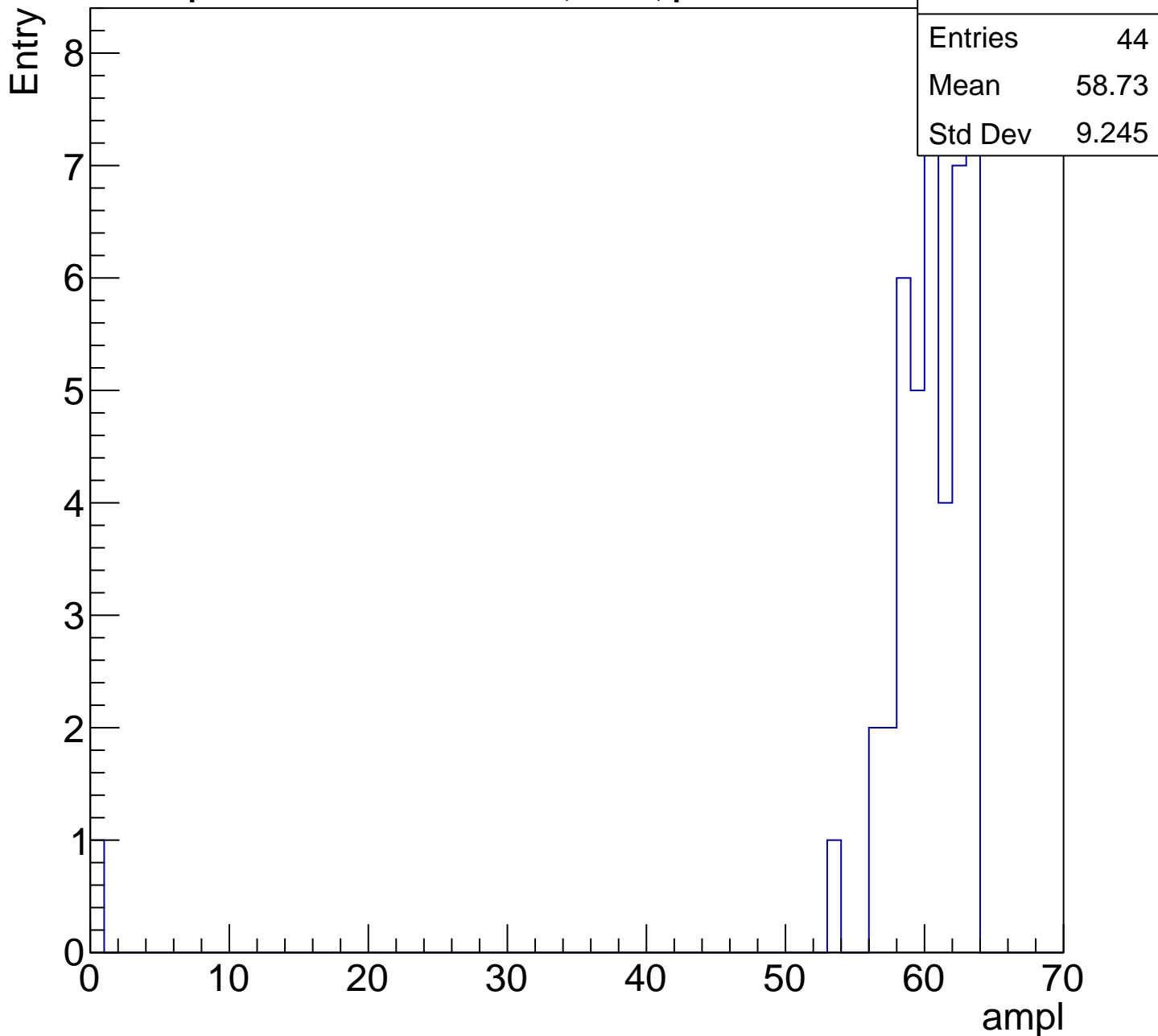
# B1L103S, U4-ch17, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2



# B1L103S, U4-ch17, adc5

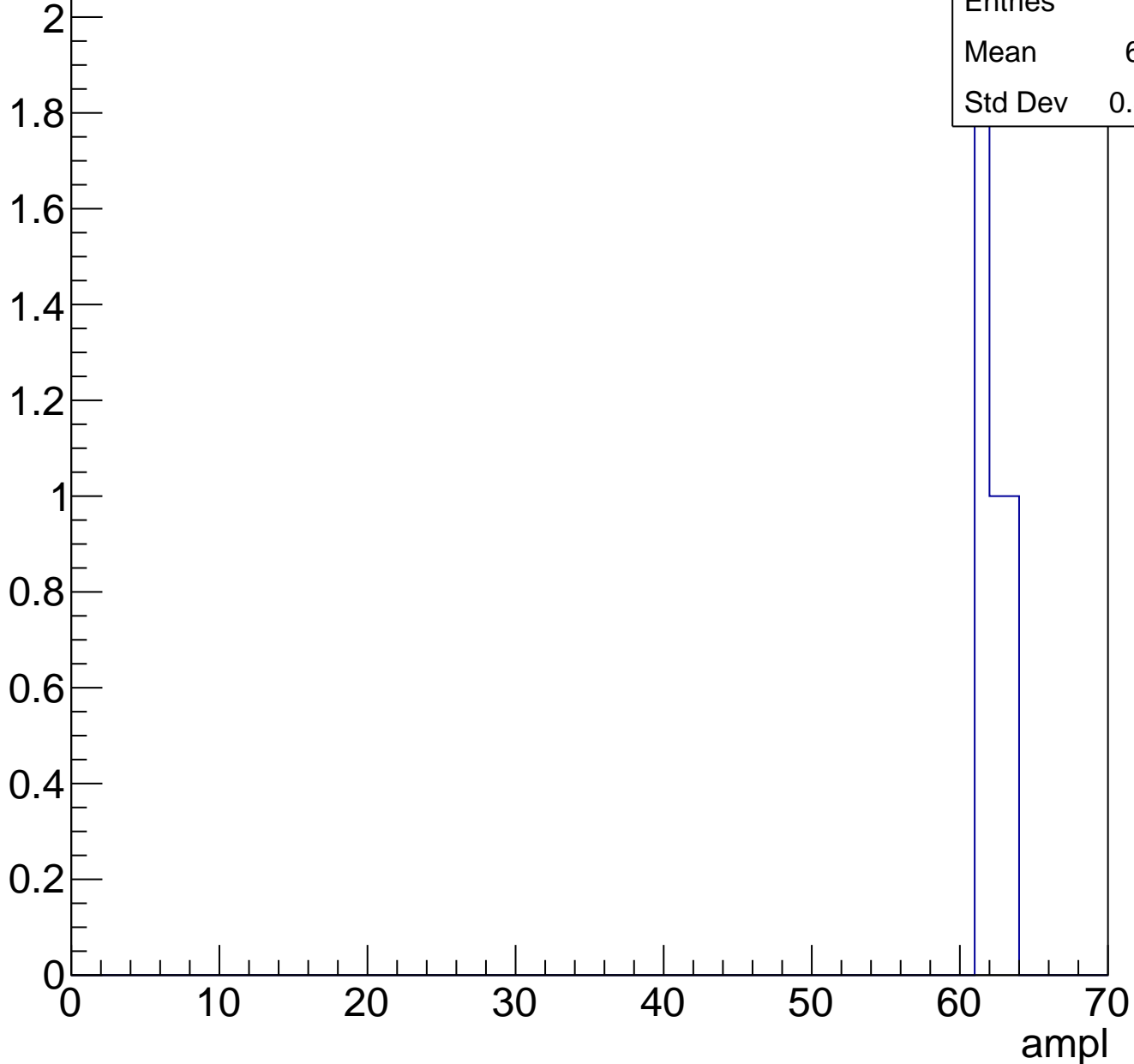
calib\_packv5\_041523\_1651.root, FC#0, port C2



# B1L103S, U4-ch17, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



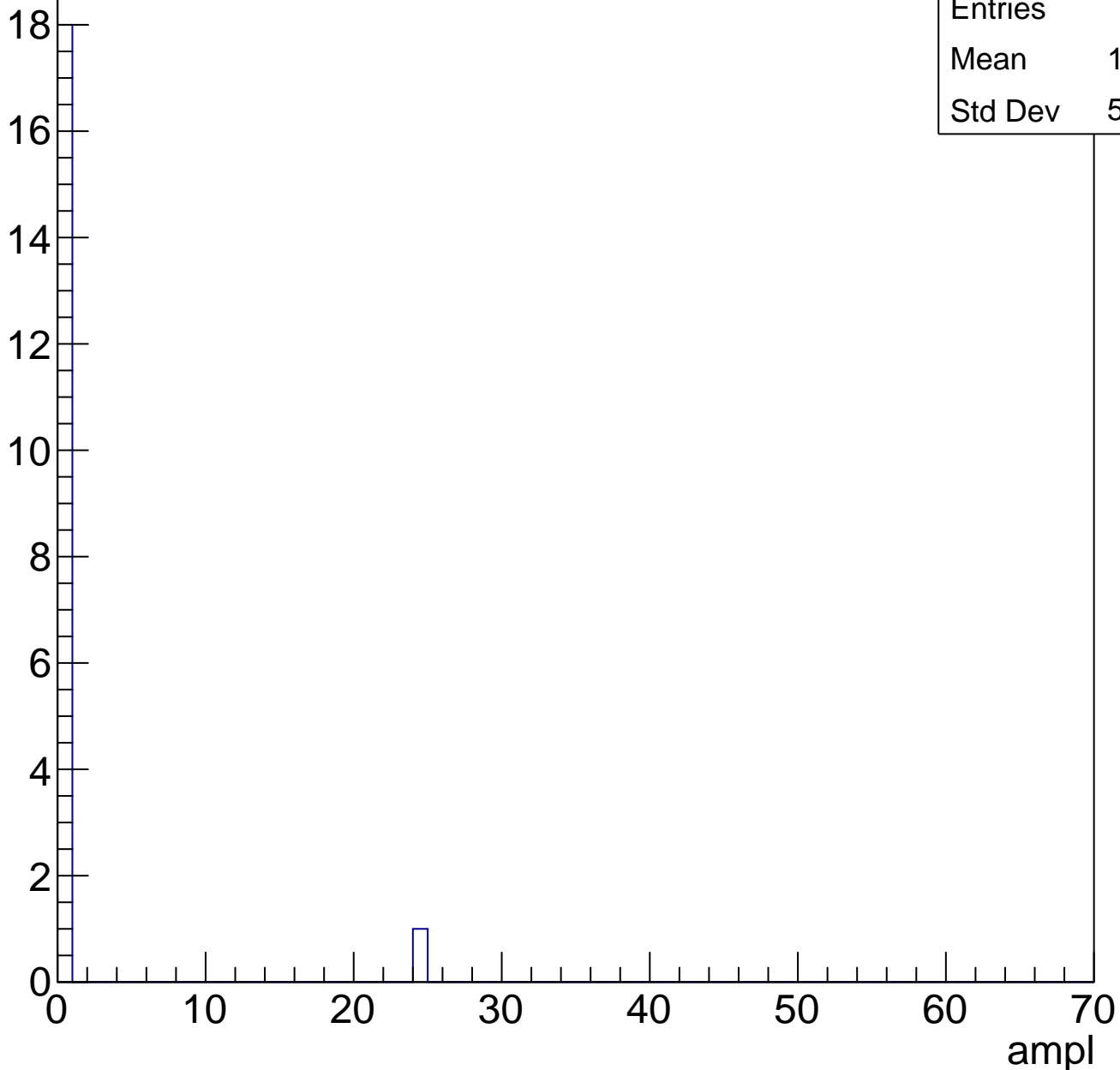


# B1L103S, U4-ch17, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 19    |
| Mean    | 1.263 |
| Std Dev | 5.359 |

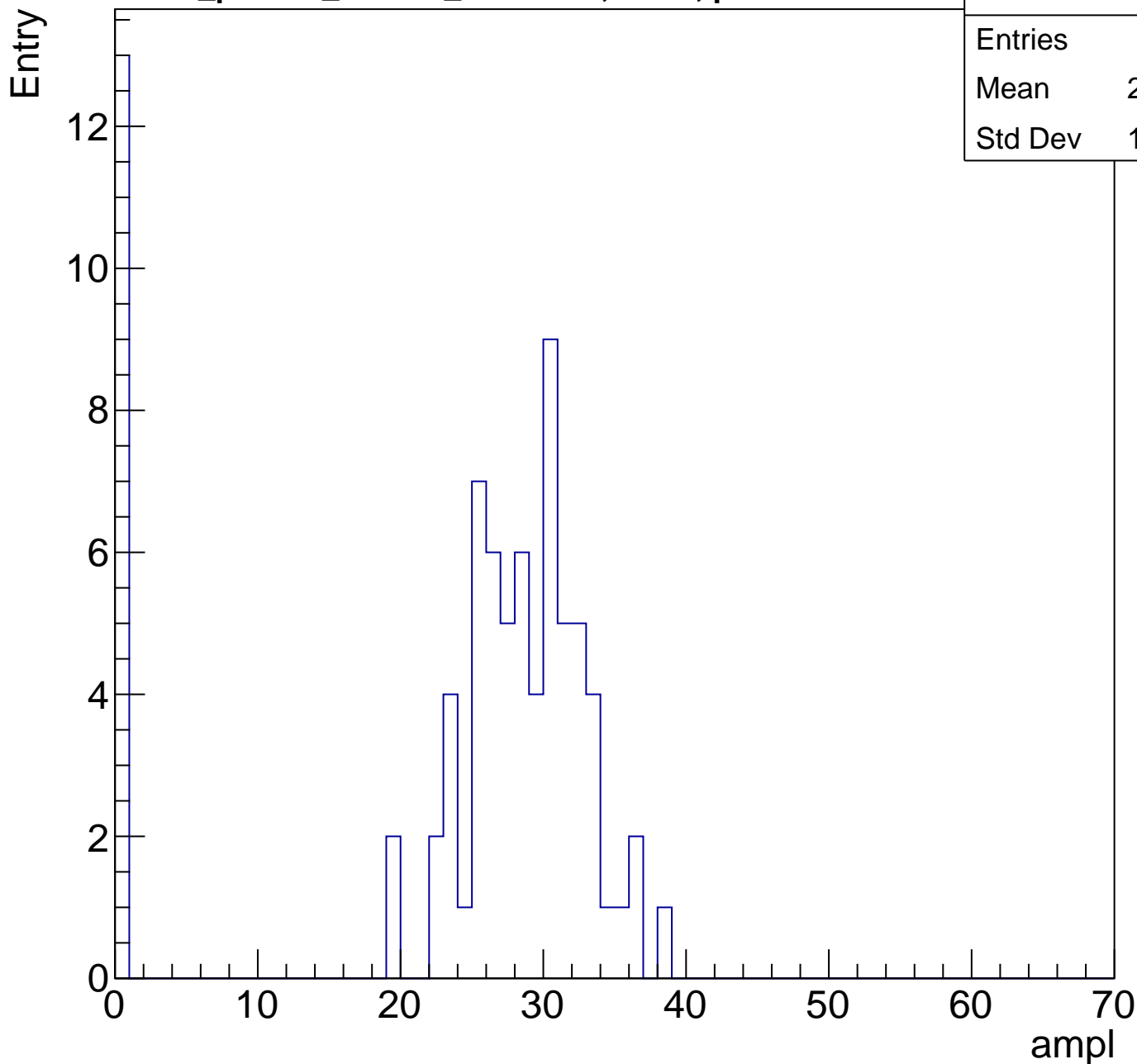
Entry



# B1L103S, U4-ch18, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 78    |
| Mean    | 23.64 |
| Std Dev | 11.17 |

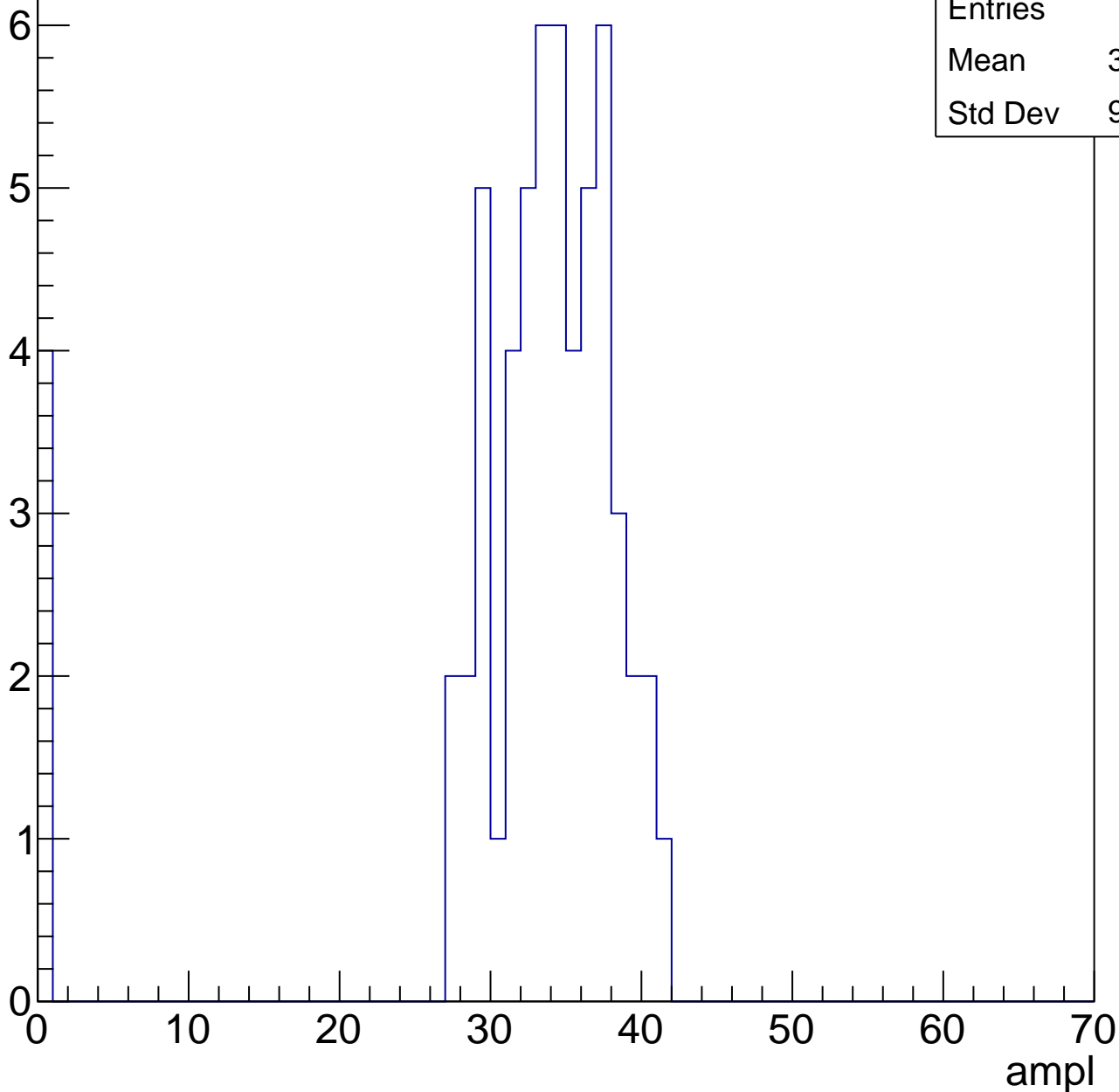


# B1L103S, U4-ch18, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 58    |
| Mean    | 31.48 |
| Std Dev | 9.216 |



# B1L103S, U4-ch18, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 86    |
| Mean    | 35.37 |
| Std Dev | 14.01 |

Entry

10

8

6

4

2

0

0

10

20

30

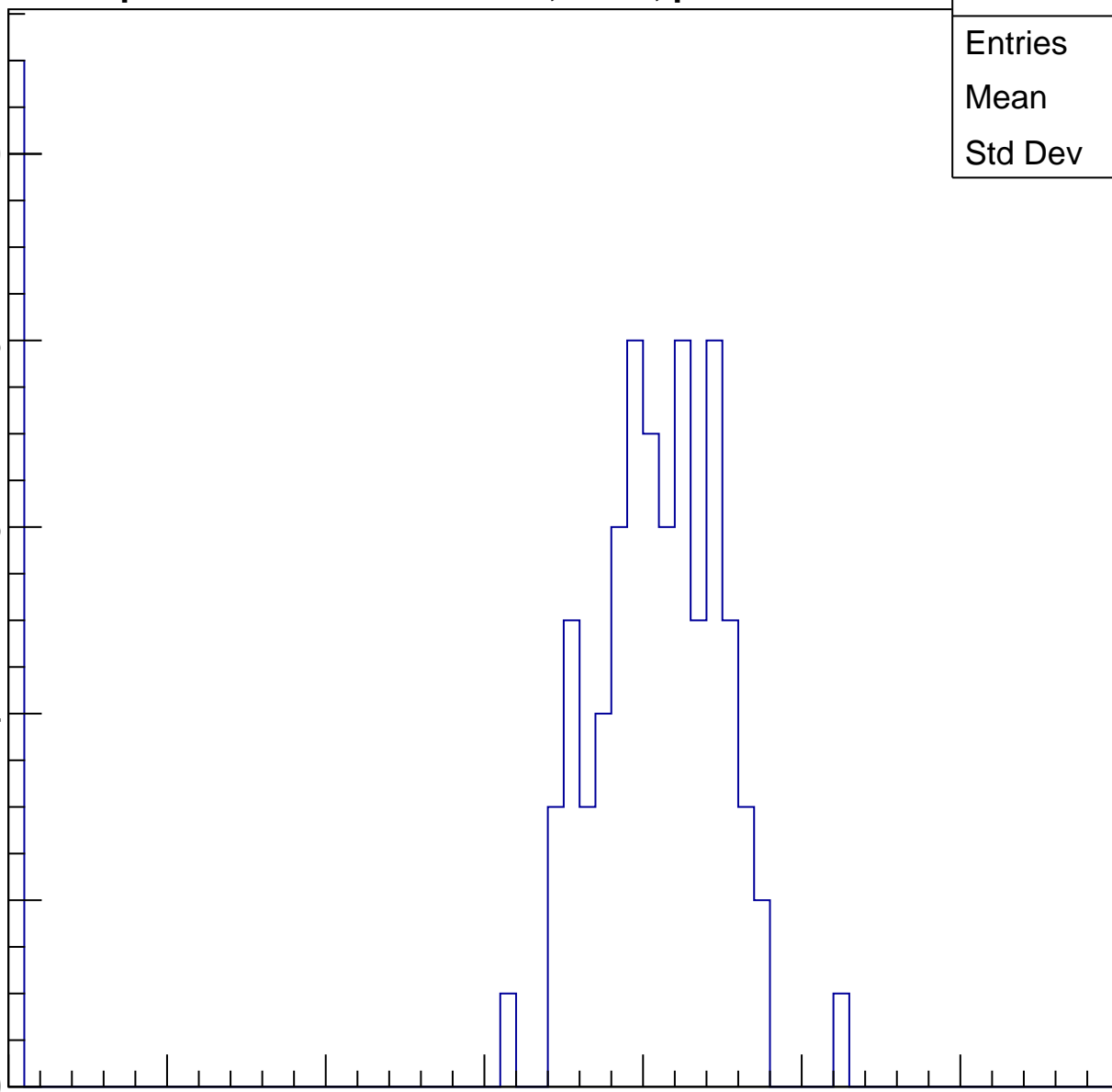
40

50

60

70

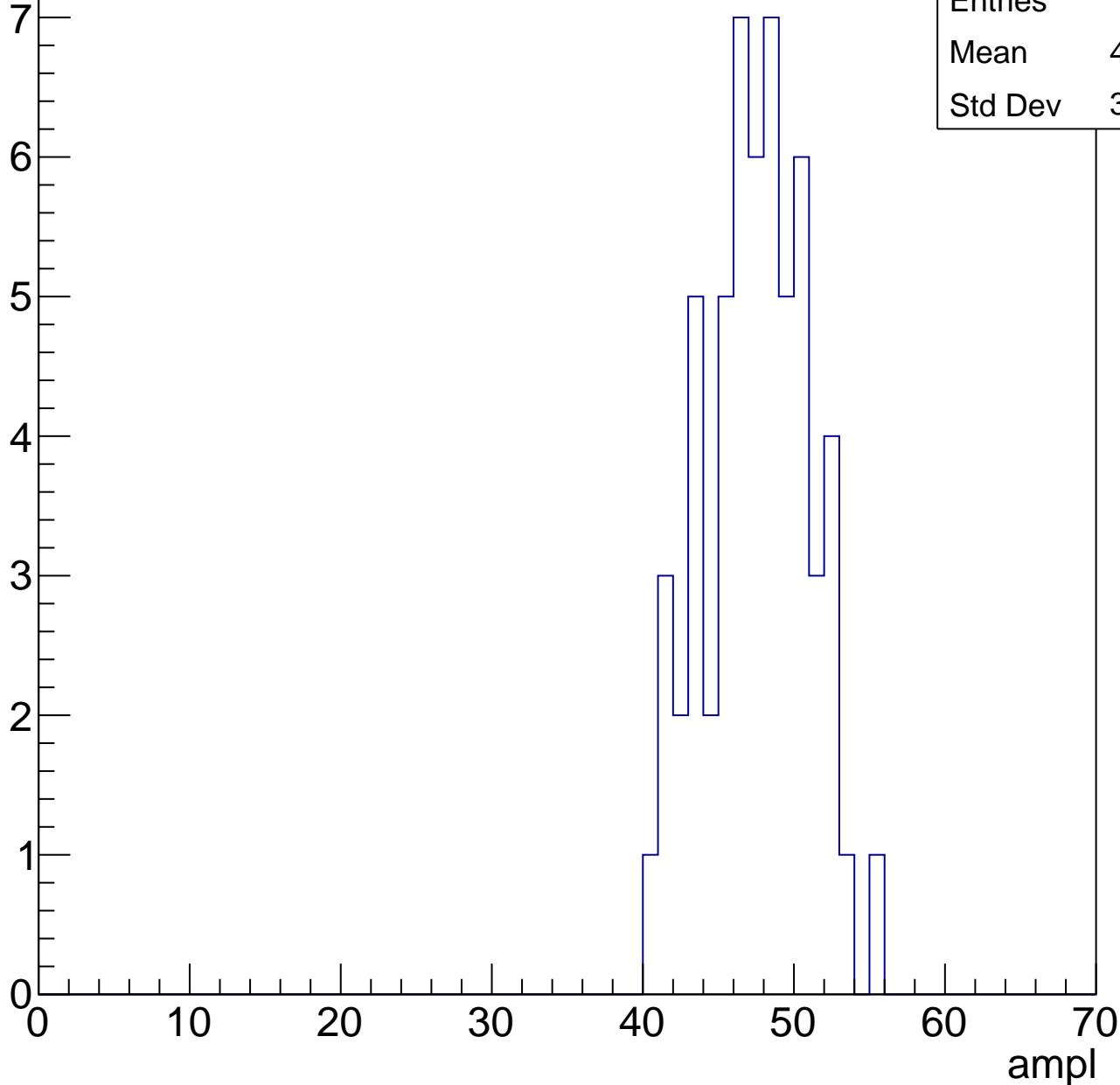
ampl



# B1L103S, U4-ch18, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

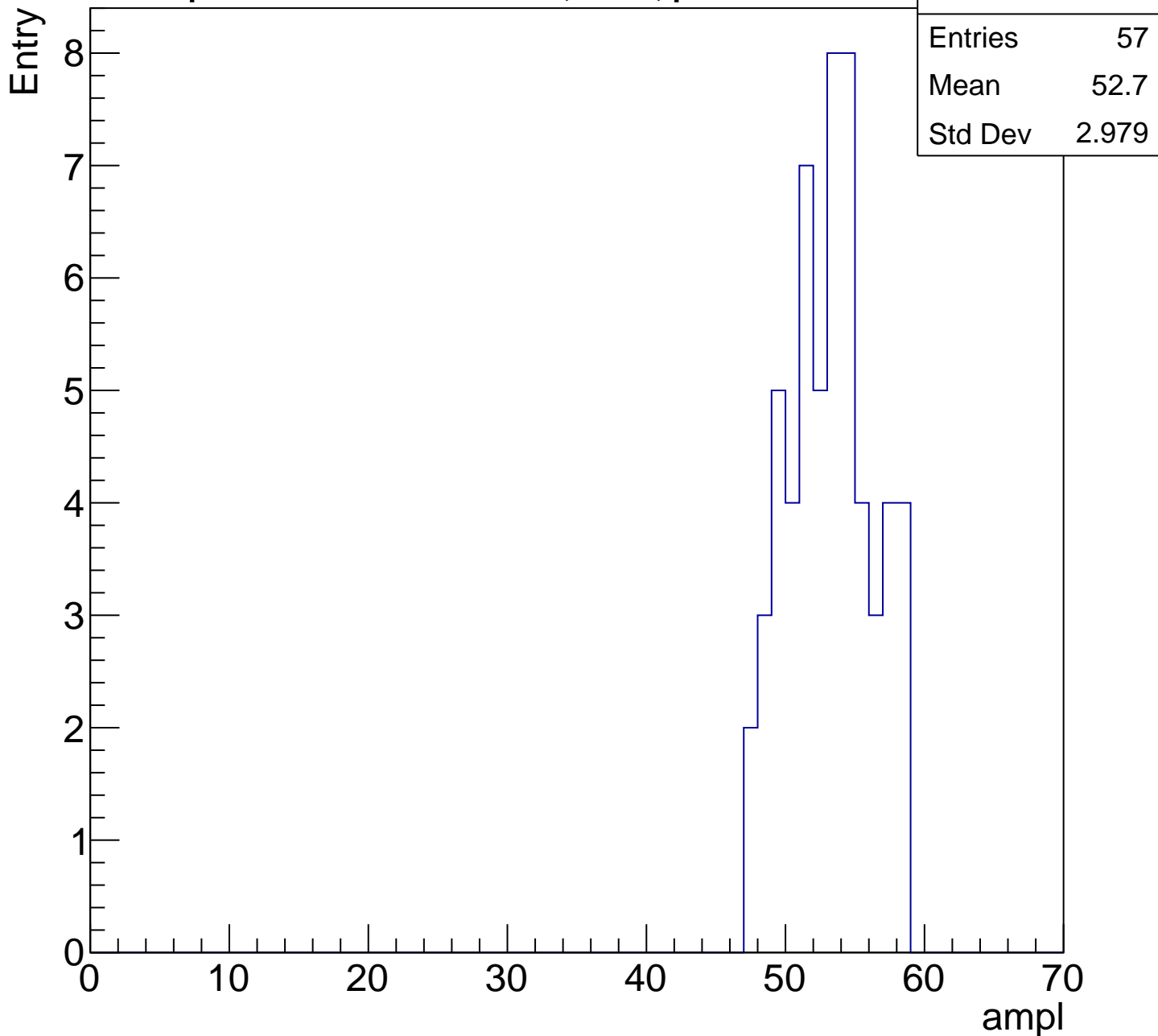
Entry



|         |       |
|---------|-------|
| Entries | 58    |
| Mean    | 47.05 |
| Std Dev | 3.375 |

# B1L103S, U4-ch18, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

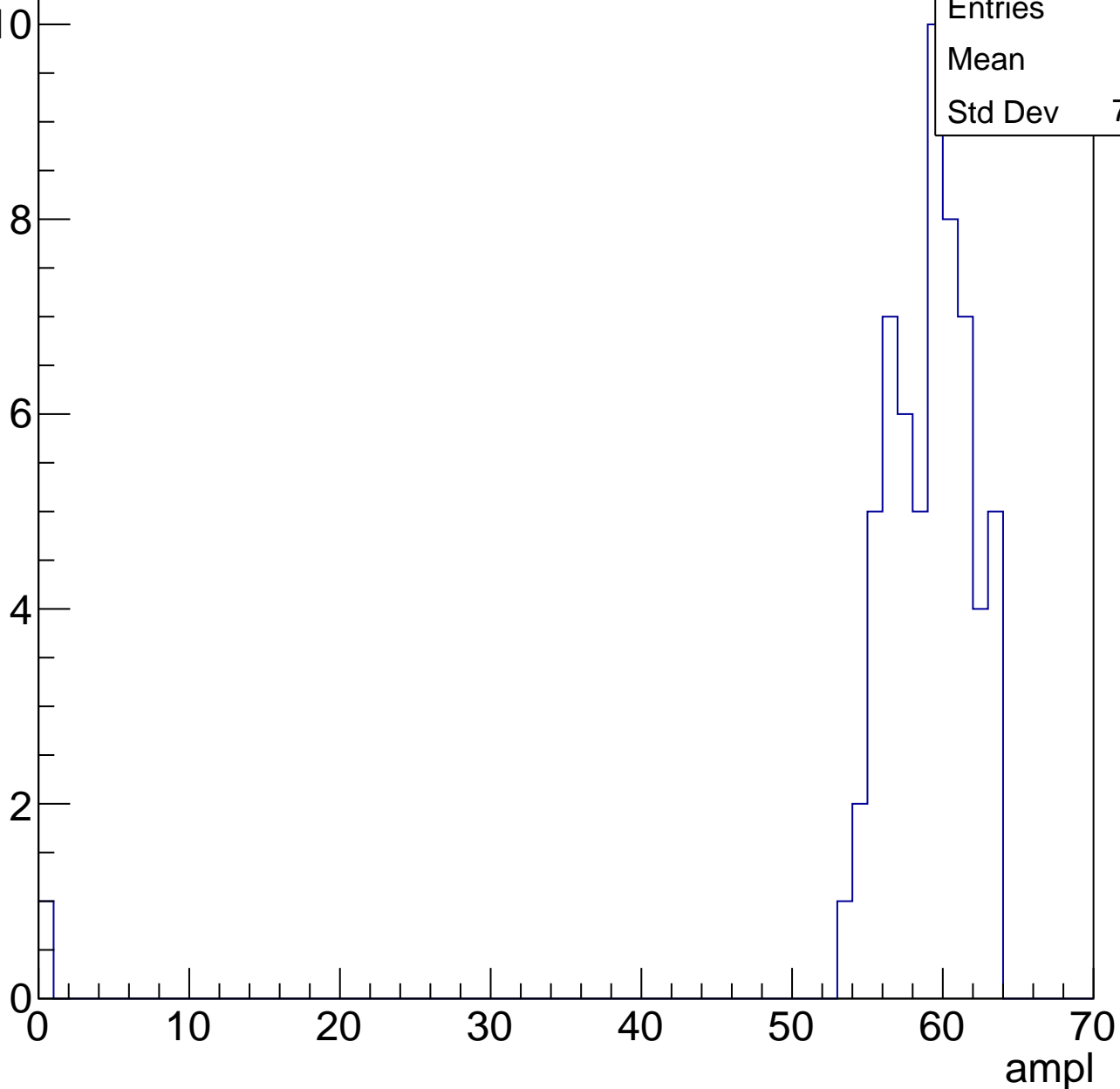


# B1L103S, U4-ch18, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 61    |
| Mean    | 57.7  |
| Std Dev | 7.881 |

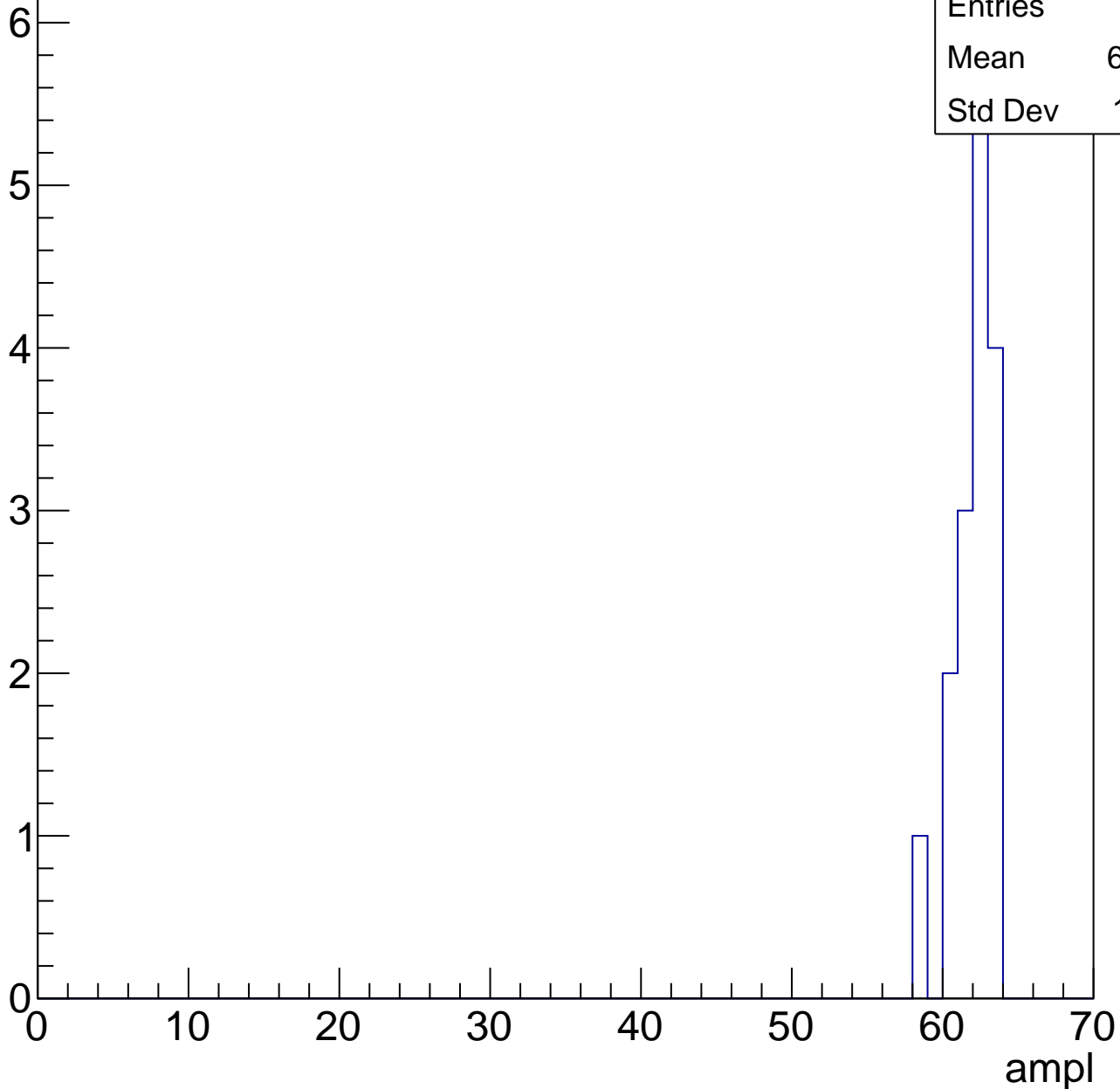


# B1L103S, U4-ch18, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 16    |
| Mean    | 61.56 |
| Std Dev | 1.321 |





# B1L103S, U4-ch18, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

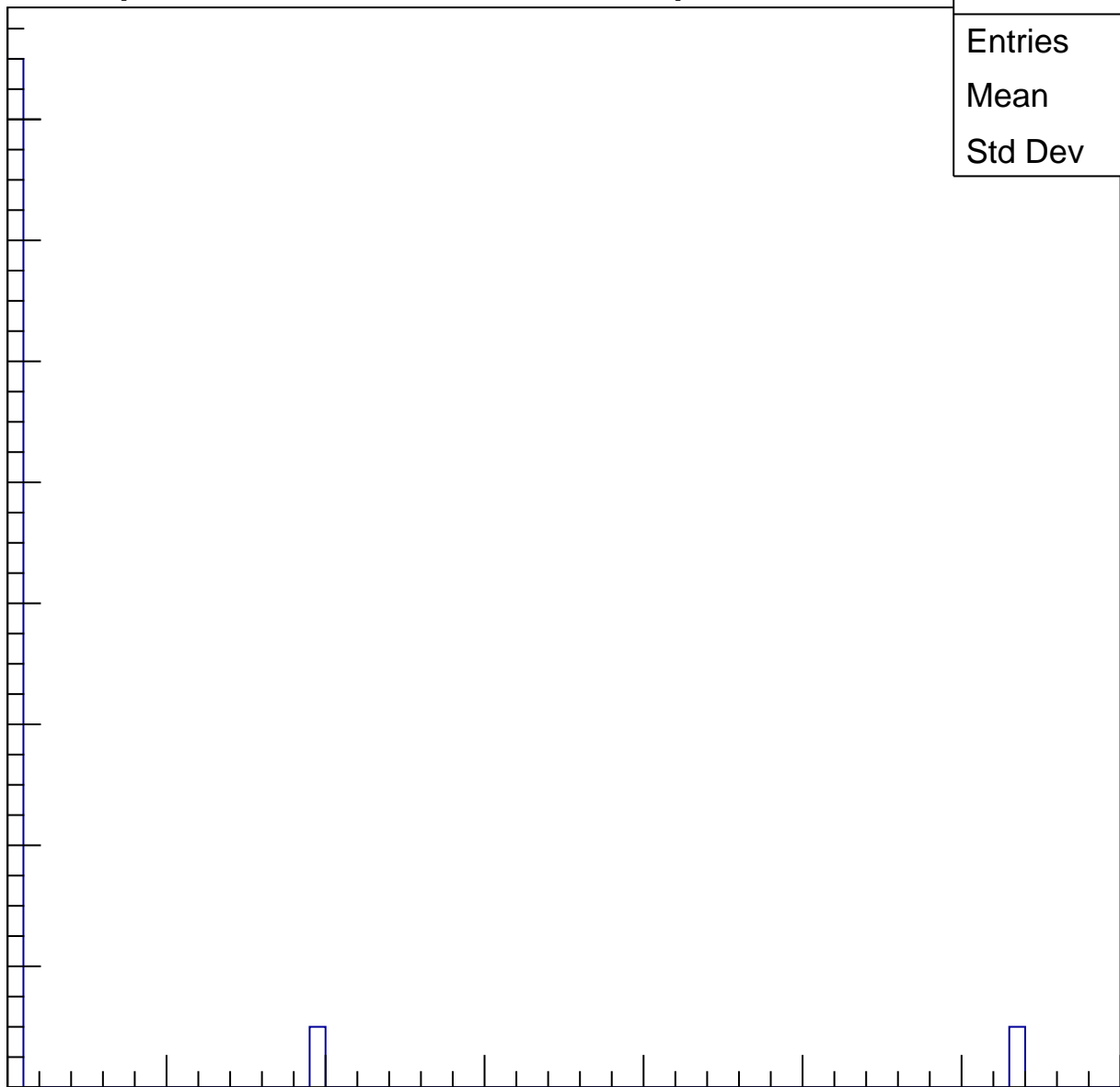
|         |       |
|---------|-------|
| Entries | 19    |
| Mean    | 4.316 |
| Std Dev | 14.47 |

Entry

16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

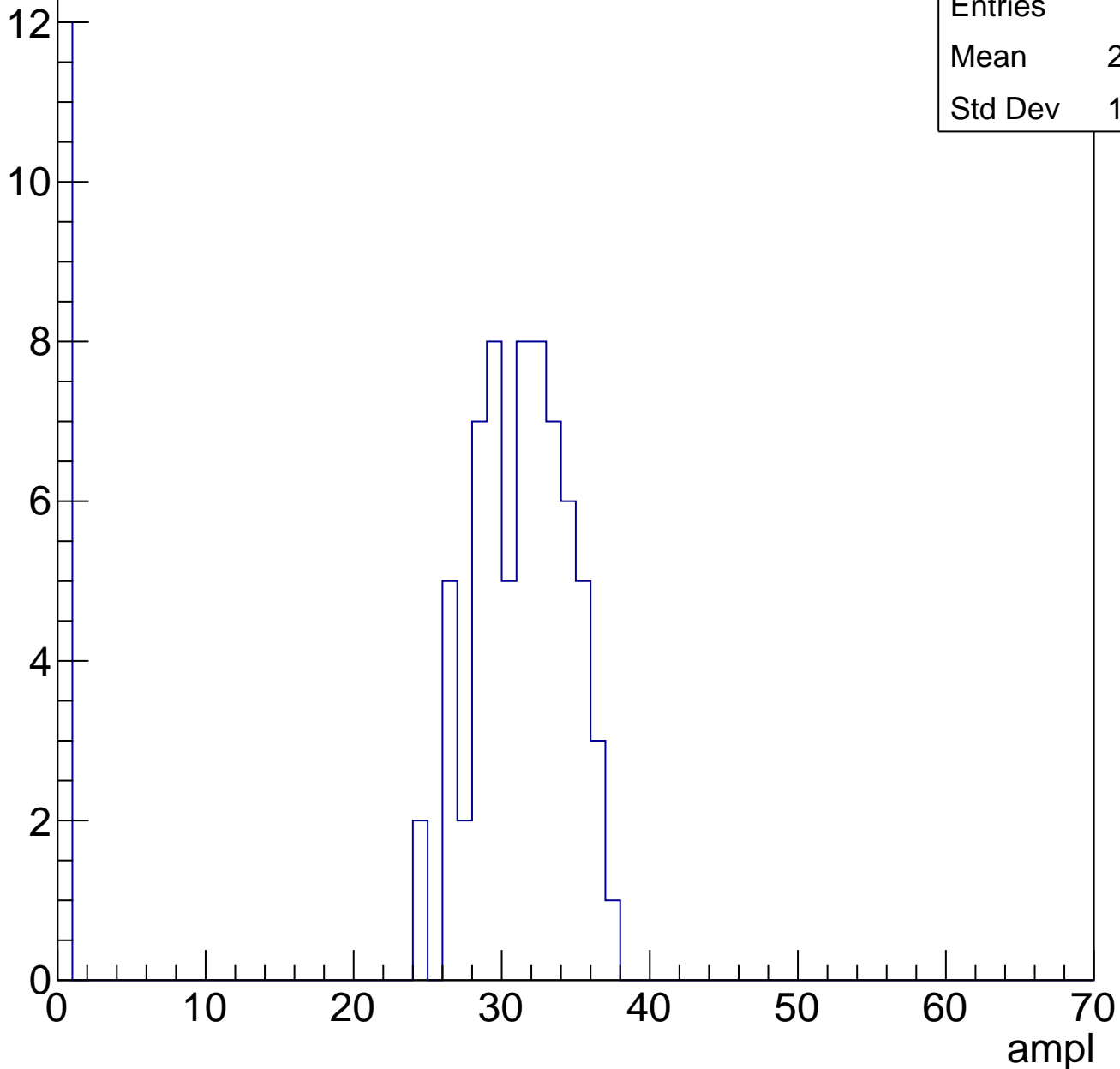


# B1L103S, U4-ch19, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 79    |
| Mean    | 26.19 |
| Std Dev | 11.44 |

Entry

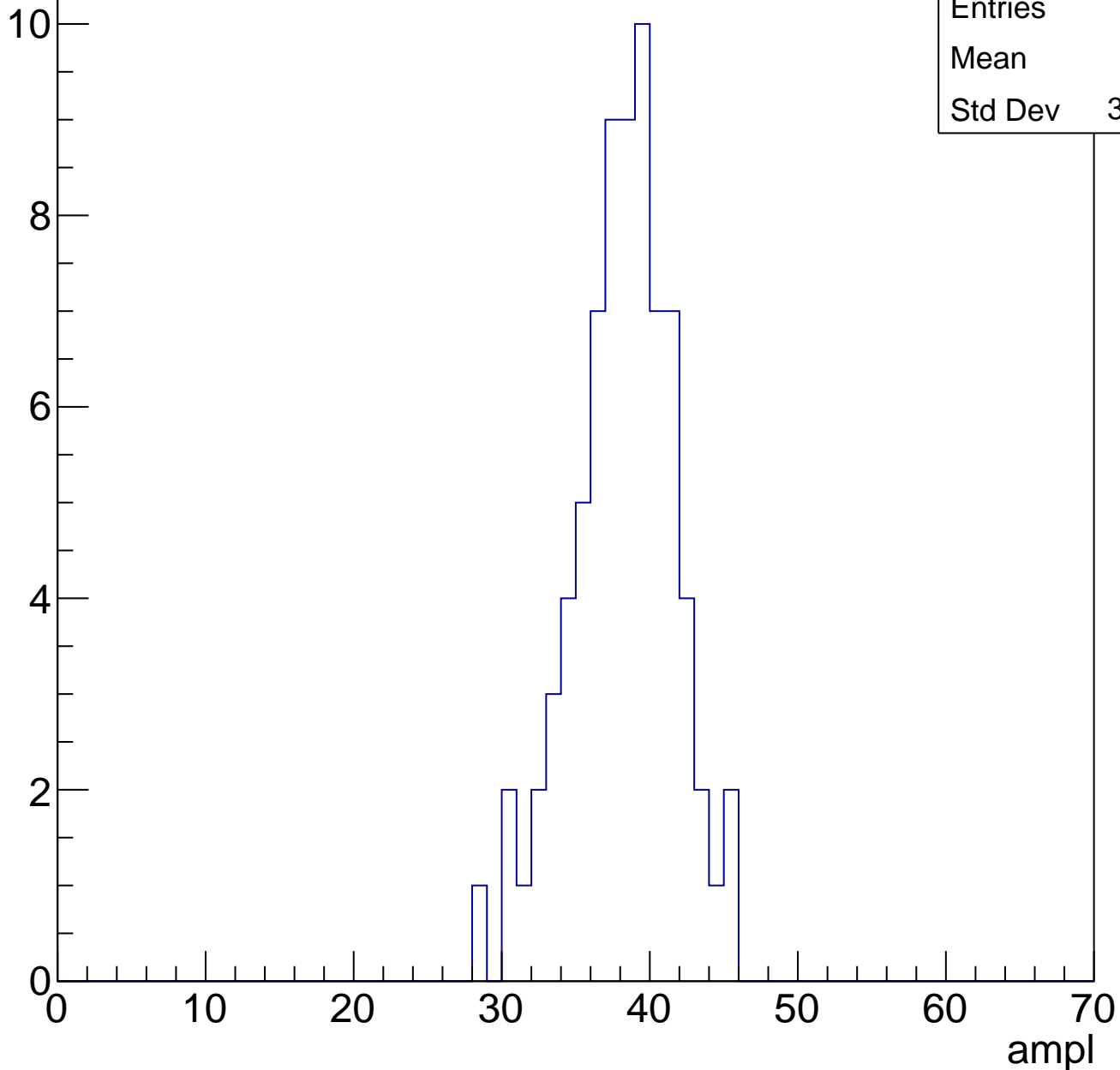


# B1L103S, U4-ch19, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 76    |
| Mean    | 37.7  |
| Std Dev | 3.464 |

Entry

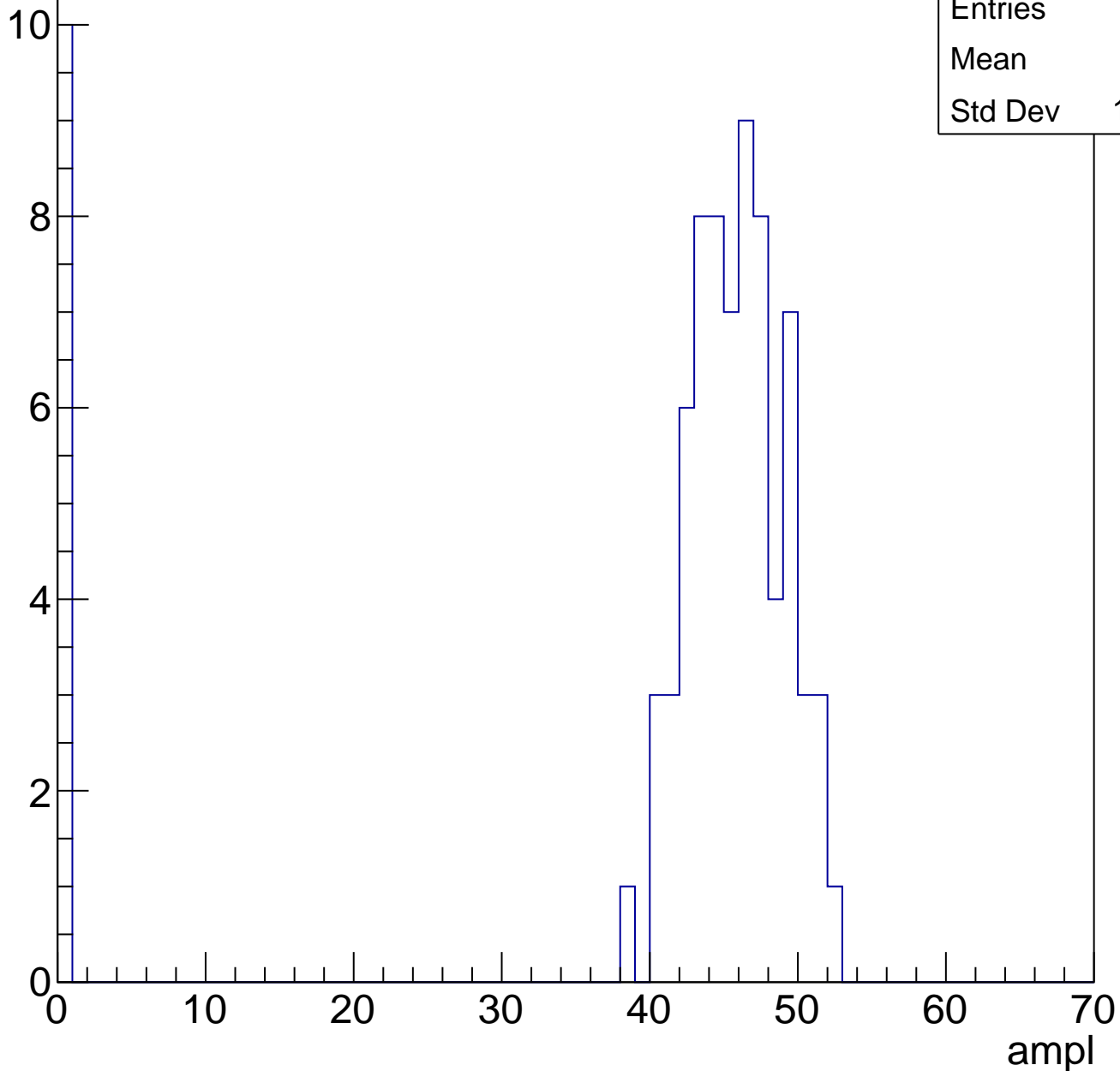


# B1L103S, U4-ch19, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 81    |
| Mean    | 39.8  |
| Std Dev | 15.21 |

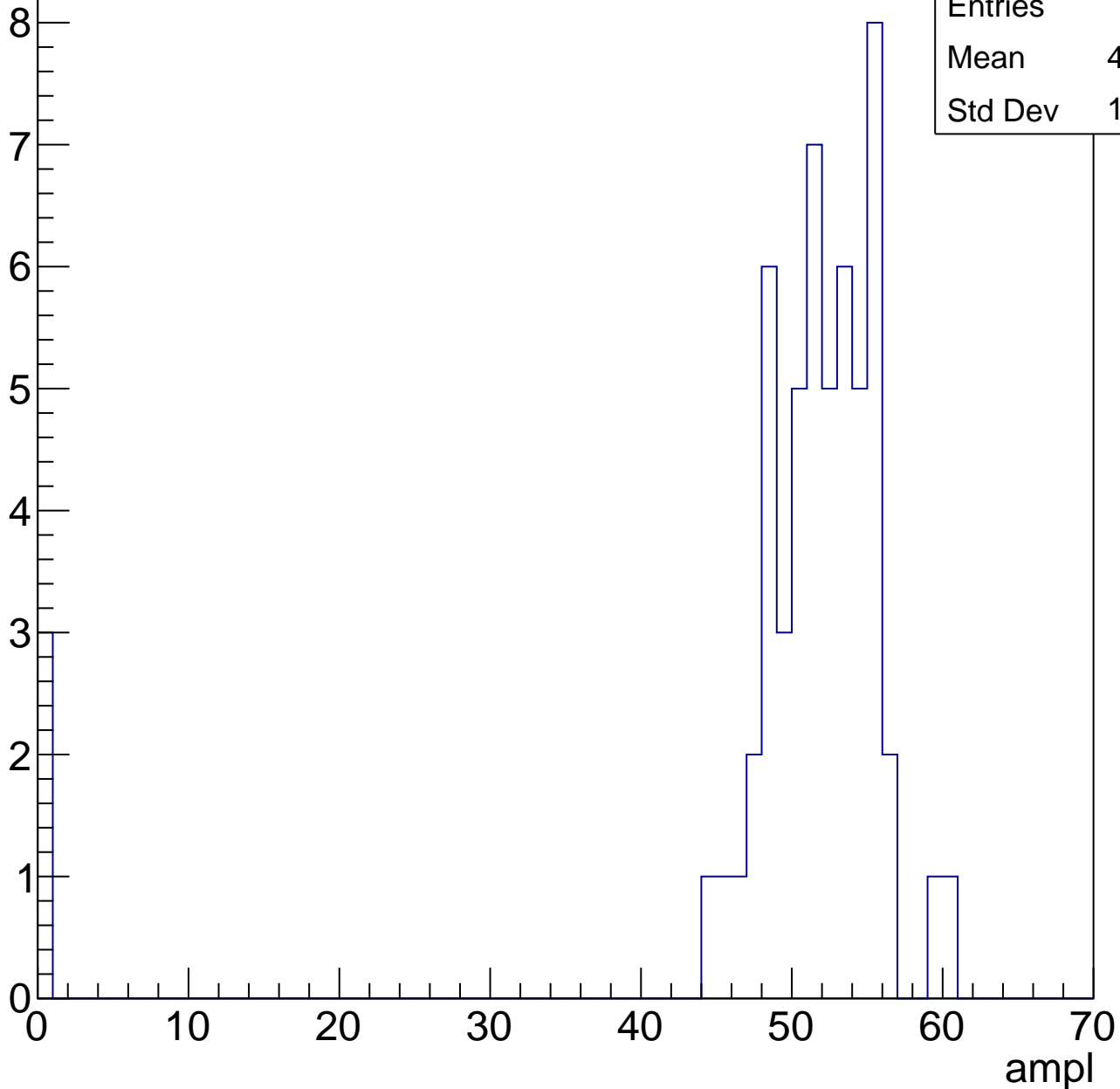


# B1L103S, U4-ch19, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 57    |
| Mean    | 48.95 |
| Std Dev | 11.97 |

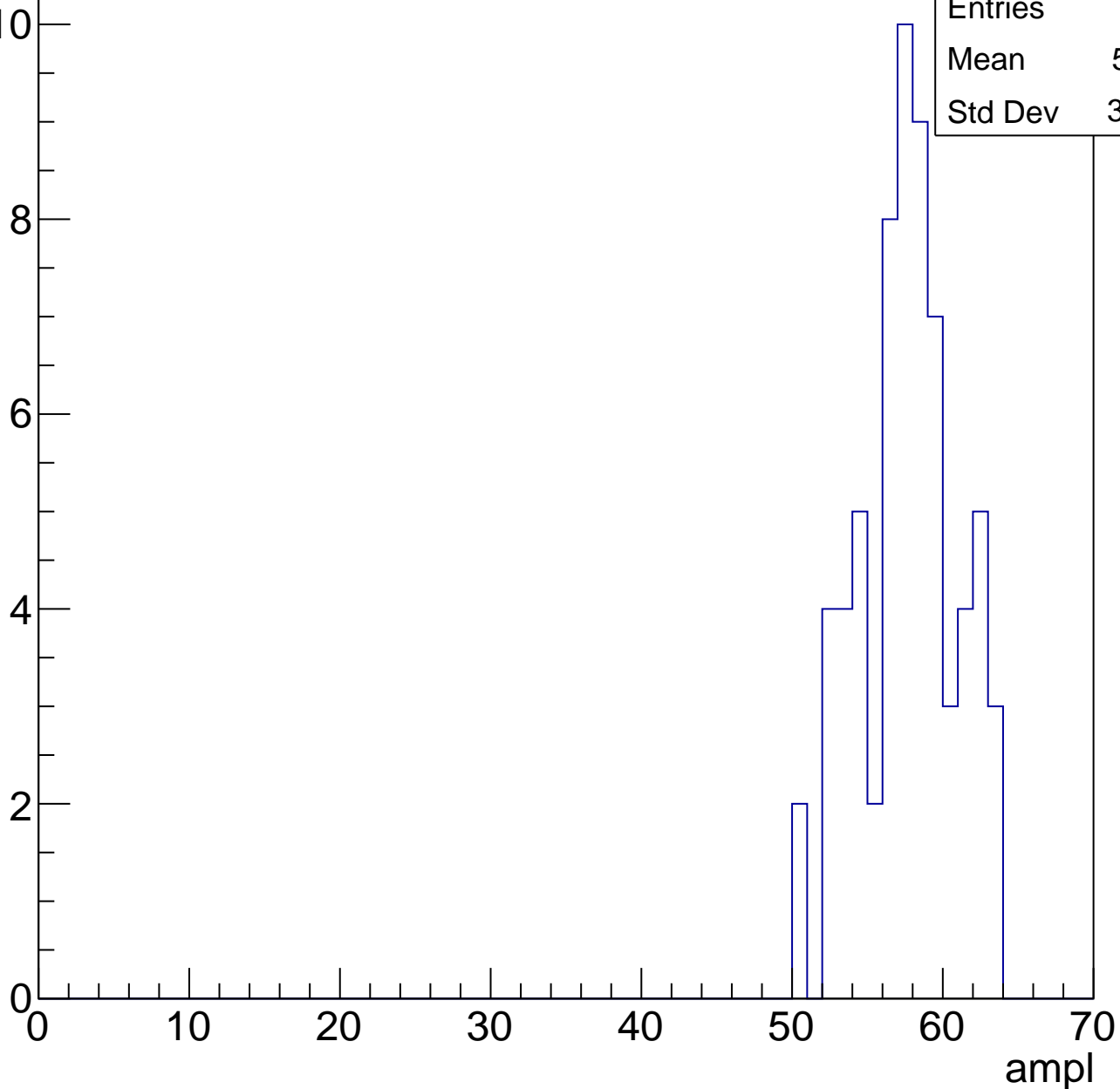


# B1L103S, U4-ch19, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

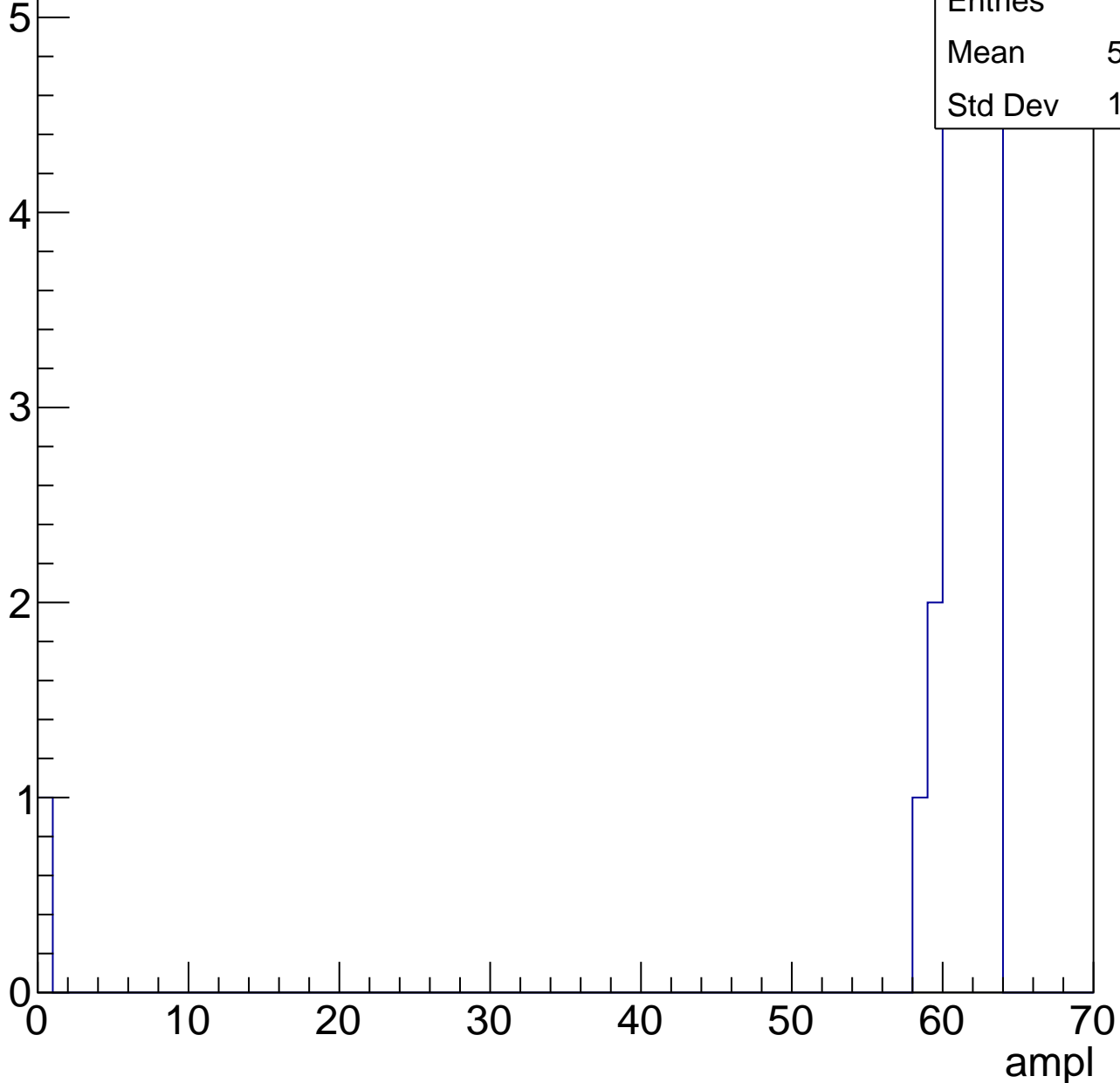
|         |       |
|---------|-------|
| Entries | 66    |
| Mean    | 57.21 |
| Std Dev | 3.212 |



# B1L103S, U4-ch19, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U4-ch19, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U4-ch19, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



|         |    |
|---------|----|
| Entries | 18 |
| Mean    | 0  |
| Std Dev | 0  |

# B1L103S, U4-ch20, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

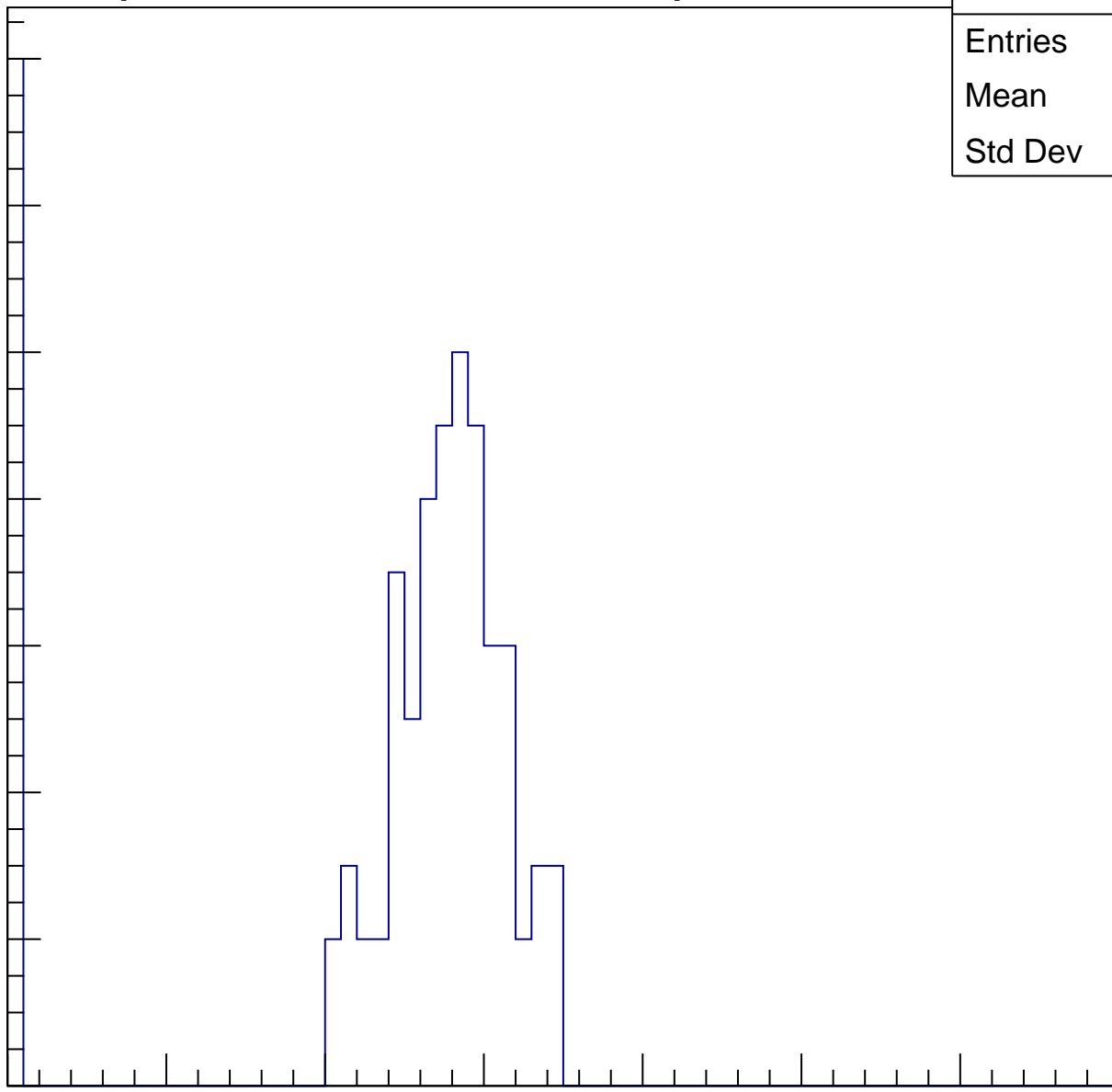
|         |       |
|---------|-------|
| Entries | 91    |
| Mean    | 23.18 |
| Std Dev | 10.35 |

Entry

14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

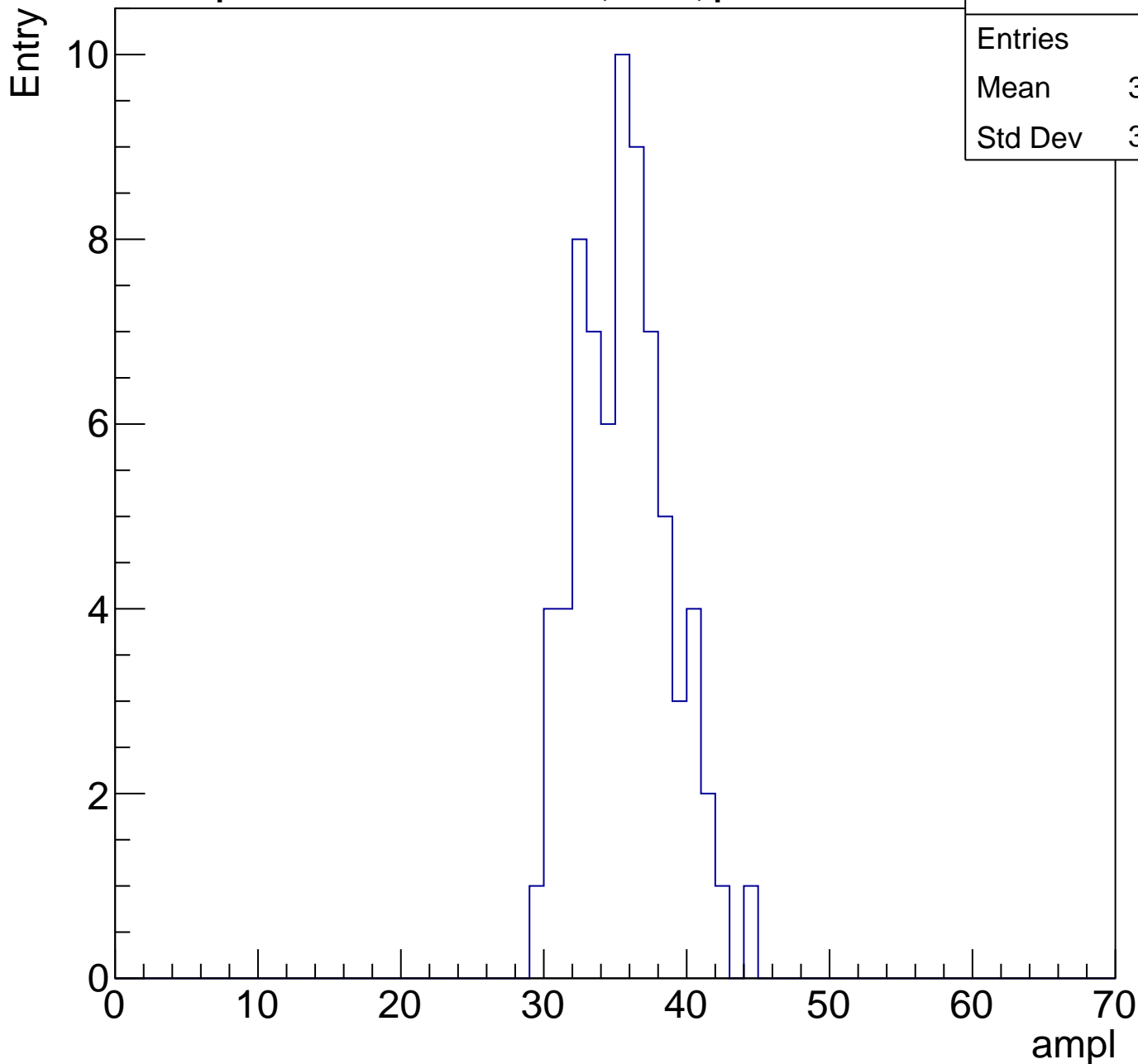
ampl



# B1L103S, U4-ch20, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 72    |
| Mean    | 35.17 |
| Std Dev | 3.197 |

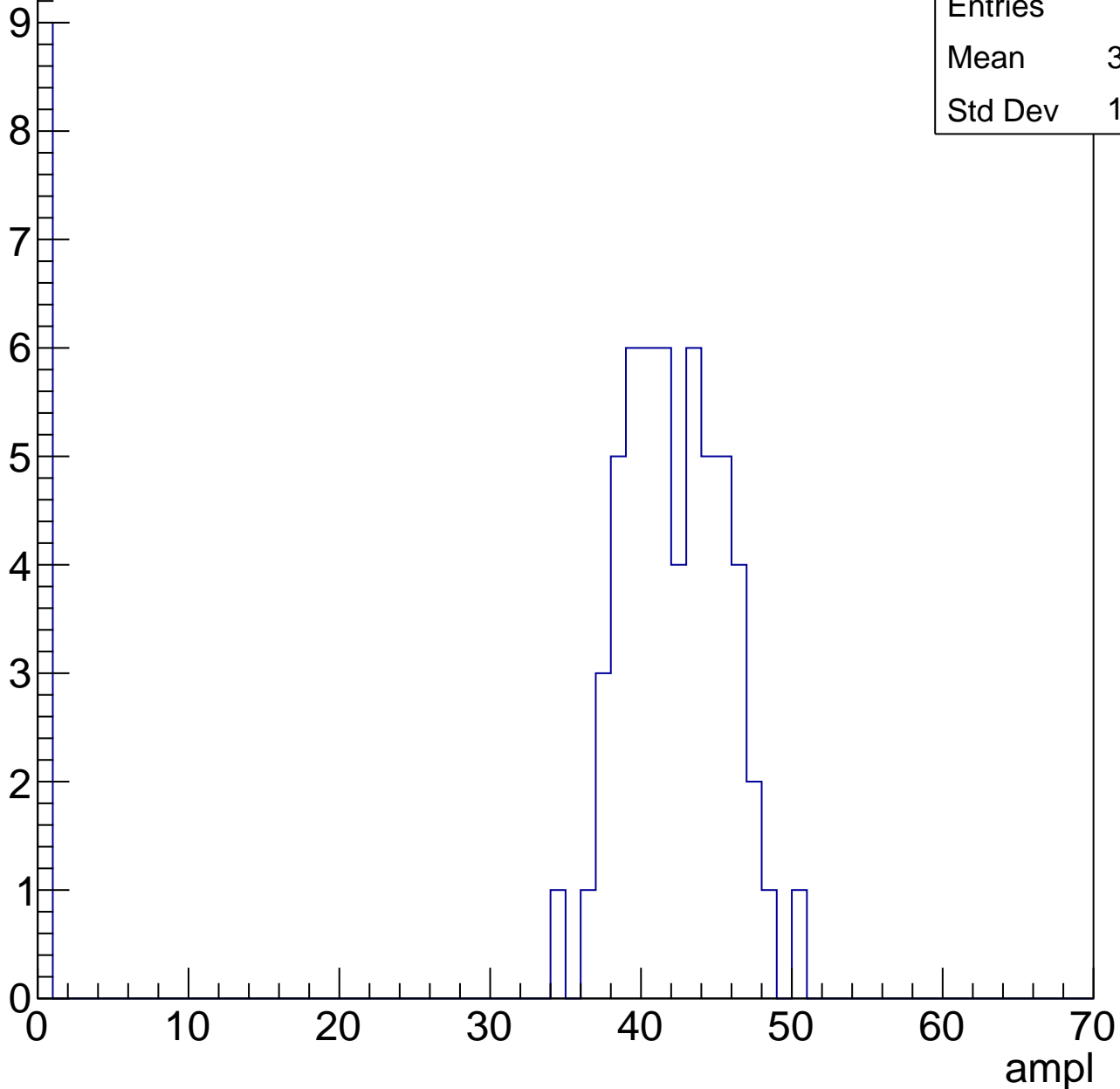


# B1L103S, U4-ch20, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

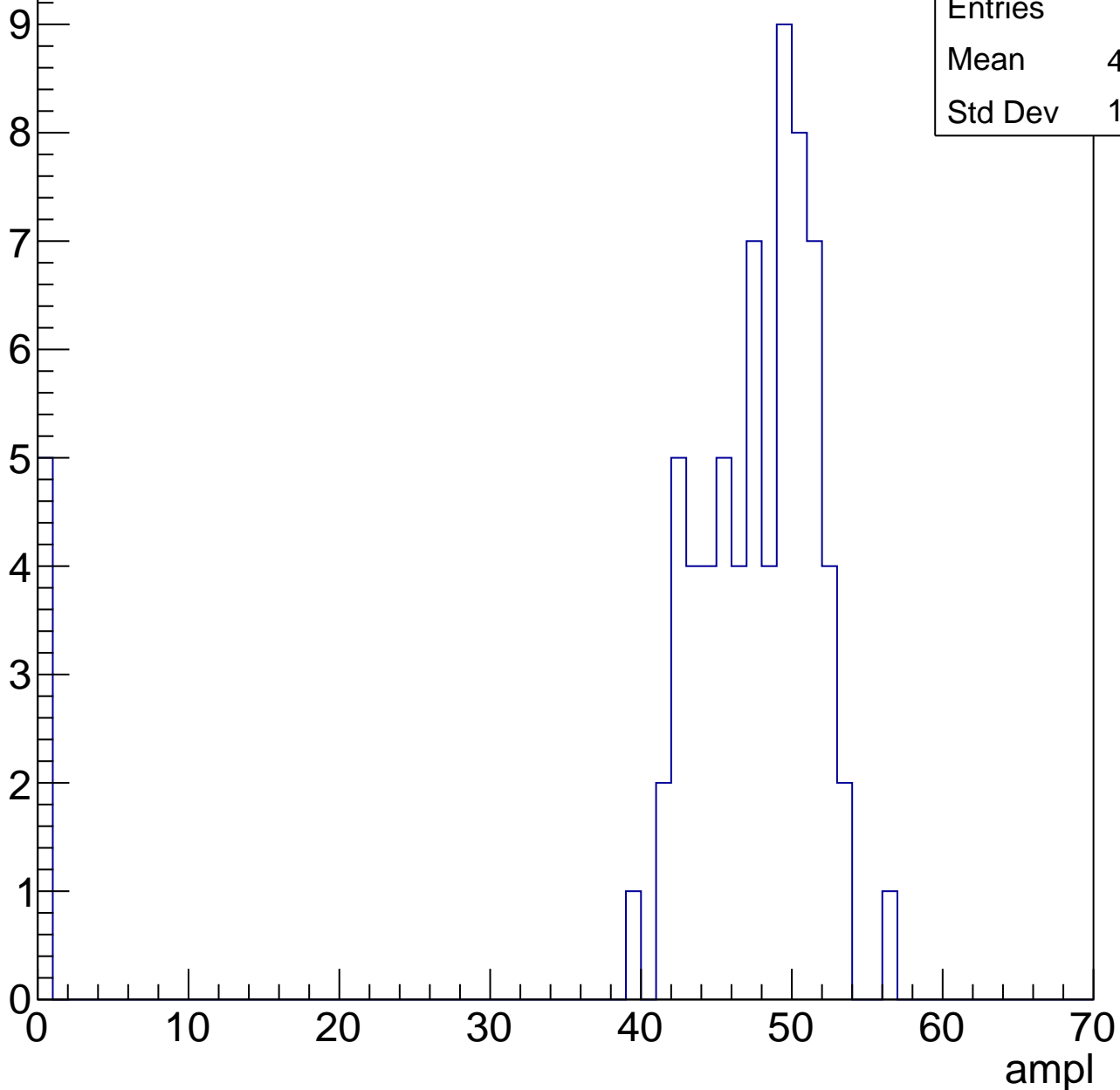
|         |       |
|---------|-------|
| Entries | 65    |
| Mean    | 35.97 |
| Std Dev | 14.75 |



# B1L103S, U4-ch20, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

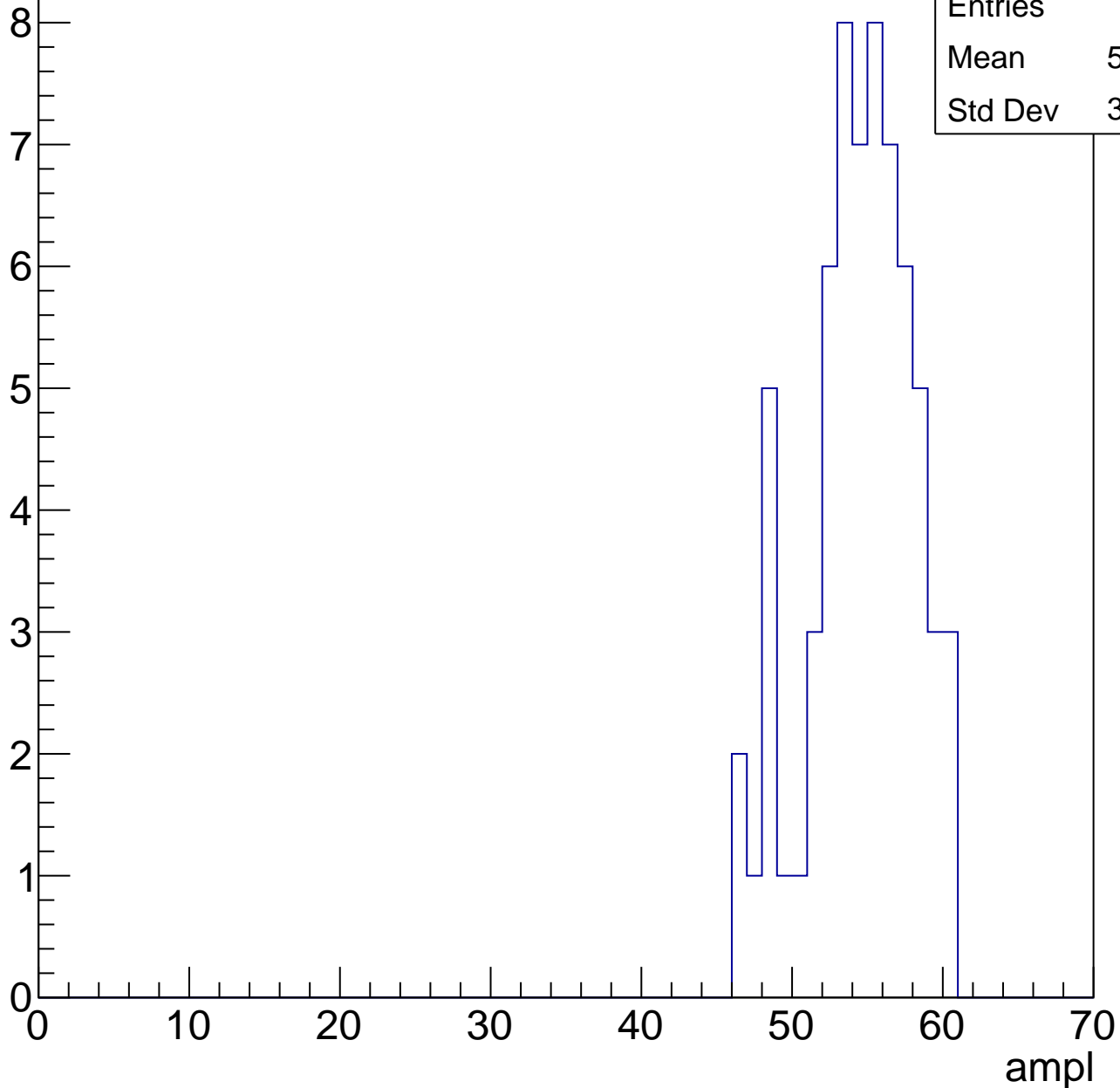
Entry



# B1L103S, U4-ch20, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



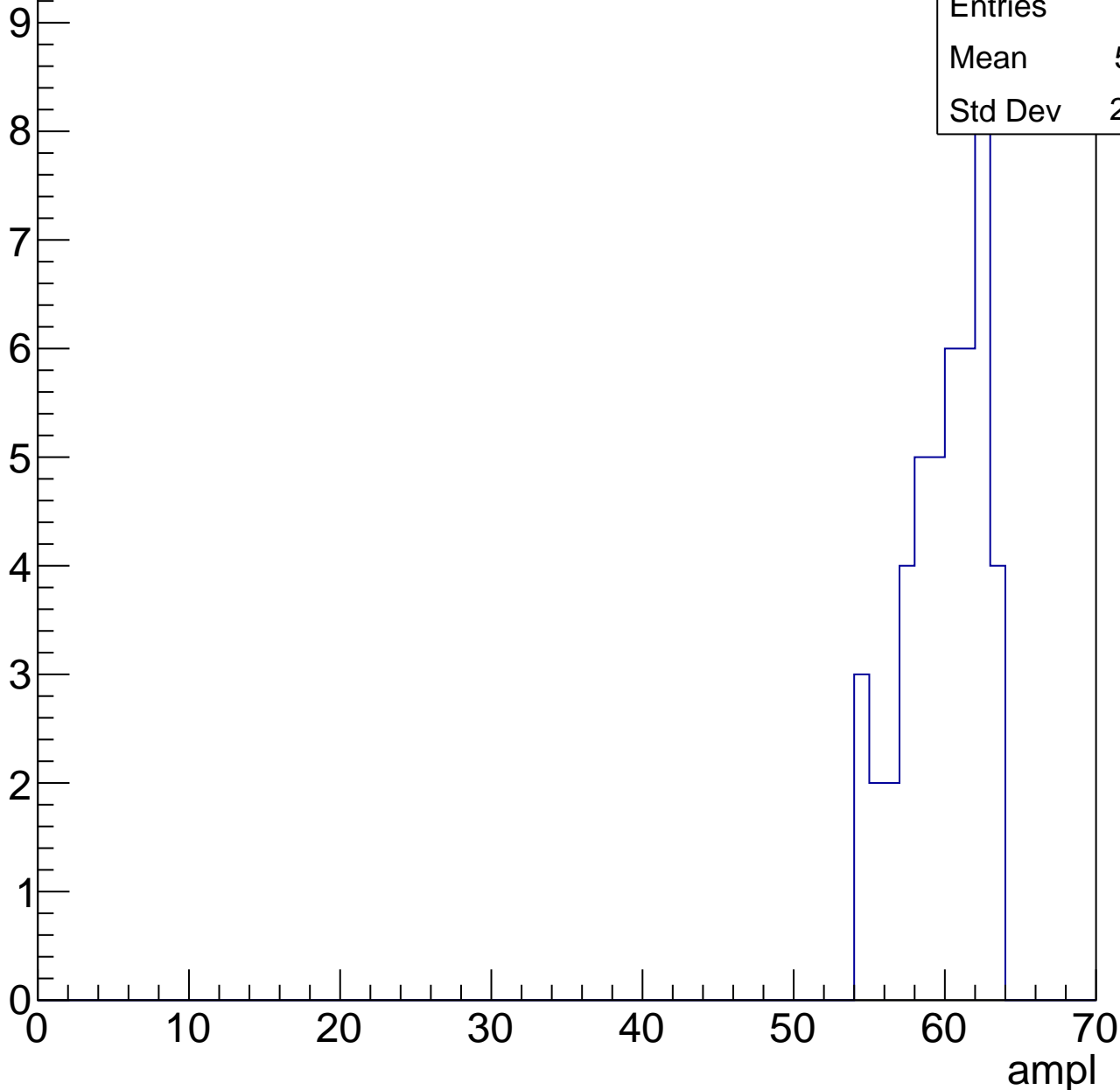
|         |       |
|---------|-------|
| Entries | 66    |
| Mean    | 54.03 |
| Std Dev | 3.503 |

# B1L103S, U4-ch20, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 46    |
| Mean    | 59.41 |
| Std Dev | 2.609 |

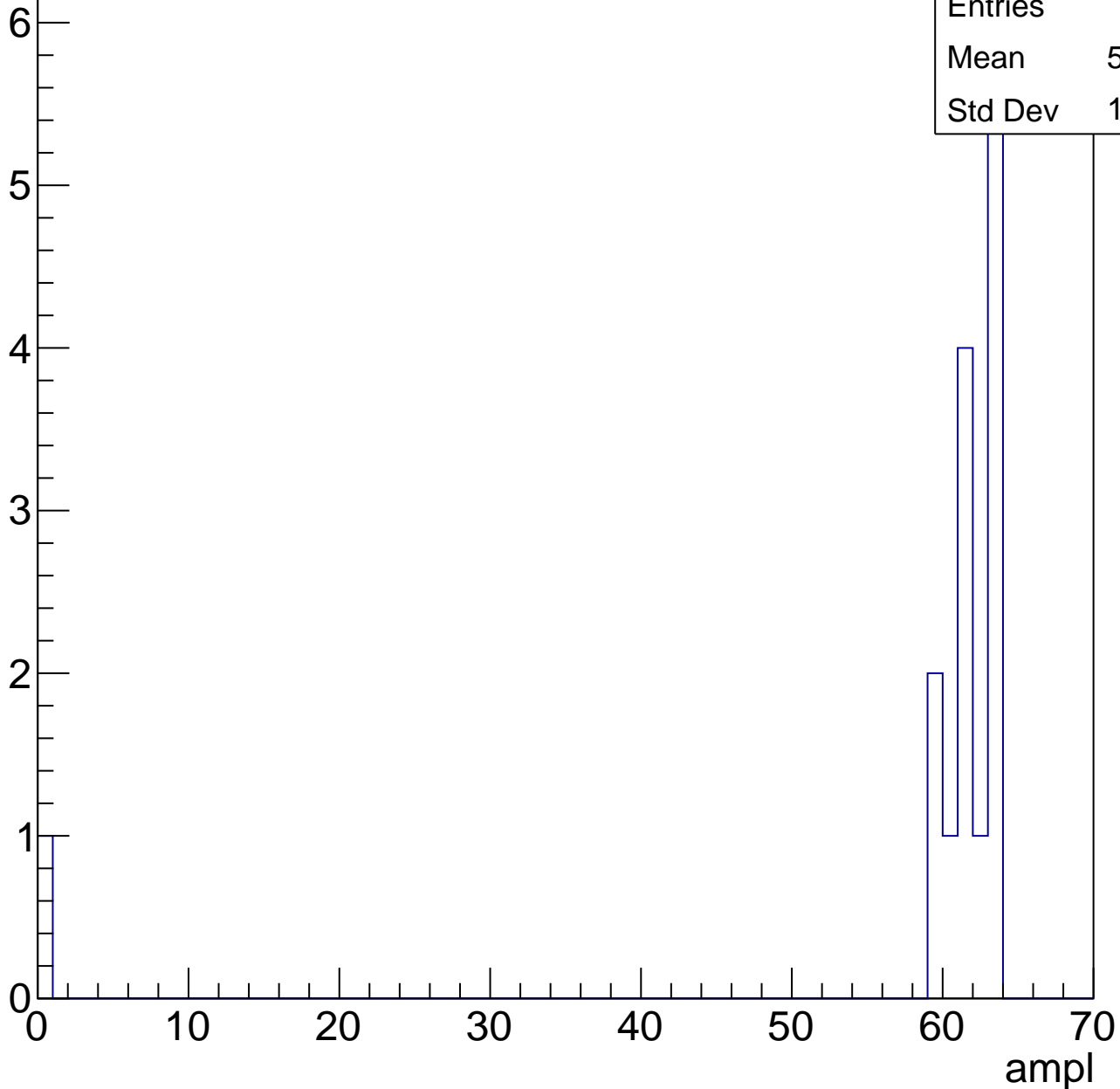


# B1L103S, U4-ch20, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 15    |
| Mean    | 57.47 |
| Std Dev | 15.42 |





# B1L103S, U4-ch20, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

|         |    |
|---------|----|
| Entries | 19 |
| Mean    | 0  |
| Std Dev | 0  |

# B1L103S, U4-ch21, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

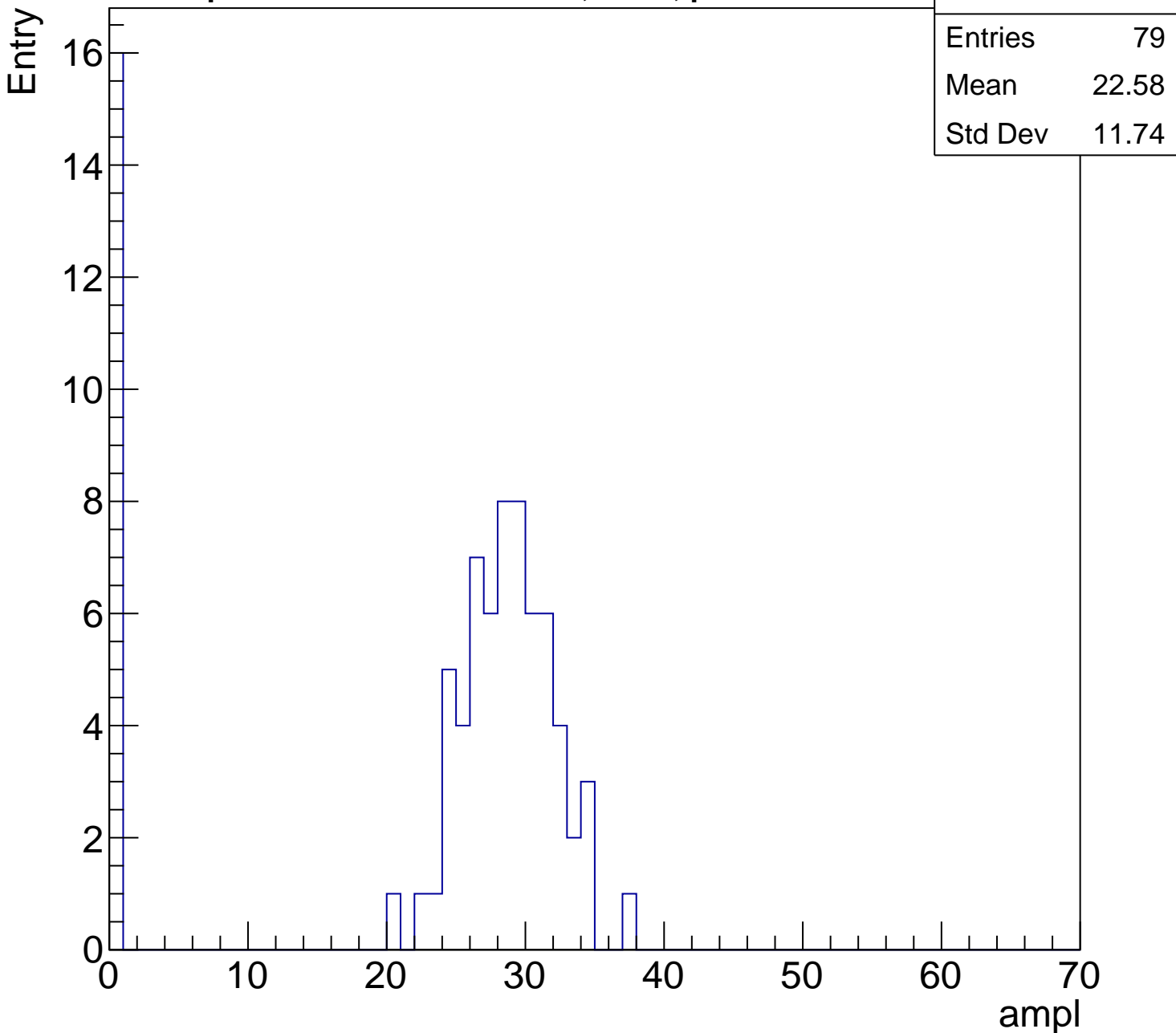
Entry

16  
14  
12  
10  
8  
6  
4  
2  
0

|         |       |
|---------|-------|
| Entries | 79    |
| Mean    | 22.58 |
| Std Dev | 11.74 |

ampl

0 10 20 30 40 50 60 70



# B1L103S, U4-ch21, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

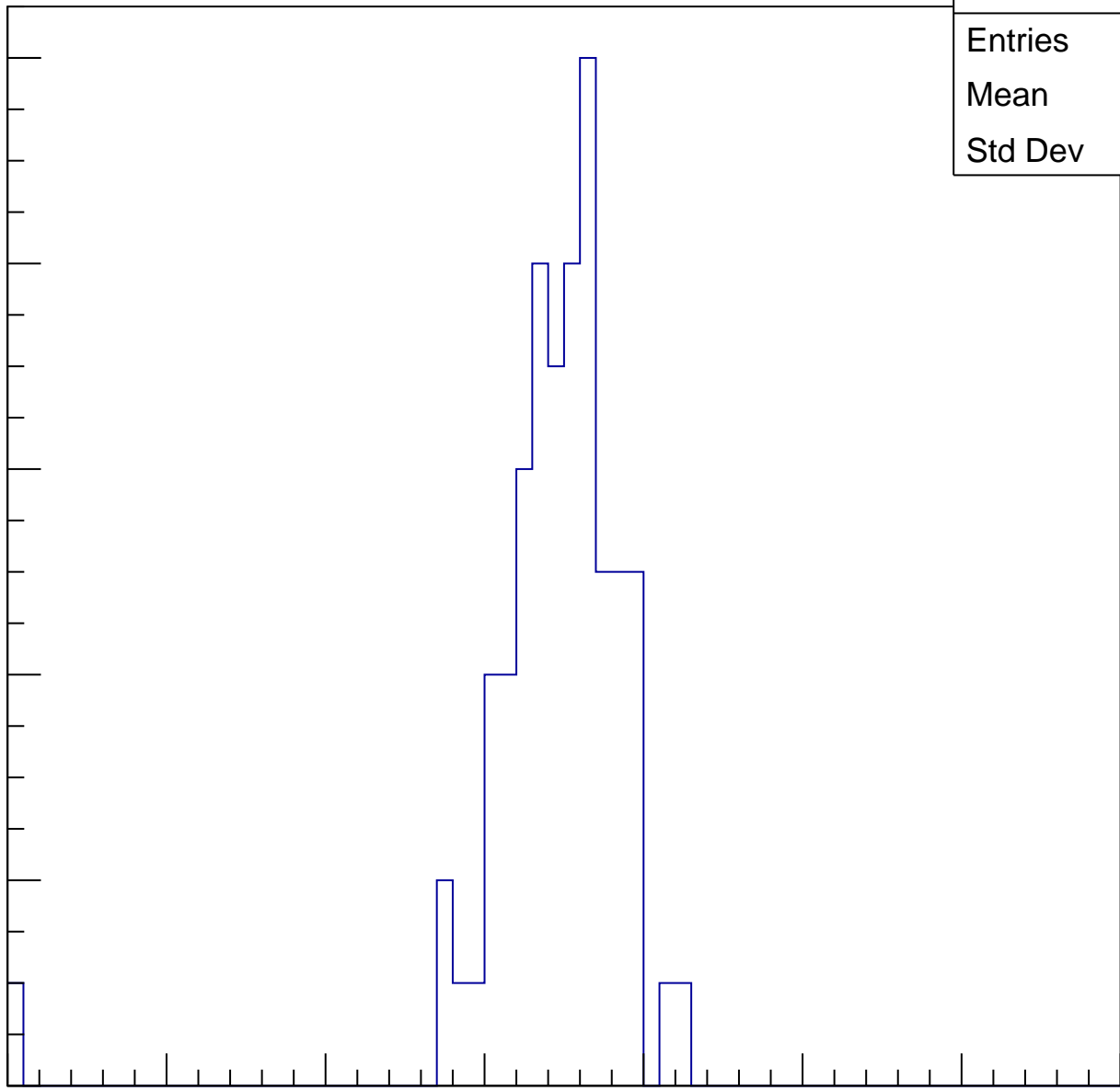
|         |       |
|---------|-------|
| Entries | 69    |
| Mean    | 33.94 |
| Std Dev | 5.189 |

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

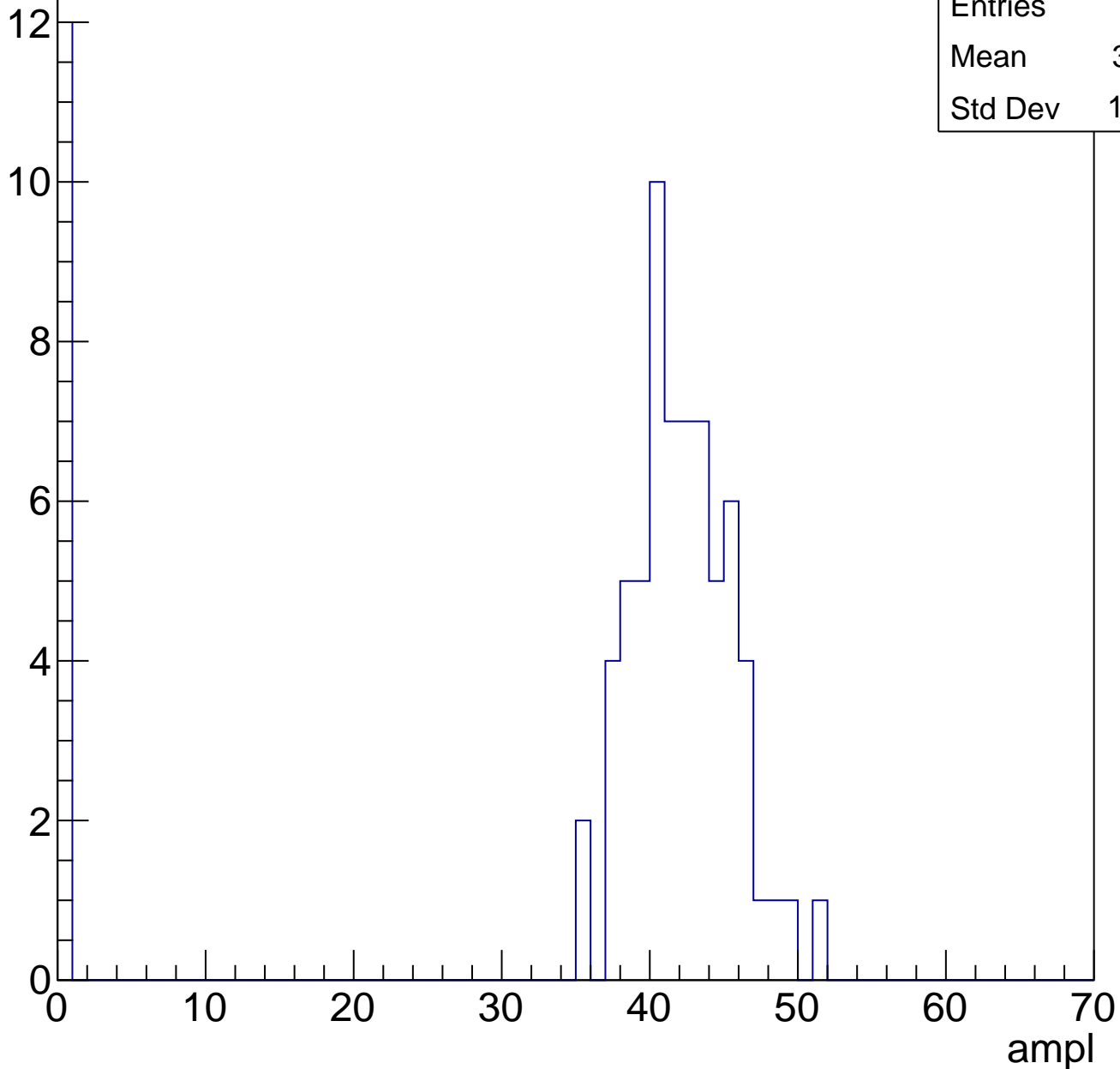


# B1L103S, U4-ch21, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 78    |
| Mean    | 35.31 |
| Std Dev | 15.35 |

Entry

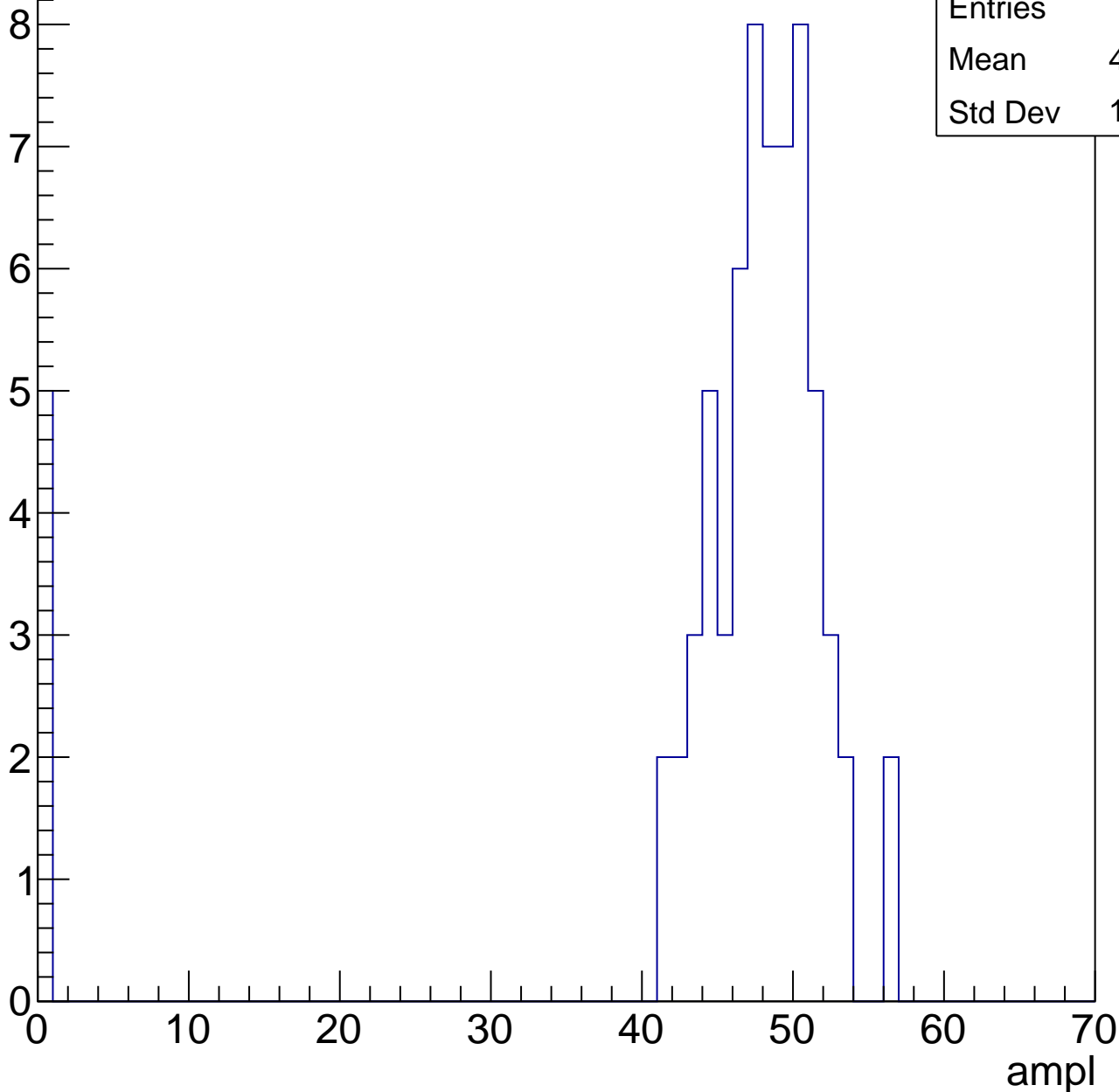


# B1L103S, U4-ch21, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 68    |
| Mean    | 44.26 |
| Std Dev | 12.87 |

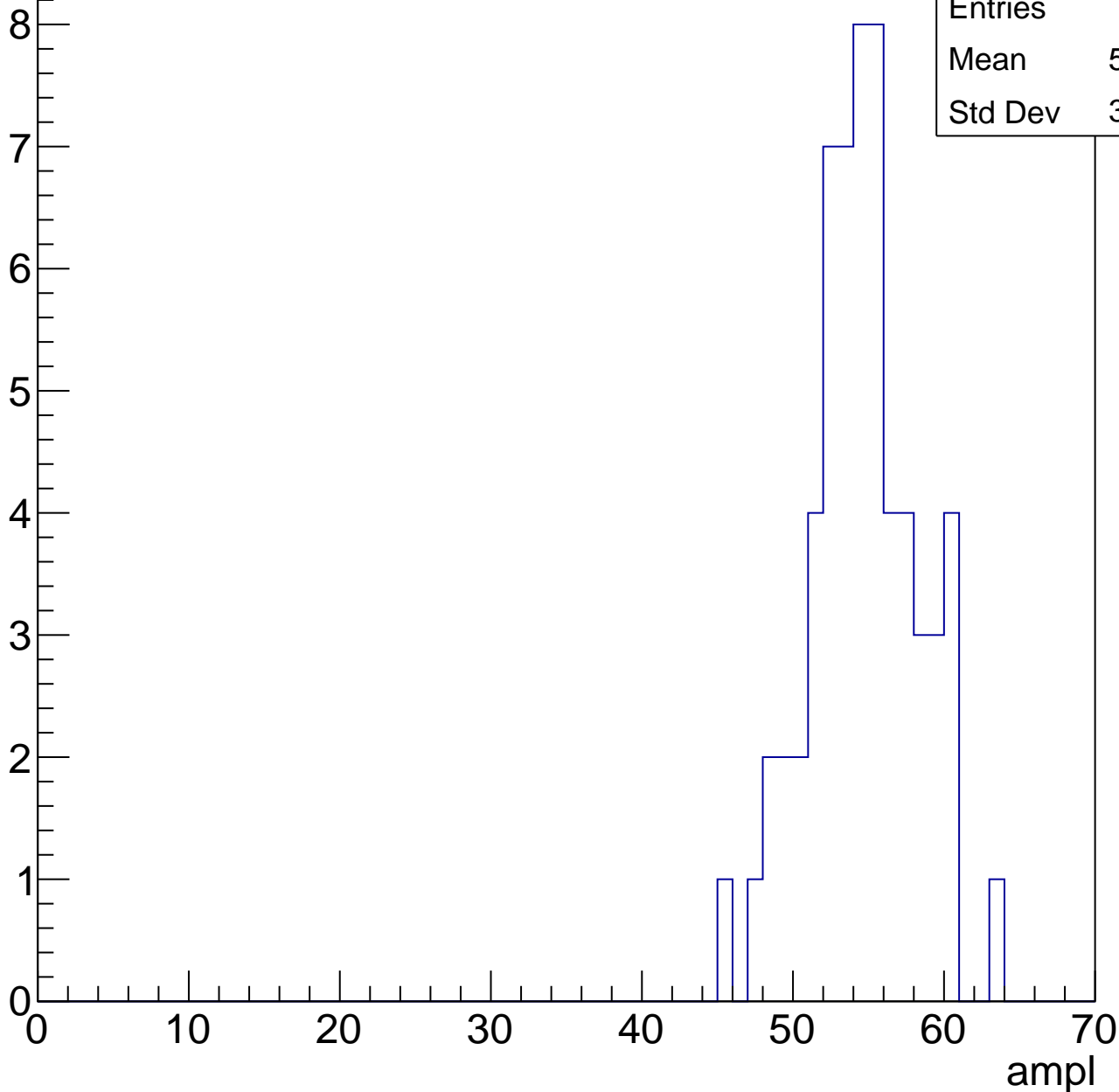


# B1L103S, U4-ch21, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 61    |
| Mean    | 54.15 |
| Std Dev | 3.534 |

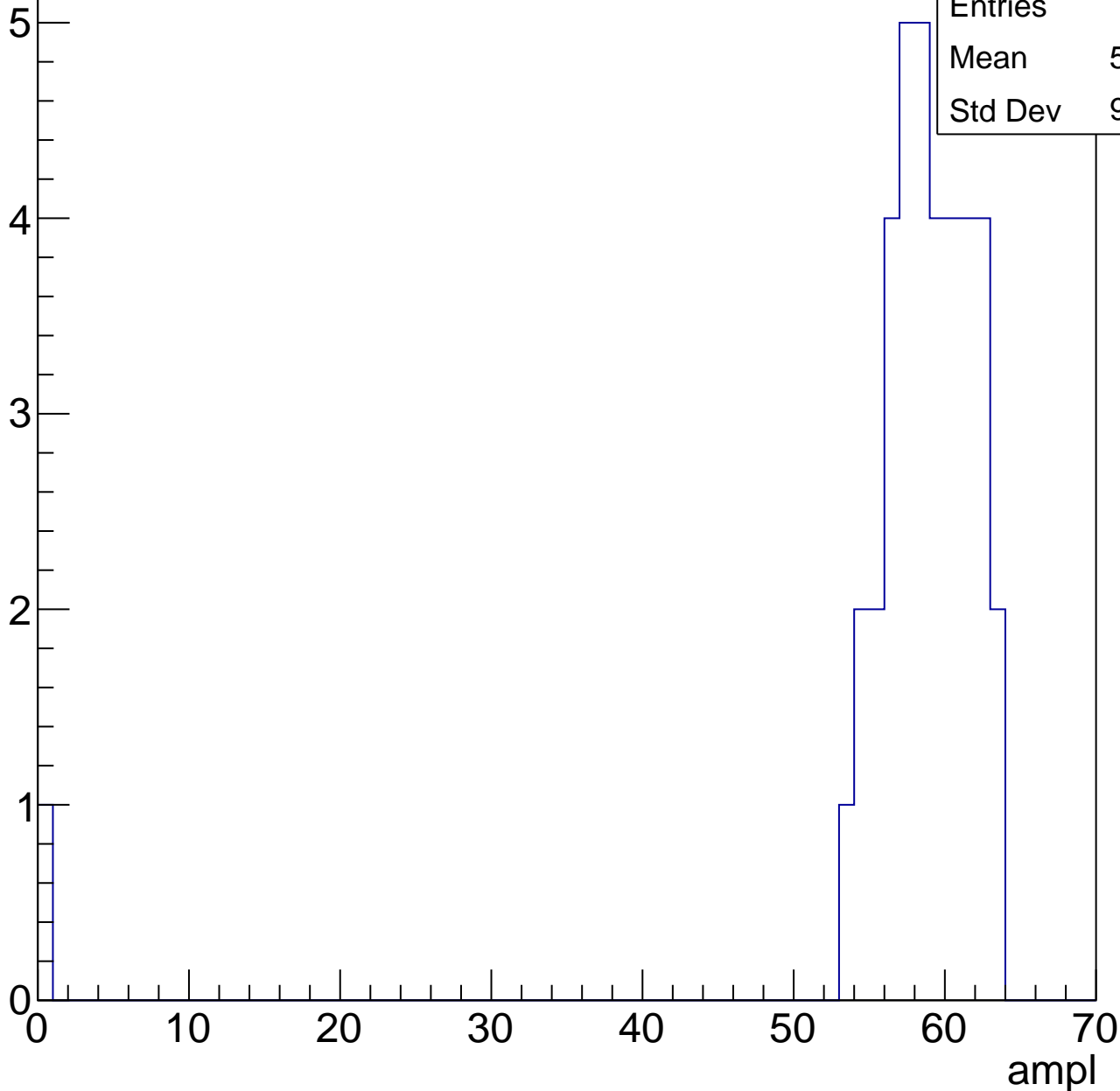


# B1L103S, U4-ch21, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 38    |
| Mean    | 56.95 |
| Std Dev | 9.717 |







# B1L103S, U4-ch21, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



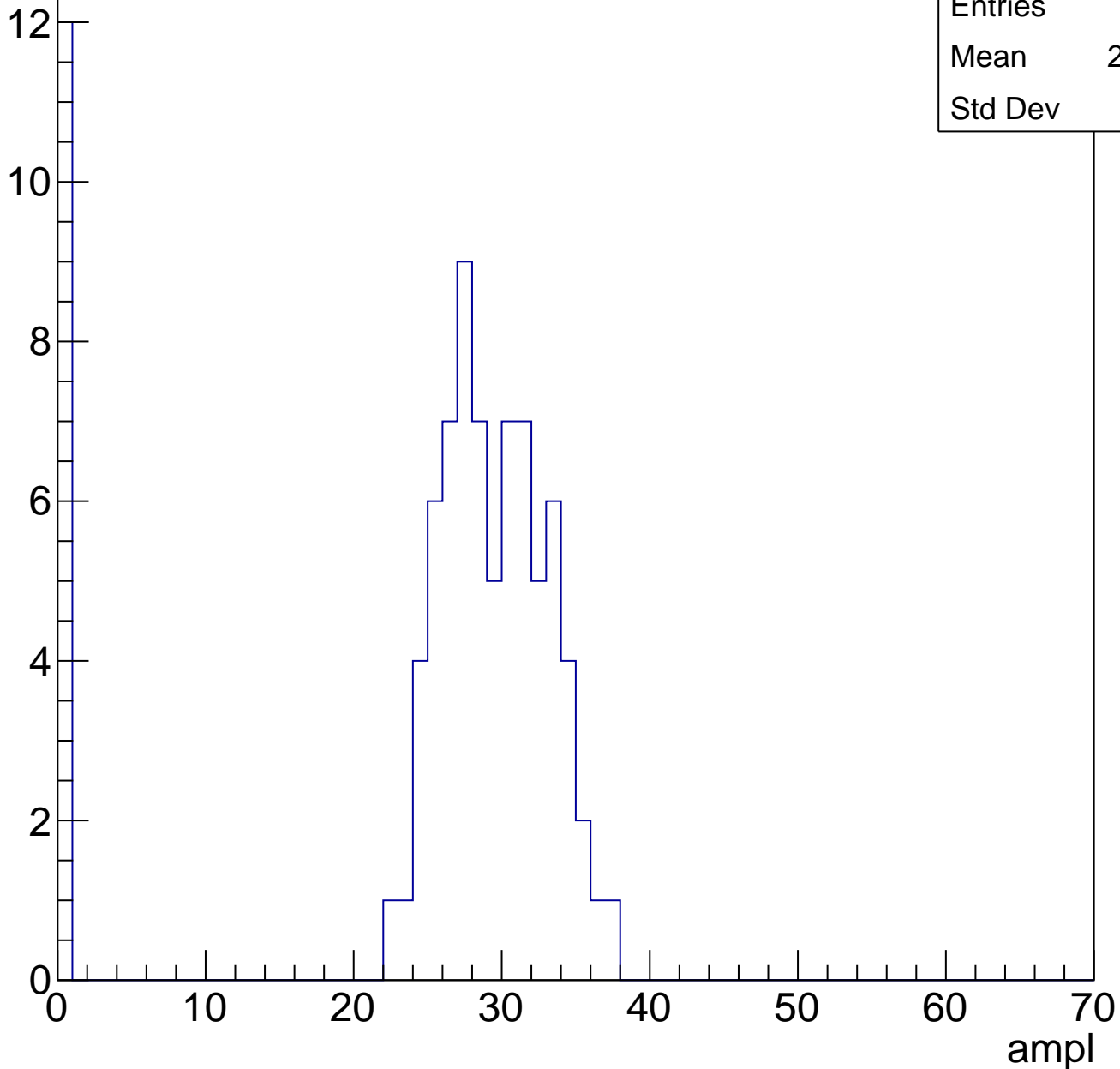
|         |       |
|---------|-------|
| Entries | 20    |
| Mean    | 3.15  |
| Std Dev | 13.73 |

# B1L103S, U4-ch22, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 85    |
| Mean    | 24.95 |
| Std Dev | 10.6  |

Entry

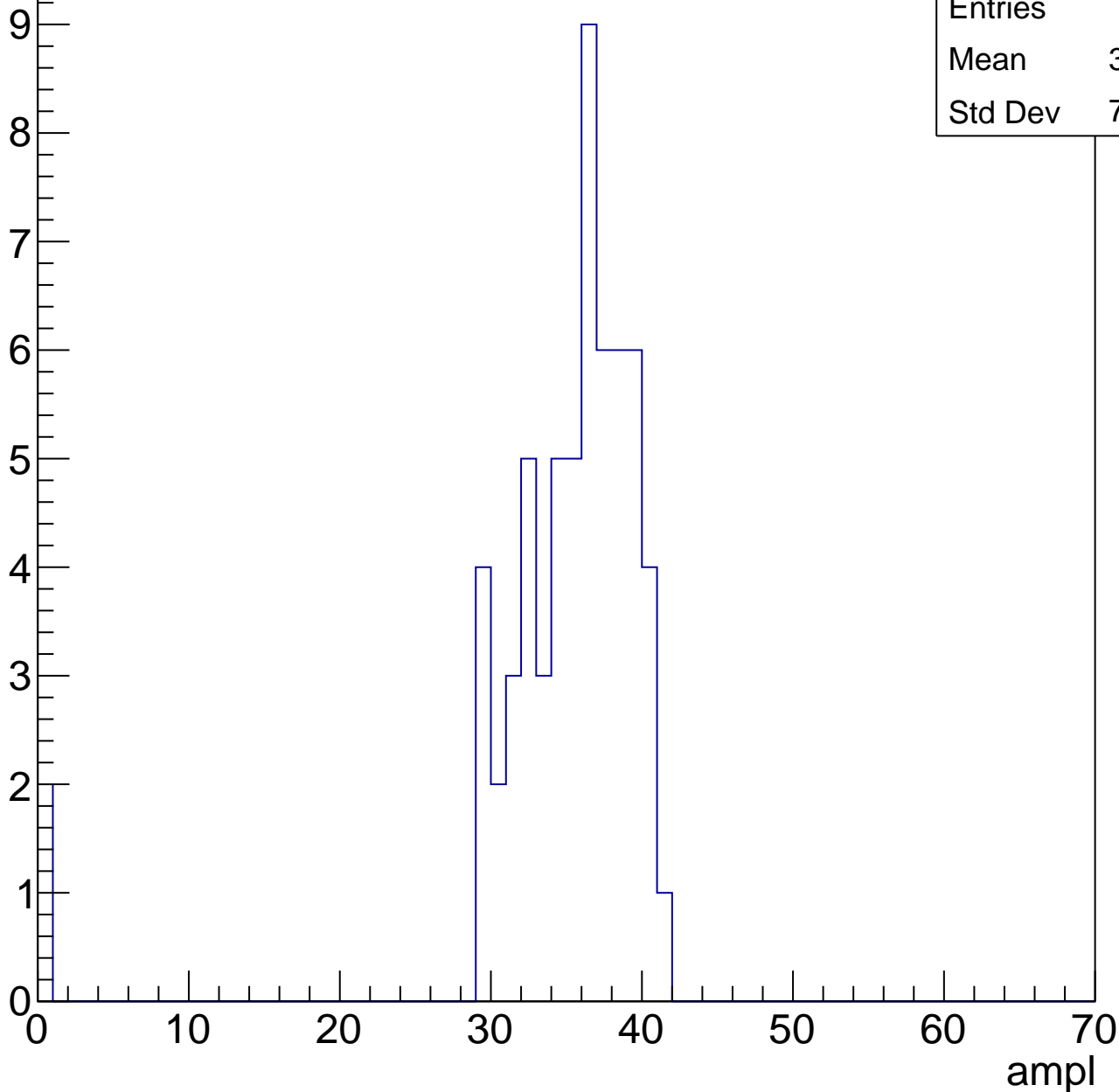


# B1L103S, U4-ch22, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 61    |
| Mean    | 34.13 |
| Std Dev | 7.044 |

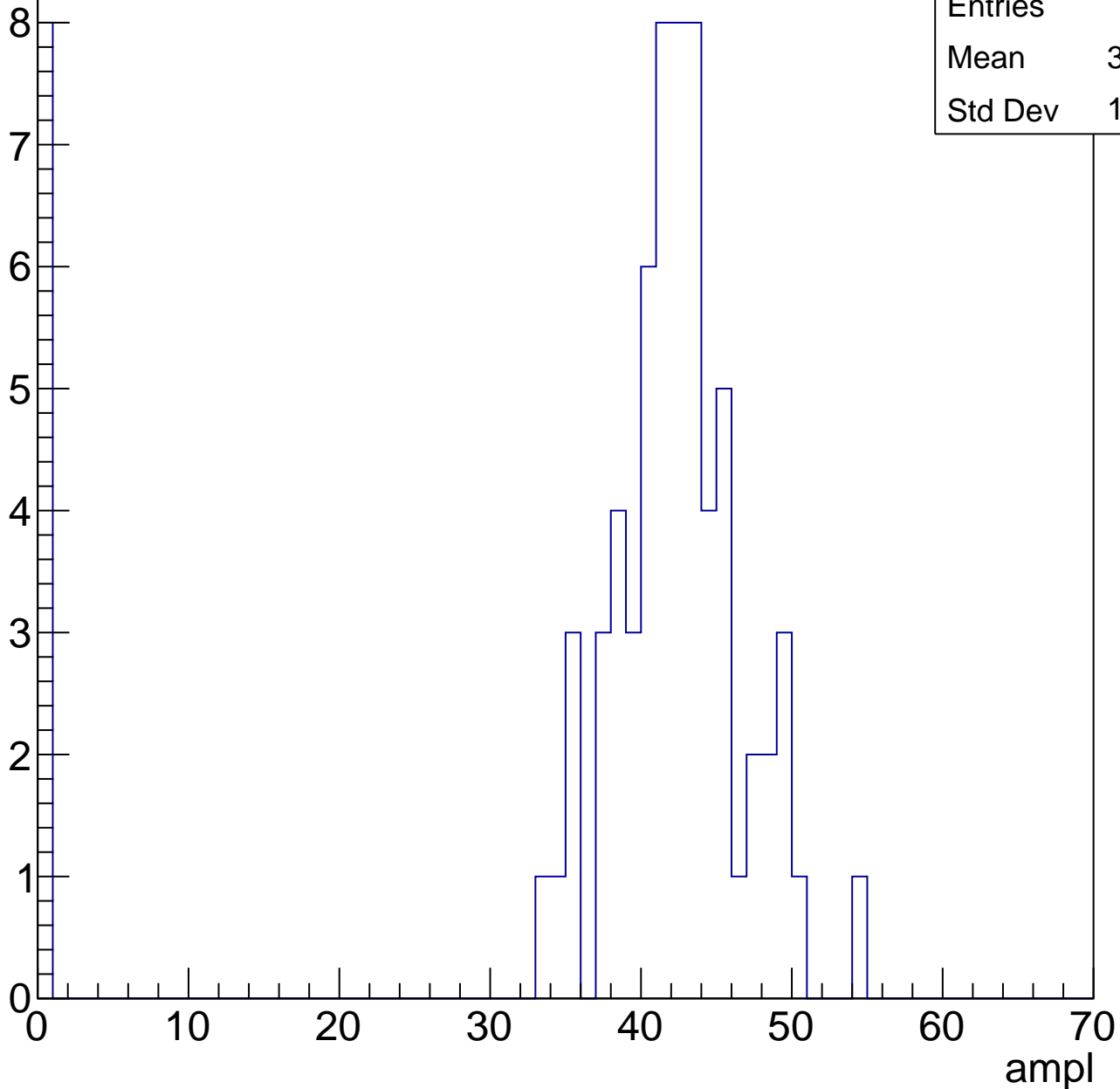


# B1L103S, U4-ch22, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 72    |
| Mean    | 37.33 |
| Std Dev | 13.74 |

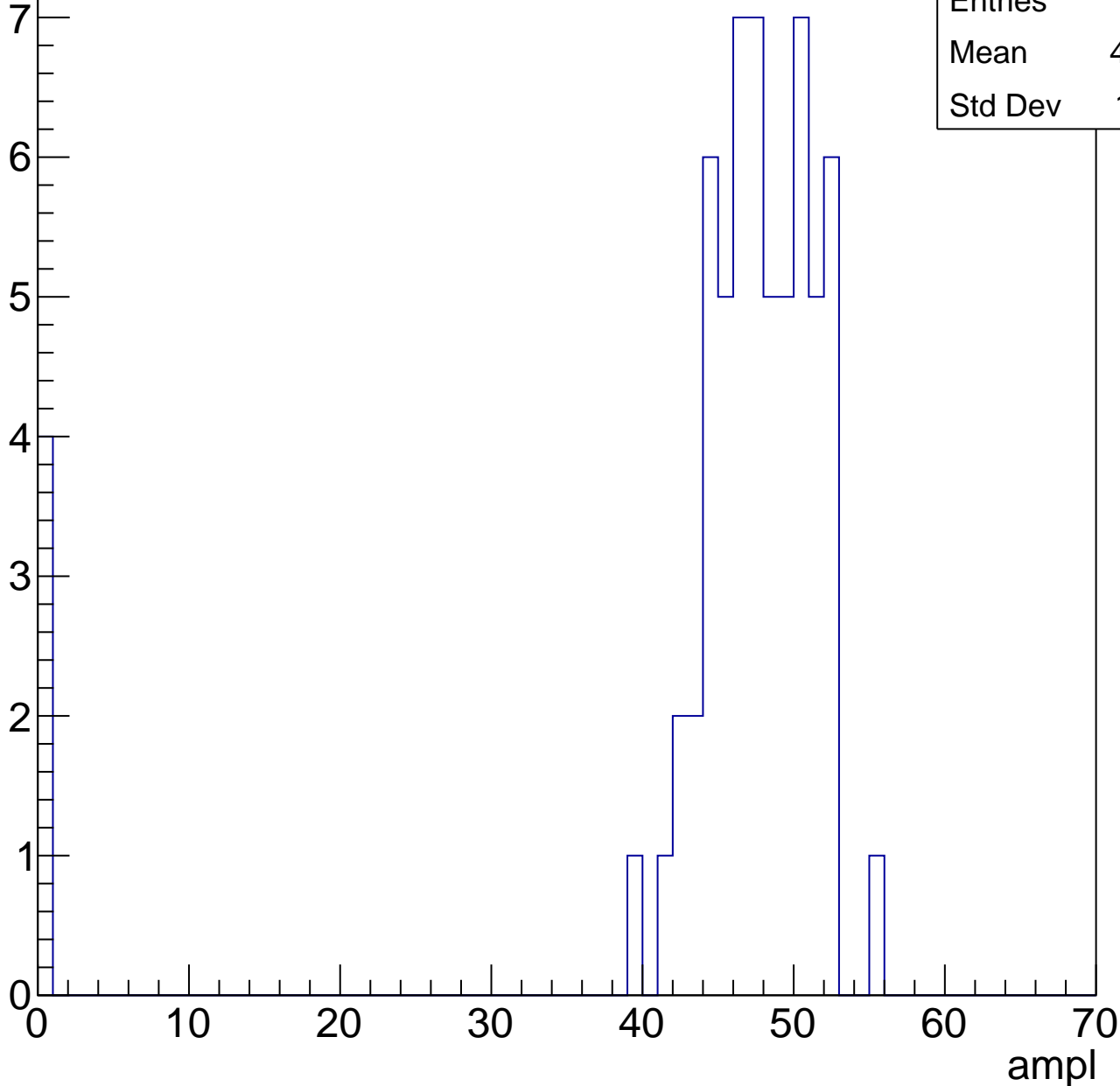


# B1L103S, U4-ch22, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 64    |
| Mean    | 44.48 |
| Std Dev | 11.91 |

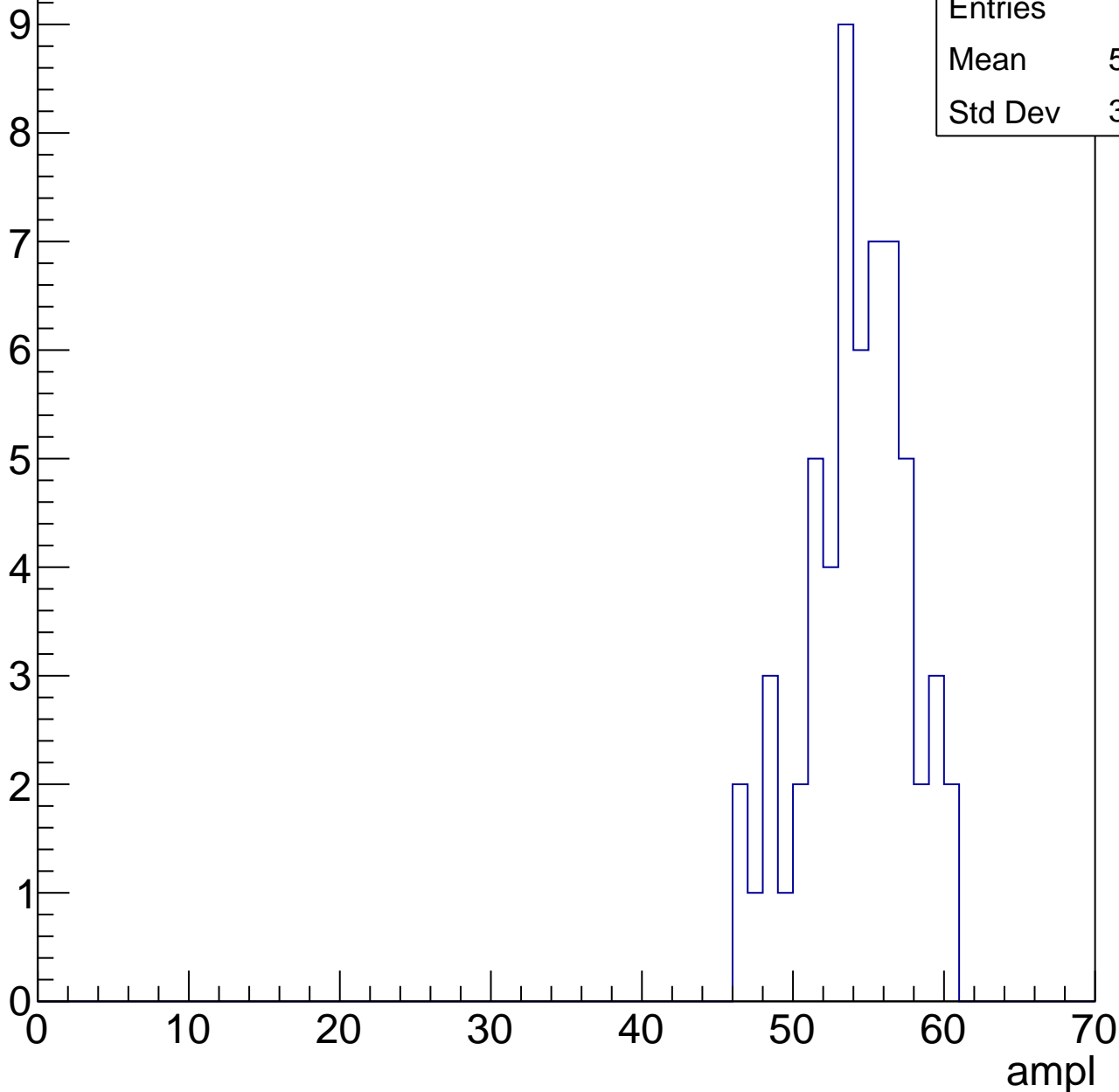


# B1L103S, U4-ch22, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 59    |
| Mean    | 53.75 |
| Std Dev | 3.363 |

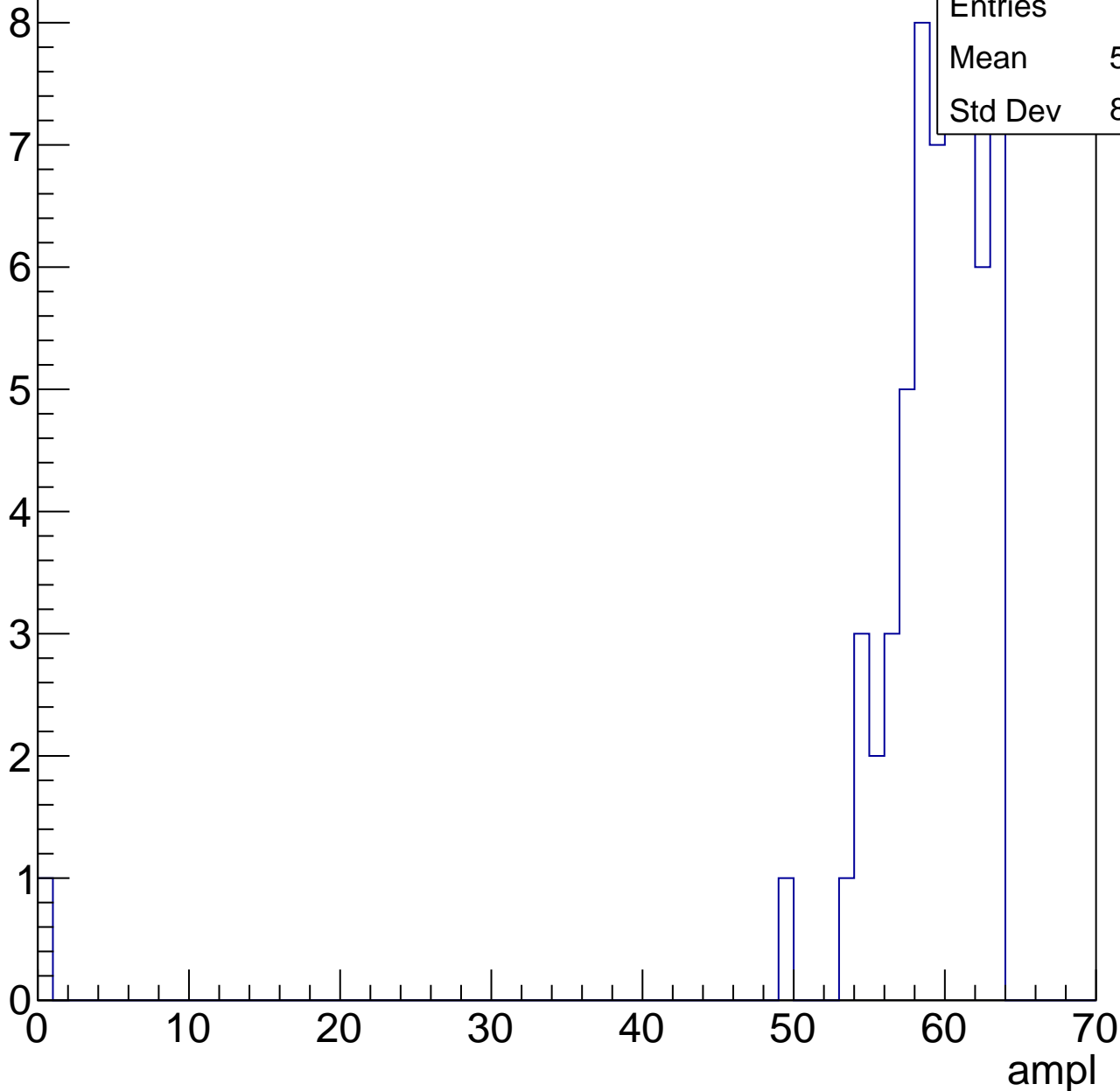


# B1L103S, U4-ch22, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

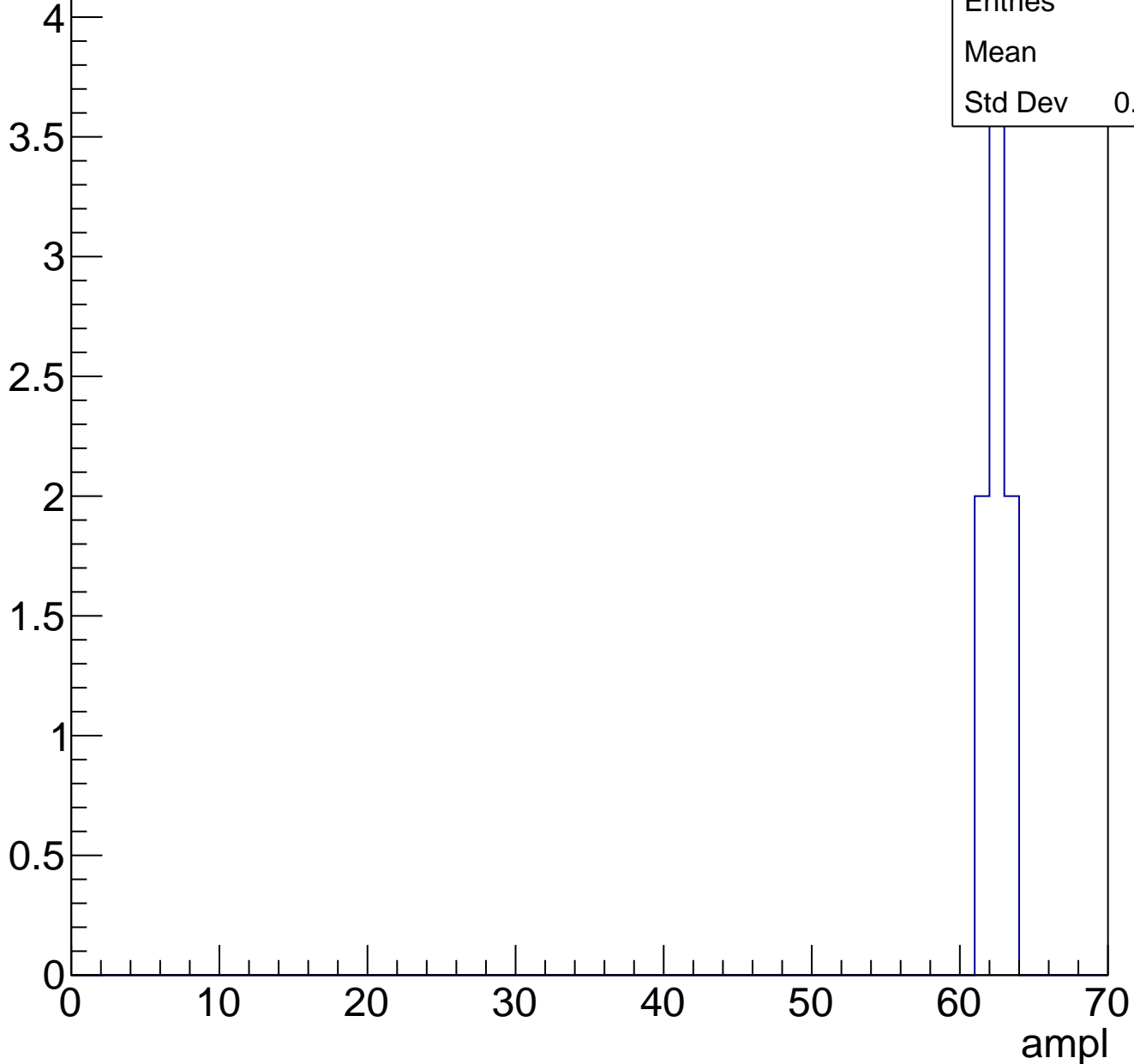
|         |       |
|---------|-------|
| Entries | 61    |
| Mean    | 58.16 |
| Std Dev | 8.056 |



# B1L103S, U4-ch22, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U4-ch22, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

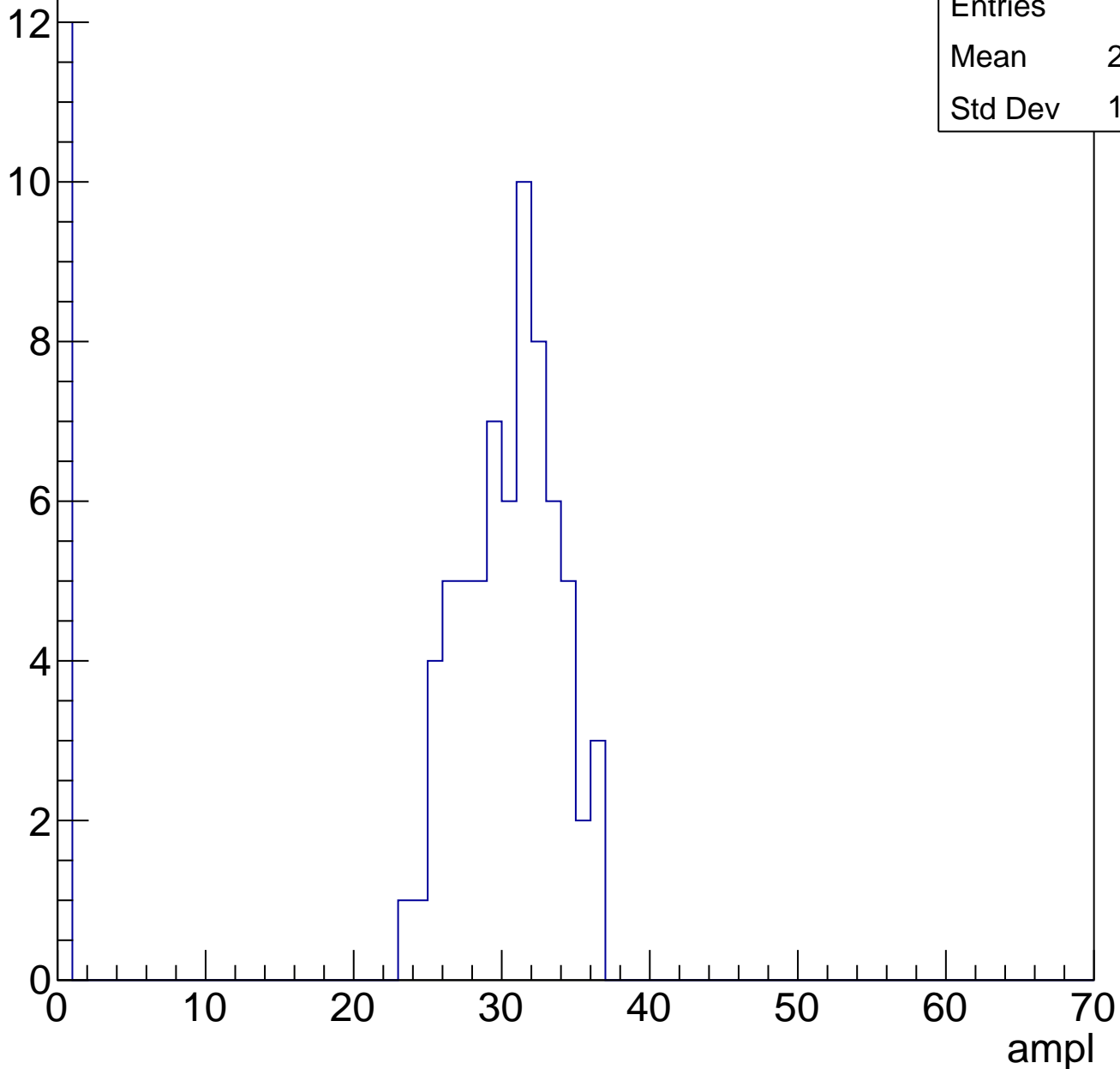
|         |    |
|---------|----|
| Entries | 19 |
| Mean    | 0  |
| Std Dev | 0  |

# B1L103S, U4-ch23, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 80    |
| Mean    | 25.59 |
| Std Dev | 11.13 |

Entry



# B1L103S, U4-ch23, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

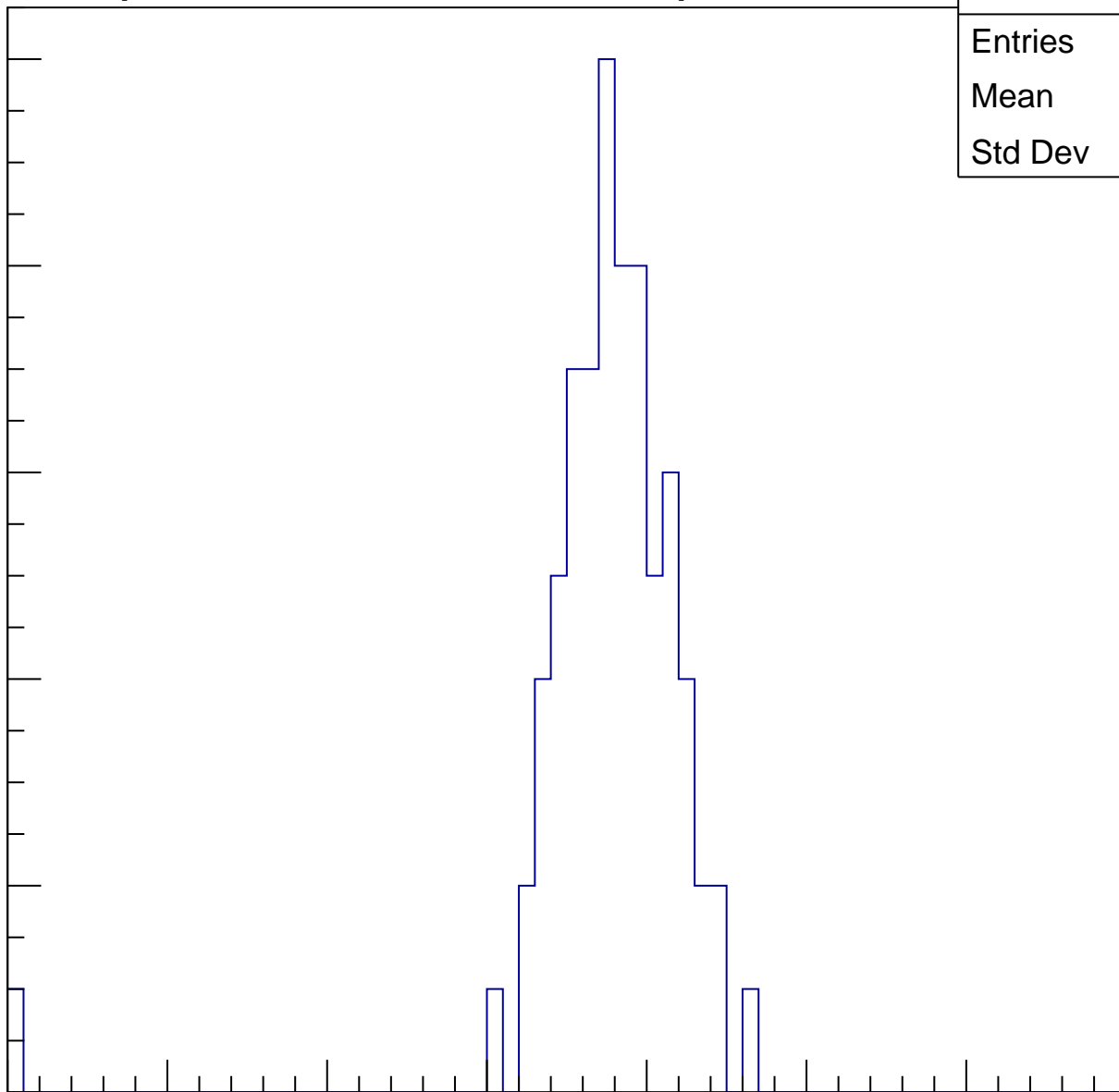
|         |       |
|---------|-------|
| Entries | 73    |
| Mean    | 37.16 |
| Std Dev | 5.417 |

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

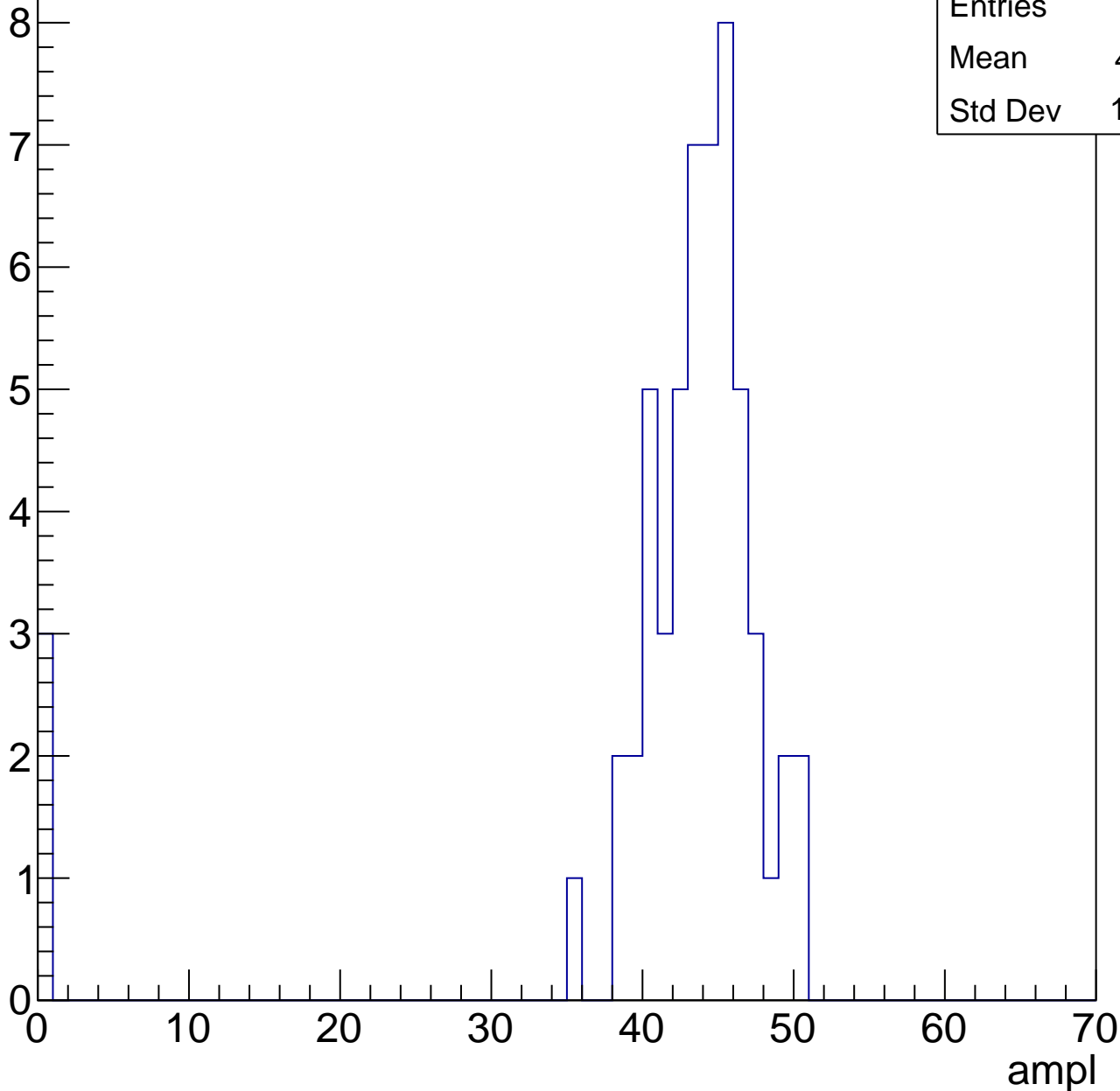


# B1L103S, U4-ch23, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 56    |
| Mean    | 41.21 |
| Std Dev | 10.27 |



# B1L103S, U4-ch23, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 80    |
| Mean    | 43.1  |
| Std Dev | 17.53 |

Entry

10

8

6

4

2

0

0

10

20

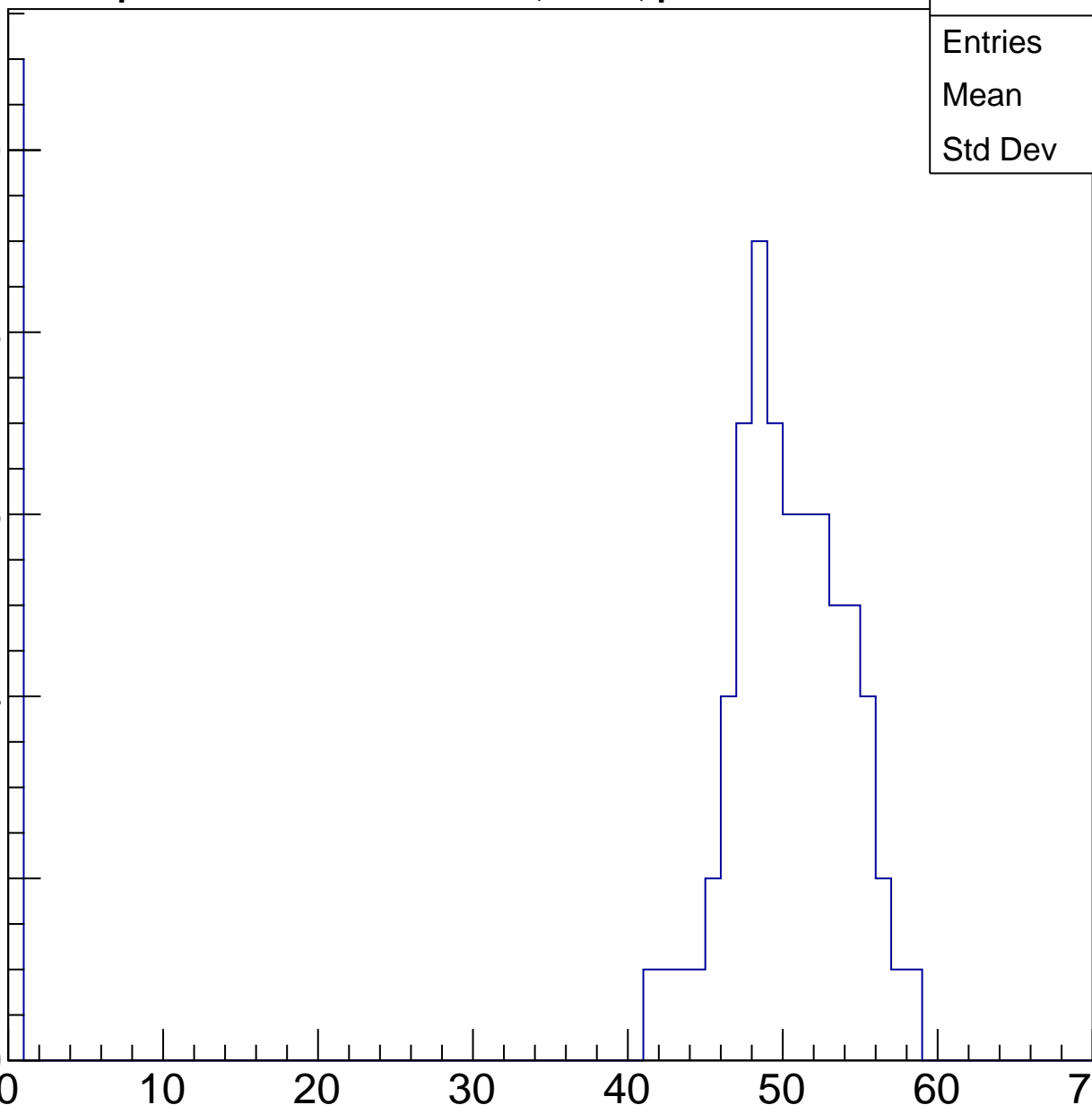
30

40

50

60

ampl

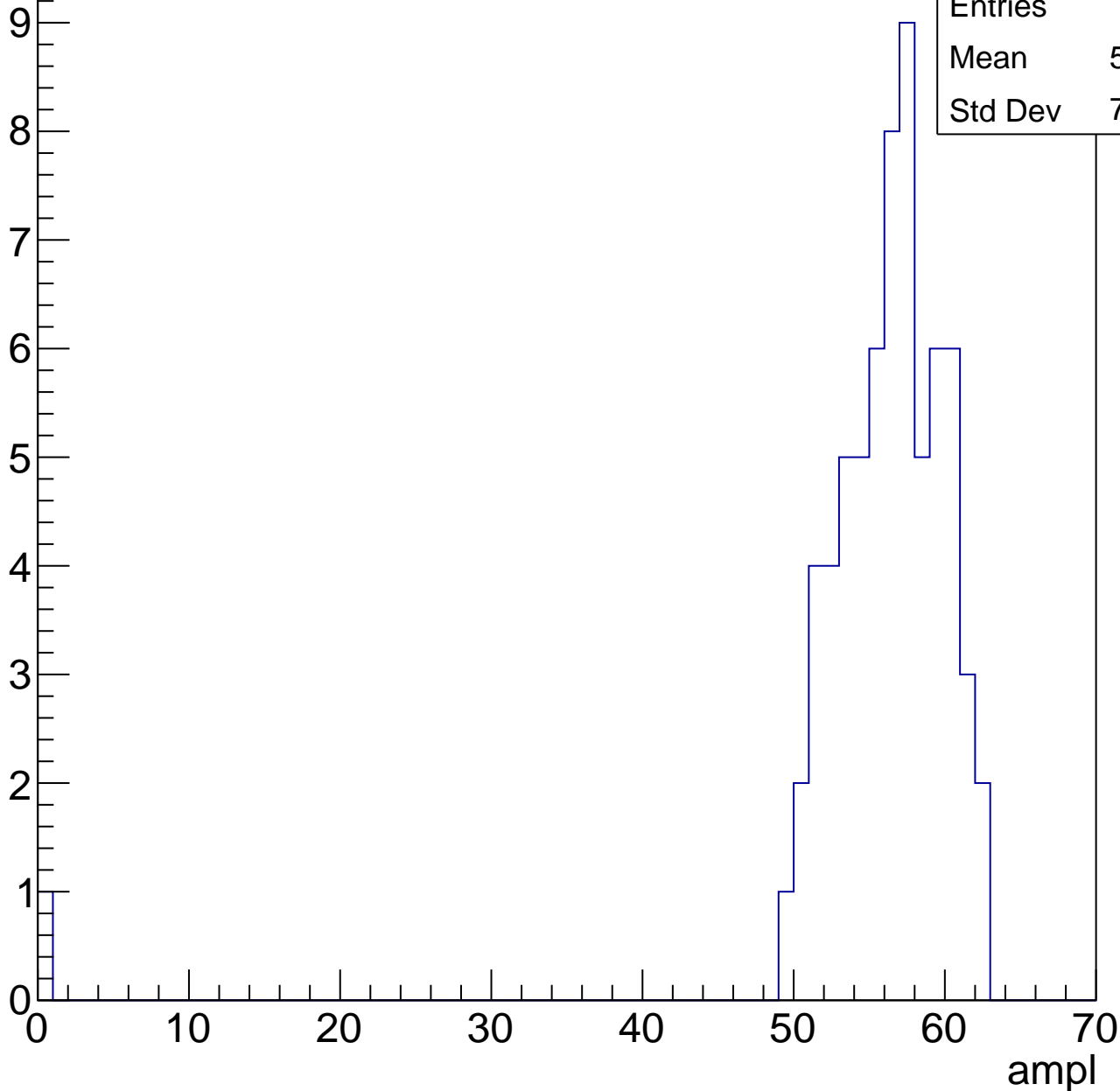


# B1L103S, U4-ch23, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 67    |
| Mean    | 55.19 |
| Std Dev | 7.506 |

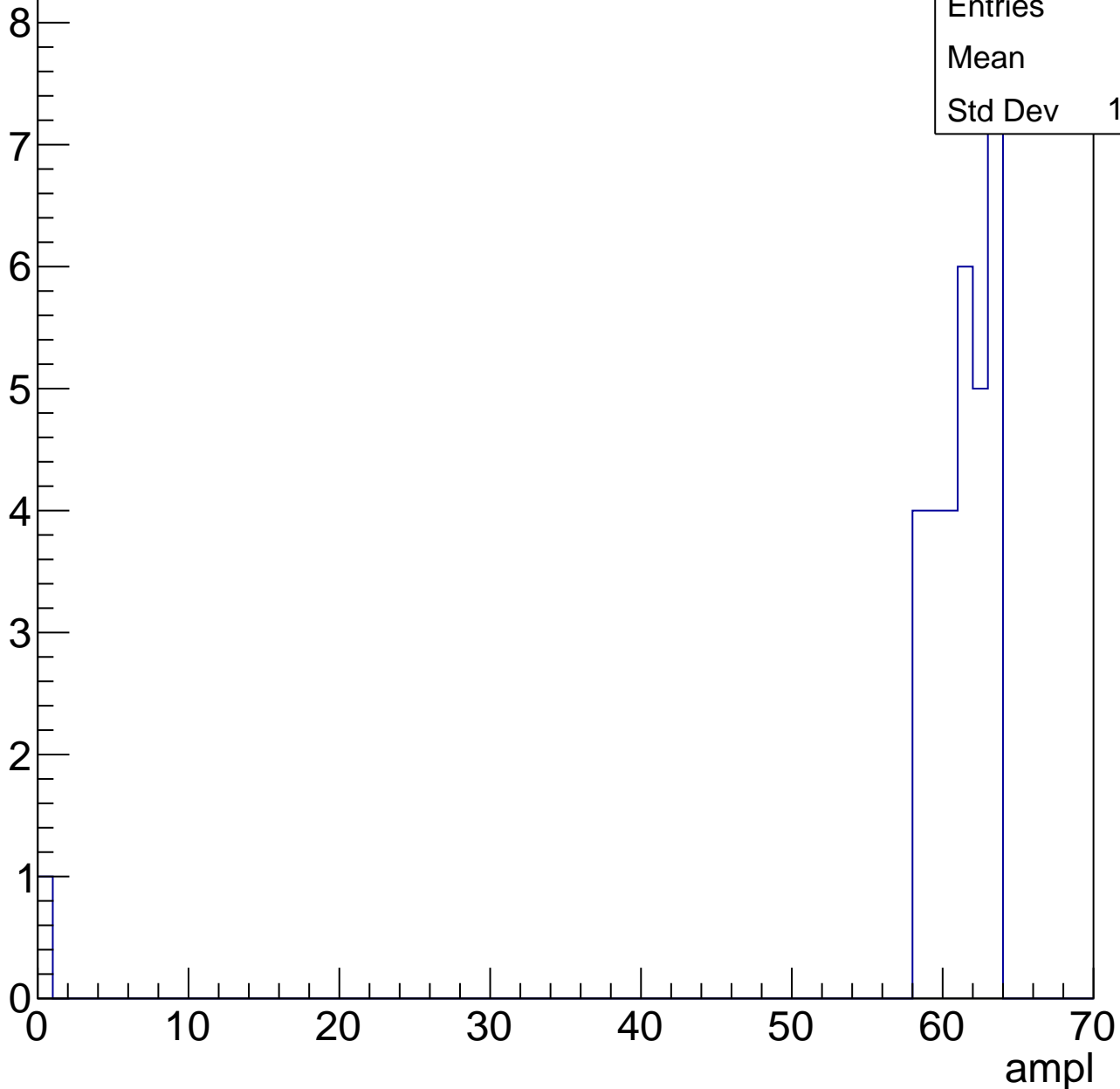


# B1L103S, U4-ch23, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

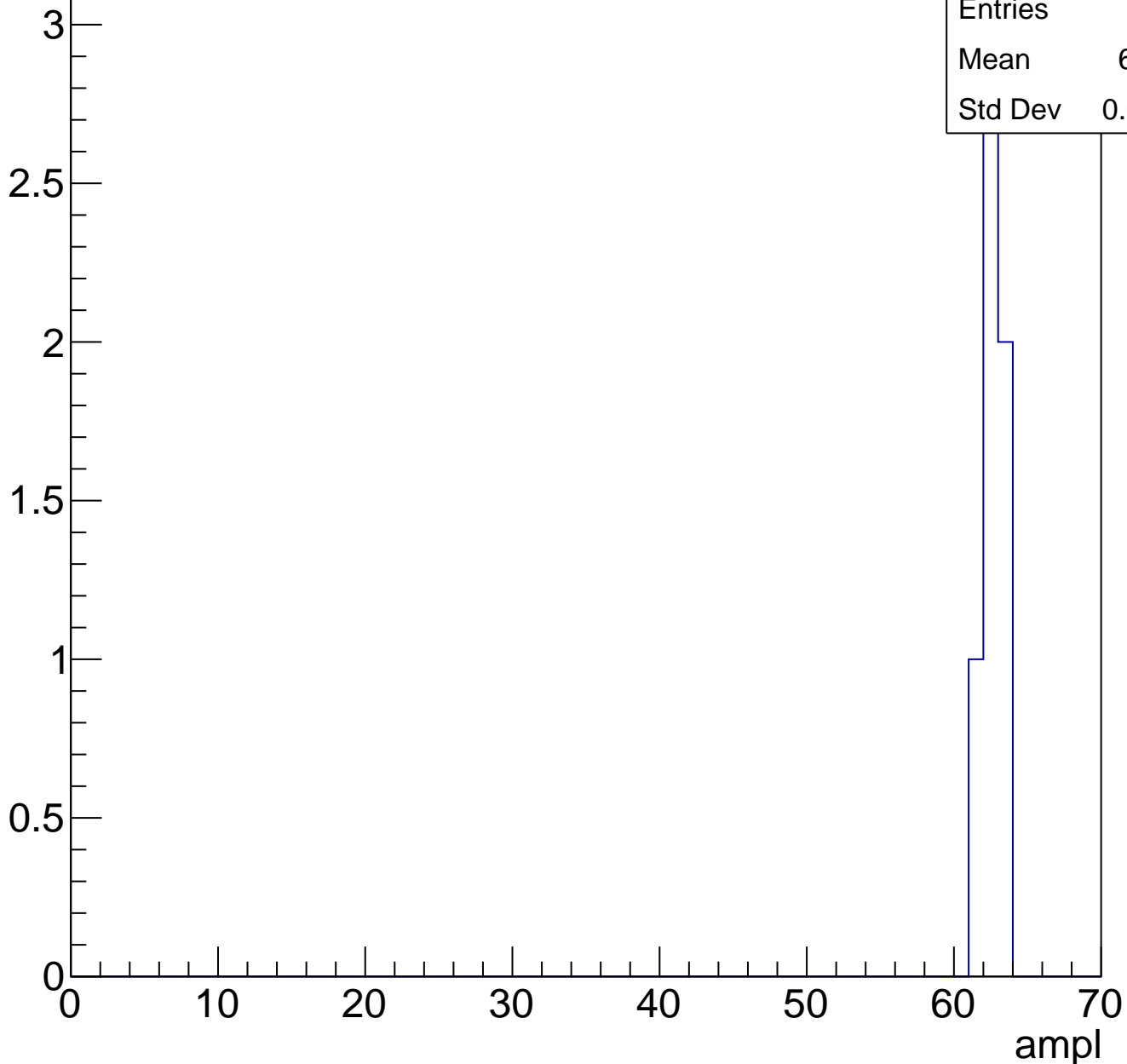
|         |       |
|---------|-------|
| Entries | 32    |
| Mean    | 59    |
| Std Dev | 10.73 |



# B1L103S, U4-ch23, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U4-ch23, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

|         |    |
|---------|----|
| Entries | 19 |
| Mean    | 0  |
| Std Dev | 0  |

# B1L103S, U4-ch24, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 92    |
| Mean    | 23.92 |
| Std Dev | 10.3  |

Entry

12

10

8

6

4

2

0

0

10

20

30

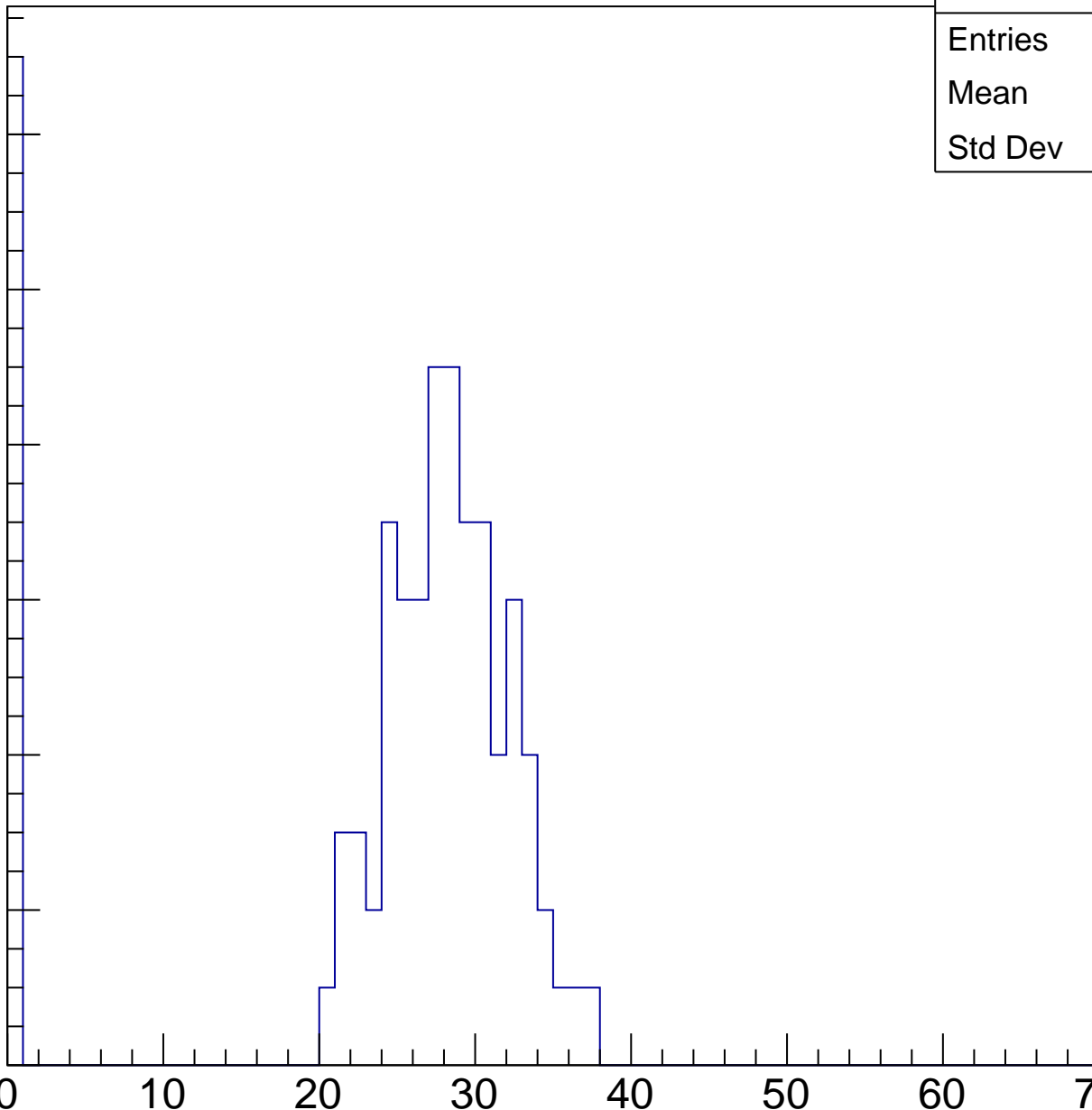
40

50

60

70

ampl

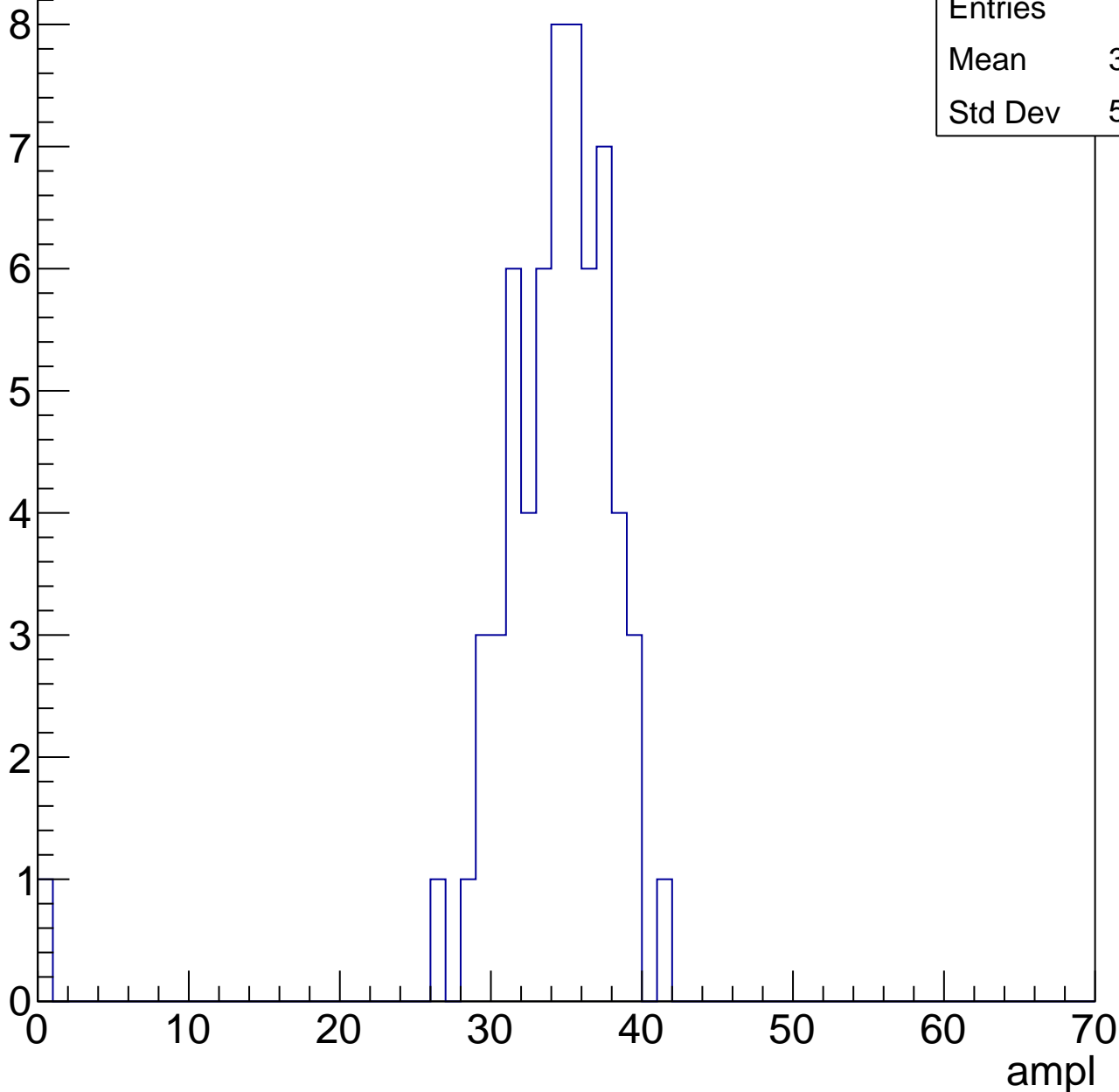


# B1L103S, U4-ch24, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 62    |
| Mean    | 33.55 |
| Std Dev | 5.275 |

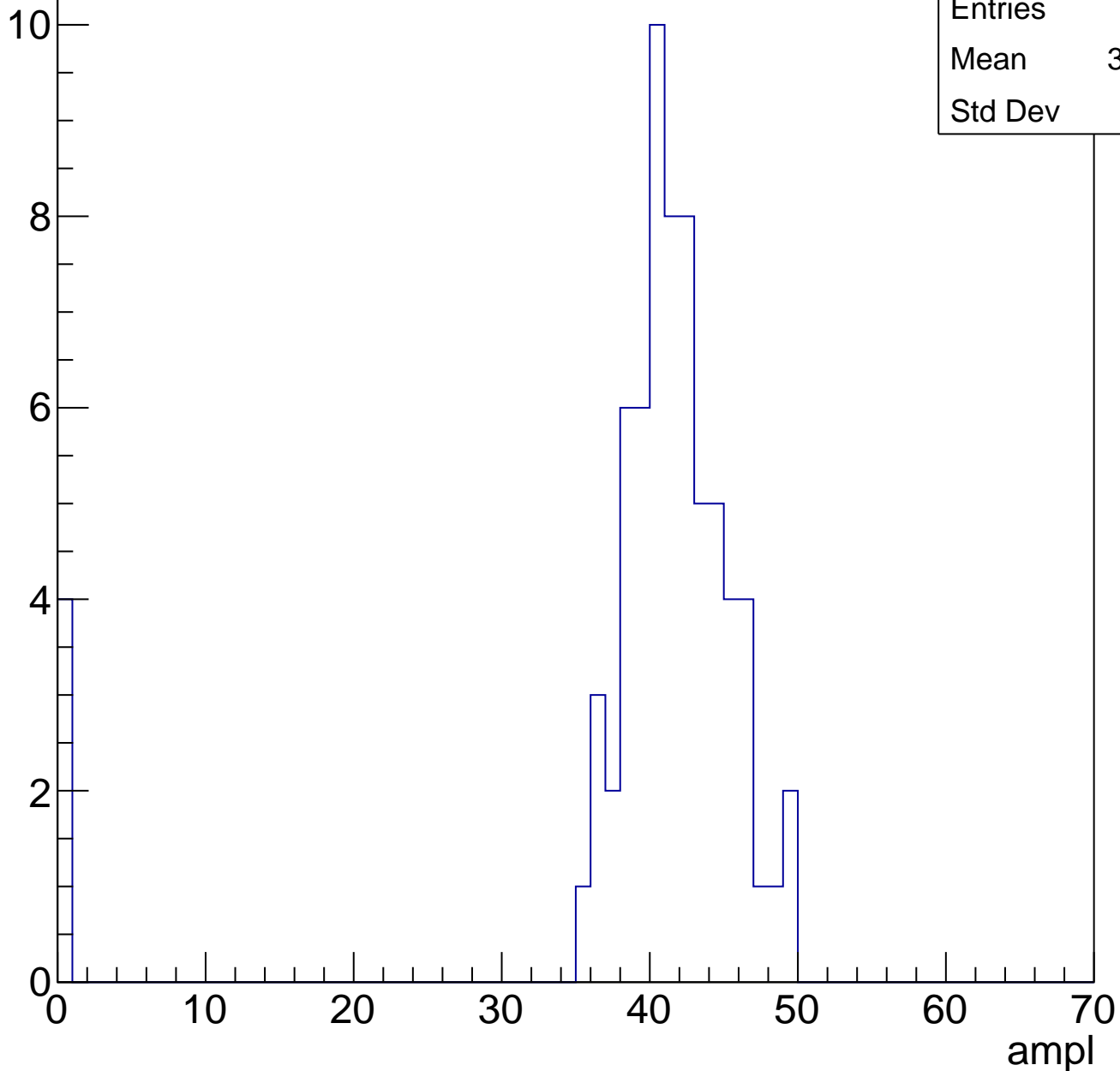


# B1L103S, U4-ch24, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 70    |
| Mean    | 39.07 |
| Std Dev | 10.1  |

Entry

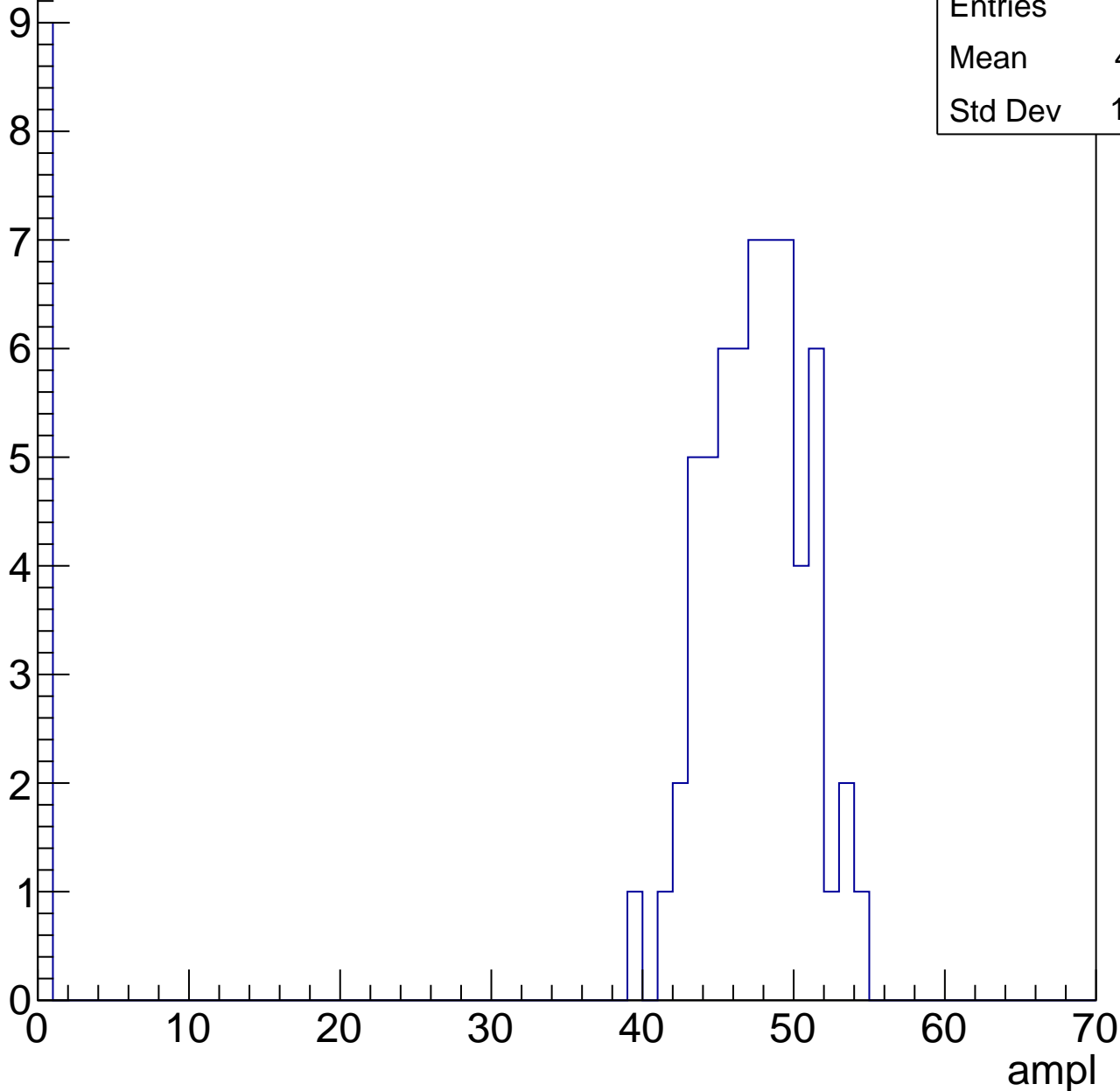


# B1L103S, U4-ch24, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 70    |
| Mean    | 41.01 |
| Std Dev | 16.03 |

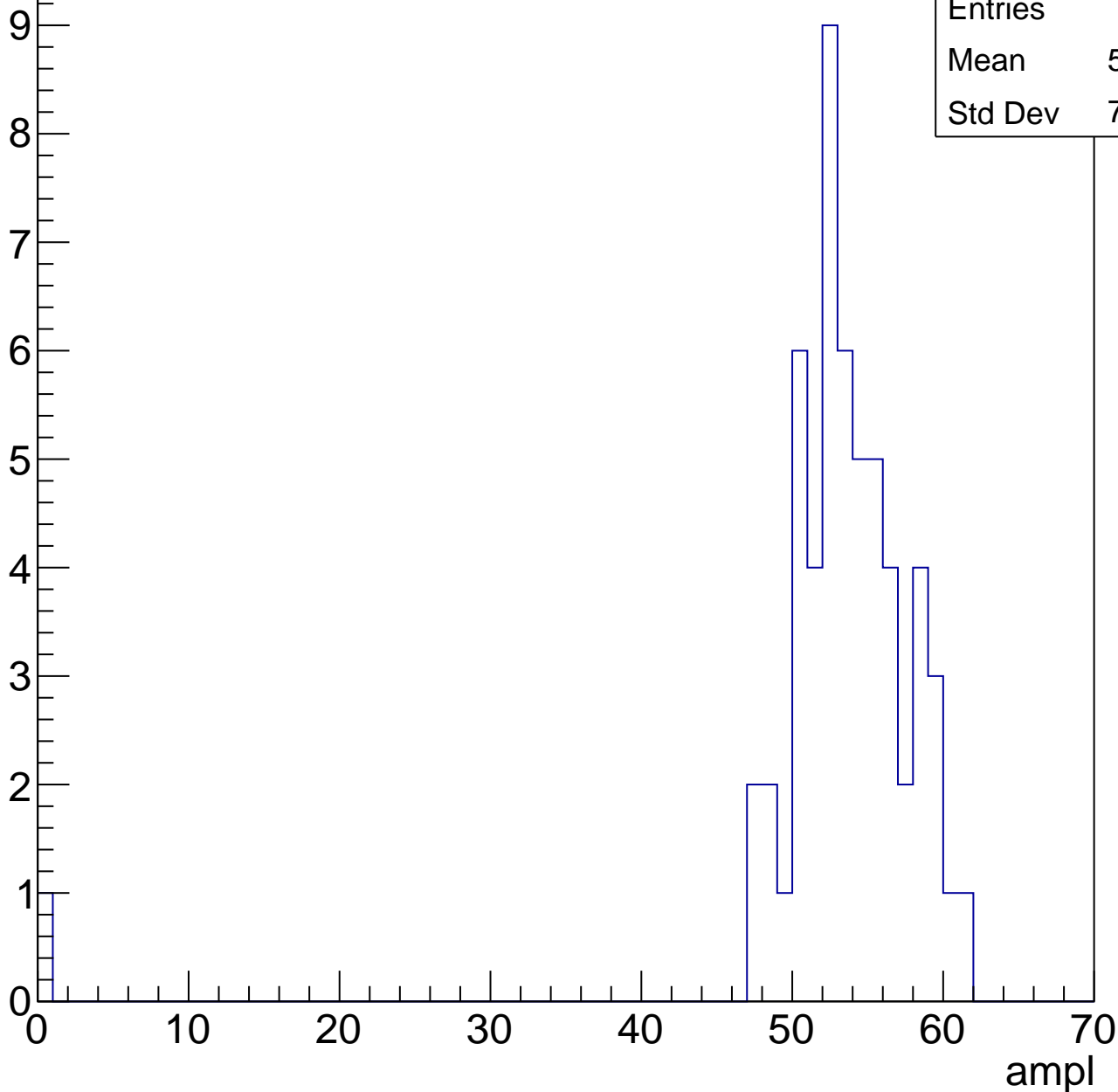


# B1L103S, U4-ch24, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

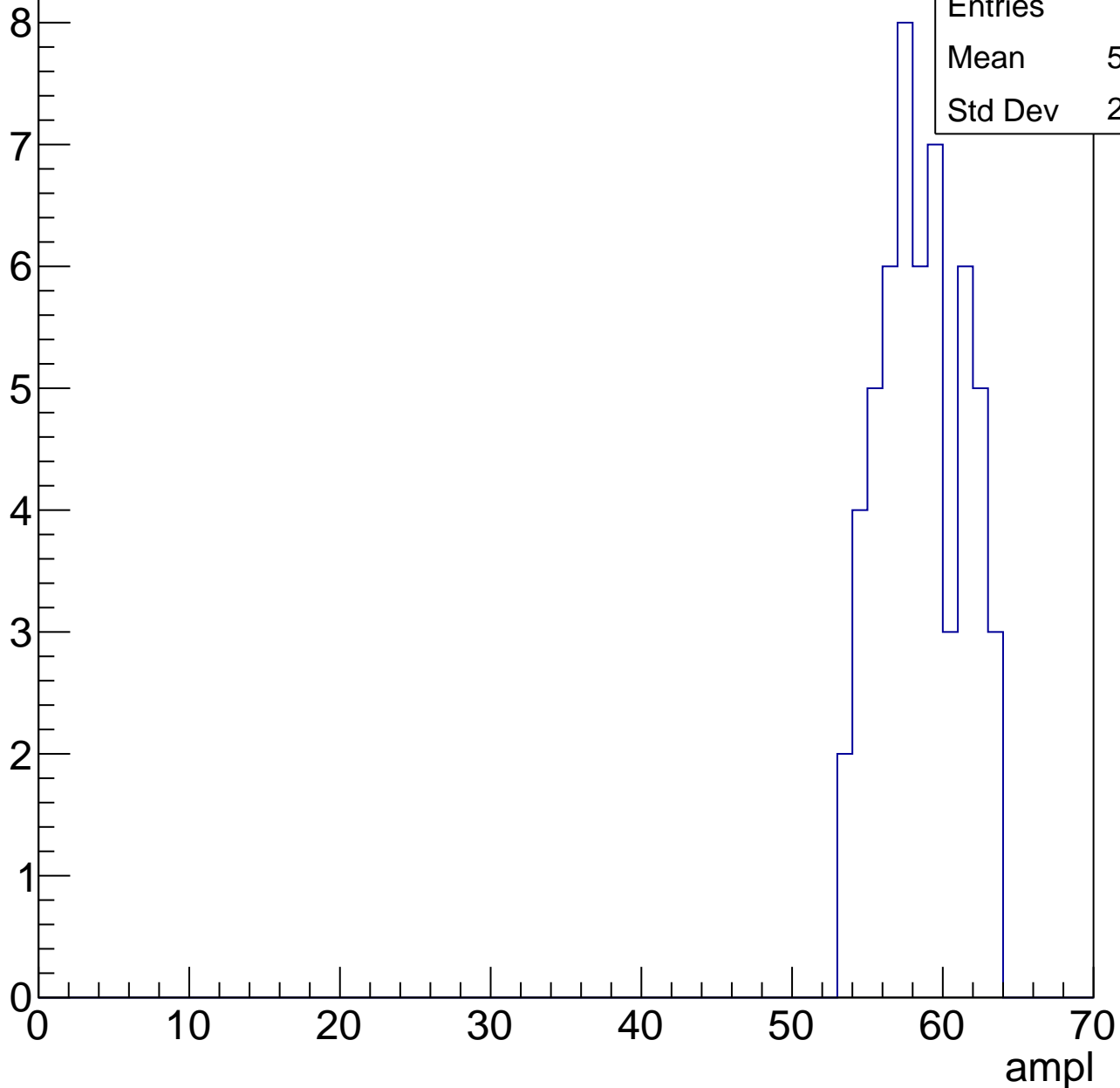
|         |       |
|---------|-------|
| Entries | 56    |
| Mean    | 52.54 |
| Std Dev | 7.824 |



# B1L103S, U4-ch24, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

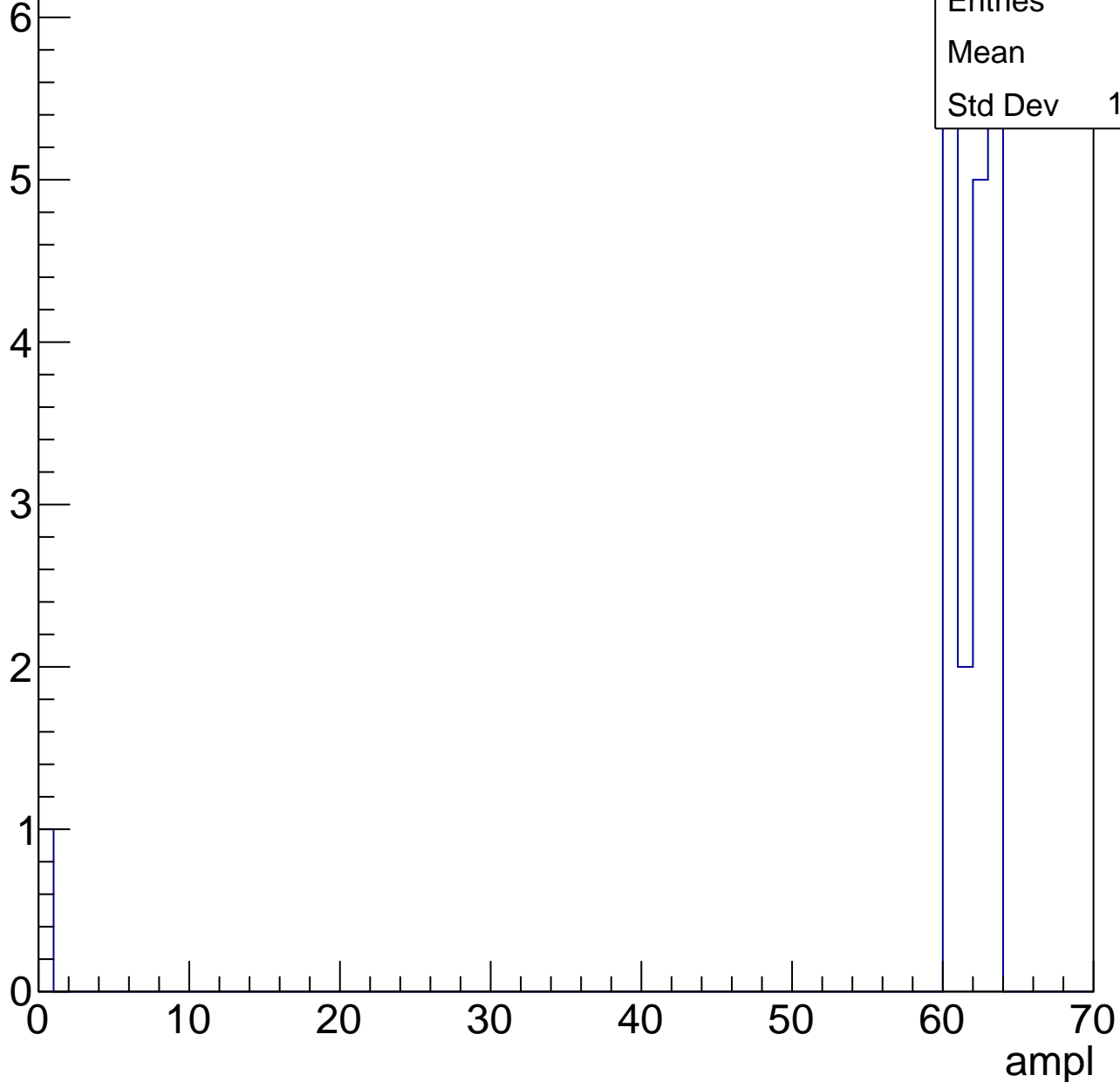


|         |       |
|---------|-------|
| Entries | 55    |
| Mean    | 58.09 |
| Std Dev | 2.759 |

# B1L103S, U4-ch24, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

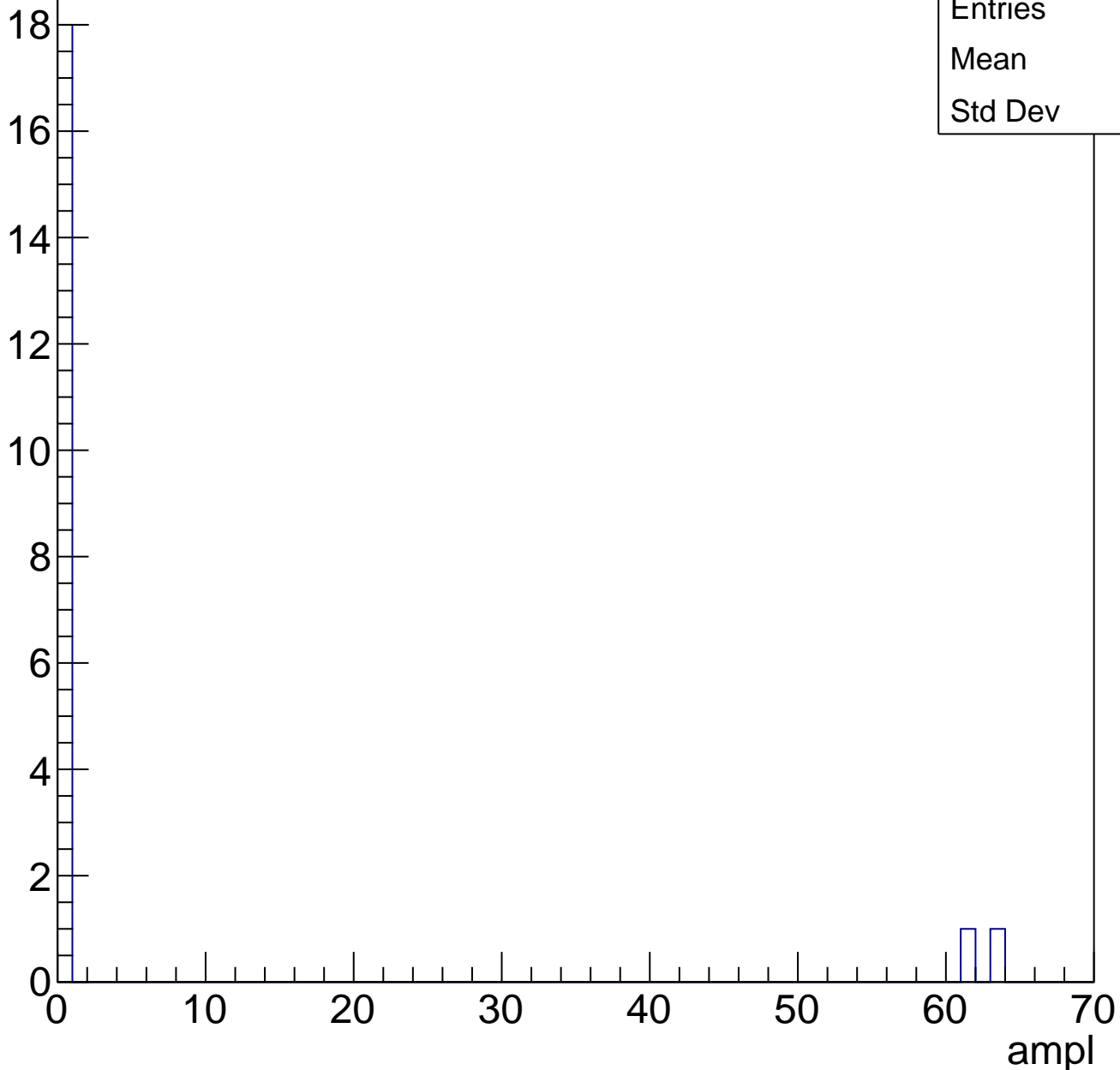




# B1L103S, U4-ch24, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



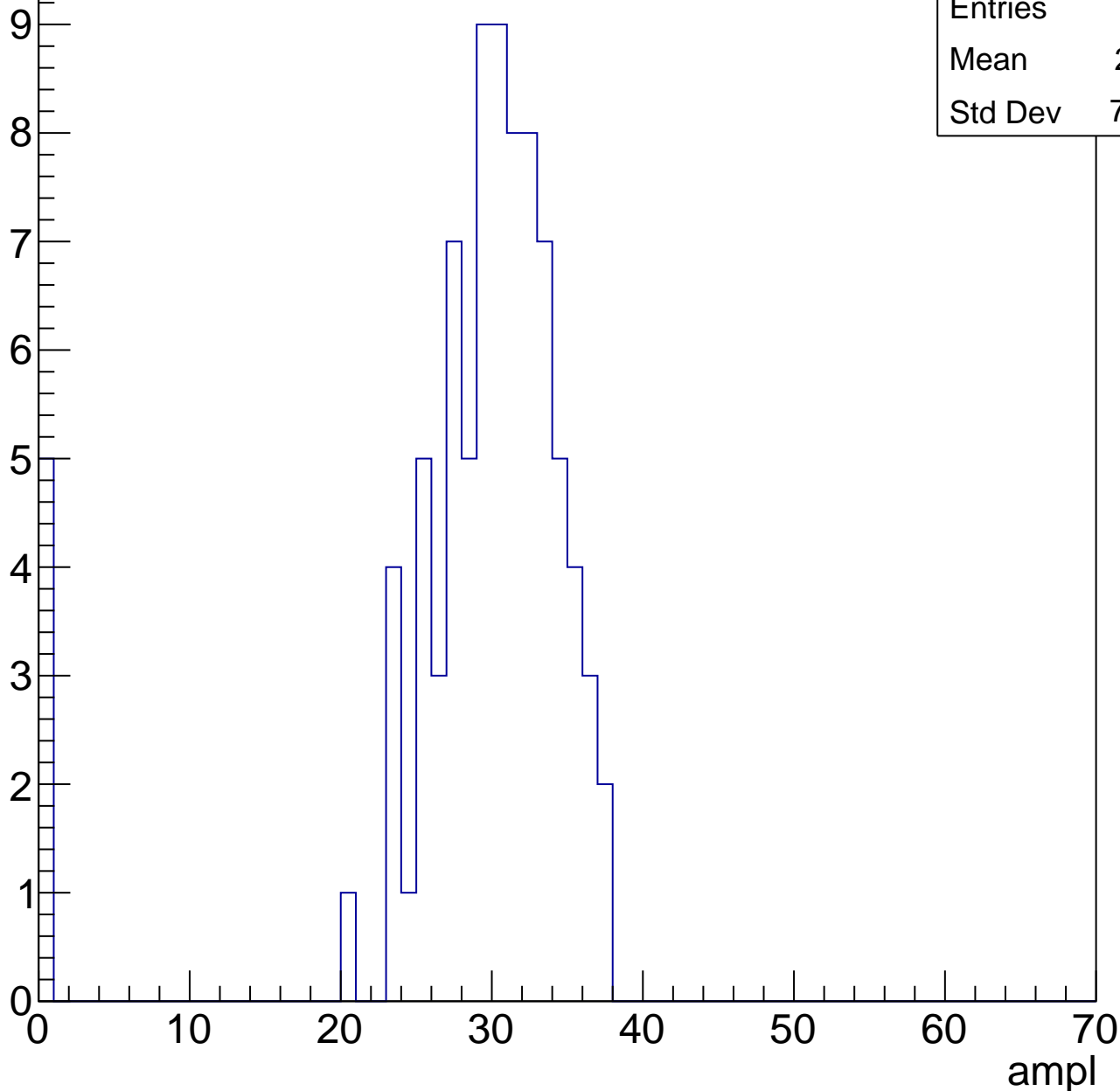
|         |      |
|---------|------|
| Entries | 20   |
| Mean    | 6.2  |
| Std Dev | 18.6 |

# B1L103S, U4-ch25, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 86    |
| Mean    | 28.21 |
| Std Dev | 7.858 |



# B1L103S, U4-ch25, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

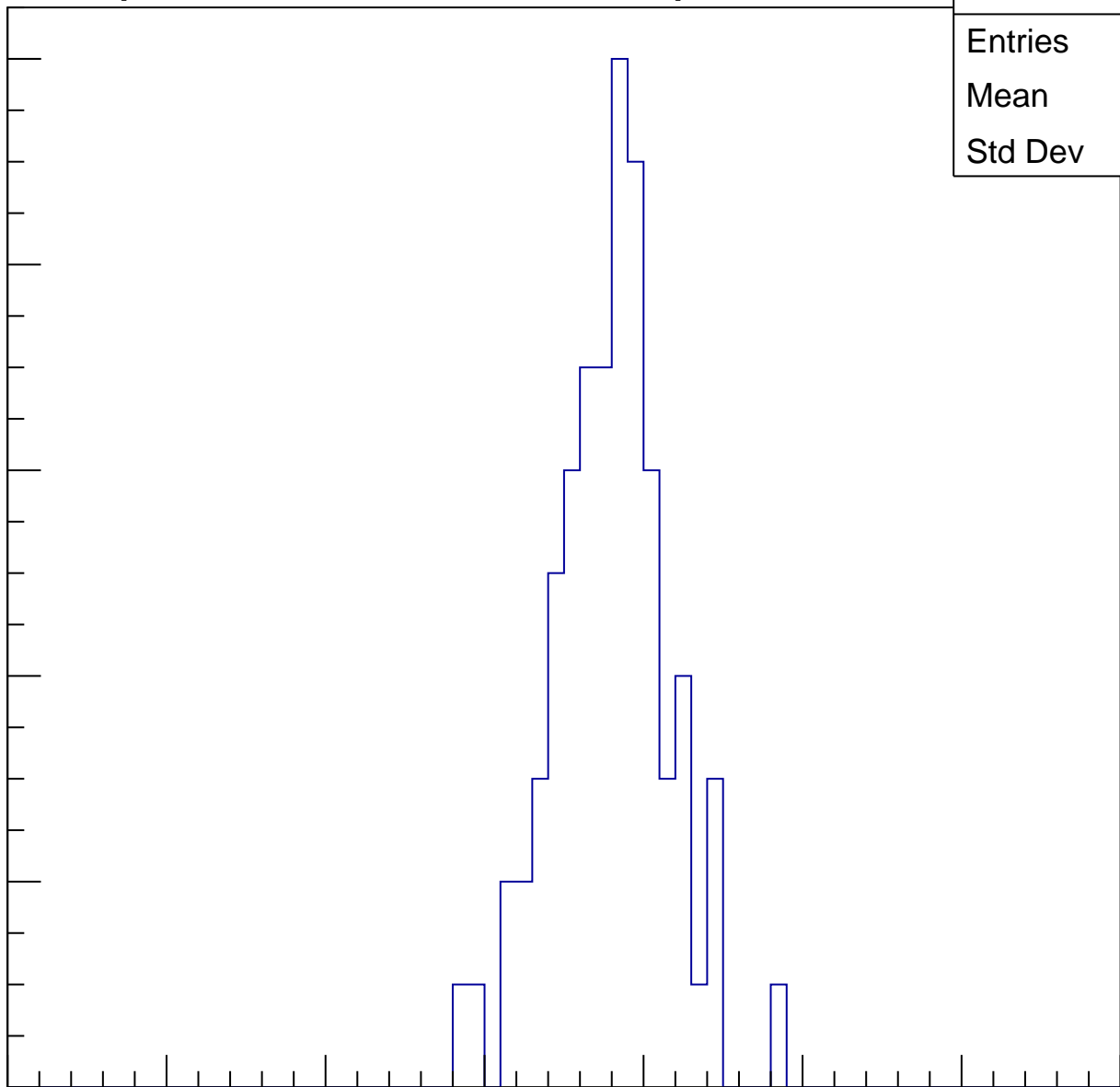
|         |       |
|---------|-------|
| Entries | 71    |
| Mean    | 37.44 |
| Std Dev | 3.618 |

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

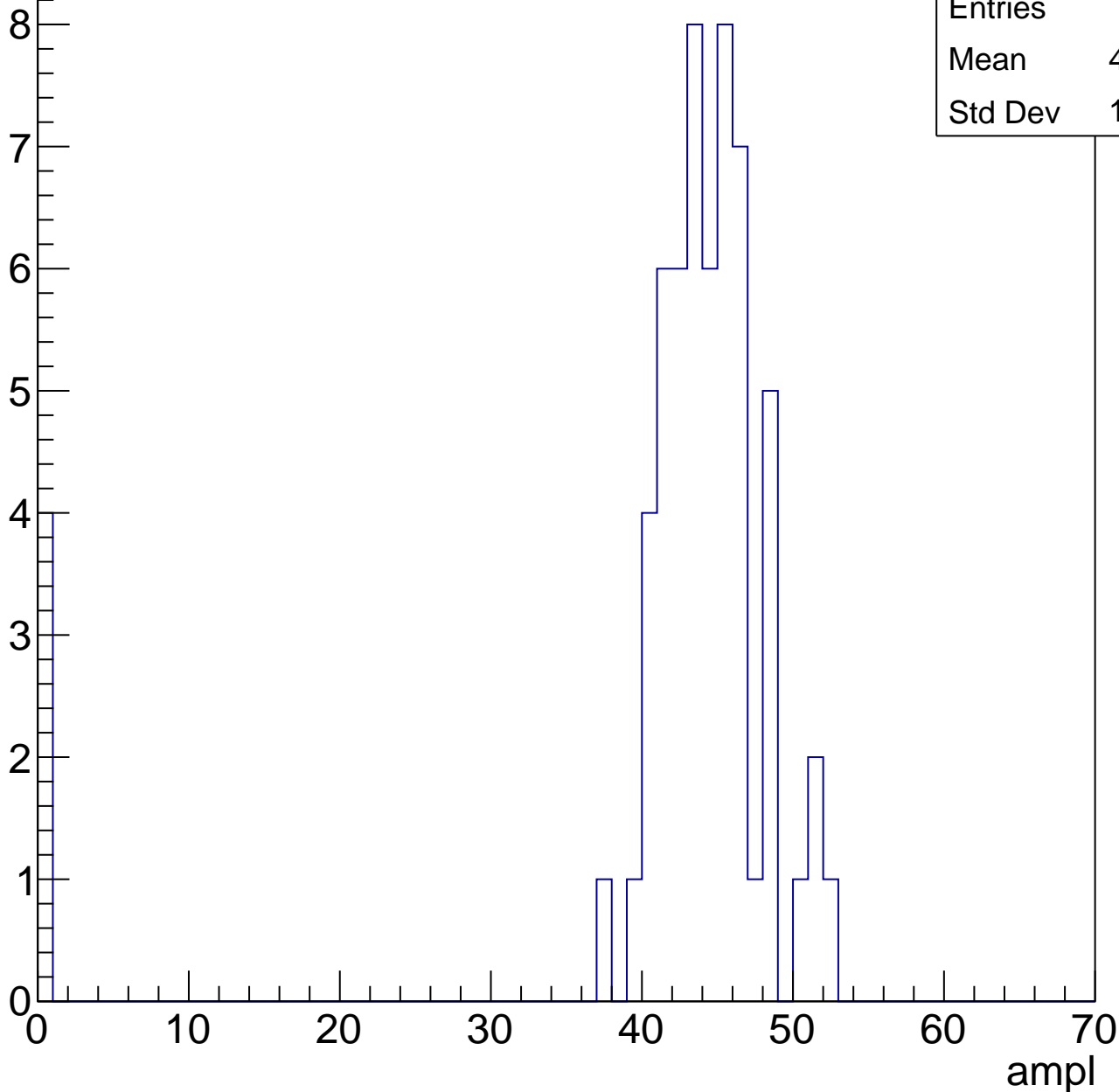


# B1L103S, U4-ch25, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 61    |
| Mean    | 41.23 |
| Std Dev | 11.32 |

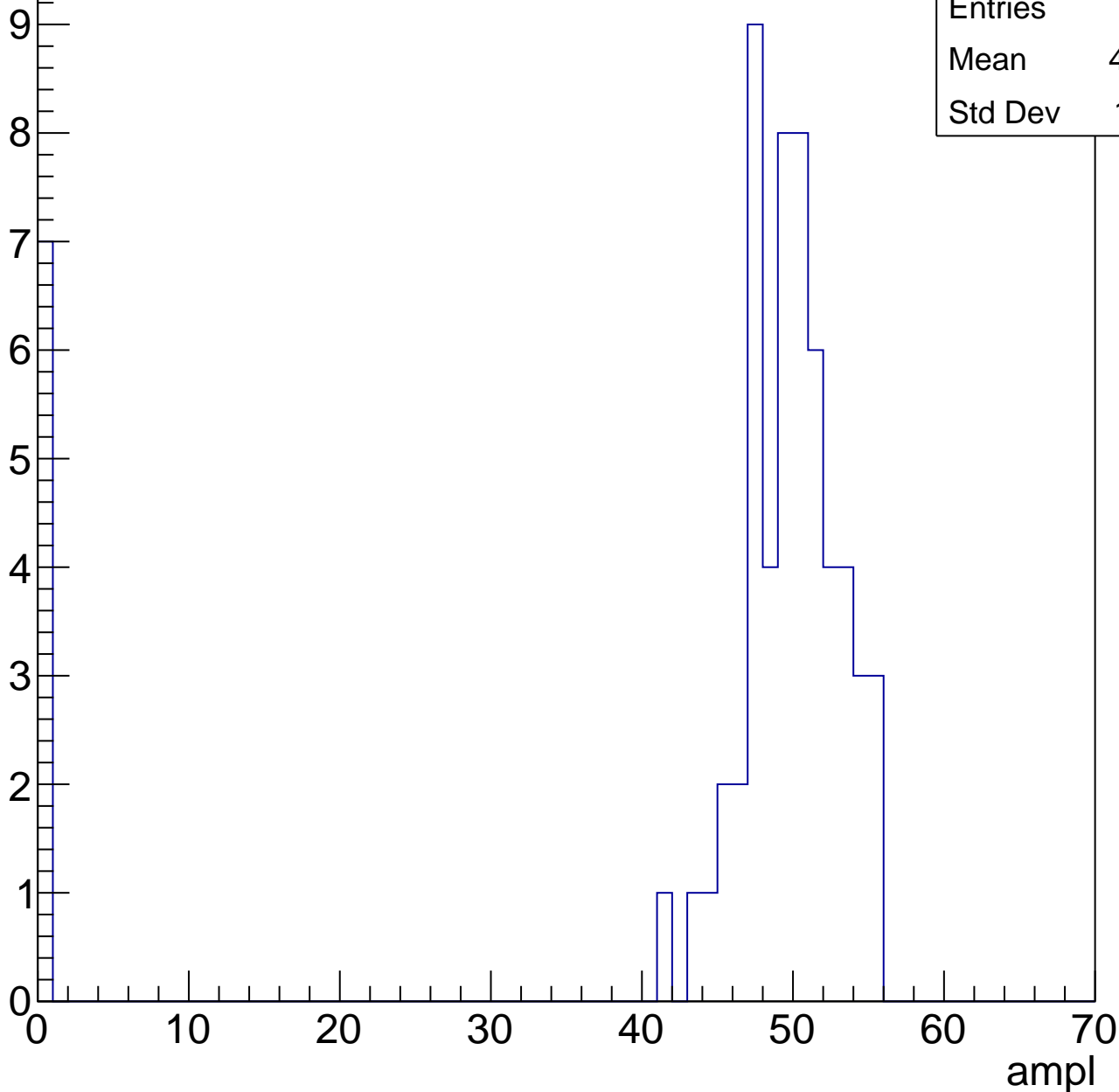


# B1L103S, U4-ch25, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 63    |
| Mean    | 43.97 |
| Std Dev | 15.81 |

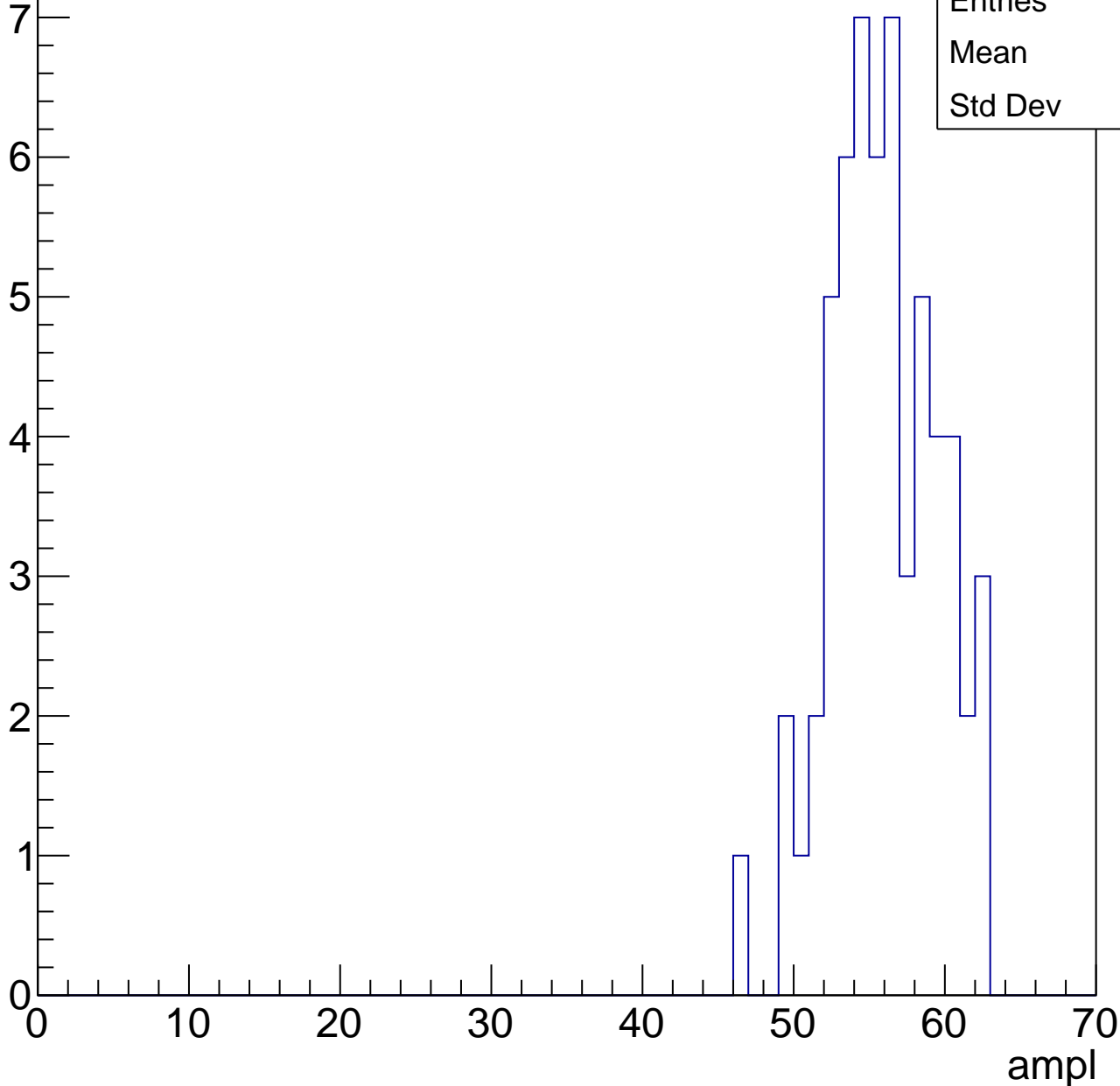


# B1L103S, U4-ch25, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |      |
|---------|------|
| Entries | 58   |
| Mean    | 55.5 |
| Std Dev | 3.52 |

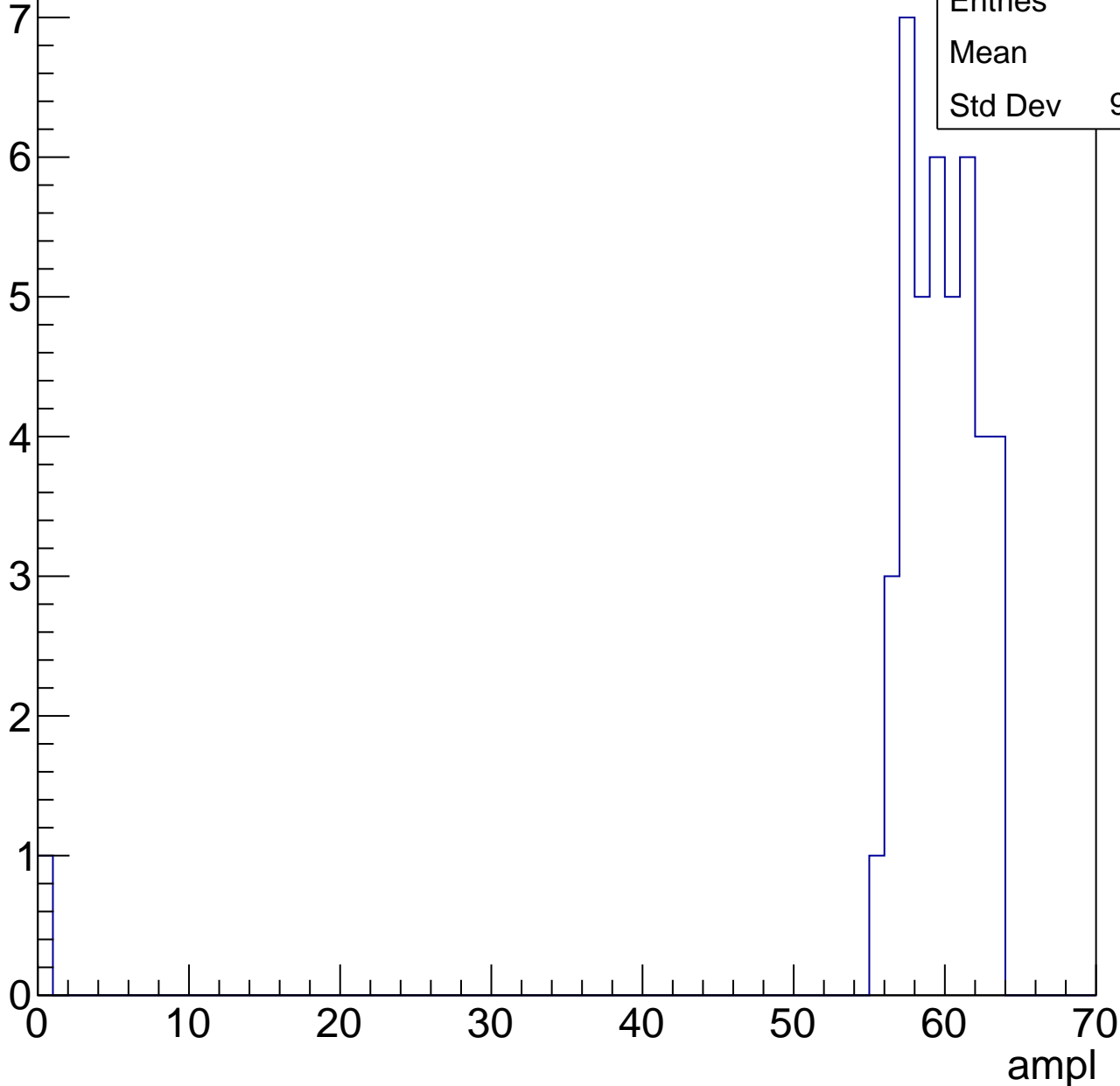


# B1L103S, U4-ch25, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 42    |
| Mean    | 57.9  |
| Std Dev | 9.304 |

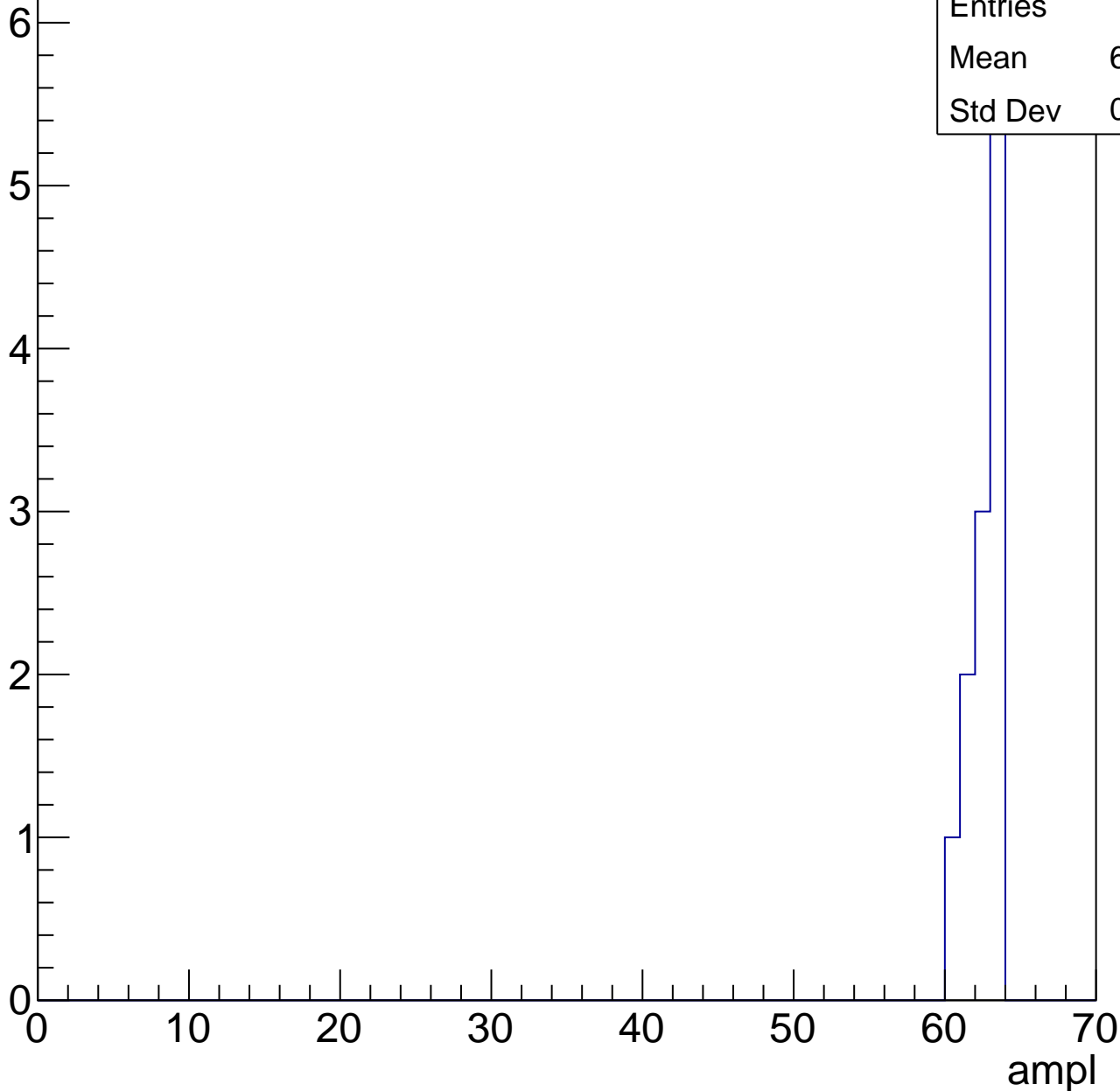


# B1L103S, U4-ch25, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 12    |
| Mean    | 62.17 |
| Std Dev | 0.986 |





# B1L103S, U4-ch25, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

|         |    |
|---------|----|
| Entries | 19 |
| Mean    | 0  |
| Std Dev | 0  |

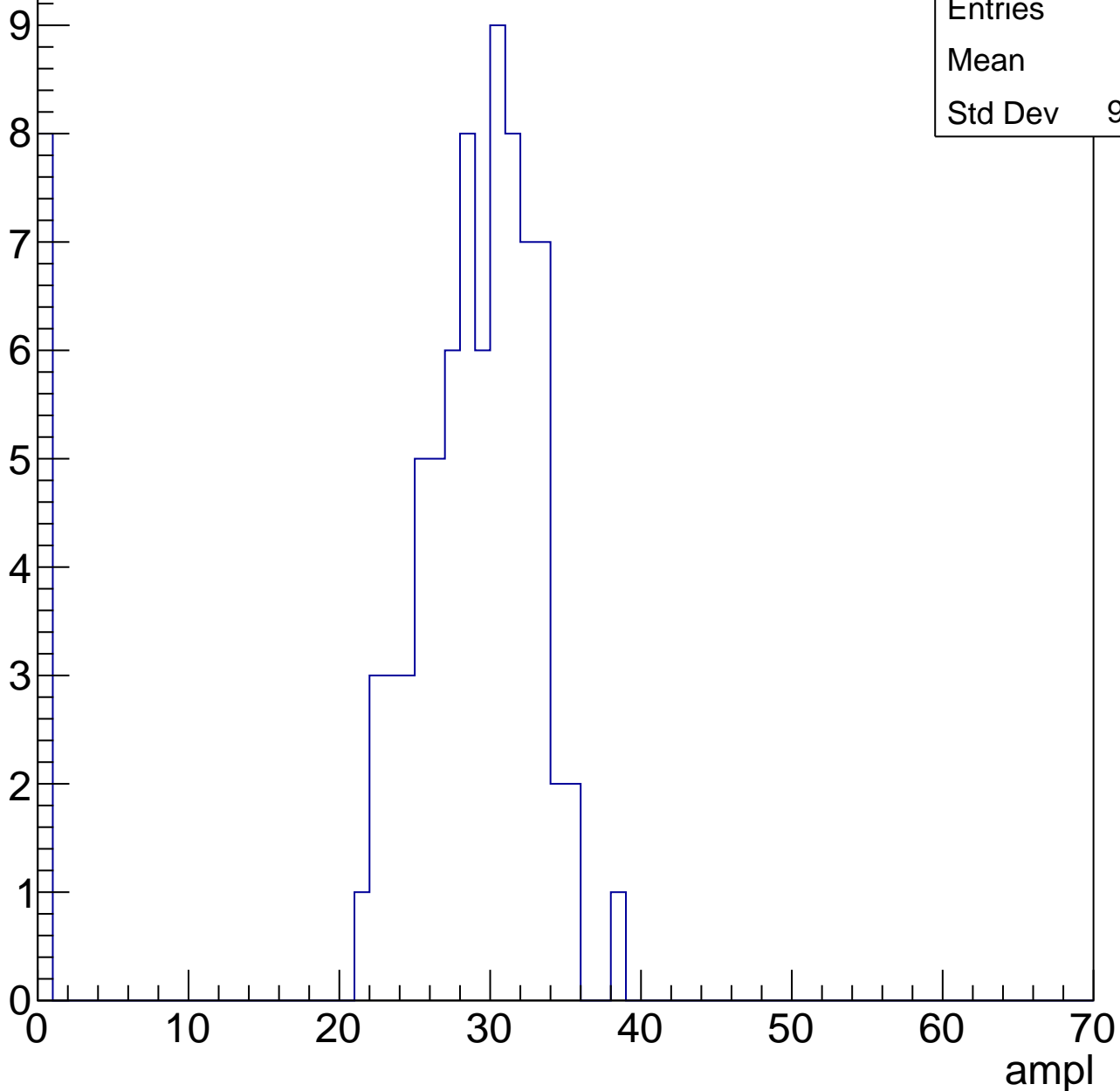
ampl

# B1L103S, U4-ch26, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 84    |
| Mean    | 26.1  |
| Std Dev | 9.122 |

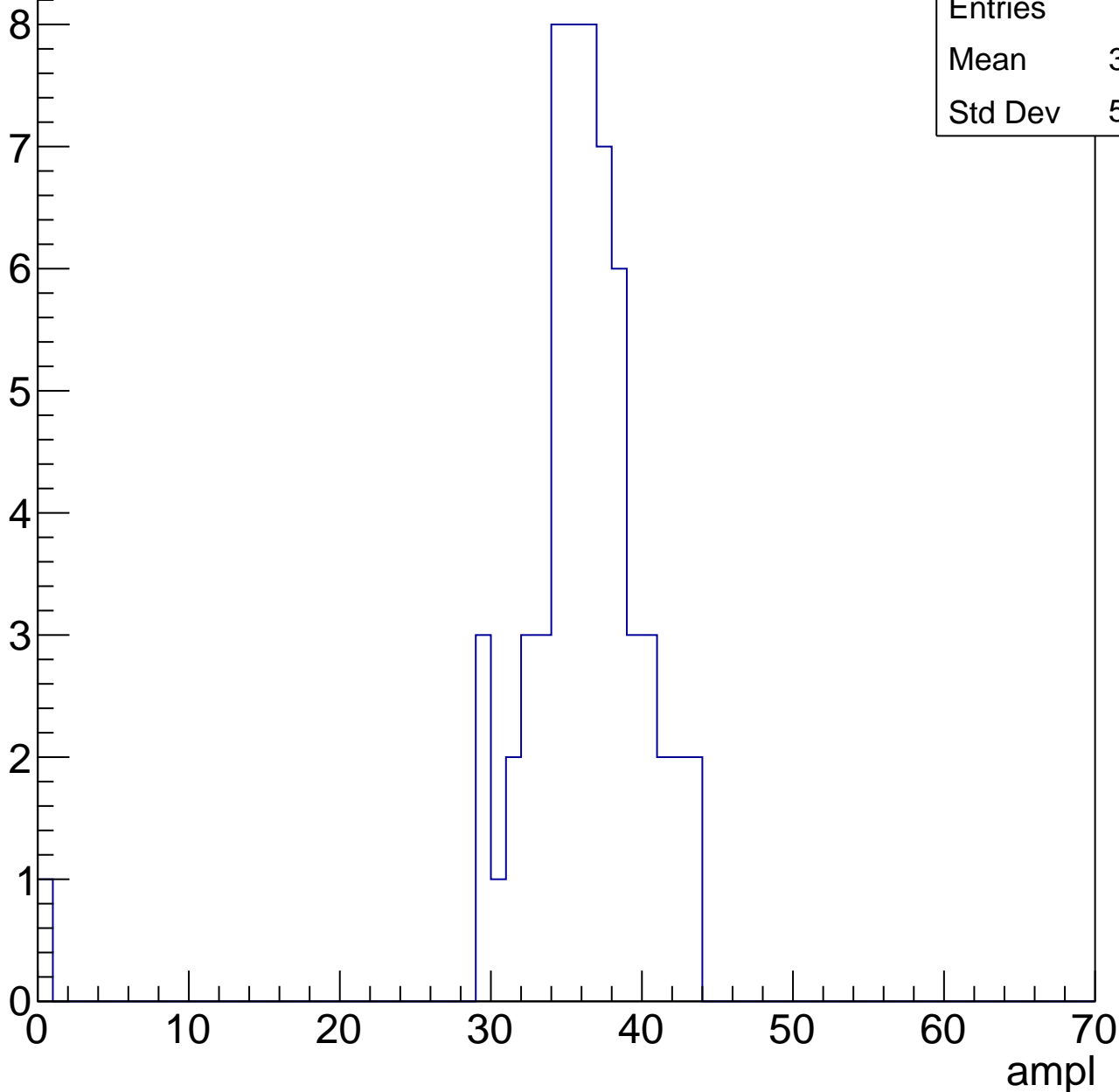


# B1L103S, U4-ch26, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 62    |
| Mean    | 35.32 |
| Std Dev | 5.596 |

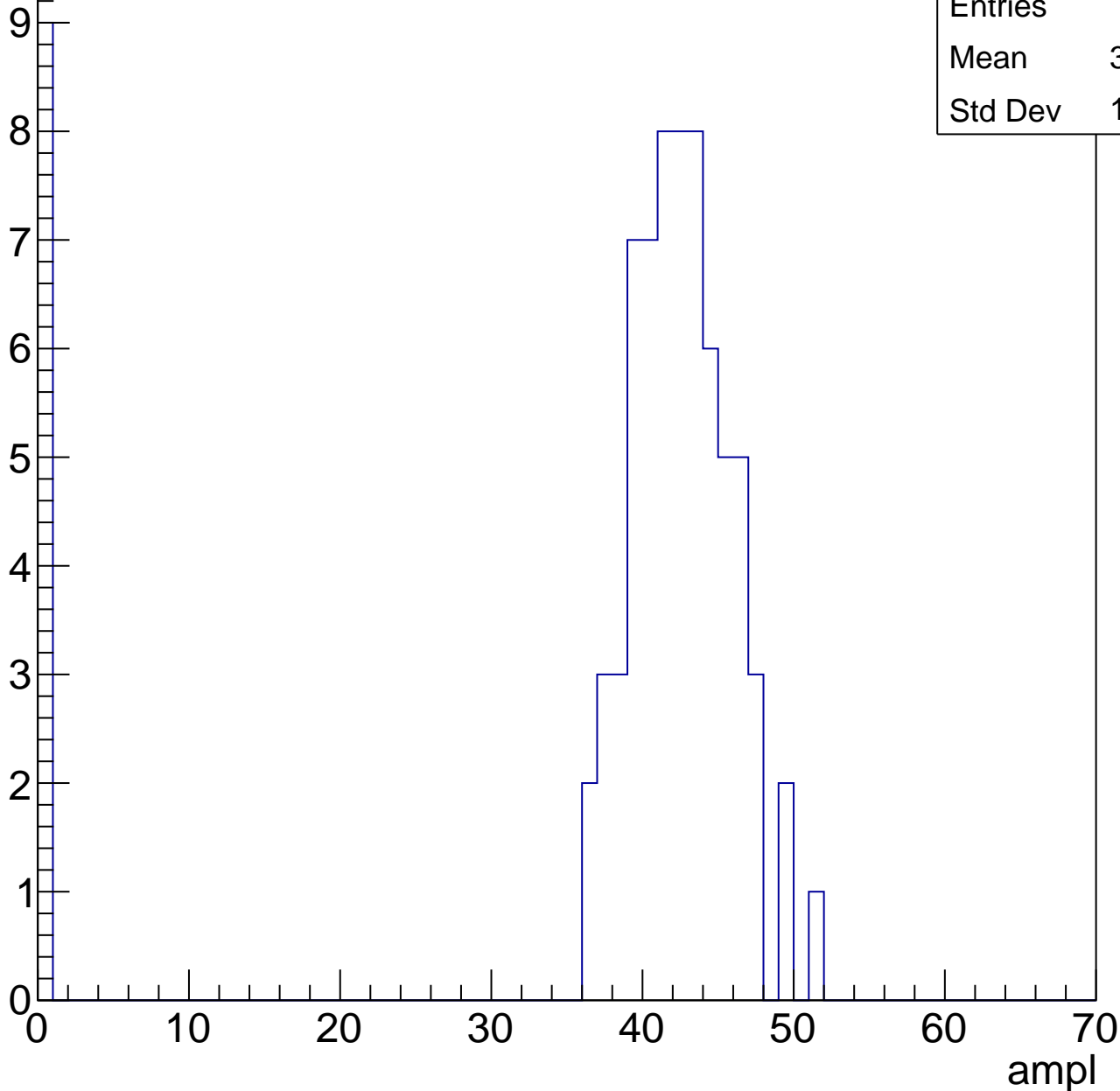


# B1L103S, U4-ch26, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 77    |
| Mean    | 37.23 |
| Std Dev | 13.88 |

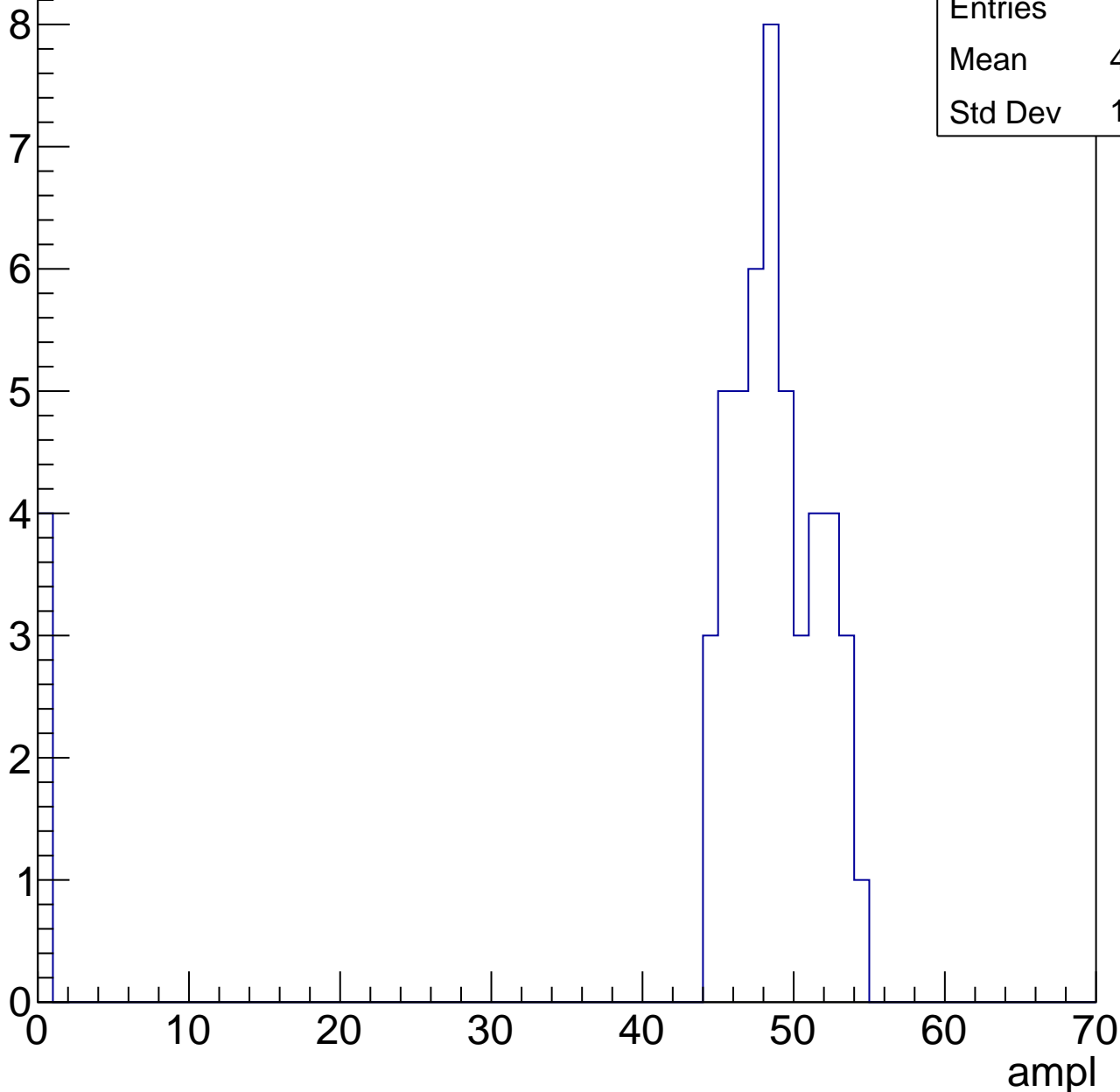


# B1L103S, U4-ch26, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 51    |
| Mean    | 44.57 |
| Std Dev | 13.26 |

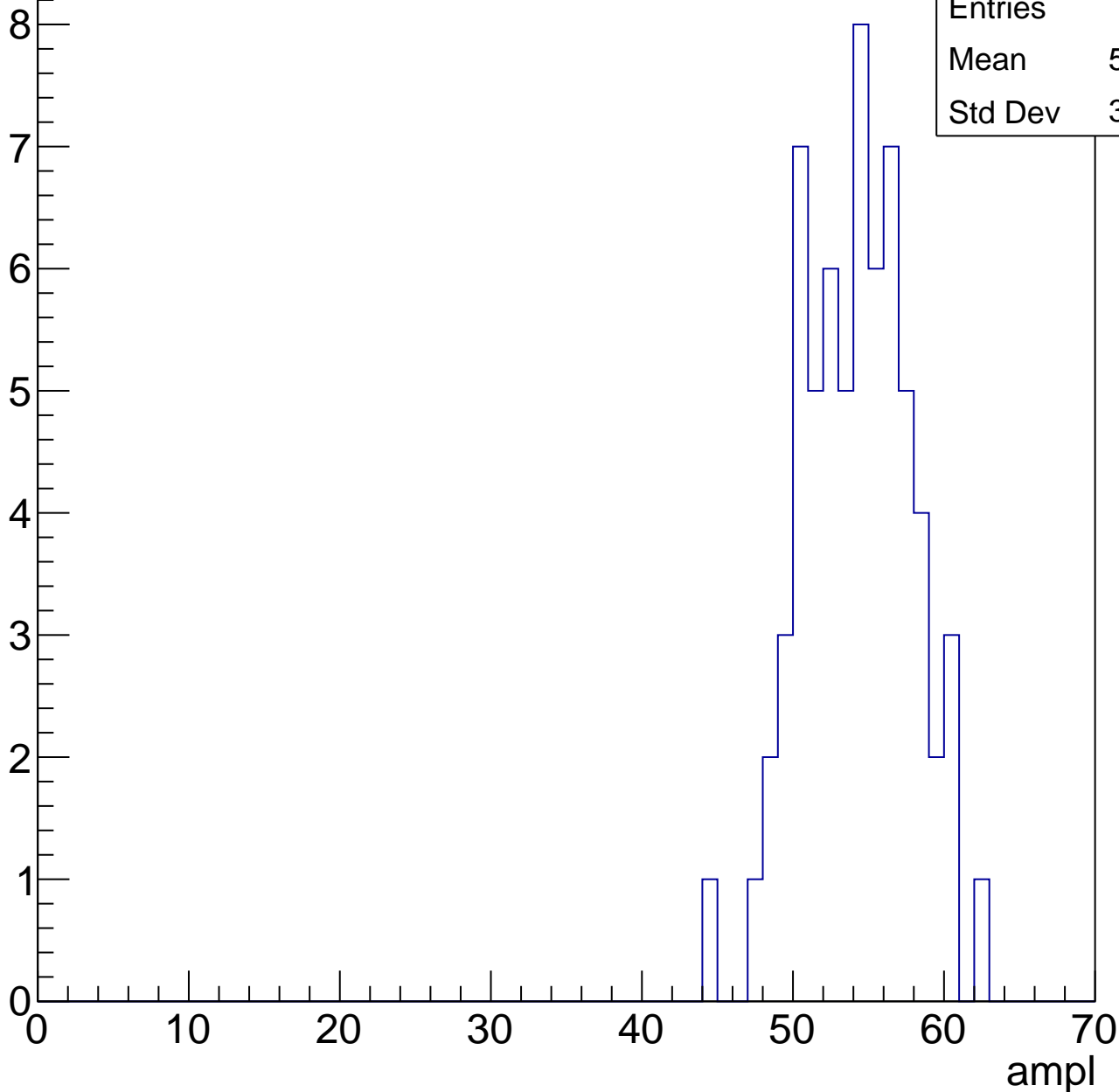


# B1L103S, U4-ch26, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 66    |
| Mean    | 53.74 |
| Std Dev | 3.573 |



# B1L103S, U4-ch26, adc5

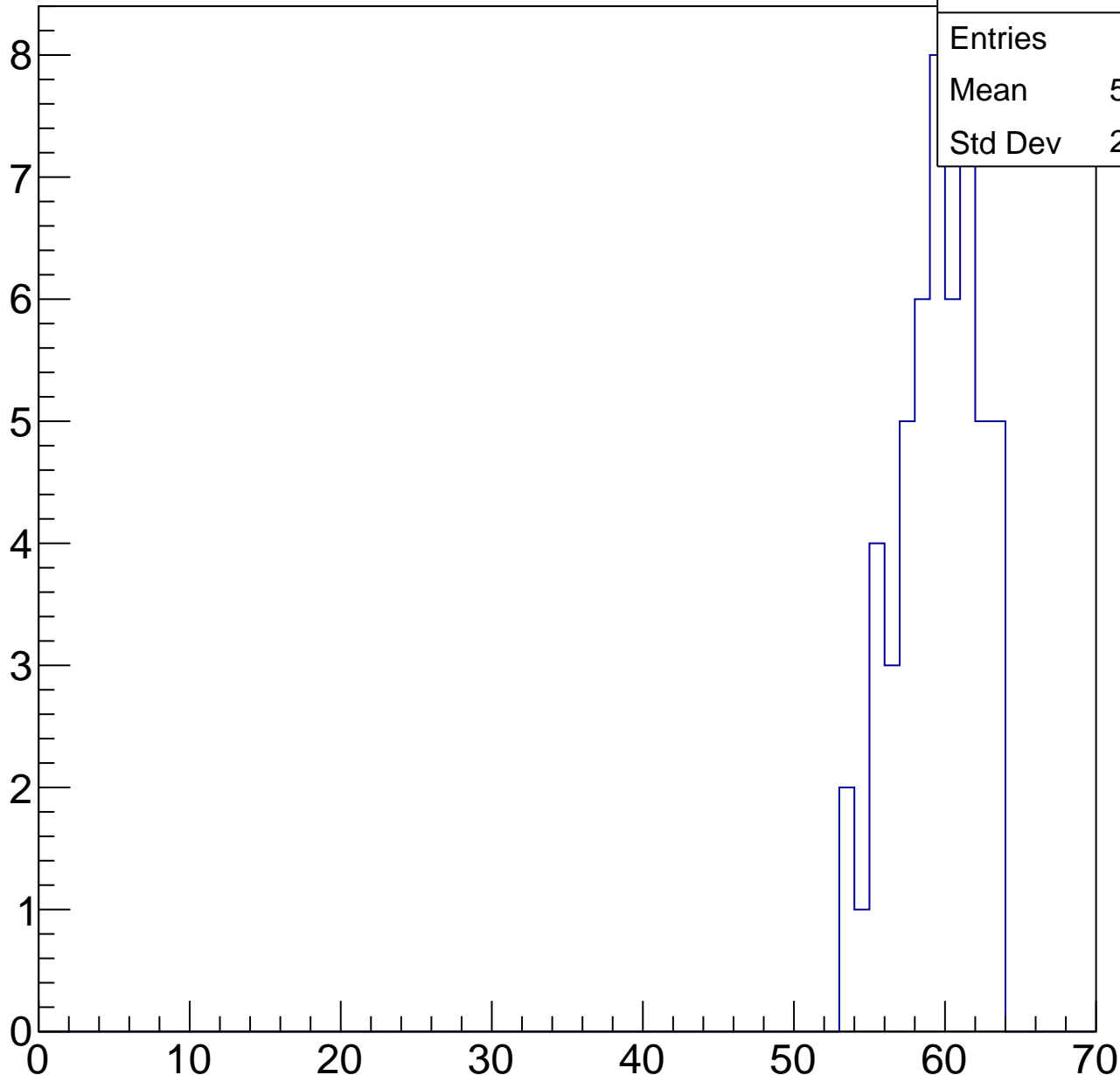
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

|         |       |
|---------|-------|
| Entries | 53    |
| Mean    | 58.98 |
| Std Dev | 2.667 |

ampl

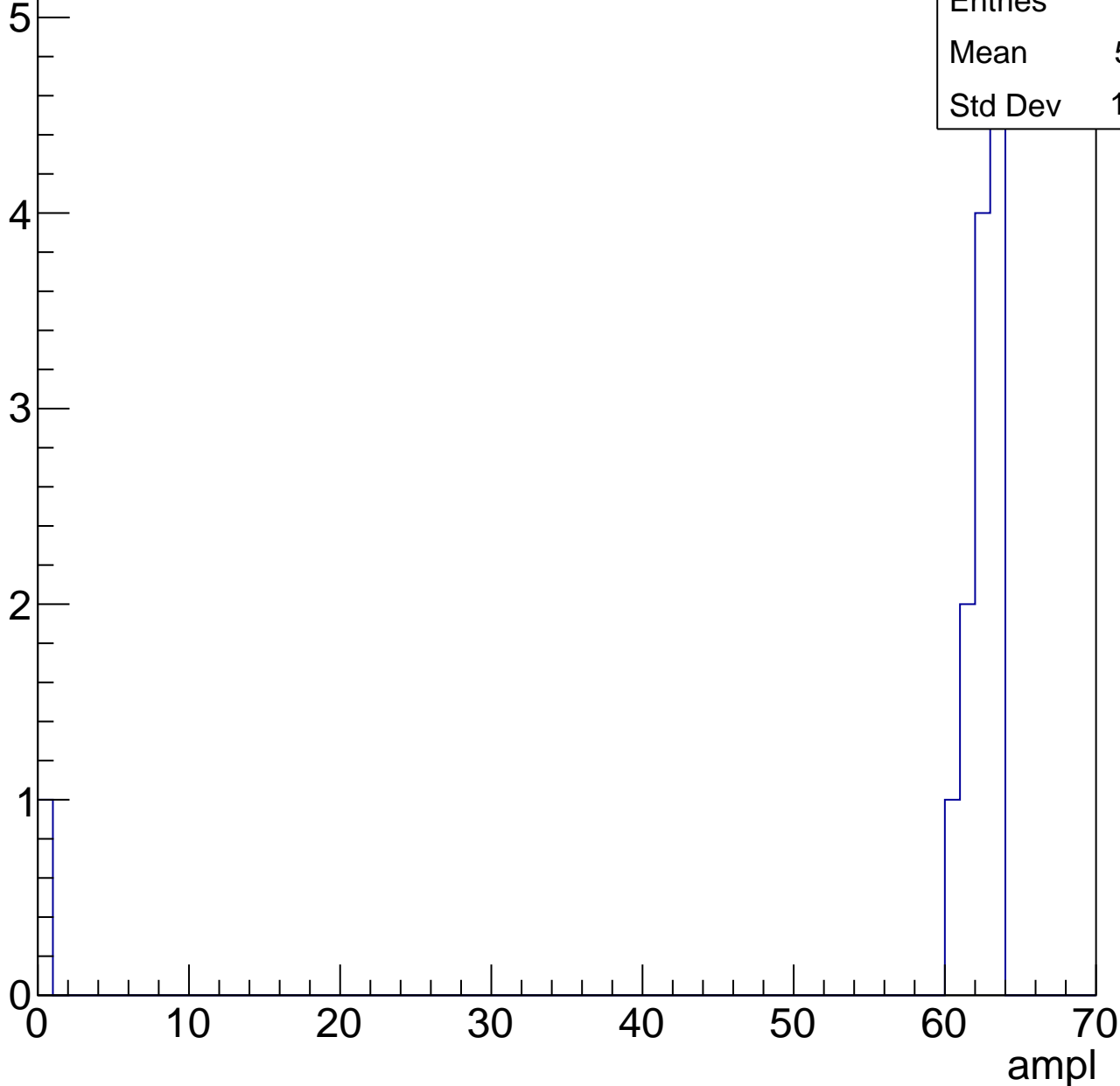


# B1L103S, U4-ch26, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 13    |
| Mean    | 57.31 |
| Std Dev | 16.57 |





# B1L103S, U4-ch26, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

|         |    |
|---------|----|
| Entries | 19 |
| Mean    | 0  |
| Std Dev | 0  |

# B1L103S, U4-ch27, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 89    |
| Mean    | 24.94 |
| Std Dev | 12.05 |

Entry

16  
14  
12  
10  
8  
6  
4  
2  
0

0

10

20

30

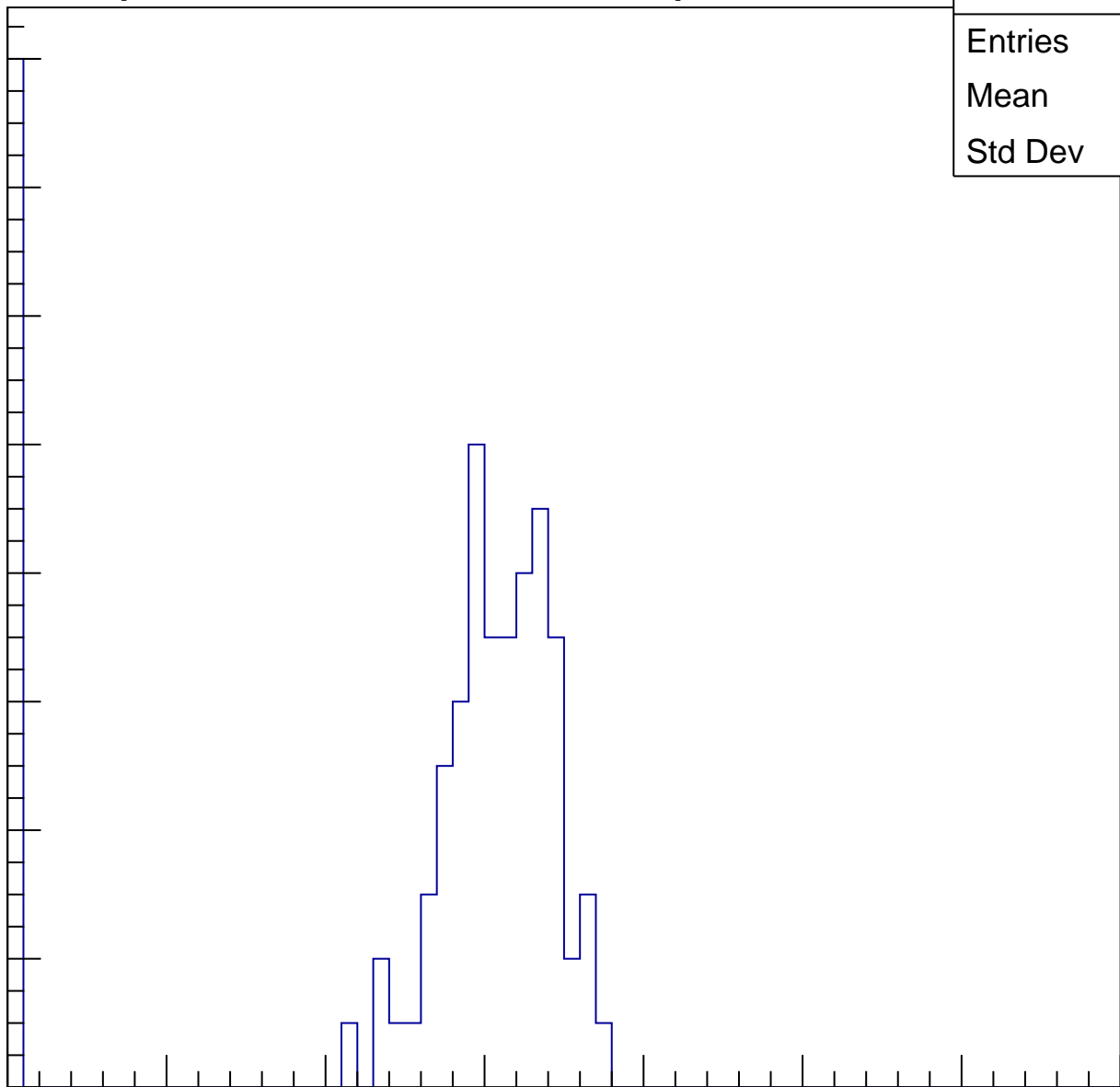
40

50

60

70

ampl

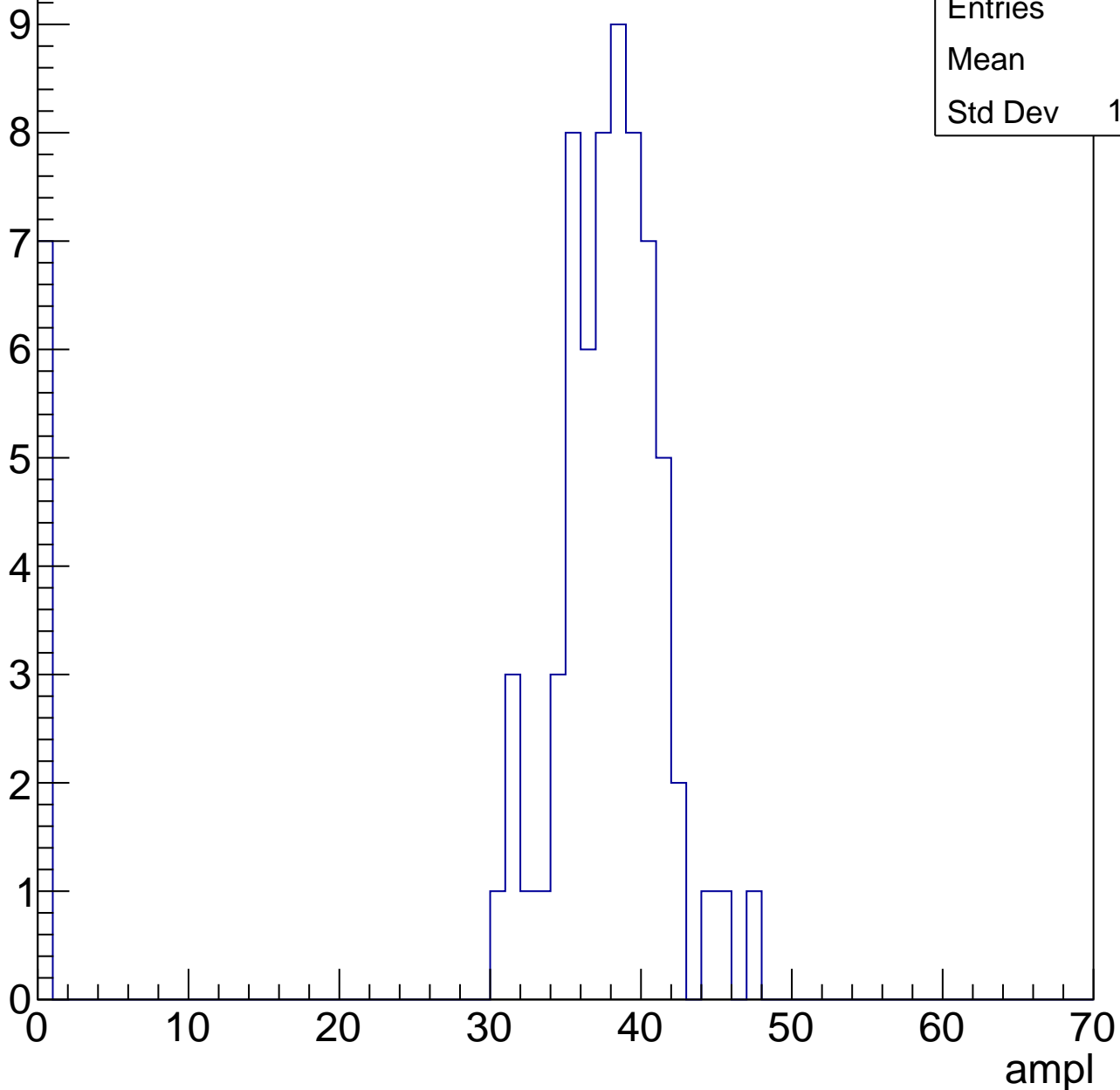


# B1L103S, U4-ch27, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 72    |
| Mean    | 33.9  |
| Std Dev | 11.55 |

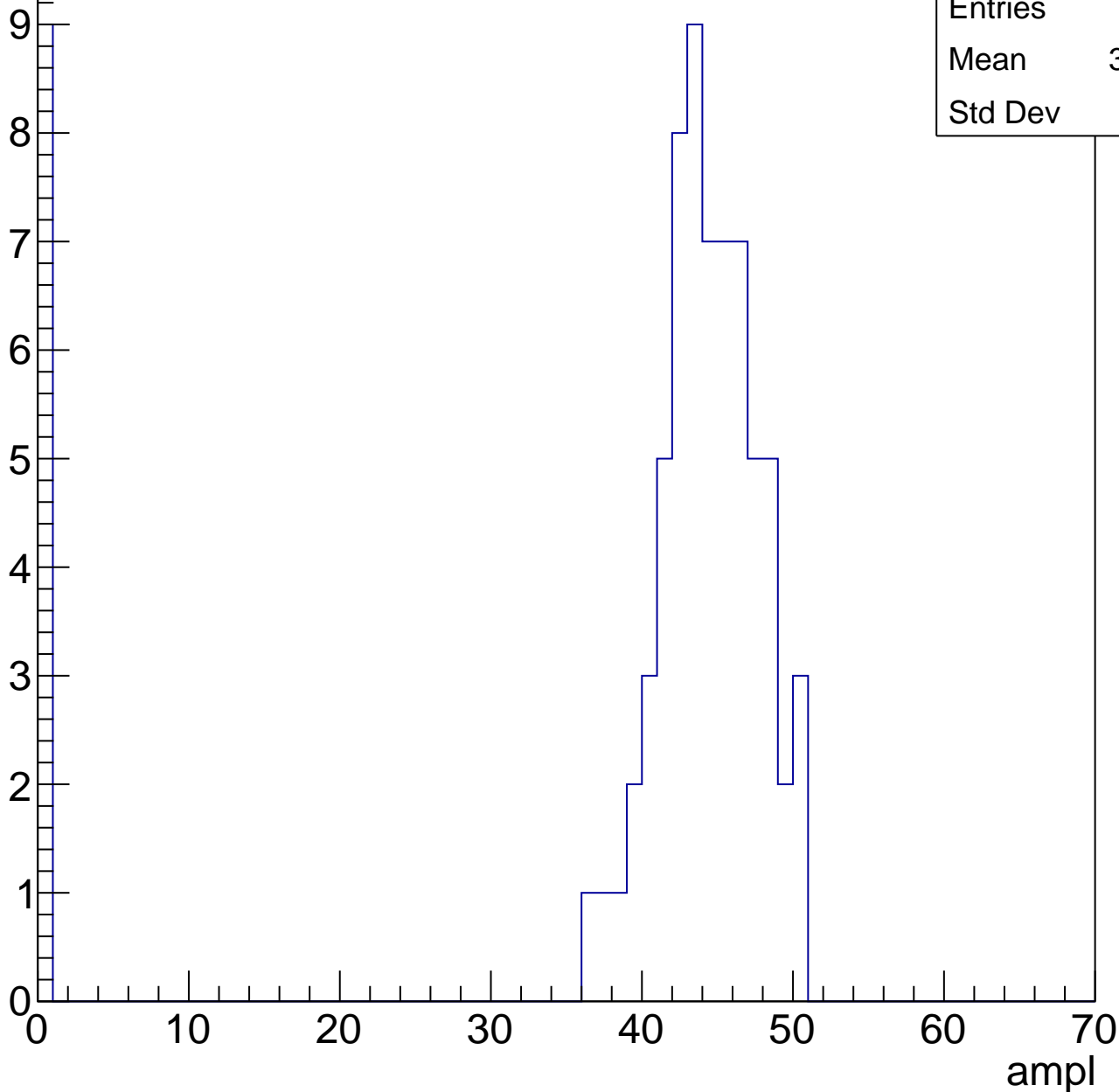


# B1L103S, U4-ch27, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 75    |
| Mean    | 38.73 |
| Std Dev | 14.6  |

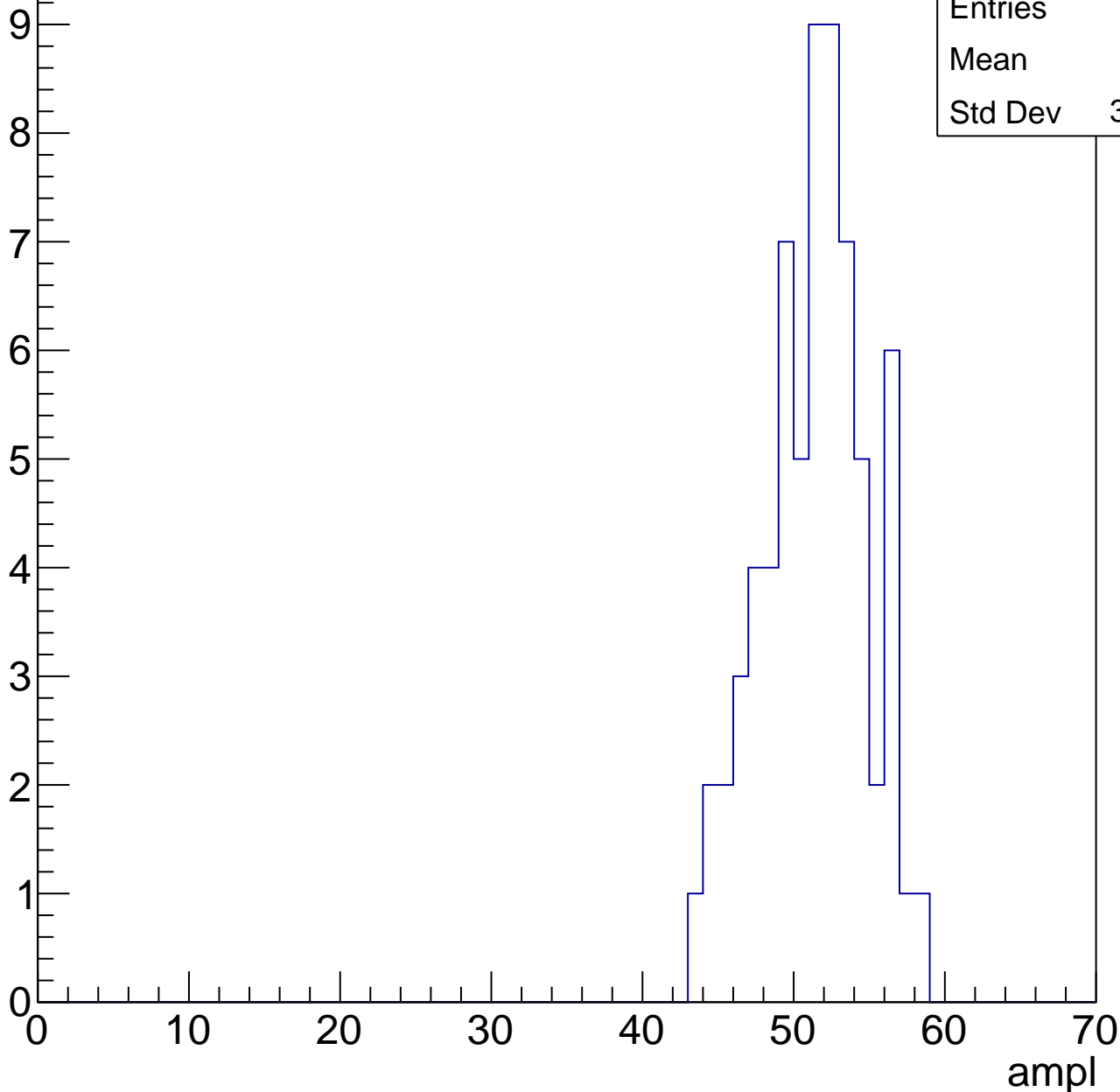


# B1L103S, U4-ch27, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 68    |
| Mean    | 50.9  |
| Std Dev | 3.409 |

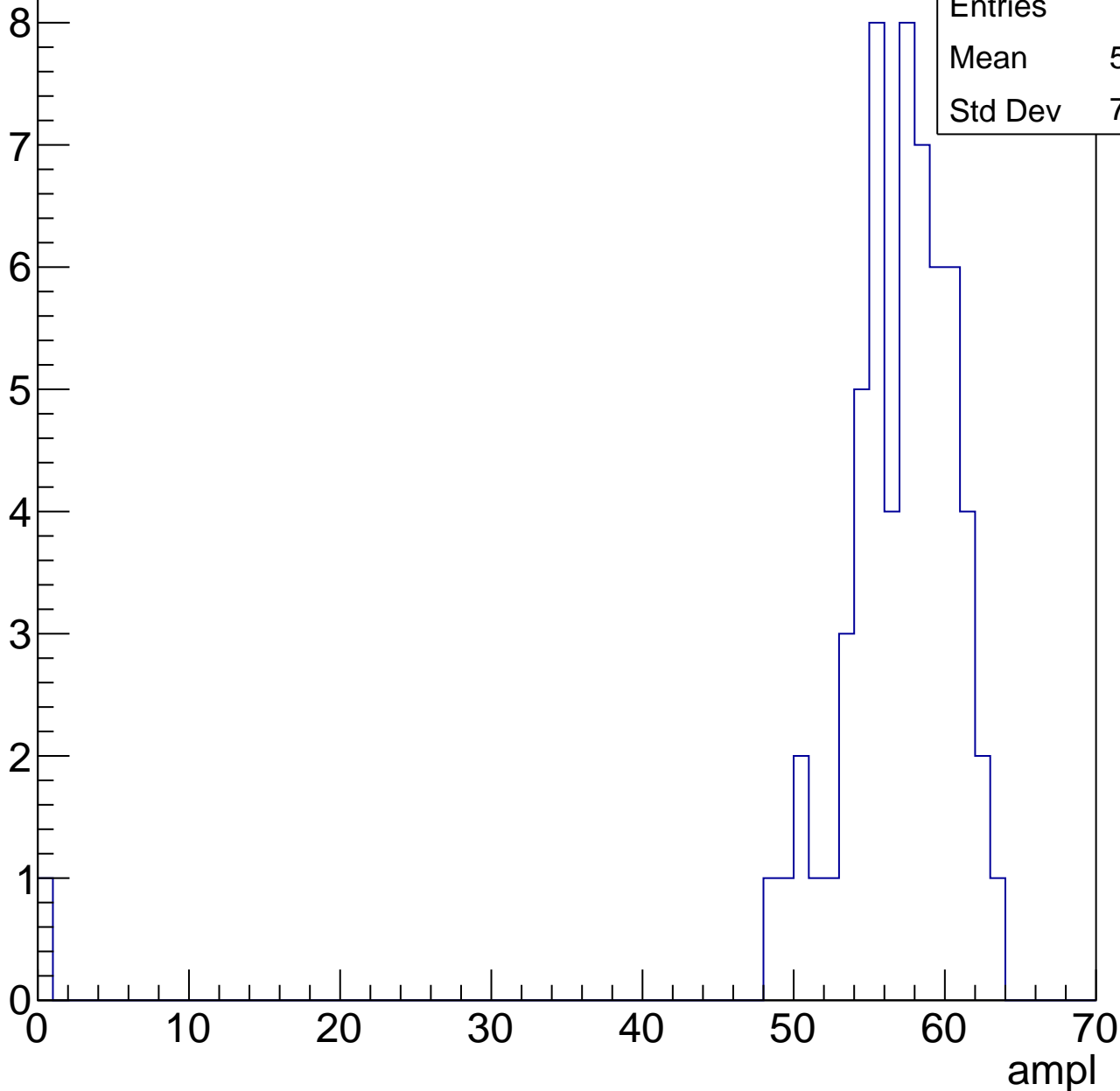


# B1L103S, U4-ch27, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 61    |
| Mean    | 55.74 |
| Std Dev | 7.913 |

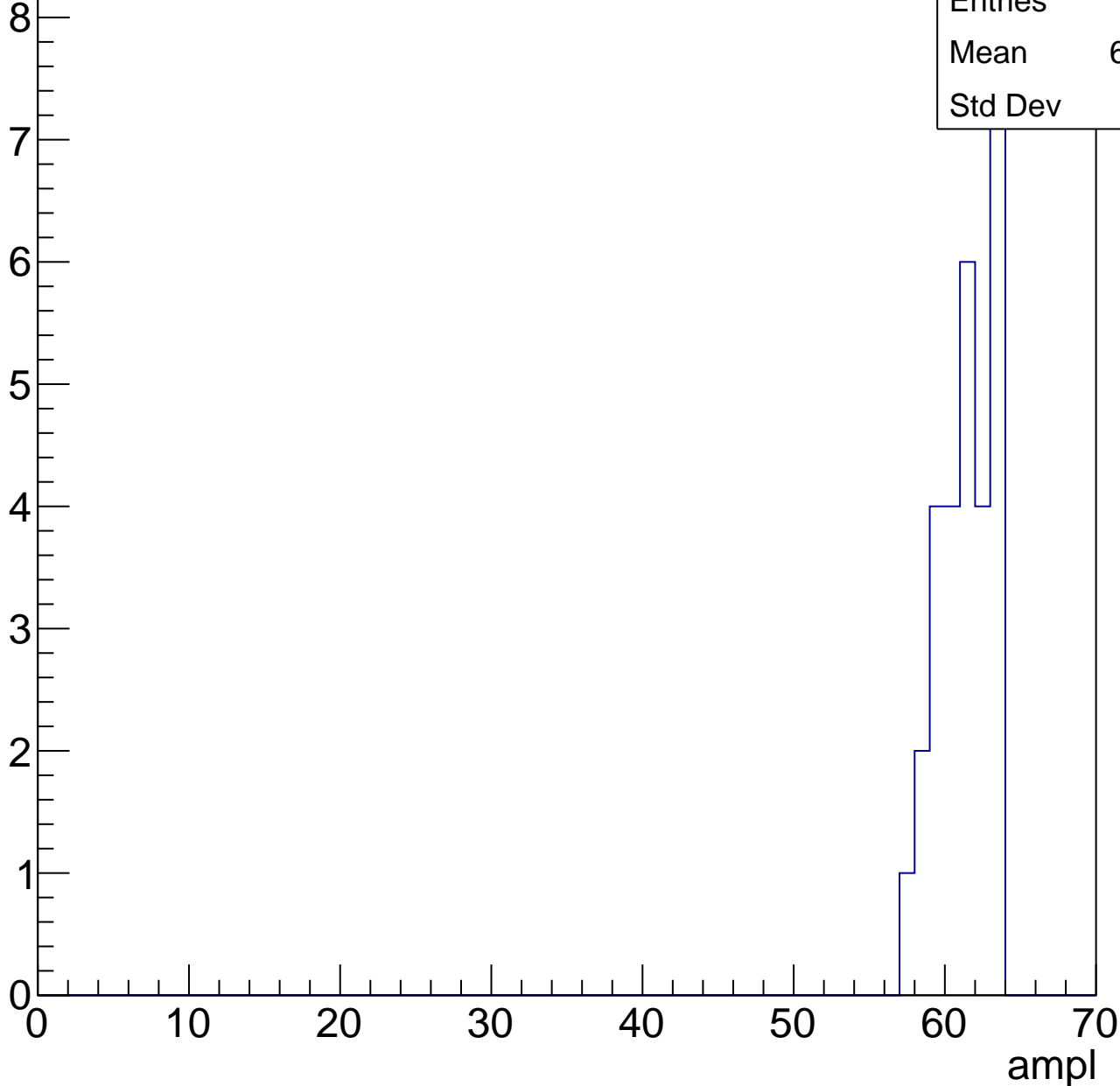


# B1L103S, U4-ch27, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

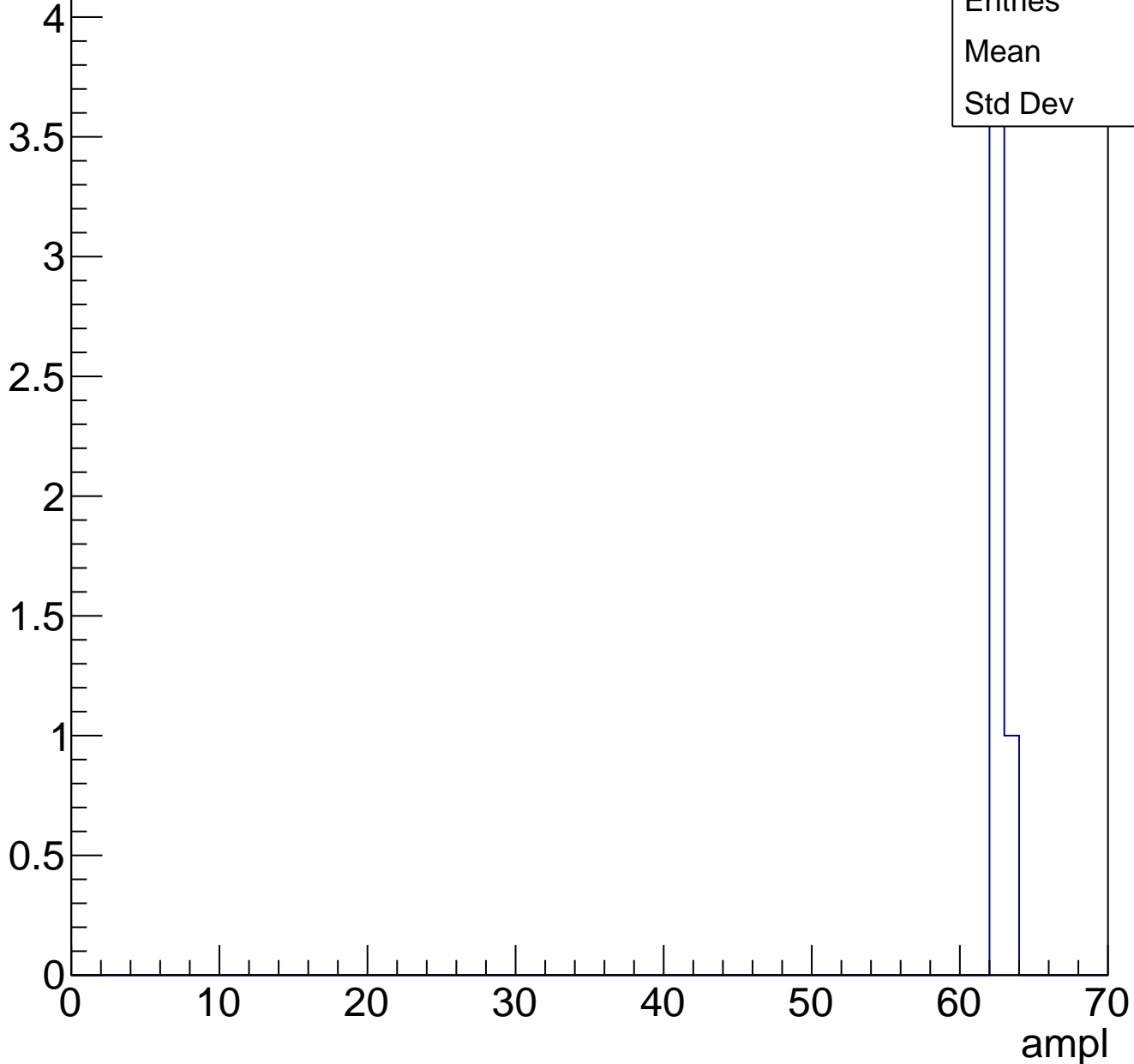
|         |       |
|---------|-------|
| Entries | 29    |
| Mean    | 60.93 |
| Std Dev | 1.76  |



# B1L103S, U4-ch27, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



|         |      |
|---------|------|
| Entries | 5    |
| Mean    | 62.2 |
| Std Dev | 0.4  |



# B1L103S, U4-ch27, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



|         |    |
|---------|----|
| Entries | 18 |
| Mean    | 0  |
| Std Dev | 0  |

# B1L103S, U4-ch28, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

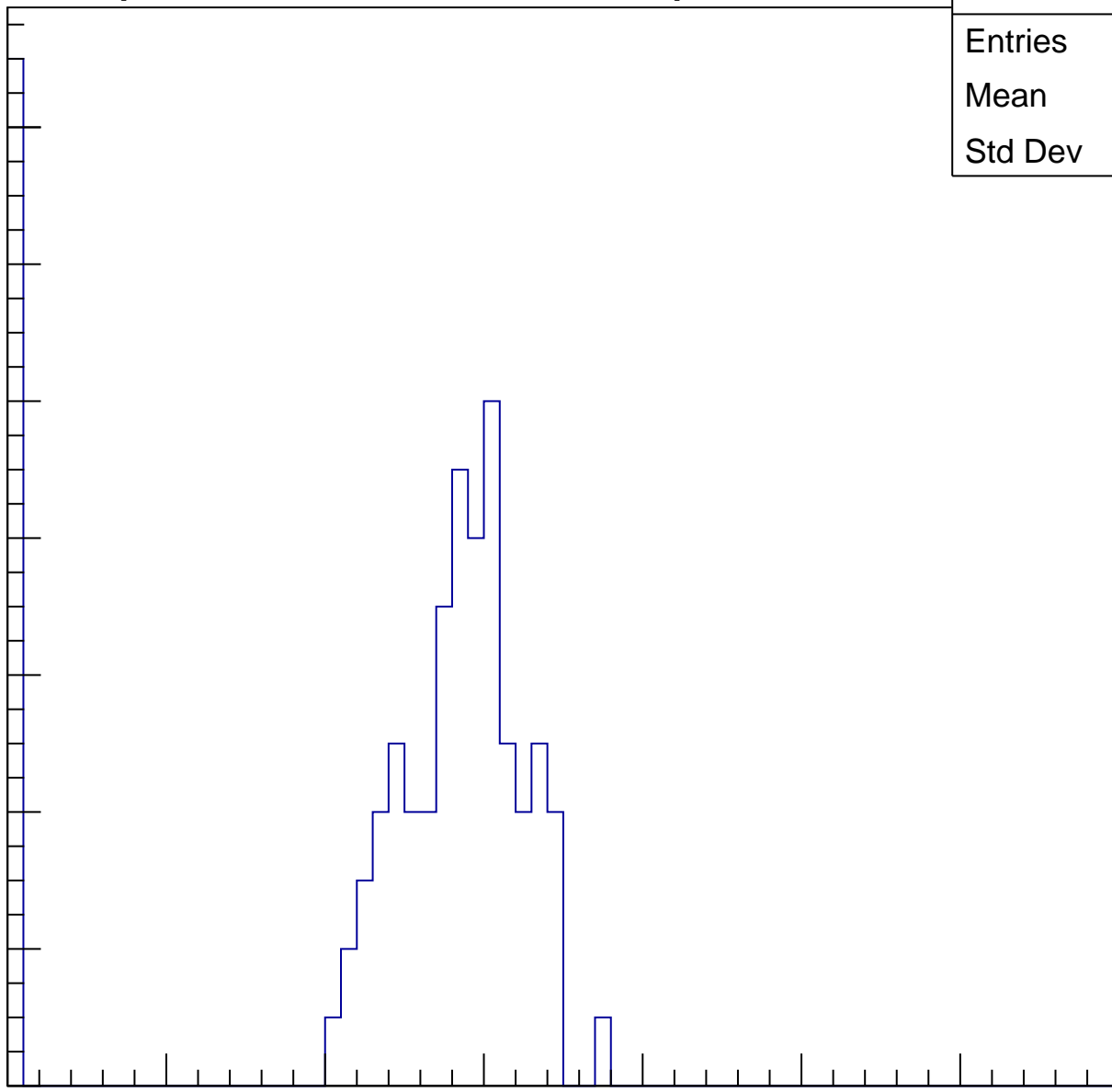
|         |       |
|---------|-------|
| Entries | 91    |
| Mean    | 23.49 |
| Std Dev | 10.96 |

Entry

14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

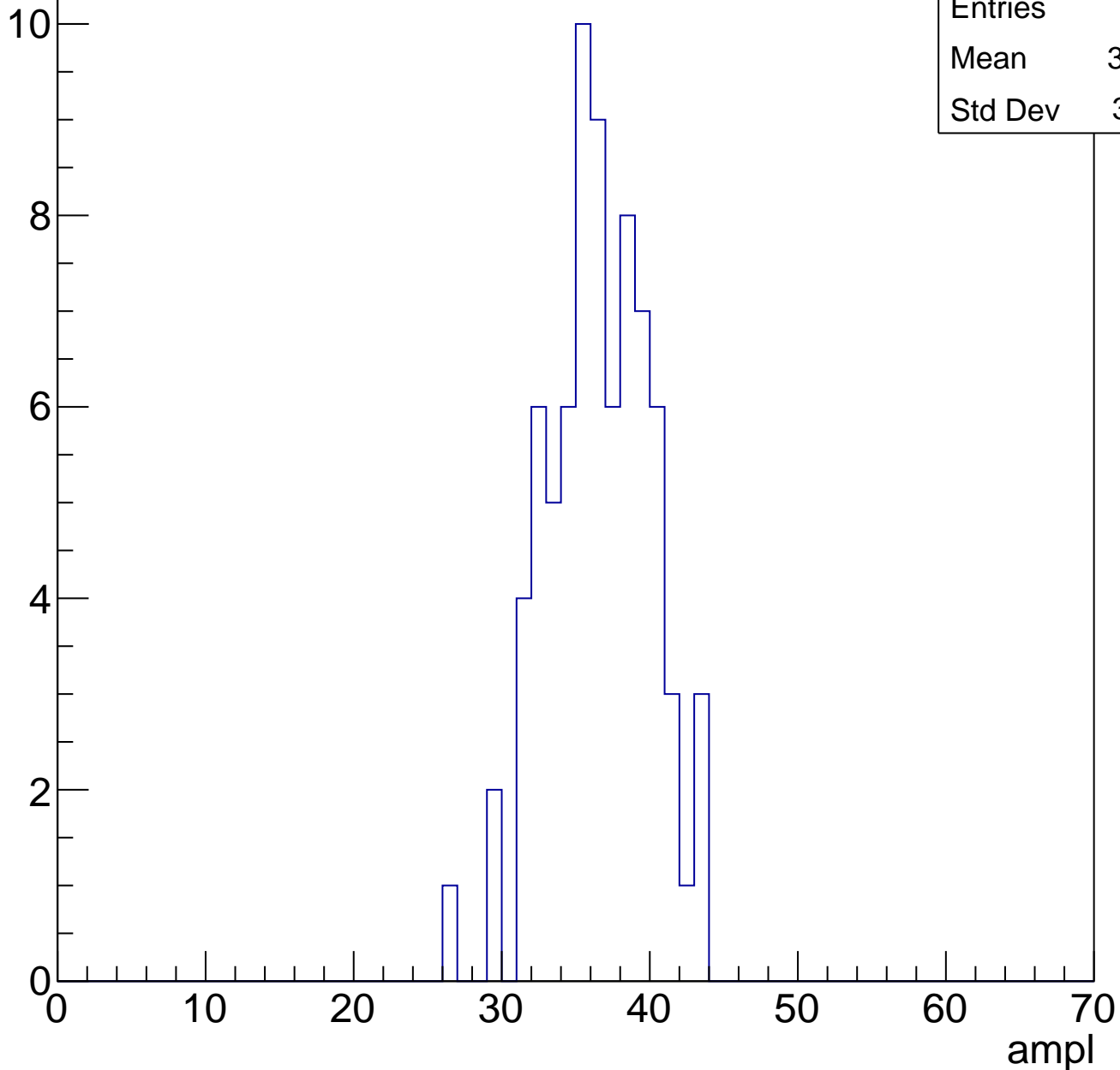


# B1L103S, U4-ch28, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 77    |
| Mean    | 36.05 |
| Std Dev | 3.471 |

Entry

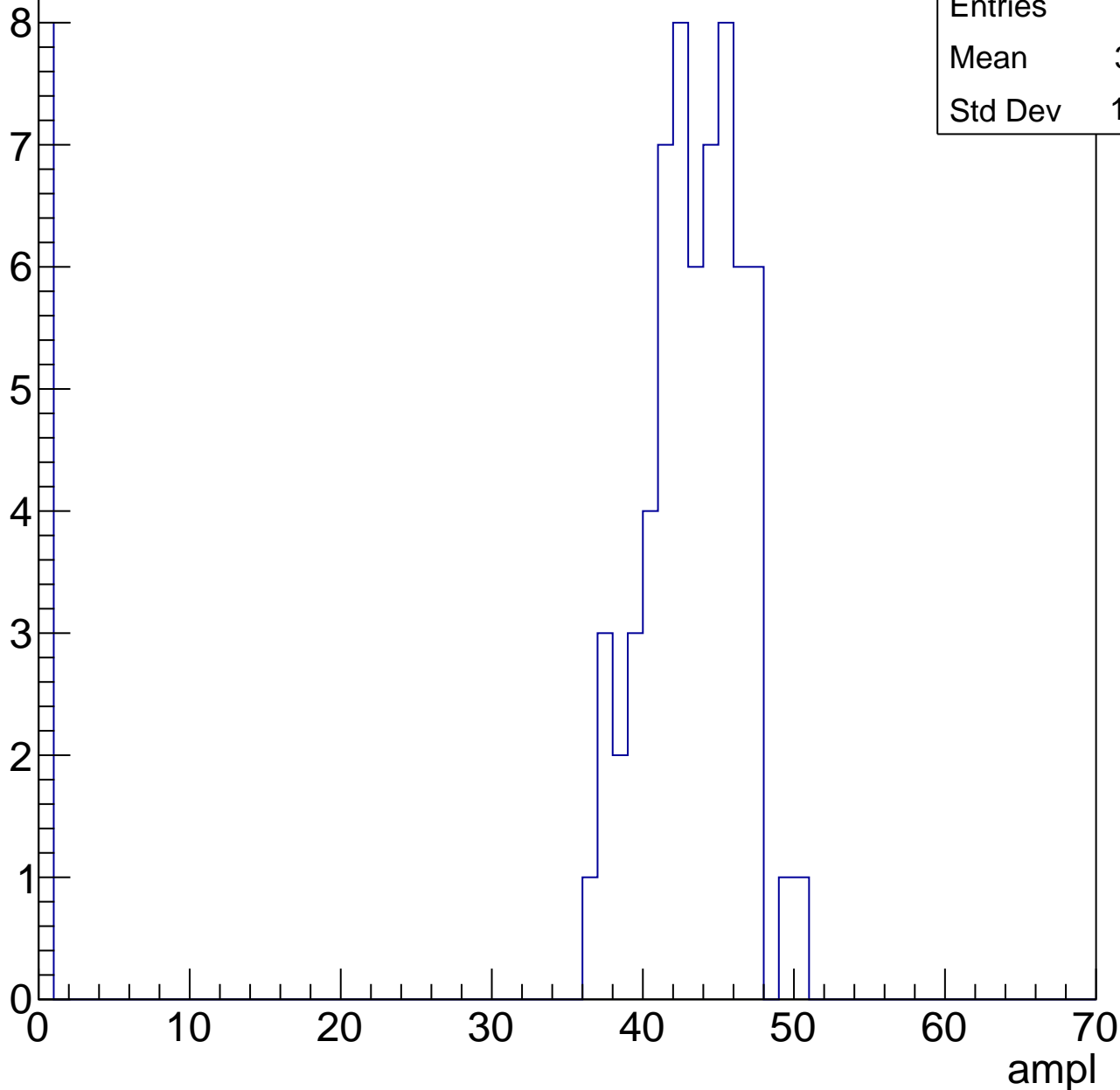


# B1L103S, U4-ch28, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 71    |
| Mean    | 38.11 |
| Std Dev | 13.89 |

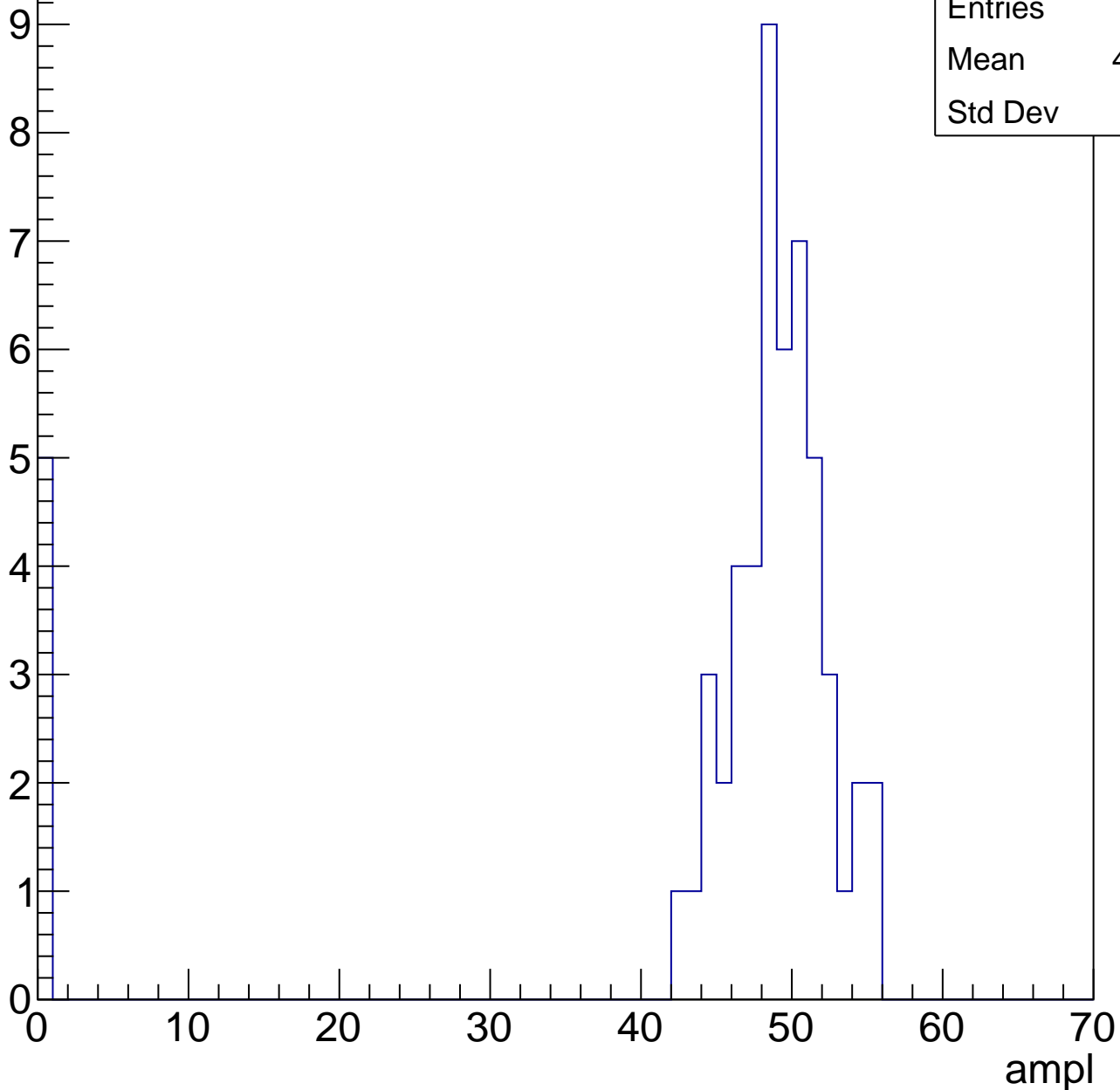


# B1L103S, U4-ch28, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 55    |
| Mean    | 44.31 |
| Std Dev | 14.3  |

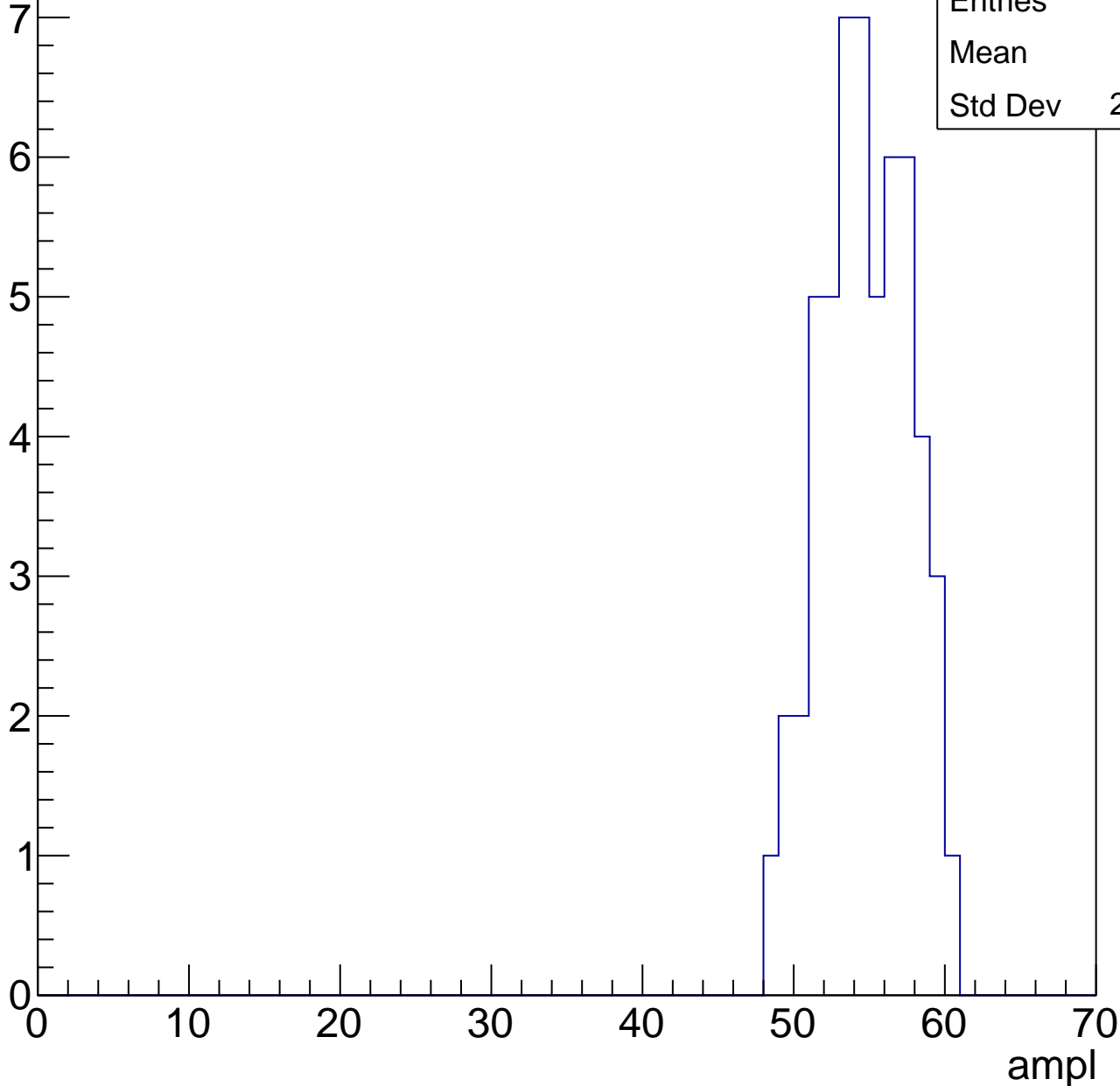


# B1L103S, U4-ch28, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

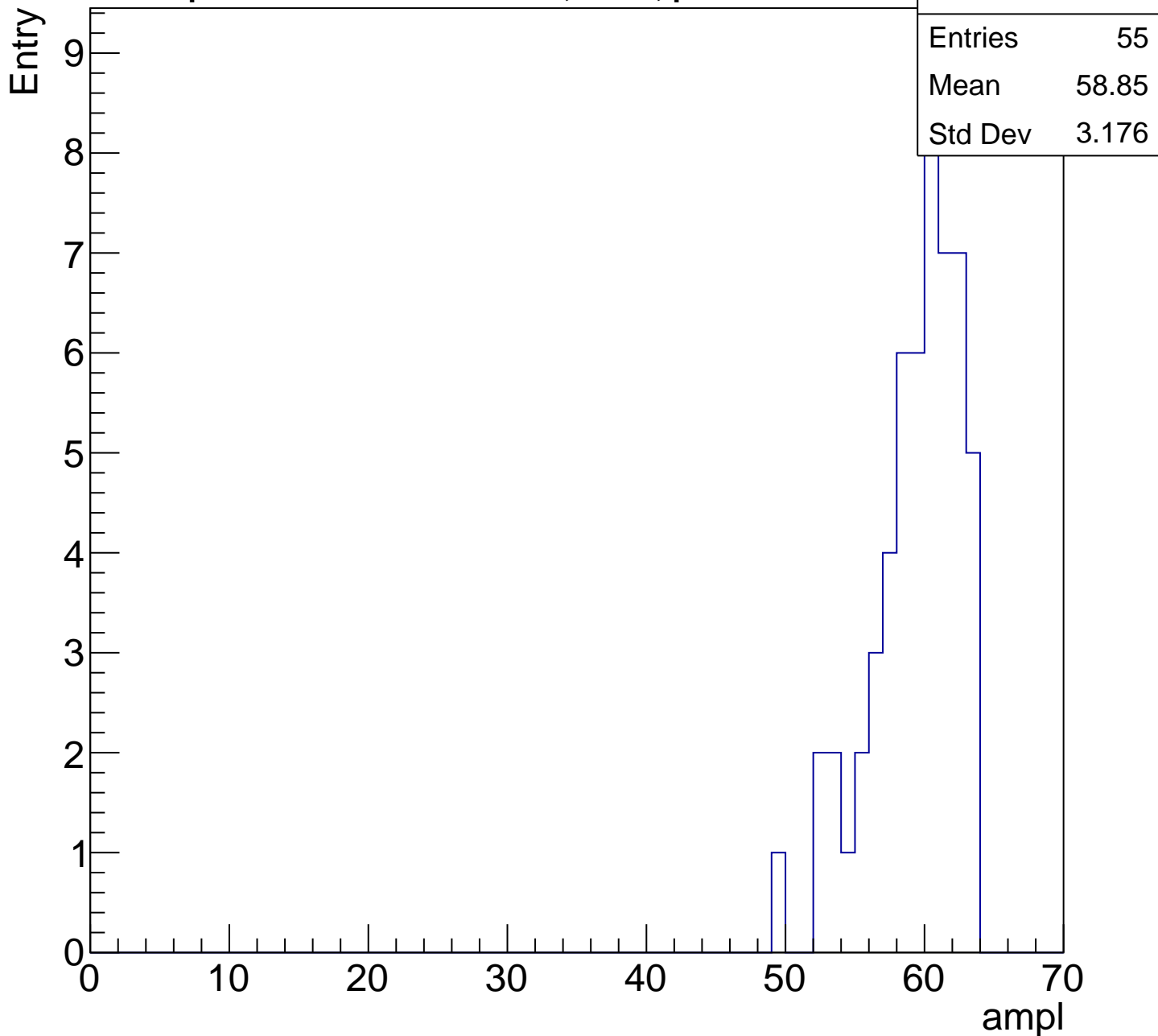
Entry

|         |       |
|---------|-------|
| Entries | 54    |
| Mean    | 54.3  |
| Std Dev | 2.865 |



# B1L103S, U4-ch28, adc5

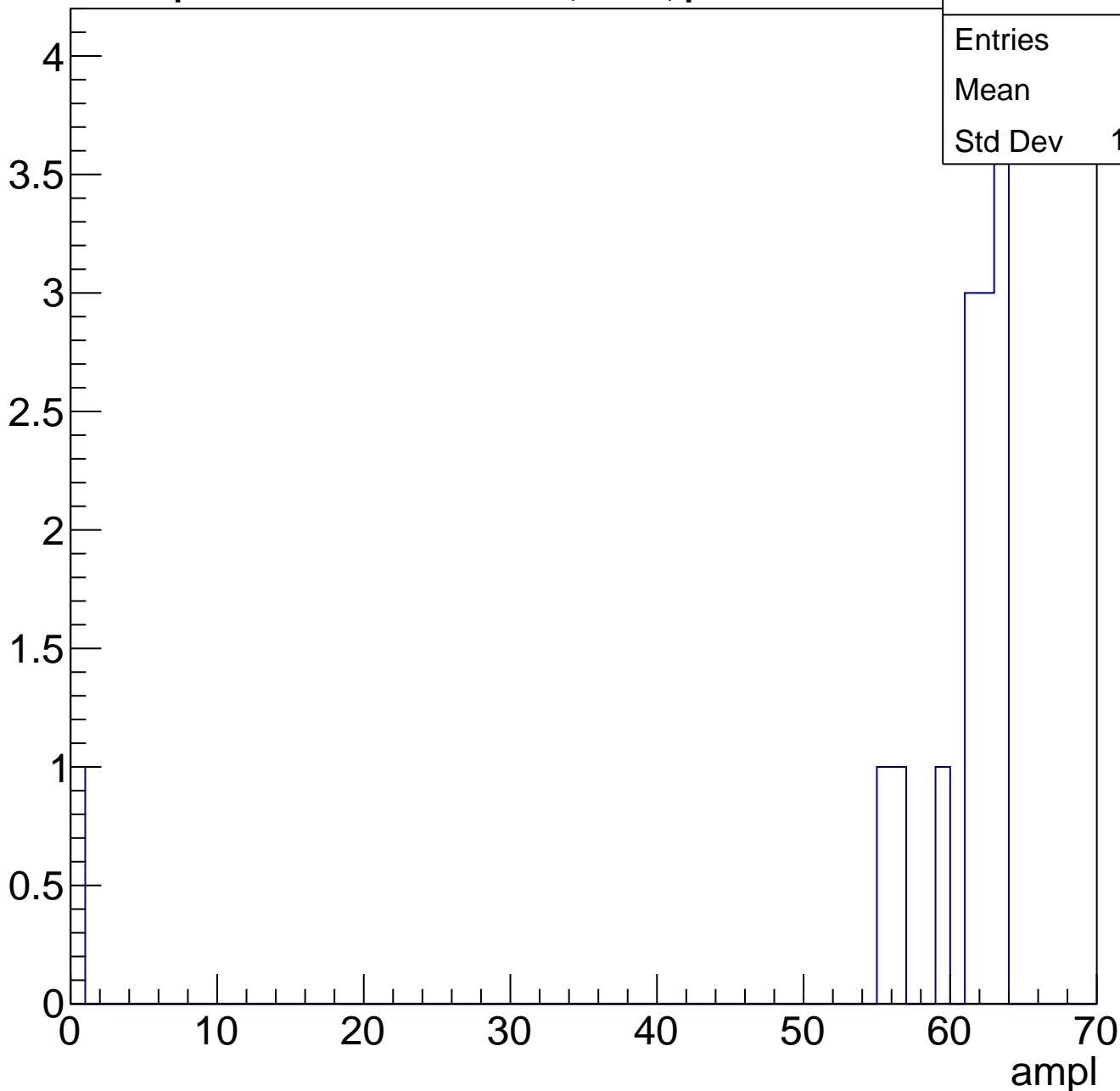
calib\_packv5\_041523\_1651.root, FC#0, port C2



# B1L103S, U4-ch28, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

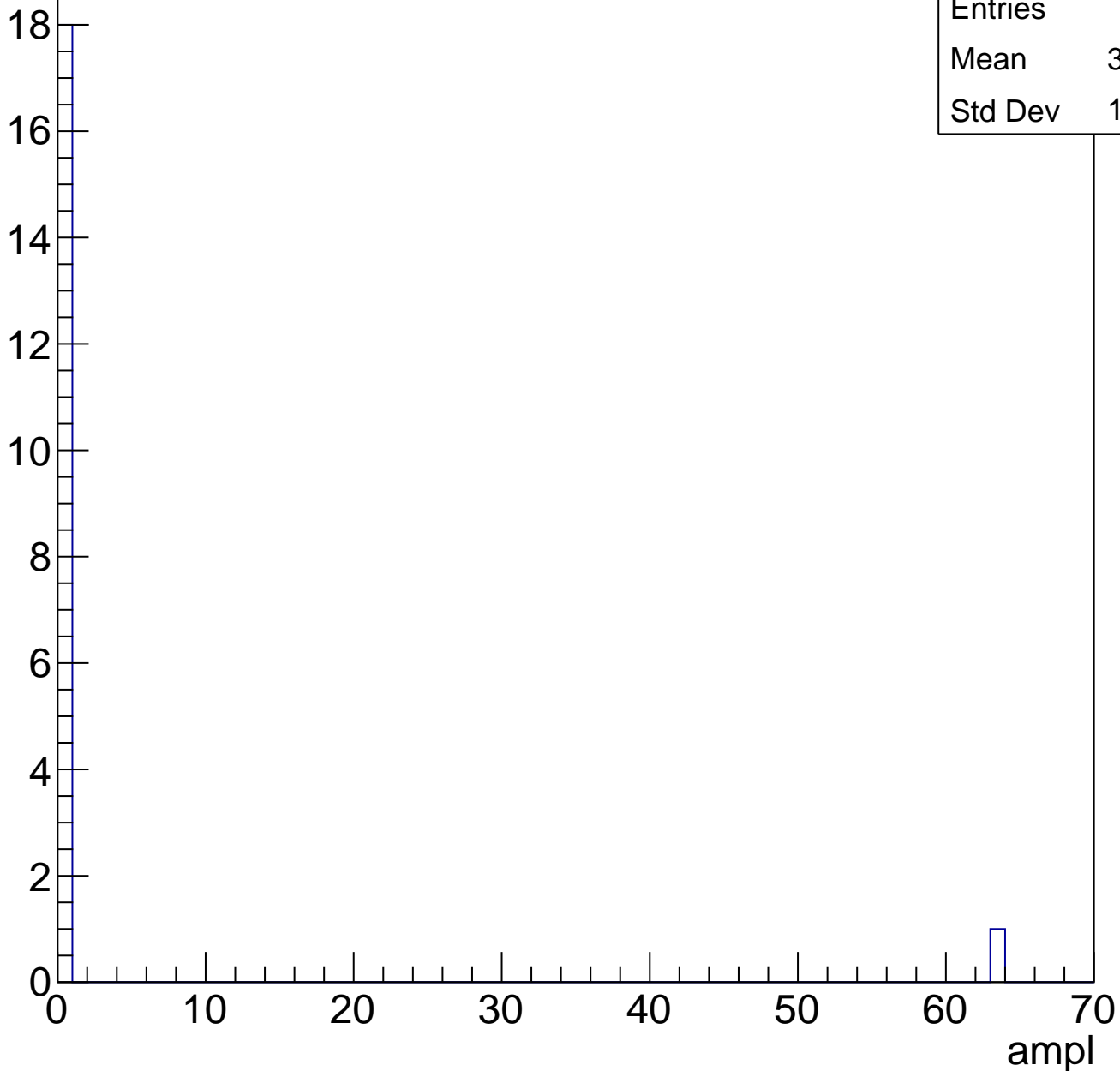




# B1L103S, U4-ch28, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U4-ch29, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

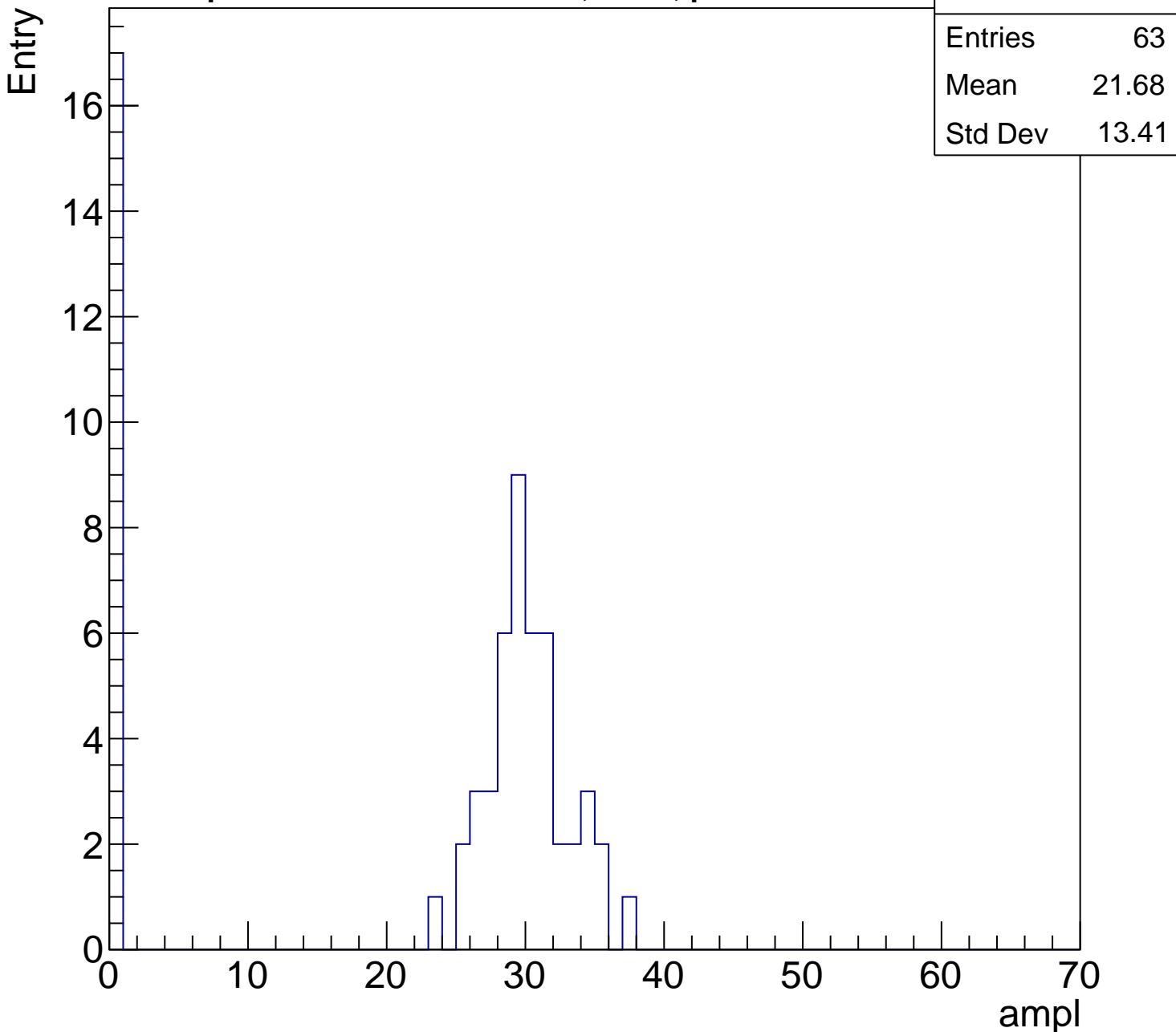
|         |       |
|---------|-------|
| Entries | 63    |
| Mean    | 21.68 |
| Std Dev | 13.41 |

Entry

16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

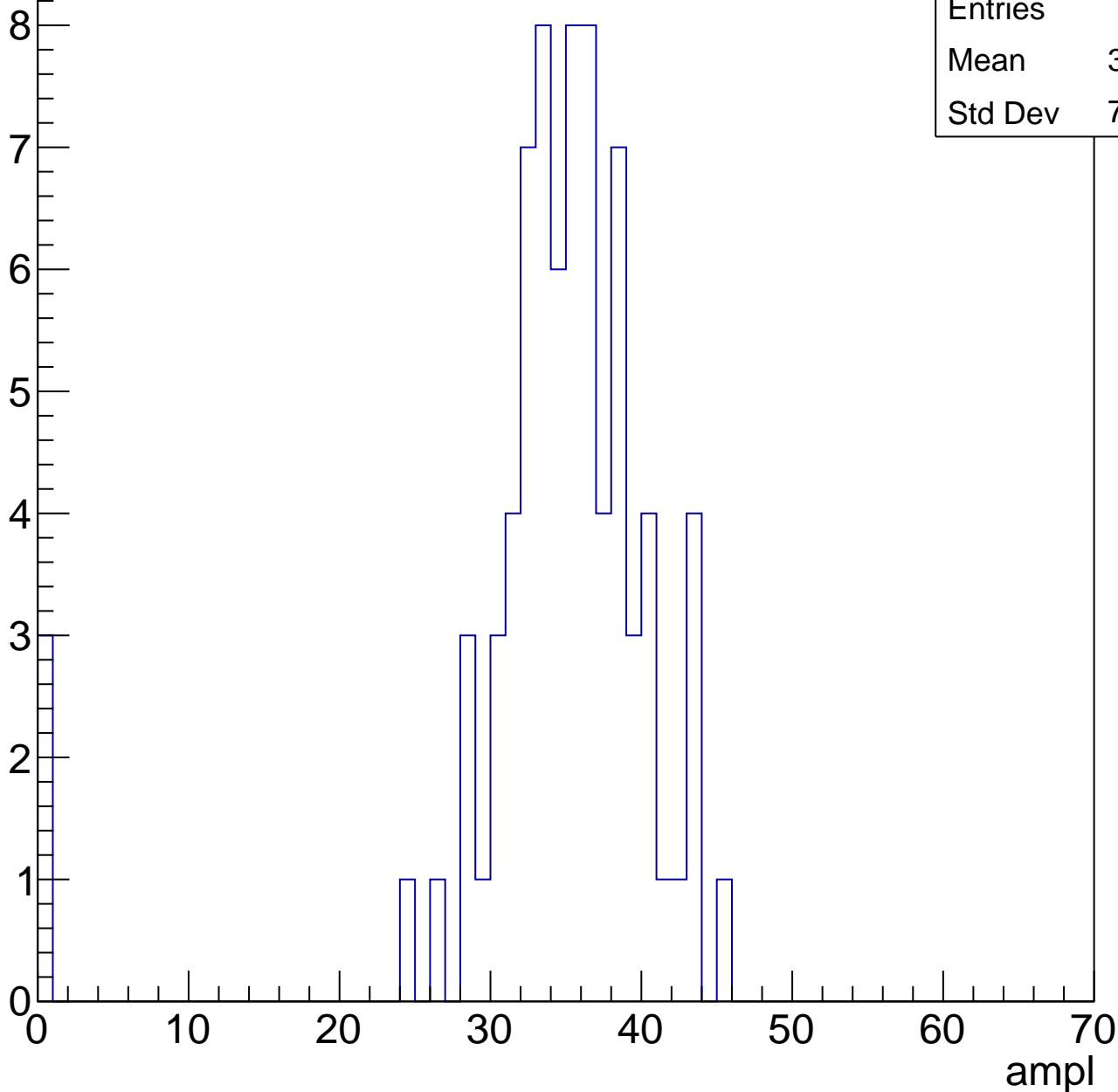


# B1L103S, U4-ch29, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 78    |
| Mean    | 33.69 |
| Std Dev | 7.879 |

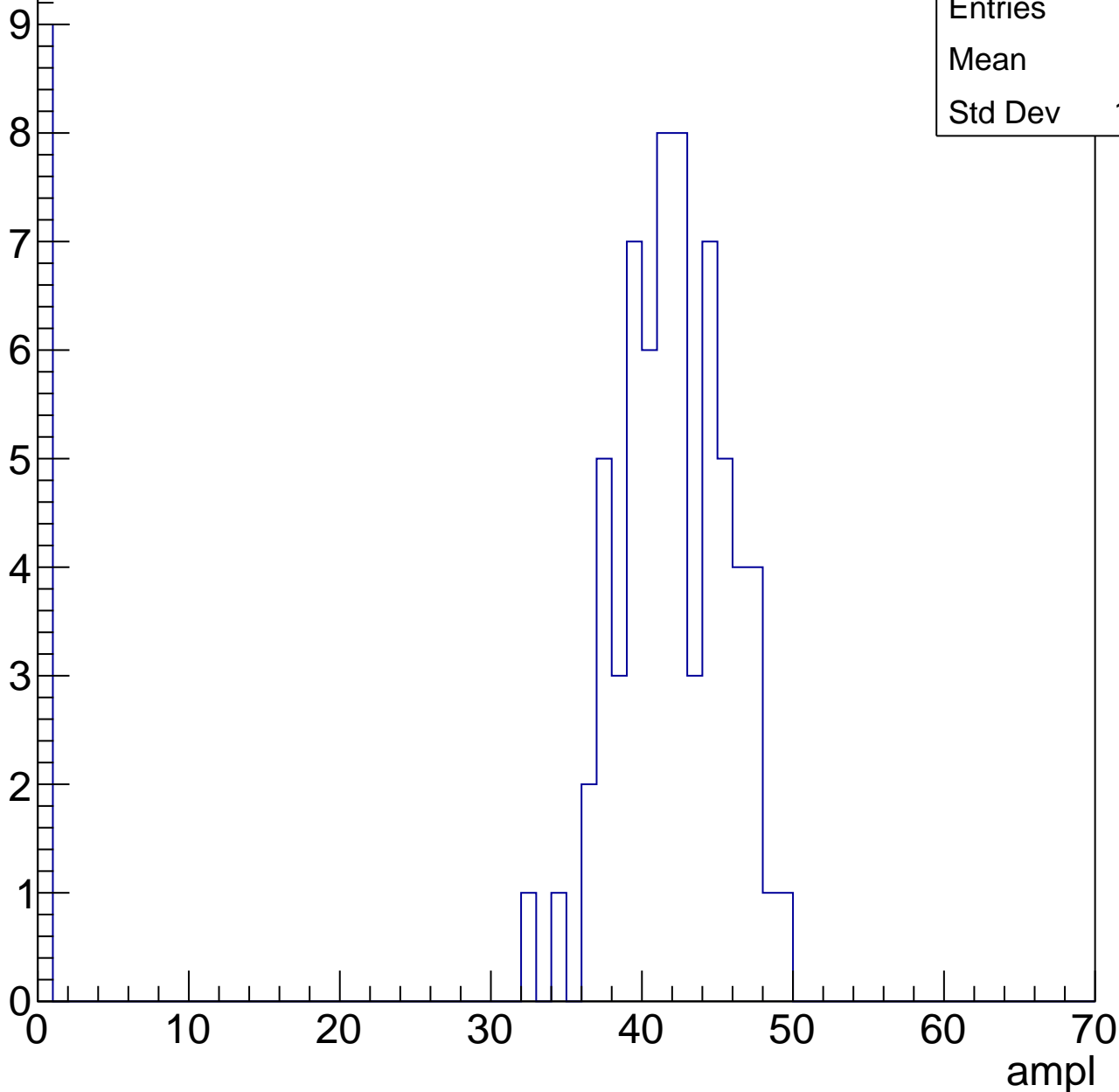


# B1L103S, U4-ch29, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 75    |
| Mean    | 36.6  |
| Std Dev | 13.91 |

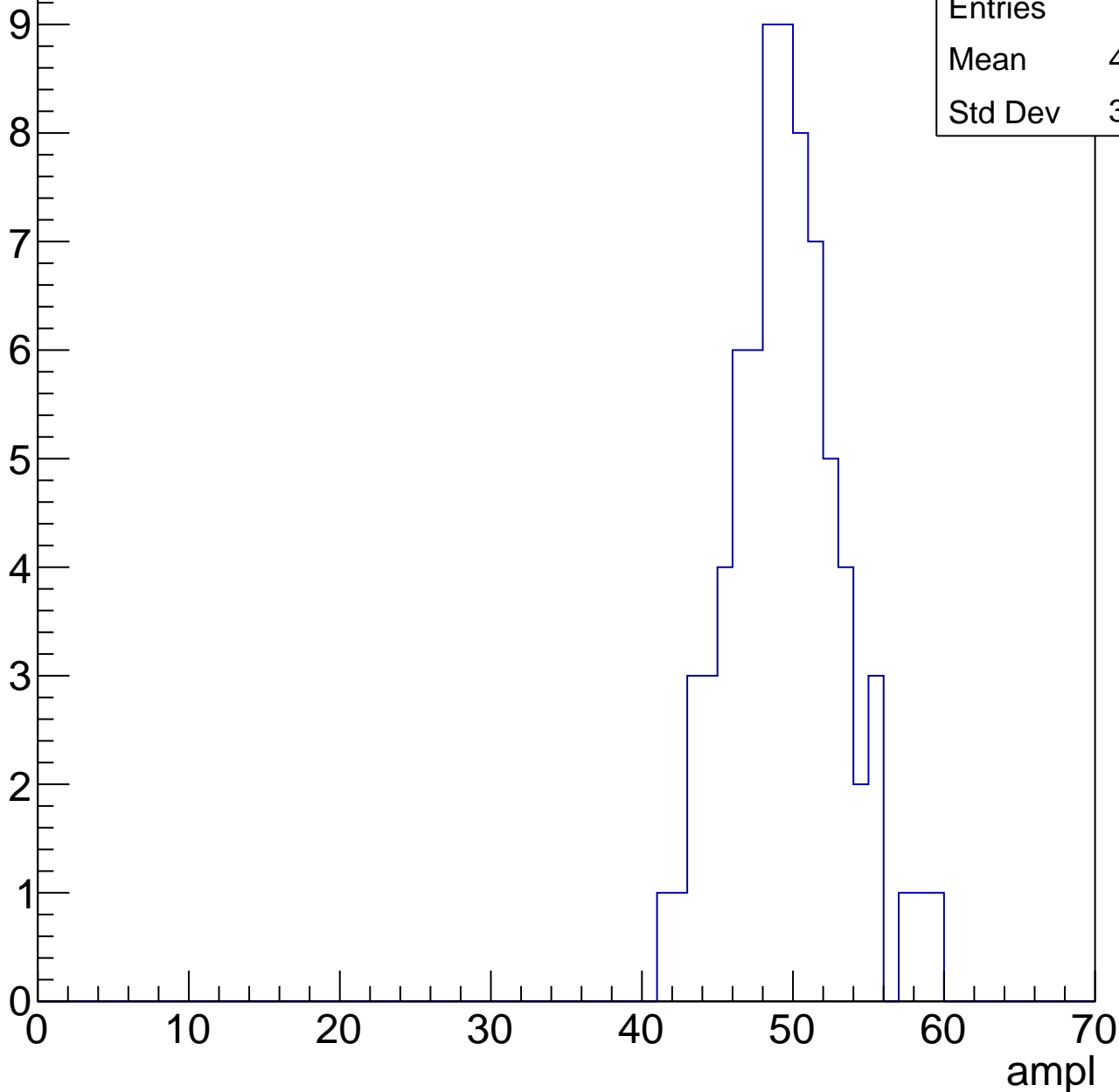


# B1L103S, U4-ch29, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

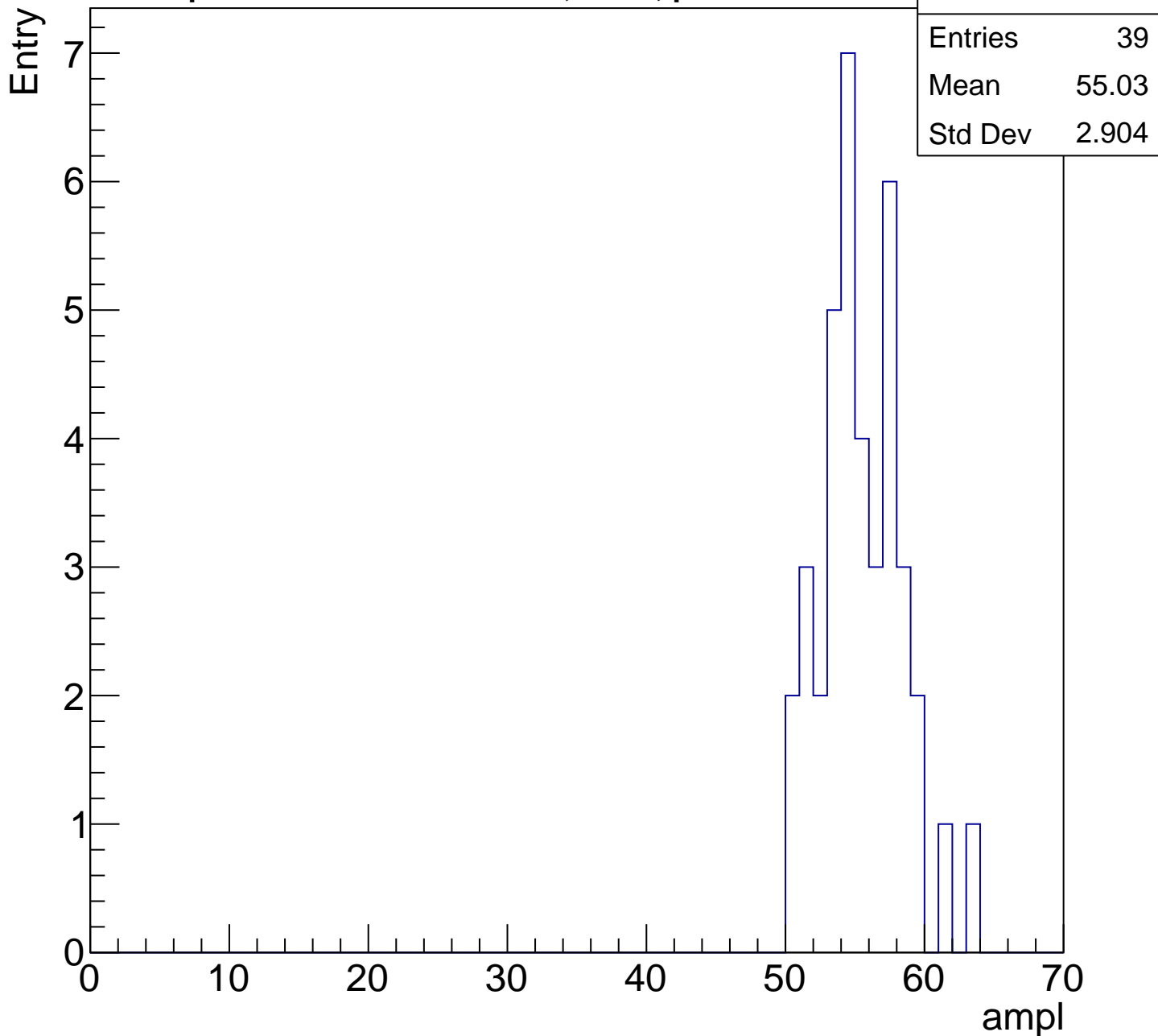
Entry

|         |       |
|---------|-------|
| Entries | 74    |
| Mean    | 49.07 |
| Std Dev | 3.666 |



# B1L103S, U4-ch29, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2



# B1L103S, U4-ch29, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

7

6

5

4

3

2

1

0

Entries 48

Mean 58.44

Std Dev 3.027

0

10

20

30

40

50

60

ampl

0

10

20

30

40

50

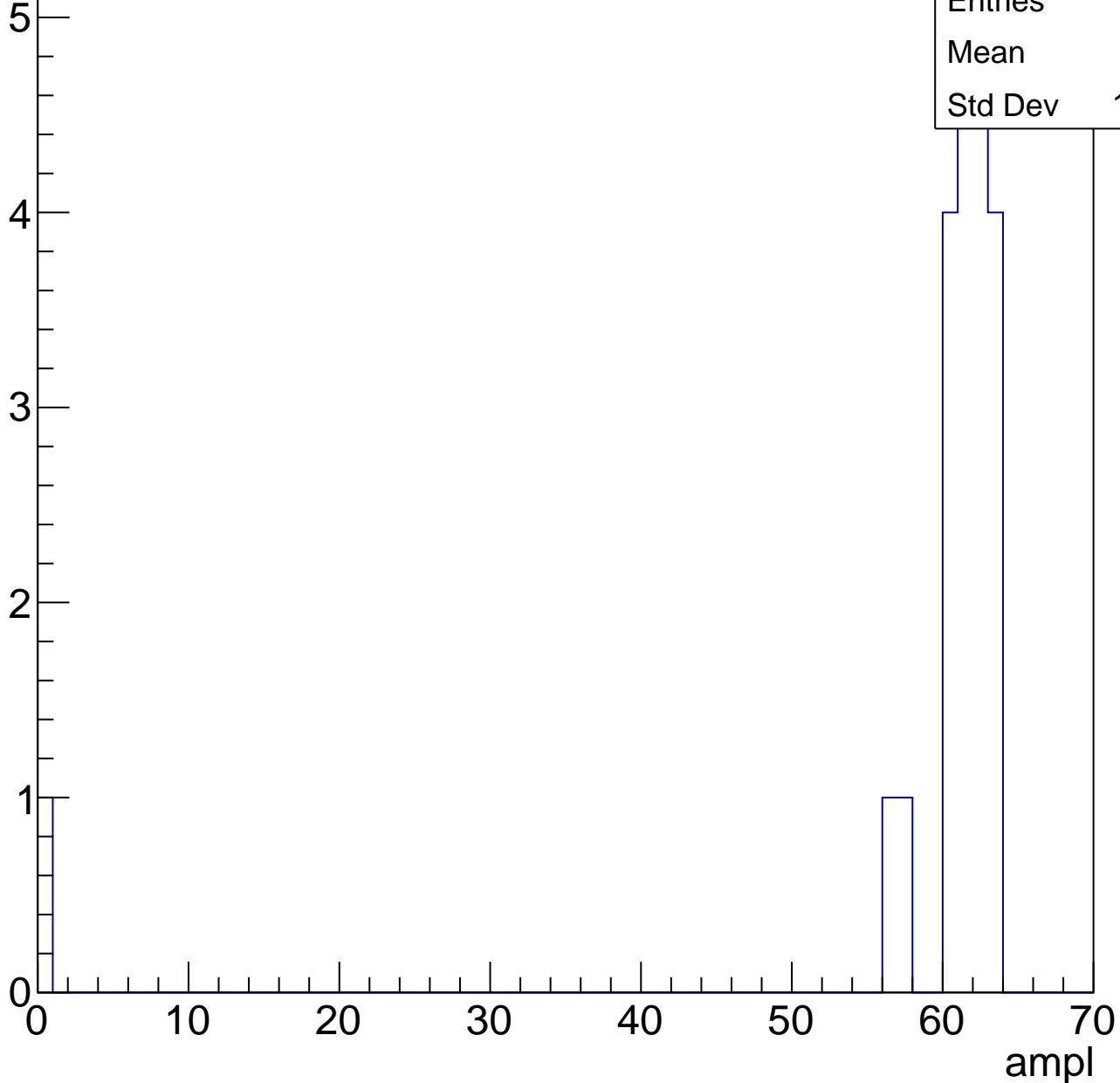
ampl

# B1L103S, U4-ch29, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 21    |
| Mean    | 58.1  |
| Std Dev | 13.11 |





# B1L103S, U4-ch29, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

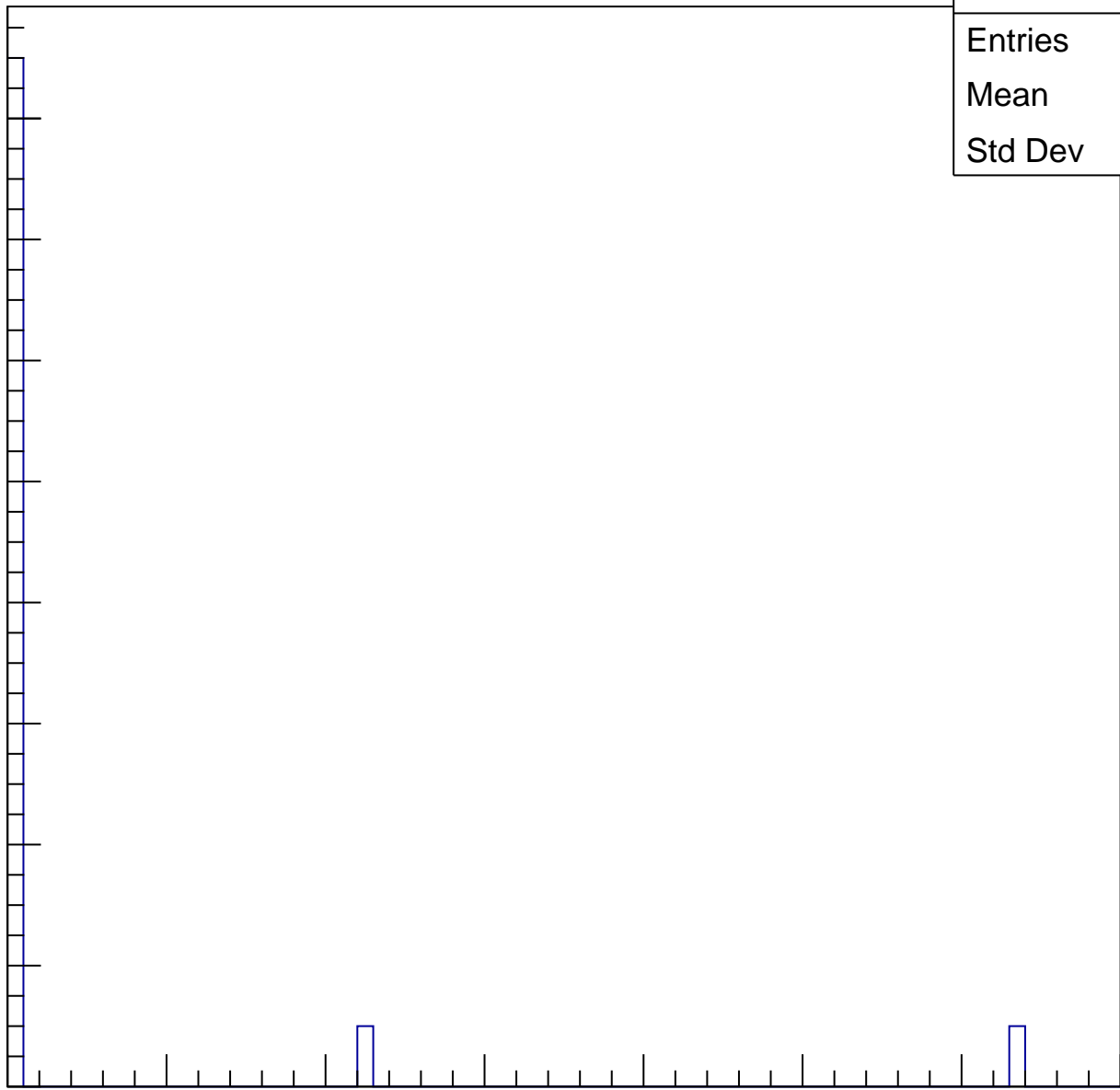
|         |       |
|---------|-------|
| Entries | 19    |
| Mean    | 4.474 |
| Std Dev | 14.64 |

Entry

16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

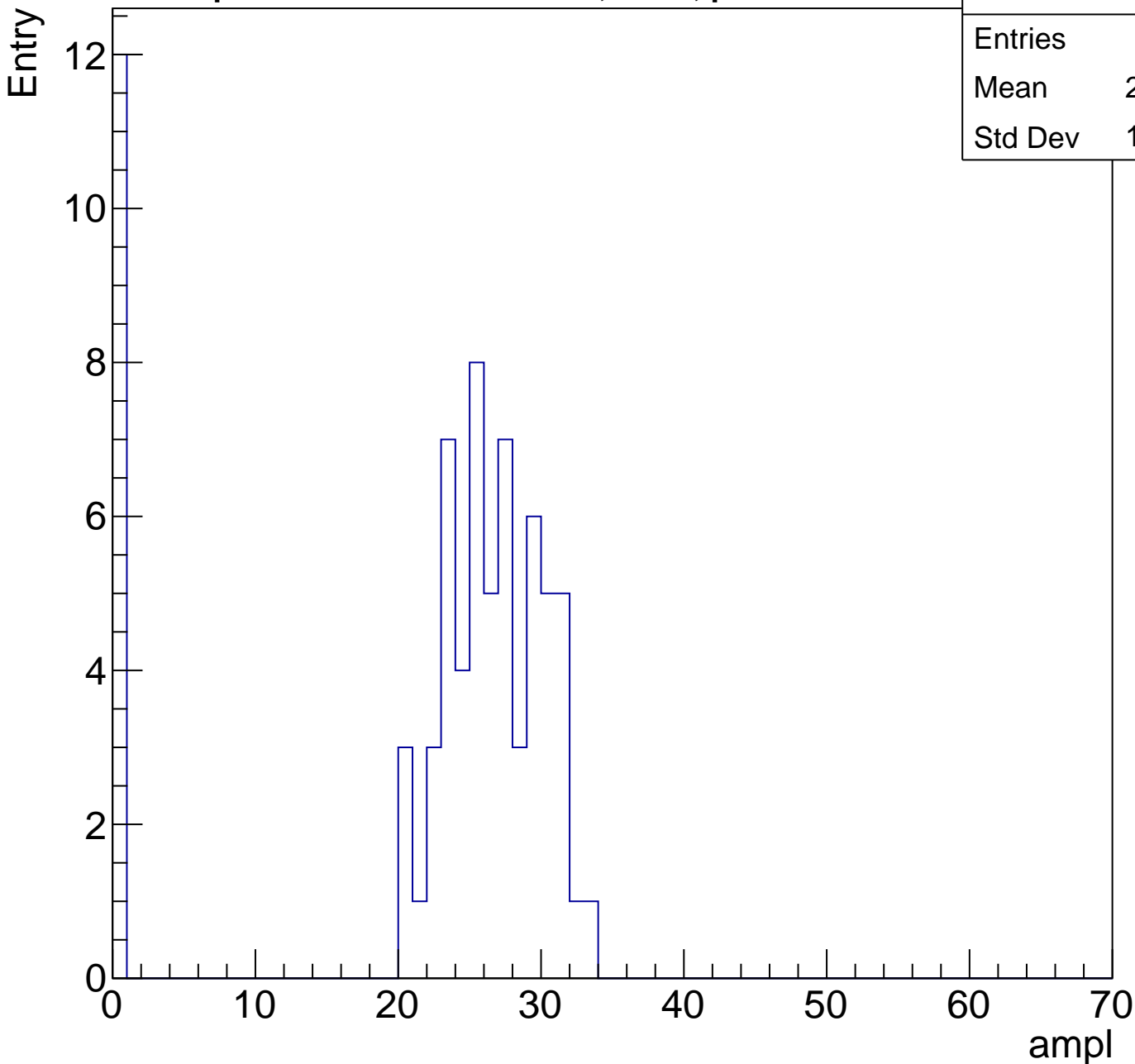
ampl



# B1L103S, U4-ch30, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

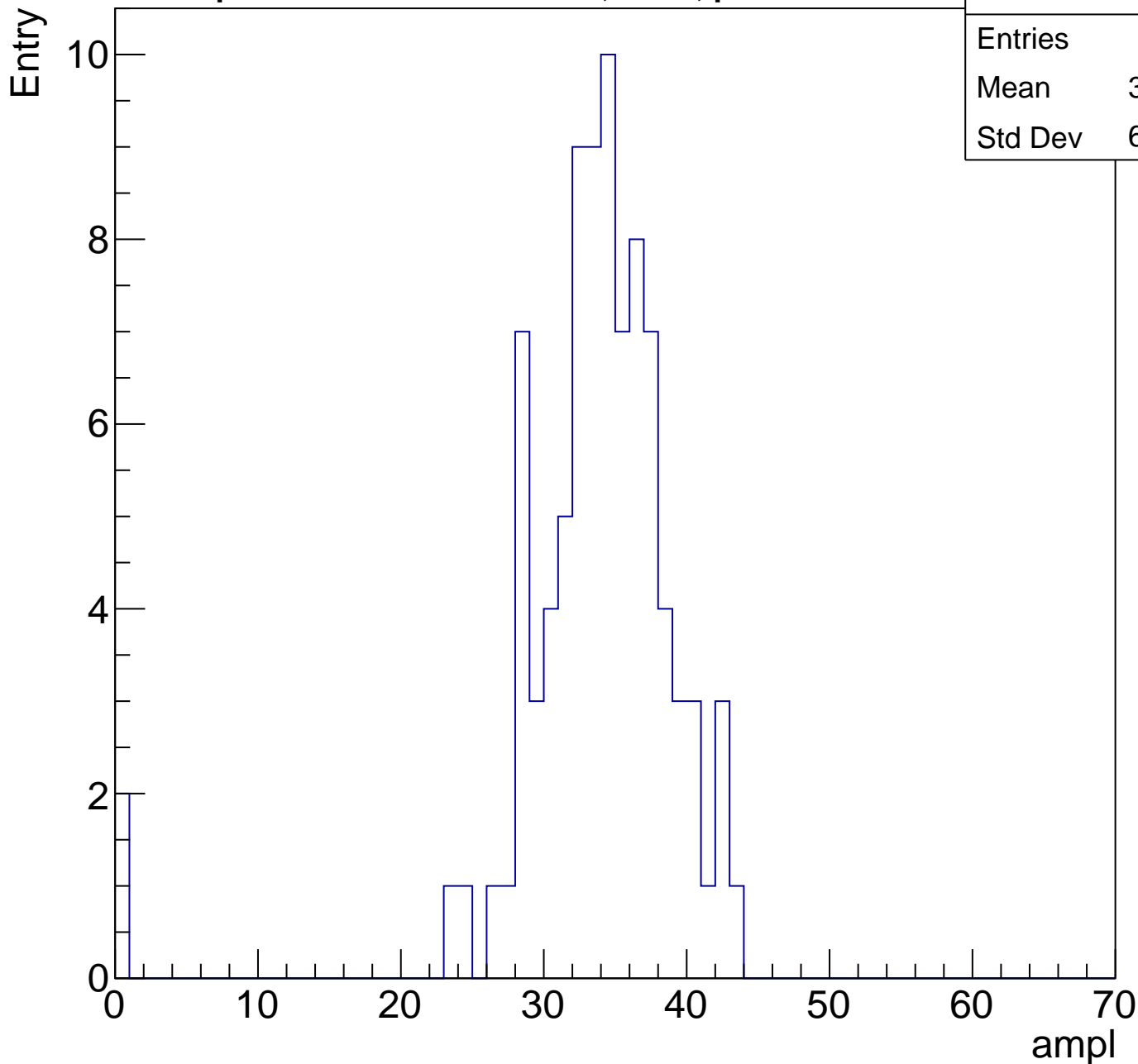
|         |       |
|---------|-------|
| Entries | 71    |
| Mean    | 21.85 |
| Std Dev | 10.29 |



# B1L103S, U4-ch30, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

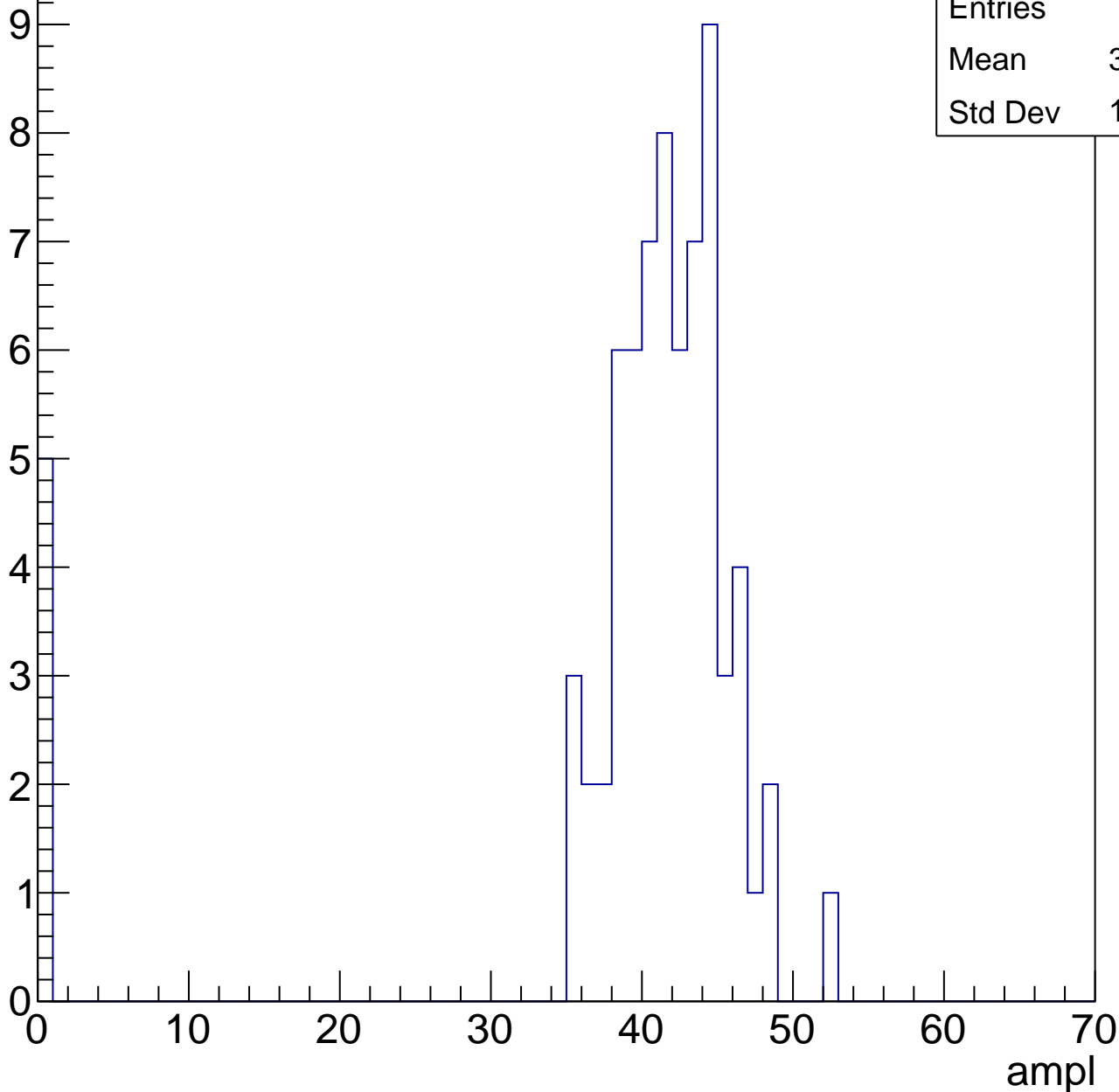
|         |       |
|---------|-------|
| Entries | 90    |
| Mean    | 33.04 |
| Std Dev | 6.425 |



# B1L103S, U4-ch30, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

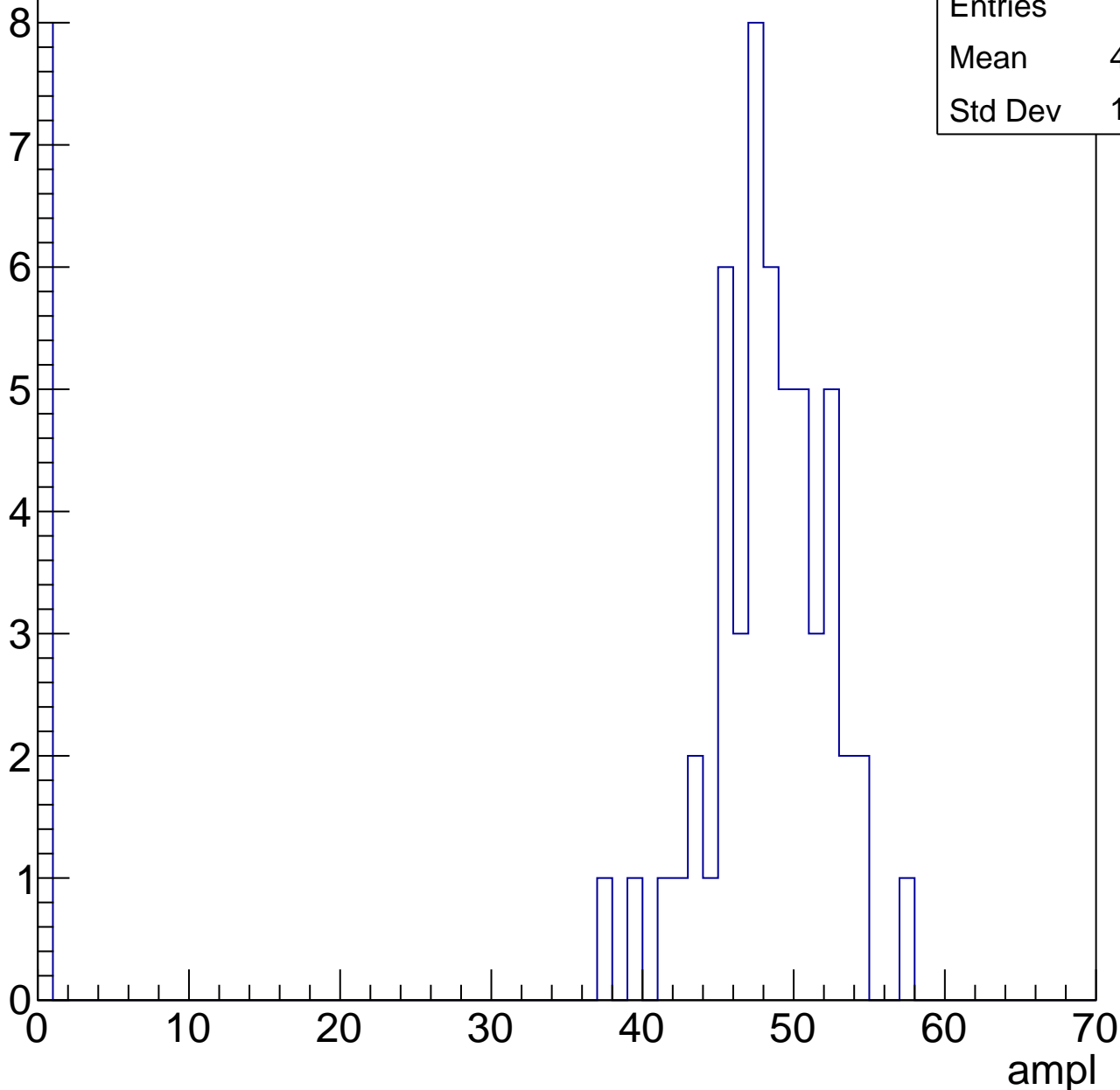


# B1L103S, U4-ch30, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

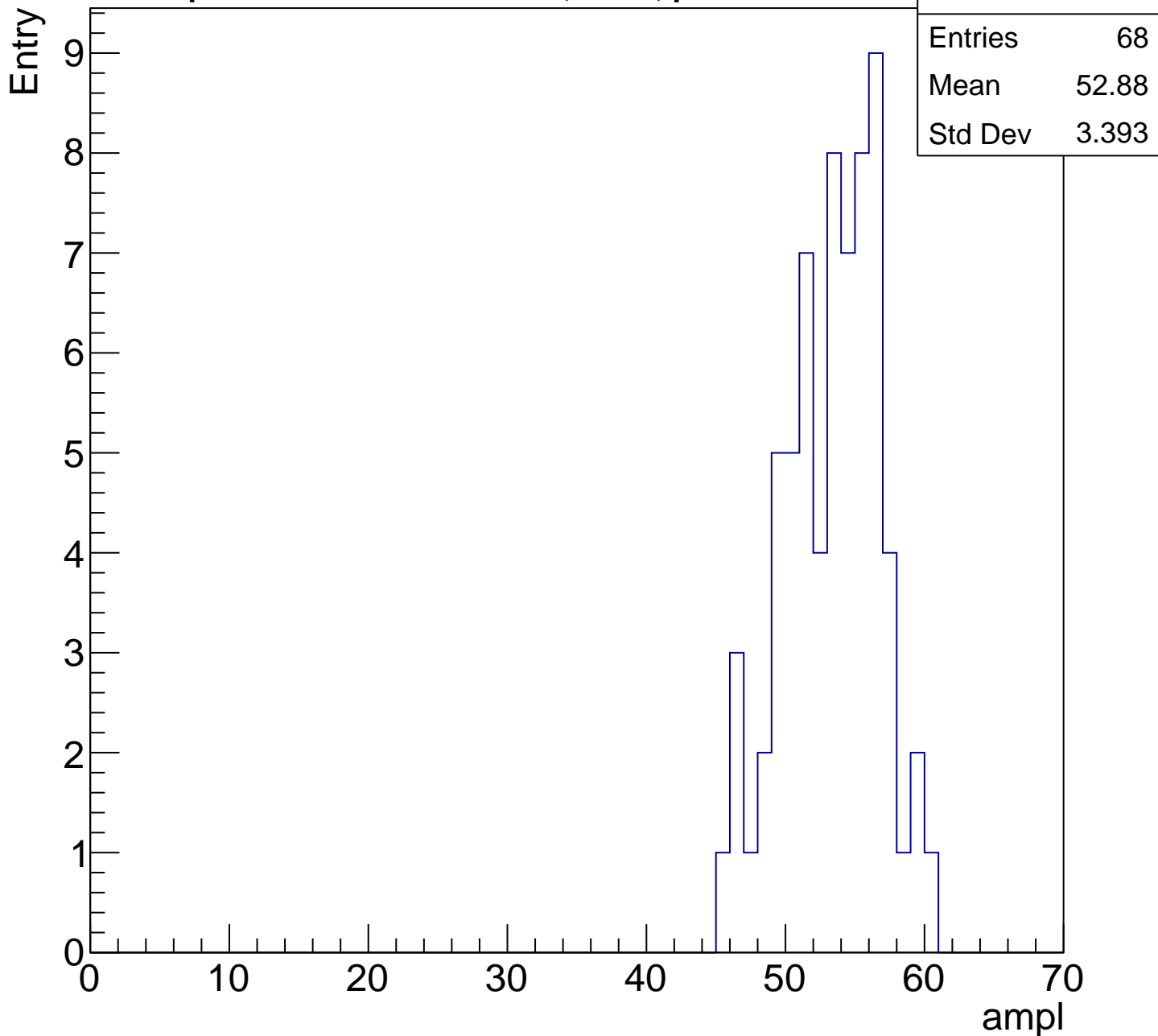
Entry

|         |       |
|---------|-------|
| Entries | 61    |
| Mean    | 41.64 |
| Std Dev | 16.56 |



# B1L103S, U4-ch30, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

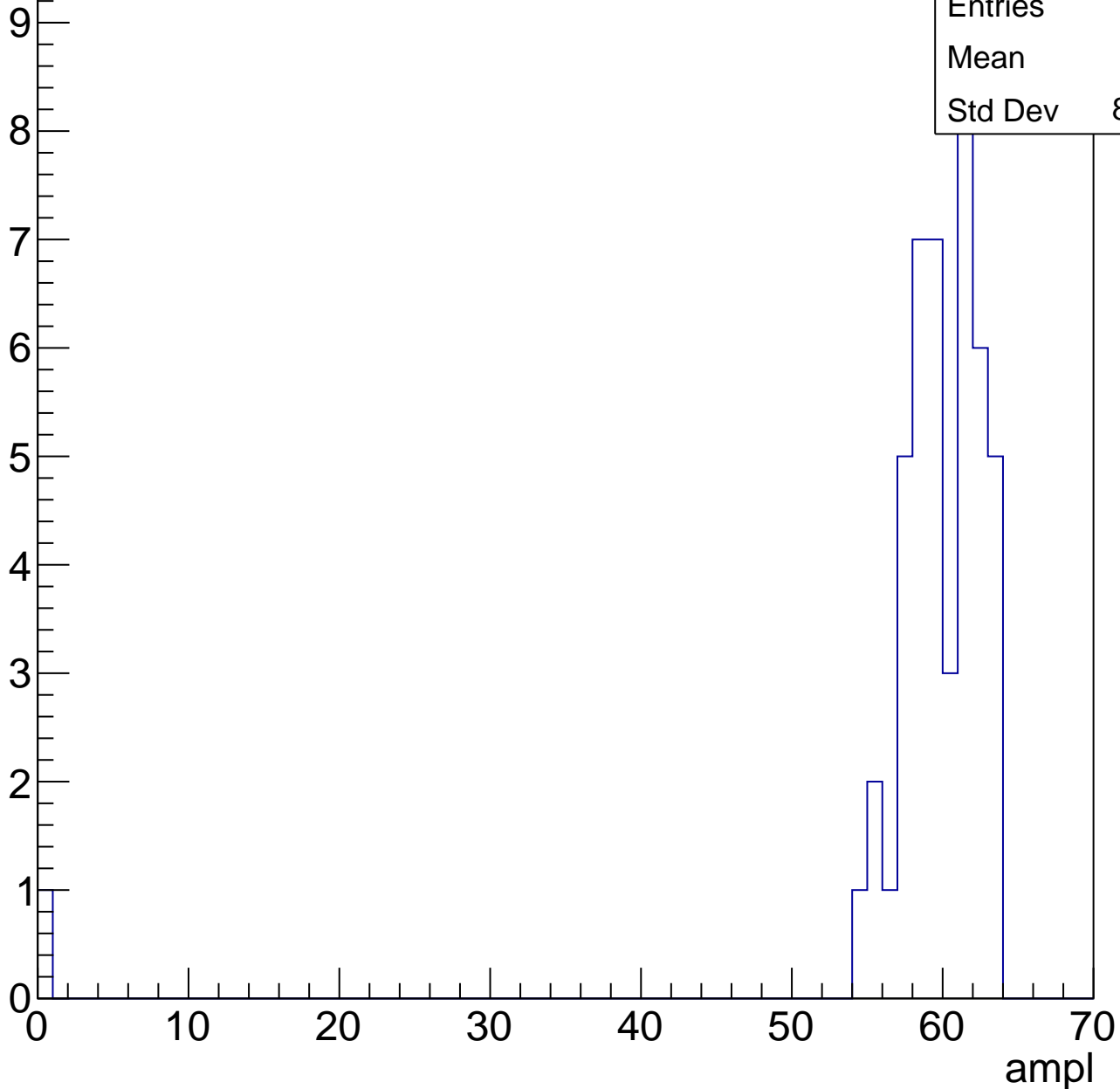


# B1L103S, U4-ch30, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

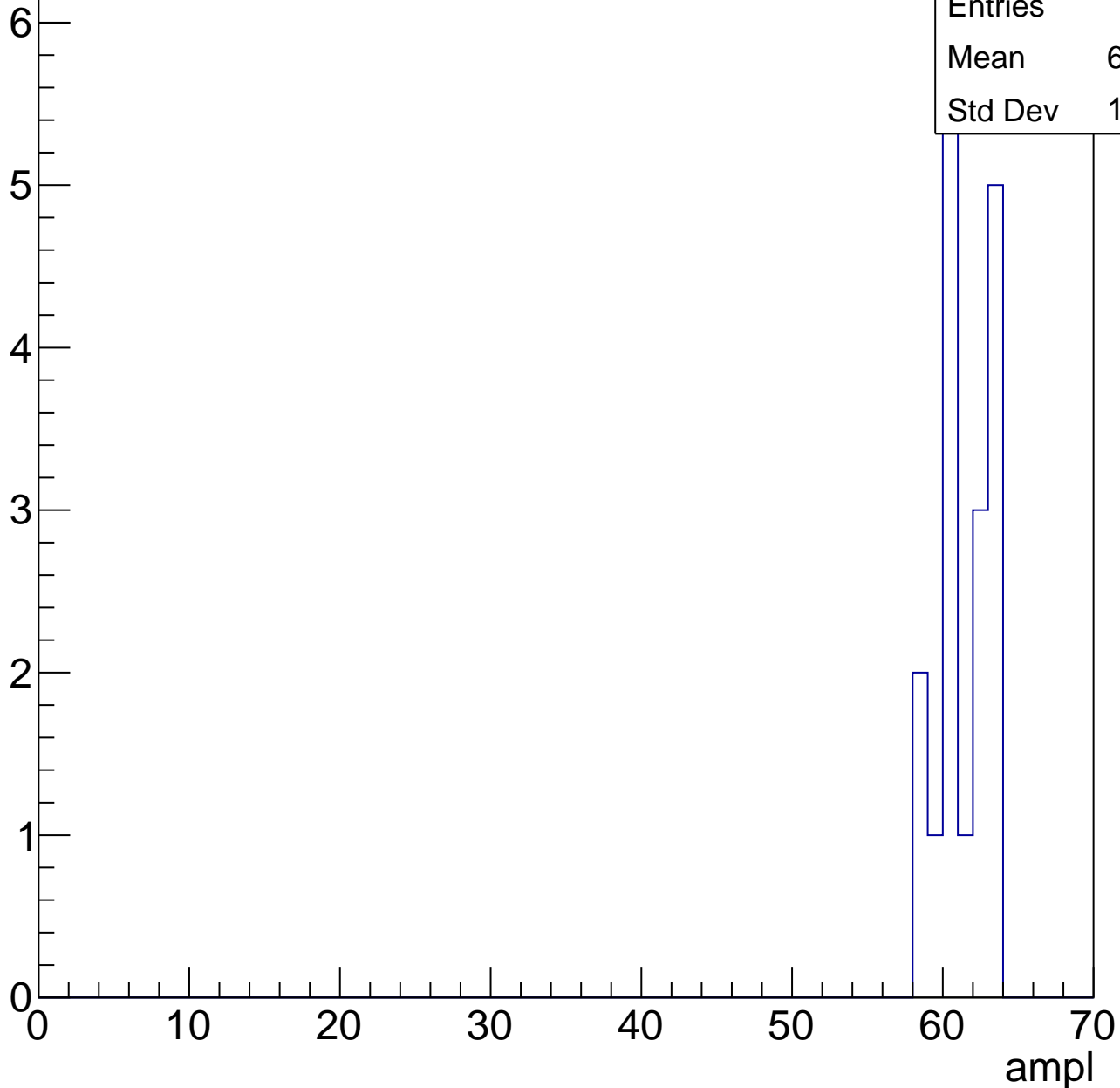
|         |       |
|---------|-------|
| Entries | 47    |
| Mean    | 58.3  |
| Std Dev | 8.901 |



# B1L103S, U4-ch30, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



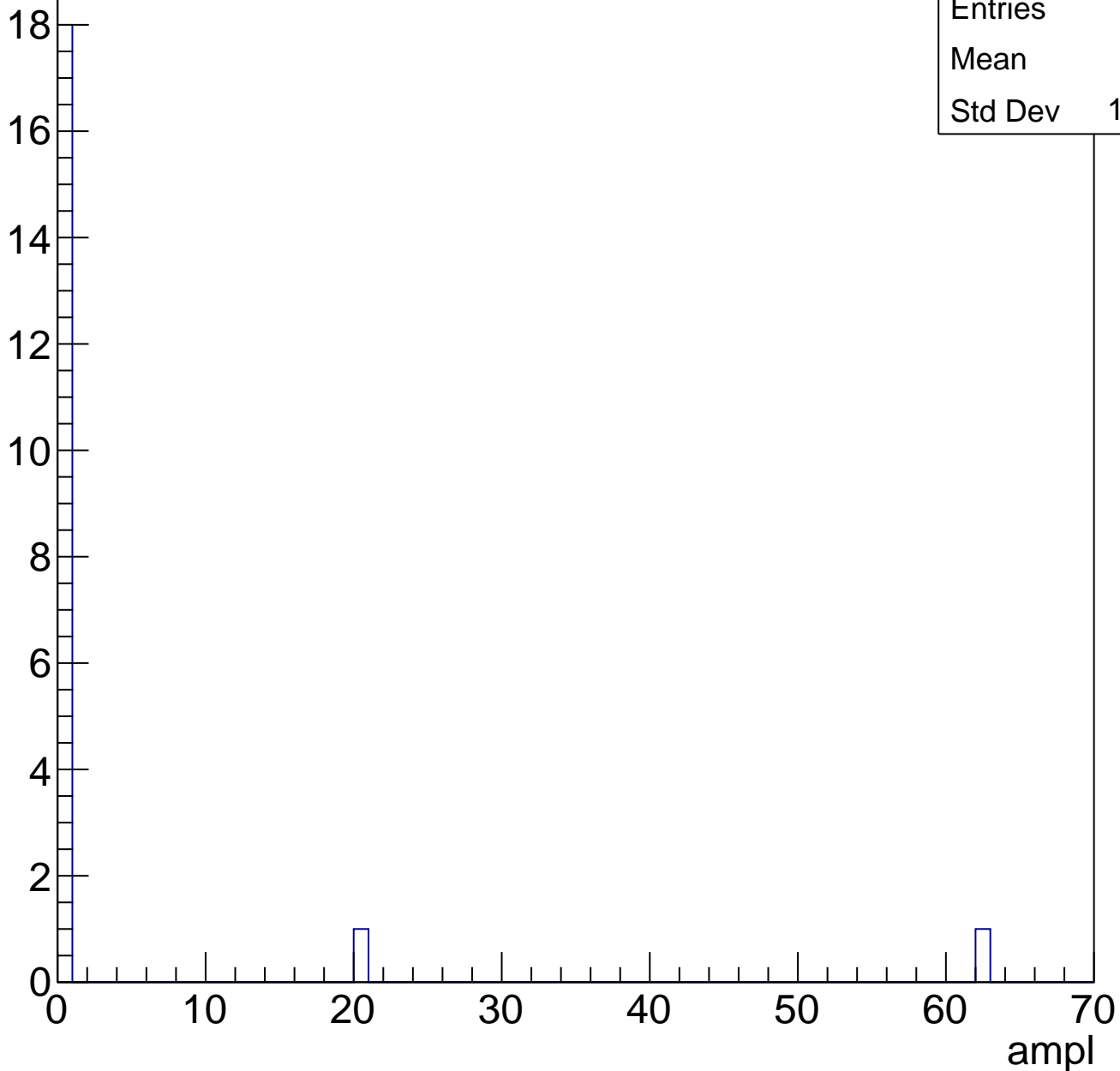


# B1L103S, U4-ch30, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 20    |
| Mean    | 4.1   |
| Std Dev | 13.98 |

Entry

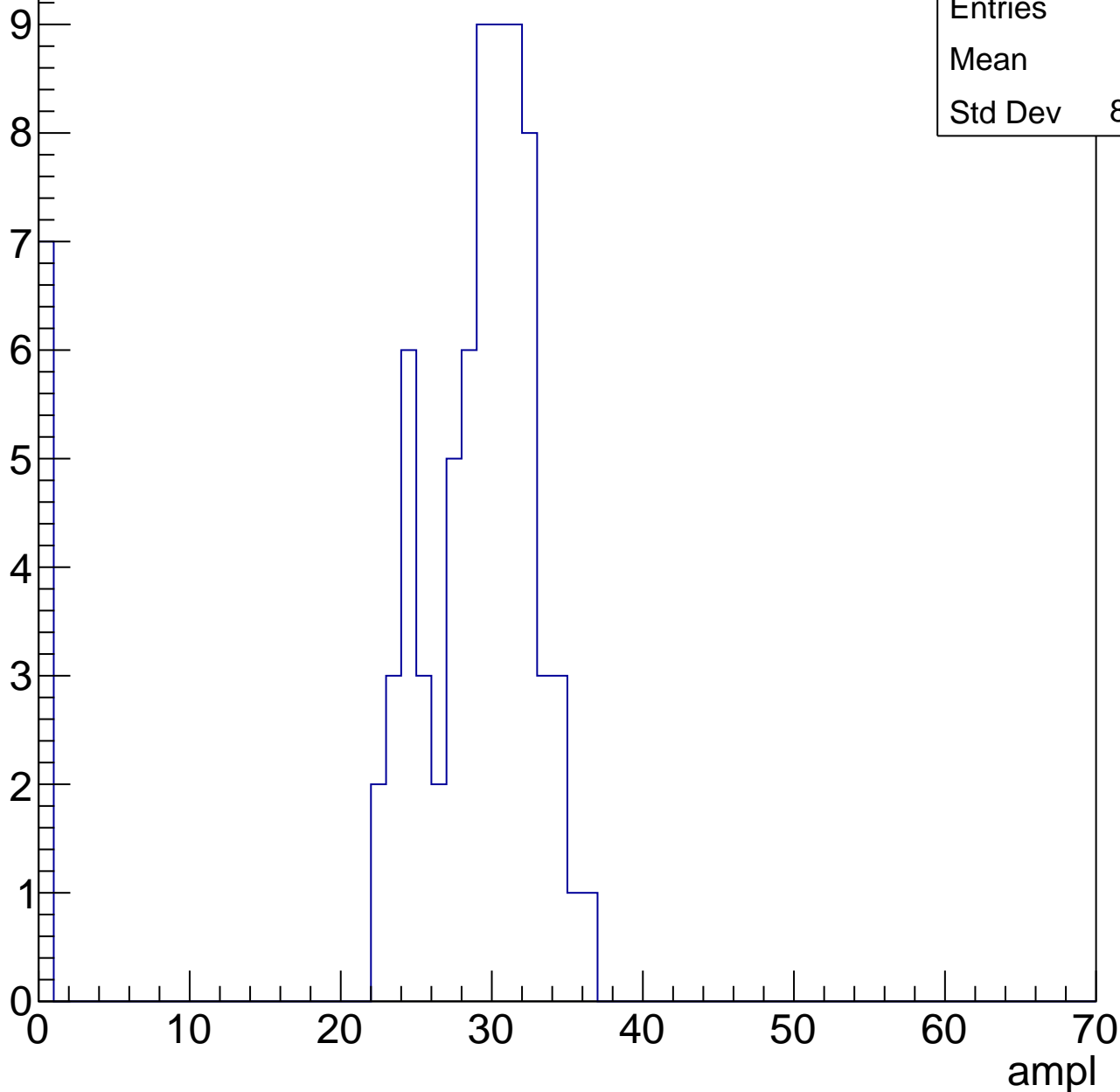


# B1L103S, U4-ch31, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 77    |
| Mean    | 26.3  |
| Std Dev | 8.899 |

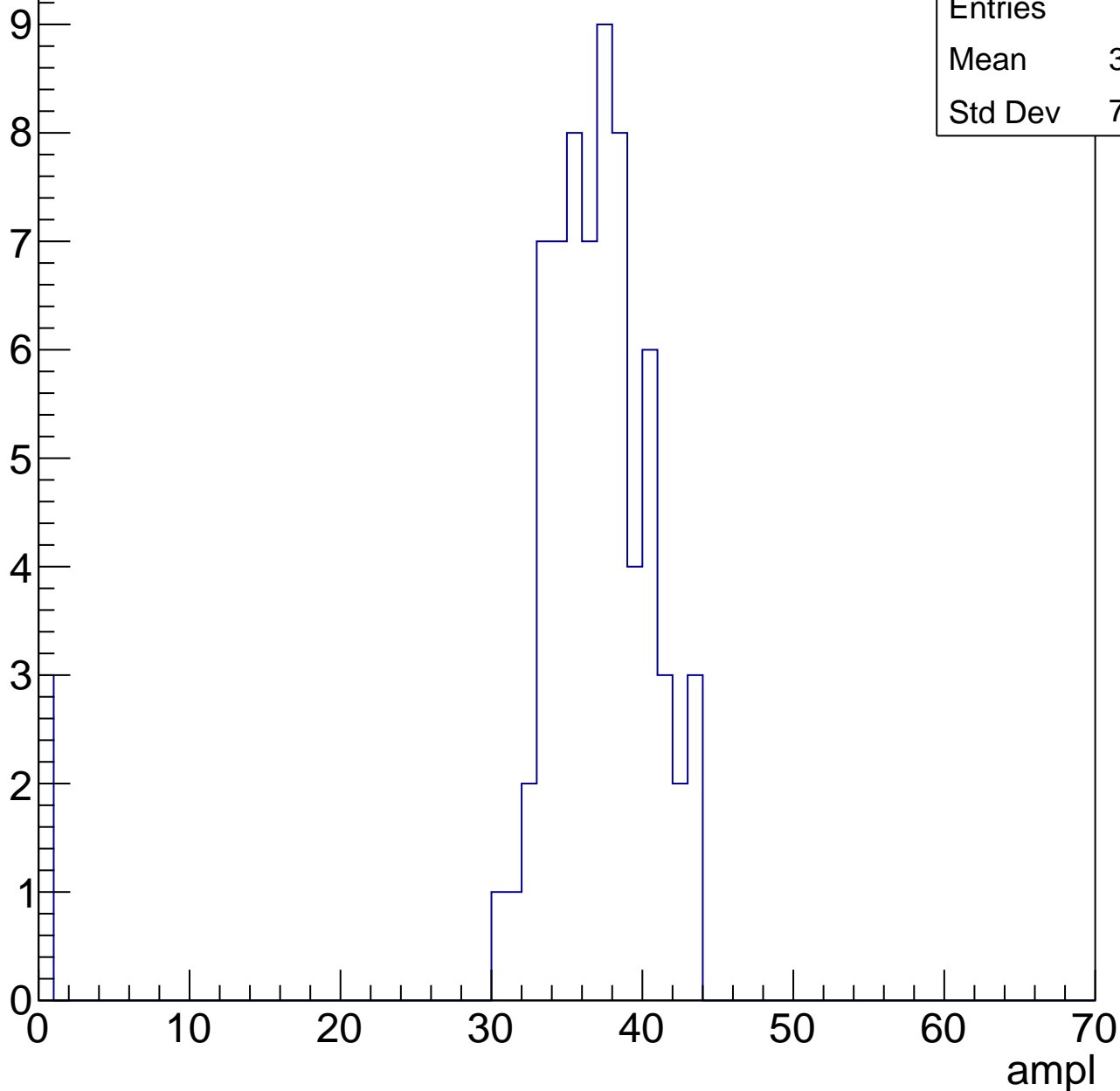


# B1L103S, U4-ch31, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 71    |
| Mean    | 35.14 |
| Std Dev | 7.956 |

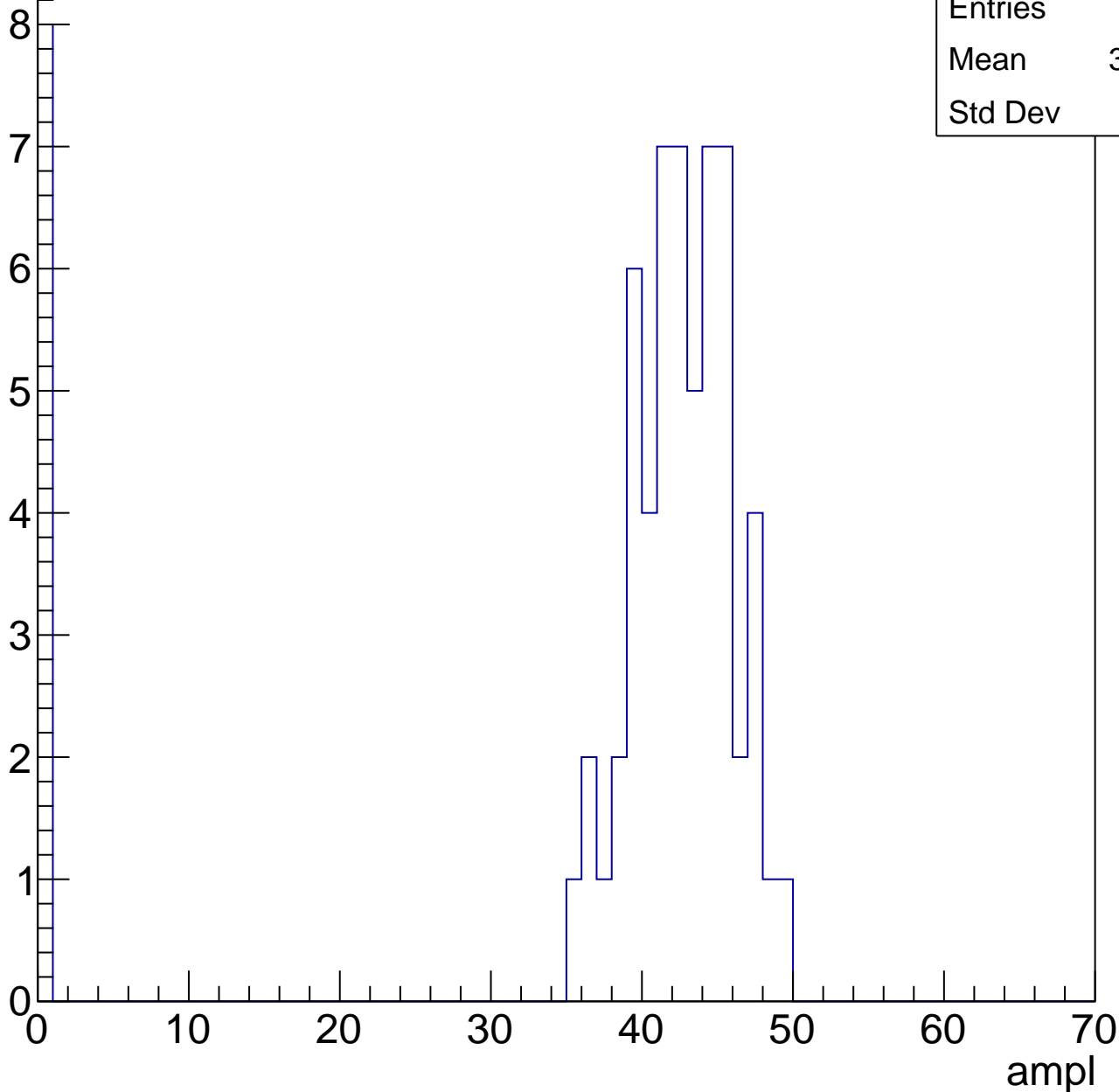


# B1L103S, U4-ch31, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 65    |
| Mean    | 37.08 |
| Std Dev | 14.2  |

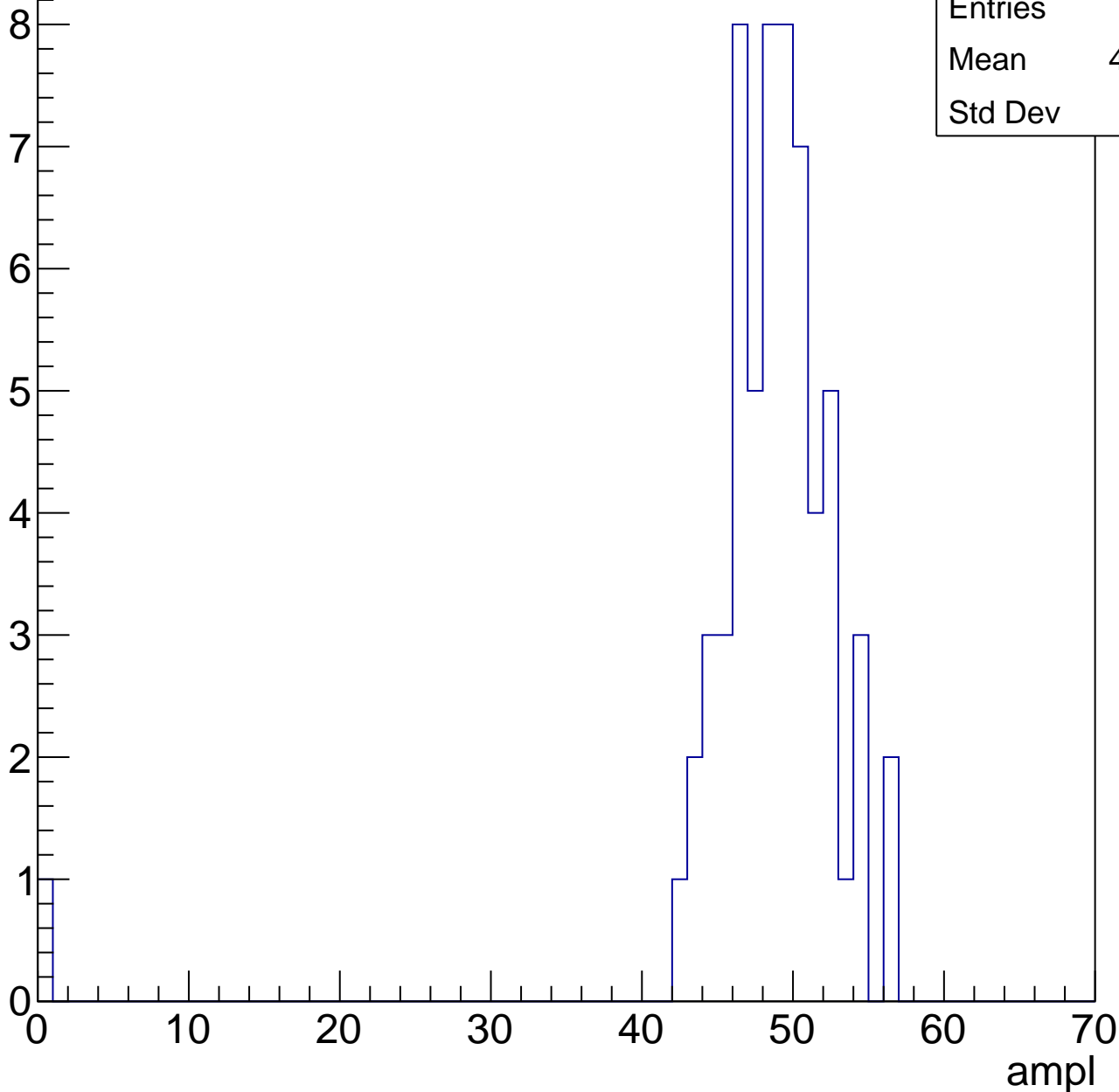


# B1L103S, U4-ch31, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

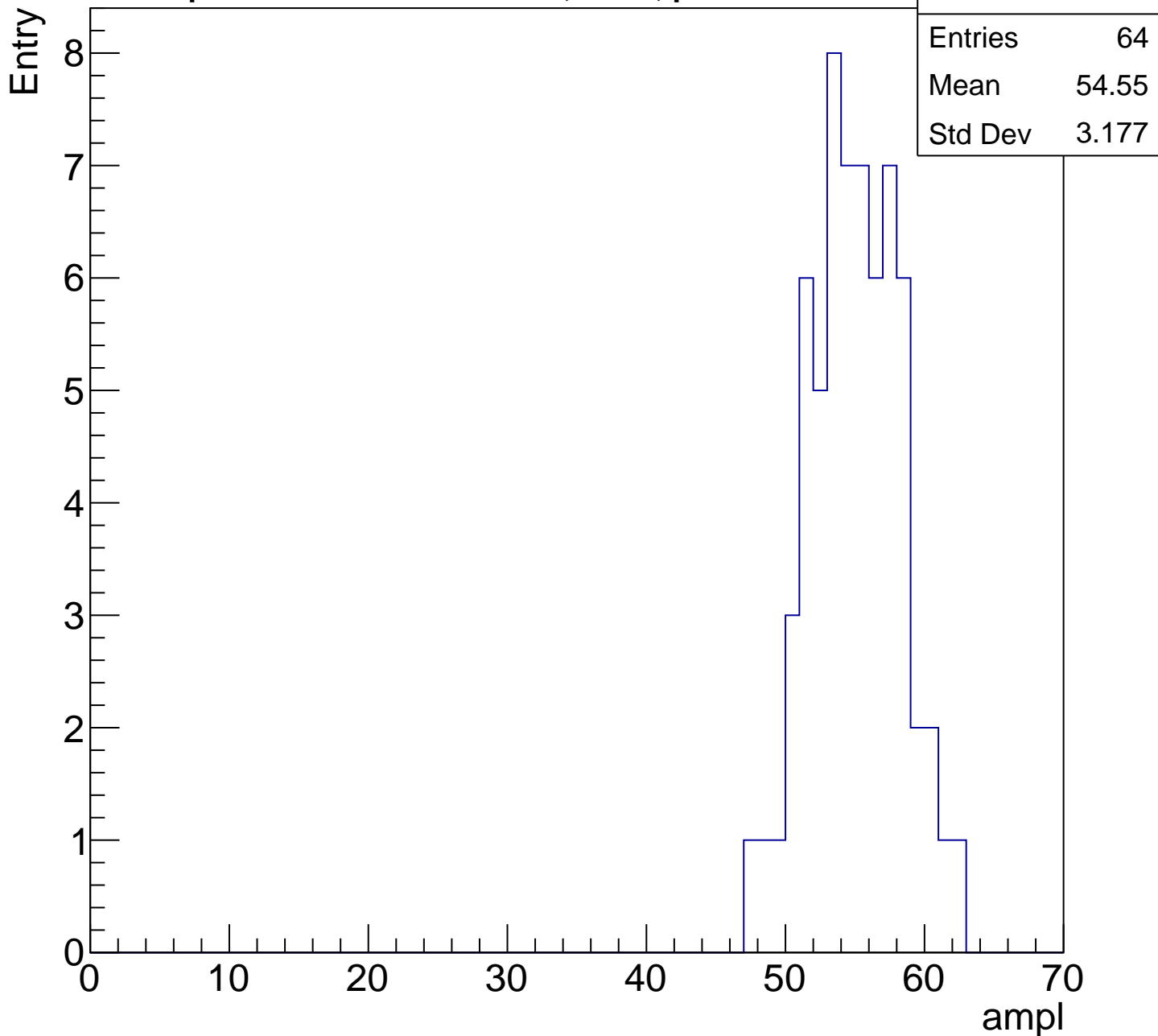
Entry

|         |       |
|---------|-------|
| Entries | 61    |
| Mean    | 47.79 |
| Std Dev | 6.91  |



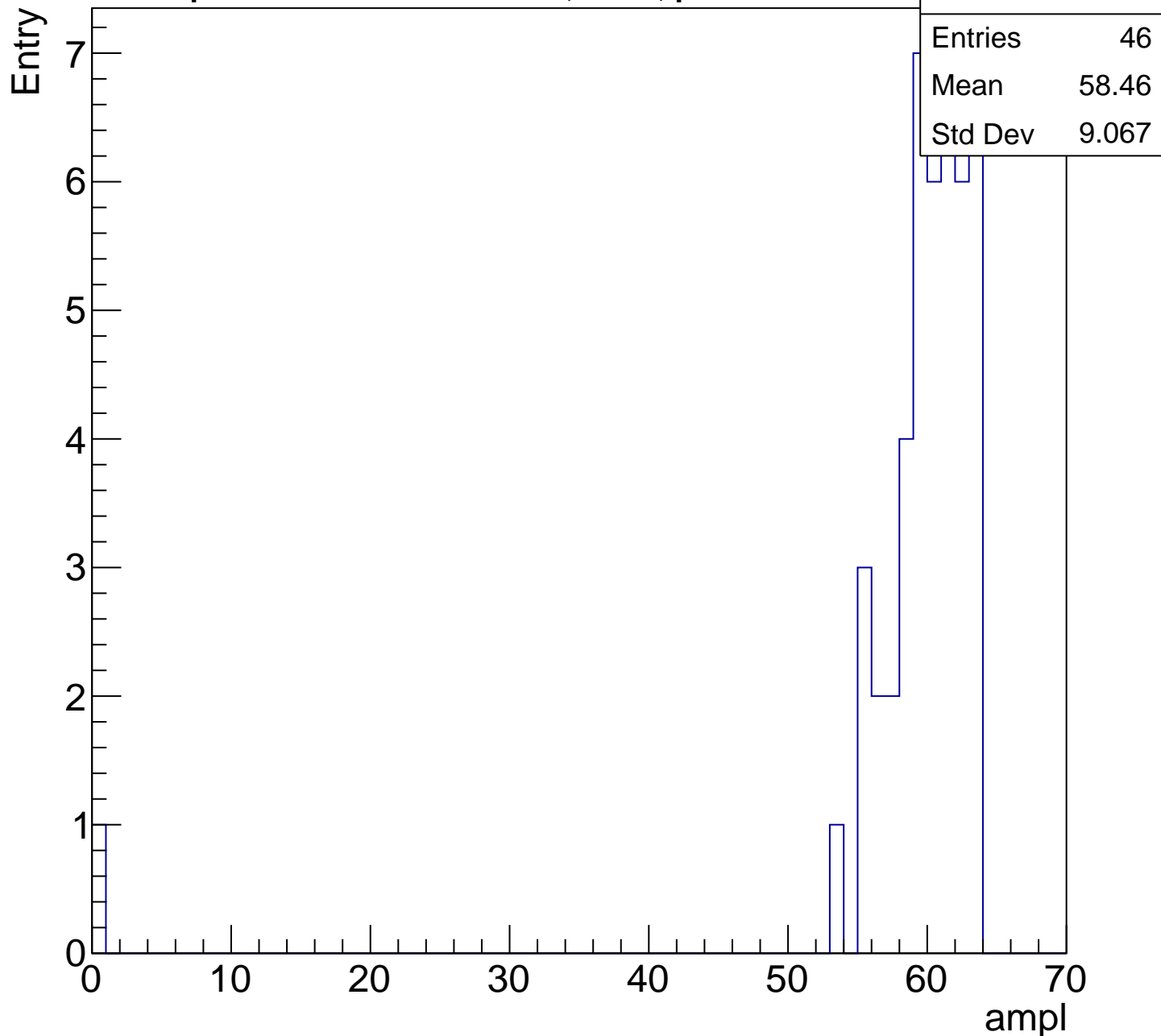
# B1L103S, U4-ch31, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2



# B1L103S, U4-ch31, adc5

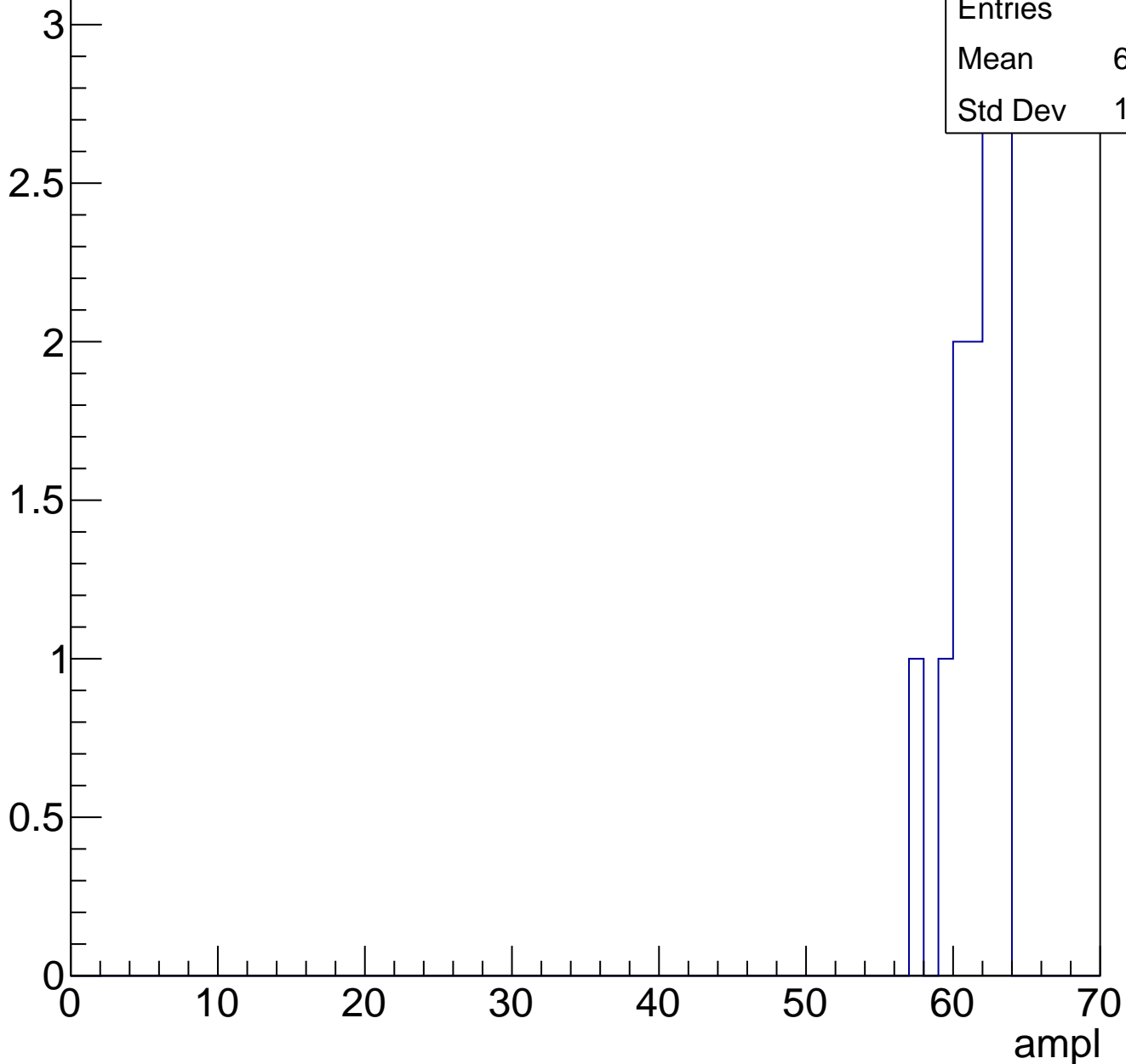
calib\_packv5\_041523\_1651.root, FC#0, port C2



# B1L103S, U4-ch31, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U4-ch31, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

|         |    |
|---------|----|
| Entries | 19 |
| Mean    | 0  |
| Std Dev | 0  |

ampl

# B1L103S, U4-ch32, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 90    |
| Mean    | 23.53 |
| Std Dev | 9.393 |

Entry

10

8

6

4

2

0

0

10

20

30

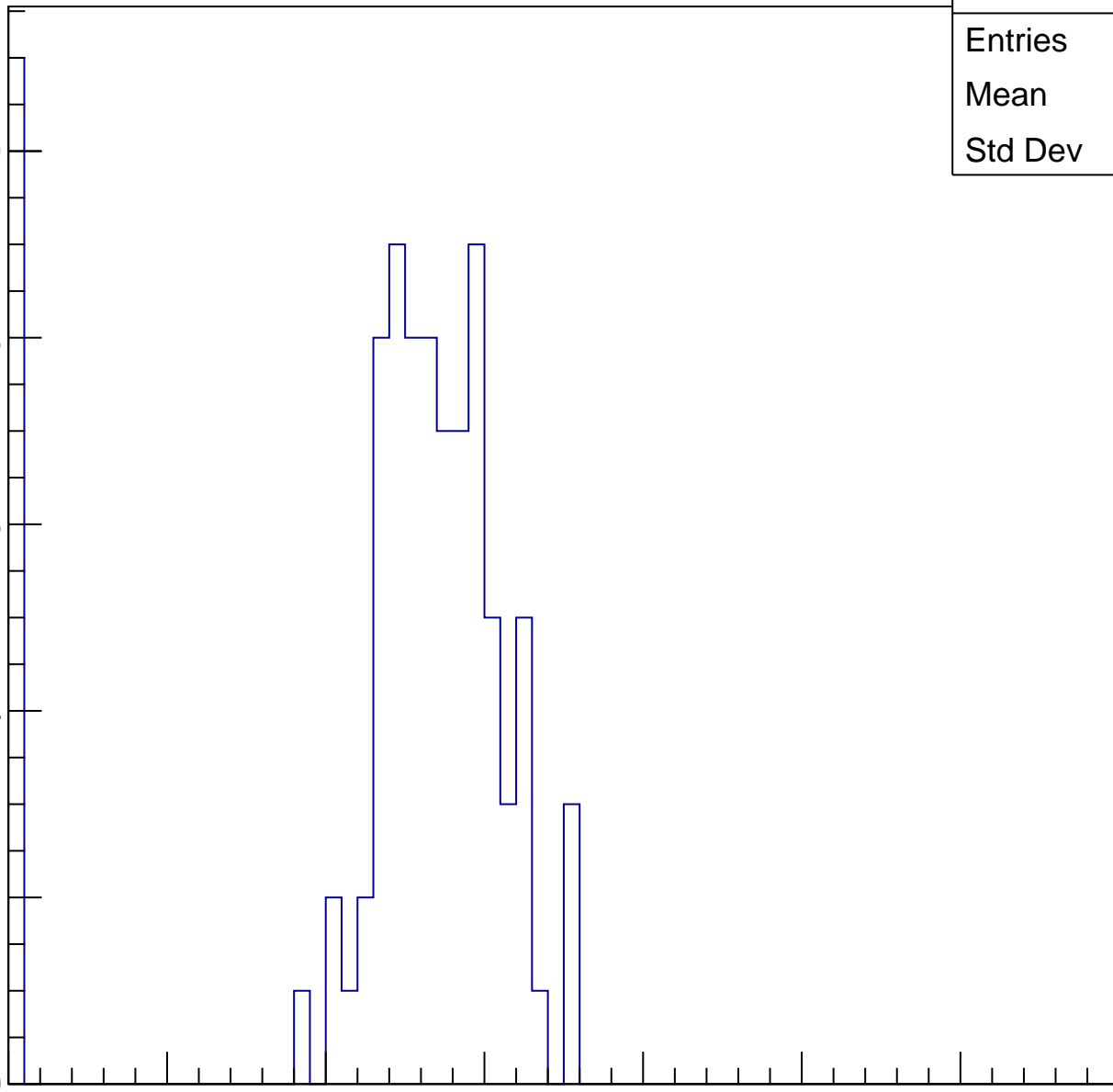
40

50

60

70

ampl

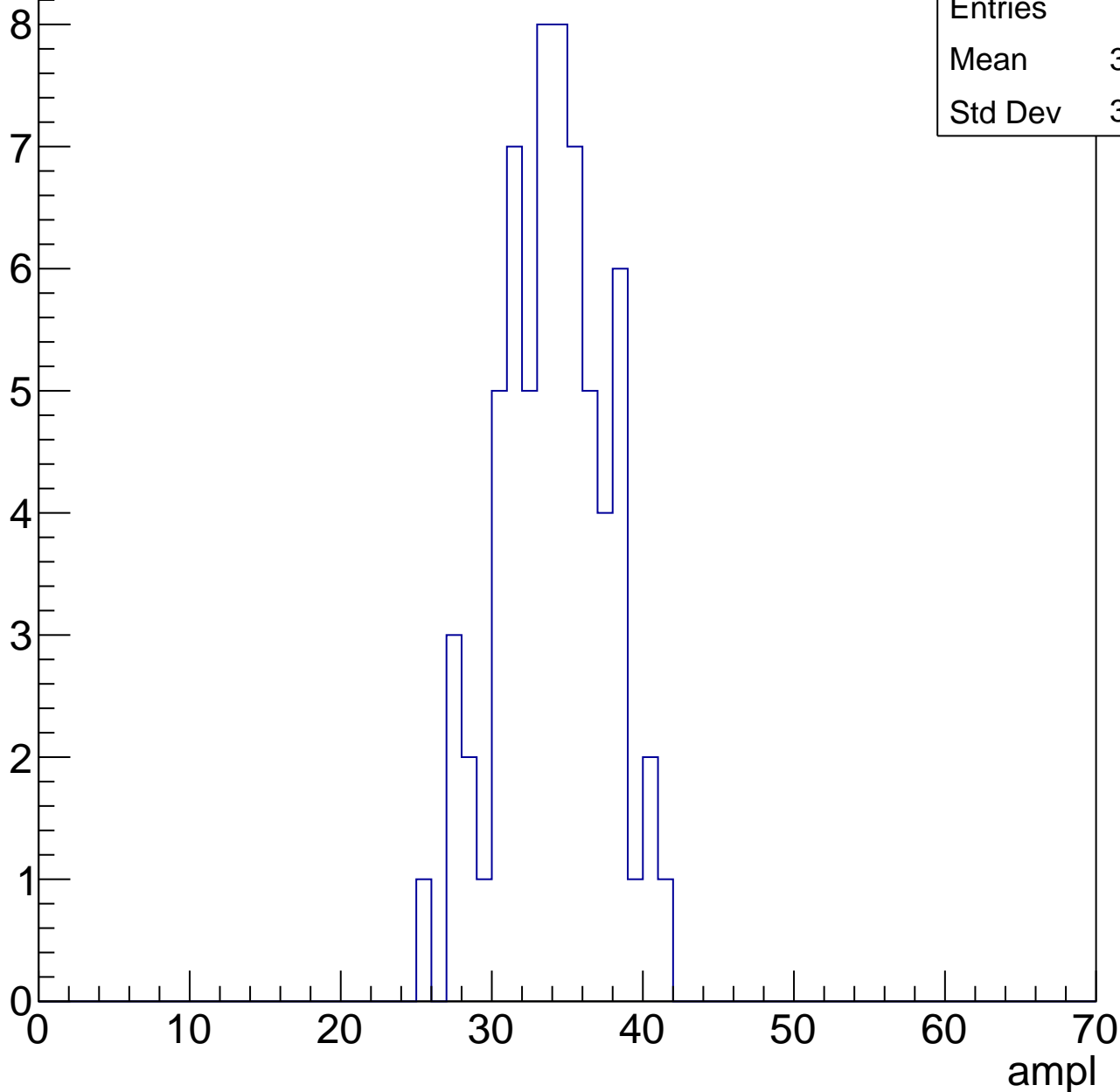


# B1L103S, U4-ch32, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

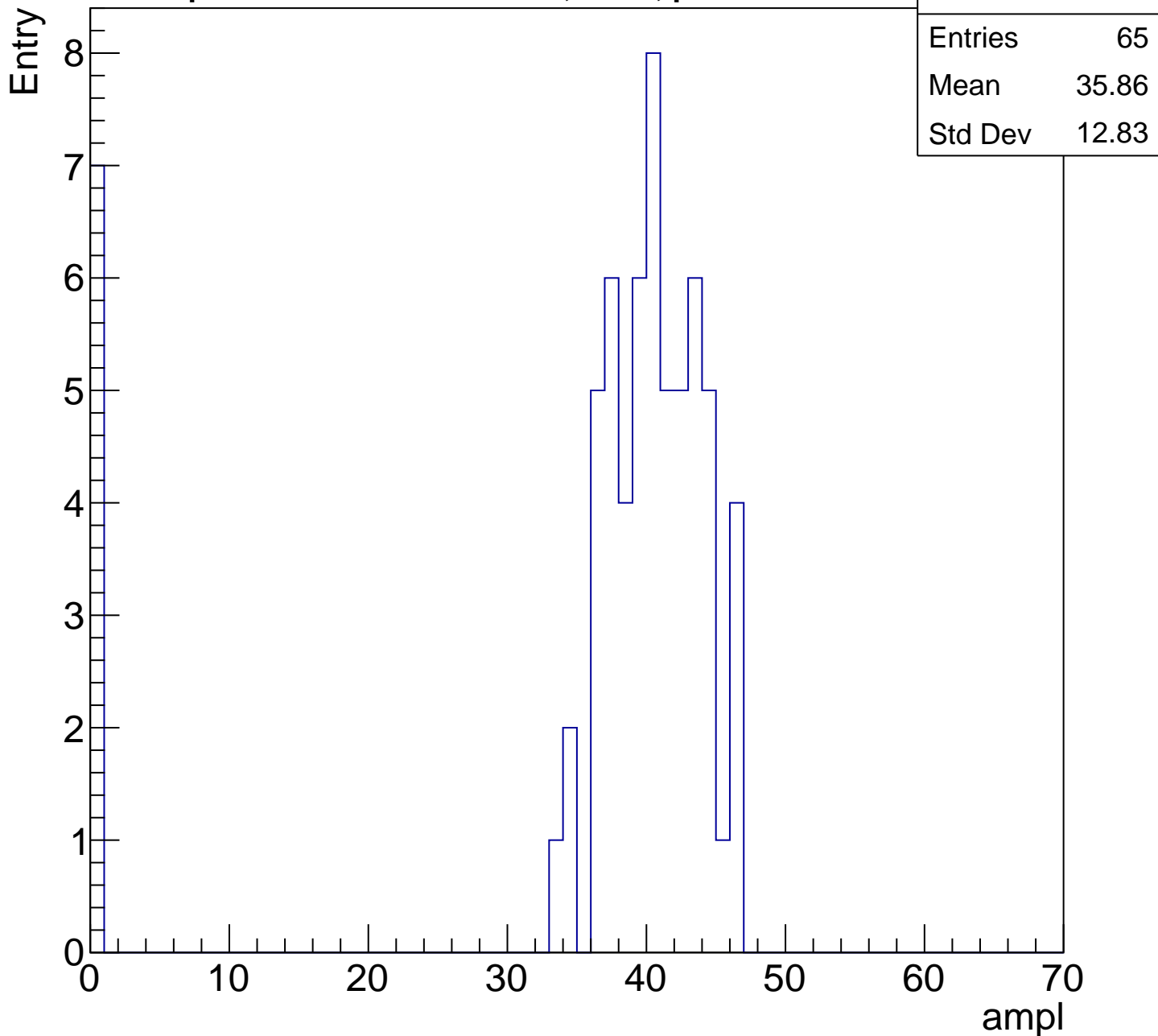
Entry

|         |       |
|---------|-------|
| Entries | 66    |
| Mean    | 33.56 |
| Std Dev | 3.456 |



# B1L103S, U4-ch32, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

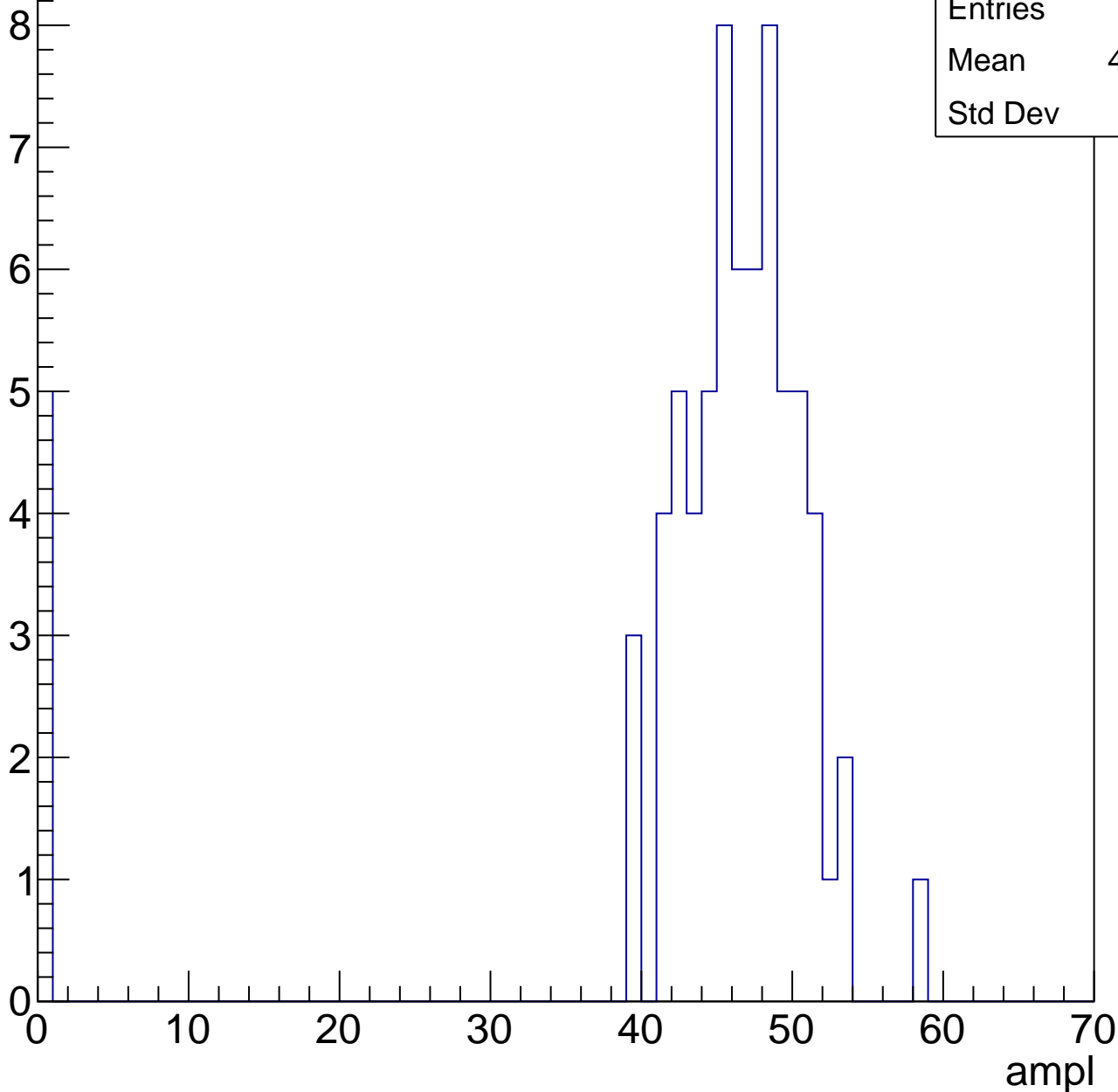


# B1L103S, U4-ch32, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

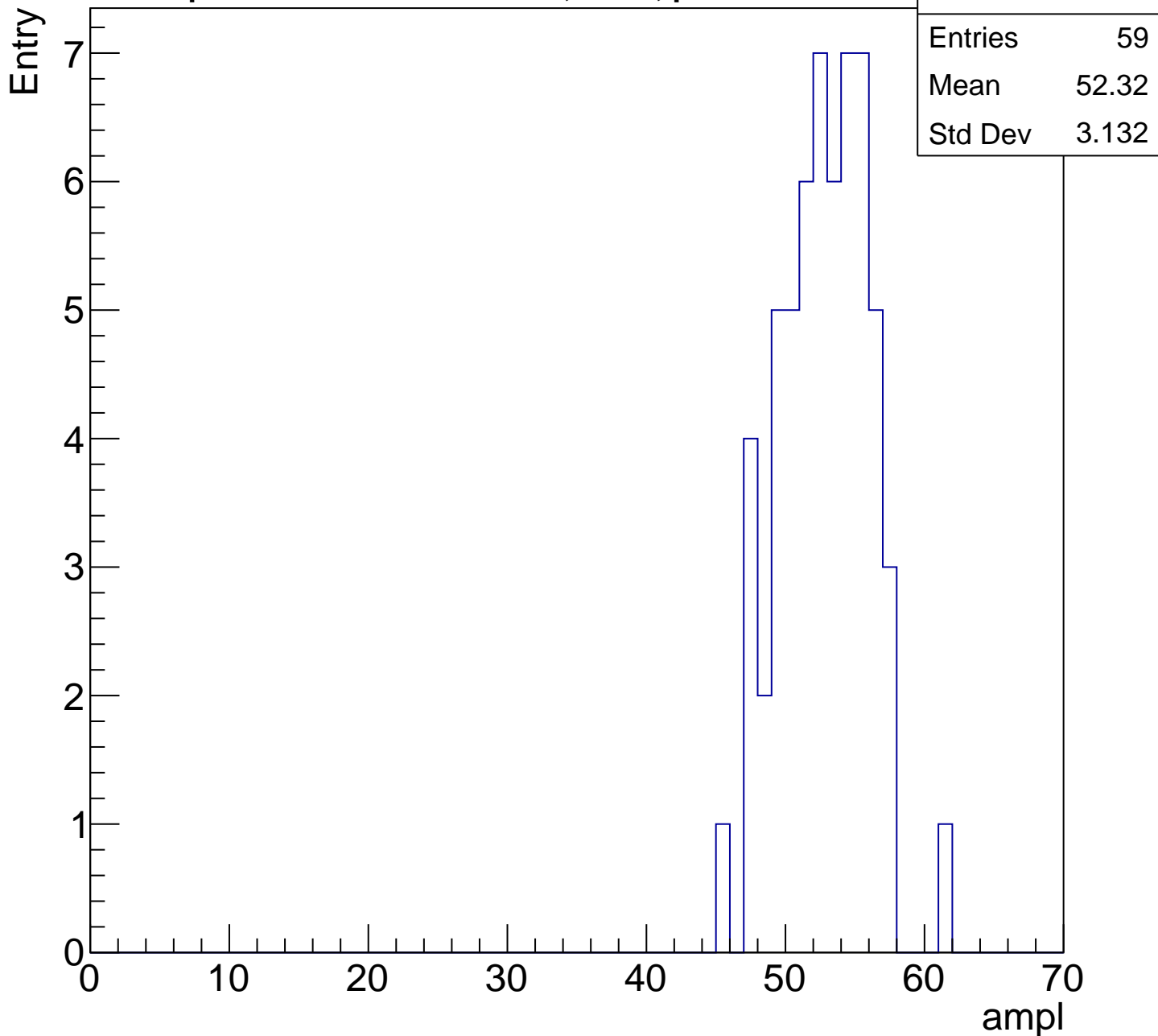
Entry

|         |       |
|---------|-------|
| Entries | 72    |
| Mean    | 43.06 |
| Std Dev | 12.3  |



# B1L103S, U4-ch32, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2



# B1L103S, U4-ch32, adc5

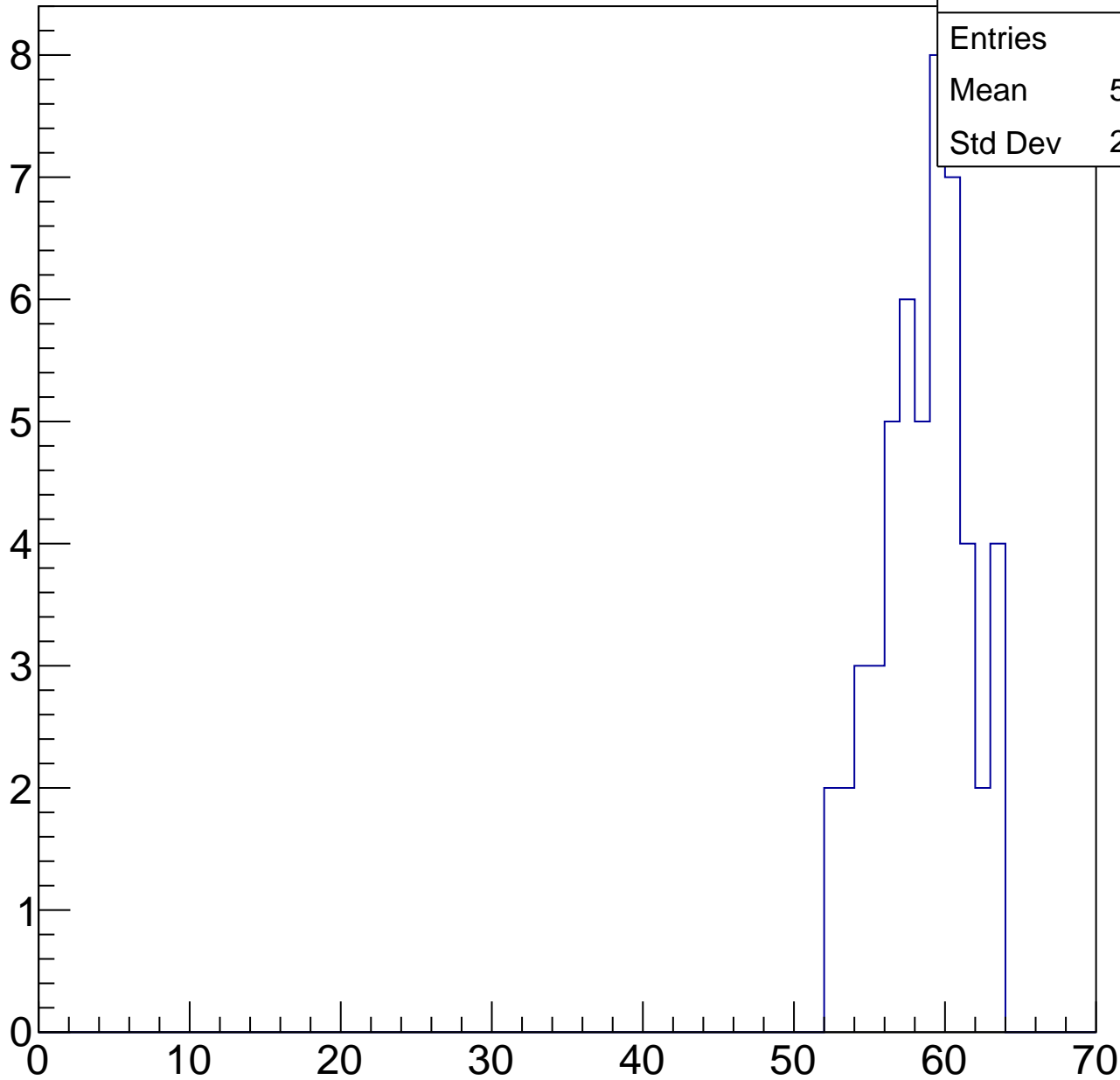
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

|         |       |
|---------|-------|
| Entries | 51    |
| Mean    | 58.06 |
| Std Dev | 2.893 |

ampl

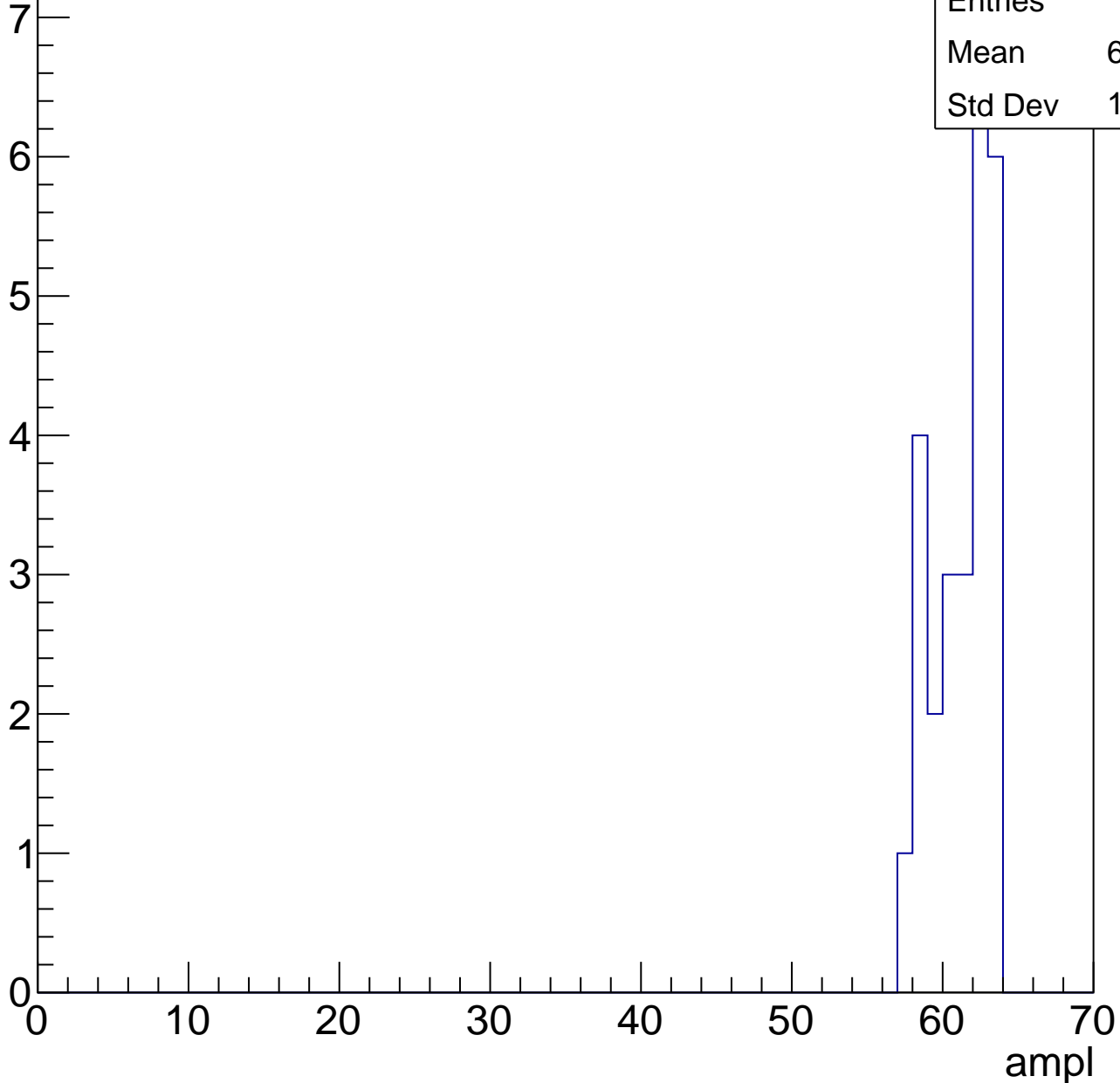


# B1L103S, U4-ch32, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 26    |
| Mean    | 60.85 |
| Std Dev | 1.895 |

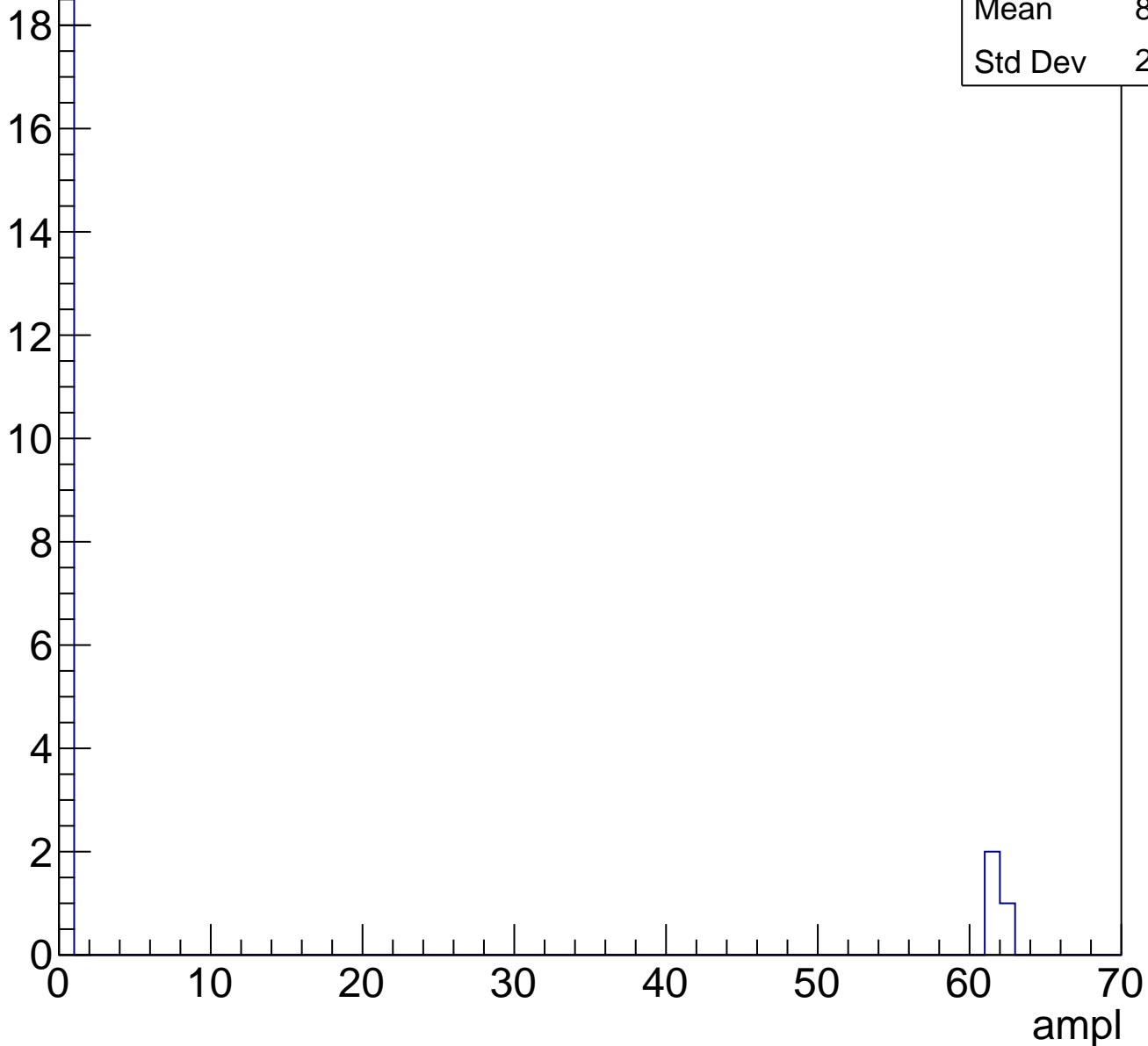




# B1L103S, U4-ch32, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



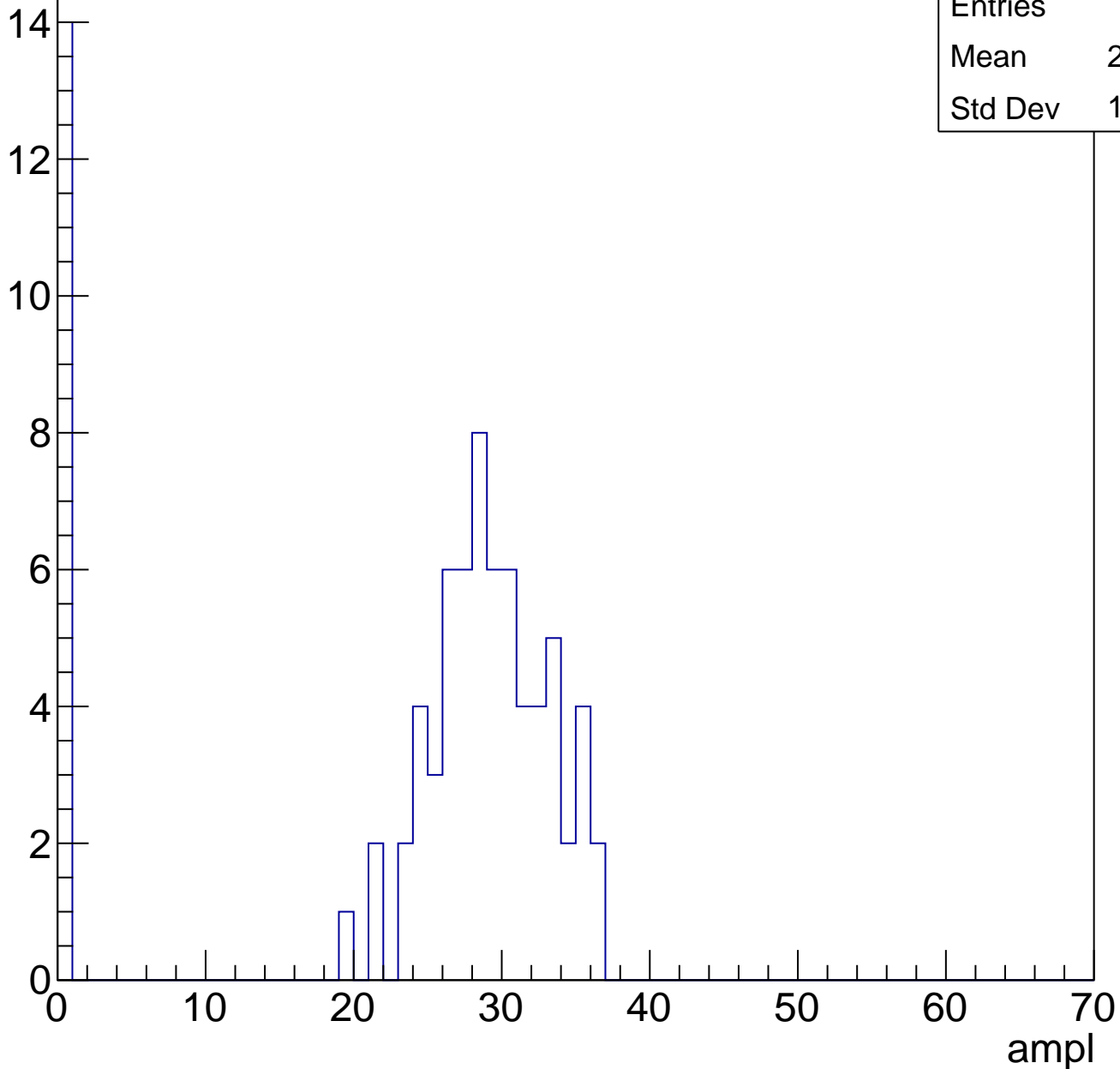
|         |       |
|---------|-------|
| Entries | 22    |
| Mean    | 8.364 |
| Std Dev | 21.05 |

# B1L103S, U4-ch33, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 79    |
| Mean    | 23.68 |
| Std Dev | 11.53 |

Entry

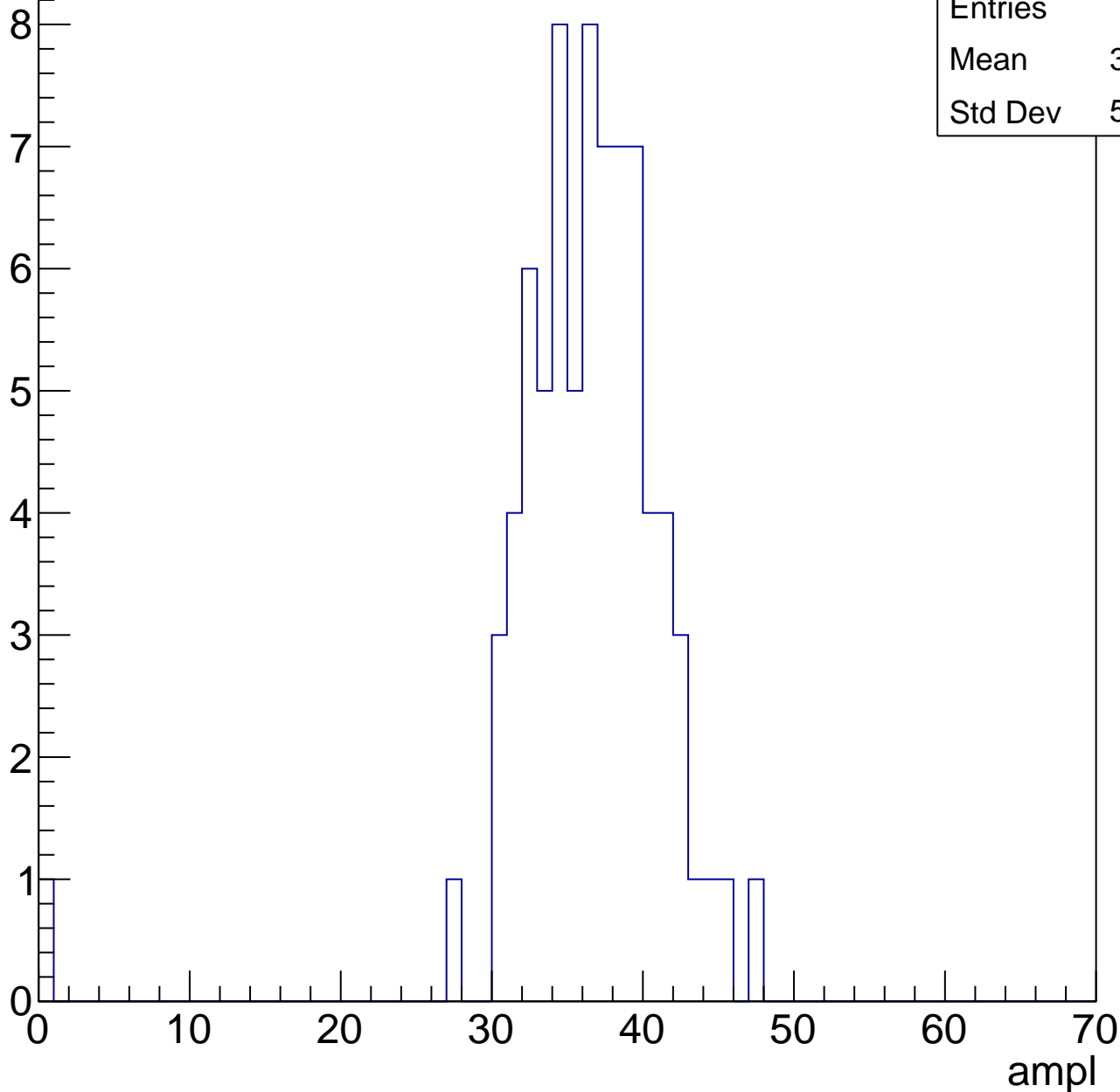


# B1L103S, U4-ch33, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 77    |
| Mean    | 35.84 |
| Std Dev | 5.636 |

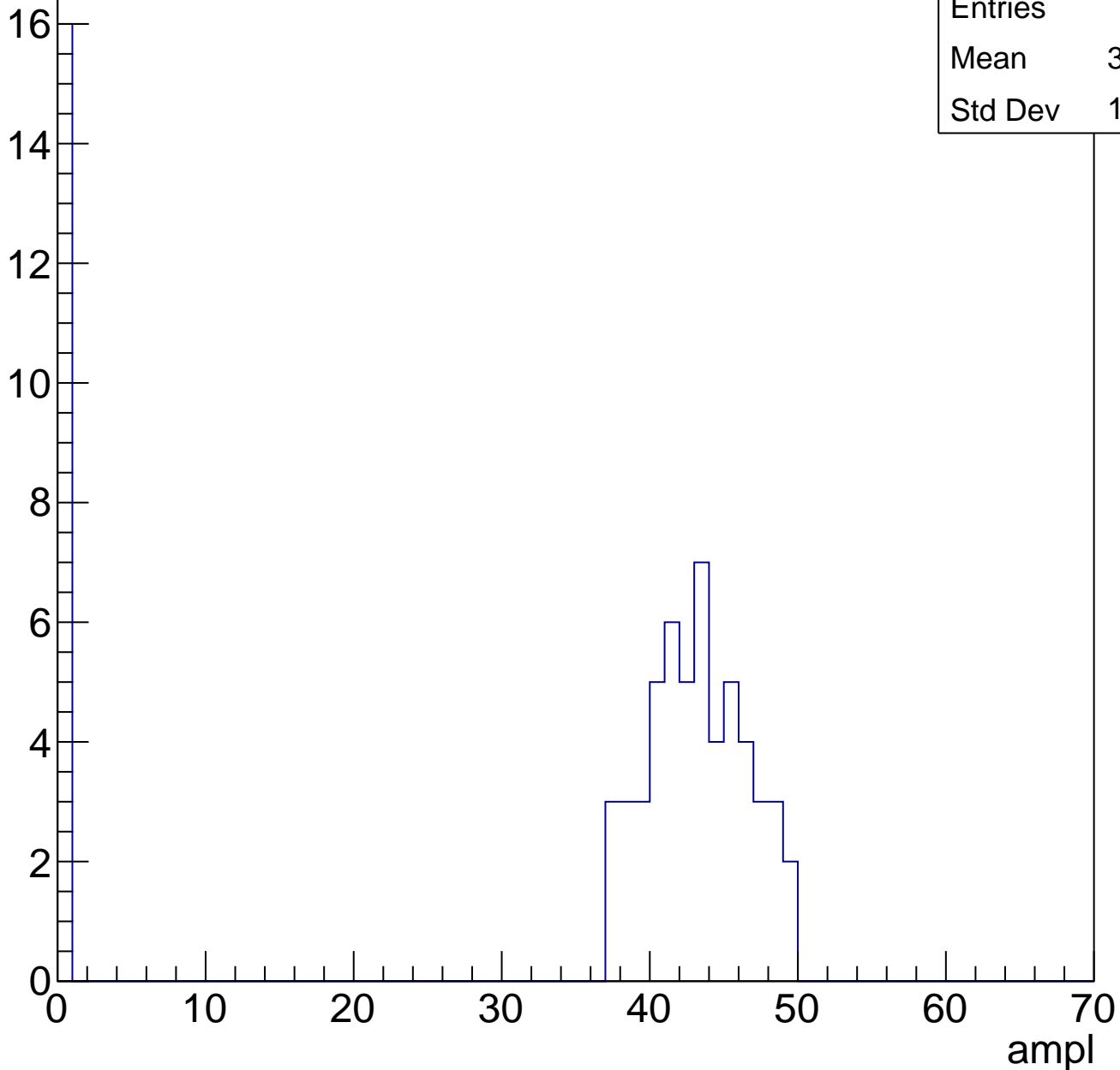


# B1L103S, U4-ch33, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 69    |
| Mean    | 32.86 |
| Std Dev | 18.27 |

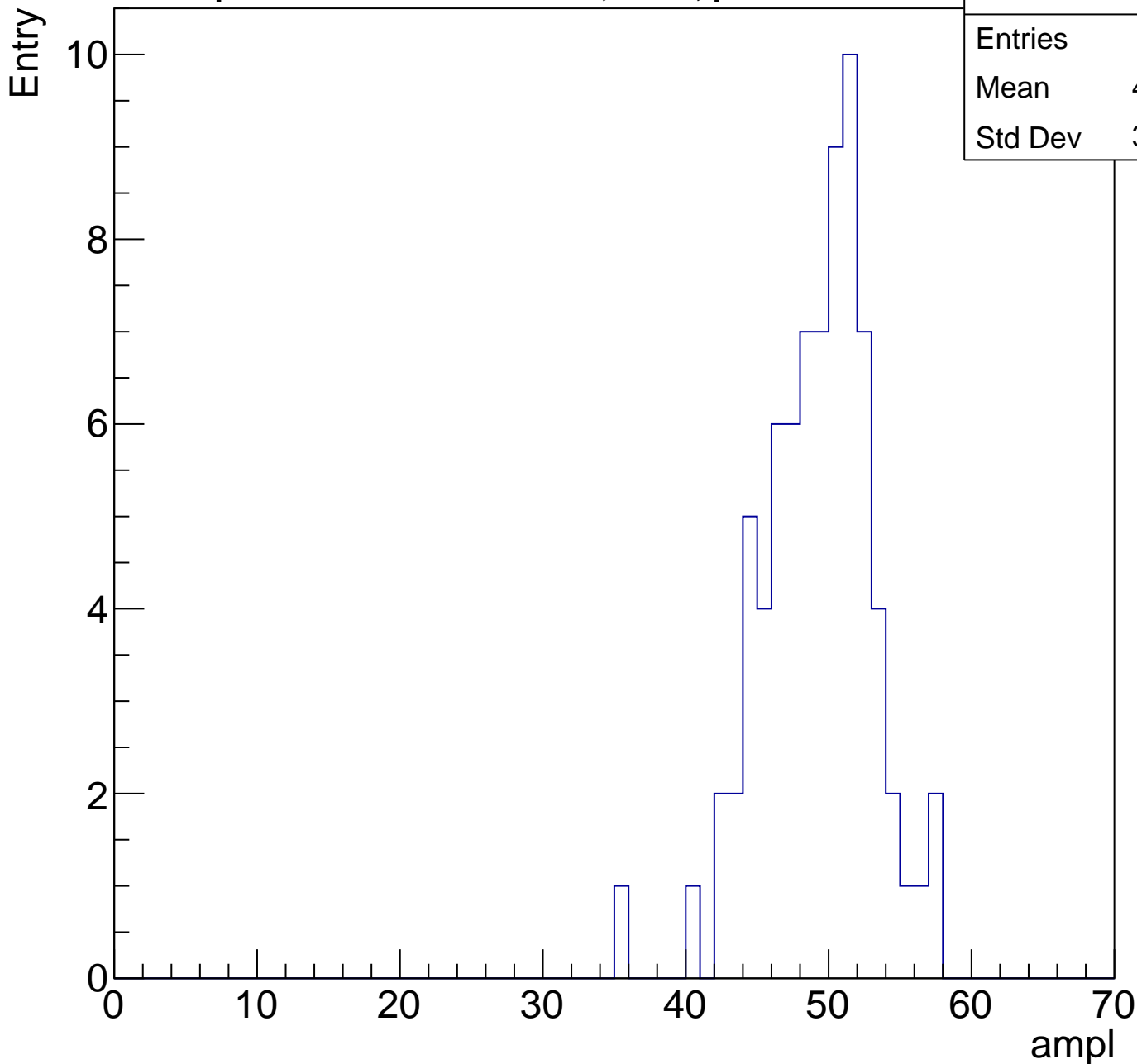
Entry



# B1L103S, U4-ch33, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 77    |
| Mean    | 48.71 |
| Std Dev | 3.871 |

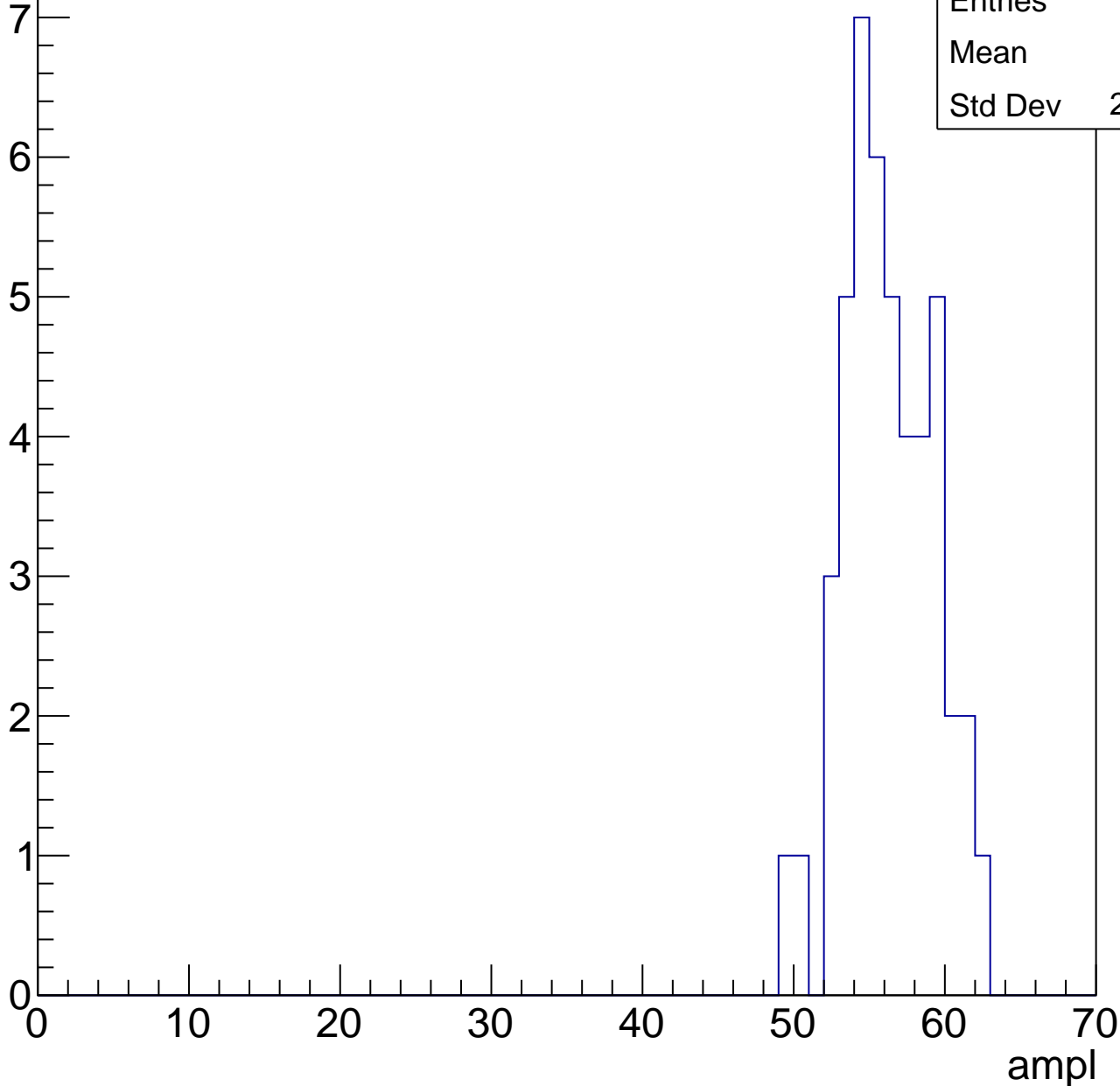


# B1L103S, U4-ch33, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 46    |
| Mean    | 55.8  |
| Std Dev | 2.924 |

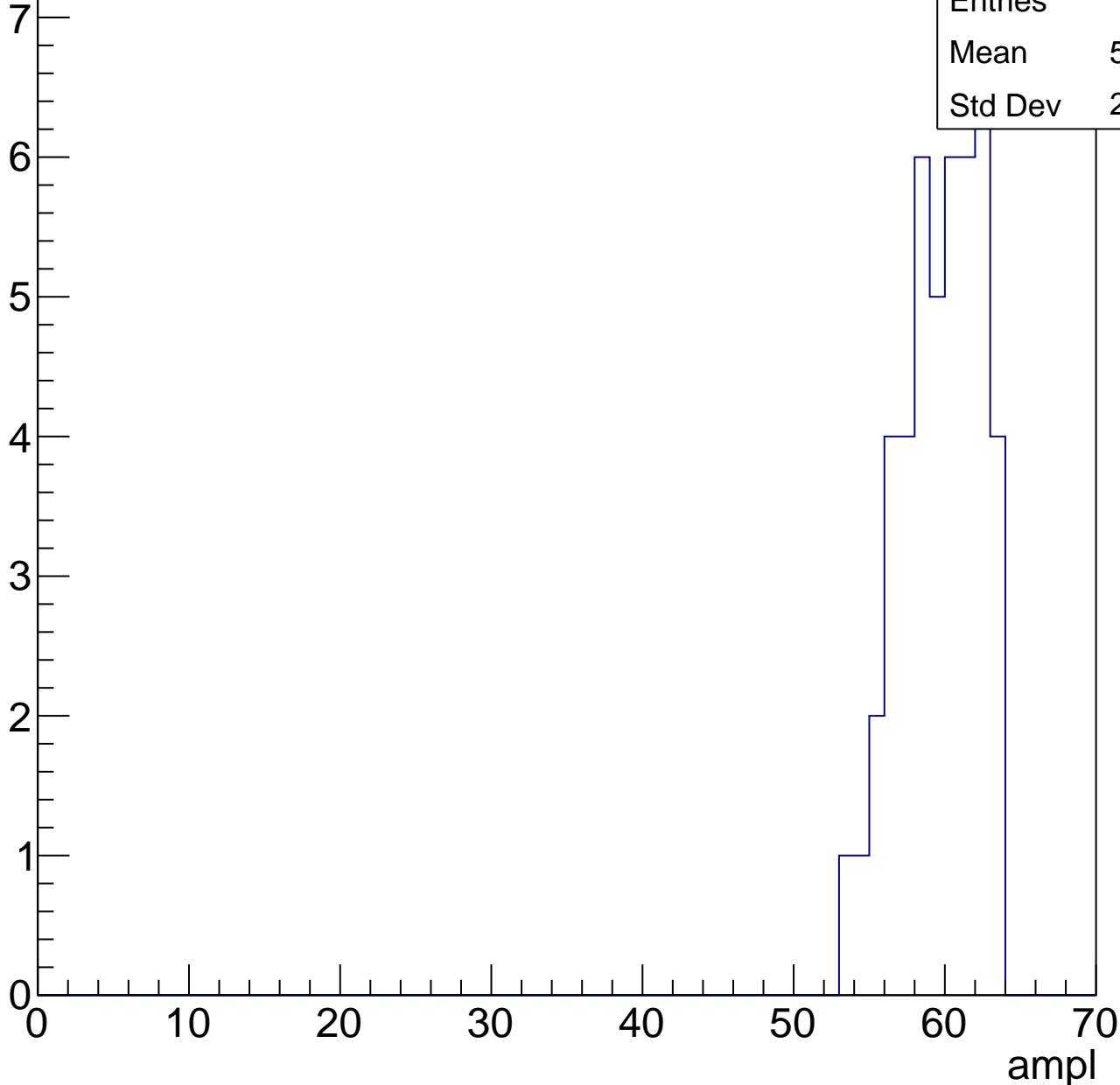


# B1L103S, U4-ch33, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 46    |
| Mean    | 59.22 |
| Std Dev | 2.578 |

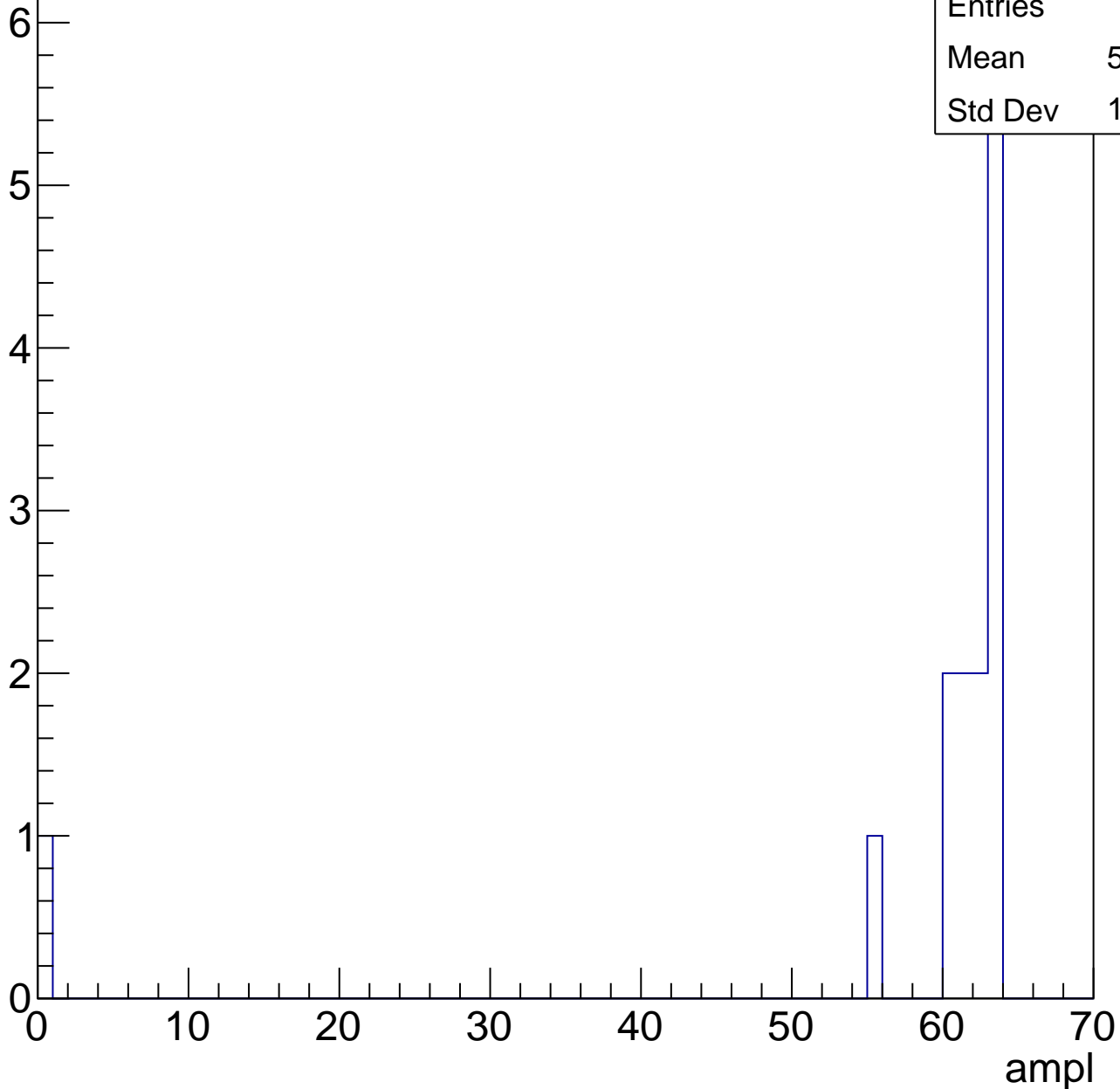


# B1L103S, U4-ch33, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 14    |
| Mean    | 57.07 |
| Std Dev | 15.97 |





# B1L103S, U4-ch33, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

|         |    |
|---------|----|
| Entries | 19 |
| Mean    | 0  |
| Std Dev | 0  |

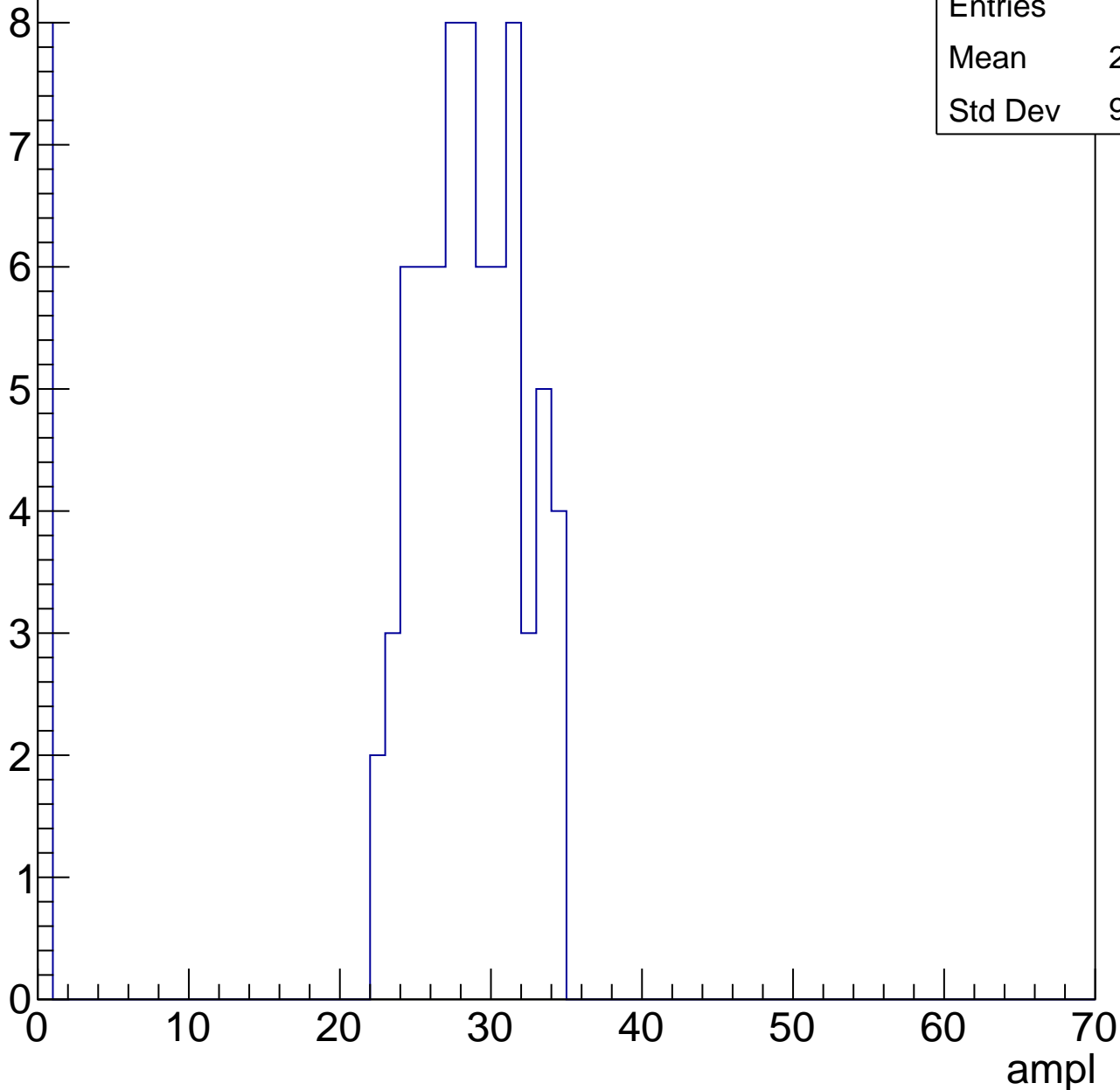
ampl

# B1L103S, U4-ch34, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 79    |
| Mean    | 25.34 |
| Std Dev | 9.044 |



# B1L103S, U4-ch34, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 60    |
| Mean    | 34.47 |
| Std Dev | 3.165 |

Entry

10

8

6

4

2

0

0

10

20

30

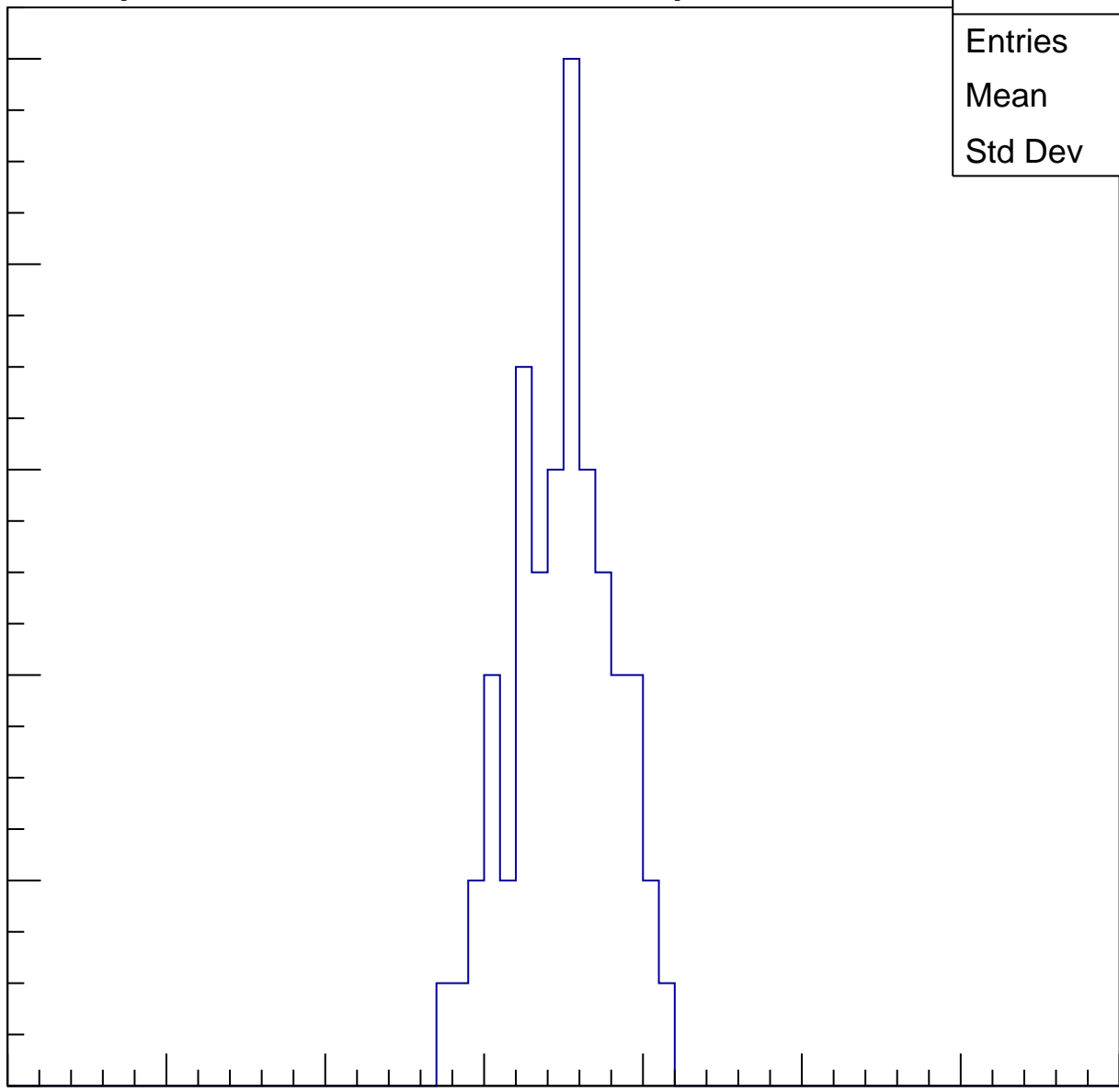
40

50

60

70

ampl

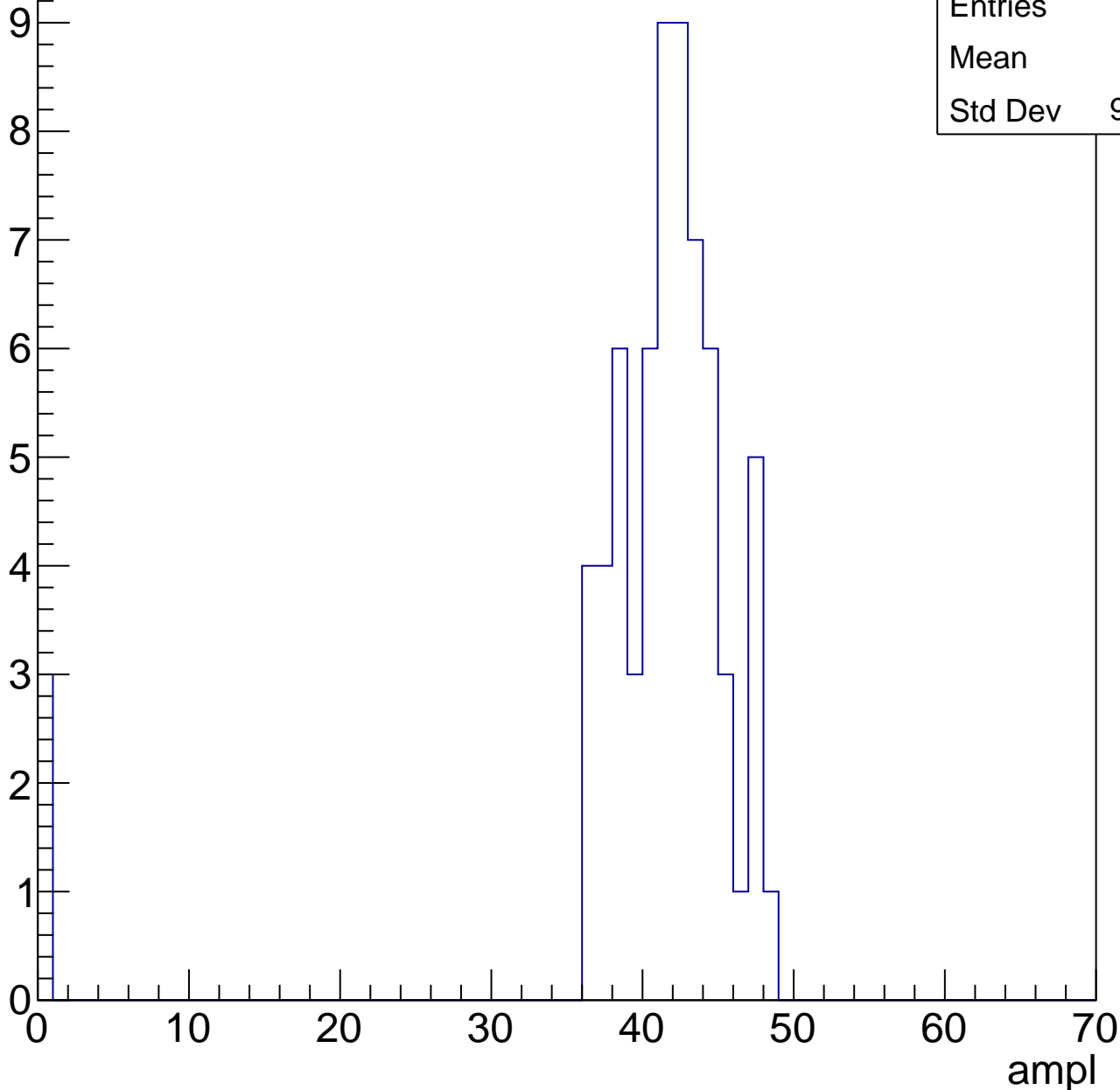


# B1L103S, U4-ch34, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 67    |
| Mean    | 39.6  |
| Std Dev | 9.093 |

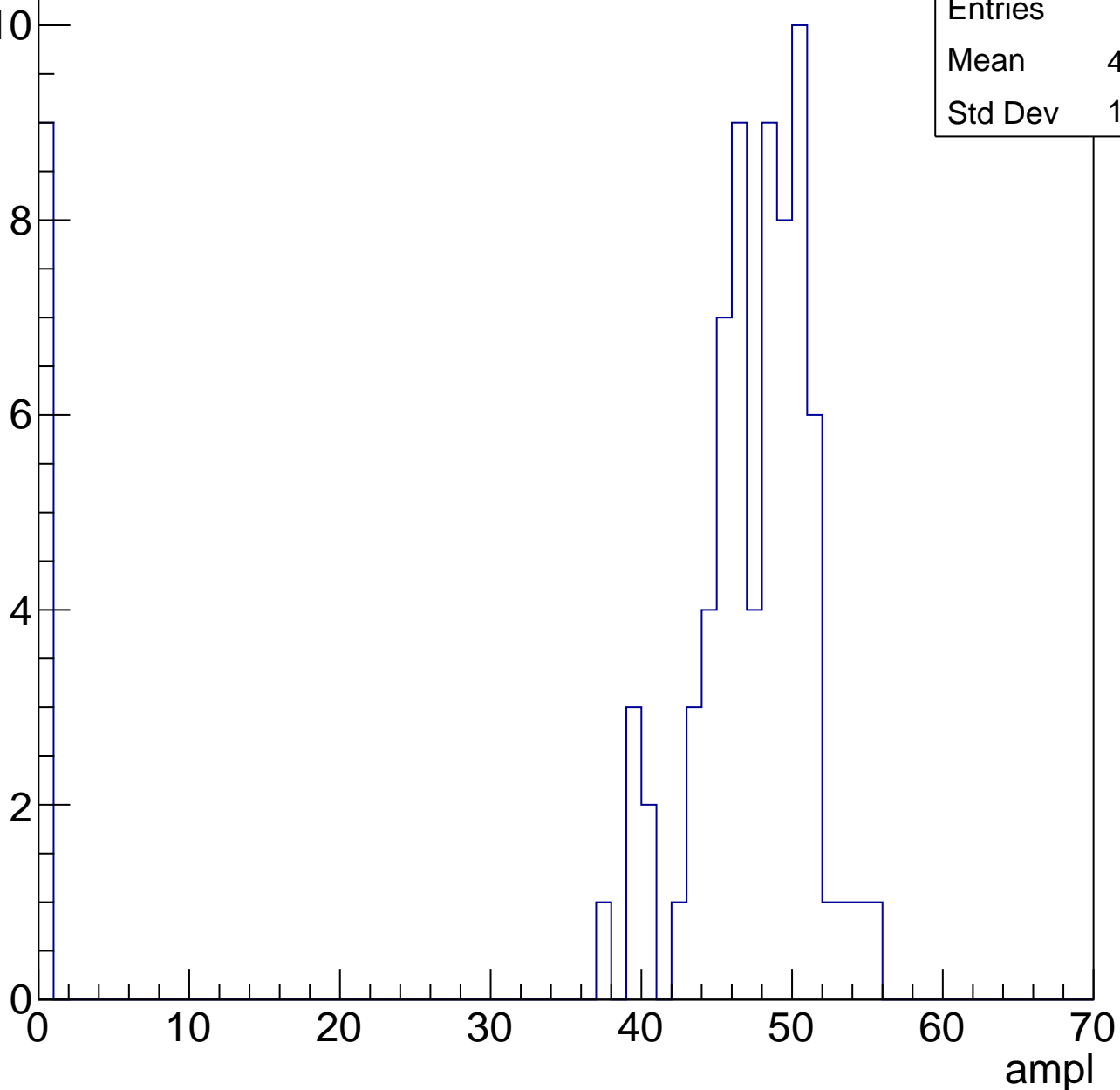


# B1L103S, U4-ch34, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 80    |
| Mean    | 41.77 |
| Std Dev | 15.26 |

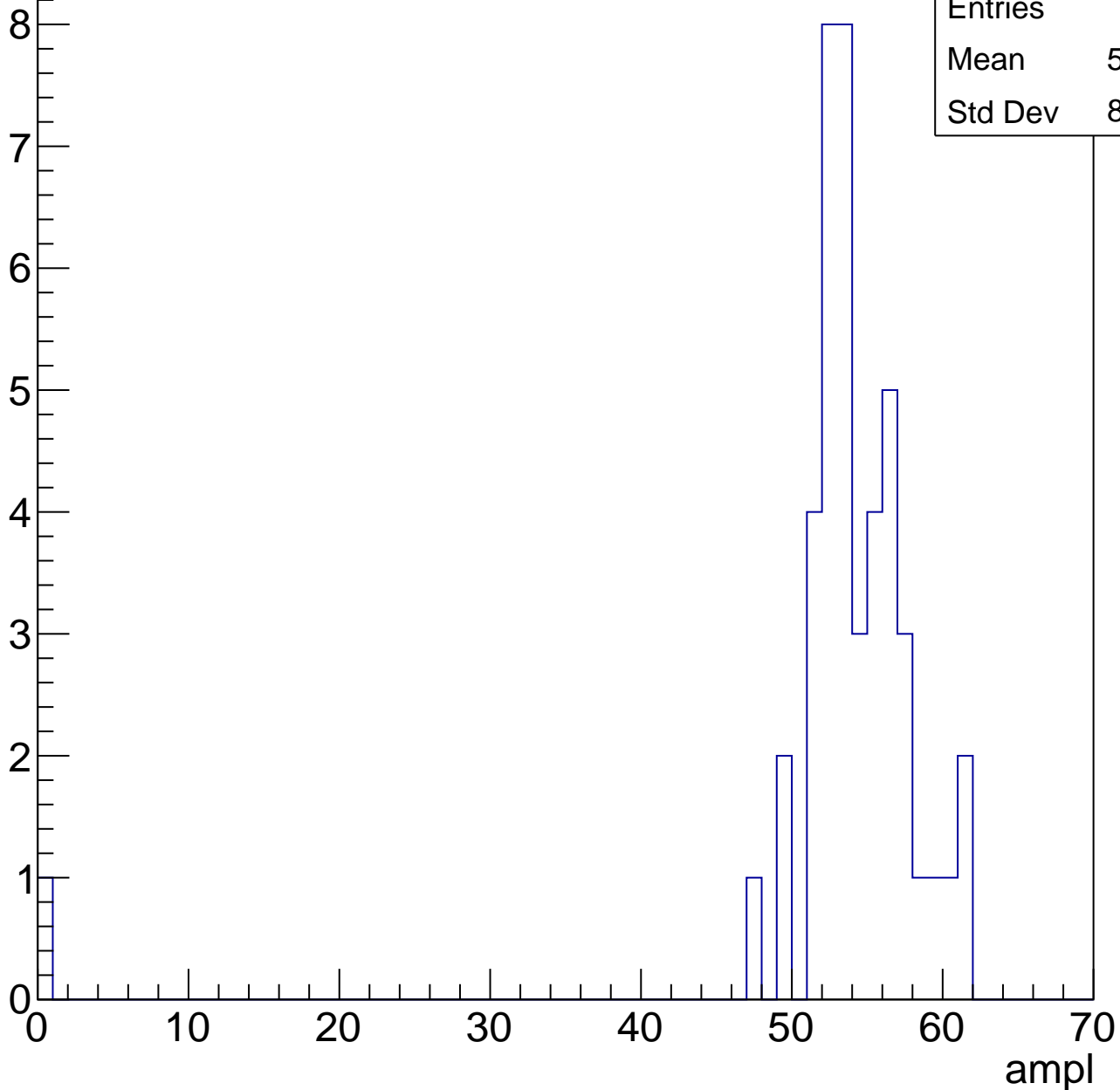


# B1L103S, U4-ch34, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

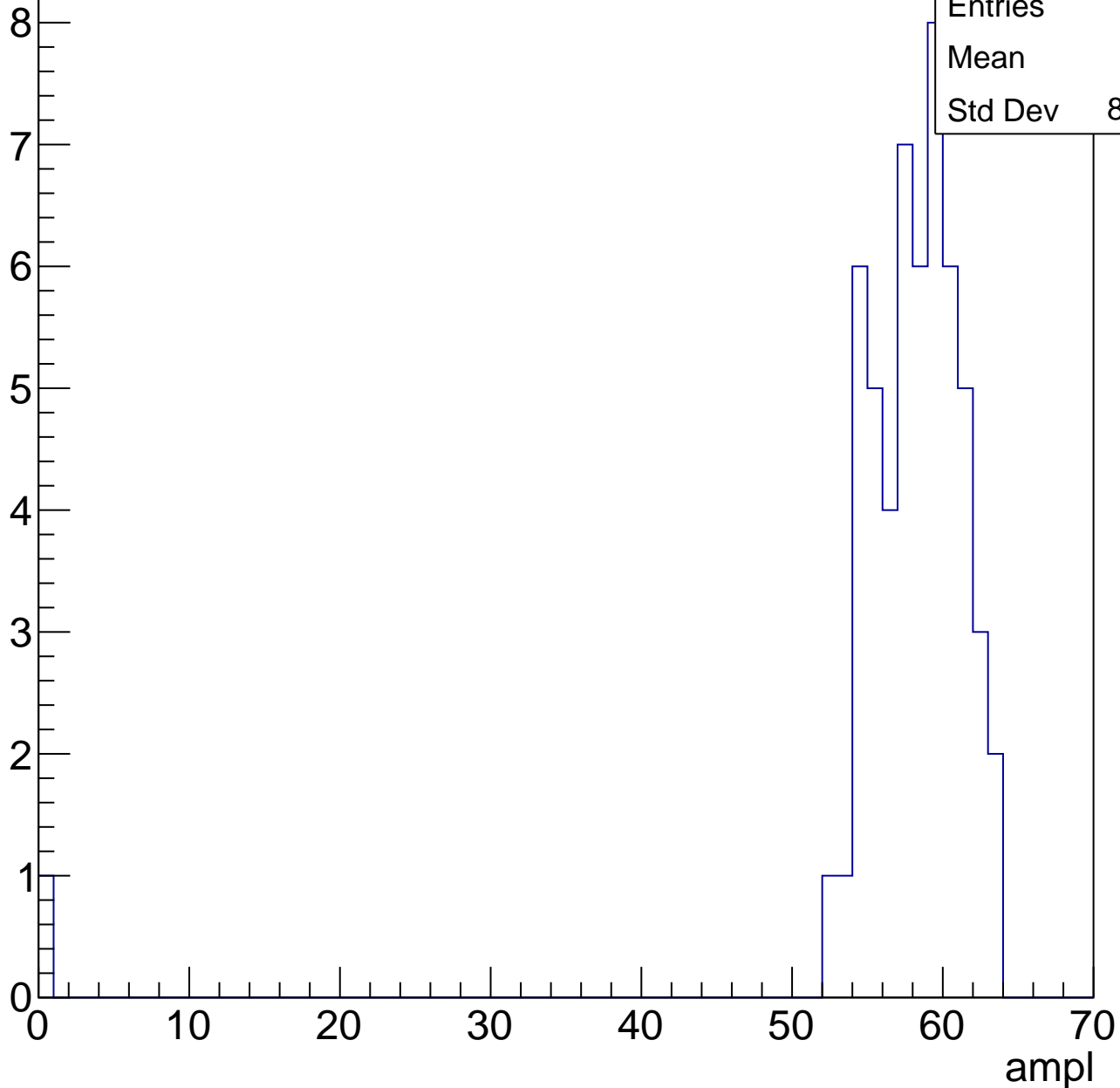
|         |       |
|---------|-------|
| Entries | 44    |
| Mean    | 52.75 |
| Std Dev | 8.592 |



# B1L103S, U4-ch34, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

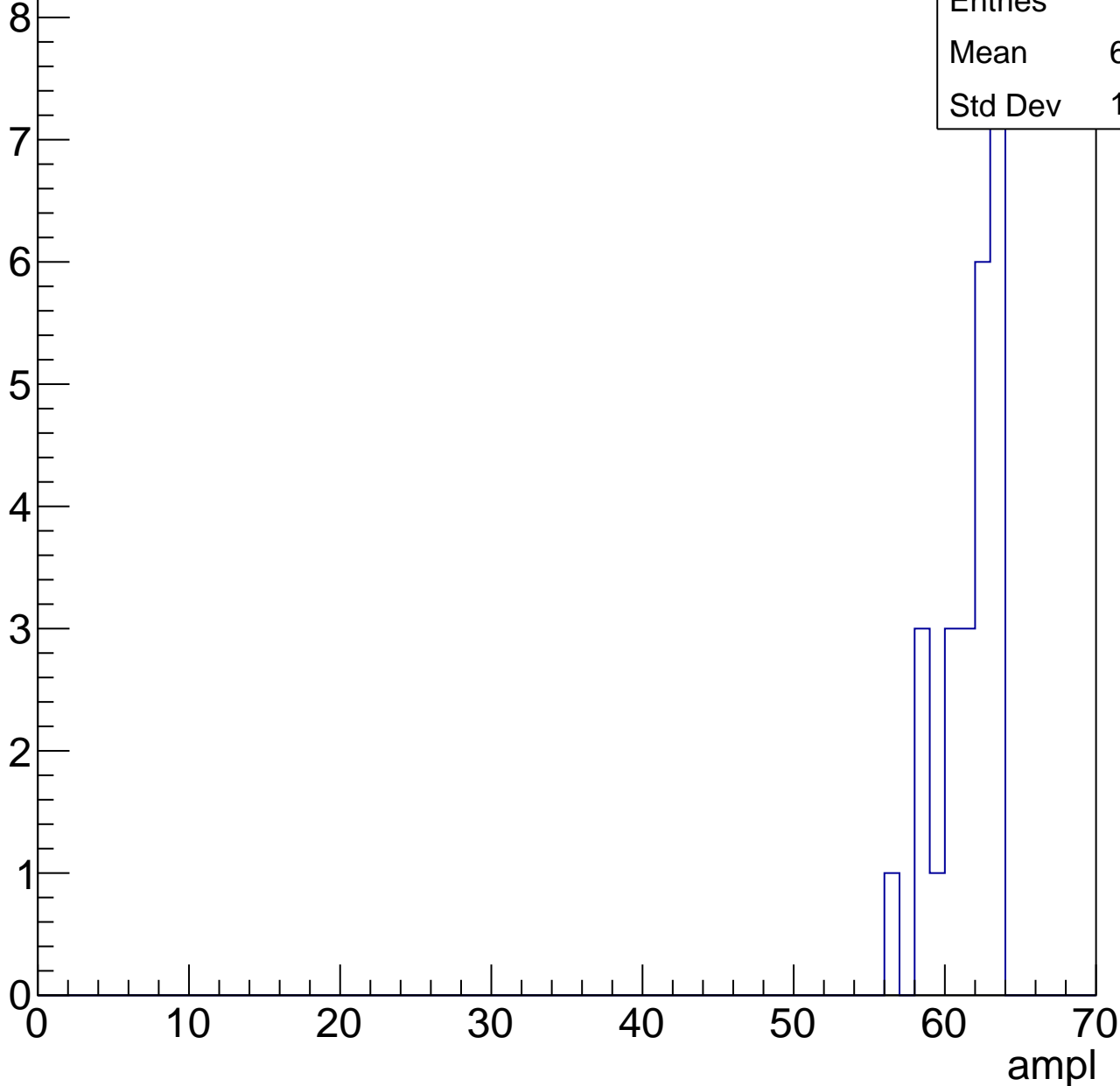


# B1L103S, U4-ch34, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 25    |
| Mean    | 61.12 |
| Std Dev | 1.966 |





# B1L103S, U4-ch34, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

|         |       |
|---------|-------|
| Entries | 19    |
| Mean    | 3.263 |
| Std Dev | 13.84 |

ampl

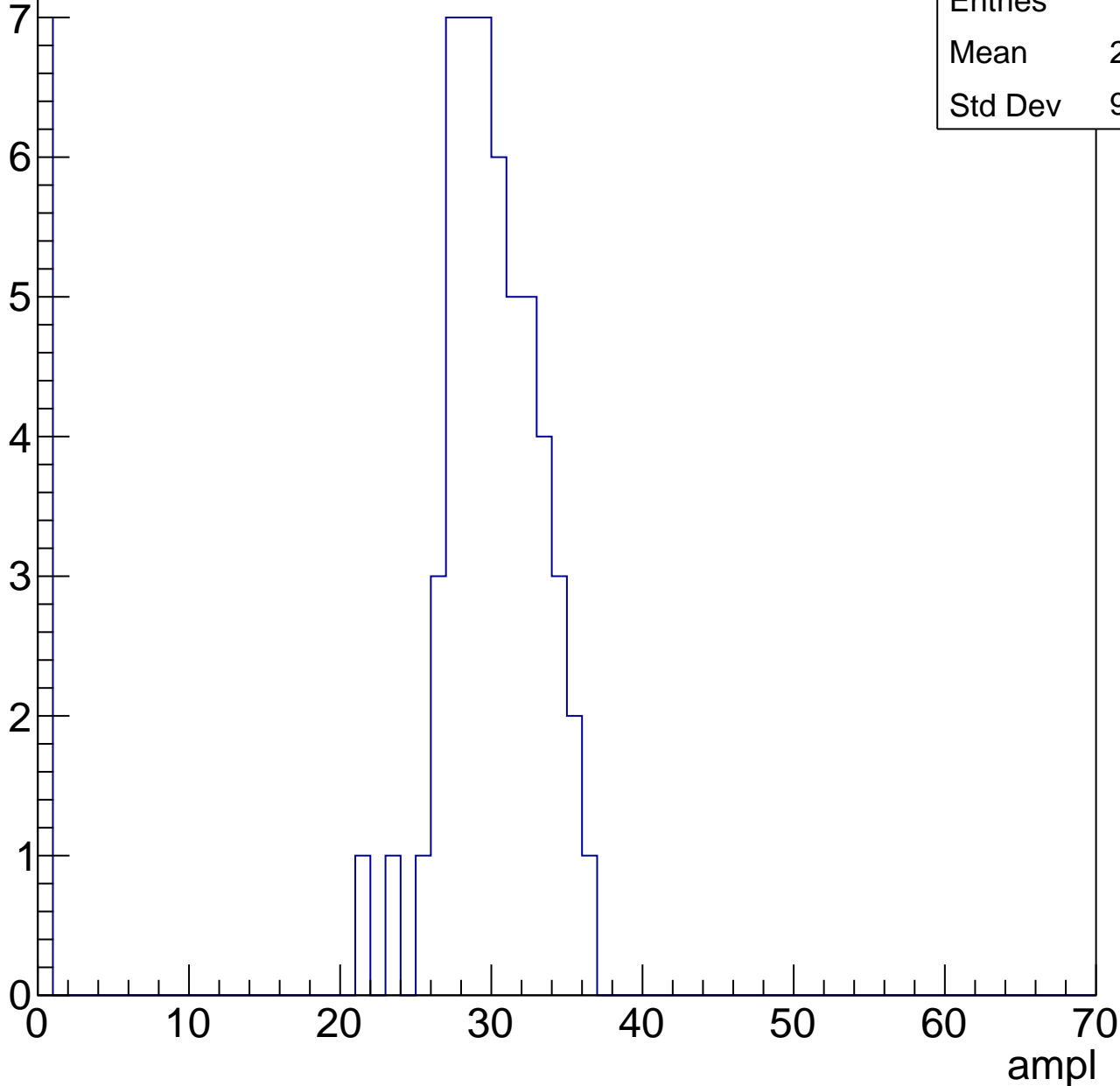
0 10 20 30 40 50 60 70

# B1L103S, U4-ch35, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 60    |
| Mean    | 26.17 |
| Std Dev | 9.928 |

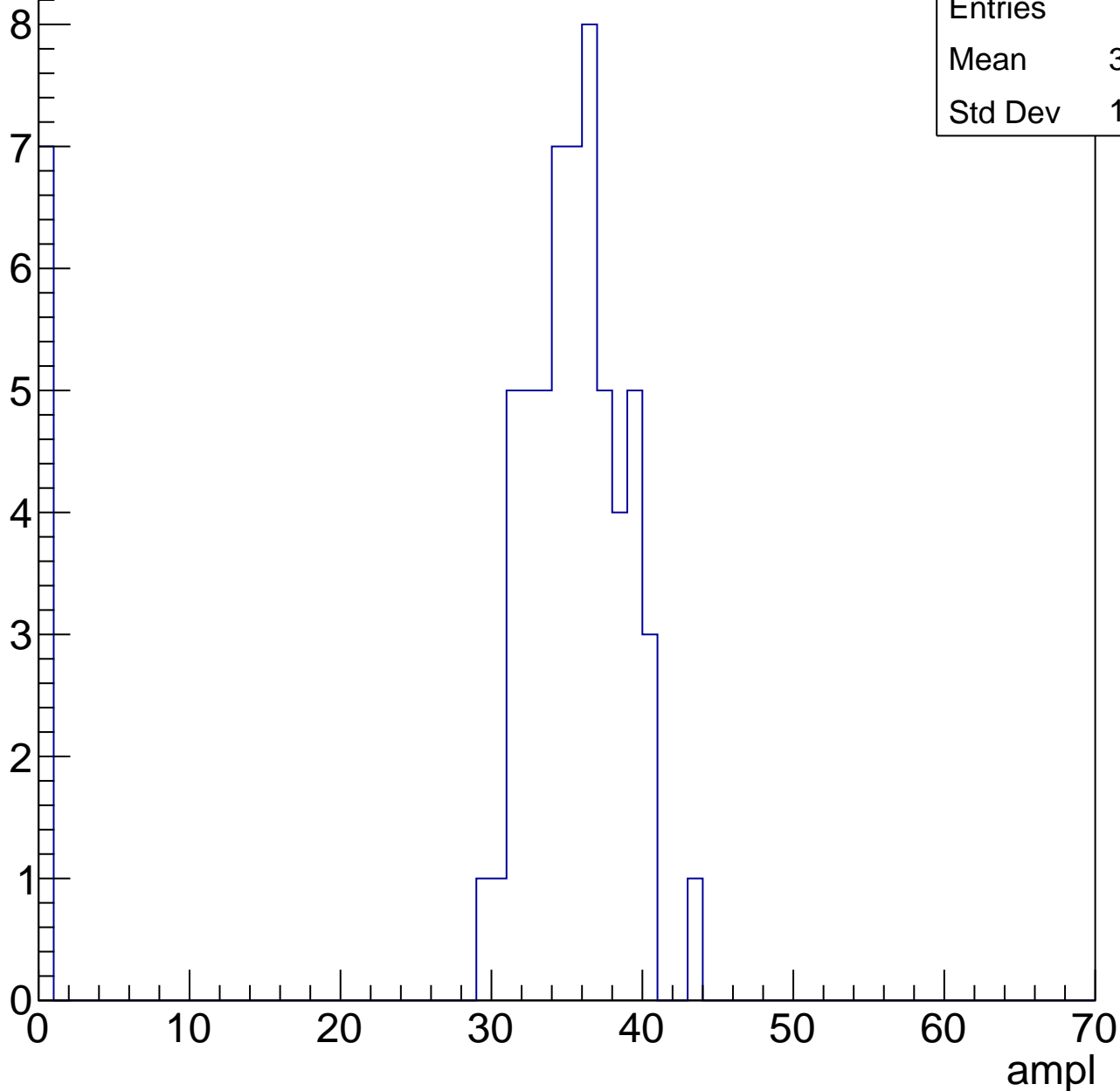


# B1L103S, U4-ch35, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 64    |
| Mean    | 31.33 |
| Std Dev | 11.32 |

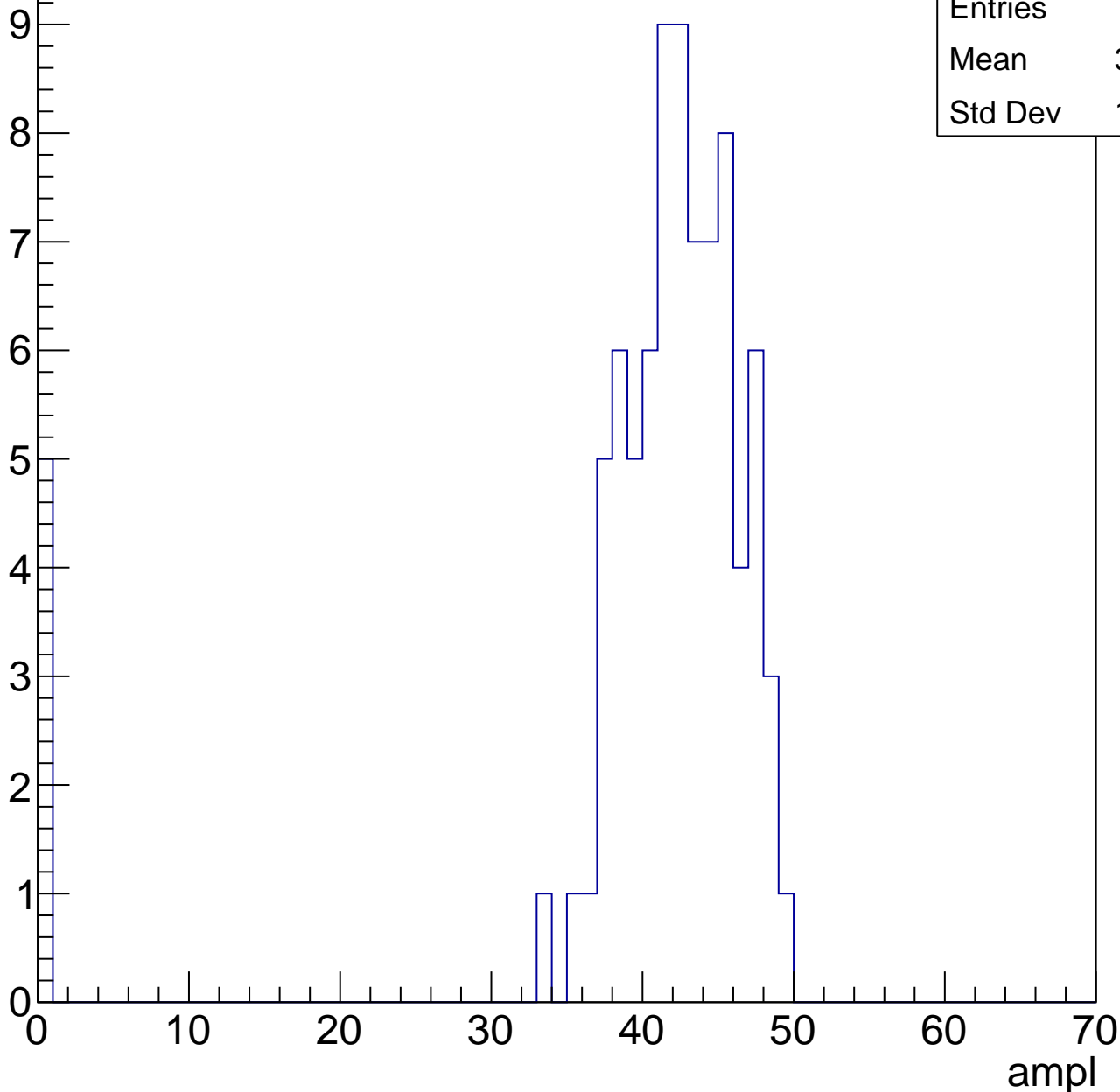


# B1L103S, U4-ch35, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

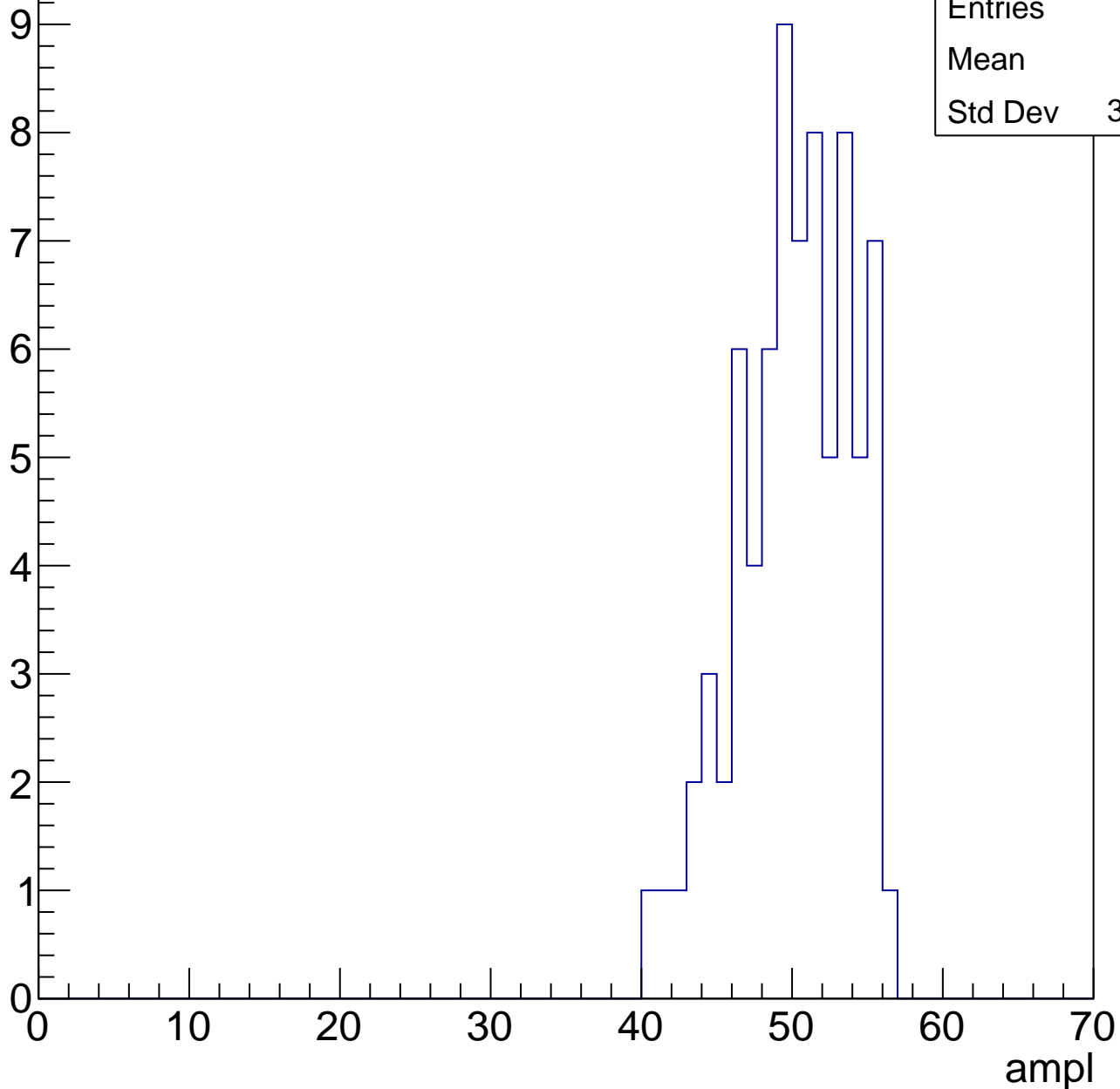
|         |       |
|---------|-------|
| Entries | 84    |
| Mean    | 39.61 |
| Std Dev | 10.51 |



# B1L103S, U4-ch35, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

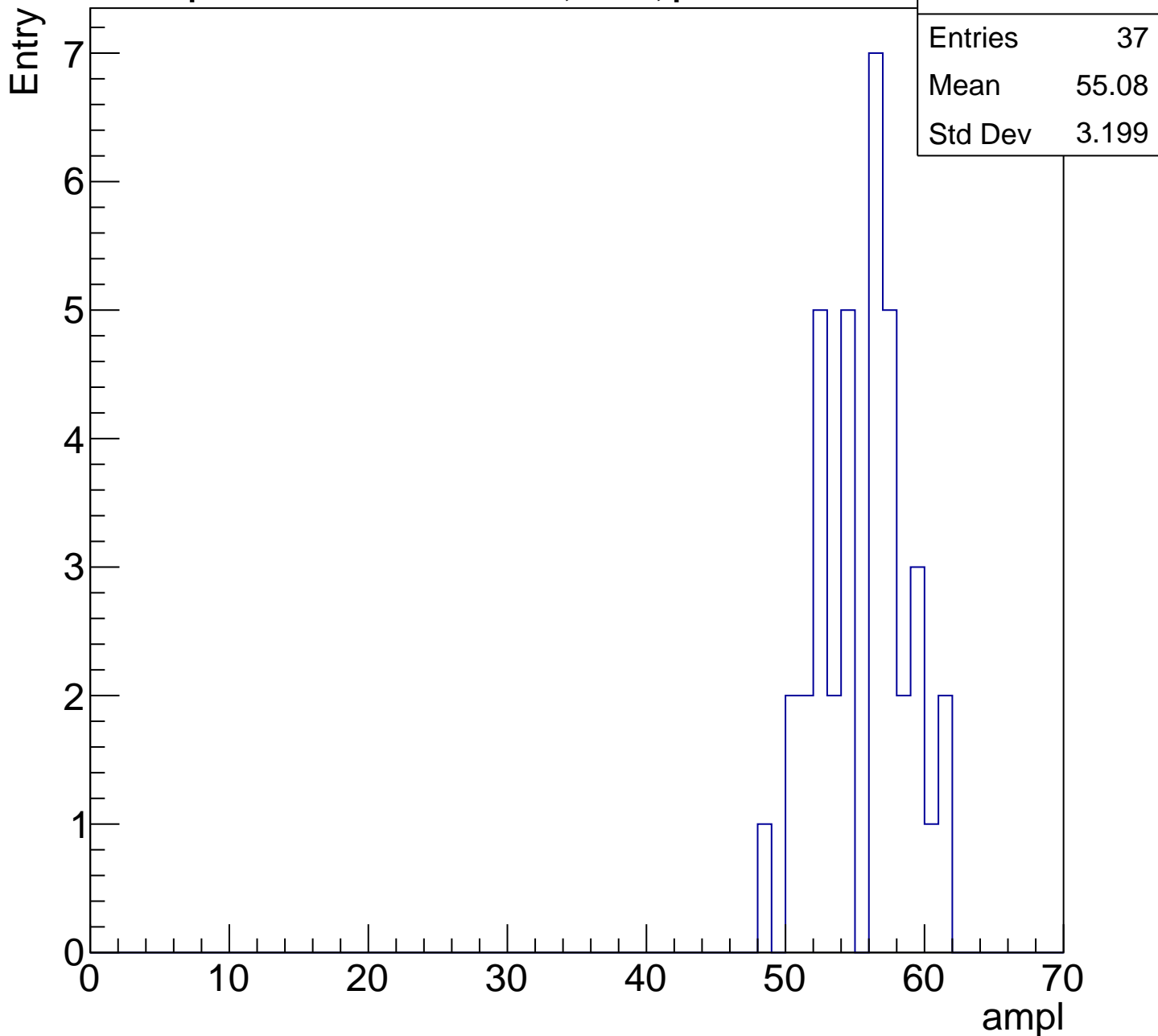
Entry



|         |       |
|---------|-------|
| Entries | 76    |
| Mean    | 49.7  |
| Std Dev | 3.717 |

# B1L103S, U4-ch35, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2



# B1L103S, U4-ch35, adc5

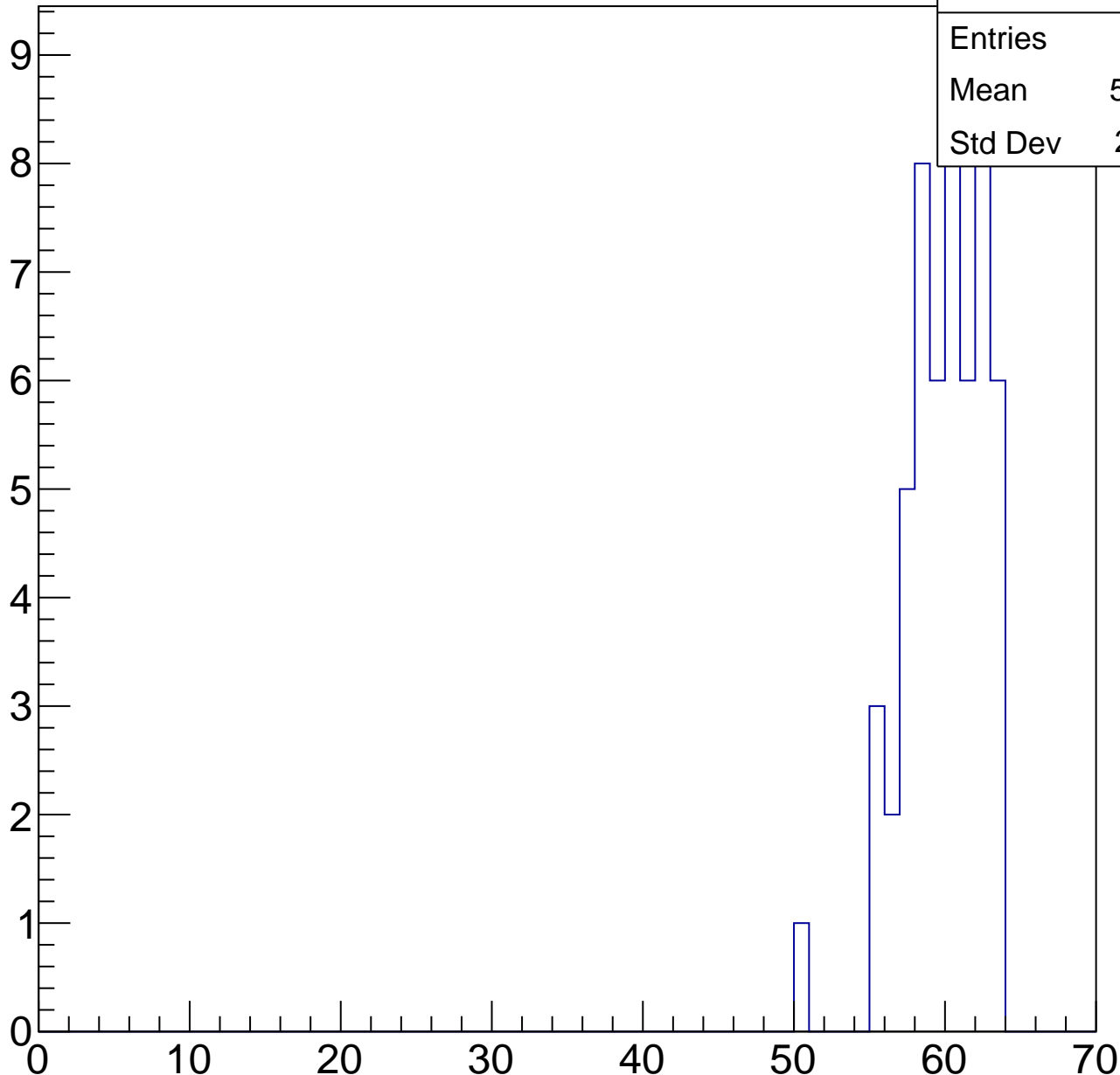
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

|         |       |
|---------|-------|
| Entries | 54    |
| Mean    | 59.44 |
| Std Dev | 2.601 |

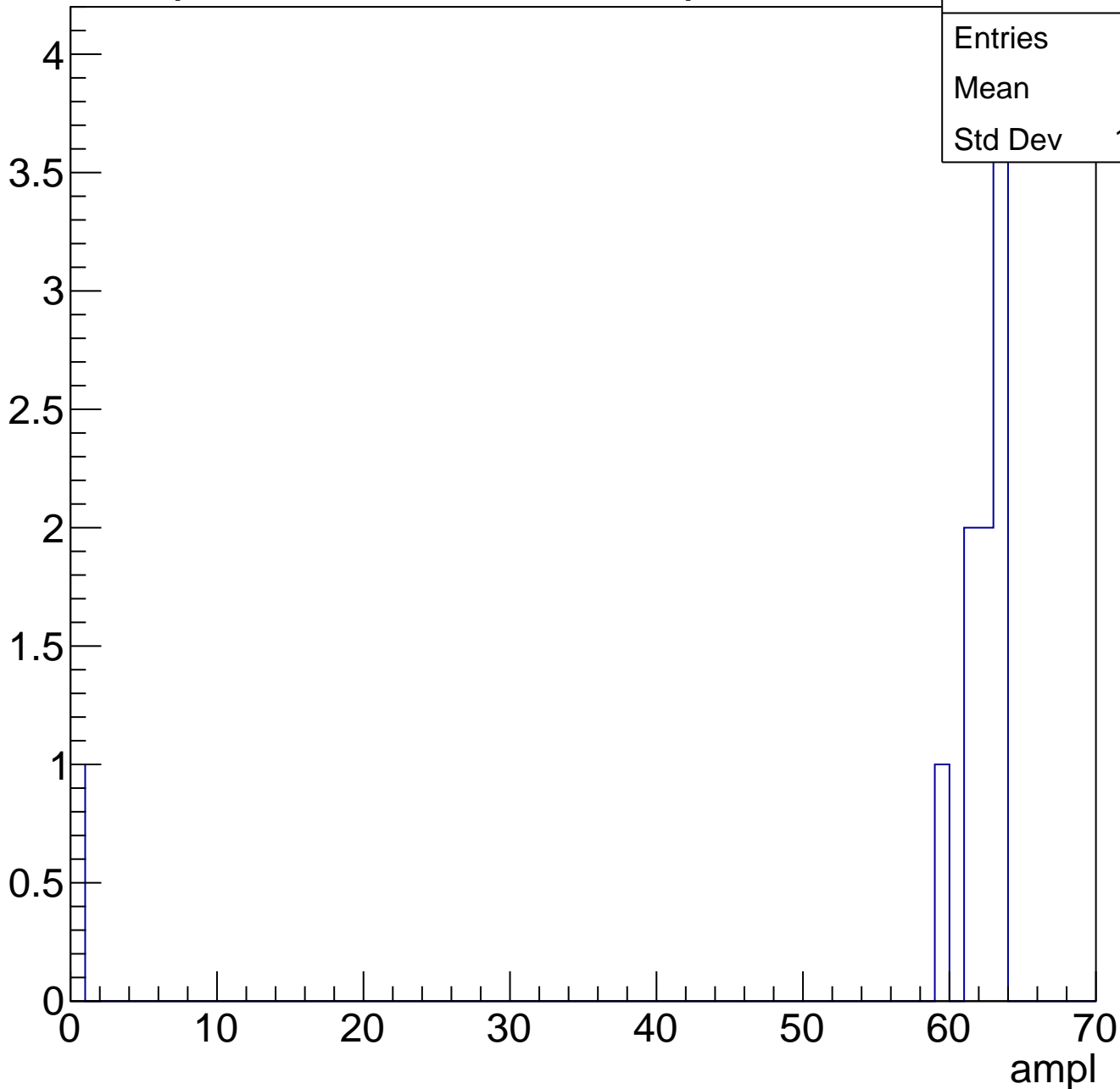
ampl



# B1L103S, U4-ch35, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U4-ch35, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

|         |    |
|---------|----|
| Entries | 19 |
| Mean    | 0  |
| Std Dev | 0  |

ampl

# B1L103S, U4-ch36, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 83    |
| Mean    | 24.72 |
| Std Dev | 11.1  |

Entry

12

10

8

6

4

2

0

0

10

20

30

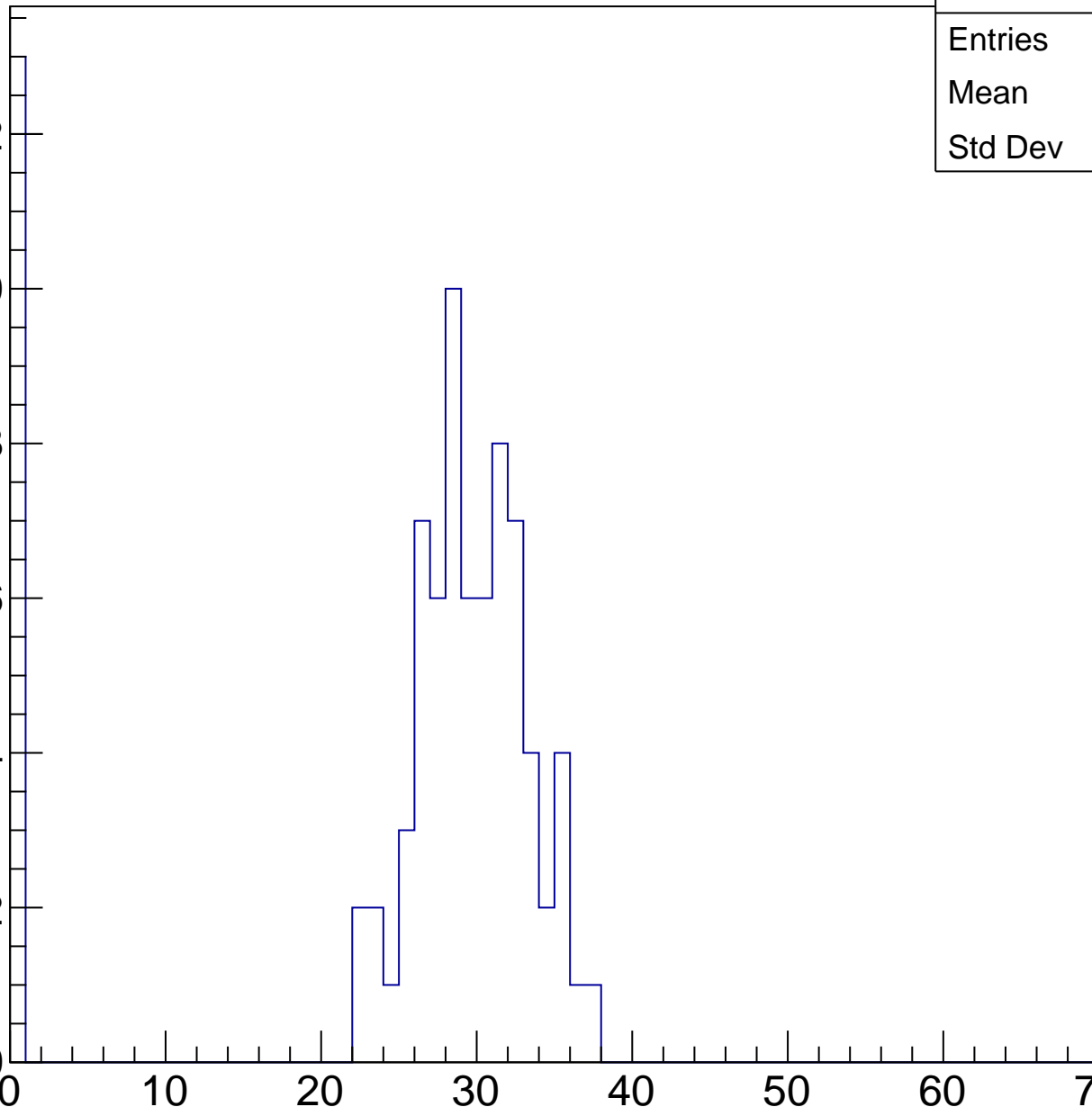
40

50

60

70

ampl

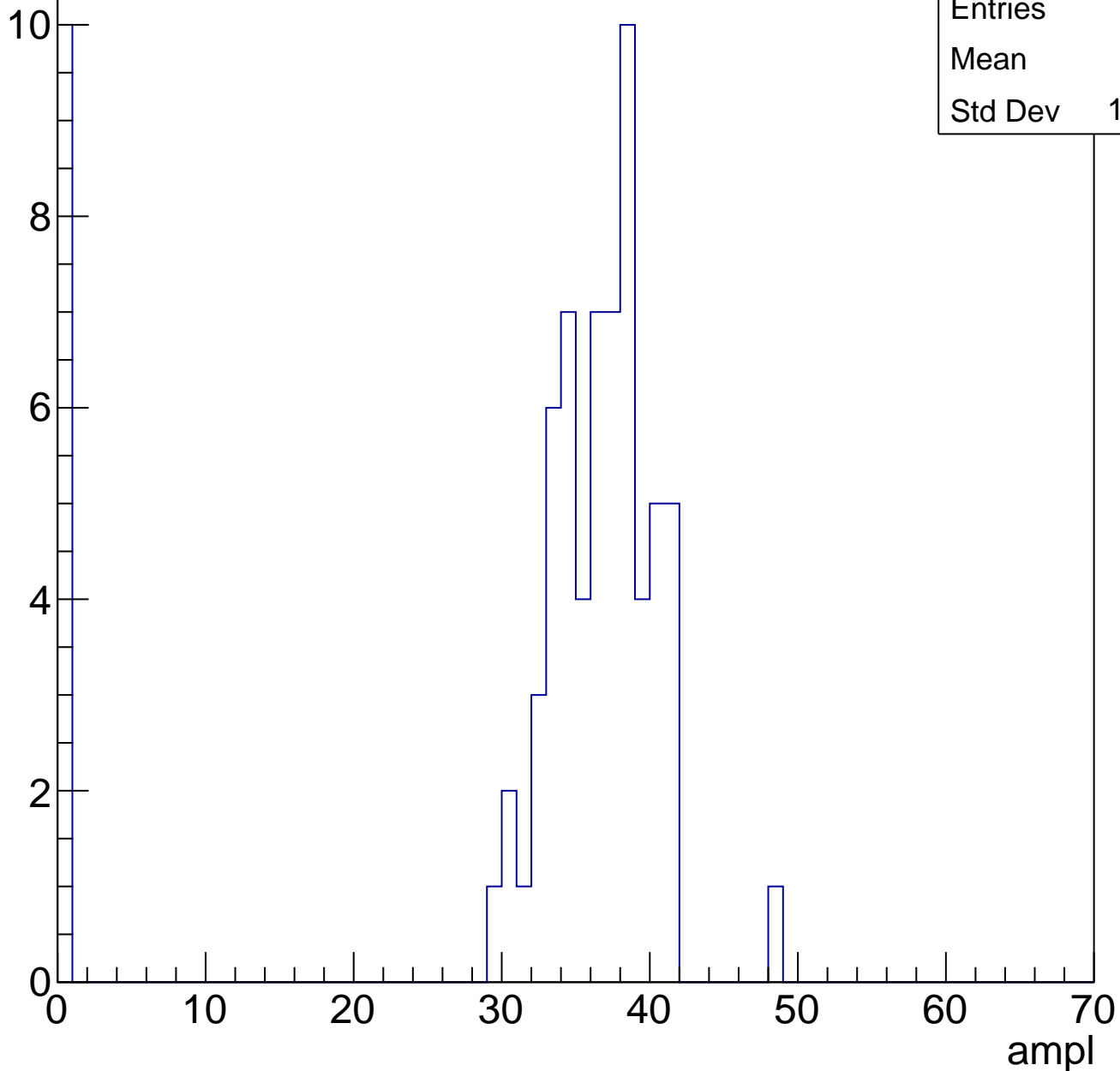


# B1L103S, U4-ch36, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 73    |
| Mean    | 31.4  |
| Std Dev | 12.89 |

Entry

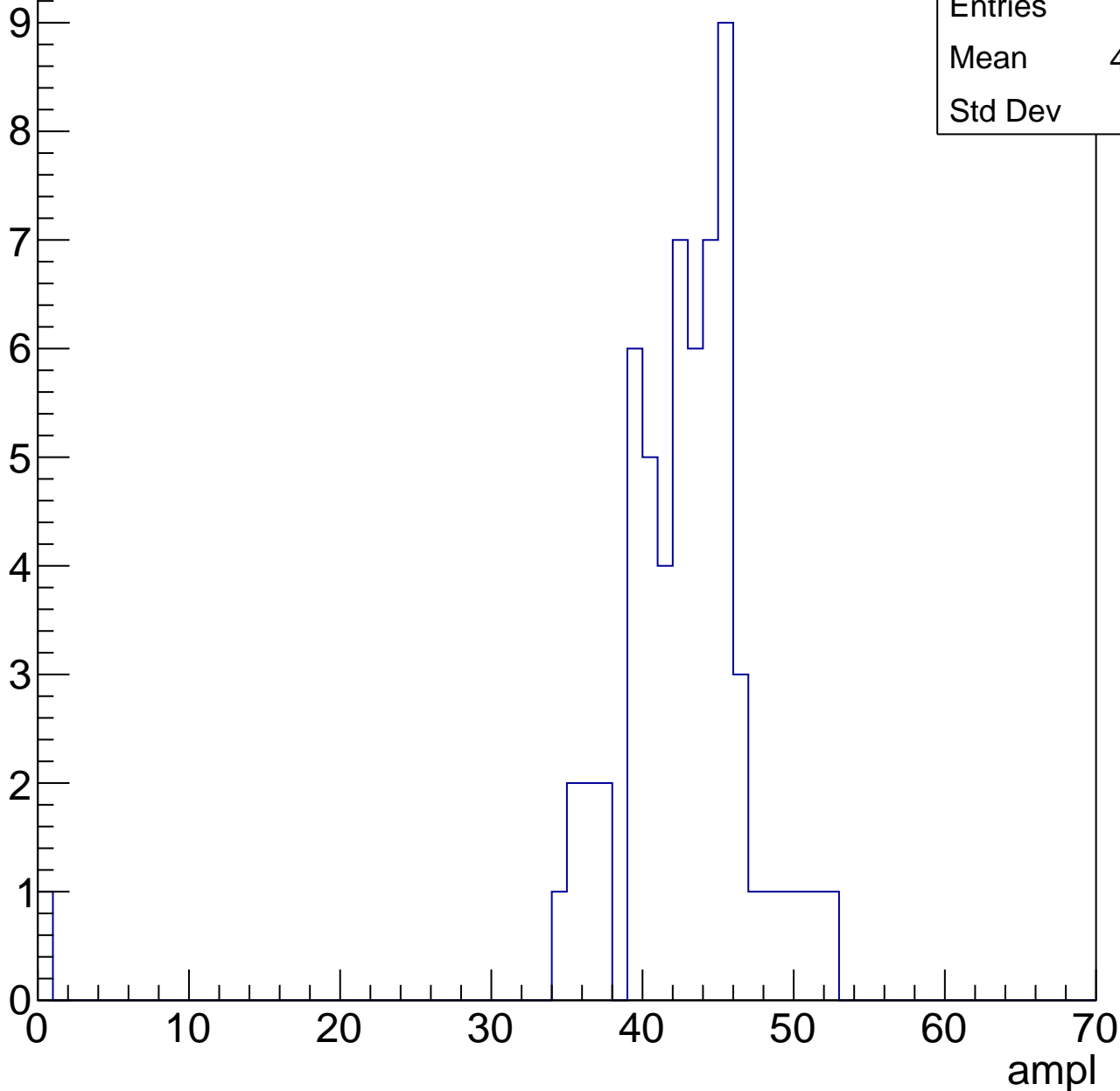


# B1L103S, U4-ch36, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 61    |
| Mean    | 41.77 |
| Std Dev | 6.58  |

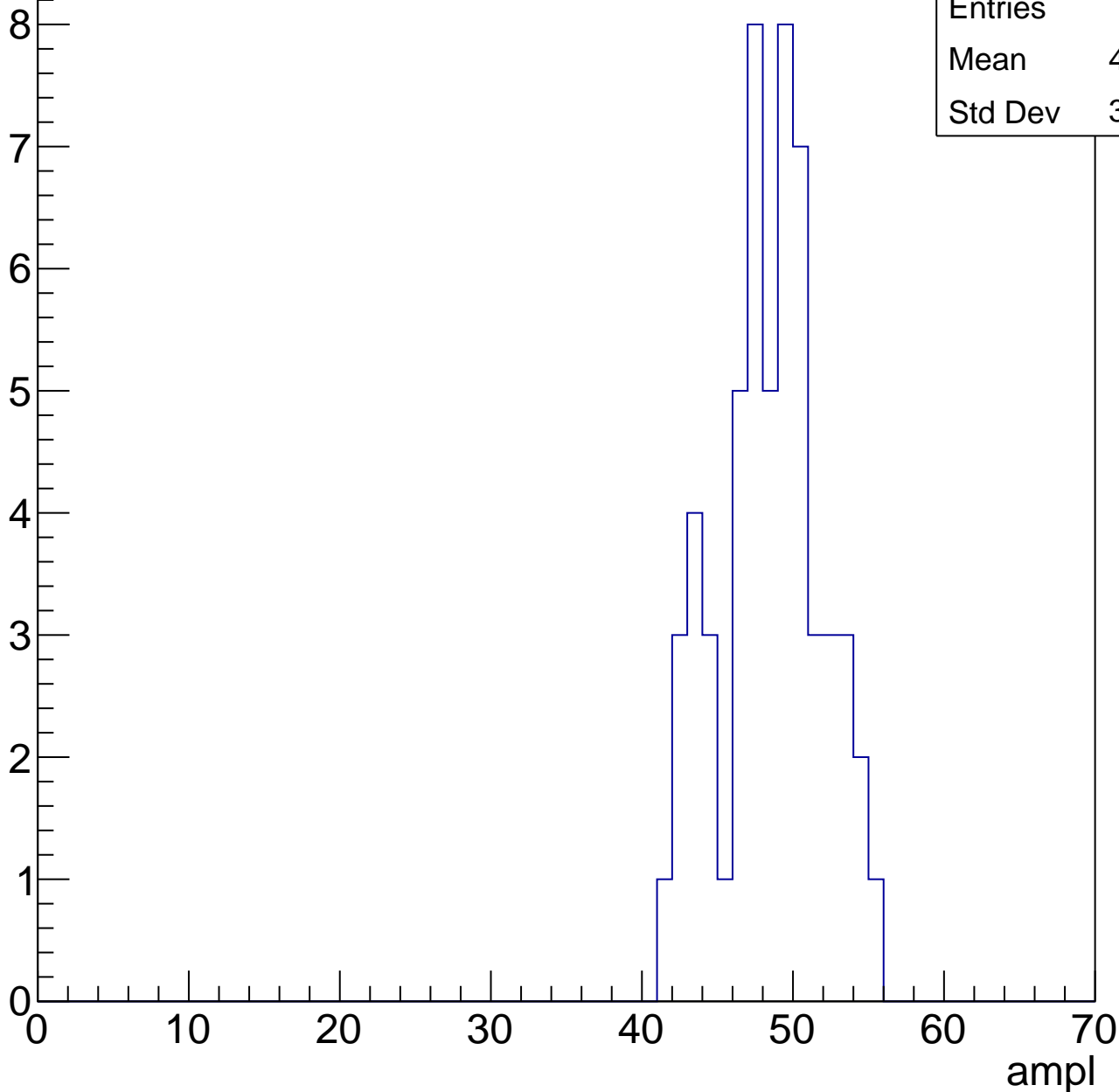


# B1L103S, U4-ch36, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 57    |
| Mean    | 47.98 |
| Std Dev | 3.374 |

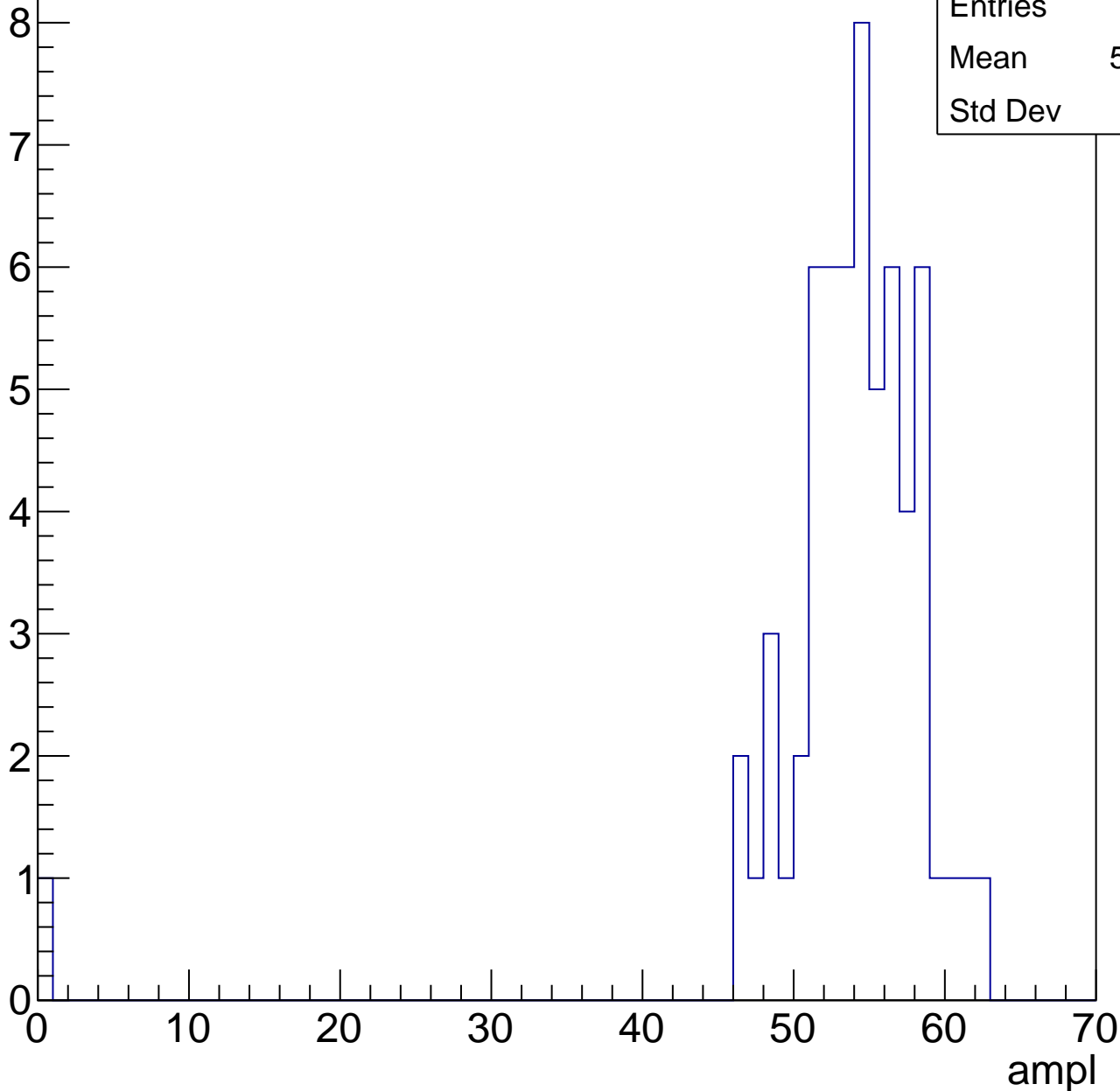


# B1L103S, U4-ch36, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 61    |
| Mean    | 52.93 |
| Std Dev | 7.69  |

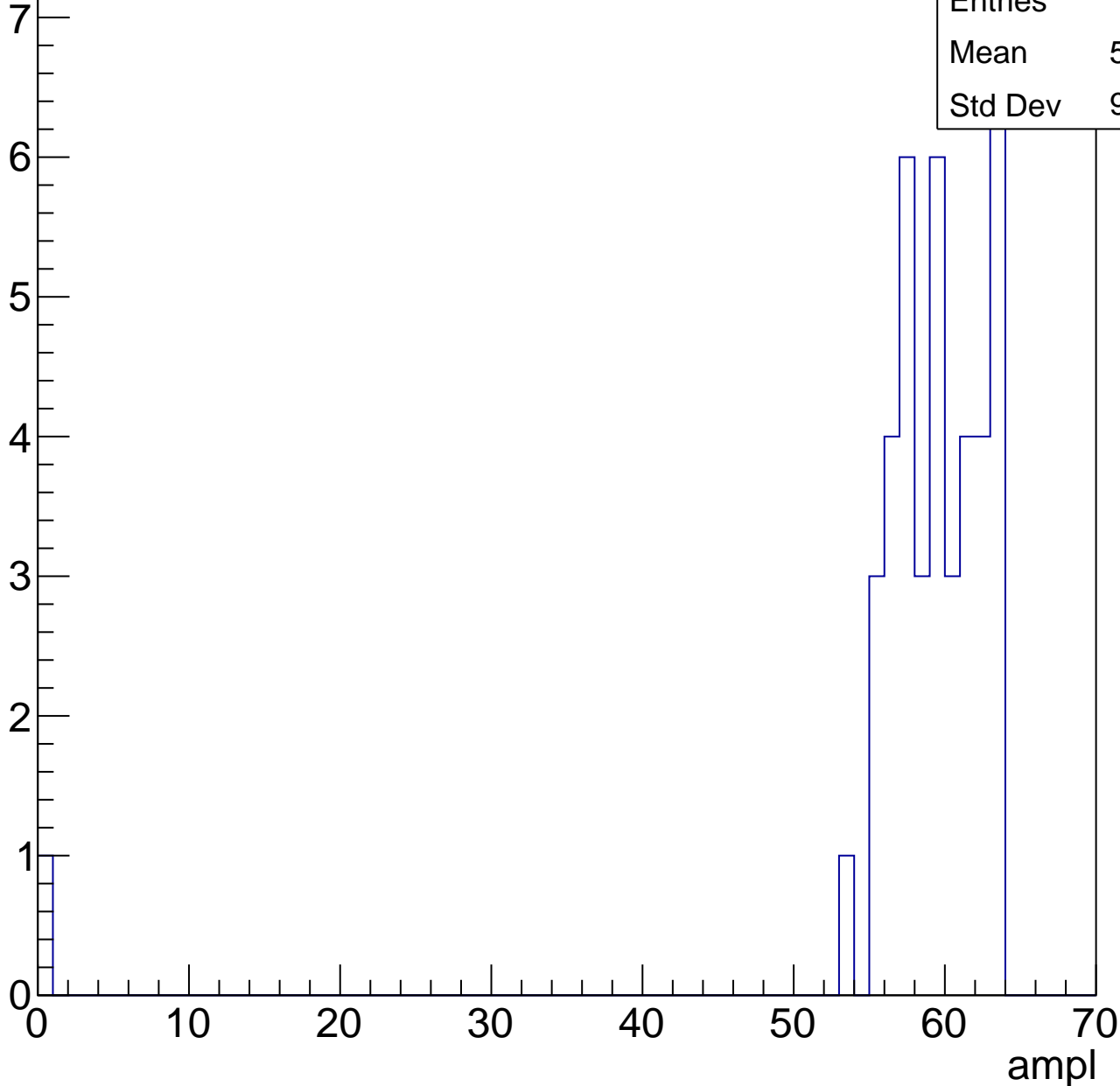


# B1L103S, U4-ch36, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 42    |
| Mean    | 57.74 |
| Std Dev | 9.422 |

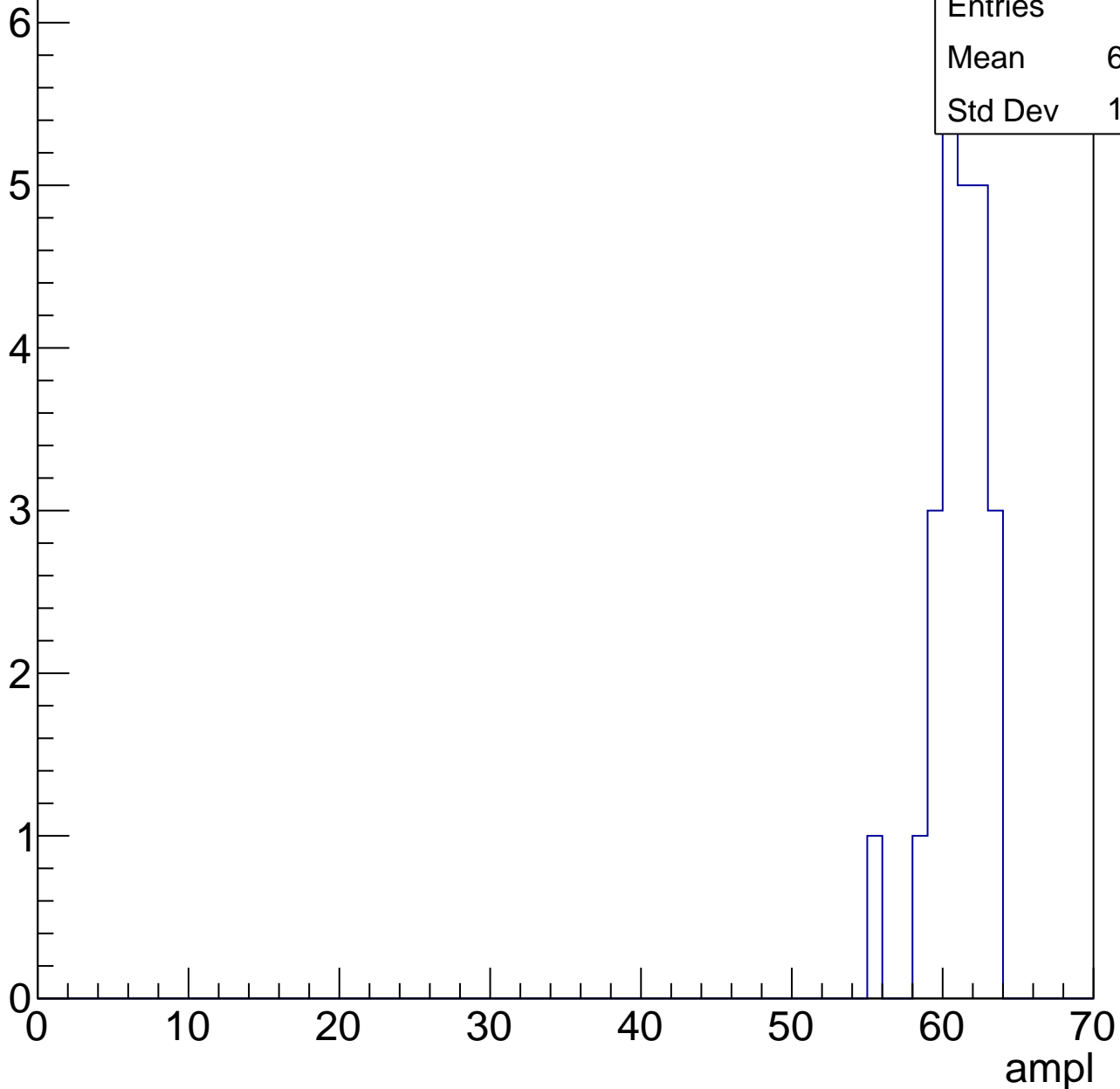


# B1L103S, U4-ch36, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 24    |
| Mean    | 60.58 |
| Std Dev | 1.778 |





# B1L103S, U4-ch36, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

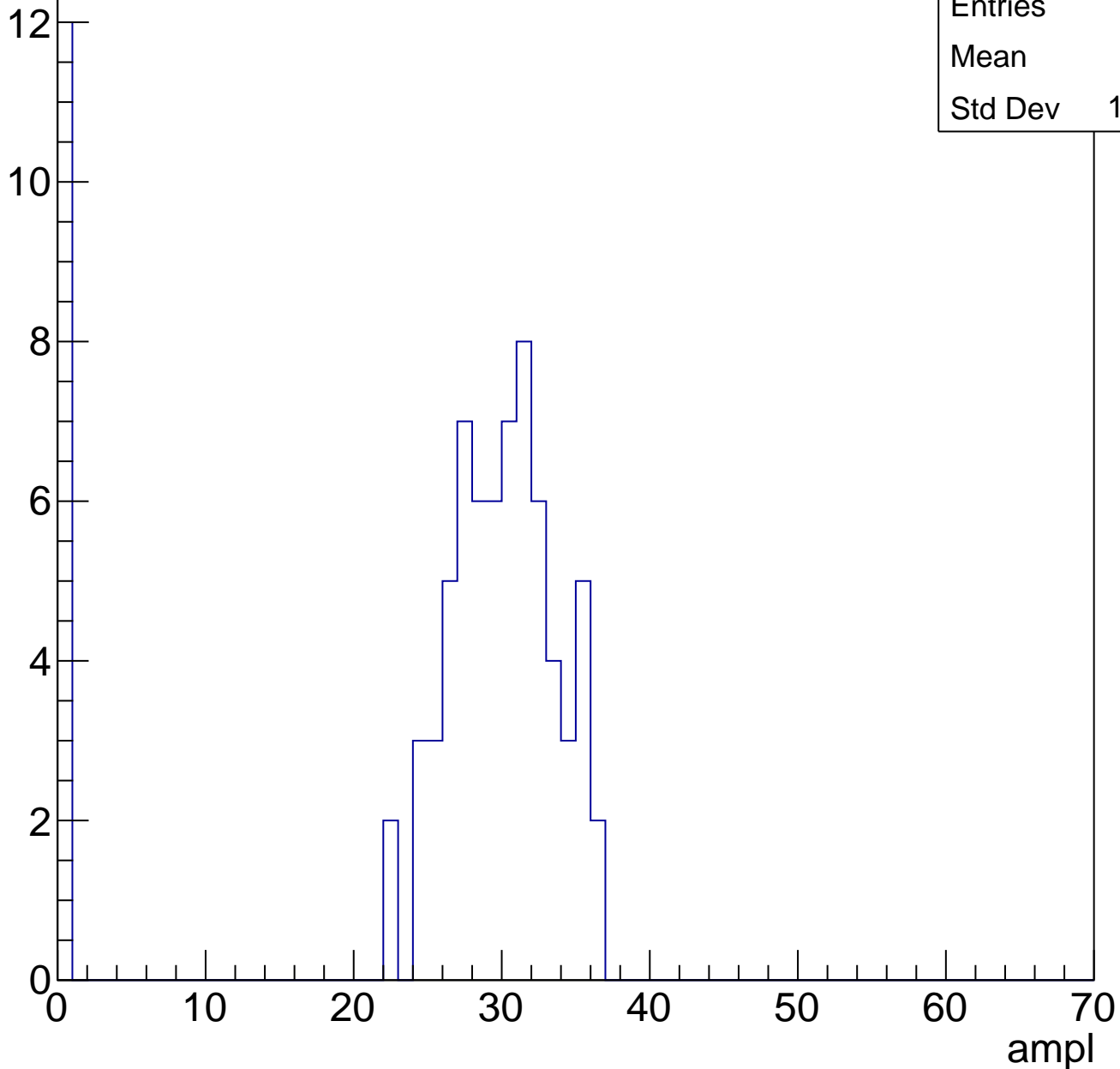


# B1L103S, U4-ch37, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 79    |
| Mean    | 25.1  |
| Std Dev | 11.08 |

Entry

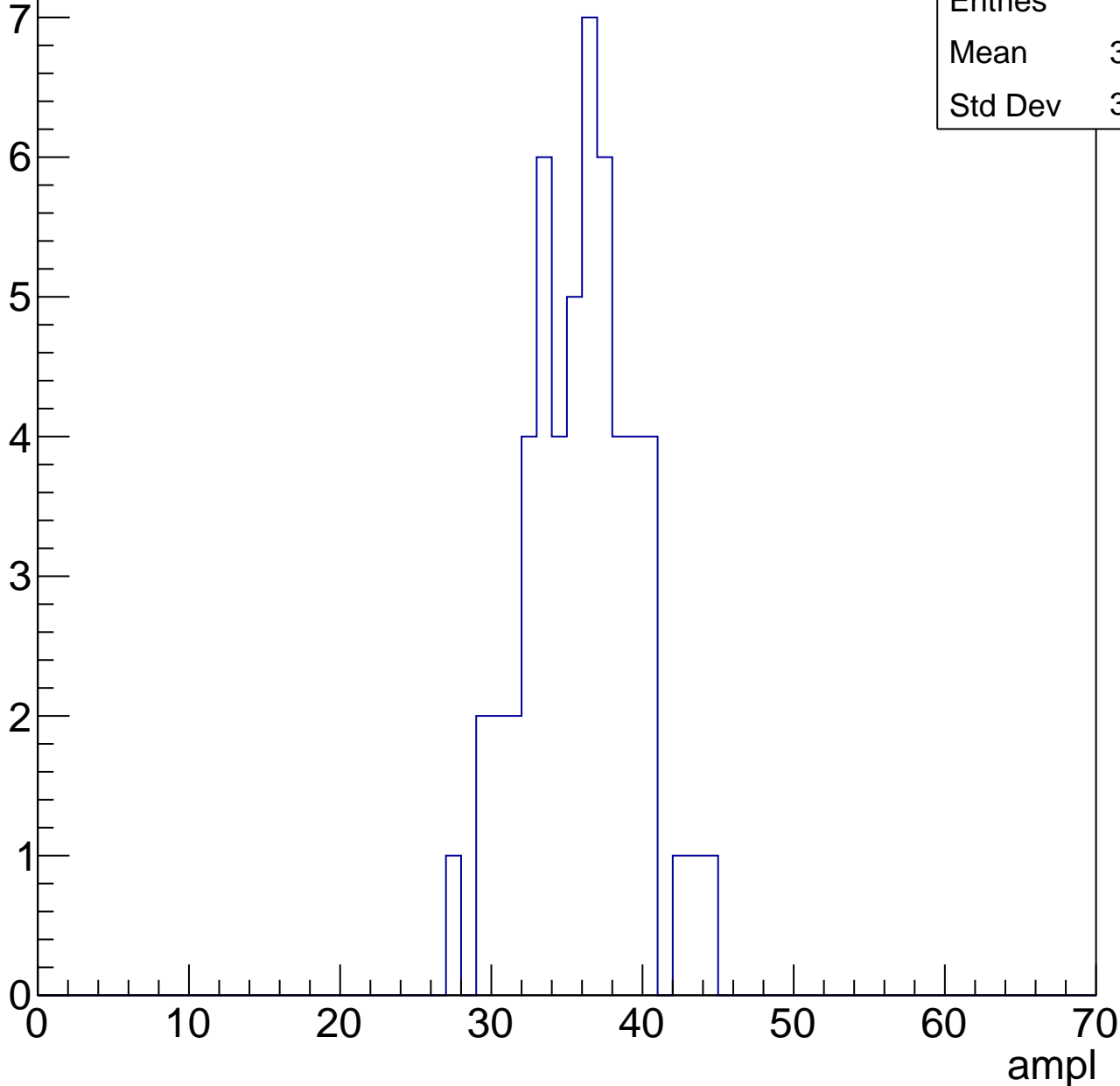


# B1L103S, U4-ch37, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

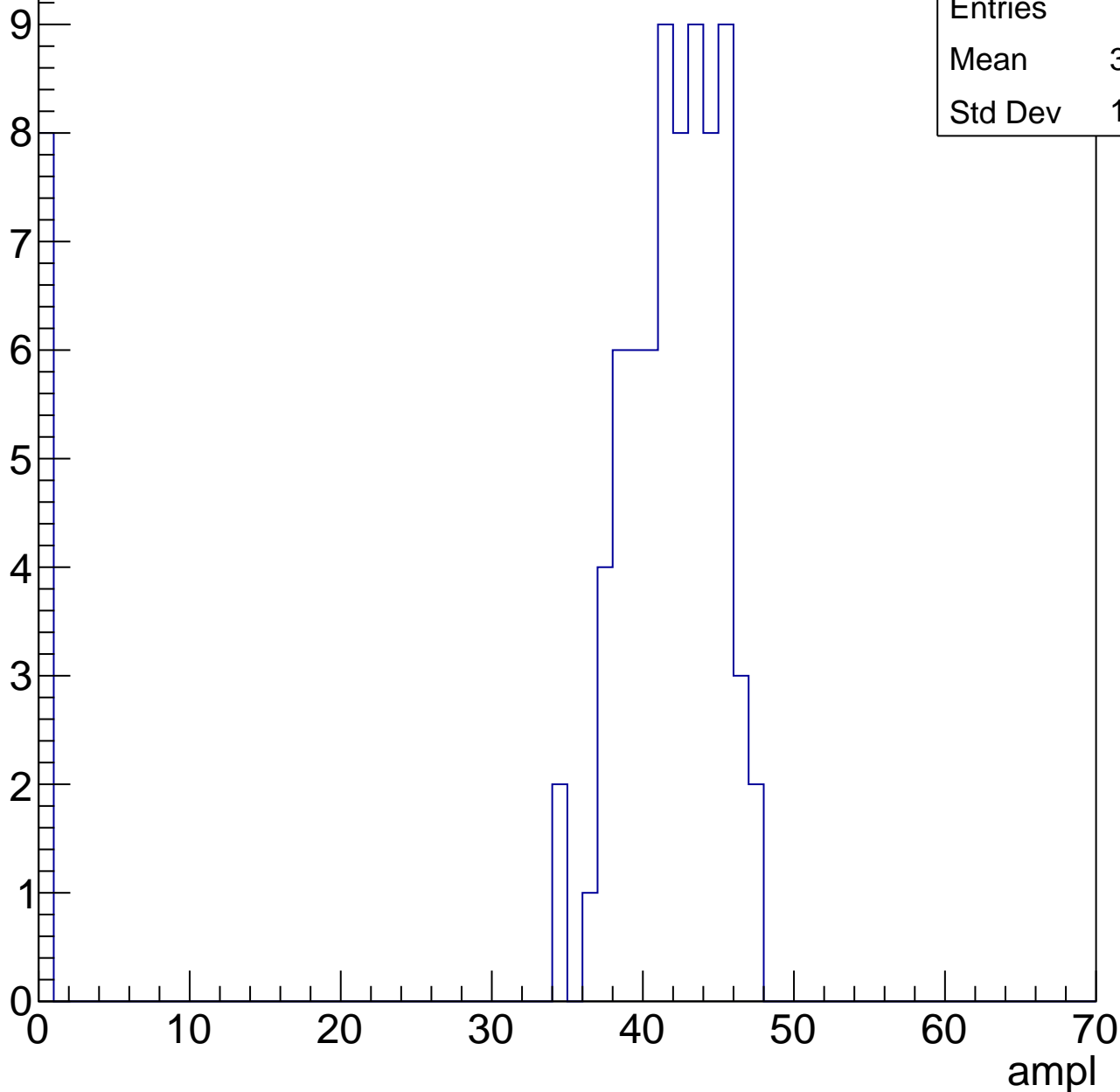
|         |       |
|---------|-------|
| Entries | 54    |
| Mean    | 35.46 |
| Std Dev | 3.589 |



# B1L103S, U4-ch37, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

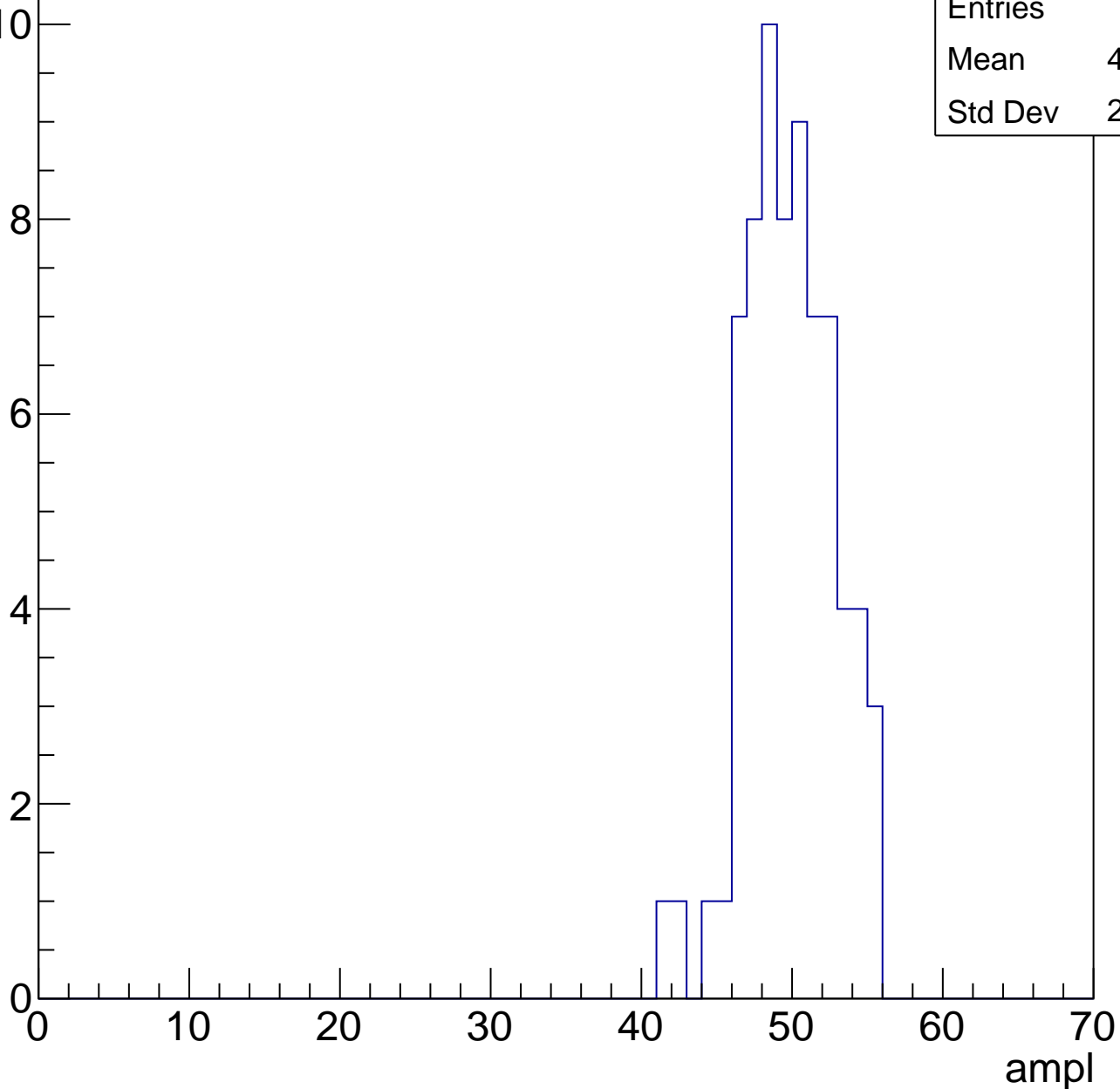


# B1L103S, U4-ch37, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

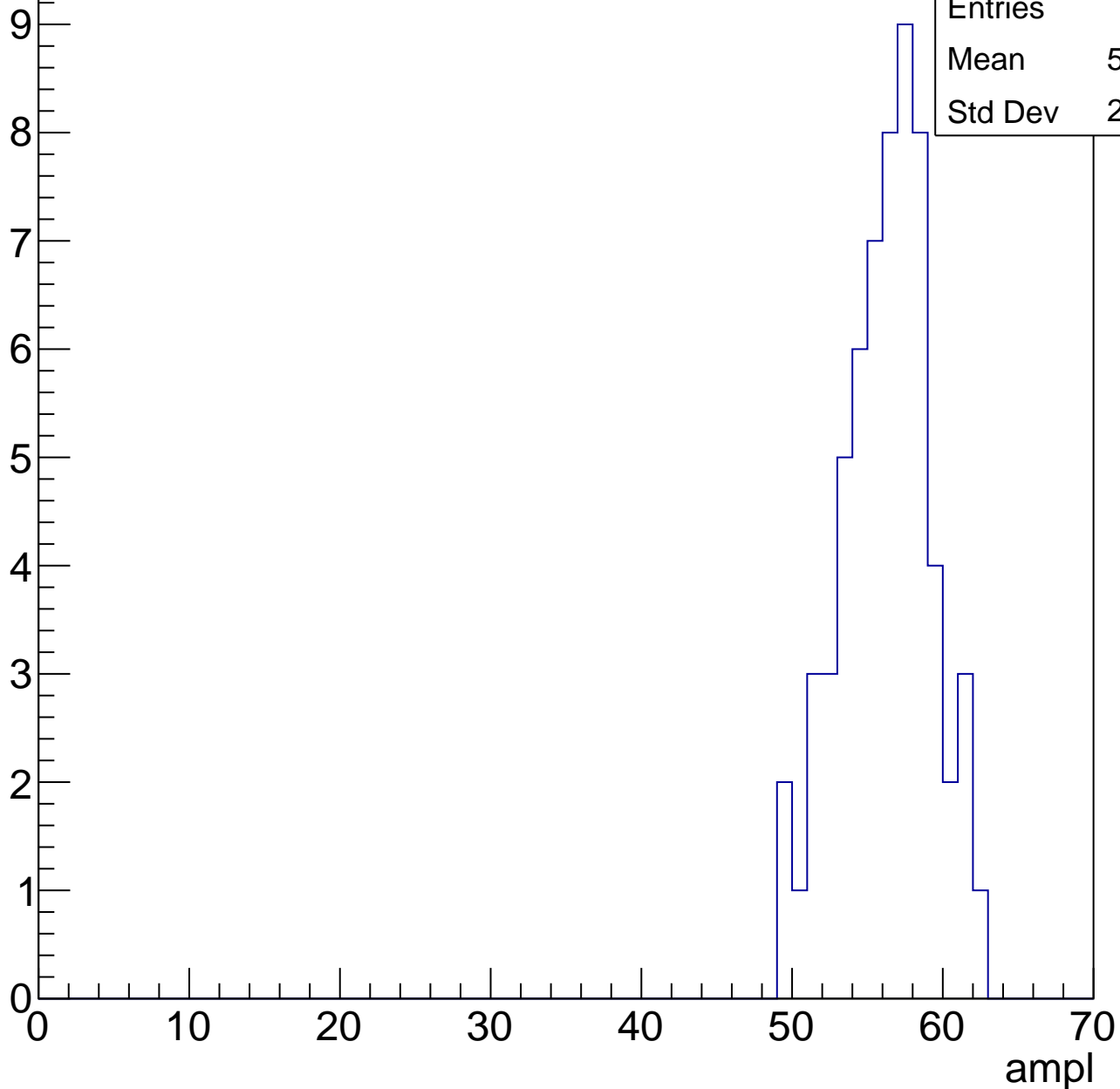
|         |       |
|---------|-------|
| Entries | 71    |
| Mean    | 49.38 |
| Std Dev | 2.957 |



# B1L103S, U4-ch37, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



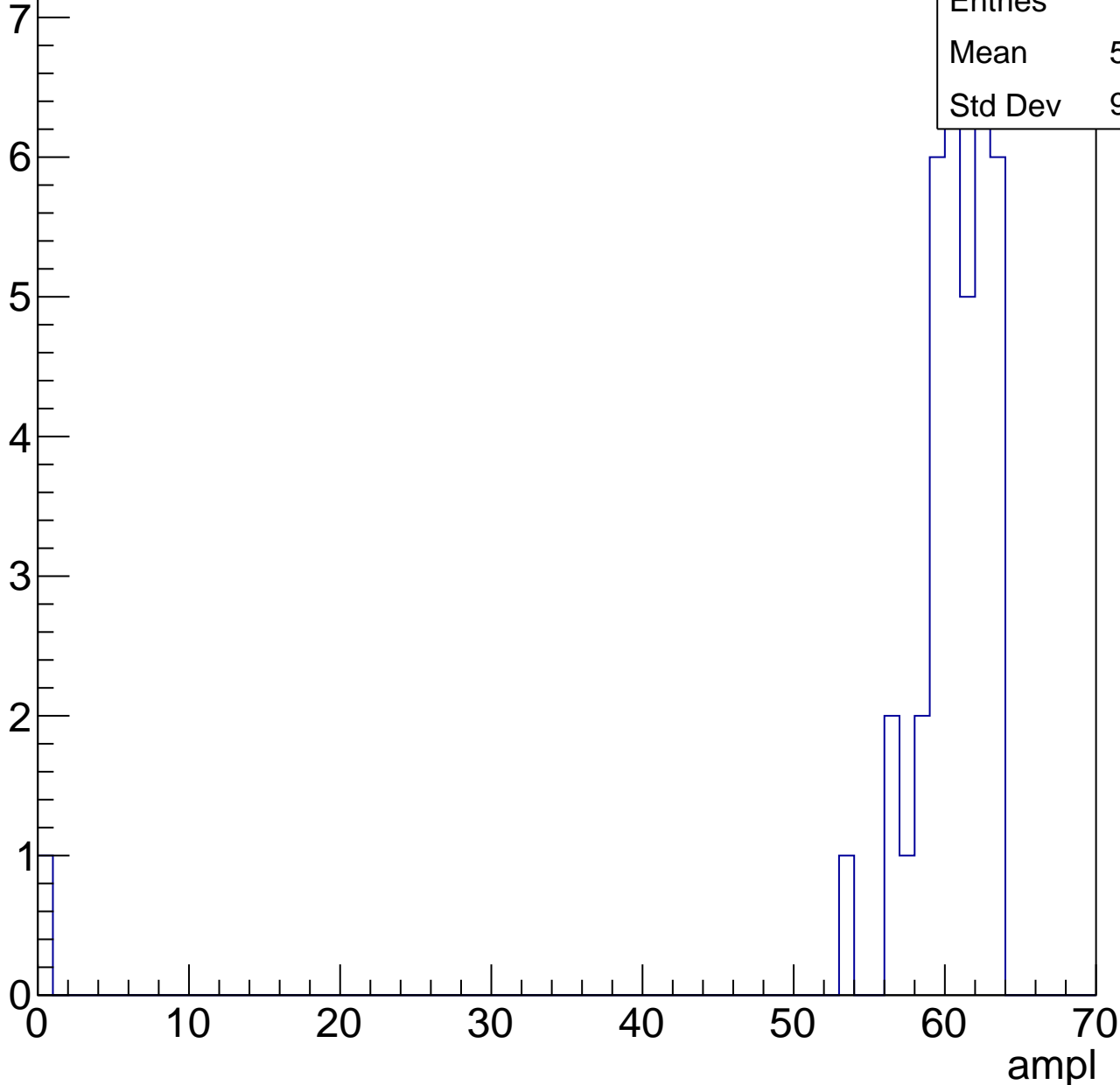
|         |       |
|---------|-------|
| Entries | 62    |
| Mean    | 55.76 |
| Std Dev | 2.977 |

# B1L103S, U4-ch37, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

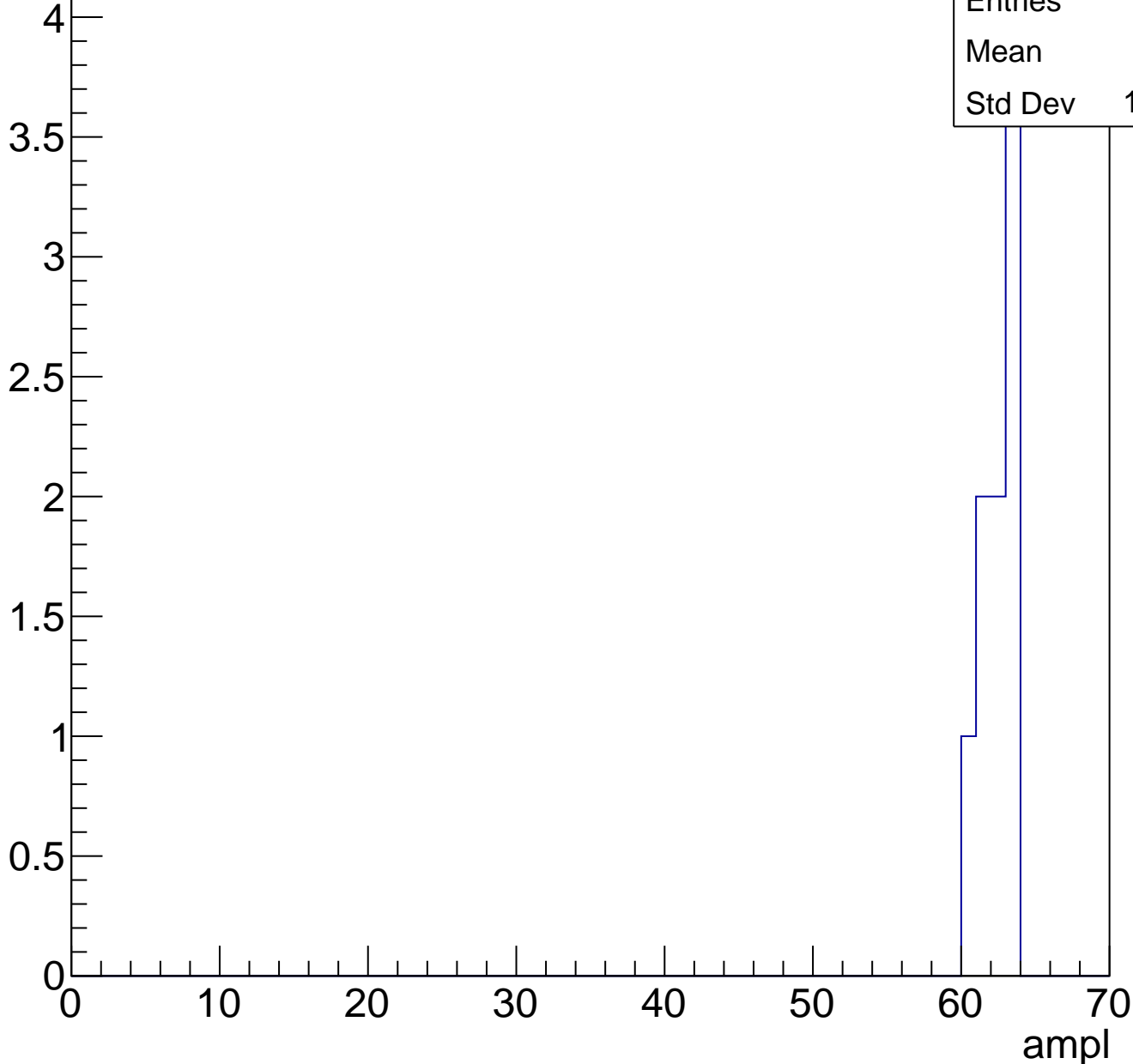
|         |       |
|---------|-------|
| Entries | 38    |
| Mean    | 58.66 |
| Std Dev | 9.898 |



# B1L103S, U4-ch37, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U4-ch37, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



|         |    |
|---------|----|
| Entries | 19 |
| Mean    | 0  |
| Std Dev | 0  |

# B1L103S, U4-ch38, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

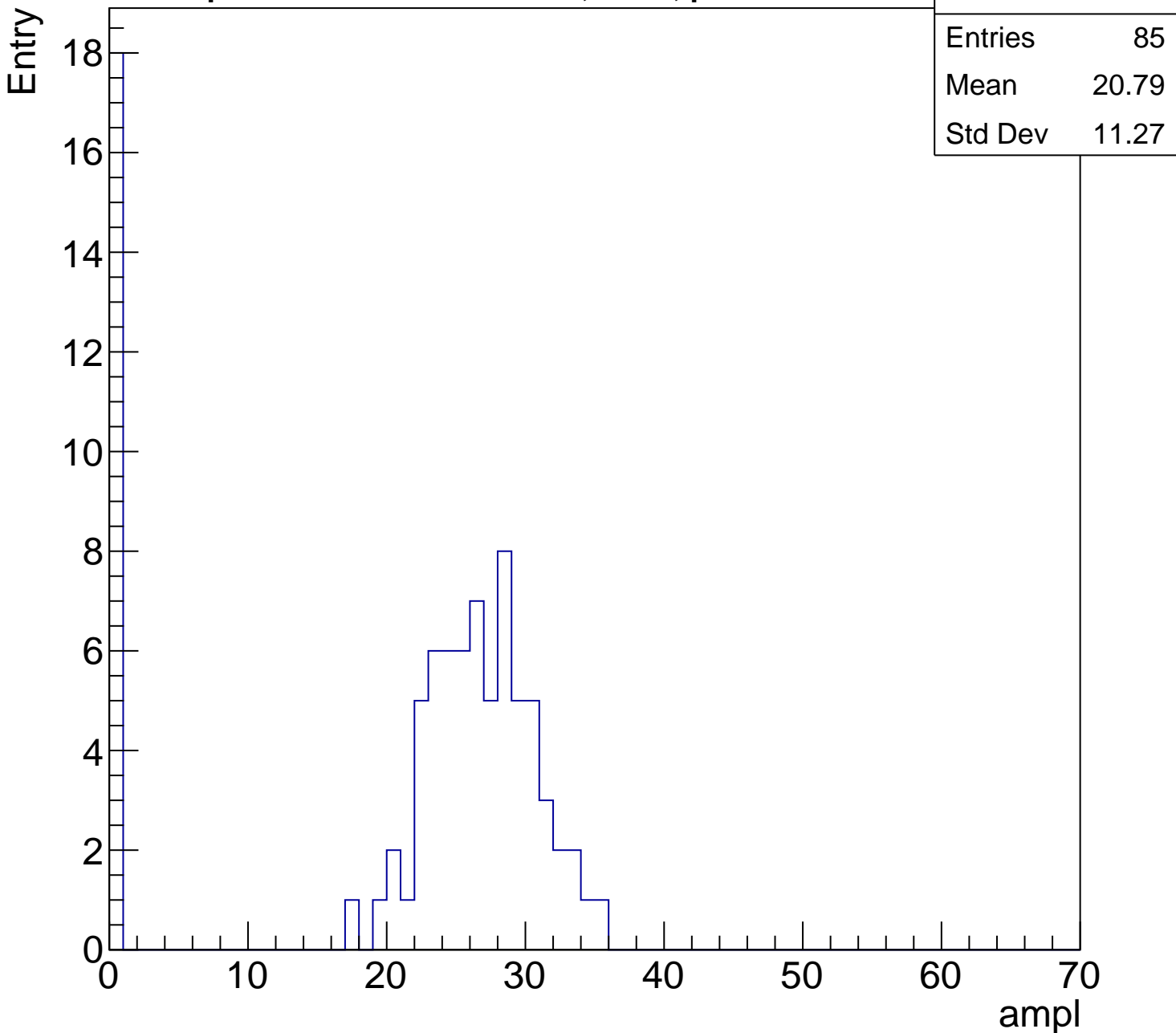
|         |       |
|---------|-------|
| Entries | 85    |
| Mean    | 20.79 |
| Std Dev | 11.27 |

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

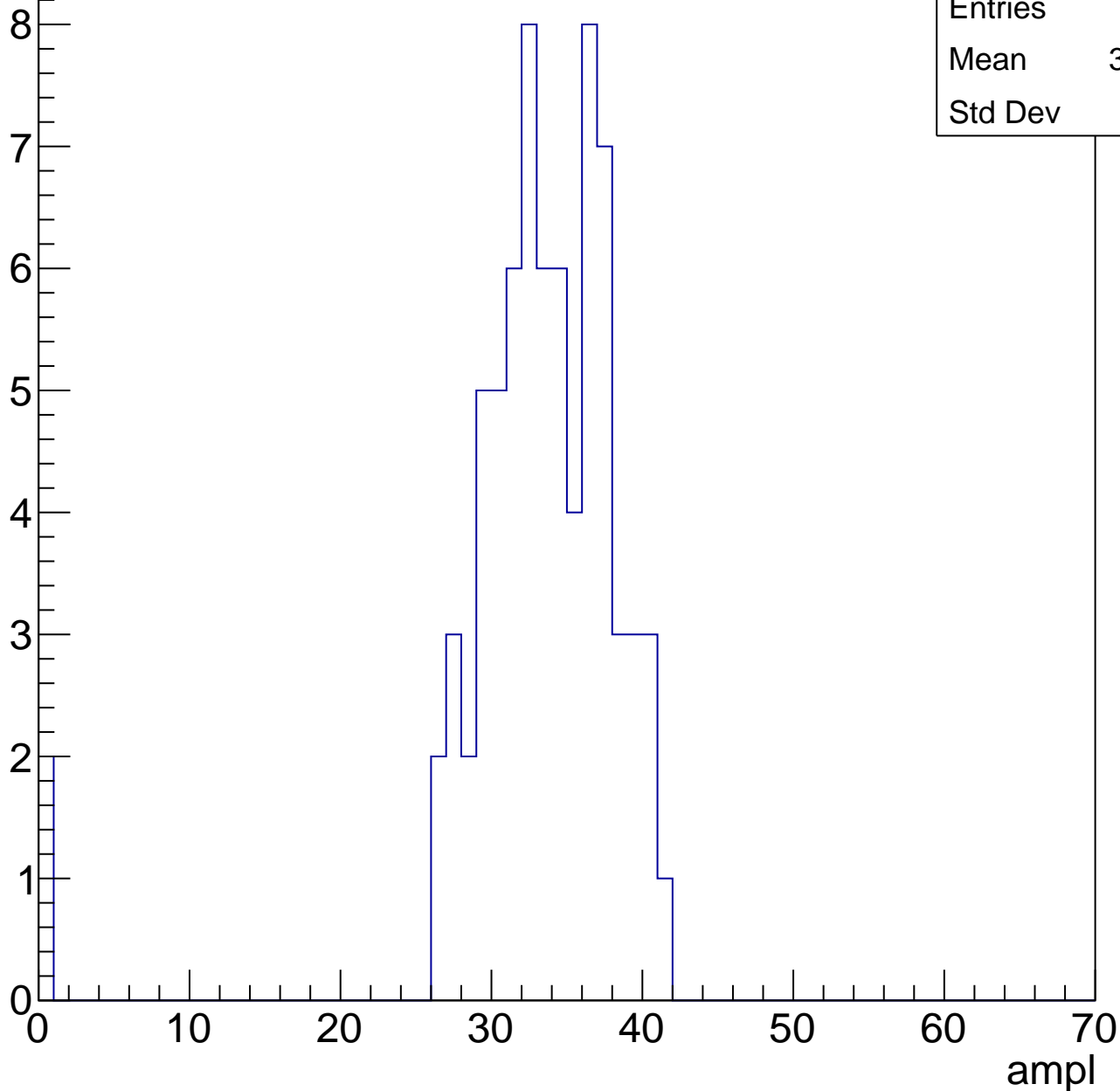


# B1L103S, U4-ch38, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 74    |
| Mean    | 32.53 |
| Std Dev | 6.55  |

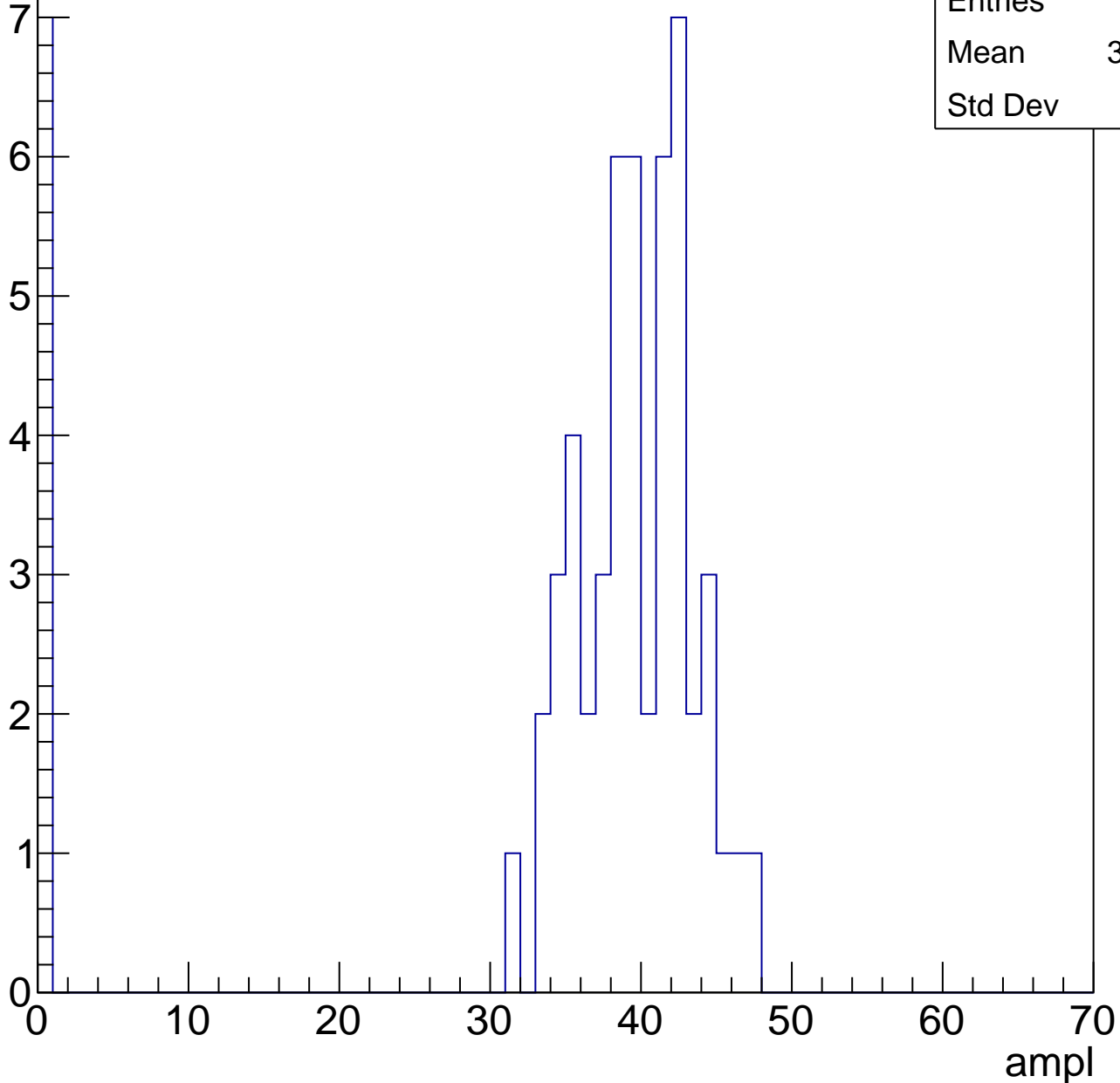


# B1L103S, U4-ch38, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 57    |
| Mean    | 34.39 |
| Std Dev | 13.3  |

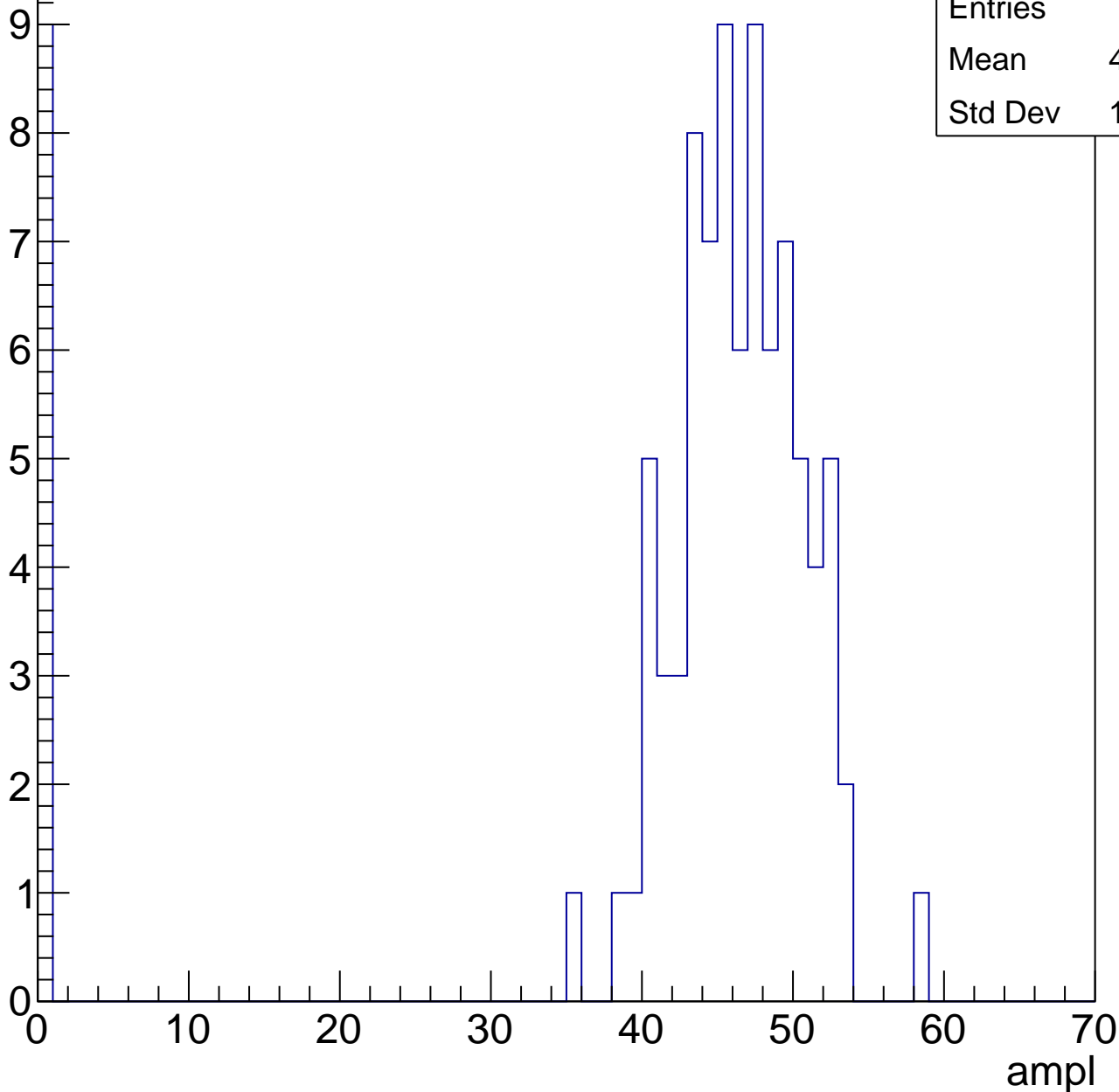


# B1L103S, U4-ch38, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 92    |
| Mean    | 41.59 |
| Std Dev | 14.22 |

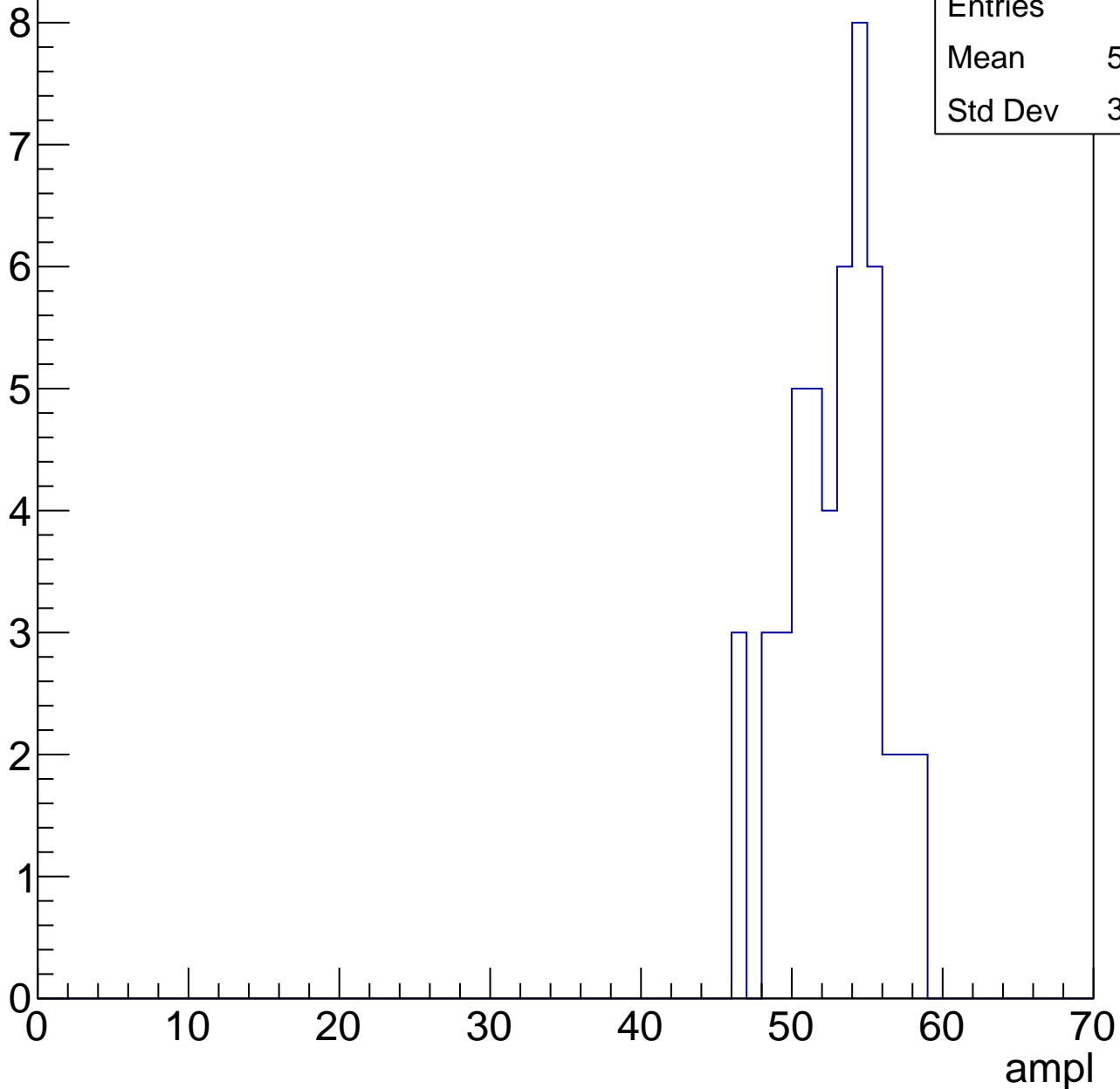


# B1L103S, U4-ch38, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

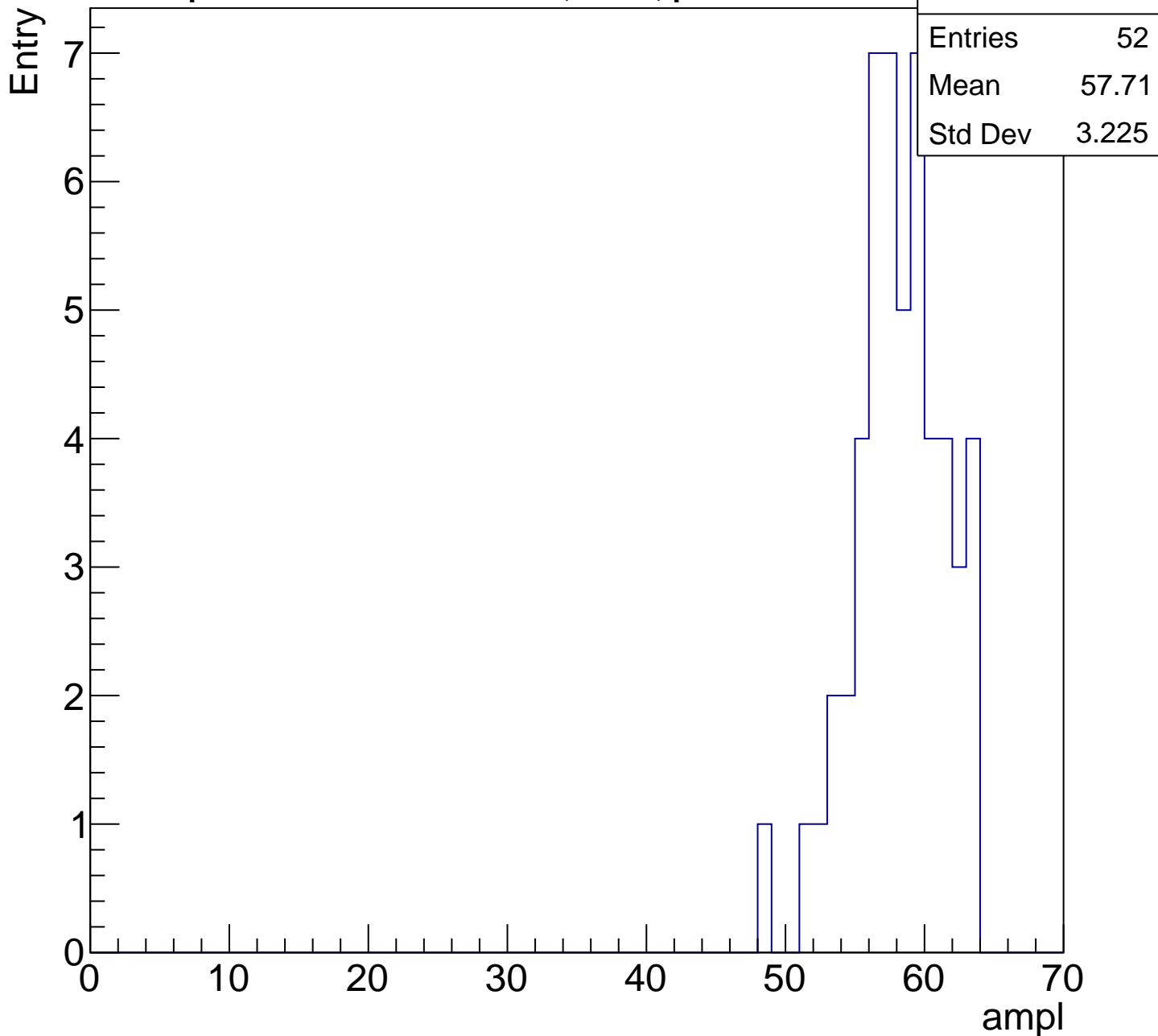
Entry

|         |       |
|---------|-------|
| Entries | 49    |
| Mean    | 52.33 |
| Std Dev | 3.026 |



# B1L103S, U4-ch38, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

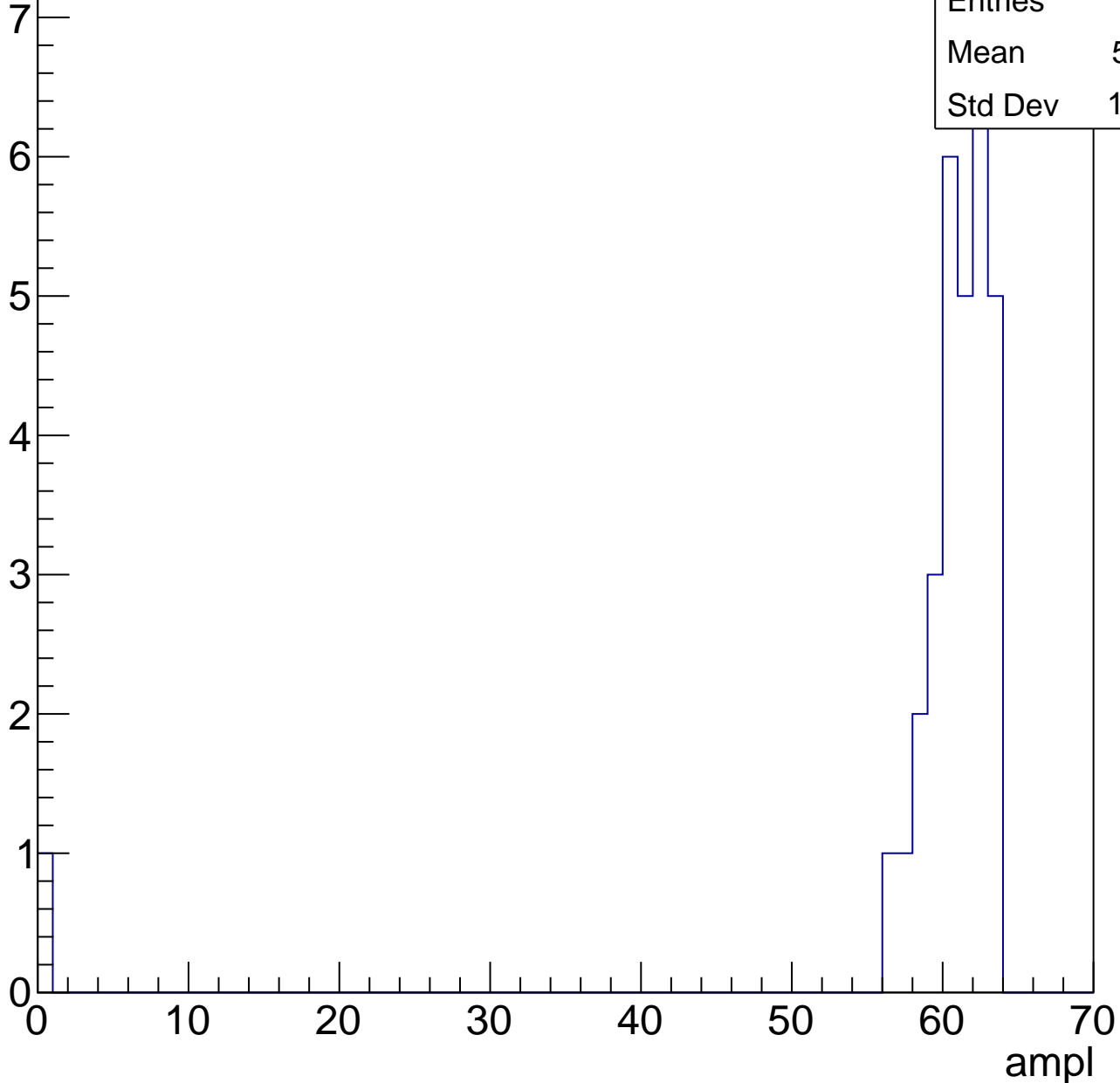


# B1L103S, U4-ch38, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 31    |
| Mean    | 58.71 |
| Std Dev | 10.87 |

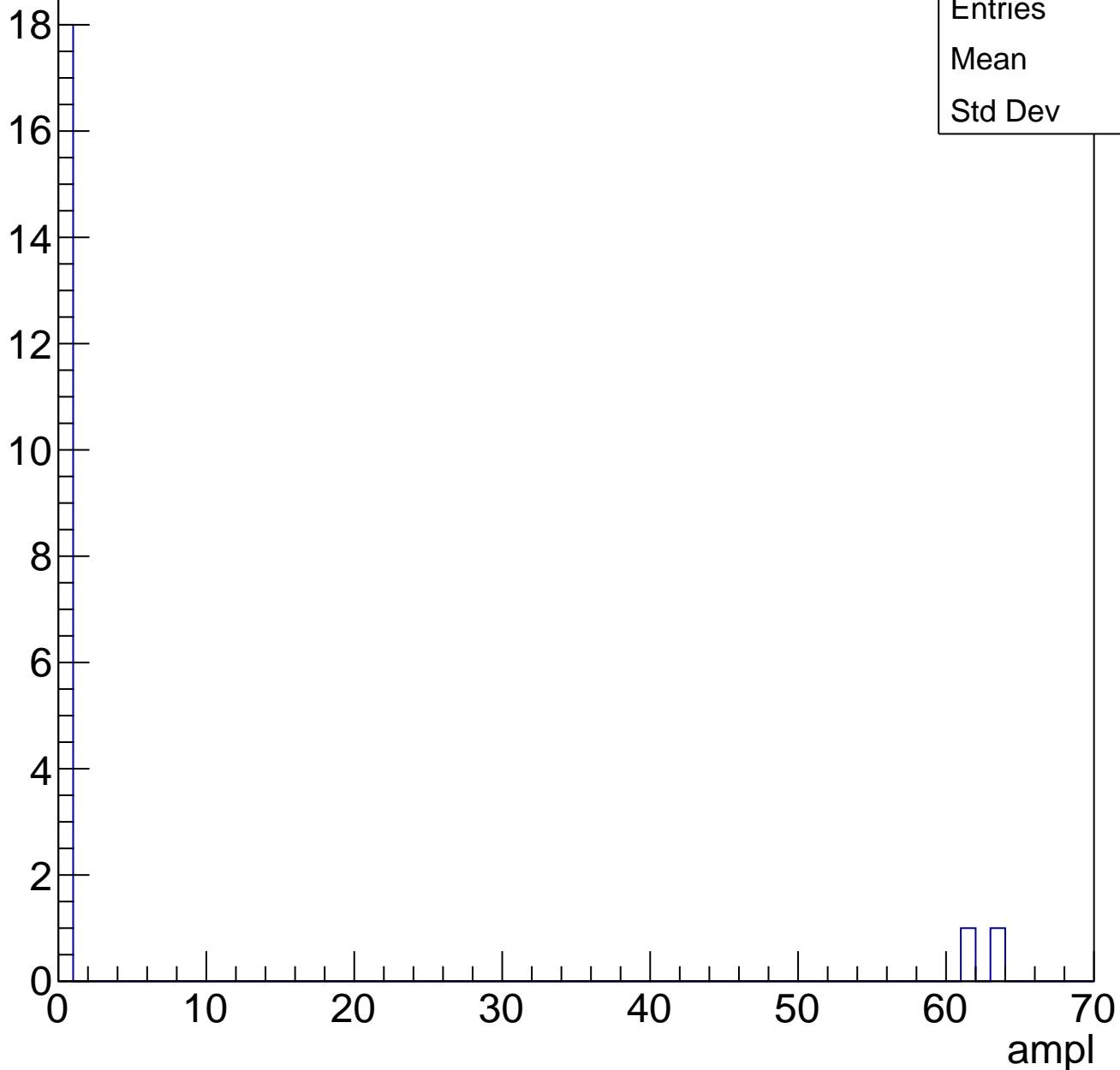




# B1L103S, U4-ch38, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



|         |      |
|---------|------|
| Entries | 20   |
| Mean    | 6.2  |
| Std Dev | 18.6 |

# B1L103S, U4-ch39, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 86    |
| Mean    | 24.42 |
| Std Dev | 12.57 |

Entry

16  
14  
12  
10  
8  
6  
4  
2  
0

0

10

20

30

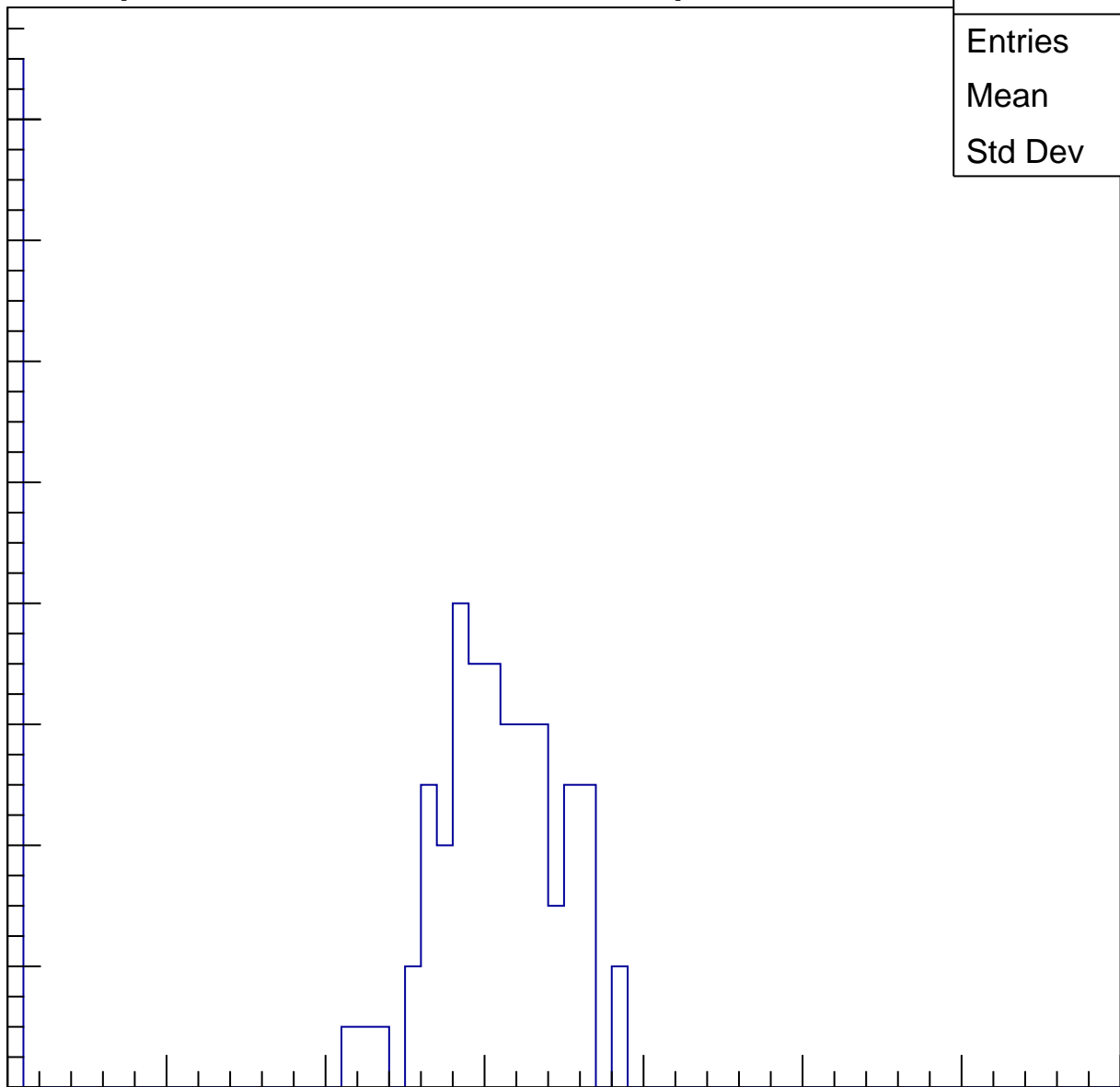
40

50

60

70

ampl

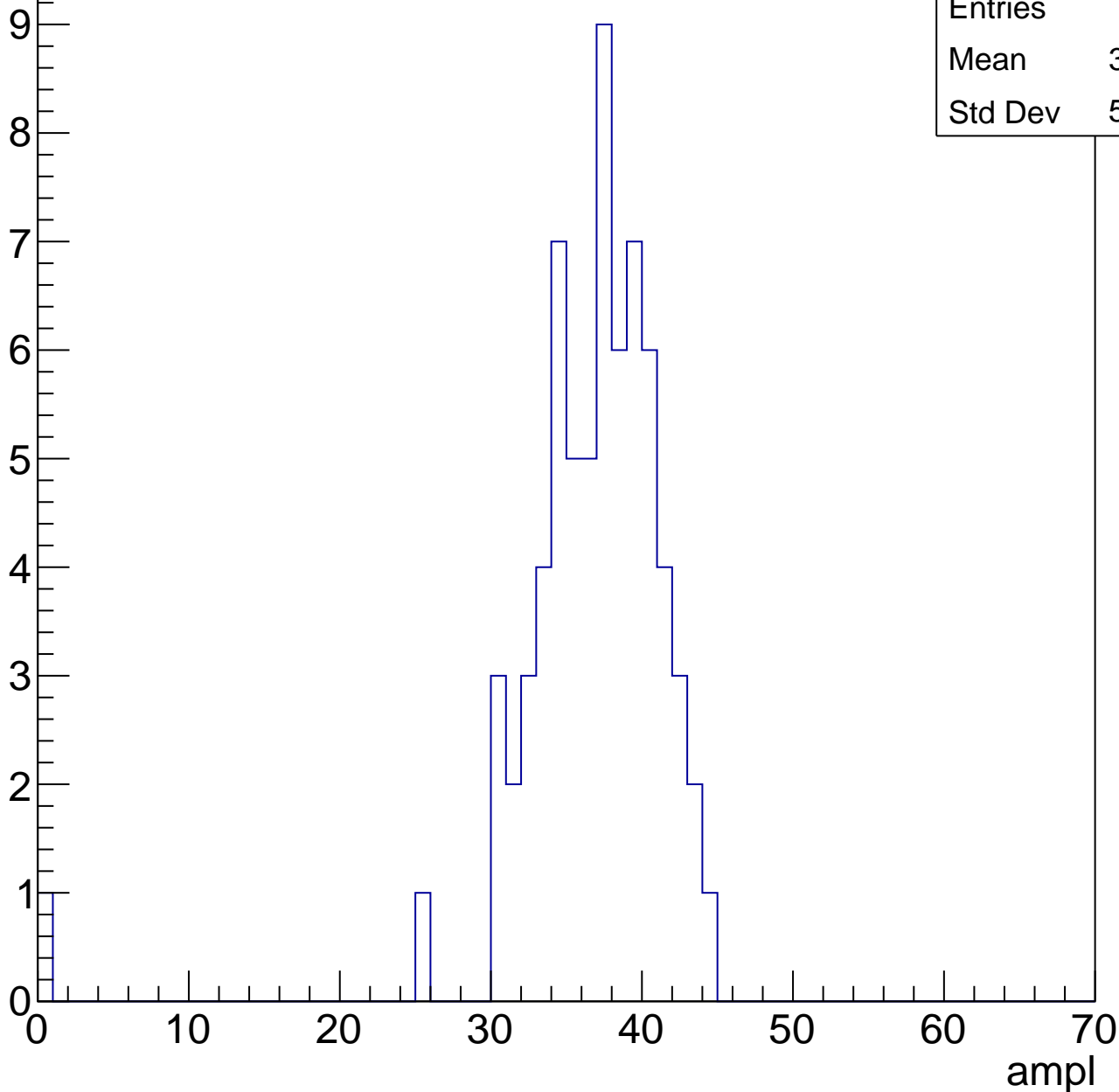


# B1L103S, U4-ch39, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 69    |
| Mean    | 36.12 |
| Std Dev | 5.714 |

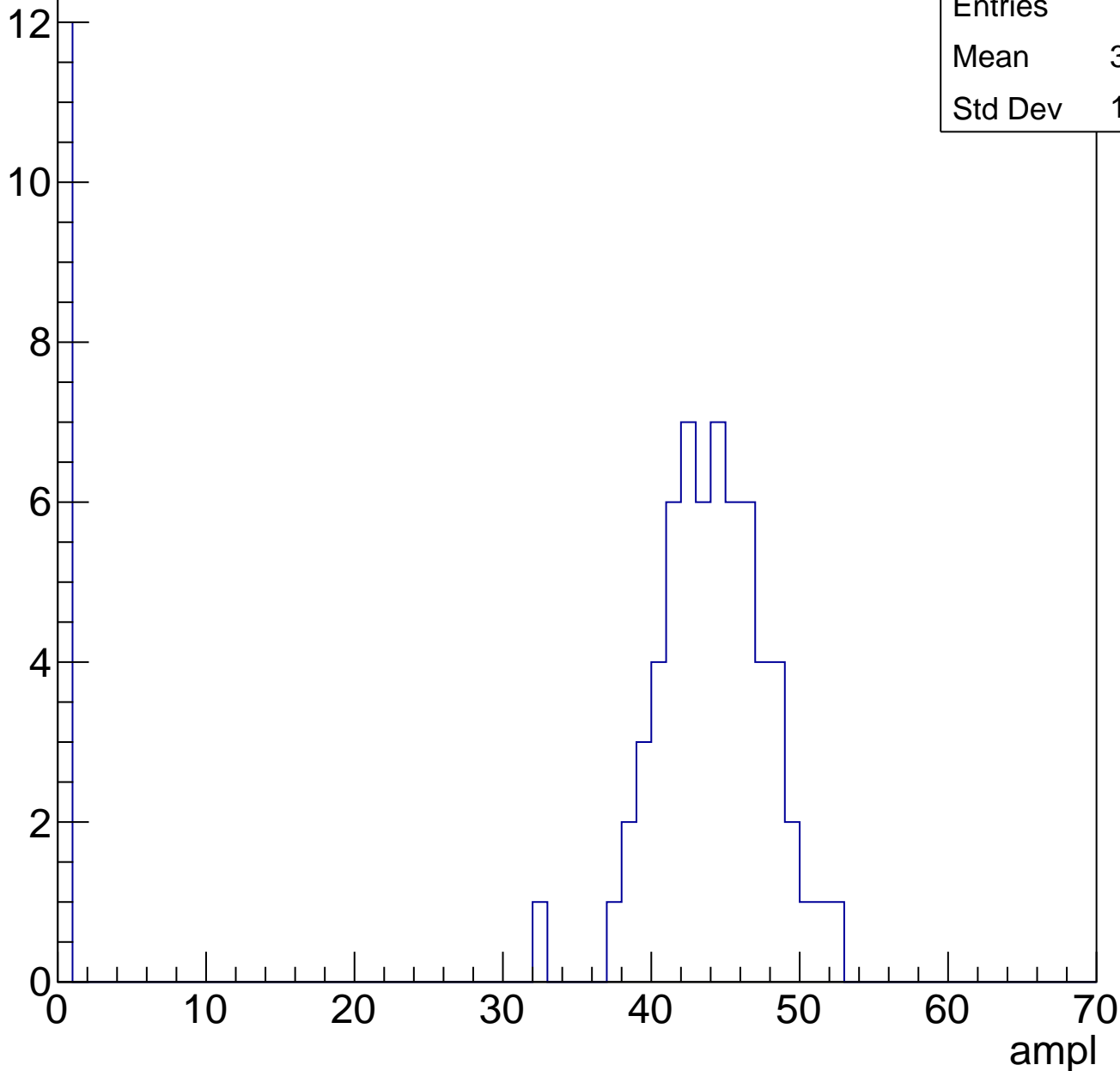


# B1L103S, U4-ch39, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 74    |
| Mean    | 36.55 |
| Std Dev | 16.42 |

Entry

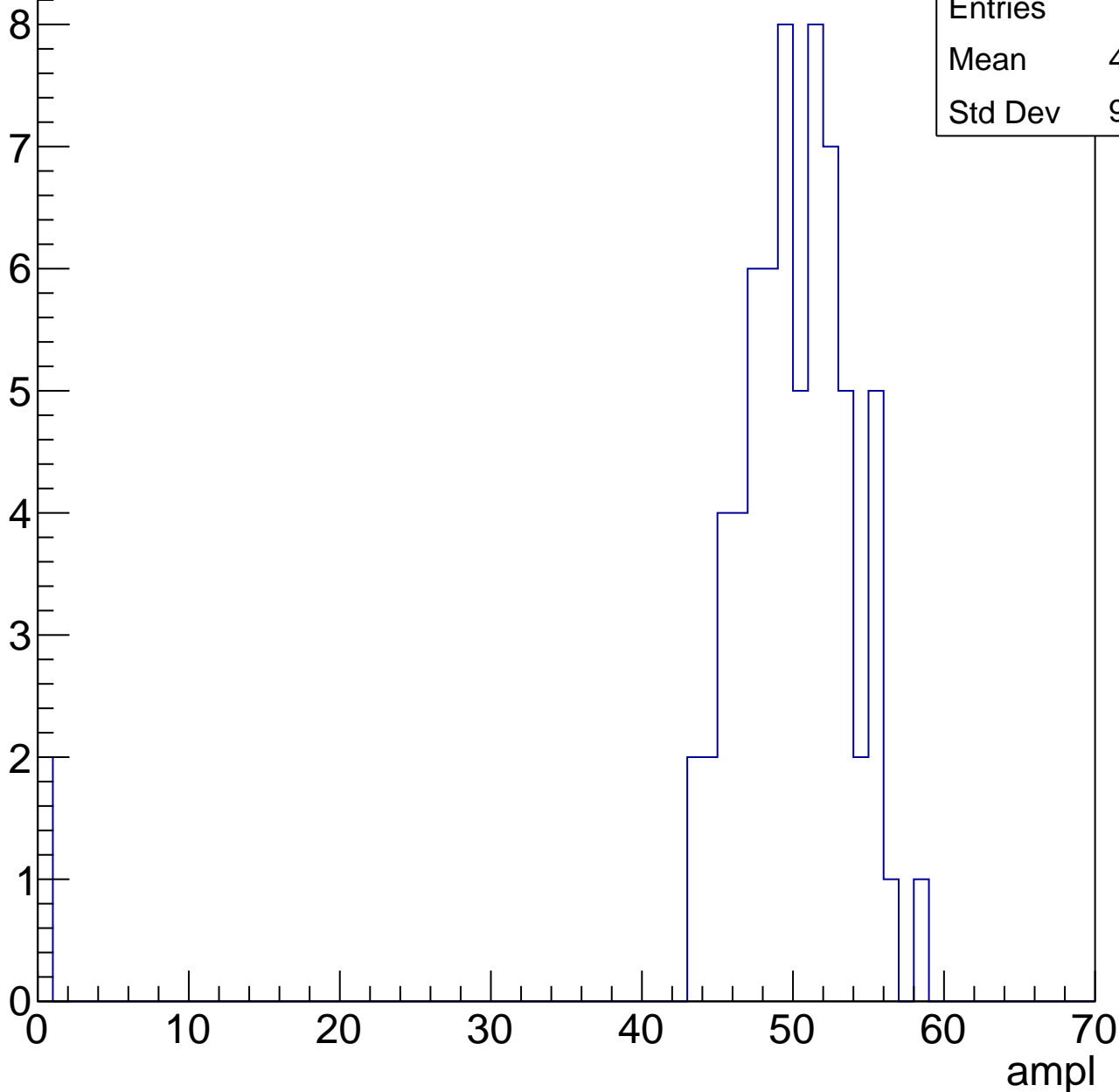


# B1L103S, U4-ch39, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

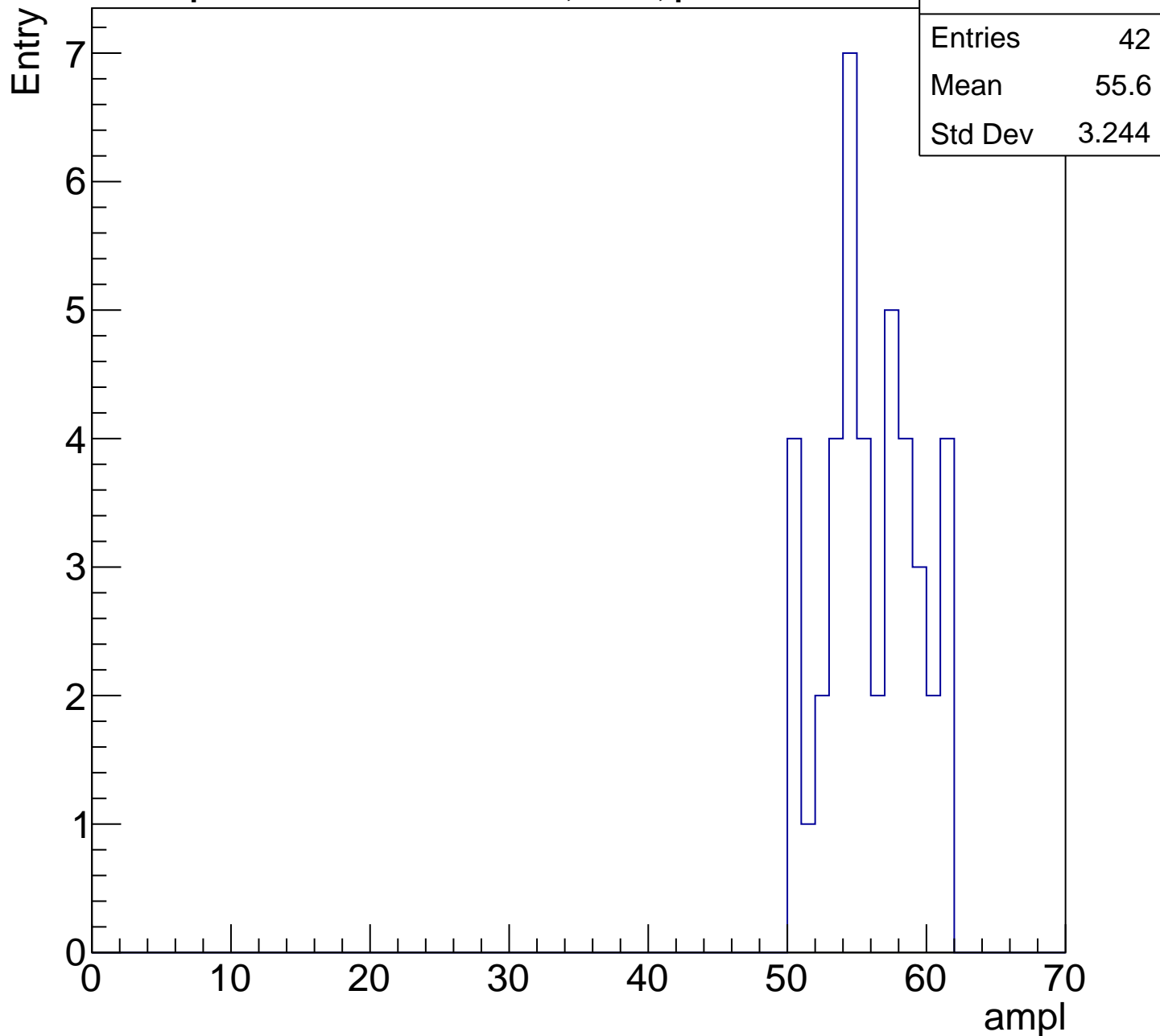
Entry

|         |       |
|---------|-------|
| Entries | 68    |
| Mean    | 48.29 |
| Std Dev | 9.042 |



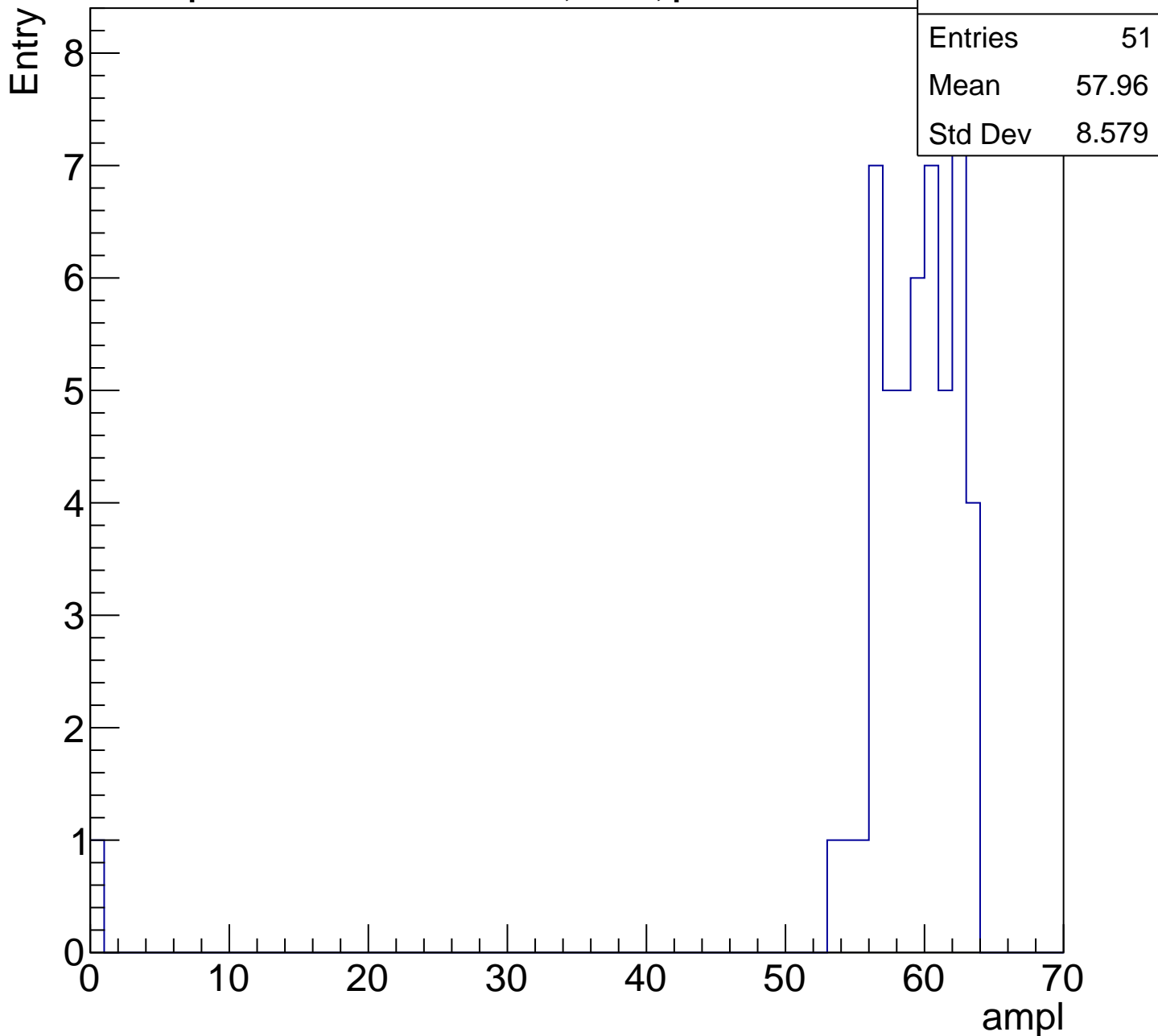
# B1L103S, U4-ch39, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2



# B1L103S, U4-ch39, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

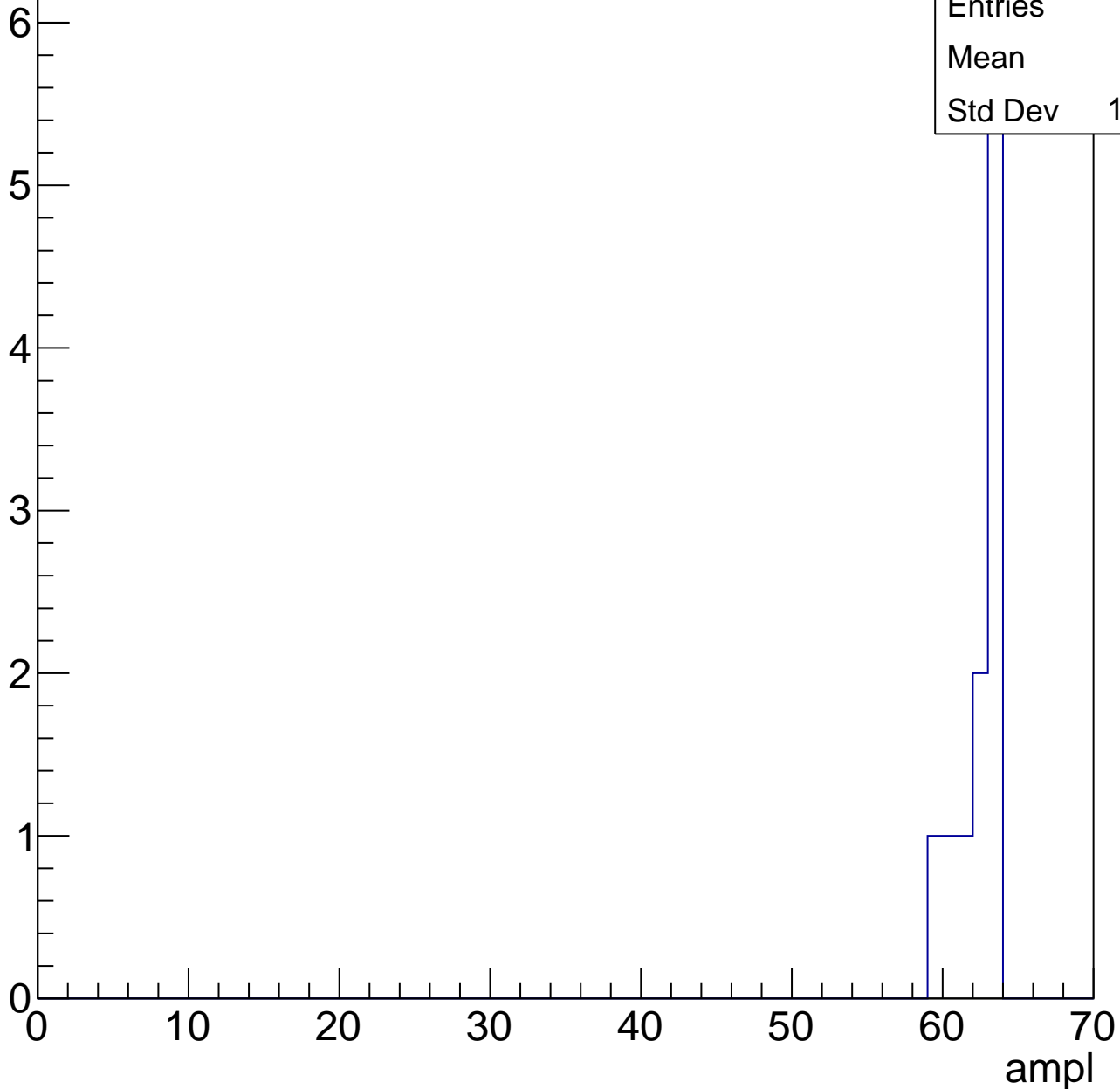


# B1L103S, U4-ch39, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 11    |
| Mean    | 62    |
| Std Dev | 1.348 |





# B1L103S, U4-ch39, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

|         |    |
|---------|----|
| Entries | 19 |
| Mean    | 0  |
| Std Dev | 0  |

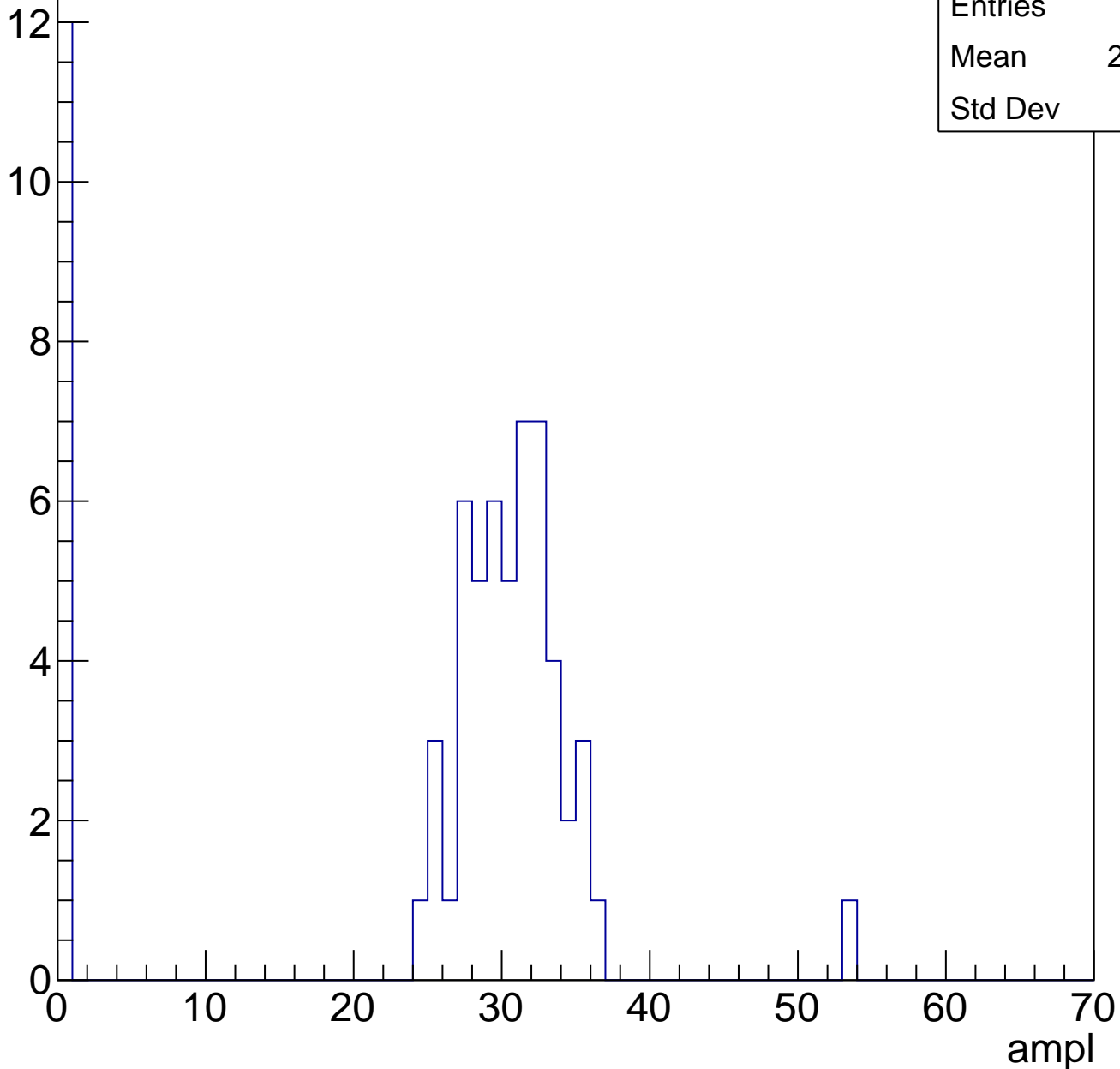
ampl

# B1L103S, U4-ch40, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 64    |
| Mean    | 24.78 |
| Std Dev | 12.5  |

Entry

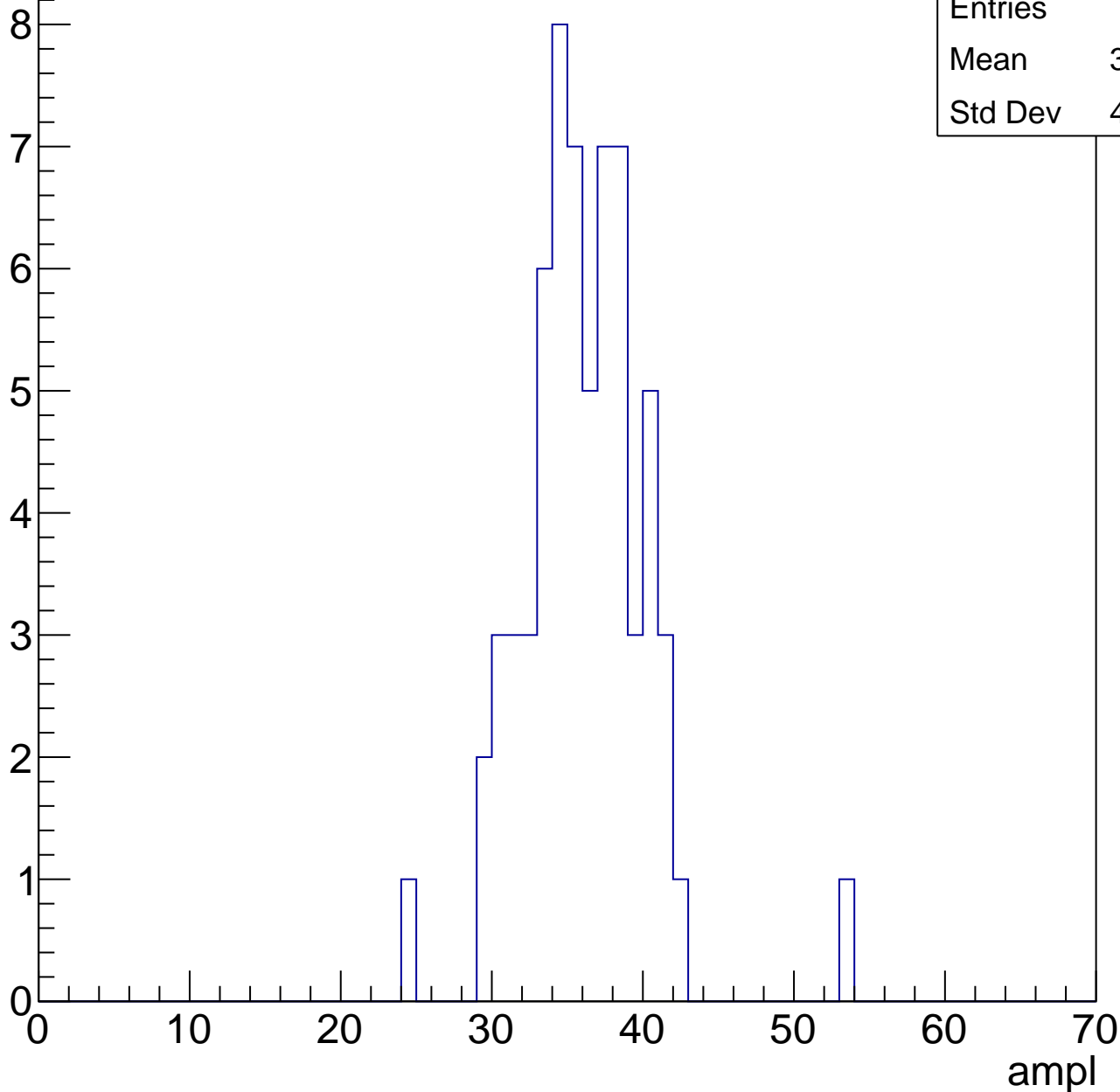


# B1L103S, U4-ch40, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 65    |
| Mean    | 35.63 |
| Std Dev | 4.112 |

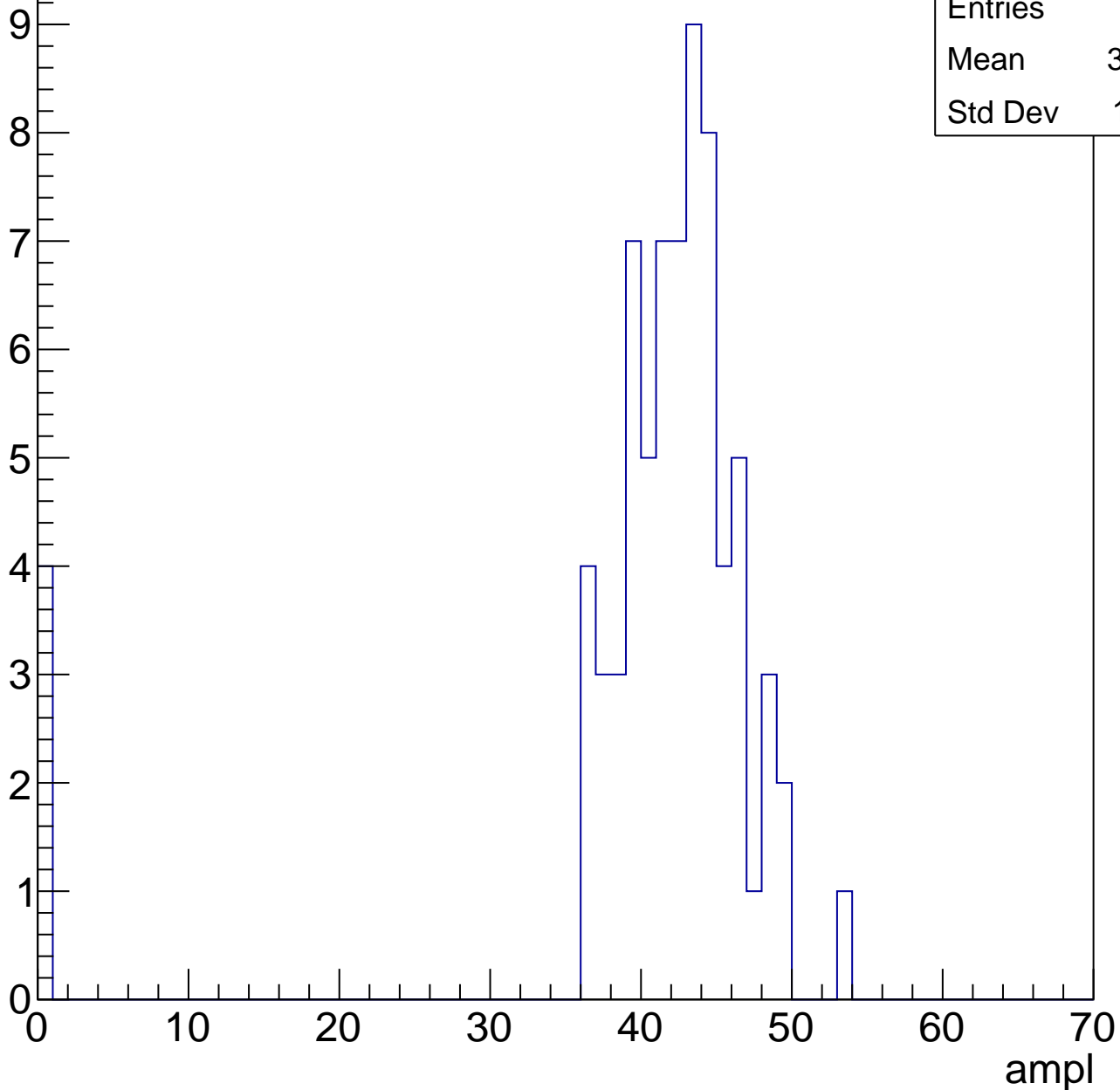


# B1L103S, U4-ch40, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

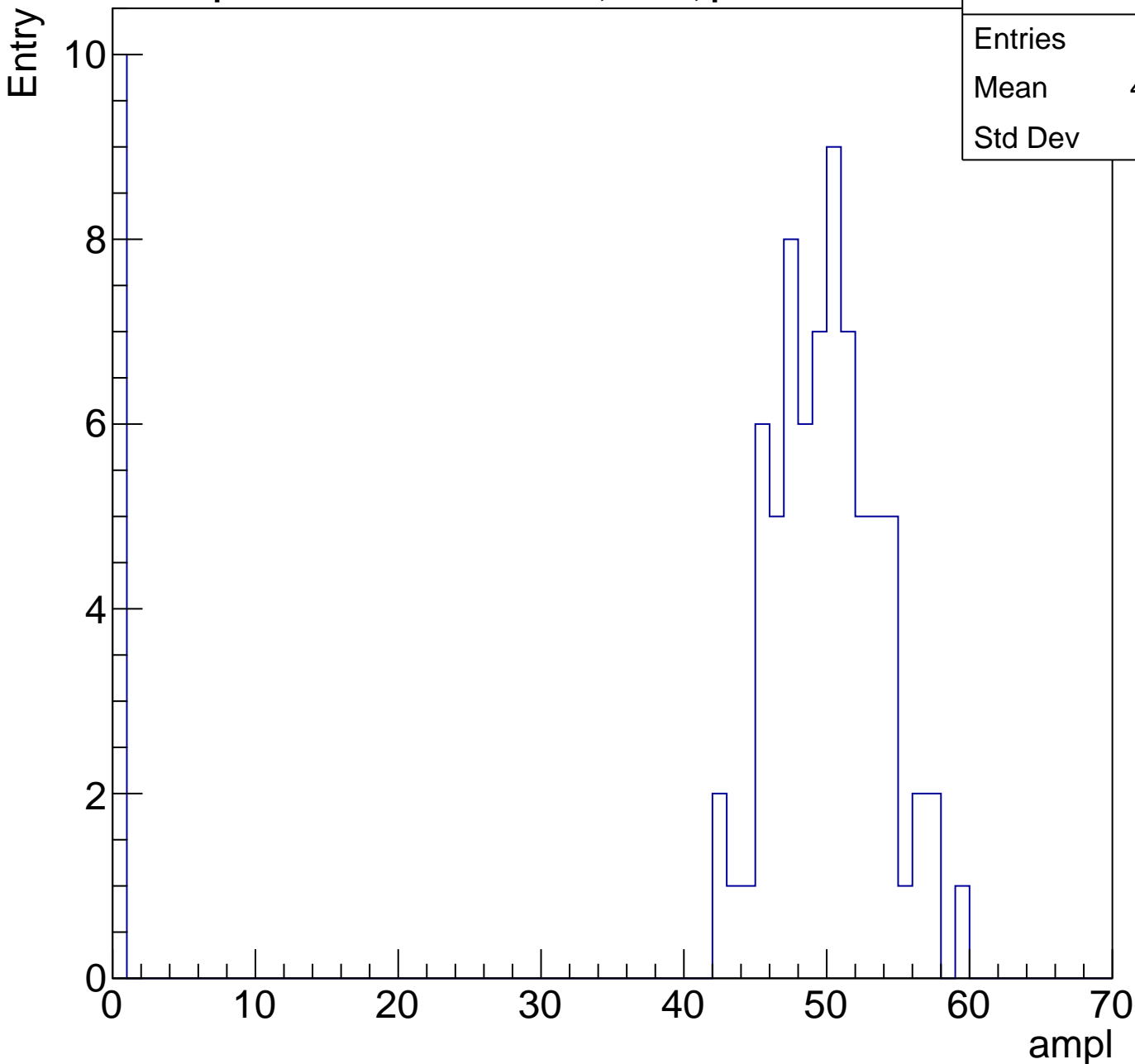
|         |       |
|---------|-------|
| Entries | 73    |
| Mean    | 39.92 |
| Std Dev | 10.21 |



# B1L103S, U4-ch40, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 83    |
| Mean    | 43.61 |
| Std Dev | 16.5  |

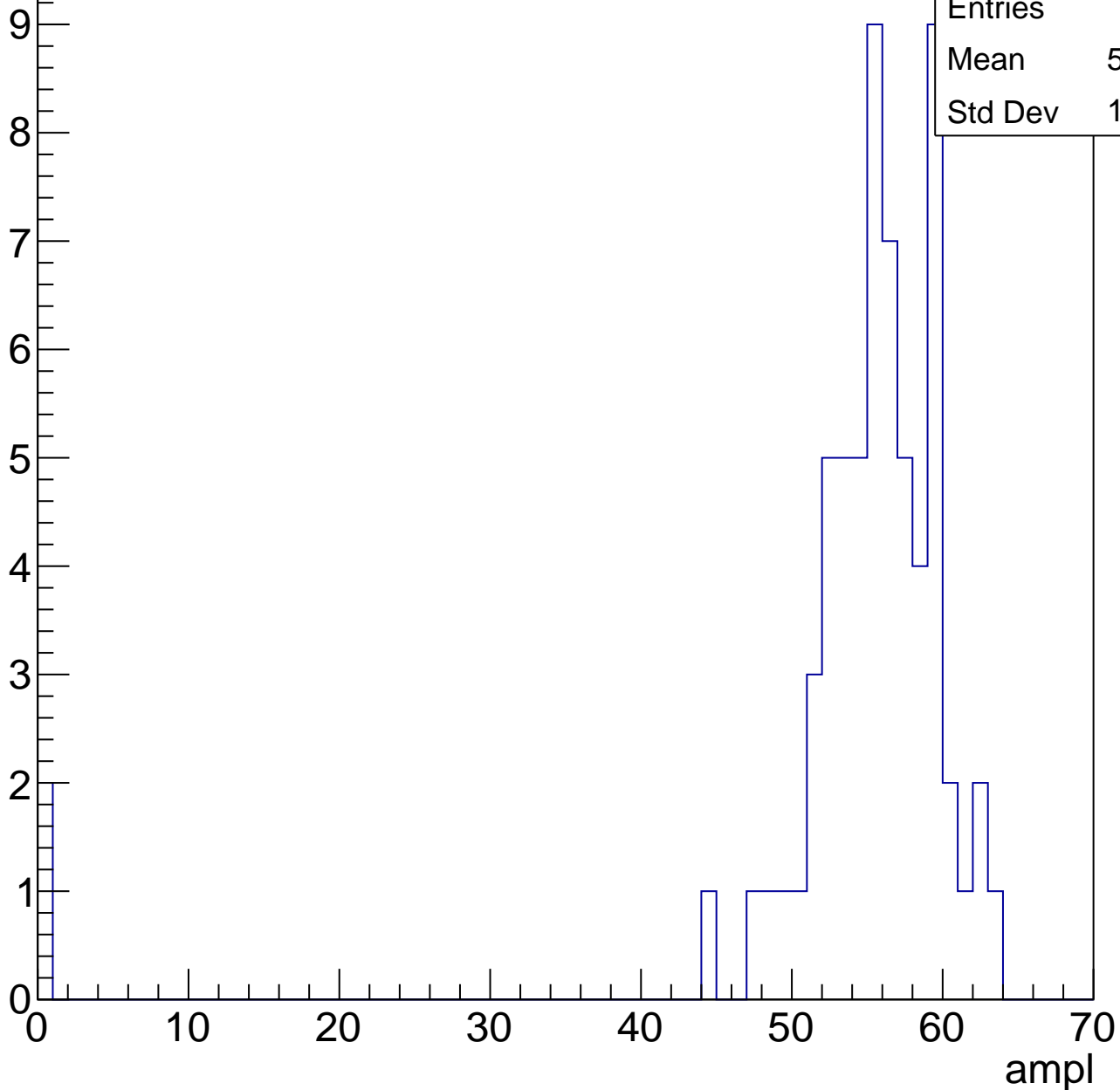


# B1L103S, U4-ch40, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 65    |
| Mean    | 53.68 |
| Std Dev | 10.23 |

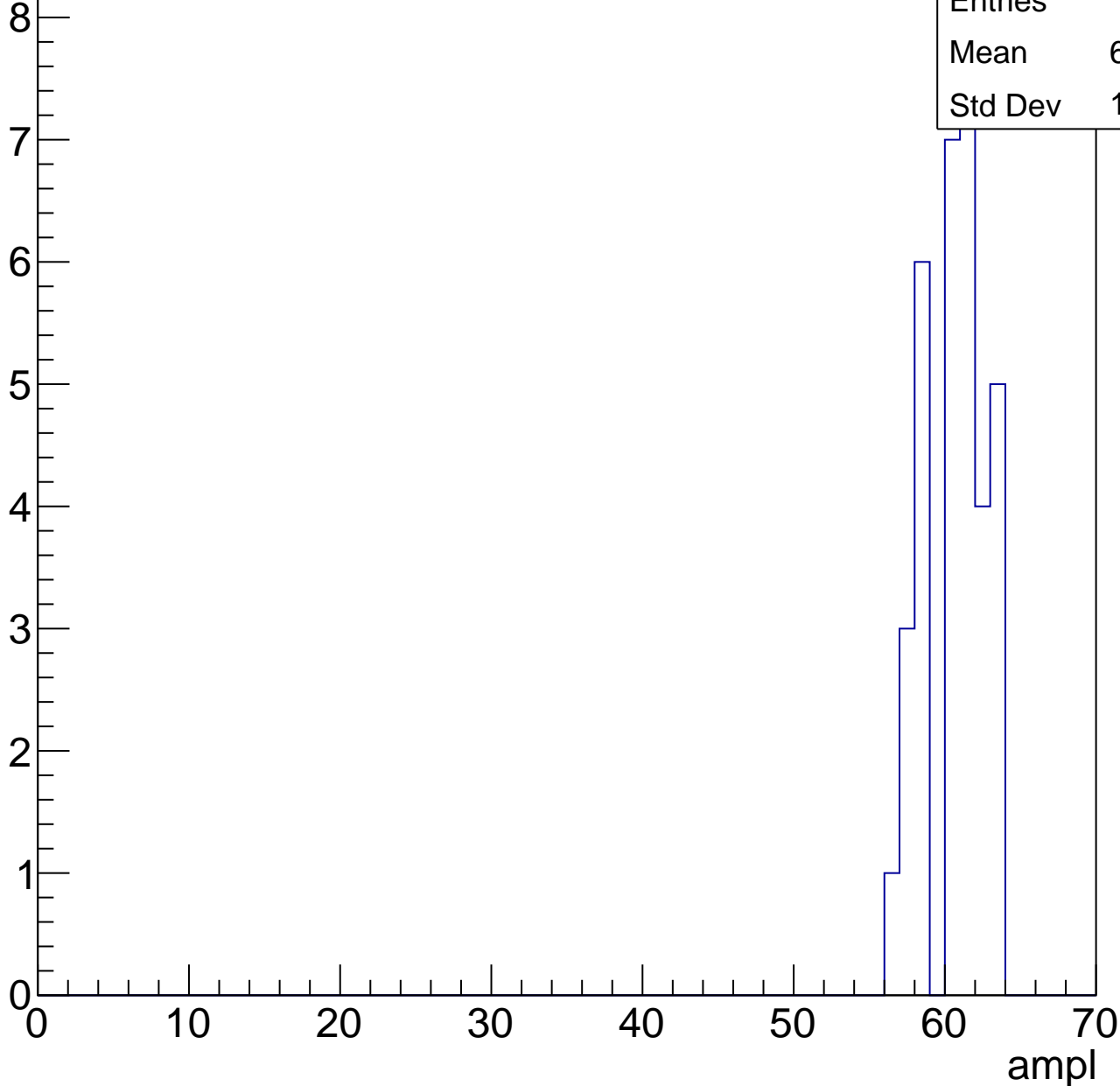


# B1L103S, U4-ch40, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

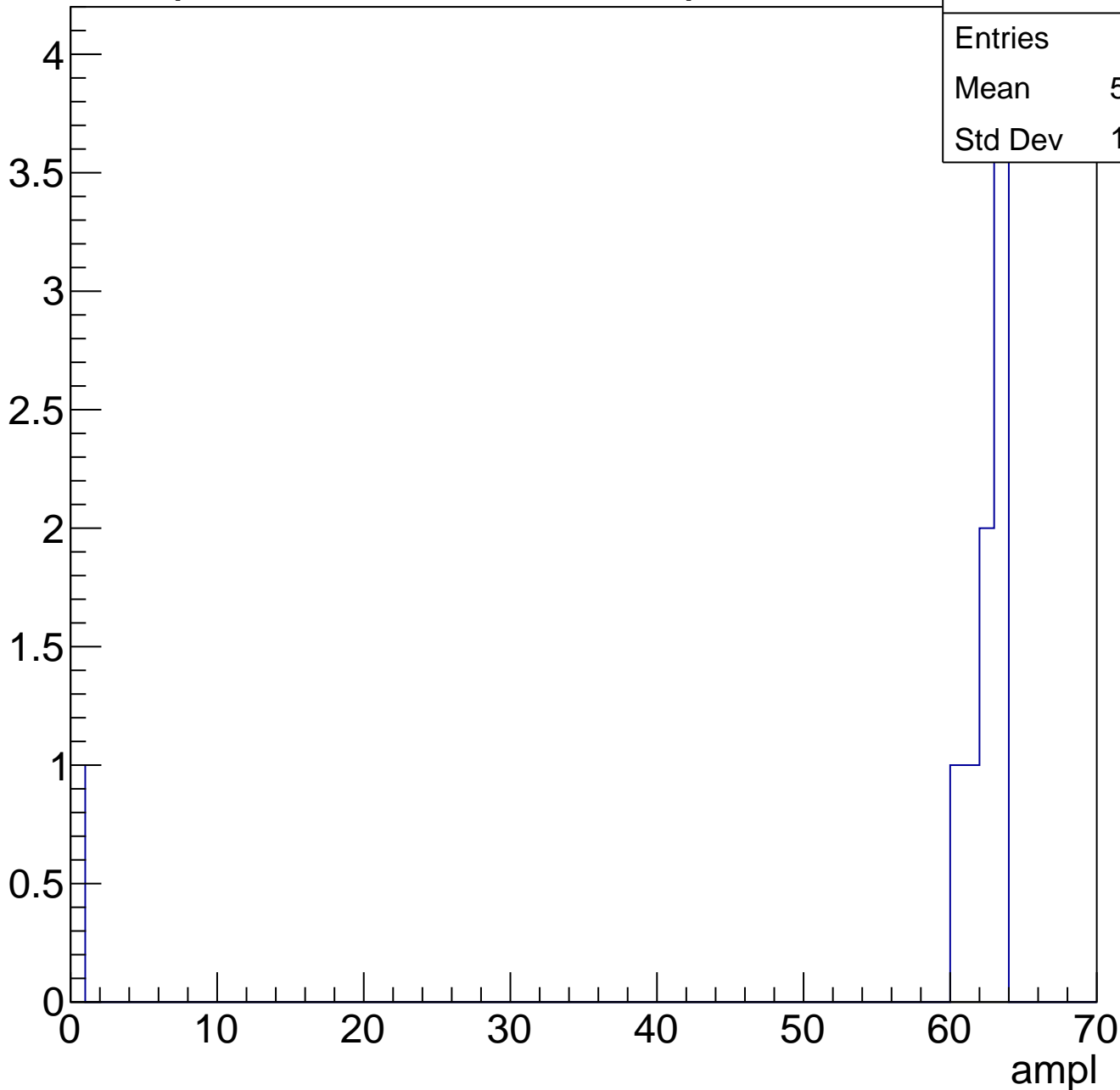
|         |       |
|---------|-------|
| Entries | 34    |
| Mean    | 60.18 |
| Std Dev | 1.992 |



# B1L103S, U4-ch40, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



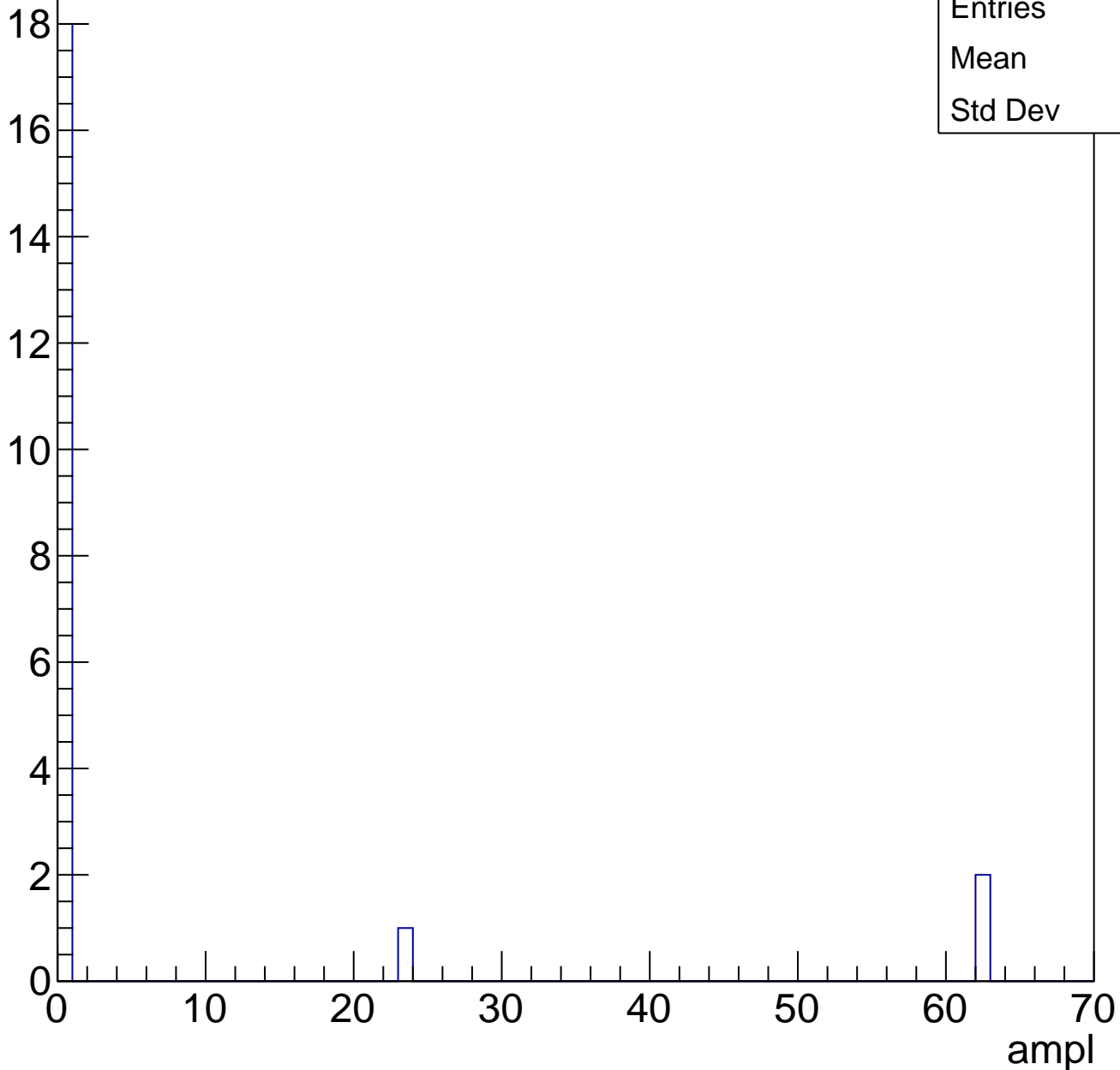


# B1L103S, U4-ch40, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |      |
|---------|------|
| Entries | 21   |
| Mean    | 7    |
| Std Dev | 18.5 |

Entry



# B1L103S, U4-ch41, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 69    |
| Mean    | 24.13 |
| Std Dev | 10.9  |

Entry

10

8

6

4

2

0

0

10

20

30

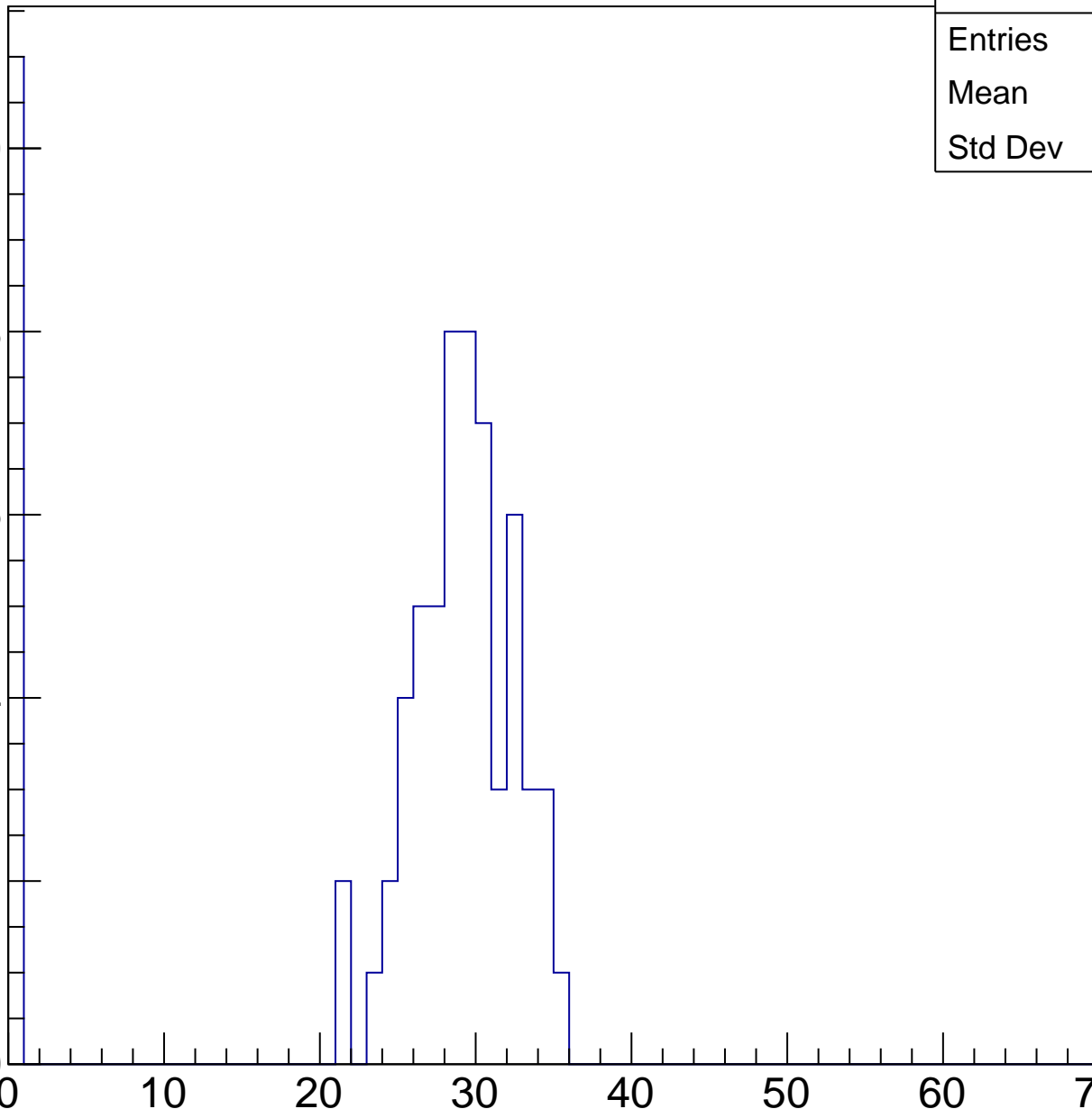
40

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ampl

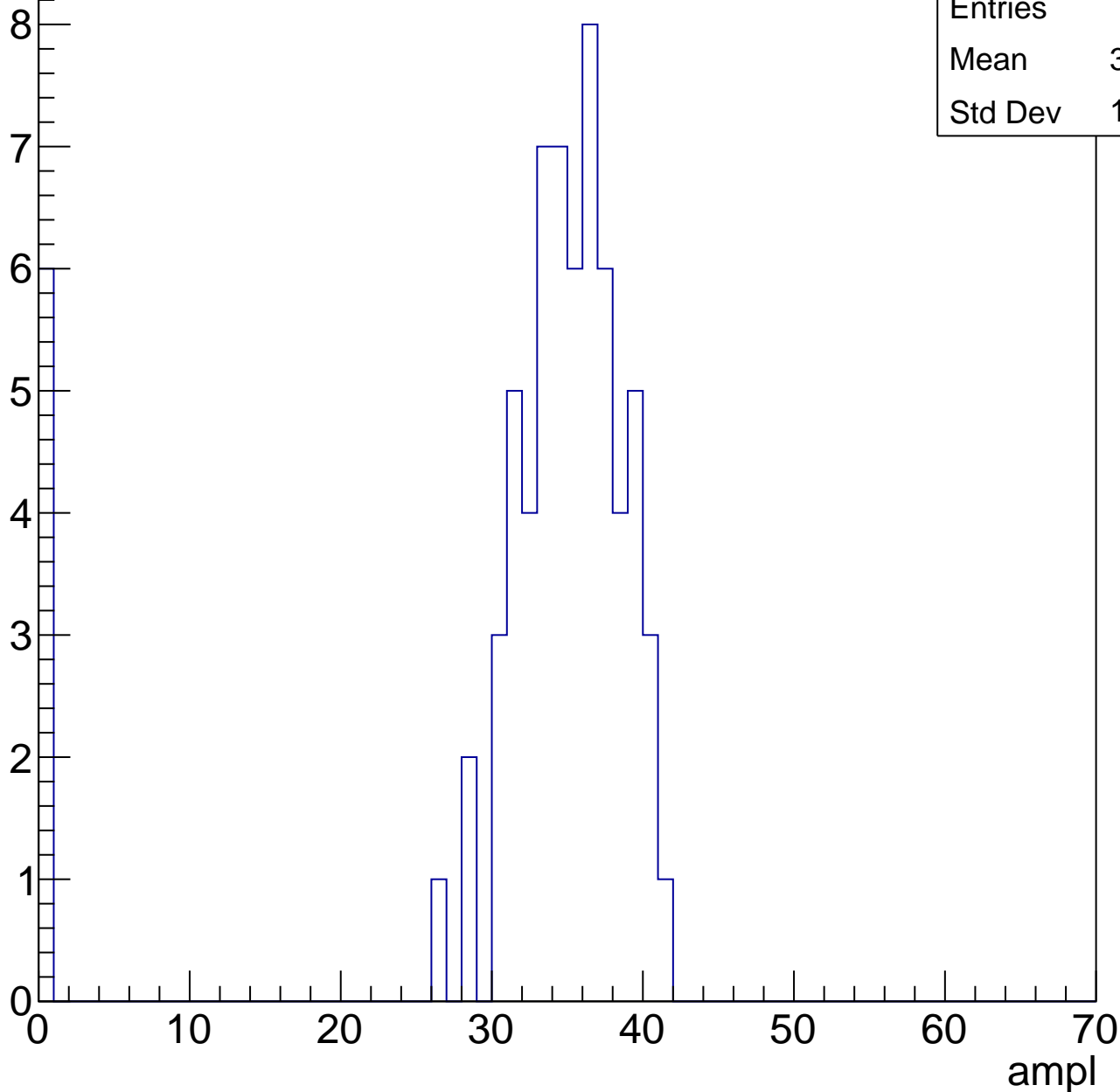


# B1L103S, U4-ch41, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 68    |
| Mean    | 31.65 |
| Std Dev | 10.33 |

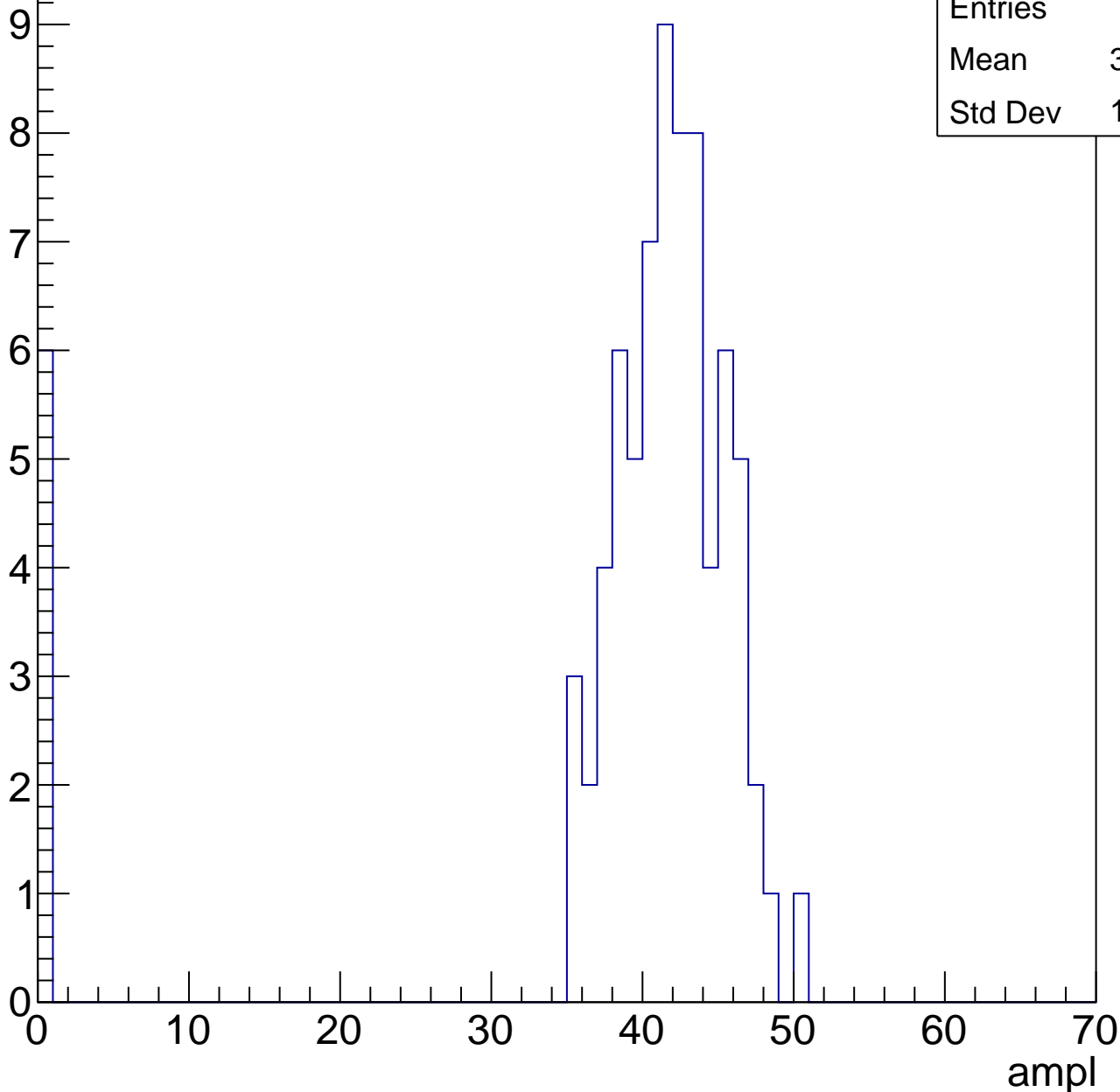


# B1L103S, U4-ch41, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 77    |
| Mean    | 38.25 |
| Std Dev | 11.57 |

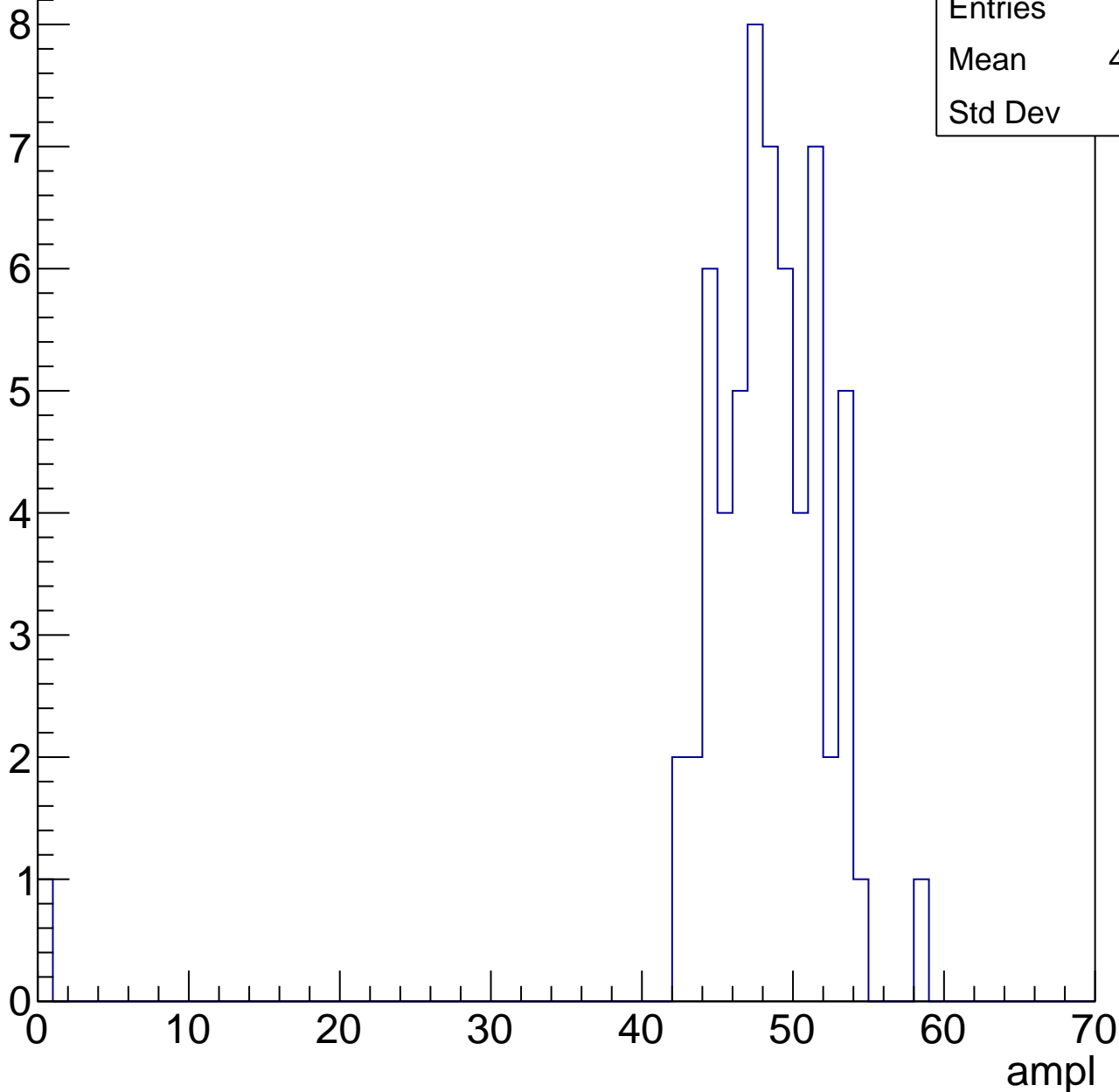


# B1L103S, U4-ch41, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 61    |
| Mean    | 47.34 |
| Std Dev | 6.94  |

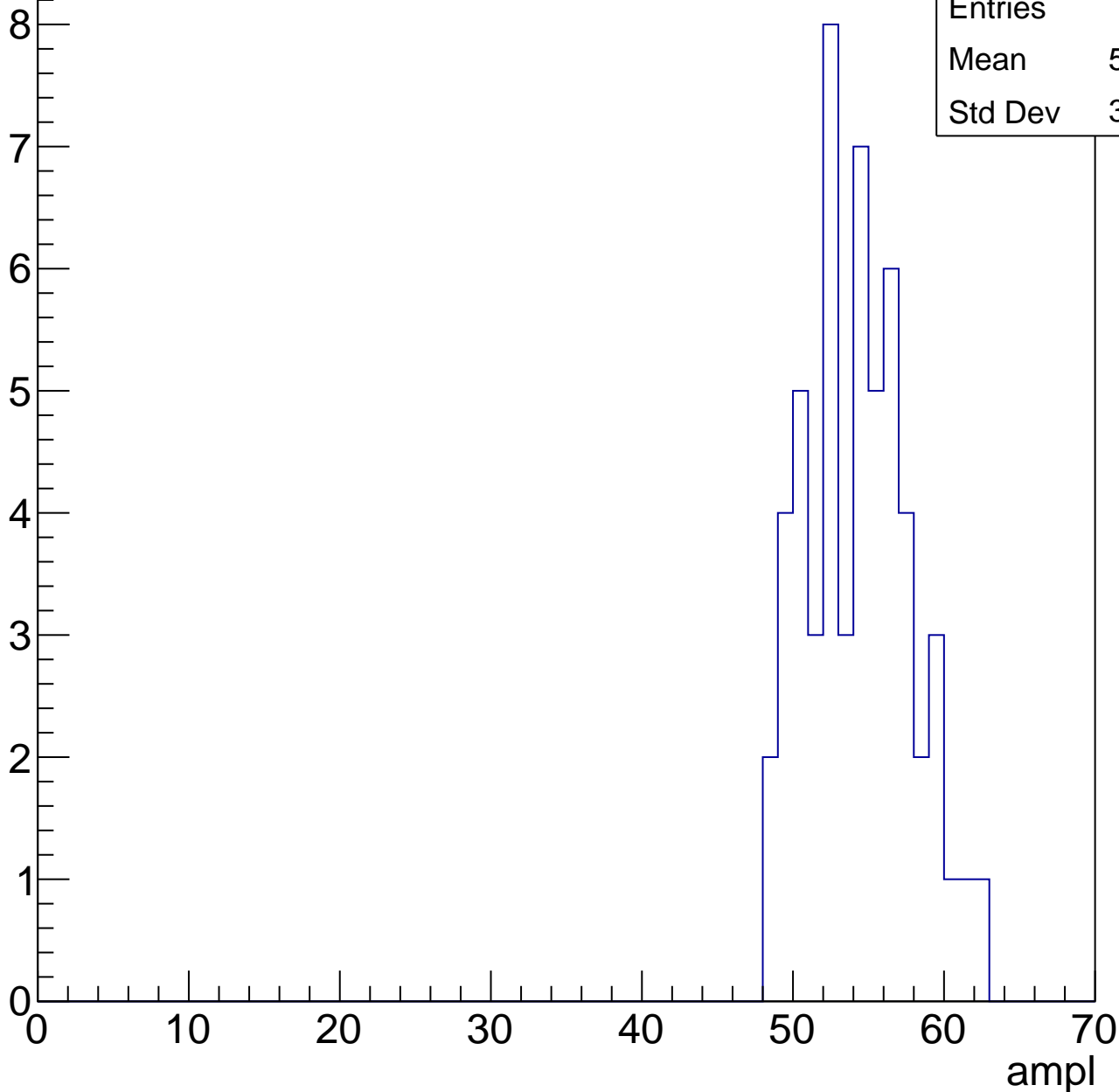


# B1L103S, U4-ch41, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

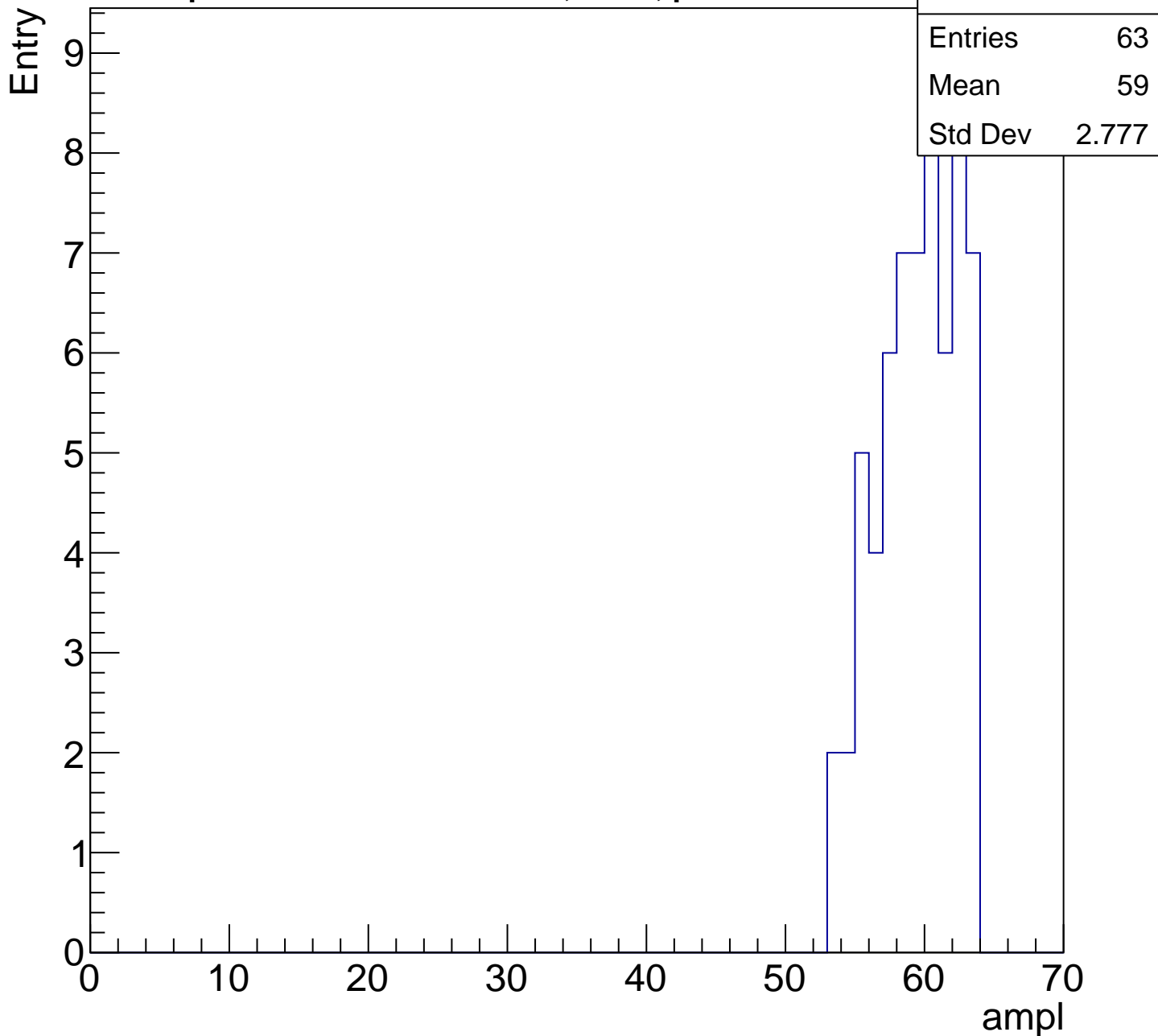
Entry

|         |       |
|---------|-------|
| Entries | 55    |
| Mean    | 53.87 |
| Std Dev | 3.395 |



# B1L103S, U4-ch41, adc5

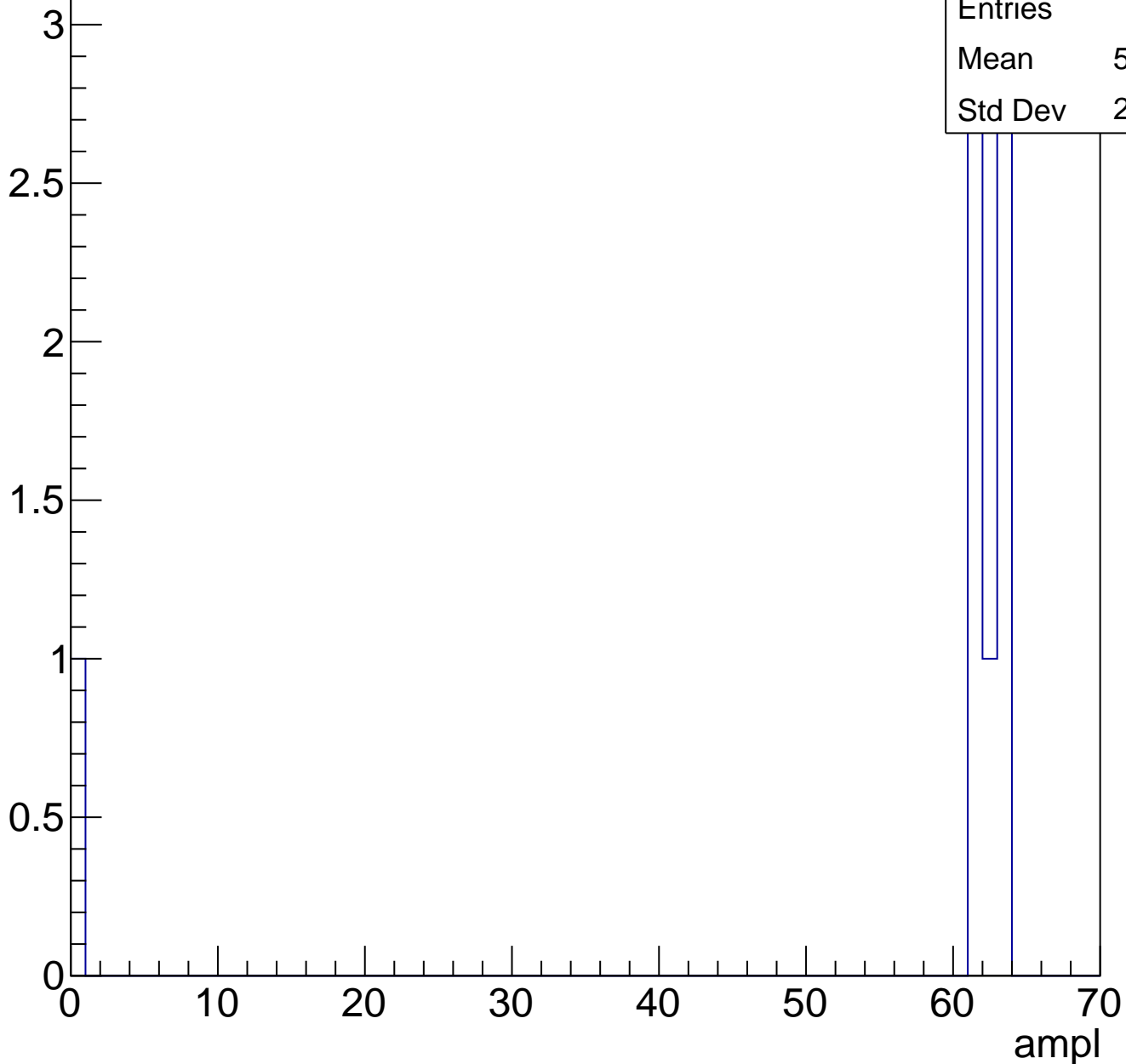
calib\_packv5\_041523\_1651.root, FC#0, port C2



# B1L103S, U4-ch41, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U4-ch41, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U4-ch42, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 84    |
| Mean    | 22.88 |
| Std Dev | 10.4  |

Entry

12

10

8

6

4

2

0

0

10

20

30

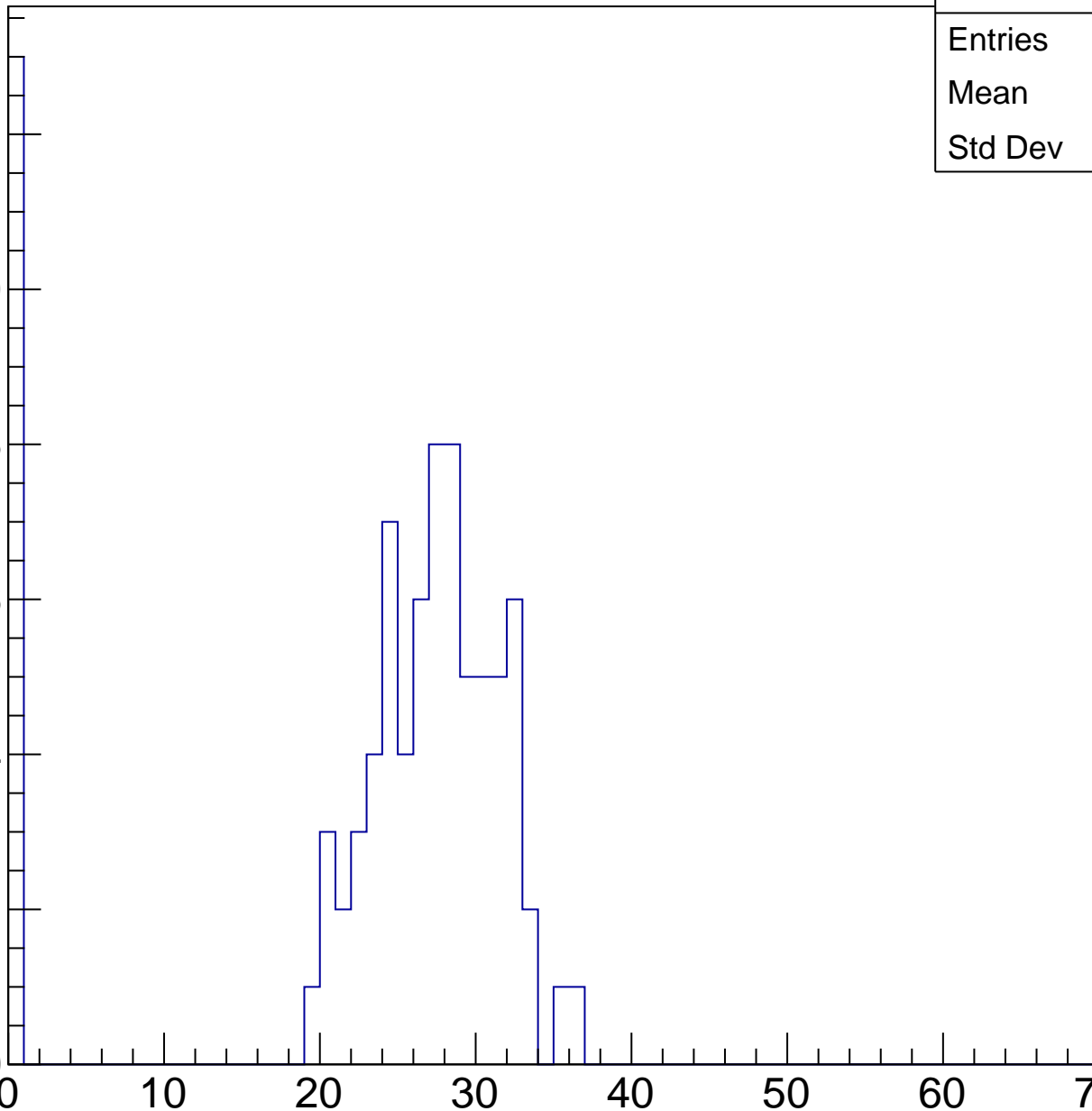
40

50

60

70

ampl

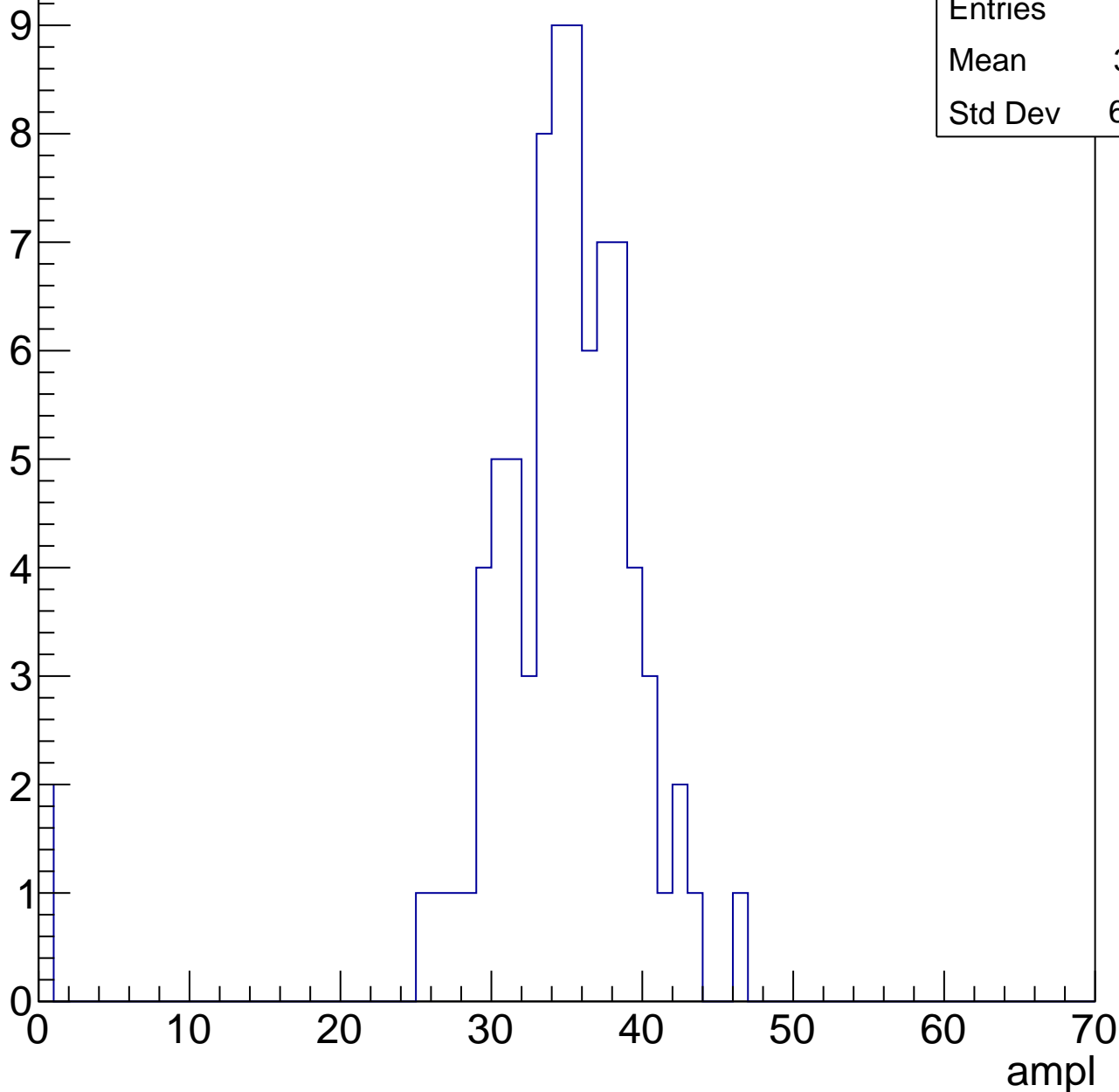


# B1L103S, U4-ch42, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

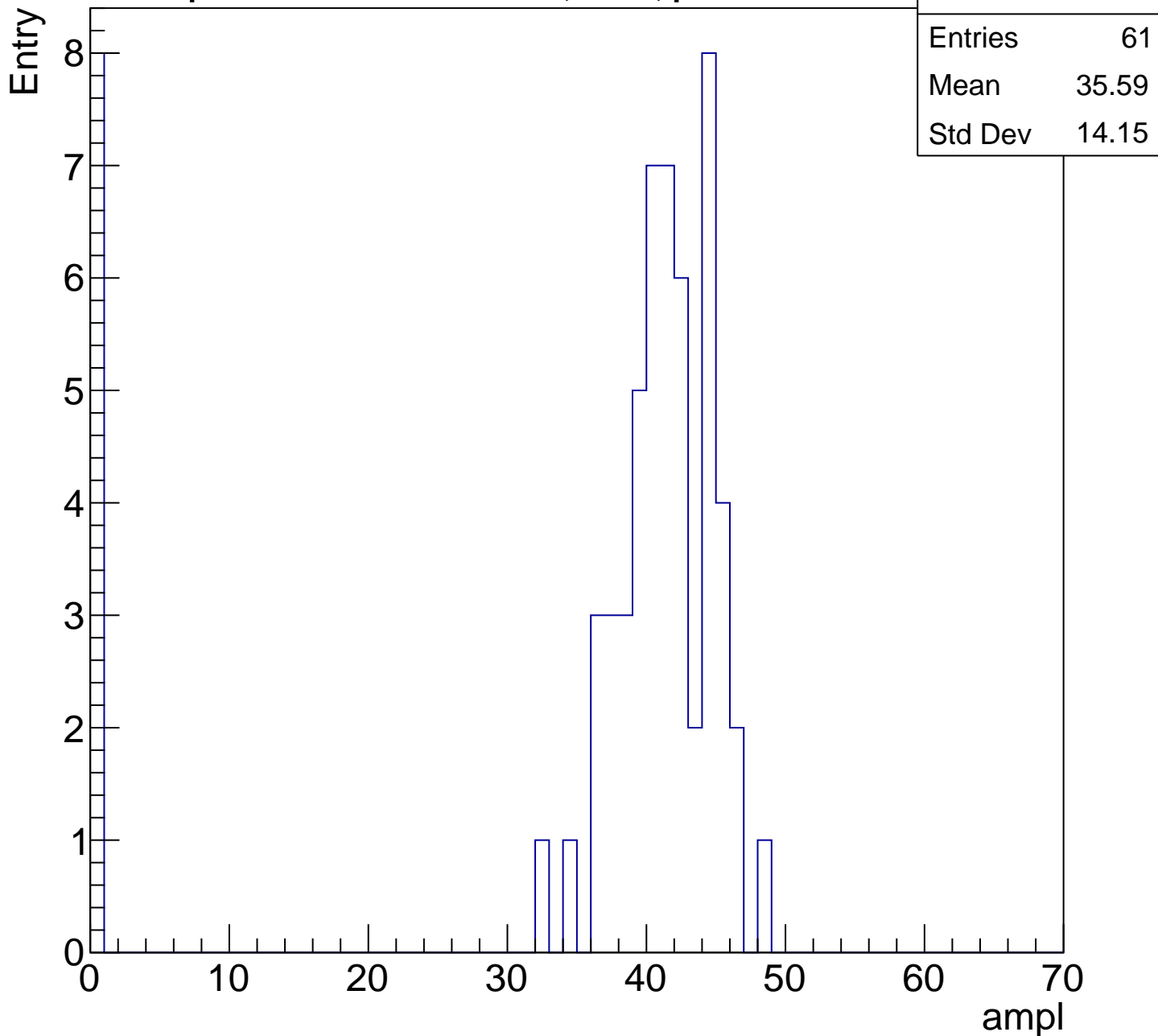
Entry

|         |       |
|---------|-------|
| Entries | 81    |
| Mean    | 33.81 |
| Std Dev | 6.669 |



# B1L103S, U4-ch42, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

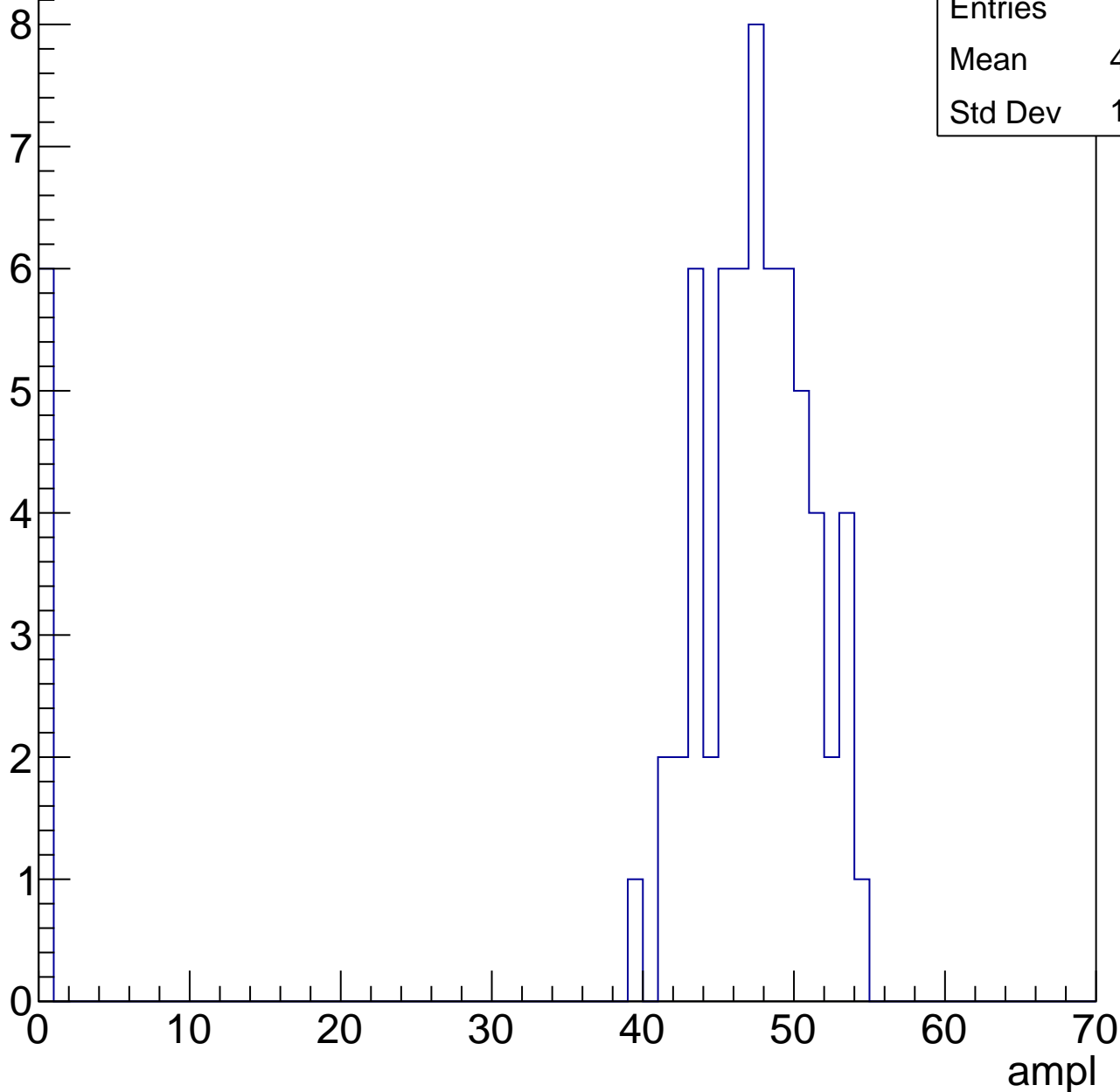


# B1L103S, U4-ch42, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 67    |
| Mean    | 42.97 |
| Std Dev | 13.86 |

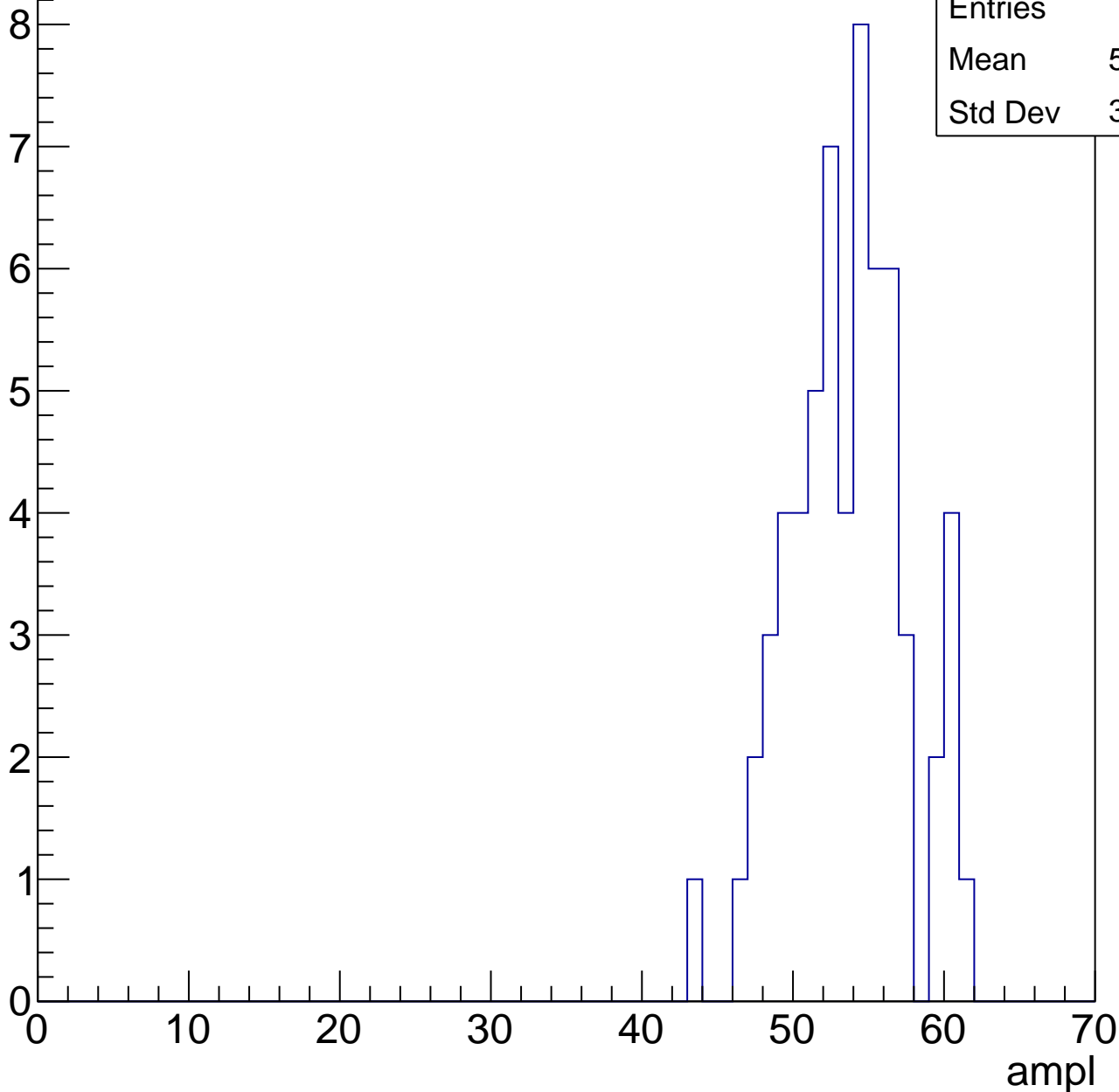


# B1L103S, U4-ch42, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

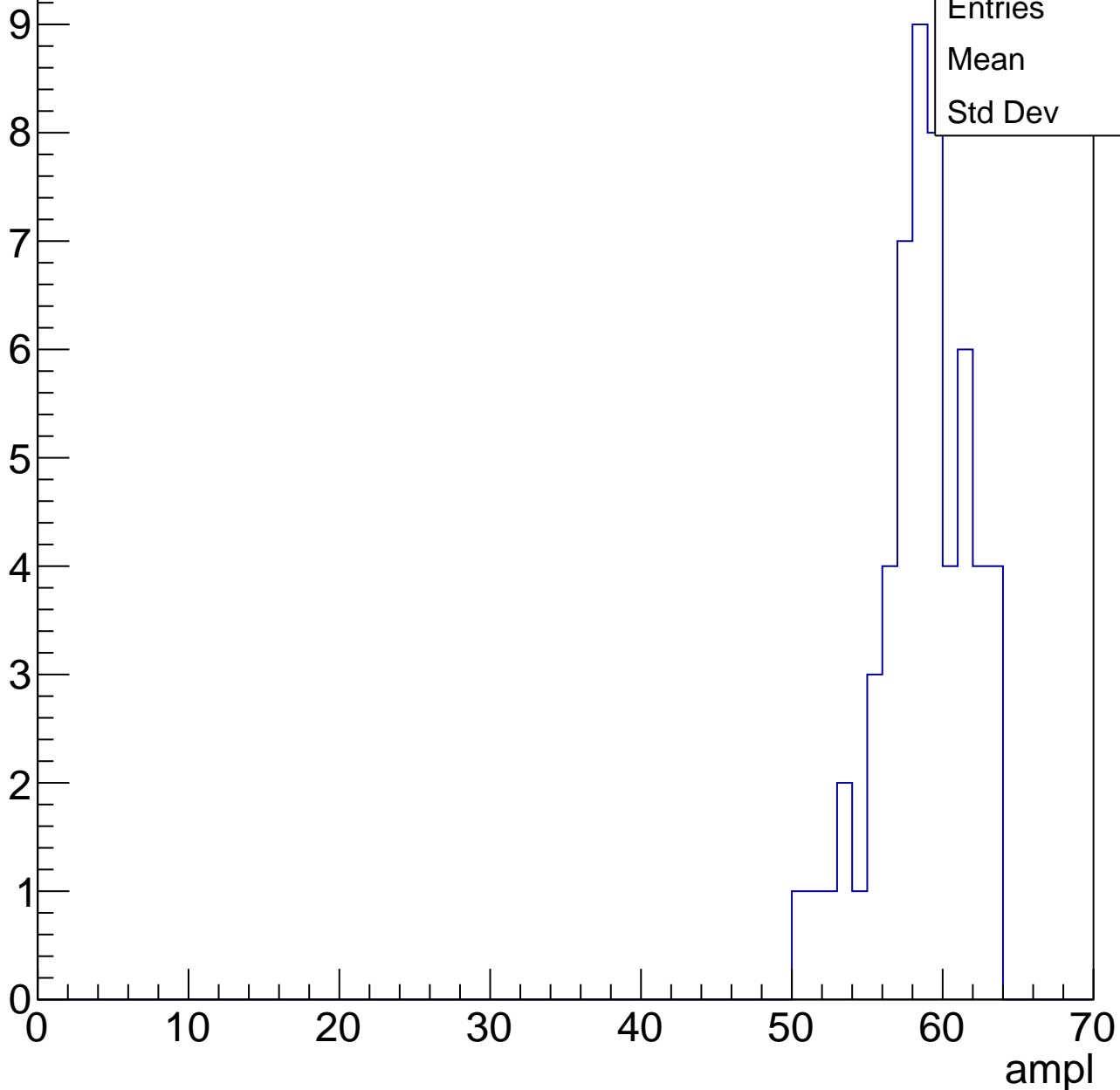
|         |       |
|---------|-------|
| Entries | 61    |
| Mean    | 53.15 |
| Std Dev | 3.815 |



# B1L103S, U4-ch42, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

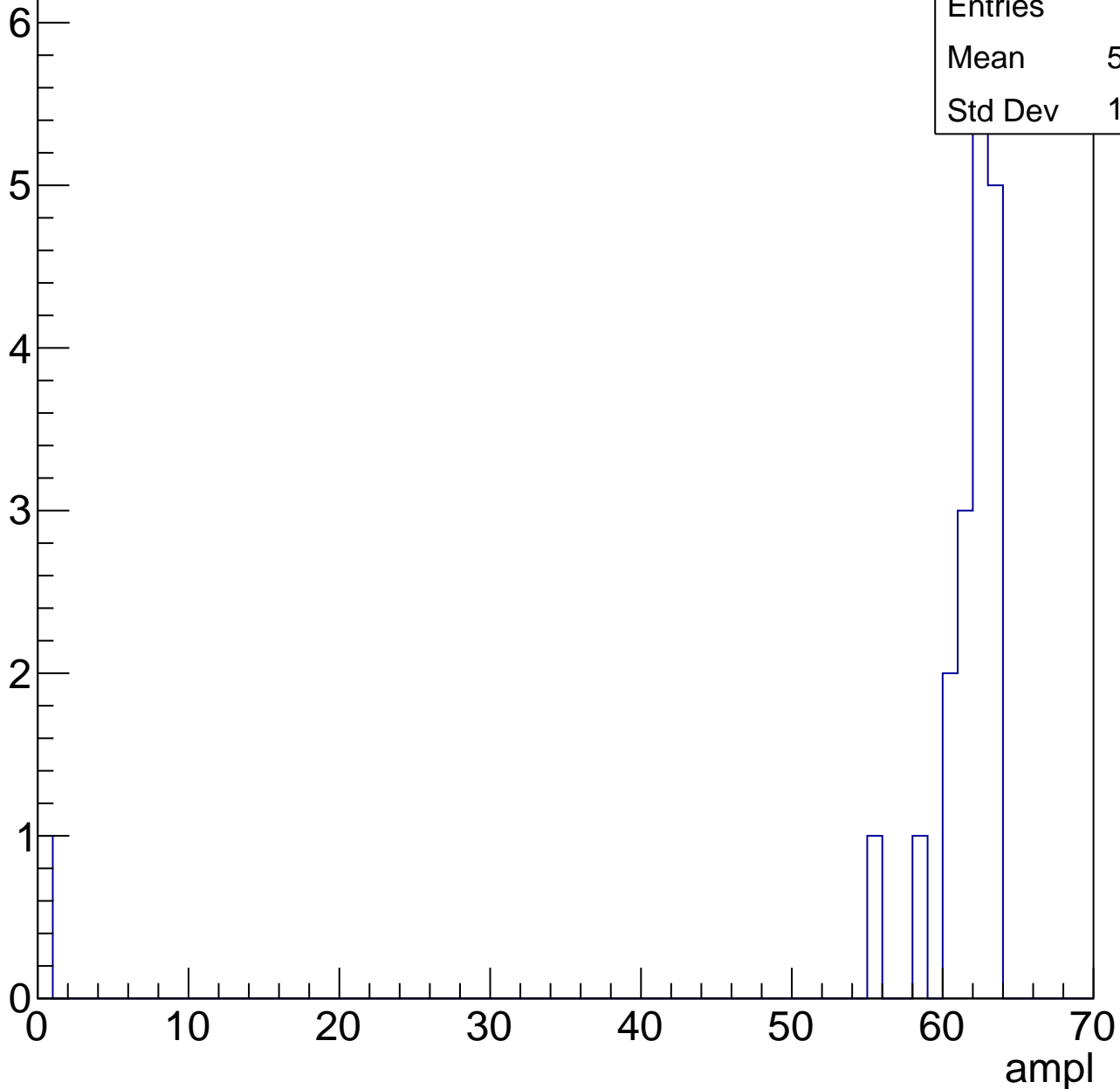


# B1L103S, U4-ch42, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 19    |
| Mean    | 58.05 |
| Std Dev | 13.82 |





# B1L103S, U4-ch42, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 20    |
| Mean    | 3.15  |
| Std Dev | 13.73 |

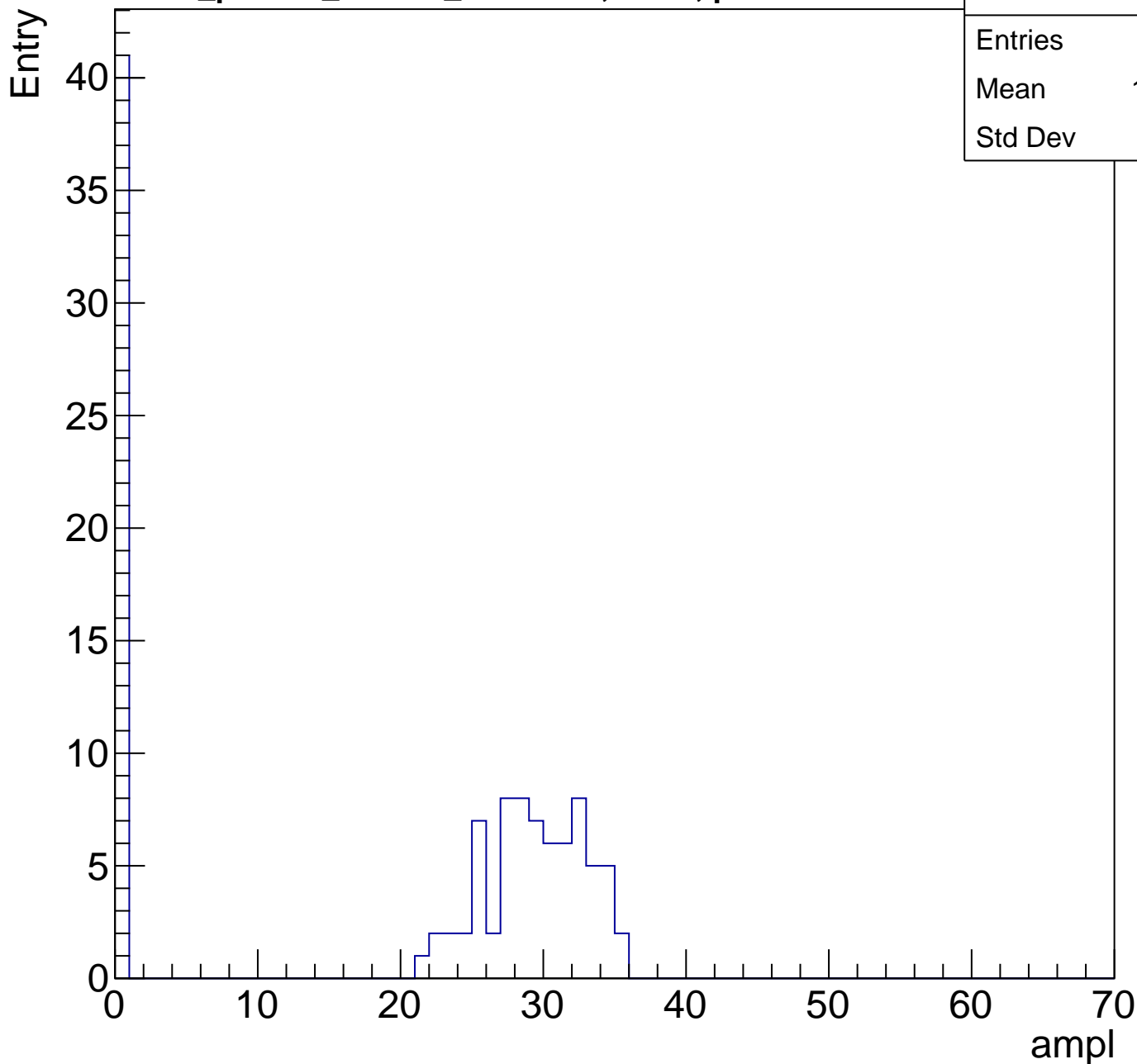
Entry



# B1L103S, U4-ch43, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 112   |
| Mean    | 18.36 |
| Std Dev | 14.21 |

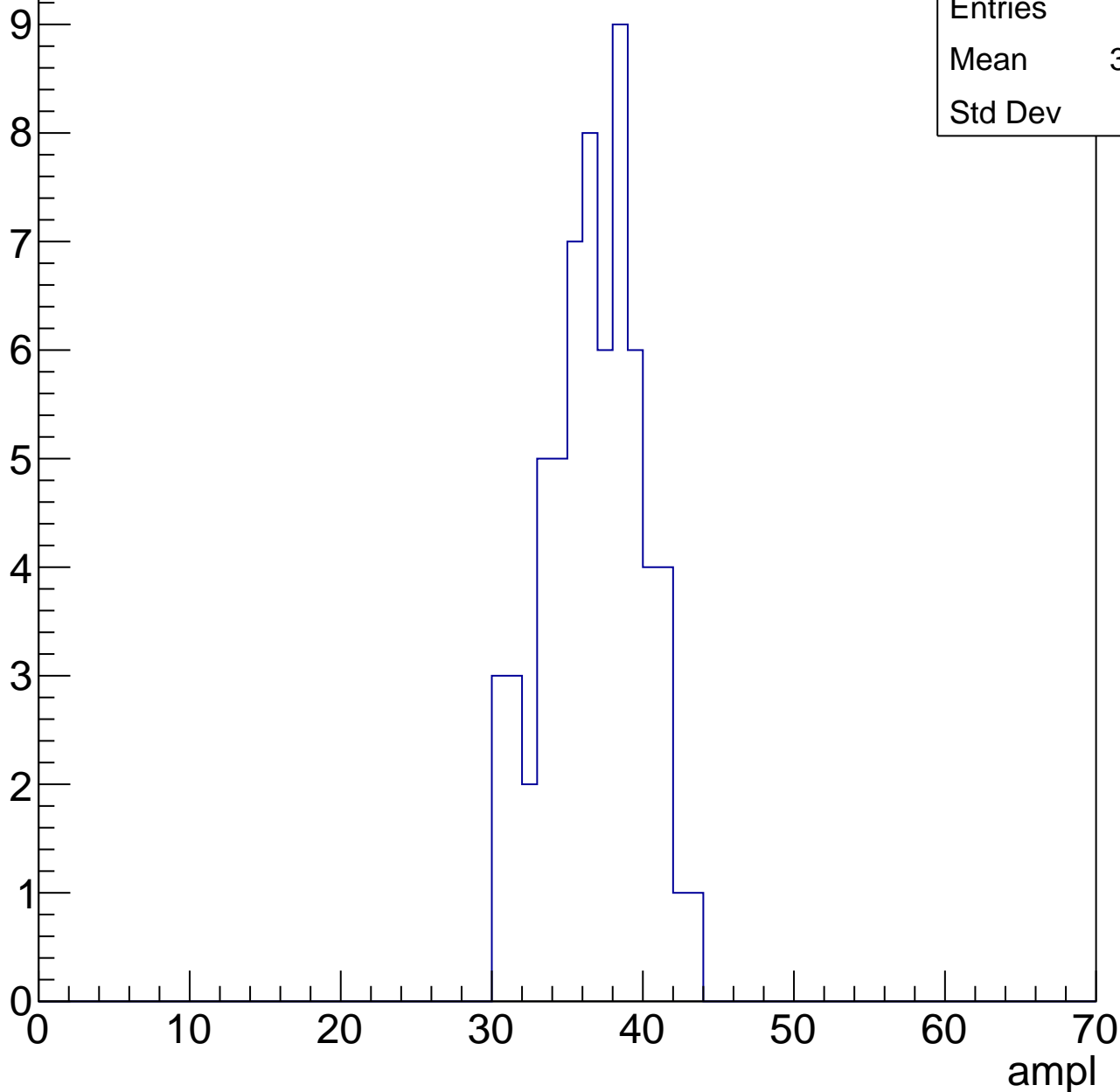


# B1L103S, U4-ch43, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 64    |
| Mean    | 36.28 |
| Std Dev | 3.13  |

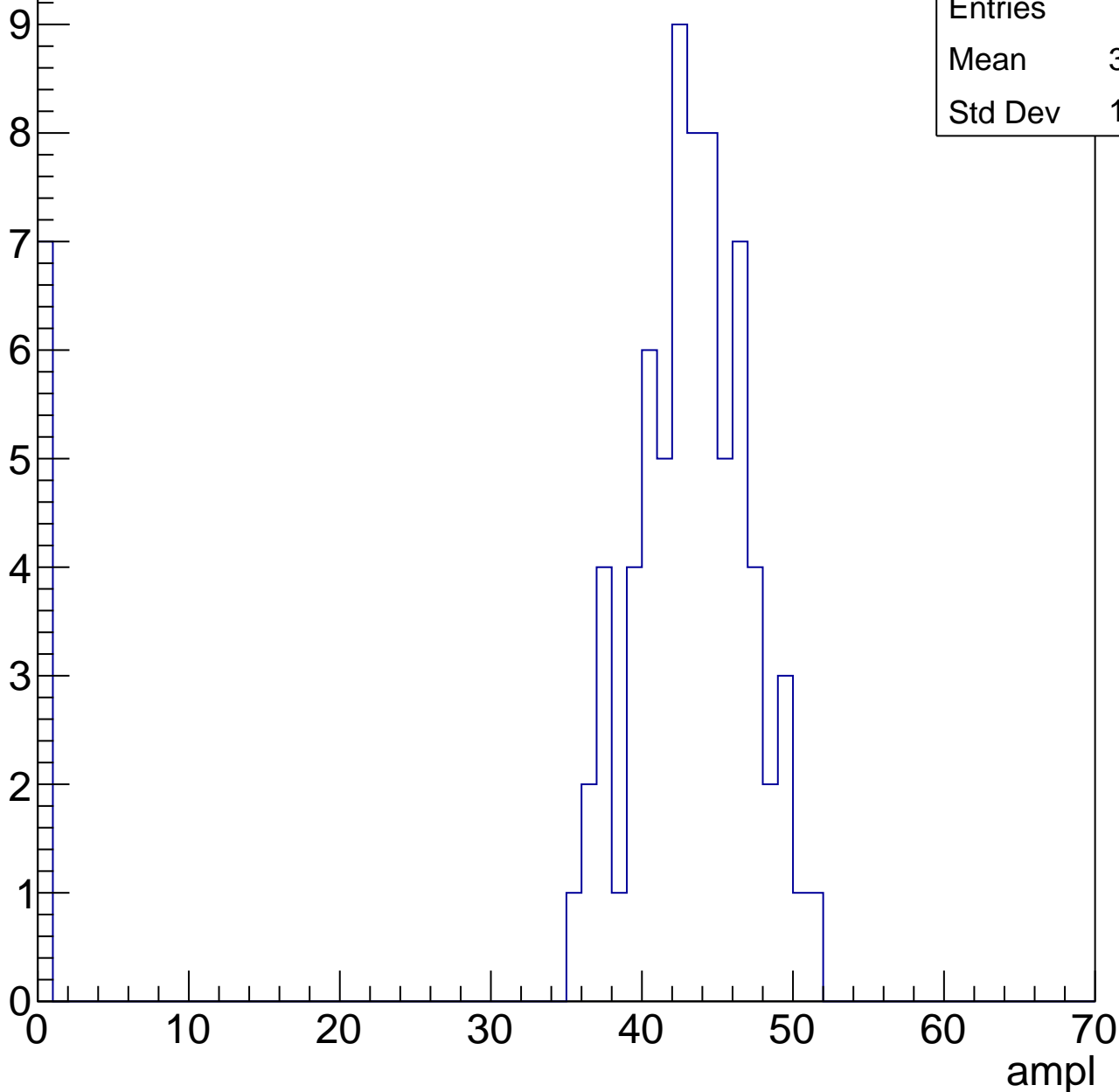


# B1L103S, U4-ch43, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 78    |
| Mean    | 39.06 |
| Std Dev | 12.73 |



# B1L103S, U4-ch43, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 82    |
| Mean    | 43.11 |
| Std Dev | 17.26 |

Entry

10

8

6

4

2

0

0

10

20

30

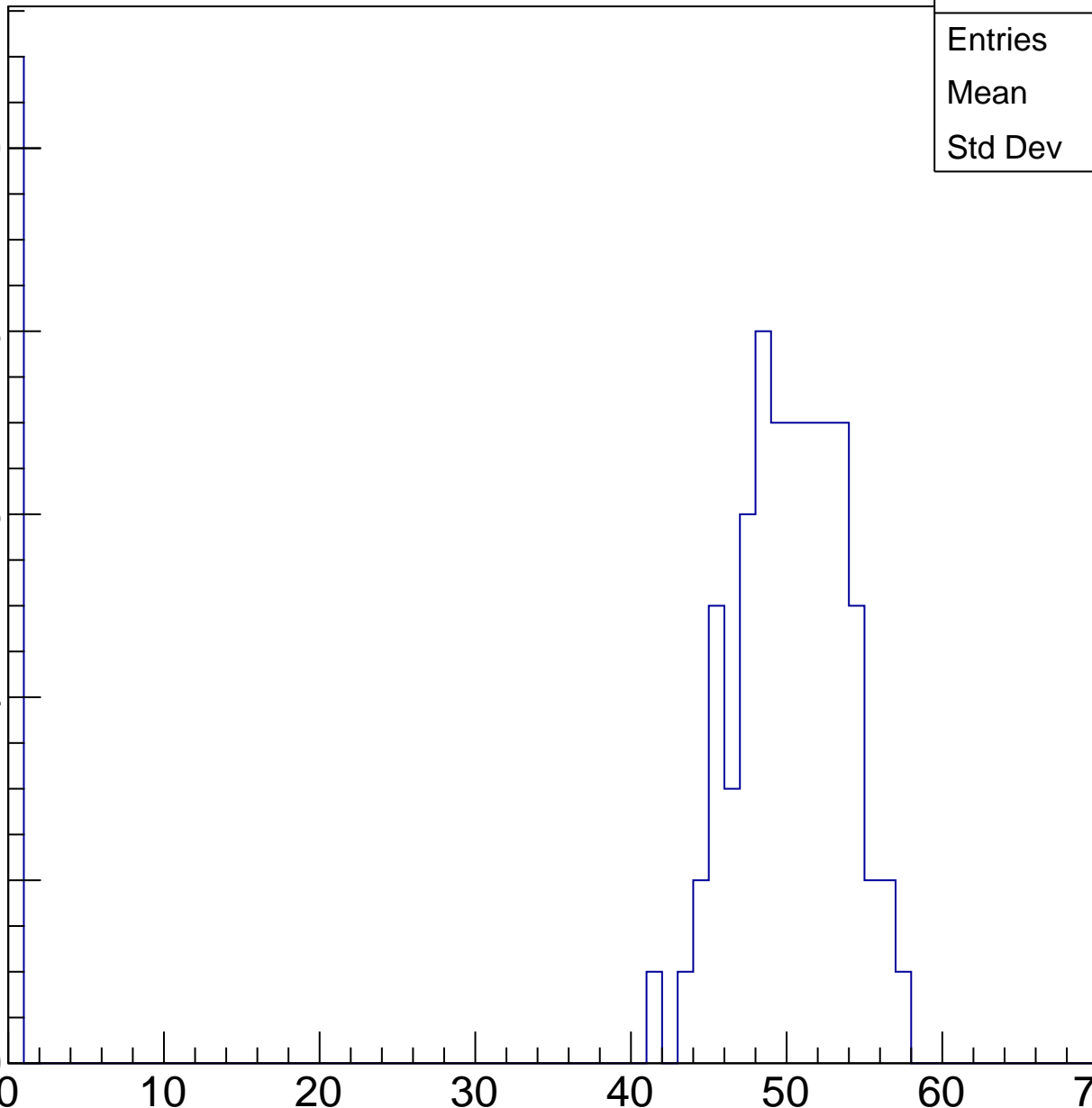
40

50

60

70

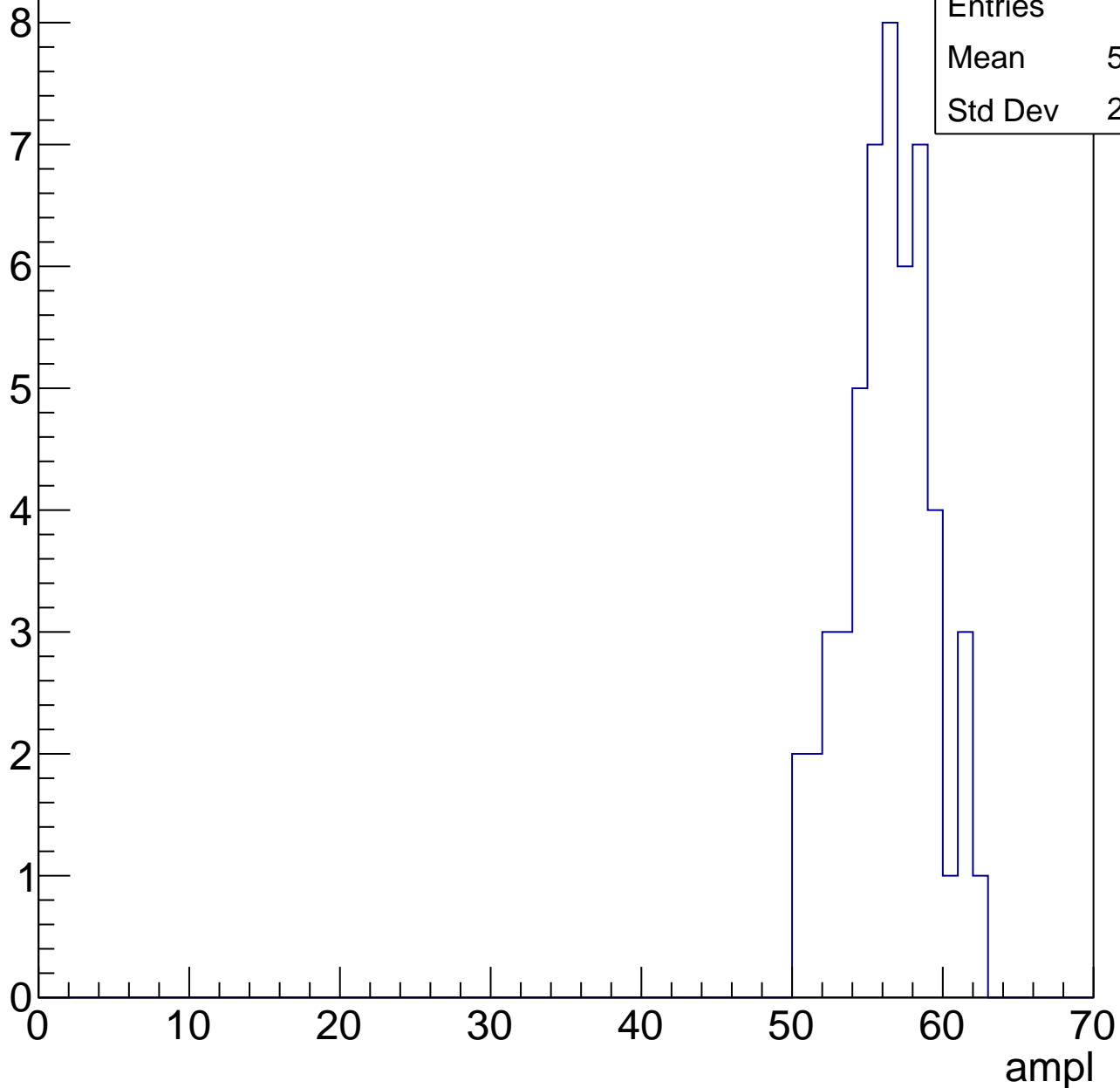
ampl



# B1L103S, U4-ch43, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U4-ch43, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

|         |       |
|---------|-------|
| Entries | 41    |
| Mean    | 58.93 |
| Std Dev | 9.524 |

ampl

0 10 20 30 40 50 60 70

1

2

3

4

5

6

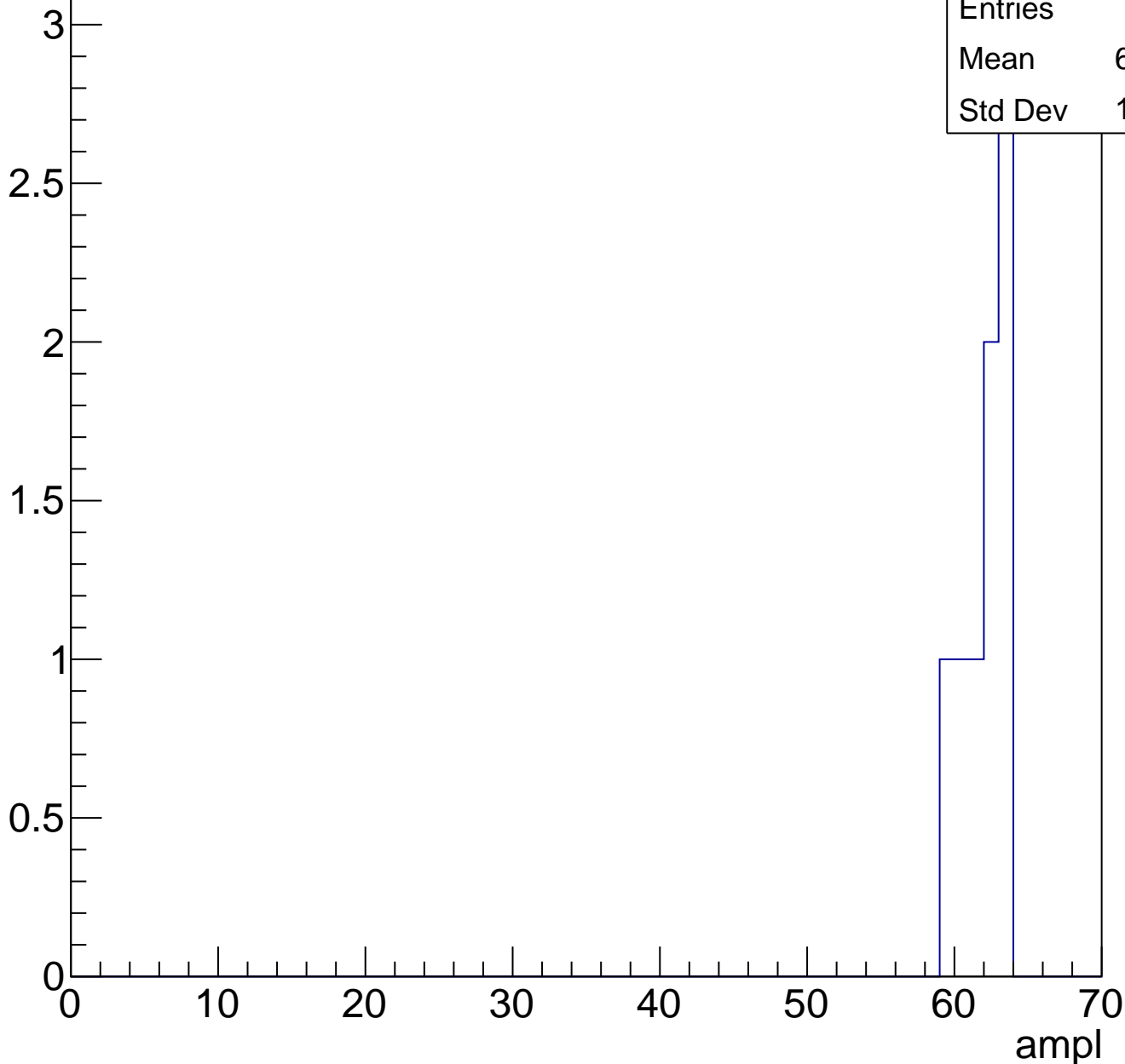
7

8

# B1L103S, U4-ch43, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U4-ch43, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

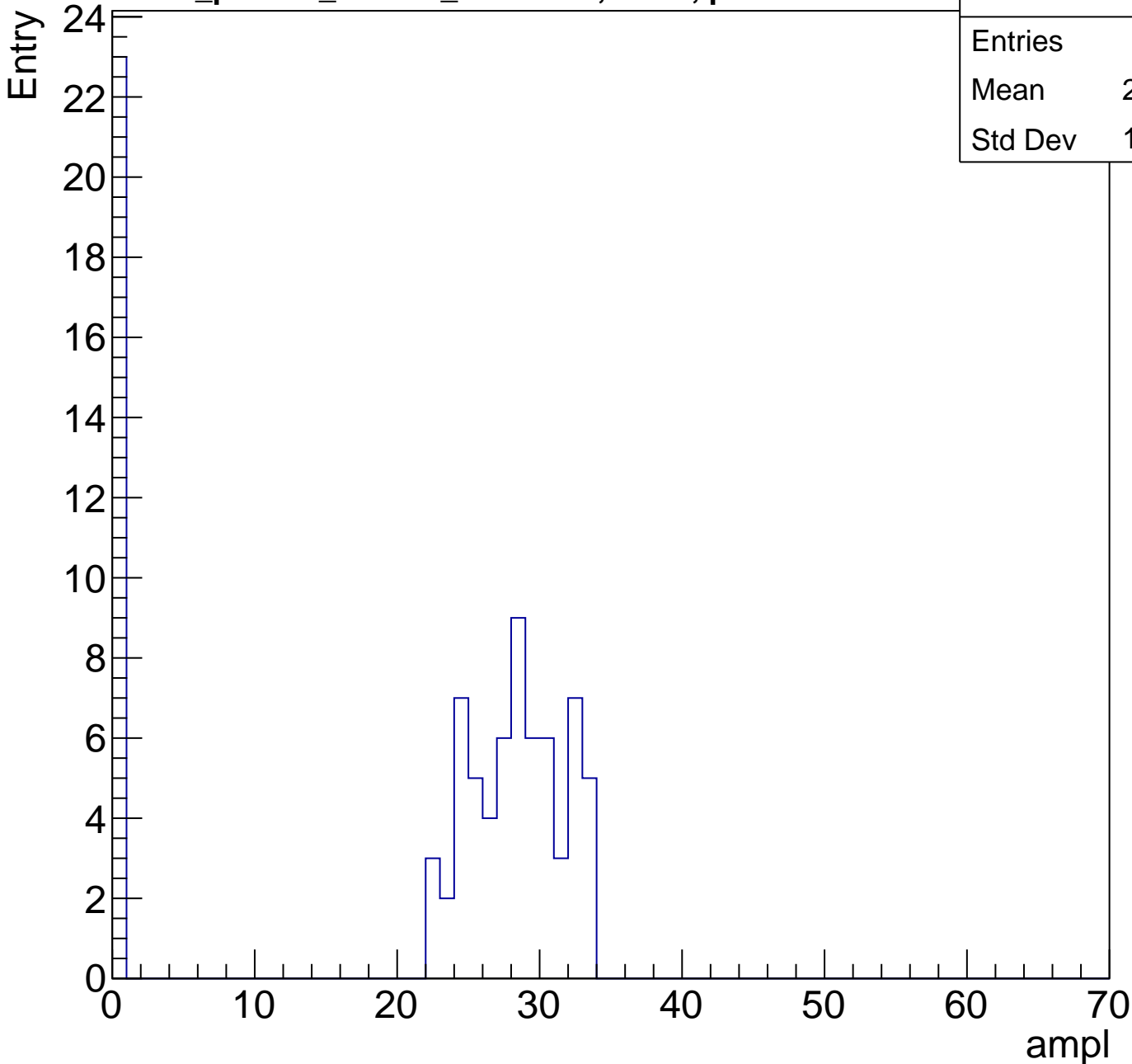
|         |    |
|---------|----|
| Entries | 19 |
| Mean    | 0  |
| Std Dev | 0  |

ampl

# B1L103S, U4-ch44, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 86    |
| Mean    | 20.45 |
| Std Dev | 12.65 |

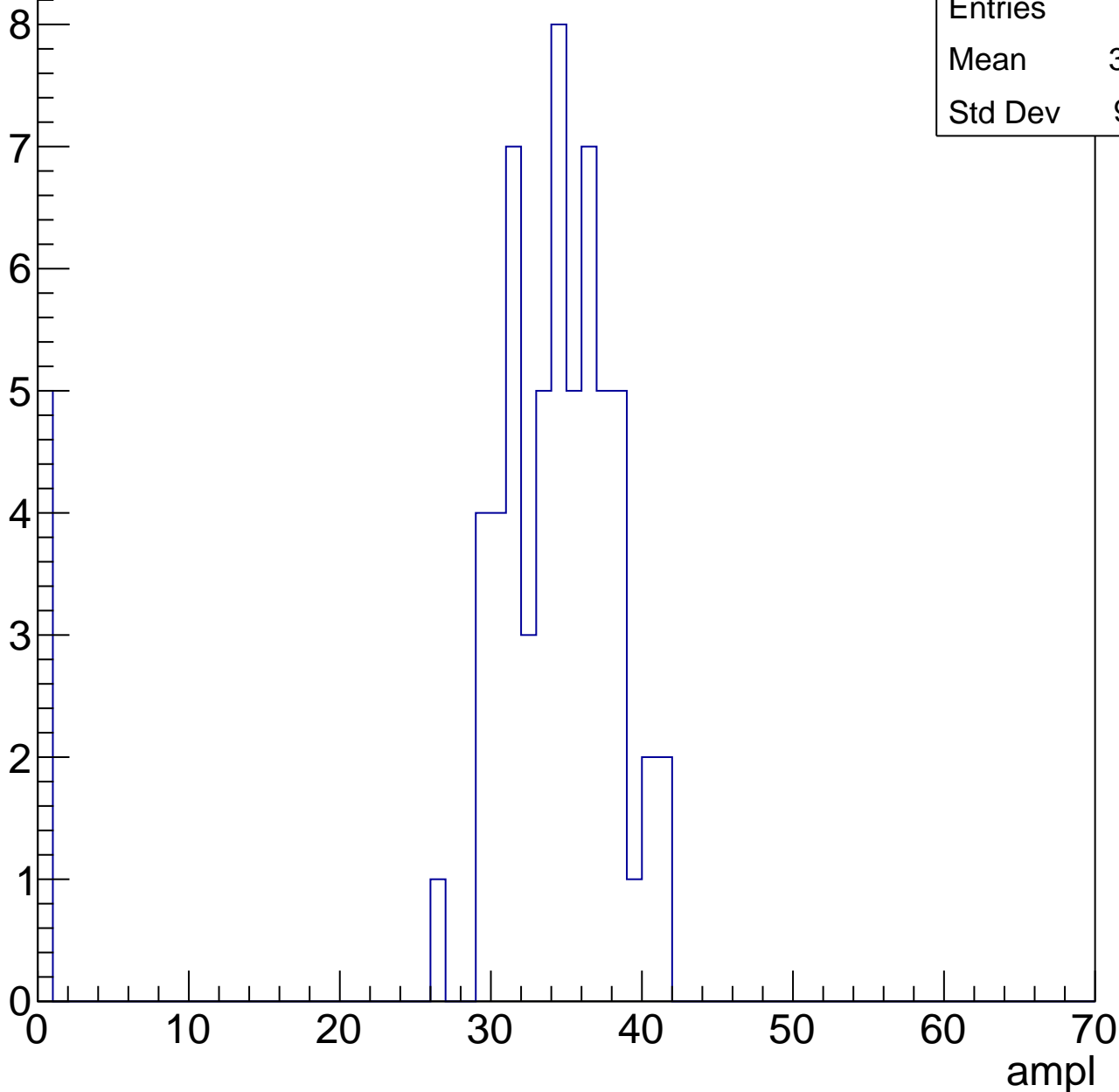


# B1L103S, U4-ch44, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 64    |
| Mean    | 31.48 |
| Std Dev | 9.711 |



# B1L103S, U4-ch44, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 92    |
| Mean    | 35.24 |
| Std Dev | 14.71 |

Entry

12

10

8

6

4

2

0

0

10

20

30

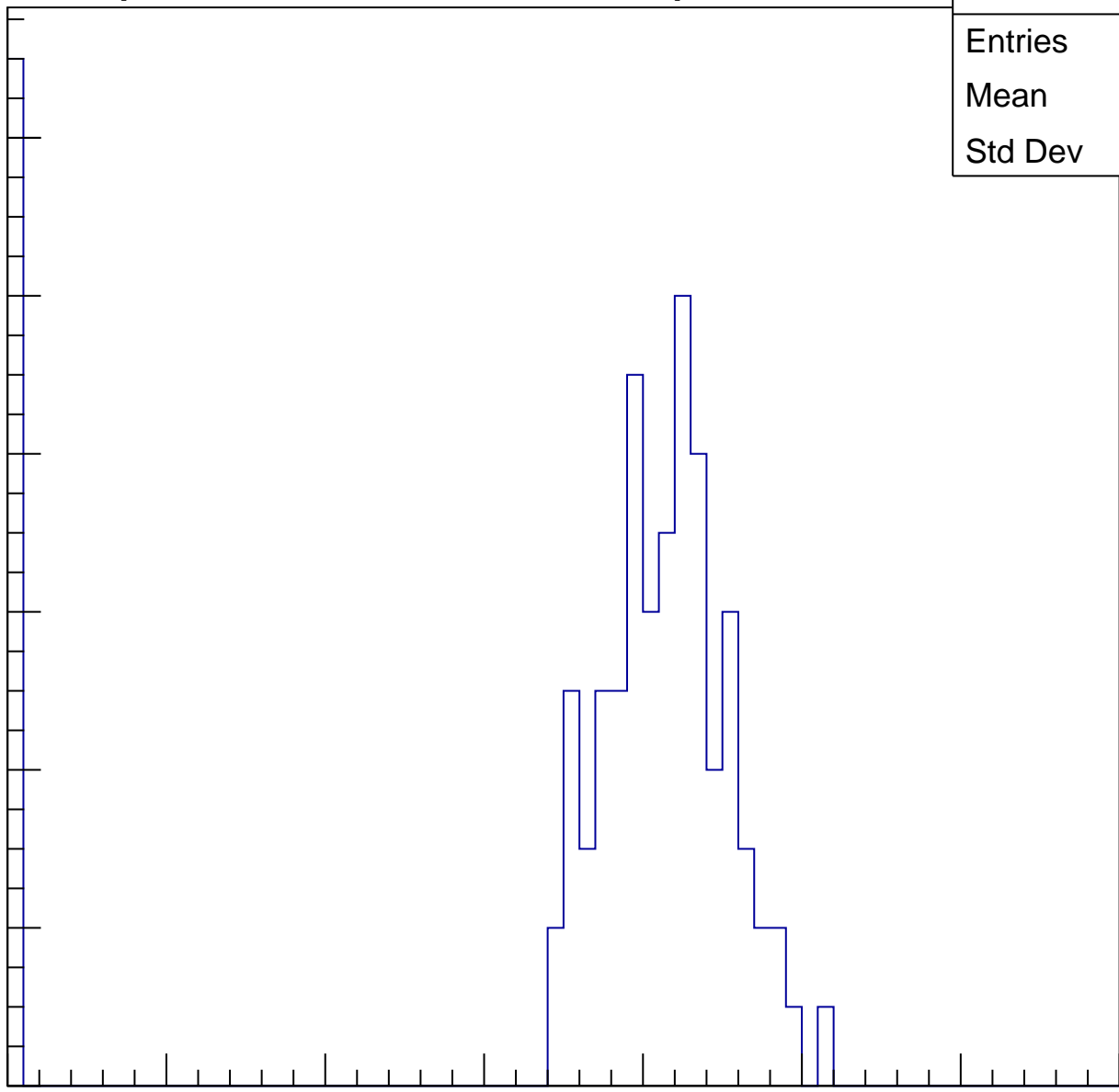
40

50

60

70

ampl

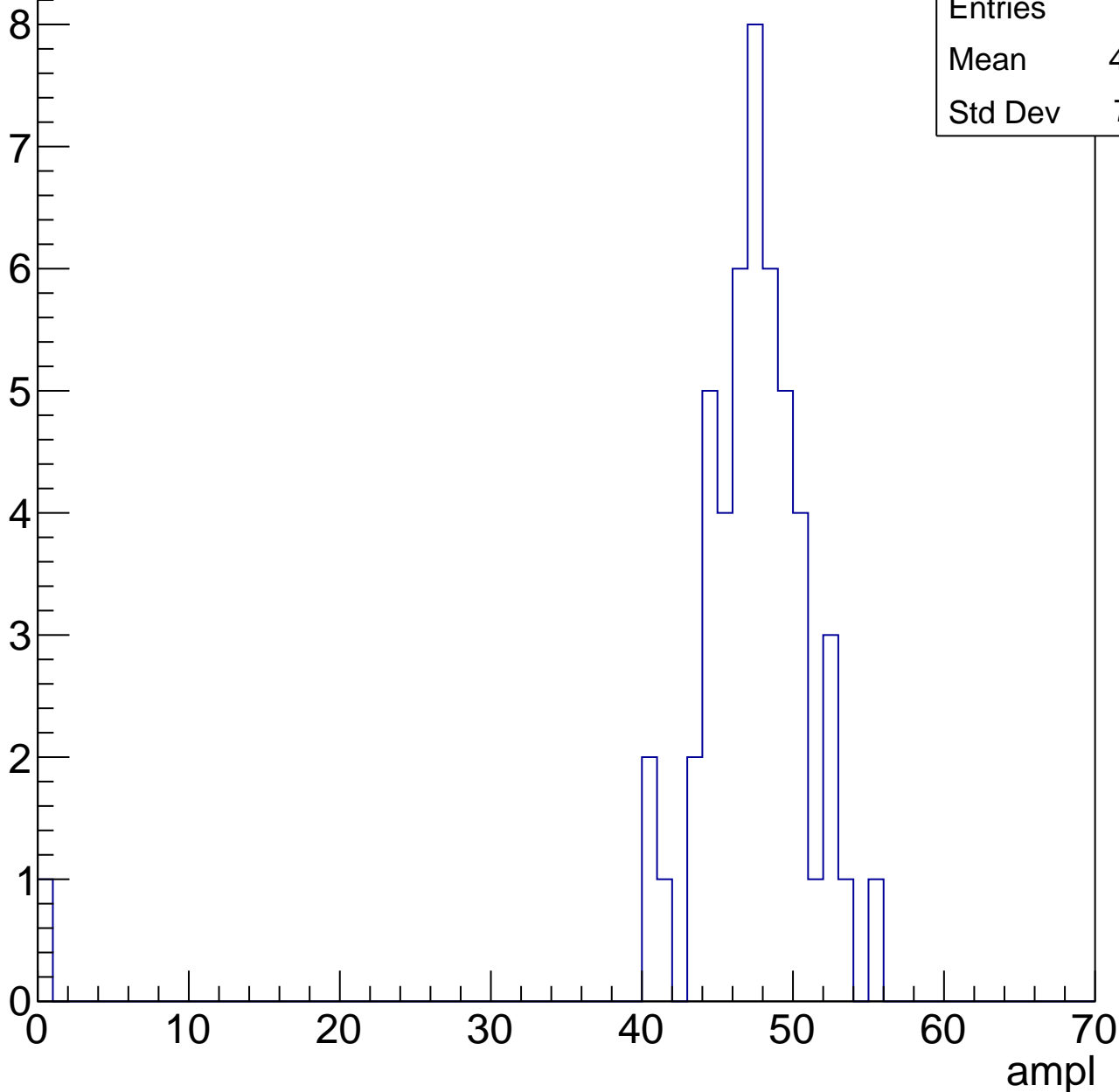


# B1L103S, U4-ch44, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

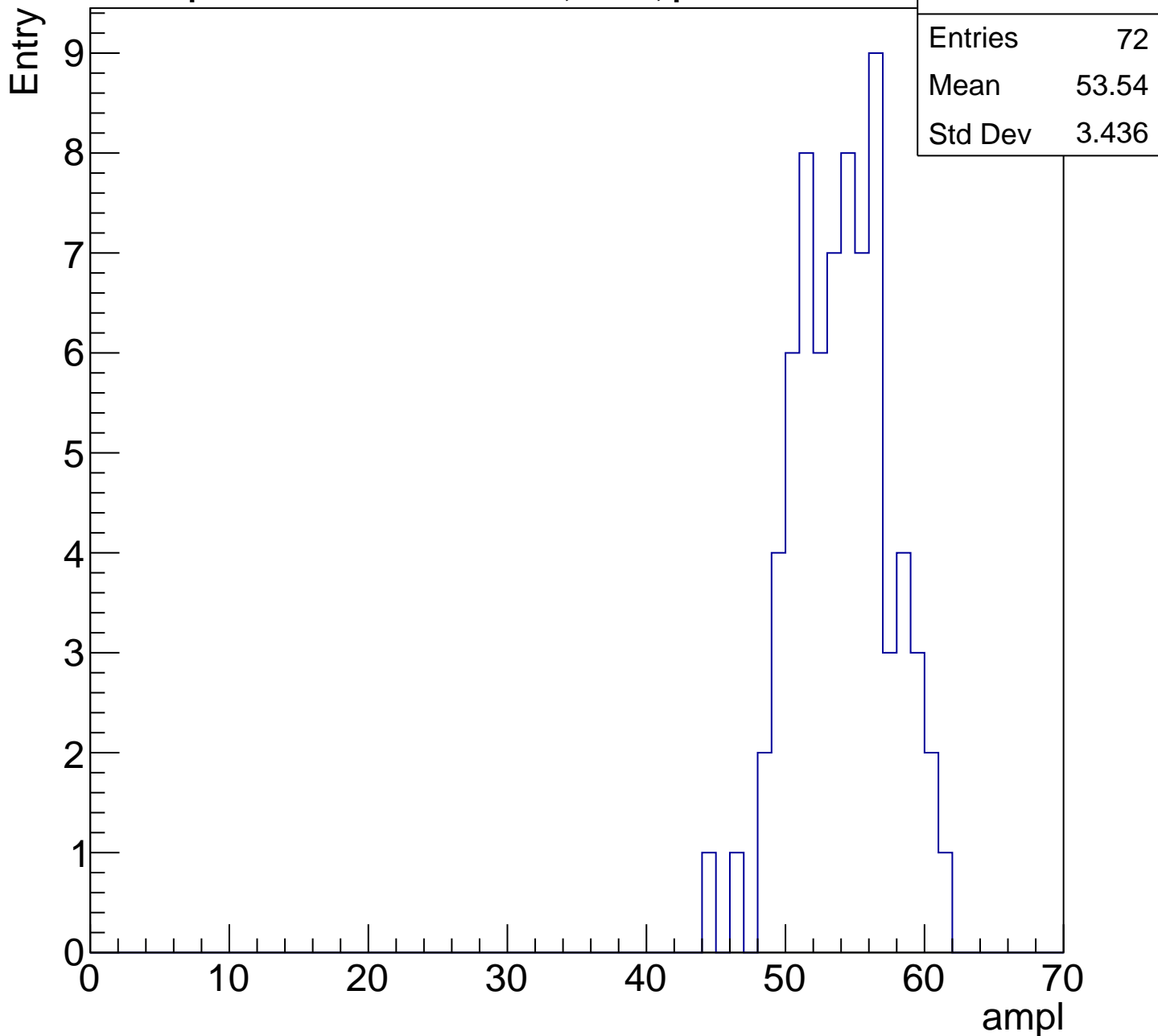
Entry

|         |       |
|---------|-------|
| Entries | 50    |
| Mean    | 46.14 |
| Std Dev | 7.291 |



# B1L103S, U4-ch44, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2



# B1L103S, U4-ch44, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

7

6

5

4

3

2

1

0

0

10

20

30

40

50

60

70

ampl

|         |       |
|---------|-------|
| Entries | 50    |
| Mean    | 59.06 |
| Std Dev | 2.908 |

2

1

0

0

1

2

1

0

0

1

2

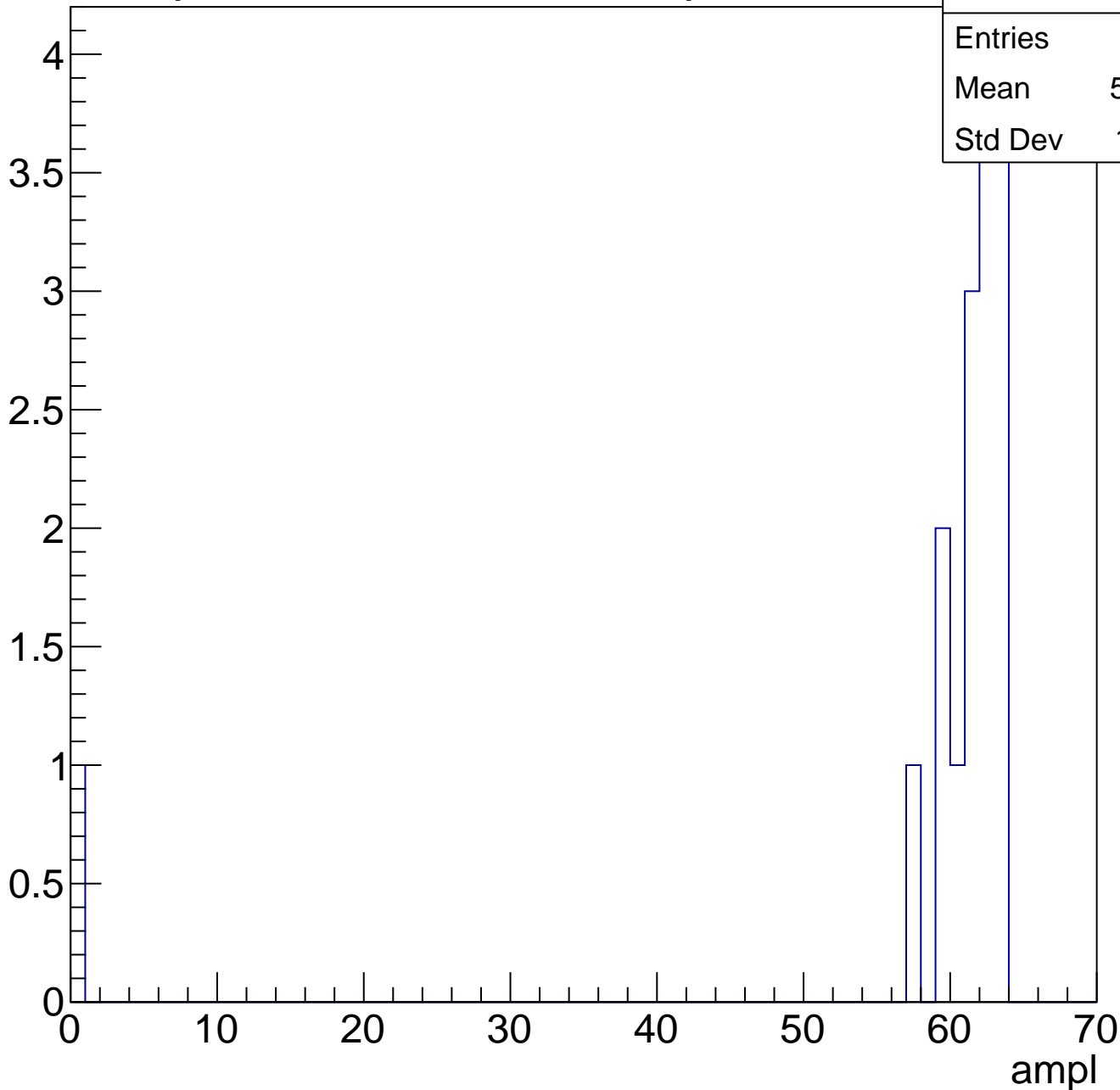
1

0

# B1L103S, U4-ch44, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U4-ch44, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

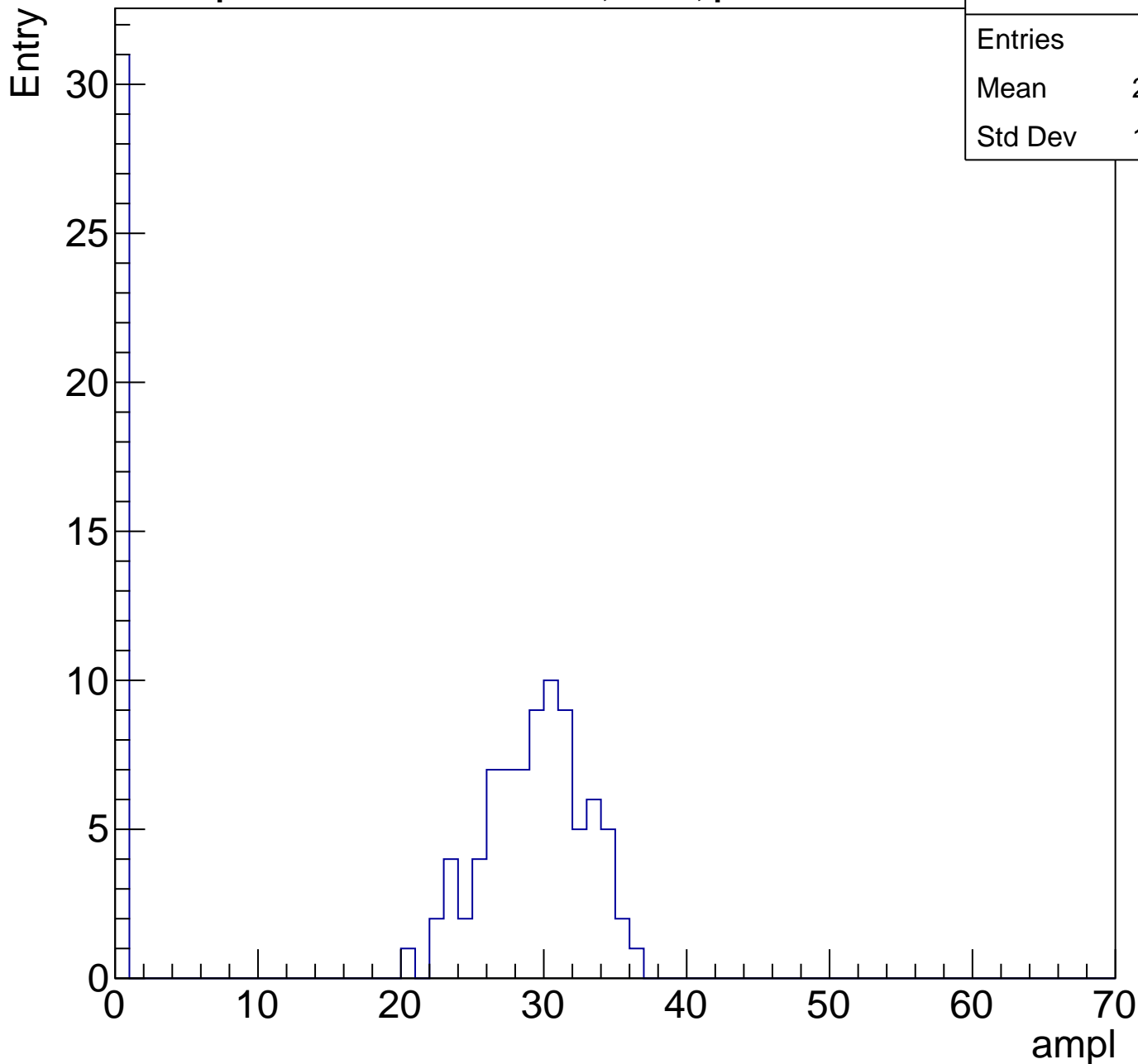
|         |    |
|---------|----|
| Entries | 19 |
| Mean    | 0  |
| Std Dev | 0  |

ampl

# B1L103S, U4-ch45, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 112   |
| Mean    | 20.94 |
| Std Dev | 13.28 |

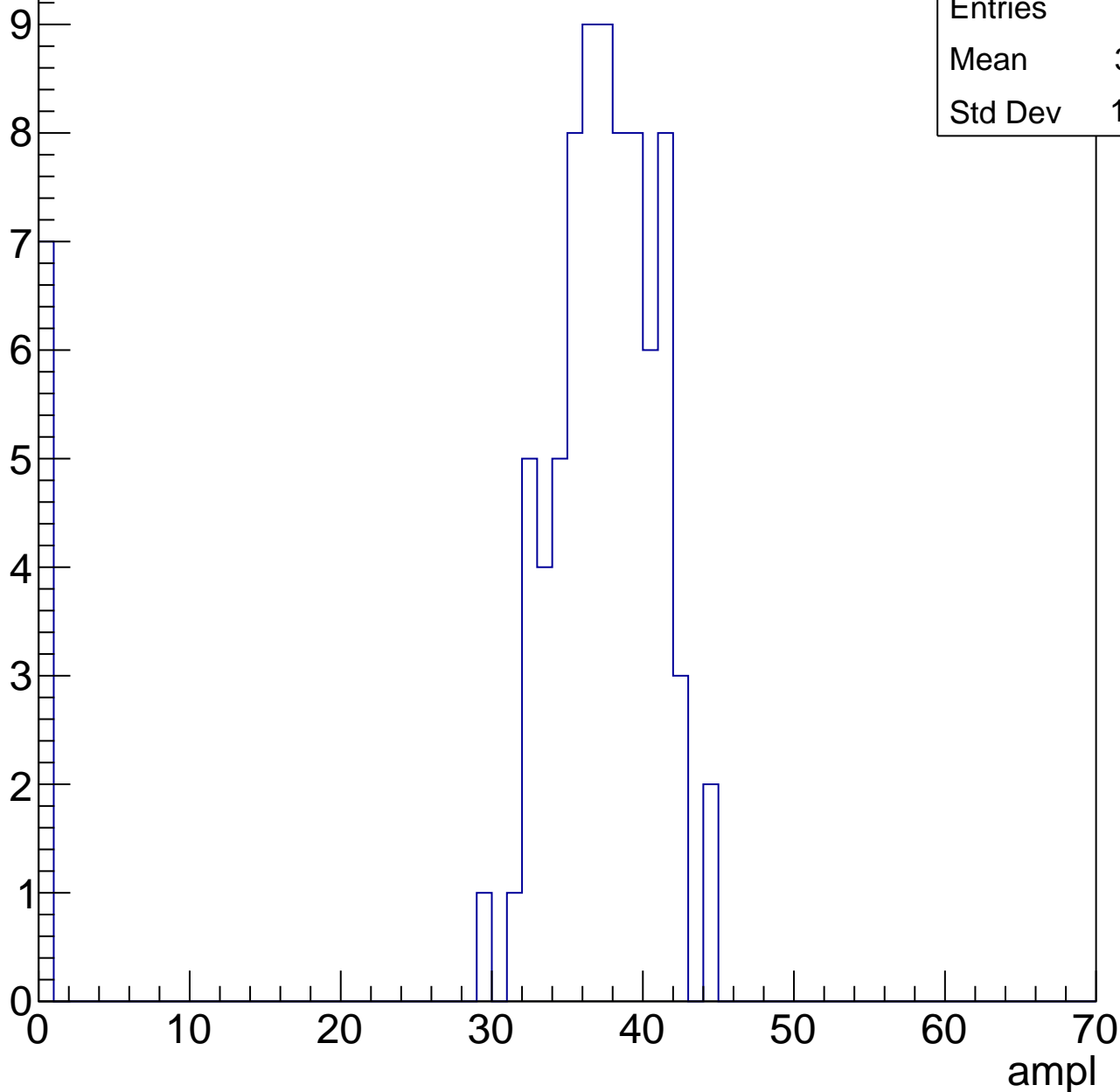


# B1L103S, U4-ch45, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 84    |
| Mean    | 34.01 |
| Std Dev | 10.69 |



# B1L103S, U4-ch45, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 74    |
| Mean    | 37.62 |
| Std Dev | 15.98 |

Entry

10

8

6

4

2

0

0

10

20

30

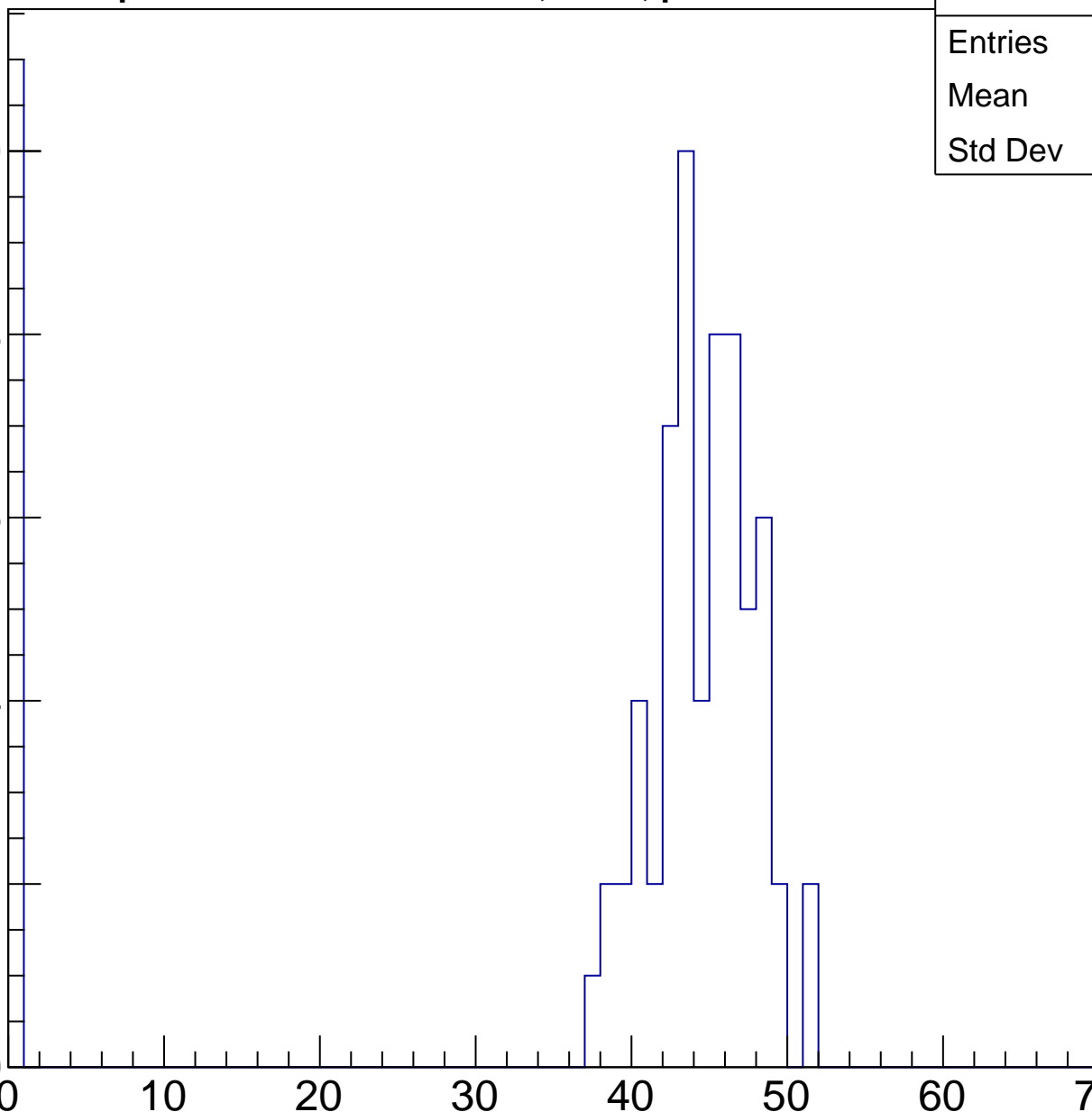
40

50

60

70

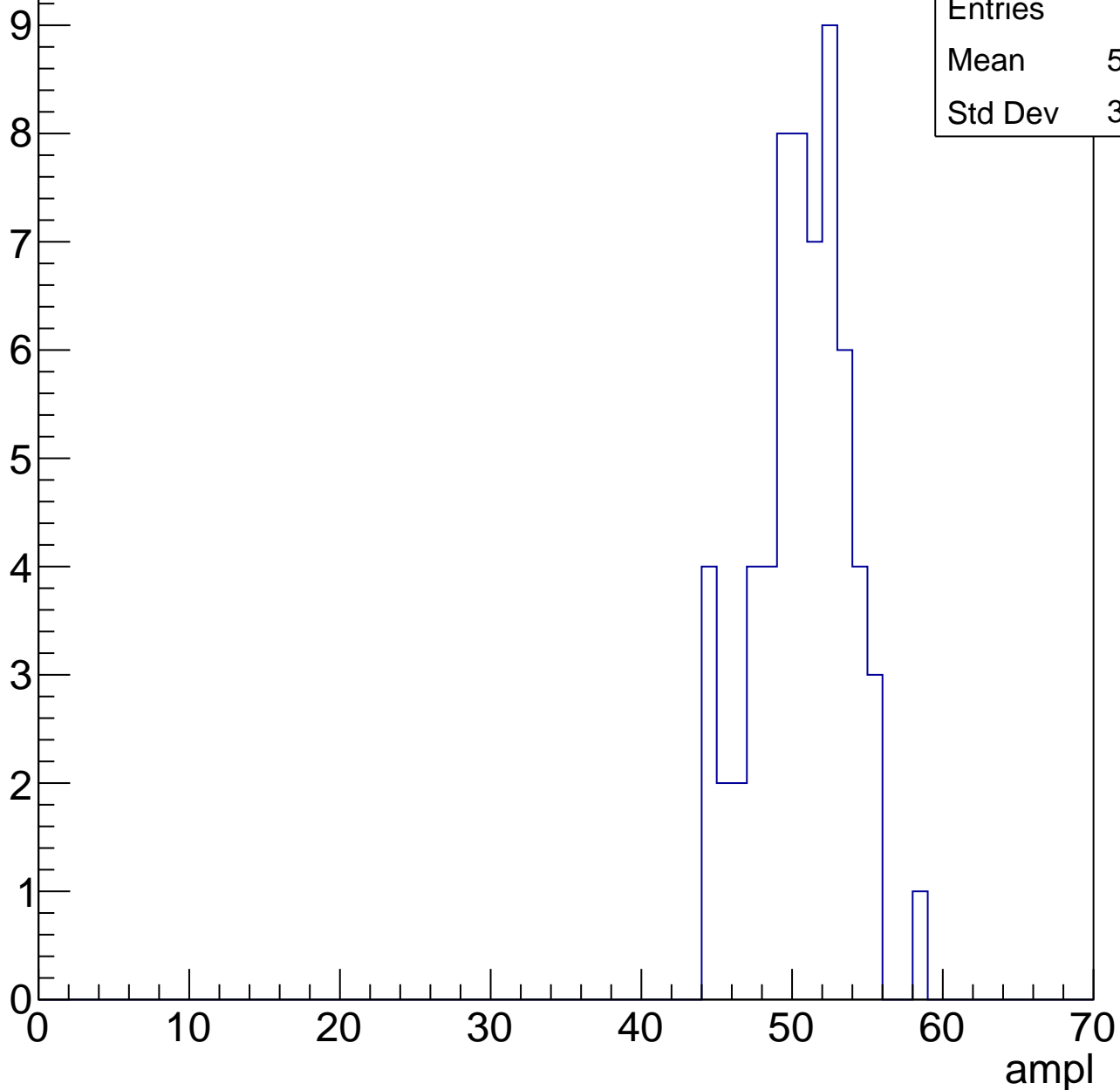
ampl



# B1L103S, U4-ch45, adc3

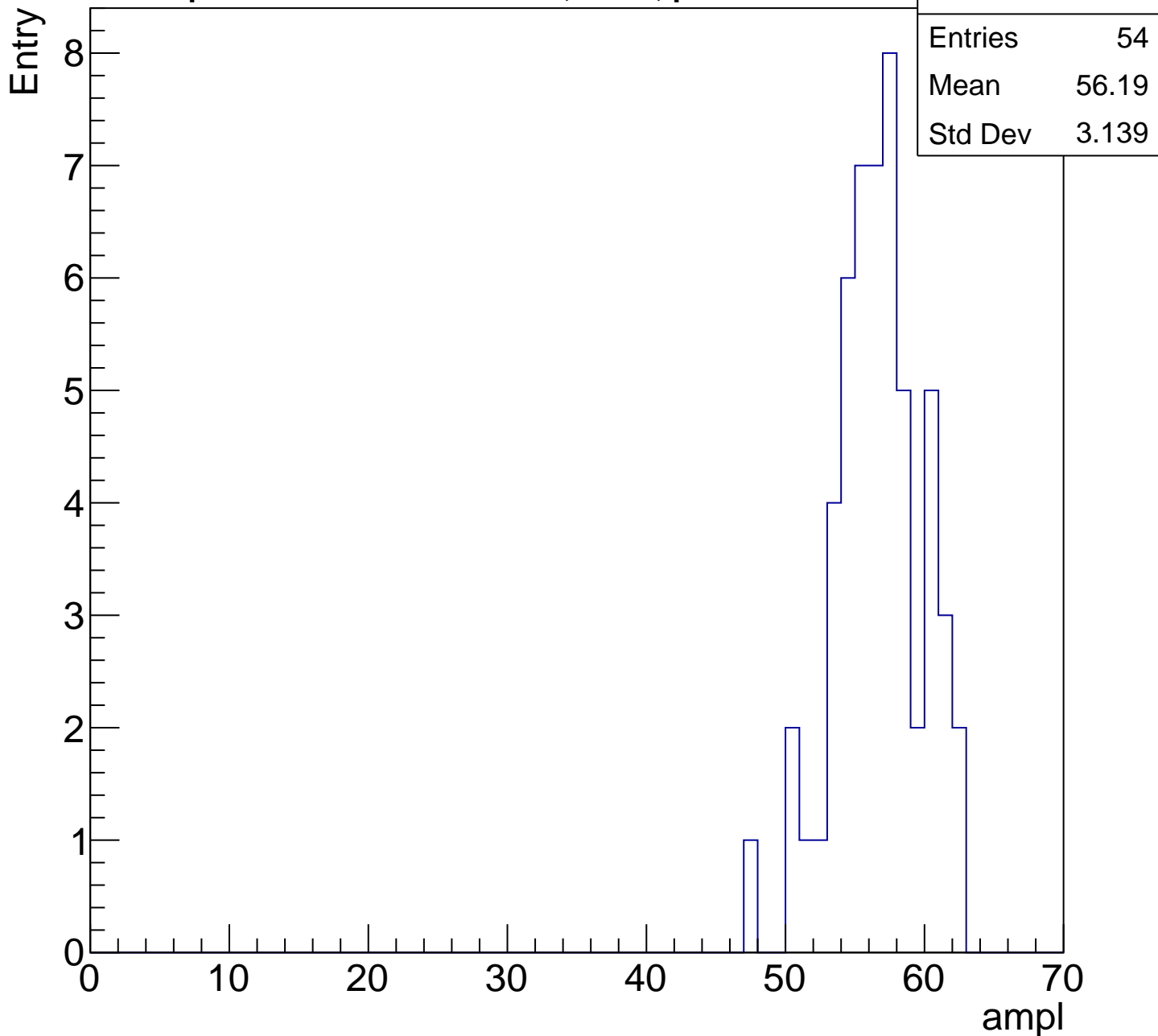
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U4-ch45, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

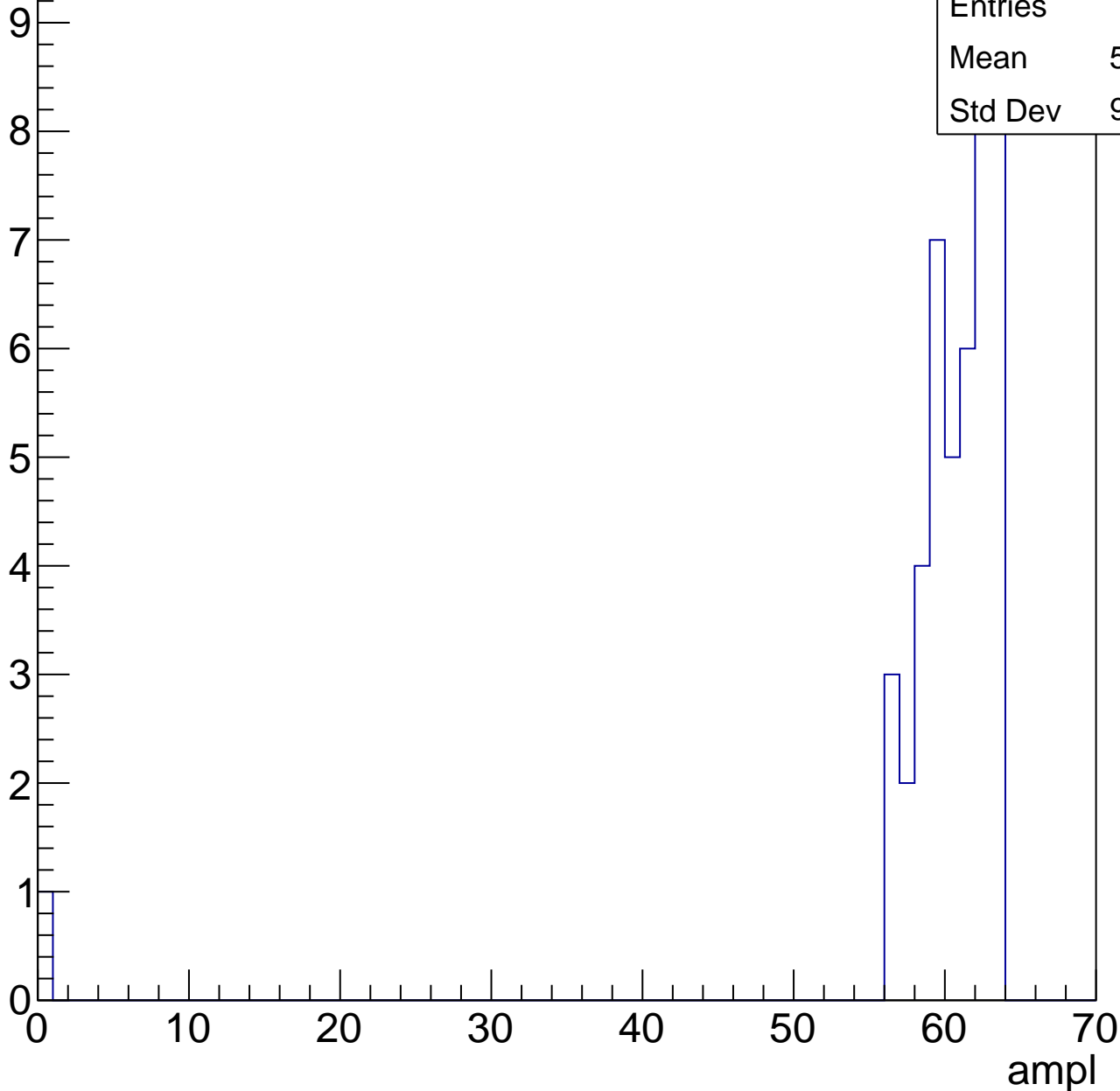


# B1L103S, U4-ch45, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

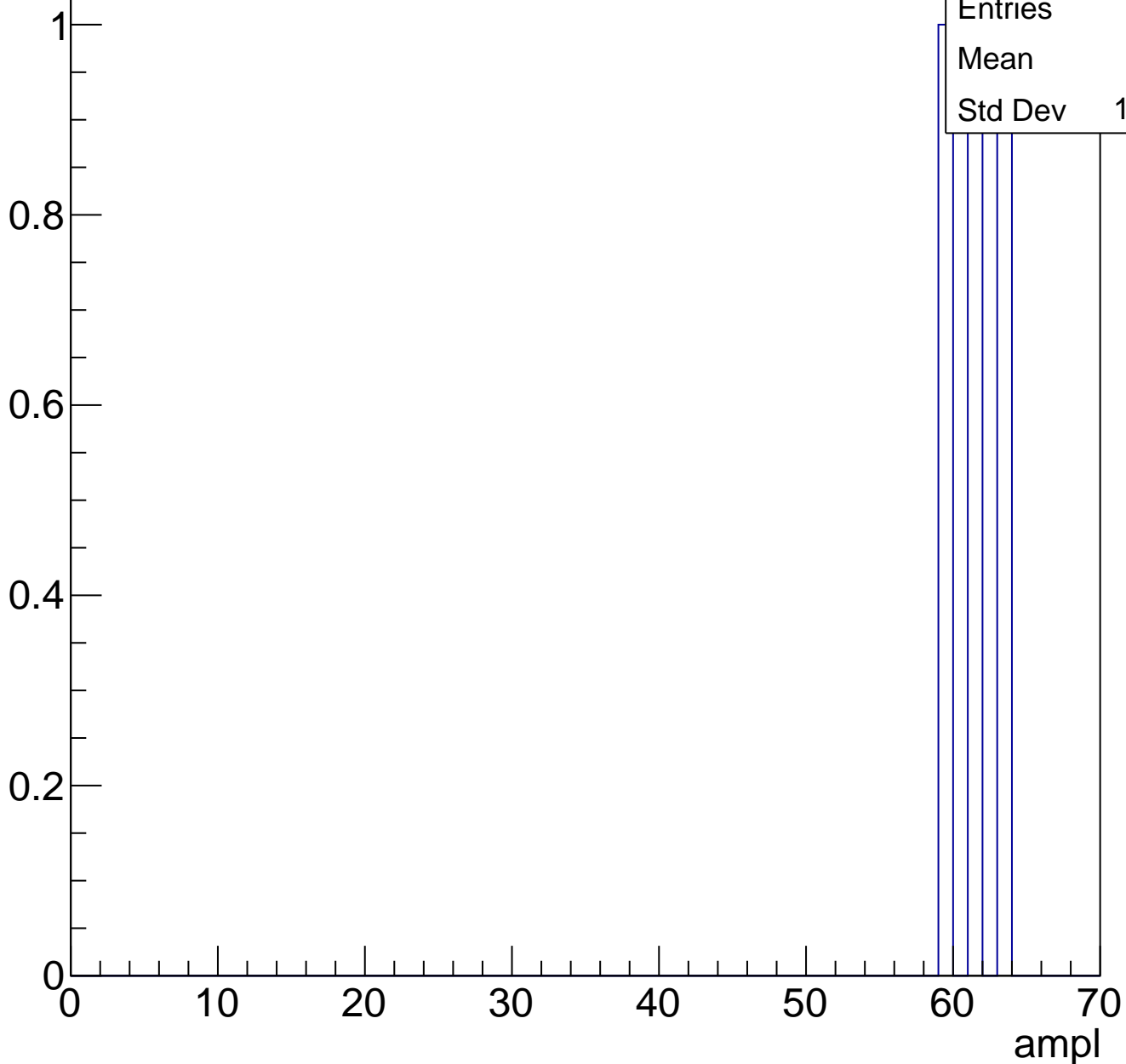
|         |       |
|---------|-------|
| Entries | 45    |
| Mean    | 59.02 |
| Std Dev | 9.147 |



# B1L103S, U4-ch45, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U4-ch45, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

|         |    |
|---------|----|
| Entries | 19 |
| Mean    | 0  |
| Std Dev | 0  |

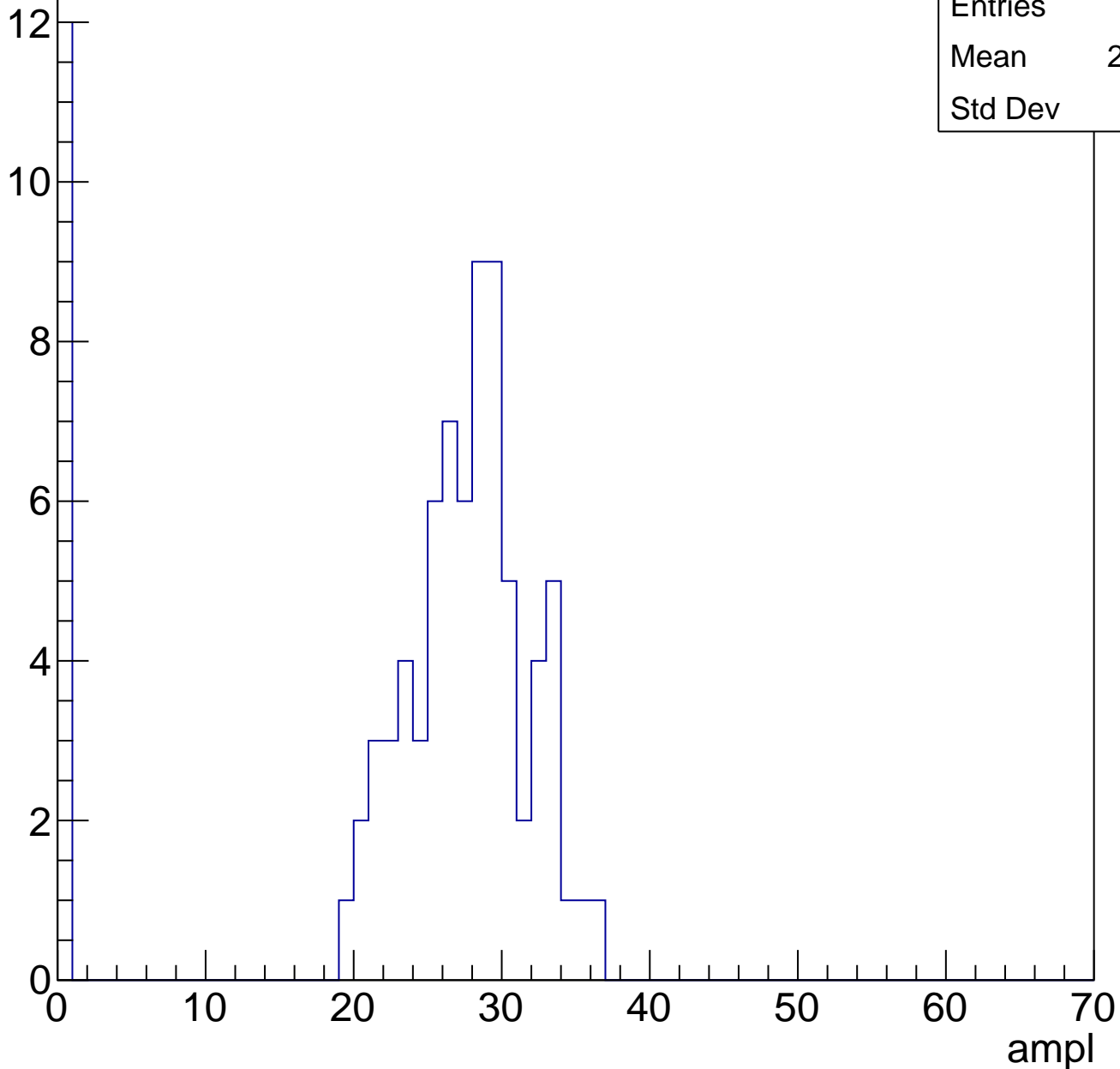
ampl

# B1L103S, U4-ch46, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 84    |
| Mean    | 23.44 |
| Std Dev | 10.2  |

Entry

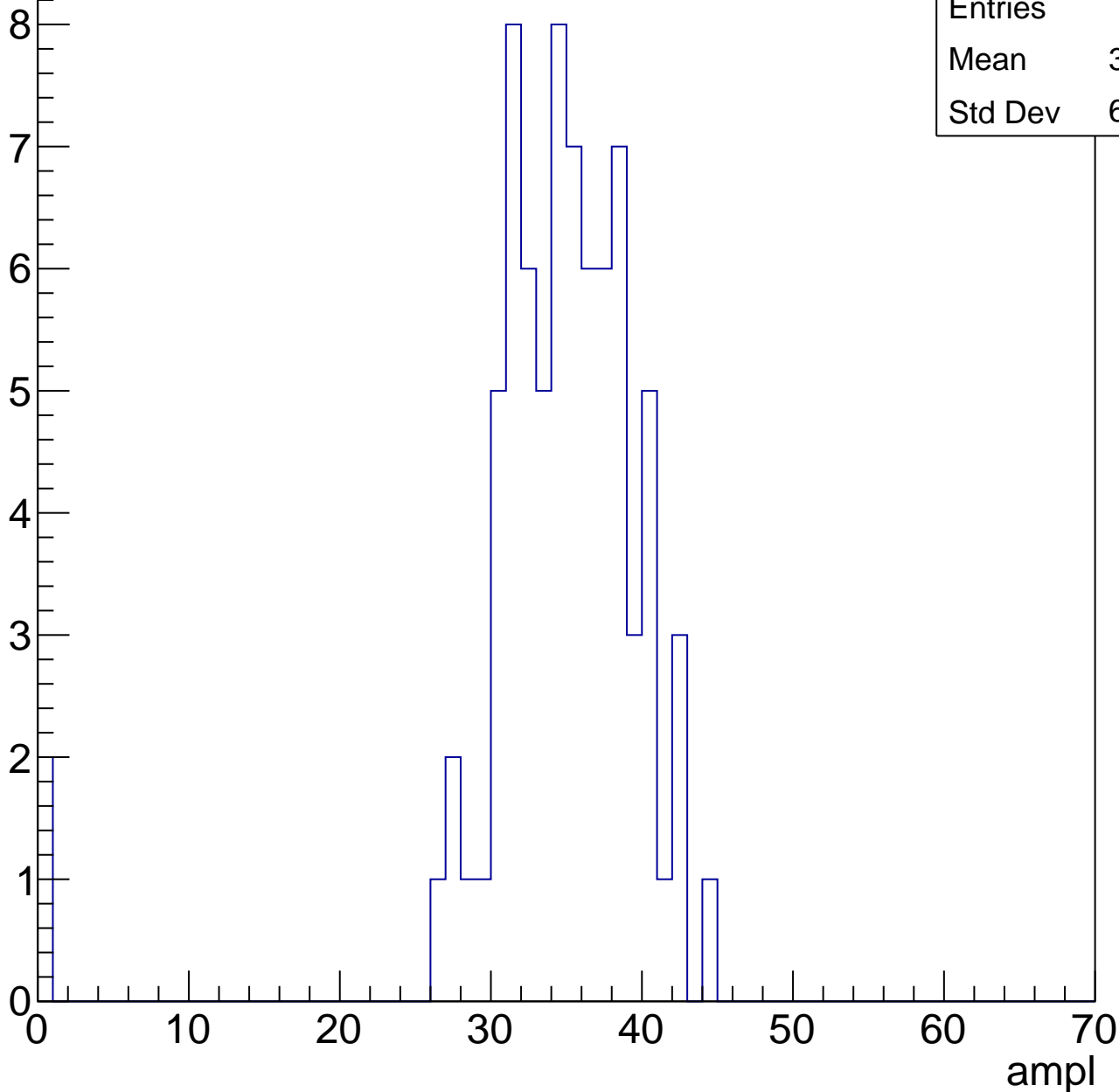


# B1L103S, U4-ch46, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 78    |
| Mean    | 33.86 |
| Std Dev | 6.706 |

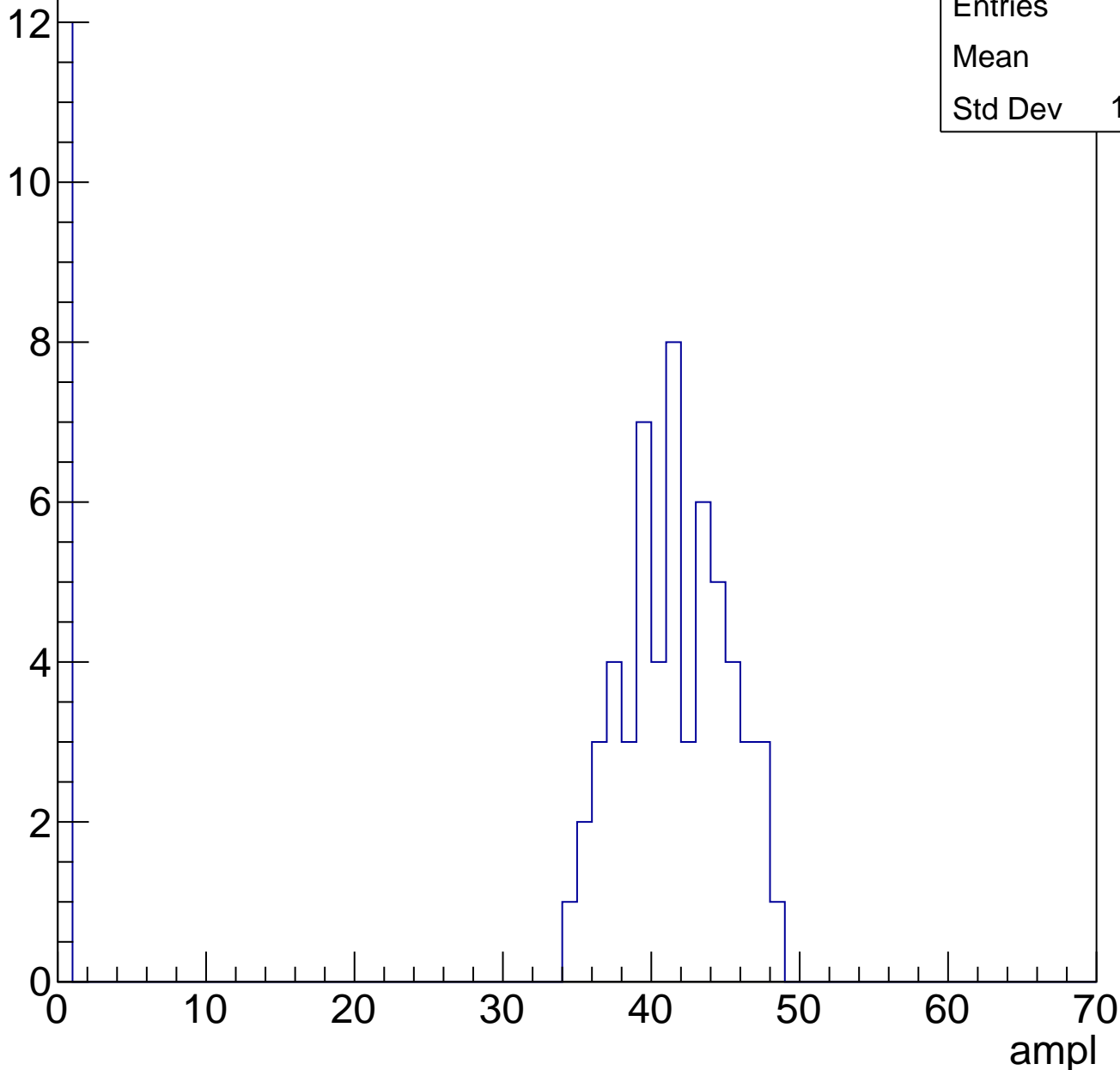


# B1L103S, U4-ch46, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 69    |
| Mean    | 34    |
| Std Dev | 15.92 |

Entry

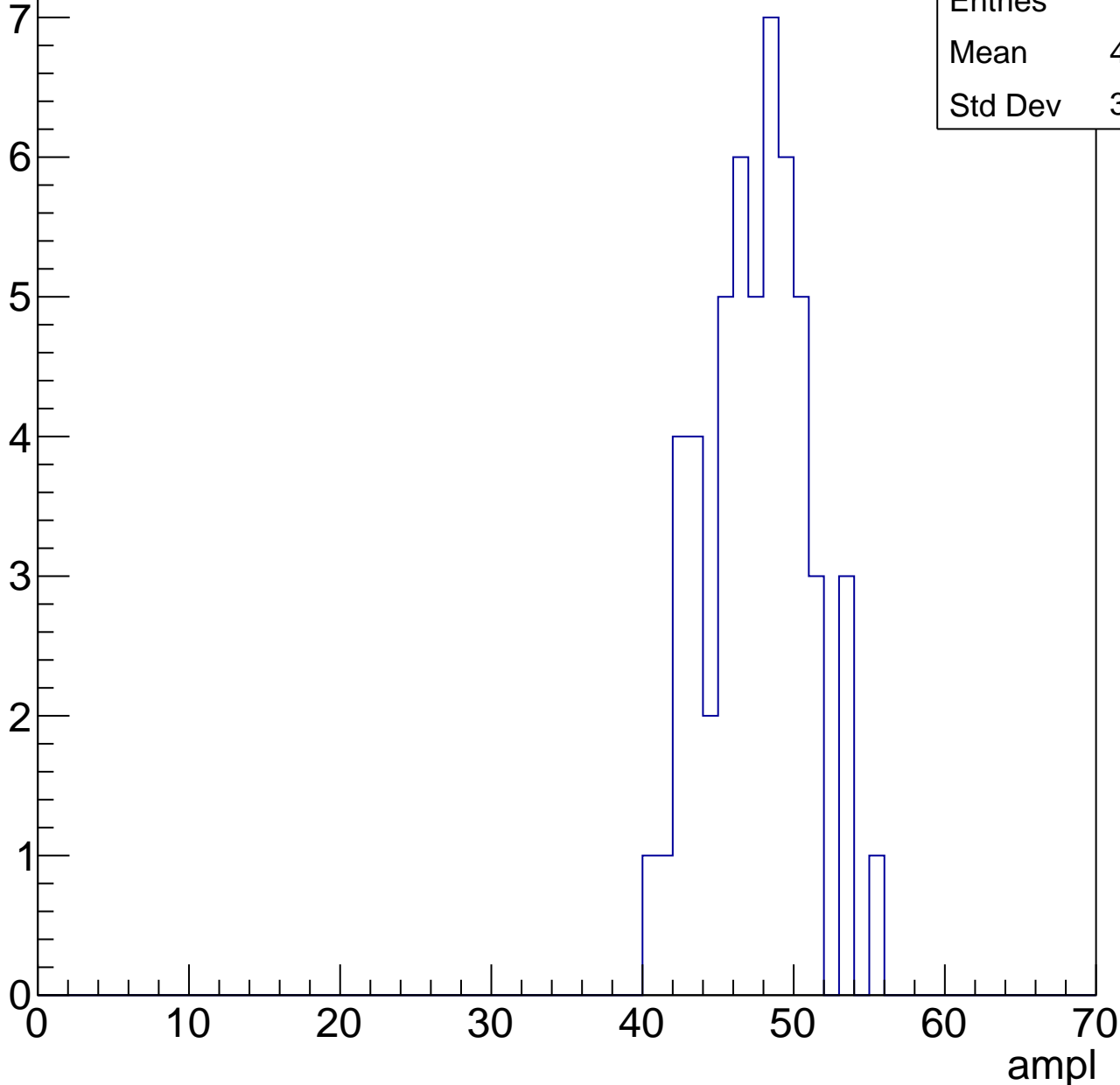


# B1L103S, U4-ch46, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

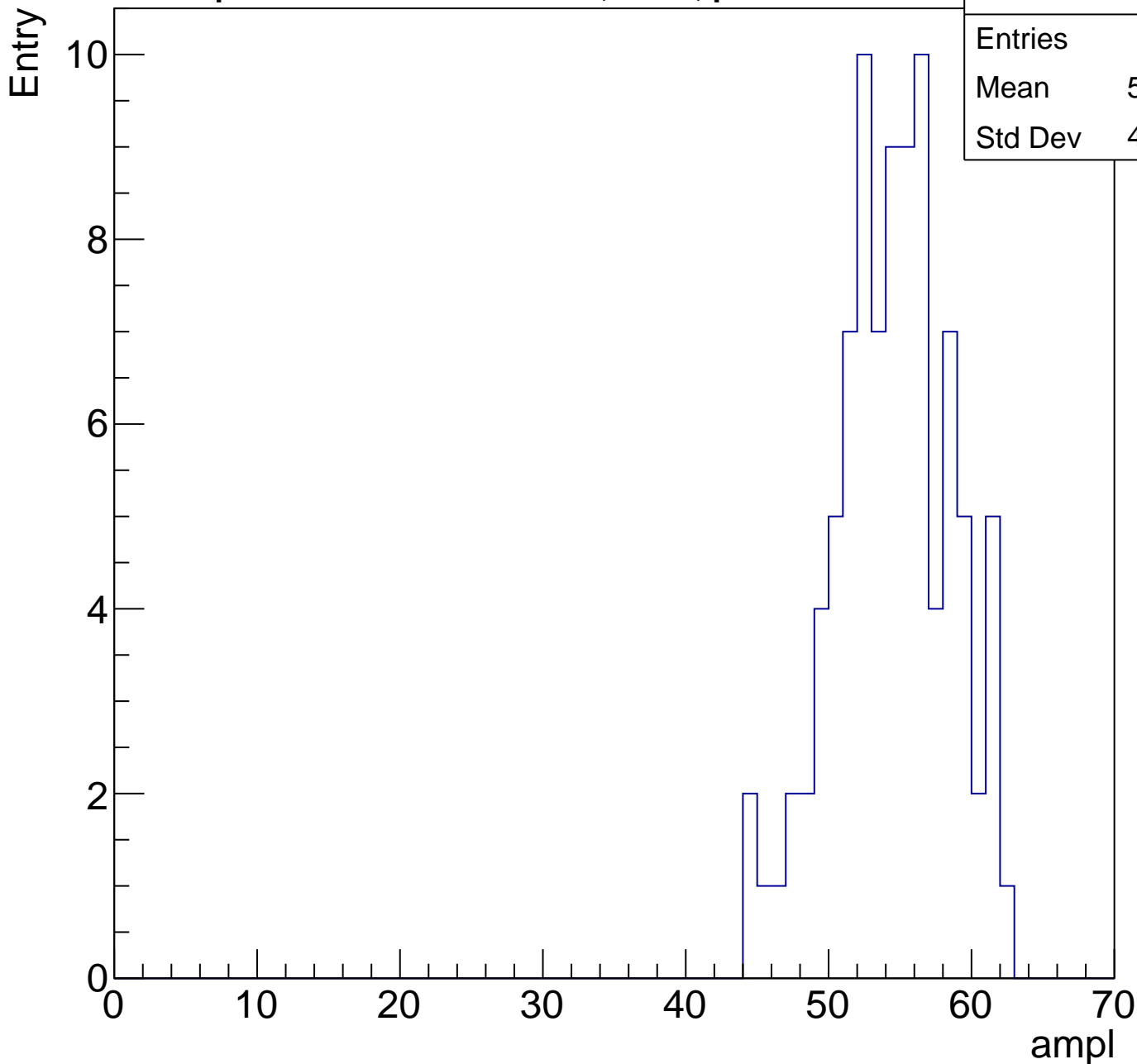
|         |       |
|---------|-------|
| Entries | 53    |
| Mean    | 47.02 |
| Std Dev | 3.334 |



# B1L103S, U4-ch46, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 93    |
| Mean    | 53.98 |
| Std Dev | 4.027 |

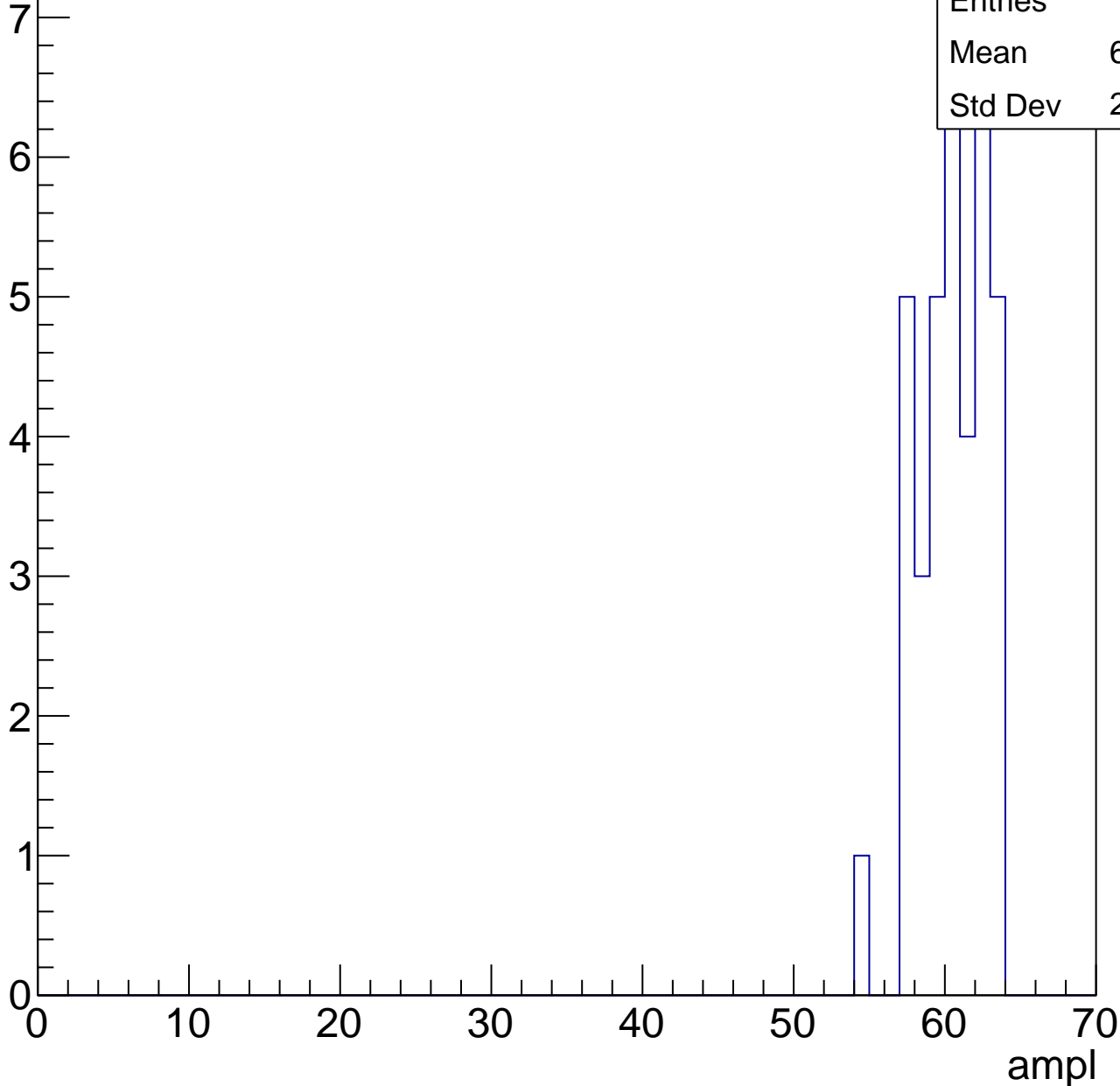


# B1L103S, U4-ch46, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 37    |
| Mean    | 60.03 |
| Std Dev | 2.175 |

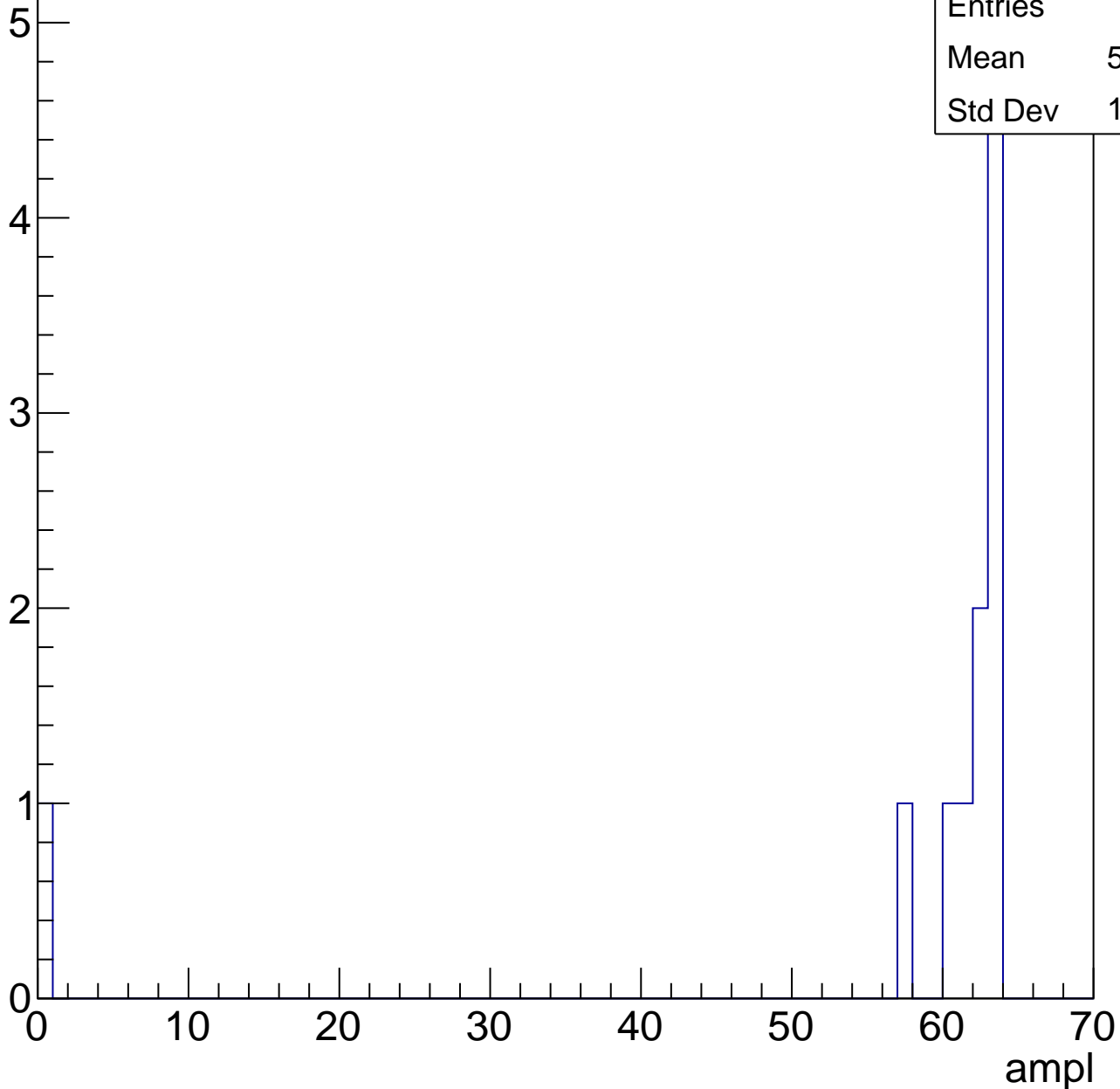


# B1L103S, U4-ch46, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 11    |
| Mean    | 56.09 |
| Std Dev | 17.82 |





# B1L103S, U4-ch46, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U4-ch47, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 74    |
| Mean    | 24.15 |
| Std Dev | 10.53 |

Entry

10

8

6

4

2

0

0

10

20

30

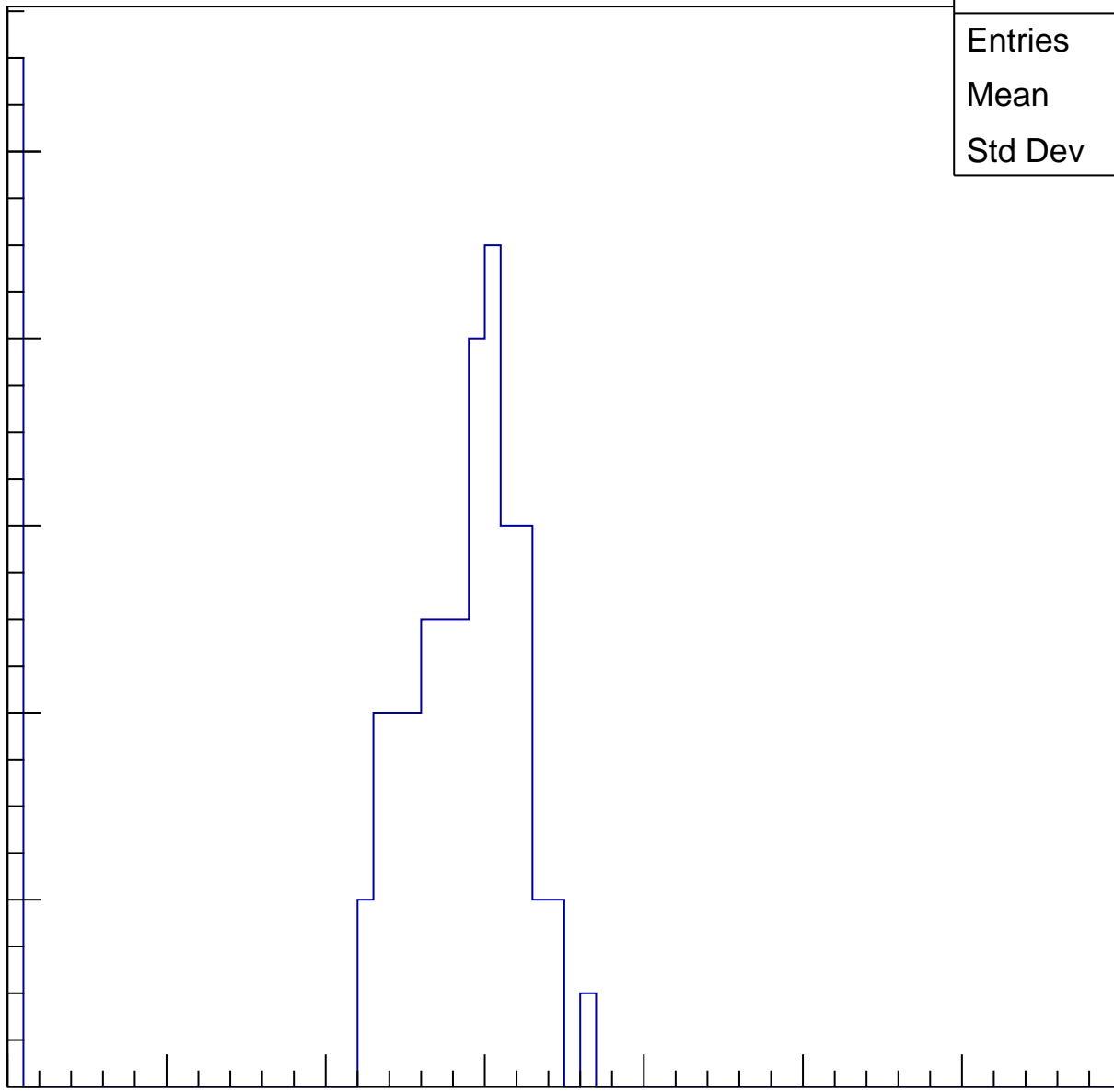
40

50

60

70

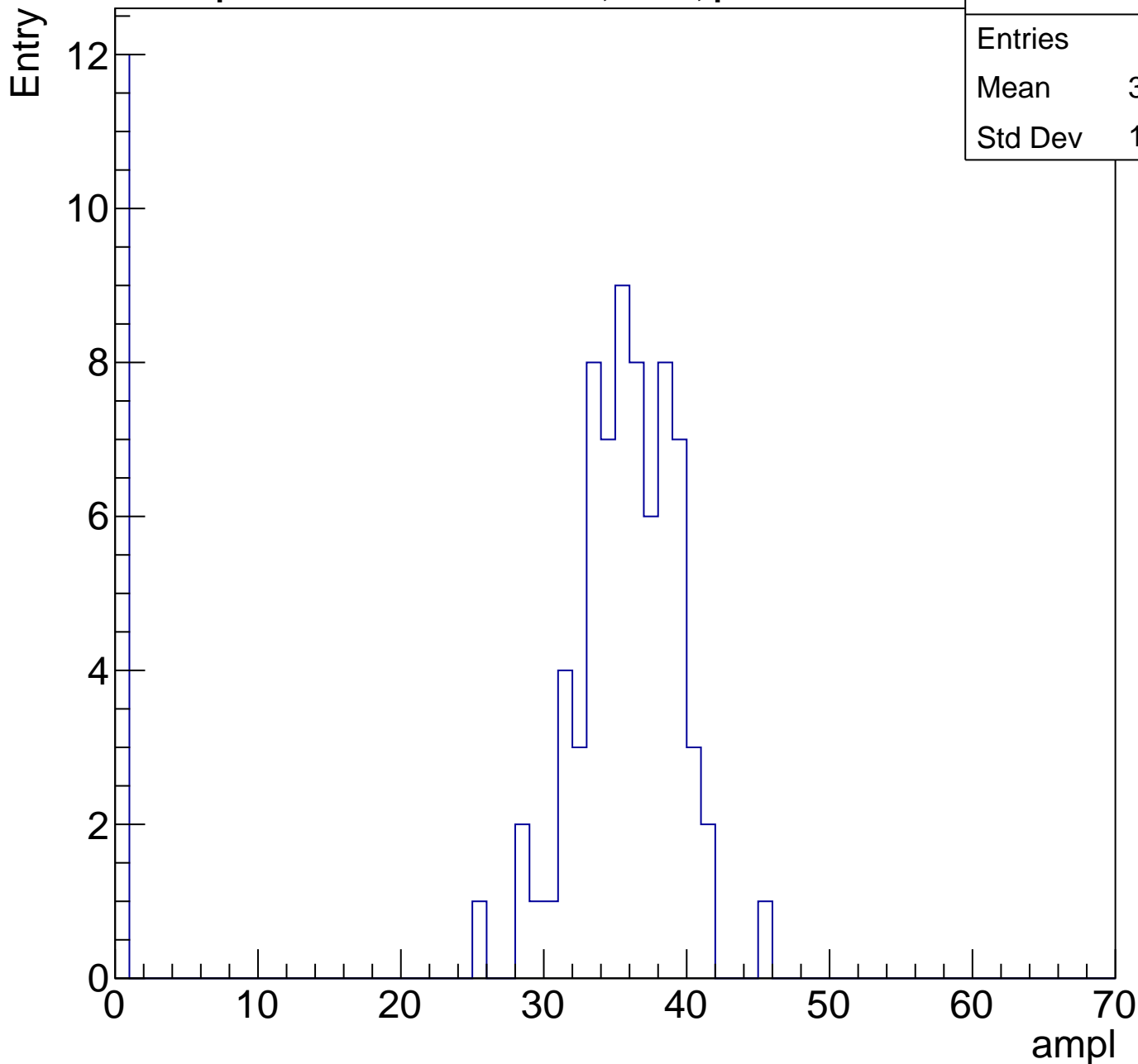
ampl



# B1L103S, U4-ch47, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 83    |
| Mean    | 30.25 |
| Std Dev | 12.84 |

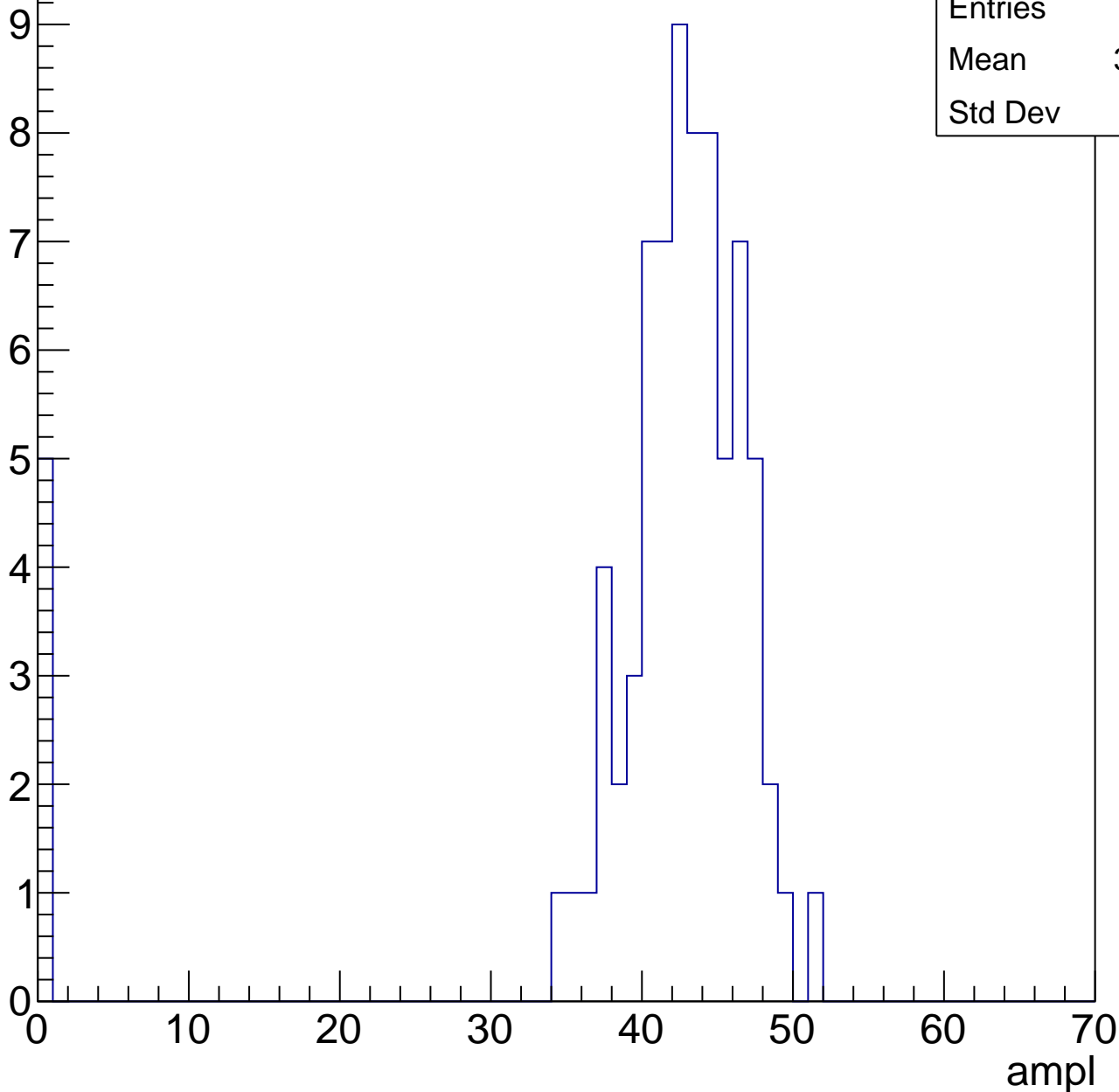


# B1L103S, U4-ch47, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

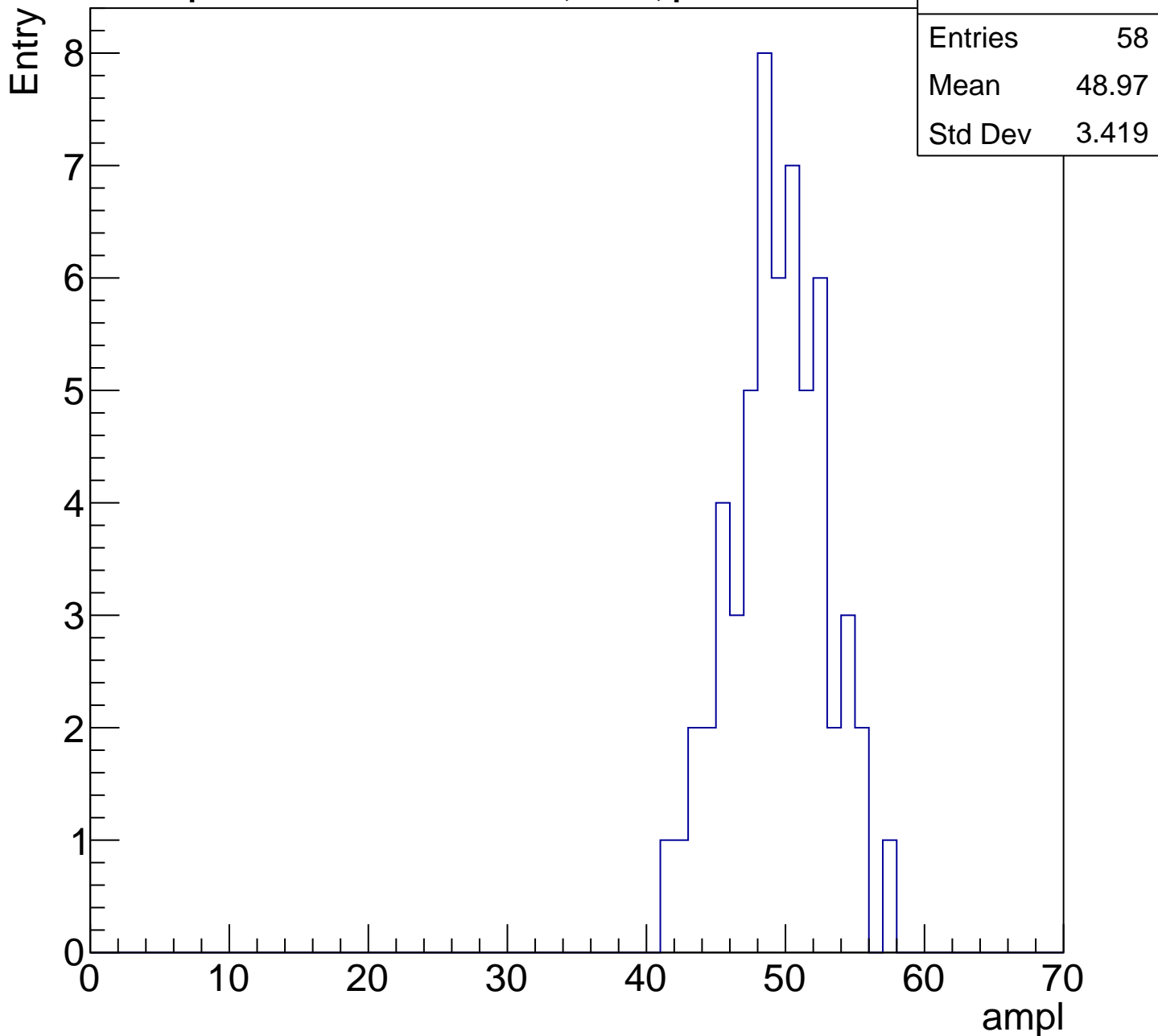
Entry

|         |       |
|---------|-------|
| Entries | 77    |
| Mean    | 39.81 |
| Std Dev | 11    |



# B1L103S, U4-ch47, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

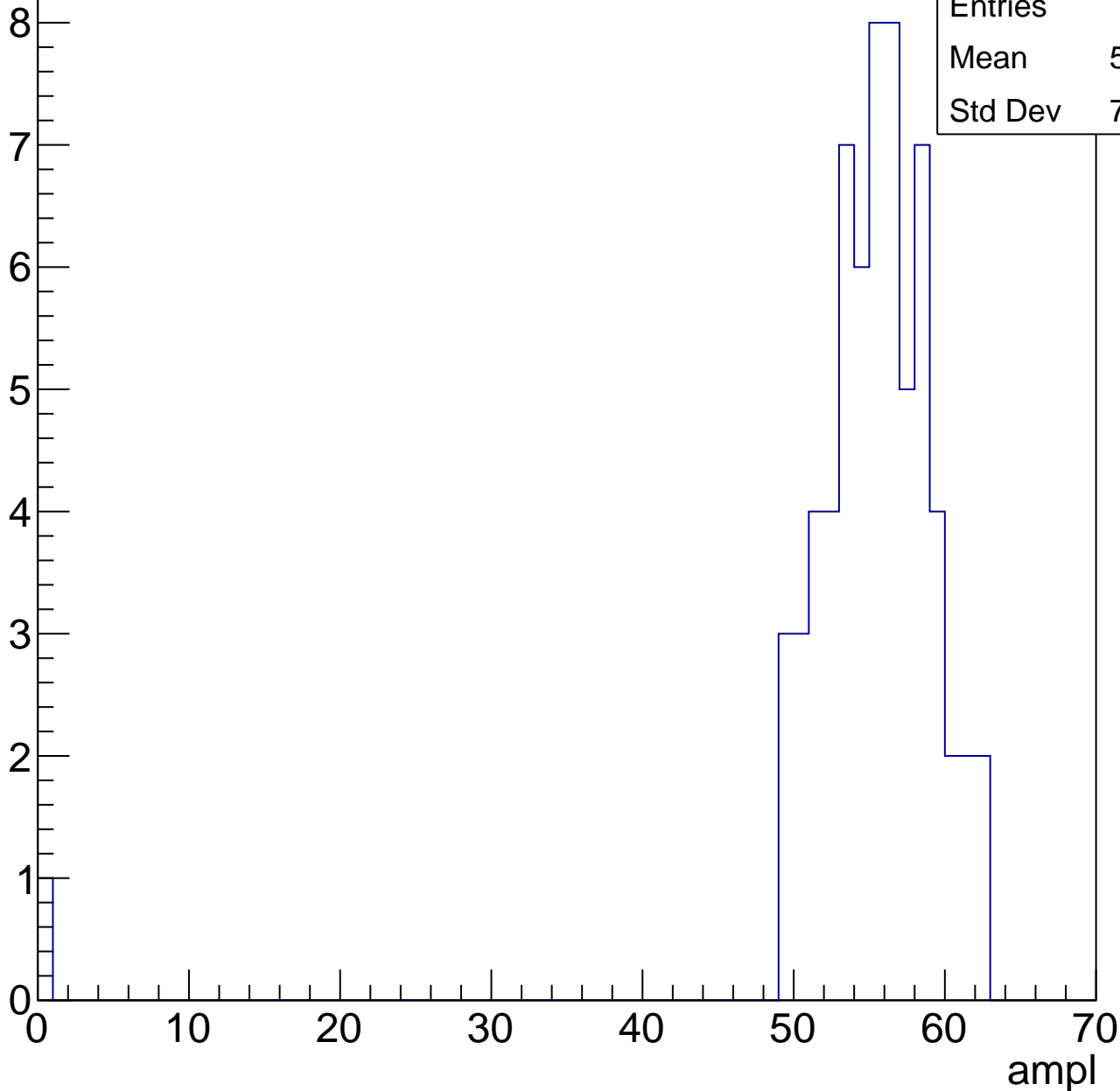


# B1L103S, U4-ch47, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 66    |
| Mean    | 54.32 |
| Std Dev | 7.474 |

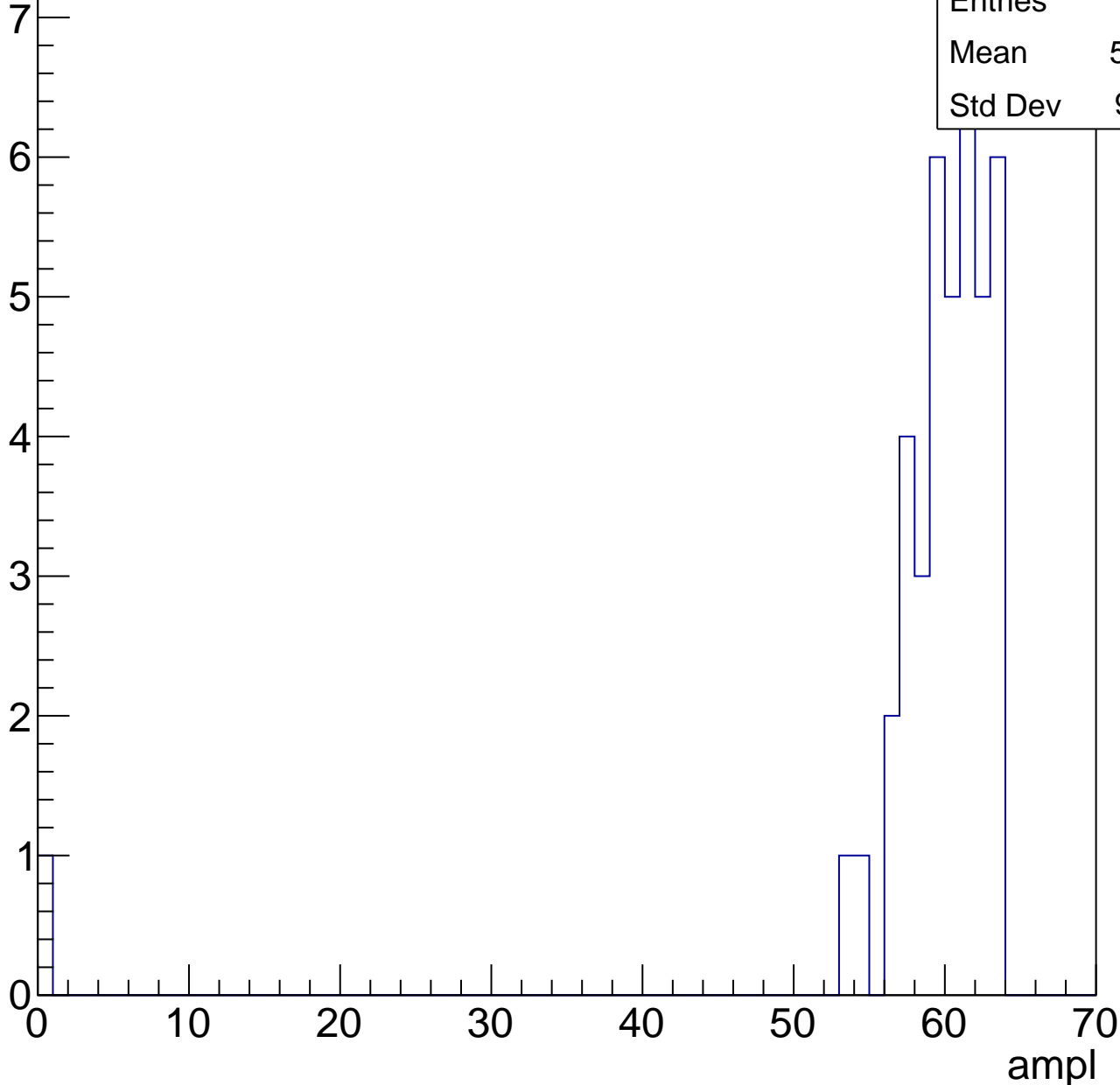


# B1L103S, U4-ch47, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

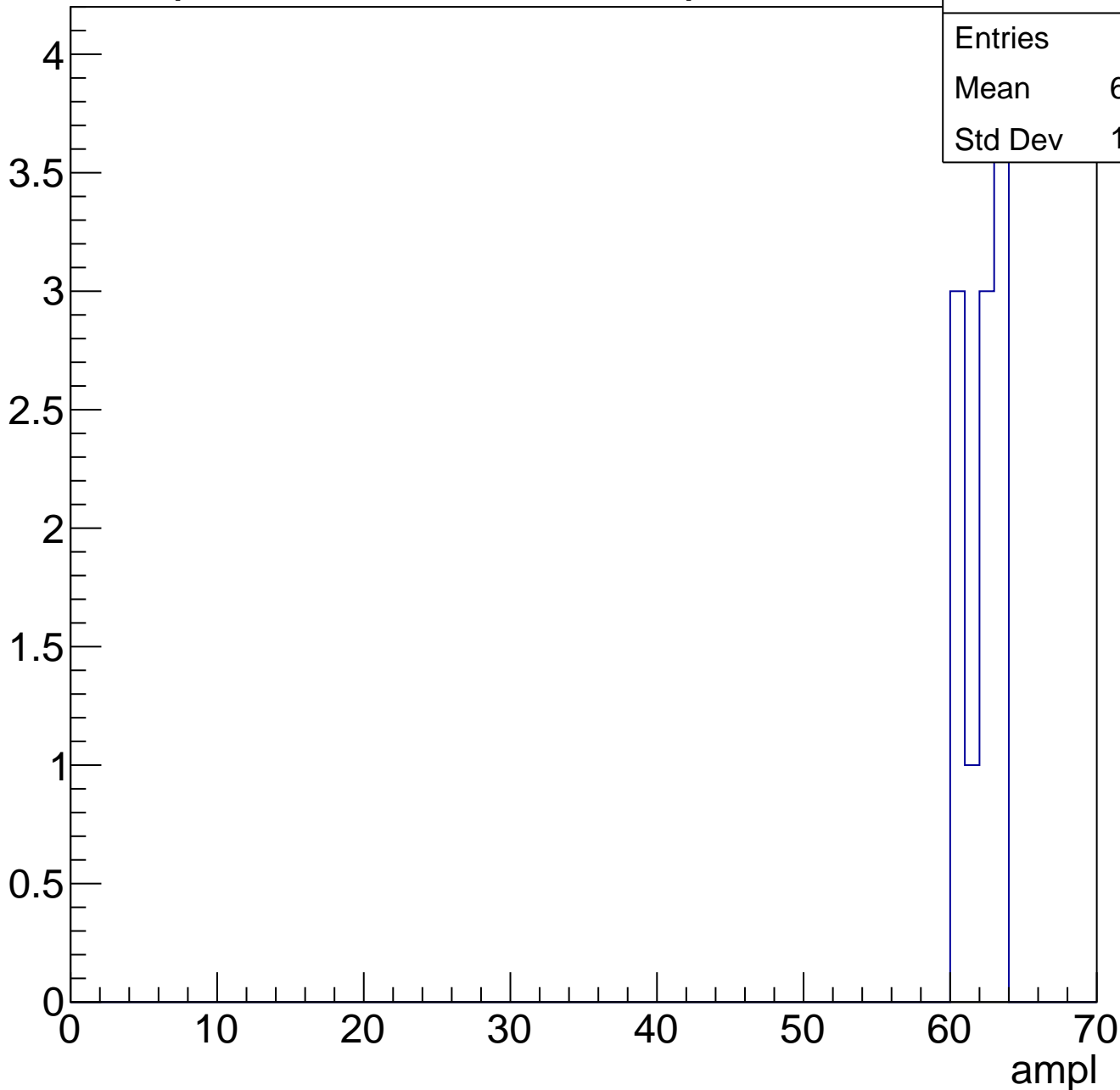
|         |       |
|---------|-------|
| Entries | 41    |
| Mean    | 58.29 |
| Std Dev | 9.541 |



# B1L103S, U4-ch47, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U4-ch47, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

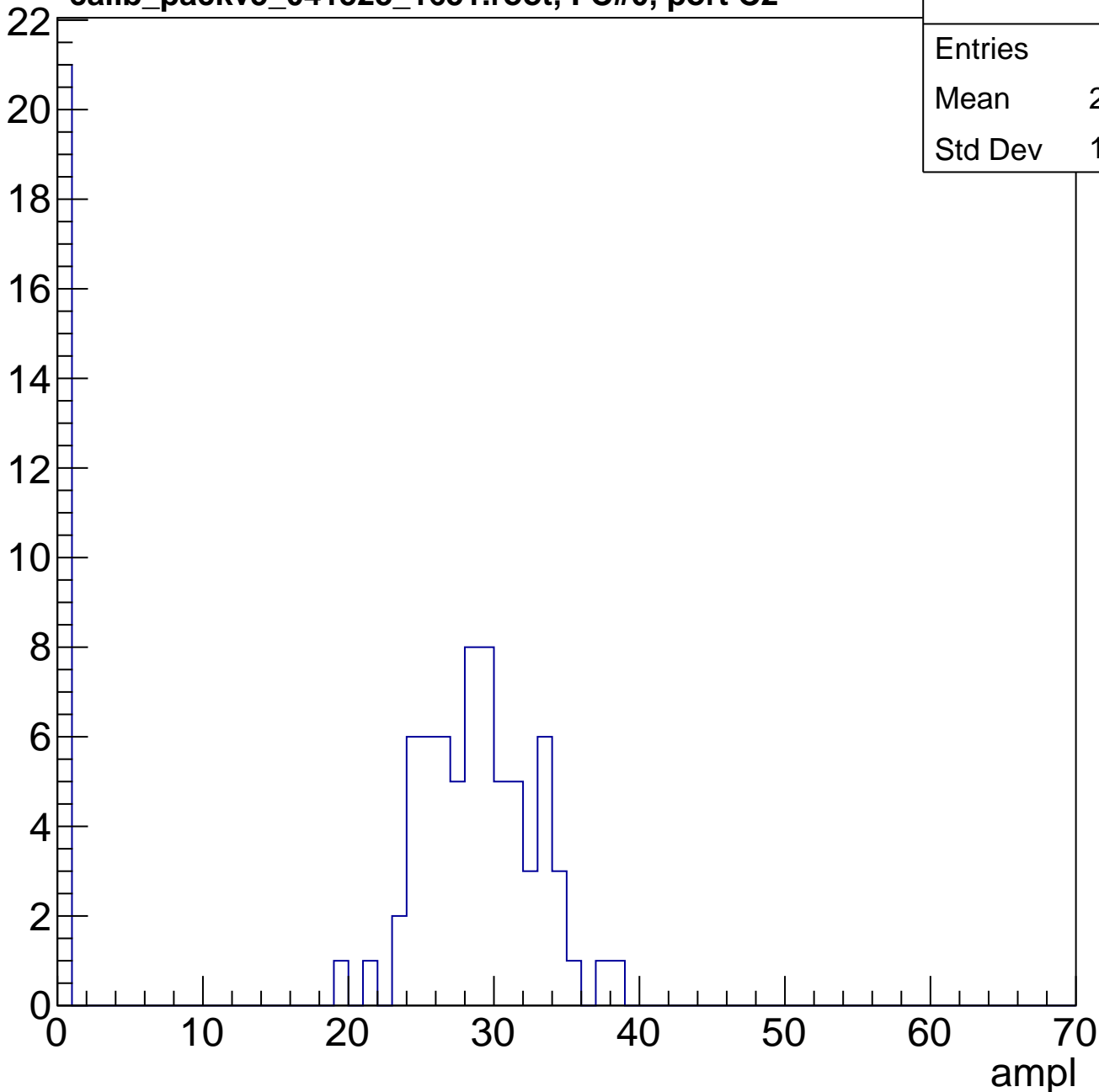
|         |    |
|---------|----|
| Entries | 19 |
| Mean    | 0  |
| Std Dev | 0  |

# B1L103S, U4-ch48, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 89    |
| Mean    | 21.78 |
| Std Dev | 12.53 |

Entry

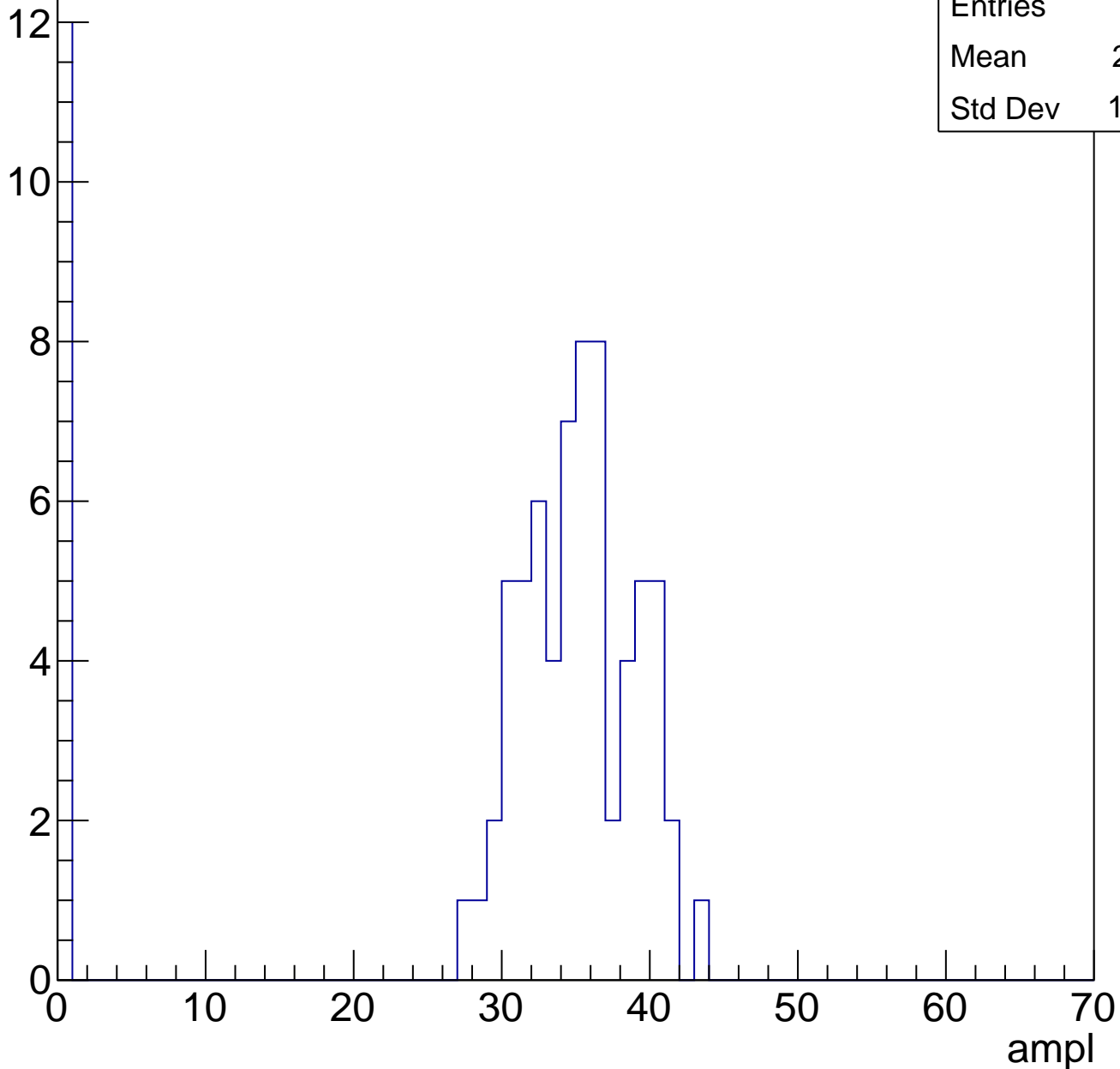


# B1L103S, U4-ch48, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 78    |
| Mean    | 29.41 |
| Std Dev | 12.97 |

Entry



# B1L103S, U4-ch48, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

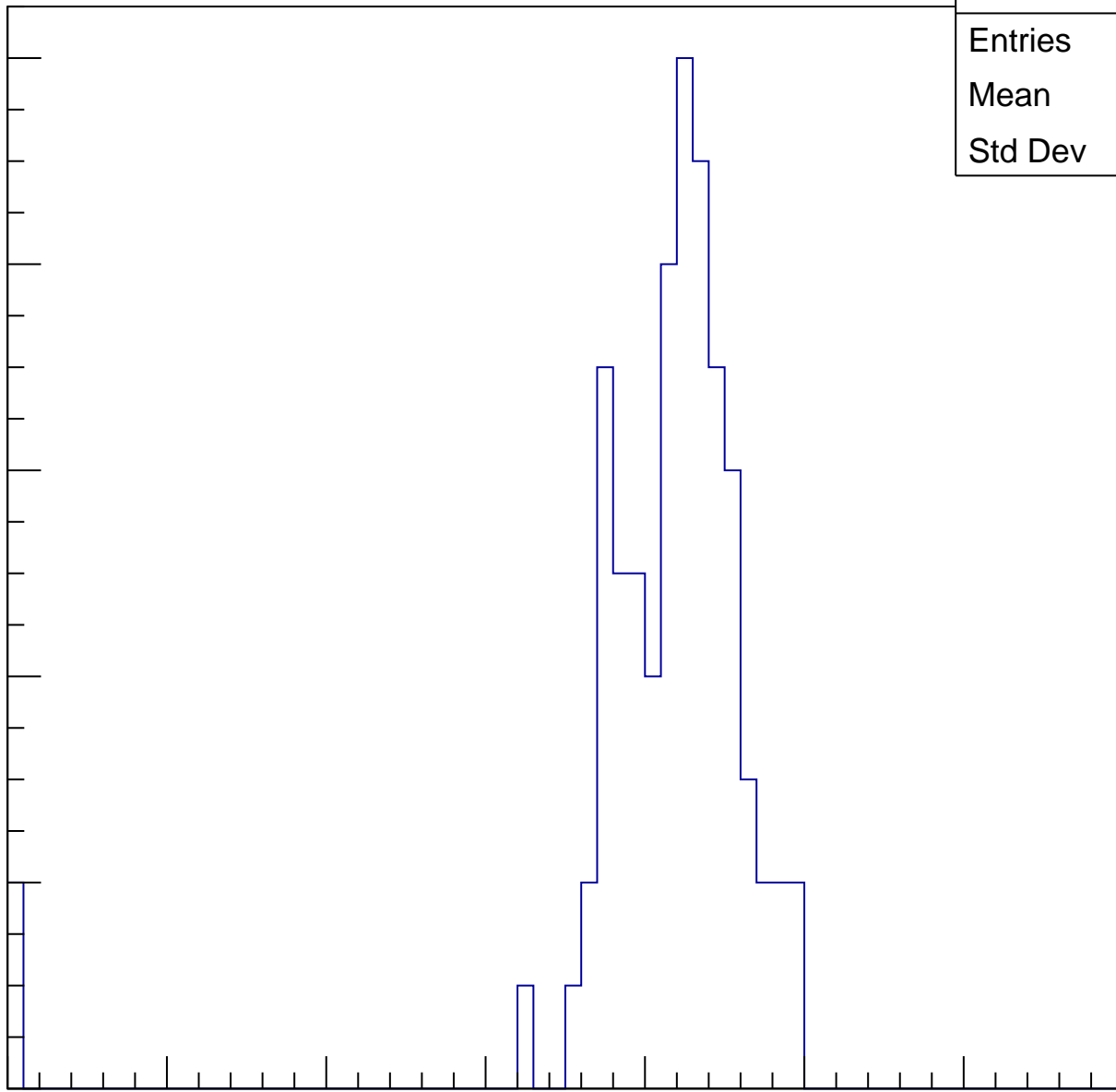
|         |       |
|---------|-------|
| Entries | 76    |
| Mean    | 40.55 |
| Std Dev | 7.498 |

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

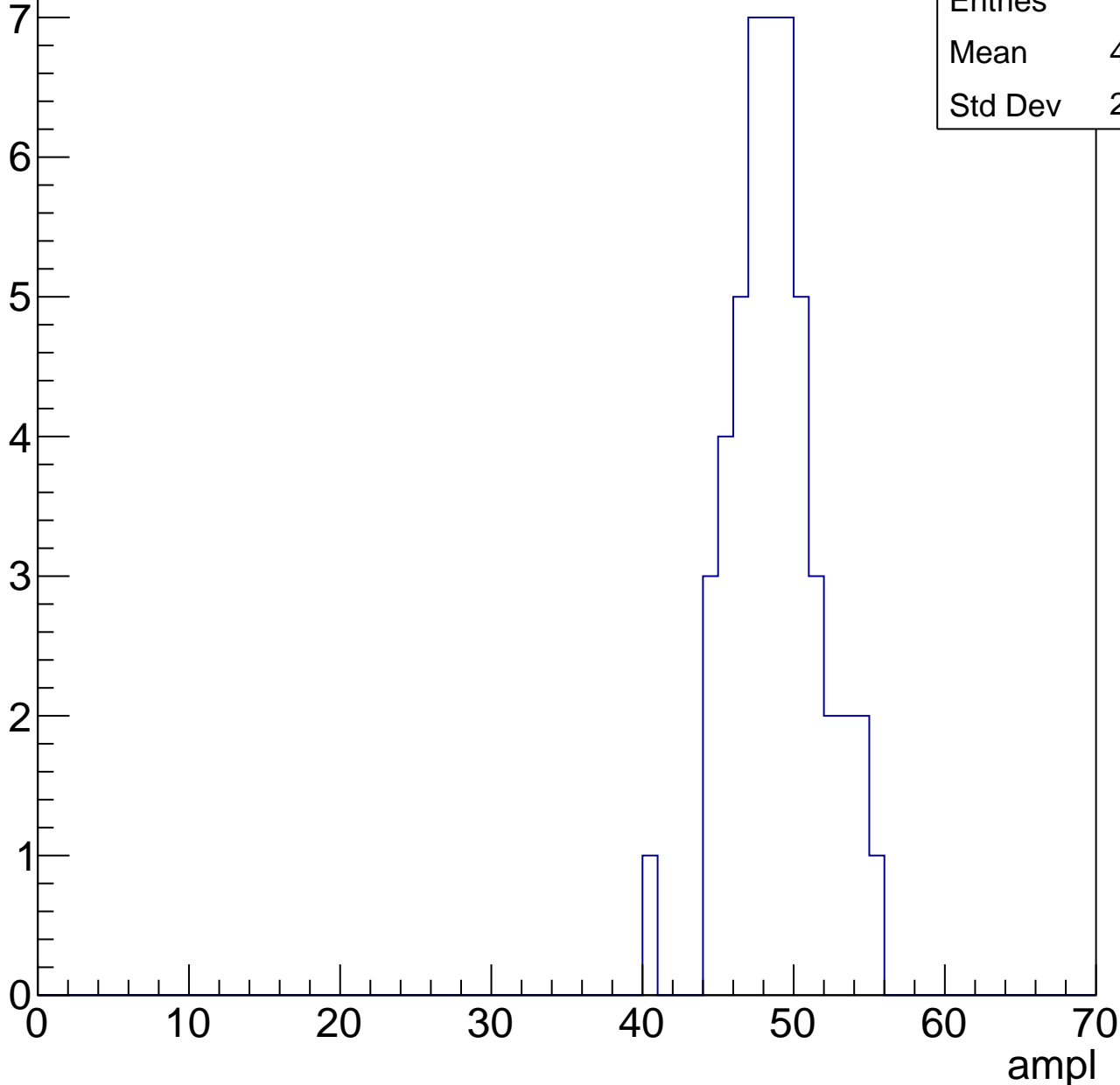


# B1L103S, U4-ch48, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 49    |
| Mean    | 48.29 |
| Std Dev | 2.955 |

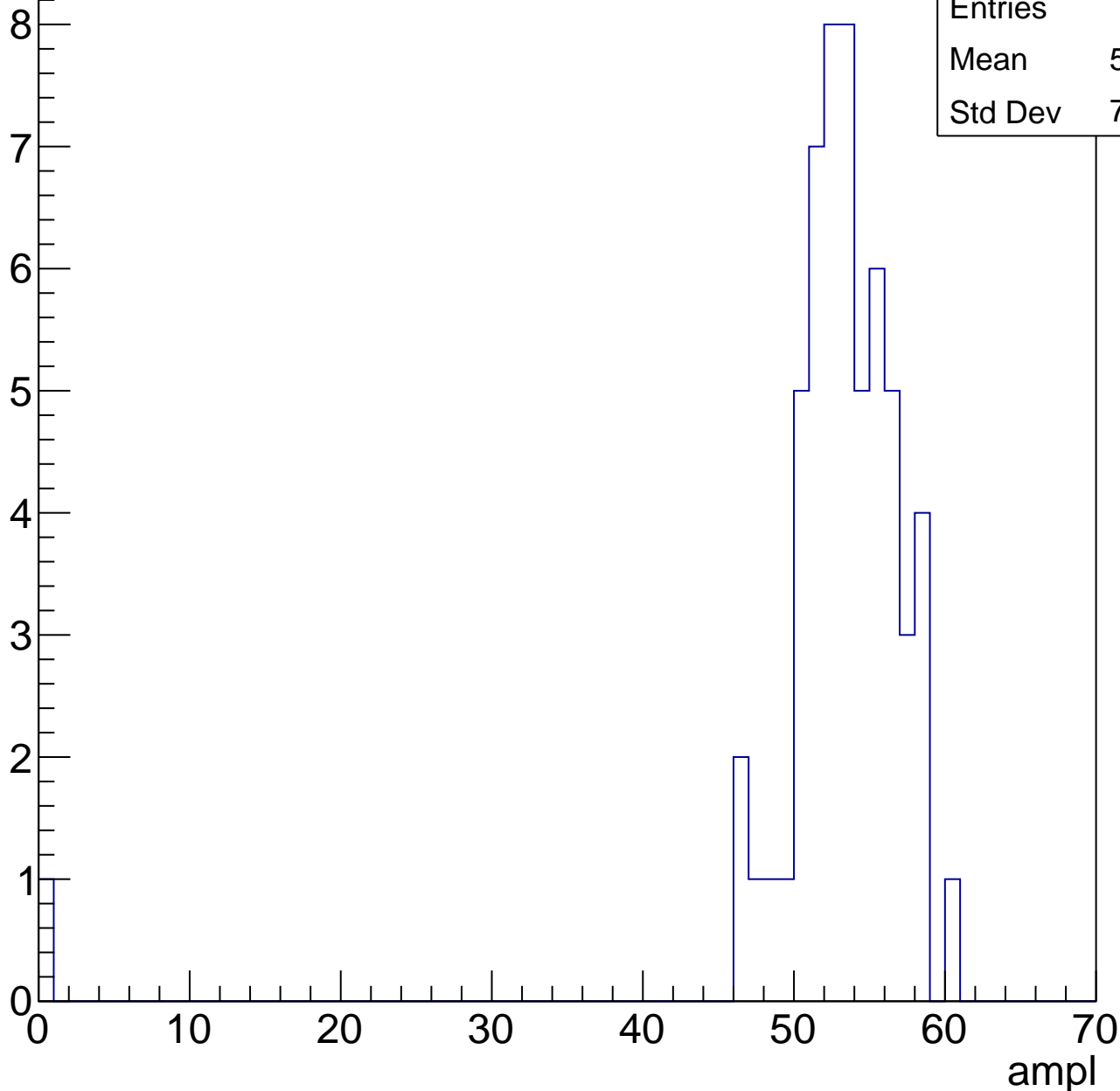


# B1L103S, U4-ch48, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

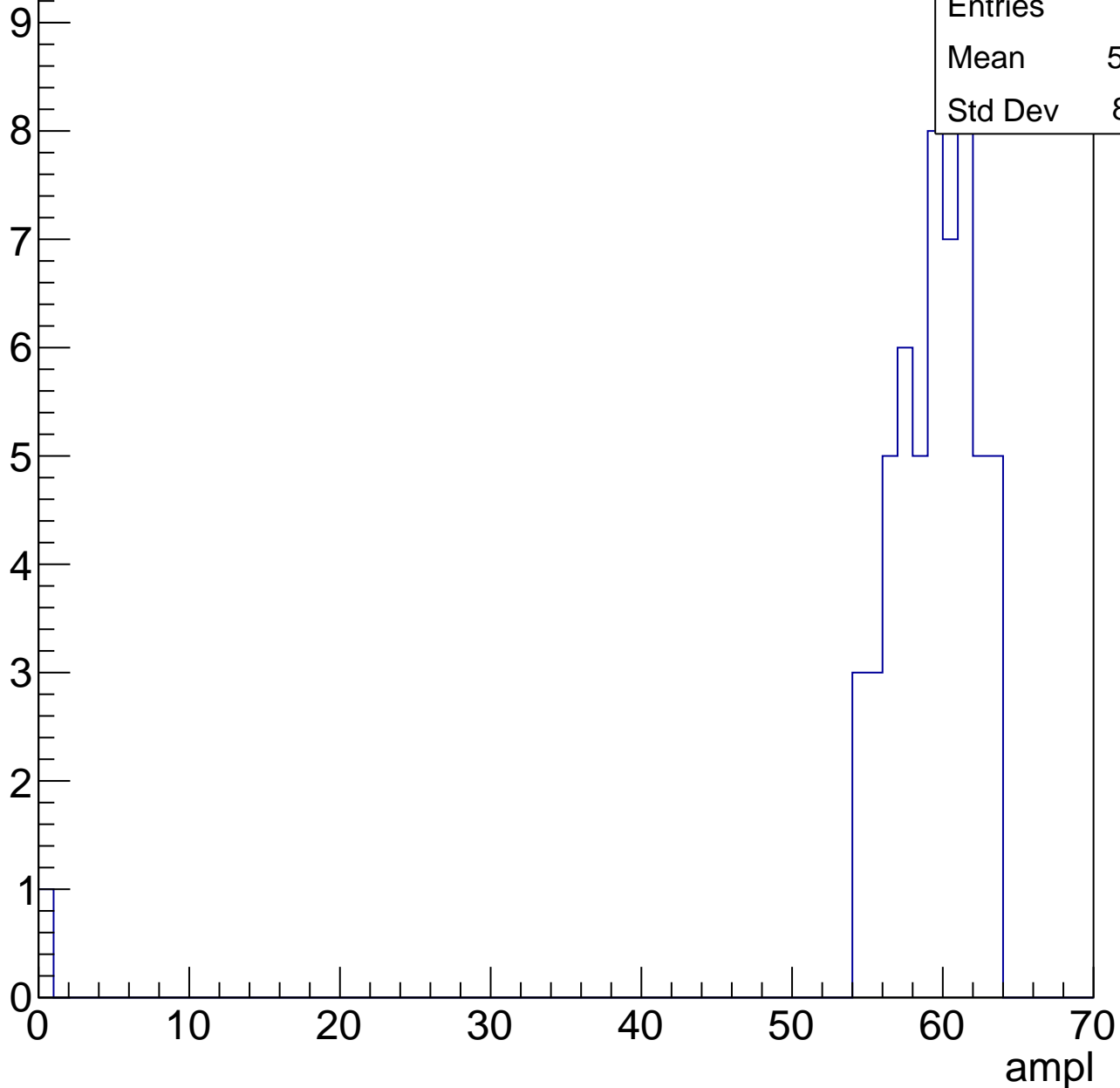
|         |       |
|---------|-------|
| Entries | 58    |
| Mean    | 52.17 |
| Std Dev | 7.539 |



# B1L103S, U4-ch48, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

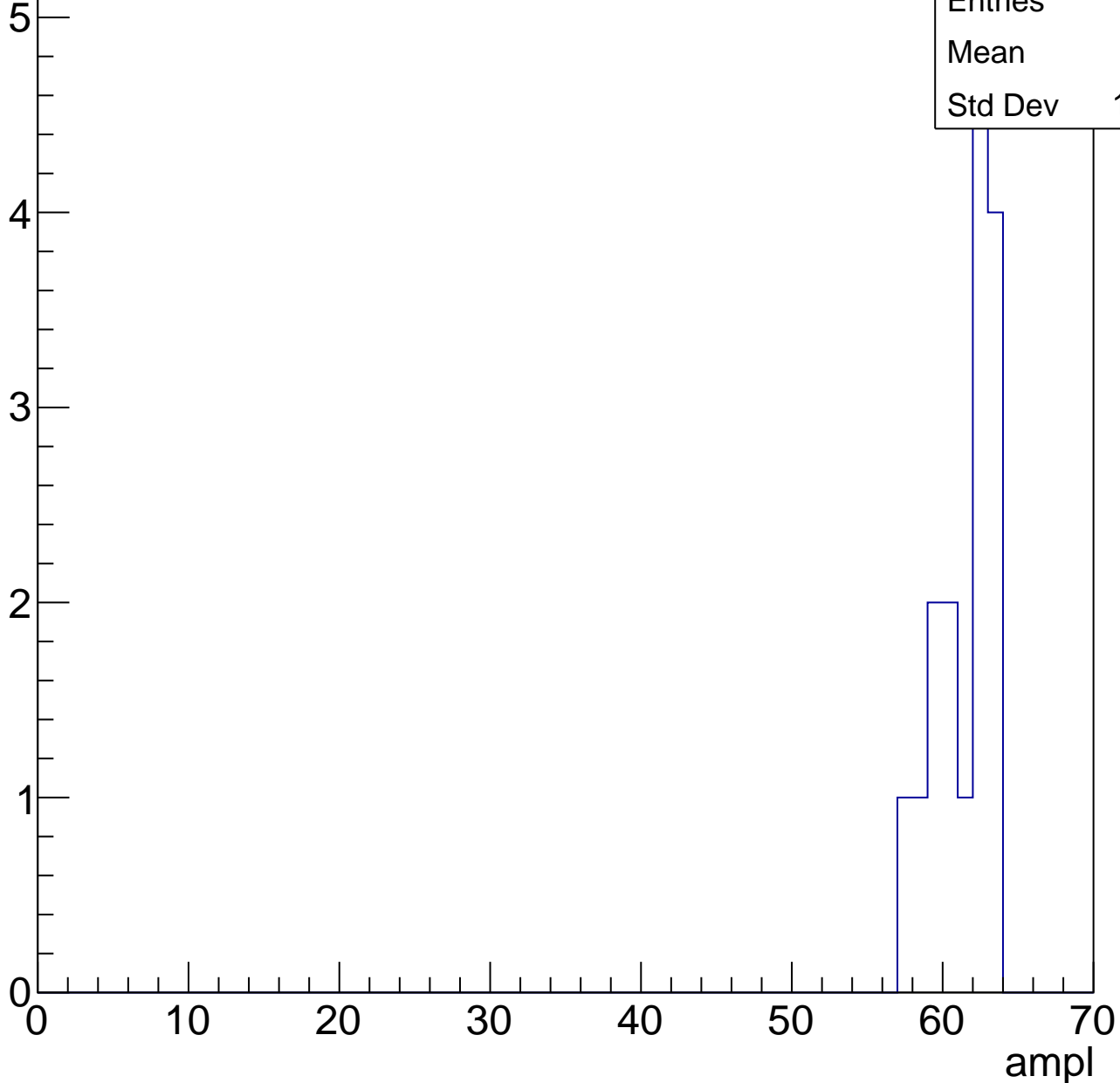


# B1L103S, U4-ch48, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 16    |
| Mean    | 61    |
| Std Dev | 1.871 |

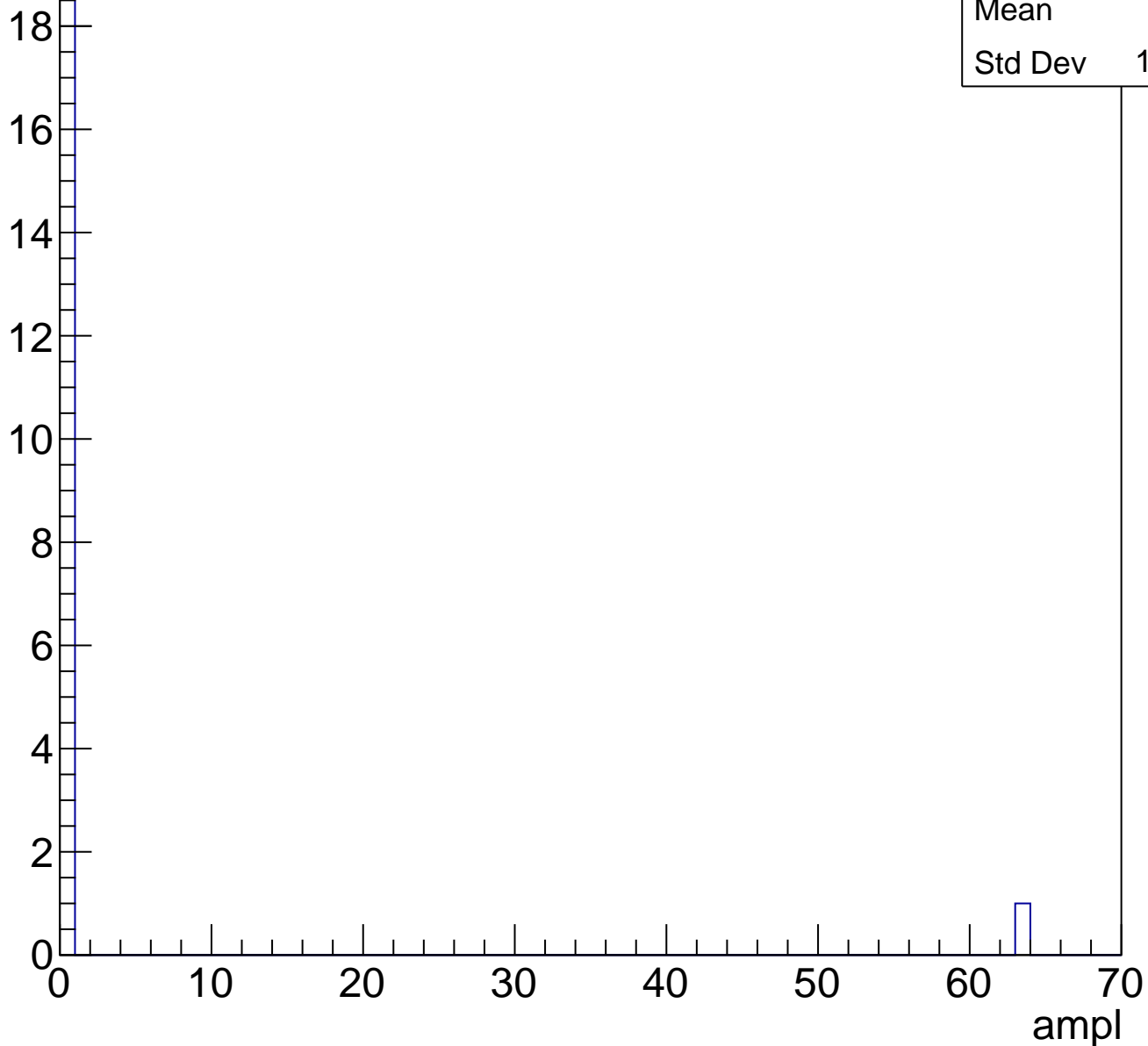




# B1L103S, U4-ch48, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



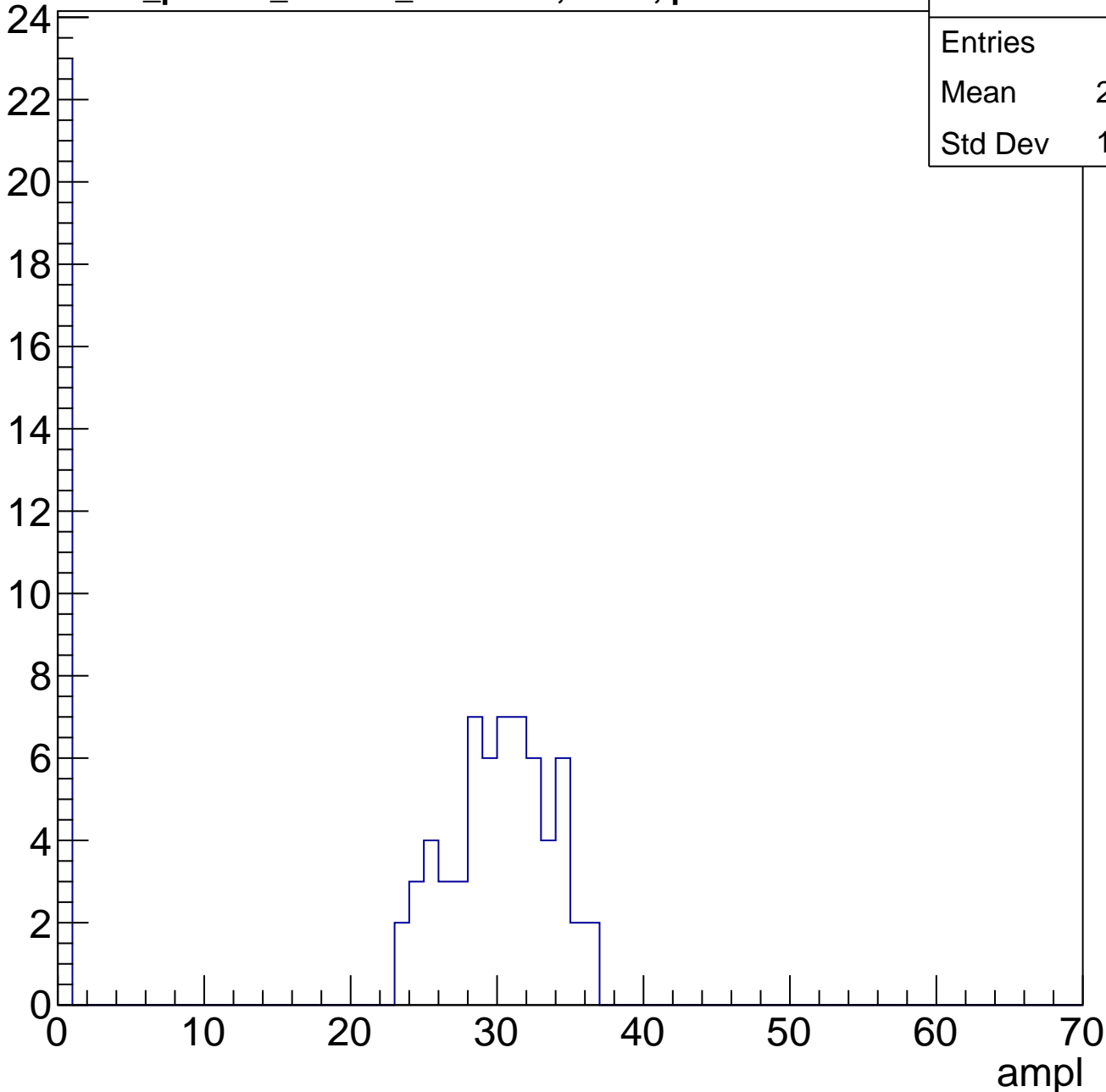
|         |       |
|---------|-------|
| Entries | 20    |
| Mean    | 3.15  |
| Std Dev | 13.73 |

# B1L103S, U4-ch49, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 85    |
| Mean    | 21.69 |
| Std Dev | 13.52 |

Entry

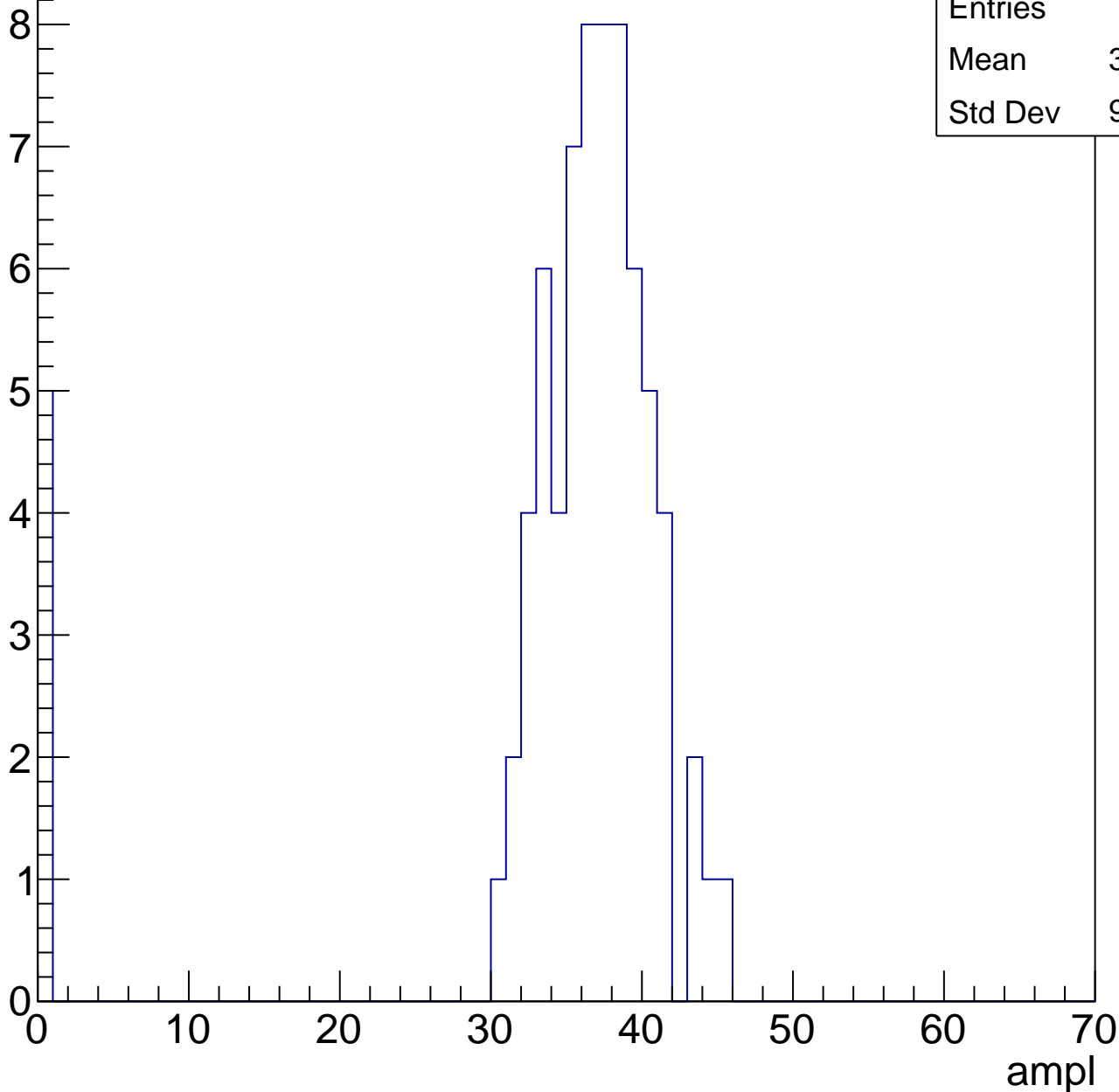


# B1L103S, U4-ch49, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 72    |
| Mean    | 34.17 |
| Std Dev | 9.847 |



# B1L103S, U4-ch49, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

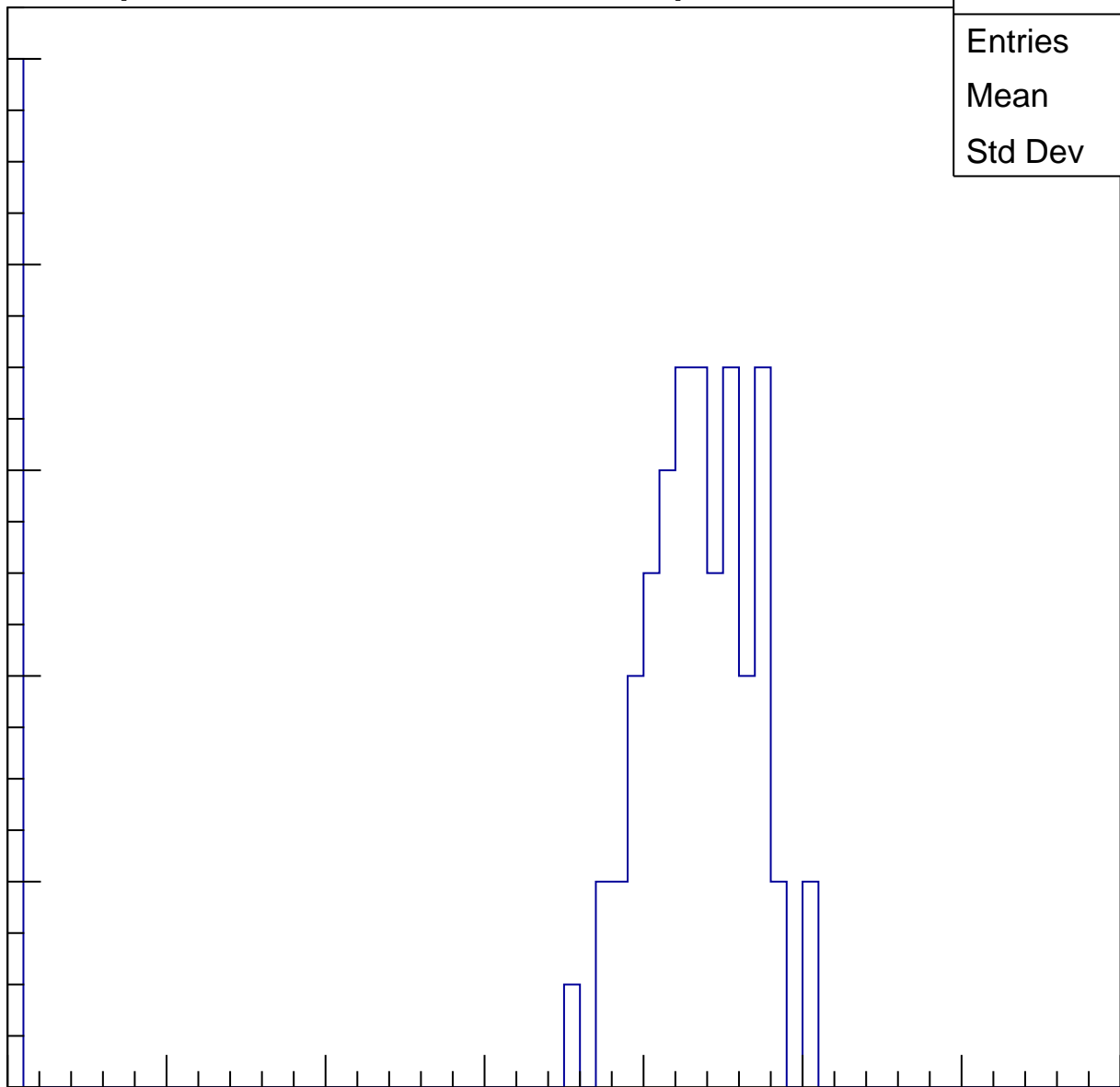
|         |       |
|---------|-------|
| Entries | 71    |
| Mean    | 36.99 |
| Std Dev | 15.28 |

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

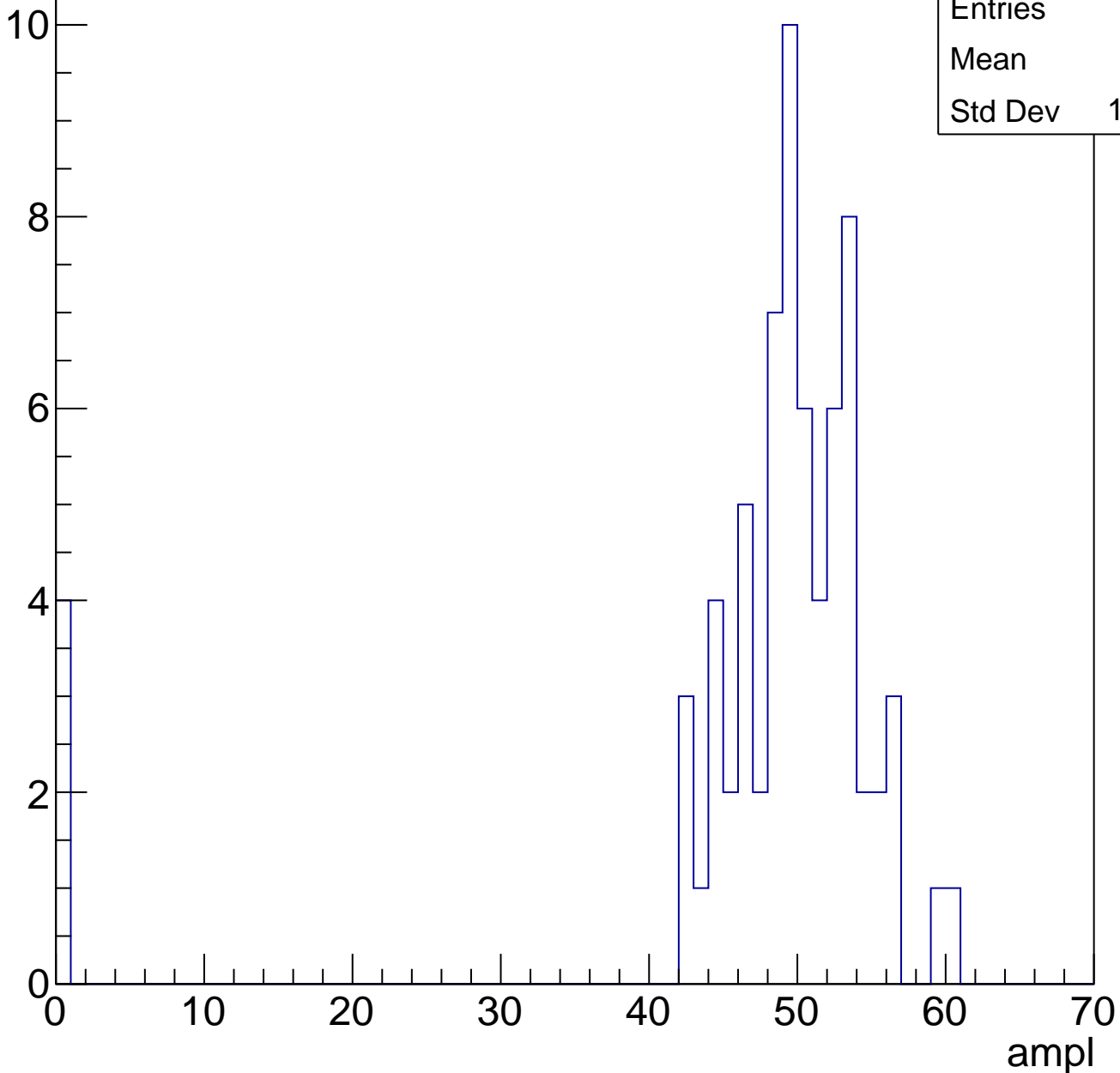


# B1L103S, U4-ch49, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 71    |
| Mean    | 46.9  |
| Std Dev | 12.08 |

Entry

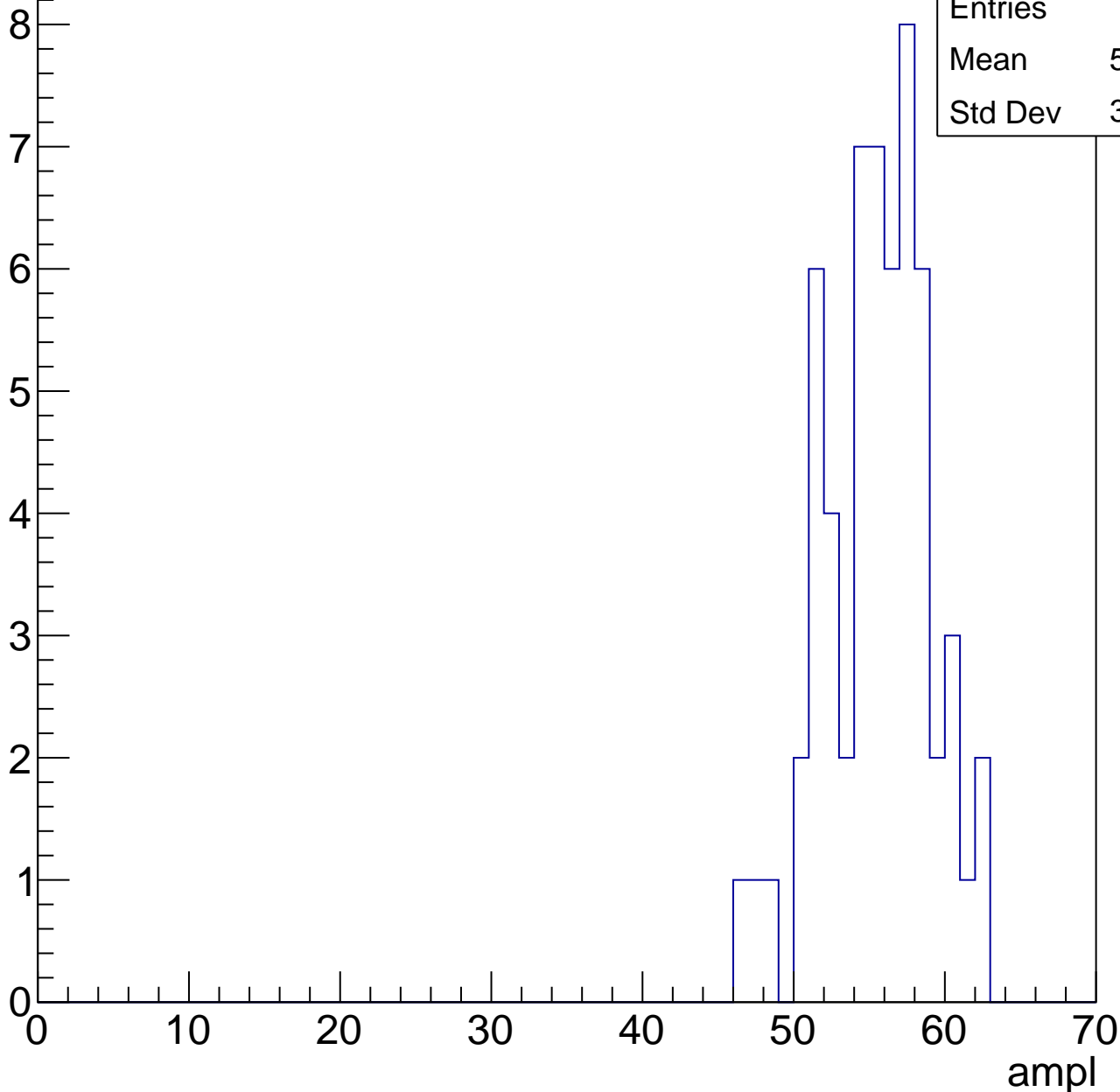


# B1L103S, U4-ch49, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 59    |
| Mean    | 55.03 |
| Std Dev | 3.503 |

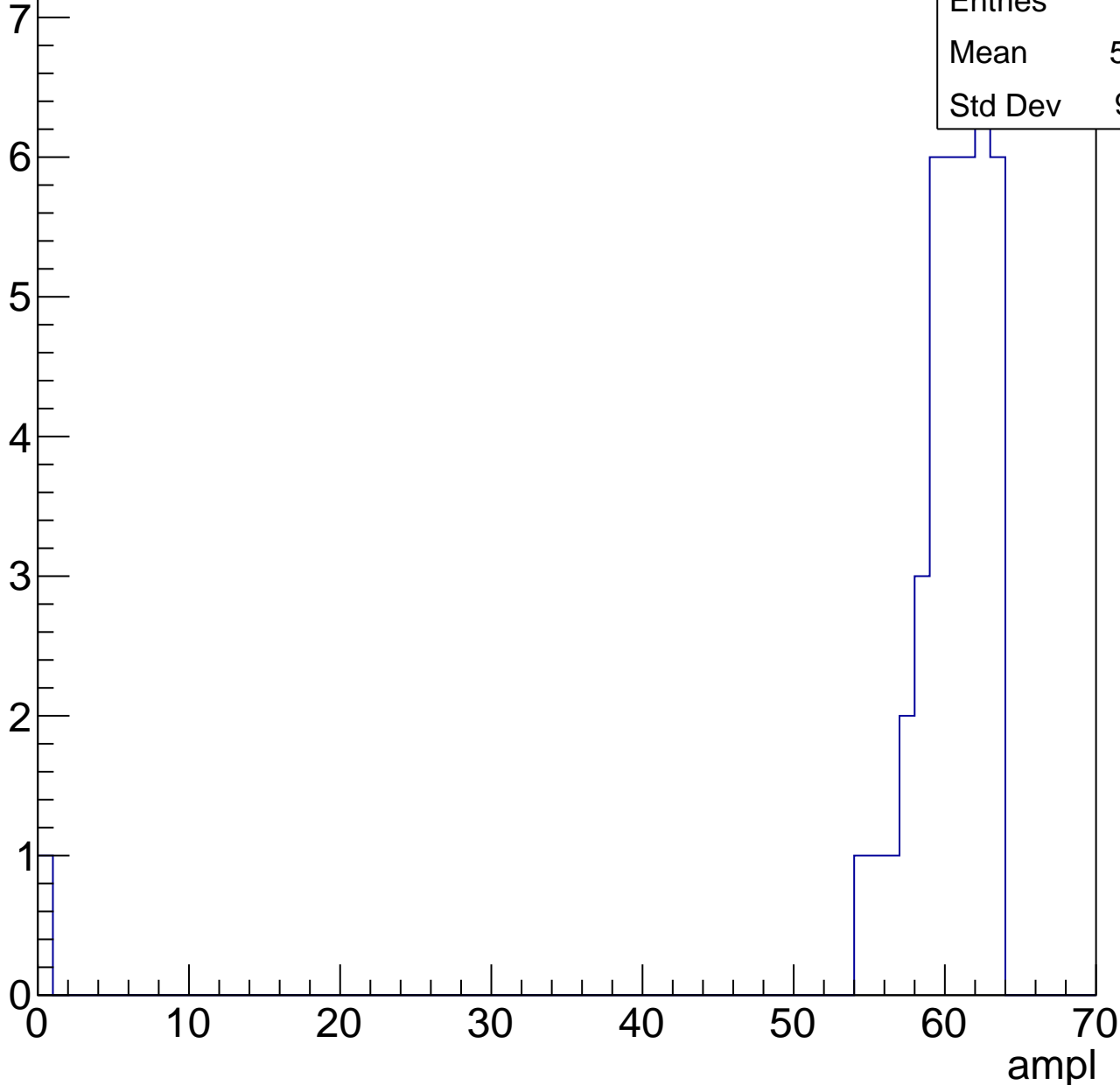


# B1L103S, U4-ch49, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

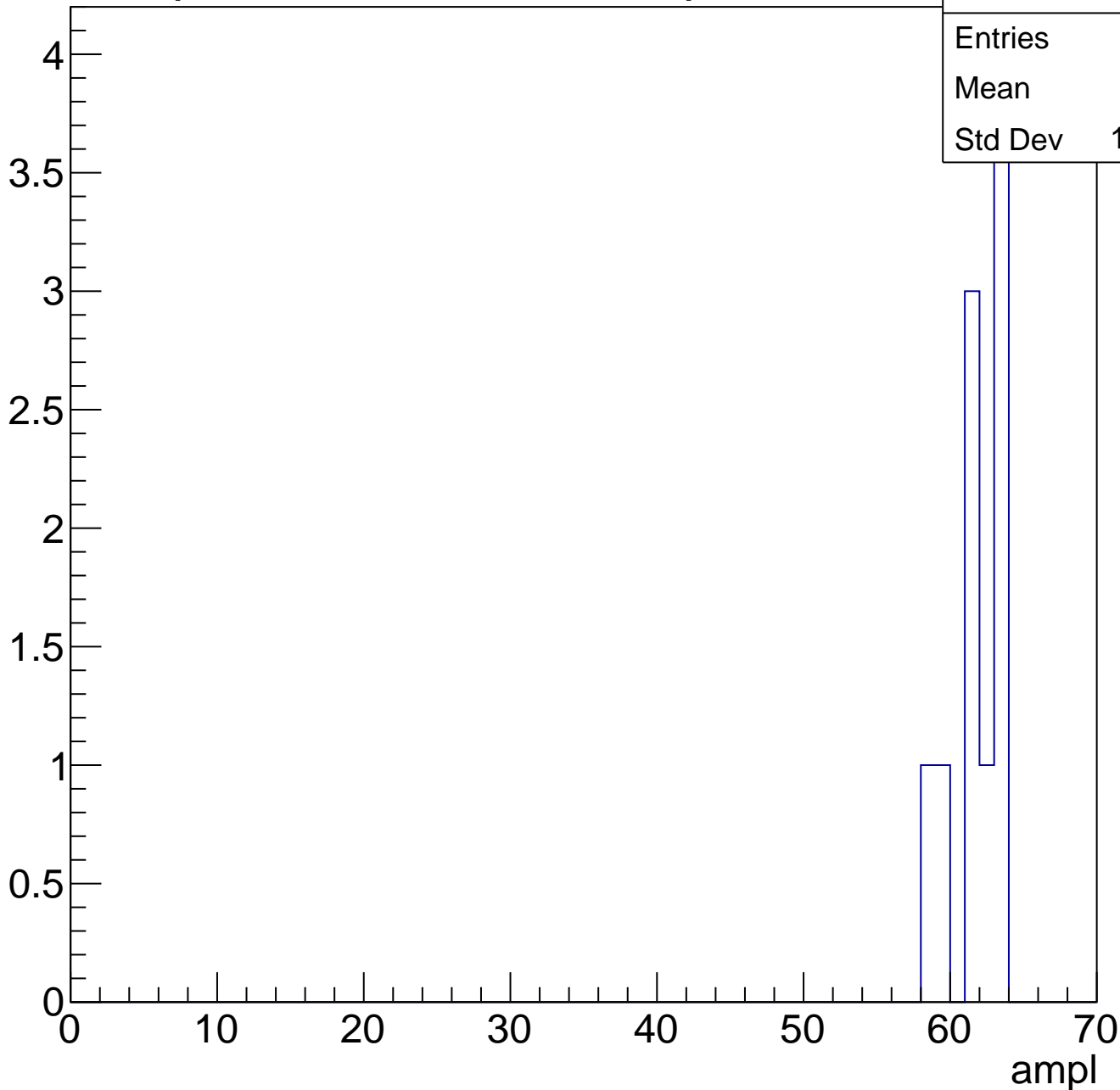
|         |       |
|---------|-------|
| Entries | 40    |
| Mean    | 58.62 |
| Std Dev | 9.651 |



# B1L103S, U4-ch49, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U4-ch49, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

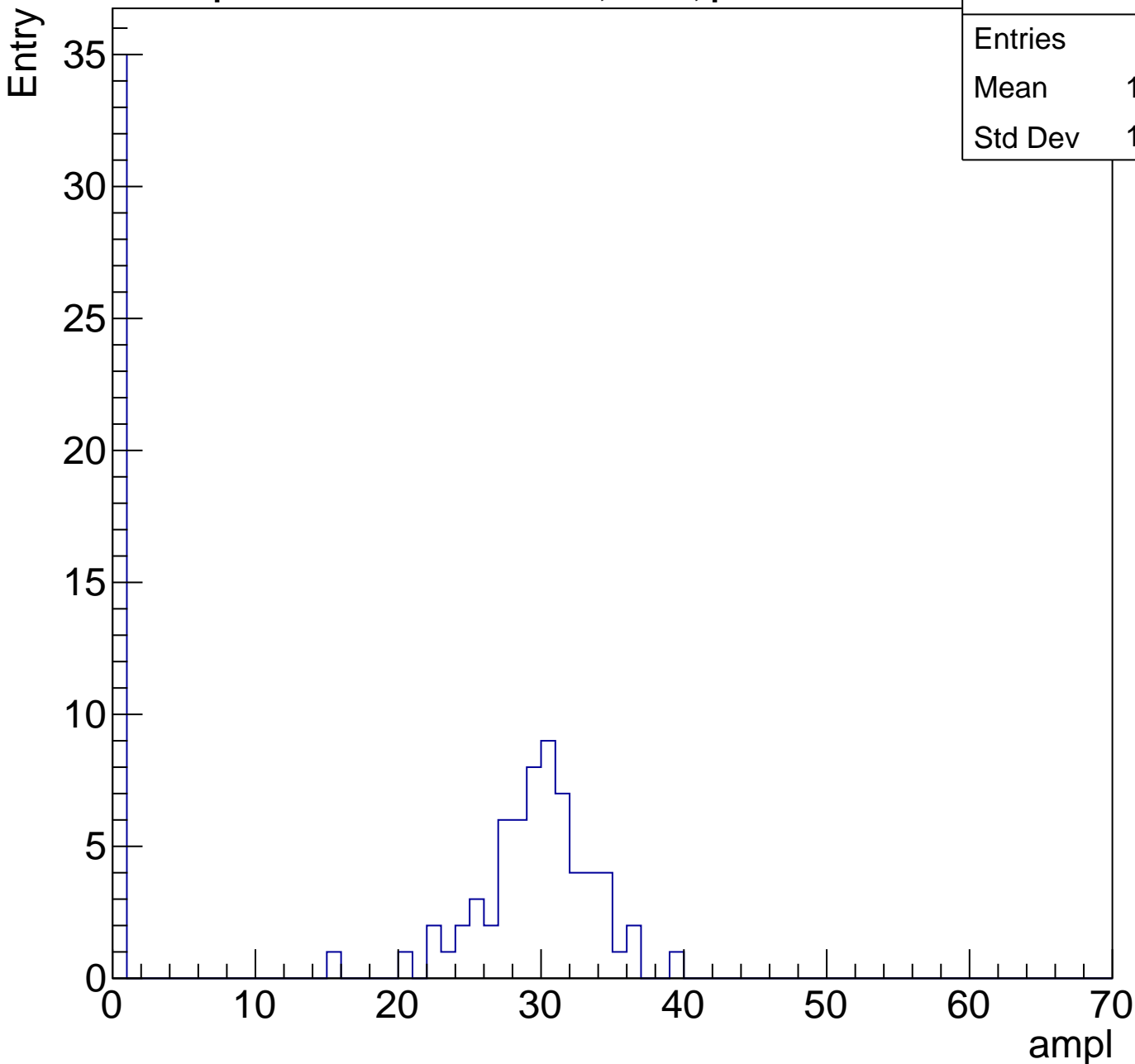
Entry



# B1L103S, U4-ch50, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 99    |
| Mean    | 18.87 |
| Std Dev | 14.32 |

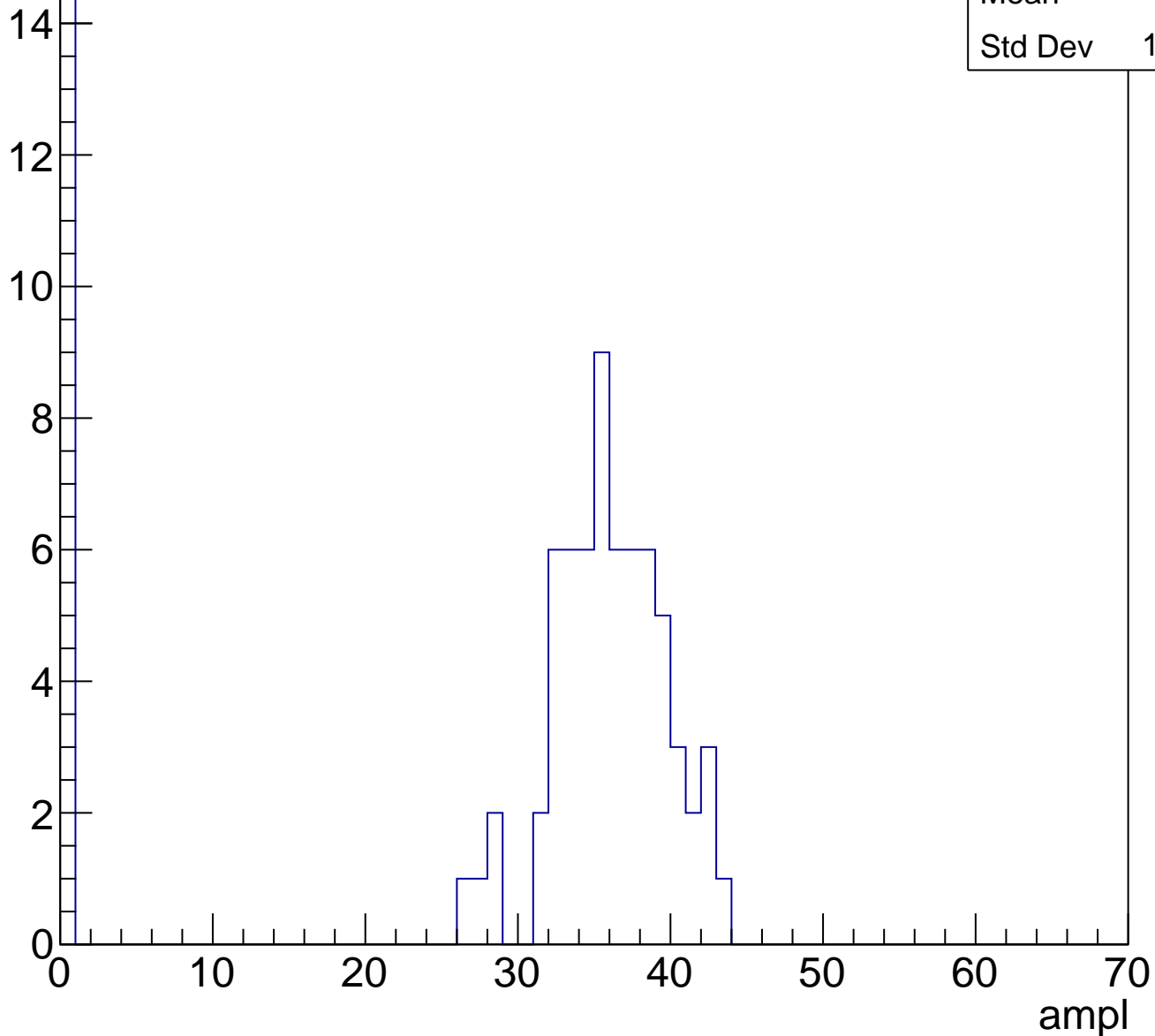


# B1L103S, U4-ch50, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 80    |
| Mean    | 28.9  |
| Std Dev | 14.26 |

Entry

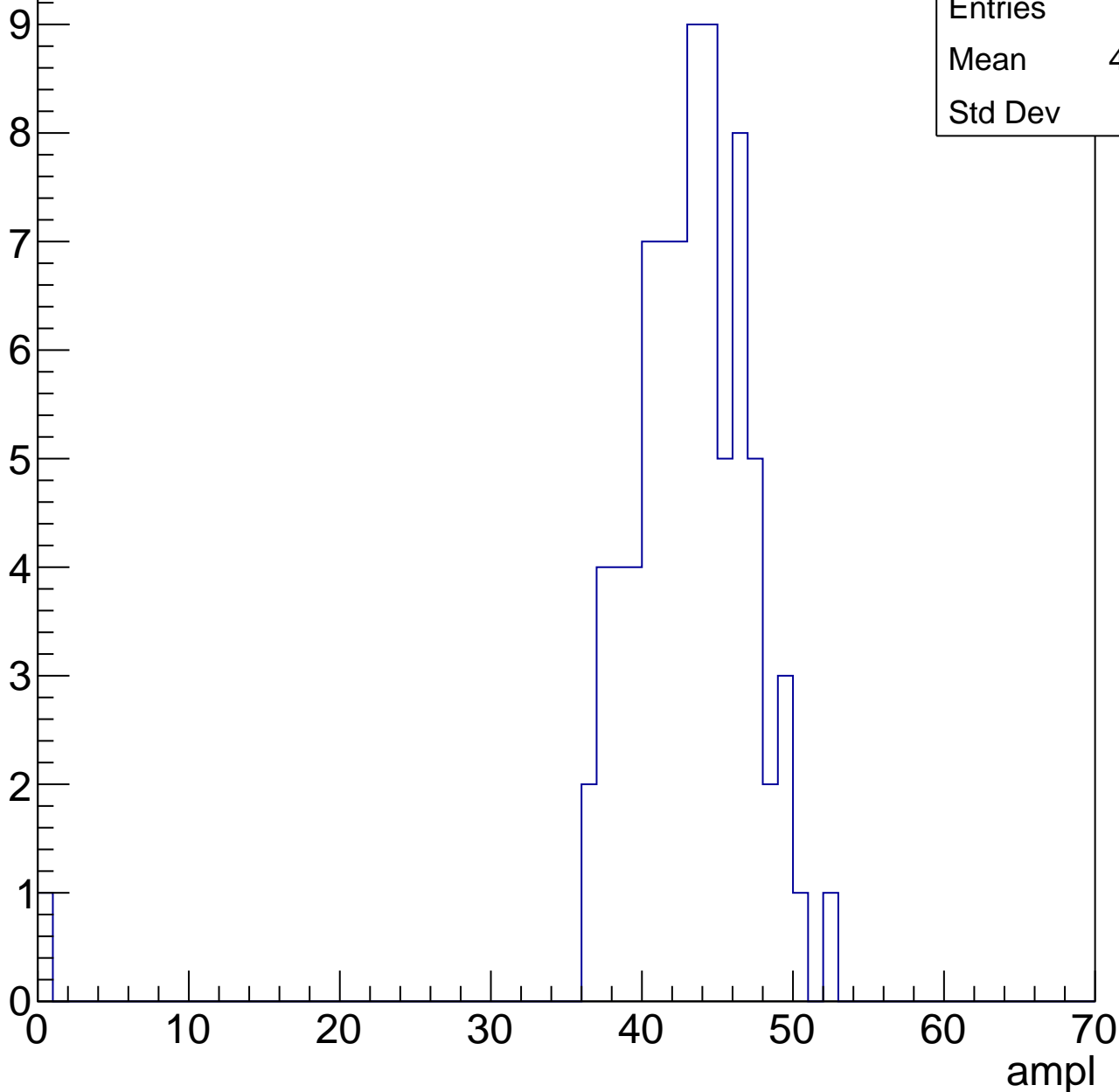


# B1L103S, U4-ch50, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 79    |
| Mean    | 42.34 |
| Std Dev | 5.94  |

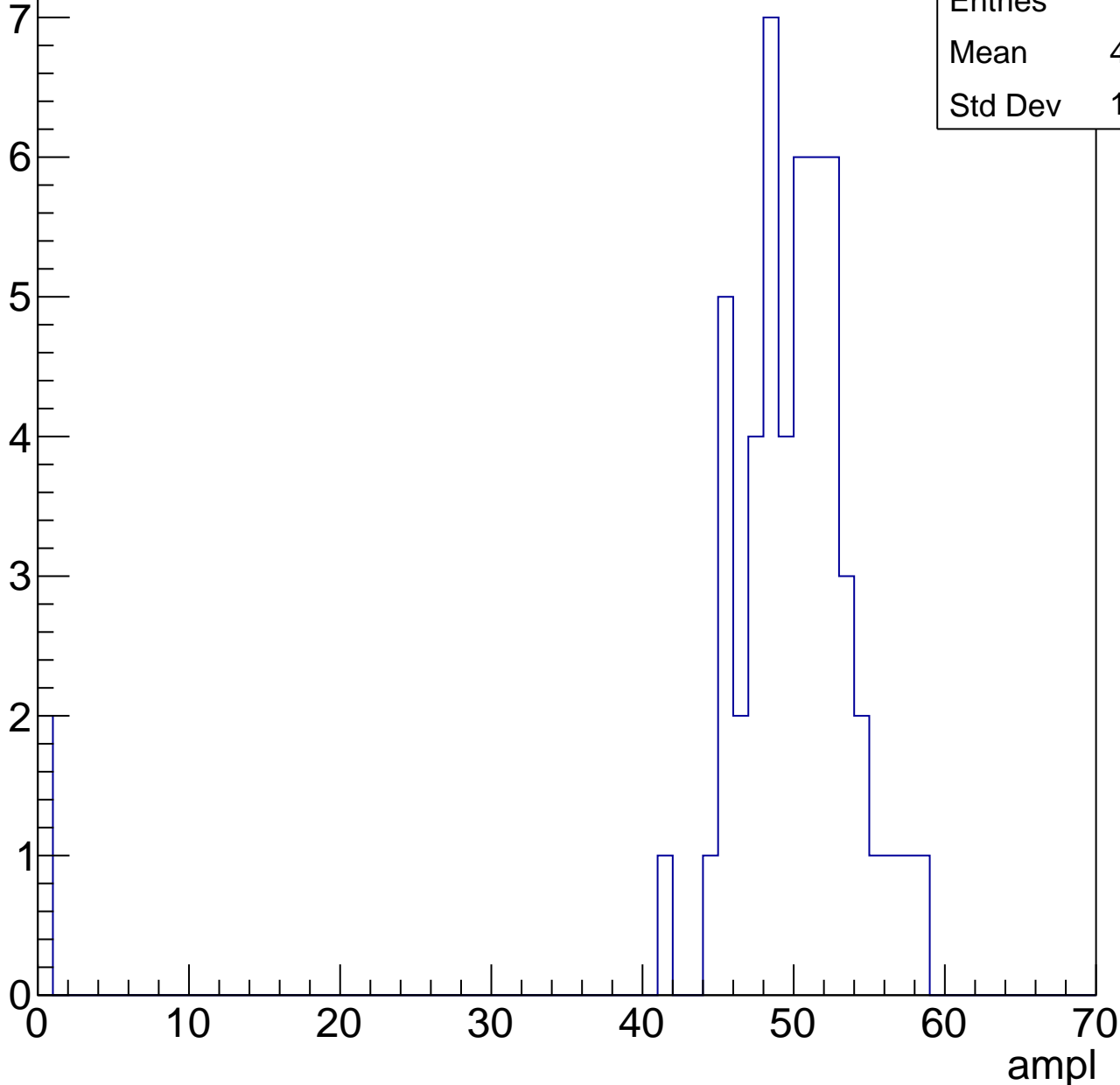


# B1L103S, U4-ch50, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

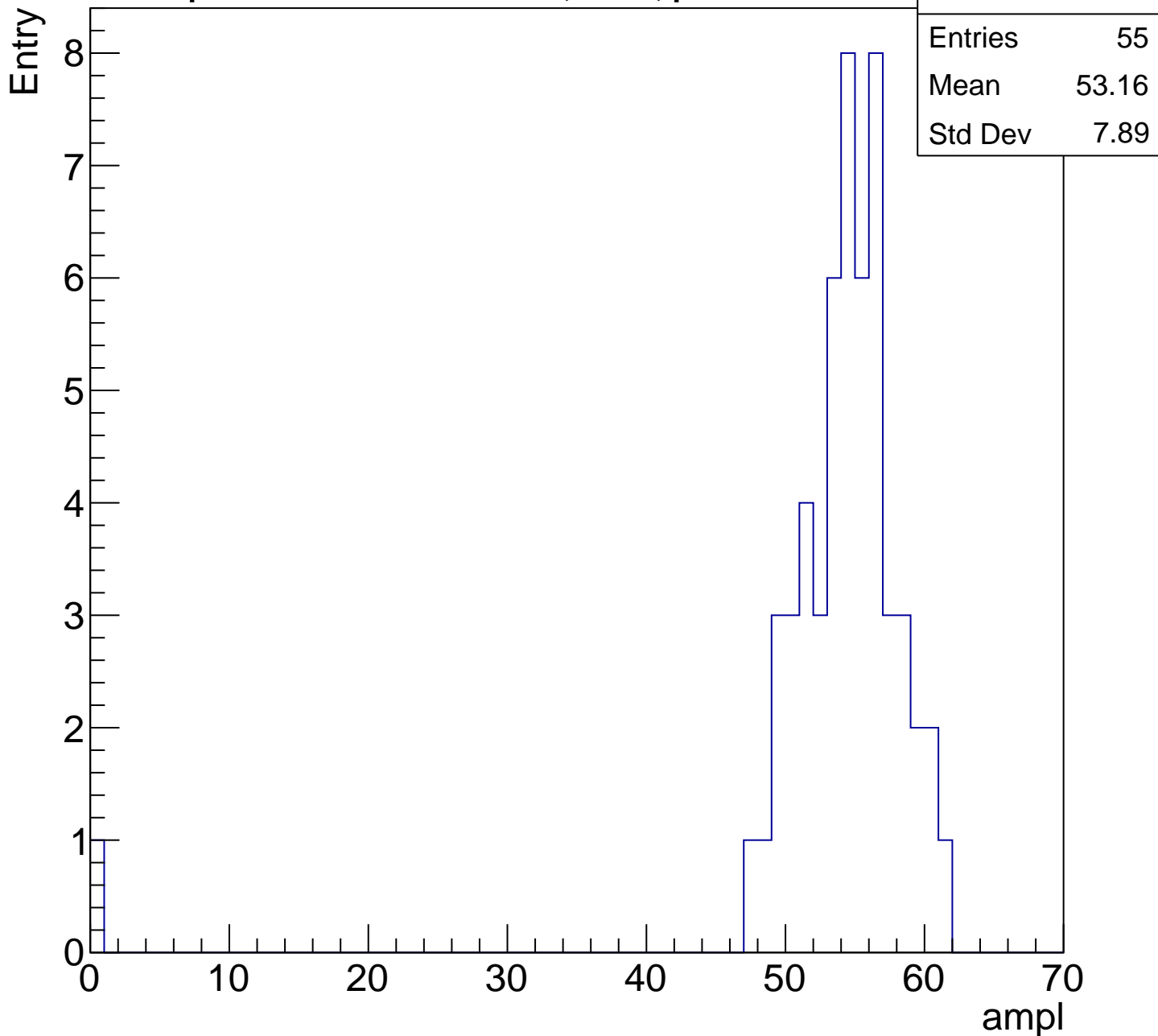
Entry

|         |       |
|---------|-------|
| Entries | 53    |
| Mean    | 47.79 |
| Std Dev | 10.04 |



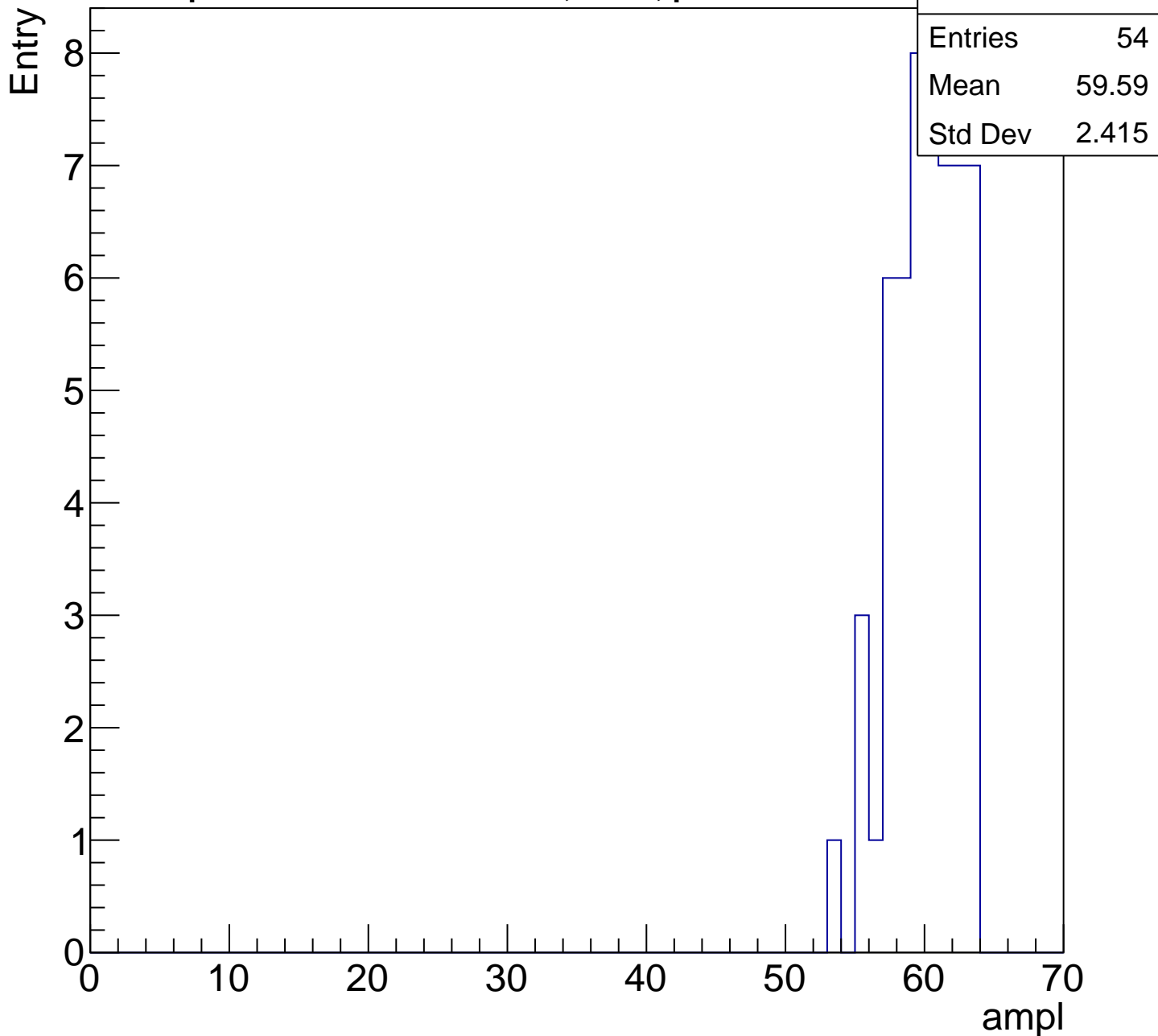
# B1L103S, U4-ch50, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2



# B1L103S, U4-ch50, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2



# B1L103S, U4-ch50, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

3

2.5

2

1.5

1

0.5

0

Entries

9

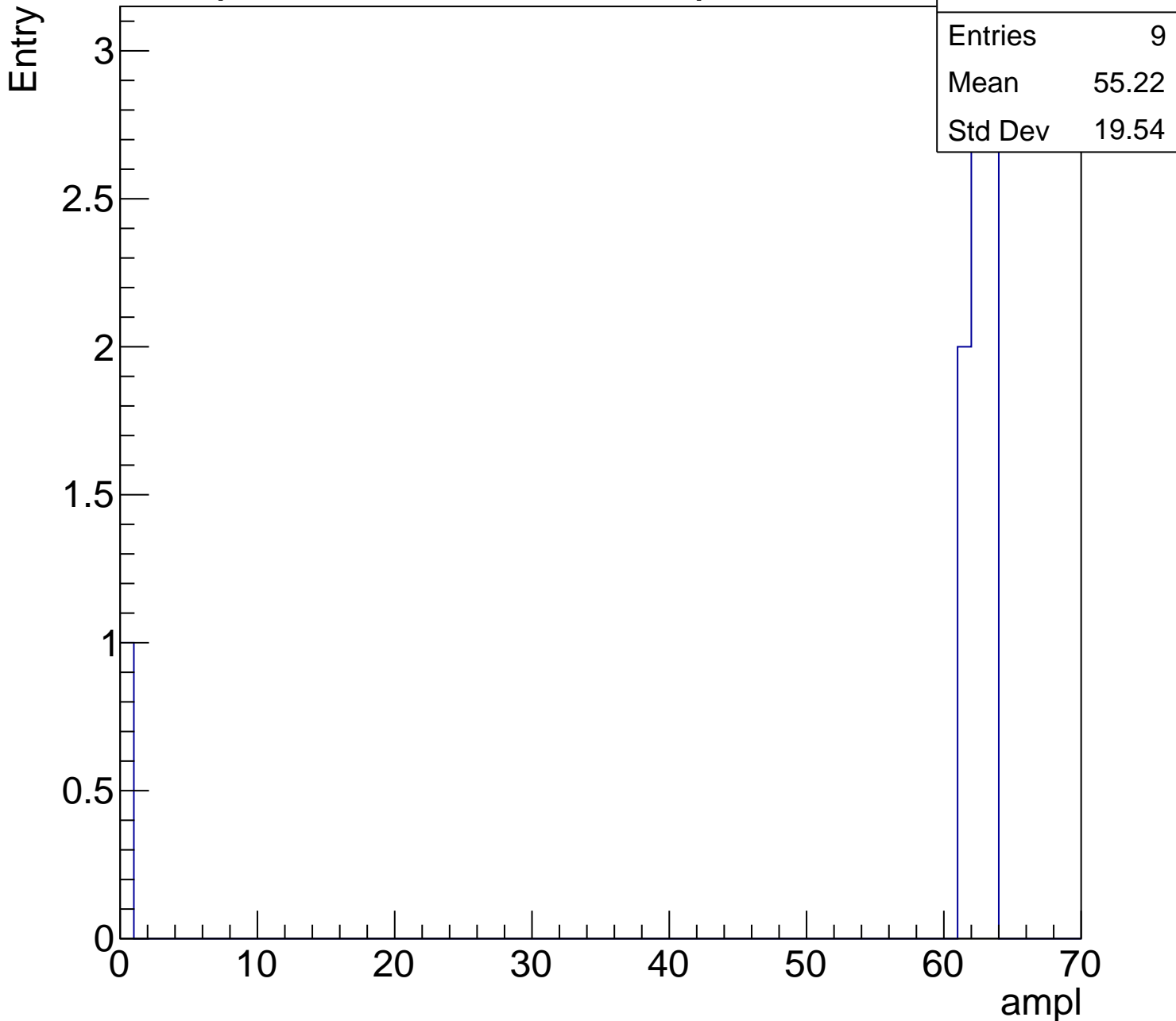
Mean

55.22

Std Dev

19.54

ampl





# B1L103S, U4-ch50, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

|         |    |
|---------|----|
| Entries | 19 |
| Mean    | 0  |
| Std Dev | 0  |

# B1L103S, U4-ch51, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

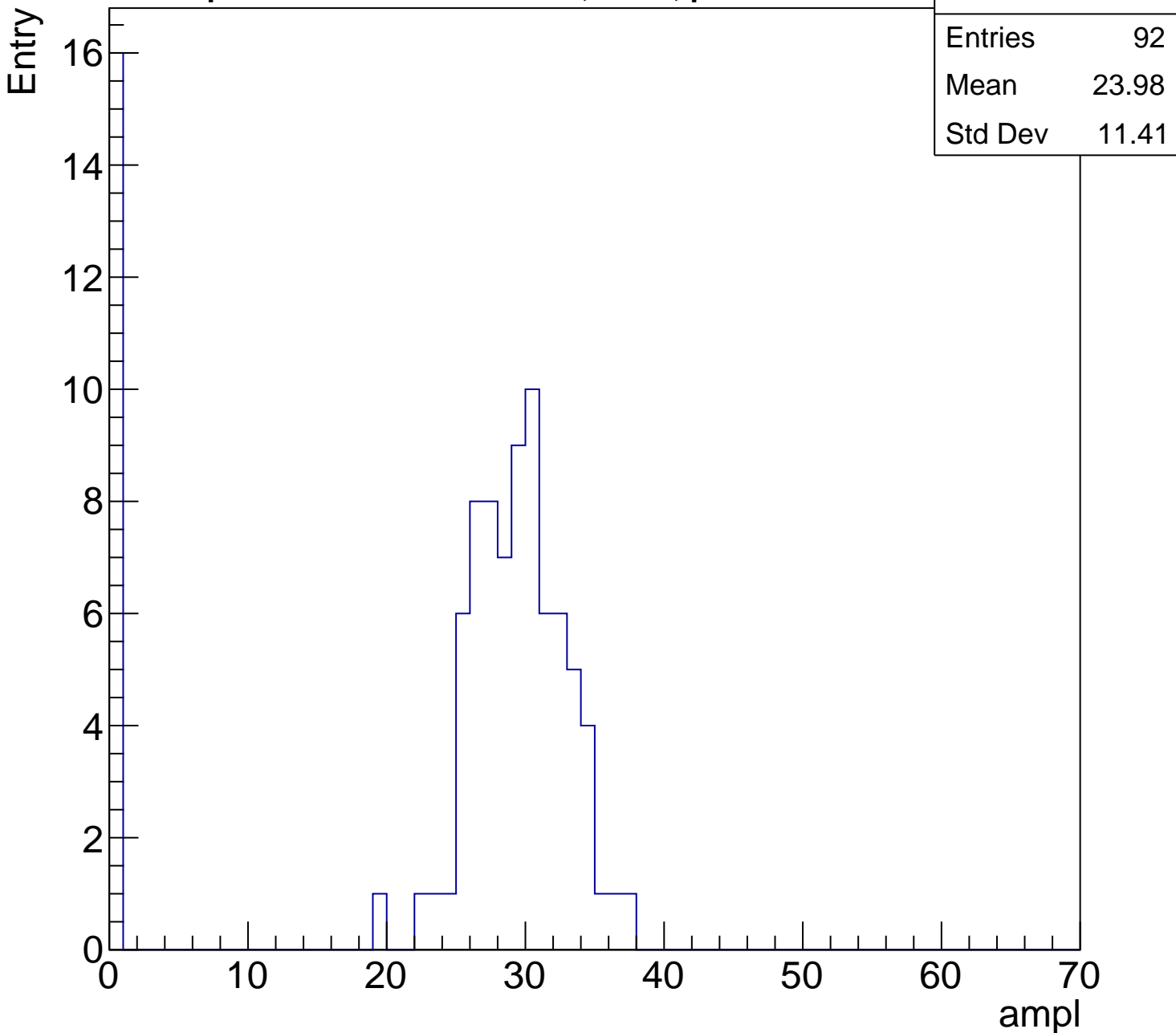
|         |       |
|---------|-------|
| Entries | 92    |
| Mean    | 23.98 |
| Std Dev | 11.41 |

Entry

16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

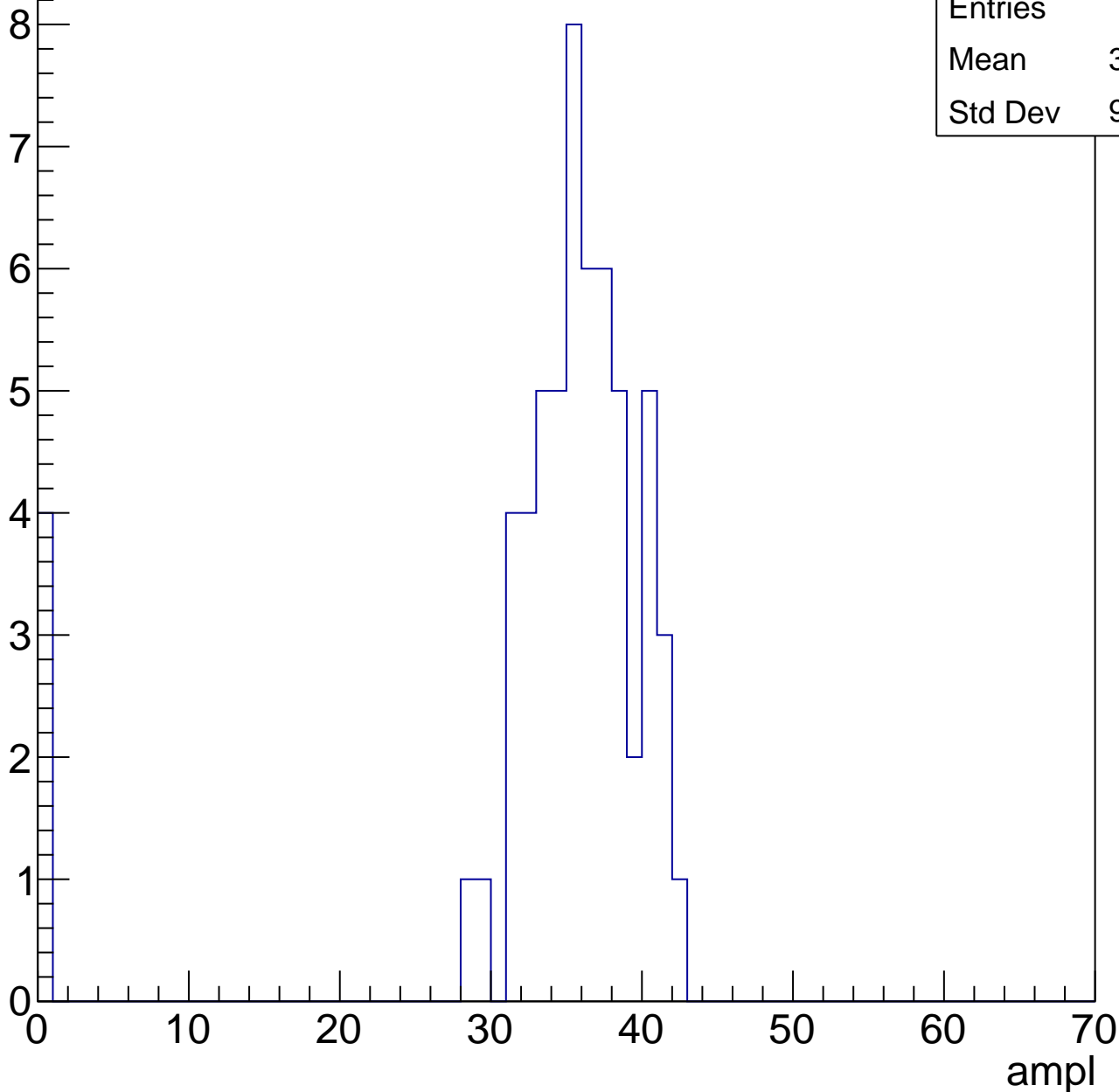


# B1L103S, U4-ch51, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 60    |
| Mean    | 33.25 |
| Std Dev | 9.412 |

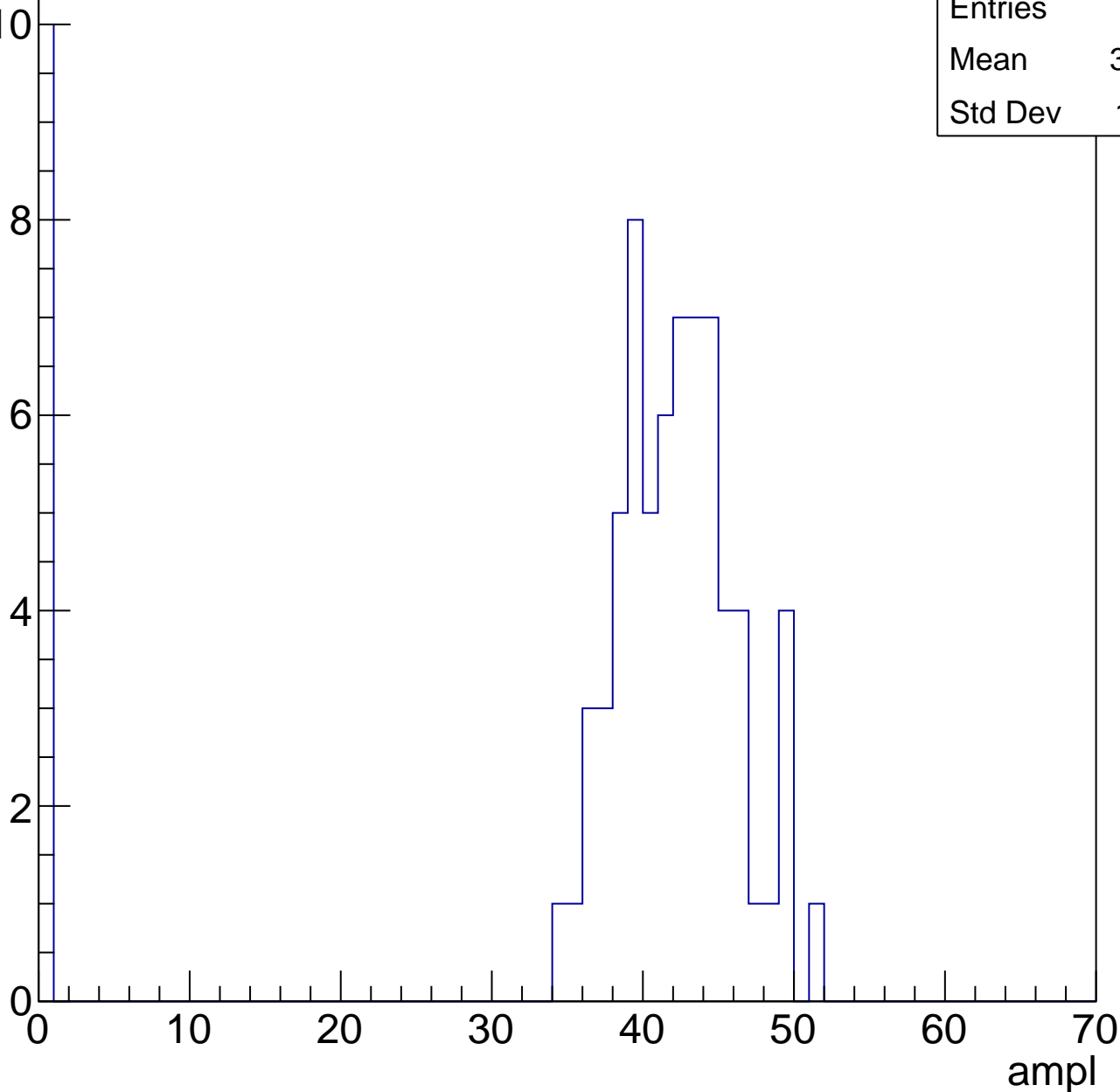


# B1L103S, U4-ch51, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 78    |
| Mean    | 36.47 |
| Std Dev | 14.41 |

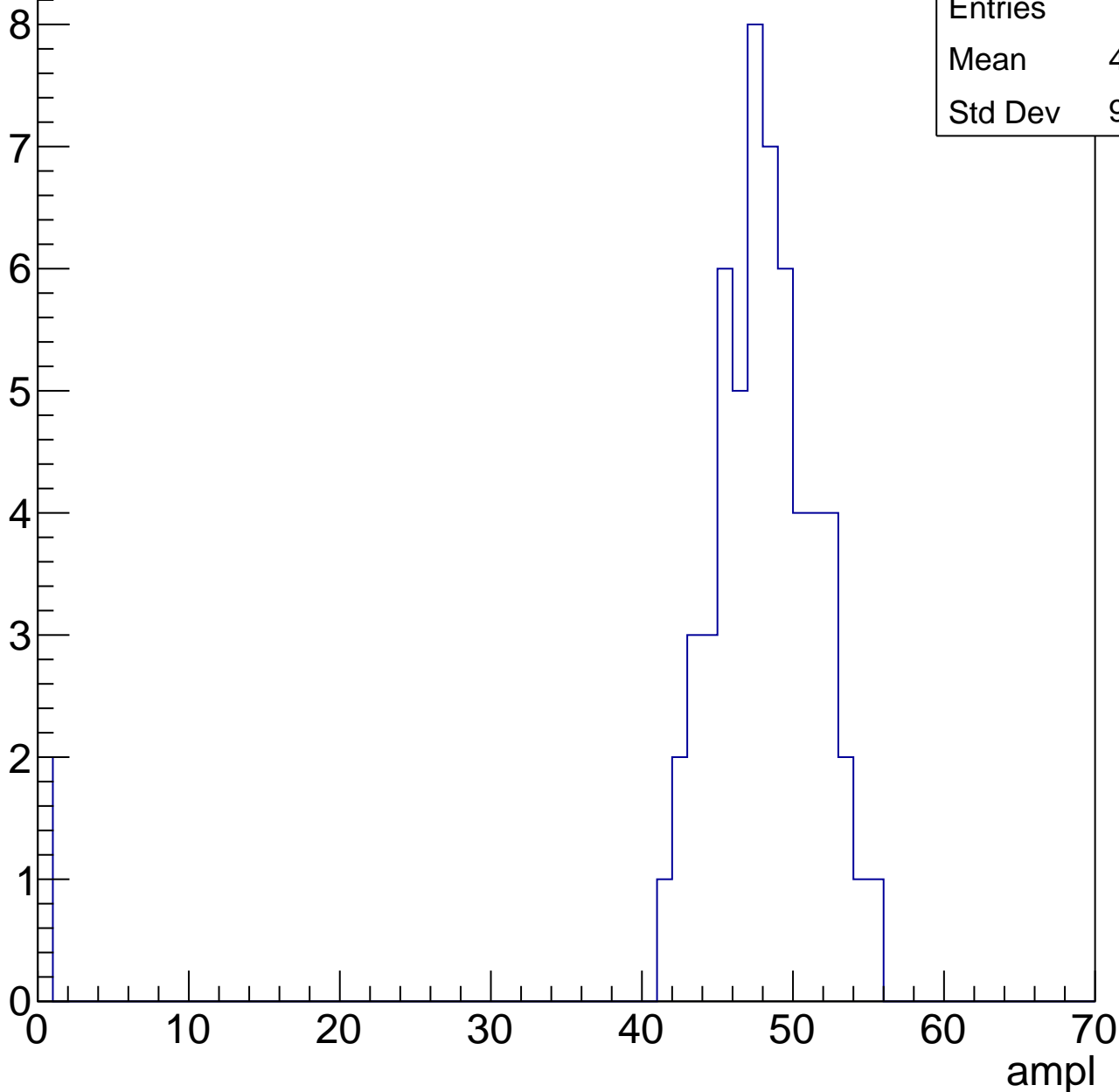


# B1L103S, U4-ch51, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 59    |
| Mean    | 46.08 |
| Std Dev | 9.182 |

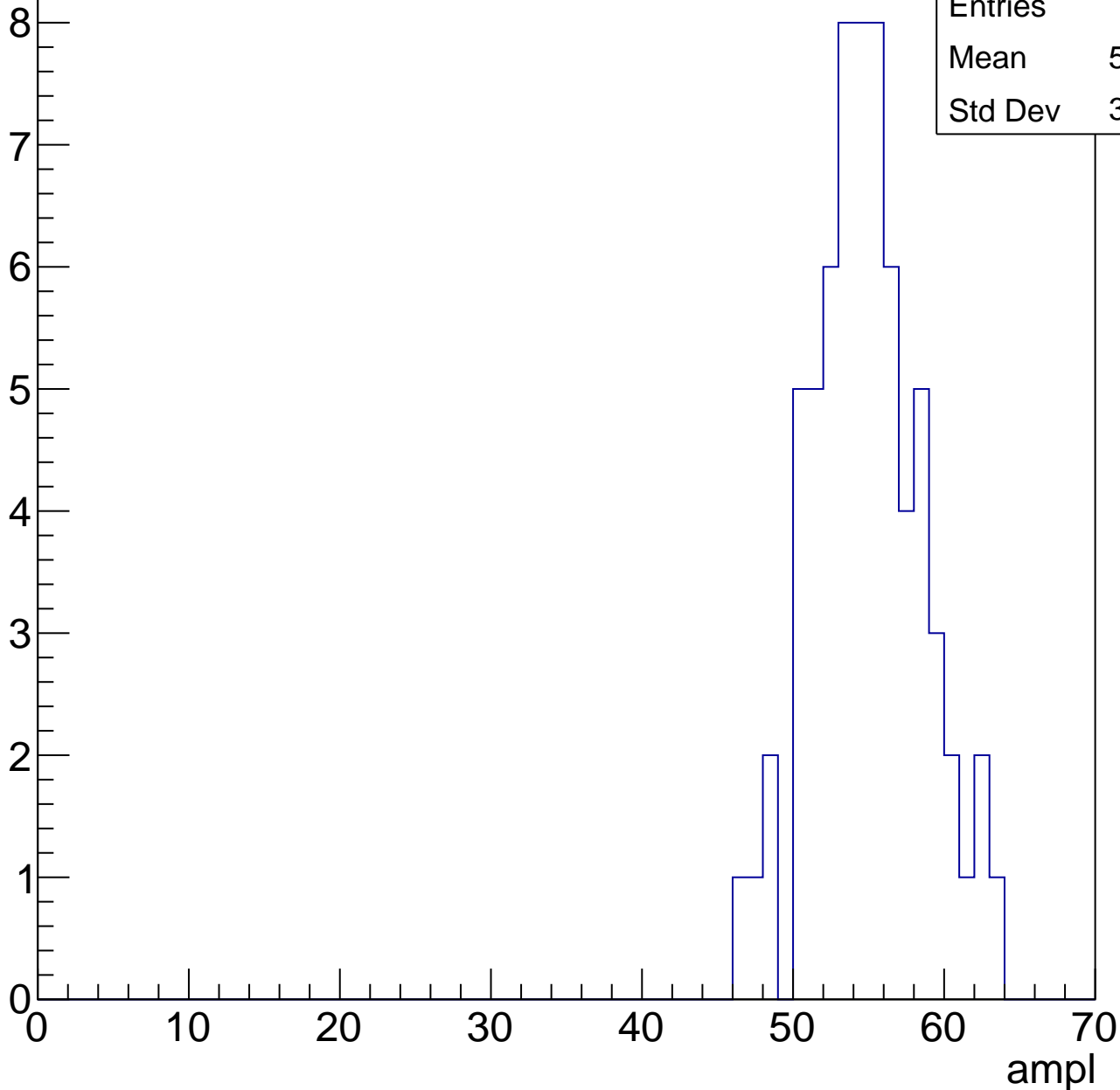


# B1L103S, U4-ch51, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 68    |
| Mean    | 54.43 |
| Std Dev | 3.603 |

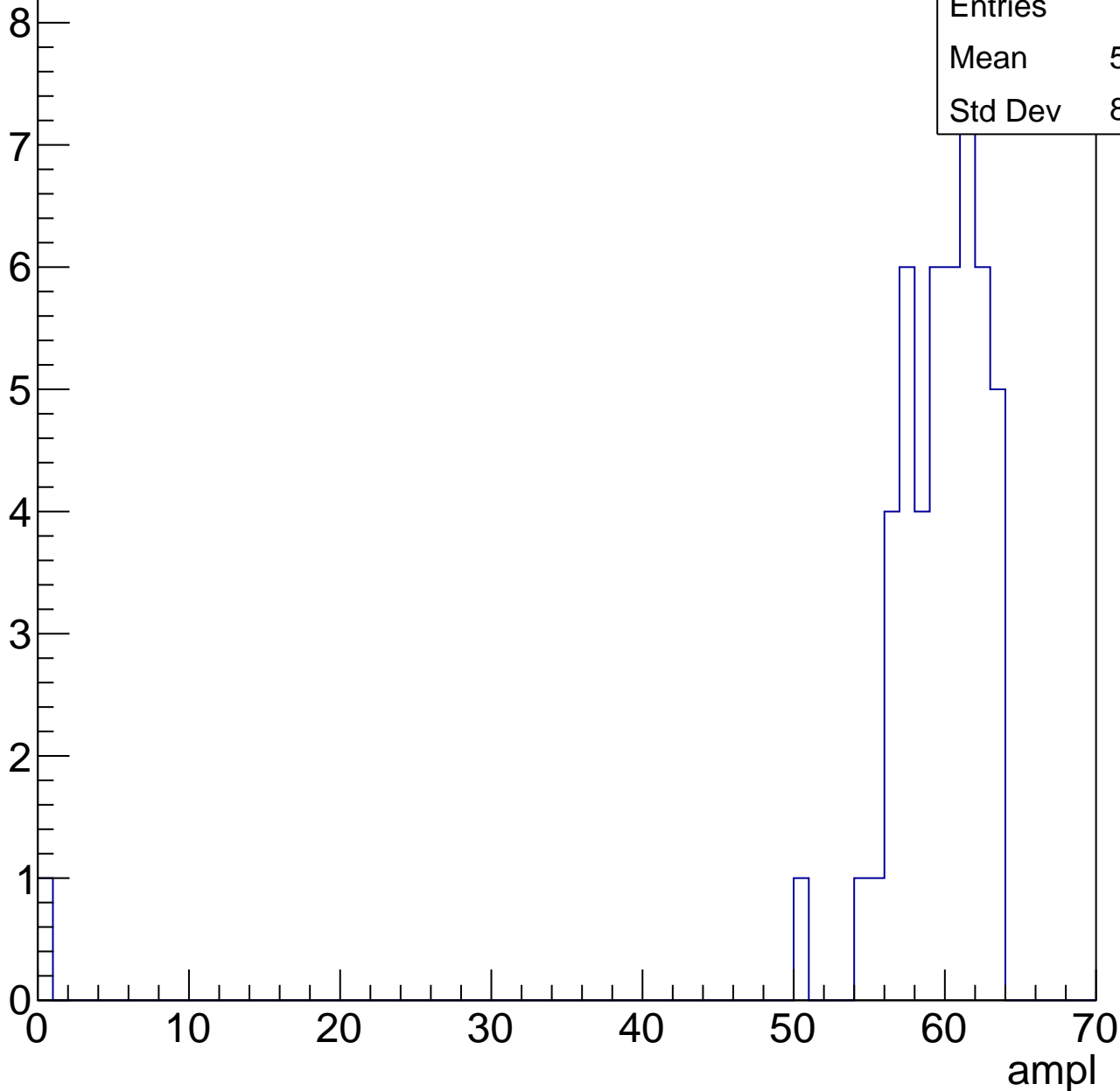


# B1L103S, U4-ch51, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

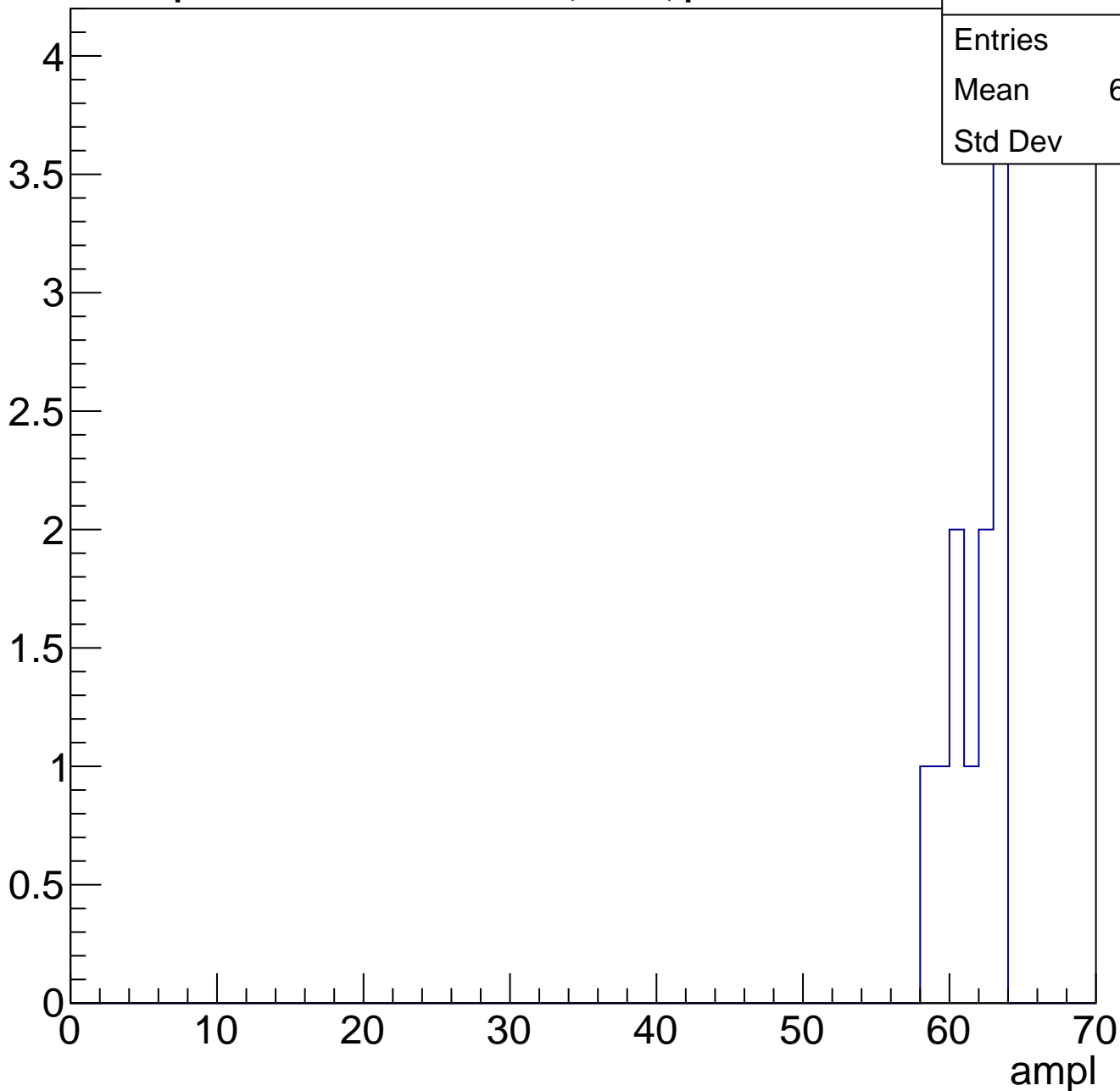
|         |       |
|---------|-------|
| Entries | 49    |
| Mean    | 58.08 |
| Std Dev | 8.804 |



# B1L103S, U4-ch51, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U4-ch51, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U4-ch52, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

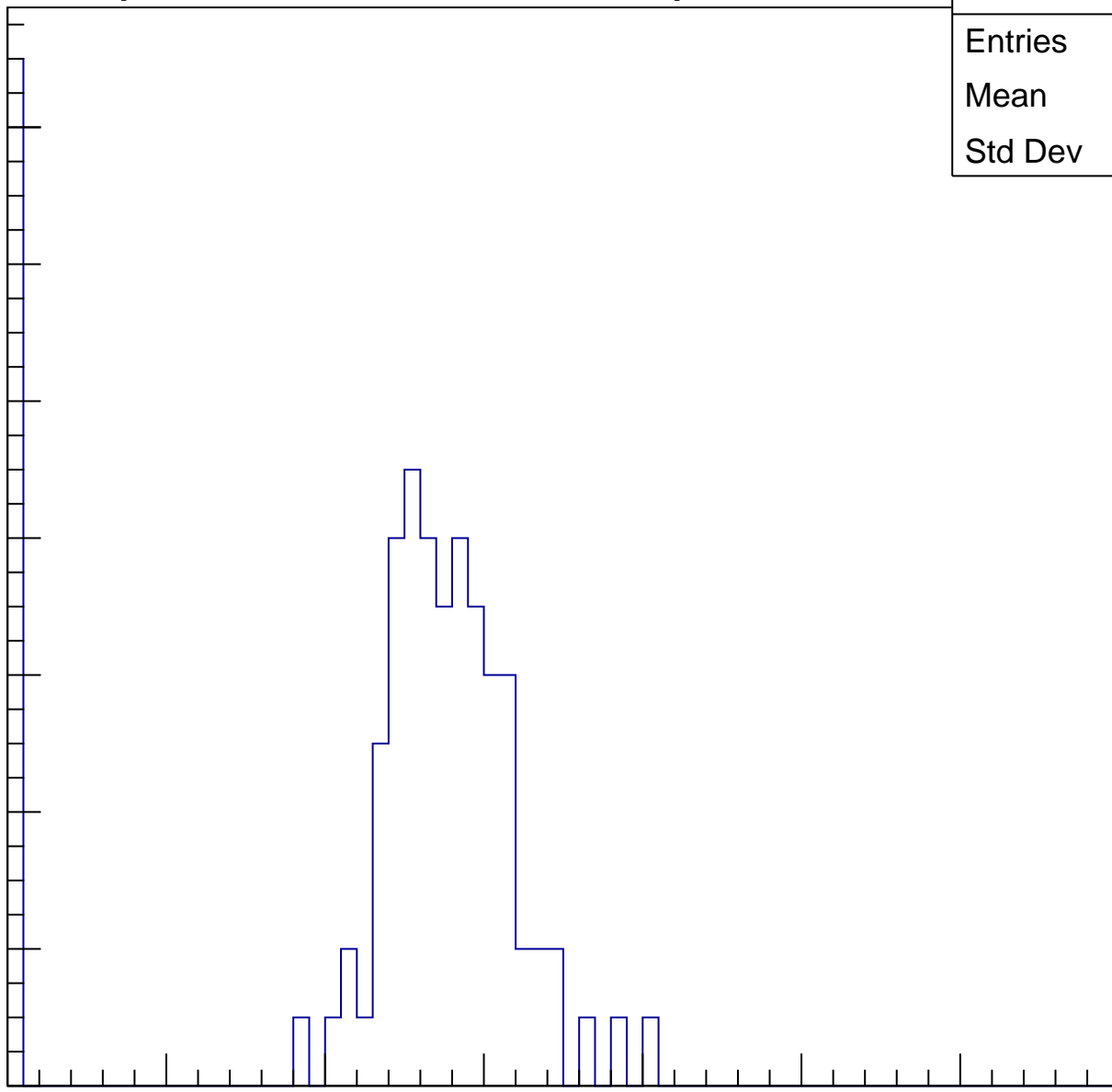
|         |       |
|---------|-------|
| Entries | 93    |
| Mean    | 22.97 |
| Std Dev | 10.69 |

Entry

14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

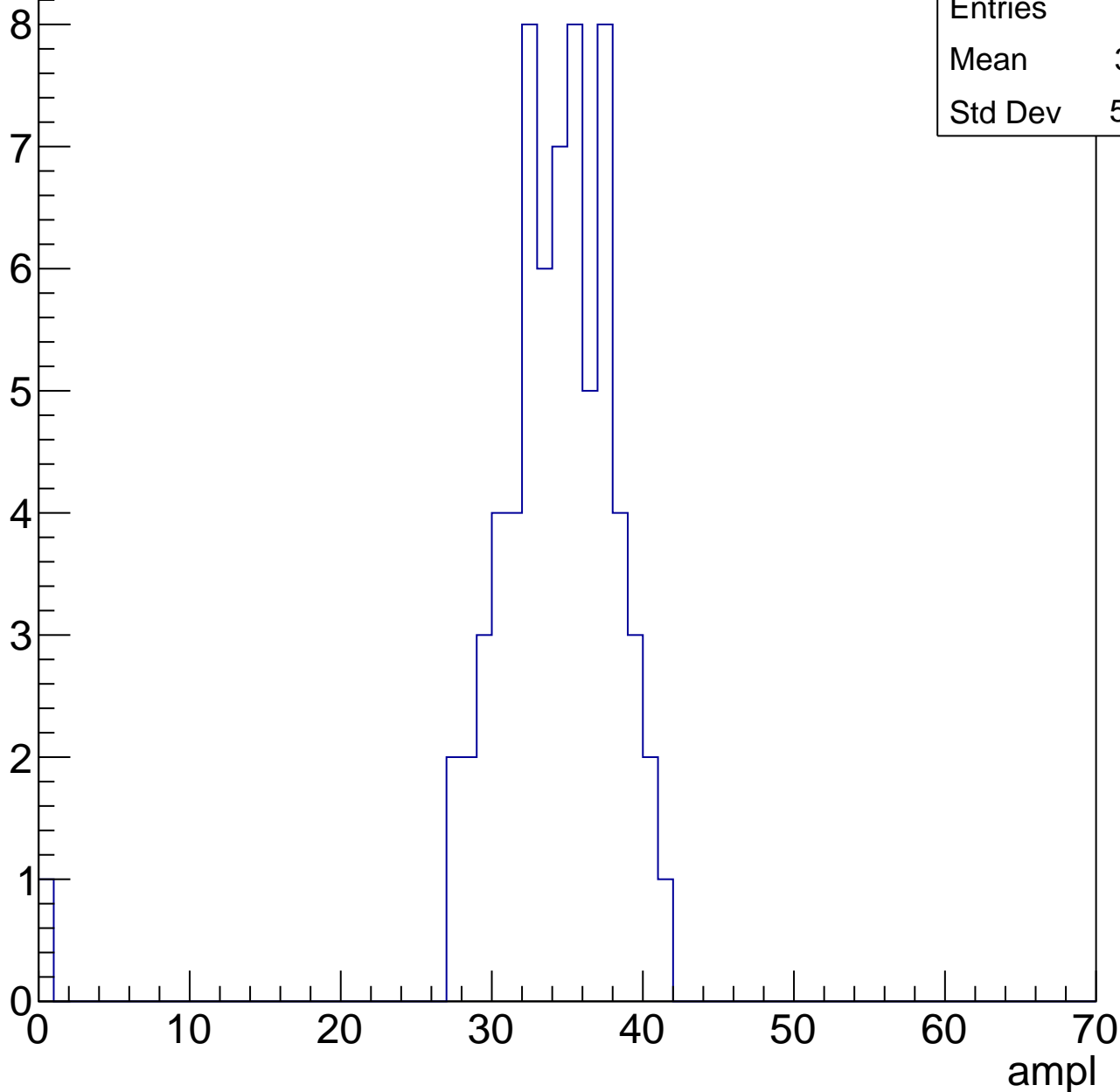


# B1L103S, U4-ch52, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 68    |
| Mean    | 33.51 |
| Std Dev | 5.262 |

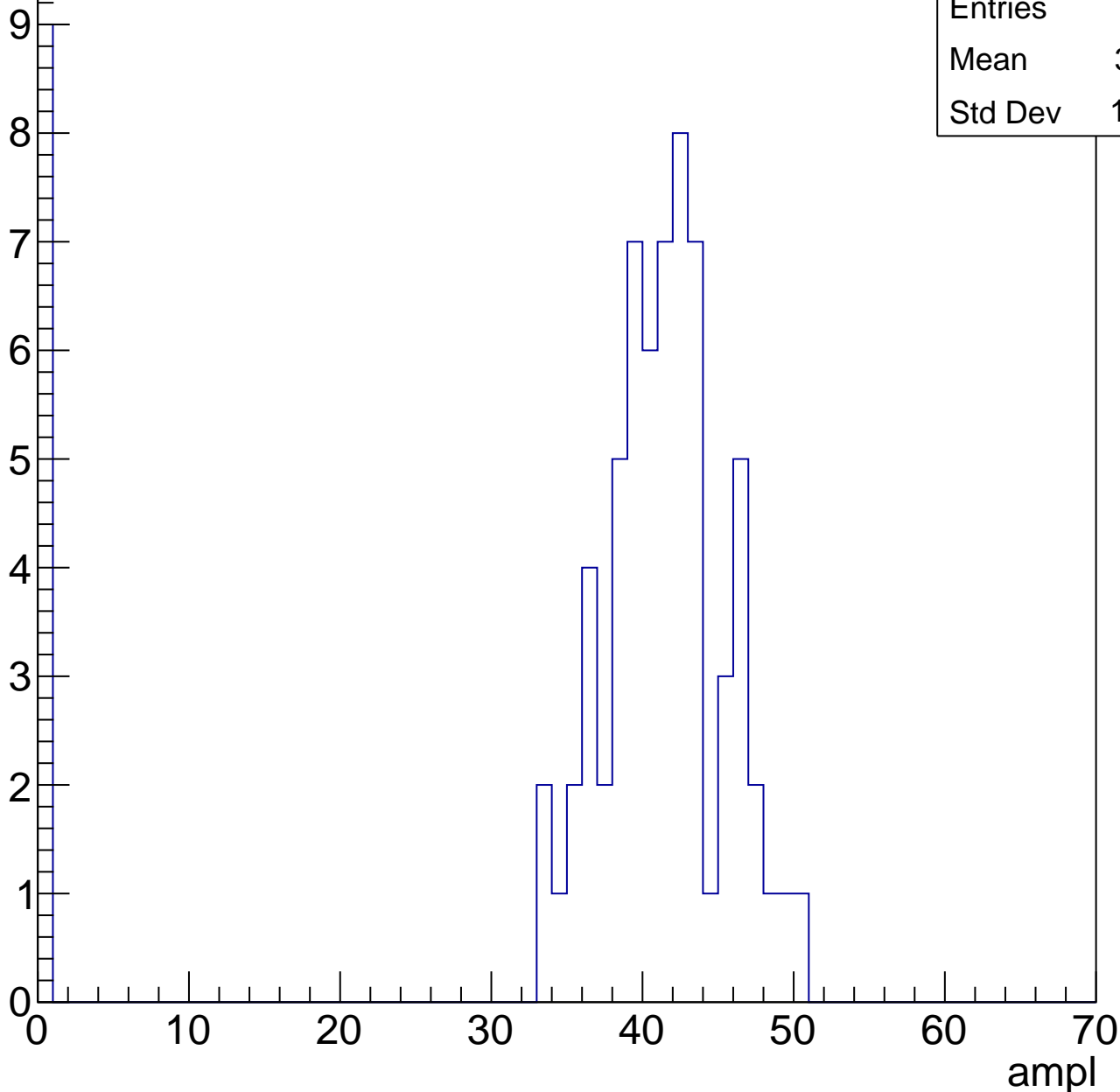


# B1L103S, U4-ch52, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 74    |
| Mean    | 36.01 |
| Std Dev | 13.87 |

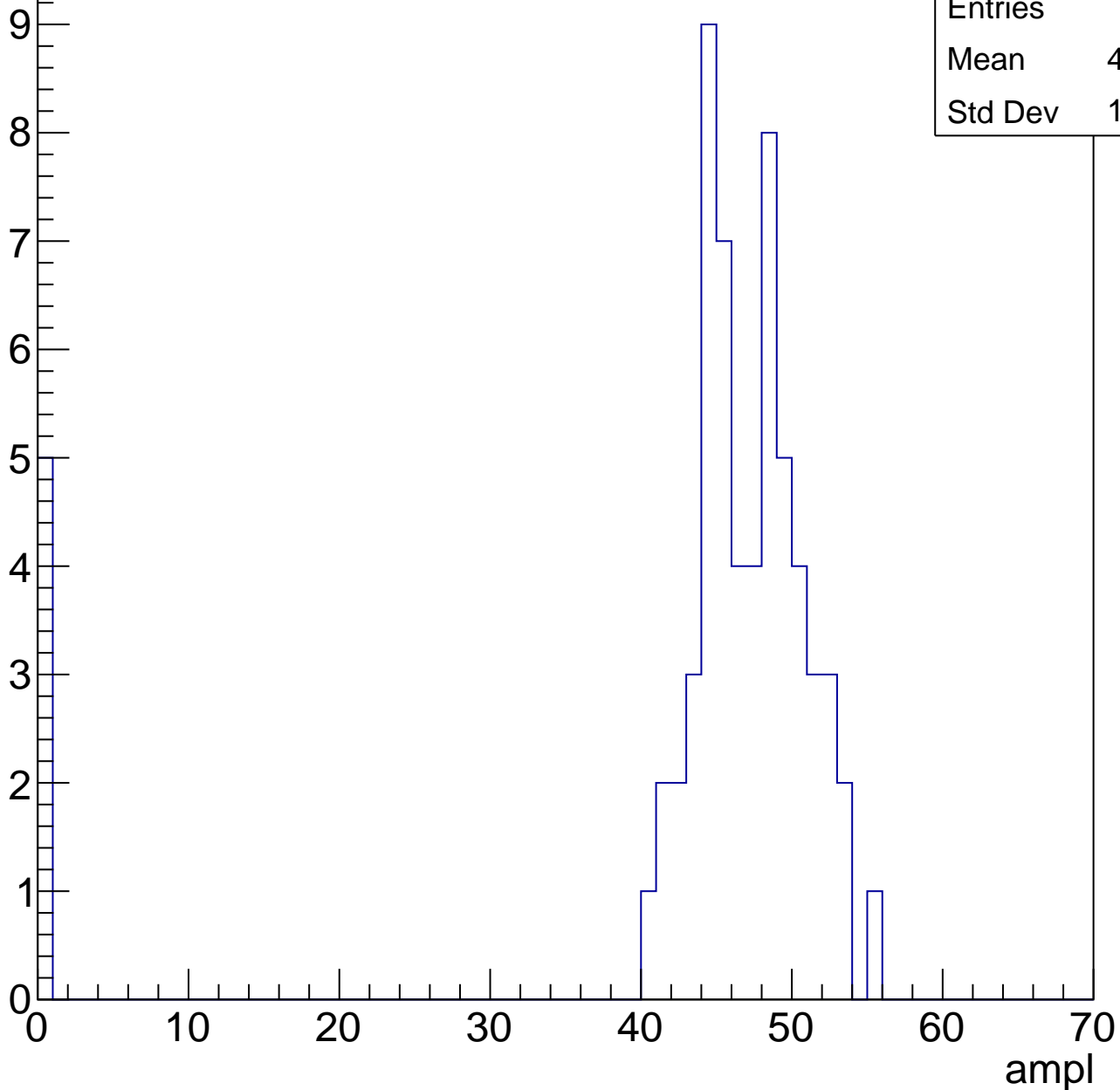


# B1L103S, U4-ch52, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 63    |
| Mean    | 43.13 |
| Std Dev | 13.07 |

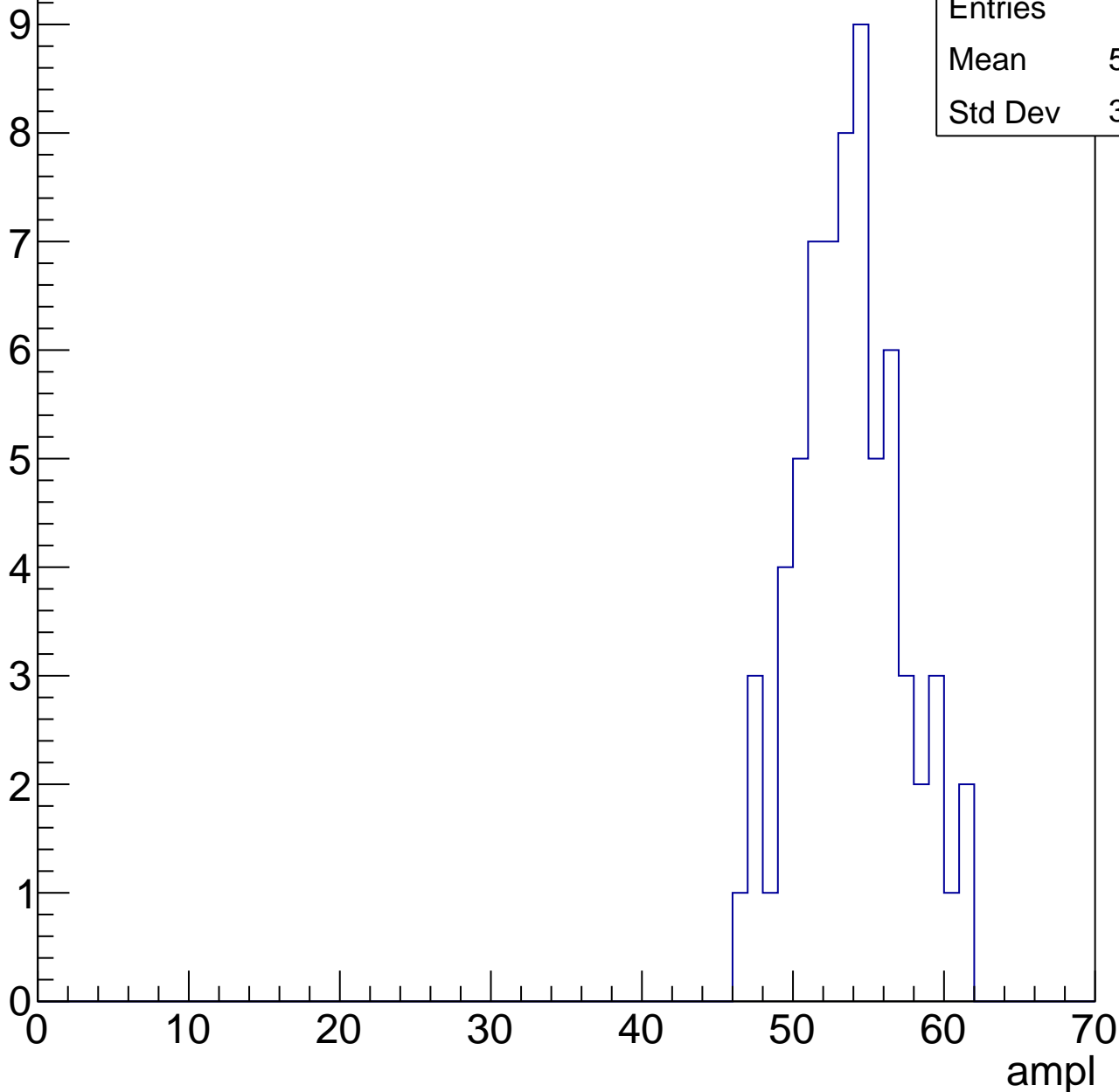


# B1L103S, U4-ch52, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 67    |
| Mean    | 53.27 |
| Std Dev | 3.428 |

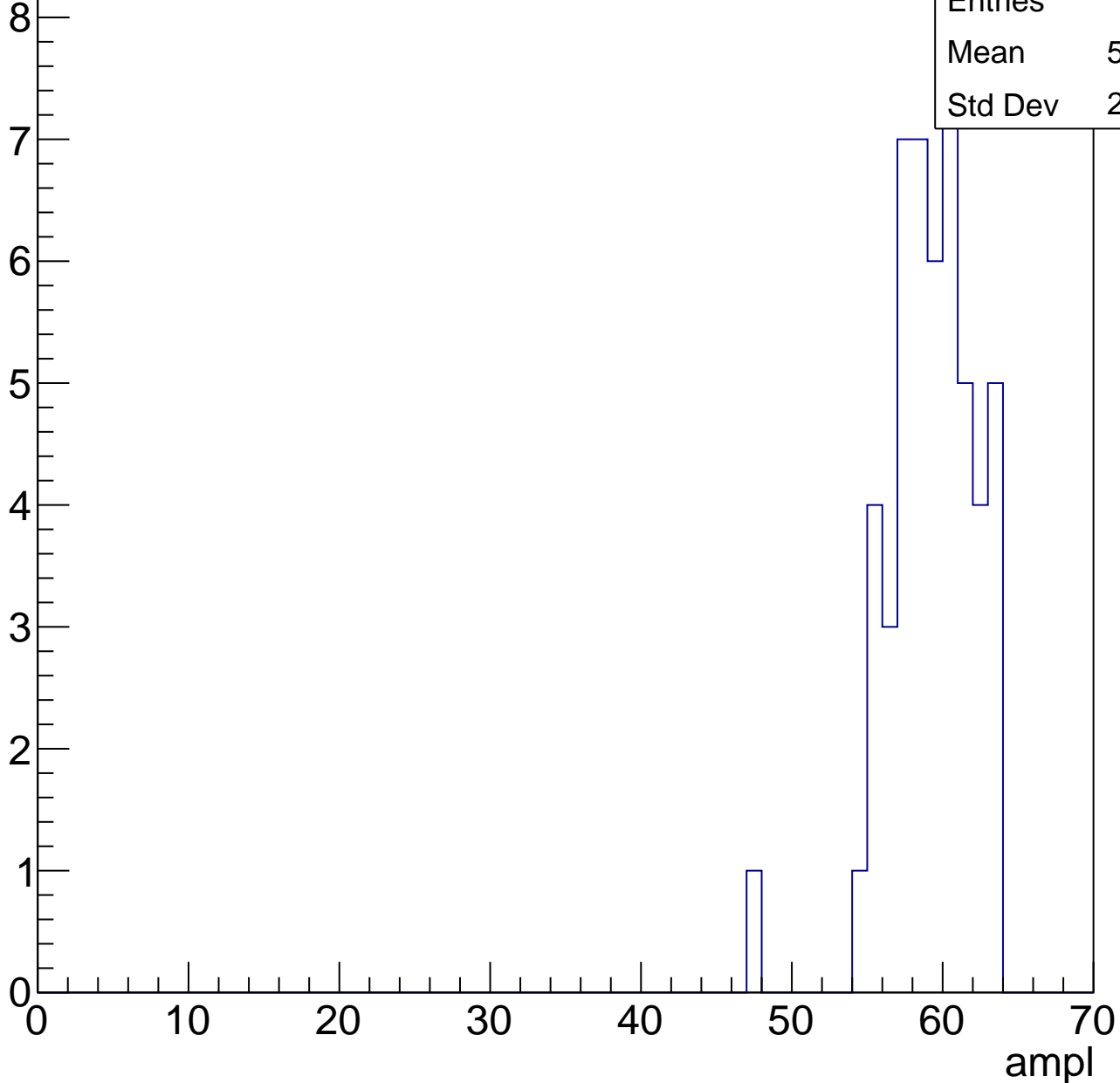


# B1L103S, U4-ch52, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 51    |
| Mean    | 58.75 |
| Std Dev | 2.923 |

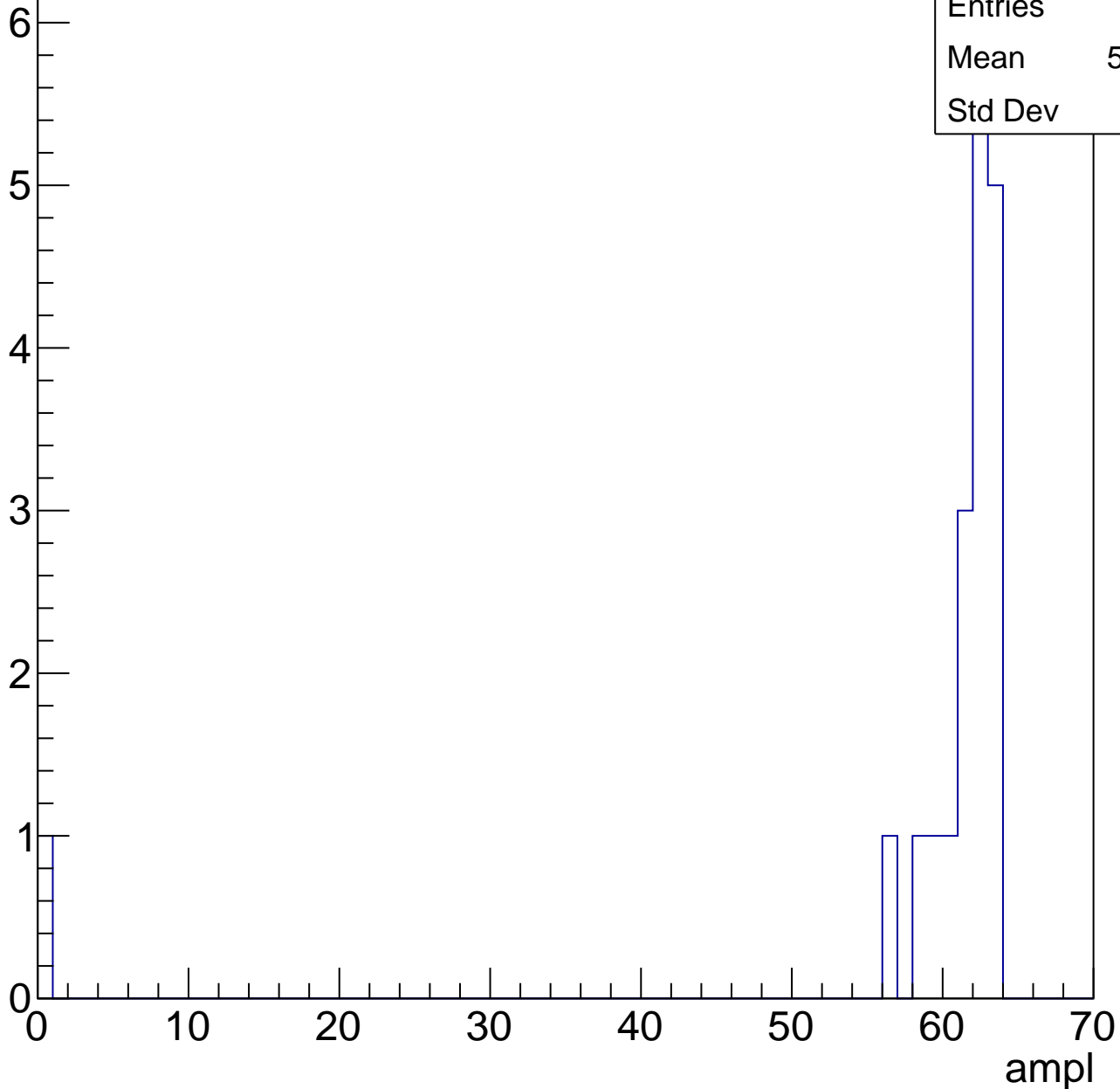


# B1L103S, U4-ch52, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 19    |
| Mean    | 58.05 |
| Std Dev | 13.8  |





# B1L103S, U4-ch52, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

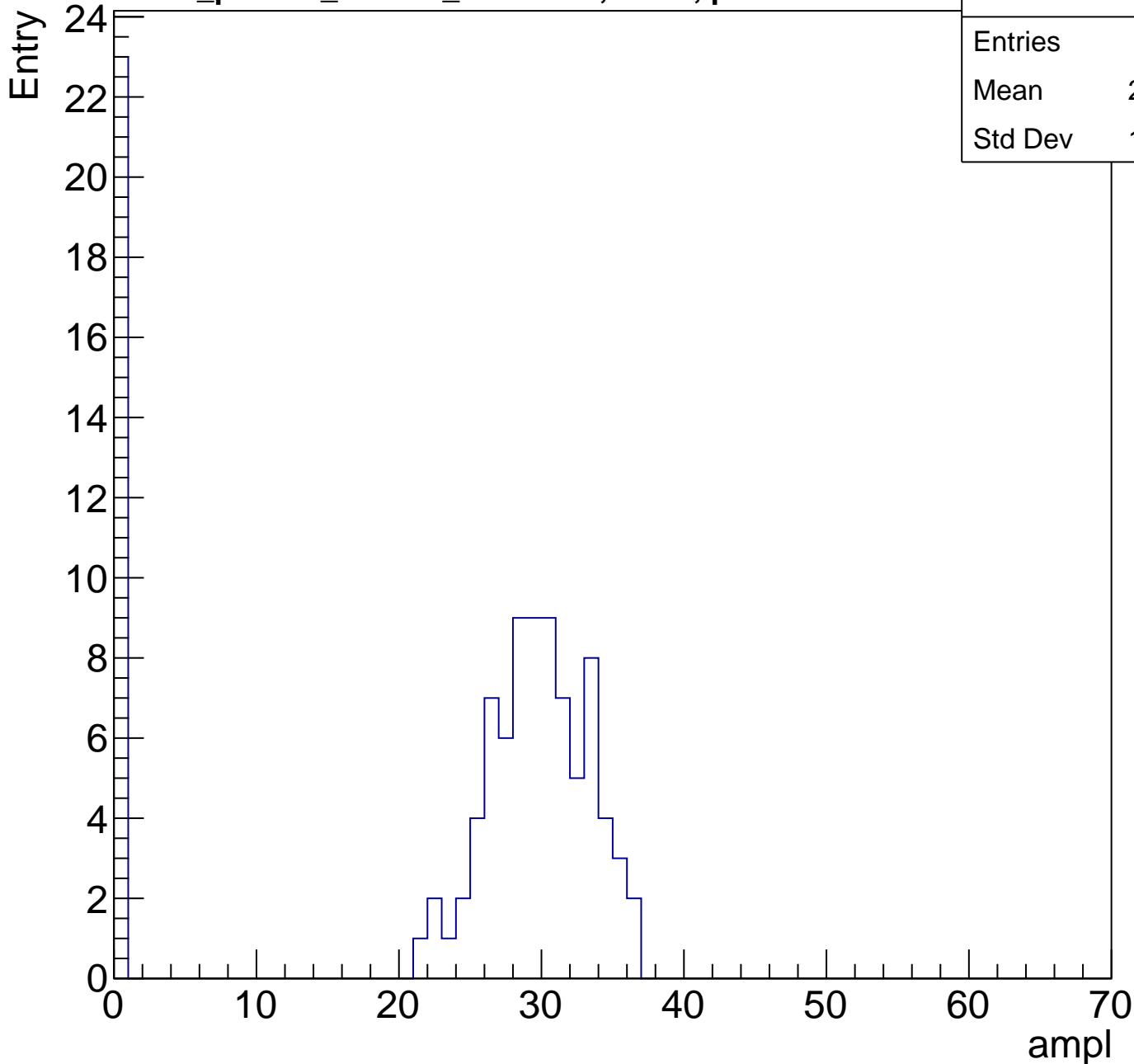


|         |    |
|---------|----|
| Entries | 18 |
| Mean    | 0  |
| Std Dev | 0  |

# B1L103S, U4-ch53, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 102   |
| Mean    | 22.72 |
| Std Dev | 12.62 |

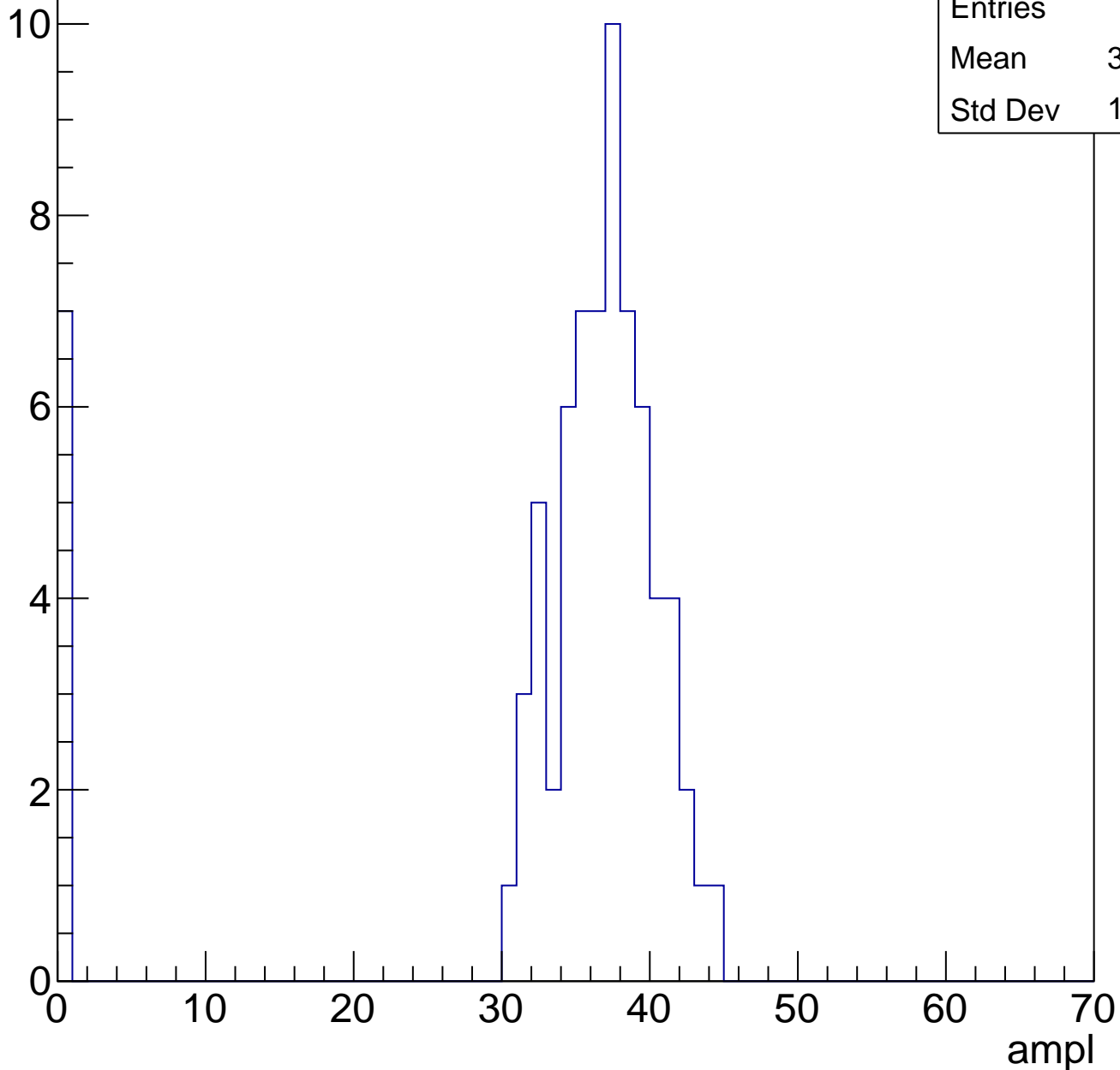


# B1L103S, U4-ch53, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 73    |
| Mean    | 33.08 |
| Std Dev | 11.18 |

Entry

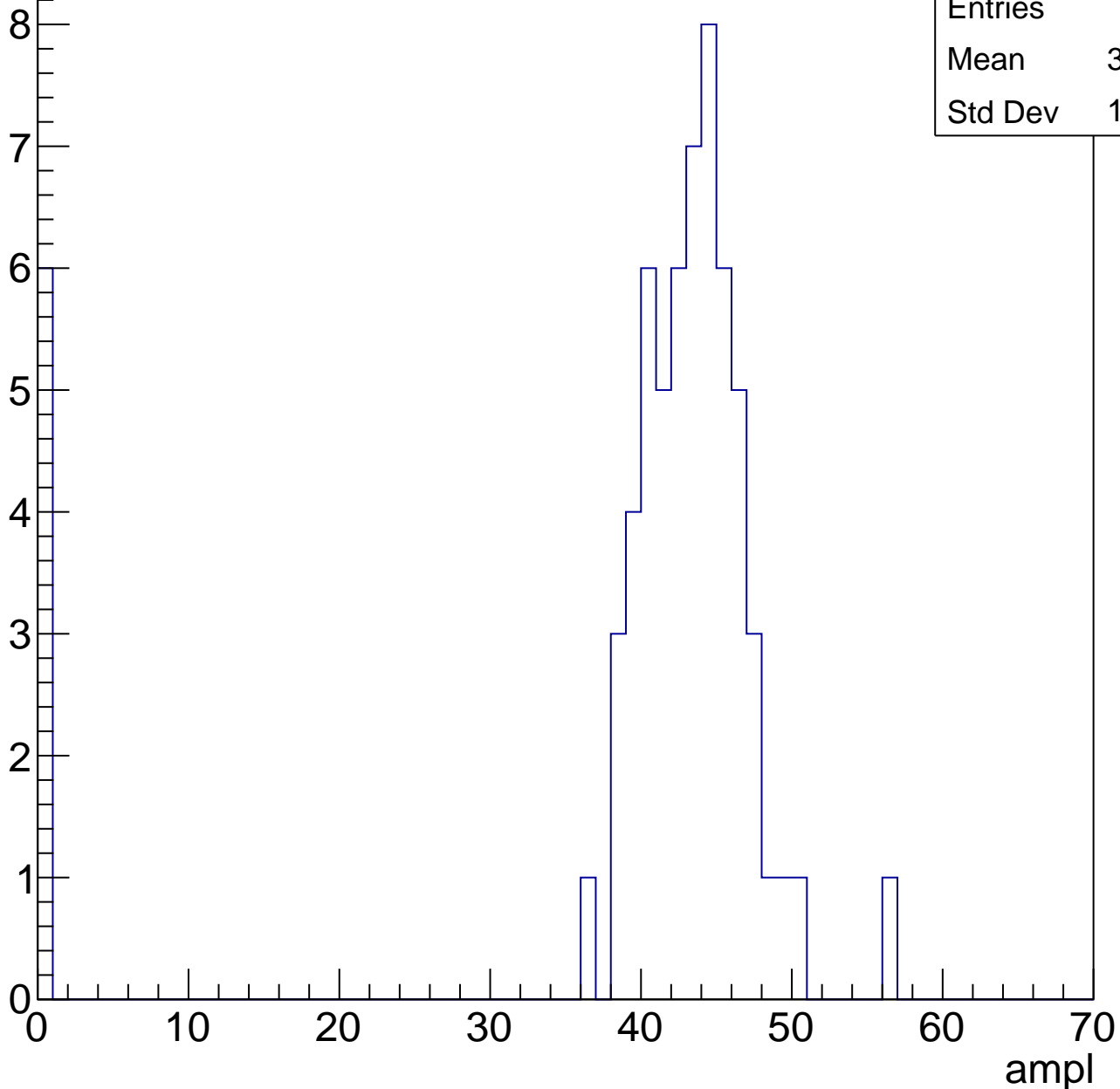


# B1L103S, U4-ch53, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 64    |
| Mean    | 39.06 |
| Std Dev | 12.97 |

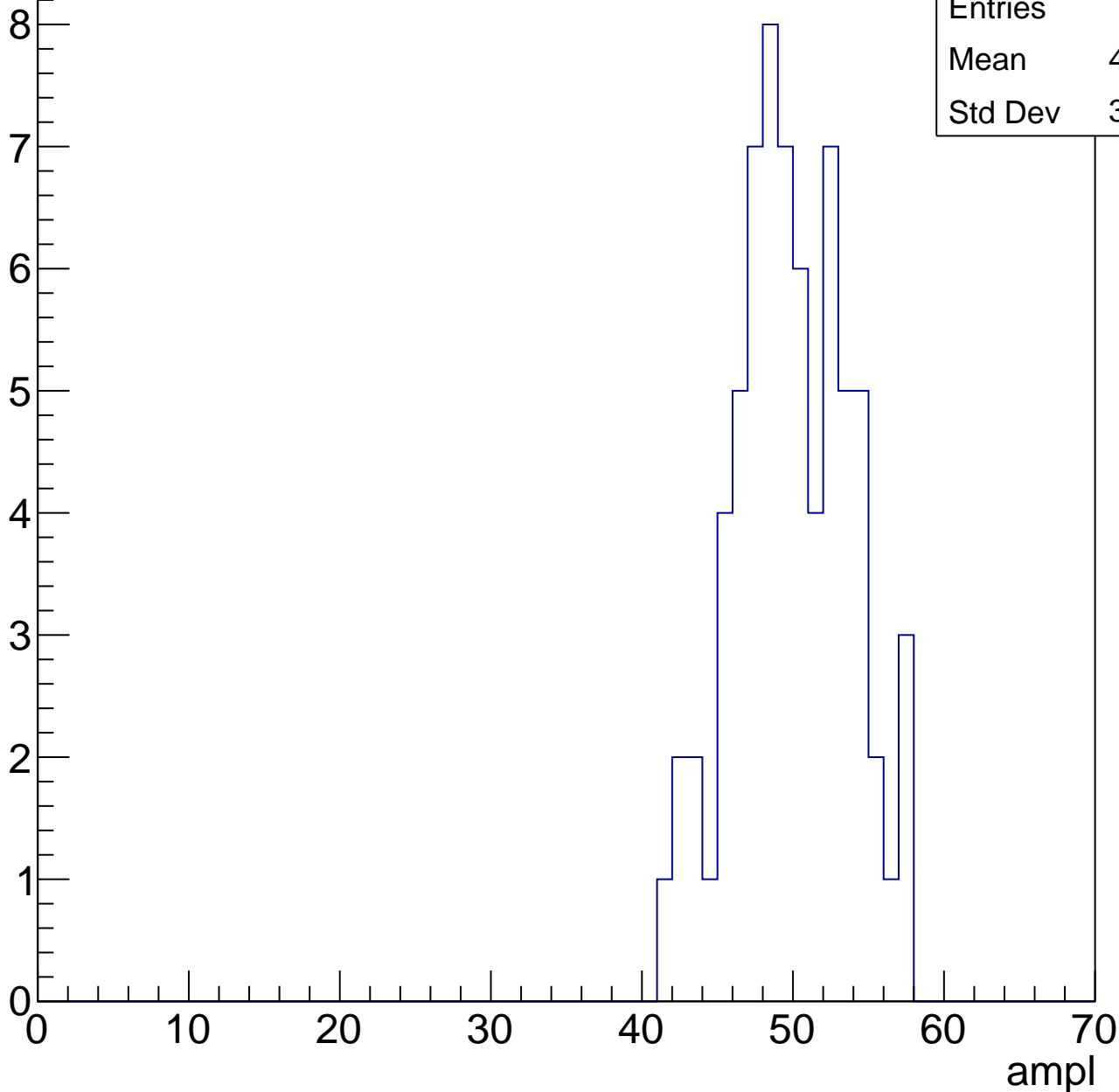


# B1L103S, U4-ch53, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

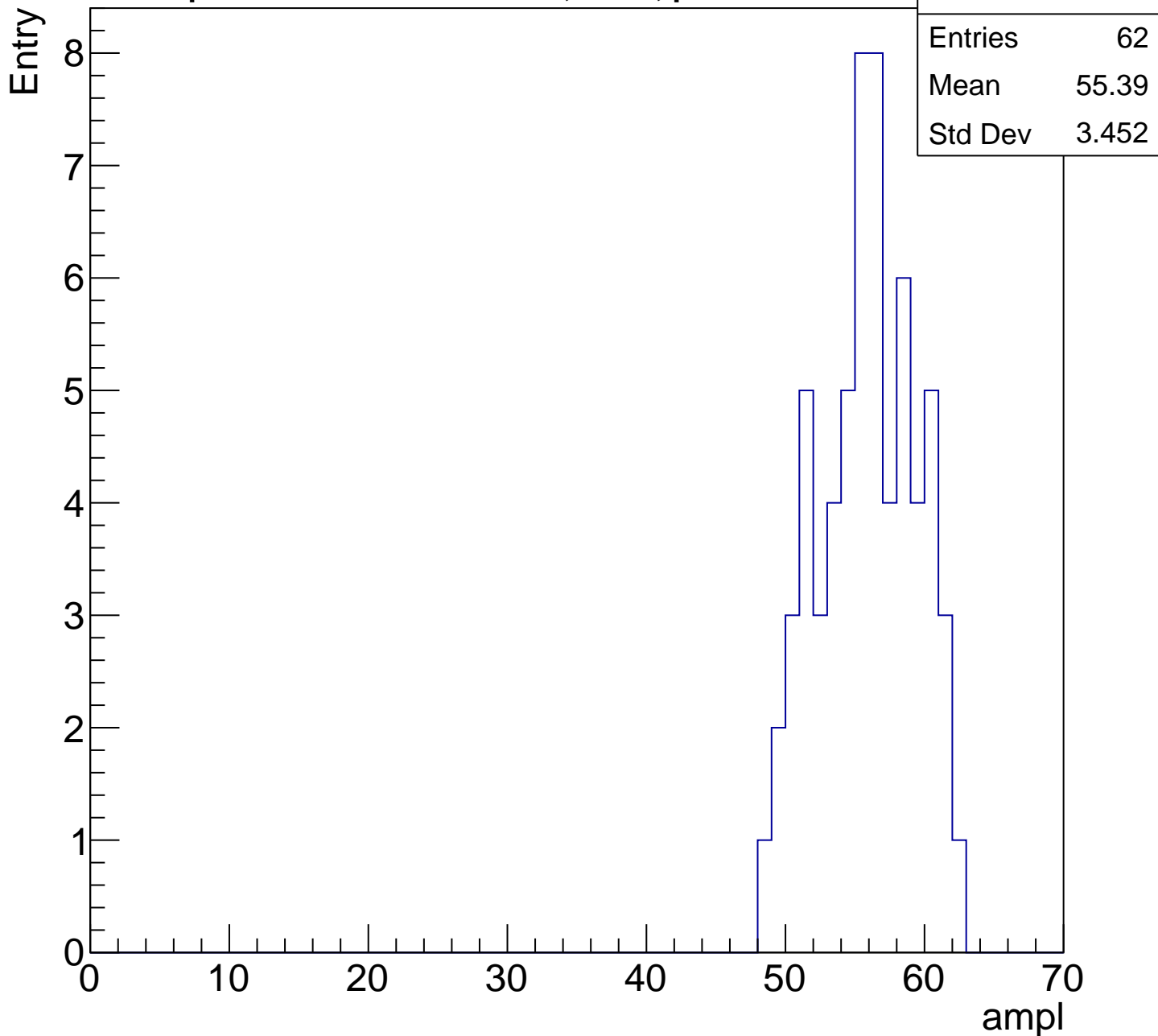
Entry

|         |       |
|---------|-------|
| Entries | 70    |
| Mean    | 49.44 |
| Std Dev | 3.767 |



# B1L103S, U4-ch53, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

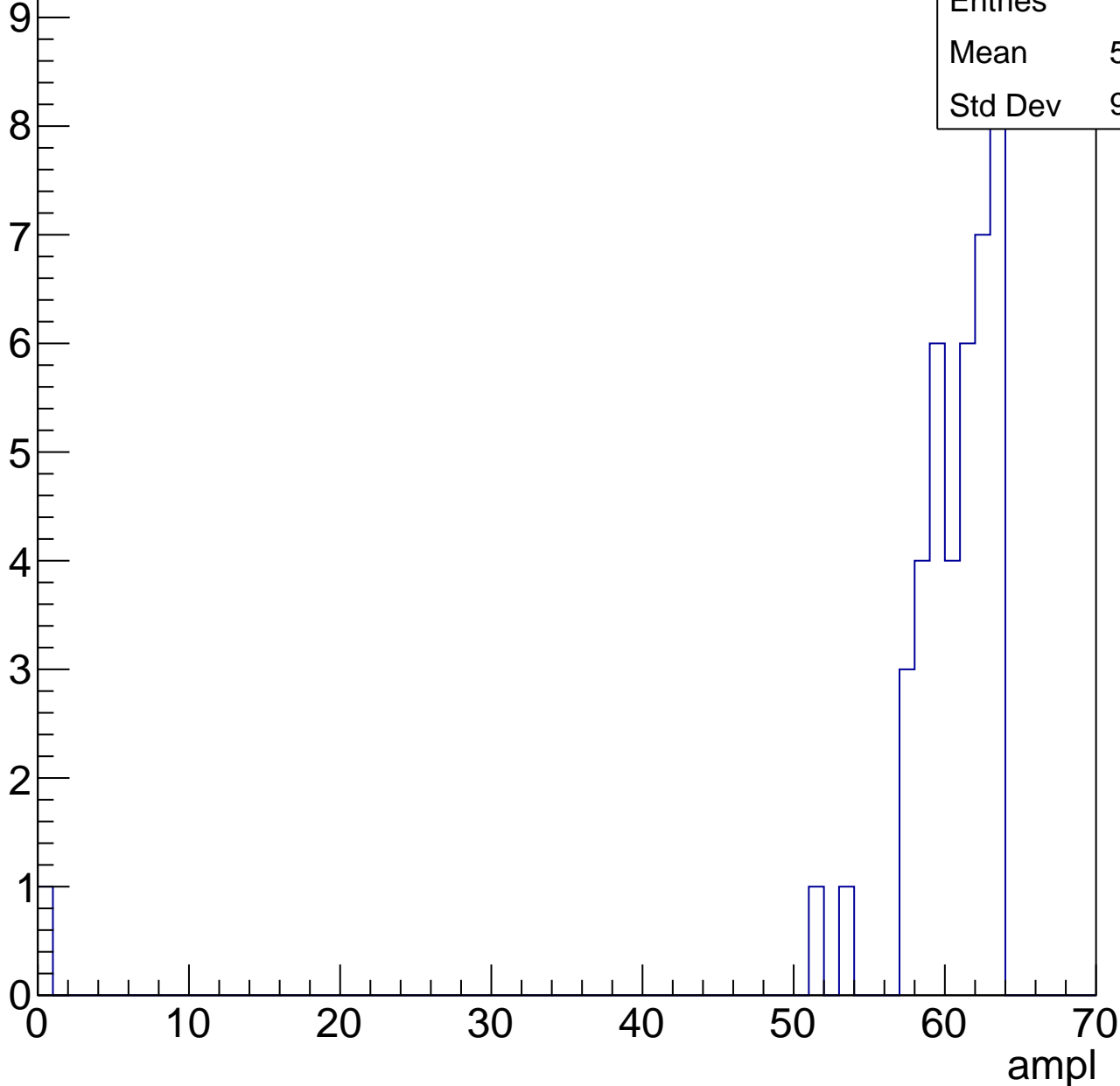


# B1L103S, U4-ch53, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 42    |
| Mean    | 58.76 |
| Std Dev | 9.549 |



# B1L103S, U4-ch53, adc6

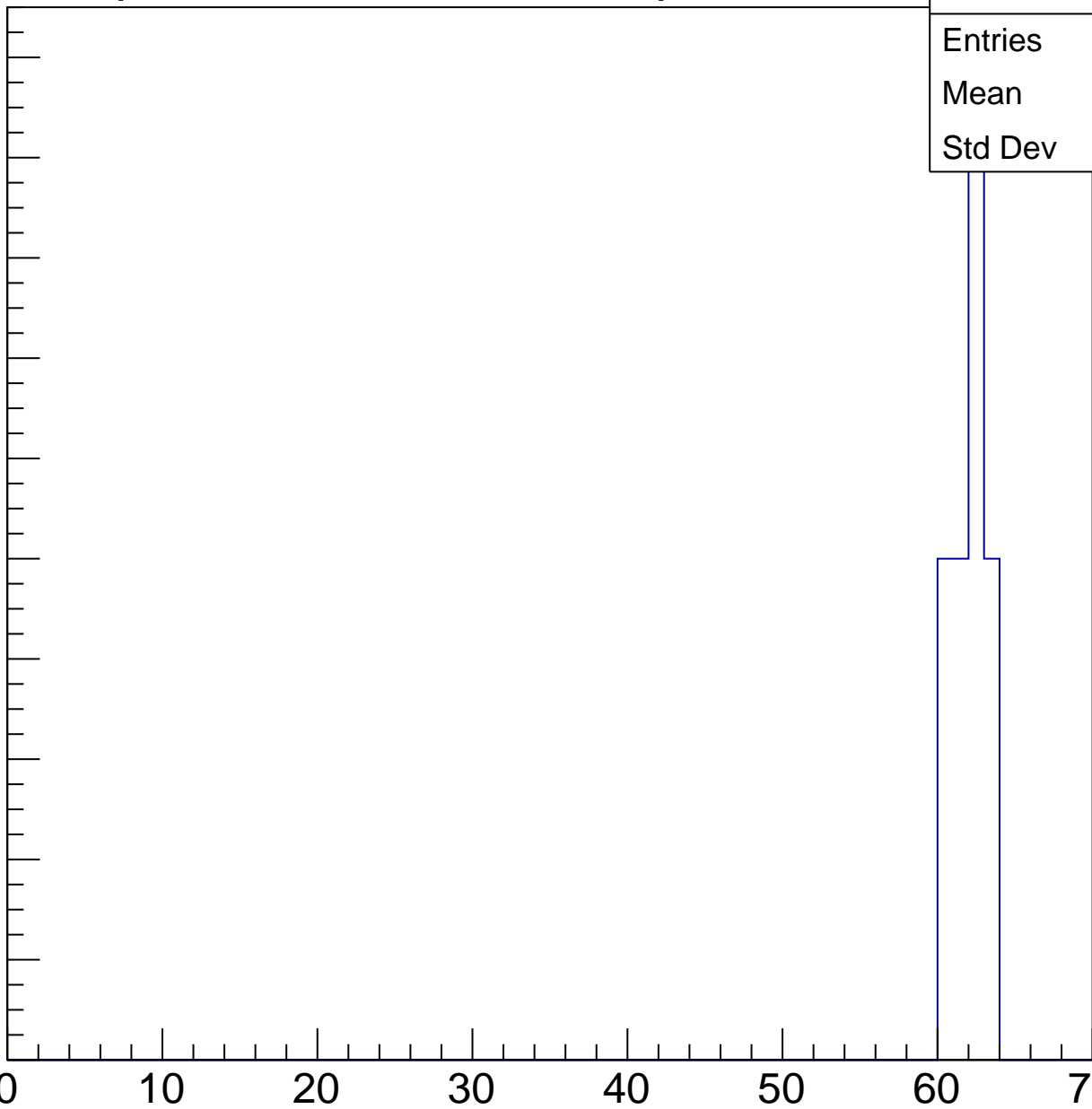
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

|         |      |
|---------|------|
| Entries | 5    |
| Mean    | 61.6 |
| Std Dev | 1.02 |

ampl





# B1L103S, U4-ch53, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U4-ch54, adc0

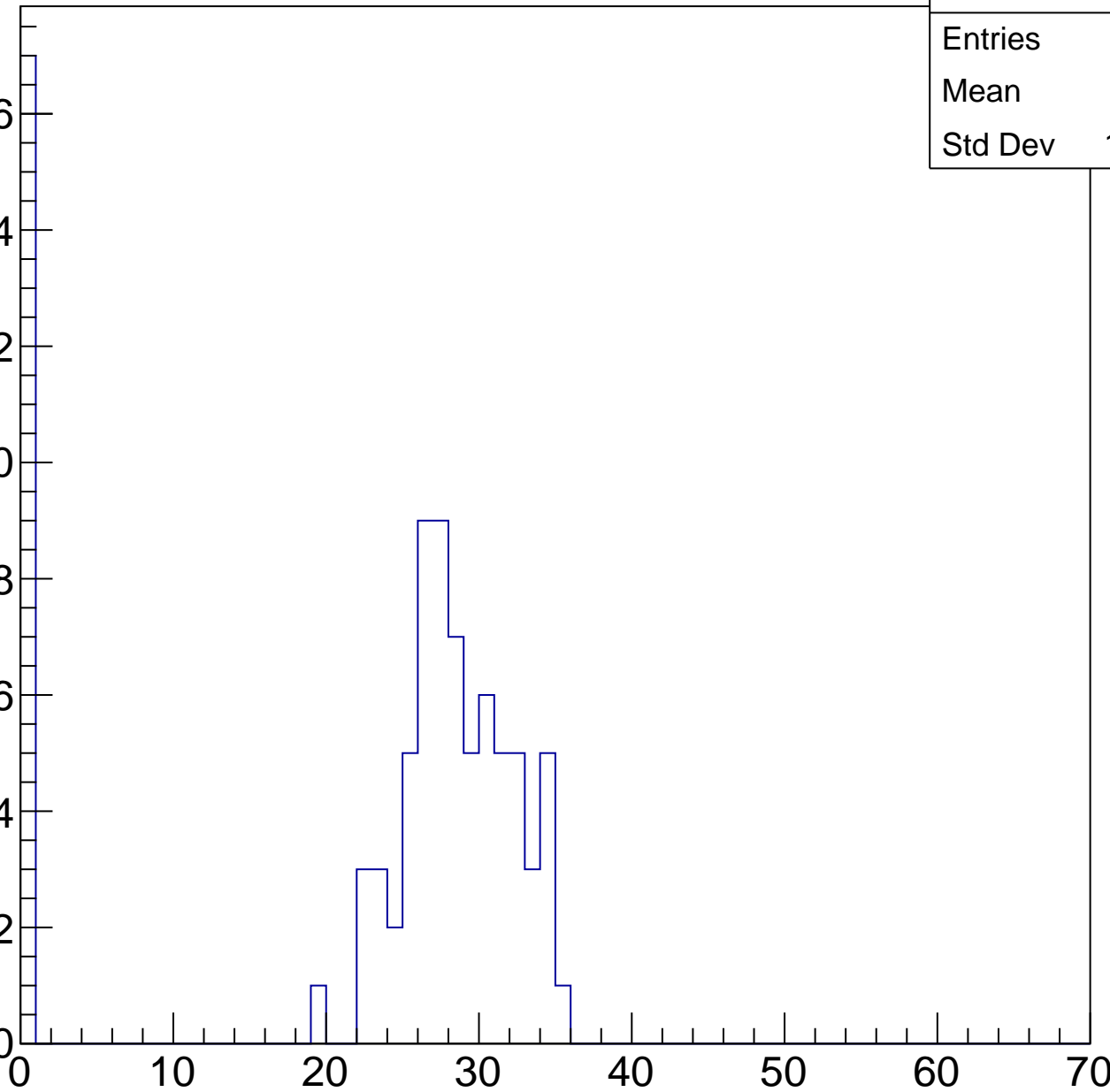
calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 86    |
| Mean    | 22.6  |
| Std Dev | 11.65 |

Entry

16  
14  
12  
10  
8  
6  
4  
2  
0

ampl

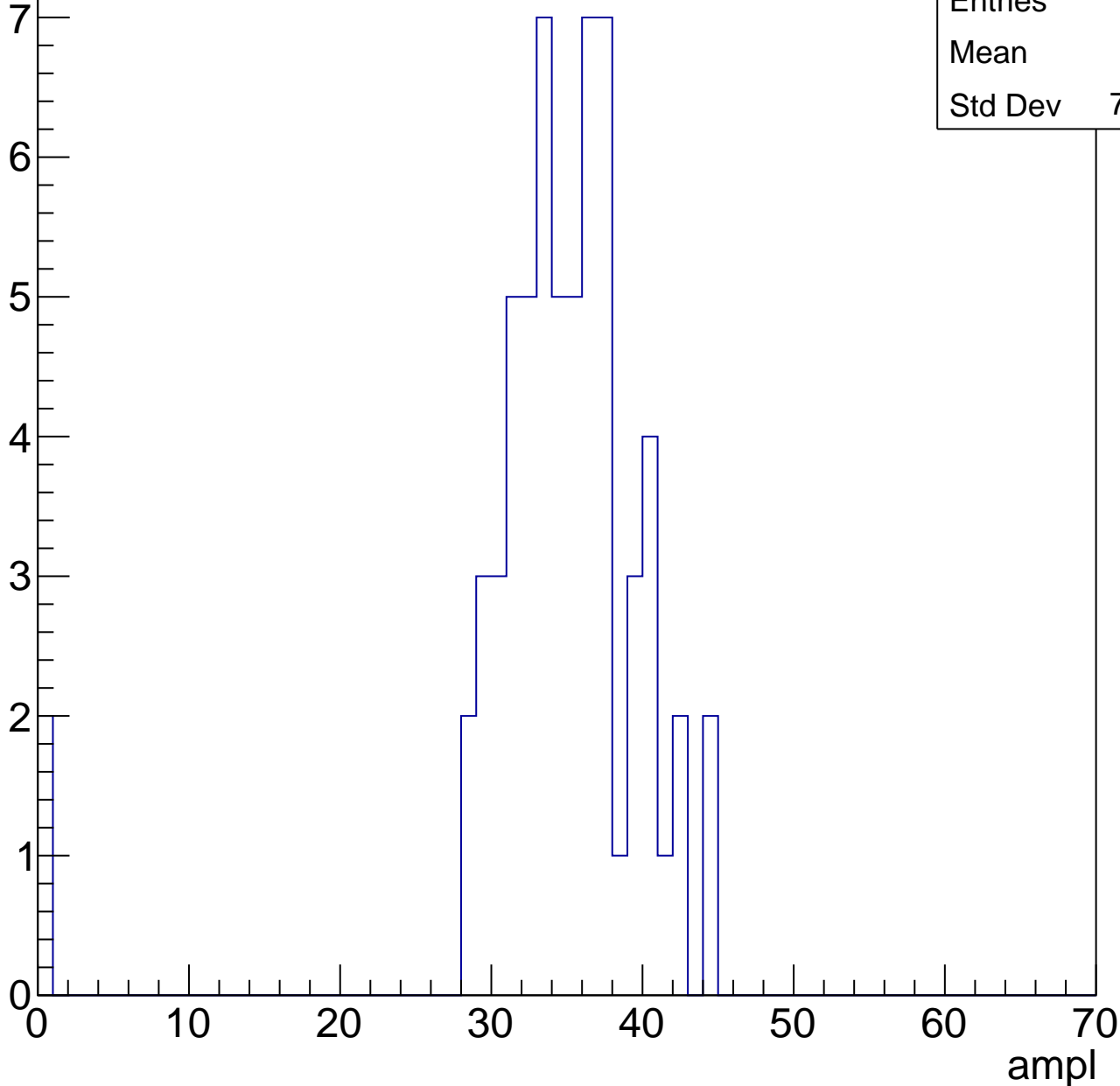


# B1L103S, U4-ch54, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 64    |
| Mean    | 33.8  |
| Std Dev | 7.164 |

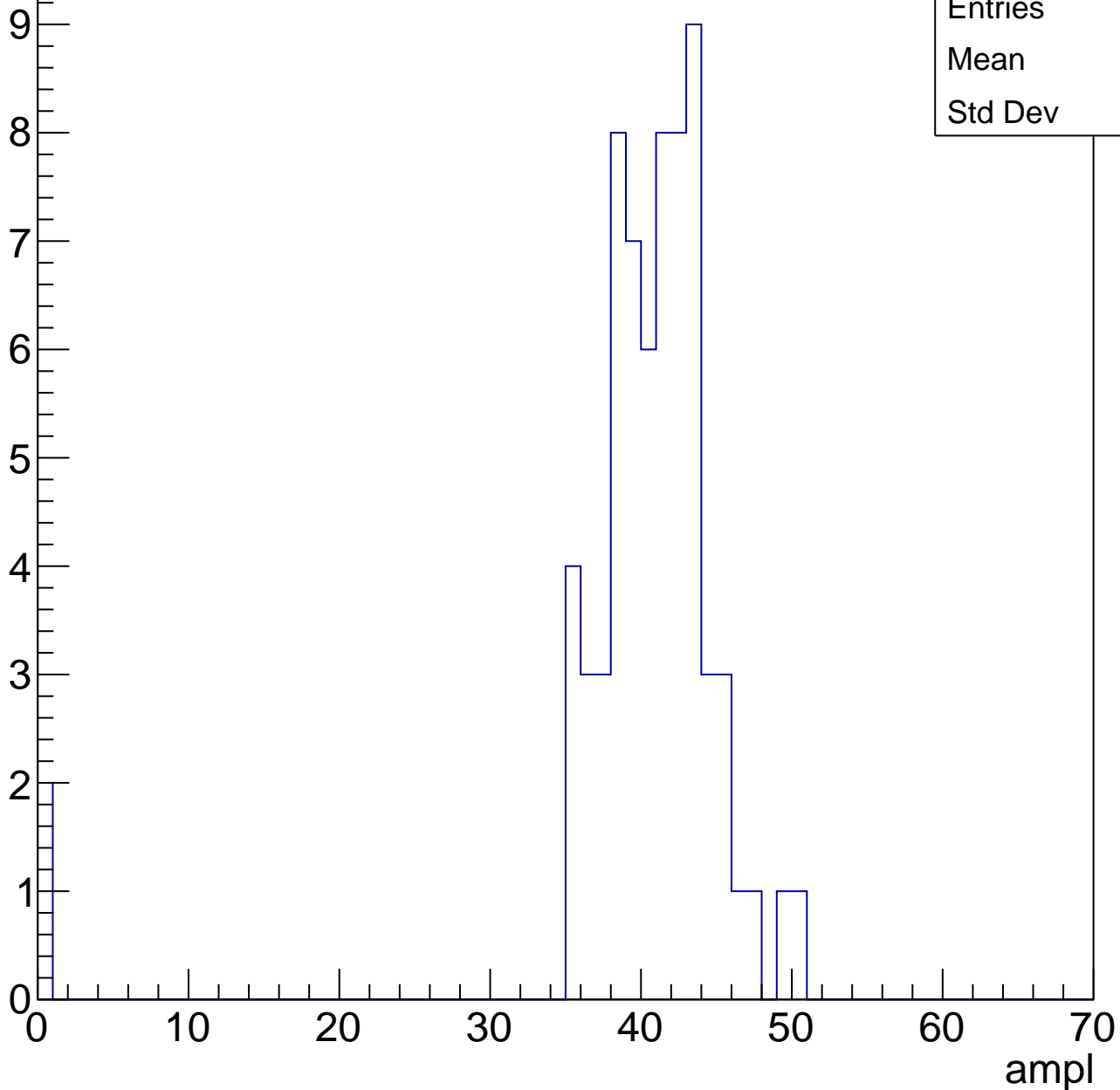


# B1L103S, U4-ch54, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

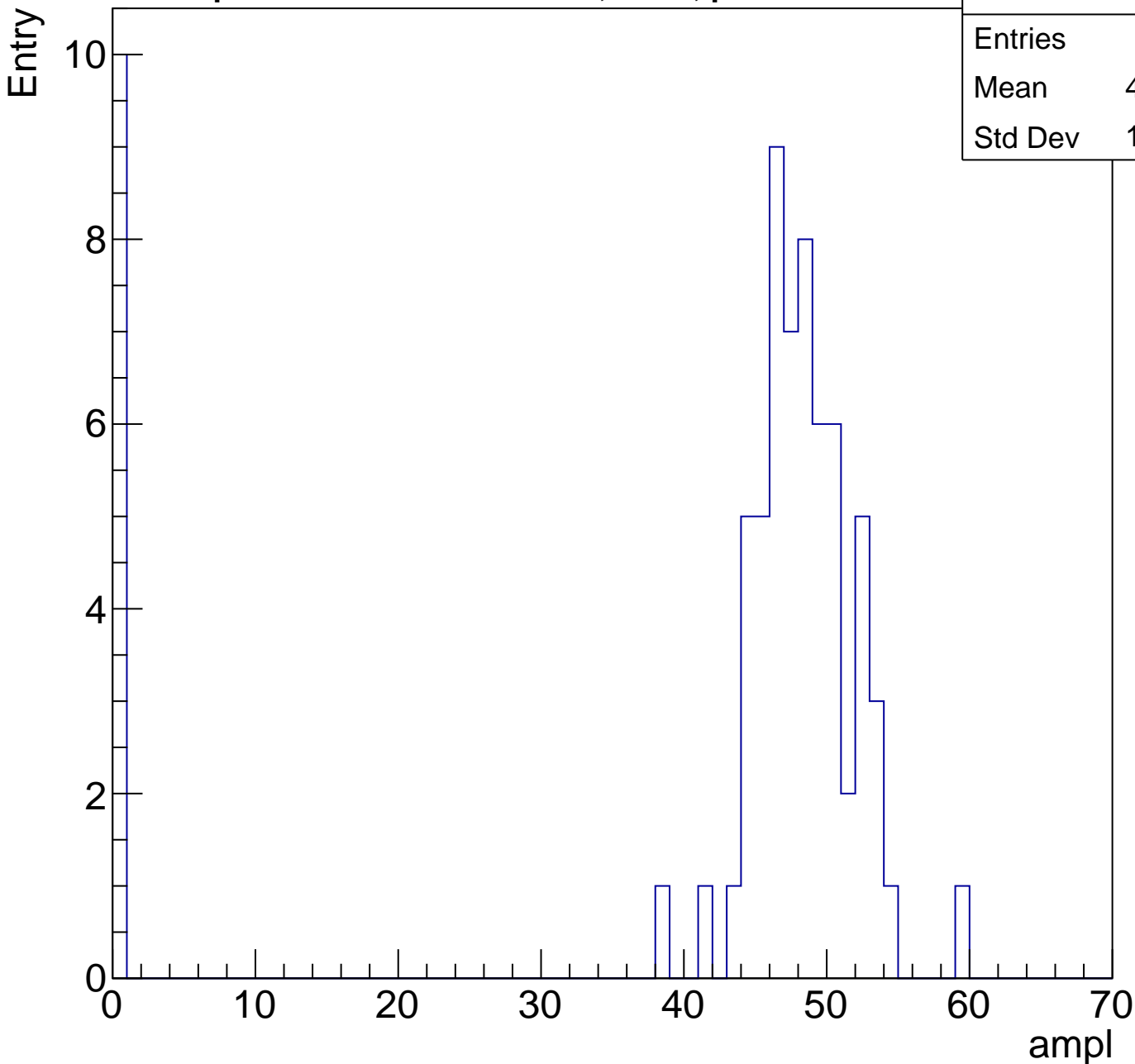
|         |      |
|---------|------|
| Entries | 68   |
| Mean    | 39.5 |
| Std Dev | 7.58 |



# B1L103S, U4-ch54, adc3

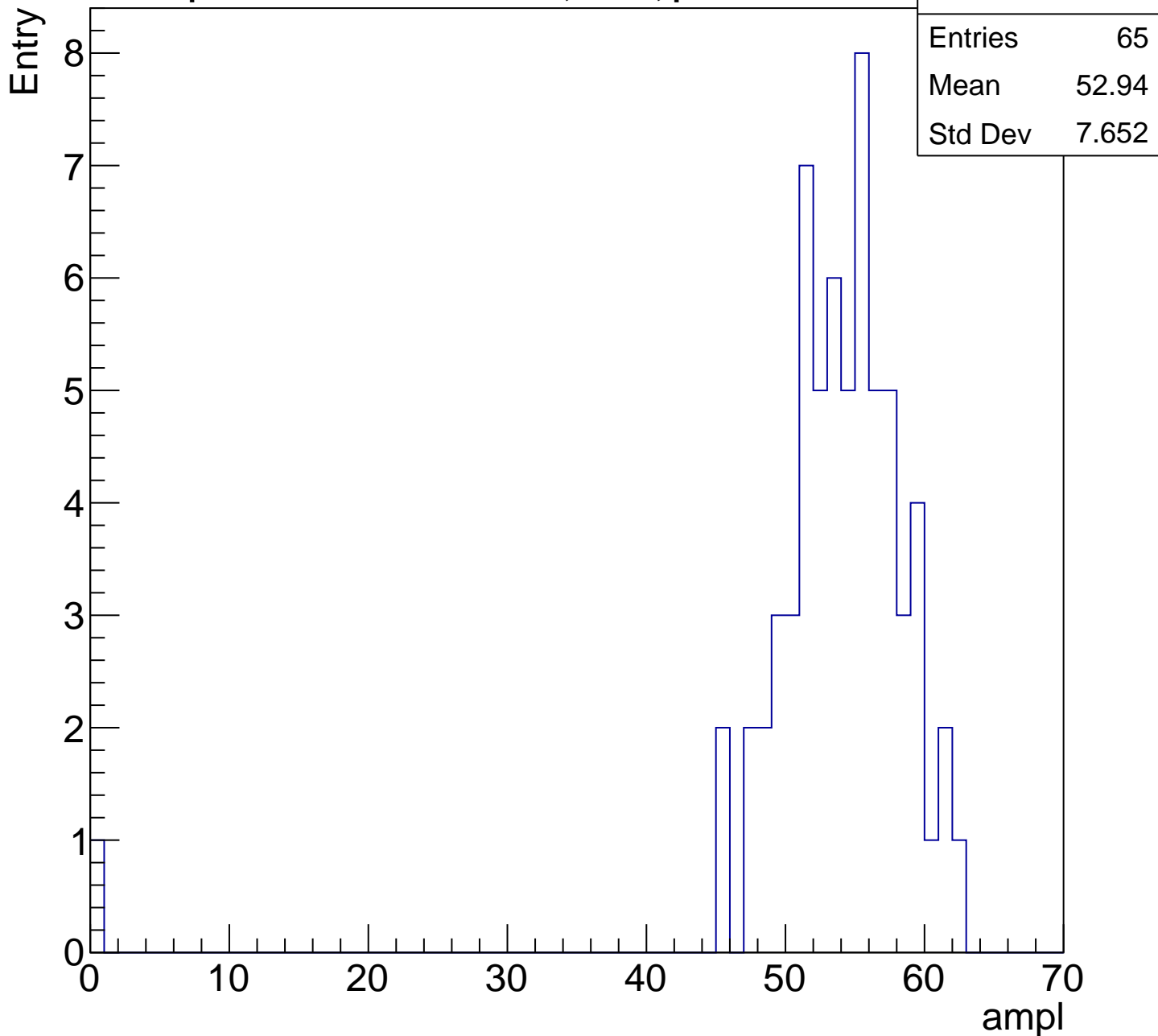
calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 71    |
| Mean    | 41.15 |
| Std Dev | 16.96 |



# B1L103S, U4-ch54, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

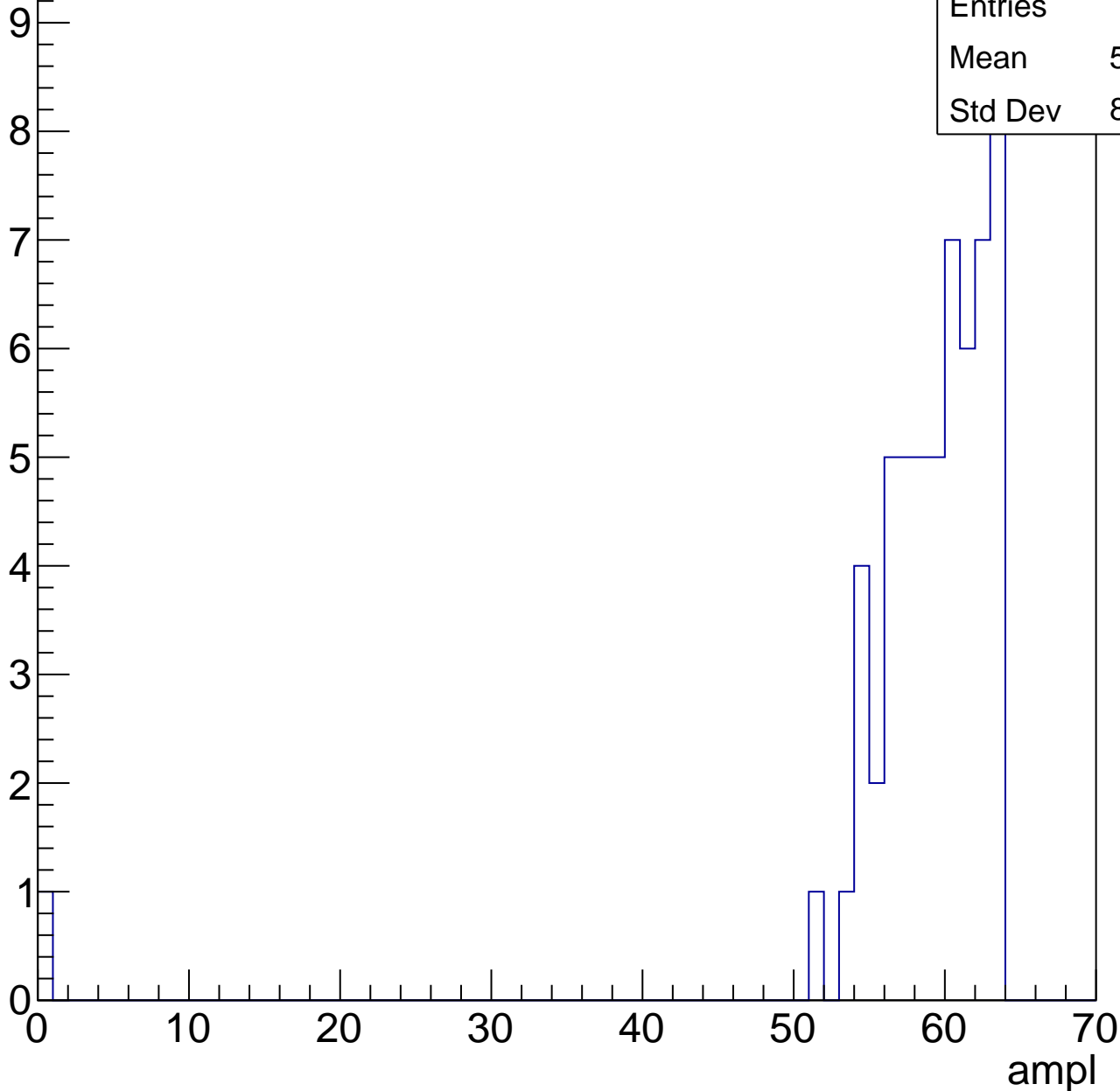


# B1L103S, U4-ch54, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 58    |
| Mean    | 58.05 |
| Std Dev | 8.272 |



# B1L103S, U4-ch54, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

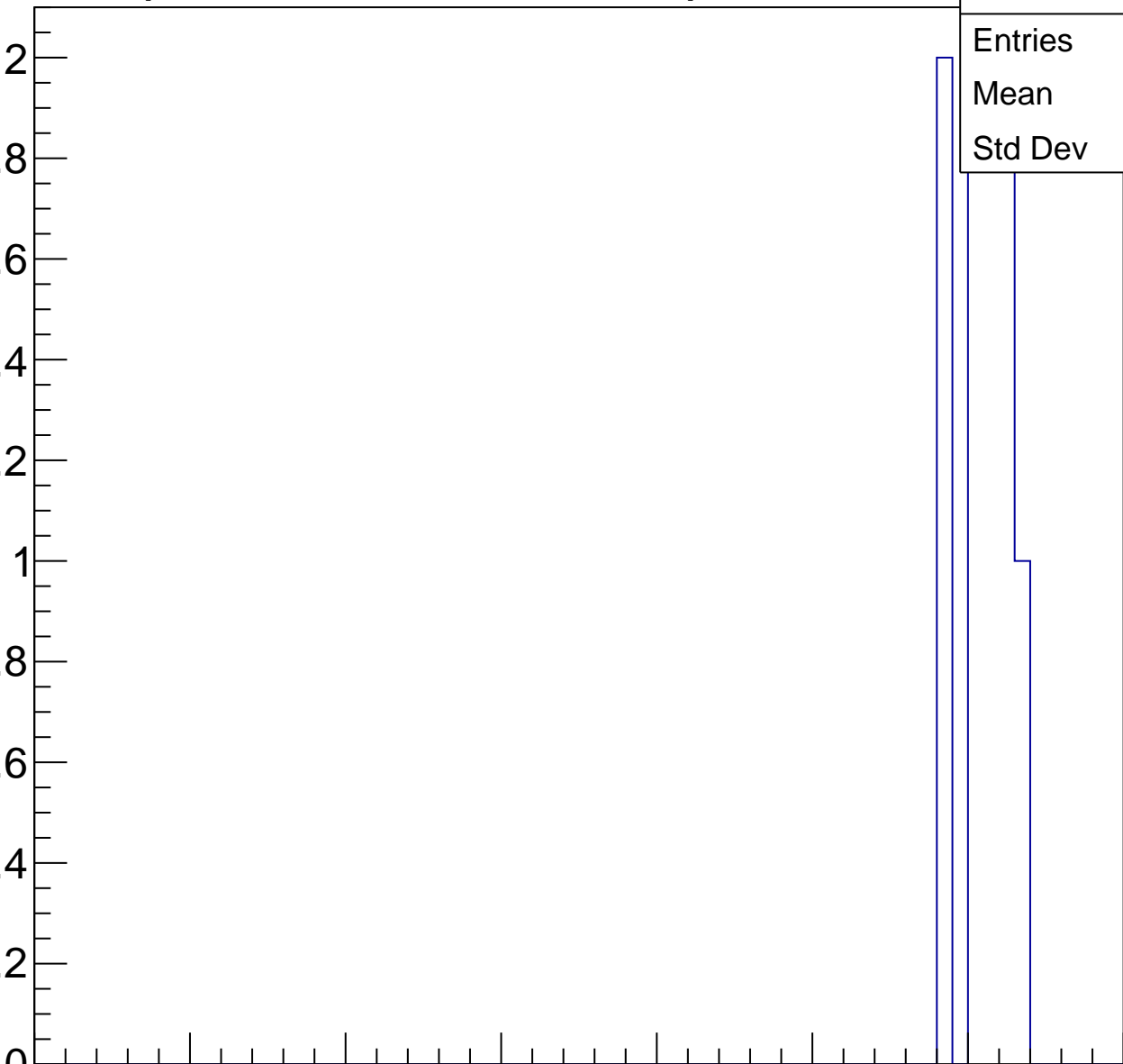
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

|         |       |
|---------|-------|
| Entries | 9     |
| Mean    | 60.56 |
| Std Dev | 1.641 |

0 10 20 30 40 50 60 70

ampl





# B1L103S, U4-ch54, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

|         |    |
|---------|----|
| Entries | 19 |
| Mean    | 0  |
| Std Dev | 0  |

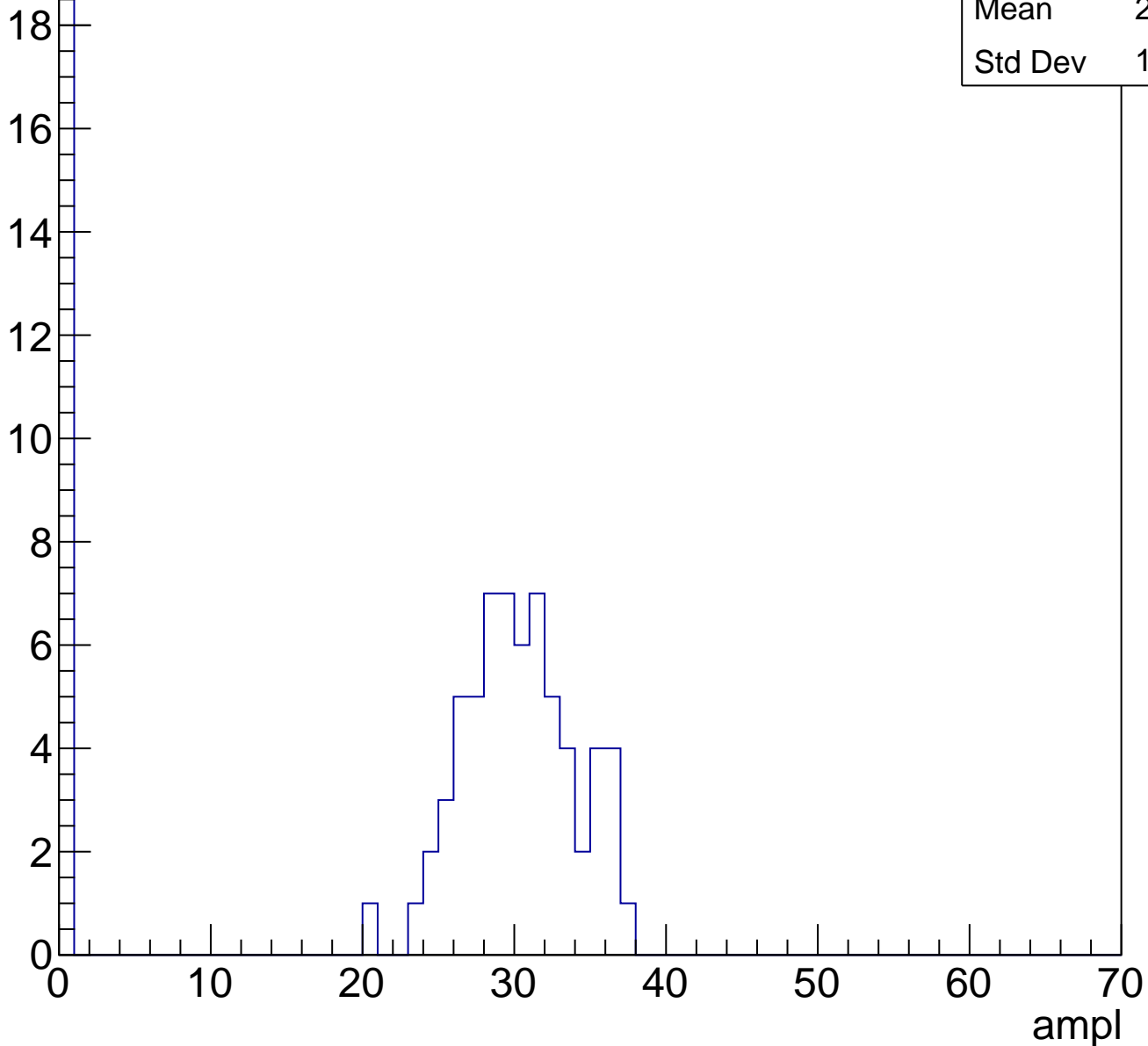
ampl

# B1L103S, U4-ch55, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 83    |
| Mean    | 22.99 |
| Std Dev | 12.92 |

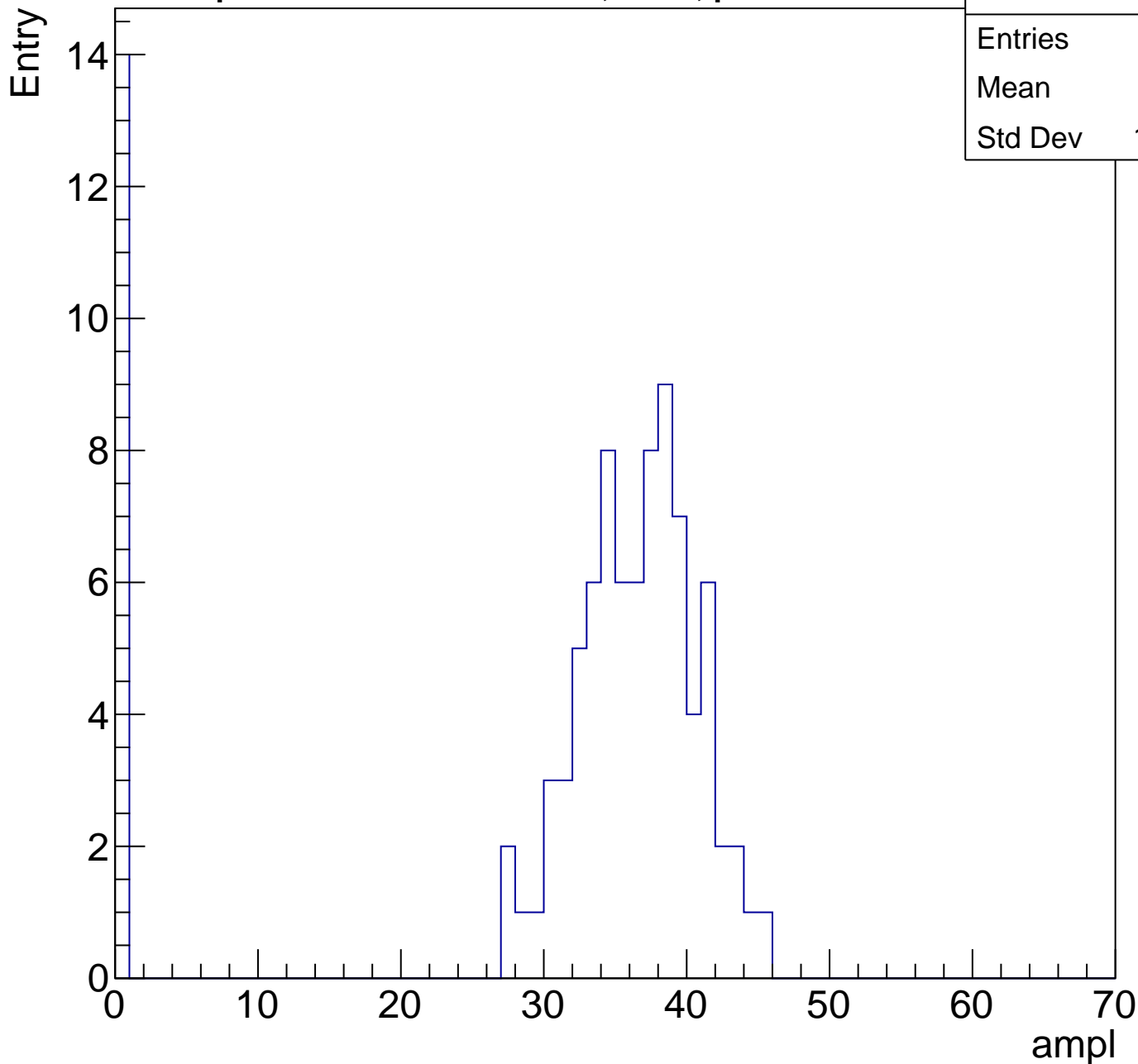
Entry



# B1L103S, U4-ch55, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 95    |
| Mean    | 30.8  |
| Std Dev | 13.31 |

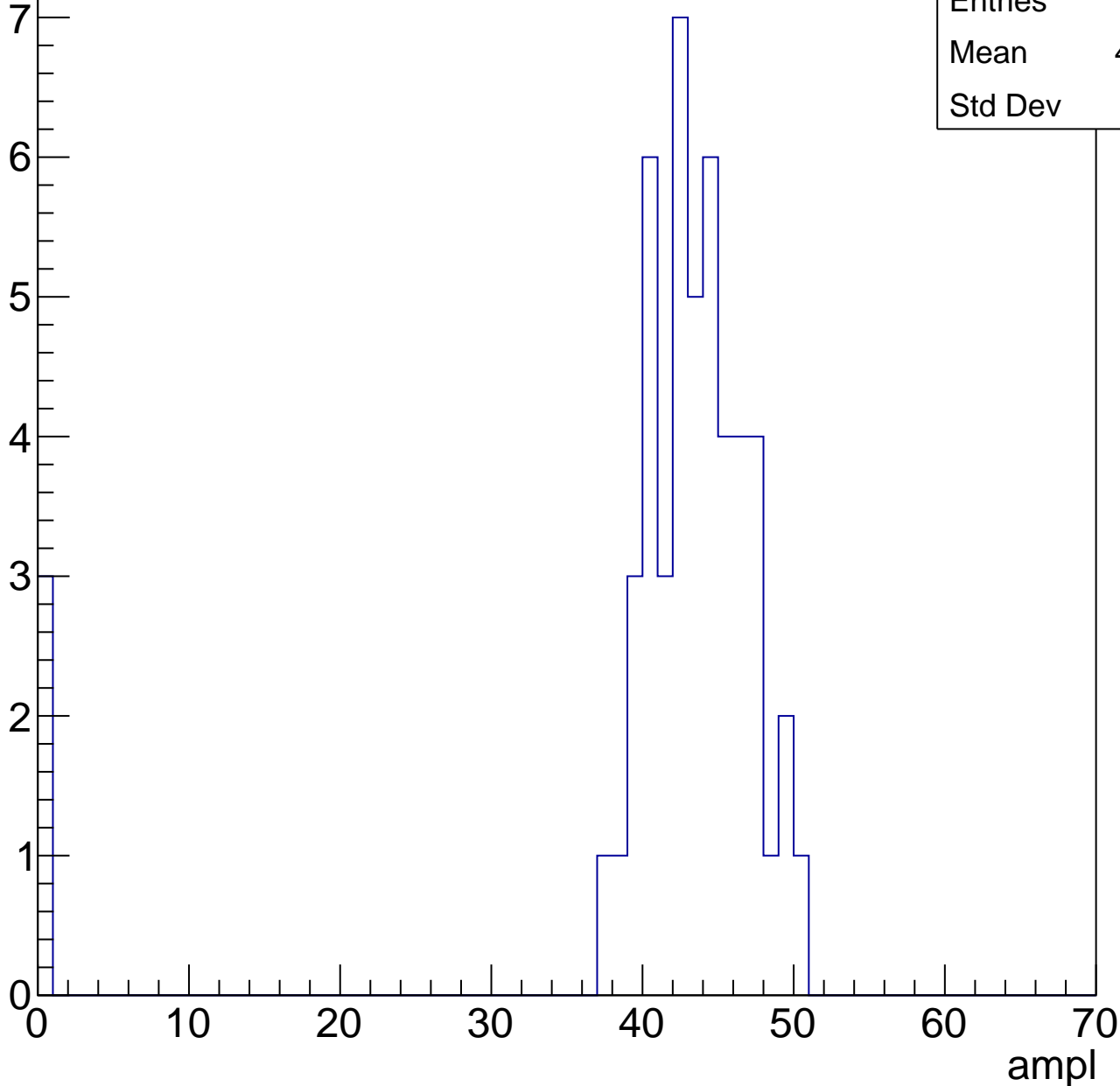


# B1L103S, U4-ch55, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

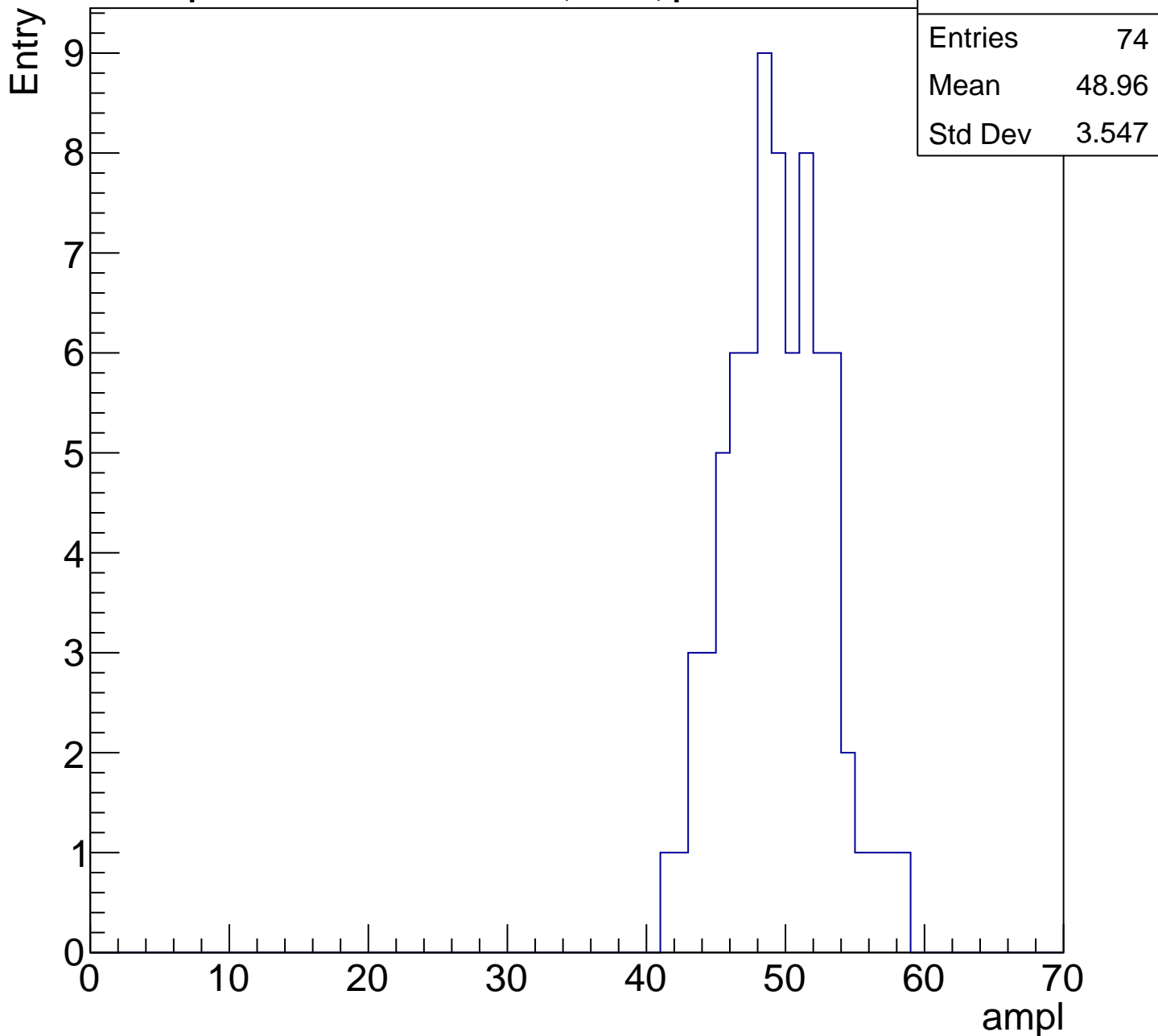
Entry

|         |       |
|---------|-------|
| Entries | 51    |
| Mean    | 40.71 |
| Std Dev | 10.6  |



# B1L103S, U4-ch55, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

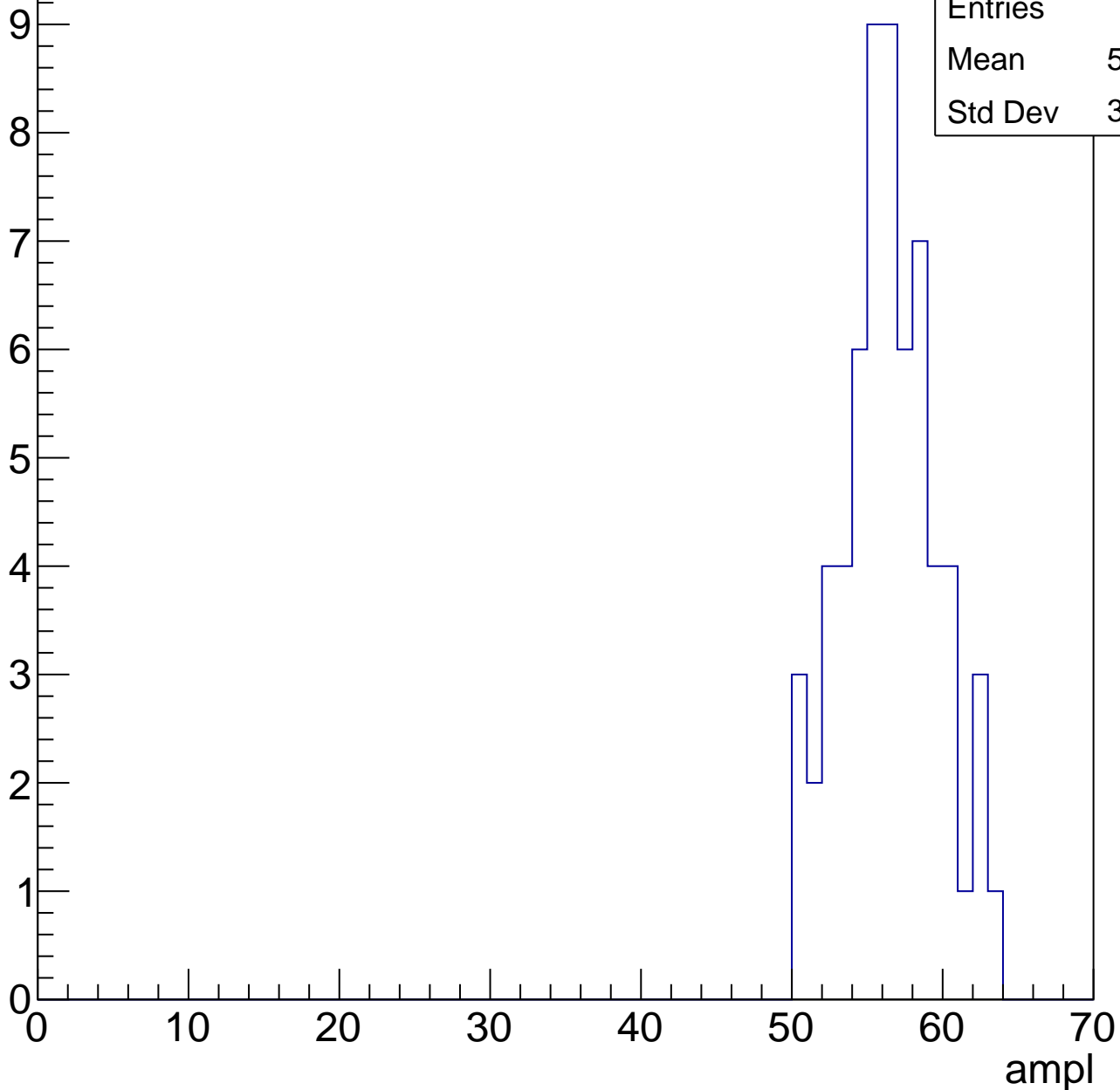


# B1L103S, U4-ch55, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 63    |
| Mean    | 56.02 |
| Std Dev | 3.104 |

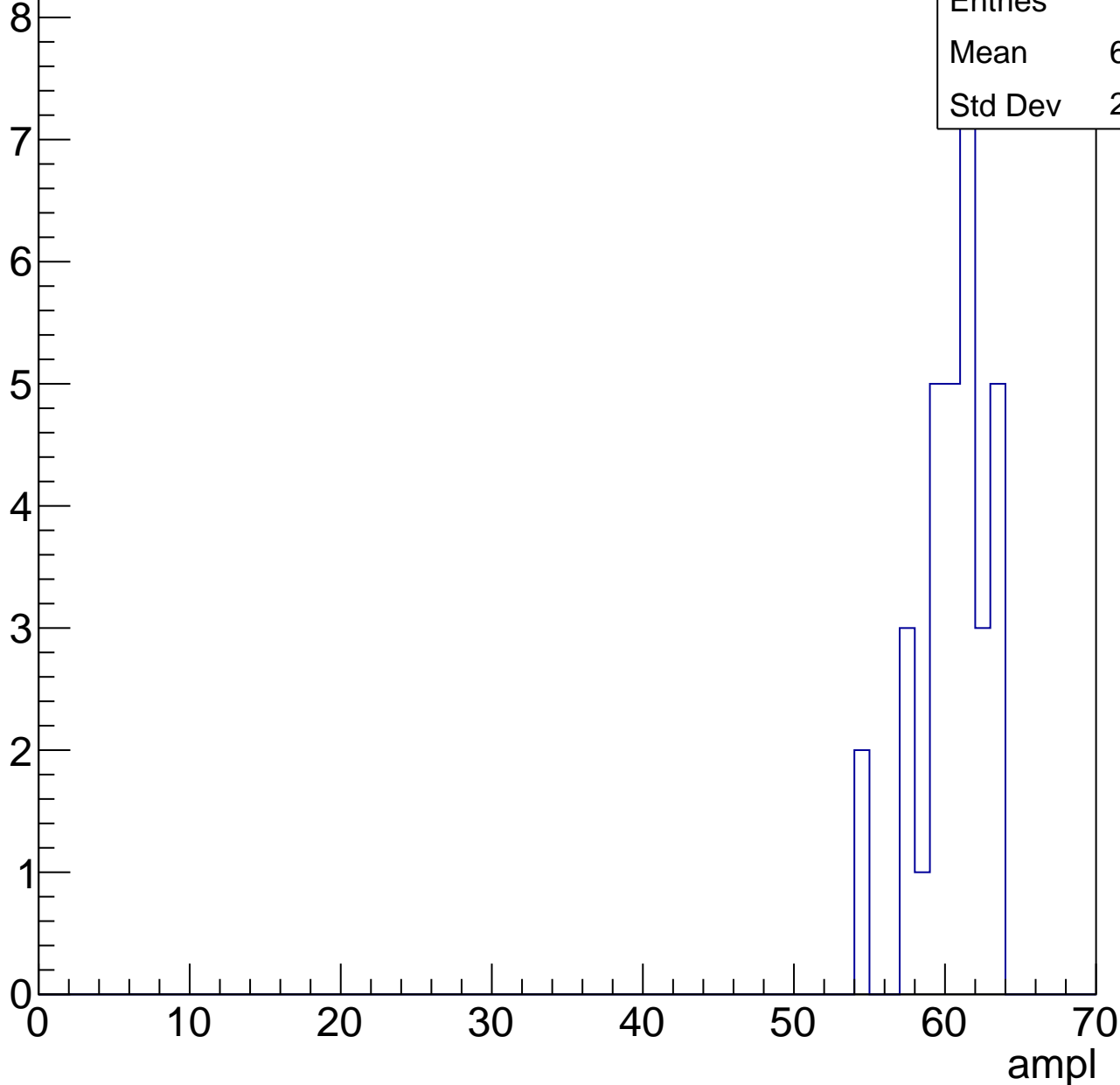


# B1L103S, U4-ch55, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

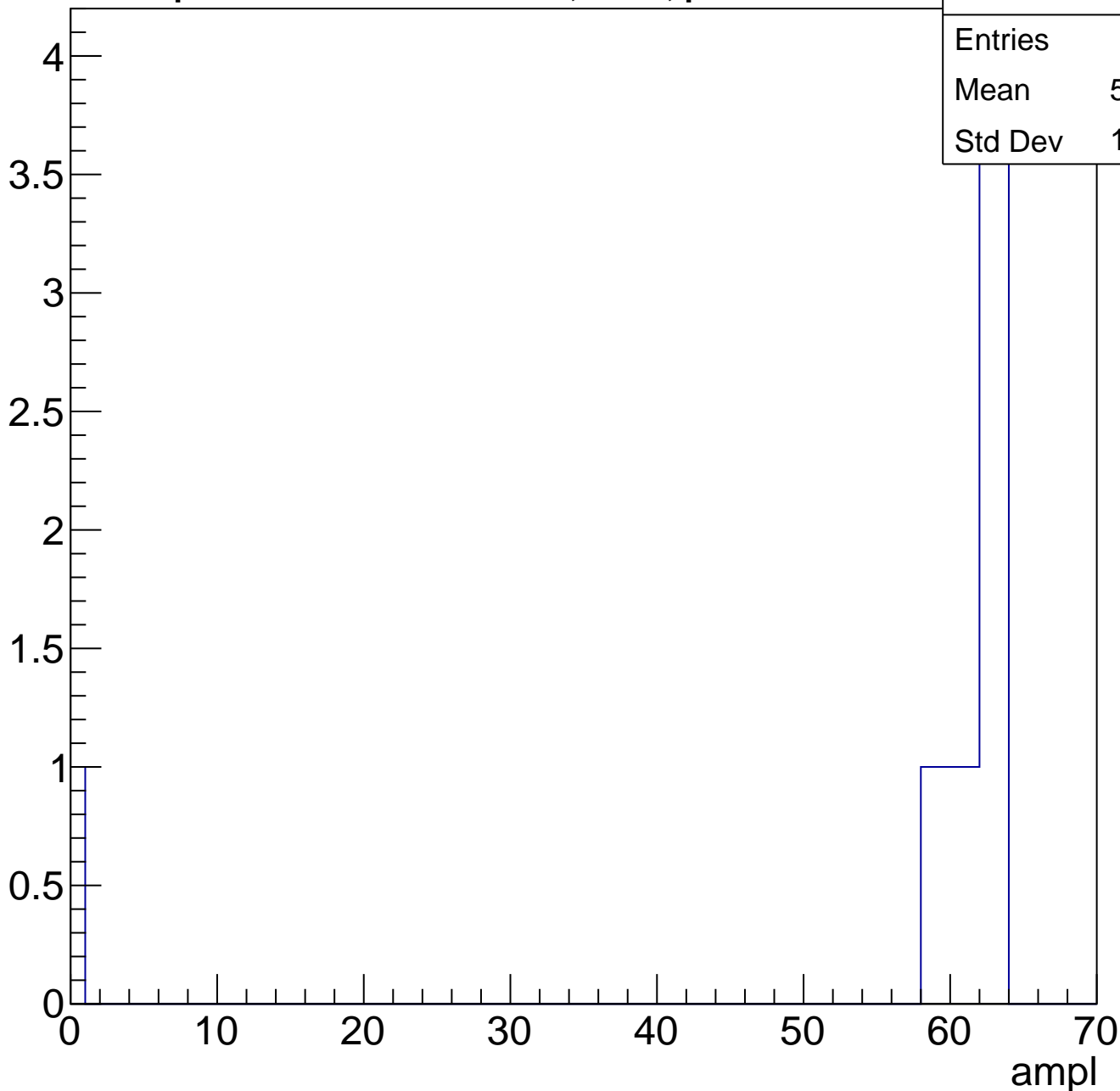
|         |       |
|---------|-------|
| Entries | 32    |
| Mean    | 60.03 |
| Std Dev | 2.325 |



# B1L103S, U4-ch55, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U4-ch55, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

|         |    |
|---------|----|
| Entries | 19 |
| Mean    | 0  |
| Std Dev | 0  |

ampl

# B1L103S, U4-ch56, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 83    |
| Mean    | 25.73 |
| Std Dev | 10.73 |

Entry

10

8

6

4

2

0

0

10

20

30

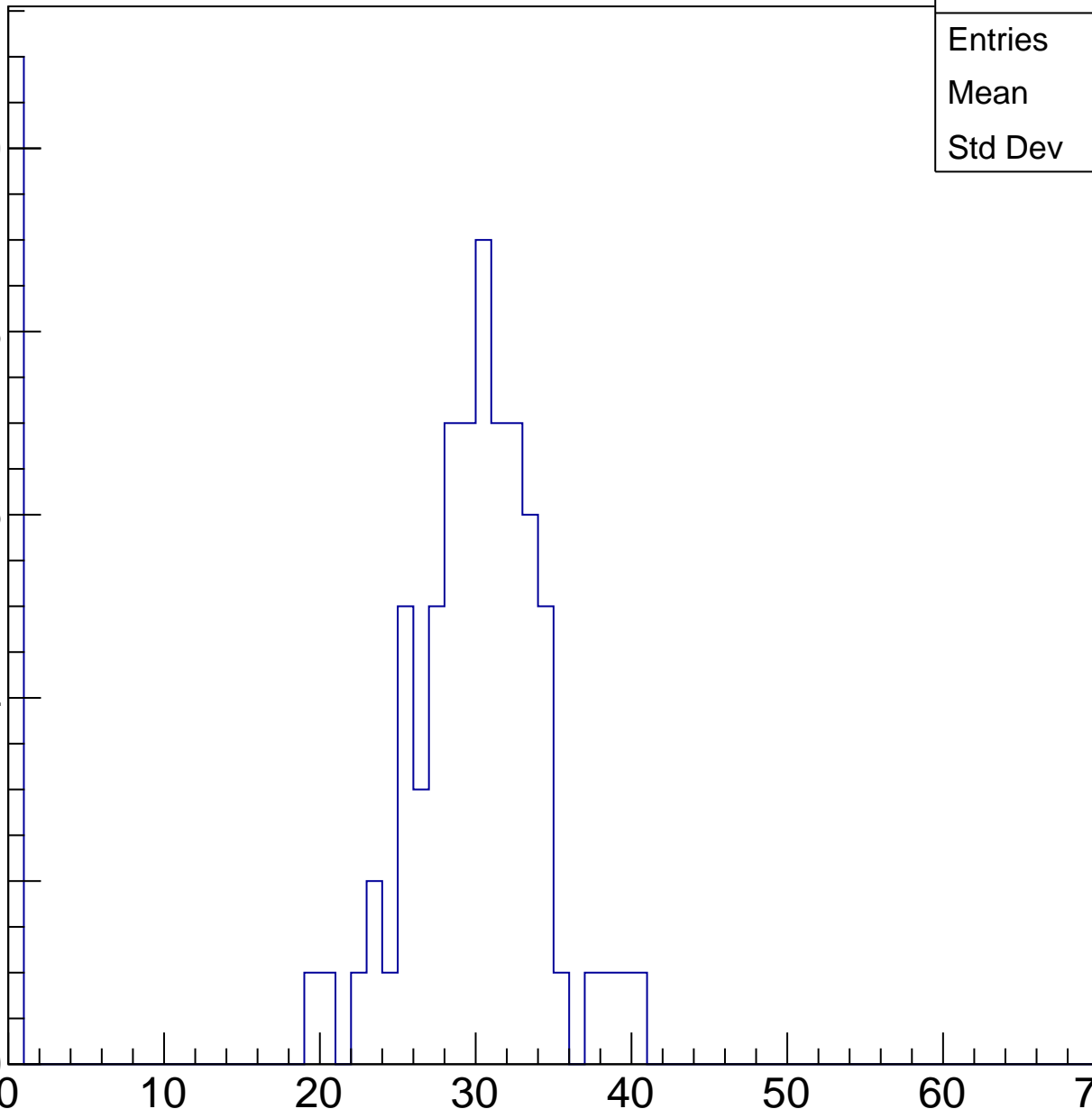
40

50

60

70

ampl

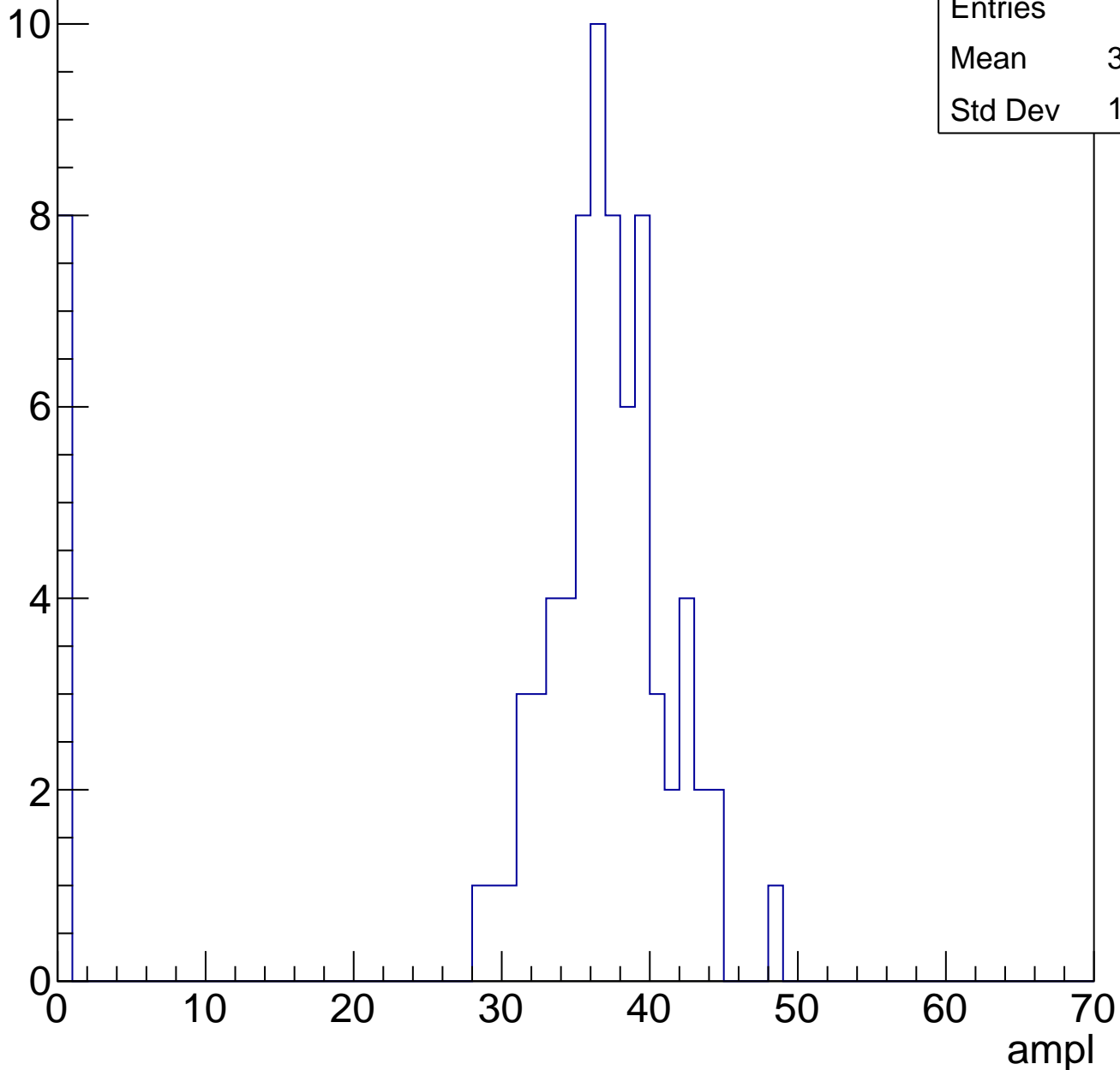


# B1L103S, U4-ch56, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 79    |
| Mean    | 33.06 |
| Std Dev | 11.66 |

Entry

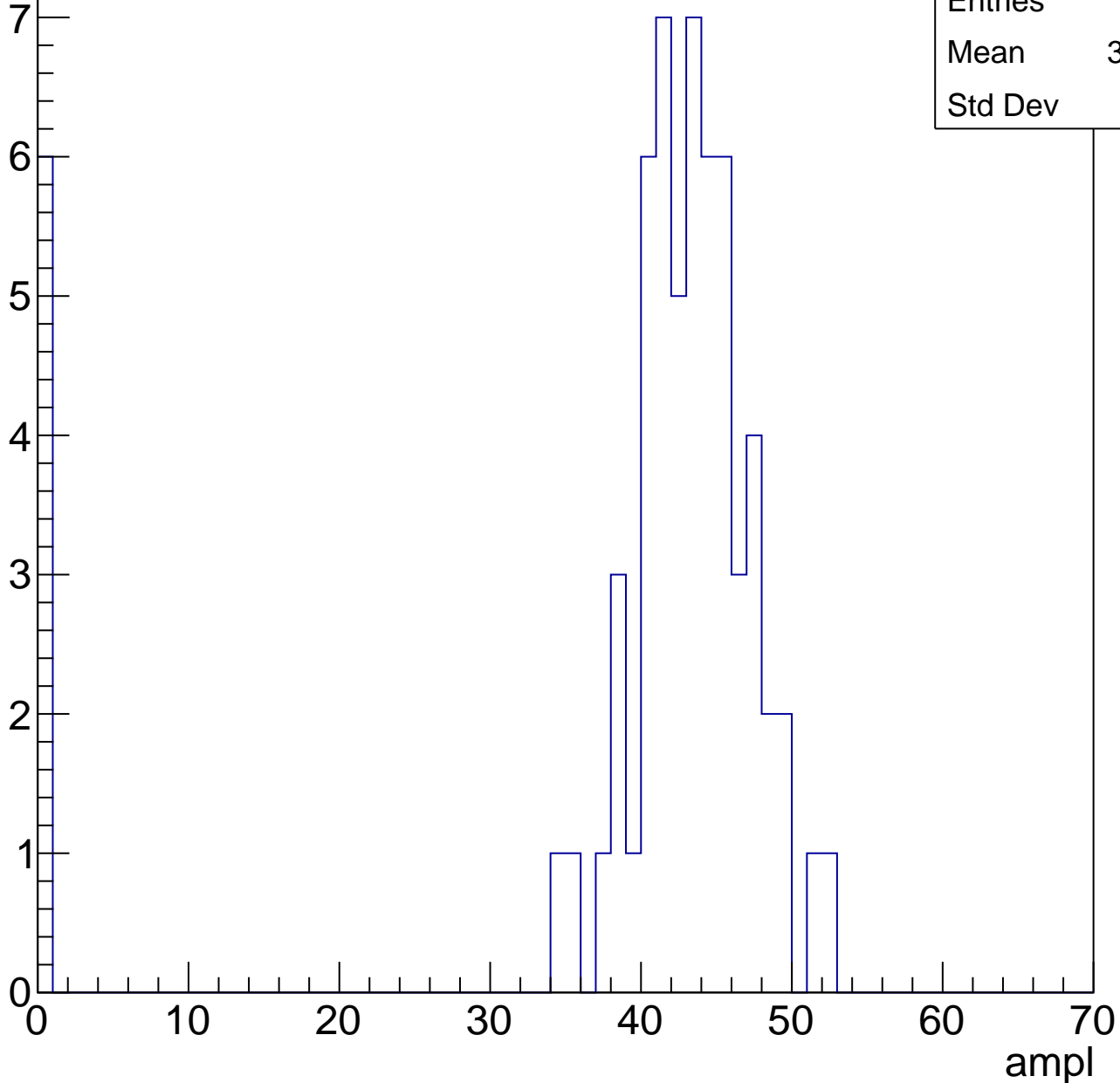


# B1L103S, U4-ch56, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 63    |
| Mean    | 38.95 |
| Std Dev | 13.1  |

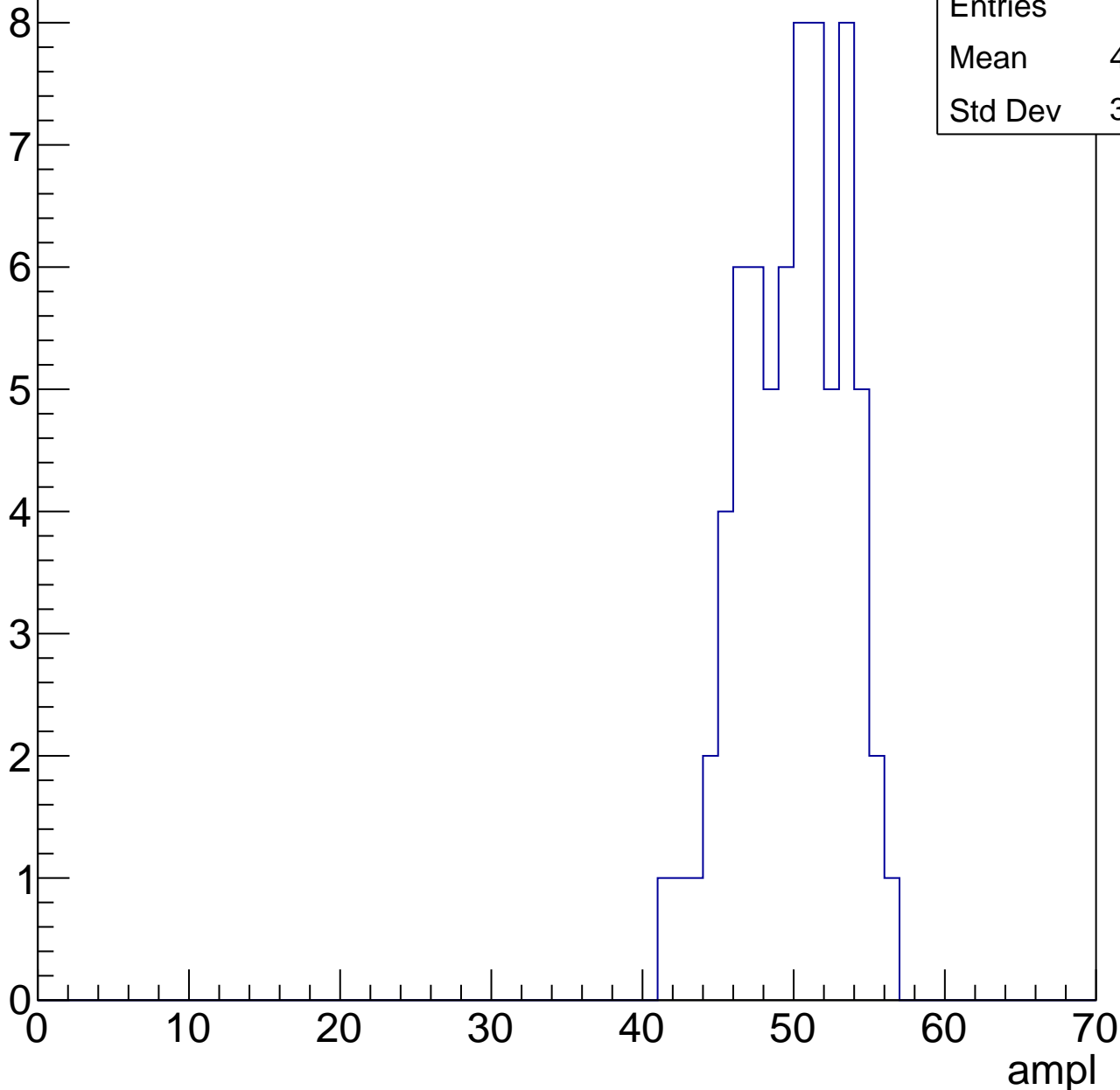


# B1L103S, U4-ch56, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

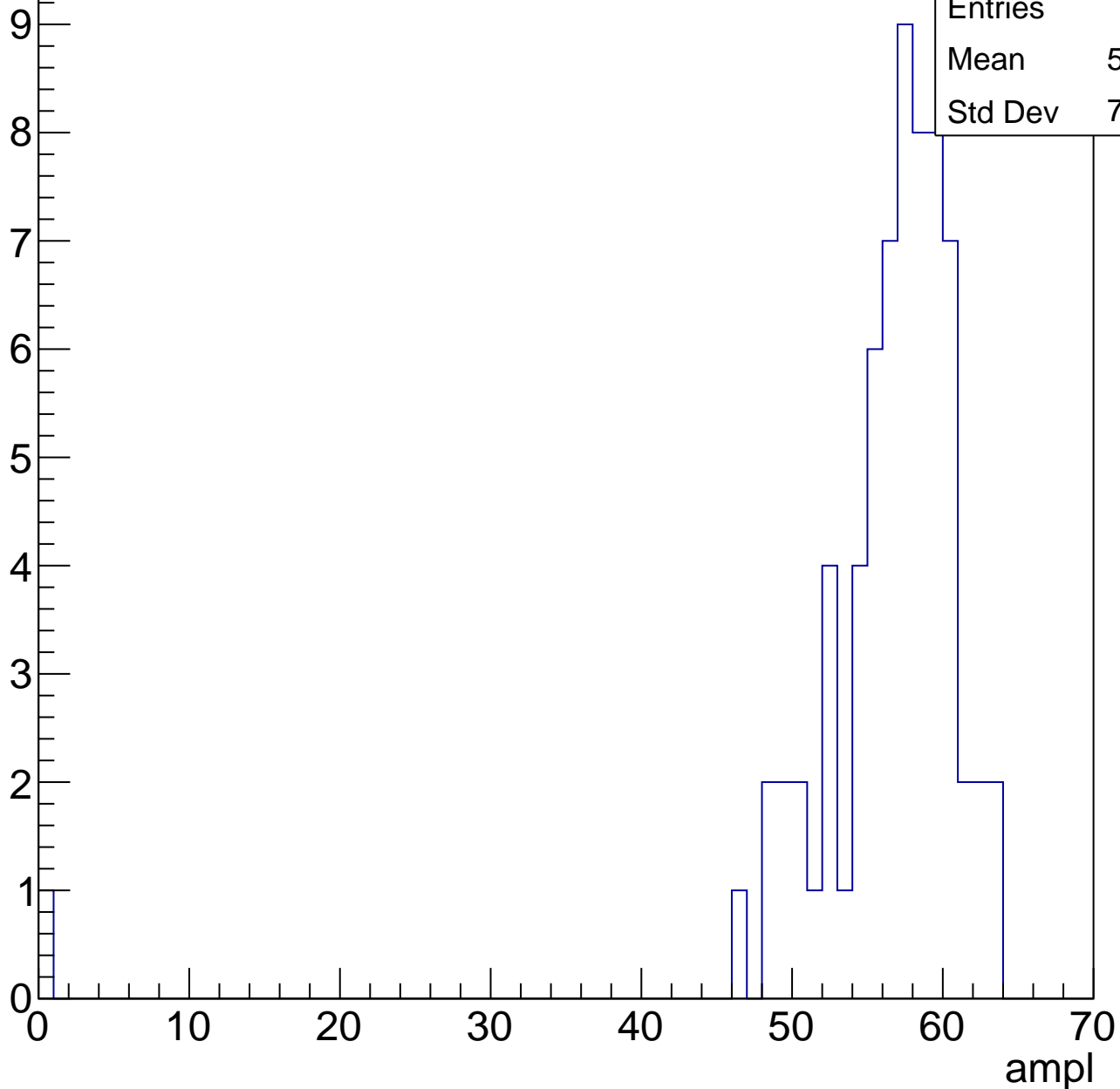
|         |       |
|---------|-------|
| Entries | 69    |
| Mean    | 49.48 |
| Std Dev | 3.382 |



# B1L103S, U4-ch56, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

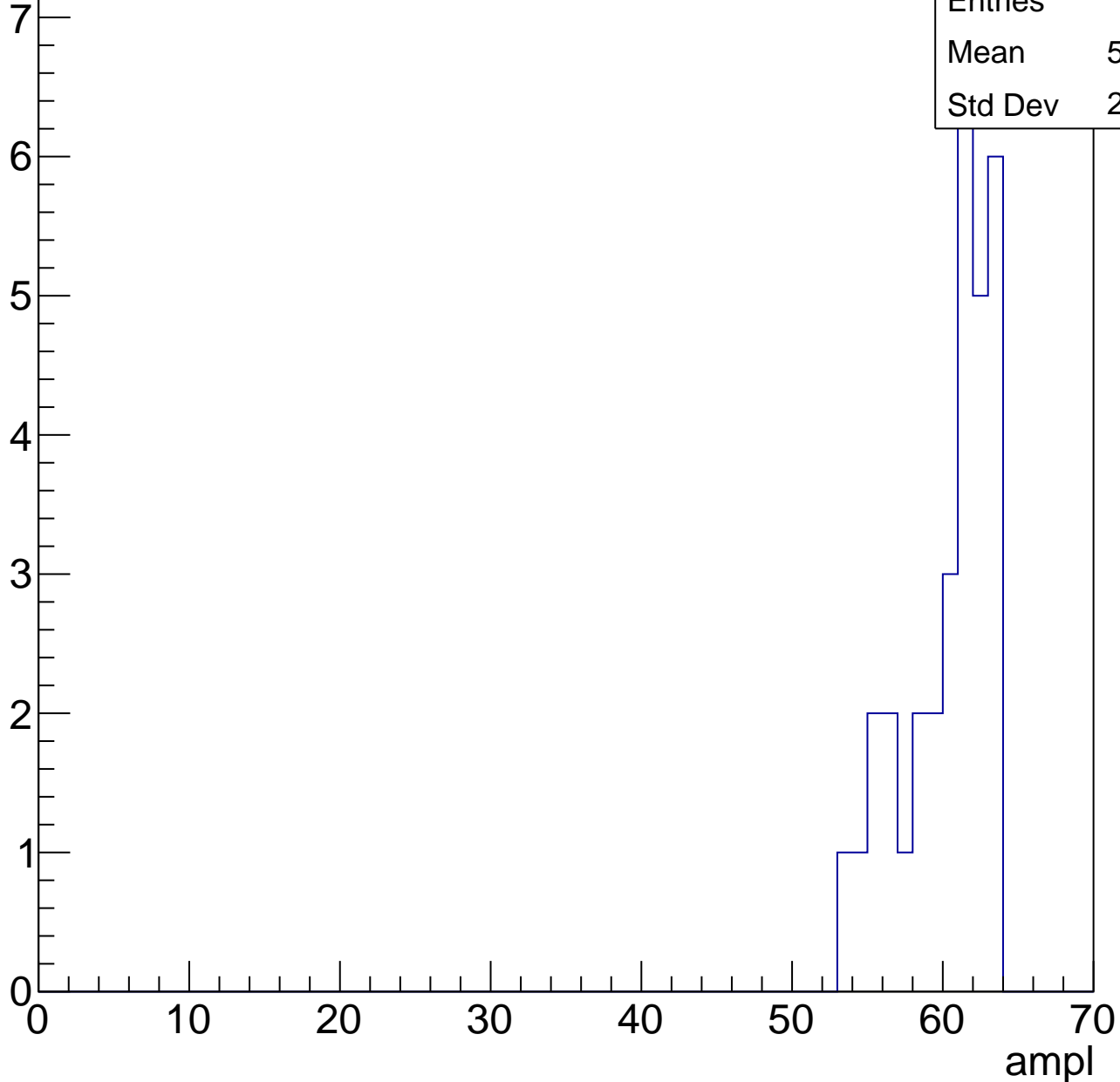
Entry



# B1L103S, U4-ch56, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

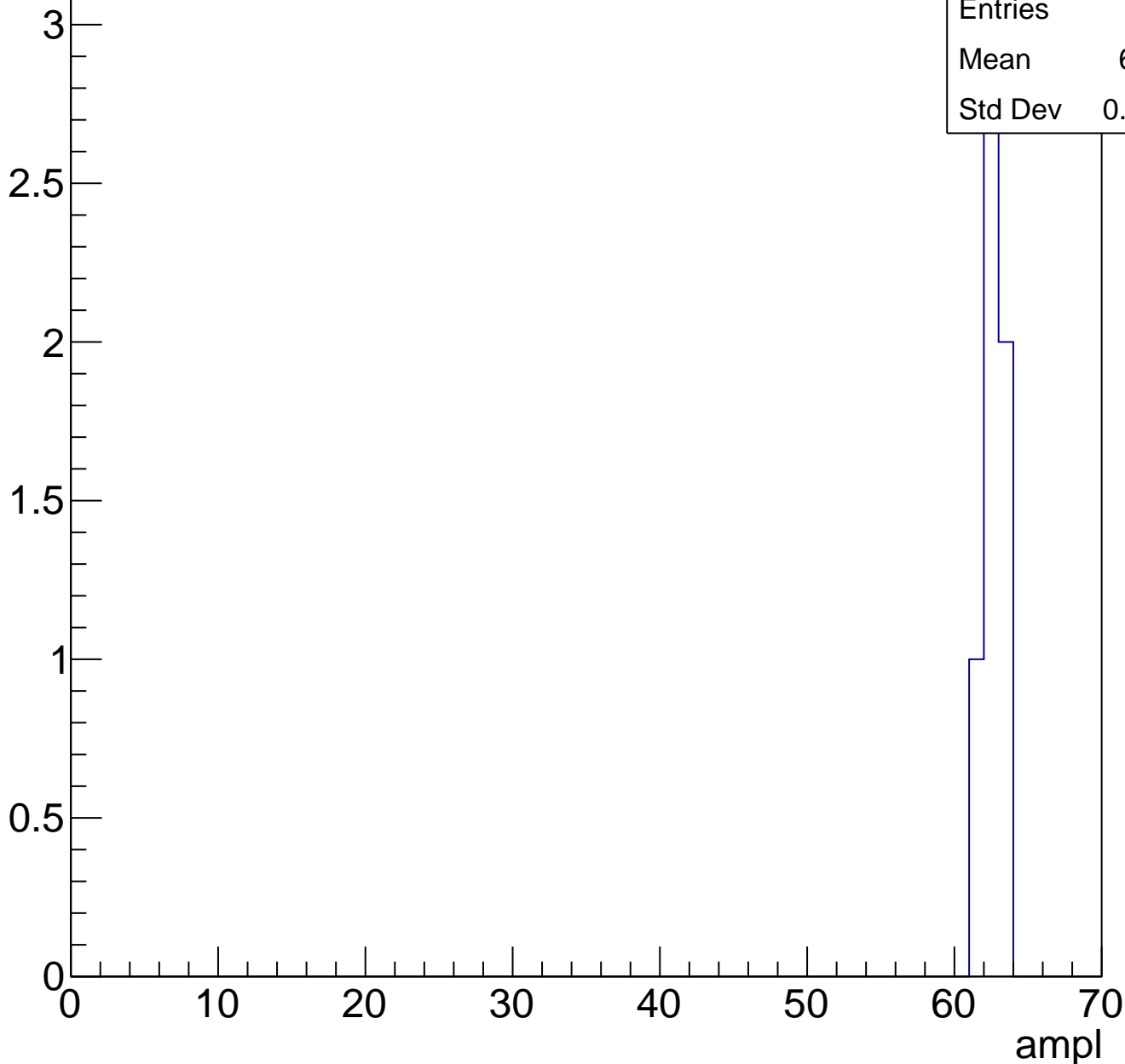
Entry



# B1L103S, U4-ch56, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U4-ch56, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

|         |    |
|---------|----|
| Entries | 19 |
| Mean    | 0  |
| Std Dev | 0  |

ampl

# B1L103S, U4-ch57, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 82    |
| Mean    | 23.74 |
| Std Dev | 11.66 |

Entry

14  
12  
10  
8  
6  
4  
2  
0

0

10

20

30

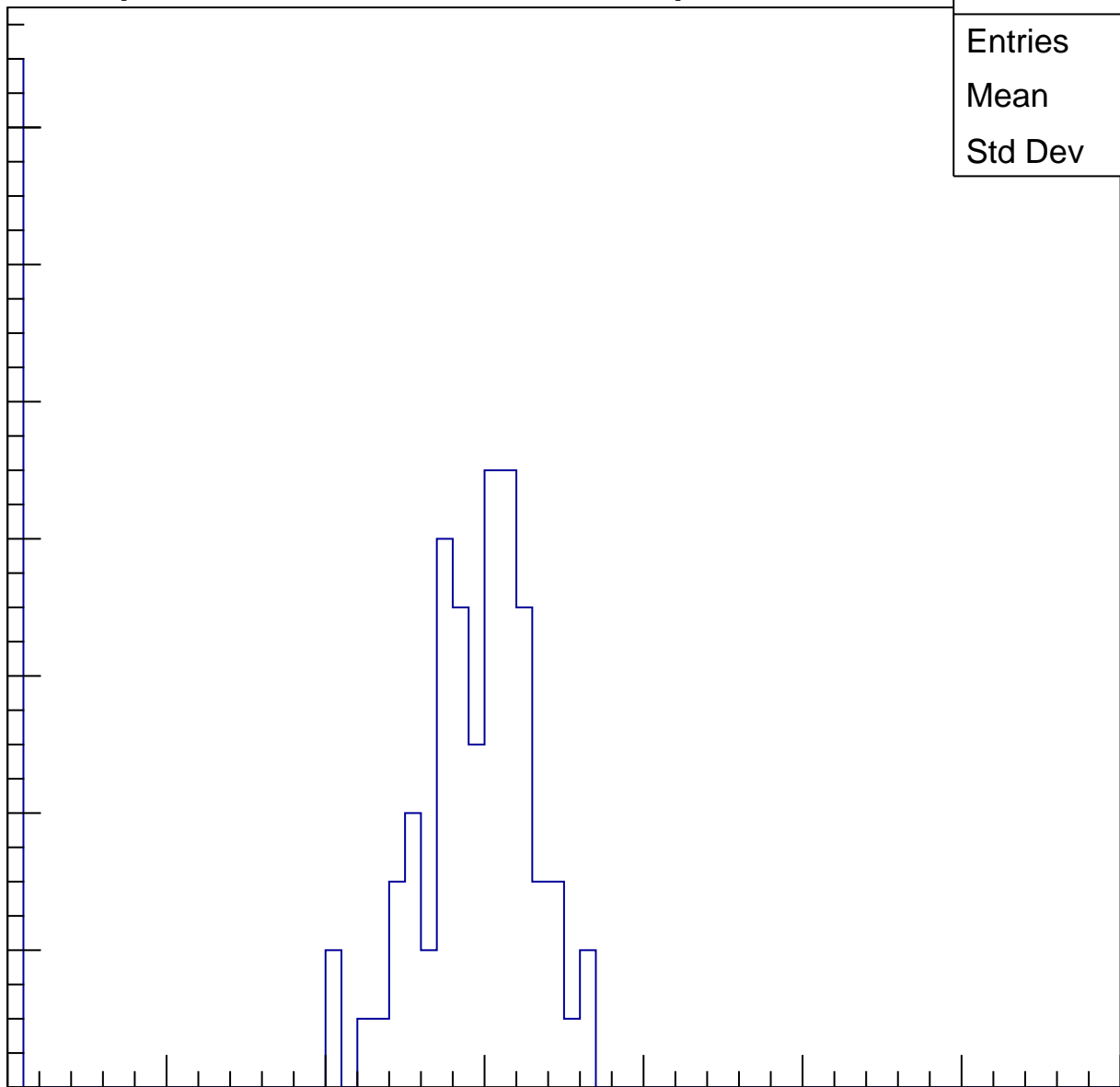
40

50

60

70

ampl

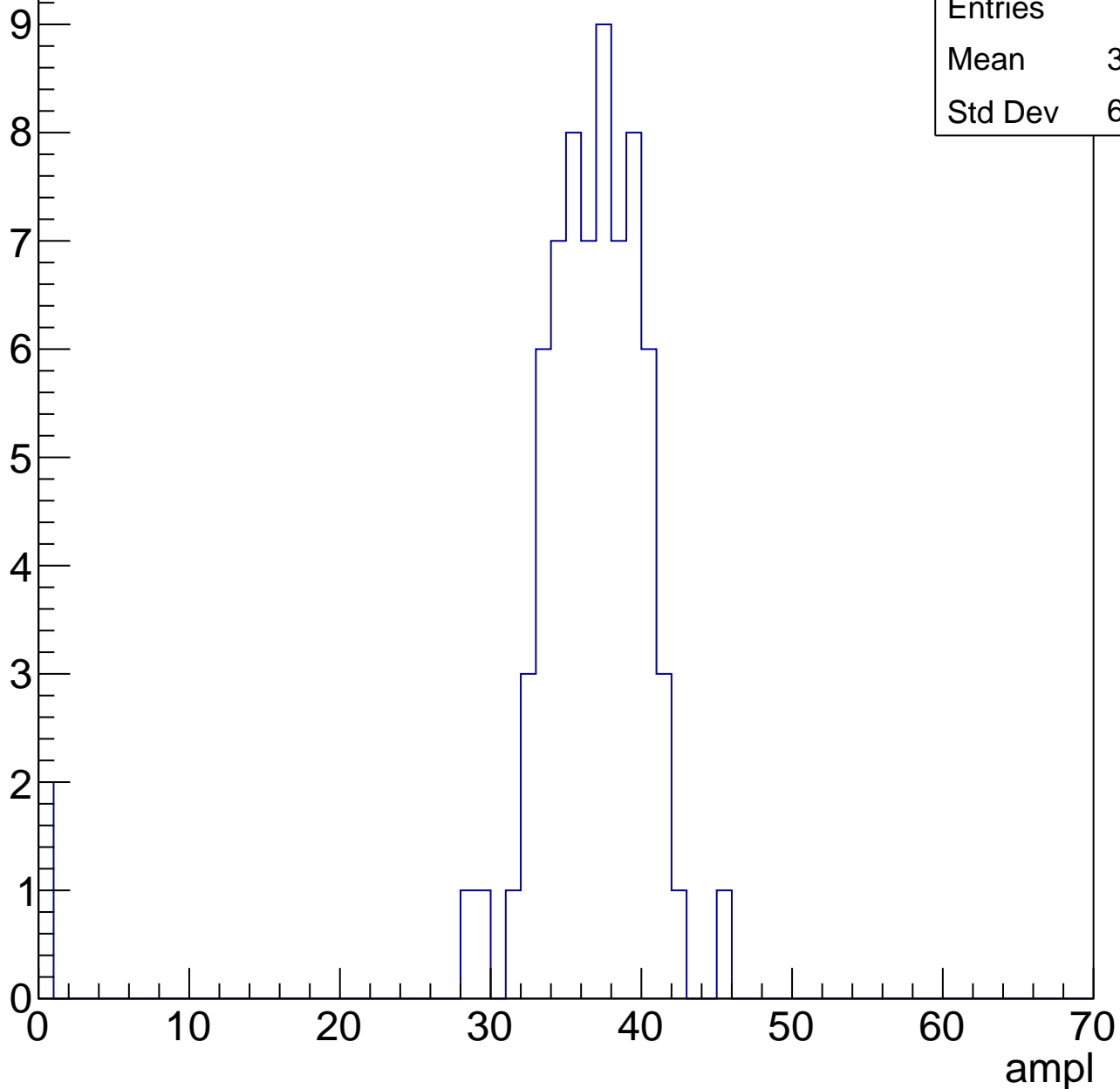


# B1L103S, U4-ch57, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

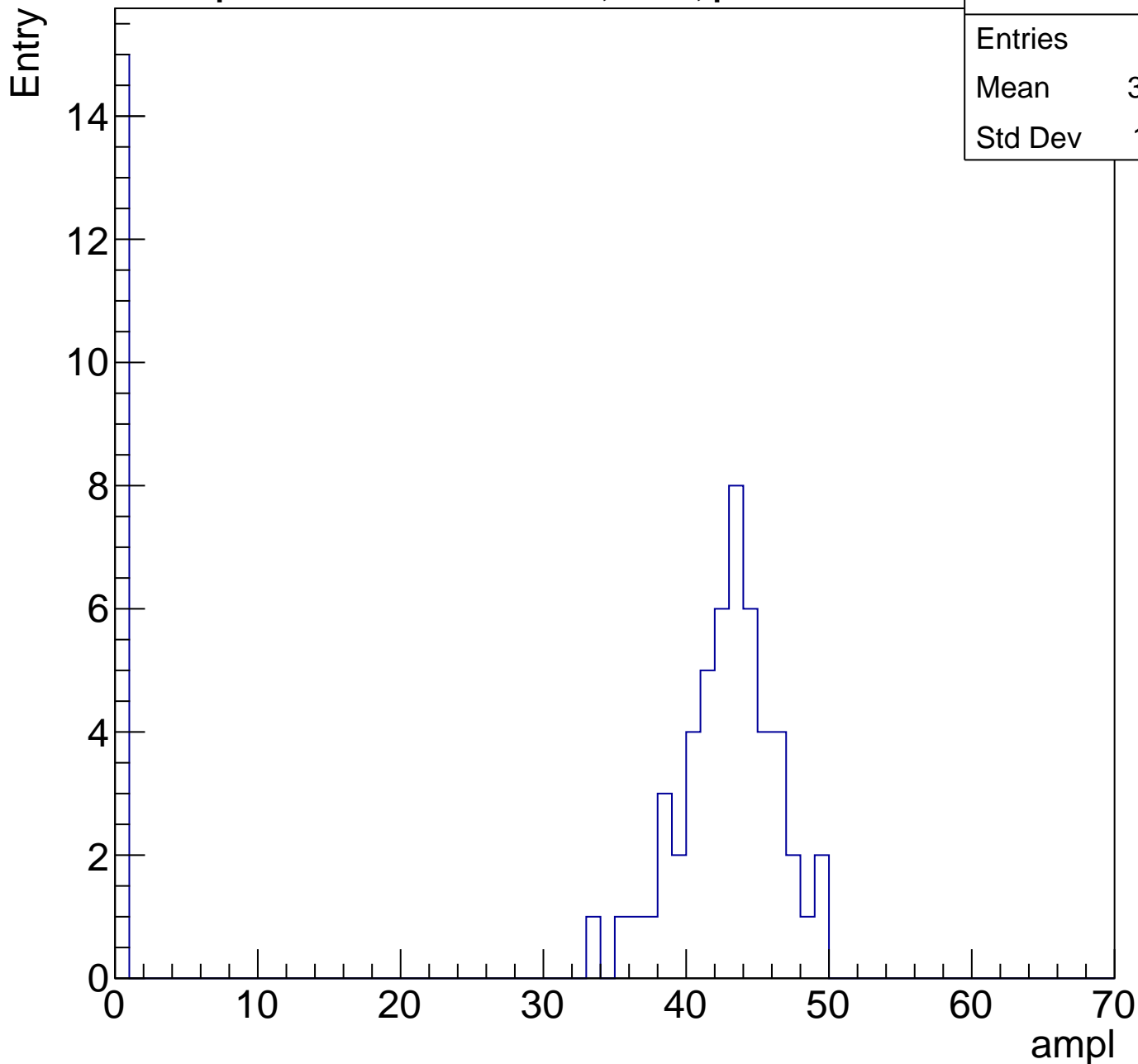
|         |       |
|---------|-------|
| Entries | 71    |
| Mean    | 35.39 |
| Std Dev | 6.754 |



# B1L103S, U4-ch57, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 66    |
| Mean    | 32.76 |
| Std Dev | 18.01 |

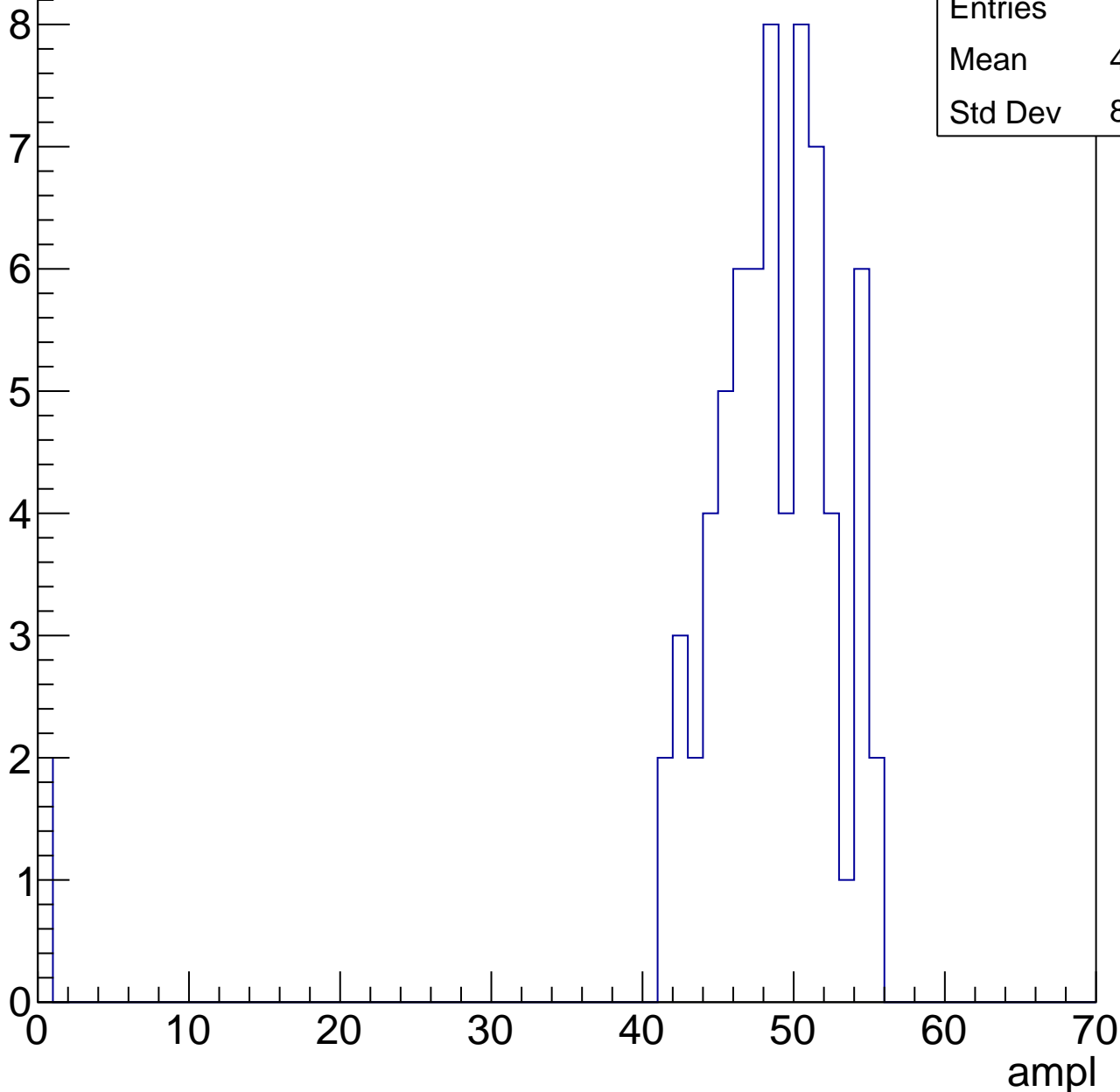


# B1L103S, U4-ch57, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 70    |
| Mean    | 46.93 |
| Std Dev | 8.803 |

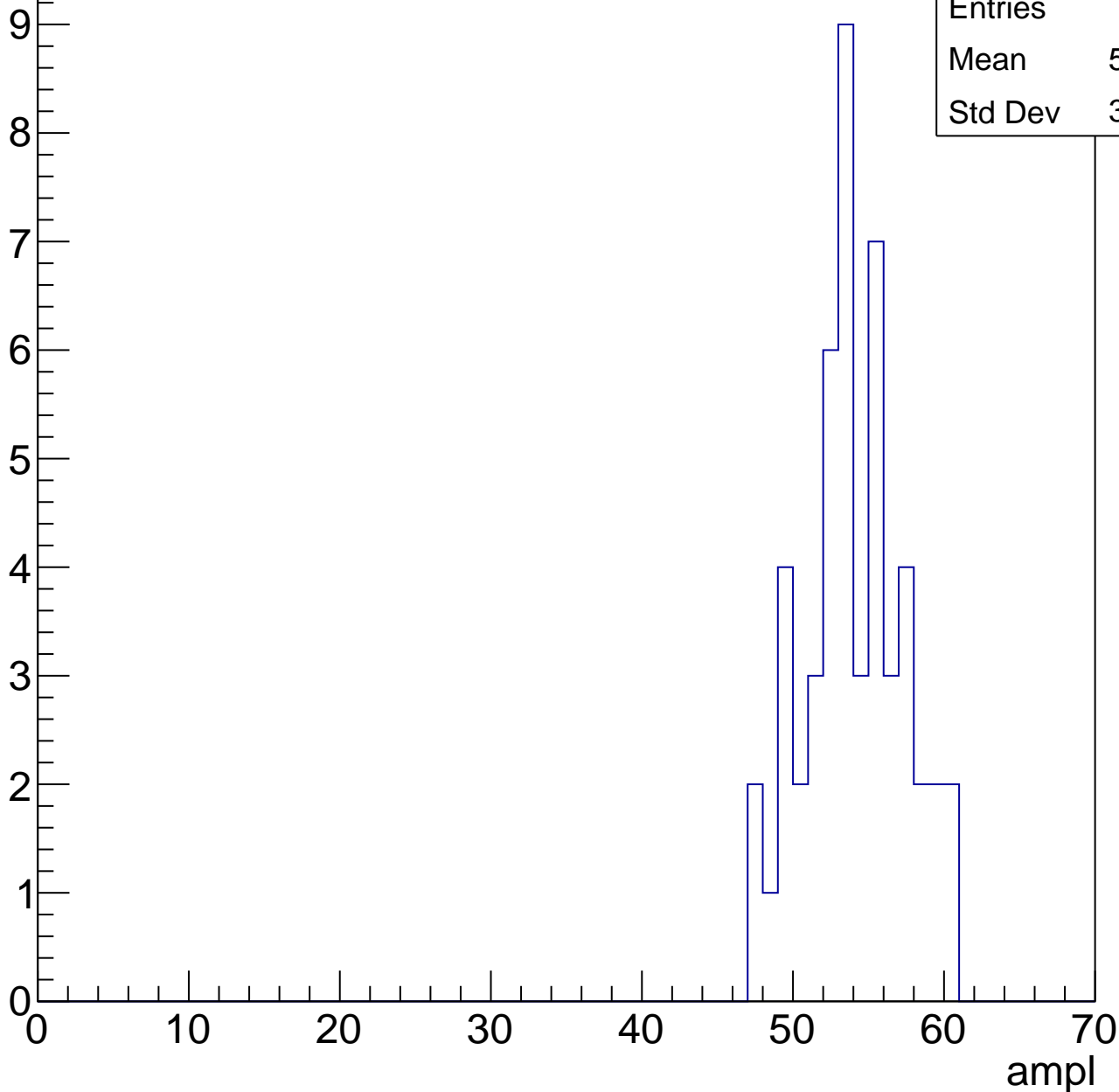


# B1L103S, U4-ch57, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 50    |
| Mean    | 53.54 |
| Std Dev | 3.239 |



# B1L103S, U4-ch57, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

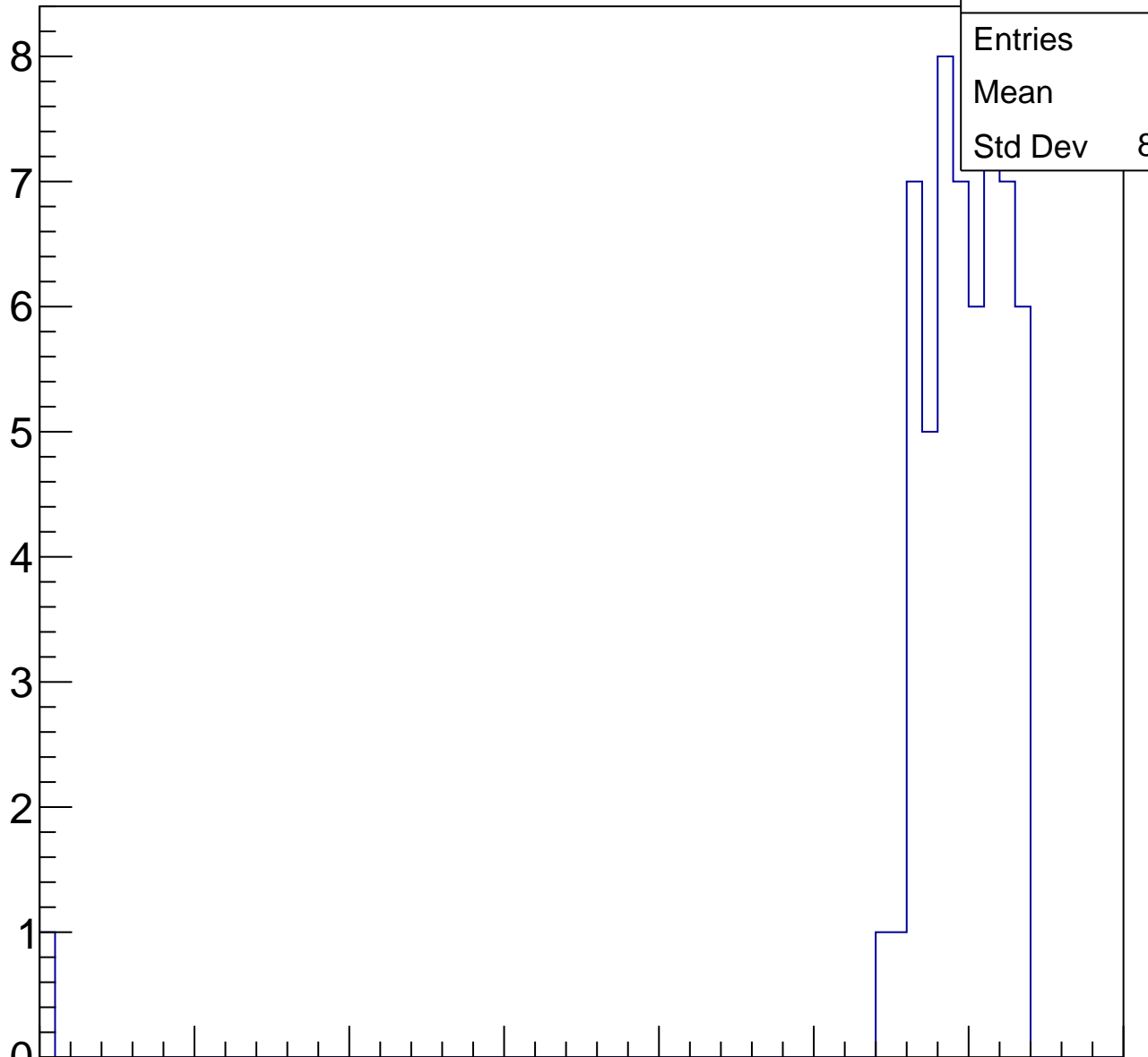
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

|         |       |
|---------|-------|
| Entries | 57    |
| Mean    | 58.3  |
| Std Dev | 8.146 |

ampl

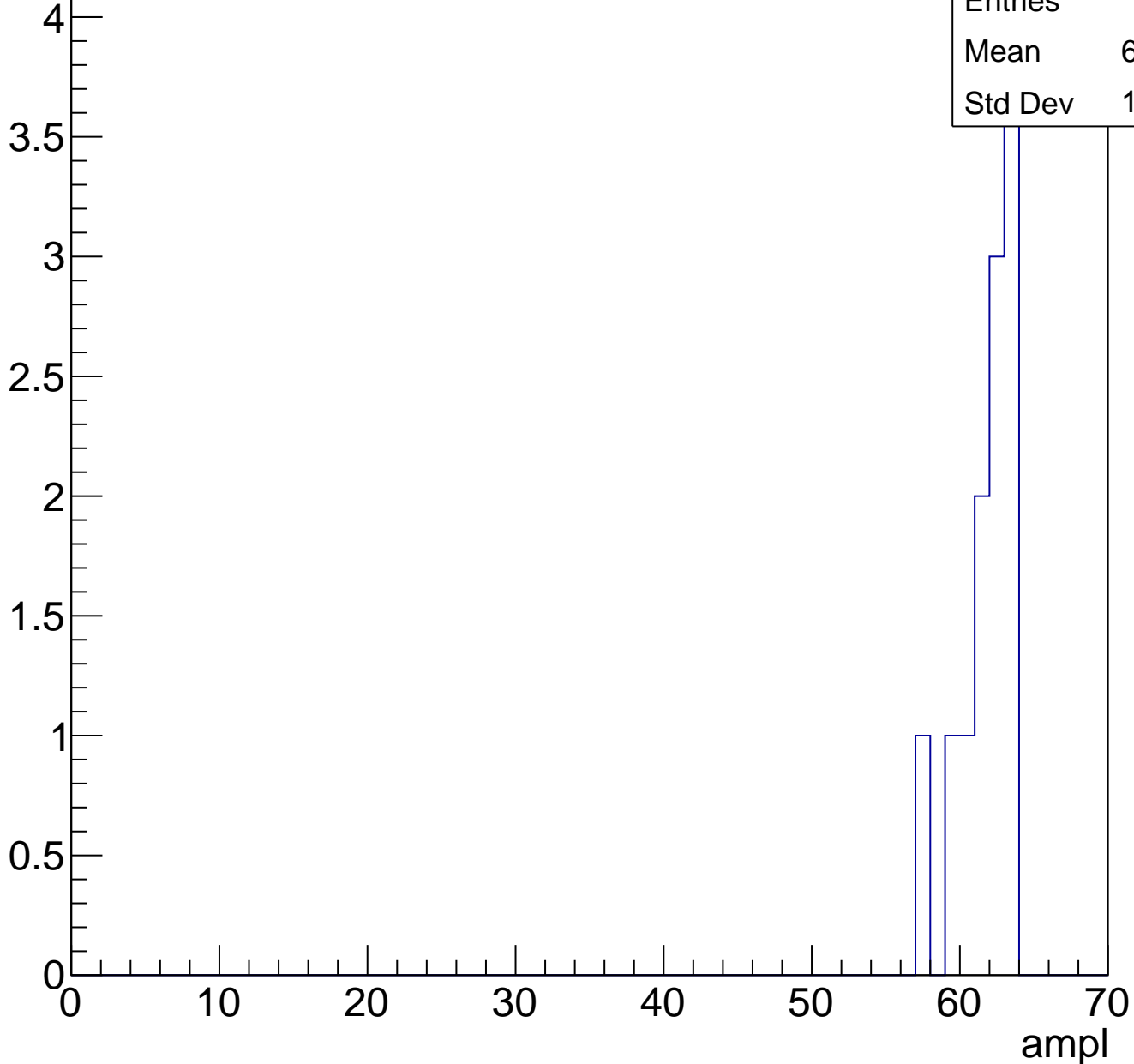
0 10 20 30 40 50 60 70



# B1L103S, U4-ch57, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U4-ch57, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 20    |
| Mean    | 3     |
| Std Dev | 13.08 |

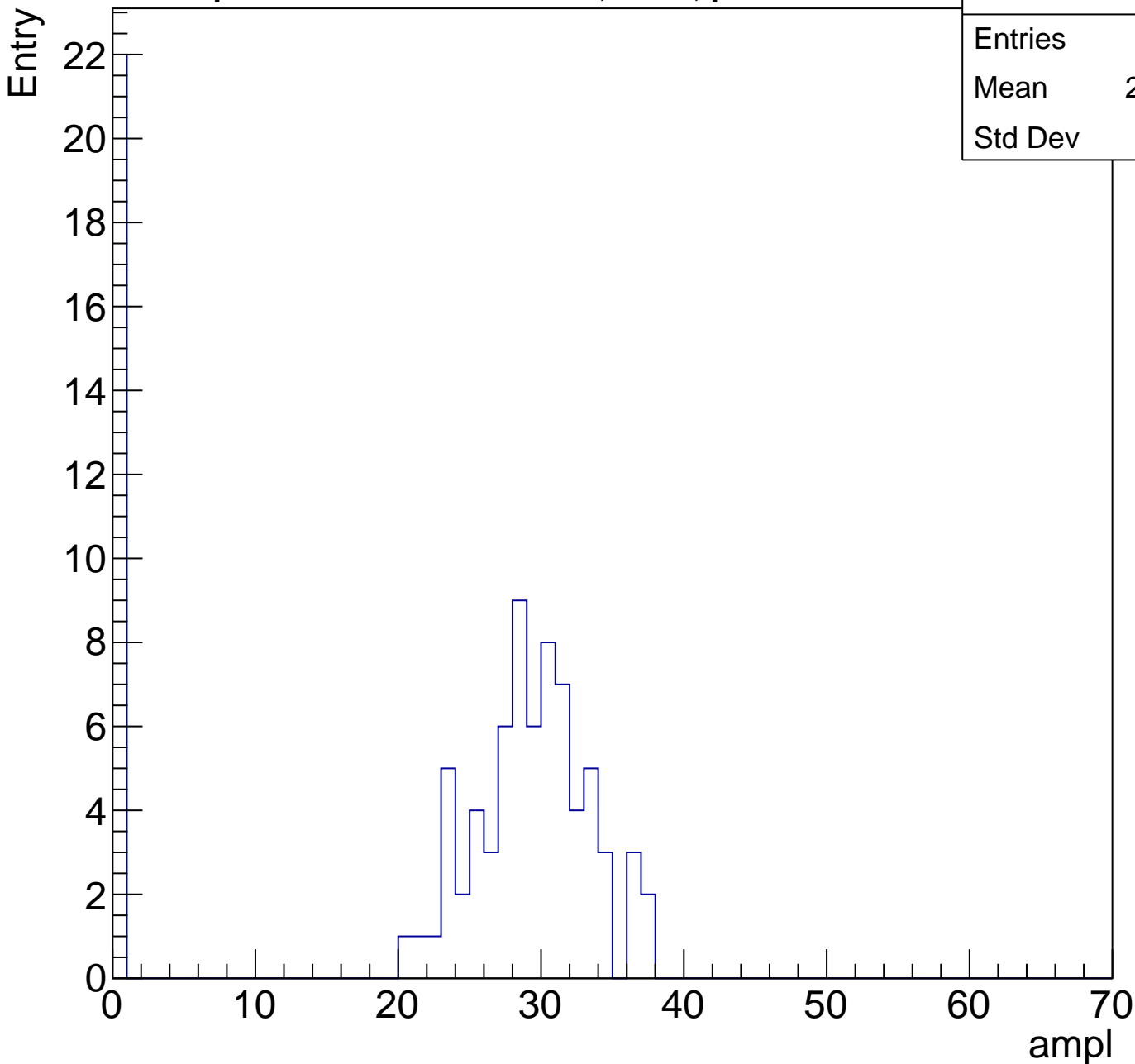
Entry



# B1L103S, U4-ch58, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 92    |
| Mean    | 22.02 |
| Std Dev | 12.8  |

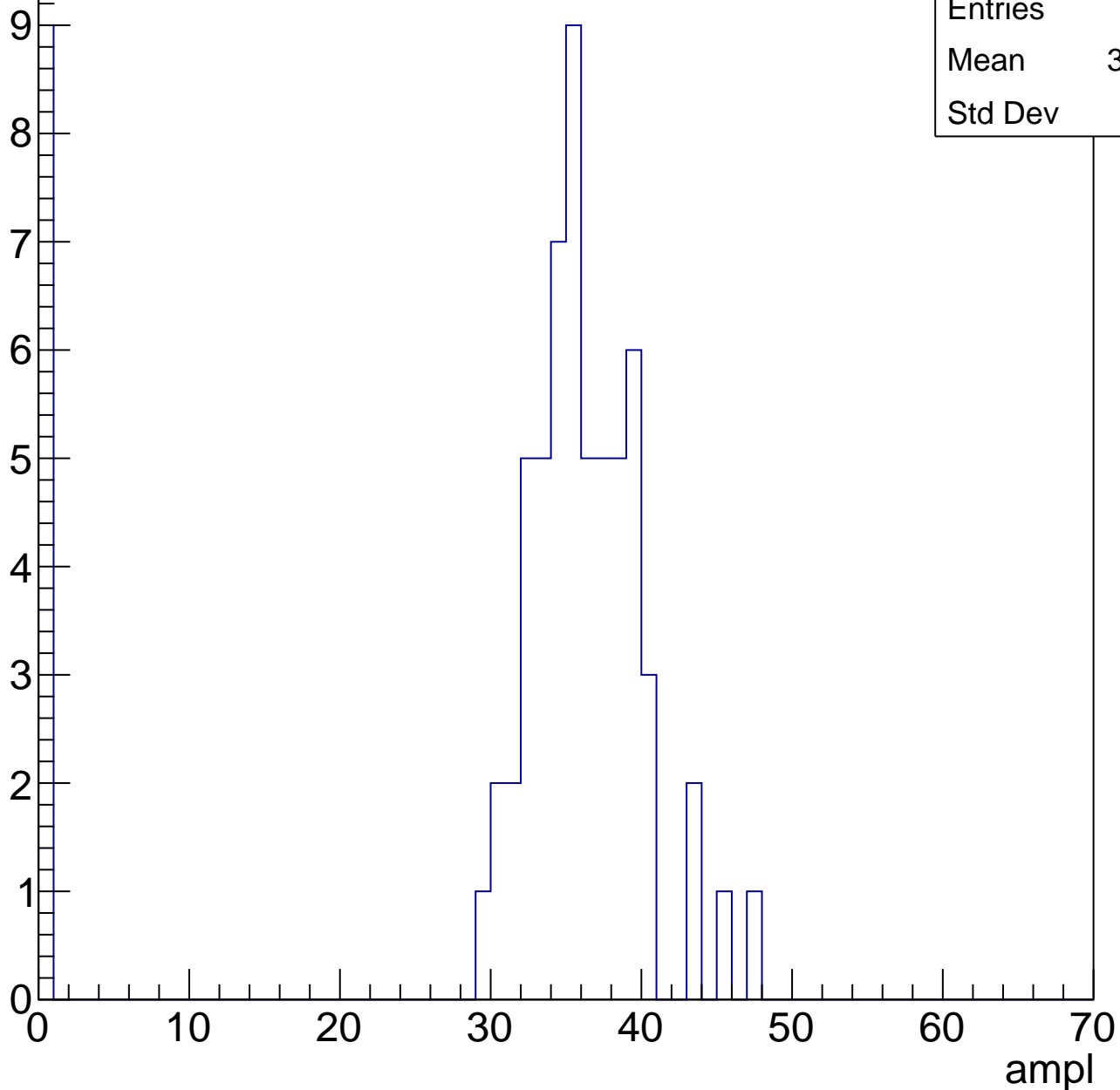


# B1L103S, U4-ch58, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 68    |
| Mean    | 31.12 |
| Std Dev | 12.6  |

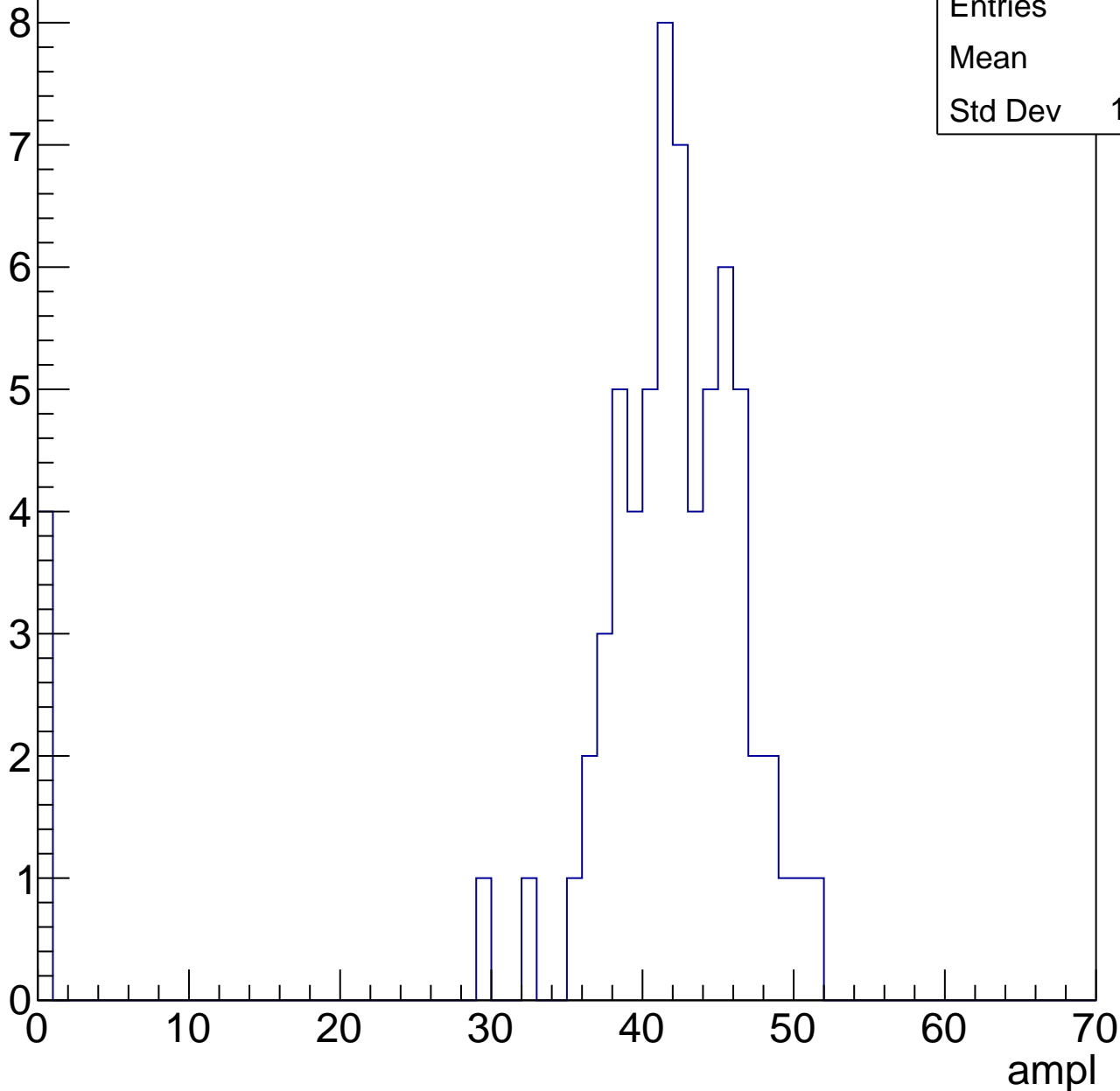


# B1L103S, U4-ch58, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

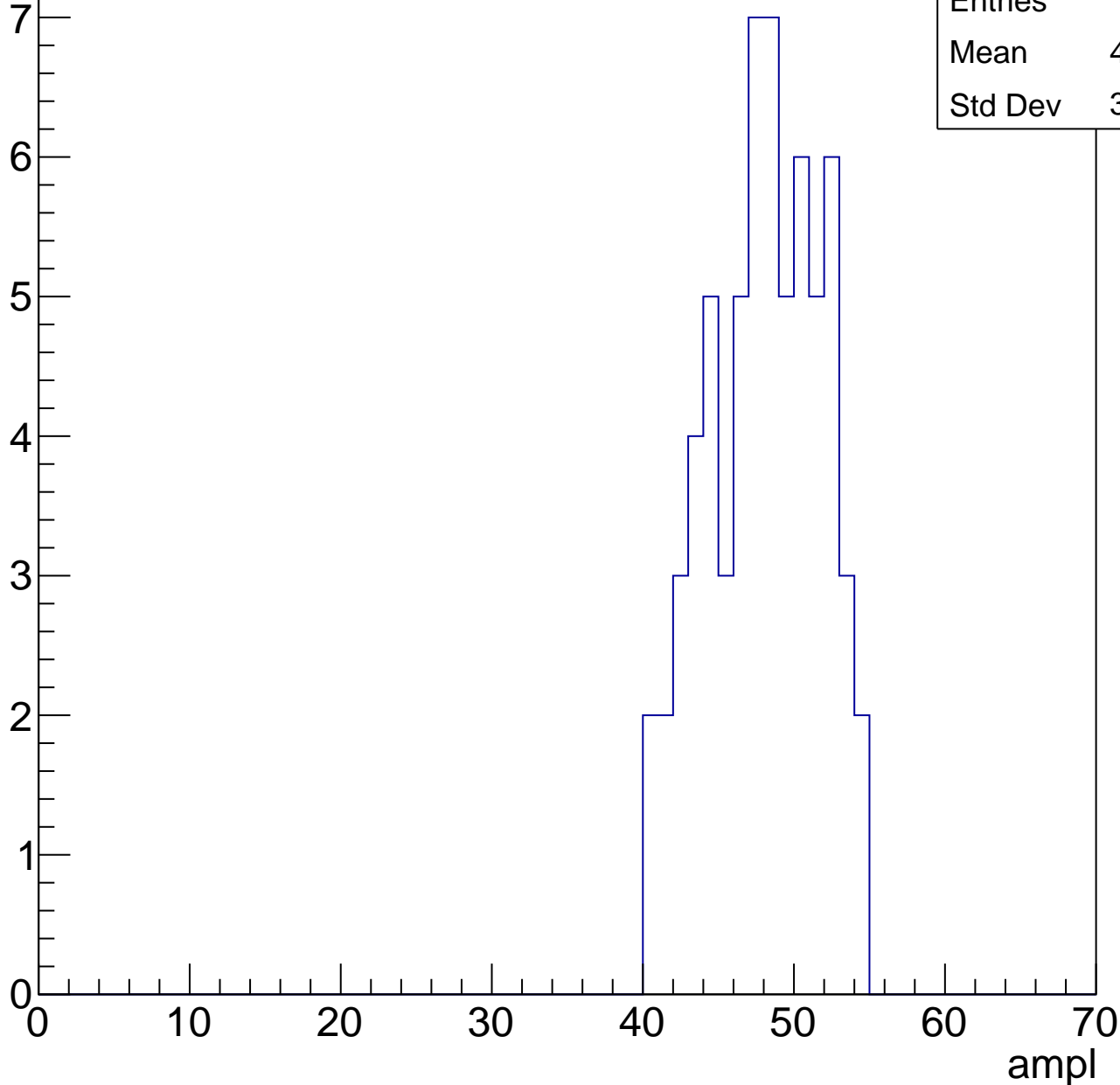
|         |       |
|---------|-------|
| Entries | 68    |
| Mean    | 39.4  |
| Std Dev | 10.63 |



# B1L103S, U4-ch58, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

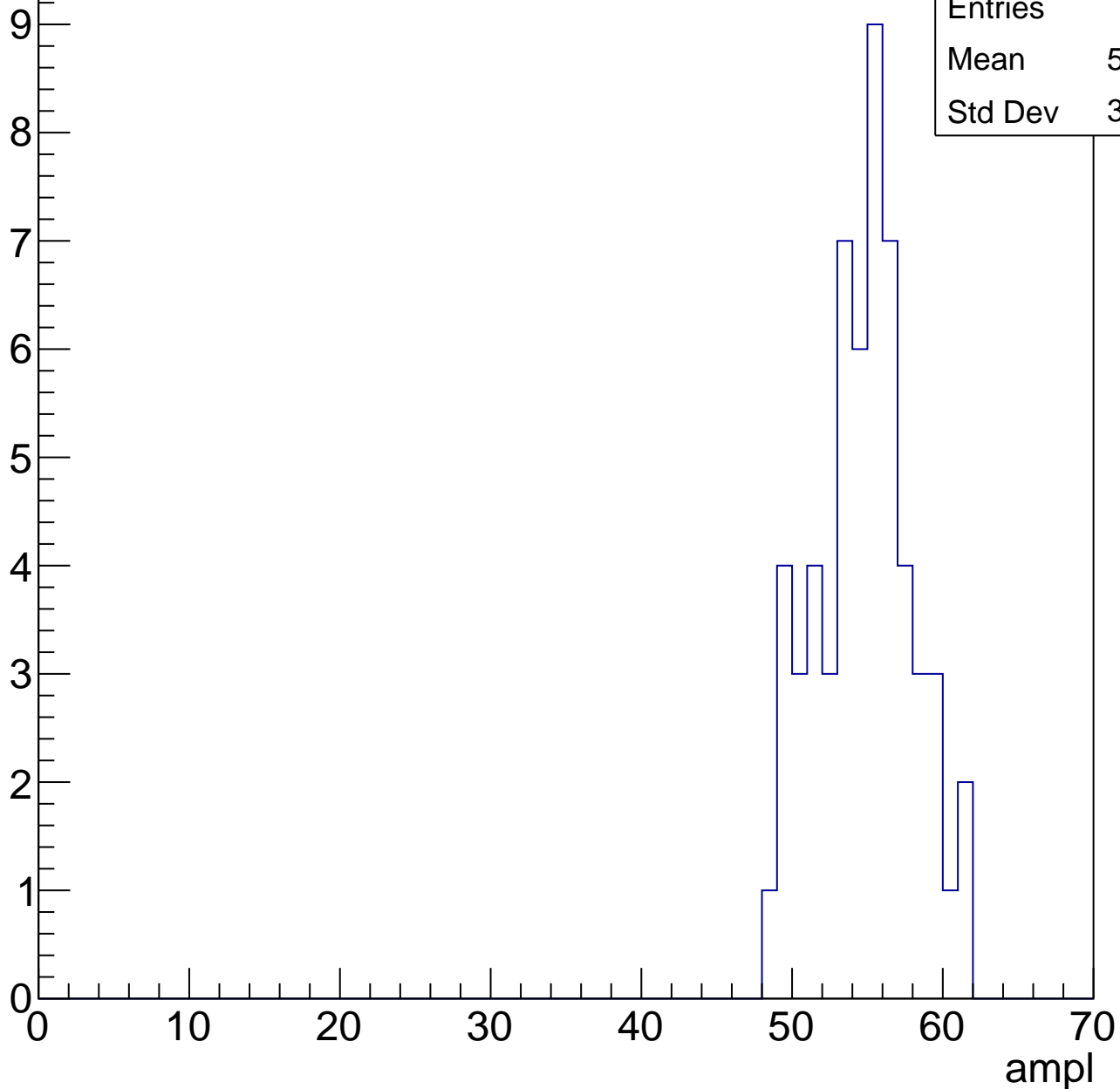


|         |       |
|---------|-------|
| Entries | 65    |
| Mean    | 47.52 |
| Std Dev | 3.659 |

# B1L103S, U4-ch58, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

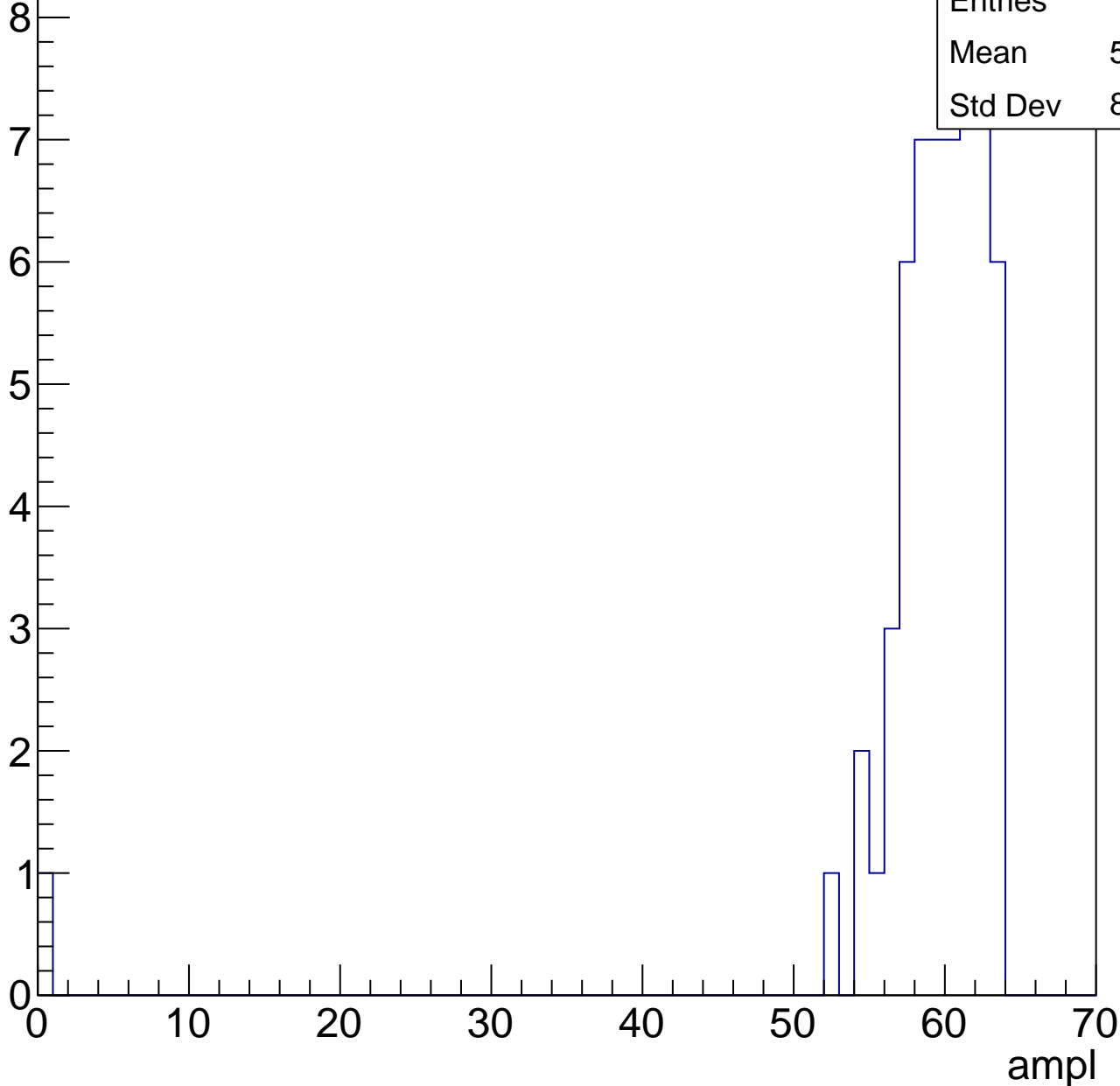


# B1L103S, U4-ch58, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

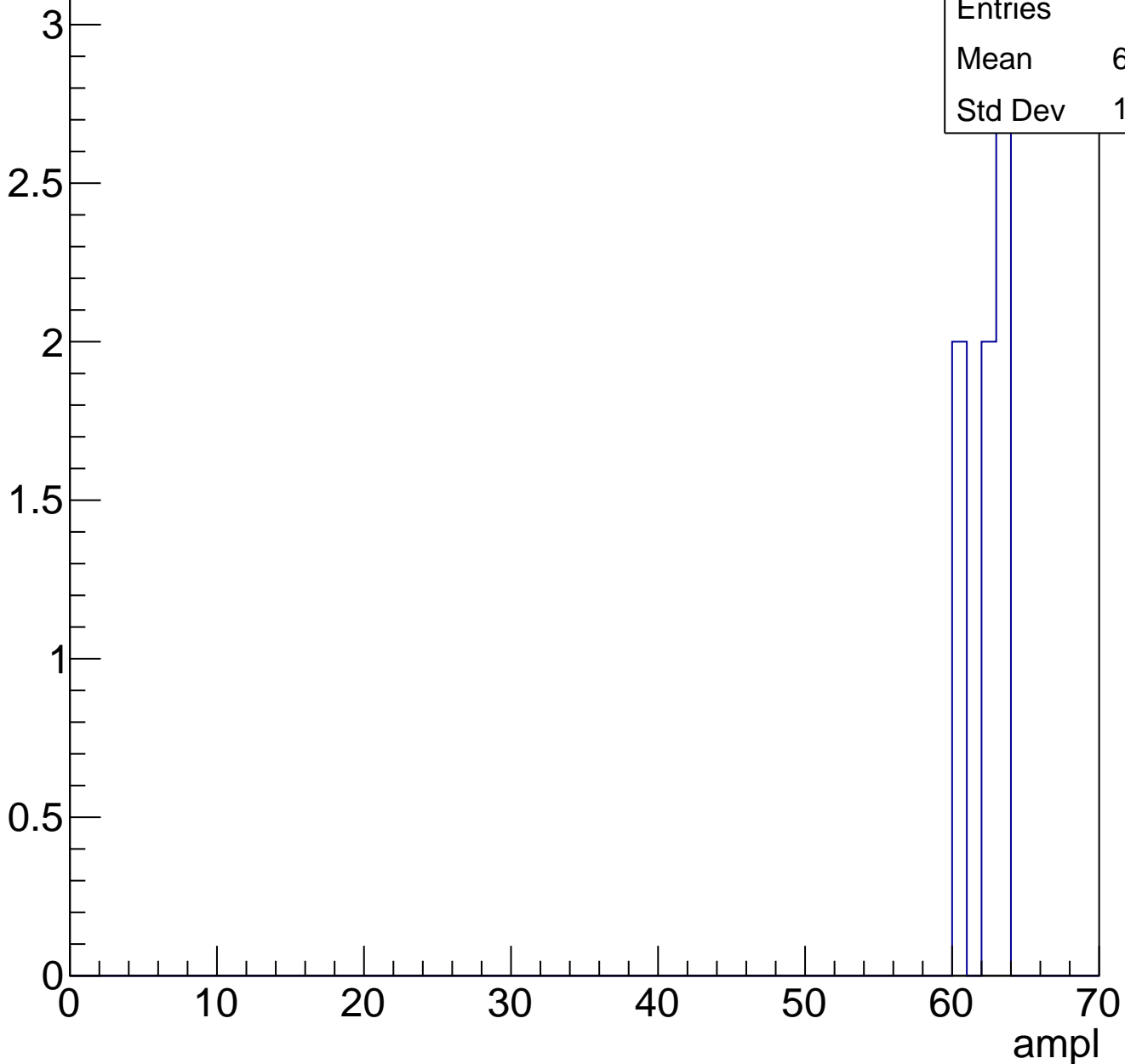
|         |       |
|---------|-------|
| Entries | 57    |
| Mean    | 58.35 |
| Std Dev | 8.205 |



# B1L103S, U4-ch58, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U4-ch58, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 20    |
| Mean    | 3.15  |
| Std Dev | 13.73 |

Entry



# B1L103S, U4-ch59, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

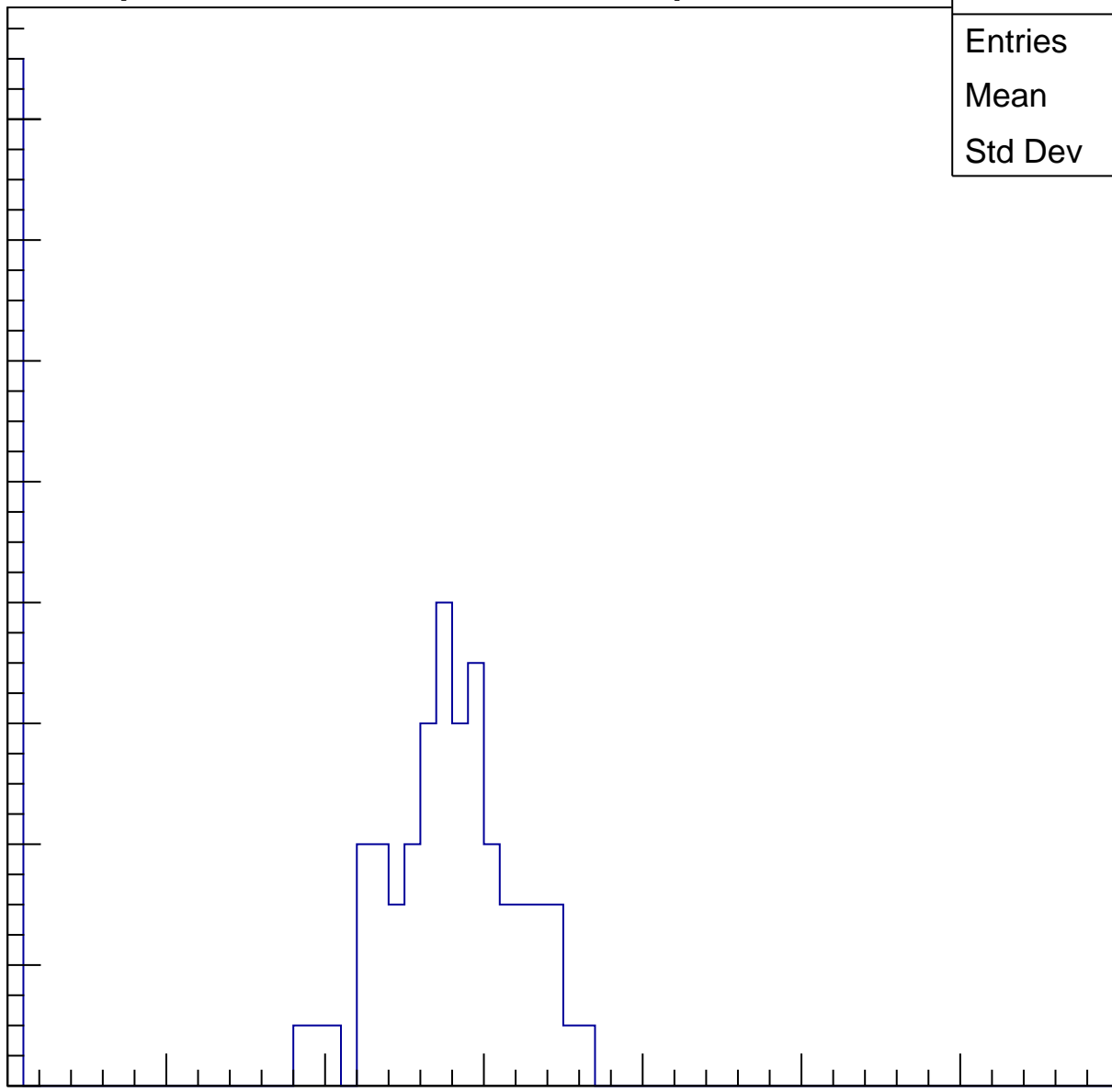
|         |       |
|---------|-------|
| Entries | 80    |
| Mean    | 21.66 |
| Std Dev | 11.79 |

Entry

16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

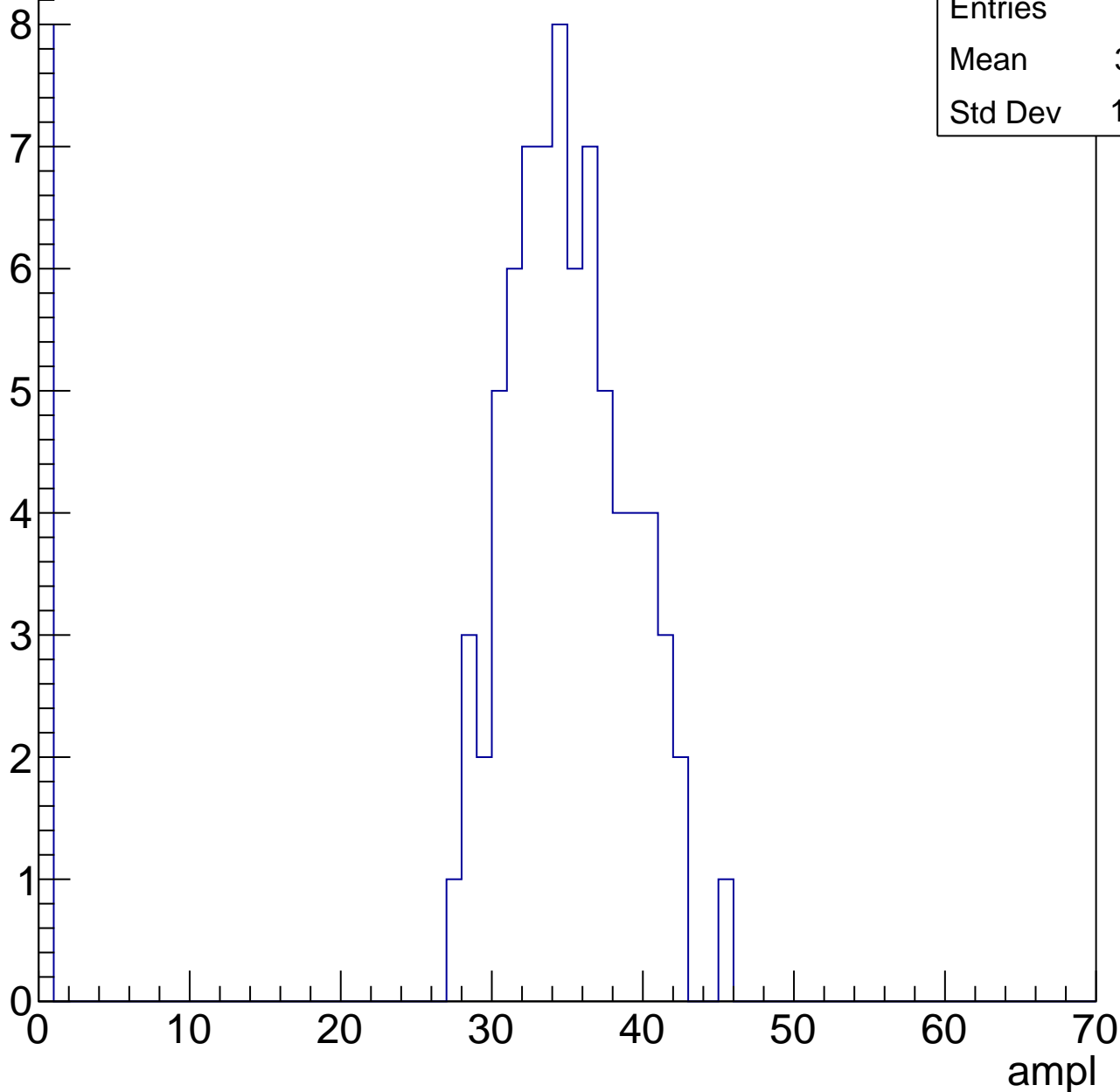


# B1L103S, U4-ch59, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 83    |
| Mean    | 31.31 |
| Std Dev | 10.87 |

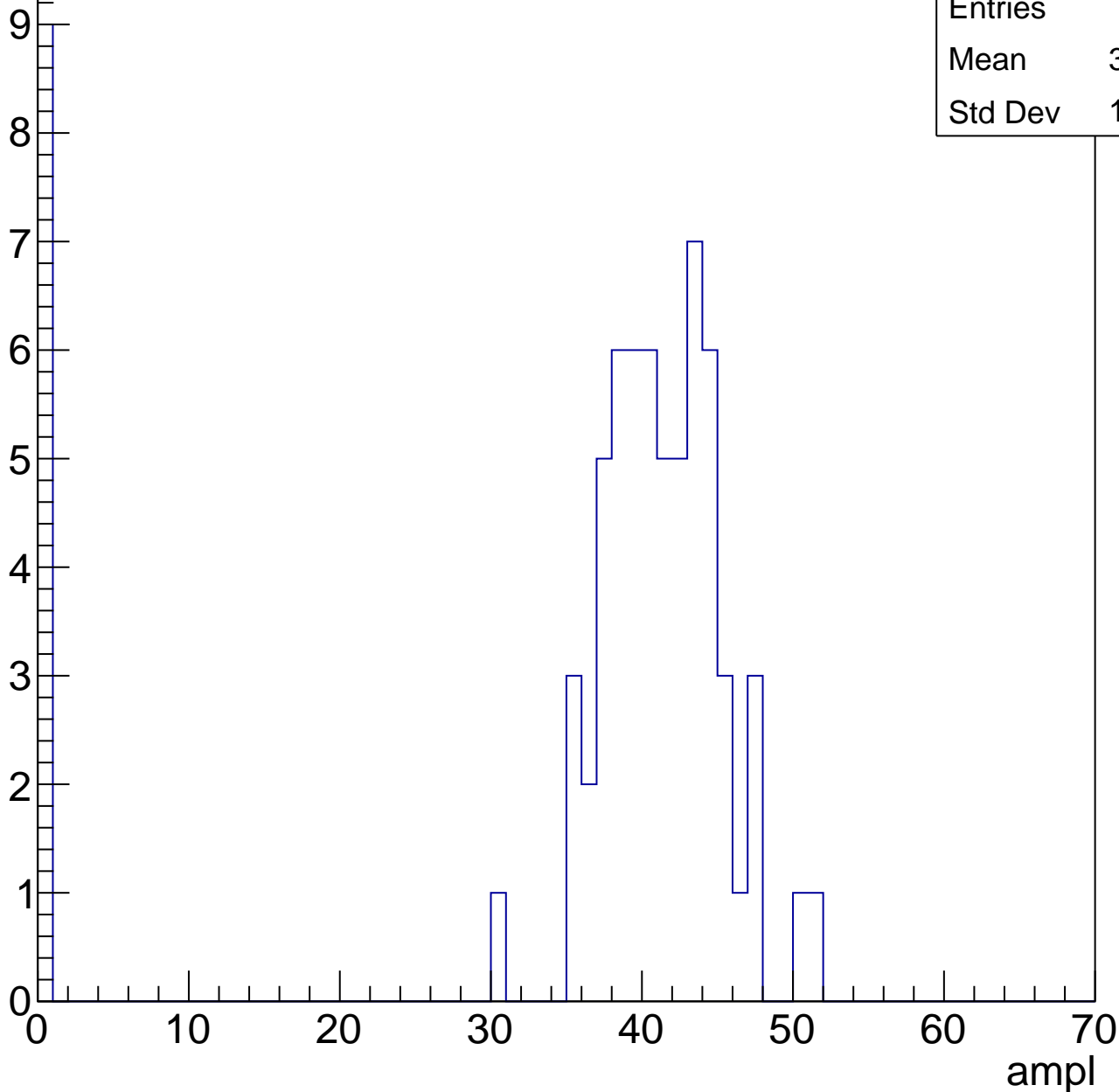


# B1L103S, U4-ch59, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

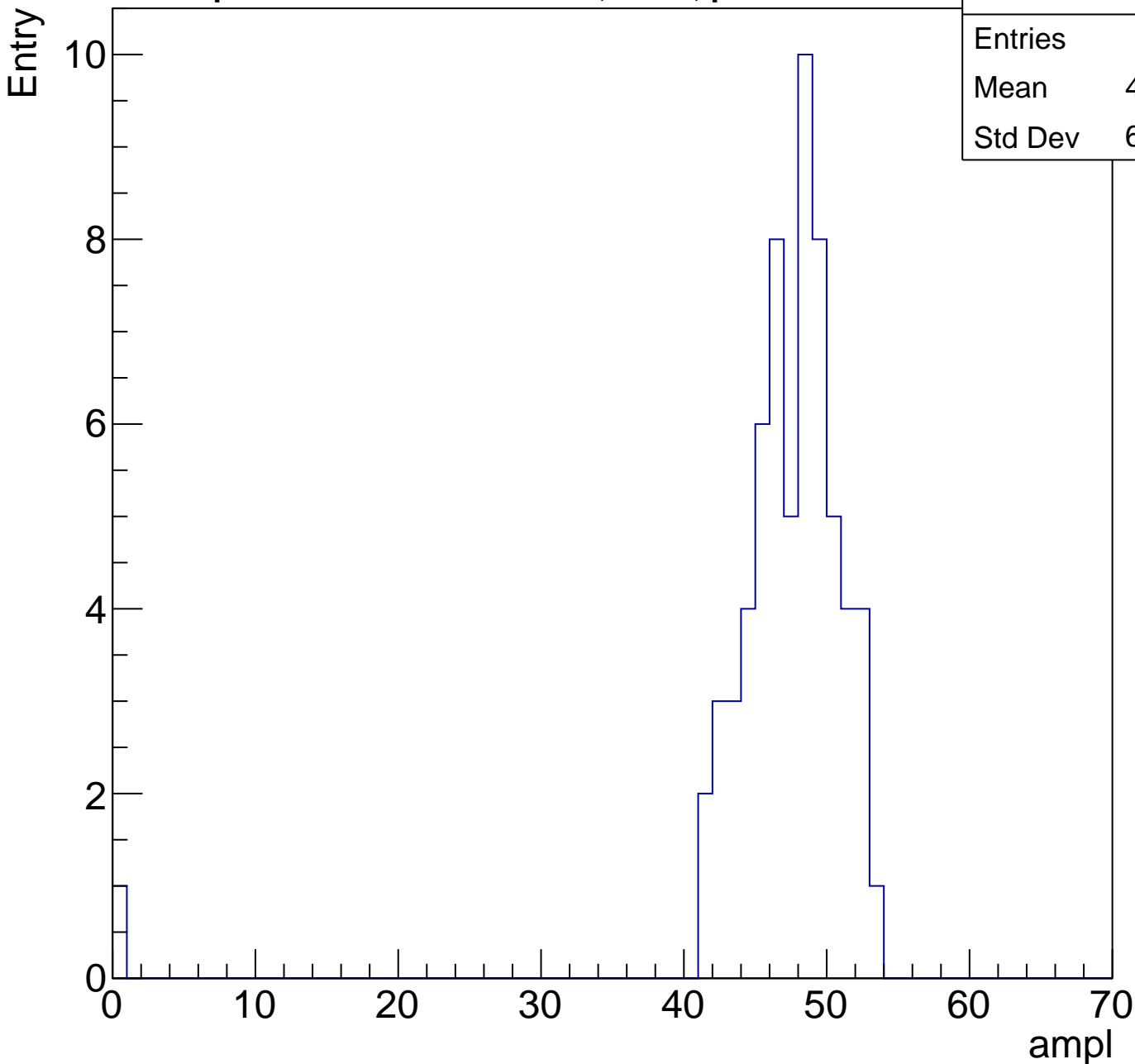
|         |       |
|---------|-------|
| Entries | 70    |
| Mean    | 35.67 |
| Std Dev | 14.16 |



# B1L103S, U4-ch59, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 64    |
| Mean    | 46.45 |
| Std Dev | 6.543 |



# B1L103S, U4-ch59, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

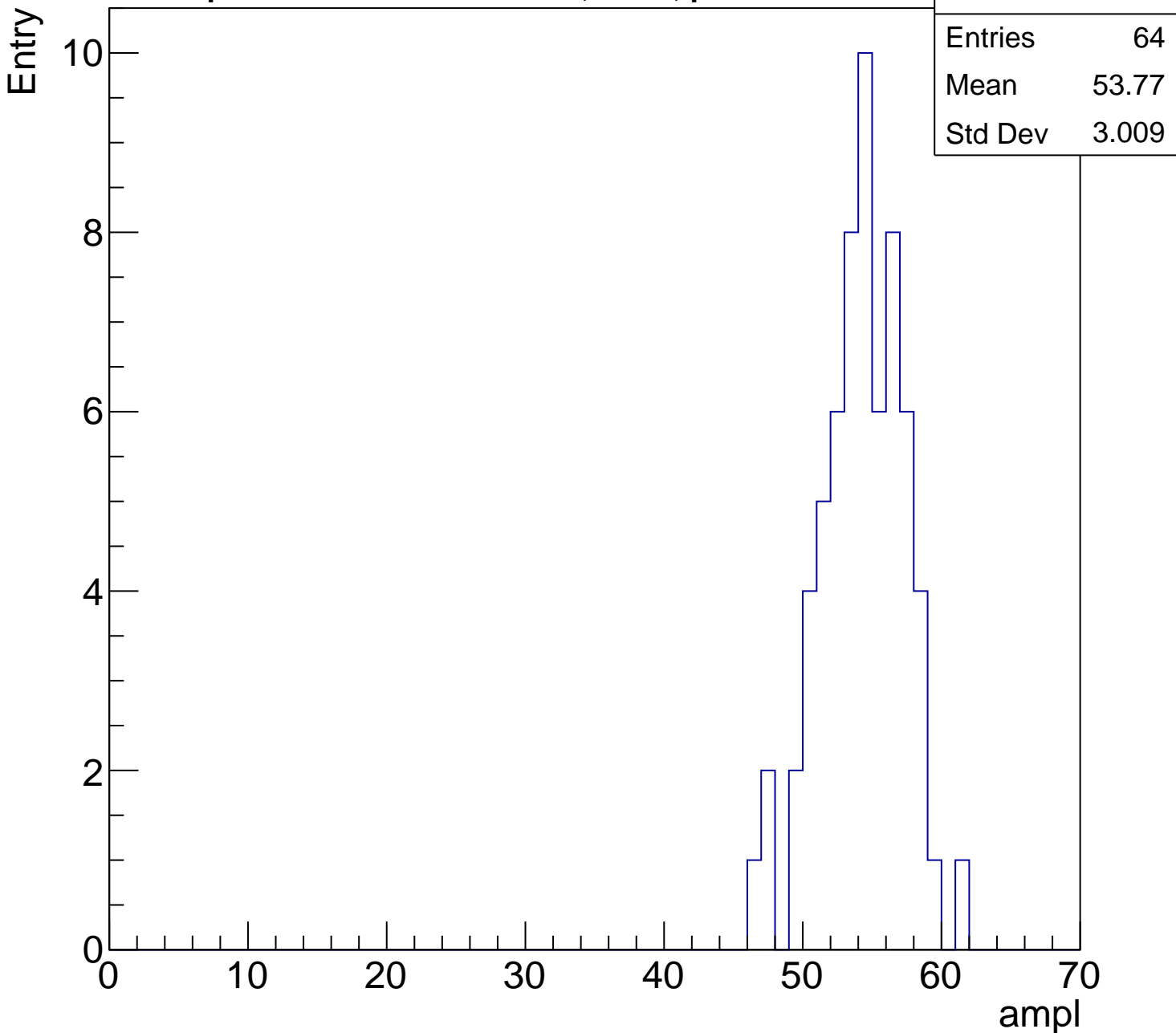
|         |       |
|---------|-------|
| Entries | 64    |
| Mean    | 53.77 |
| Std Dev | 3.009 |

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L103S, U4-ch59, adc5

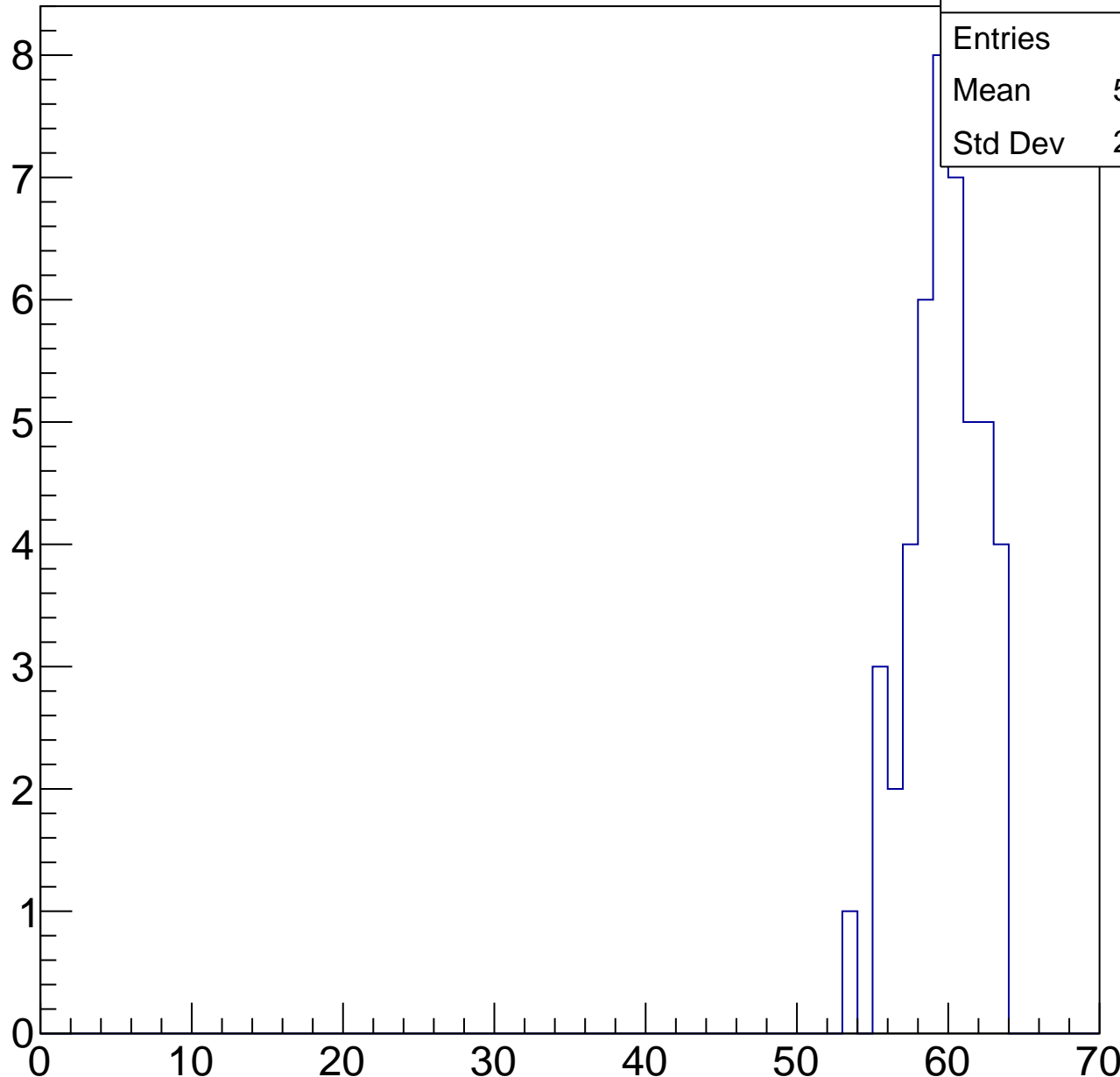
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

|         |       |
|---------|-------|
| Entries | 45    |
| Mean    | 59.22 |
| Std Dev | 2.393 |

ampl

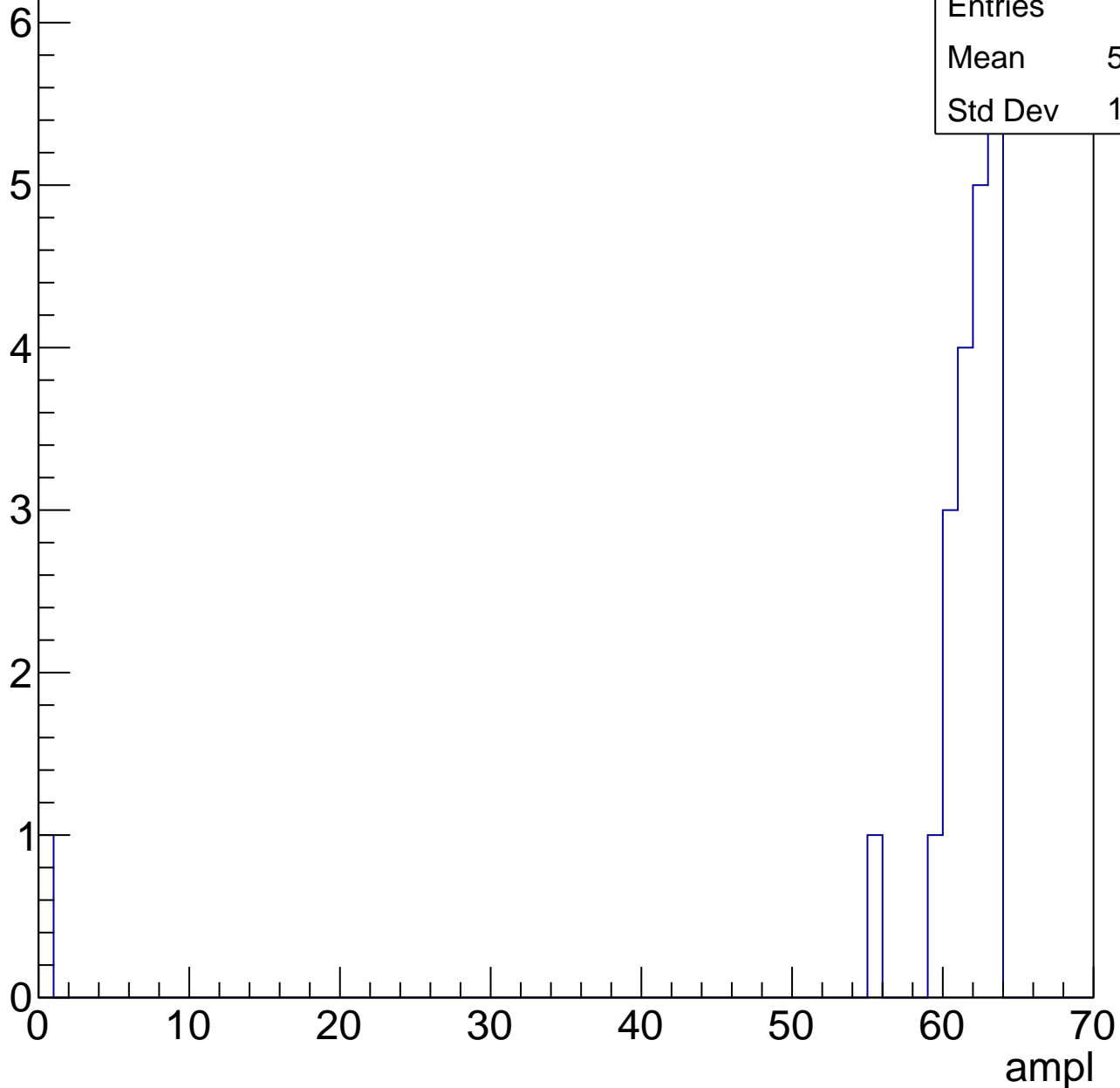


# B1L103S, U4-ch59, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 21    |
| Mean    | 58.38 |
| Std Dev | 13.18 |





# B1L103S, U4-ch59, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

|         |    |
|---------|----|
| Entries | 19 |
| Mean    | 0  |
| Std Dev | 0  |

ampl

# B1L103S, U4-ch60, adc0

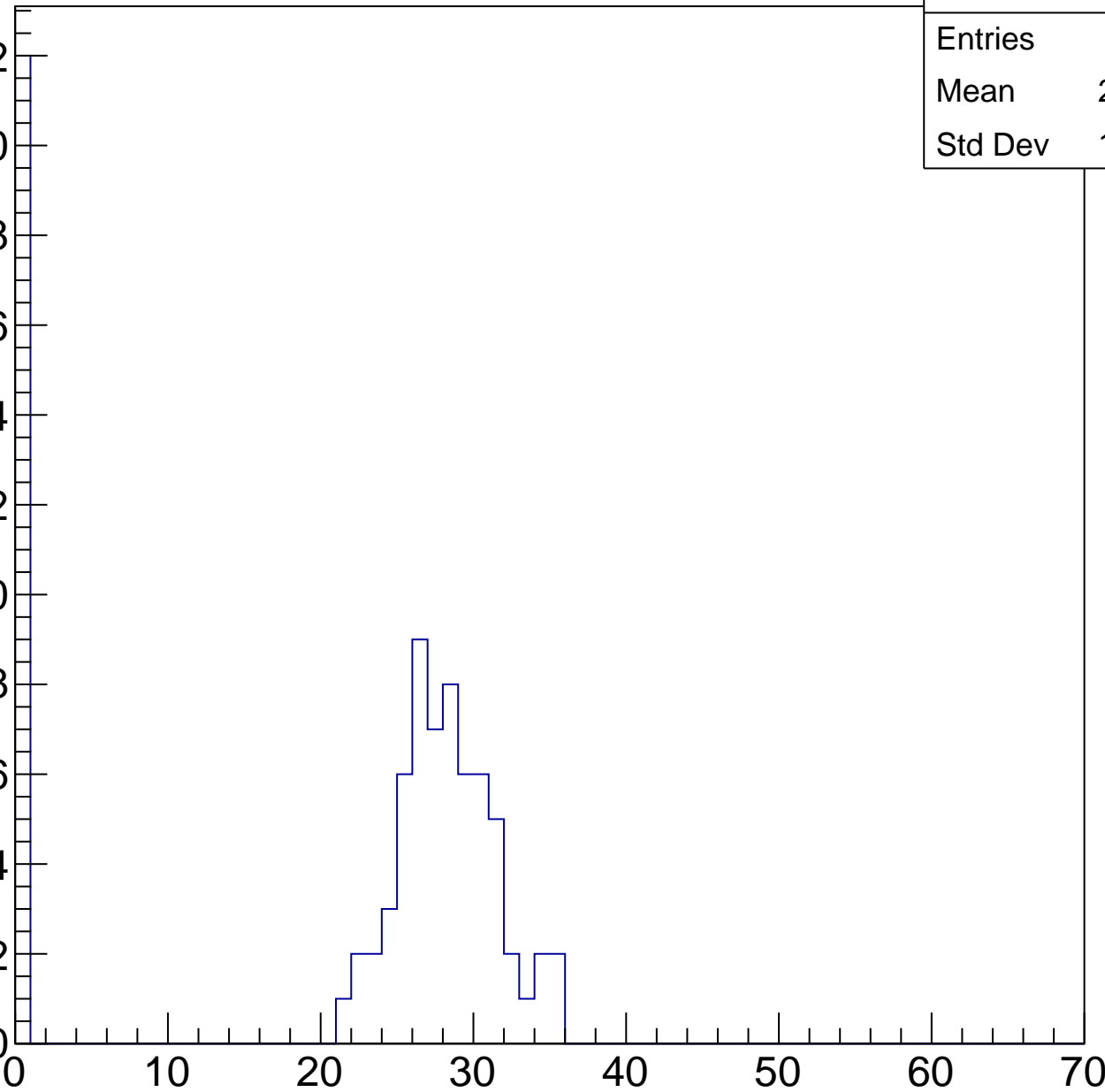
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

22  
20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

|         |       |
|---------|-------|
| Entries | 84    |
| Mean    | 20.52 |
| Std Dev | 12.52 |

ampl



# B1L103S, U4-ch60, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 81    |
| Mean    | 29.36 |
| Std Dev | 12.02 |

Entry

10

8

6

4

2

0

0

10

20

30

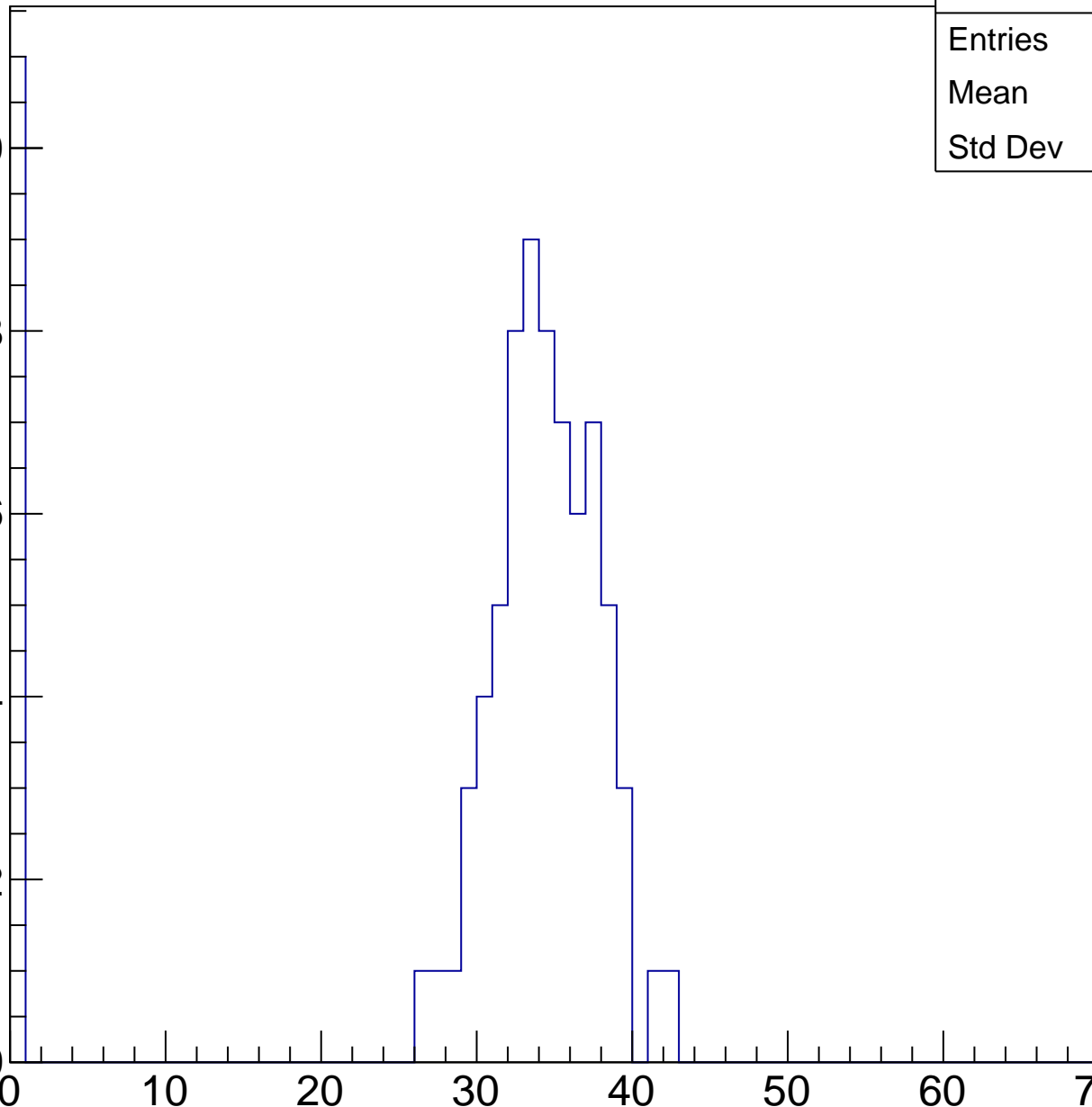
40

50

60

70

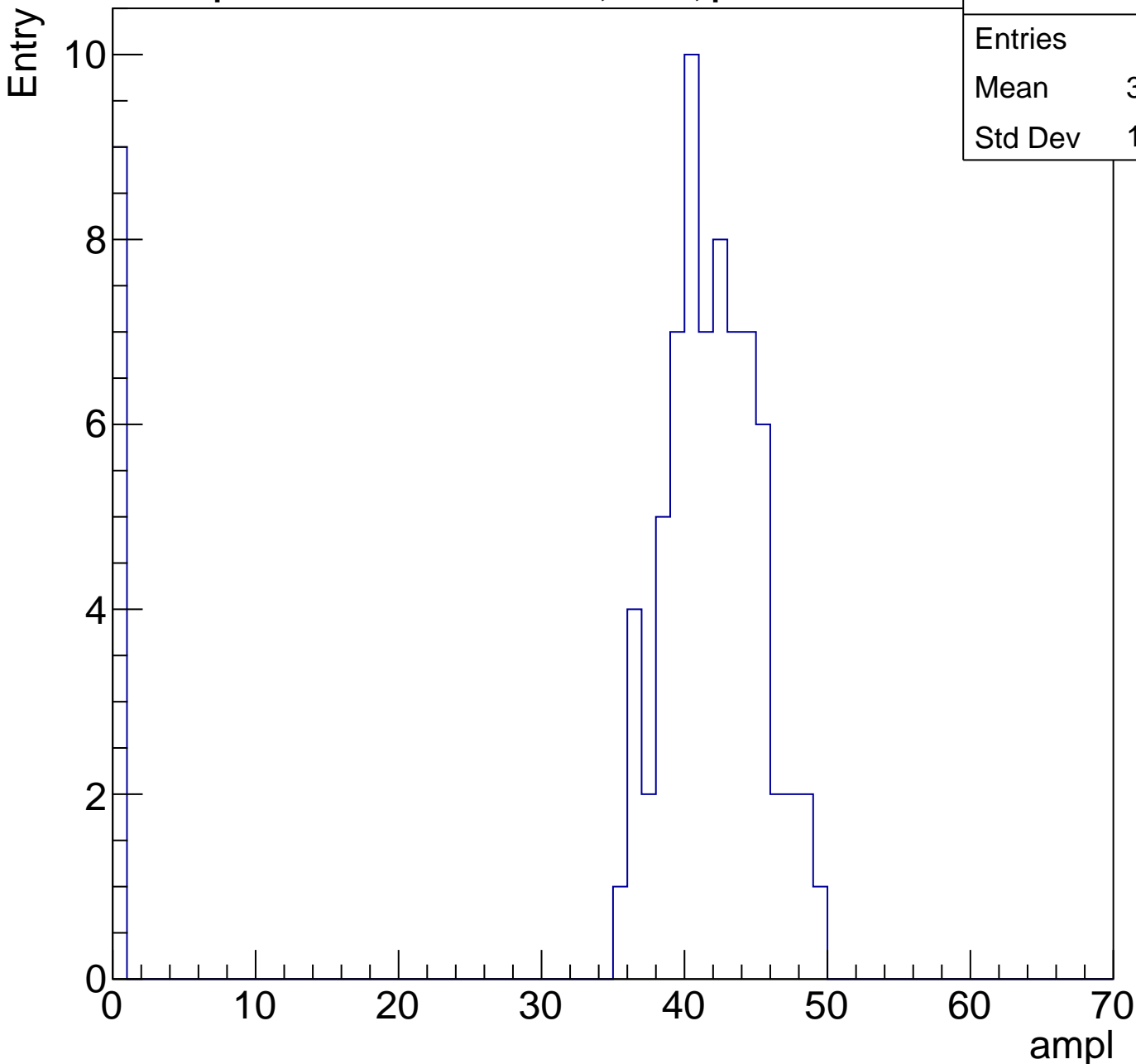
ampl



# B1L103S, U4-ch60, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 80    |
| Mean    | 36.86 |
| Std Dev | 13.46 |

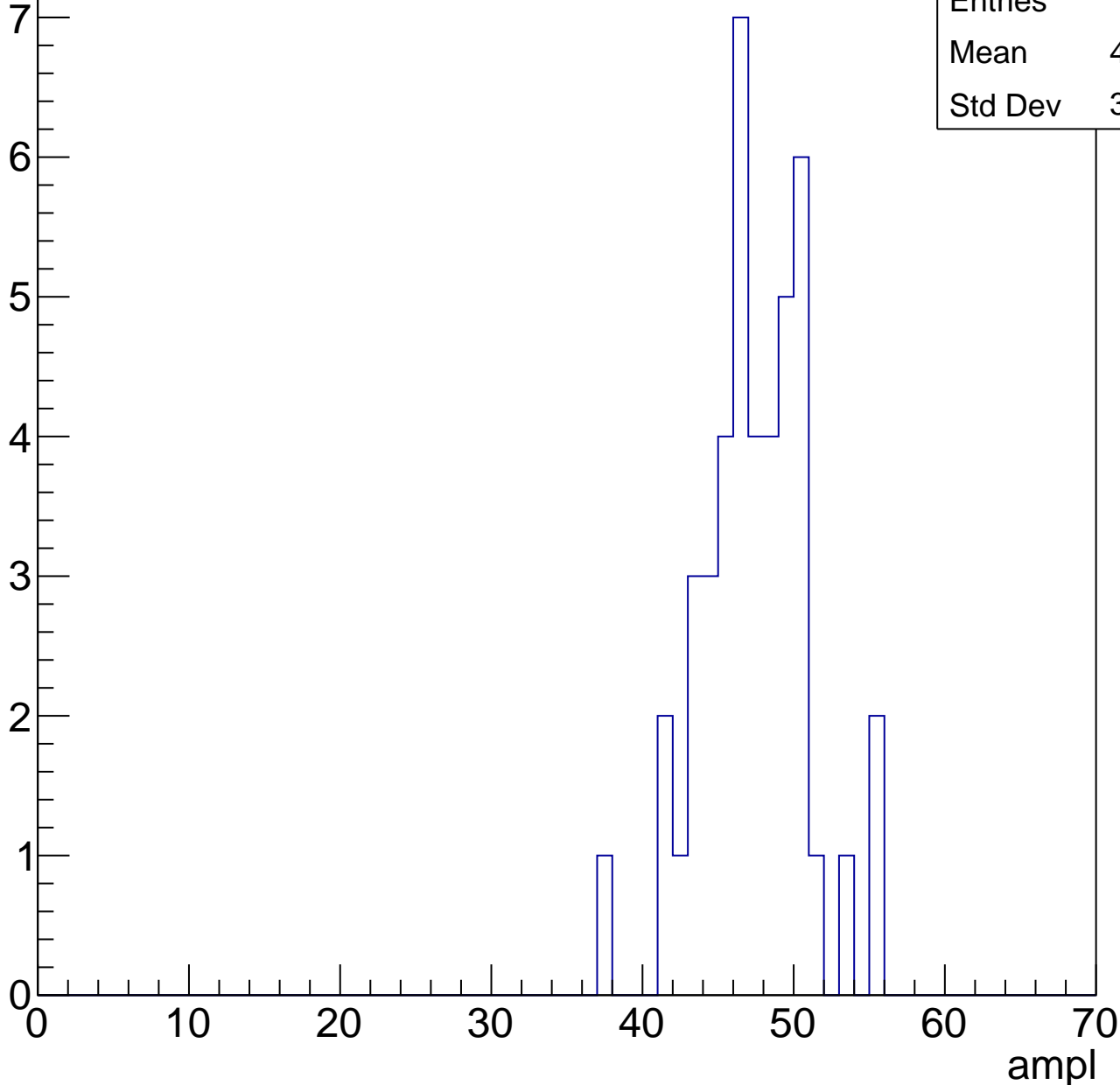


# B1L103S, U4-ch60, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 44    |
| Mean    | 46.89 |
| Std Dev | 3.543 |

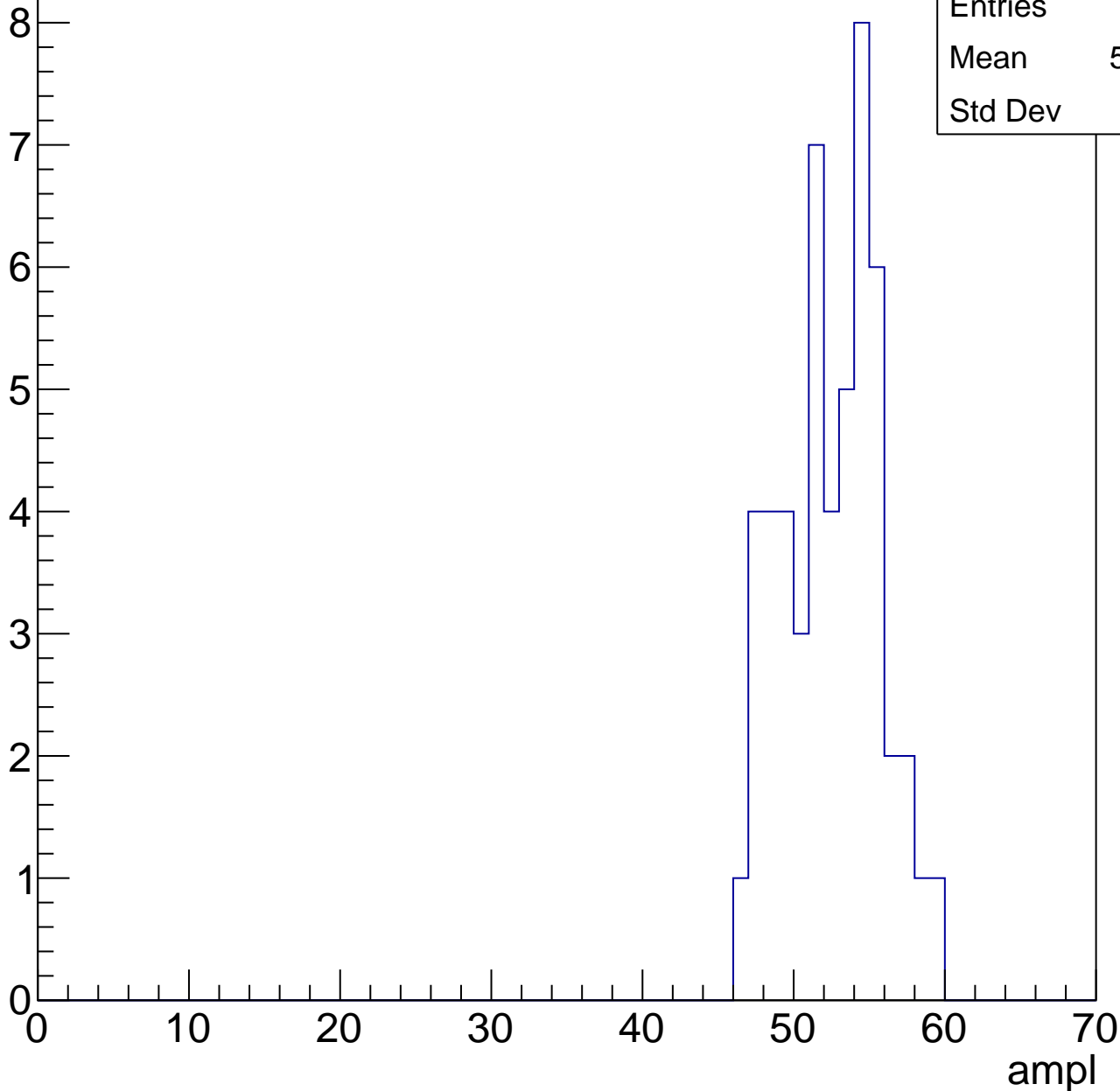


# B1L103S, U4-ch60, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 52    |
| Mean    | 52.06 |
| Std Dev | 3.14  |

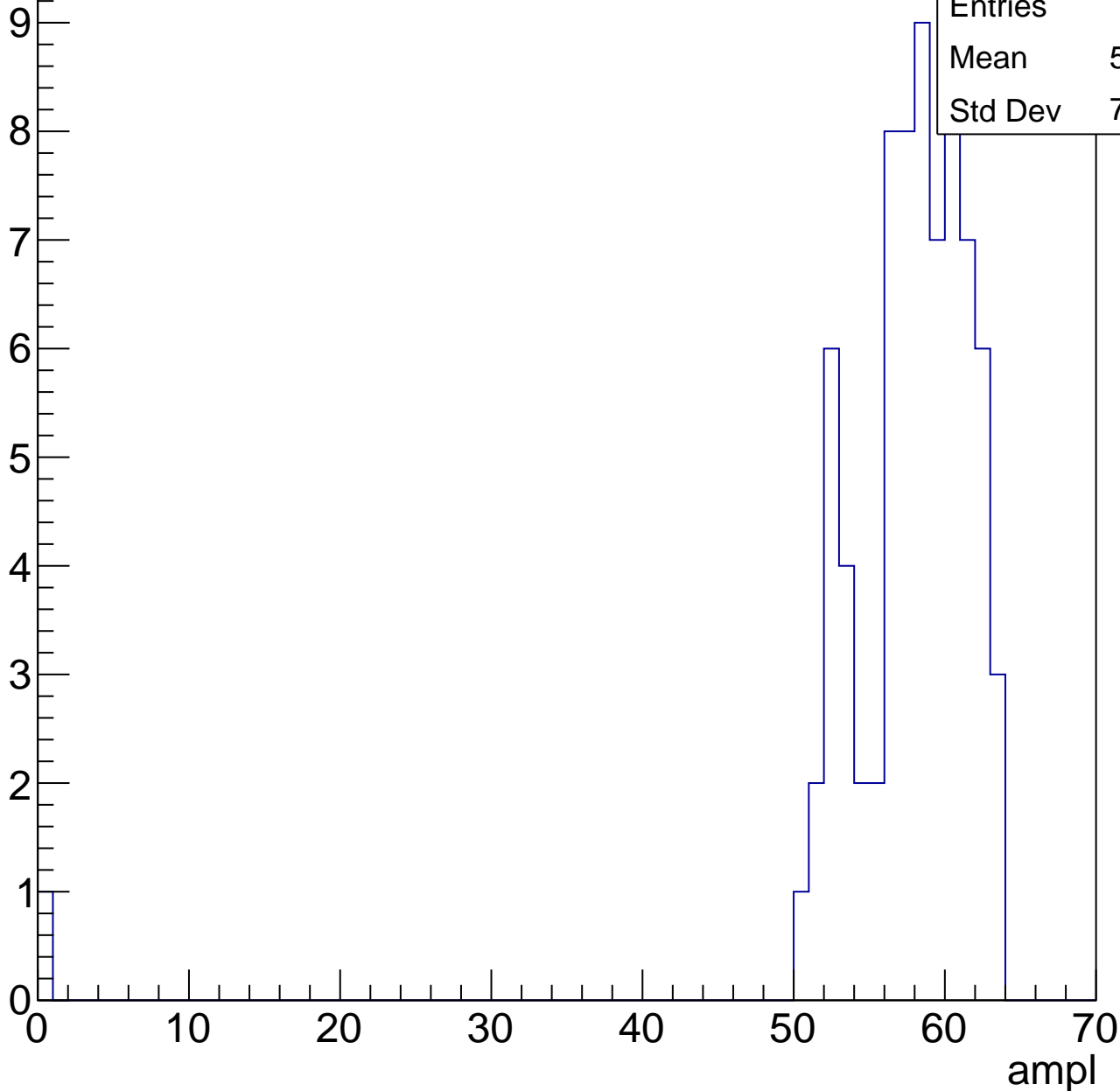


# B1L103S, U4-ch60, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 74    |
| Mean    | 56.77 |
| Std Dev | 7.437 |

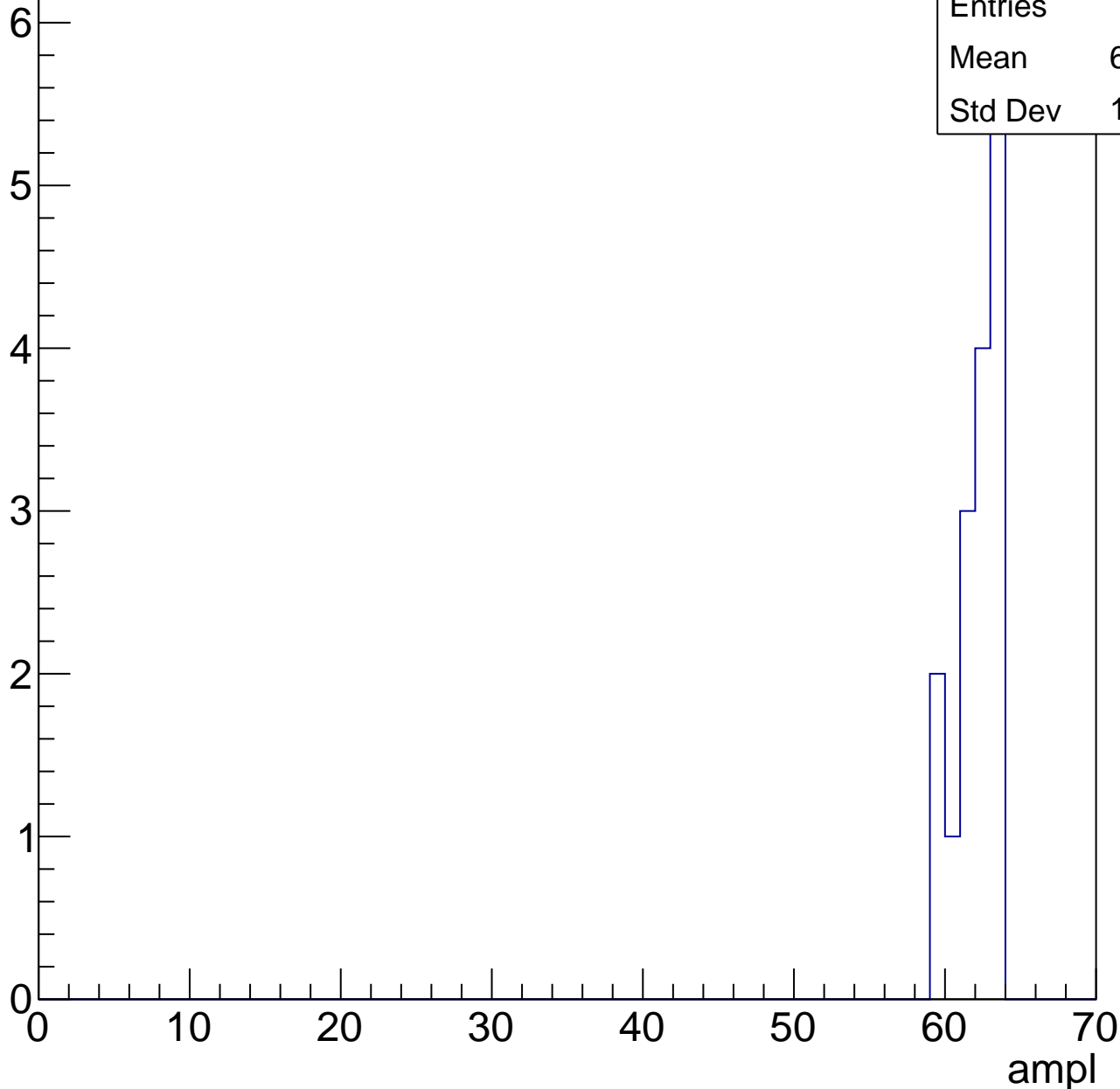


# B1L103S, U4-ch60, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 16    |
| Mean    | 61.69 |
| Std Dev | 1.356 |





# B1L103S, U4-ch60, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

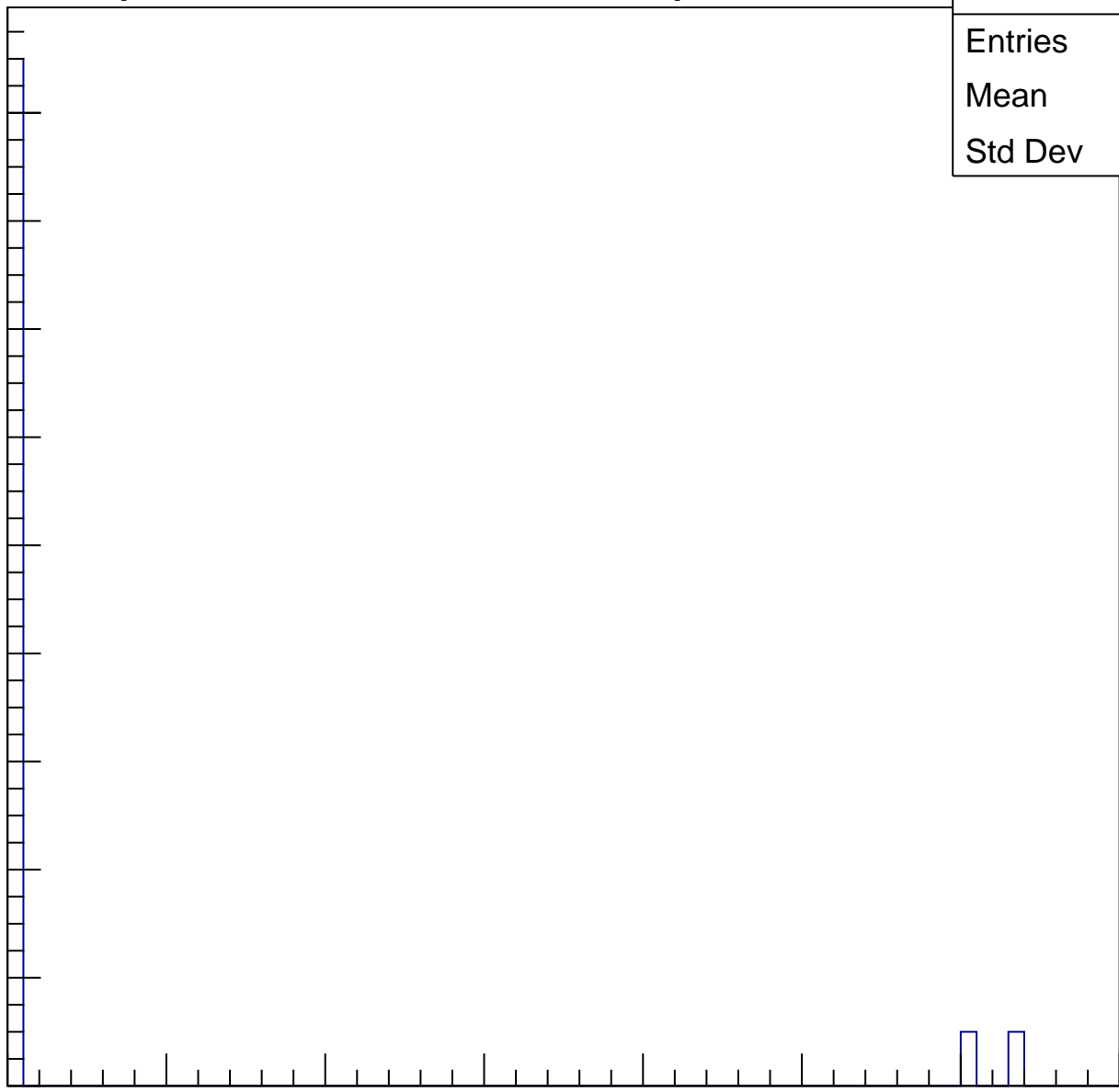
Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

|         |       |
|---------|-------|
| Entries | 21    |
| Mean    | 5.857 |
| Std Dev | 18.06 |

0 10 20 30 40 50 60 70

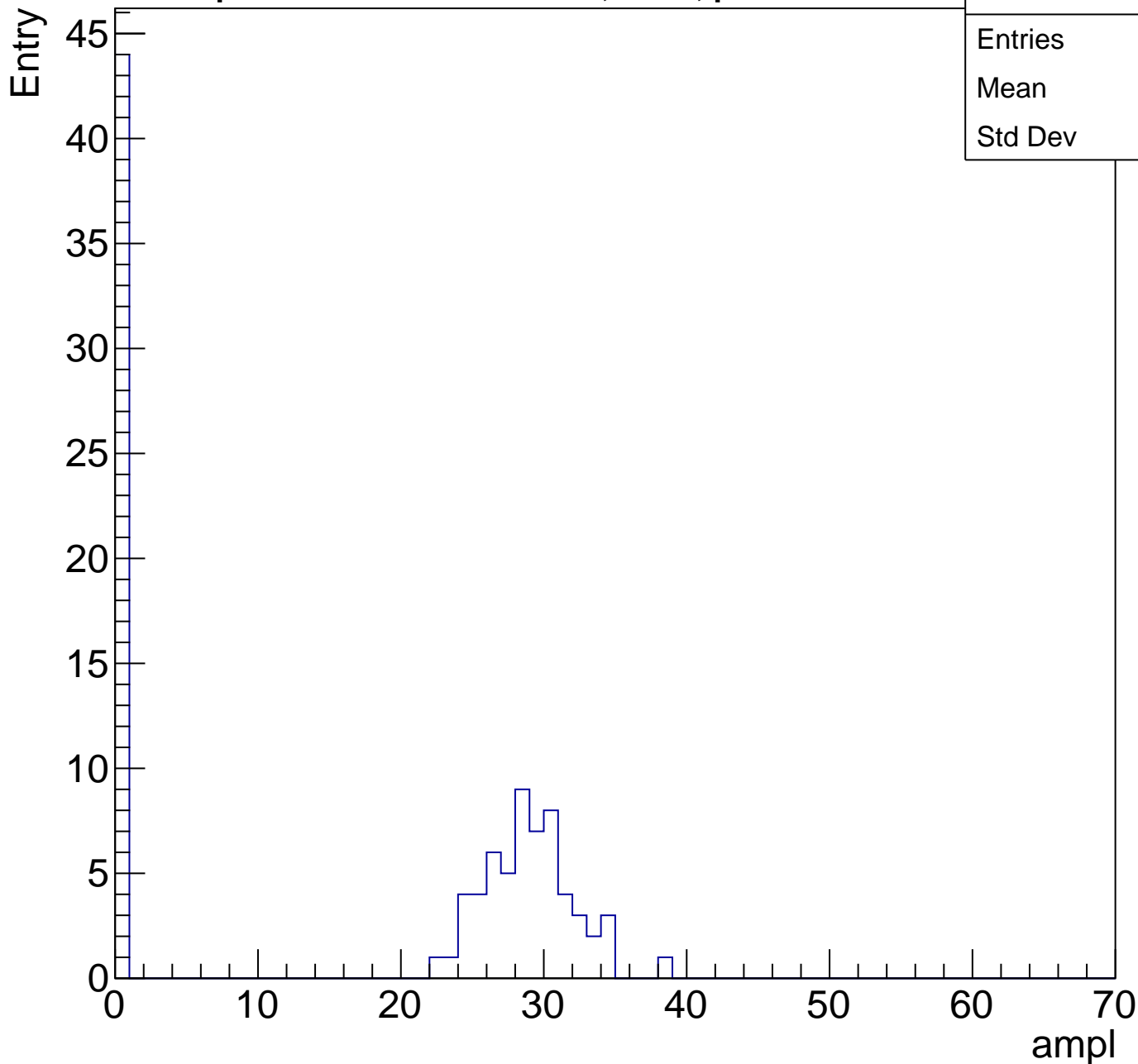
ampl



# B1L103S, U4-ch61, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 102   |
| Mean    | 16.21 |
| Std Dev | 14.31 |

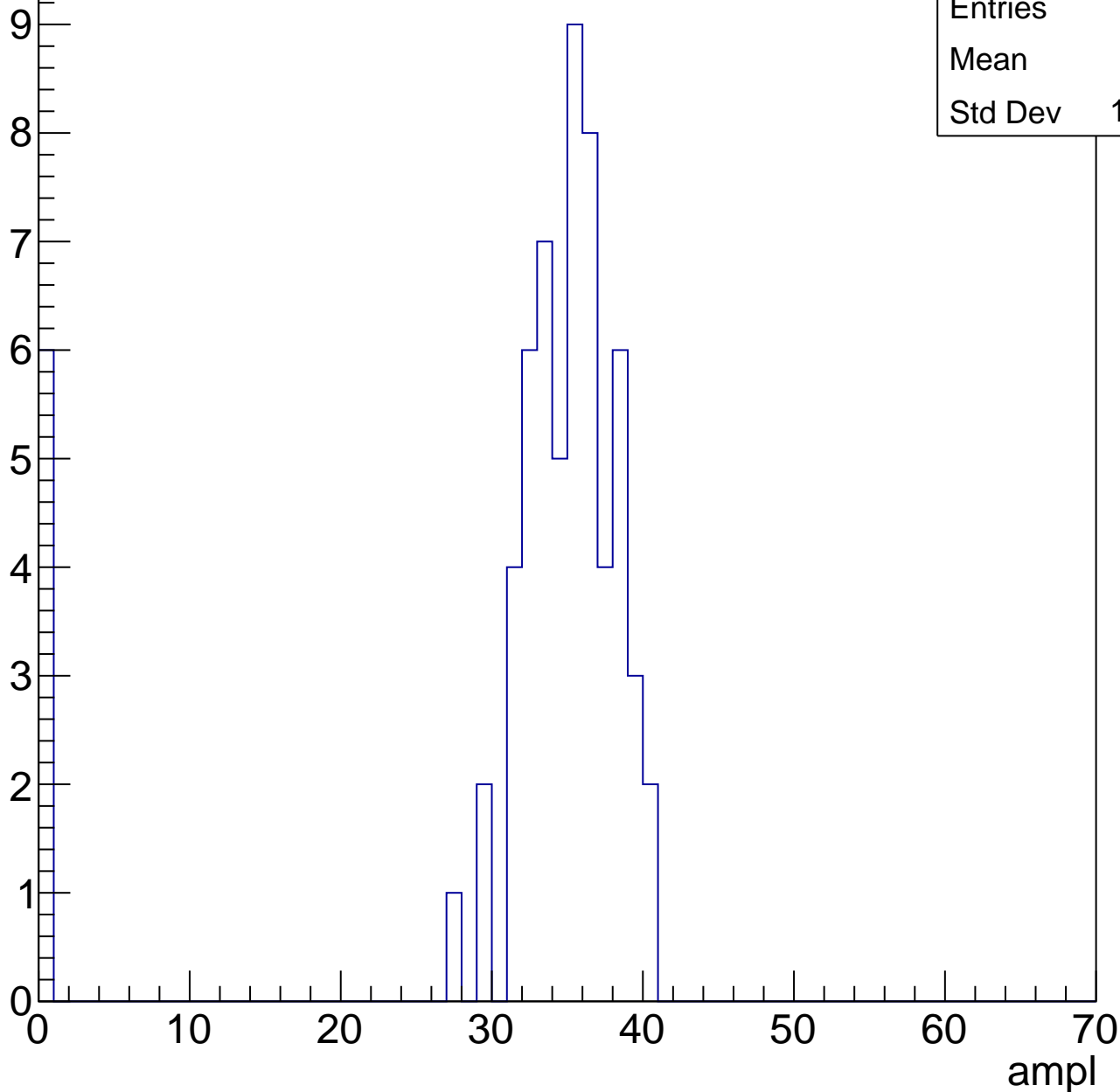


# B1L103S, U4-ch61, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 63    |
| Mean    | 31.4  |
| Std Dev | 10.54 |



# B1L103S, U4-ch61, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 91    |
| Mean    | 34.43 |
| Std Dev | 15.73 |

Entry

14  
12  
10  
8  
6  
4  
2  
0

0

10

20

30

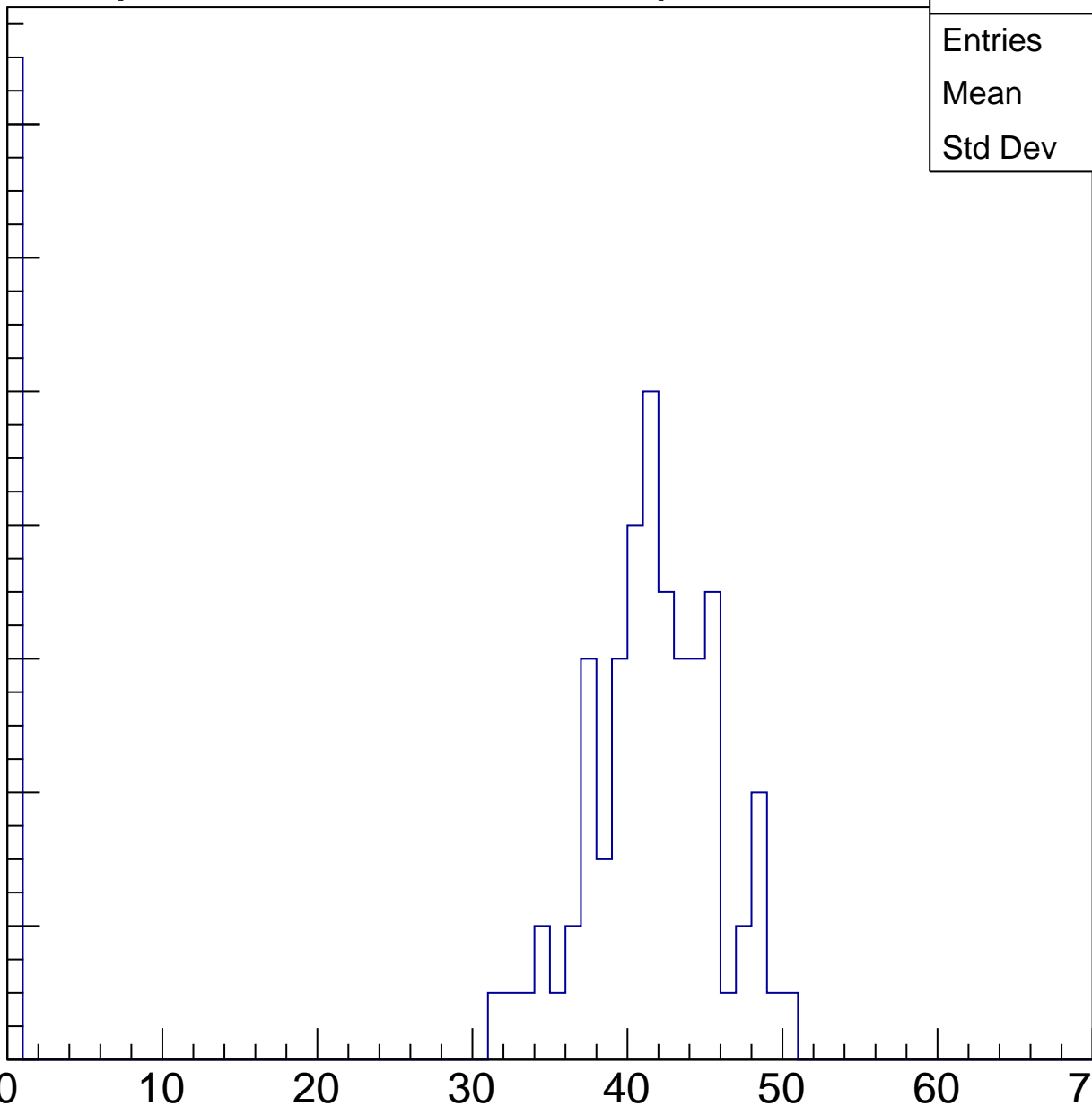
40

50

60

70

ampl

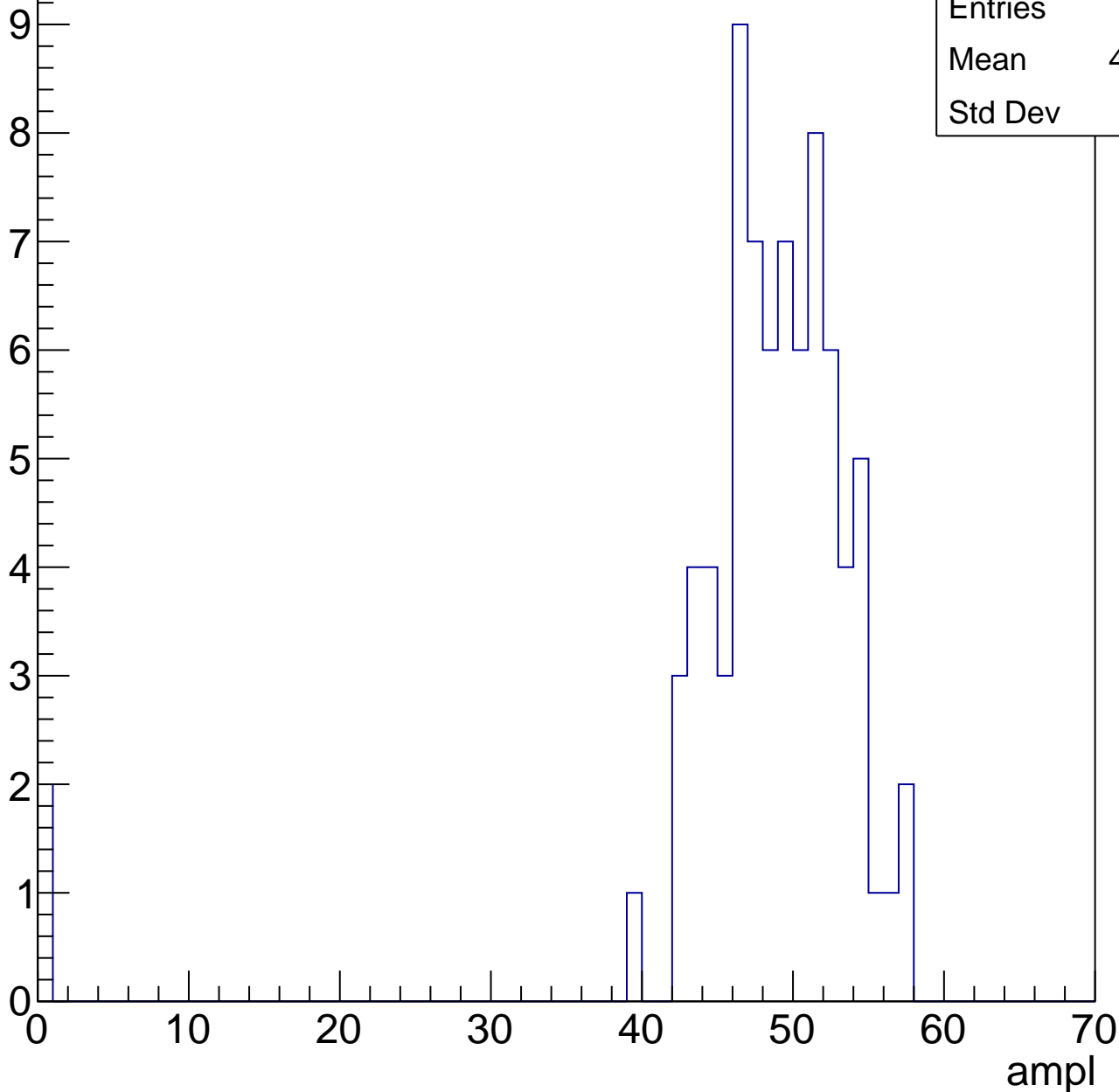


# B1L103S, U4-ch61, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 79    |
| Mean    | 47.46 |
| Std Dev | 8.54  |

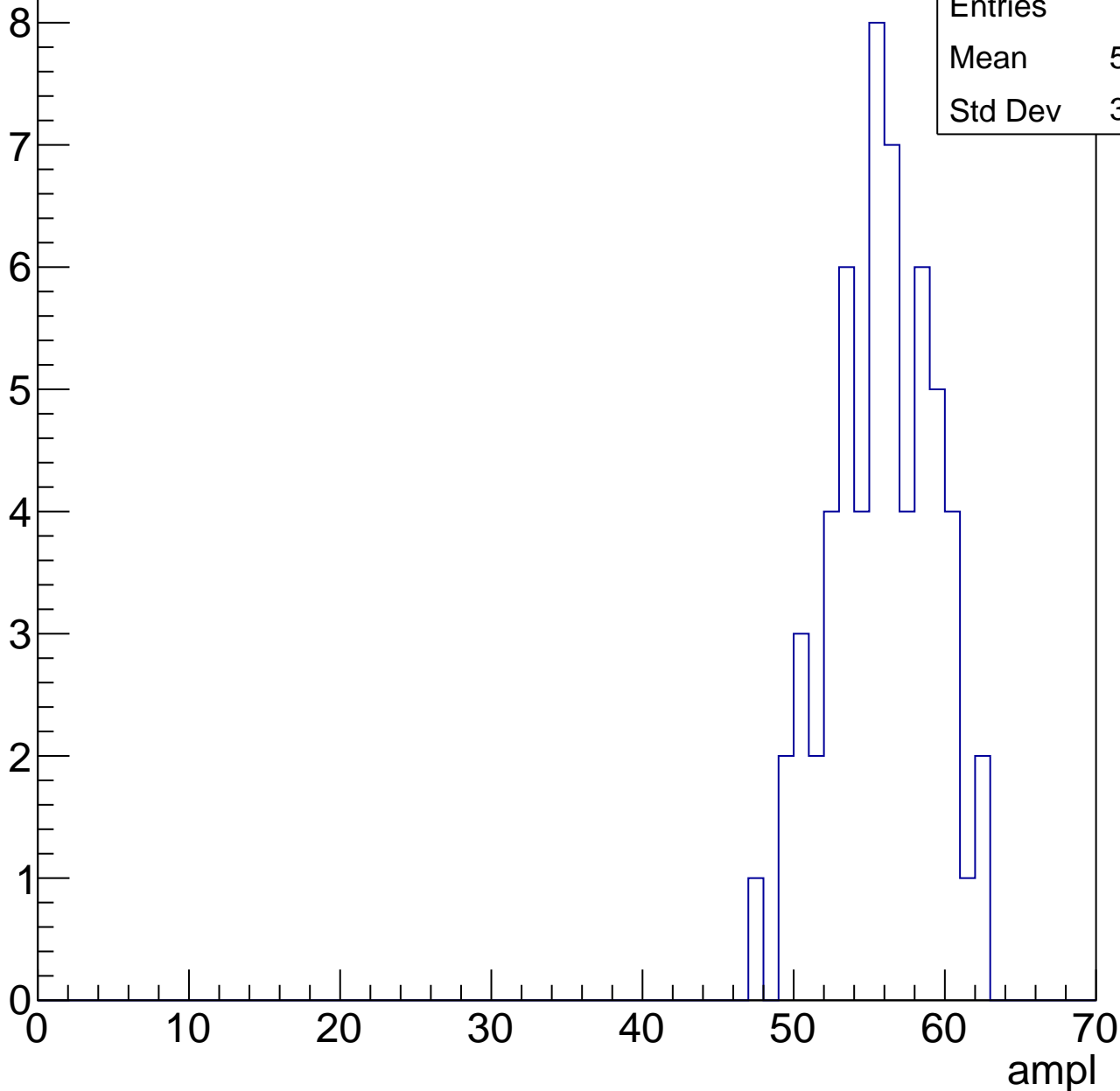


# B1L103S, U4-ch61, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 59    |
| Mean    | 55.37 |
| Std Dev | 3.419 |



# B1L103S, U4-ch61, adc5

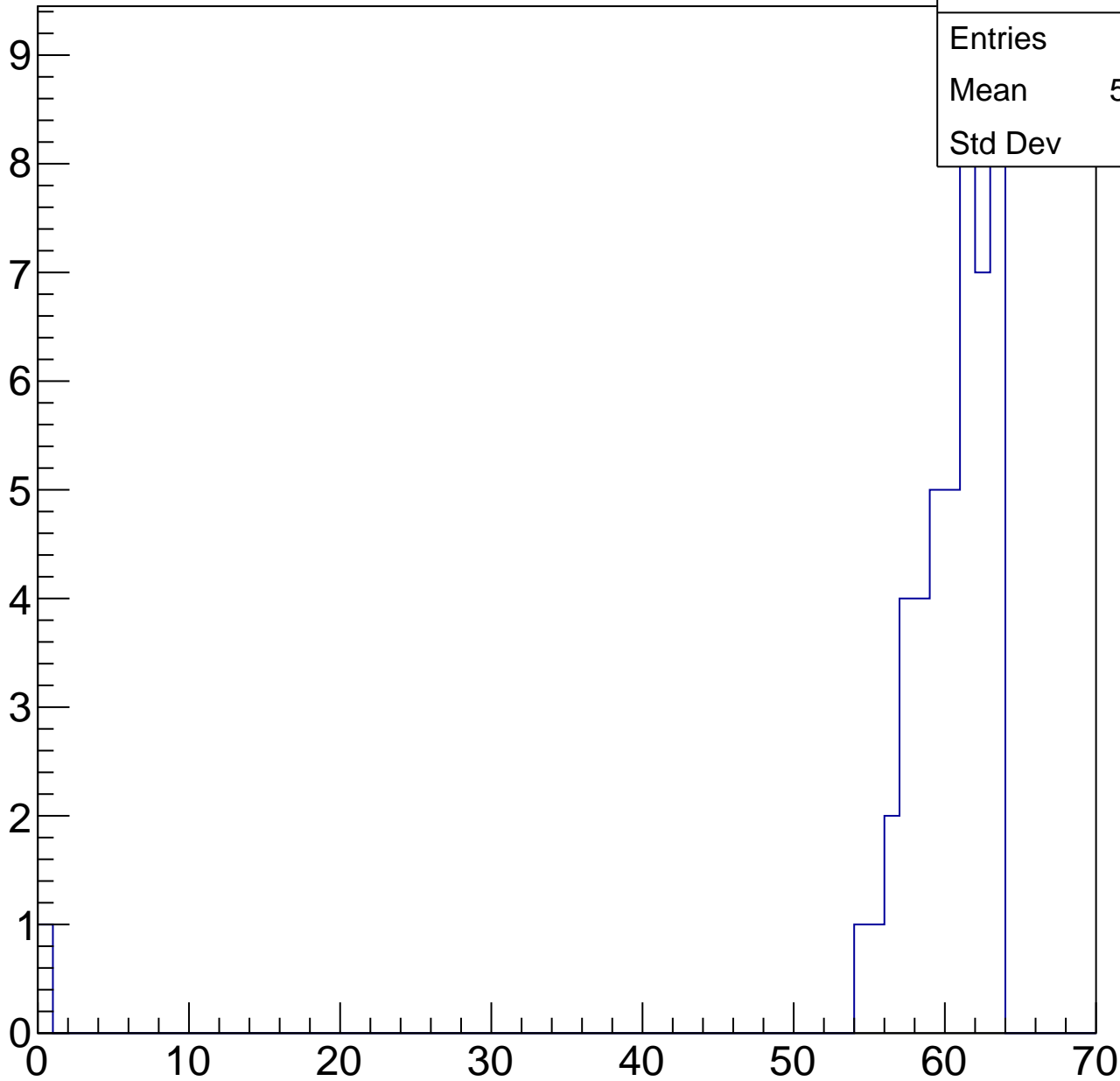
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

|         |       |
|---------|-------|
| Entries | 47    |
| Mean    | 58.79 |
| Std Dev | 8.98  |

ampl



# B1L103S, U4-ch61, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U4-ch61, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

|         |    |
|---------|----|
| Entries | 19 |
| Mean    | 0  |
| Std Dev | 0  |

ampl

# B1L103S, U4-ch62, adc0

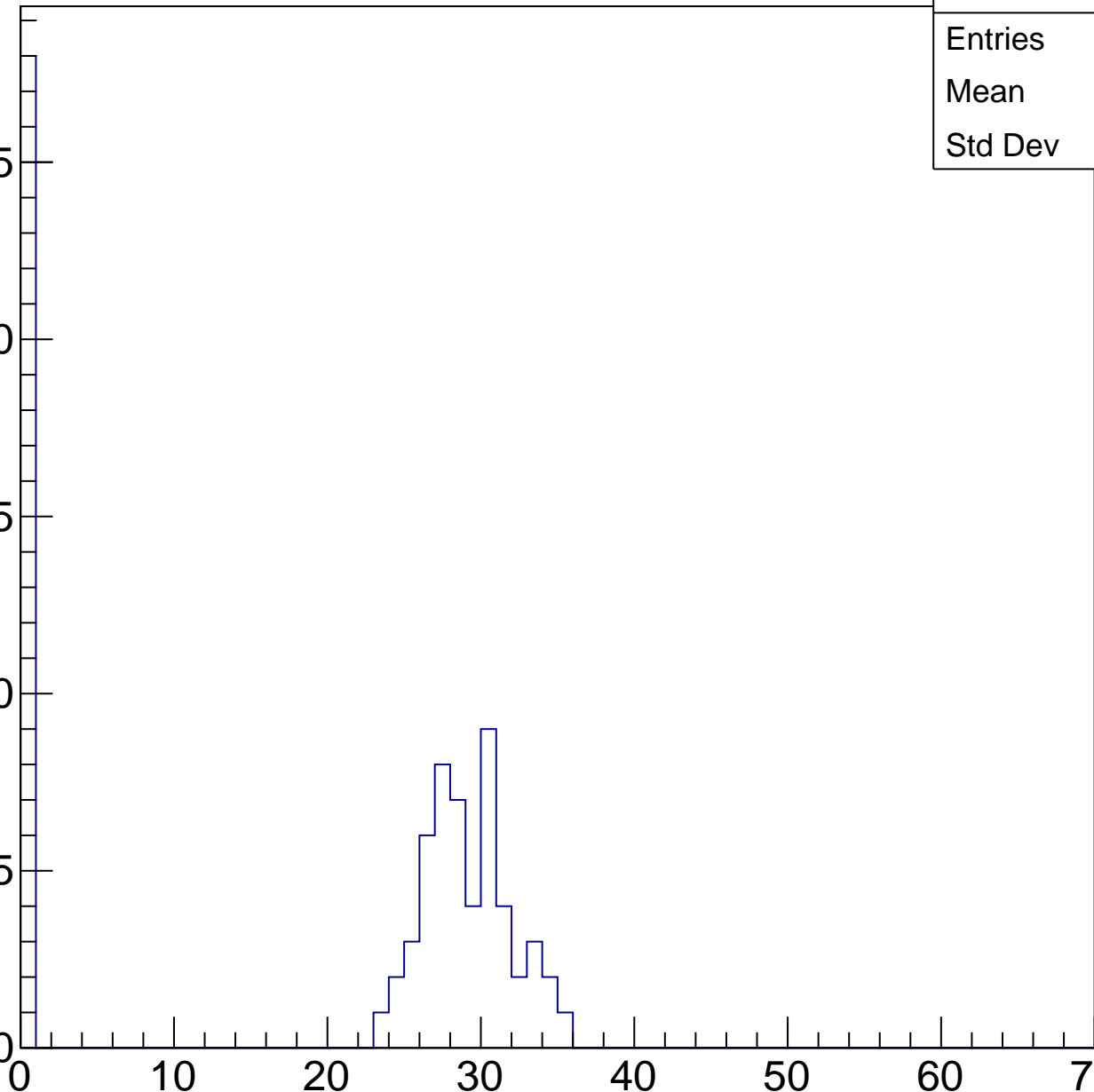
calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 80    |
| Mean    | 18.62 |
| Std Dev | 13.85 |

Entry

25  
20  
15  
10  
5  
0

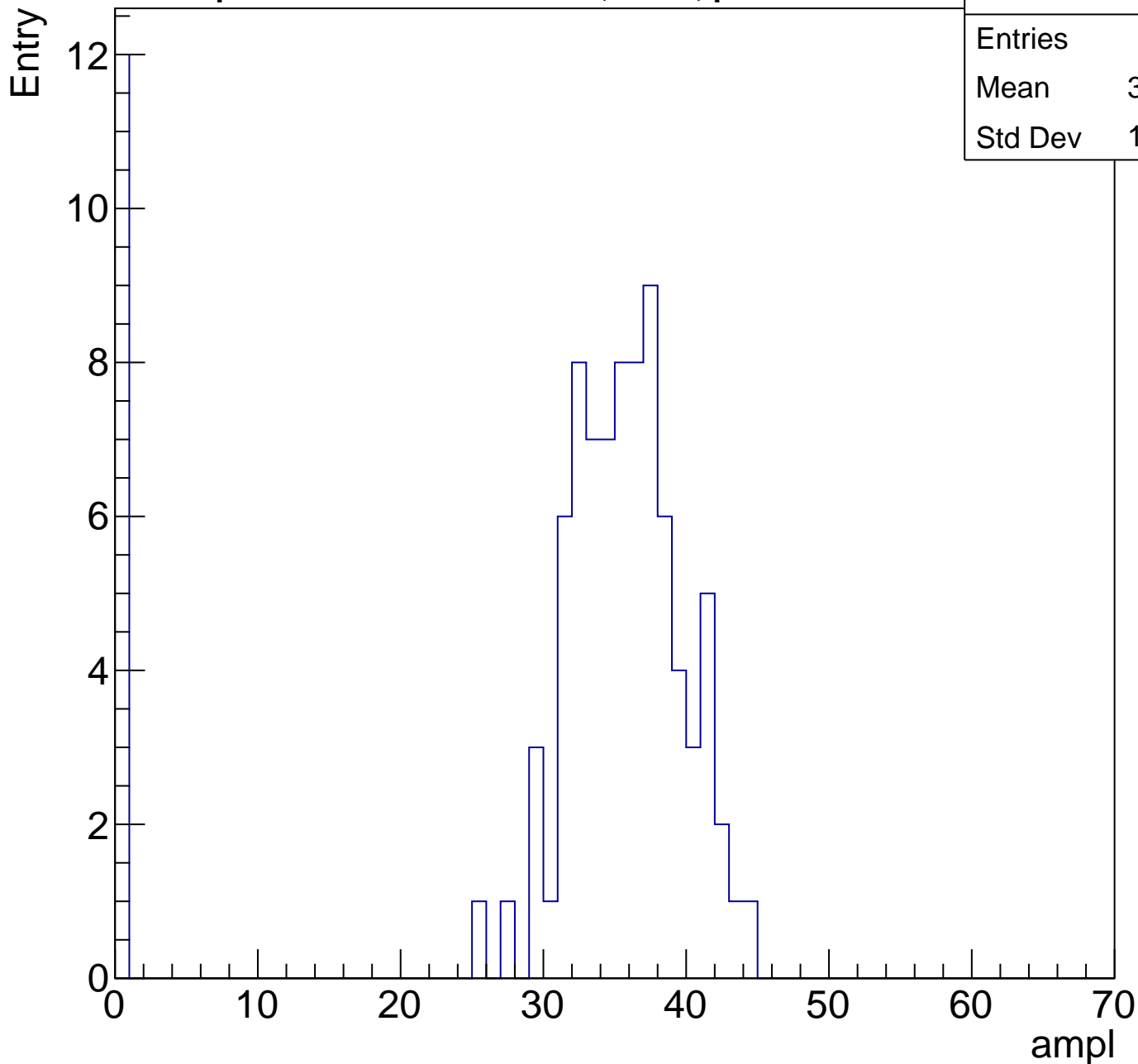
ampl



# B1L103S, U4-ch62, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 93    |
| Mean    | 30.76 |
| Std Dev | 12.35 |

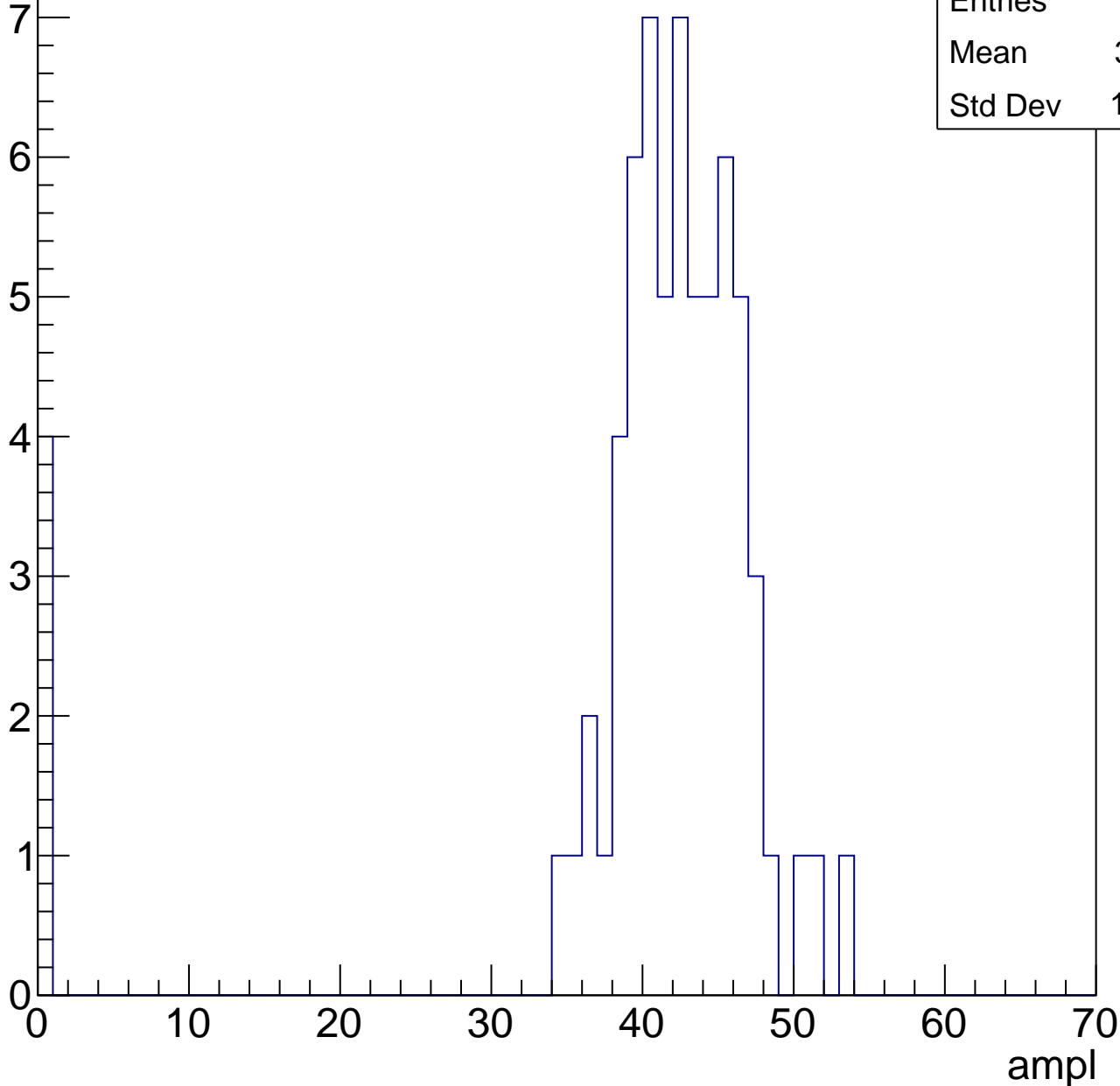


# B1L103S, U4-ch62, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 66    |
| Mean    | 39.71 |
| Std Dev | 10.74 |

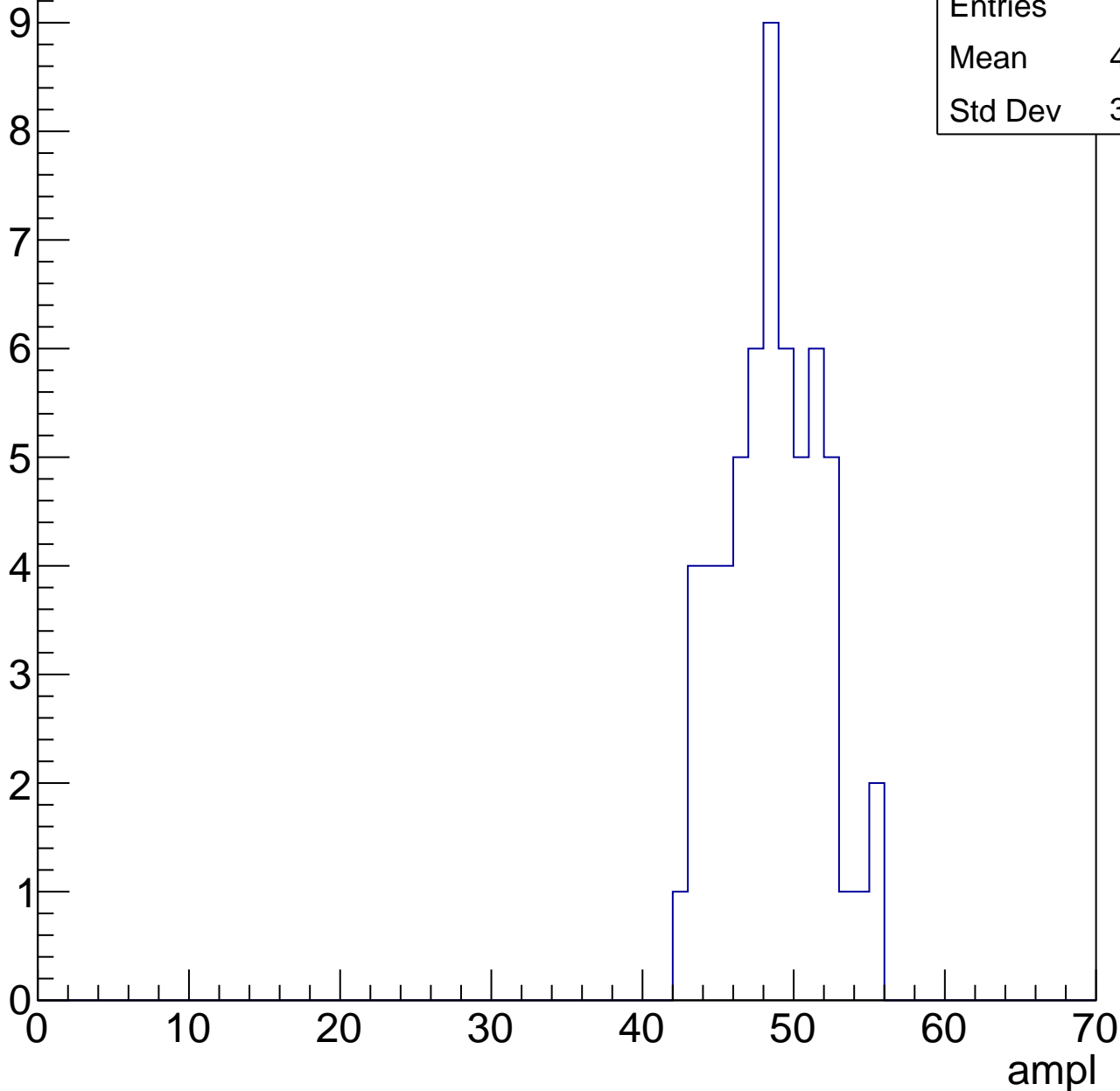


# B1L103S, U4-ch62, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 59    |
| Mean    | 48.15 |
| Std Dev | 3.134 |

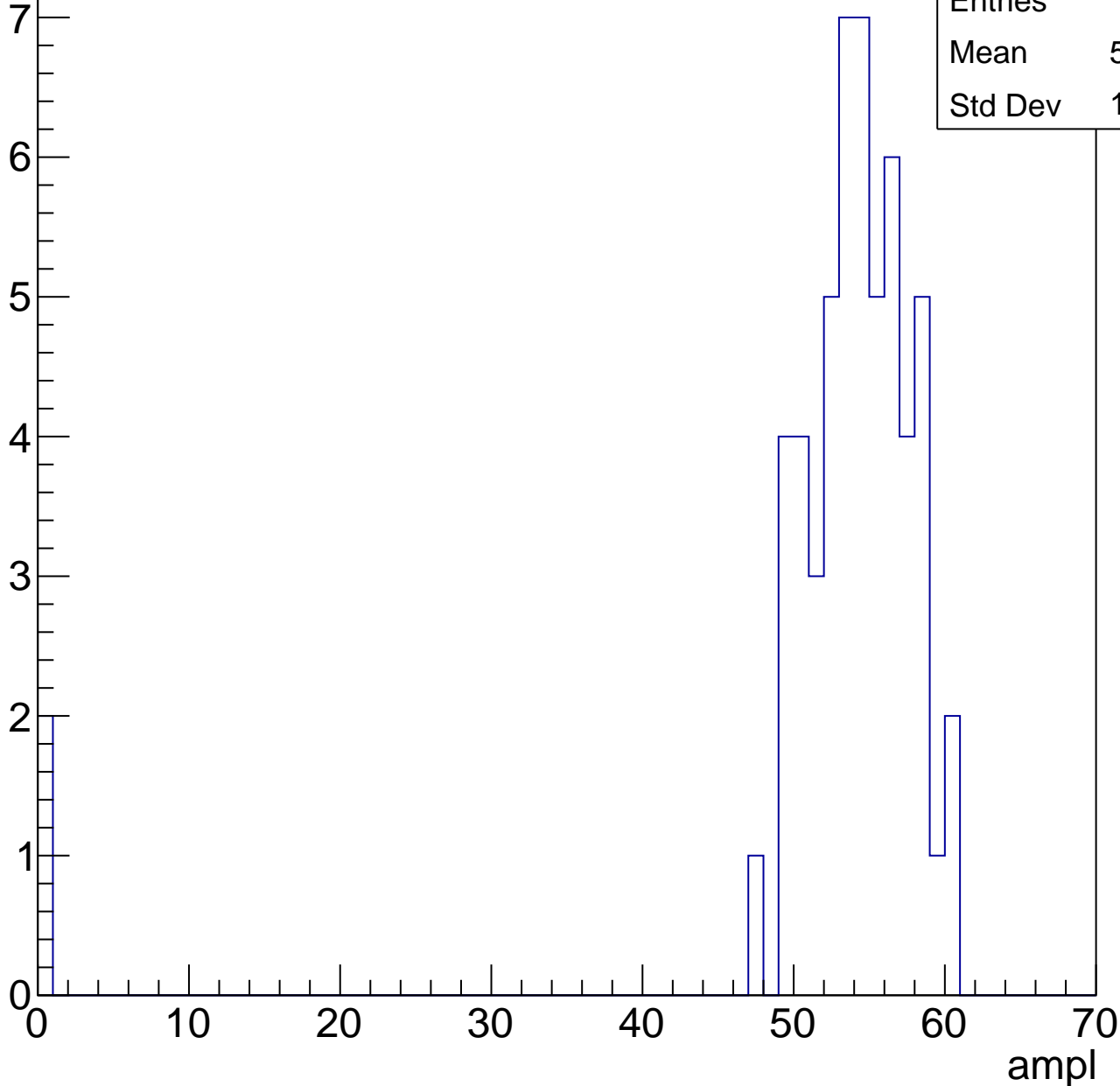


# B1L103S, U4-ch62, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

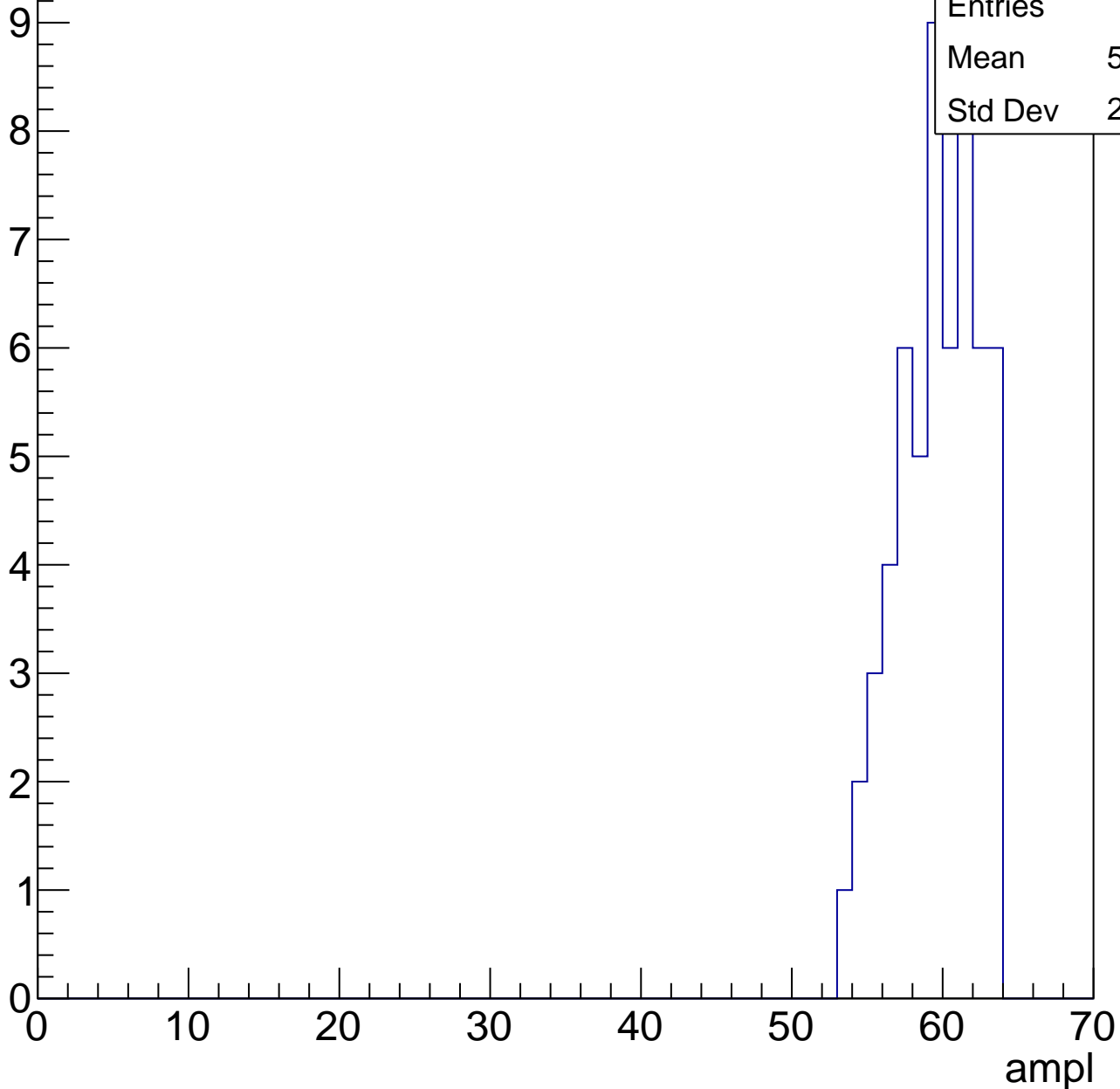
|         |       |
|---------|-------|
| Entries | 56    |
| Mean    | 52.02 |
| Std Dev | 10.45 |



# B1L103S, U4-ch62, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

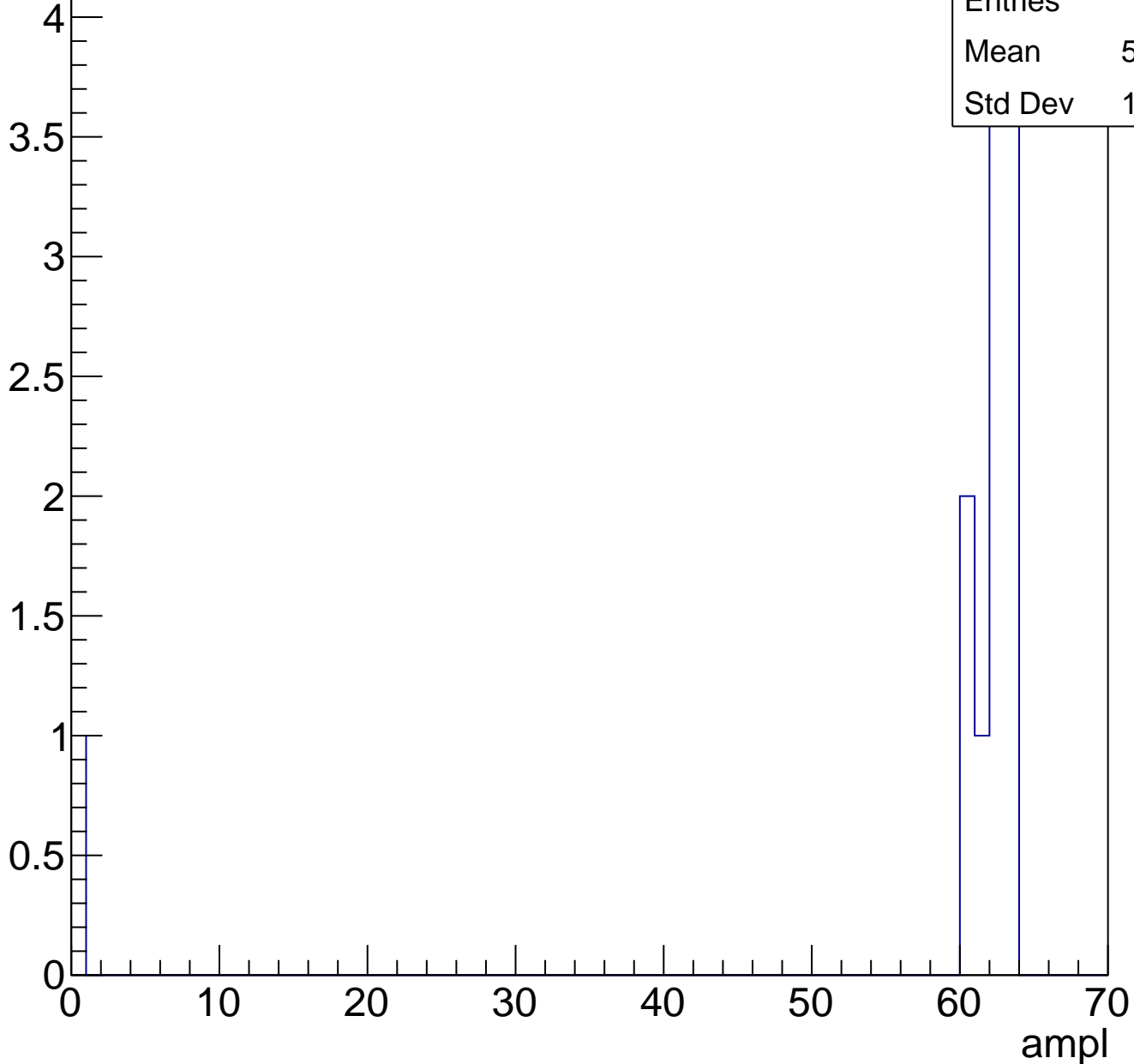
Entry



# B1L103S, U4-ch62, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U4-ch62, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

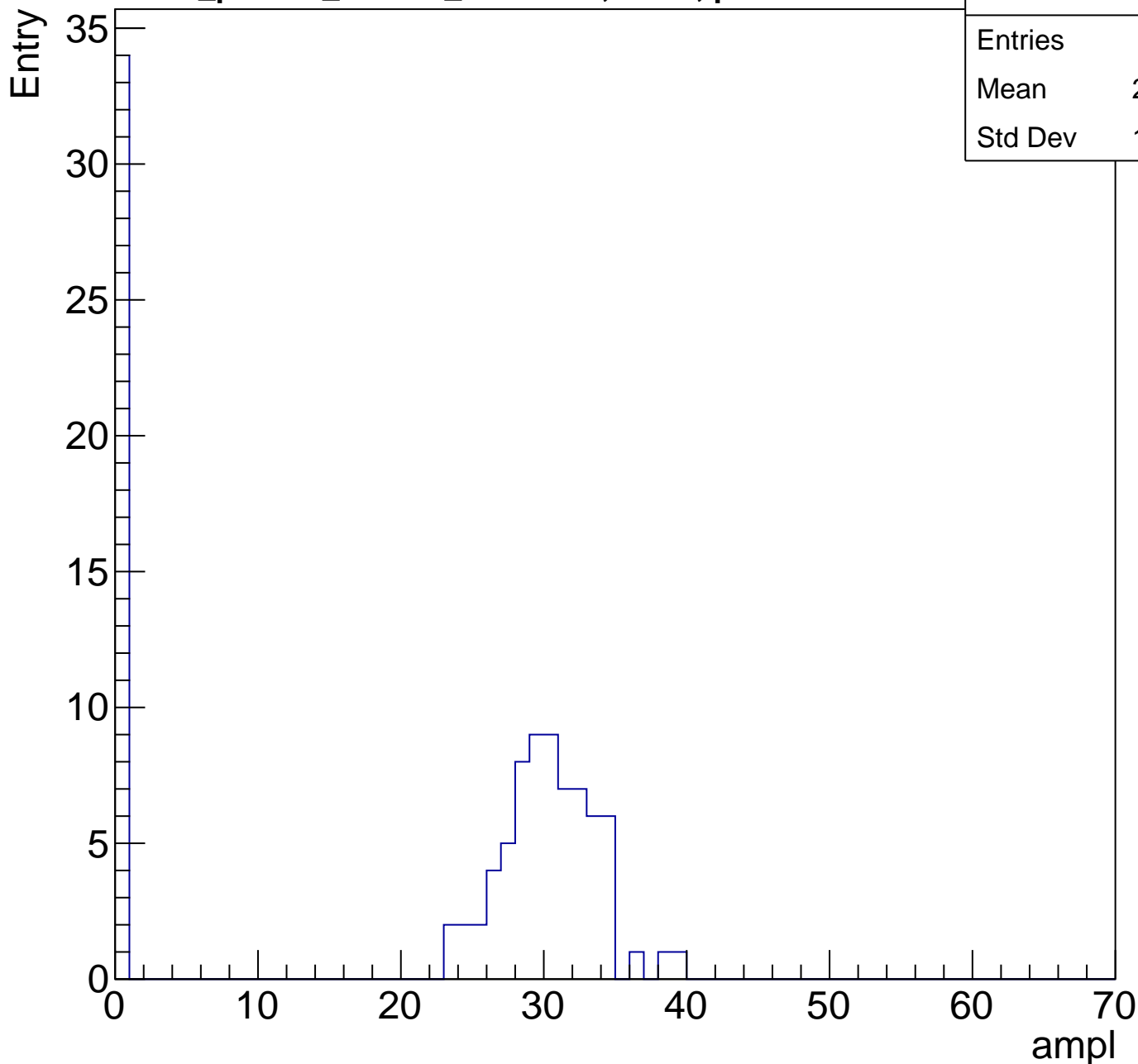
Entry



# B1L103S, U4-ch63, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 104   |
| Mean    | 20.13 |
| Std Dev | 14.28 |



# B1L103S, U4-ch63, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |      |
|---------|------|
| Entries | 70   |
| Mean    | 33.6 |
| Std Dev | 9.75 |

Entry

10

8

6

4

2

0

0

10

20

30

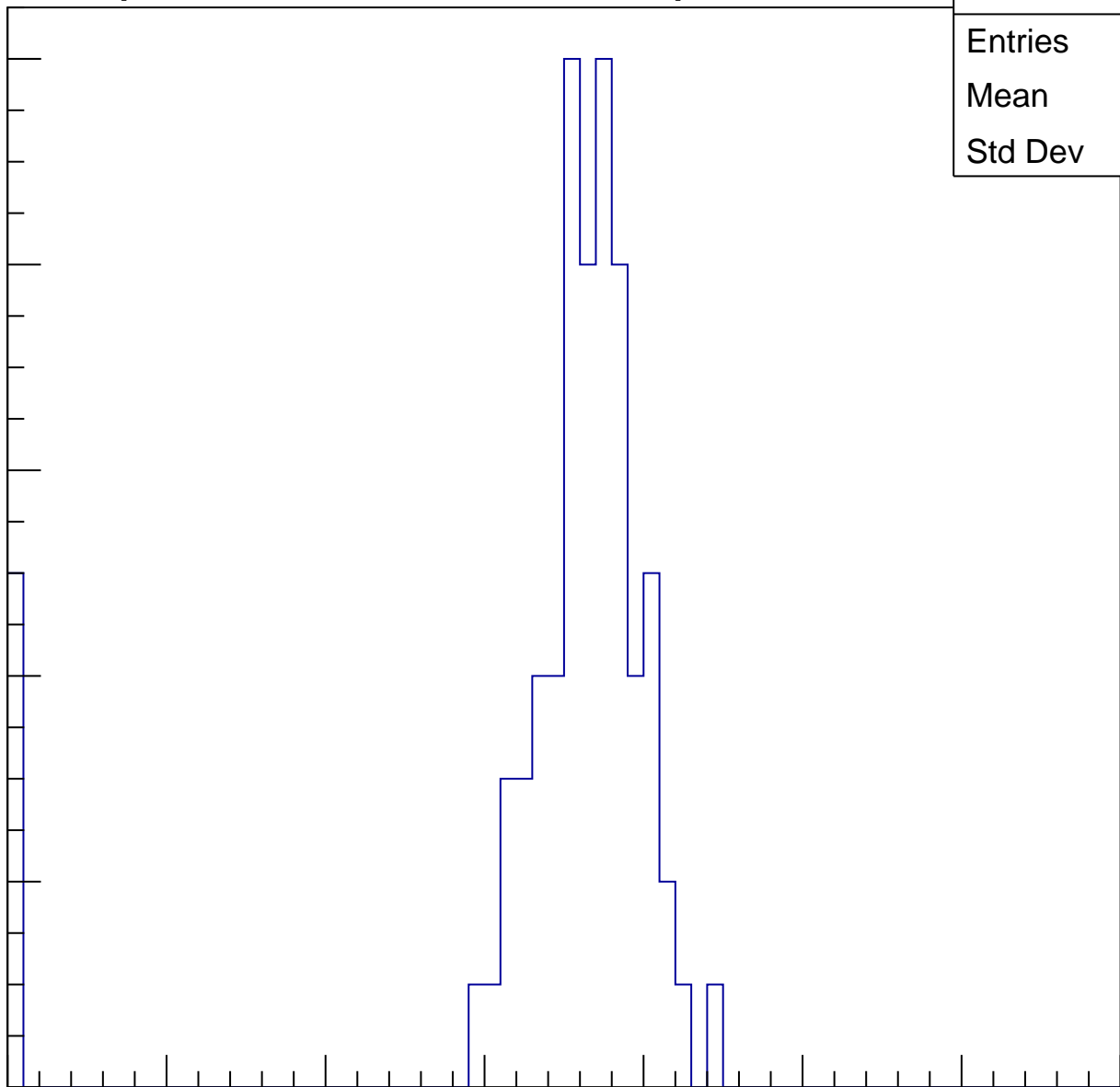
40

50

60

70

ampl

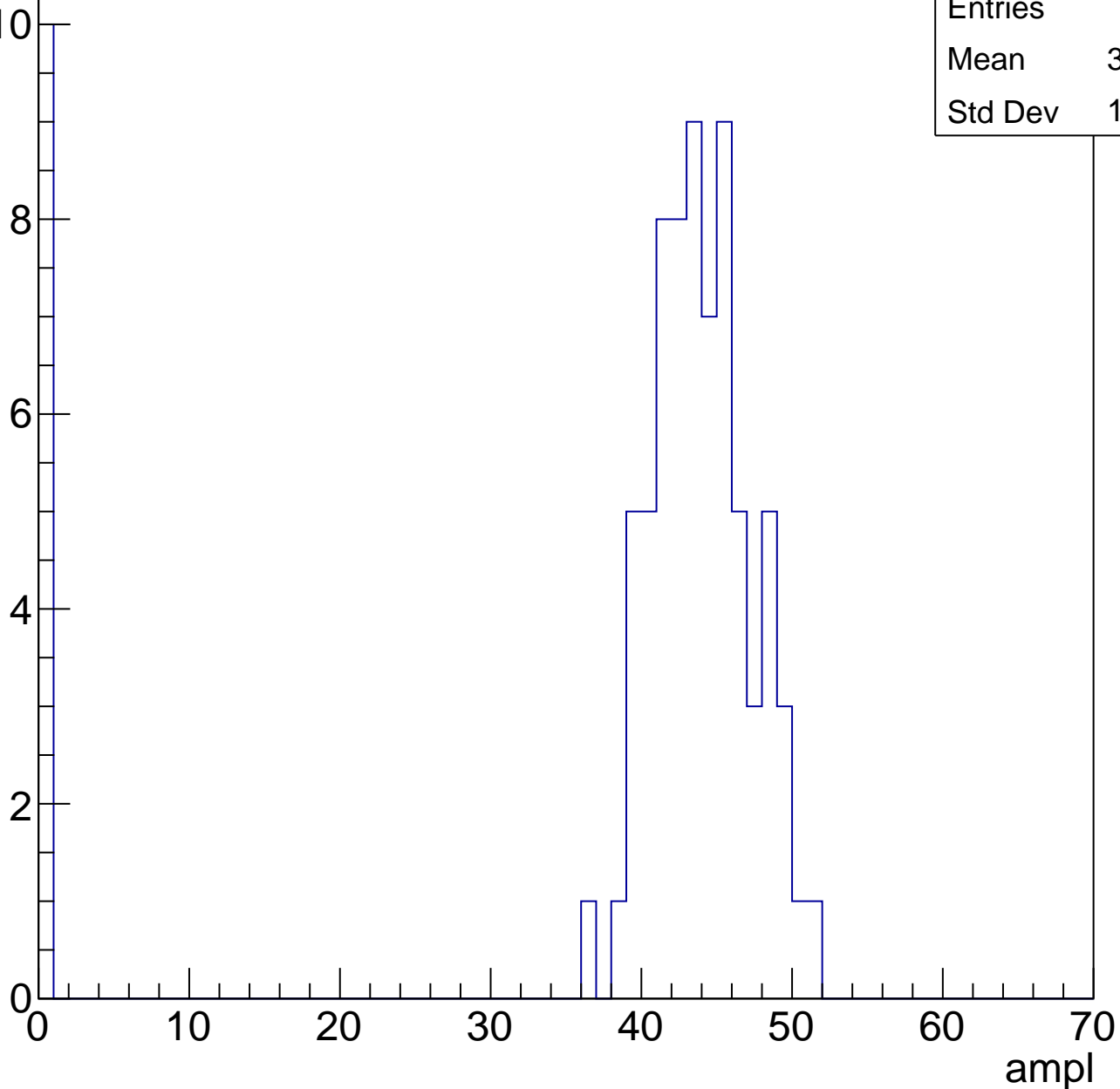


# B1L103S, U4-ch63, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 81    |
| Mean    | 38.17 |
| Std Dev | 14.62 |

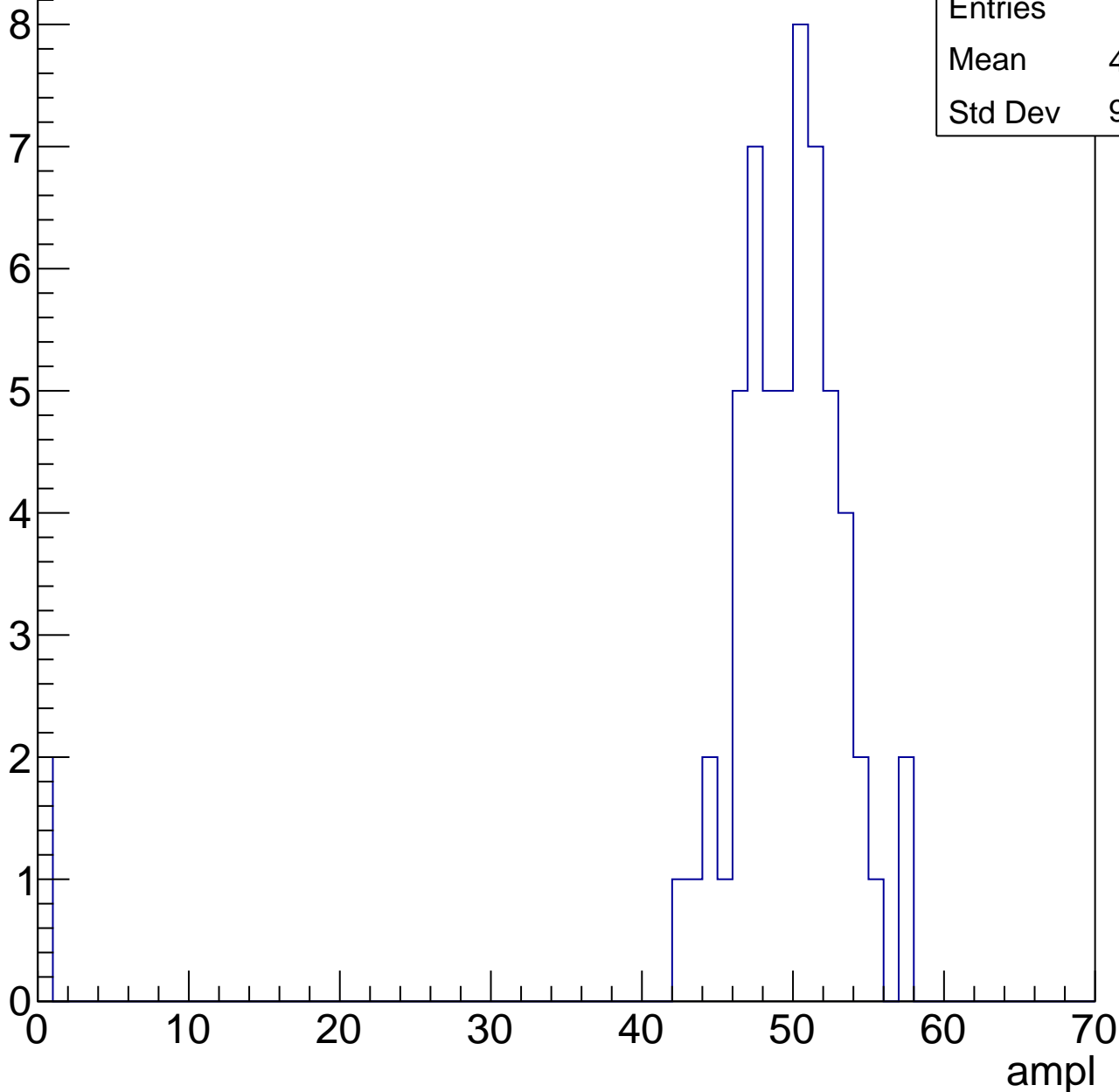


# B1L103S, U4-ch63, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 58    |
| Mean    | 47.72 |
| Std Dev | 9.555 |

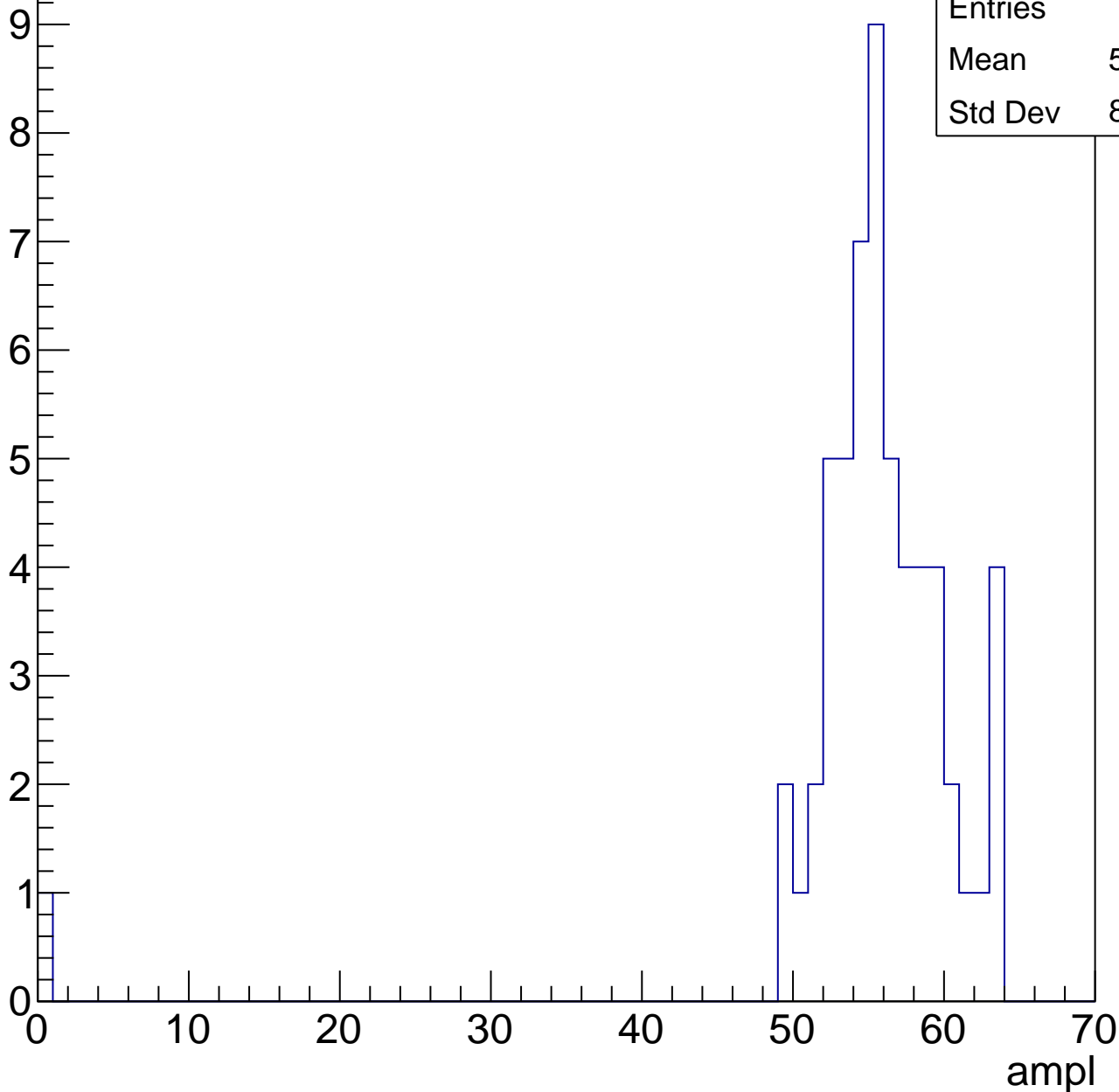


# B1L103S, U4-ch63, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 57    |
| Mean    | 54.72 |
| Std Dev | 8.093 |

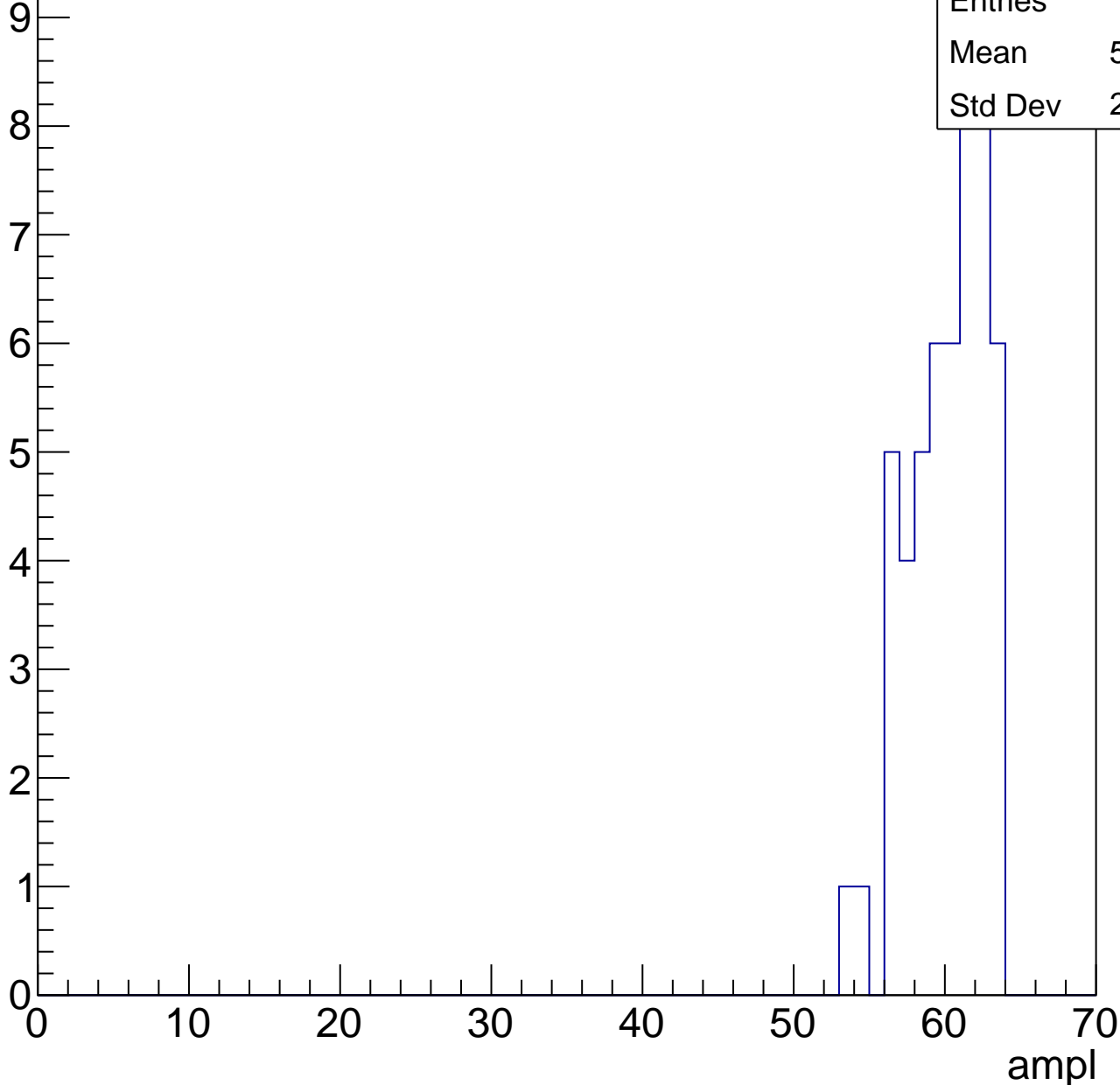


# B1L103S, U4-ch63, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

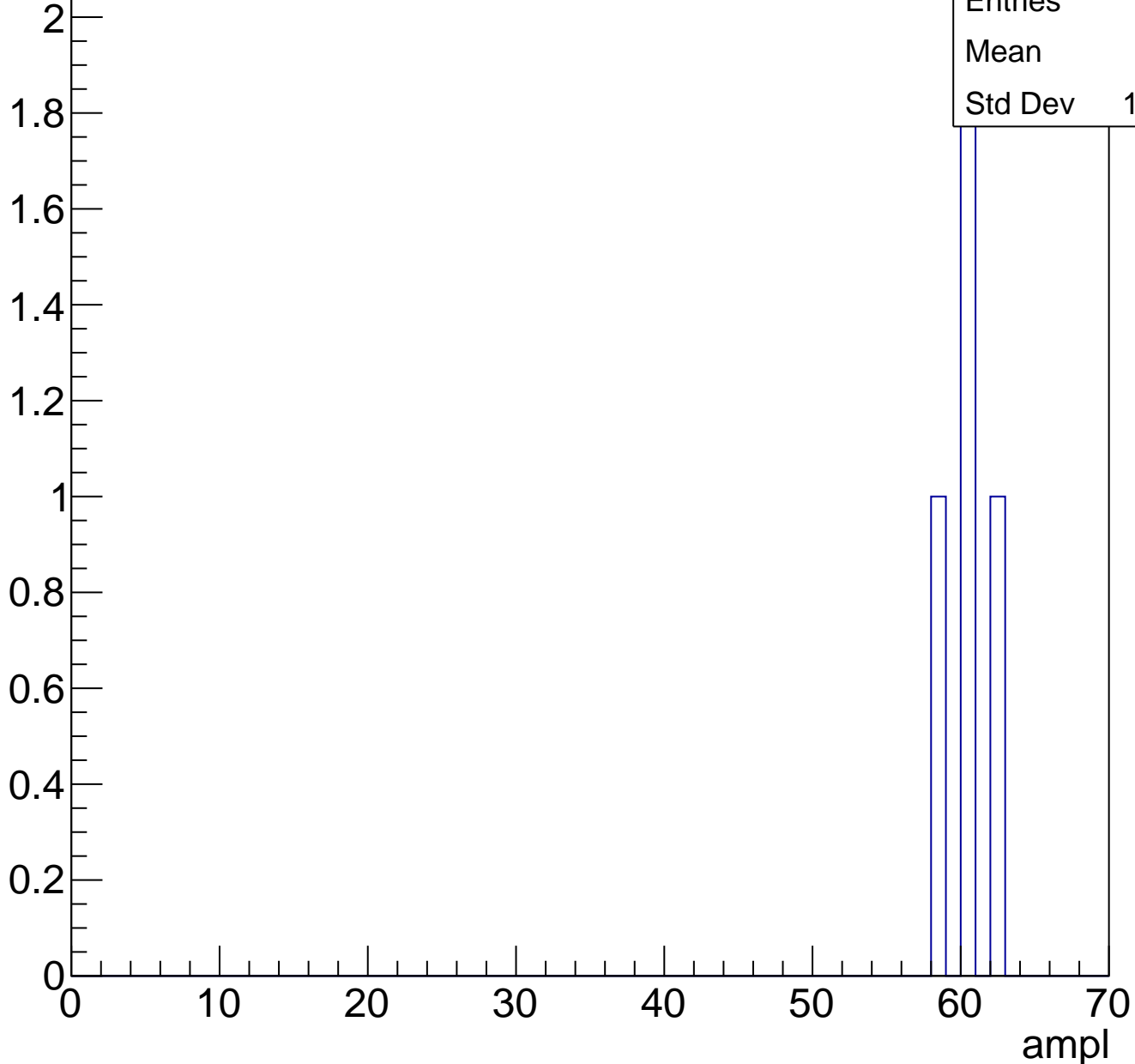
|         |       |
|---------|-------|
| Entries | 51    |
| Mean    | 59.65 |
| Std Dev | 2.488 |



# B1L103S, U4-ch63, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U4-ch63, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

|         |    |
|---------|----|
| Entries | 19 |
| Mean    | 0  |
| Std Dev | 0  |

ampl

# B1L103S, U4-ch64, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 75    |
| Mean    | 22.91 |
| Std Dev | 11.09 |

Entry

12

10

8

6

4

2

0

0

10

20

30

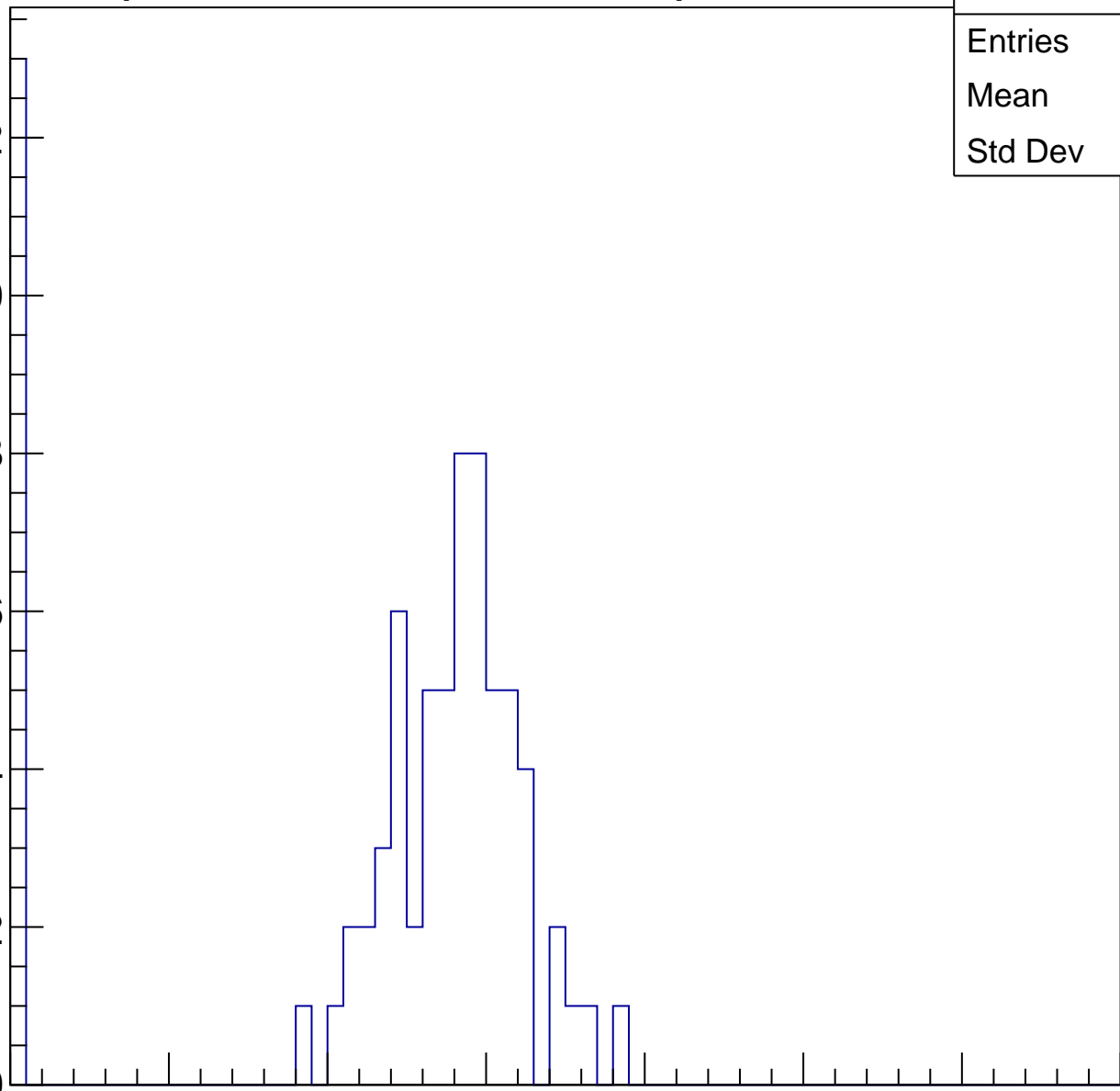
40

50

60

70

ampl

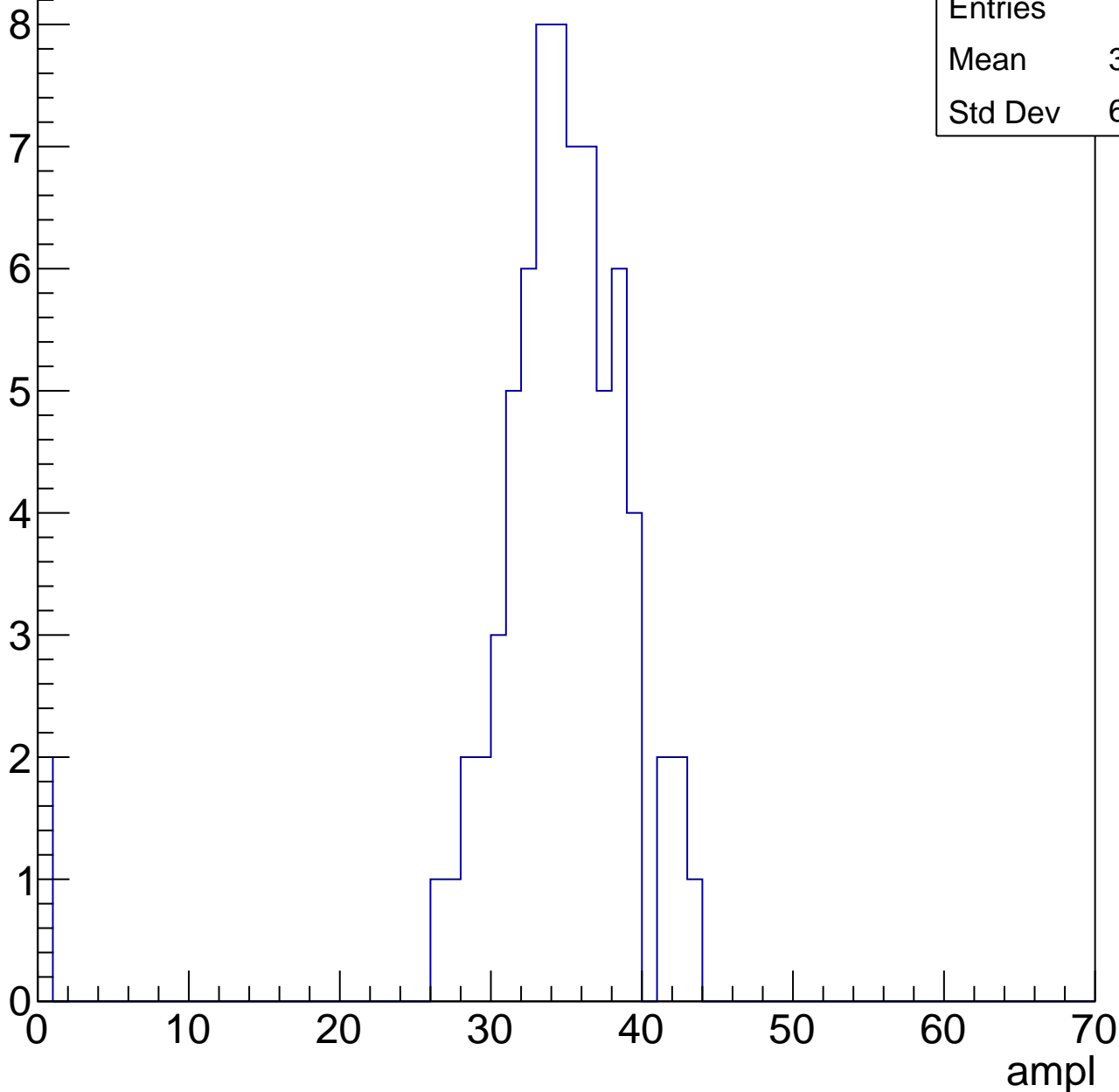


# B1L103S, U4-ch64, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 72    |
| Mean    | 33.54 |
| Std Dev | 6.708 |



# B1L103S, U4-ch64, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 67    |
| Mean    | 33.69 |
| Std Dev | 15.27 |

Entry

10

8

6

4

2

0

0

10

20

30

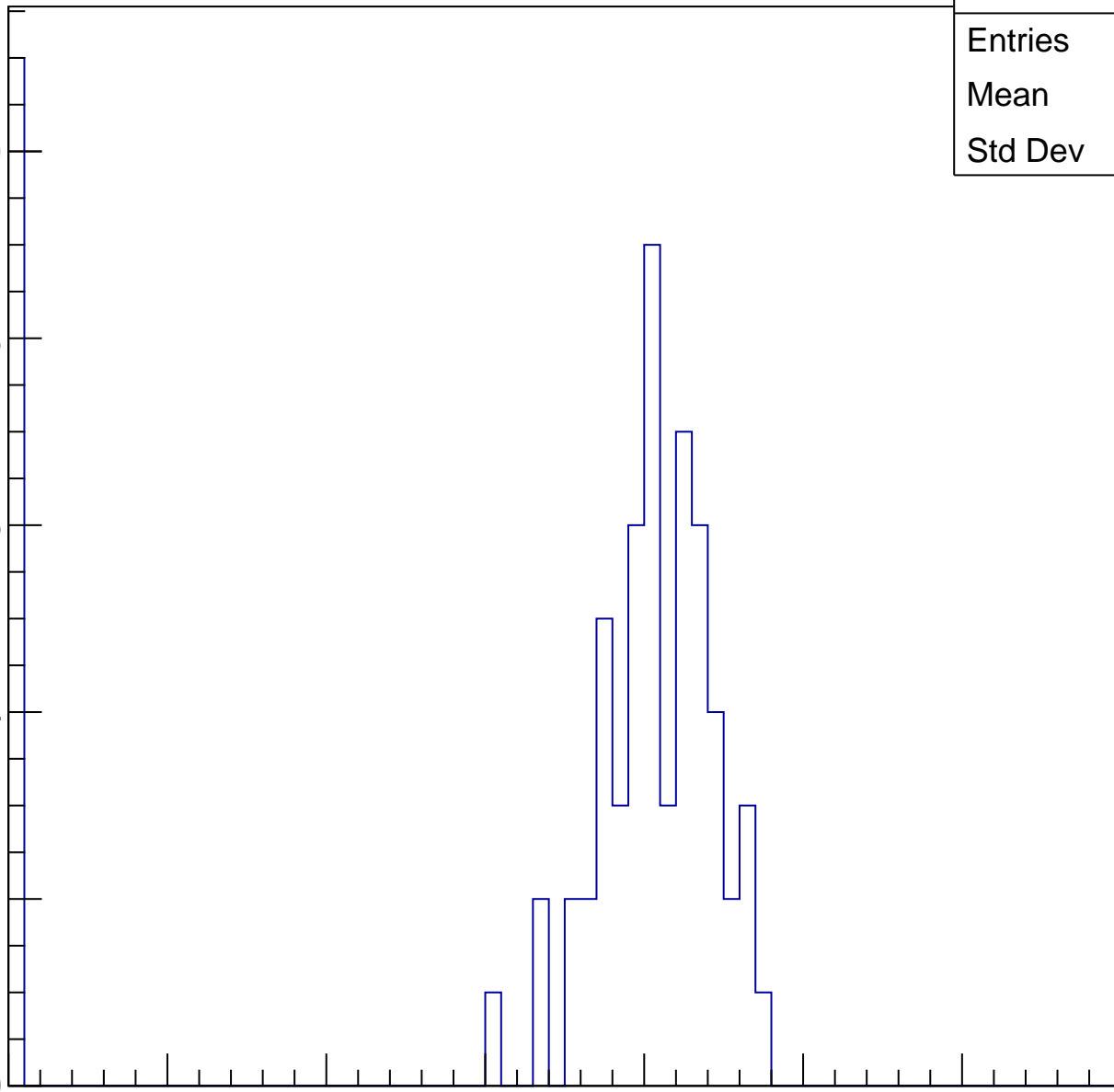
40

50

60

70

ampl

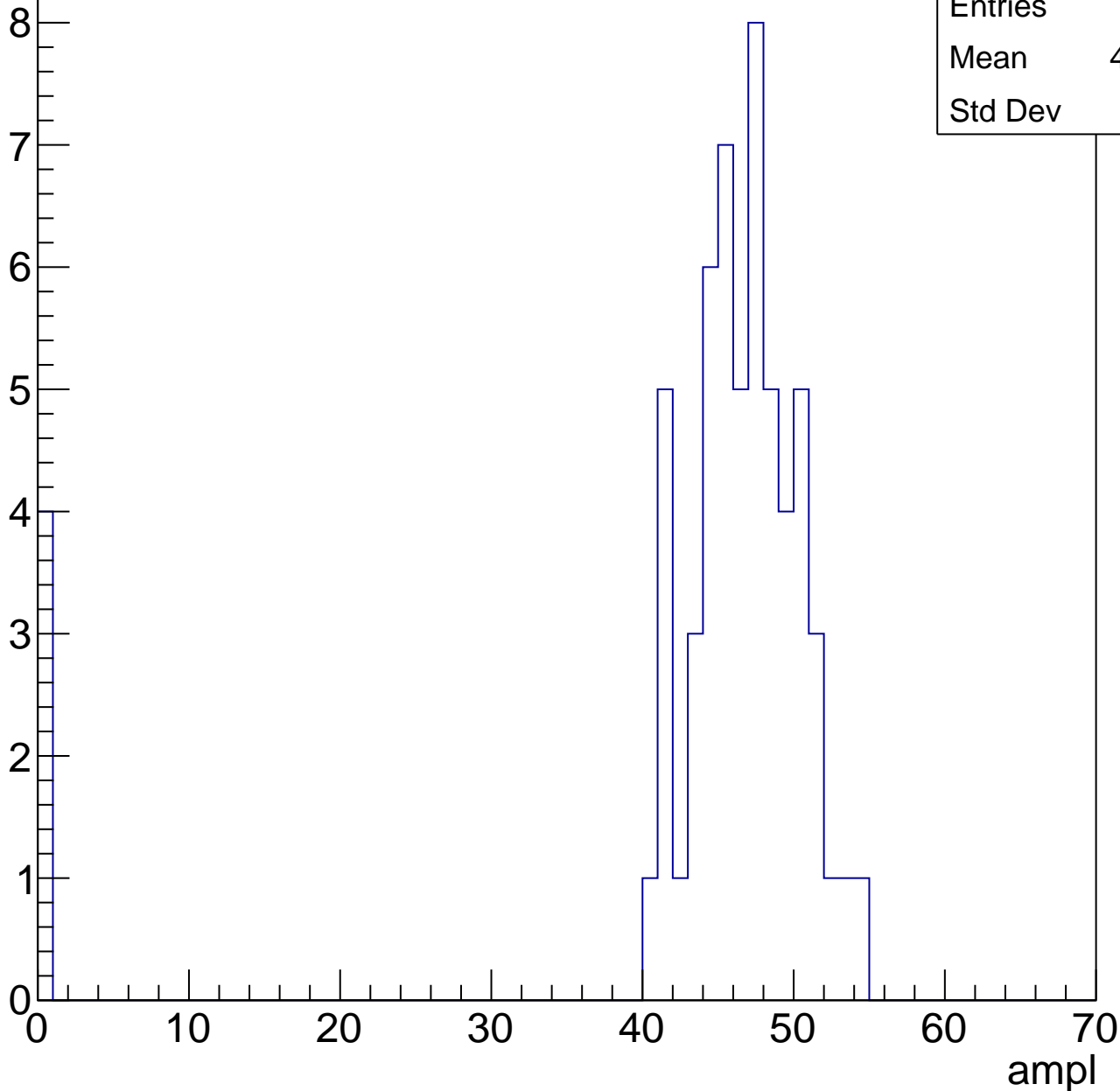


# B1L103S, U4-ch64, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

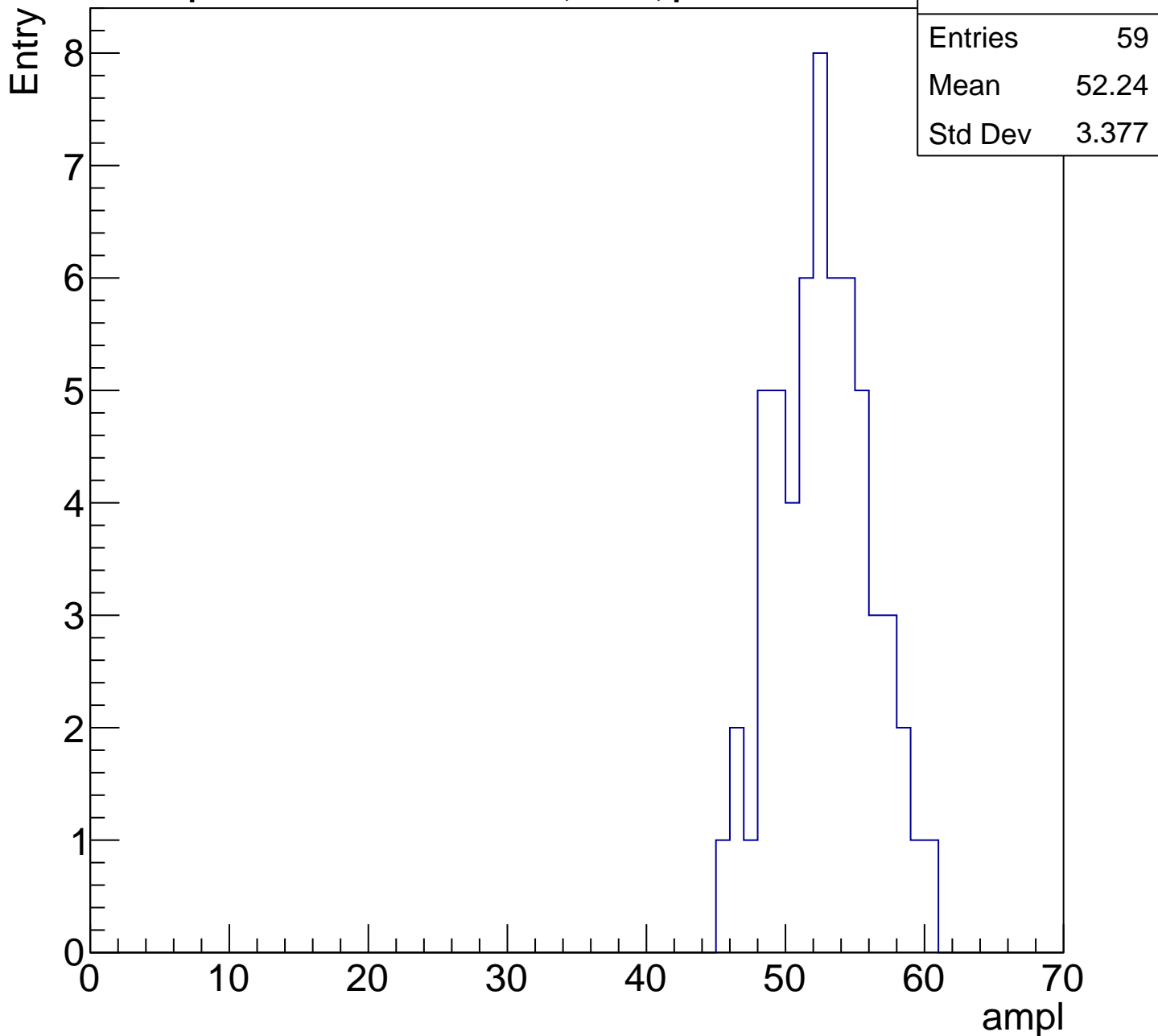
Entry

|         |       |
|---------|-------|
| Entries | 60    |
| Mean    | 43.32 |
| Std Dev | 12    |



# B1L103S, U4-ch64, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

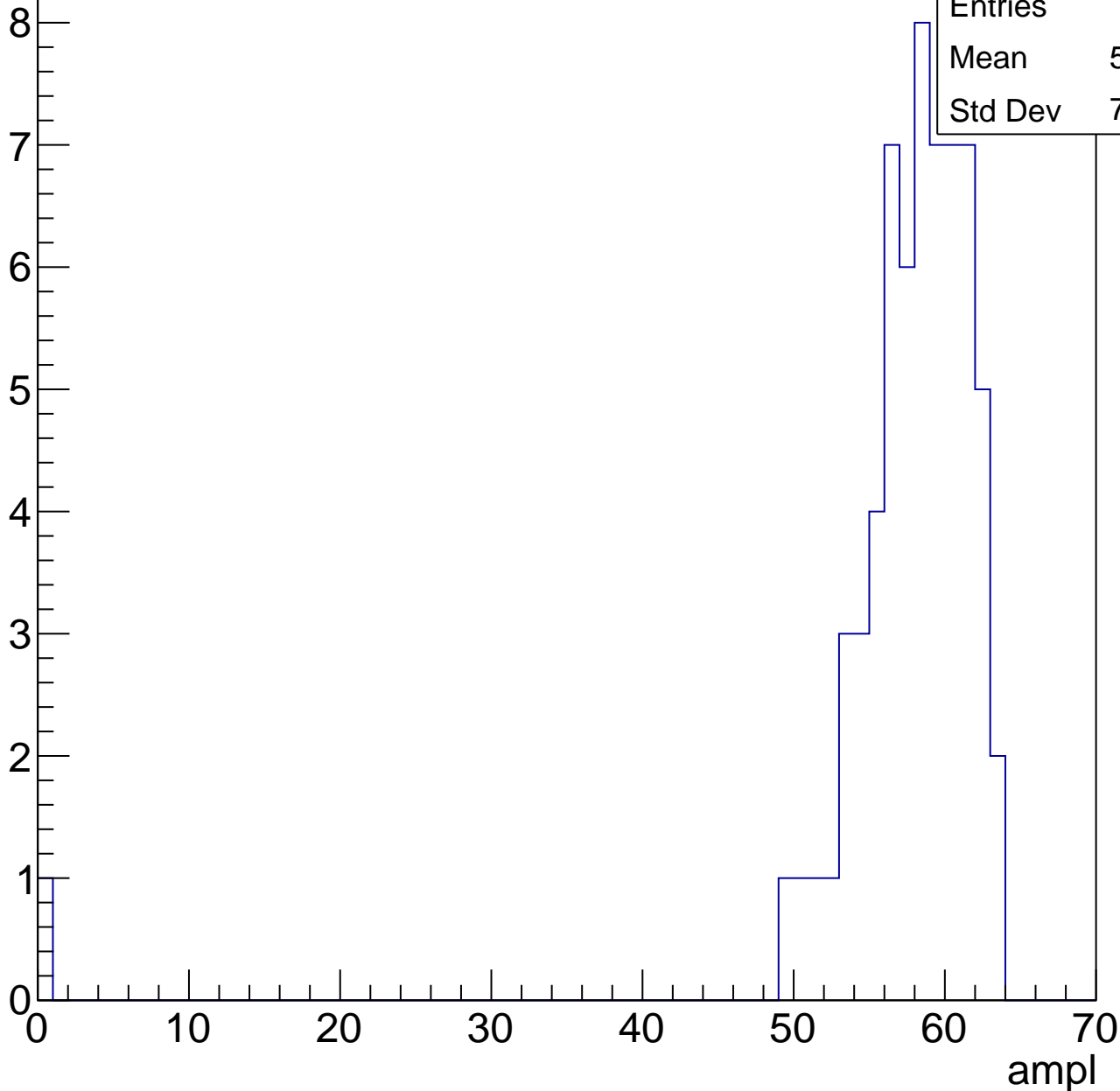


# B1L103S, U4-ch64, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 64    |
| Mean    | 56.83 |
| Std Dev | 7.833 |

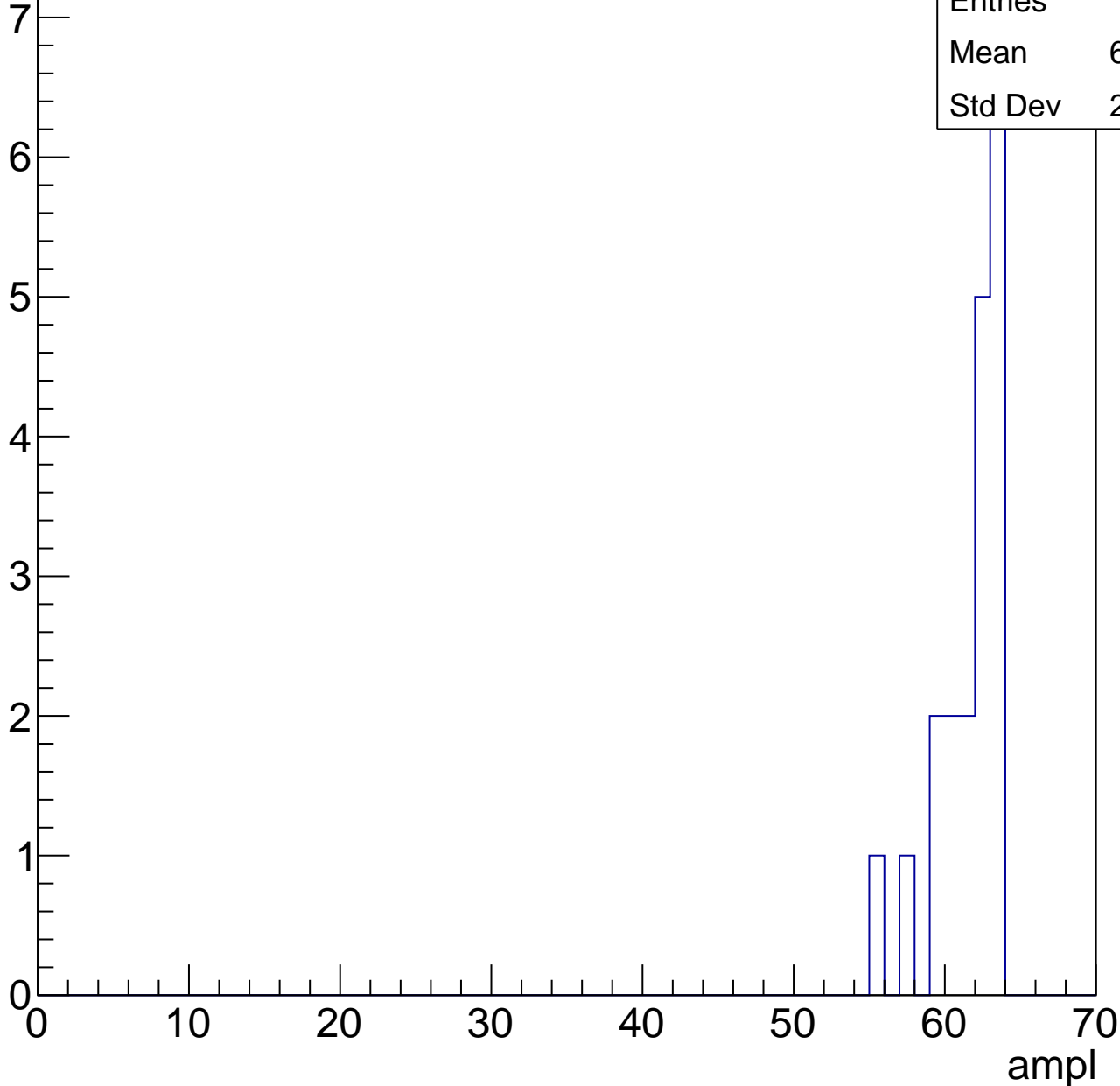


# B1L103S, U4-ch64, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 20    |
| Mean    | 61.15 |
| Std Dev | 2.174 |

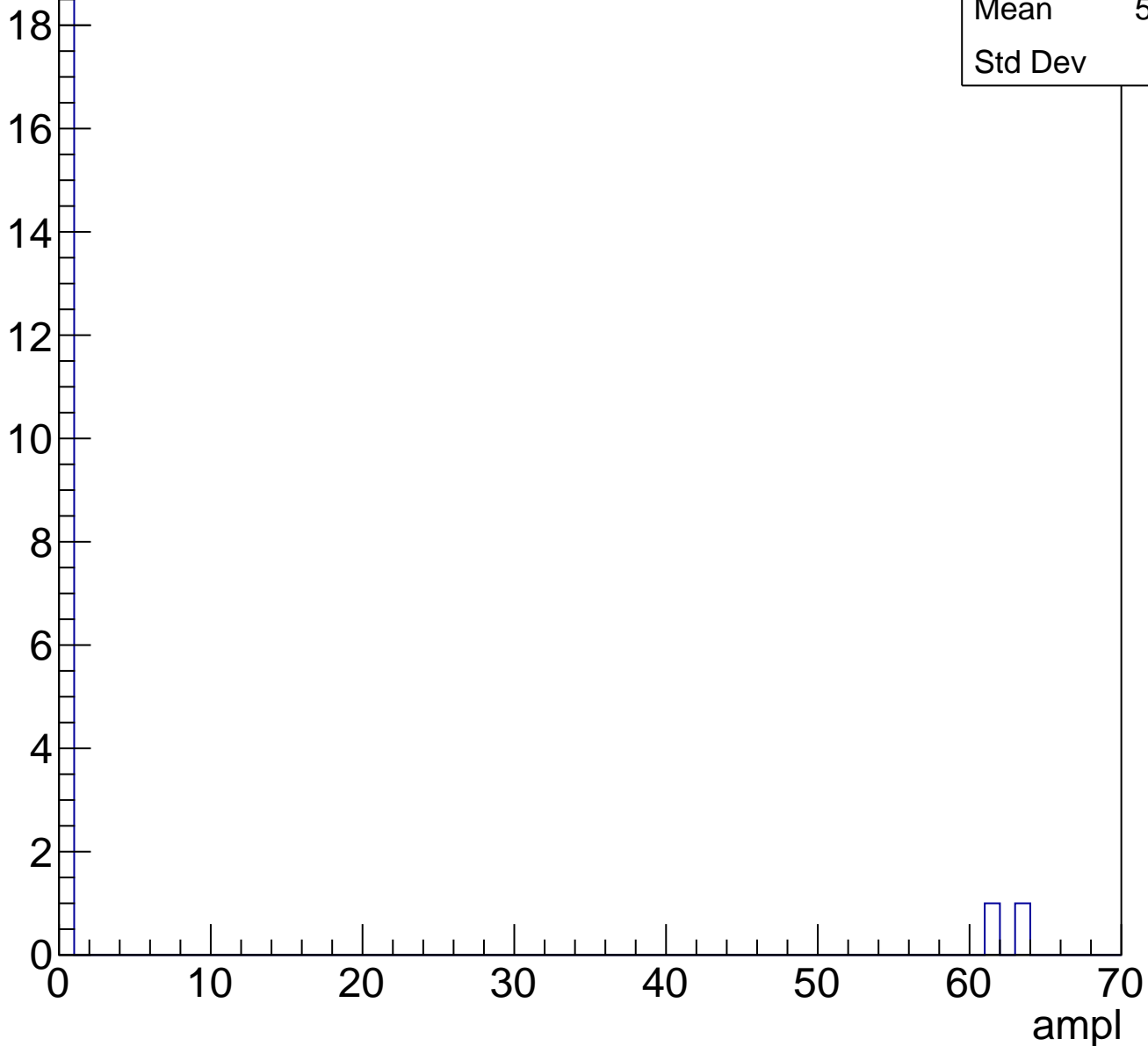




# B1L103S, U4-ch64, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

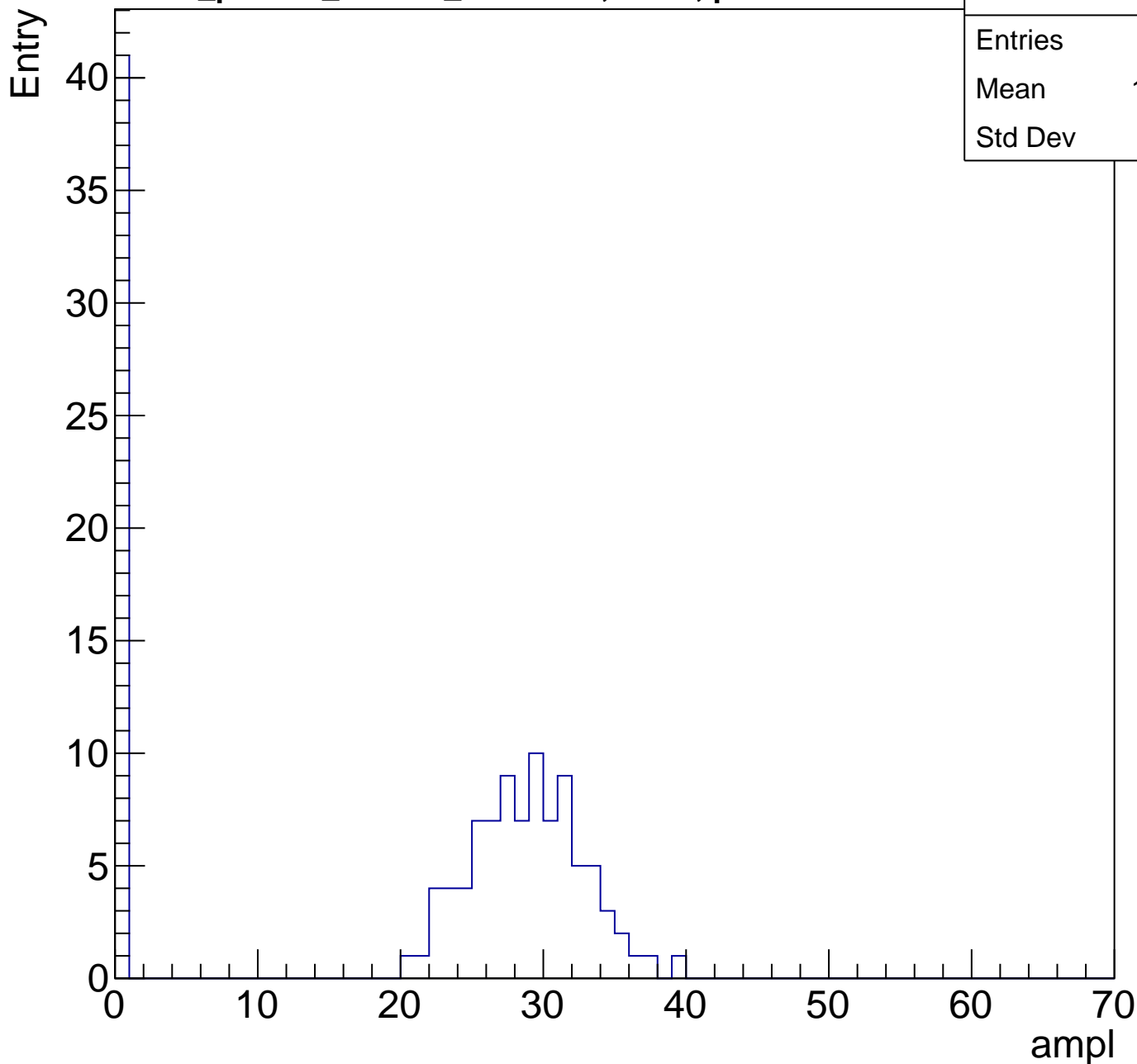
Entry



# B1L103S, U4-ch65, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 129   |
| Mean    | 19.39 |
| Std Dev | 13.61 |



# B1L103S, U4-ch65, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 69    |
| Mean    | 28.84 |
| Std Dev | 14.19 |

Entry

12

10

8

6

4

2

0

0

10

20

30

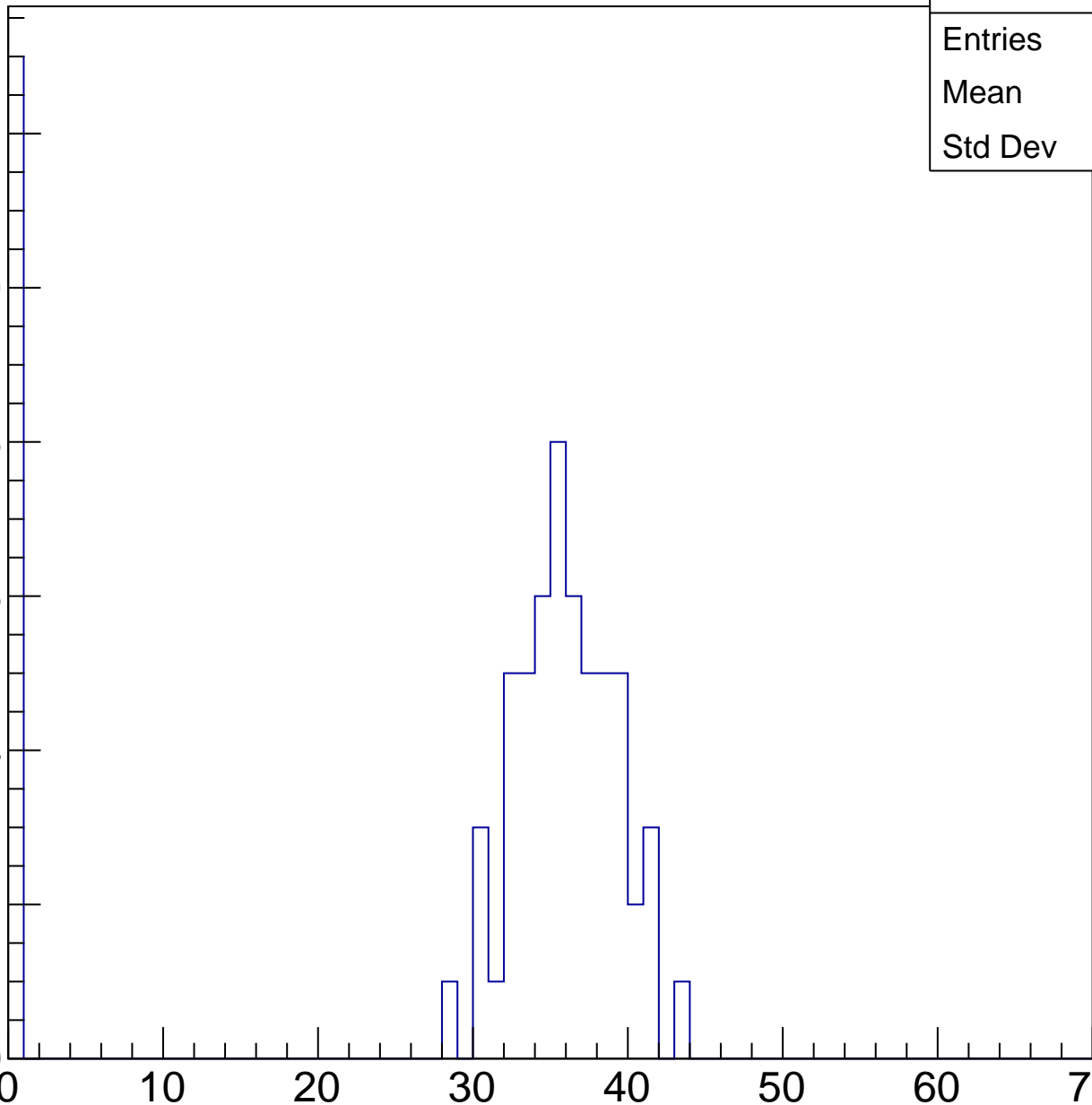
40

50

60

70

ampl



# B1L103S, U4-ch65, adc2

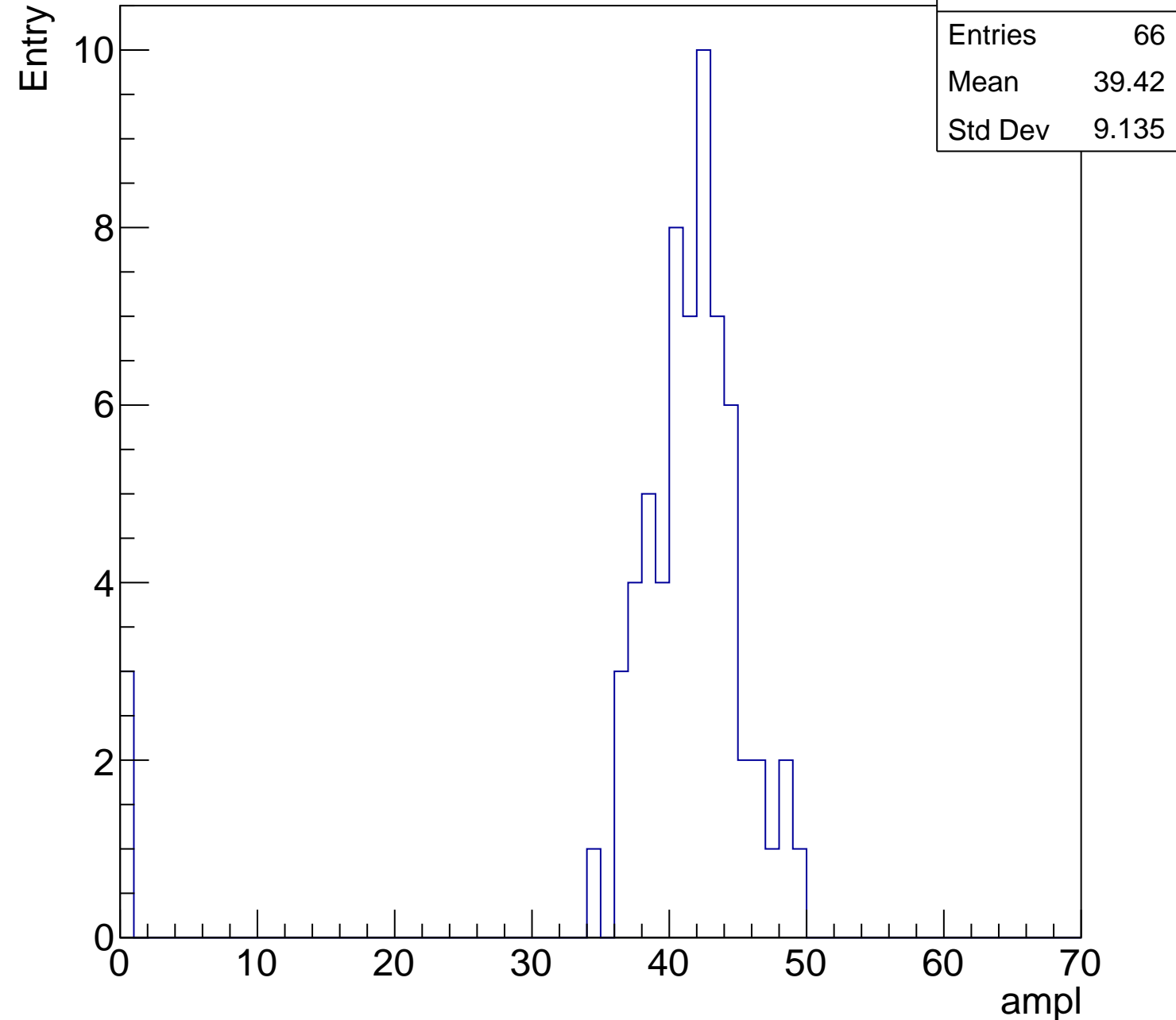
calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 66    |
| Mean    | 39.42 |
| Std Dev | 9.135 |

Entry

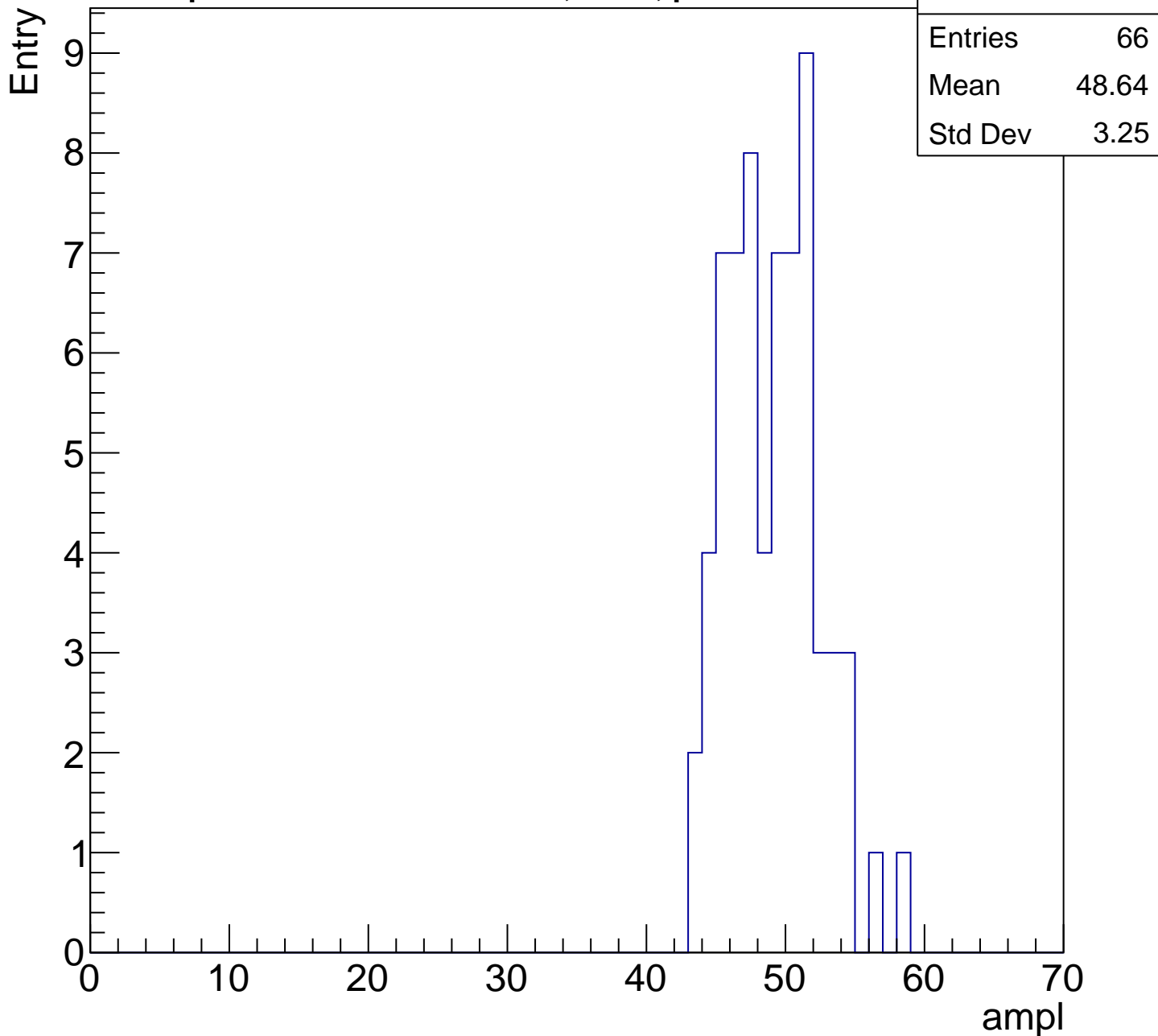
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch65, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

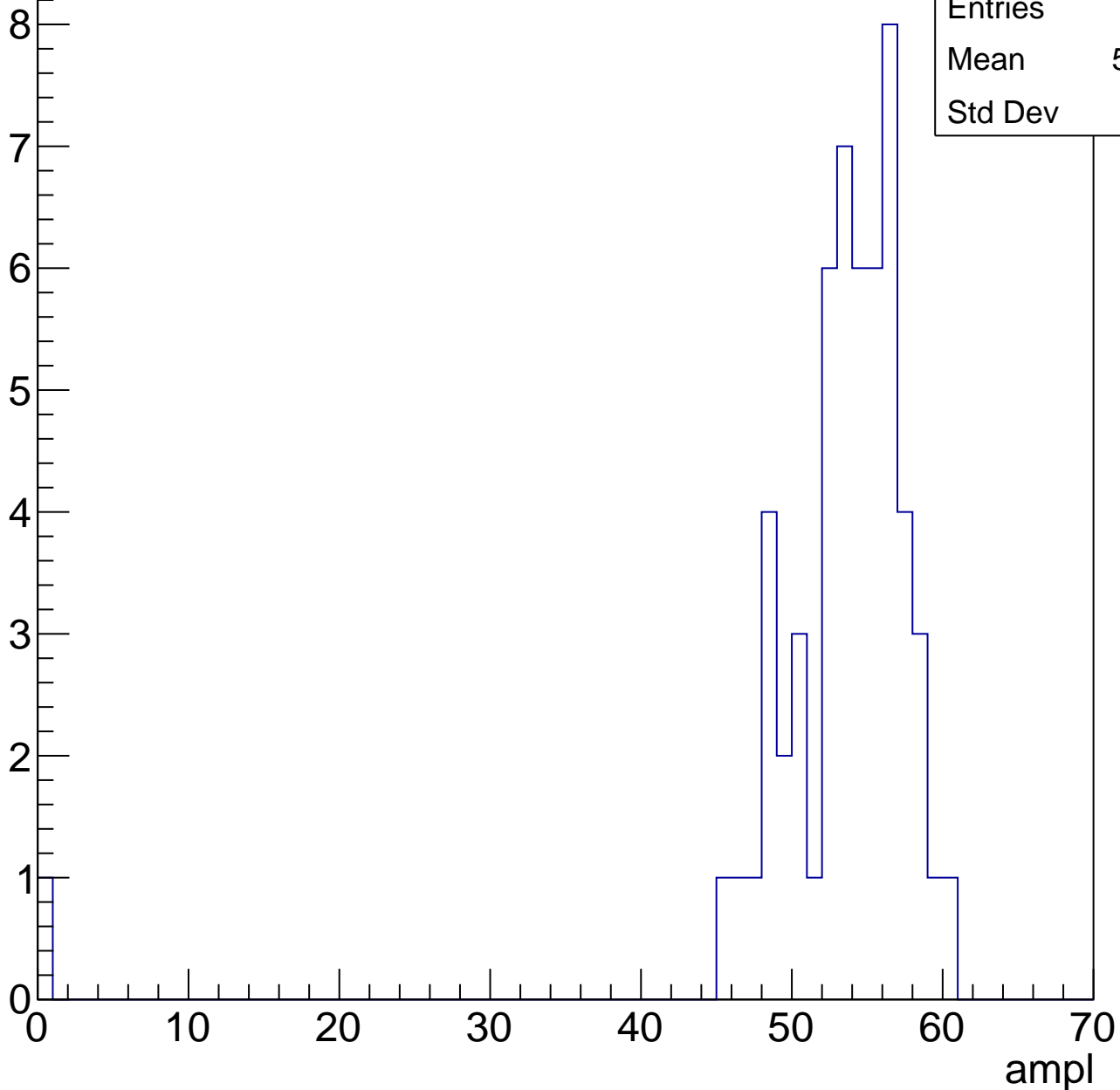


# B1L103S, U4-ch65, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 56    |
| Mean    | 52.41 |
| Std Dev | 7.83  |

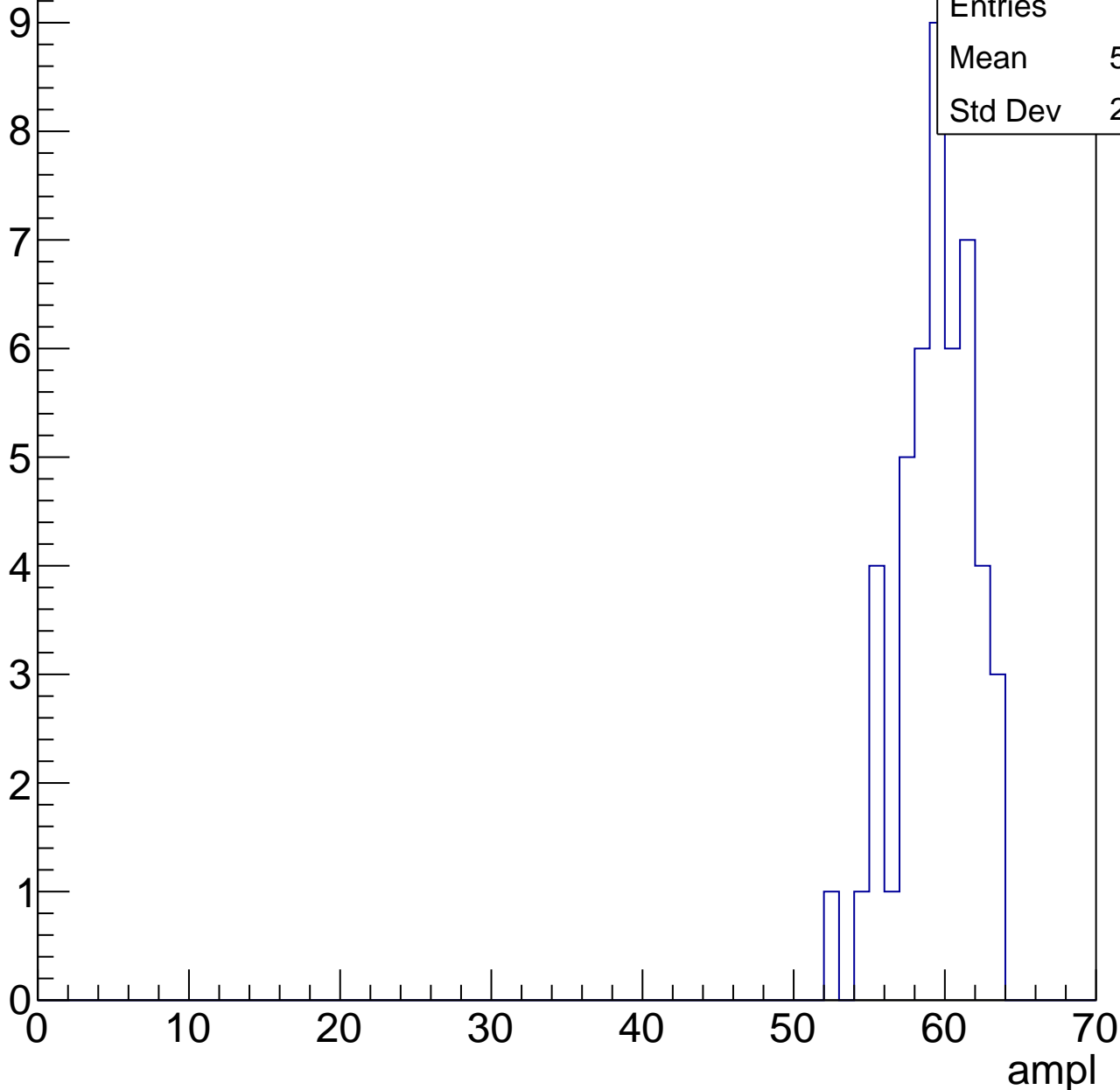


# B1L103S, U4-ch65, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 47    |
| Mean    | 58.94 |
| Std Dev | 2.487 |

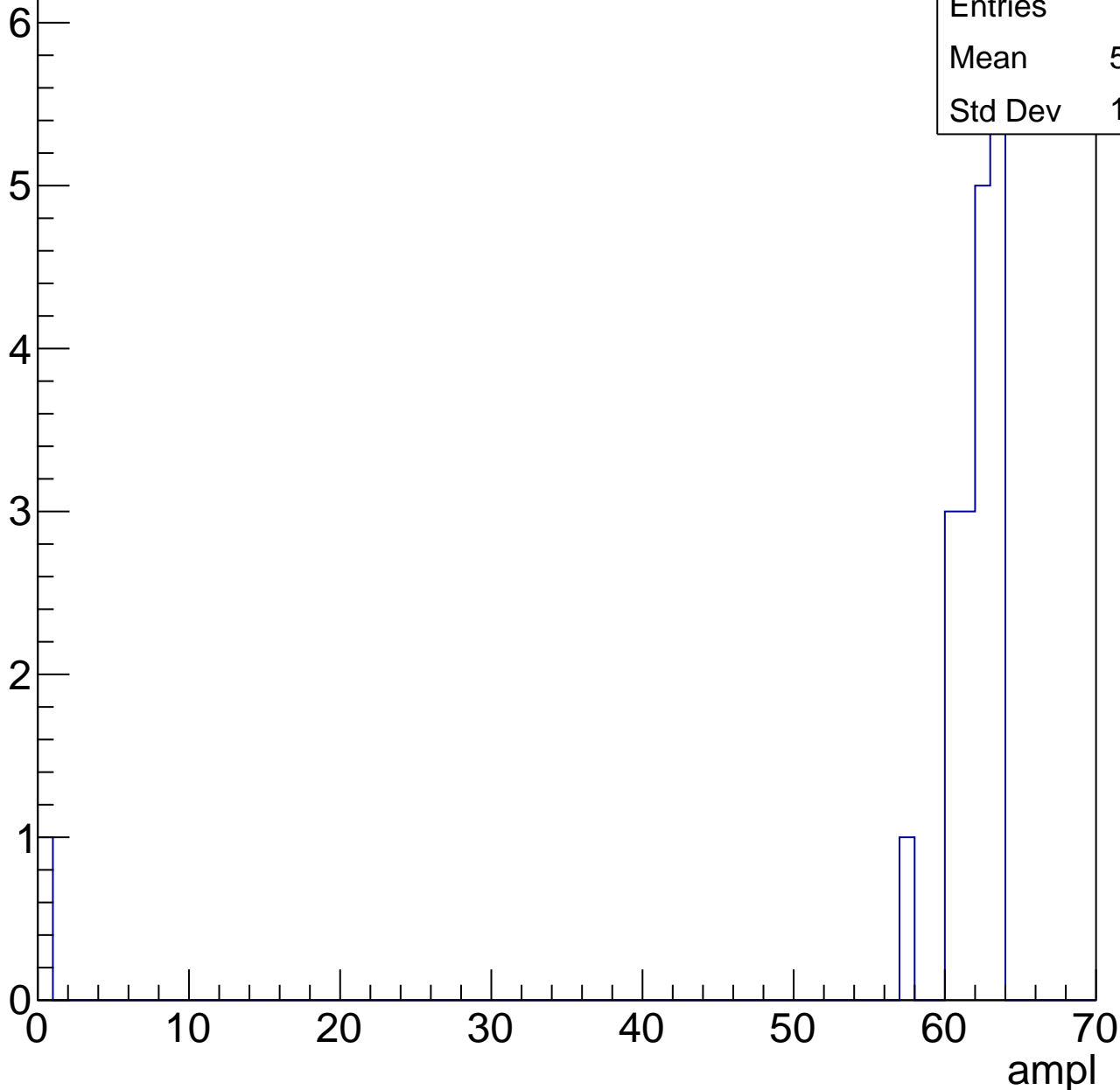


# B1L103S, U4-ch65, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 19    |
| Mean    | 58.32 |
| Std Dev | 13.83 |

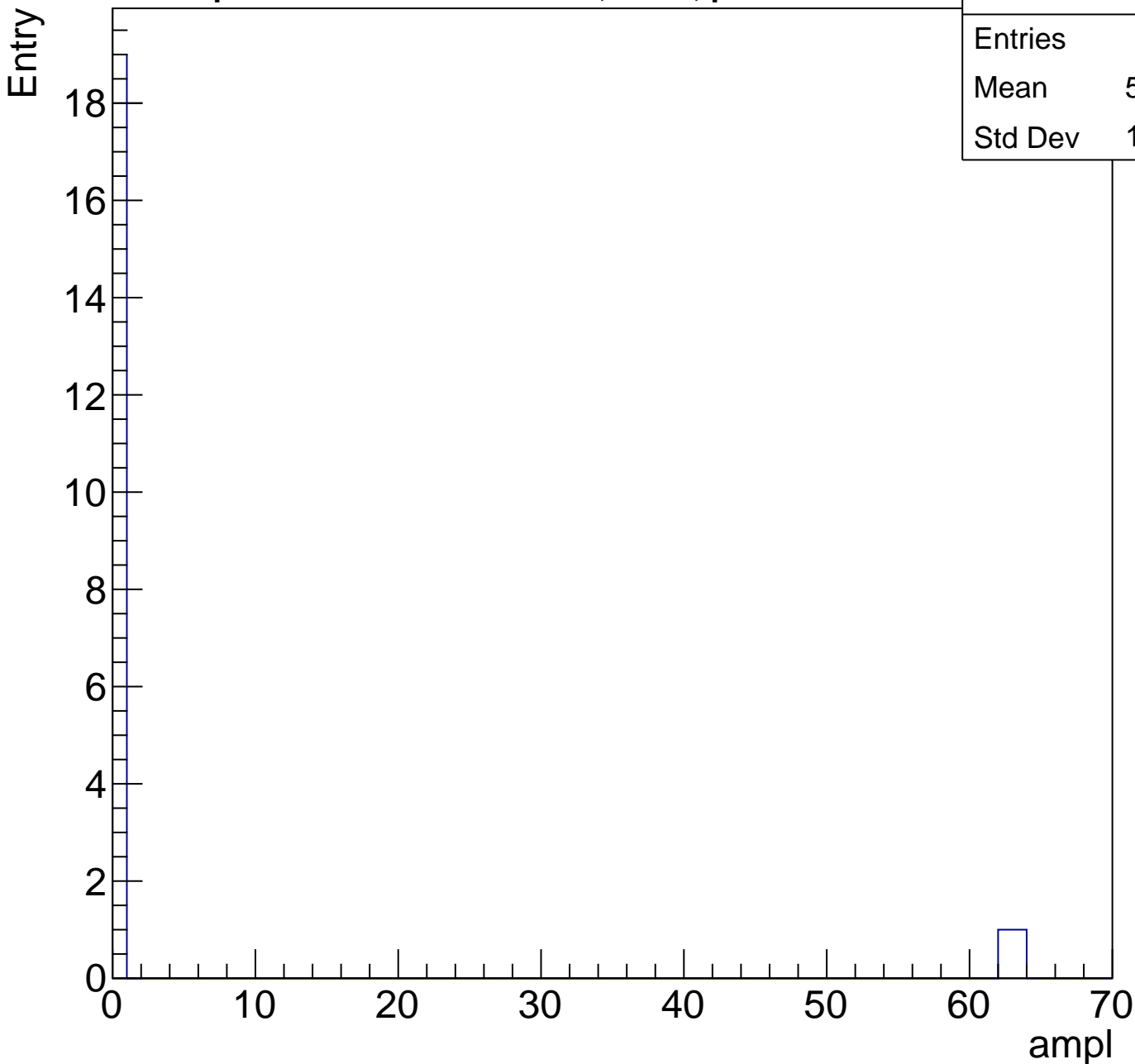




# B1L103S, U4-ch65, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 21    |
| Mean    | 5.952 |
| Std Dev | 18.35 |

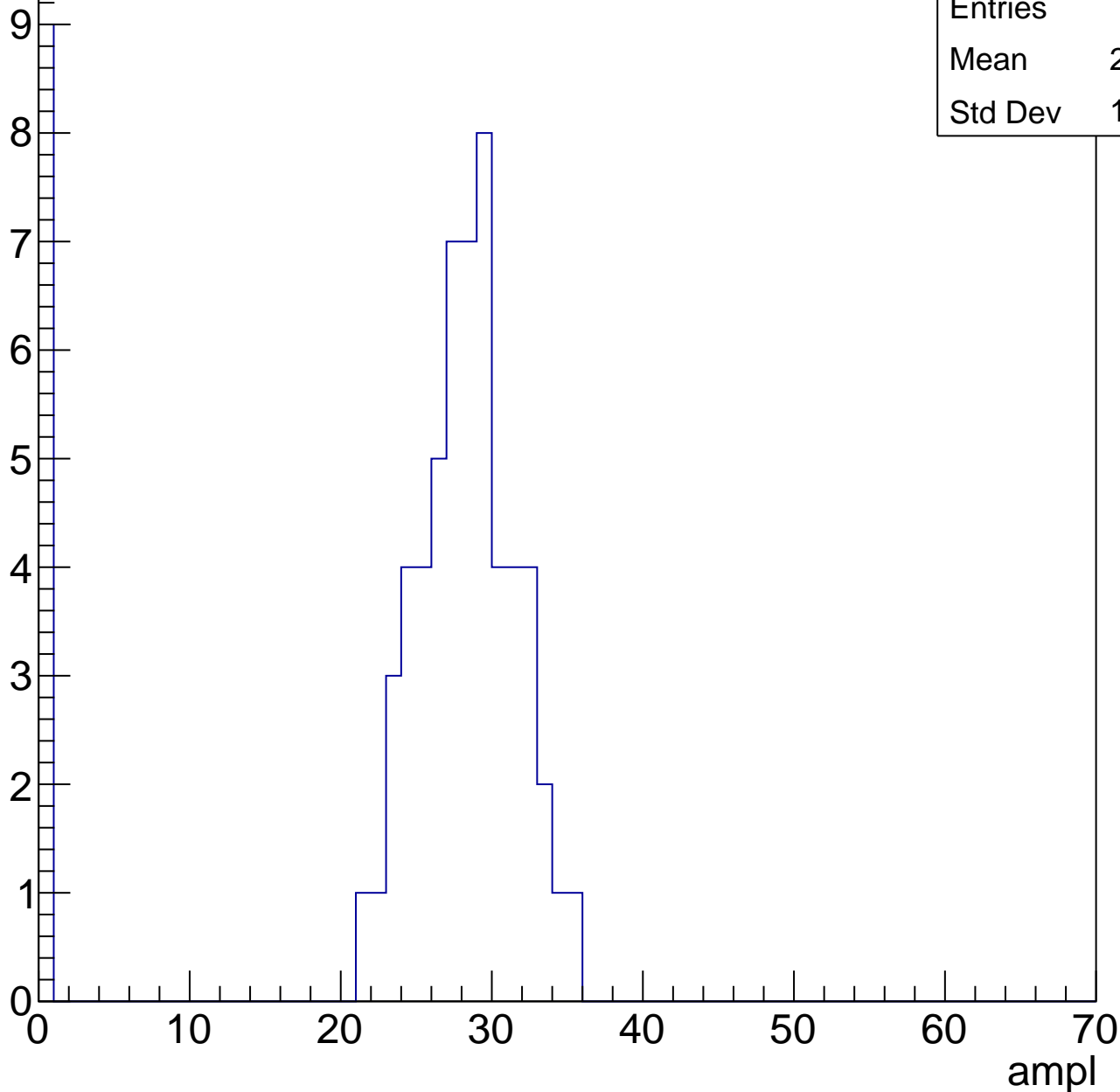


# B1L103S, U4-ch66, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 65    |
| Mean    | 24.03 |
| Std Dev | 10.06 |

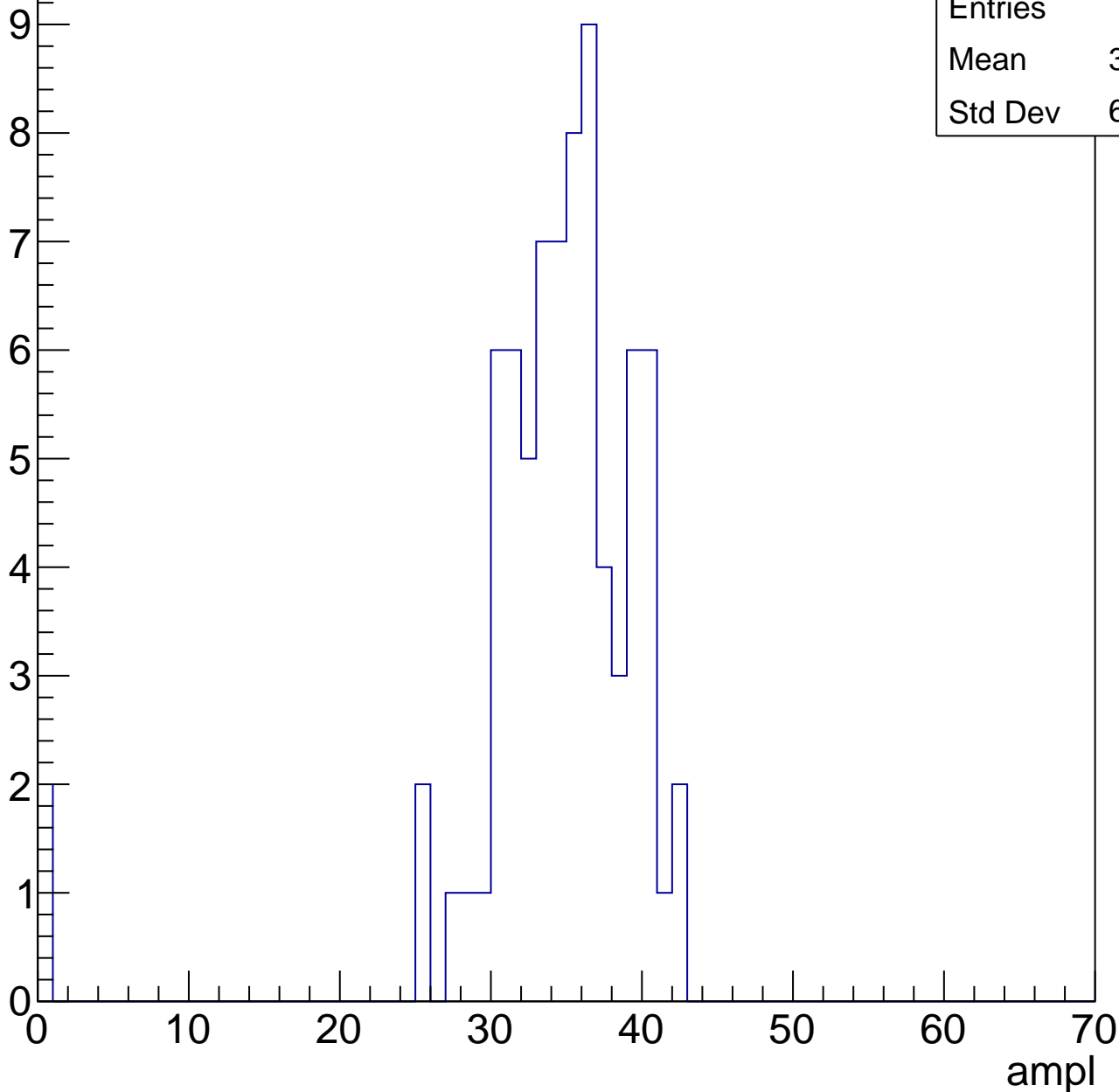


# B1L103S, U4-ch66, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 77    |
| Mean    | 33.69 |
| Std Dev | 6.669 |

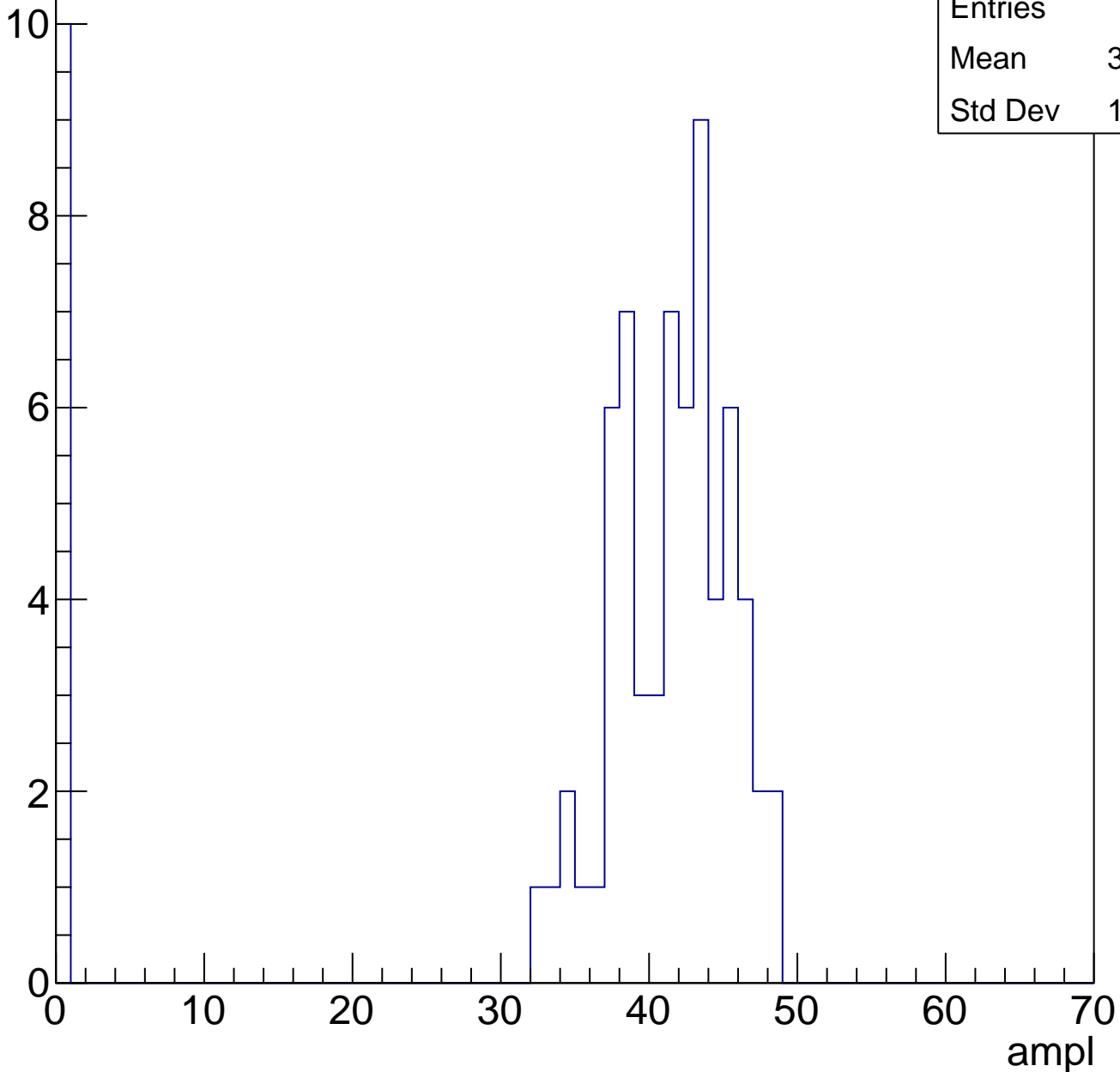


# B1L103S, U4-ch66, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 75    |
| Mean    | 35.67 |
| Std Dev | 14.42 |

Entry

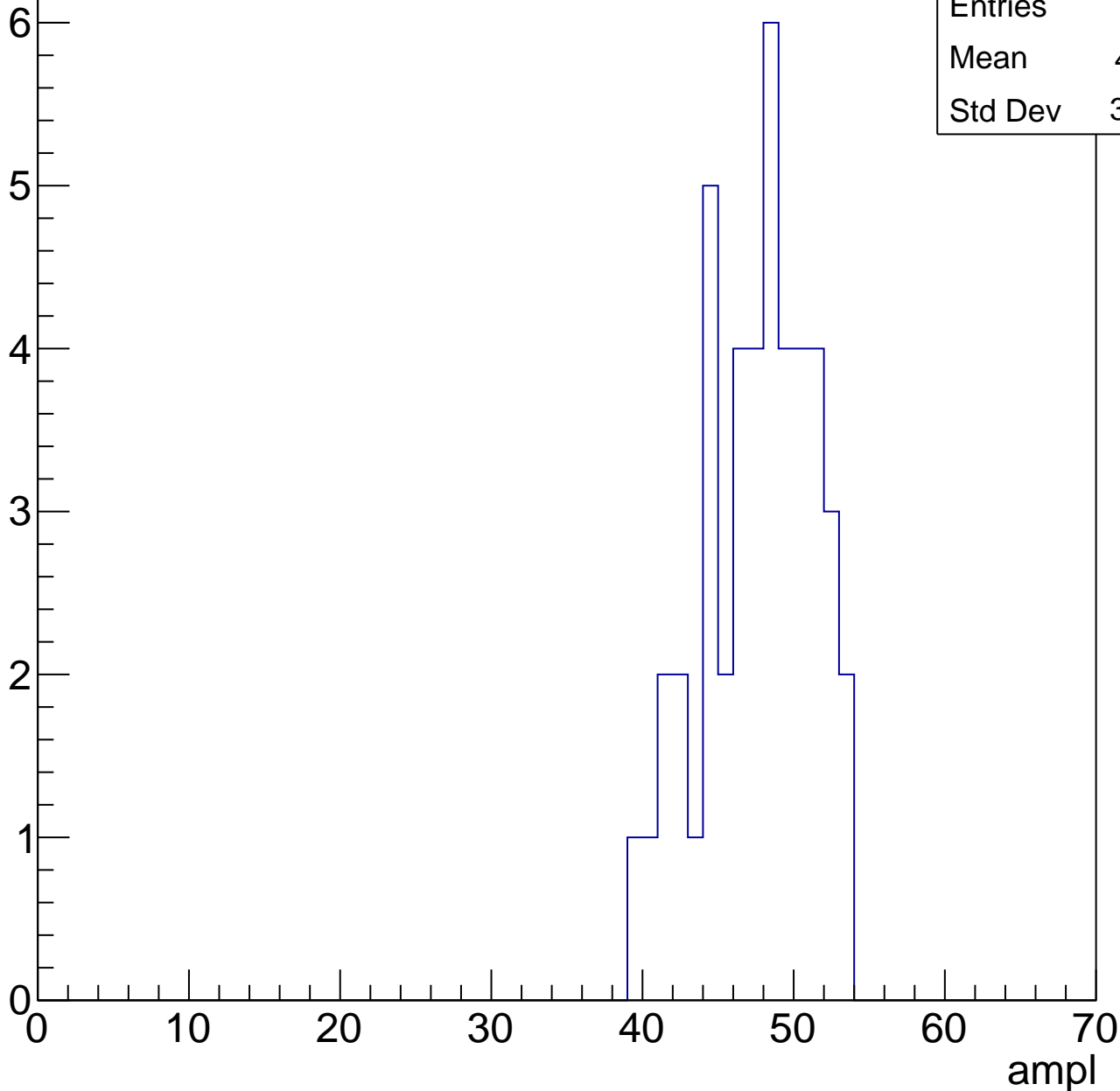


# B1L103S, U4-ch66, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 45    |
| Mean    | 47.11 |
| Std Dev | 3.579 |

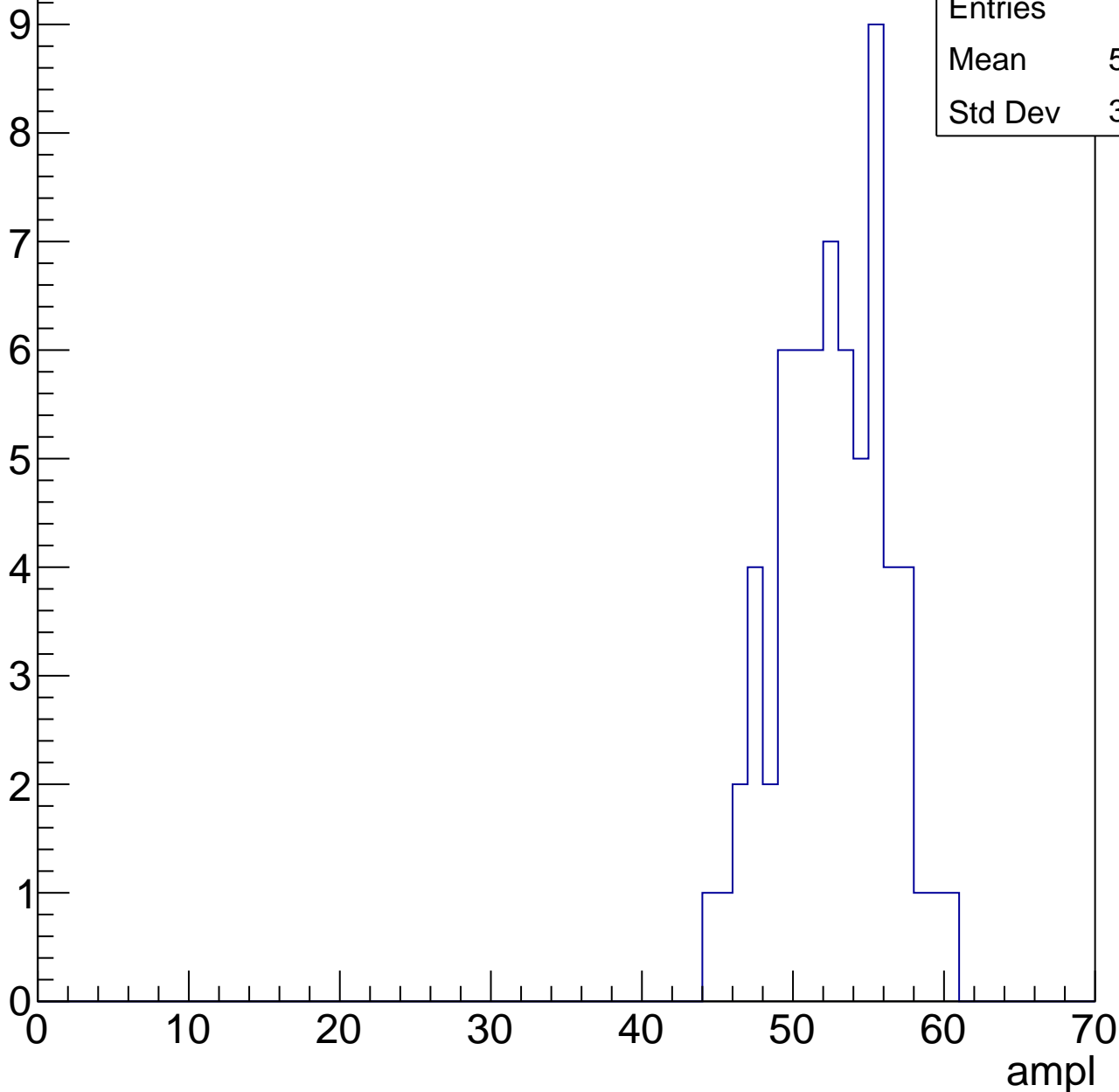


# B1L103S, U4-ch66, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

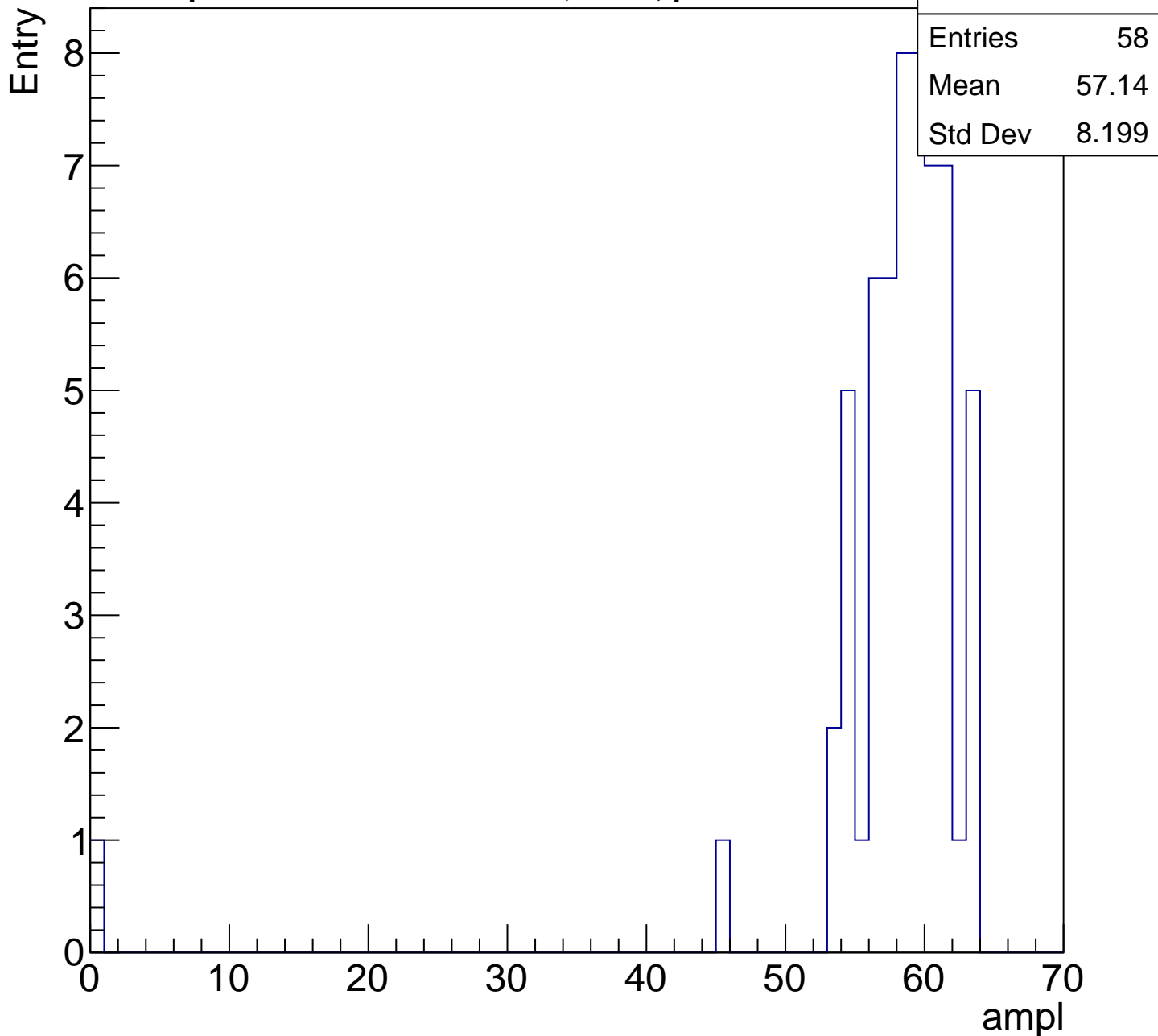
Entry

|         |       |
|---------|-------|
| Entries | 66    |
| Mean    | 52.14 |
| Std Dev | 3.524 |



# B1L103S, U4-ch66, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

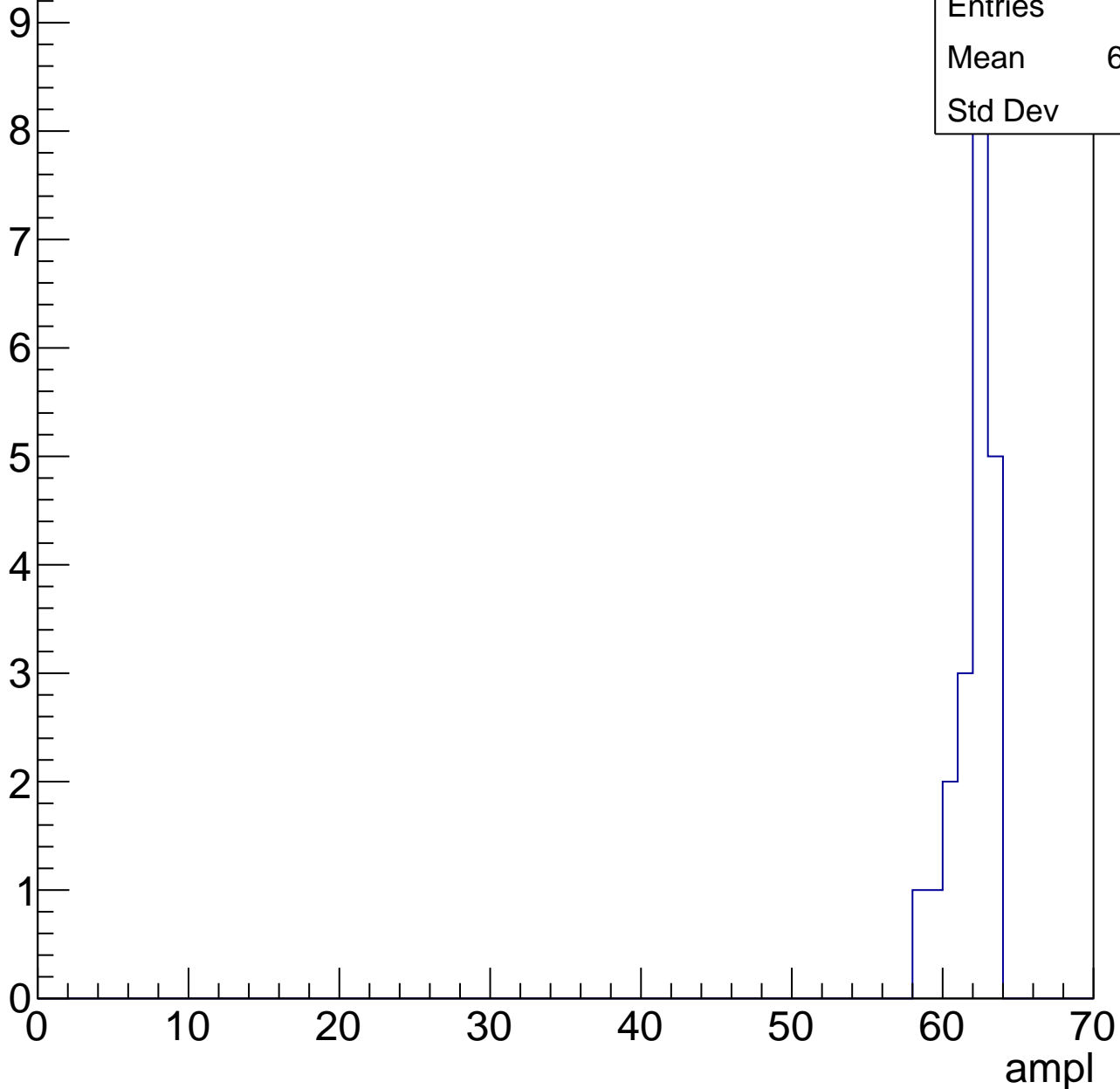


# B1L103S, U4-ch66, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 21    |
| Mean    | 61.57 |
| Std Dev | 1.33  |





# B1L103S, U4-ch66, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 19    |
| Mean    | 1.105 |
| Std Dev | 4.689 |

Entry



# B1L103S, U4-ch67, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 99    |
| Mean    | 21.26 |
| Std Dev | 13.69 |

Entry

25

20

15

10

5

0

0

10

20

30

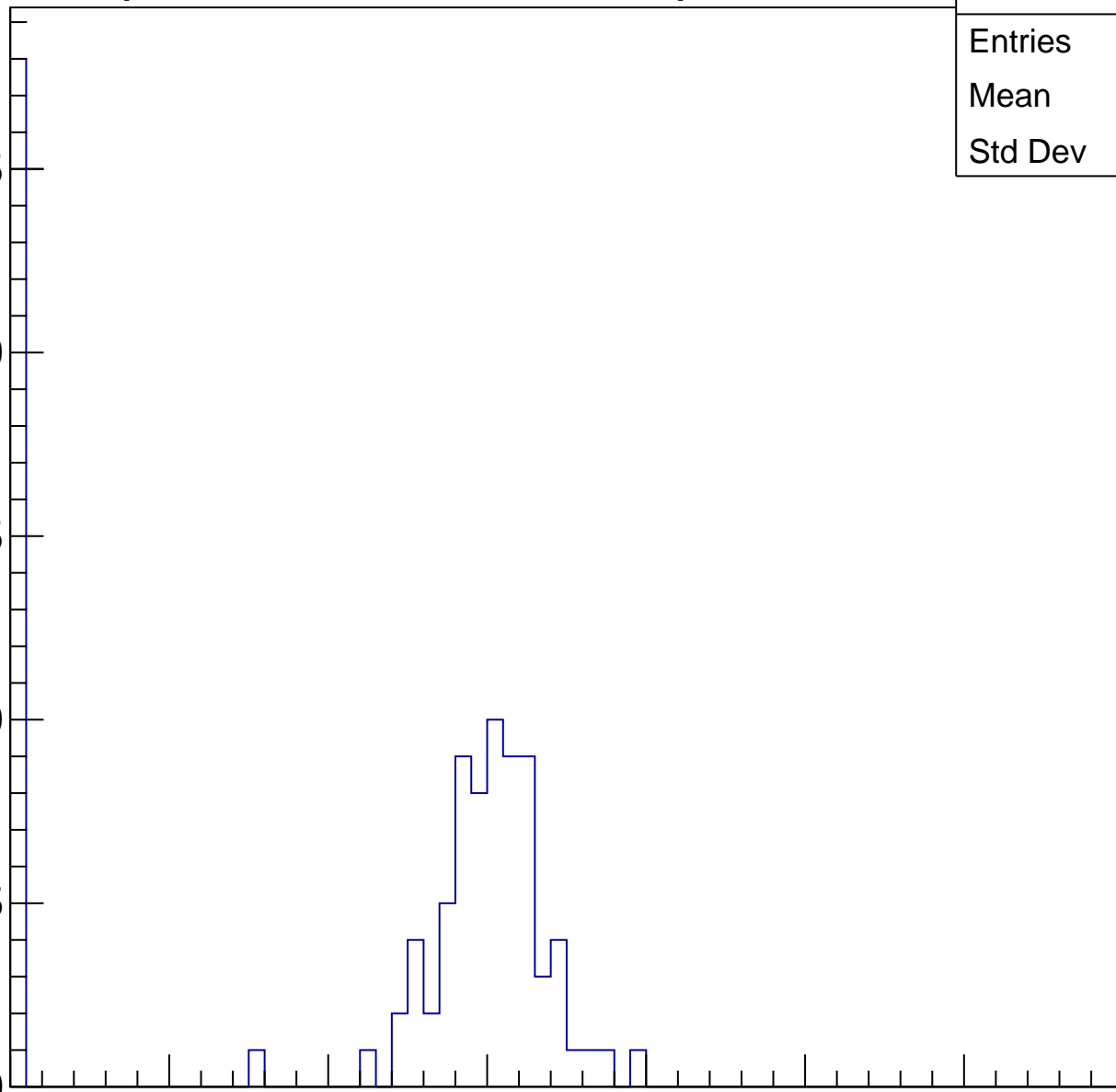
40

50

60

70

ampl

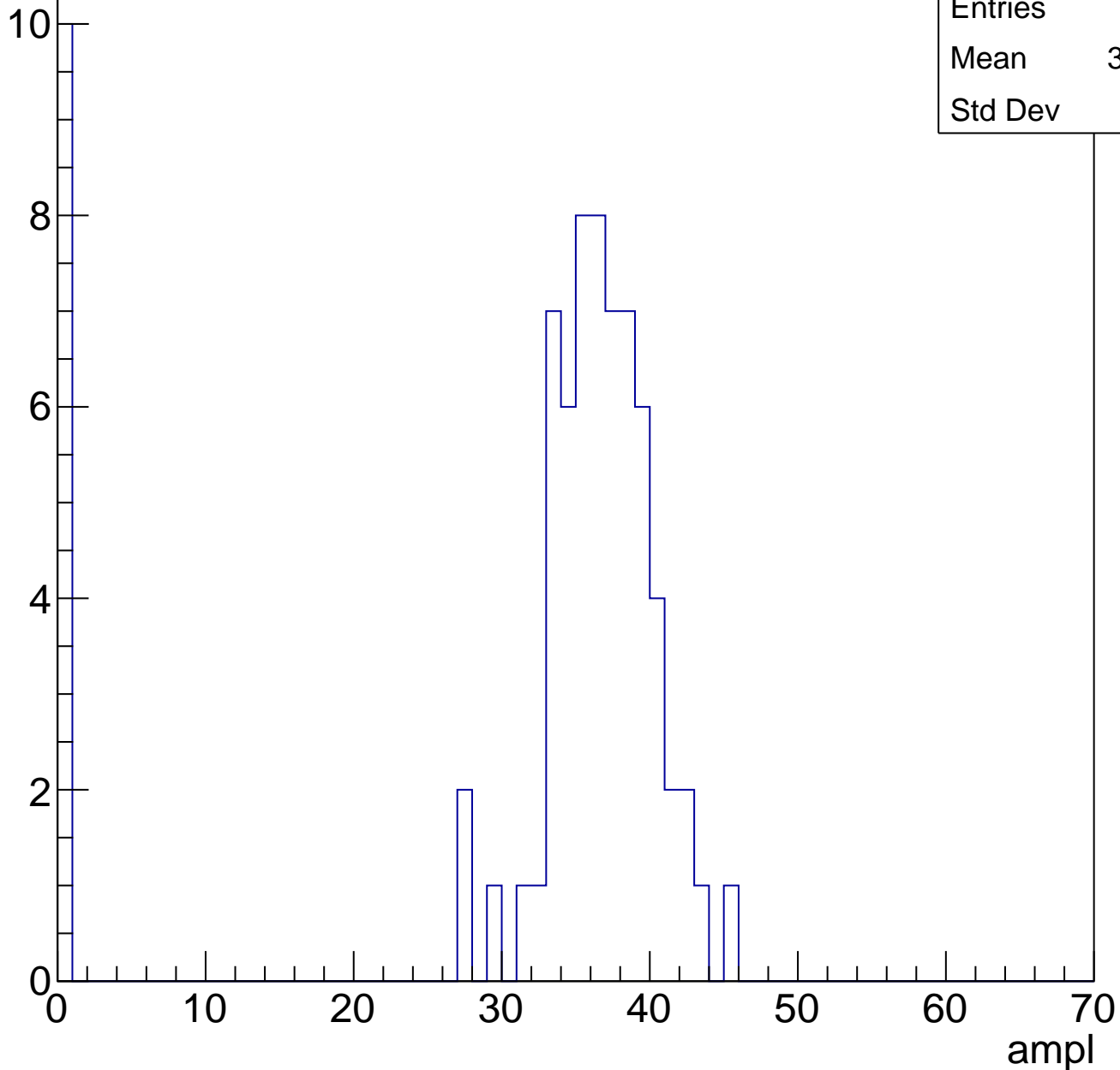


# B1L103S, U4-ch67, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 74    |
| Mean    | 31.38 |
| Std Dev | 12.8  |

Entry

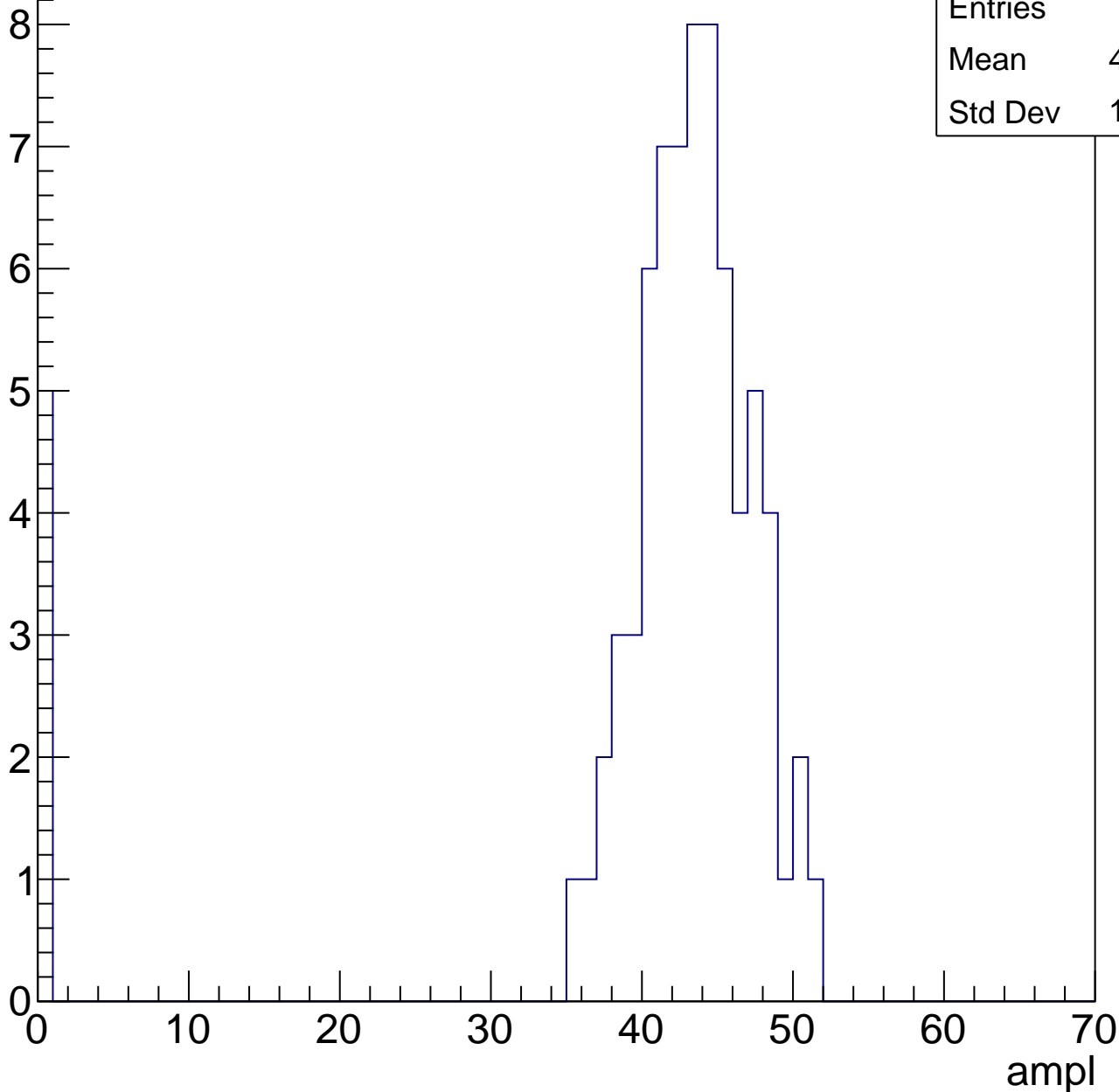


# B1L103S, U4-ch67, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 74    |
| Mean    | 40.19 |
| Std Dev | 11.33 |

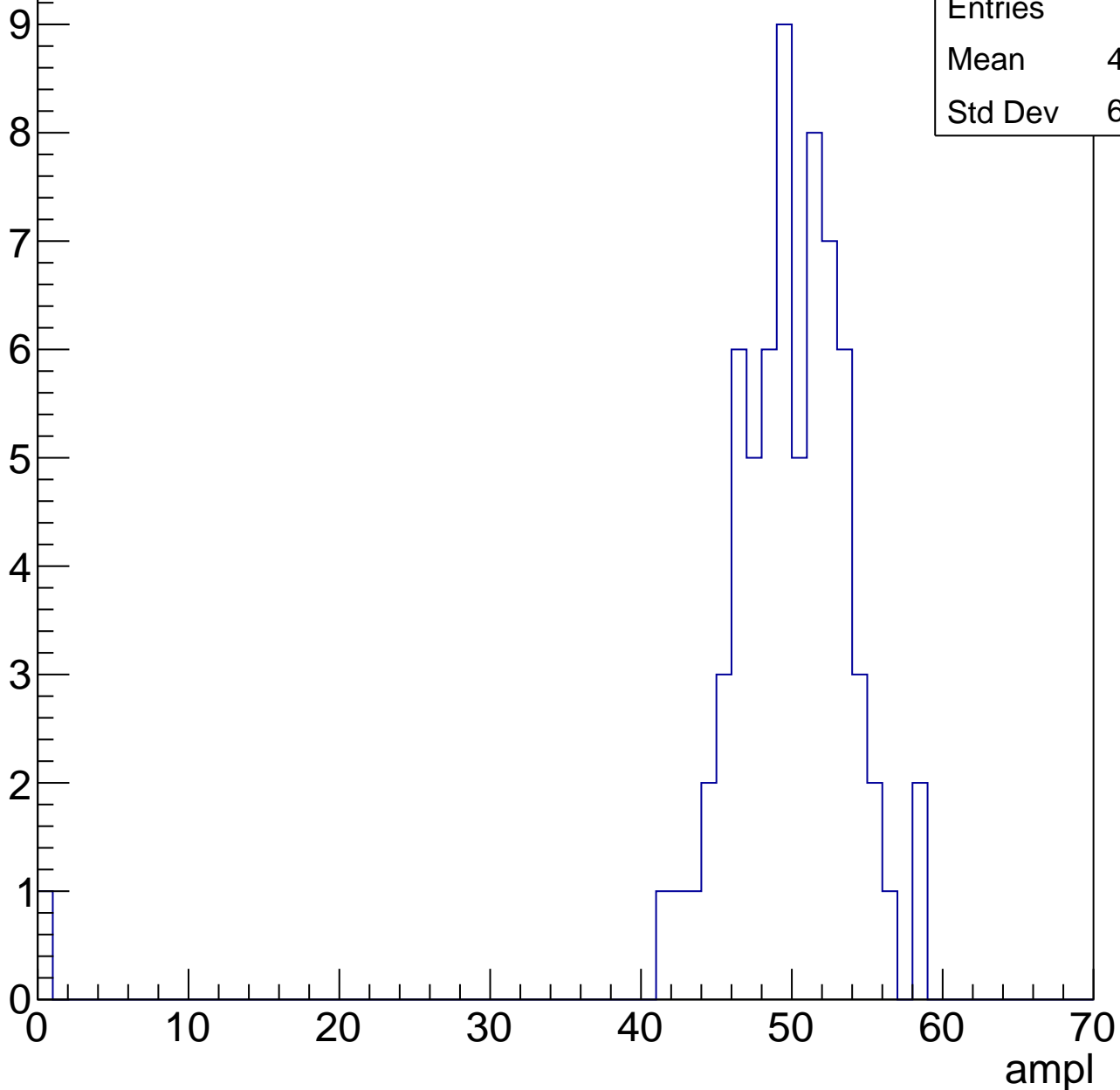


# B1L103S, U4-ch67, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 69    |
| Mean    | 48.88 |
| Std Dev | 6.896 |

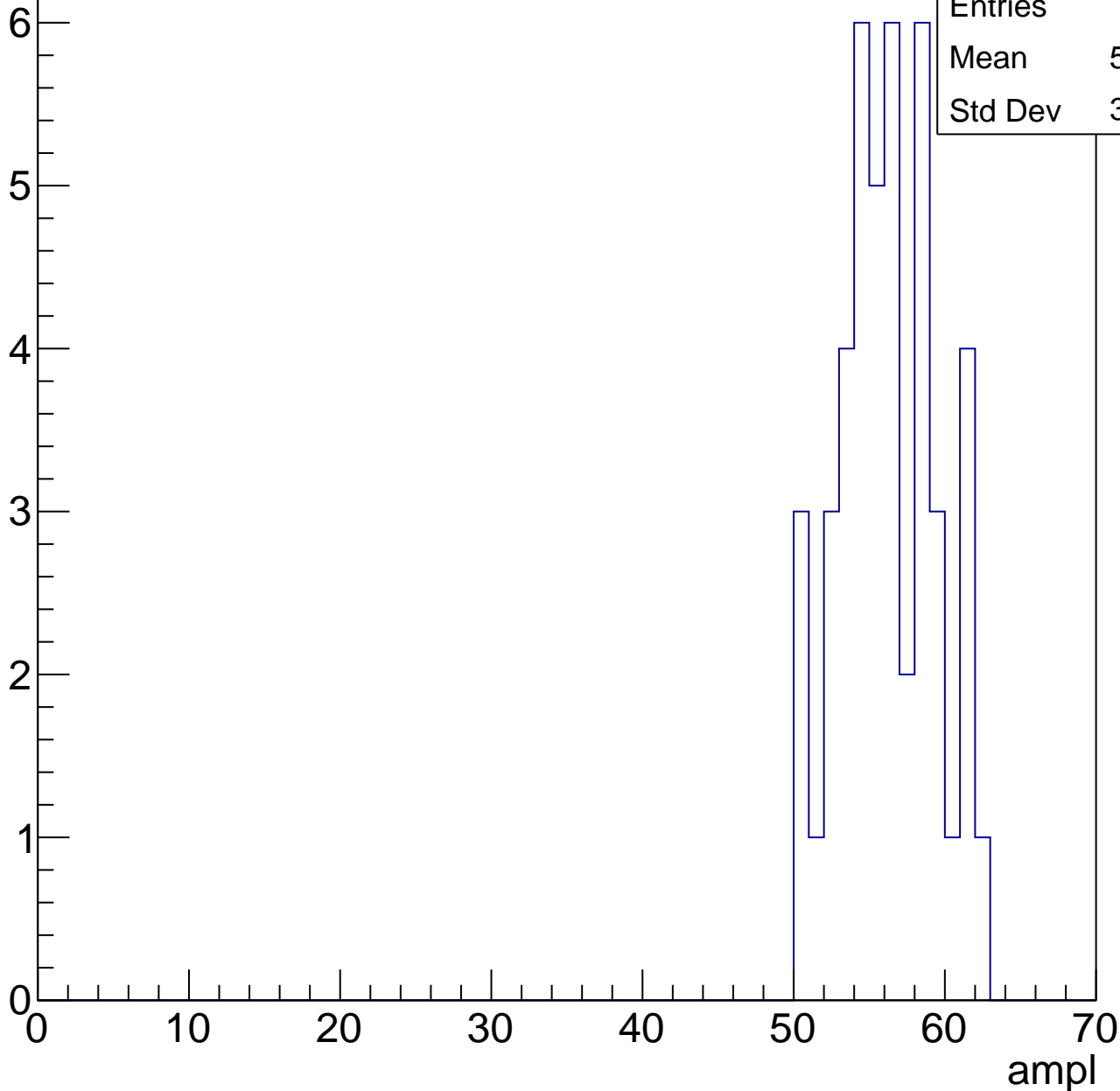


# B1L103S, U4-ch67, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

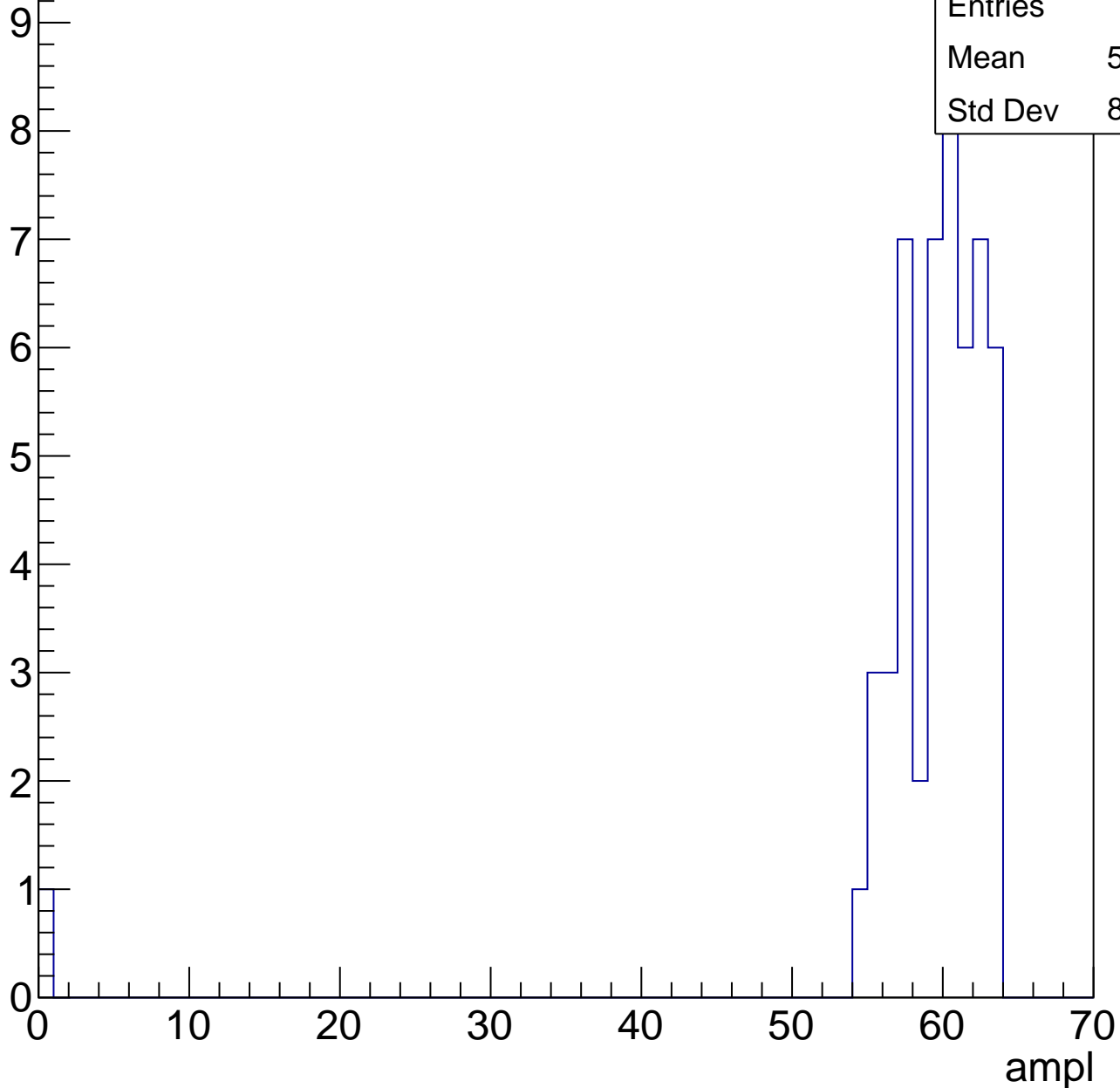
|         |       |
|---------|-------|
| Entries | 45    |
| Mean    | 55.76 |
| Std Dev | 3.156 |



# B1L103S, U4-ch67, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

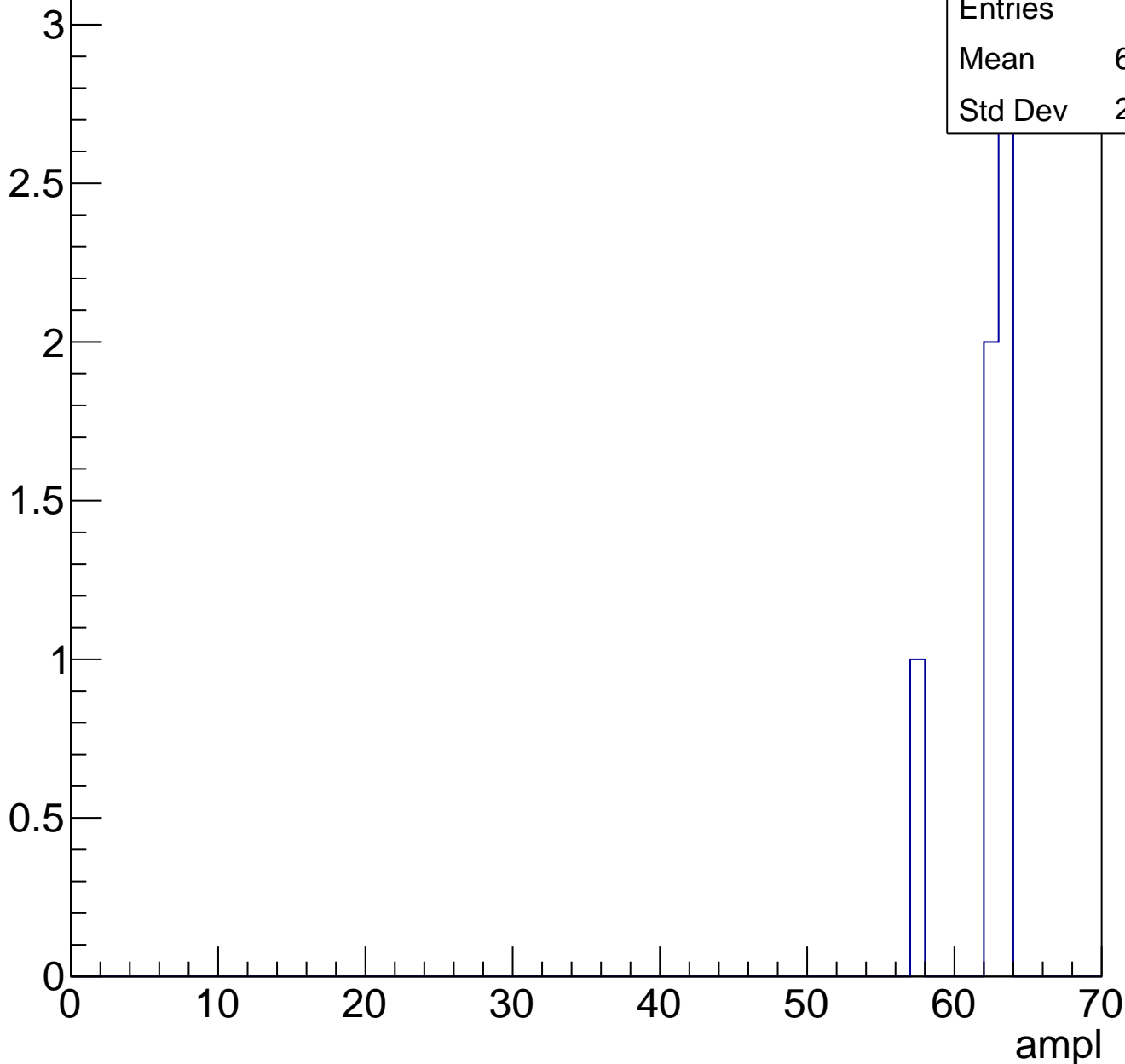


|         |       |
|---------|-------|
| Entries | 52    |
| Mean    | 58.33 |
| Std Dev | 8.525 |

# B1L103S, U4-ch67, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U4-ch67, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 20    |
| Mean    | 3.15  |
| Std Dev | 13.73 |

Entry



# B1L103S, U4-ch68, adc0

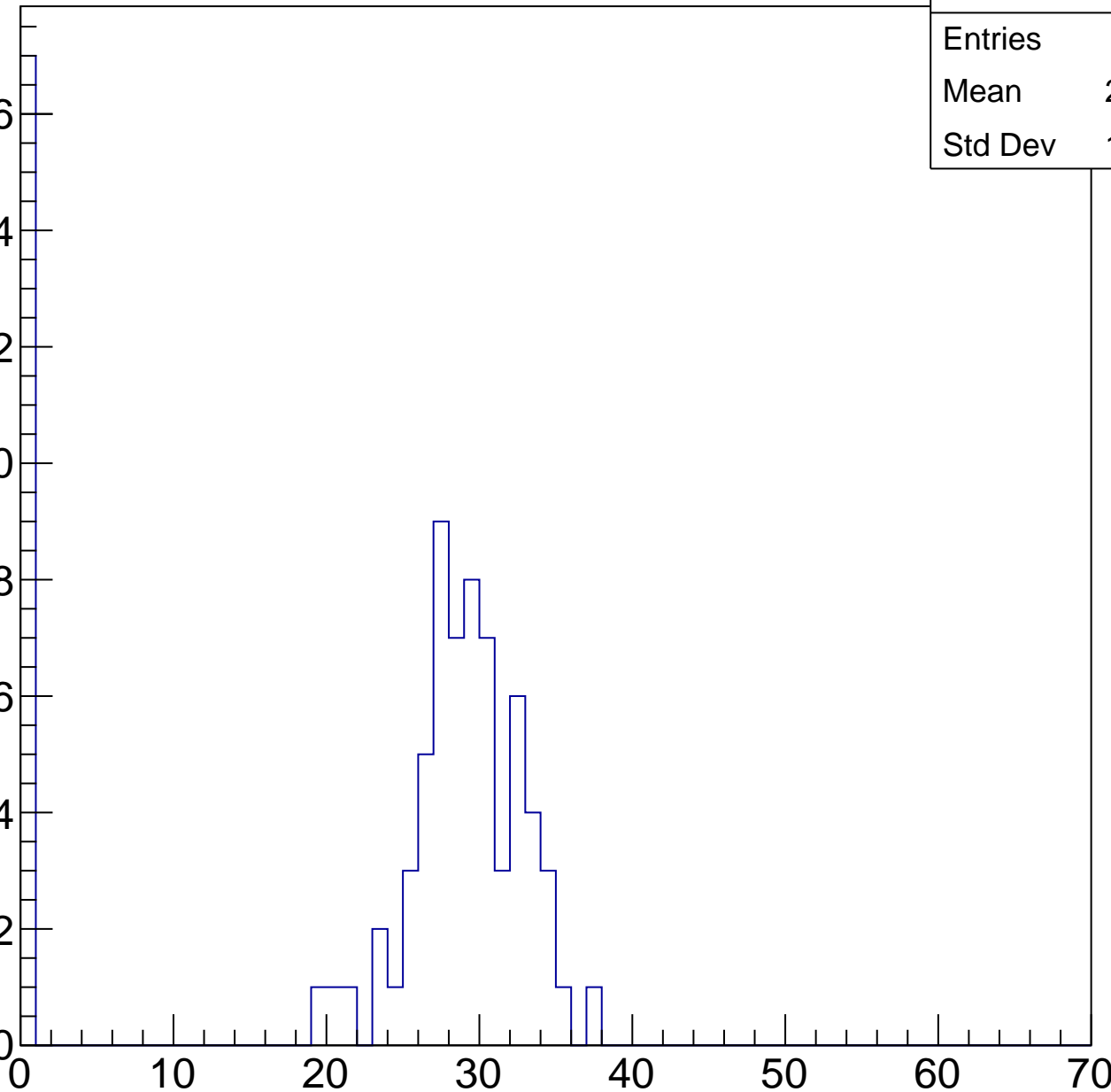
calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 80    |
| Mean    | 22.59 |
| Std Dev | 12.14 |

Entry

16  
14  
12  
10  
8  
6  
4  
2  
0

ampl

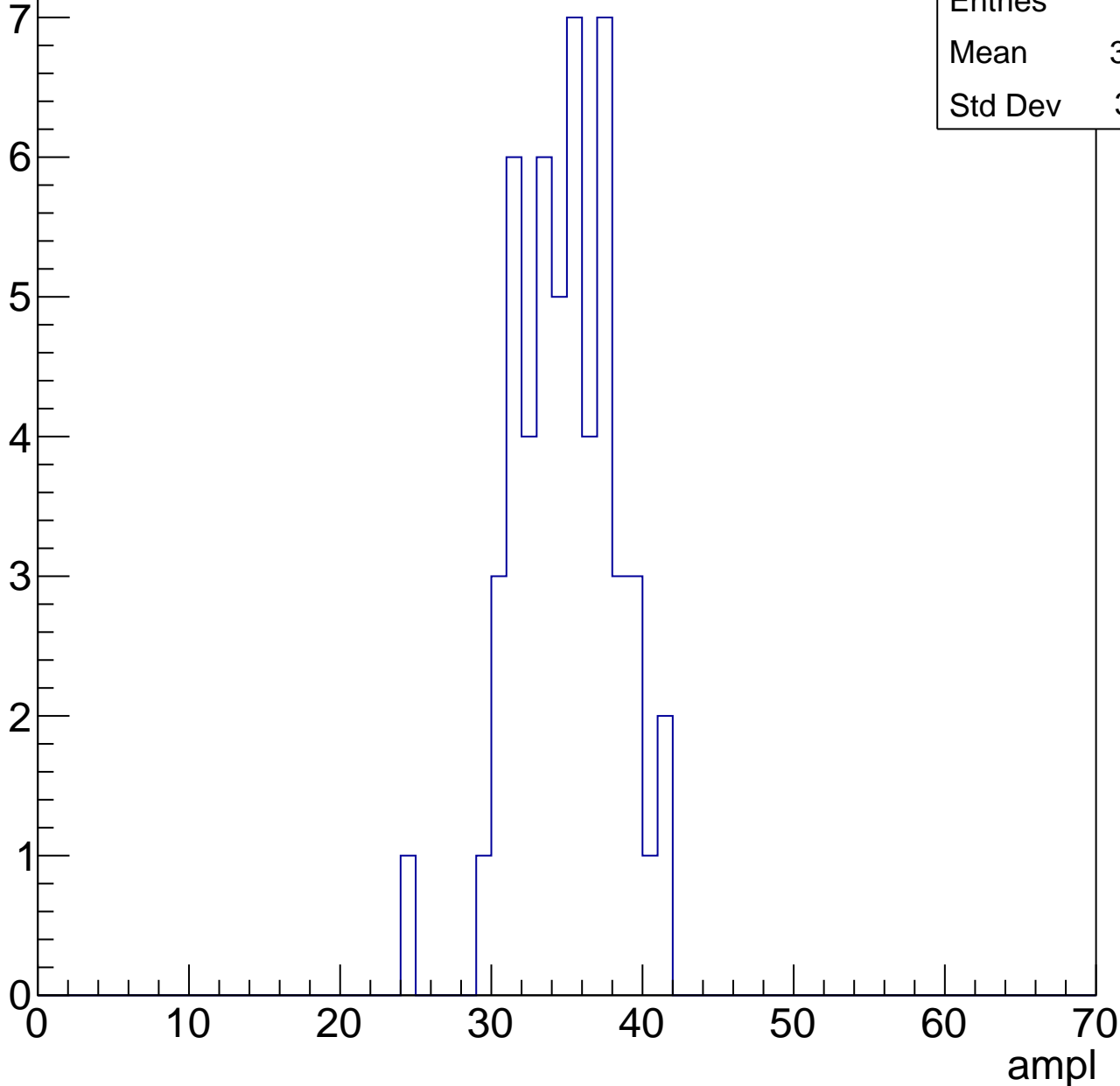


# B1L103S, U4-ch68, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

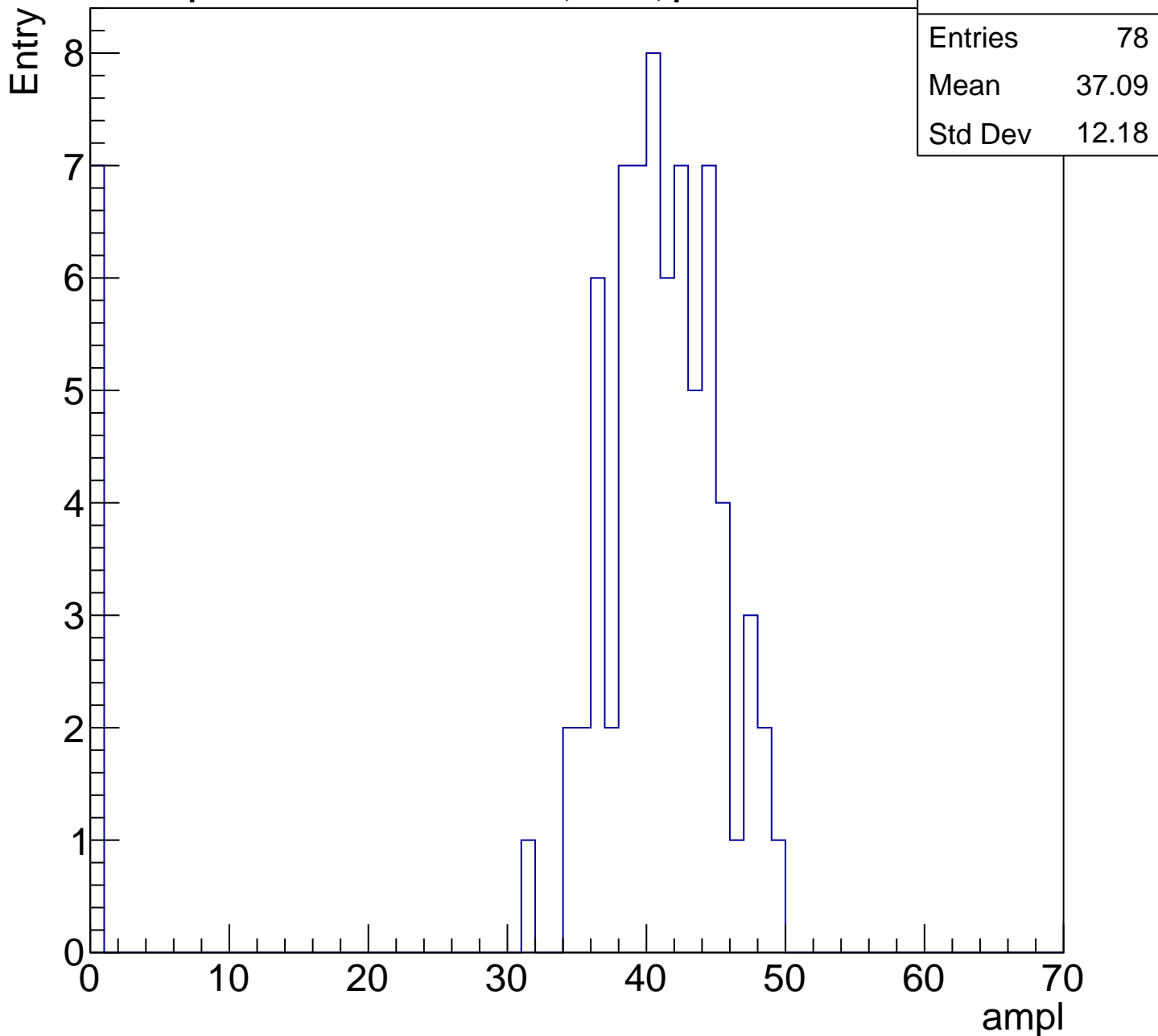
Entry

|         |       |
|---------|-------|
| Entries | 53    |
| Mean    | 34.45 |
| Std Dev | 3.311 |



# B1L103S, U4-ch68, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

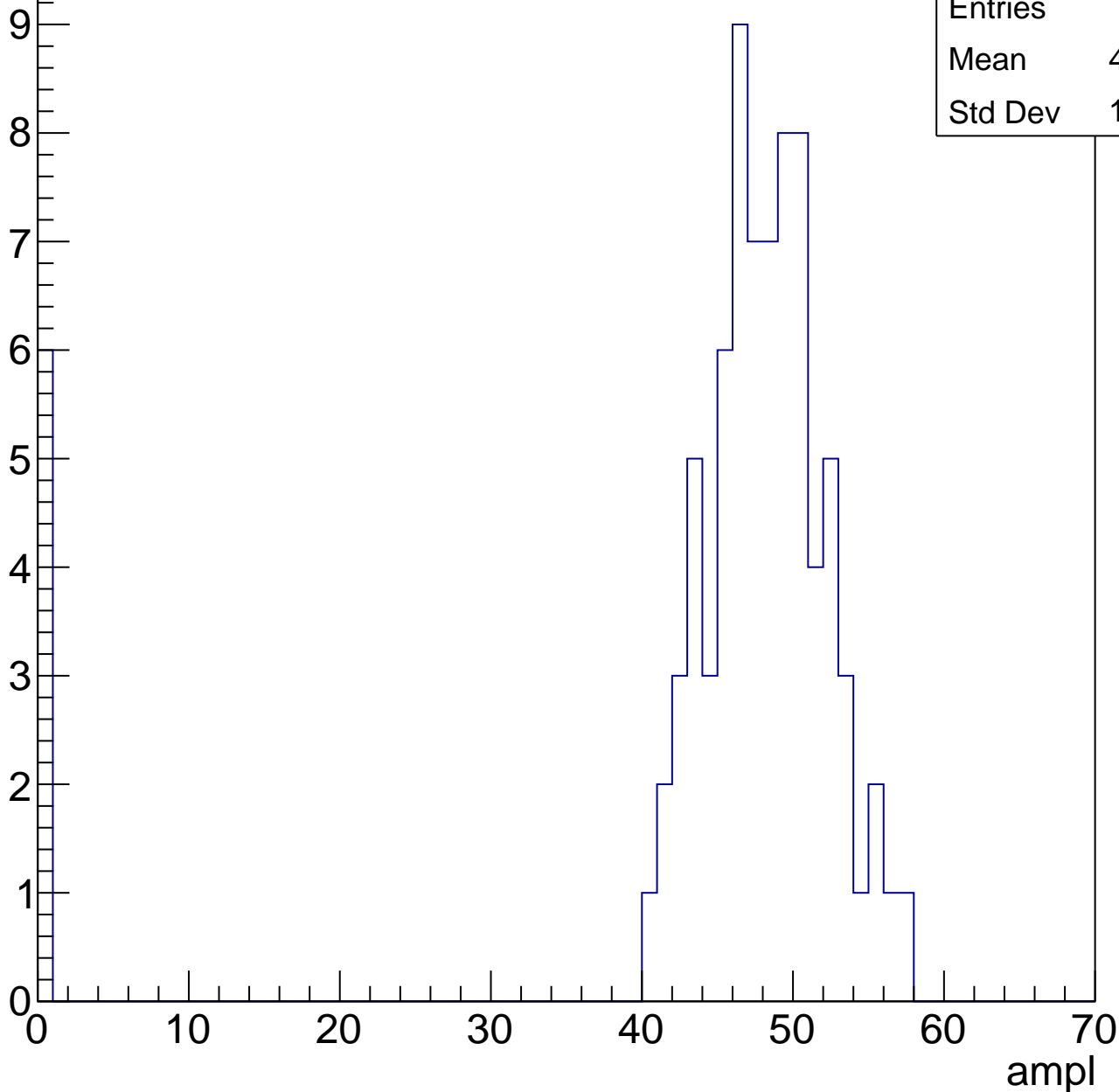


# B1L103S, U4-ch68, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

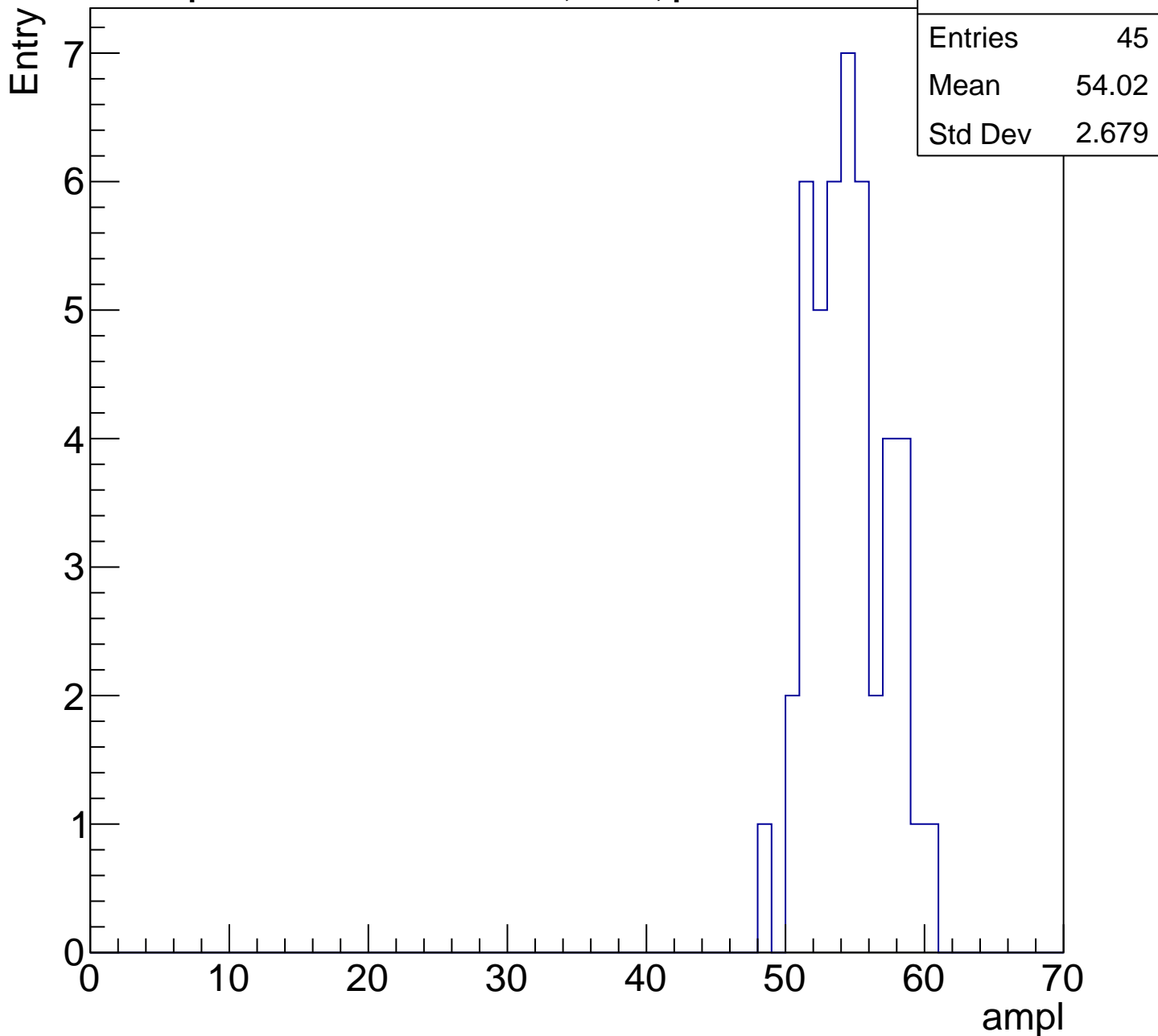
Entry

|         |       |
|---------|-------|
| Entries | 82    |
| Mean    | 44.34 |
| Std Dev | 12.96 |



# B1L103S, U4-ch68, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

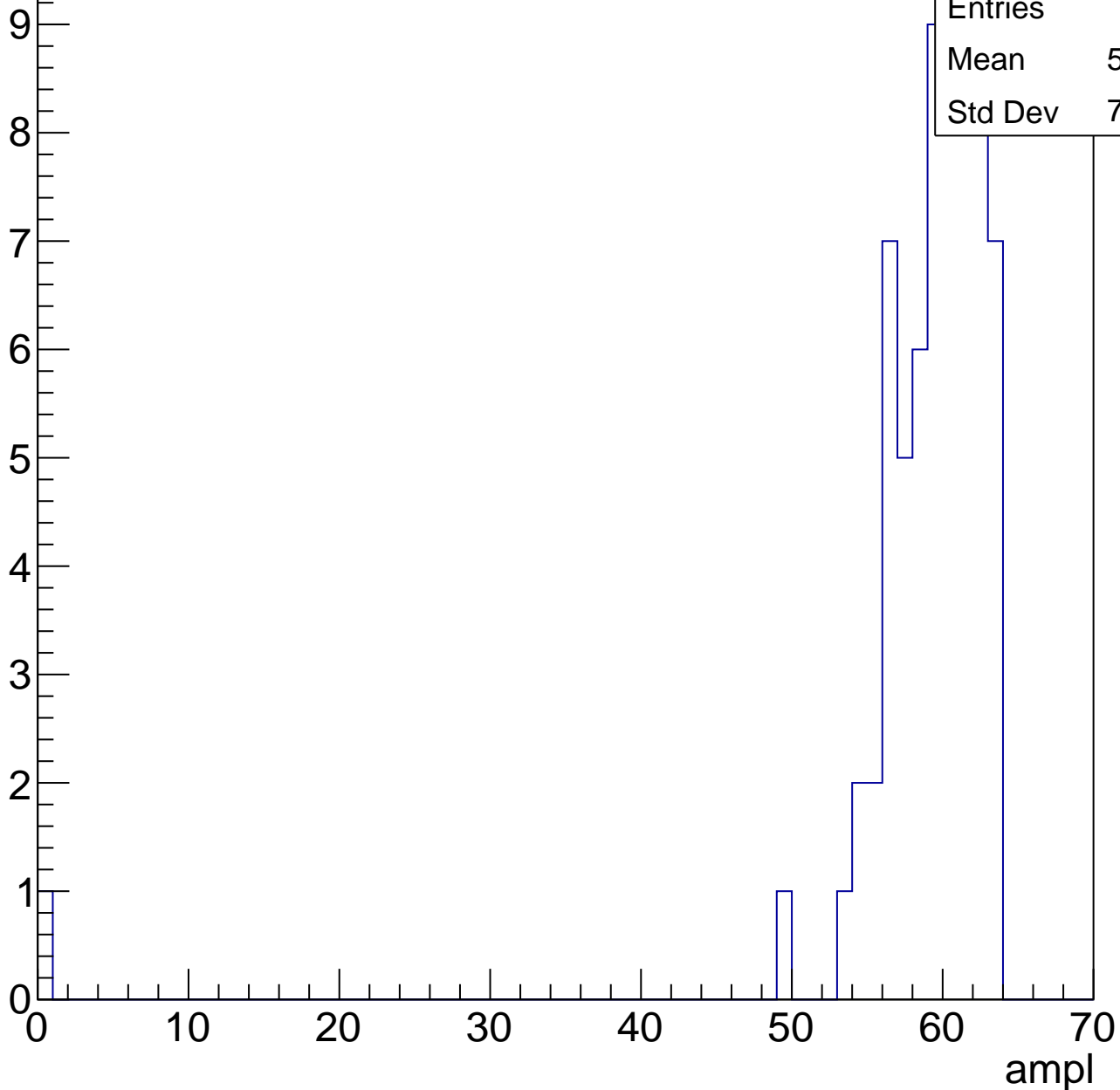


# B1L103S, U4-ch68, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

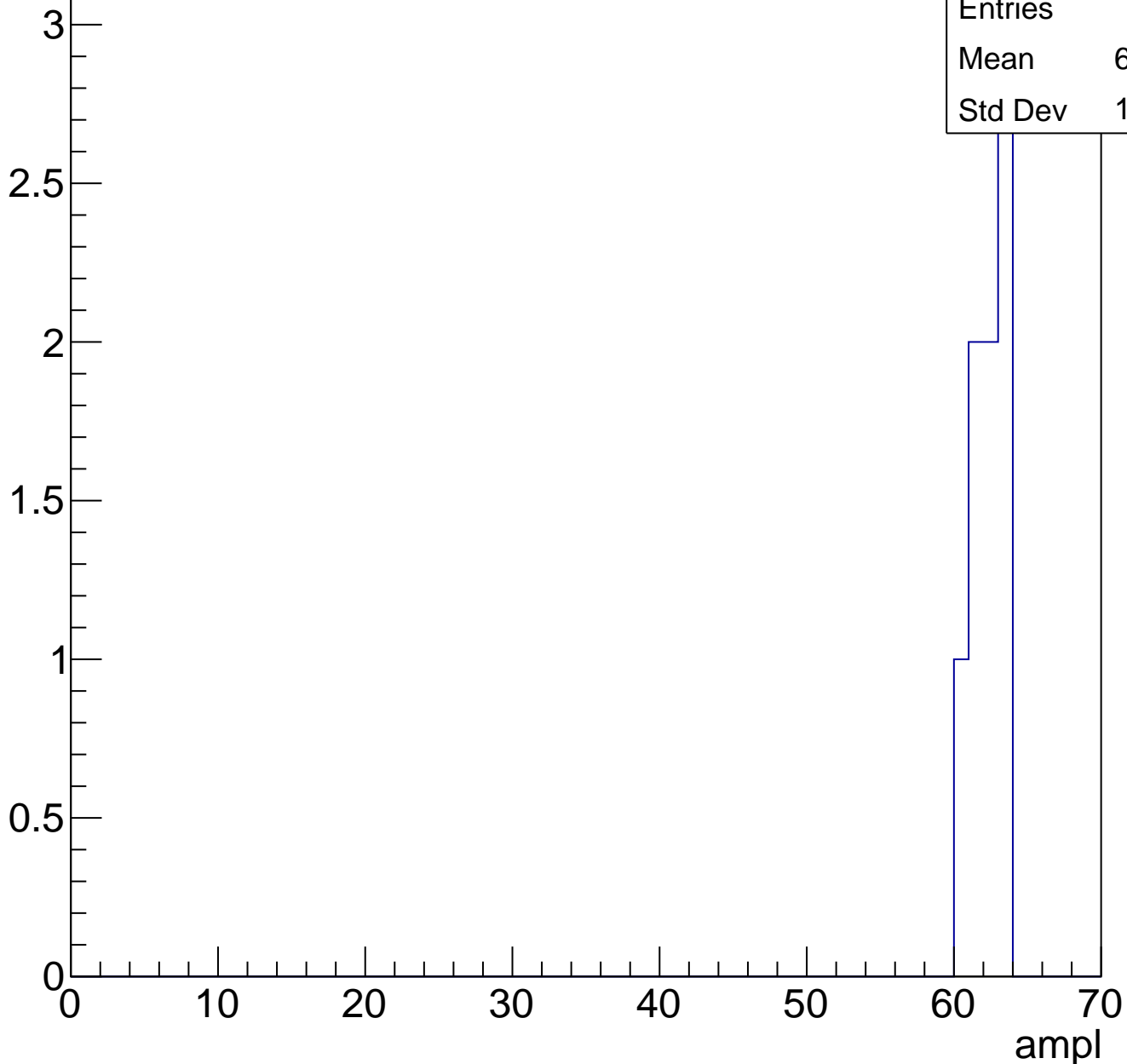
|         |       |
|---------|-------|
| Entries | 65    |
| Mean    | 58.17 |
| Std Dev | 7.812 |



# B1L103S, U4-ch68, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U4-ch68, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

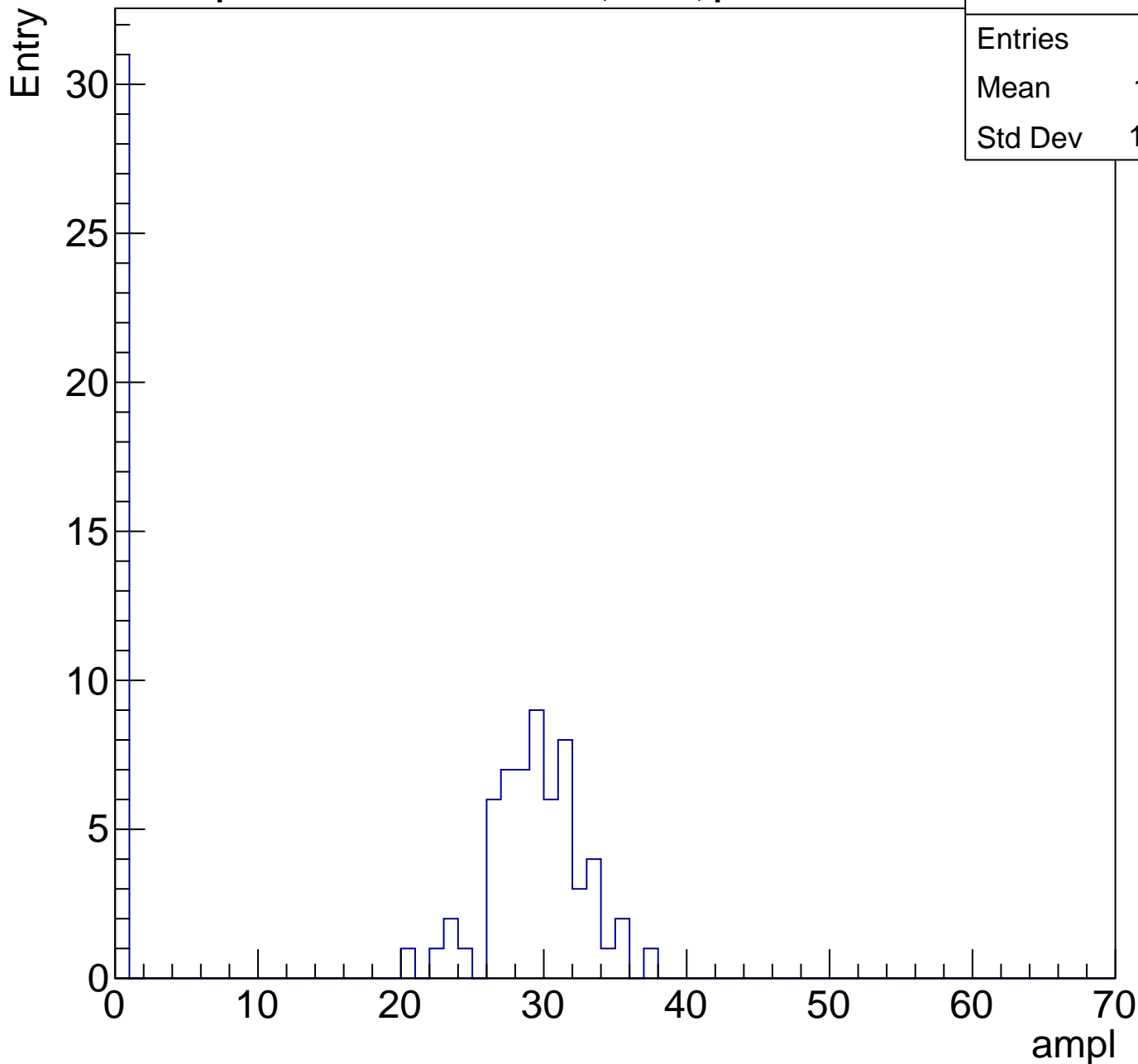
Entry



# B1L103S, U4-ch69, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 90    |
| Mean    | 19.01 |
| Std Dev | 14.02 |



# B1L103S, U4-ch69, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 93    |
| Mean    | 35.06 |
| Std Dev | 7.389 |

Entry

10

8

6

4

2

0

ampl

0

10

20

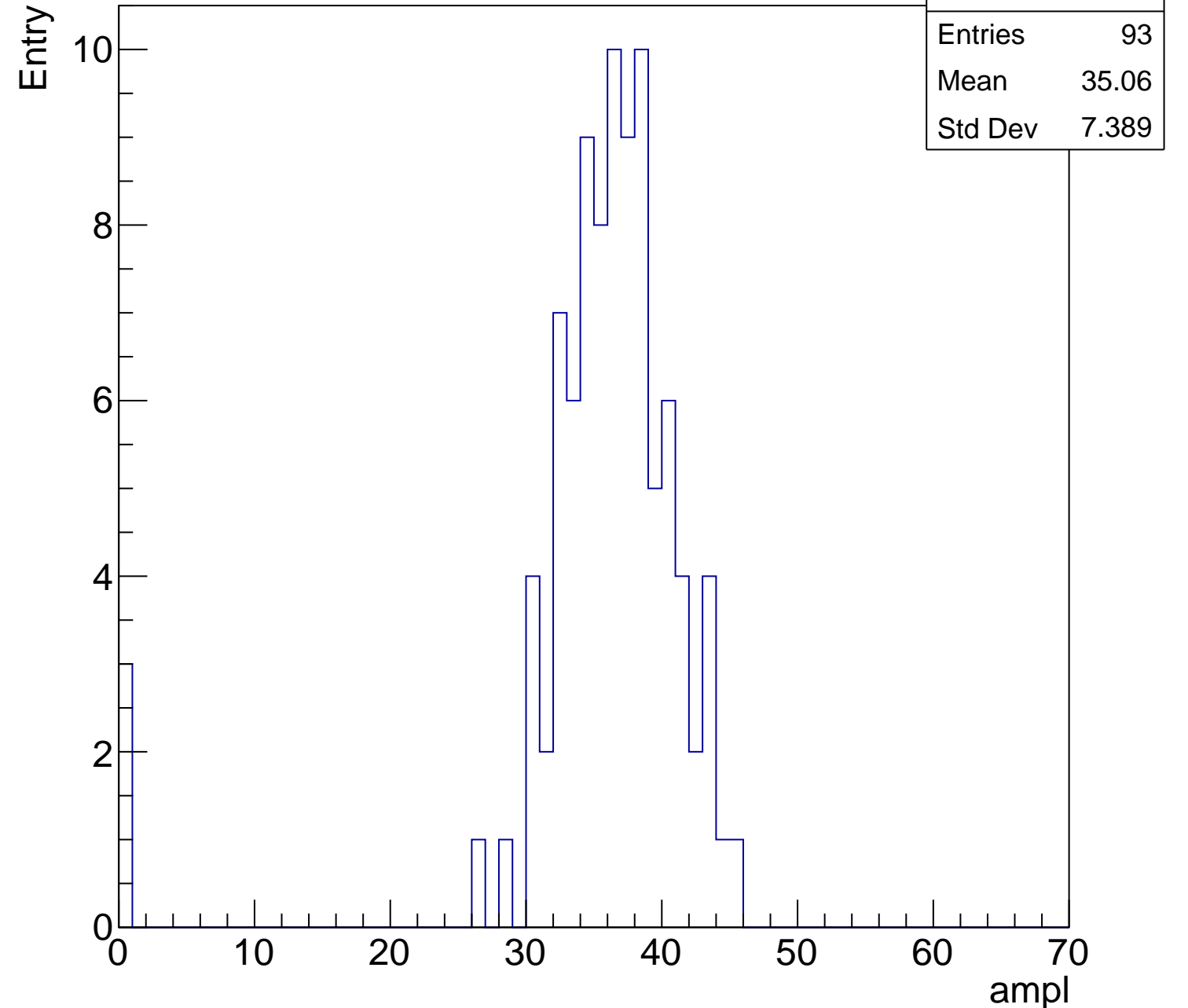
30

40

50

60

70



# B1L103S, U4-ch69, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 68    |
| Mean    | 36.68 |
| Std Dev | 16.35 |

Entry

10

8

6

4

2

0

0

10

20

30

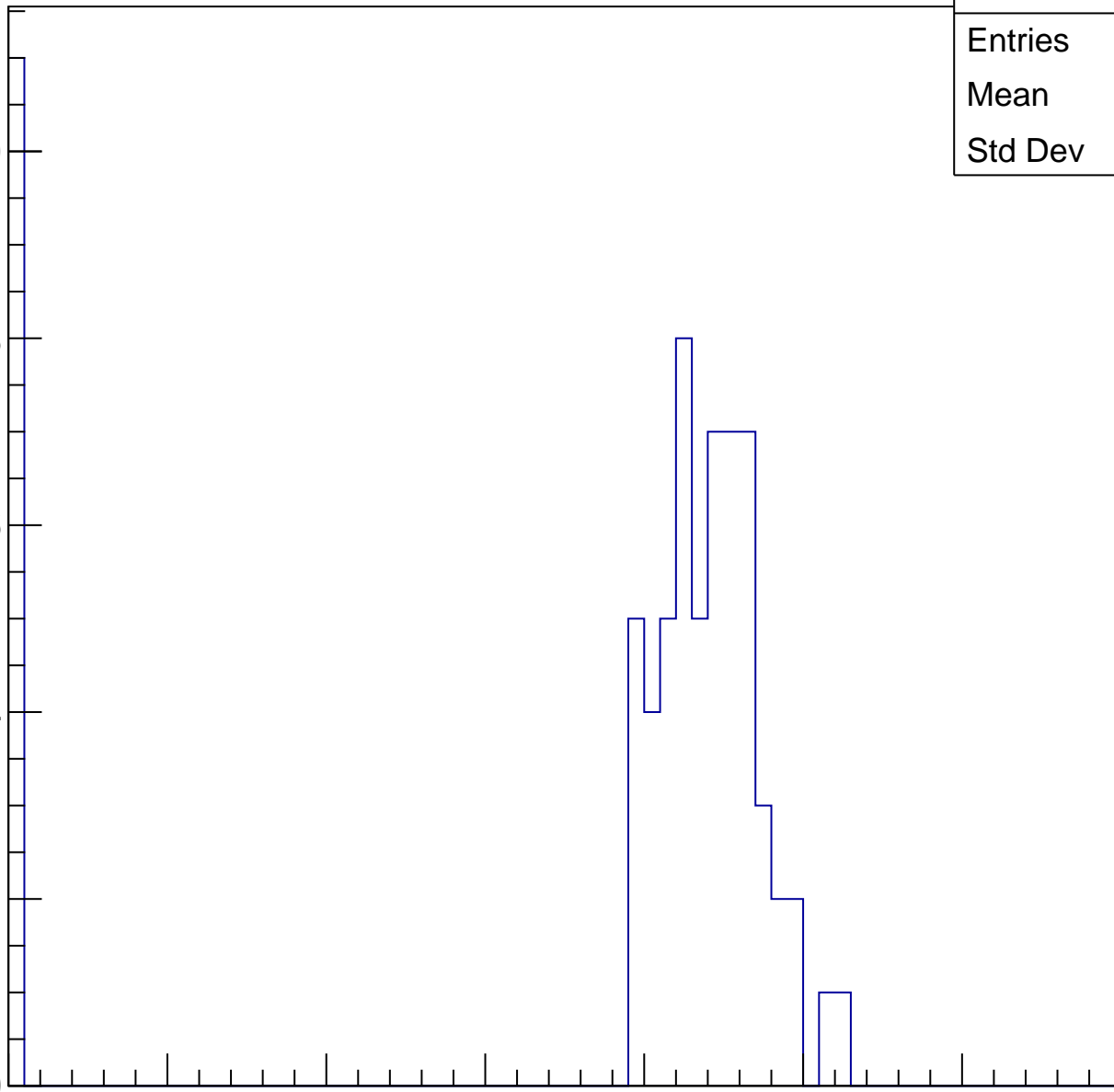
40

50

60

70

ampl



# B1L103S, U4-ch69, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

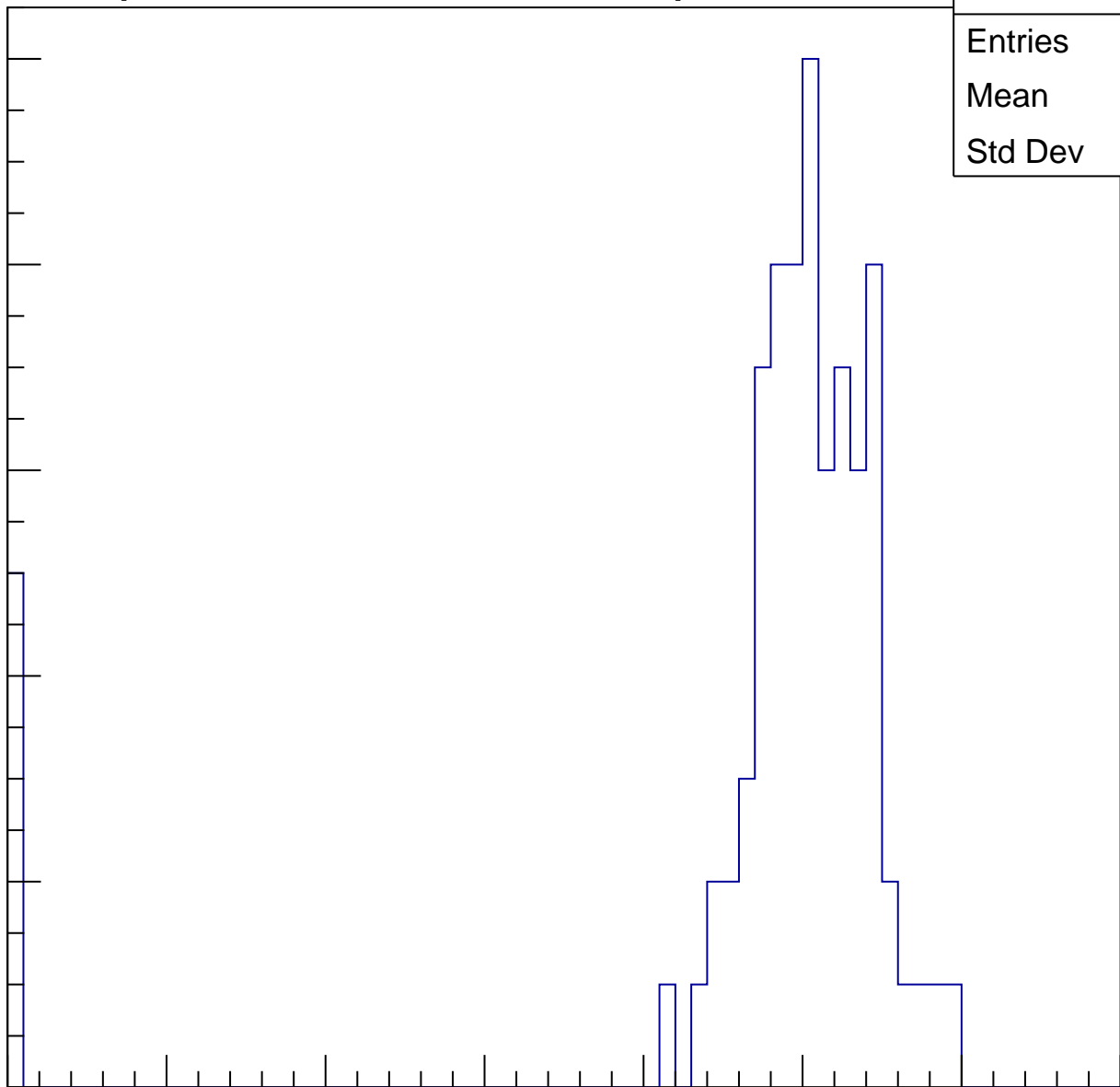
|         |       |
|---------|-------|
| Entries | 80    |
| Mean    | 47.06 |
| Std Dev | 12.6  |

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

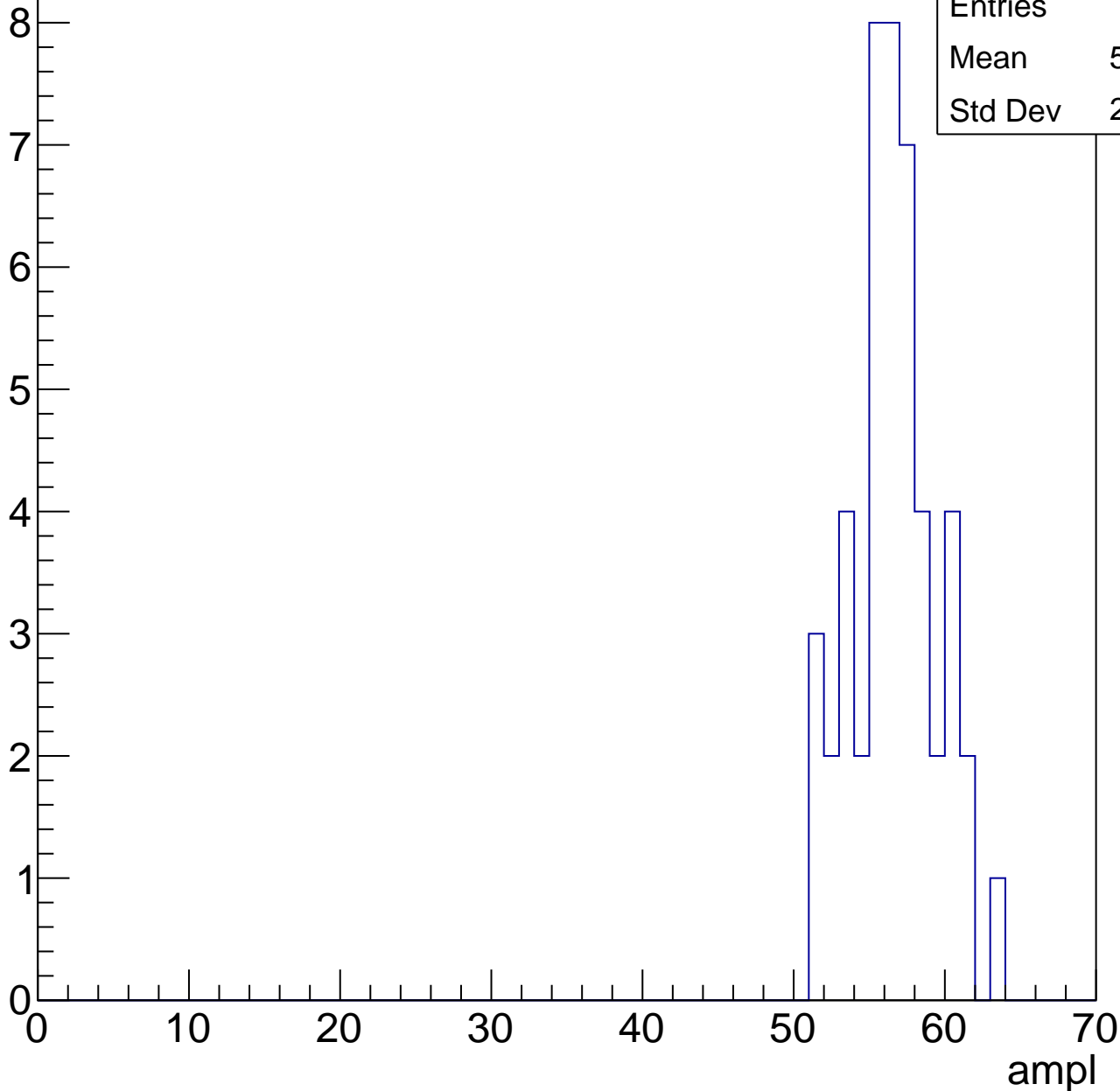


# B1L103S, U4-ch69, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 47    |
| Mean    | 56.15 |
| Std Dev | 2.775 |

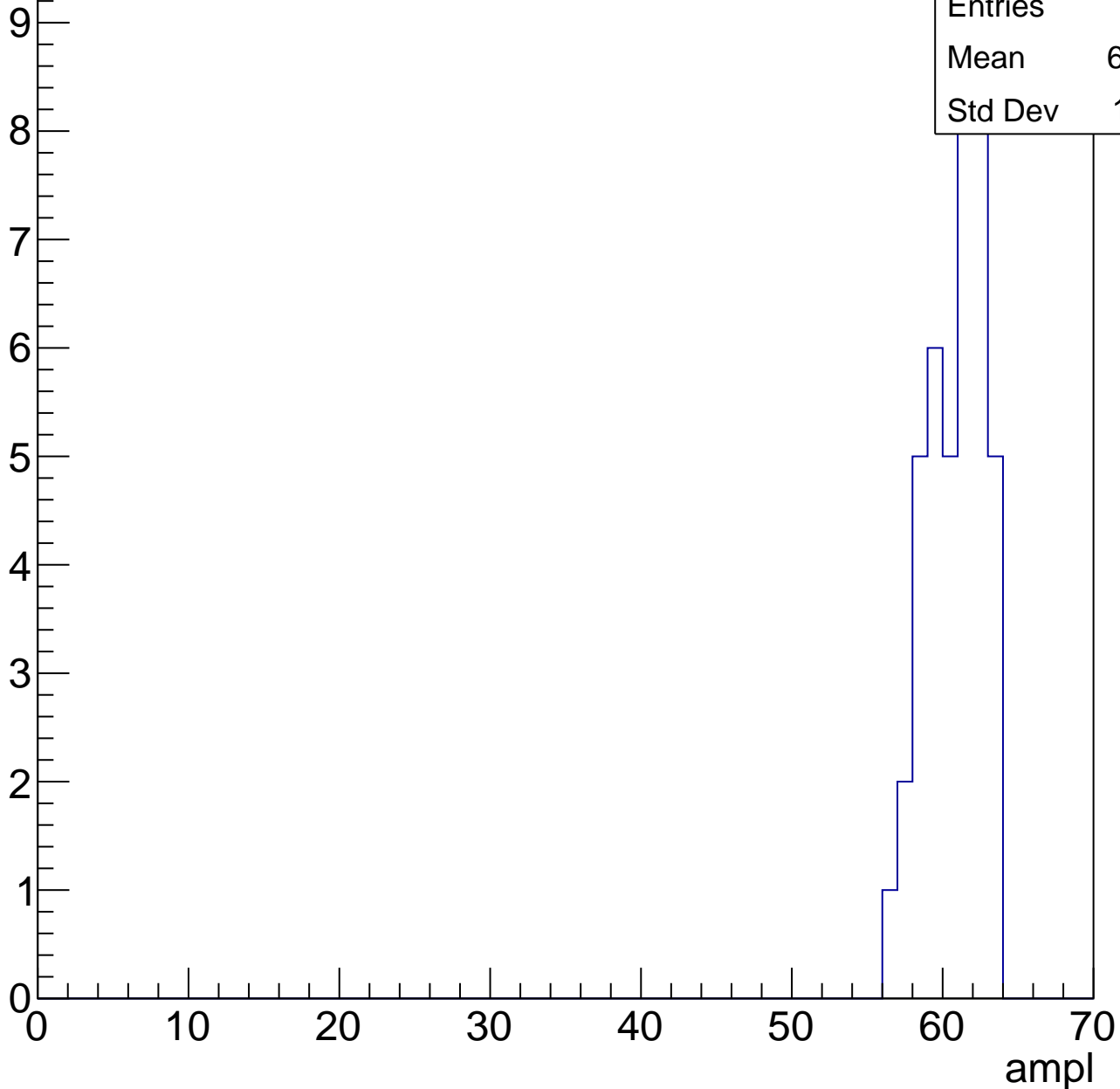


# B1L103S, U4-ch69, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

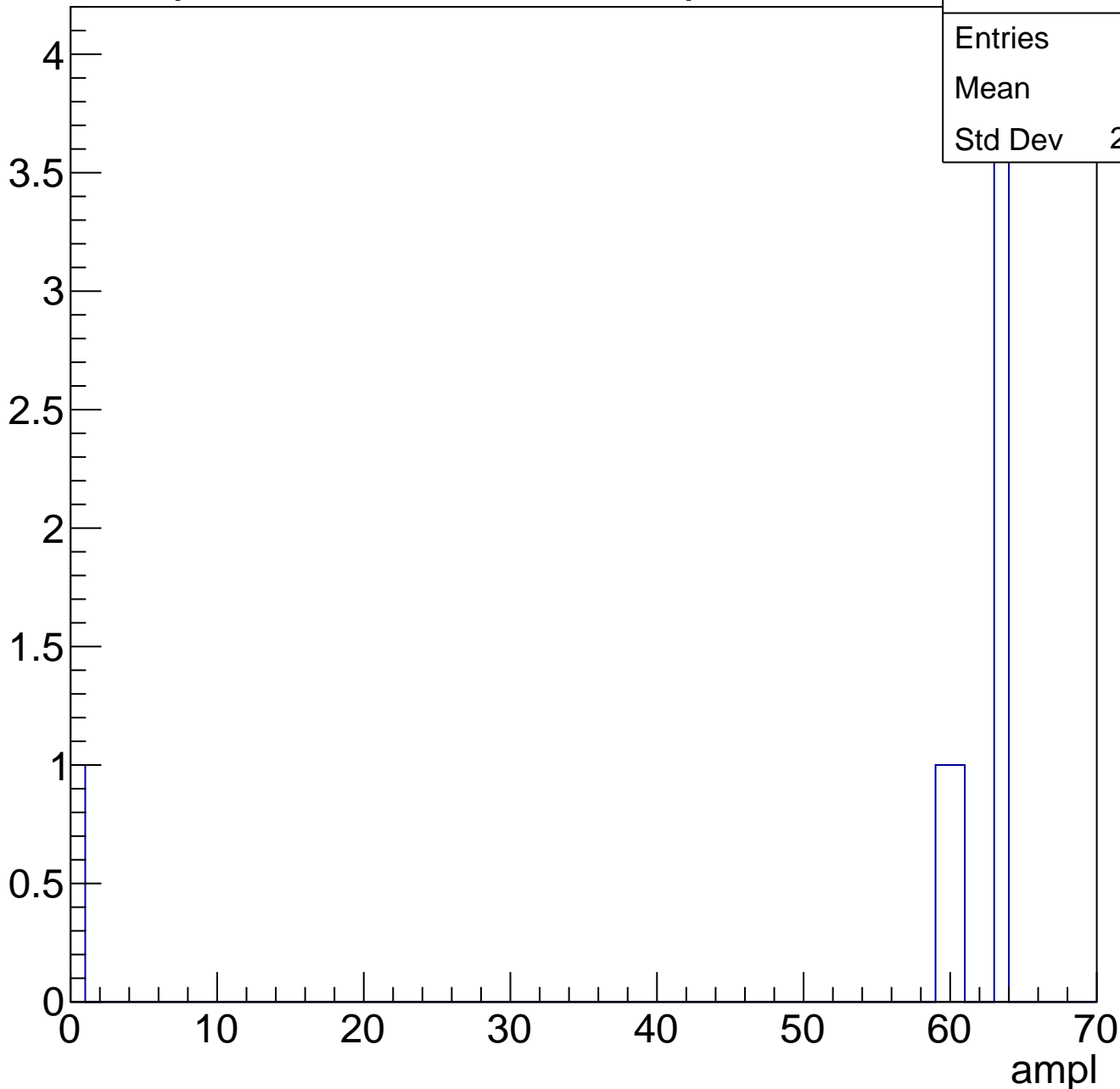
|         |       |
|---------|-------|
| Entries | 41    |
| Mean    | 60.37 |
| Std Dev | 1.871 |



# B1L103S, U4-ch69, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

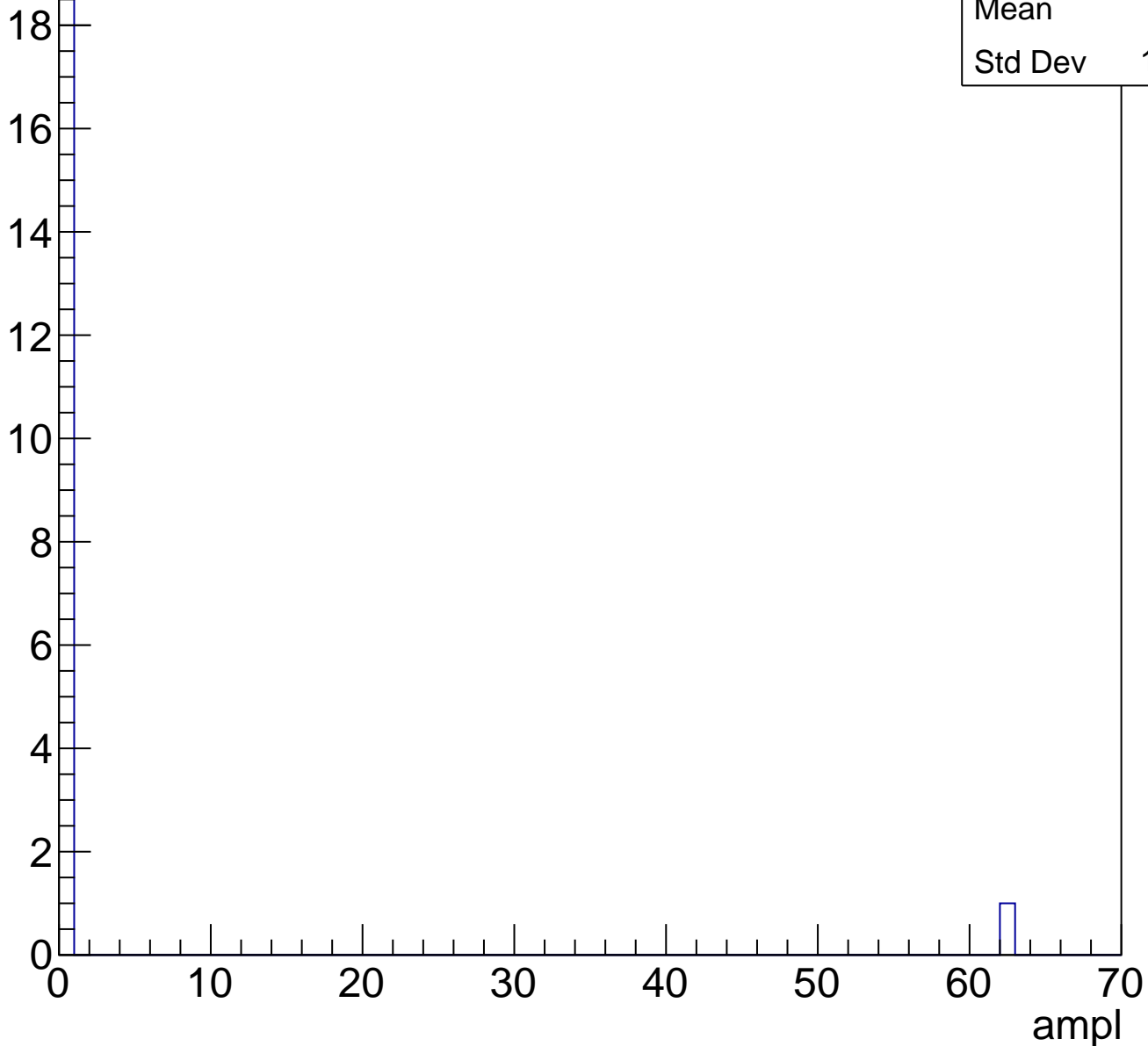




# B1L103S, U4-ch69, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

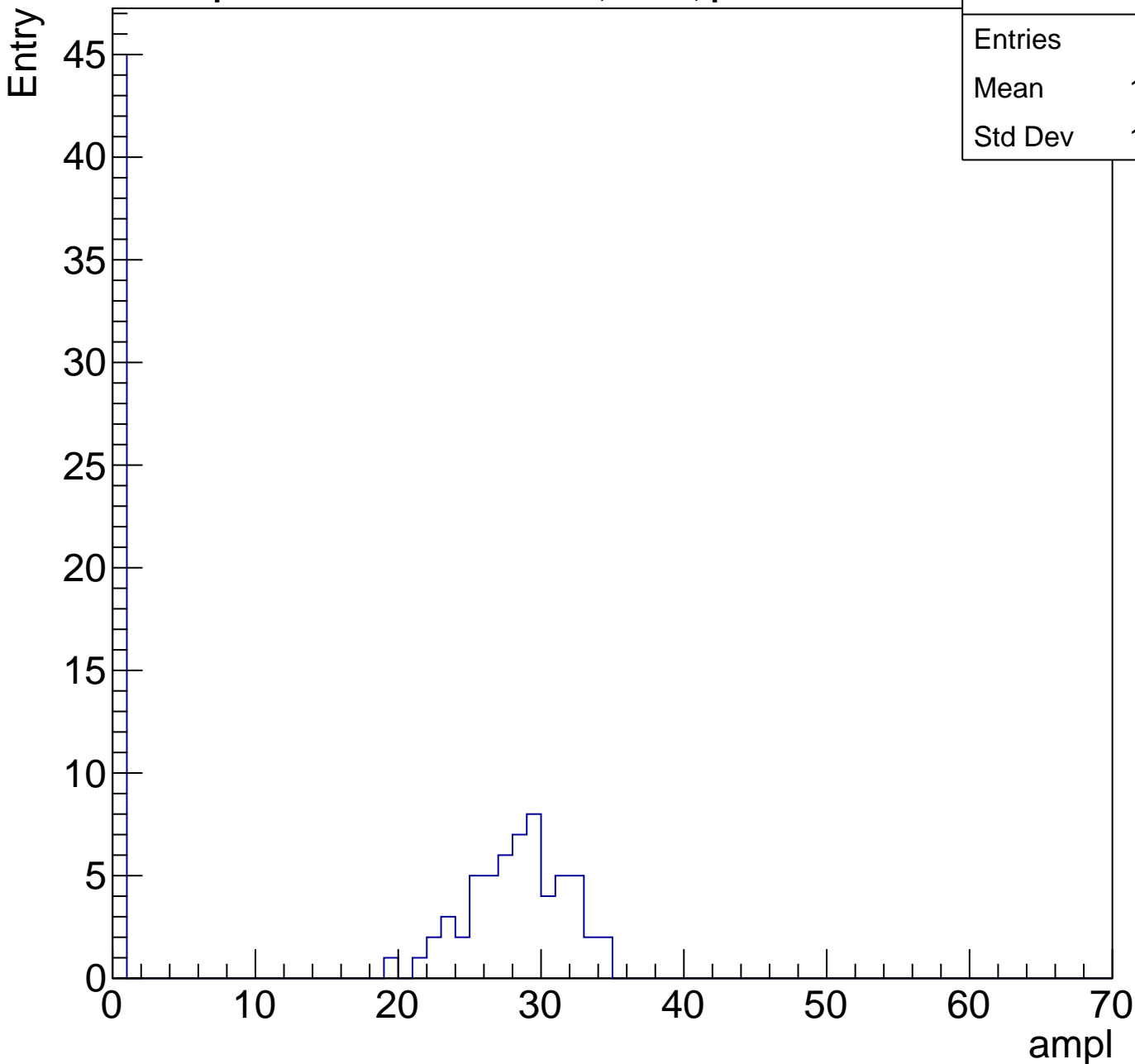


|         |       |
|---------|-------|
| Entries | 20    |
| Mean    | 3.1   |
| Std Dev | 13.51 |

# B1L103S, U4-ch70, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 103   |
| Mean    | 15.68 |
| Std Dev | 14.04 |



# B1L103S, U4-ch70, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 71    |
| Mean    | 27.82 |
| Std Dev | 13.51 |

Entry

12

10

8

6

4

2

0

0

10

20

30

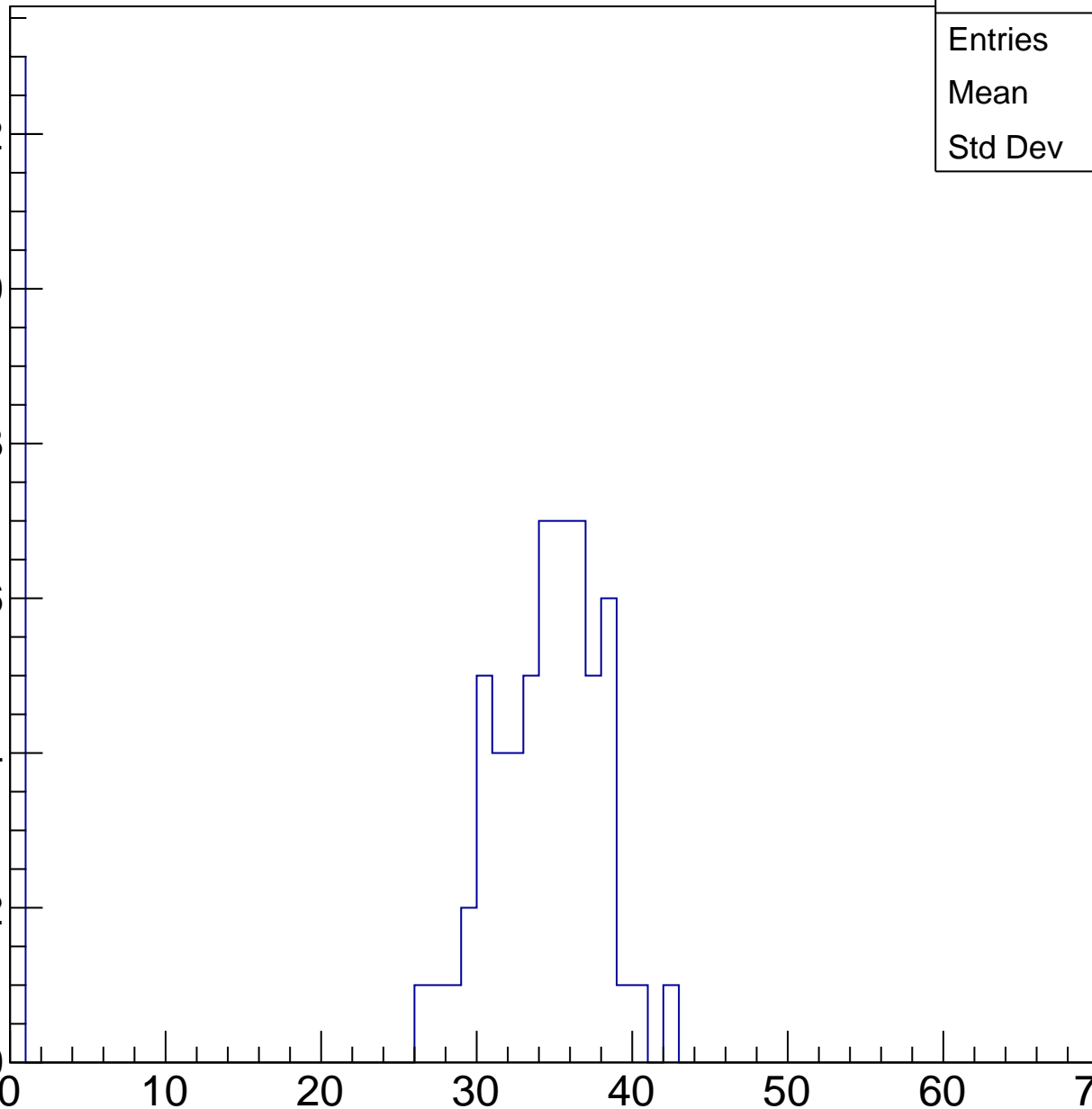
40

50

60

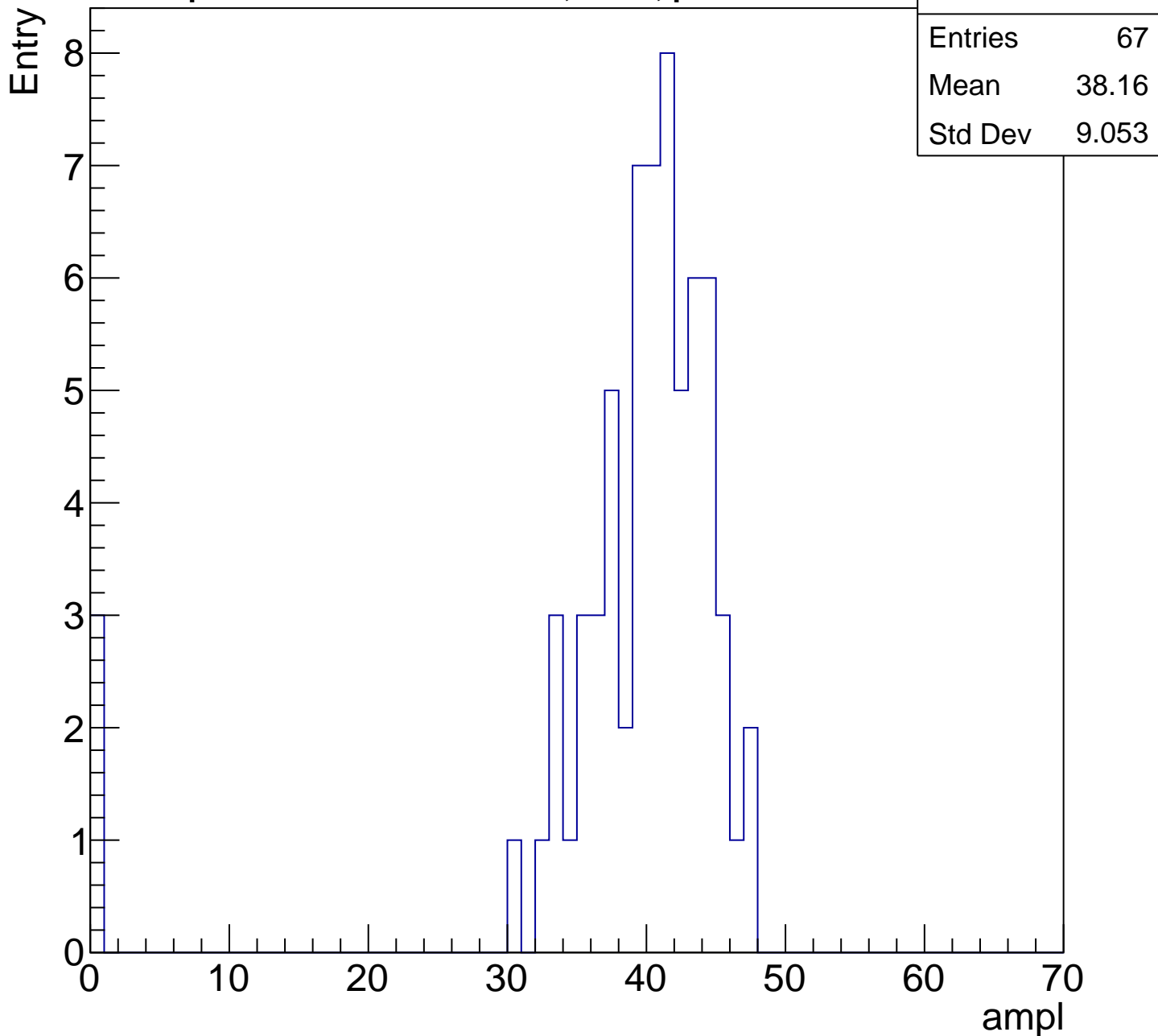
70

ampl



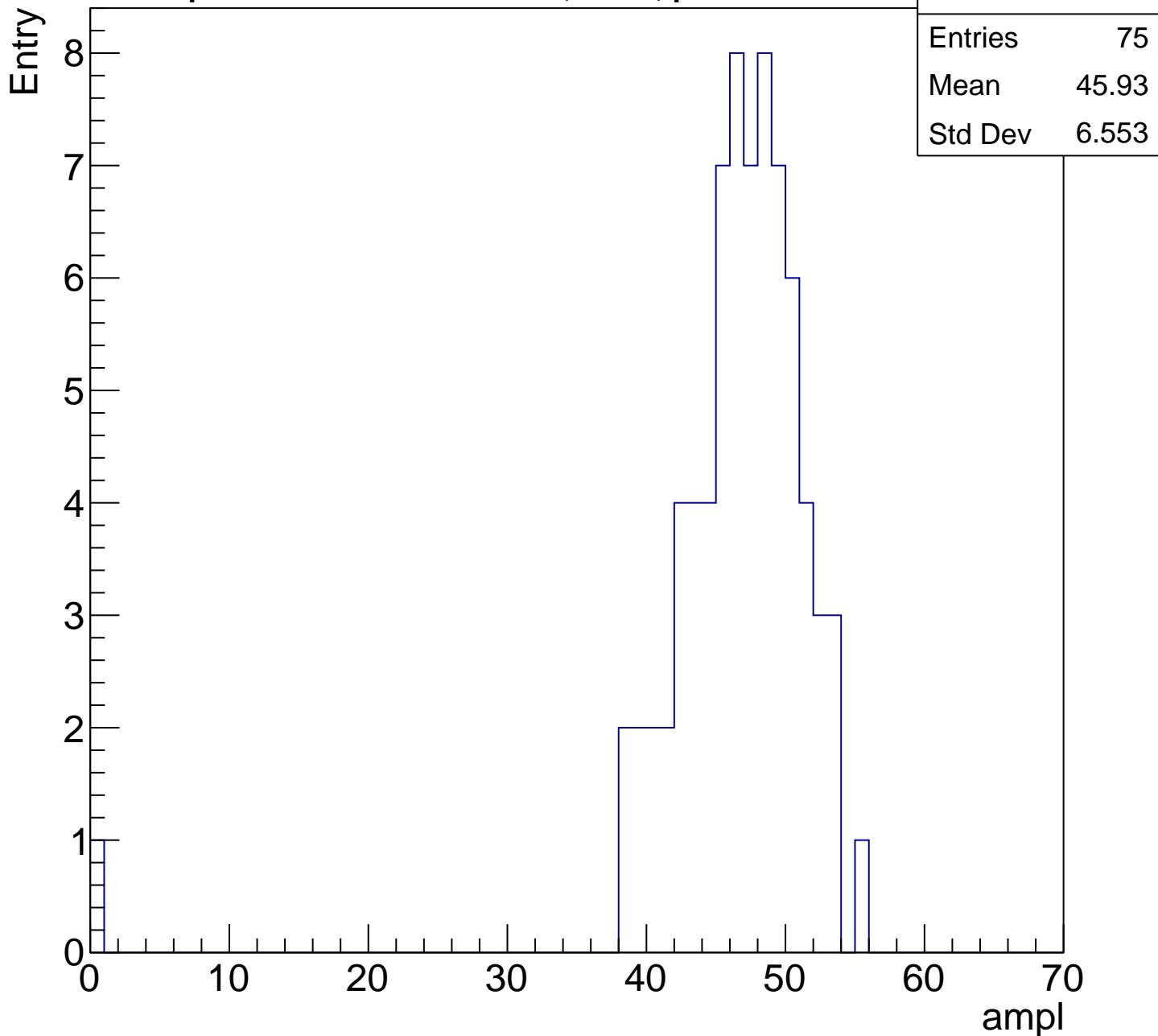
# B1L103S, U4-ch70, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2



# B1L103S, U4-ch70, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

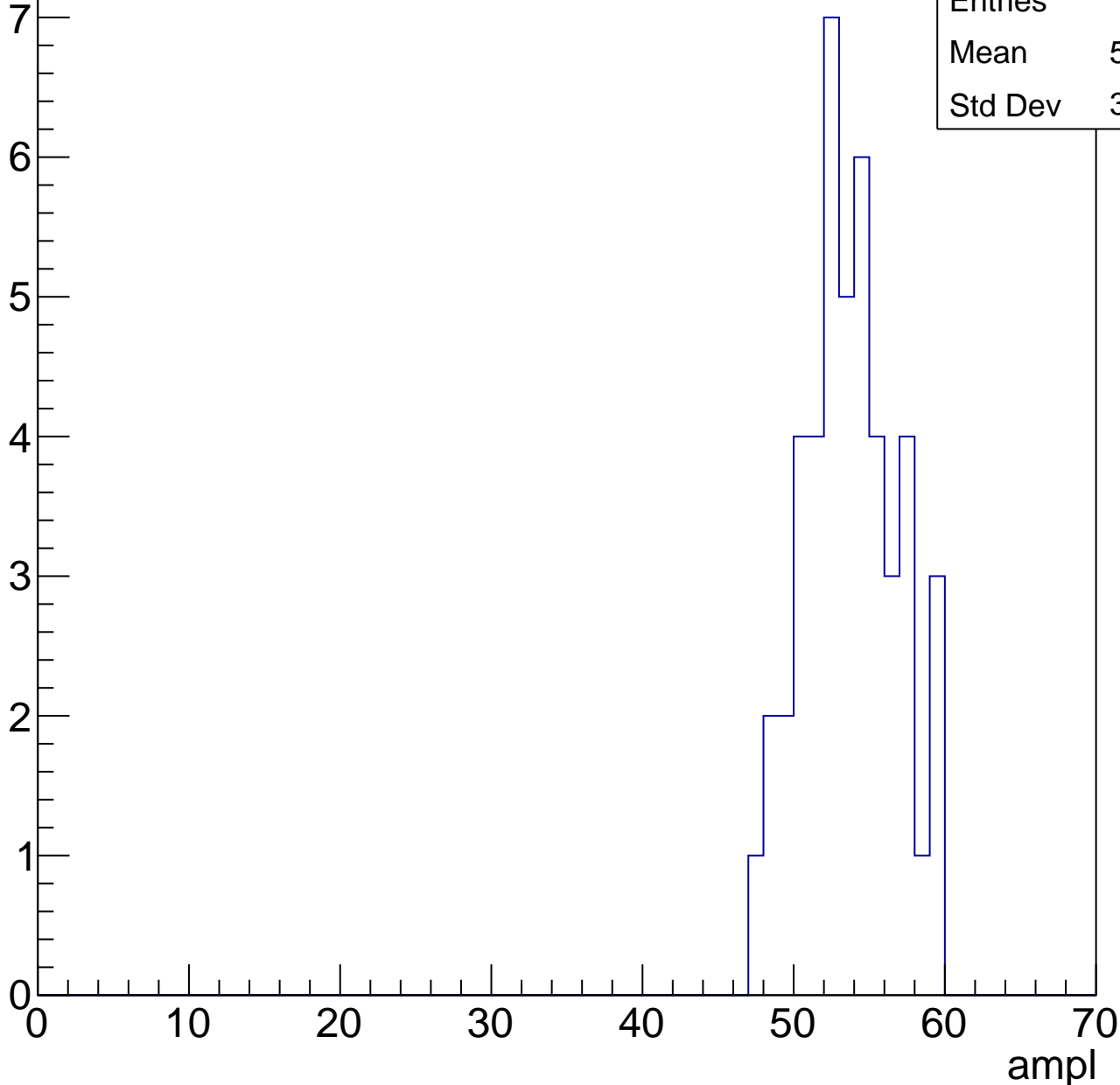


# B1L103S, U4-ch70, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 46    |
| Mean    | 53.24 |
| Std Dev | 3.023 |

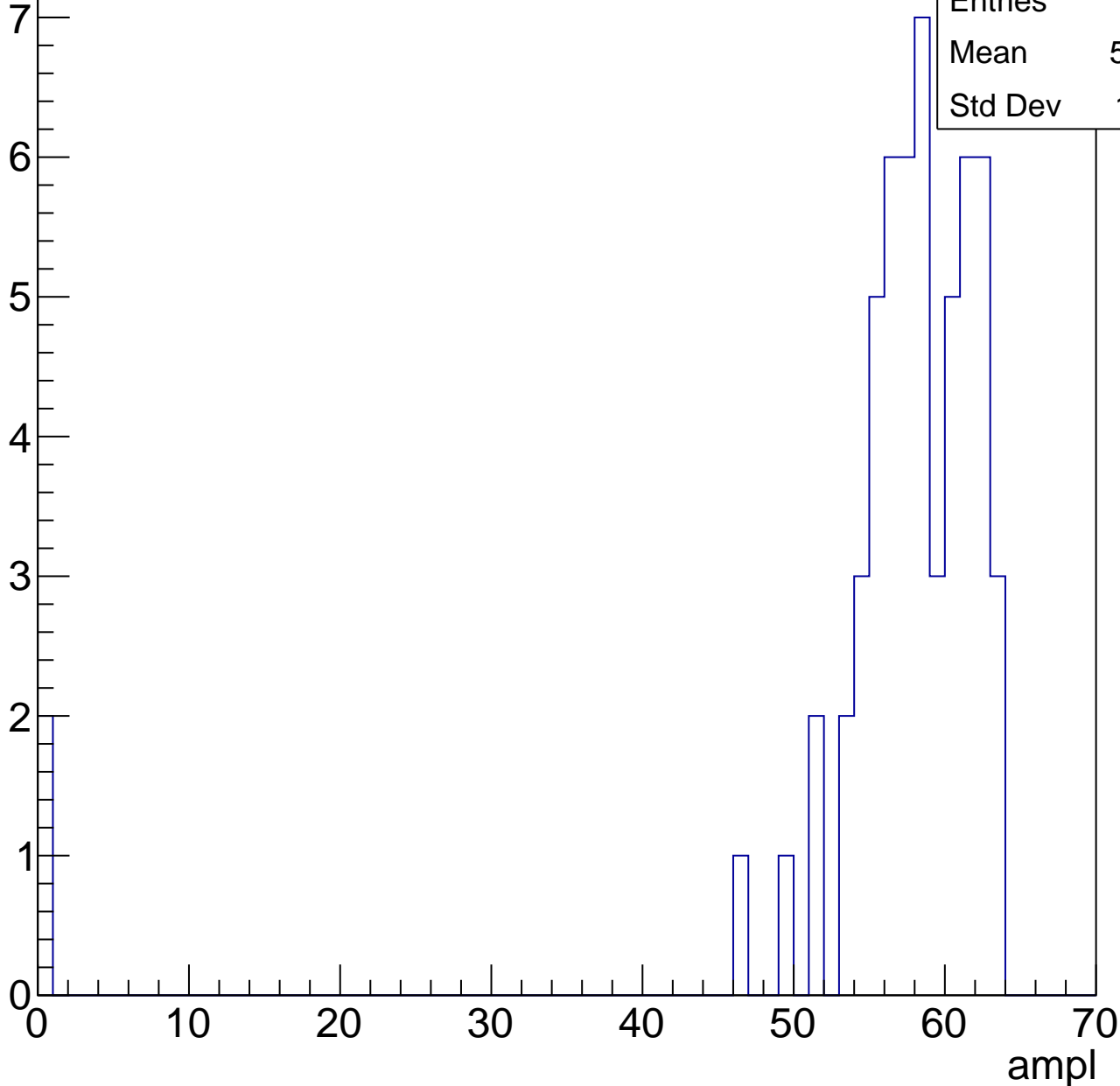


# B1L103S, U4-ch70, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 58    |
| Mean    | 55.66 |
| Std Dev | 11.11 |

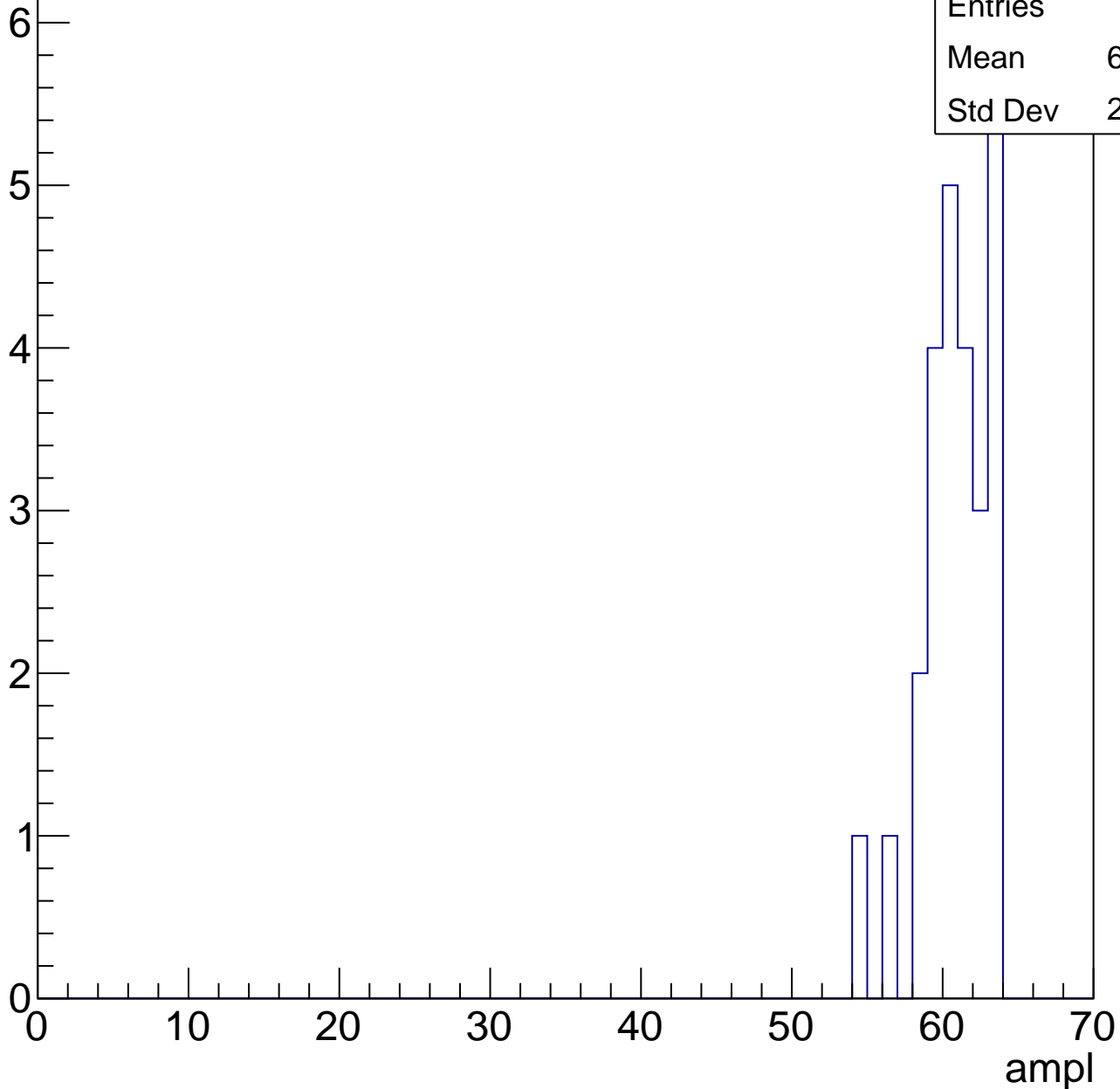


# B1L103S, U4-ch70, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 26    |
| Mean    | 60.38 |
| Std Dev | 2.237 |

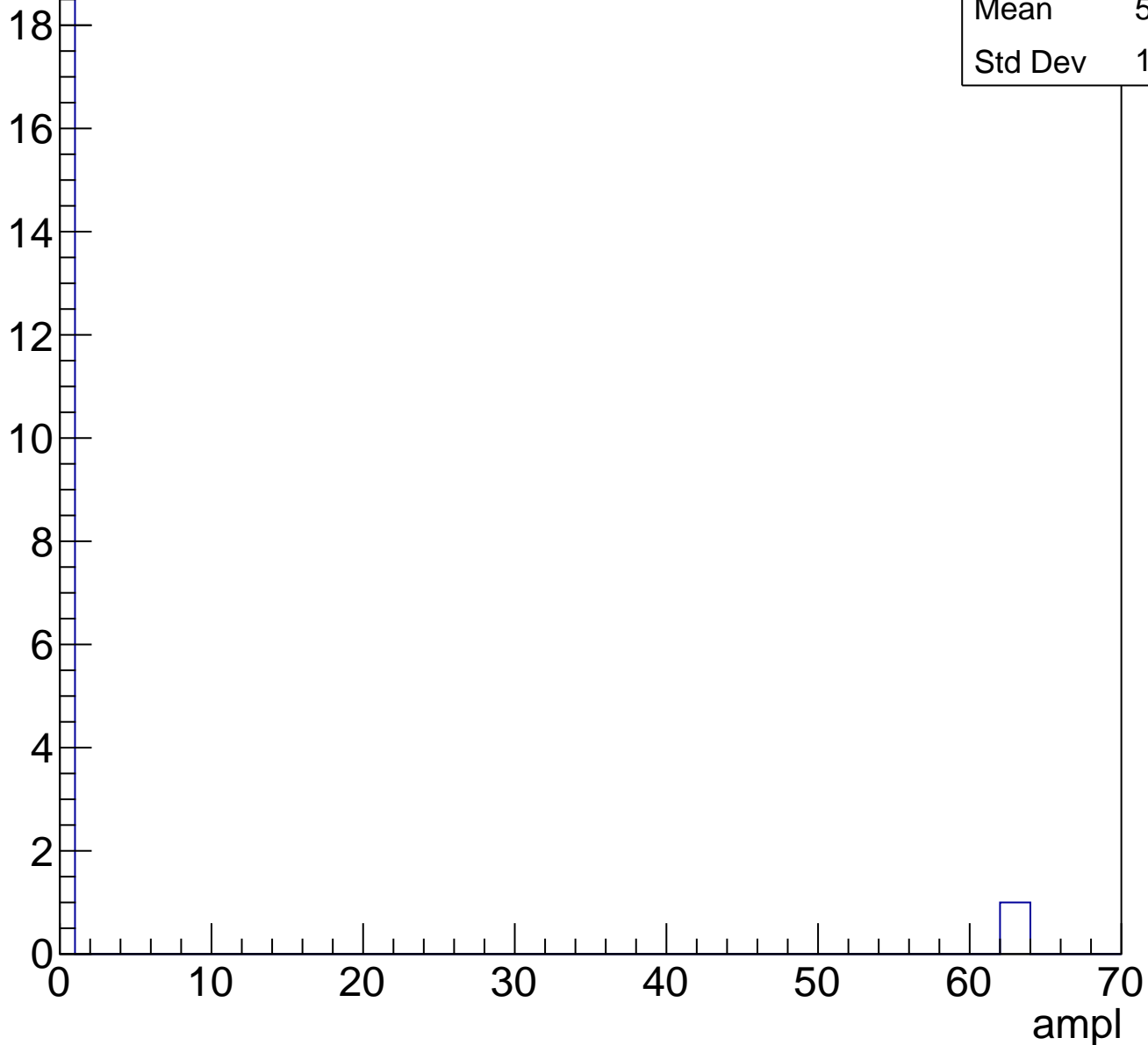




# B1L103S, U4-ch70, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



|         |       |
|---------|-------|
| Entries | 21    |
| Mean    | 5.952 |
| Std Dev | 18.35 |

# B1L103S, U4-ch71, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 90    |
| Mean    | 23.71 |
| Std Dev | 11.43 |

Entry

16  
14  
12  
10  
8  
6  
4  
2  
0

ampl

0

10

20

30

40

50

60

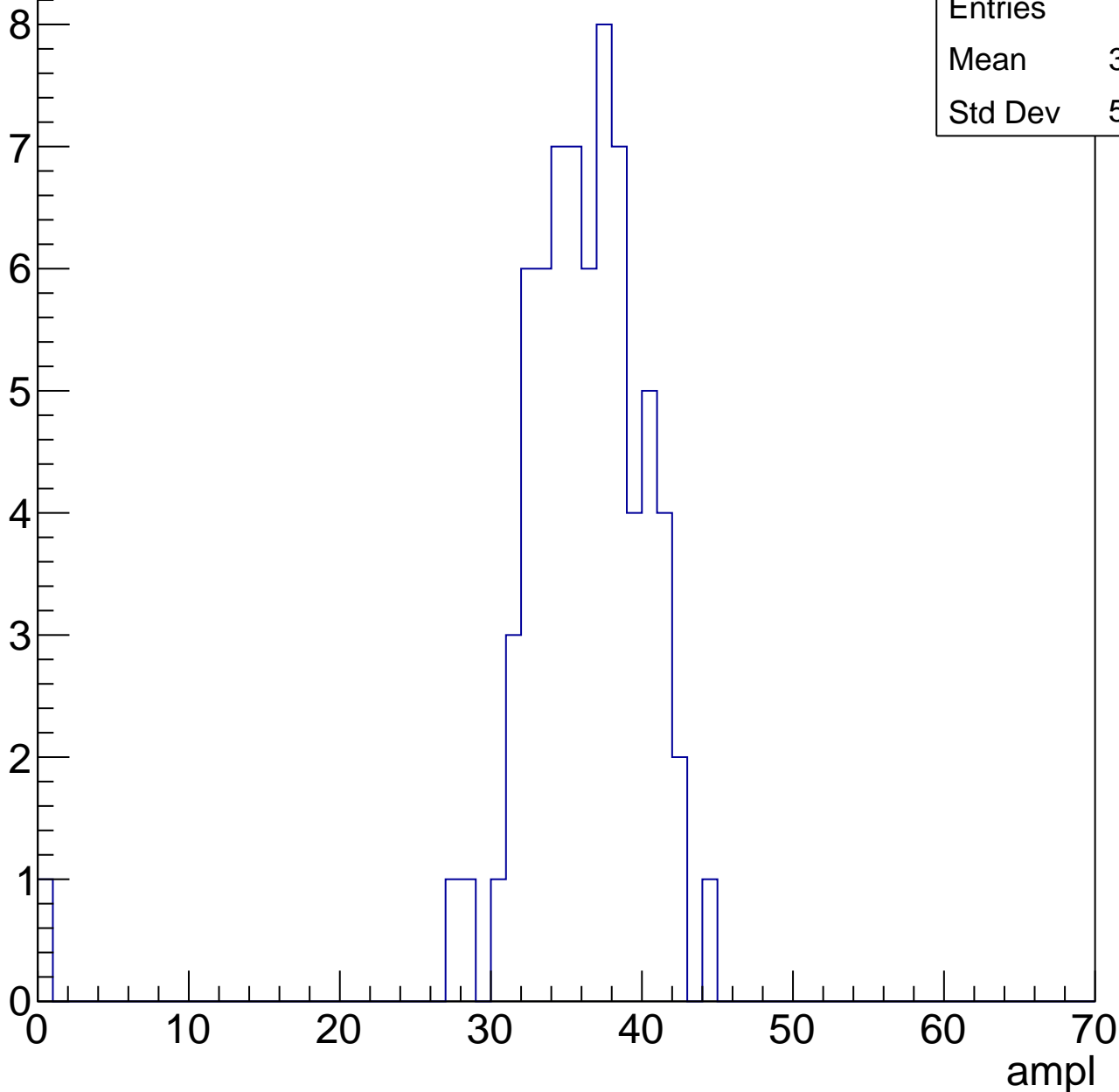
70

# B1L103S, U4-ch71, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

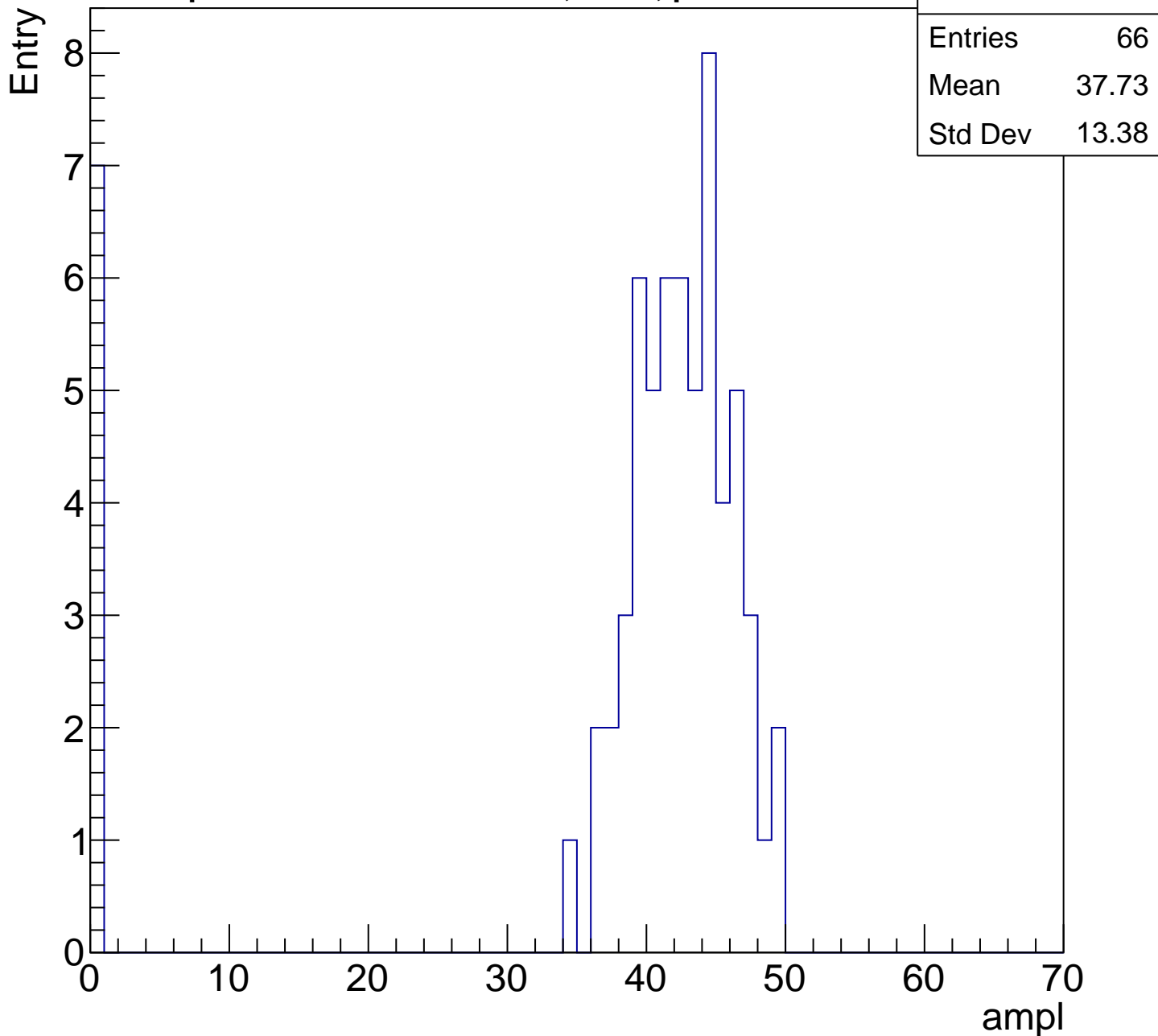
Entry

|         |       |
|---------|-------|
| Entries | 70    |
| Mean    | 35.39 |
| Std Dev | 5.475 |



# B1L103S, U4-ch71, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

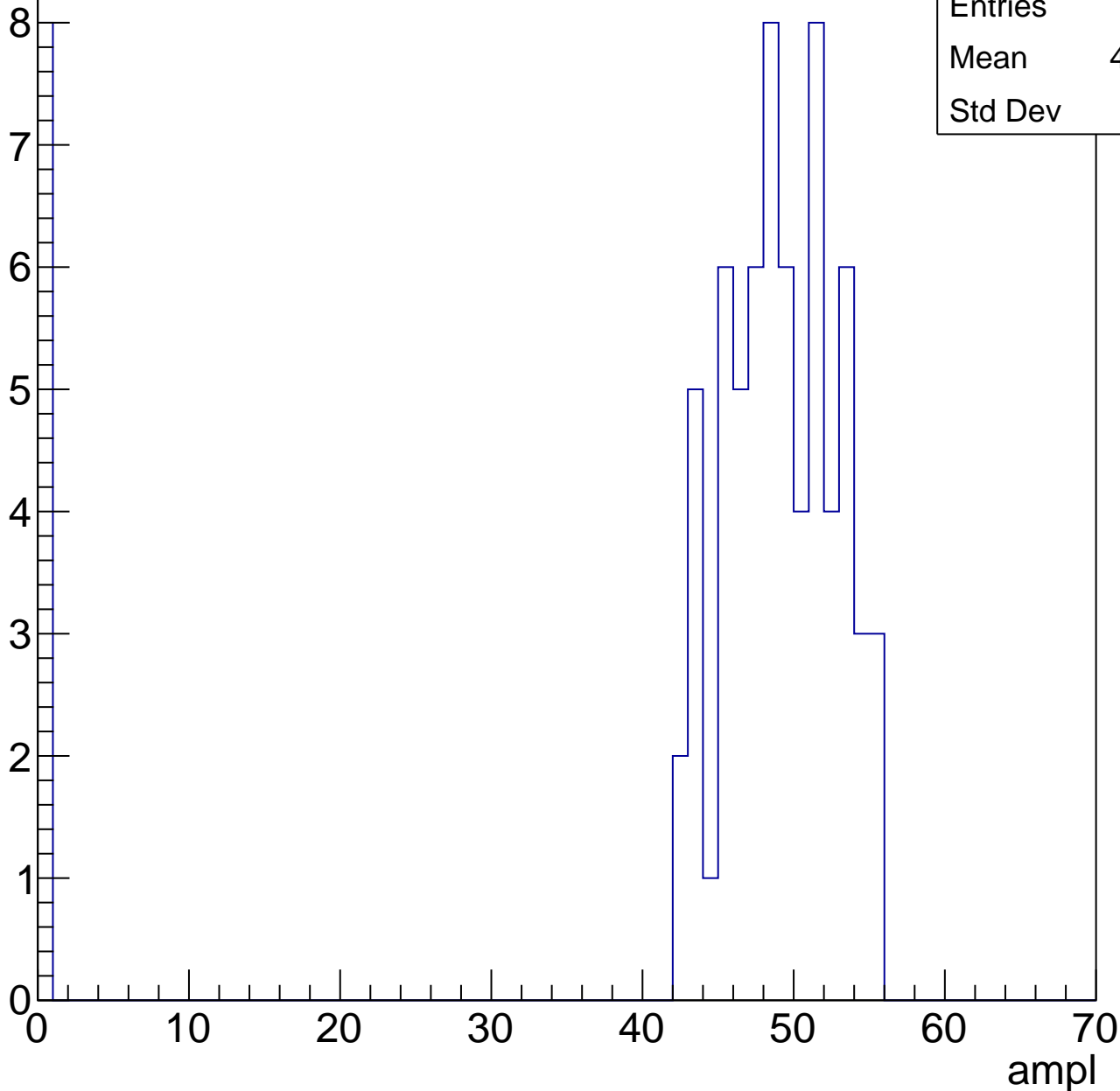


# B1L103S, U4-ch71, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

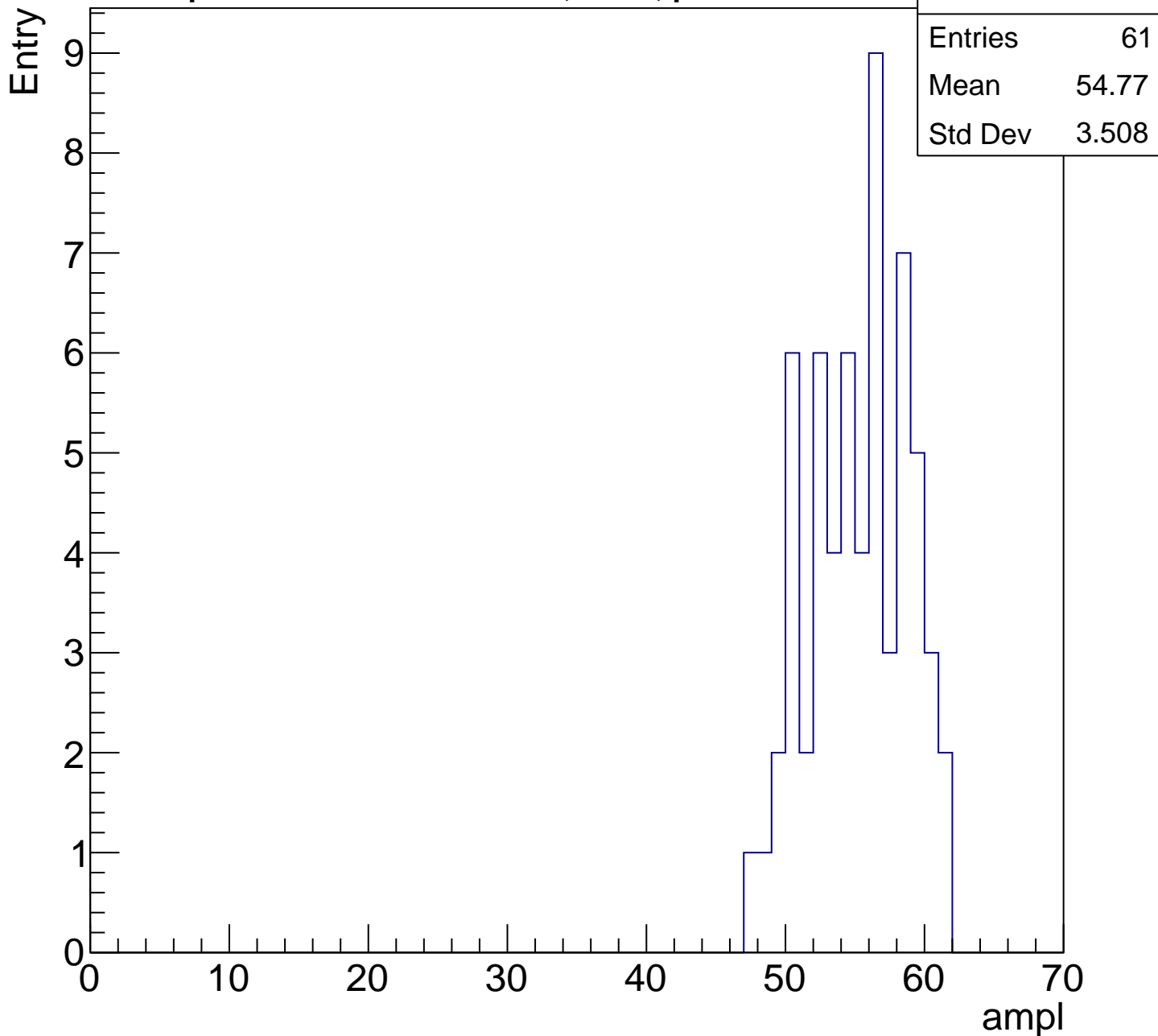
Entry

|         |       |
|---------|-------|
| Entries | 75    |
| Mean    | 43.52 |
| Std Dev | 15.4  |



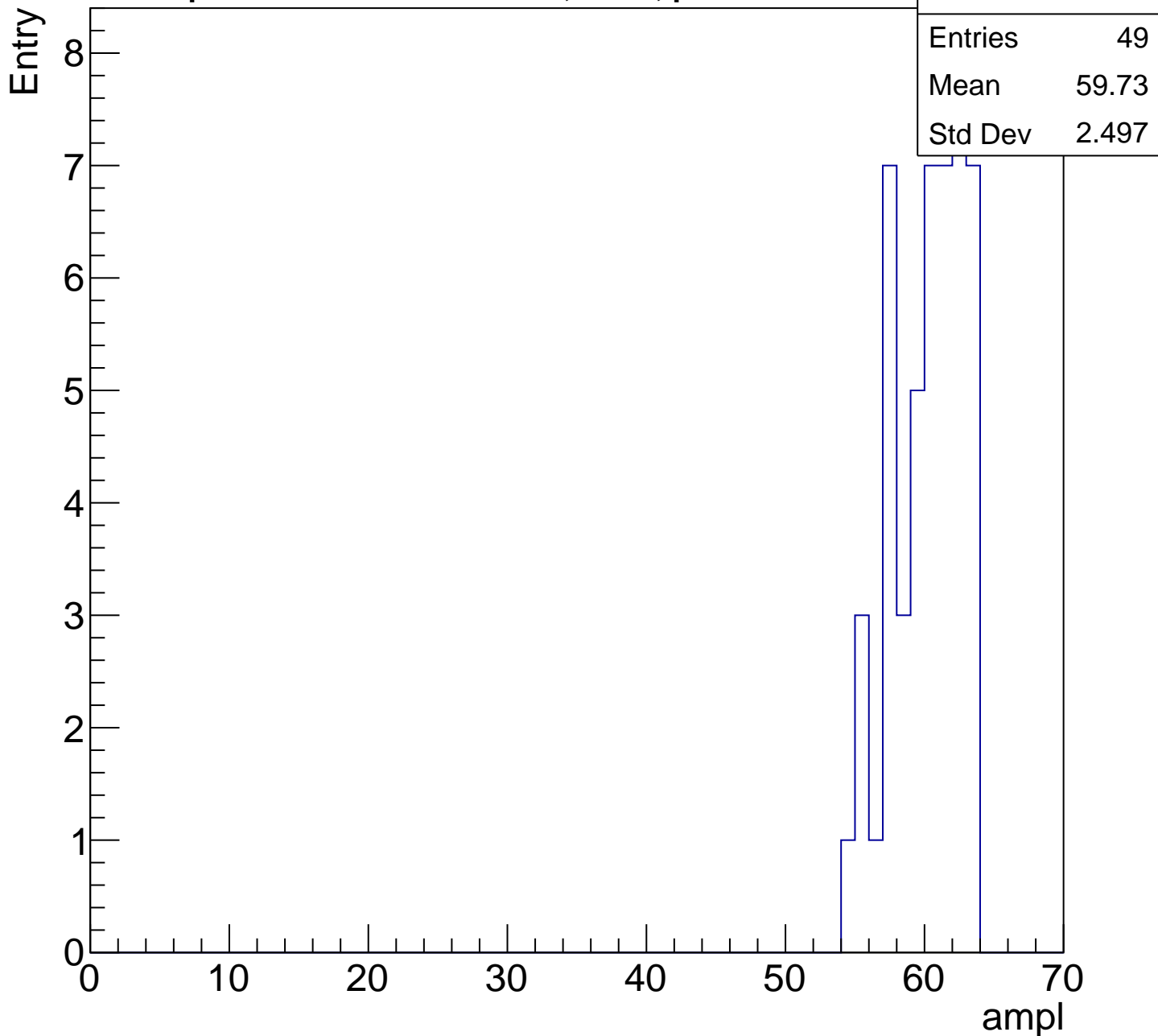
# B1L103S, U4-ch71, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2



# B1L103S, U4-ch71, adc5

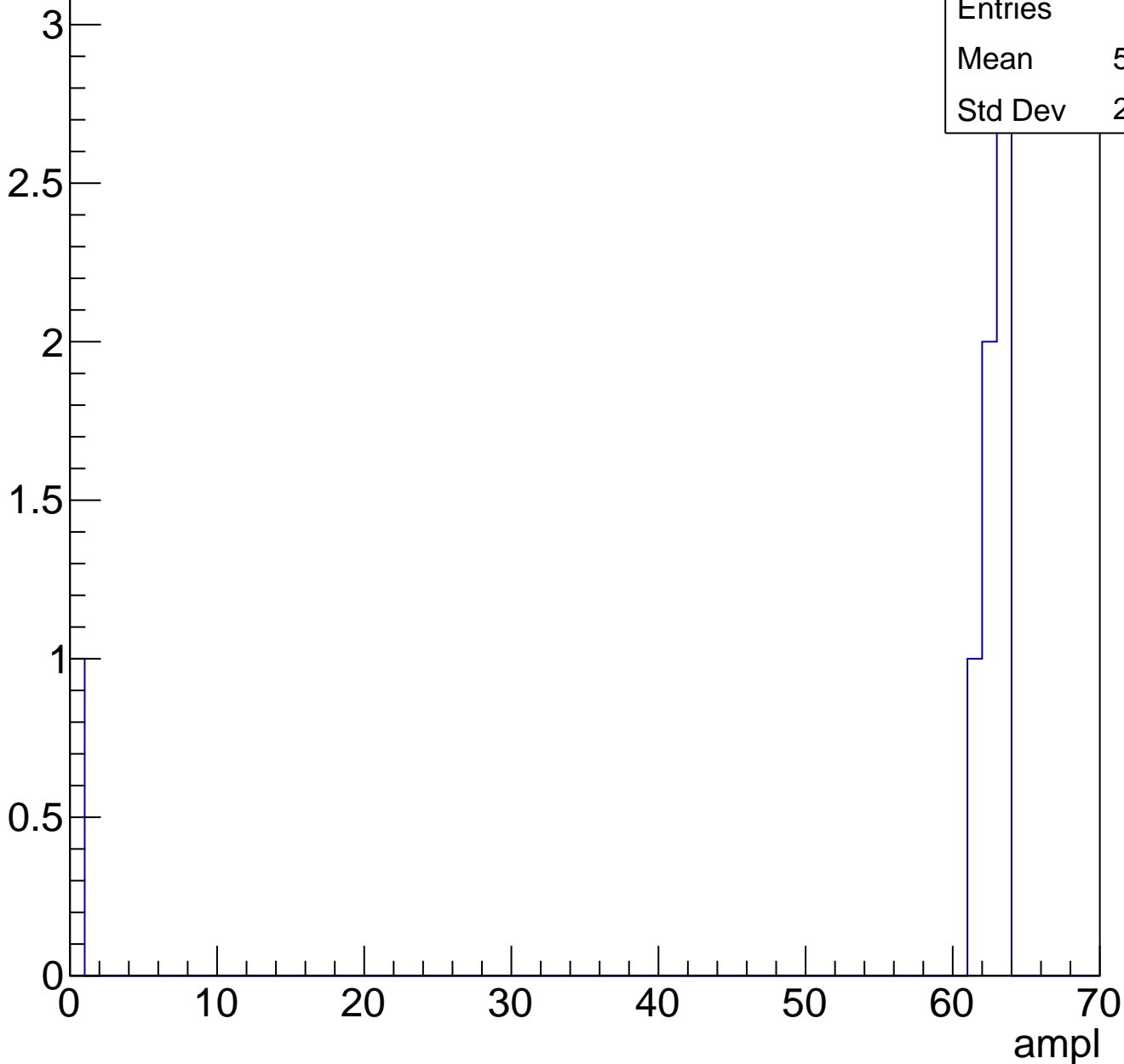
calib\_packv5\_041523\_1651.root, FC#0, port C2



# B1L103S, U4-ch71, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U4-ch71, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

|         |    |
|---------|----|
| Entries | 18 |
| Mean    | 0  |
| Std Dev | 0  |

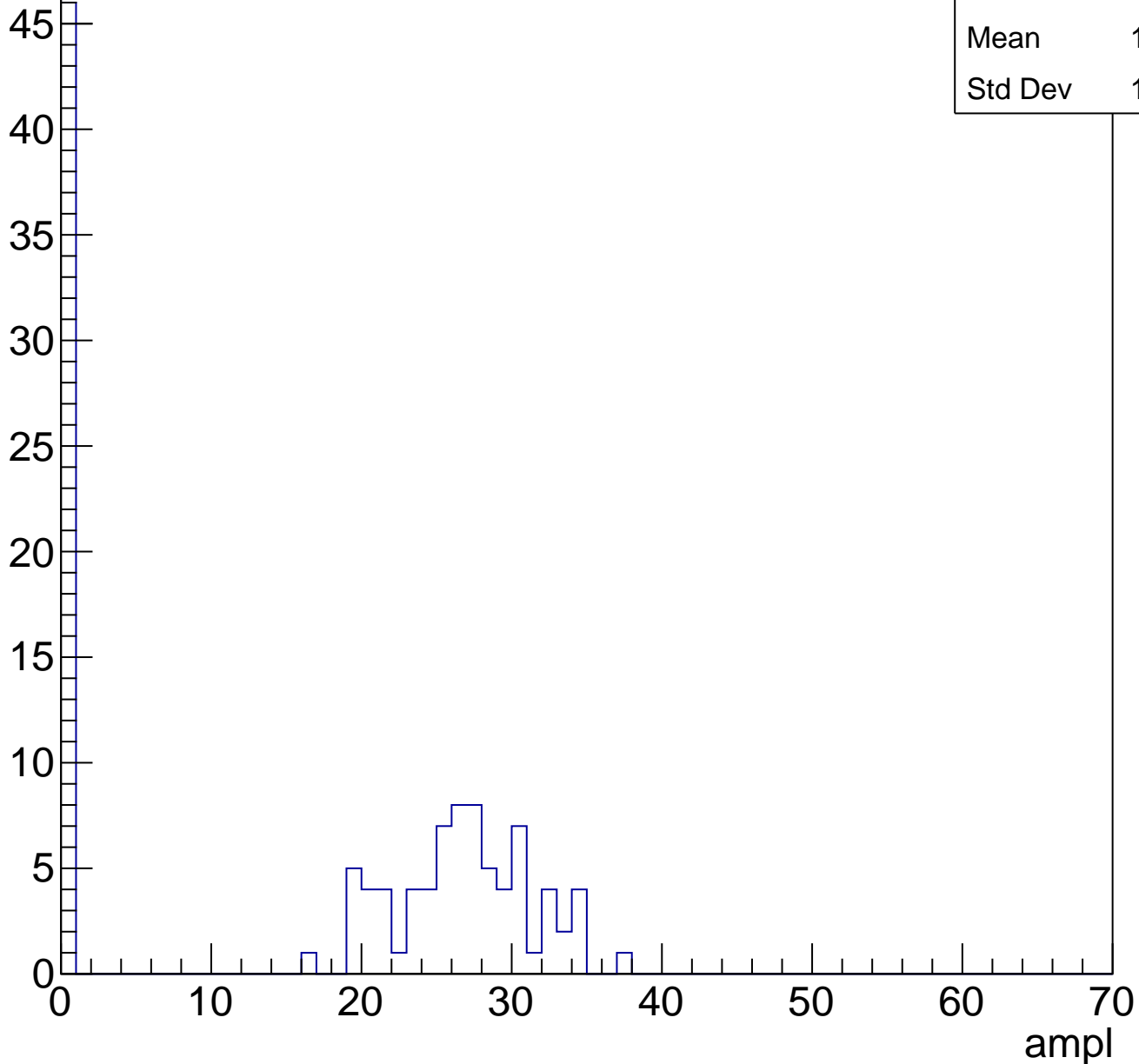
ampl

# B1L103S, U4-ch72, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 120   |
| Mean    | 16.23 |
| Std Dev | 13.27 |

Entry



# B1L103S, U4-ch72, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 91    |
| Mean    | 32.18 |
| Std Dev | 8.583 |

Entry

10

8

6

4

2

0

0

10

20

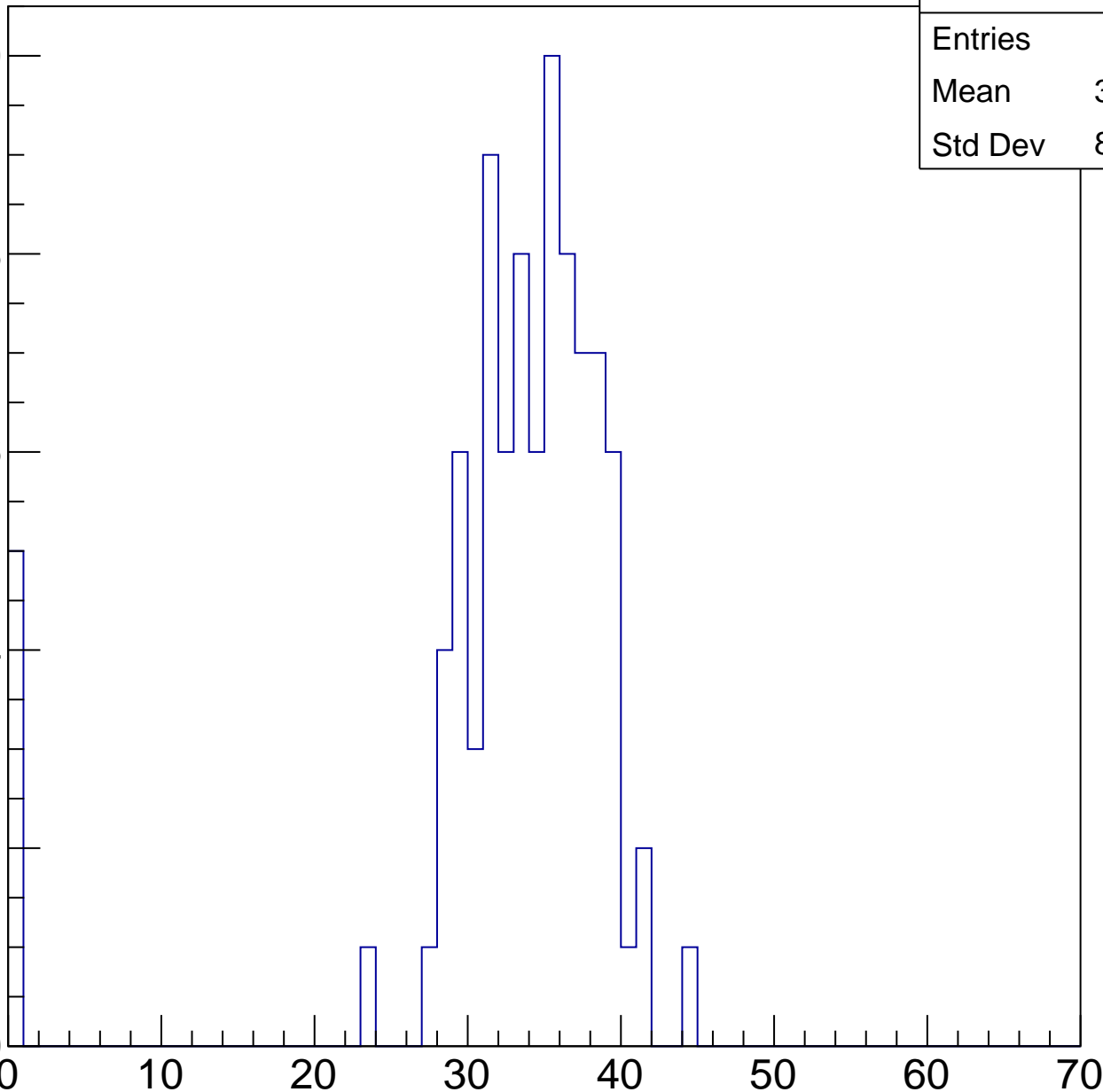
30

40

50

60

ampl

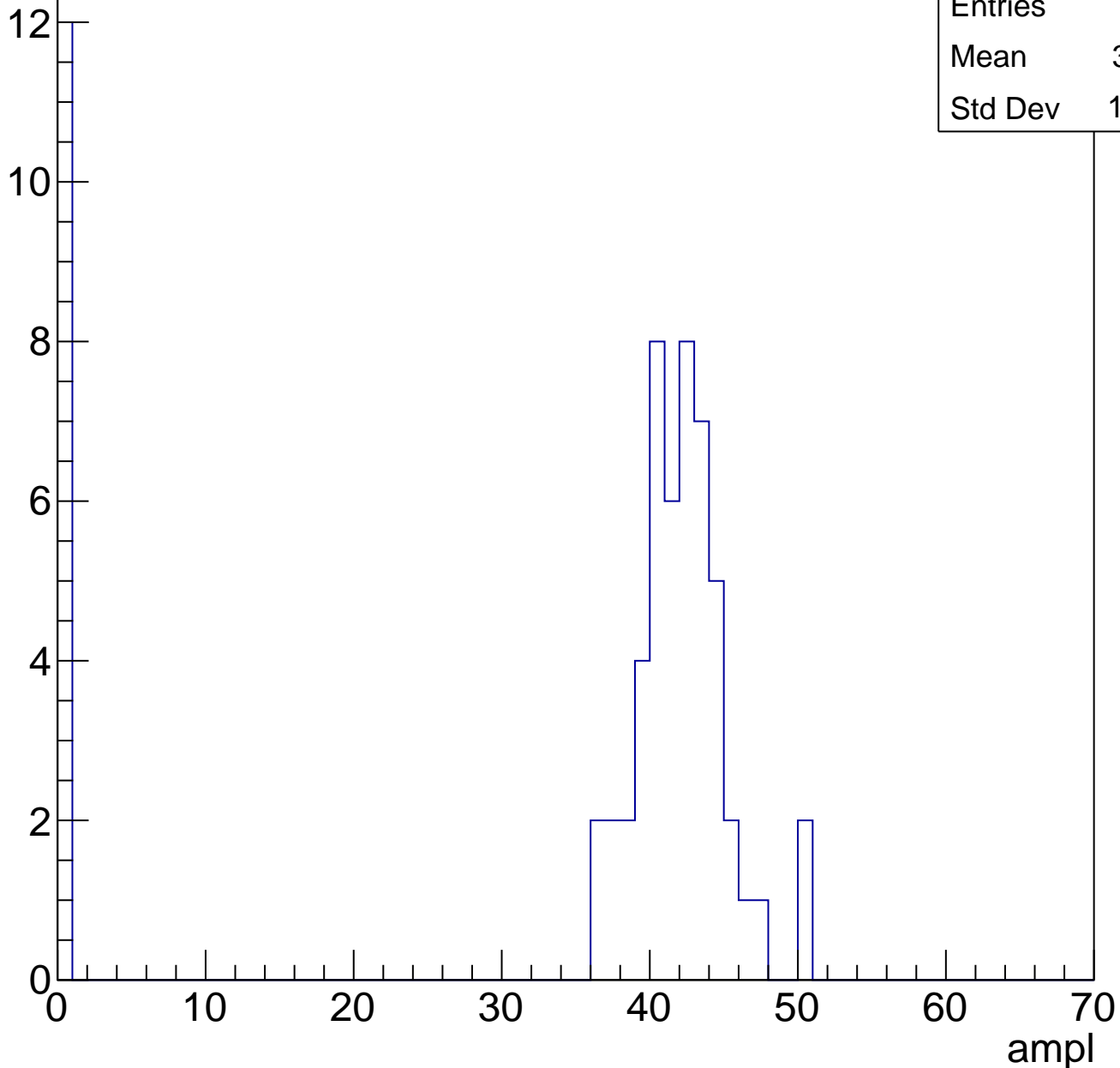


# B1L103S, U4-ch72, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

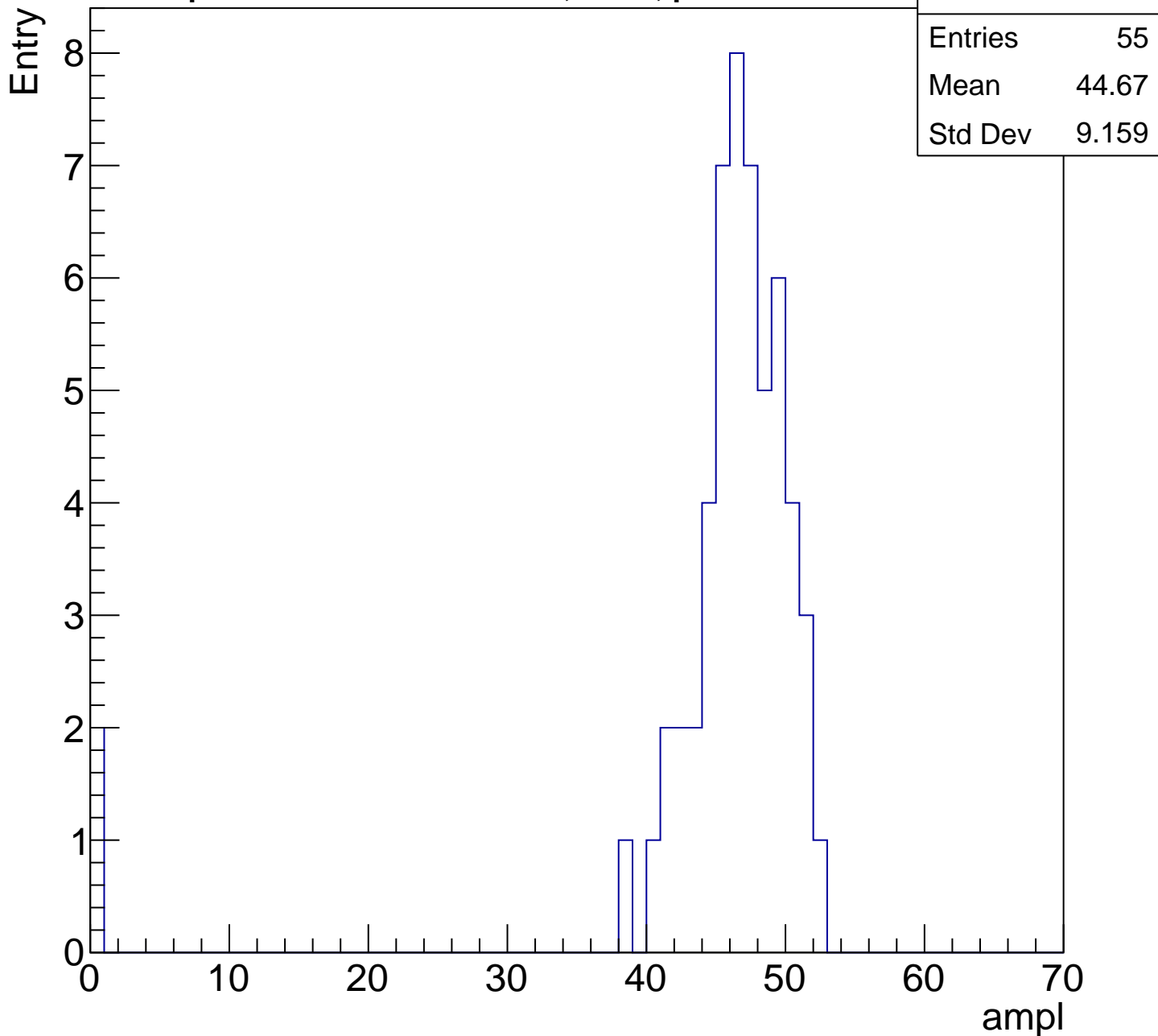
|         |       |
|---------|-------|
| Entries | 62    |
| Mean    | 33.61 |
| Std Dev | 16.68 |

Entry



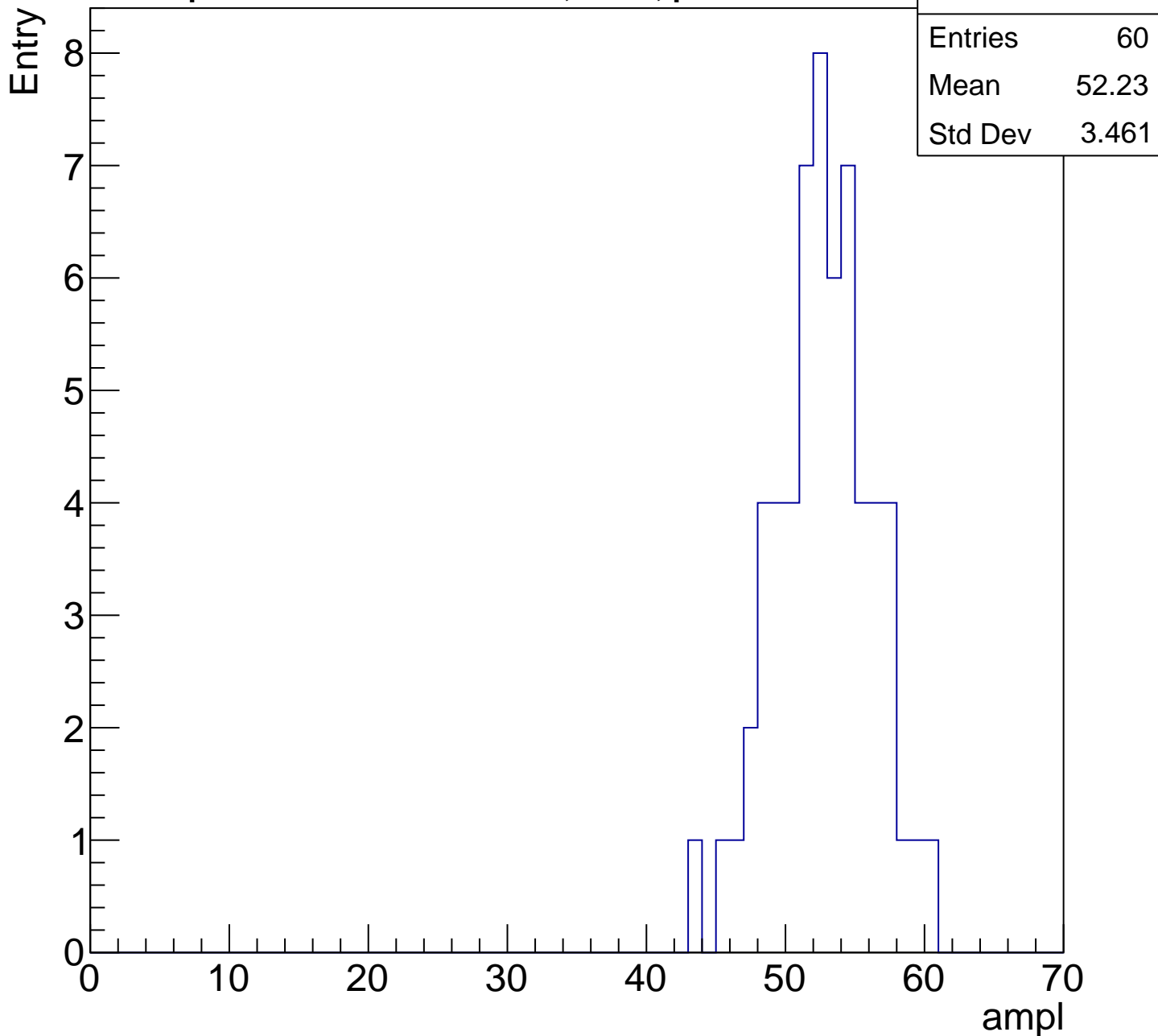
# B1L103S, U4-ch72, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2



# B1L103S, U4-ch72, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

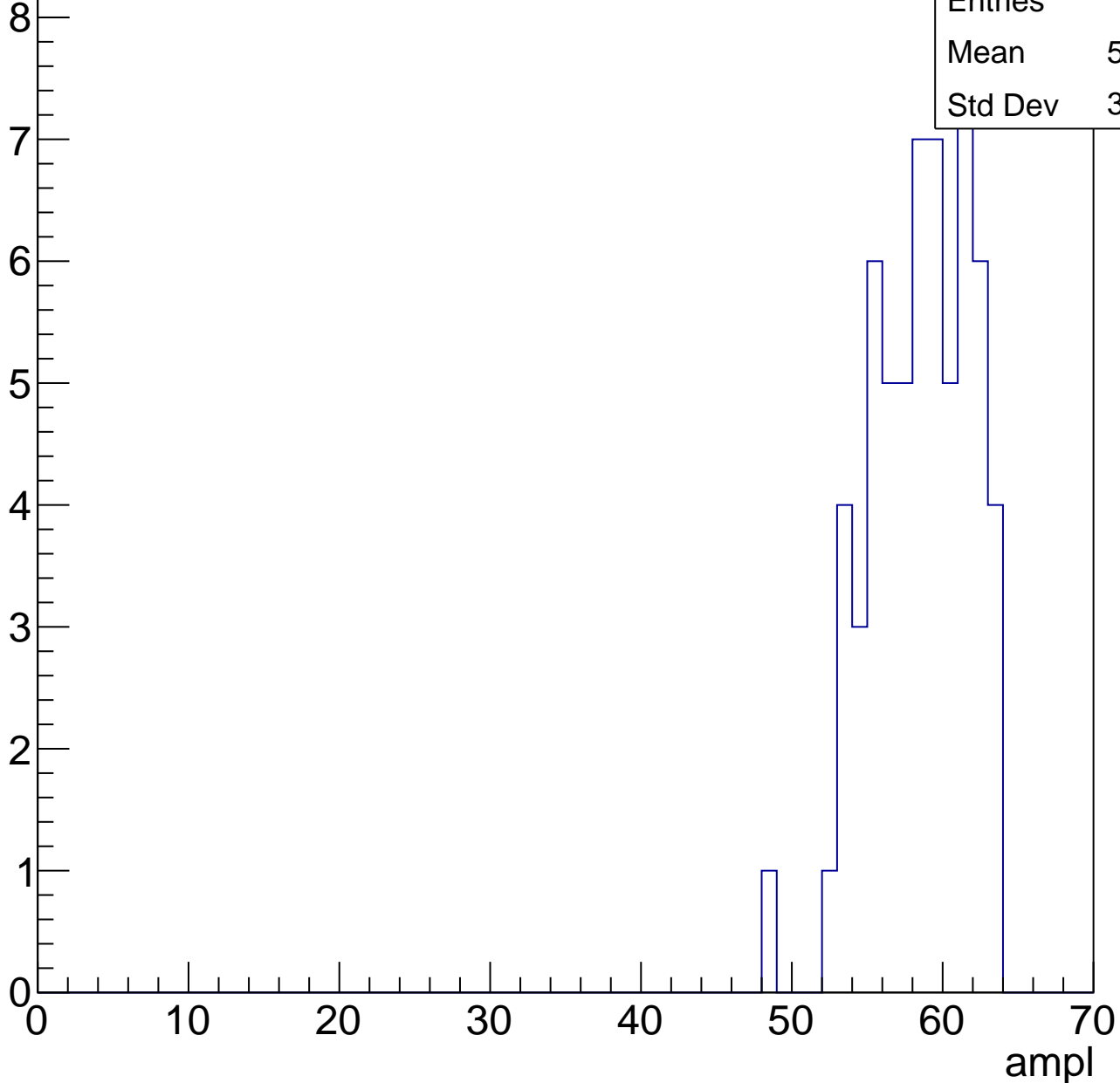


# B1L103S, U4-ch72, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 62    |
| Mean    | 58.06 |
| Std Dev | 3.257 |

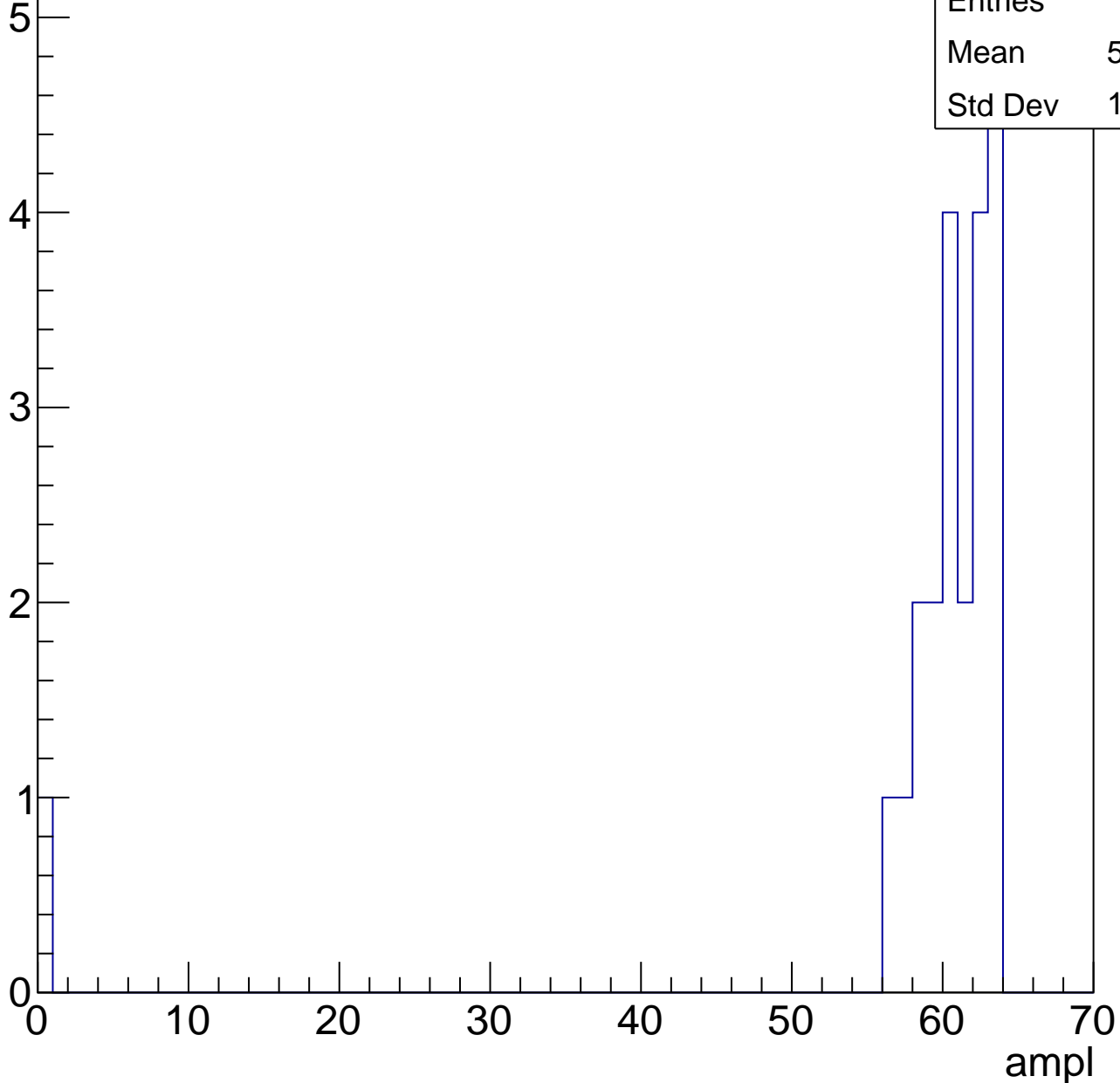


# B1L103S, U4-ch72, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 22    |
| Mean    | 57.82 |
| Std Dev | 12.78 |





# B1L103S, U4-ch72, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 20    |
| Mean    | 3.15  |
| Std Dev | 13.73 |

Entry



# B1L103S, U4-ch73, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 83    |
| Mean    | 24.66 |
| Std Dev | 11.2  |

Entry

12

10

8

6

4

2

0

0

10

20

30

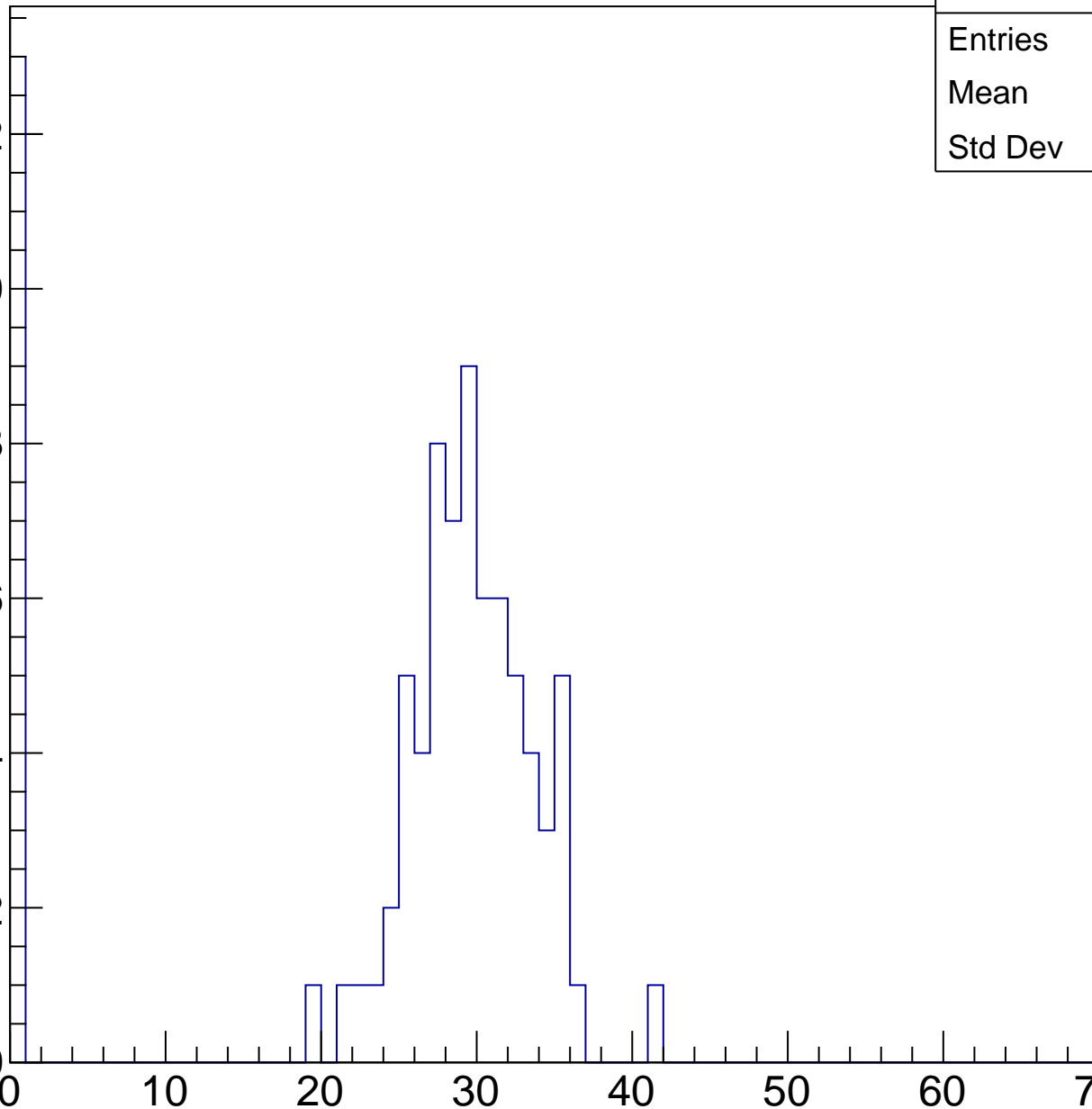
40

50

60

70

ampl

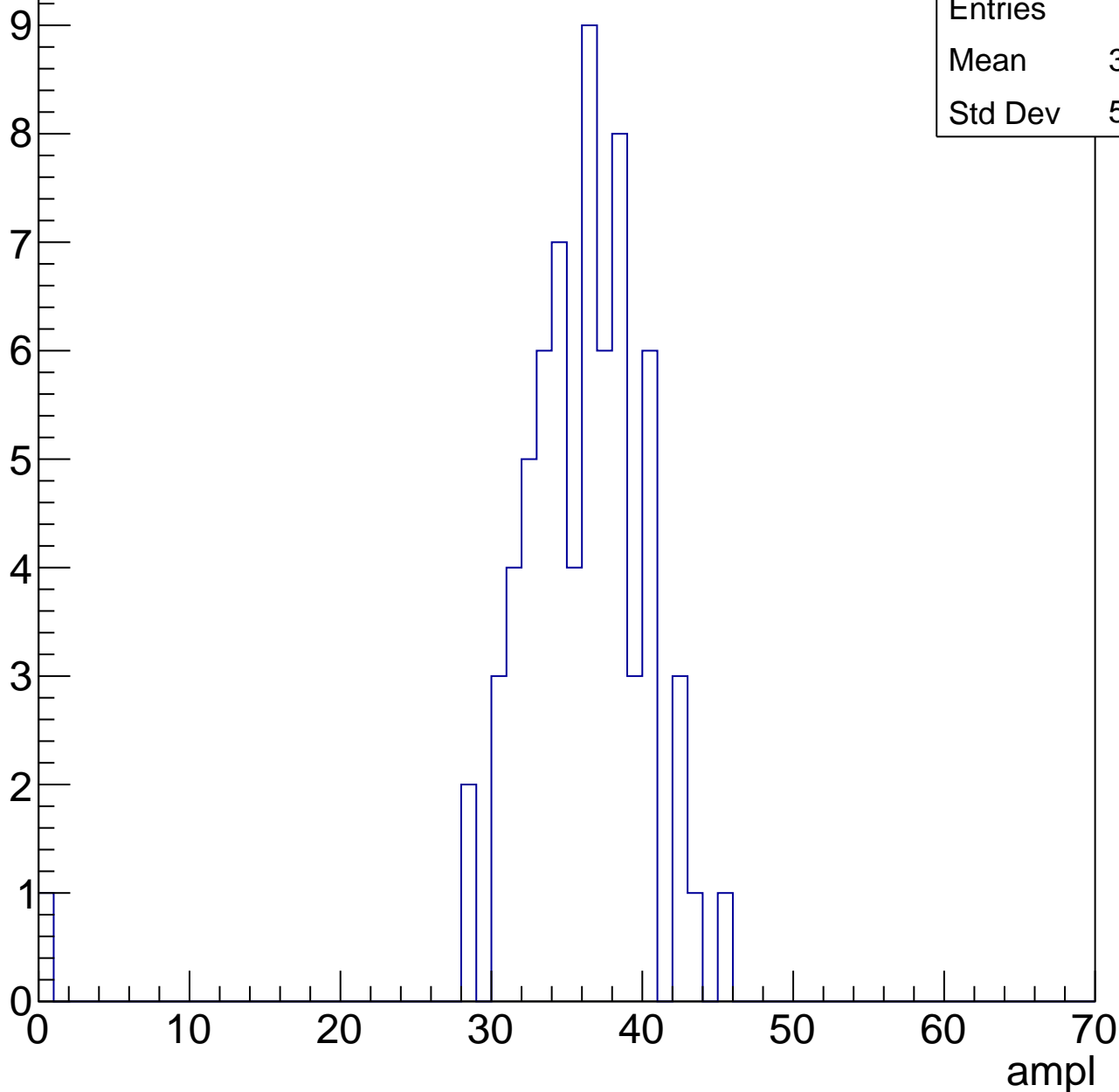


# B1L103S, U4-ch73, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 69    |
| Mean    | 35.17 |
| Std Dev | 5.582 |

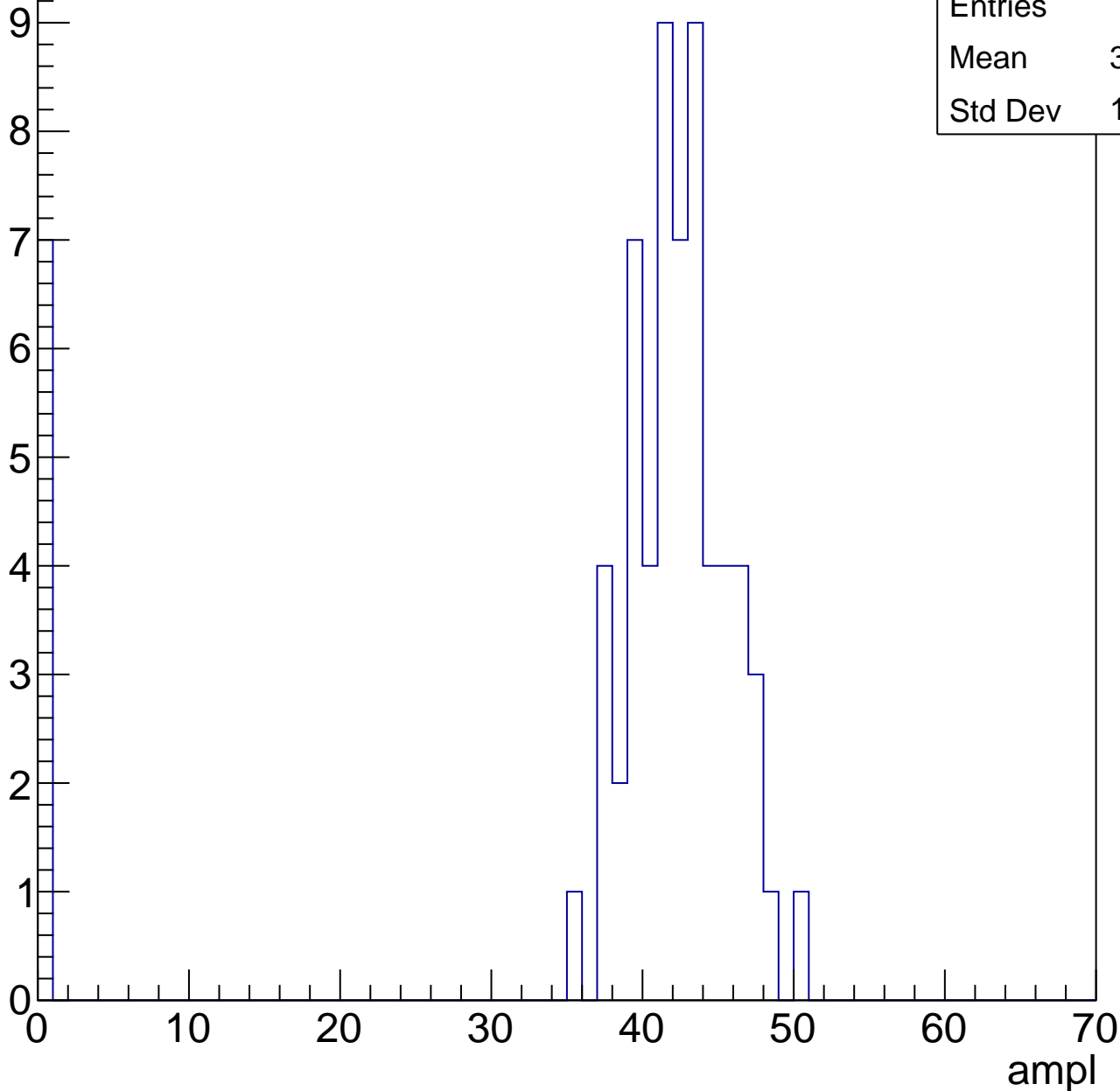


# B1L103S, U4-ch73, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

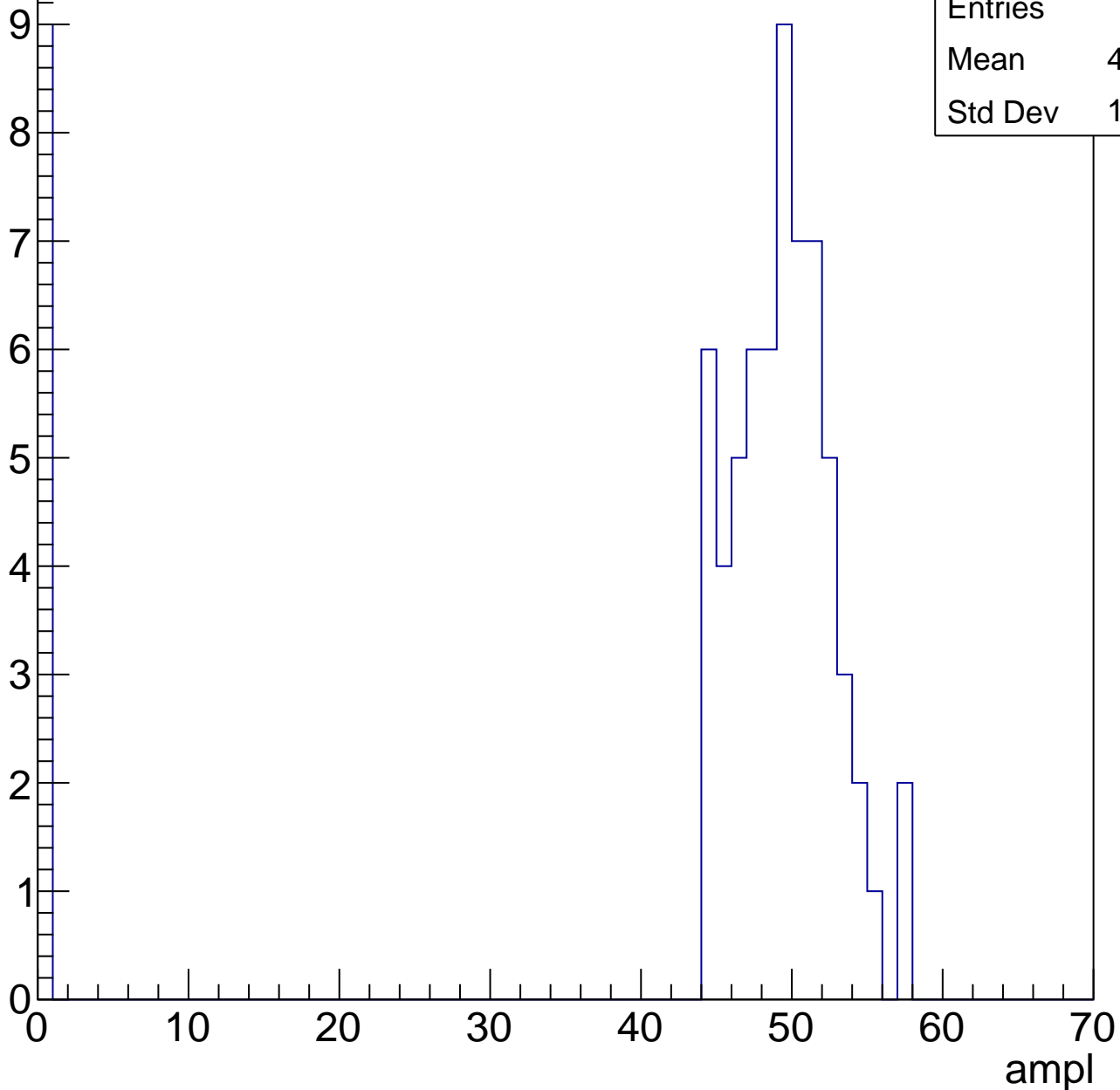
|         |       |
|---------|-------|
| Entries | 67    |
| Mean    | 37.63 |
| Std Dev | 13.18 |



# B1L103S, U4-ch73, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

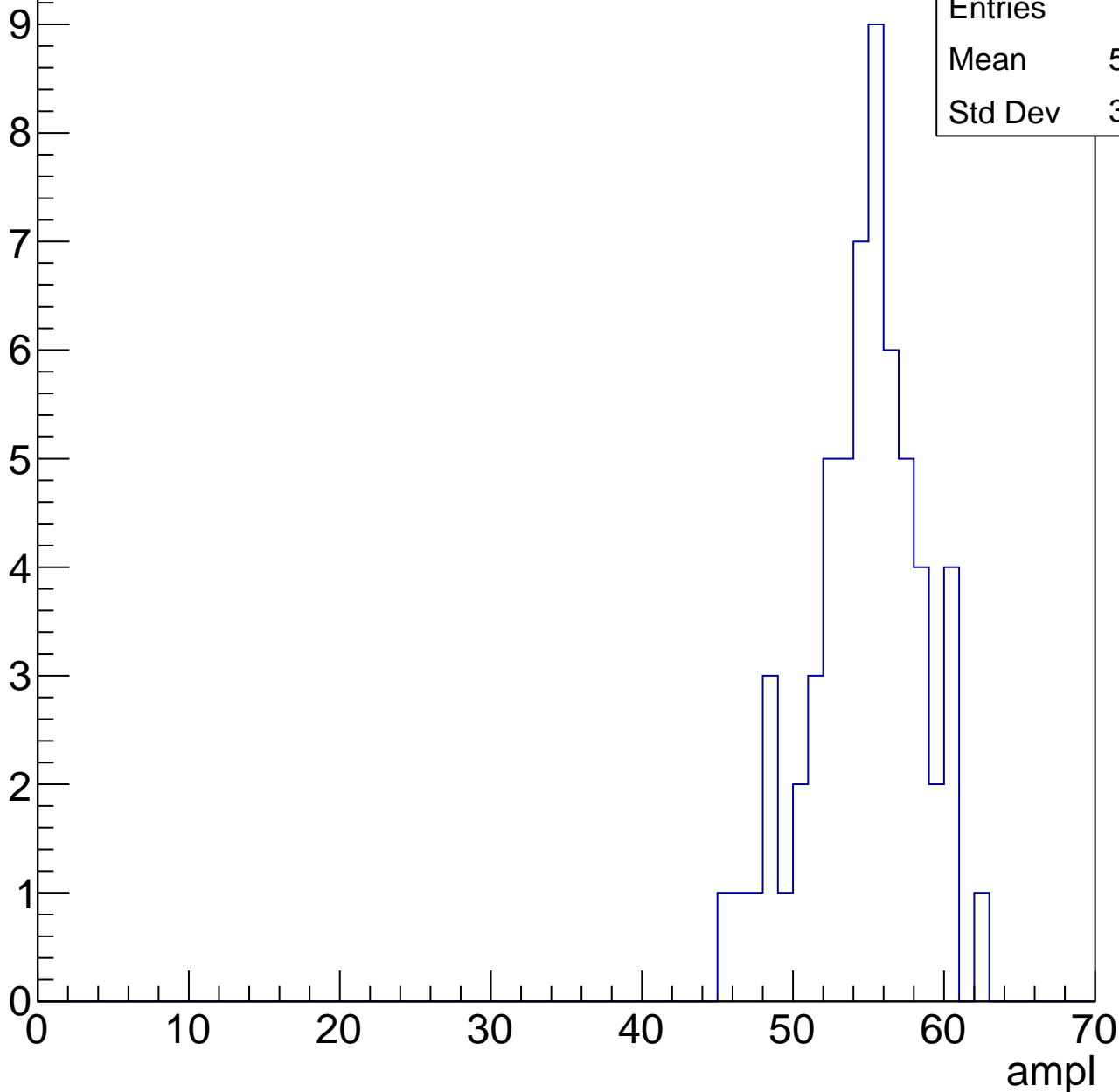


# B1L103S, U4-ch73, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 60    |
| Mean    | 54.25 |
| Std Dev | 3.668 |

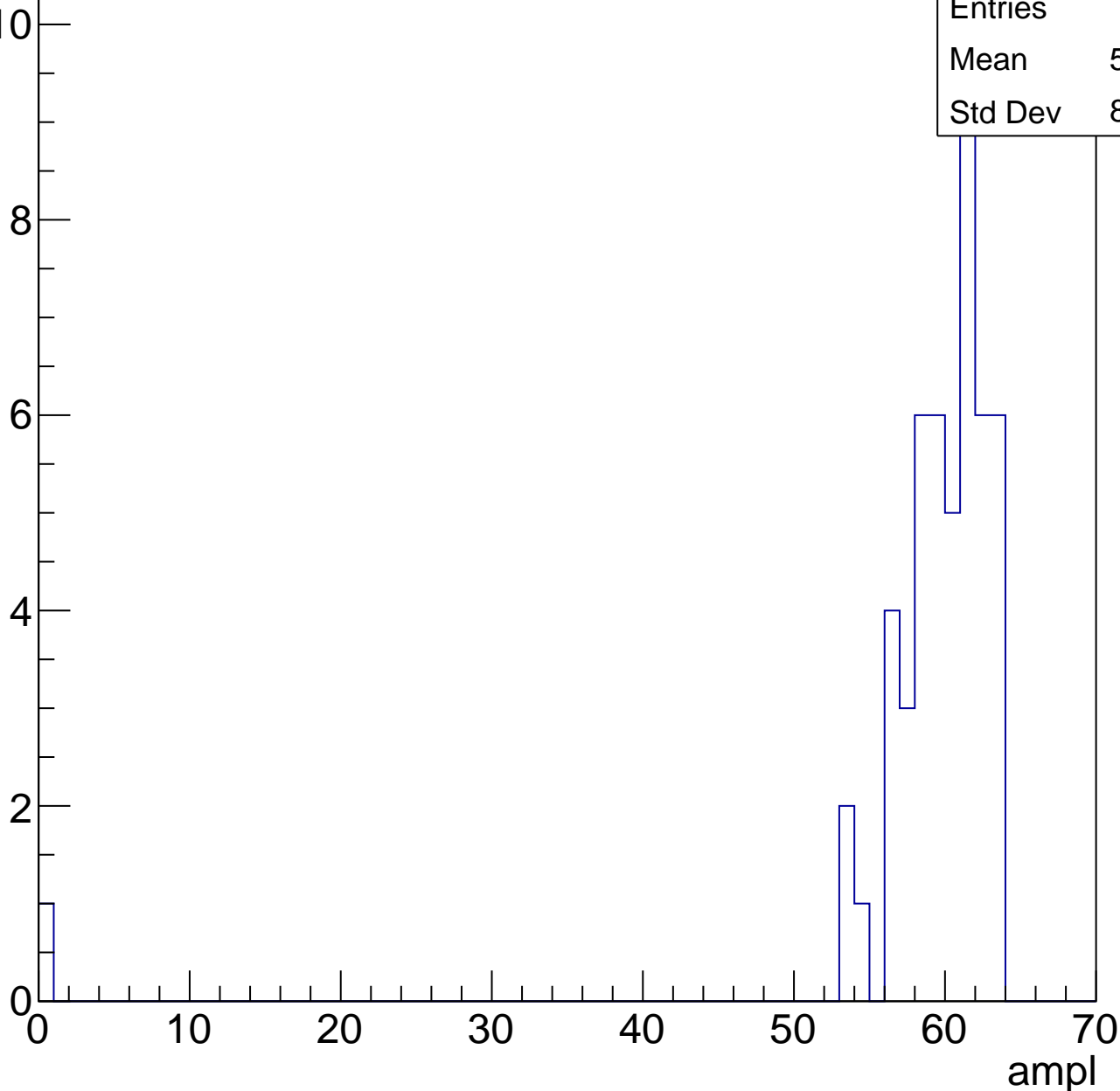


# B1L103S, U4-ch73, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

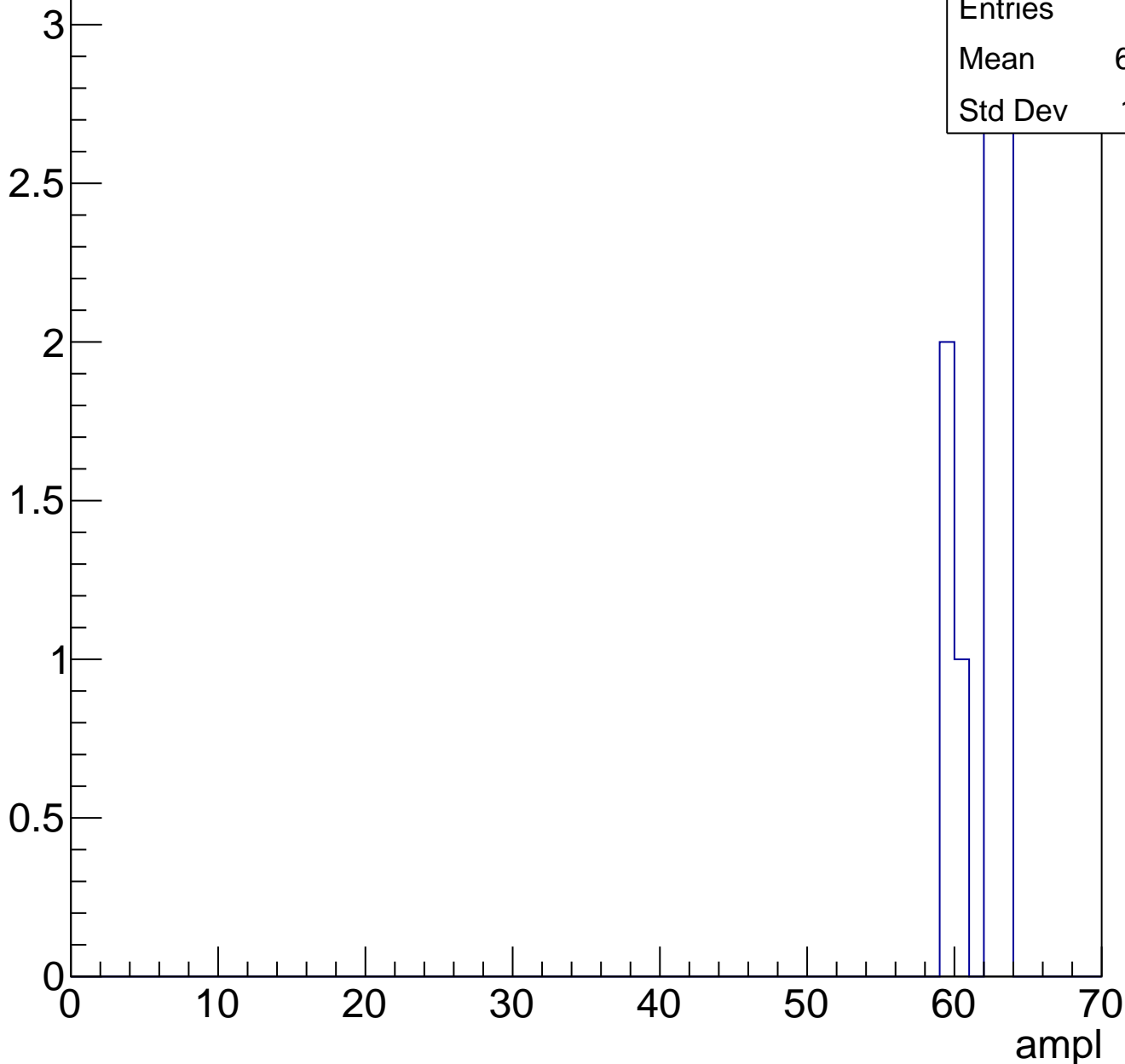
|         |       |
|---------|-------|
| Entries | 50    |
| Mean    | 58.34 |
| Std Dev | 8.724 |



# B1L103S, U4-ch73, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U4-ch73, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

|         |       |
|---------|-------|
| Entries | 20    |
| Mean    | 3.15  |
| Std Dev | 13.73 |

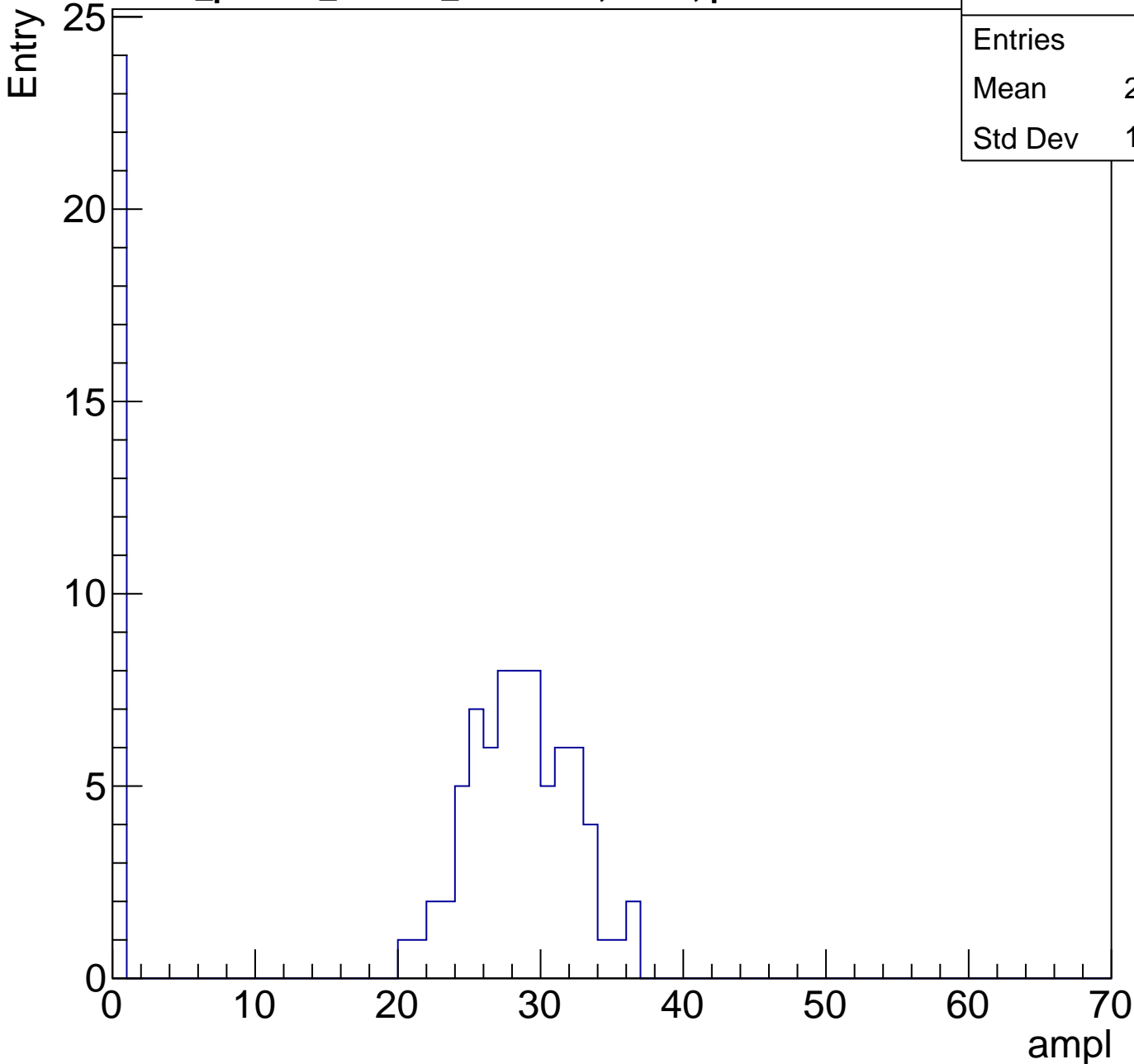
ampl

0 10 20 30 40 50 60 70

# B1L103S, U4-ch74, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 97    |
| Mean    | 21.19 |
| Std Dev | 12.52 |

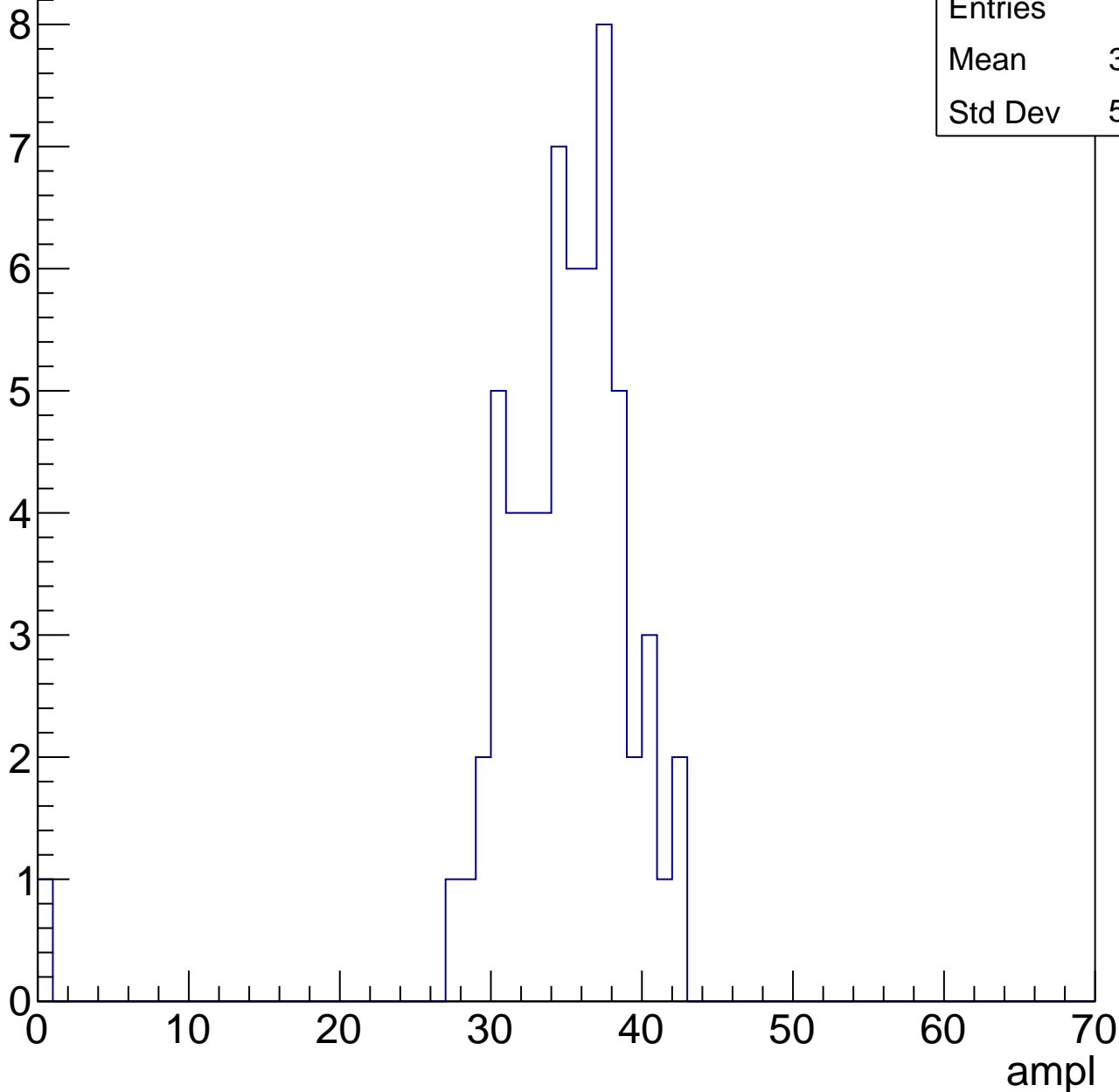


# B1L103S, U4-ch74, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 62    |
| Mean    | 34.19 |
| Std Dev | 5.596 |

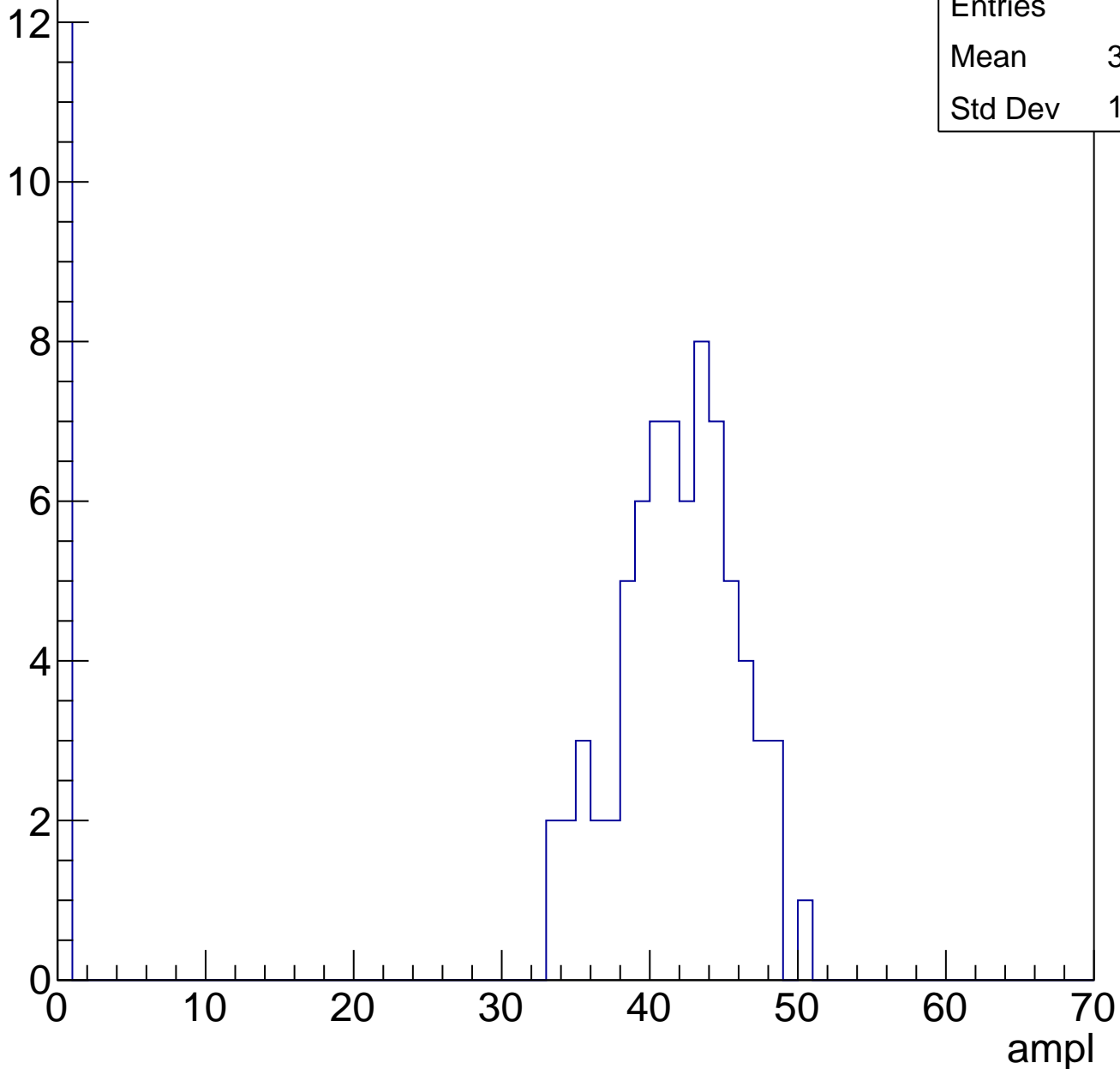


# B1L103S, U4-ch74, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 85    |
| Mean    | 35.58 |
| Std Dev | 14.86 |

Entry

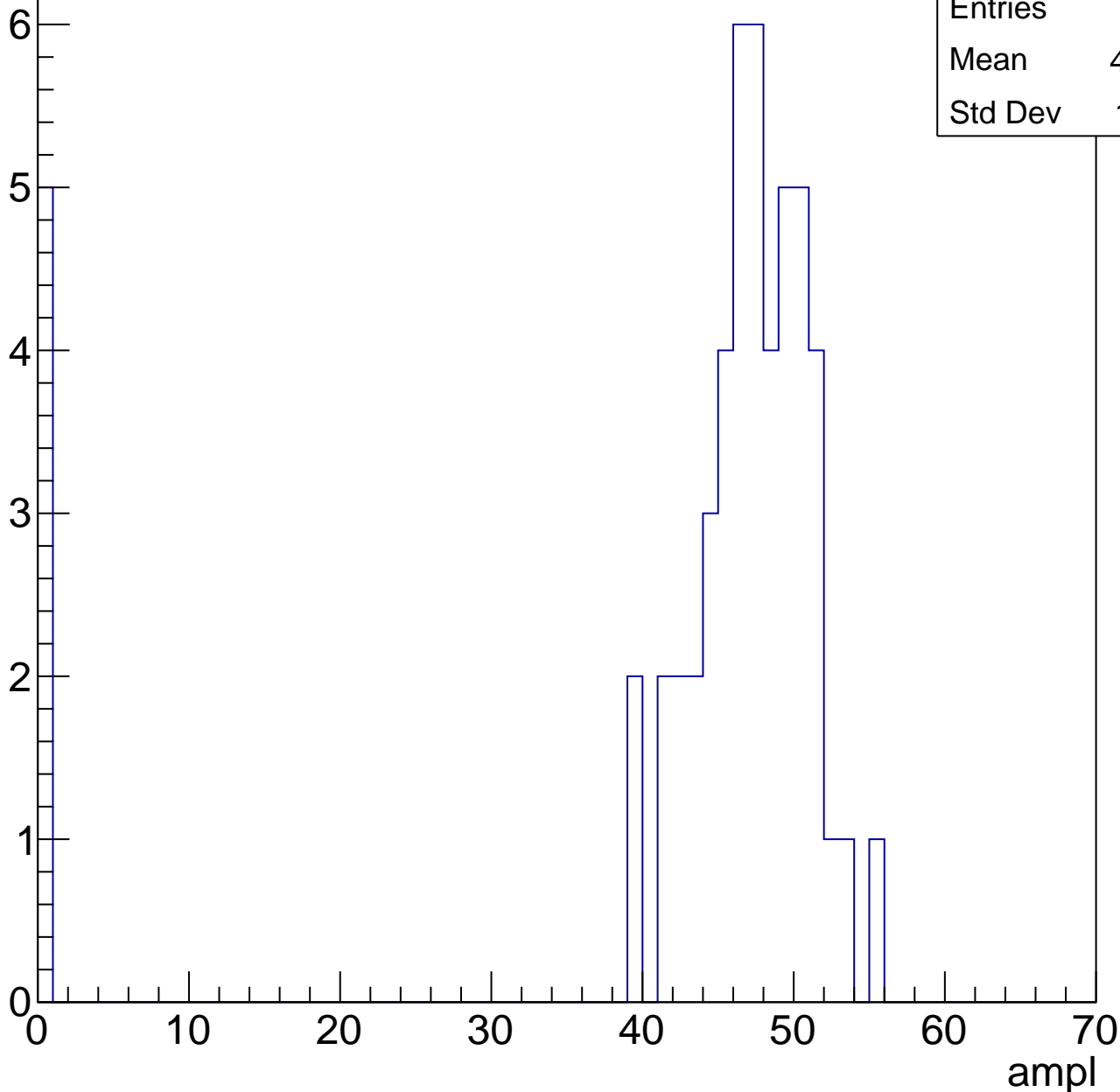


# B1L103S, U4-ch74, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 53    |
| Mean    | 42.47 |
| Std Dev | 14.11 |

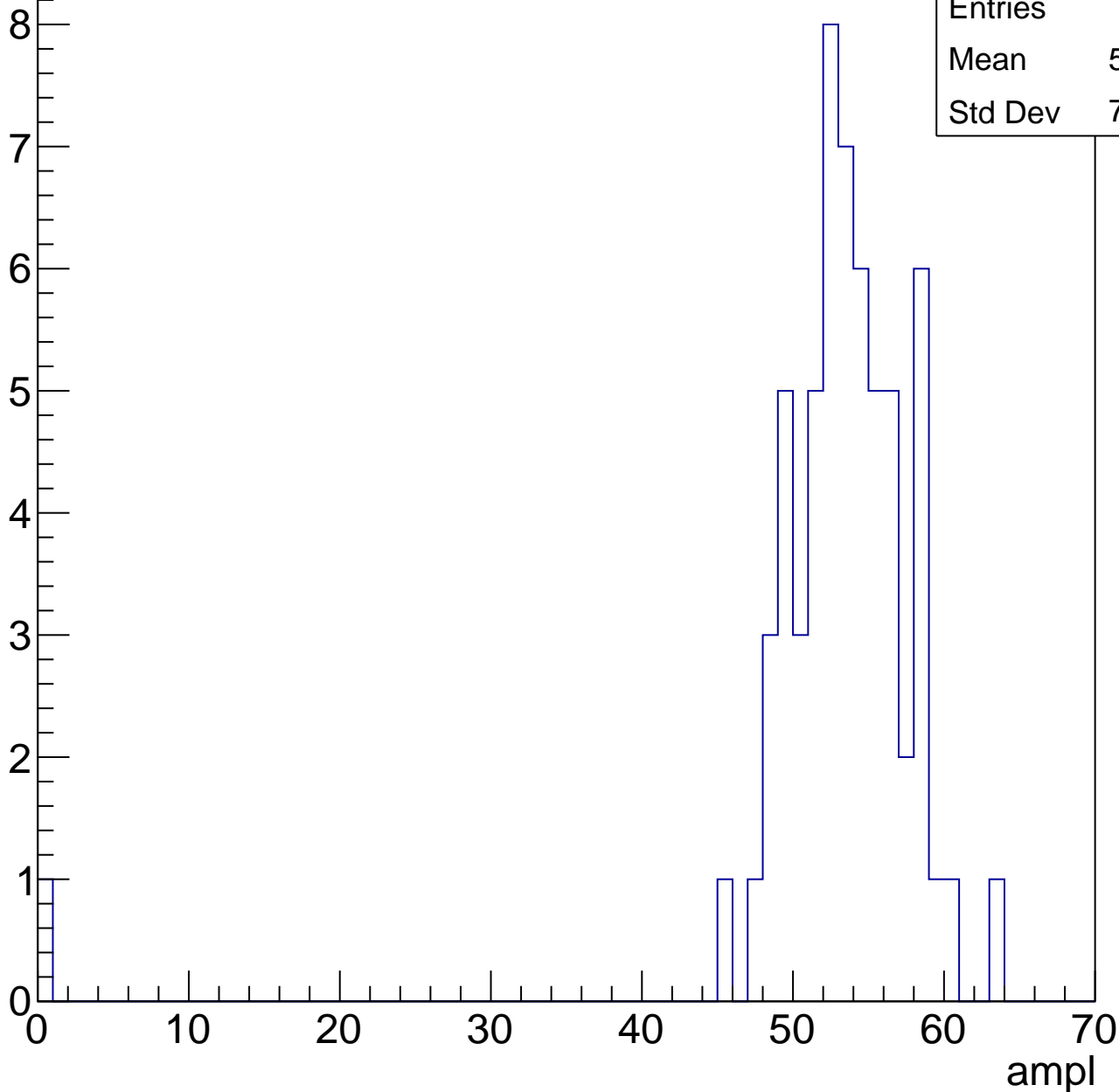


# B1L103S, U4-ch74, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 61    |
| Mean    | 52.39 |
| Std Dev | 7.612 |

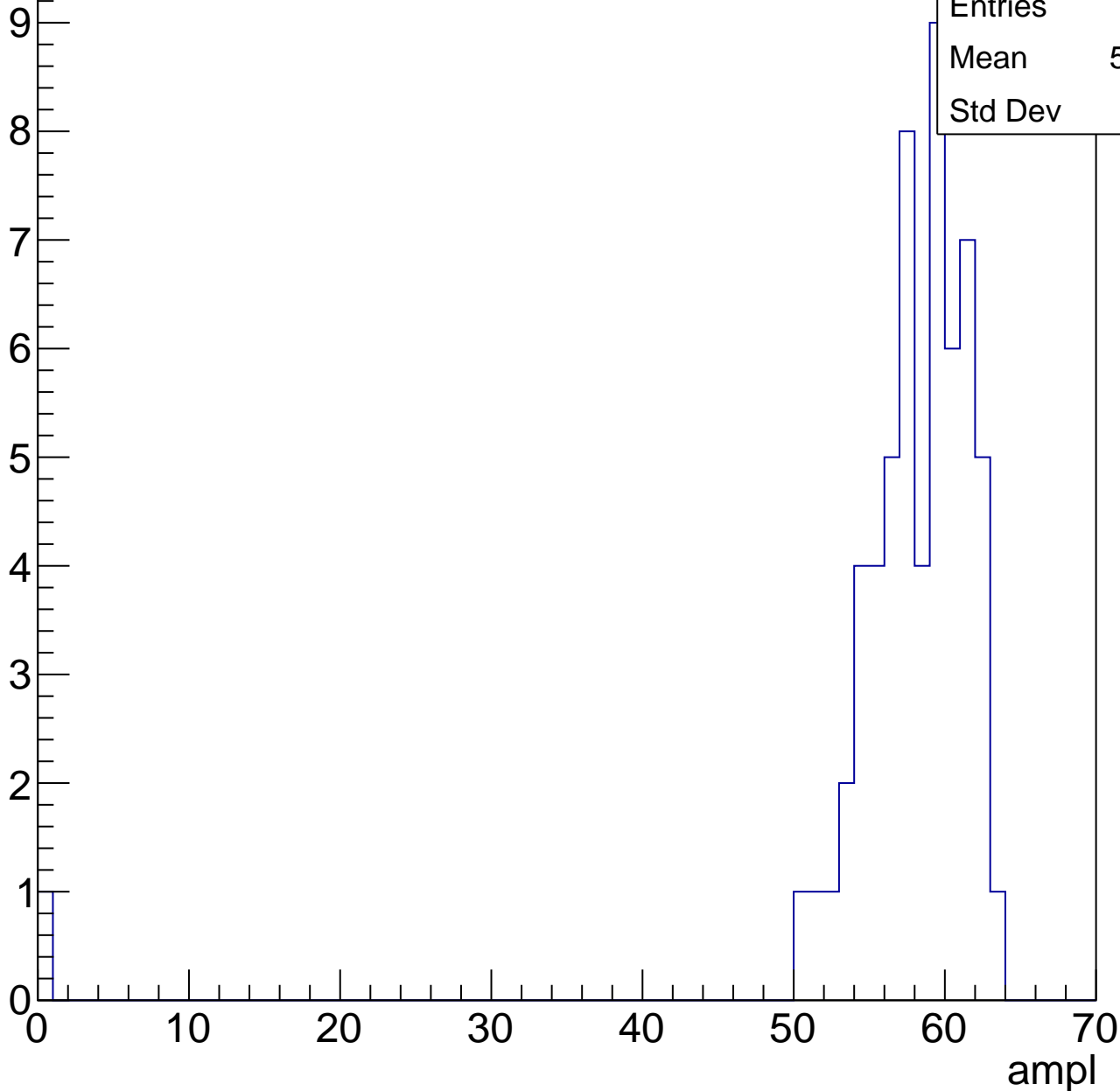


# B1L103S, U4-ch74, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 59    |
| Mean    | 56.85 |
| Std Dev | 8.04  |

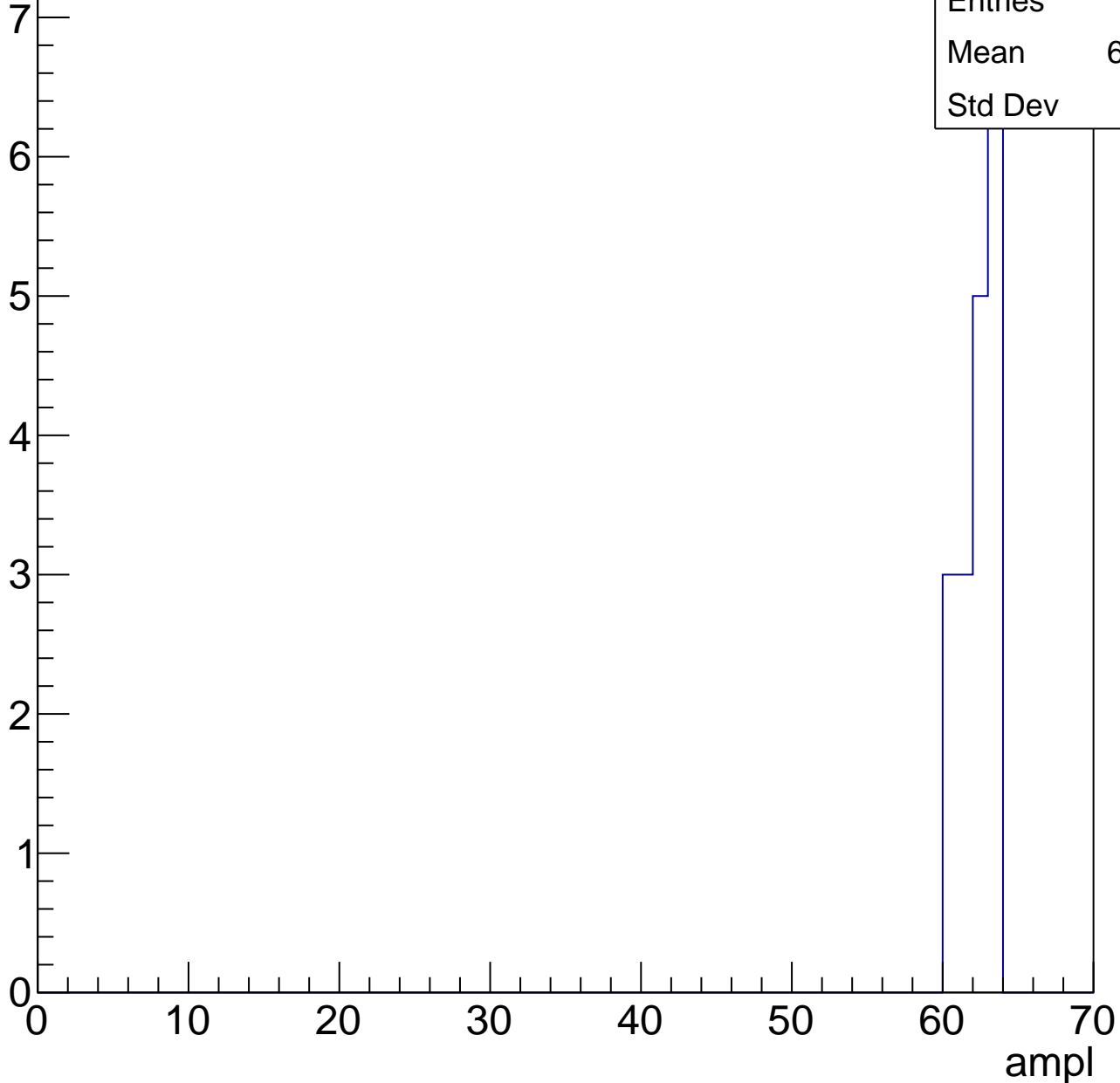


# B1L103S, U4-ch74, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 18    |
| Mean    | 61.89 |
| Std Dev | 1.1   |





# B1L103S, U4-ch74, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 20    |
| Mean    | 3.15  |
| Std Dev | 13.73 |

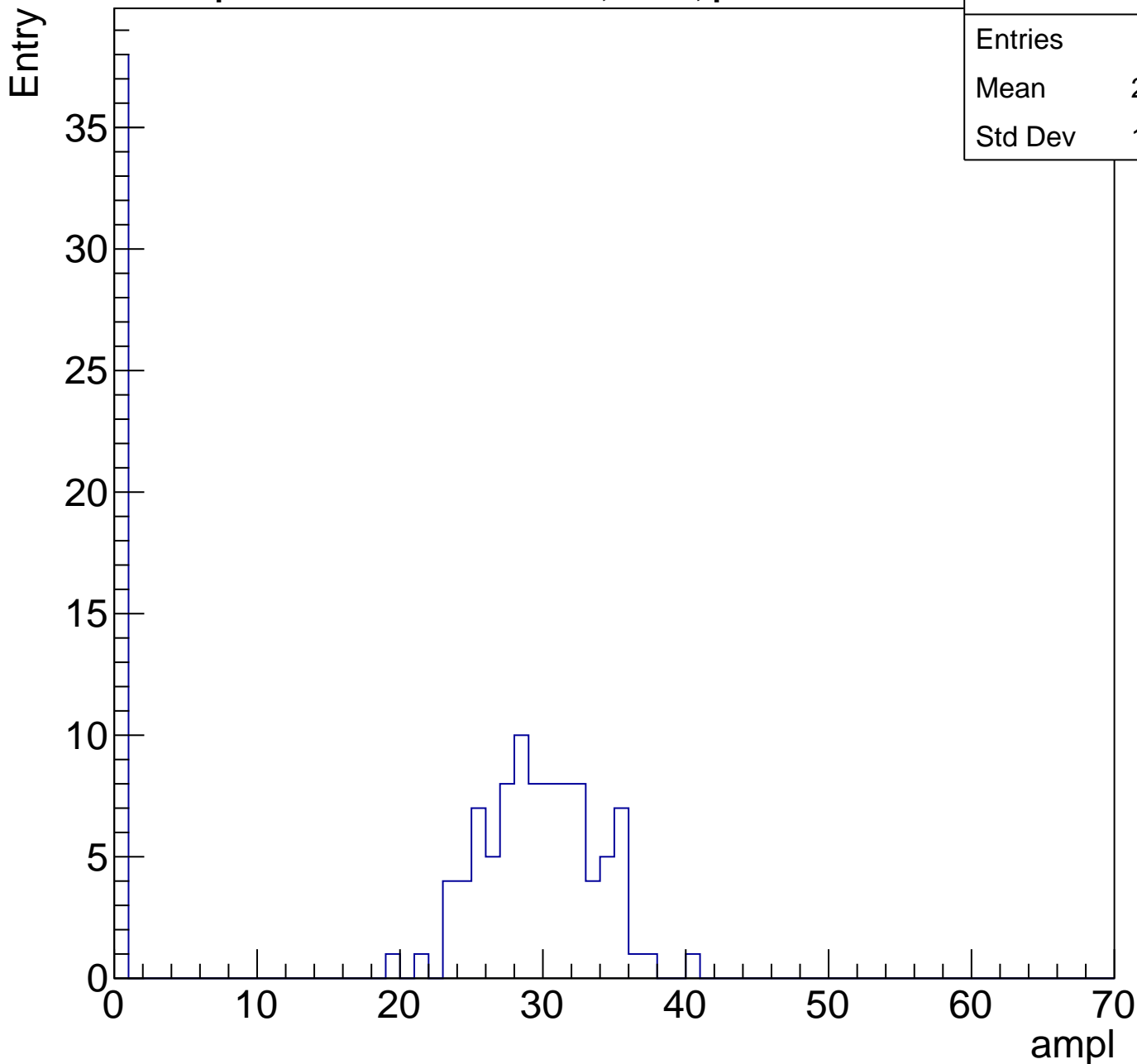
Entry



# B1L103S, U4-ch75, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 129   |
| Mean    | 20.66 |
| Std Dev | 13.75 |



# B1L103S, U4-ch75, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

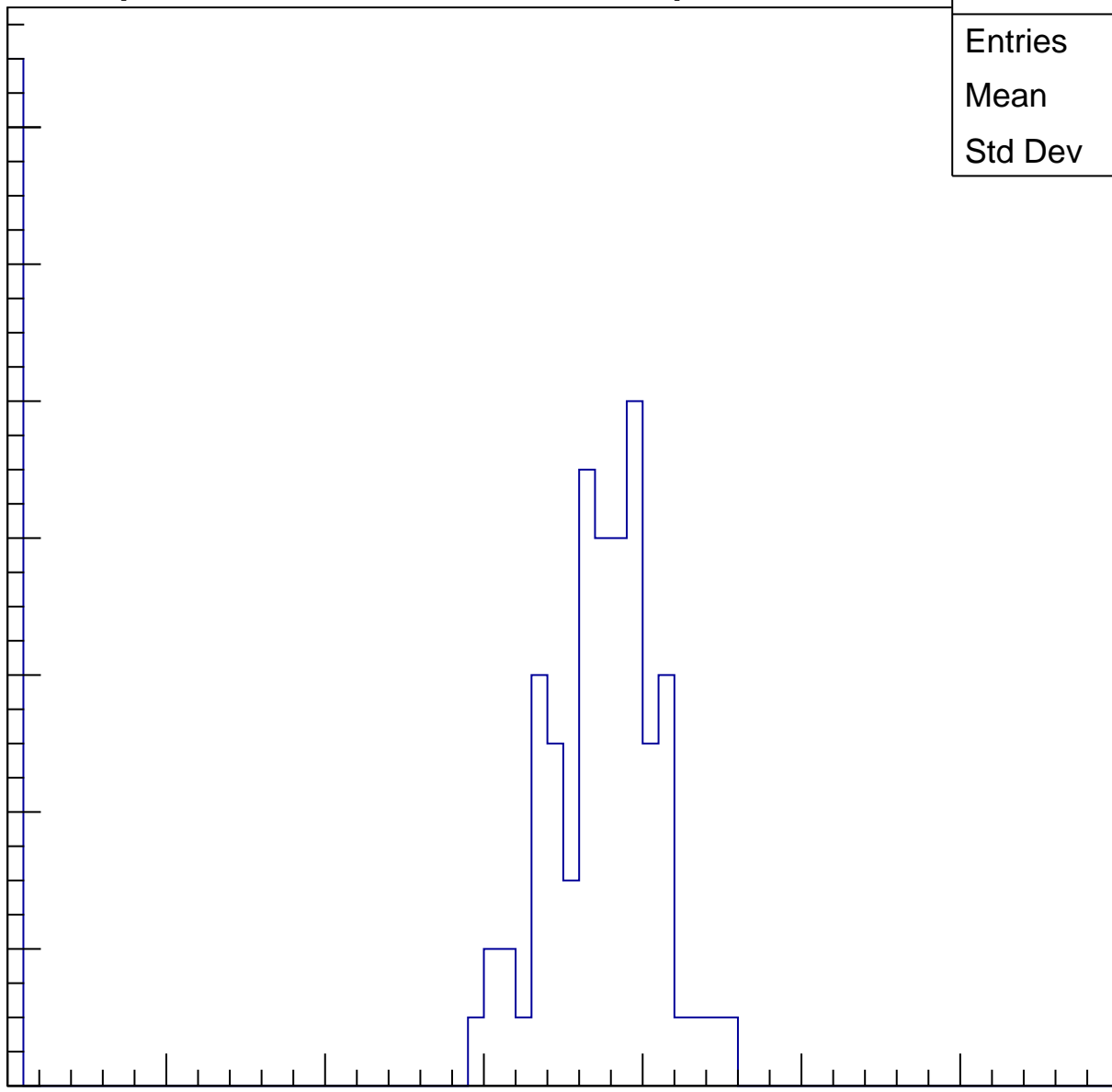
|         |       |
|---------|-------|
| Entries | 85    |
| Mean    | 30.47 |
| Std Dev | 14.43 |

Entry

14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

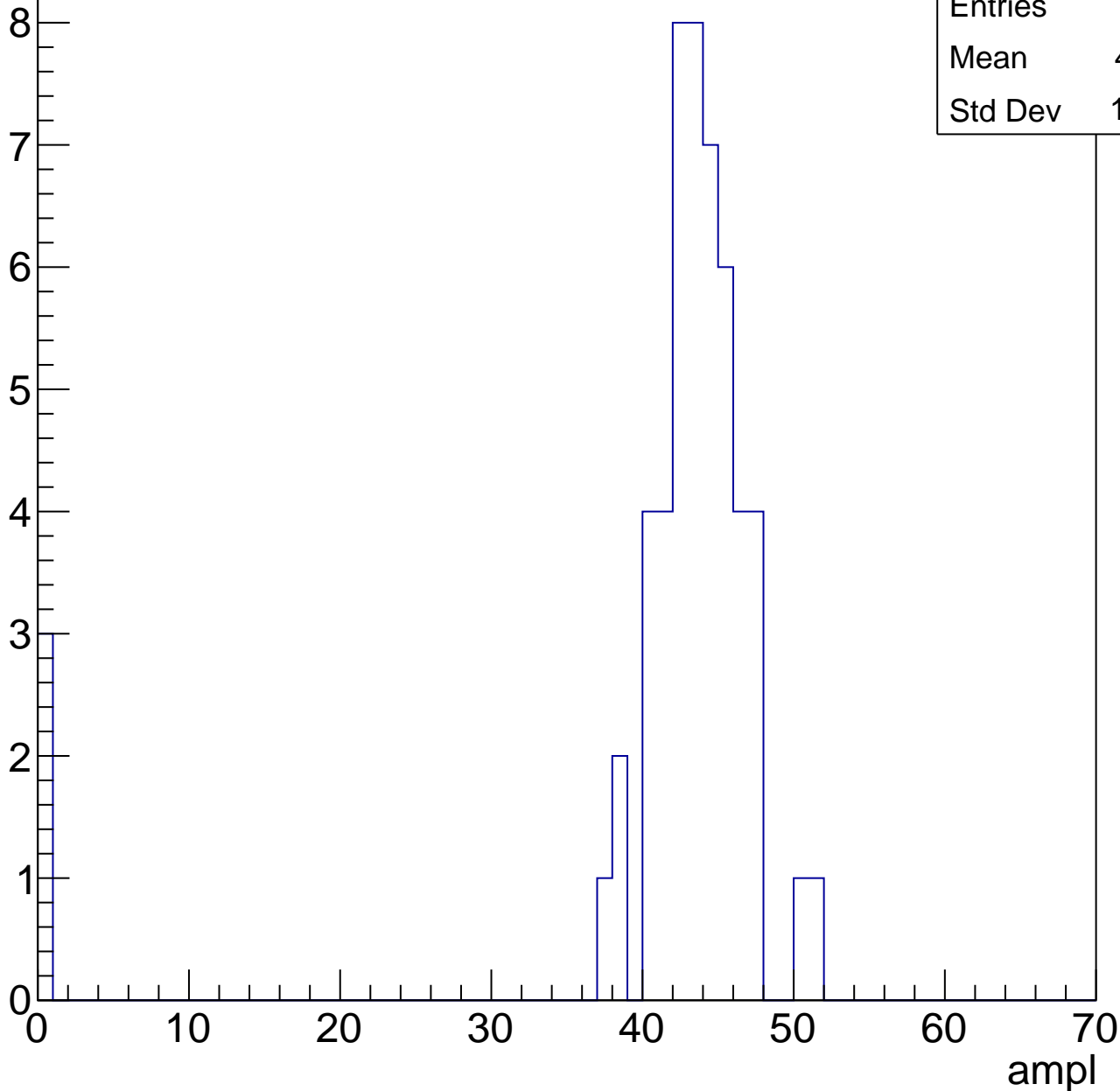


# B1L103S, U4-ch75, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 53    |
| Mean    | 40.91 |
| Std Dev | 10.37 |

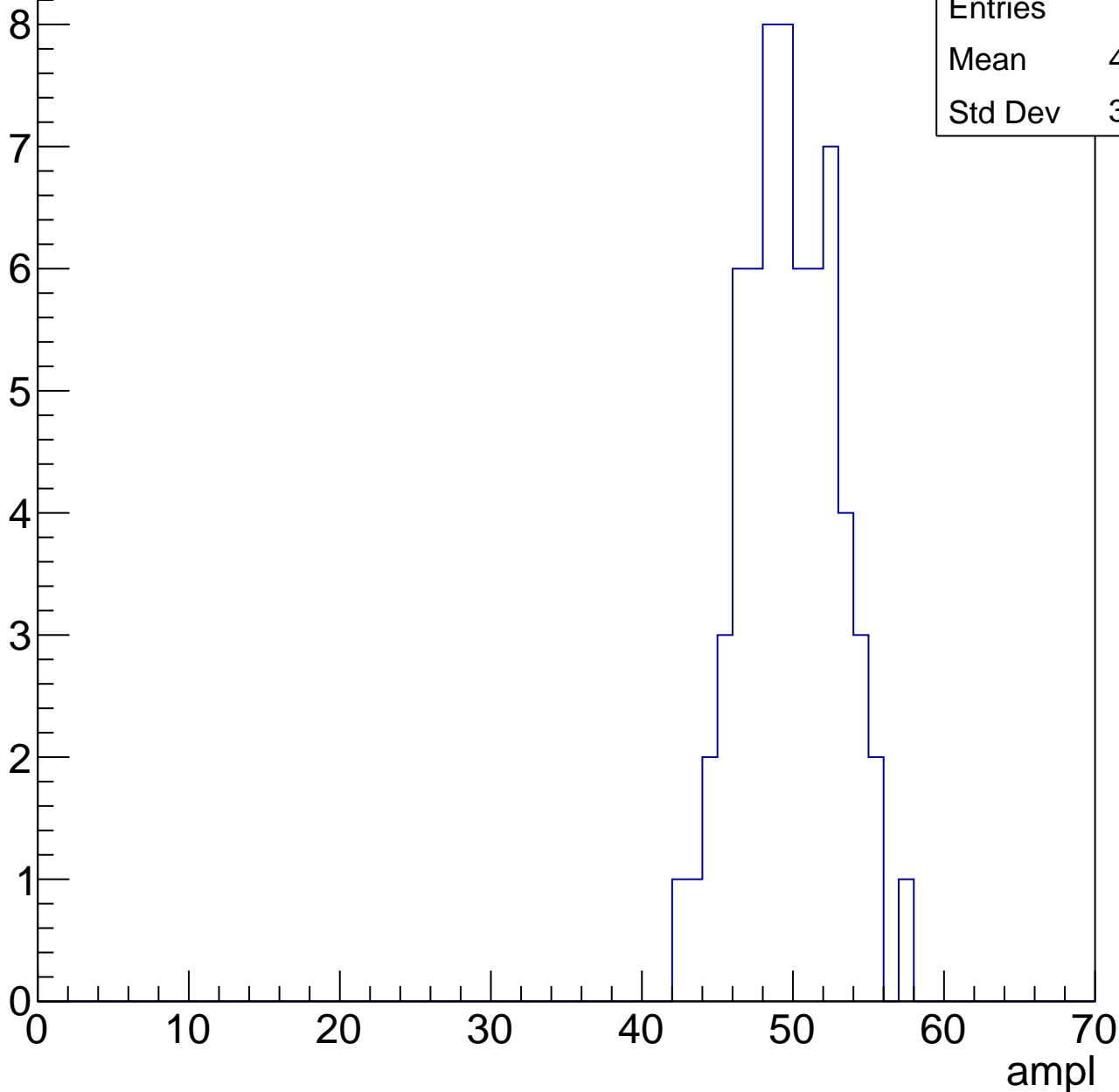


# B1L103S, U4-ch75, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 64    |
| Mean    | 49.27 |
| Std Dev | 3.144 |

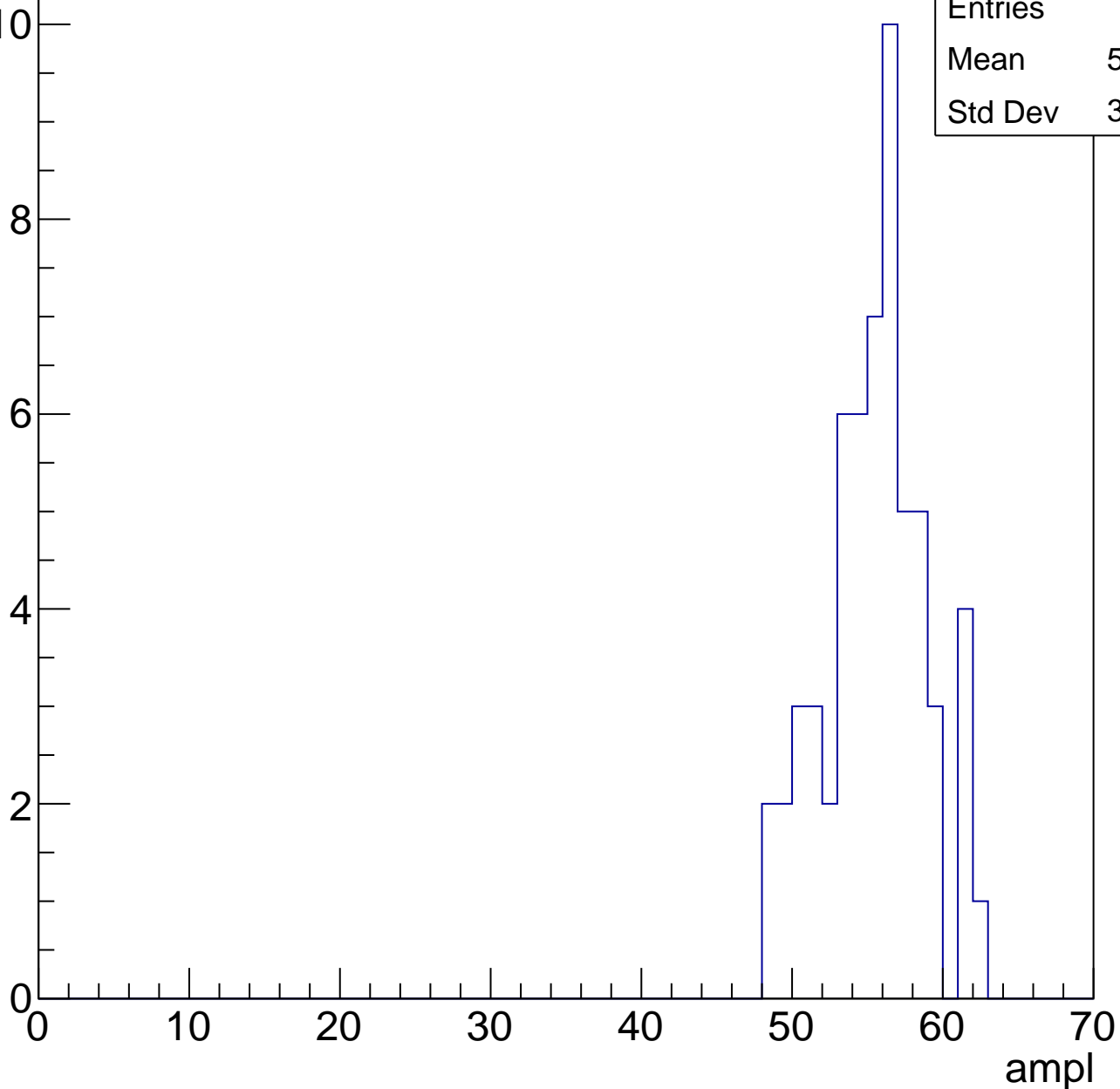


# B1L103S, U4-ch75, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 59    |
| Mean    | 55.02 |
| Std Dev | 3.337 |

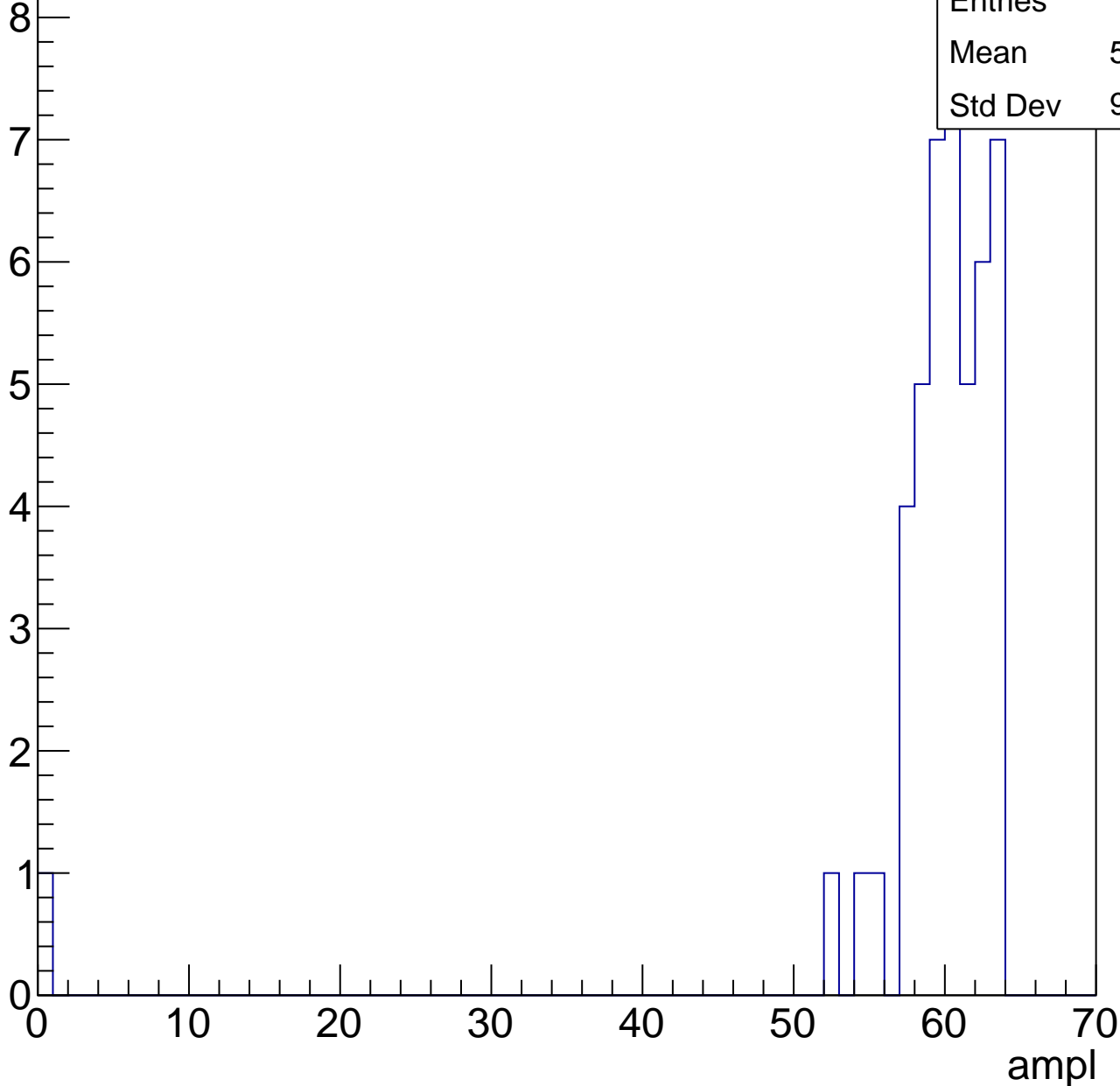


# B1L103S, U4-ch75, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

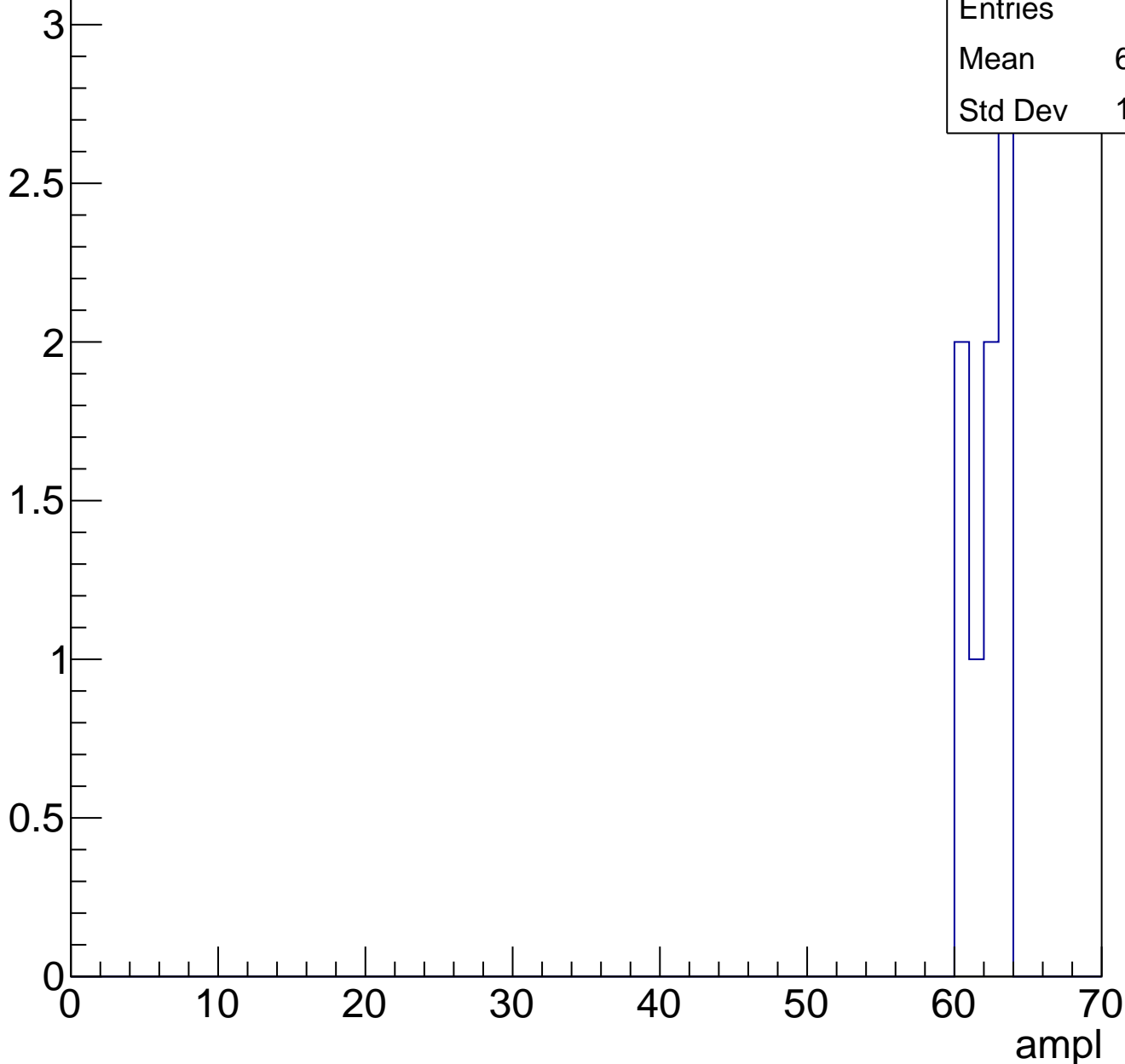
|         |       |
|---------|-------|
| Entries | 46    |
| Mean    | 58.48 |
| Std Dev | 9.057 |



# B1L103S, U4-ch75, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

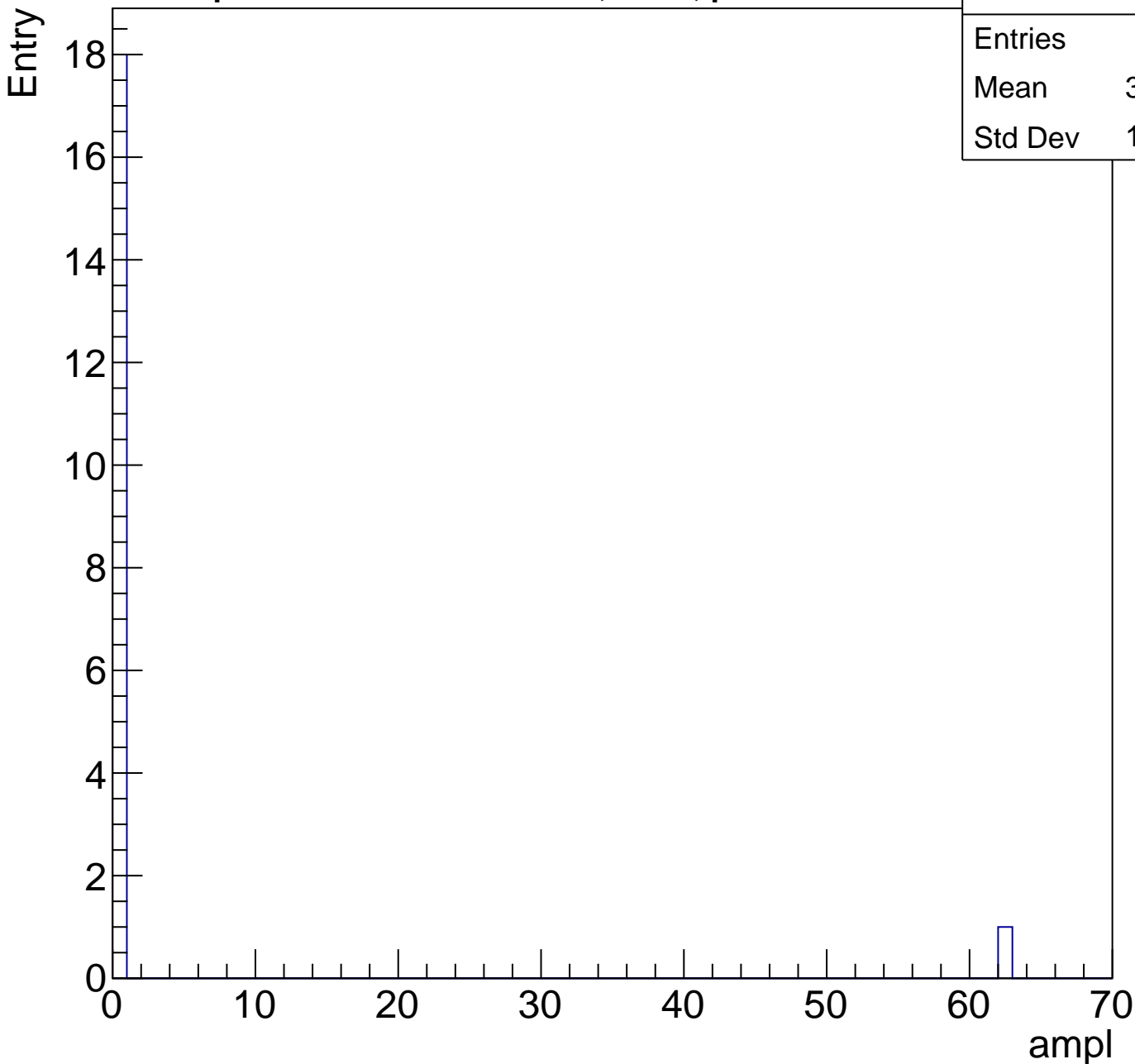




# B1L103S, U4-ch75, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

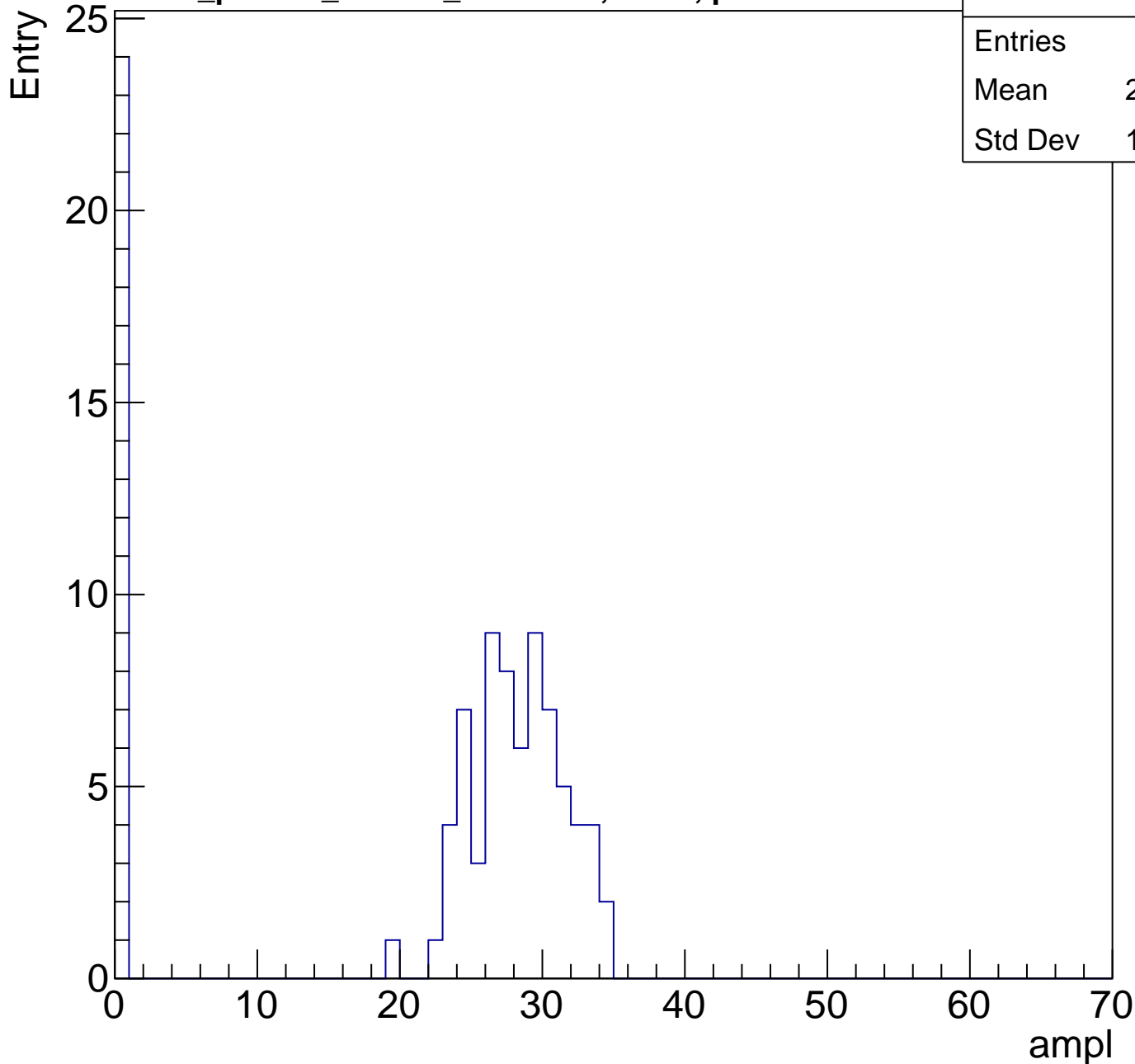
|         |       |
|---------|-------|
| Entries | 19    |
| Mean    | 3.263 |
| Std Dev | 13.84 |



# B1L103S, U4-ch76, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 94    |
| Mean    | 20.72 |
| Std Dev | 12.44 |



# B1L103S, U4-ch76, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

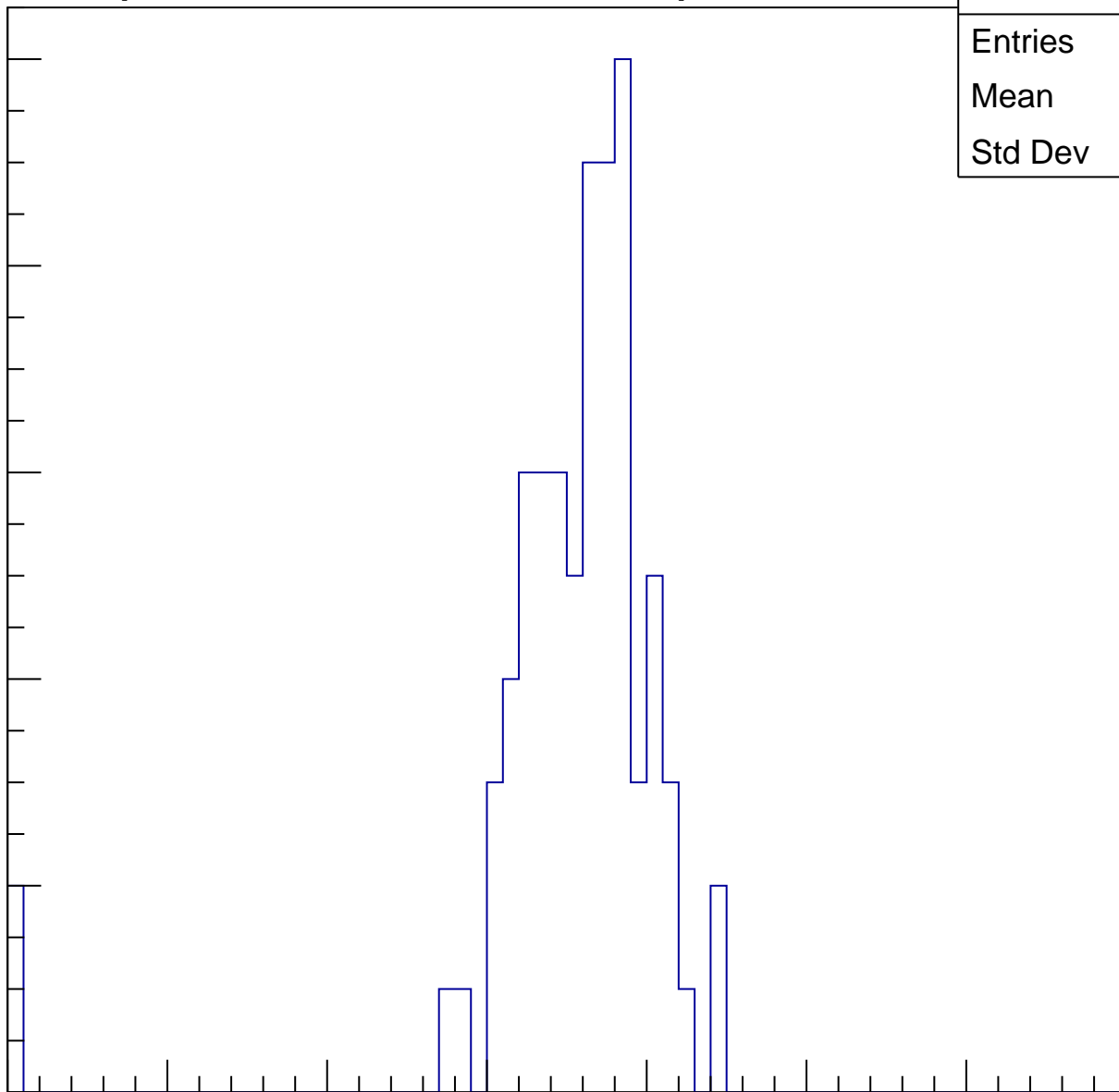
|         |       |
|---------|-------|
| Entries | 76    |
| Mean    | 34.8  |
| Std Dev | 6.698 |

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L103S, U4-ch76, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

10

8

6

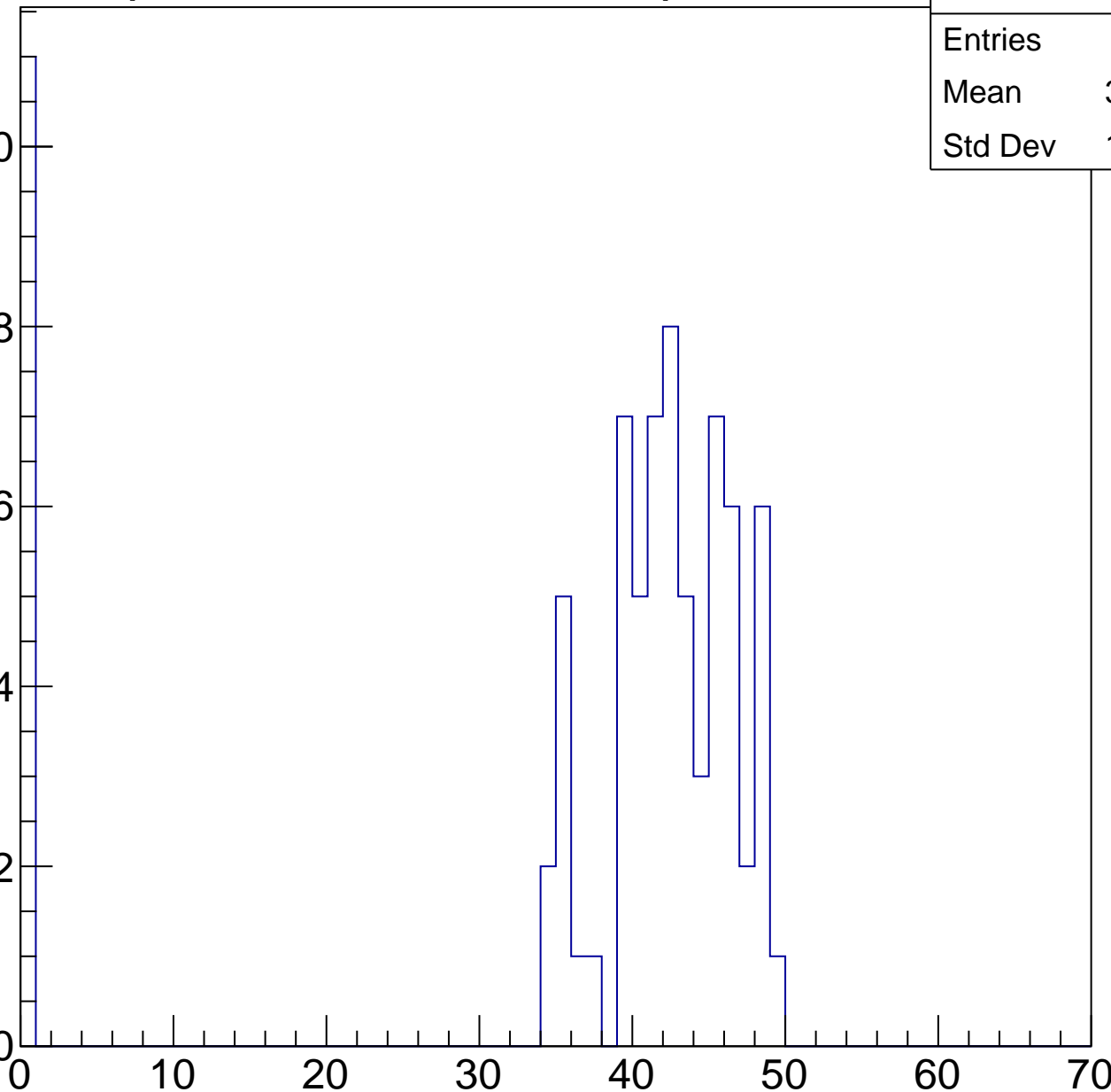
4

2

0

|         |       |
|---------|-------|
| Entries | 77    |
| Mean    | 36.12 |
| Std Dev | 15.18 |

ampl

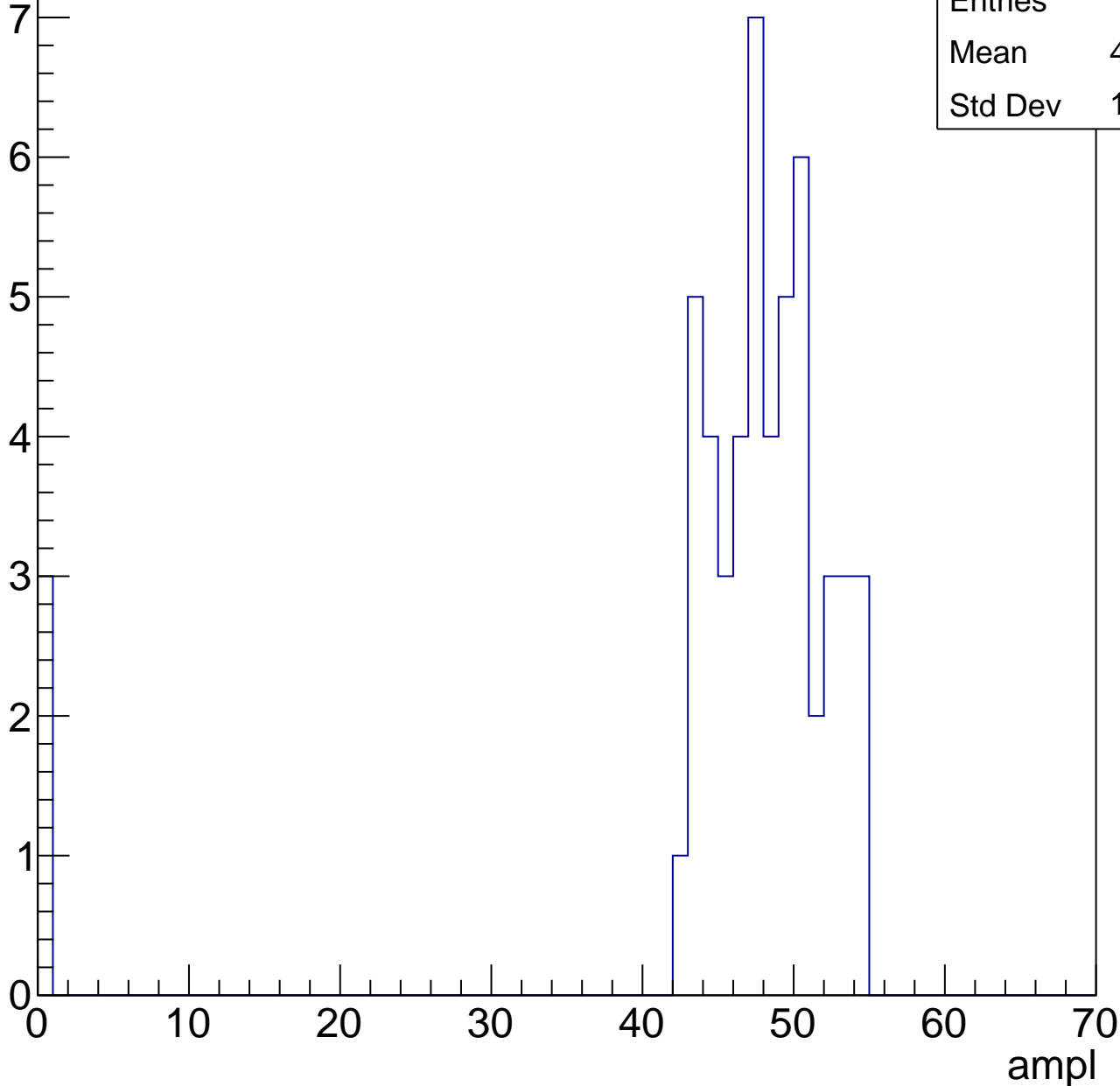


# B1L103S, U4-ch76, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

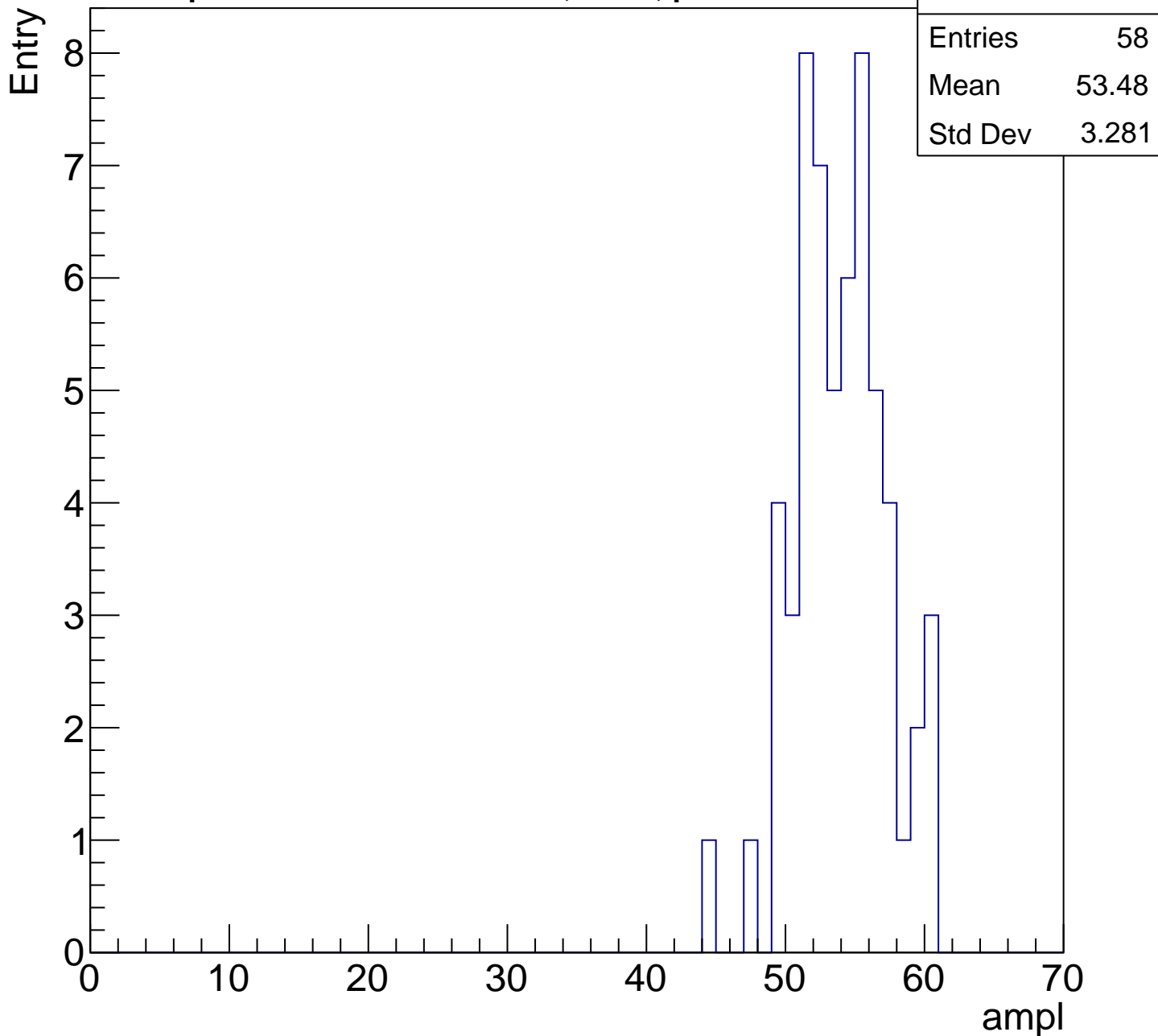
Entry

|         |       |
|---------|-------|
| Entries | 53    |
| Mean    | 45.23 |
| Std Dev | 11.54 |



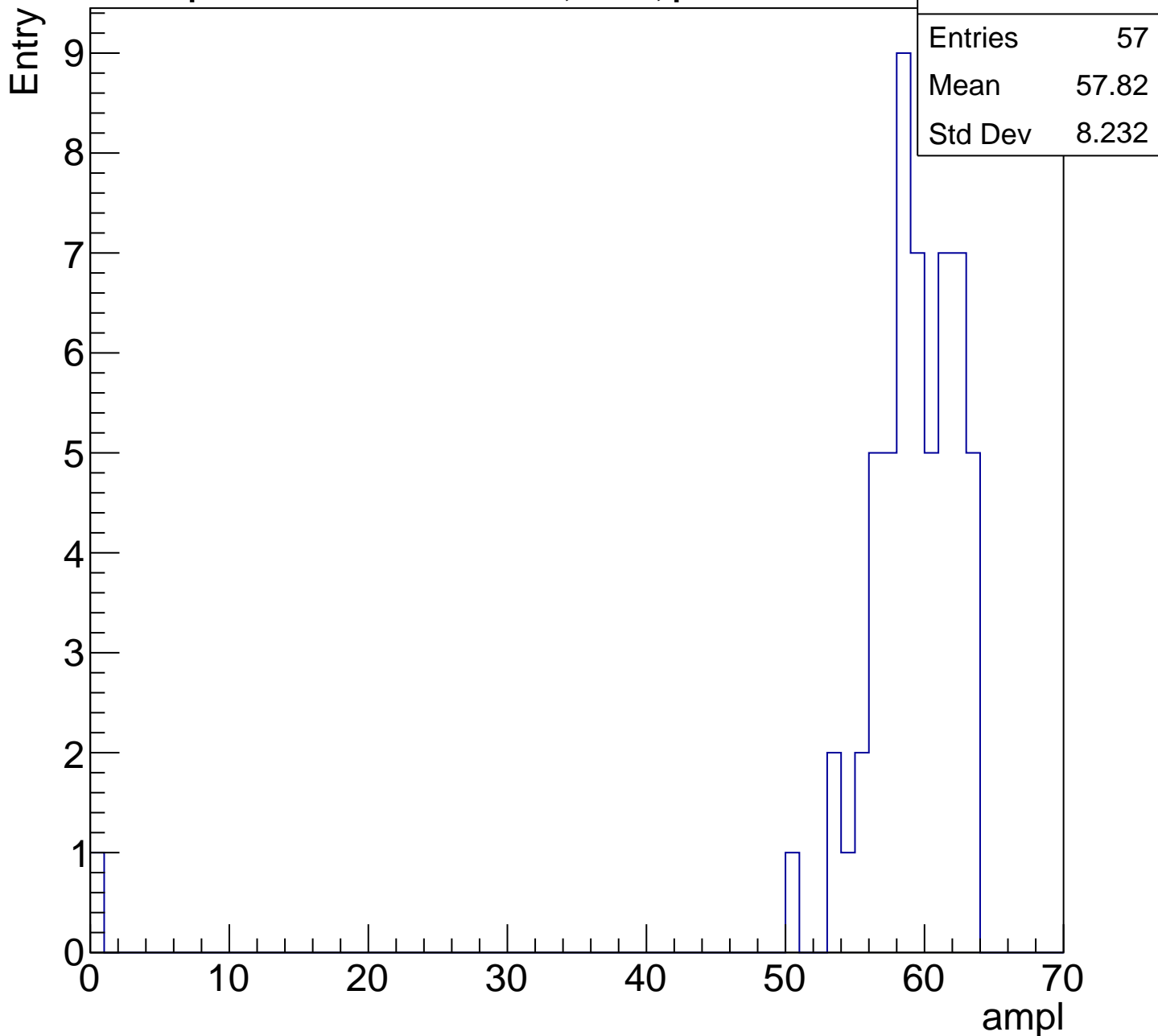
# B1L103S, U4-ch76, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2



# B1L103S, U4-ch76, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

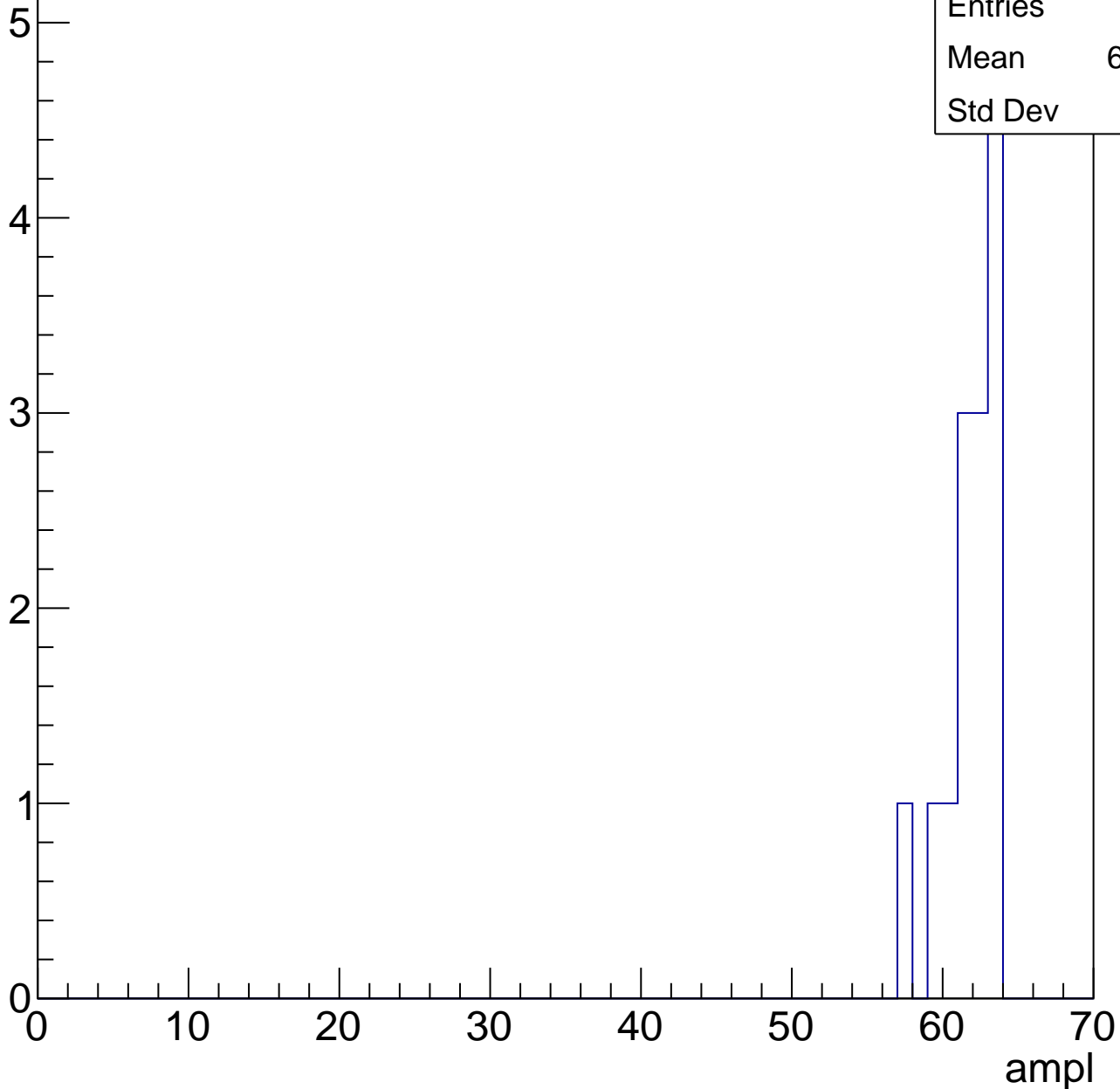


# B1L103S, U4-ch76, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 14    |
| Mean    | 61.43 |
| Std Dev | 1.72  |





# B1L103S, U4-ch76, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 20    |
| Mean    | 3     |
| Std Dev | 13.08 |

Entry

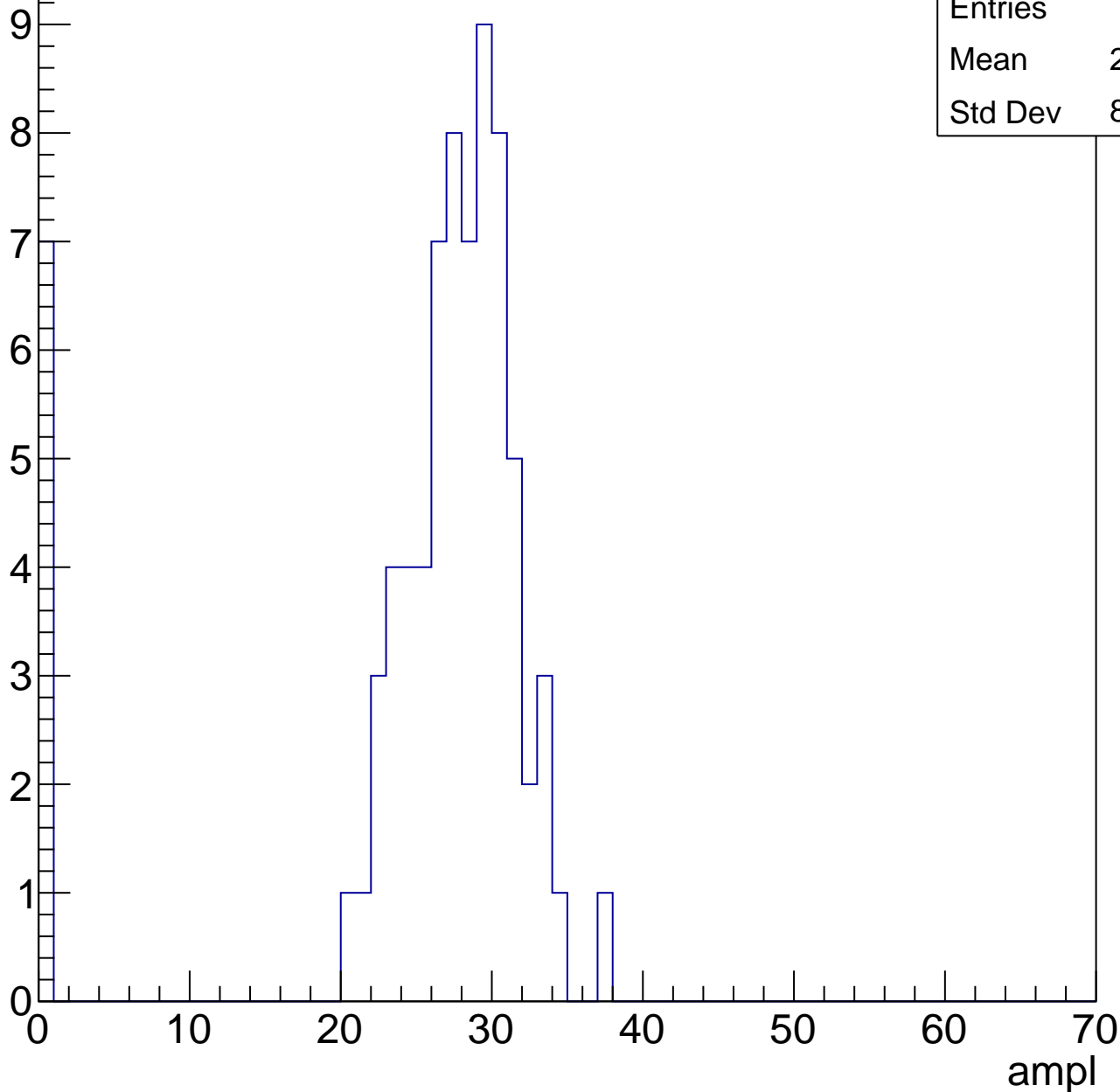


# B1L103S, U4-ch77, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 75    |
| Mean    | 25.05 |
| Std Dev | 8.644 |

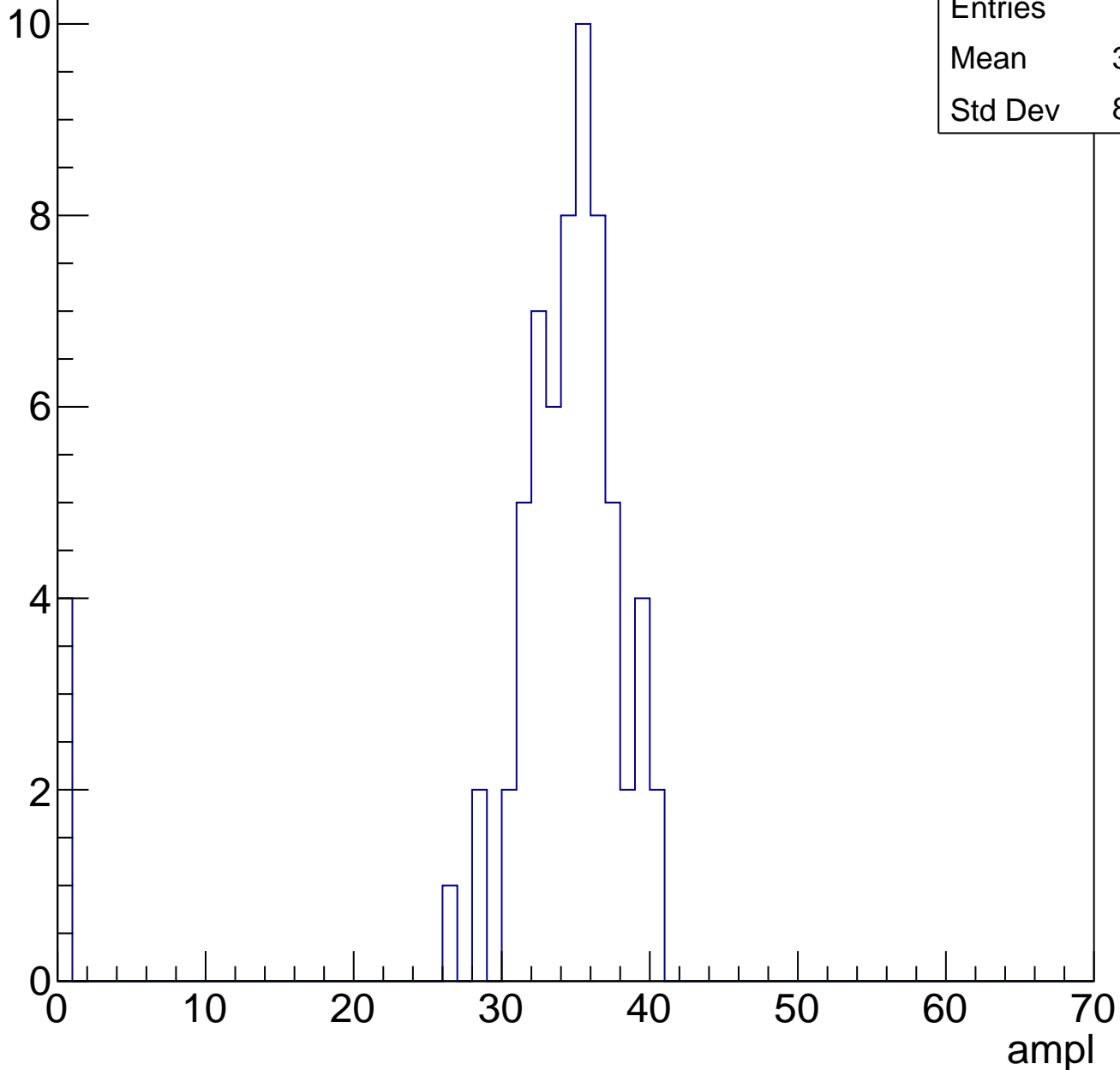


# B1L103S, U4-ch77, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 66    |
| Mean    | 32.21 |
| Std Dev | 8.661 |

Entry

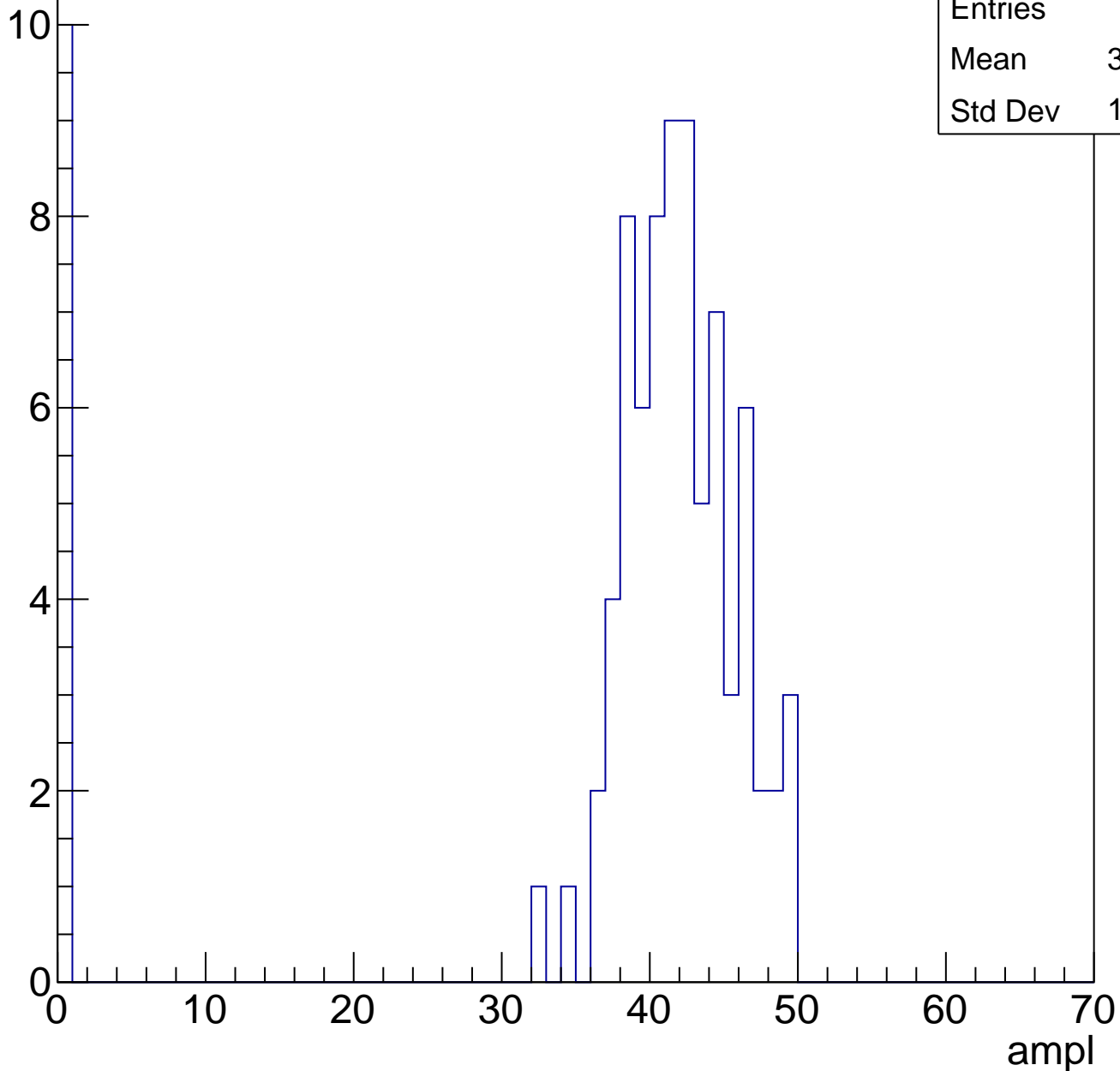


# B1L103S, U4-ch77, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

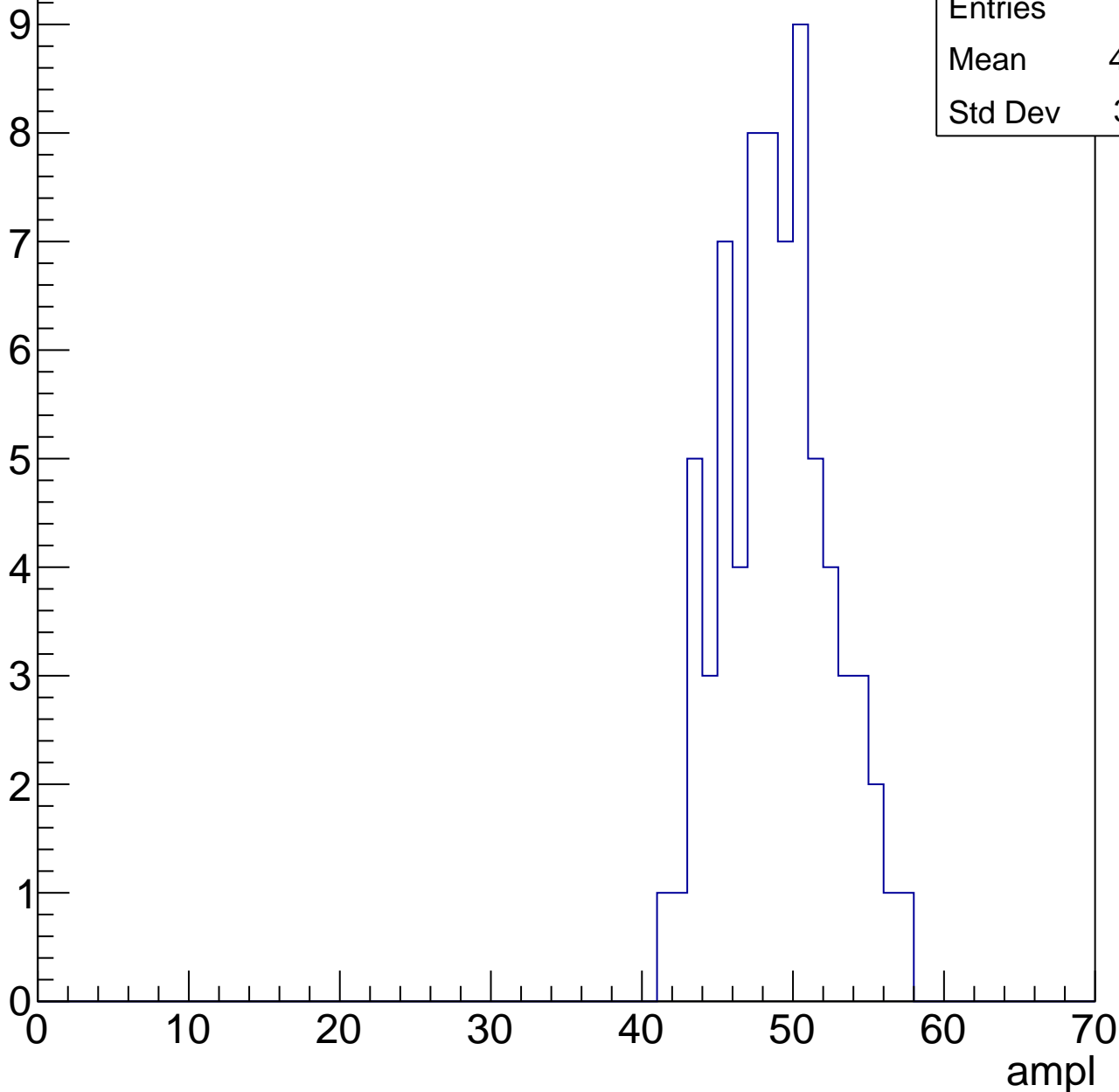
|         |       |
|---------|-------|
| Entries | 86    |
| Mean    | 36.77 |
| Std Dev | 13.75 |



# B1L103S, U4-ch77, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



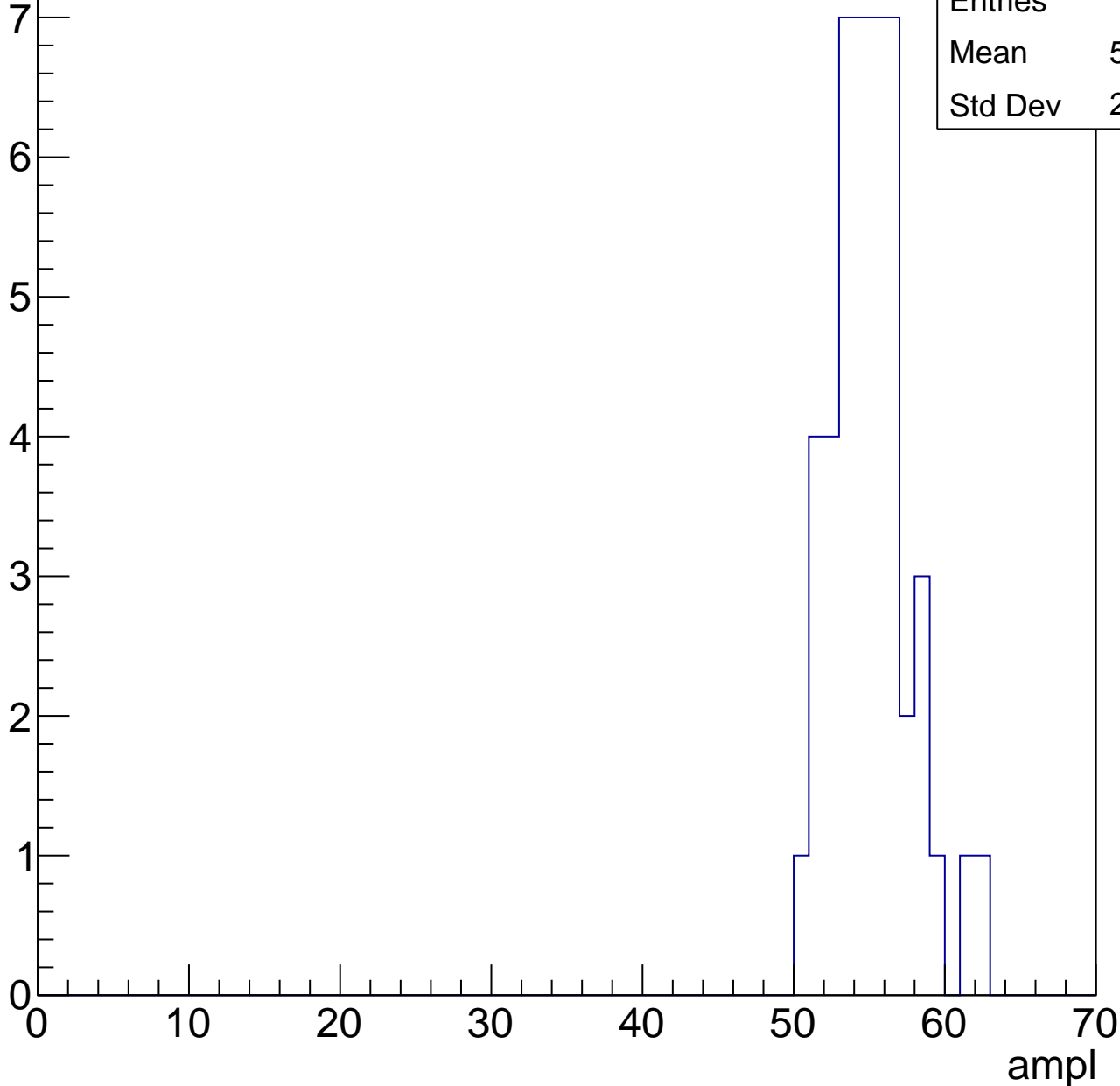
|         |       |
|---------|-------|
| Entries | 72    |
| Mean    | 48.46 |
| Std Dev | 3.551 |

# B1L103S, U4-ch77, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 45    |
| Mean    | 54.62 |
| Std Dev | 2.567 |



# B1L103S, U4-ch77, adc5

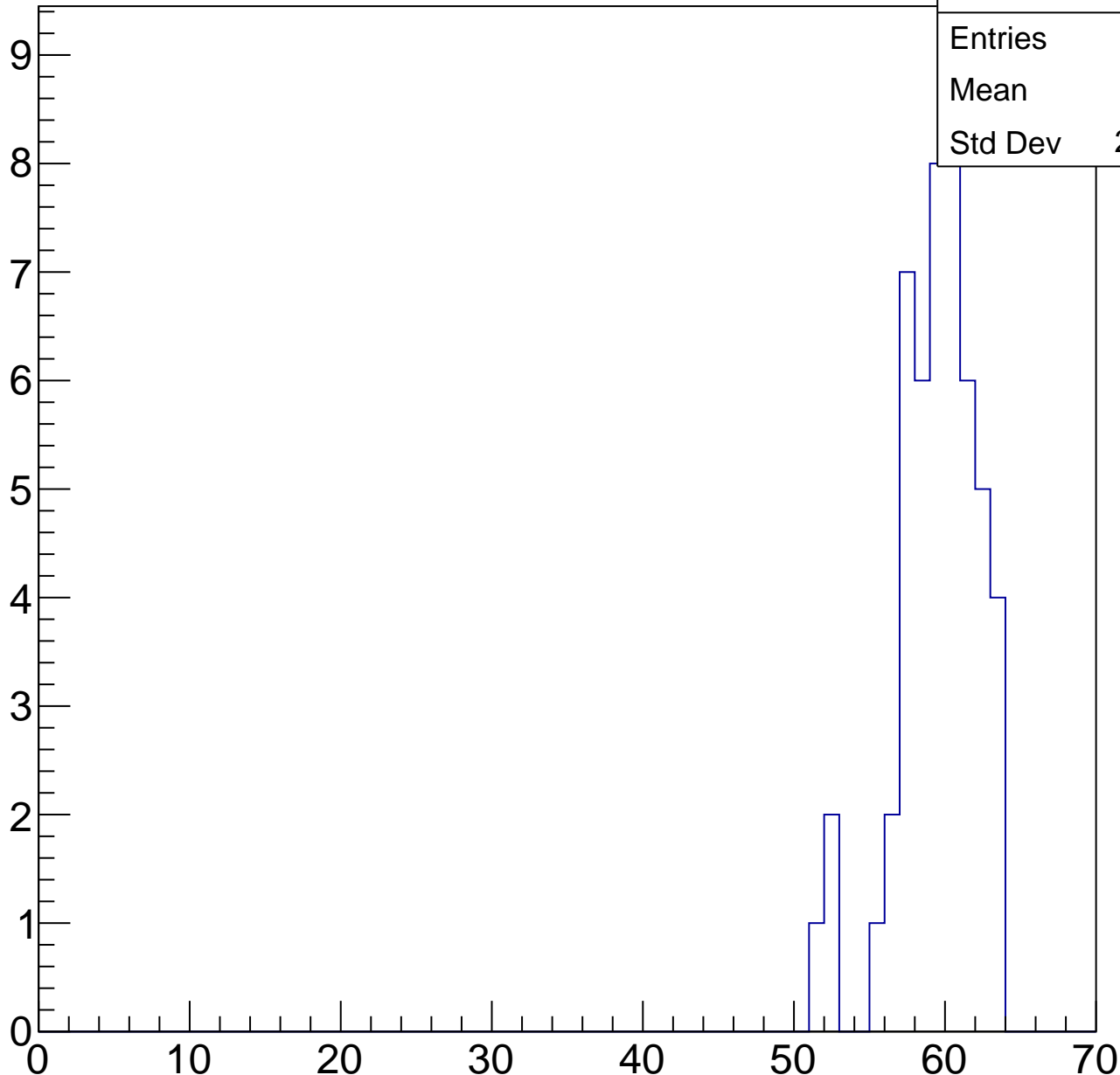
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

|         |       |
|---------|-------|
| Entries | 51    |
| Mean    | 59    |
| Std Dev | 2.701 |

ampl

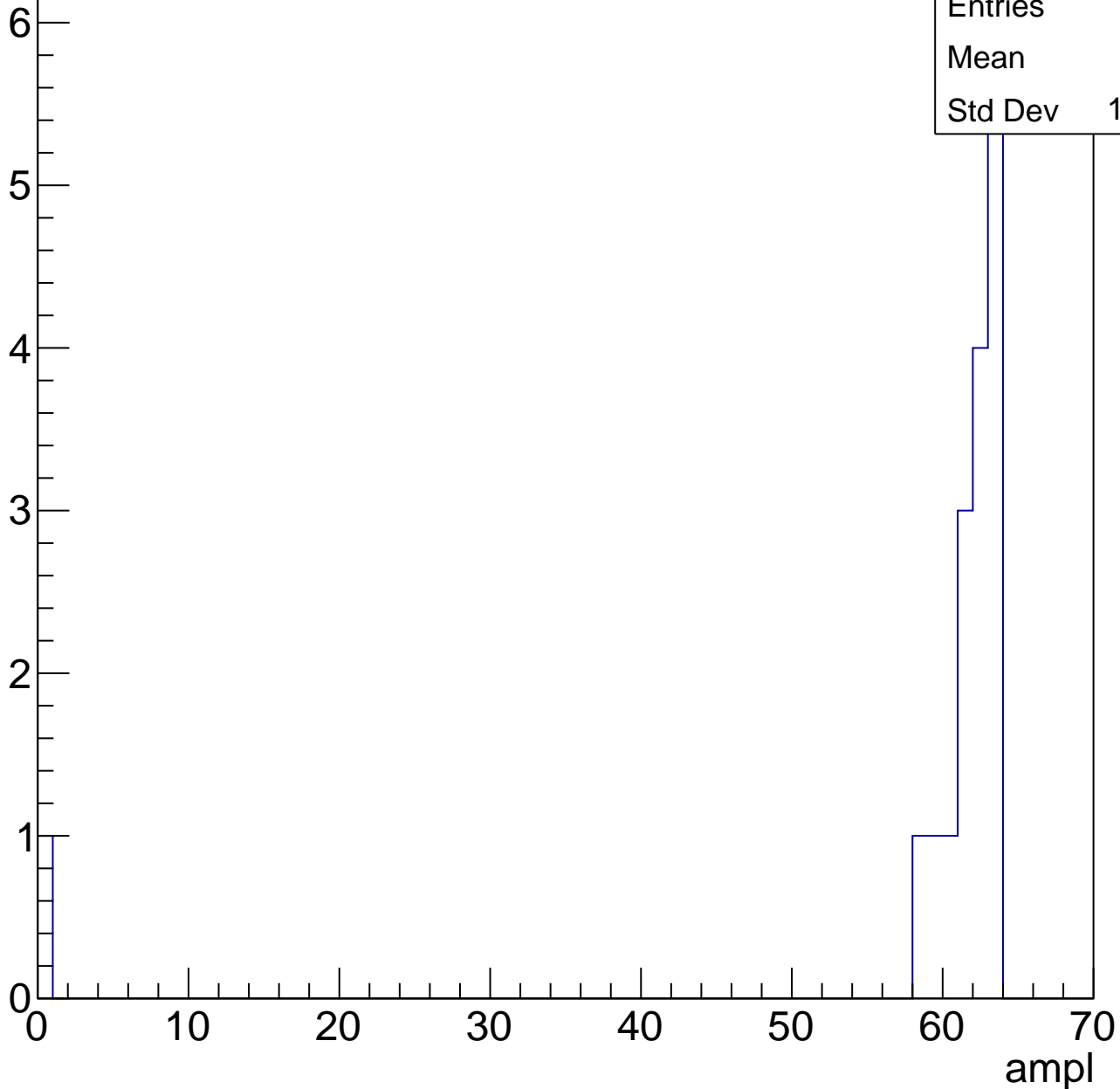


# B1L103S, U4-ch77, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 17    |
| Mean    | 58    |
| Std Dev | 14.57 |





# B1L103S, U4-ch77, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



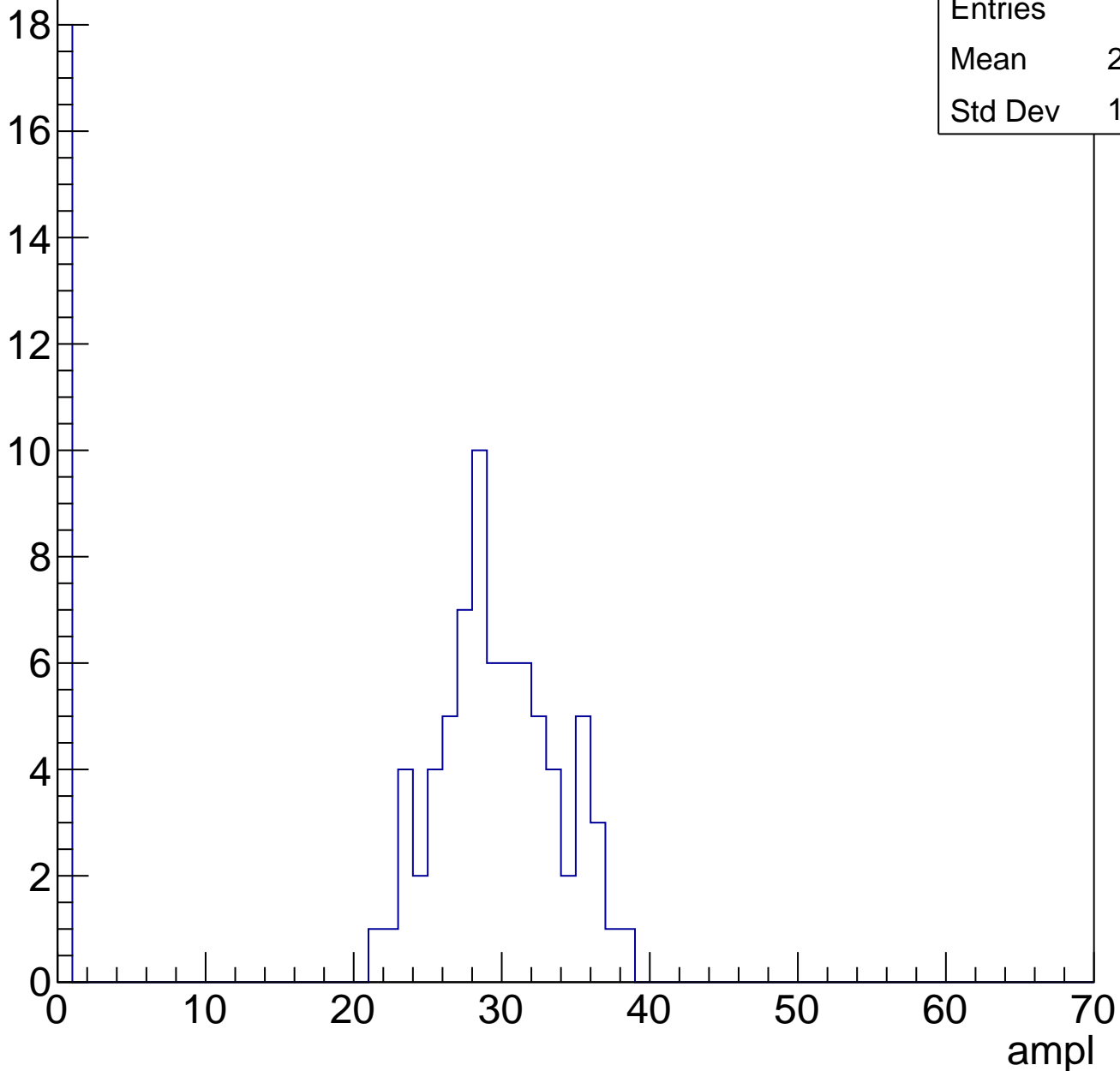
|         |    |
|---------|----|
| Entries | 18 |
| Mean    | 0  |
| Std Dev | 0  |

# B1L103S, U4-ch78, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 91    |
| Mean    | 23.52 |
| Std Dev | 12.19 |

Entry

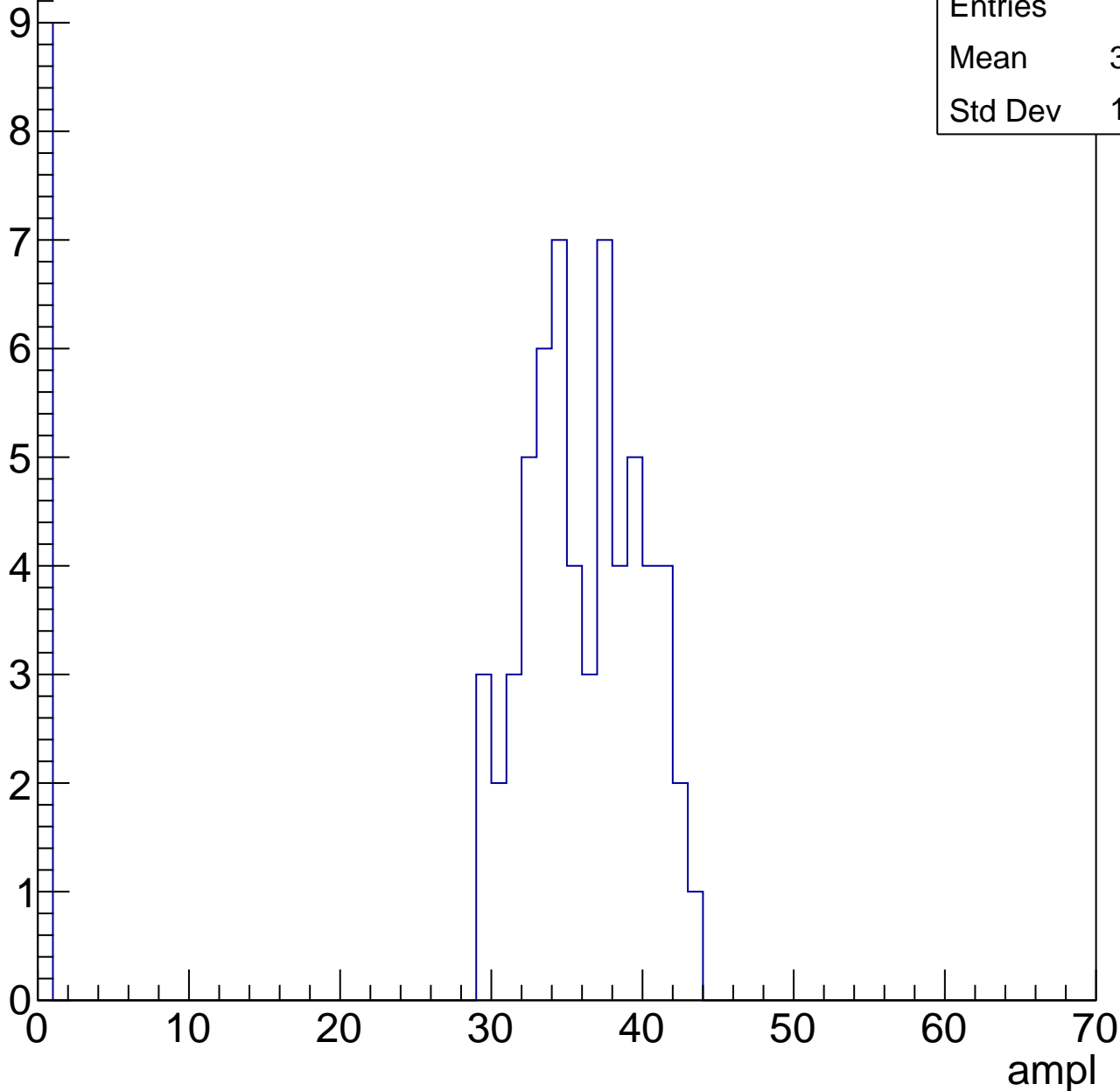


# B1L103S, U4-ch78, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 69    |
| Mean    | 31.03 |
| Std Dev | 12.49 |

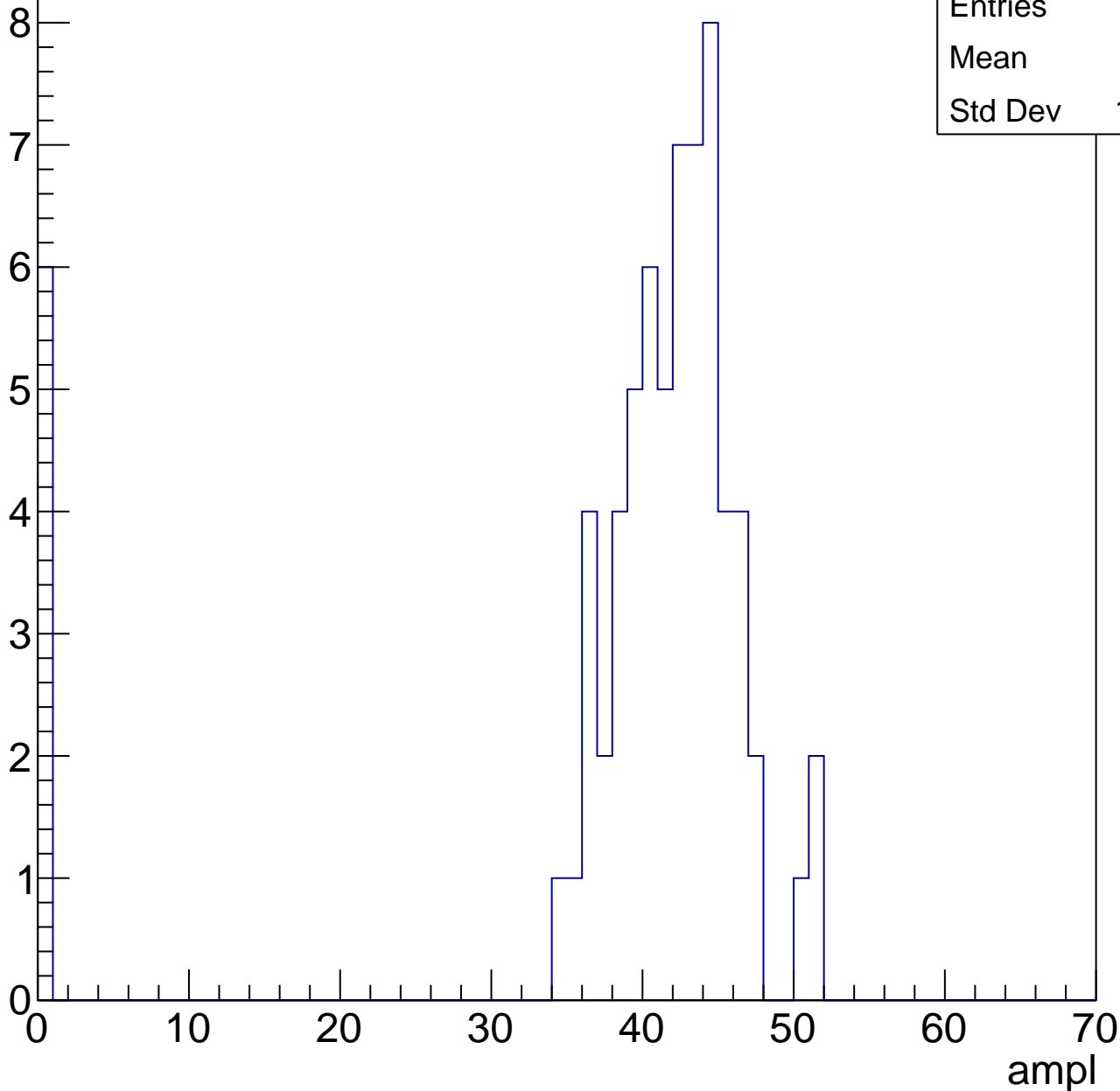


# B1L103S, U4-ch78, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 69    |
| Mean    | 38.2  |
| Std Dev | 12.31 |

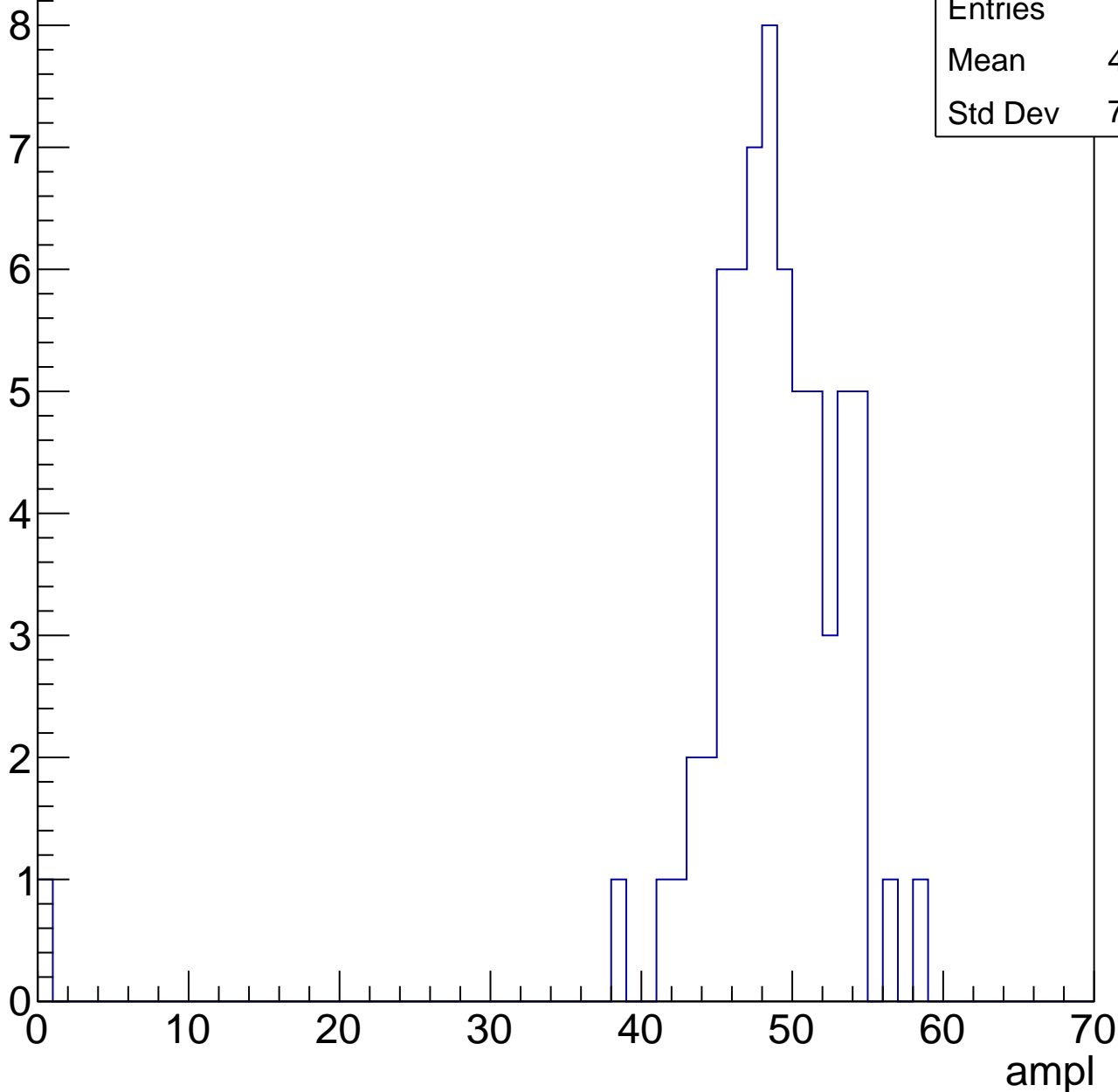


# B1L103S, U4-ch78, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

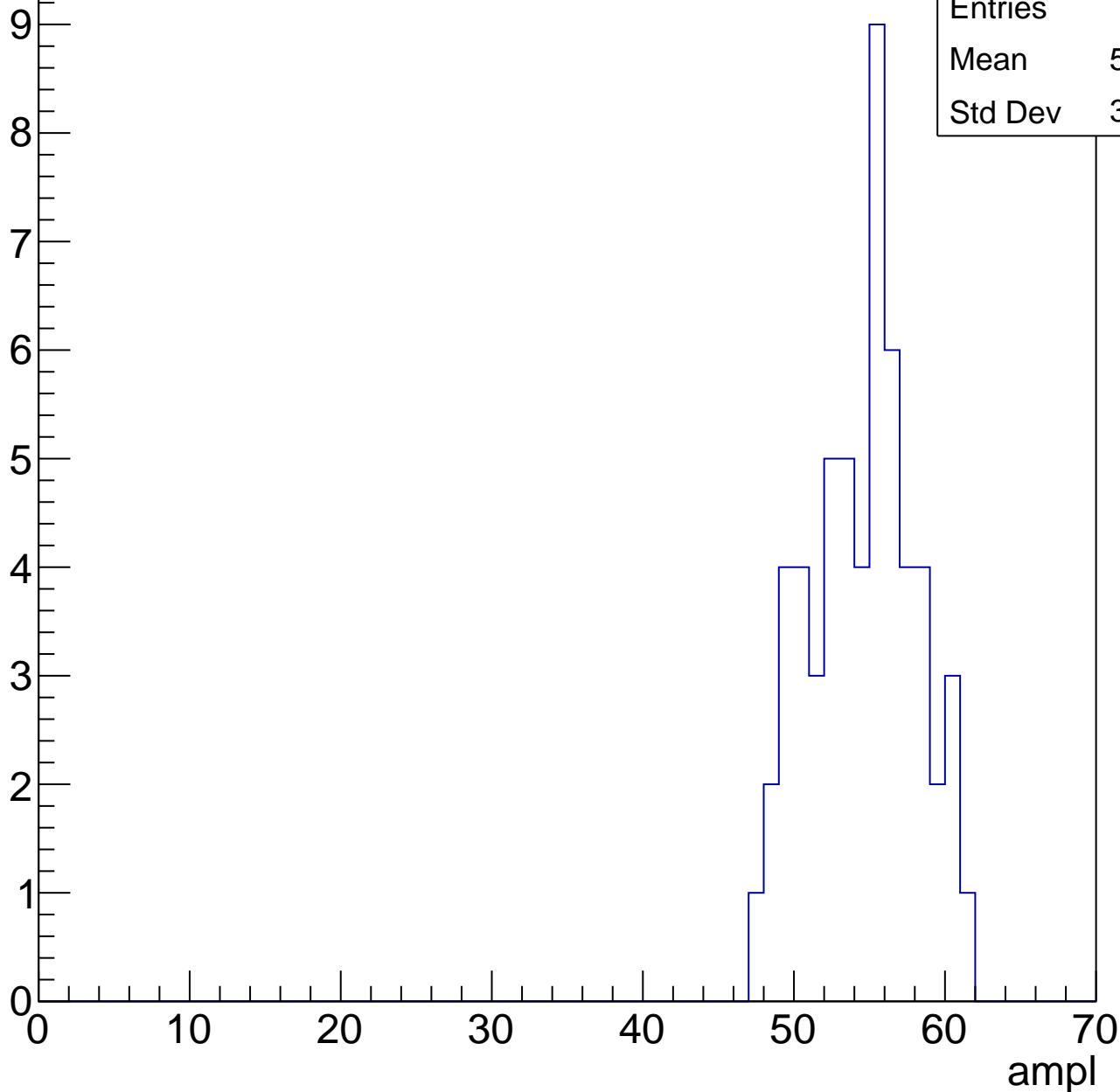
|         |       |
|---------|-------|
| Entries | 66    |
| Mean    | 47.85 |
| Std Dev | 7.009 |



# B1L103S, U4-ch78, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

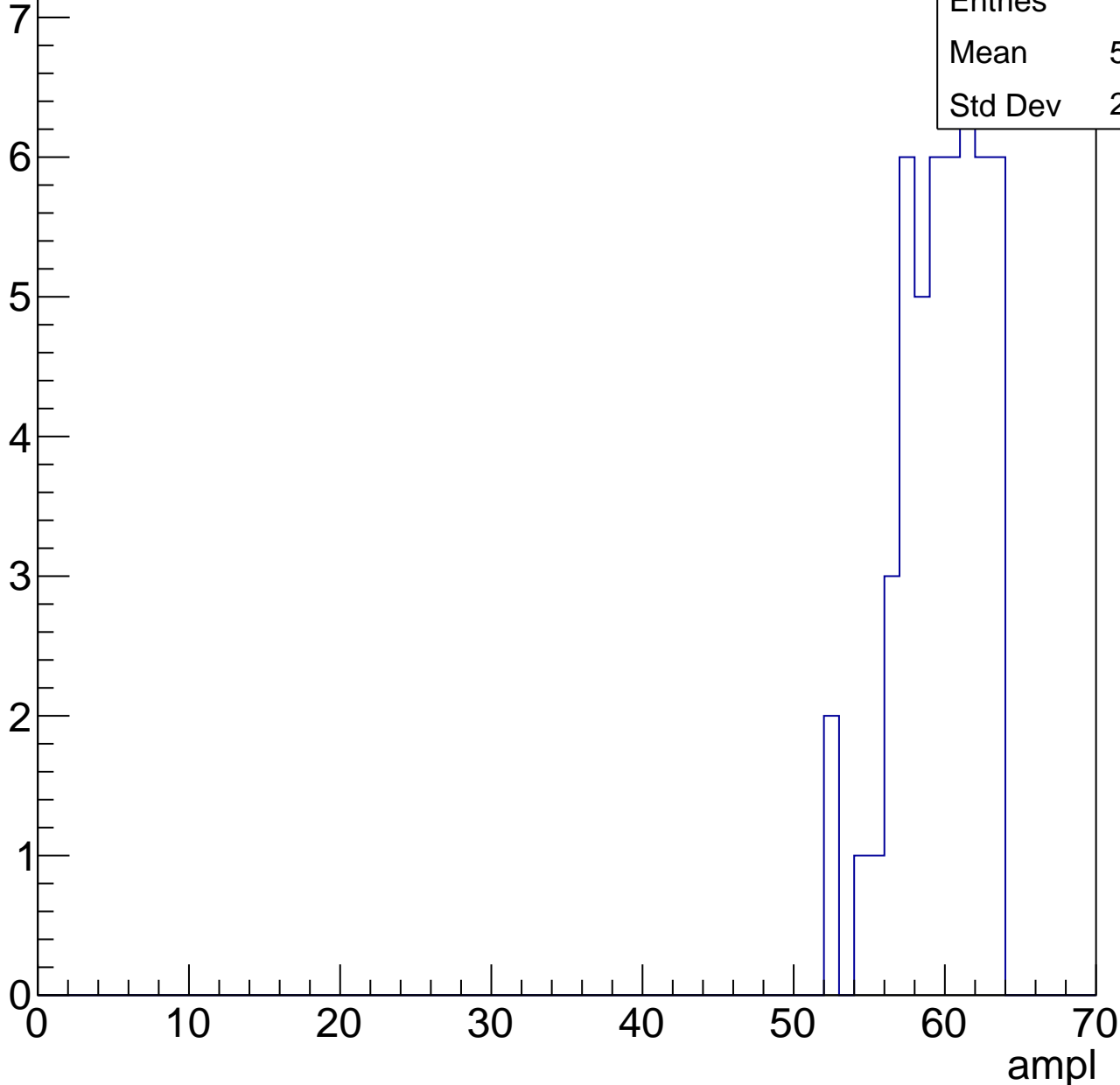


# B1L103S, U4-ch78, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

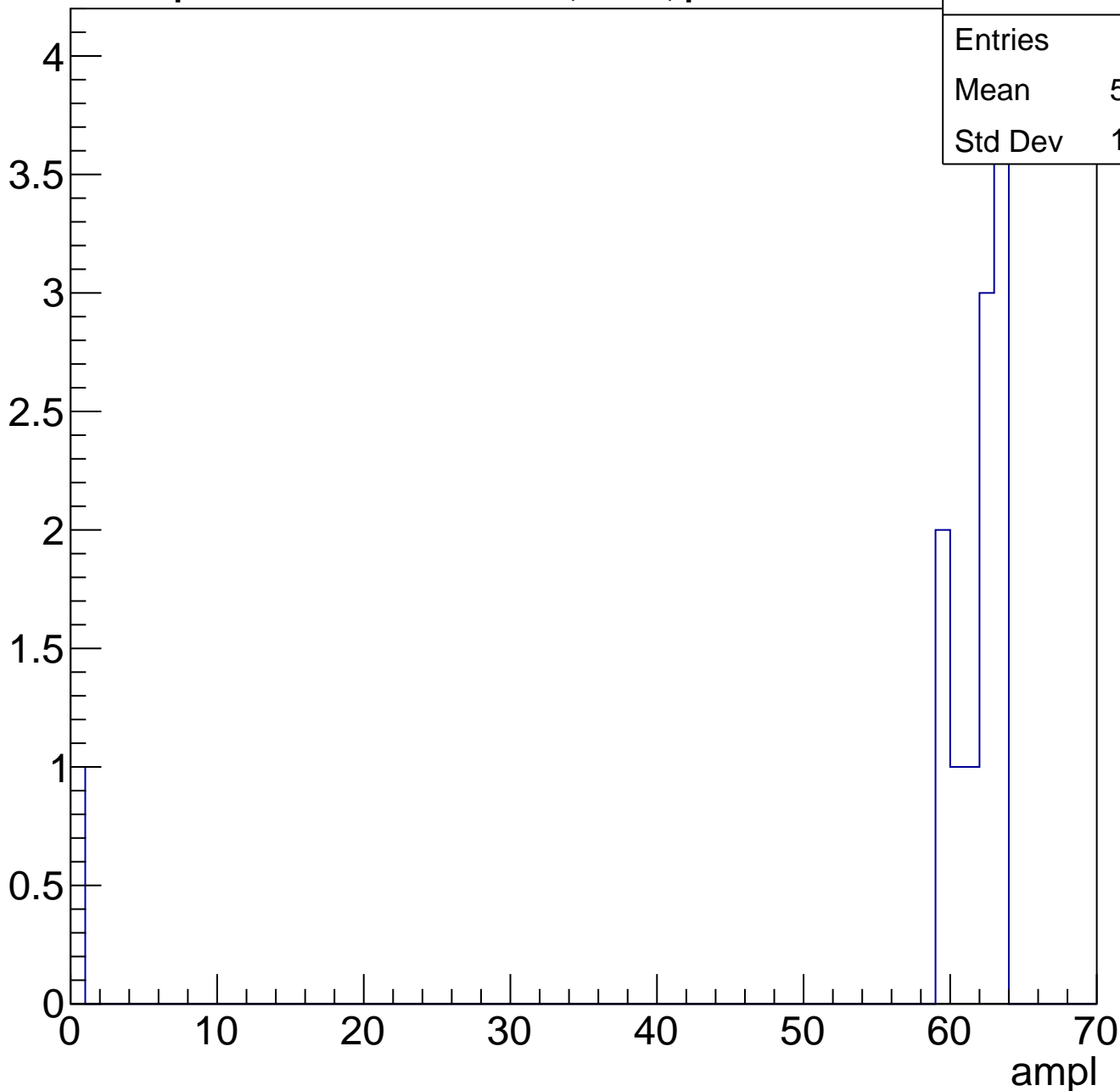
|         |       |
|---------|-------|
| Entries | 49    |
| Mean    | 59.27 |
| Std Dev | 2.768 |



# B1L103S, U4-ch78, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



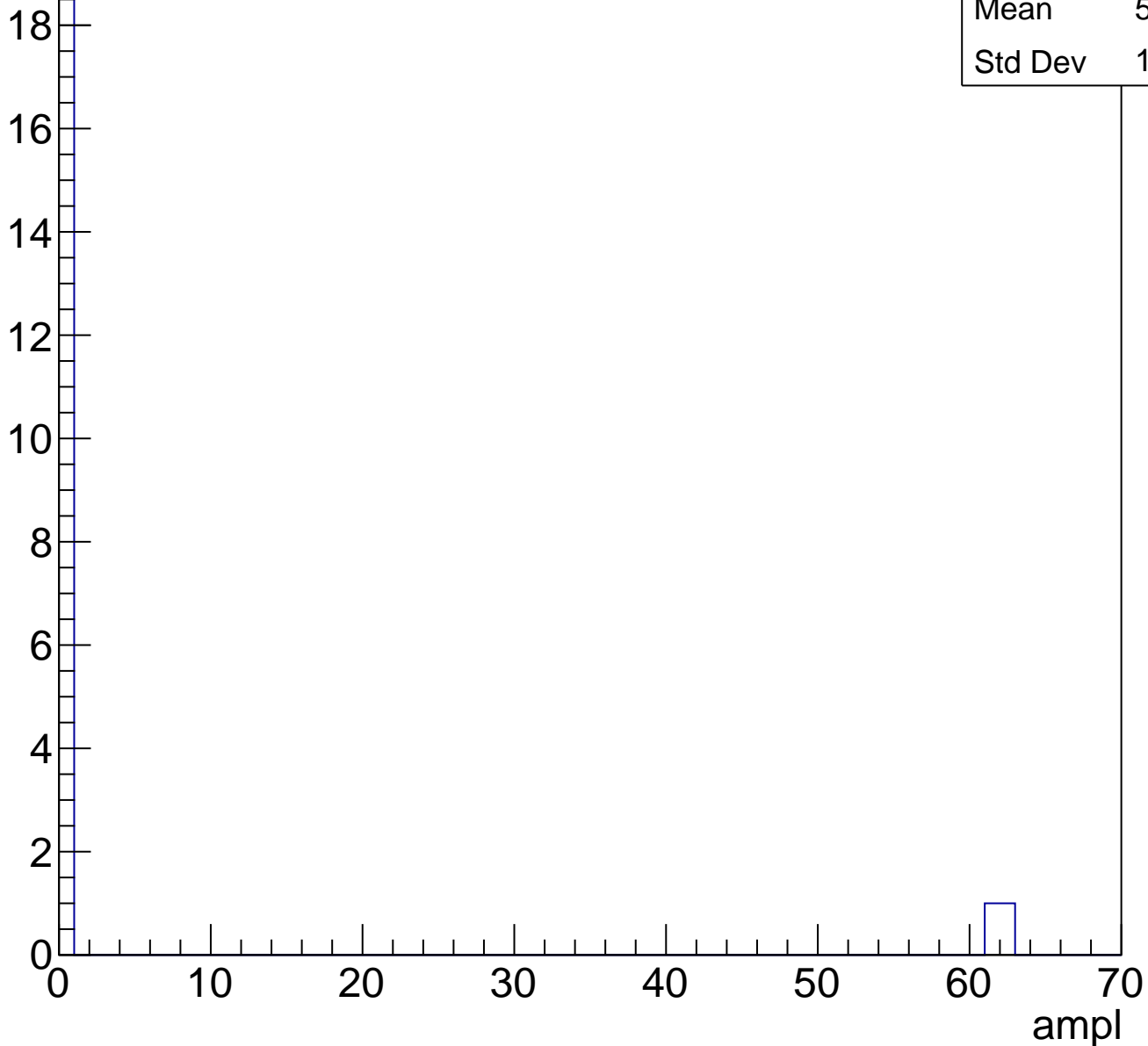


# B1L103S, U4-ch78, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 21    |
| Mean    | 5.857 |
| Std Dev | 18.05 |

Entry



# B1L103S, U4-ch79, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

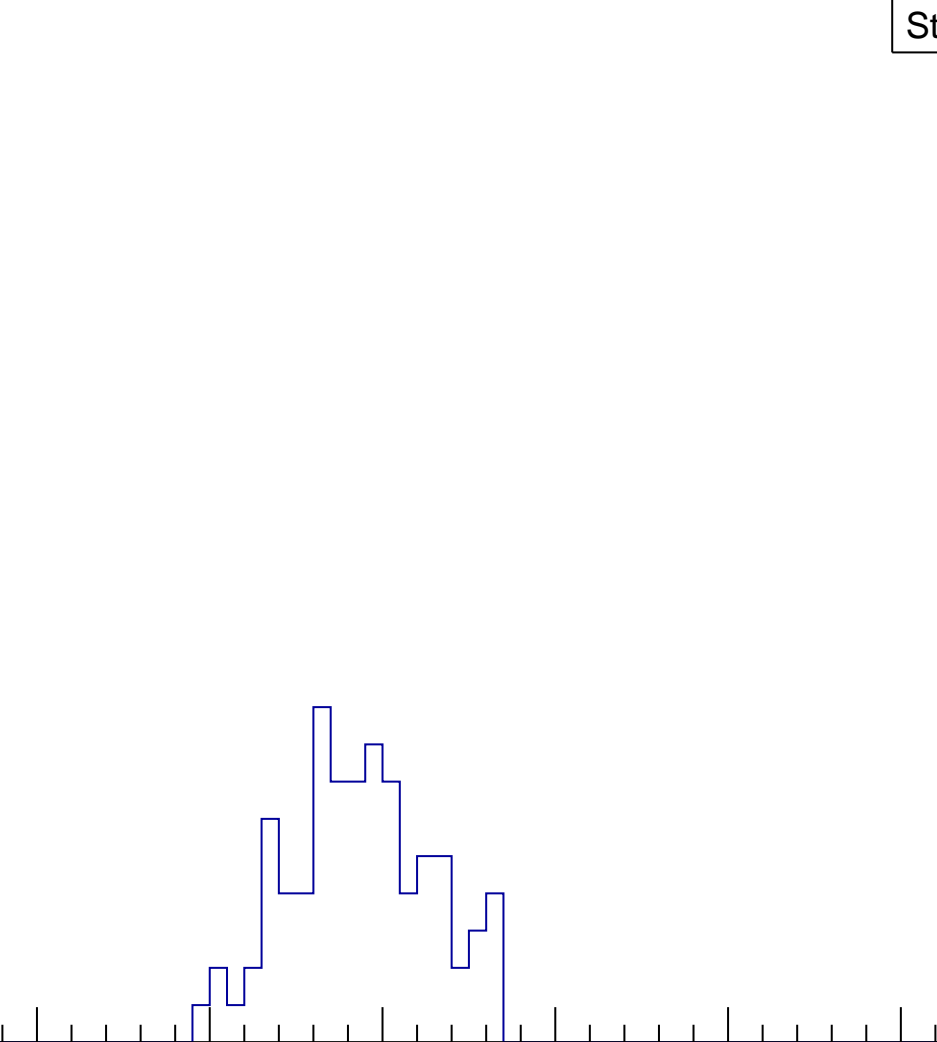
|         |       |
|---------|-------|
| Entries | 111   |
| Mean    | 20.59 |
| Std Dev | 13.01 |

Entry

30  
25  
20  
15  
10  
5  
0

0 10 20 30 40 50 60 70

ampl

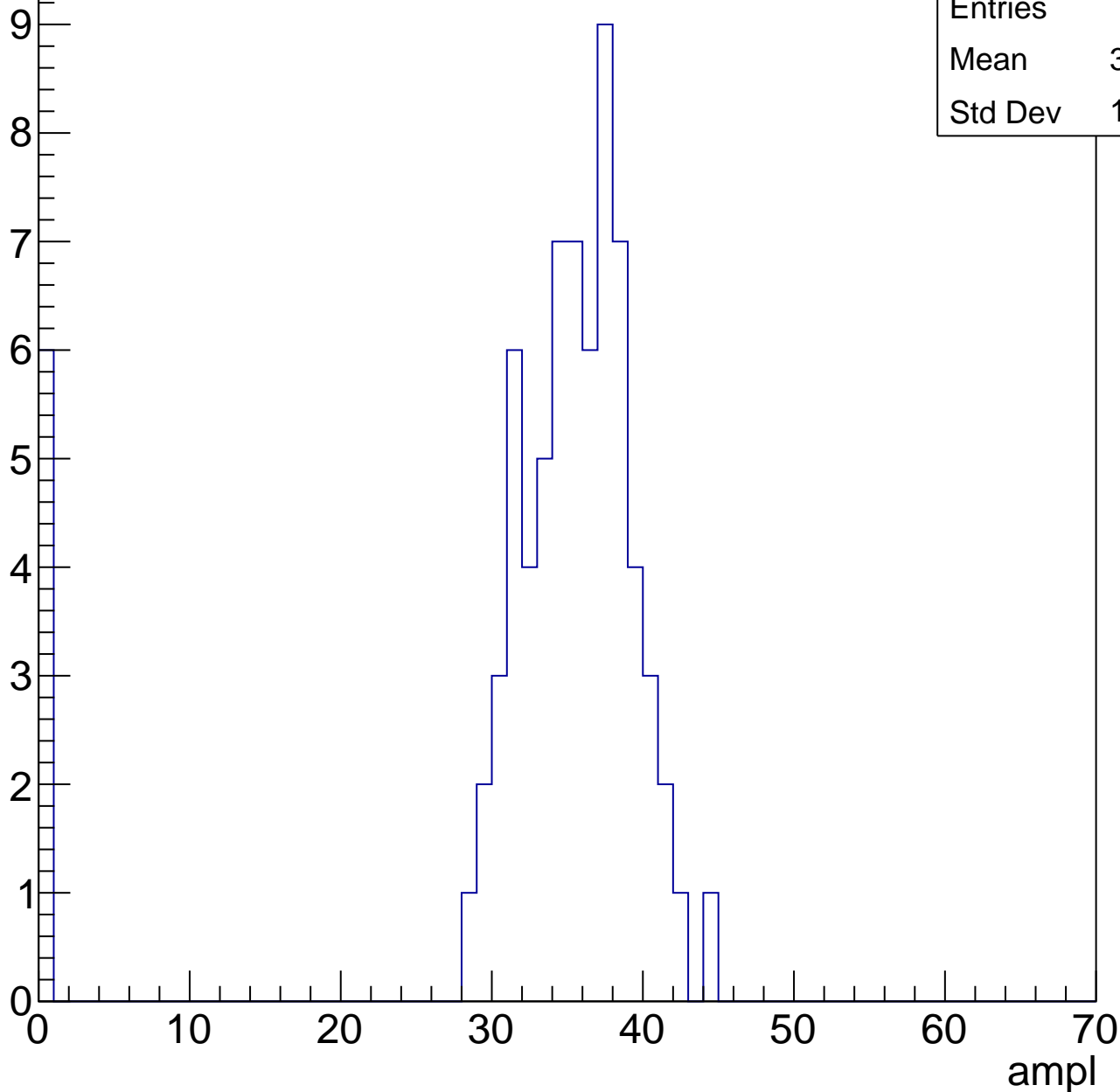


# B1L103S, U4-ch79, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 74    |
| Mean    | 32.39 |
| Std Dev | 10.17 |

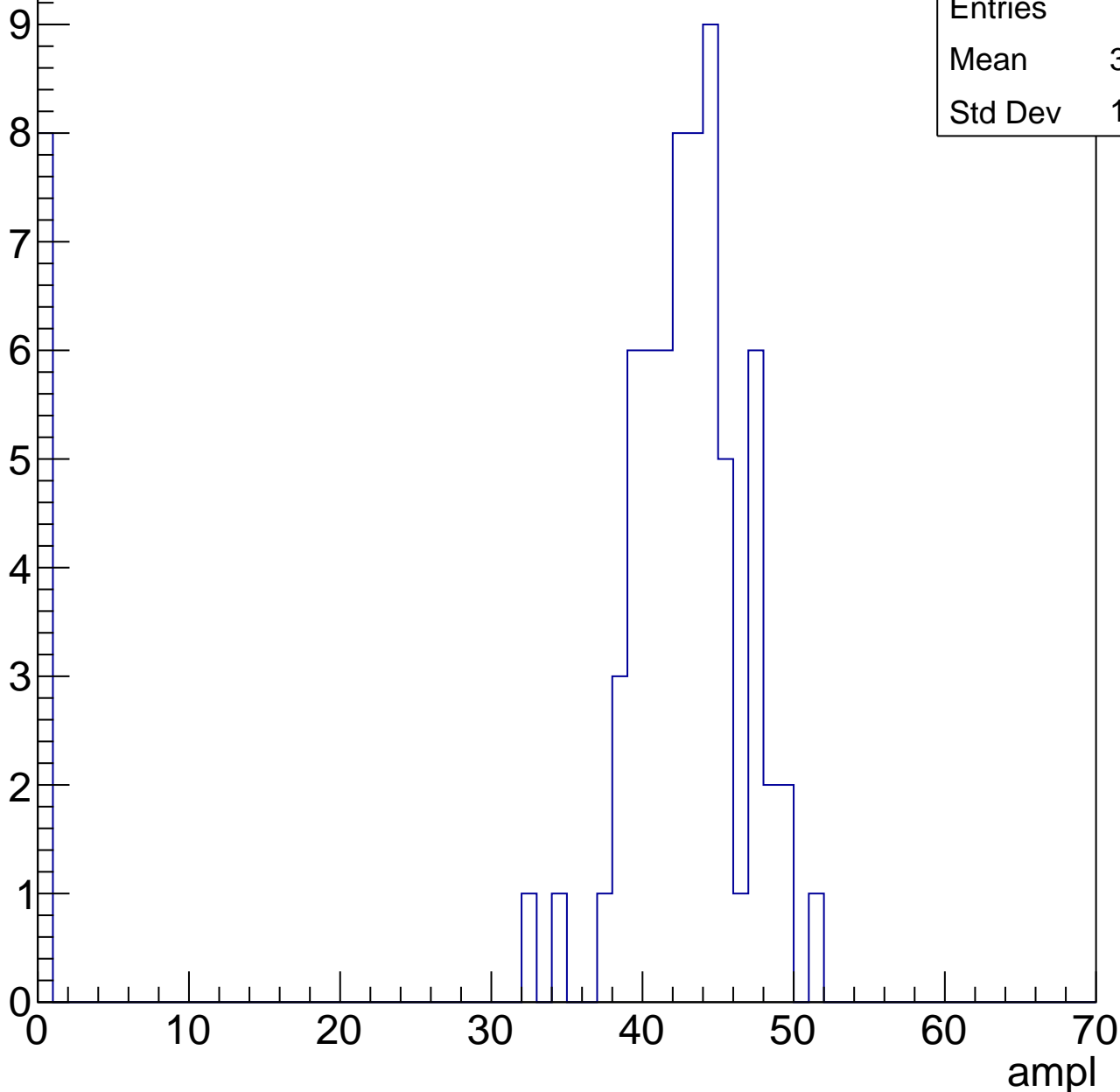


# B1L103S, U4-ch79, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 74    |
| Mean    | 37.99 |
| Std Dev | 13.63 |

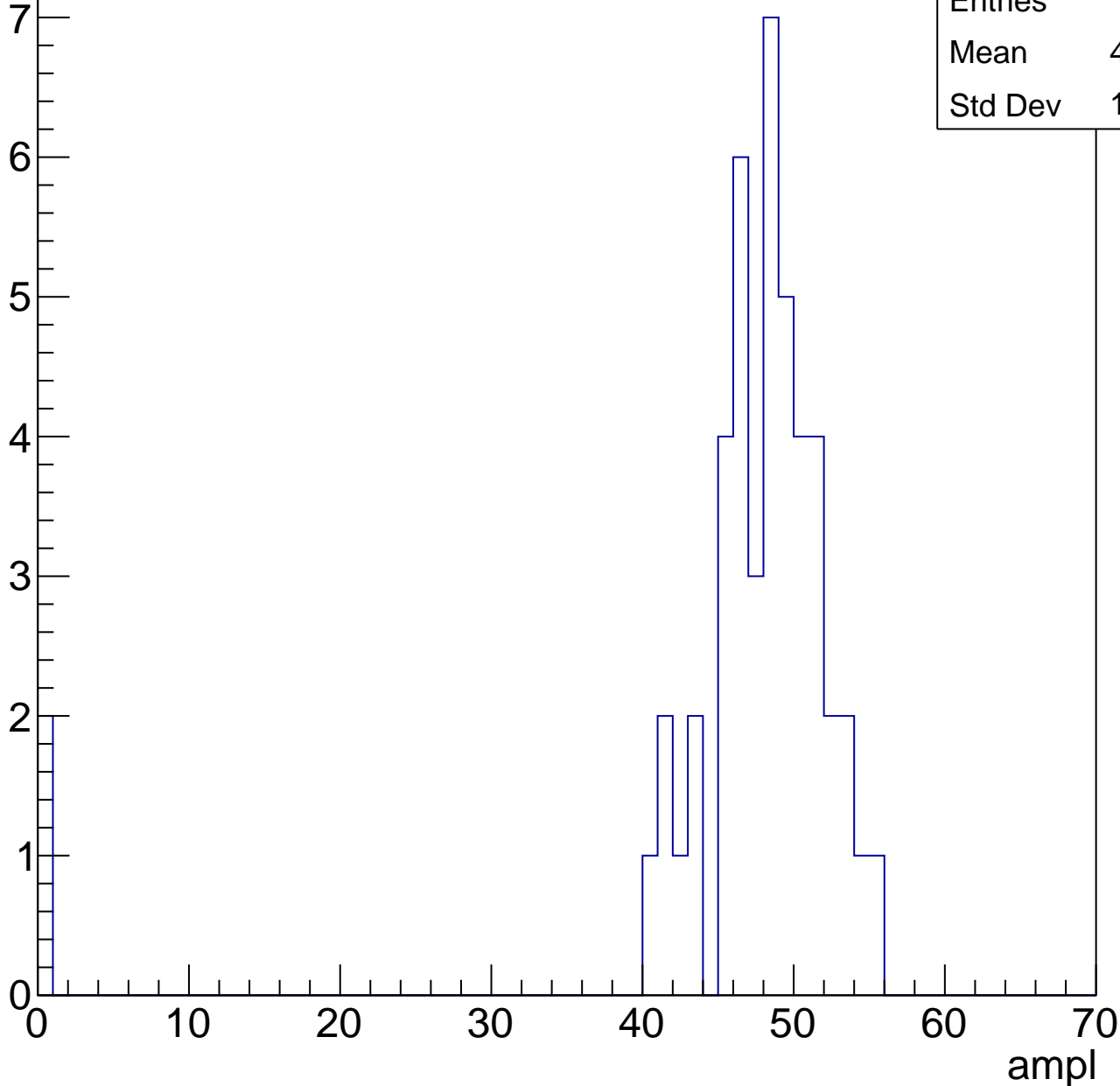


# B1L103S, U4-ch79, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 47    |
| Mean    | 45.77 |
| Std Dev | 10.22 |

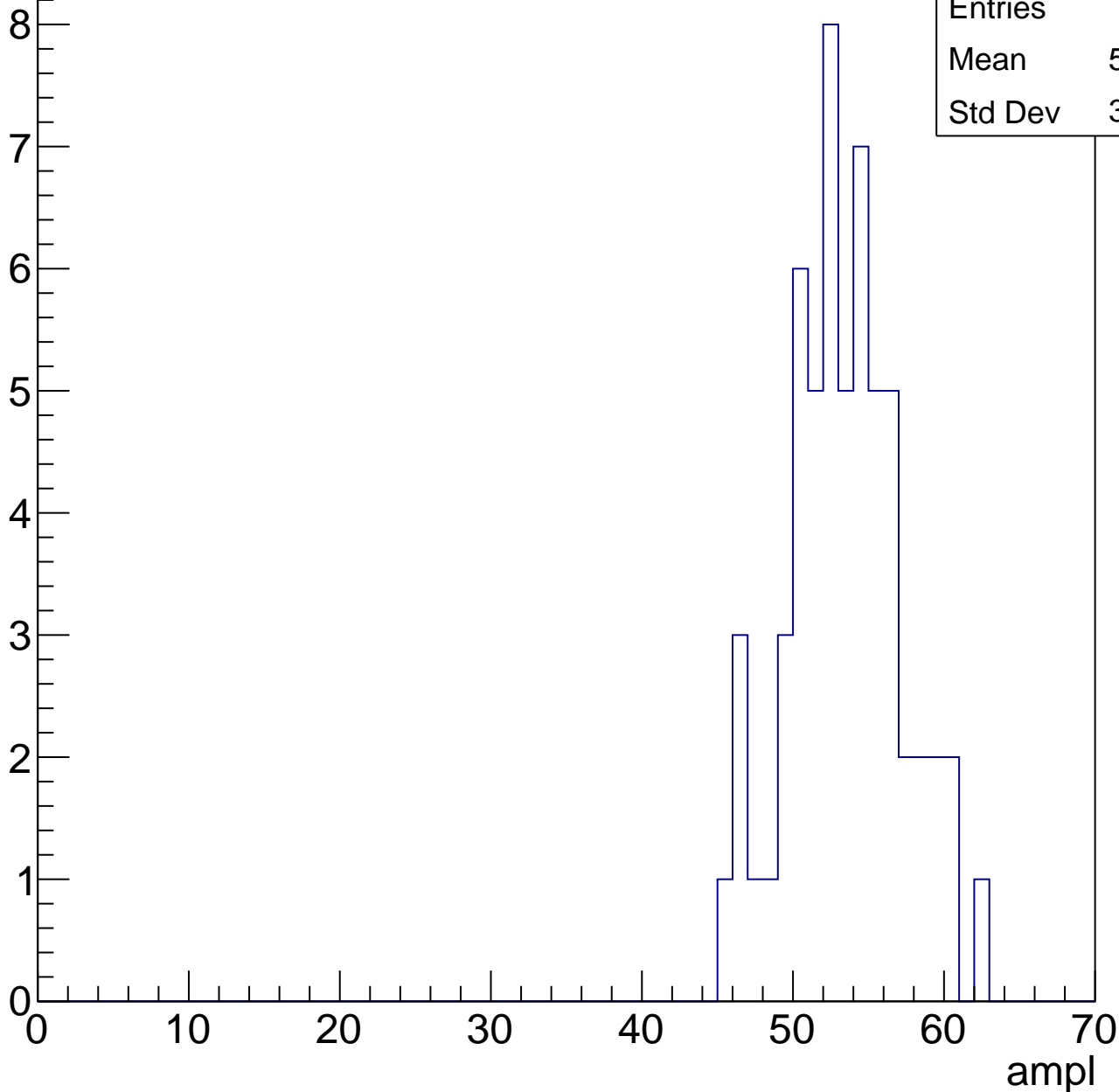


# B1L103S, U4-ch79, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

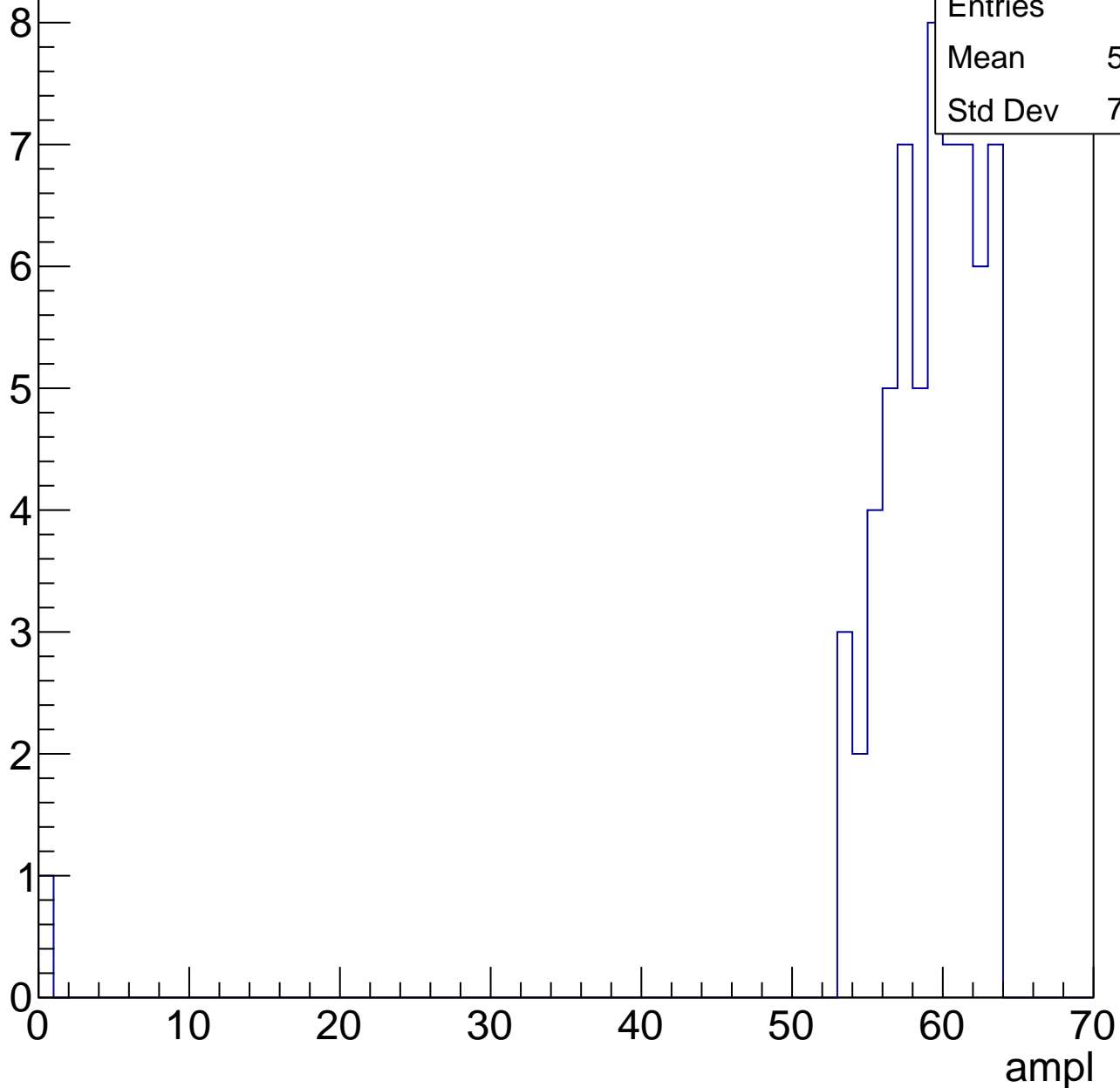
|         |       |
|---------|-------|
| Entries | 59    |
| Mean    | 52.95 |
| Std Dev | 3.698 |



# B1L103S, U4-ch79, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U4-ch79, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

|         |       |
|---------|-------|
| Entries | 14    |
| Mean    | 60.64 |
| Std Dev | 2.022 |



# B1L103S, U4-ch79, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

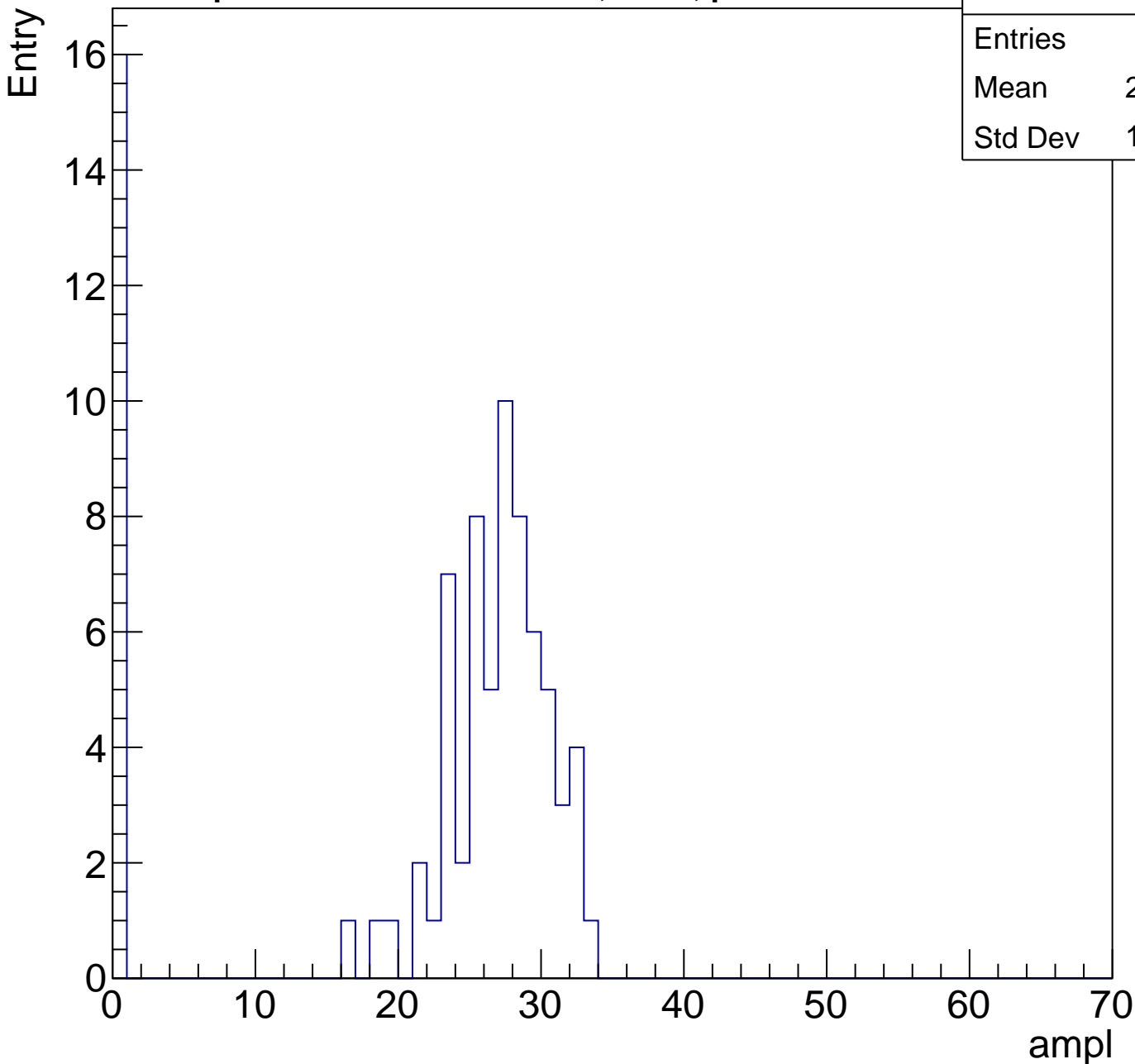
Entry



# B1L103S, U4-ch80, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

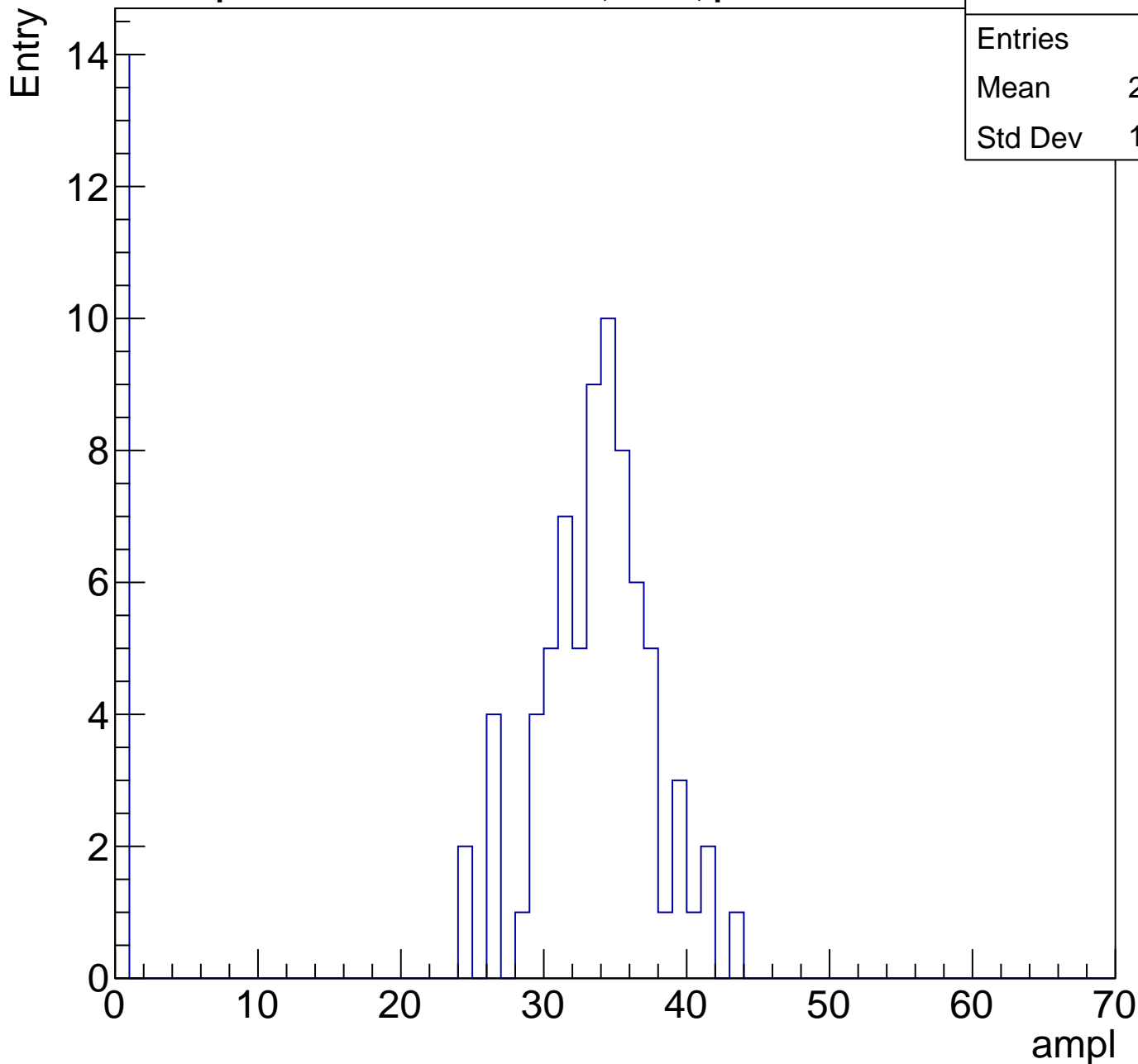
|         |       |
|---------|-------|
| Entries | 81    |
| Mean    | 21.33 |
| Std Dev | 11.03 |



# B1L103S, U4-ch80, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 88    |
| Mean    | 27.97 |
| Std Dev | 12.67 |

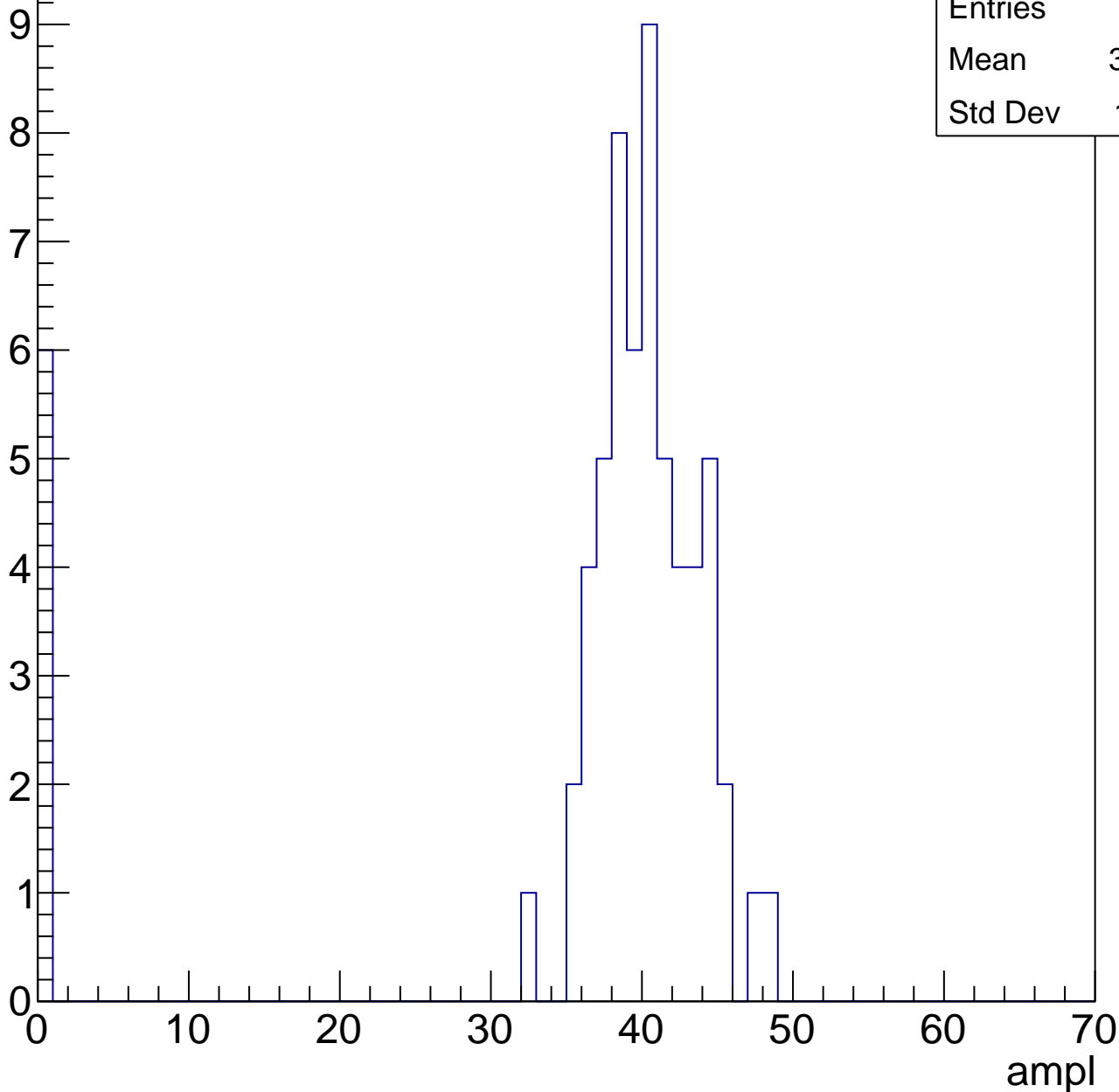


# B1L103S, U4-ch80, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

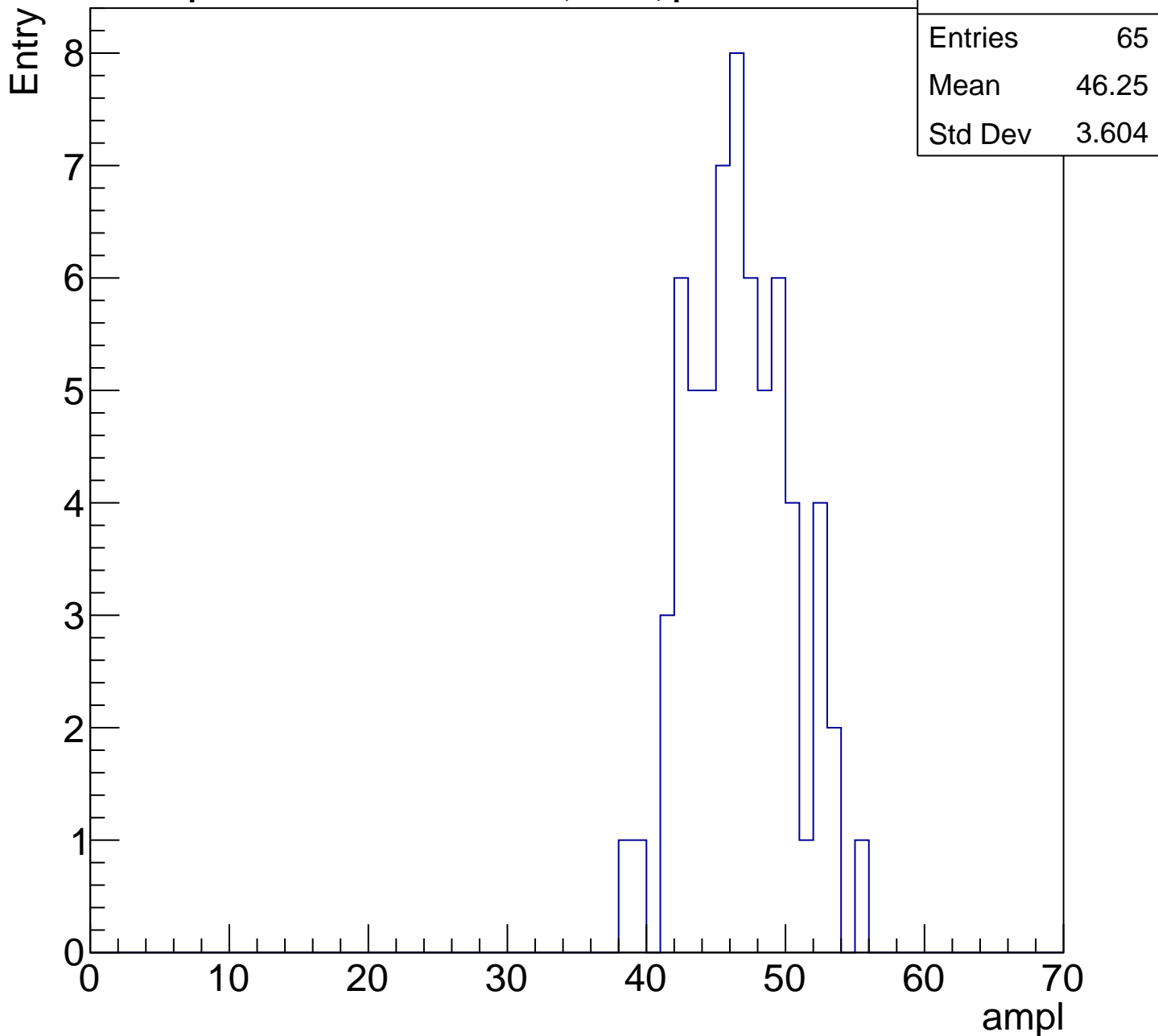
Entry

|         |       |
|---------|-------|
| Entries | 63    |
| Mean    | 36.17 |
| Std Dev | 12.11 |



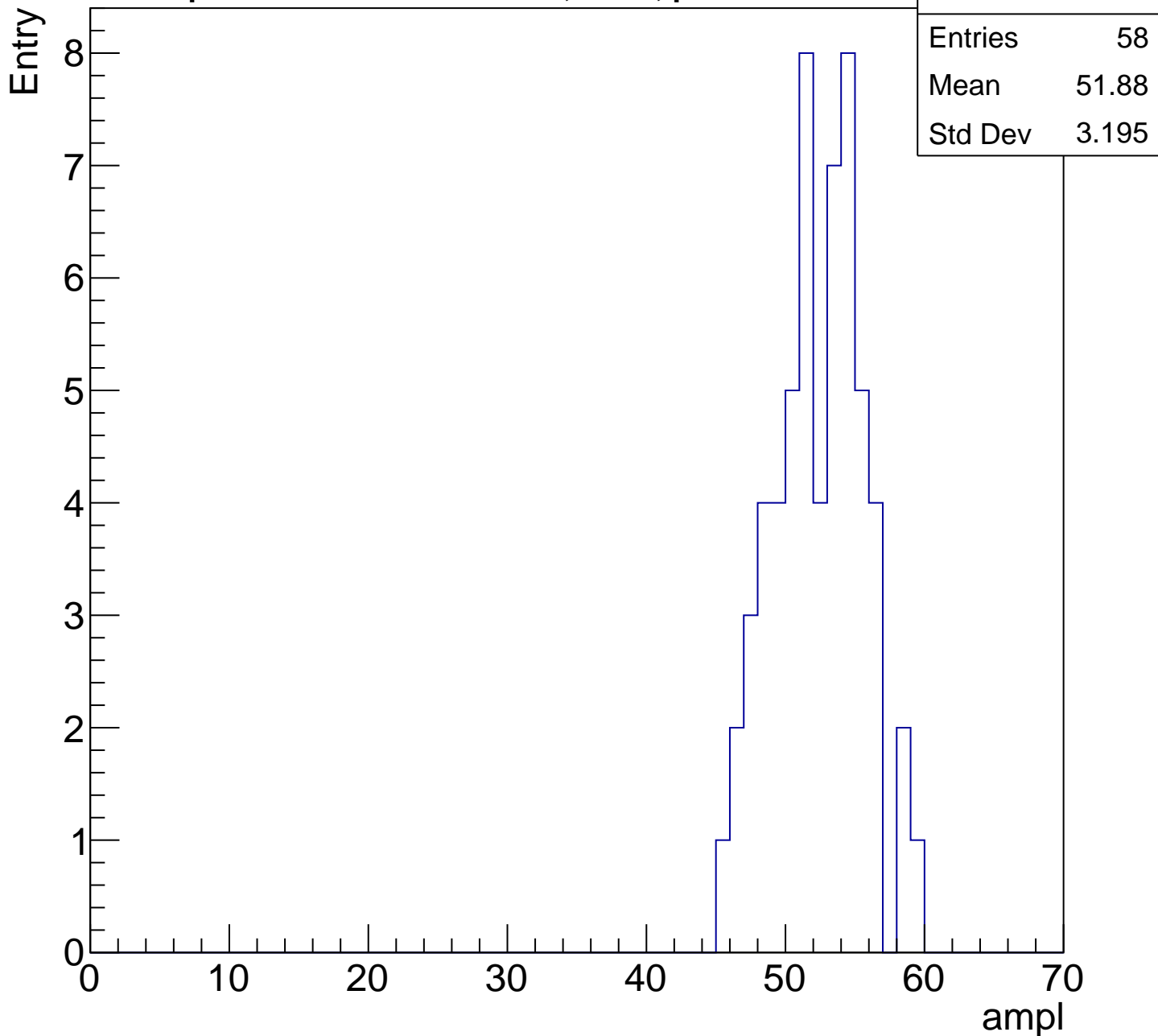
# B1L103S, U4-ch80, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2



# B1L103S, U4-ch80, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

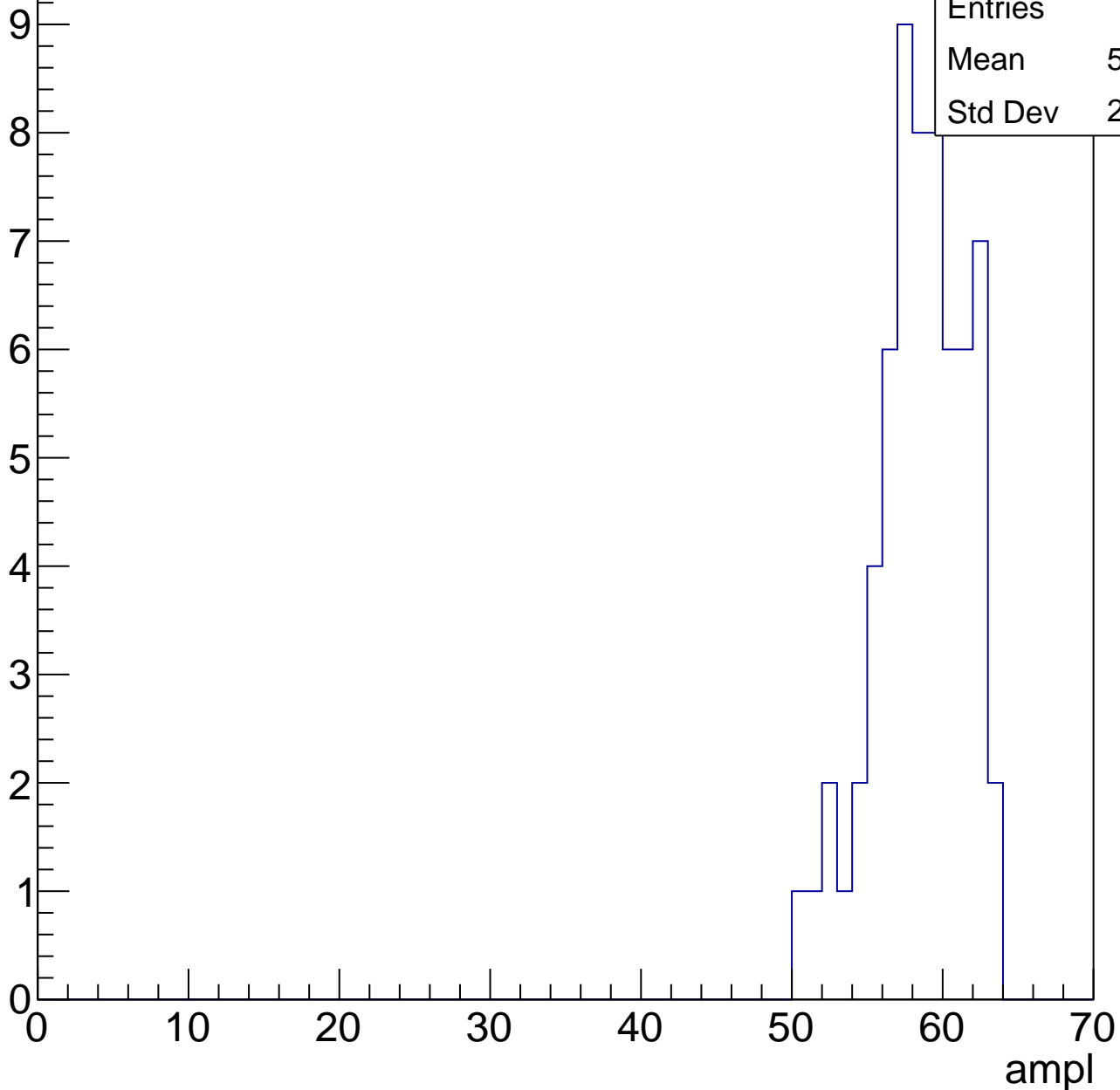


# B1L103S, U4-ch80, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 63    |
| Mean    | 58.05 |
| Std Dev | 2.978 |

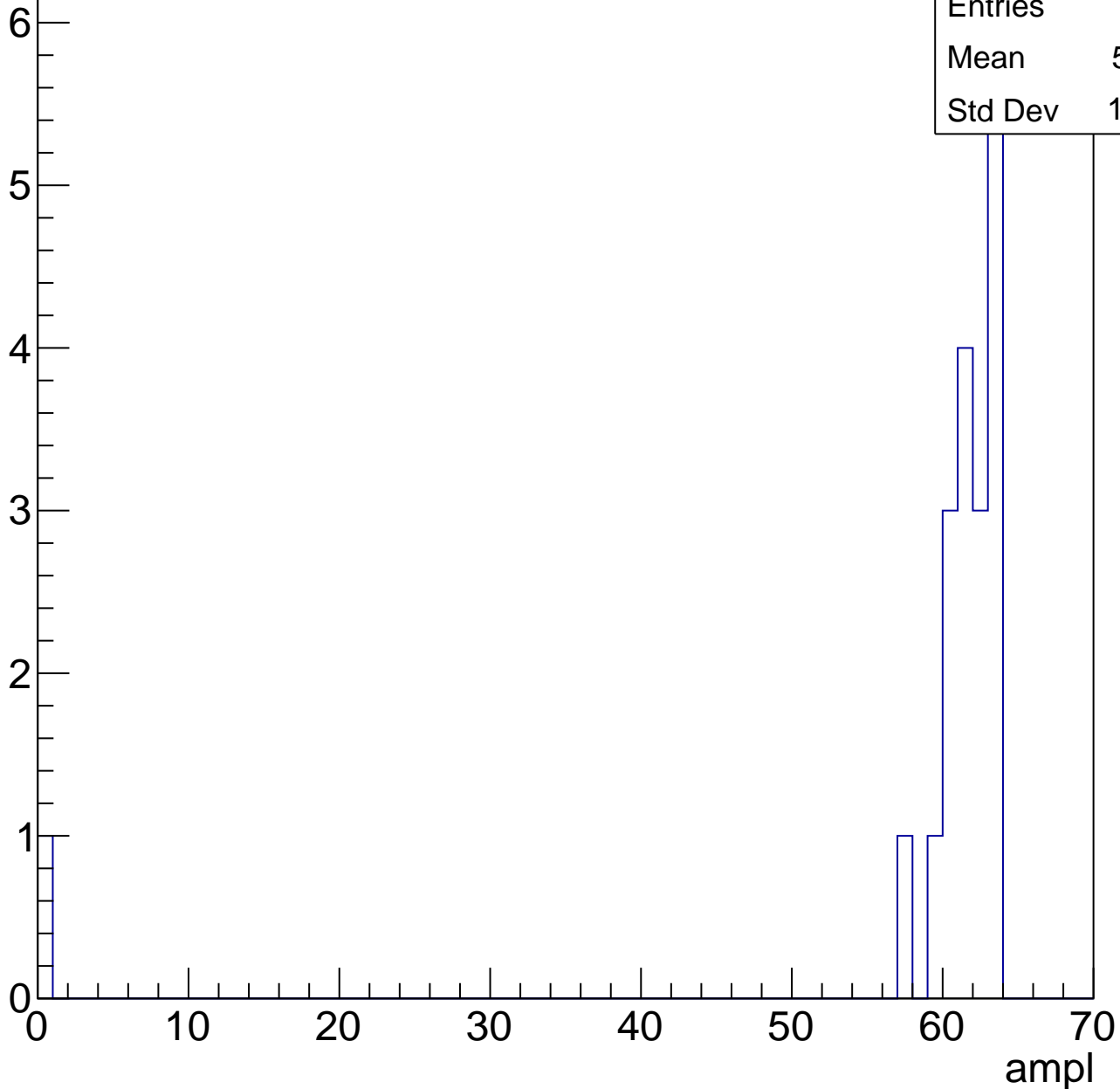


# B1L103S, U4-ch80, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 19    |
| Mean    | 58.11 |
| Std Dev | 13.79 |



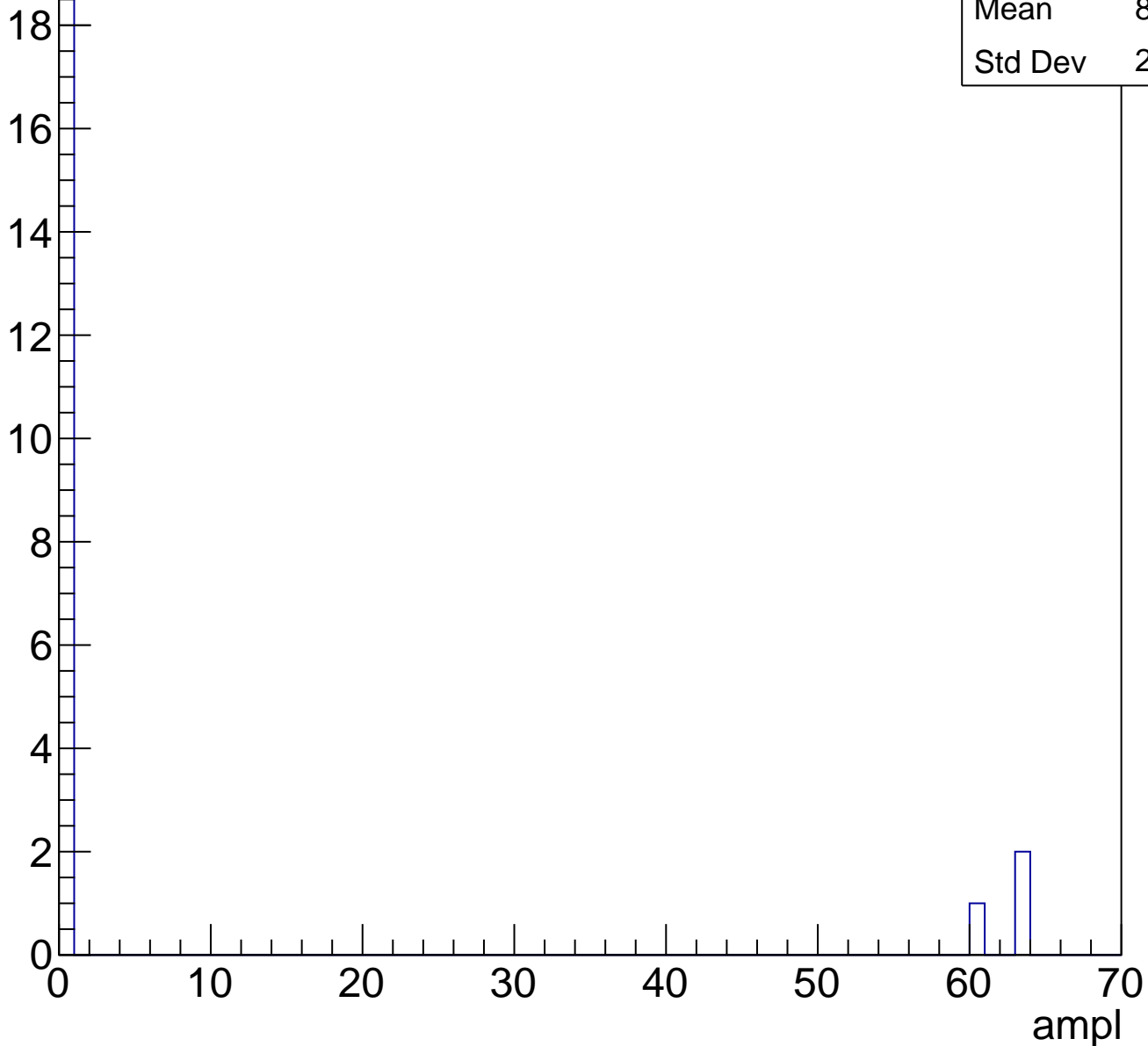


# B1L103S, U4-ch80, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 22    |
| Mean    | 8.455 |
| Std Dev | 21.28 |

Entry

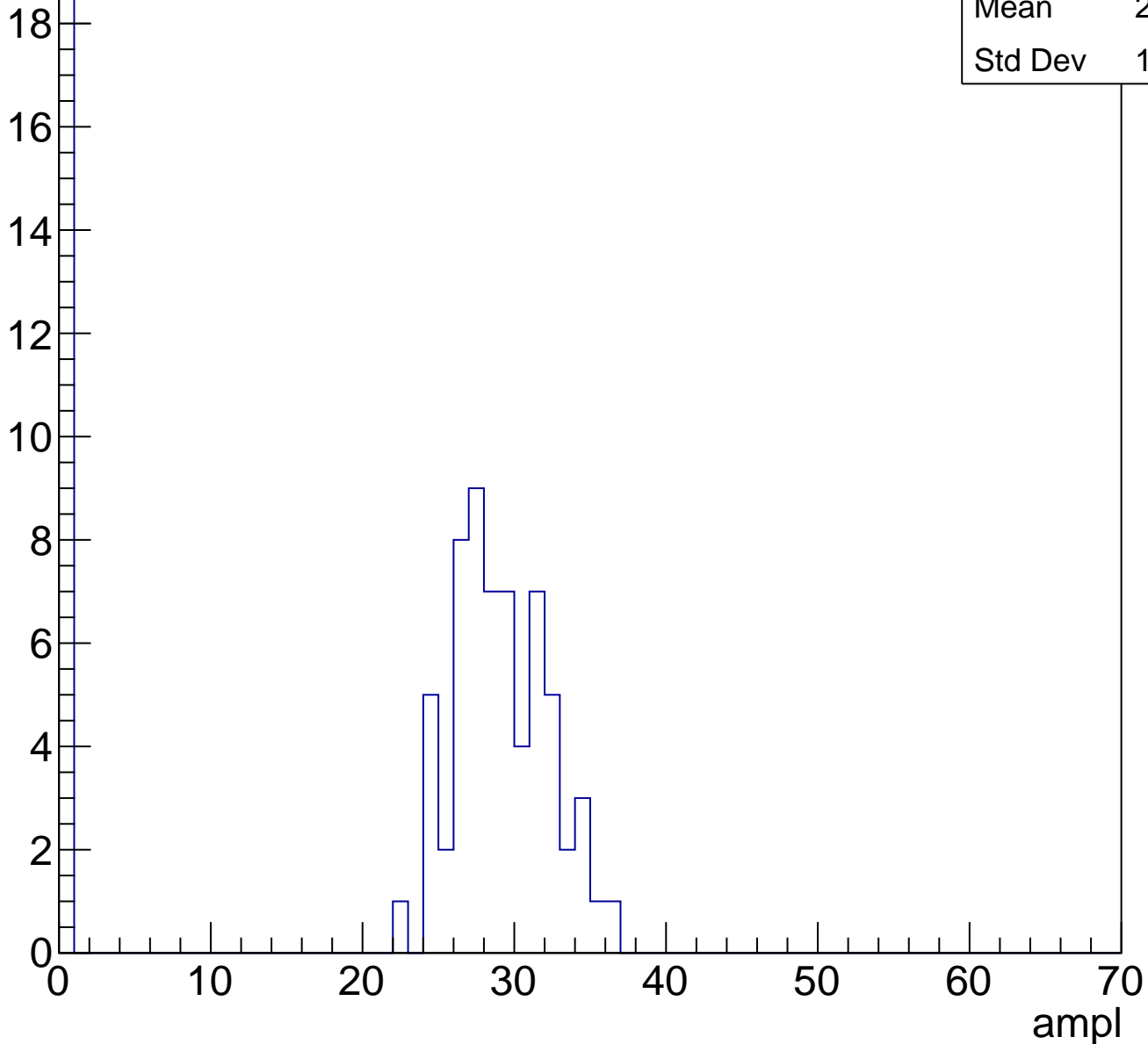


# B1L103S, U4-ch81, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 81    |
| Mean    | 21.95 |
| Std Dev | 12.44 |

Entry

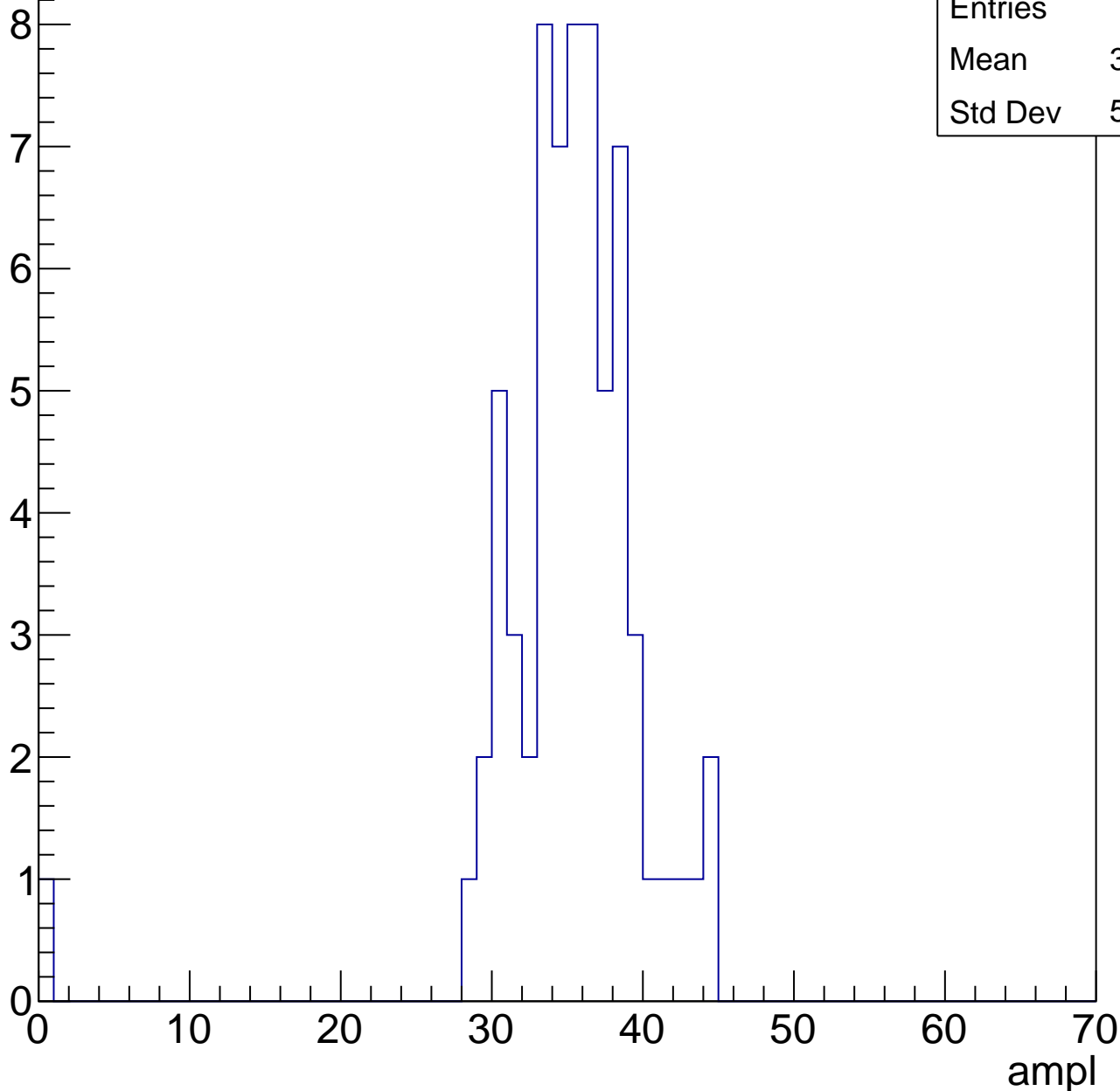


# B1L103S, U4-ch81, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 66    |
| Mean    | 34.62 |
| Std Dev | 5.562 |

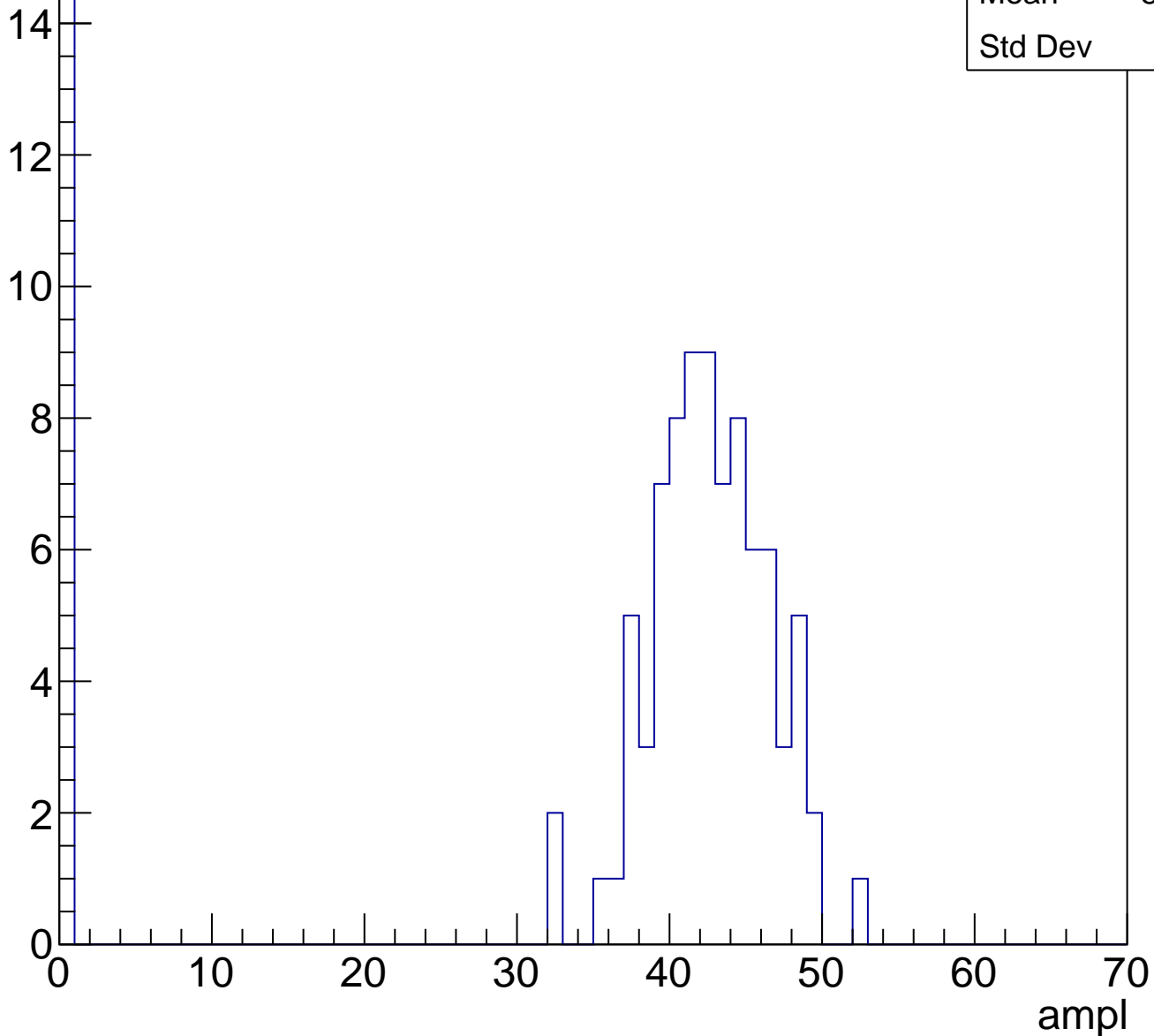


# B1L103S, U4-ch81, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 98    |
| Mean    | 35.76 |
| Std Dev | 15.6  |

Entry

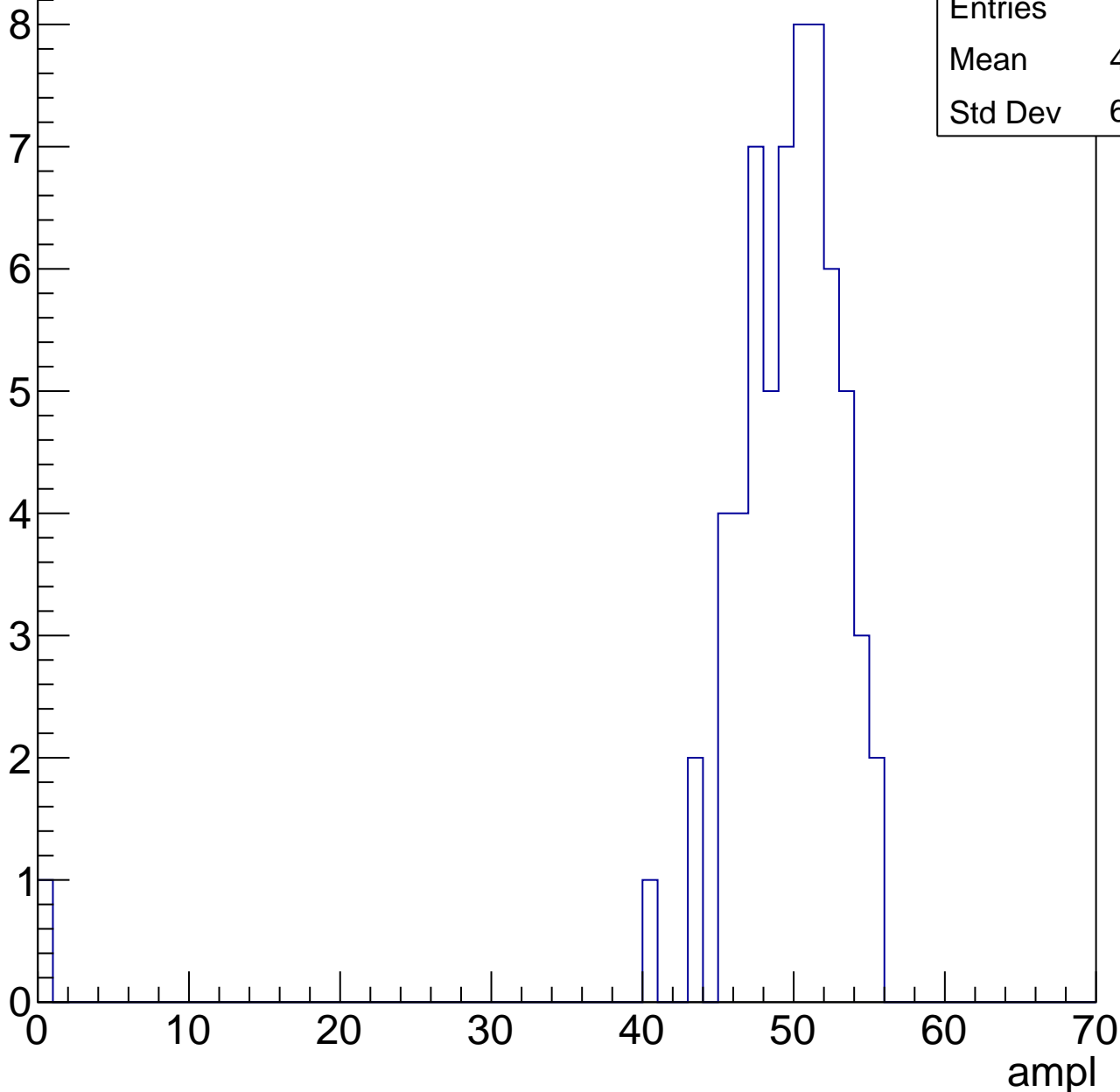


# B1L103S, U4-ch81, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 63    |
| Mean    | 48.56 |
| Std Dev | 6.896 |

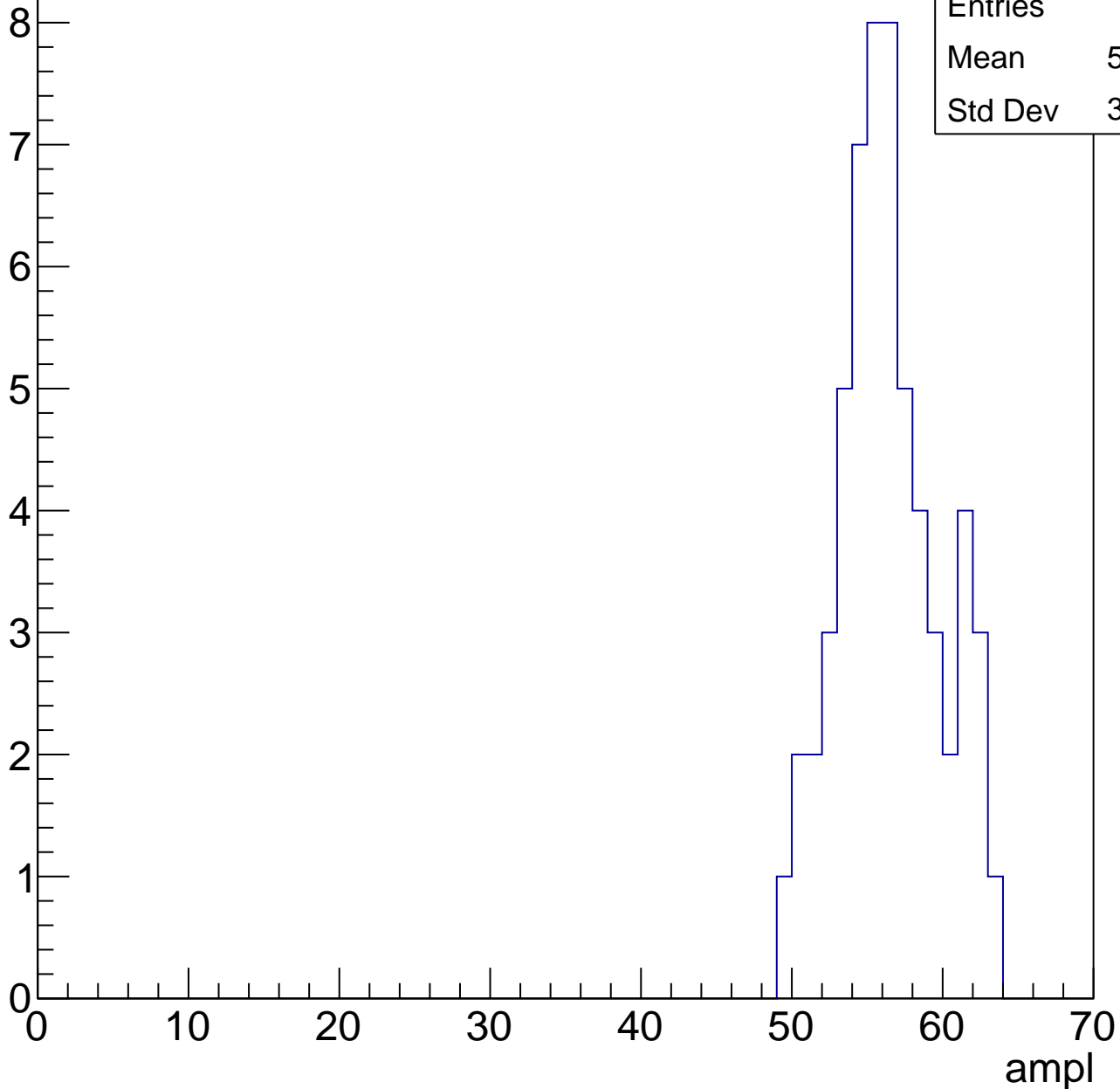


# B1L103S, U4-ch81, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 58    |
| Mean    | 55.95 |
| Std Dev | 3.314 |

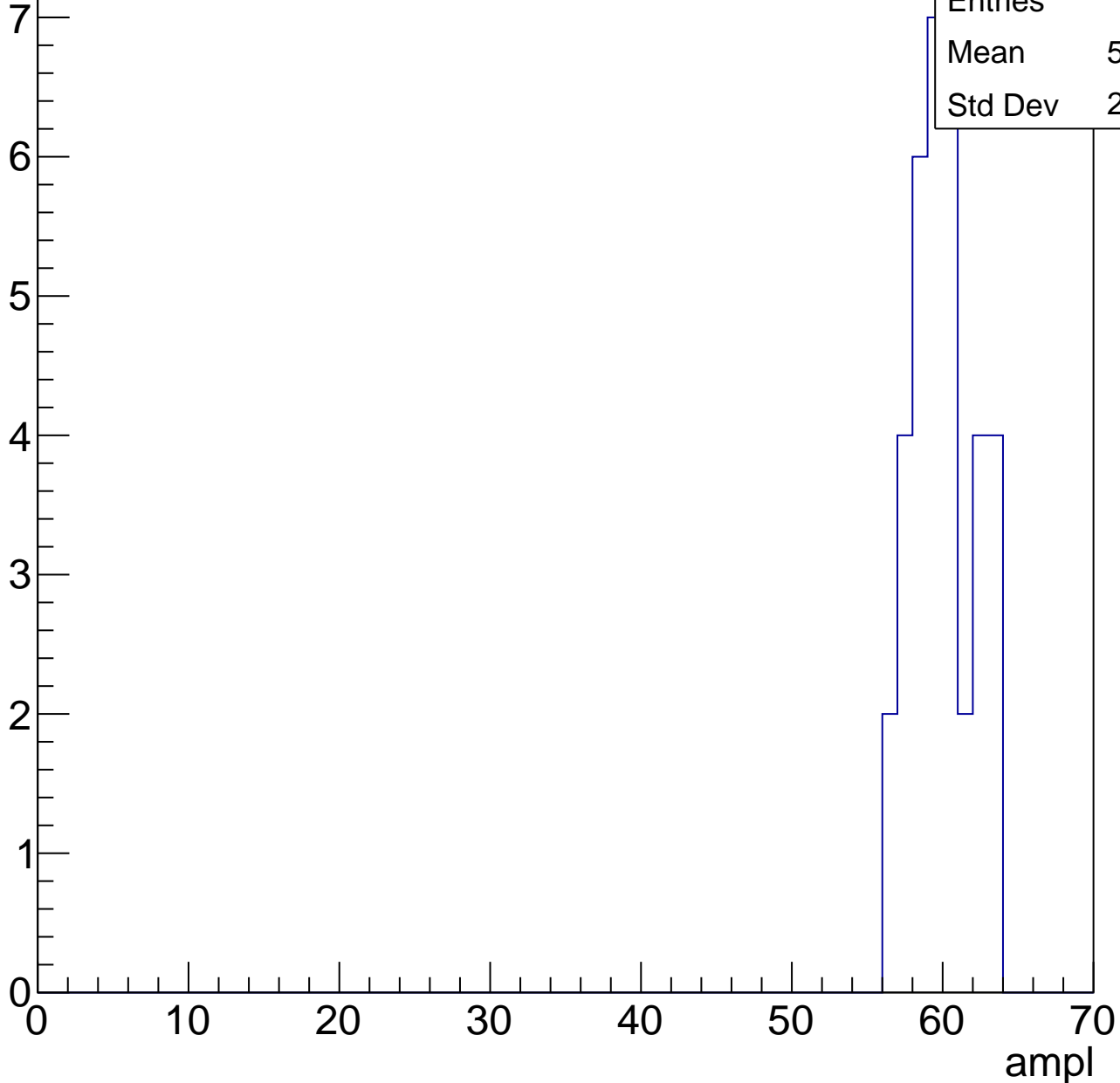


# B1L103S, U4-ch81, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

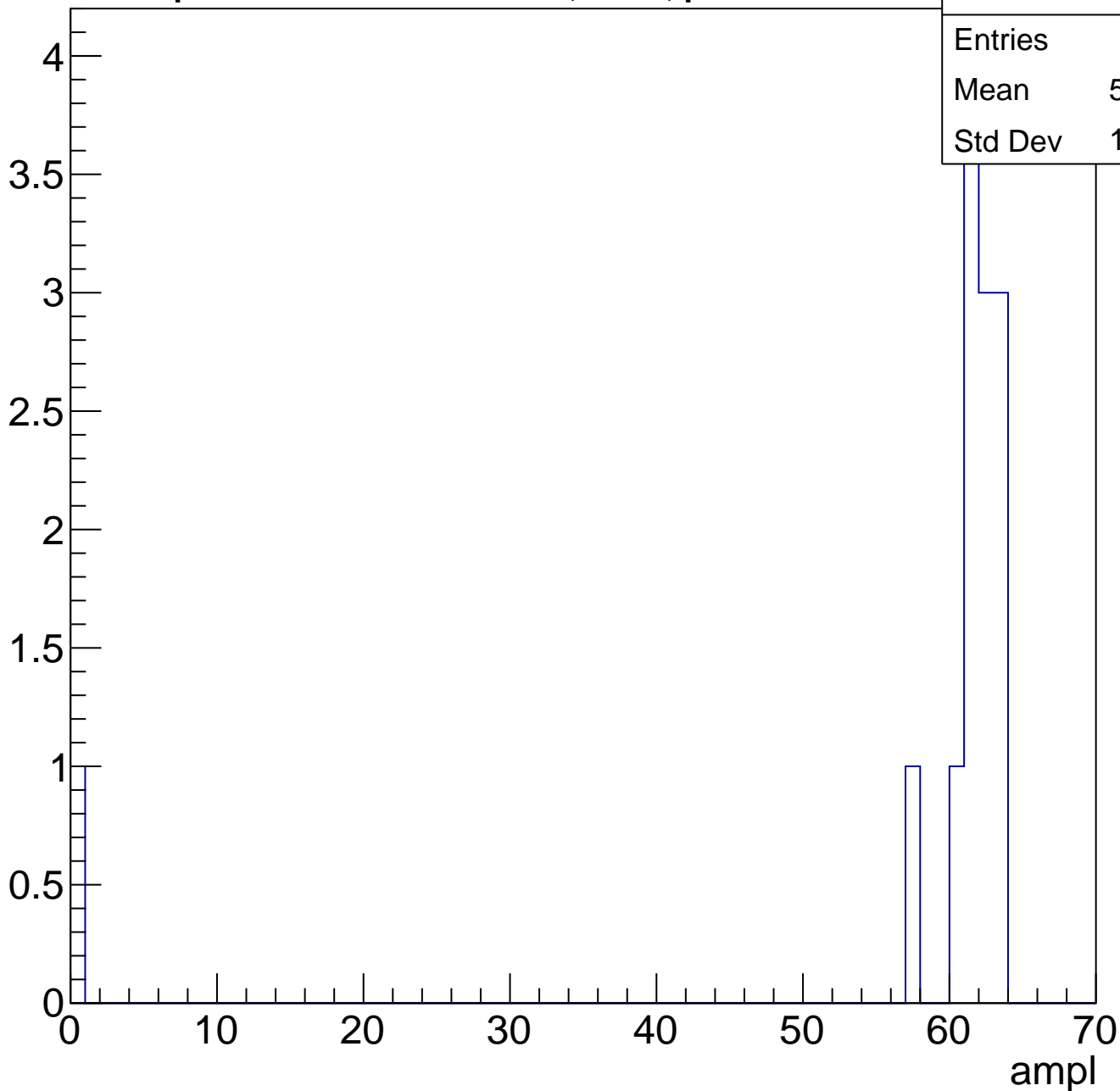
|         |       |
|---------|-------|
| Entries | 36    |
| Mean    | 59.53 |
| Std Dev | 2.007 |



# B1L103S, U4-ch81, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U4-ch81, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U4-ch82, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

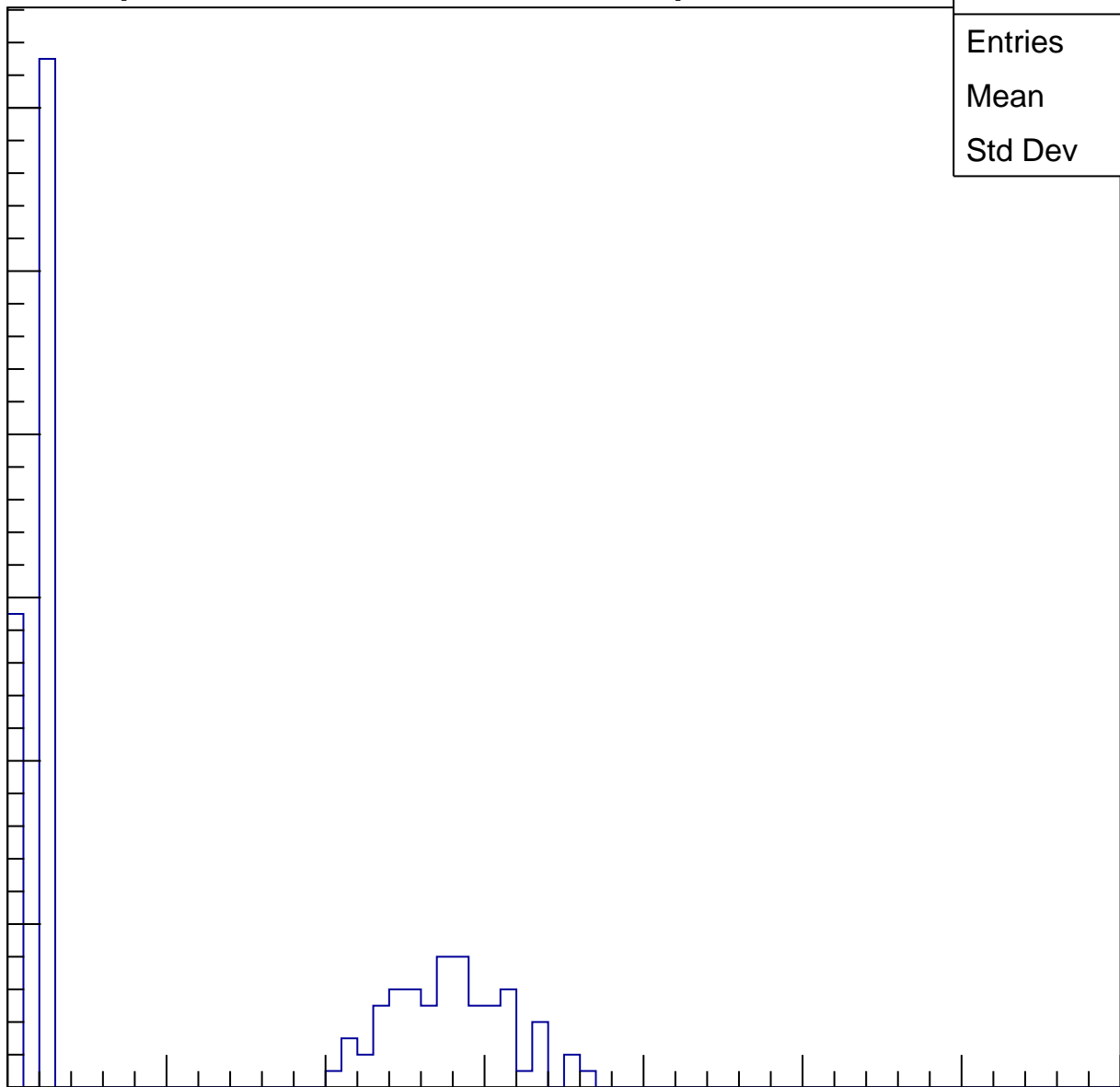
|         |       |
|---------|-------|
| Entries | 160   |
| Mean    | 12.39 |
| Std Dev | 13.06 |

Entry

60  
50  
40  
30  
20  
10  
0

0 10 20 30 40 50 60 70

ampl



# B1L103S, U4-ch82, adc1

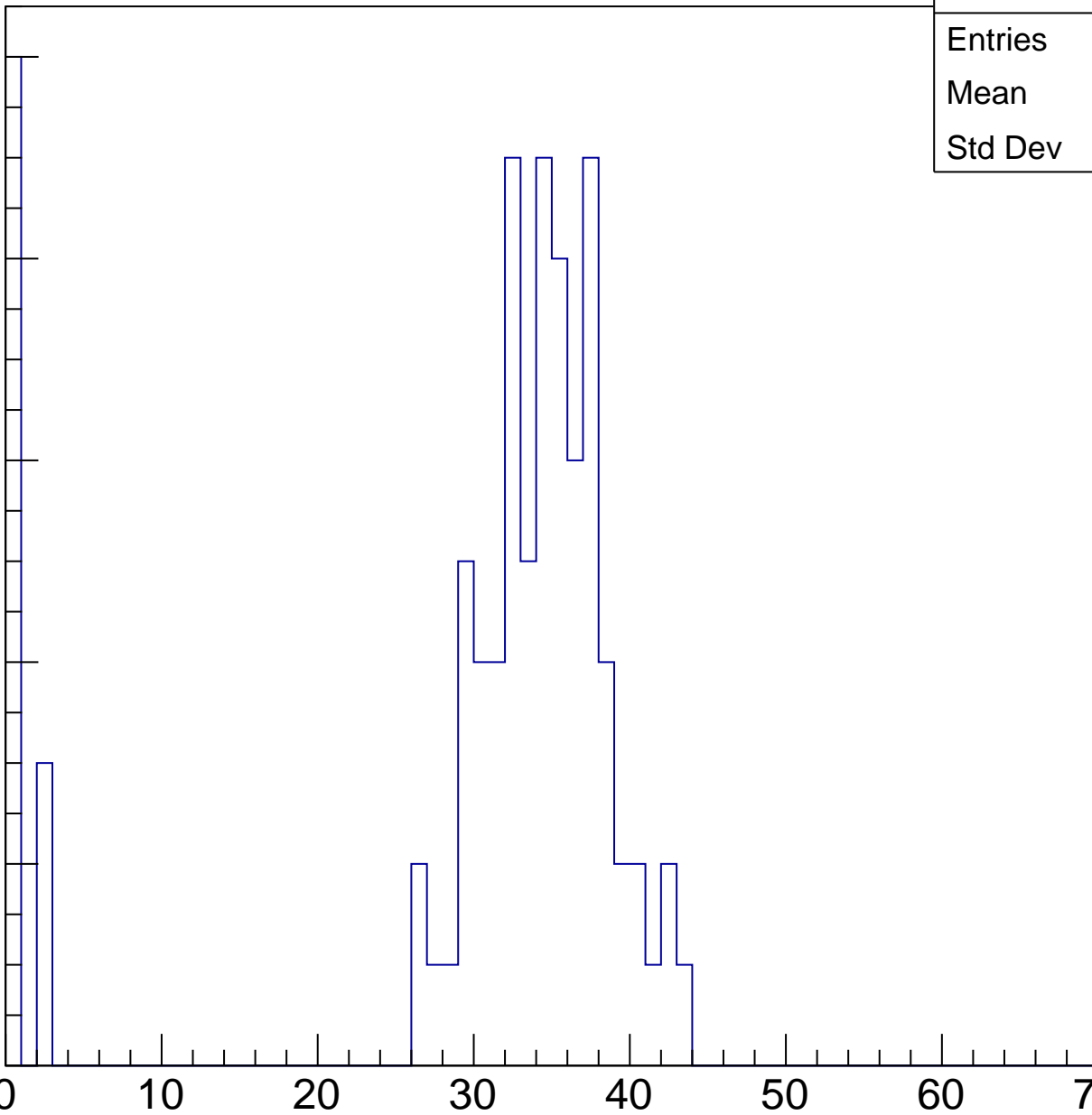
calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 88    |
| Mean    | 29.18 |
| Std Dev | 12.44 |

Entry

10  
8  
6  
4  
2  
0

ampl

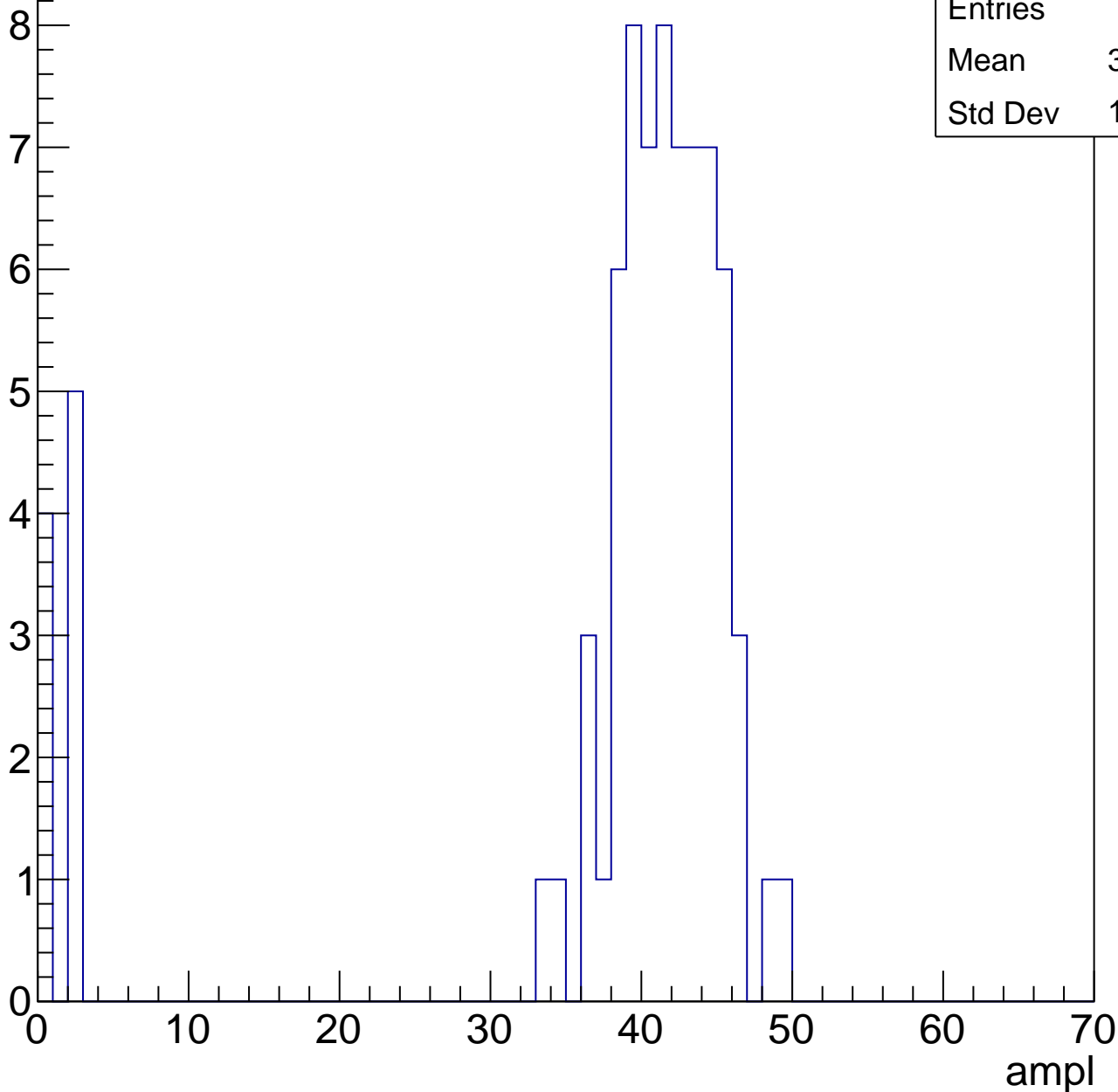


# B1L103S, U4-ch82, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 76    |
| Mean    | 36.55 |
| Std Dev | 13.33 |



# B1L103S, U4-ch82, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 65    |
| Mean    | 45.94 |
| Std Dev | 10.19 |

Entry

10

8

6

4

2

0

ampl

0

10

20

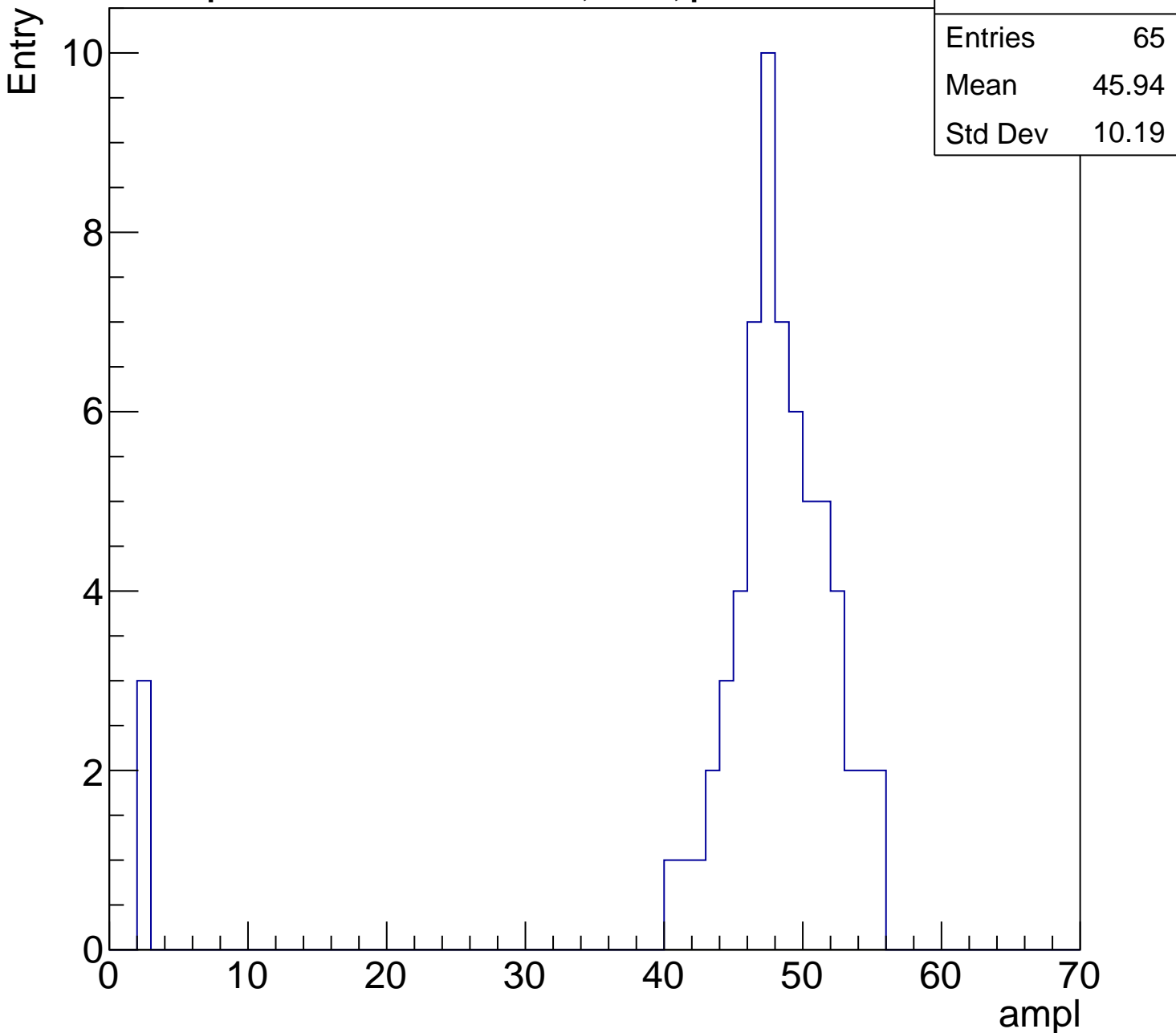
30

40

50

60

70

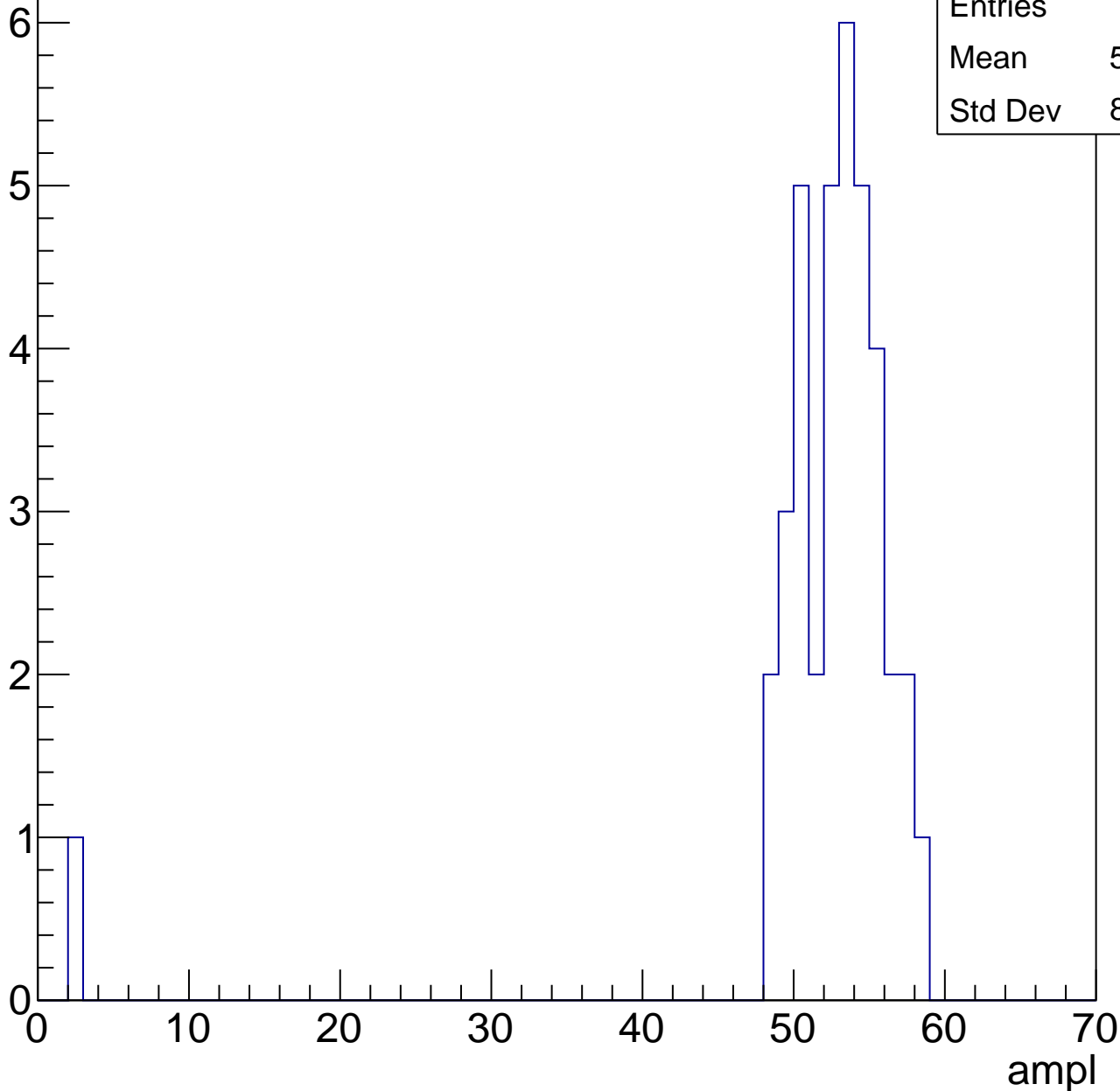


# B1L103S, U4-ch82, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

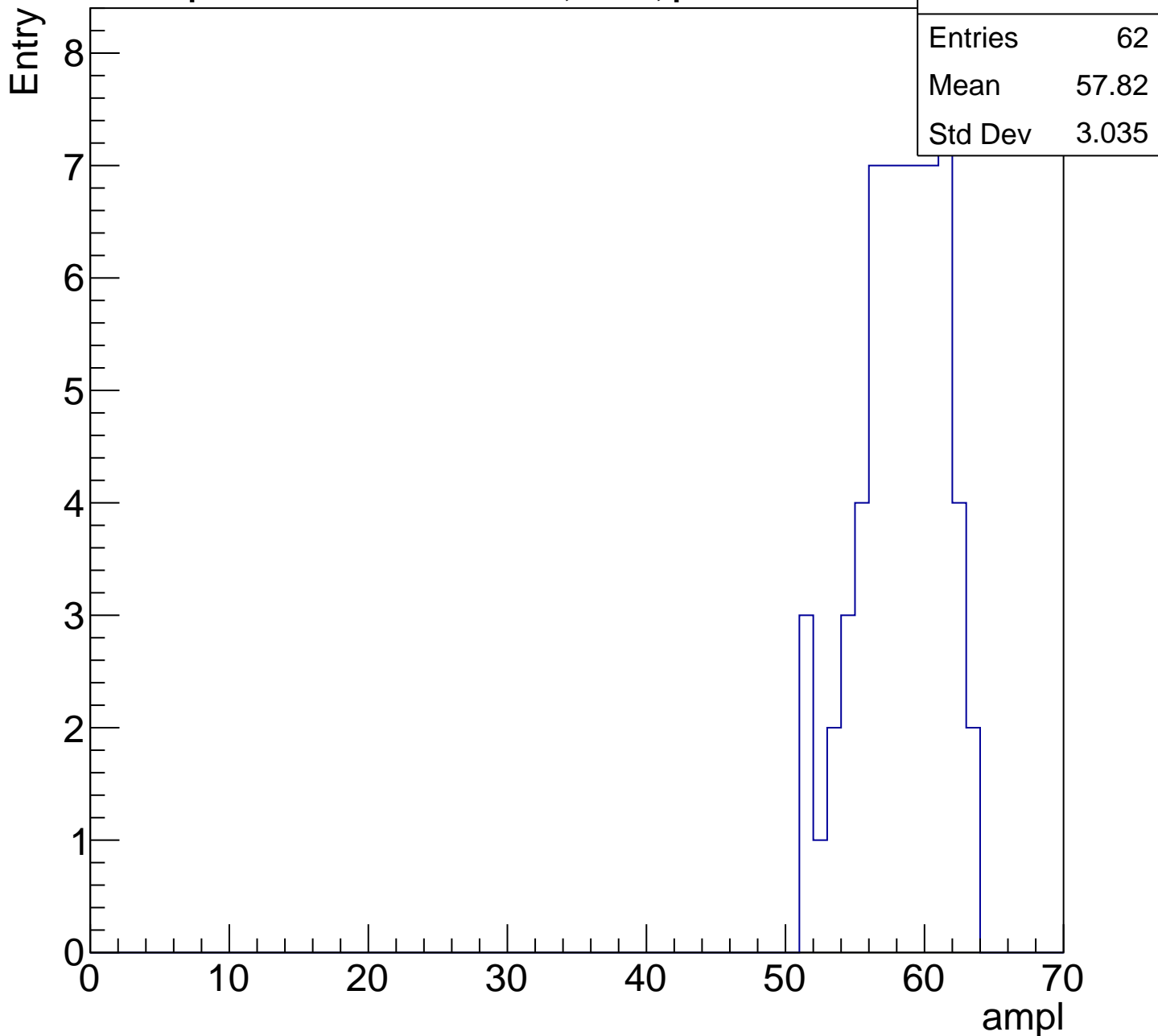
Entry

|         |       |
|---------|-------|
| Entries | 38    |
| Mean    | 51.29 |
| Std Dev | 8.494 |



# B1L103S, U4-ch82, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

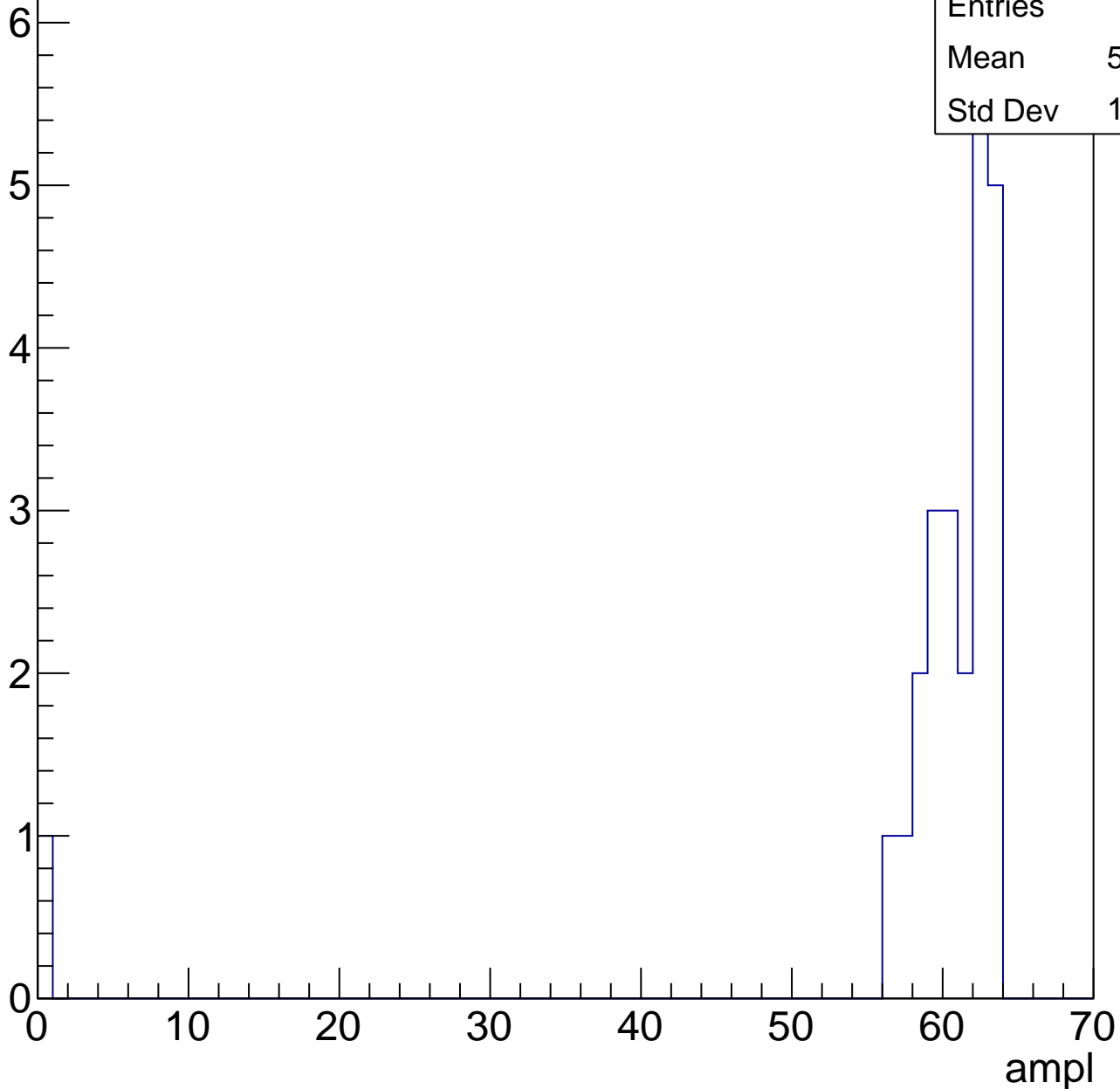


# B1L103S, U4-ch82, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 24    |
| Mean    | 58.12 |
| Std Dev | 12.29 |



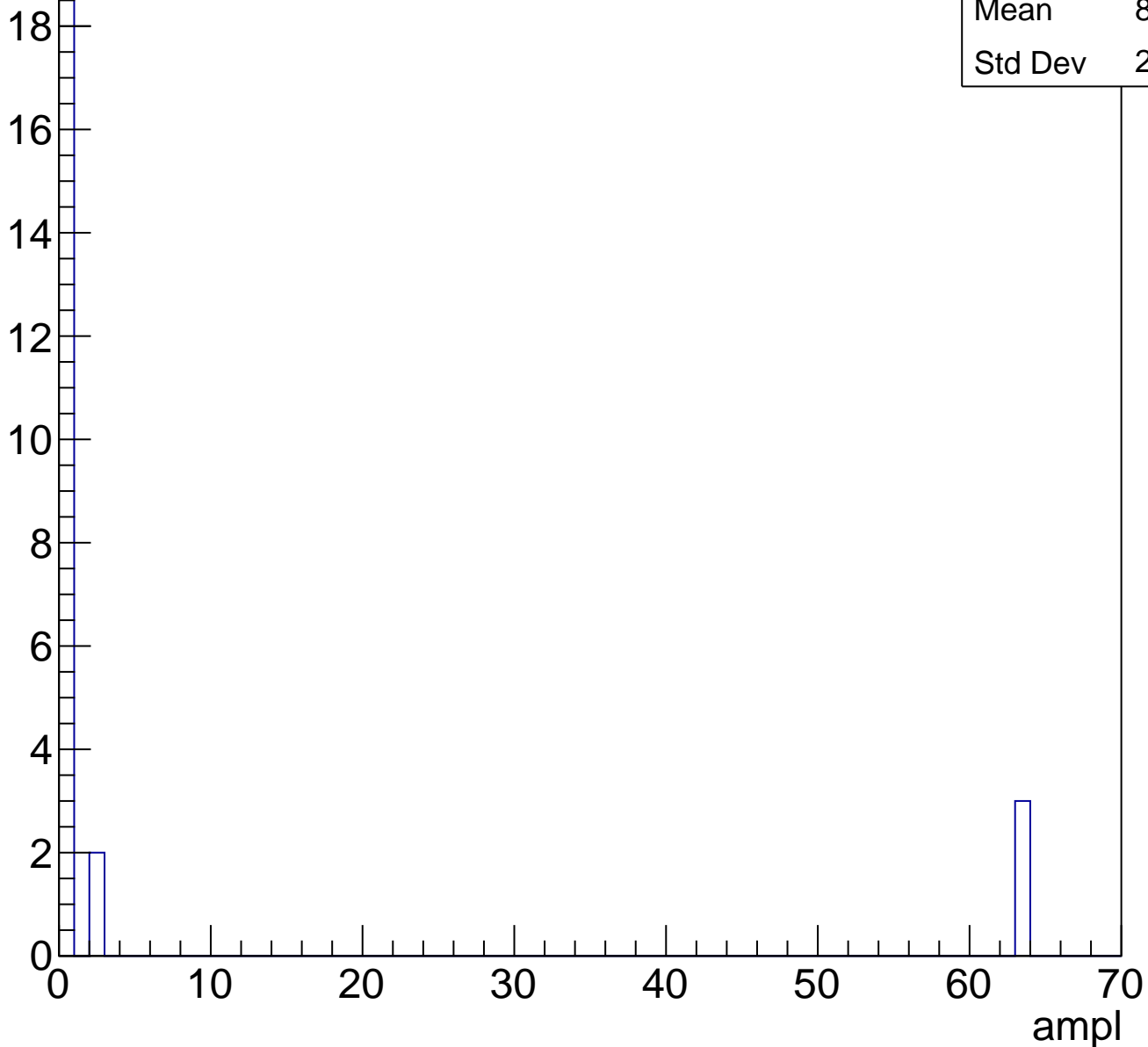


# B1L103S, U4-ch82, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 24    |
| Mean    | 8.042 |
| Std Dev | 20.78 |

Entry

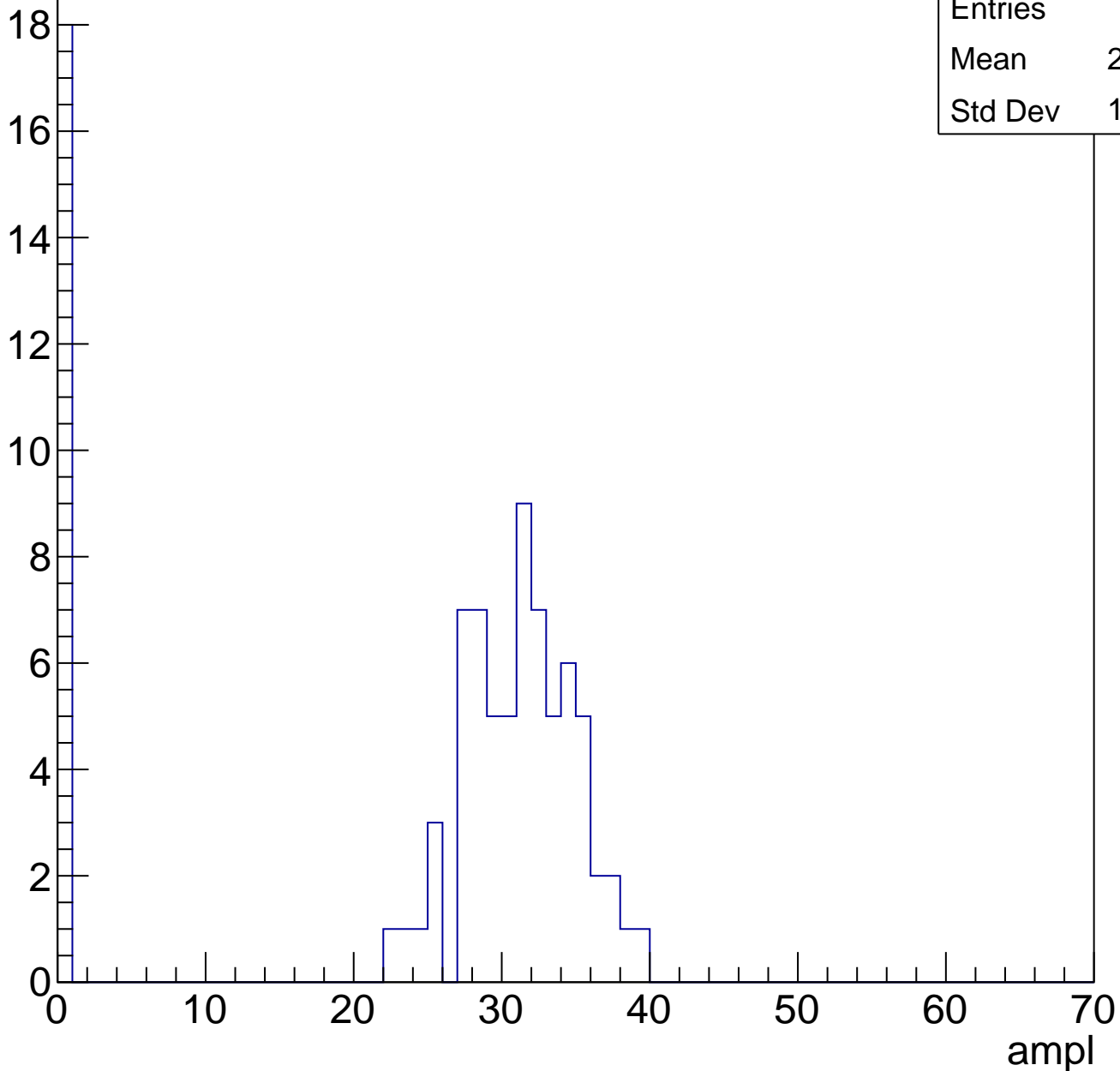


# B1L103S, U4-ch83, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 86    |
| Mean    | 24.35 |
| Std Dev | 12.94 |

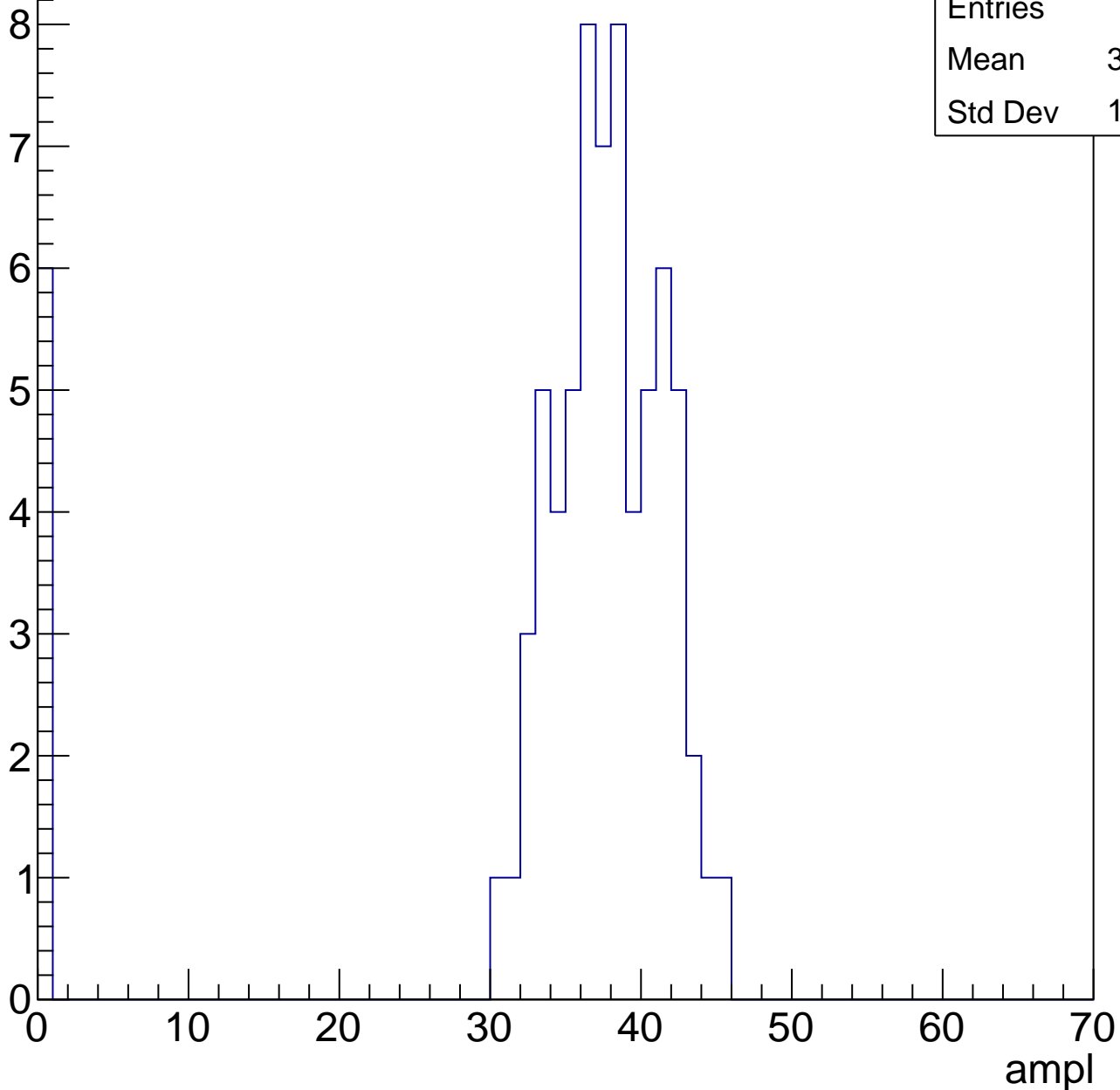
Entry



# B1L103S, U4-ch83, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



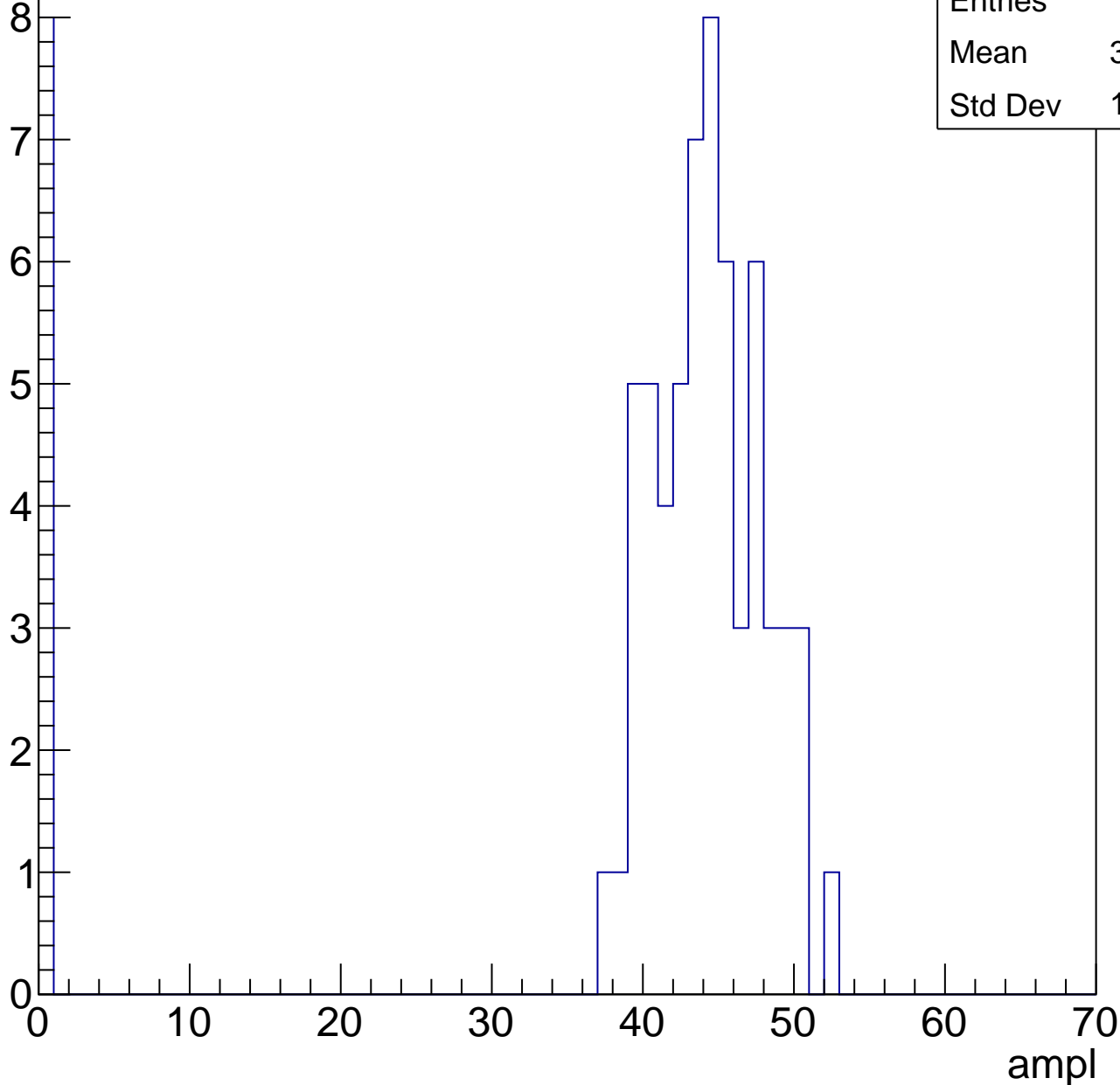
|         |       |
|---------|-------|
| Entries | 72    |
| Mean    | 34.32 |
| Std Dev | 10.85 |

# B1L103S, U4-ch83, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 69    |
| Mean    | 38.84 |
| Std Dev | 14.43 |

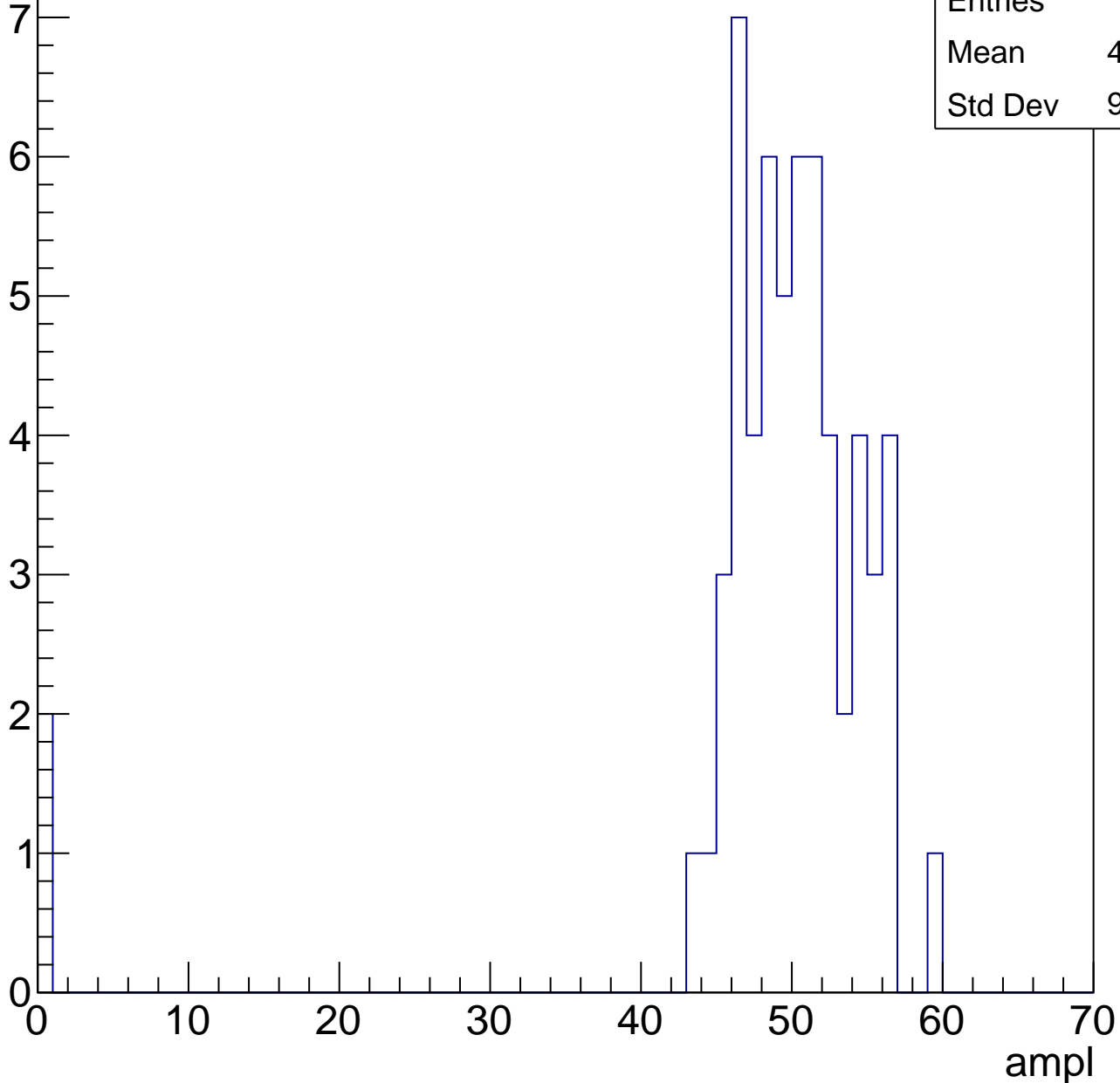


# B1L103S, U4-ch83, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 59    |
| Mean    | 48.29 |
| Std Dev | 9.715 |

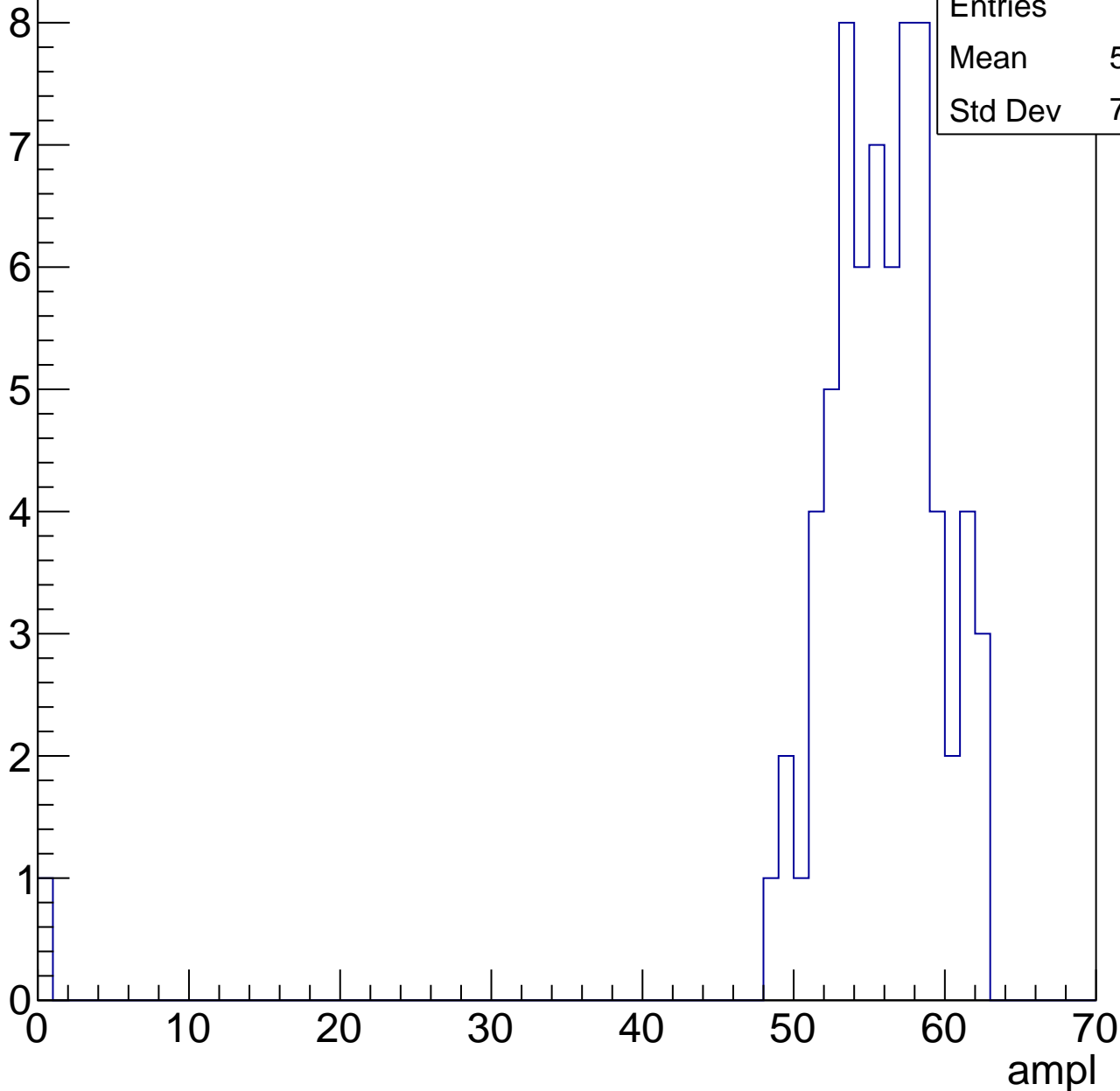


# B1L103S, U4-ch83, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

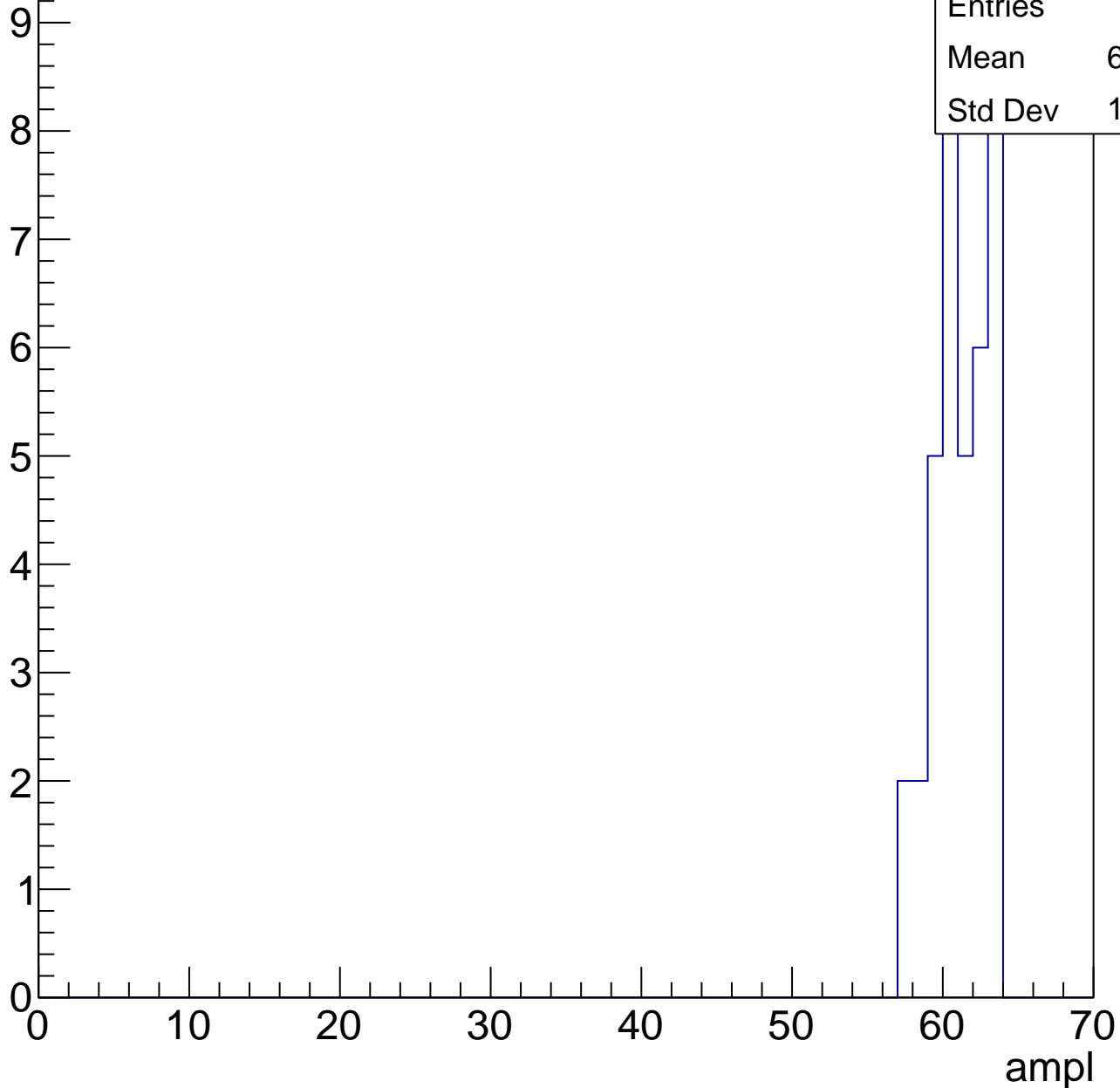
|         |       |
|---------|-------|
| Entries | 70    |
| Mean    | 54.79 |
| Std Dev | 7.397 |



# B1L103S, U4-ch83, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U4-ch83, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

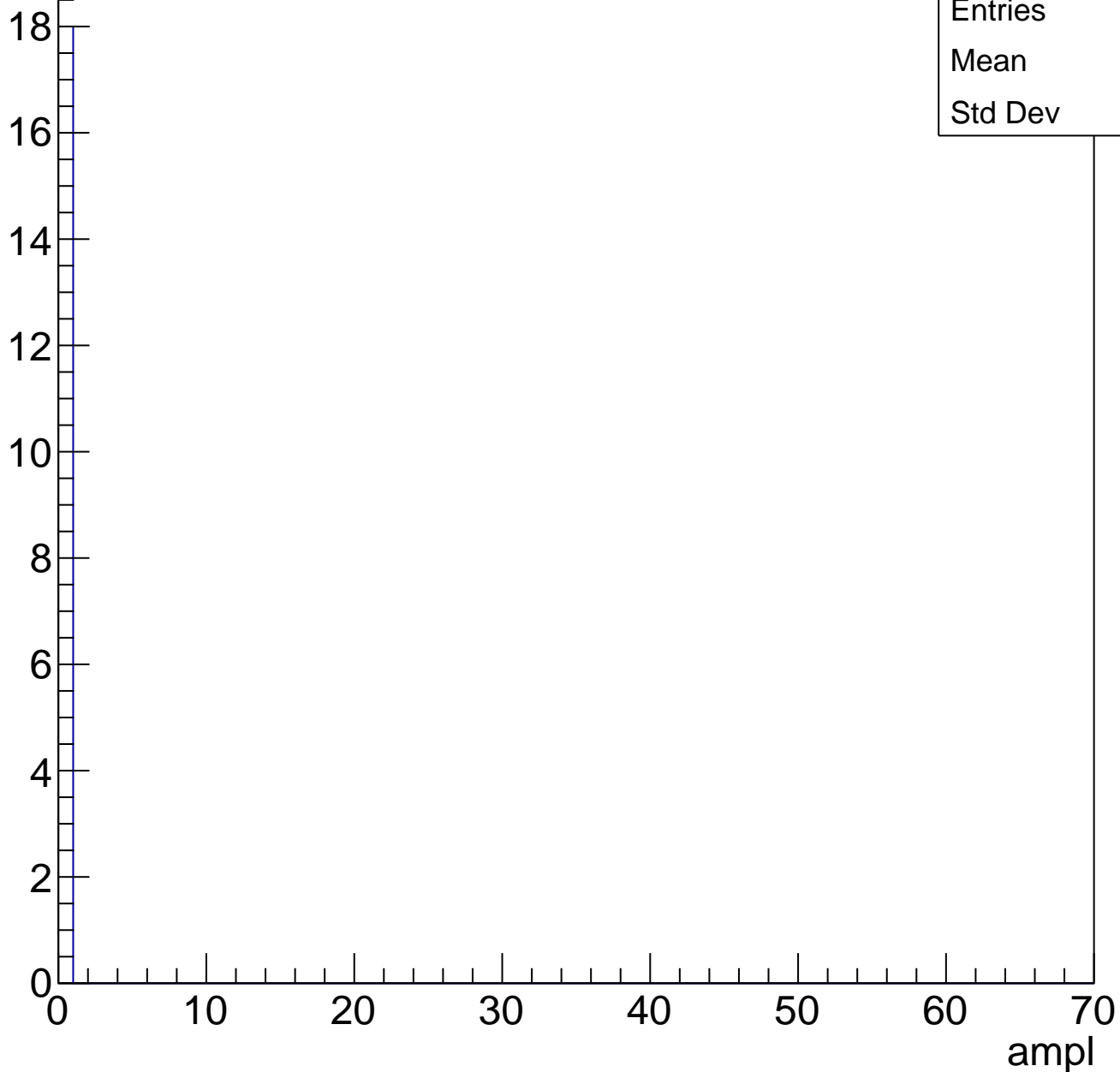




# B1L103S, U4-ch83, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



|         |    |
|---------|----|
| Entries | 18 |
| Mean    | 0  |
| Std Dev | 0  |

# B1L103S, U4-ch84, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

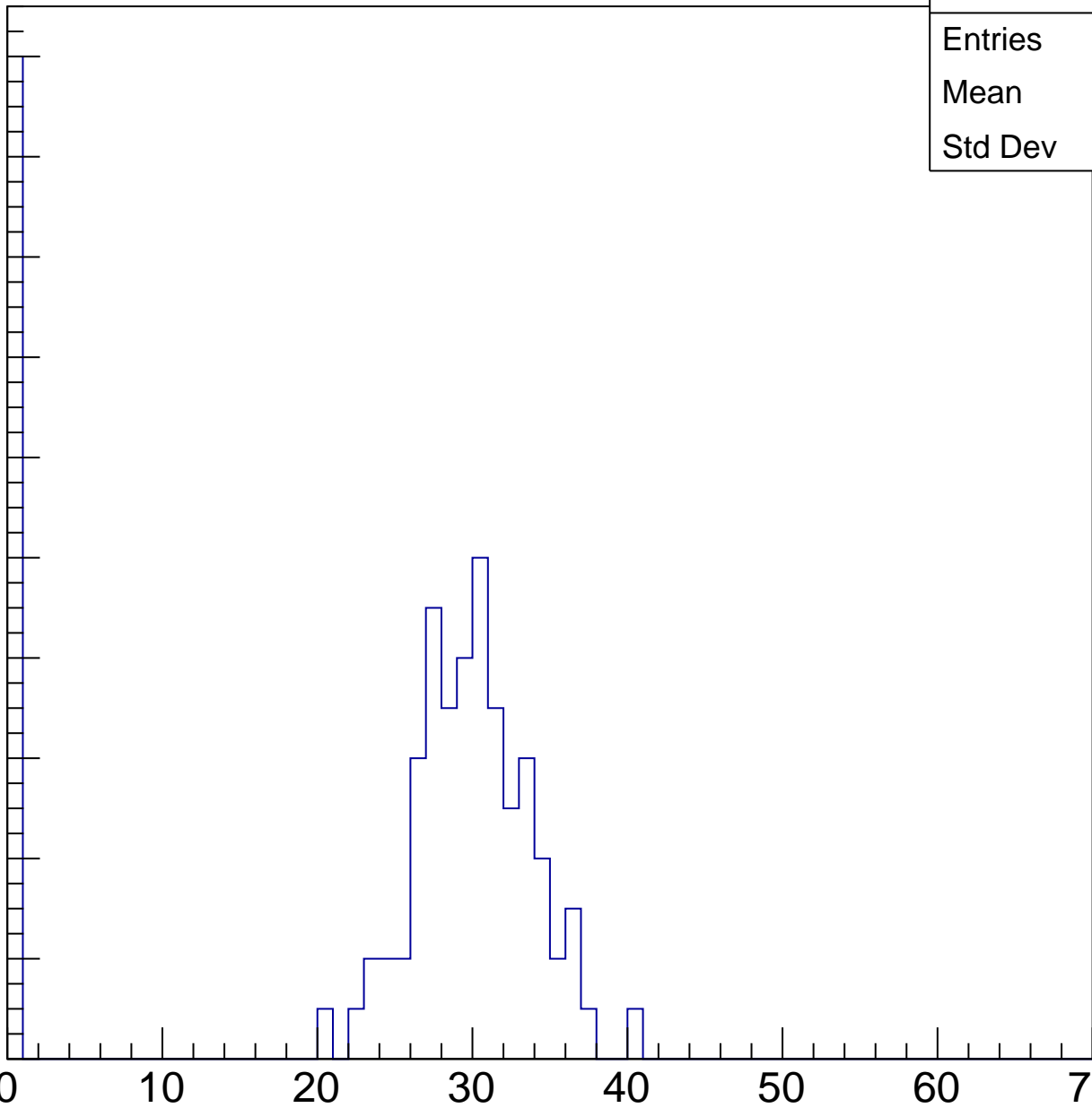
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

|         |       |
|---------|-------|
| Entries | 97    |
| Mean    | 23.49 |
| Std Dev | 12.41 |

0 10 20 30 40 50 60 70

ampl

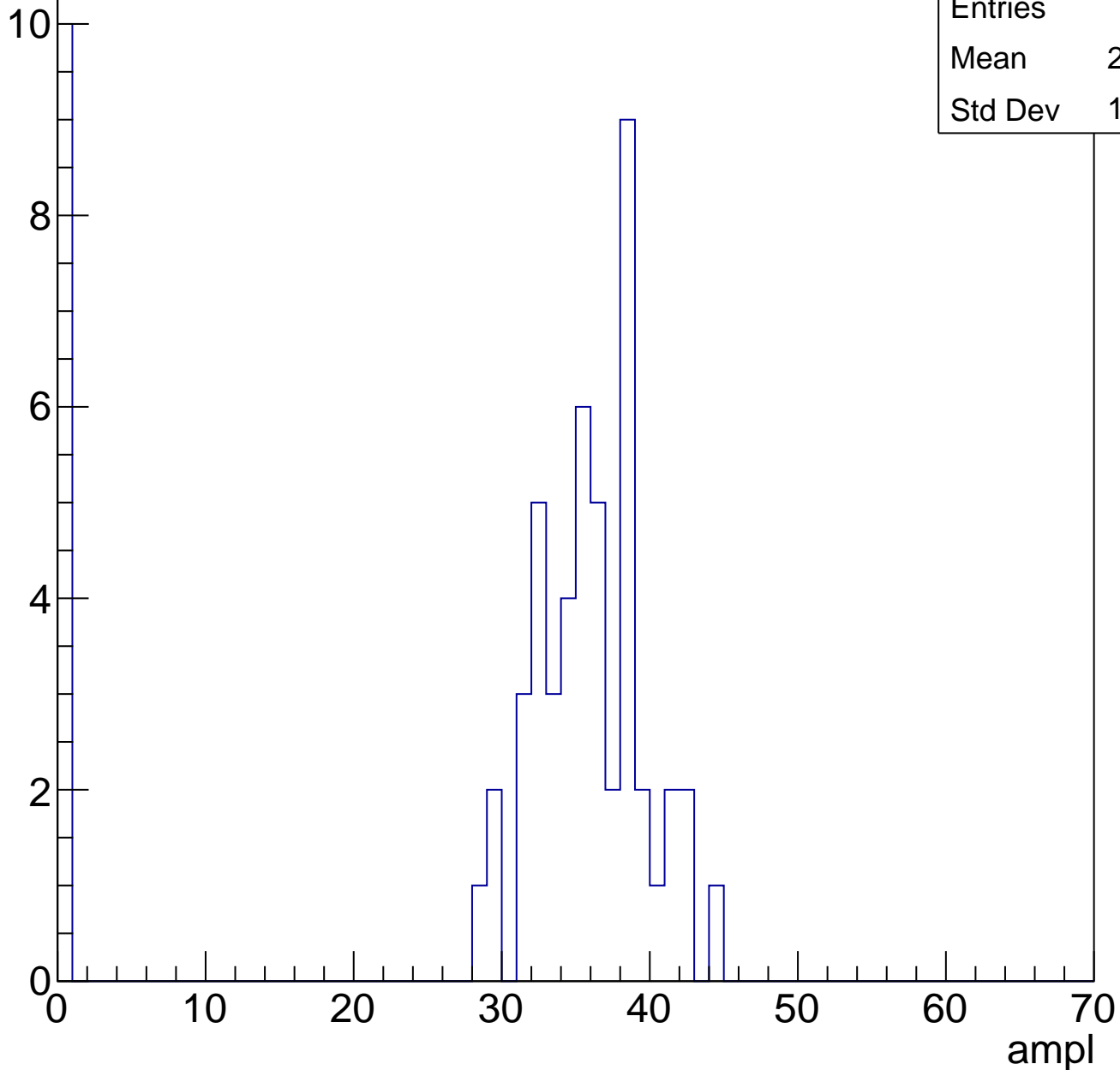


# B1L103S, U4-ch84, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 58    |
| Mean    | 29.45 |
| Std Dev | 13.83 |

Entry

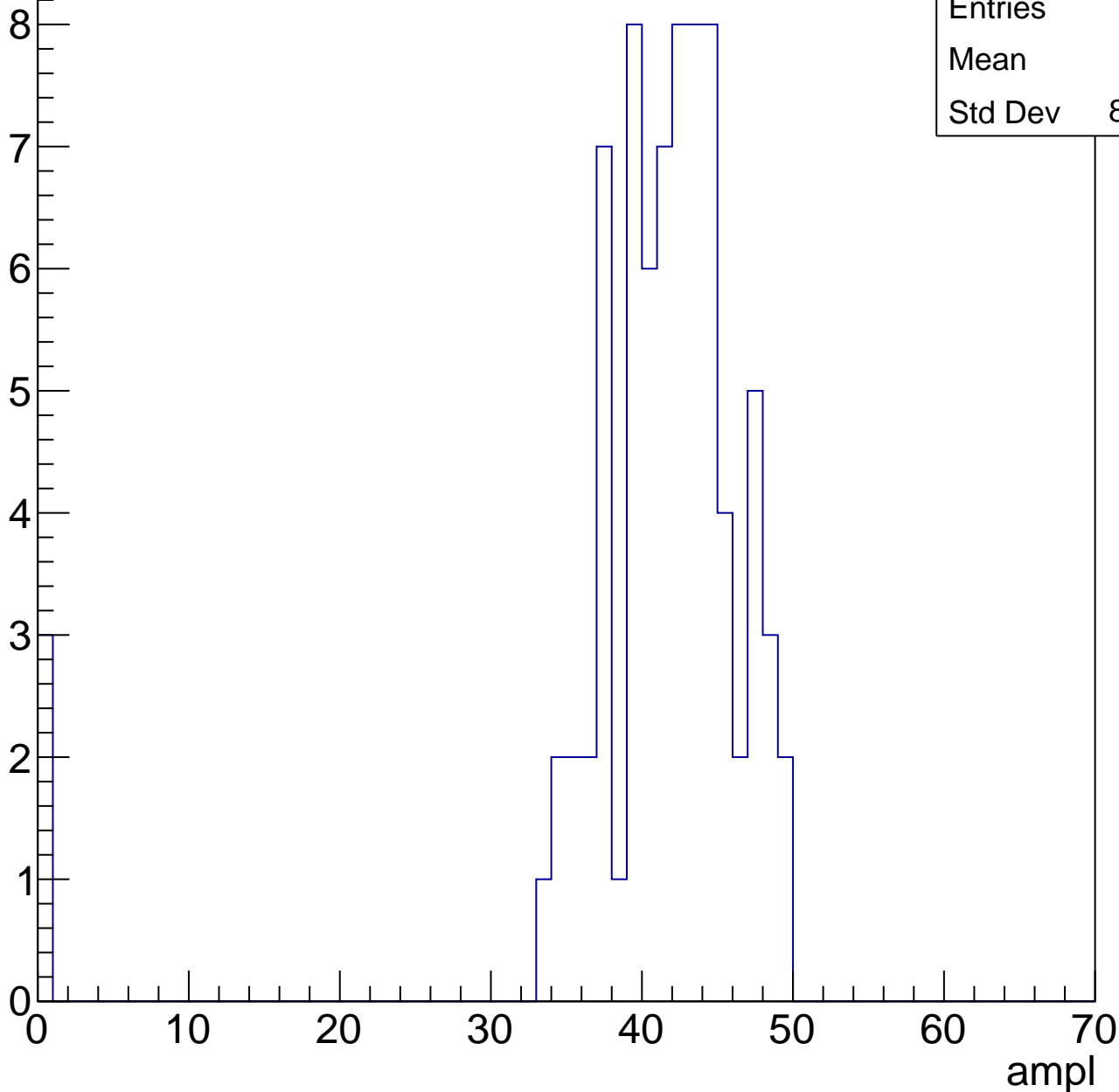


# B1L103S, U4-ch84, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 79    |
| Mean    | 40    |
| Std Dev | 8.779 |

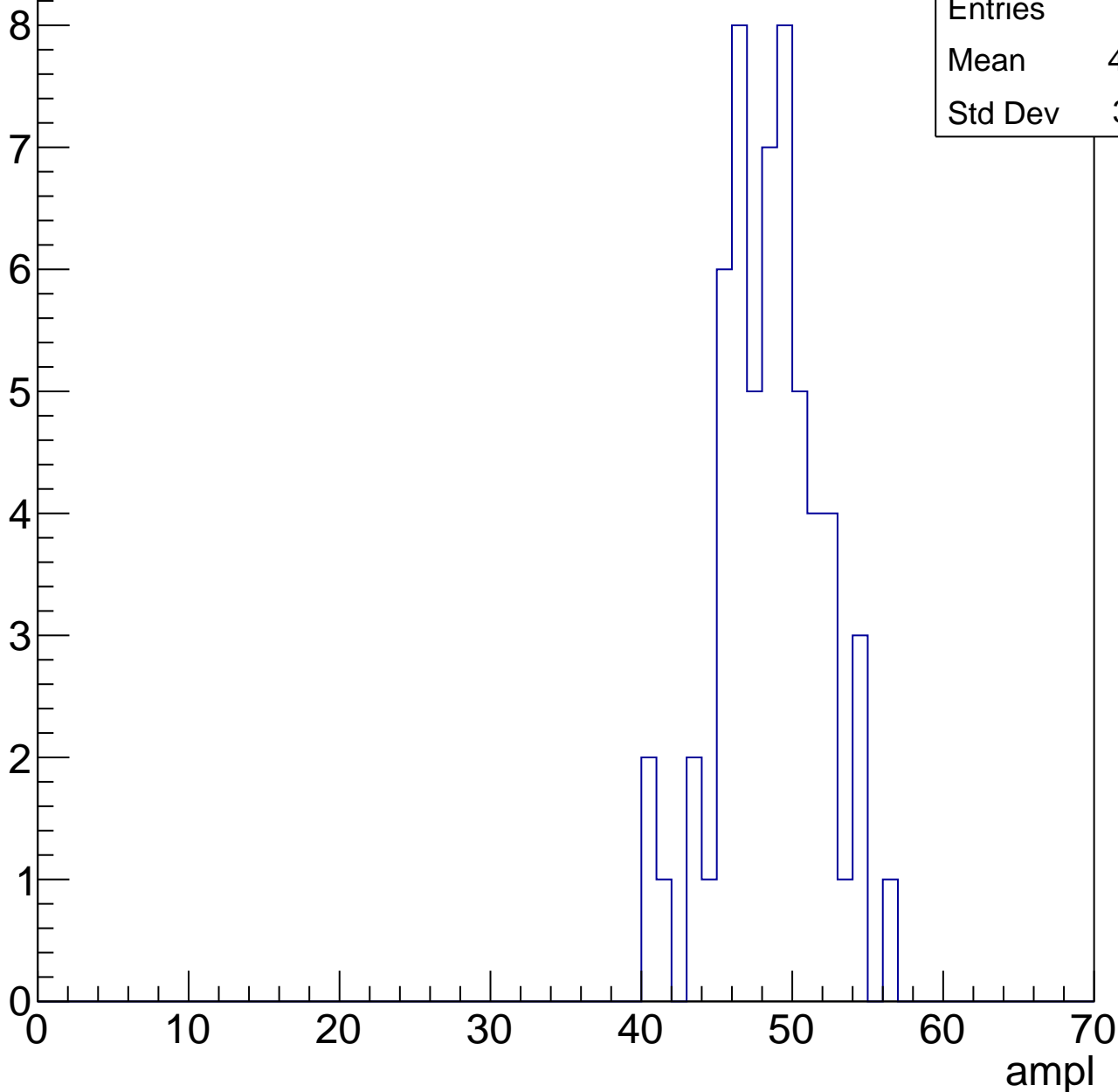


# B1L103S, U4-ch84, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

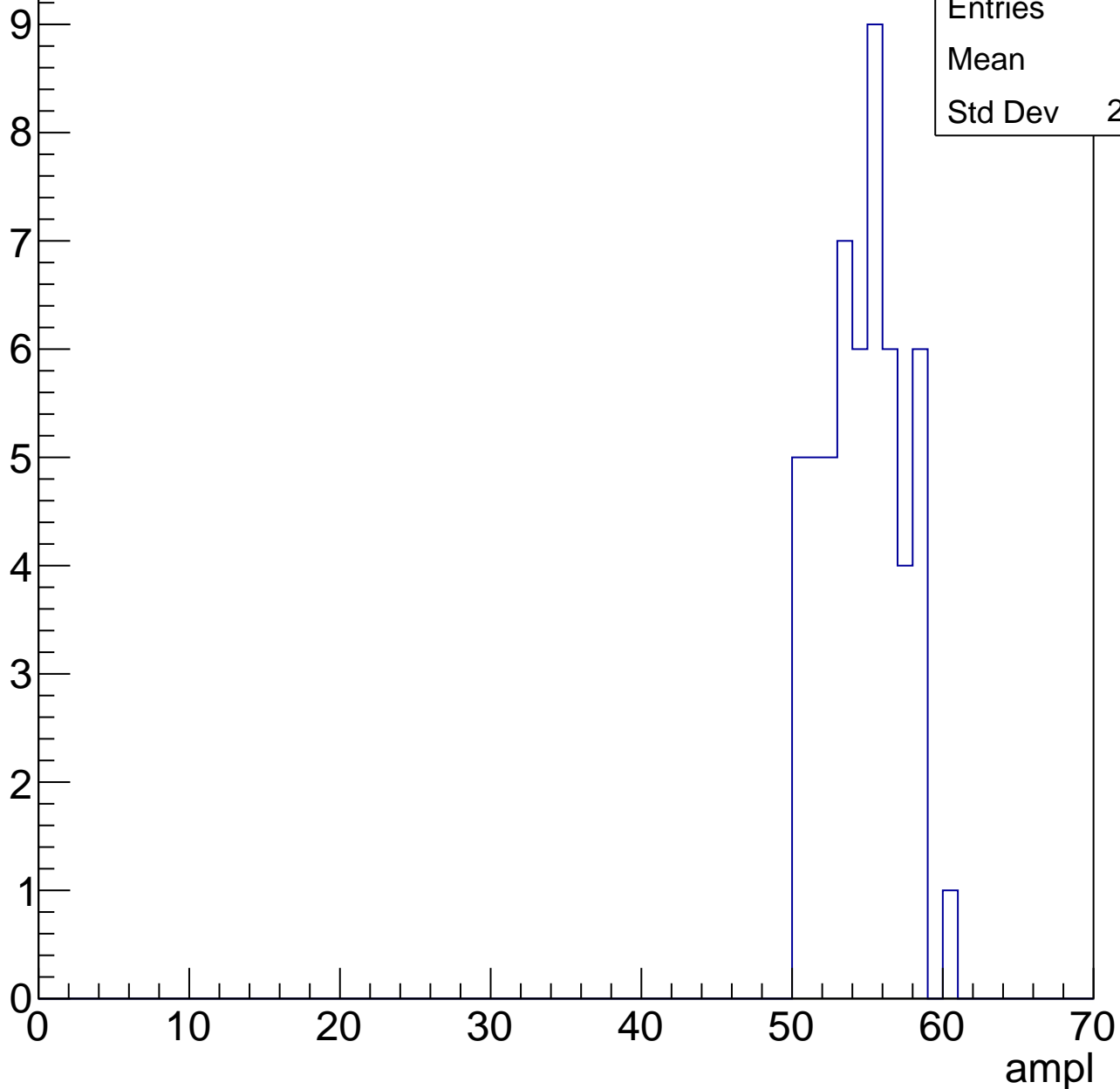
|         |       |
|---------|-------|
| Entries | 58    |
| Mean    | 48.02 |
| Std Dev | 3.371 |



# B1L103S, U4-ch84, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

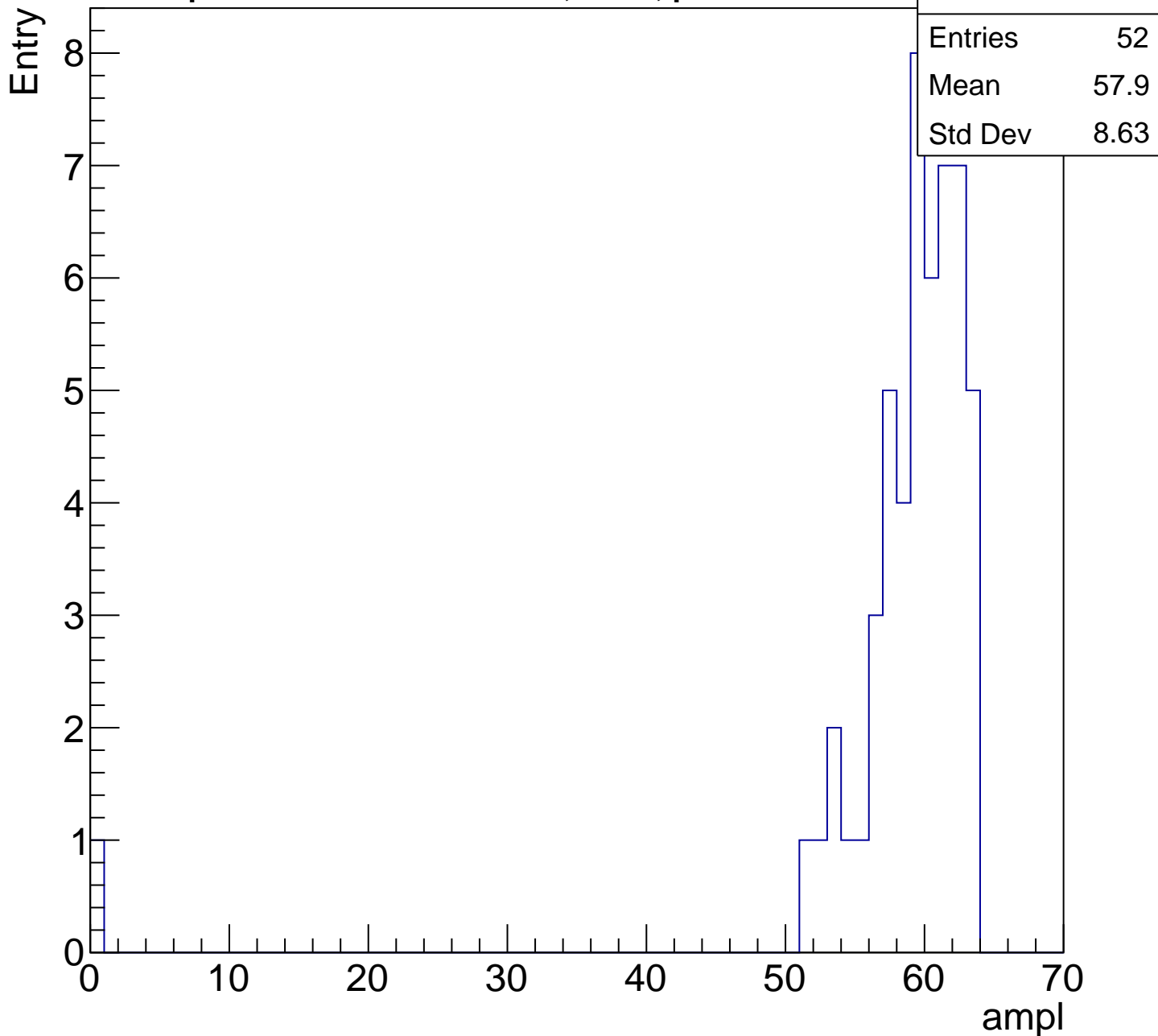
Entry



|         |       |
|---------|-------|
| Entries | 54    |
| Mean    | 54.2  |
| Std Dev | 2.549 |

# B1L103S, U4-ch84, adc5

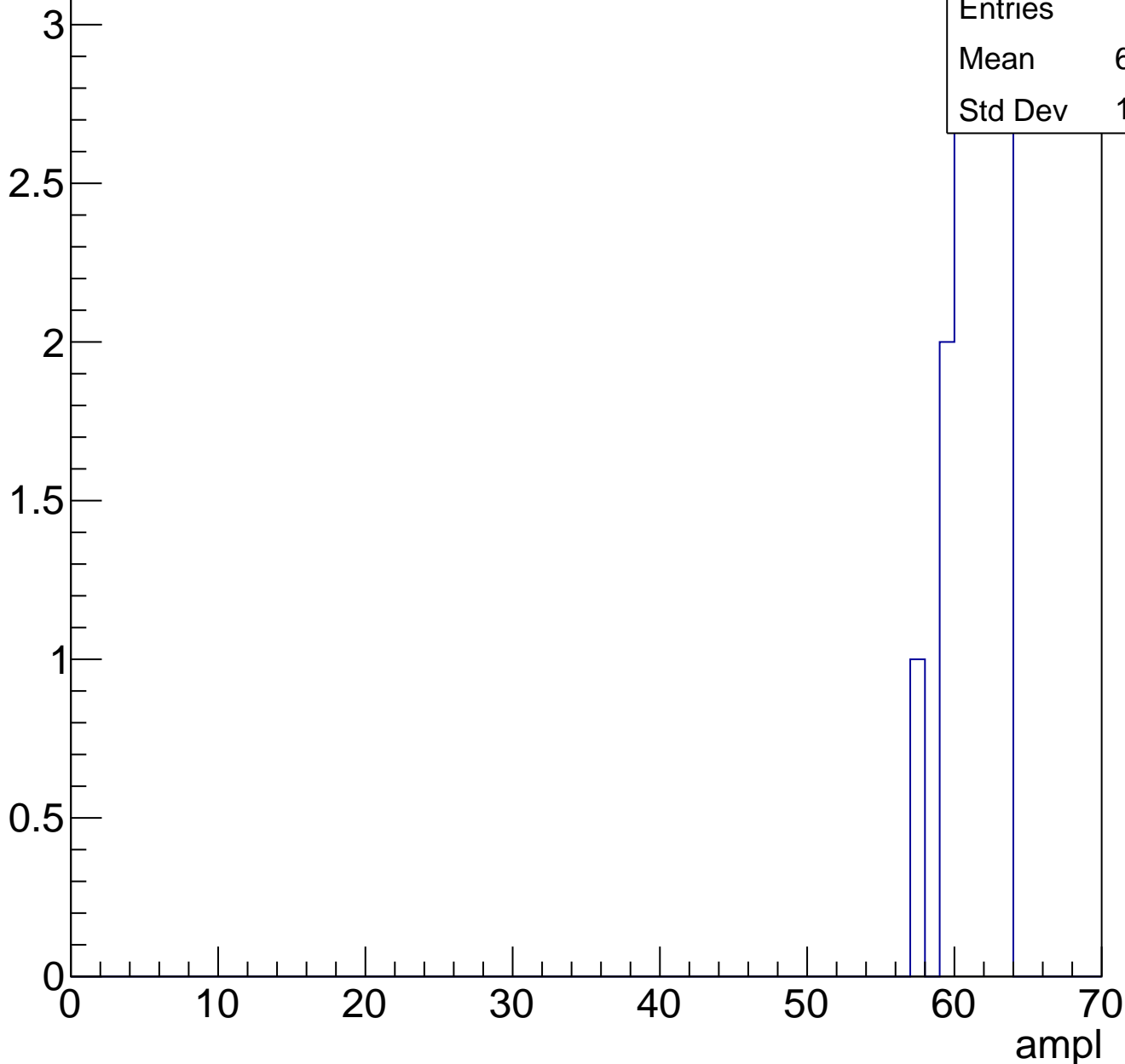
calib\_packv5\_041523\_1651.root, FC#0, port C2



# B1L103S, U4-ch84, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U4-ch84, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

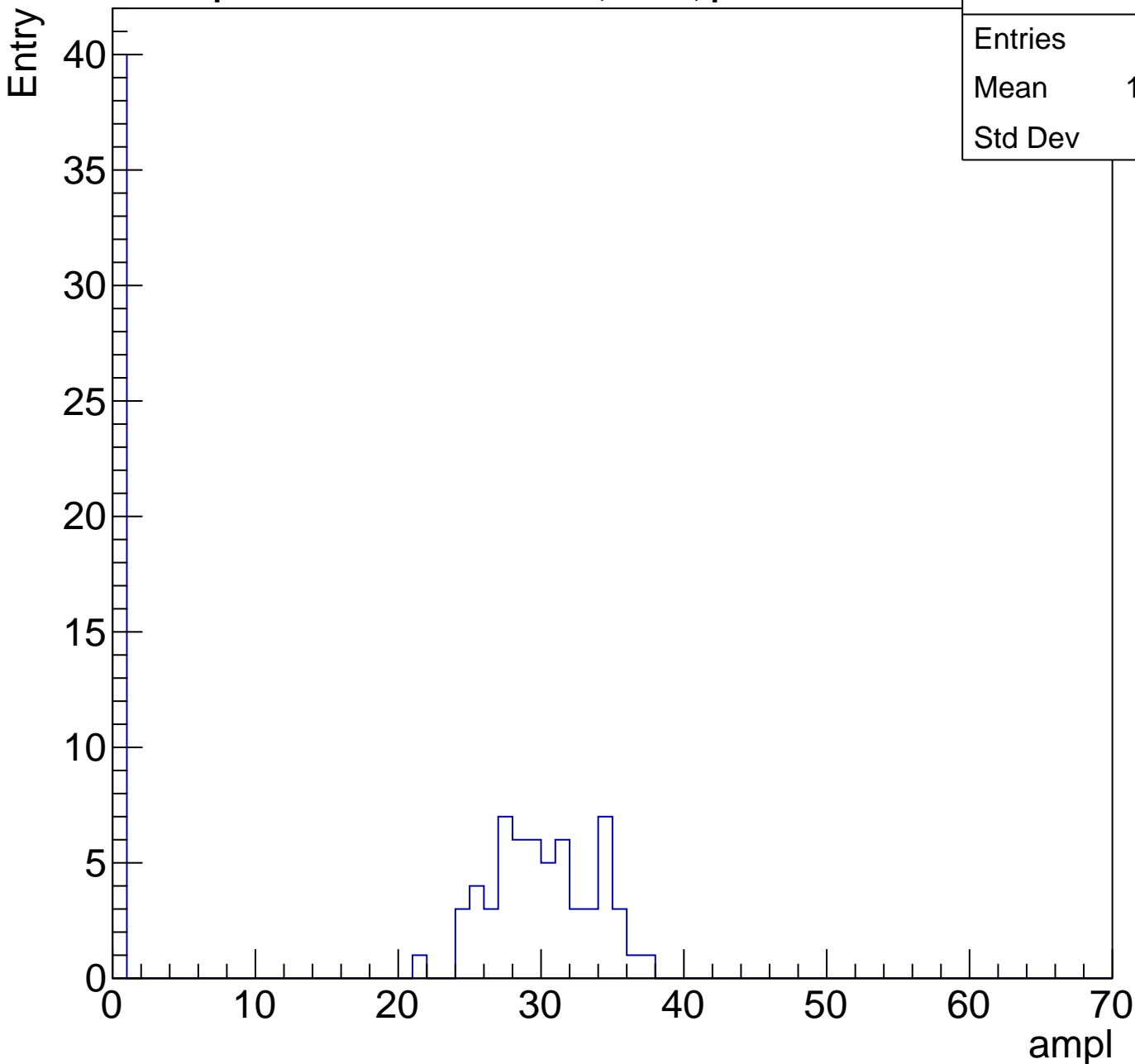
Entry



# B1L103S, U4-ch85, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 99    |
| Mean    | 17.67 |
| Std Dev | 14.8  |



# B1L103S, U4-ch85, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 78    |
| Mean    | 29.83 |
| Std Dev | 13.76 |

Entry

12

10

8

6

4

2

0

0

10

20

30

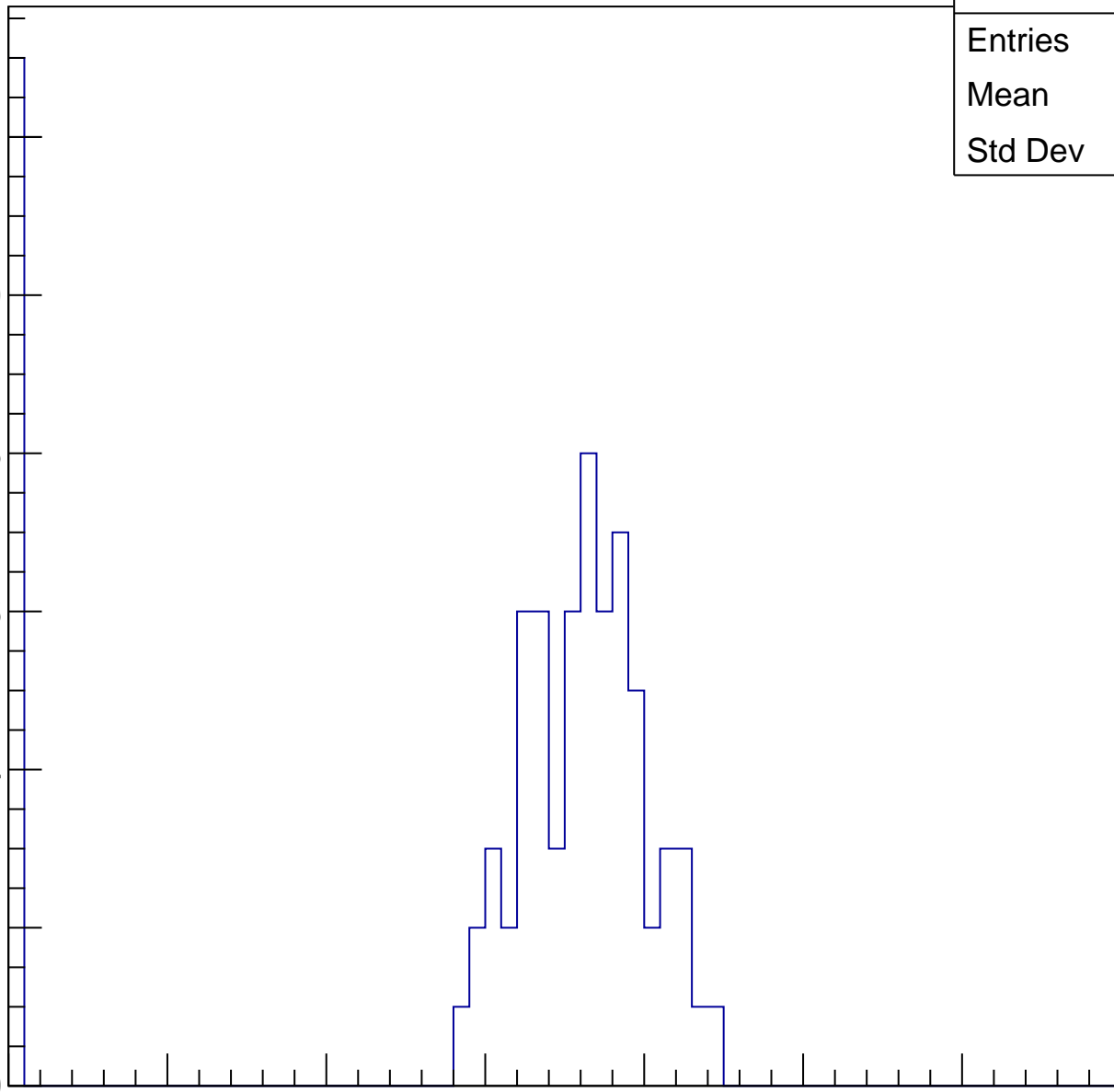
40

50

60

70

ampl

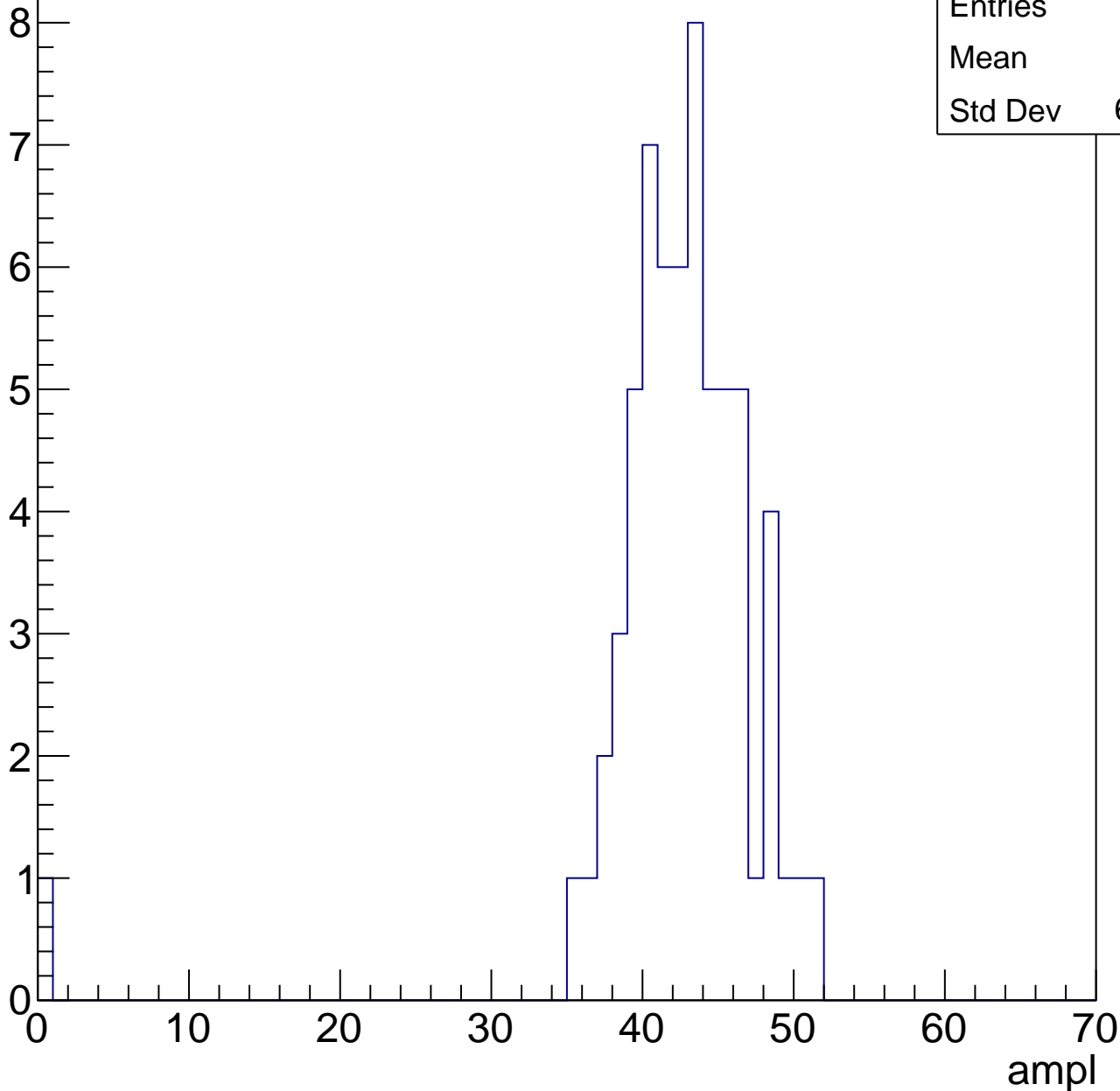


# B1L103S, U4-ch85, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

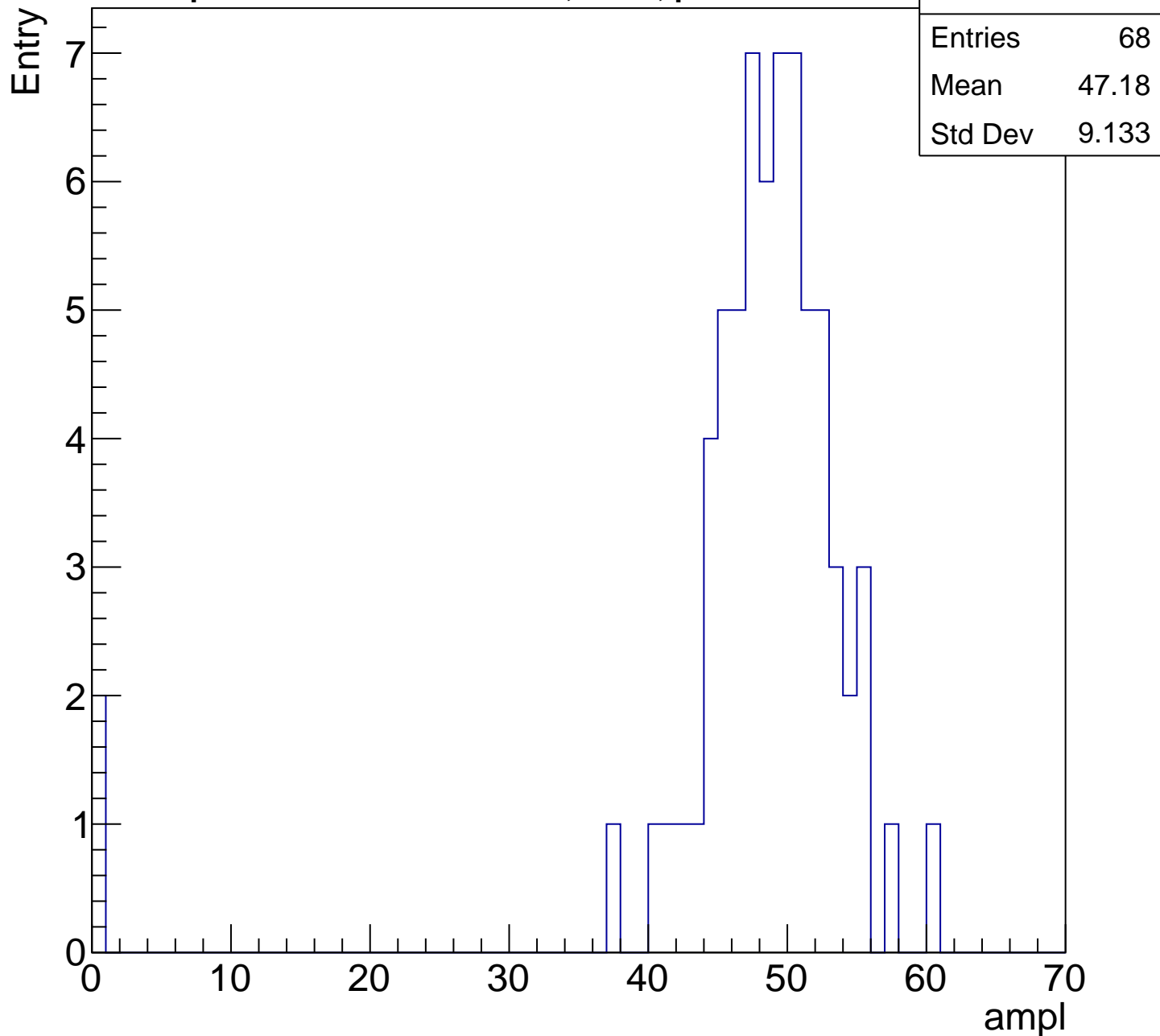
Entry

|         |       |
|---------|-------|
| Entries | 63    |
| Mean    | 41.9  |
| Std Dev | 6.351 |



# B1L103S, U4-ch85, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

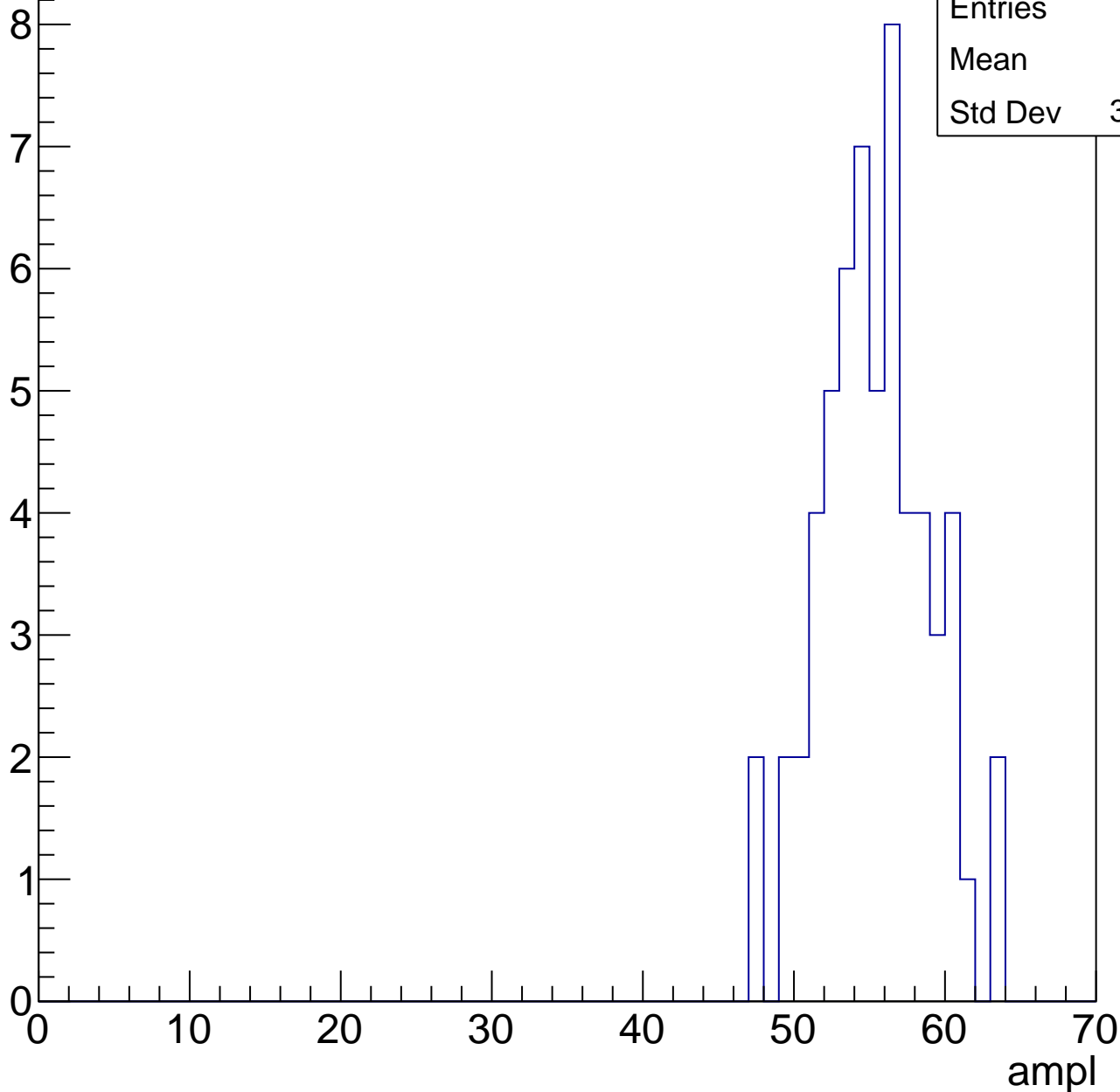


# B1L103S, U4-ch85, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

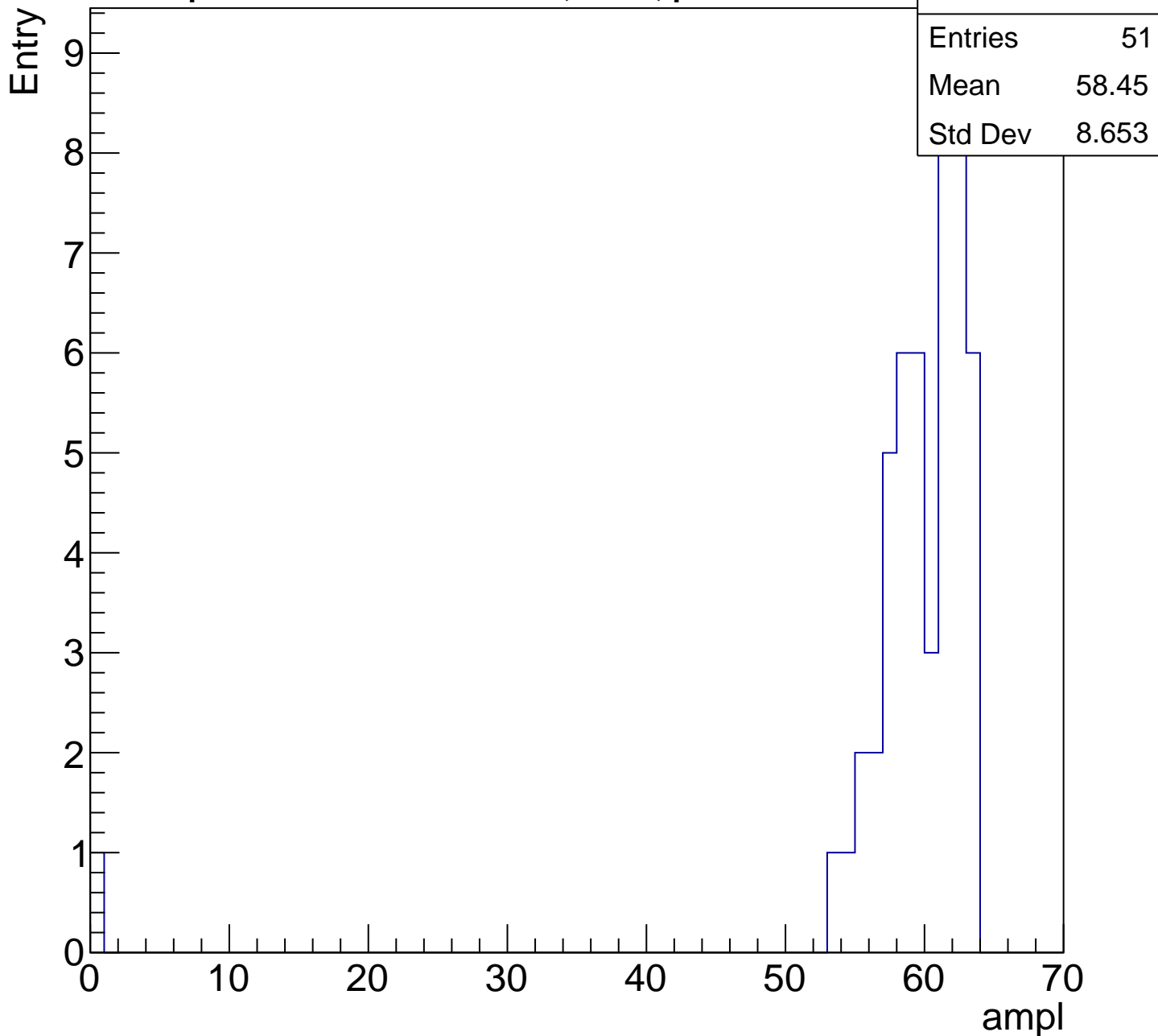
Entry

|         |       |
|---------|-------|
| Entries | 59    |
| Mean    | 54.9  |
| Std Dev | 3.592 |



# B1L103S, U4-ch85, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2



# B1L103S, U4-ch85, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

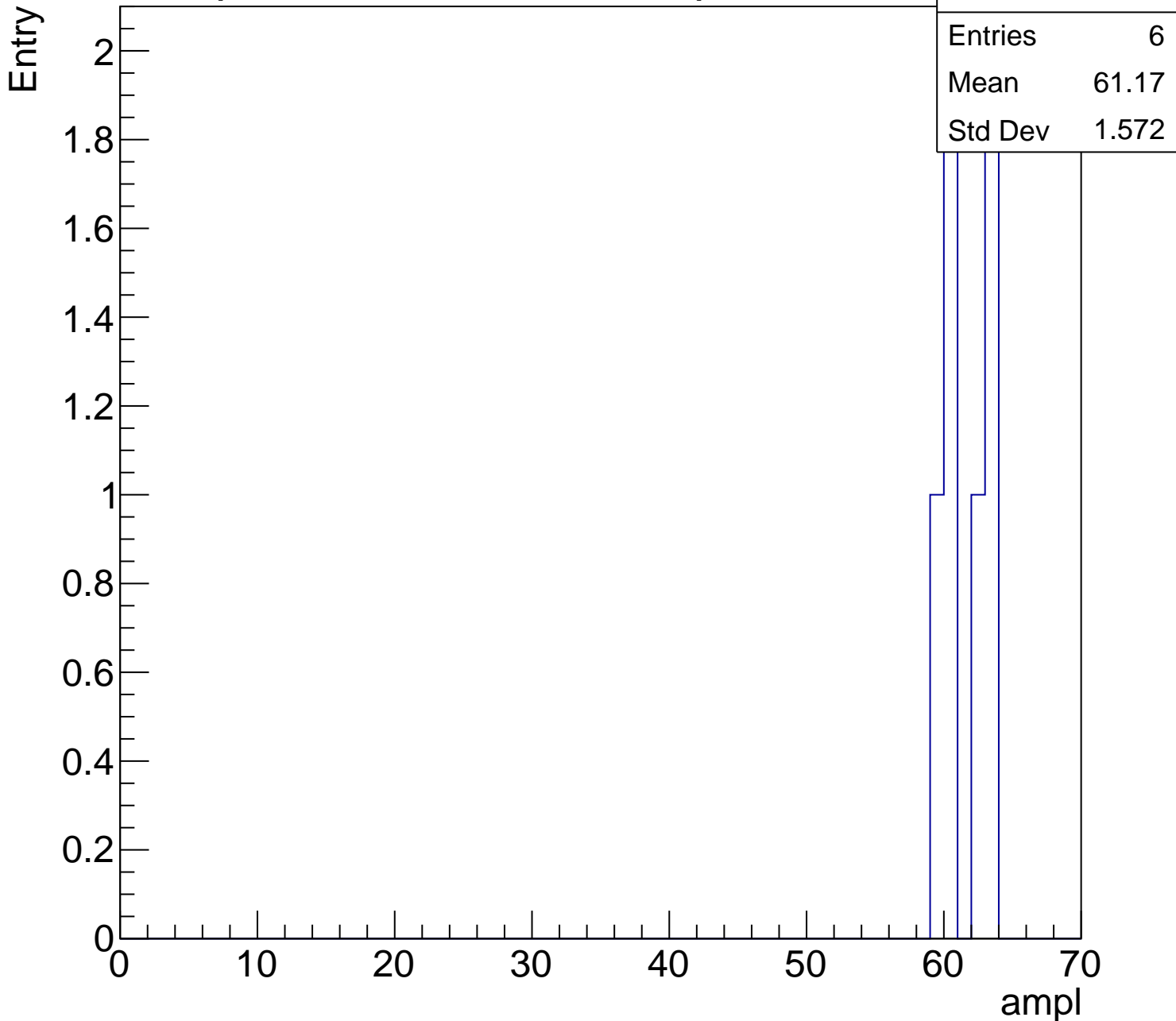
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

|         |       |
|---------|-------|
| Entries | 6     |
| Mean    | 61.17 |
| Std Dev | 1.572 |

0 10 20 30 40 50 60 70

ampl





# B1L103S, U4-ch85, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

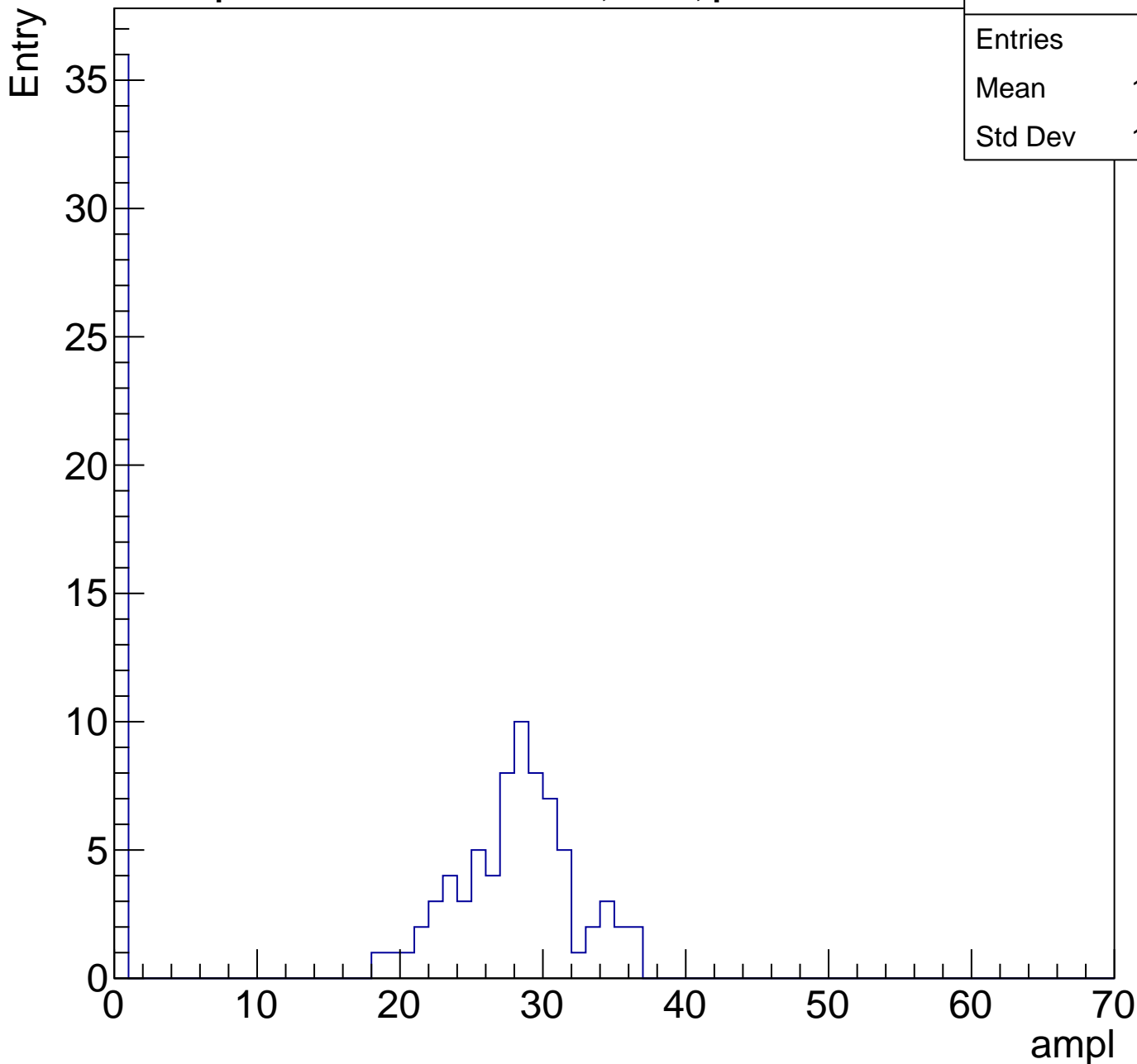
|         |    |
|---------|----|
| Entries | 19 |
| Mean    | 0  |
| Std Dev | 0  |

ampl

# B1L103S, U4-ch86, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 108   |
| Mean    | 18.45 |
| Std Dev | 13.45 |



# B1L103S, U4-ch86, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 69    |
| Mean    | 27.45 |
| Std Dev | 13.5  |

Entry

12

10

8

6

4

2

0

0

10

20

30

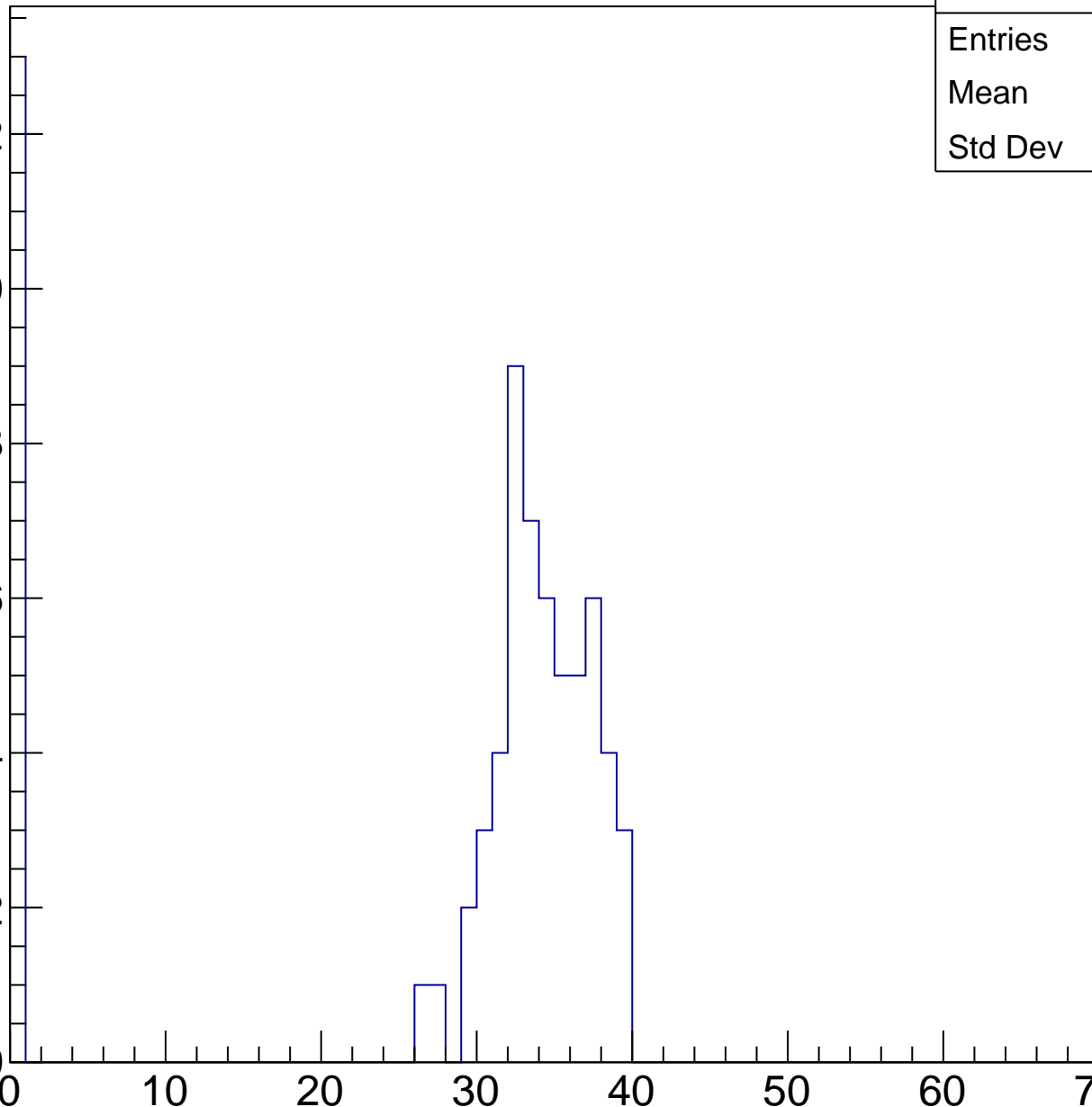
40

50

60

70

ampl

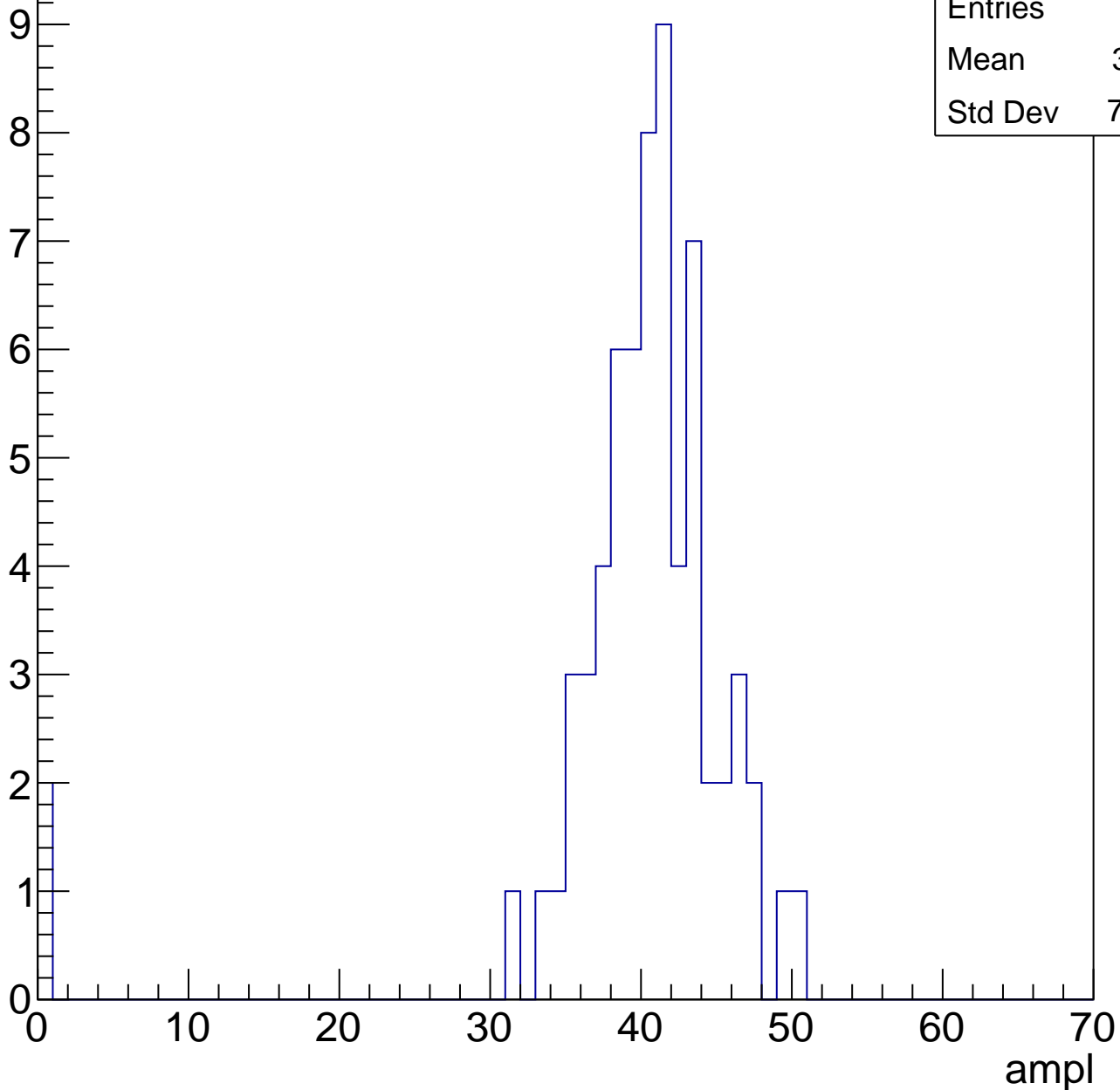


# B1L103S, U4-ch86, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 66    |
| Mean    | 39.21 |
| Std Dev | 7.854 |



# B1L103S, U4-ch86, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

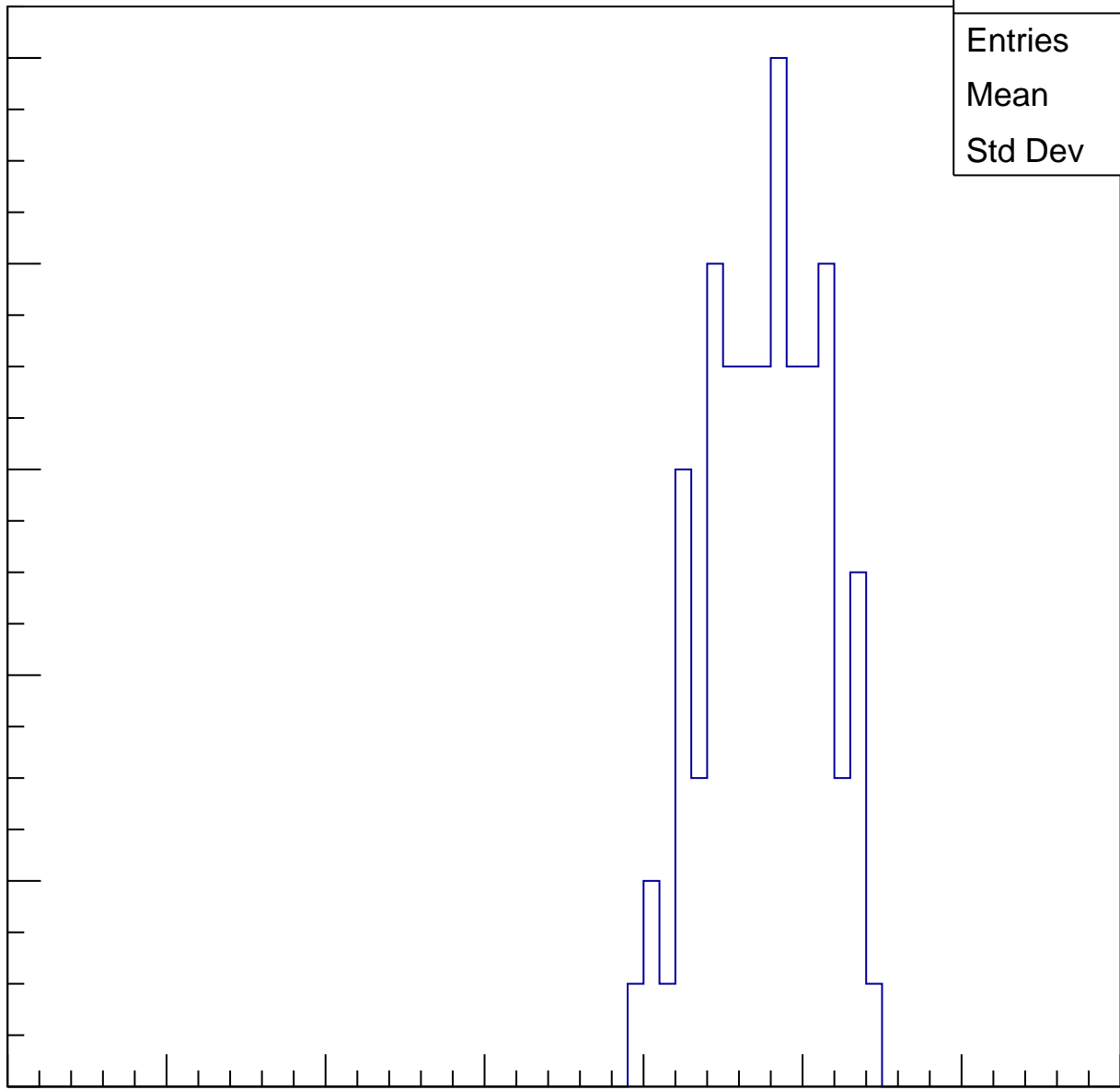
|         |       |
|---------|-------|
| Entries | 83    |
| Mean    | 47.17 |
| Std Dev | 3.529 |

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

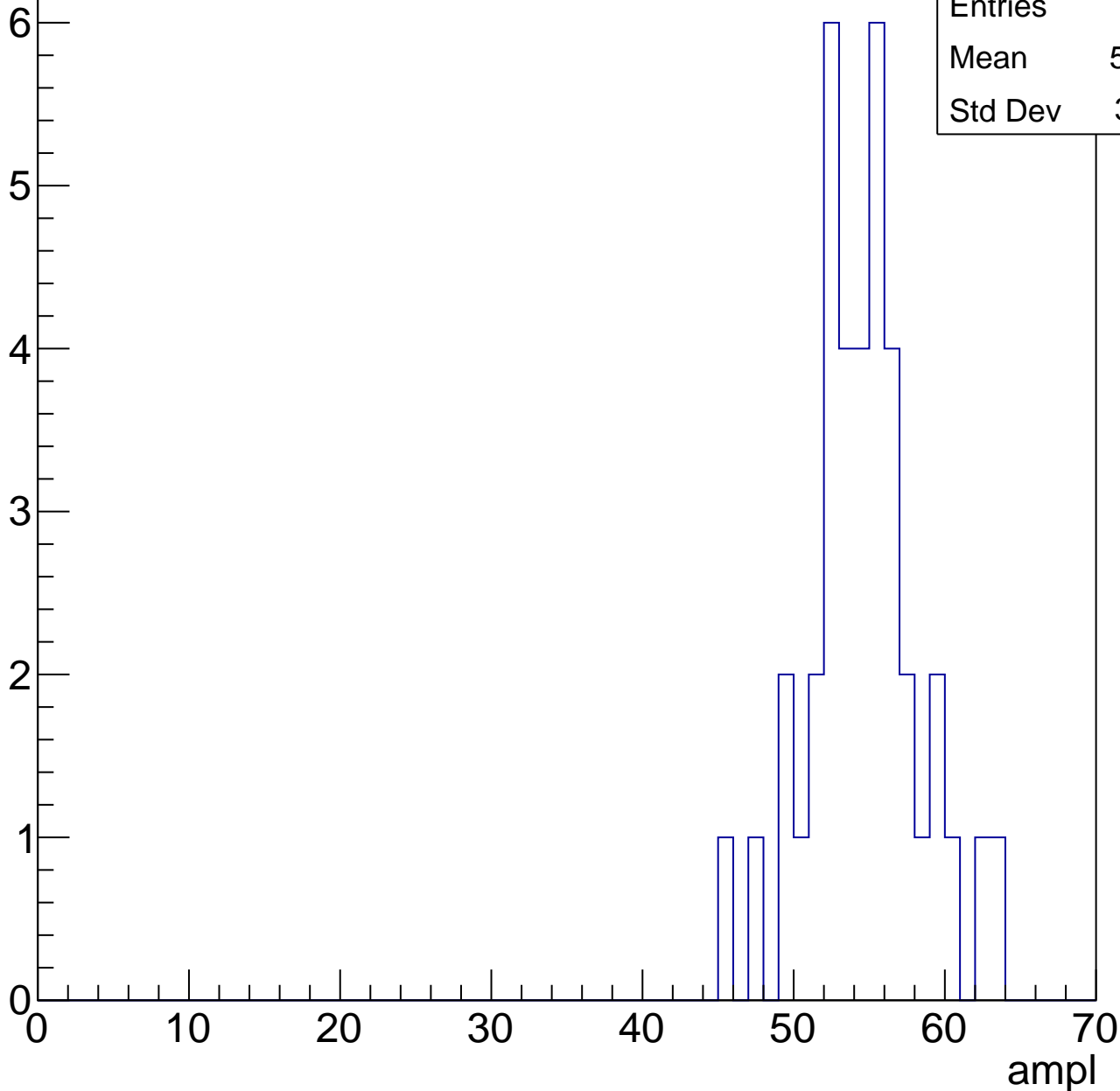


# B1L103S, U4-ch86, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 39    |
| Mean    | 54.13 |
| Std Dev | 3.681 |

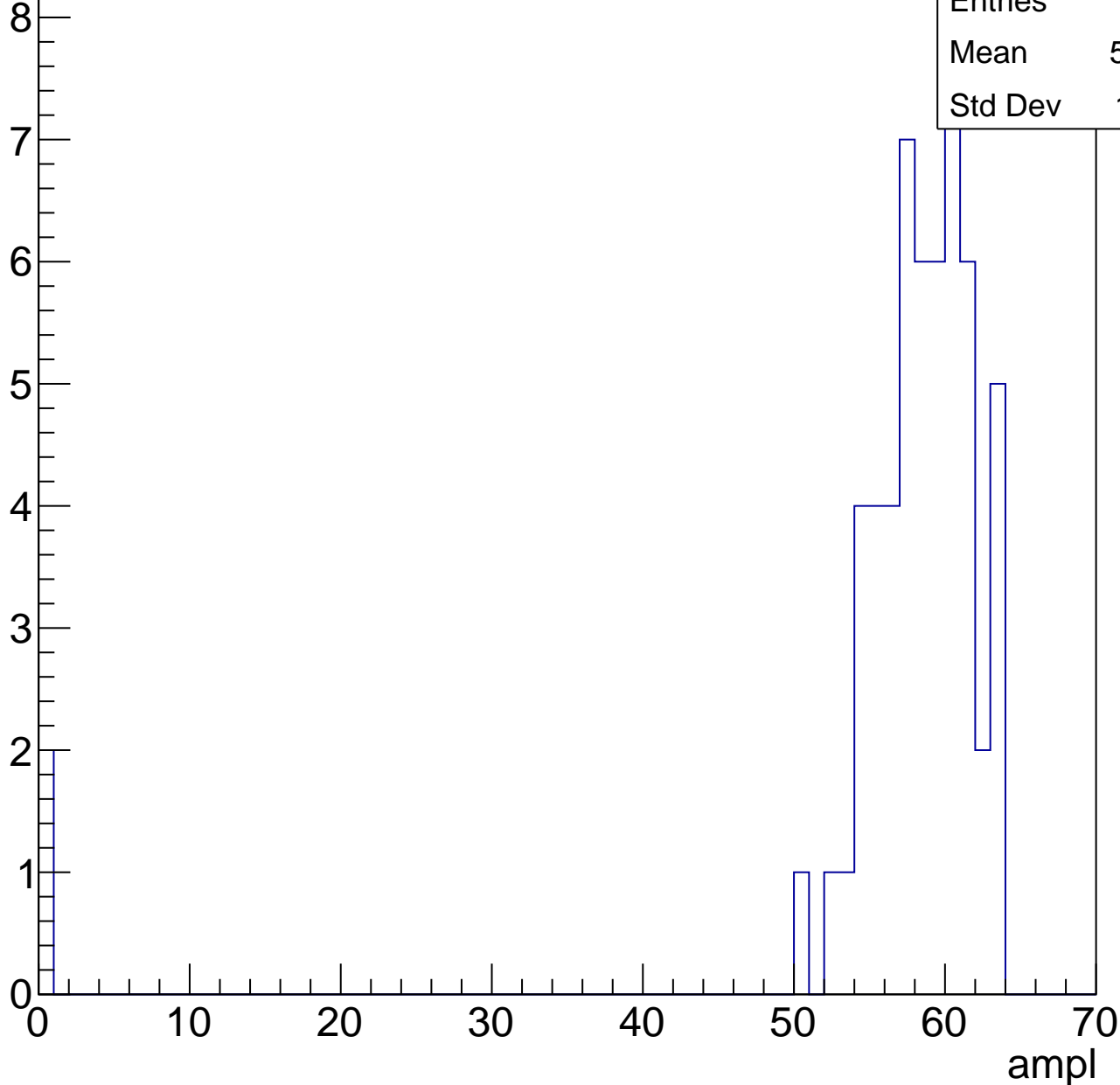


# B1L103S, U4-ch86, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 57    |
| Mean    | 56.16 |
| Std Dev | 11.11 |

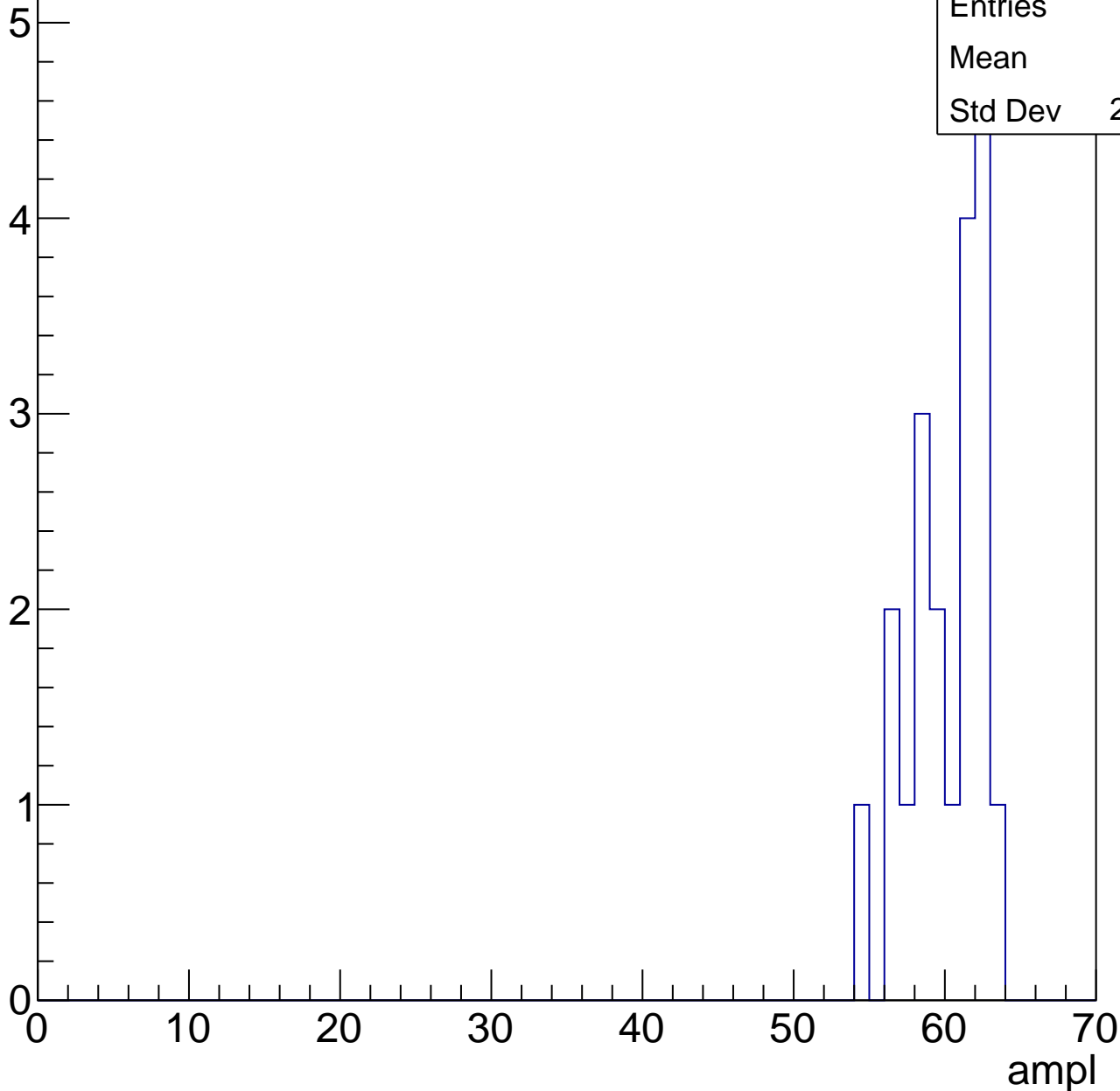


# B1L103S, U4-ch86, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 20    |
| Mean    | 59.6  |
| Std Dev | 2.458 |



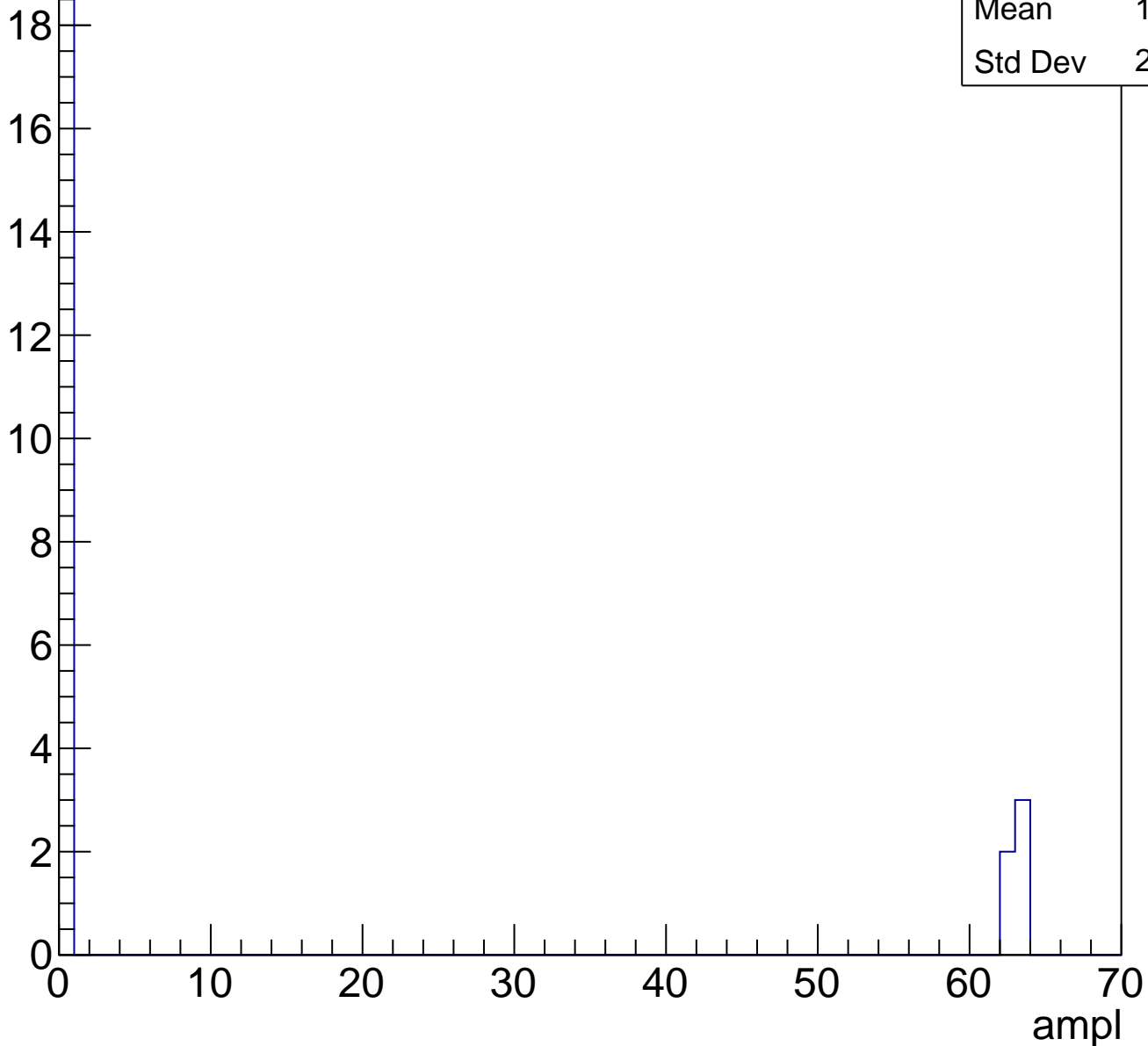


# B1L103S, U4-ch86, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 24    |
| Mean    | 13.04 |
| Std Dev | 25.42 |

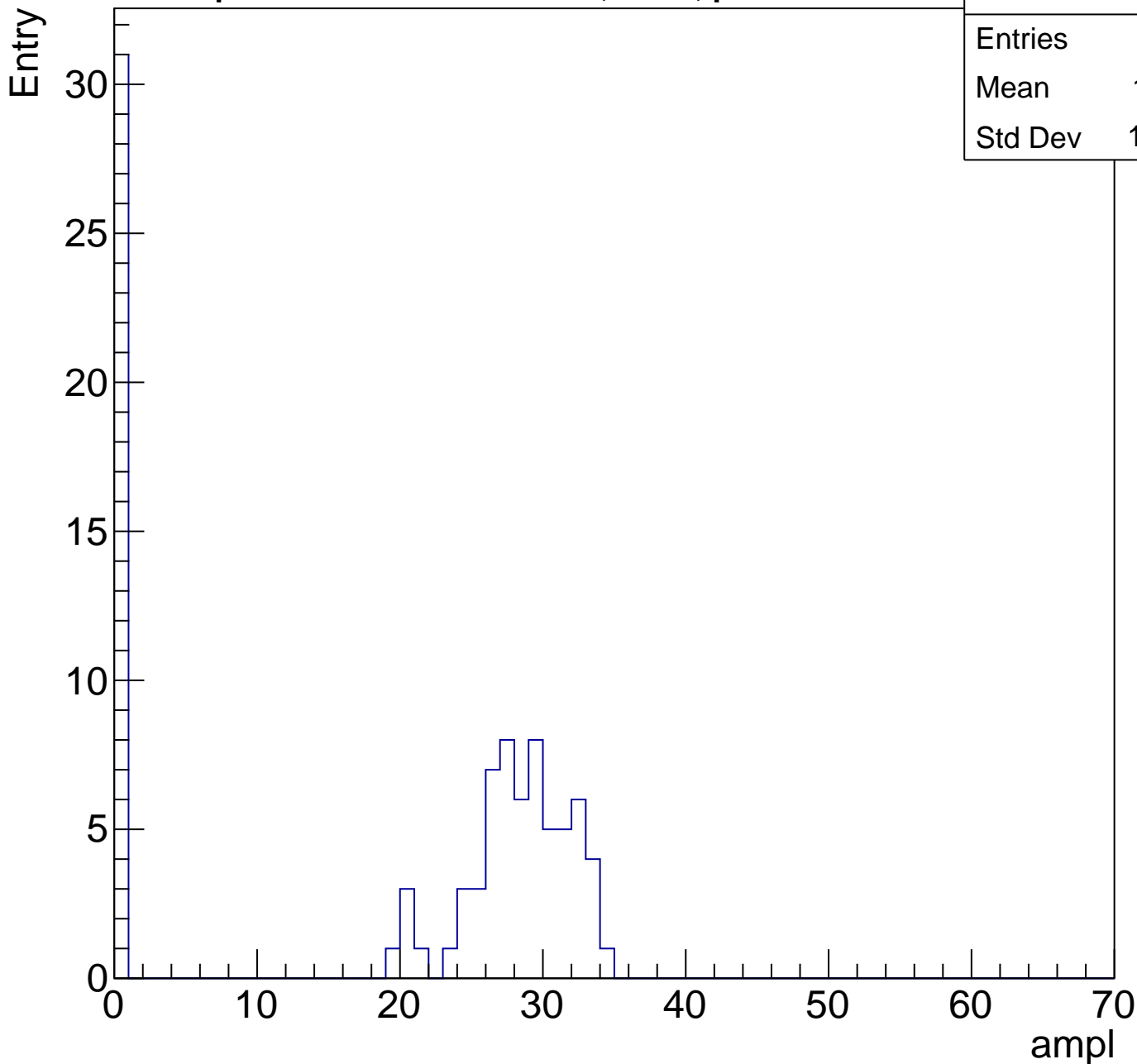
Entry



# B1L103S, U4-ch87, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 93    |
| Mean    | 18.61 |
| Std Dev | 13.47 |

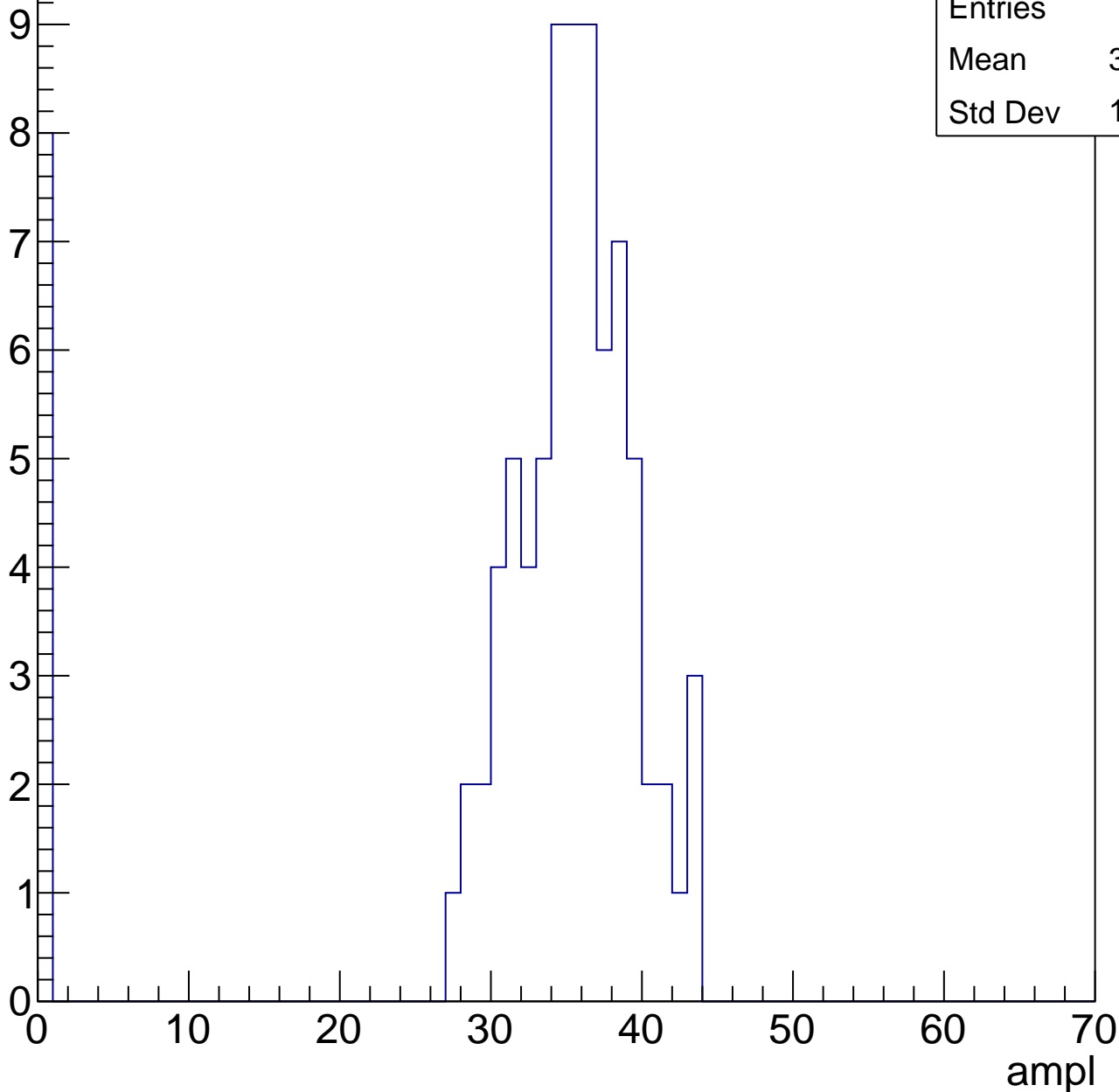


# B1L103S, U4-ch87, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 84    |
| Mean    | 31.79 |
| Std Dev | 10.88 |

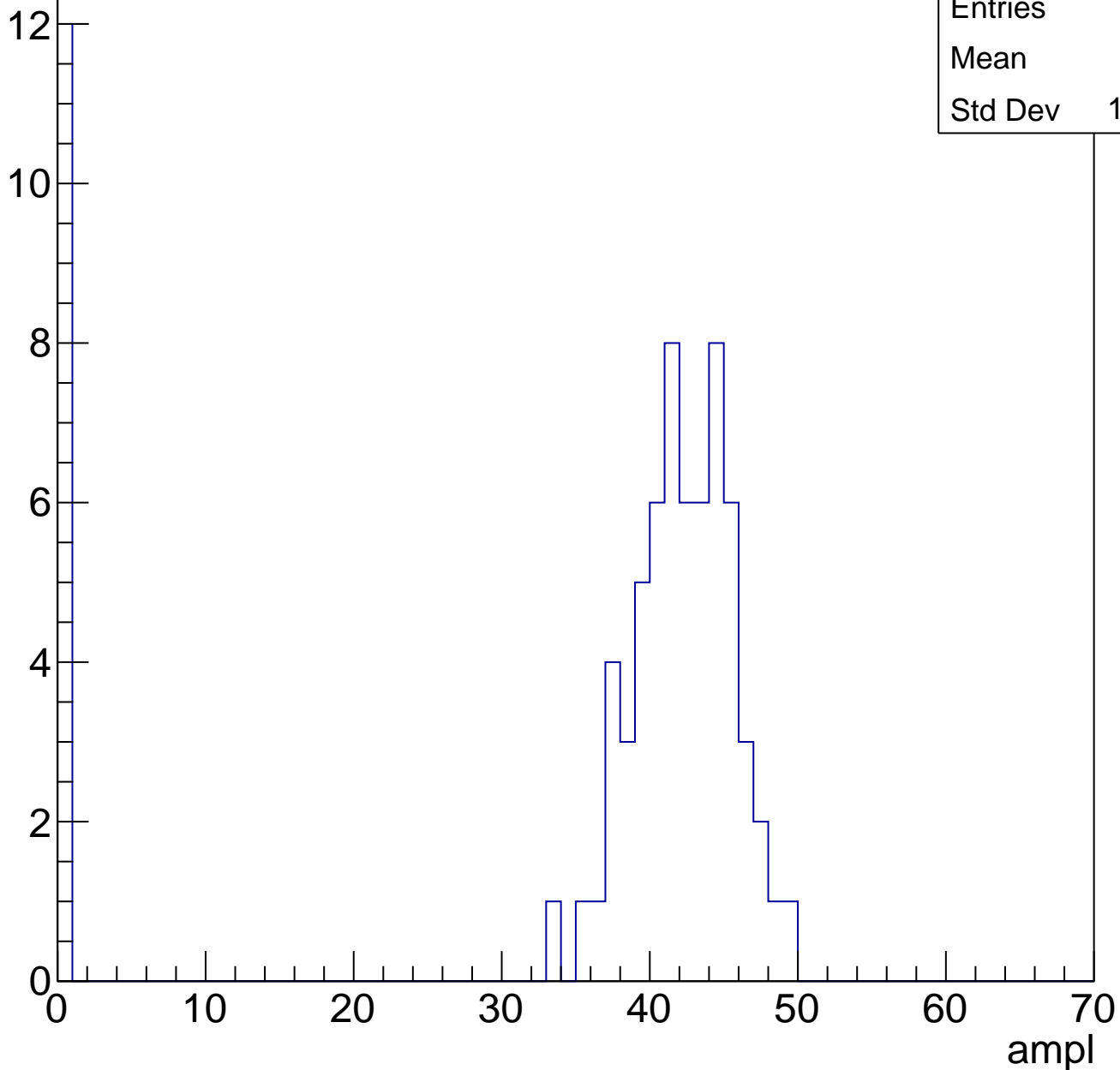


# B1L103S, U4-ch87, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

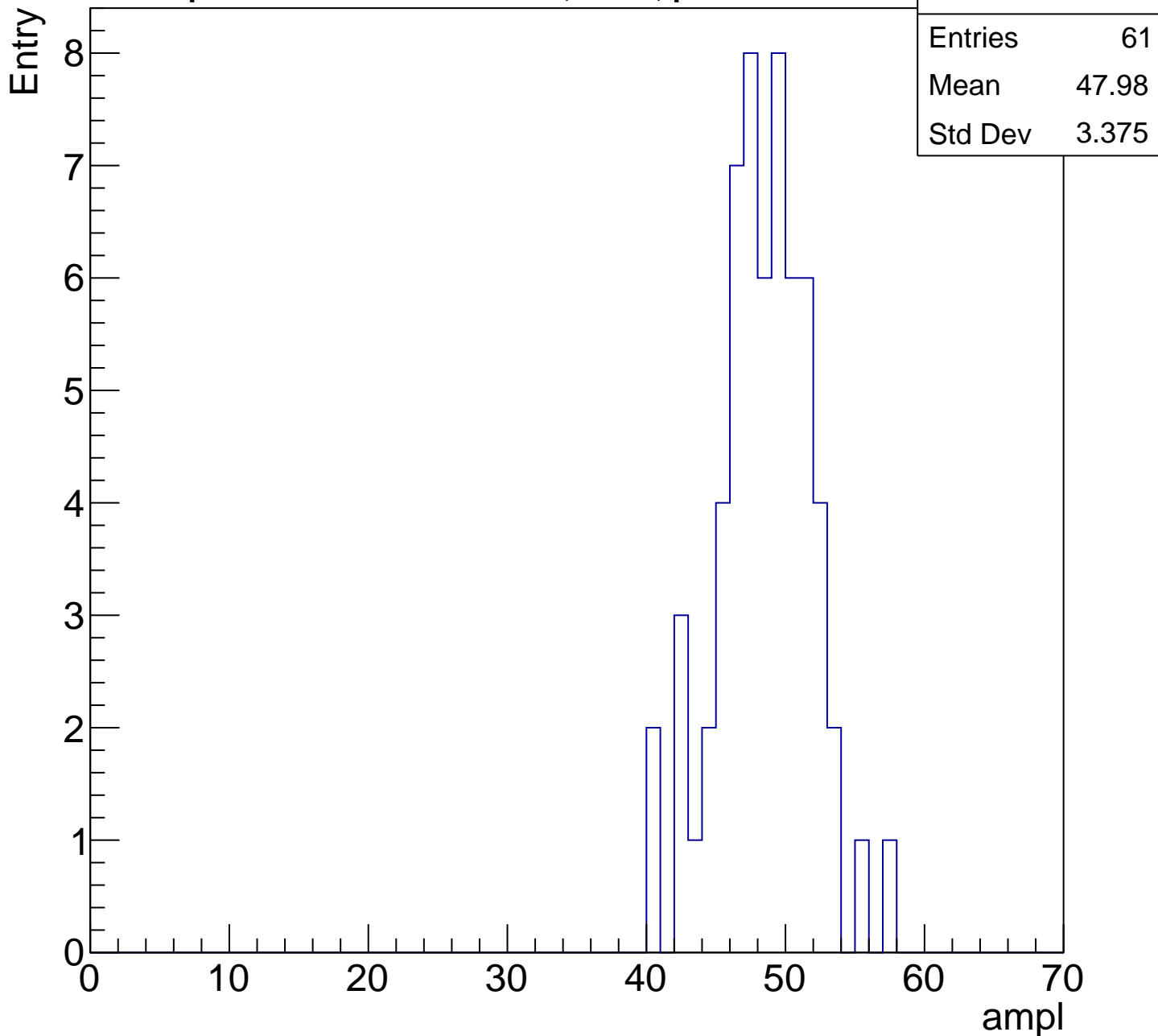
|         |       |
|---------|-------|
| Entries | 74    |
| Mean    | 35    |
| Std Dev | 15.69 |

Entry



# B1L103S, U4-ch87, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

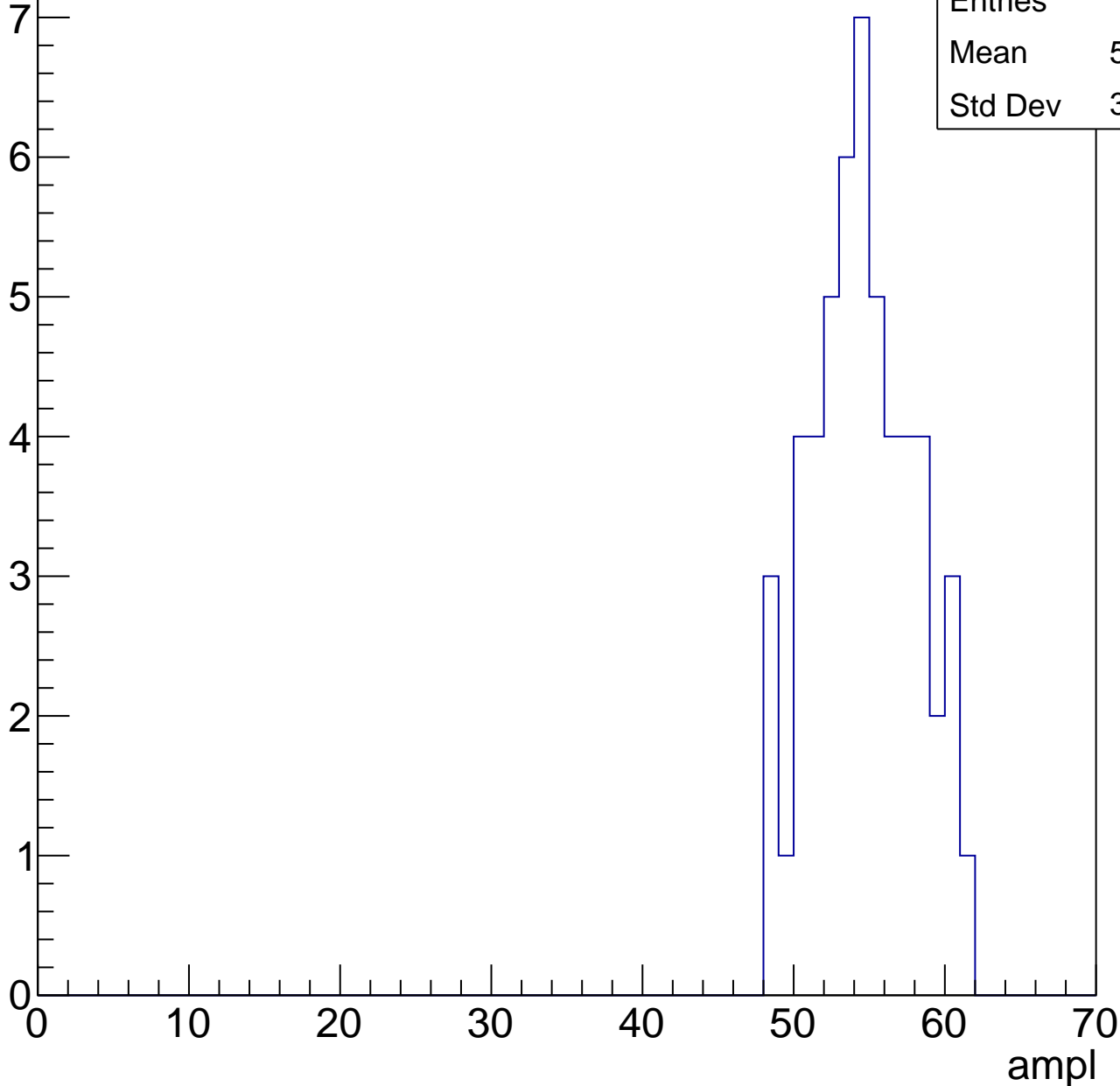


# B1L103S, U4-ch87, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 53    |
| Mean    | 54.17 |
| Std Dev | 3.324 |



# B1L103S, U4-ch87, adc5

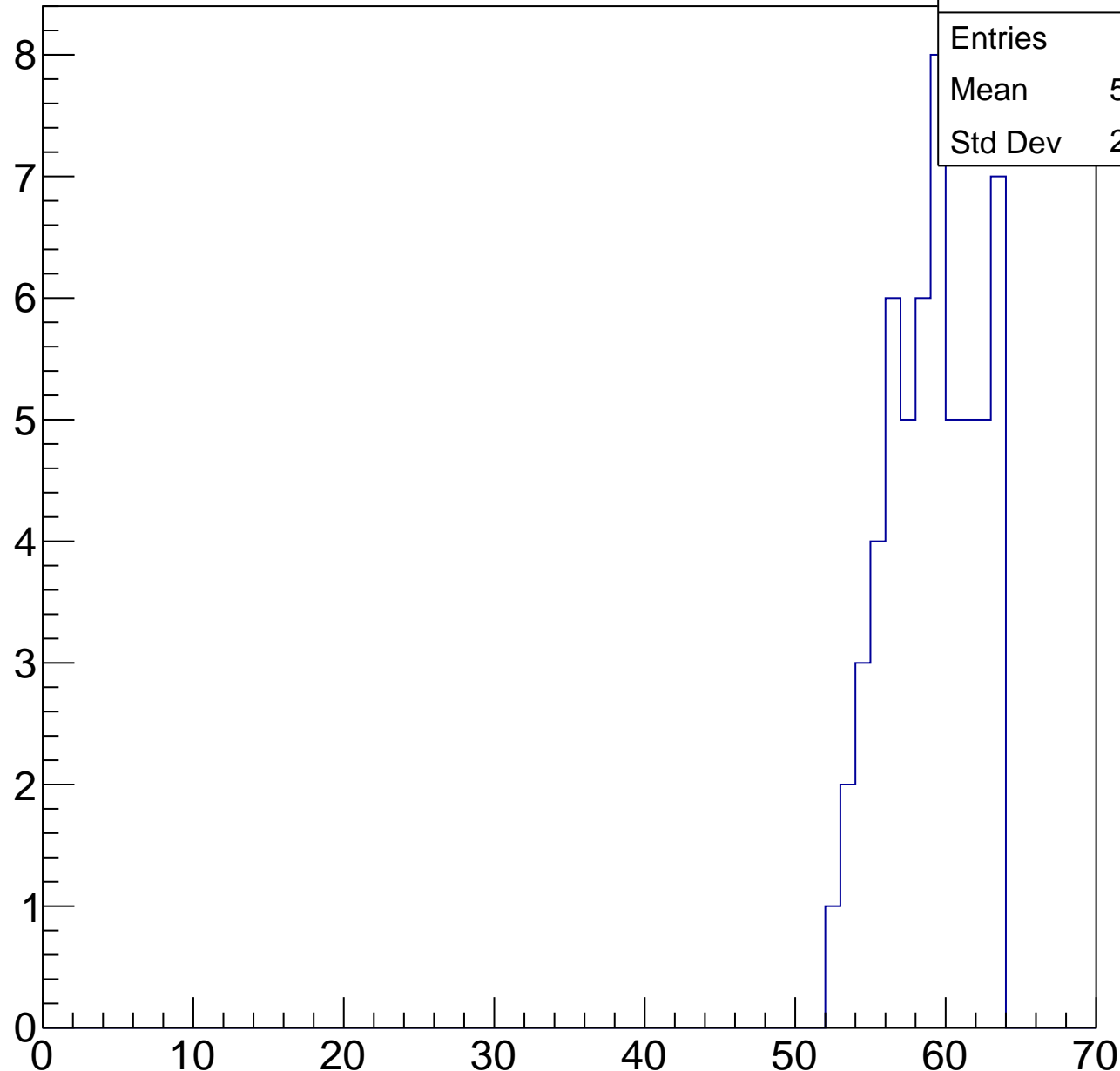
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

|         |       |
|---------|-------|
| Entries | 57    |
| Mean    | 58.54 |
| Std Dev | 2.992 |

ampl

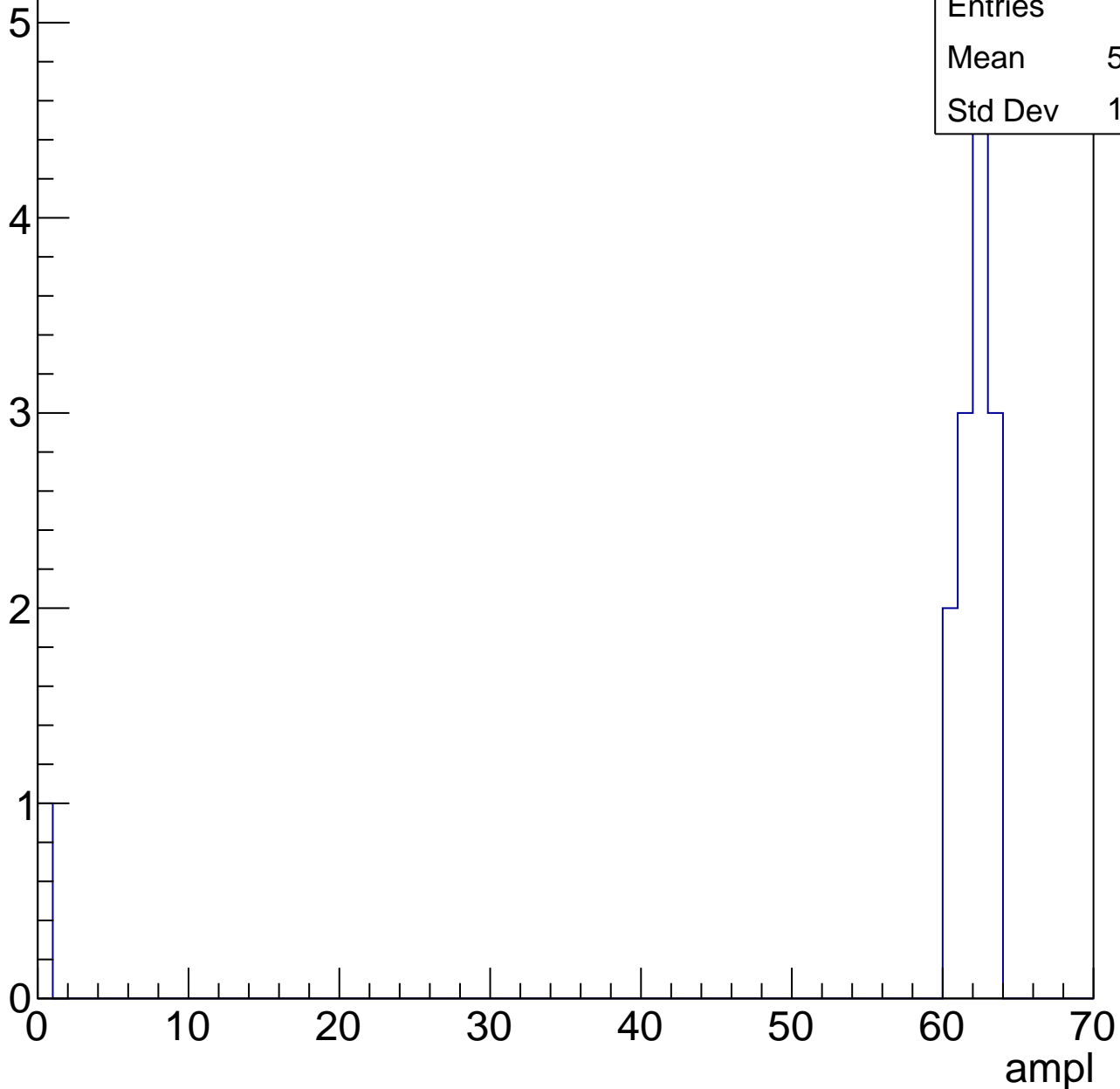


# B1L103S, U4-ch87, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 14    |
| Mean    | 57.29 |
| Std Dev | 15.92 |





# B1L103S, U4-ch87, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 20    |
| Mean    | 3.05  |
| Std Dev | 13.29 |

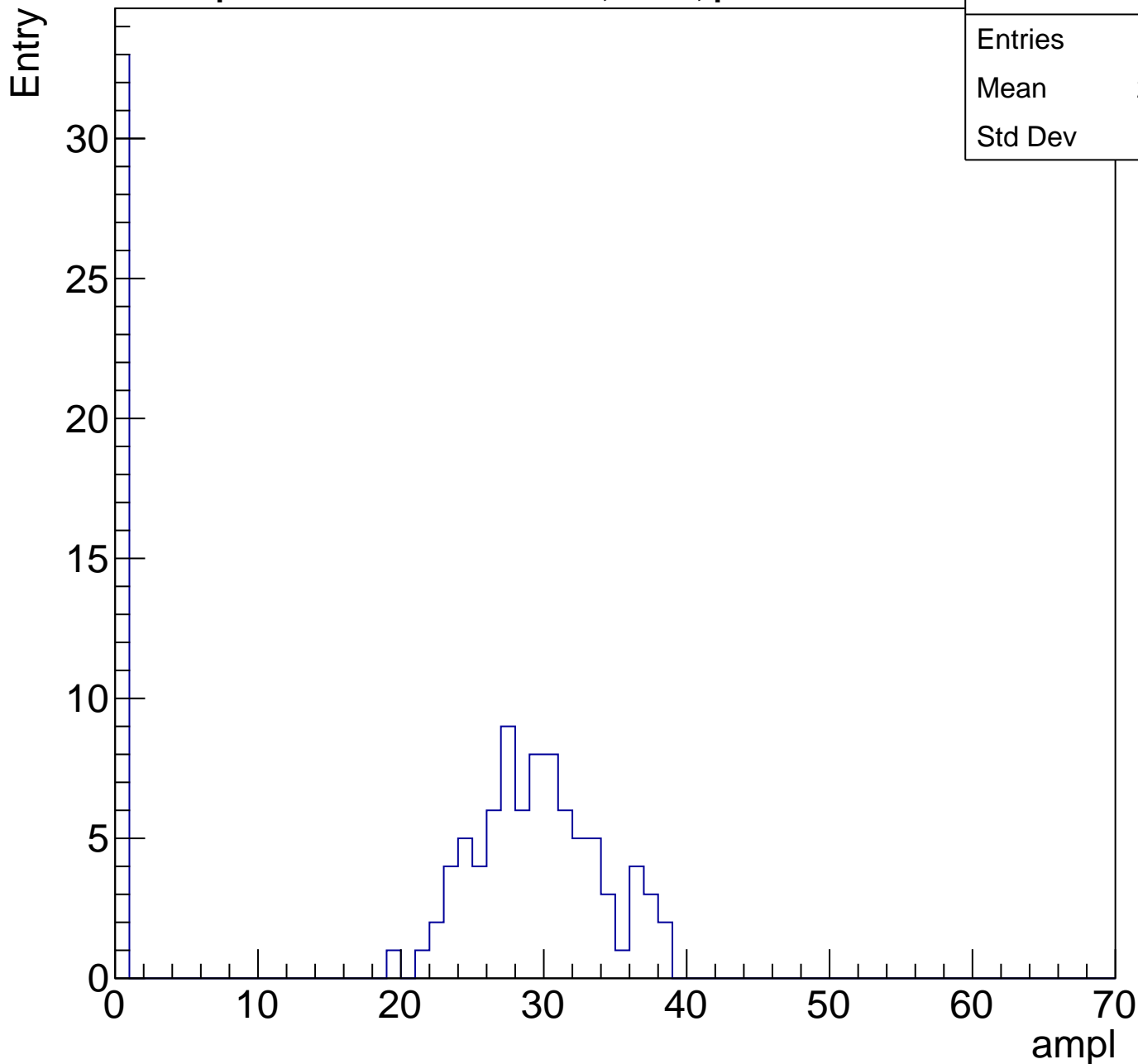
Entry



# B1L103S, U4-ch88, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 116   |
| Mean    | 20.81 |
| Std Dev | 13.61 |

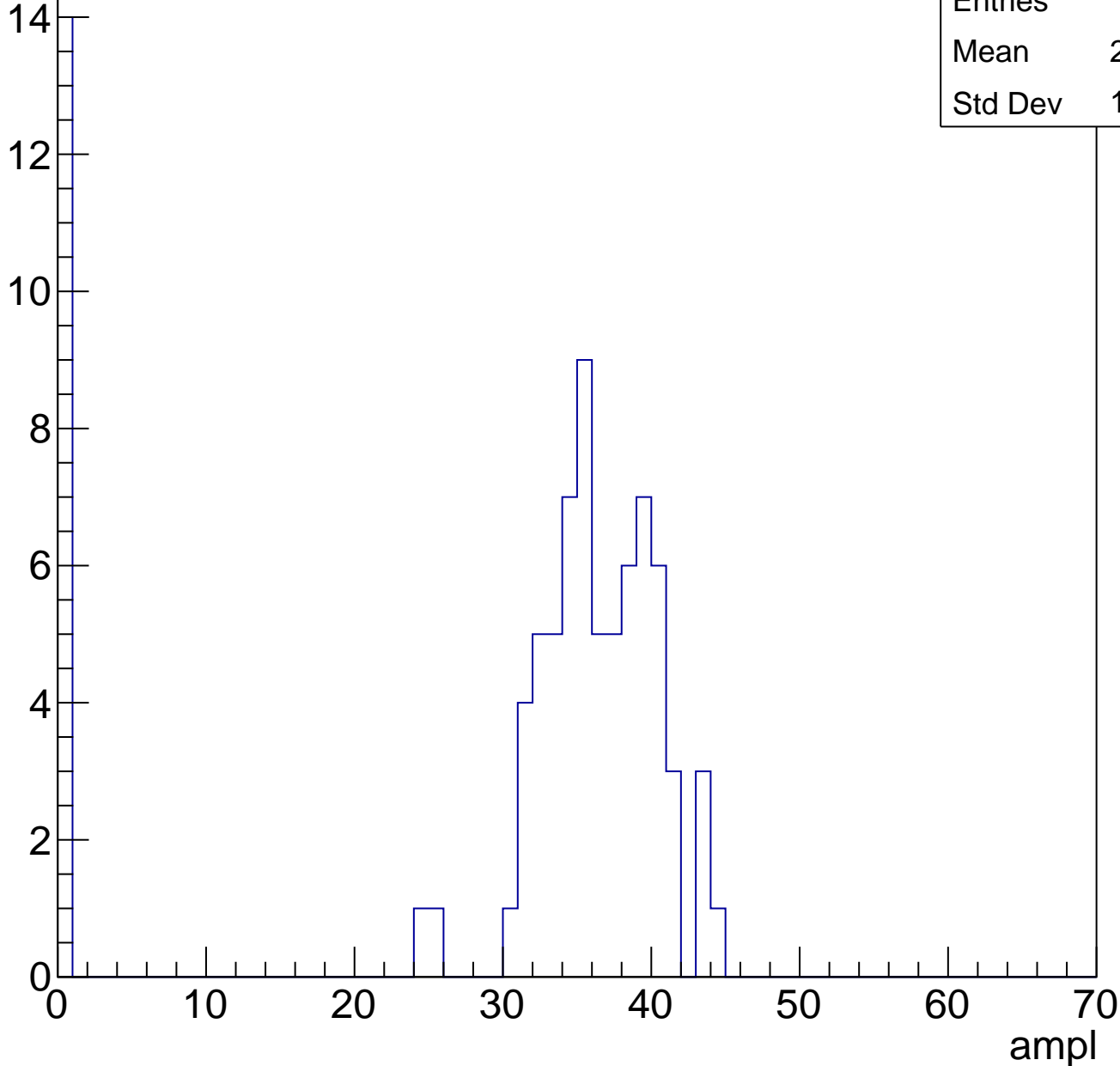


# B1L103S, U4-ch88, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 83    |
| Mean    | 29.92 |
| Std Dev | 13.93 |

Entry

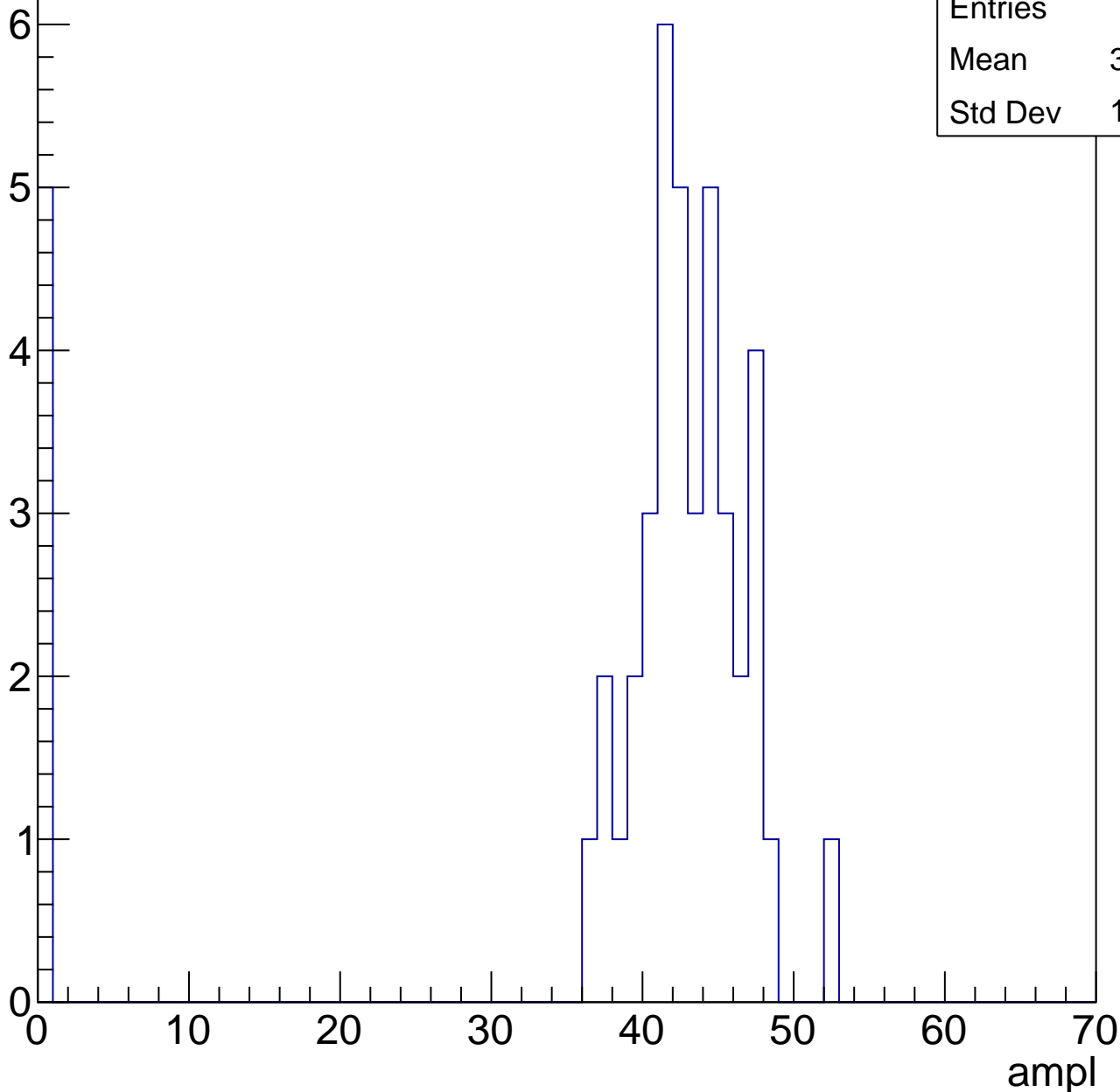


# B1L103S, U4-ch88, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

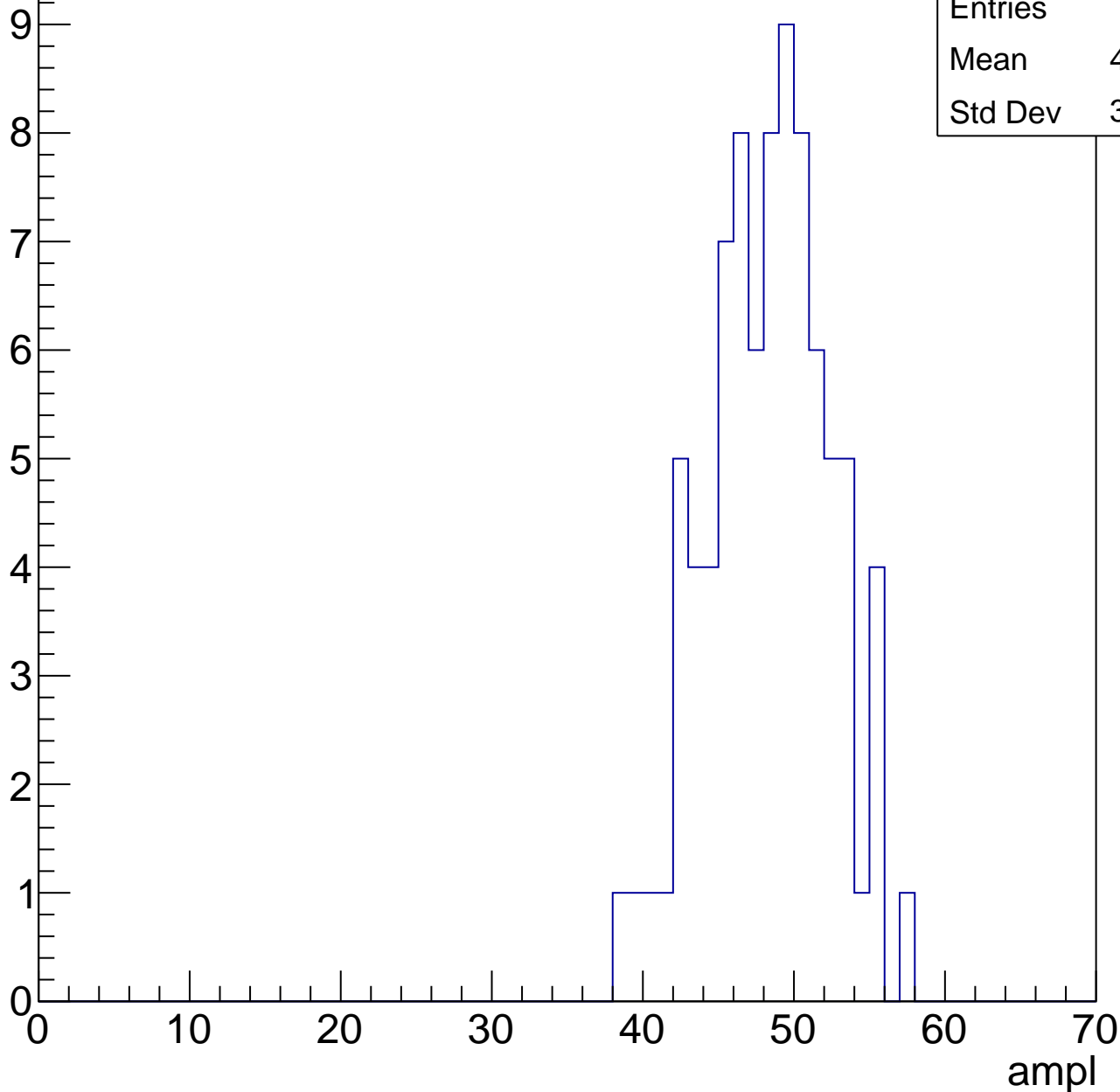
|         |       |
|---------|-------|
| Entries | 44    |
| Mean    | 37.86 |
| Std Dev | 13.92 |



# B1L103S, U4-ch88, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

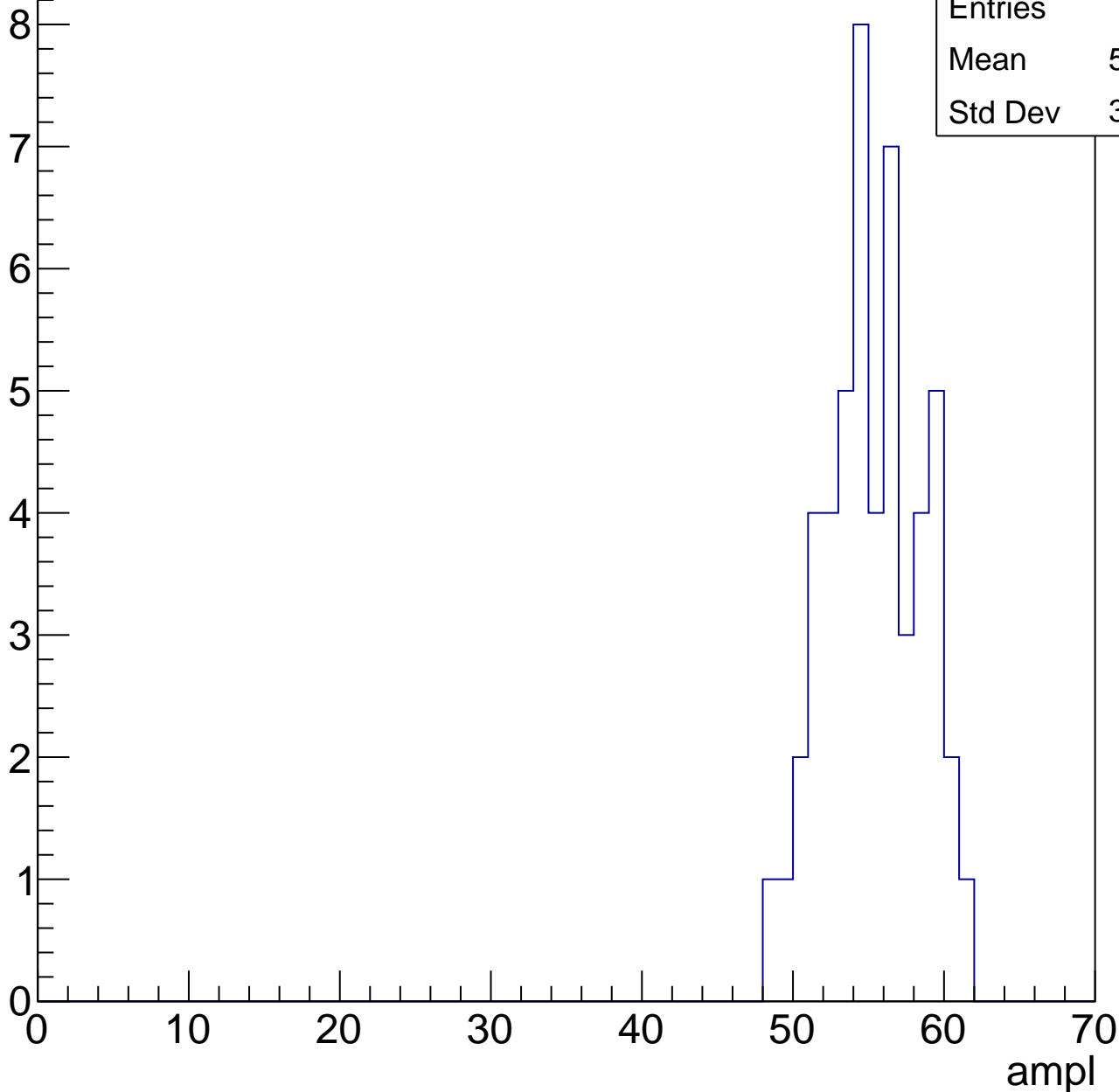


# B1L103S, U4-ch88, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 51    |
| Mean    | 54.84 |
| Std Dev | 3.077 |

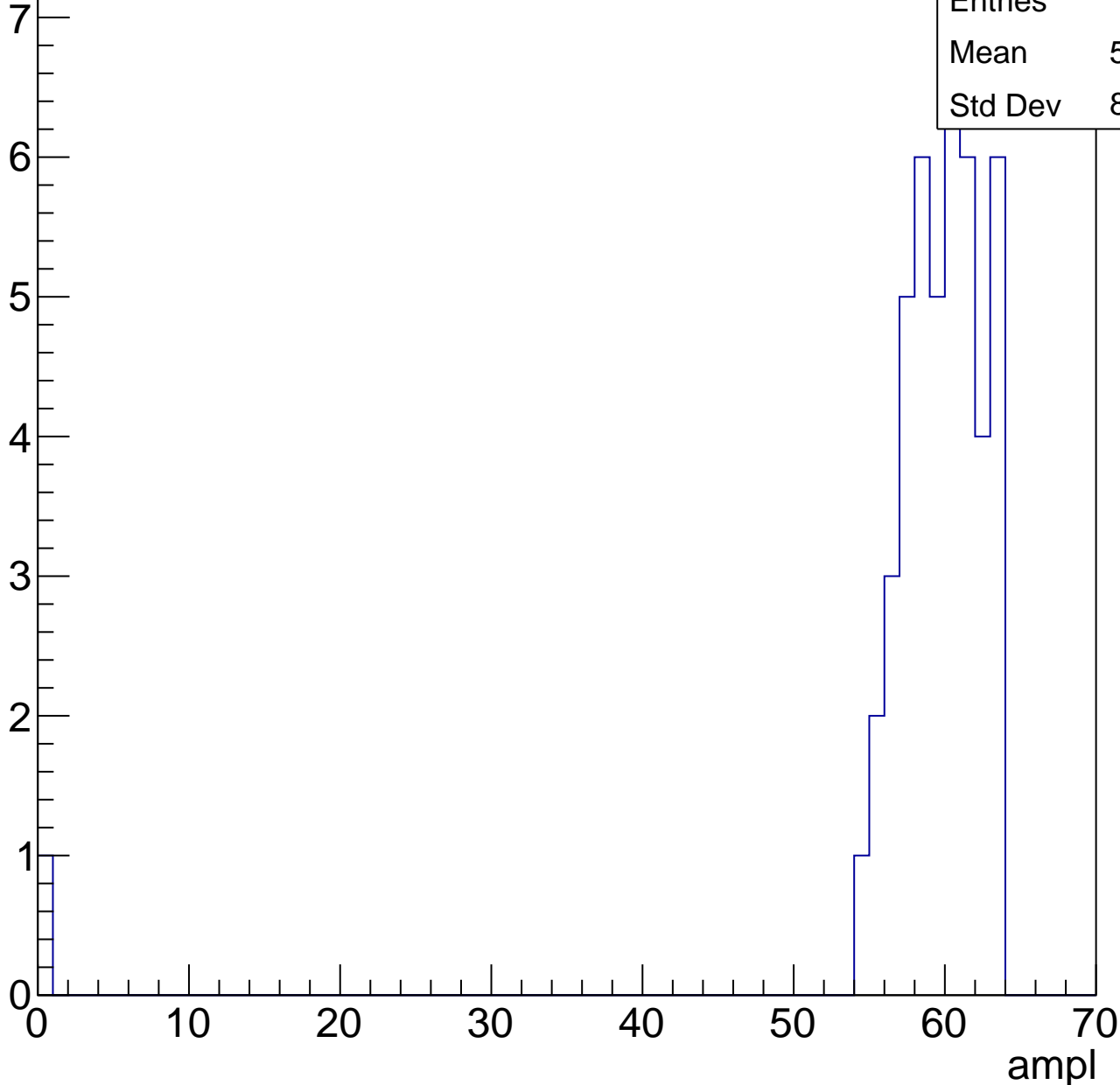


# B1L103S, U4-ch88, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 46    |
| Mean    | 58.09 |
| Std Dev | 8.987 |

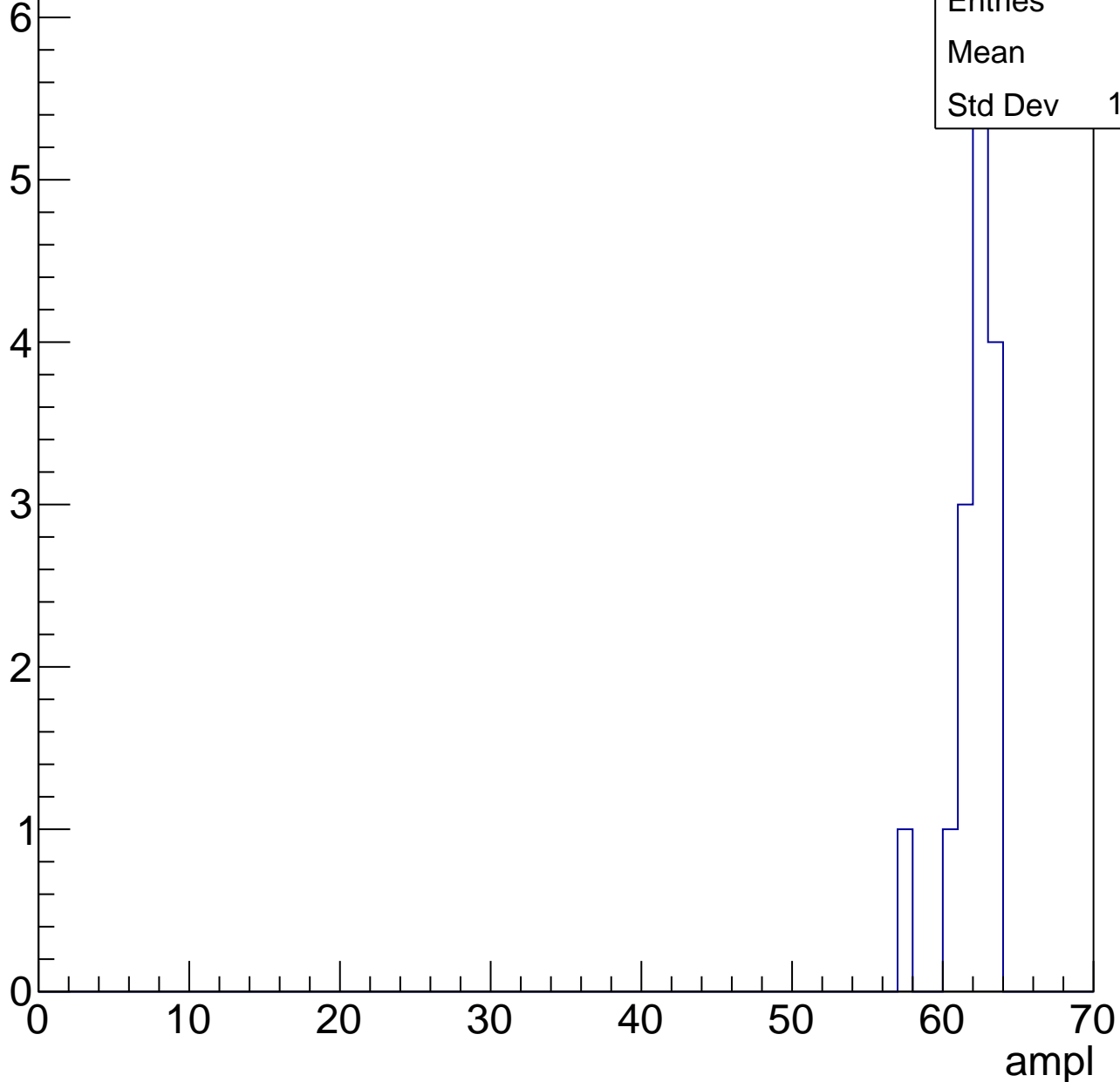


# B1L103S, U4-ch88, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 15    |
| Mean    | 61.6  |
| Std Dev | 1.497 |





# B1L103S, U4-ch88, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

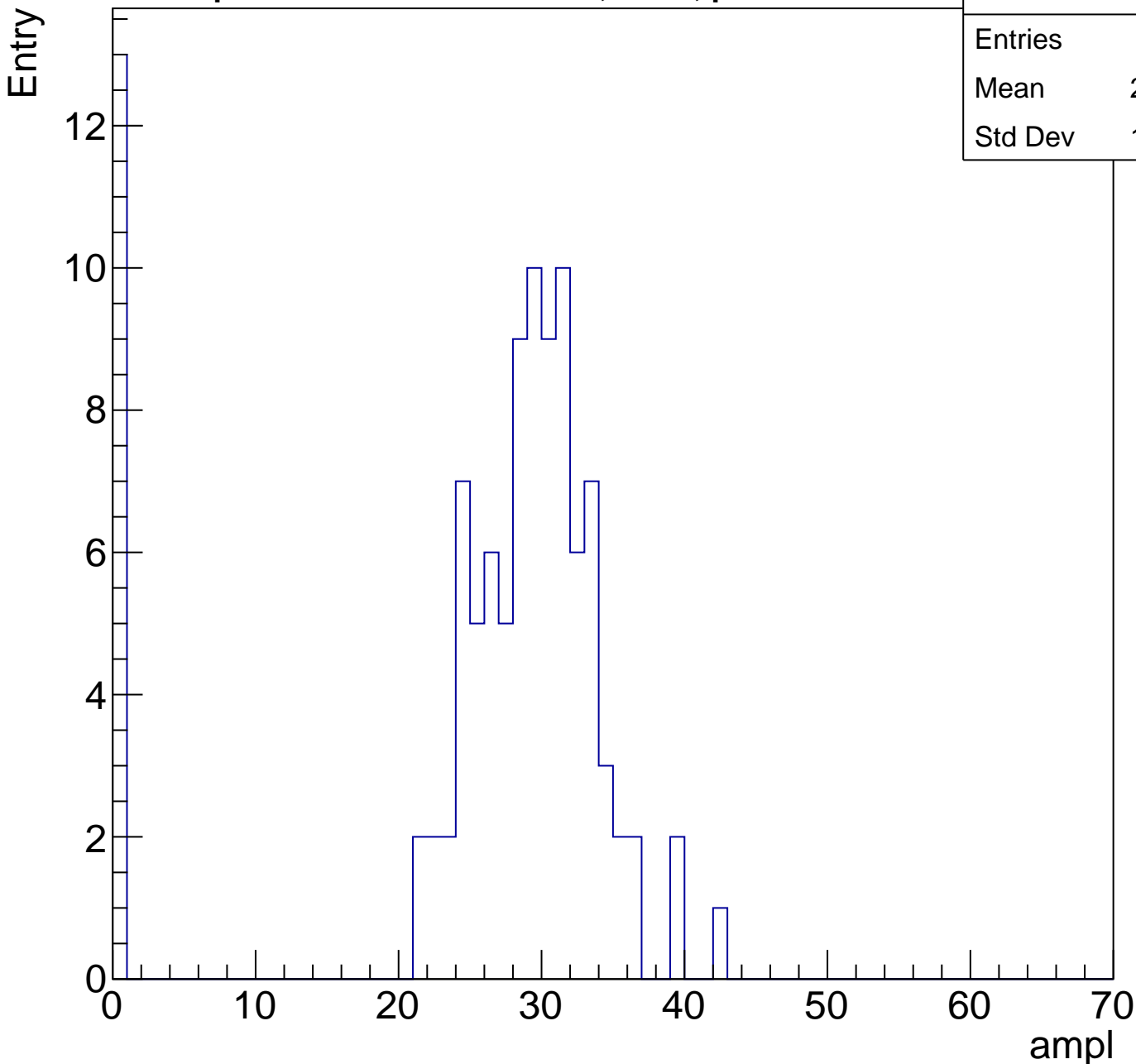
|         |    |
|---------|----|
| Entries | 19 |
| Mean    | 0  |
| Std Dev | 0  |

ampl

# B1L103S, U4-ch89, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 103   |
| Mean    | 25.49 |
| Std Dev | 10.39 |

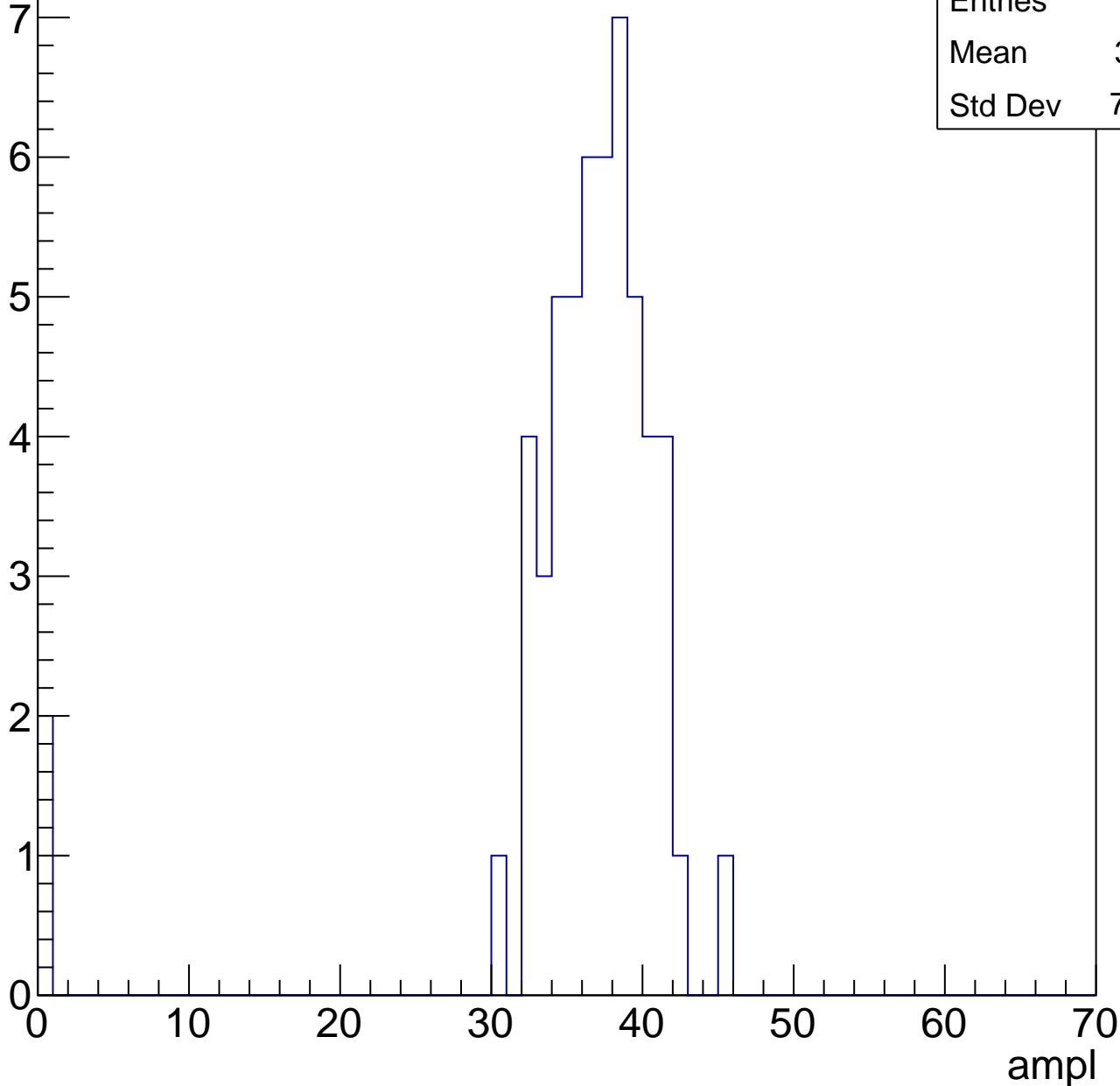


# B1L103S, U4-ch89, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 54    |
| Mean    | 35.41 |
| Std Dev | 7.558 |

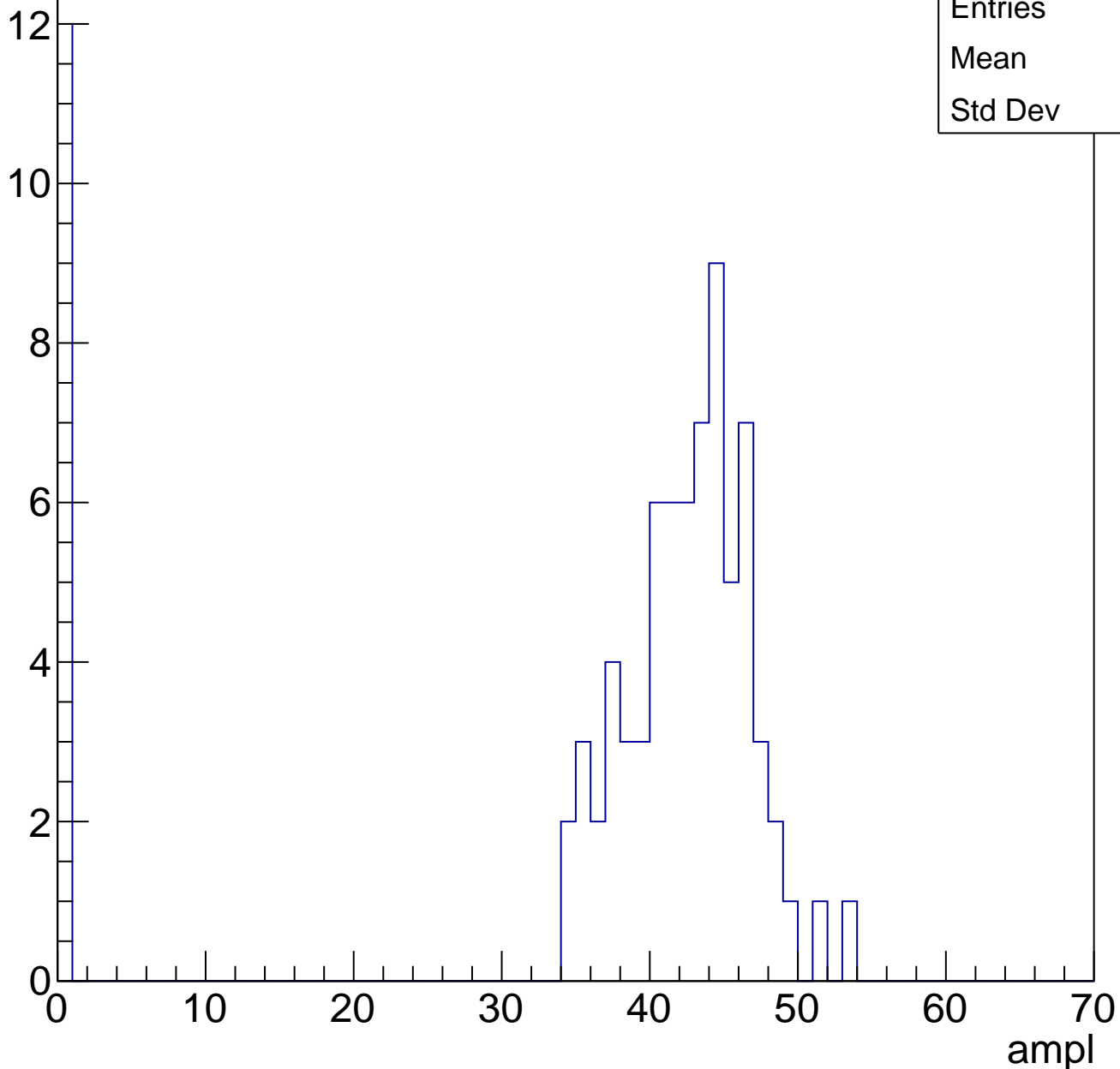


# B1L103S, U4-ch89, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |      |
|---------|------|
| Entries | 83   |
| Mean    | 36.1 |
| Std Dev | 15.3 |

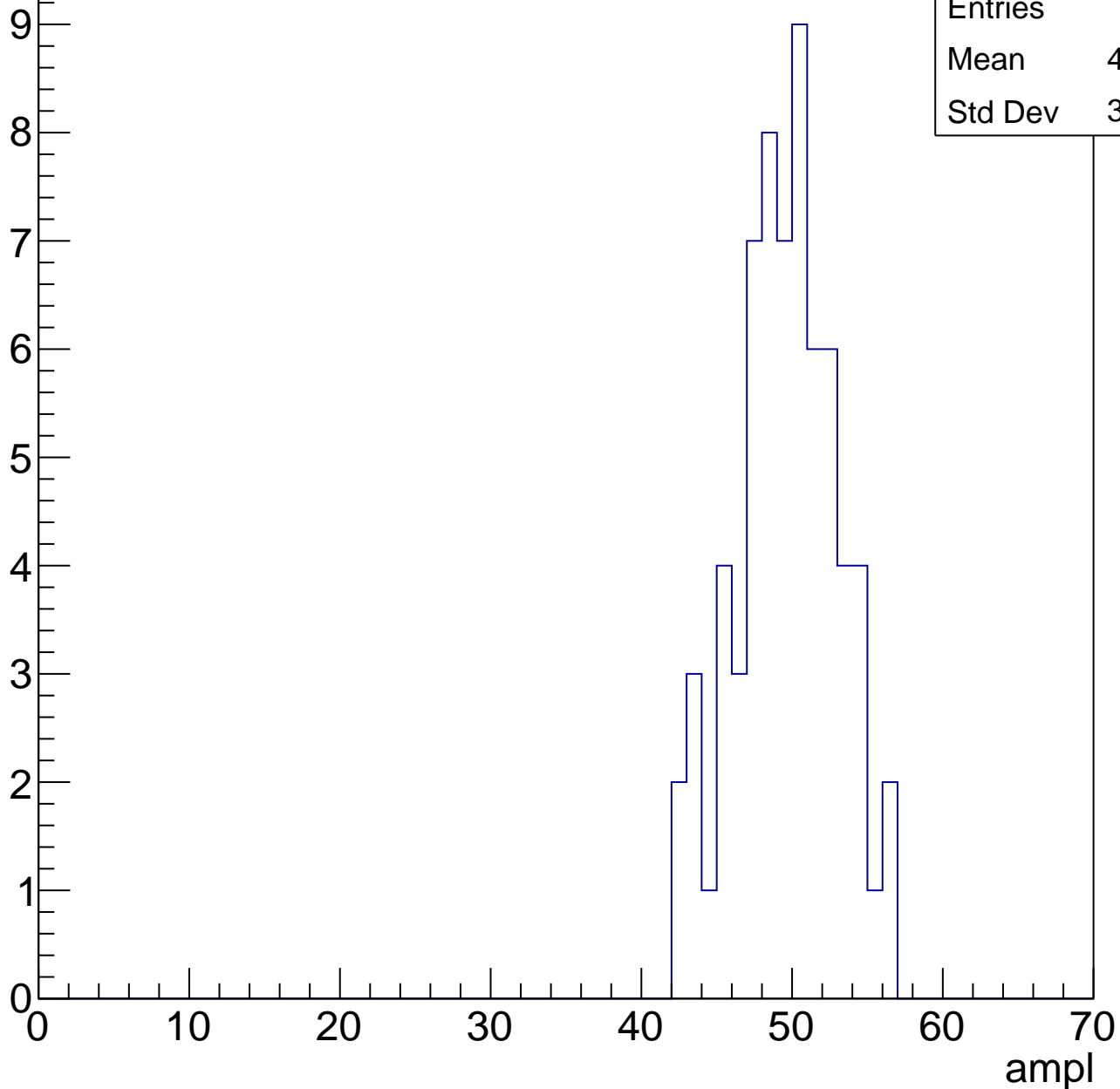
Entry



# B1L103S, U4-ch89, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

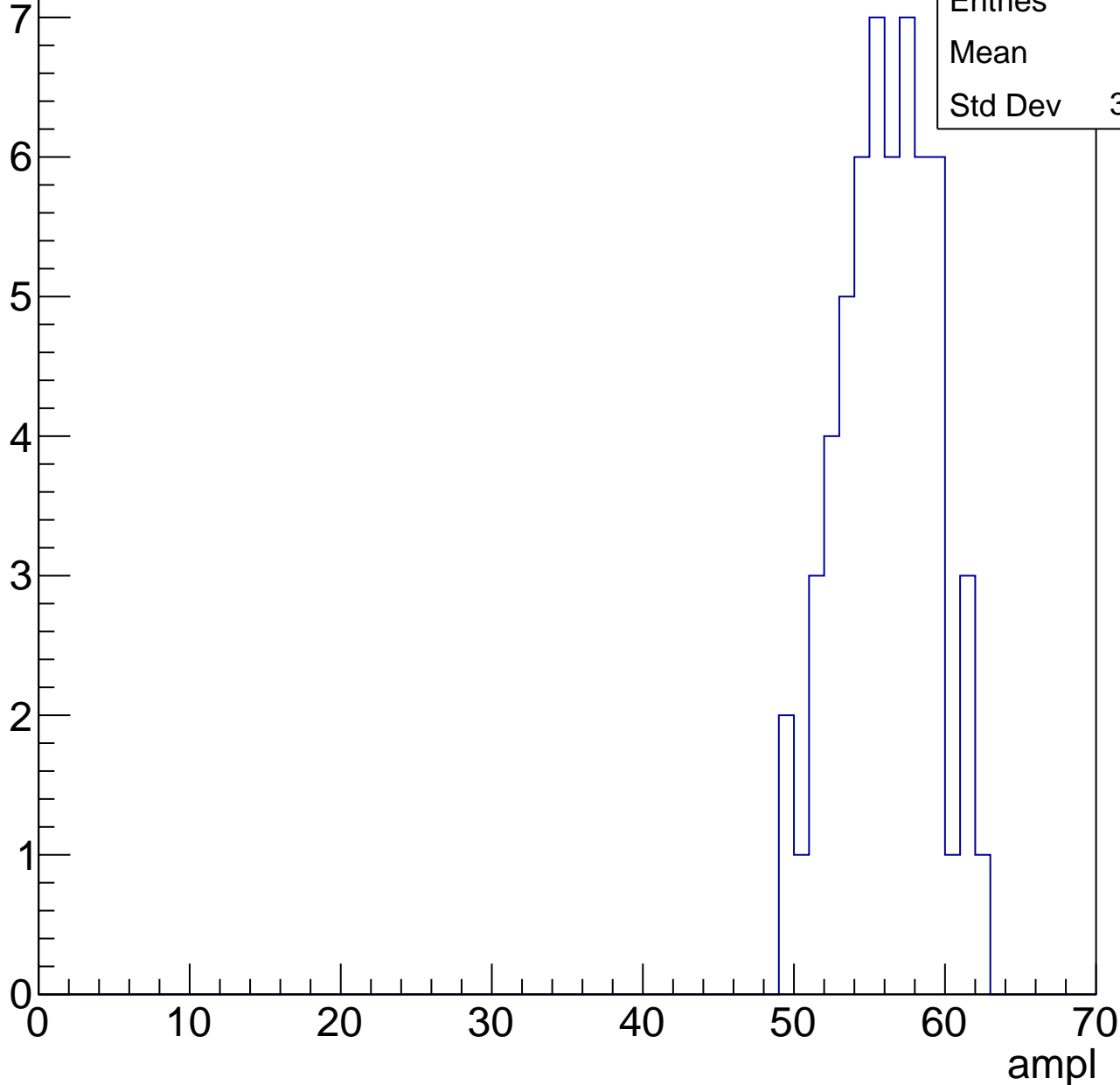
Entry



# B1L103S, U4-ch89, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

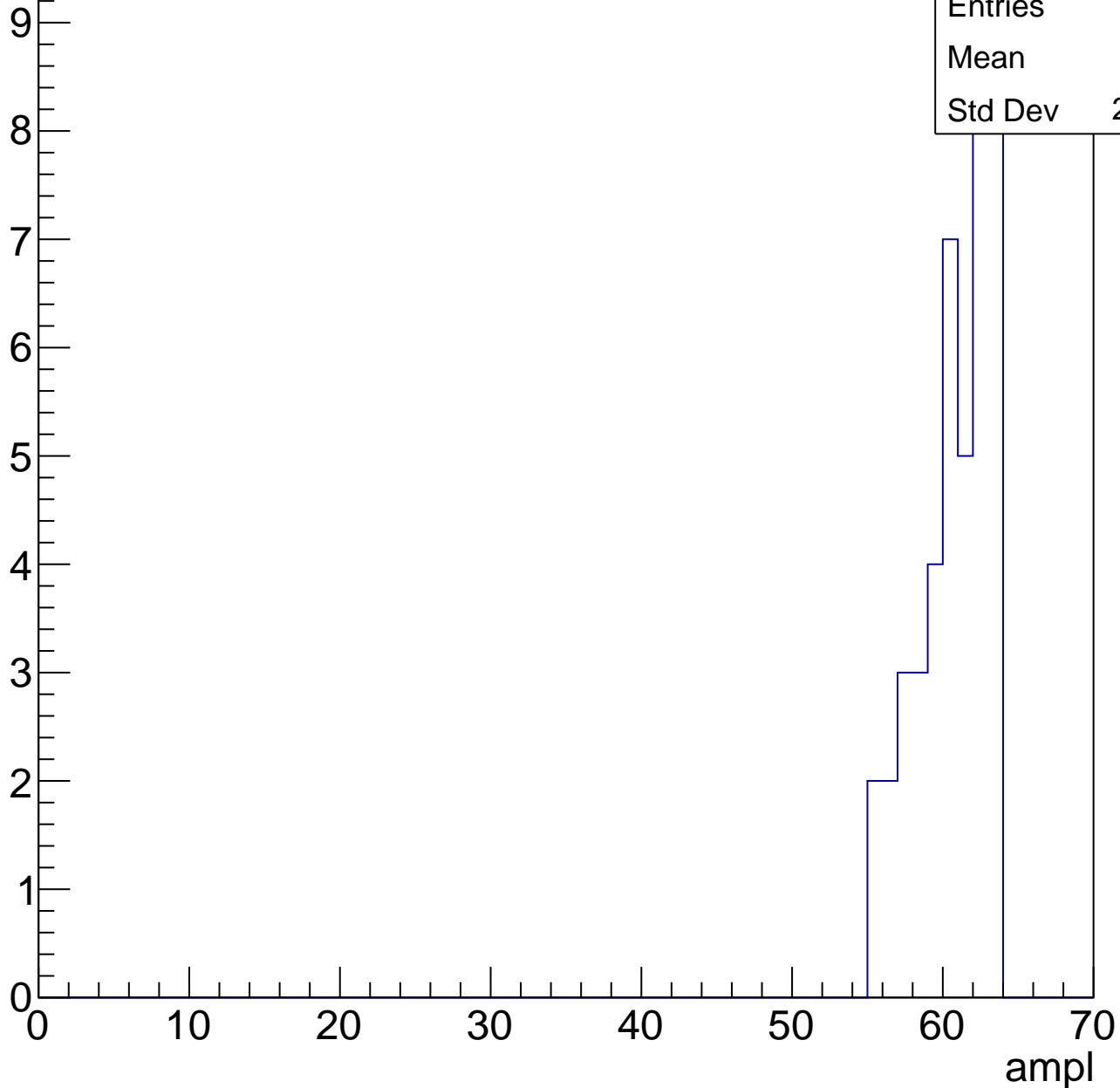
Entry



# B1L103S, U4-ch89, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



|         |       |
|---------|-------|
| Entries | 44    |
| Mean    | 60.3  |
| Std Dev | 2.351 |

# B1L103S, U4-ch89, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

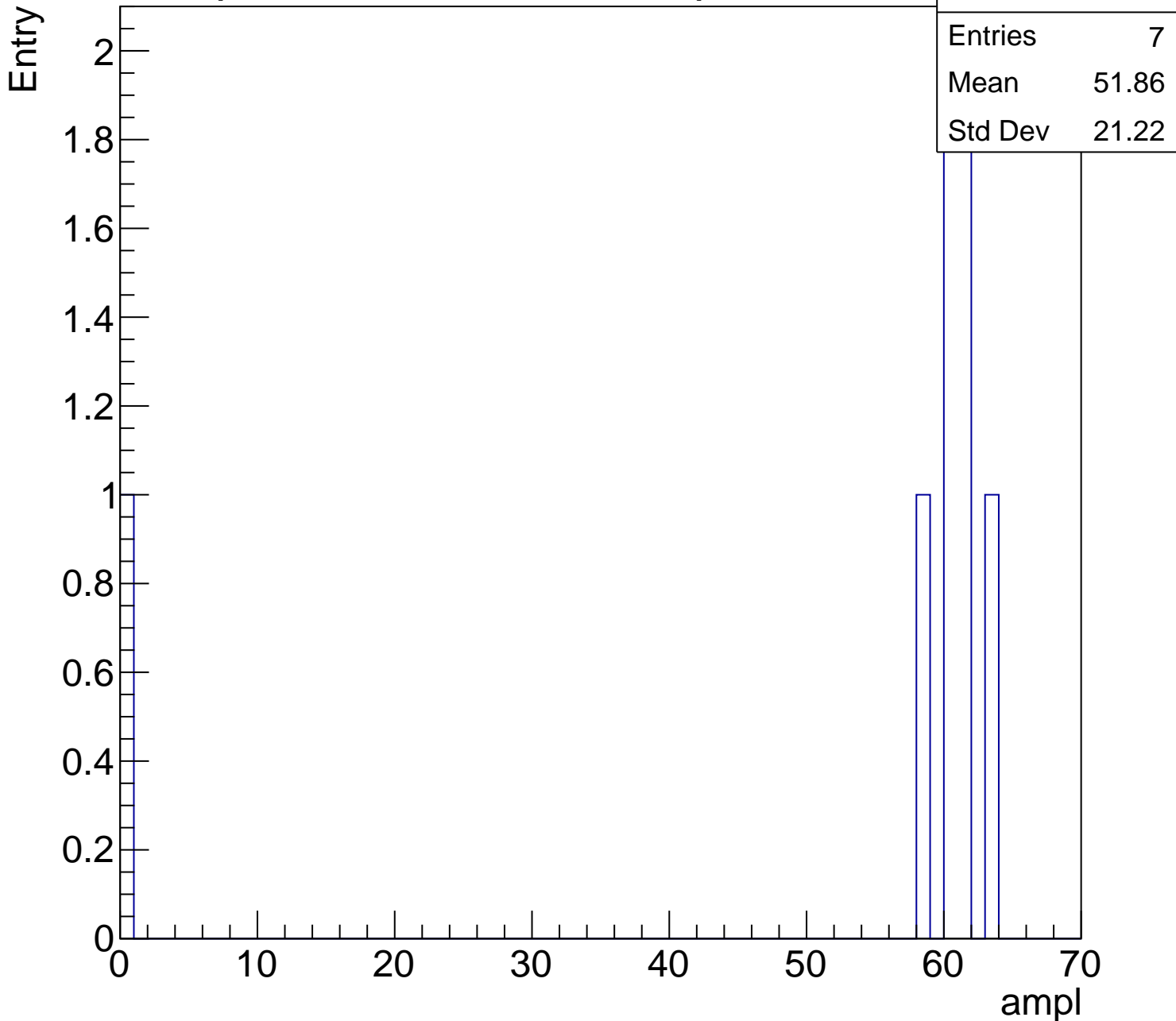
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

|         |       |
|---------|-------|
| Entries | 7     |
| Mean    | 51.86 |
| Std Dev | 21.22 |

0 10 20 30 40 50 60 70

ampl





# B1L103S, U4-ch89, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

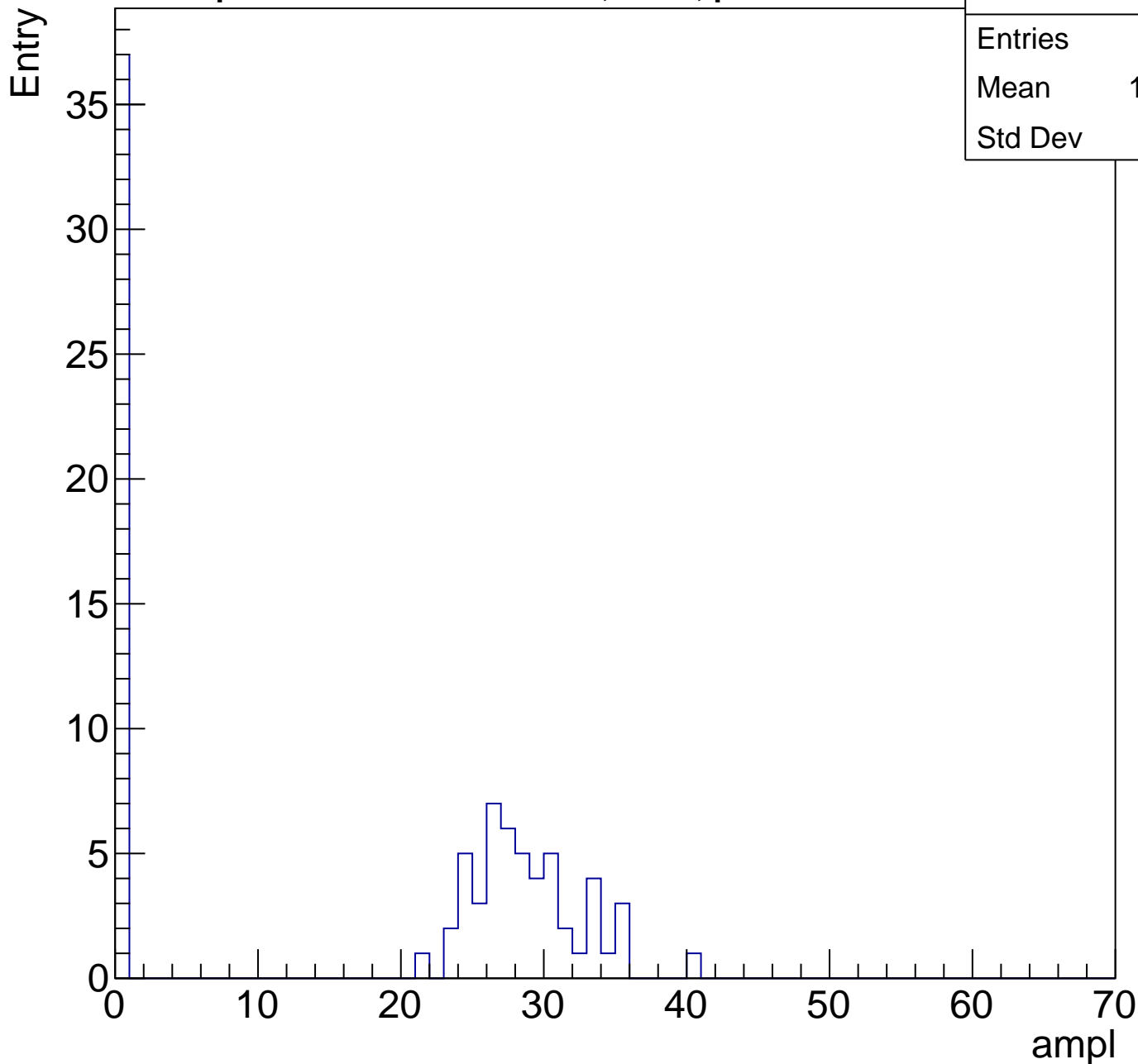
Entry



# B1L103S, U4-ch90, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 87    |
| Mean    | 16.29 |
| Std Dev | 14.3  |

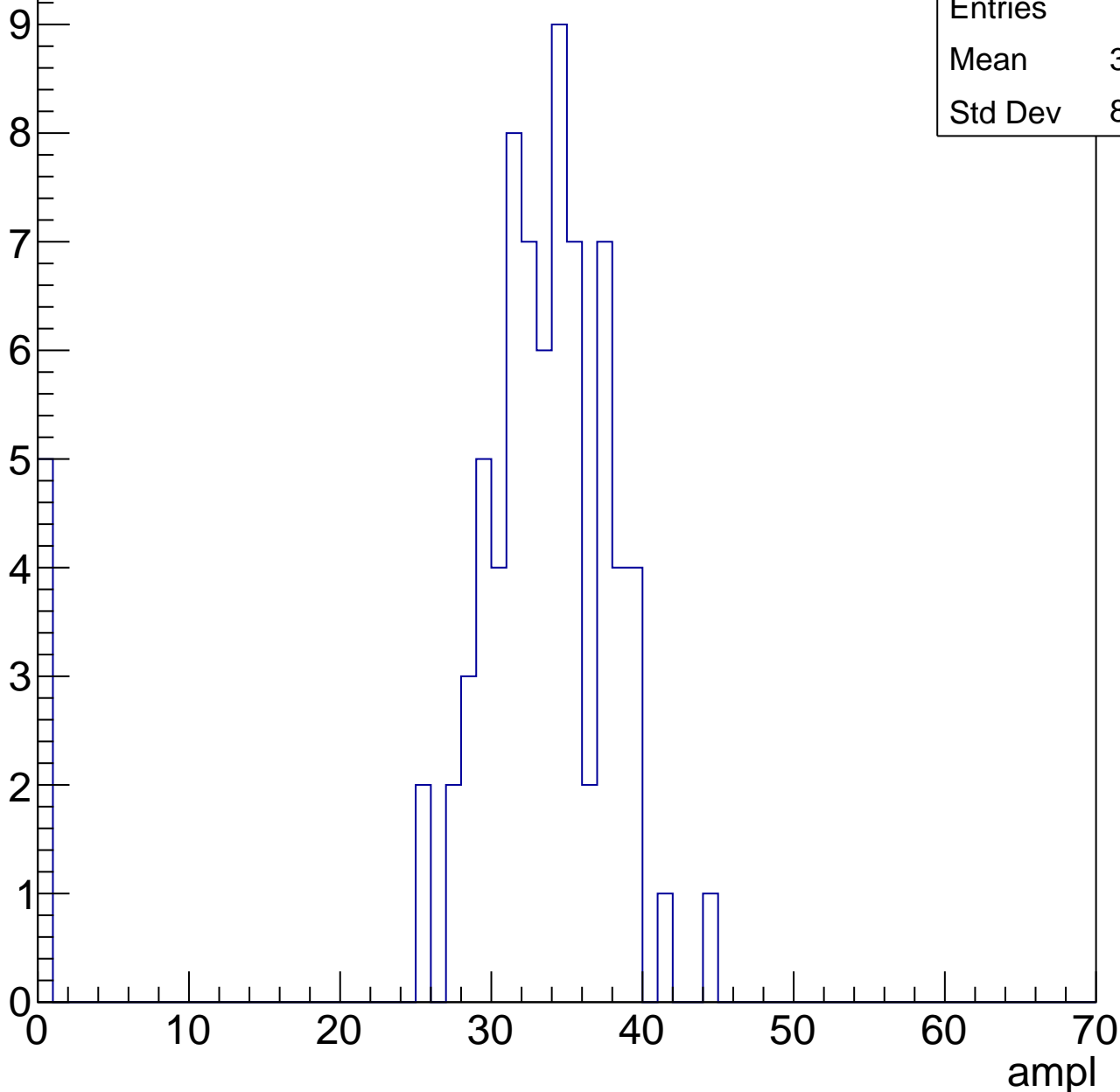


# B1L103S, U4-ch90, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 77    |
| Mean    | 31.14 |
| Std Dev | 8.977 |

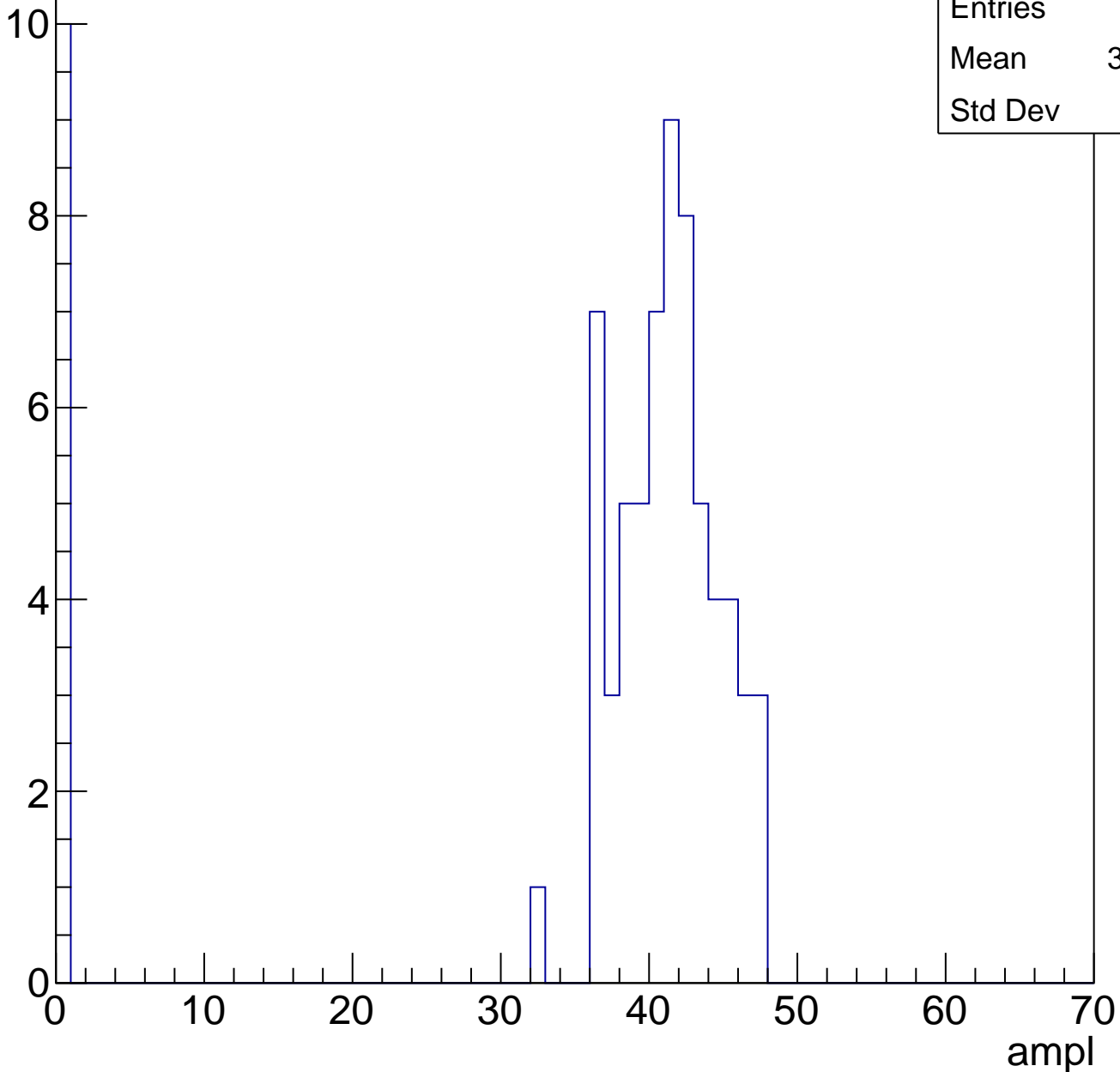


# B1L103S, U4-ch90, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 74    |
| Mean    | 35.34 |
| Std Dev | 14.3  |

Entry

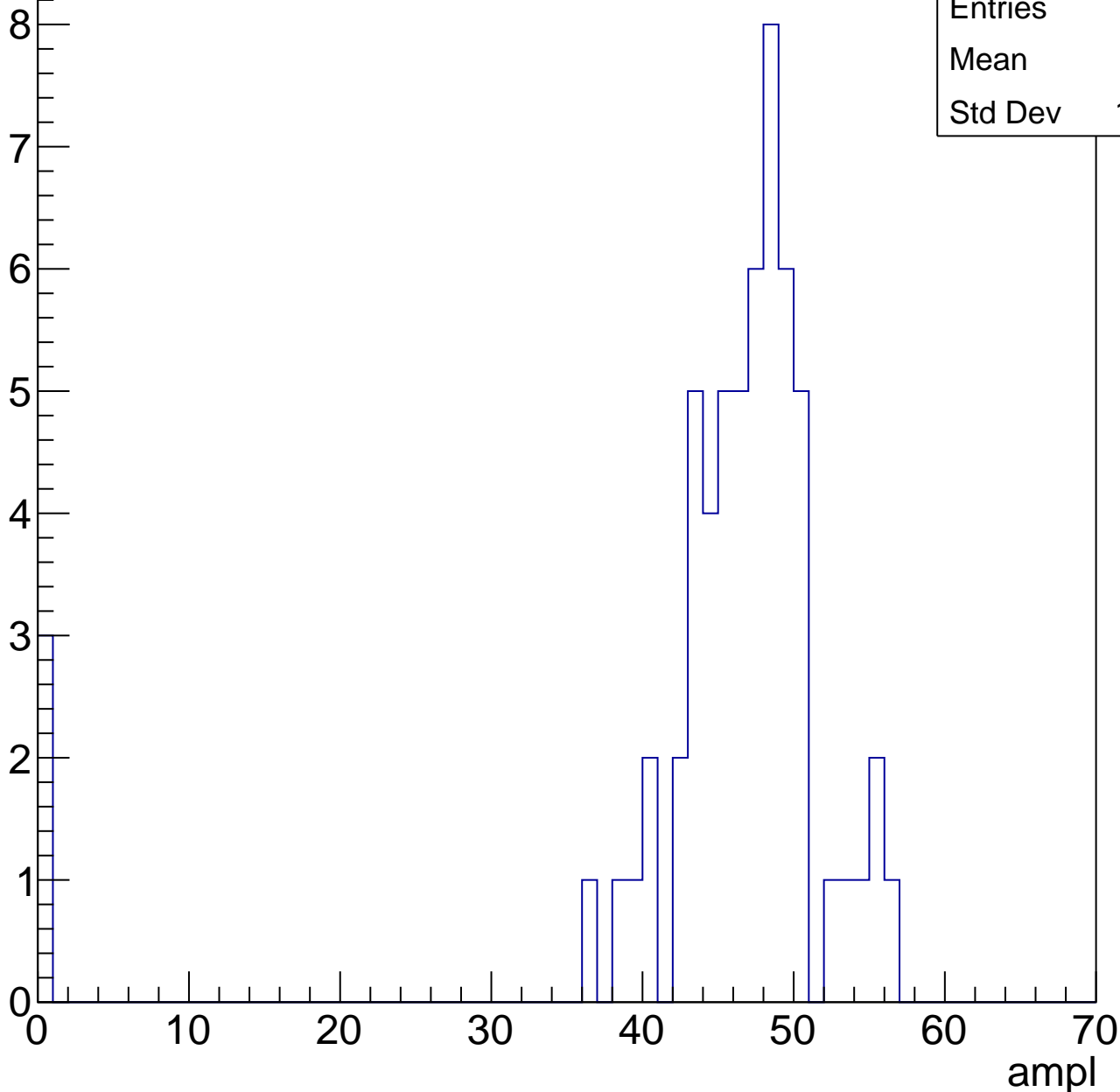


# B1L103S, U4-ch90, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 60    |
| Mean    | 44.3  |
| Std Dev | 10.91 |



# B1L103S, U4-ch90, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

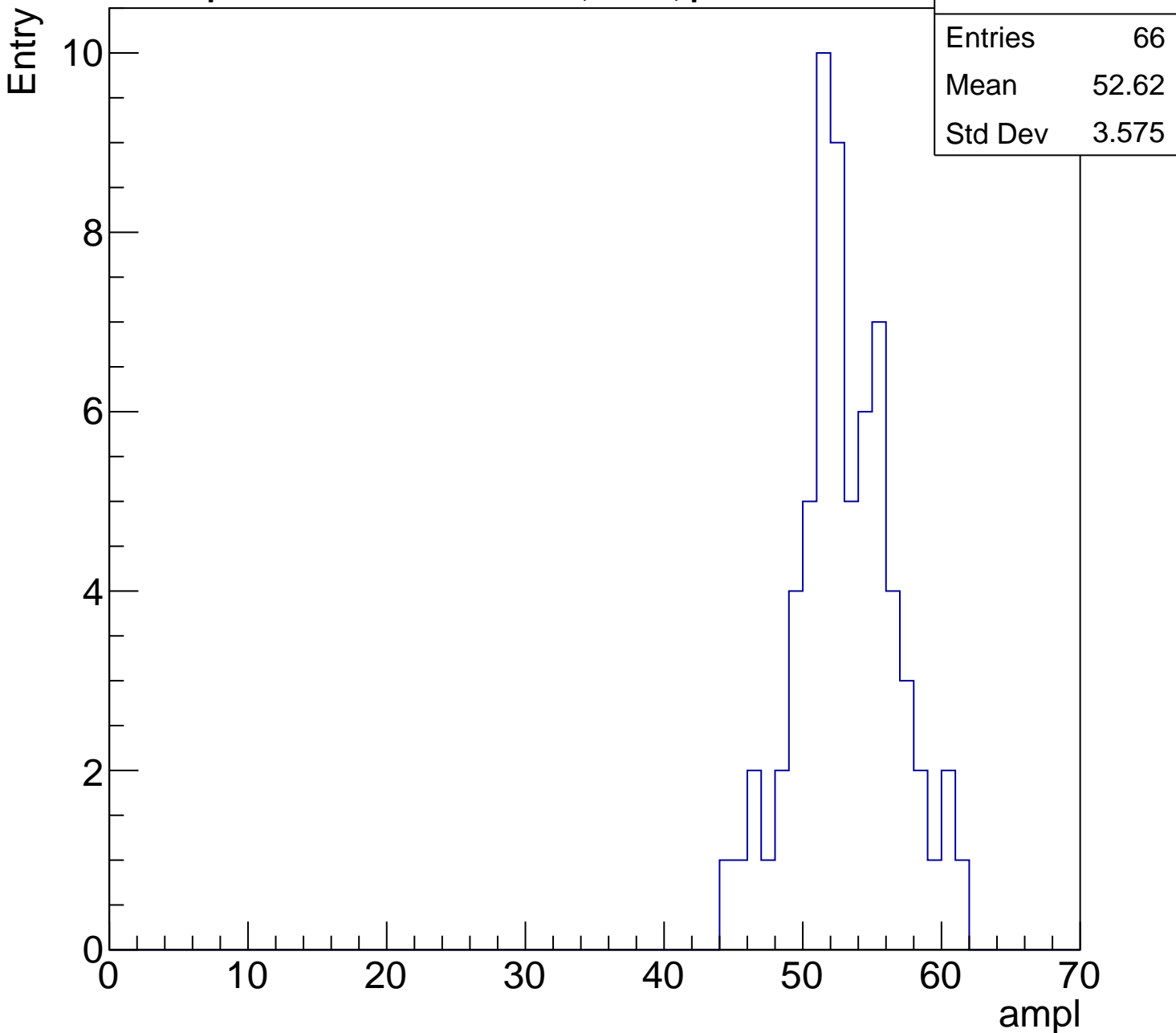
|         |       |
|---------|-------|
| Entries | 66    |
| Mean    | 52.62 |
| Std Dev | 3.575 |

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

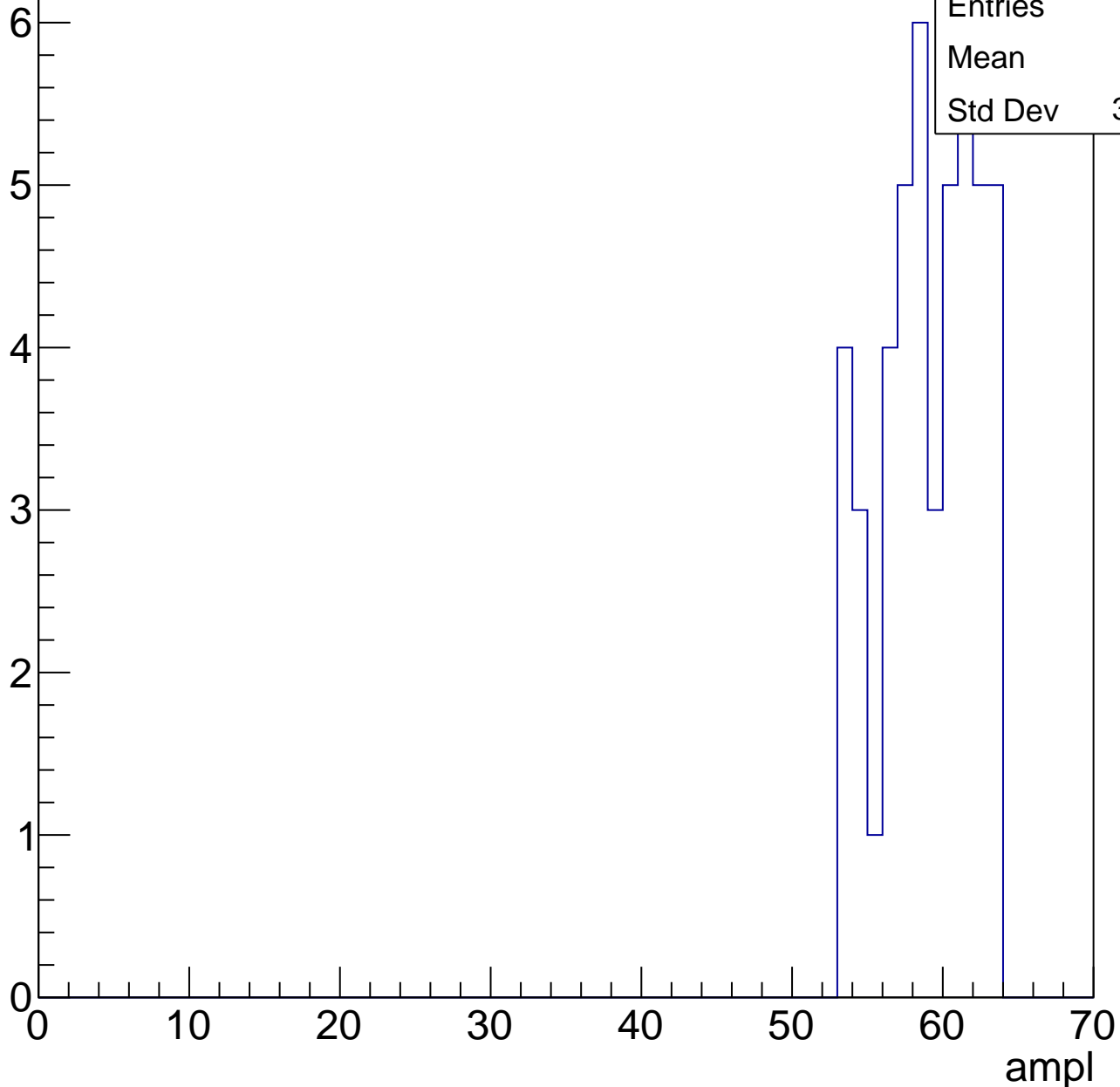
ampl



# B1L103S, U4-ch90, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



|         |       |
|---------|-------|
| Entries | 47    |
| Mean    | 58.6  |
| Std Dev | 3.071 |





# B1L103S, U4-ch90, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

|         |       |
|---------|-------|
| Entries | 21    |
| Mean    | 3     |
| Std Dev | 13.42 |

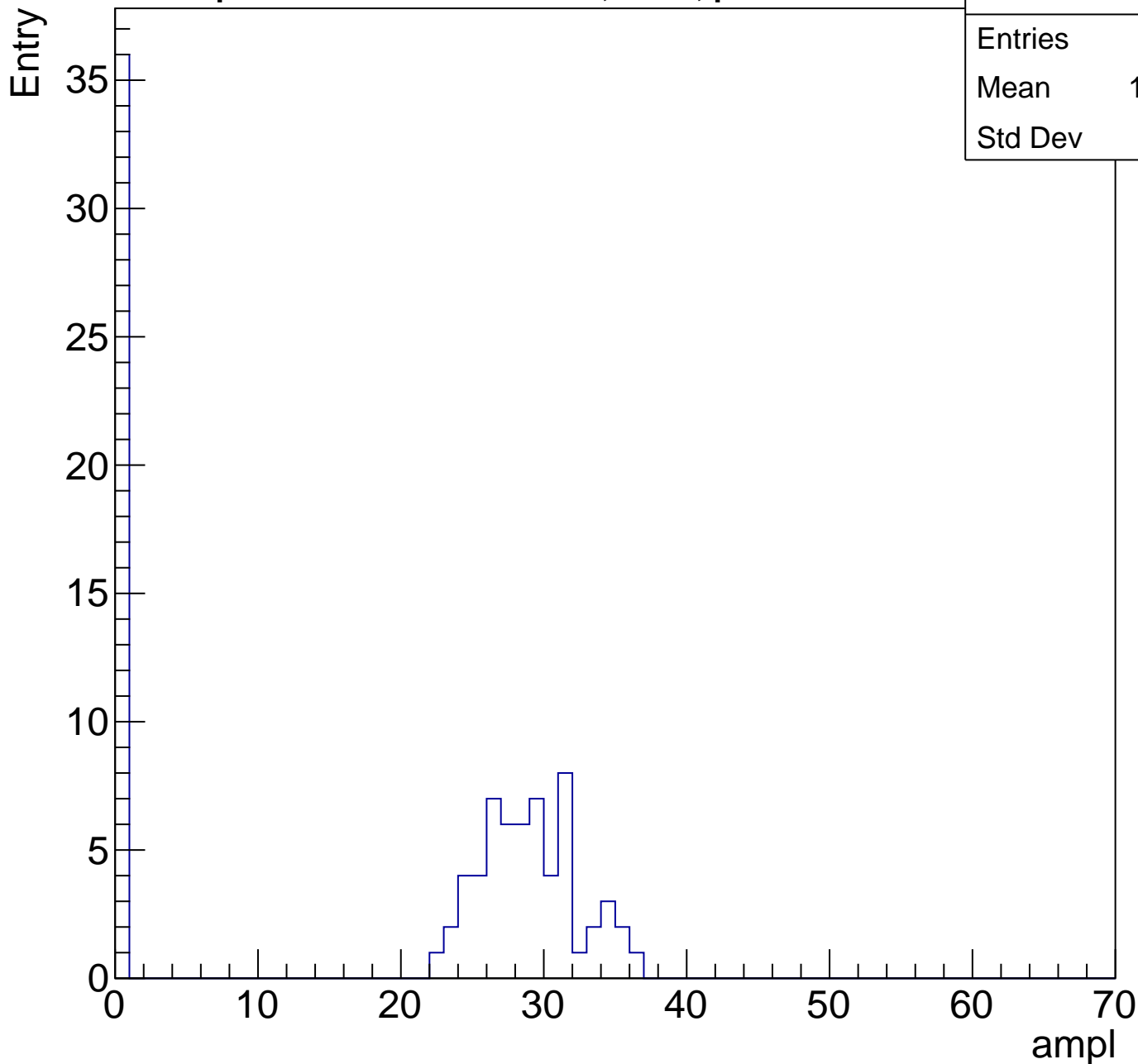
ampl

0 10 20 30 40 50 60 70

# B1L103S, U4-ch91, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 94    |
| Mean    | 17.59 |
| Std Dev | 14.1  |

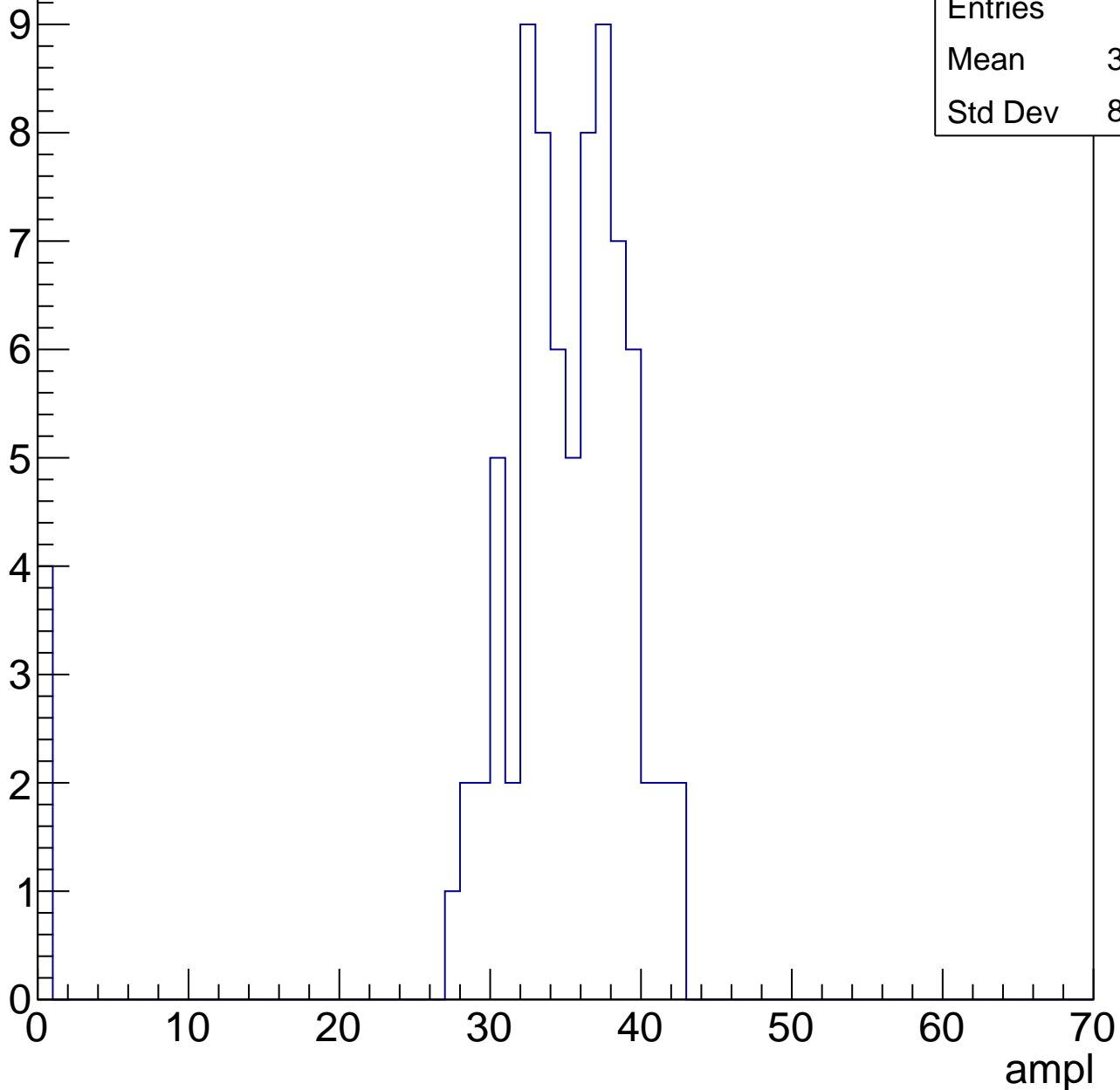


# B1L103S, U4-ch91, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 80    |
| Mean    | 33.14 |
| Std Dev | 8.333 |



# B1L103S, U4-ch91, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

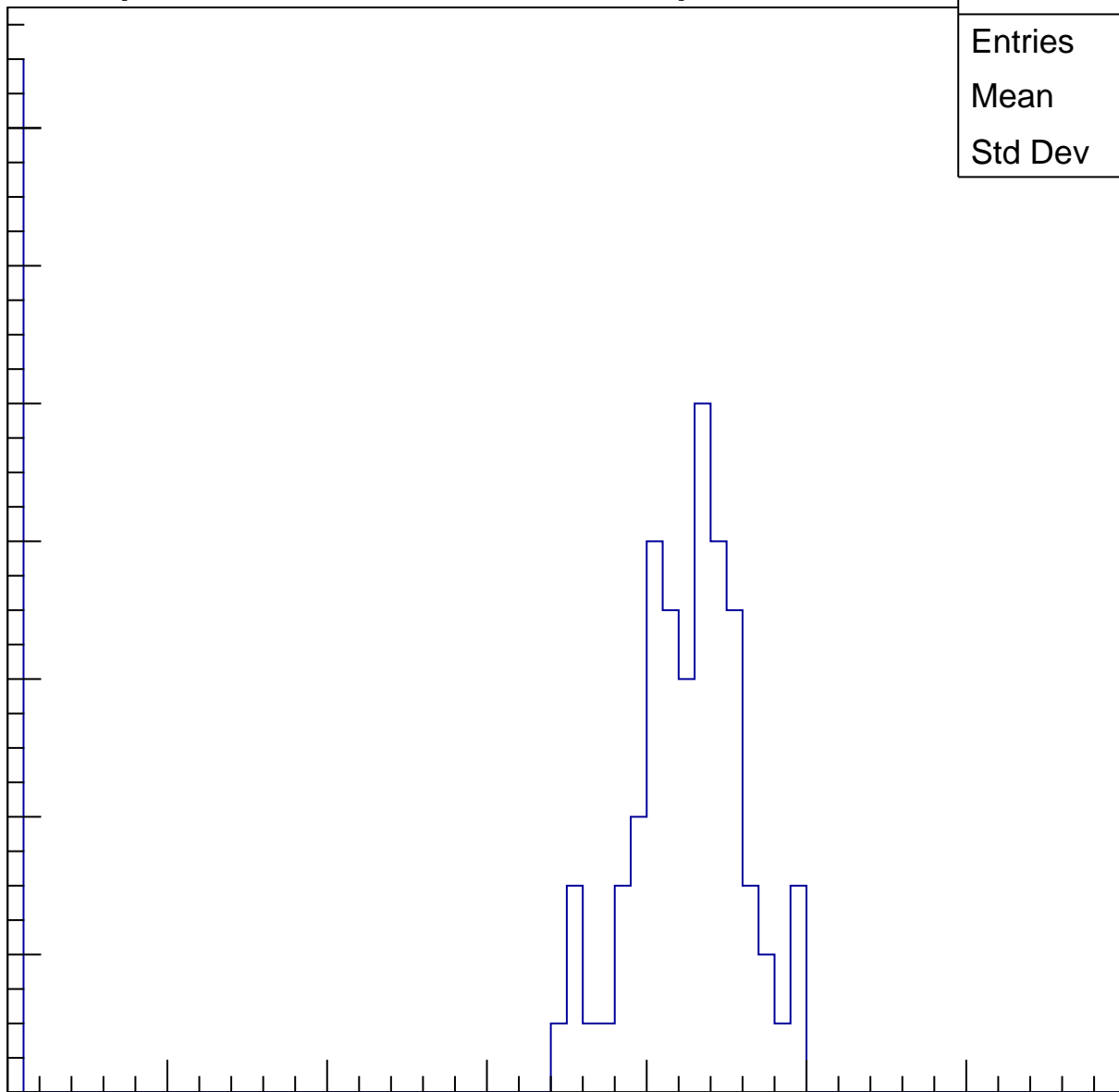
|         |       |
|---------|-------|
| Entries | 83    |
| Mean    | 34.52 |
| Std Dev | 16.5  |

Entry

14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

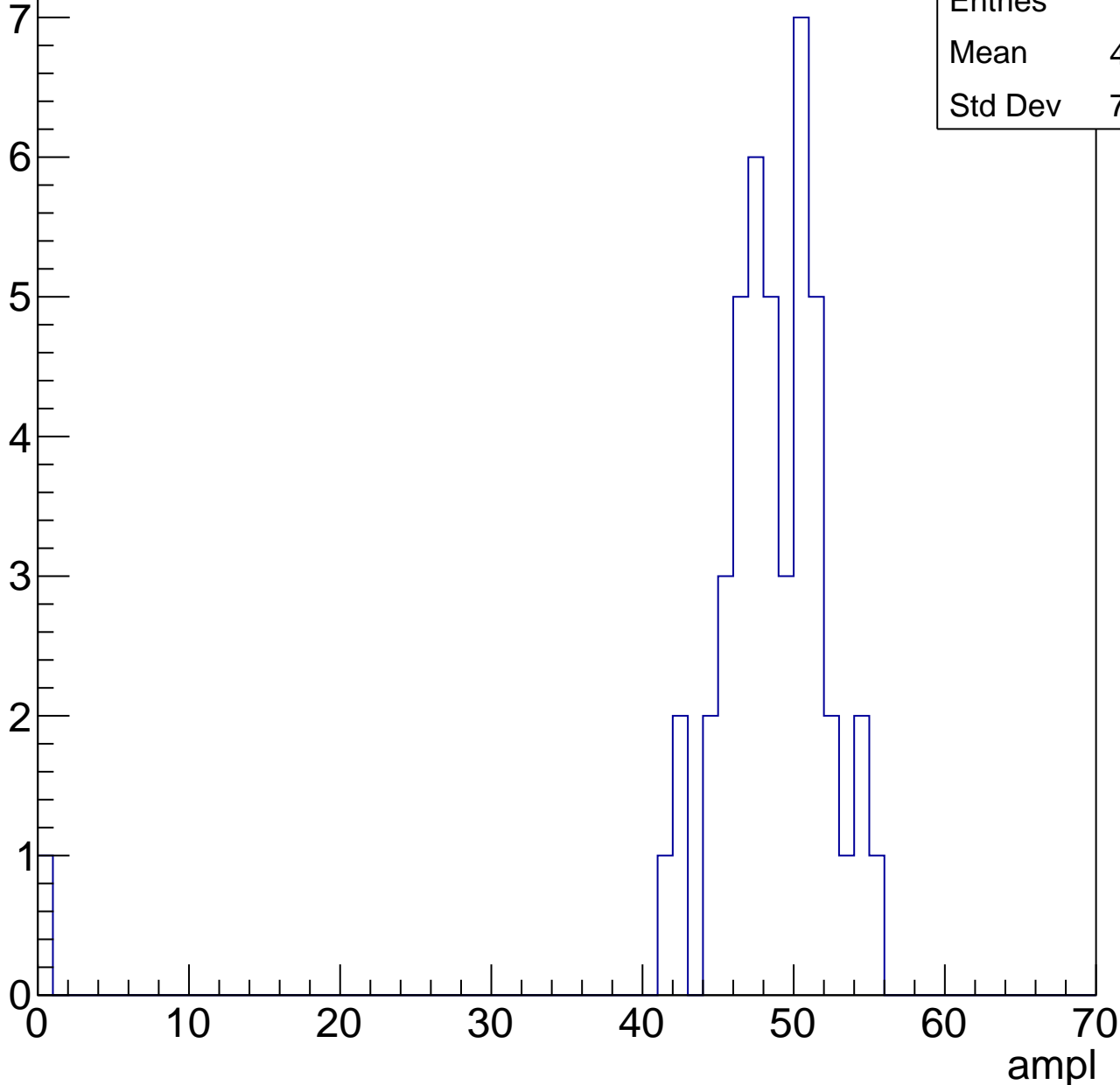


# B1L103S, U4-ch91, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 46    |
| Mean    | 47.22 |
| Std Dev | 7.712 |

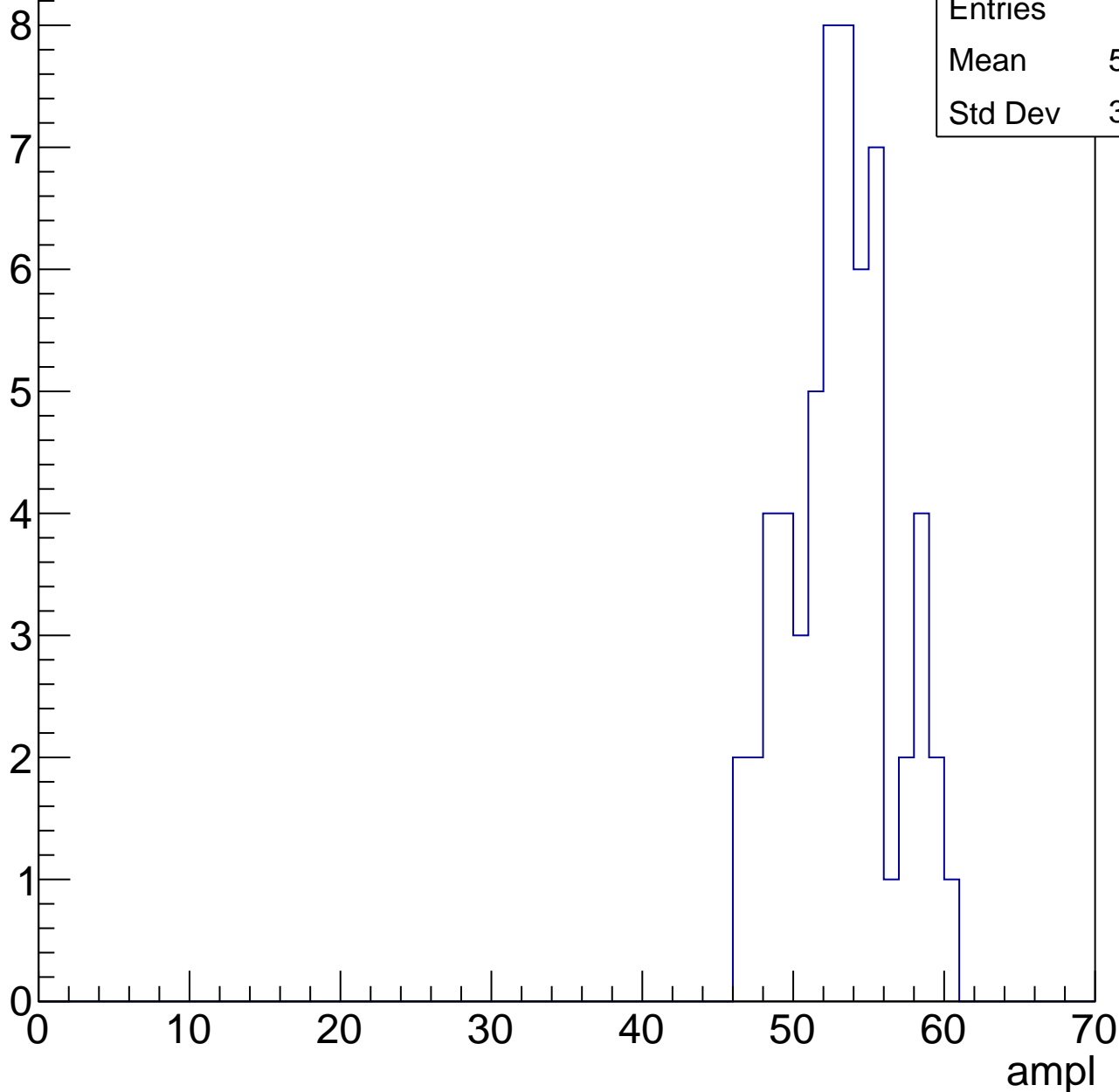


# B1L103S, U4-ch91, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 59    |
| Mean    | 52.68 |
| Std Dev | 3.392 |

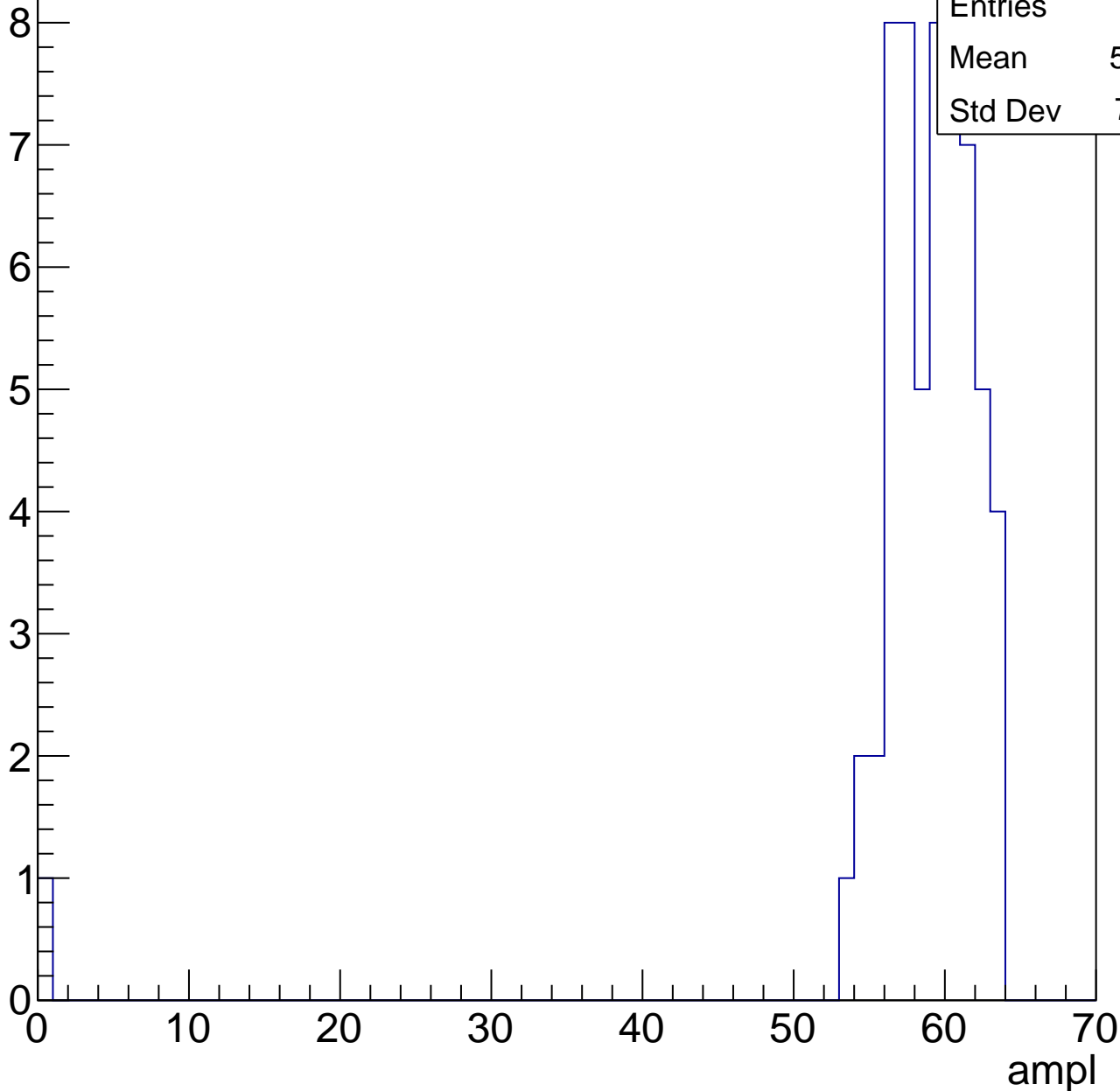


# B1L103S, U4-ch91, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 59    |
| Mean    | 57.73 |
| Std Dev | 7.981 |

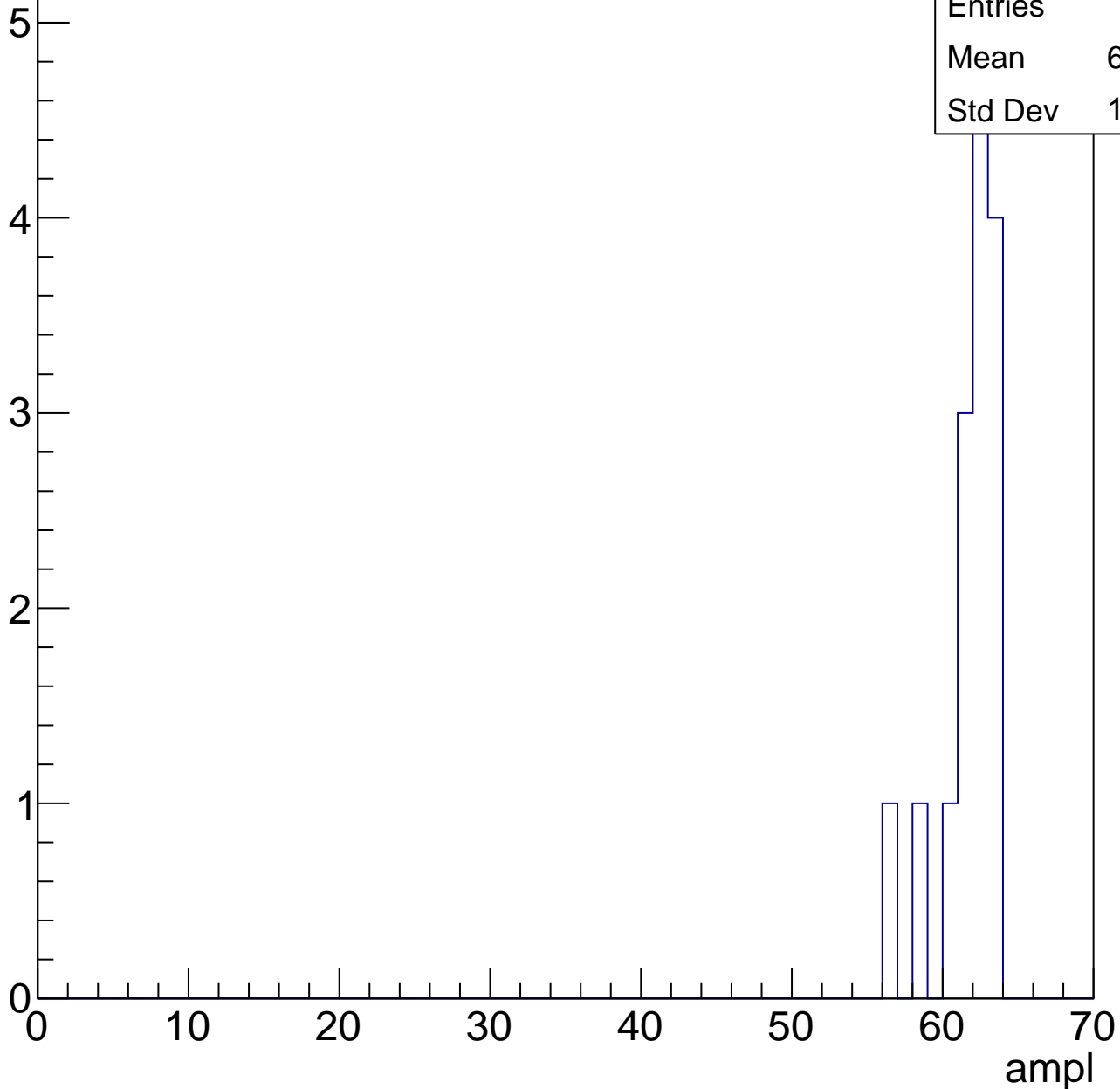


# B1L103S, U4-ch91, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 15    |
| Mean    | 61.27 |
| Std Dev | 1.914 |





# B1L103S, U4-ch91, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 21    |
| Mean    | 6     |
| Std Dev | 18.49 |

Entry

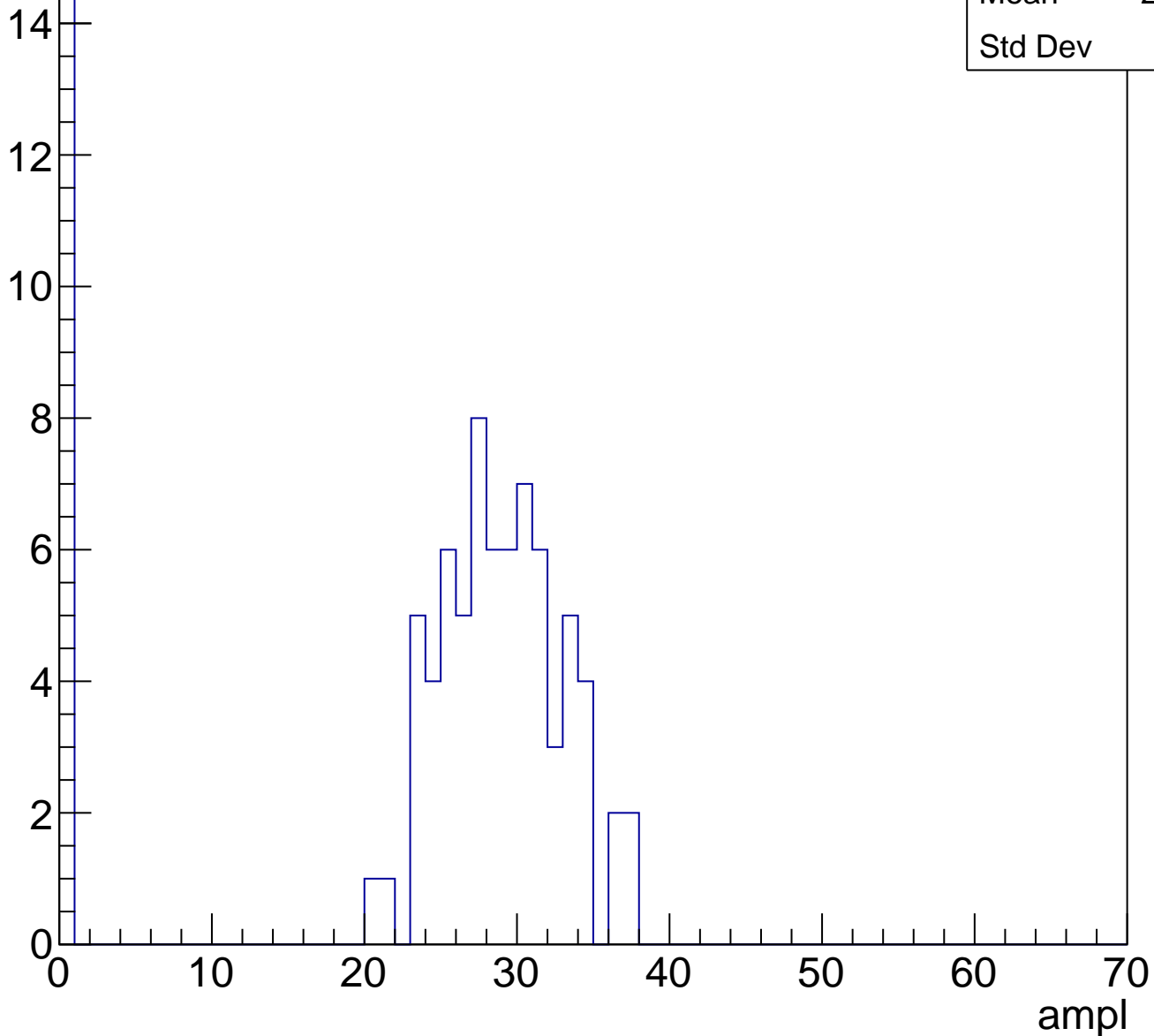


# B1L103S, U4-ch92, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 86    |
| Mean    | 23.59 |
| Std Dev | 11.4  |

Entry



# B1L103S, U4-ch92, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 76    |
| Mean    | 30.22 |
| Std Dev | 12.88 |

Entry

10

8

6

4

2

0

0

10

20

30

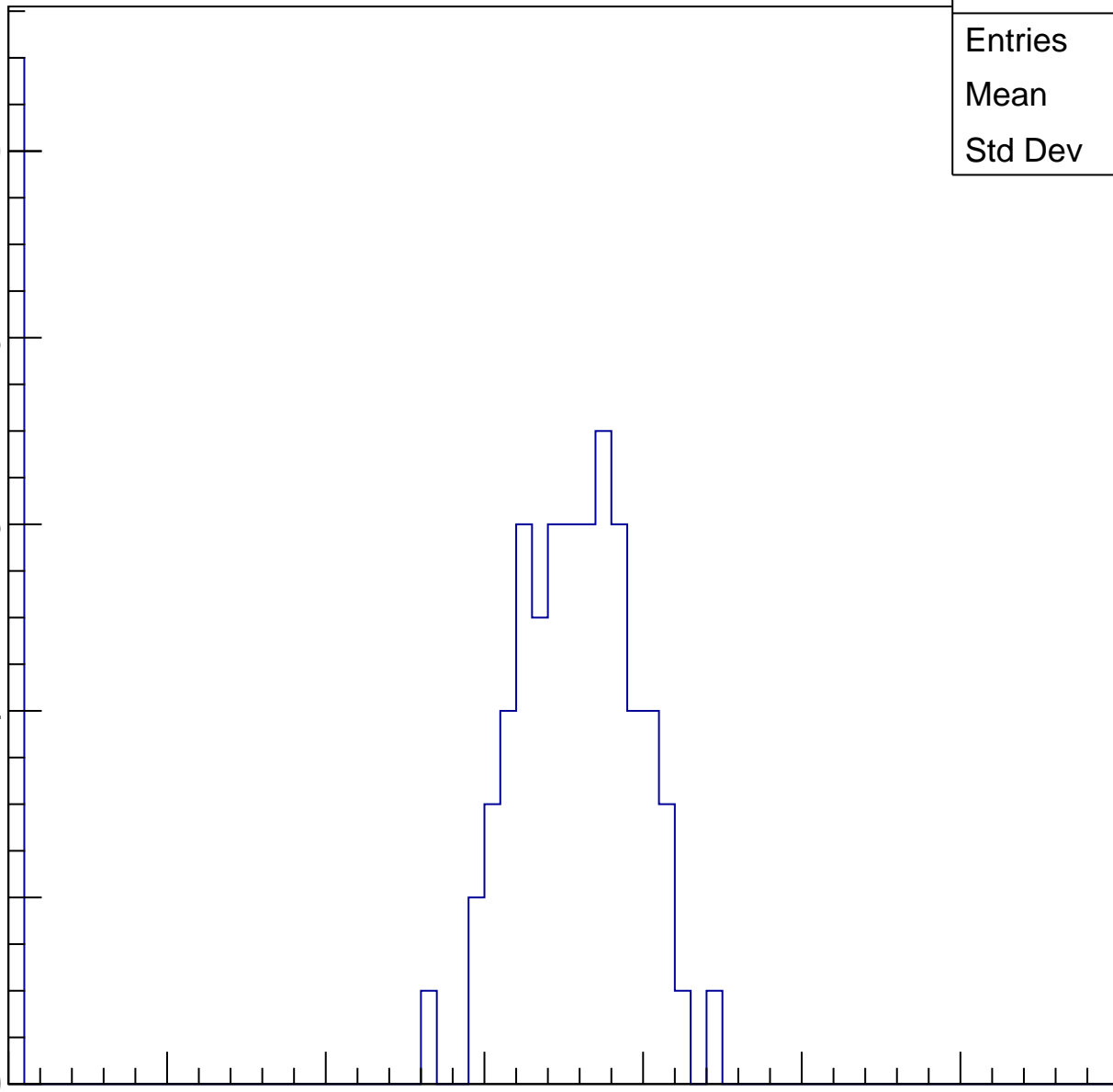
40

50

60

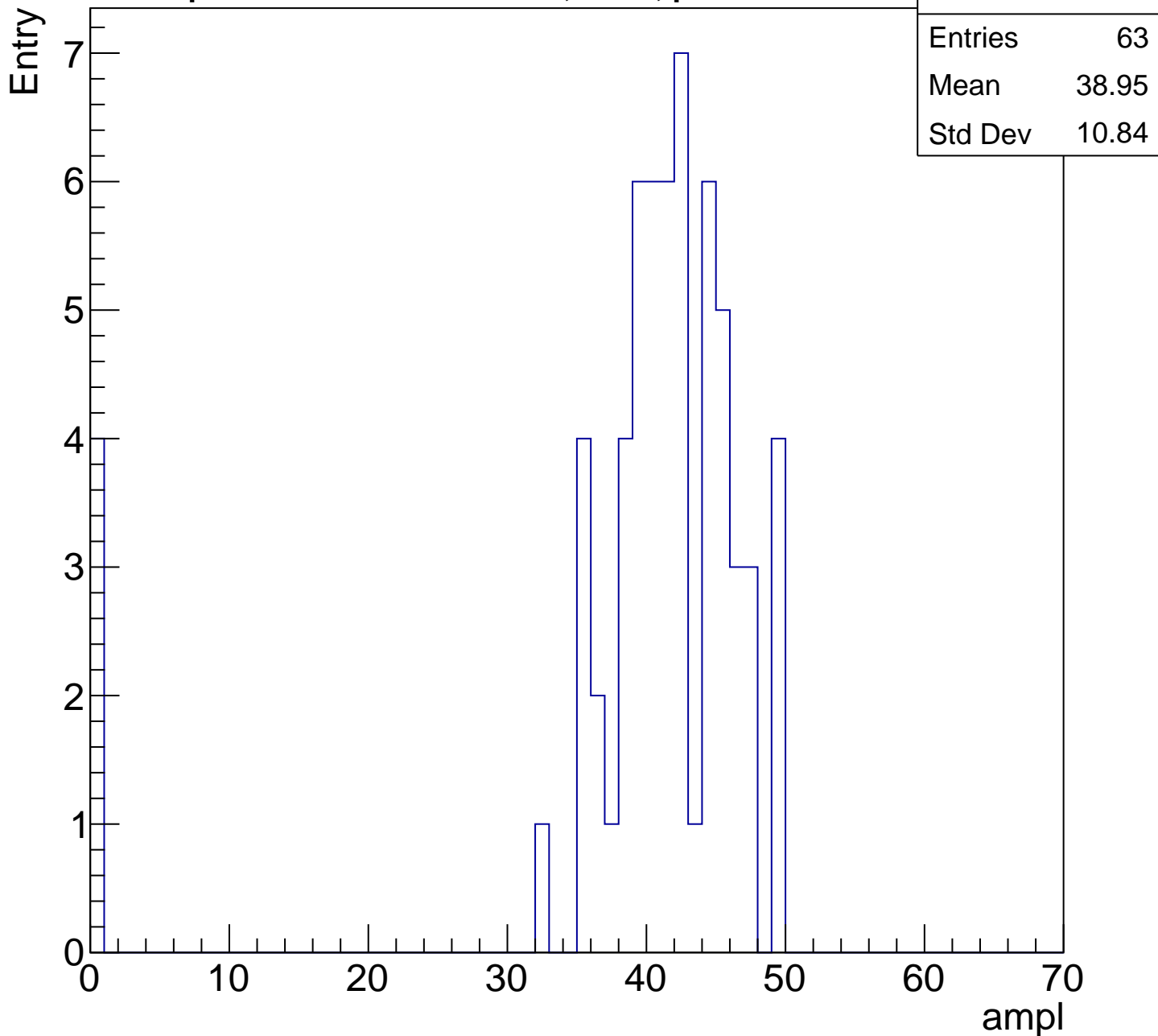
70

ampl



# B1L103S, U4-ch92, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

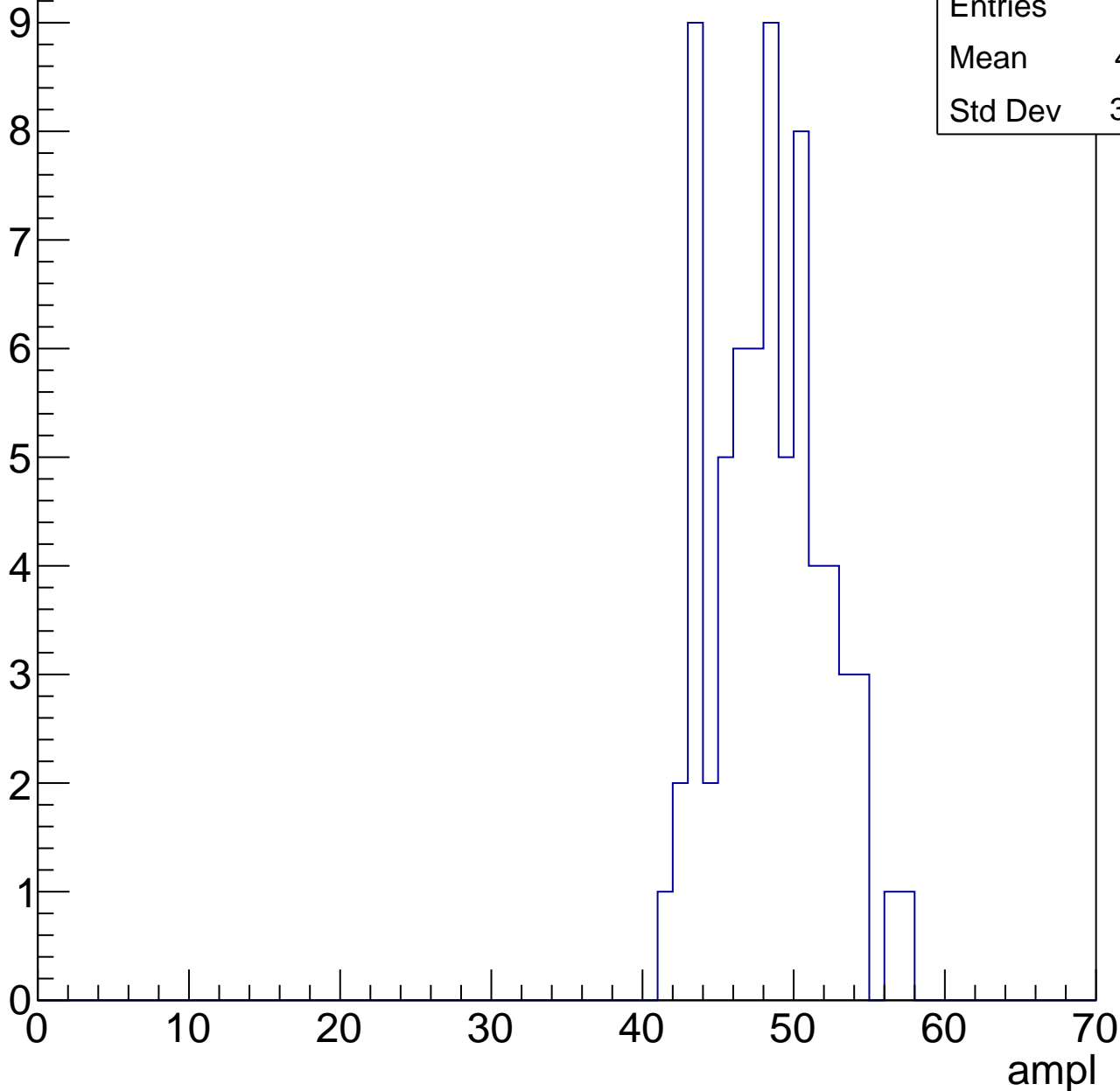


# B1L103S, U4-ch92, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 69    |
| Mean    | 47.91 |
| Std Dev | 3.646 |

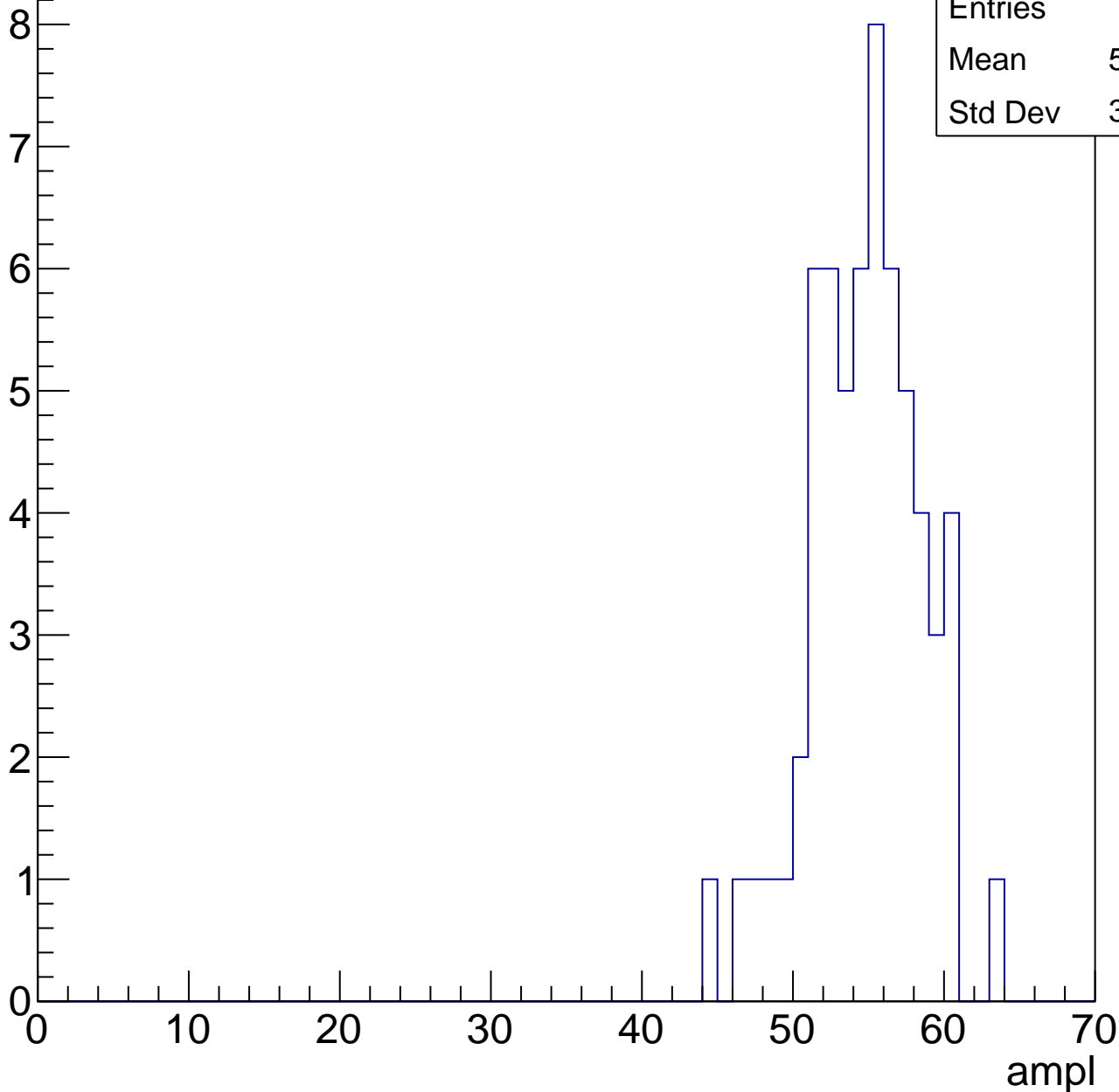


# B1L103S, U4-ch92, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 61    |
| Mean    | 54.33 |
| Std Dev | 3.674 |



# B1L103S, U4-ch92, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

7

6

5

4

3

2

1

0

Entries 45

Mean 57.91

Std Dev 9.123

ampl

0

10

20

30

40

50

60

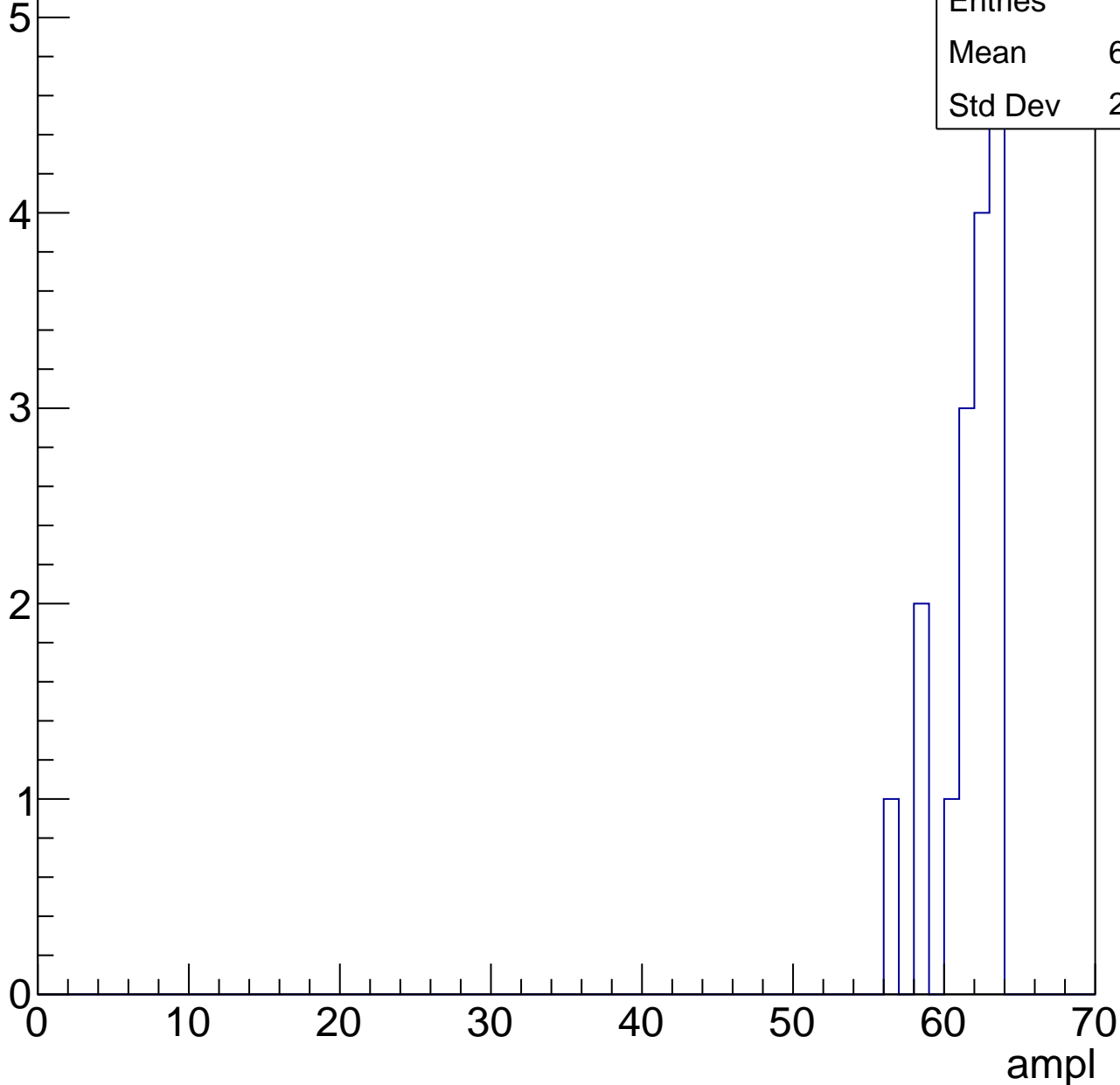
70

# B1L103S, U4-ch92, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 16    |
| Mean    | 61.12 |
| Std Dev | 2.058 |





# B1L103S, U4-ch92, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

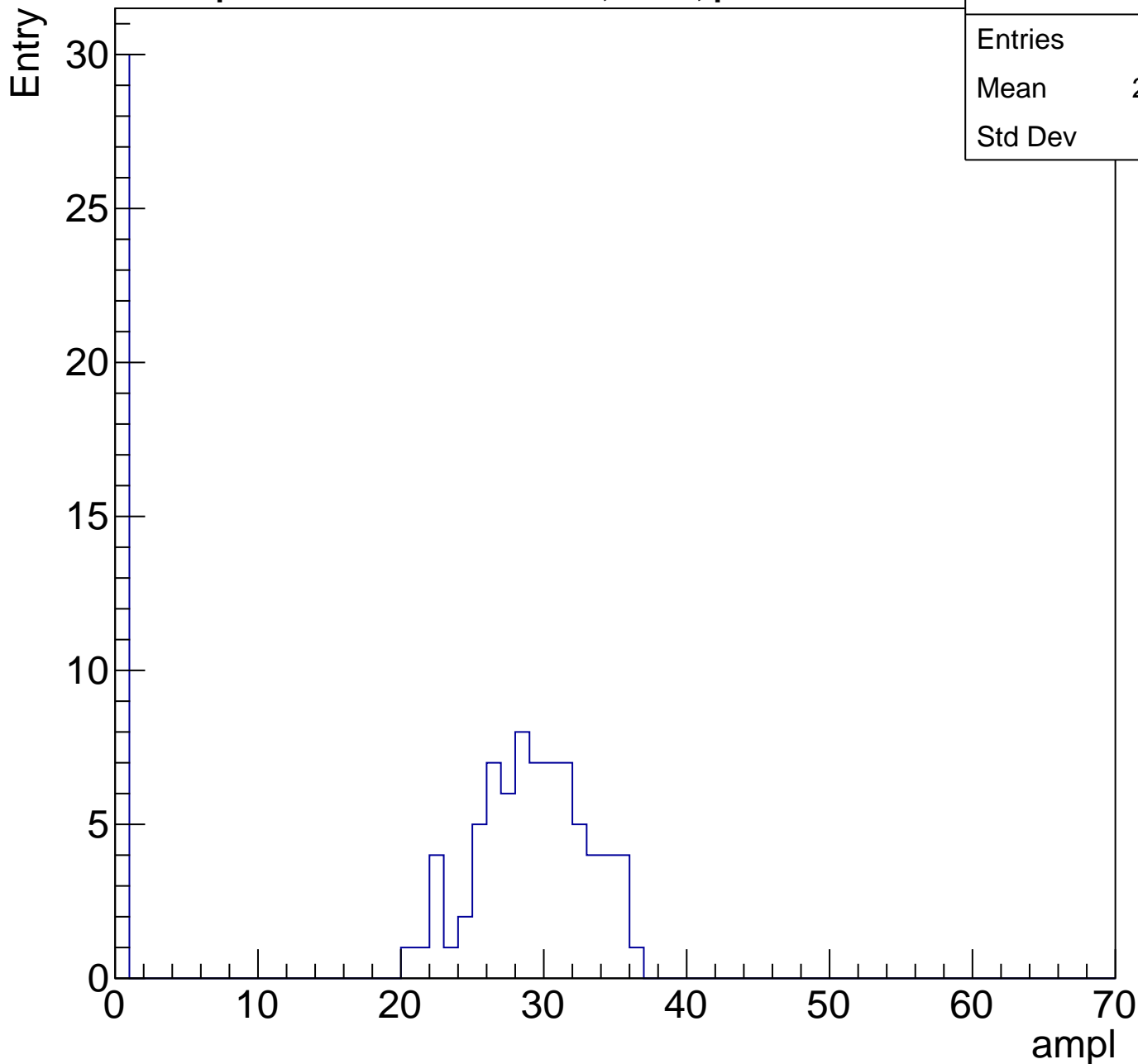
|         |    |
|---------|----|
| Entries | 19 |
| Mean    | 0  |
| Std Dev | 0  |

ampl

# B1L103S, U4-ch93, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 104   |
| Mean    | 20.45 |
| Std Dev | 13.4  |



# B1L103S, U4-ch93, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 71    |
| Mean    | 30.49 |
| Std Dev | 13.58 |

Entry

10

8

6

4

2

0

0

10

20

30

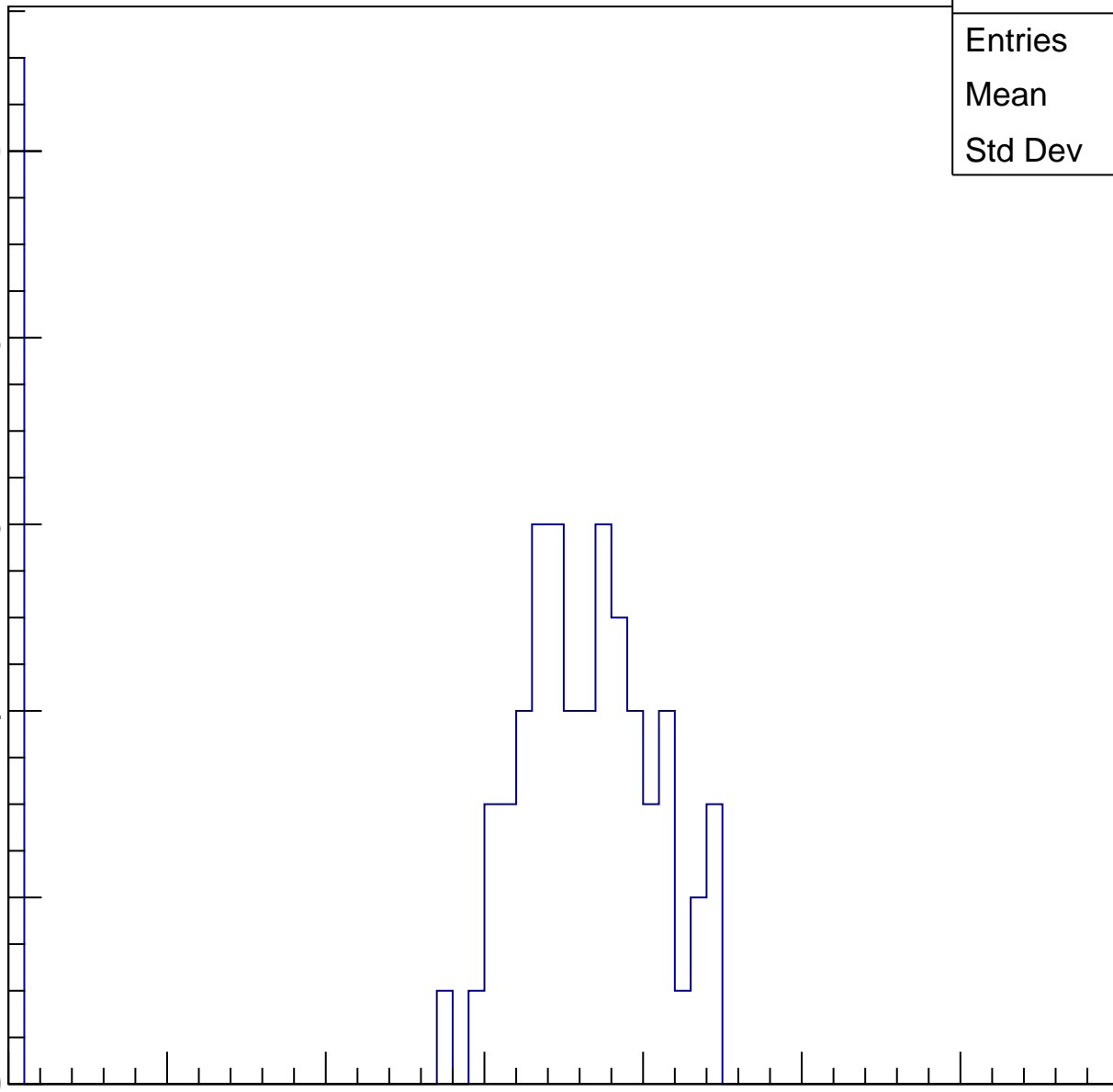
40

50

60

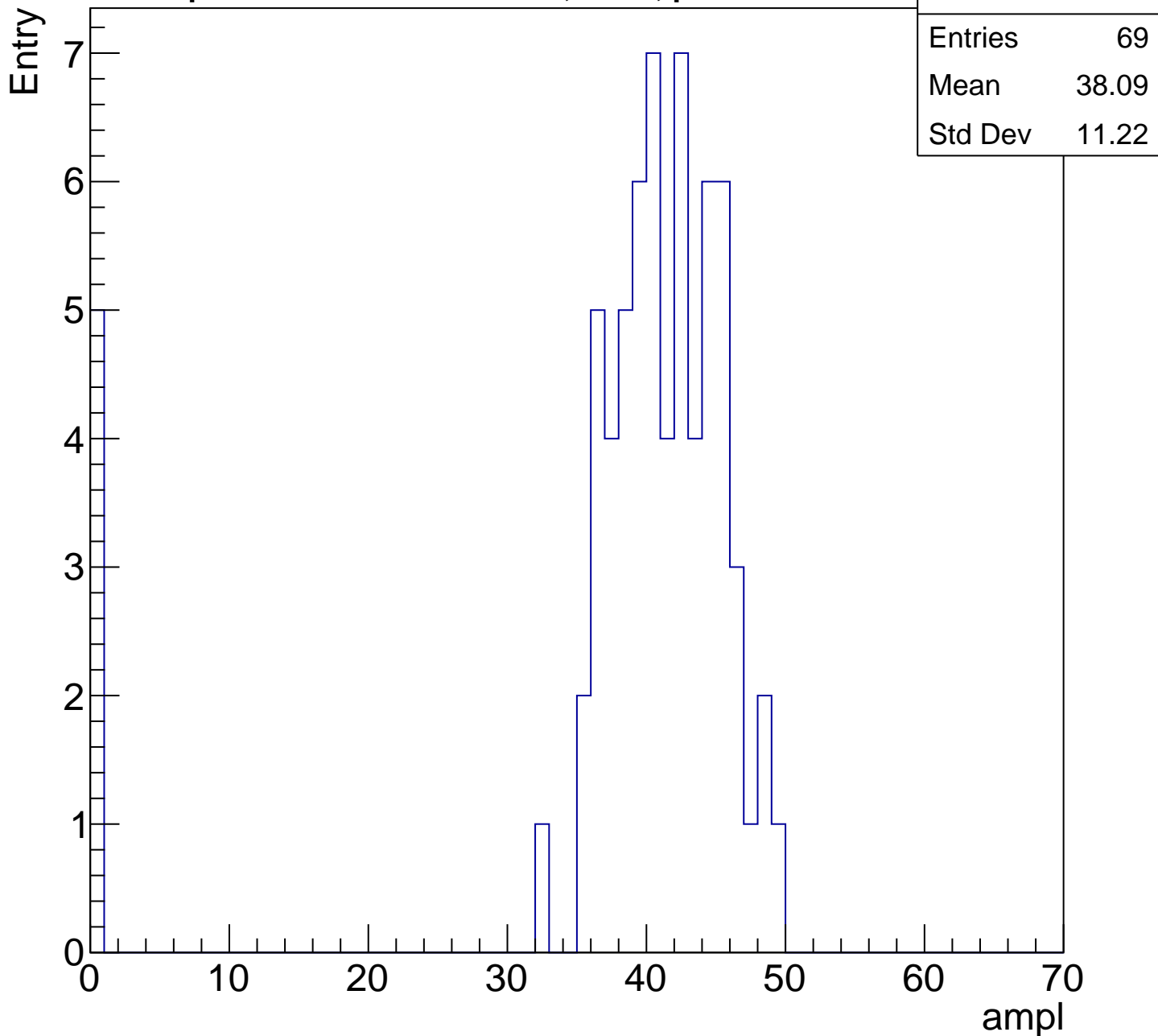
70

ampl



# B1L103S, U4-ch93, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

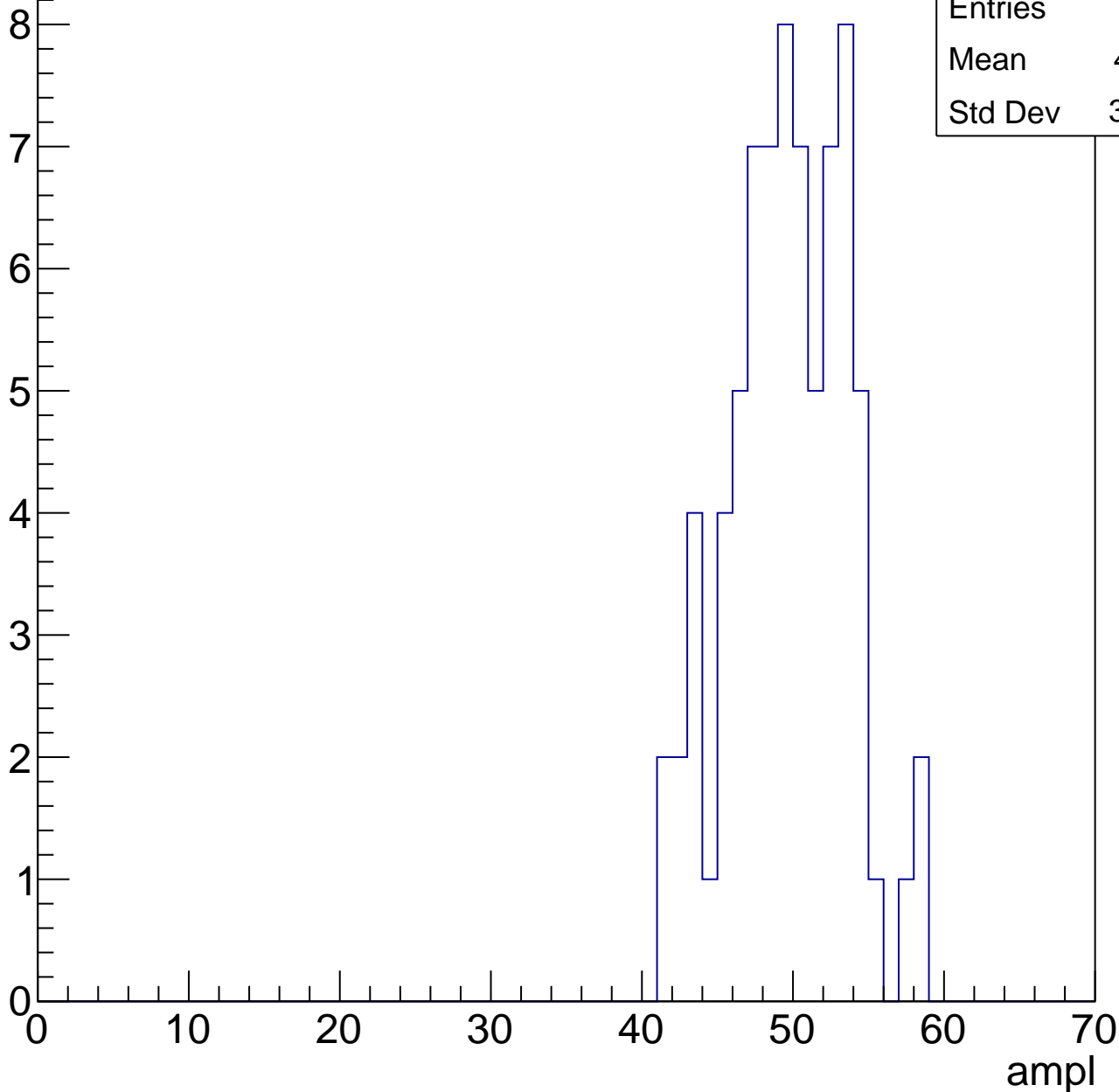


# B1L103S, U4-ch93, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 76    |
| Mean    | 49.21 |
| Std Dev | 3.874 |

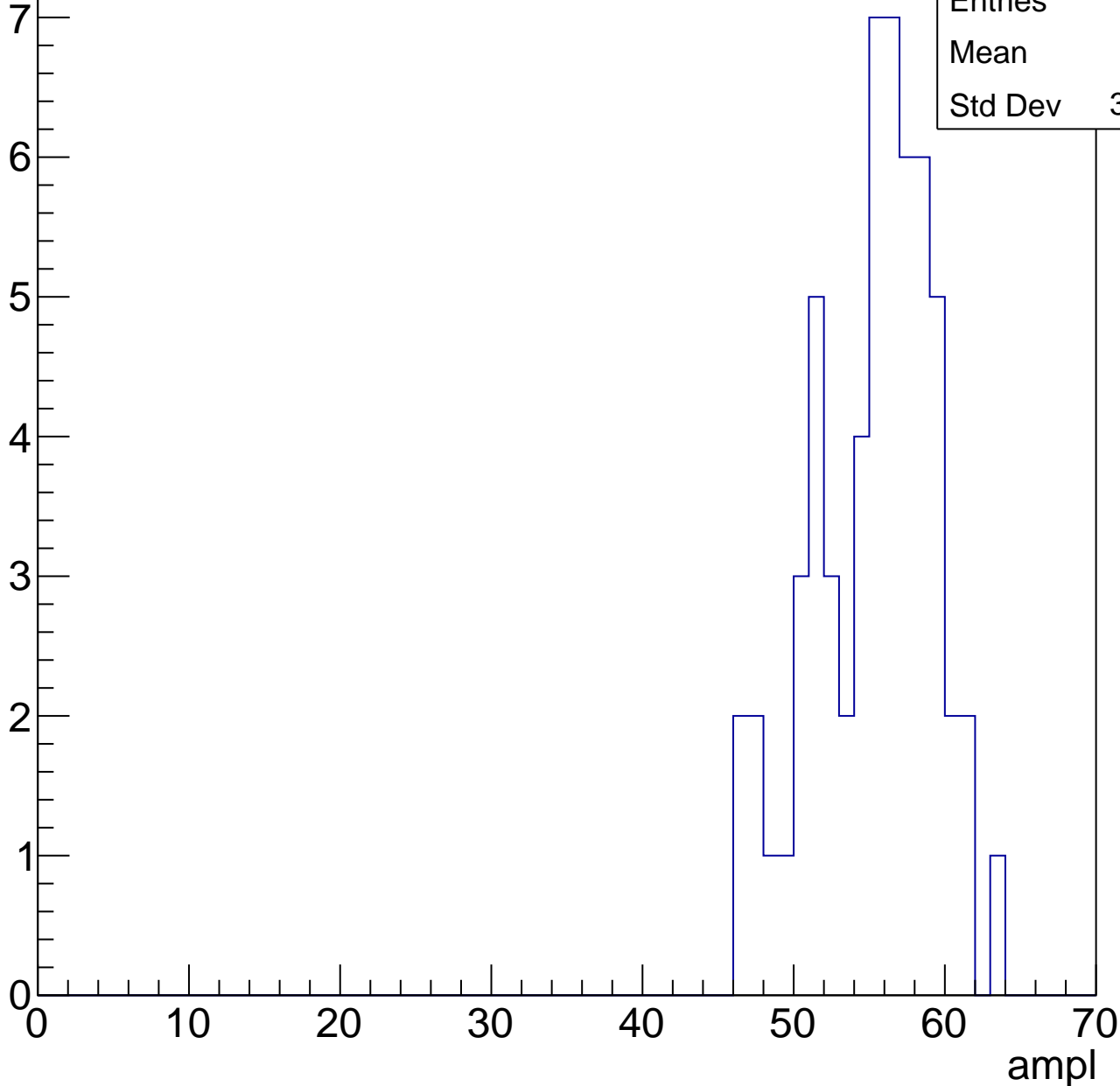


# B1L103S, U4-ch93, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 59    |
| Mean    | 54.8  |
| Std Dev | 3.944 |



# B1L103S, U4-ch93, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

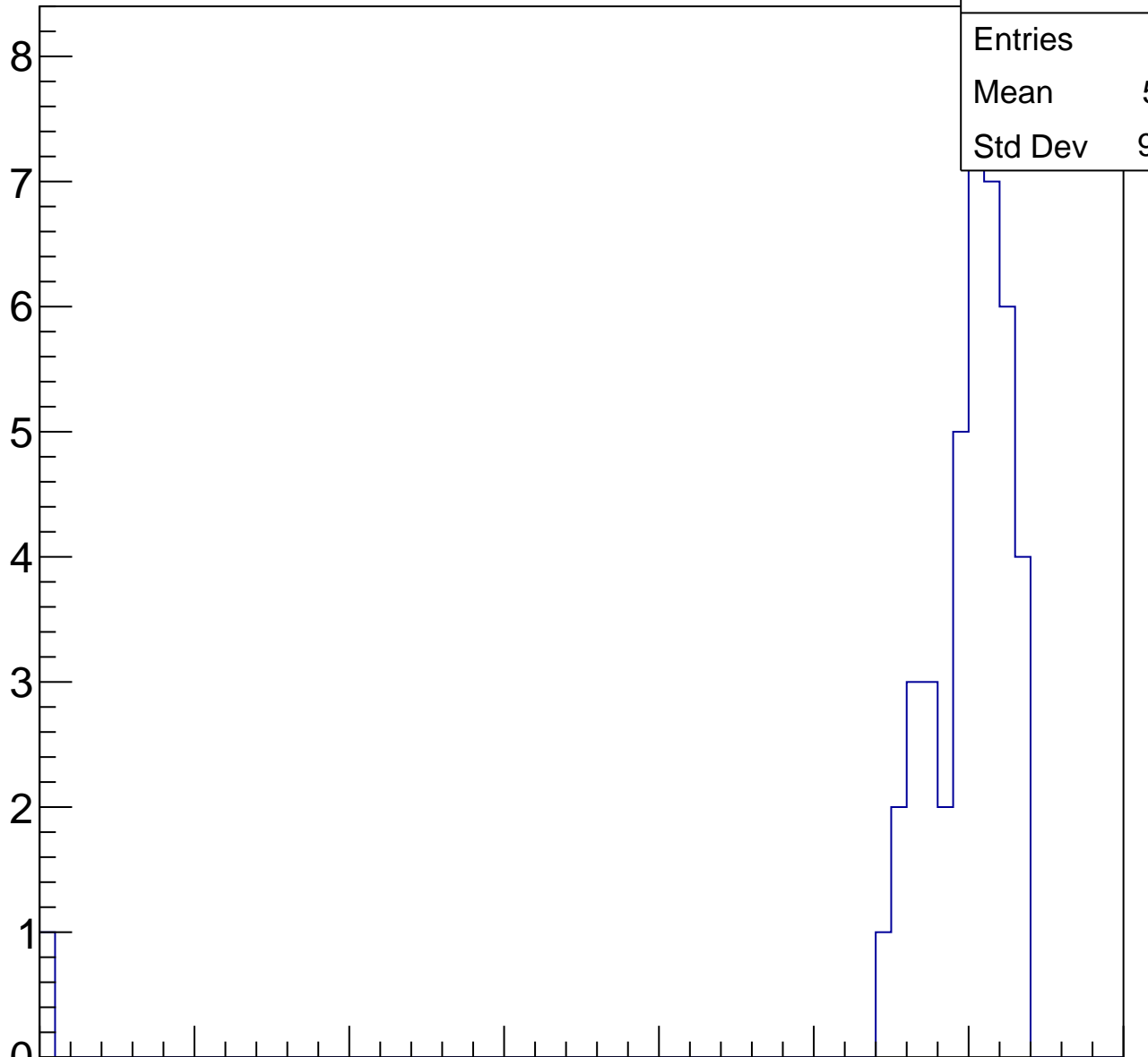
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

|         |       |
|---------|-------|
| Entries | 42    |
| Mean    | 58.21 |
| Std Dev | 9.395 |

ampl

0 10 20 30 40 50 60 70

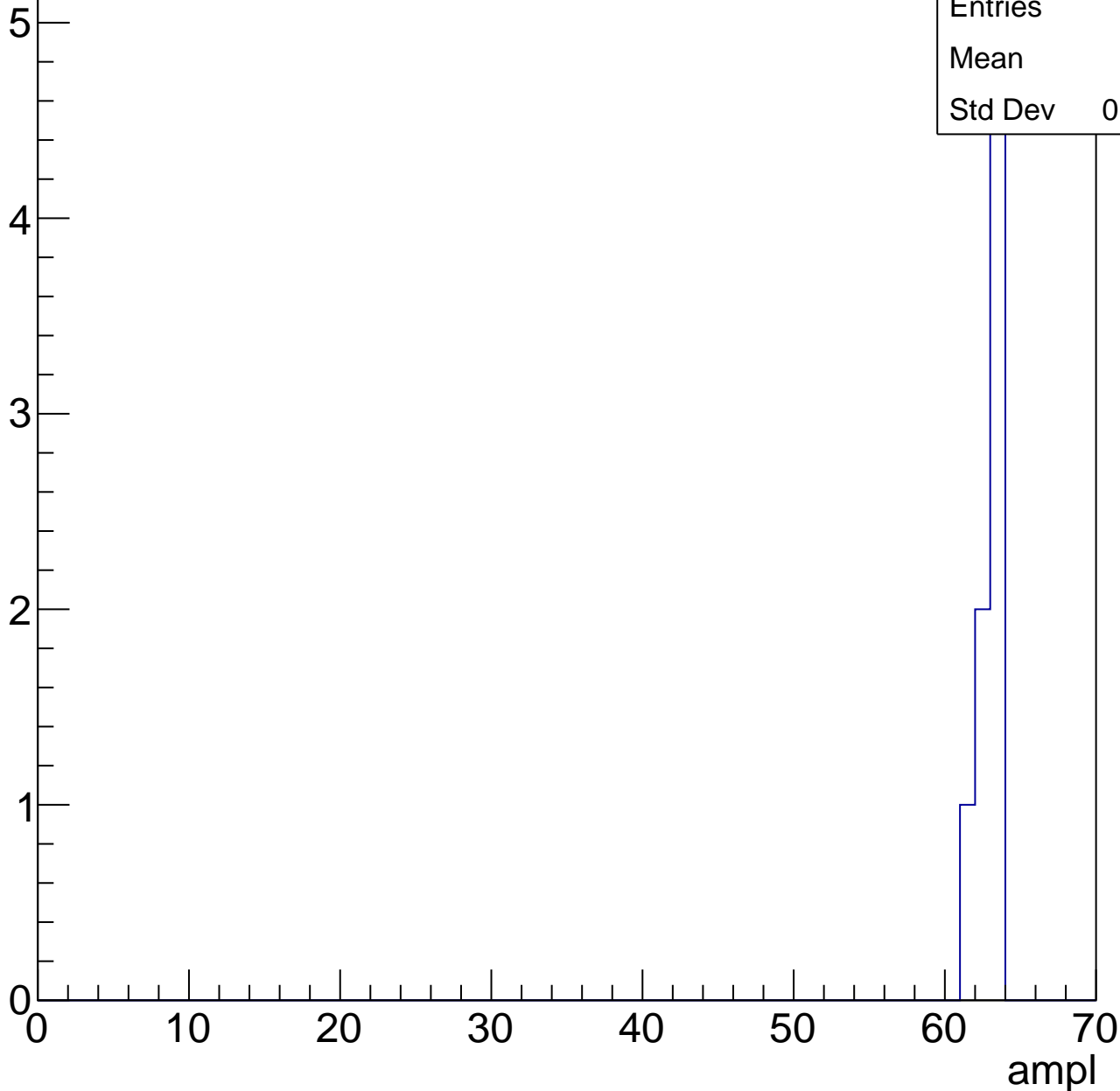


# B1L103S, U4-ch93, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |        |
|---------|--------|
| Entries | 8      |
| Mean    | 62.5   |
| Std Dev | 0.7071 |



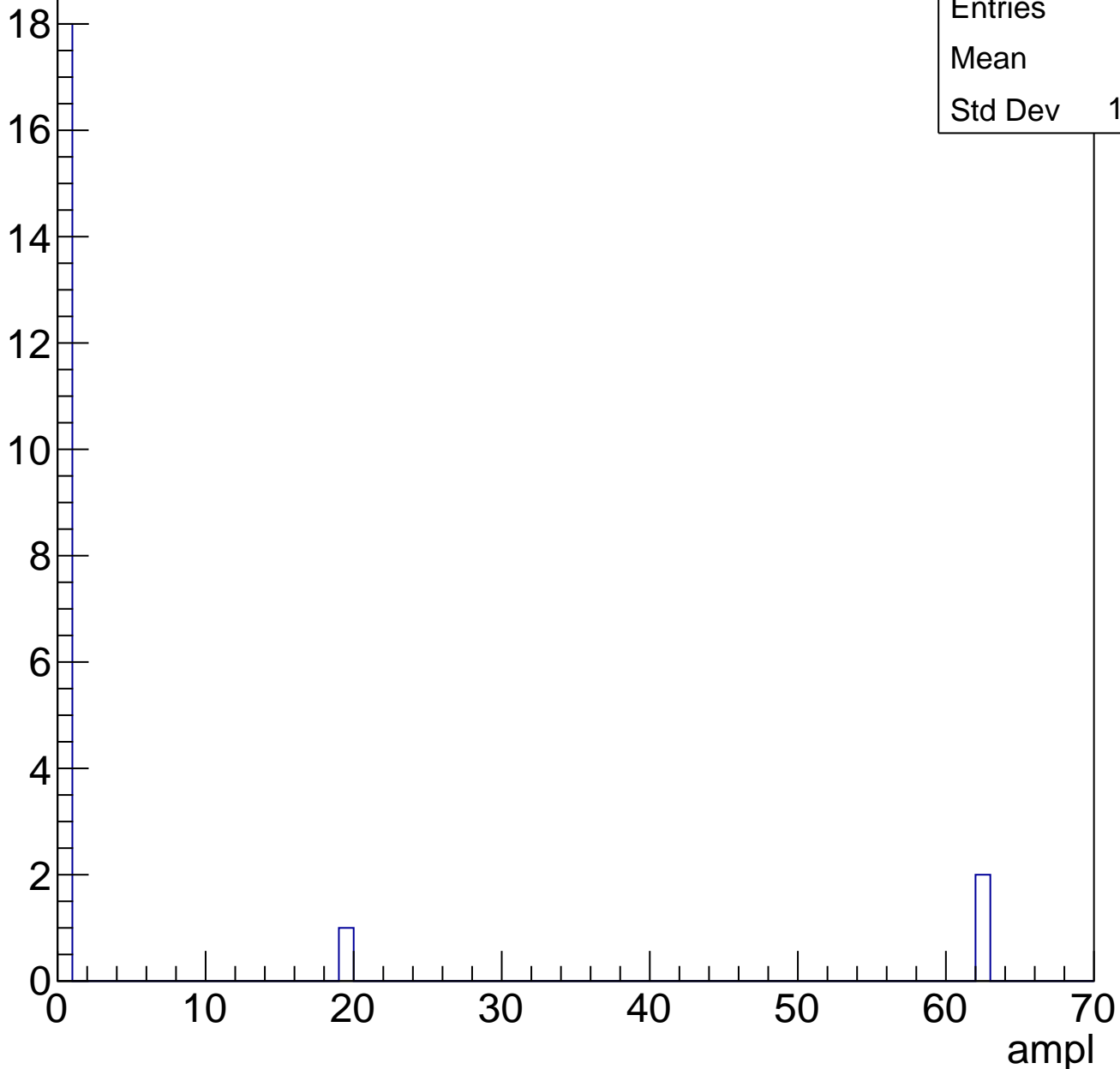


# B1L103S, U4-ch93, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 21    |
| Mean    | 6.81  |
| Std Dev | 18.36 |

Entry



# B1L103S, U4-ch94, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 71    |
| Mean    | 24.49 |
| Std Dev | 10.83 |

Entry

10

8

6

4

2

0

0

10

20

30

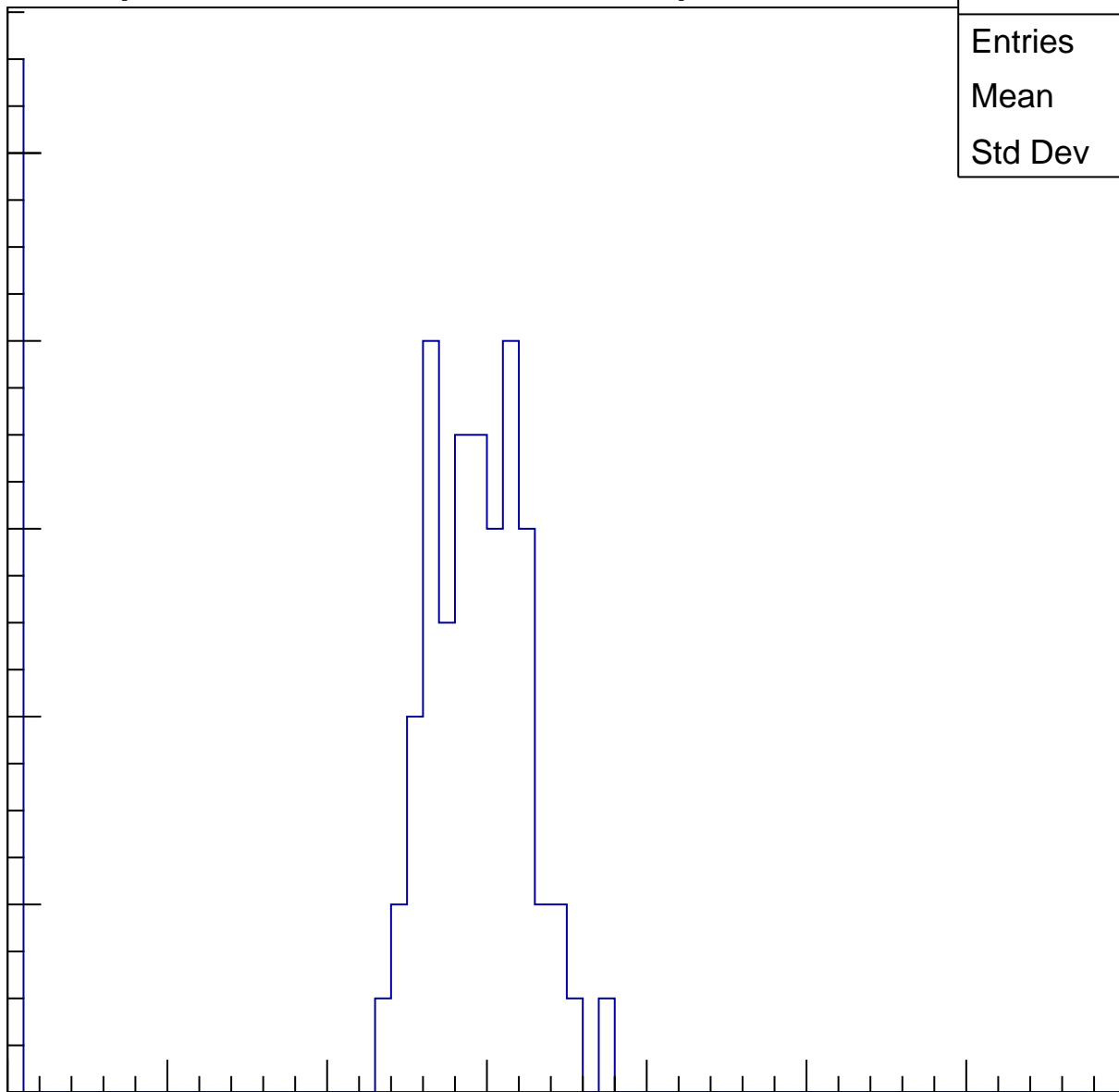
40

50

60

70

ampl



# B1L103S, U4-ch94, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

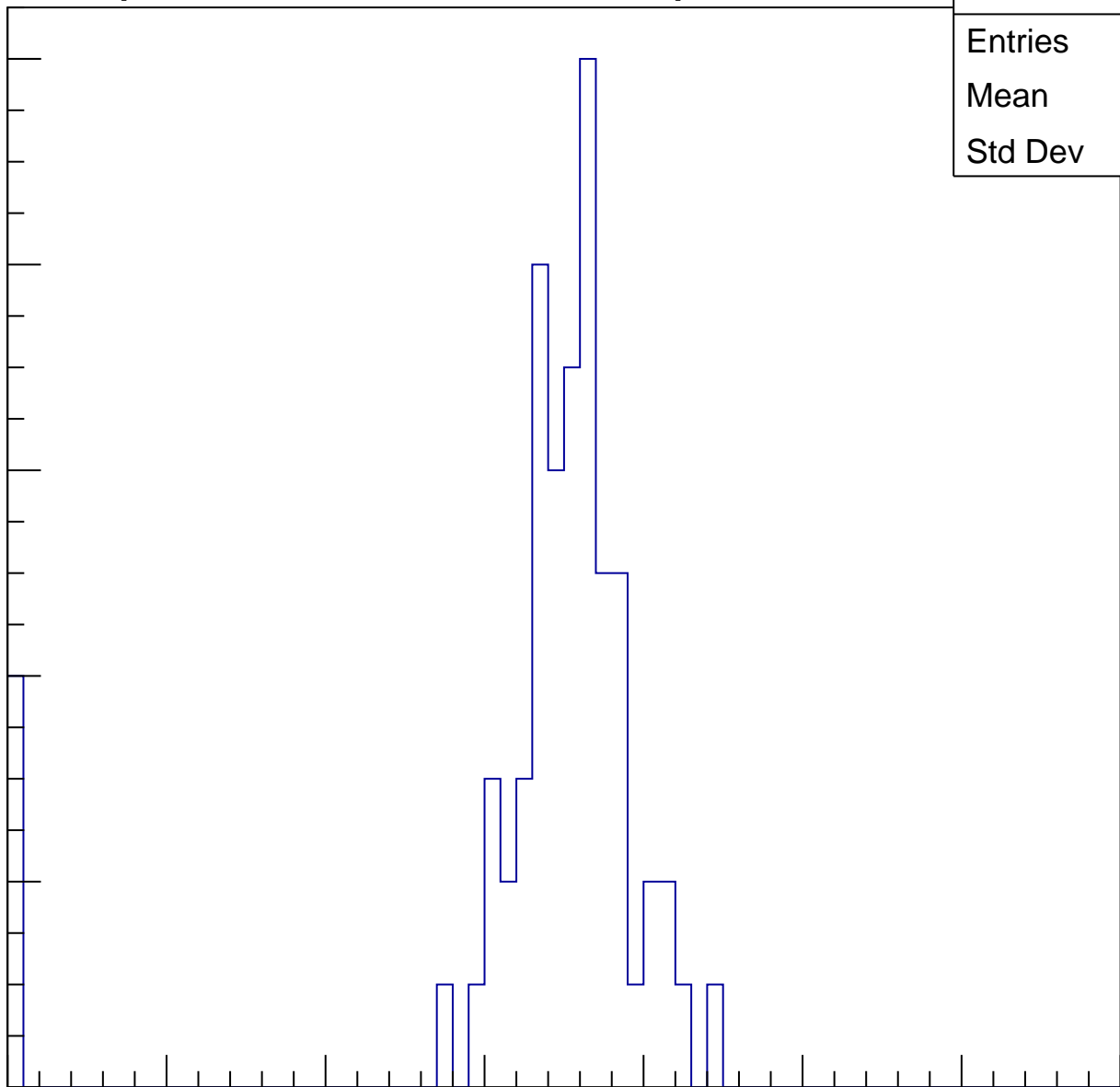
|         |       |
|---------|-------|
| Entries | 62    |
| Mean    | 32.89 |
| Std Dev | 9.192 |

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L103S, U4-ch94, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

10

8

6

4

2

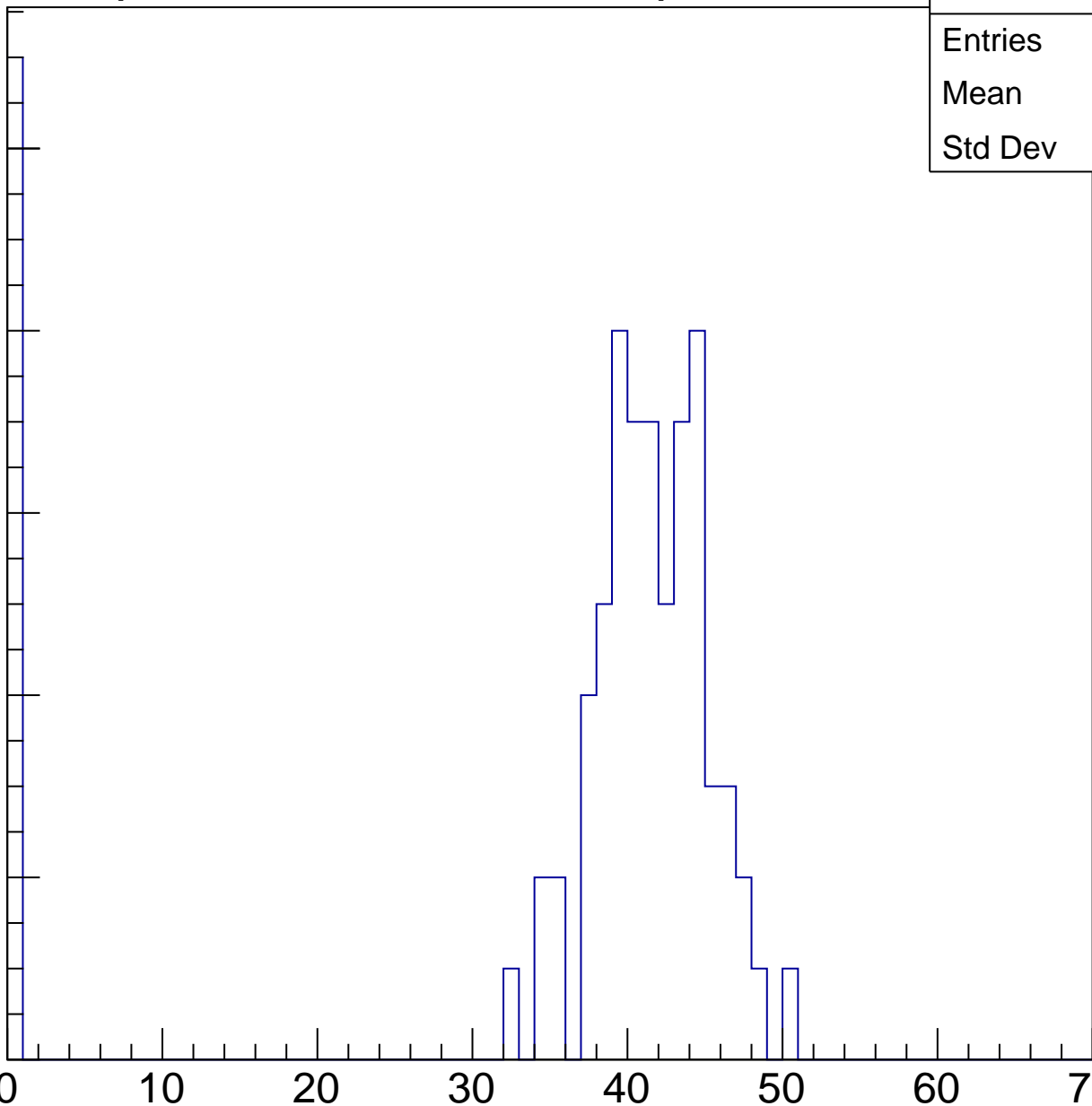
0

Entries 77

Mean 35.26

Std Dev 14.76

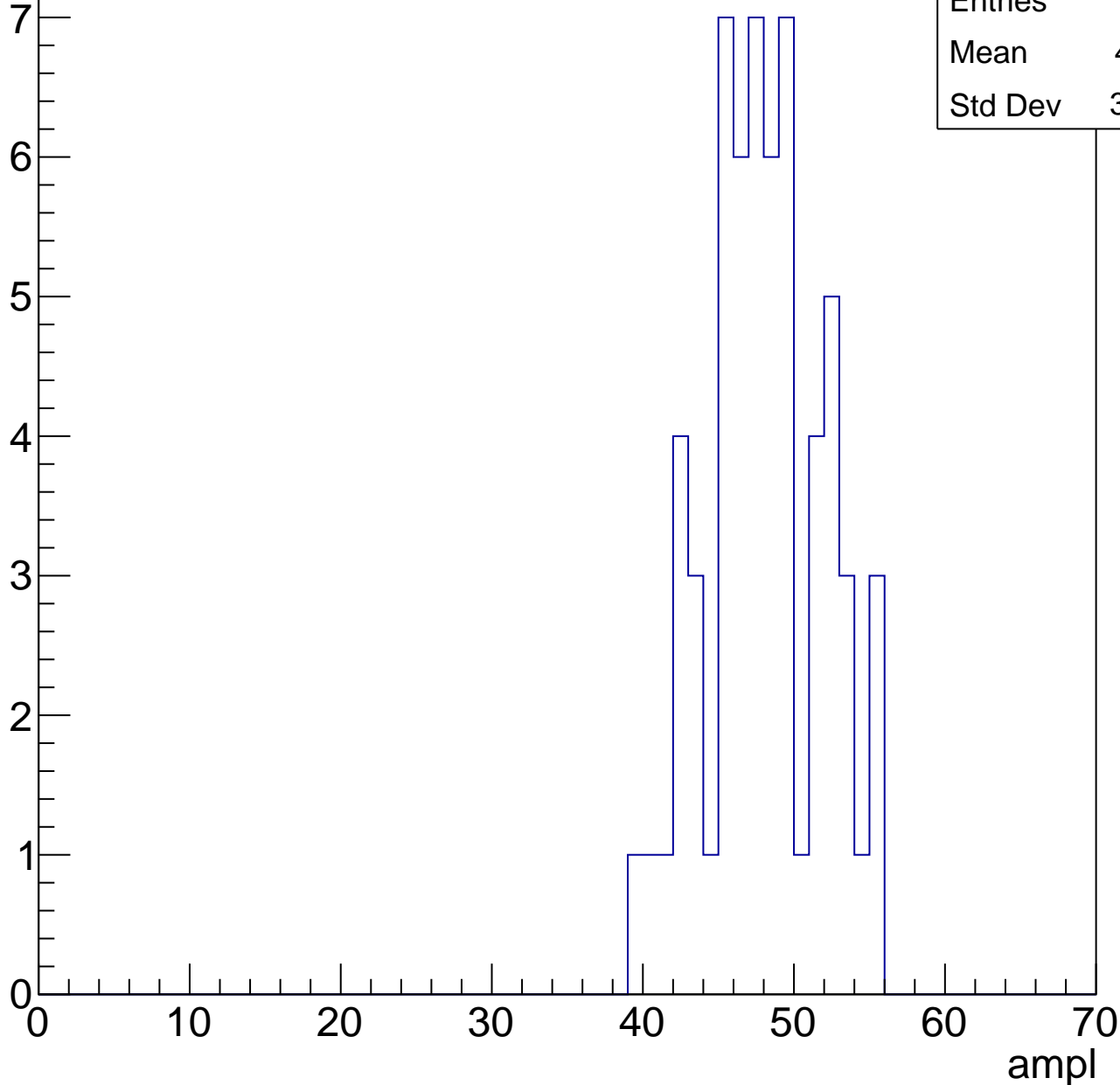
ampl



# B1L103S, U4-ch94, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



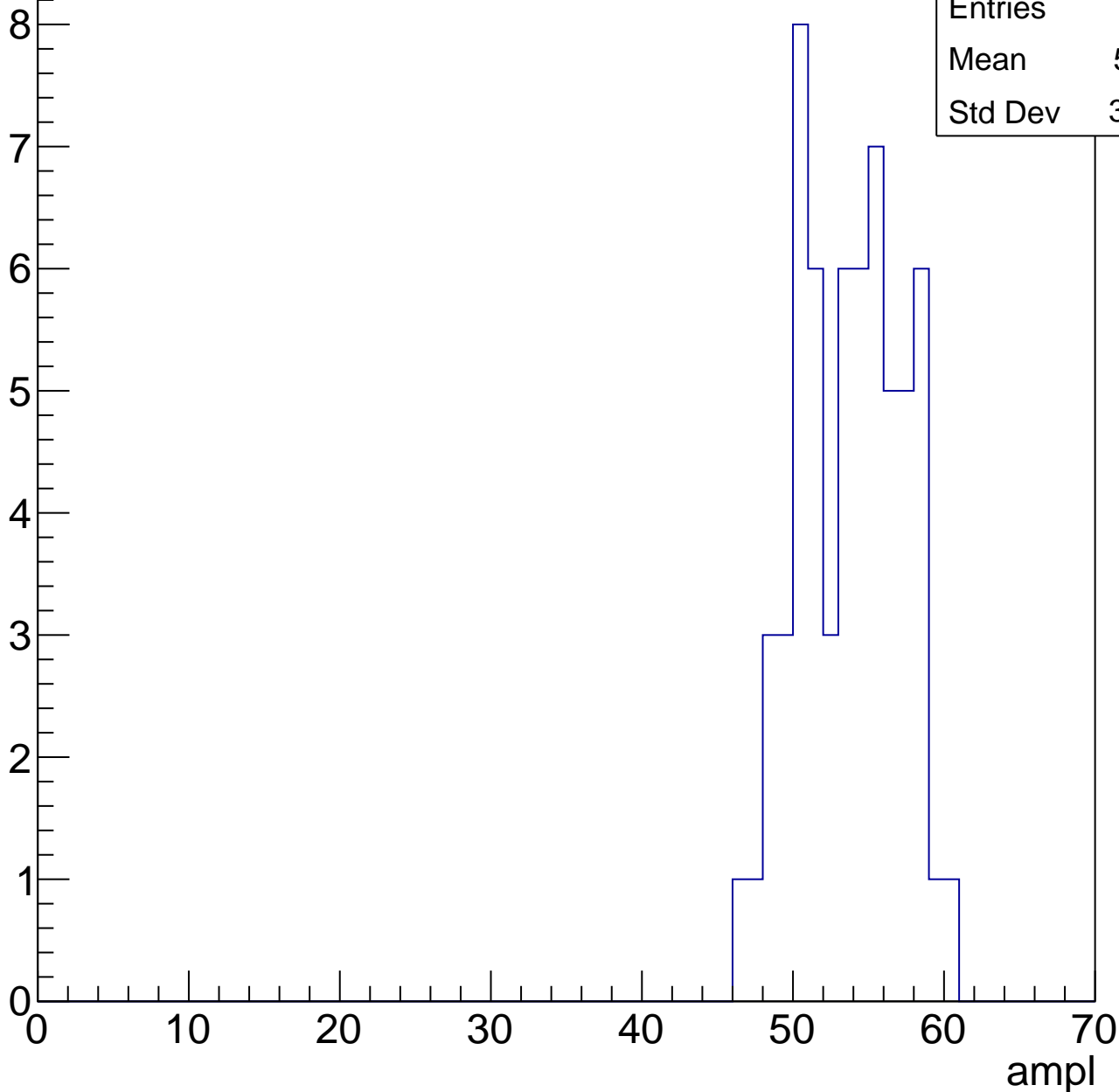
|         |       |
|---------|-------|
| Entries | 61    |
| Mean    | 47.61 |
| Std Dev | 3.838 |

# B1L103S, U4-ch94, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 62    |
| Mean    | 53.31 |
| Std Dev | 3.349 |



# B1L103S, U4-ch94, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

7

6

5

4

3

2

1

0

Entries

45

Mean

58.84

Std Dev

3.127

0

0

10

20

30

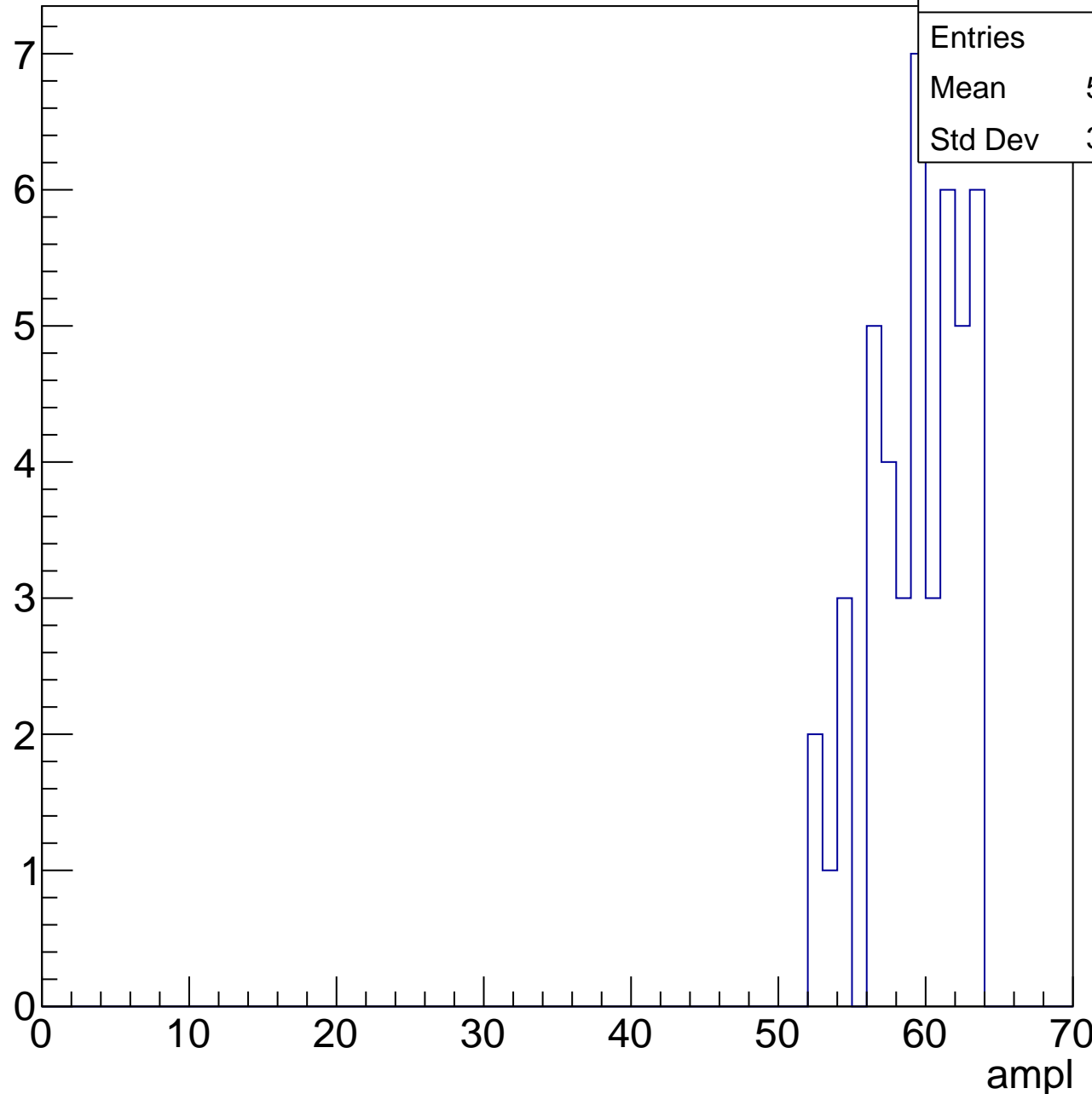
40

50

60

70

ampl

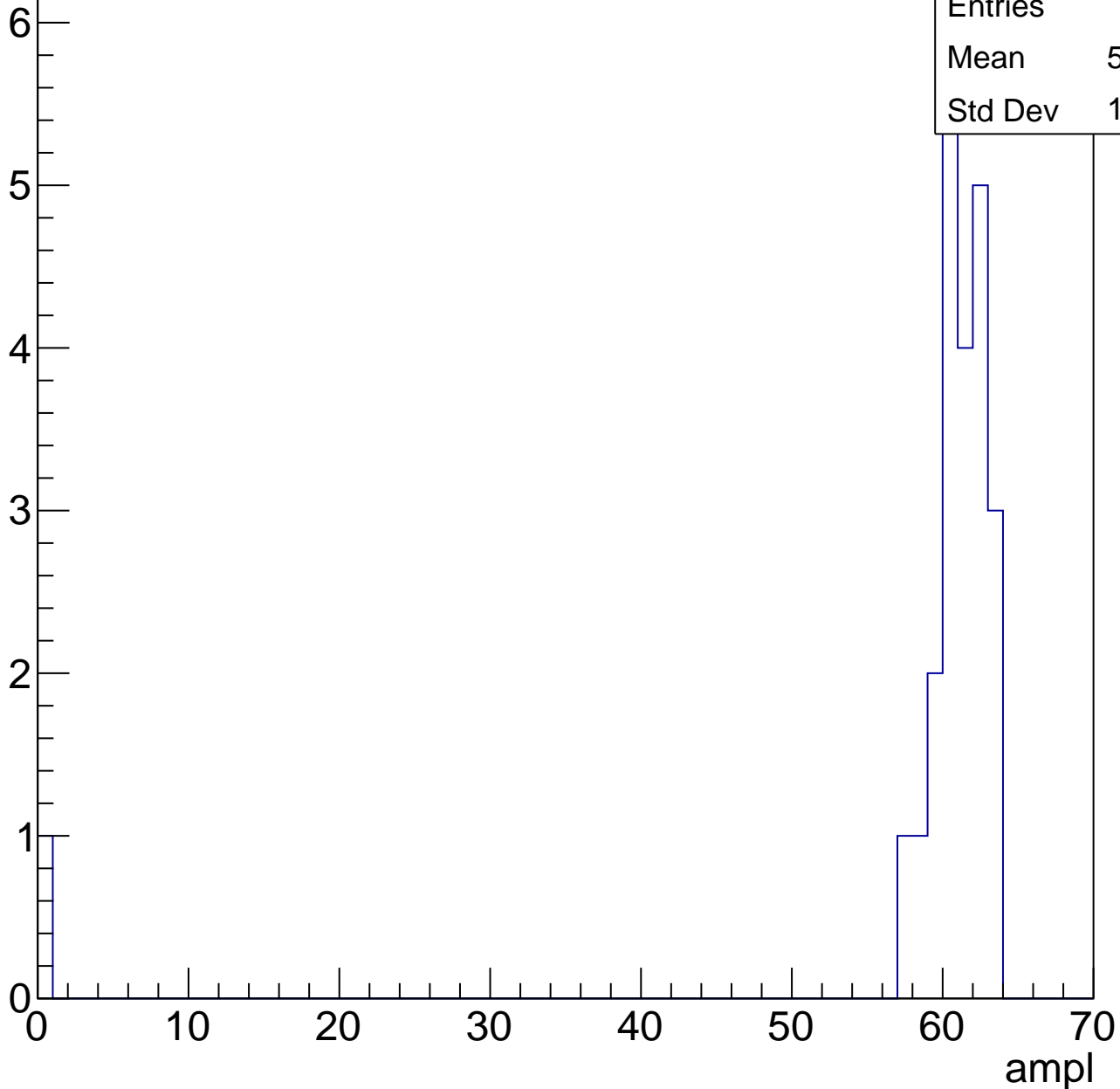


# B1L103S, U4-ch94, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 23    |
| Mean    | 58.09 |
| Std Dev | 12.48 |



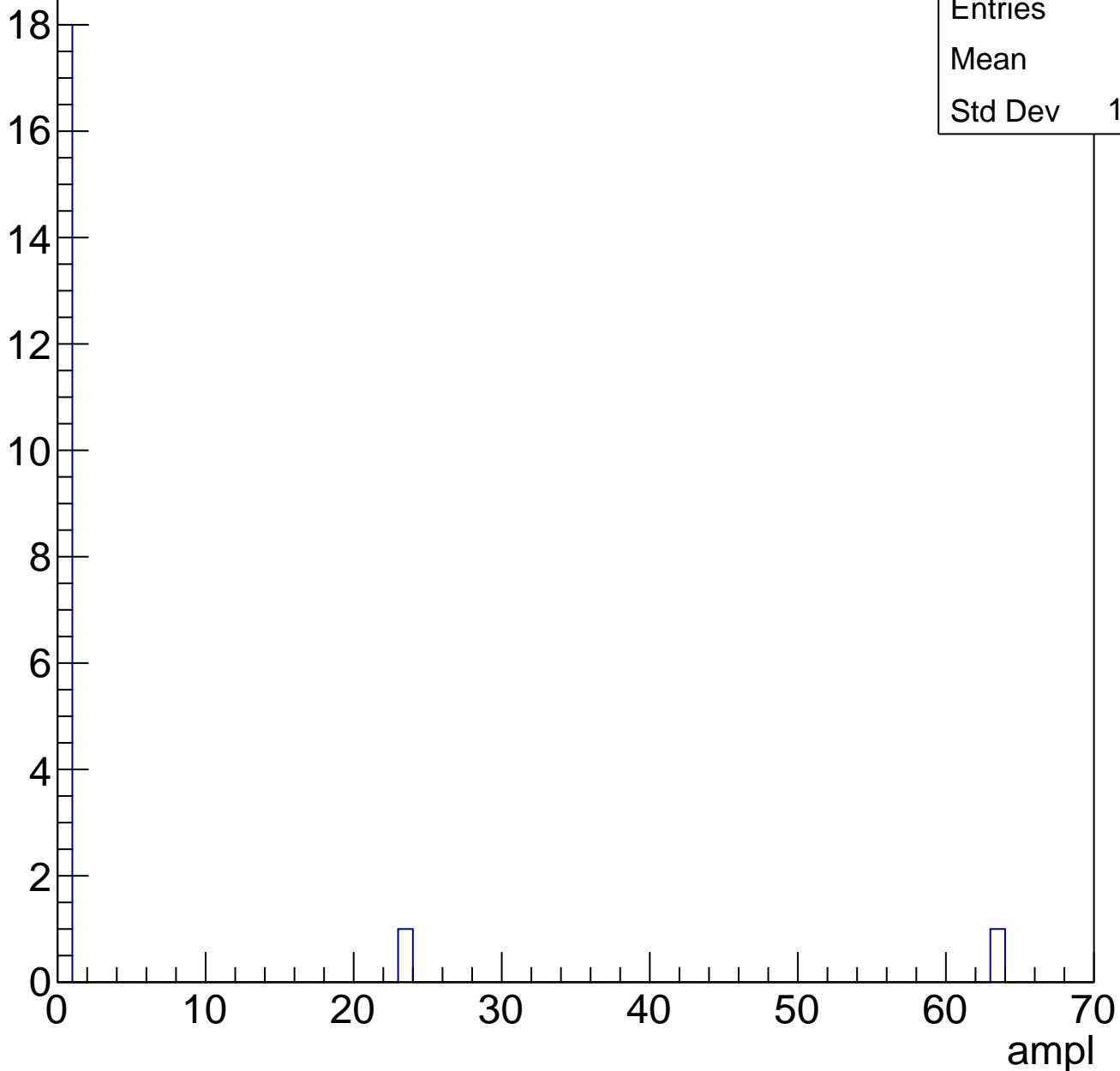


# B1L103S, U4-ch94, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 20    |
| Mean    | 4.3   |
| Std Dev | 14.37 |

Entry

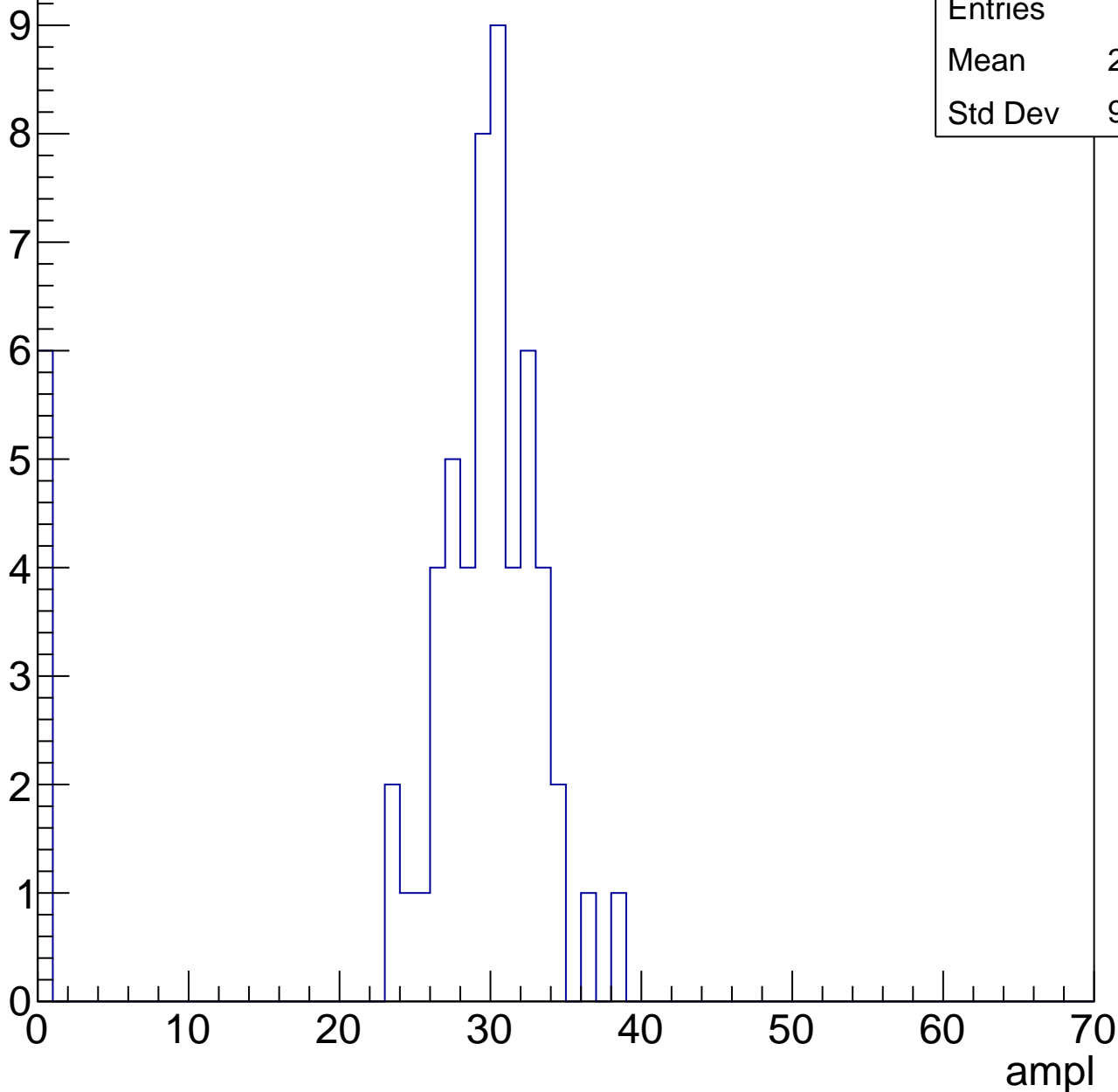


# B1L103S, U4-ch95, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 58    |
| Mean    | 26.52 |
| Std Dev | 9.455 |

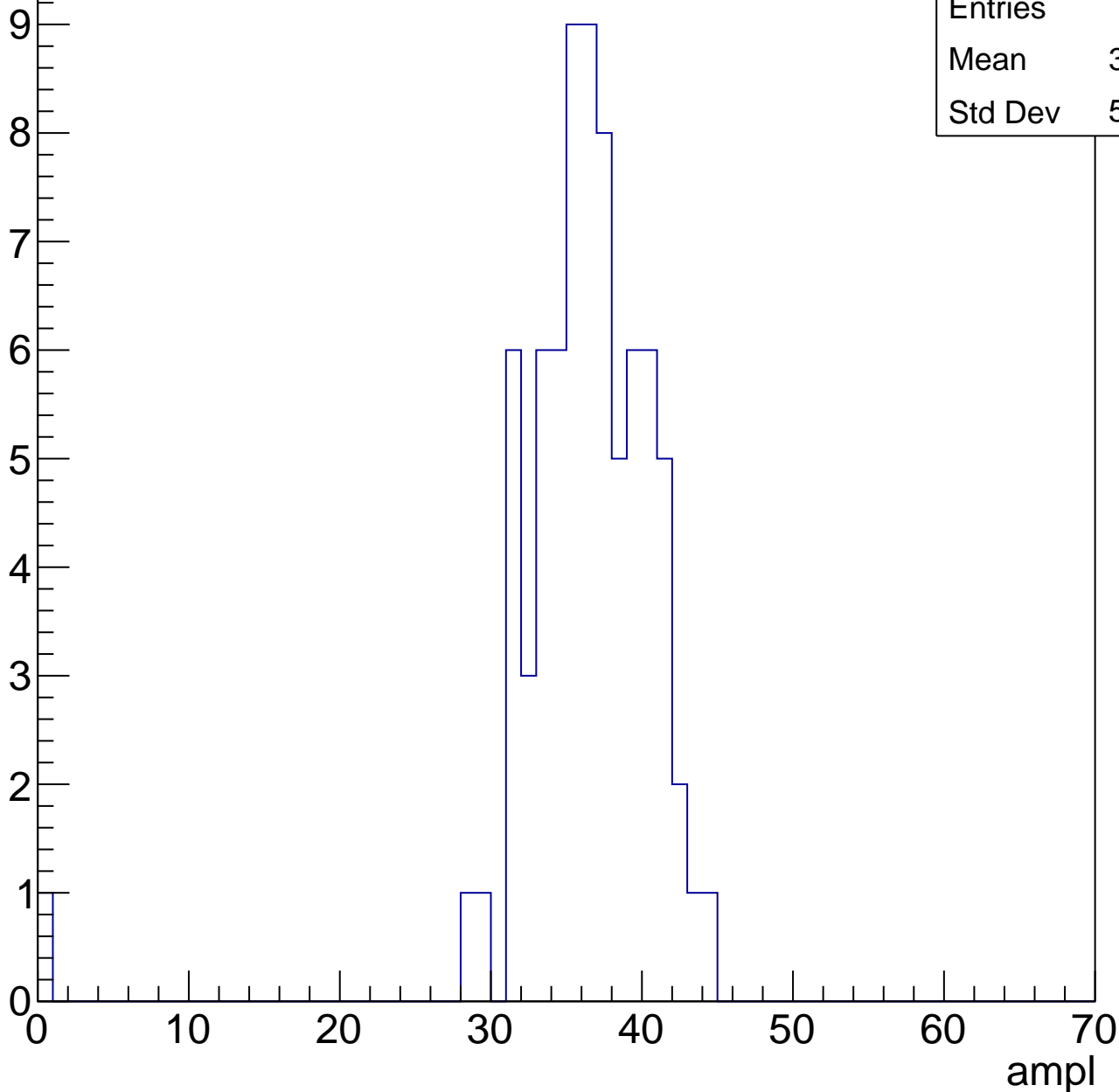


# B1L103S, U4-ch95, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 76    |
| Mean    | 35.74 |
| Std Dev | 5.352 |



# B1L103S, U4-ch95, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 92    |
| Mean    | 37.37 |
| Std Dev | 15.52 |

Entry

12

10

8

6

4

2

0

0

10

20

30

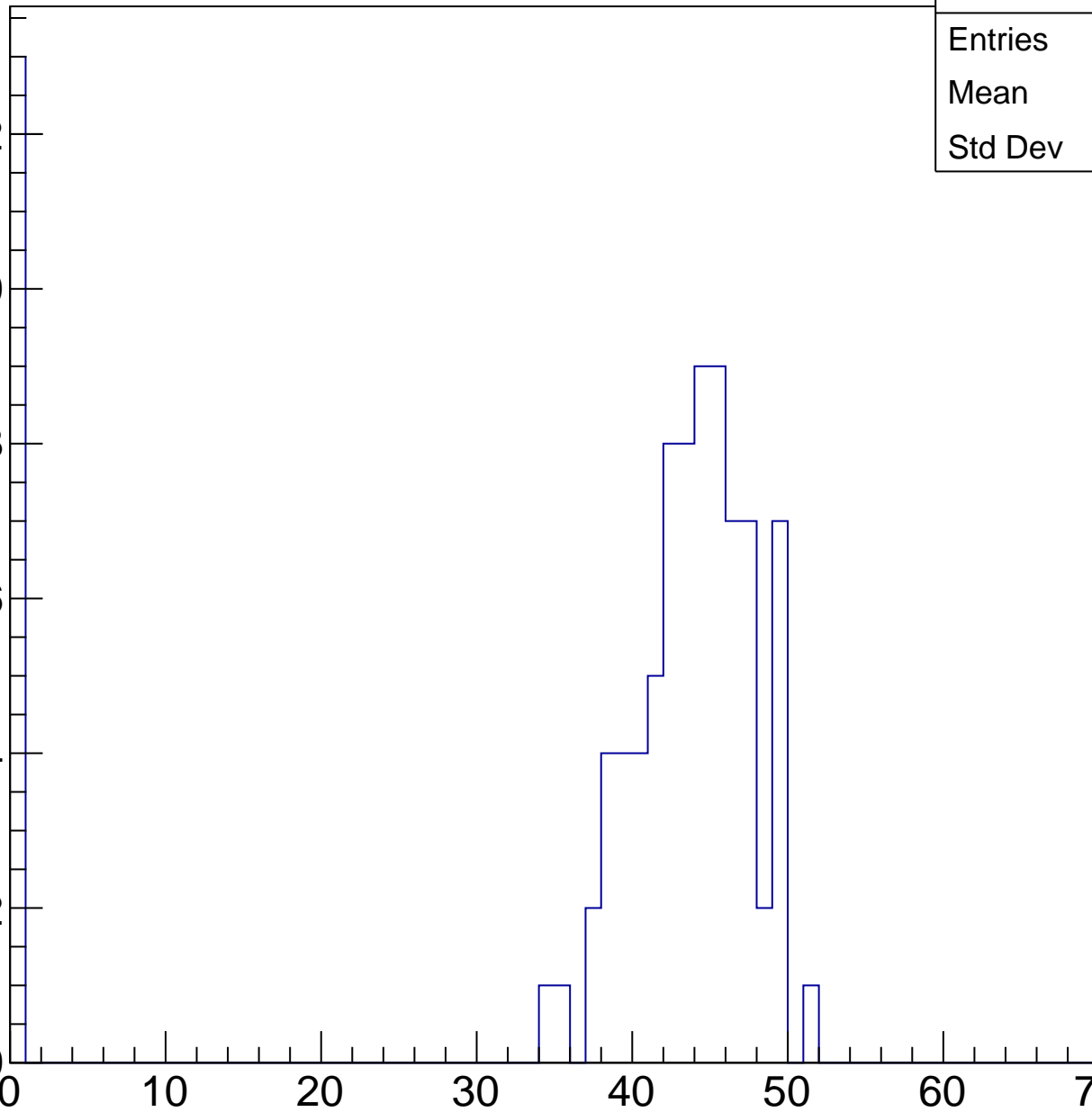
40

50

60

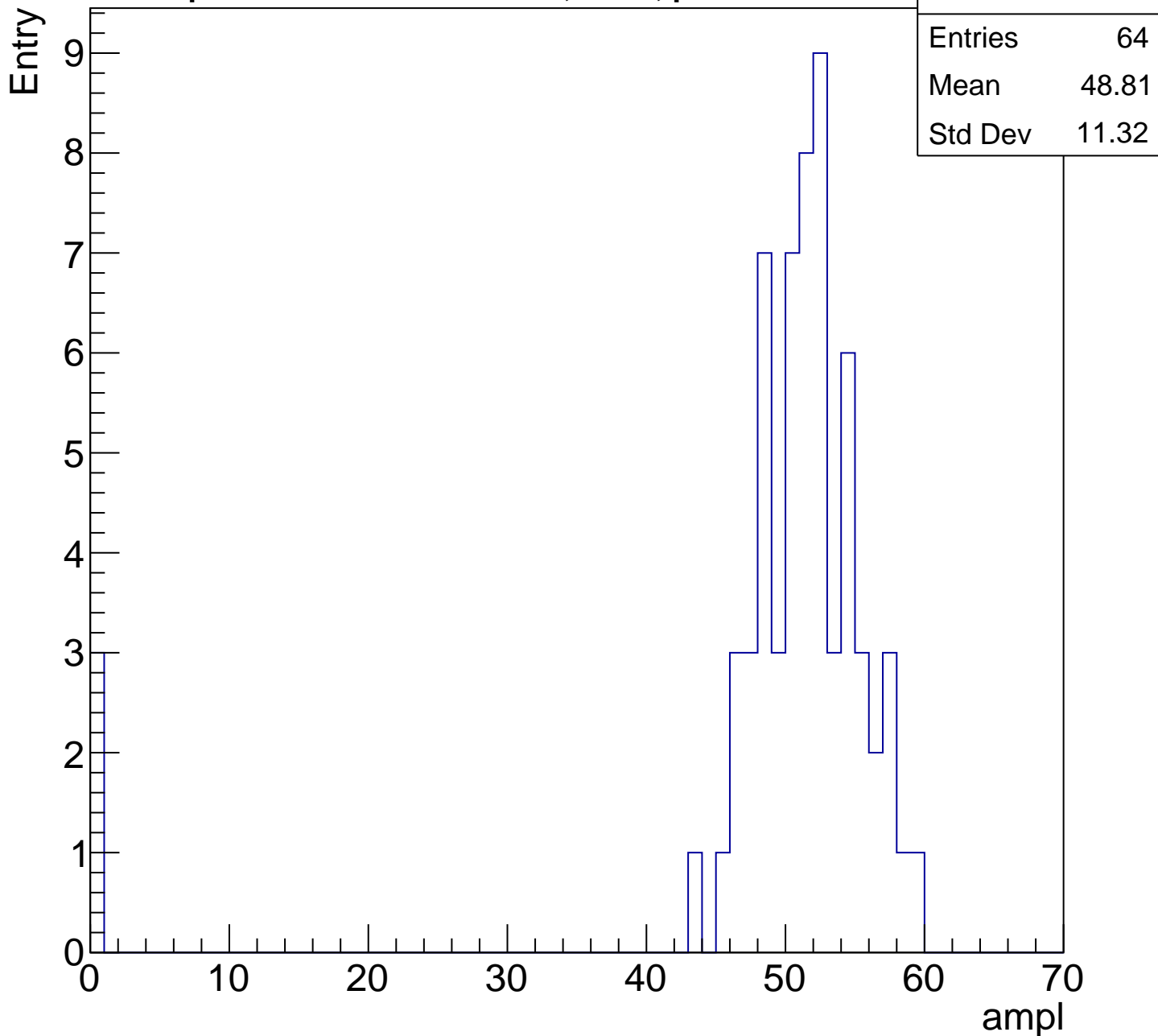
70

ampl



# B1L103S, U4-ch95, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

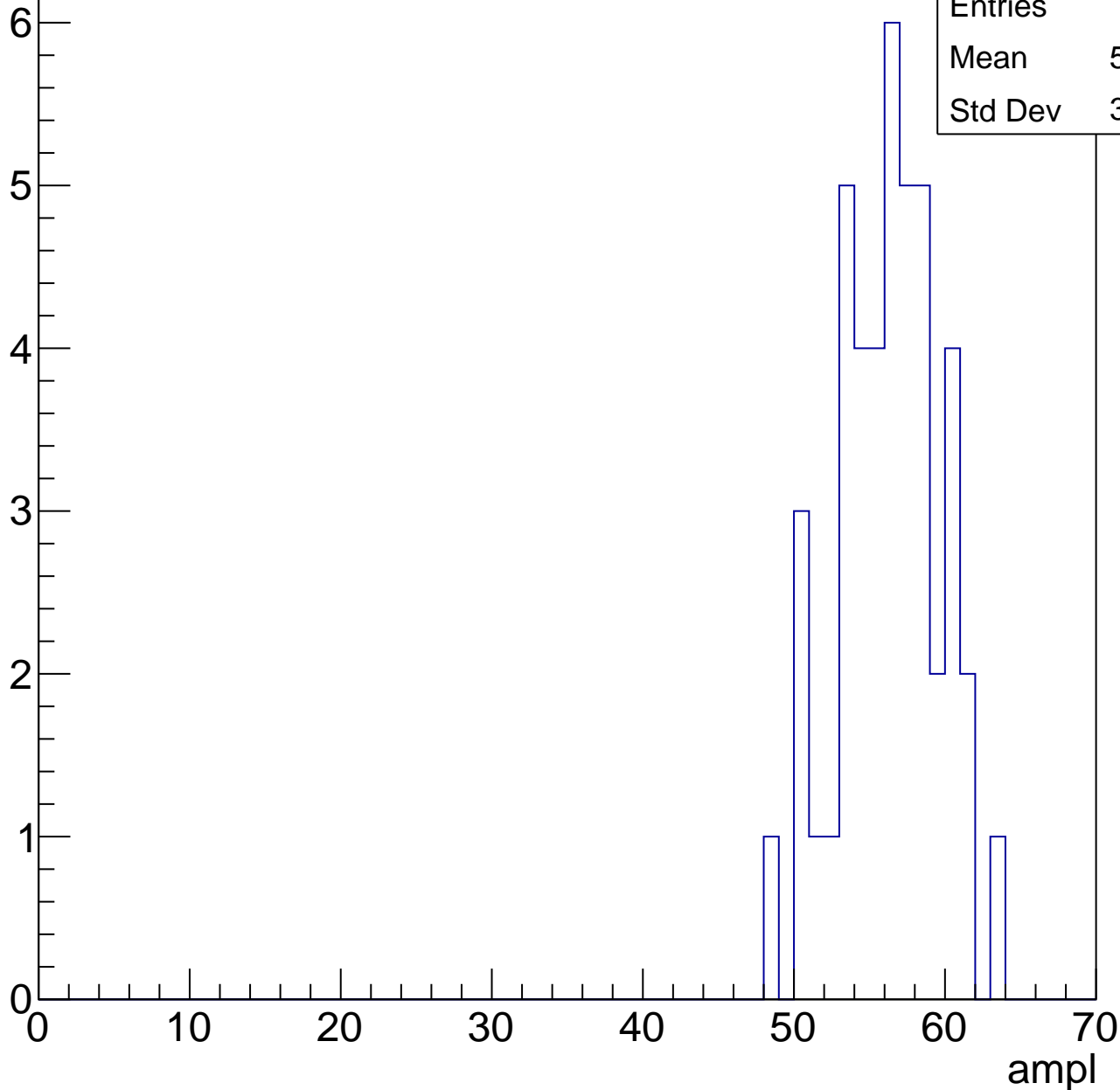


# B1L103S, U4-ch95, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 44    |
| Mean    | 55.82 |
| Std Dev | 3.312 |

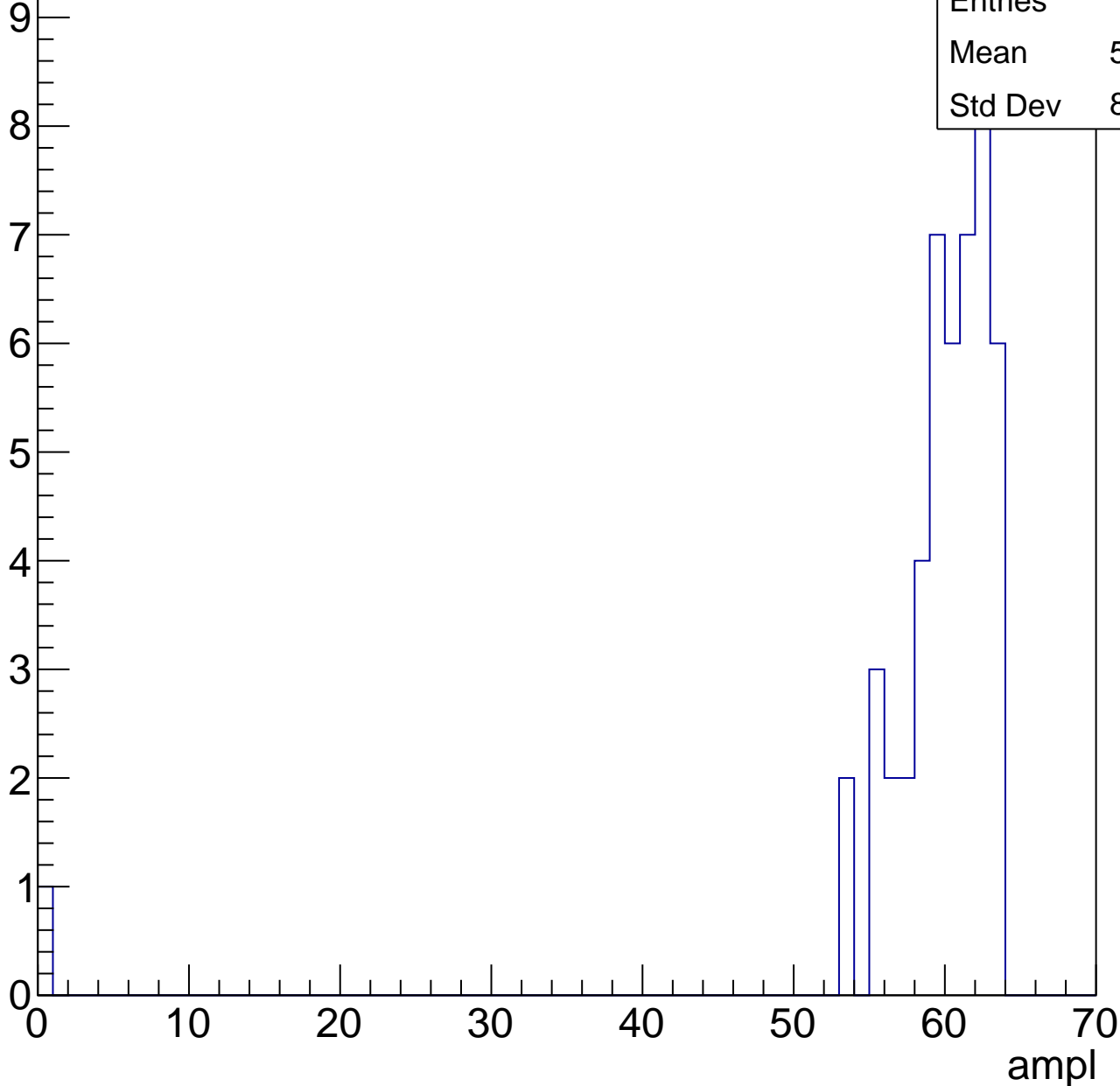


# B1L103S, U4-ch95, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 49    |
| Mean    | 58.47 |
| Std Dev | 8.839 |



# B1L103S, U4-ch95, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U4-ch95, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

|         |    |
|---------|----|
| Entries | 19 |
| Mean    | 0  |
| Std Dev | 0  |

# B1L103S, U4-ch96, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 98    |
| Mean    | 19.78 |
| Std Dev | 12.85 |

Entry

25  
20  
15  
10  
5  
0

0 10 20 30 40 50 60 70

ampl

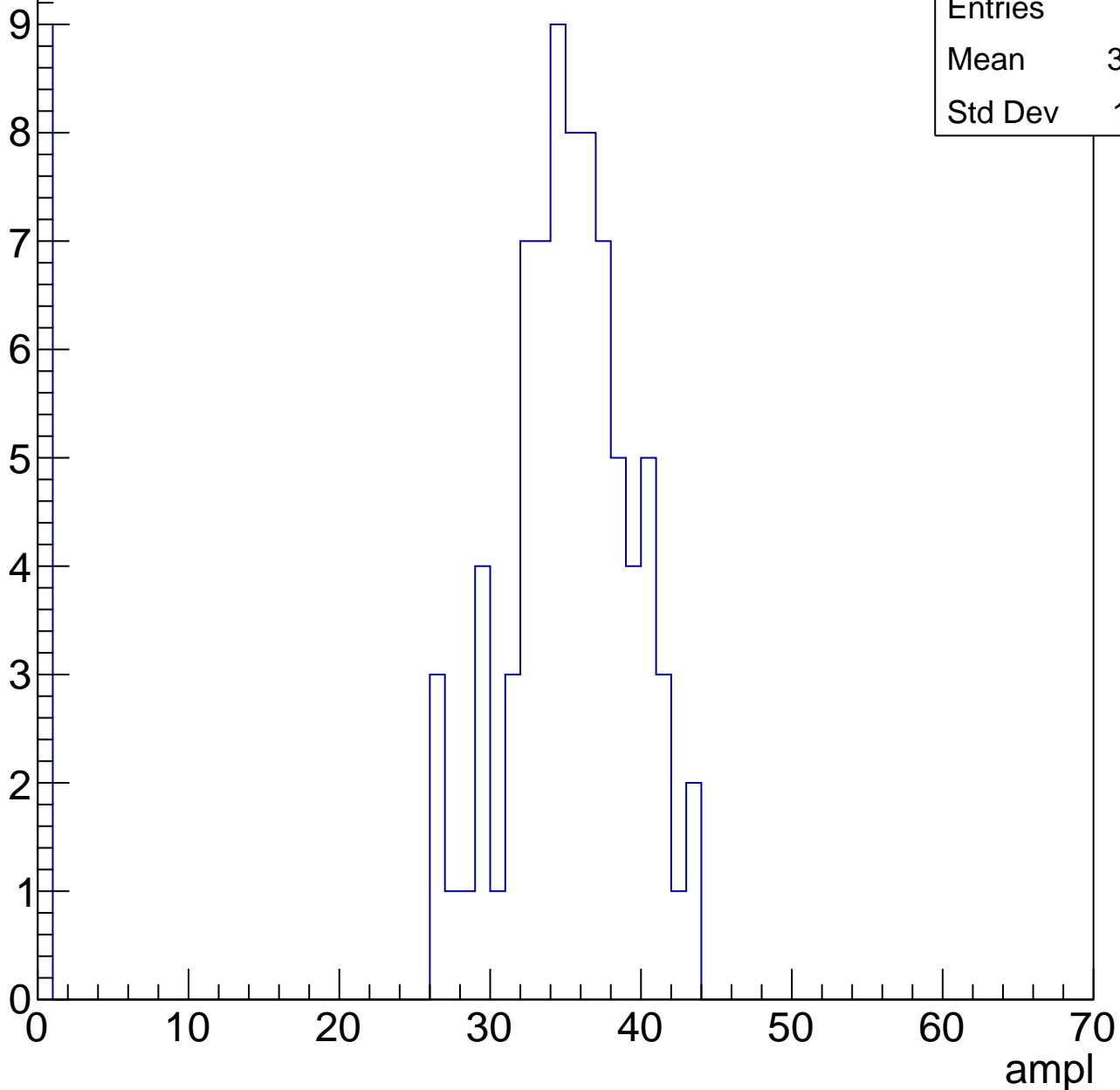
0 5 10 15 20 25

# B1L103S, U4-ch96, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 88    |
| Mean    | 31.33 |
| Std Dev | 11.21 |

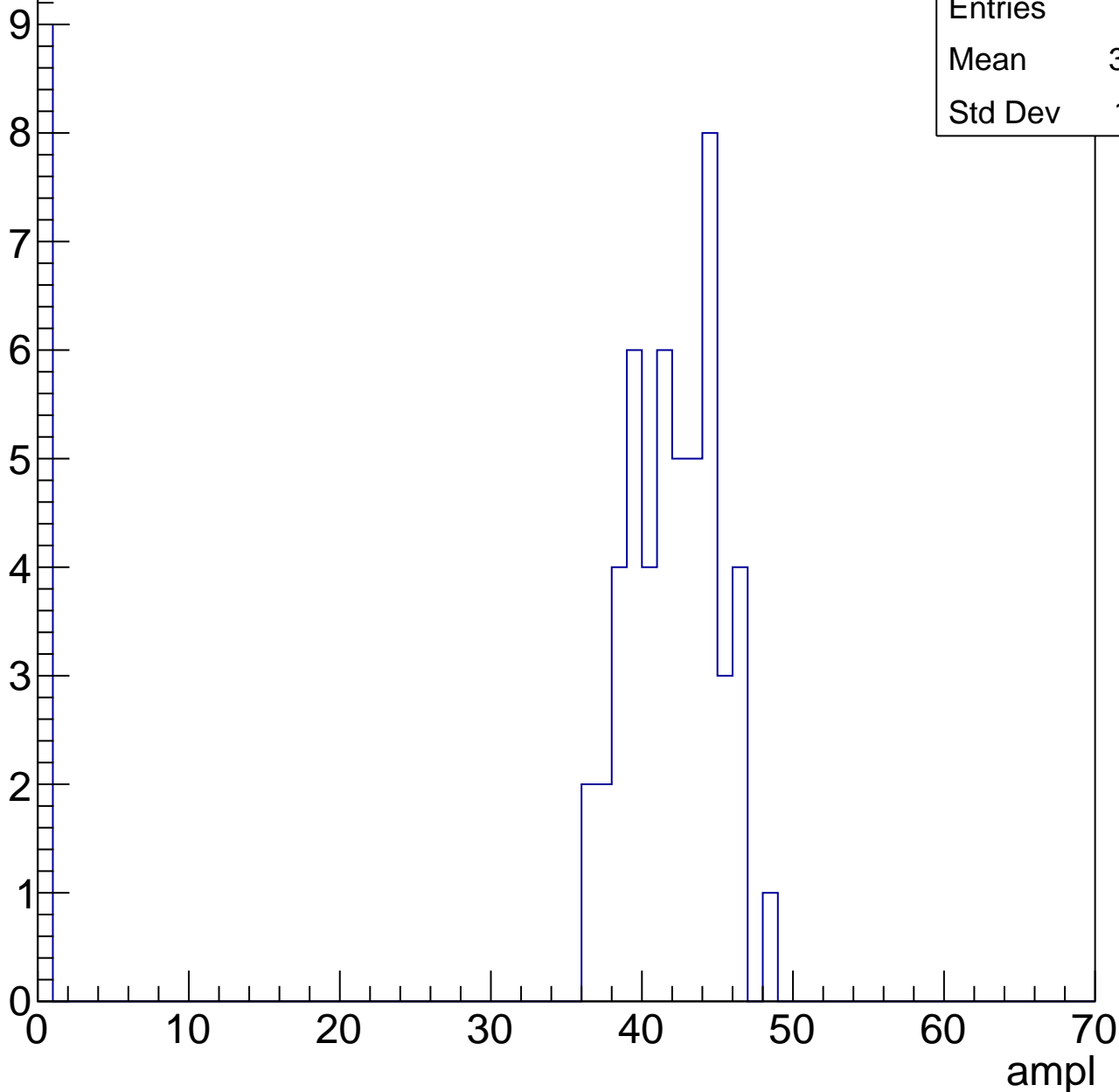


# B1L103S, U4-ch96, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 59    |
| Mean    | 35.29 |
| Std Dev | 15.21 |

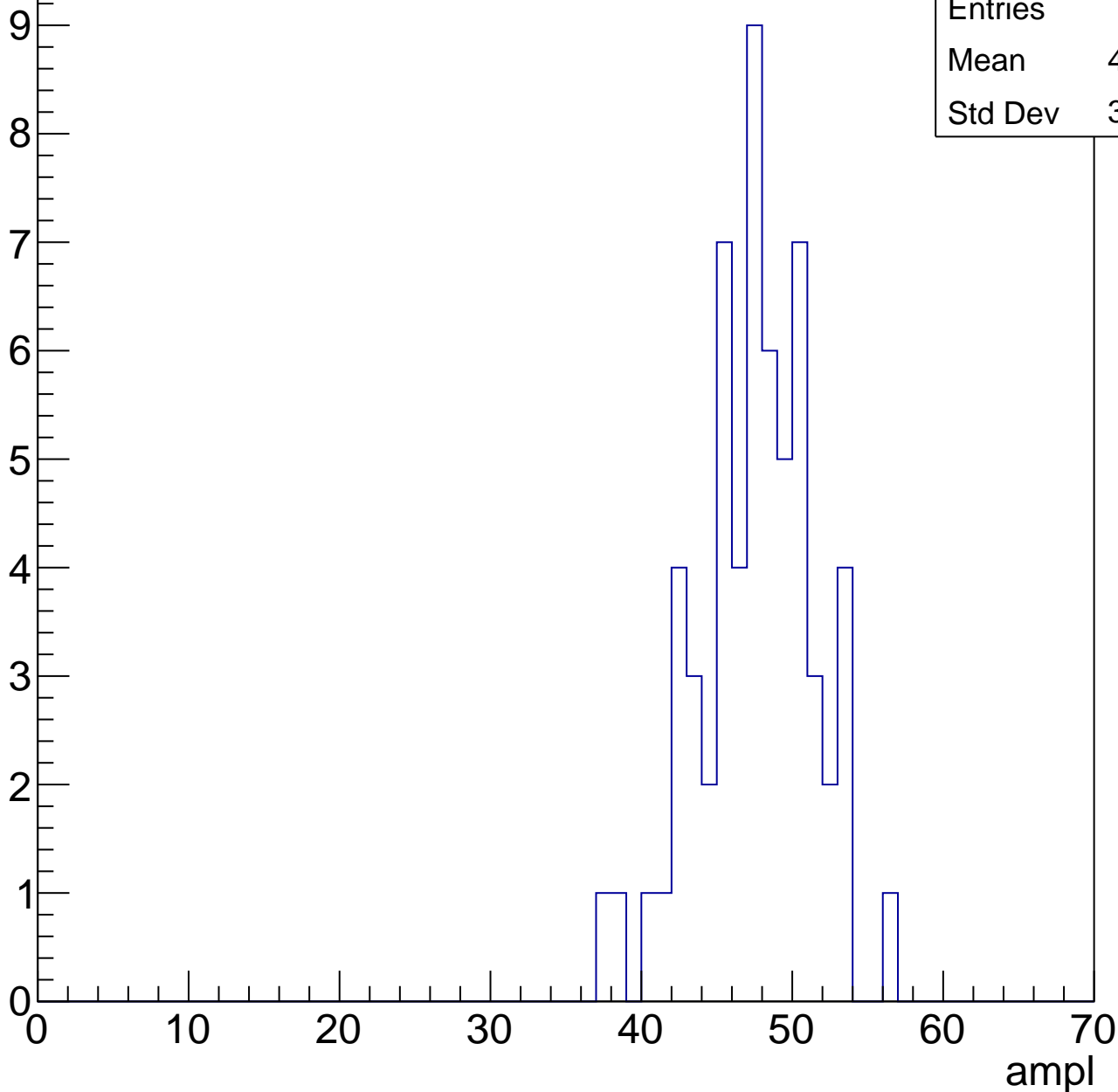


# B1L103S, U4-ch96, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 61    |
| Mean    | 47.07 |
| Std Dev | 3.789 |

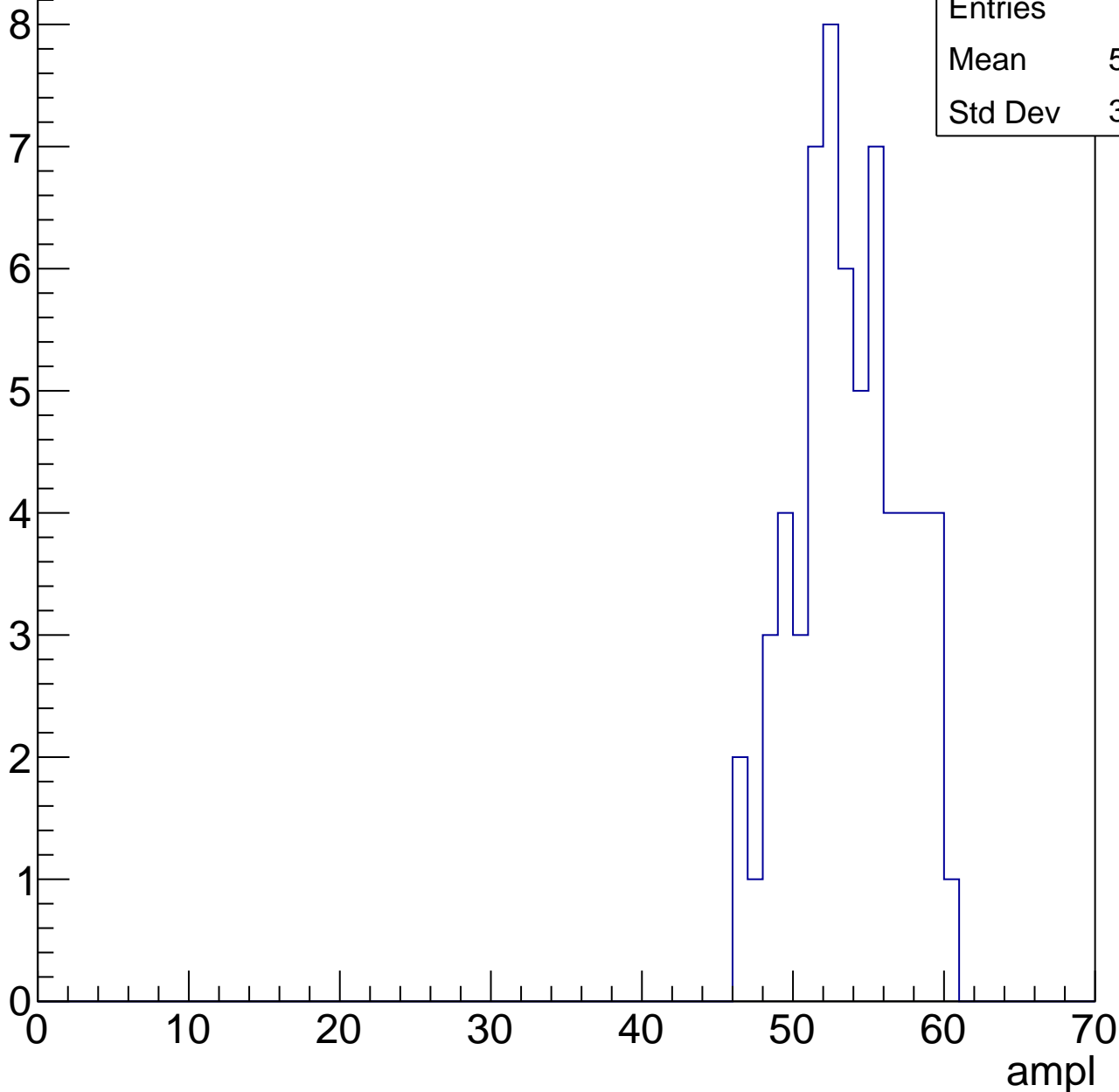


# B1L103S, U4-ch96, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 63    |
| Mean    | 53.25 |
| Std Dev | 3.469 |



# B1L103S, U4-ch96, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

6

5

4

3

2

1

0

0

10

20

30

40

50

60

70

ampl

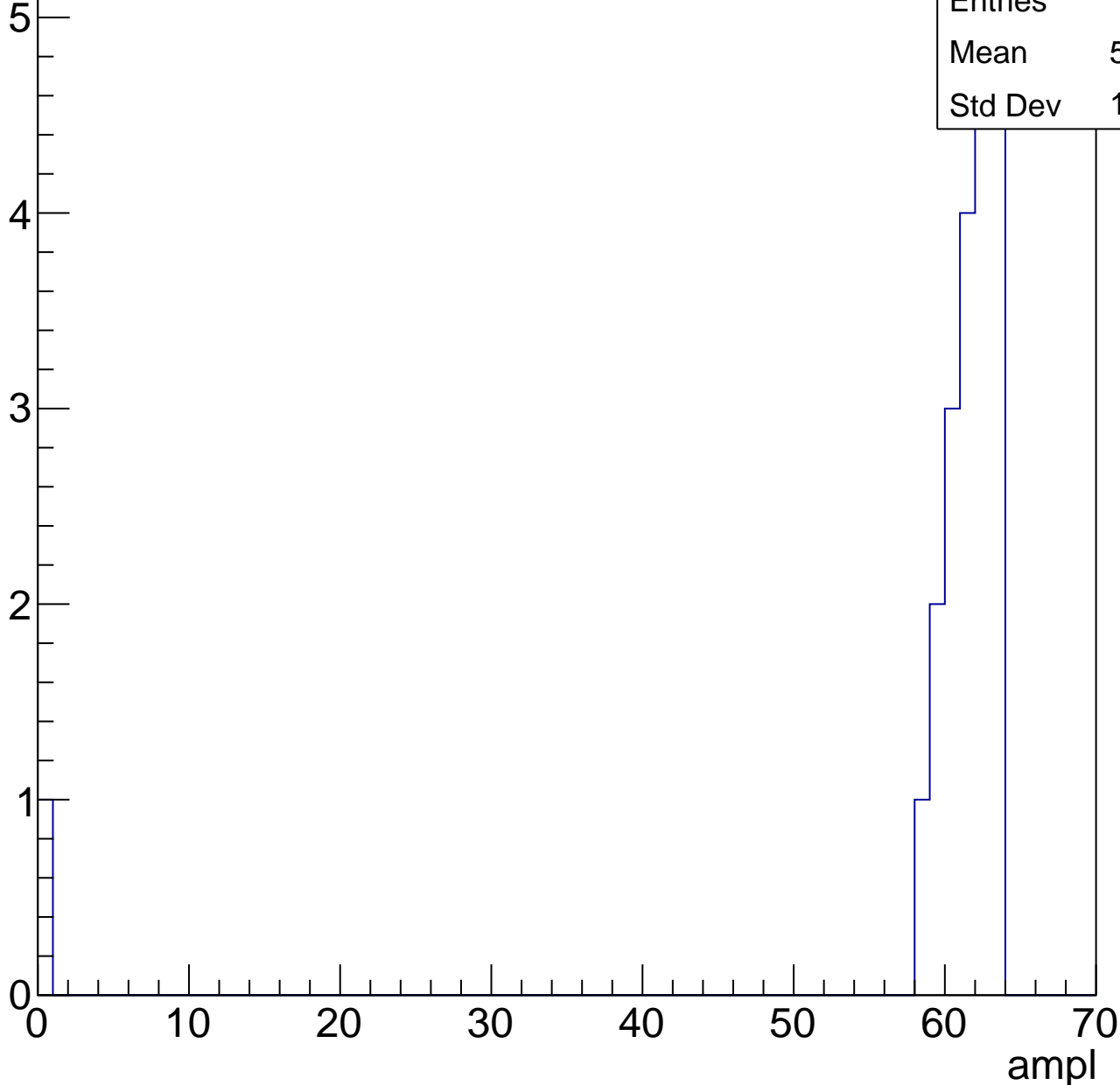
|         |       |
|---------|-------|
| Entries | 51    |
| Mean    | 58.49 |
| Std Dev | 3.096 |

# B1L103S, U4-ch96, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 21    |
| Mean    | 58.33 |
| Std Dev | 13.12 |





# B1L103S, U4-ch96, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

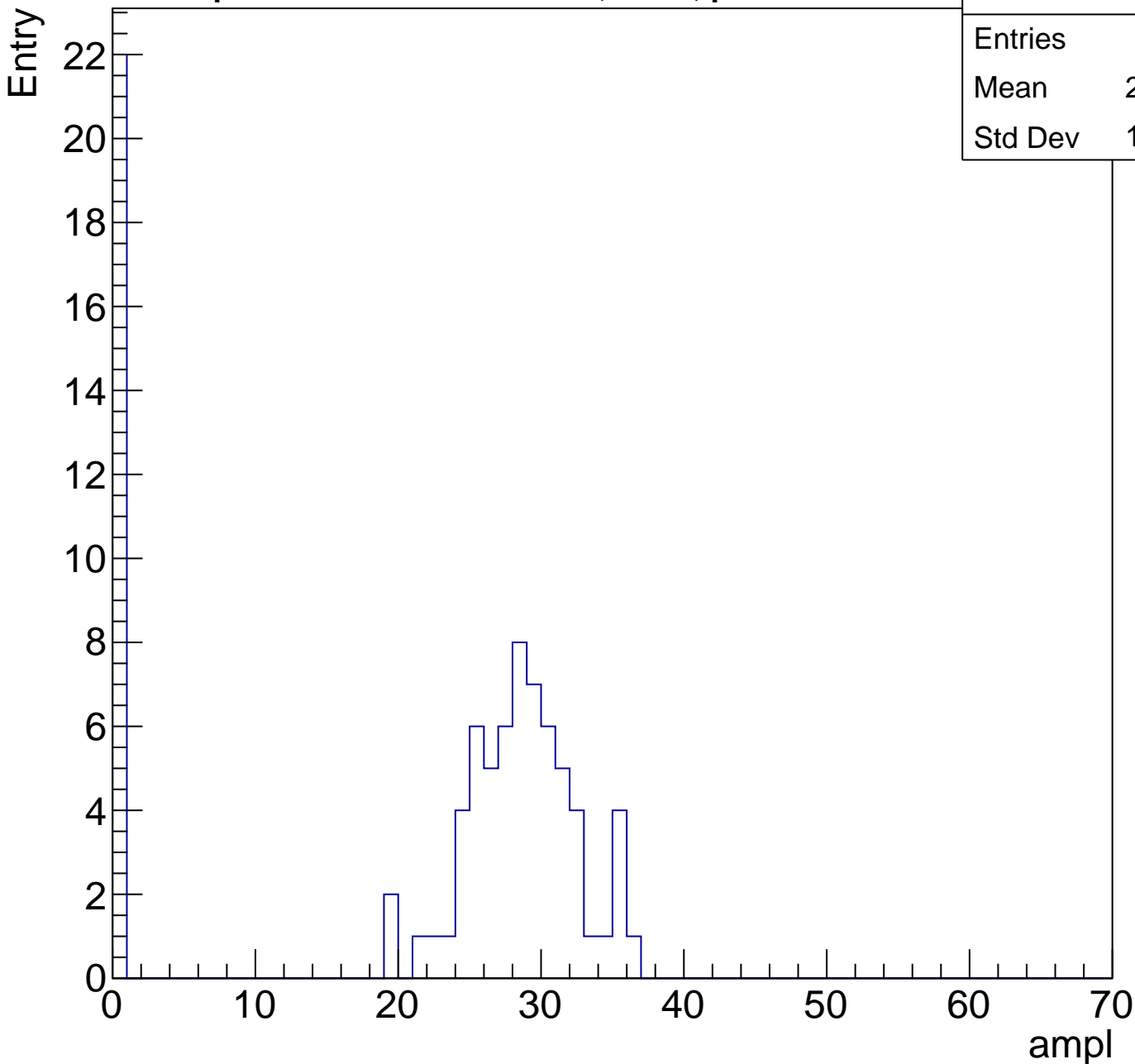
ampl

|         |    |
|---------|----|
| Entries | 19 |
| Mean    | 0  |
| Std Dev | 0  |

# B1L103S, U4-ch97, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 85    |
| Mean    | 20.88 |
| Std Dev | 12.75 |



# B1L103S, U4-ch97, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 78    |
| Mean    | 30.01 |
| Std Dev | 12.66 |

Entry

10

8

6

4

2

0

0

10

20

30

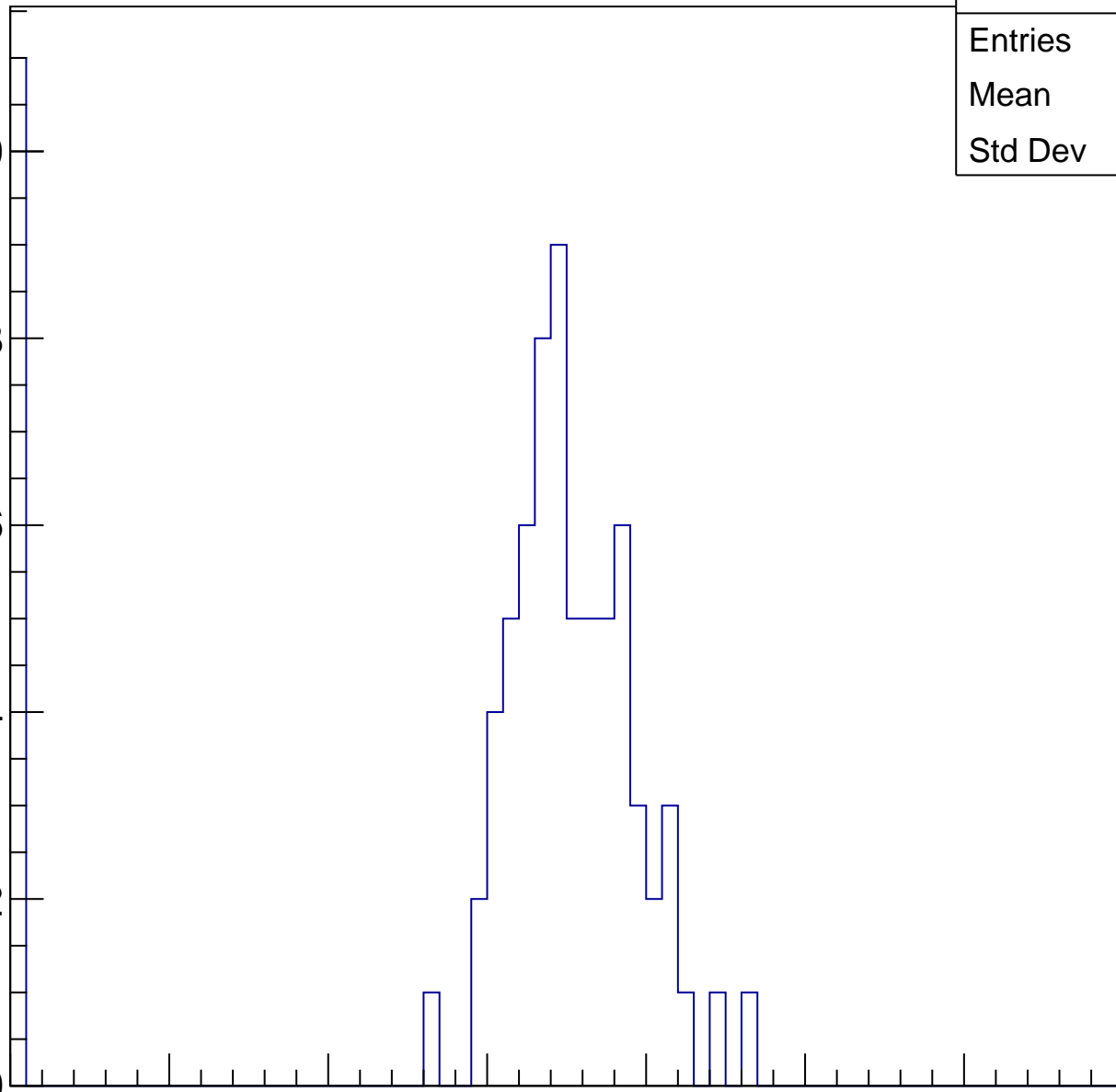
40

50

60

70

ampl

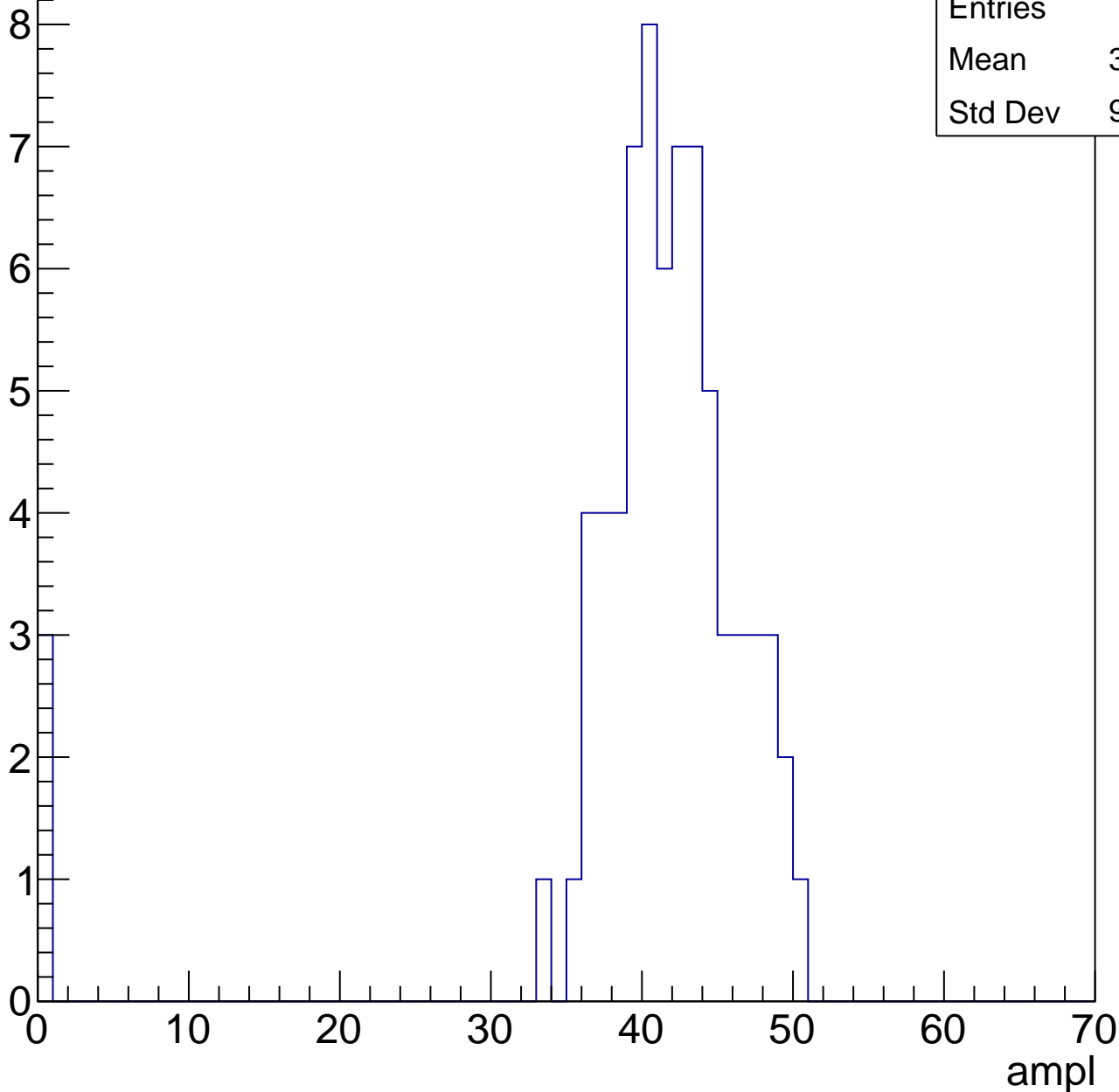


# B1L103S, U4-ch97, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 72    |
| Mean    | 39.89 |
| Std Dev | 9.096 |

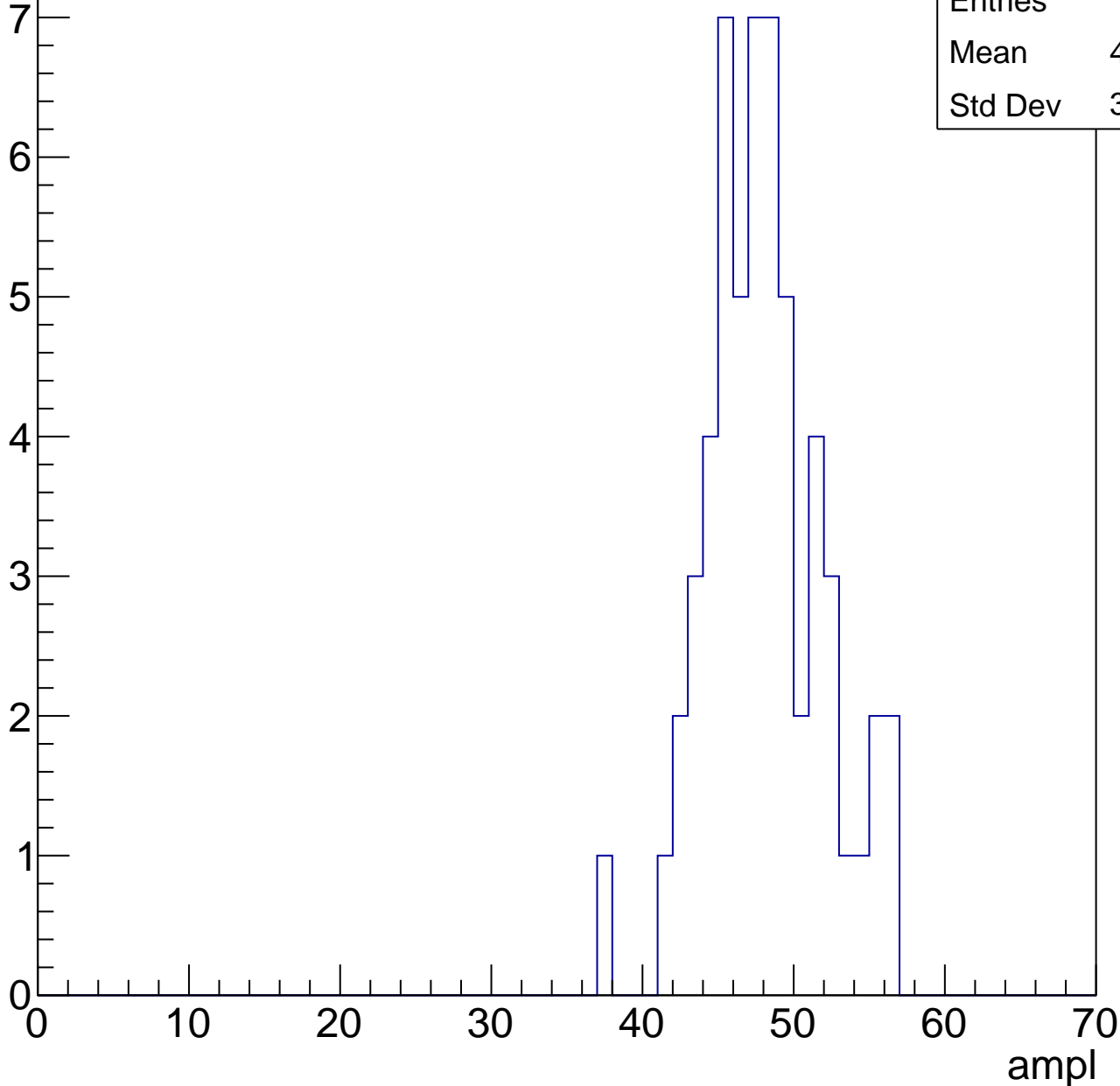


# B1L103S, U4-ch97, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 57    |
| Mean    | 47.56 |
| Std Dev | 3.848 |

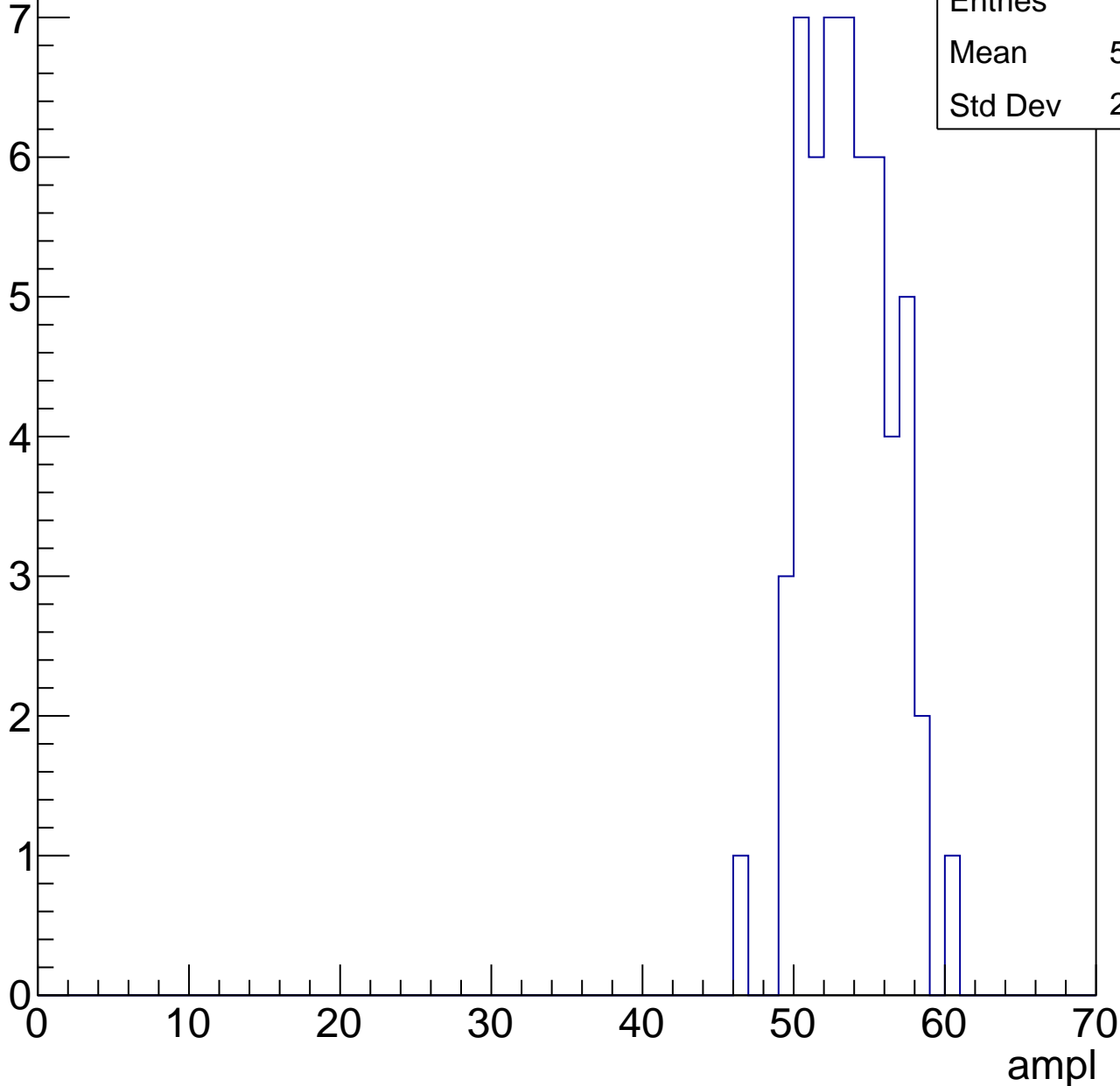


# B1L103S, U4-ch97, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 55    |
| Mean    | 53.15 |
| Std Dev | 2.812 |

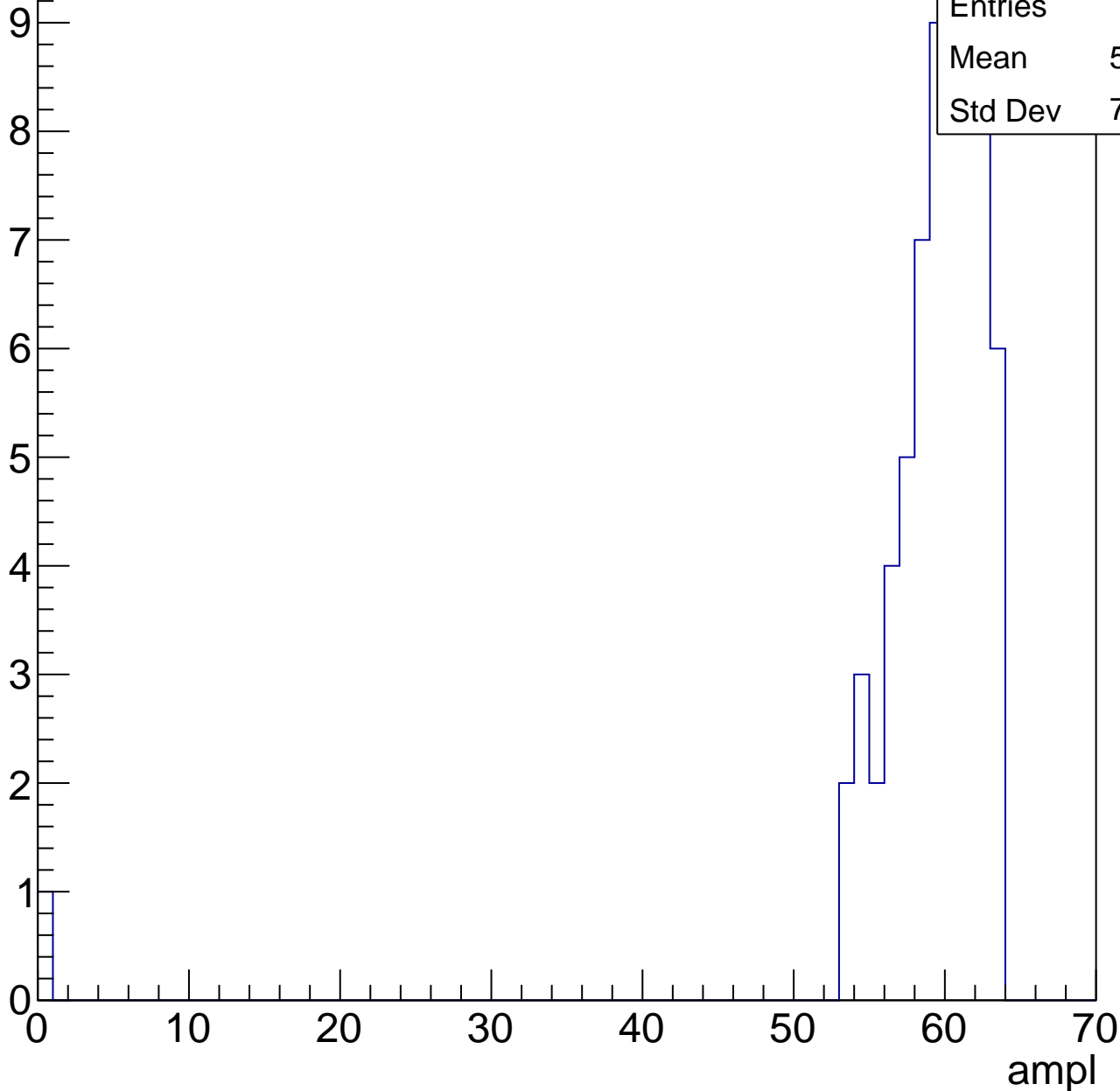


# B1L103S, U4-ch97, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

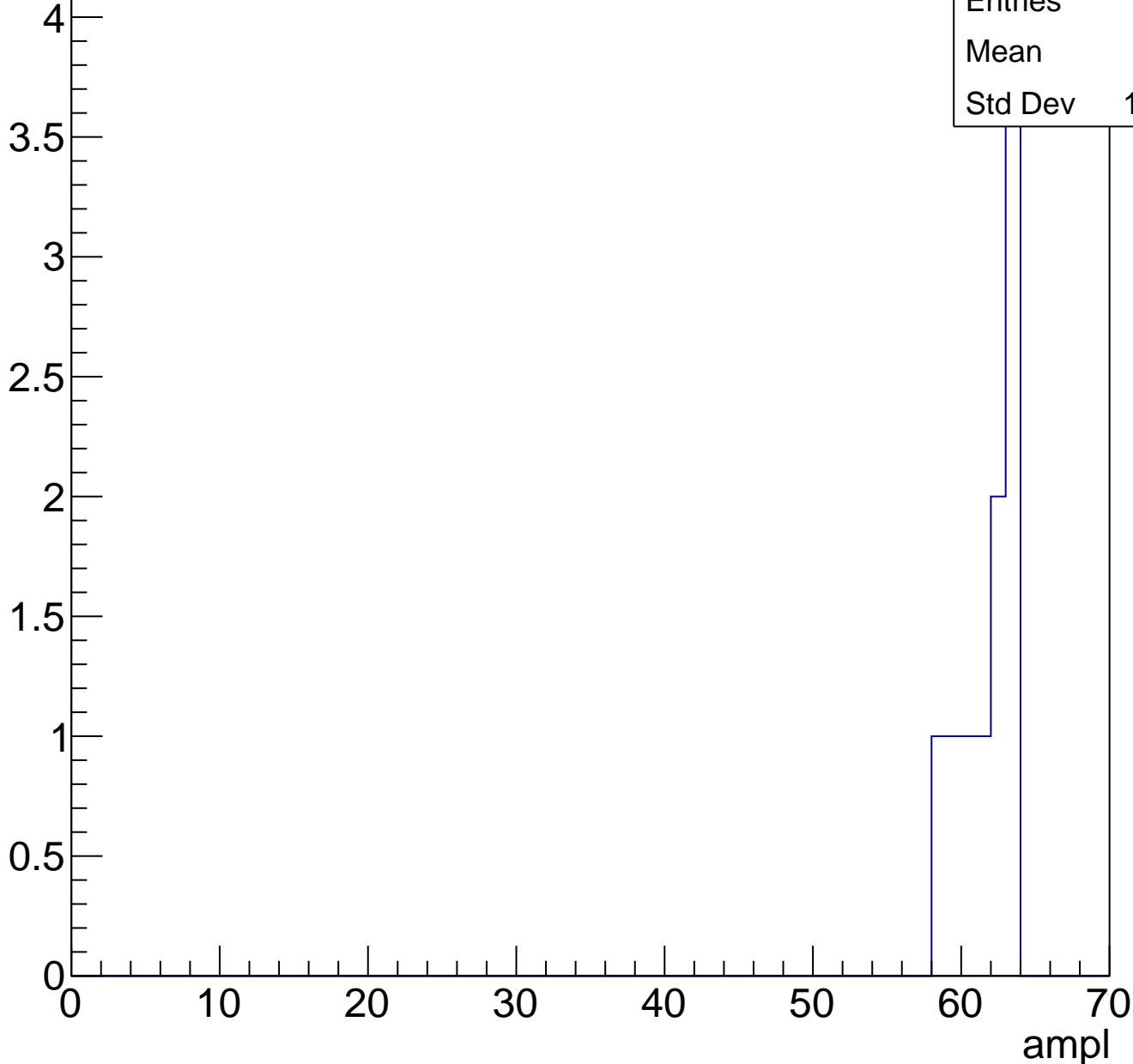
|         |       |
|---------|-------|
| Entries | 64    |
| Mean    | 58.23 |
| Std Dev | 7.804 |



# B1L103S, U4-ch97, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



|         |       |
|---------|-------|
| Entries | 10    |
| Mean    | 61.4  |
| Std Dev | 1.744 |



# B1L103S, U4-ch97, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



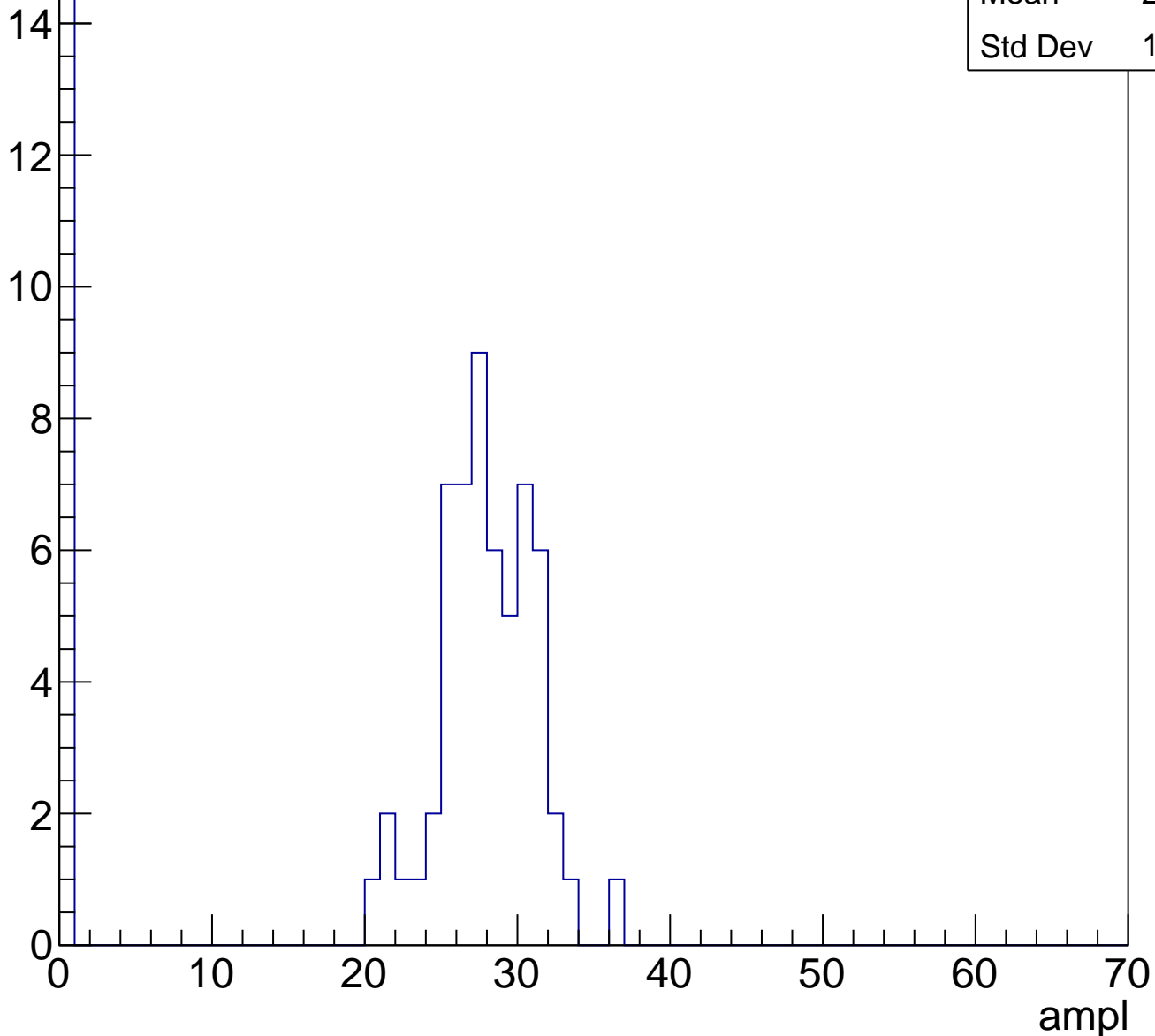
|         |    |
|---------|----|
| Entries | 19 |
| Mean    | 0  |
| Std Dev | 0  |

# B1L103S, U4-ch98, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 73    |
| Mean    | 21.88 |
| Std Dev | 11.46 |

Entry

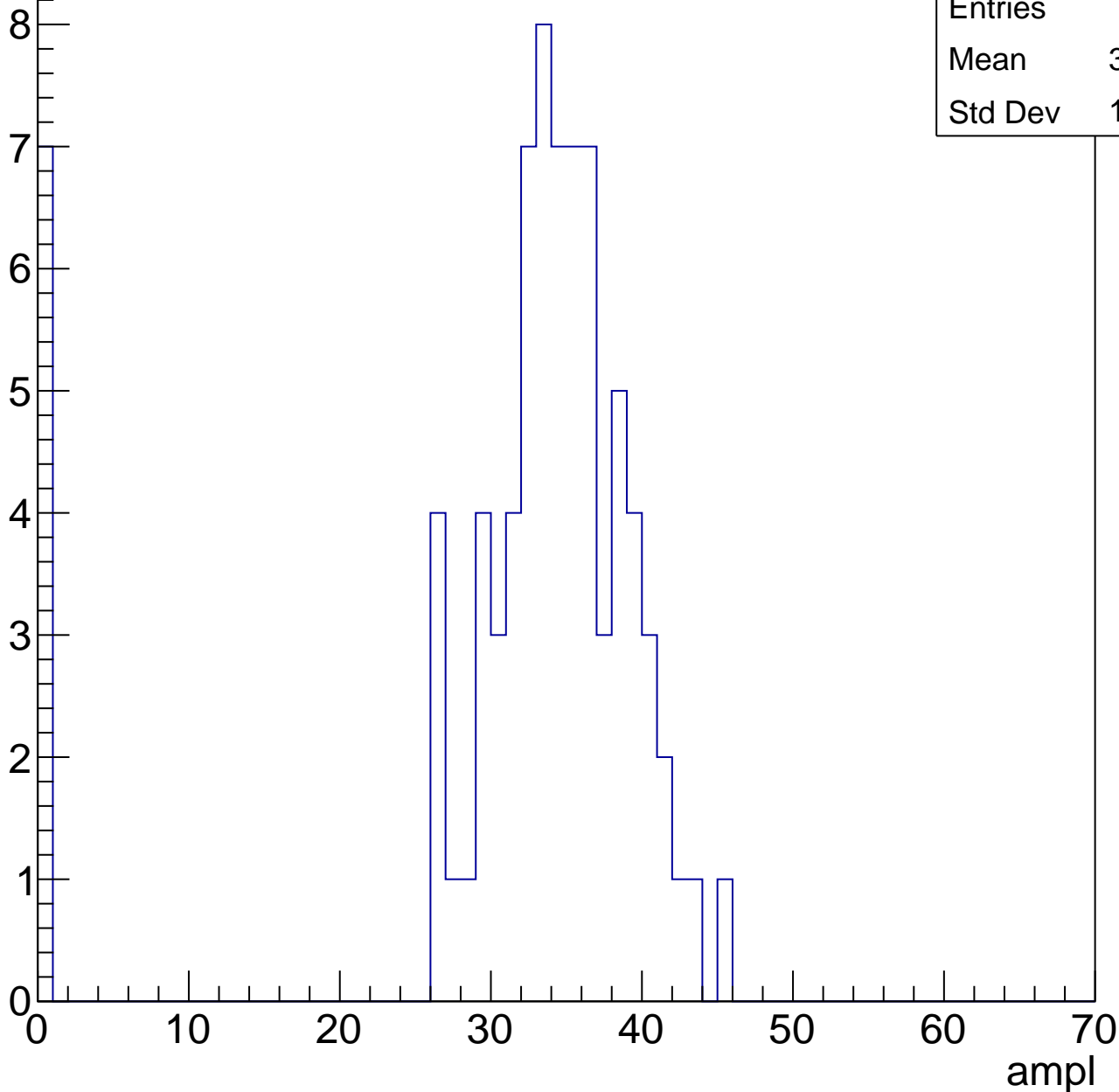


# B1L103S, U4-ch98, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 80    |
| Mean    | 31.26 |
| Std Dev | 10.47 |

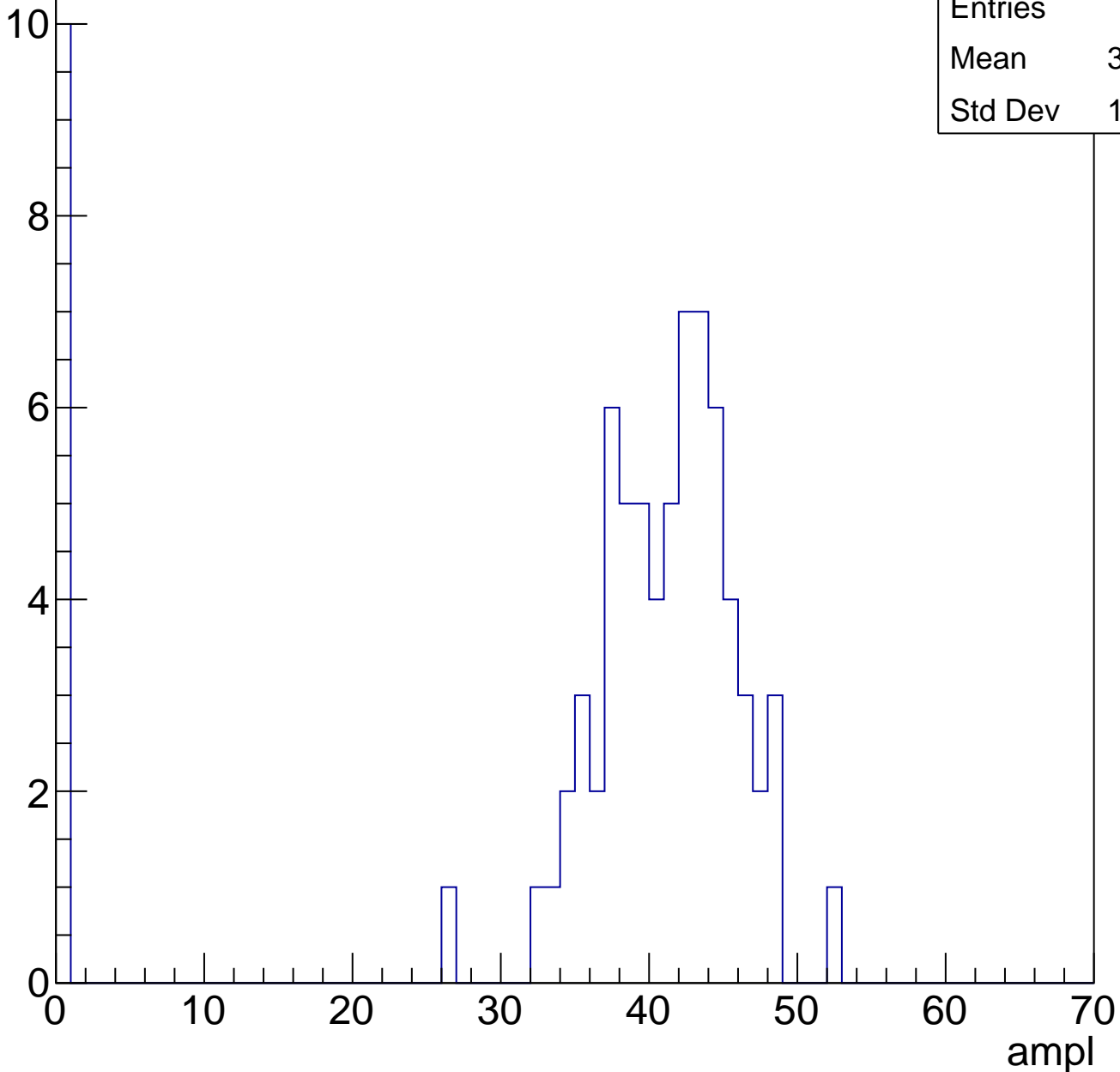


# B1L103S, U4-ch98, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 78    |
| Mean    | 35.58 |
| Std Dev | 14.27 |

Entry

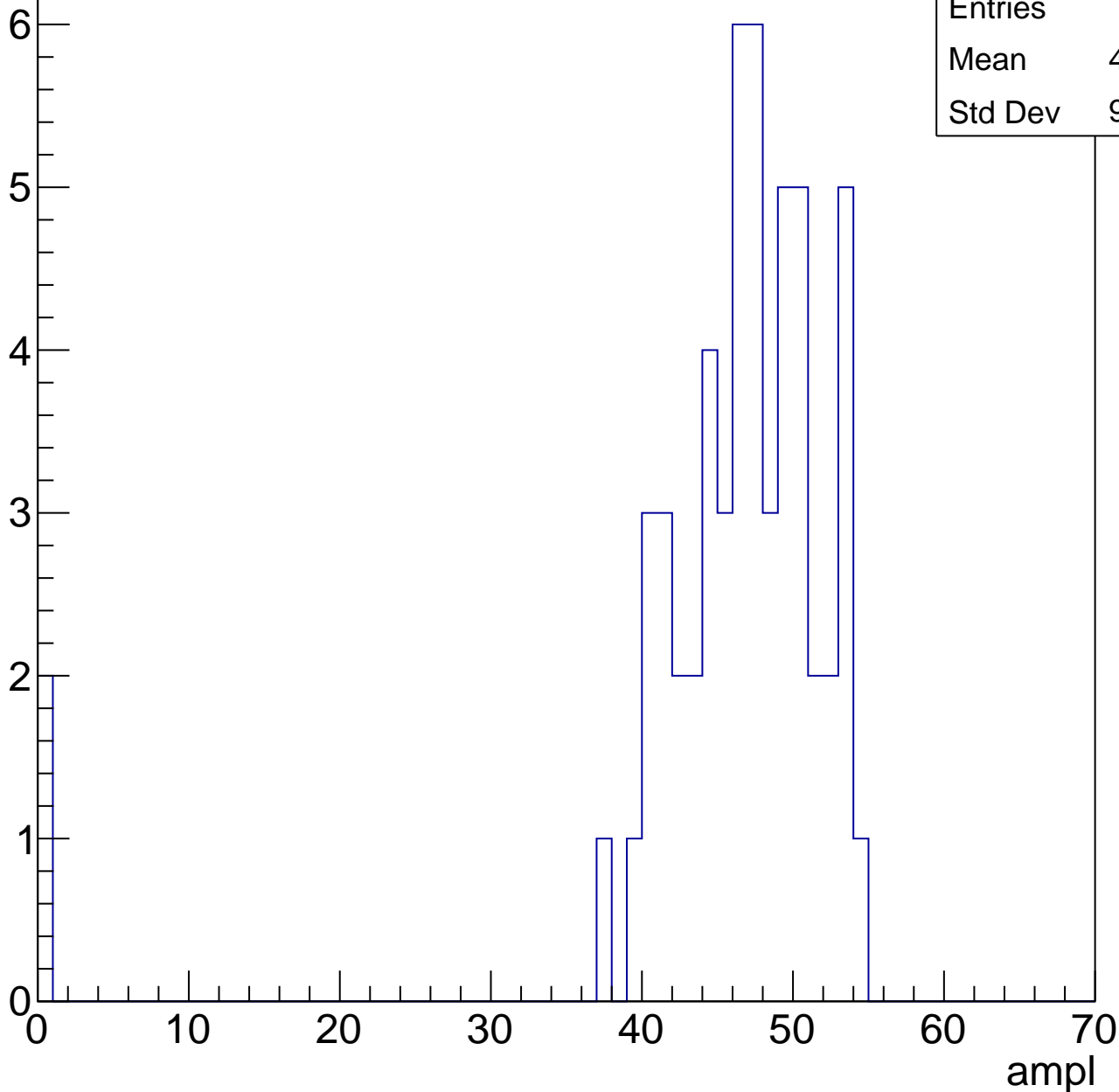


# B1L103S, U4-ch98, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 56    |
| Mean    | 45.04 |
| Std Dev | 9.577 |

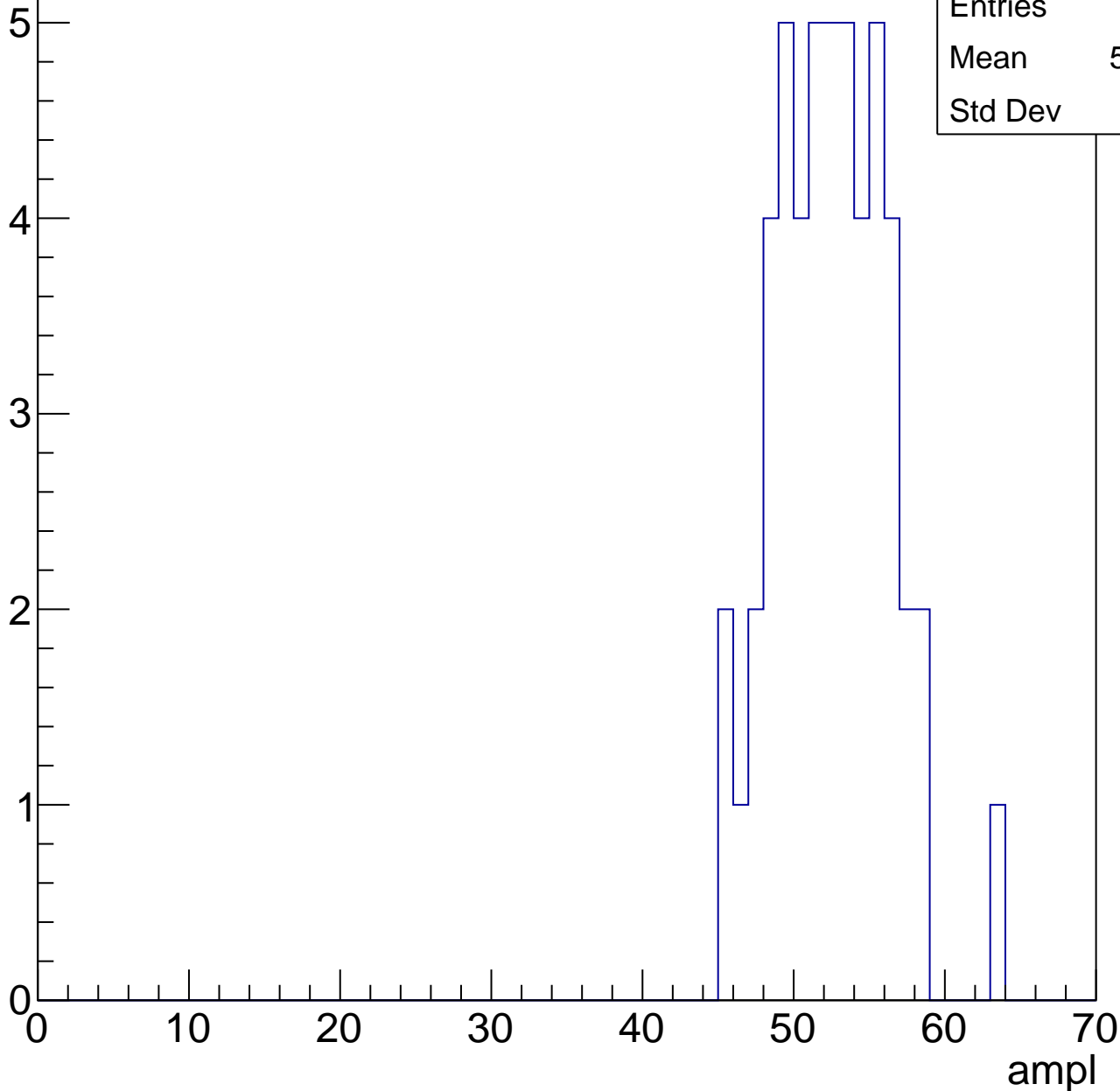


# B1L103S, U4-ch98, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 51    |
| Mean    | 52.06 |
| Std Dev | 3.67  |

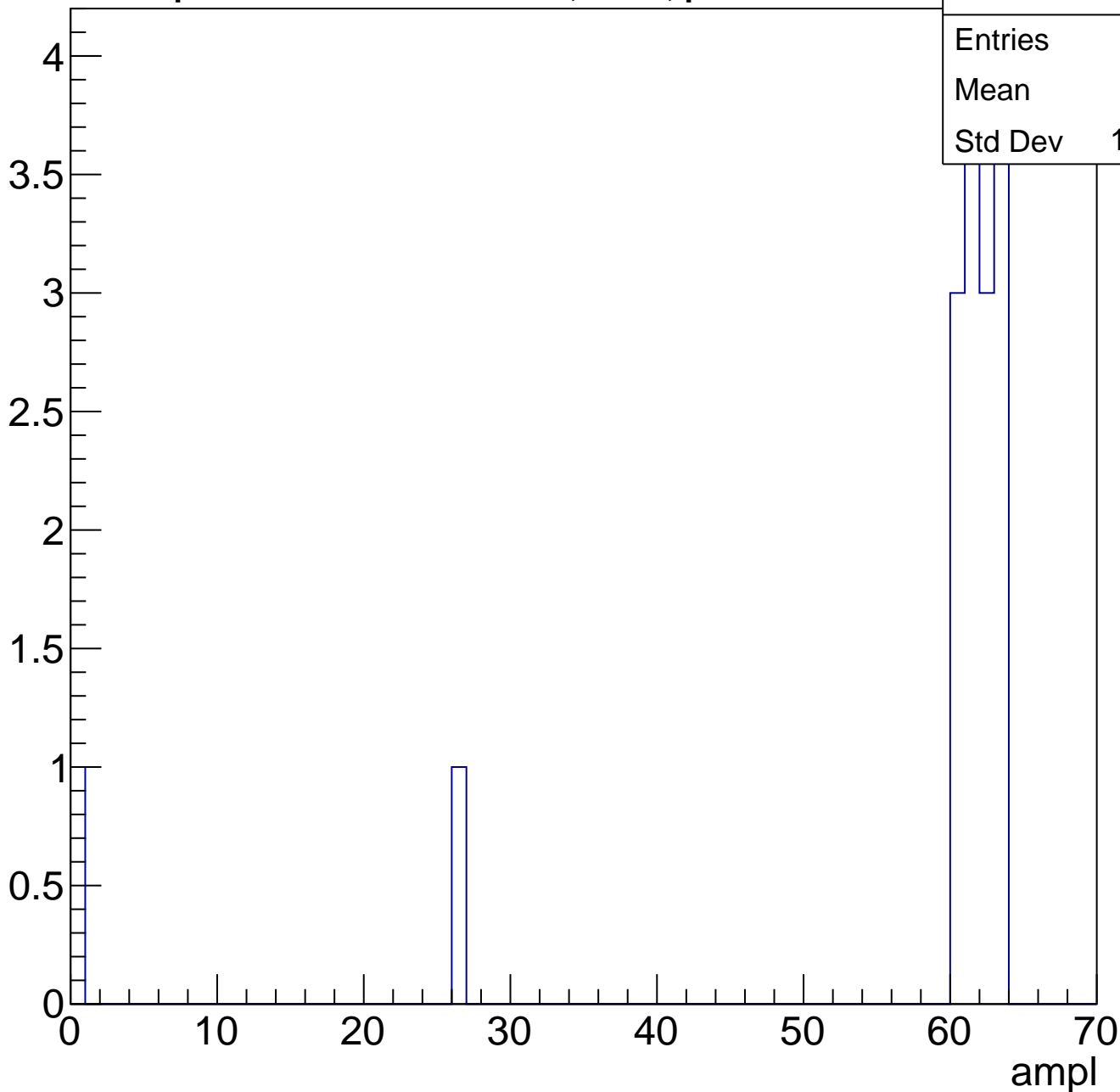




# B1L103S, U4-ch98, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



|         |       |
|---------|-------|
| Entries | 16    |
| Mean    | 55.5  |
| Std Dev | 16.74 |



# B1L103S, U4-ch98, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 20    |
| Mean    | 3.1   |
| Std Dev | 13.51 |

Entry



# B1L103S, U4-ch99, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

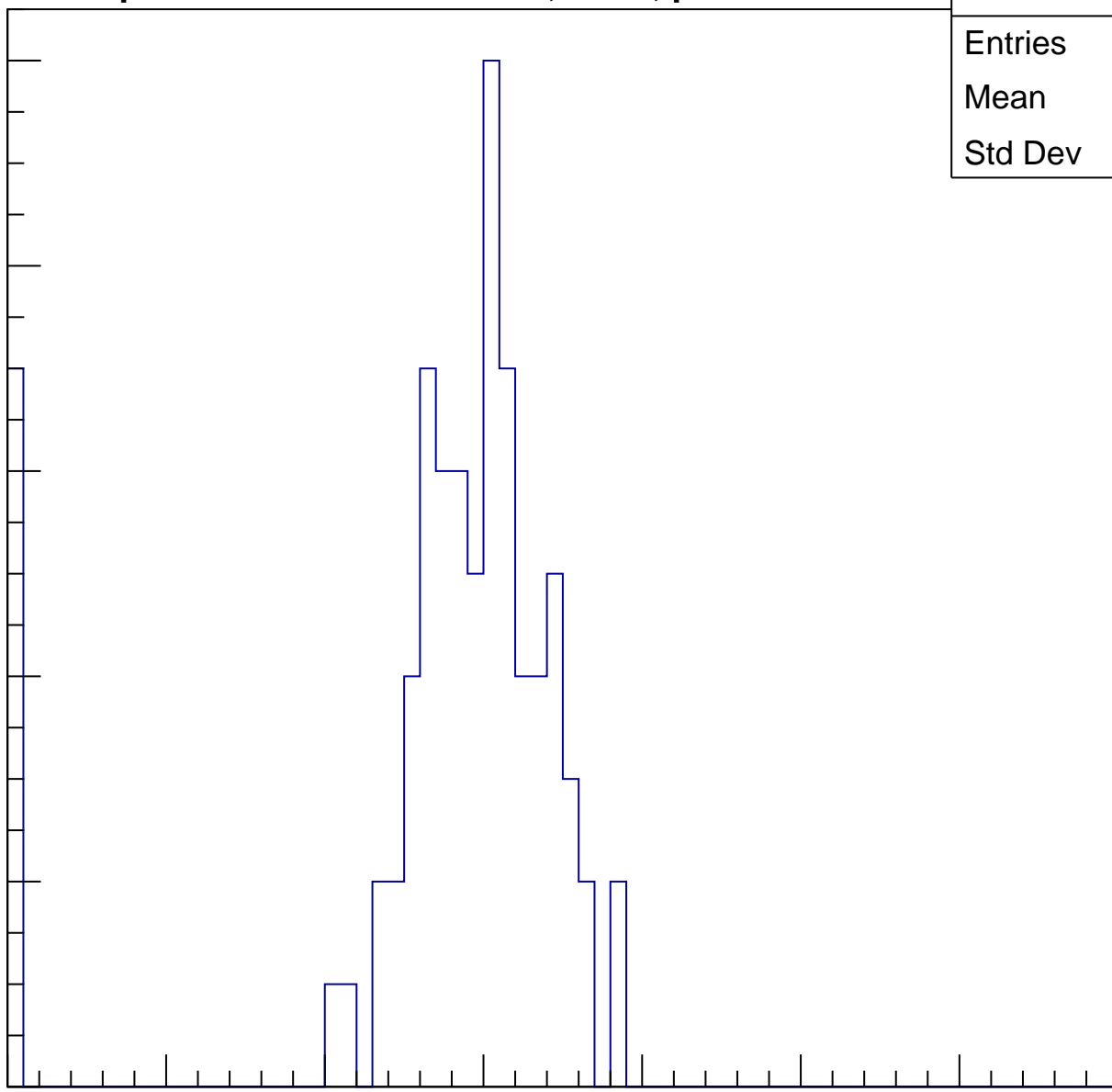
|         |       |
|---------|-------|
| Entries | 78    |
| Mean    | 26.82 |
| Std Dev | 9.179 |

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

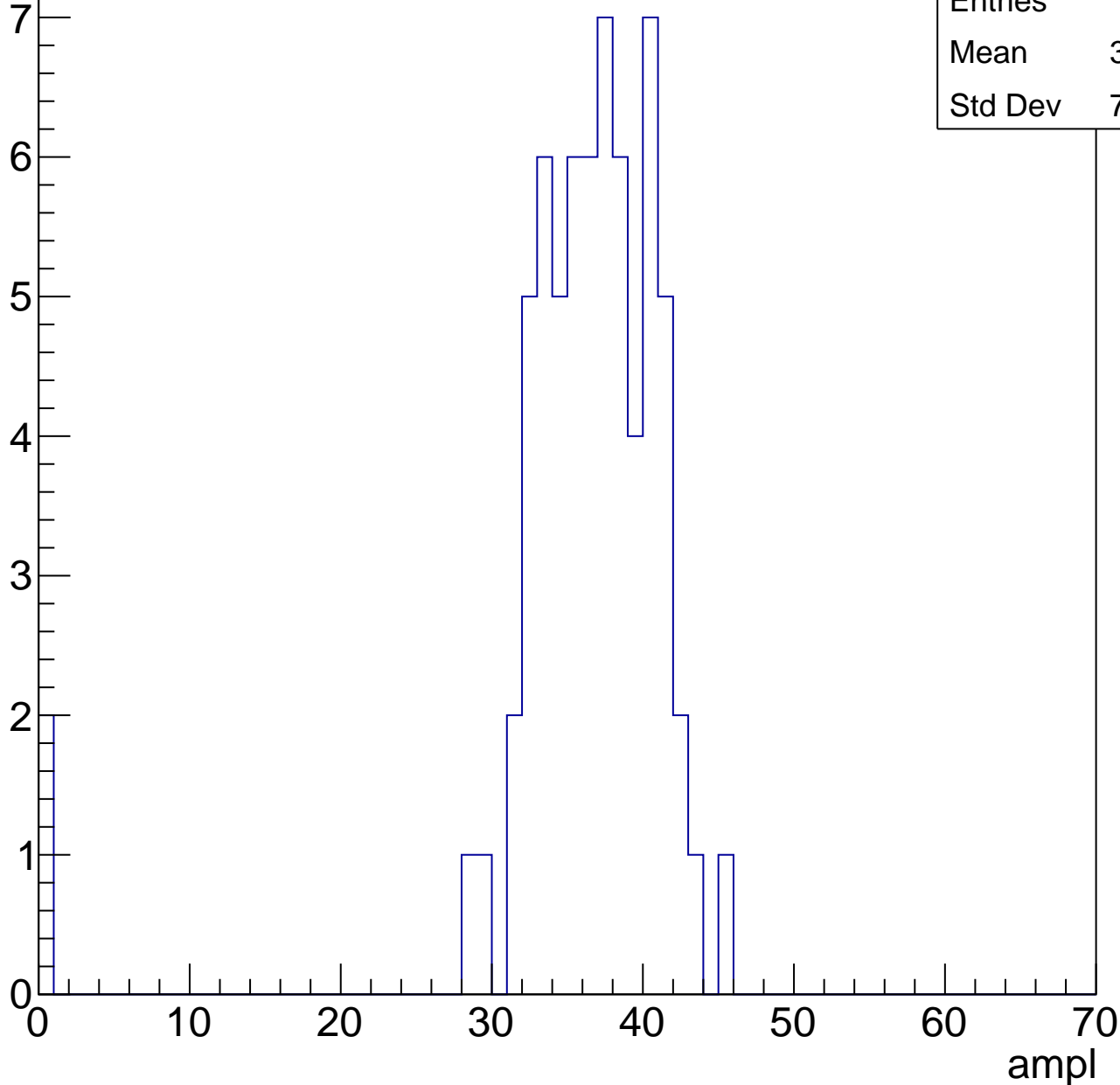


# B1L103S, U4-ch99, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 67    |
| Mean    | 35.42 |
| Std Dev | 7.122 |

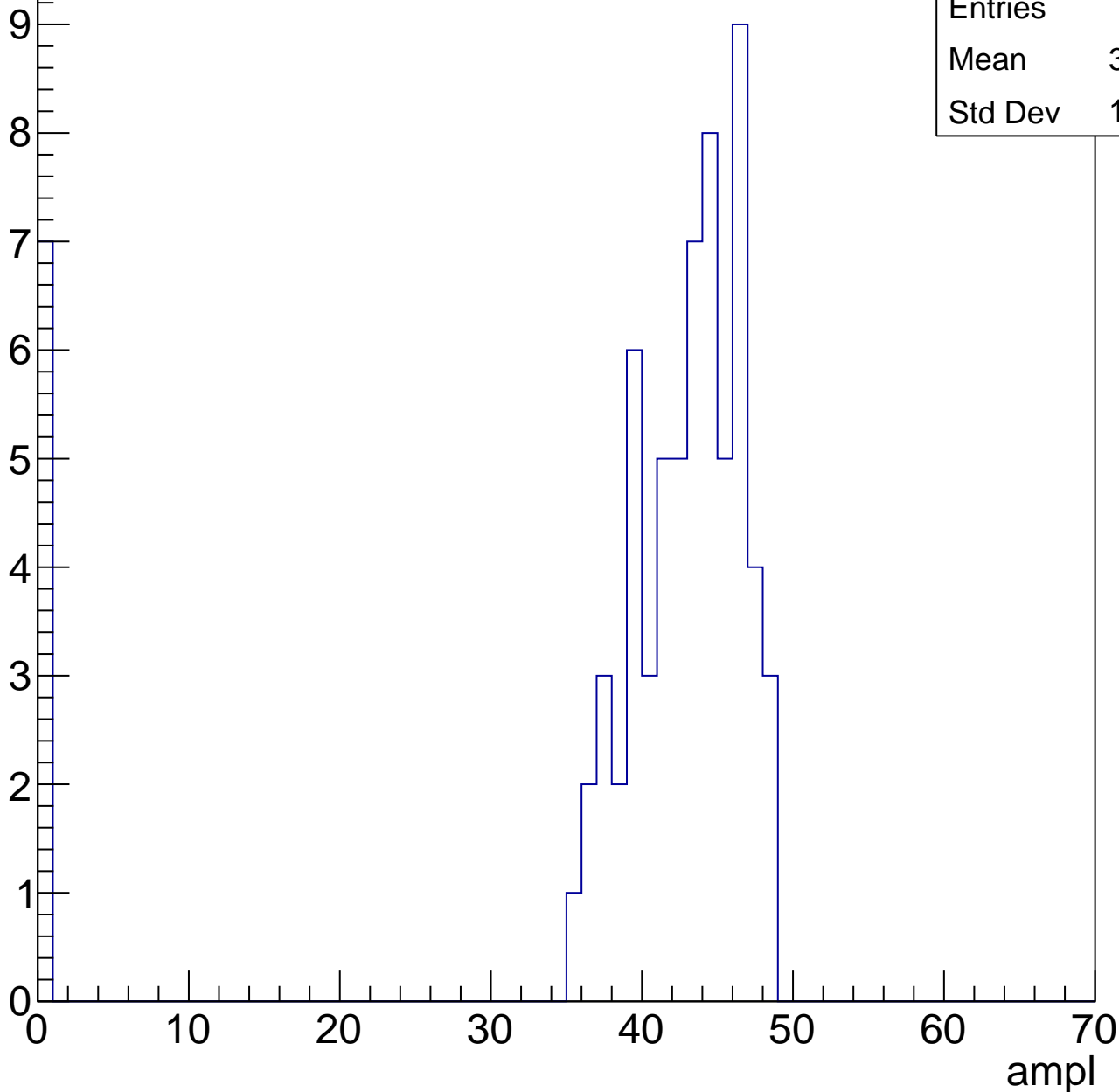


# B1L103S, U4-ch99, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 70    |
| Mean    | 38.39 |
| Std Dev | 13.18 |

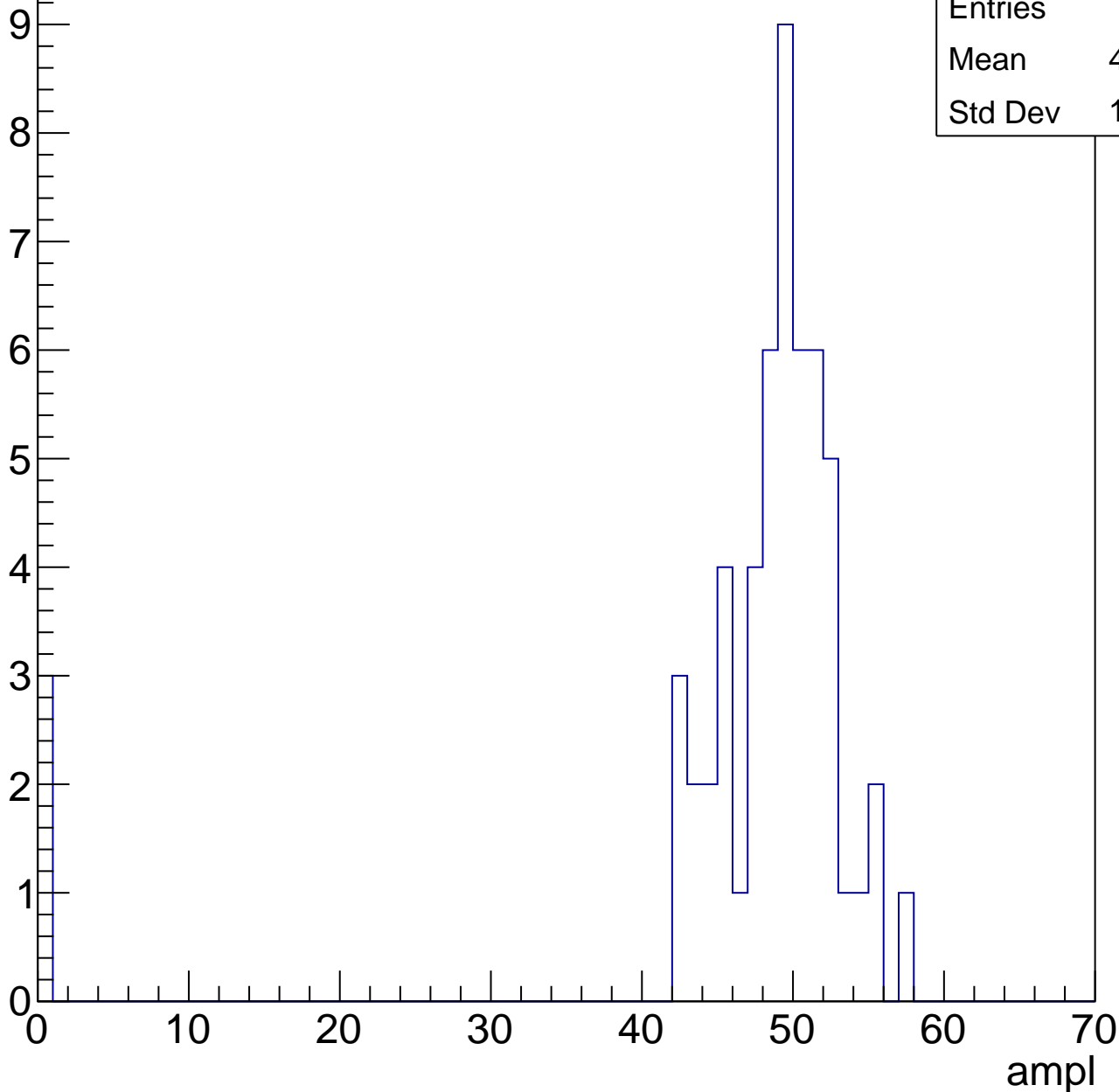


# B1L103S, U4-ch99, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 56    |
| Mean    | 46.12 |
| Std Dev | 11.46 |

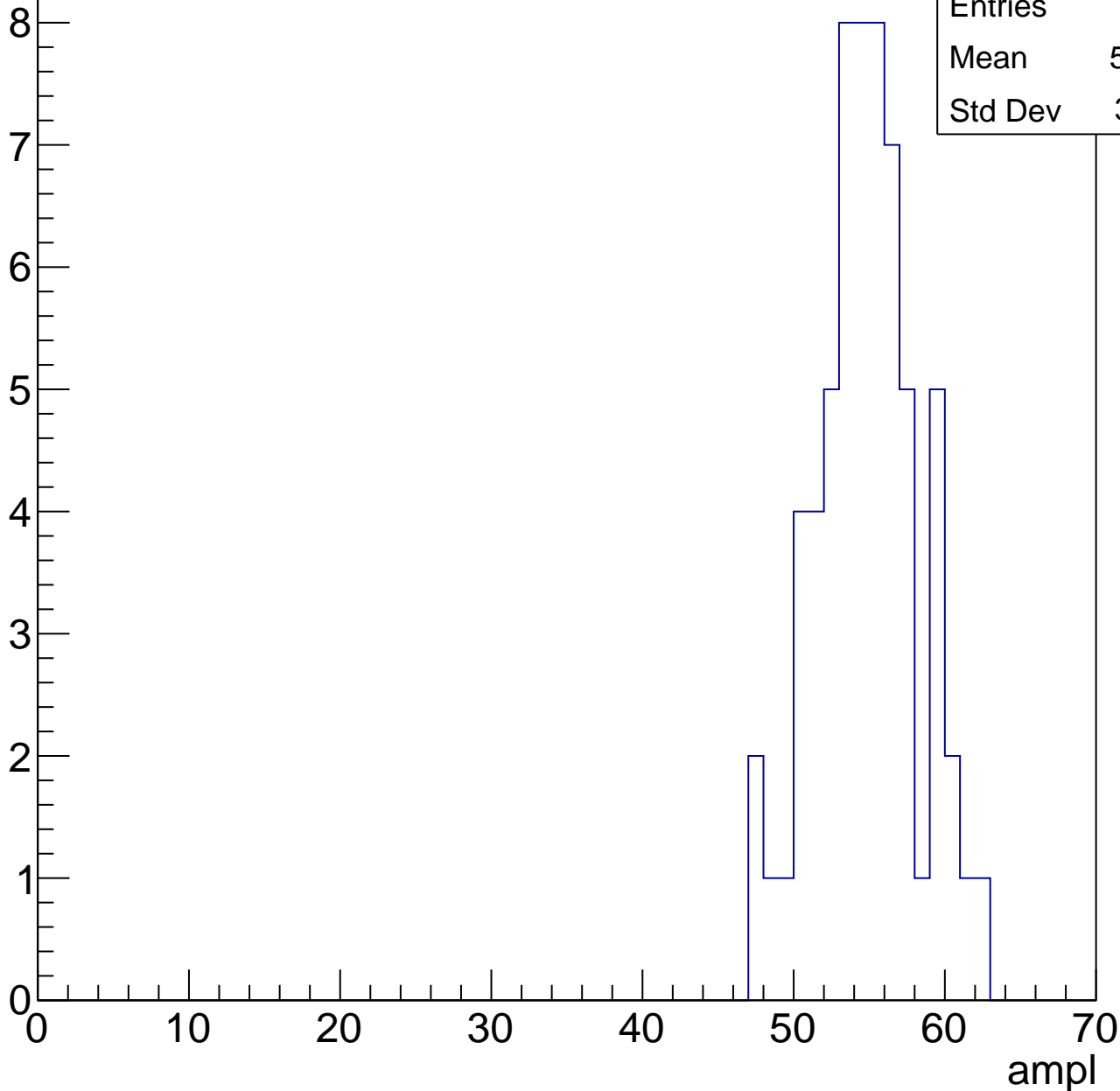


# B1L103S, U4-ch99, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

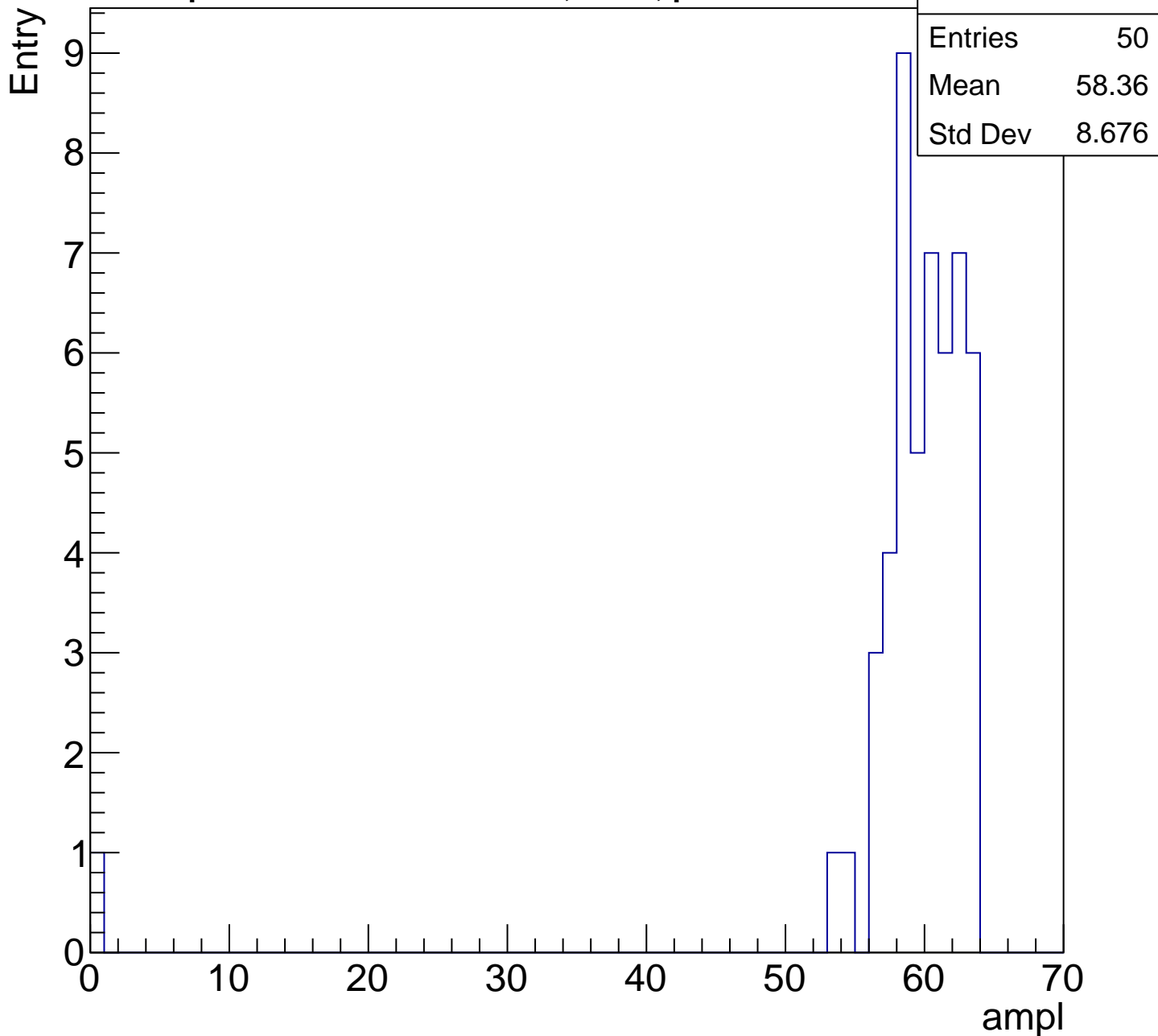
Entry

|         |       |
|---------|-------|
| Entries | 63    |
| Mean    | 54.35 |
| Std Dev | 3.301 |



# B1L103S, U4-ch99, adc5

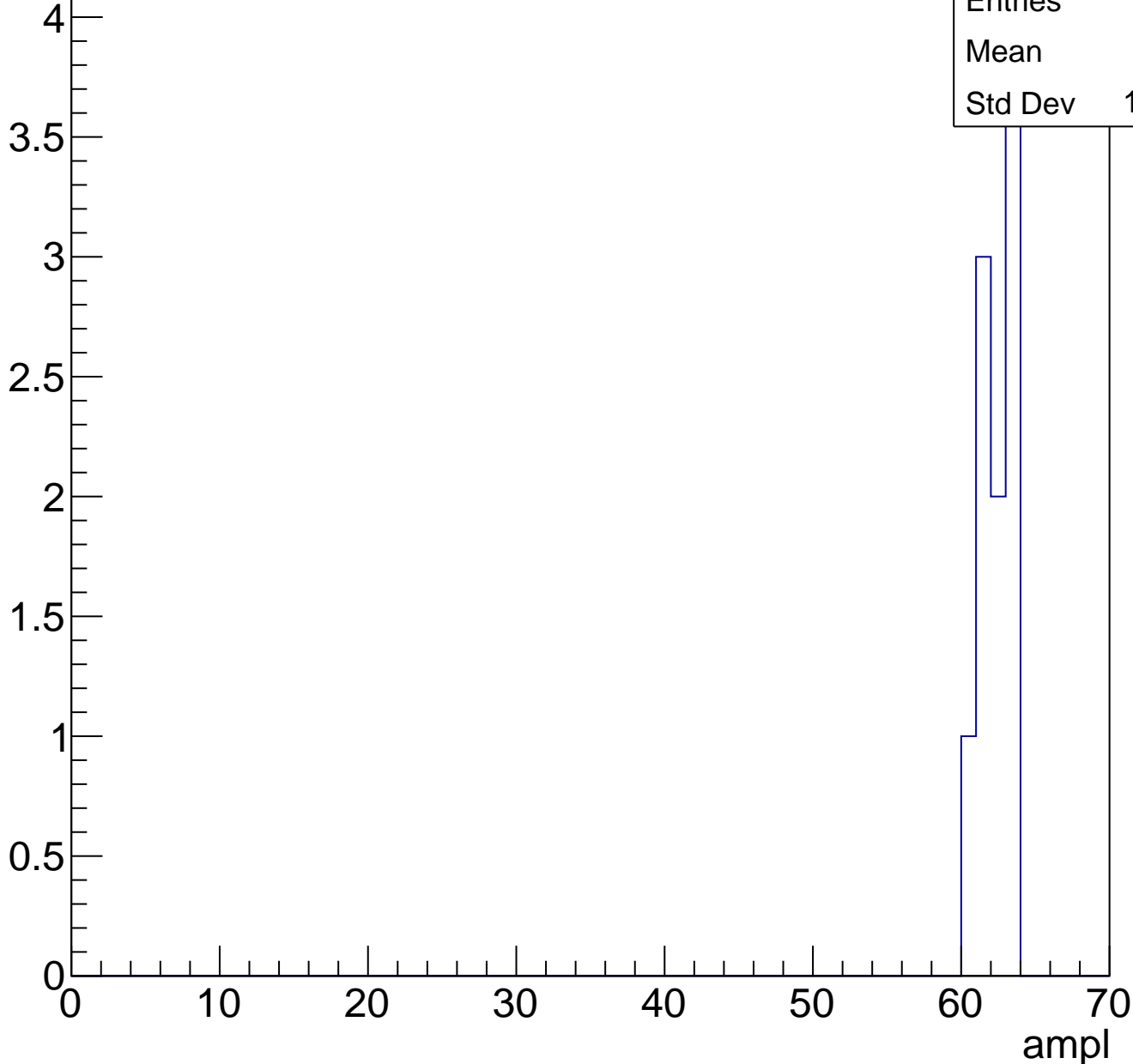
calib\_packv5\_041523\_1651.root, FC#0, port C2



# B1L103S, U4-ch99, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



|         |       |
|---------|-------|
| Entries | 10    |
| Mean    | 61.9  |
| Std Dev | 1.044 |



# B1L103S, U4-ch99, adc7

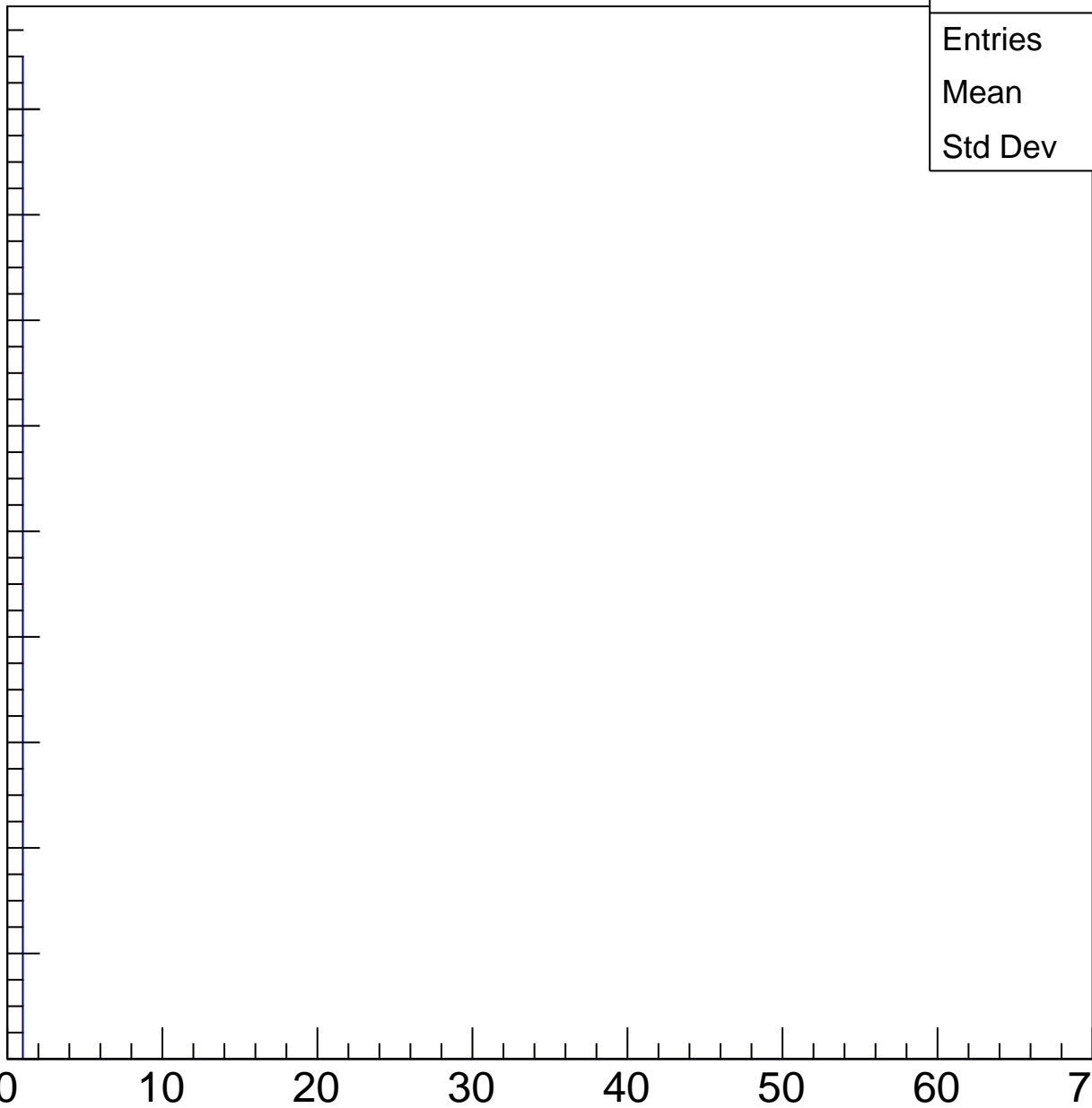
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

|         |    |
|---------|----|
| Entries | 19 |
| Mean    | 0  |
| Std Dev | 0  |

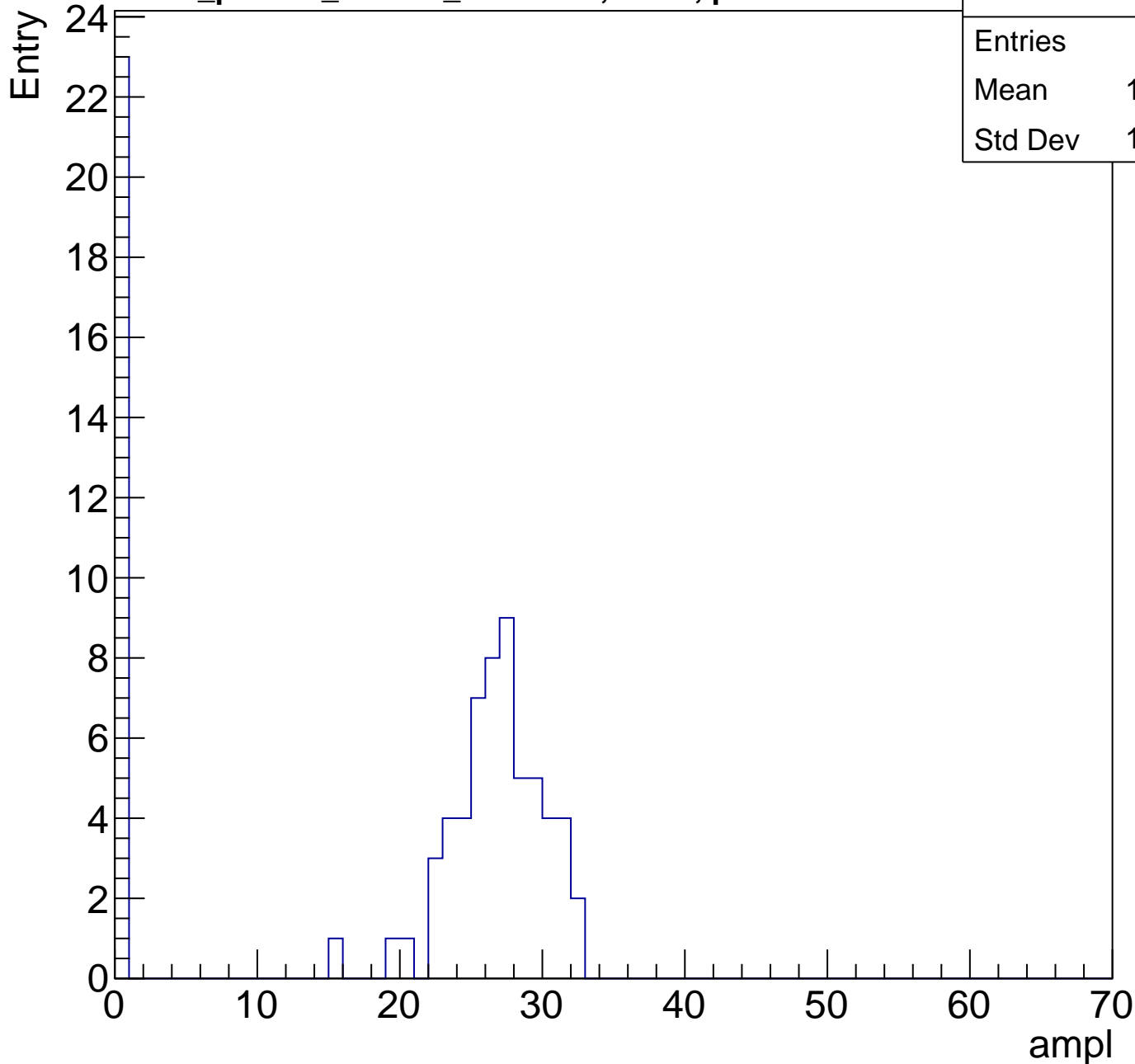
ampl



# B1L103S, U4-ch100, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 81    |
| Mean    | 18.85 |
| Std Dev | 12.19 |



# B1L103S, U4-ch100, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 71    |
| Mean    | 32.93 |
| Std Dev | 5.39  |

Entry

10  
8  
6  
4  
2  
0

ampl

0

10

20

30

40

50

60

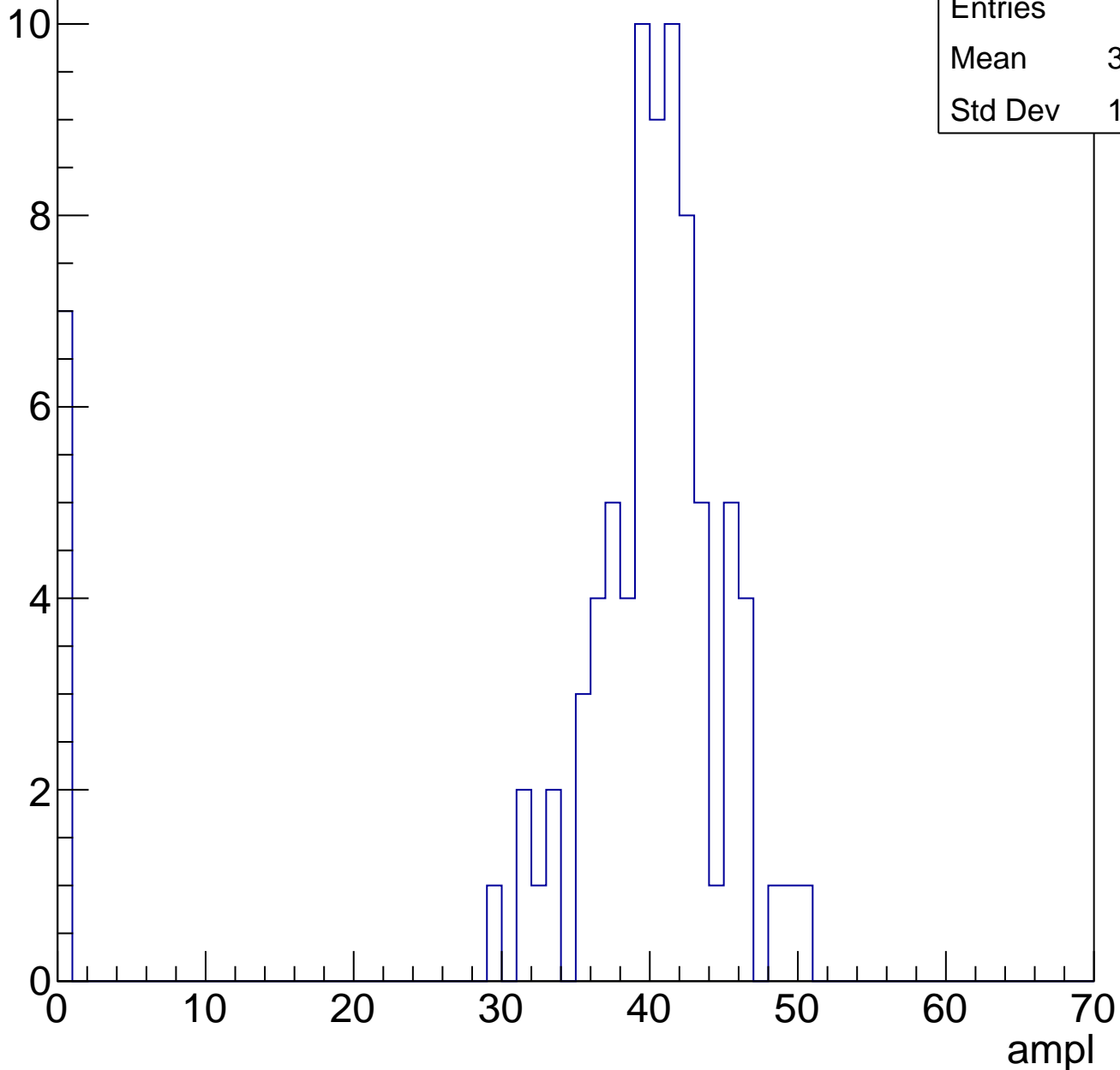
70

# B1L103S, U4-ch100, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 84    |
| Mean    | 36.74 |
| Std Dev | 11.74 |

Entry

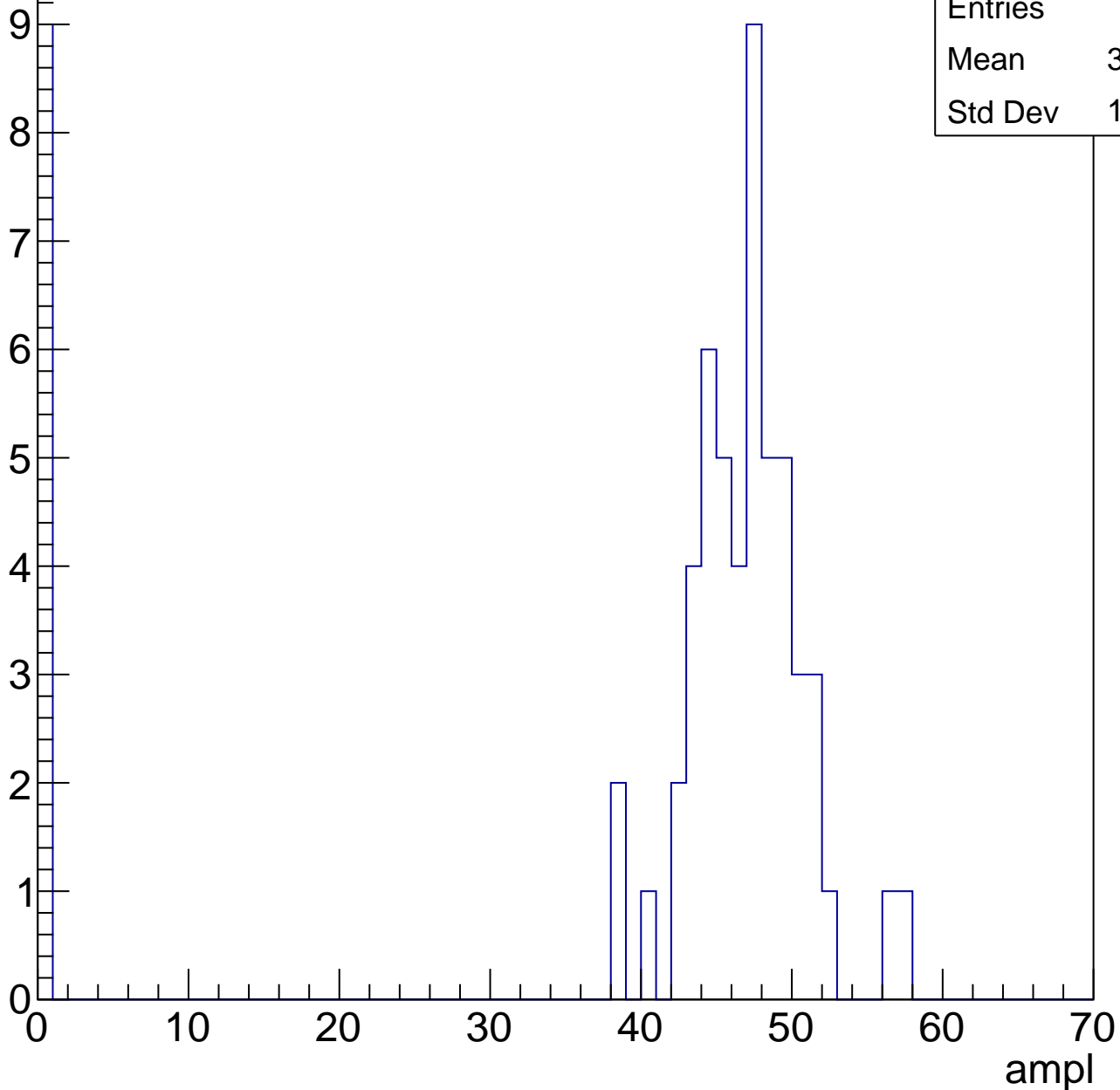


# B1L103S, U4-ch100, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 61    |
| Mean    | 39.69 |
| Std Dev | 16.85 |

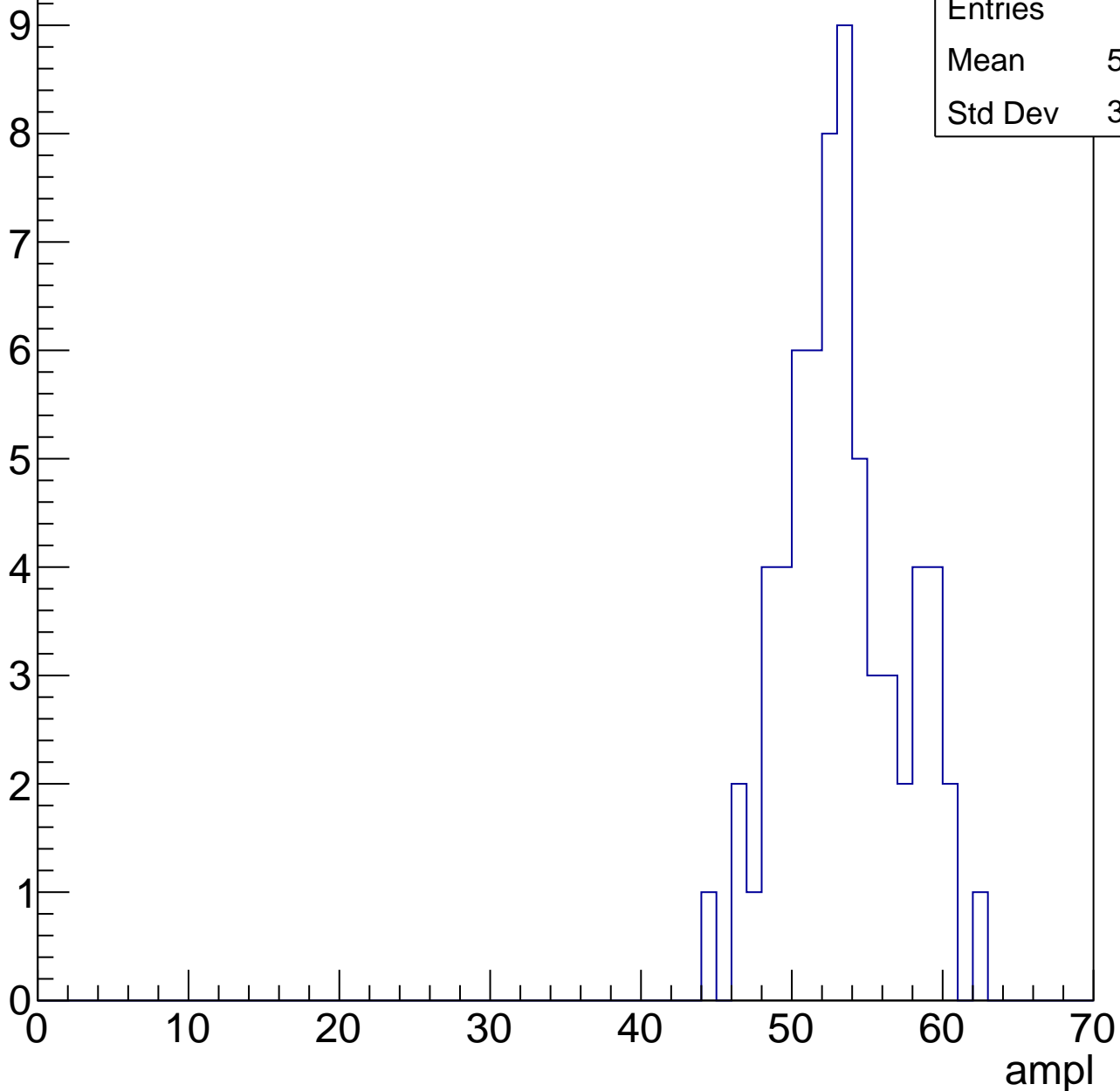


# B1L103S, U4-ch100, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

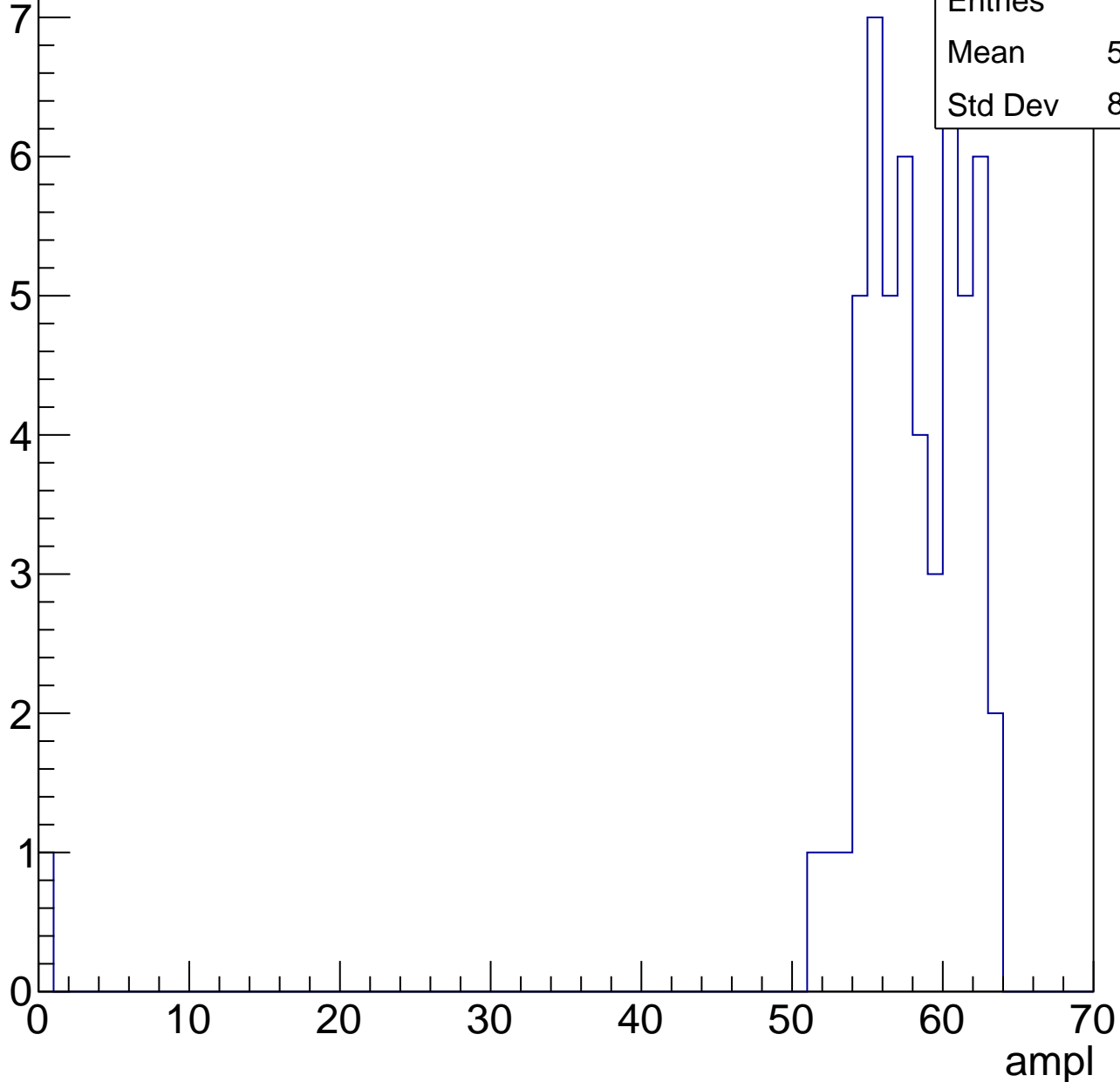
|         |       |
|---------|-------|
| Entries | 65    |
| Mean    | 52.88 |
| Std Dev | 3.849 |



# B1L103S, U4-ch100, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

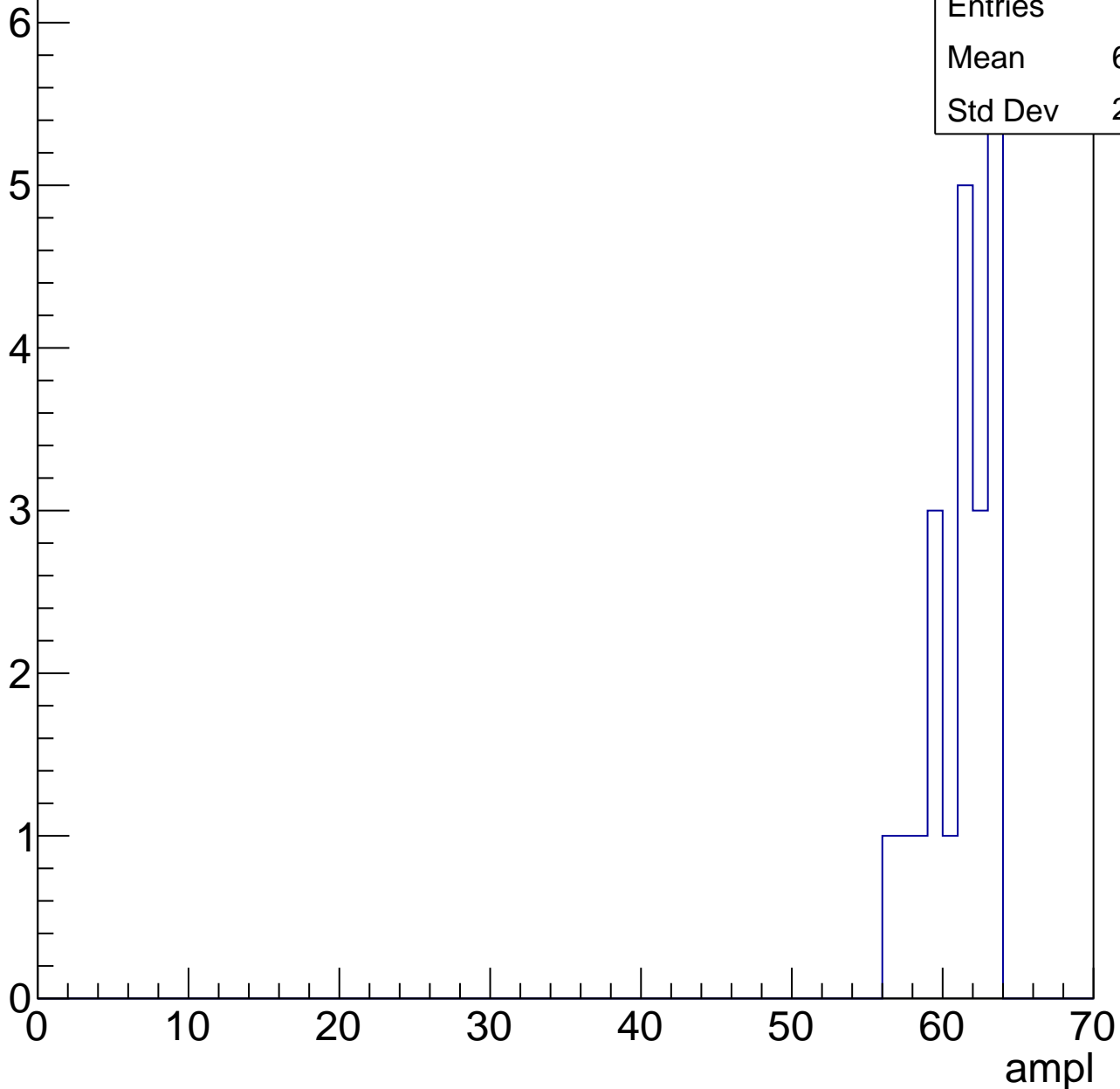


# B1L103S, U4-ch100, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 21    |
| Mean    | 60.81 |
| Std Dev | 2.061 |



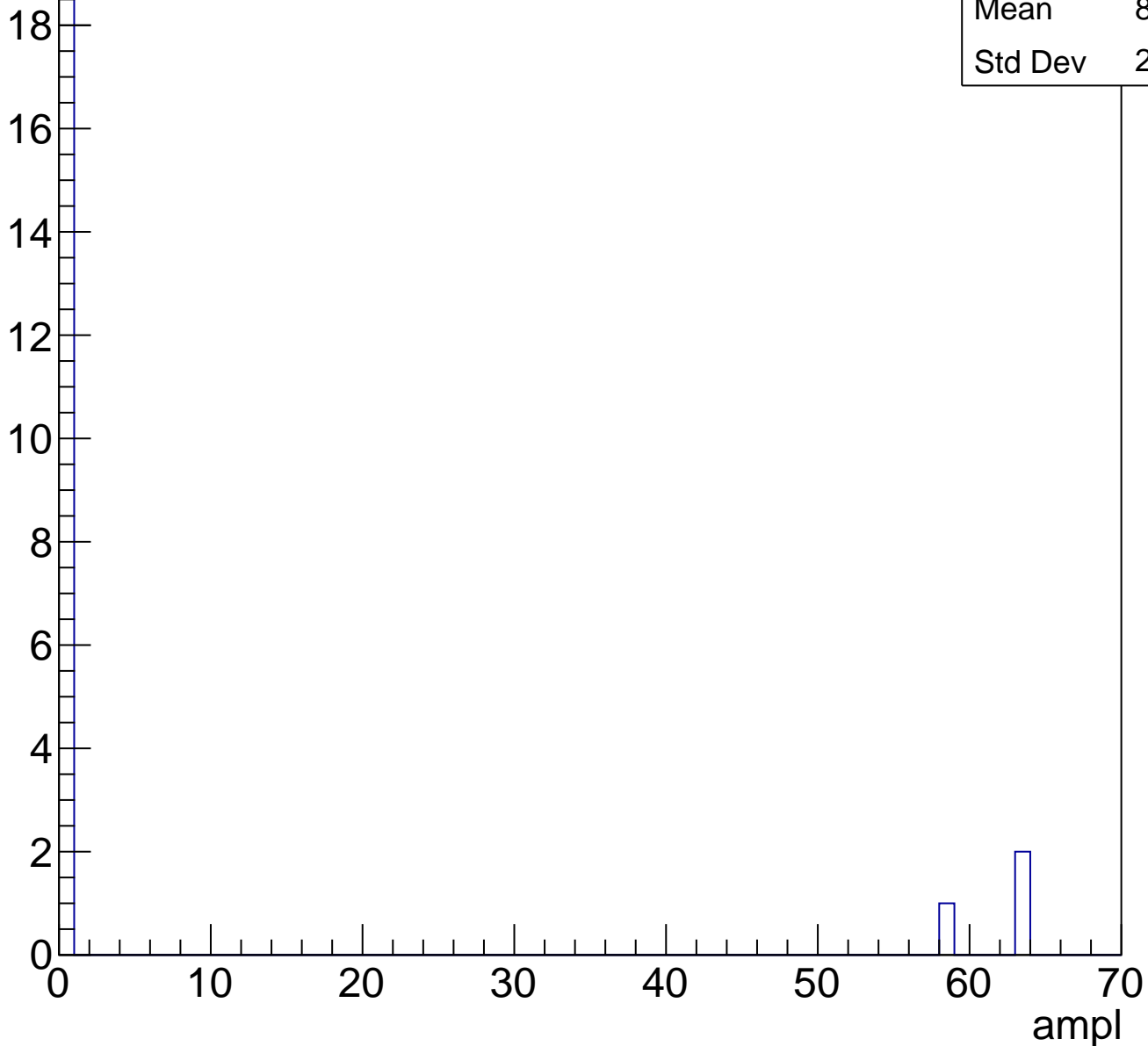


# B1L103S, U4-ch100, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 22    |
| Mean    | 8.364 |
| Std Dev | 21.07 |

Entry



# B1L103S, U4-ch101, adc0

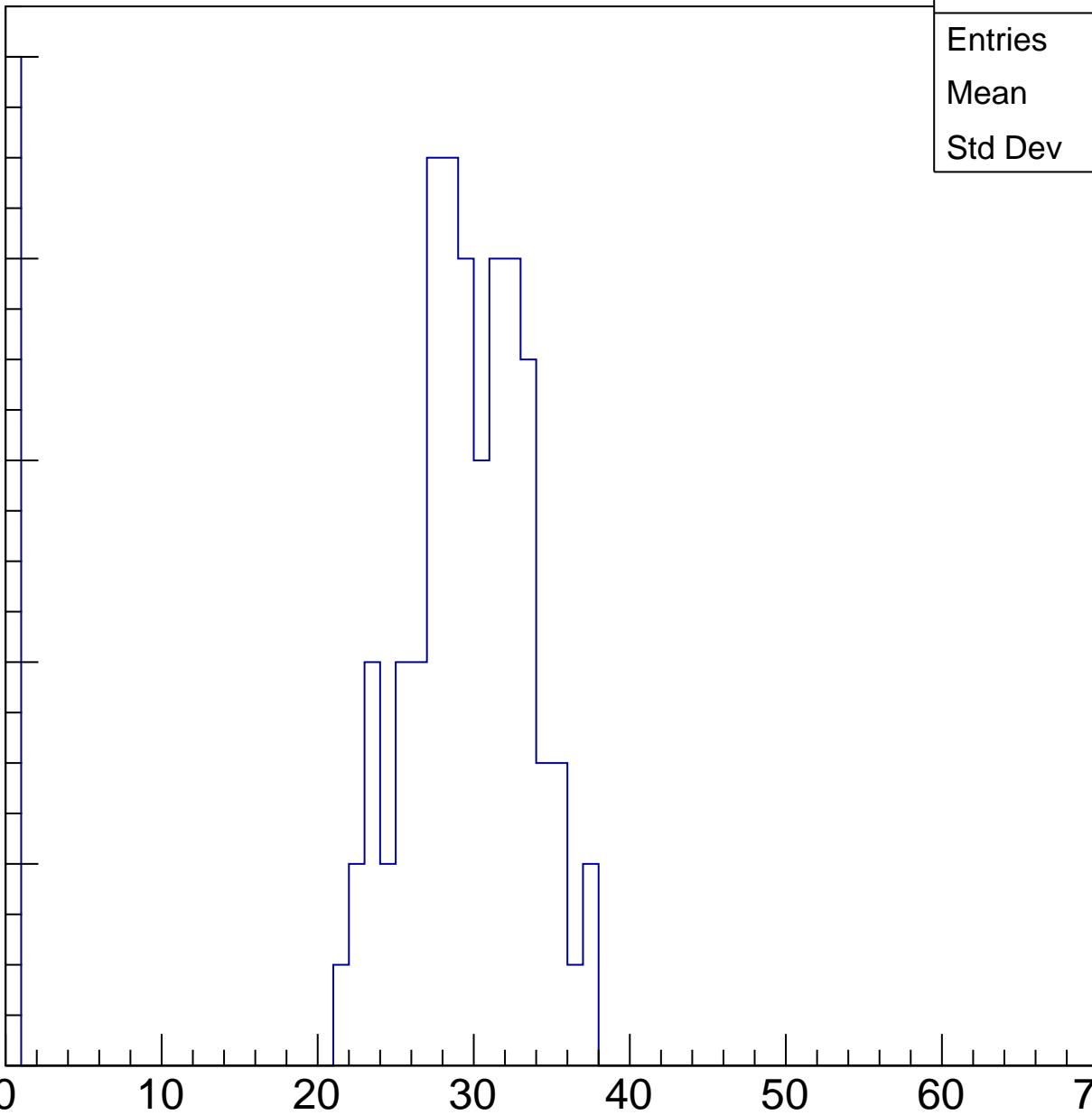
calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 91    |
| Mean    | 26.02 |
| Std Dev | 9.77  |

Entry

10  
8  
6  
4  
2  
0

ampl

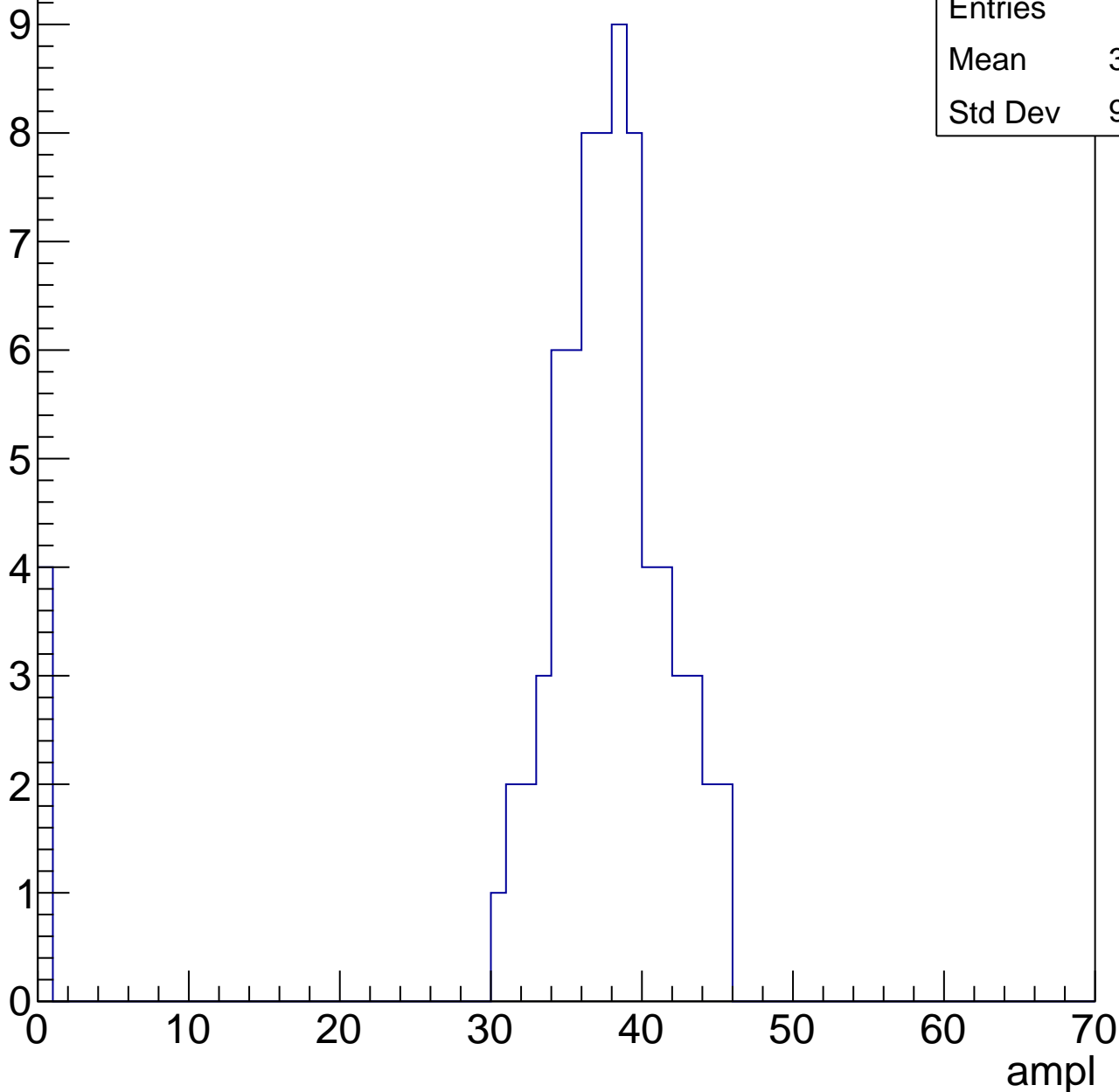


# B1L103S, U4-ch101, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 75    |
| Mean    | 35.52 |
| Std Dev | 9.068 |

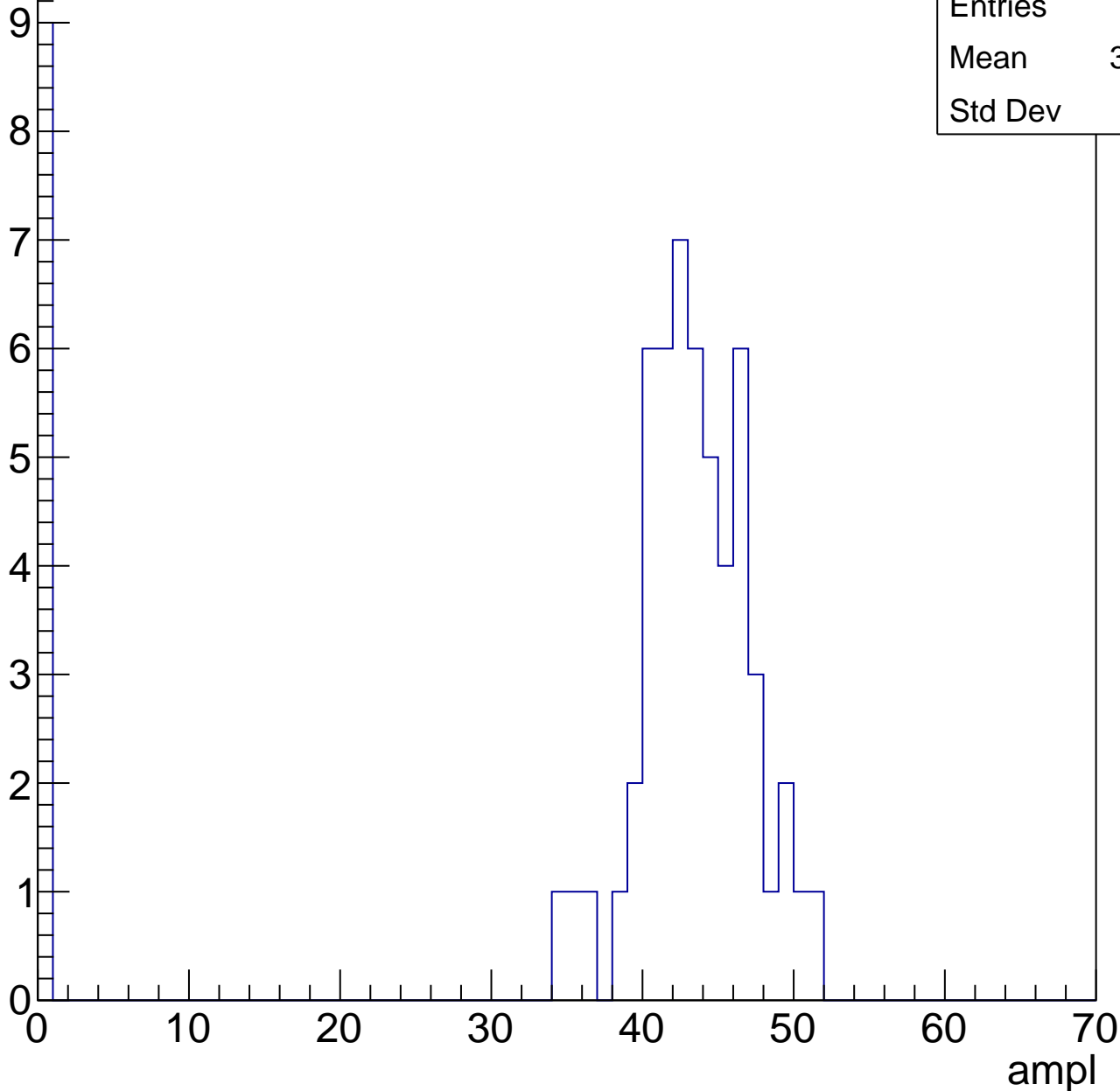


# B1L103S, U4-ch101, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 63    |
| Mean    | 36.87 |
| Std Dev | 15.4  |

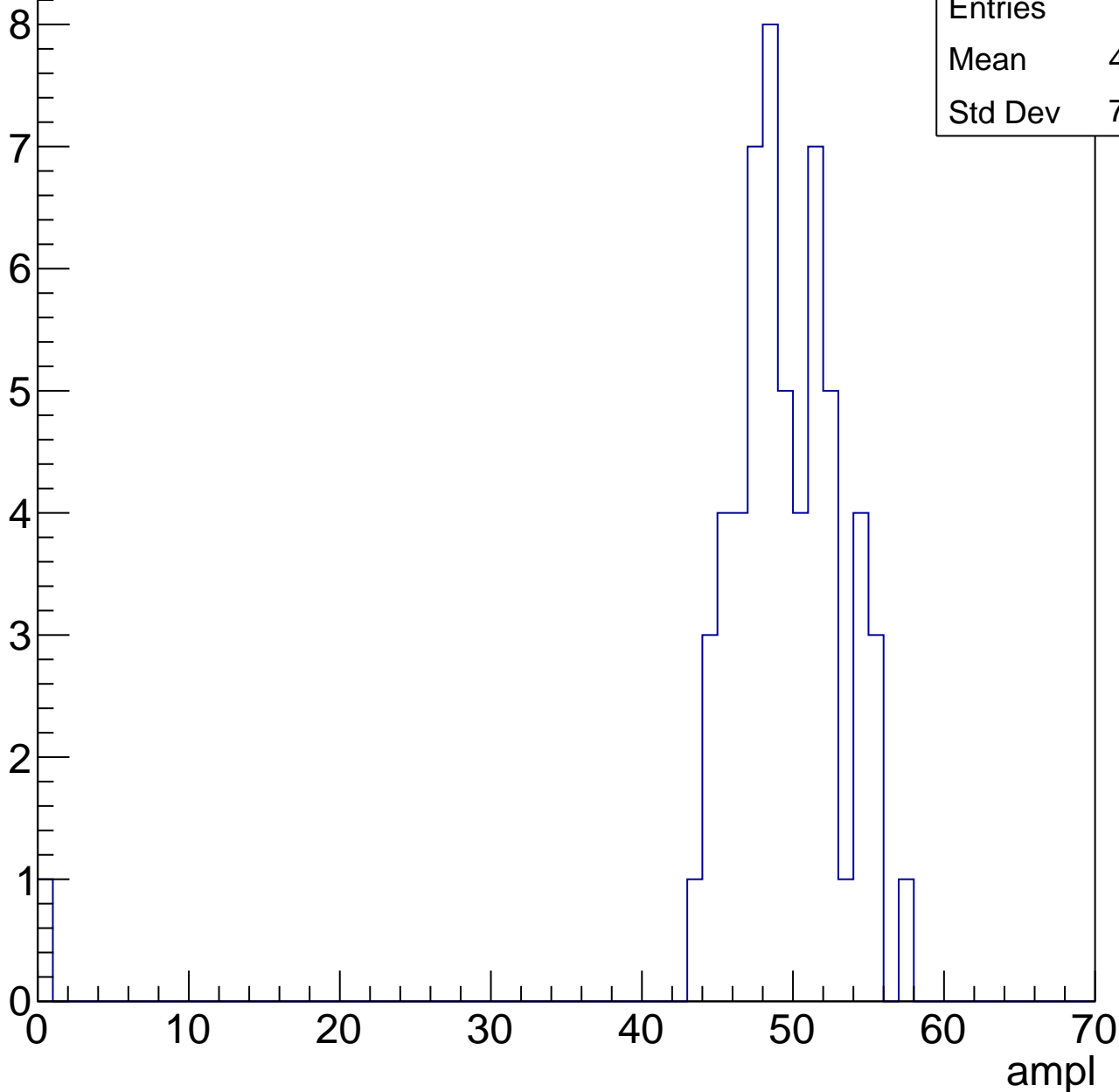


# B1L103S, U4-ch101, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 58    |
| Mean    | 48.36 |
| Std Dev | 7.179 |

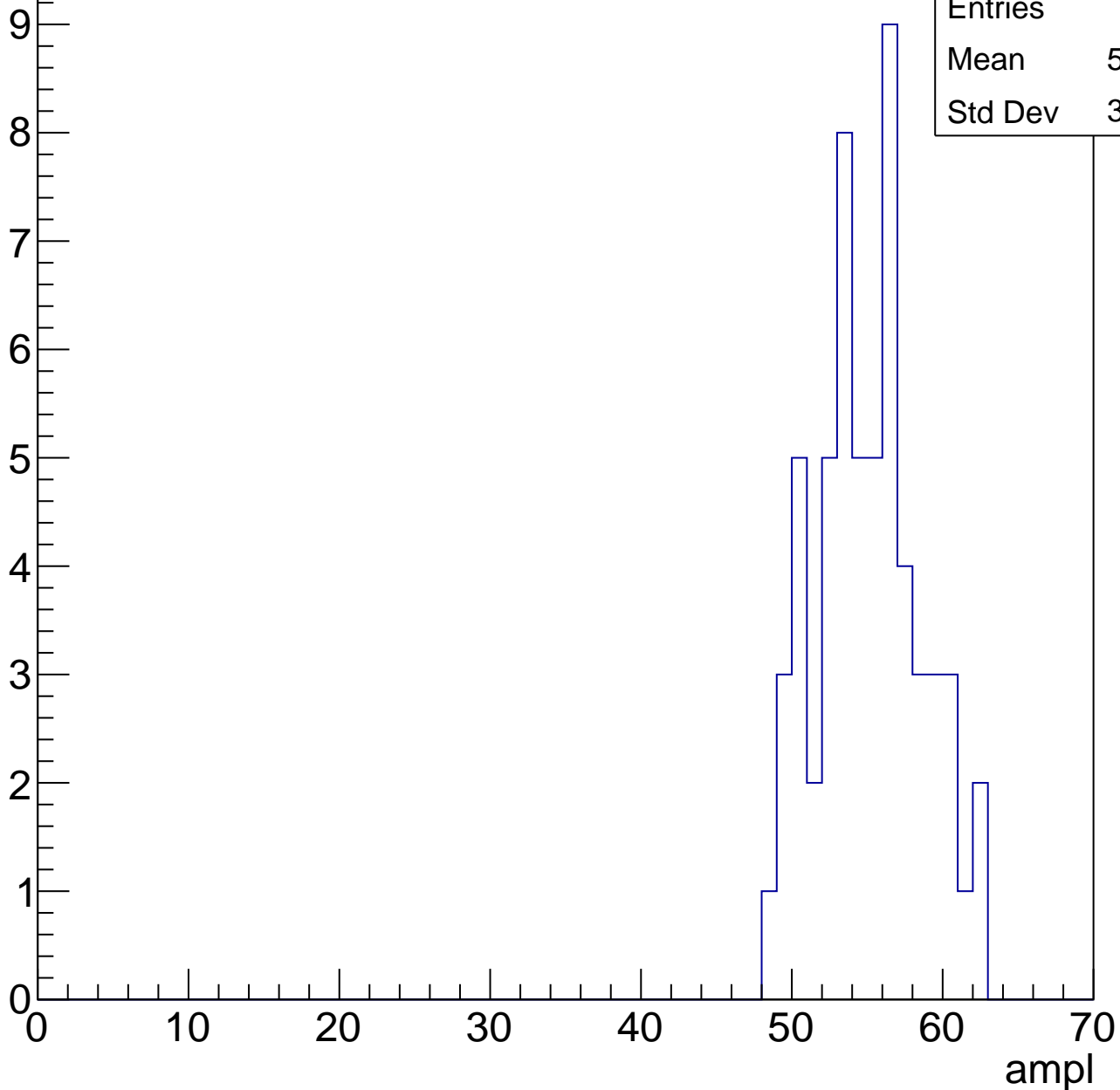


# B1L103S, U4-ch101, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 59    |
| Mean    | 54.64 |
| Std Dev | 3.438 |

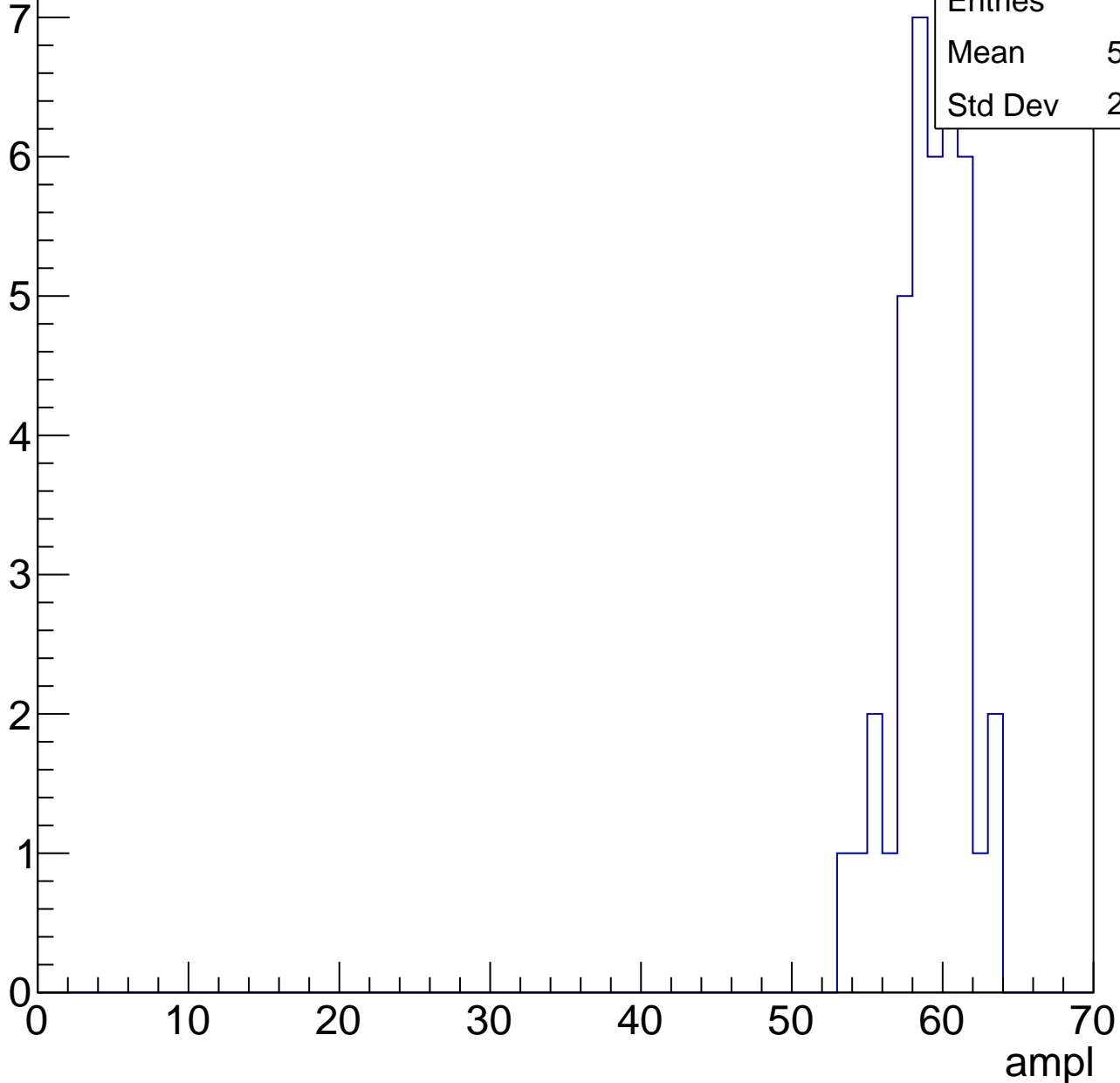


# B1L103S, U4-ch101, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 39    |
| Mean    | 58.77 |
| Std Dev | 2.258 |

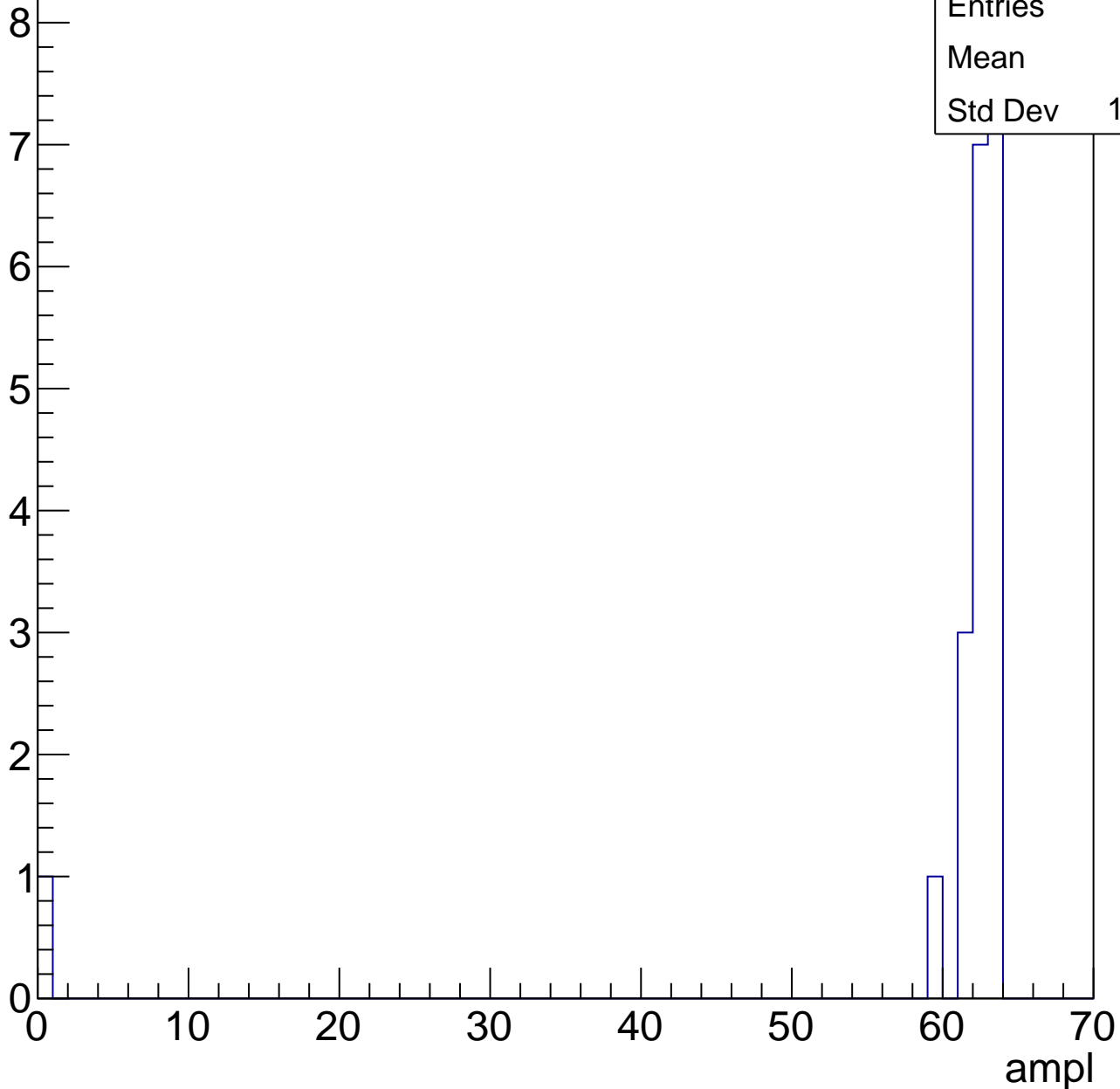


# B1L103S, U4-ch101, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 20    |
| Mean    | 59    |
| Std Dev | 13.57 |





# B1L103S, U4-ch101, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



|         |    |
|---------|----|
| Entries | 19 |
| Mean    | 0  |
| Std Dev | 0  |

# B1L103S, U4-ch102, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

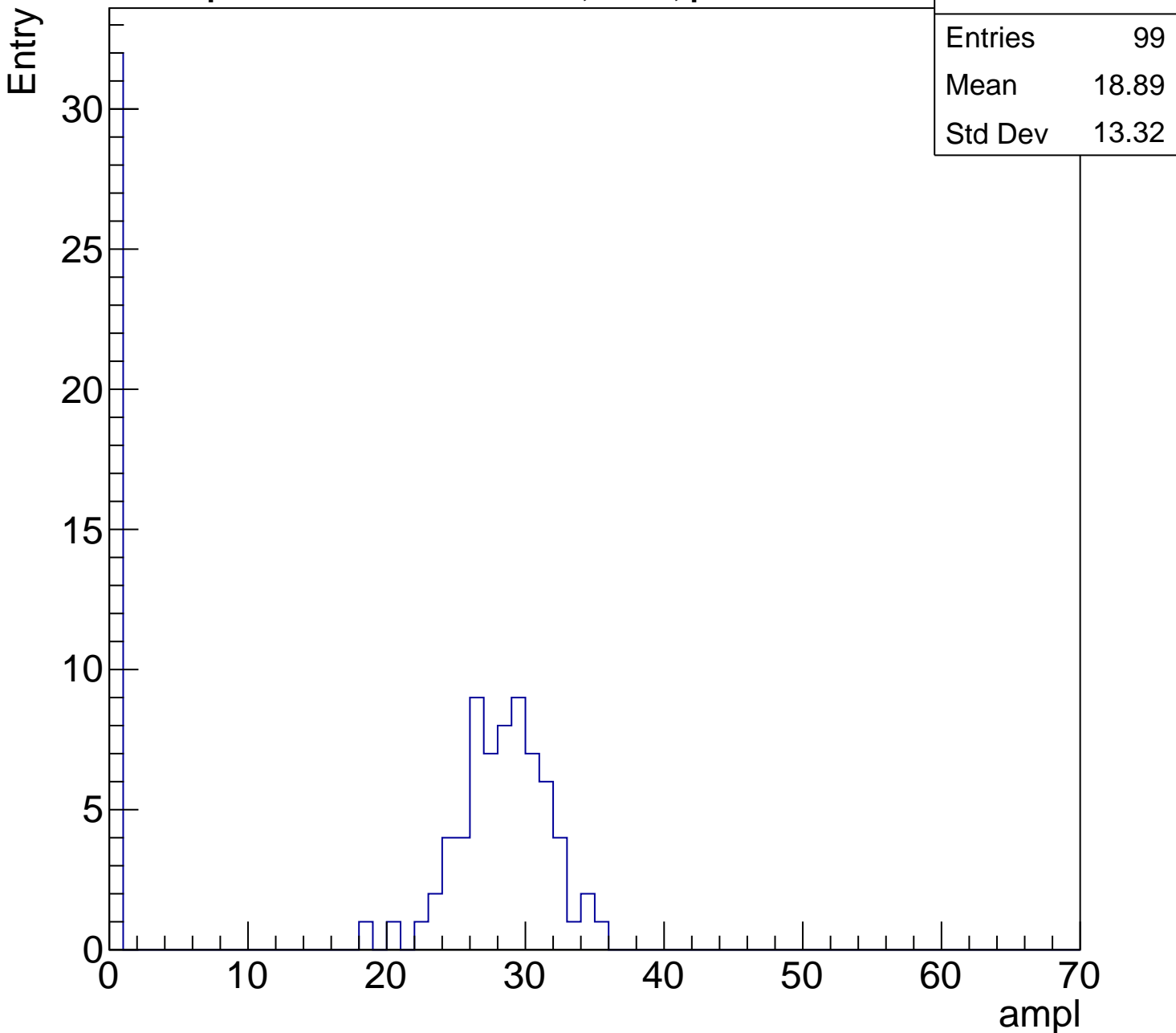
|         |       |
|---------|-------|
| Entries | 99    |
| Mean    | 18.89 |
| Std Dev | 13.32 |

Entry

30  
25  
20  
15  
10  
5  
0

0 10 20 30 40 50 60 70

ampl

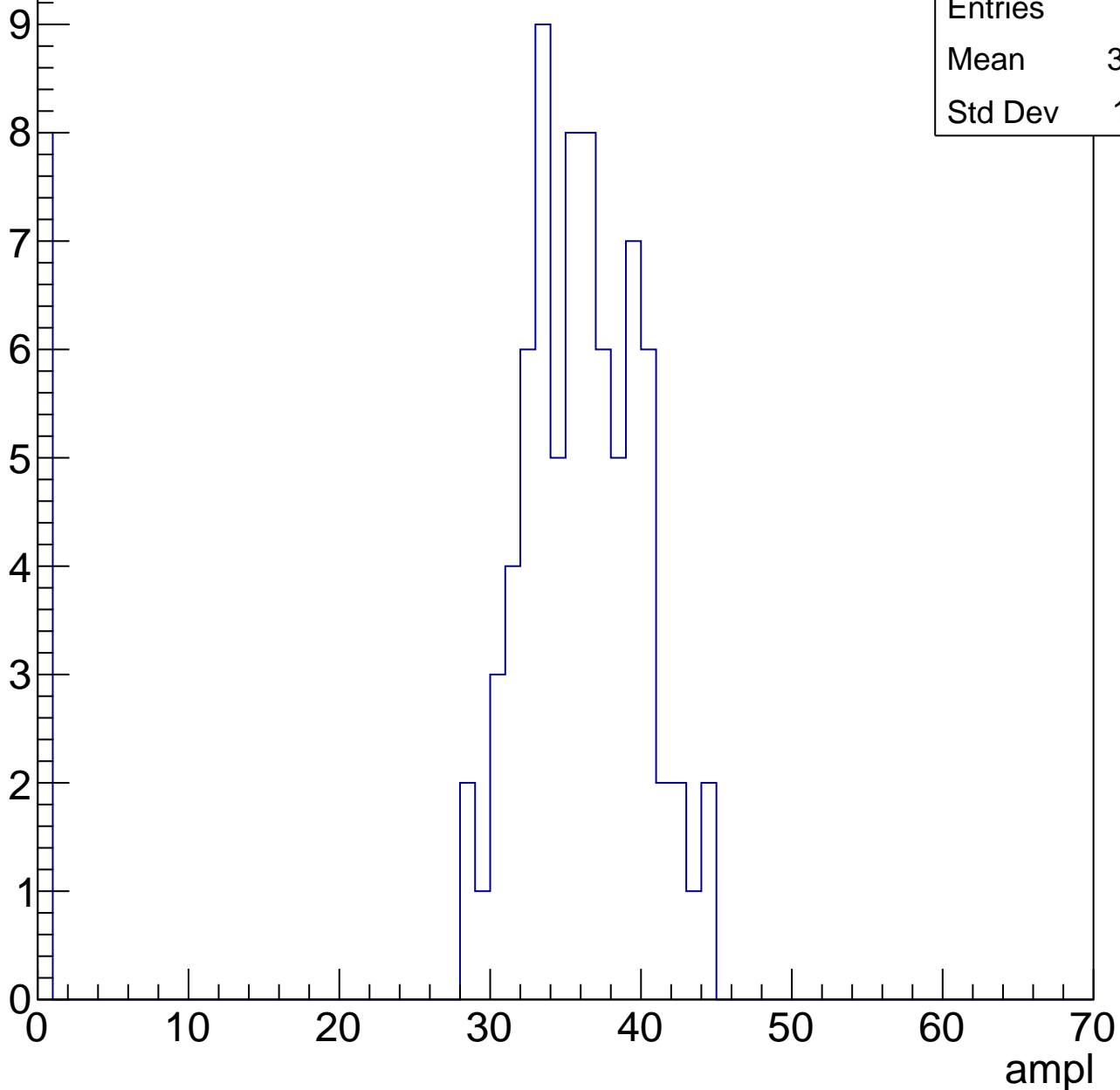


# B1L103S, U4-ch102, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 85    |
| Mean    | 32.33 |
| Std Dev | 11.01 |

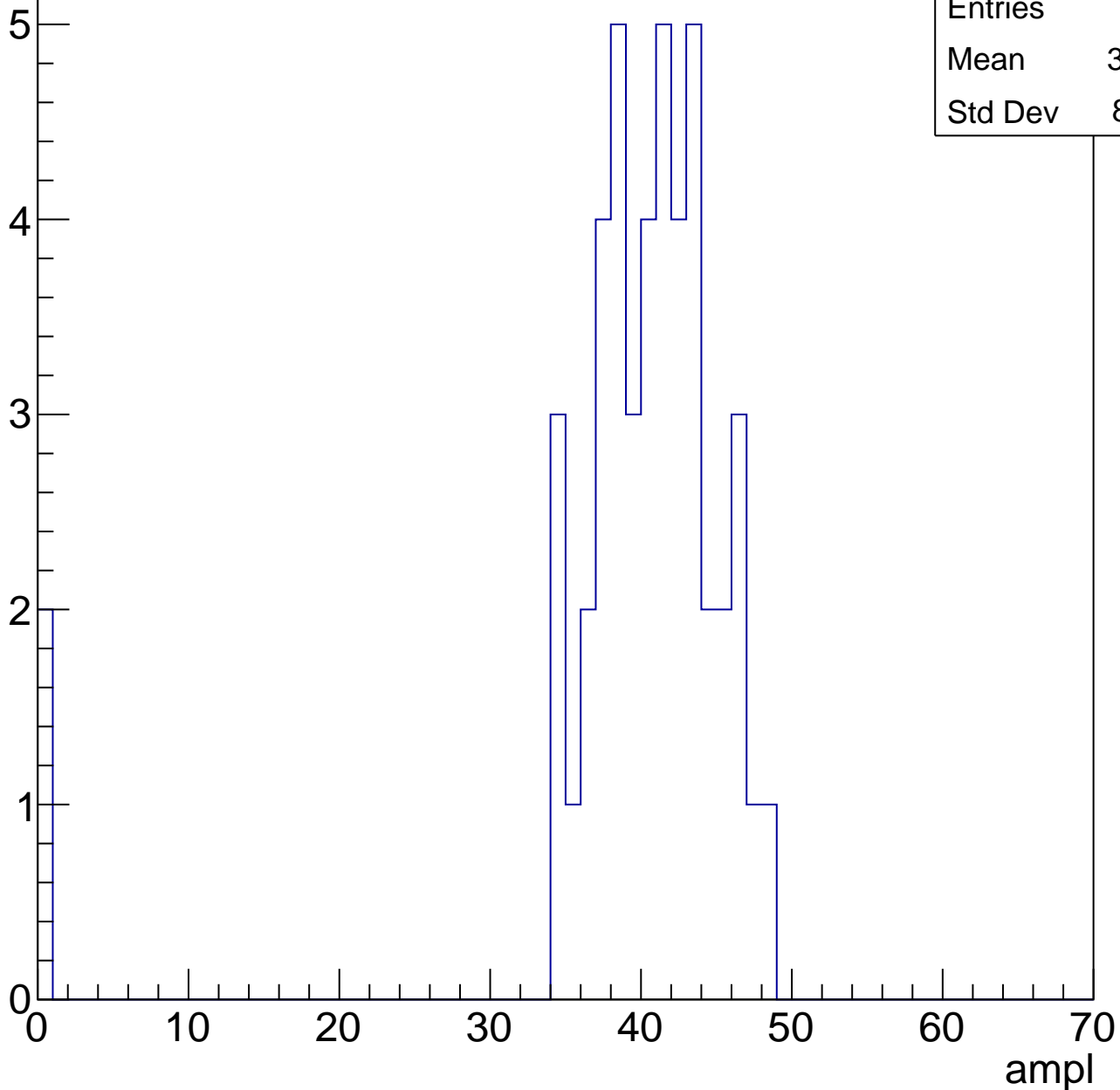


# B1L103S, U4-ch102, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 47    |
| Mean    | 38.79 |
| Std Dev | 8.901 |

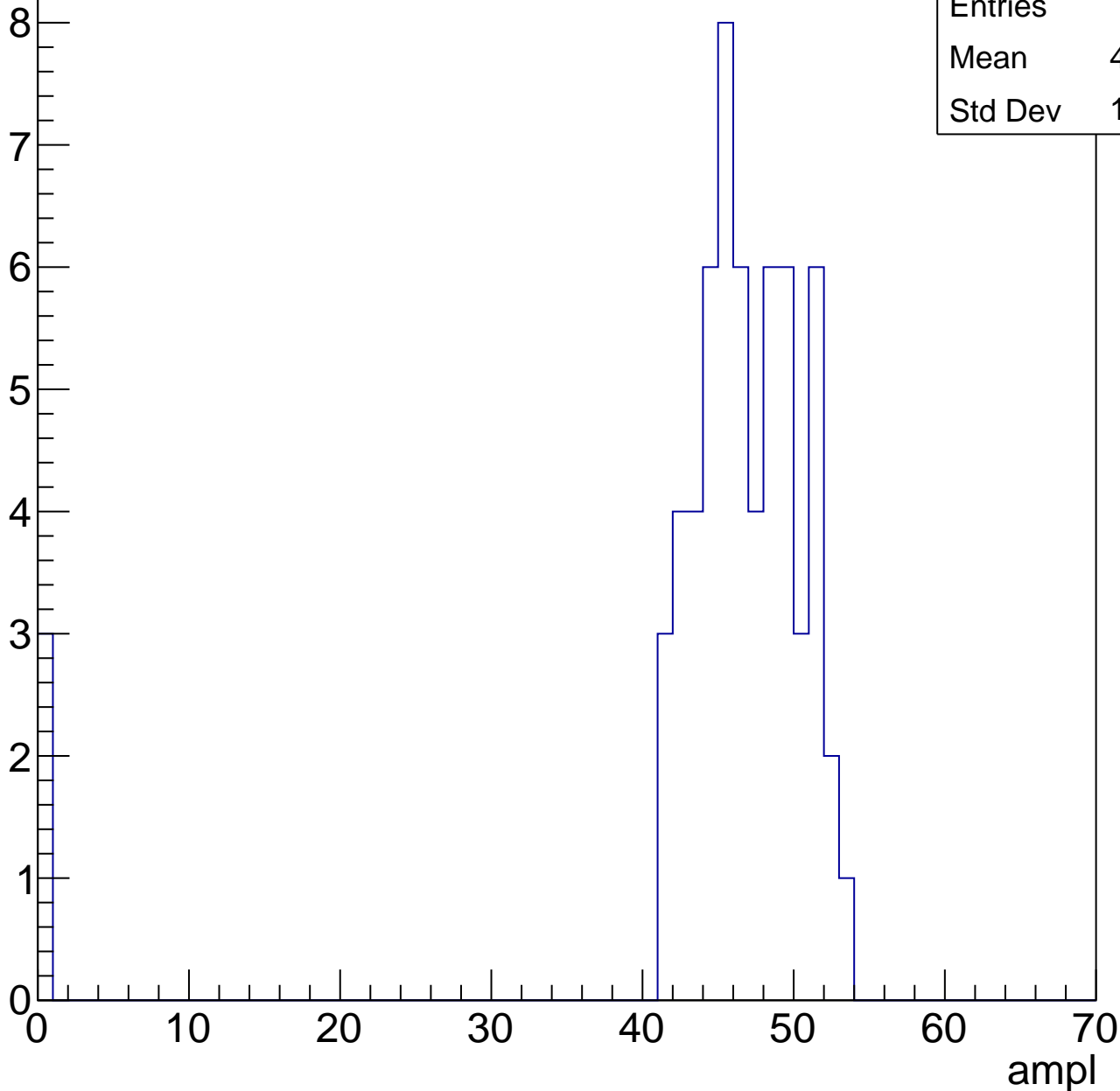


# B1L103S, U4-ch102, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 62    |
| Mean    | 44.29 |
| Std Dev | 10.45 |

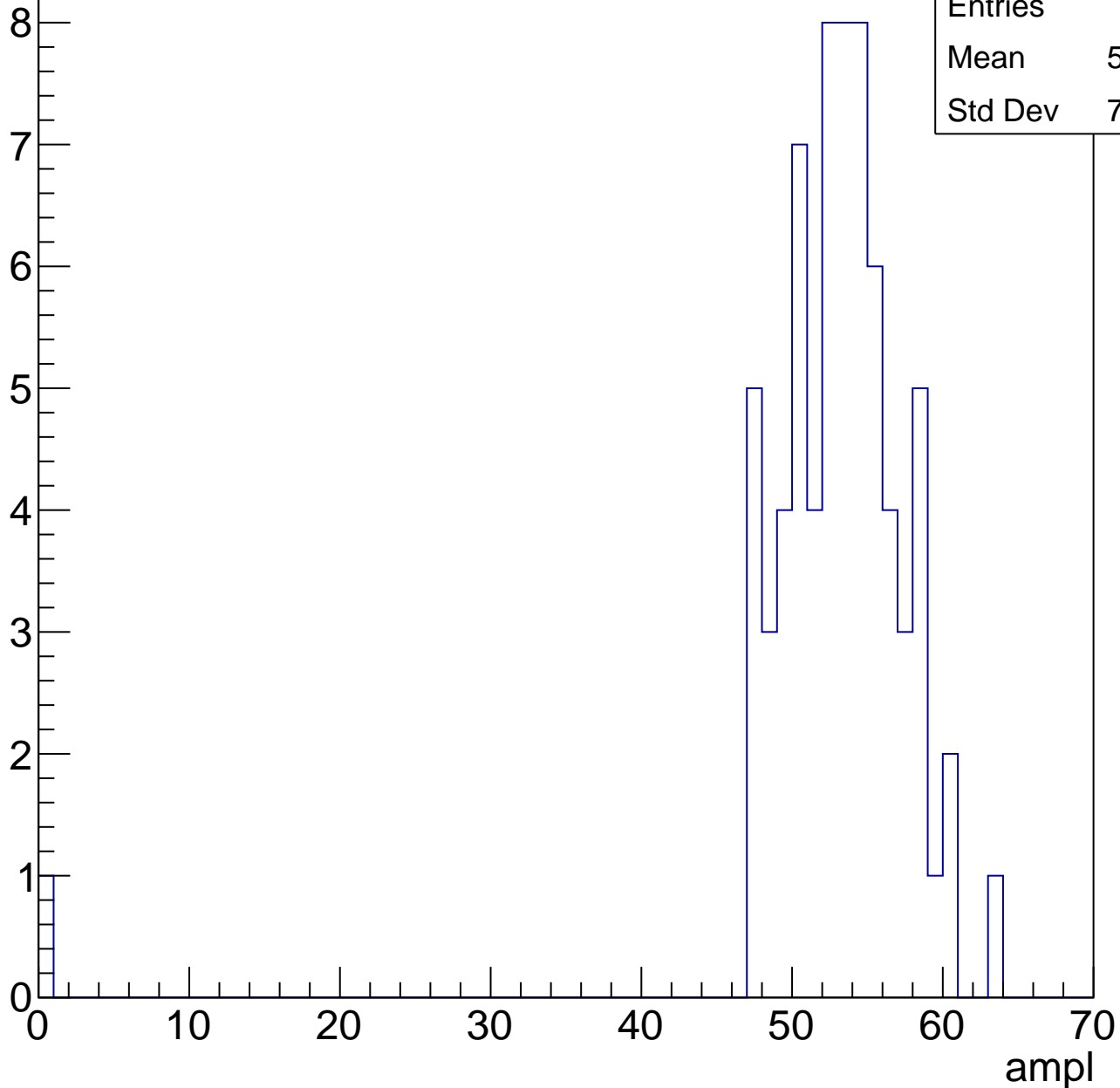


# B1L103S, U4-ch102, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 70    |
| Mean    | 52.26 |
| Std Dev | 7.222 |

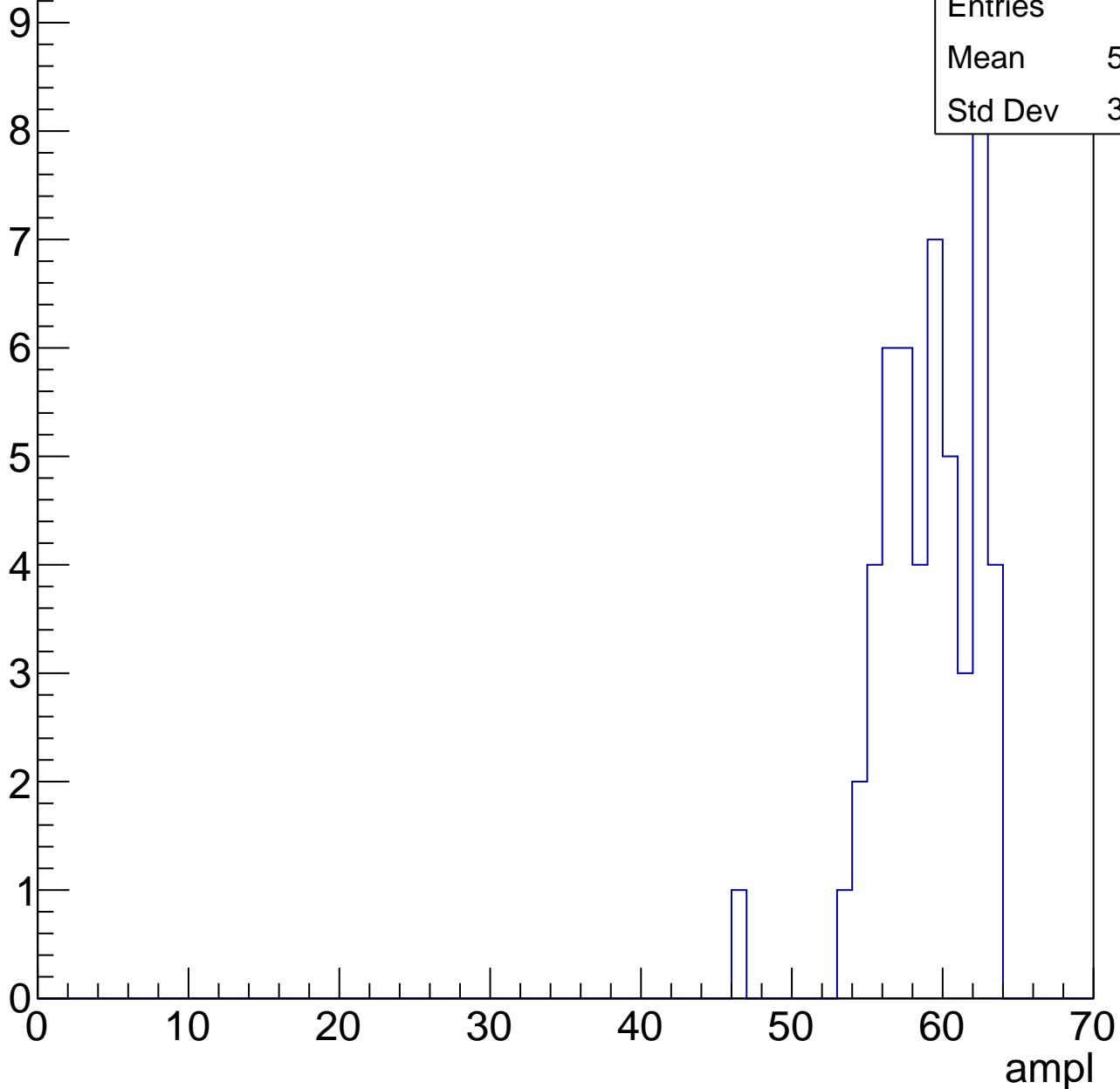


# B1L103S, U4-ch102, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 52    |
| Mean    | 58.52 |
| Std Dev | 3.255 |

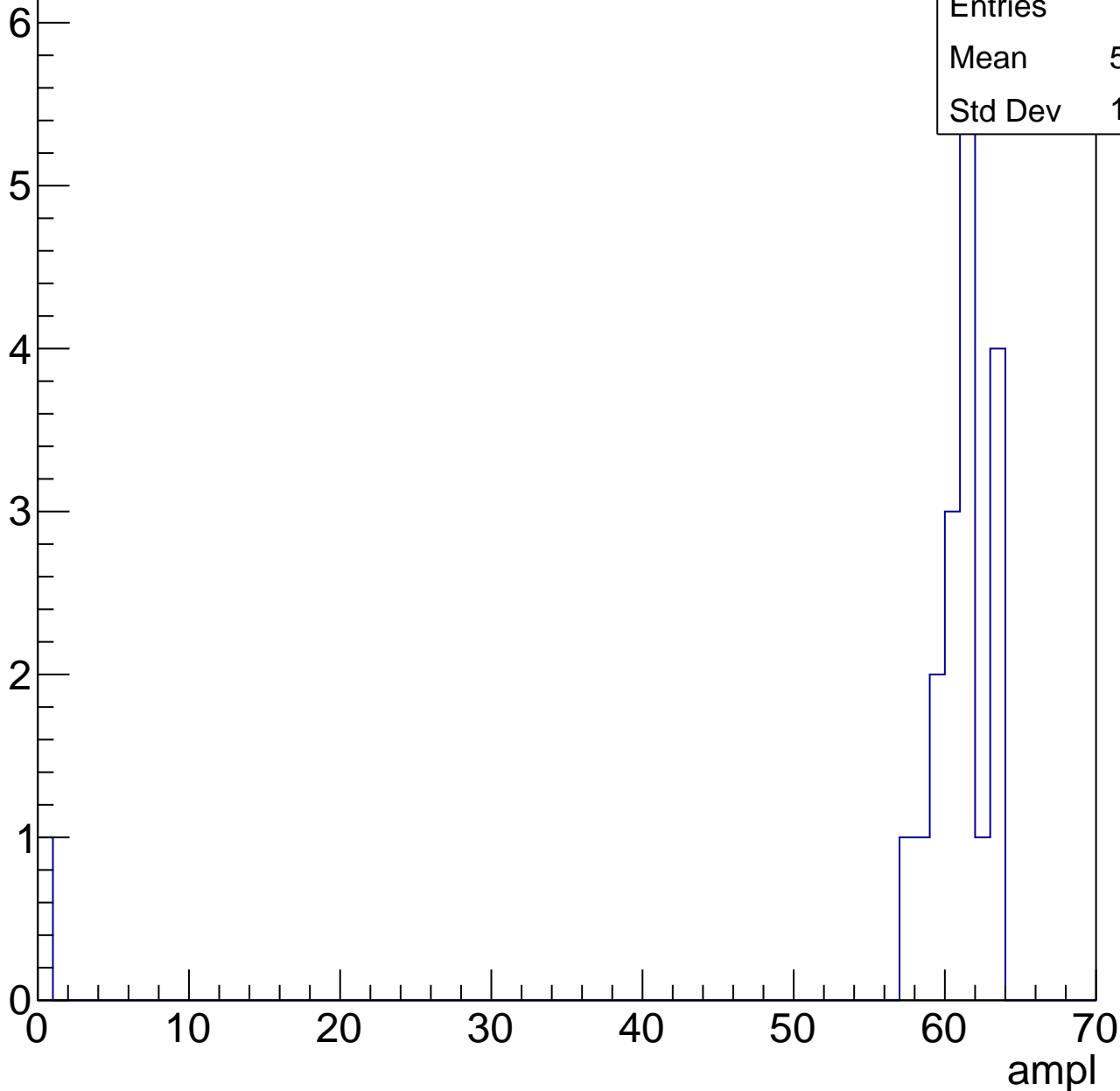


# B1L103S, U4-ch102, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 19    |
| Mean    | 57.53 |
| Std Dev | 13.66 |





# B1L103S, U4-ch102, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 21    |
| Mean    | 5.905 |
| Std Dev | 18.2  |

Entry



# B1L103S, U4-ch103, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 88    |
| Mean    | 25.32 |
| Std Dev | 8.224 |

Entry

10  
8  
6  
4  
2  
0

ampl

0

10

20

30

40

50

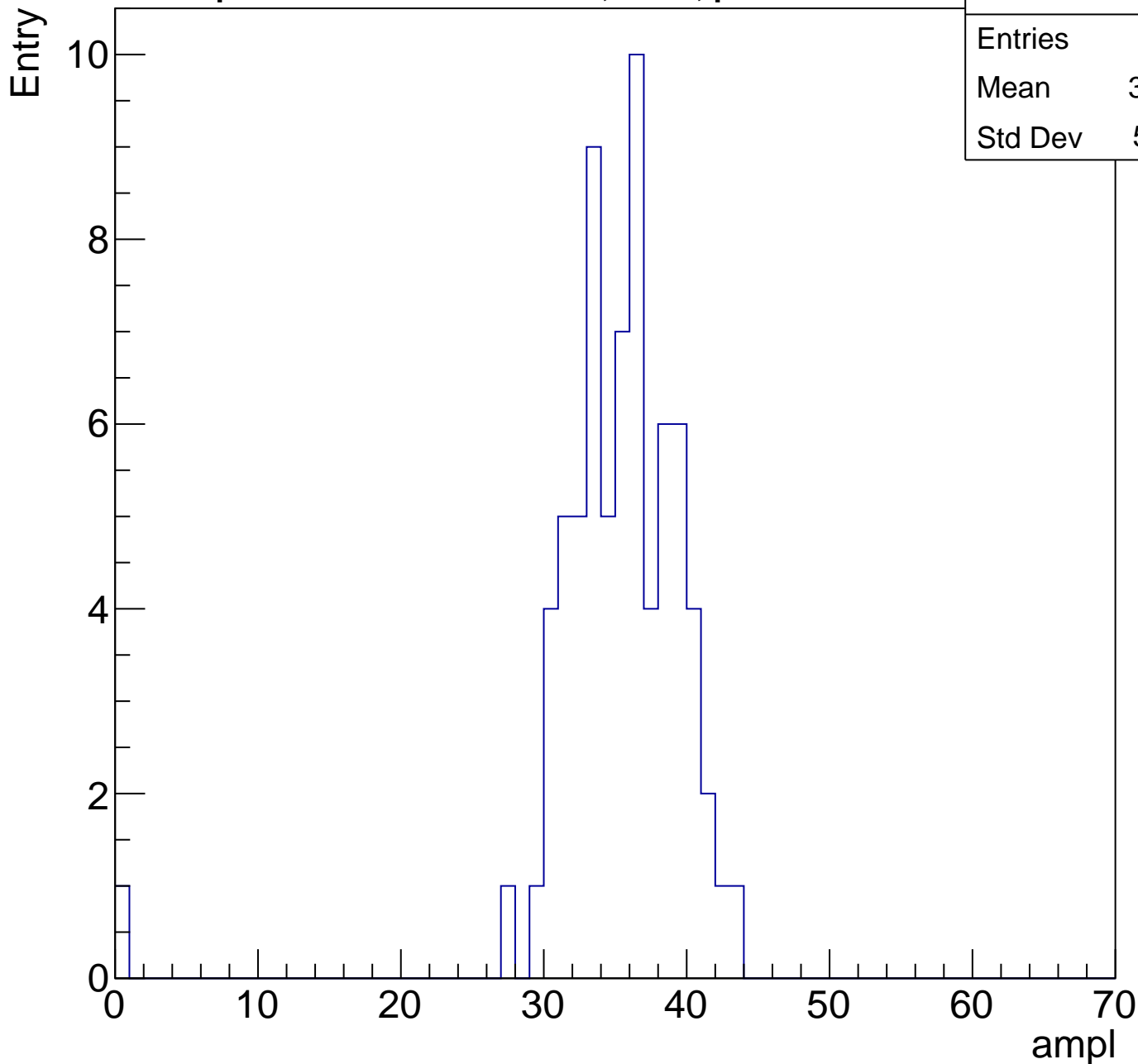
60

70

# B1L103S, U4-ch103, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 72    |
| Mean    | 34.72 |
| Std Dev | 5.331 |

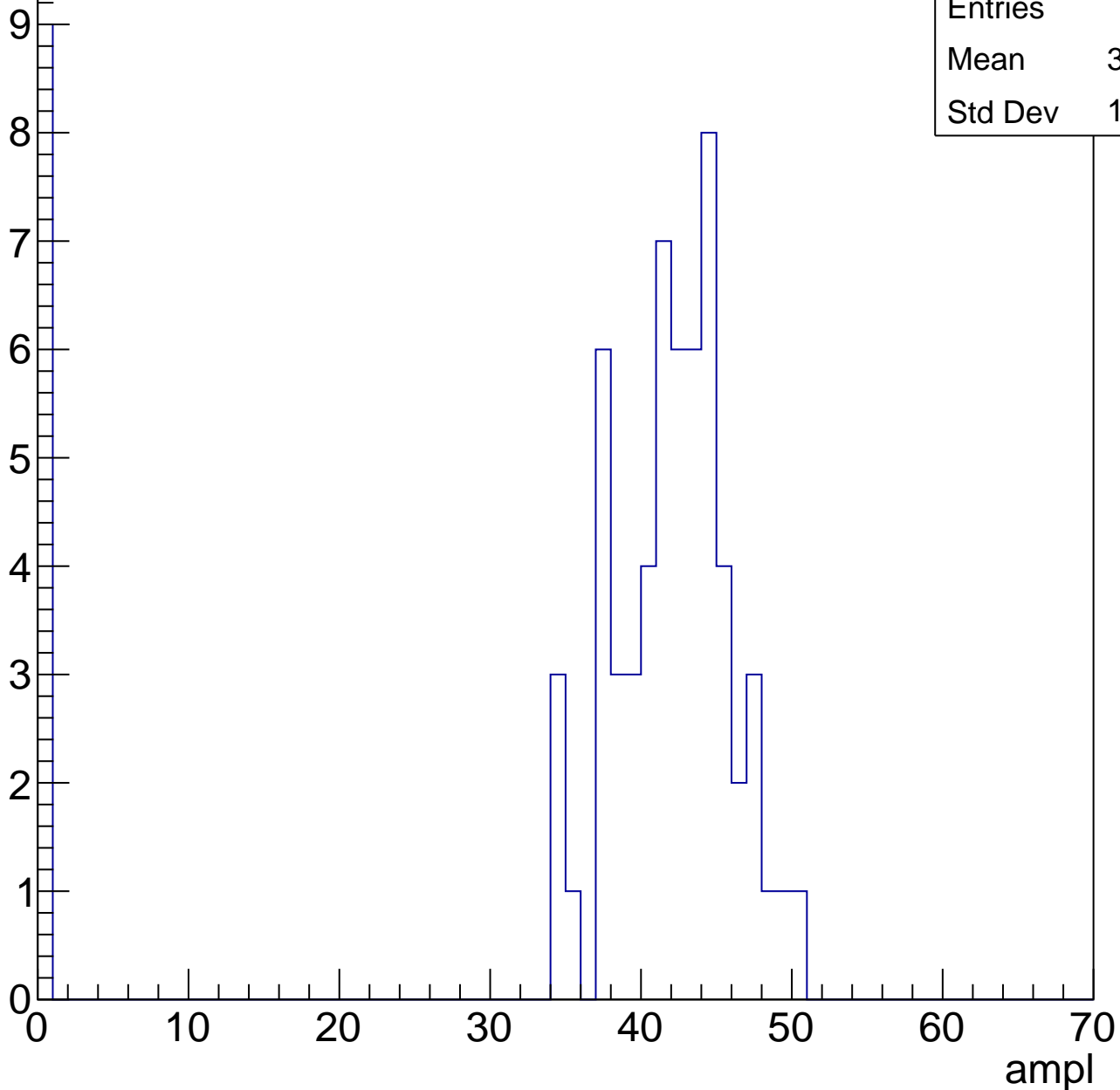


# B1L103S, U4-ch103, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 68    |
| Mean    | 36.16 |
| Std Dev | 14.54 |

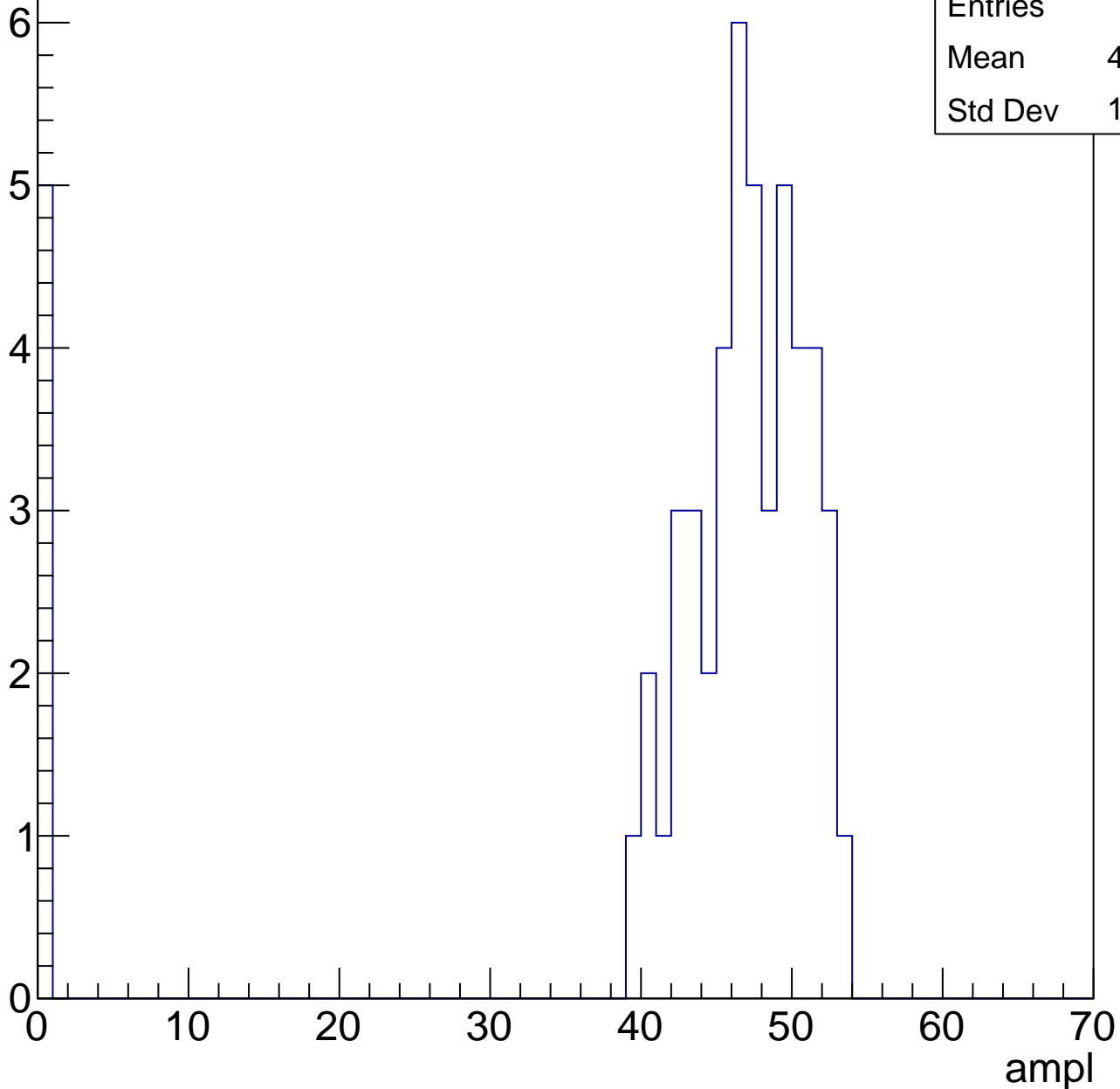


# B1L103S, U4-ch103, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 52    |
| Mean    | 42.23 |
| Std Dev | 14.18 |

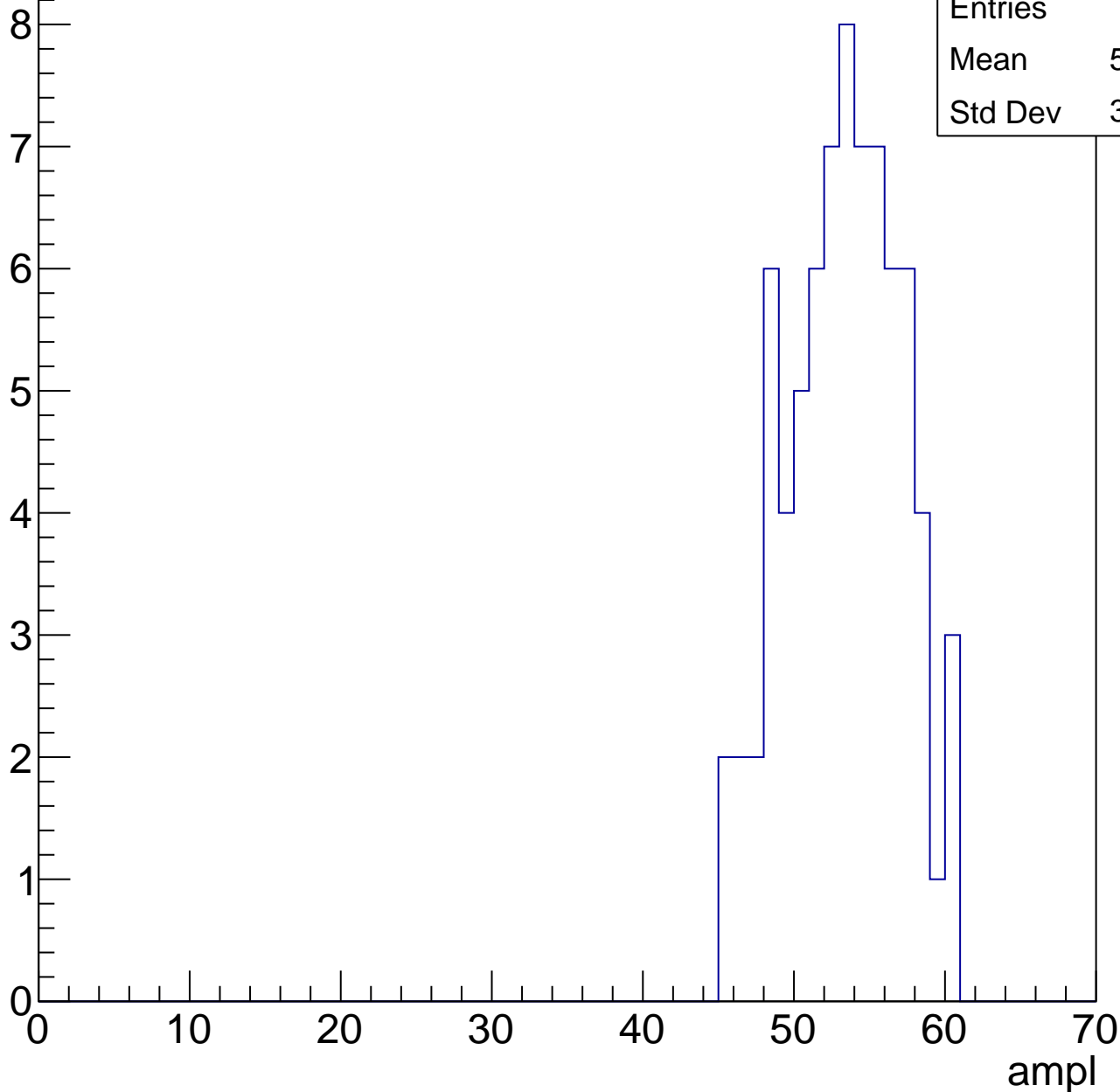


# B1L103S, U4-ch103, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 76    |
| Mean    | 52.84 |
| Std Dev | 3.724 |

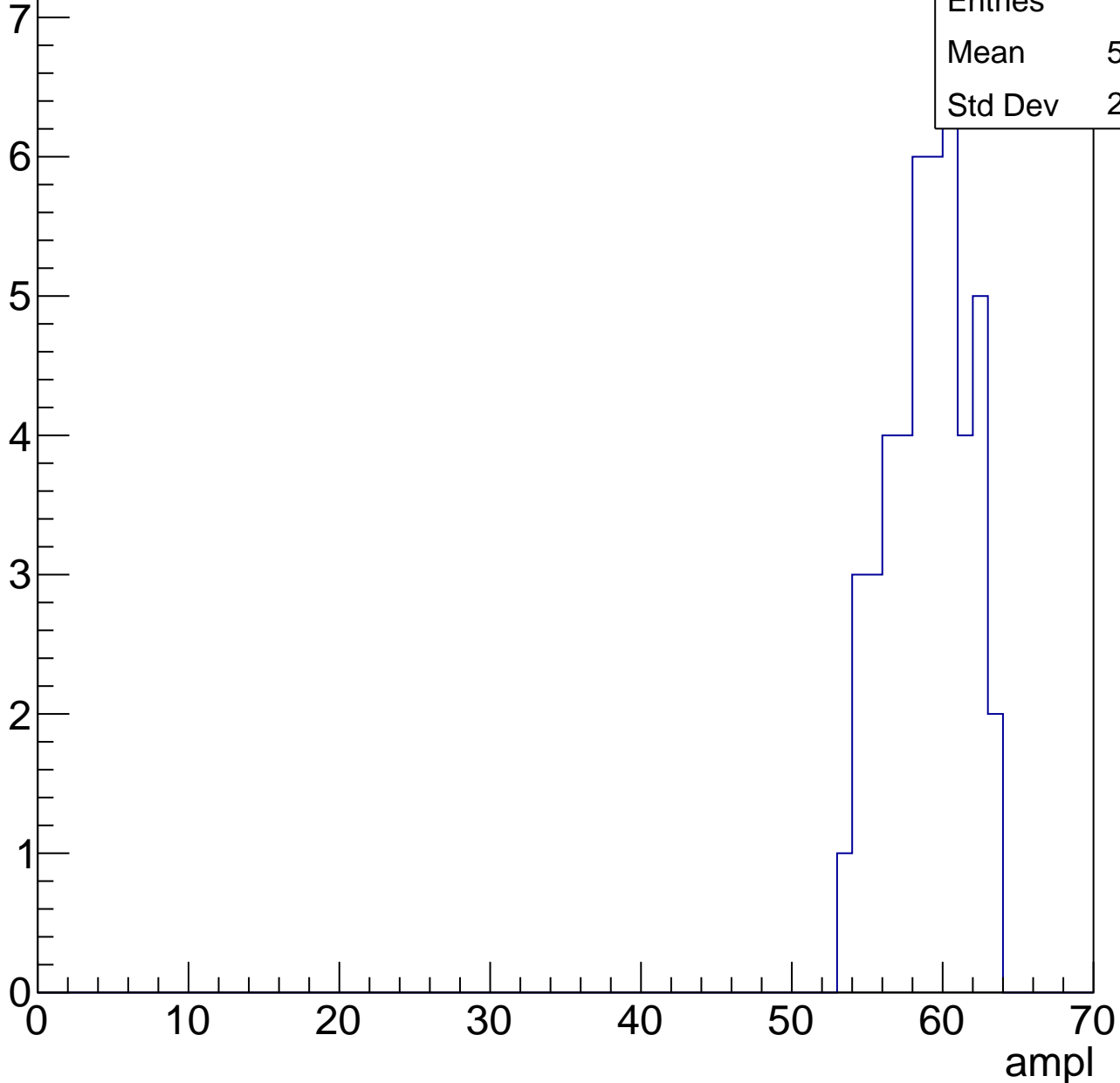


# B1L103S, U4-ch103, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 45    |
| Mean    | 58.53 |
| Std Dev | 2.613 |

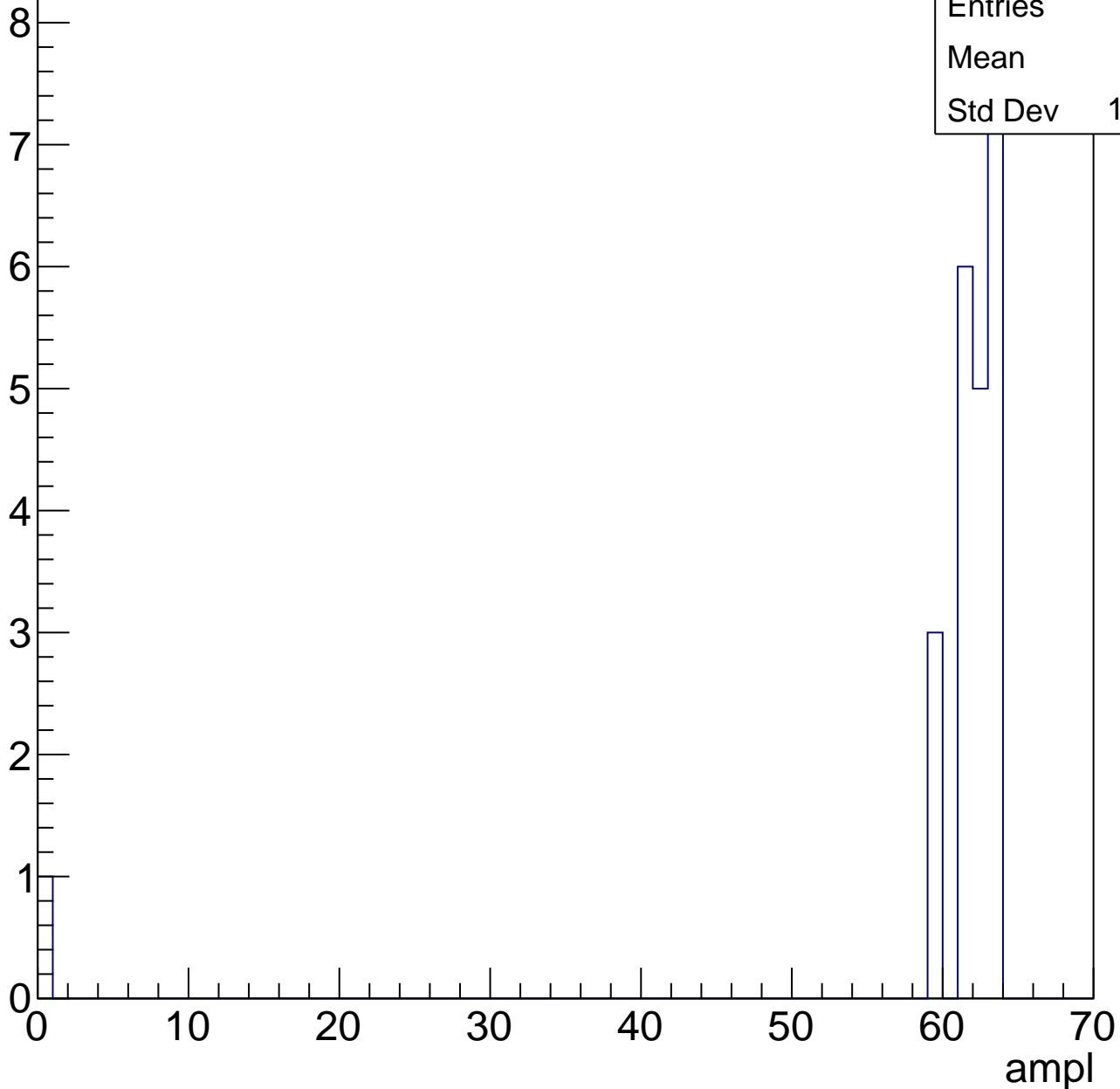


# B1L103S, U4-ch103, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 23    |
| Mean    | 59    |
| Std Dev | 12.65 |





# B1L103S, U4-ch103, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

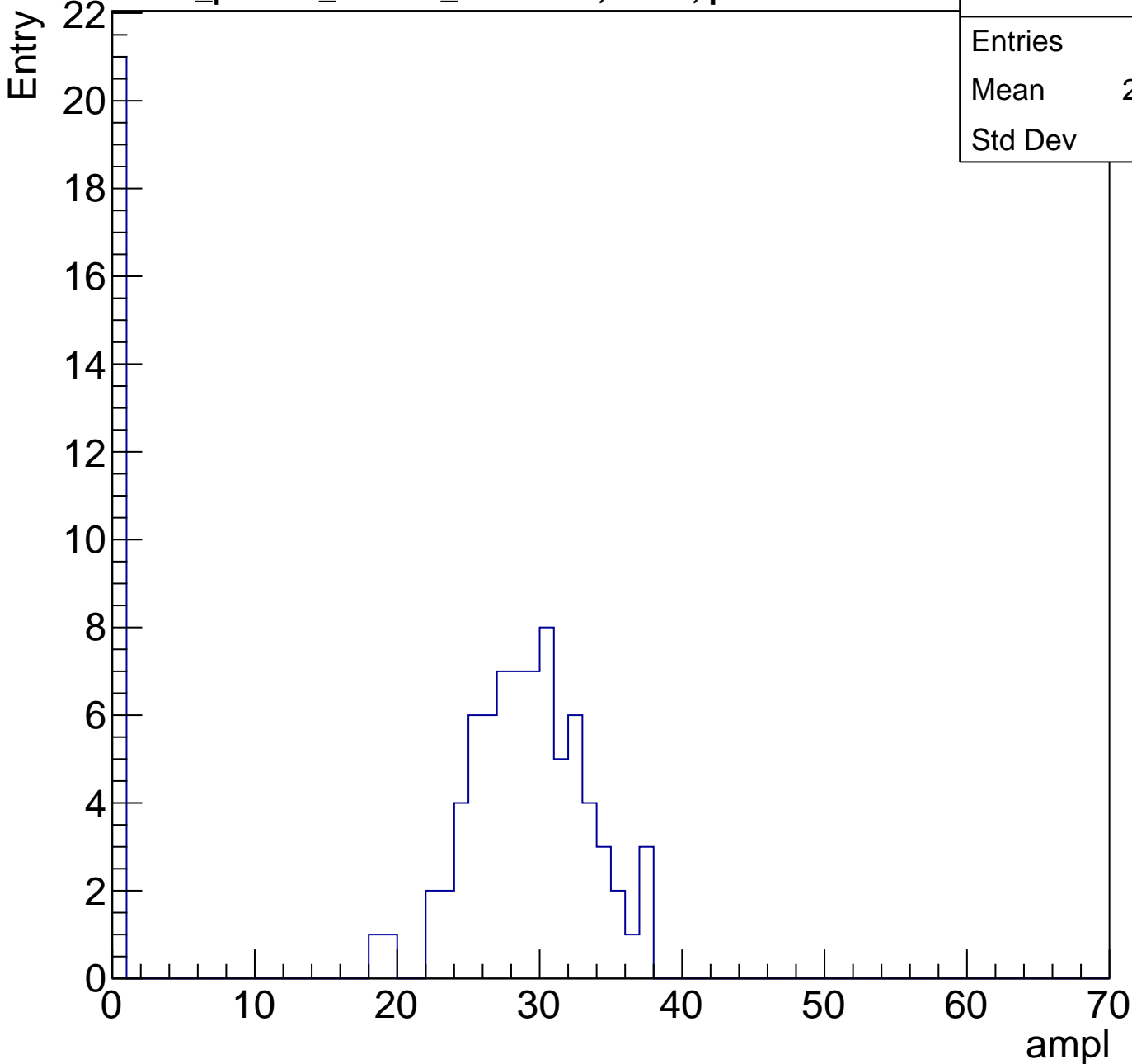
ampl

|         |    |
|---------|----|
| Entries | 19 |
| Mean    | 0  |
| Std Dev | 0  |

# B1L103S, U4-ch104, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 96    |
| Mean    | 22.45 |
| Std Dev | 12.4  |



# B1L103S, U4-ch104, adc1

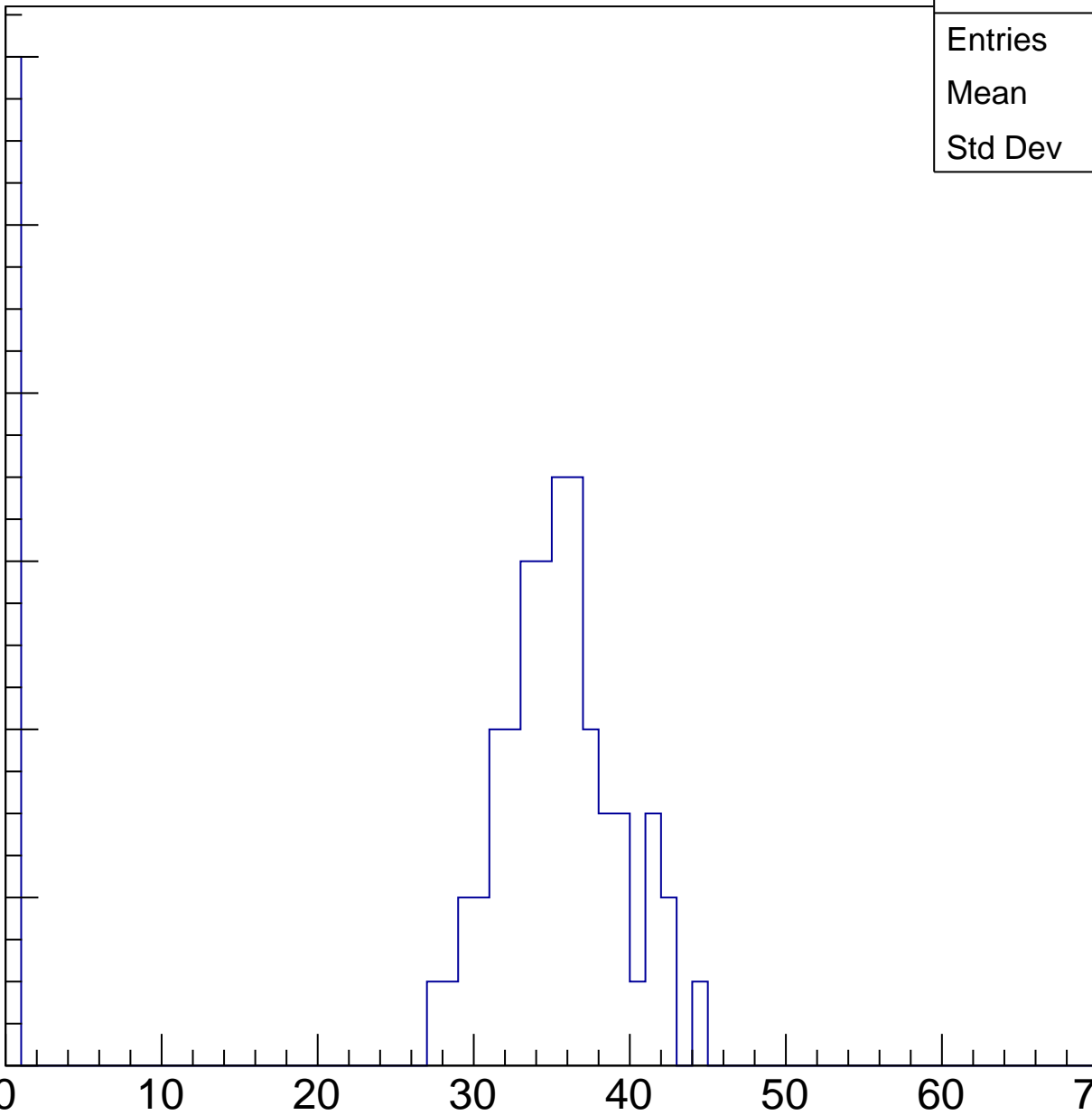
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

12  
10  
8  
6  
4  
2  
0

|         |       |
|---------|-------|
| Entries | 69    |
| Mean    | 28.9  |
| Std Dev | 13.68 |

ampl

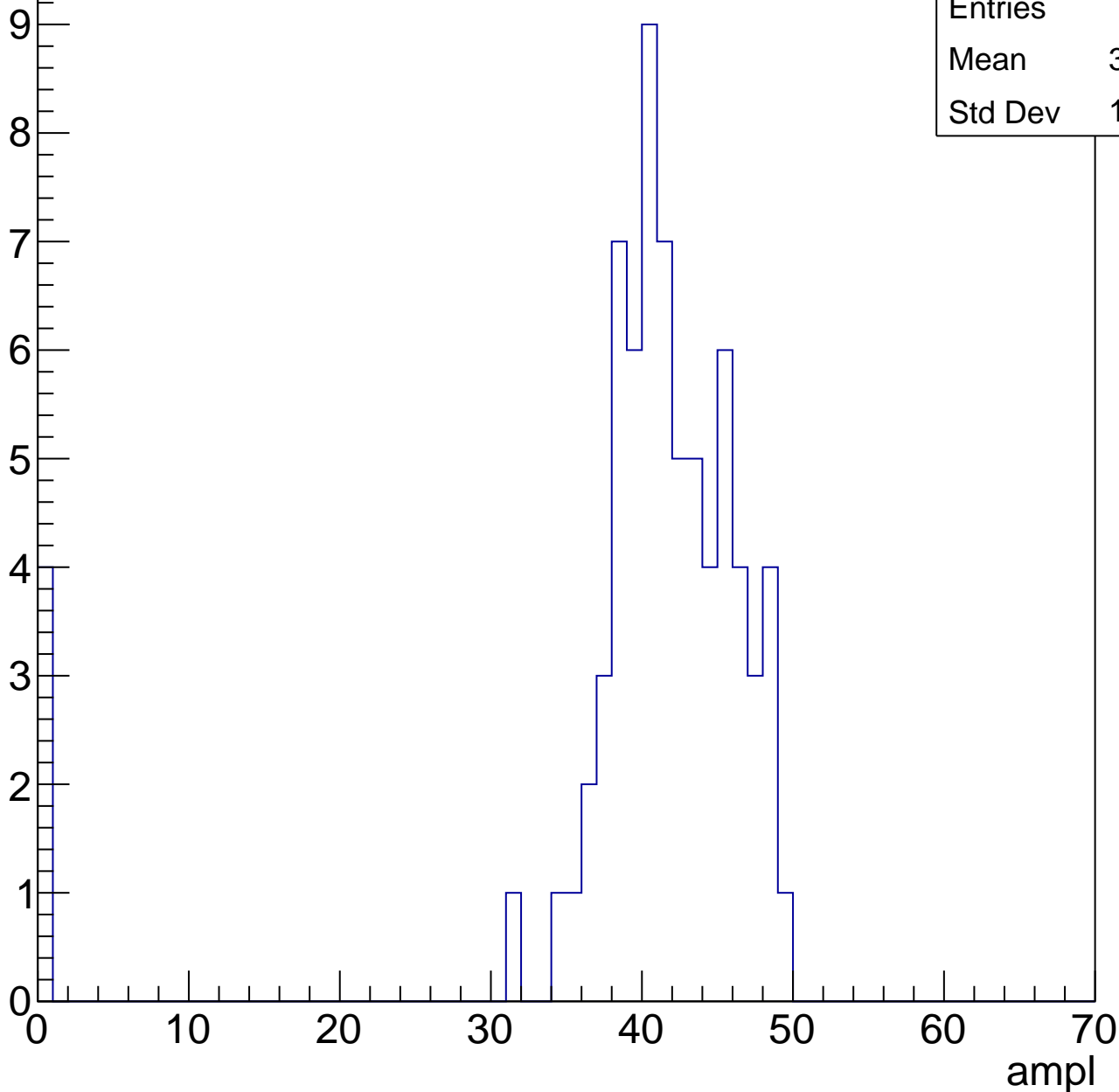


# B1L103S, U4-ch104, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 73    |
| Mean    | 39.27 |
| Std Dev | 10.14 |

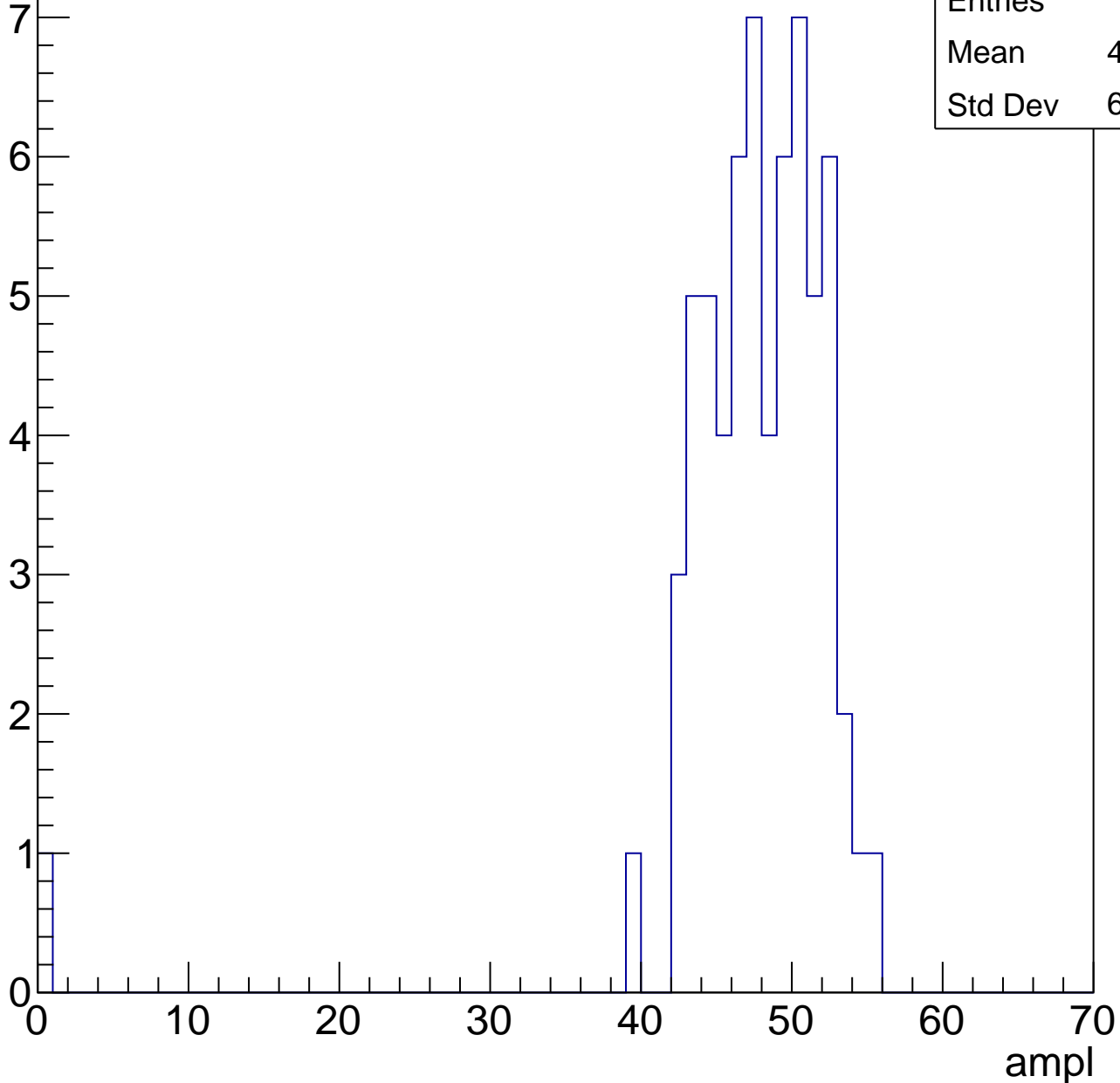


# B1L103S, U4-ch104, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

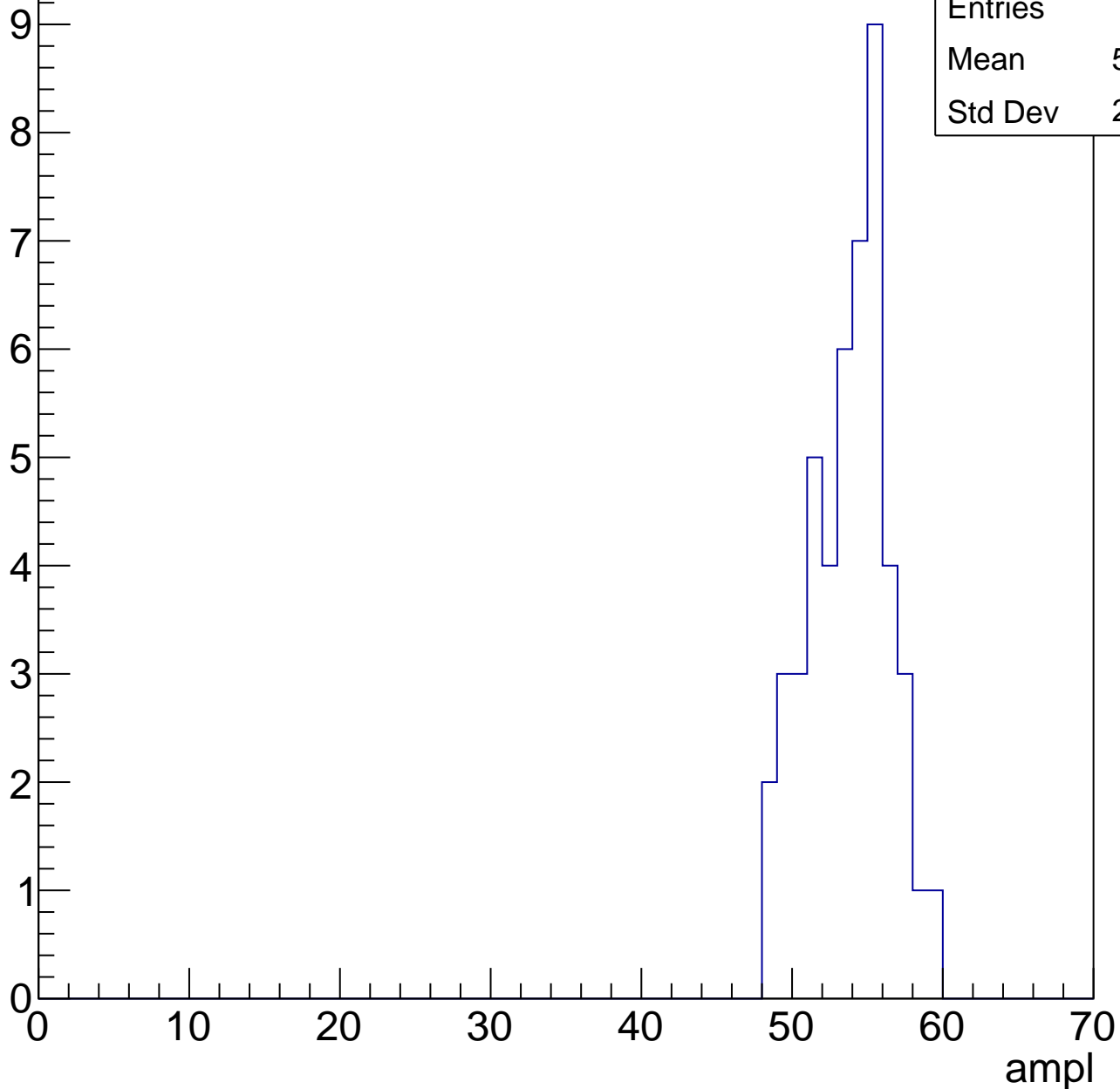
|         |       |
|---------|-------|
| Entries | 64    |
| Mean    | 46.92 |
| Std Dev | 6.847 |



# B1L103S, U4-ch104, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

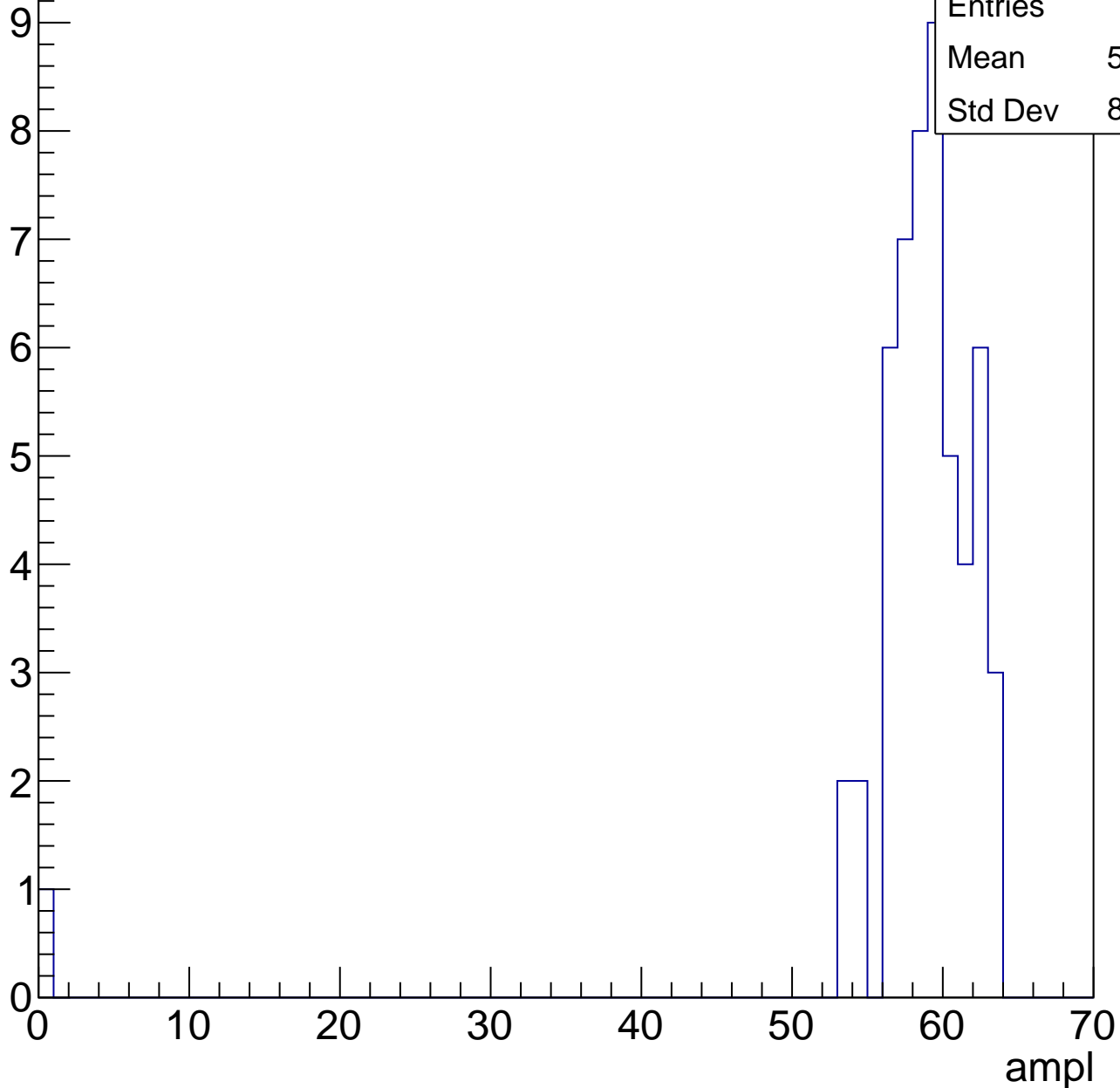
Entry



# B1L103S, U4-ch104, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

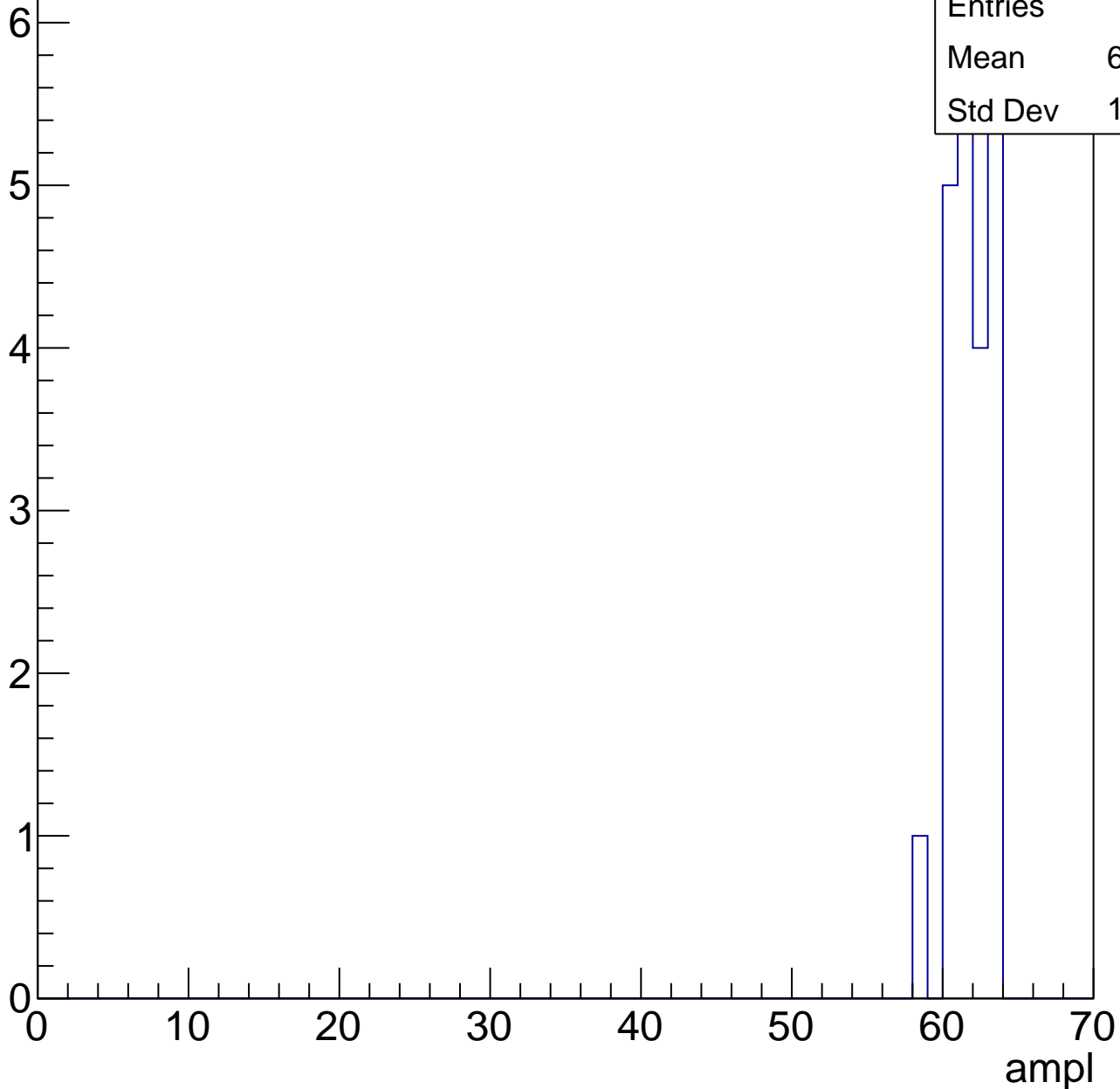


# B1L103S, U4-ch104, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 22    |
| Mean    | 61.36 |
| Std Dev | 1.333 |





# B1L103S, U4-ch104, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

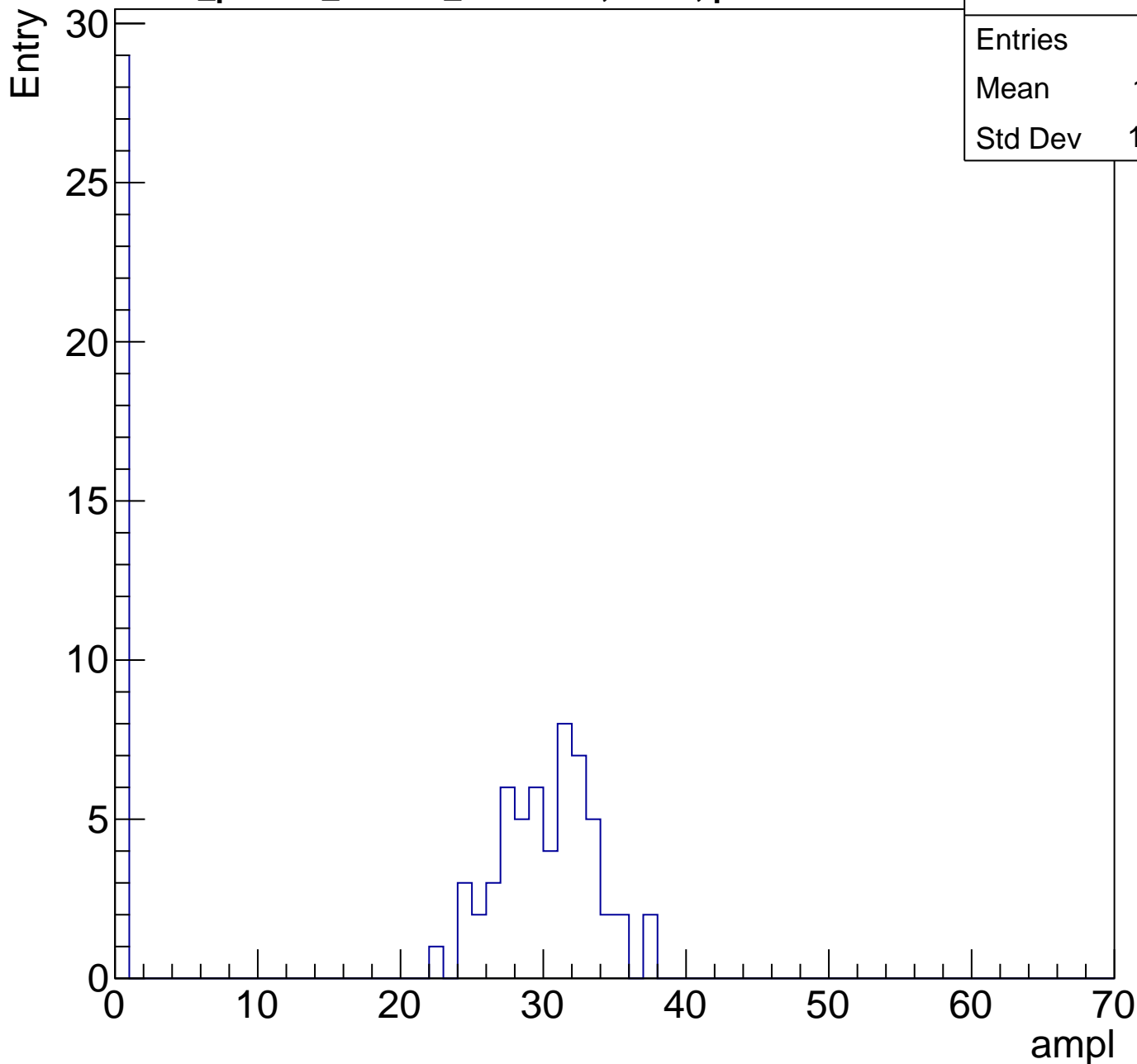
|         |       |
|---------|-------|
| Entries | 20    |
| Mean    | 3.15  |
| Std Dev | 13.73 |



# B1L103S, U4-ch105, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

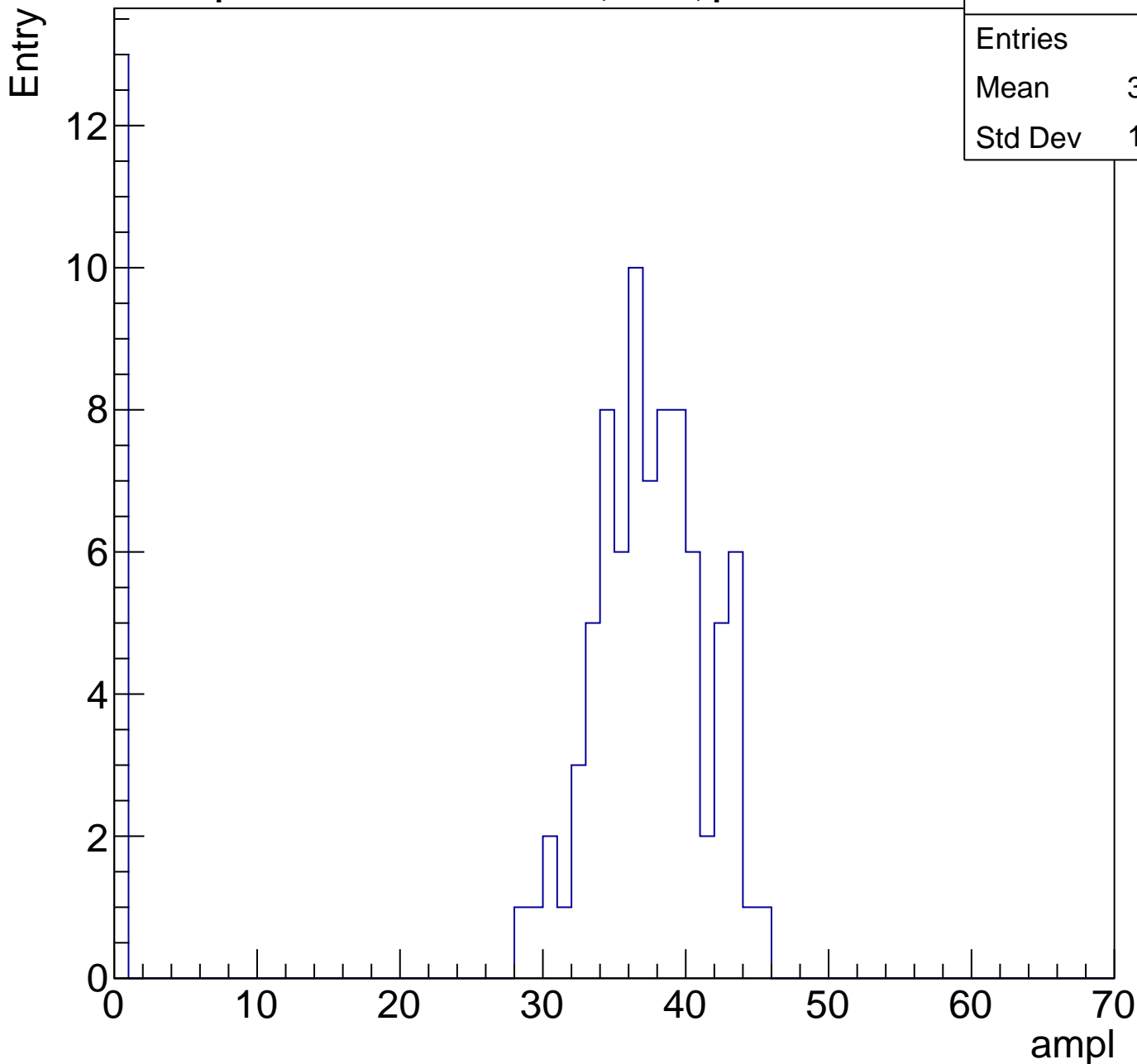
|         |       |
|---------|-------|
| Entries | 85    |
| Mean    | 19.61 |
| Std Dev | 14.36 |



# B1L103S, U4-ch105, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 94    |
| Mean    | 31.97 |
| Std Dev | 13.26 |

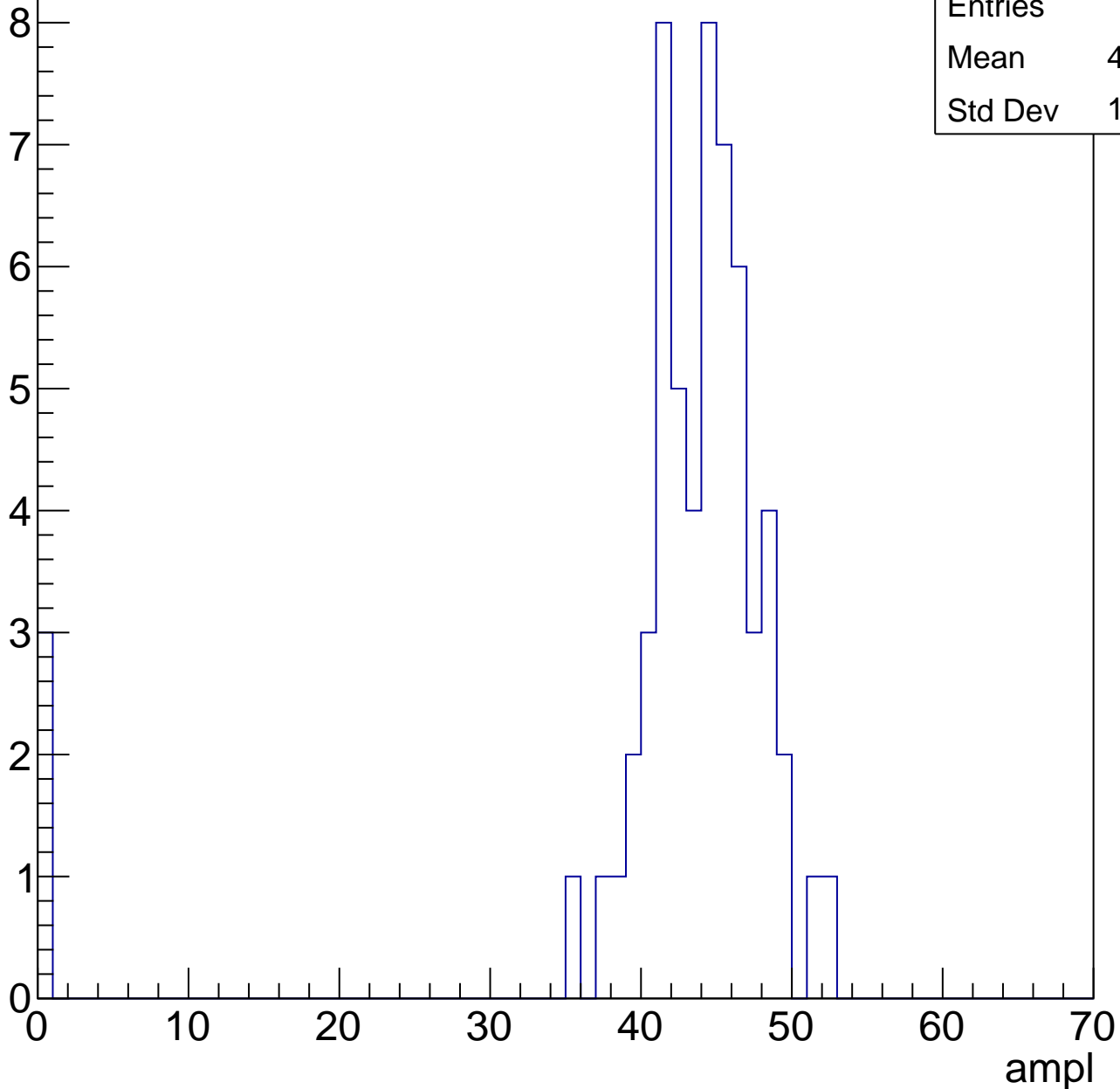


# B1L103S, U4-ch105, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 60    |
| Mean    | 41.58 |
| Std Dev | 10.09 |

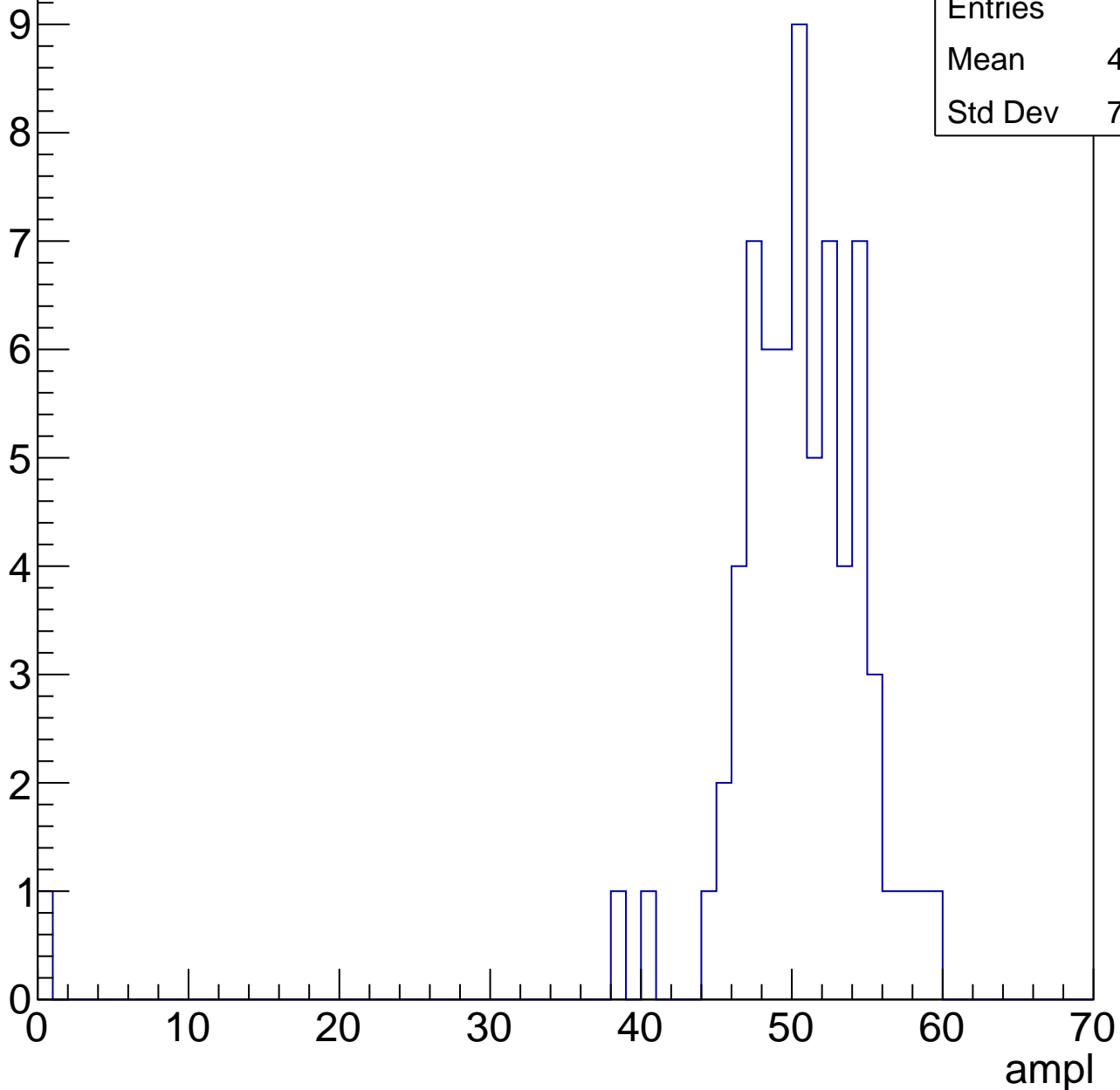


# B1L103S, U4-ch105, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

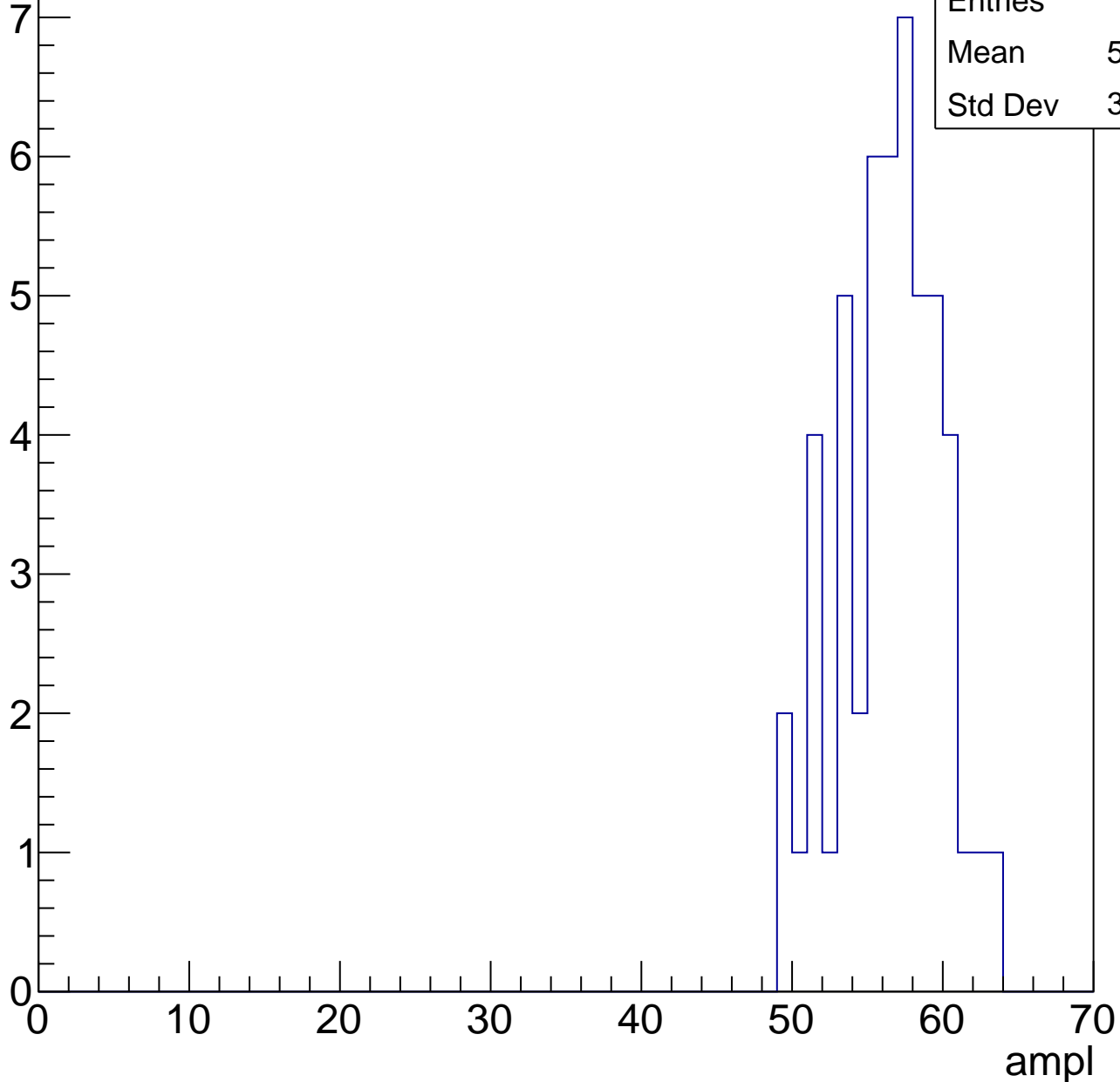
|         |       |
|---------|-------|
| Entries | 68    |
| Mean    | 49.43 |
| Std Dev | 7.124 |



# B1L103S, U4-ch105, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



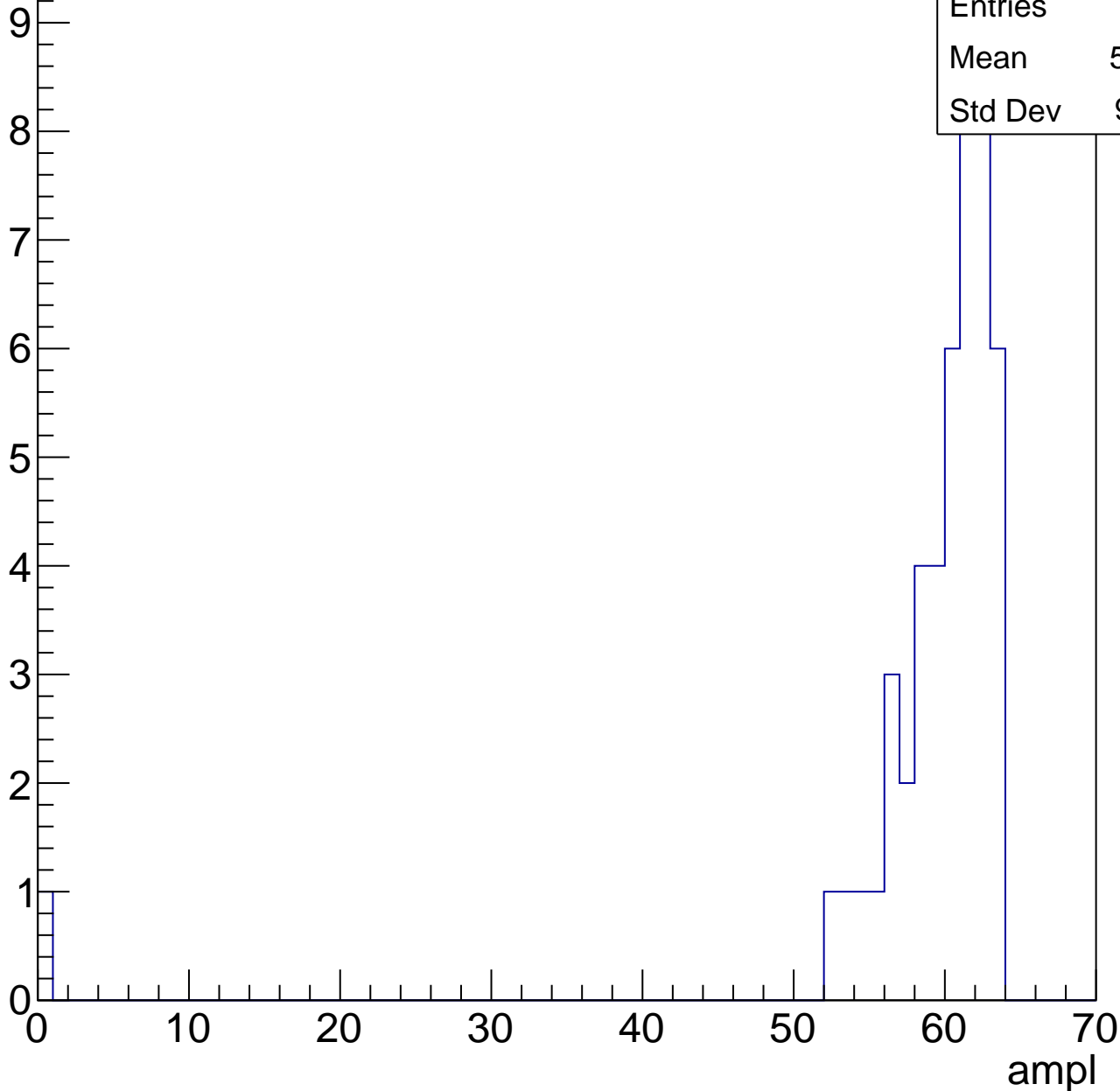
|         |       |
|---------|-------|
| Entries | 51    |
| Mean    | 55.94 |
| Std Dev | 3.298 |

# B1L103S, U4-ch105, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 47    |
| Mean    | 58.45 |
| Std Dev | 9.041 |



# B1L103S, U4-ch105, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U4-ch105, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 19    |
| Mean    | 1.053 |
| Std Dev | 4.466 |

Entry

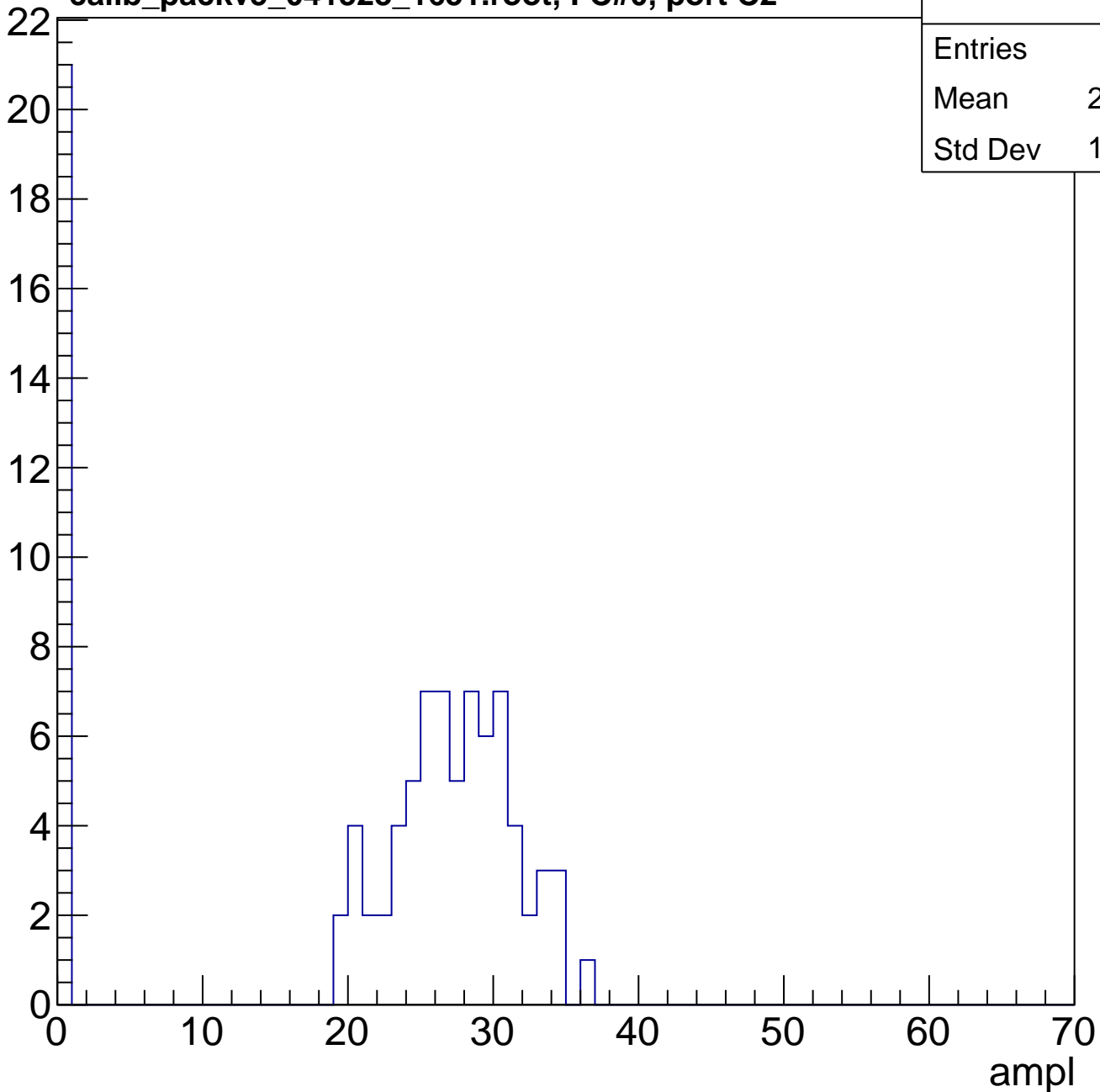


# B1L103S, U4-ch106, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 92    |
| Mean    | 20.79 |
| Std Dev | 11.84 |

Entry



# B1L103S, U4-ch106, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 89    |
| Mean    | 30.09 |
| Std Dev | 11.55 |

Entry

10  
8  
6  
4  
2  
0

0

10

20

30

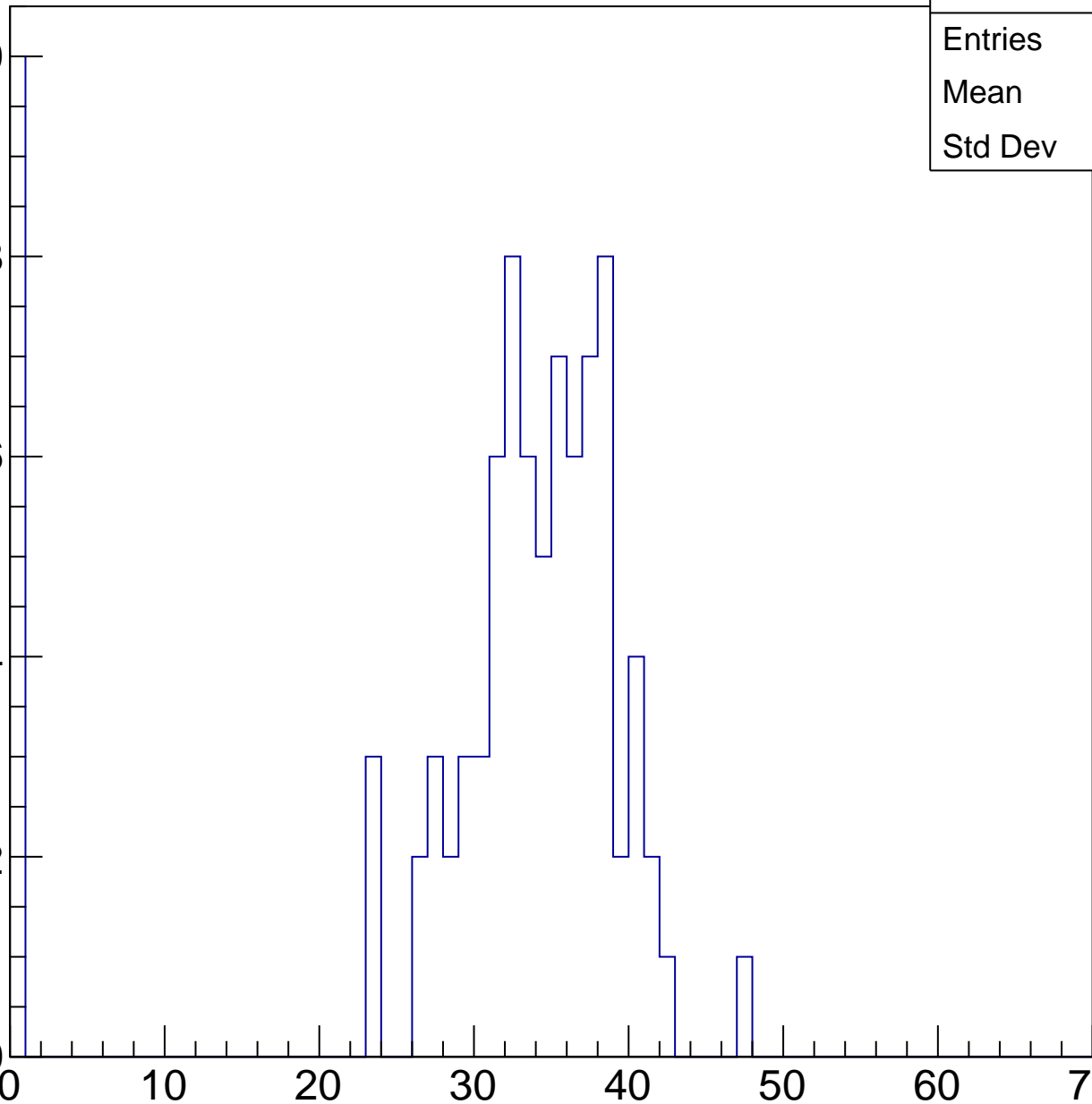
40

50

60

70

ampl

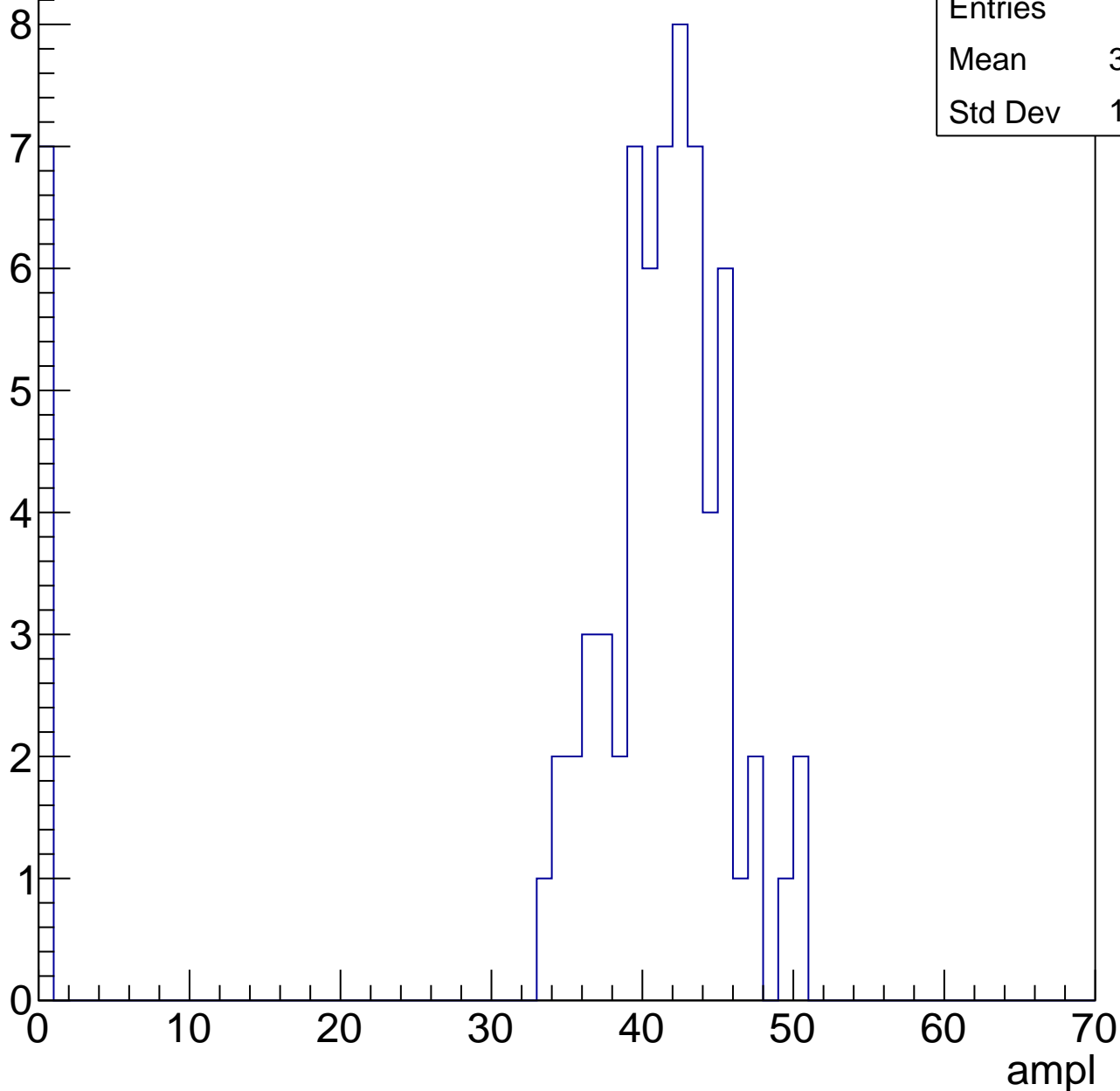


# B1L103S, U4-ch106, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 71    |
| Mean    | 37.15 |
| Std Dev | 12.79 |

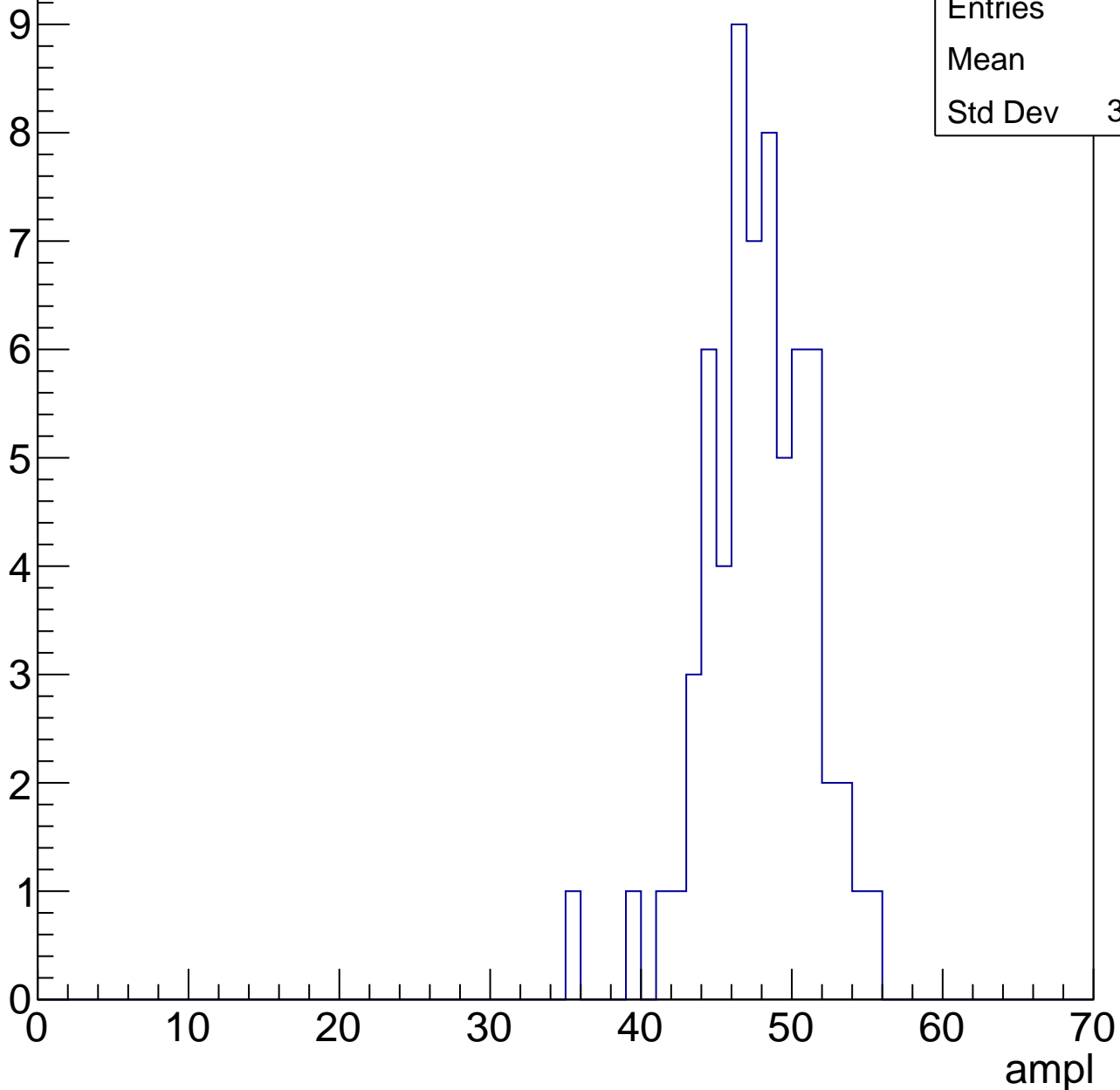


# B1L103S, U4-ch106, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 64    |
| Mean    | 47.3  |
| Std Dev | 3.543 |

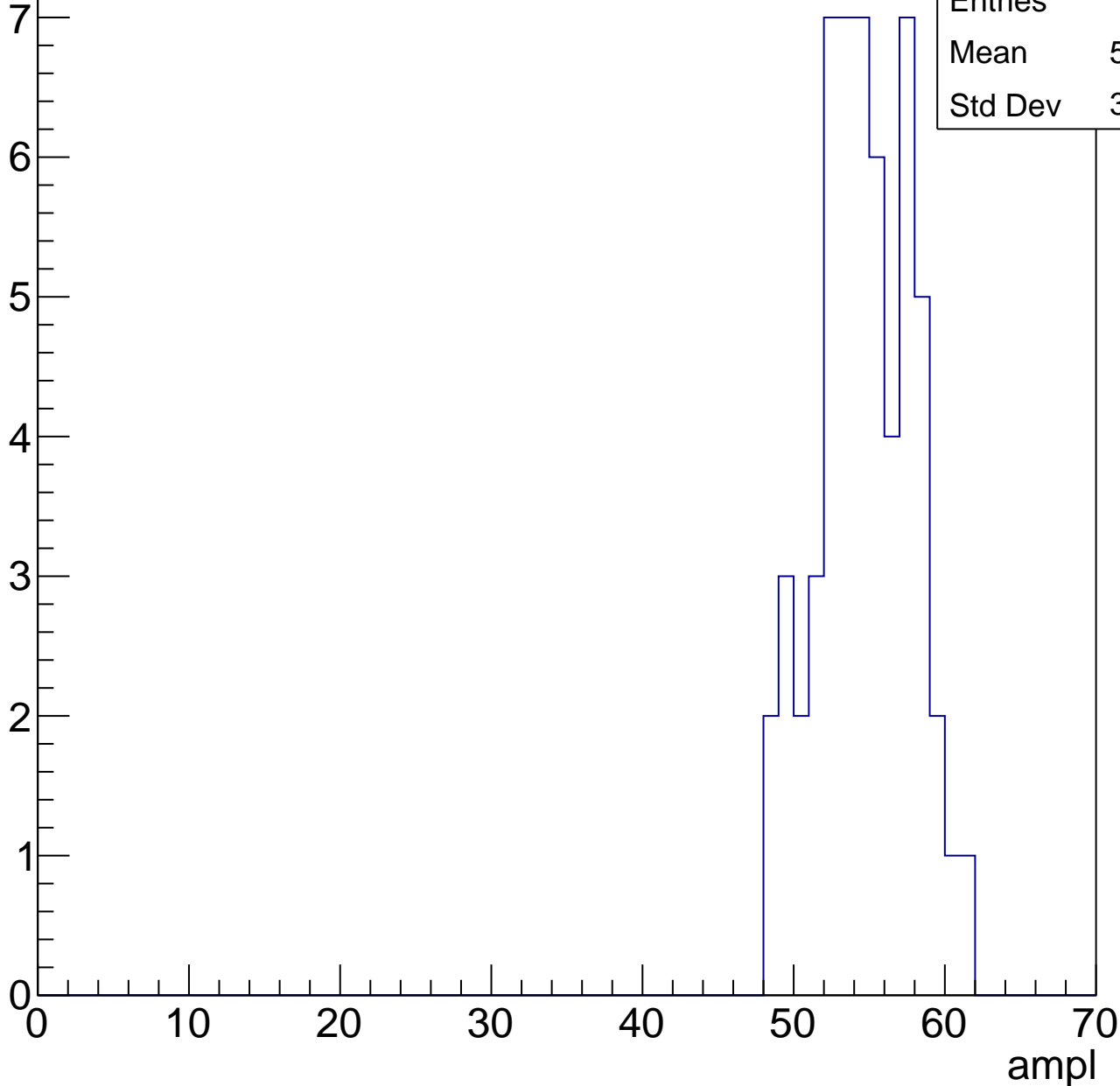


# B1L103S, U4-ch106, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

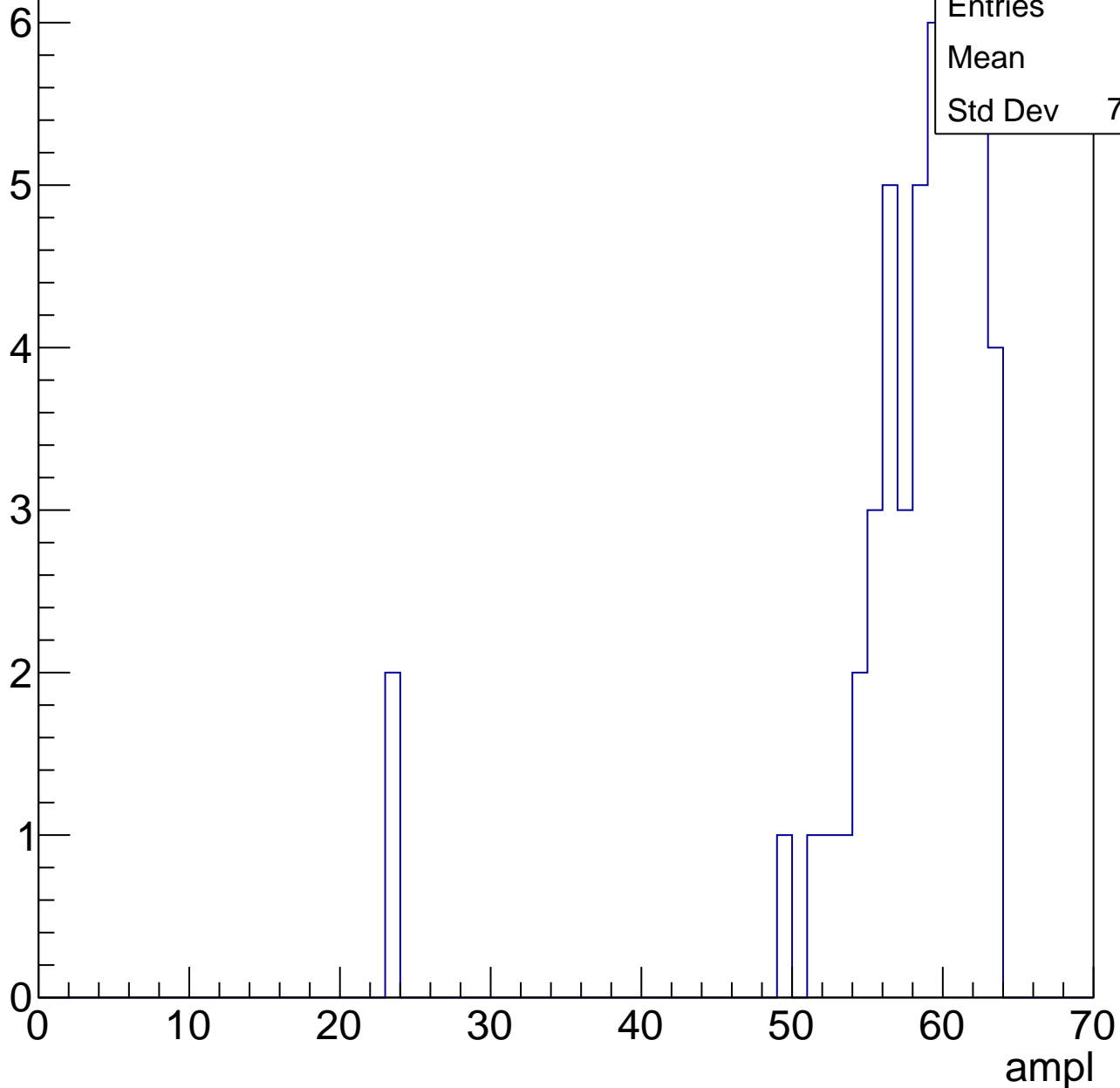
|         |       |
|---------|-------|
| Entries | 57    |
| Mean    | 54.23 |
| Std Dev | 3.072 |



# B1L103S, U4-ch106, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

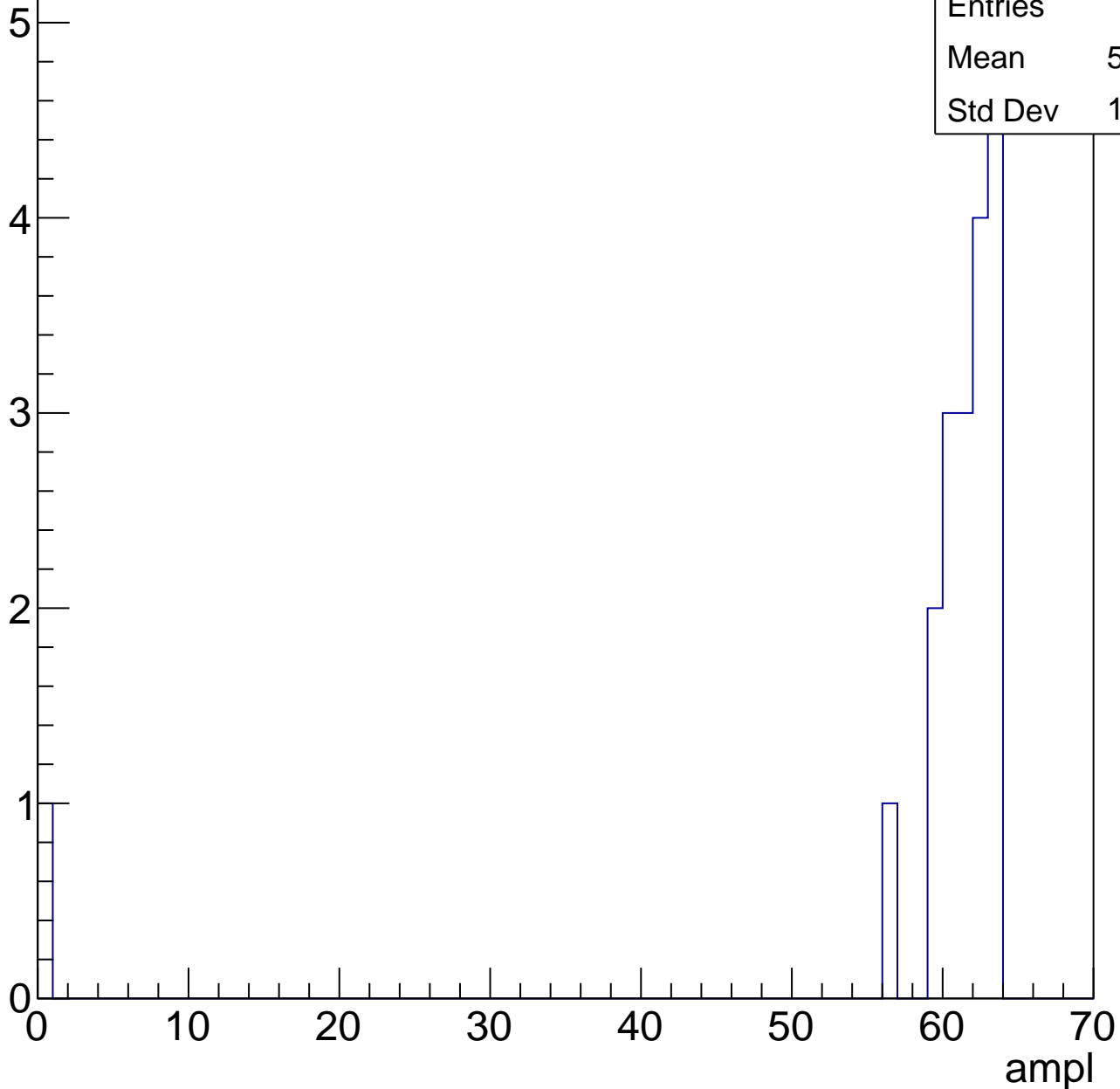


# B1L103S, U4-ch106, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 19    |
| Mean    | 57.89 |
| Std Dev | 13.76 |





# B1L103S, U4-ch106, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

|         |       |
|---------|-------|
| Entries | 19    |
| Mean    | 3.316 |
| Std Dev | 14.07 |

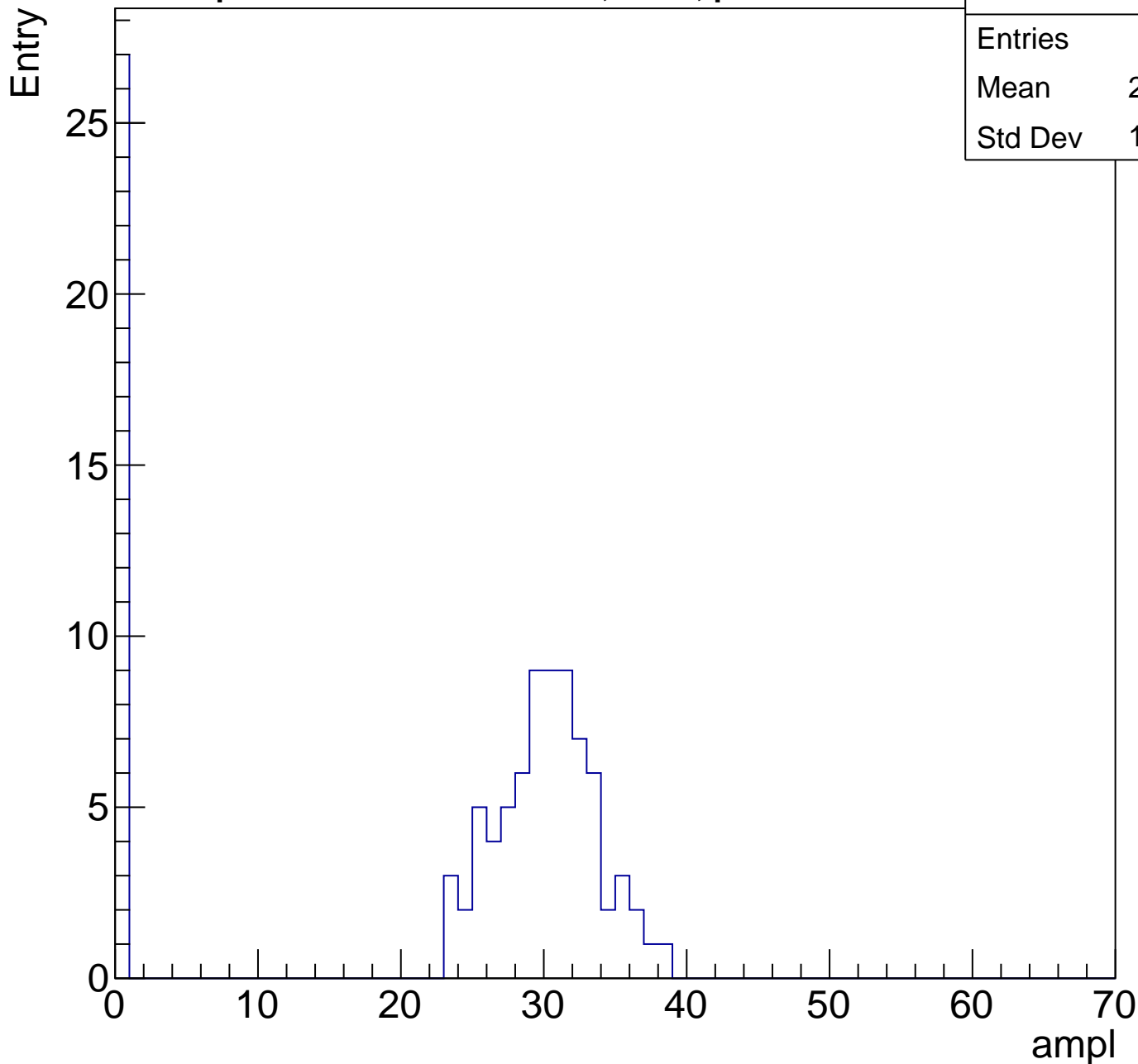
ampl

0 10 20 30 40 50 60 70

# B1L103S, U4-ch107, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

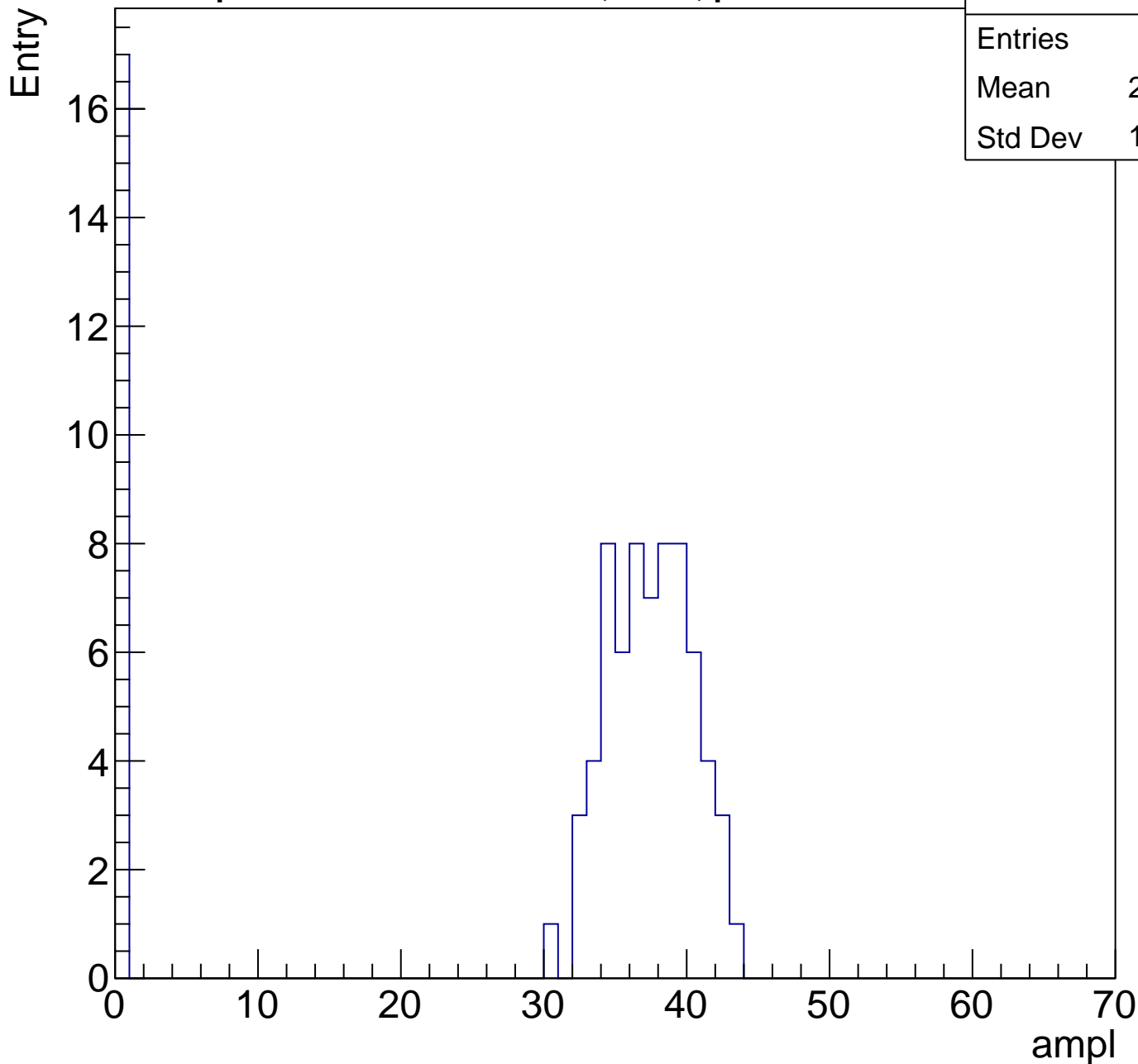
|         |       |
|---------|-------|
| Entries | 101   |
| Mean    | 21.79 |
| Std Dev | 13.48 |



# B1L103S, U4-ch107, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 84    |
| Mean    | 29.48 |
| Std Dev | 15.07 |

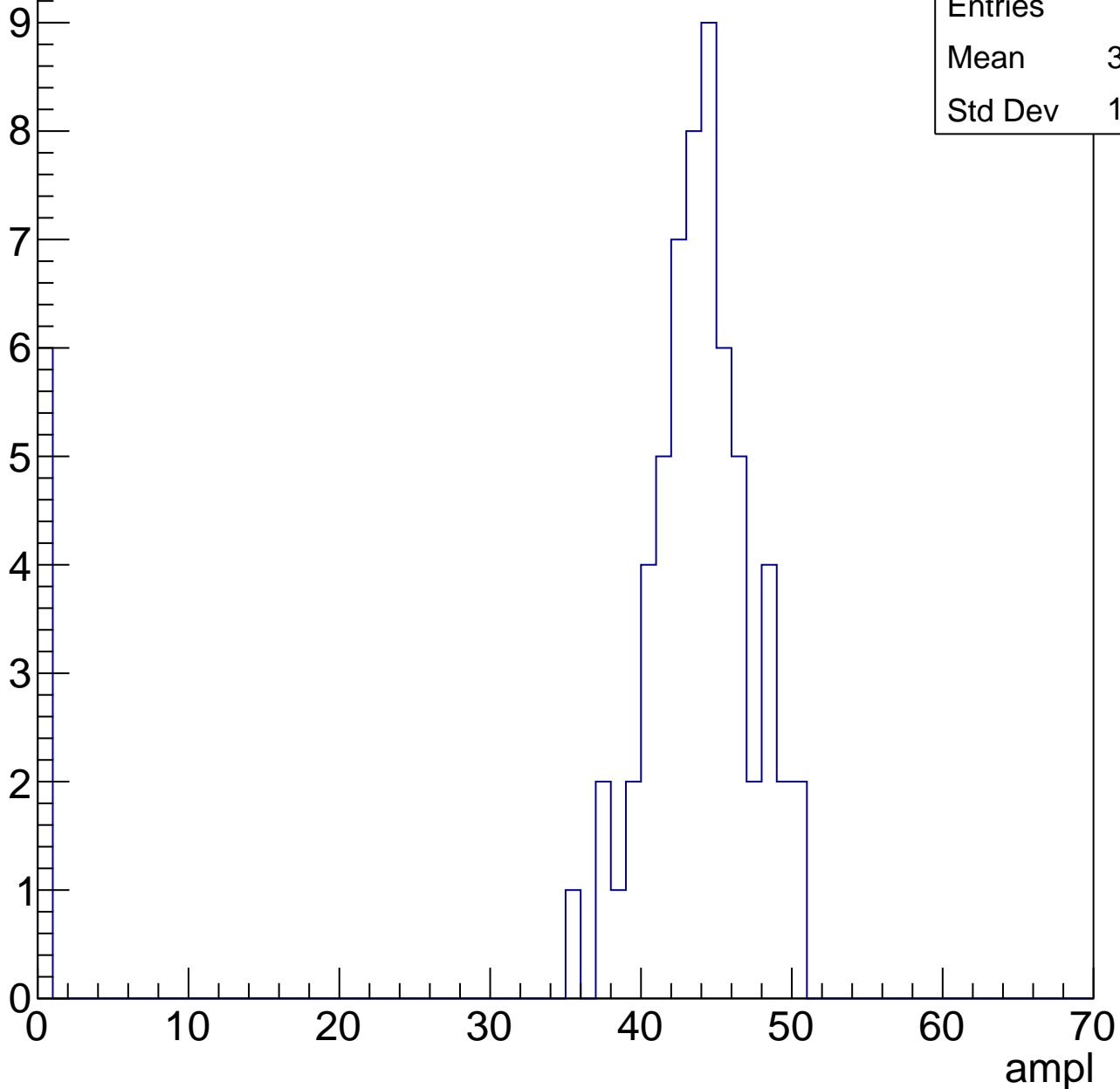


# B1L103S, U4-ch107, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 66    |
| Mean    | 39.52 |
| Std Dev | 12.87 |

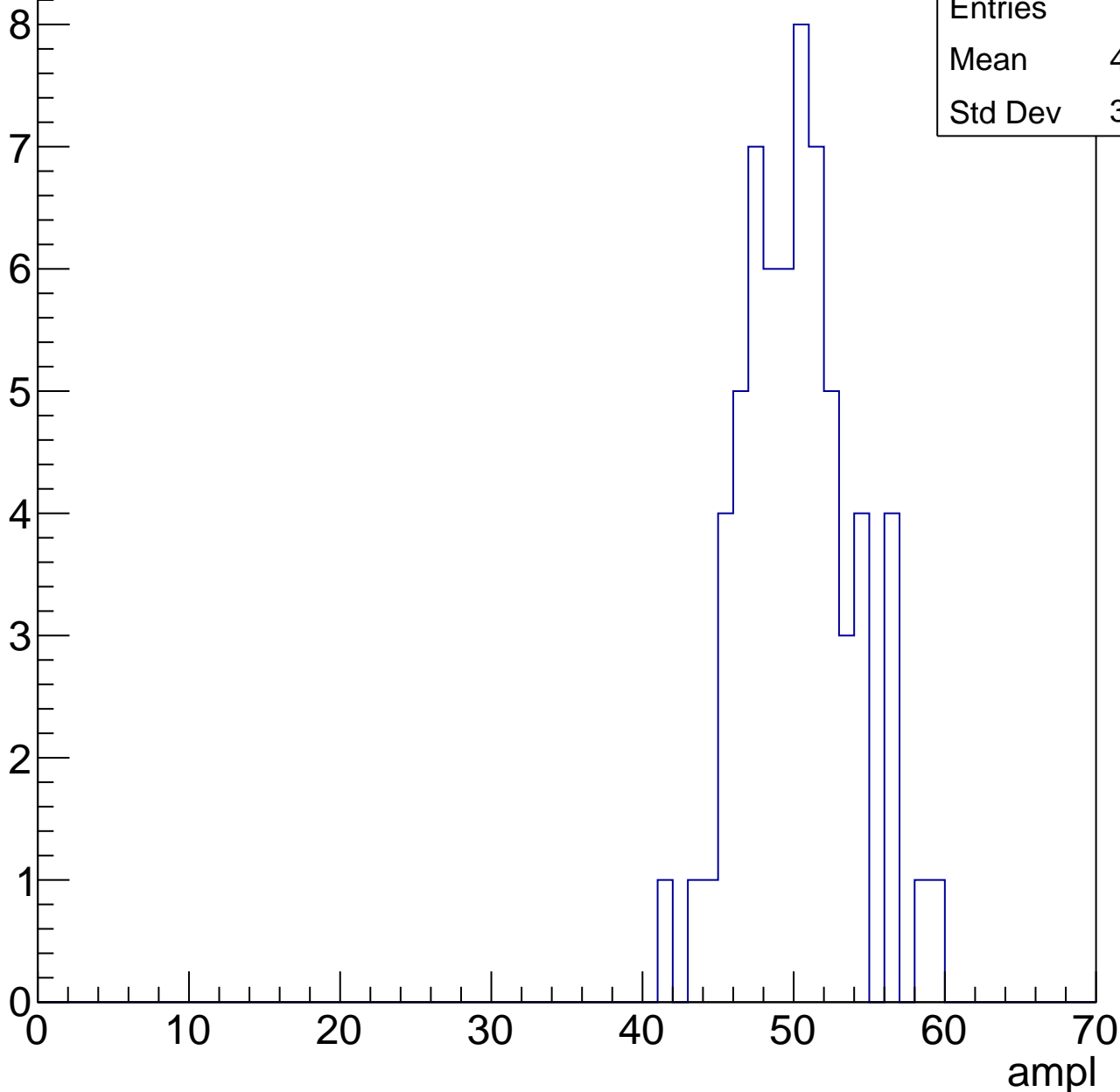


# B1L103S, U4-ch107, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 64    |
| Mean    | 49.72 |
| Std Dev | 3.625 |

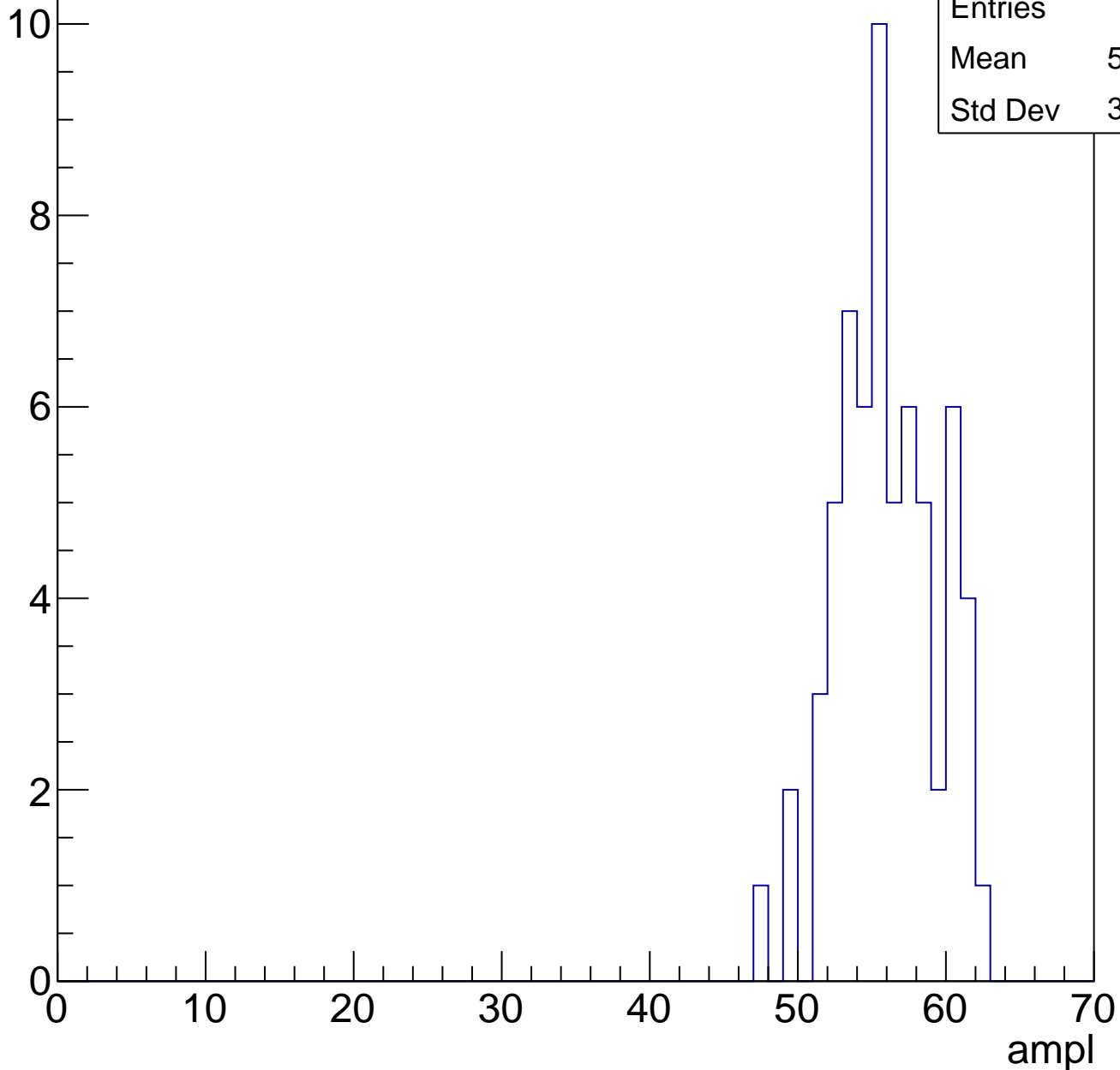


# B1L103S, U4-ch107, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 63    |
| Mean    | 55.54 |
| Std Dev | 3.318 |

Entry

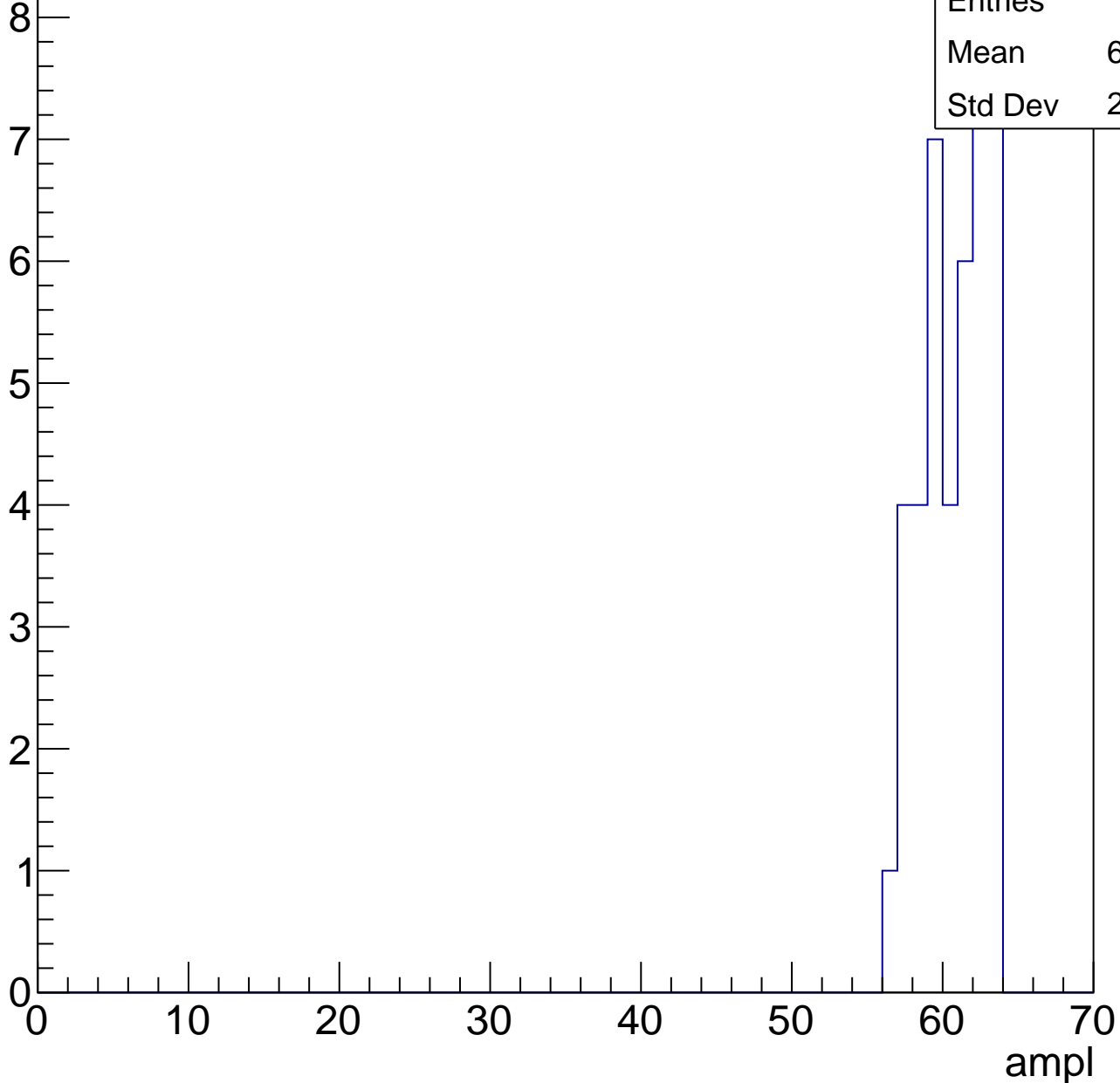


# B1L103S, U4-ch107, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 42    |
| Mean    | 60.36 |
| Std Dev | 2.068 |



# B1L103S, U4-ch107, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U4-ch107, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

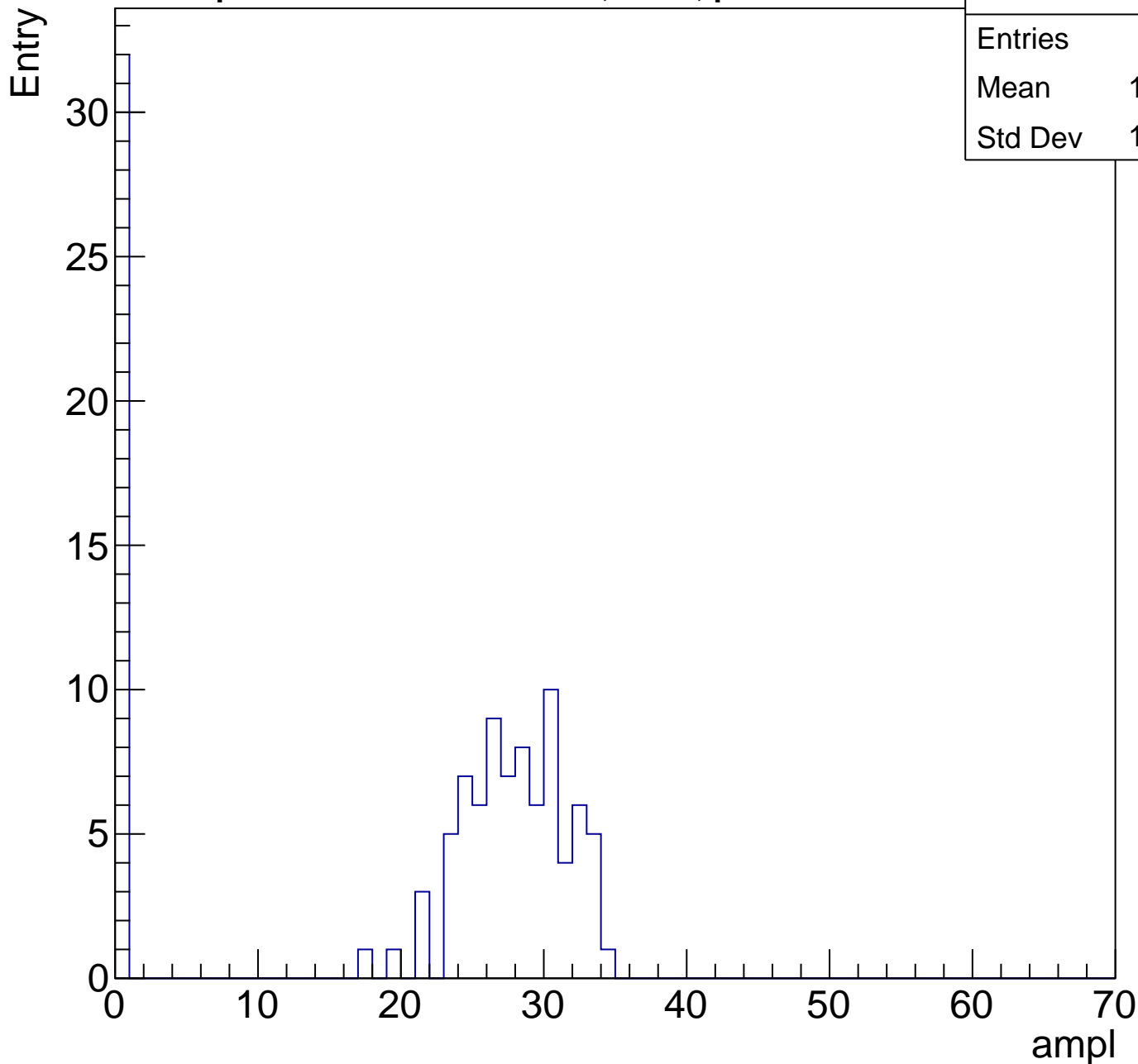
Entry



# B1L103S, U4-ch108, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 111   |
| Mean    | 19.53 |
| Std Dev | 12.79 |

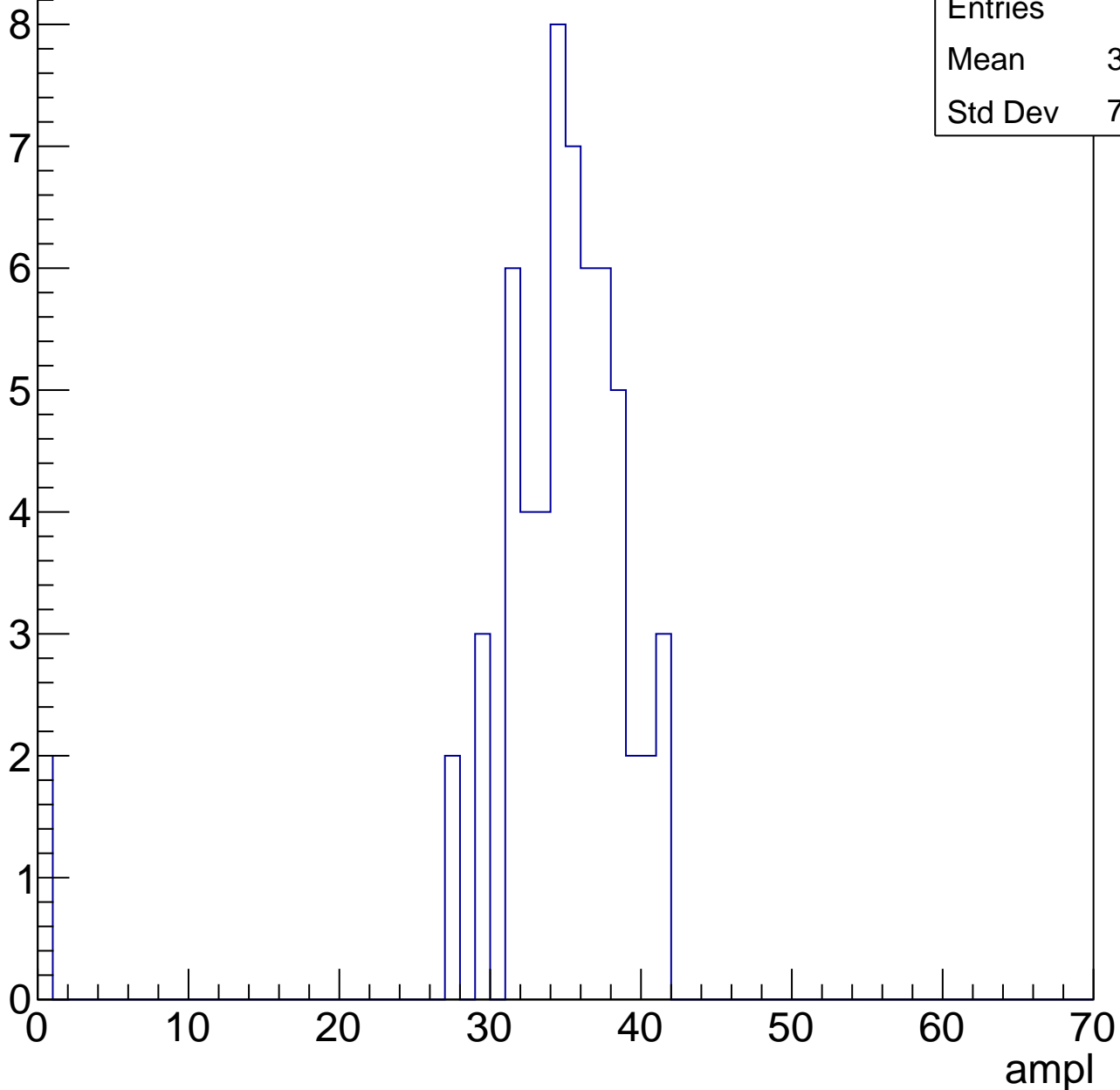


# B1L103S, U4-ch108, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 60    |
| Mean    | 33.55 |
| Std Dev | 7.048 |



# B1L103S, U4-ch108, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 79    |
| Mean    | 34.09 |
| Std Dev | 15.47 |

Entry

12

10

8

6

4

2

0

0

10

20

30

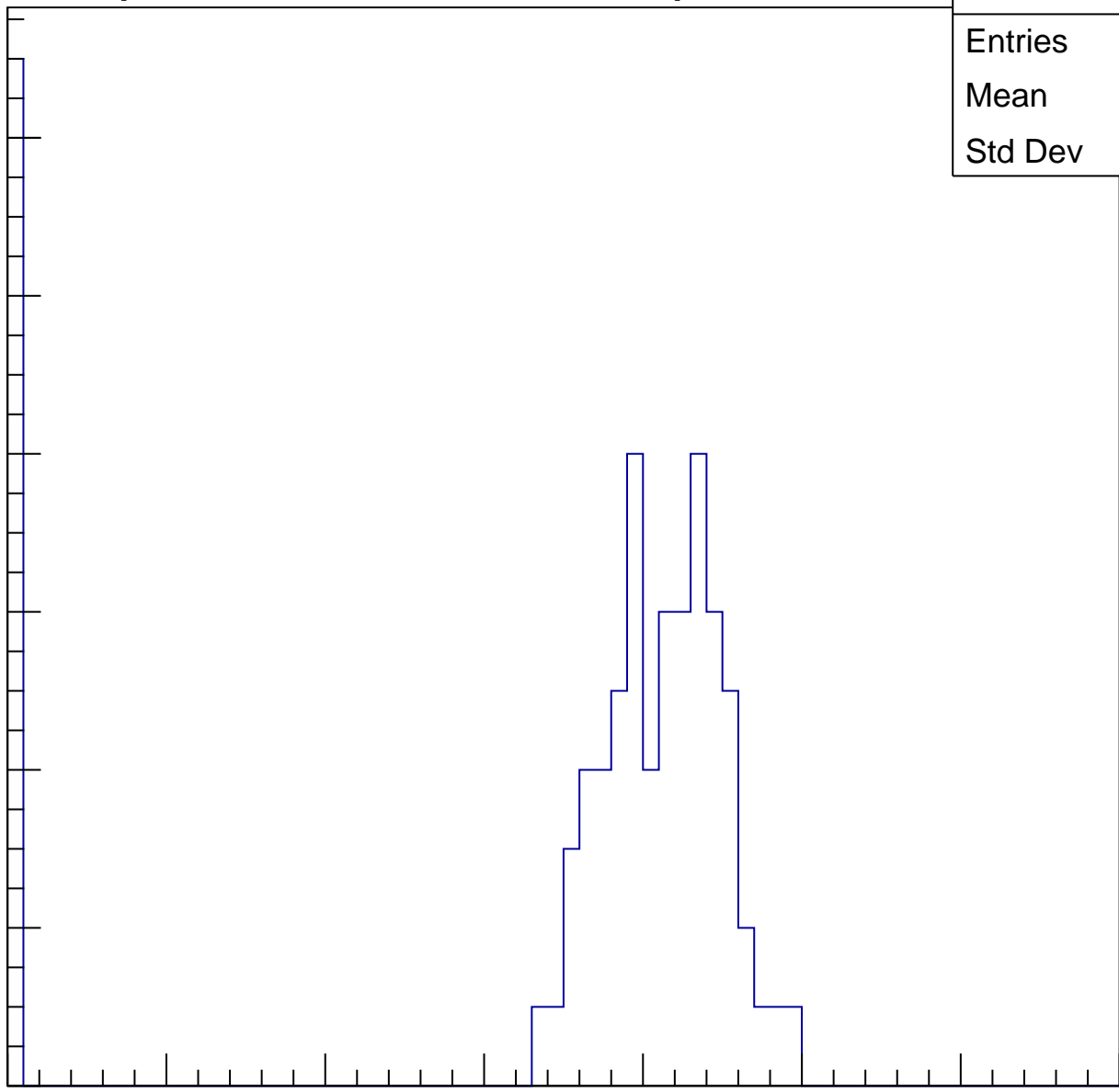
40

50

60

70

ampl

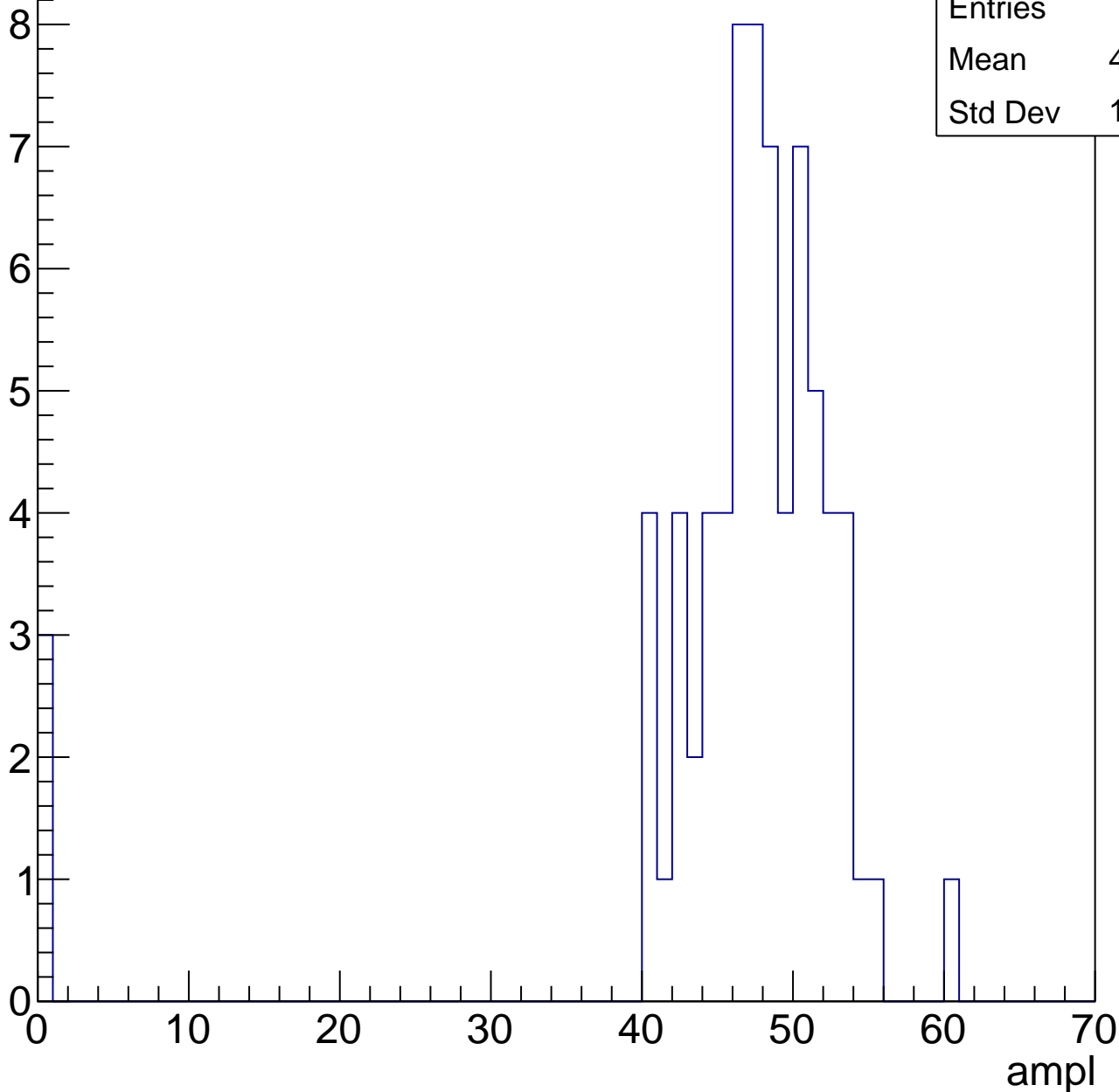


# B1L103S, U4-ch108, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 72    |
| Mean    | 45.57 |
| Std Dev | 10.27 |

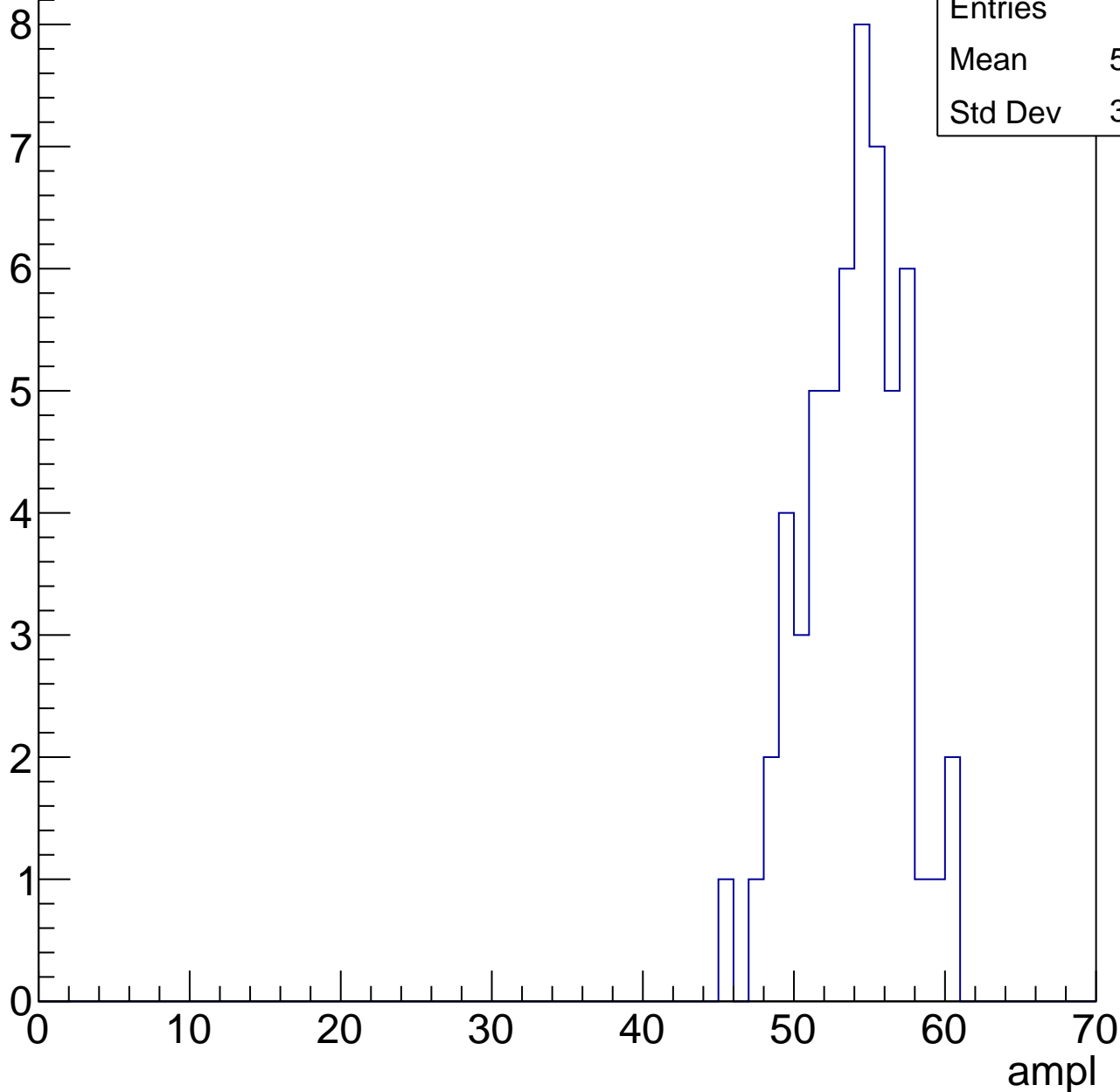


# B1L103S, U4-ch108, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 57    |
| Mean    | 53.39 |
| Std Dev | 3.227 |

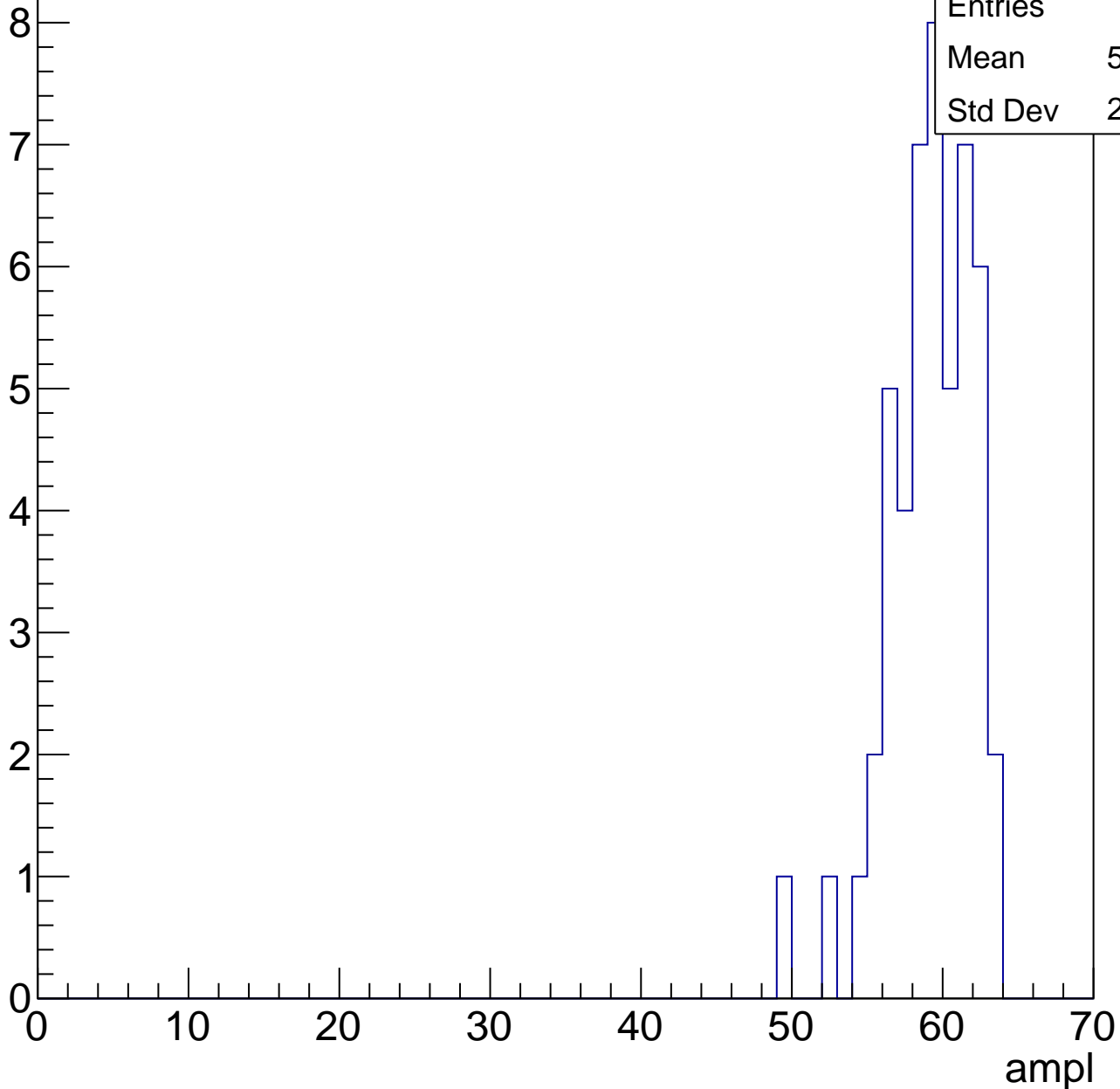


# B1L103S, U4-ch108, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 49    |
| Mean    | 58.69 |
| Std Dev | 2.815 |

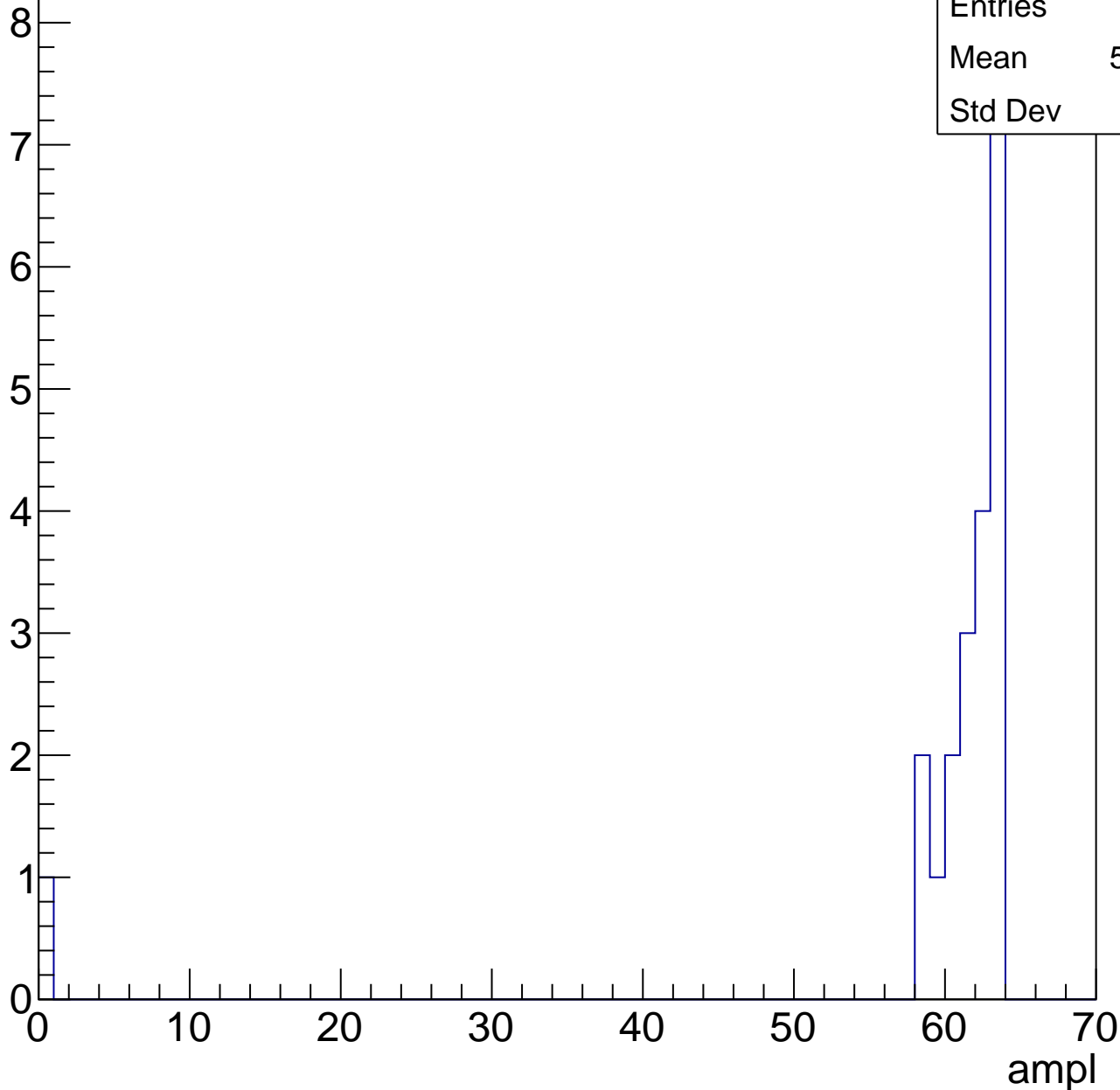


# B1L103S, U4-ch108, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 21    |
| Mean    | 58.57 |
| Std Dev | 13.2  |





# B1L103S, U4-ch108, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

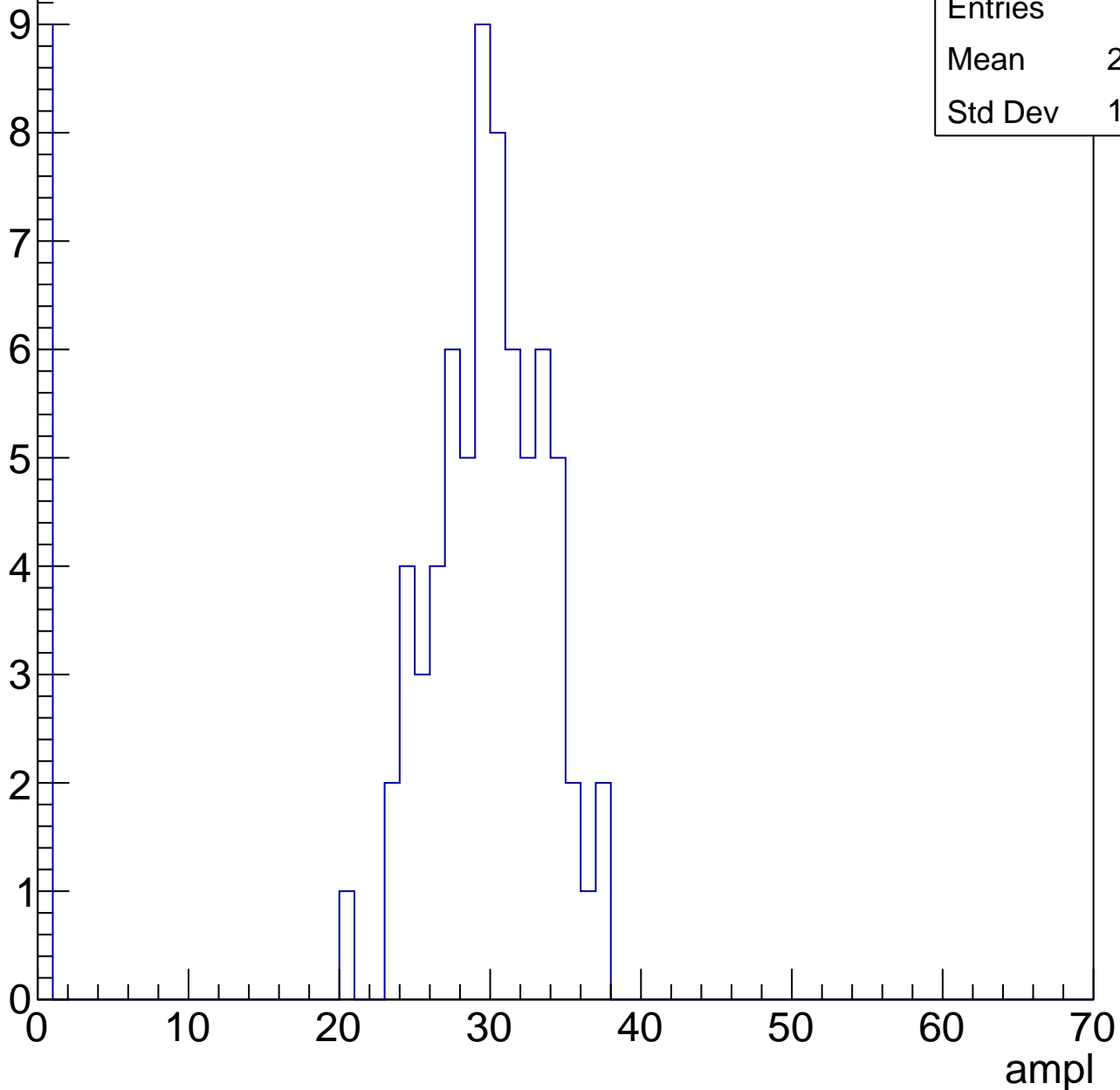


# B1L103S, U4-ch109, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 78    |
| Mean    | 26.13 |
| Std Dev | 10.02 |

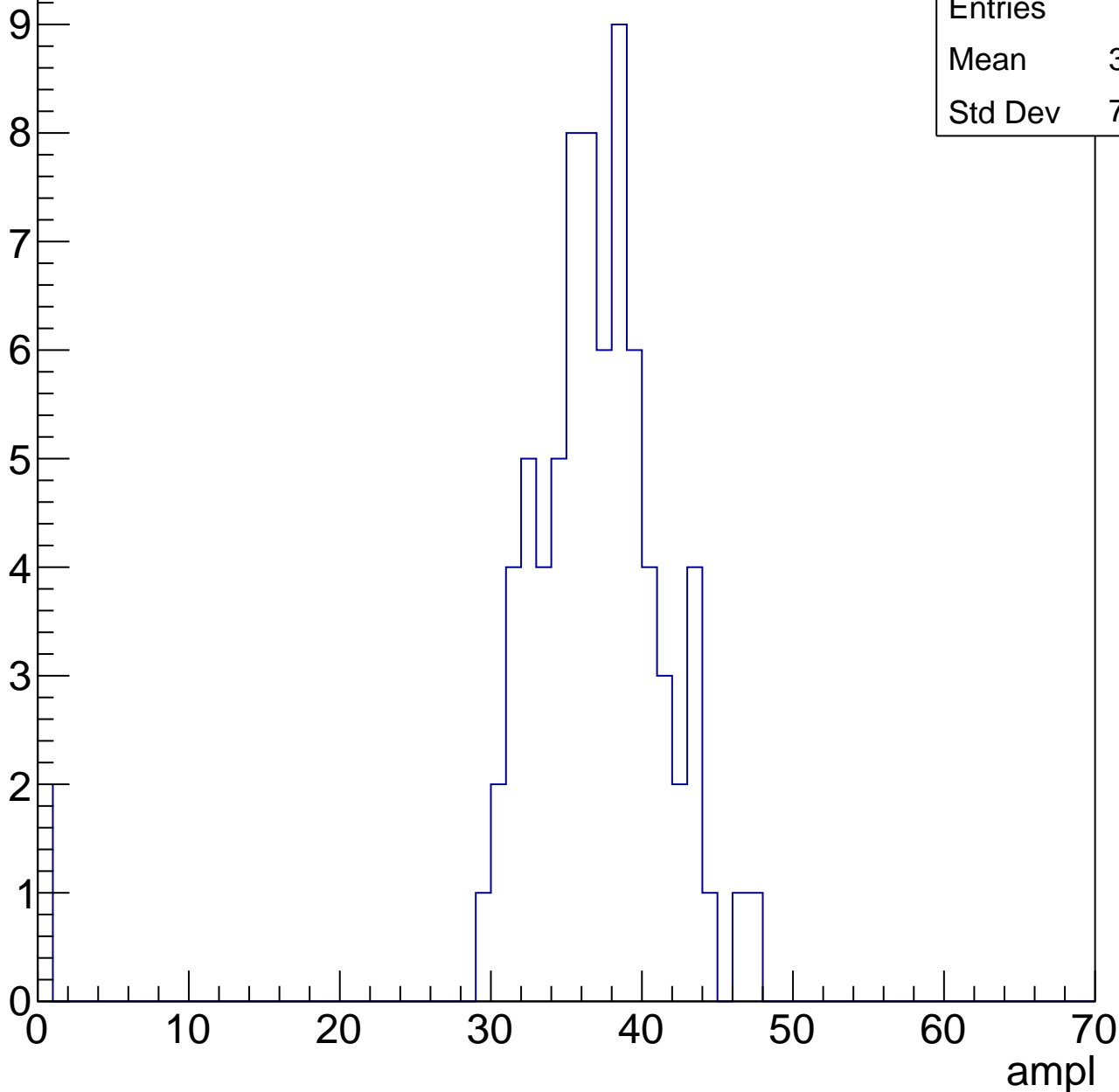


# B1L103S, U4-ch109, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 76    |
| Mean    | 35.75 |
| Std Dev | 7.015 |

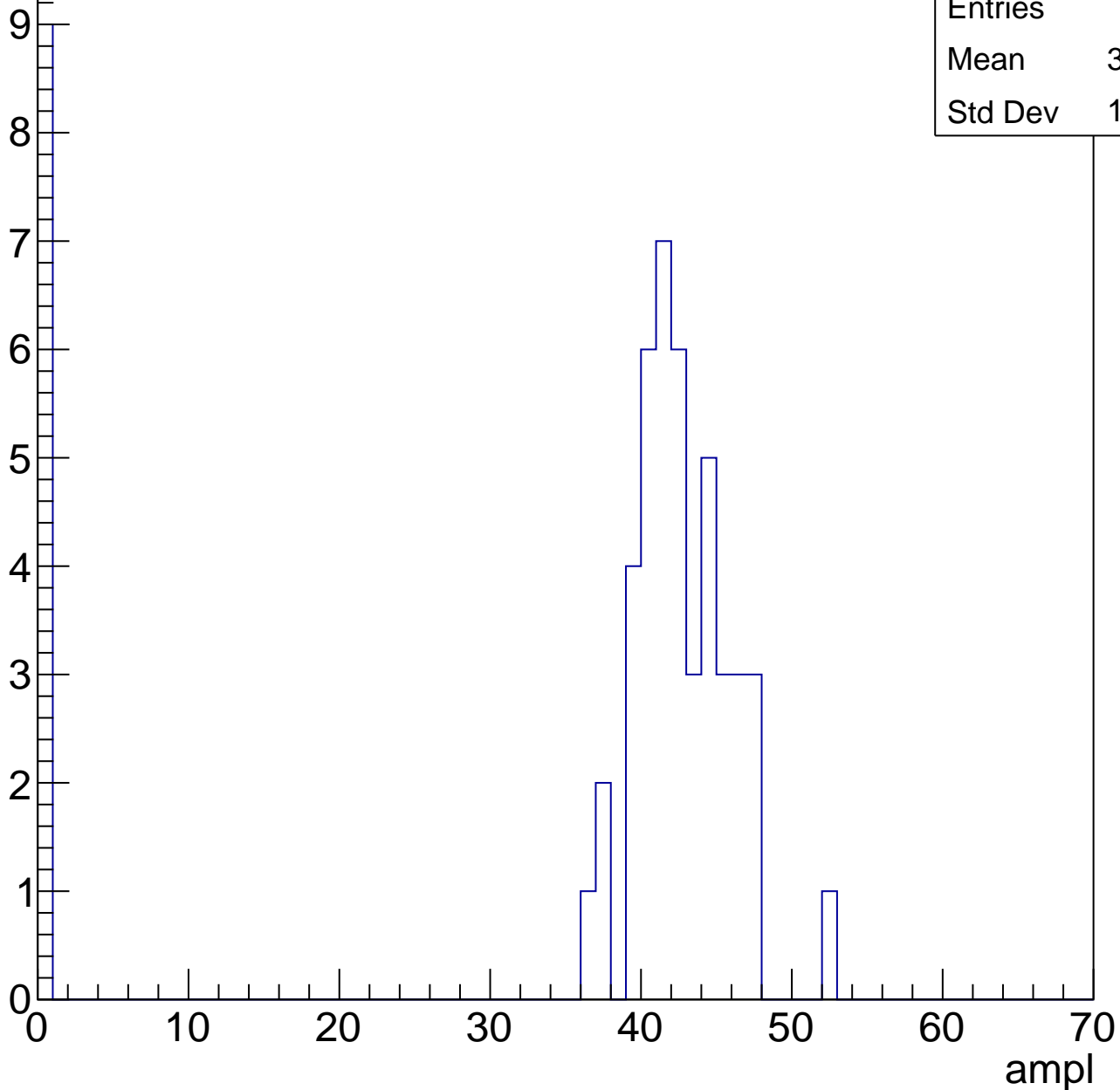


# B1L103S, U4-ch109, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 53    |
| Mean    | 35.09 |
| Std Dev | 16.12 |

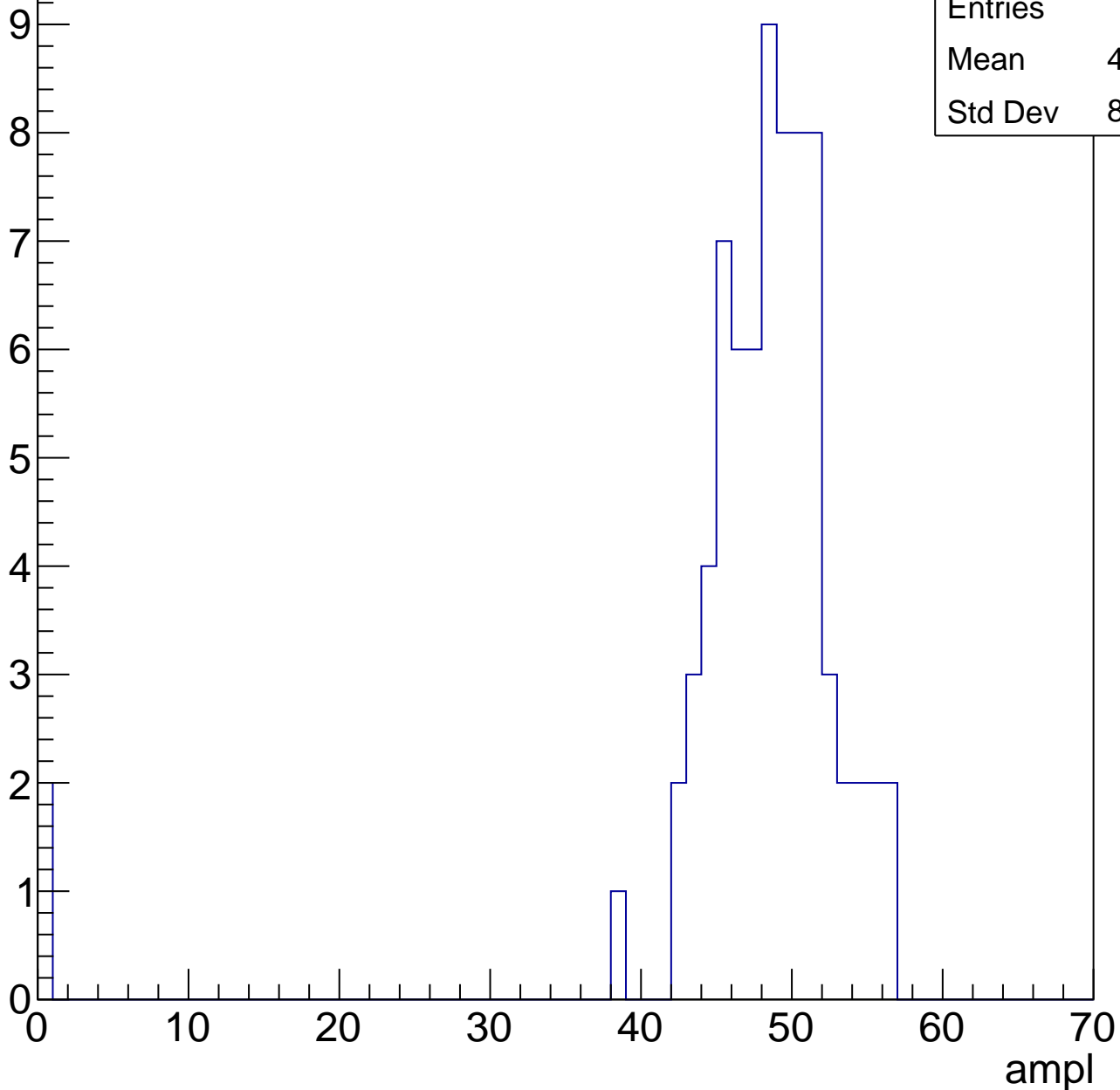


# B1L103S, U4-ch109, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 75    |
| Mean    | 46.99 |
| Std Dev | 8.519 |

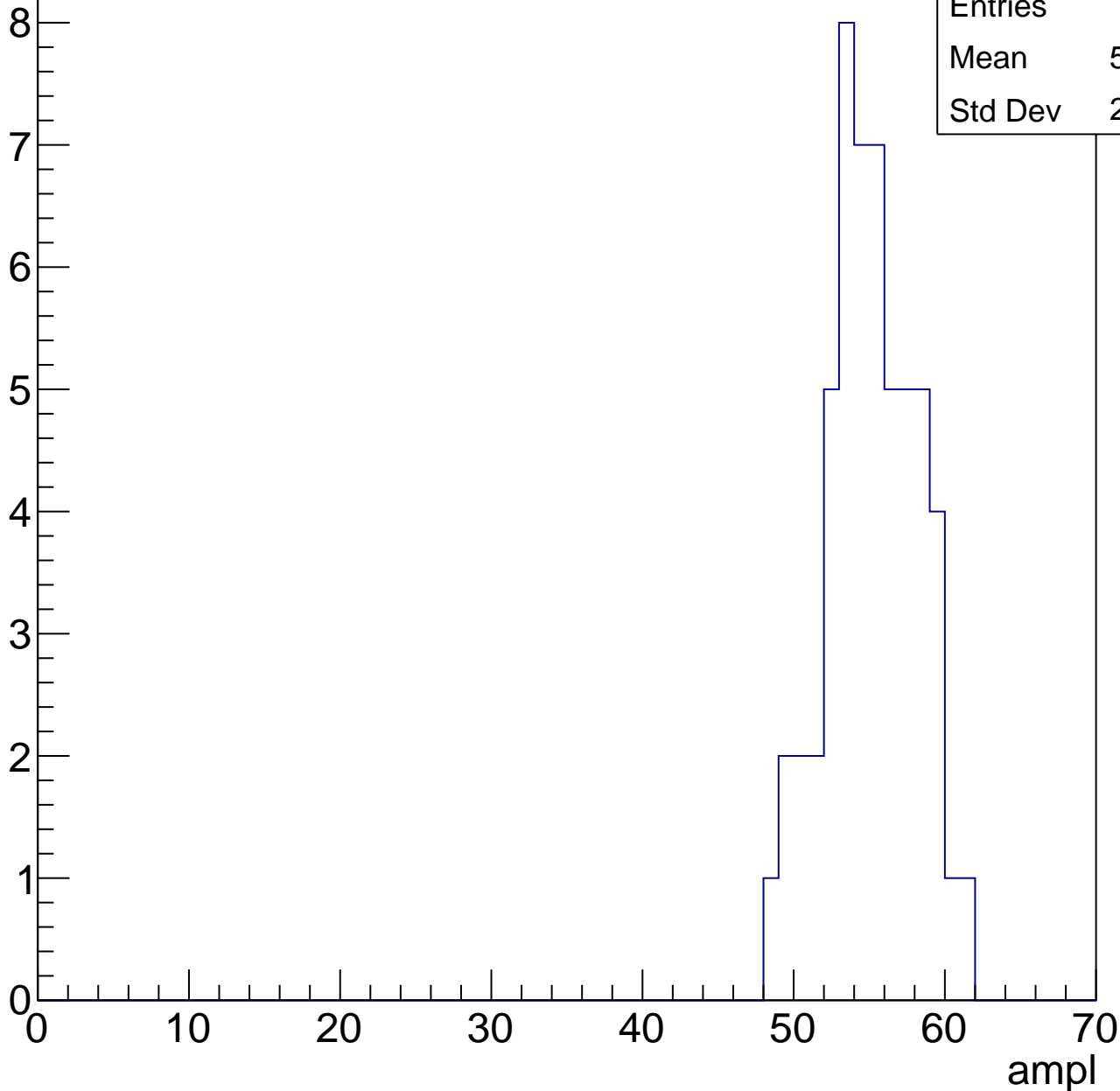


# B1L103S, U4-ch109, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 55    |
| Mean    | 54.67 |
| Std Dev | 2.942 |

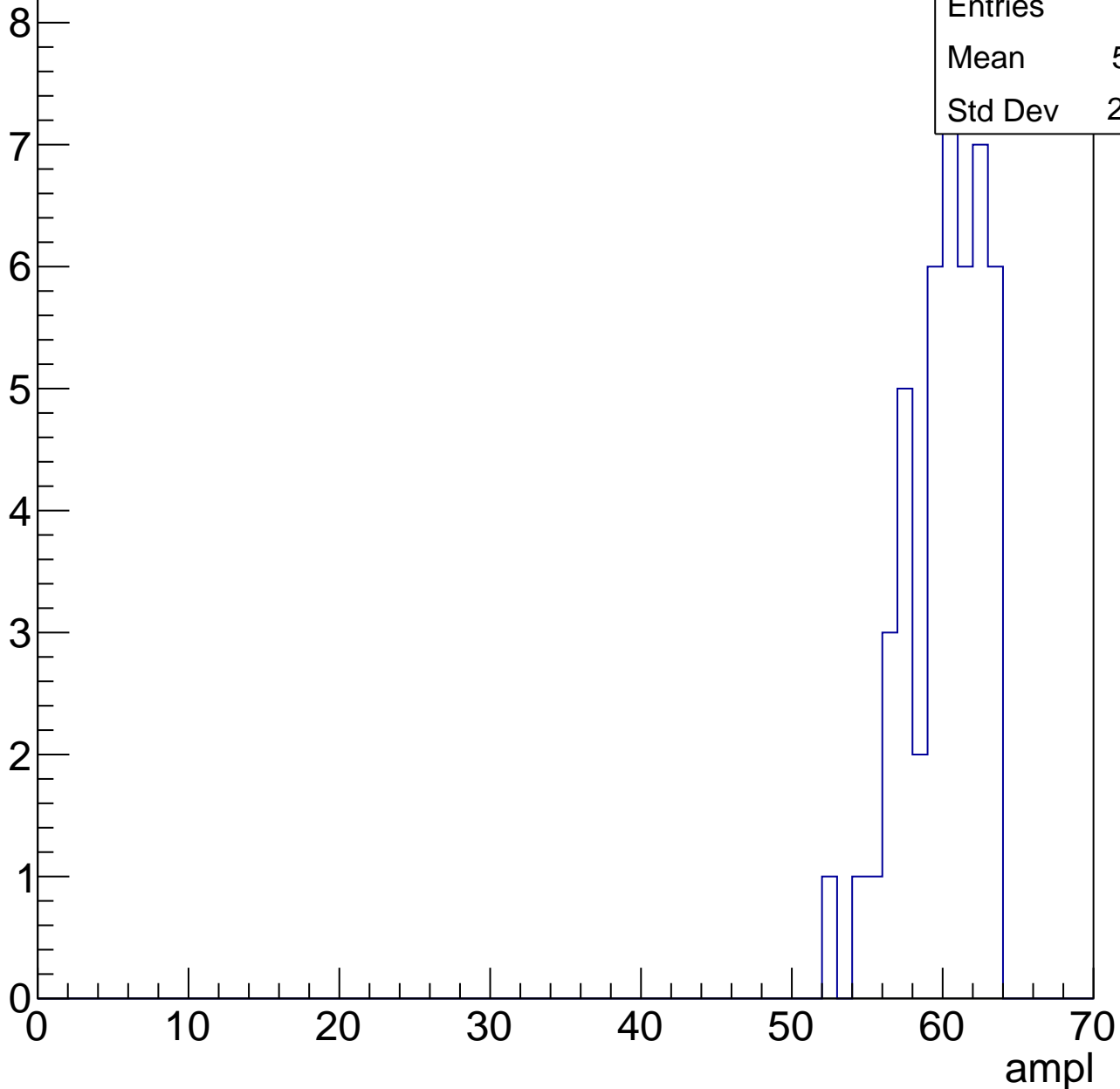


# B1L103S, U4-ch109, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

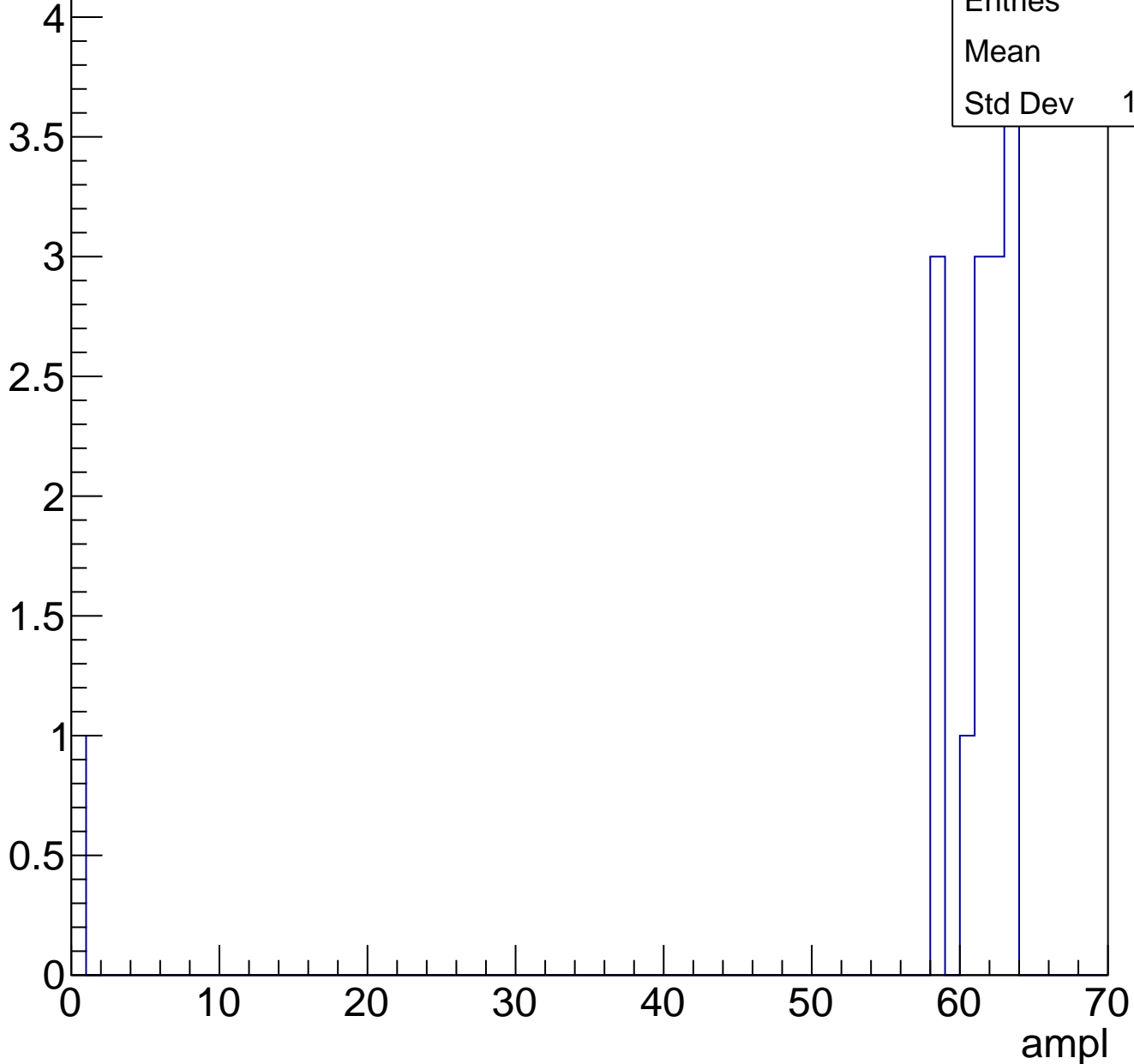
|         |       |
|---------|-------|
| Entries | 46    |
| Mean    | 59.61 |
| Std Dev | 2.608 |



# B1L103S, U4-ch109, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U4-ch109, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

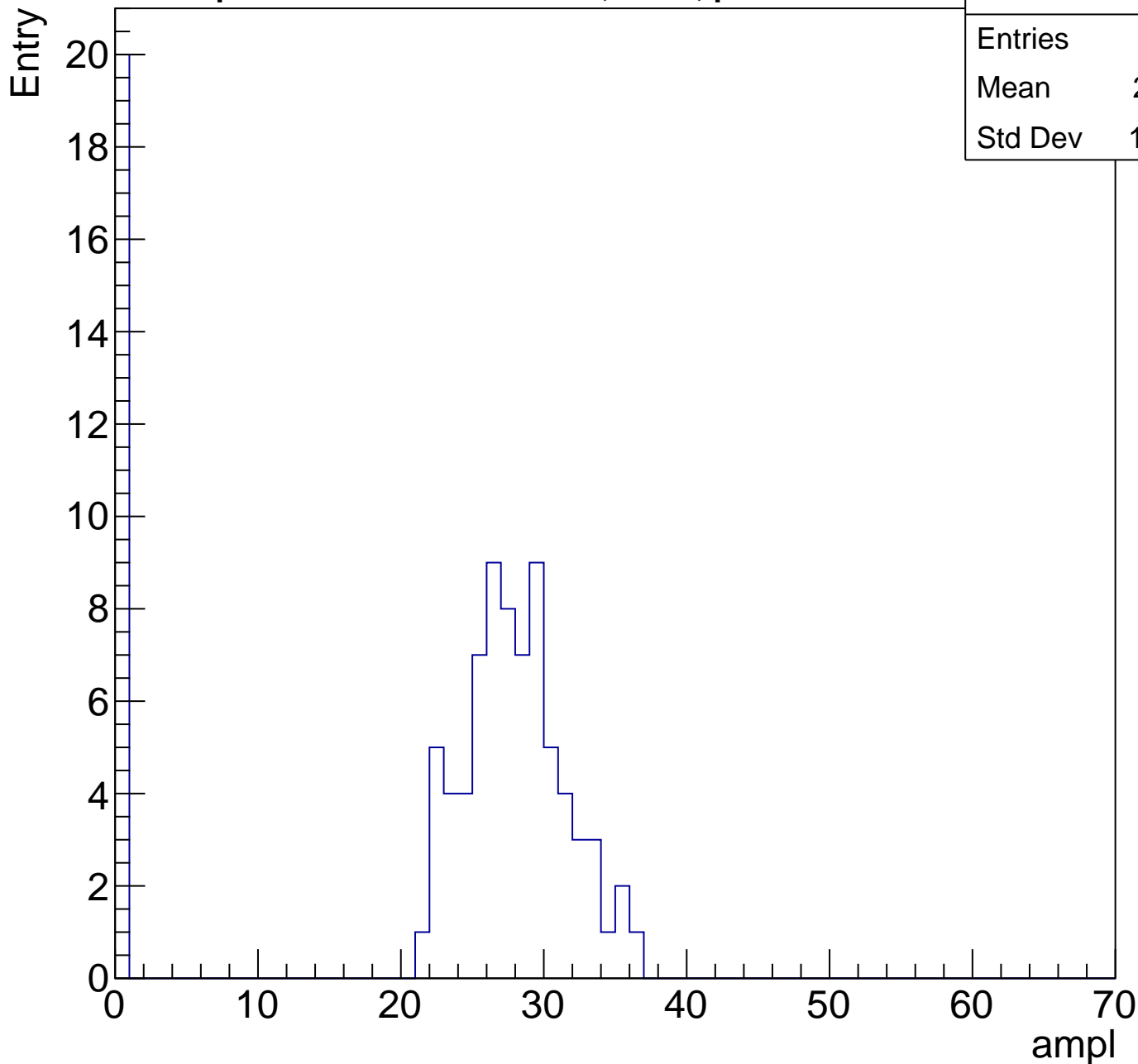
ampl

|         |    |
|---------|----|
| Entries | 19 |
| Mean    | 0  |
| Std Dev | 0  |

# B1L103S, U4-ch110, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 93    |
| Mean    | 21.61 |
| Std Dev | 11.72 |



# B1L103S, U4-ch110, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 59    |
| Mean    | 27.58 |
| Std Dev | 13.5  |

Entry

10

8

6

4

2

0

0

10

20

30

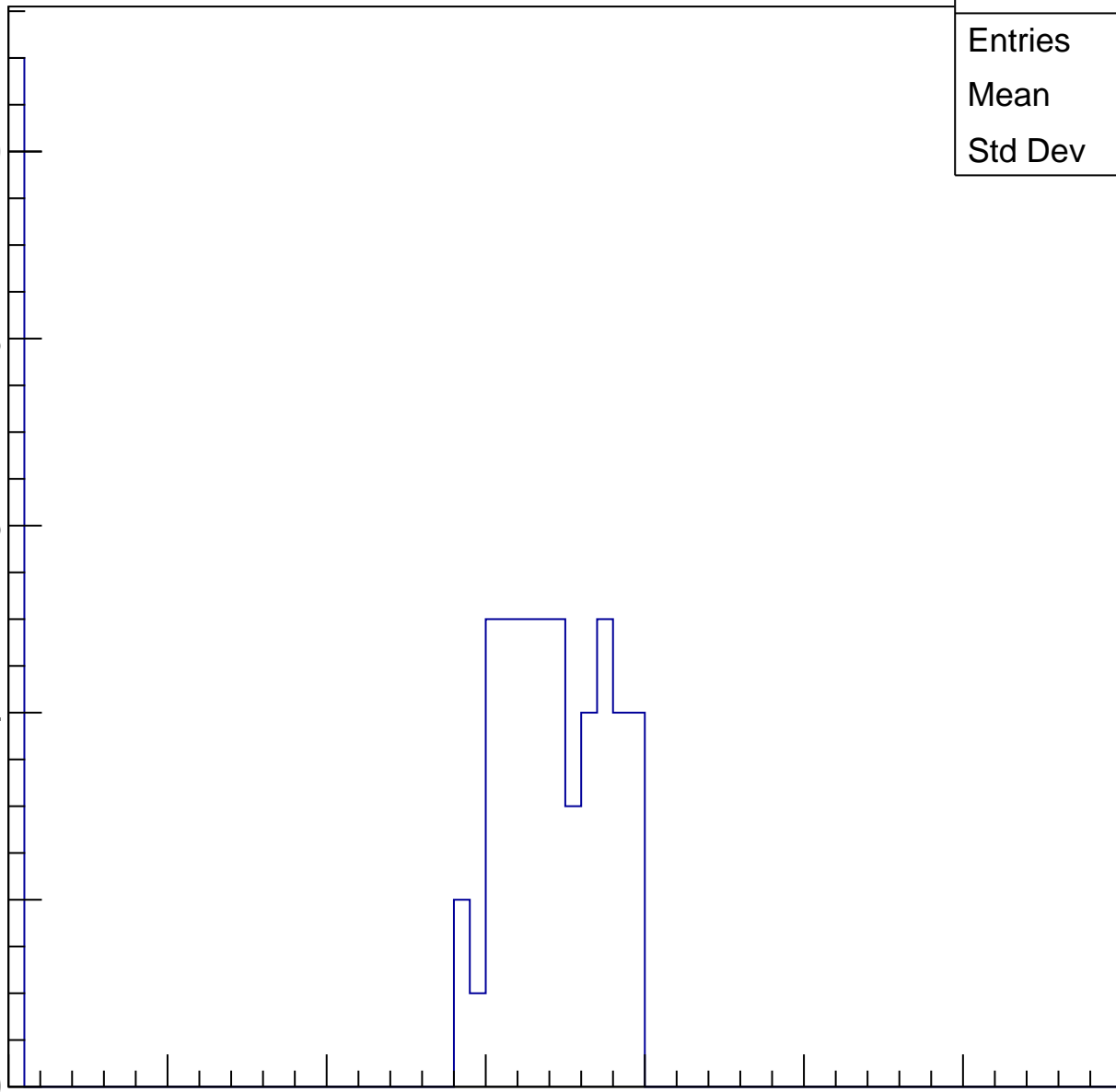
40

50

60

70

ampl

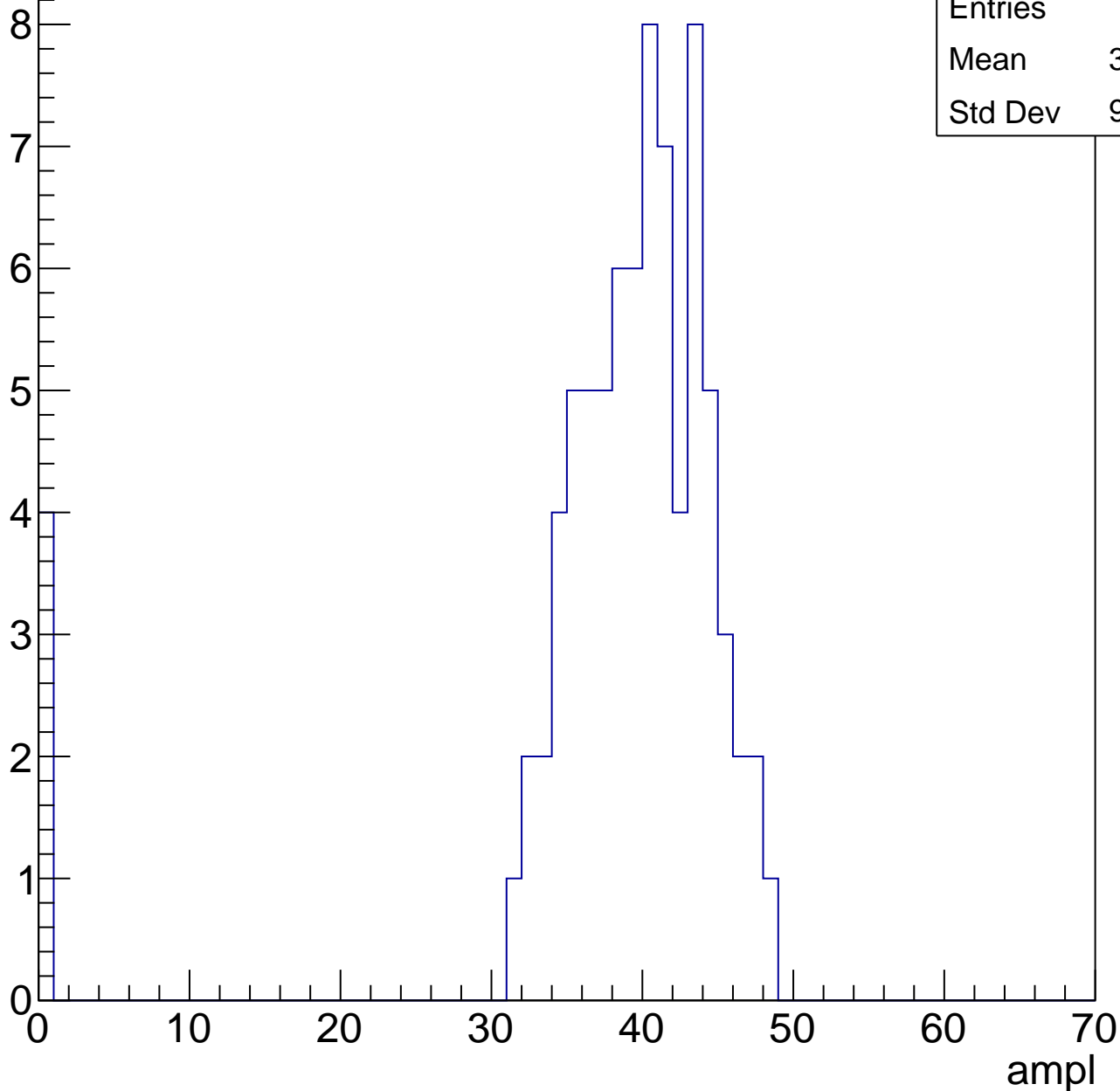


# B1L103S, U4-ch110, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 80    |
| Mean    | 37.59 |
| Std Dev | 9.453 |

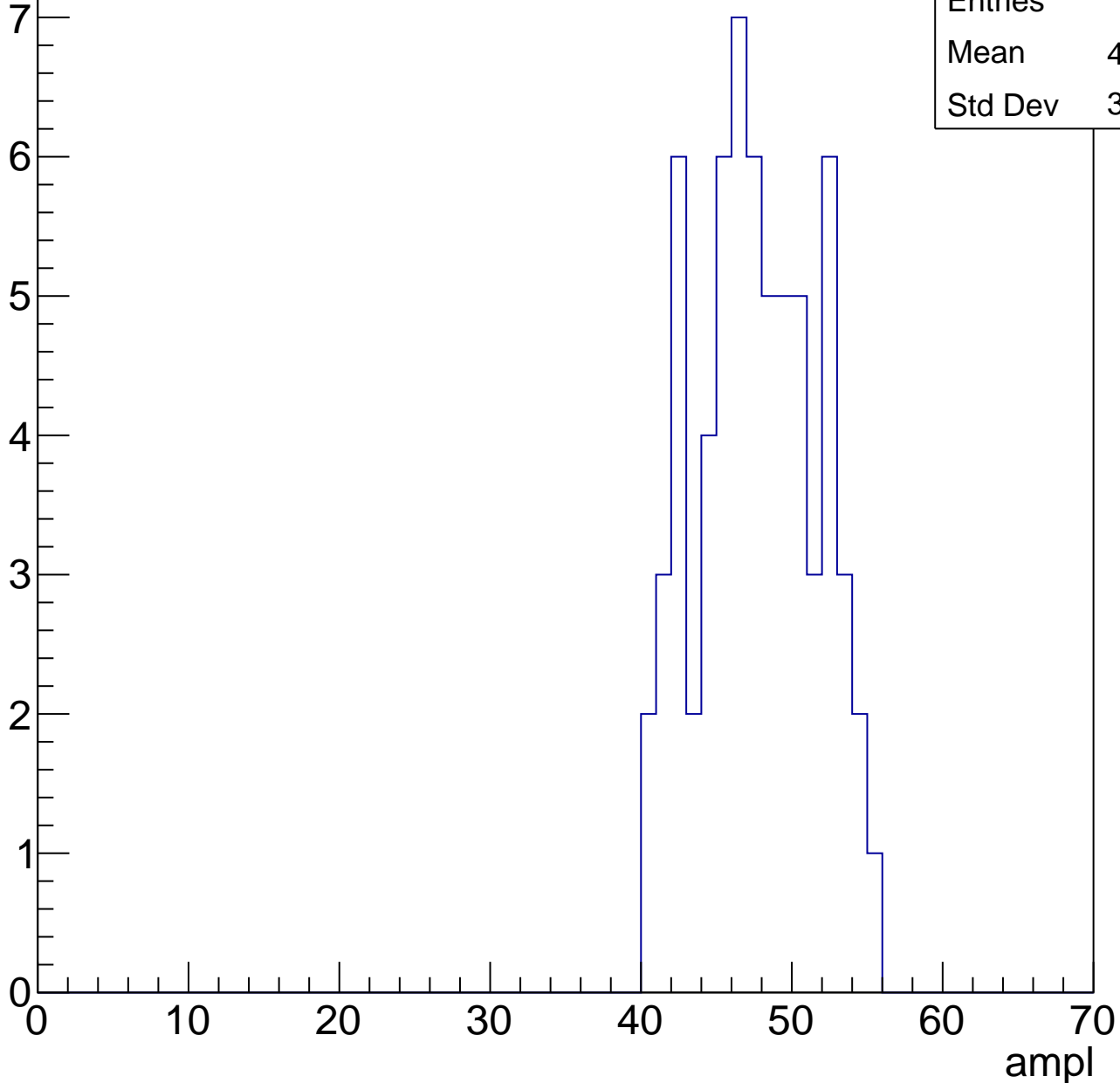


# B1L103S, U4-ch110, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 66    |
| Mean    | 47.17 |
| Std Dev | 3.875 |



# B1L103S, U4-ch110, adc4

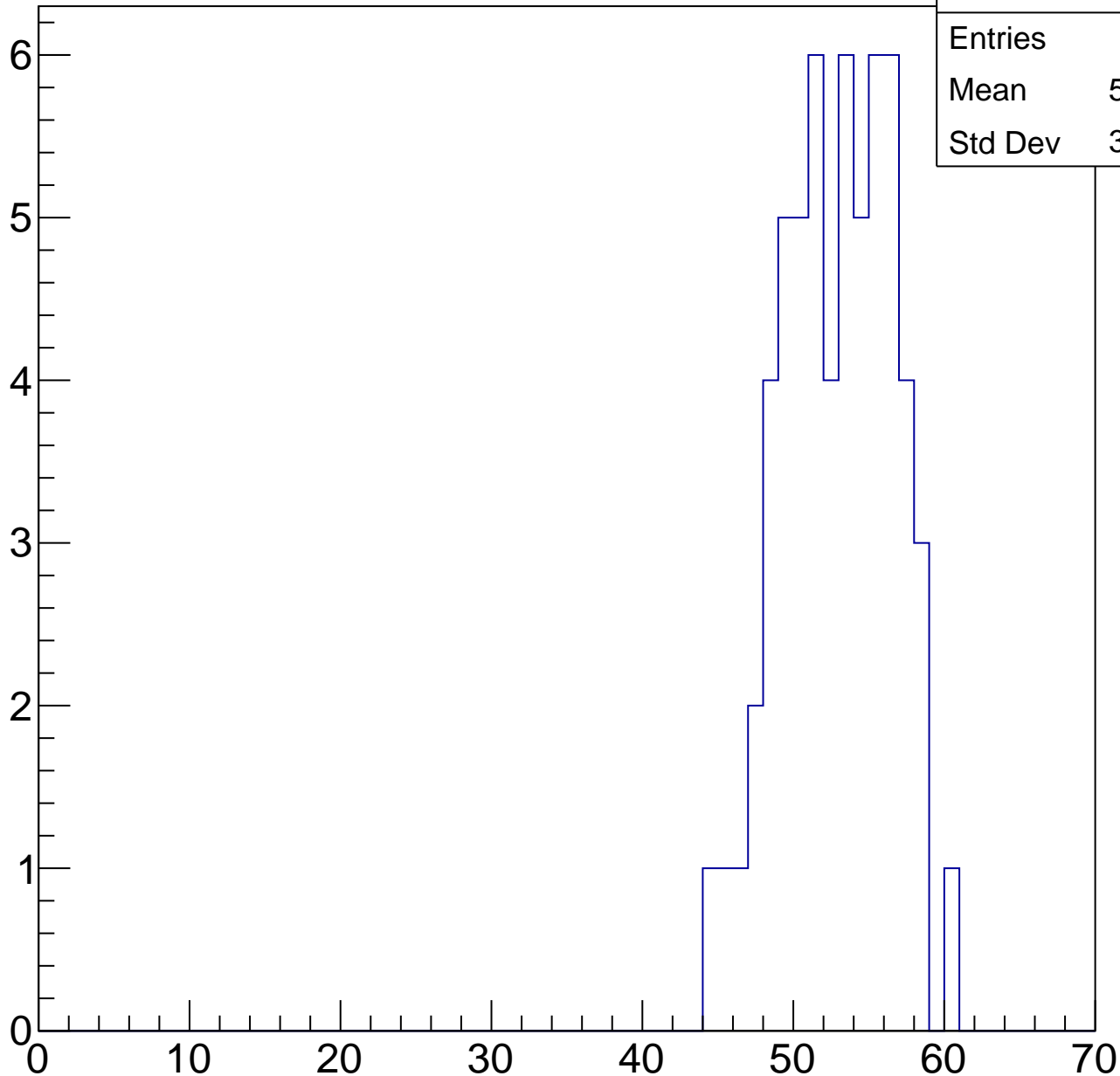
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

6  
5  
4  
3  
2  
1  
0

|         |       |
|---------|-------|
| Entries | 60    |
| Mean    | 52.43 |
| Std Dev | 3.584 |

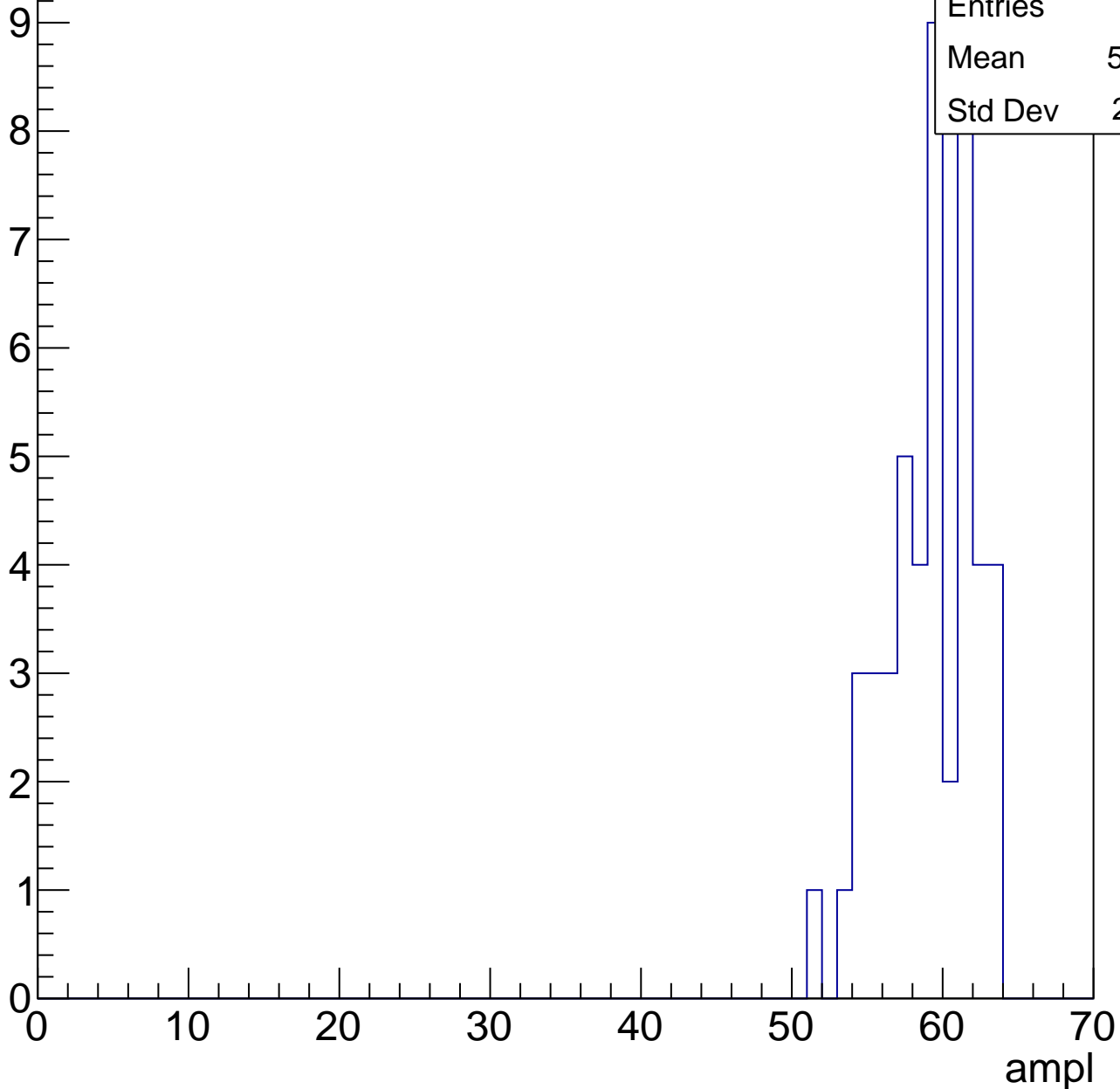
ampl



# B1L103S, U4-ch110, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

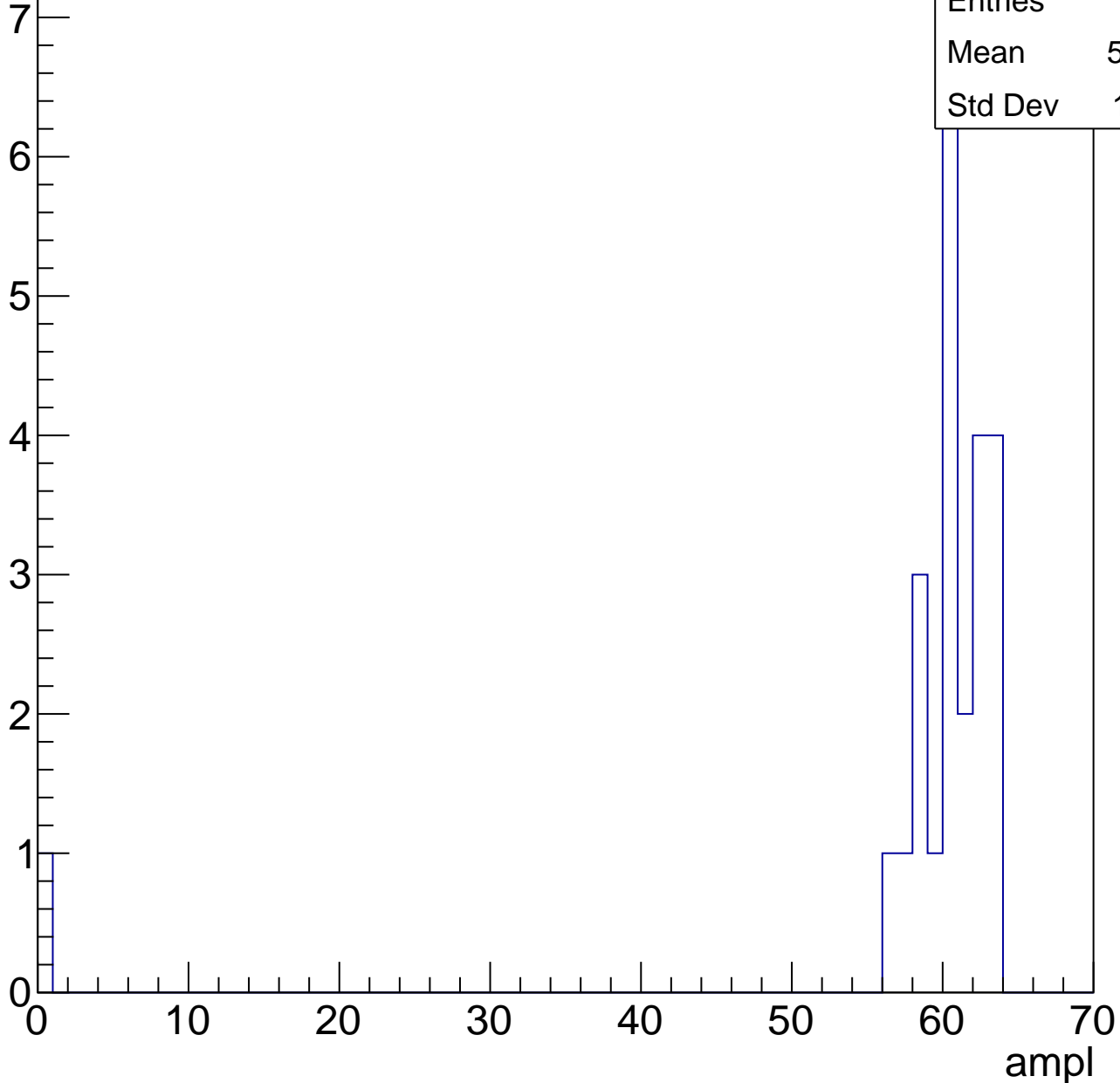


# B1L103S, U4-ch110, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 24    |
| Mean    | 57.83 |
| Std Dev | 12.21 |



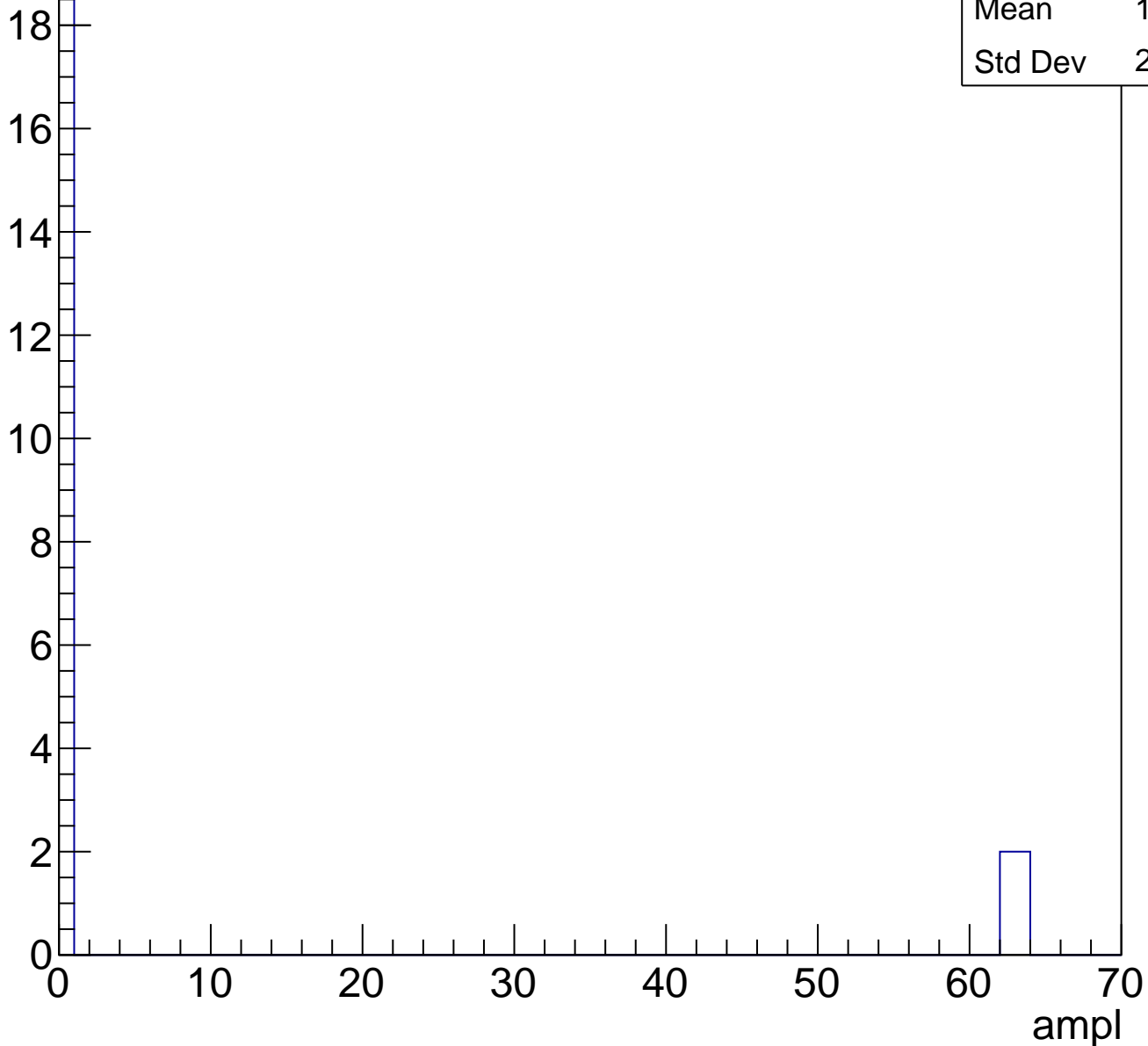


# B1L103S, U4-ch110, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 23    |
| Mean    | 10.87 |
| Std Dev | 23.69 |

Entry

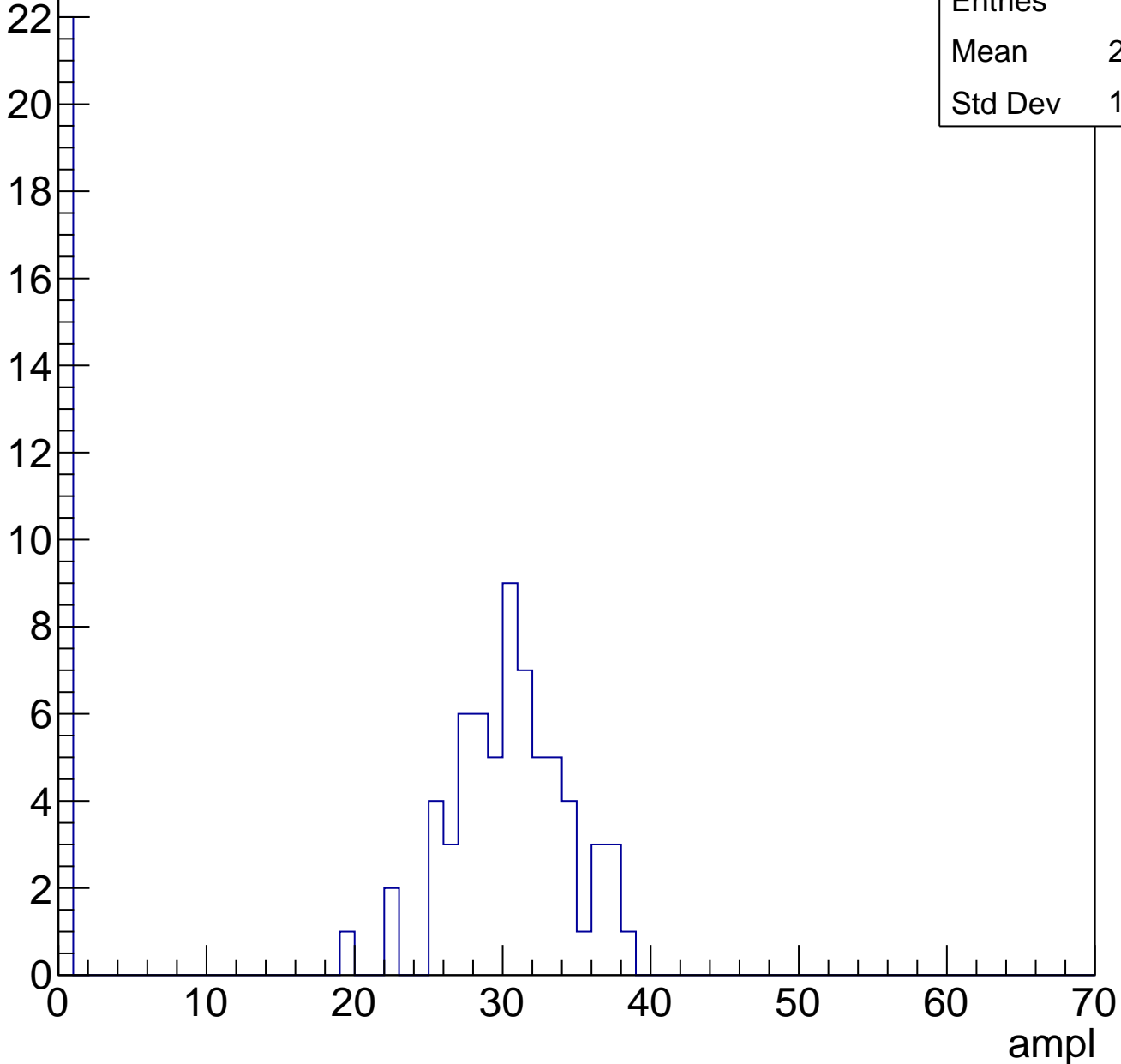


# B1L103S, U4-ch111, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 87    |
| Mean    | 22.48 |
| Std Dev | 13.49 |

Entry



# B1L103S, U4-ch111, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 73    |
| Mean    | 30.33 |
| Std Dev | 13.11 |

Entry

10

8

6

4

2

0

0

10

20

30

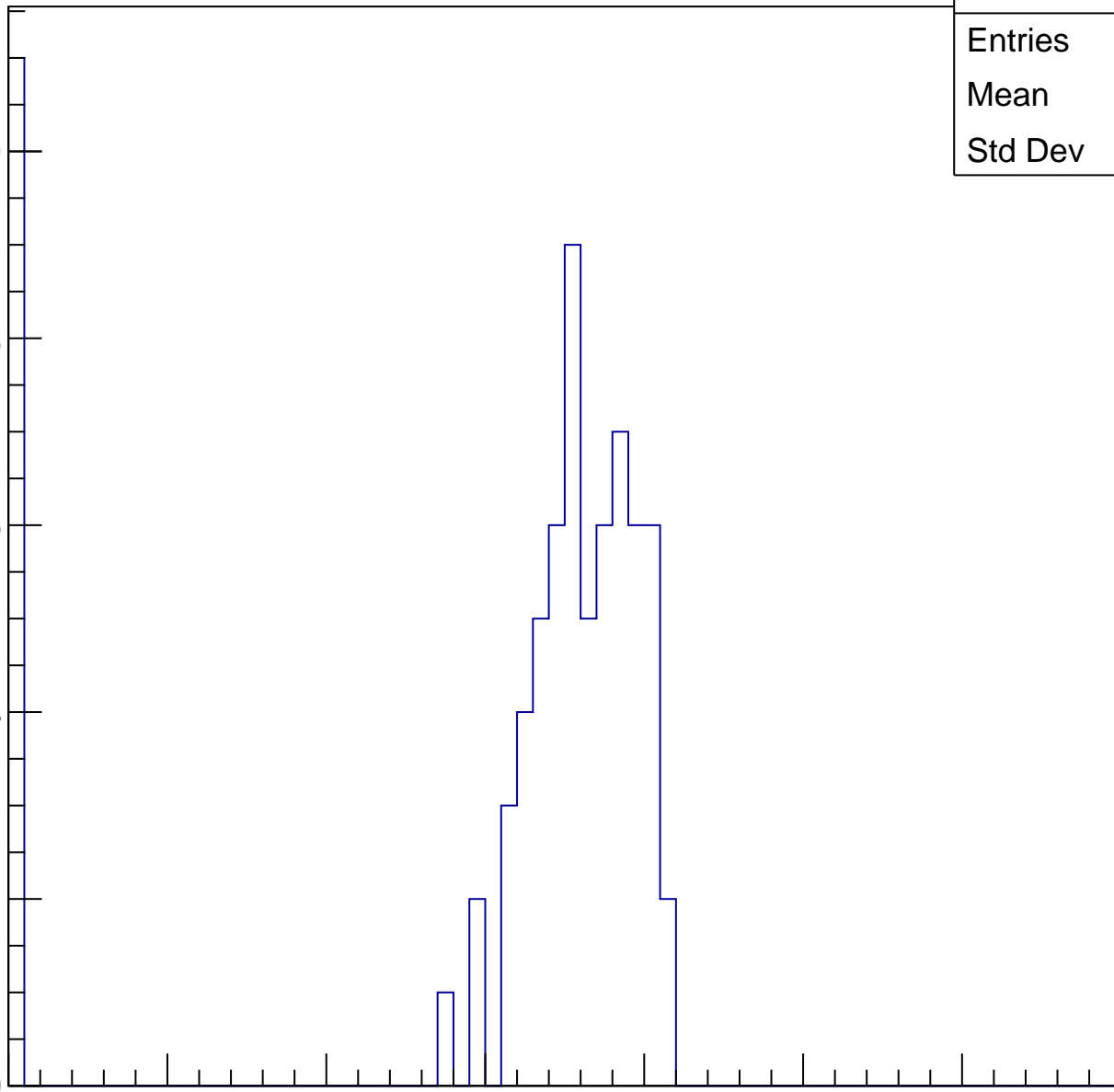
40

50

60

70

ampl

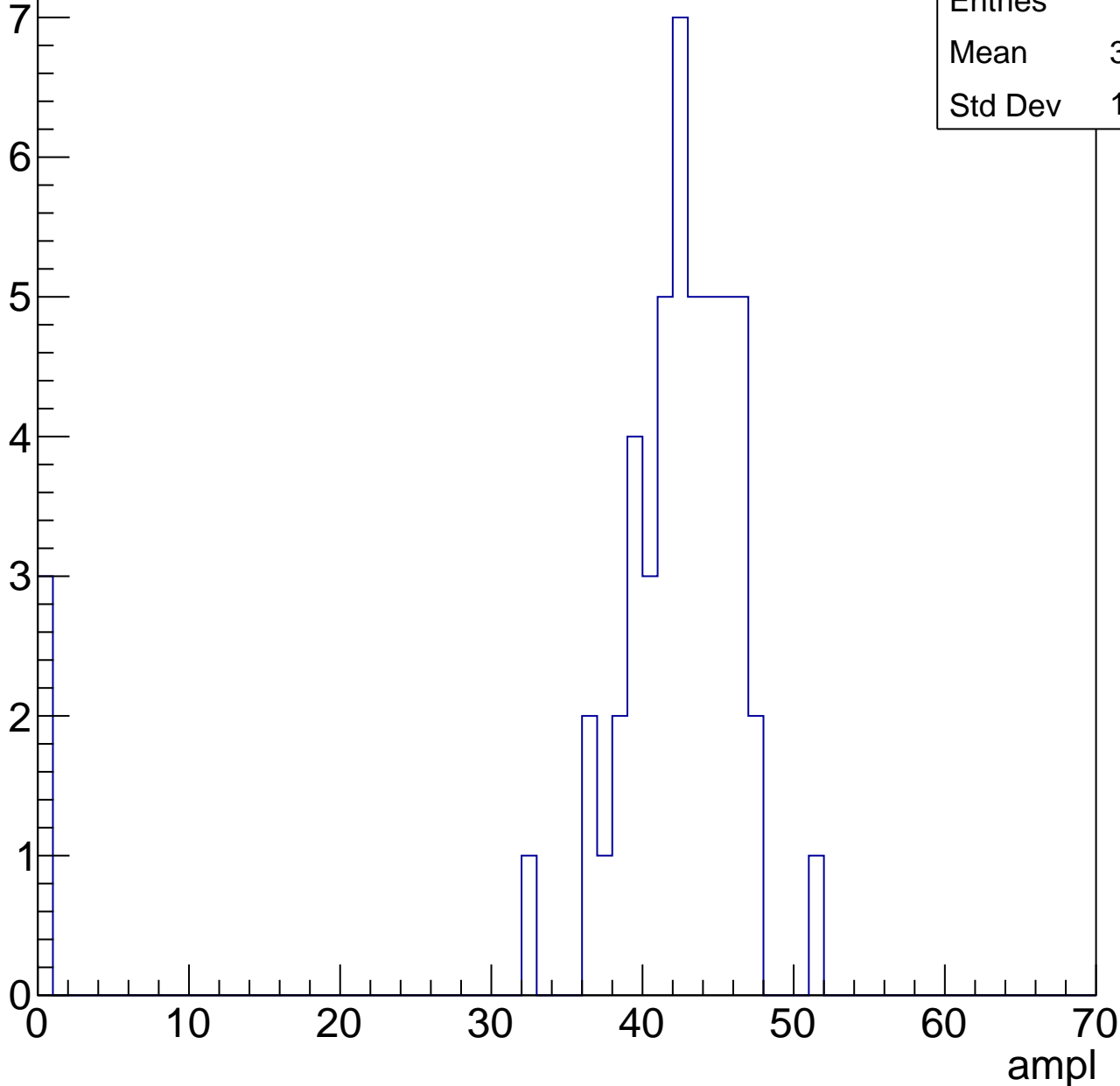


# B1L103S, U4-ch111, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 51    |
| Mean    | 39.75 |
| Std Dev | 10.47 |

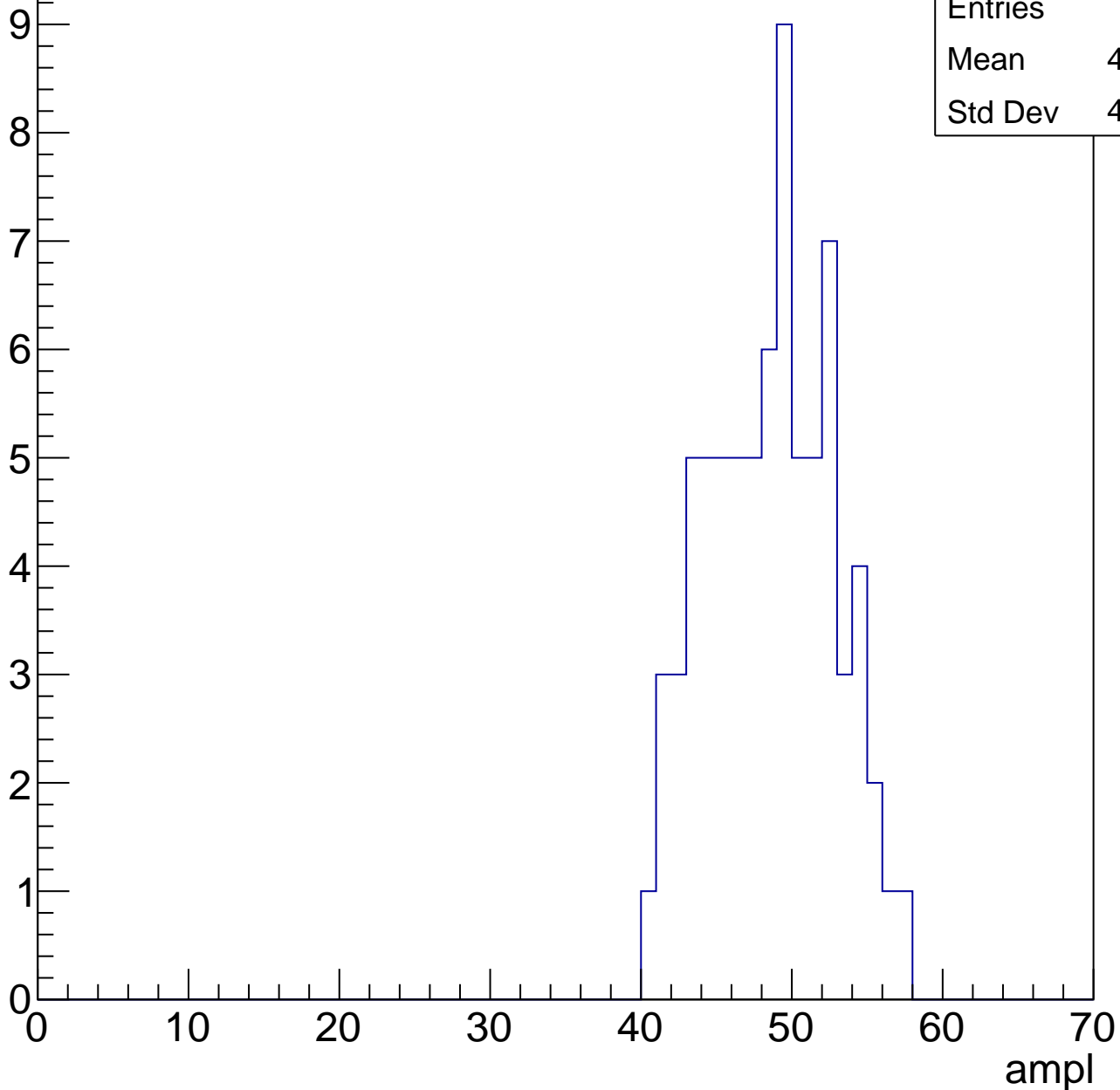


# B1L103S, U4-ch111, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 75    |
| Mean    | 48.13 |
| Std Dev | 4.067 |

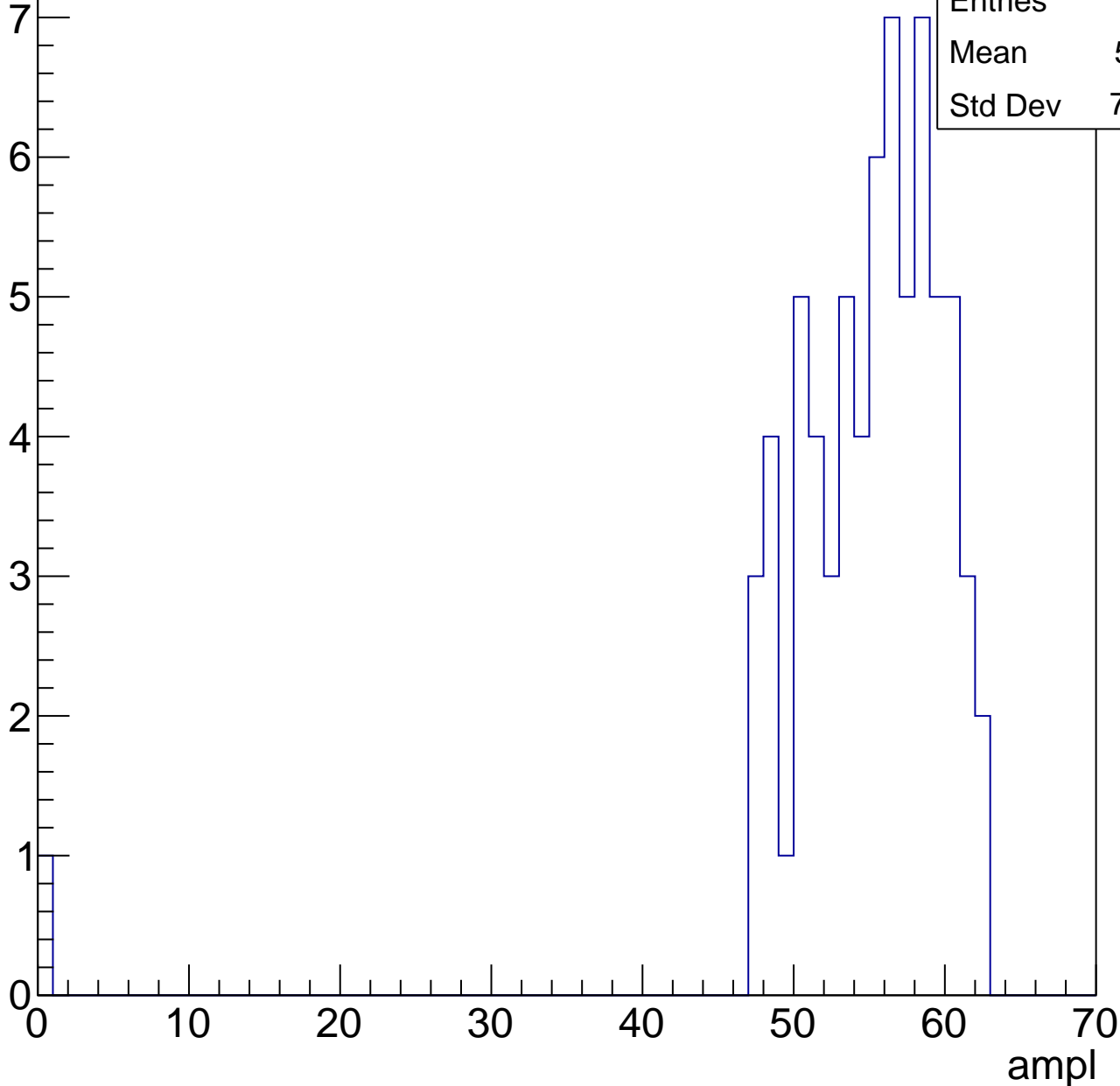


# B1L103S, U4-ch111, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 70    |
| Mean    | 54.11 |
| Std Dev | 7.686 |



# B1L103S, U4-ch111, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

5

4

3

2

1

0

|         |    |
|---------|----|
| Entries | 39 |
|---------|----|

|      |       |
|------|-------|
| Mean | 57.46 |
|------|-------|

|         |       |
|---------|-------|
| Std Dev | 9.766 |
|---------|-------|

ampl

0

10

20

30

40

50

60

70

# B1L103S, U4-ch111, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



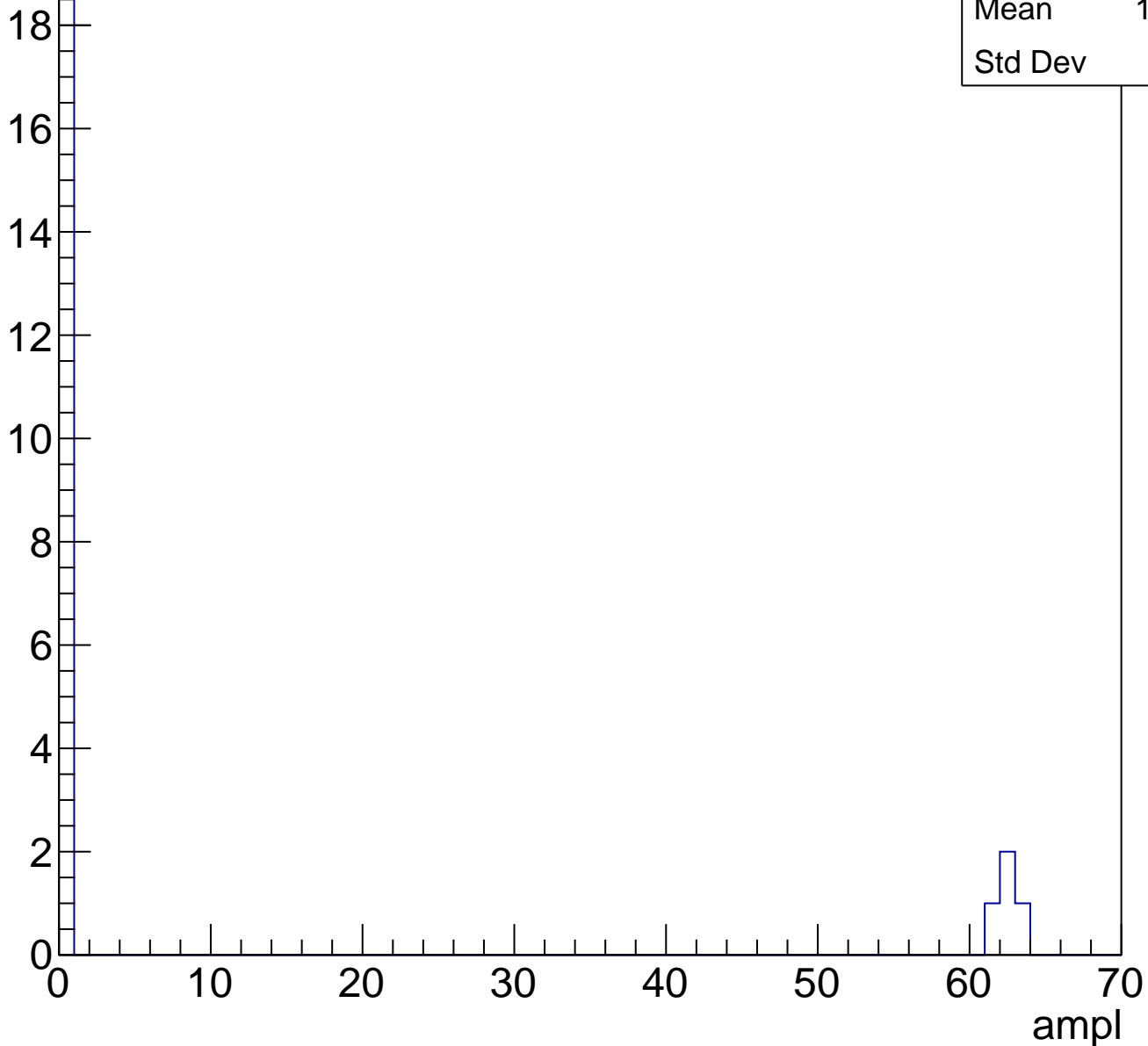


# B1L103S, U4-ch111, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 23    |
| Mean    | 10.78 |
| Std Dev | 23.5  |

Entry



# B1L103S, U4-ch112, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

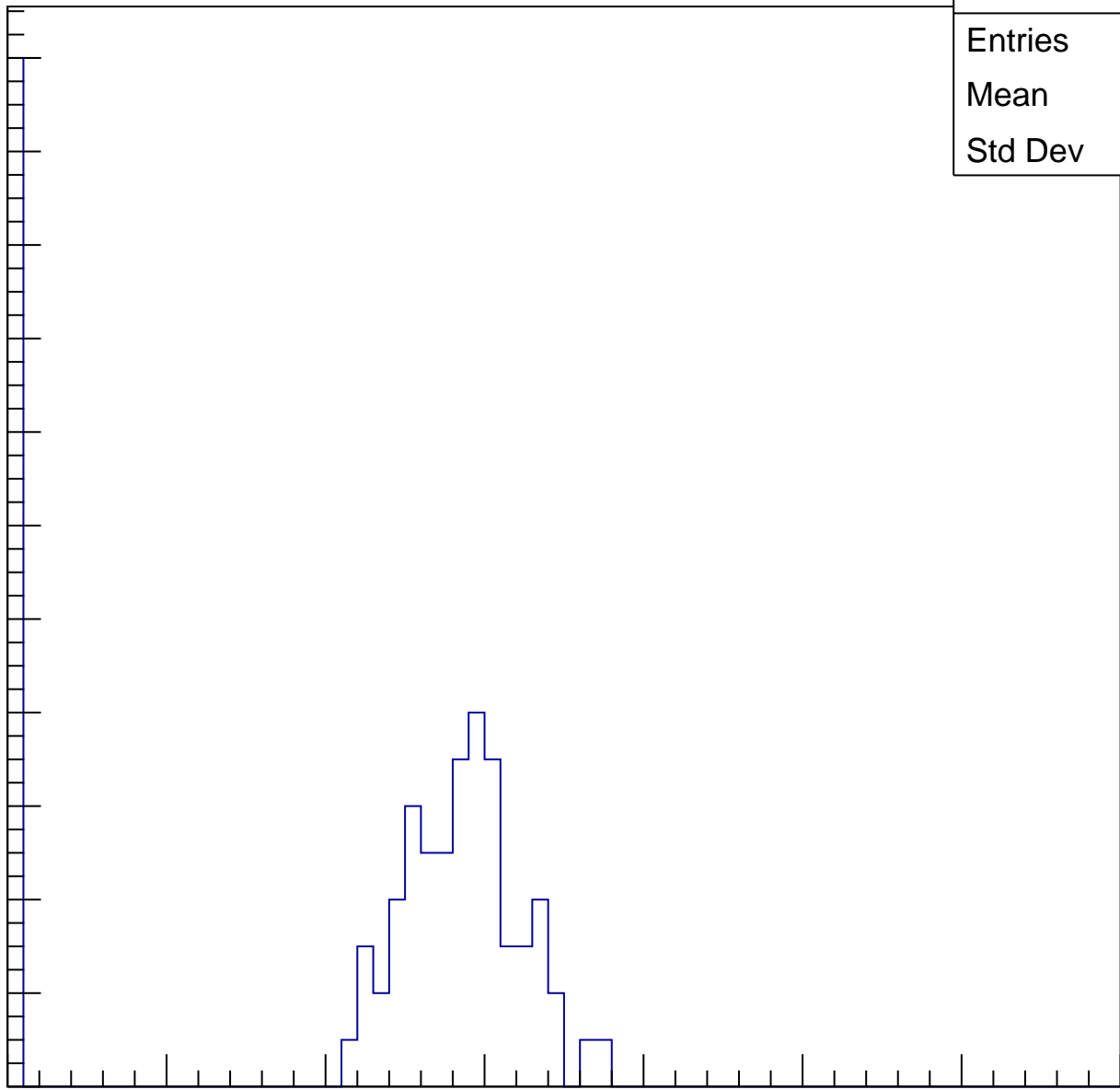
|         |       |
|---------|-------|
| Entries | 84    |
| Mean    | 20.76 |
| Std Dev | 12.74 |

Entry

22  
20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U4-ch112, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 94    |
| Mean    | 31.02 |
| Std Dev | 12.92 |

Entry

12

10

8

6

4

2

0

0

10

20

30

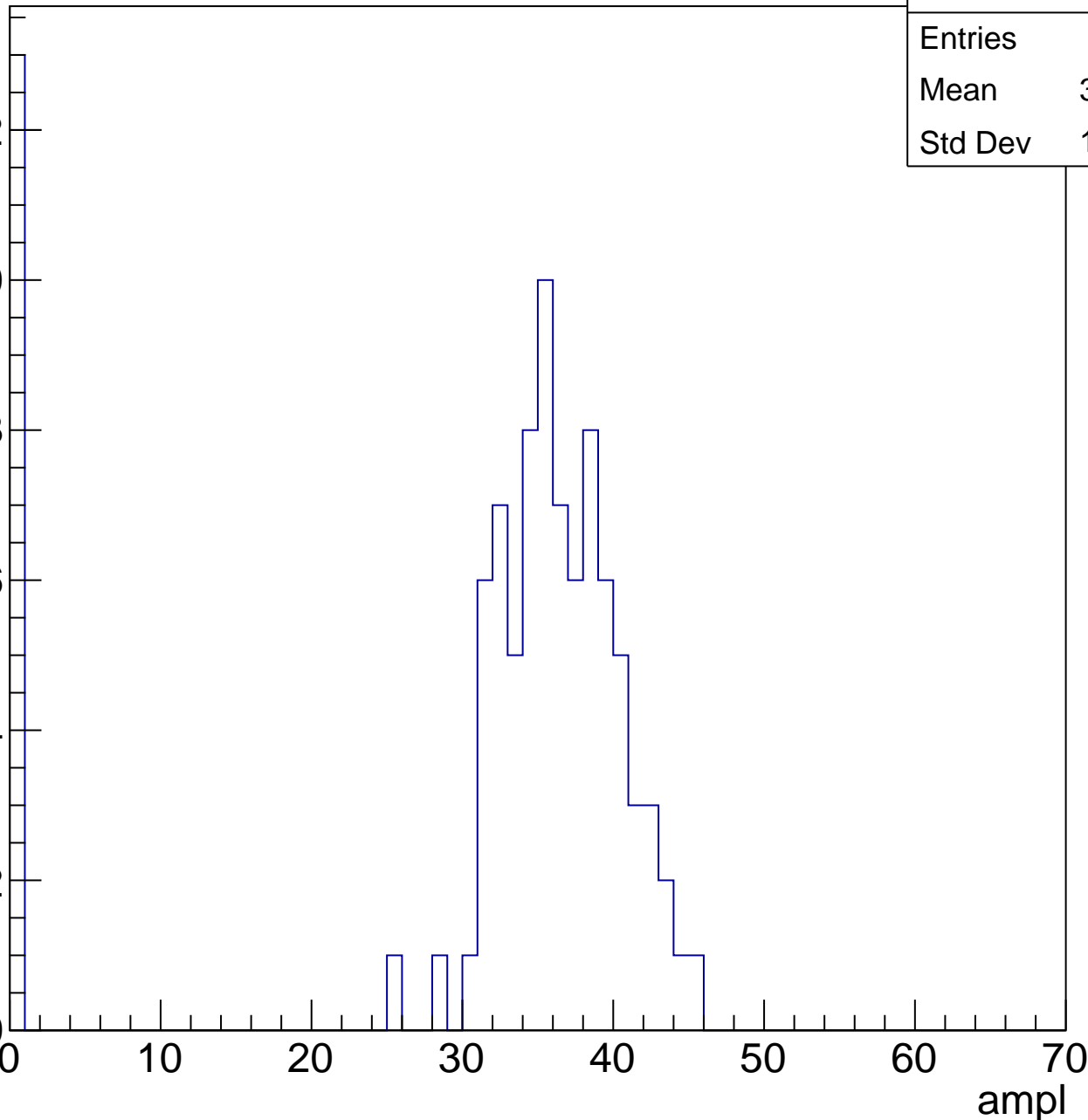
40

50

60

70

ampl

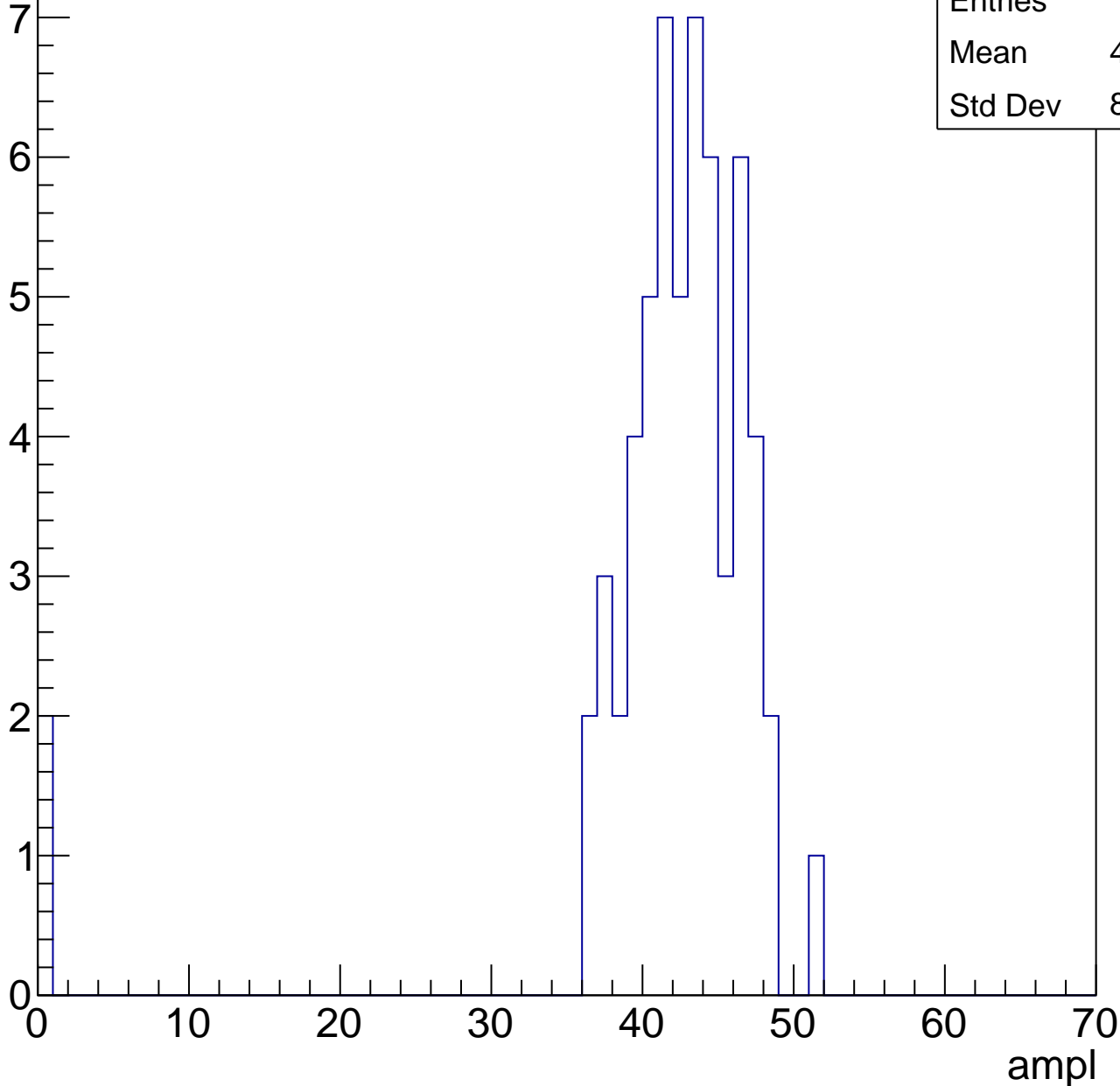


# B1L103S, U4-ch112, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 59    |
| Mean    | 41.07 |
| Std Dev | 8.362 |

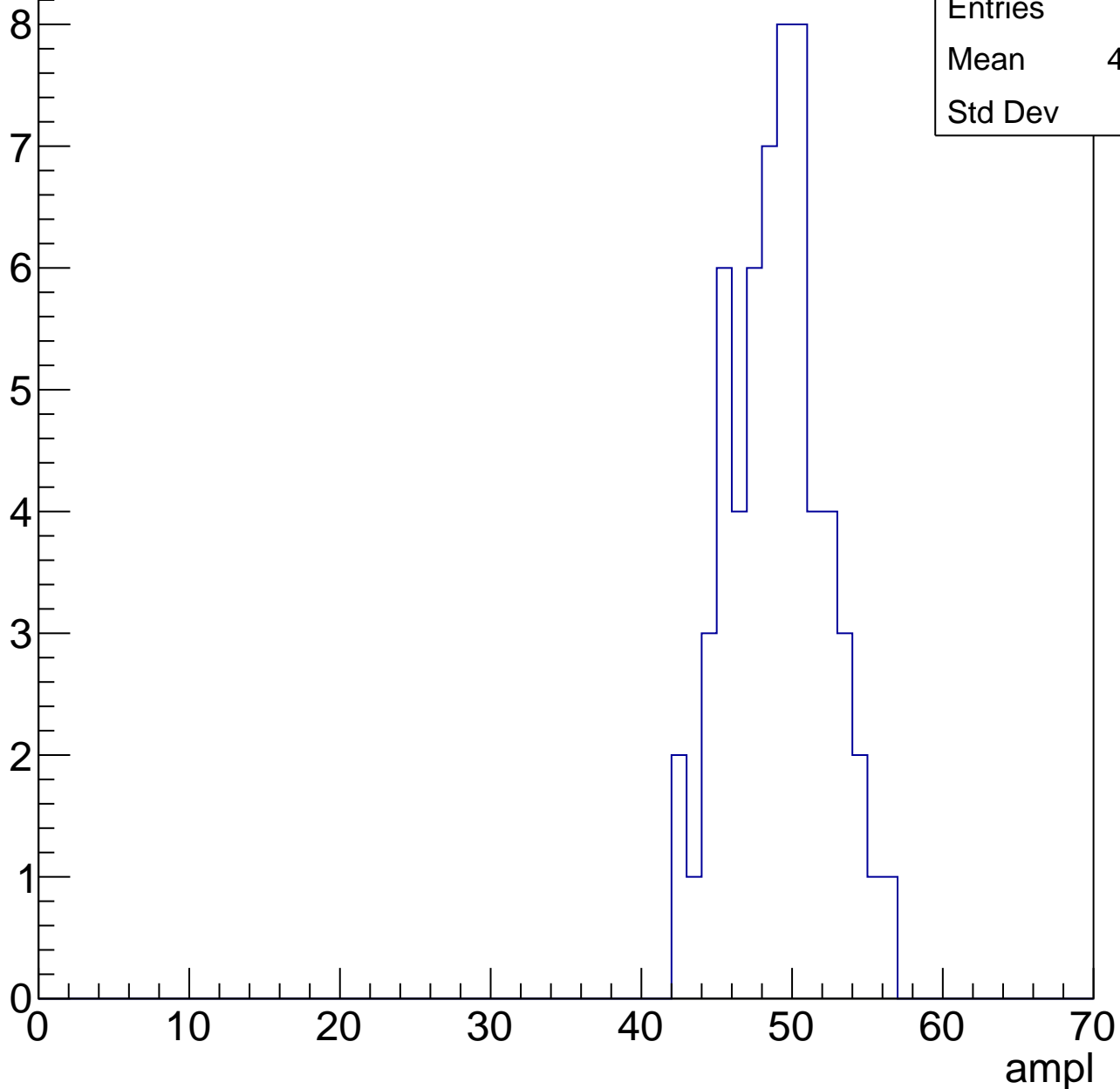


# B1L103S, U4-ch112, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 60    |
| Mean    | 48.55 |
| Std Dev | 3.17  |

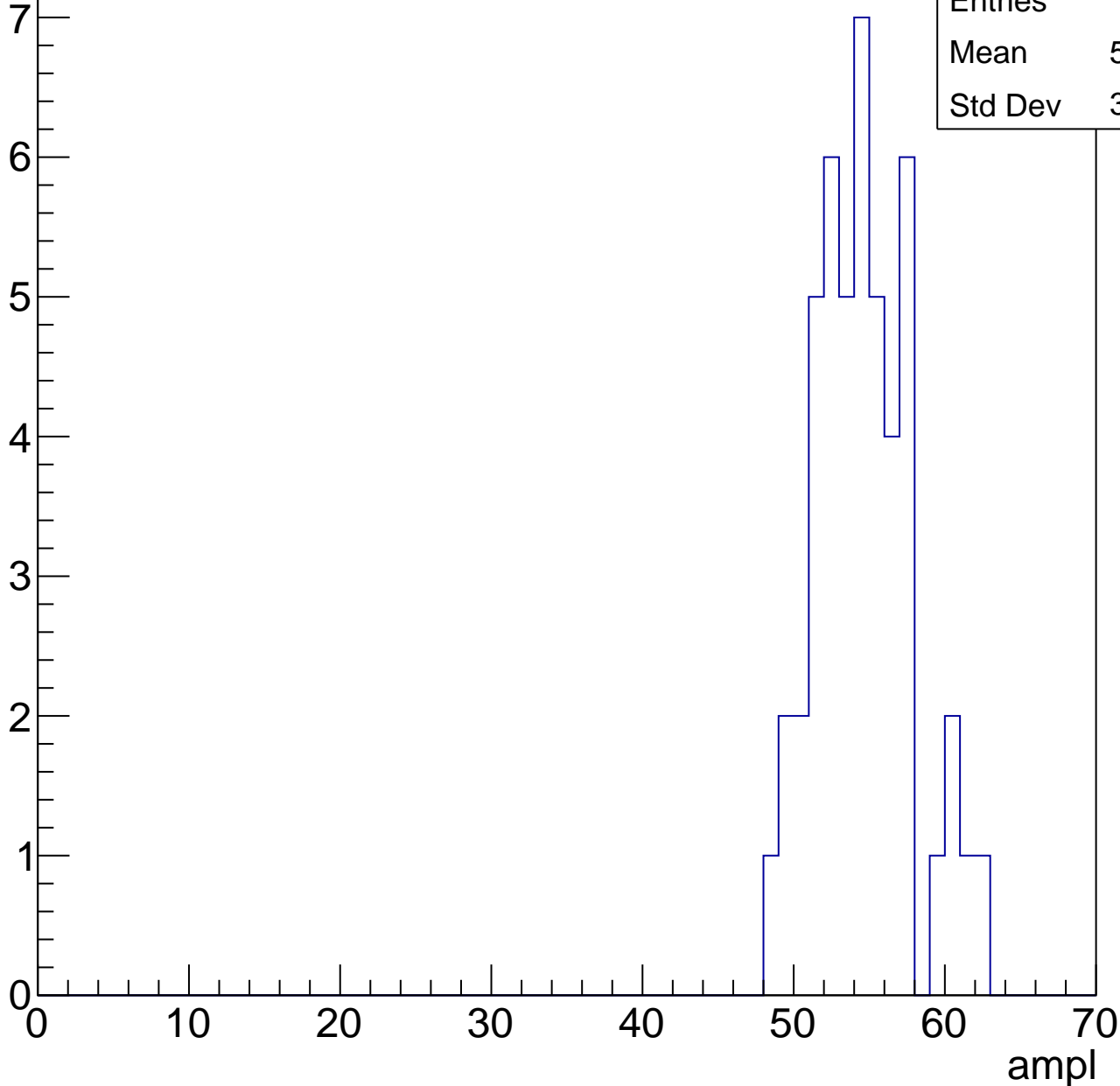


# B1L103S, U4-ch112, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 48    |
| Mean    | 54.15 |
| Std Dev | 3.149 |



# B1L103S, U4-ch112, adc5

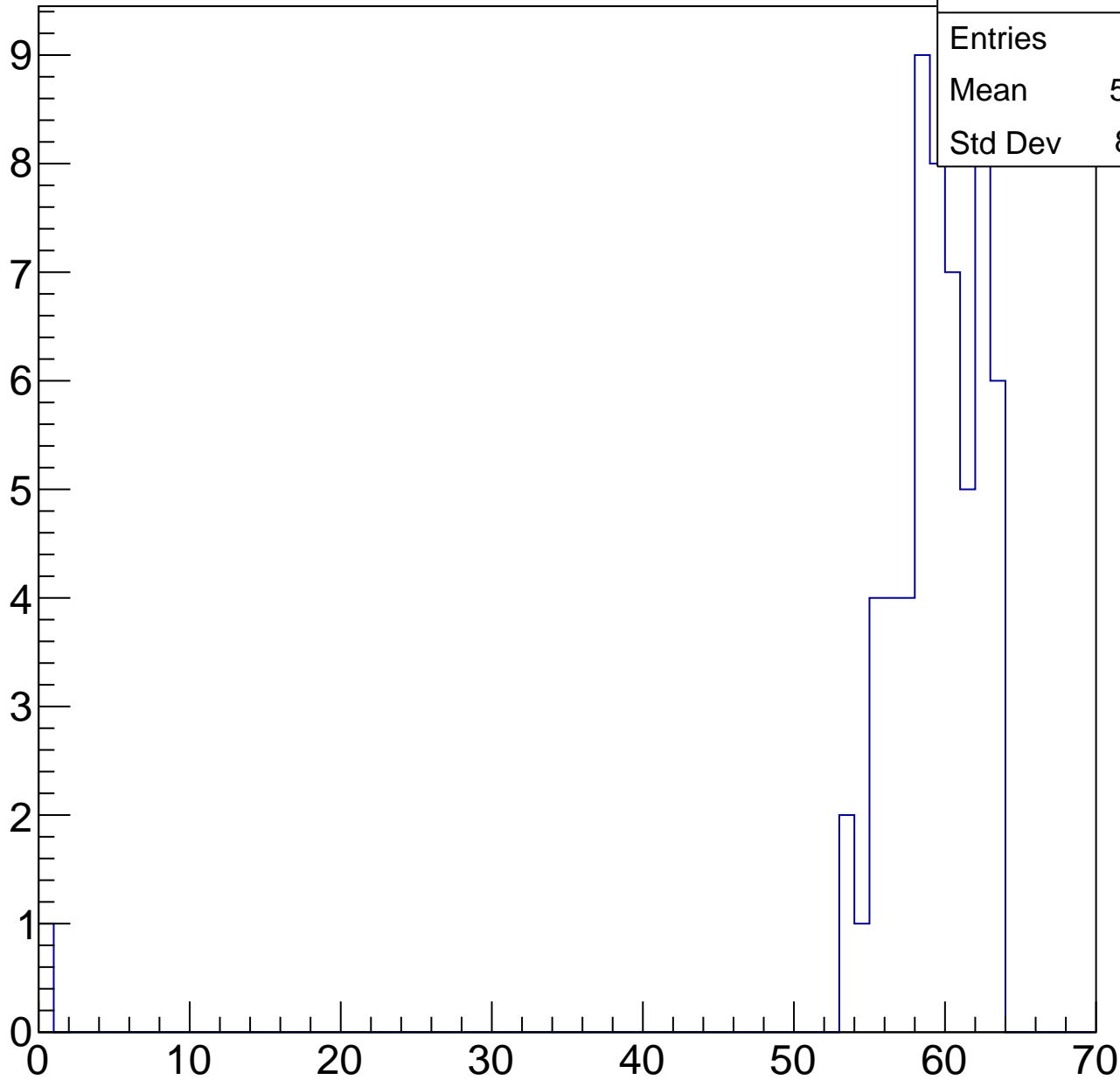
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

|         |       |
|---------|-------|
| Entries | 60    |
| Mean    | 58.12 |
| Std Dev | 8.021 |

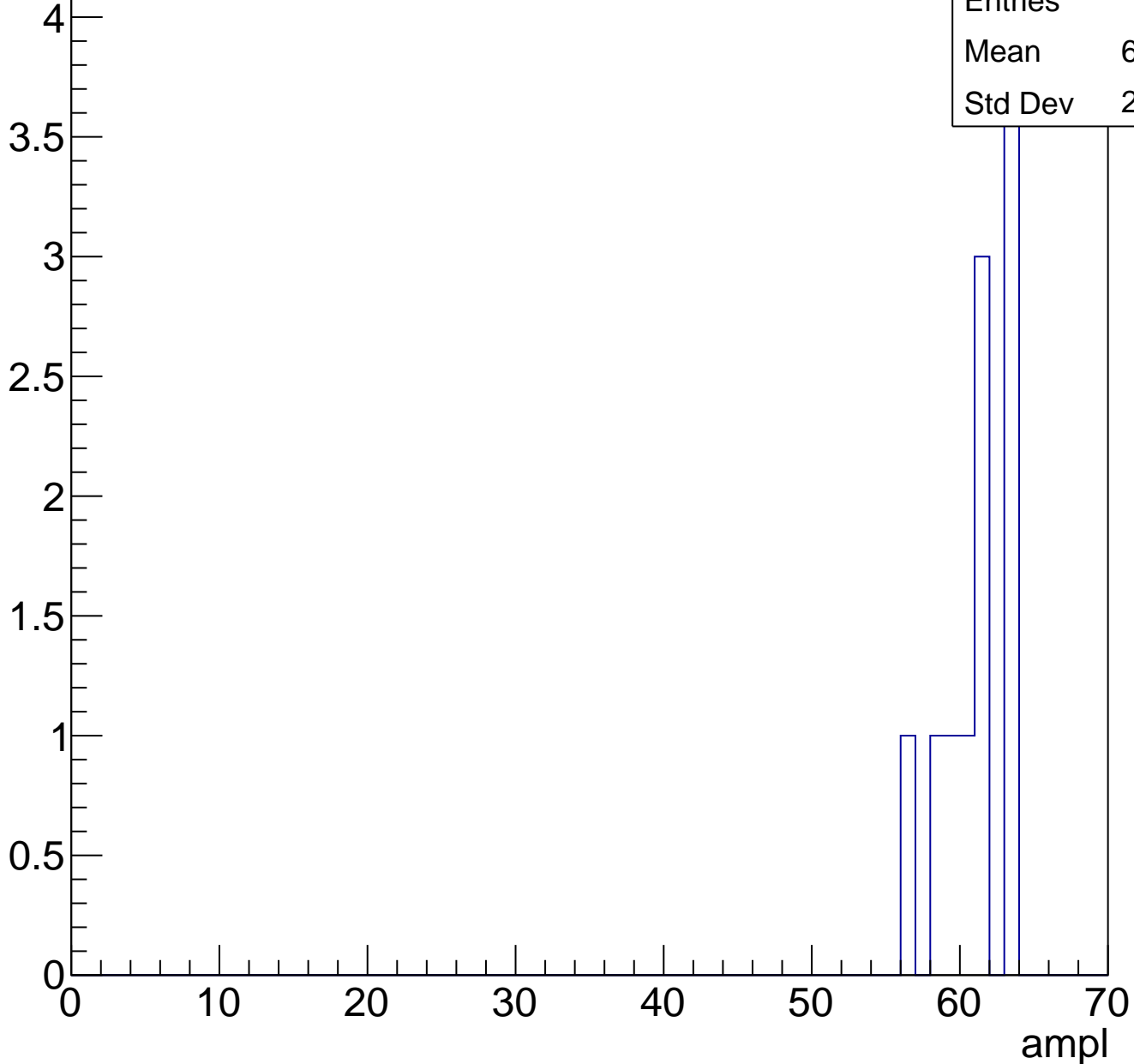
ampl



# B1L103S, U4-ch112, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U4-ch112, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 20    |
| Mean    | 3.05  |
| Std Dev | 13.29 |

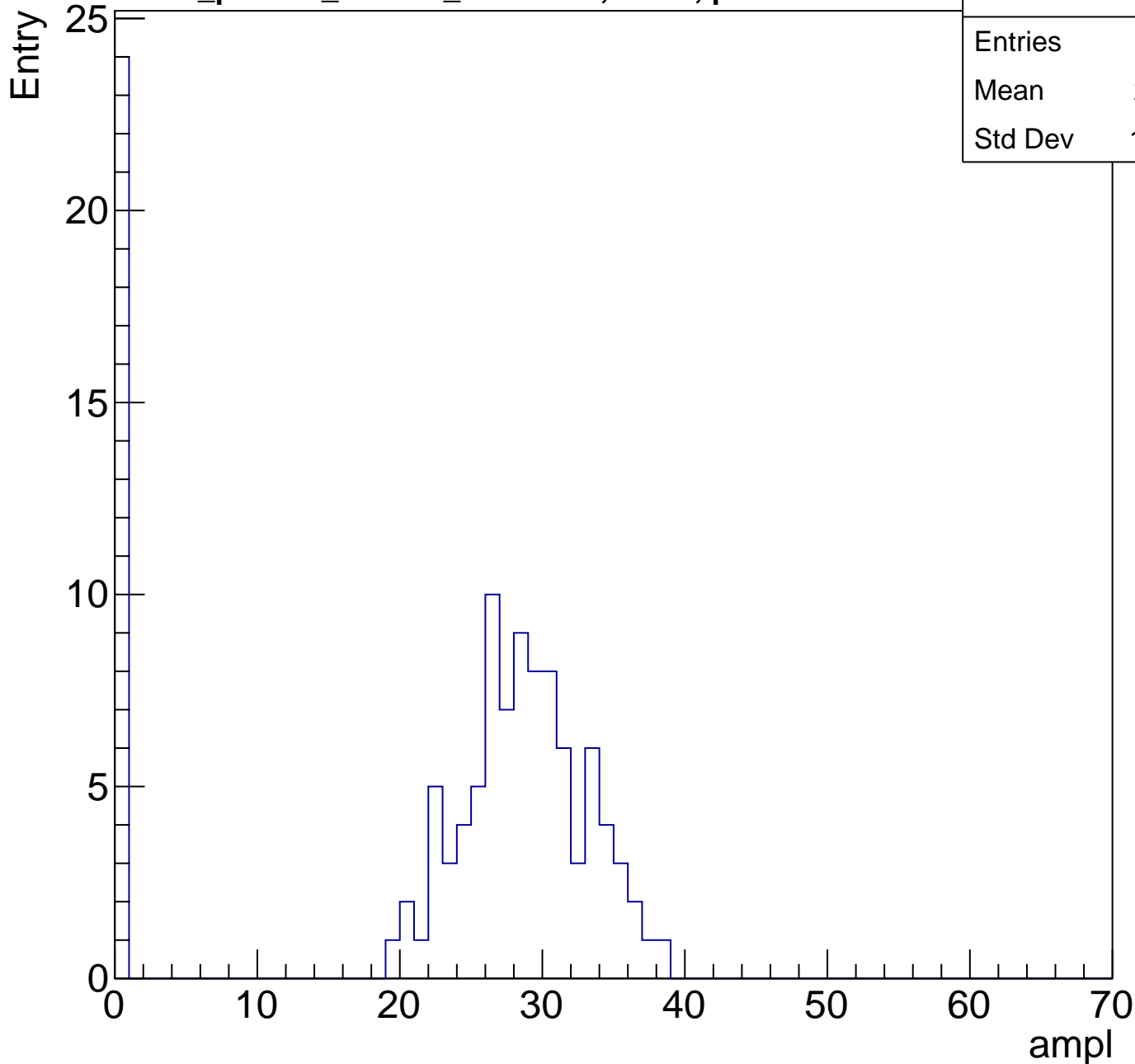
Entry



# B1L103S, U4-ch113, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 113   |
| Mean    | 22.31 |
| Std Dev | 12.16 |



# B1L103S, U4-ch113, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 85    |
| Mean    | 30.64 |
| Std Dev | 13.38 |

Entry

12

10

8

6

4

2

0

0

10

20

30

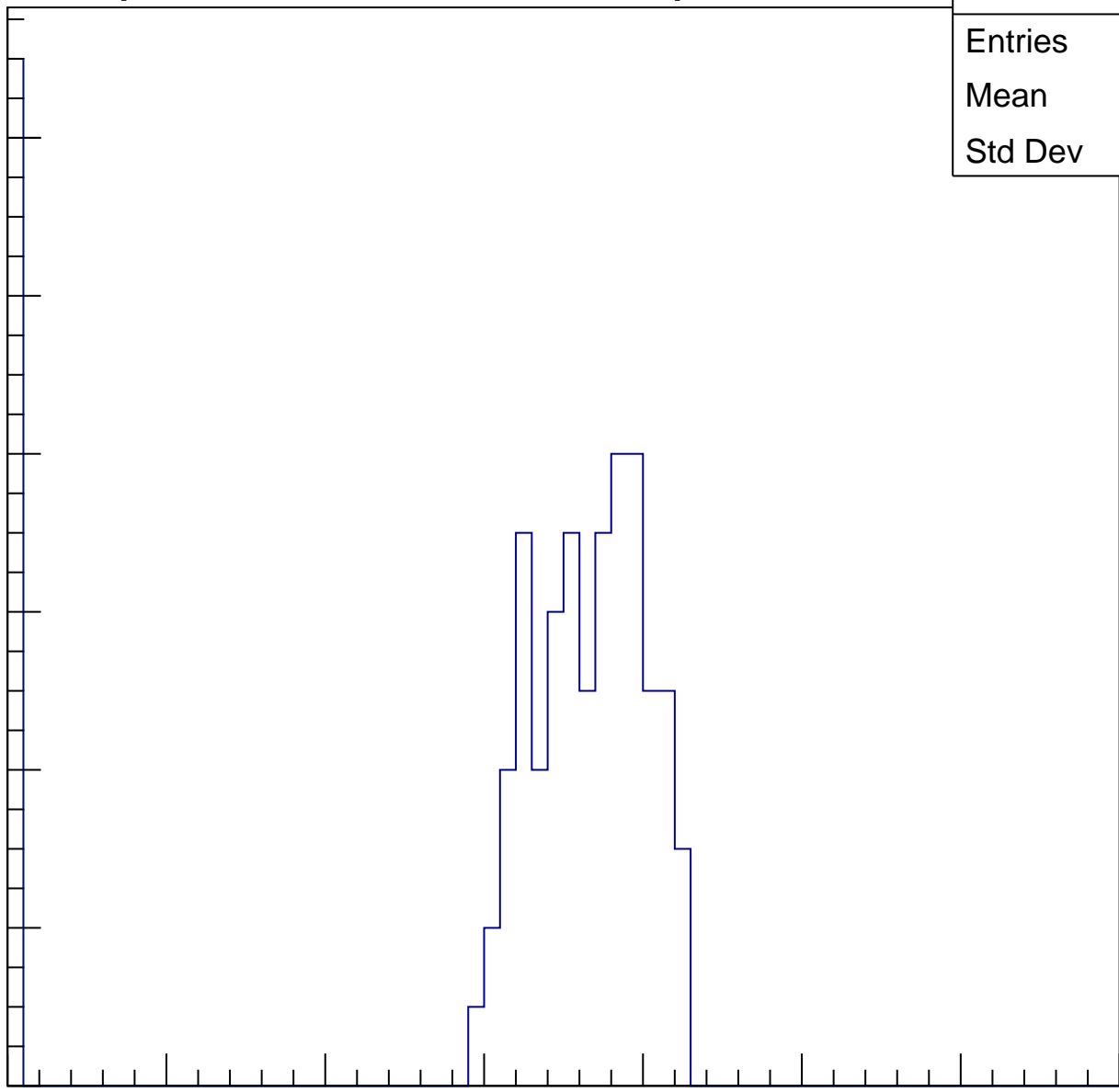
40

50

60

70

ampl

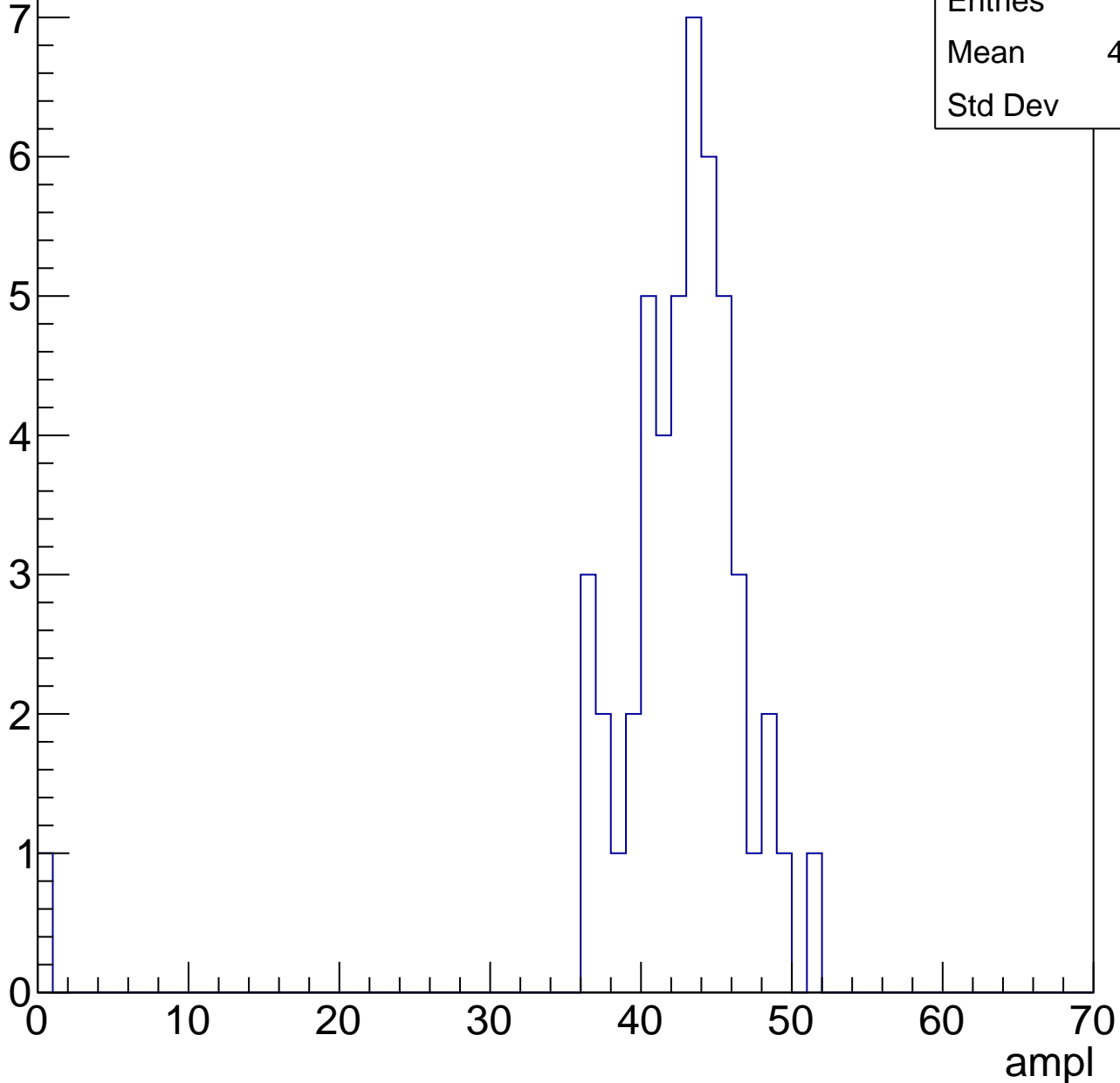


# B1L103S, U4-ch113, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 49    |
| Mean    | 41.69 |
| Std Dev | 6.89  |

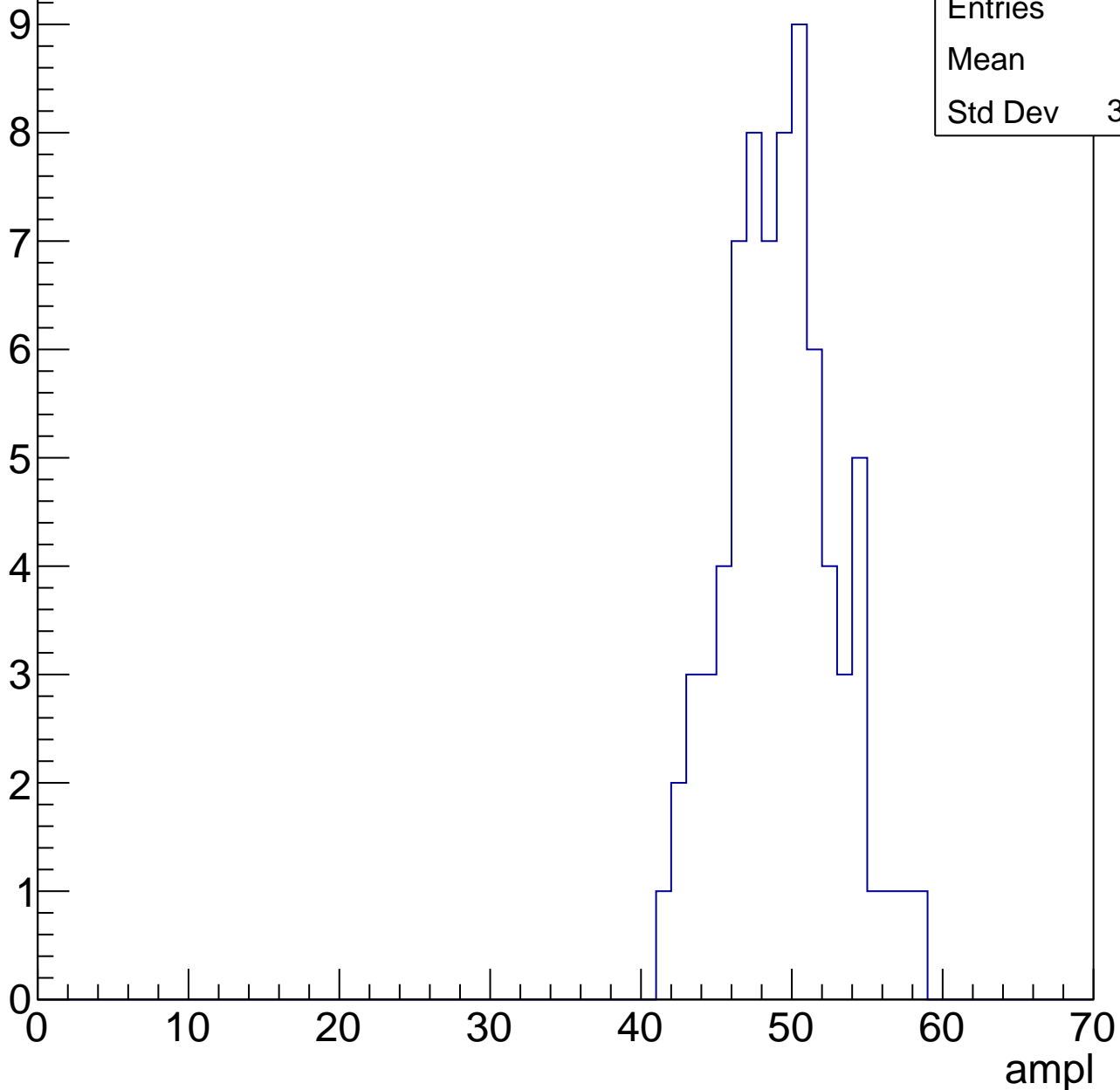


# B1L103S, U4-ch113, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 74    |
| Mean    | 48.8  |
| Std Dev | 3.639 |

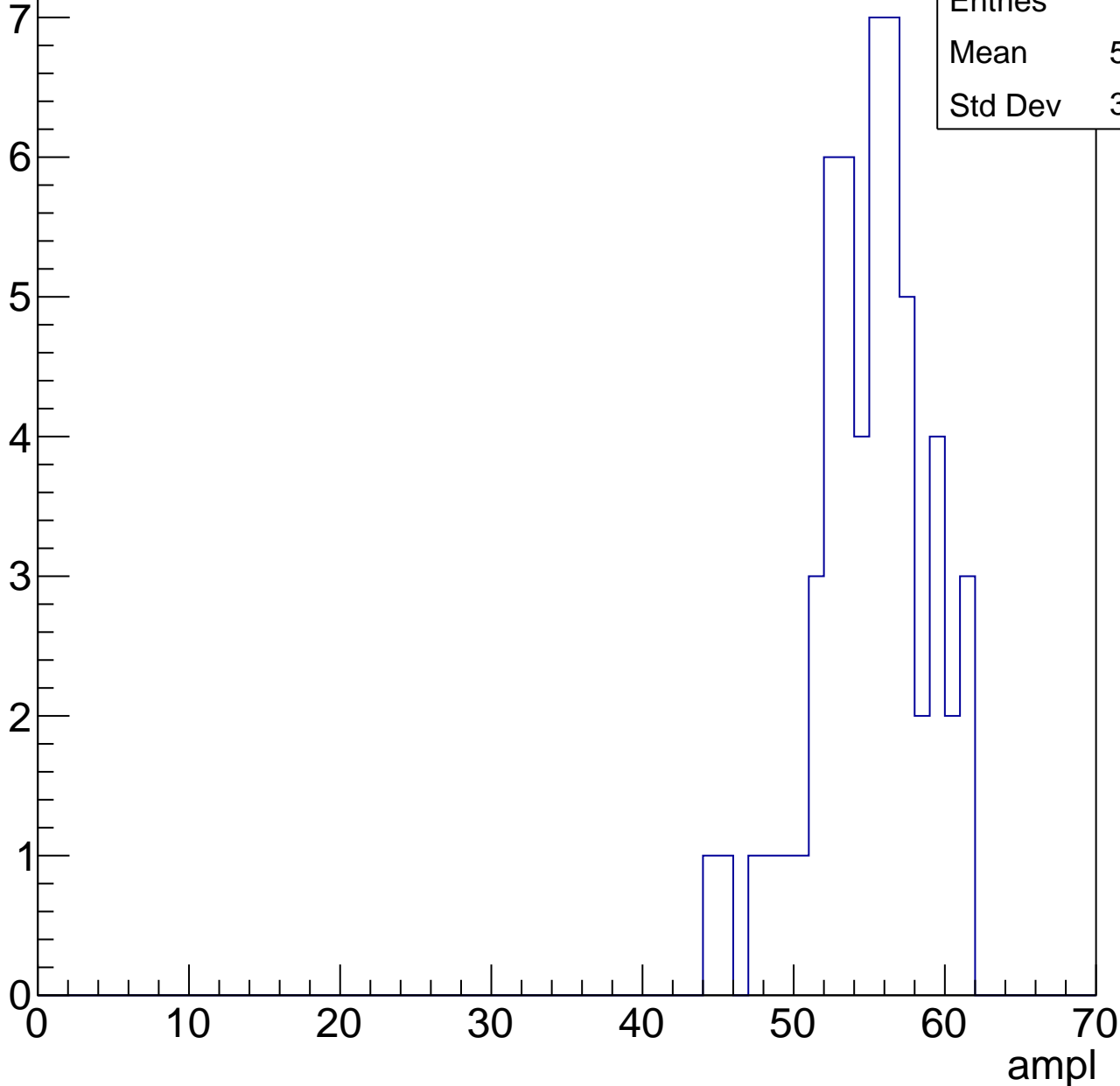


# B1L103S, U4-ch113, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 55    |
| Mean    | 54.53 |
| Std Dev | 3.765 |

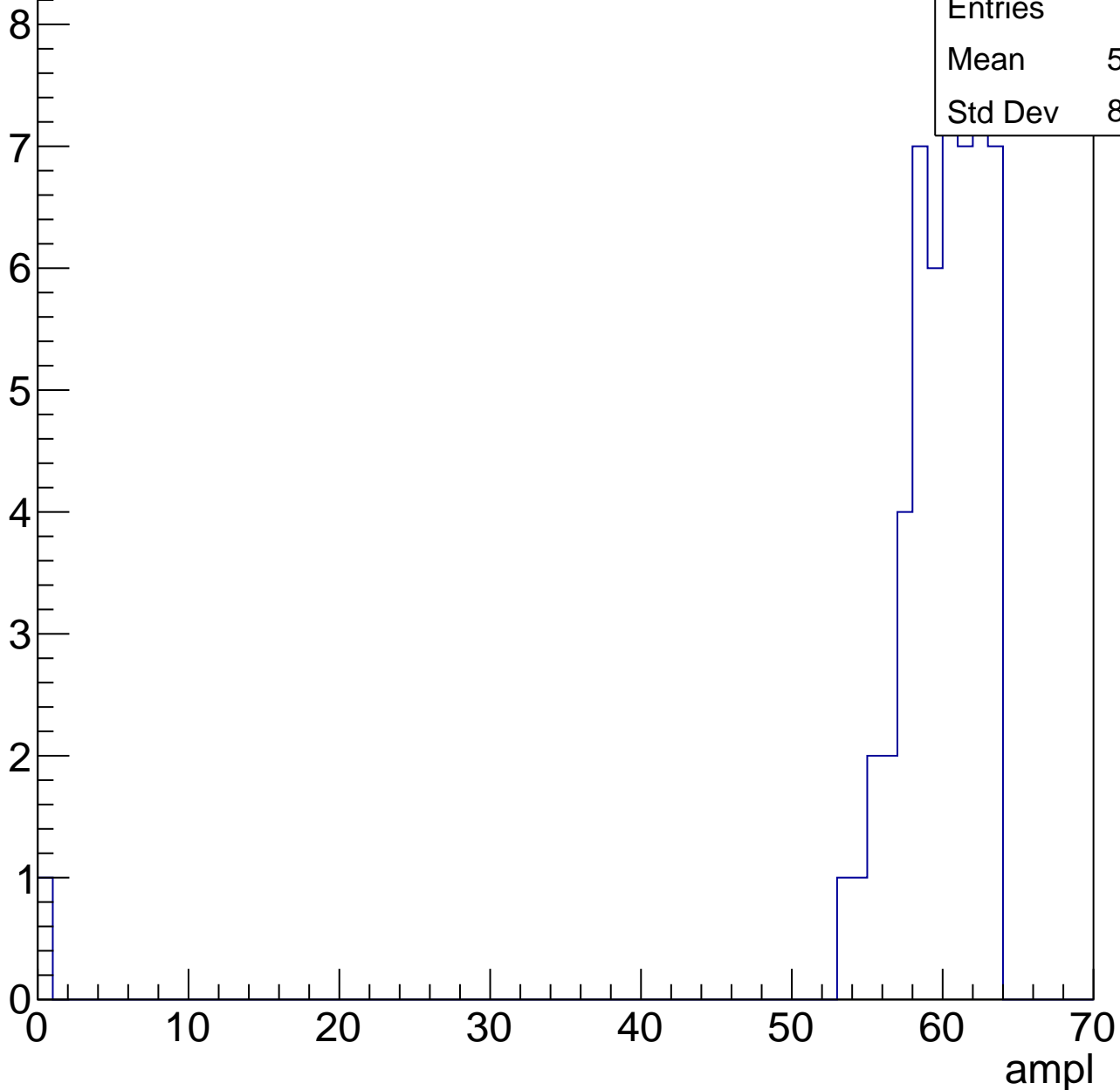


# B1L103S, U4-ch113, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 54    |
| Mean    | 58.54 |
| Std Dev | 8.415 |



# B1L103S, U4-ch113, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U4-ch113, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 20    |
| Mean    | 3.15  |
| Std Dev | 13.73 |

Entry

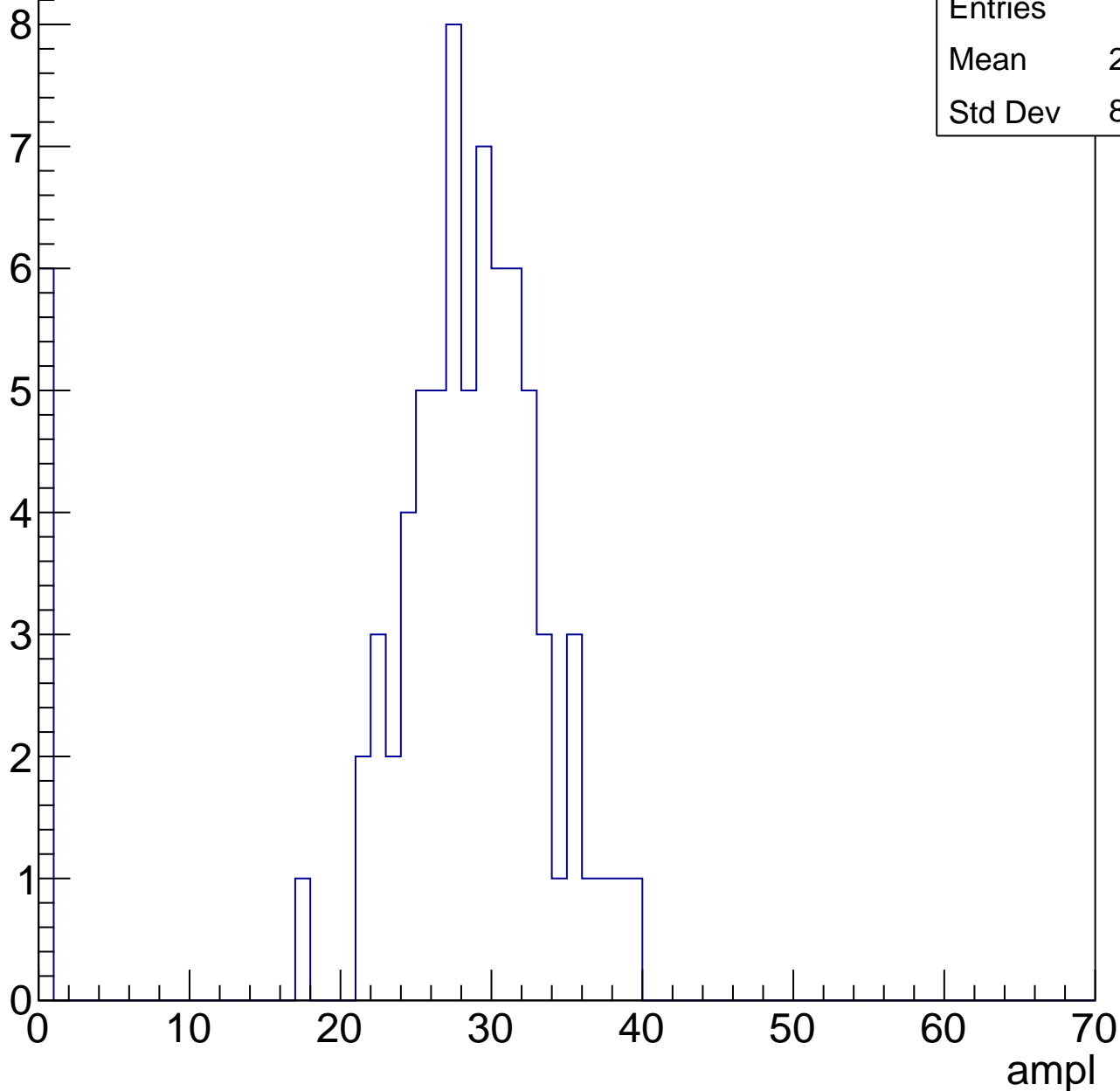


# B1L103S, U4-ch114, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 76    |
| Mean    | 26.25 |
| Std Dev | 8.716 |

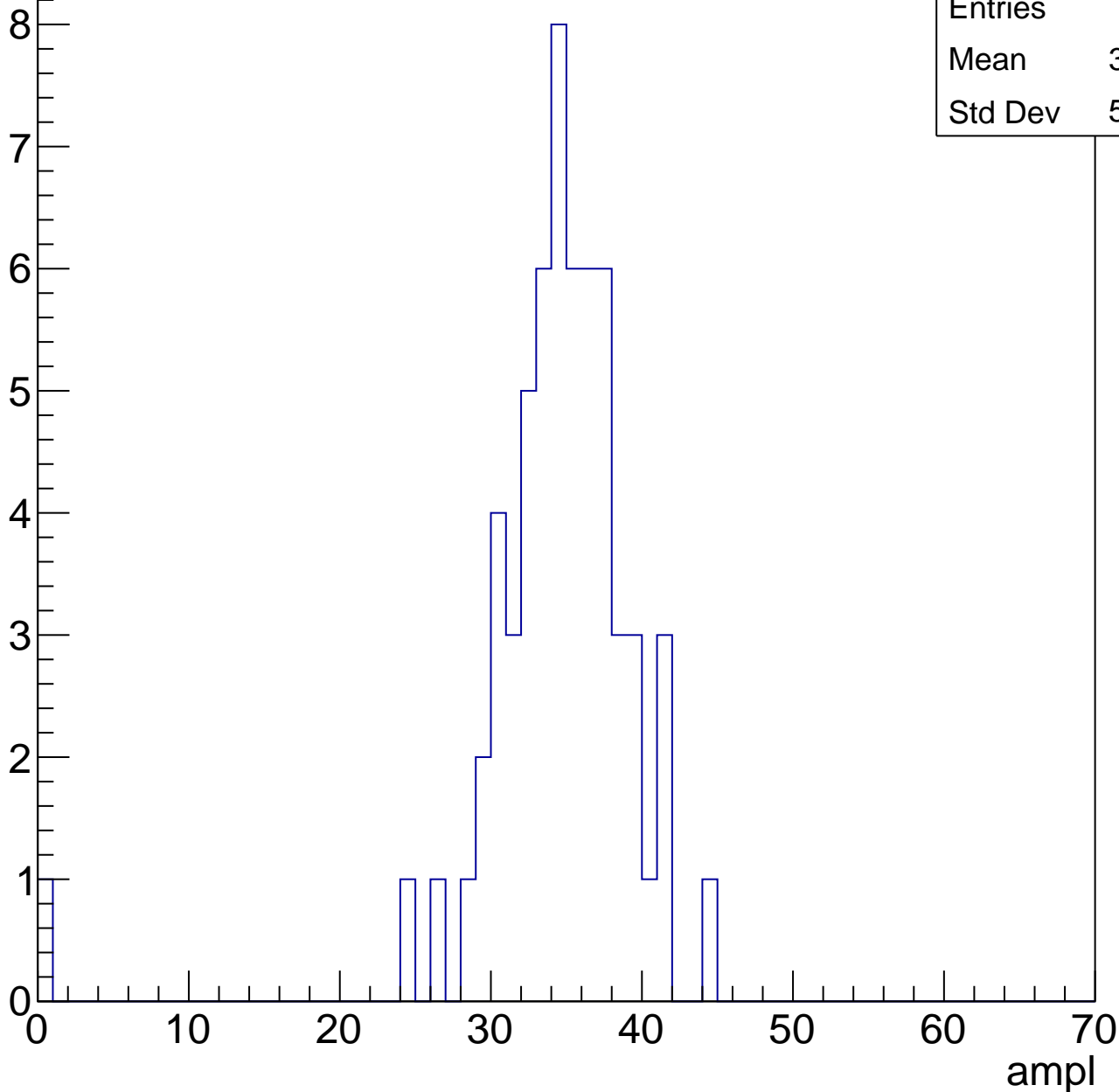


# B1L103S, U4-ch114, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 61    |
| Mean    | 33.85 |
| Std Dev | 5.743 |



# B1L103S, U4-ch114, adc2

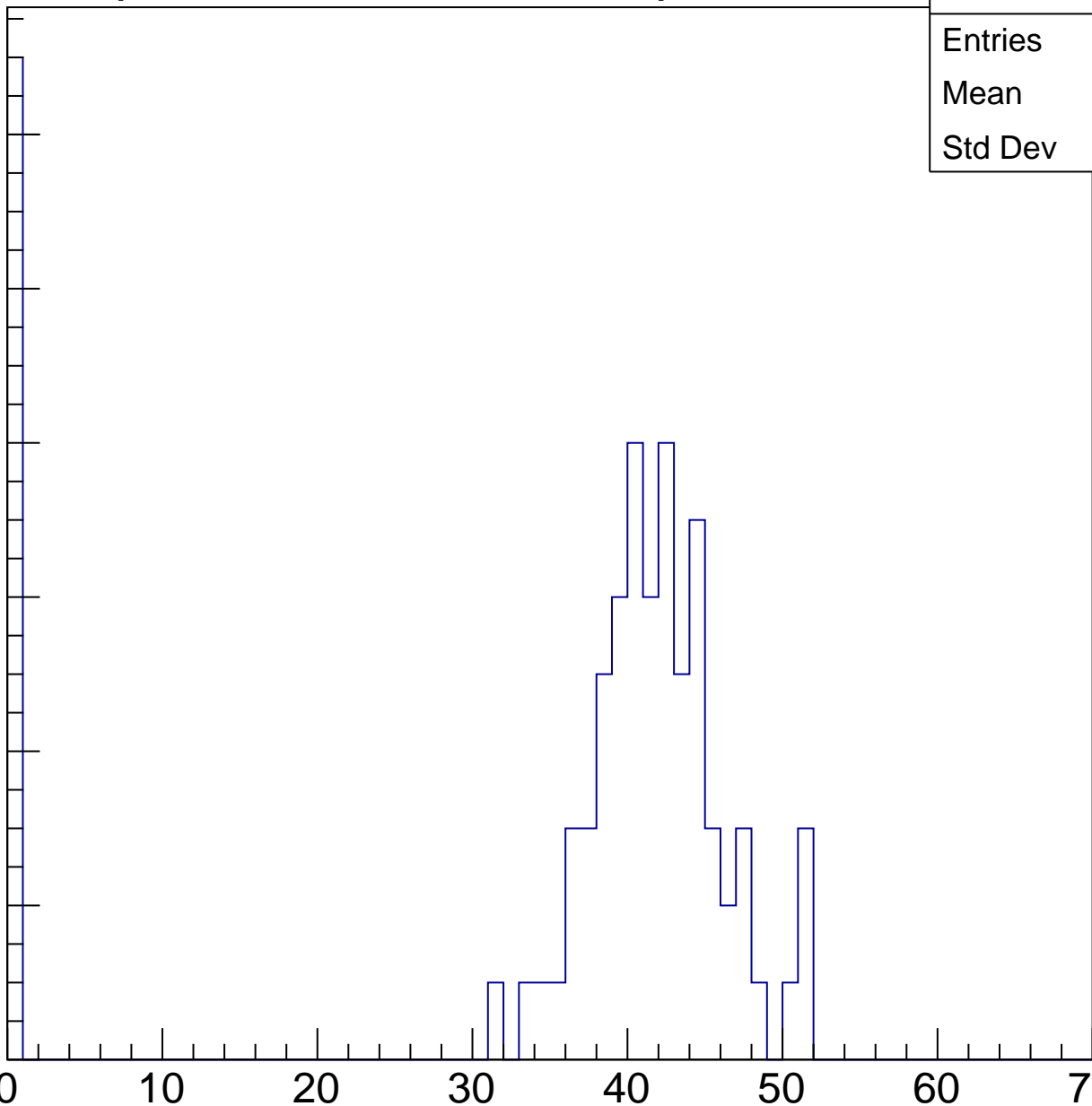
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

12  
10  
8  
6  
4  
2  
0

|         |       |
|---------|-------|
| Entries | 81    |
| Mean    | 34.81 |
| Std Dev | 15.69 |

ampl

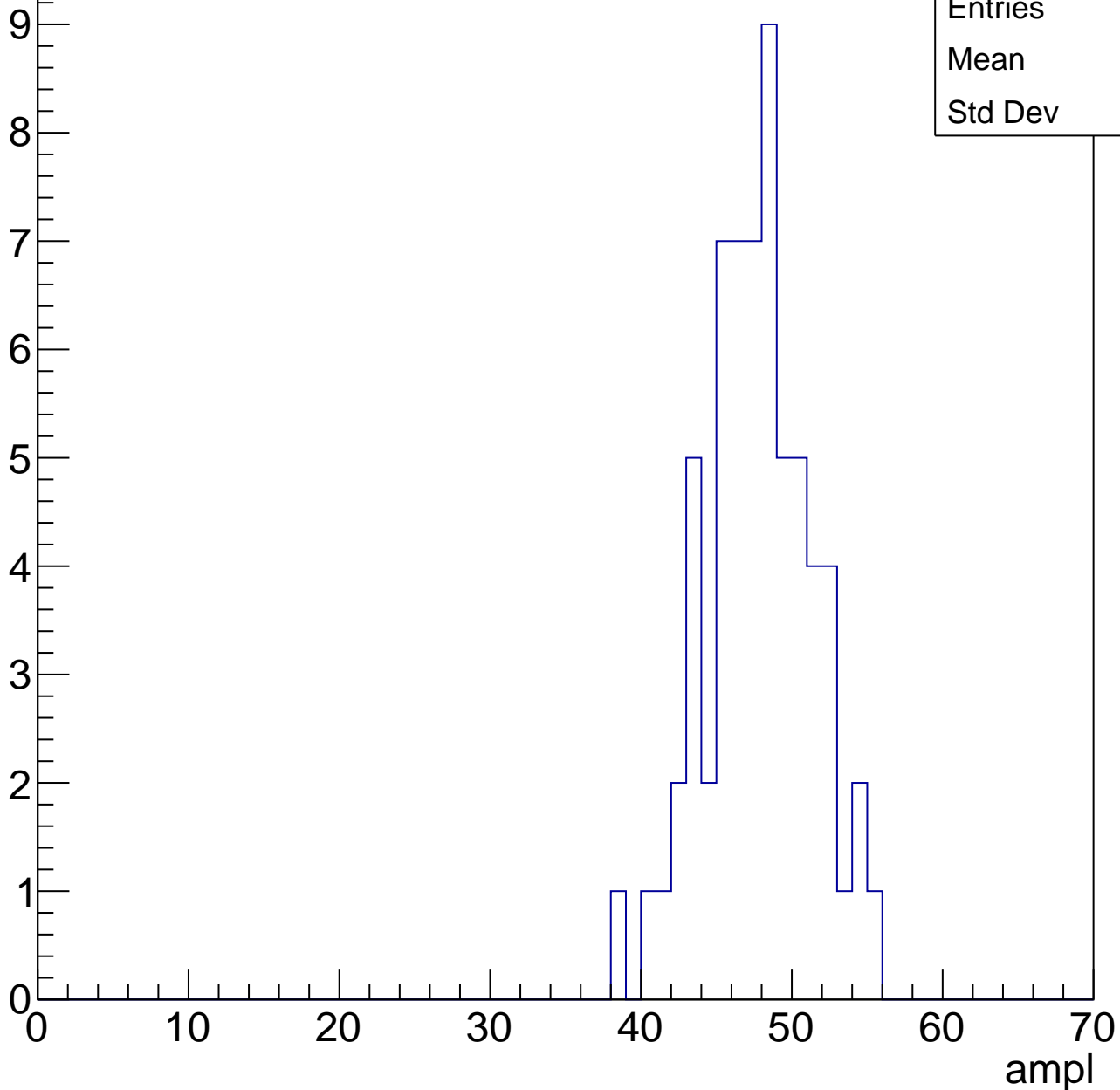


# B1L103S, U4-ch114, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |      |
|---------|------|
| Entries | 64   |
| Mean    | 47.3 |
| Std Dev | 3.49 |

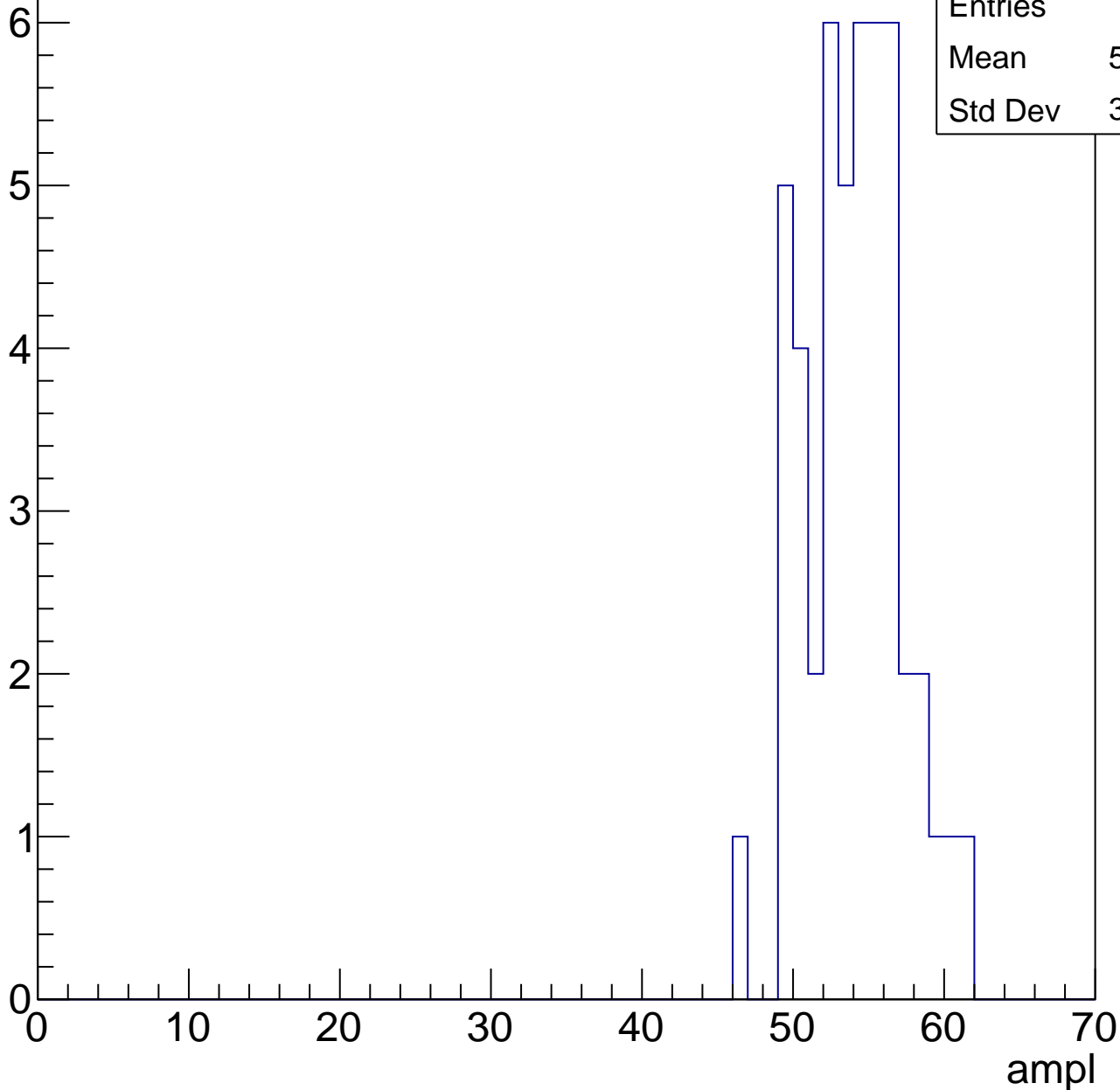


# B1L103S, U4-ch114, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 48    |
| Mean    | 53.54 |
| Std Dev | 3.162 |

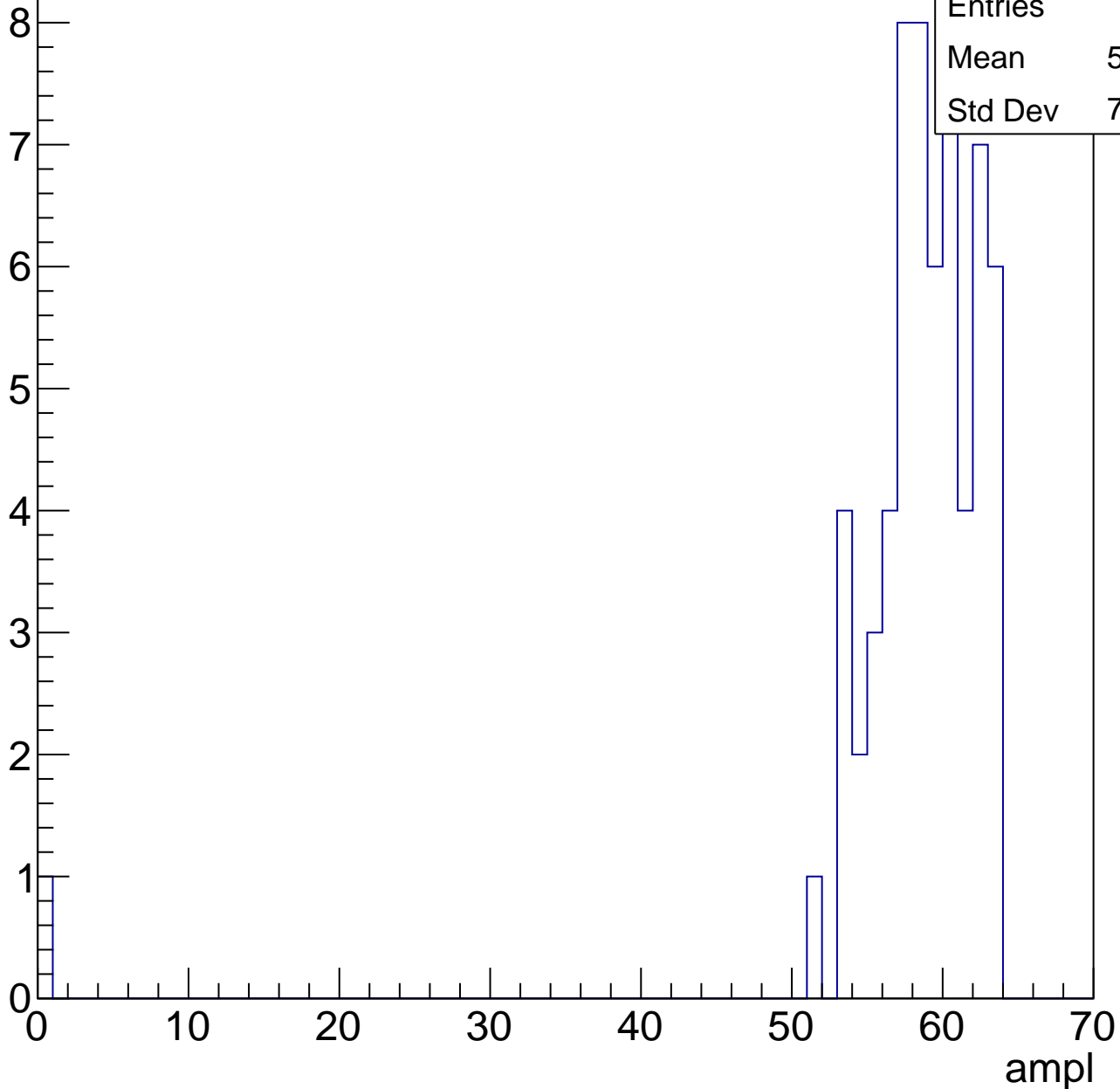


# B1L103S, U4-ch114, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 62    |
| Mean    | 57.58 |
| Std Dev | 7.953 |

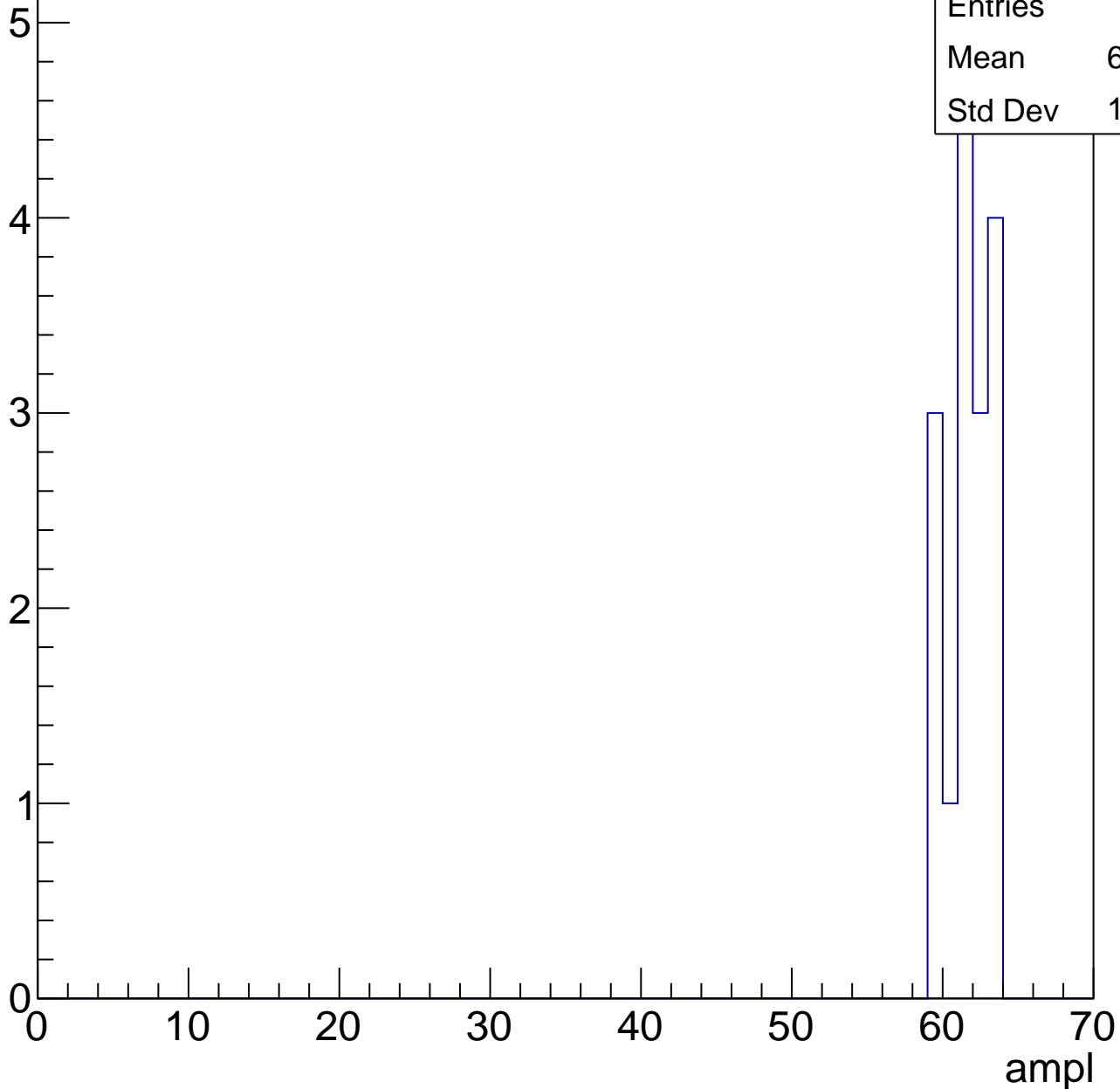


# B1L103S, U4-ch114, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 16    |
| Mean    | 61.25 |
| Std Dev | 1.392 |





# B1L103S, U4-ch114, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |        |
|---------|--------|
| Entries | 18     |
| Mean    | 0.8889 |
| Std Dev | 3.665  |

Entry

16  
14  
12  
10  
8  
6  
4  
2  
0

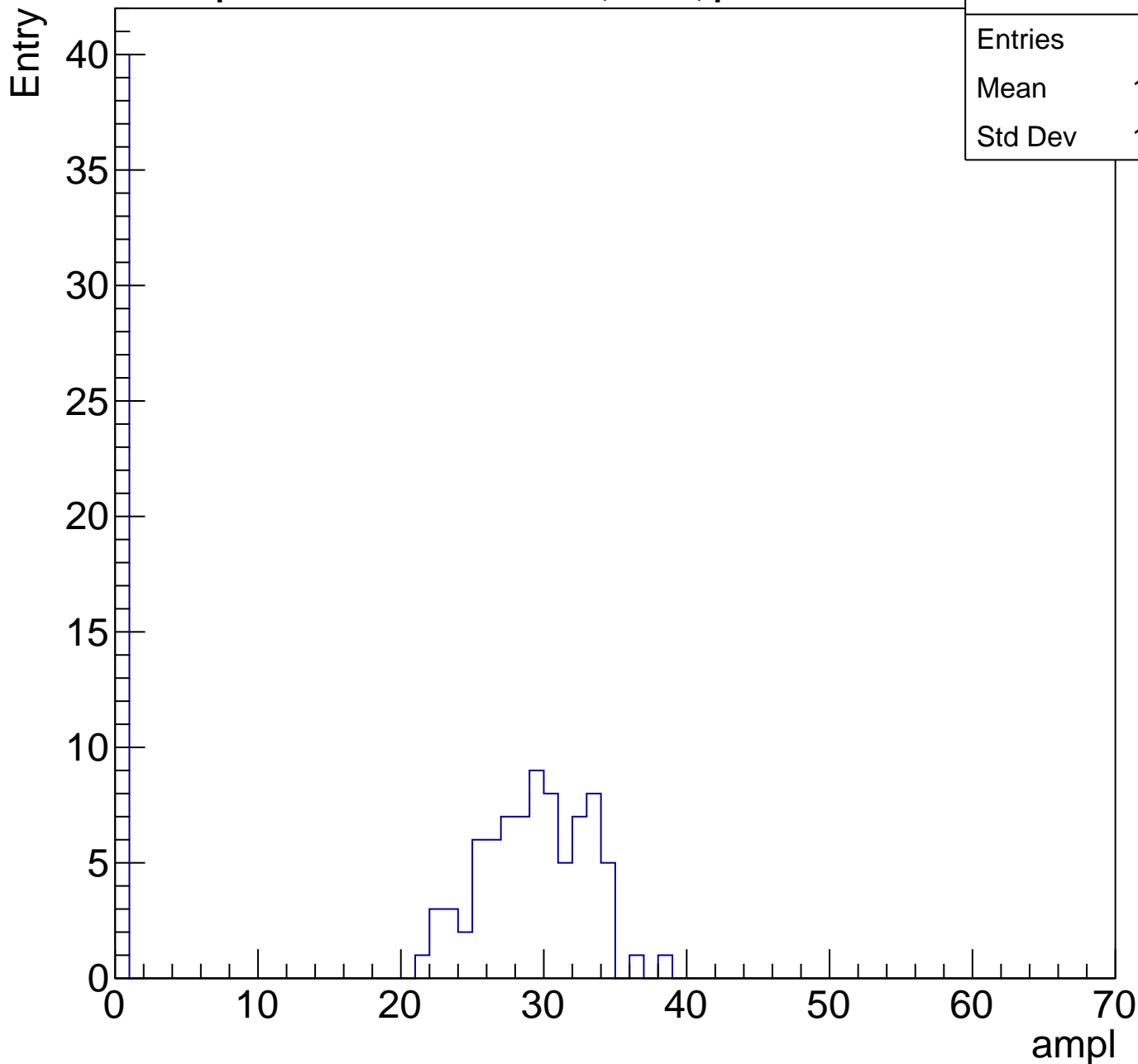
ampl

0 10 20 30 40 50 60 70

# B1L103S, U4-ch115, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 119   |
| Mean    | 19.18 |
| Std Dev | 13.96 |



# B1L103S, U4-ch115, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

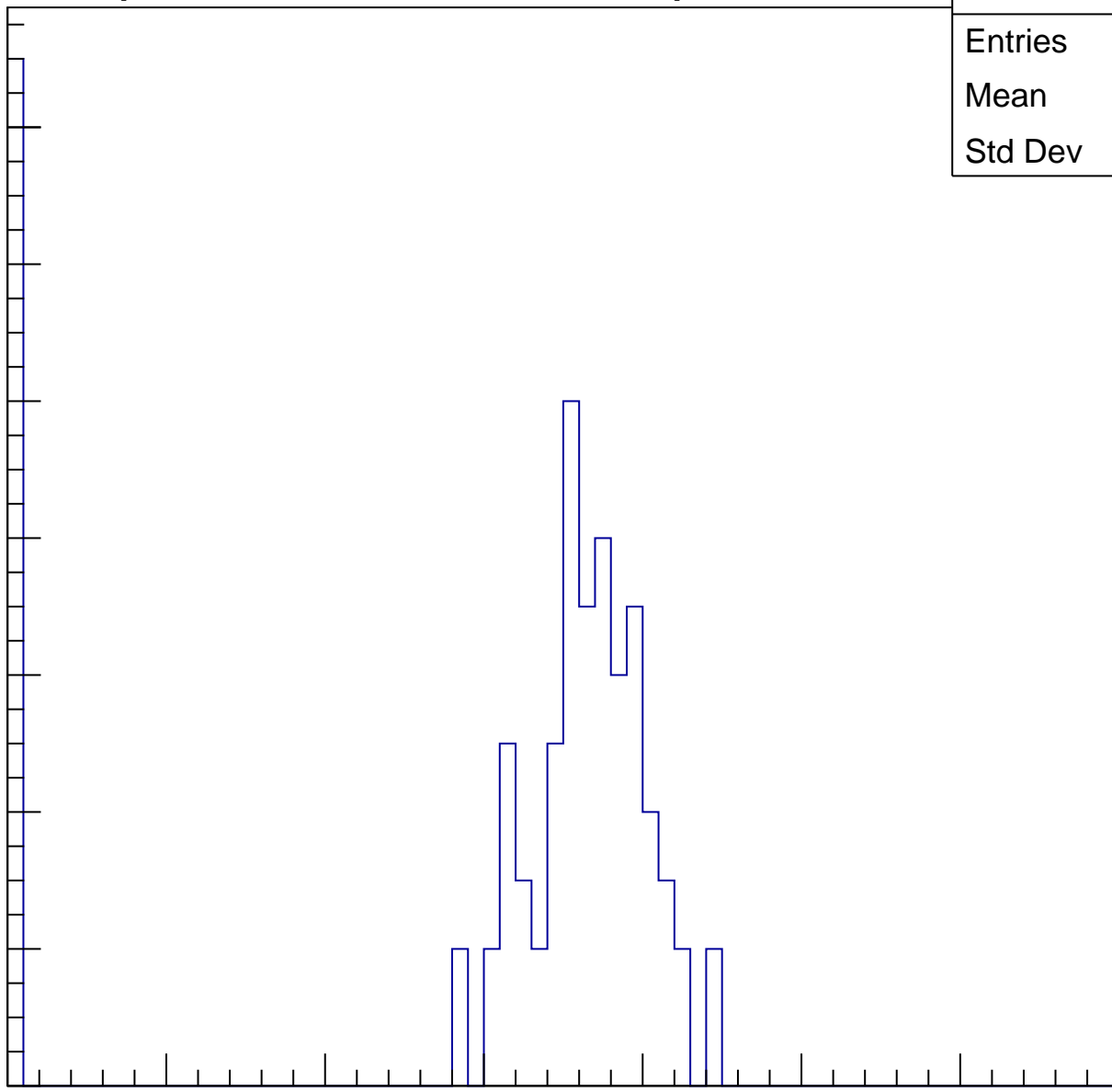
|         |       |
|---------|-------|
| Entries | 83    |
| Mean    | 29.6  |
| Std Dev | 14.27 |

Entry

14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

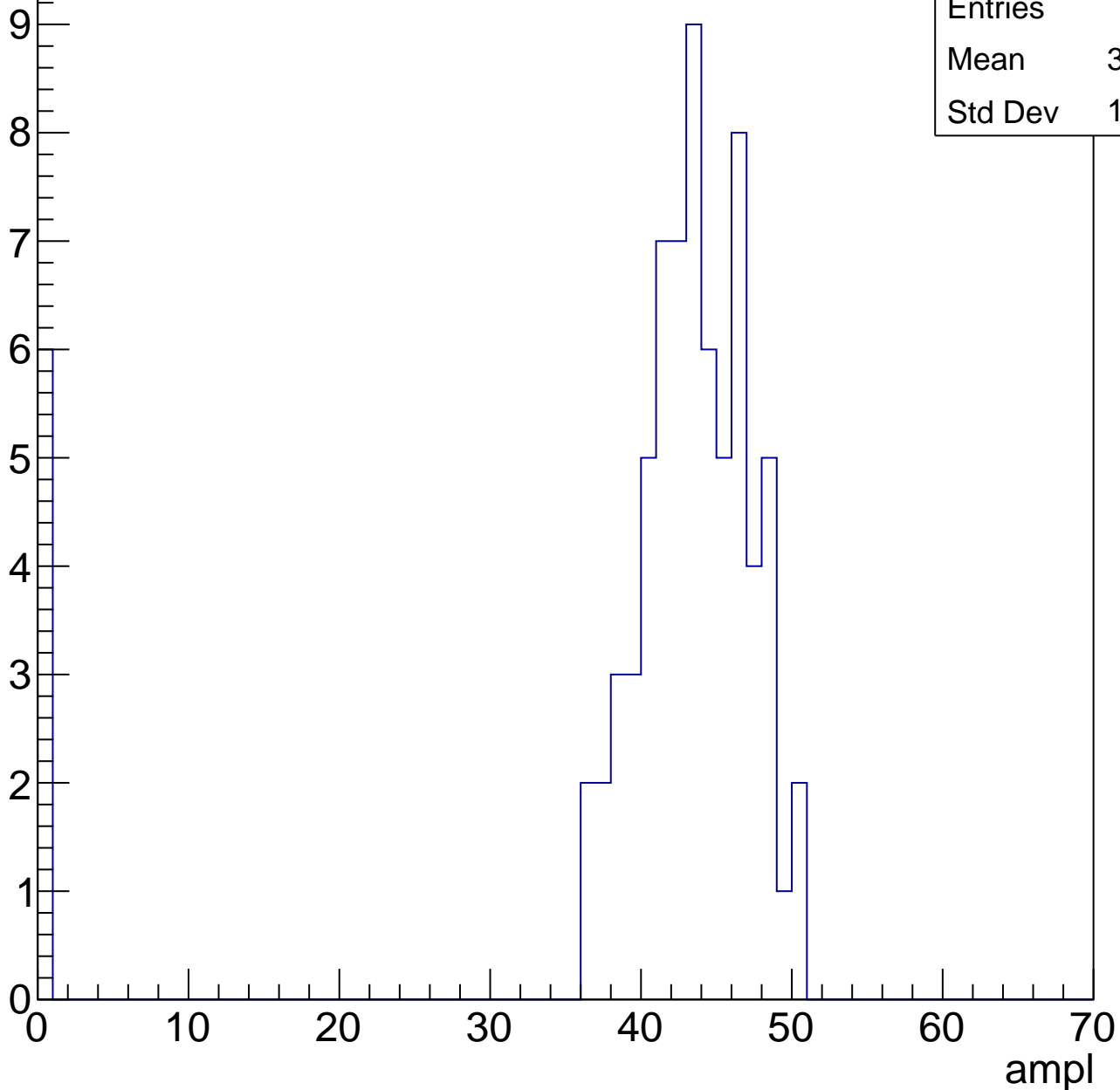


# B1L103S, U4-ch115, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 75    |
| Mean    | 39.72 |
| Std Dev | 12.16 |

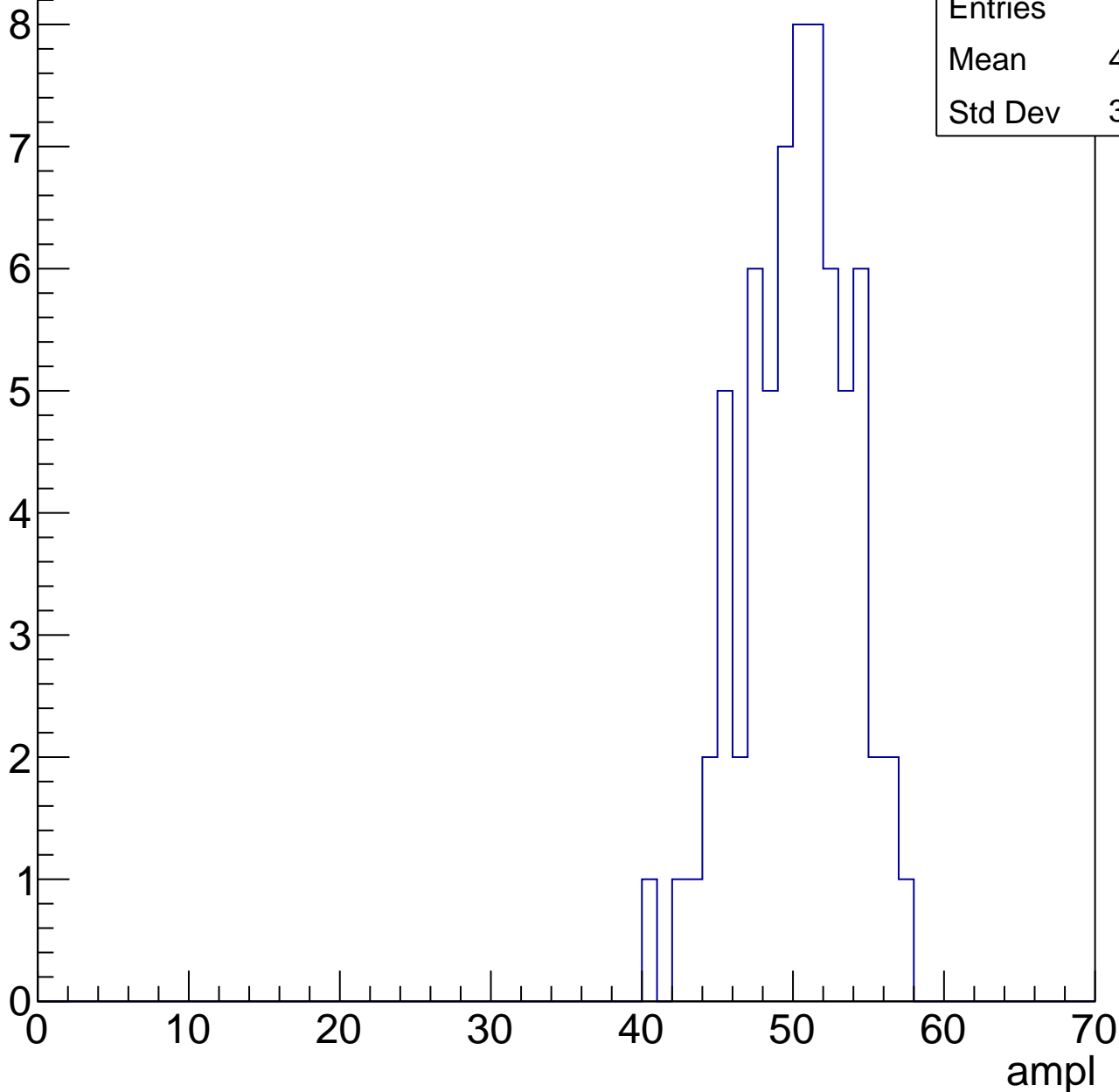


# B1L103S, U4-ch115, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 68    |
| Mean    | 49.75 |
| Std Dev | 3.562 |

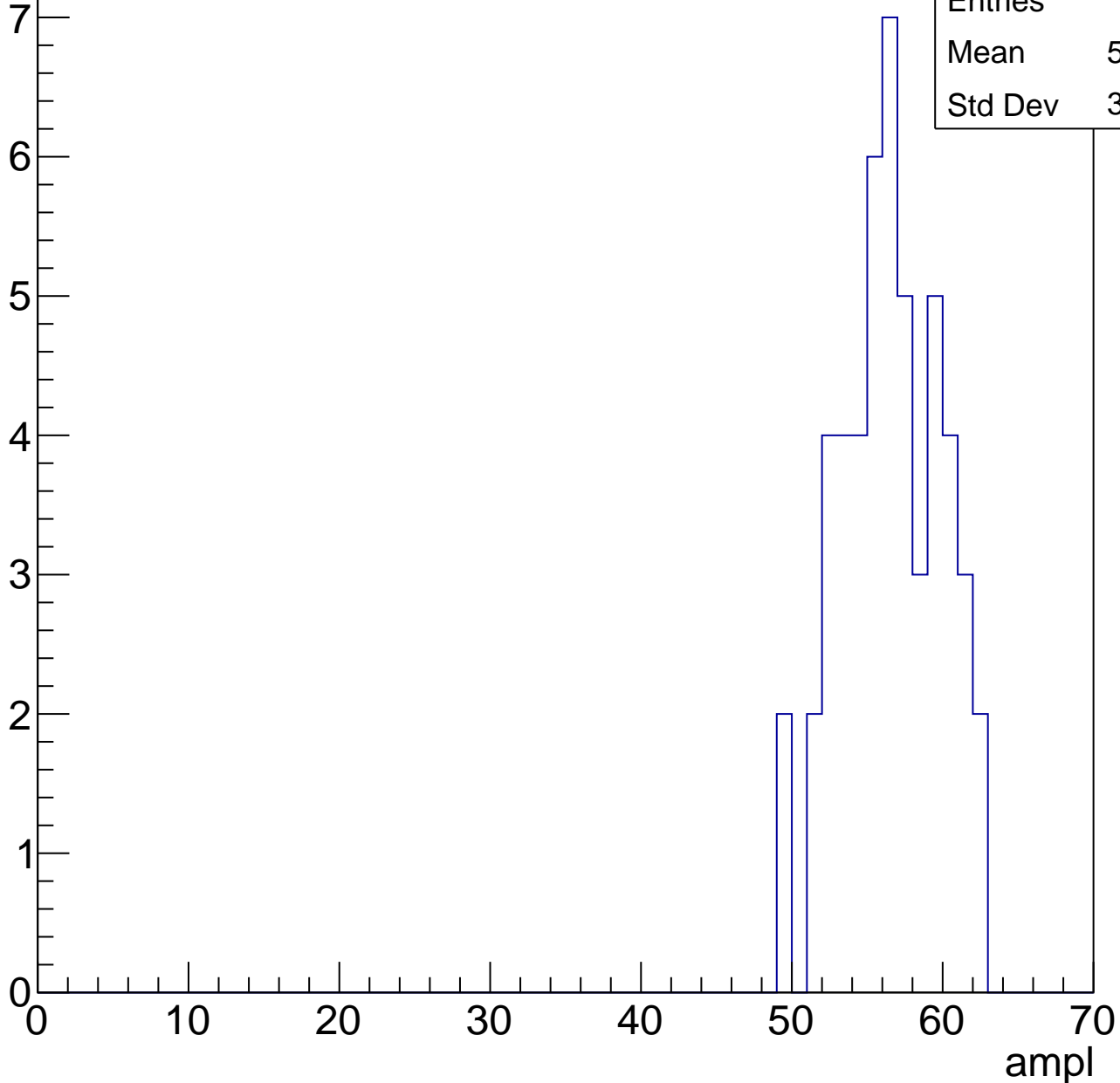


# B1L103S, U4-ch115, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 51    |
| Mean    | 56.06 |
| Std Dev | 3.262 |

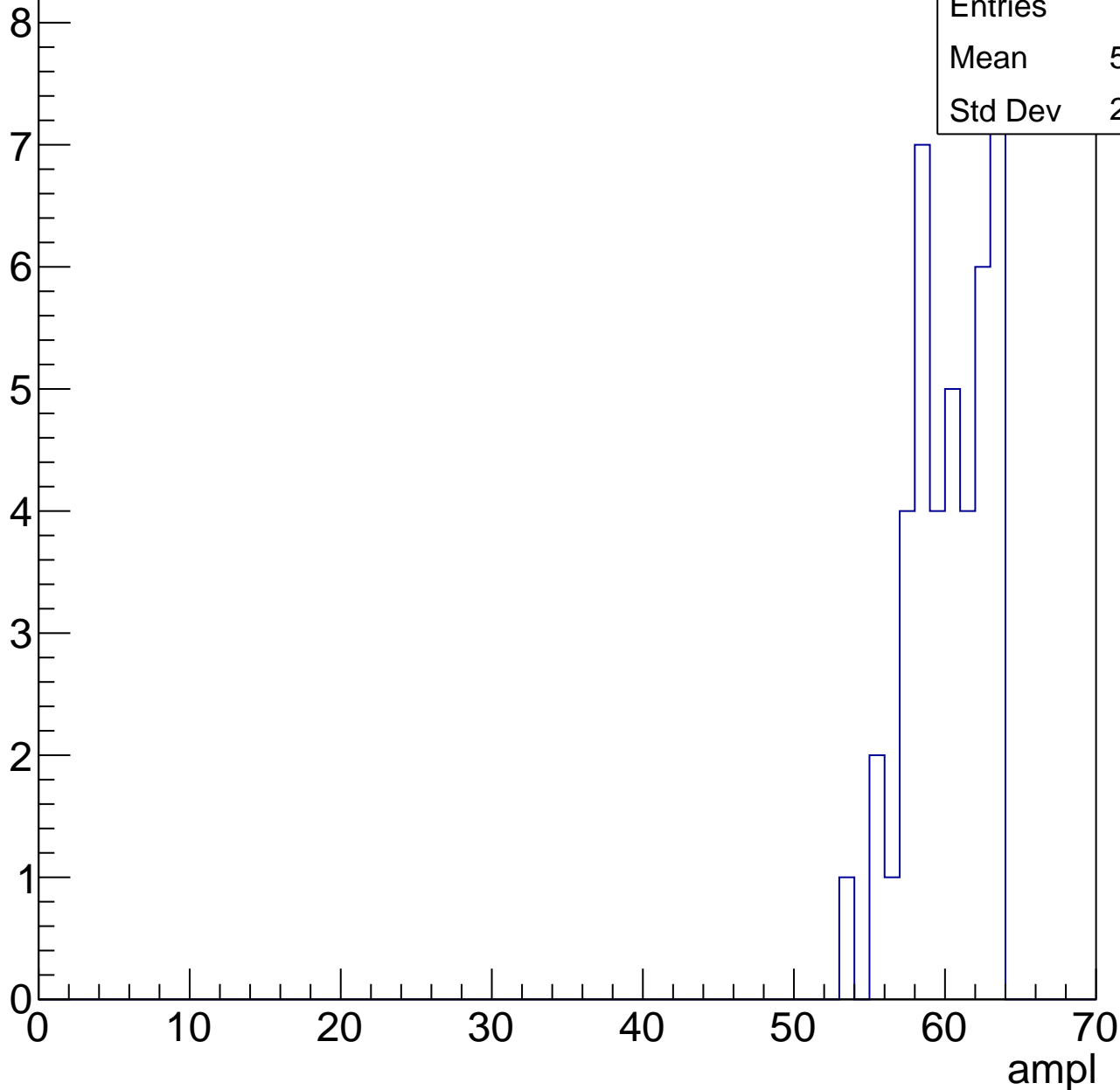


# B1L103S, U4-ch115, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 42    |
| Mean    | 59.74 |
| Std Dev | 2.583 |



# B1L103S, U4-ch115, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

3

2.5

2

1.5

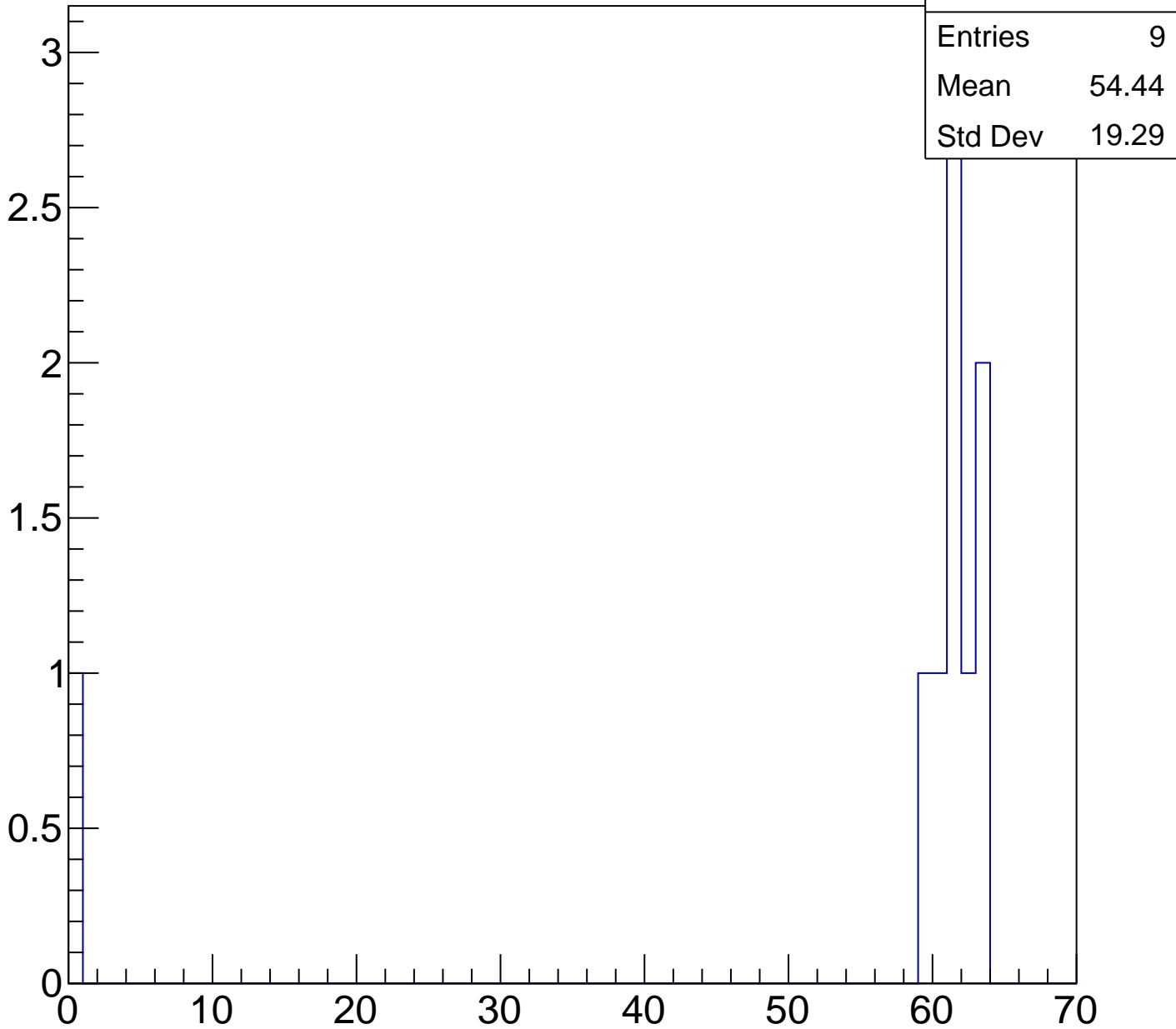
1

0.5

0

ampl

|         |       |
|---------|-------|
| Entries | 9     |
| Mean    | 54.44 |
| Std Dev | 19.29 |



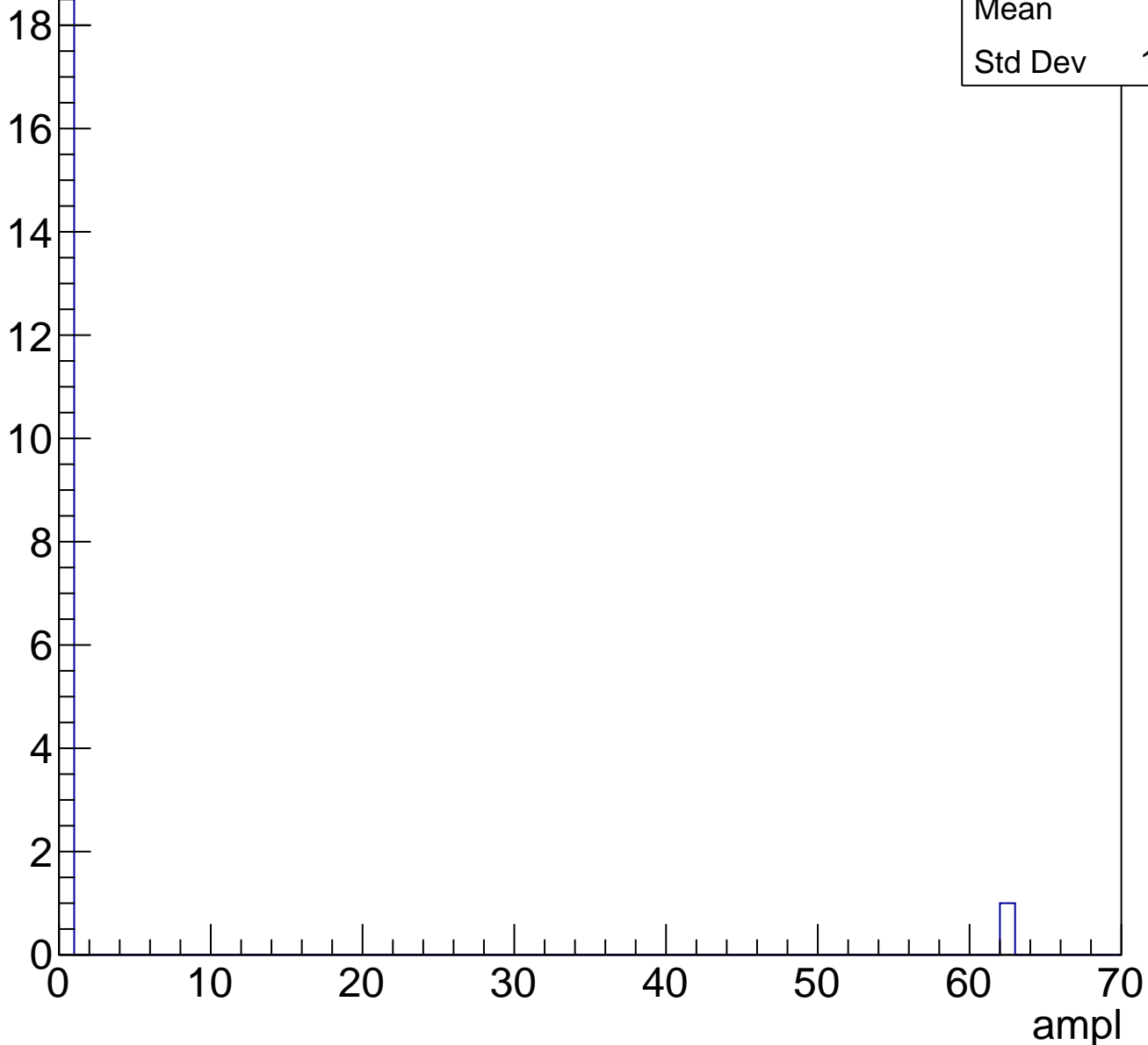


# B1L103S, U4-ch115, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 20    |
| Mean    | 3.1   |
| Std Dev | 13.51 |

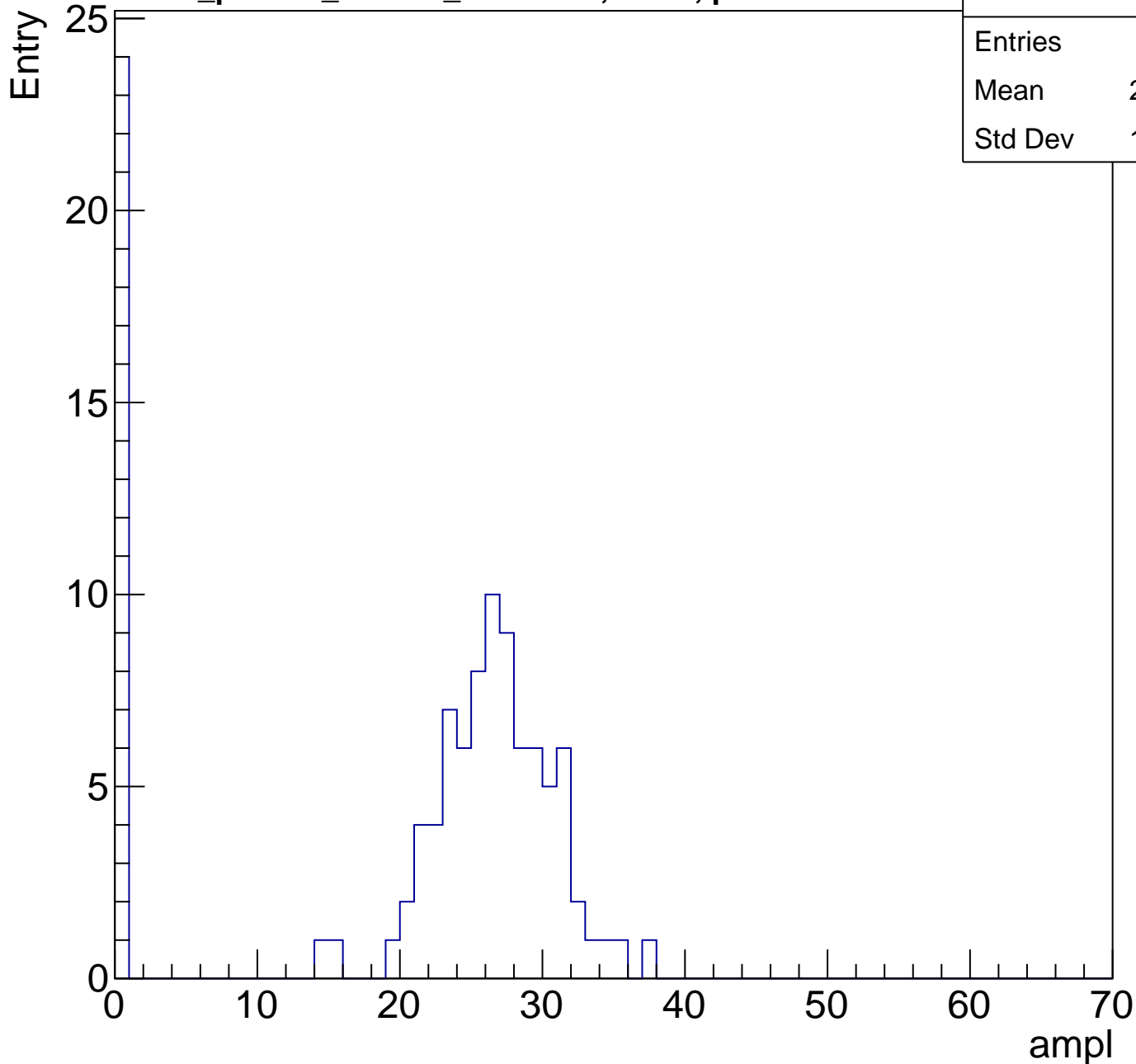
Entry



# B1L103S, U4-ch116, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 106   |
| Mean    | 20.27 |
| Std Dev | 11.53 |

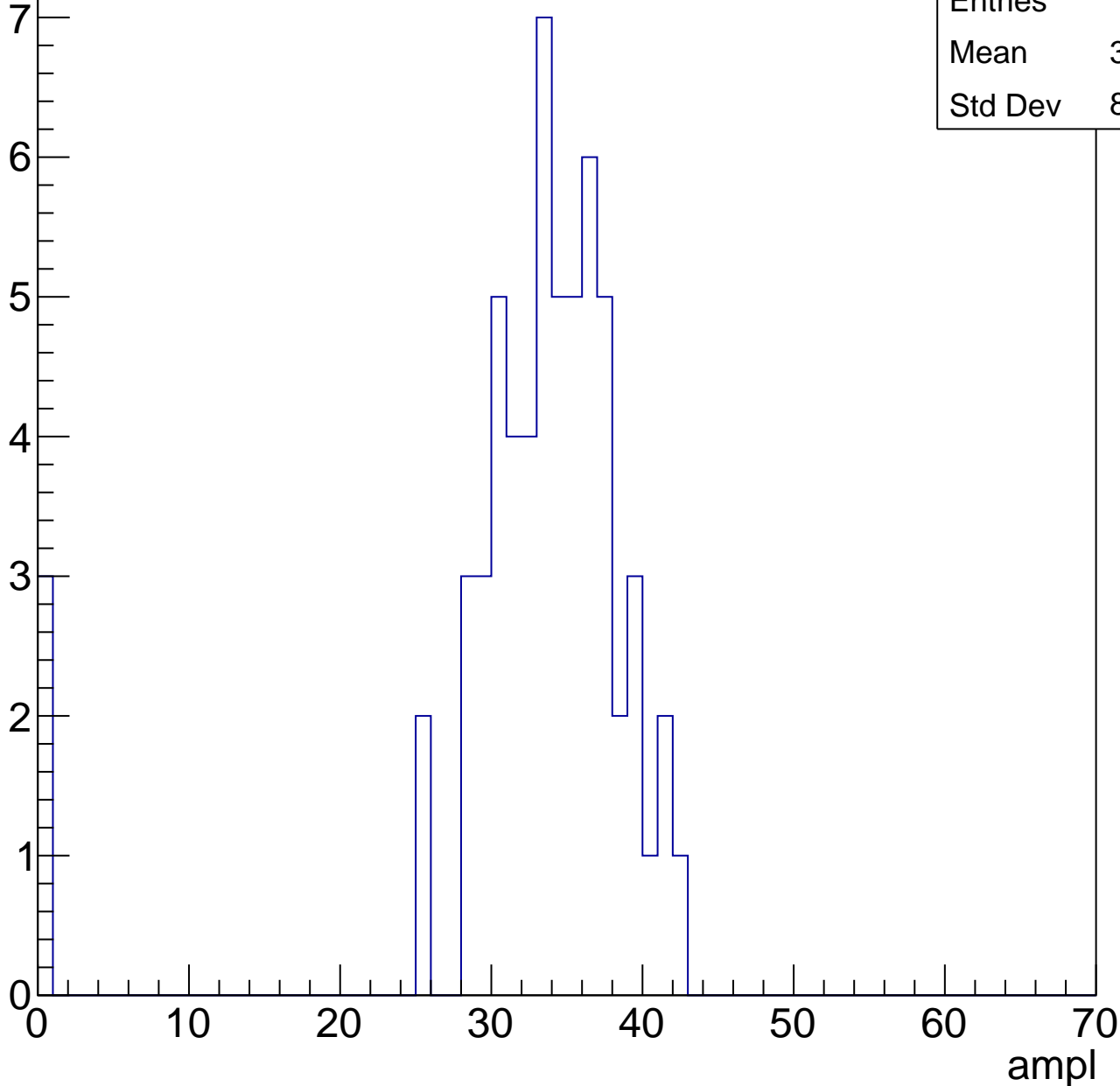


# B1L103S, U4-ch116, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 61    |
| Mean    | 32.08 |
| Std Dev | 8.205 |

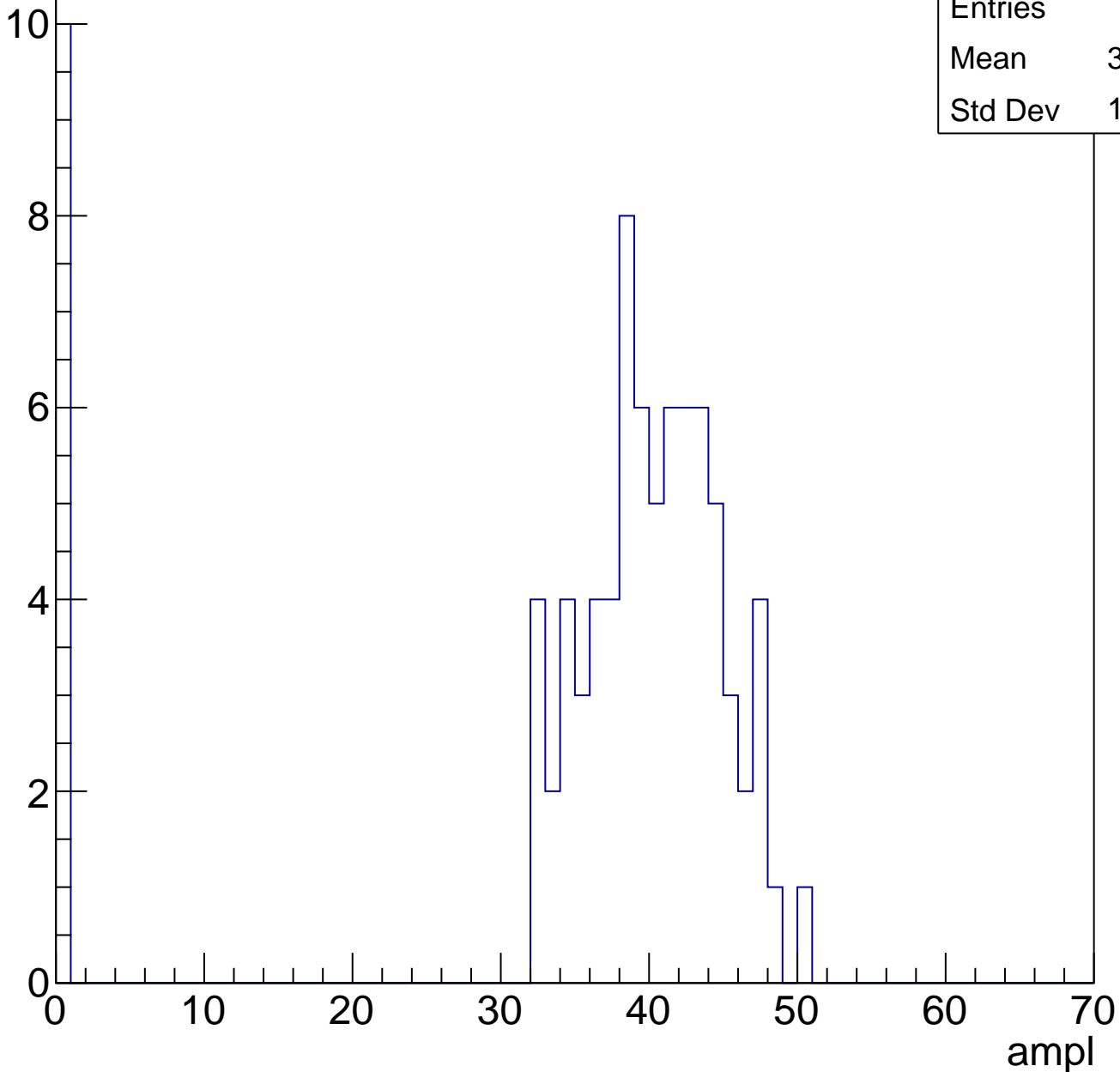


# B1L103S, U4-ch116, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 84    |
| Mean    | 35.17 |
| Std Dev | 13.55 |

Entry

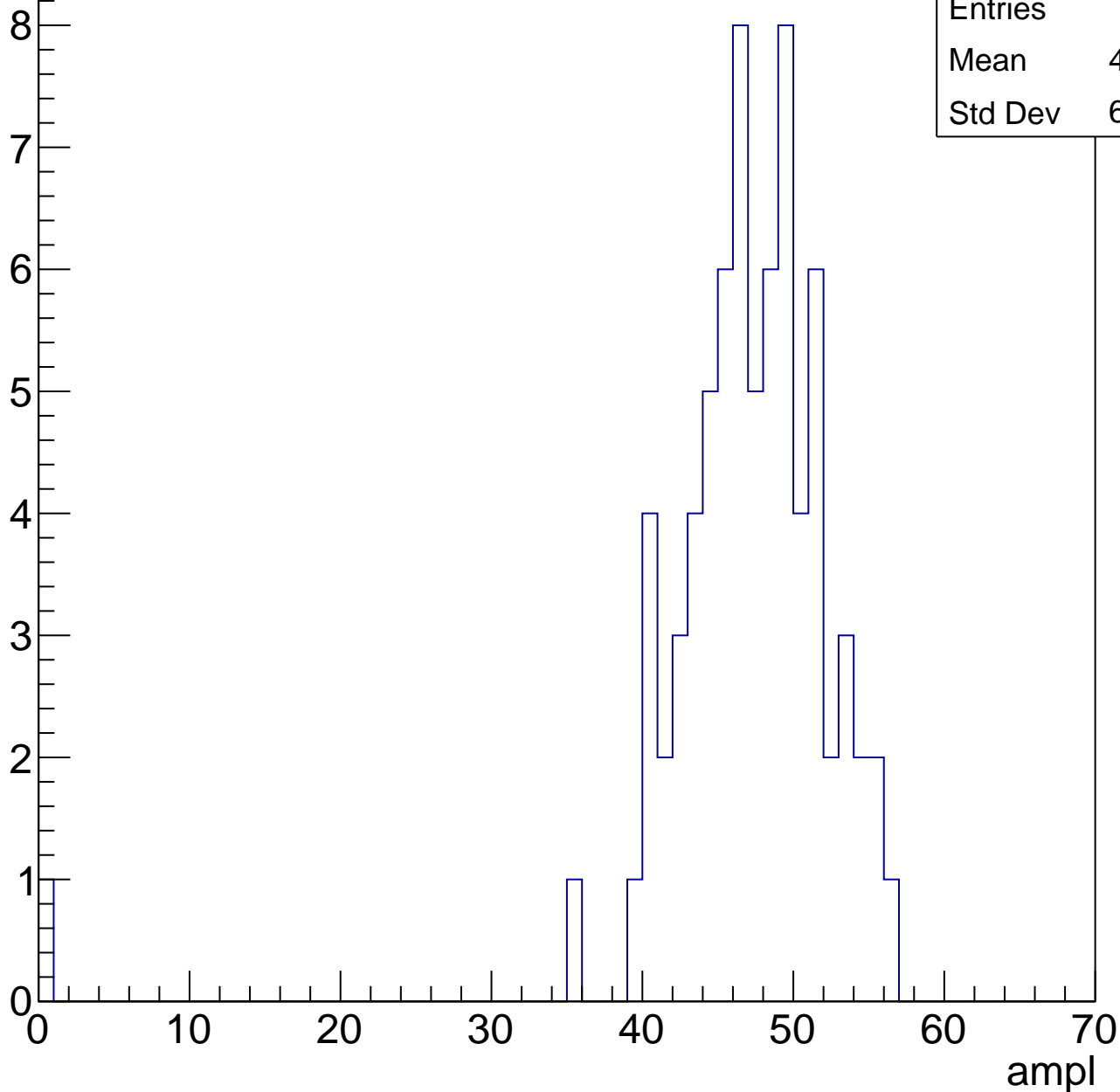


# B1L103S, U4-ch116, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 74    |
| Mean    | 46.35 |
| Std Dev | 6.882 |

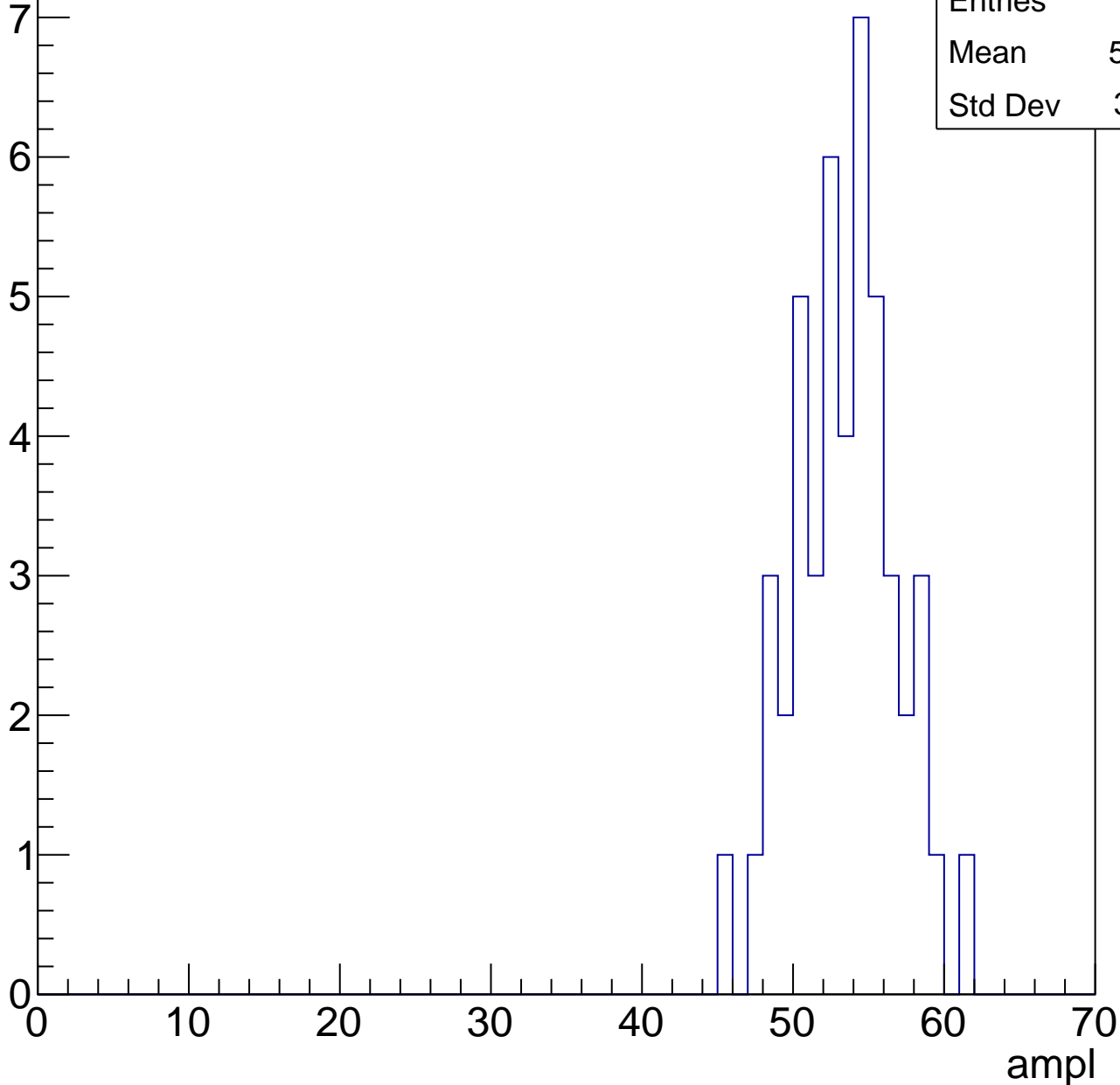


# B1L103S, U4-ch116, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 47    |
| Mean    | 52.98 |
| Std Dev | 3.361 |

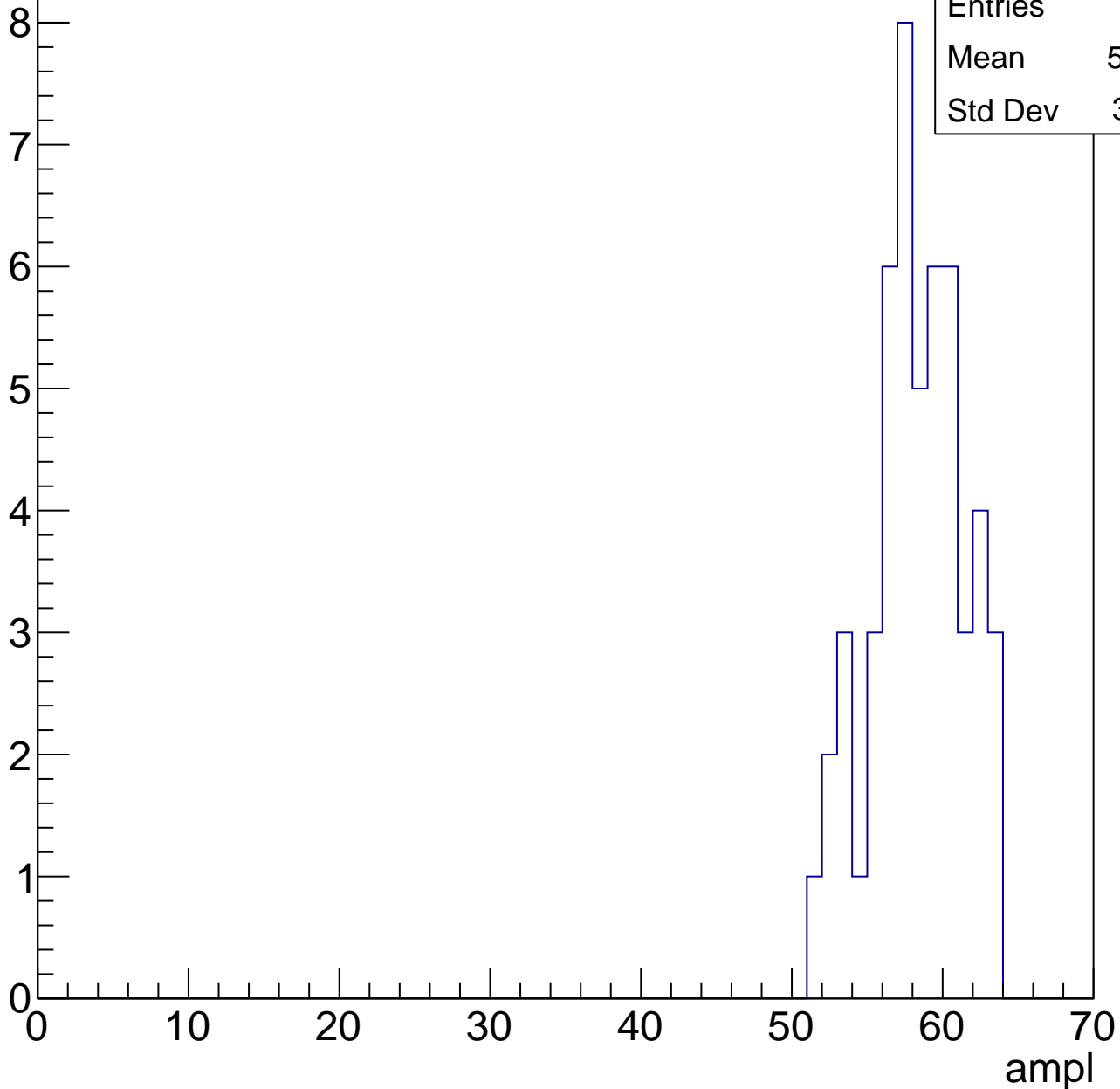


# B1L103S, U4-ch116, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 51    |
| Mean    | 57.82 |
| Std Dev | 3.021 |

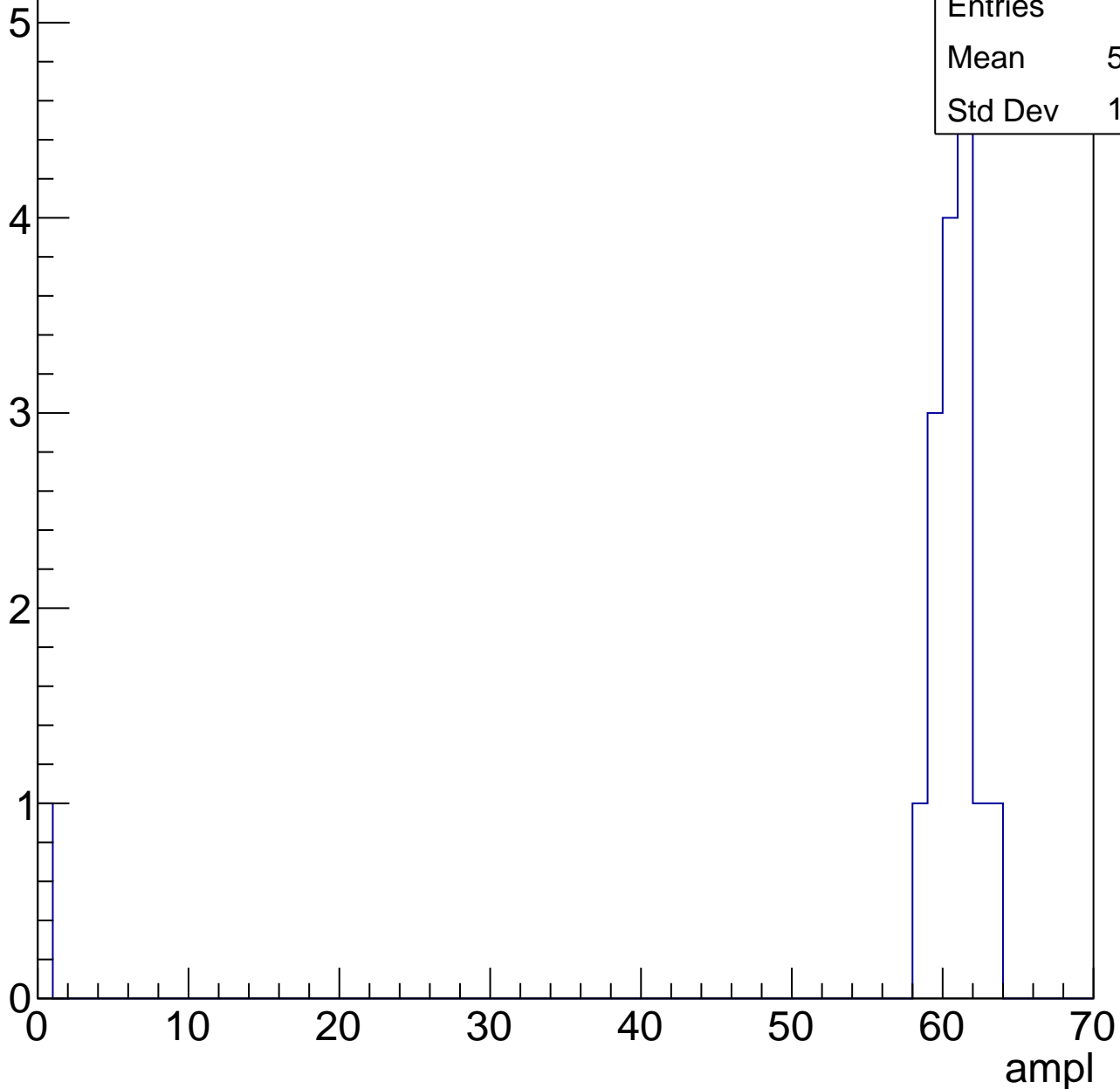


# B1L103S, U4-ch116, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 16    |
| Mean    | 56.56 |
| Std Dev | 14.65 |



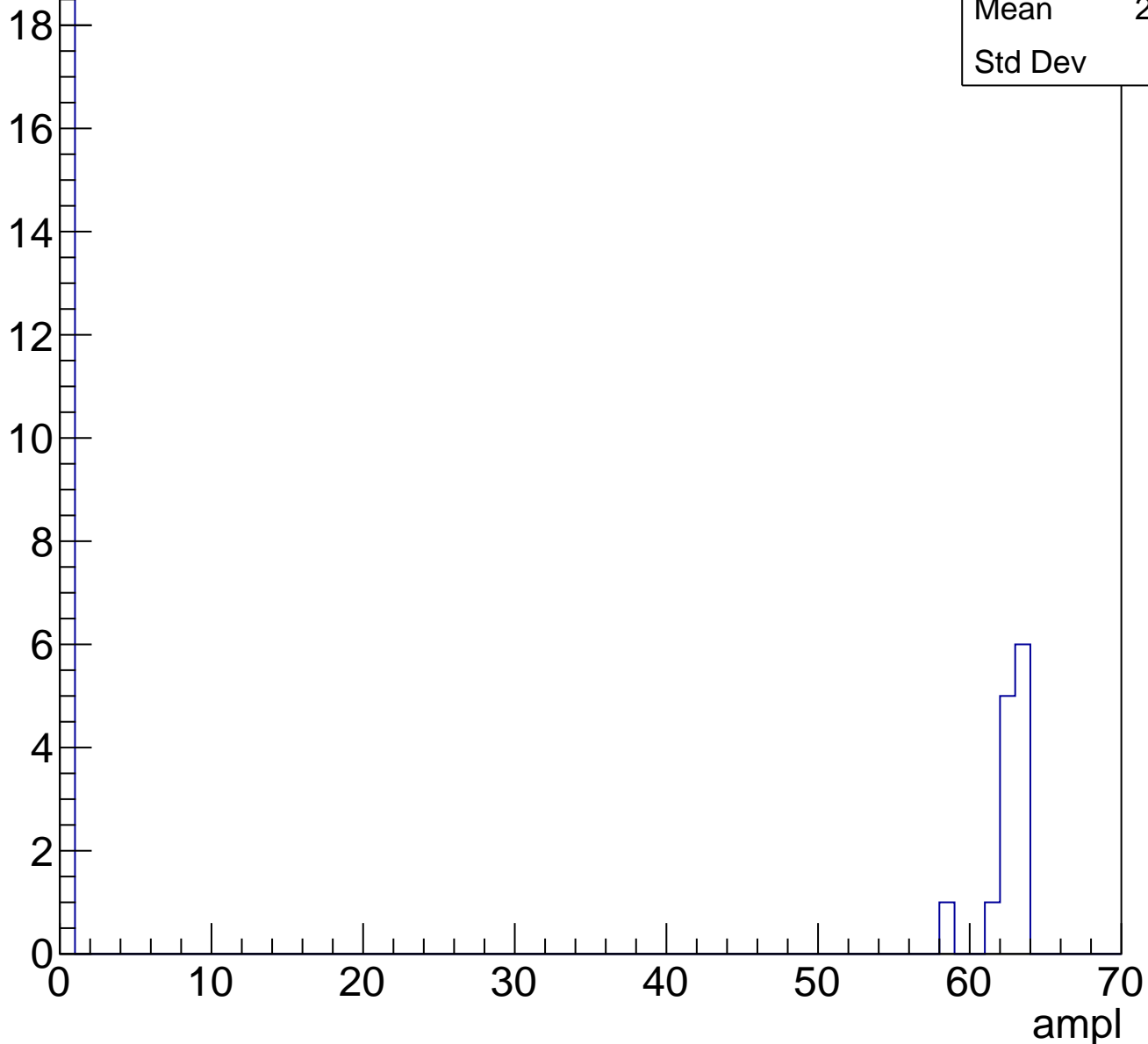


# B1L103S, U4-ch116, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 32    |
| Mean    | 25.22 |
| Std Dev | 30.5  |

Entry

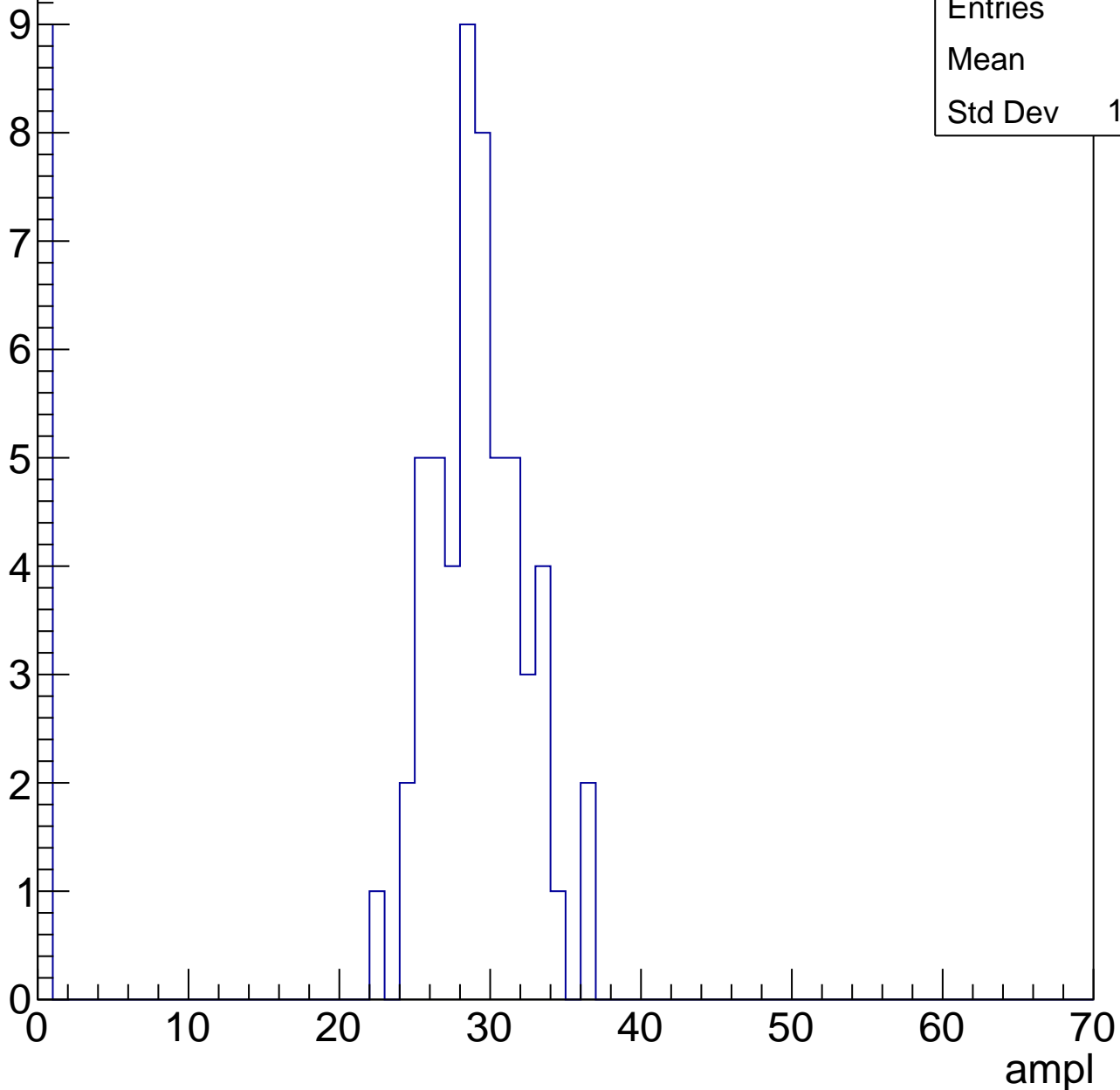


# B1L103S, U4-ch117, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 63    |
| Mean    | 24.7  |
| Std Dev | 10.46 |

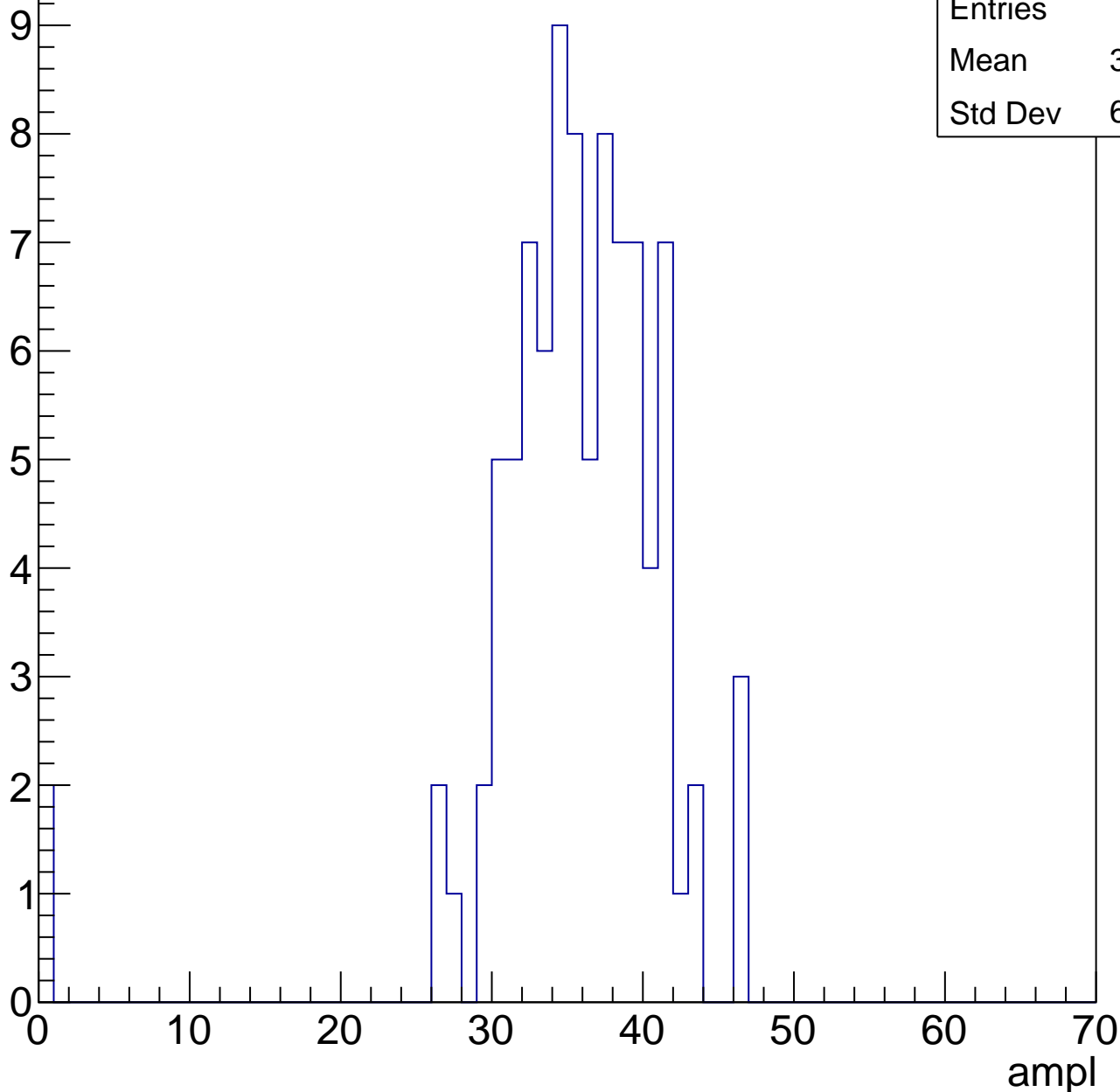


# B1L103S, U4-ch117, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 91    |
| Mean    | 34.92 |
| Std Dev | 6.755 |

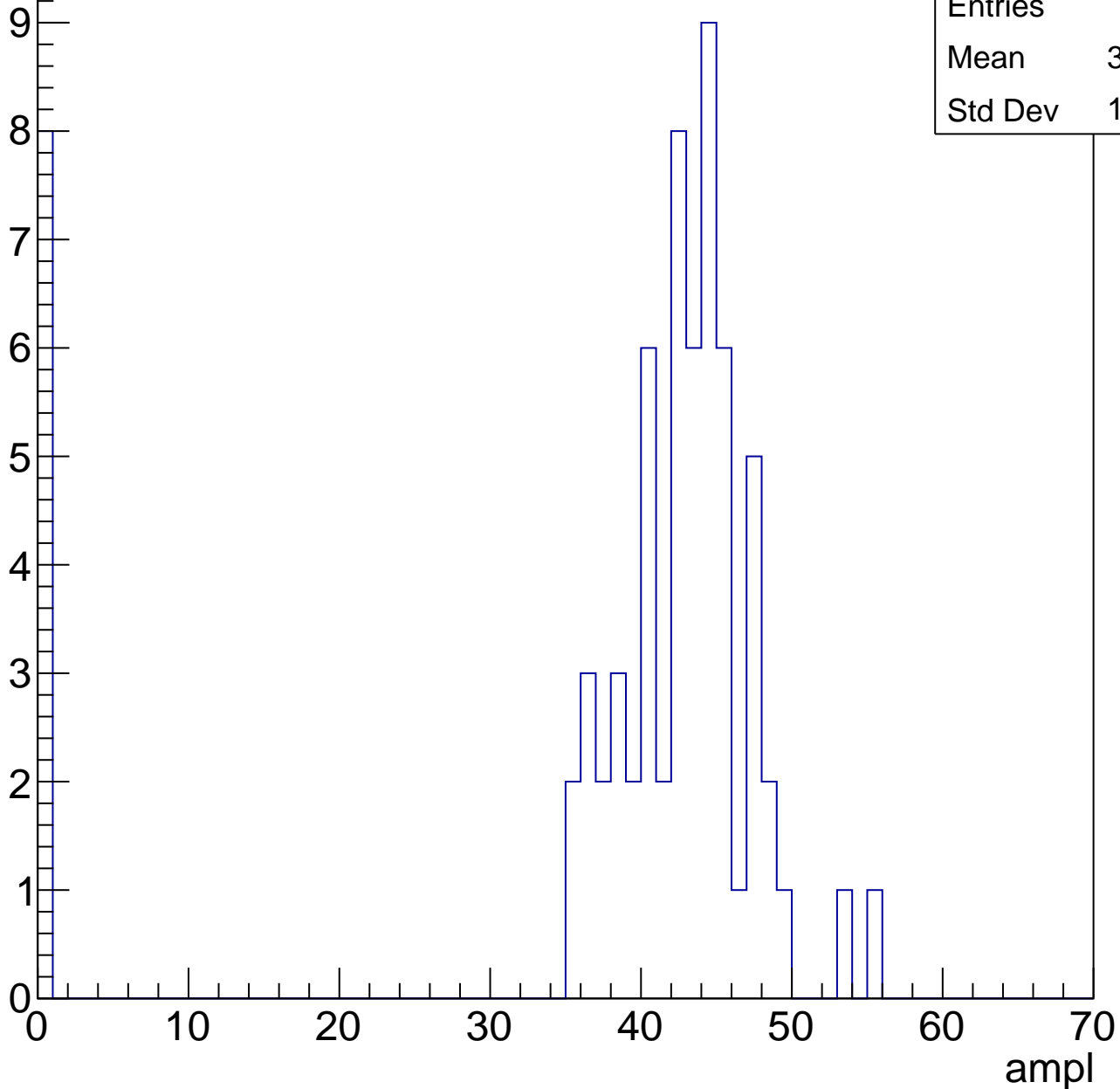


# B1L103S, U4-ch117, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 68    |
| Mean    | 37.65 |
| Std Dev | 14.26 |



# B1L103S, U4-ch117, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

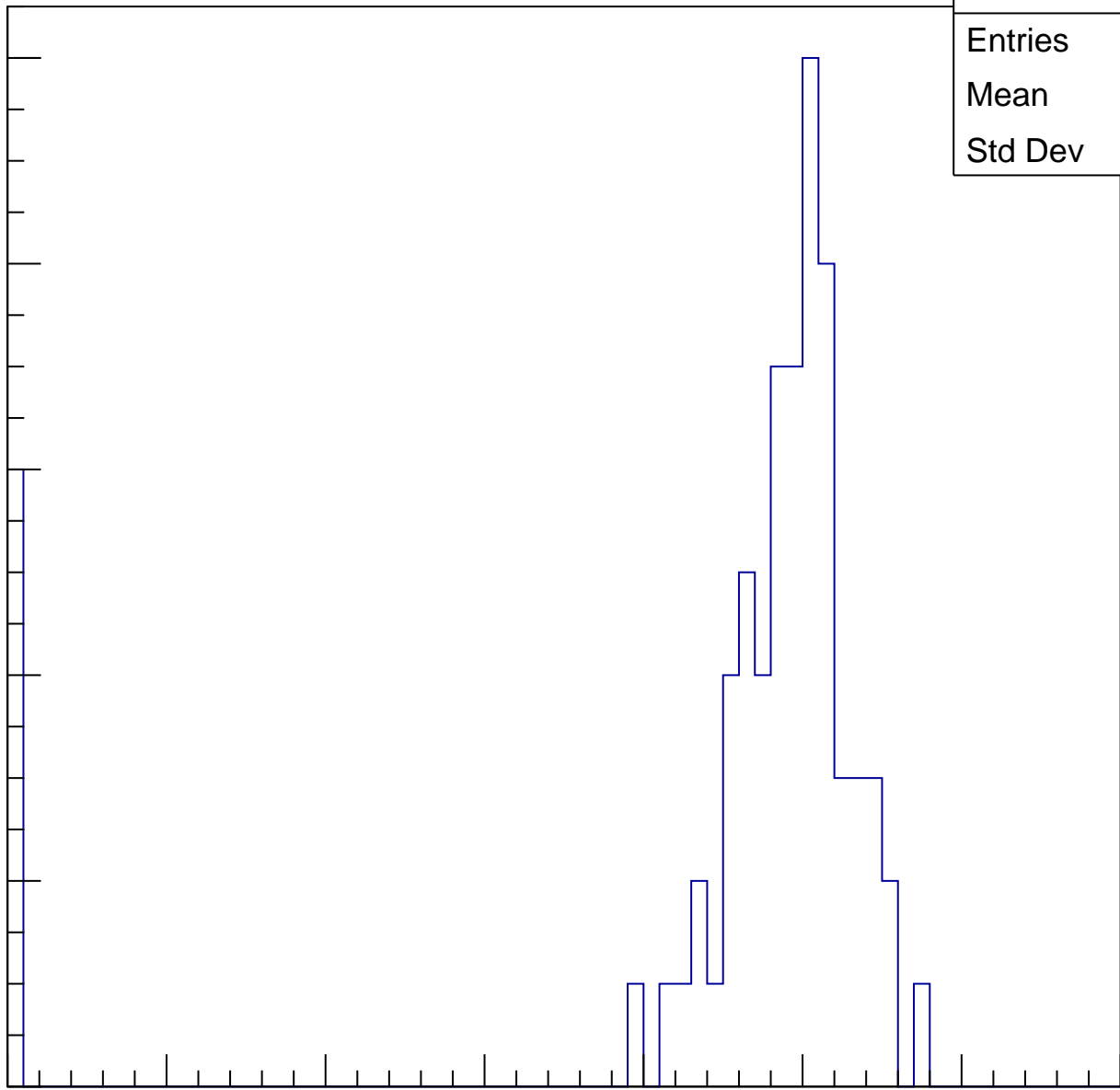
|         |       |
|---------|-------|
| Entries | 69    |
| Mean    | 44.65 |
| Std Dev | 14.18 |

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

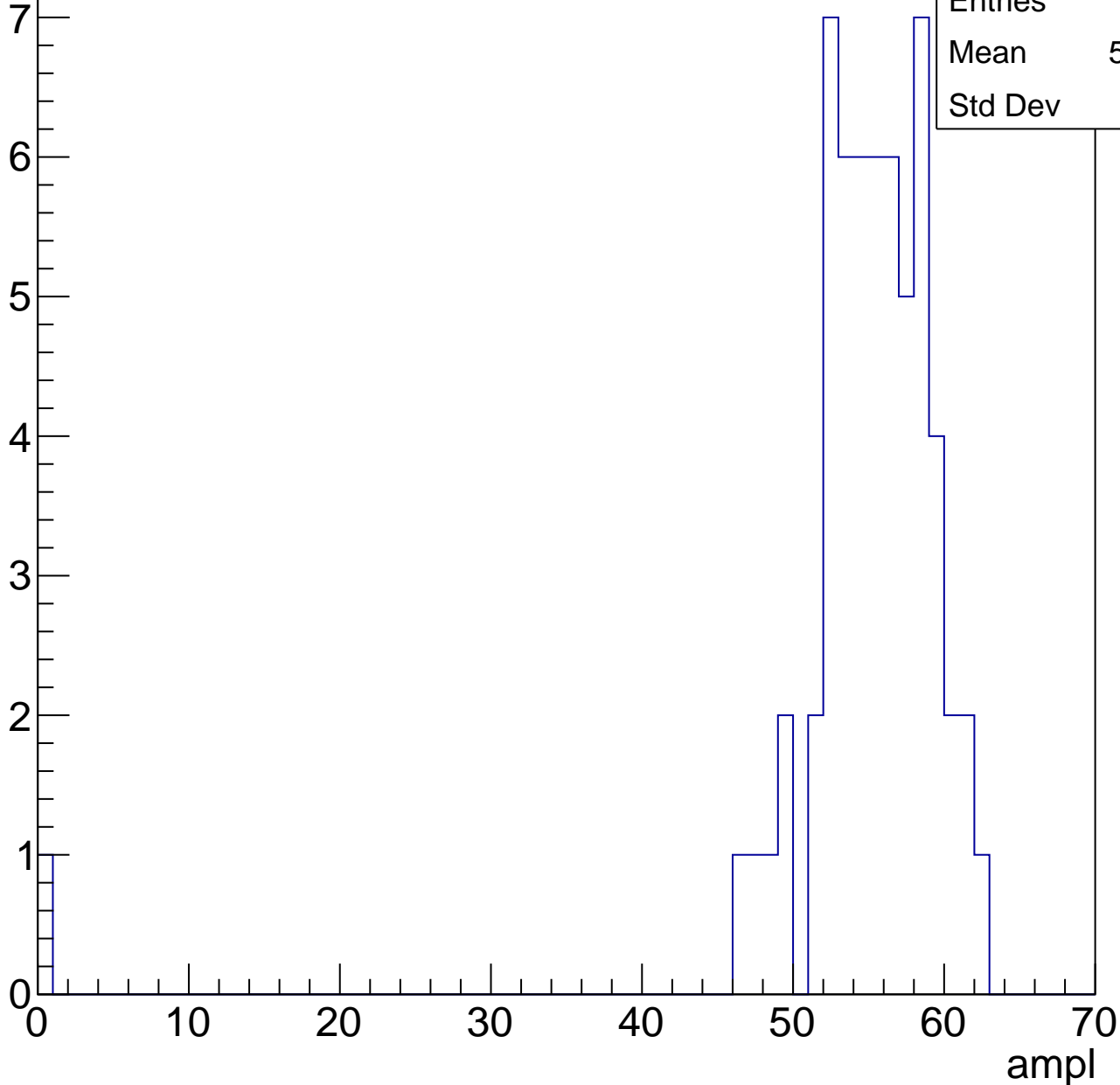


# B1L103S, U4-ch117, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 60    |
| Mean    | 54.07 |
| Std Dev | 7.84  |

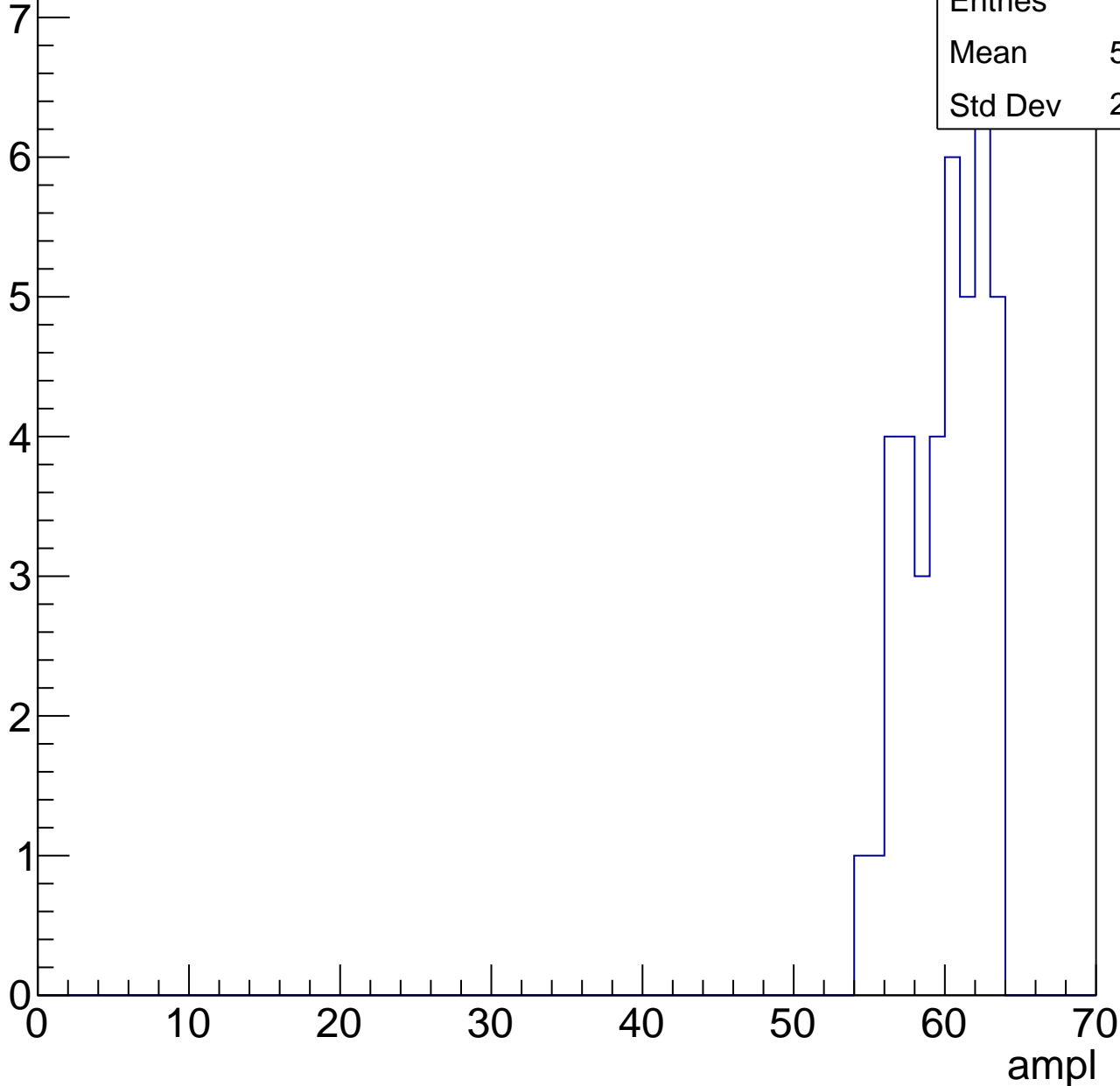


# B1L103S, U4-ch117, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

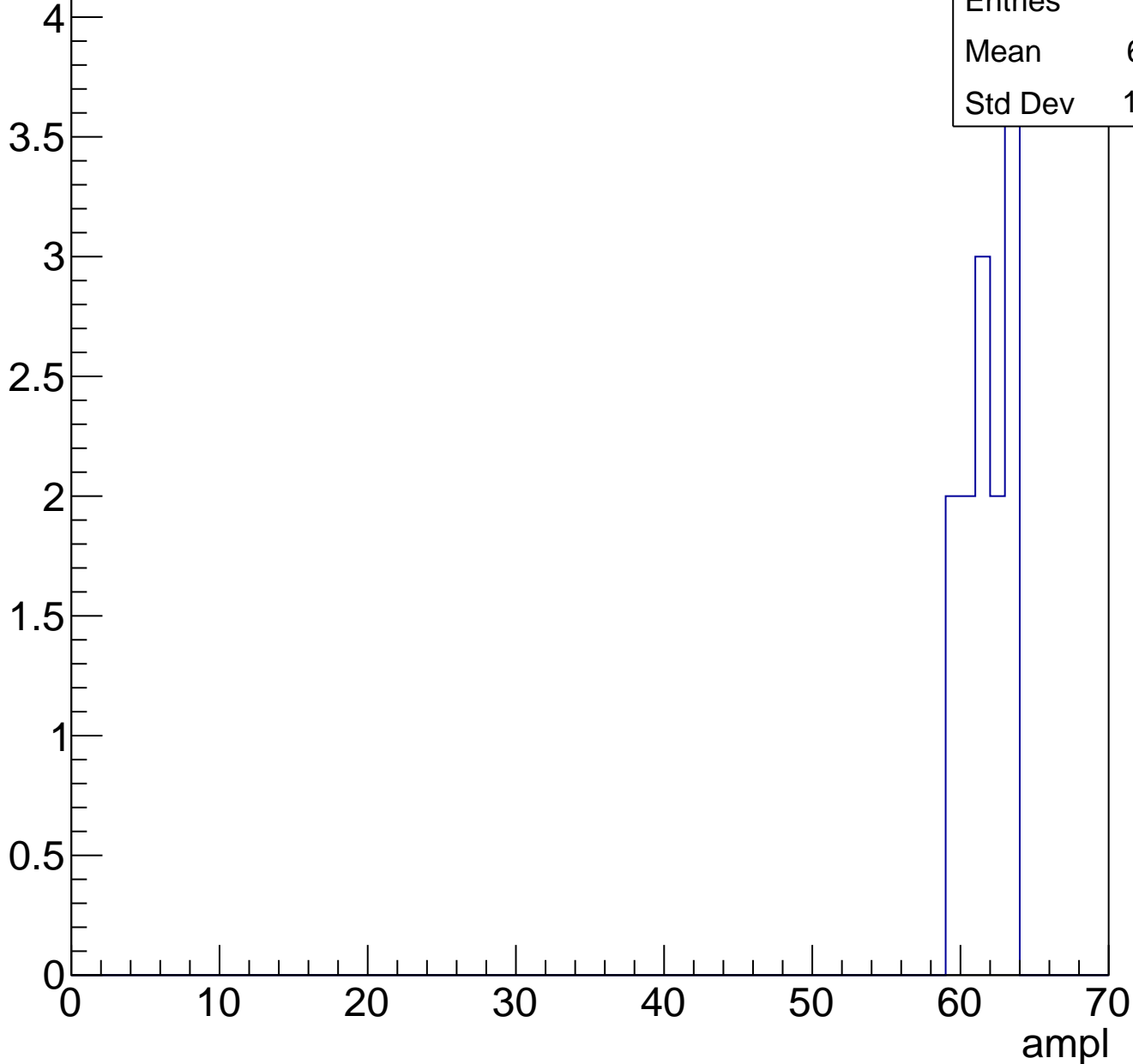
|         |       |
|---------|-------|
| Entries | 40    |
| Mean    | 59.62 |
| Std Dev | 2.497 |



# B1L103S, U4-ch117, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



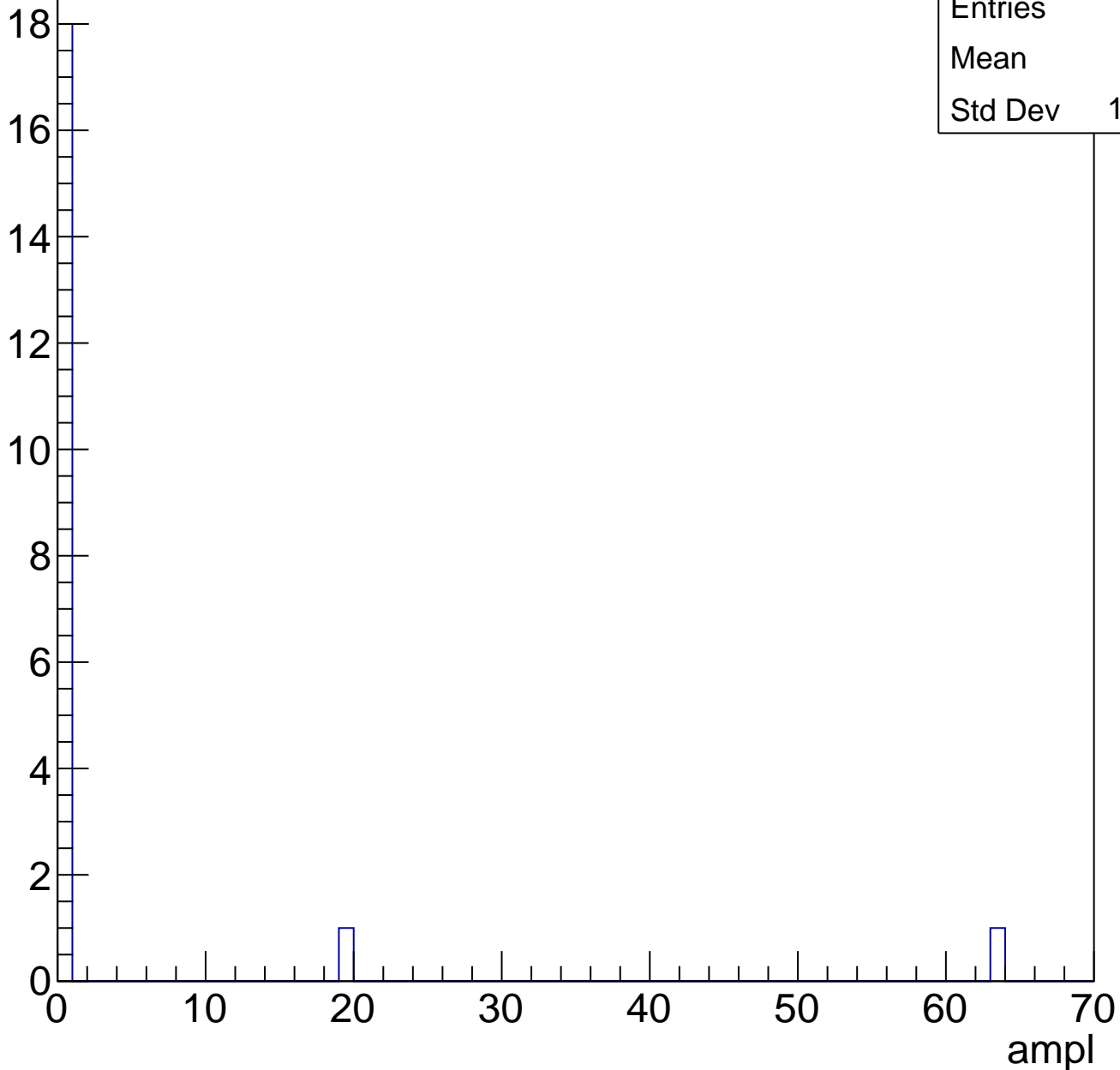


# B1L103S, U4-ch117, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 20    |
| Mean    | 4.1   |
| Std Dev | 14.13 |

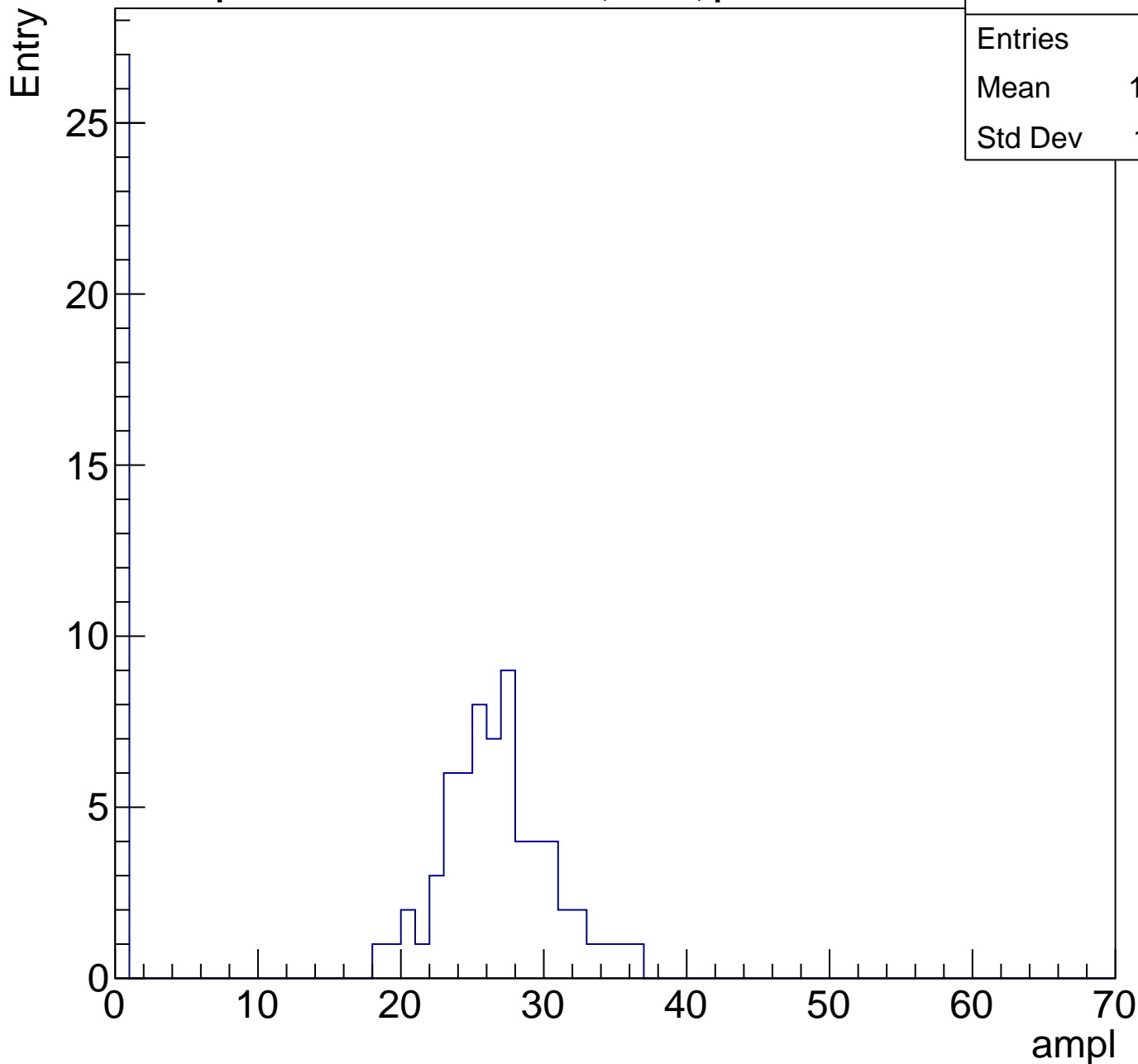
Entry



# B1L103S, U4-ch118, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 91    |
| Mean    | 18.49 |
| Std Dev | 12.41 |

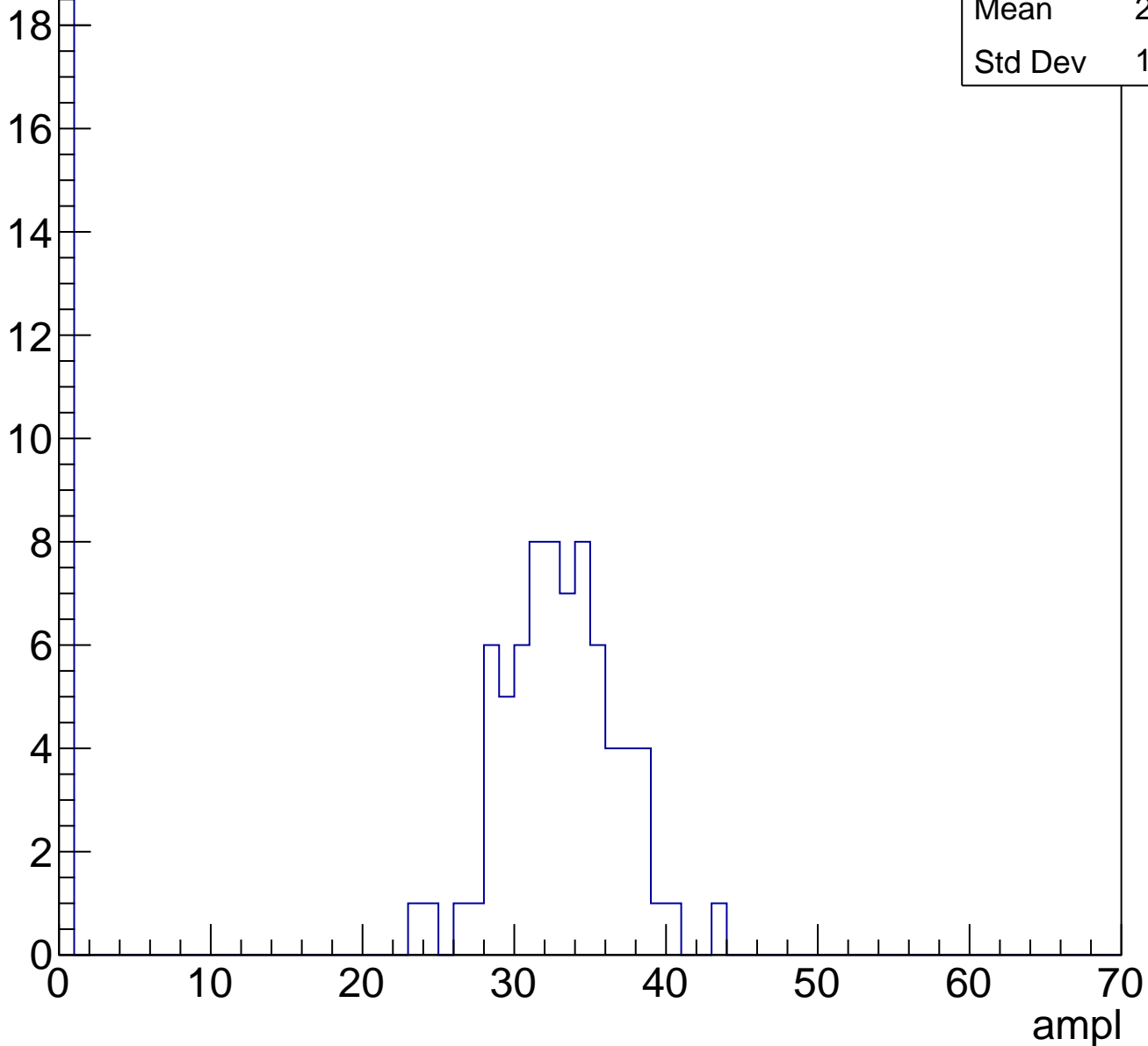


# B1L103S, U4-ch118, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 92    |
| Mean    | 25.83 |
| Std Dev | 13.58 |

Entry

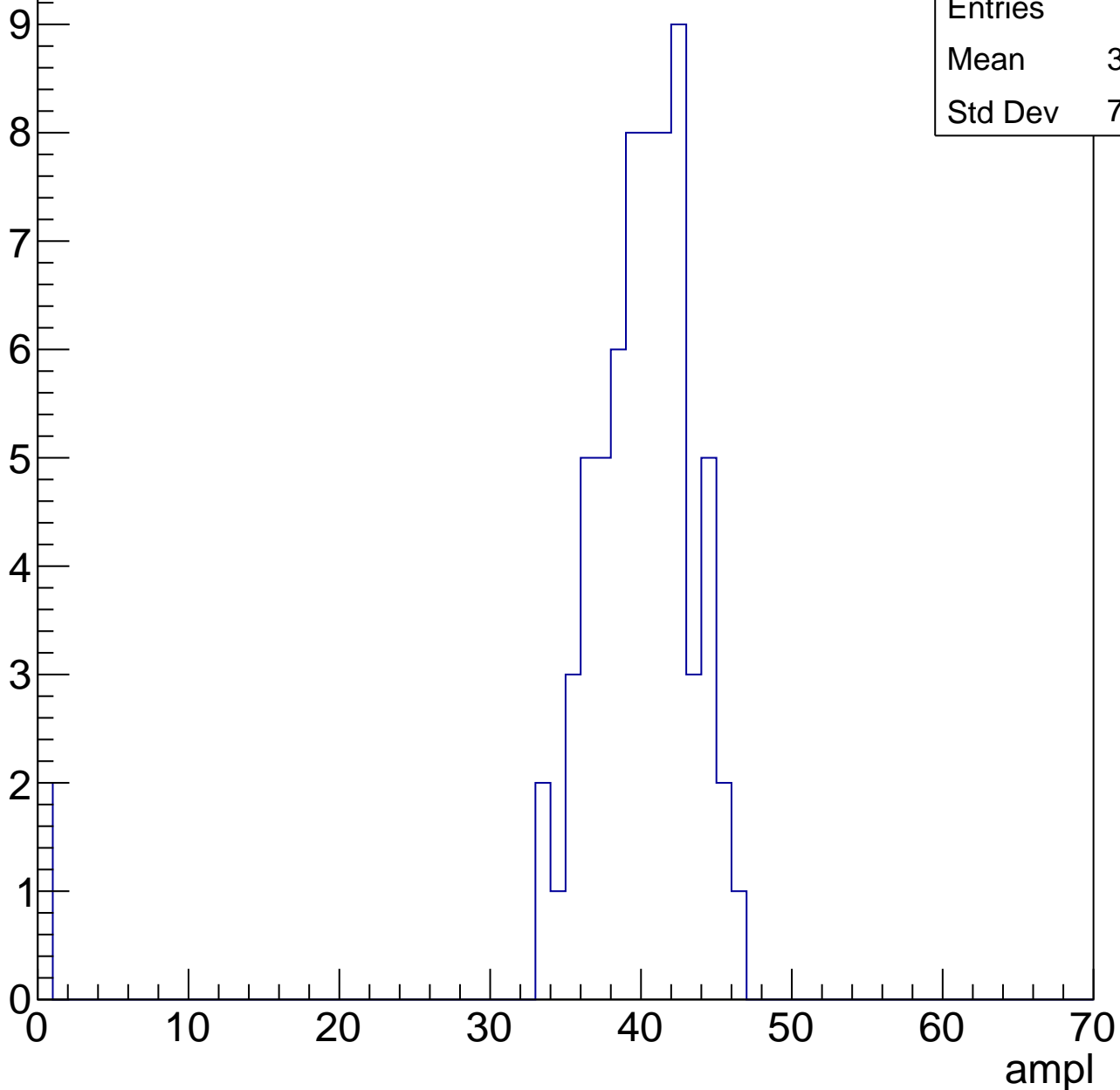


# B1L103S, U4-ch118, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 68    |
| Mean    | 38.54 |
| Std Dev | 7.335 |

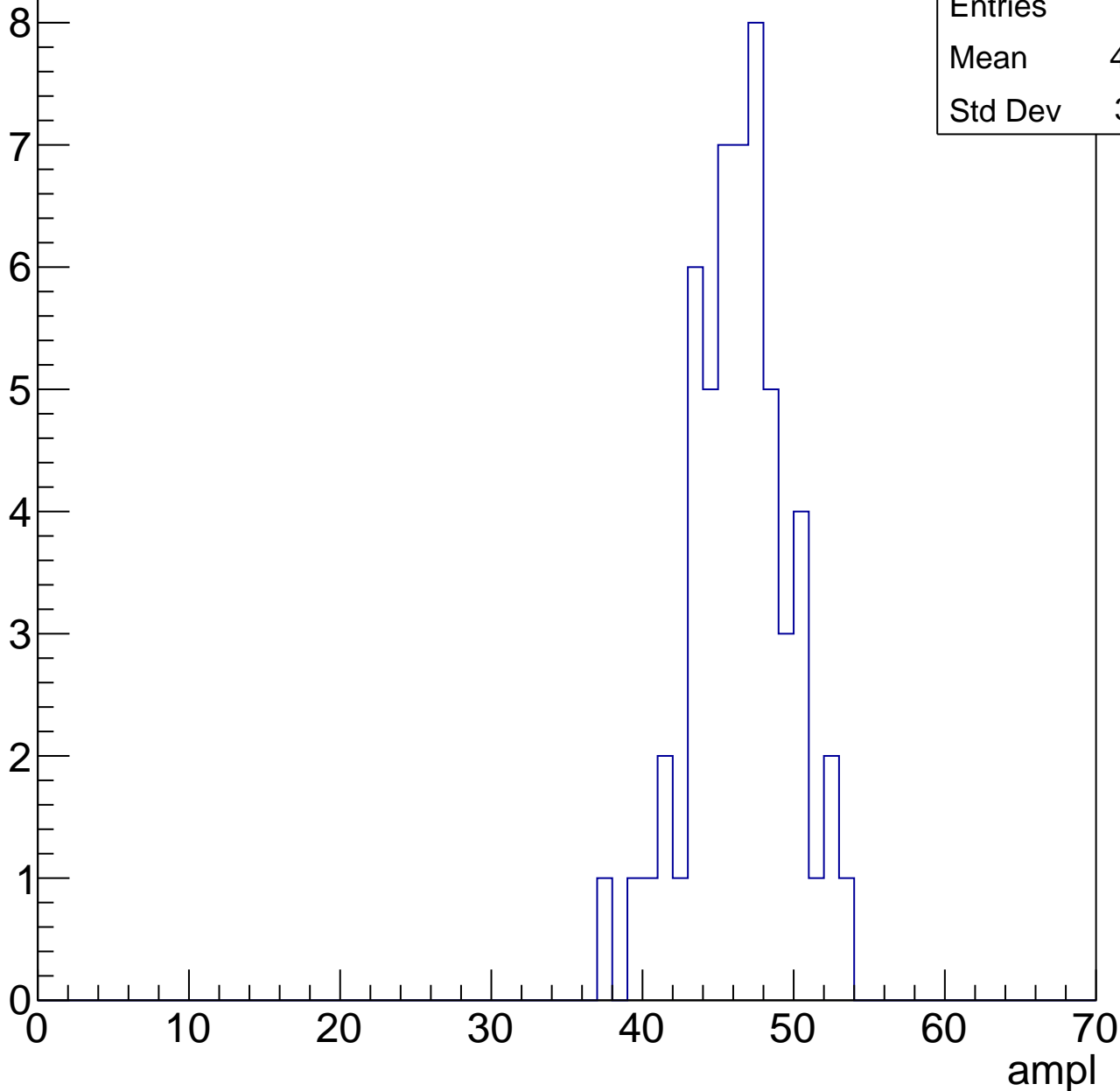


# B1L103S, U4-ch118, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 55    |
| Mean    | 45.93 |
| Std Dev | 3.241 |

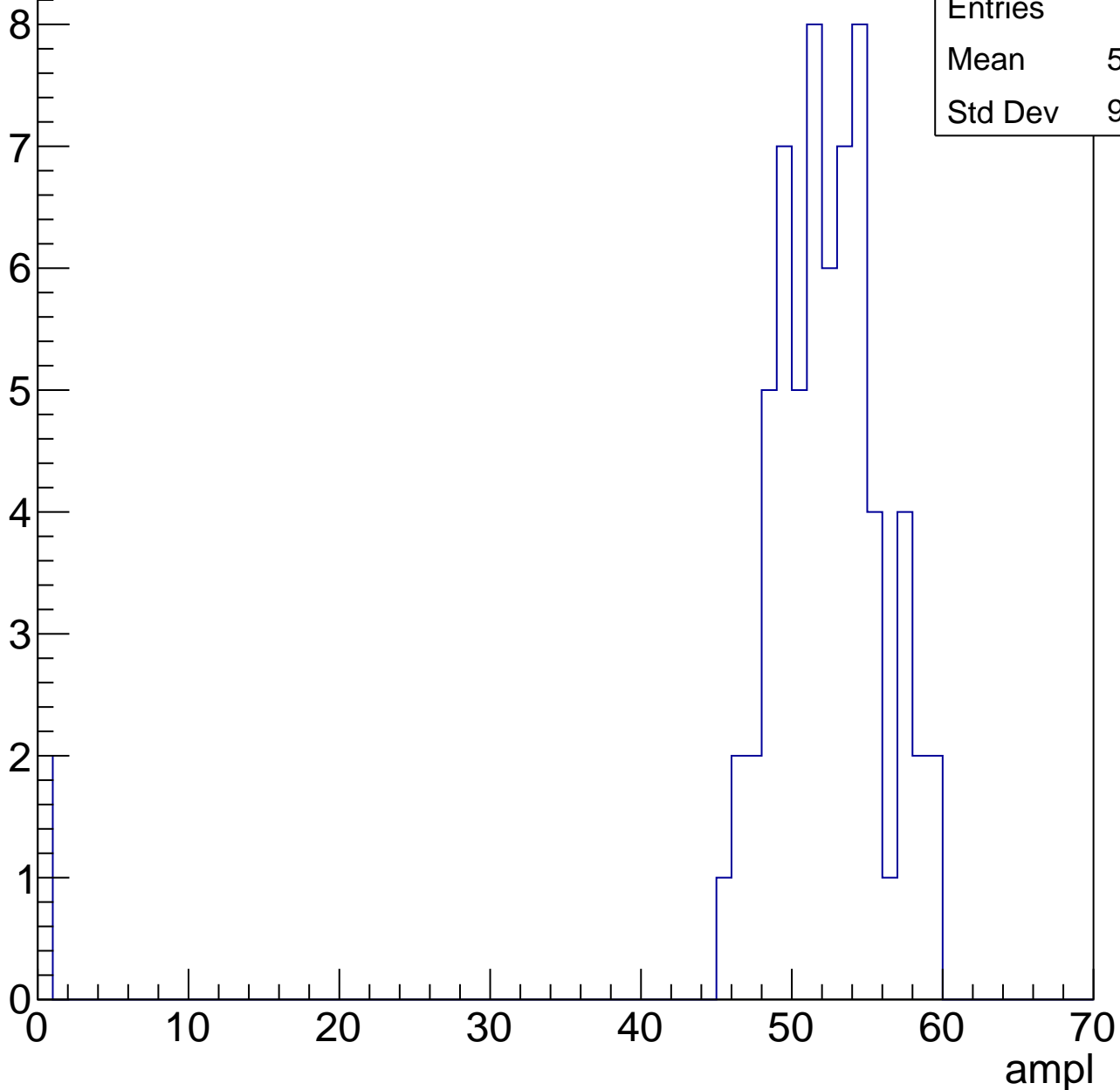


# B1L103S, U4-ch118, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 66    |
| Mean    | 50.38 |
| Std Dev | 9.485 |

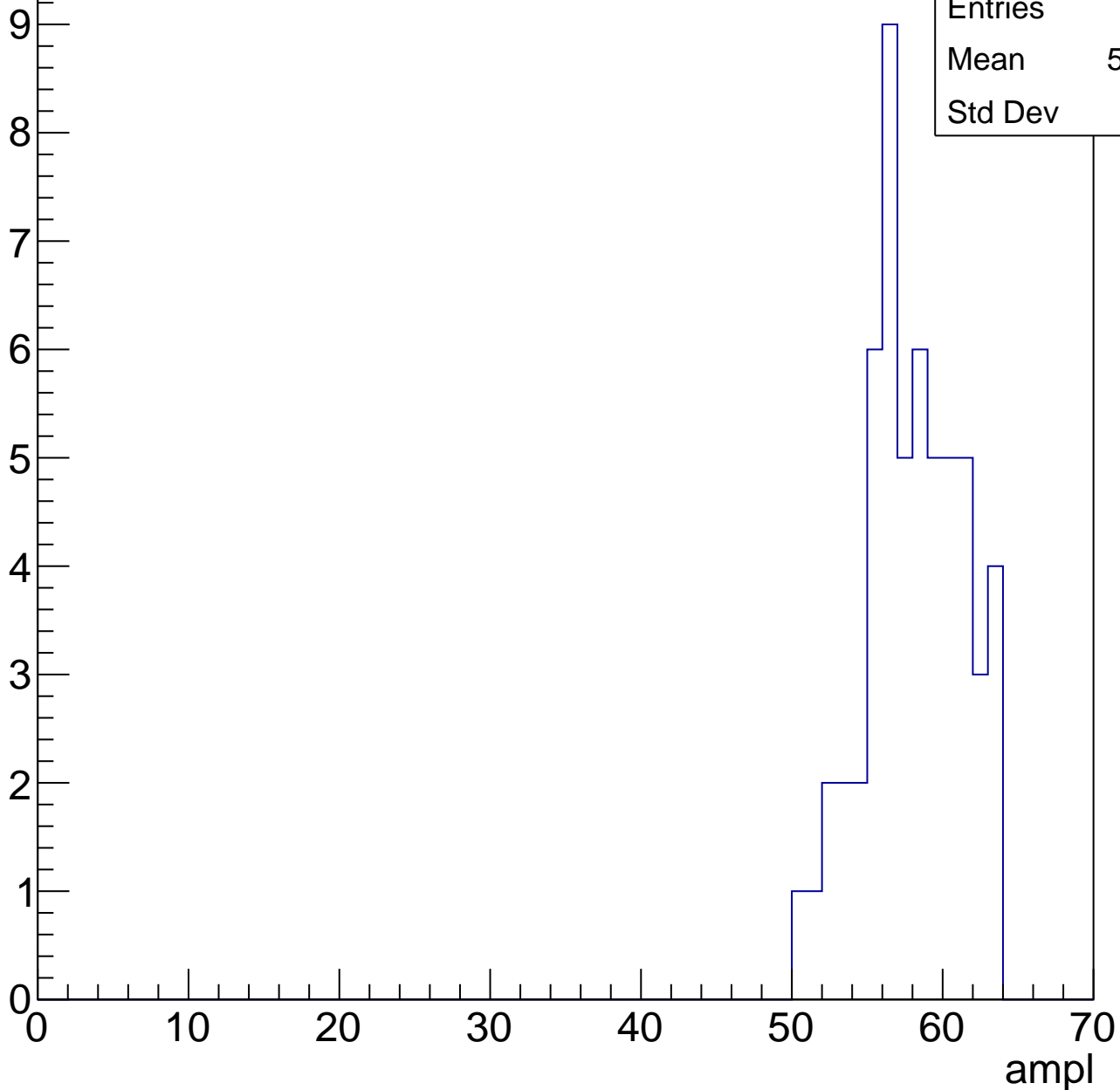


# B1L103S, U4-ch118, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 56    |
| Mean    | 57.57 |
| Std Dev | 3.19  |

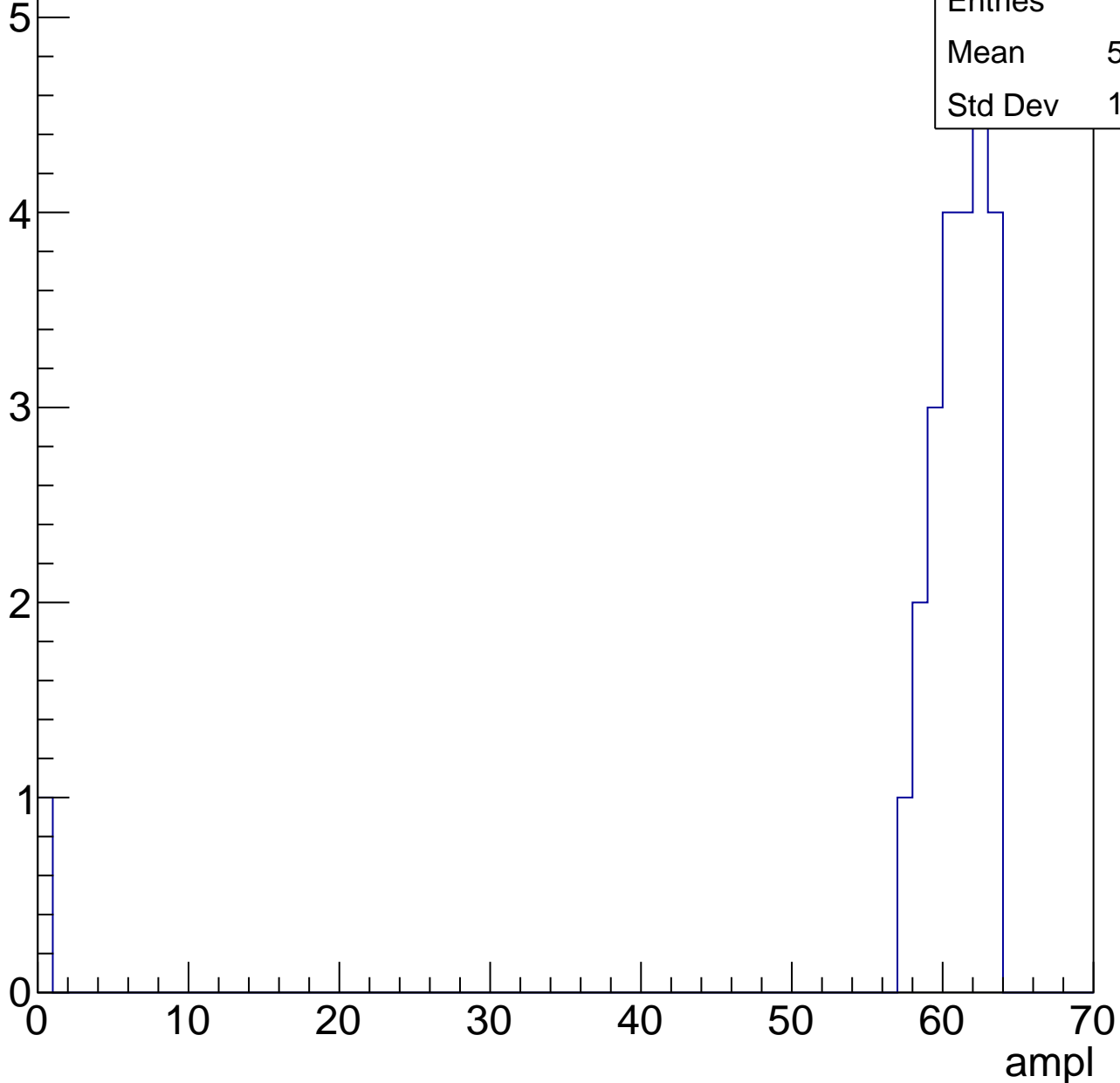


# B1L103S, U4-ch118, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 24    |
| Mean    | 58.17 |
| Std Dev | 12.25 |



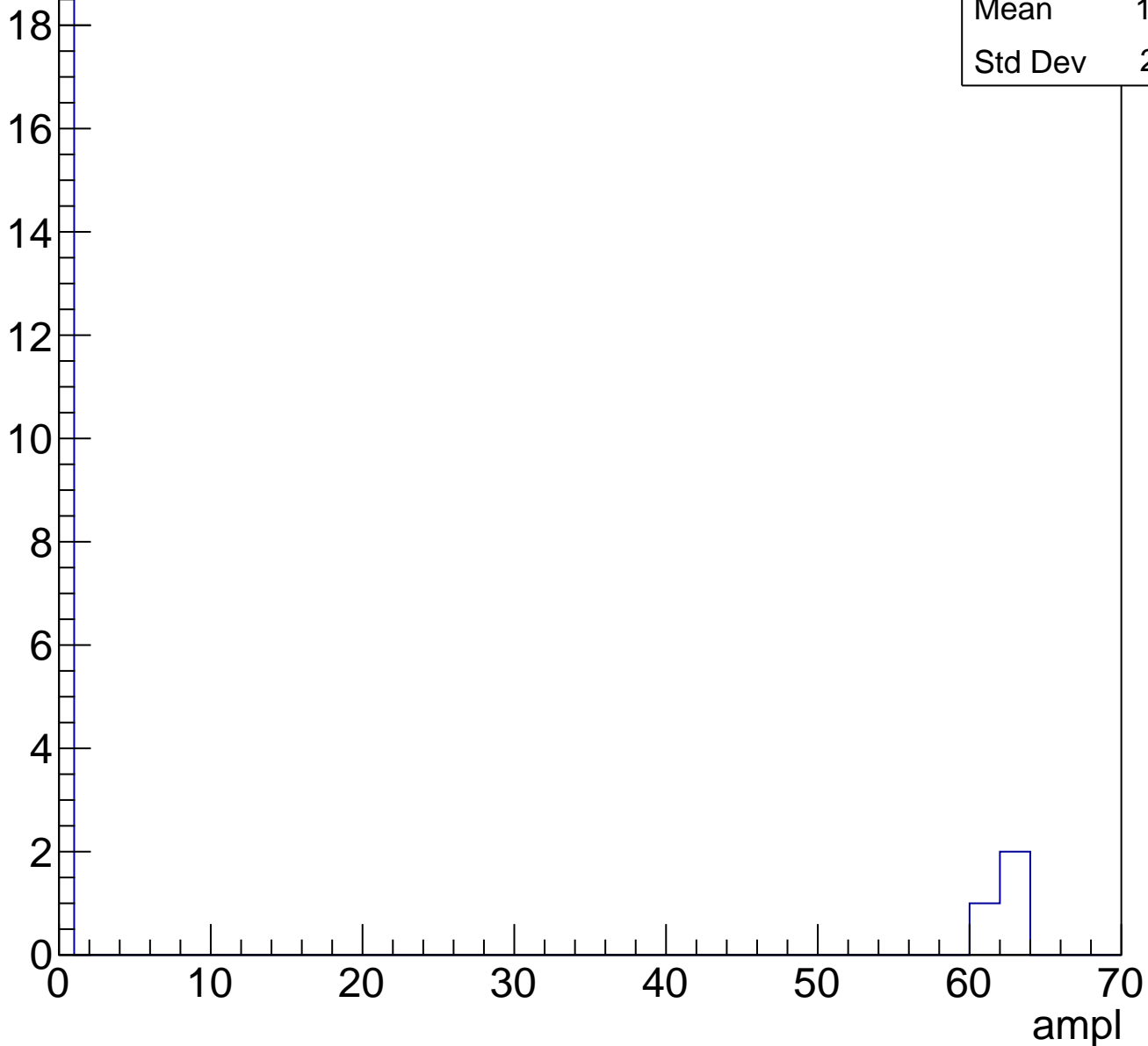


# B1L103S, U4-ch118, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 25    |
| Mean    | 14.84 |
| Std Dev | 26.41 |

Entry

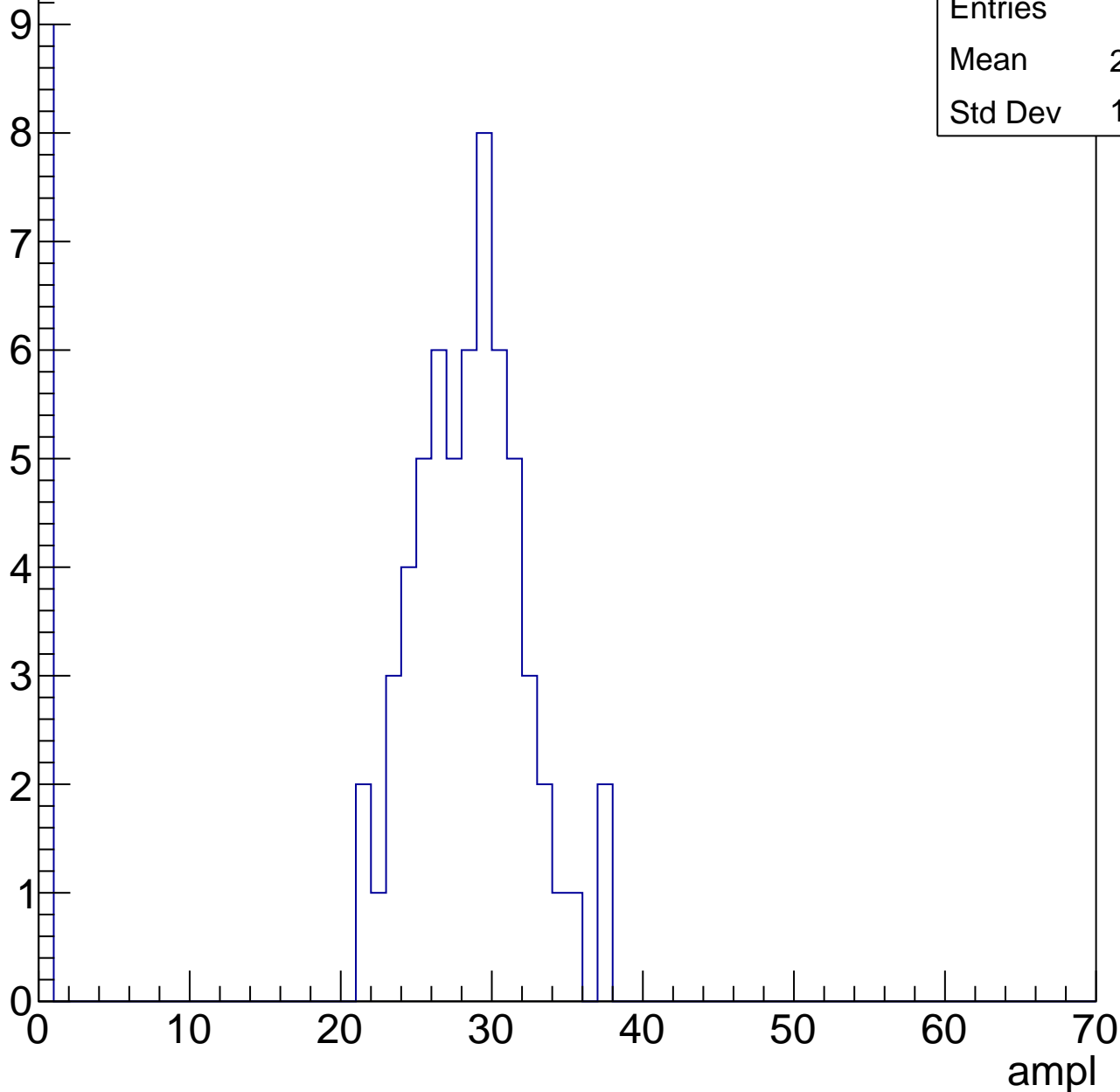


# B1L103S, U4-ch119, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 69    |
| Mean    | 24.42 |
| Std Dev | 10.03 |

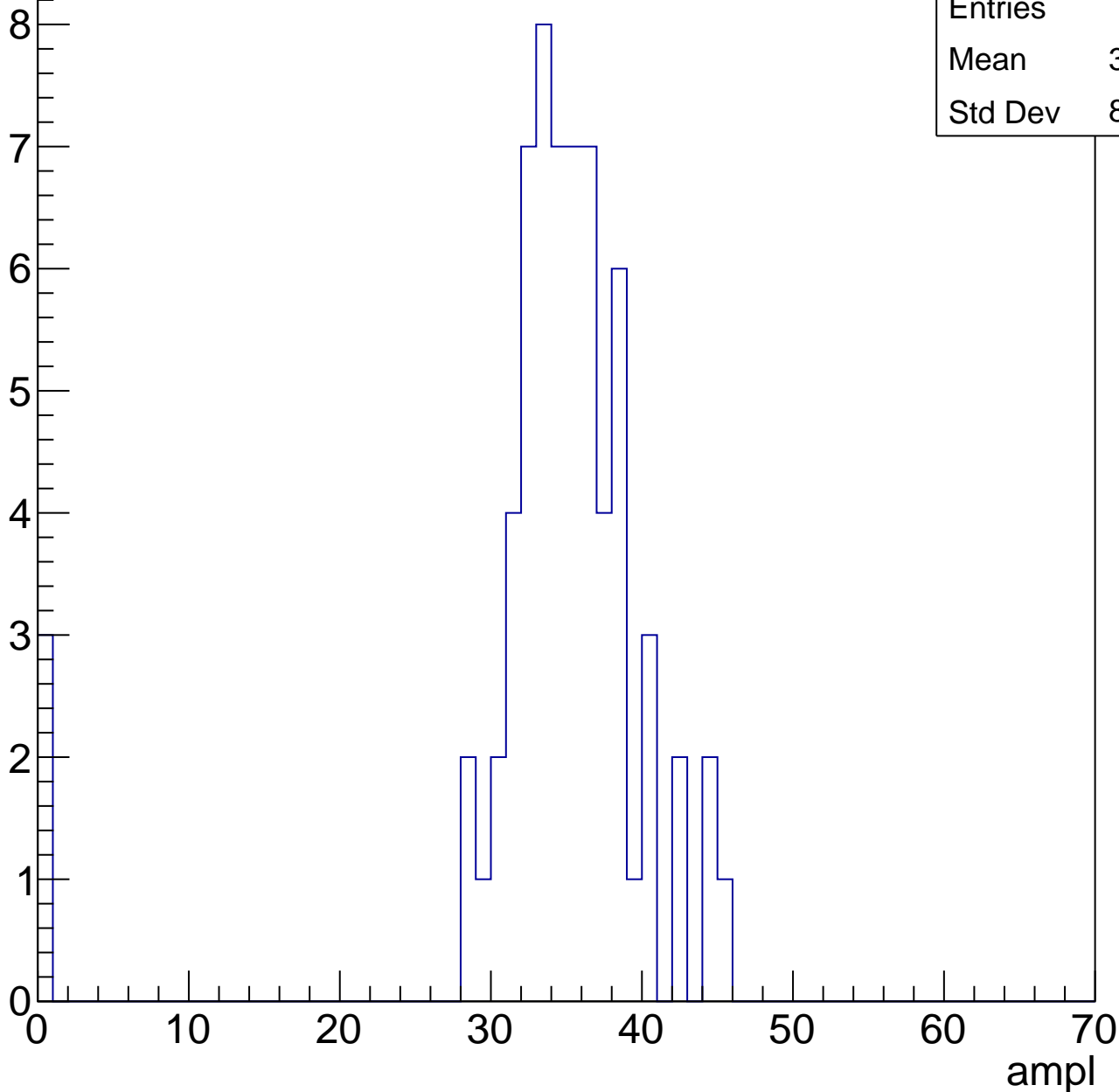


# B1L103S, U4-ch119, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 67    |
| Mean    | 33.49 |
| Std Dev | 8.104 |

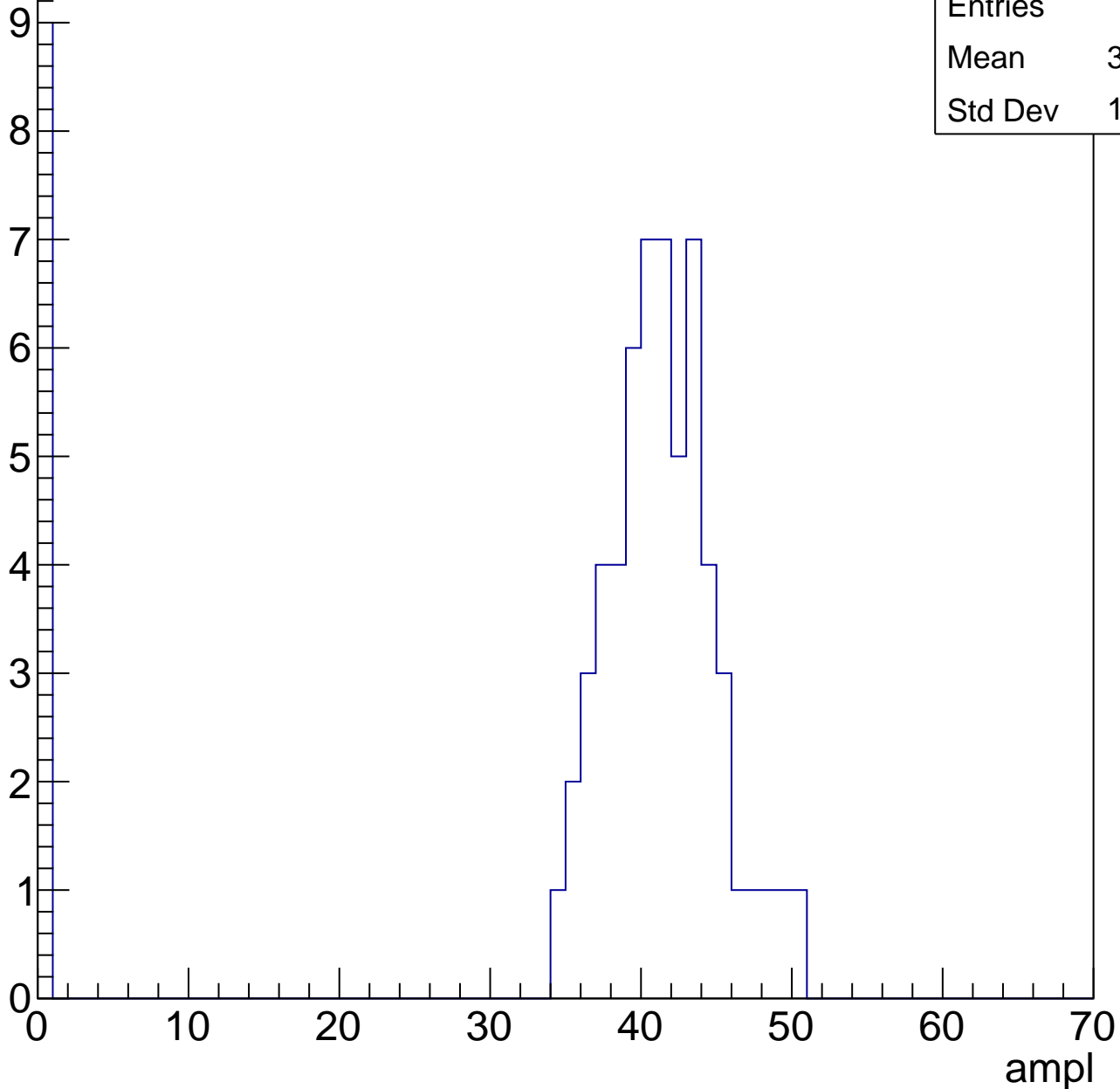


# B1L103S, U4-ch119, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 67    |
| Mean    | 35.45 |
| Std Dev | 14.33 |

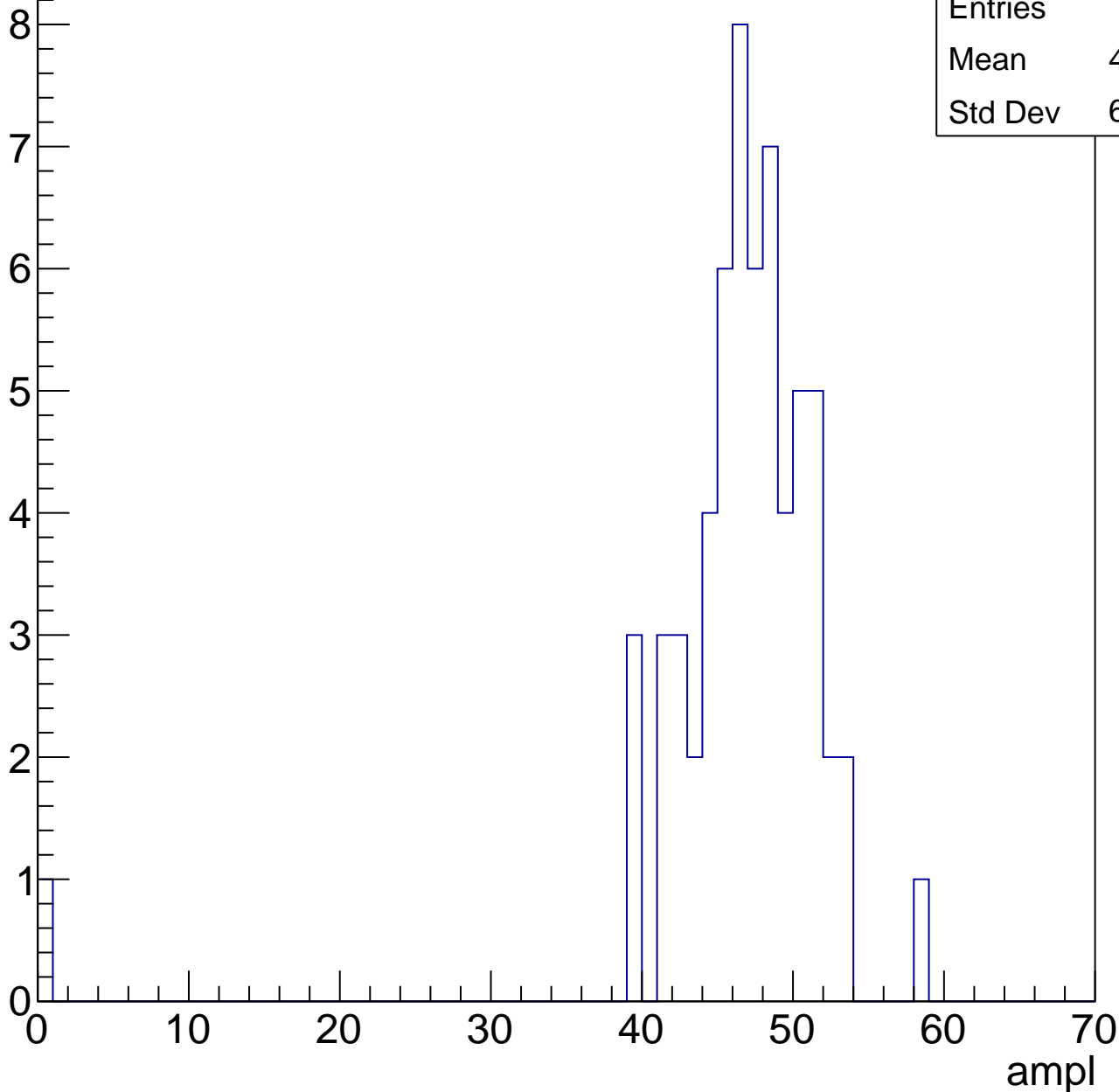


# B1L103S, U4-ch119, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 62    |
| Mean    | 46.02 |
| Std Dev | 6.973 |



# B1L103S, U4-ch119, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 72    |
| Mean    | 53.28 |
| Std Dev | 3.481 |

Entry

10

8

6

4

2

0

0

10

20

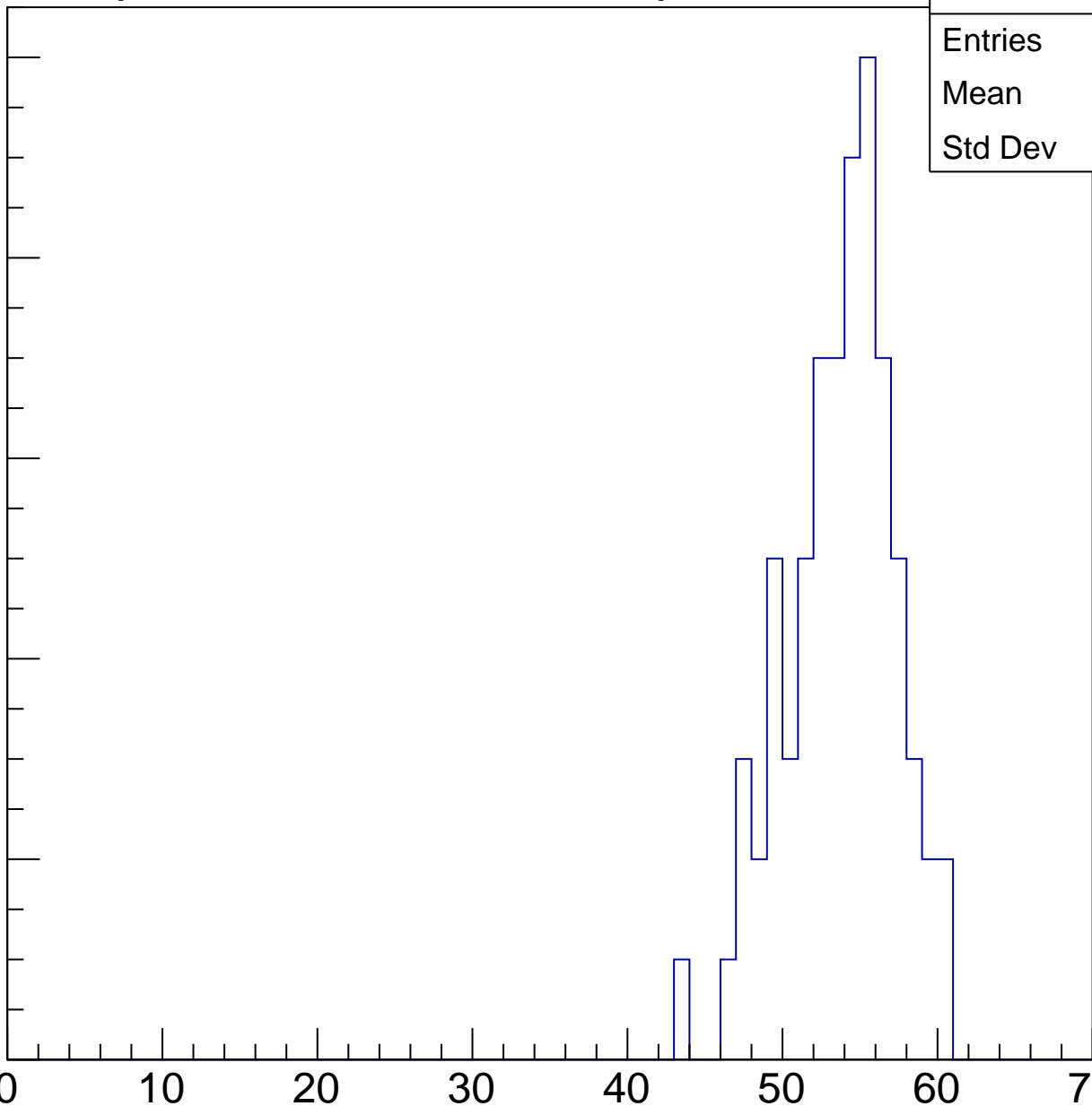
30

40

50

60

ampl

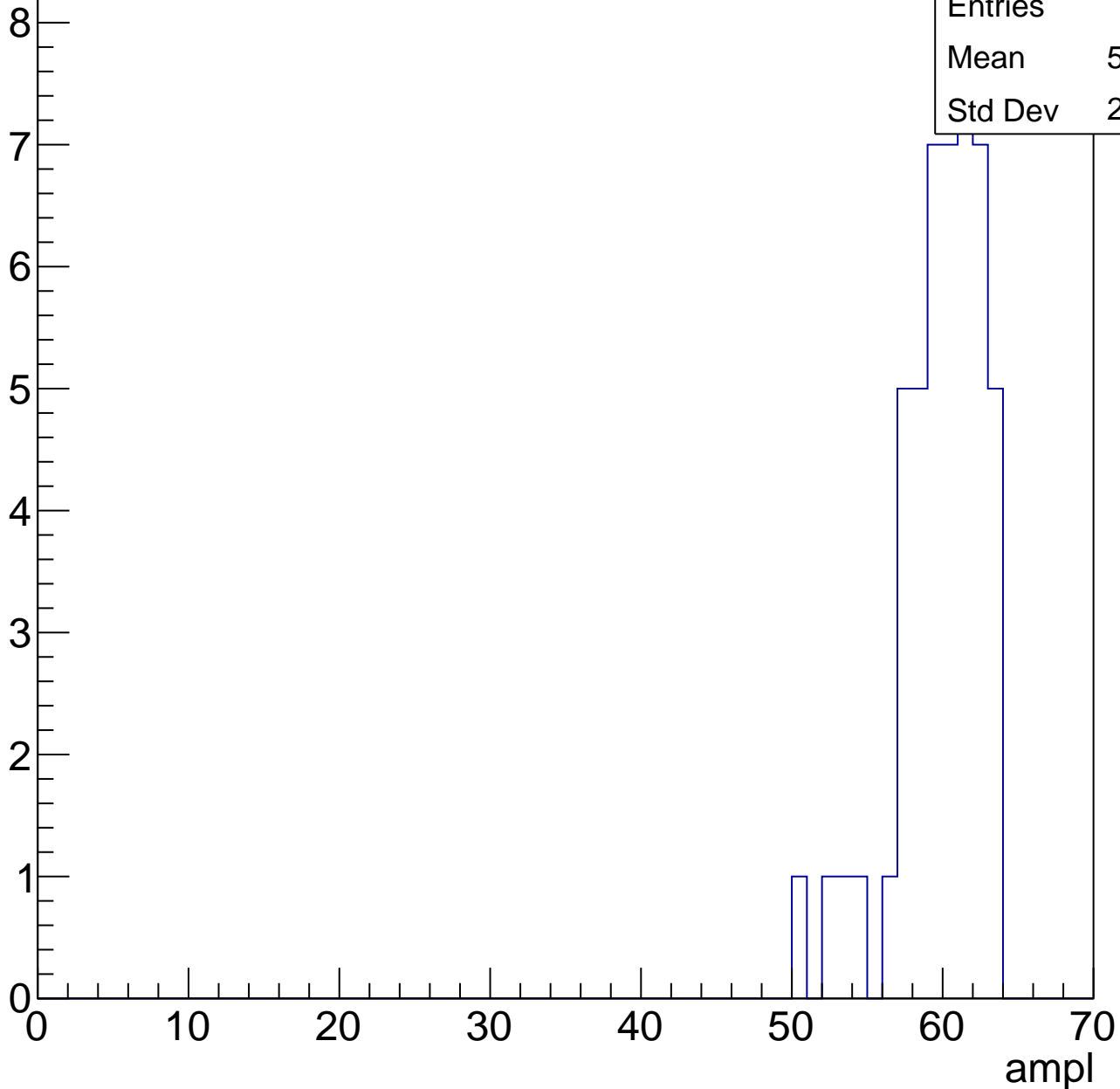


# B1L103S, U4-ch119, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 49    |
| Mean    | 59.39 |
| Std Dev | 2.856 |

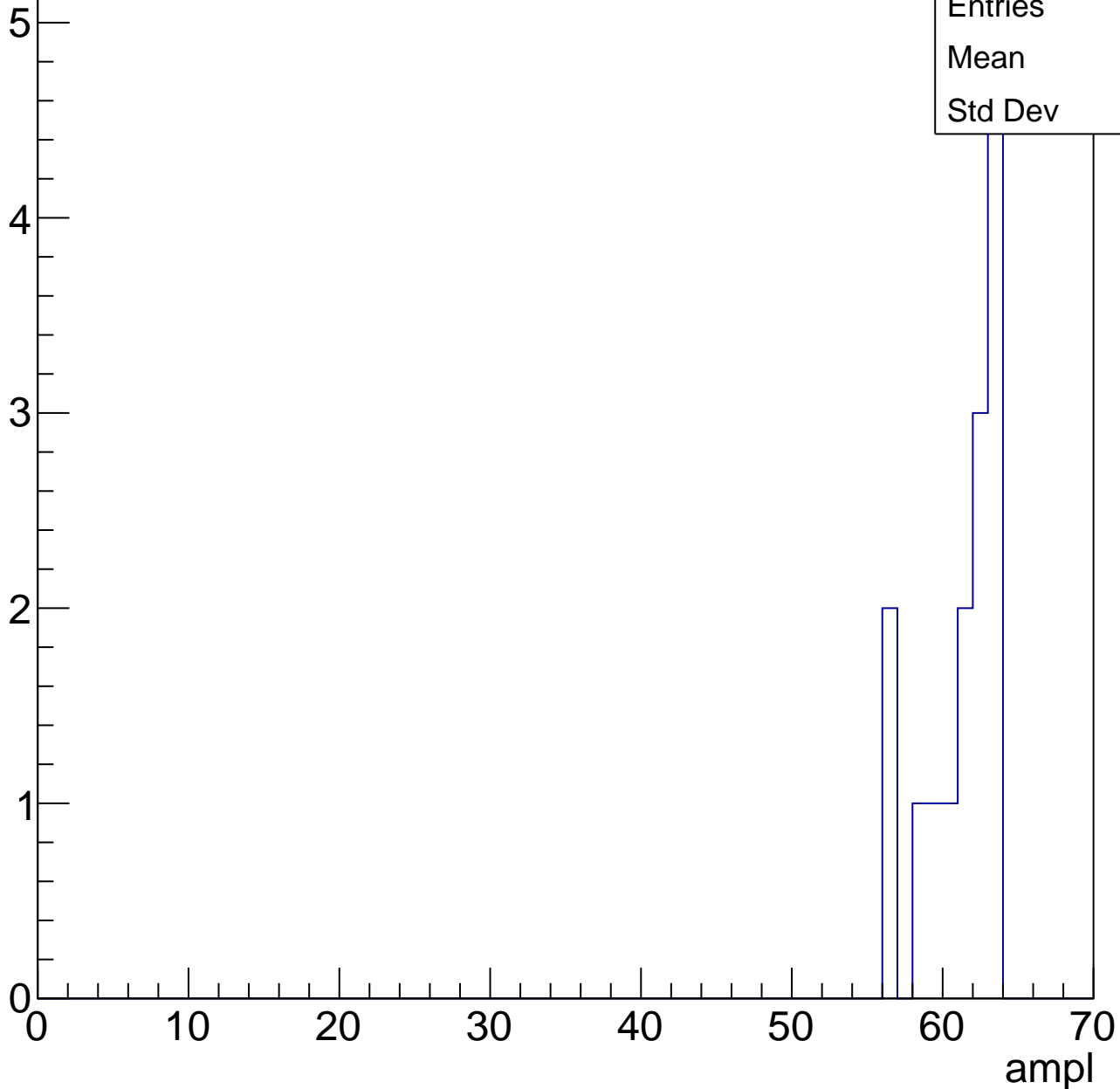


# B1L103S, U4-ch119, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |      |
|---------|------|
| Entries | 15   |
| Mean    | 60.8 |
| Std Dev | 2.4  |





# B1L103S, U4-ch119, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

|         |    |
|---------|----|
| Entries | 20 |
| Mean    | 0  |
| Std Dev | 0  |

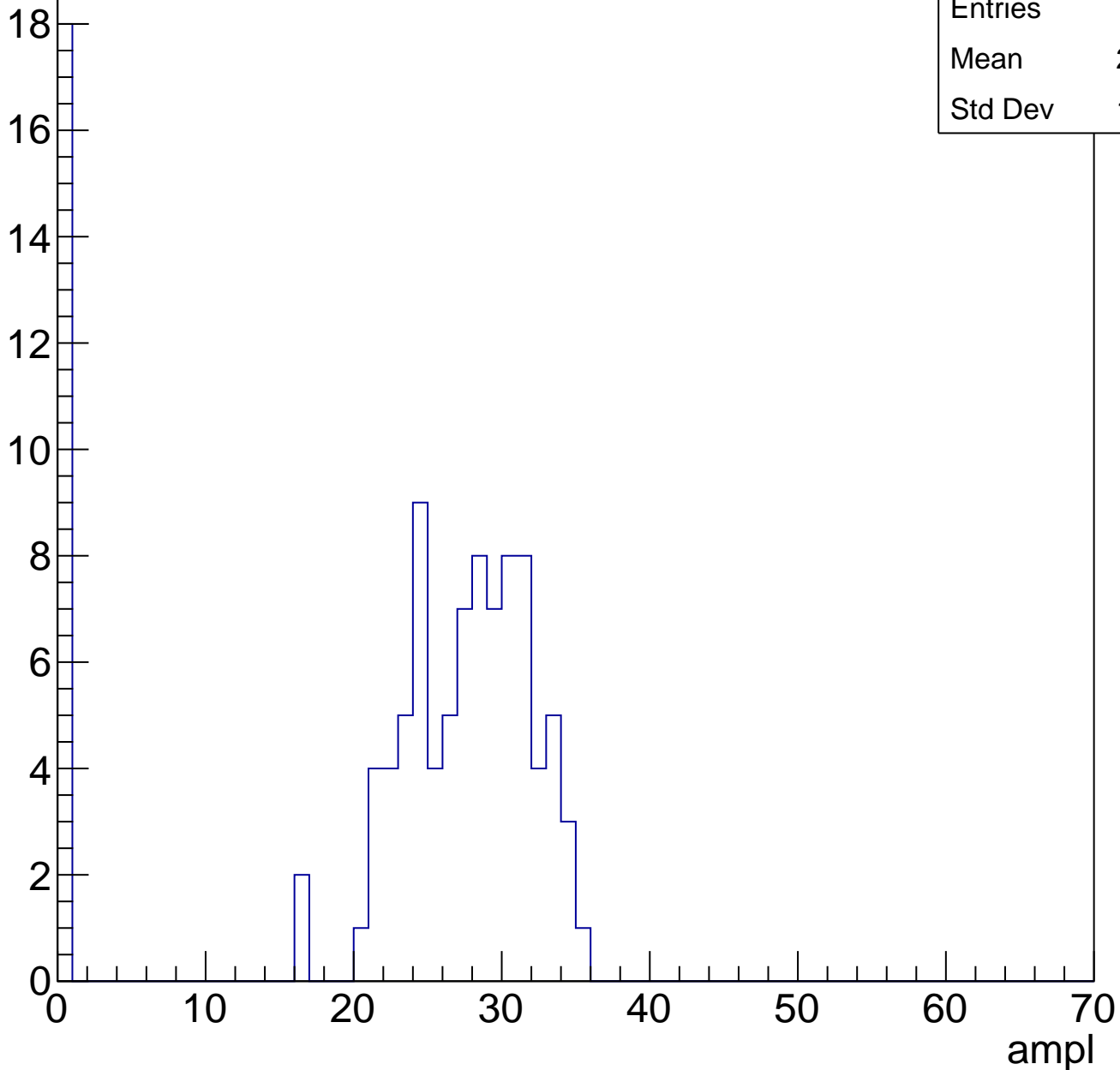
ampl

# B1L103S, U4-ch120, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 103   |
| Mean    | 22.51 |
| Std Dev | 11.01 |

Entry

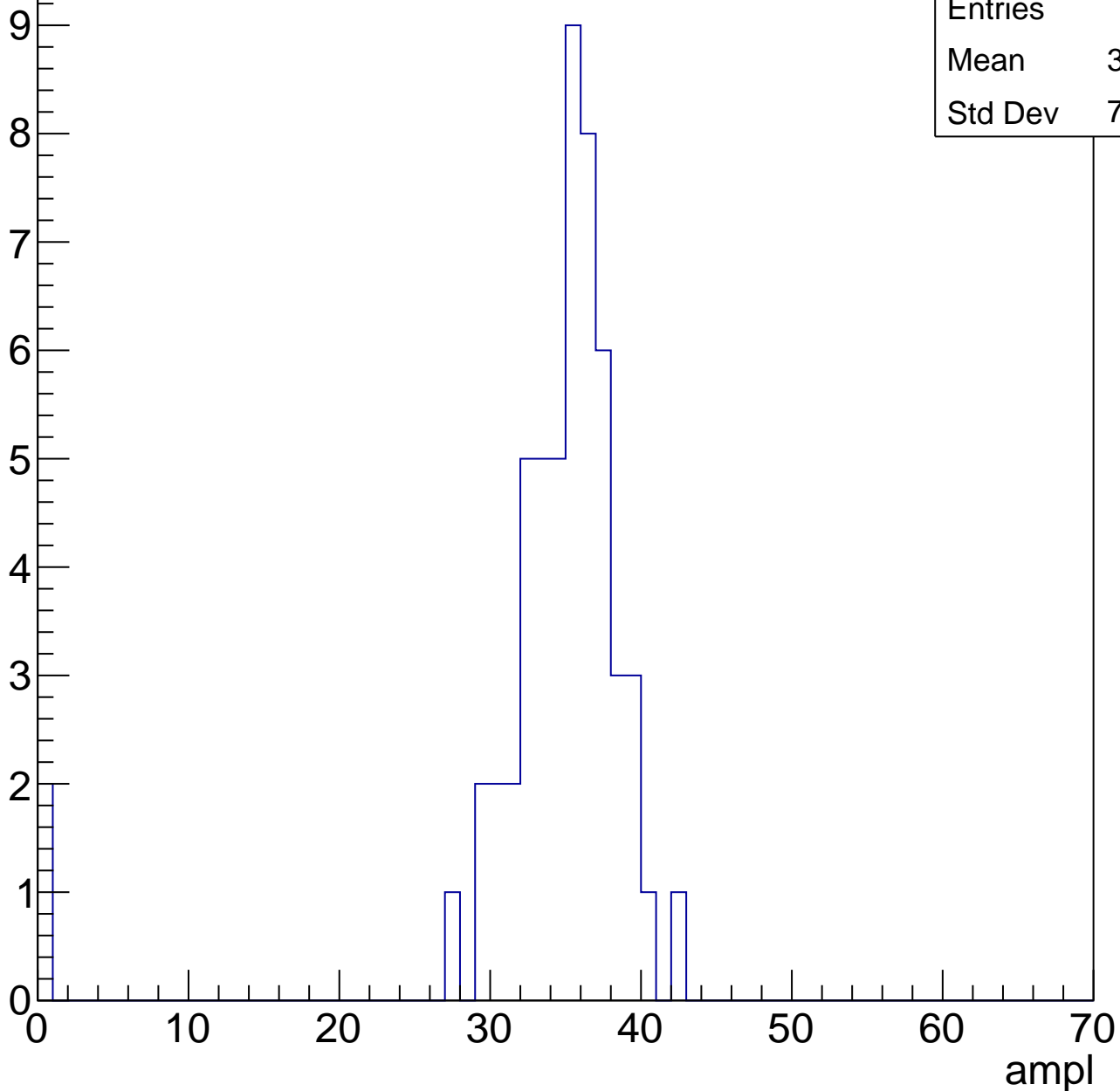


# B1L103S, U4-ch120, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 55    |
| Mean    | 33.45 |
| Std Dev | 7.119 |



# B1L103S, U4-ch120, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

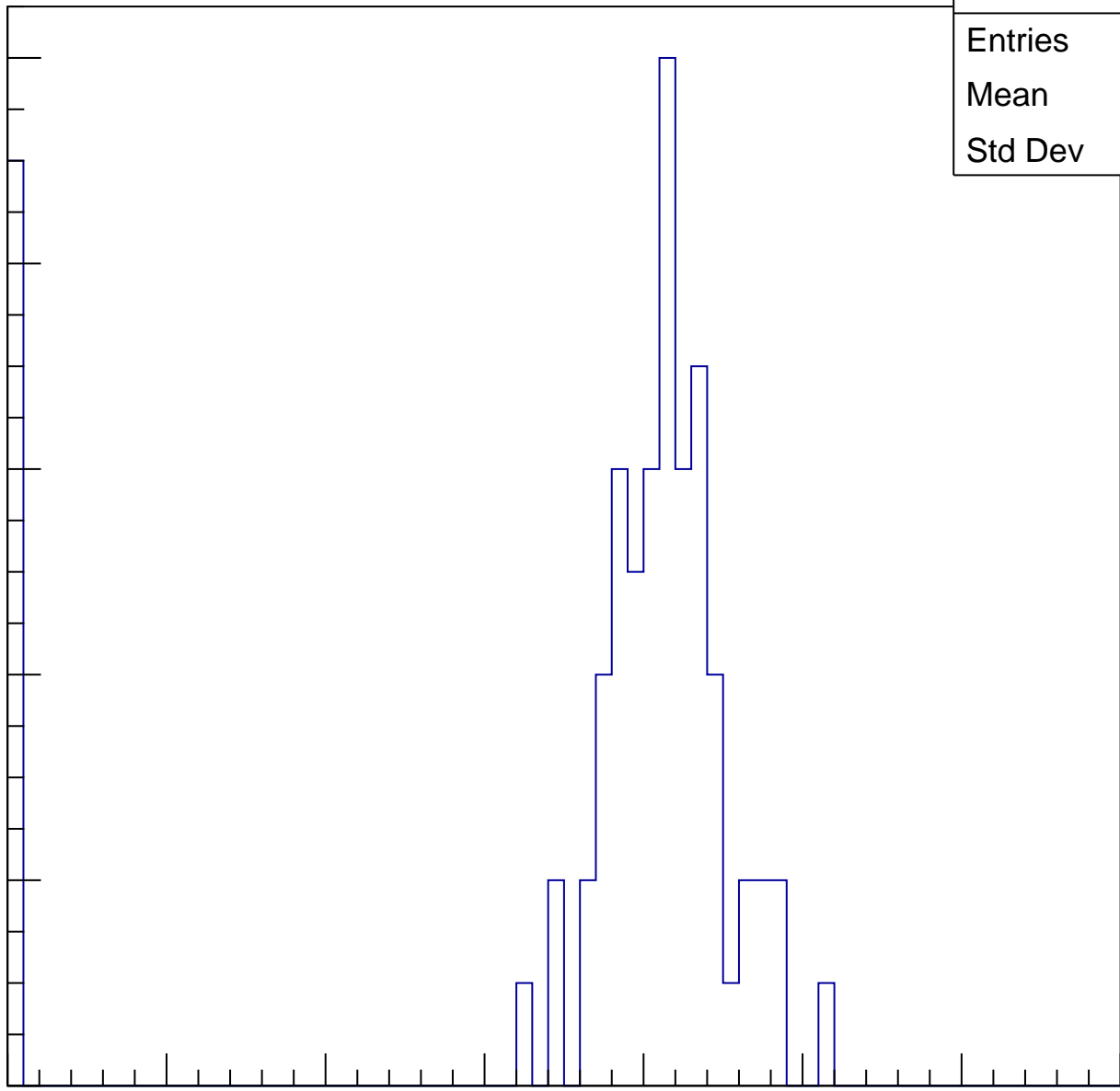
|         |       |
|---------|-------|
| Entries | 70    |
| Mean    | 35.71 |
| Std Dev | 14.12 |

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

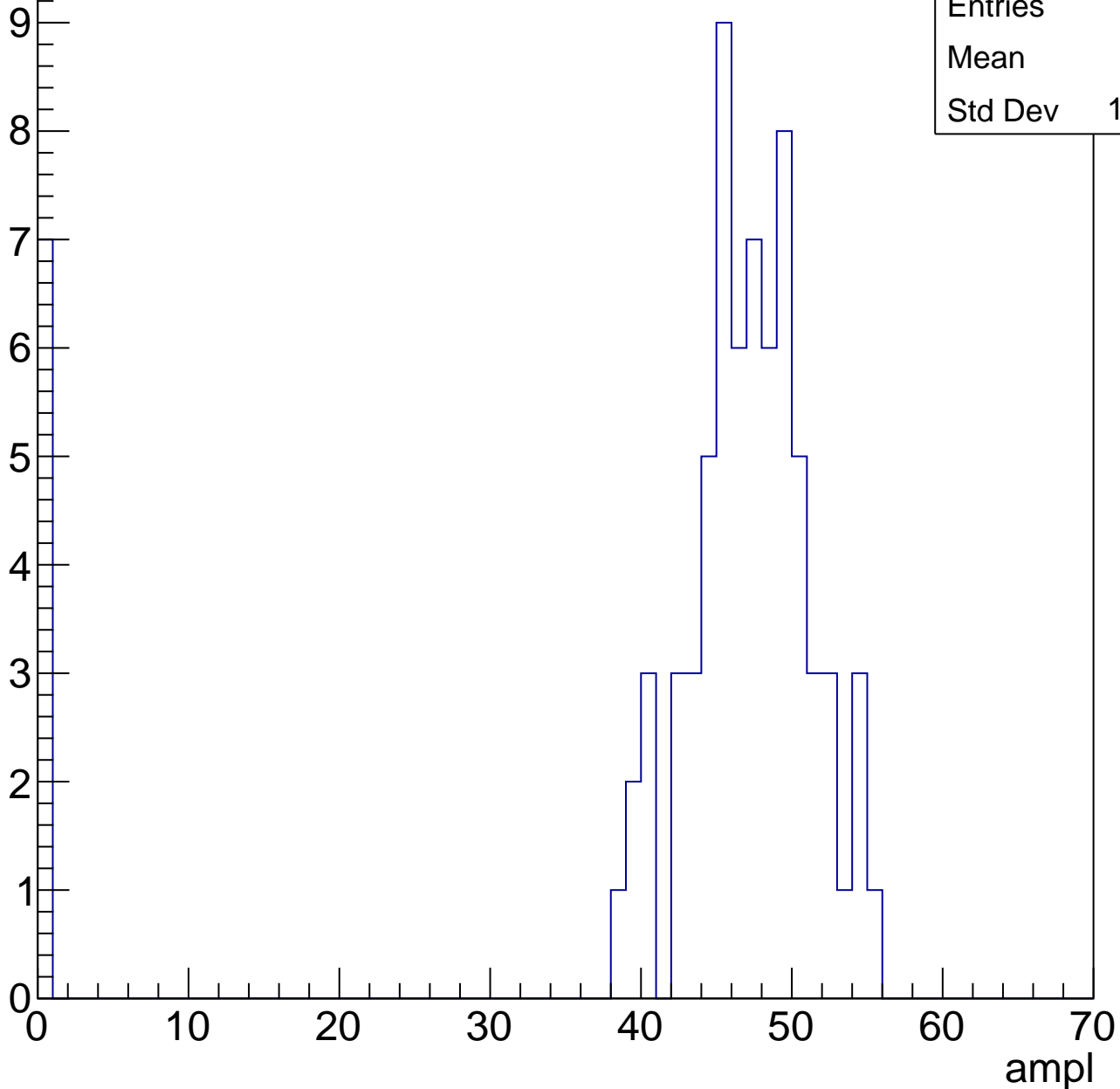


# B1L103S, U4-ch120, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

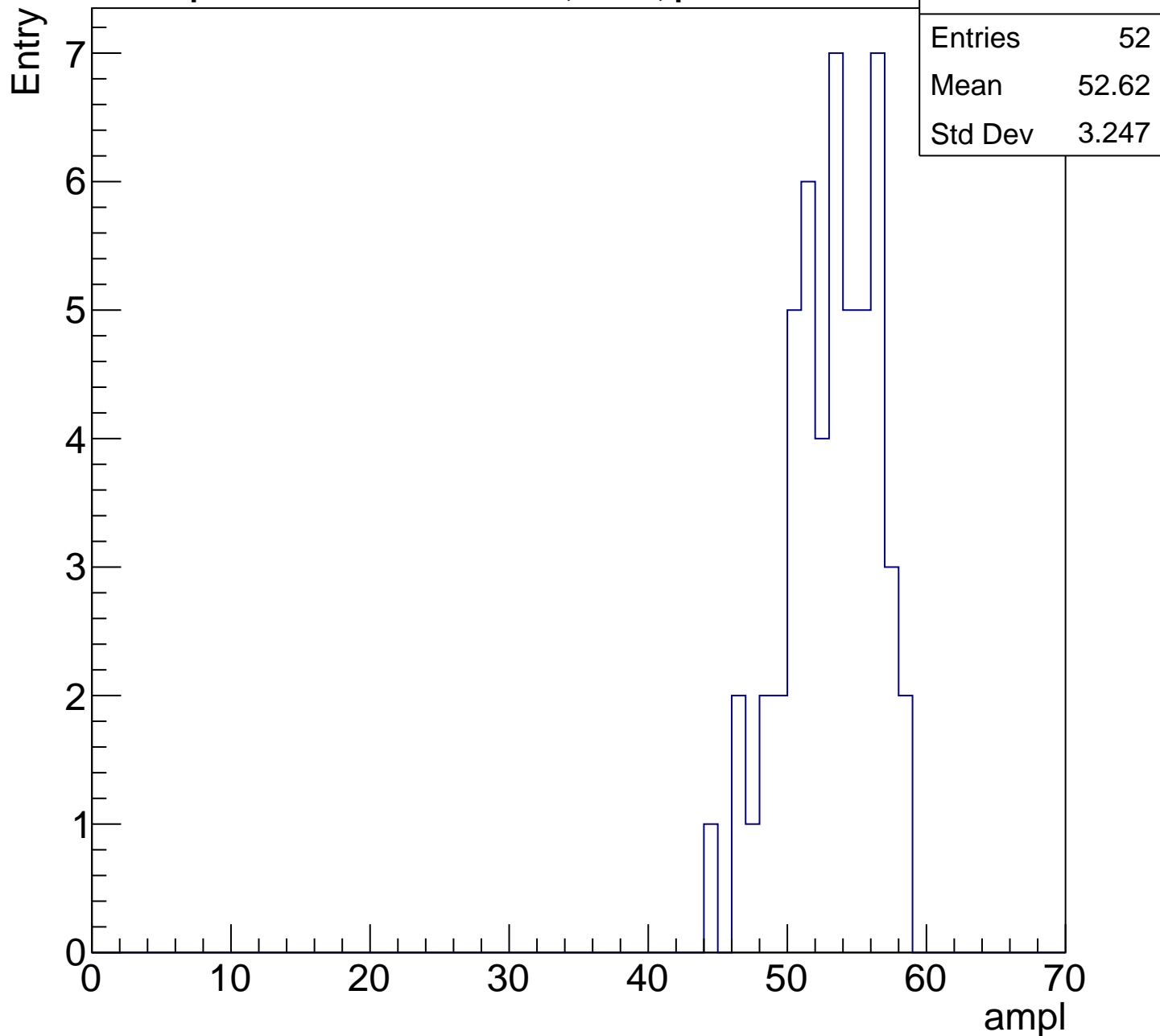
Entry

|         |       |
|---------|-------|
| Entries | 76    |
| Mean    | 42.5  |
| Std Dev | 14.02 |



# B1L103S, U4-ch120, adc4

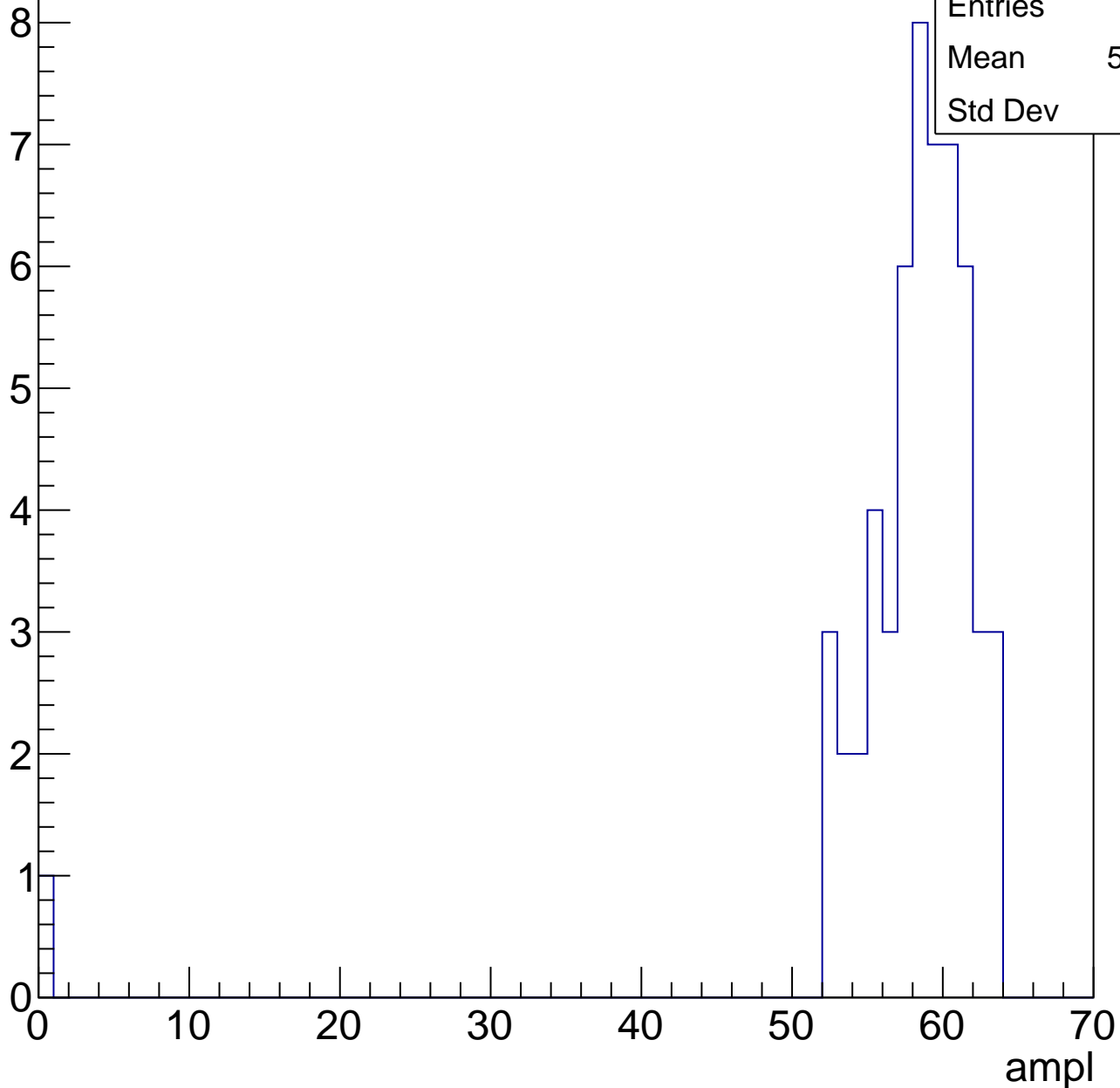
calib\_packv5\_041523\_1651.root, FC#0, port C2



# B1L103S, U4-ch120, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

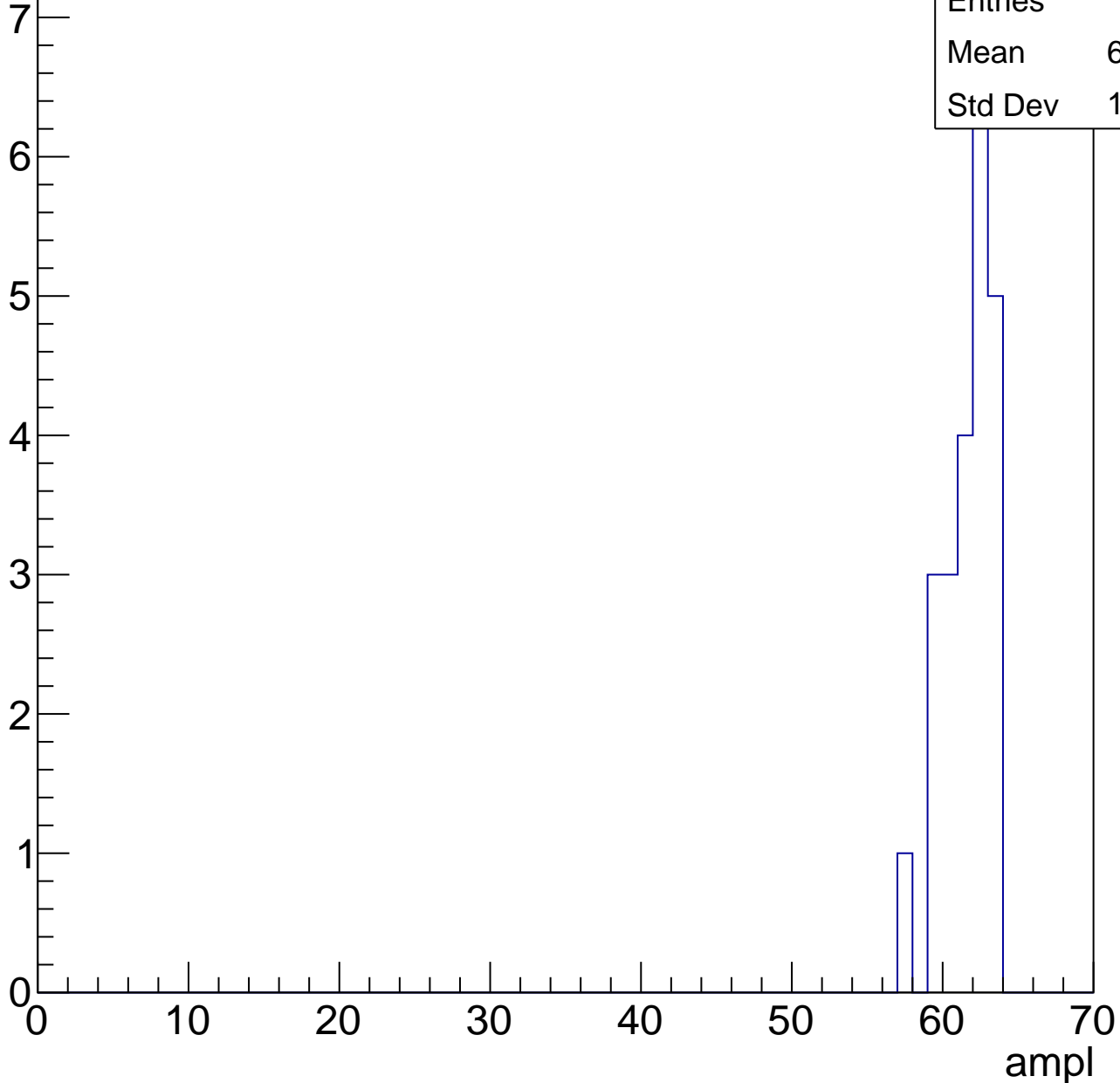


# B1L103S, U4-ch120, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 23    |
| Mean    | 61.17 |
| Std Dev | 1.578 |





# B1L103S, U4-ch120, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 21    |
| Mean    | 6     |
| Std Dev | 18.49 |

Entry



# B1L103S, U4-ch121, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 82    |
| Mean    | 23.05 |
| Std Dev | 11.71 |

Entry

16  
14  
12  
10  
8  
6  
4  
2  
0

0

10

20

30

40

50

60

70

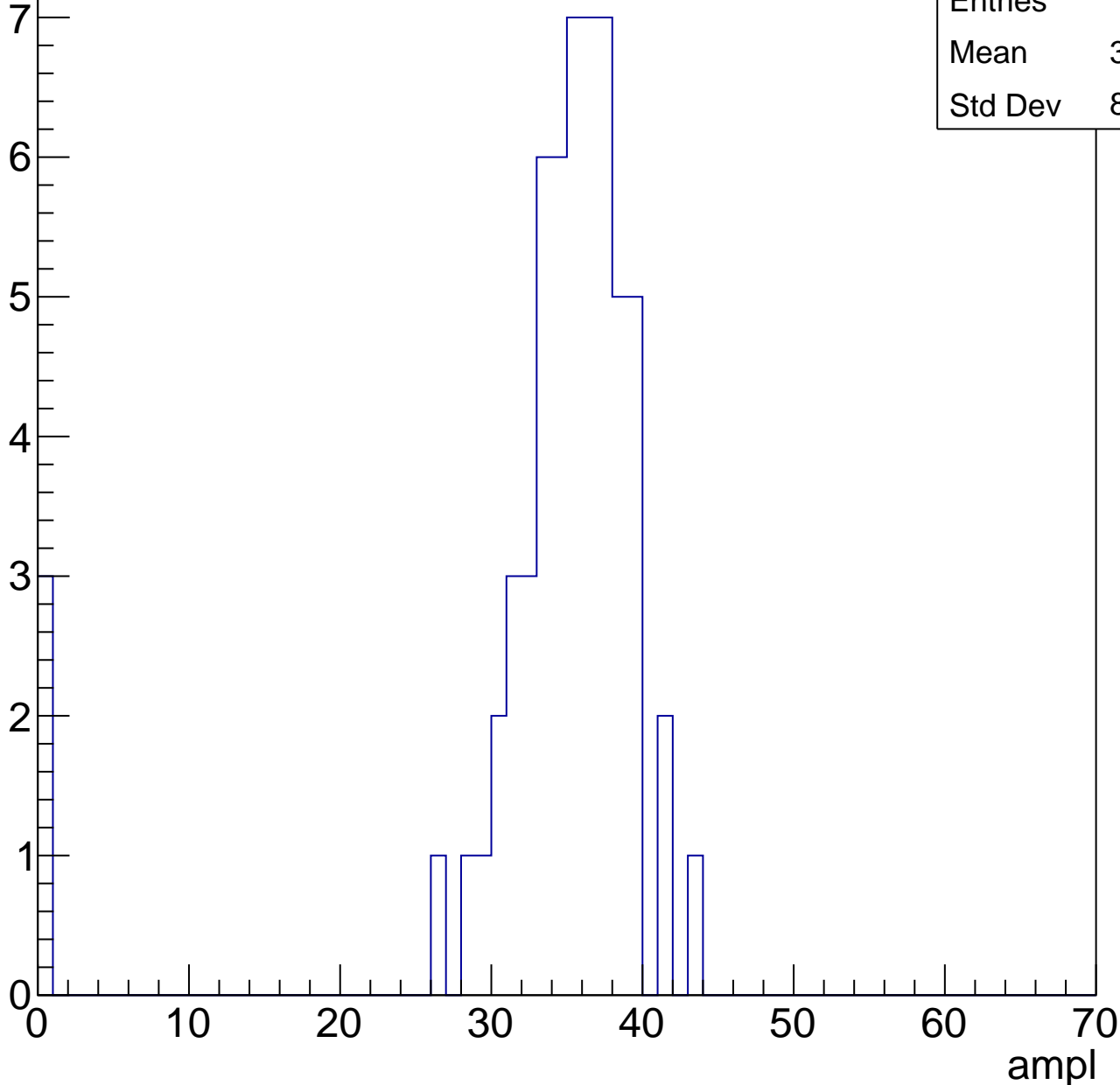
ampl

# B1L103S, U4-ch121, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 60    |
| Mean    | 33.33 |
| Std Dev | 8.292 |



# B1L103S, U4-ch121, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 76    |
| Mean    | 34.68 |
| Std Dev | 14.65 |

Entry

10

8

6

4

2

0

0

10

20

30

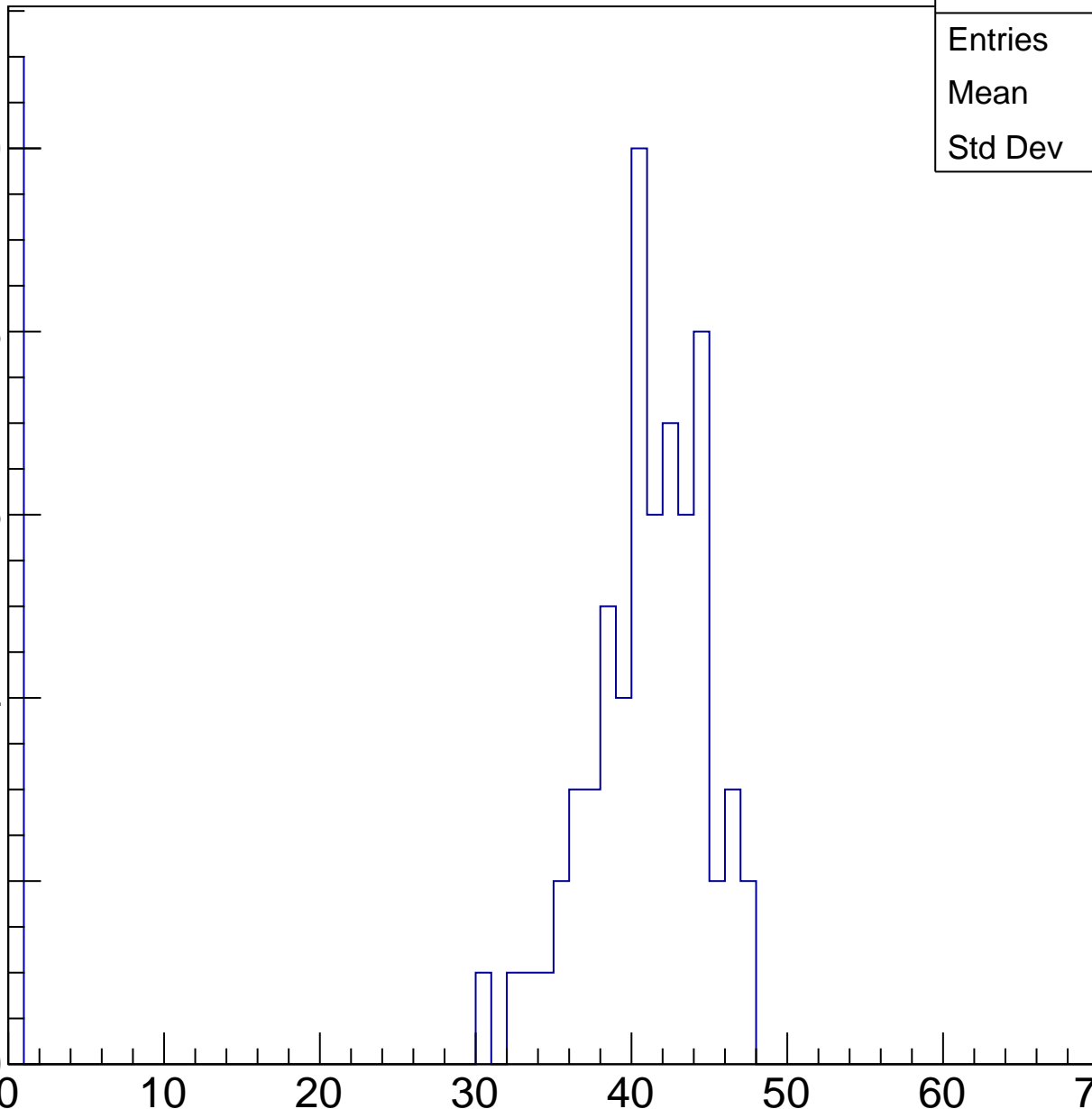
40

50

60

70

ampl

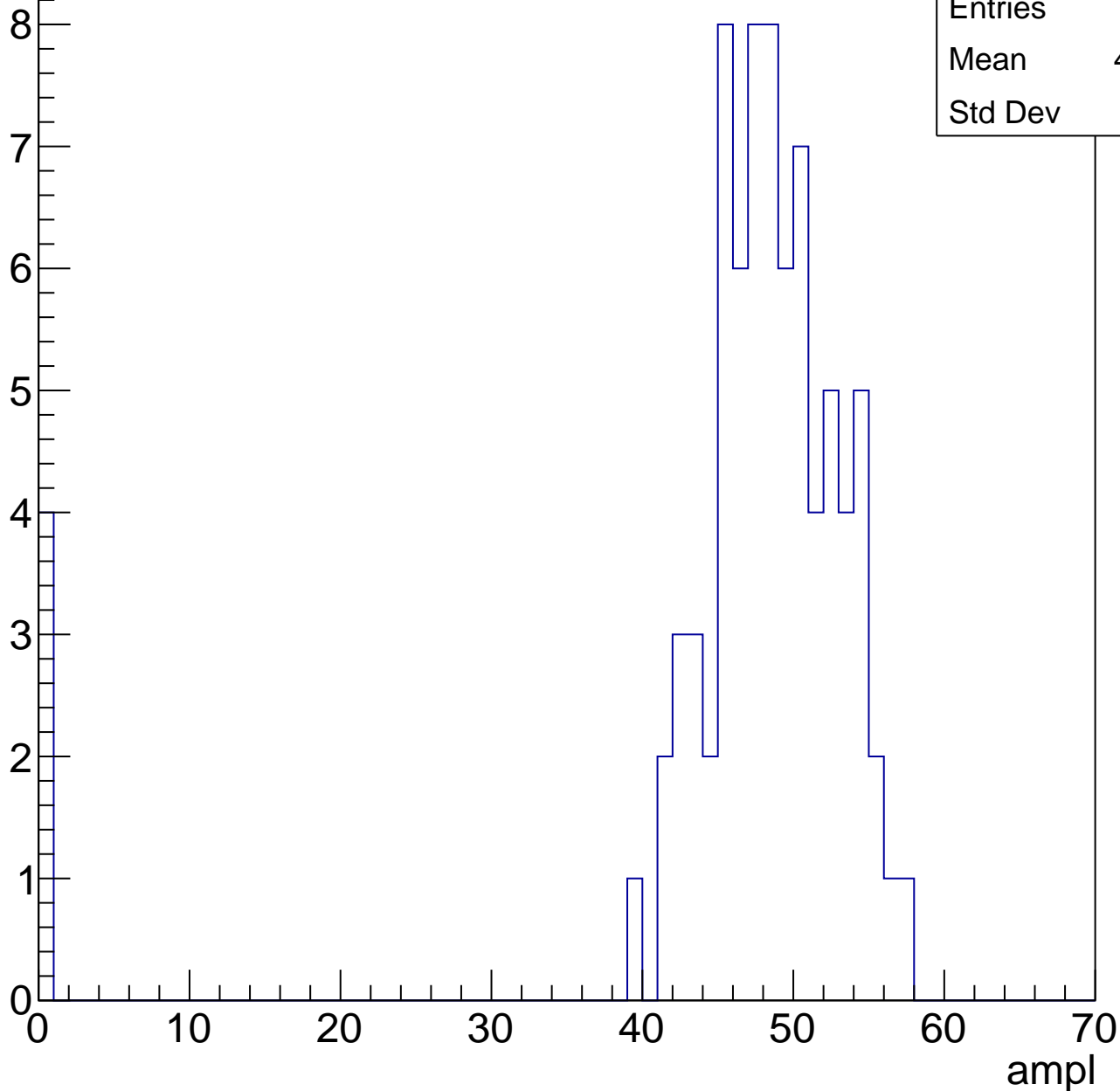


# B1L103S, U4-ch121, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 80    |
| Mean    | 45.91 |
| Std Dev | 11.2  |

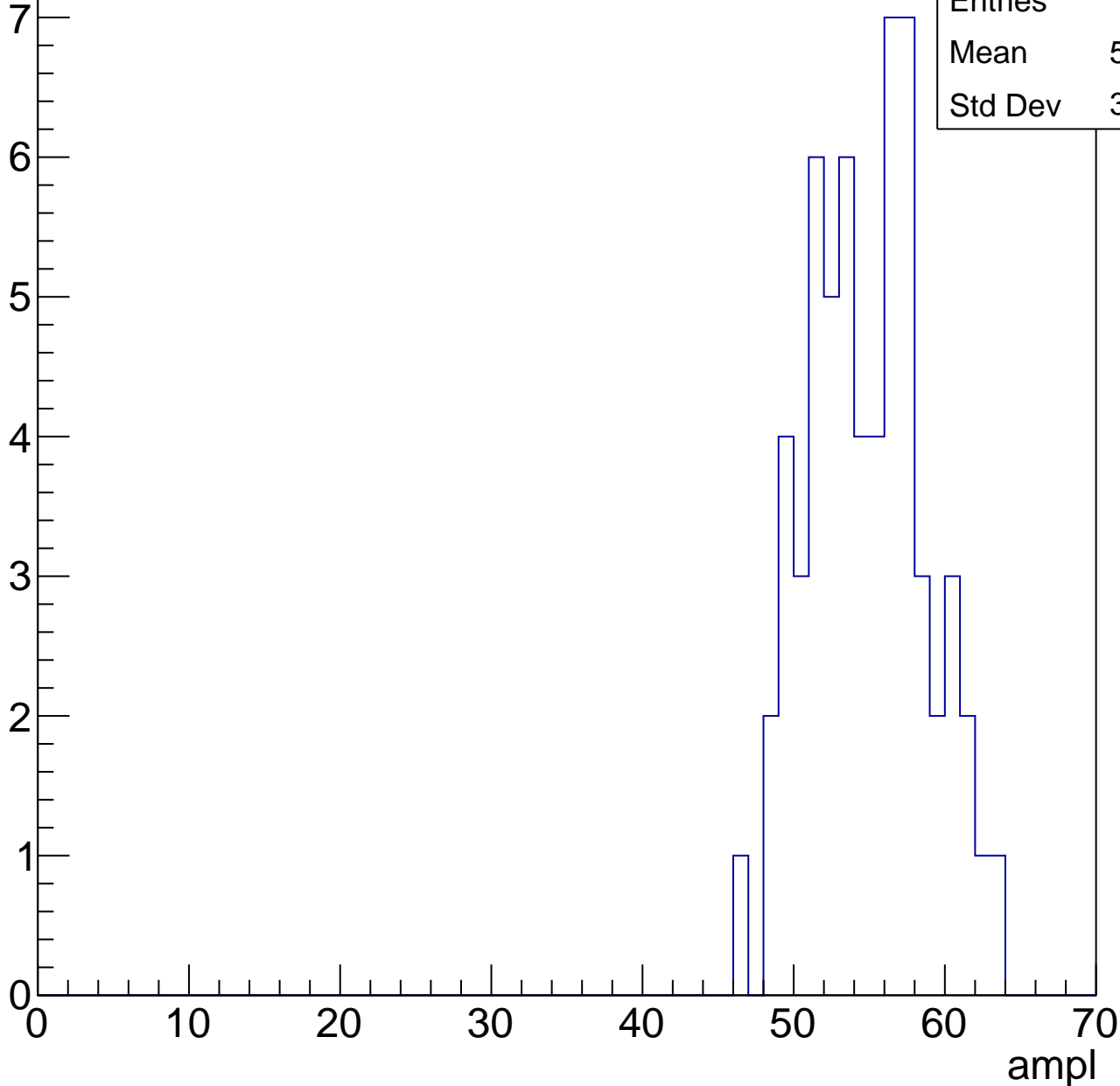


# B1L103S, U4-ch121, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

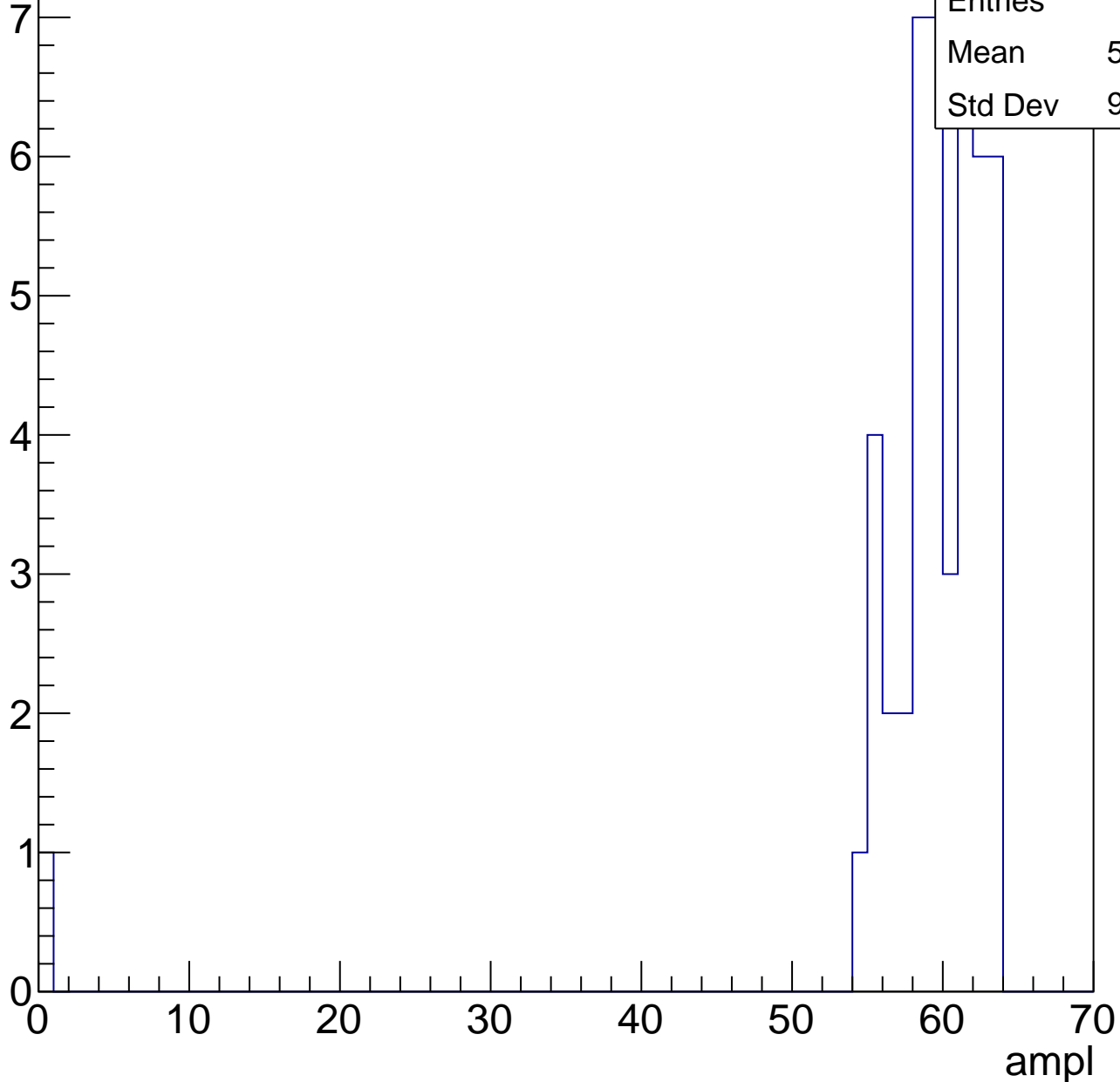
|         |       |
|---------|-------|
| Entries | 61    |
| Mean    | 54.39 |
| Std Dev | 3.838 |



# B1L103S, U4-ch121, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

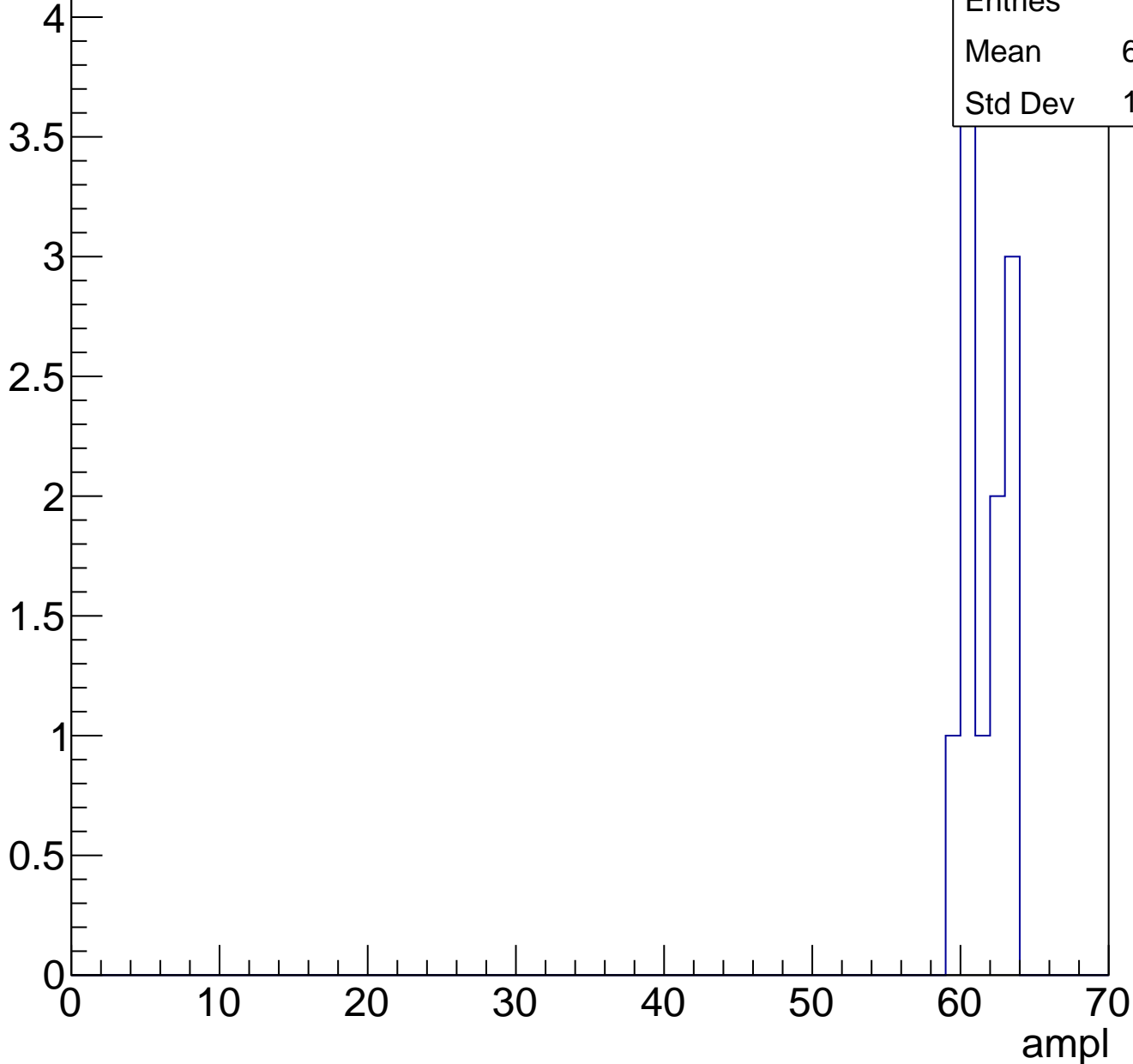
Entry



# B1L103S, U4-ch121, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

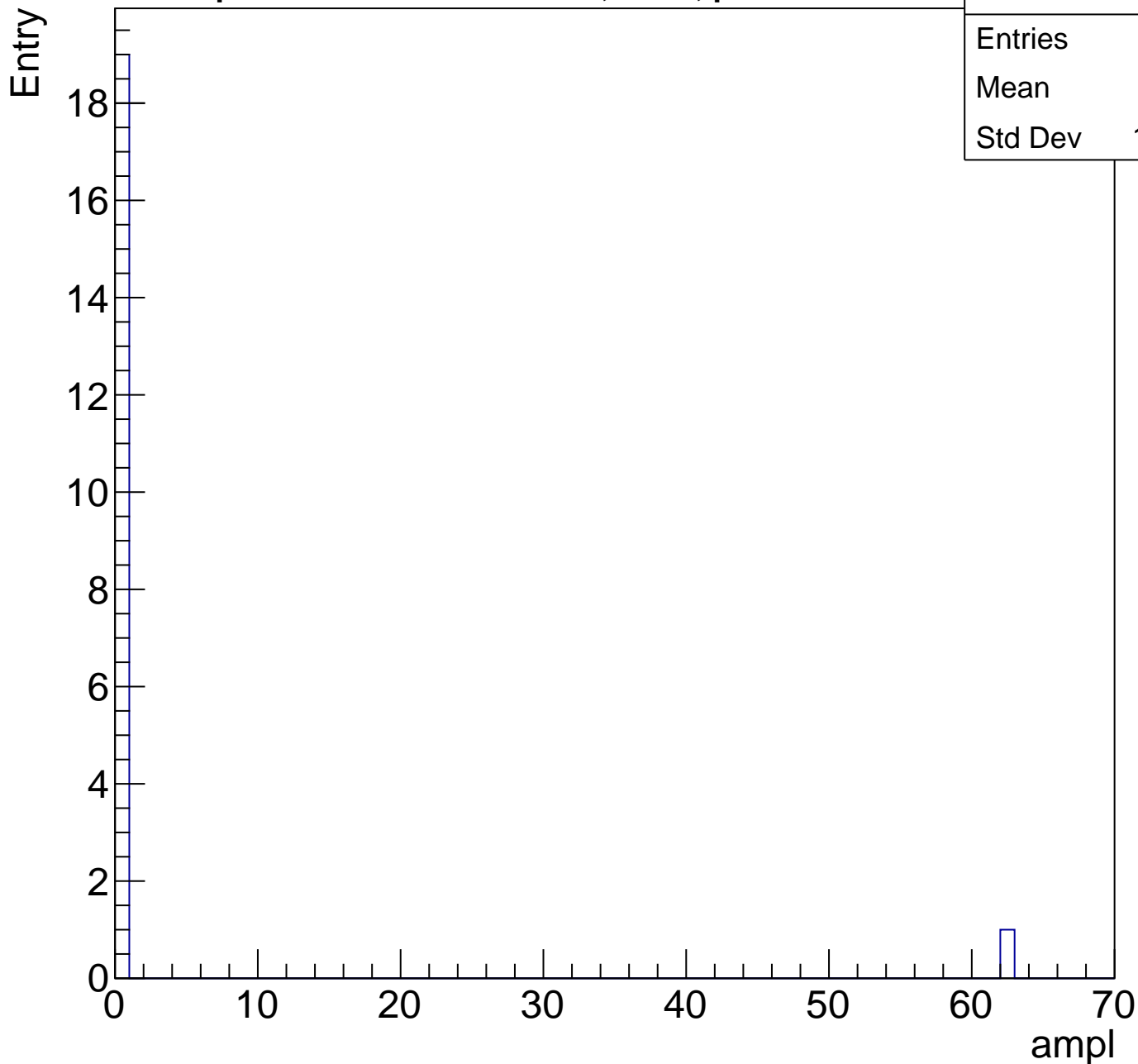




# B1L103S, U4-ch121, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

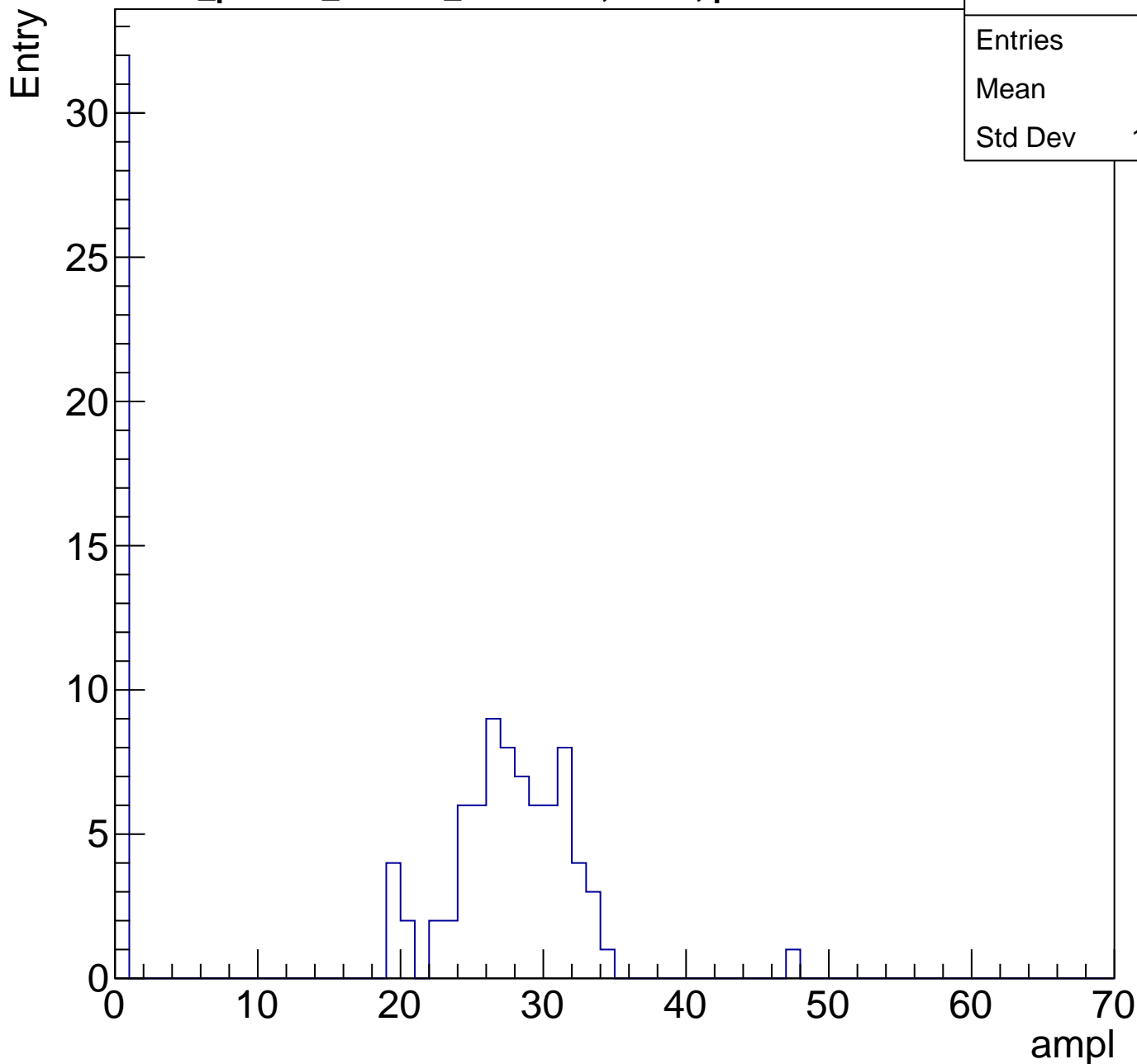
|         |       |
|---------|-------|
| Entries | 20    |
| Mean    | 3.1   |
| Std Dev | 13.51 |



# B1L103S, U4-ch122, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

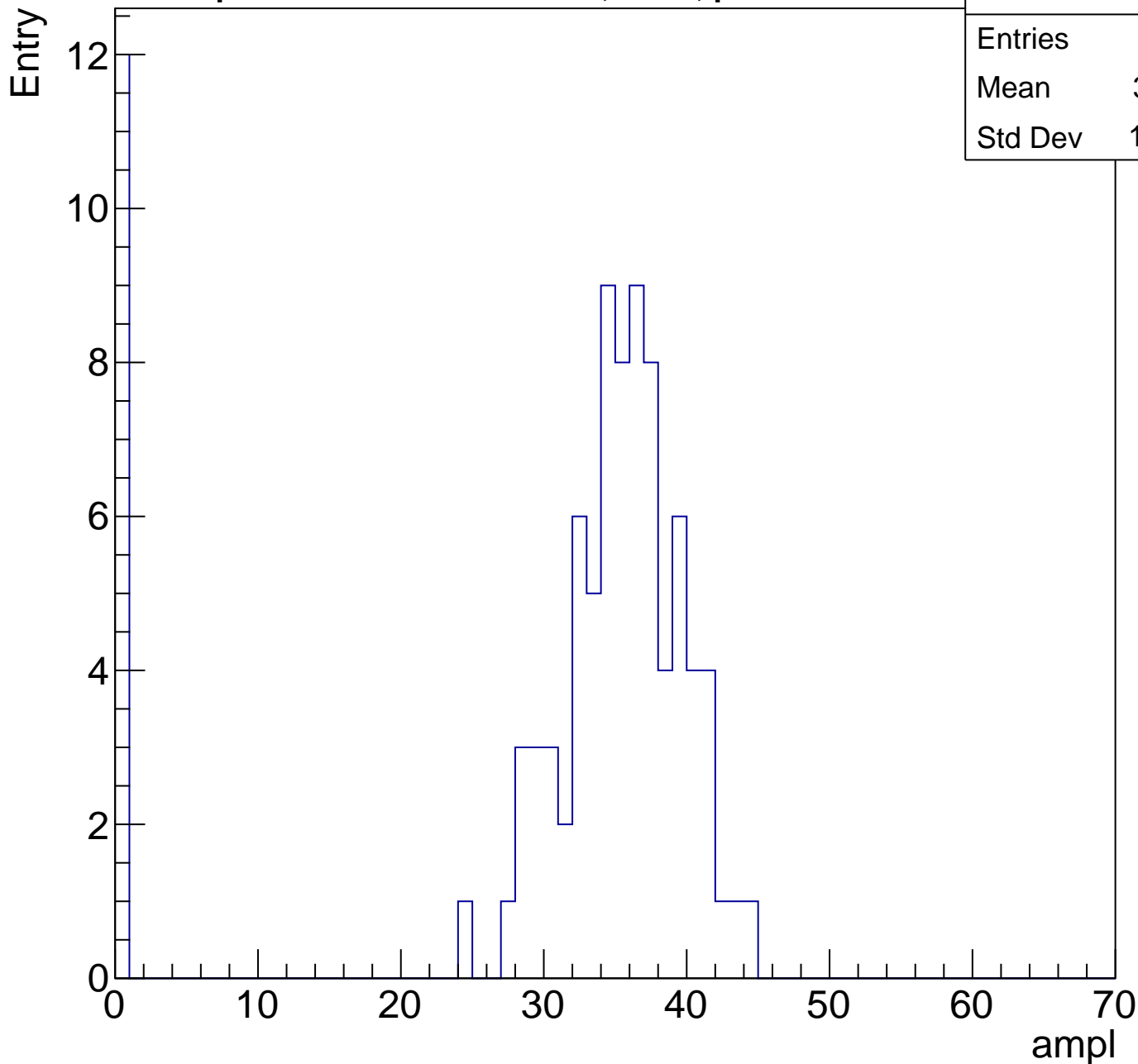
|         |       |
|---------|-------|
| Entries | 107   |
| Mean    | 19.21 |
| Std Dev | 13.05 |



# B1L103S, U4-ch122, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 91    |
| Mean    | 30.51 |
| Std Dev | 12.45 |

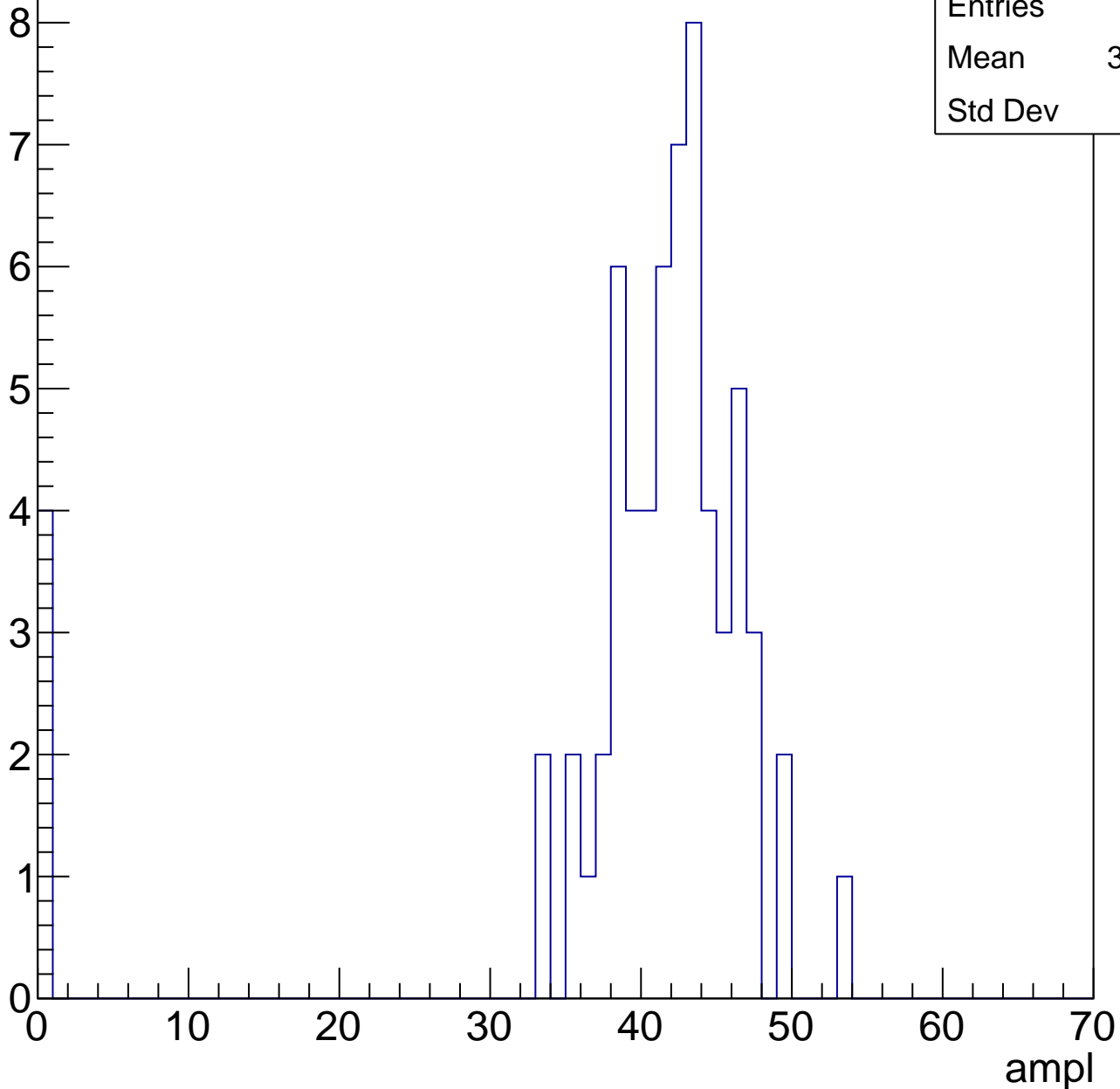


# B1L103S, U4-ch122, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 64    |
| Mean    | 39.17 |
| Std Dev | 10.8  |

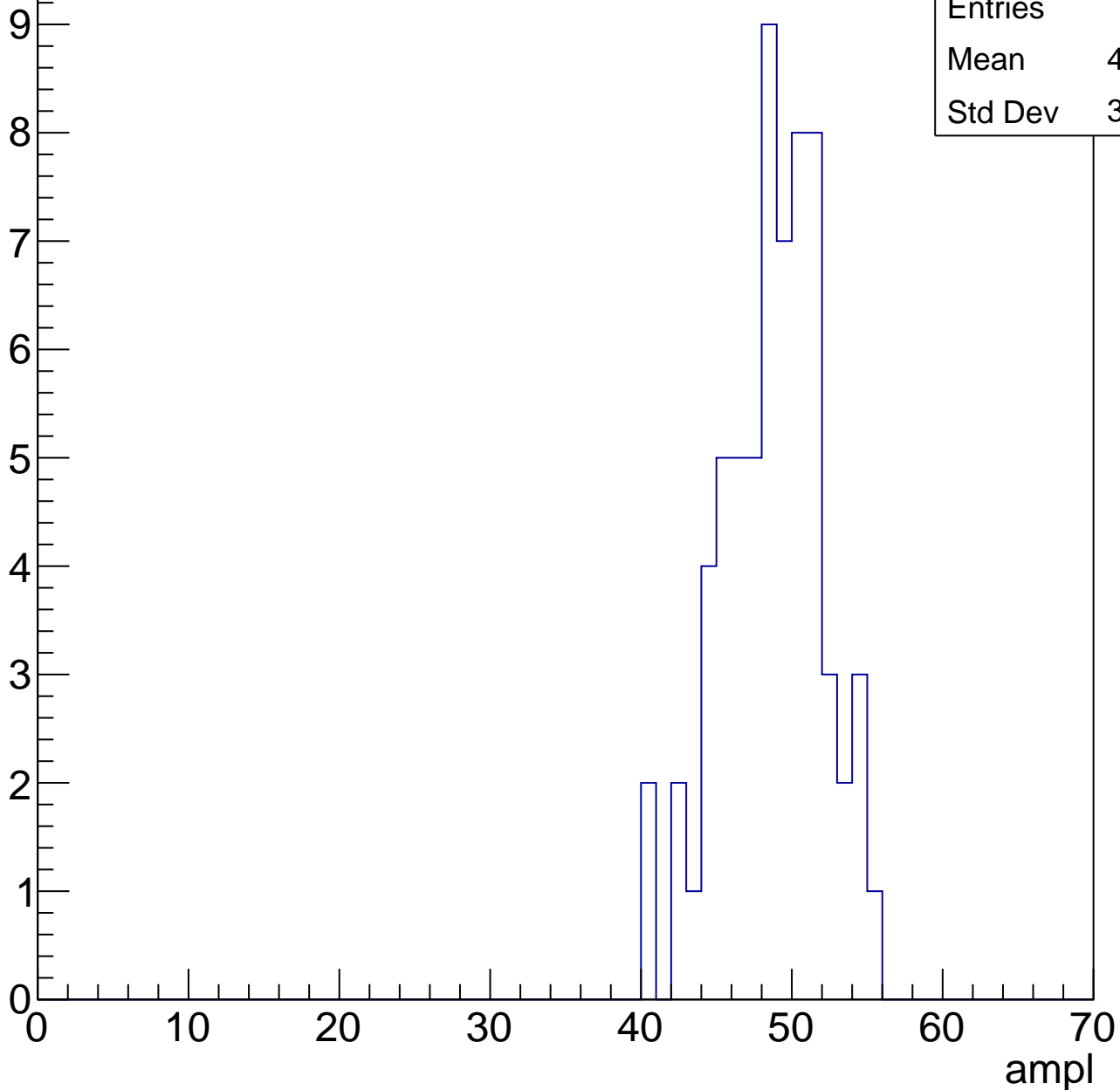


# B1L103S, U4-ch122, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 65    |
| Mean    | 48.23 |
| Std Dev | 3.332 |

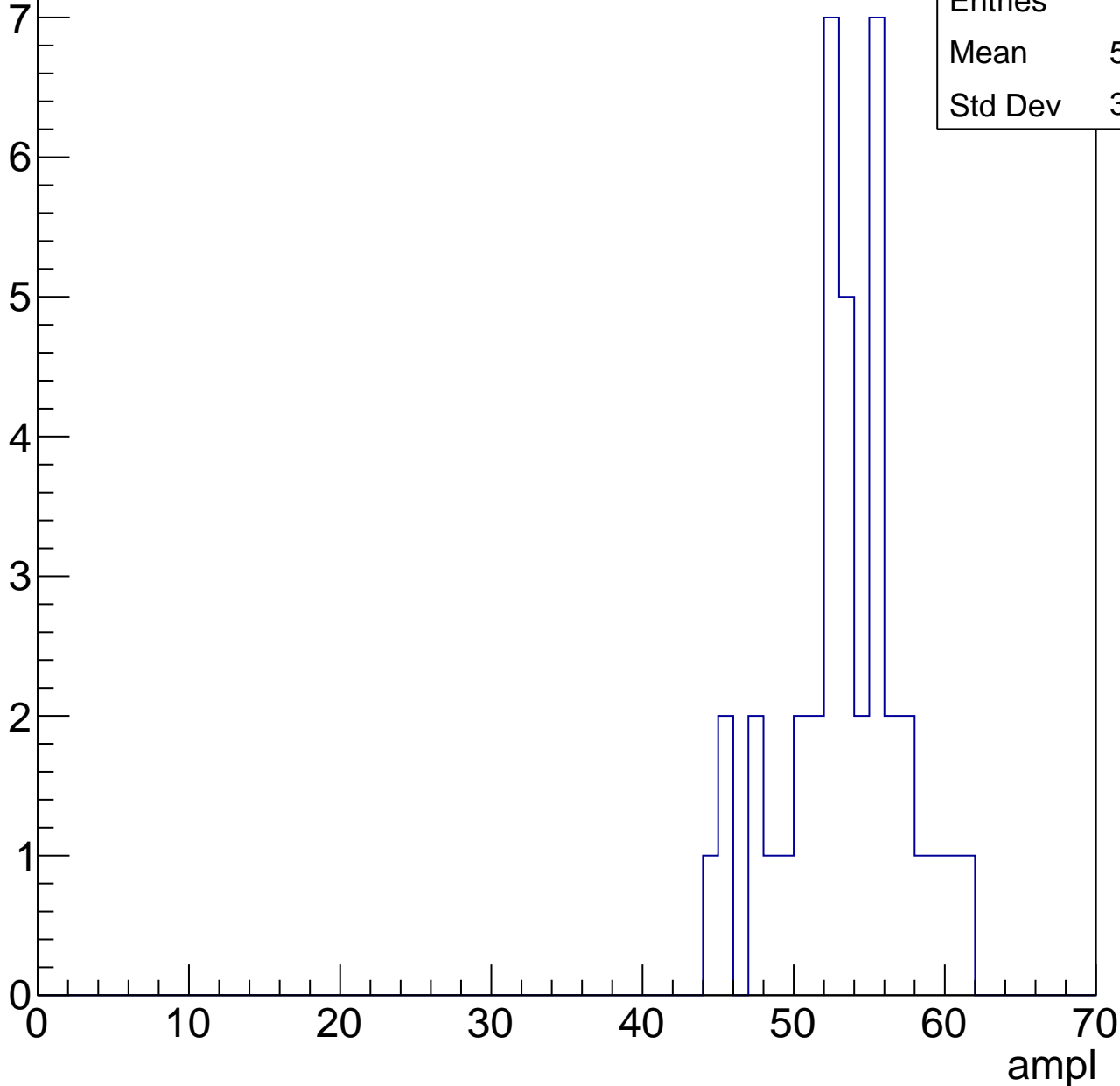


# B1L103S, U4-ch122, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

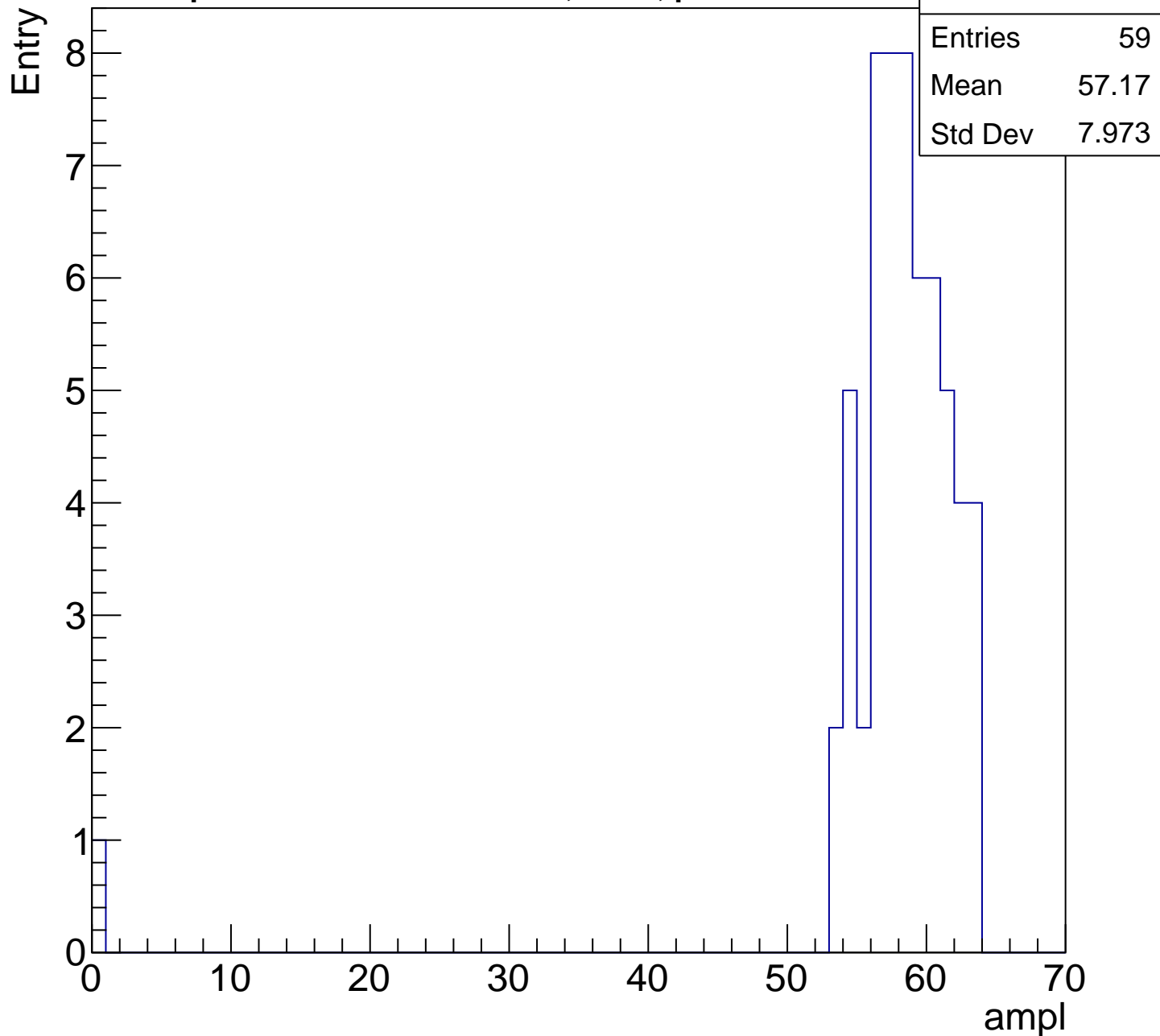
Entry

|         |       |
|---------|-------|
| Entries | 40    |
| Mean    | 52.83 |
| Std Dev | 3.898 |



# B1L103S, U4-ch122, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

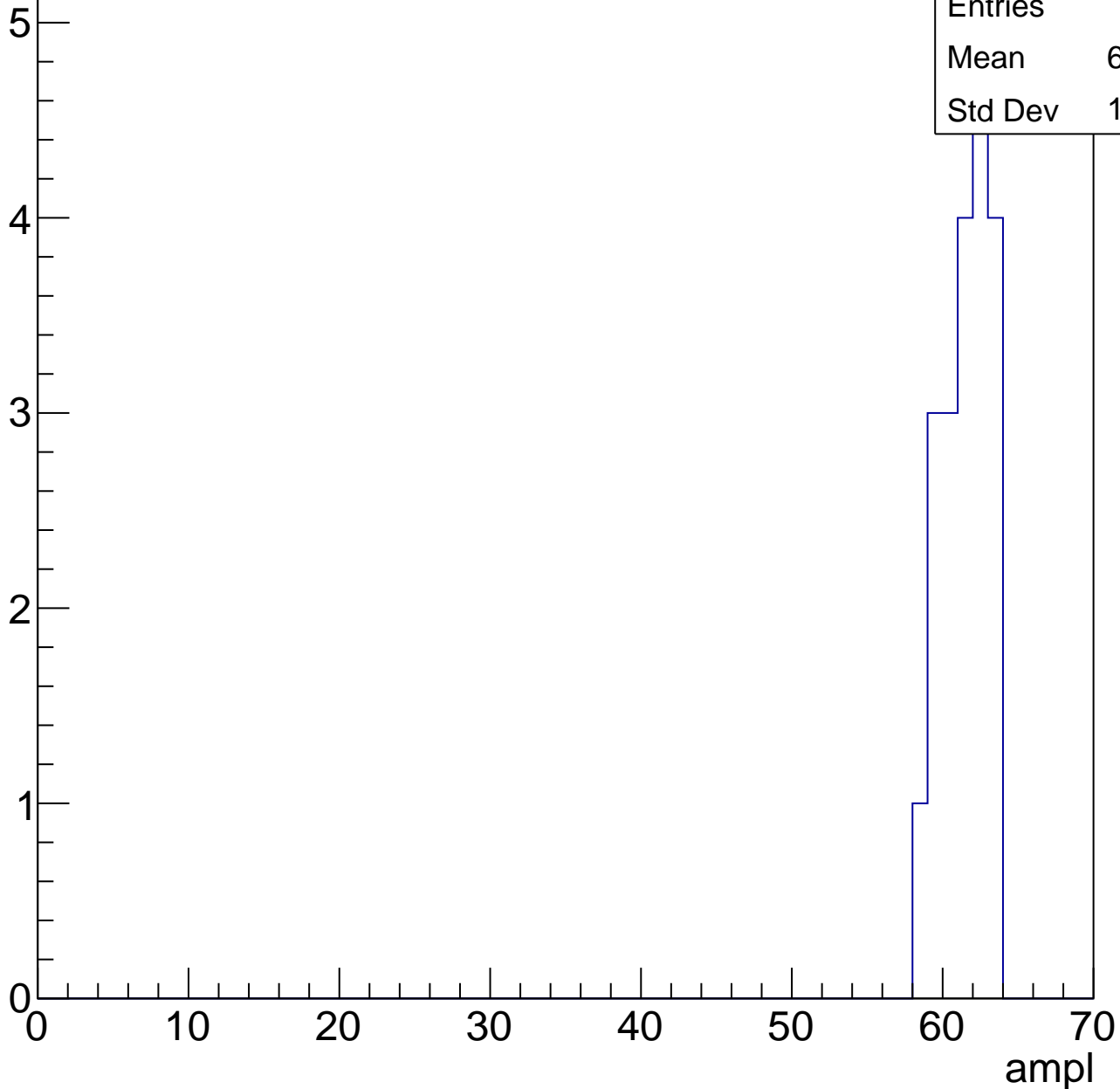


# B1L103S, U4-ch122, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 20    |
| Mean    | 61.05 |
| Std Dev | 1.499 |

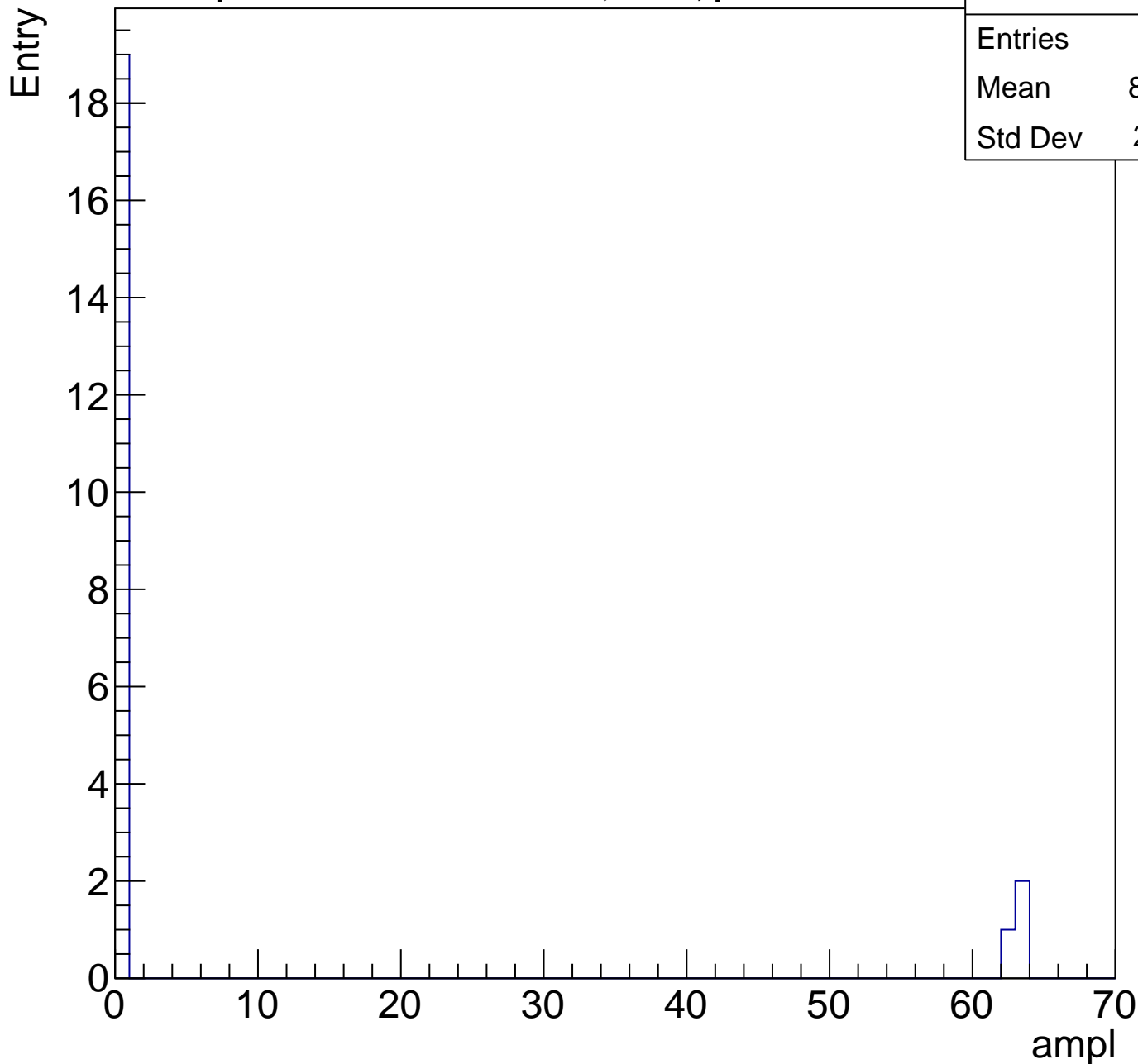




# B1L103S, U4-ch122, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

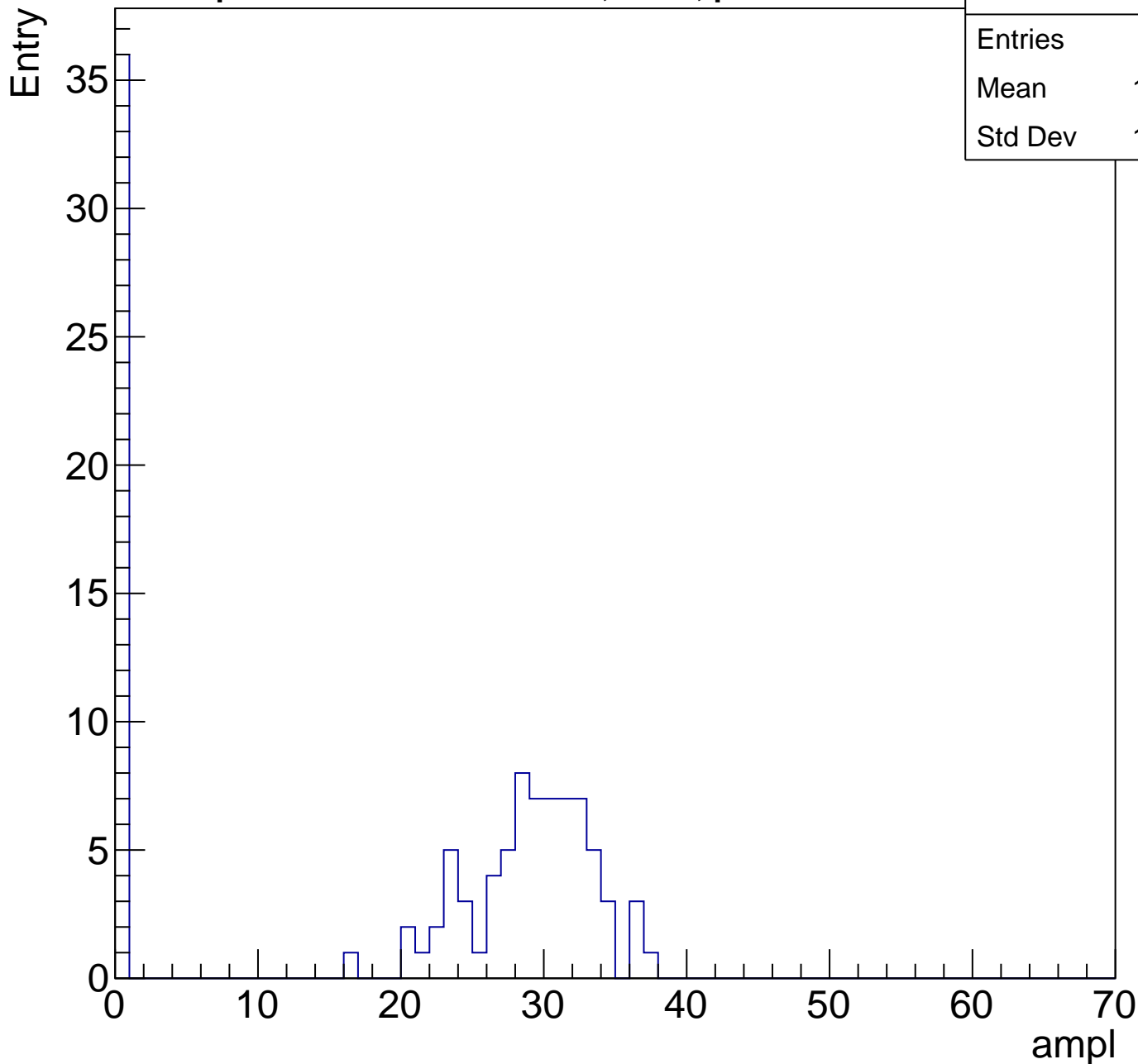
|         |       |
|---------|-------|
| Entries | 22    |
| Mean    | 8.545 |
| Std Dev | 21.51 |



# B1L103S, U4-ch123, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 108   |
| Mean    | 19.09 |
| Std Dev | 13.93 |

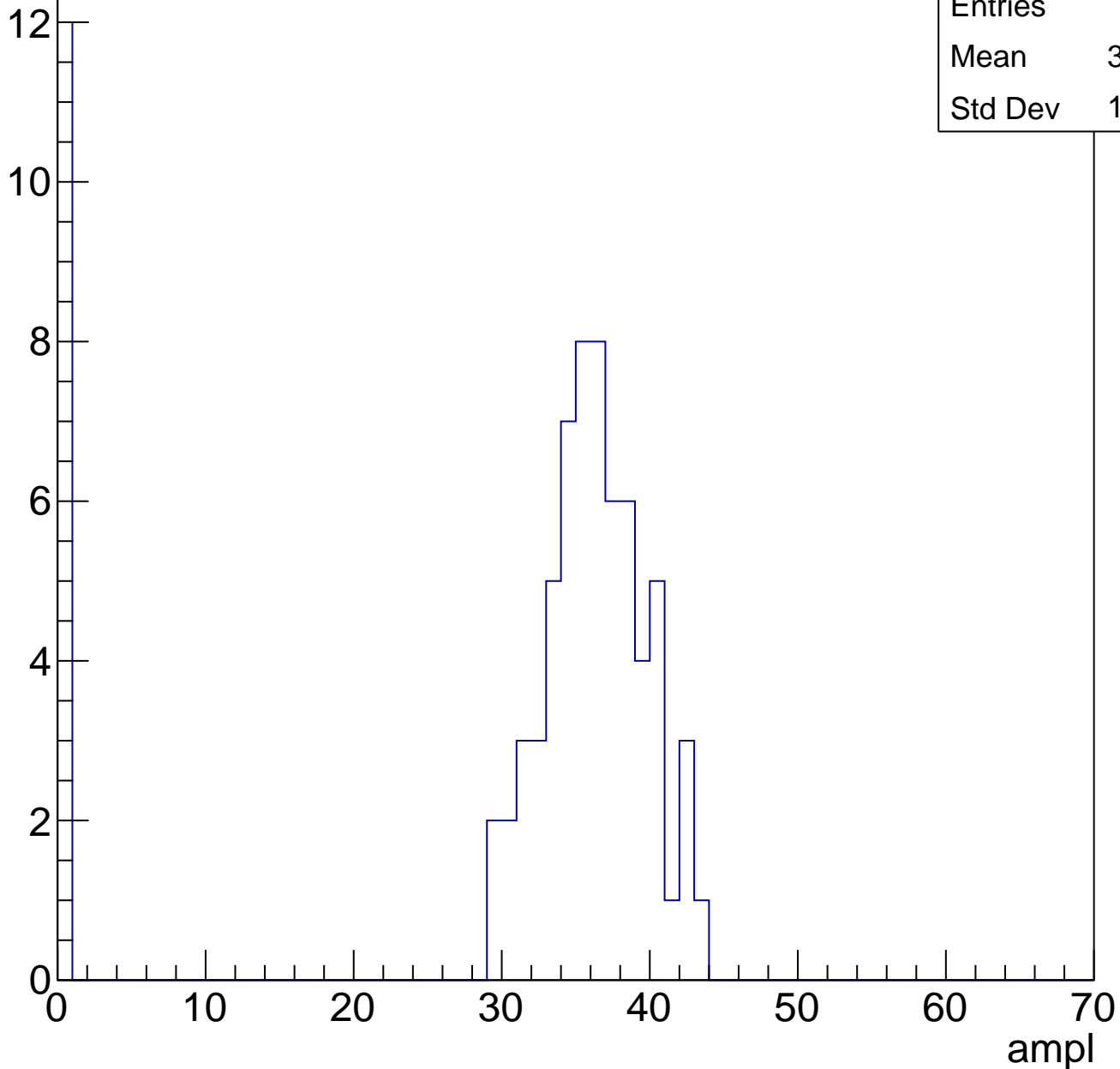


# B1L103S, U4-ch123, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 76    |
| Mean    | 30.18 |
| Std Dev | 13.42 |

Entry

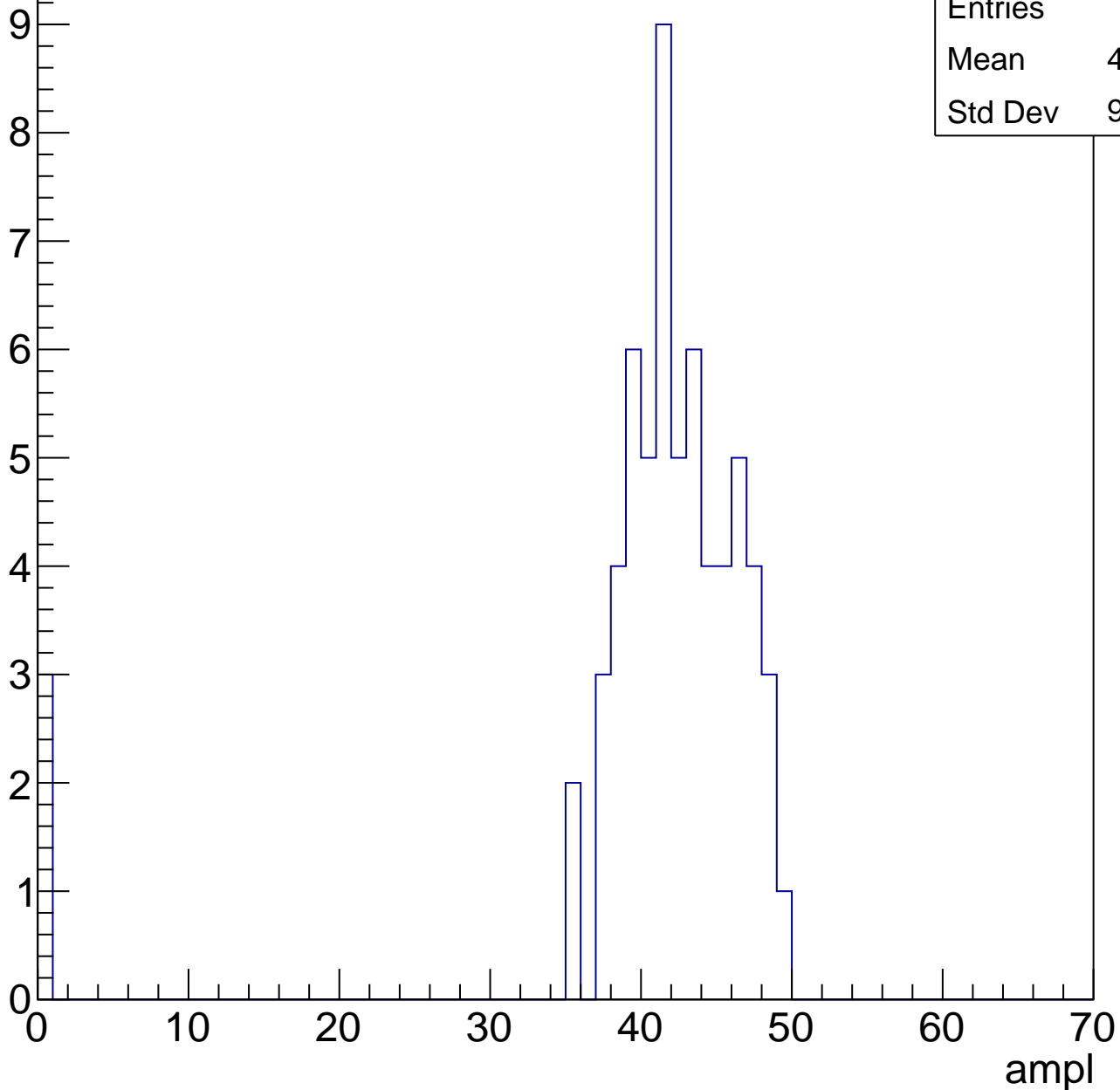


# B1L103S, U4-ch123, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

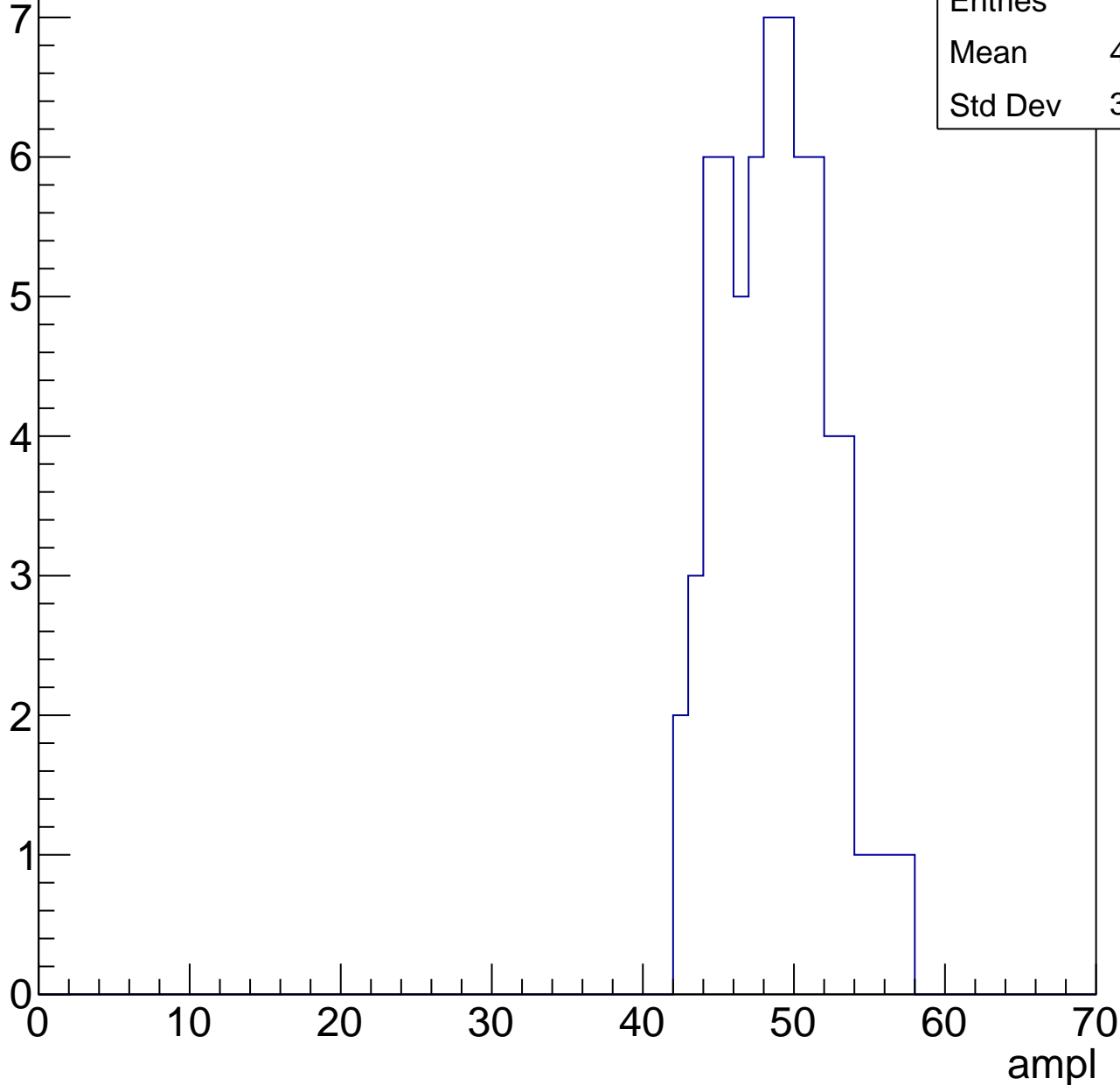
|         |       |
|---------|-------|
| Entries | 64    |
| Mean    | 40.17 |
| Std Dev | 9.514 |



# B1L103S, U4-ch123, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



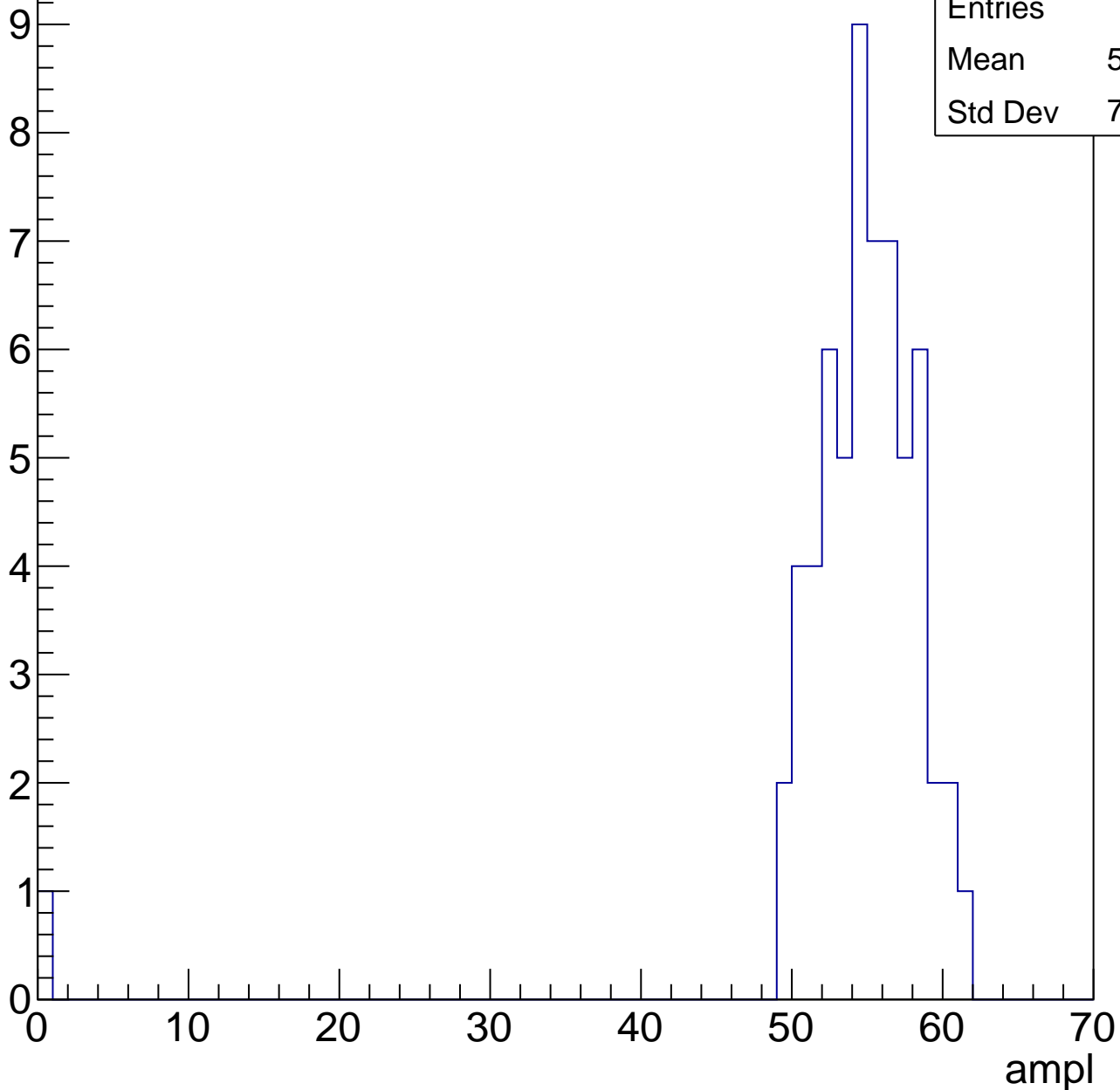
|         |       |
|---------|-------|
| Entries | 66    |
| Mean    | 48.27 |
| Std Dev | 3.475 |

# B1L103S, U4-ch123, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 61    |
| Mean    | 53.67 |
| Std Dev | 7.505 |

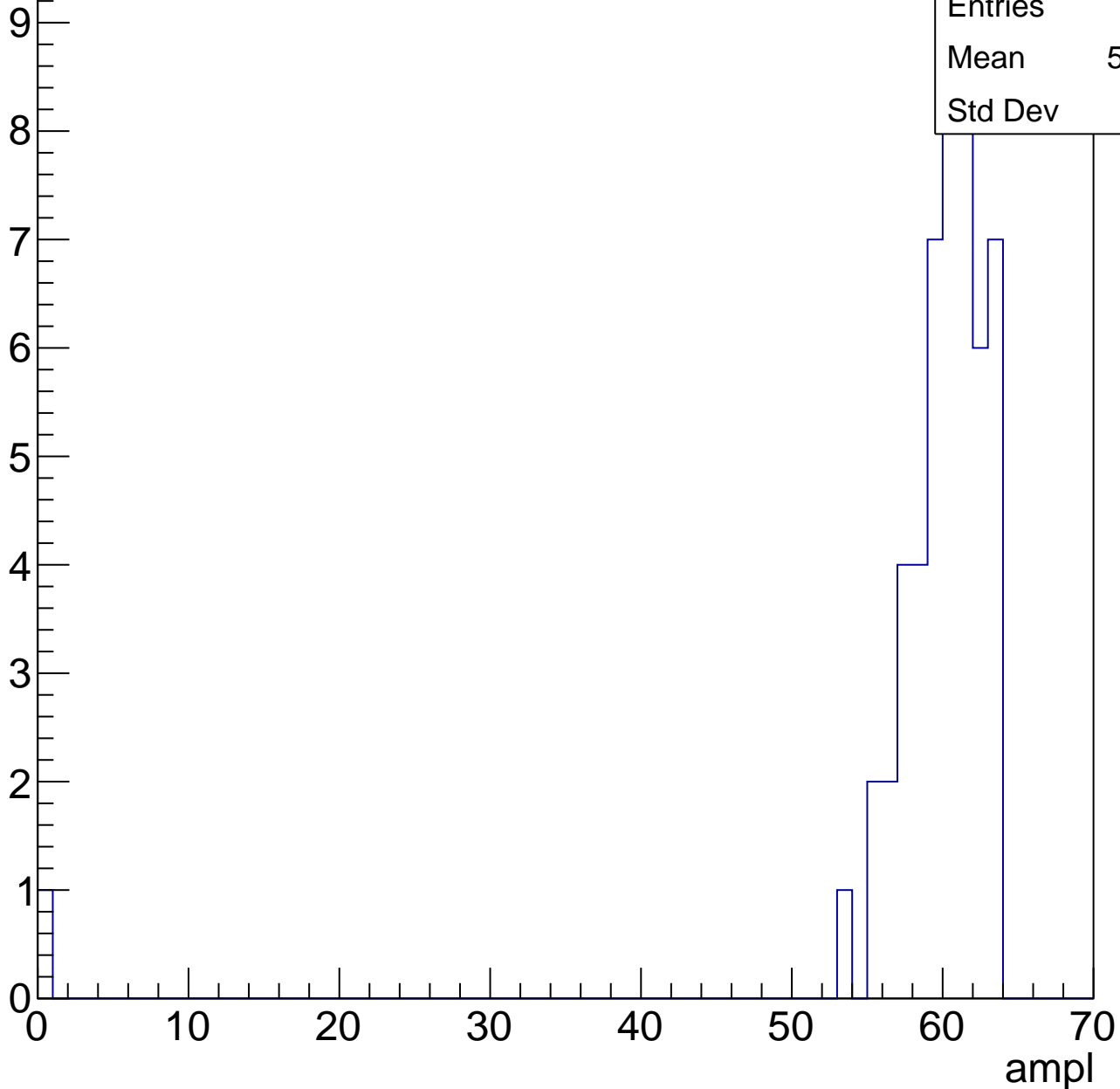


# B1L103S, U4-ch123, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

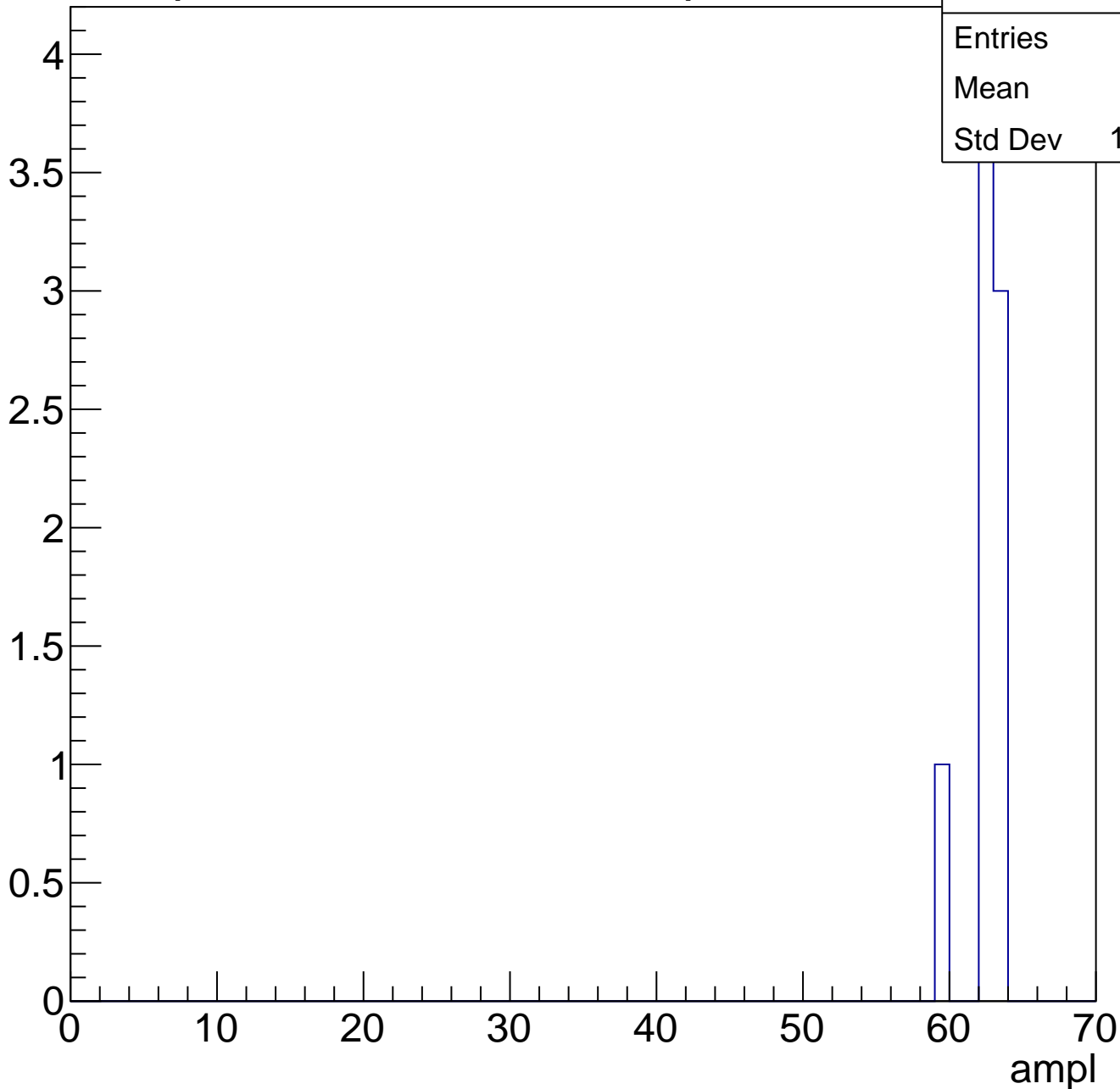
|         |       |
|---------|-------|
| Entries | 51    |
| Mean    | 58.63 |
| Std Dev | 8.62  |



# B1L103S, U4-ch123, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U4-ch123, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

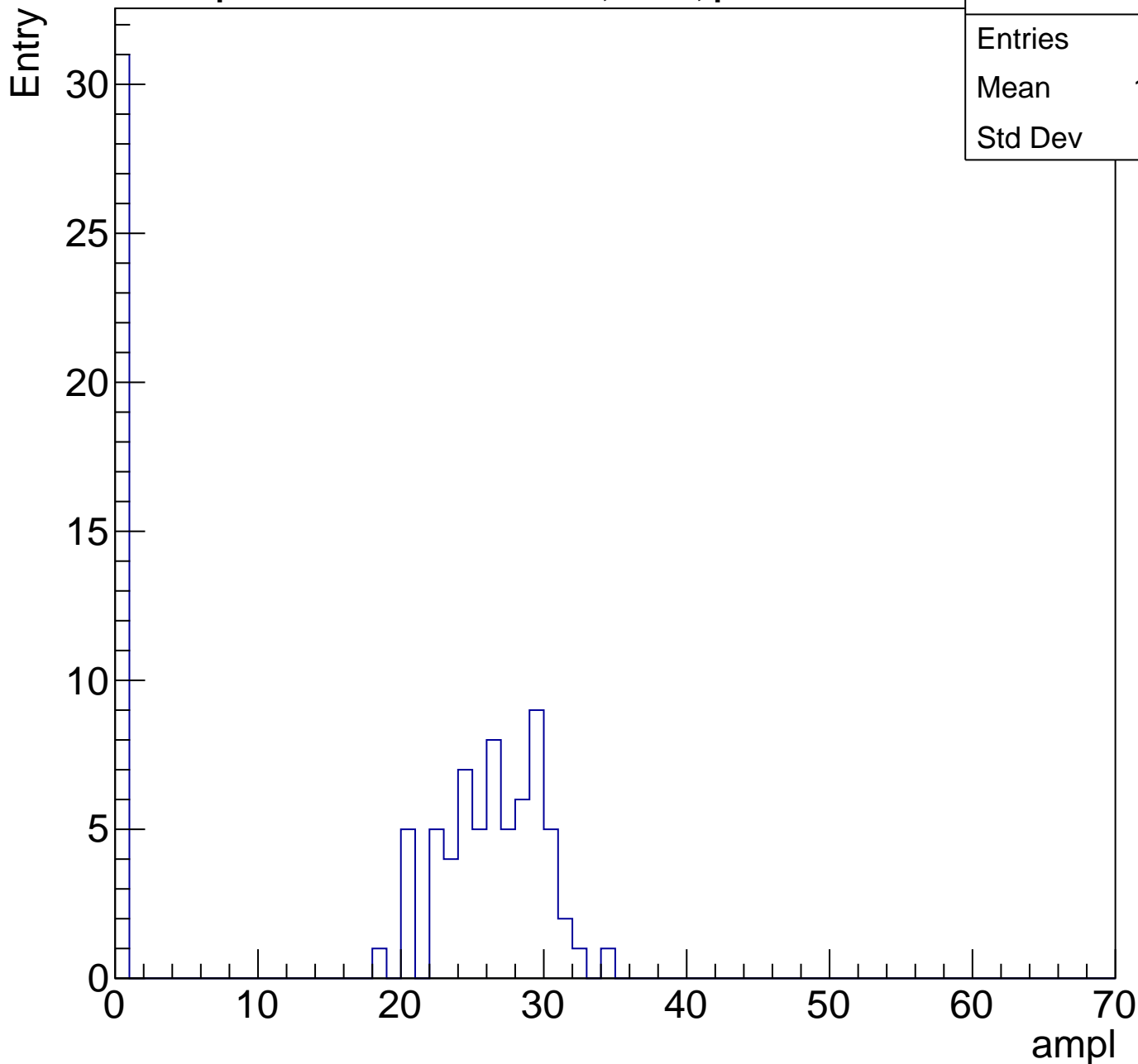
Entry



# B1L103S, U4-ch124, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

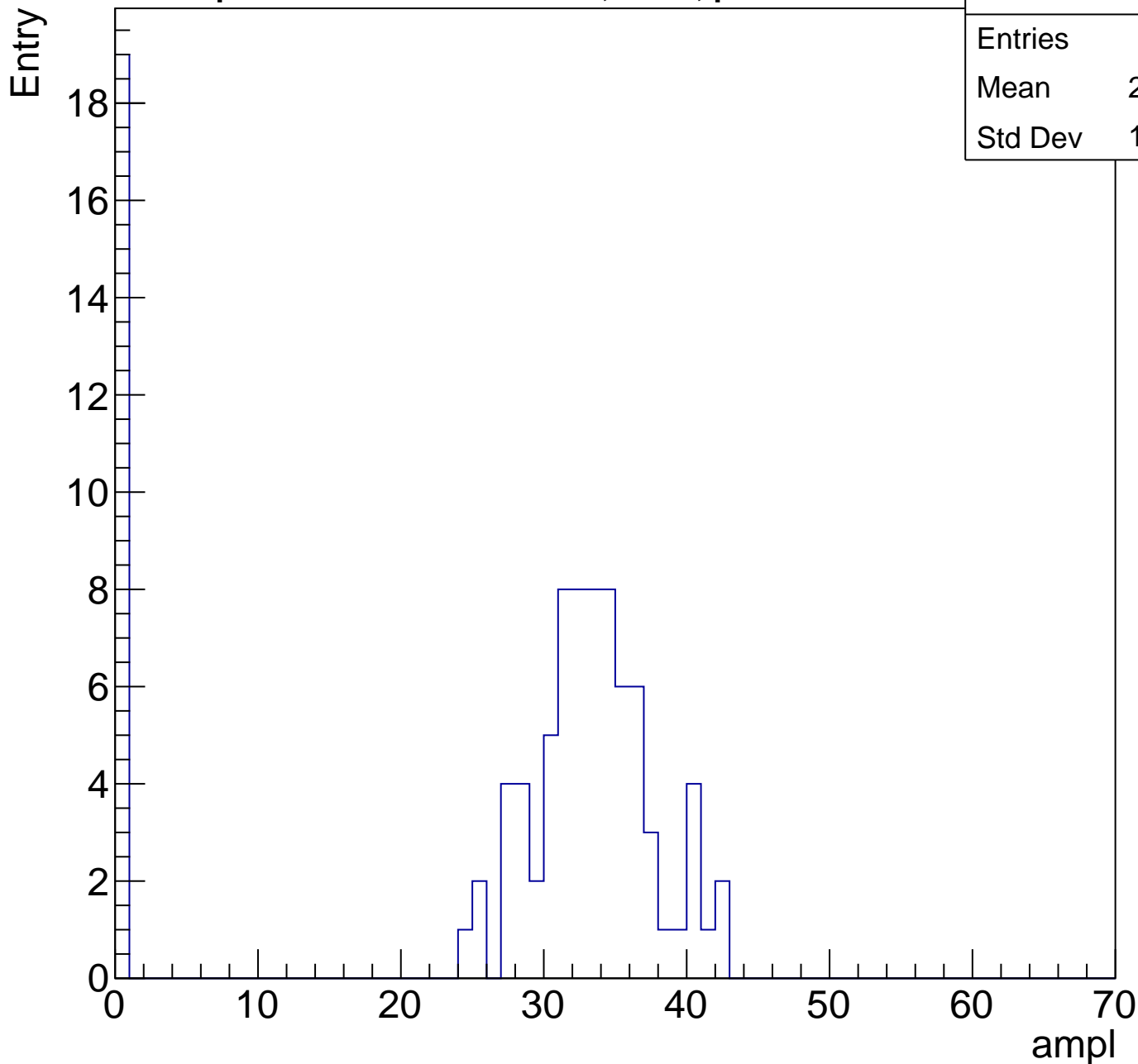
|         |       |
|---------|-------|
| Entries | 95    |
| Mean    | 17.51 |
| Std Dev | 12.5  |



# B1L103S, U4-ch124, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 93    |
| Mean    | 26.25 |
| Std Dev | 13.77 |

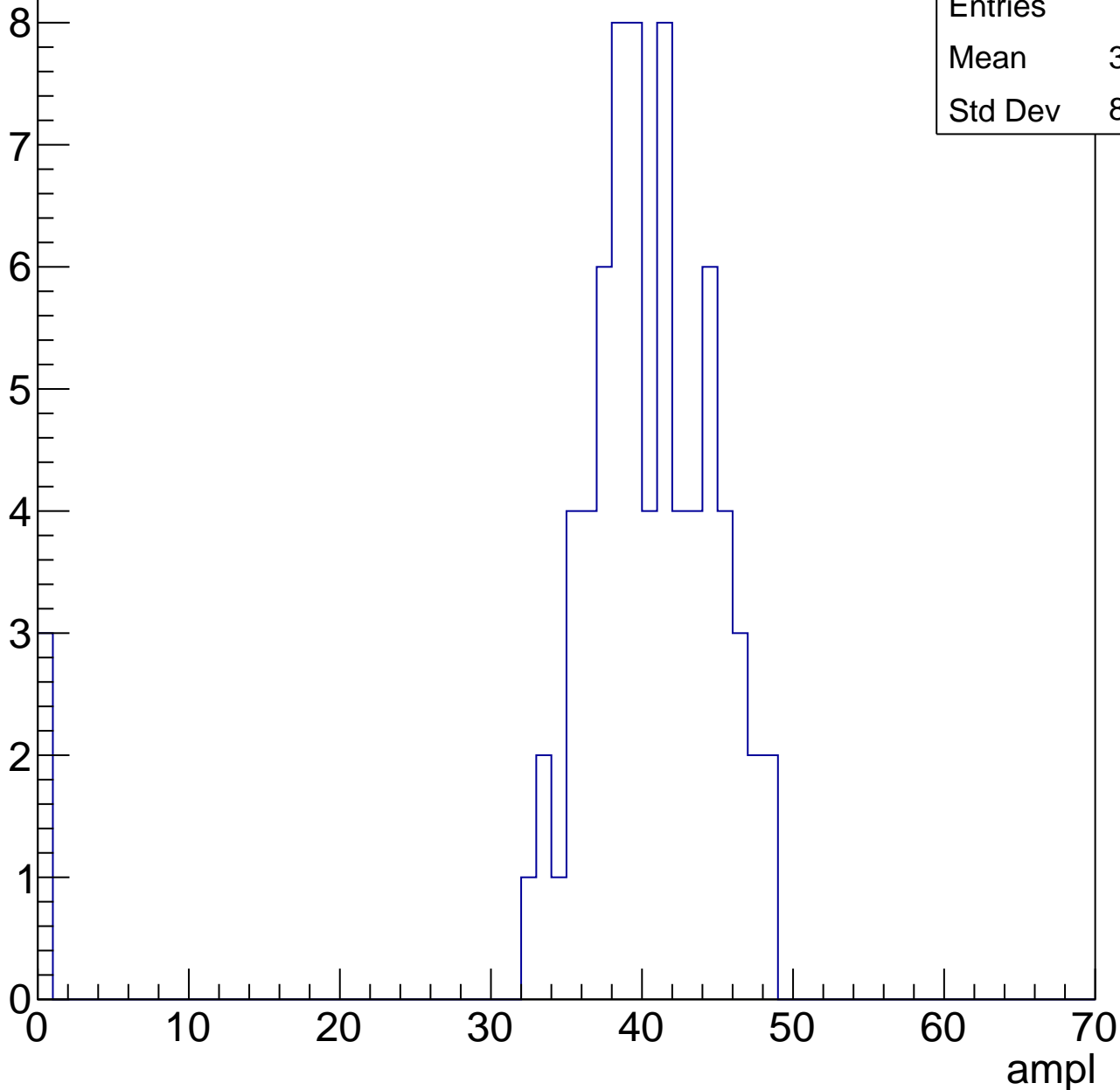


# B1L103S, U4-ch124, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 74    |
| Mean    | 38.57 |
| Std Dev | 8.772 |

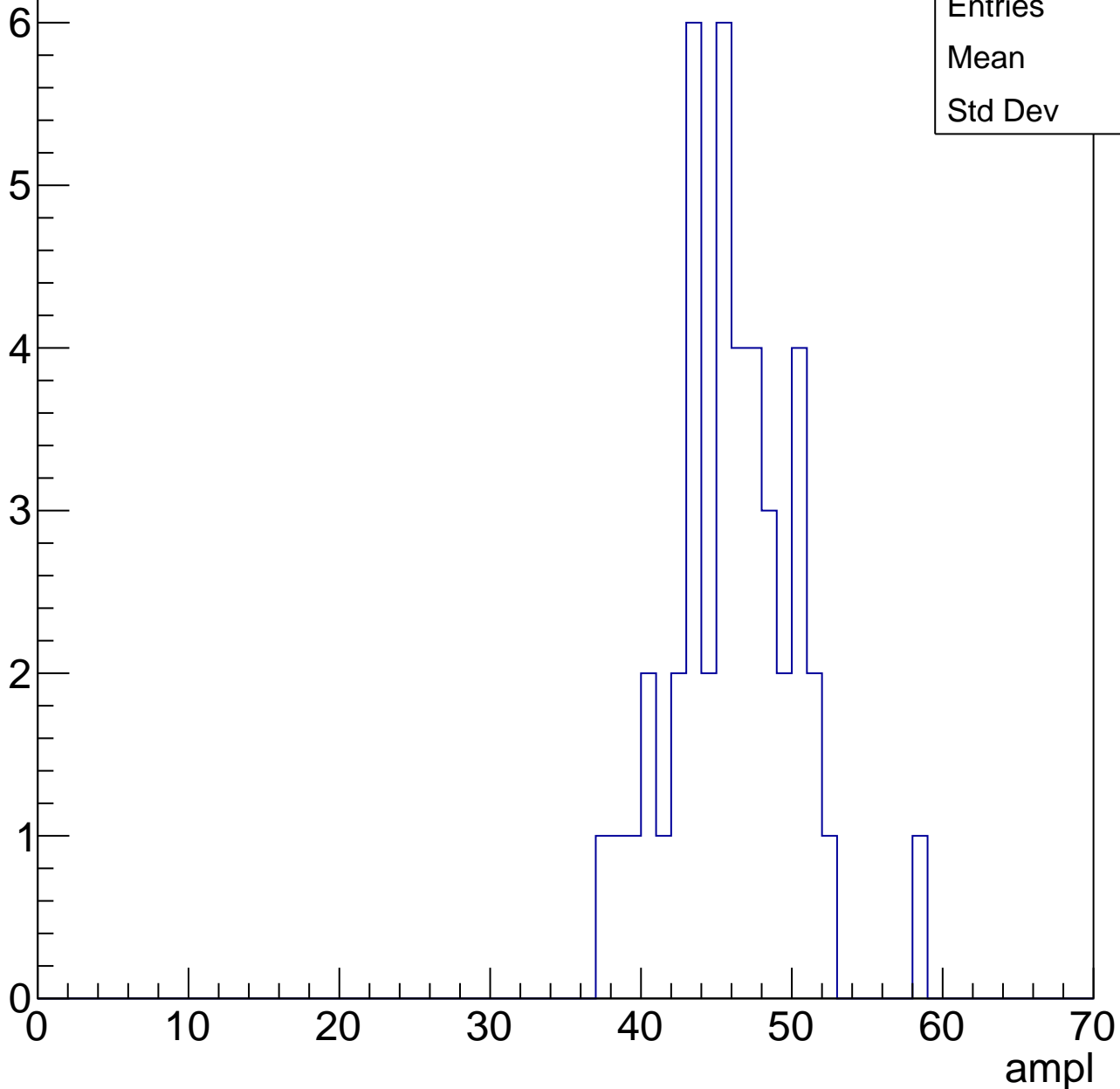


# B1L103S, U4-ch124, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |      |
|---------|------|
| Entries | 43   |
| Mean    | 45.6 |
| Std Dev | 4.07 |

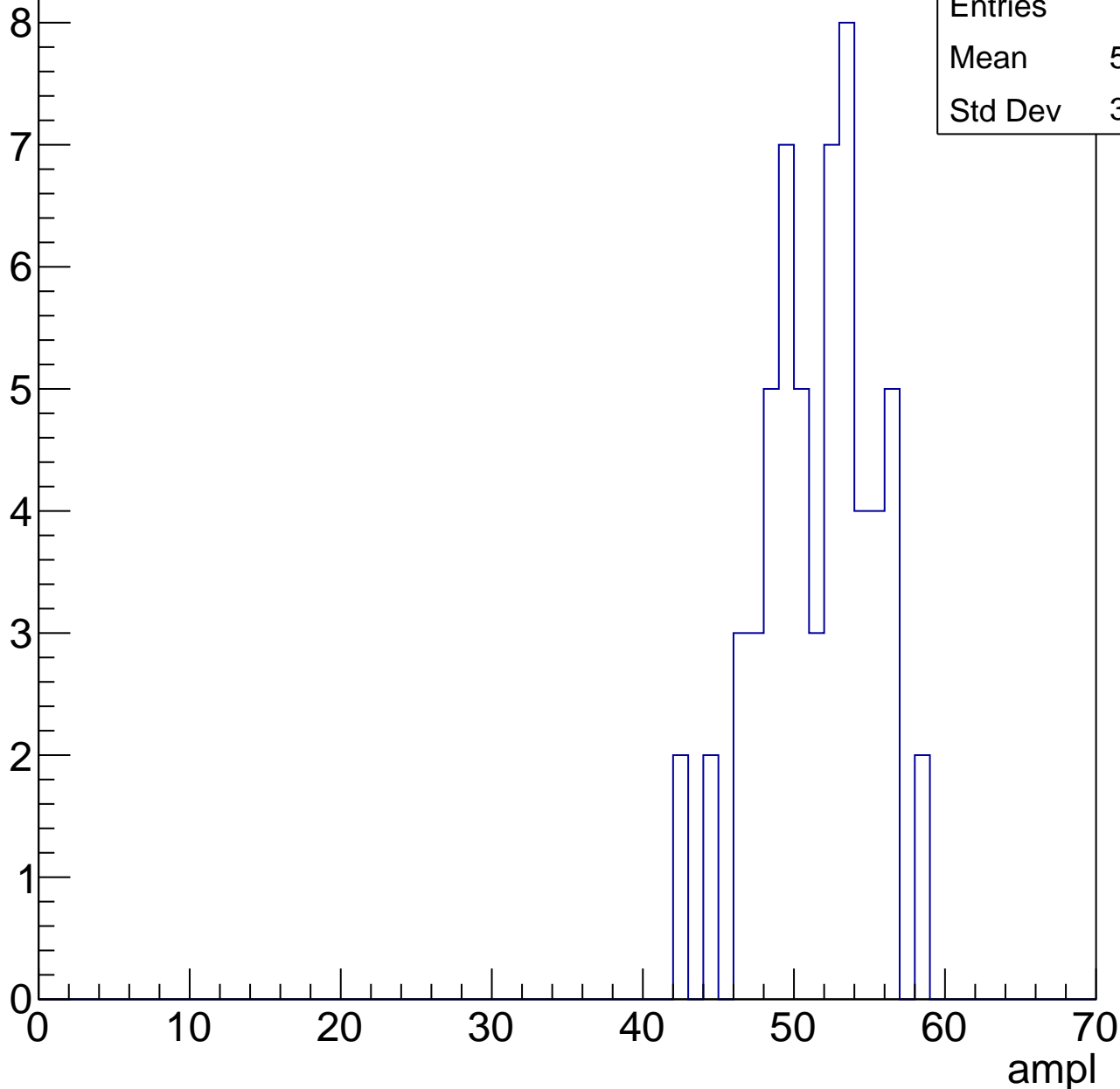


# B1L103S, U4-ch124, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 60    |
| Mean    | 50.95 |
| Std Dev | 3.703 |

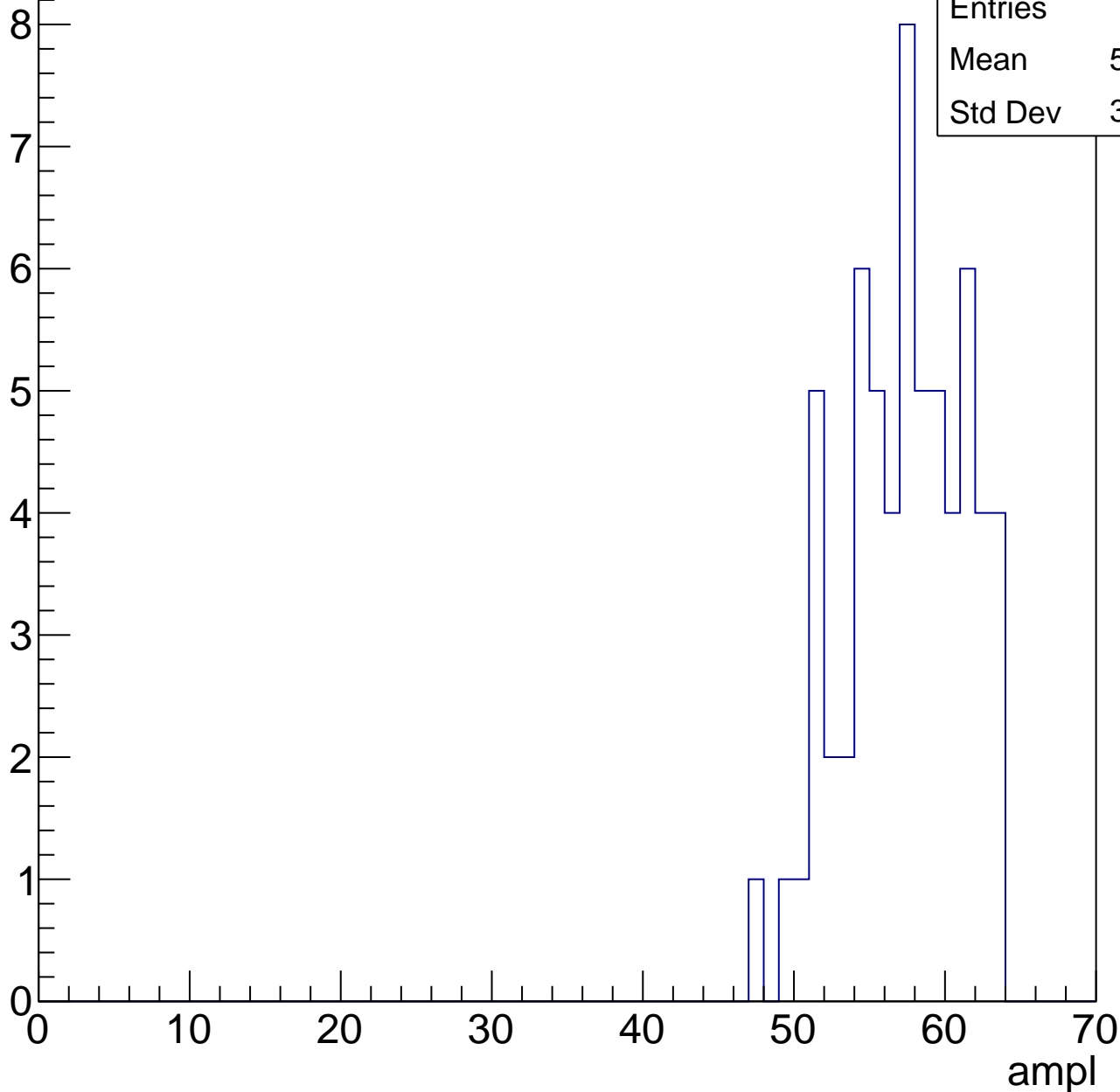


# B1L103S, U4-ch124, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

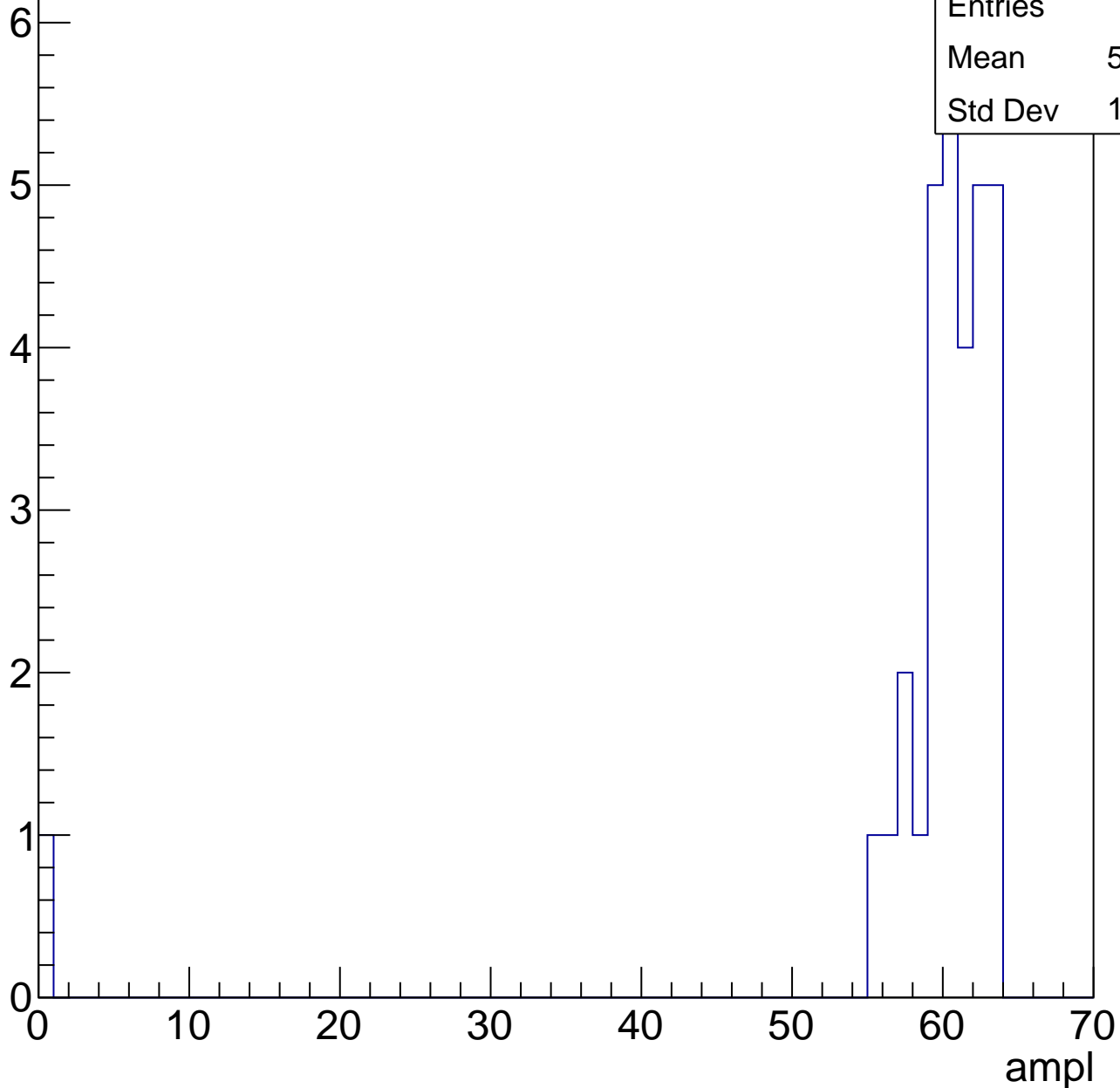
|         |       |
|---------|-------|
| Entries | 63    |
| Mean    | 56.84 |
| Std Dev | 3.888 |



# B1L103S, U4-ch124, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



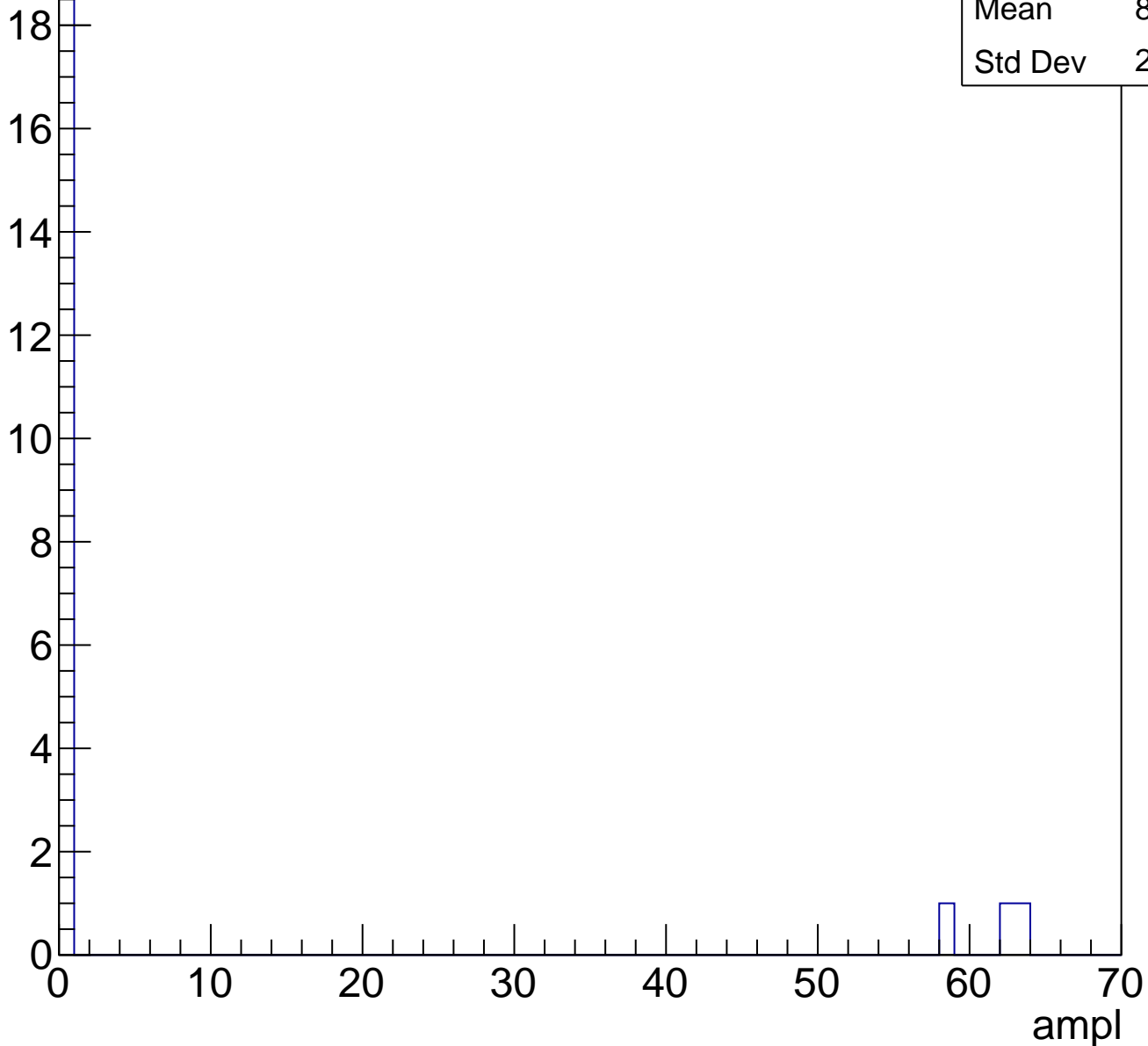


# B1L103S, U4-ch124, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 22    |
| Mean    | 8.318 |
| Std Dev | 20.95 |

Entry

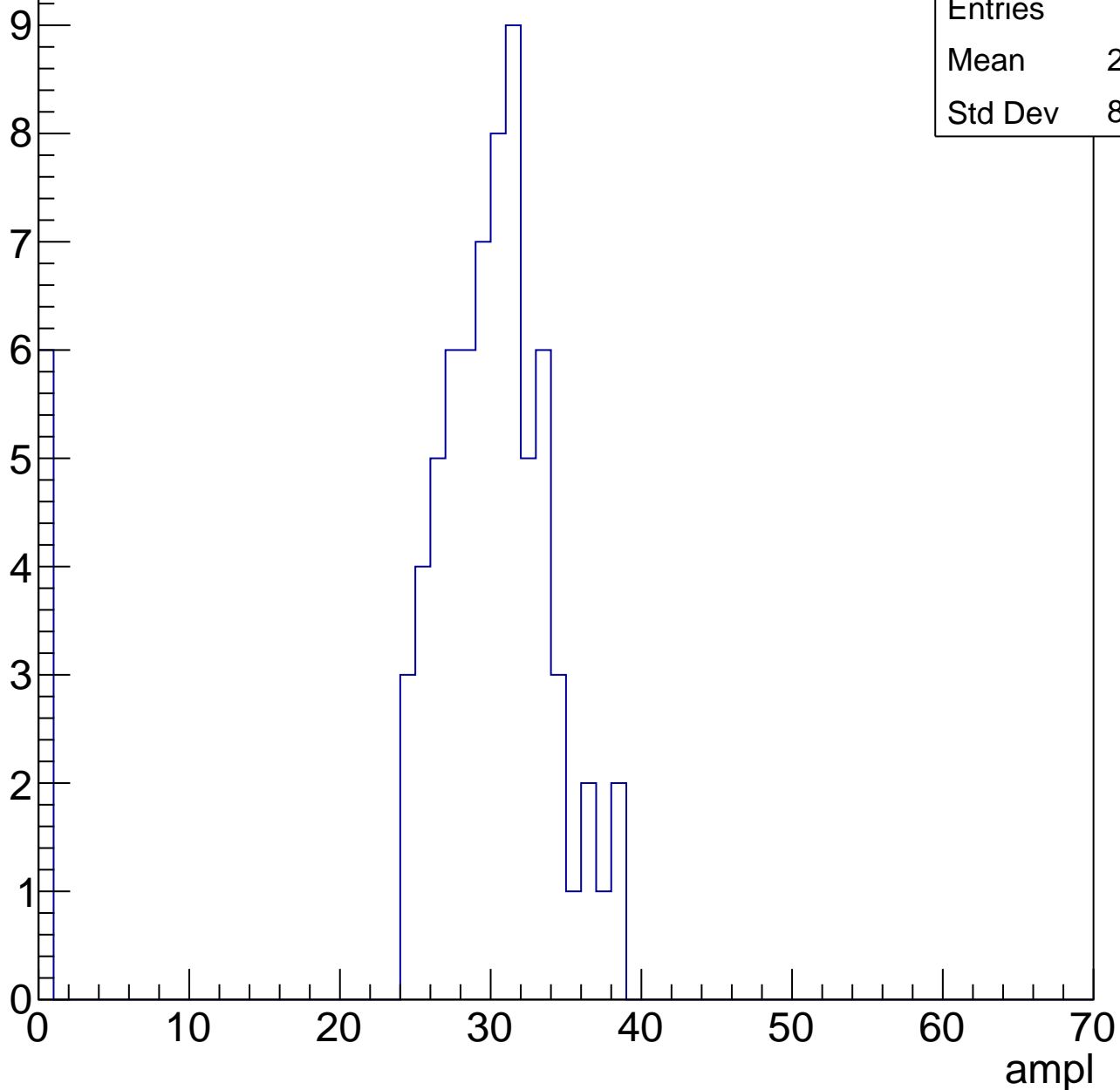


# B1L103S, U4-ch125, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 74    |
| Mean    | 27.49 |
| Std Dev | 8.785 |

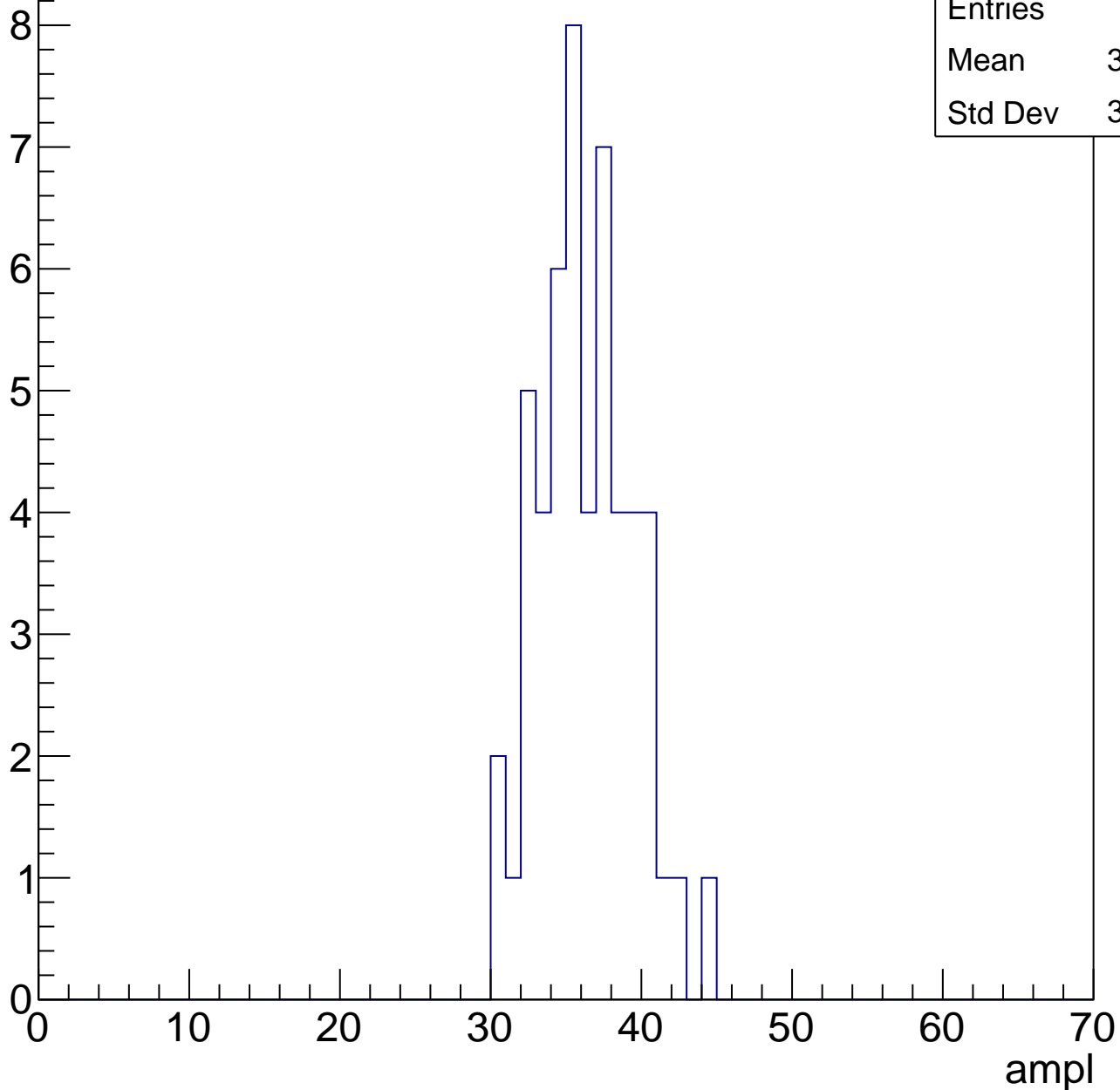


# B1L103S, U4-ch125, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 52    |
| Mean    | 35.87 |
| Std Dev | 3.076 |

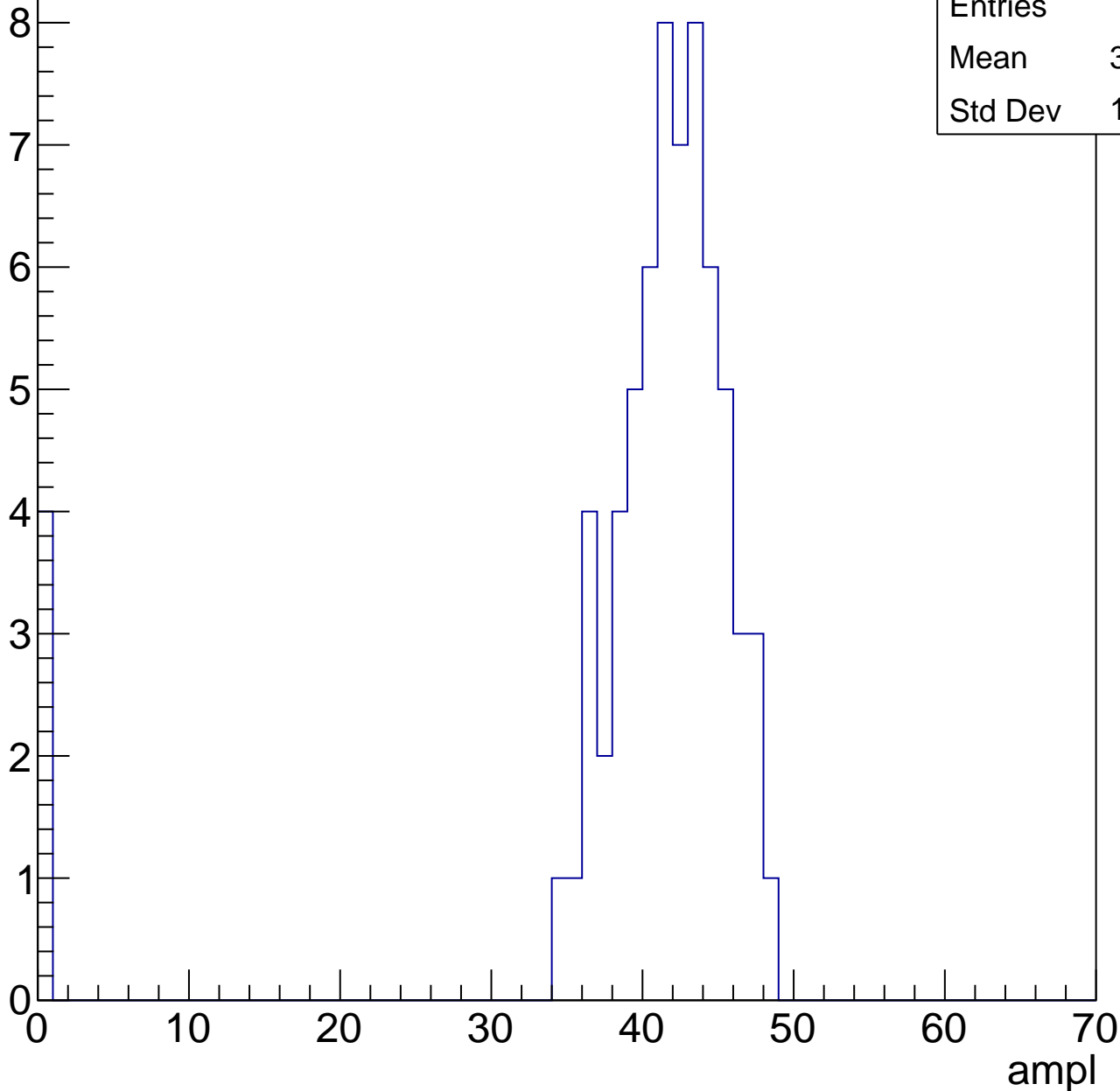


# B1L103S, U4-ch125, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 68    |
| Mean    | 39.06 |
| Std Dev | 10.26 |

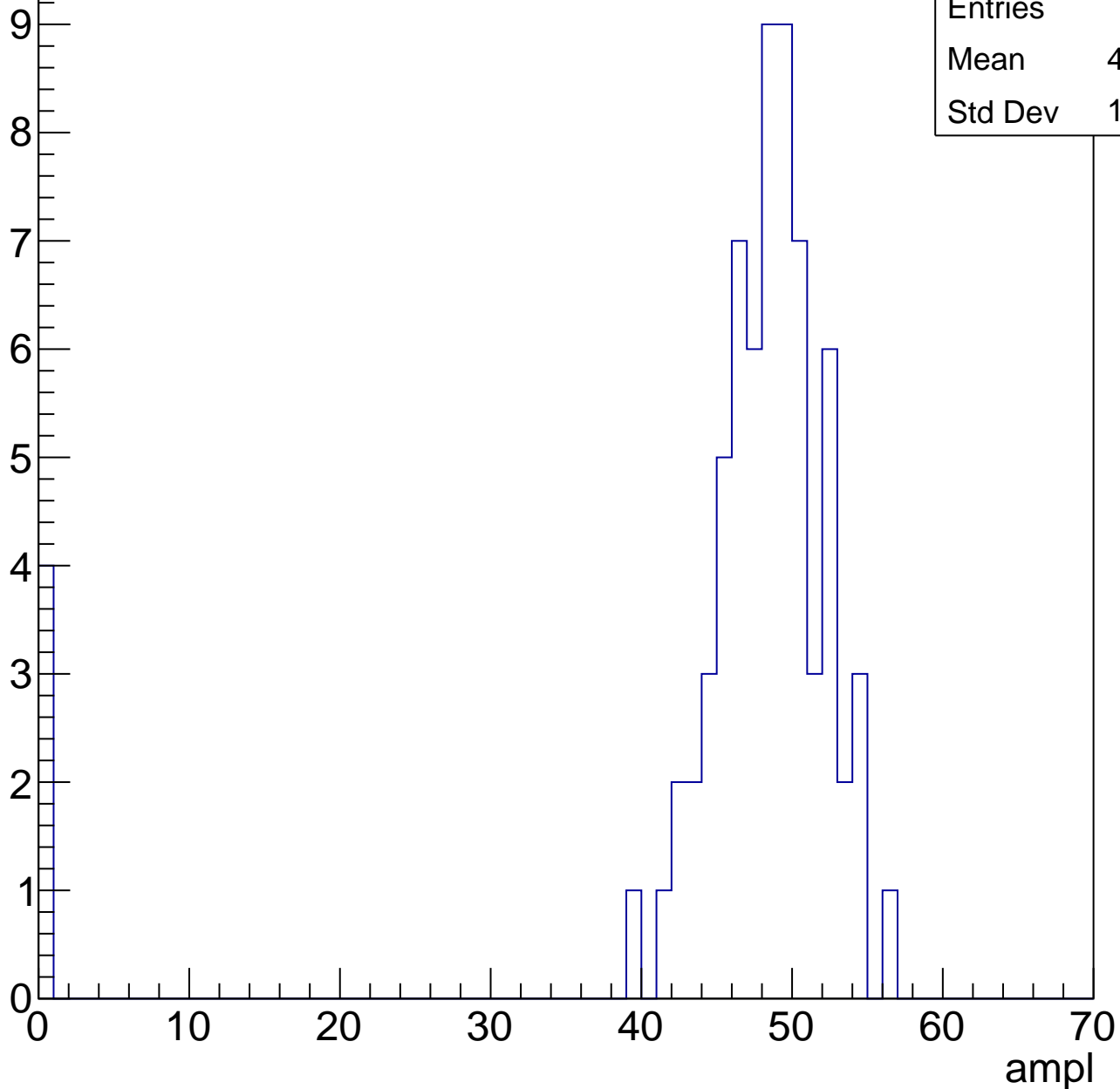


# B1L103S, U4-ch125, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 71    |
| Mean    | 45.39 |
| Std Dev | 11.56 |

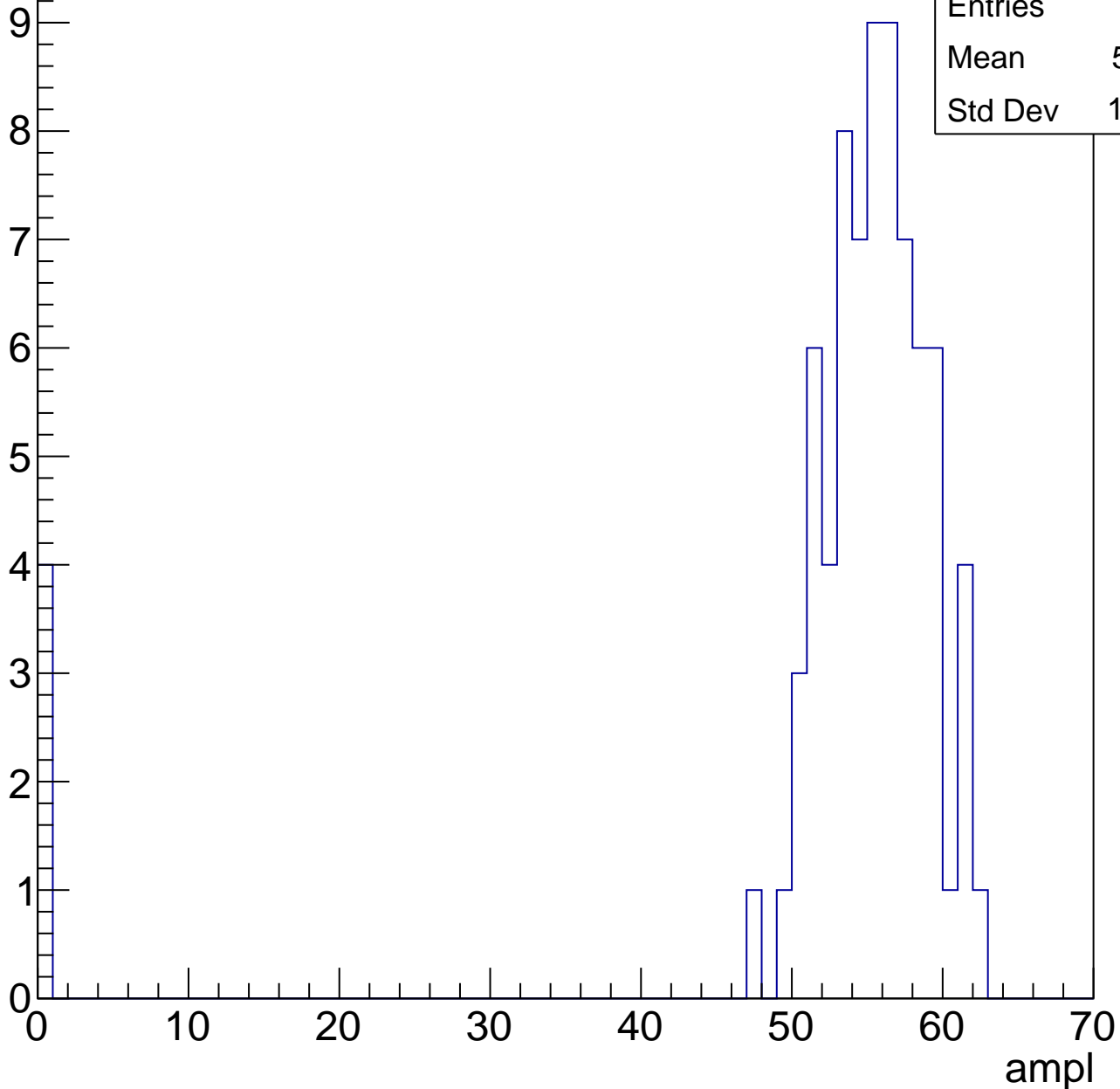


# B1L103S, U4-ch125, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 77    |
| Mean    | 52.31 |
| Std Dev | 12.64 |

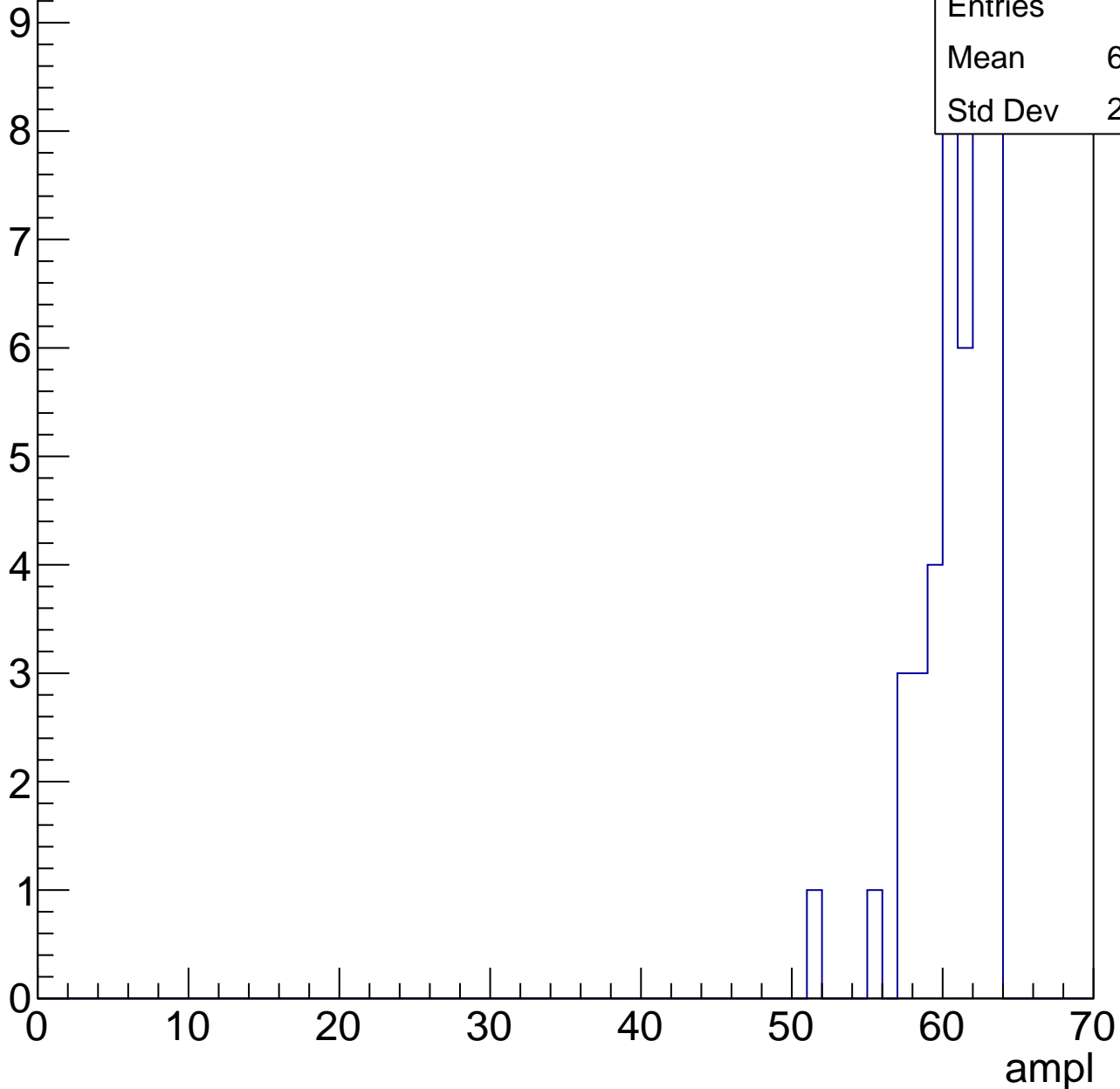


# B1L103S, U4-ch125, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

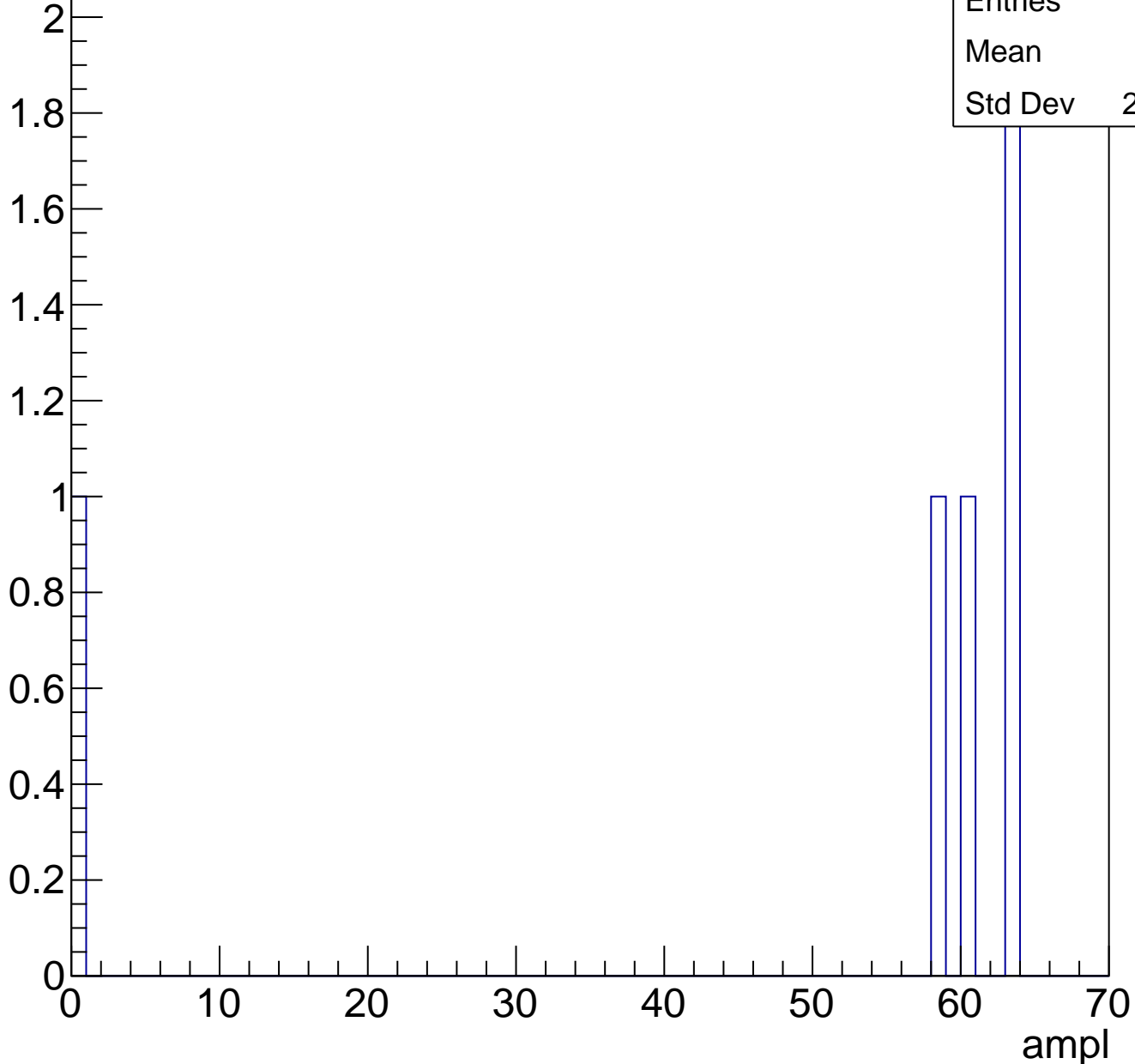
|         |       |
|---------|-------|
| Entries | 43    |
| Mean    | 60.35 |
| Std Dev | 2.448 |



# B1L103S, U4-ch125, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



|         |       |
|---------|-------|
| Entries | 5     |
| Mean    | 48.8  |
| Std Dev | 24.47 |



# B1L103S, U4-ch125, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 18    |
| Mean    | 1.167 |
| Std Dev | 4.81  |

Entry

16  
14  
12  
10  
8  
6  
4  
2  
0

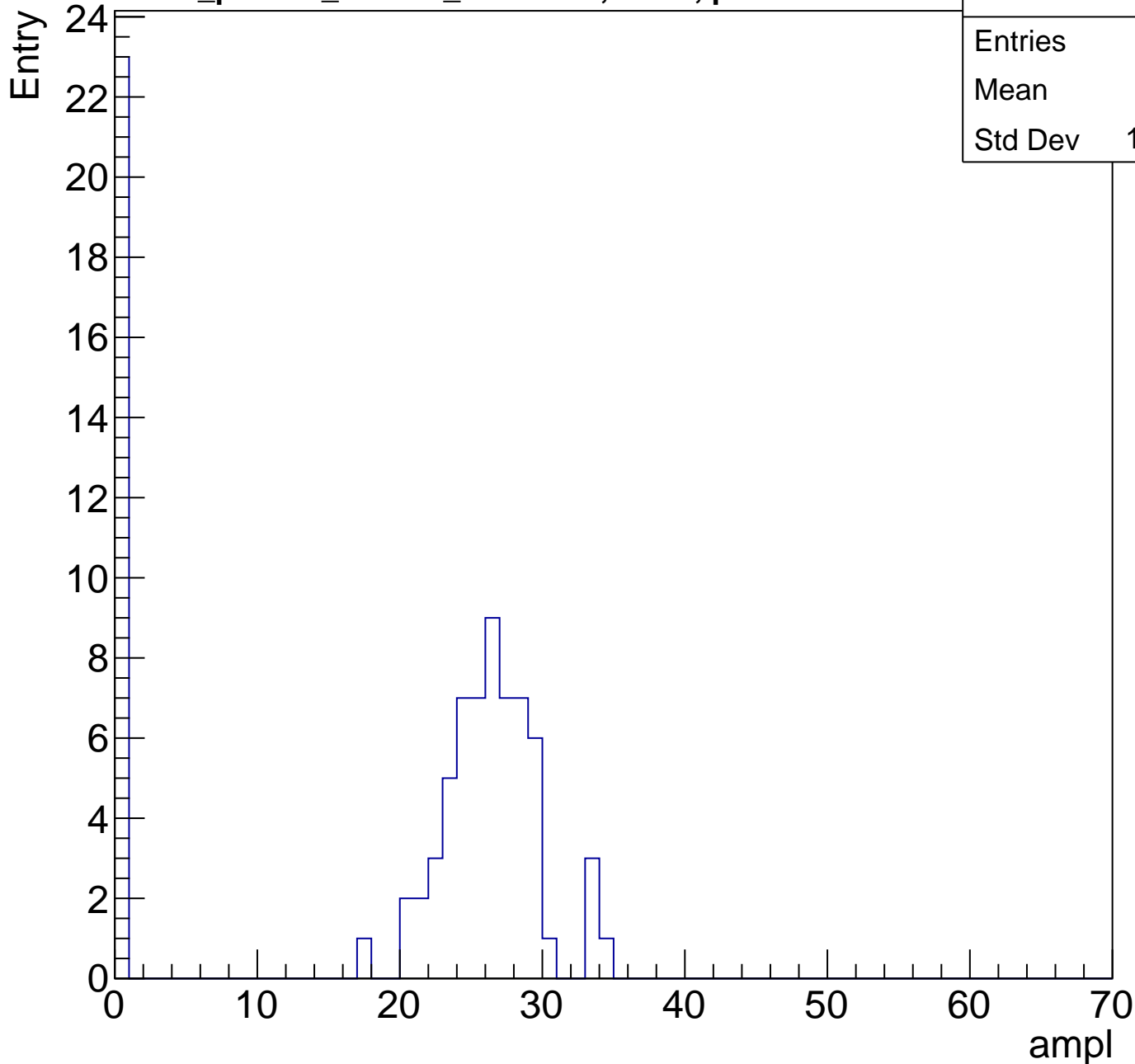
ampl

0 10 20 30 40 50 60 70

# B1L103S, U4-ch126, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 84    |
| Mean    | 18.8  |
| Std Dev | 11.87 |

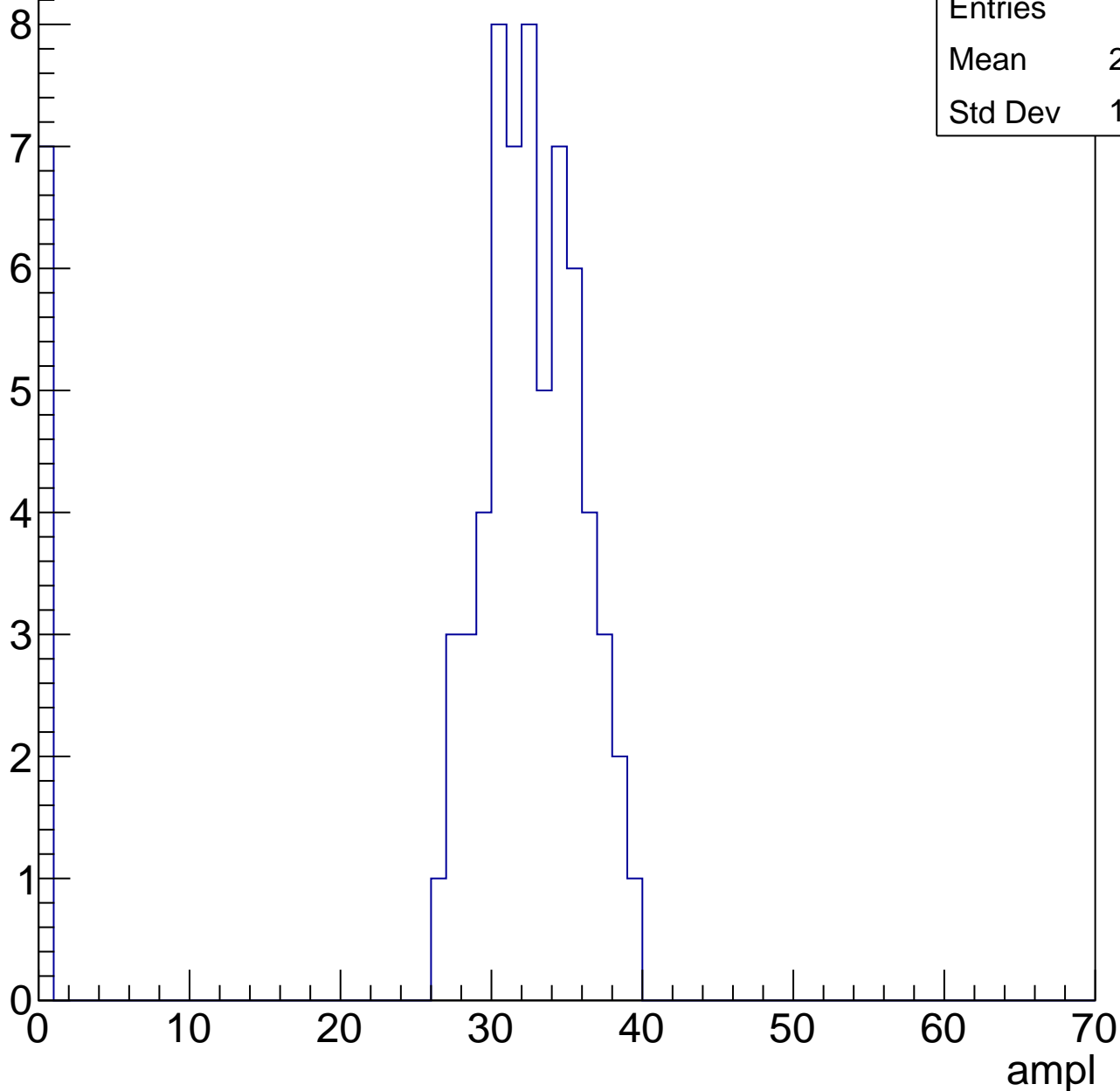


# B1L103S, U4-ch126, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 69    |
| Mean    | 29.03 |
| Std Dev | 10.17 |



# B1L103S, U4-ch126, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

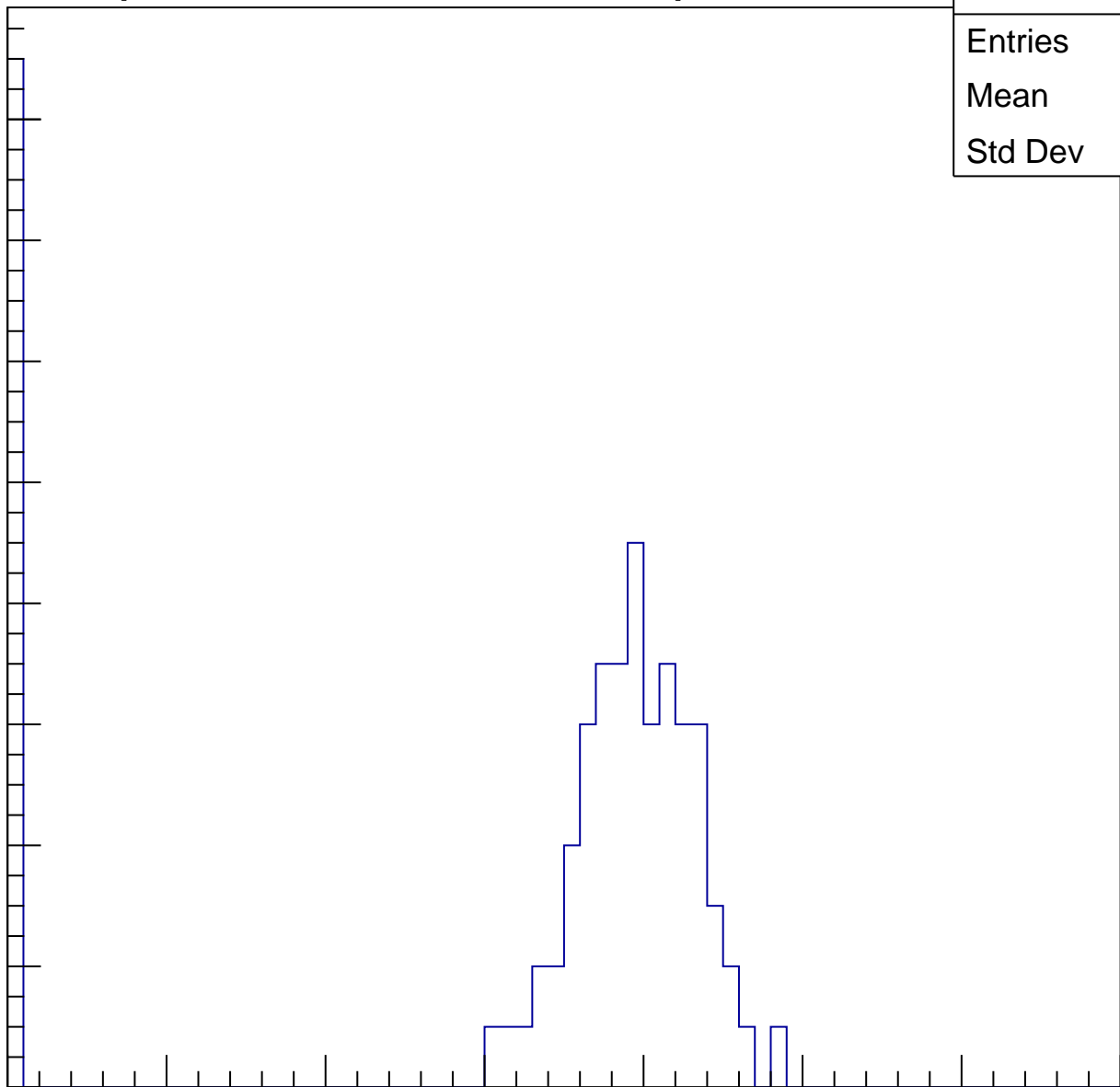
|         |       |
|---------|-------|
| Entries | 89    |
| Mean    | 31.6  |
| Std Dev | 15.69 |

Entry

16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

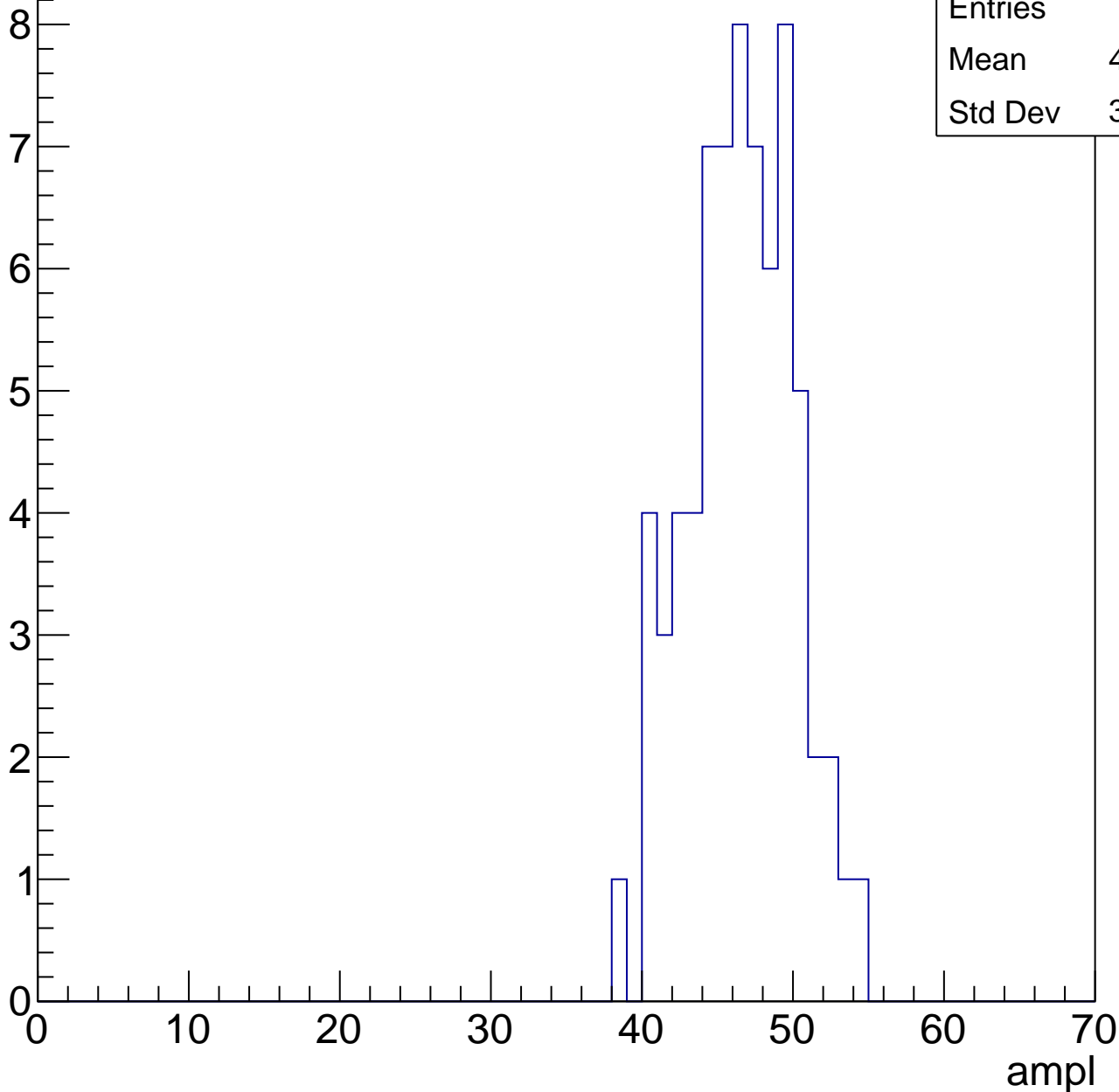


# B1L103S, U4-ch126, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

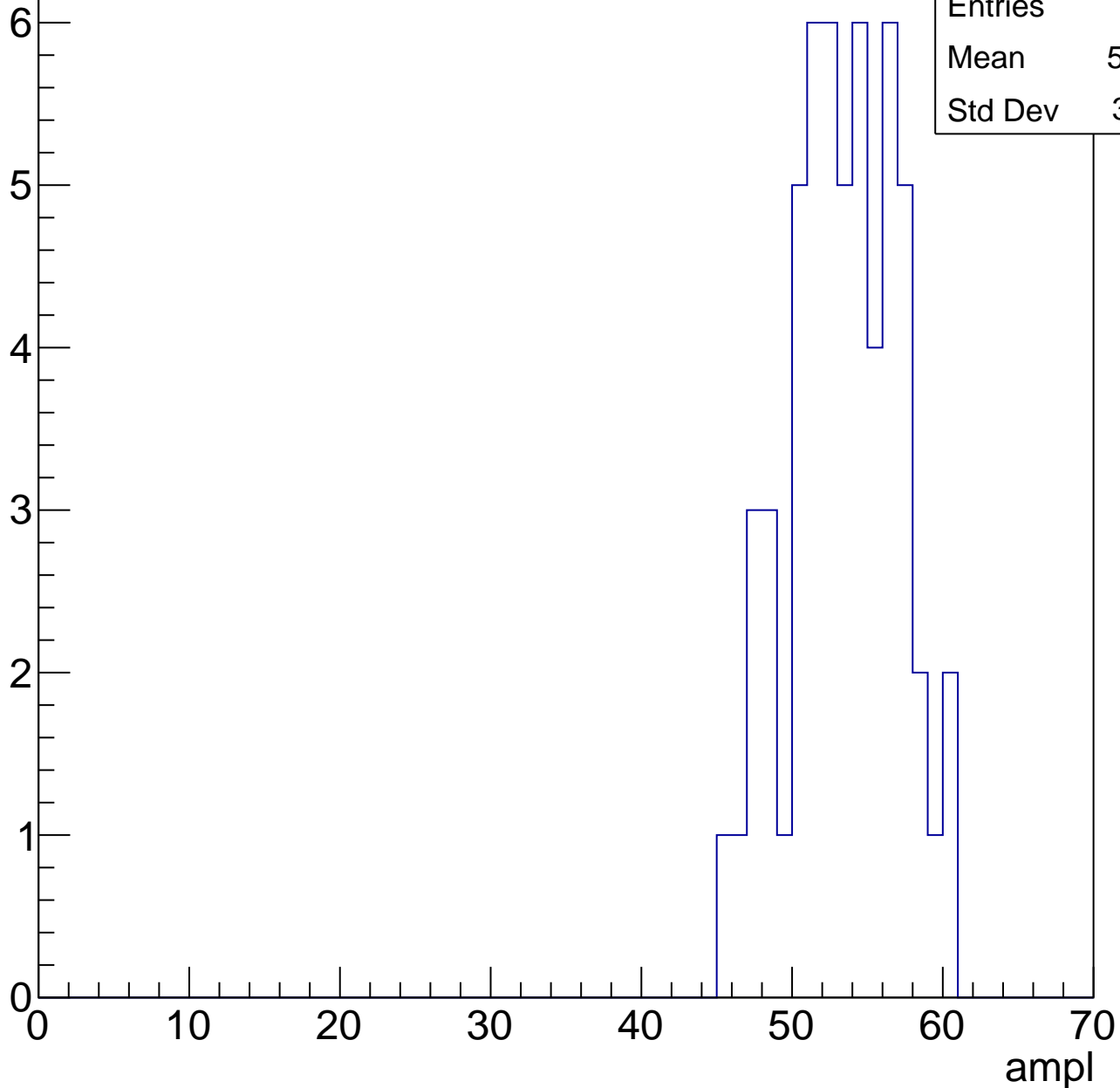
|         |       |
|---------|-------|
| Entries | 70    |
| Mean    | 46.06 |
| Std Dev | 3.455 |



# B1L103S, U4-ch126, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

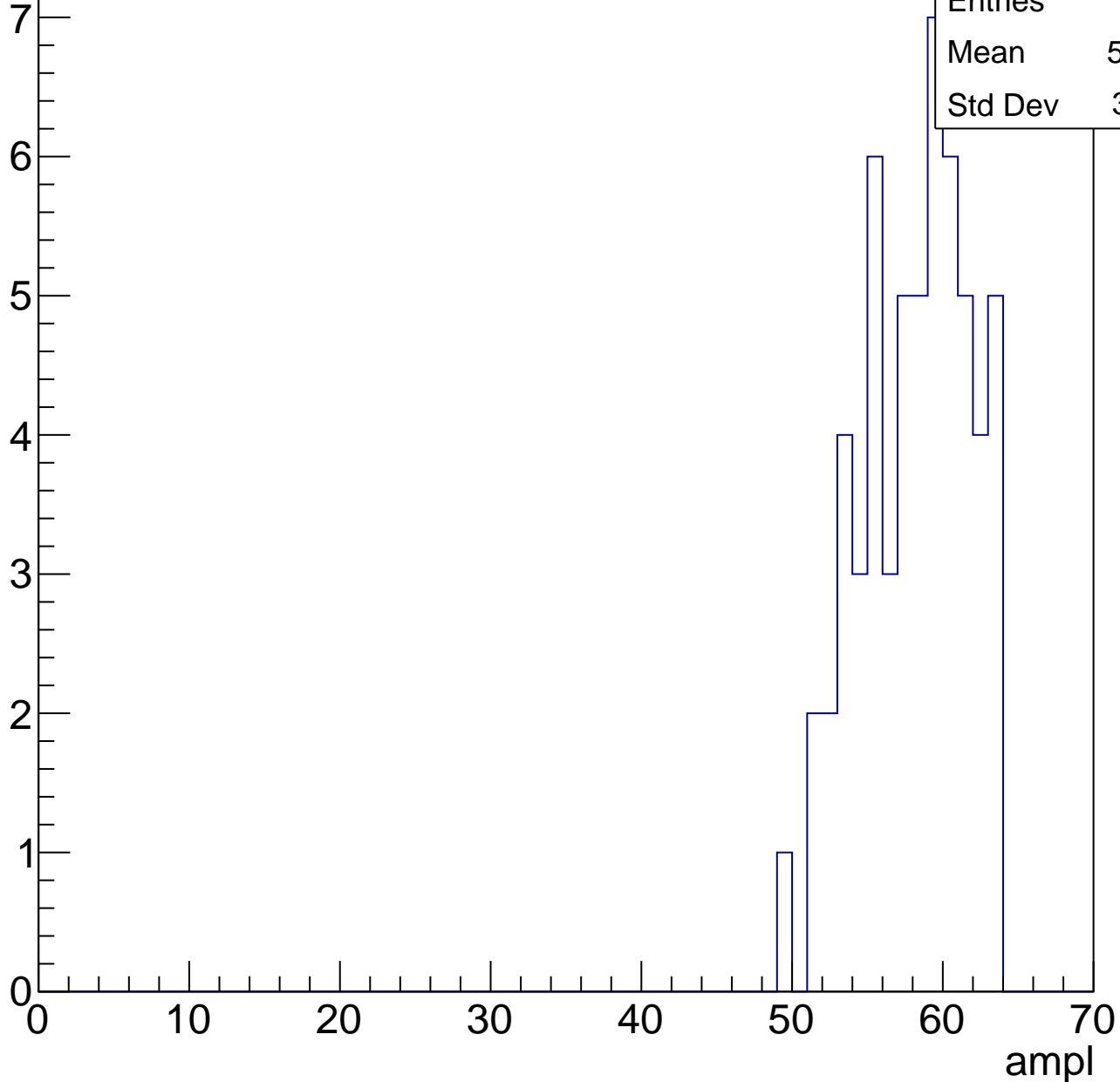


|         |       |
|---------|-------|
| Entries | 57    |
| Mean    | 52.95 |
| Std Dev | 3.571 |

# B1L103S, U4-ch126, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



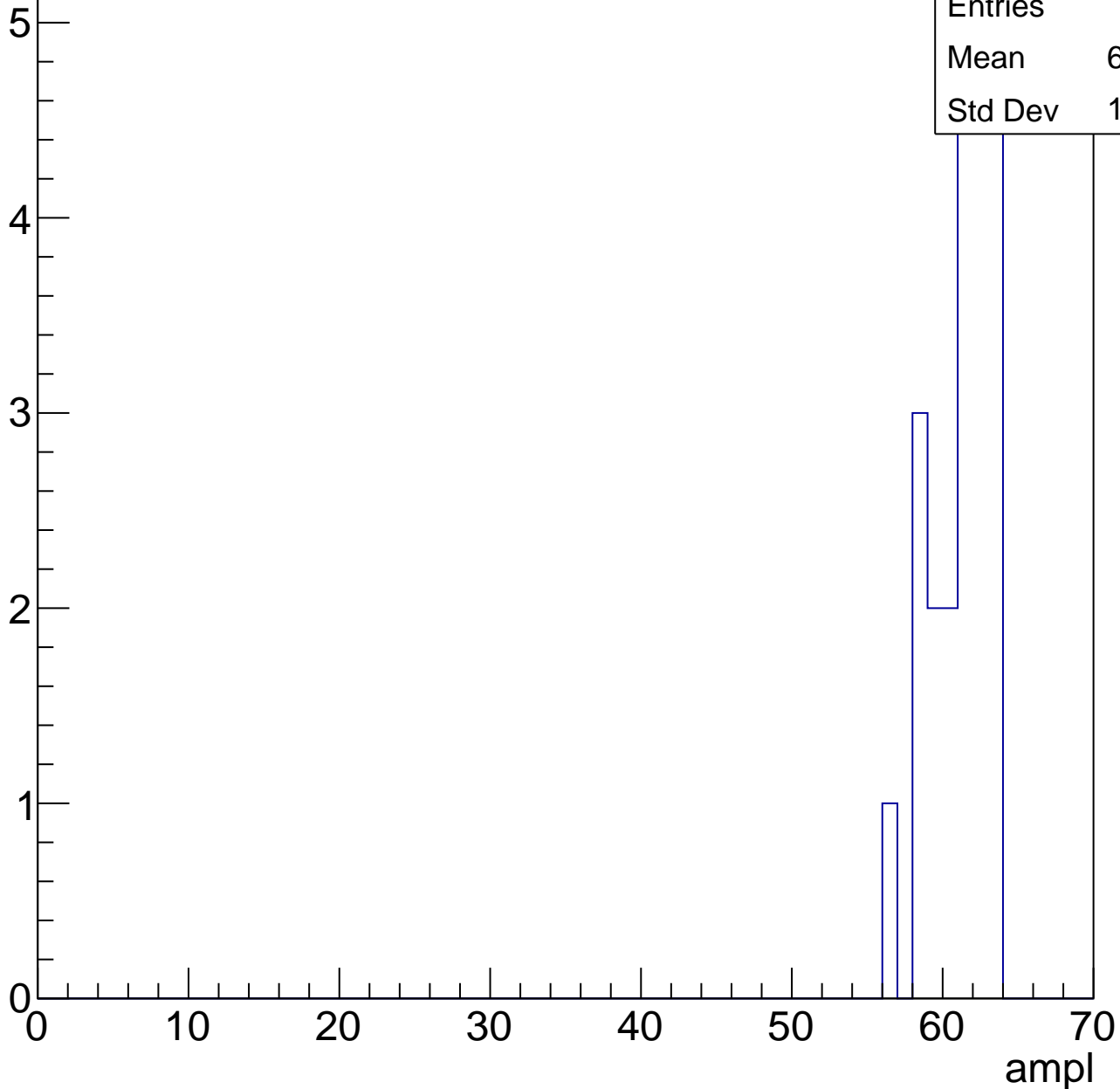
|         |       |
|---------|-------|
| Entries | 58    |
| Mean    | 57.64 |
| Std Dev | 3.541 |

# B1L103S, U4-ch126, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 23    |
| Mean    | 60.78 |
| Std Dev | 1.933 |

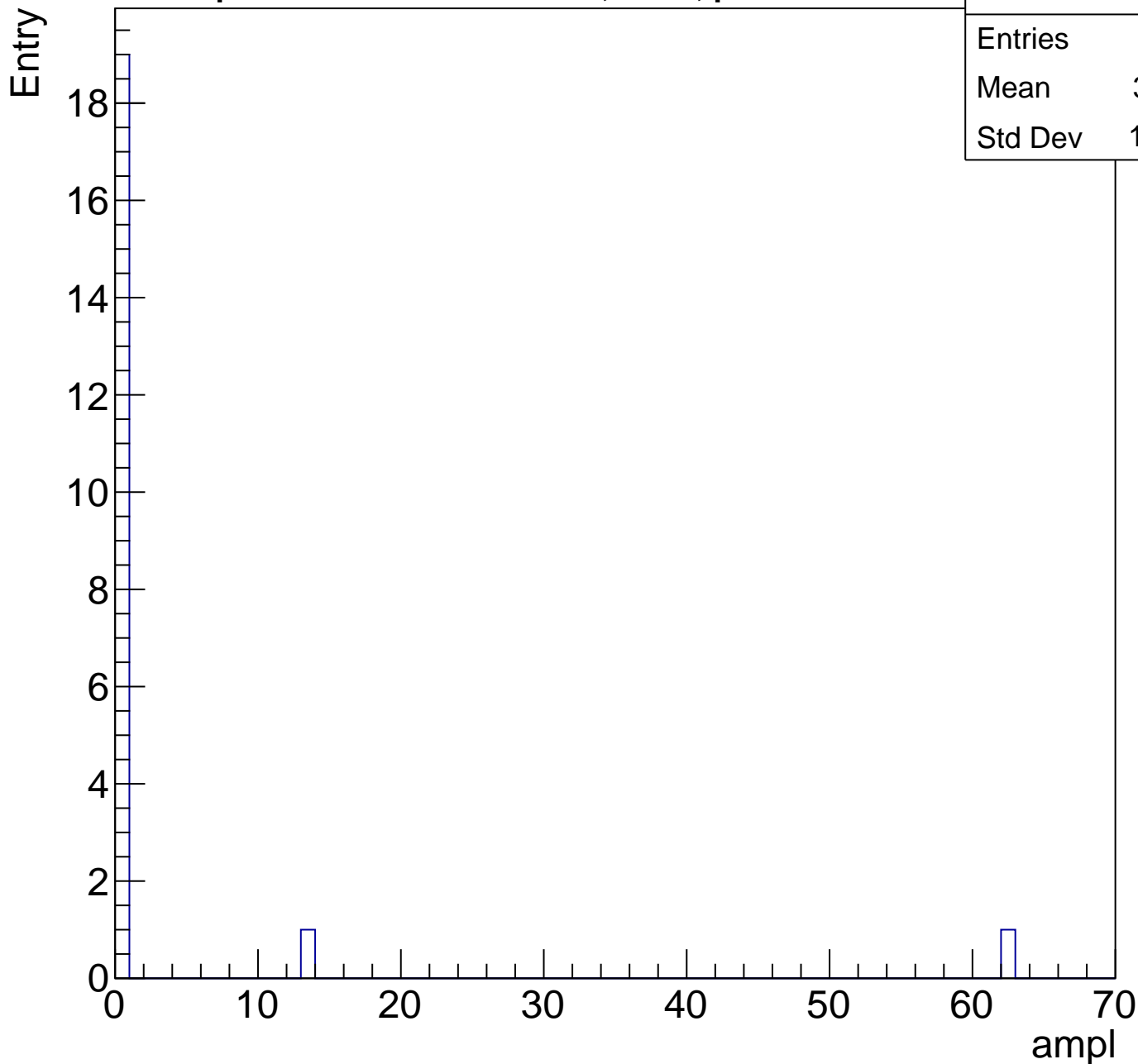




# B1L103S, U4-ch126, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 21    |
| Mean    | 3.571 |
| Std Dev | 13.35 |

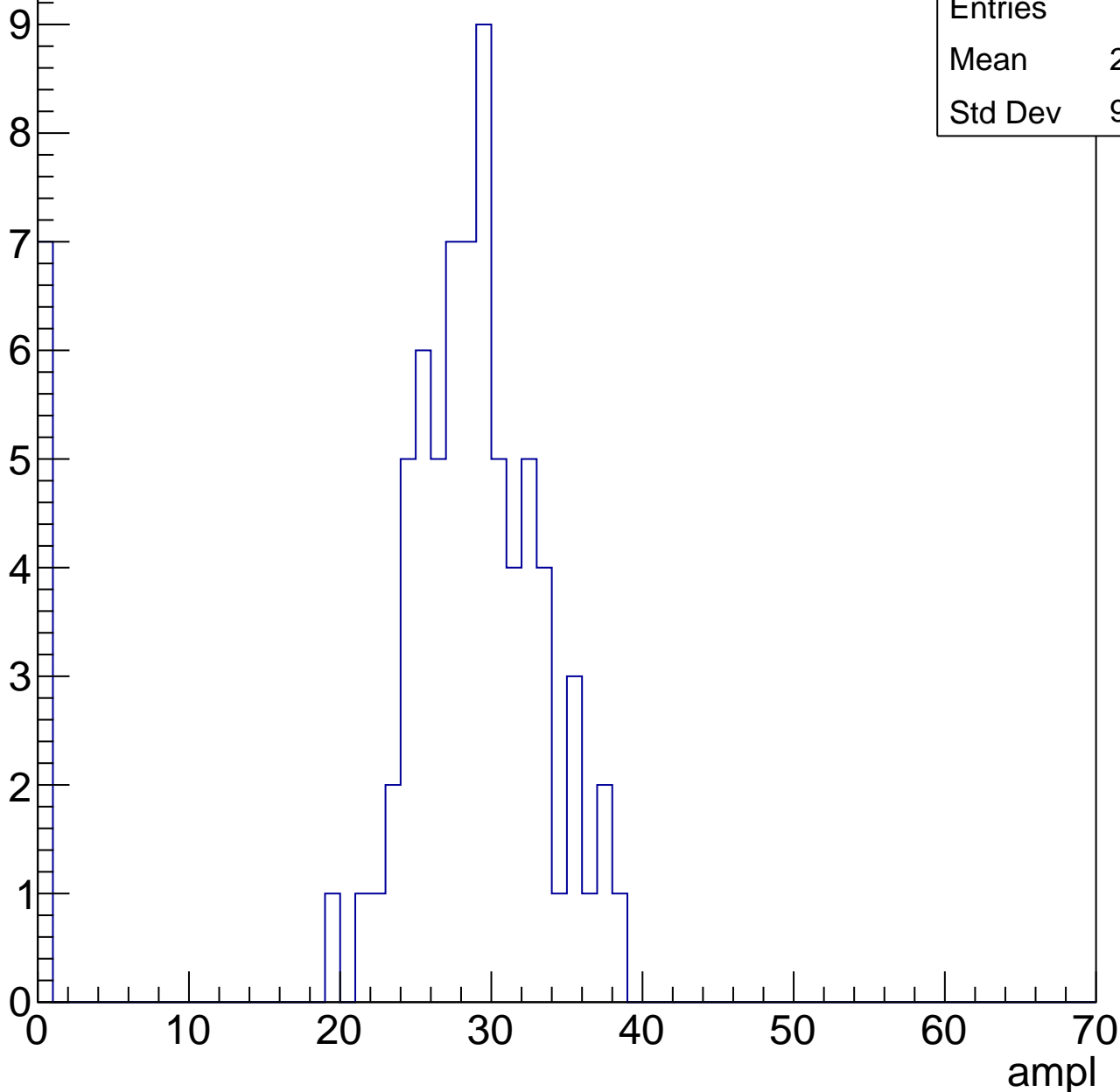


# B1L103S, U4-ch127, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 77    |
| Mean    | 26.06 |
| Std Dev | 9.067 |

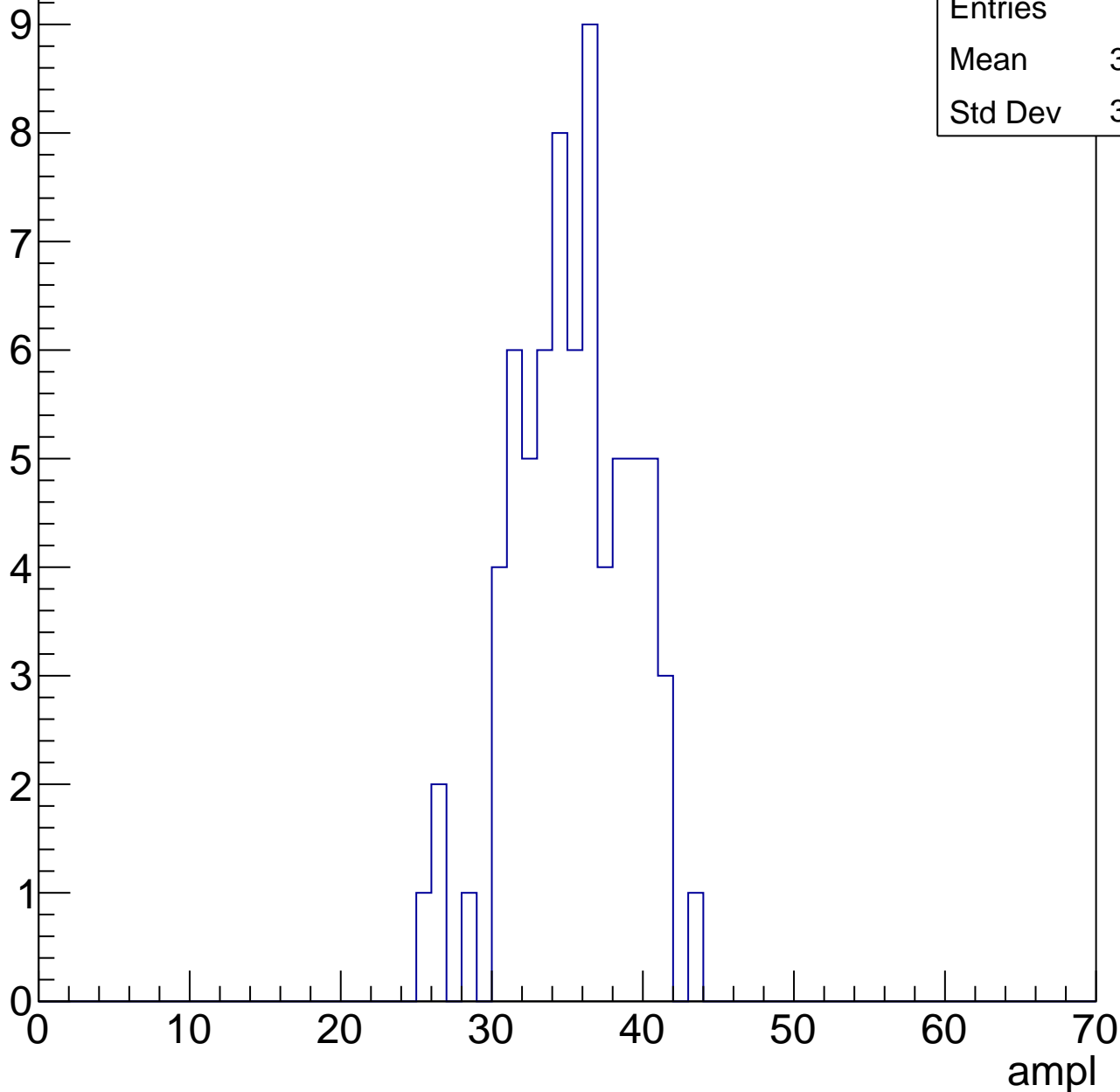


# B1L103S, U4-ch127, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 71    |
| Mean    | 34.85 |
| Std Dev | 3.808 |



# B1L103S, U4-ch127, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

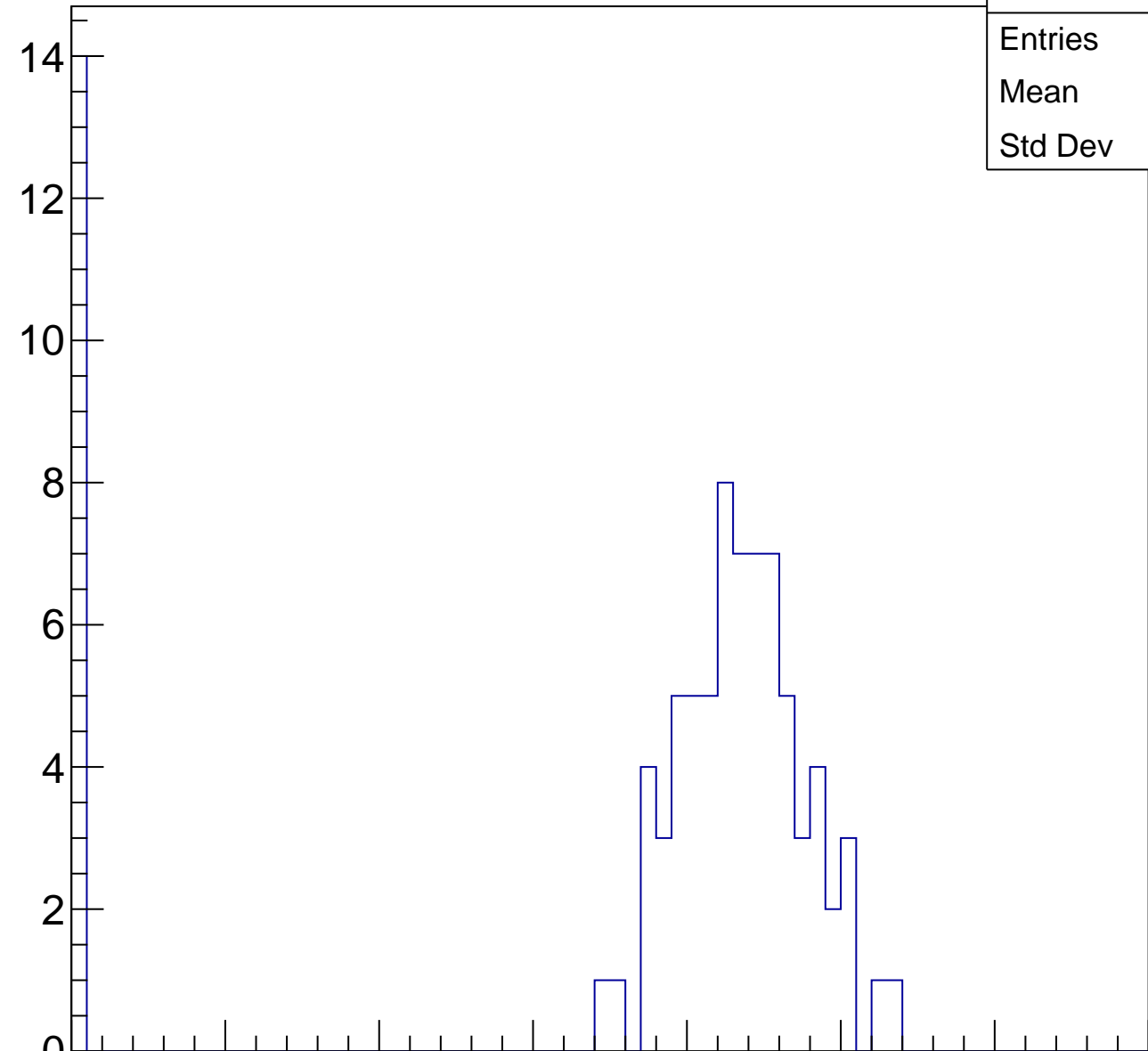
|         |       |
|---------|-------|
| Entries | 86    |
| Mean    | 36.13 |
| Std Dev | 16.34 |

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

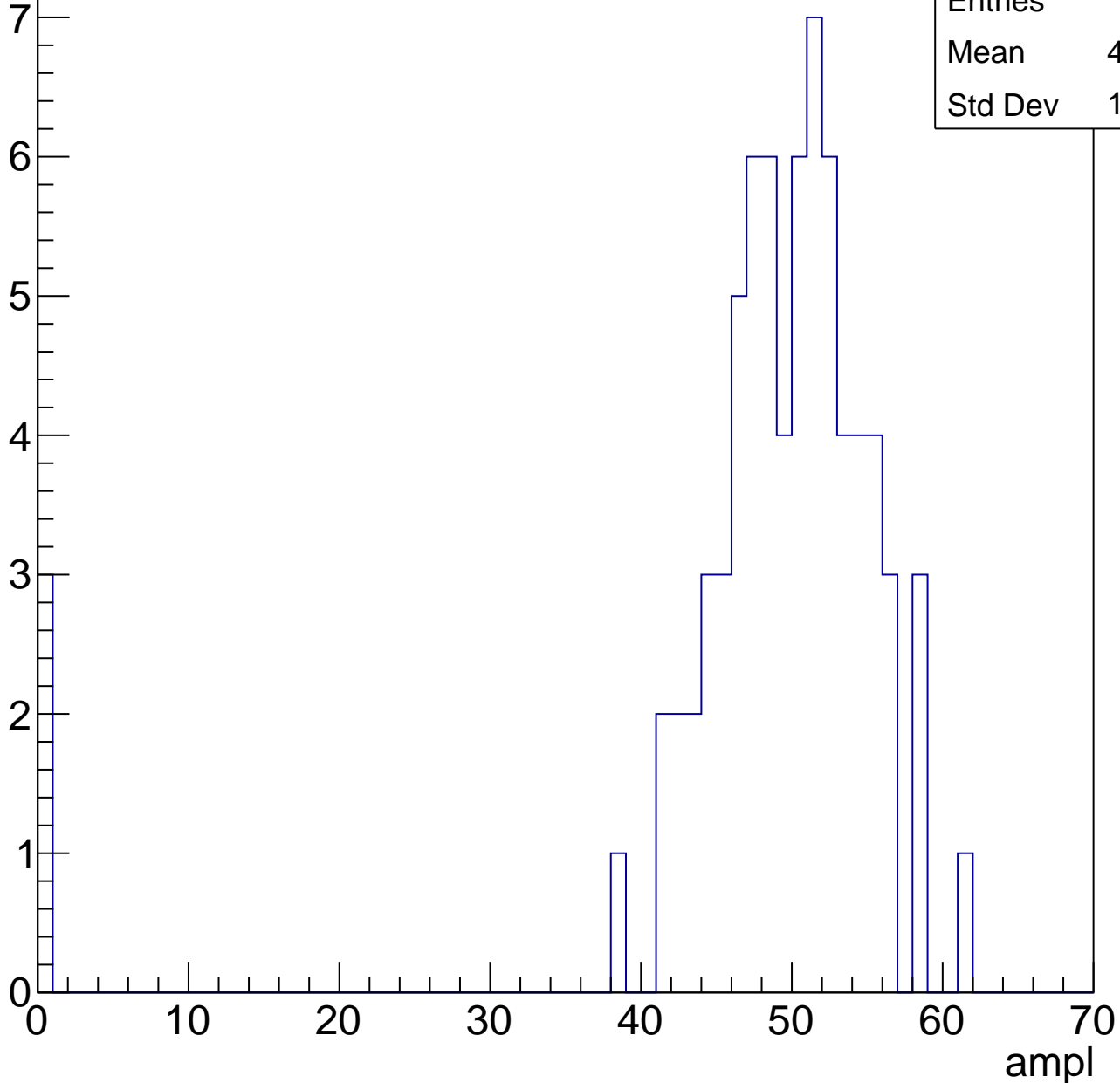


# B1L103S, U4-ch127, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 75    |
| Mean    | 47.64 |
| Std Dev | 10.72 |

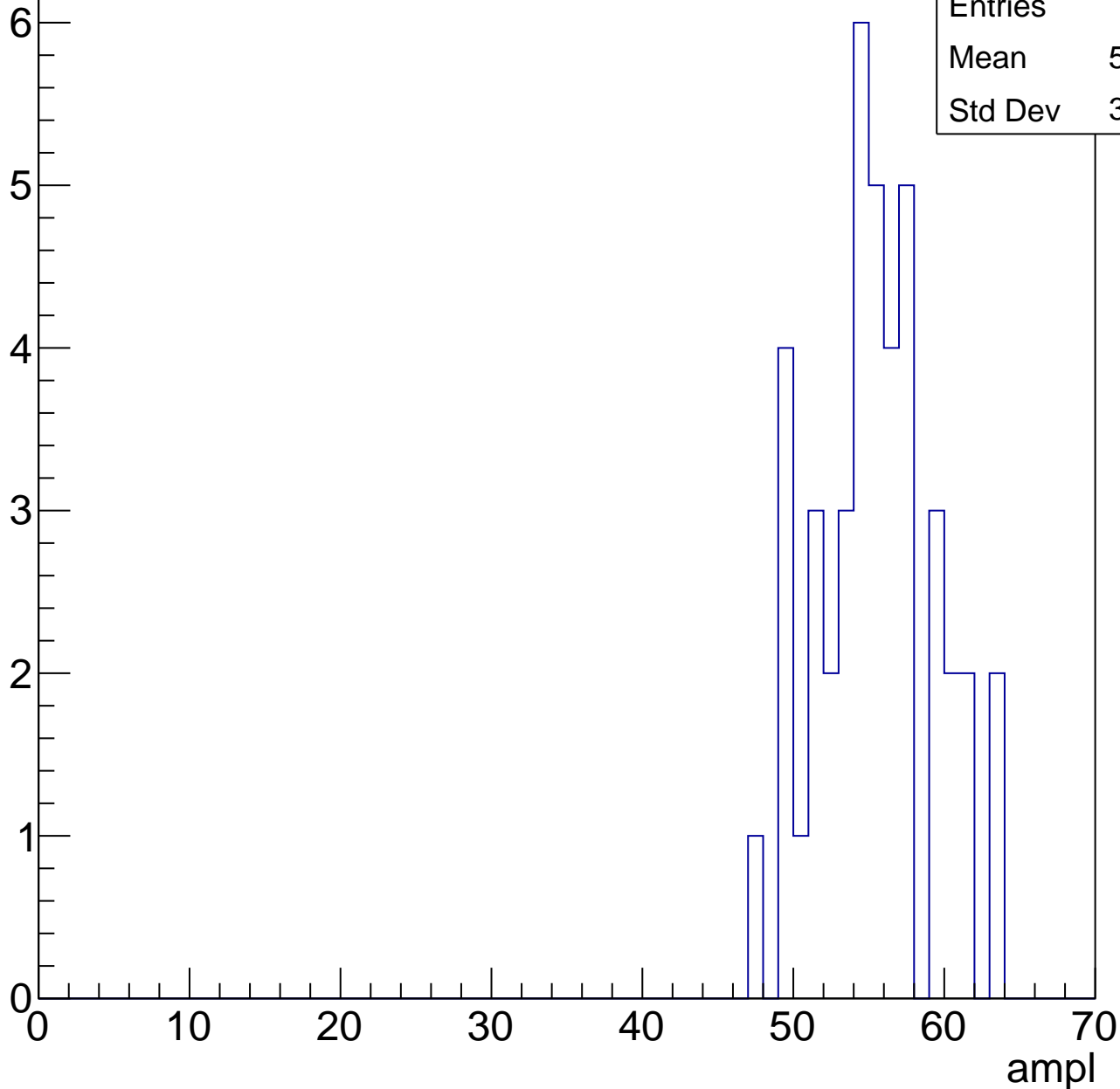


# B1L103S, U4-ch127, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 43    |
| Mean    | 54.93 |
| Std Dev | 3.854 |

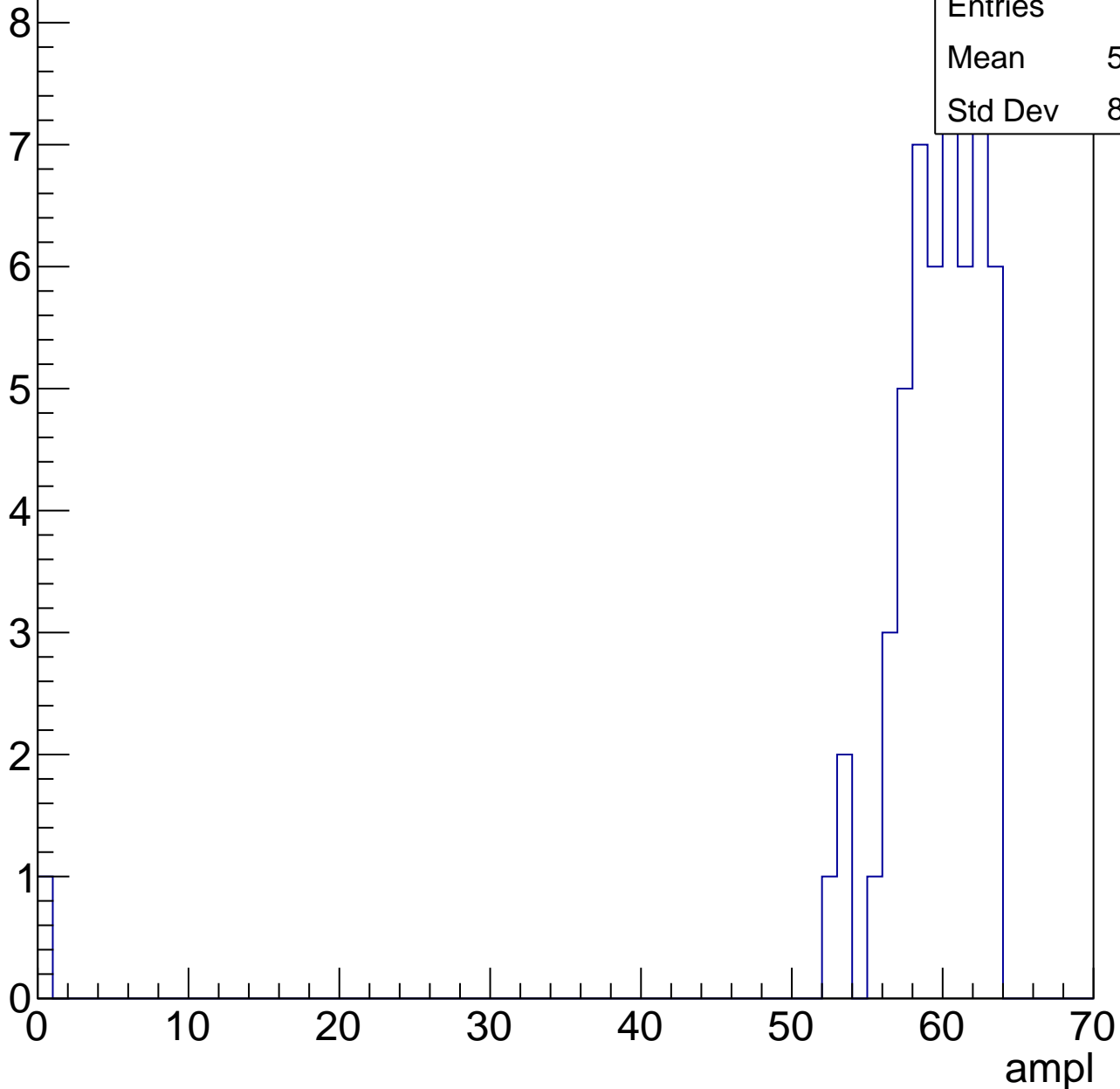


# B1L103S, U4-ch127, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

|         |       |
|---------|-------|
| Entries | 54    |
| Mean    | 58.26 |
| Std Dev | 8.435 |



# B1L103S, U4-ch127, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

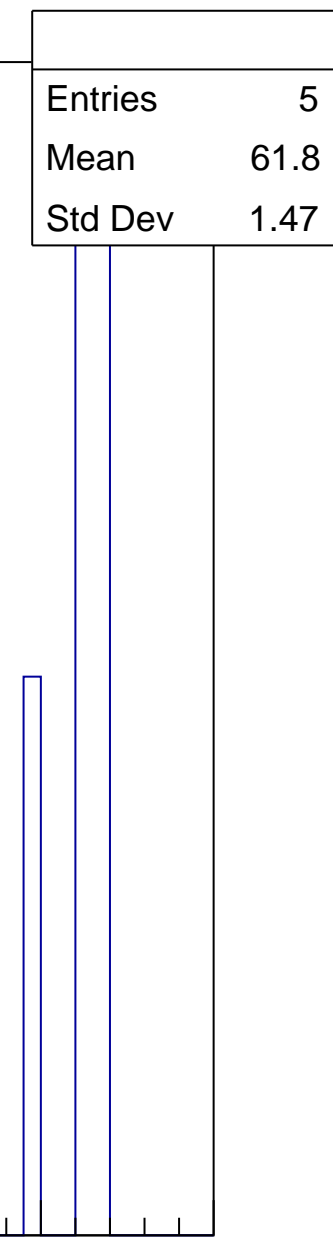
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

|         |      |
|---------|------|
| Entries | 5    |
| Mean    | 61.8 |
| Std Dev | 1.47 |

0 10 20 30 40 50 60 70

ampl

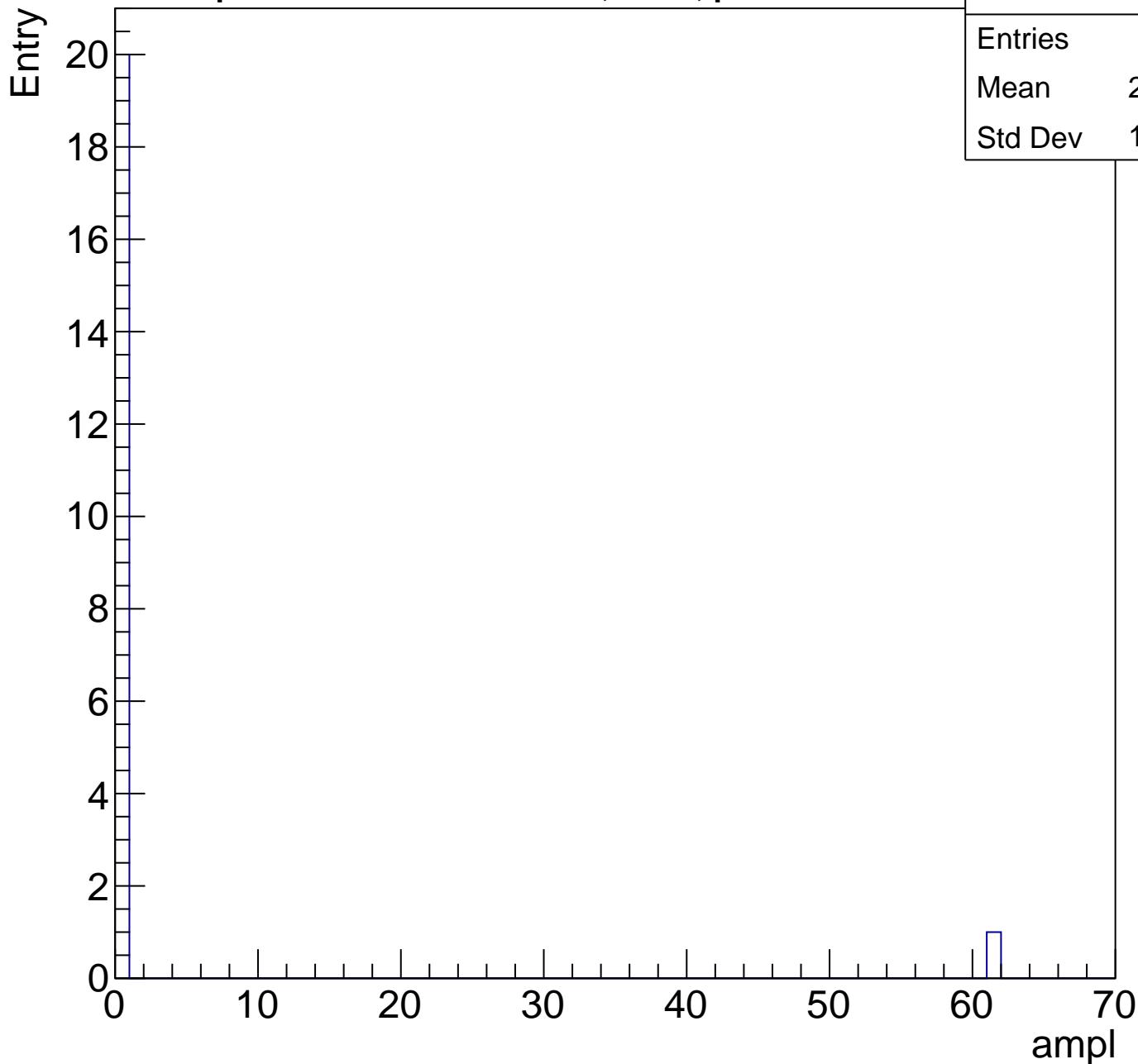




# B1L103S, U4-ch127, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 21    |
| Mean    | 2.905 |
| Std Dev | 12.99 |



# B1L103S, U4-ch127, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

|         |       |
|---------|-------|
| Entries | 21    |
| Mean    | 2.905 |
| Std Dev | 12.99 |

