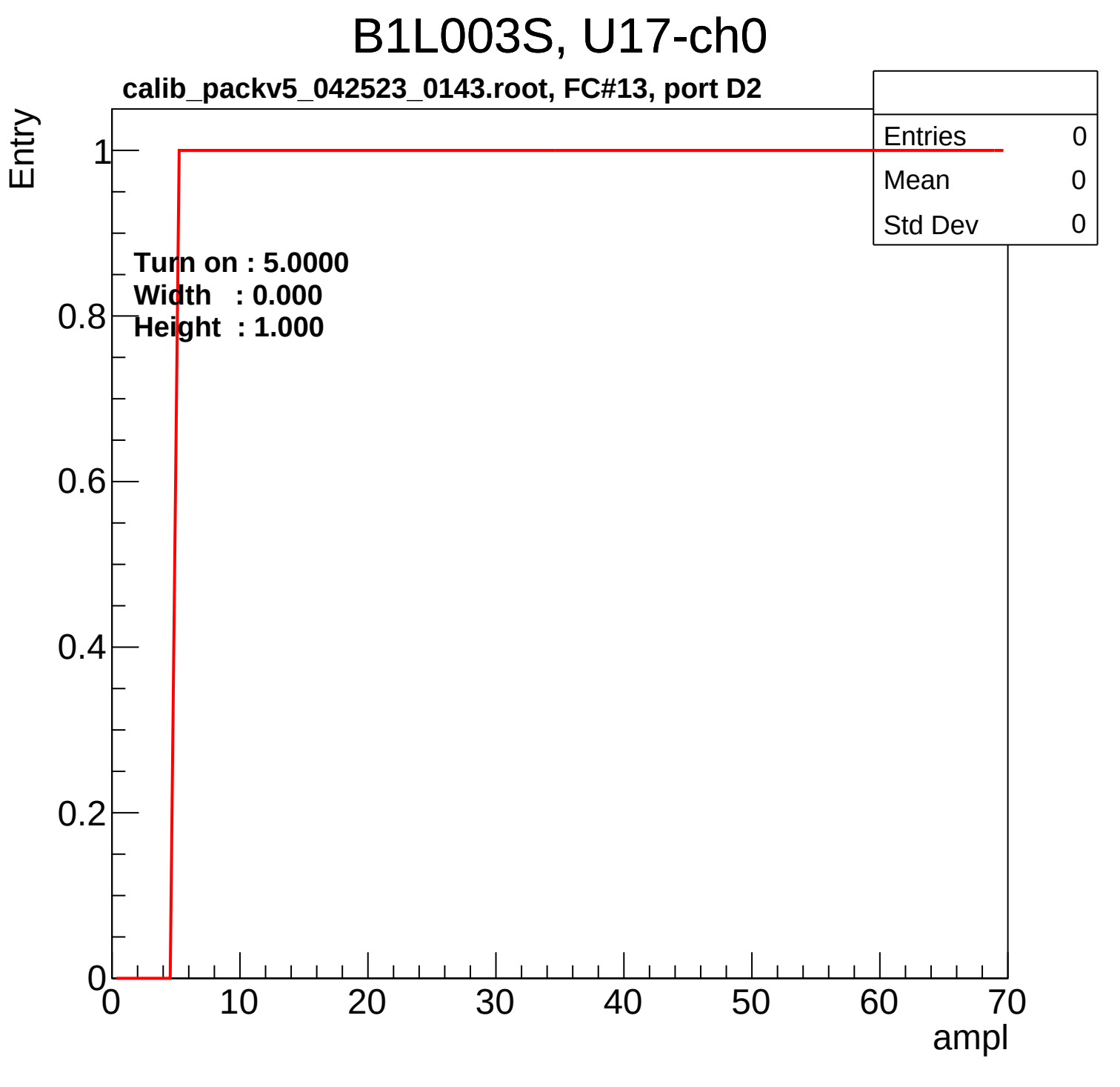
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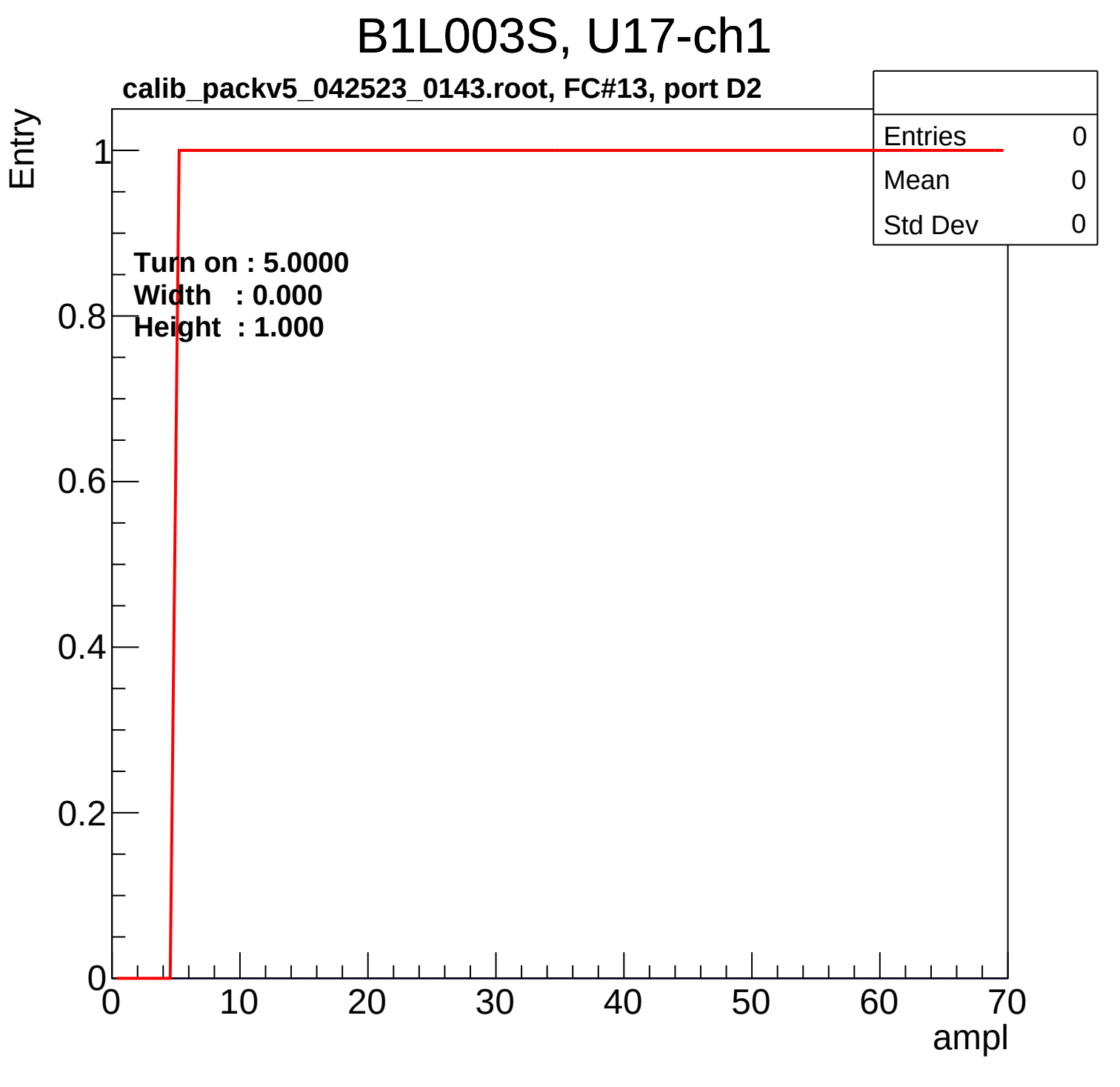
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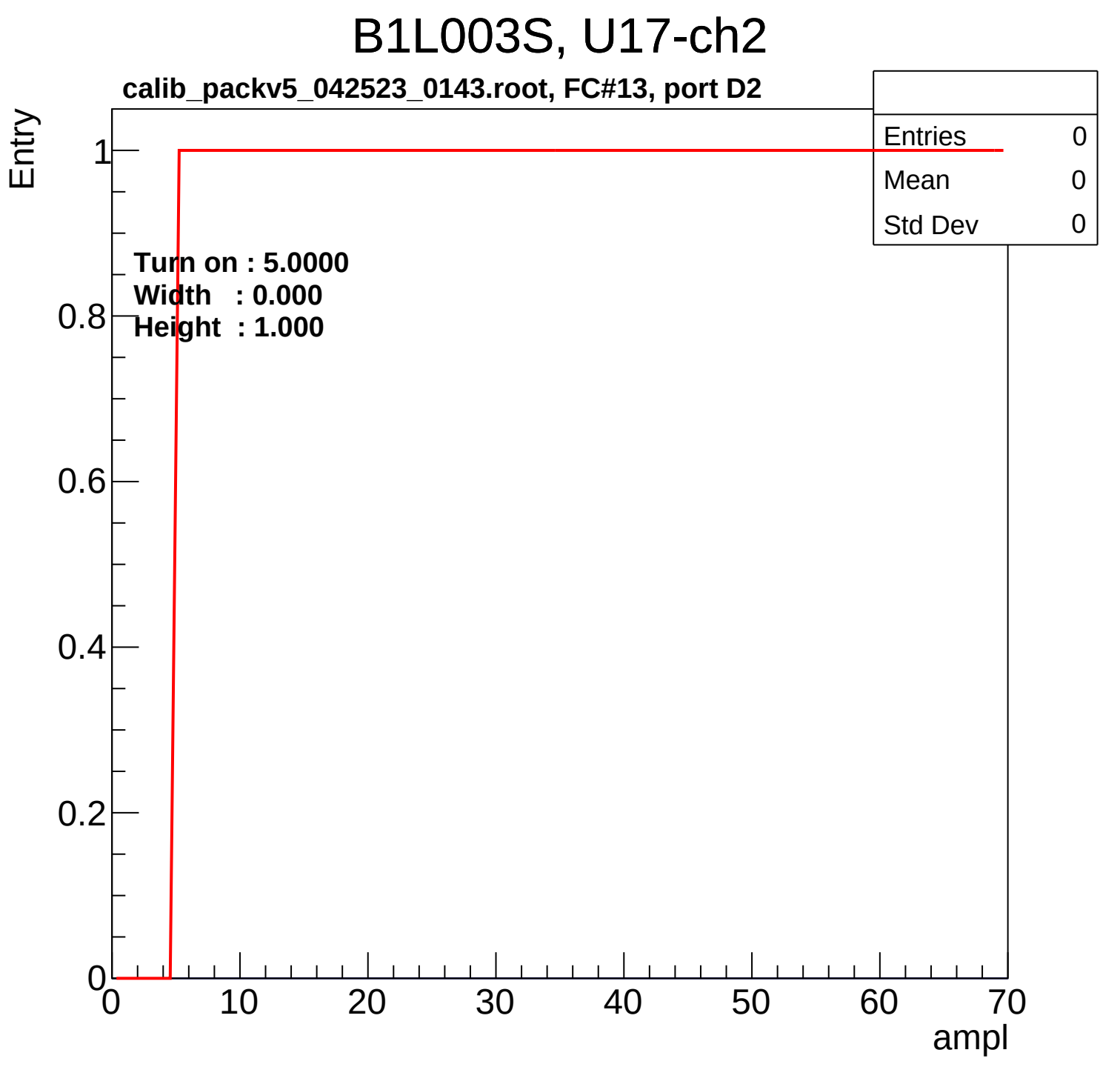
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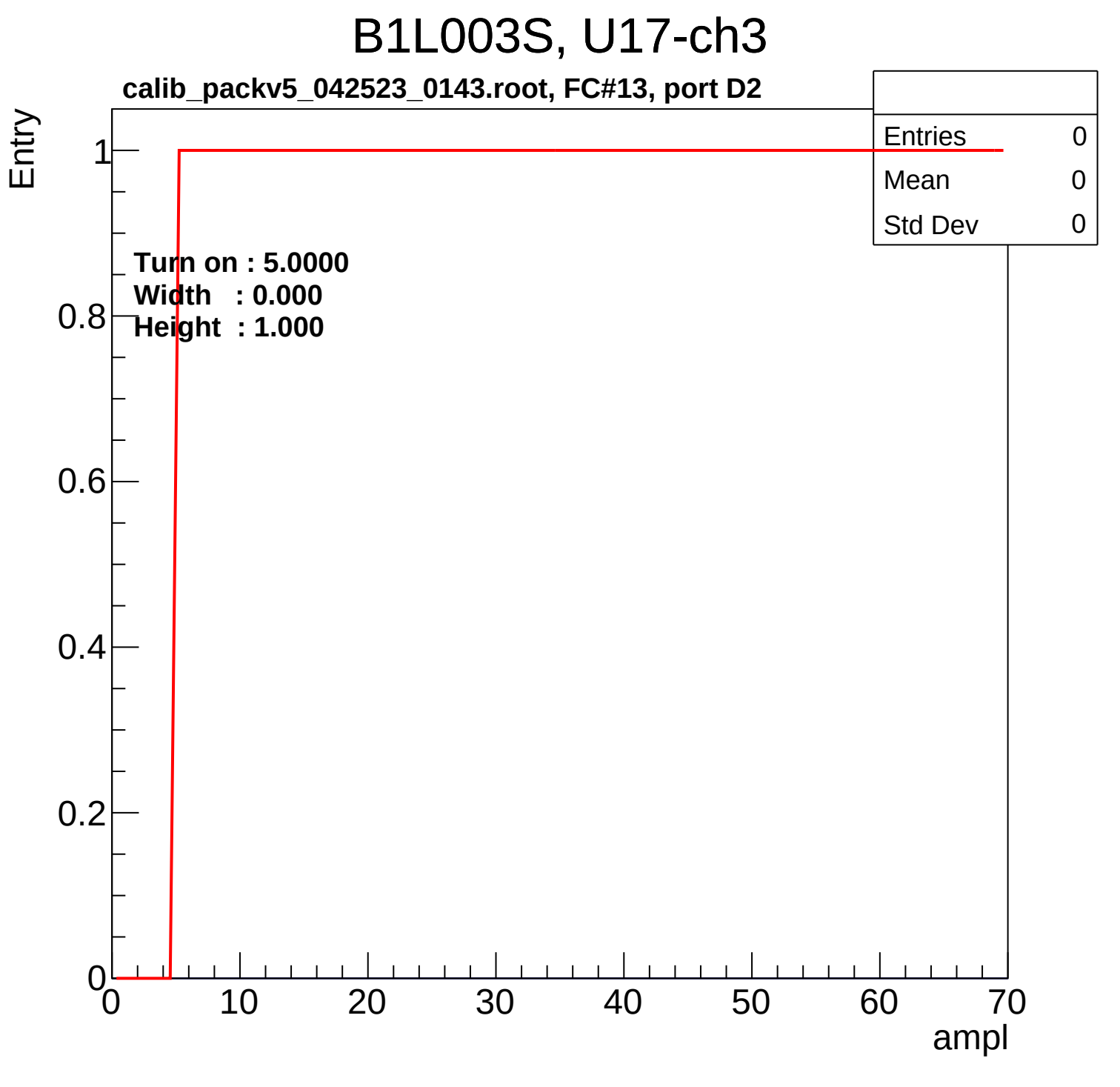
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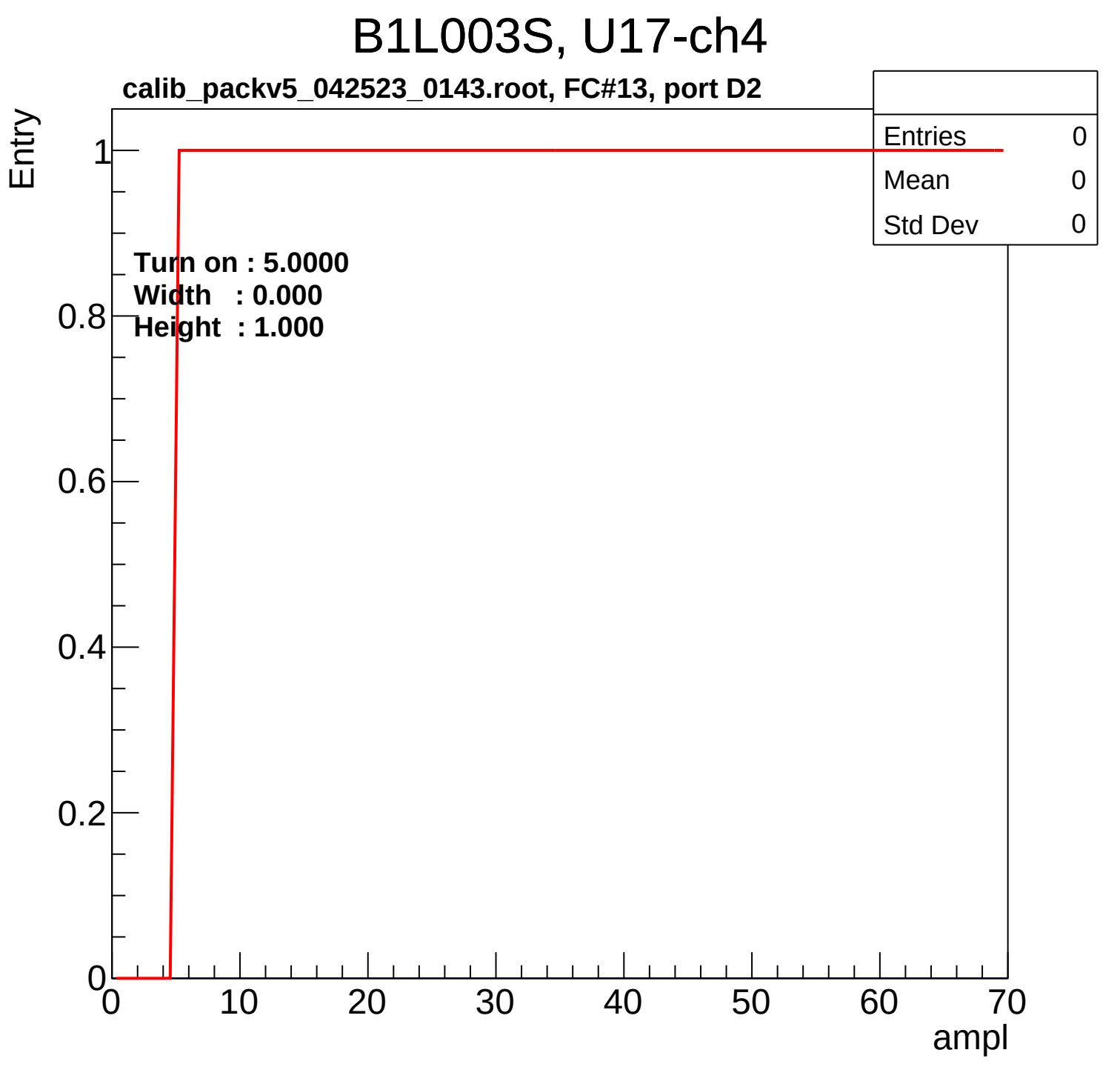
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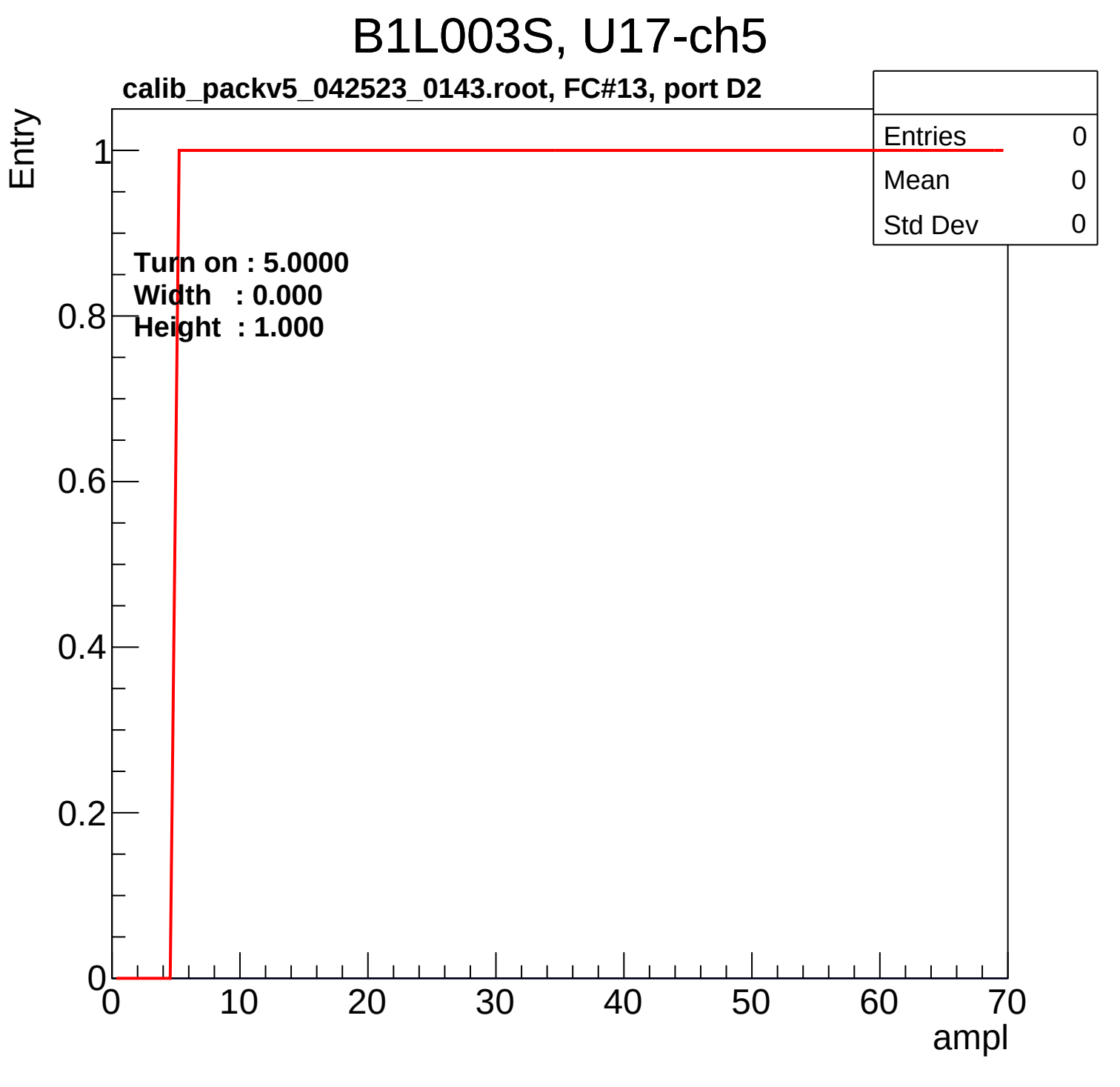
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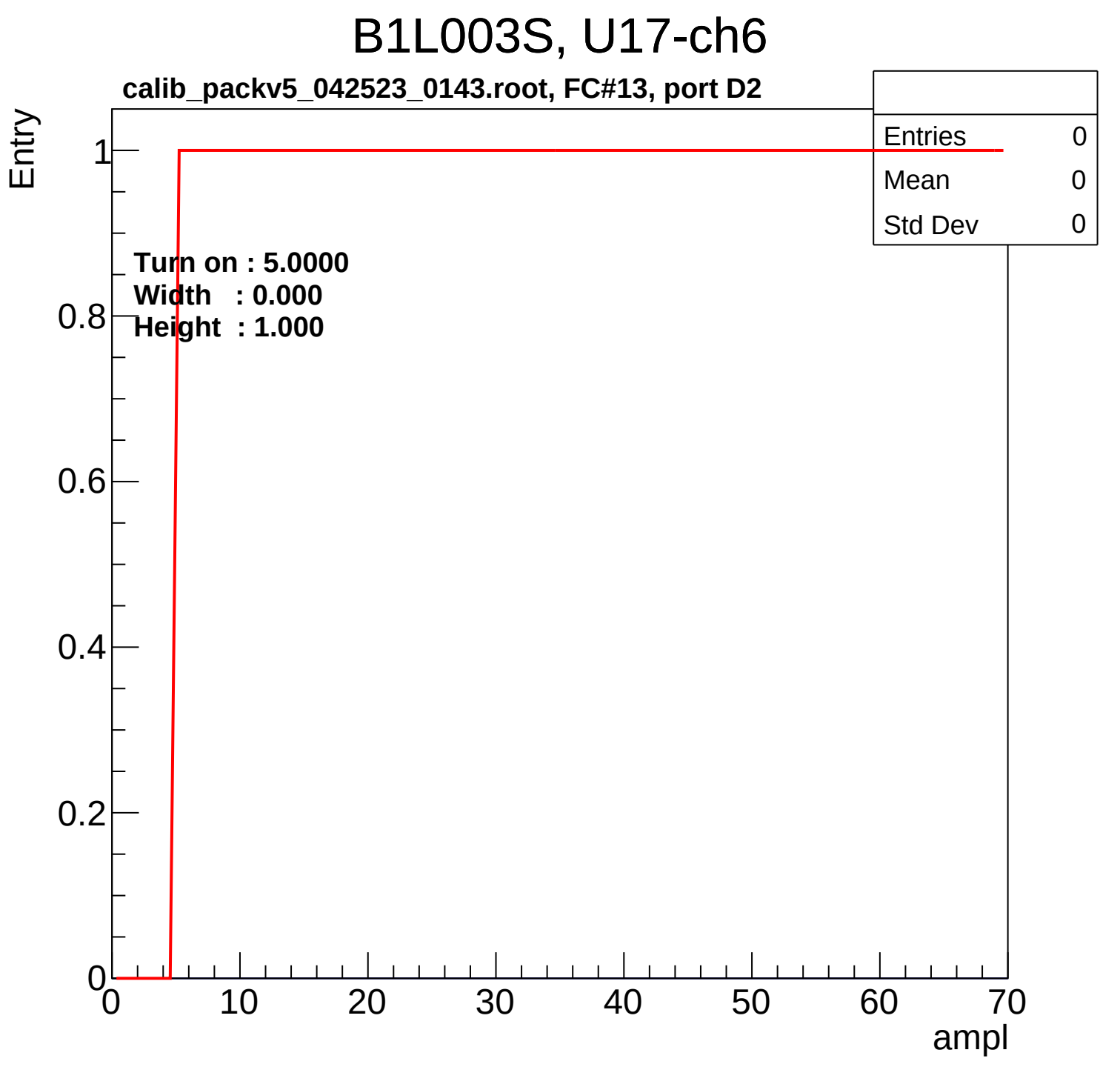
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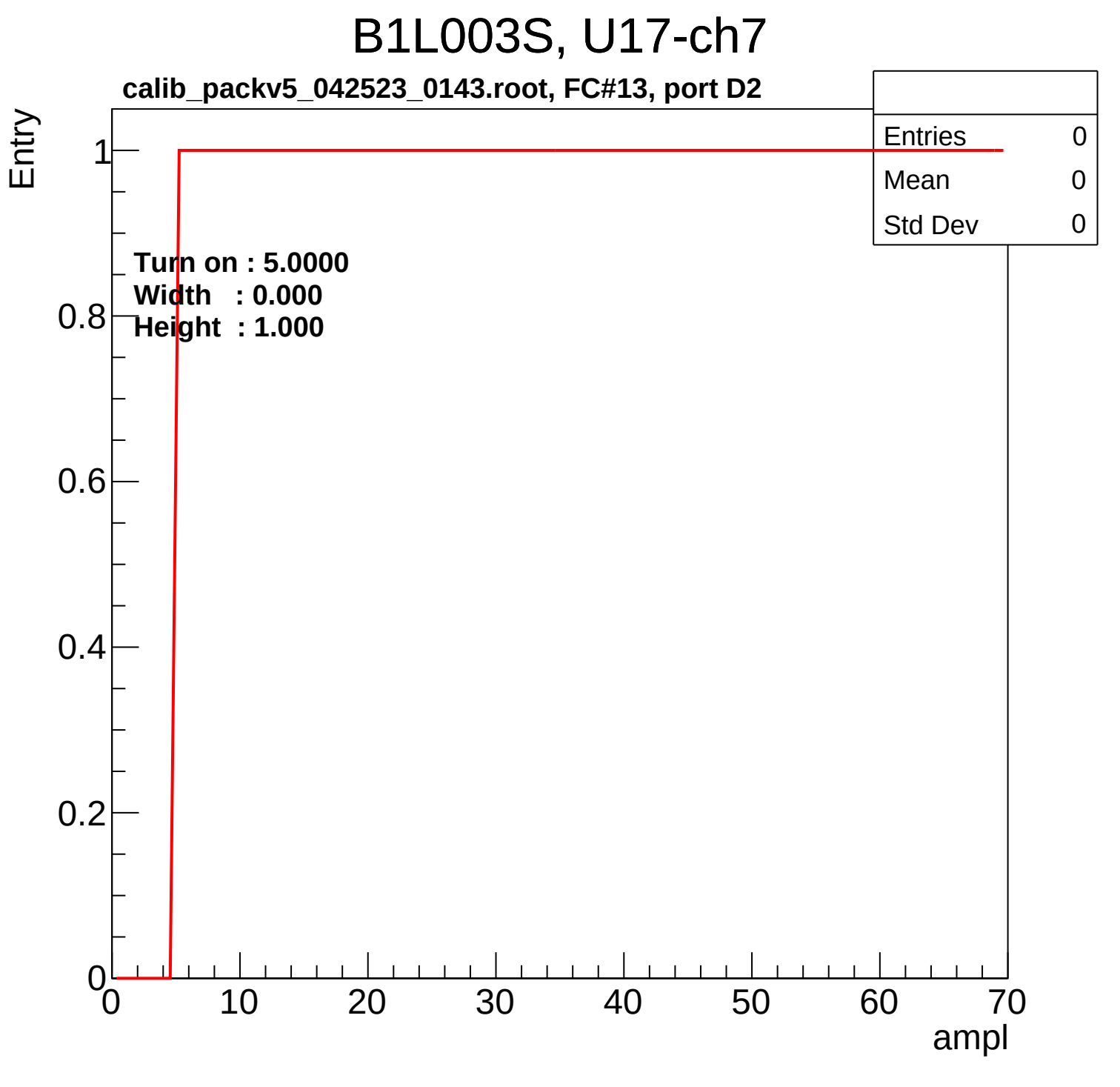
ampl


B1L003S, U17-ch7
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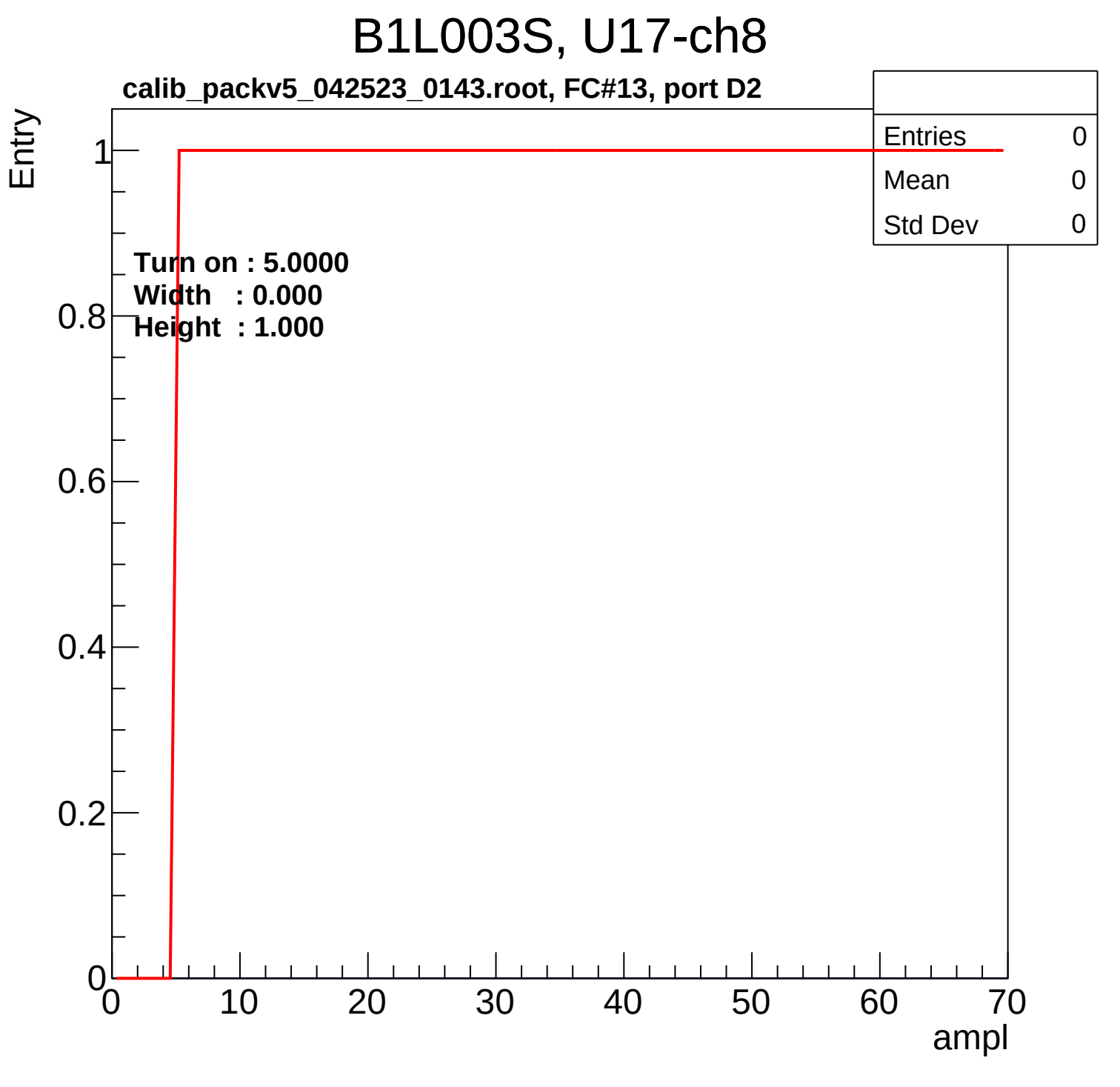
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Std Dev 0
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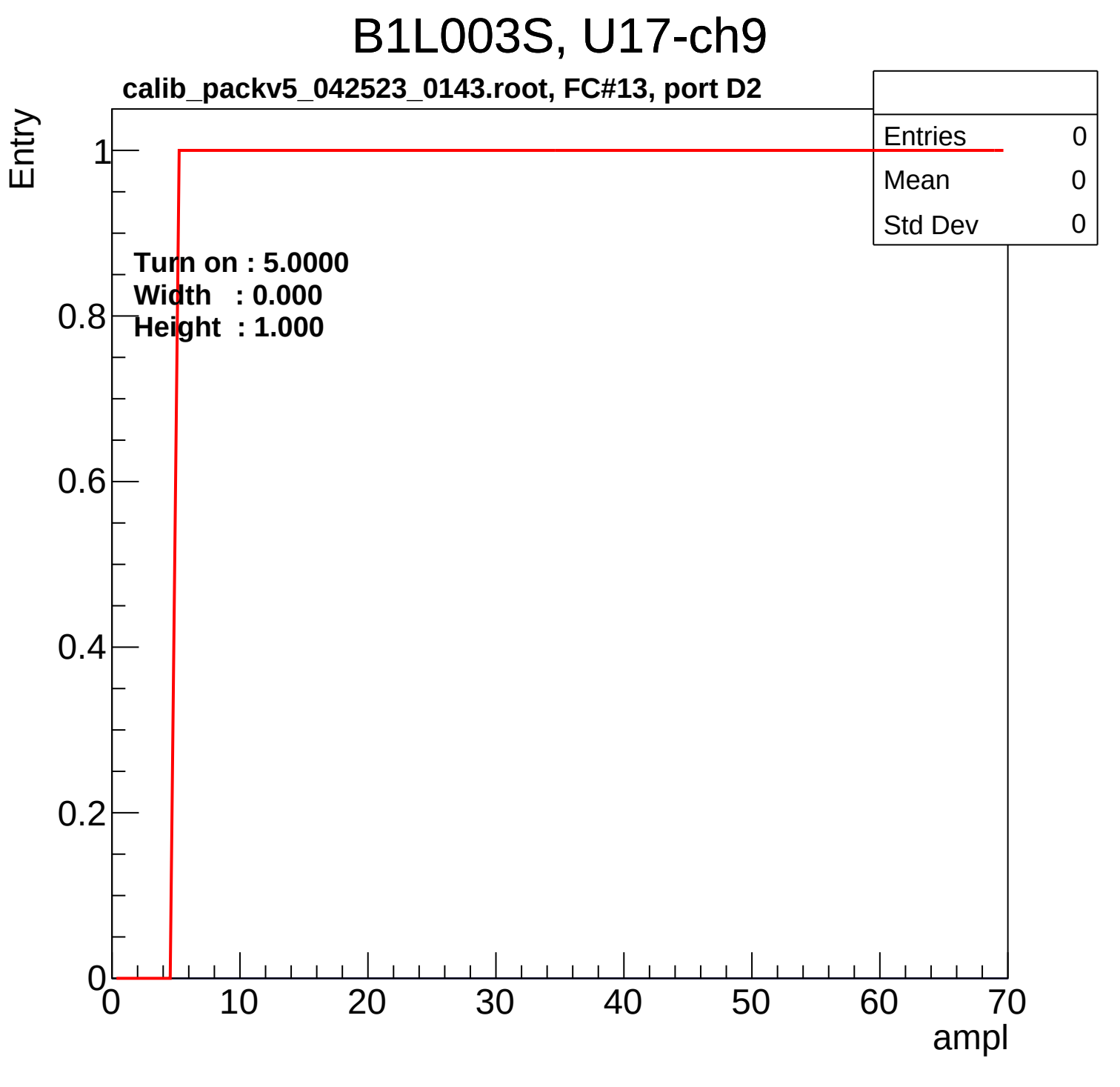
ampl


B1L003S, U17-ch9
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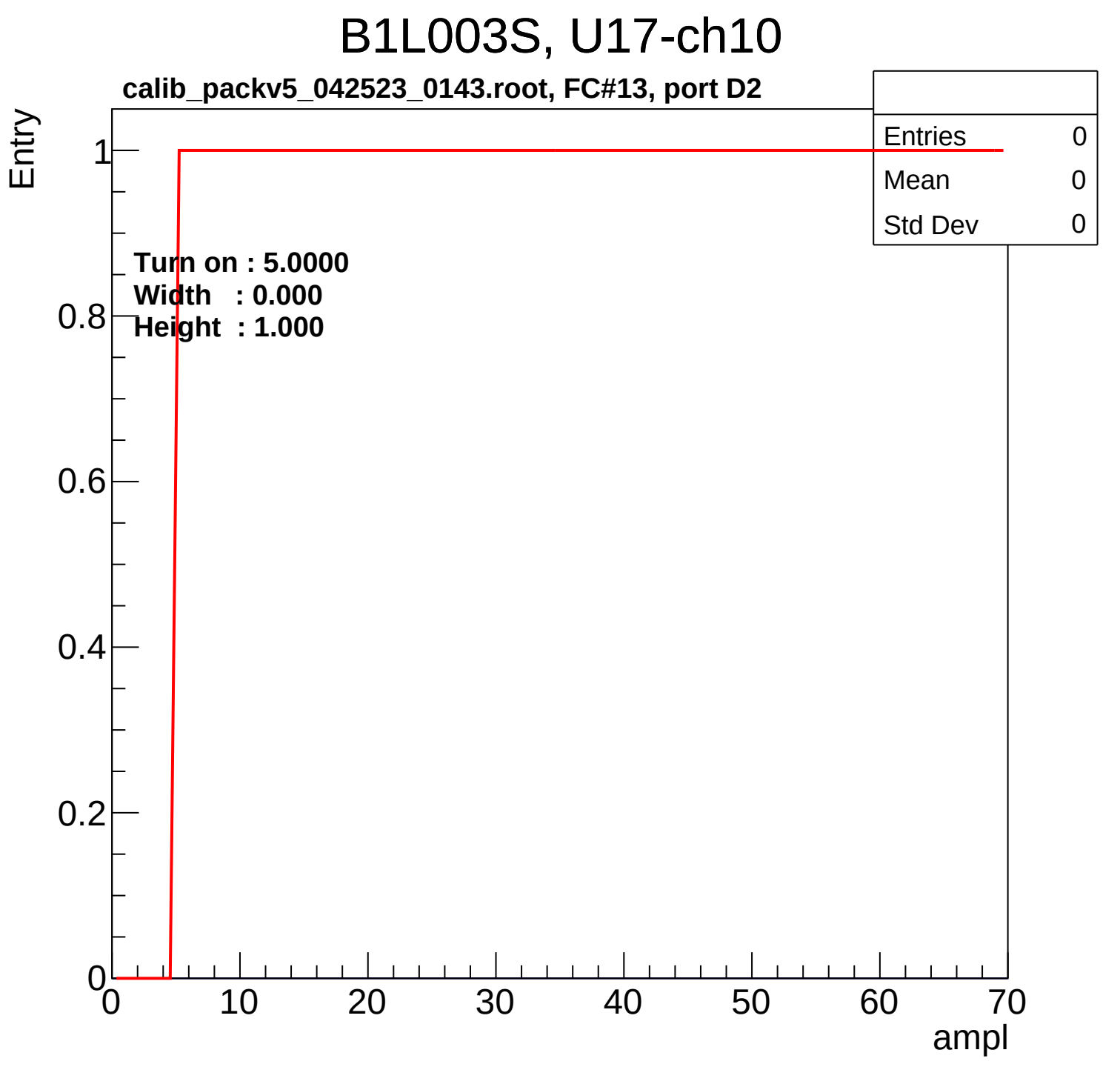
ampl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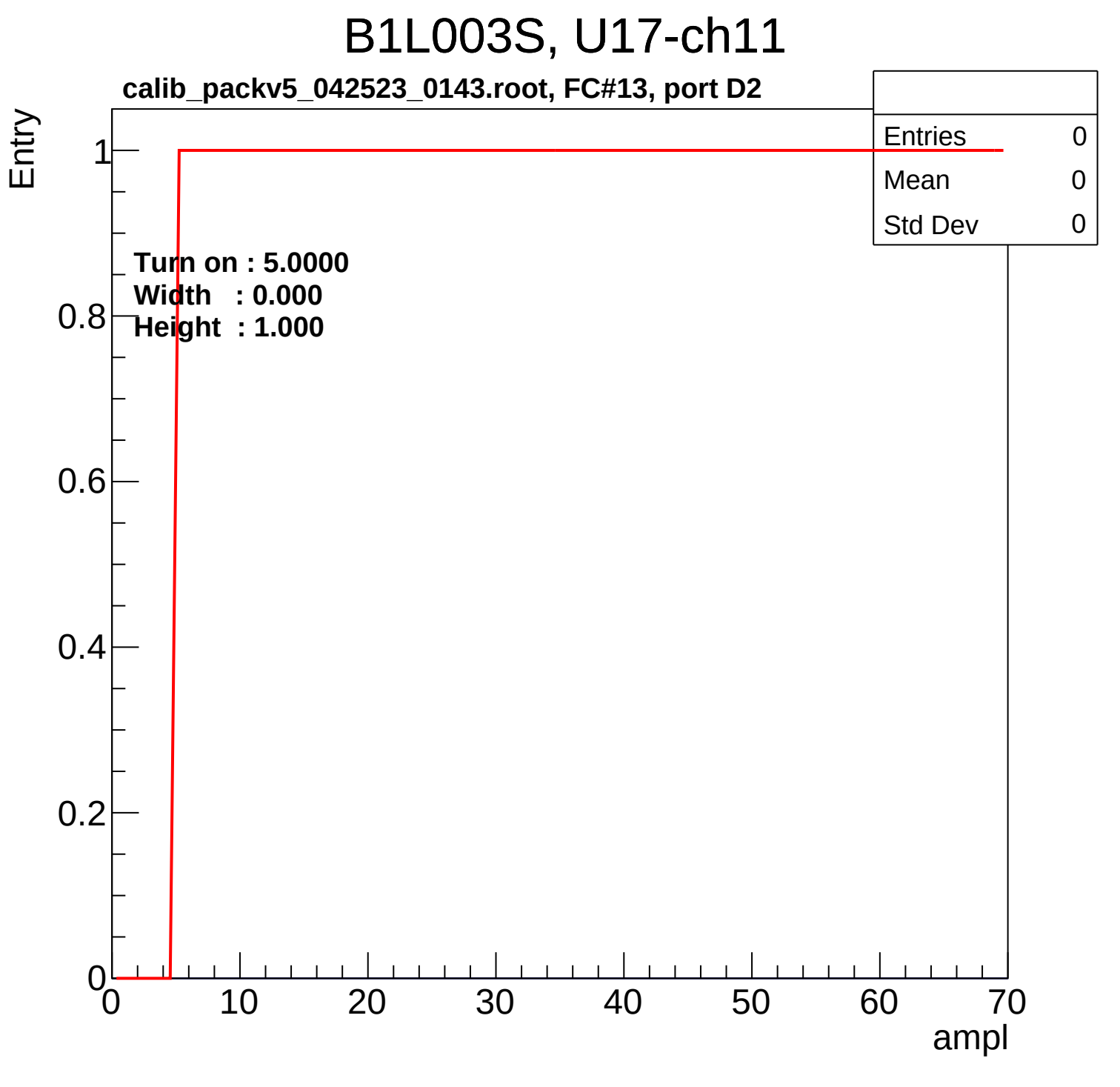
ampl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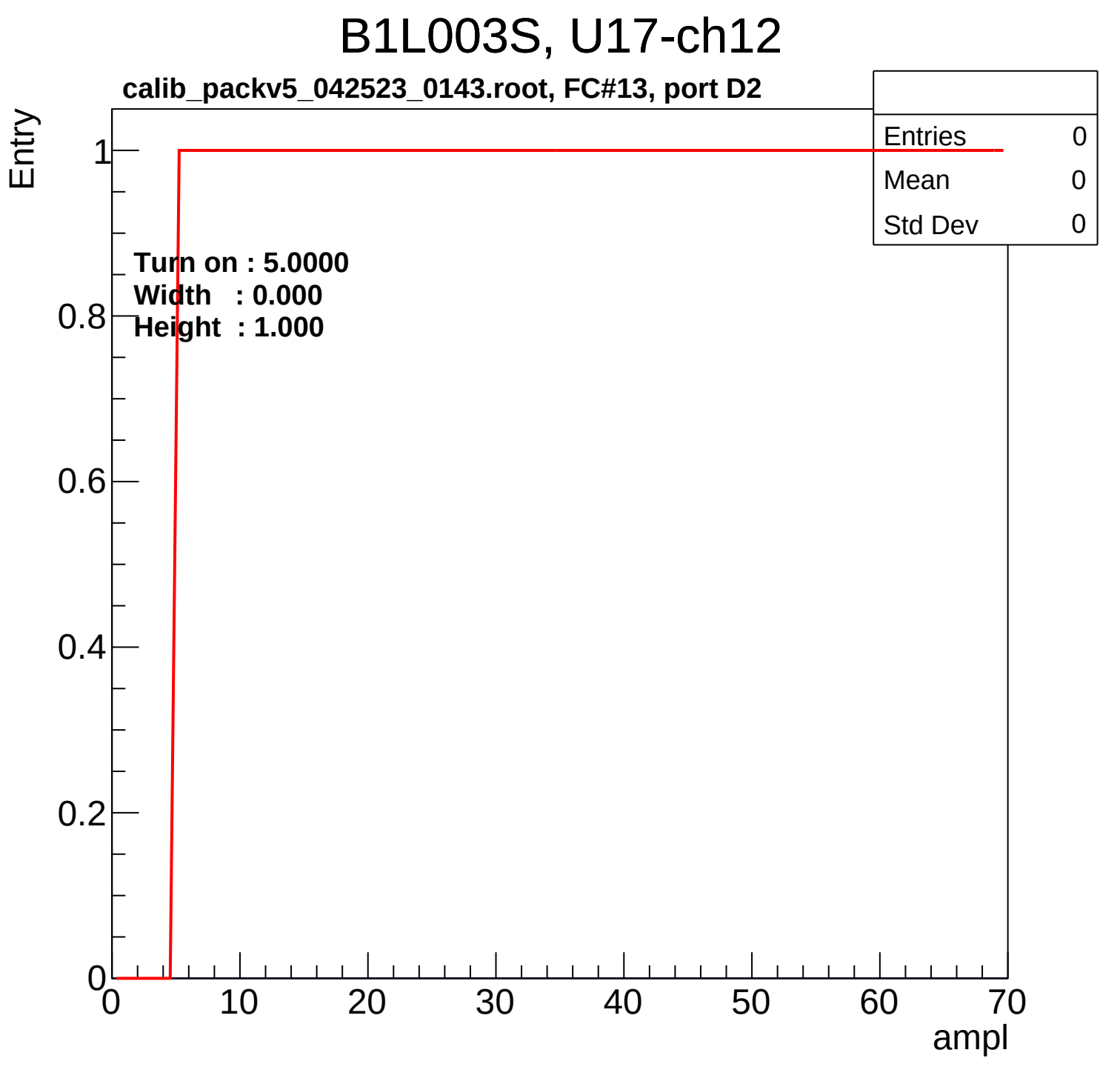
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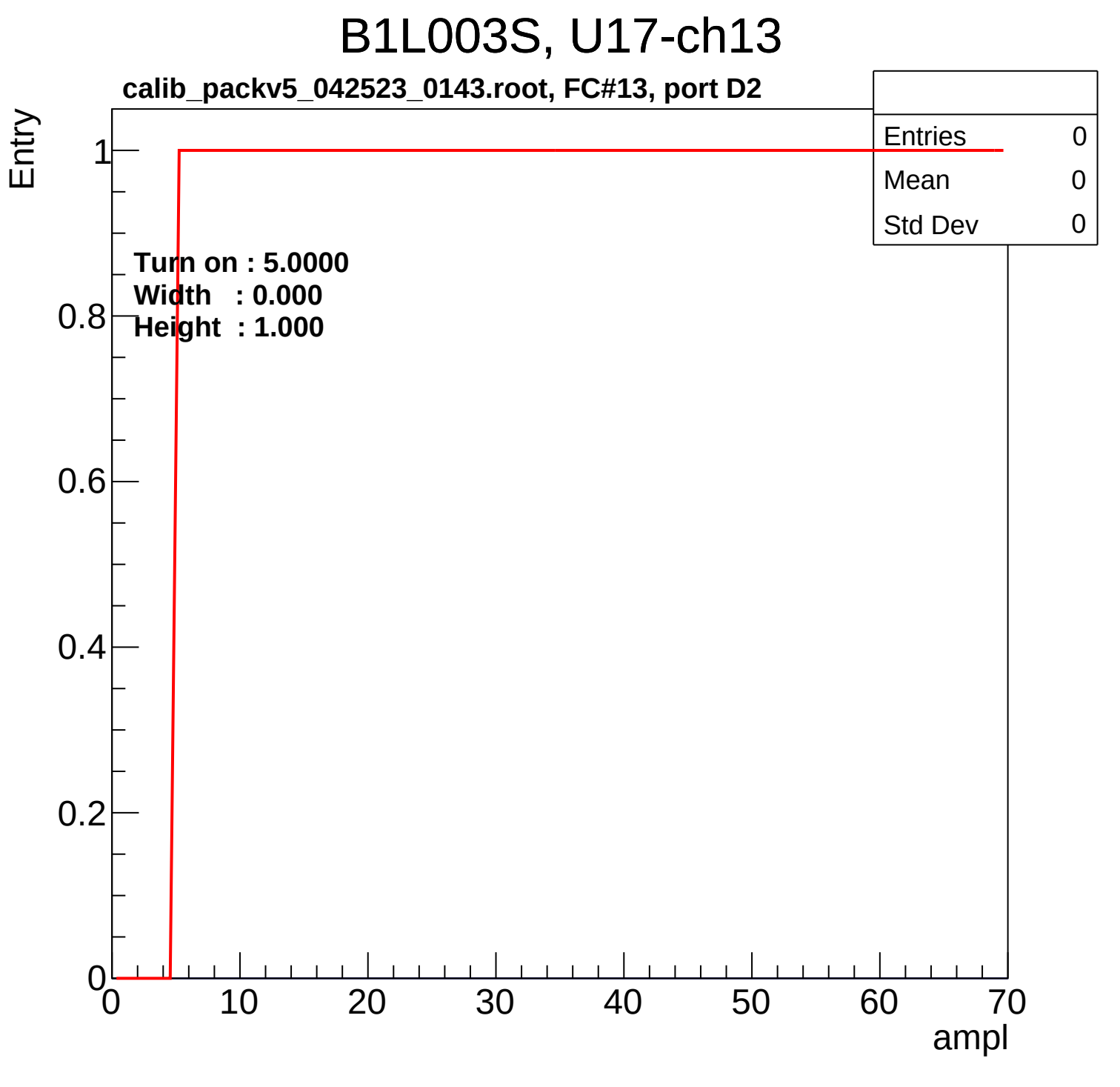
ampl


B1L003S, U17-ch13
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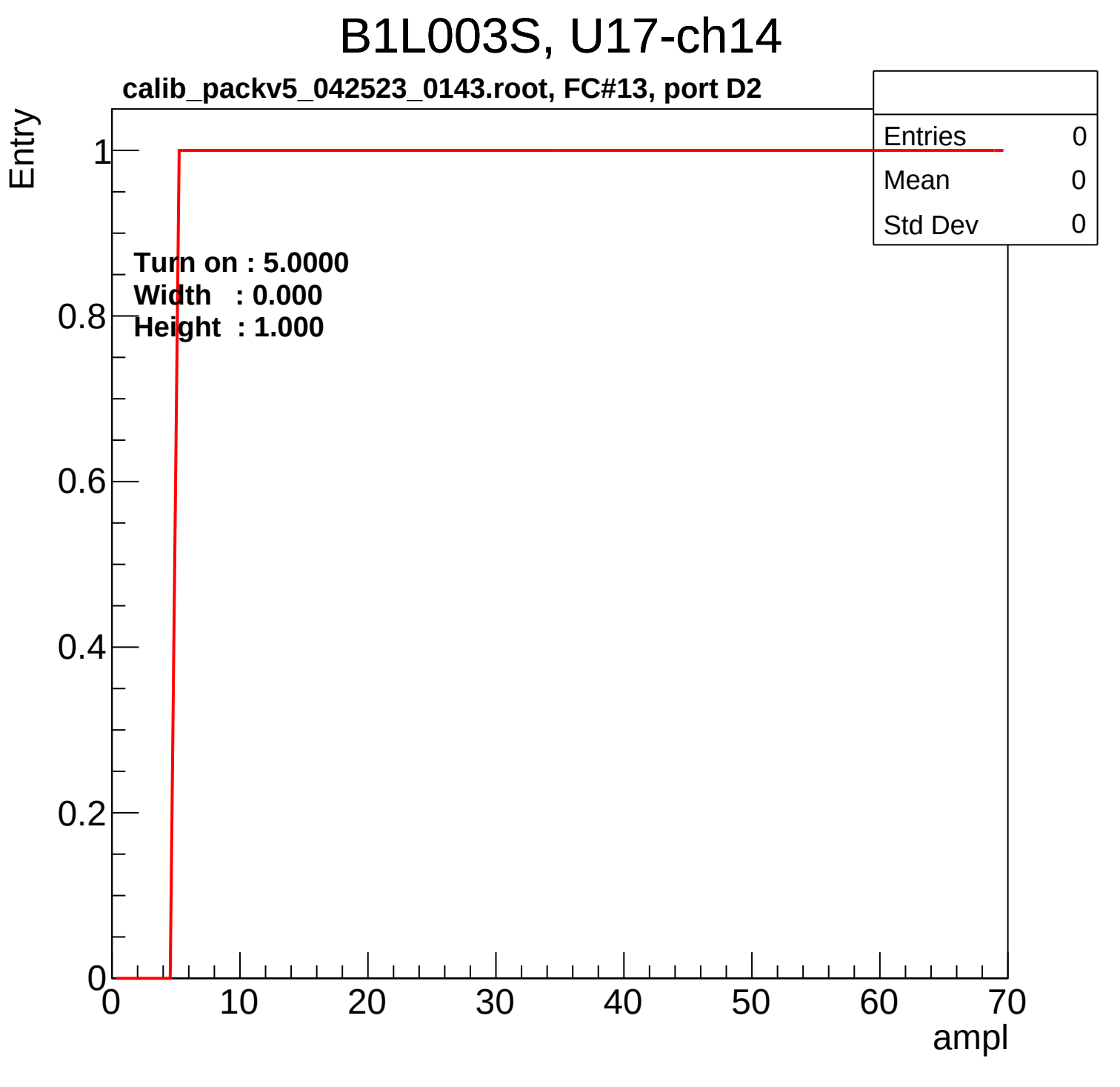
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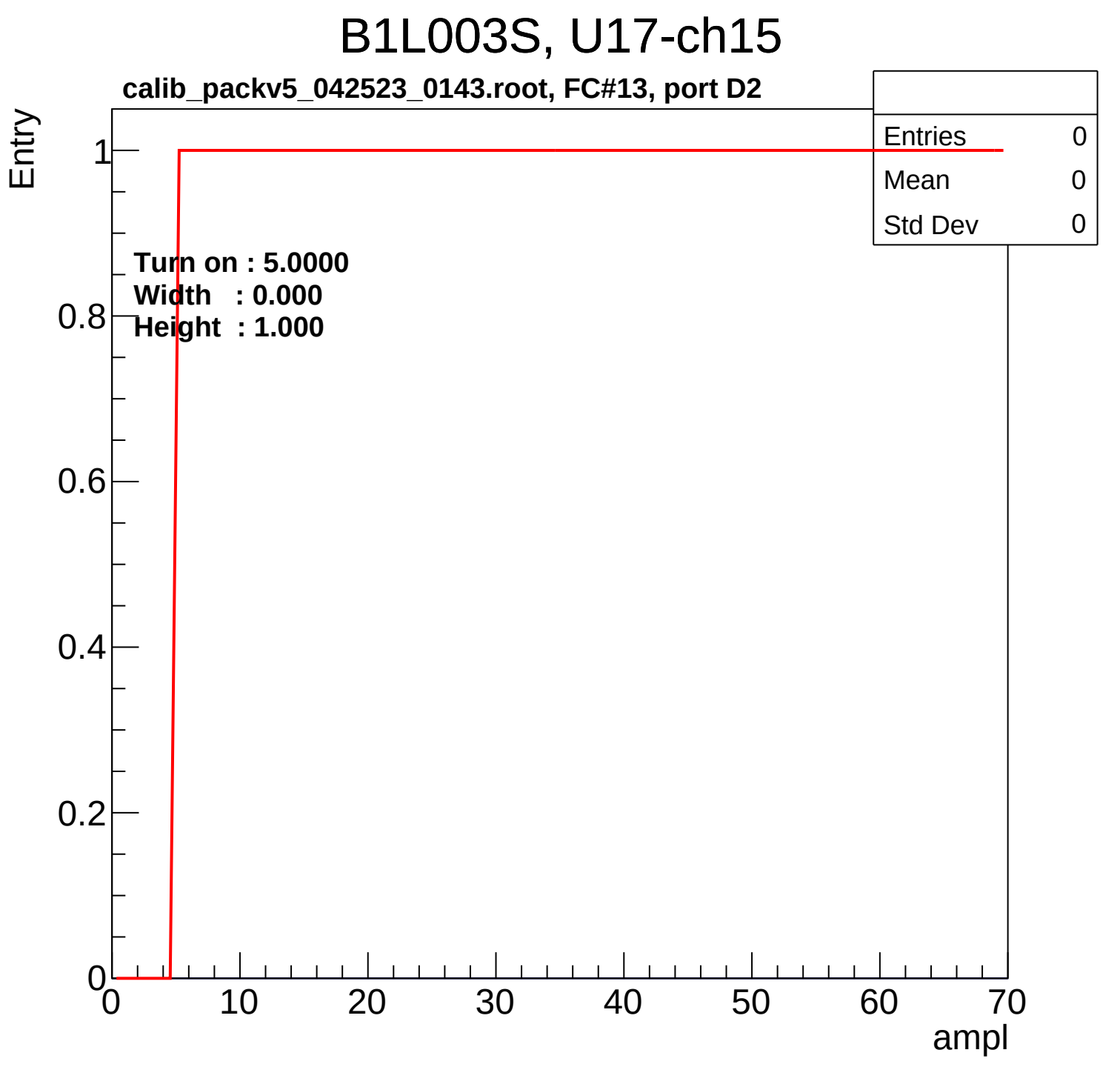
ampl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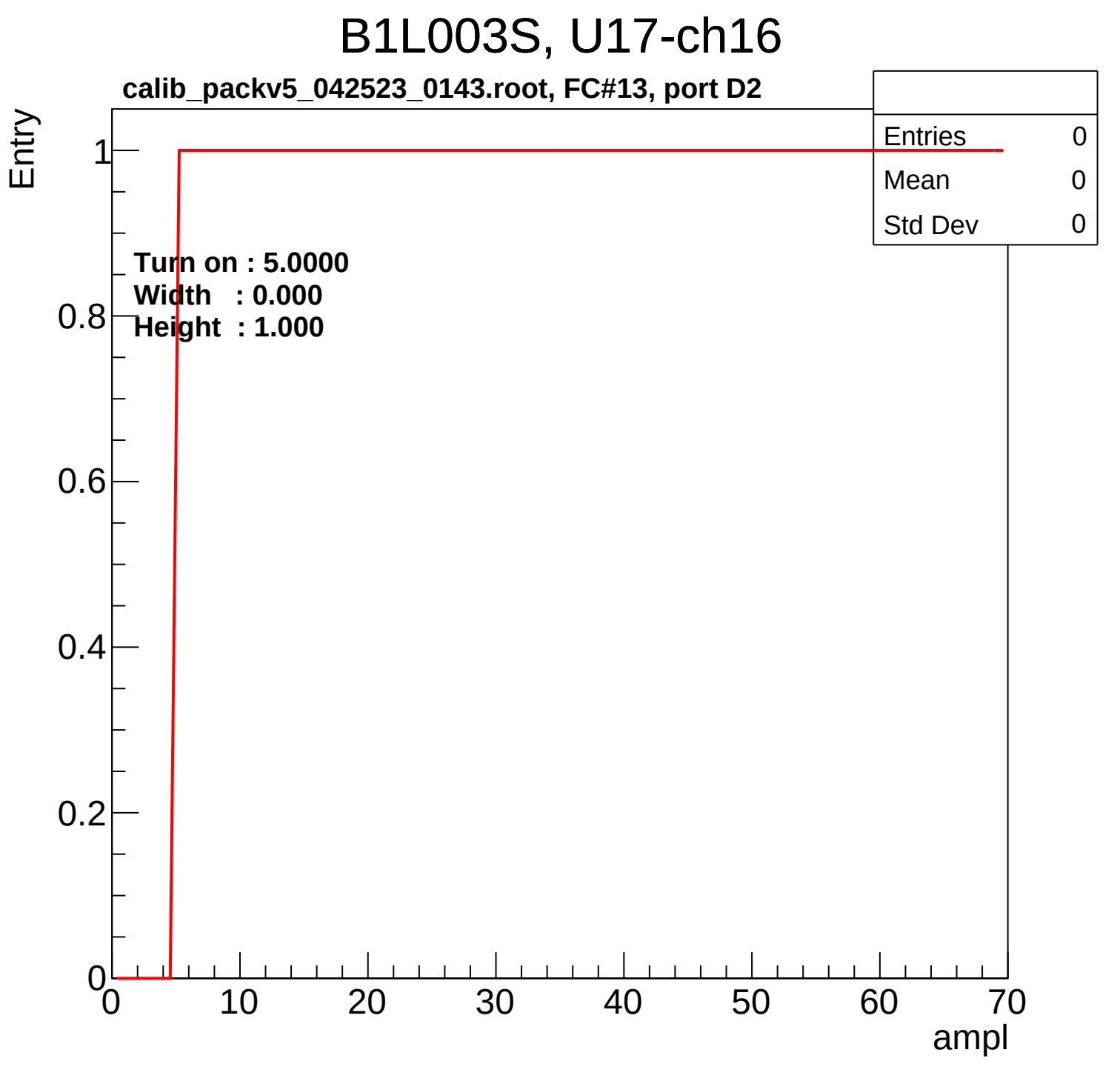
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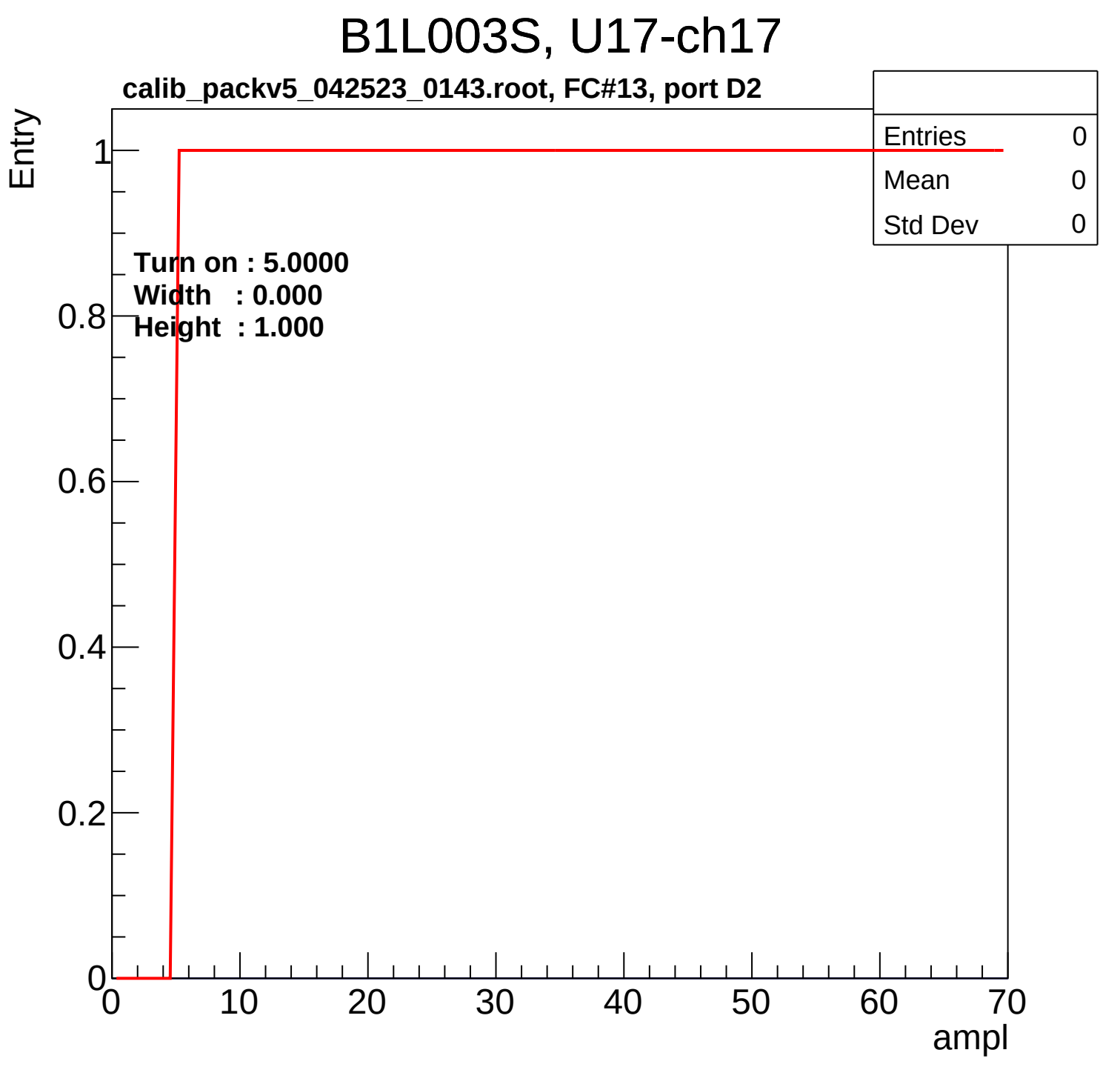
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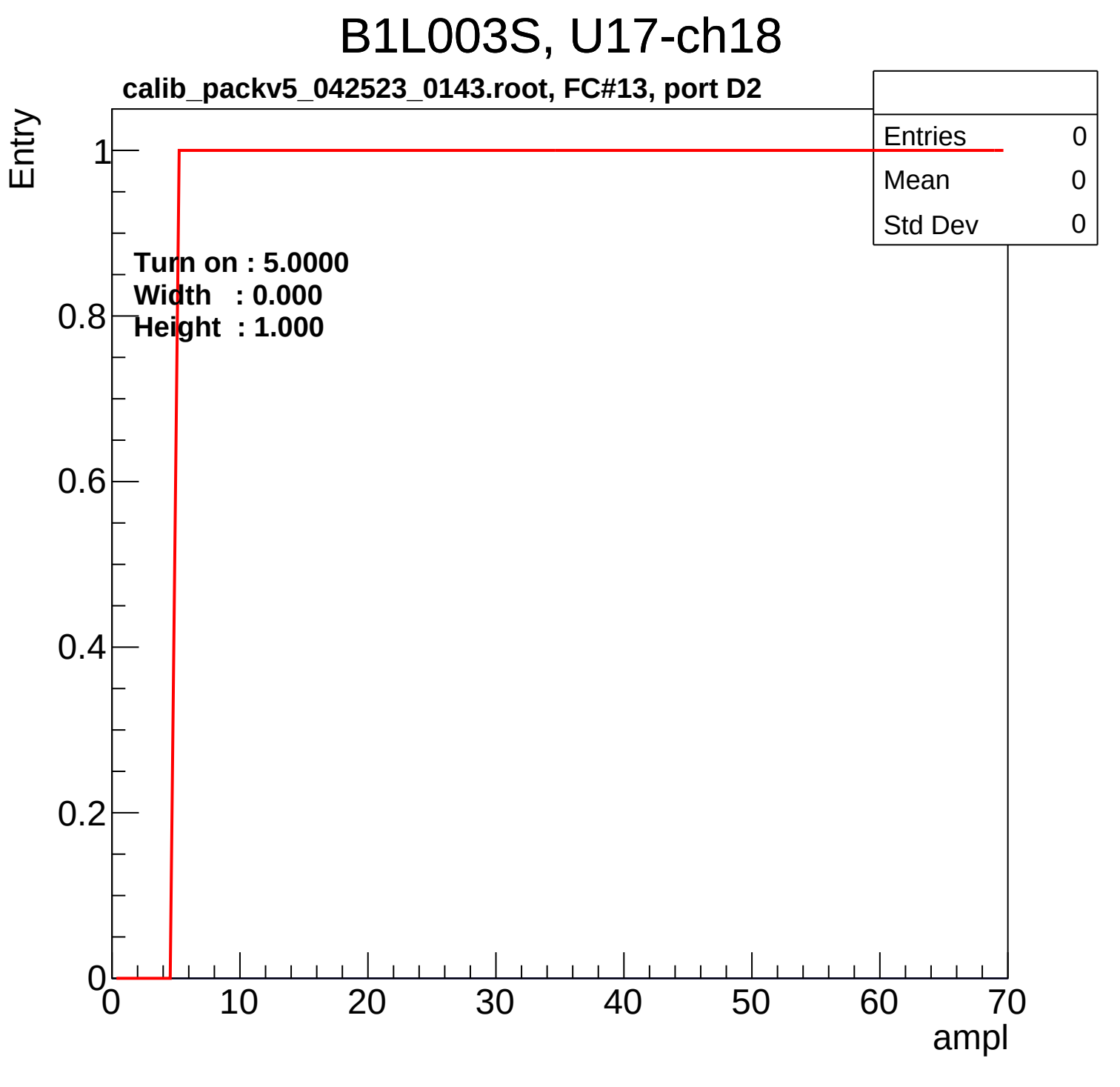
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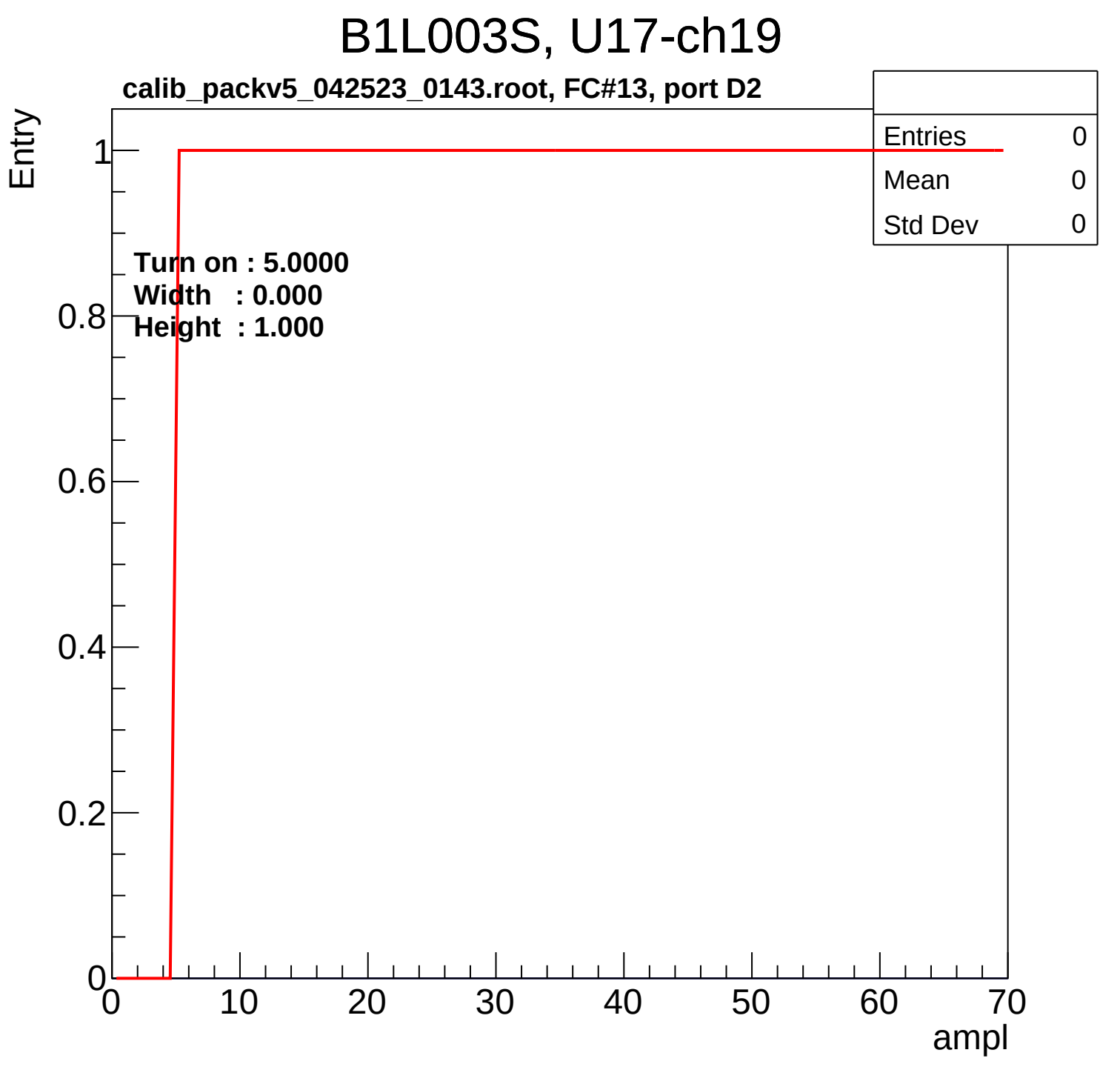
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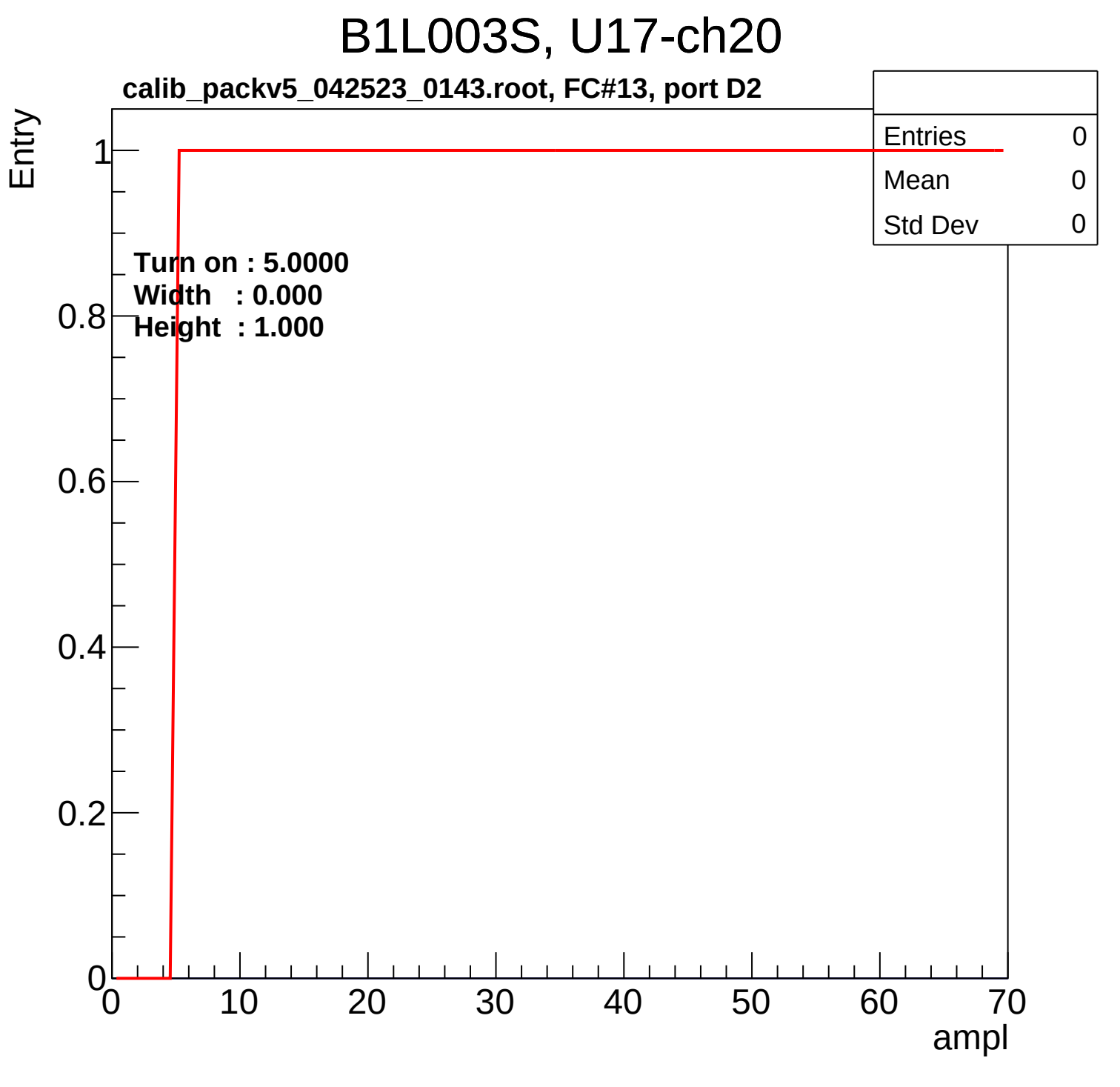
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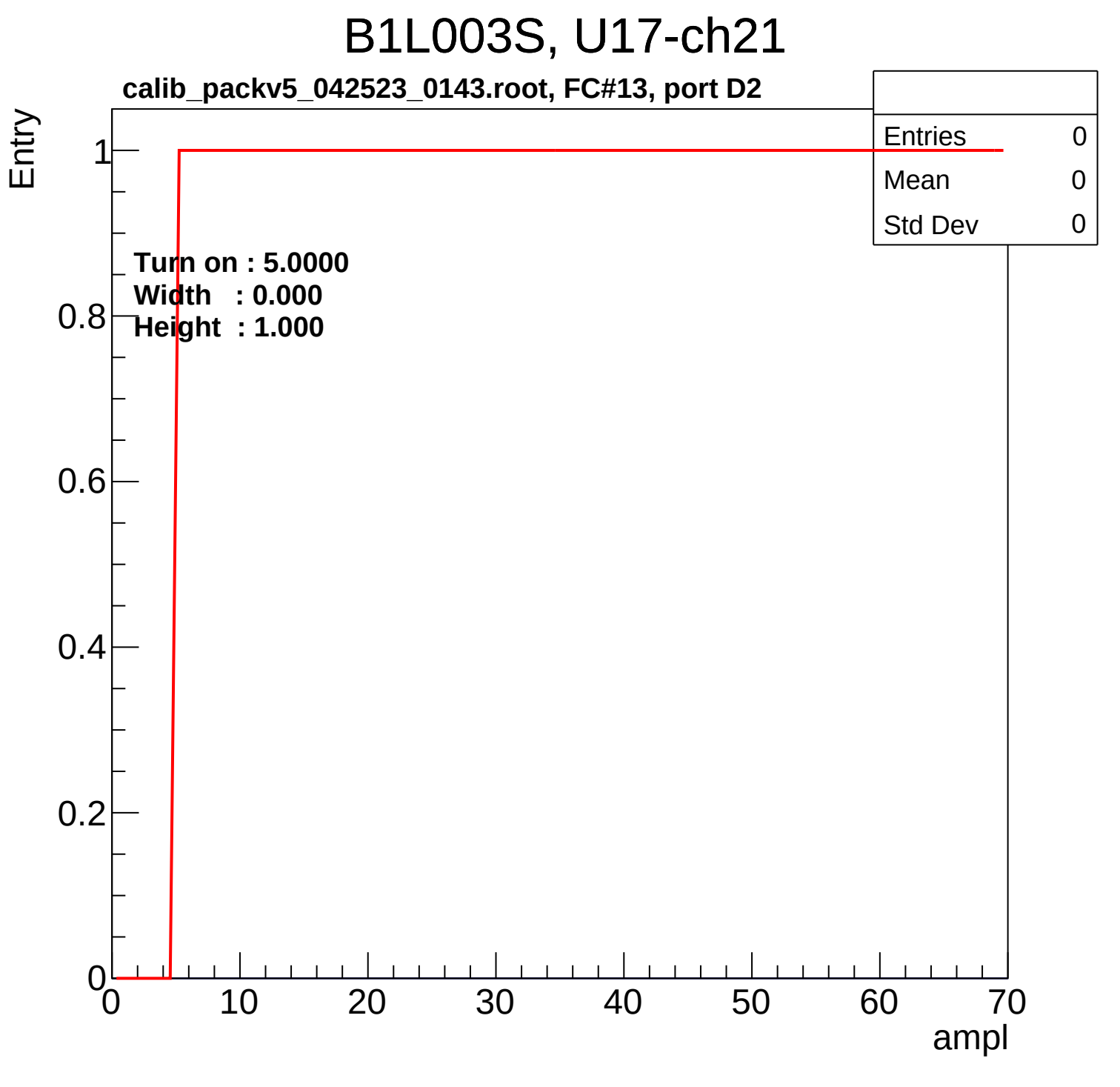
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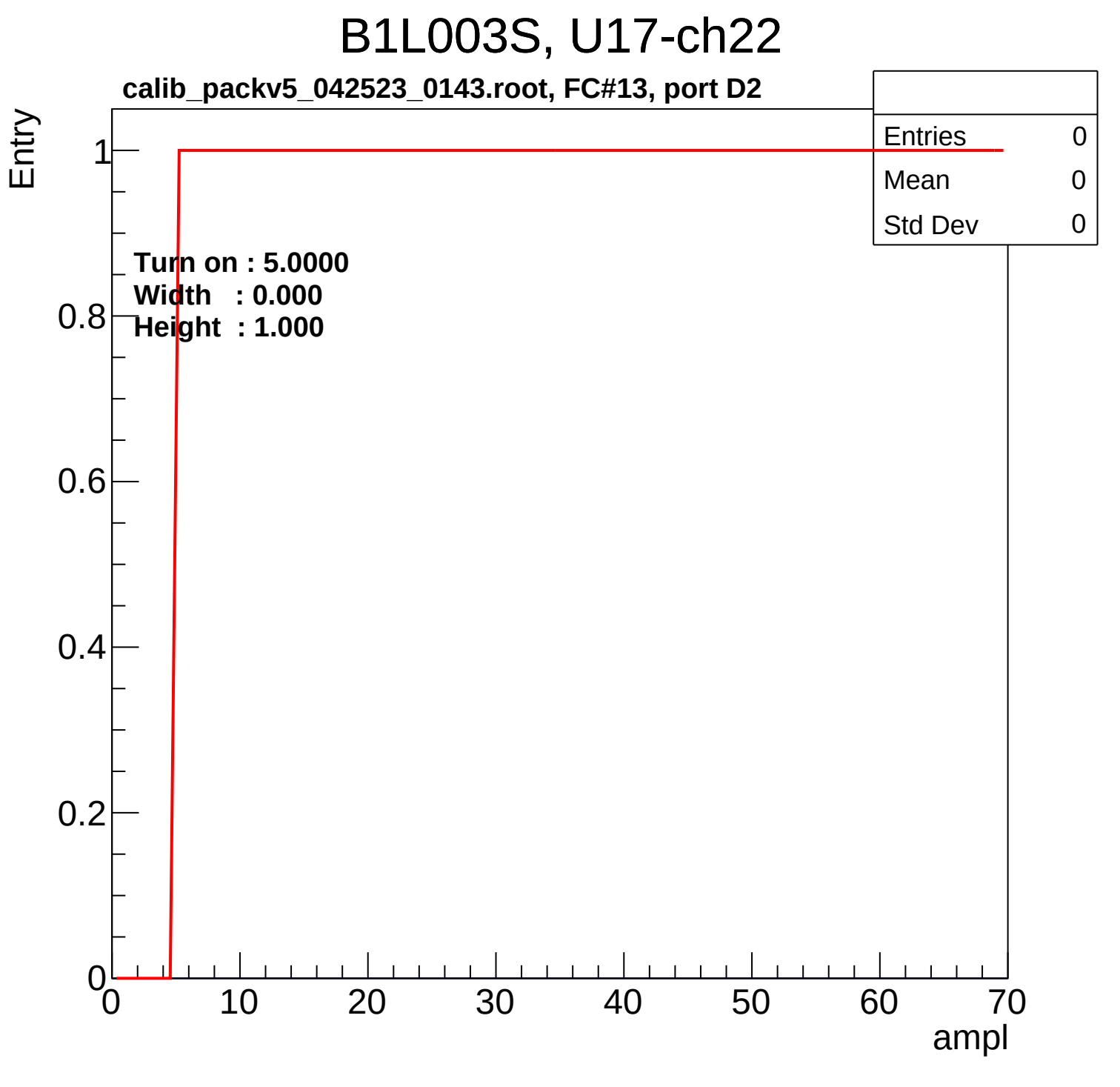
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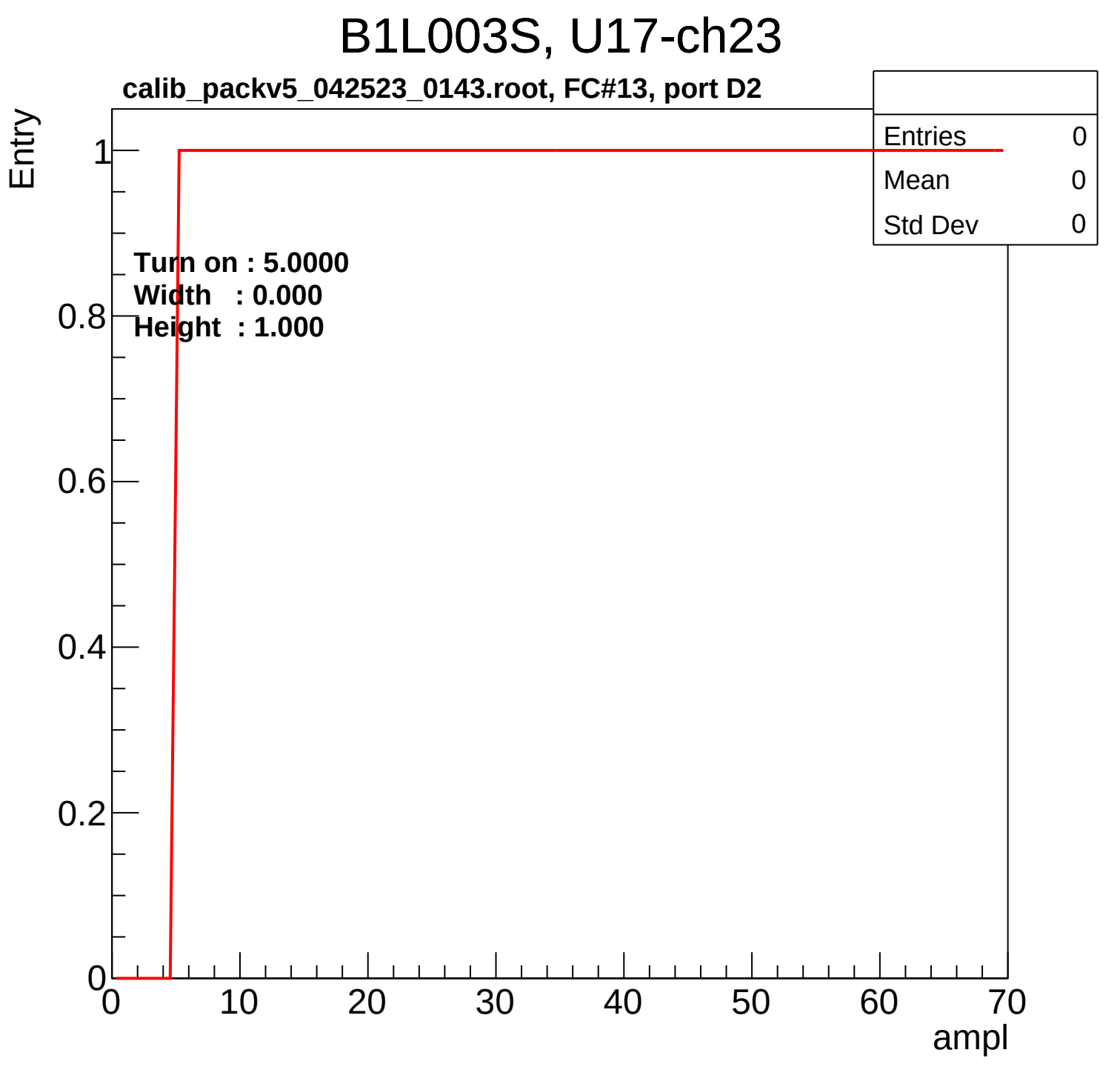
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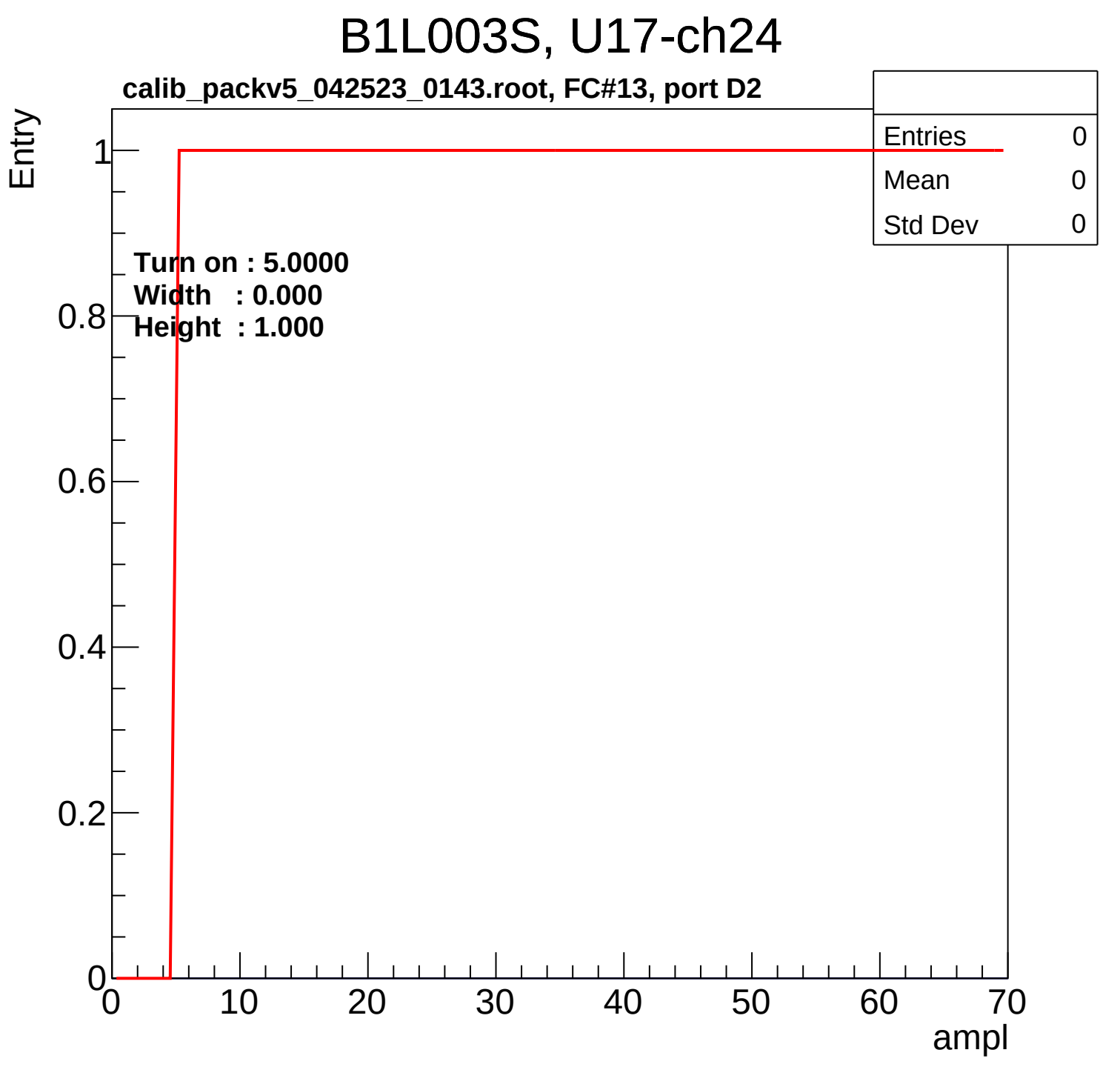
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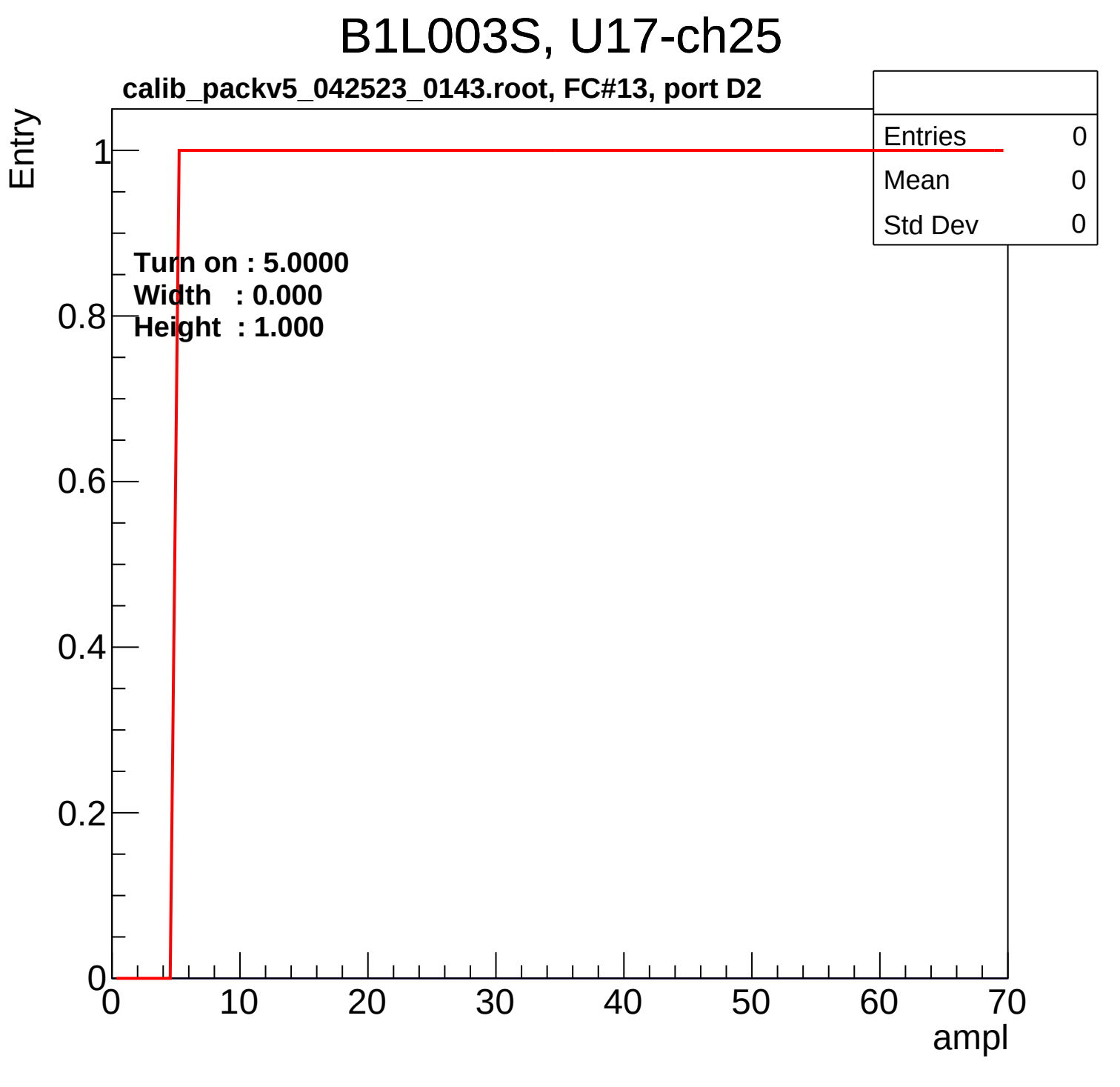
B1L003S, U17-ch25
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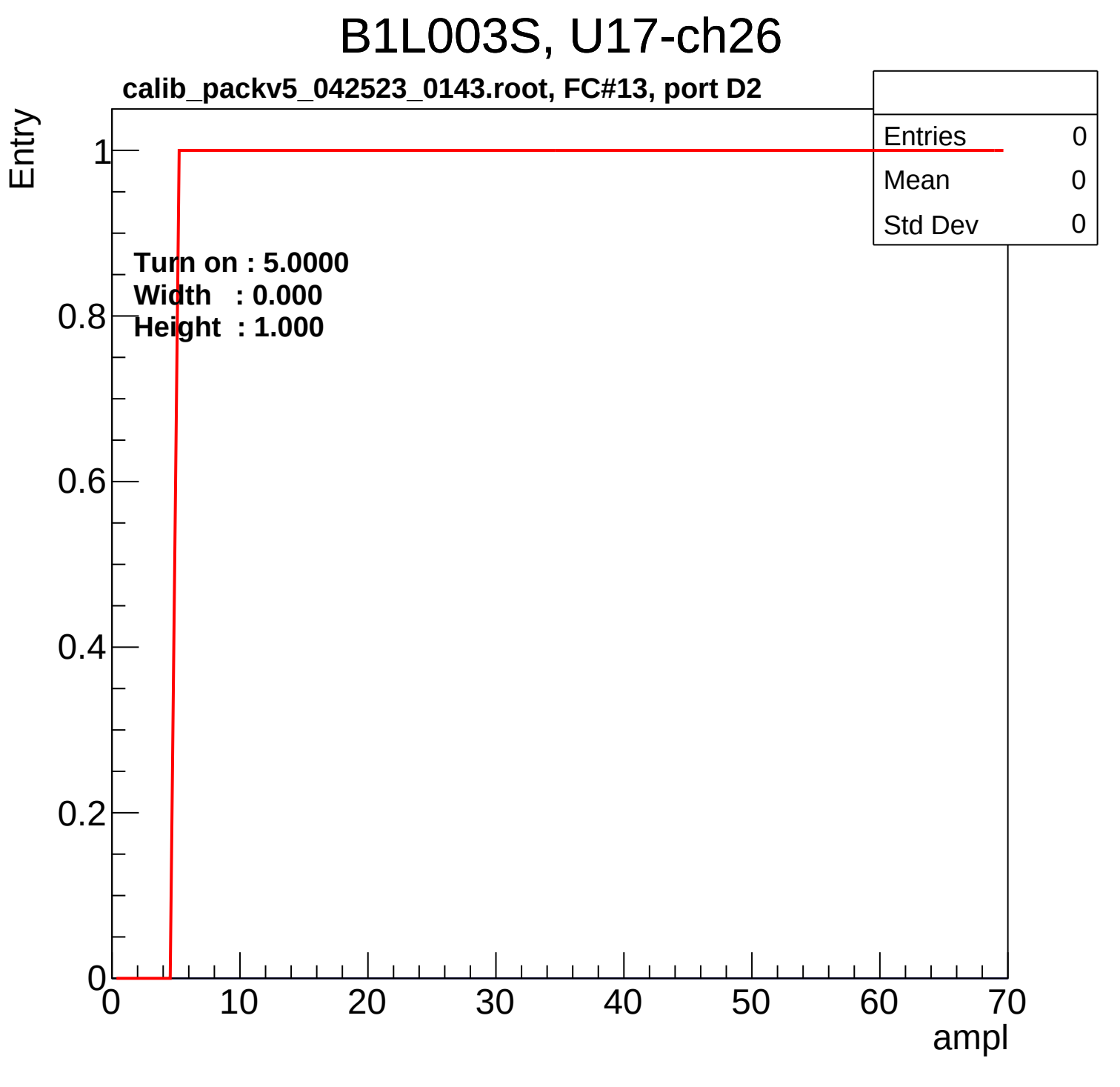
B1L003S, U17-ch26
calib_packv5_042523_0143.root, FC#13, port D2
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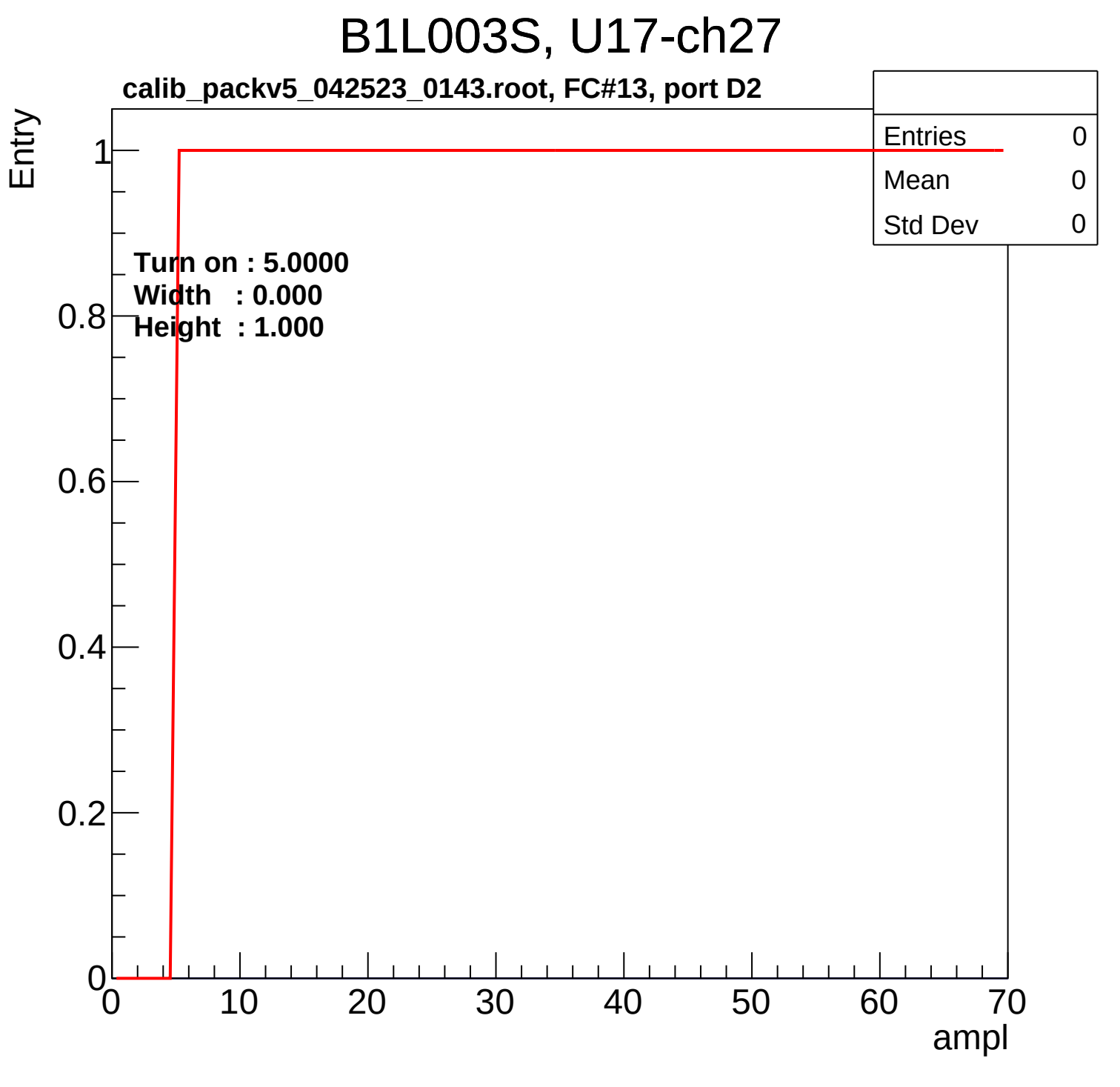
B1L003S, U17-ch27
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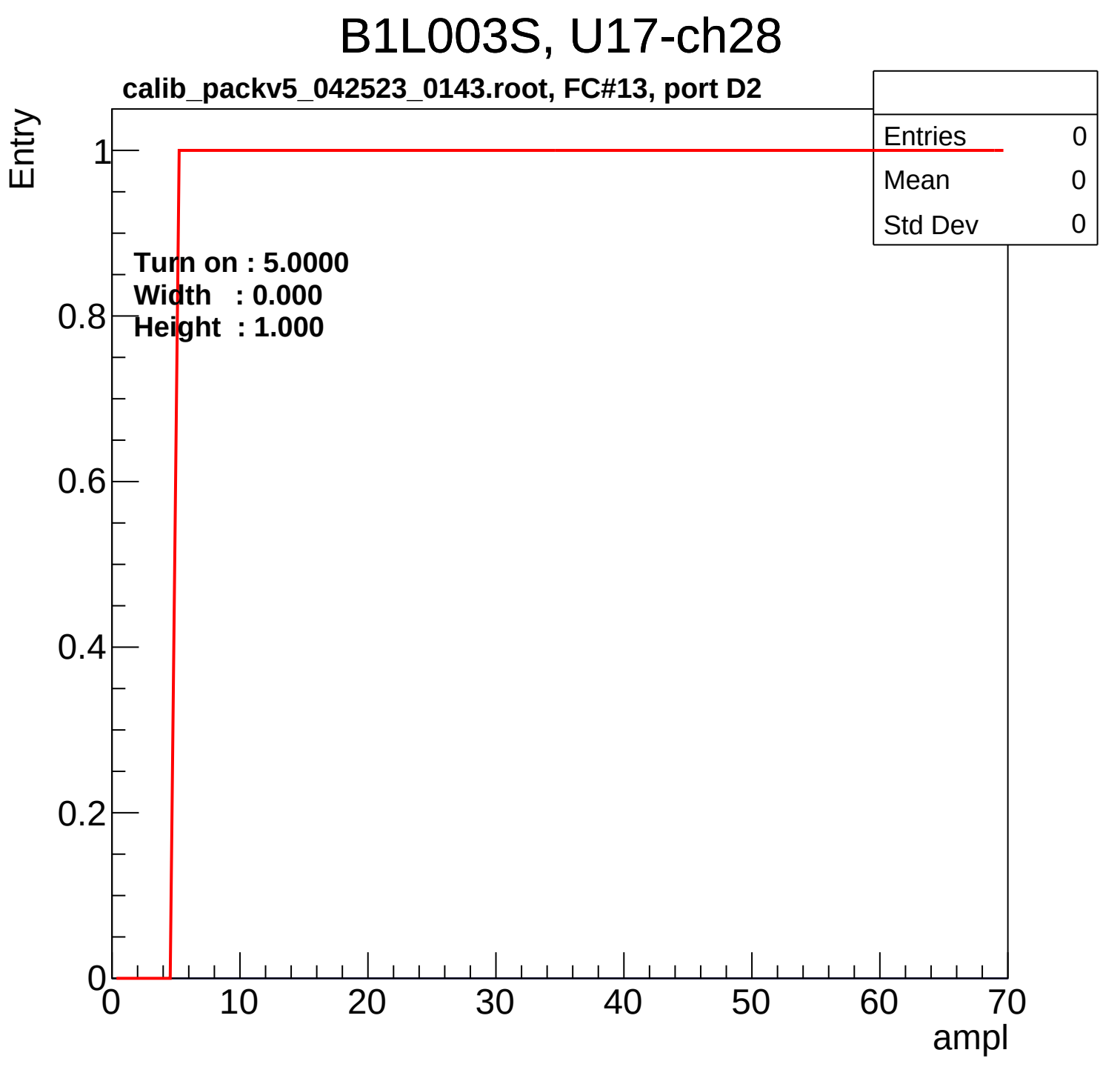
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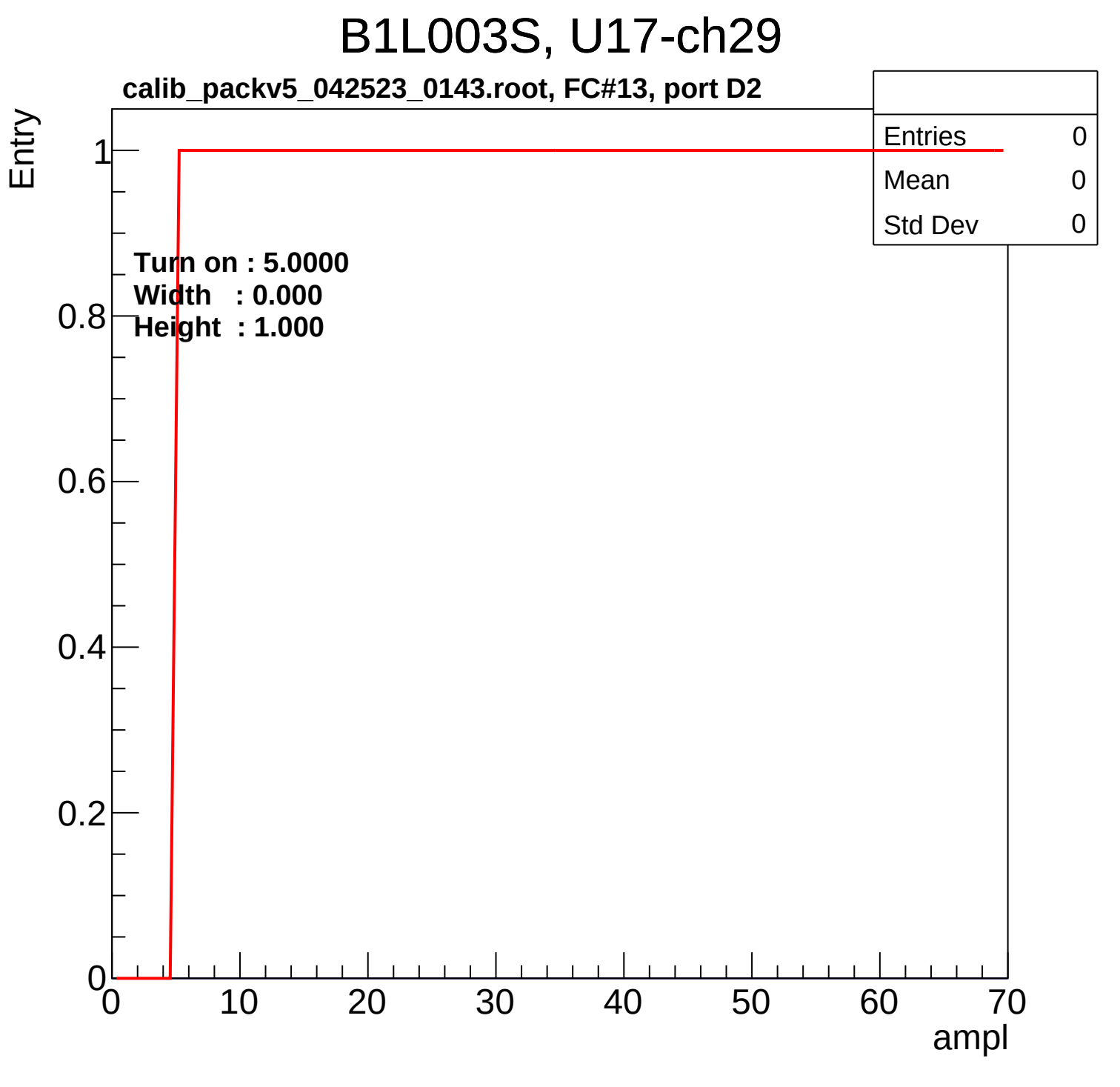
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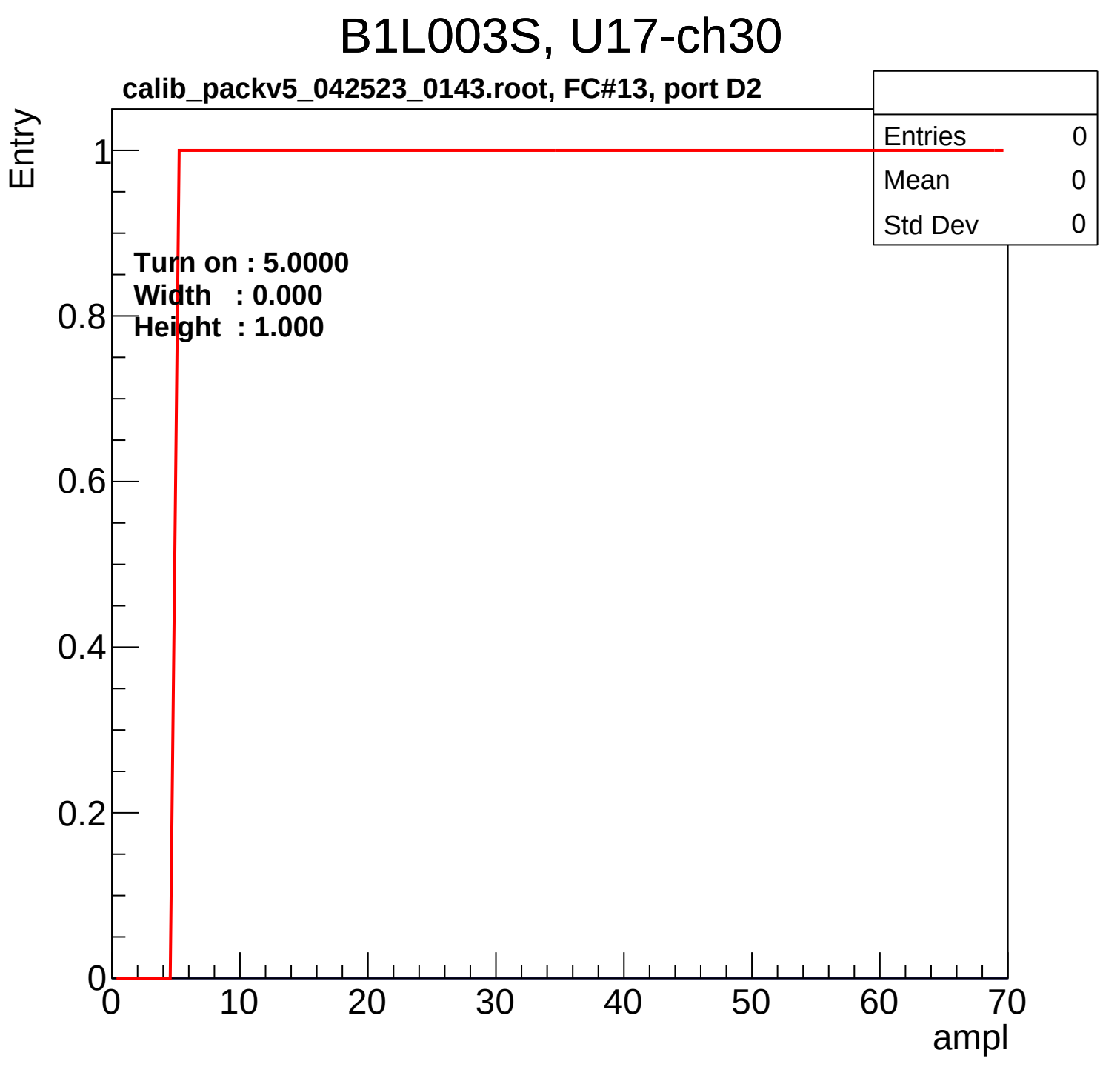
B1L003S, U17-ch30
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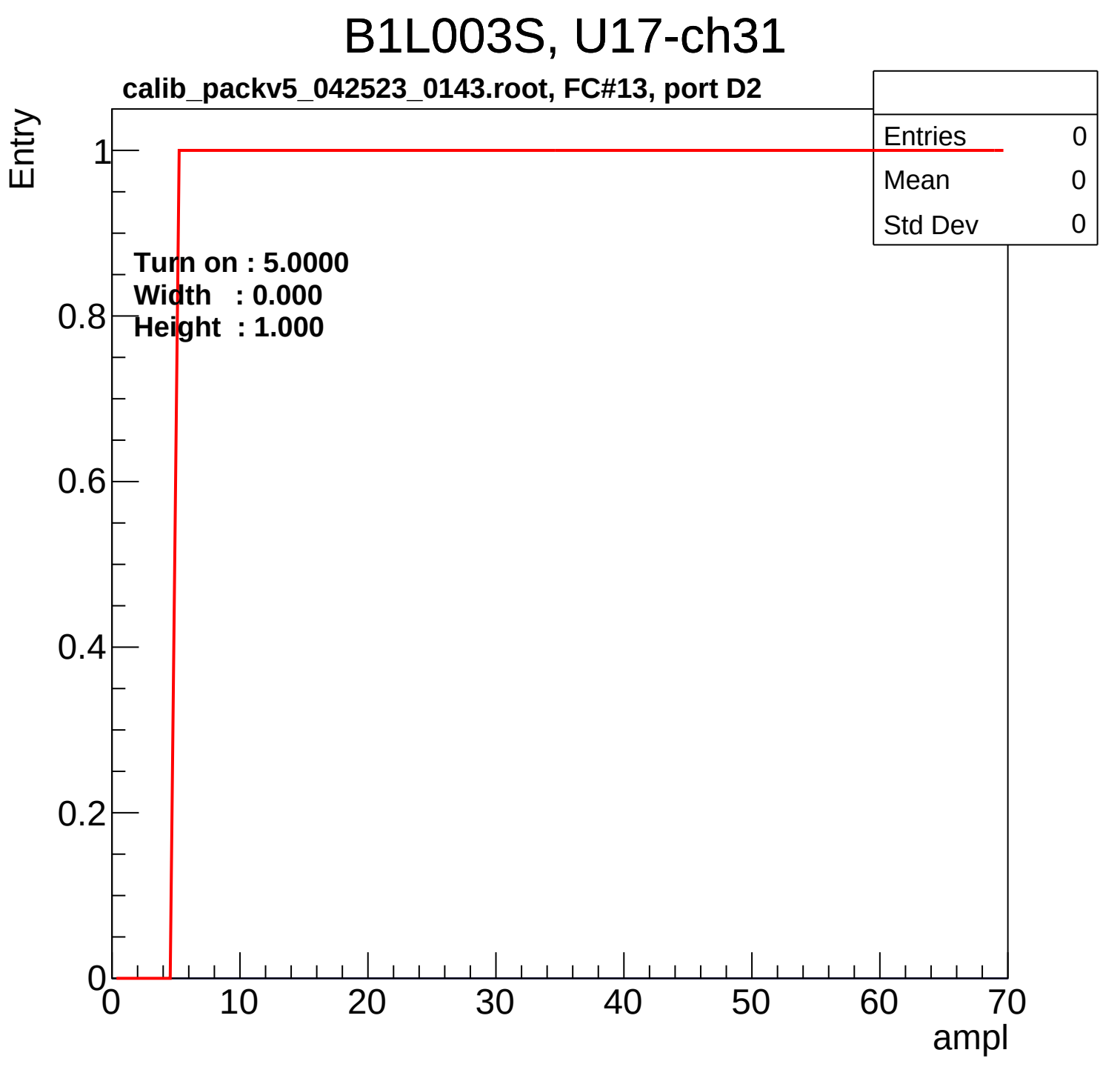
70
ampl


B1L003S, U17-ch31
calib_packv5_042523_0143.root, FC#13, port D2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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0.6
0.4
0.2
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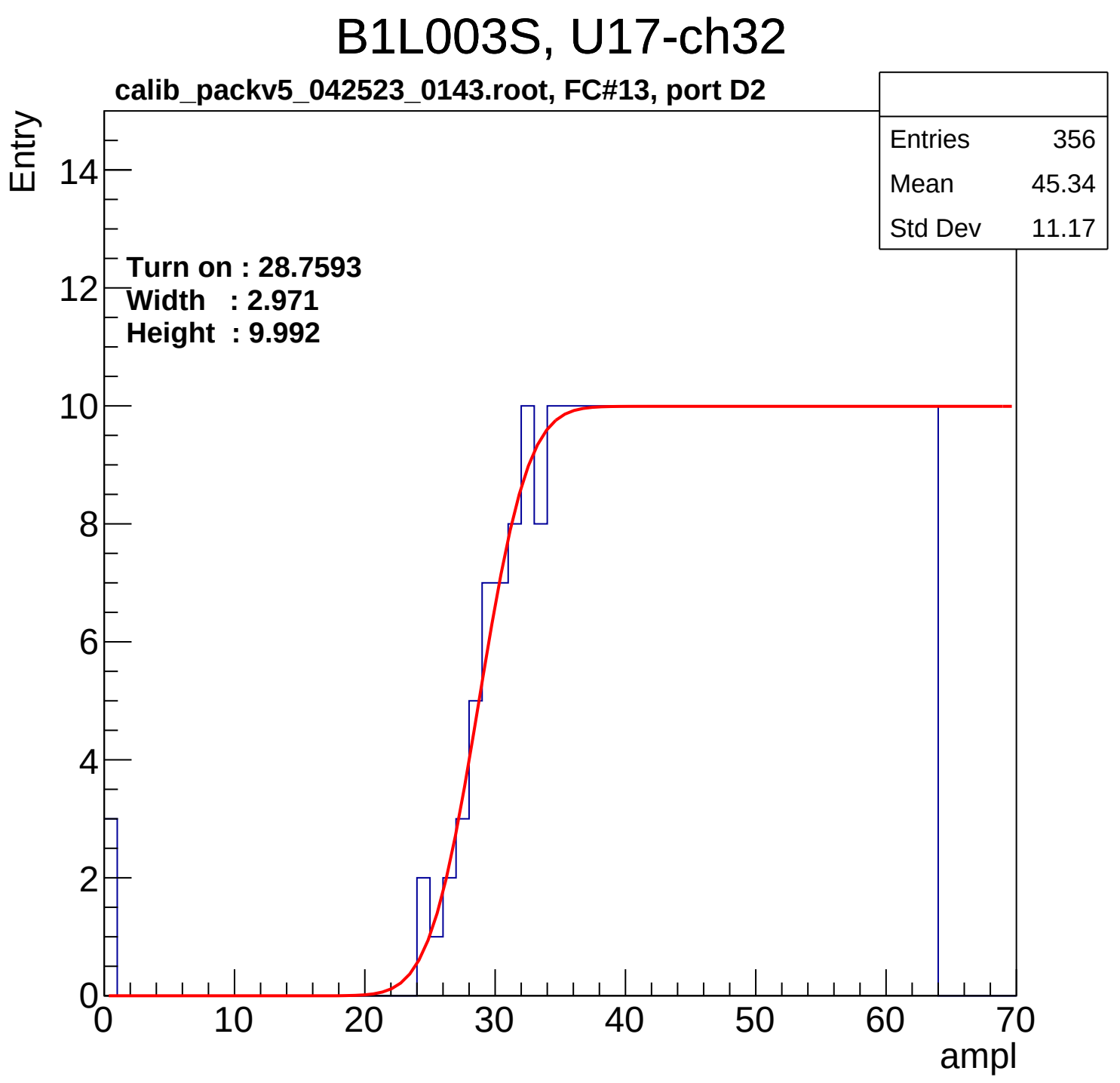
ampl


B1L003S, U17-ch32
calib_packv5_042523_0143.root, FC#13, port D2
Entries 356
Mean 45.34
Std Dev 11.17
Turn on : 28.7593
Width : 2.971
Height : 9.992
Entry
ampl
0
2
4
6
8
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12
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0
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60
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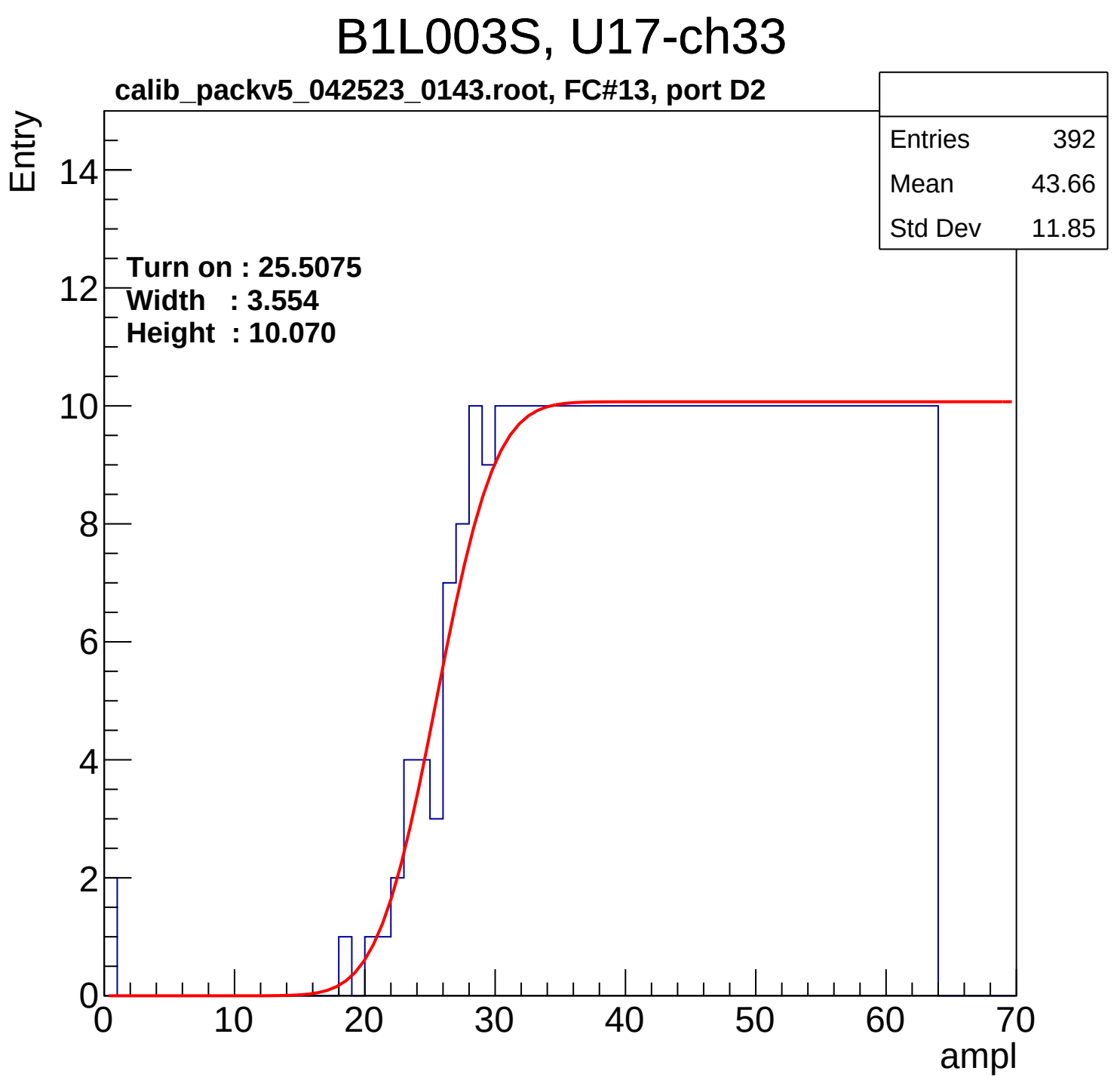
B1L003S, U17-ch33
calib_packv5_042523_0143.root, FC#13, port D2
Entries 392
Mean 43.66
Std Dev 11.85
Turn on : 25.5075
Width : 3.554
Height : 10.070
Entry
ampl
0
2
4
6
8
10
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0
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60
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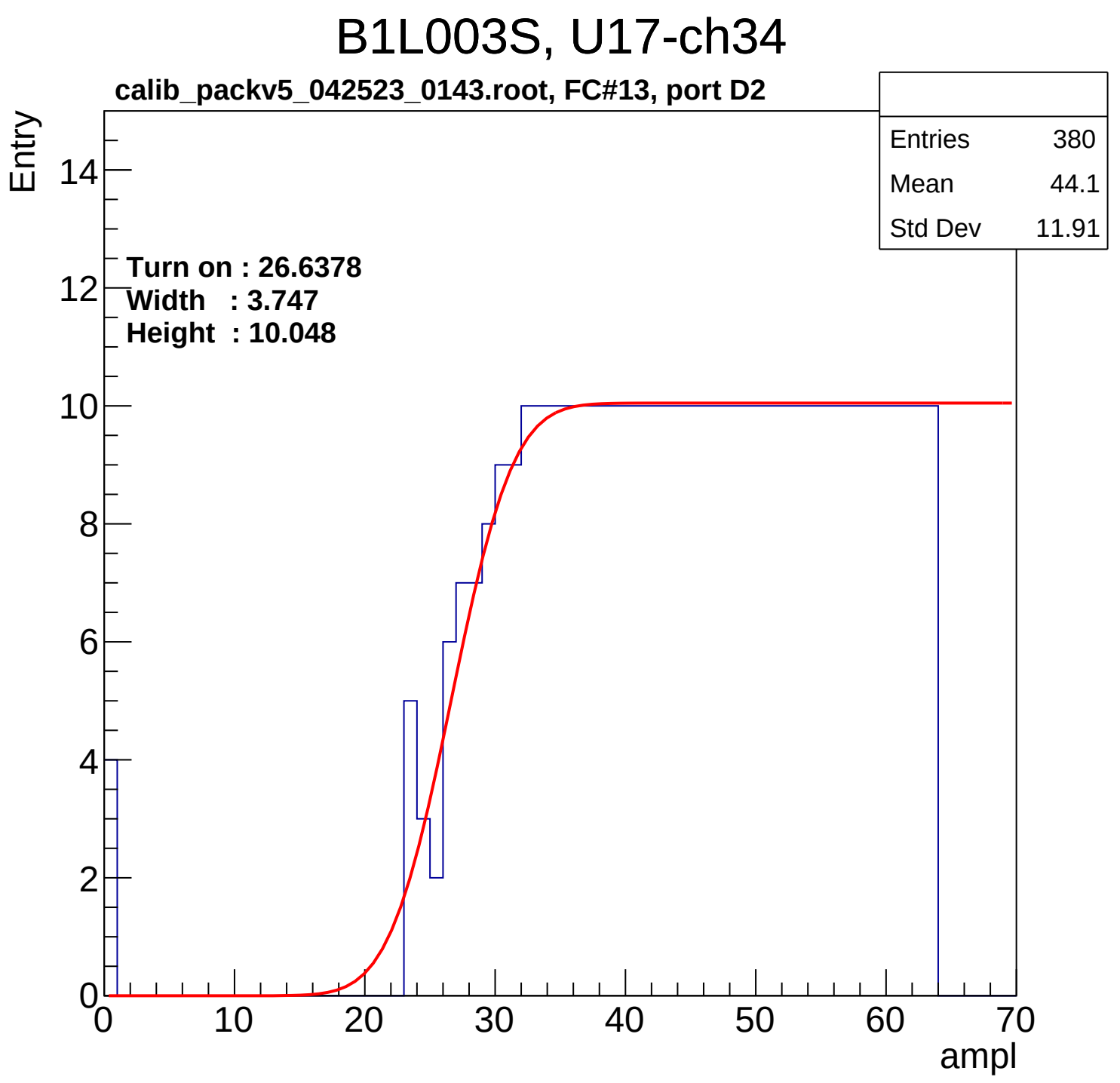
B1L003S, U17-ch34
calib_packv5_042523_0143.root, FC#13, port D2
Entries 380
Mean 44.1
Std Dev 11.91
Turn on : 26.6378
Width : 3.747
Height : 10.048
Entry
ampl
0
2
4
6
8
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60
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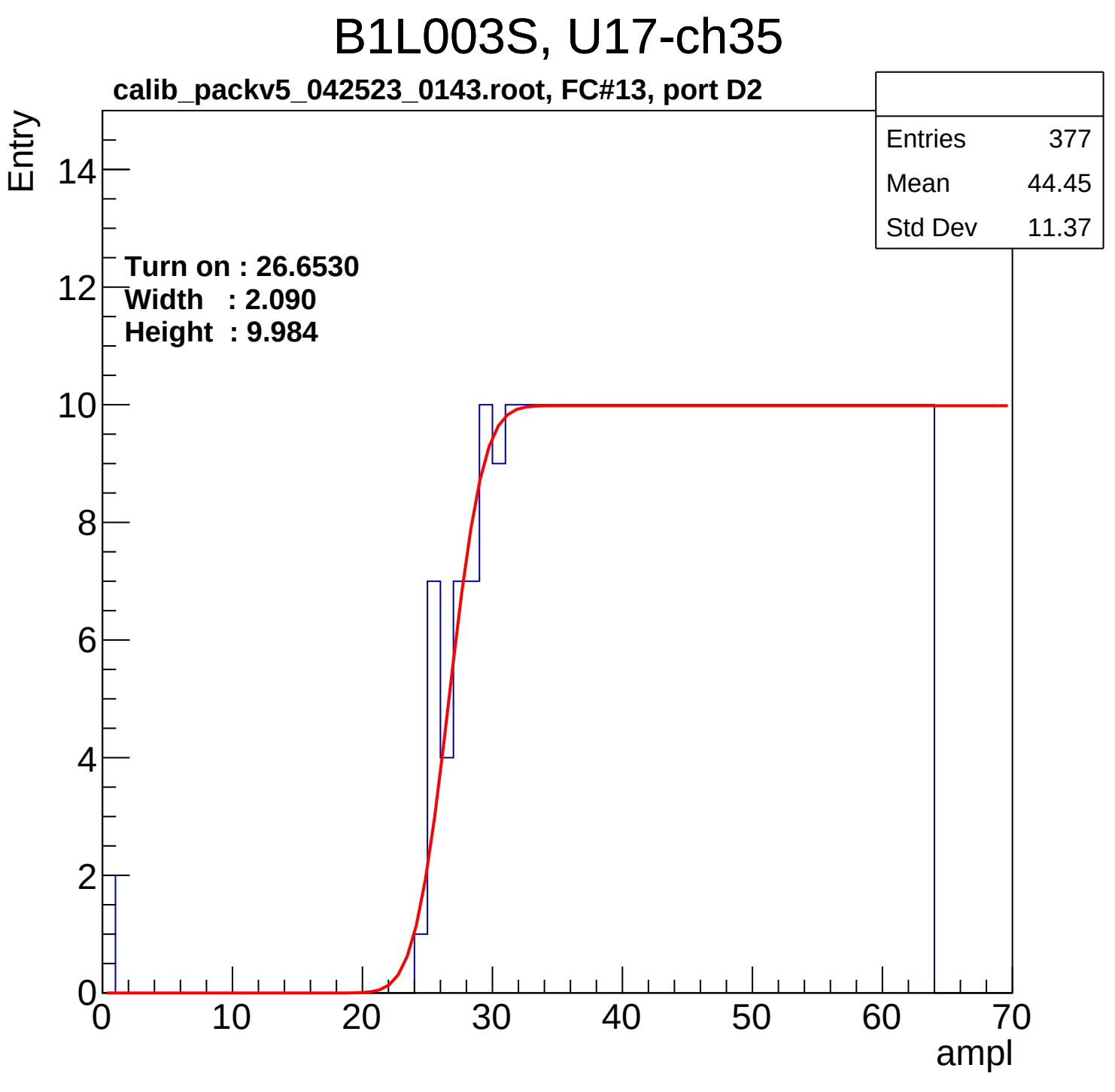
B1L003S, U17-ch35
calib_packv5_042523_0143.root, FC#13, port D2
Entries 377
Mean 44.45
Std Dev 11.37
Turn on : 26.6530
Width : 2.090
Height : 9.984
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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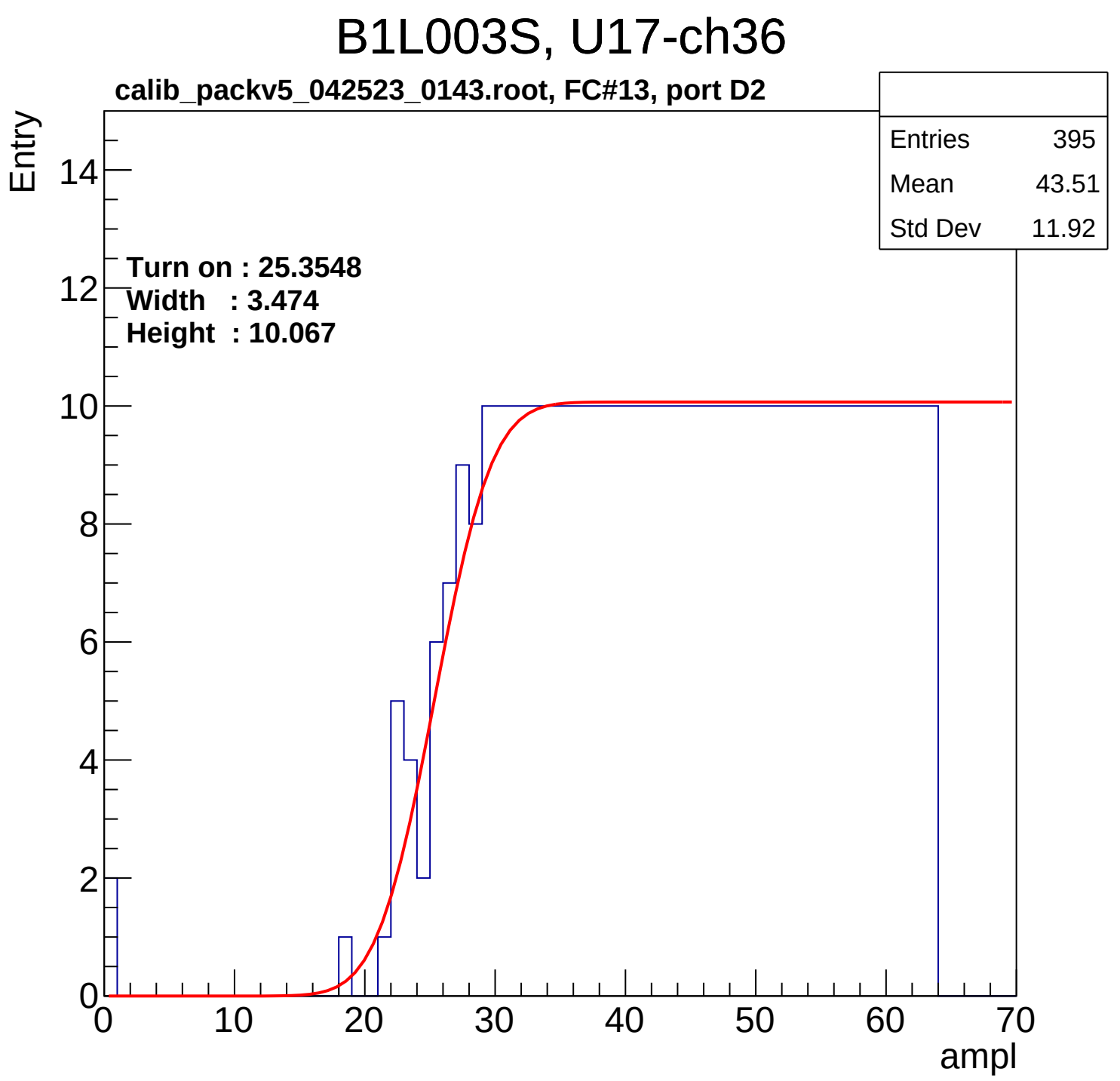
B1L003S, U17-ch36
calib_packv5_042523_0143.root, FC#13, port D2
Entries 395
Mean 43.51
Std Dev 11.92
Turn on : 25.3548
Width : 3.474
Height : 10.067
Entry
ampl
0
2
4
6
8
10
12
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0
10
20
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40
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60
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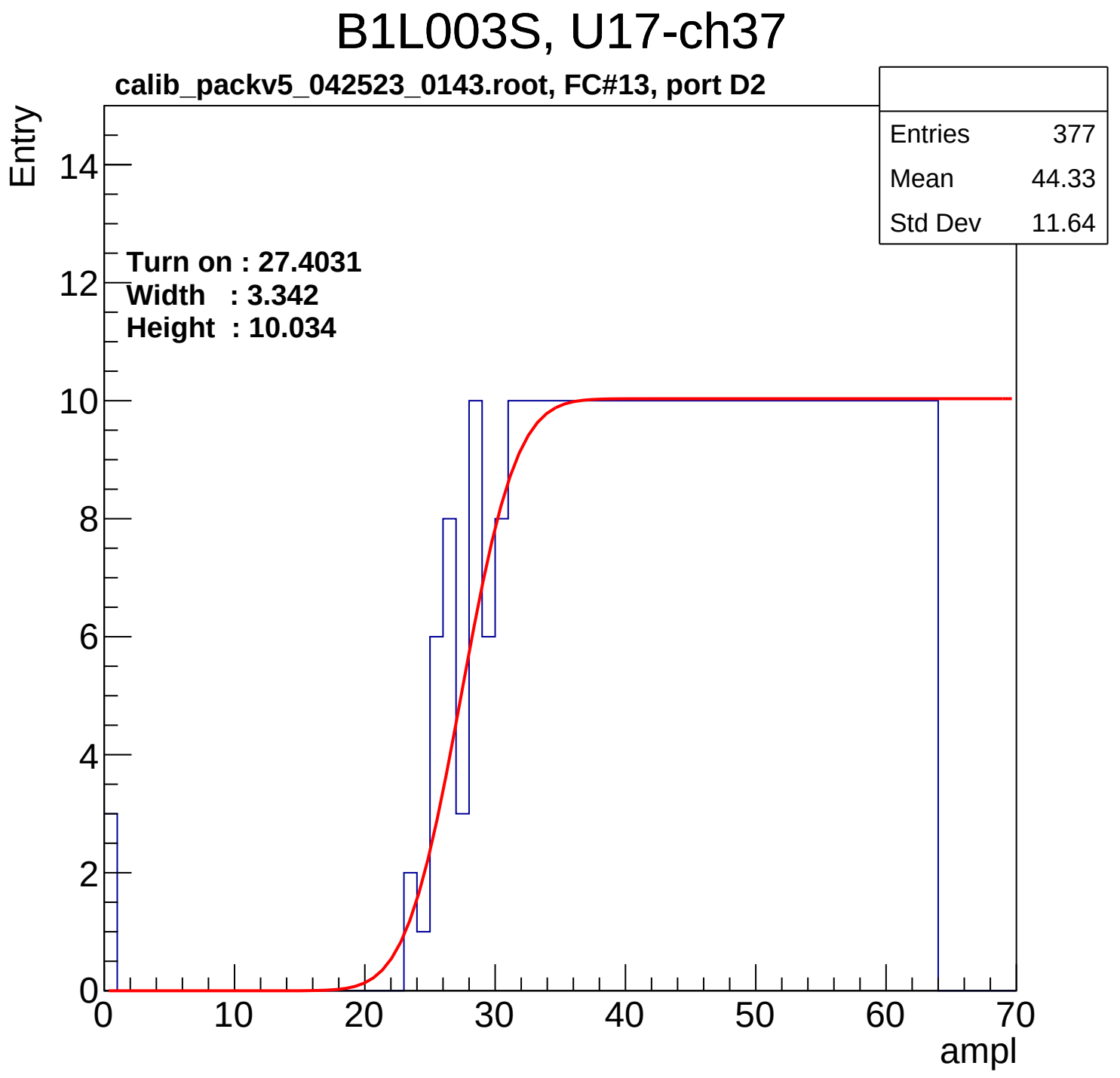
B1L003S, U17-ch37
calib_packv5_042523_0143.root, FC#13, port D2
Entries 377
Mean 44.33
Std Dev 11.64
Turn on : 27.4031
Width : 3.342
Height : 10.034
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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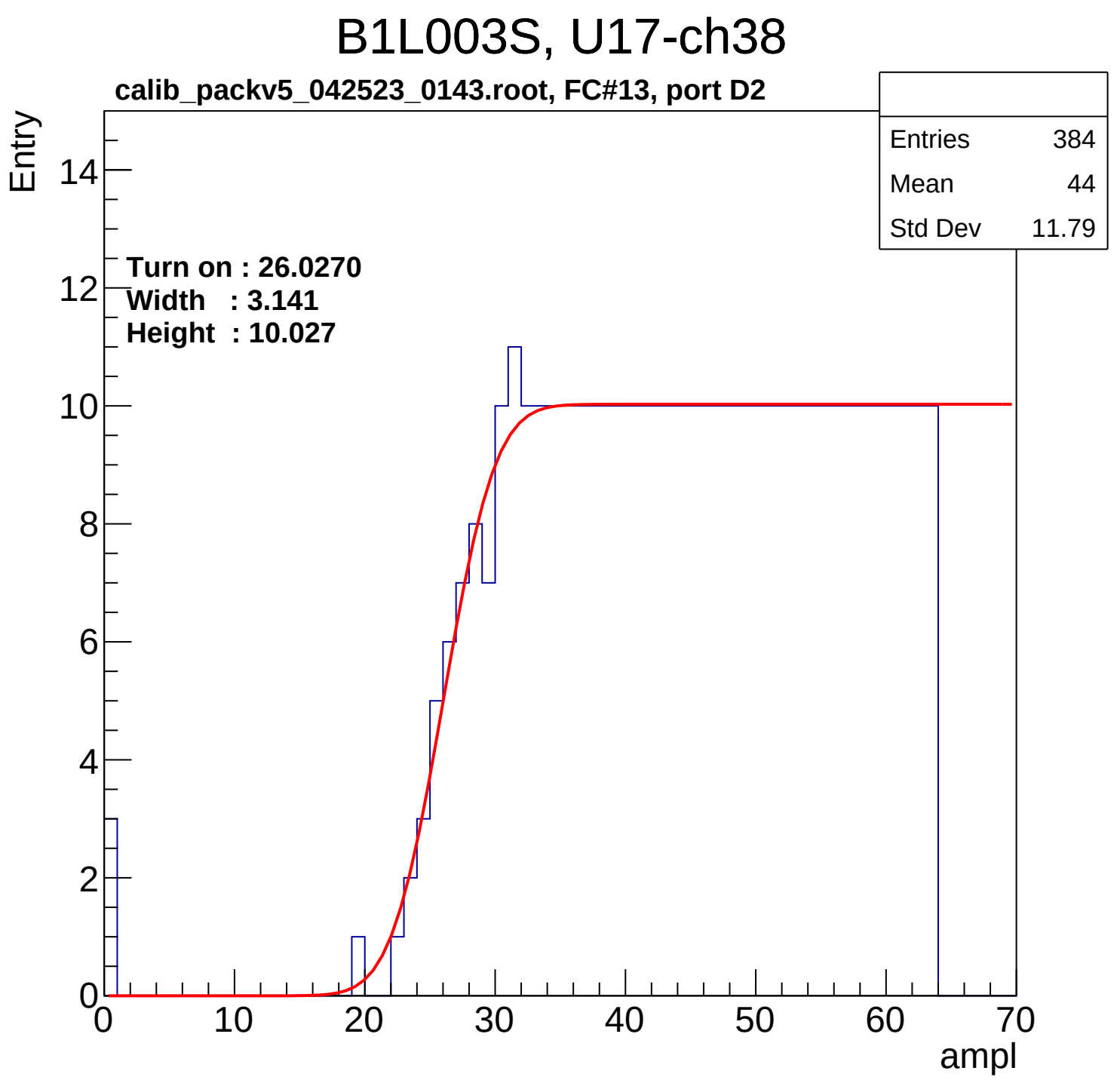
B1L003S, U17-ch38
calib_packv5_042523_0143.root, FC#13, port D2
Entries 384
Mean 44
Std Dev 11.79
Turn on : 26.0270
Width : 3.141
Height : 10.027
Entry
ampl
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2
4
6
8
10
12
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0
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60
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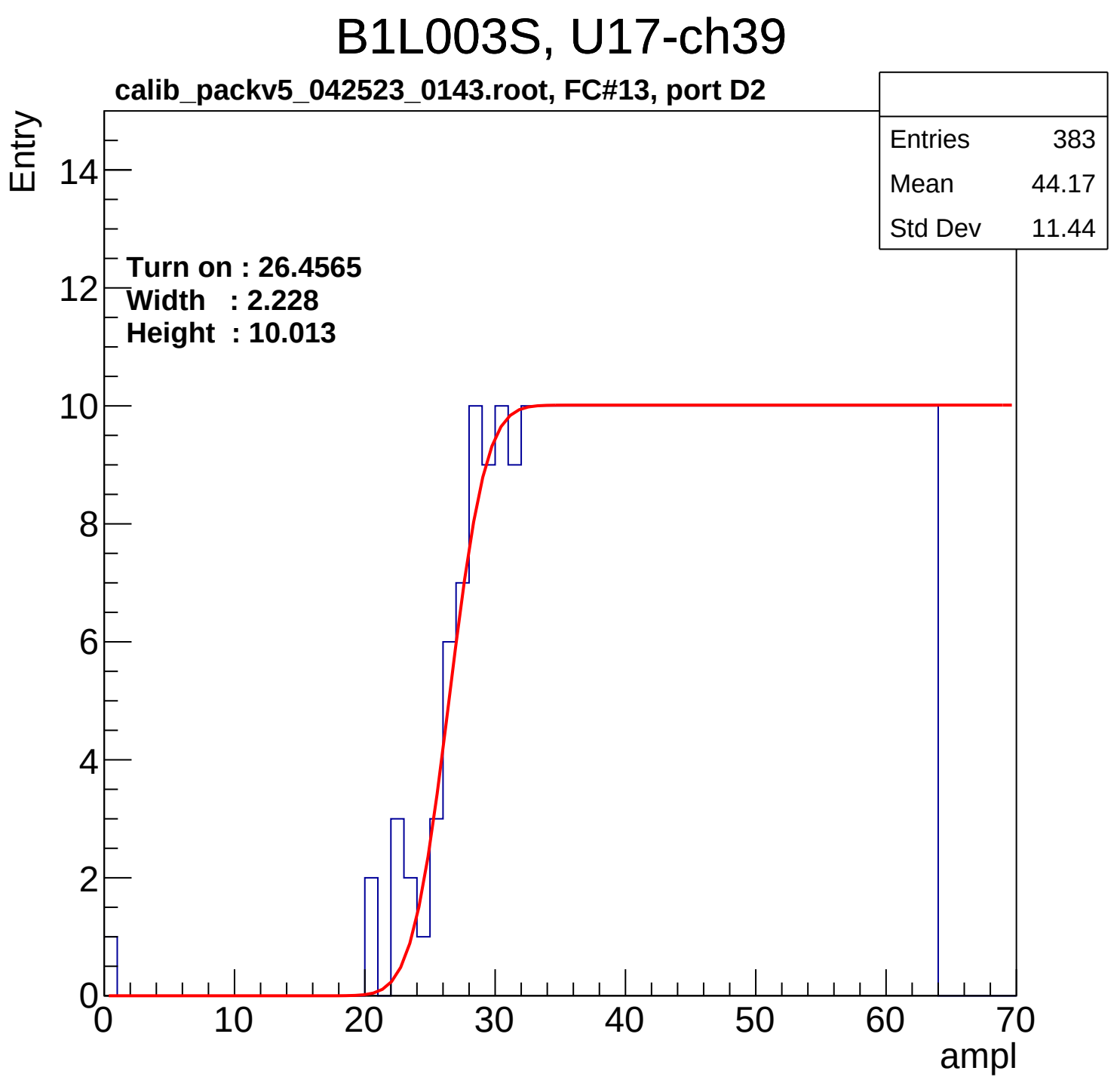
B1L003S, U17-ch39
calib_packv5_042523_0143.root, FC#13, port D2
Entries 383
Mean 44.17
Std Dev 11.44
Turn on : 26.4565
Width : 2.228
Height : 10.013
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
50
60
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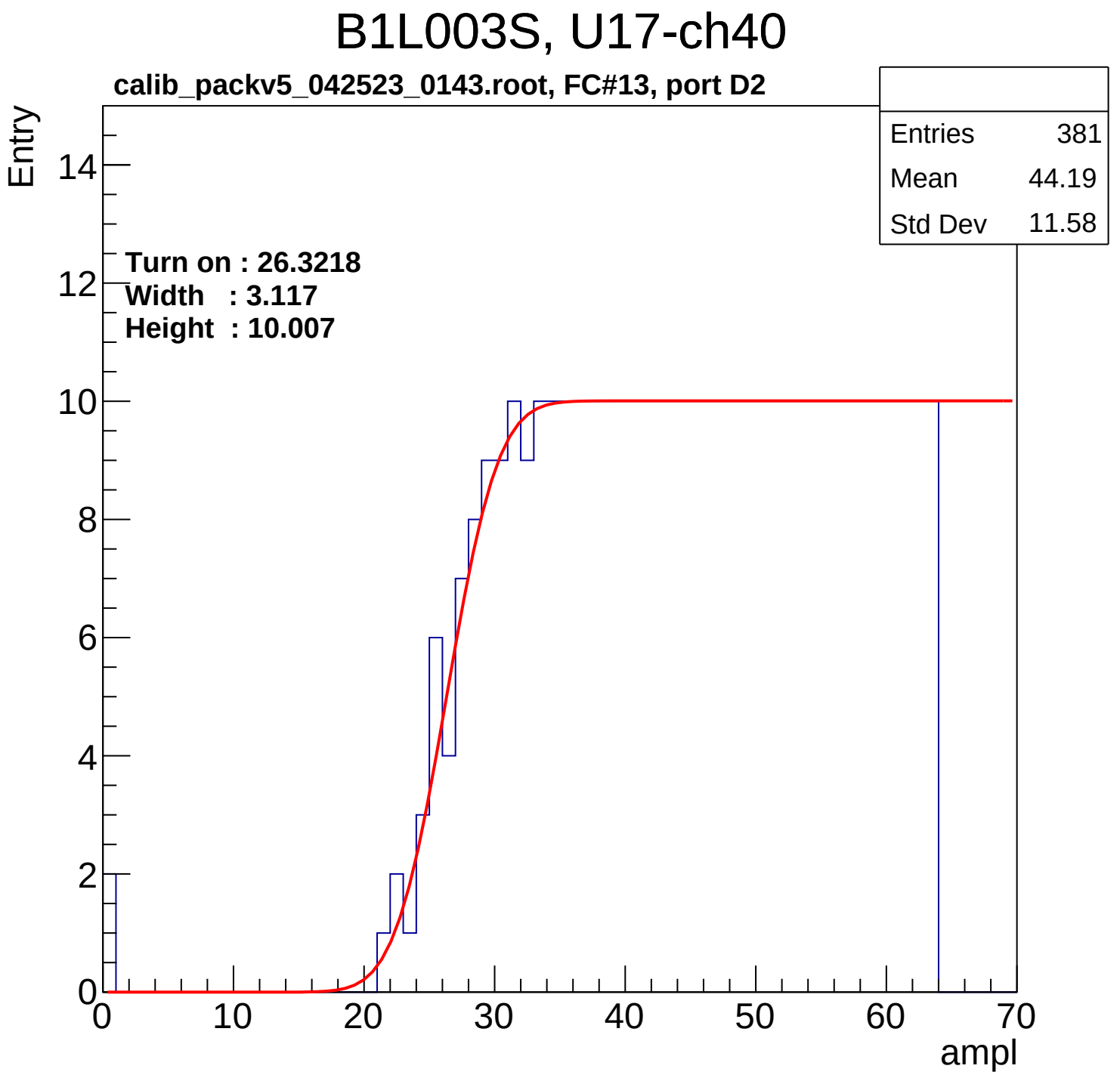
B1L003S, U17-ch40
calib_packv5_042523_0143.root, FC#13, port D2
Entries 381
Mean 44.19
Std Dev 11.58
Turn on : 26.3218
Width : 3.117
Height : 10.007
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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40
50
60
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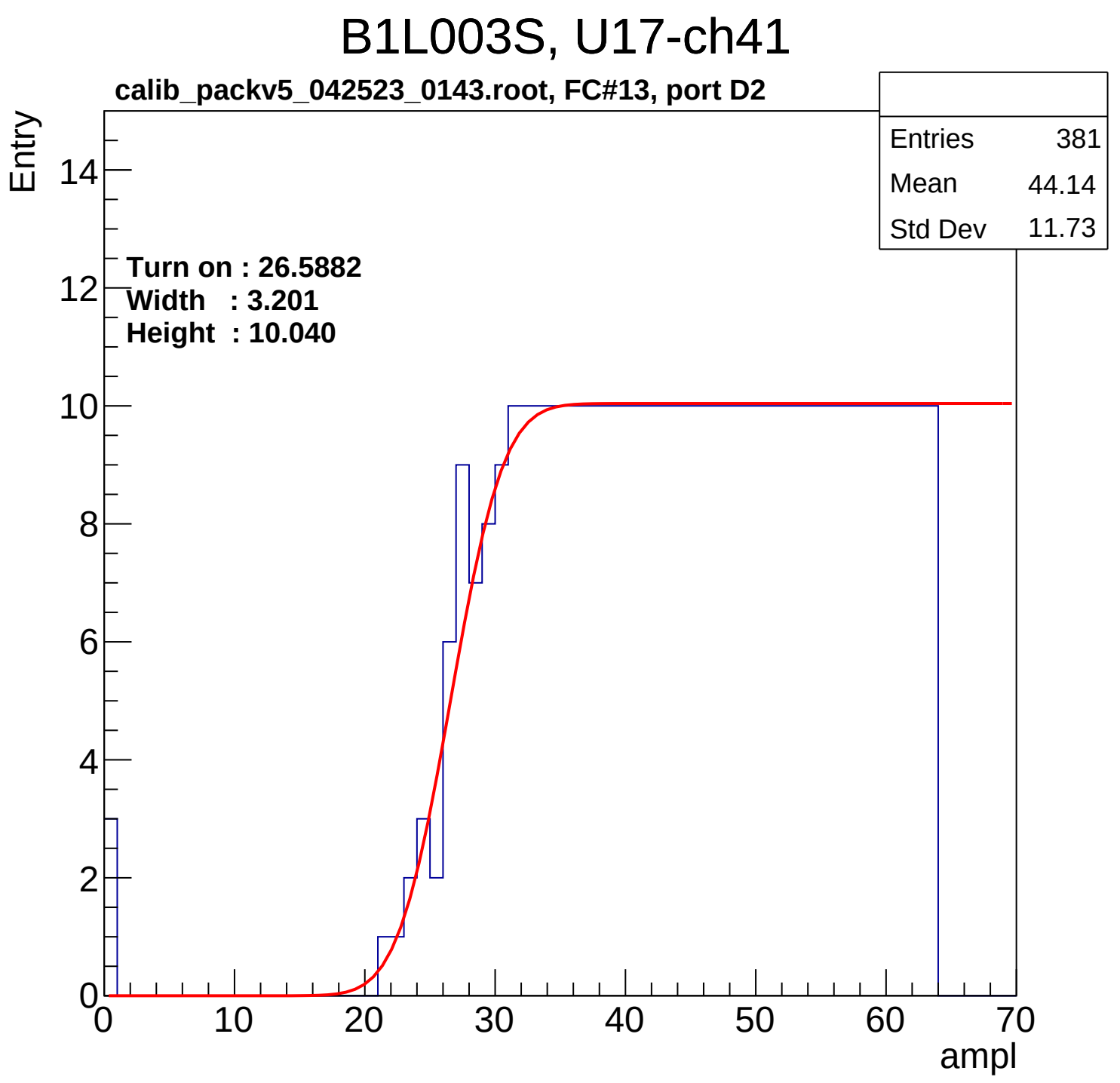
B1L003S, U17-ch41
calib_packv5_042523_0143.root, FC#13, port D2
Entries 381
Mean 44.14
Std Dev 11.73
Turn on : 26.5882
Width : 3.201
Height : 10.040
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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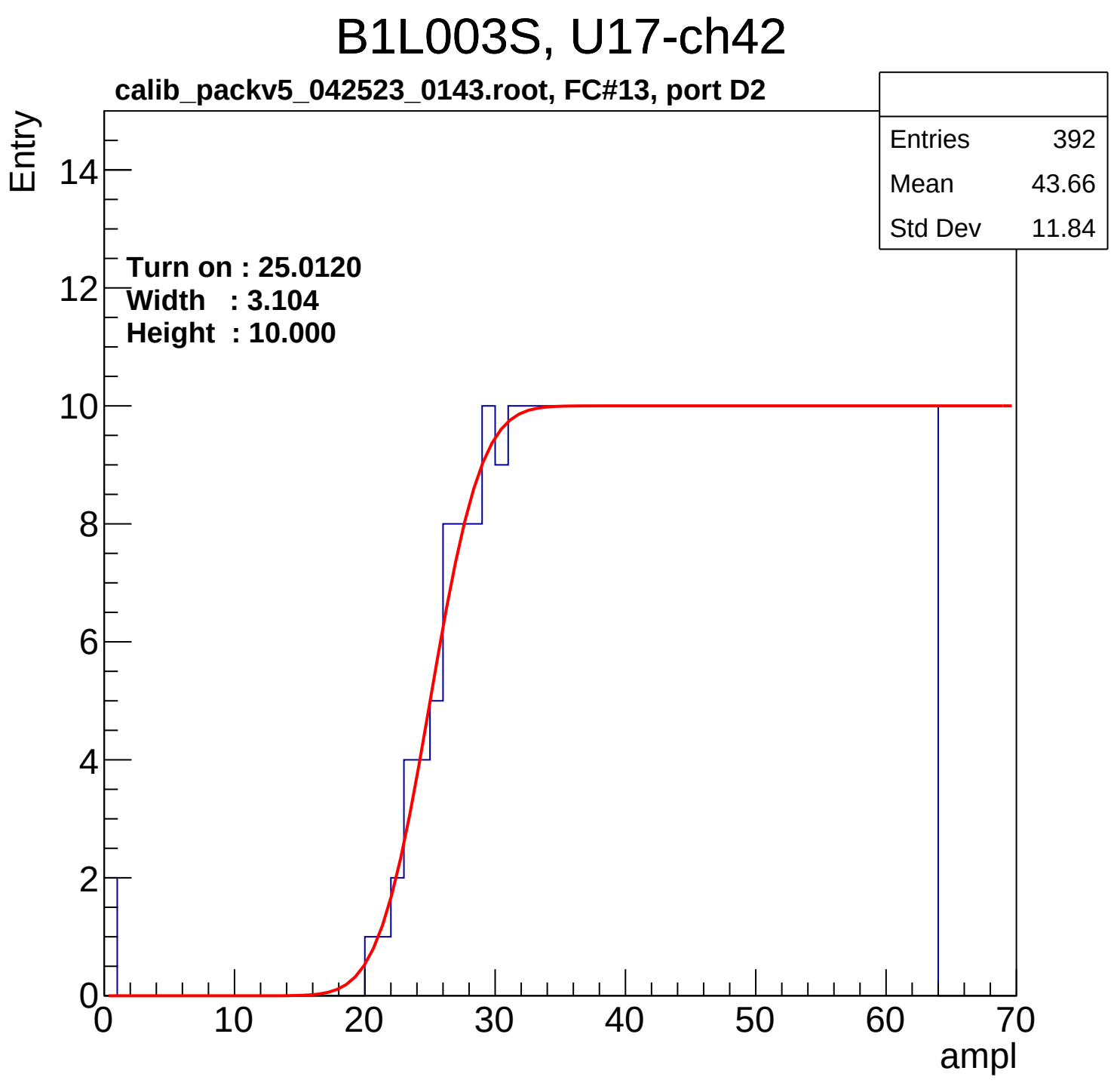
B1L003S, U17-ch42
calib_packv5_042523_0143.root, FC#13, port D2
Entries 392
Mean 43.66
Std Dev 11.84
Turn on : 25.0120
Width : 3.104
Height : 10.000
Entry
ampl
0
2
4
6
8
10
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60
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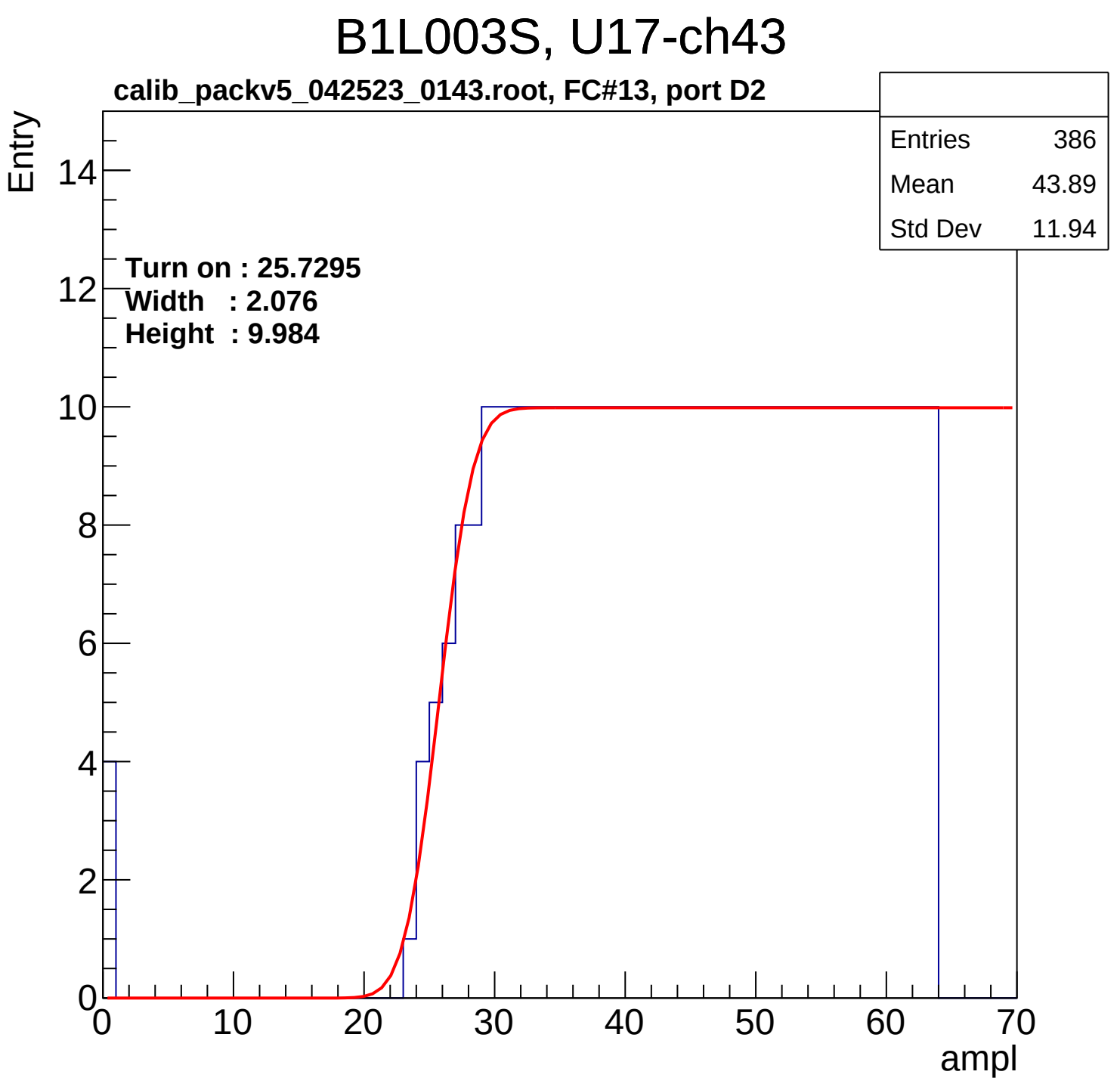
B1L003S, U17-ch43
calib_packv5_042523_0143.root, FC#13, port D2
Entries 386
Mean 43.89
Std Dev 11.94
Turn on : 25.7295
Width : 2.076
Height : 9.984
Entry
ampl
0
2
4
6
8
10
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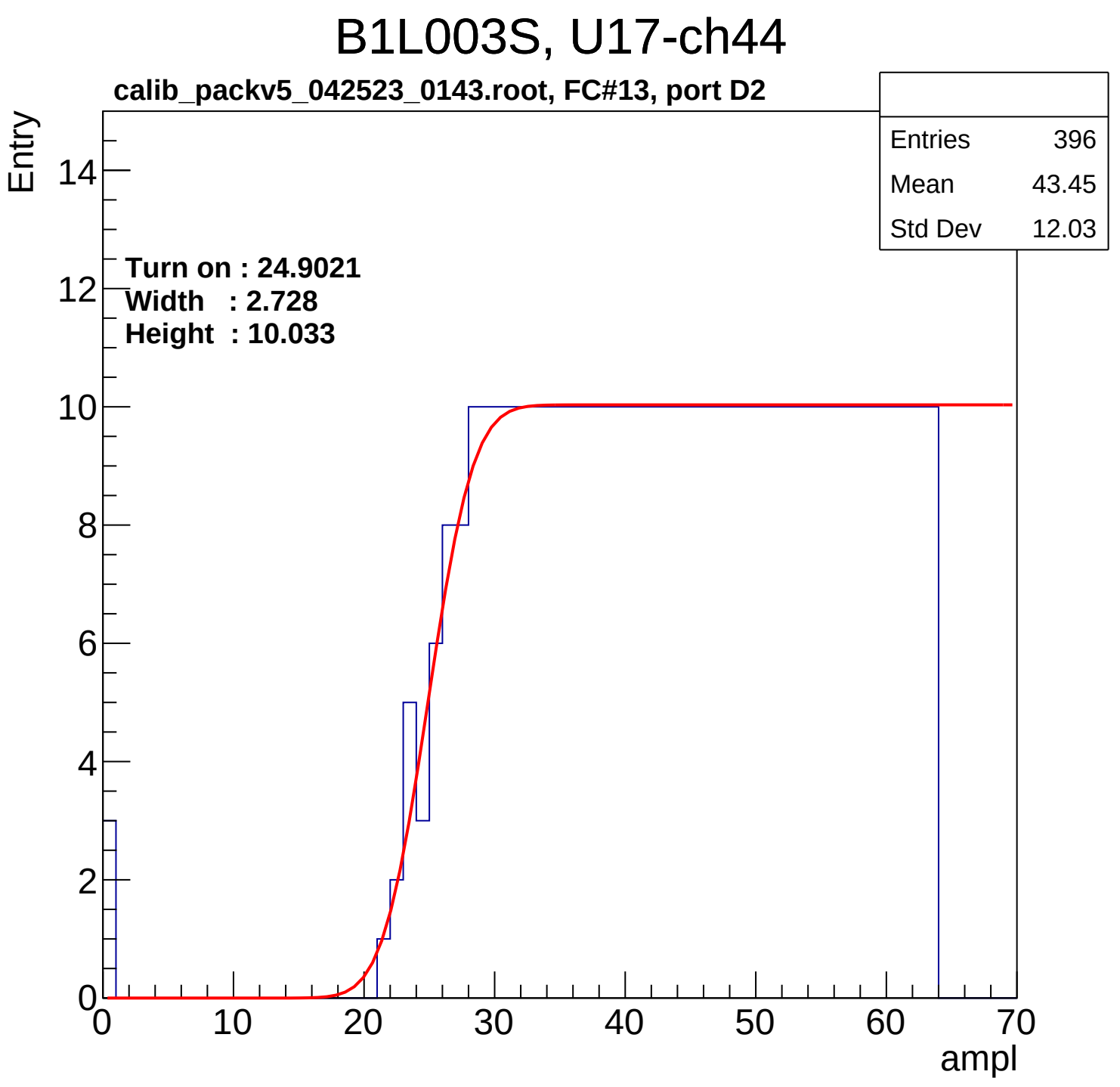
B1L003S, U17-ch44
calib_packv5_042523_0143.root, FC#13, port D2
Entries 396
Mean 43.45
Std Dev 12.03
Turn on : 24.9021
Width : 2.728
Height : 10.033
Entry
ampl
0
2
4
6
8
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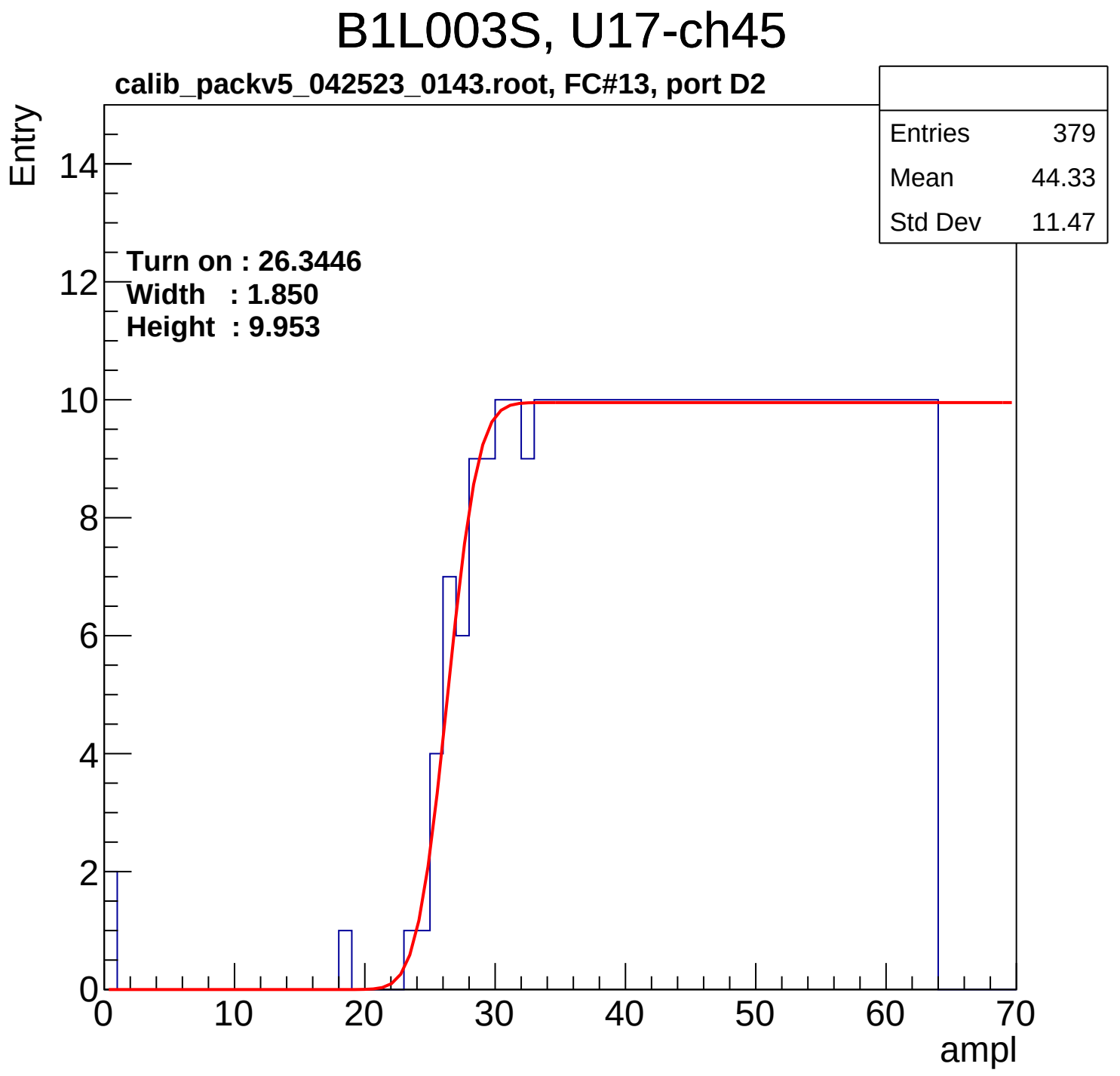
B1L003S, U17-ch45
calib_packv5_042523_0143.root, FC#13, port D2
Entries 379
Mean 44.33
Std Dev 11.47
Turn on : 26.3446
Width : 1.850
Height : 9.953
Entry
ampl
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4
6
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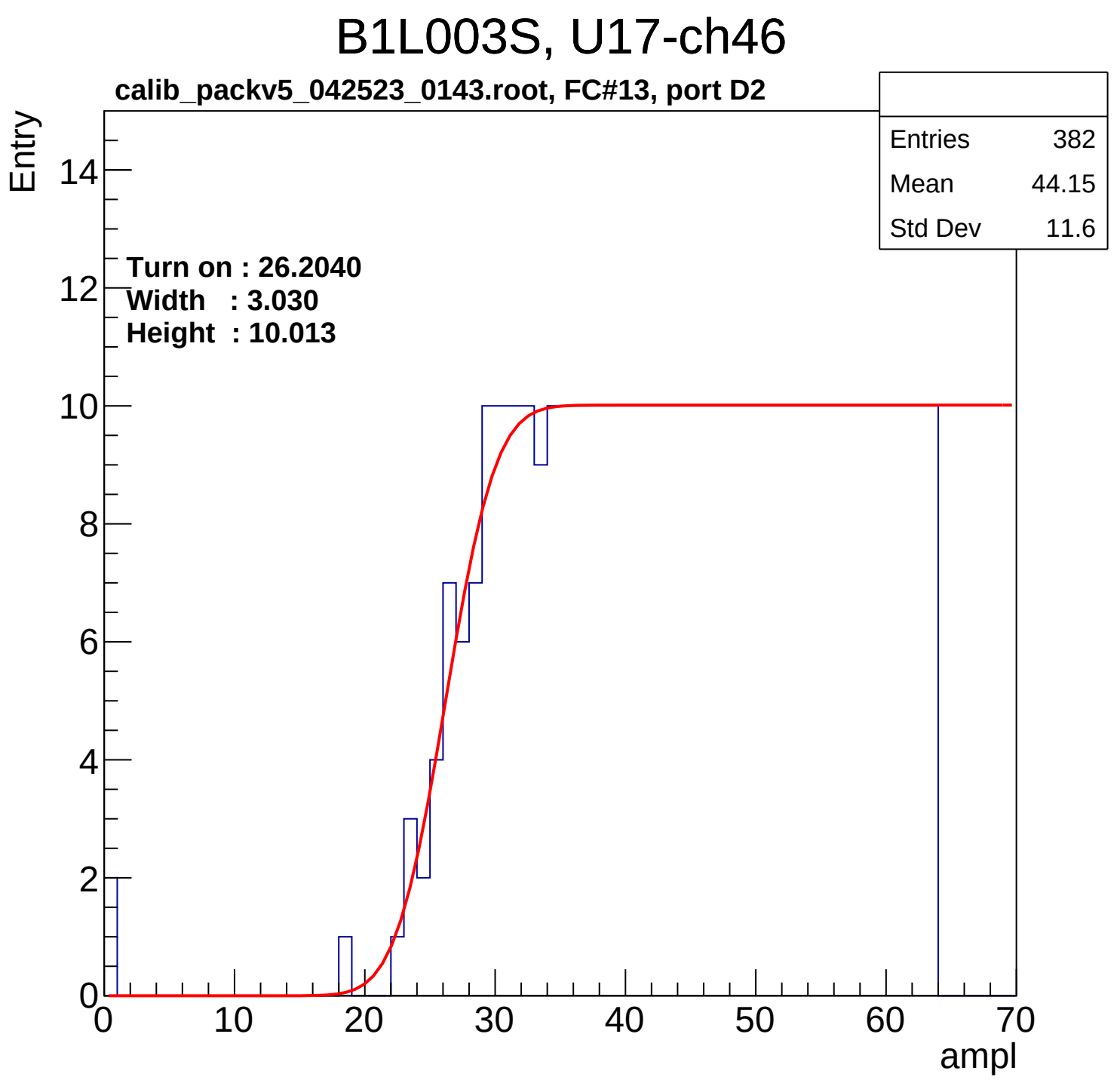
B1L003S, U17-ch46
calib_packv5_042523_0143.root, FC#13, port D2
Entries 382
Mean 44.15
Std Dev 11.6
Turn on : 26.2040
Width : 3.030
Height : 10.013
Entry
ampl
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2
4
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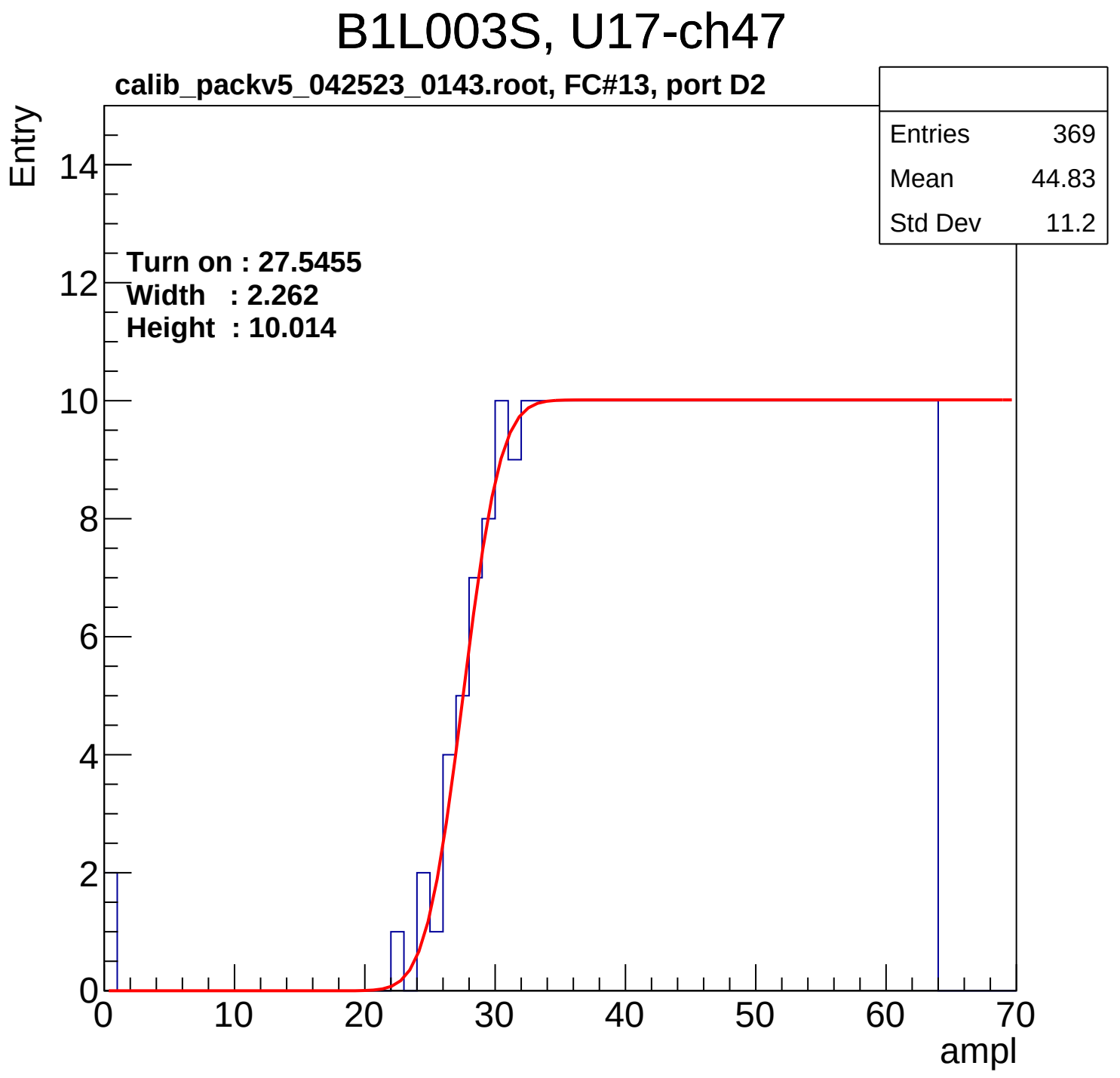
B1L003S, U17-ch47
calib_packv5_042523_0143.root, FC#13, port D2
Entries 369
Mean 44.83
Std Dev 11.2
Turn on : 27.5455
Width : 2.262
Height : 10.014
Entry
ampl
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2
4
6
8
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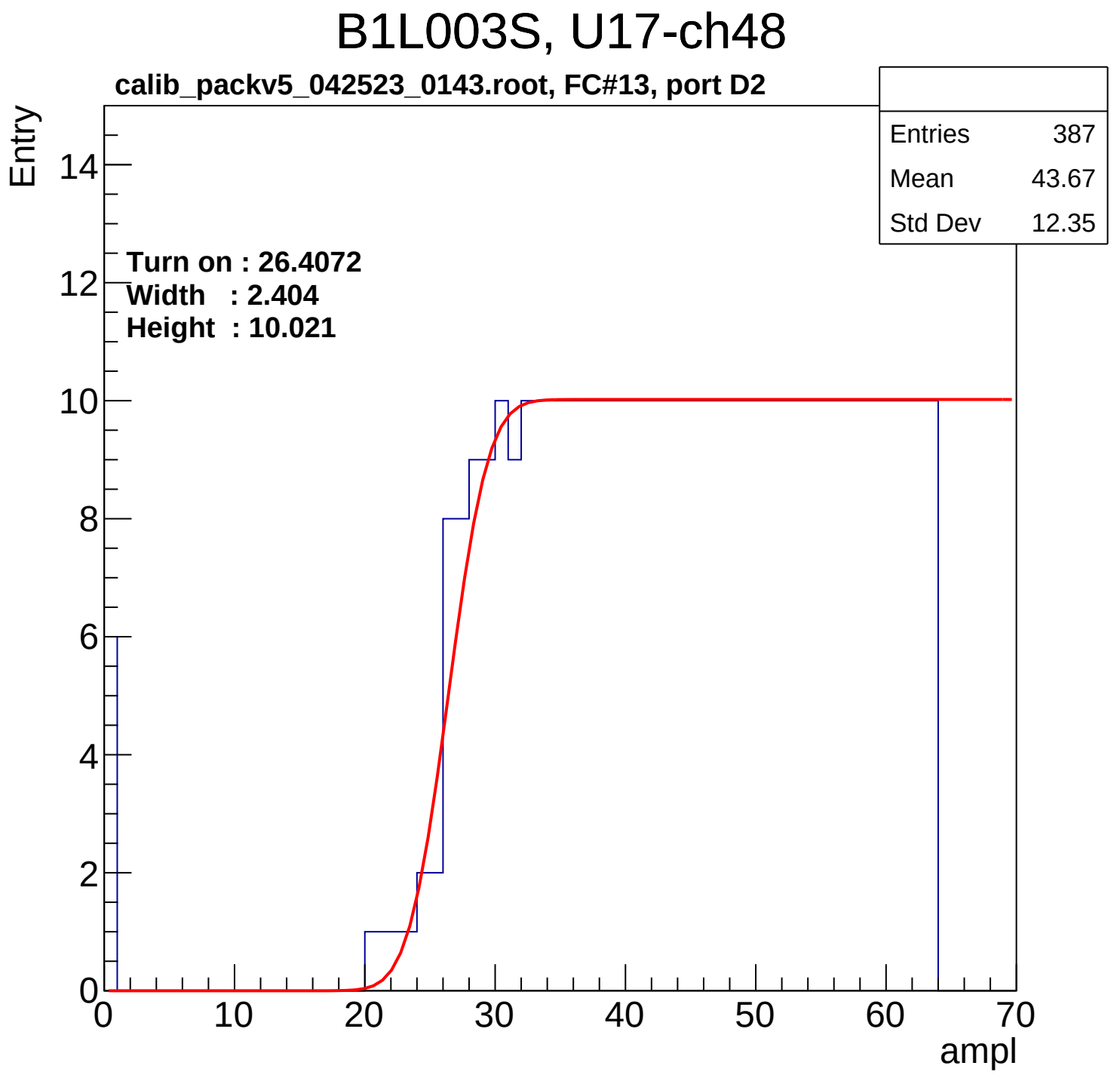
B1L003S, U17-ch48
calib_packv5_042523_0143.root, FC#13, port D2
Entries 387
Mean 43.67
Std Dev 12.35
Turn on : 26.4072
Width : 2.404
Height : 10.021
Entry
ampl
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2
4
6
8
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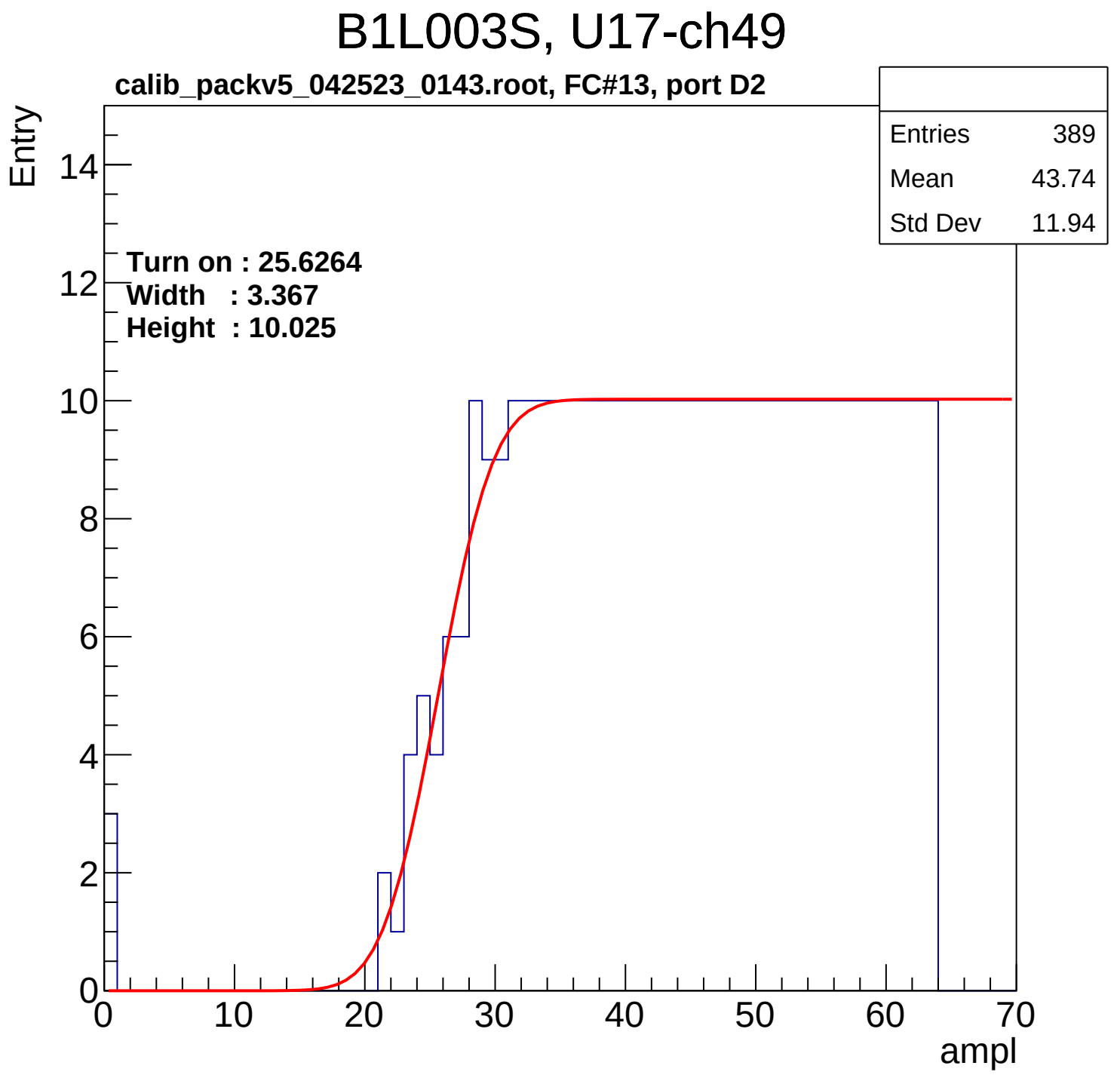
B1L003S, U17-ch49
calib_packv5_042523_0143.root, FC#13, port D2
Entries 389
Mean 43.74
Std Dev 11.94
Turn on : 25.6264
Width : 3.367
Height : 10.025
Entry
ampl
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4
6
8
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60
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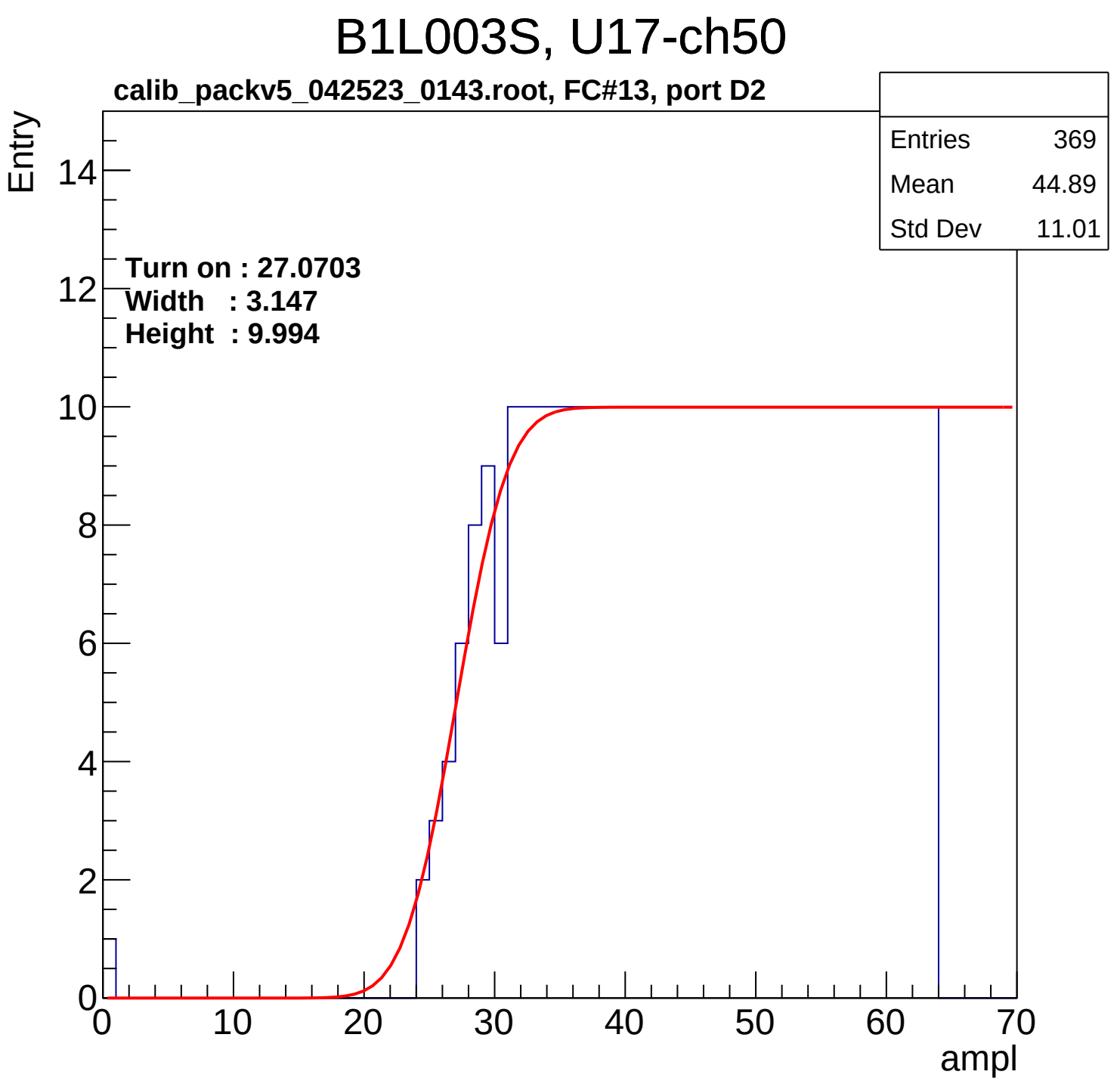
B1L003S, U17-ch50
calib_packv5_042523_0143.root, FC#13, port D2
Entries 369
Mean 44.89
Std Dev 11.01
Turn on : 27.0703
Width : 3.147
Height : 9.994
Entry
ampl
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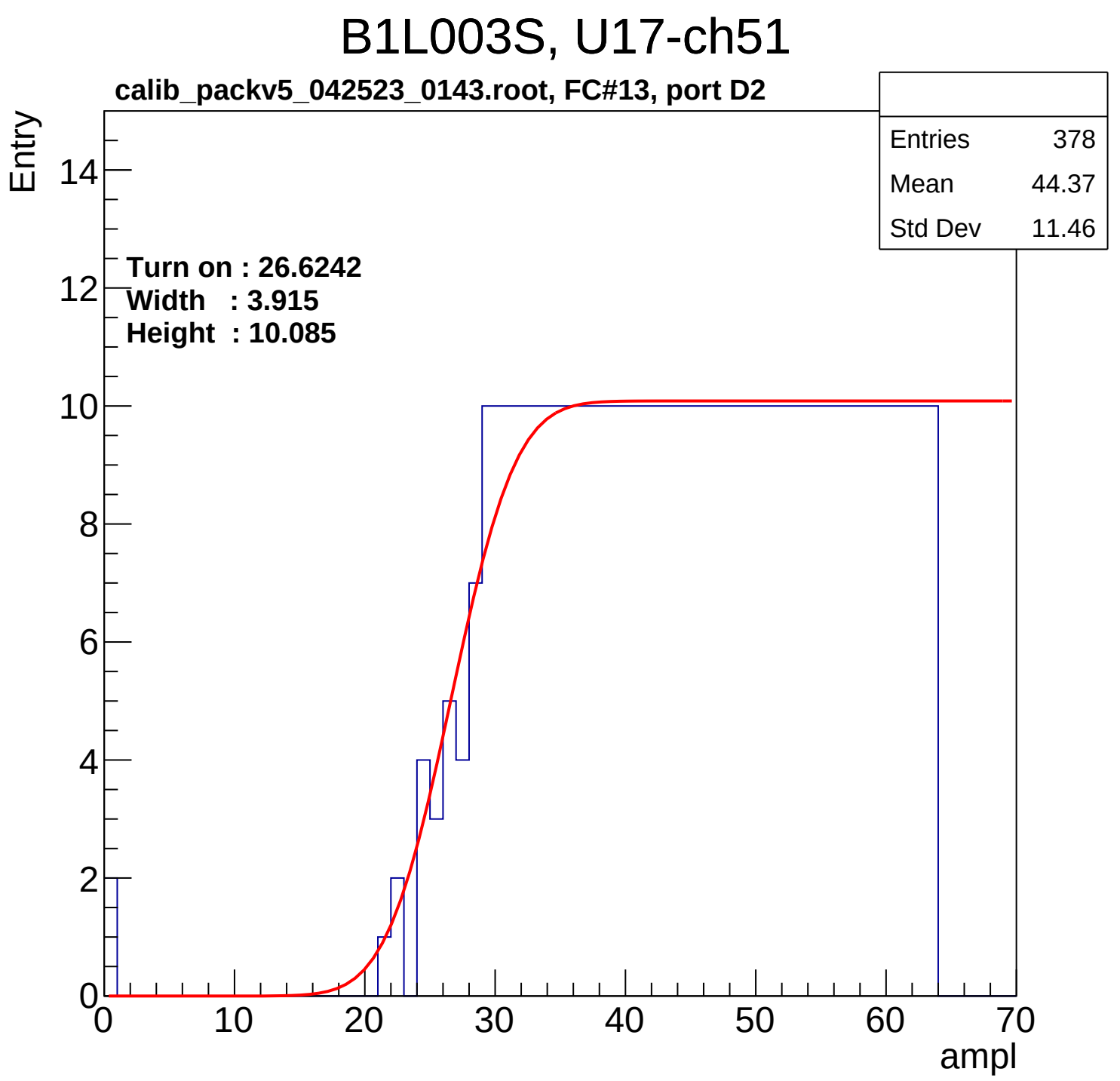
B1L003S, U17-ch51
calib_packv5_042523_0143.root, FC#13, port D2
Entries 378
Mean 44.37
Std Dev 11.46
Turn on : 26.6242
Width : 3.915
Height : 10.085
Entry
ampl
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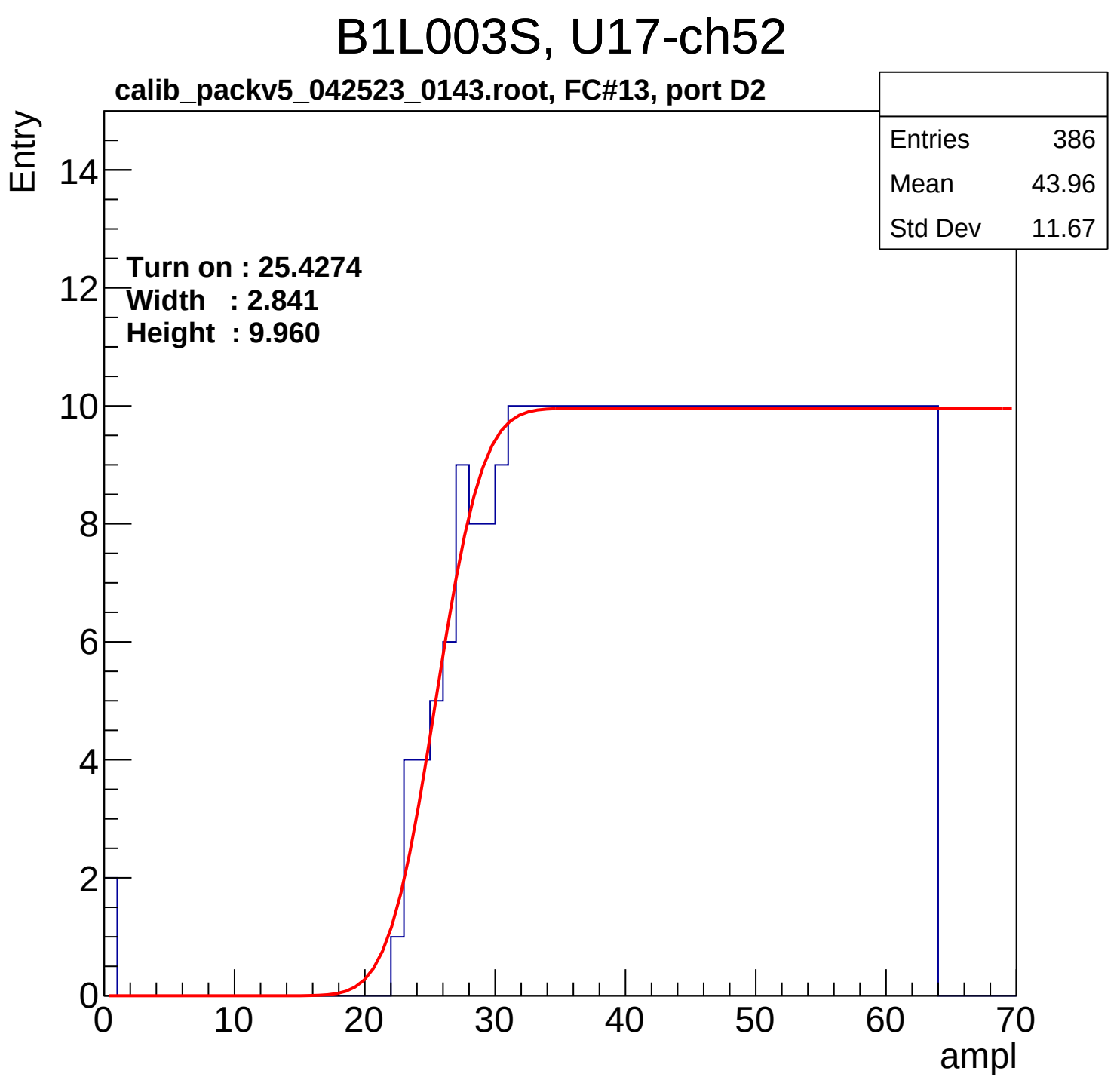
B1L003S, U17-ch52
calib_packv5_042523_0143.root, FC#13, port D2
Entries 386
Mean 43.96
Std Dev 11.67
Turn on : 25.4274
Width : 2.841
Height : 9.960
Entry
ampl
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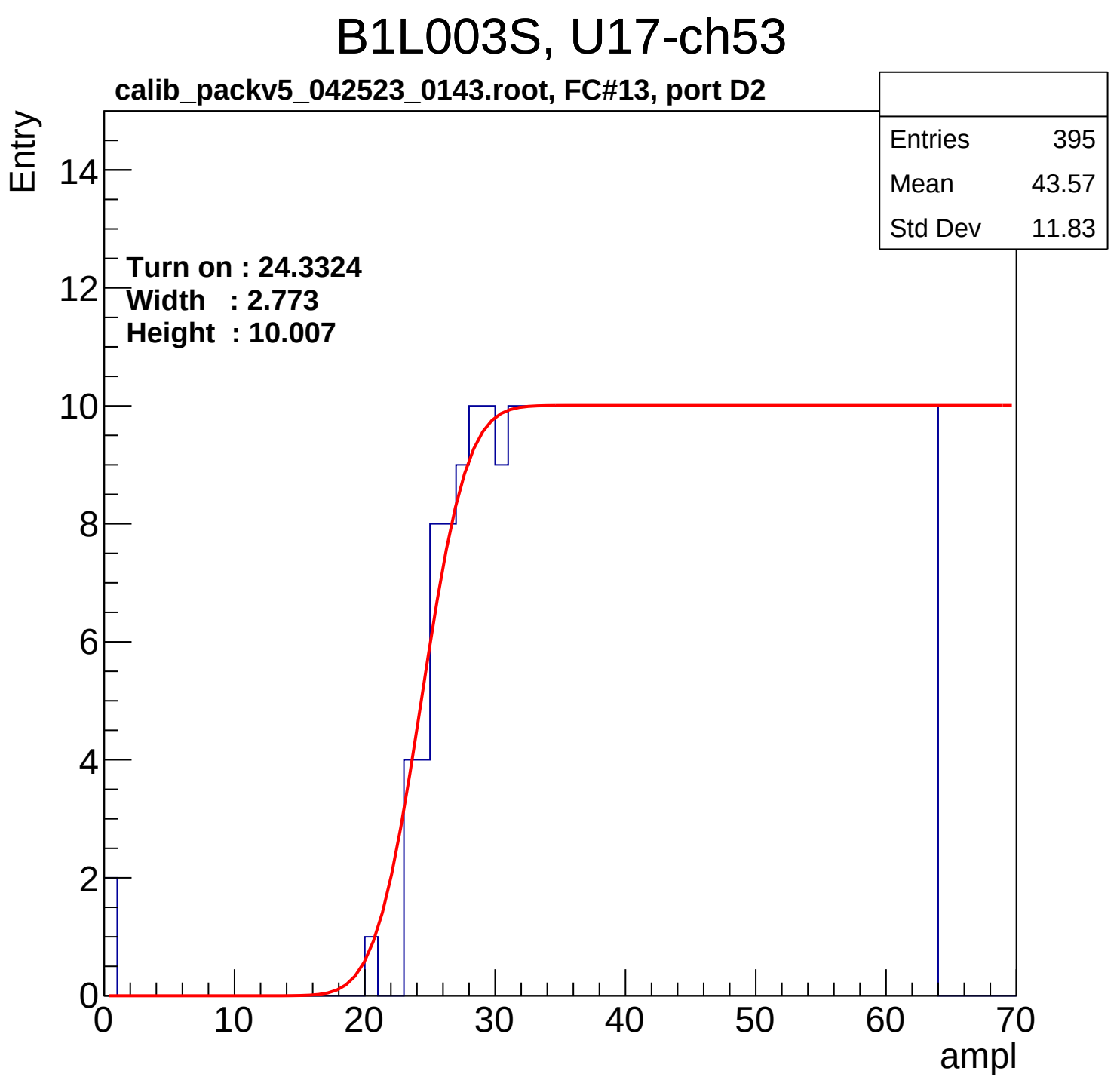
B1L003S, U17-ch53
calib_packv5_042523_0143.root, FC#13, port D2
Entries 395
Mean 43.57
Std Dev 11.83
Turn on : 24.3324
Width : 2.773
Height : 10.007
Entry
ampl
0
2
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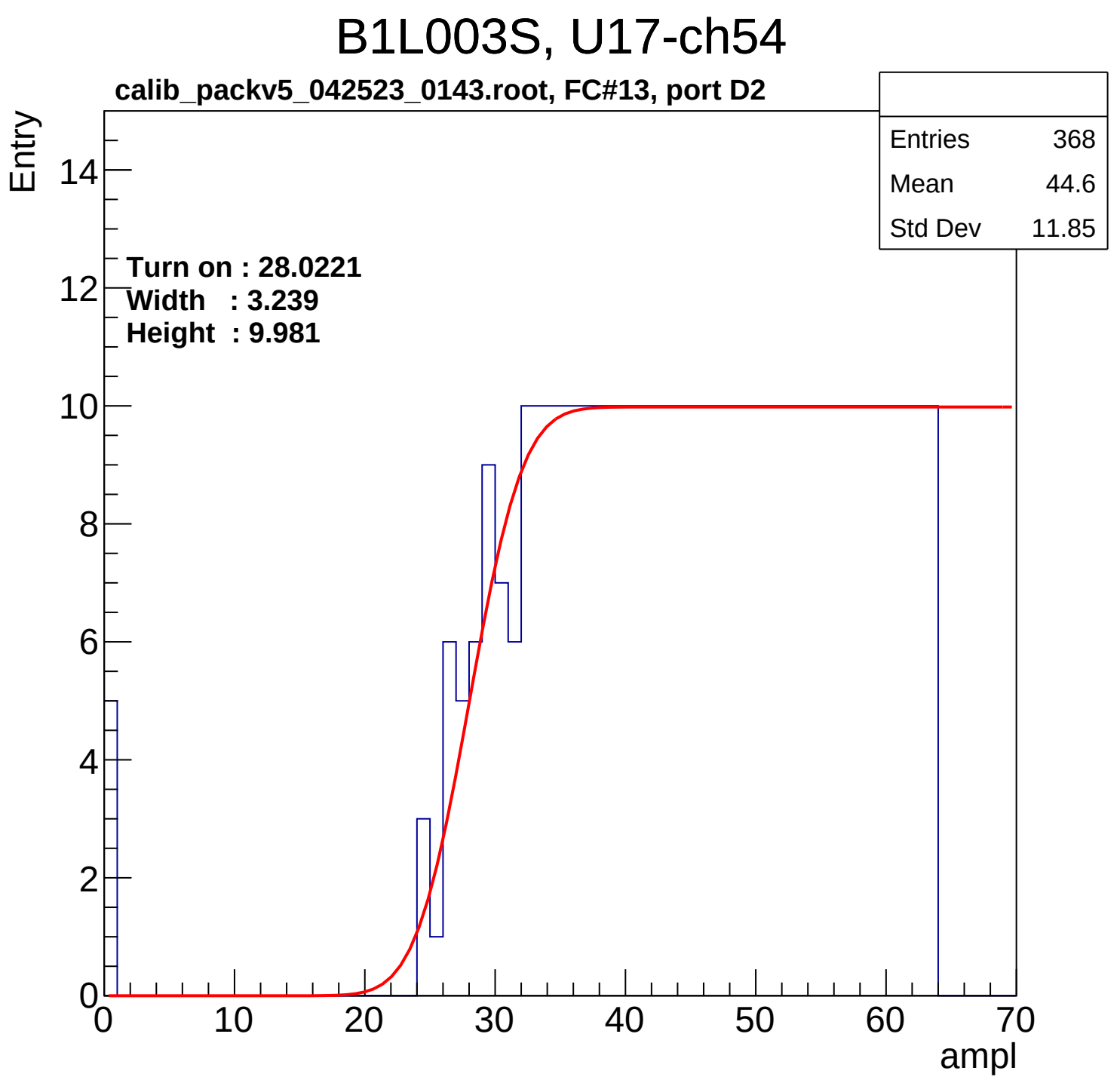
B1L003S, U17-ch54
calib_packv5_042523_0143.root, FC#13, port D2
Entries 368
Mean 44.6
Std Dev 11.85
Turn on : 28.0221
Width : 3.239
Height : 9.981
Entry
ampl
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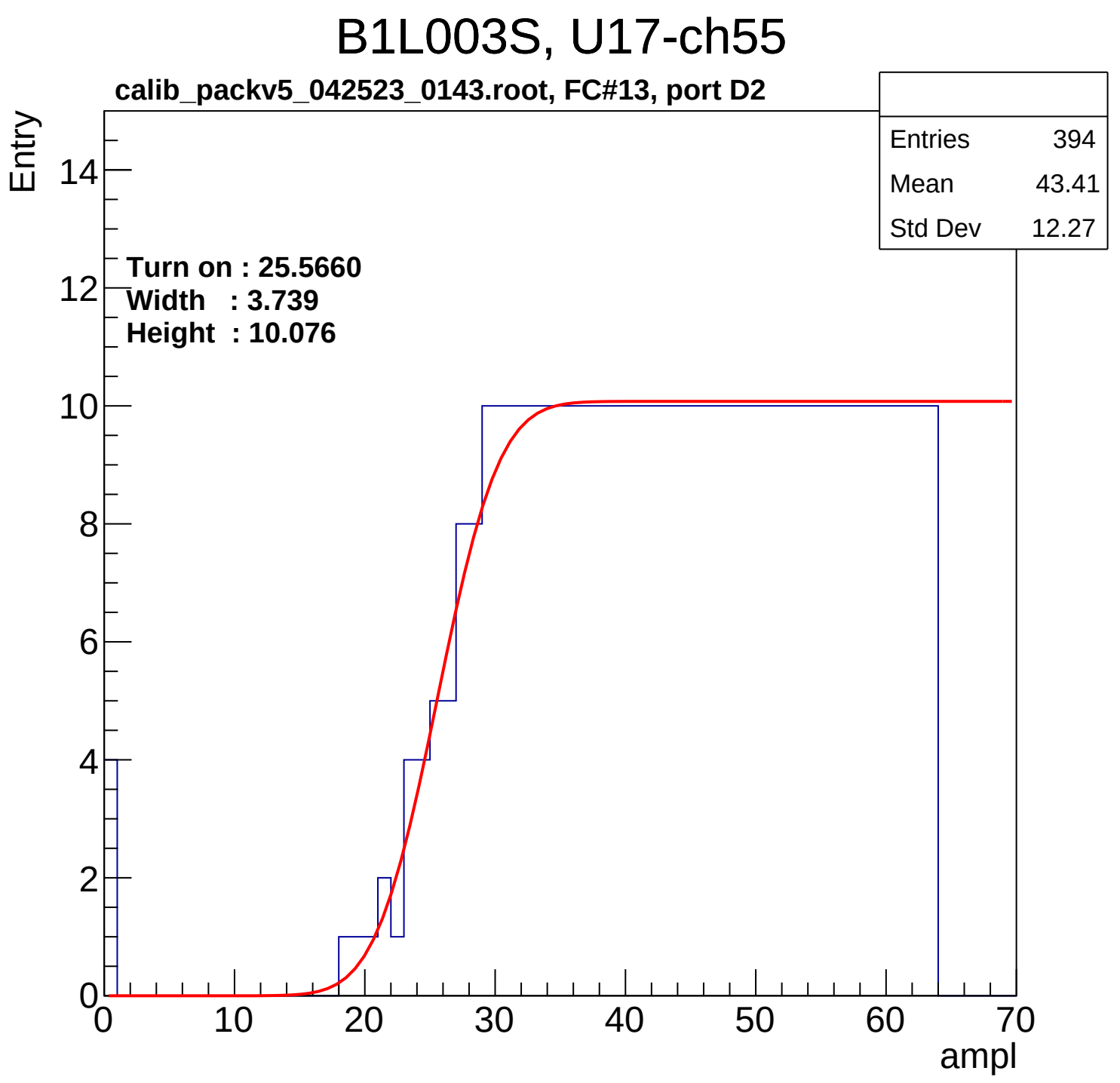
B1L003S, U17-ch55
calib_packv5_042523_0143.root, FC#13, port D2
Entries 394
Mean 43.41
Std Dev 12.27
Turn on : 25.5660
Width : 3.739
Height : 10.076
Entry
ampl
0
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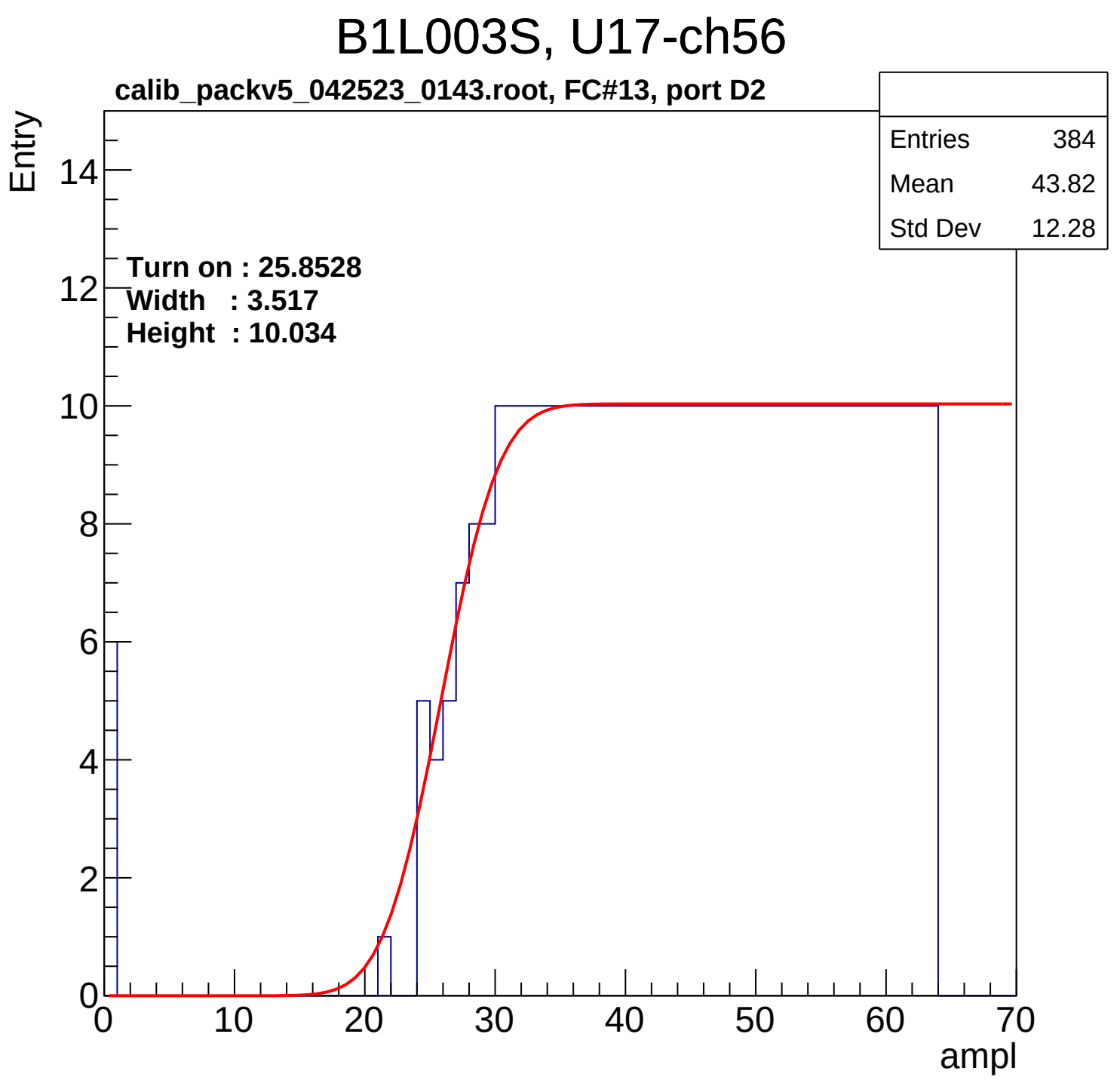
B1L003S, U17-ch56
calib_packv5_042523_0143.root, FC#13, port D2
Entries 384
Mean 43.82
Std Dev 12.28
Turn on : 25.8528
Width : 3.517
Height : 10.034
Entry
ampl
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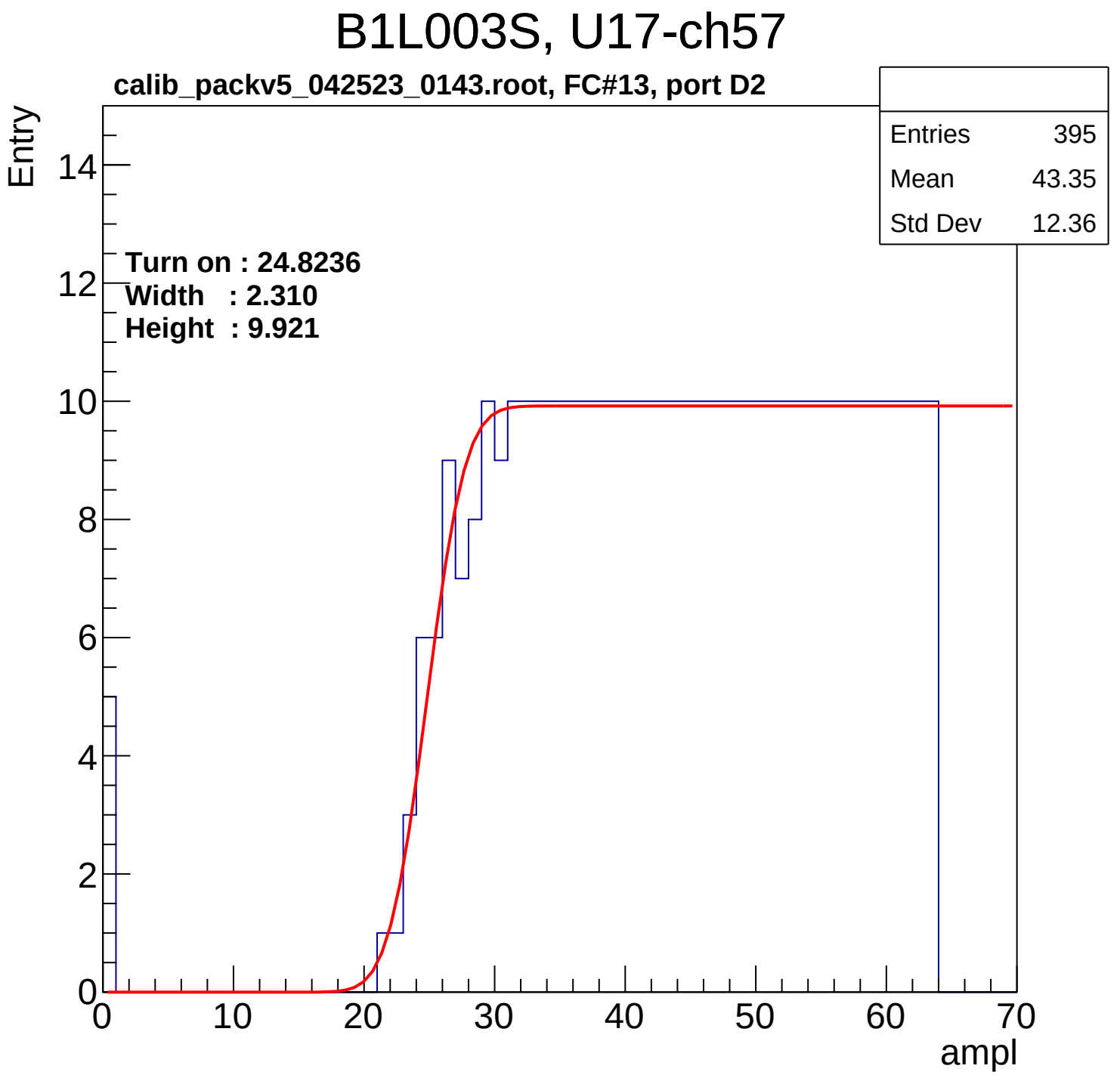
B1L003S, U17-ch57
calib_packv5_042523_0143.root, FC#13, port D2
Entries 395
Mean 43.35
Std Dev 12.36
Turn on : 24.8236
Width : 2.310
Height : 9.921
Entry
ampl
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6
8
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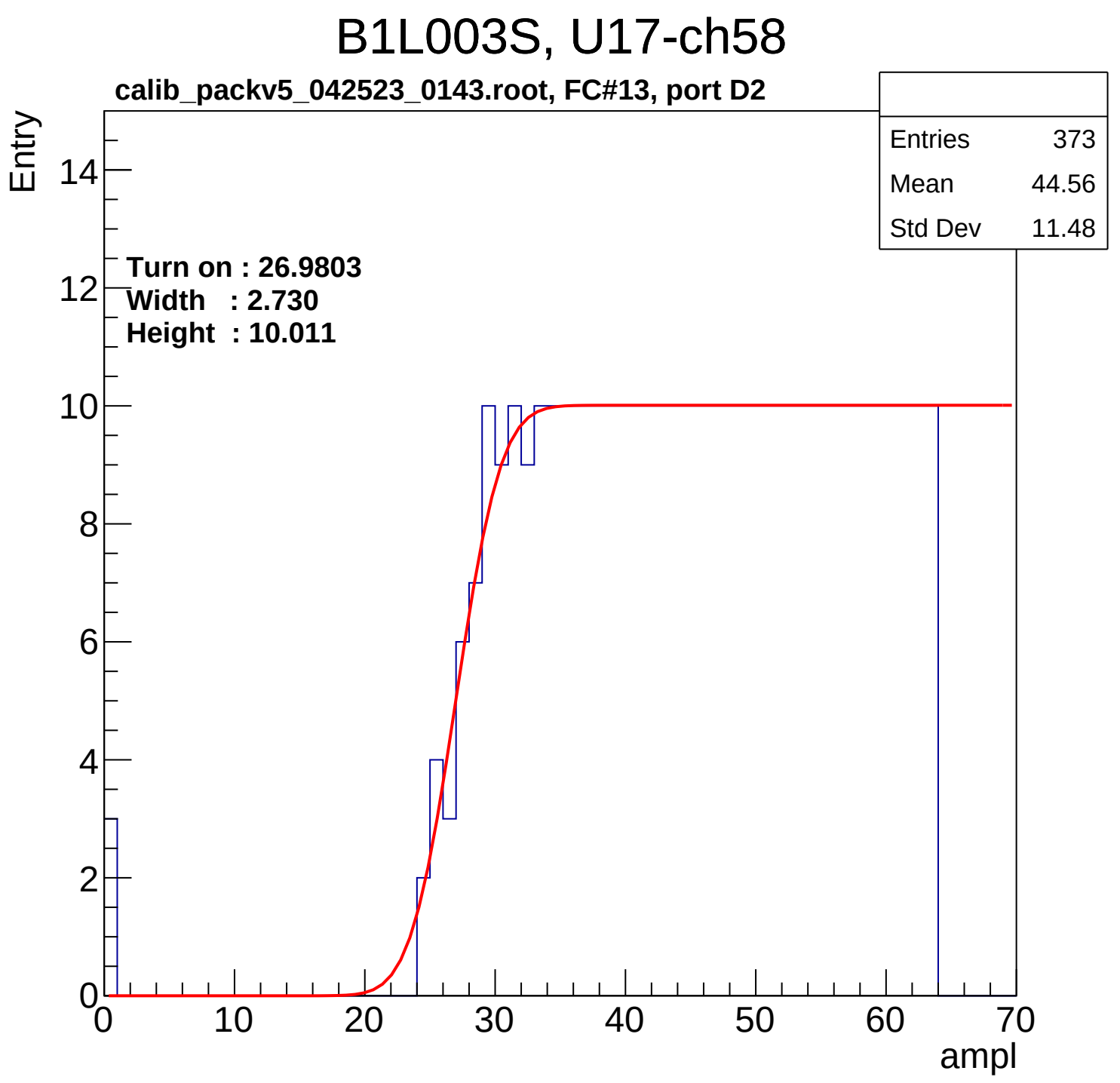
B1L003S, U17-ch58
calib_packv5_042523_0143.root, FC#13, port D2
Entries 373
Mean 44.56
Std Dev 11.48
Turn on : 26.9803
Width : 2.730
Height : 10.011
Entry
ampl
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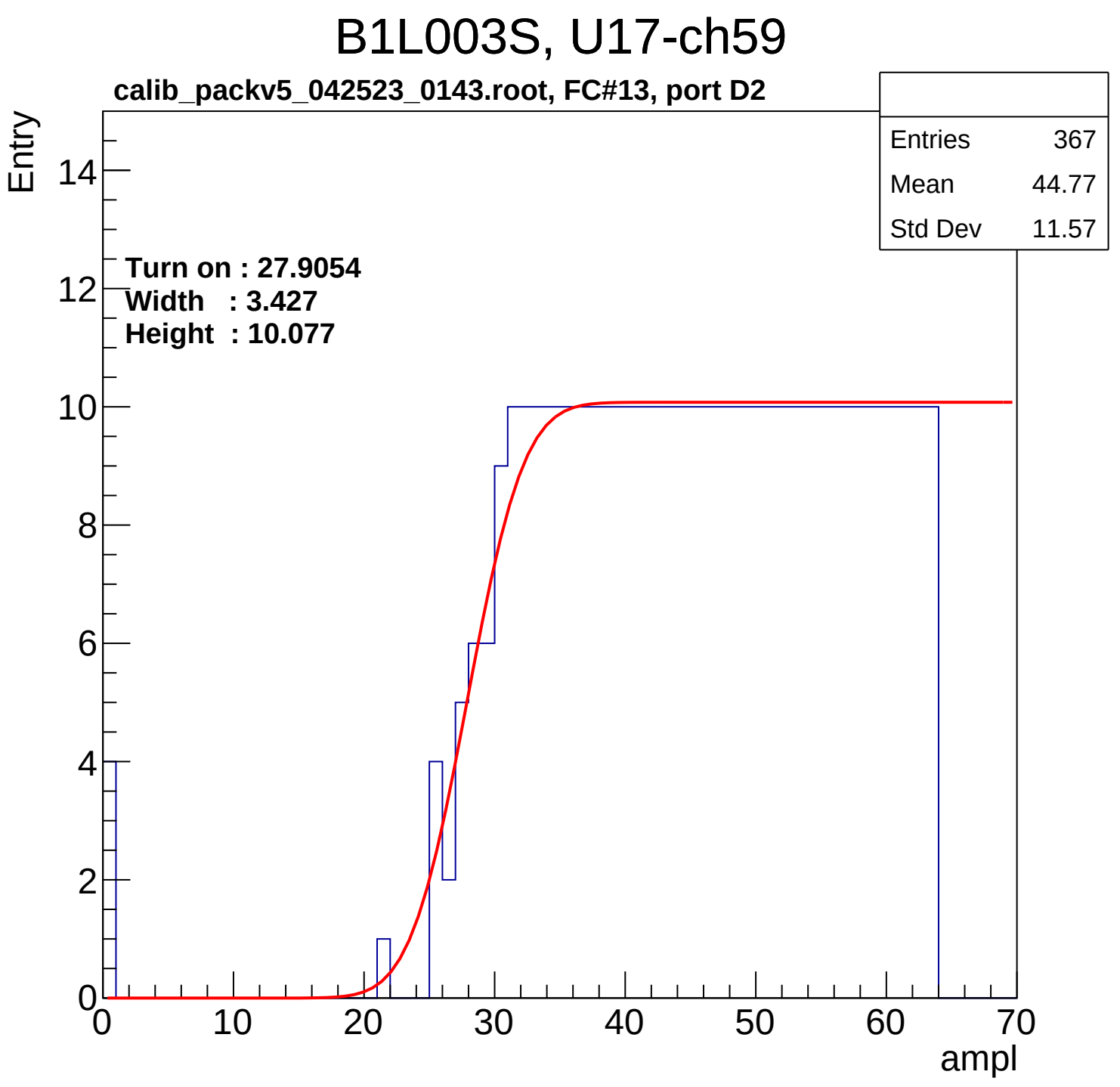
B1L003S, U17-ch59
calib_packv5_042523_0143.root, FC#13, port D2
Entries 367
Mean 44.77
Std Dev 11.57
Turn on : 27.9054
Width : 3.427
Height : 10.077
Entry
ampl
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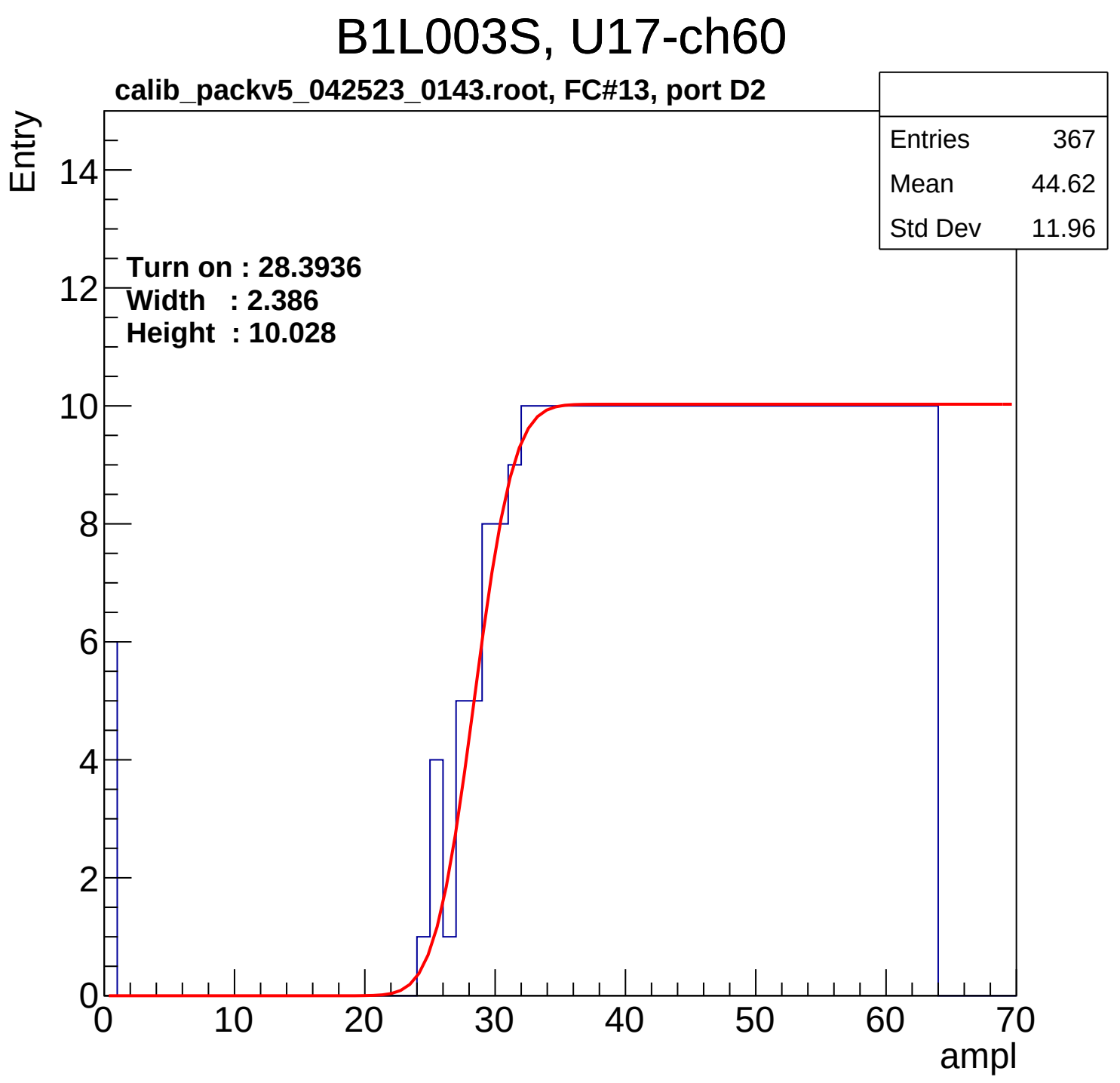
B1L003S, U17-ch60
calib_packv5_042523_0143.root, FC#13, port D2
Entries 367
Mean 44.62
Std Dev 11.96
Turn on : 28.3936
Width : 2.386
Height : 10.028
Entry
ampl
0
2
4
6
8
10
12
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10
20
30
40
50
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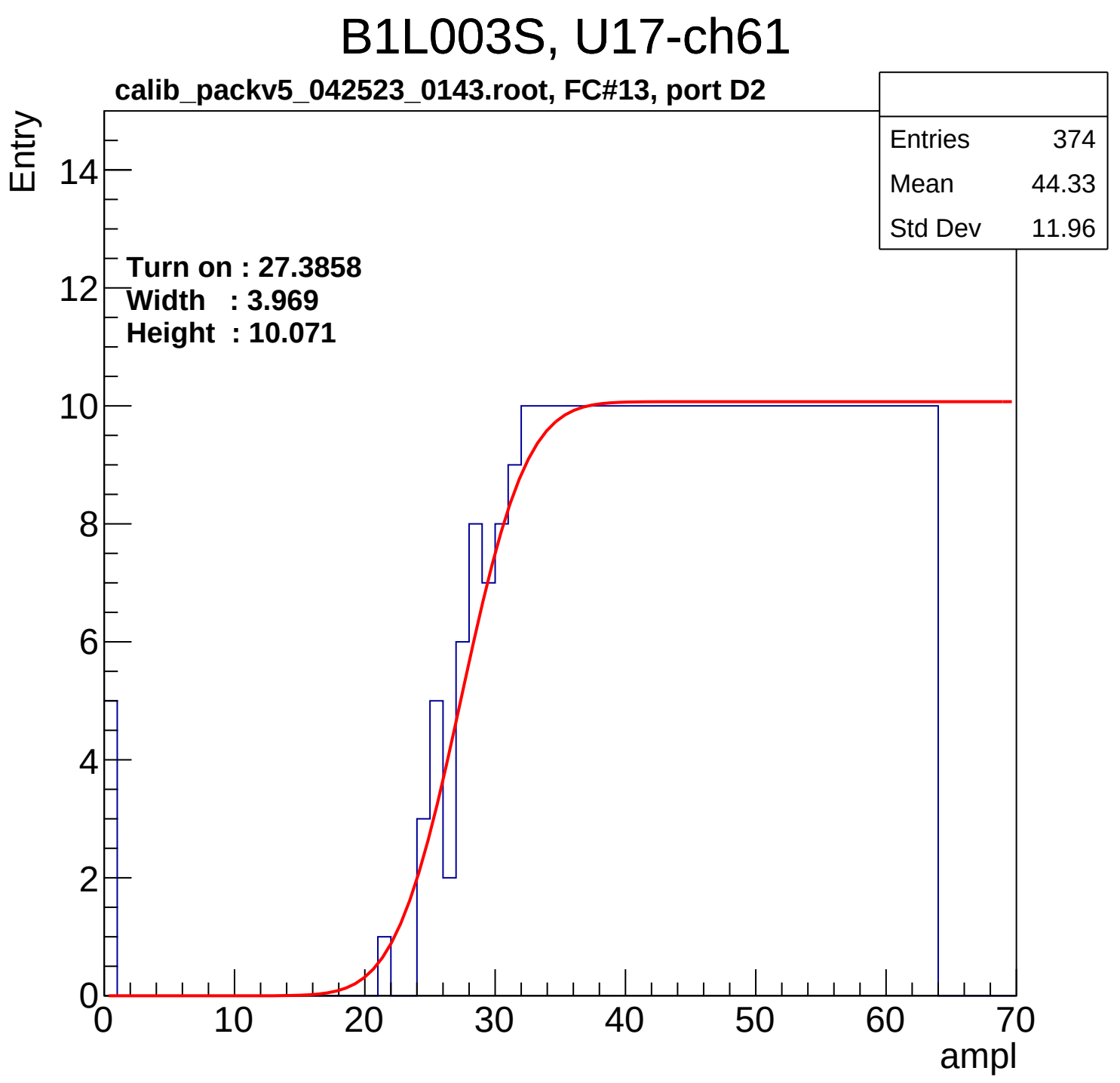
B1L003S, U17-ch61
calib_packv5_042523_0143.root, FC#13, port D2
Entries 374
Mean 44.33
Std Dev 11.96
Turn on : 27.3858
Width : 3.969
Height : 10.071
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ampl
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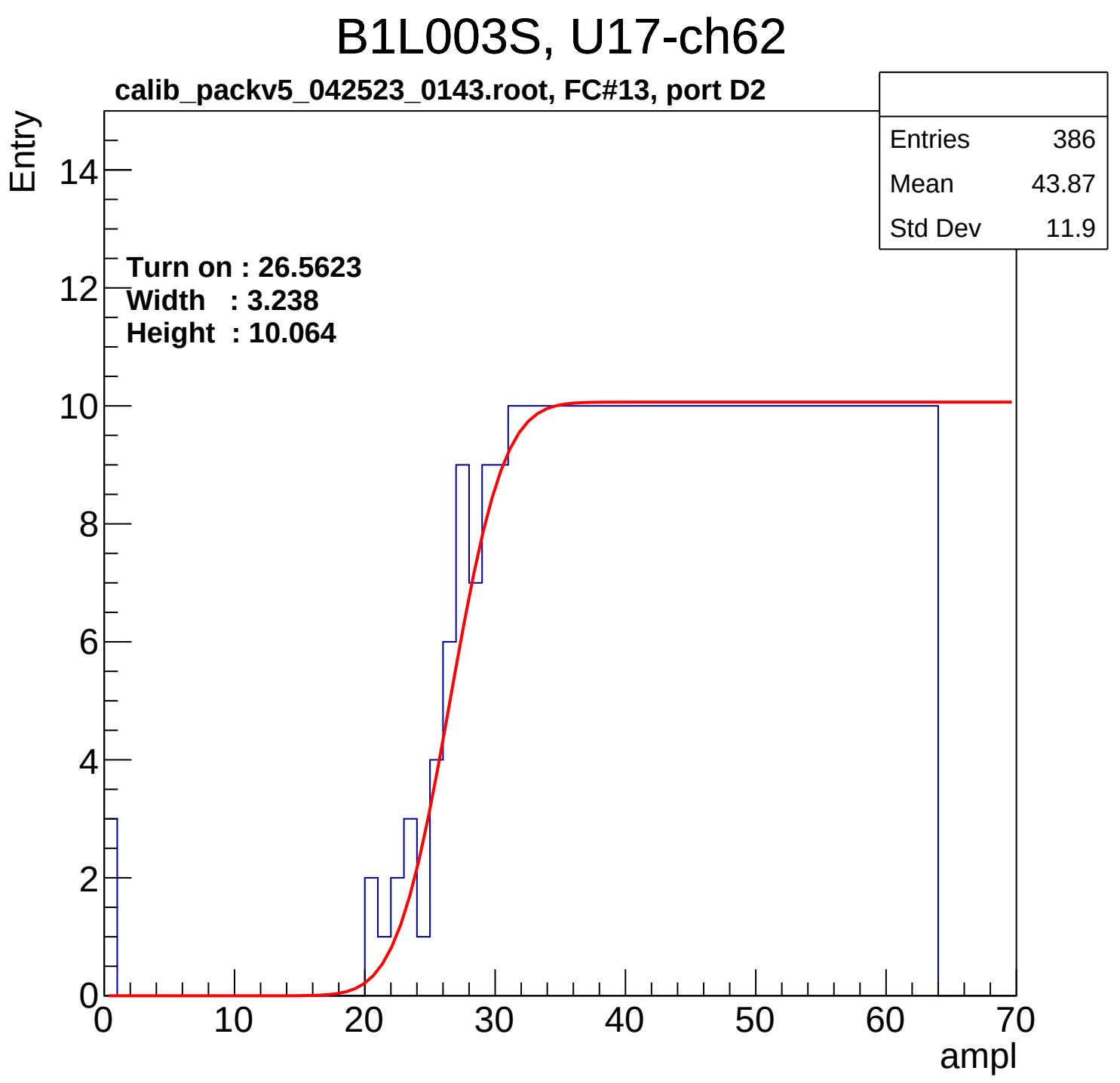
B1L003S, U17-ch62
calib_packv5_042523_0143.root, FC#13, port D2
Entries 386
Mean 43.87
Std Dev 11.9
Turn on : 26.5623
Width : 3.238
Height : 10.064
Entry
ampl
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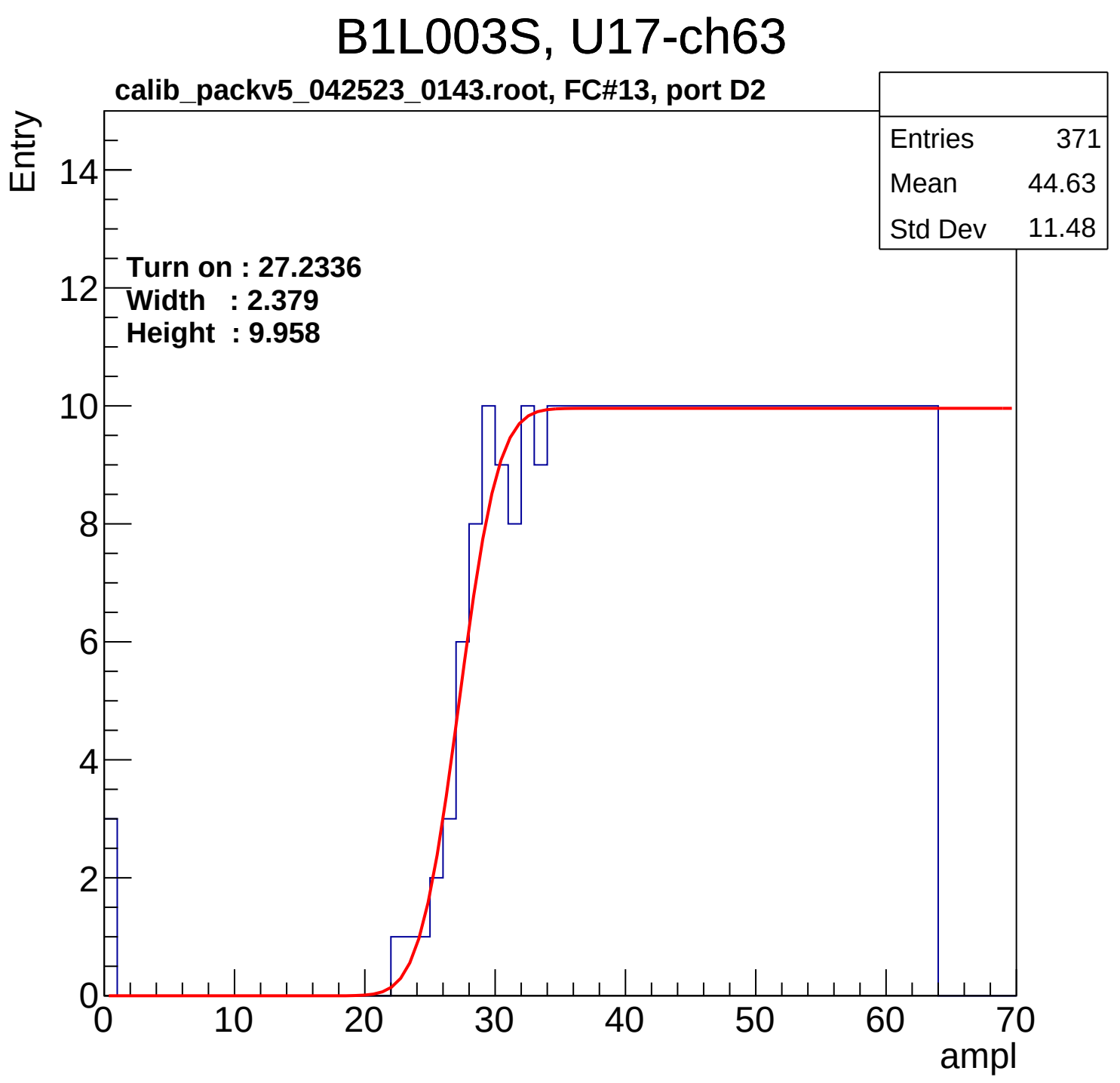
B1L003S, U17-ch63
calib_packv5_042523_0143.root, FC#13, port D2
Entries 371
Mean 44.63
Std Dev 11.48
Turn on : 27.2336
Width : 2.379
Height : 9.958
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ampl
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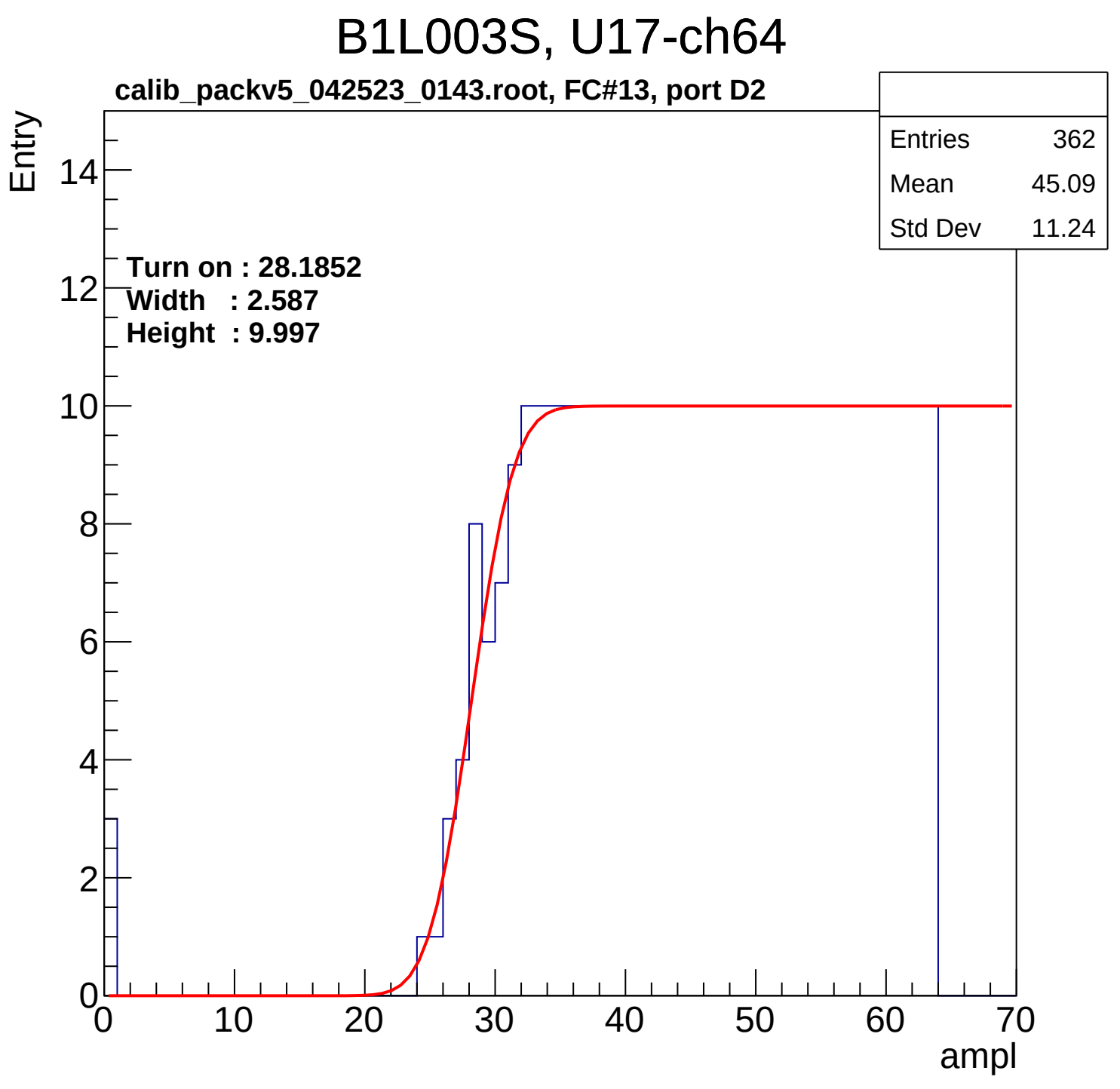
B1L003S, U17-ch64
calib_packv5_042523_0143.root, FC#13, port D2
Entries 362
Mean 45.09
Std Dev 11.24
Turn on : 28.1852
Width : 2.587
Height : 9.997
Entry
ampl
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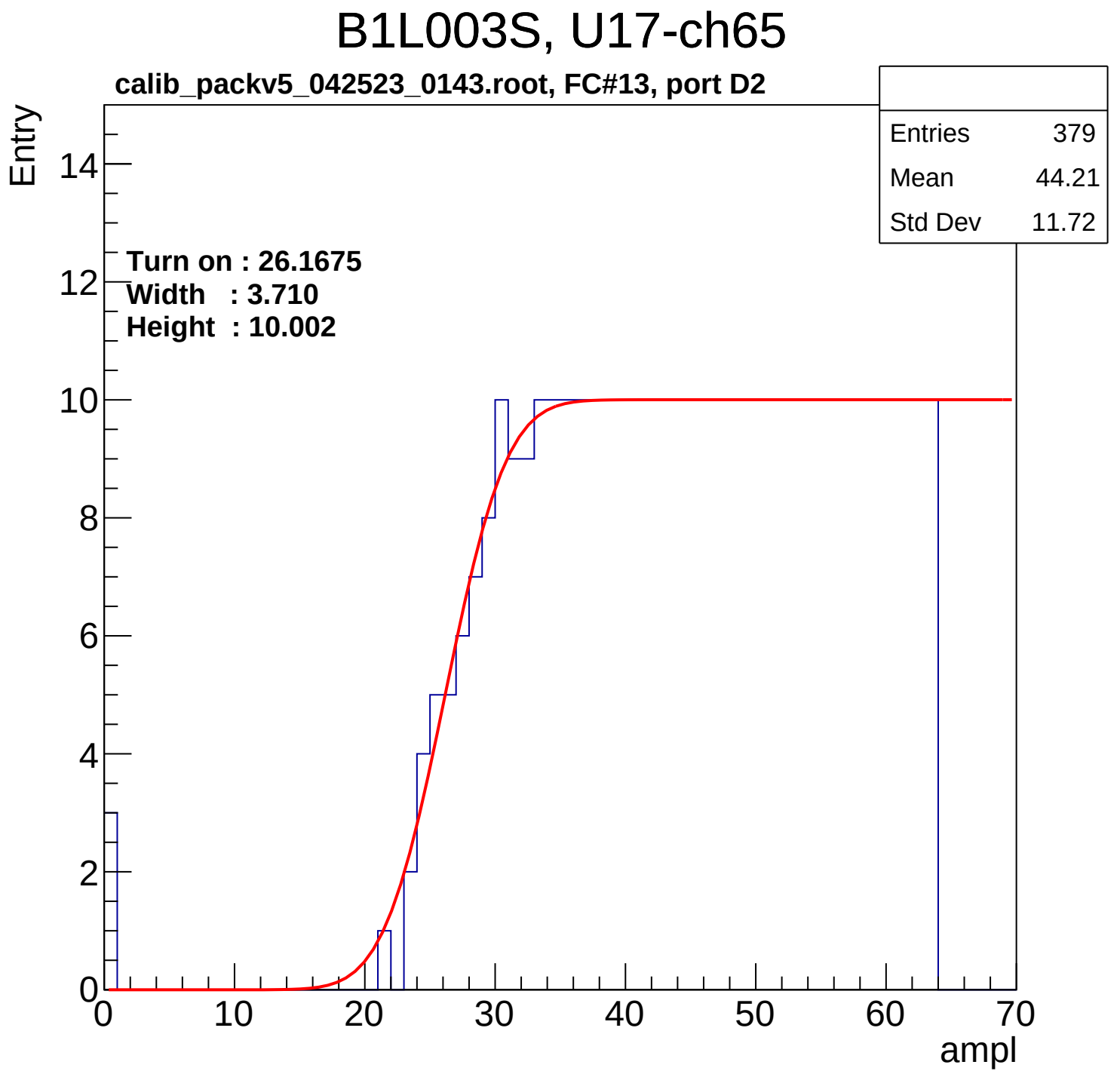
B1L003S, U17-ch65
calib_packv5_042523_0143.root, FC#13, port D2
Entries 379
Mean 44.21
Std Dev 11.72
Turn on : 26.1675
Width : 3.710
Height : 10.002
Entry
ampl
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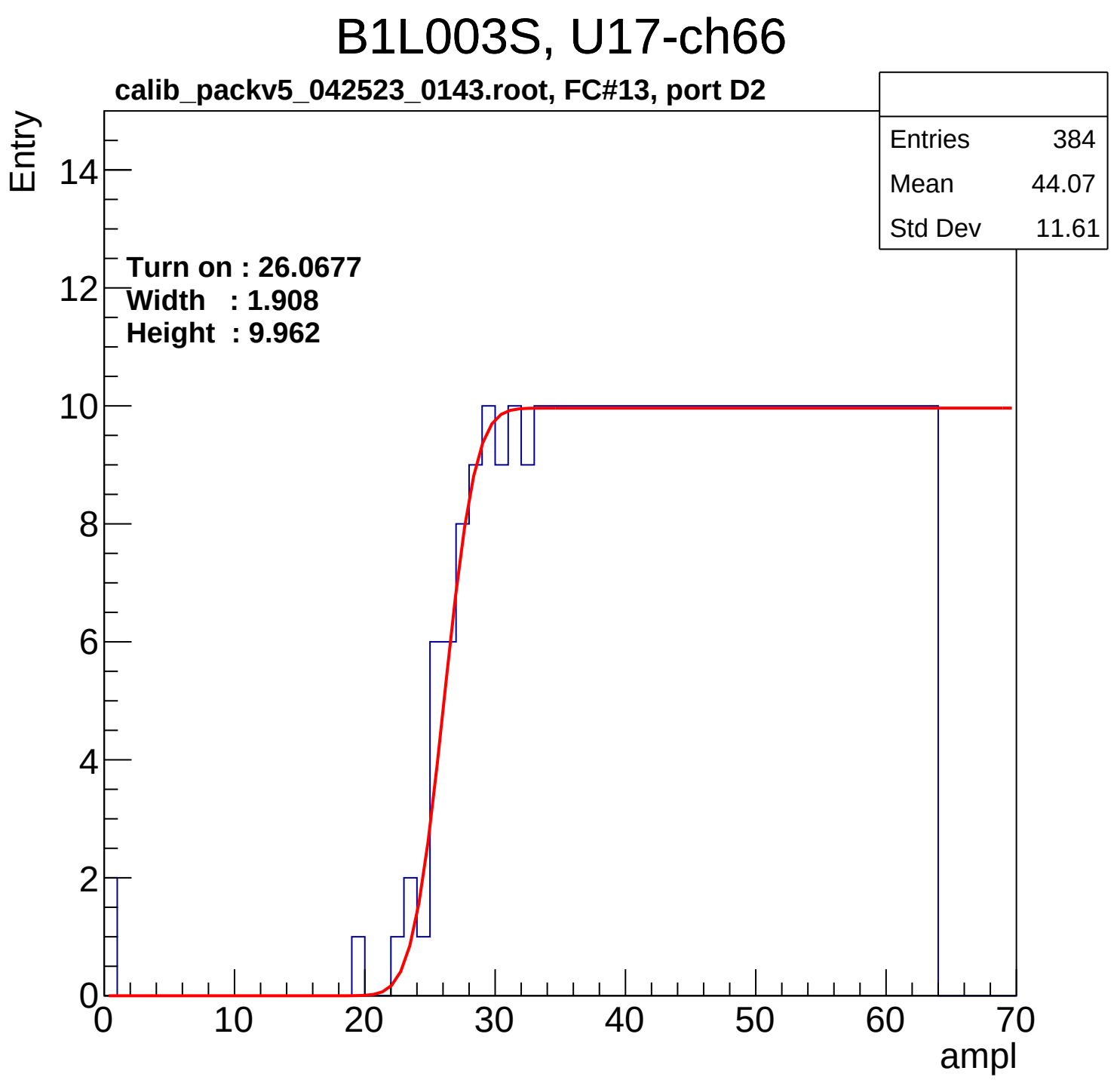
B1L003S, U17-ch66
calib_packv5_042523_0143.root, FC#13, port D2
Entries 384
Mean 44.07
Std Dev 11.61
Turn on : 26.0677
Width : 1.908
Height : 9.962
Entry
ampl
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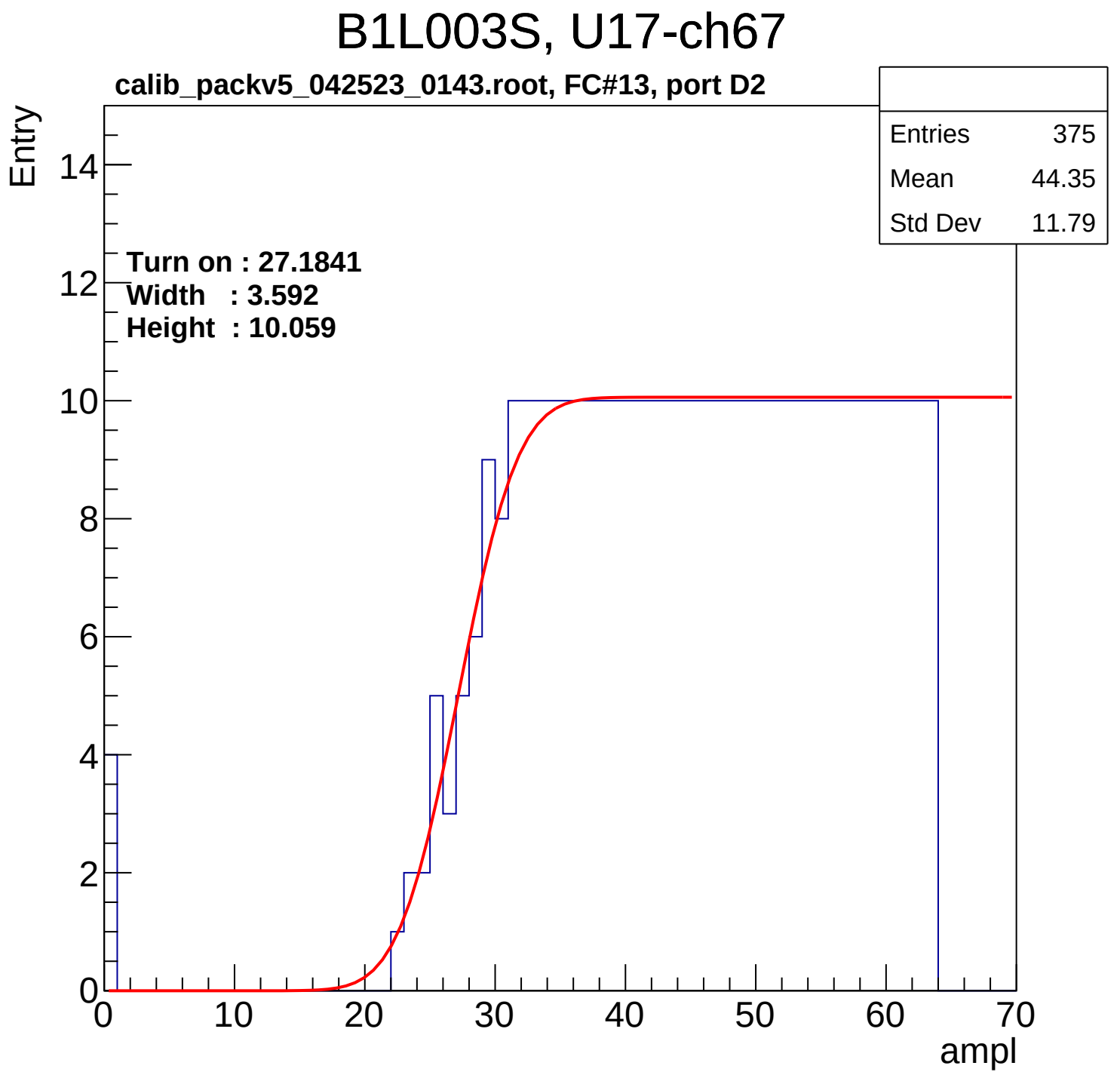
B1L003S, U17-ch67
calib_packv5_042523_0143.root, FC#13, port D2
Entries 375
Mean 44.35
Std Dev 11.79
Turn on : 27.1841
Width : 3.592
Height : 10.059
Entry
ampl
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4
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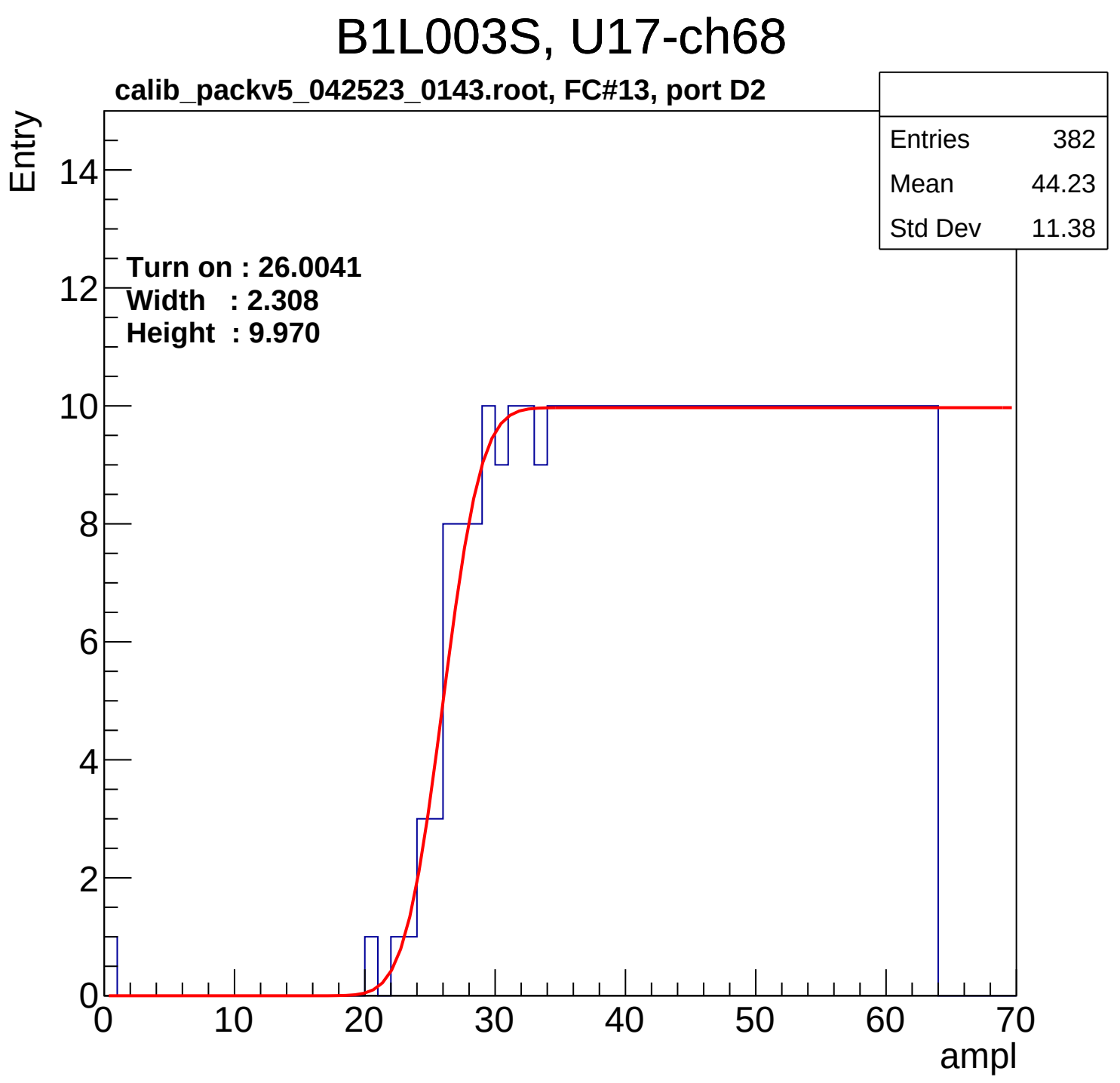
B1L003S, U17-ch68
calib_packv5_042523_0143.root, FC#13, port D2
Entries 382
Mean 44.23
Std Dev 11.38
Turn on : 26.0041
Width : 2.308
Height : 9.970
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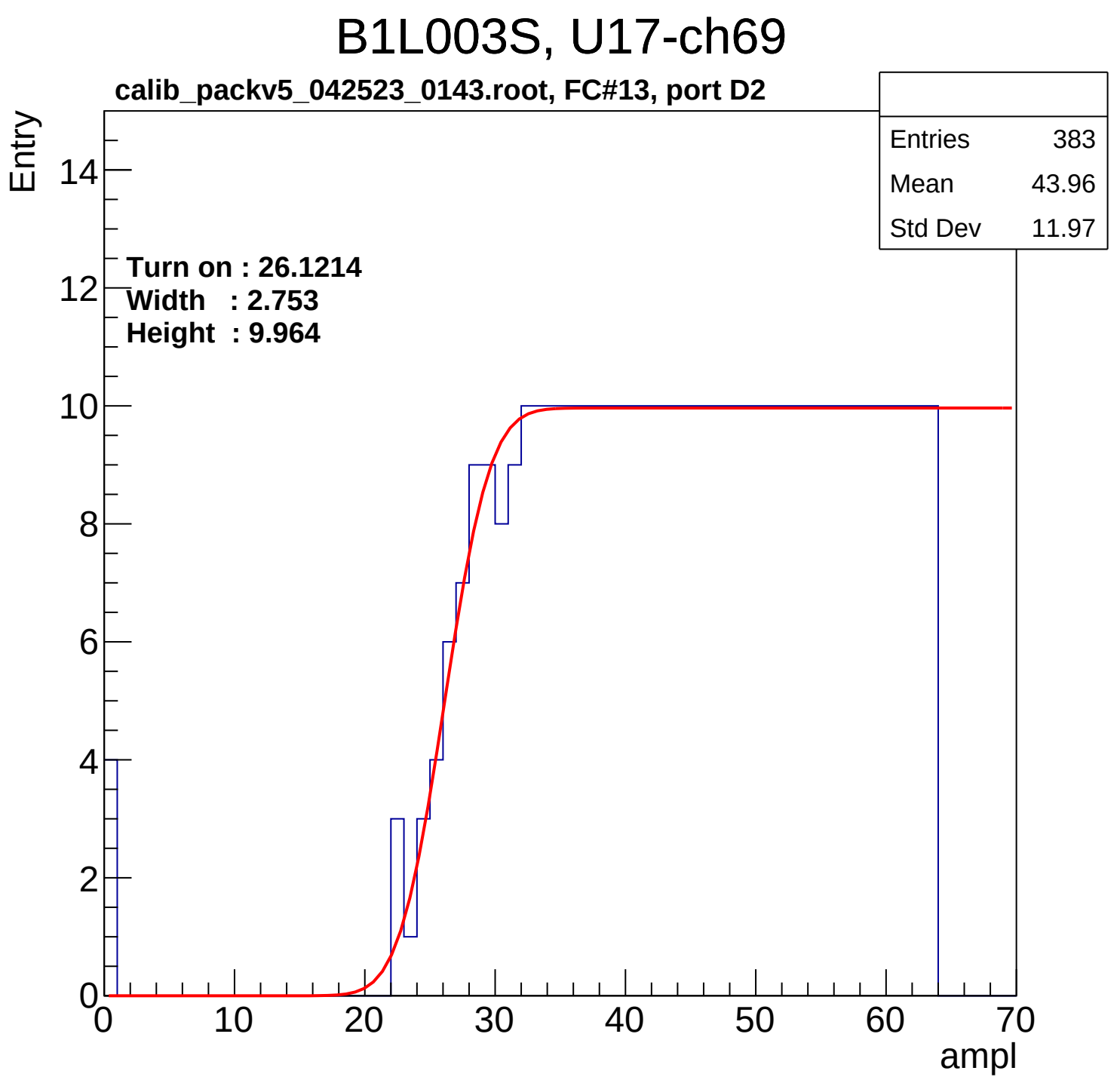
B1L003S, U17-ch69
calib_packv5_042523_0143.root, FC#13, port D2
Entries 383
Mean 43.96
Std Dev 11.97
Turn on : 26.1214
Width : 2.753
Height : 9.964
Entry
ampl
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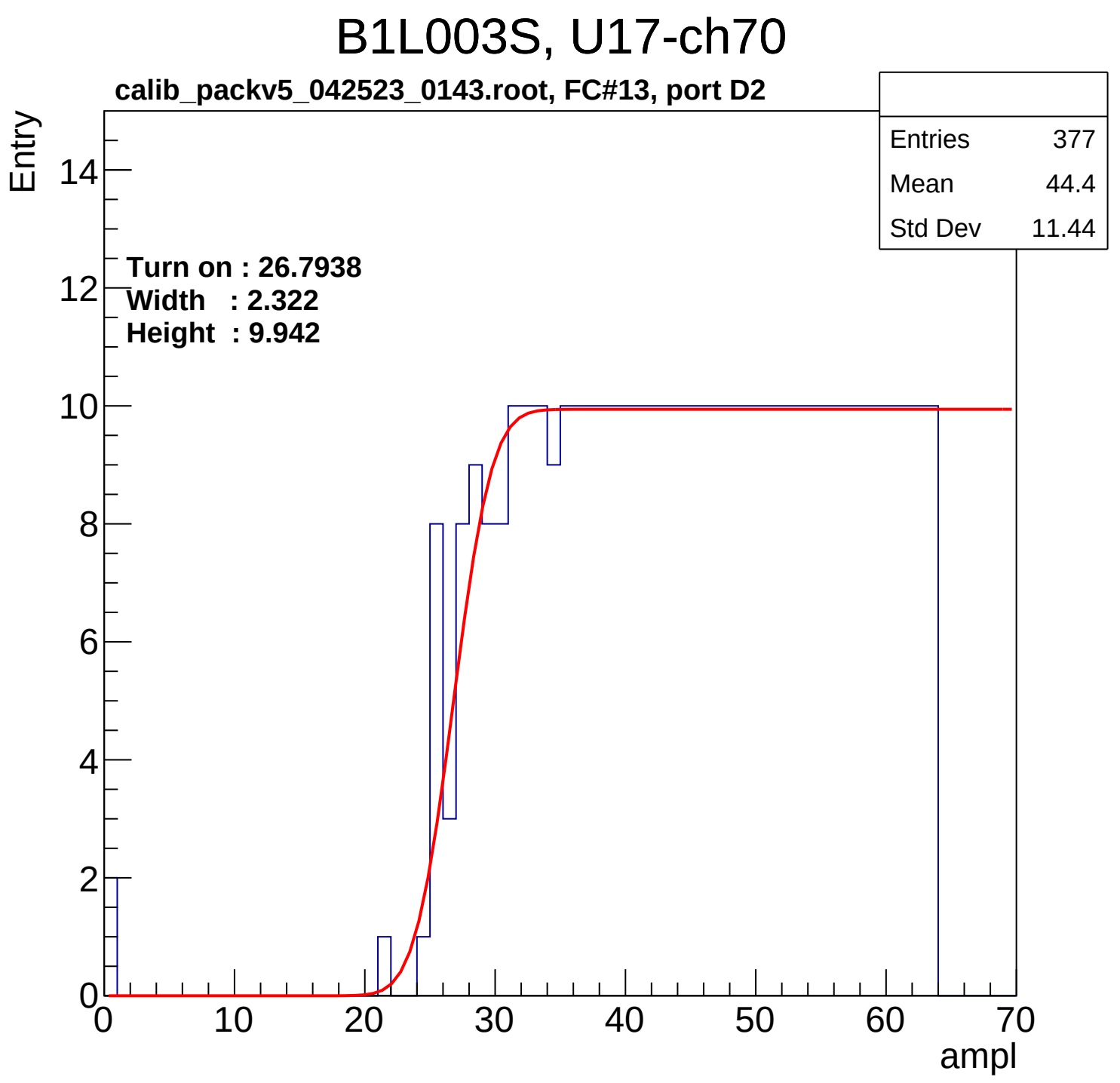
B1L003S, U17-ch70
calib_packv5_042523_0143.root, FC#13, port D2
Entries 377
Mean 44.4
Std Dev 11.44
Turn on : 26.7938
Width : 2.322
Height : 9.942
Entry
ampl
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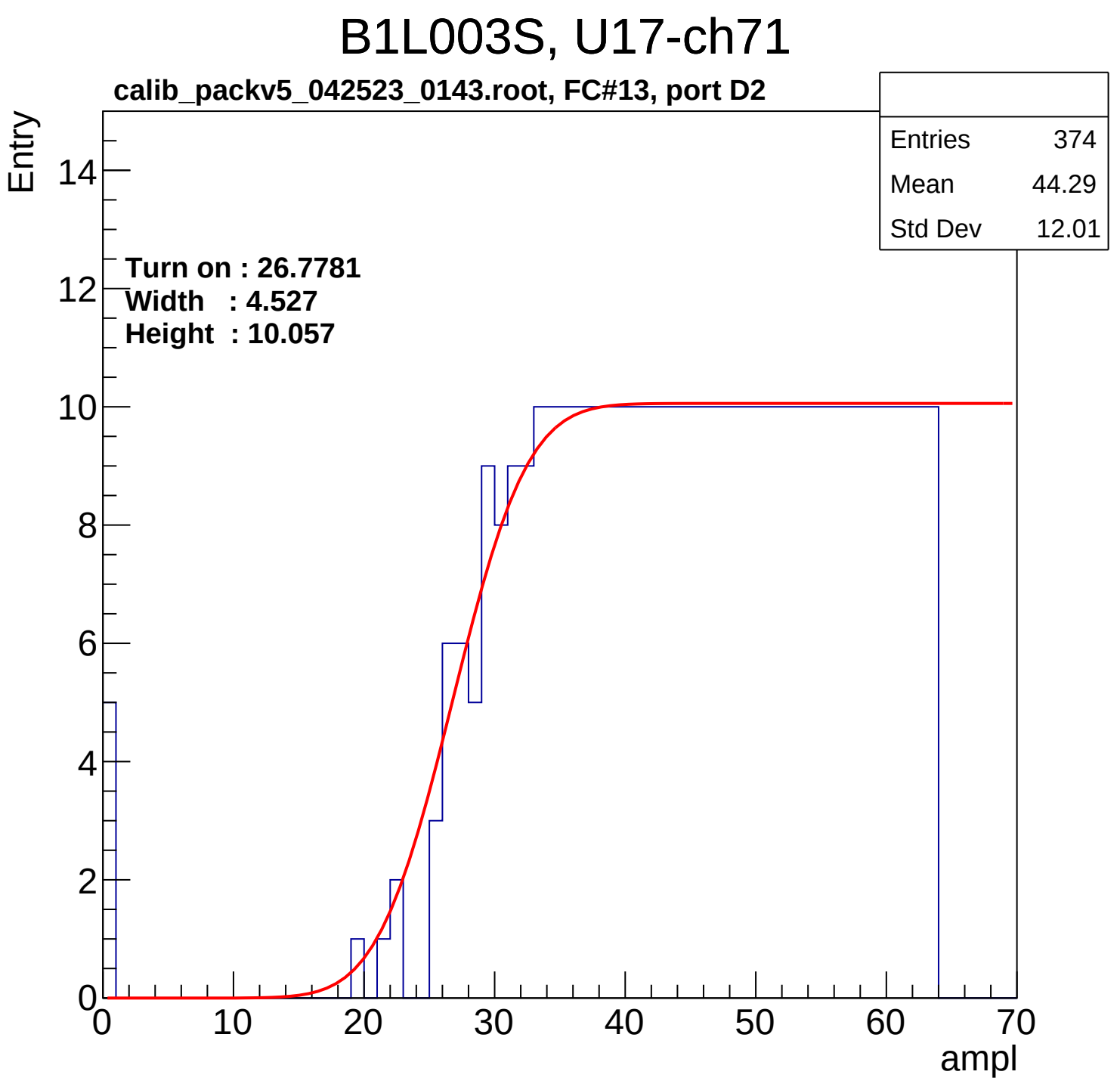
B1L003S, U17-ch71
calib_packv5_042523_0143.root, FC#13, port D2
Entries 374
Mean 44.29
Std Dev 12.01
Turn on : 26.7781
Width : 4.527
Height : 10.057
Entry
ampl
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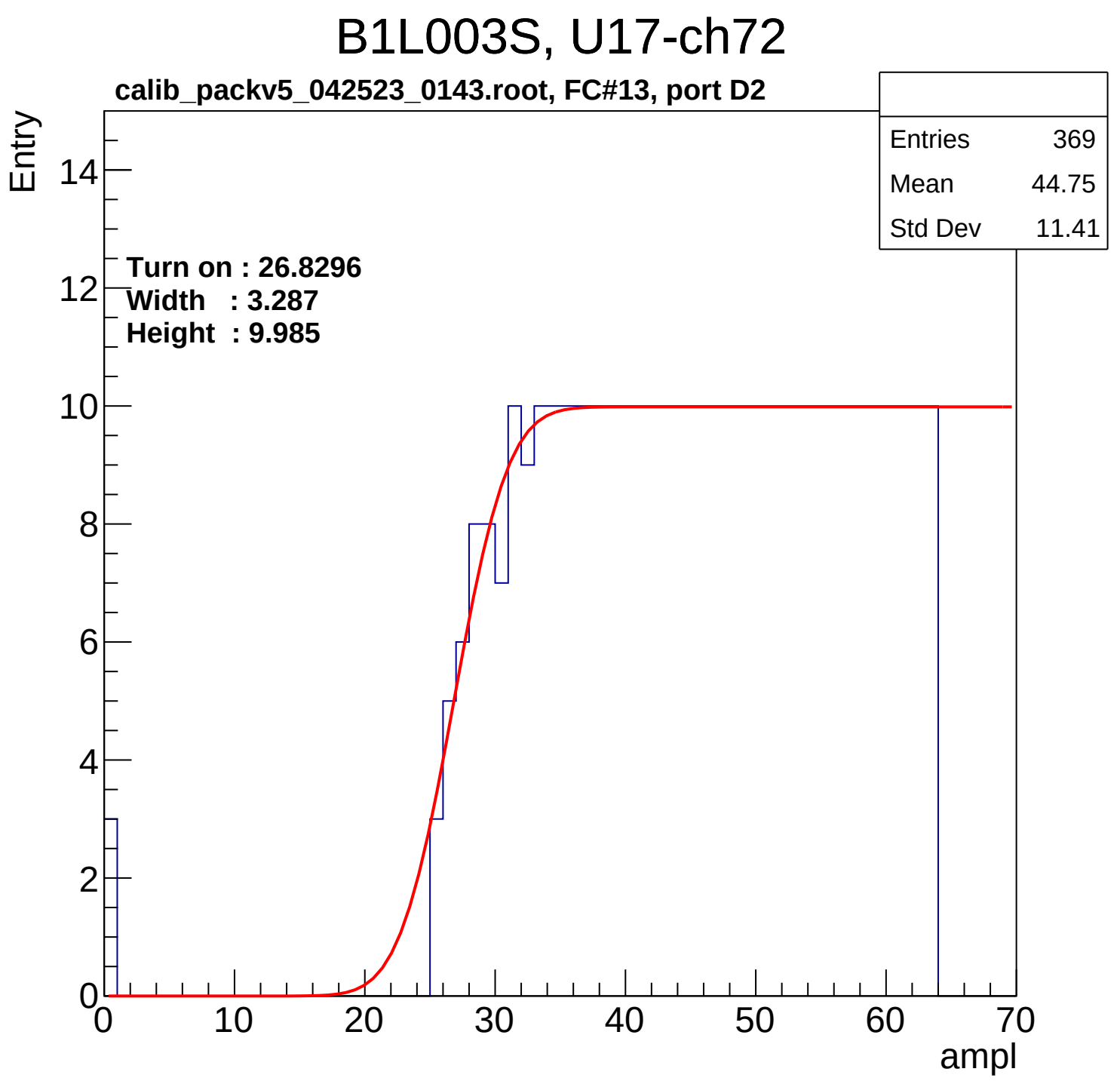
B1L003S, U17-ch72
calib_packv5_042523_0143.root, FC#13, port D2
Entries 369
Mean 44.75
Std Dev 11.41
Turn on : 26.8296
Width : 3.287
Height : 9.985
Entry
ampl
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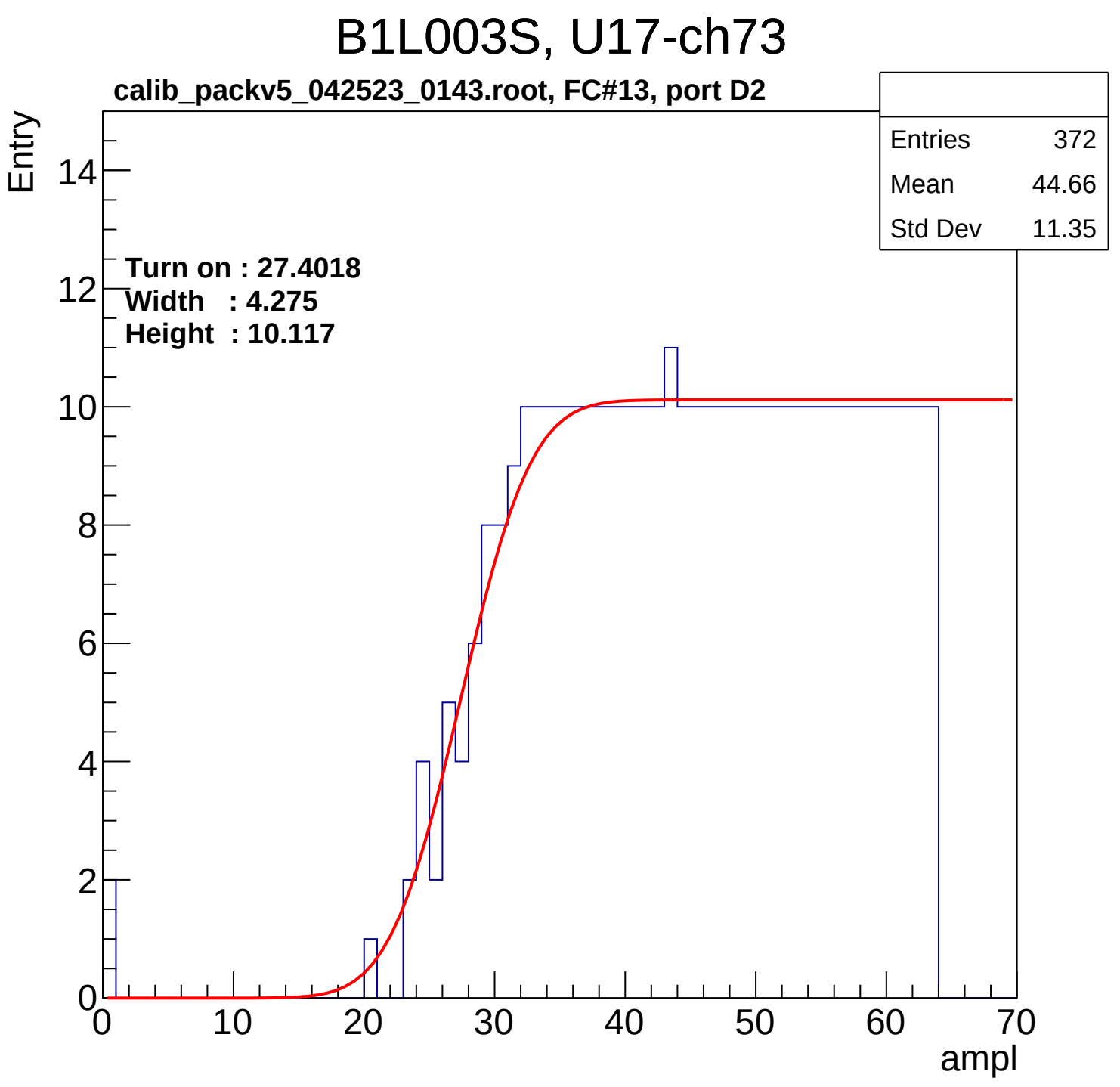
B1L003S, U17-ch73
calib_packv5_042523_0143.root, FC#13, port D2
Entries 372
Mean 44.66
Std Dev 11.35
Turn on : 27.4018
Width : 4.275
Height : 10.117
Entry
ampl
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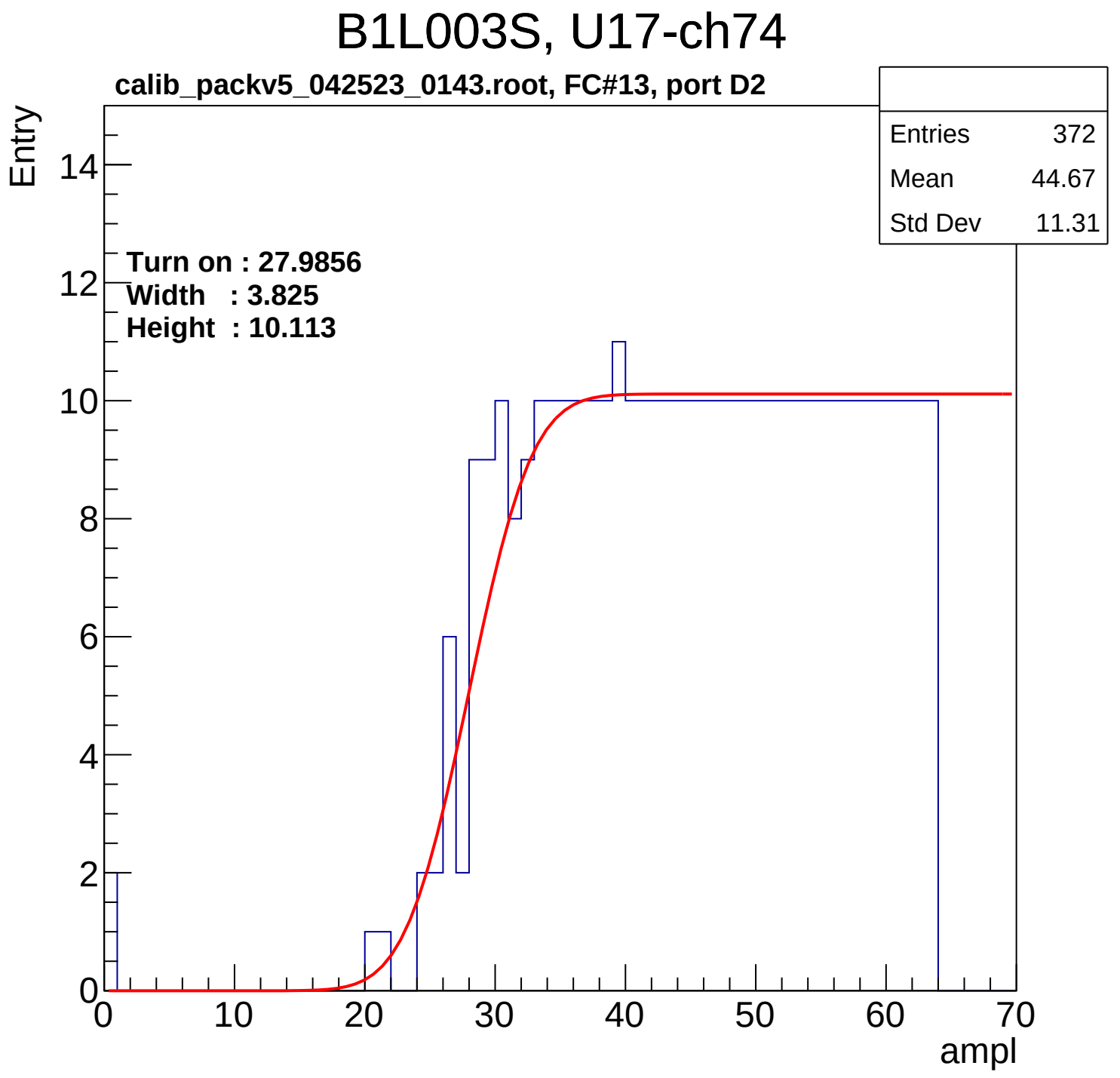
B1L003S, U17-ch74
calib_packv5_042523_0143.root, FC#13, port D2
Entries 372
Mean 44.67
Std Dev 11.31
Turn on : 27.9856
Width : 3.825
Height : 10.113
Entry
ampl
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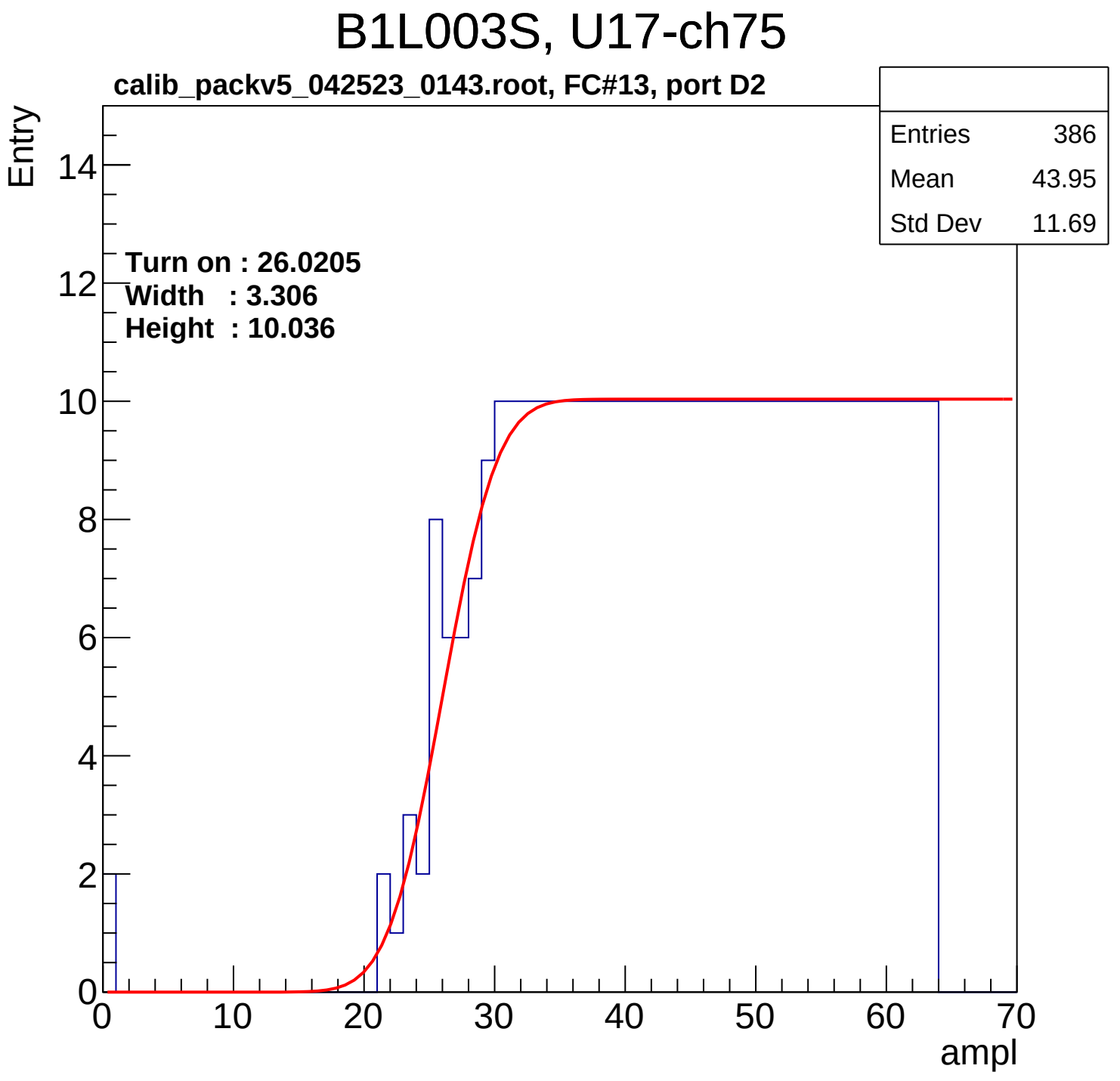
B1L003S, U17-ch75
calib_packv5_042523_0143.root, FC#13, port D2
Entries 386
Mean 43.95
Std Dev 11.69
Turn on : 26.0205
Width : 3.306
Height : 10.036
Entry
ampl
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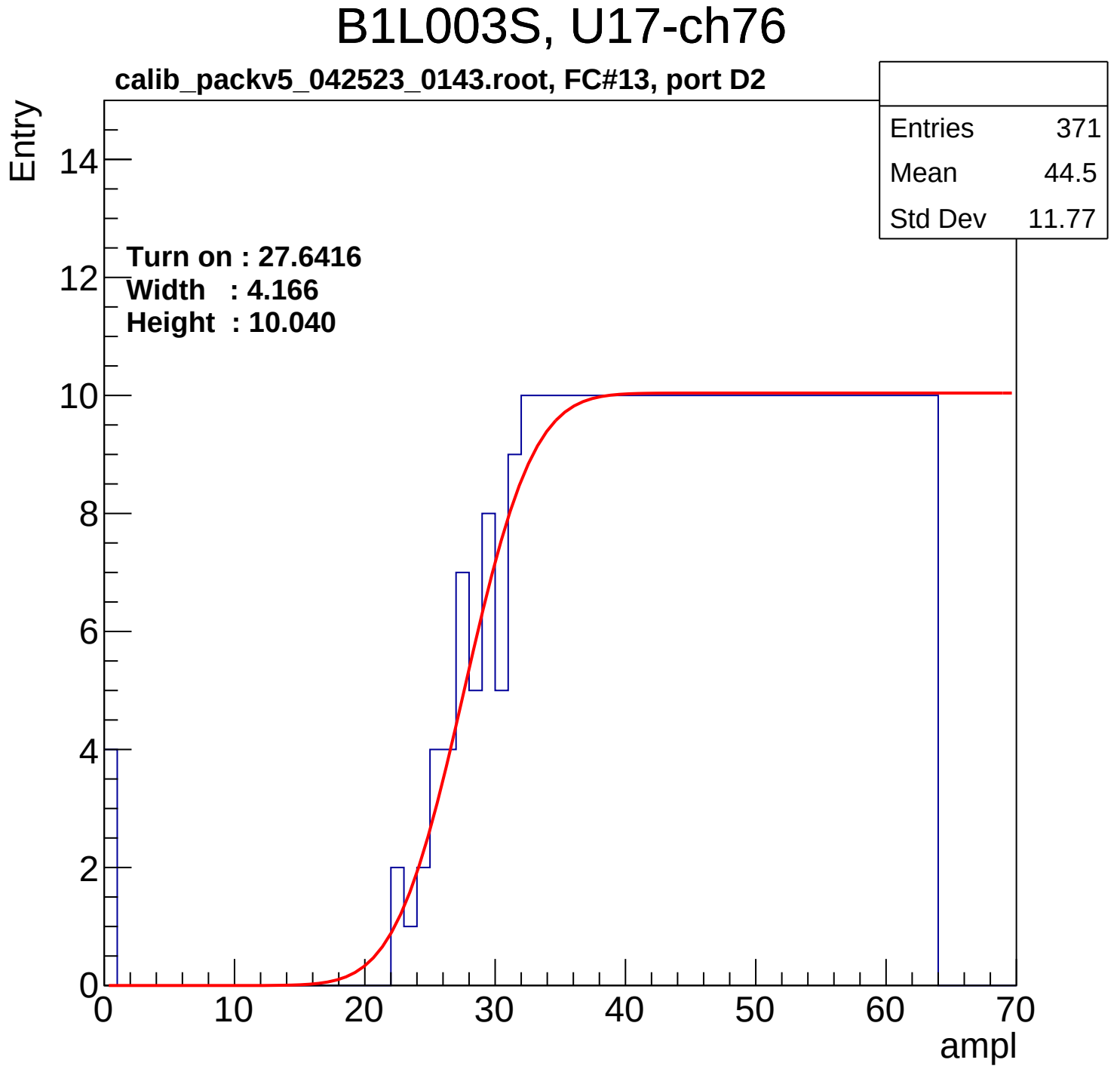
B1L003S, U17-ch76
calib_packv5_042523_0143.root, FC#13, port D2
Entries 371
Mean 44.5
Std Dev 11.77
Turn on : 27.6416
Width : 4.166
Height : 10.040
Entry
ampl
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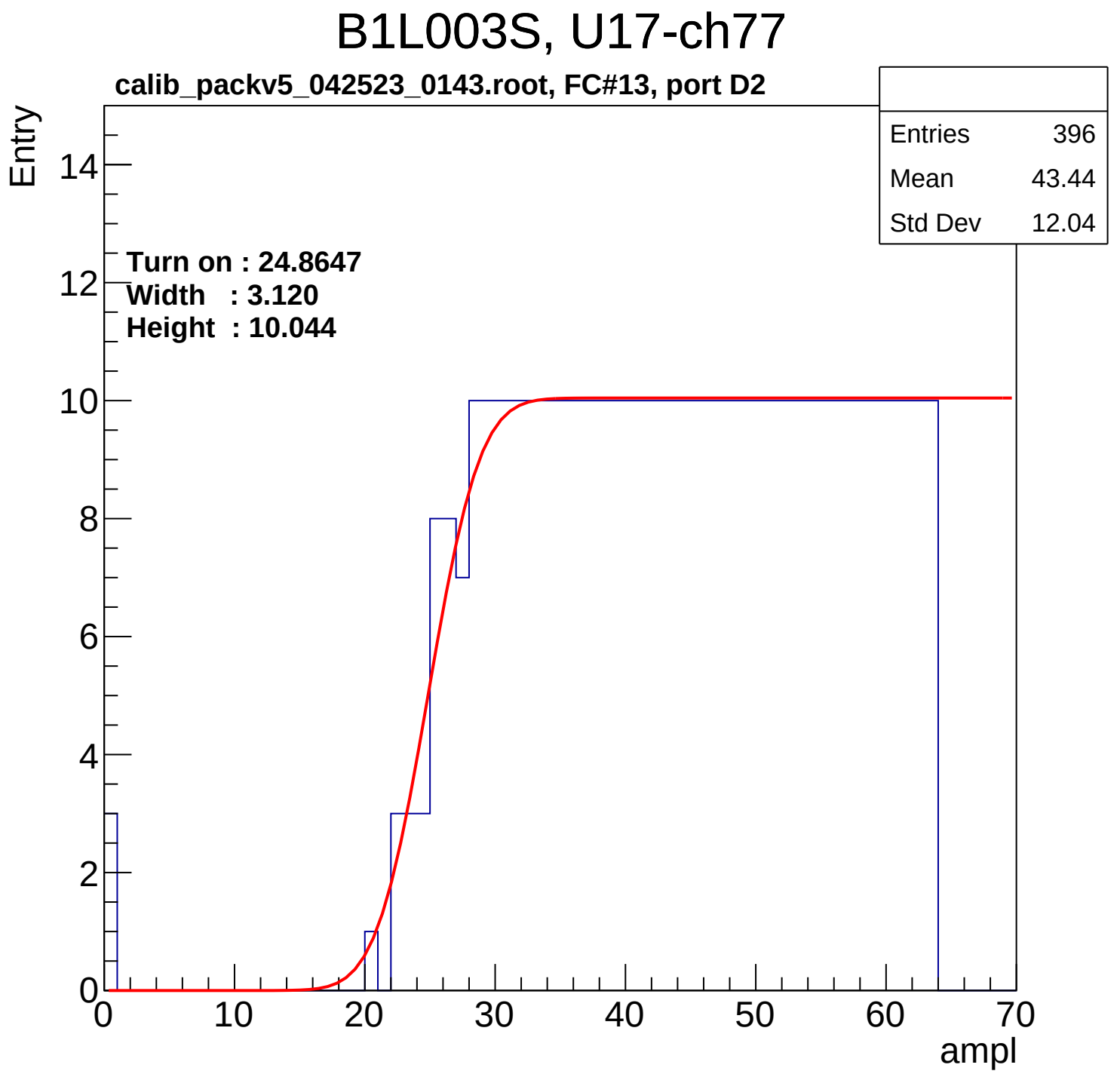
B1L003S, U17-ch77
calib_packv5_042523_0143.root, FC#13, port D2
Entries 396
Mean 43.44
Std Dev 12.04
Turn on : 24.8647
Width : 3.120
Height : 10.044
Entry
ampl
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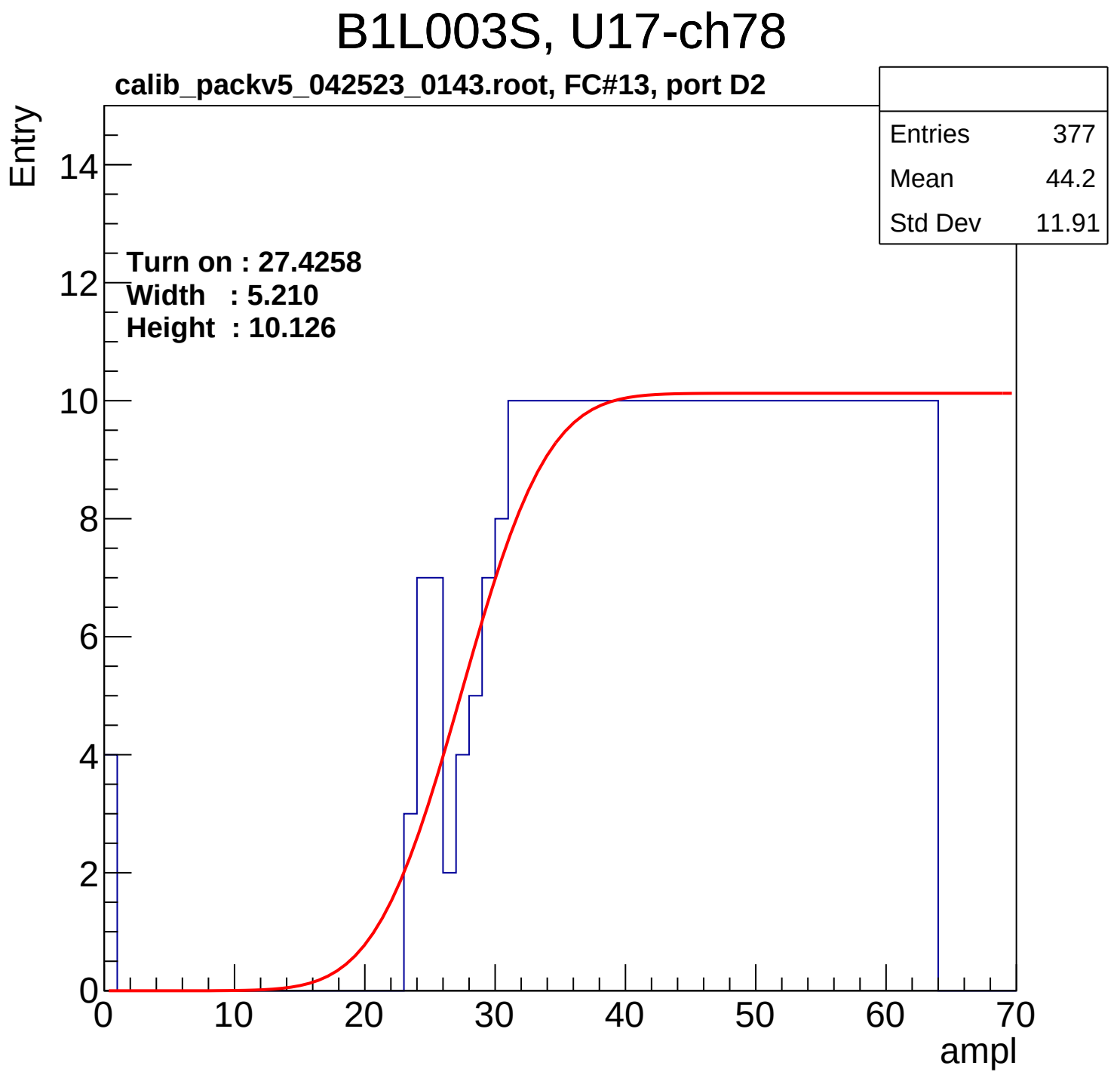
B1L003S, U17-ch78
calib_packv5_042523_0143.root, FC#13, port D2
Entries 377
Mean 44.2
Std Dev 11.91
Turn on : 27.4258
Width : 5.210
Height : 10.126
Entry
ampl
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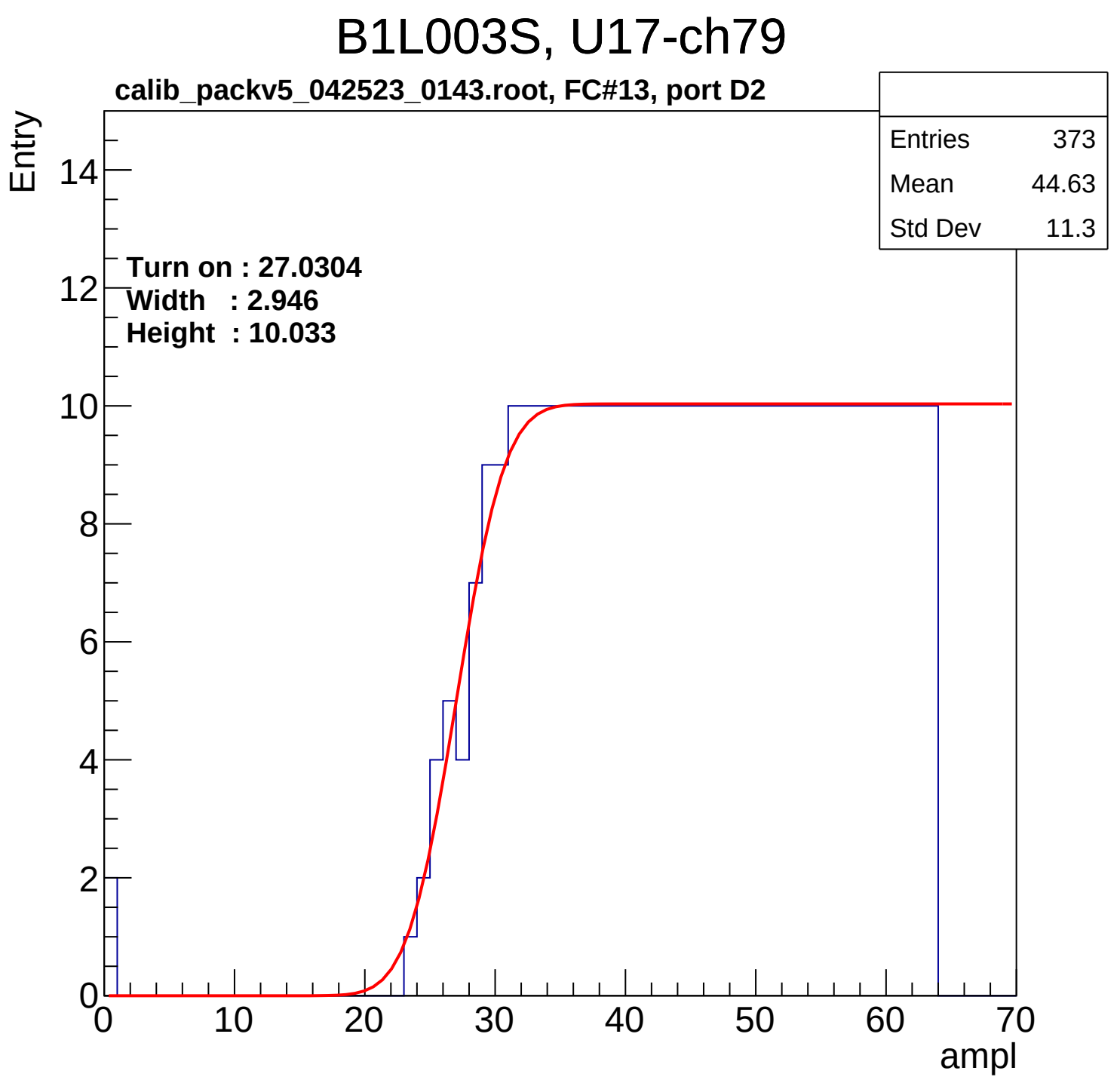
B1L003S, U17-ch79
calib_packv5_042523_0143.root, FC#13, port D2
Entries 373
Mean 44.63
Std Dev 11.3
Turn on : 27.0304
Width : 2.946
Height : 10.033
Entry
ampl
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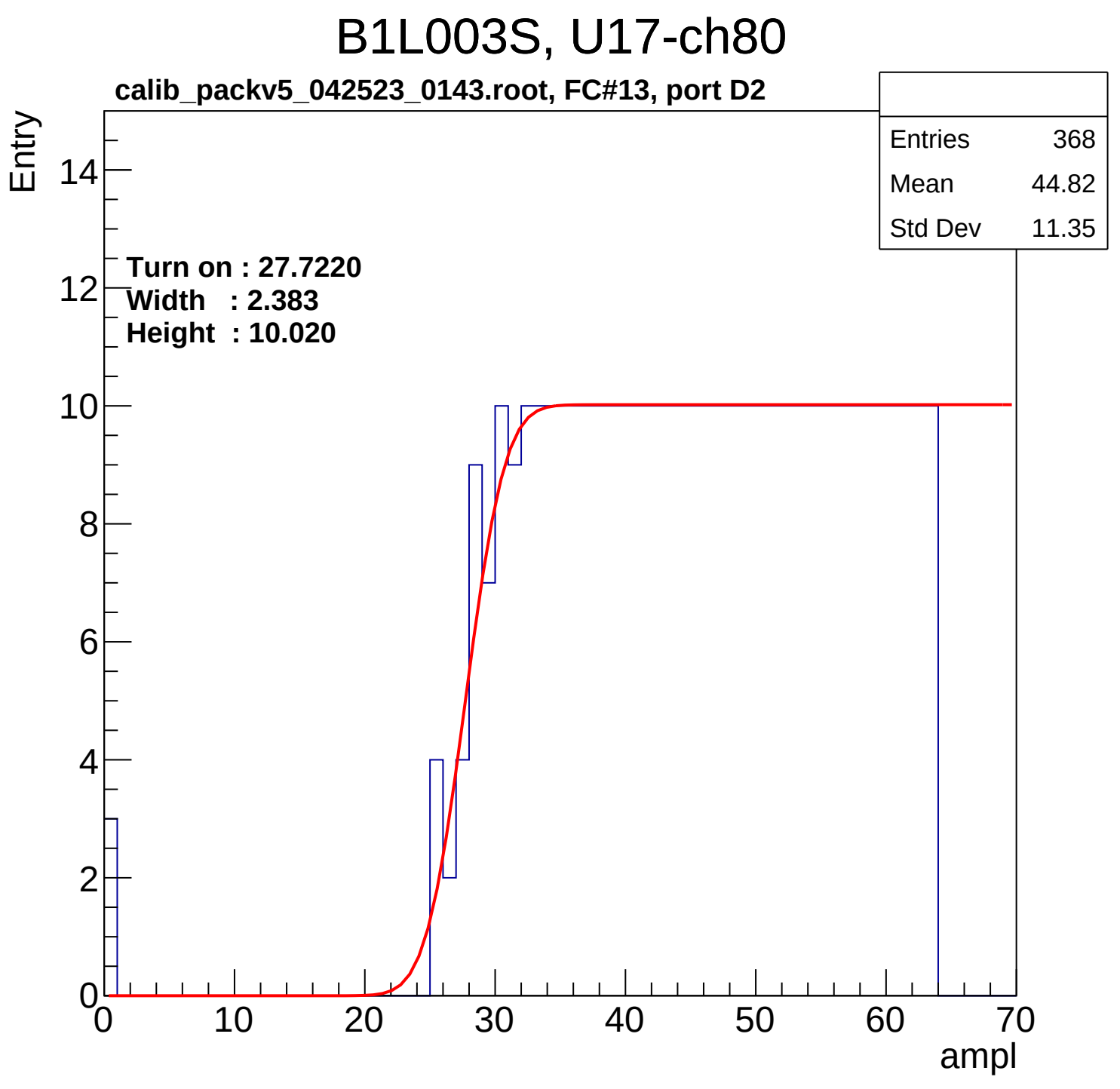
B1L003S, U17-ch80
calib_packv5_042523_0143.root, FC#13, port D2
Entries 368
Mean 44.82
Std Dev 11.35
Turn on : 27.7220
Width : 2.383
Height : 10.020
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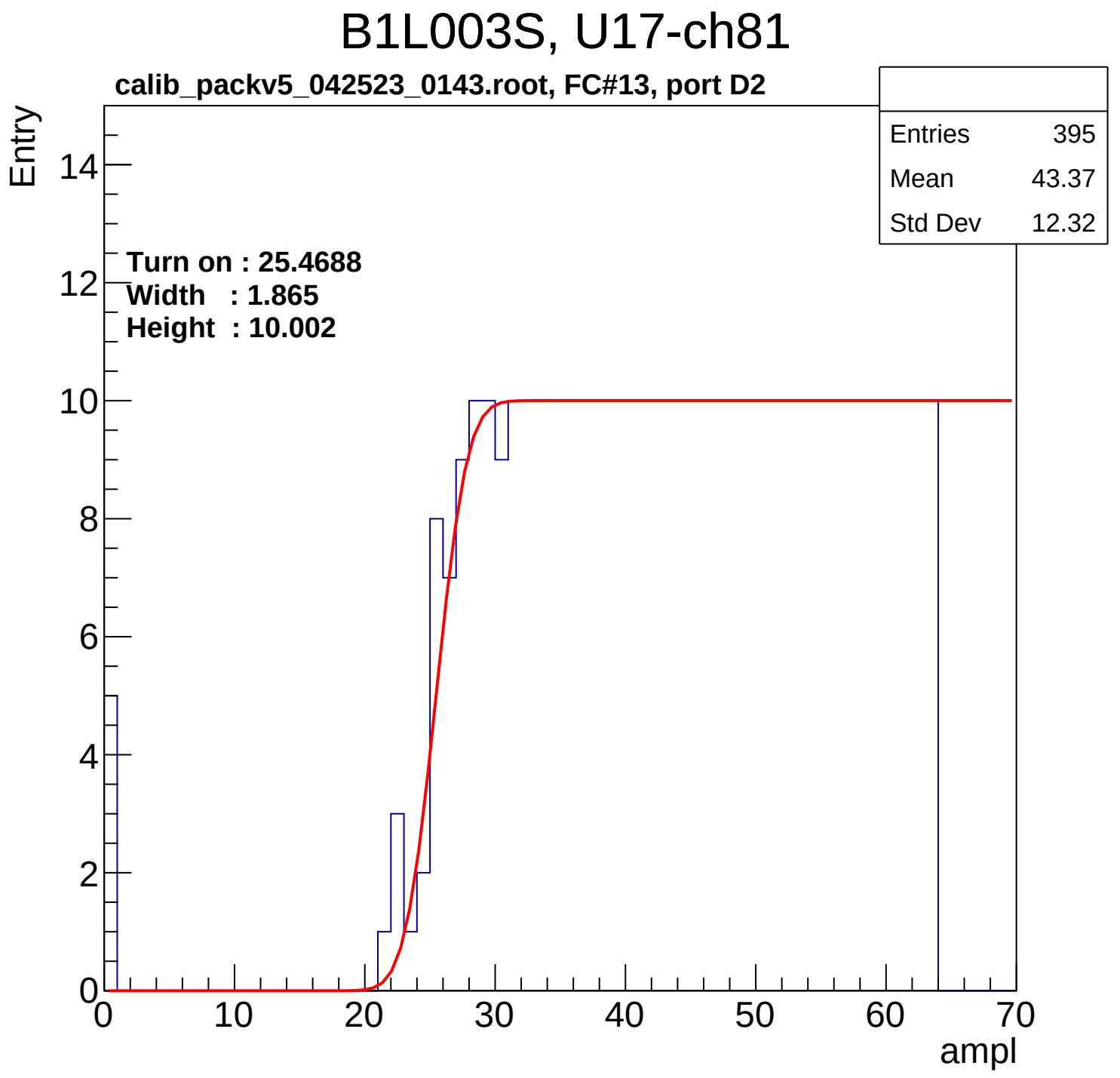
B1L003S, U17-ch81
calib_packv5_042523_0143.root, FC#13, port D2
Entries 395
Mean 43.37
Std Dev 12.32
Turn on : 25.4688
Width : 1.865
Height : 10.002
Entry
ampl
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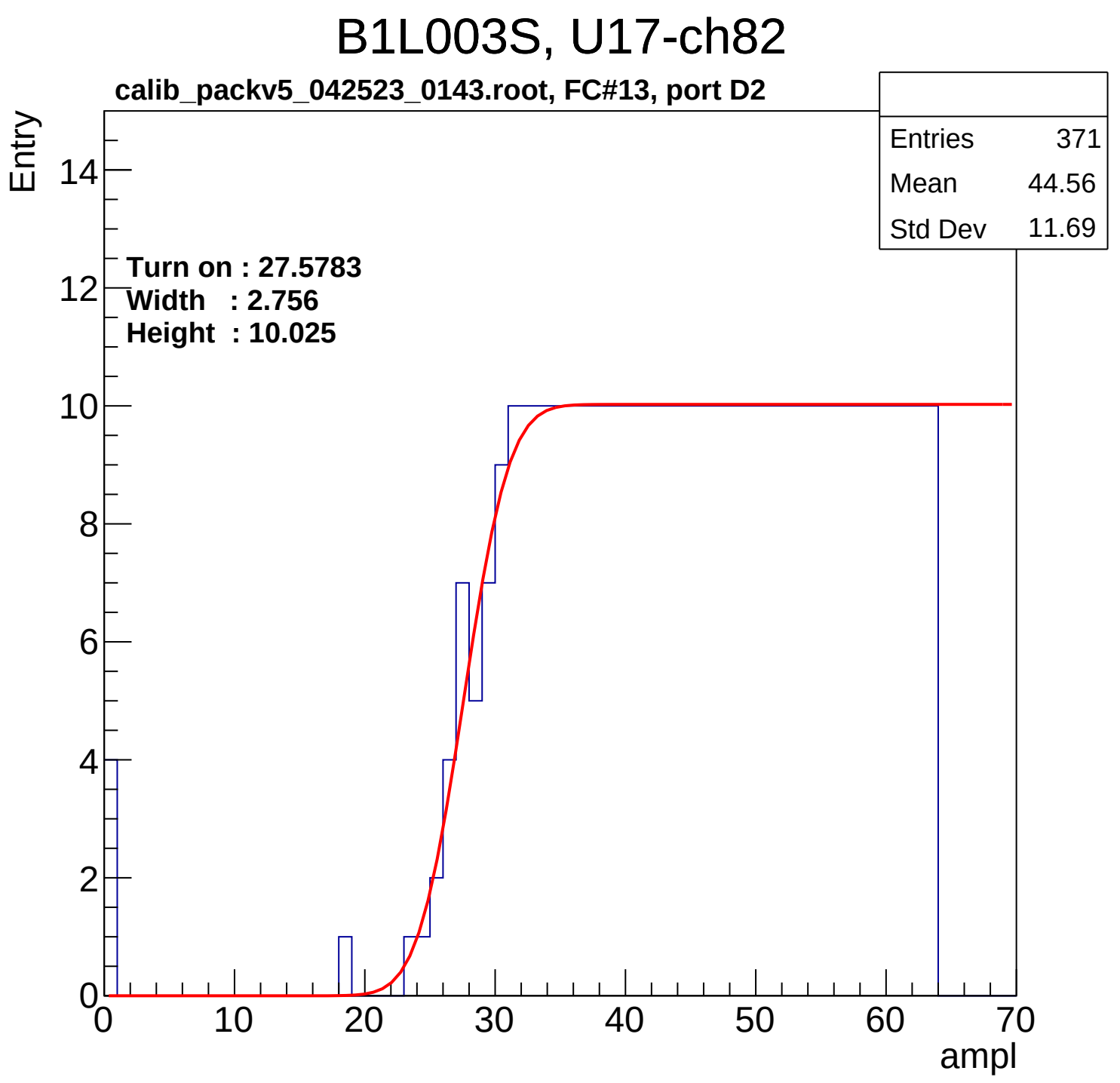
B1L003S, U17-ch82
calib_packv5_042523_0143.root, FC#13, port D2
Entries 371
Mean 44.56
Std Dev 11.69
Turn on : 27.5783
Width : 2.756
Height : 10.025
Entry
ampl
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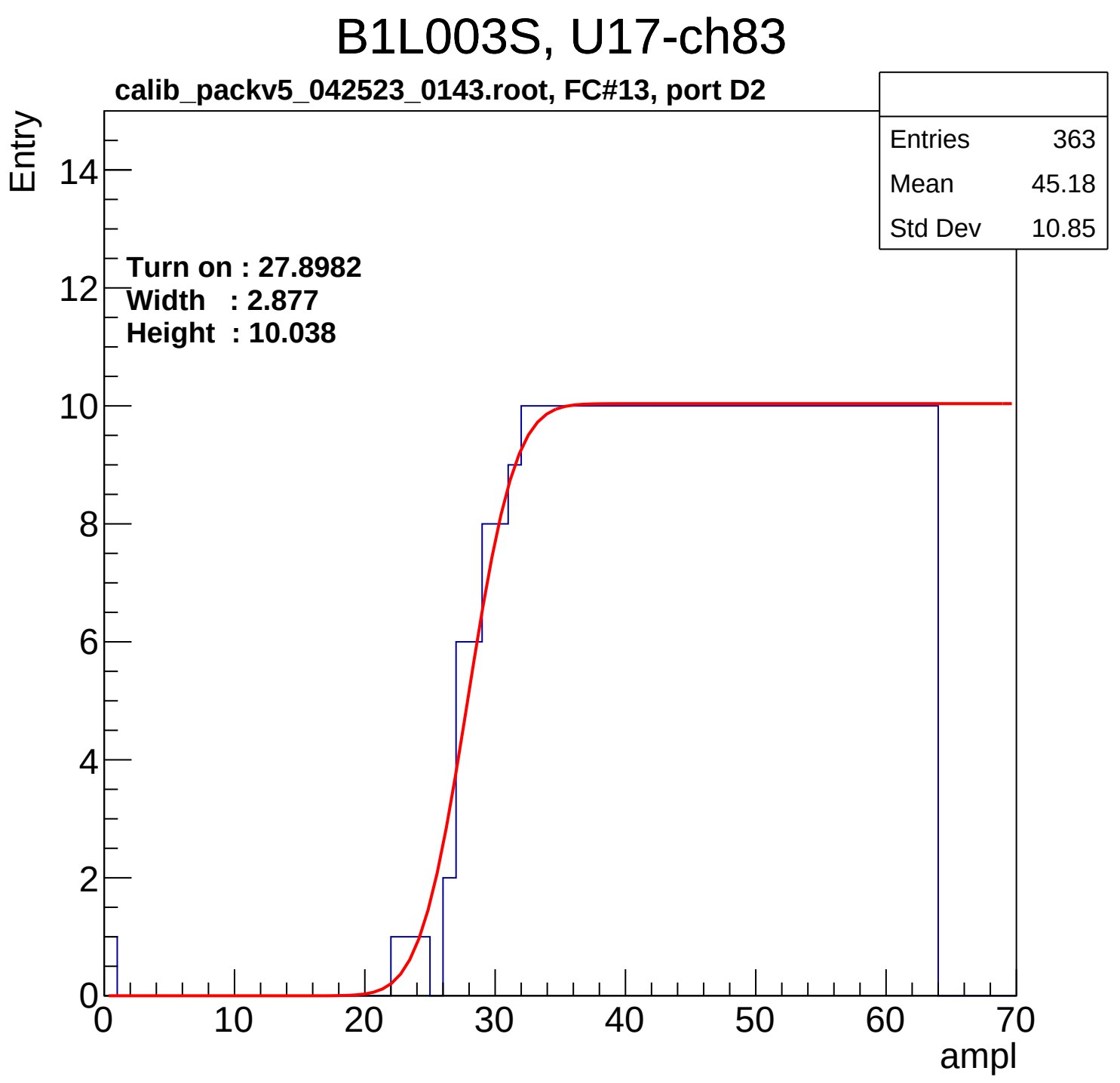
B1L003S, U17-ch83
calib_packv5_042523_0143.root, FC#13, port D2
Entries 363
Mean 45.18
Std Dev 10.85
Turn on : 27.8982
Width : 2.877
Height : 10.038
Entry
ampl
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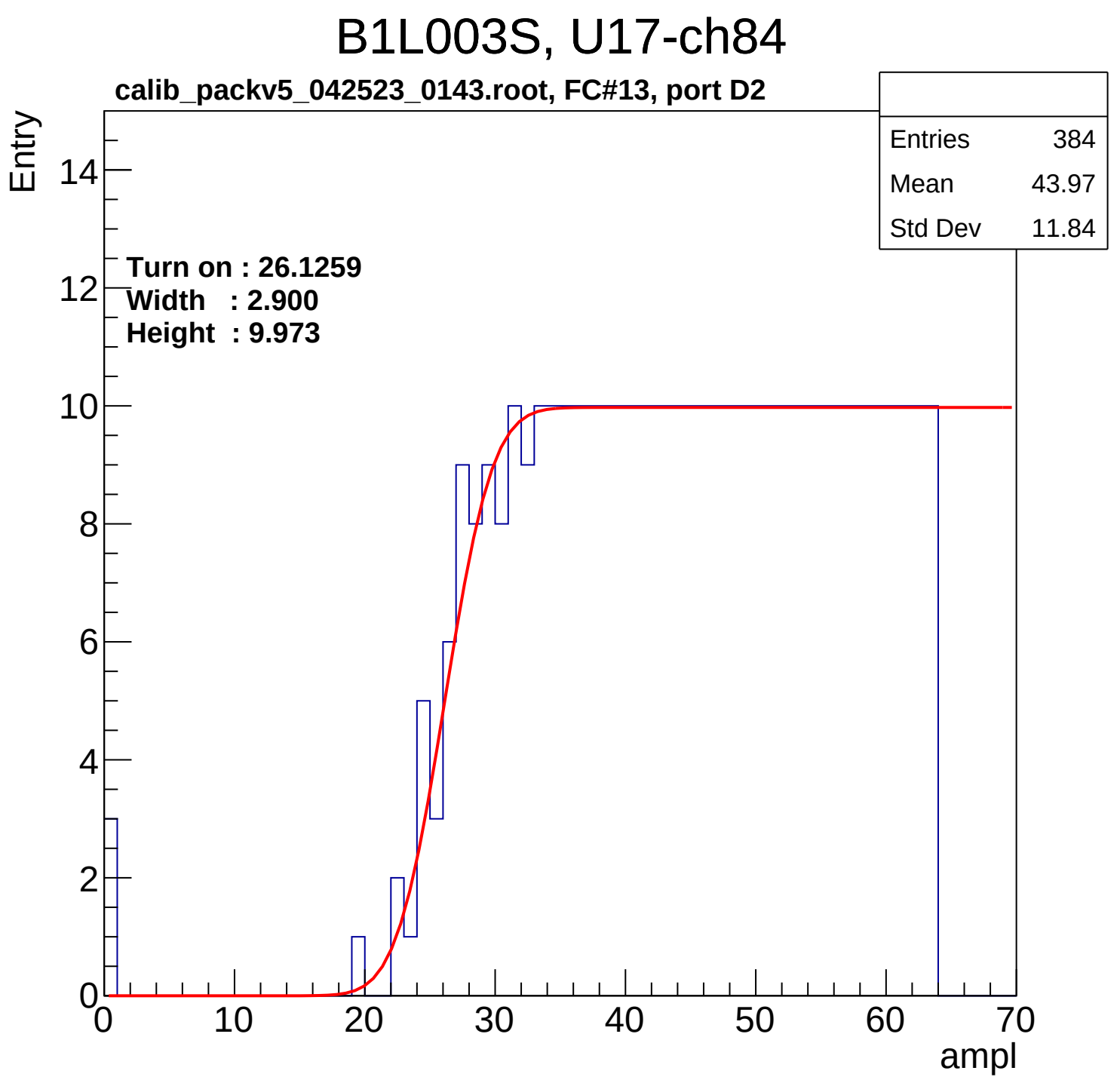
B1L003S, U17-ch84
calib_packv5_042523_0143.root, FC#13, port D2
Entries 384
Mean 43.97
Std Dev 11.84
Turn on : 26.1259
Width : 2.900
Height : 9.973
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ampl
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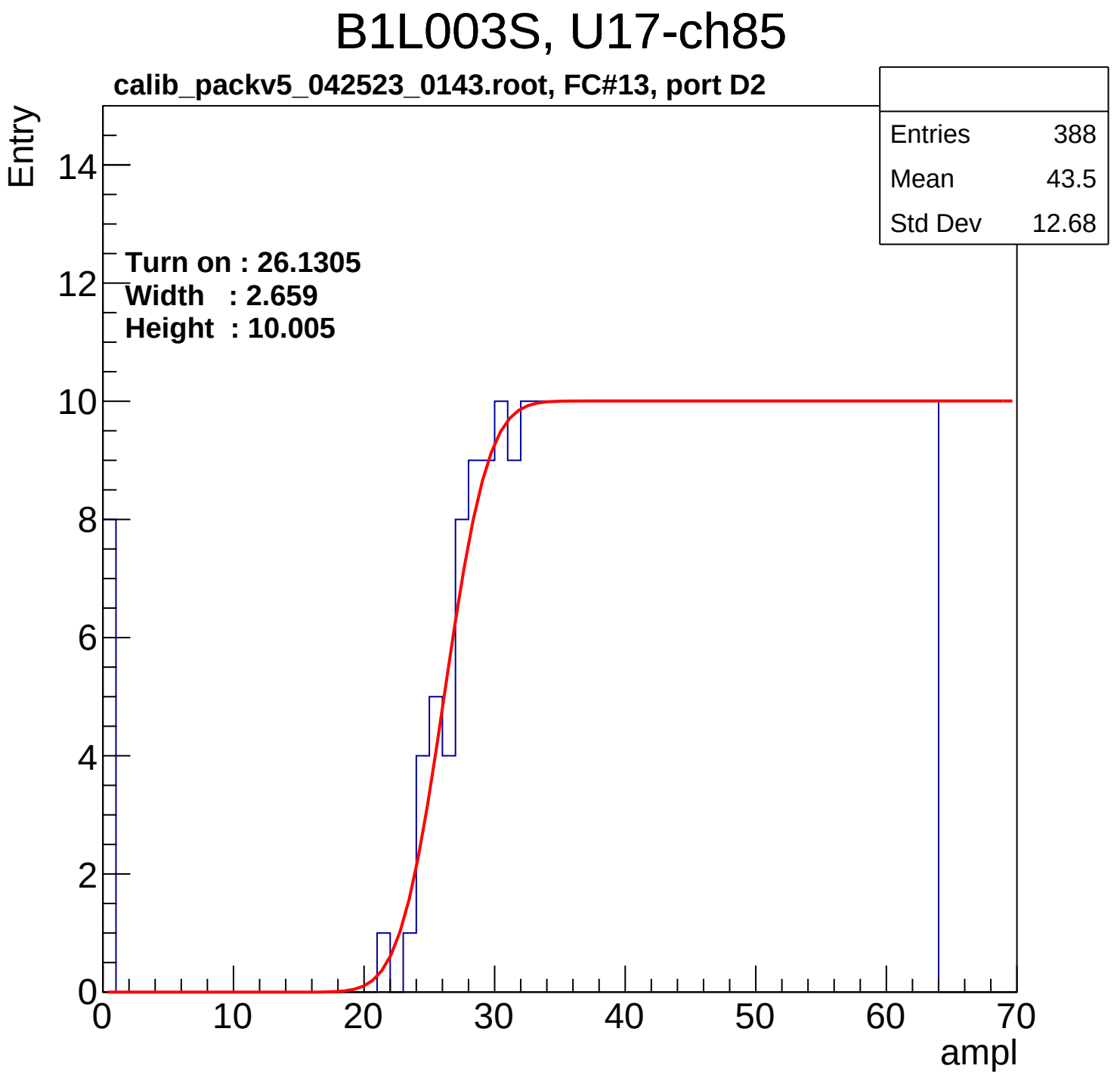
B1L003S, U17-ch85
calib_packv5_042523_0143.root, FC#13, port D2
Entries 388
Mean 43.5
Std Dev 12.68
Turn on : 26.1305
Width : 2.659
Height : 10.005
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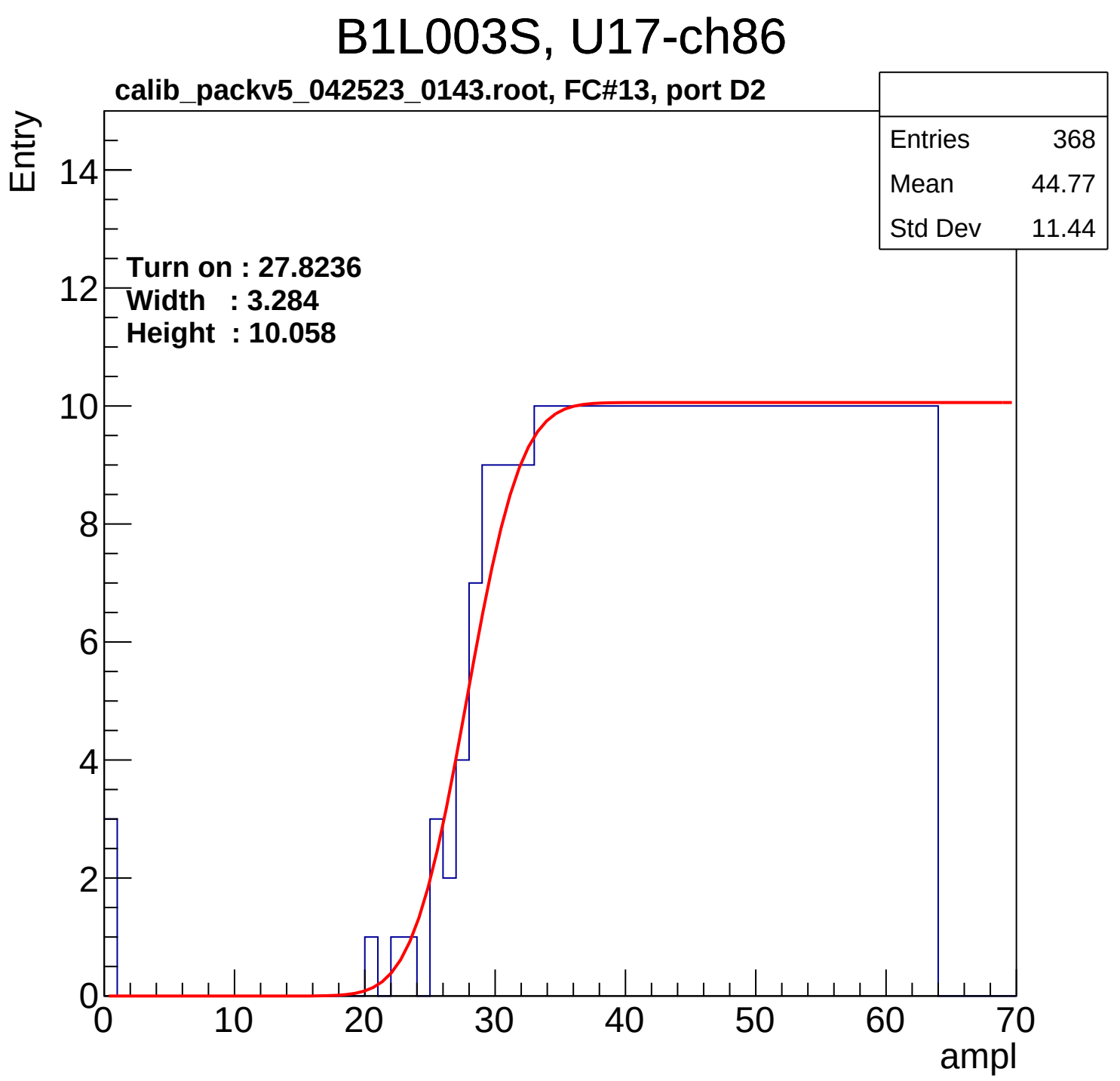
B1L003S, U17-ch86
calib_packv5_042523_0143.root, FC#13, port D2
Entries 368
Mean 44.77
Std Dev 11.44
Turn on : 27.8236
Width : 3.284
Height : 10.058
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ampl
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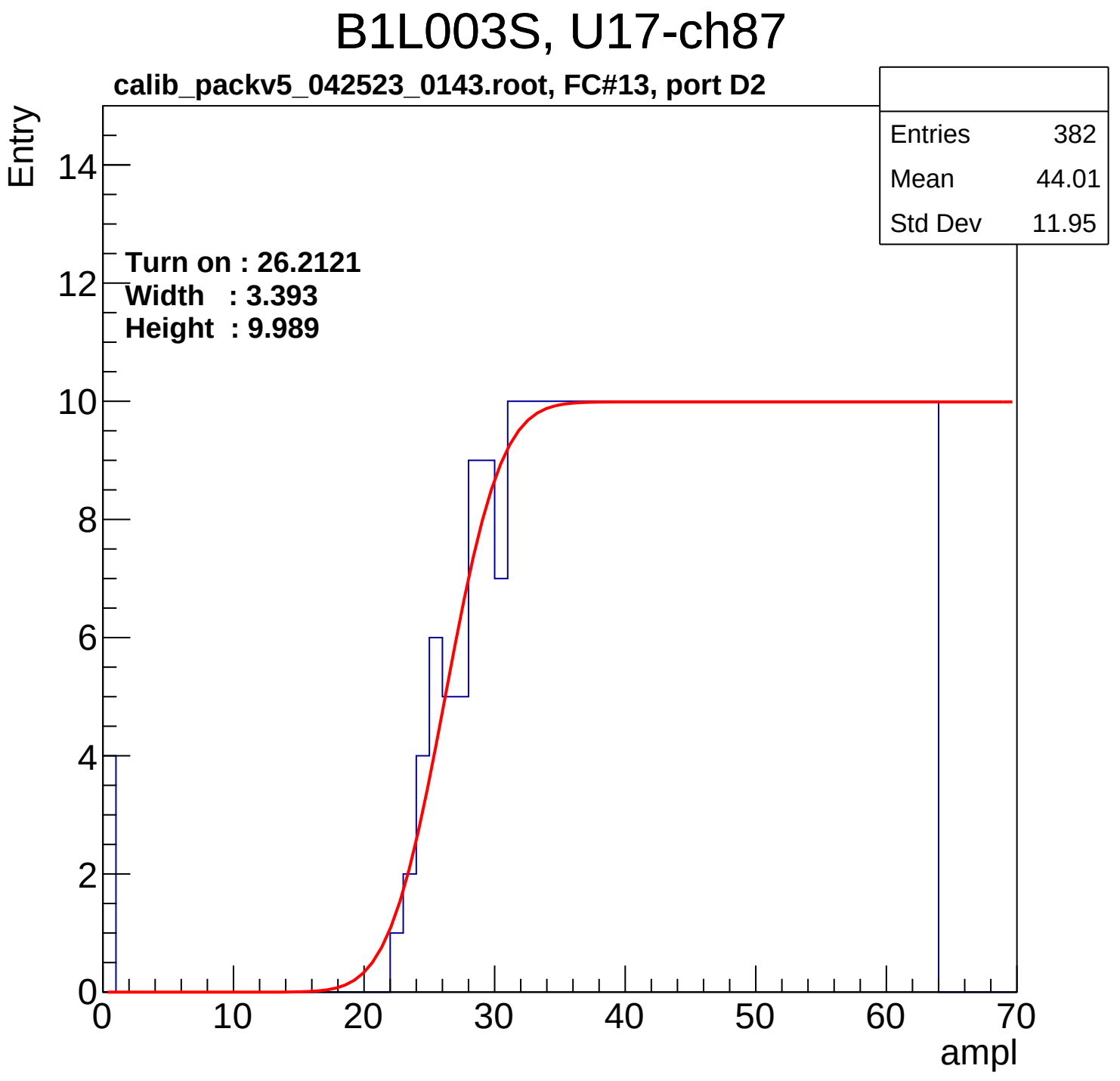
B1L003S, U17-ch87
calib_packv5_042523_0143.root, FC#13, port D2
Entries 382
Mean 44.01
Std Dev 11.95
Turn on : 26.2121
Width : 3.393
Height : 9.989
Entry
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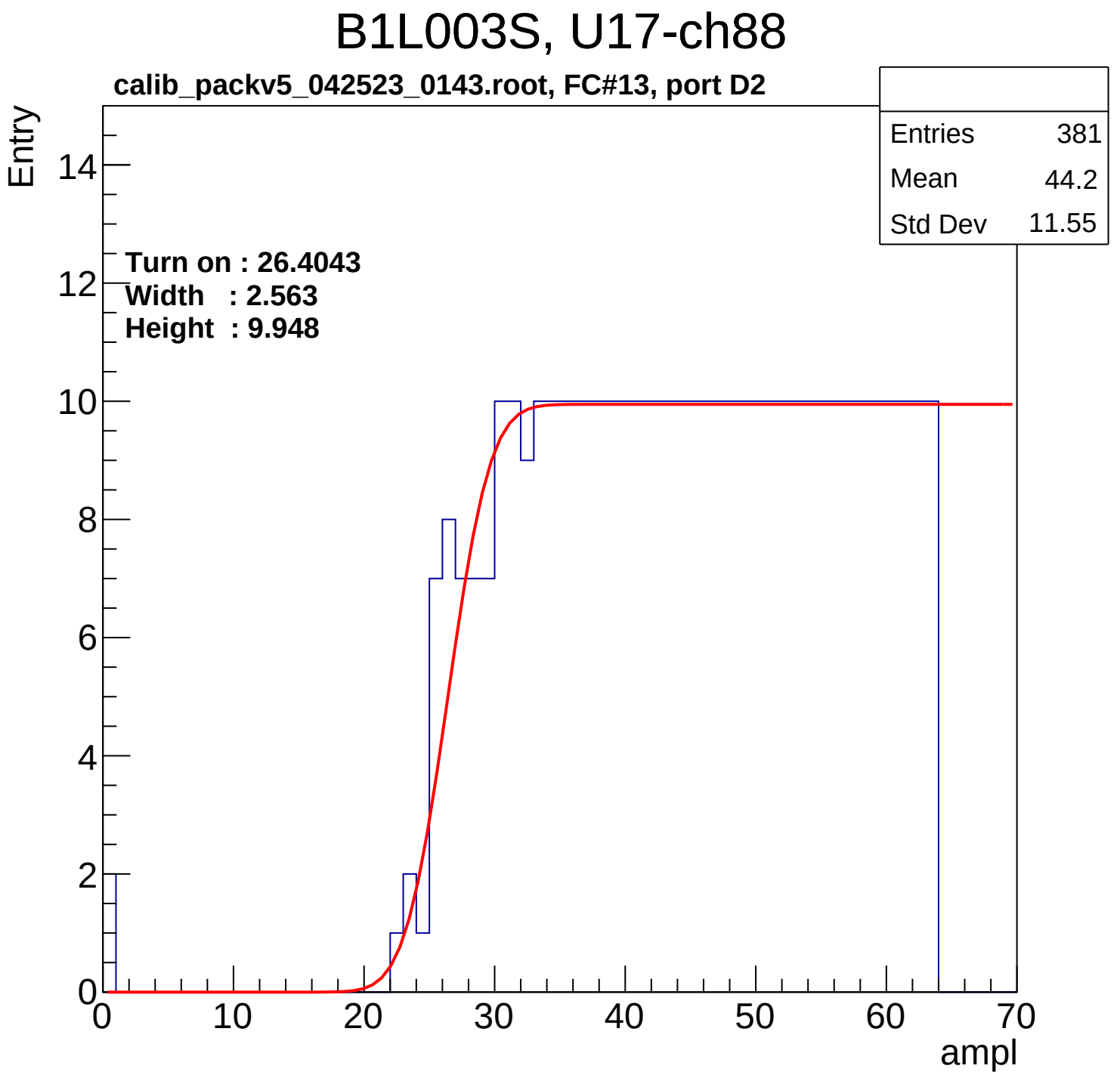
B1L003S, U17-ch88
calib_packv5_042523_0143.root, FC#13, port D2
Entries 381
Mean 44.2
Std Dev 11.55
Turn on : 26.4043
Width : 2.563
Height : 9.948
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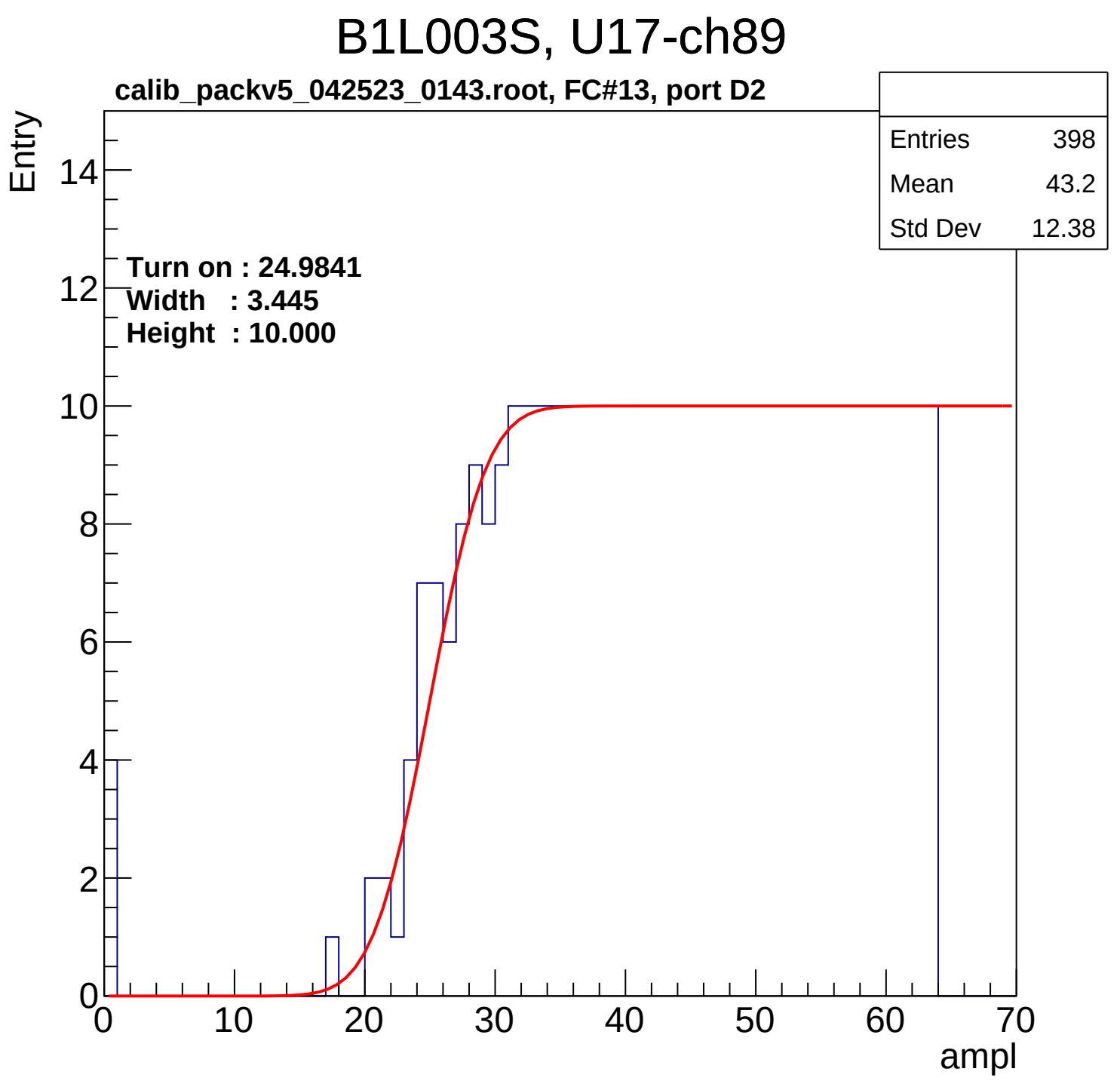
B1L003S, U17-ch89
calib_packv5_042523_0143.root, FC#13, port D2
Entries 398
Mean 43.2
Std Dev 12.38
Turn on : 24.9841
Width : 3.445
Height : 10.000
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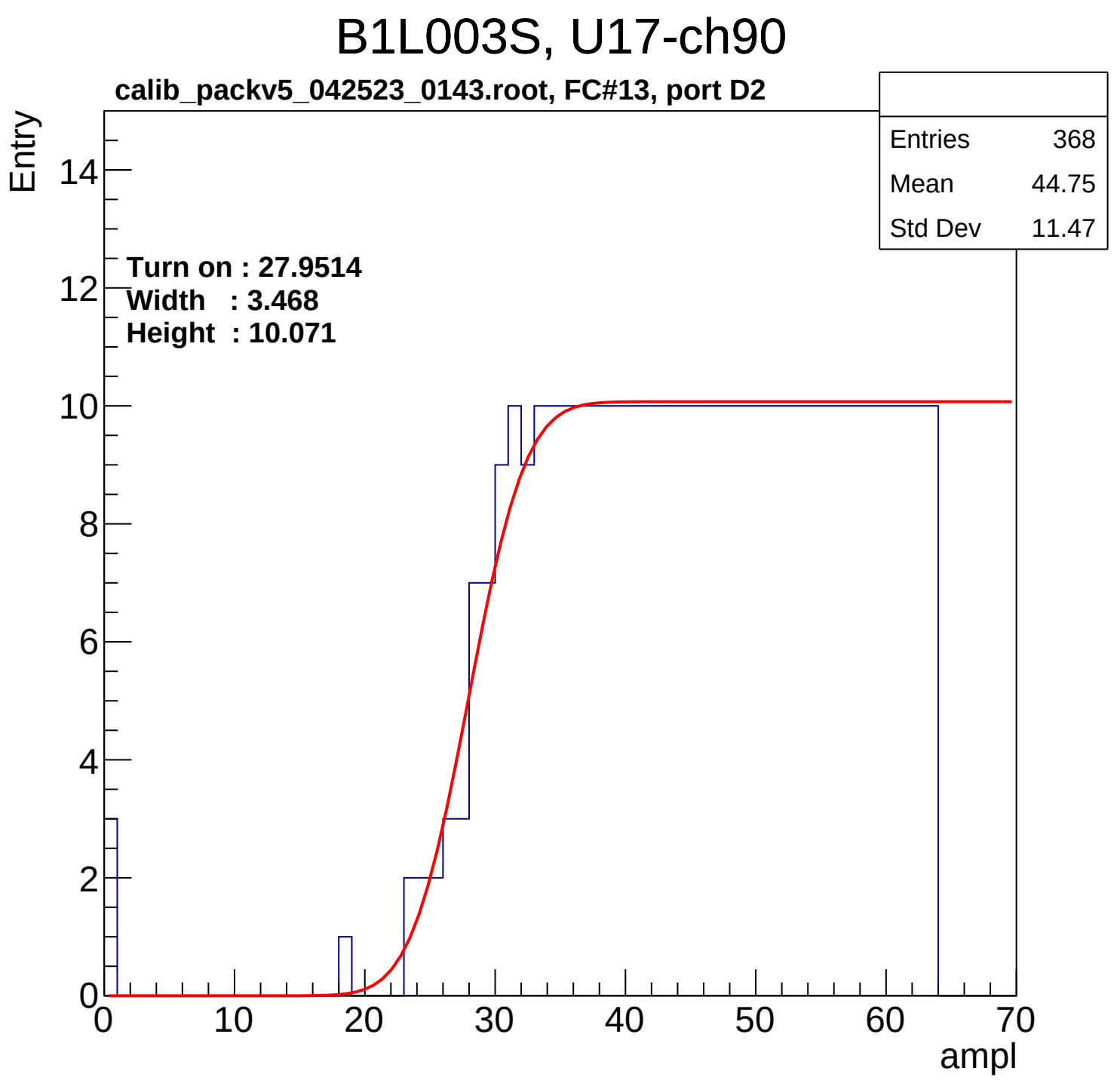
B1L003S, U17-ch90
calib_packv5_042523_0143.root, FC#13, port D2
Entries 368
Mean 44.75
Std Dev 11.47
Turn on : 27.9514
Width : 3.468
Height : 10.071
Entry
ampl
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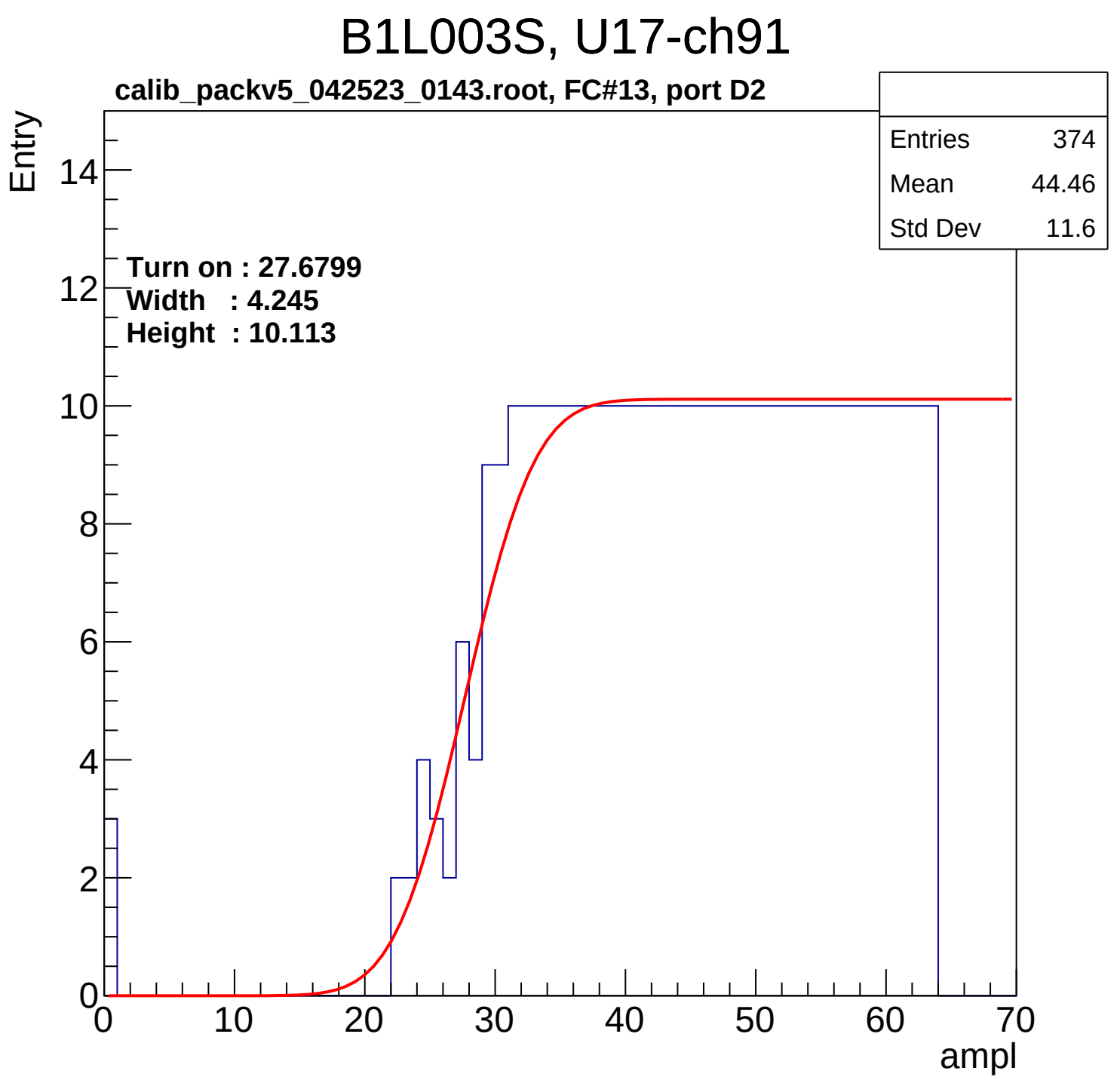
B1L003S, U17-ch91
calib_packv5_042523_0143.root, FC#13, port D2
Entries 374
Mean 44.46
Std Dev 11.6
Turn on : 27.6799
Width : 4.245
Height : 10.113
Entry
ampl
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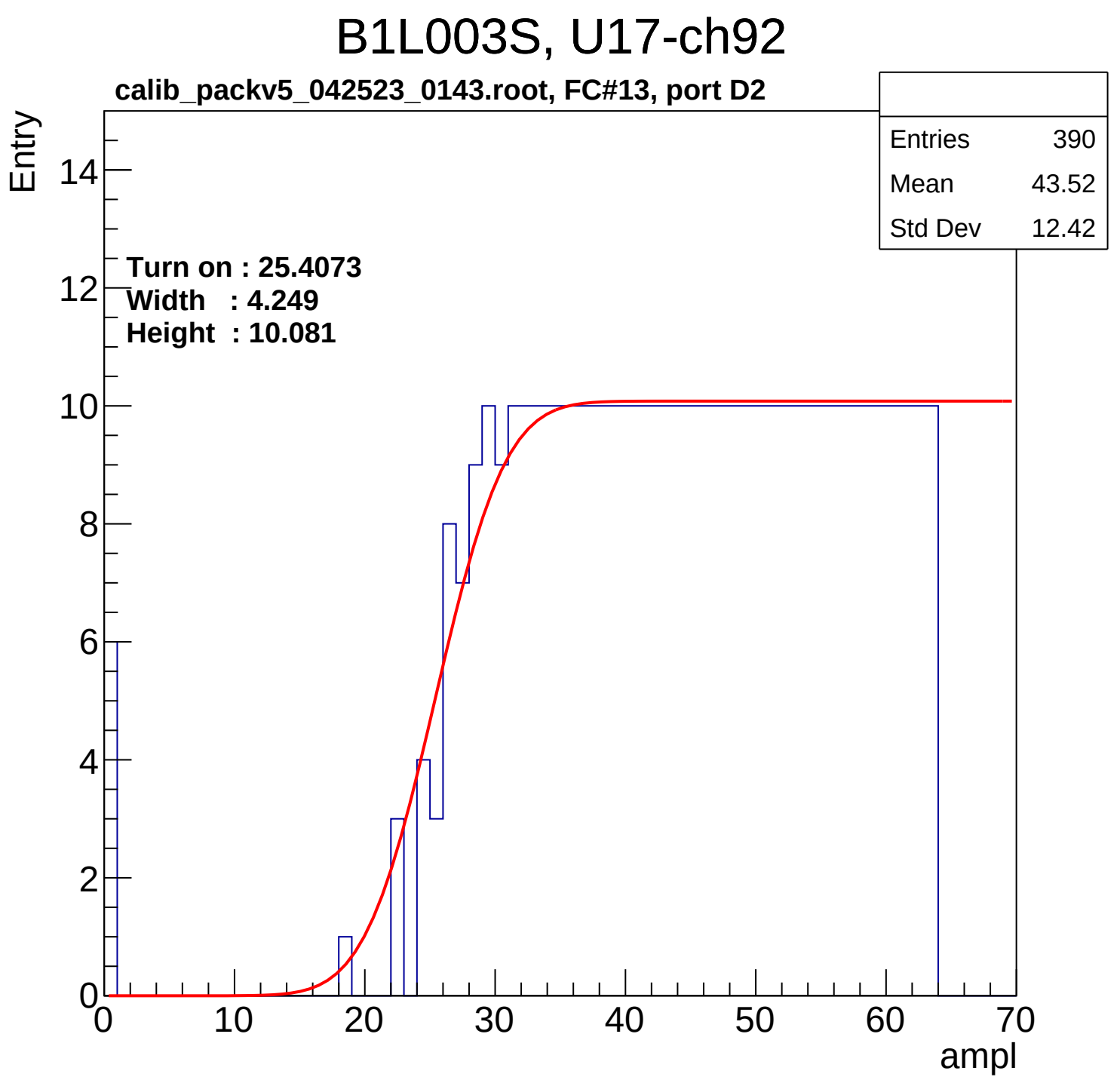
B1L003S, U17-ch92
calib_packv5_042523_0143.root, FC#13, port D2
Entries 390
Mean 43.52
Std Dev 12.42
Turn on : 25.4073
Width : 4.249
Height : 10.081
Entry
ampl
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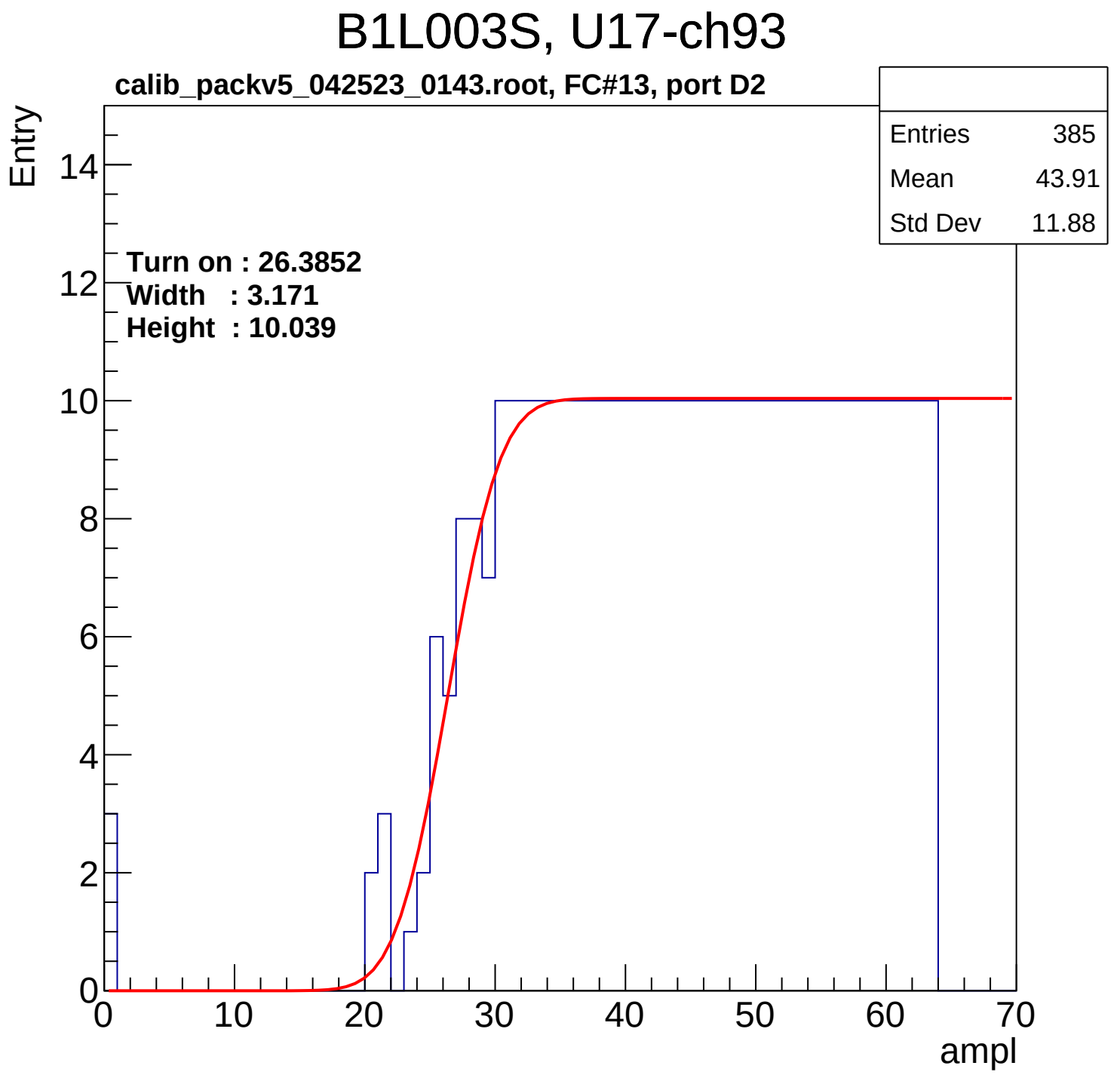
B1L003S, U17-ch93
calib_packv5_042523_0143.root, FC#13, port D2
Entries 385
Mean 43.91
Std Dev 11.88
Turn on : 26.3852
Width : 3.171
Height : 10.039
Entry
ampl
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2
4
6
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12
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60
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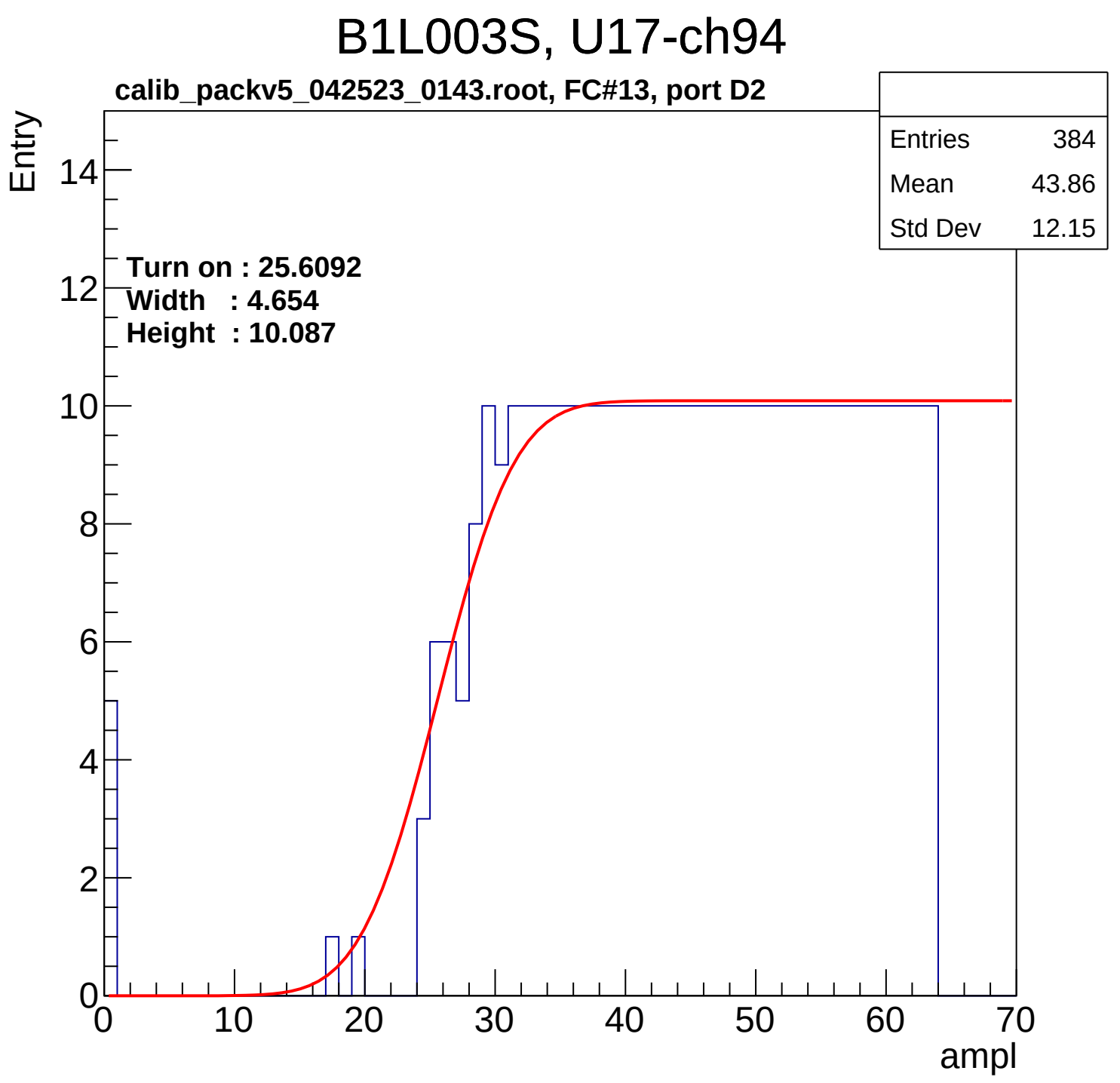
B1L003S, U17-ch94
calib_packv5_042523_0143.root, FC#13, port D2
Entries 384
Mean 43.86
Std Dev 12.15
Turn on : 25.6092
Width : 4.654
Height : 10.087
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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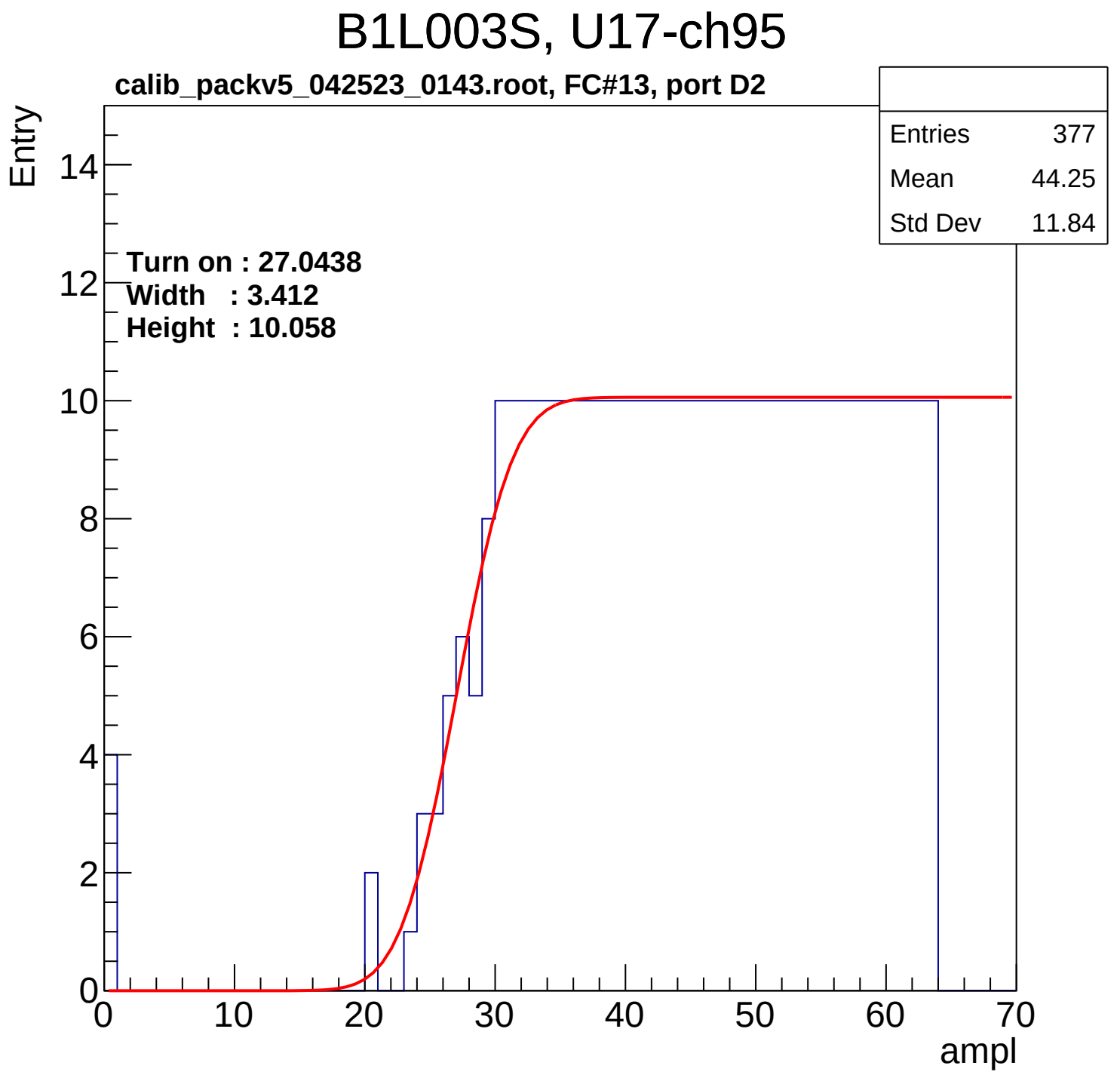
B1L003S, U17-ch95
calib_packv5_042523_0143.root, FC#13, port D2
Entries 377
Mean 44.25
Std Dev 11.84
Turn on : 27.0438
Width : 3.412
Height : 10.058
Entry
ampl
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4
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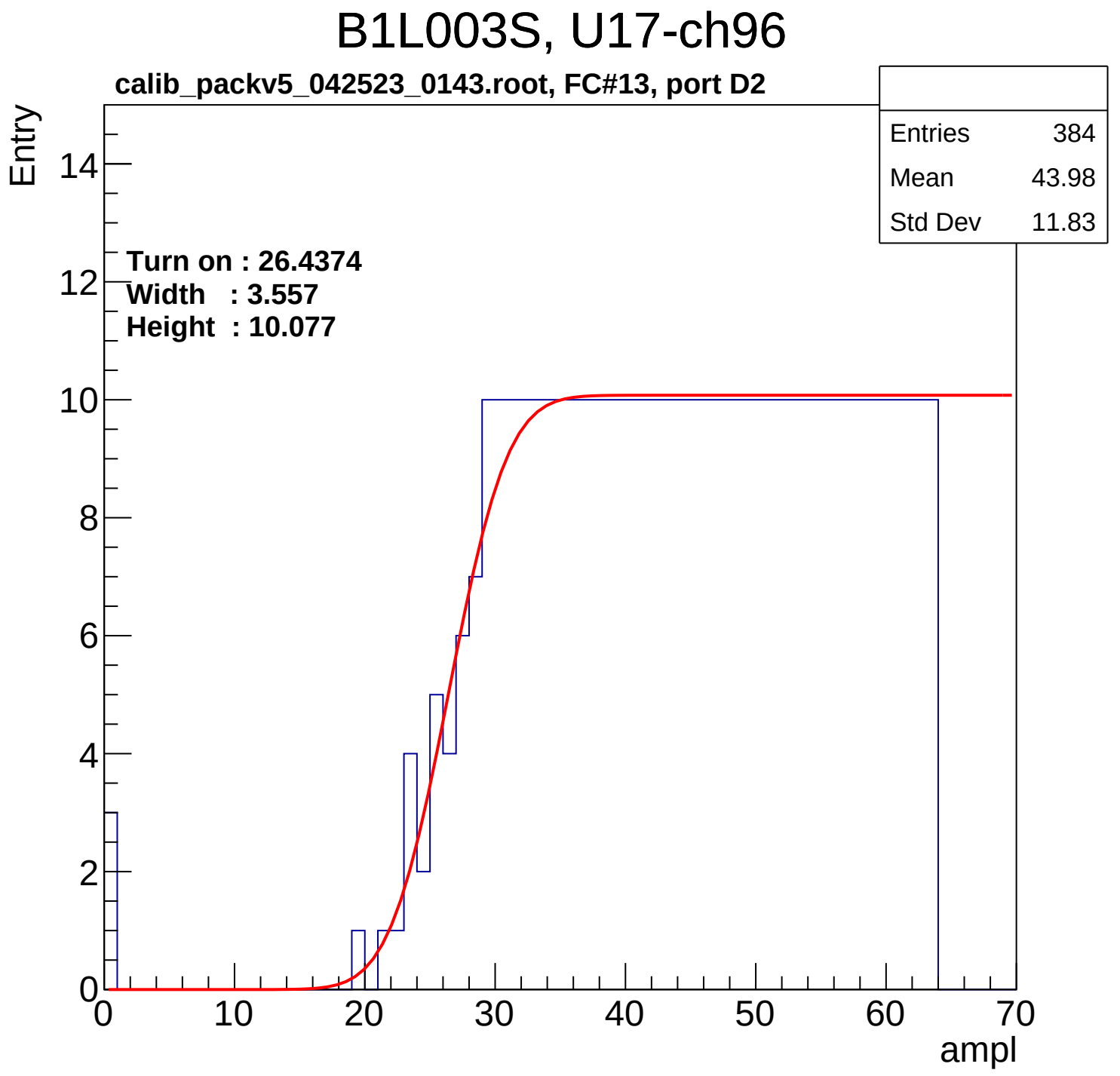
B1L003S, U17-ch96
calib_packv5_042523_0143.root, FC#13, port D2
Entries 384
Mean 43.98
Std Dev 11.83
Turn on : 26.4374
Width : 3.557
Height : 10.077
Entry
ampl
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4
6
8
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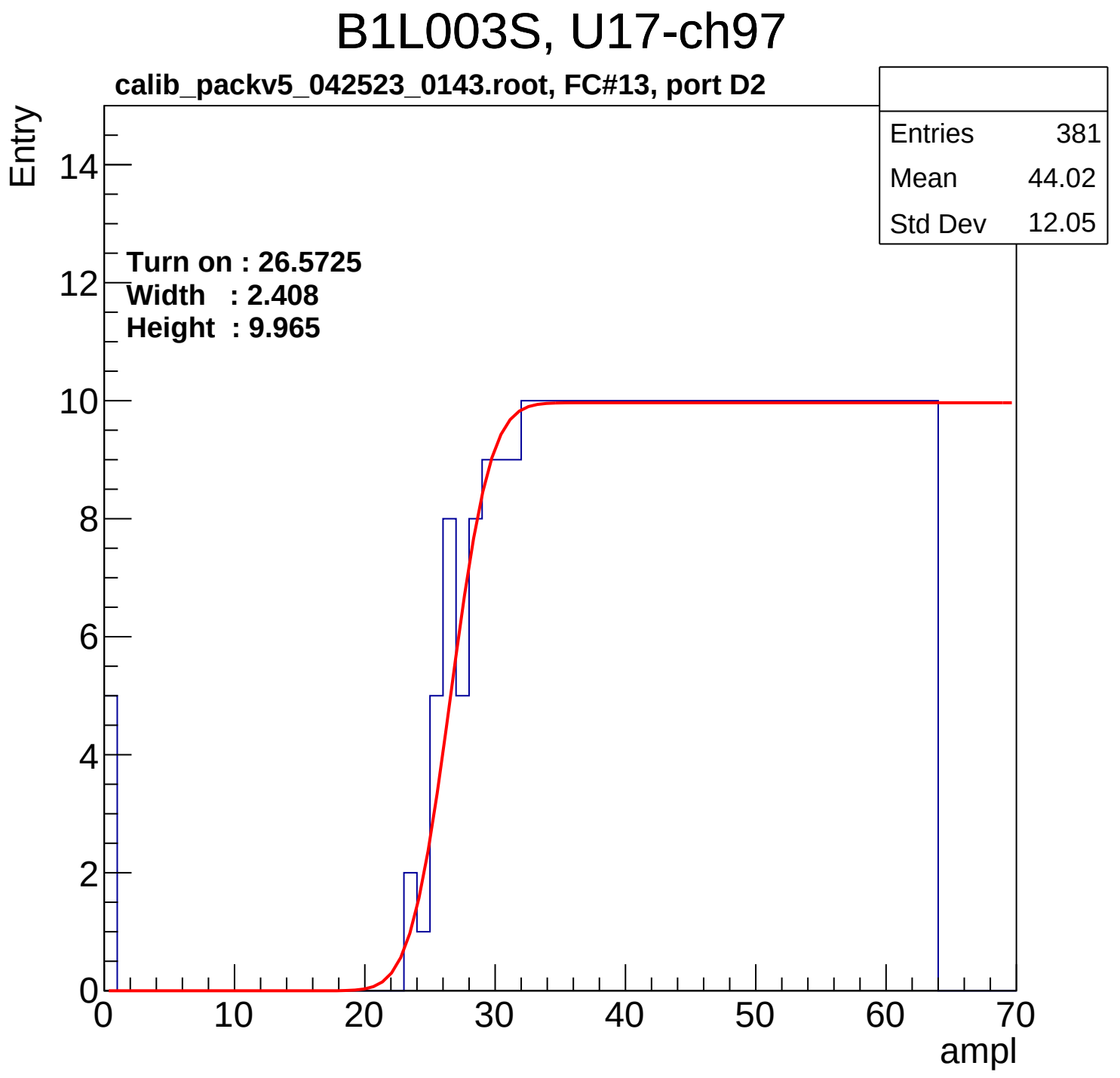
B1L003S, U17-ch97
calib_packv5_042523_0143.root, FC#13, port D2
Entries 381
Mean 44.02
Std Dev 12.05
Turn on : 26.5725
Width : 2.408
Height : 9.965
Entry
ampl
0
2
4
6
8
10
12
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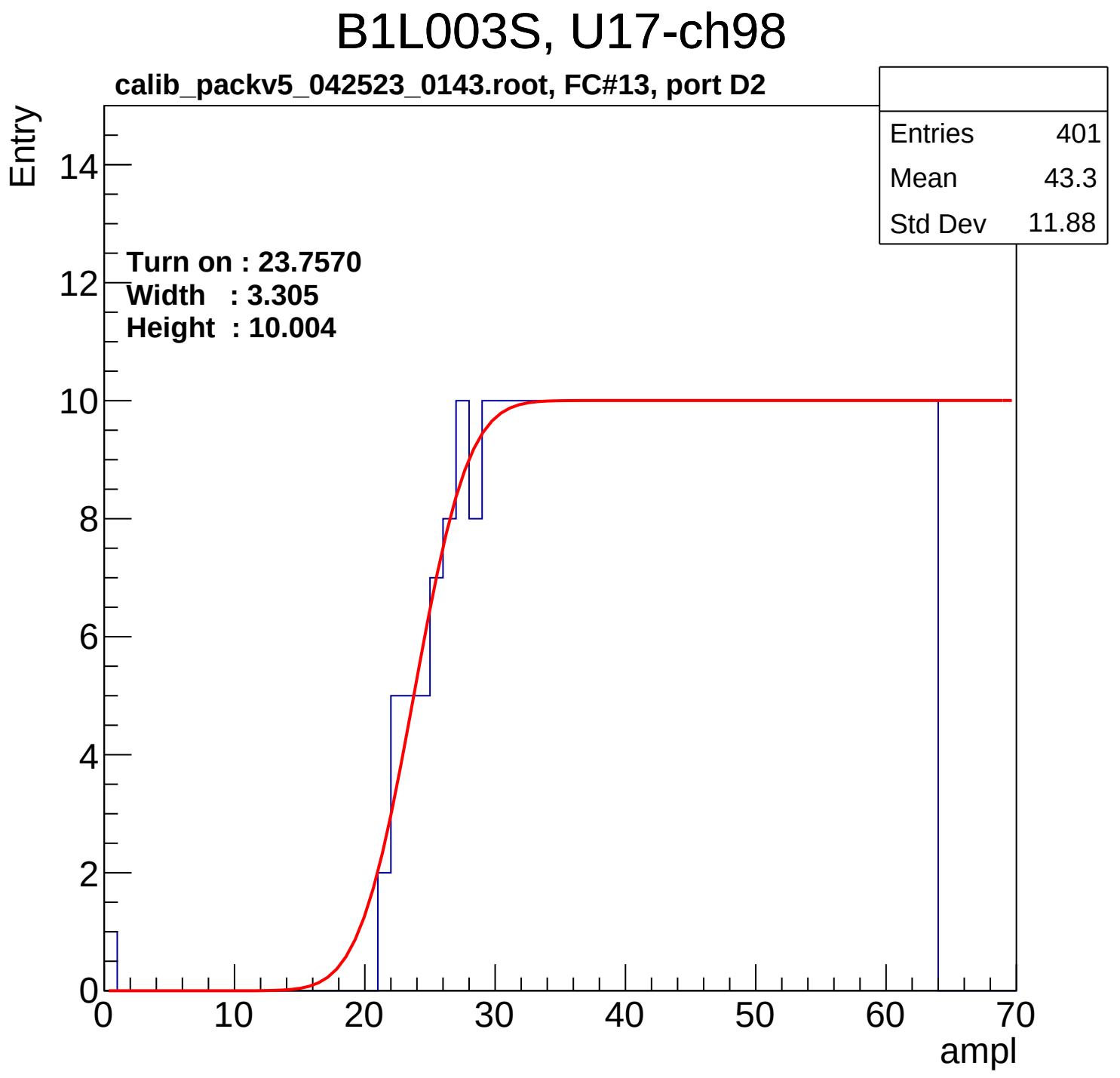
B1L003S, U17-ch98
calib_packv5_042523_0143.root, FC#13, port D2
Entries 401
Mean 43.3
Std Dev 11.88
Turn on : 23.7570
Width : 3.305
Height : 10.004
Entry
ampl
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2
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6
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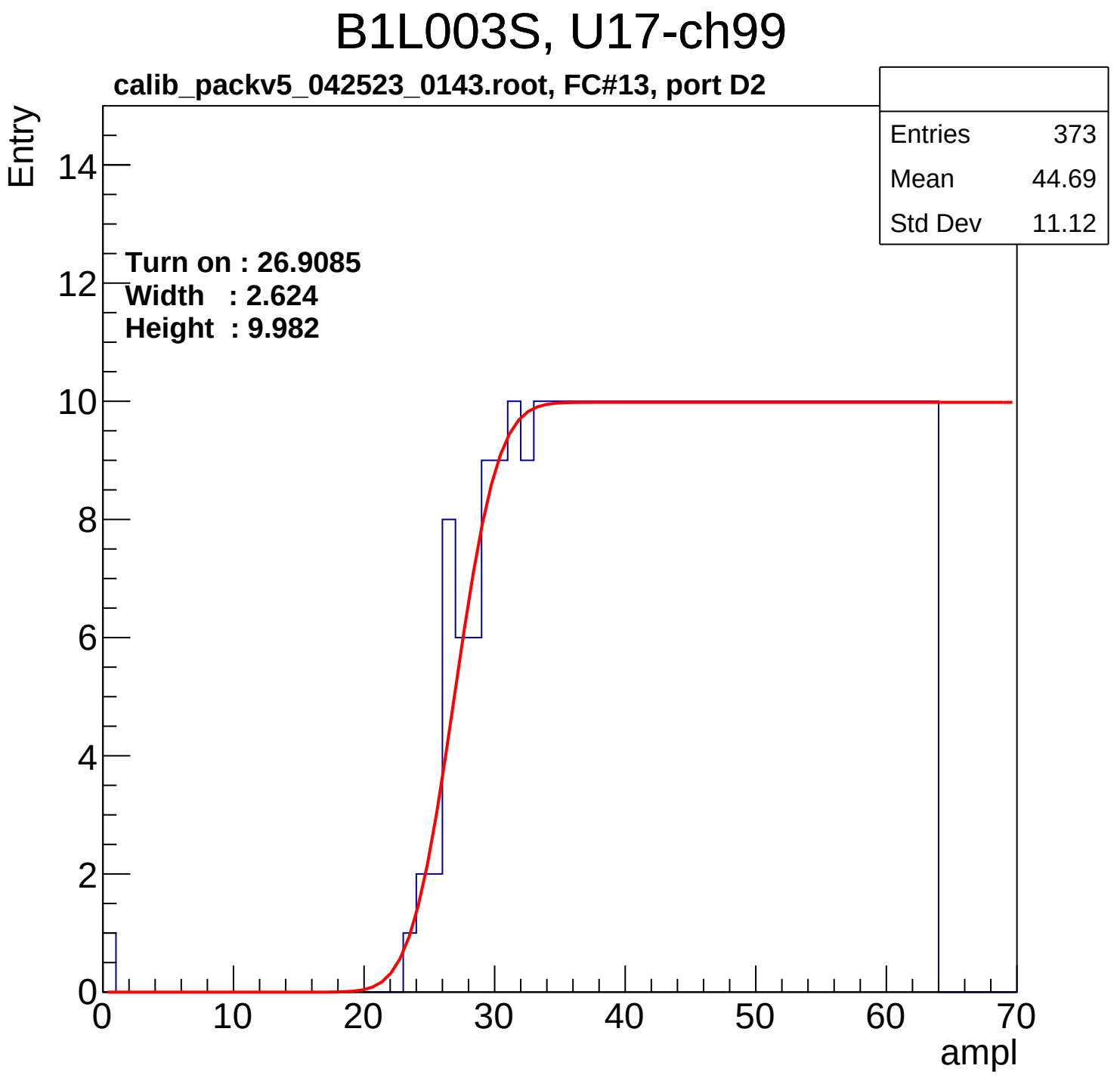
B1L003S, U17-ch99
calib_packv5_042523_0143.root, FC#13, port D2
Entries 373
Mean 44.69
Std Dev 11.12
Turn on : 26.9085
Width : 2.624
Height : 9.982
Entry
ampl
0
2
4
6
8
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0
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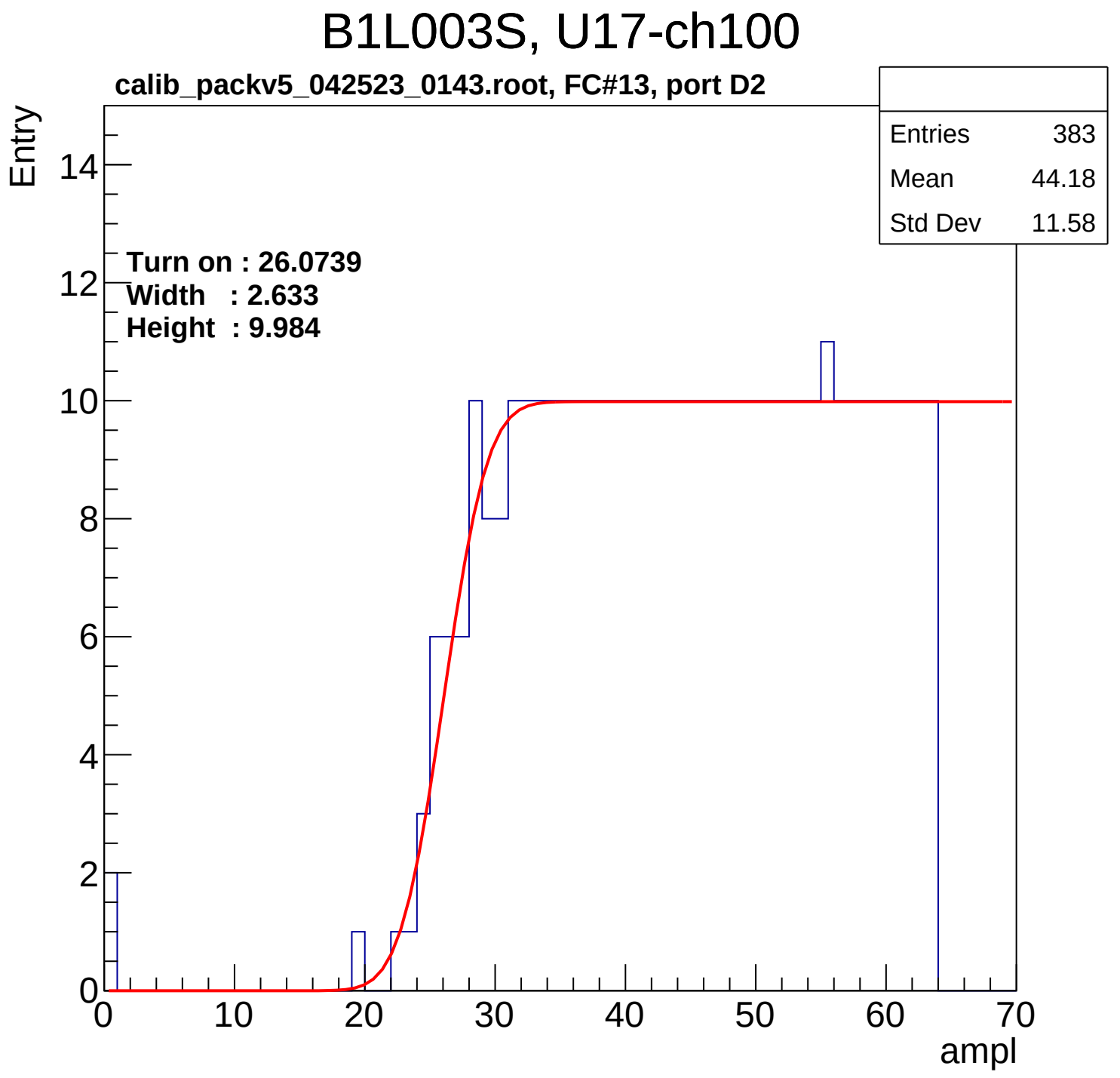
B1L003S, U17-ch100
calib_packv5_042523_0143.root, FC#13, port D2
Entries 383
Mean 44.18
Std Dev 11.58
Turn on : 26.0739
Width : 2.633
Height : 9.984
Entry
ampl
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6
8
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0
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60
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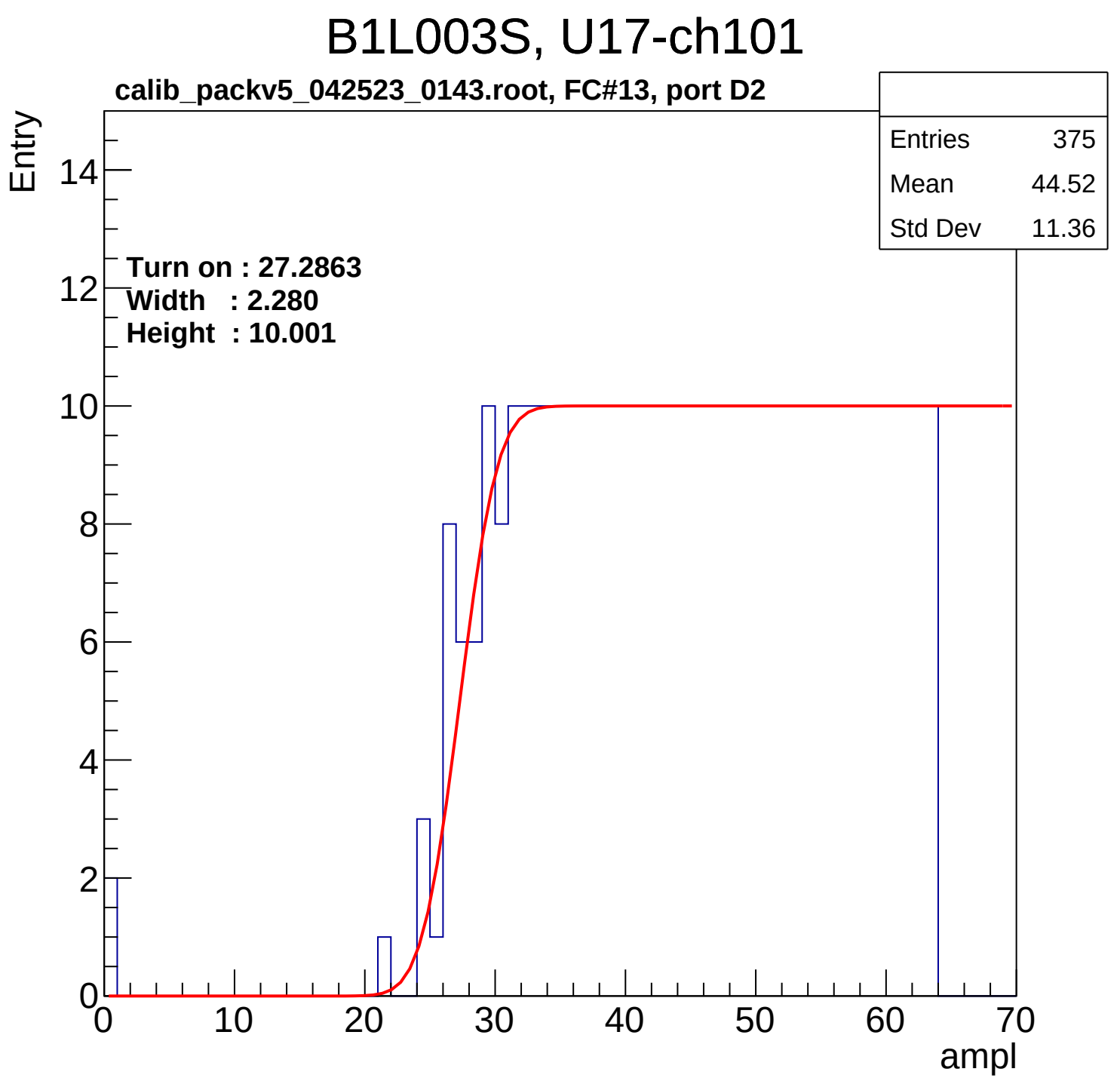
B1L003S, U17-ch101
calib_packv5_042523_0143.root, FC#13, port D2
Entries 375
Mean 44.52
Std Dev 11.36
Turn on : 27.2863
Width : 2.280
Height : 10.001
Entry
ampl
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6
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0
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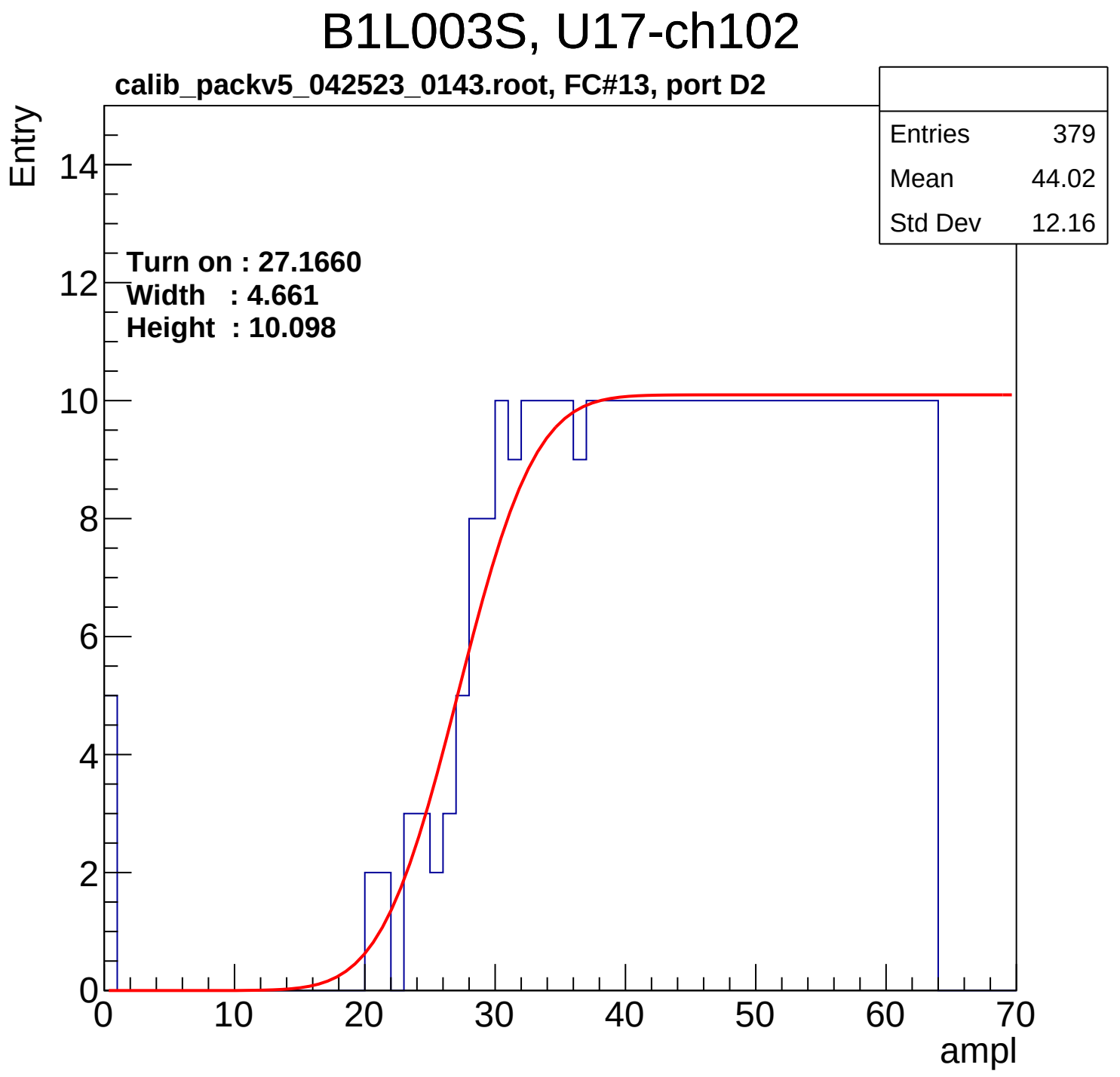
B1L003S, U17-ch102
calib_packv5_042523_0143.root, FC#13, port D2
Entries 379
Mean 44.02
Std Dev 12.16
Turn on : 27.1660
Width : 4.661
Height : 10.098
Entry
ampl
0
2
4
6
8
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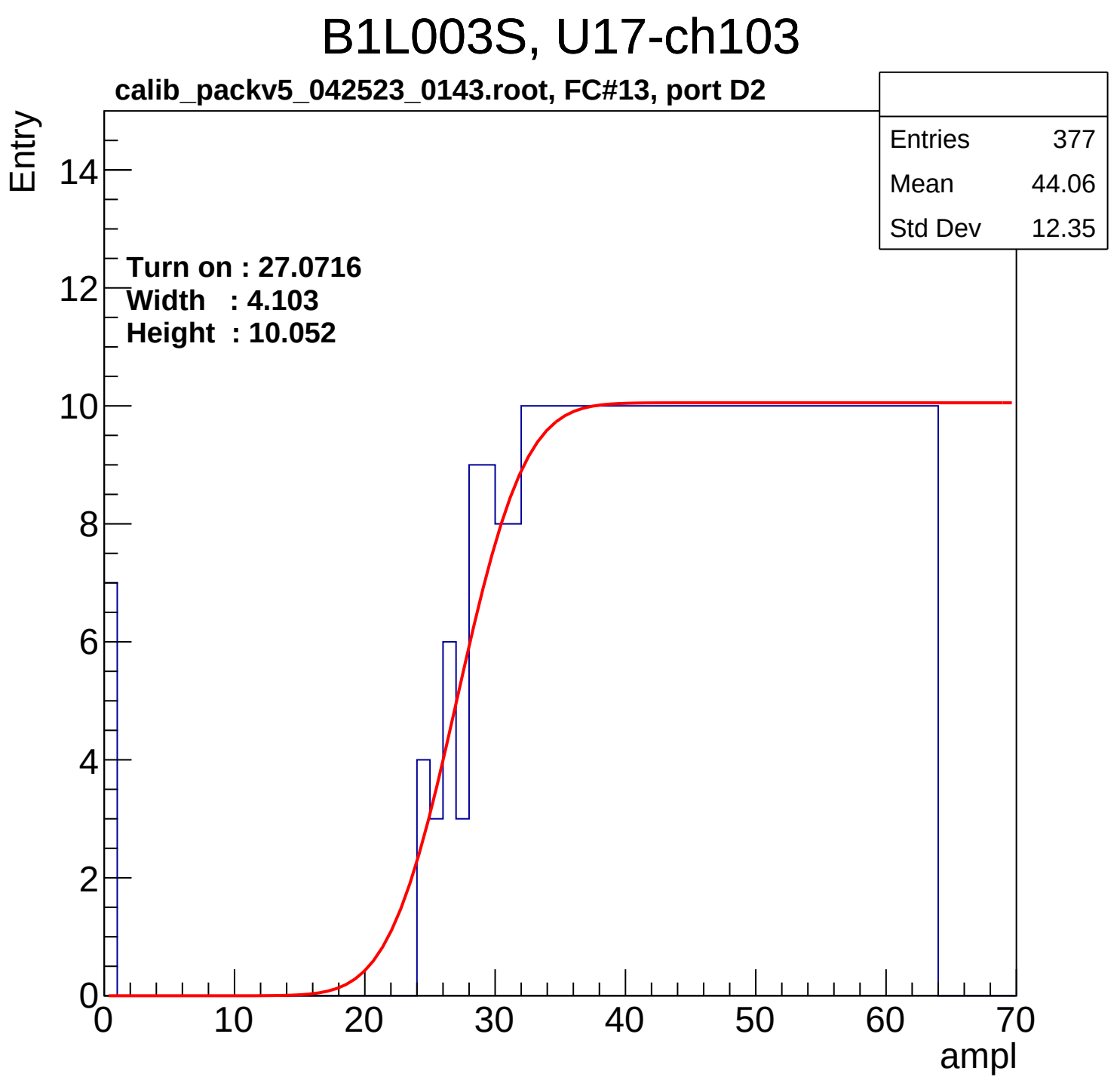
B1L003S, U17-ch103
calib_packv5_042523_0143.root, FC#13, port D2
Entries 377
Mean 44.06
Std Dev 12.35
Turn on : 27.0716
Width : 4.103
Height : 10.052
Entry
ampl
0
2
4
6
8
10
12
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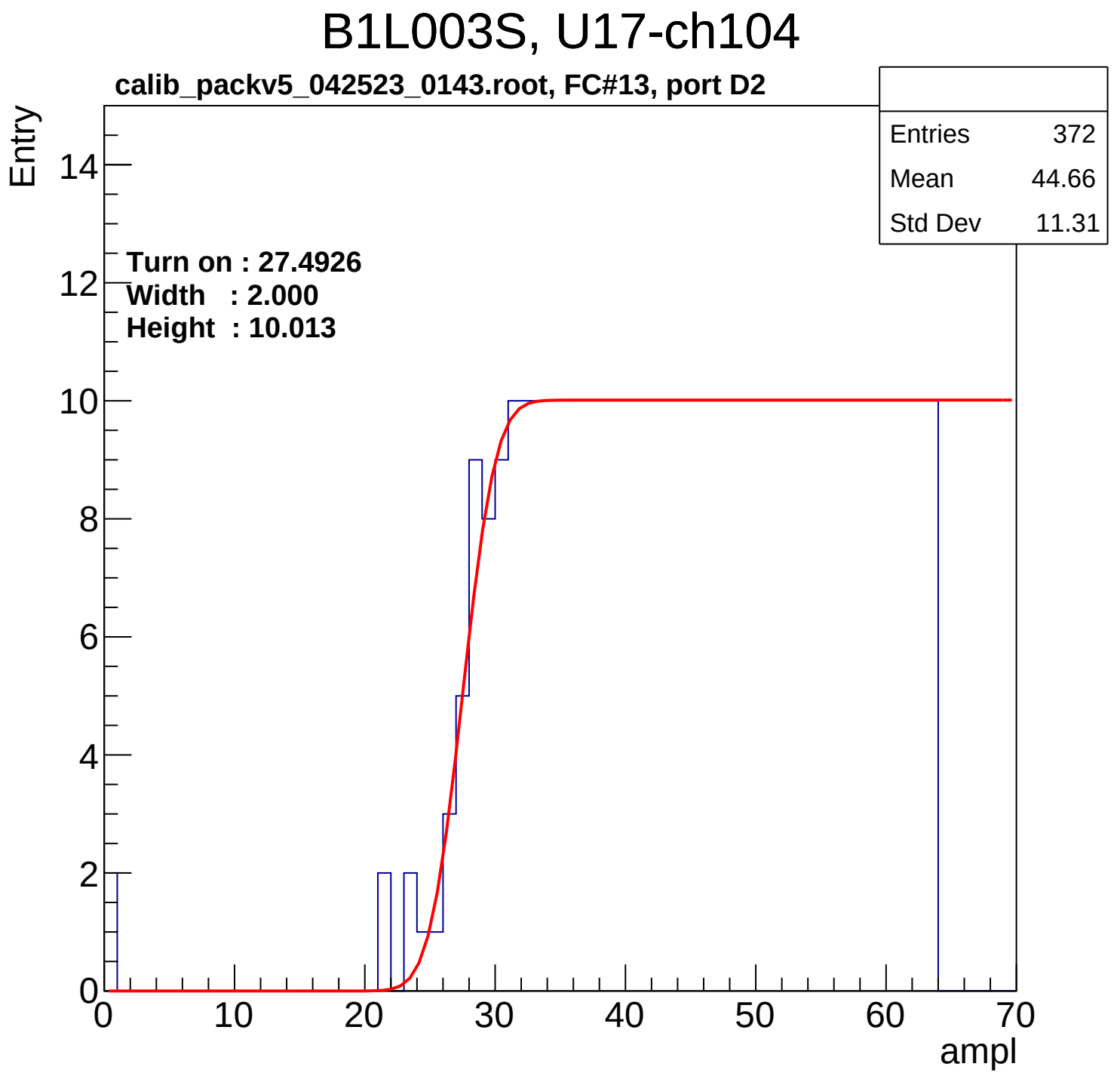
B1L003S, U17-ch104
calib_packv5_042523_0143.root, FC#13, port D2
Entries 372
Mean 44.66
Std Dev 11.31
Turn on : 27.4926
Width : 2.000
Height : 10.013
Entry
ampl
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2
4
6
8
10
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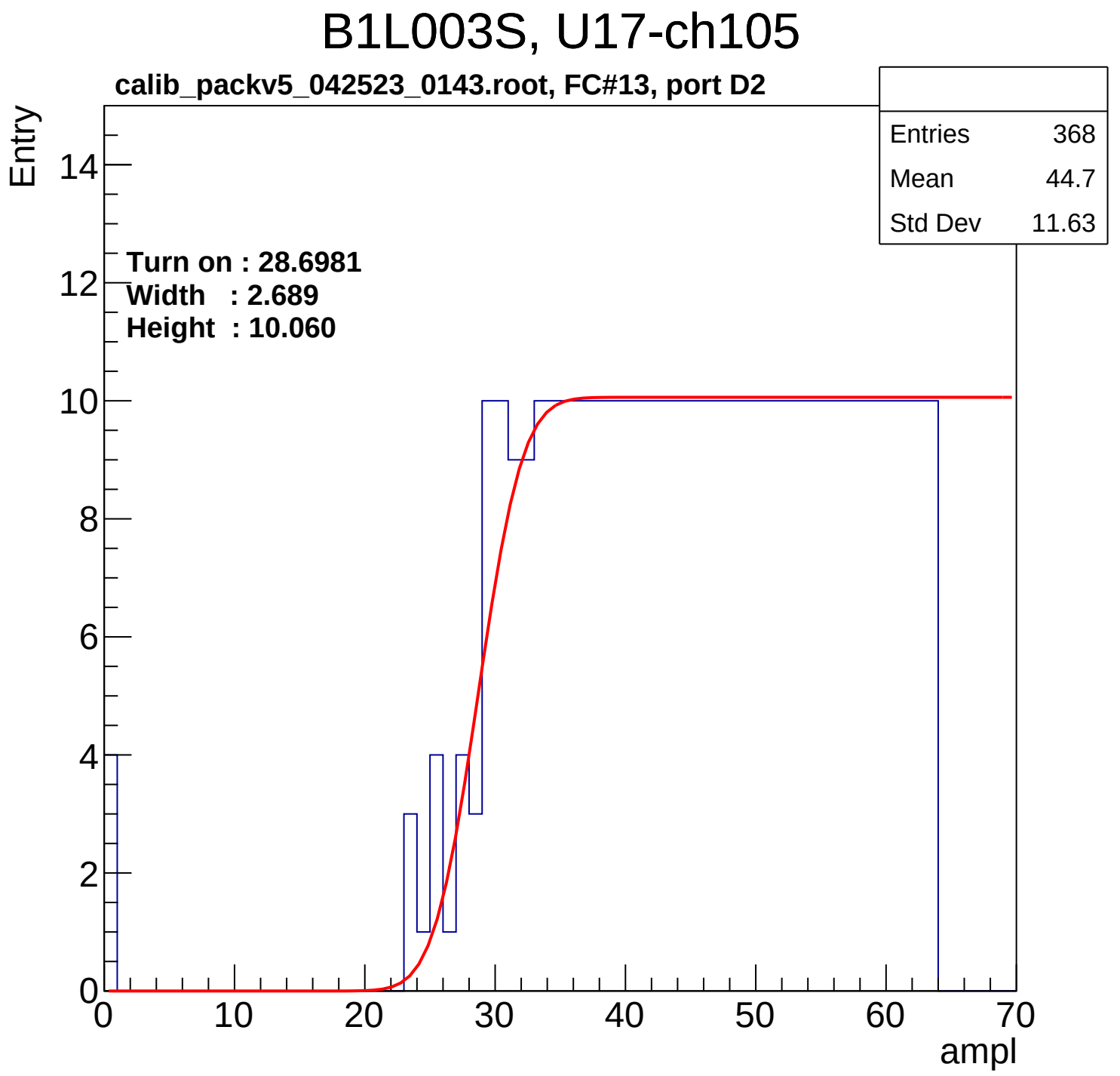
B1L003S, U17-ch105
calib_packv5_042523_0143.root, FC#13, port D2
Entries 368
Mean 44.7
Std Dev 11.63
Turn on : 28.6981
Width : 2.689
Height : 10.060
Entry
ampl
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2
4
6
8
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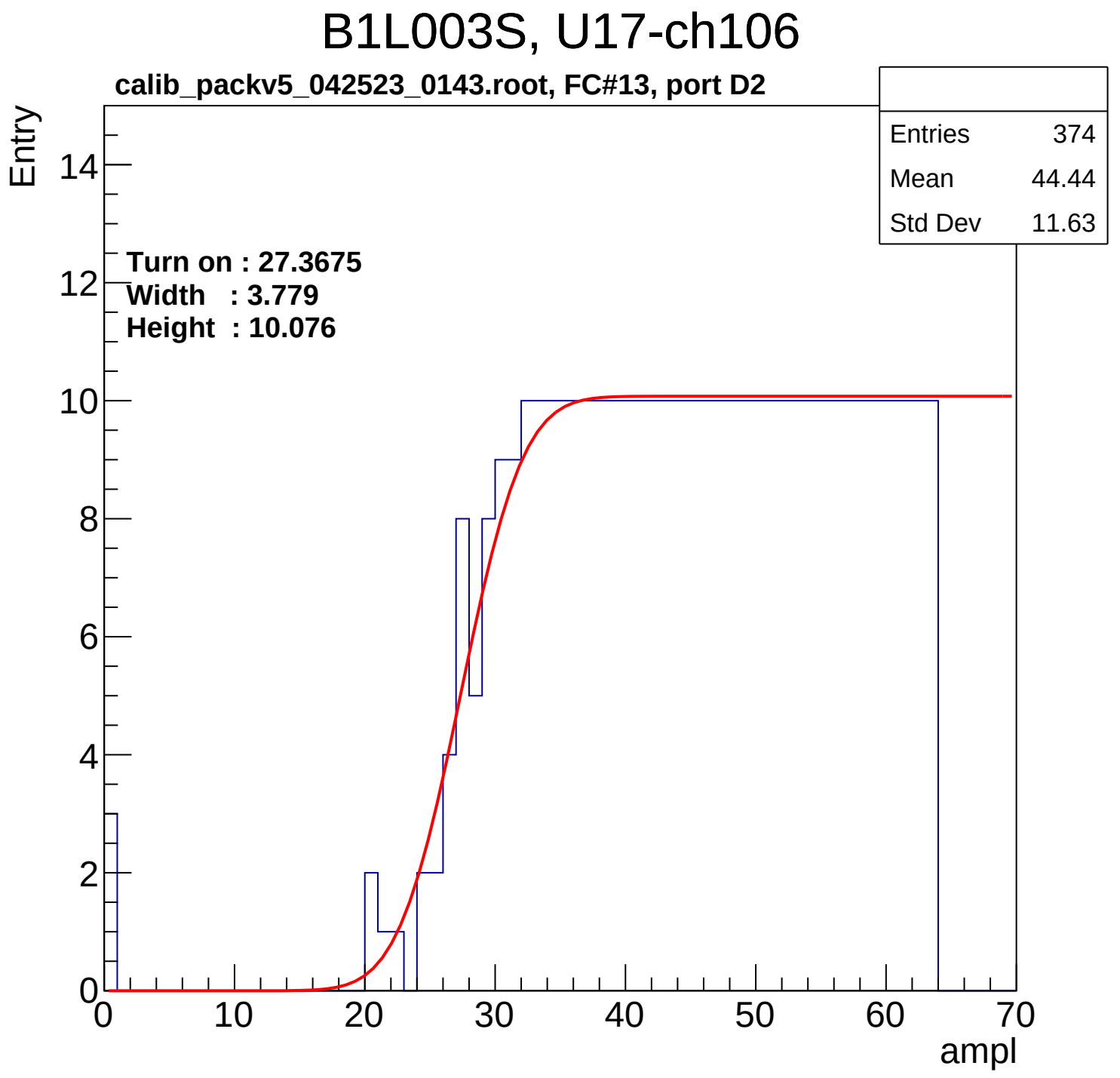
B1L003S, U17-ch106
calib_packv5_042523_0143.root, FC#13, port D2
Entries 374
Mean 44.44
Std Dev 11.63
Turn on : 27.3675
Width : 3.779
Height : 10.076
Entry
ampl
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2
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6
8
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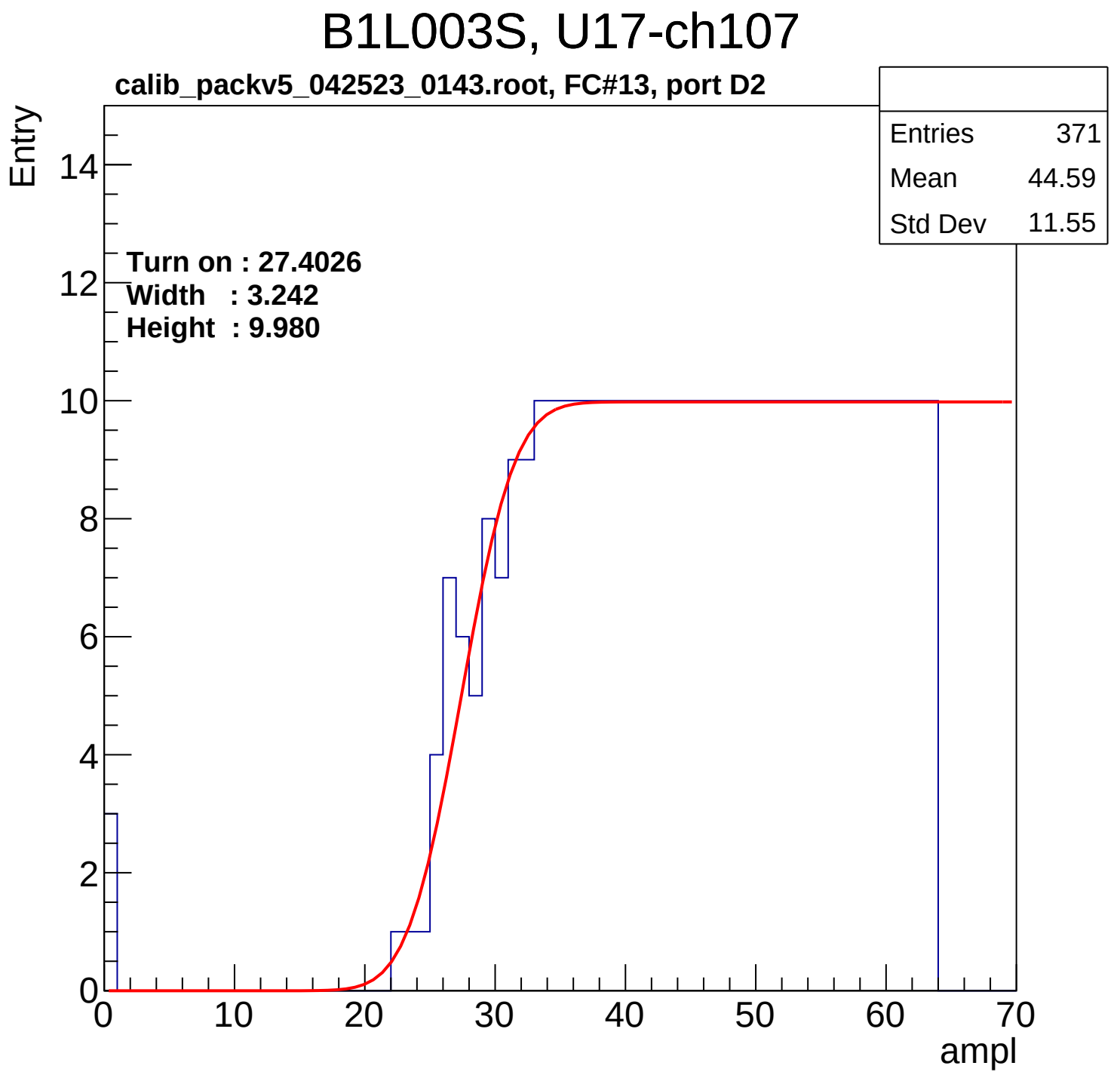
B1L003S, U17-ch107
calib_packv5_042523_0143.root, FC#13, port D2
Entries 371
Mean 44.59
Std Dev 11.55
Turn on : 27.4026
Width : 3.242
Height : 9.980
Entry
ampl
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2
4
6
8
10
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0
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60
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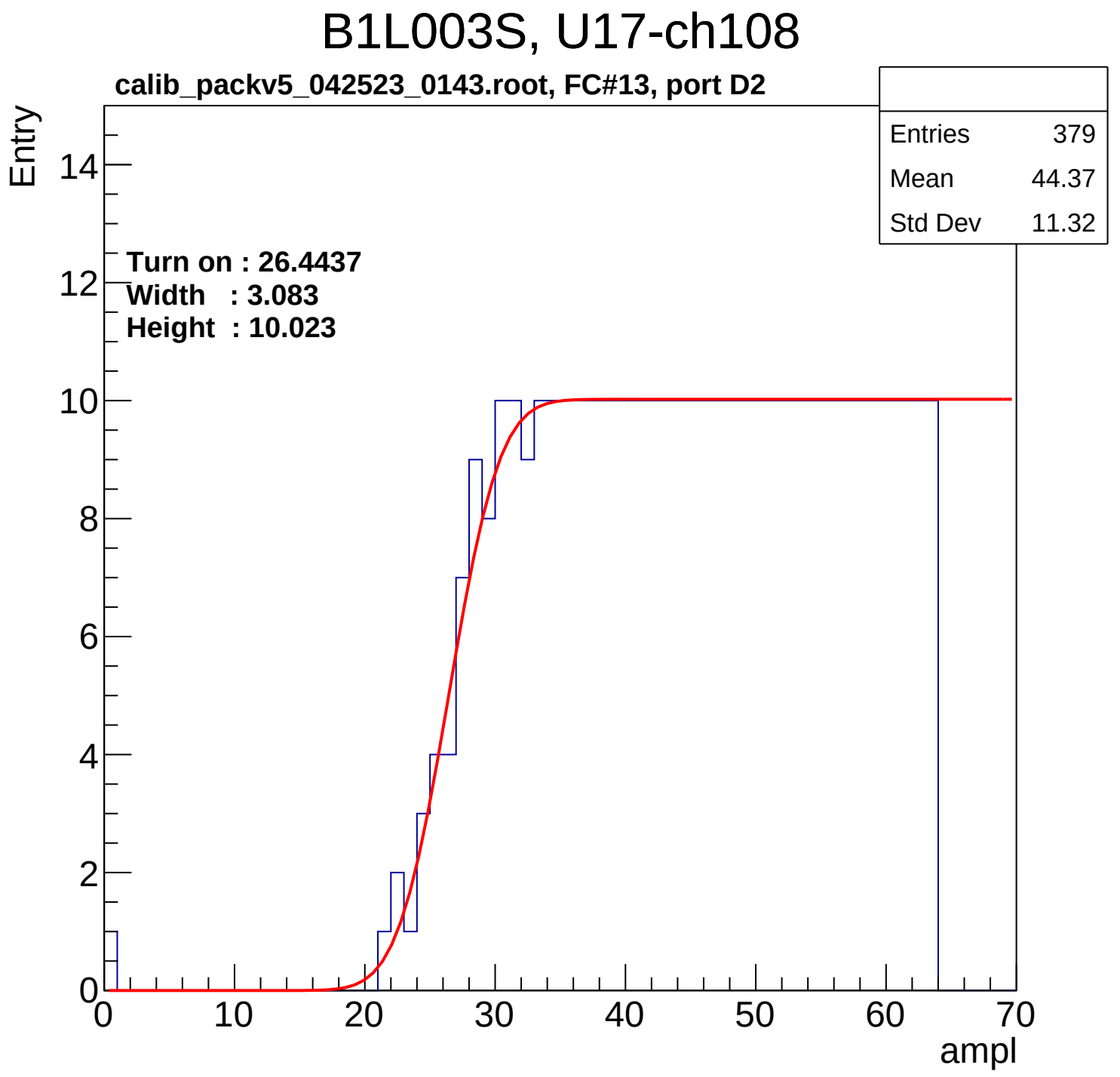
B1L003S, U17-ch108
calib_packv5_042523_0143.root, FC#13, port D2
Entries 379
Mean 44.37
Std Dev 11.32
Turn on : 26.4437
Width : 3.083
Height : 10.023
Entry
ampl
0
2
4
6
8
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0
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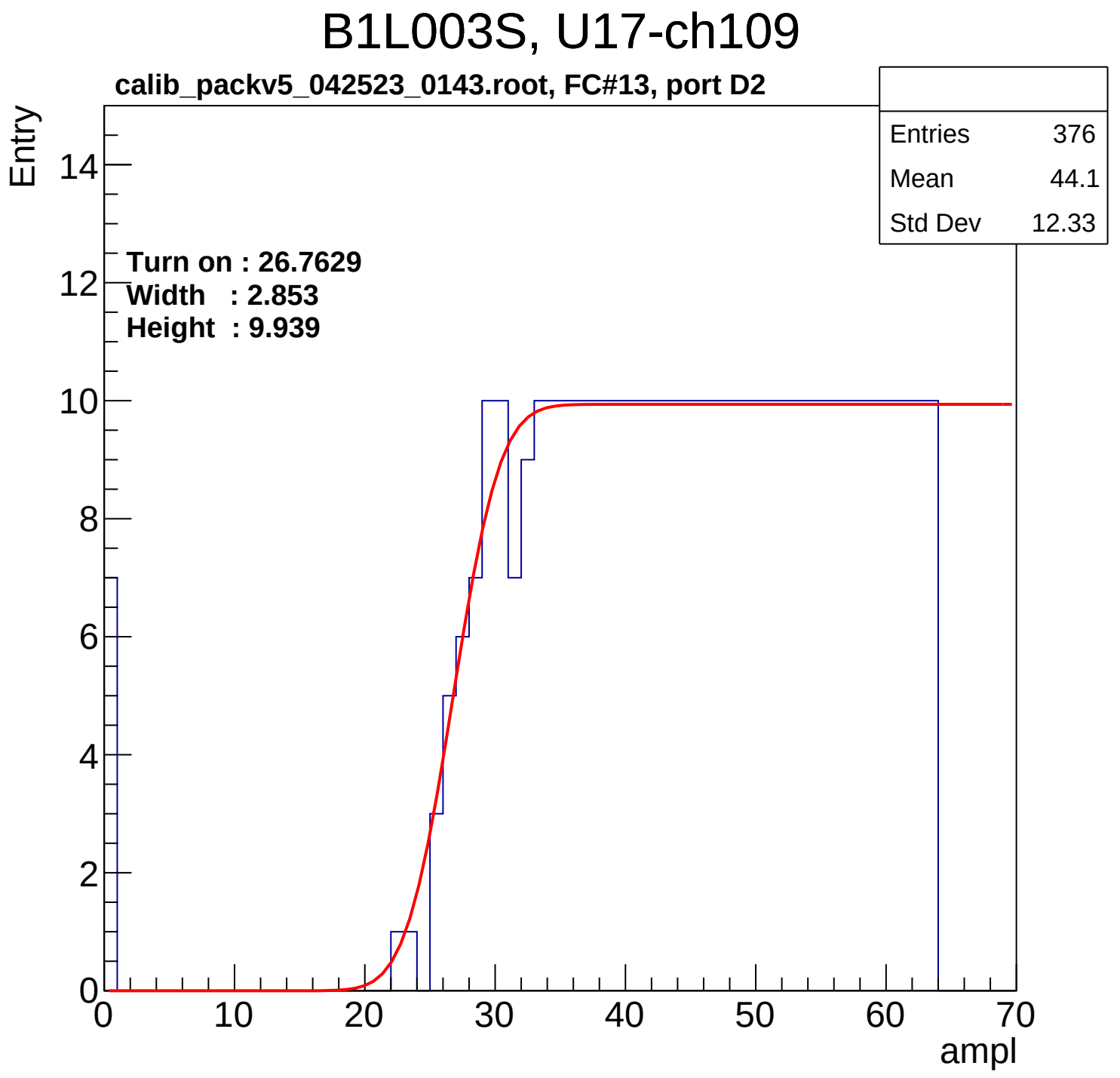
B1L003S, U17-ch109
calib_packv5_042523_0143.root, FC#13, port D2
Entries 376
Mean 44.1
Std Dev 12.33
Turn on : 26.7629
Width : 2.853
Height : 9.939
Entry
ampl
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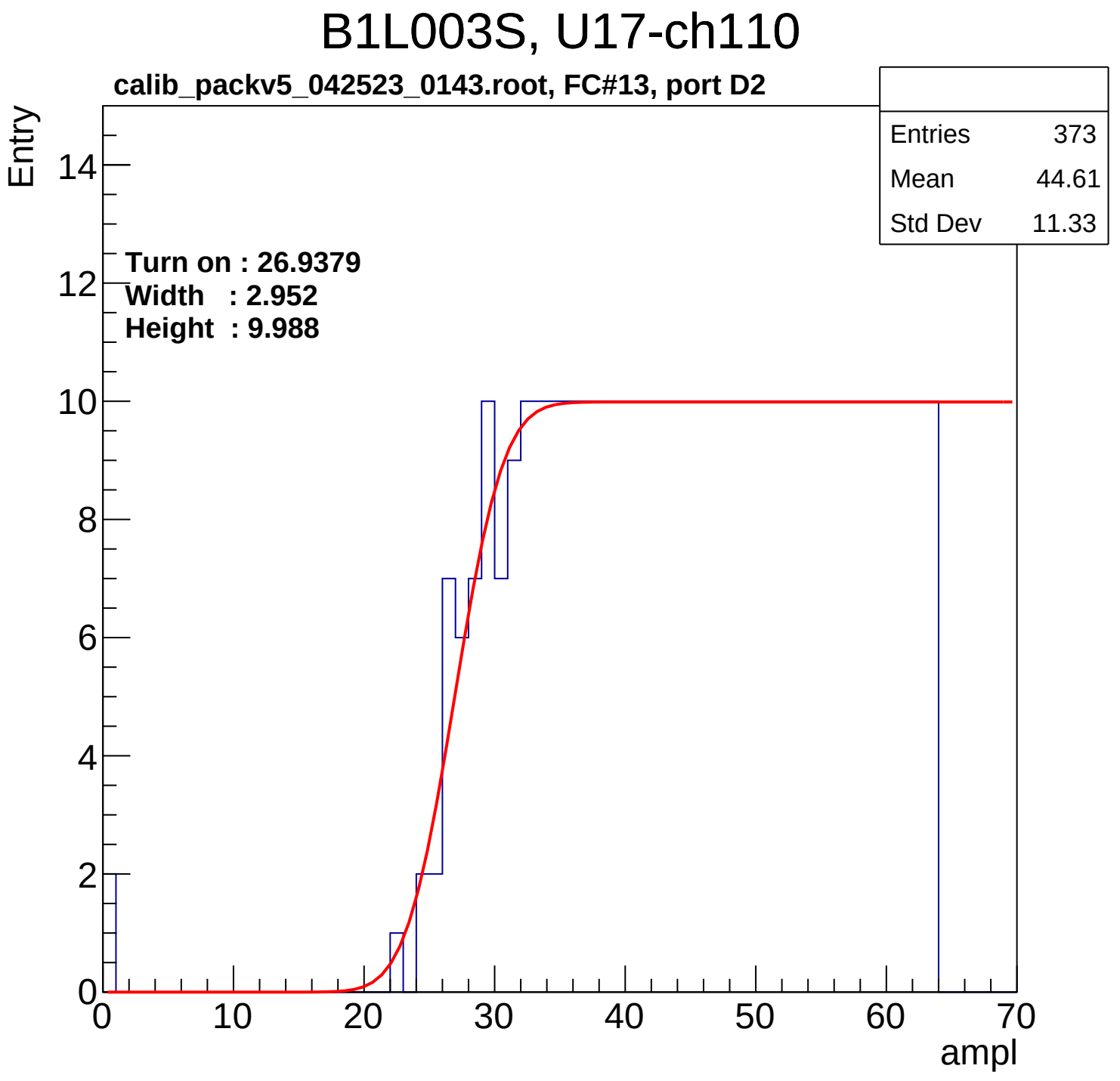
B1L003S, U17-ch110
calib_packv5_042523_0143.root, FC#13, port D2
Entries 373
Mean 44.61
Std Dev 11.33
Turn on : 26.9379
Width : 2.952
Height : 9.988
Entry
ampl
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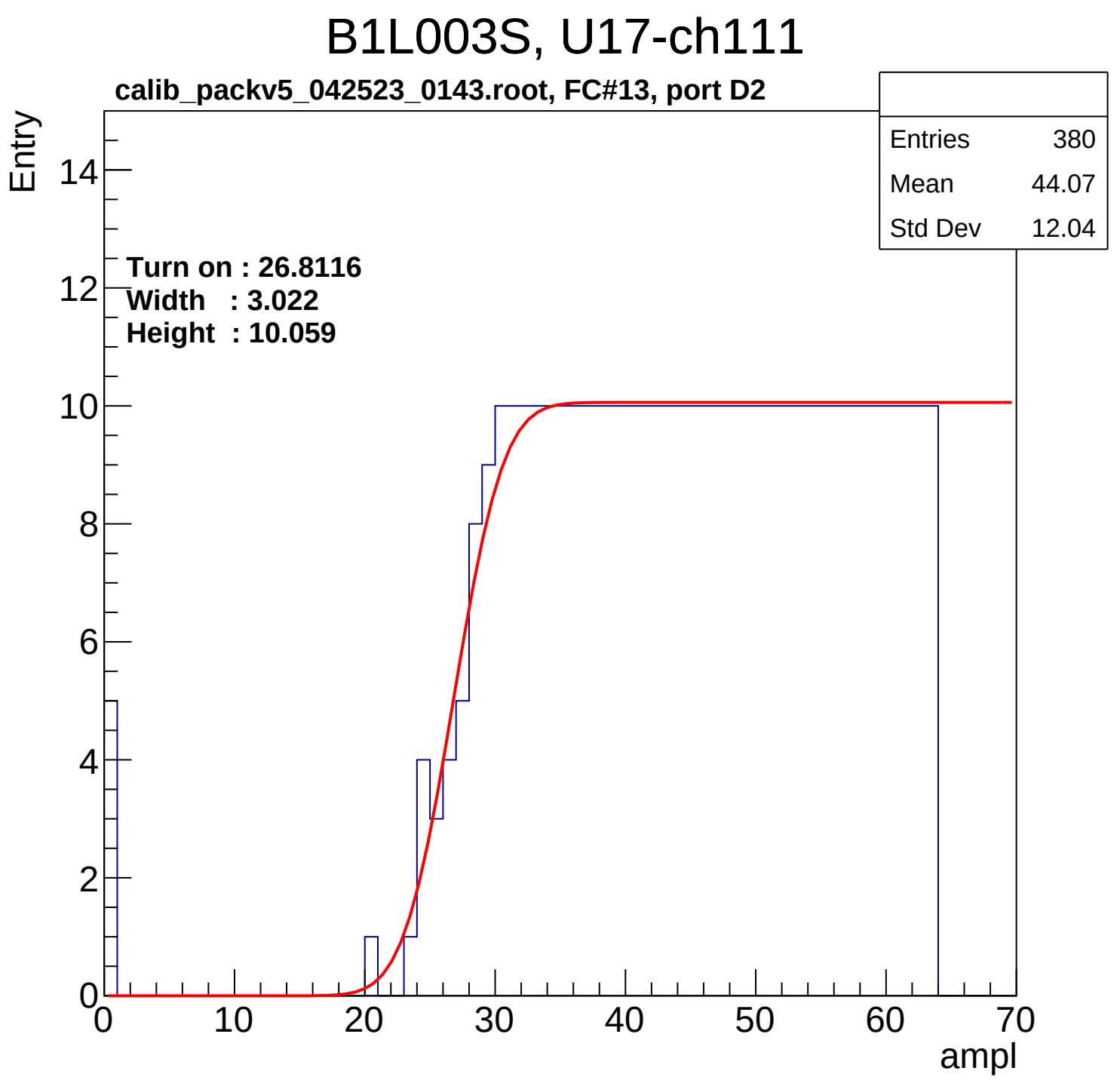
B1L003S, U17-ch111
calib_packv5_042523_0143.root, FC#13, port D2
Entries 380
Mean 44.07
Std Dev 12.04
Turn on : 26.8116
Width : 3.022
Height : 10.059
Entry
ampl
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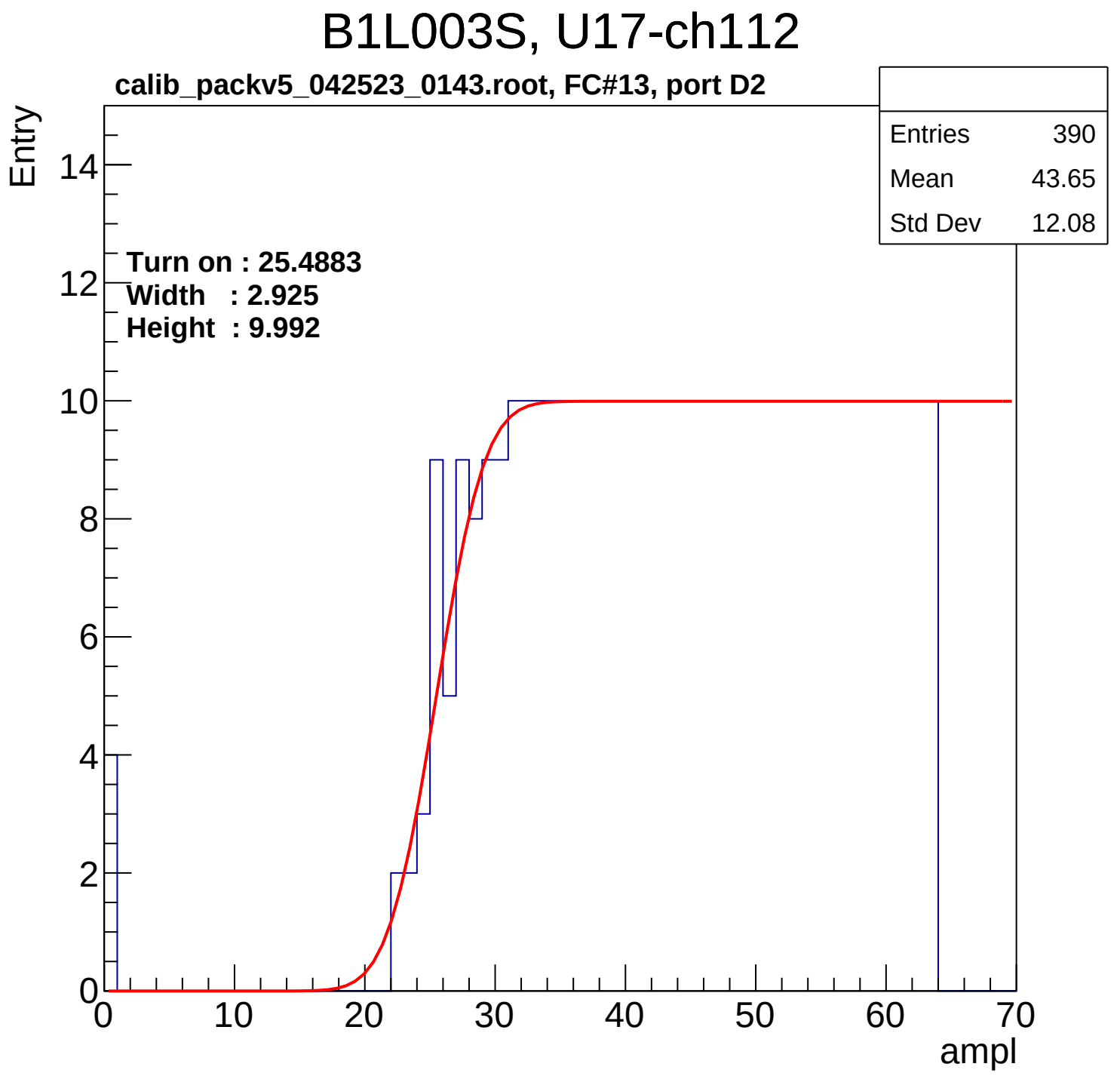
B1L003S, U17-ch112
calib_packv5_042523_0143.root, FC#13, port D2
Entries 390
Mean 43.65
Std Dev 12.08
Turn on : 25.4883
Width : 2.925
Height : 9.992
Entry
ampl
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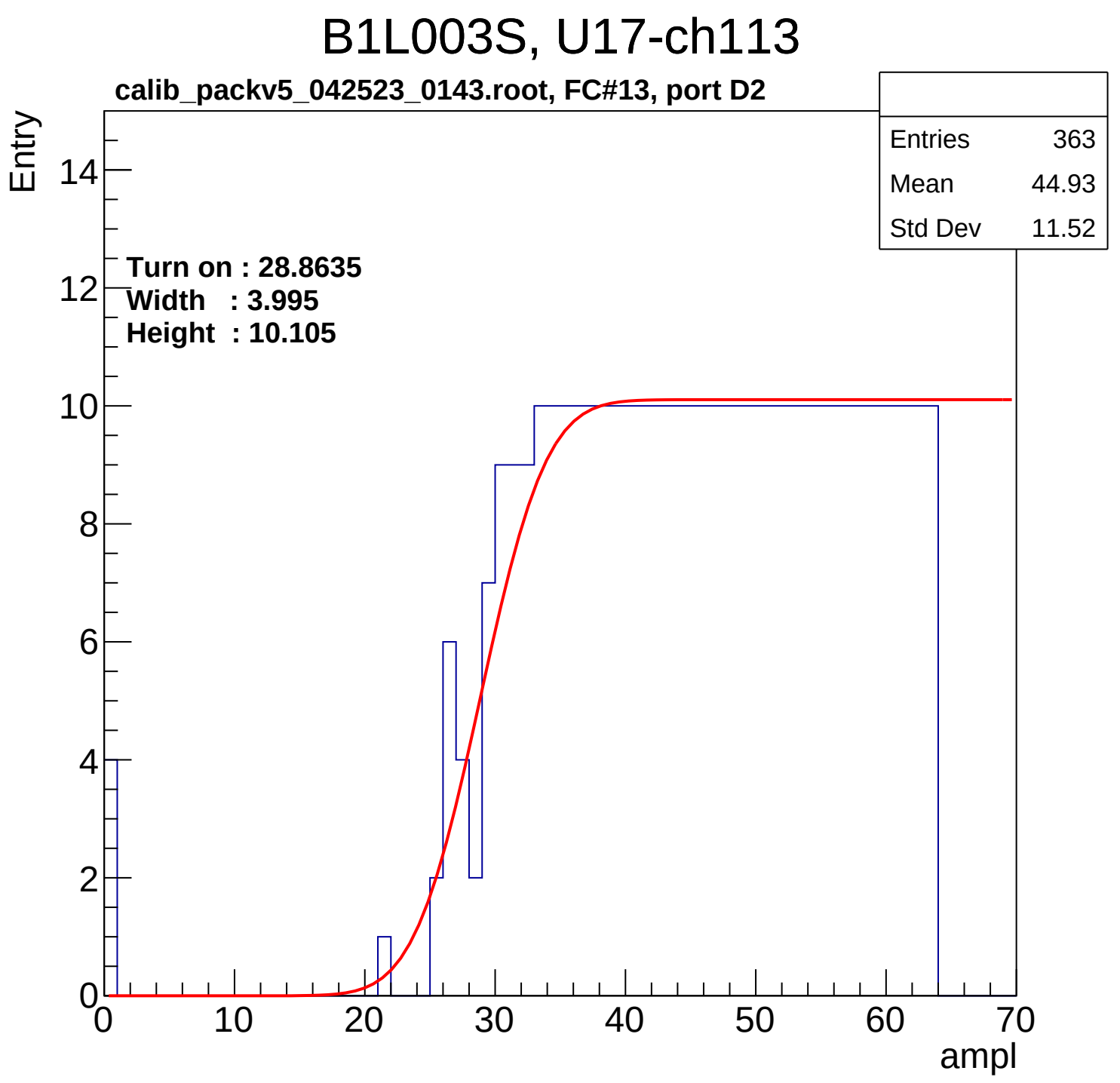
B1L003S, U17-ch113
calib_packv5_042523_0143.root, FC#13, port D2
Entries 363
Mean 44.93
Std Dev 11.52
Turn on : 28.8635
Width : 3.995
Height : 10.105
Entry
ampl
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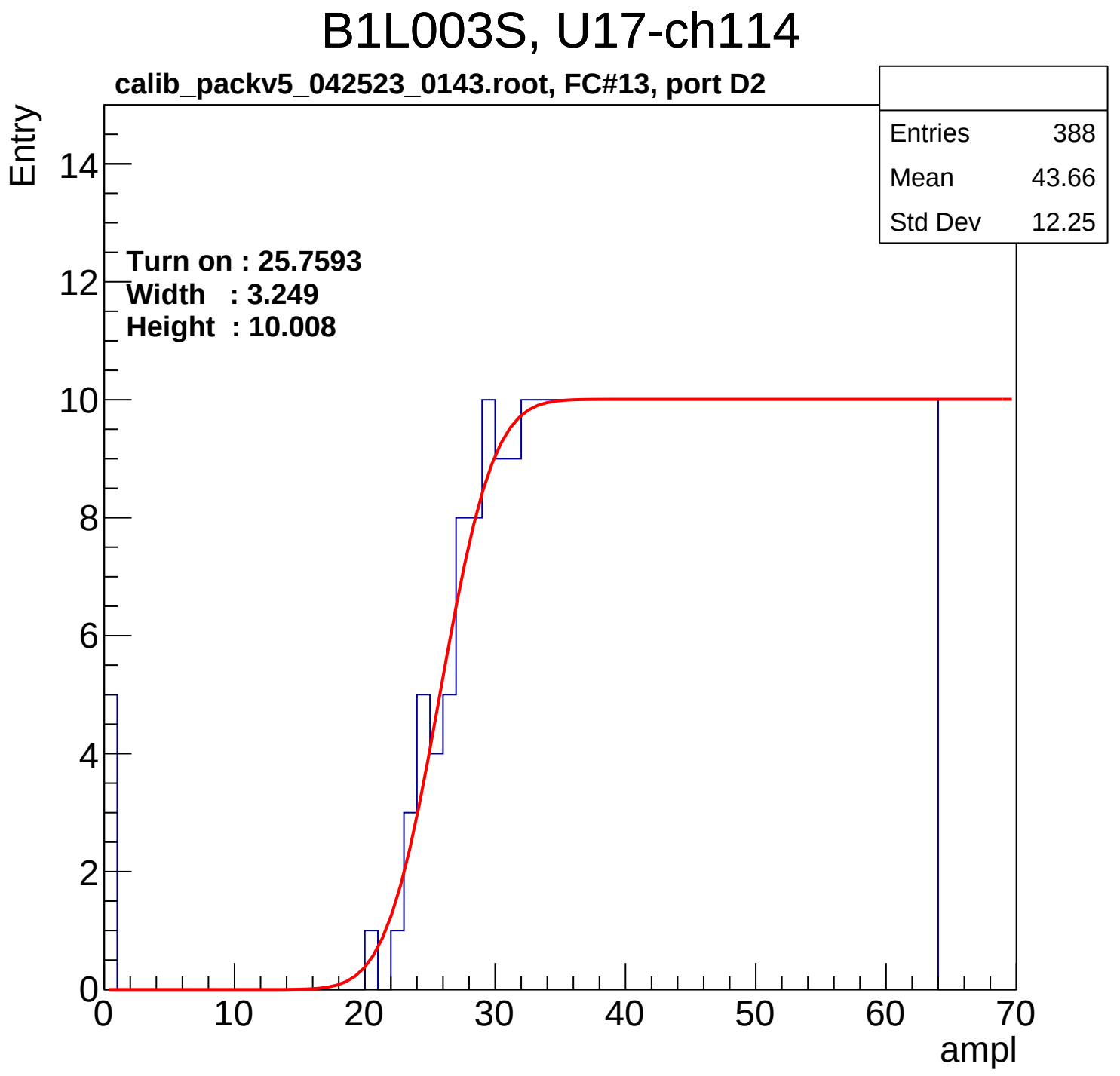
B1L003S, U17-ch114
calib_packv5_042523_0143.root, FC#13, port D2
Entries 388
Mean 43.66
Std Dev 12.25
Turn on : 25.7593
Width : 3.249
Height : 10.008
Entry
ampl
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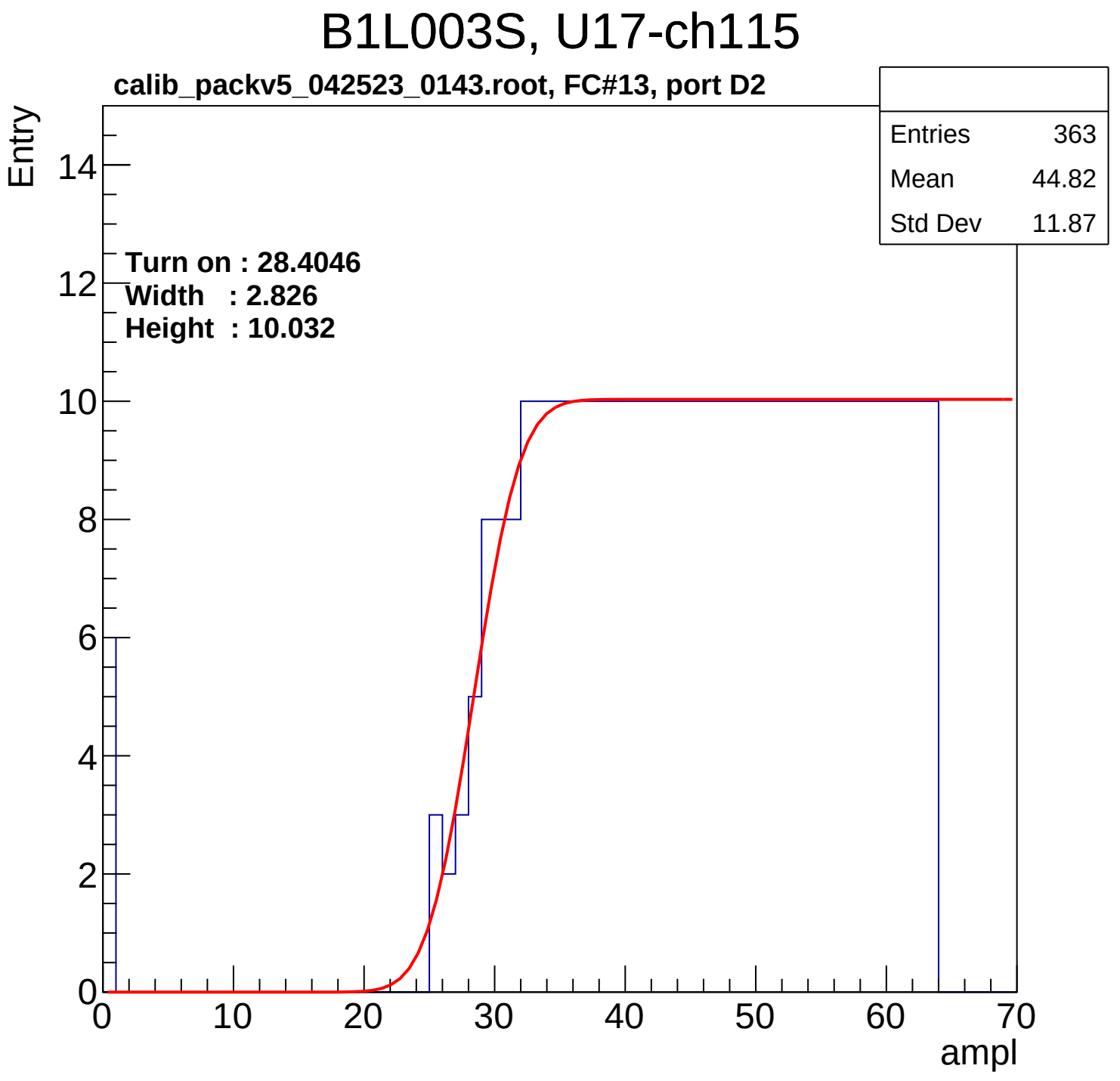
B1L003S, U17-ch115
calib_packv5_042523_0143.root, FC#13, port D2
Entries 363
Mean 44.82
Std Dev 11.87
Turn on : 28.4046
Width : 2.826
Height : 10.032
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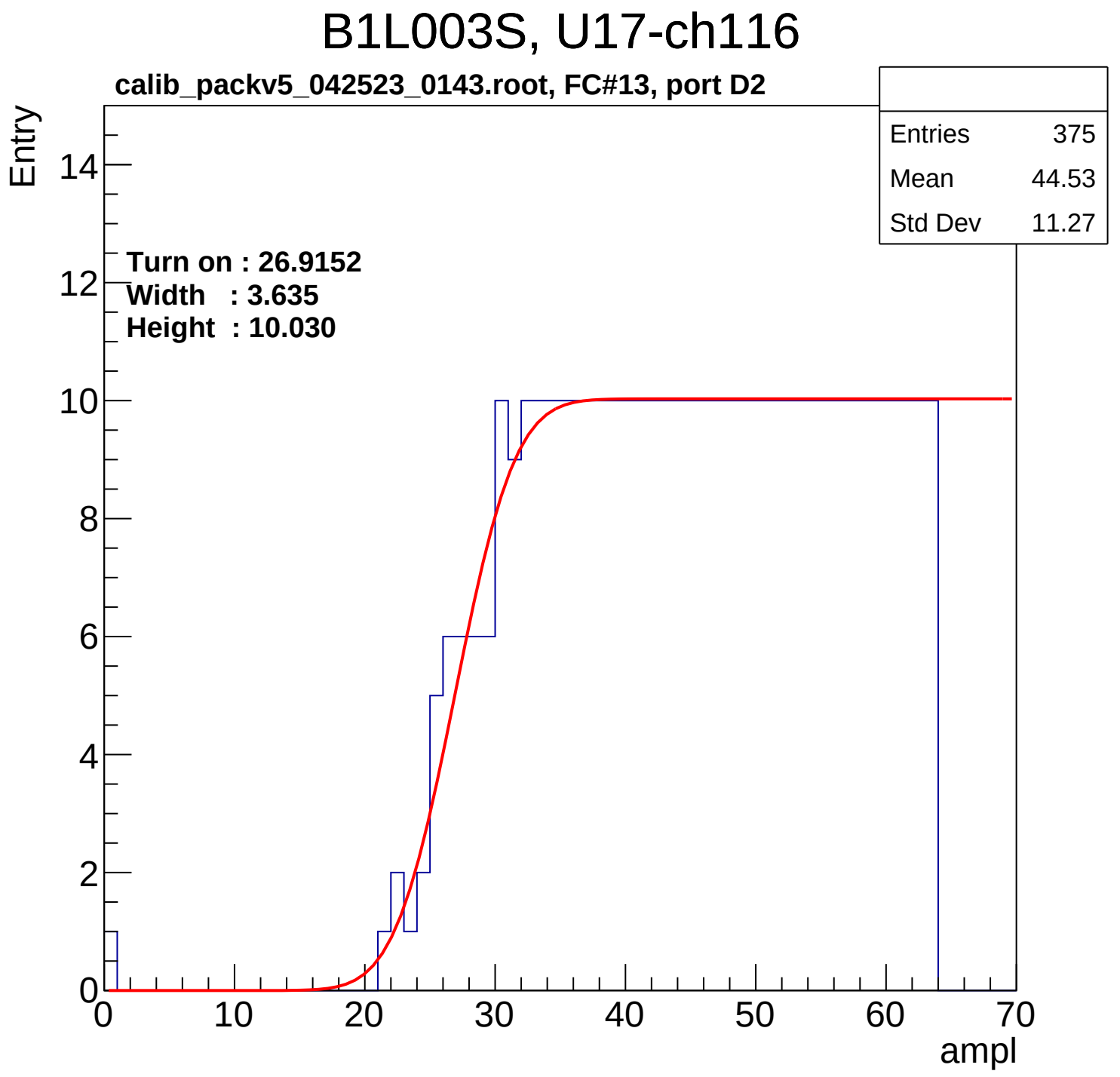
B1L003S, U17-ch116
calib_packv5_042523_0143.root, FC#13, port D2
Entries 375
Mean 44.53
Std Dev 11.27
Turn on : 26.9152
Width : 3.635
Height : 10.030
Entry
ampl
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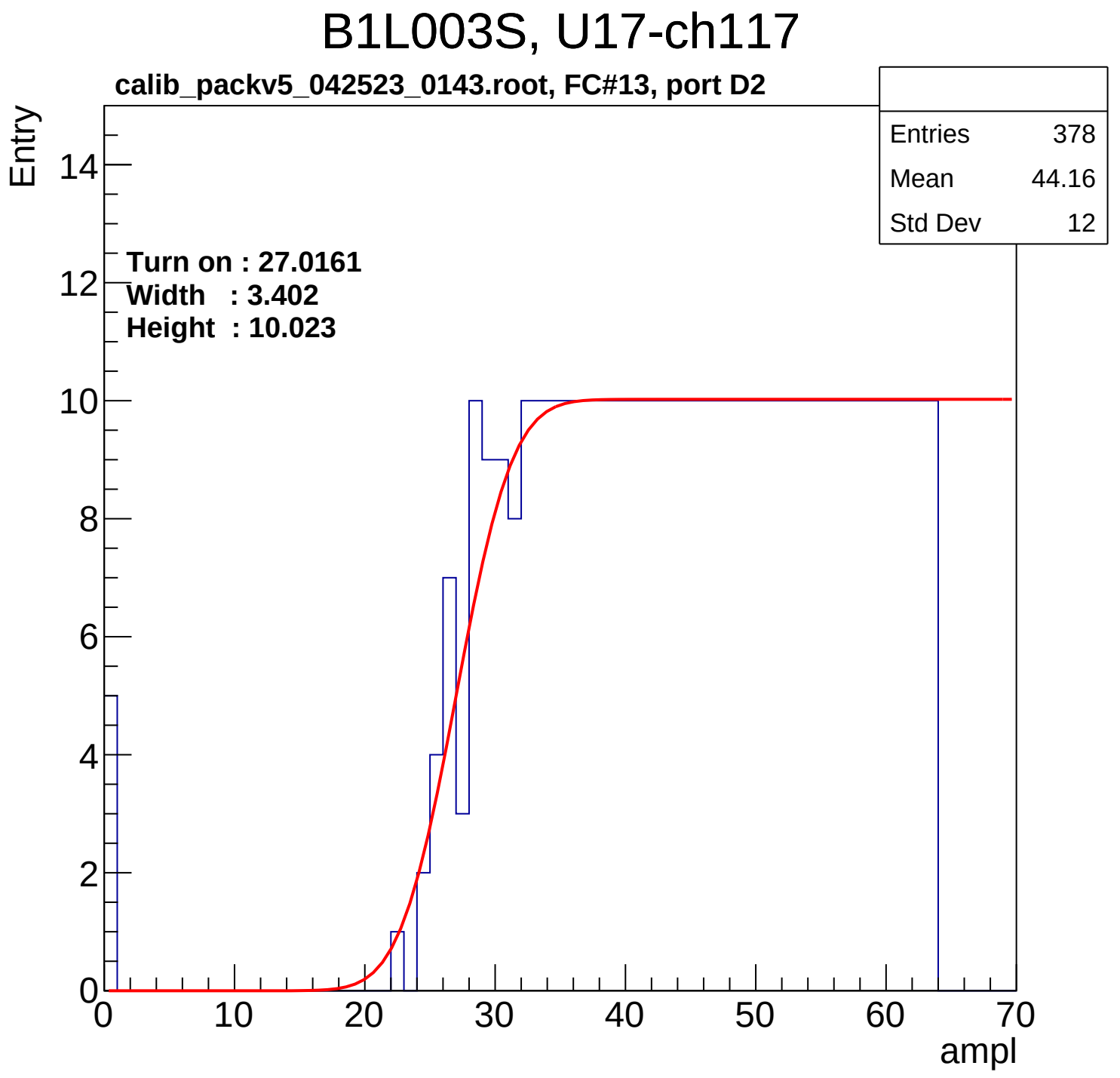
B1L003S, U17-ch117
calib_packv5_042523_0143.root, FC#13, port D2
Entries 378
Mean 44.16
Std Dev 12
Turn on : 27.0161
Width : 3.402
Height : 10.023
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ampl
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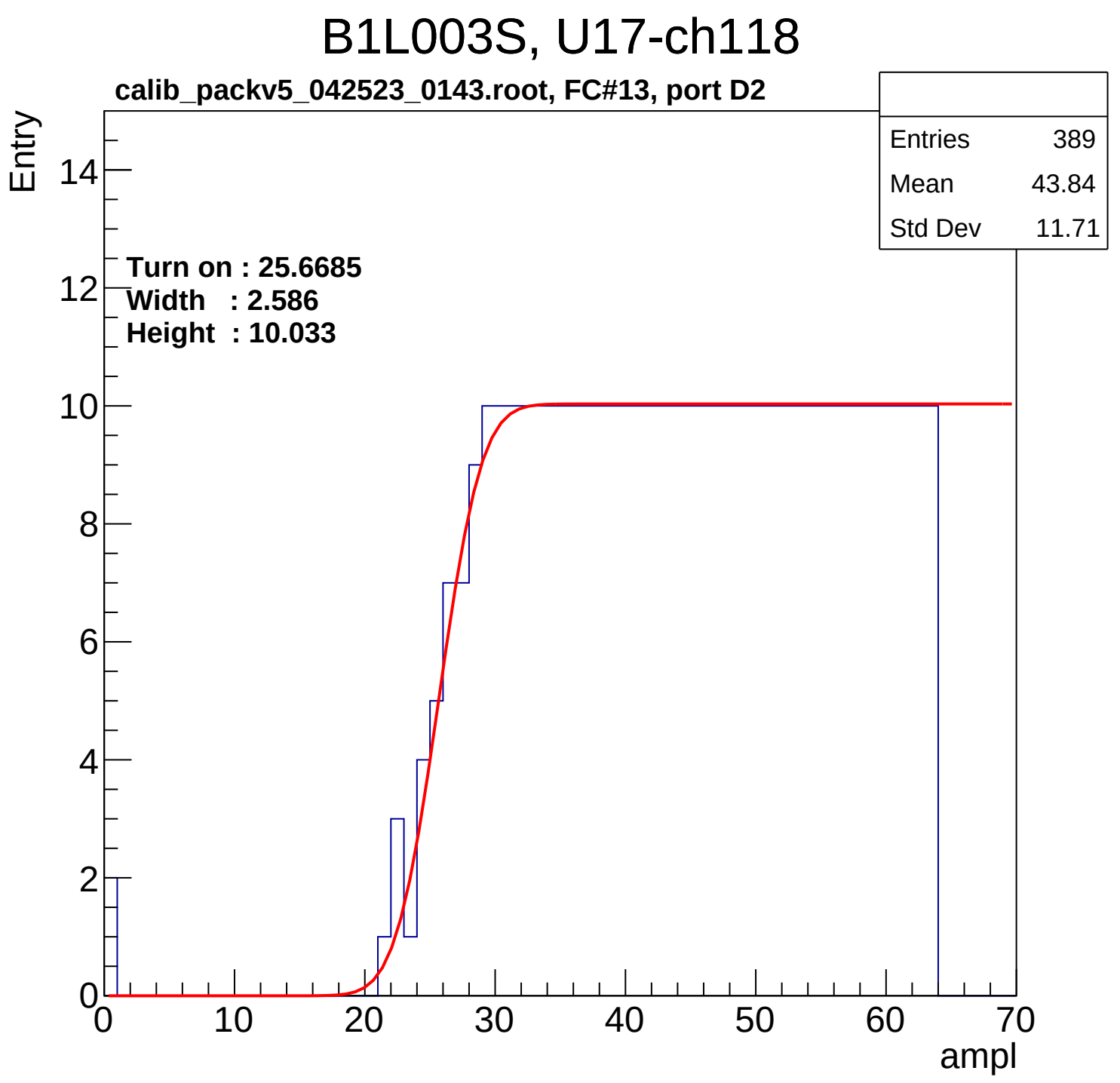
B1L003S, U17-ch118
calib_packv5_042523_0143.root, FC#13, port D2
Entries 389
Mean 43.84
Std Dev 11.71
Turn on : 25.6685
Width : 2.586
Height : 10.033
Entry
ampl
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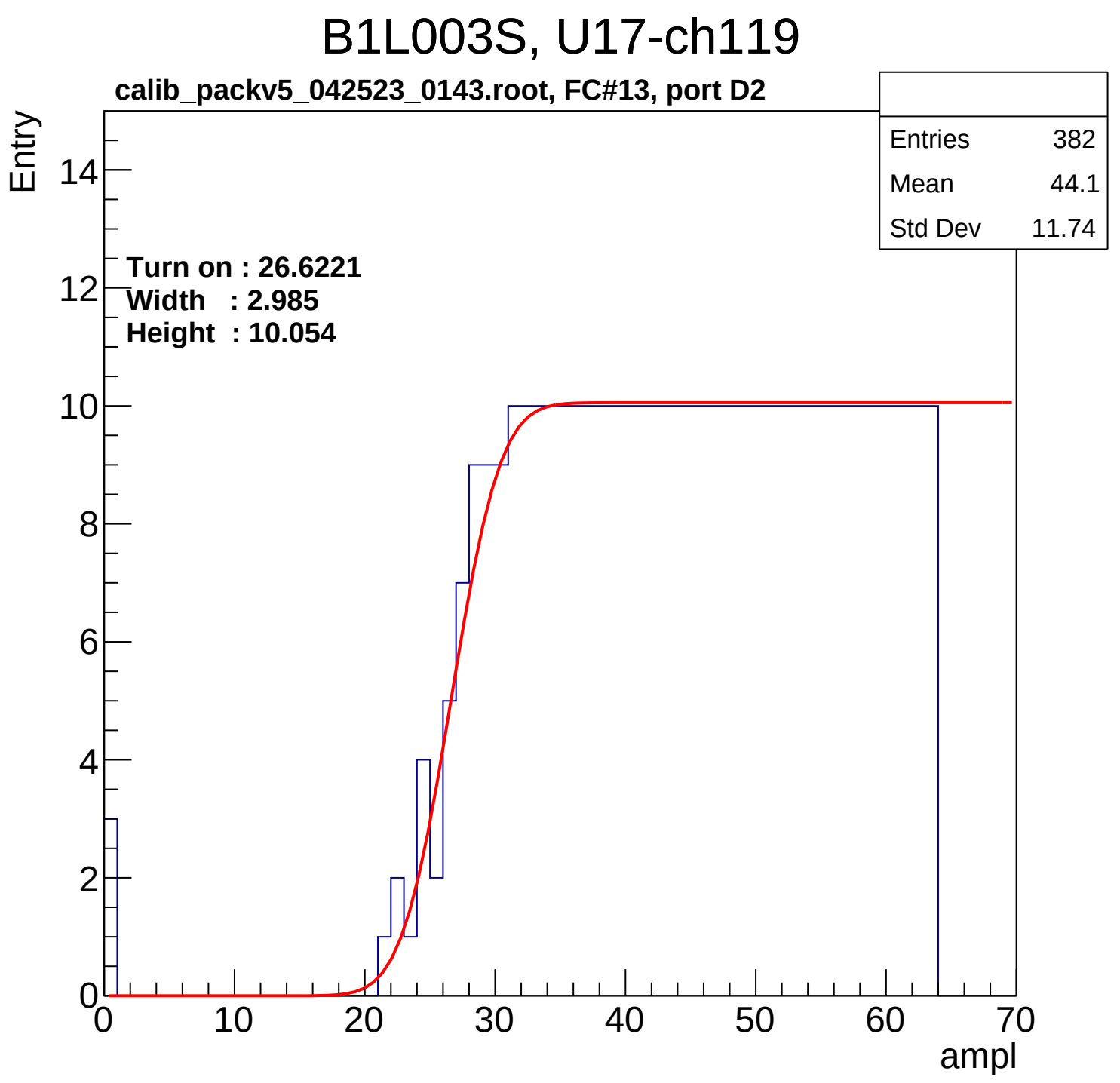
B1L003S, U17-ch119
calib_packv5_042523_0143.root, FC#13, port D2
Entries 382
Mean 44.1
Std Dev 11.74
Turn on : 26.6221
Width : 2.985
Height : 10.054
Entry
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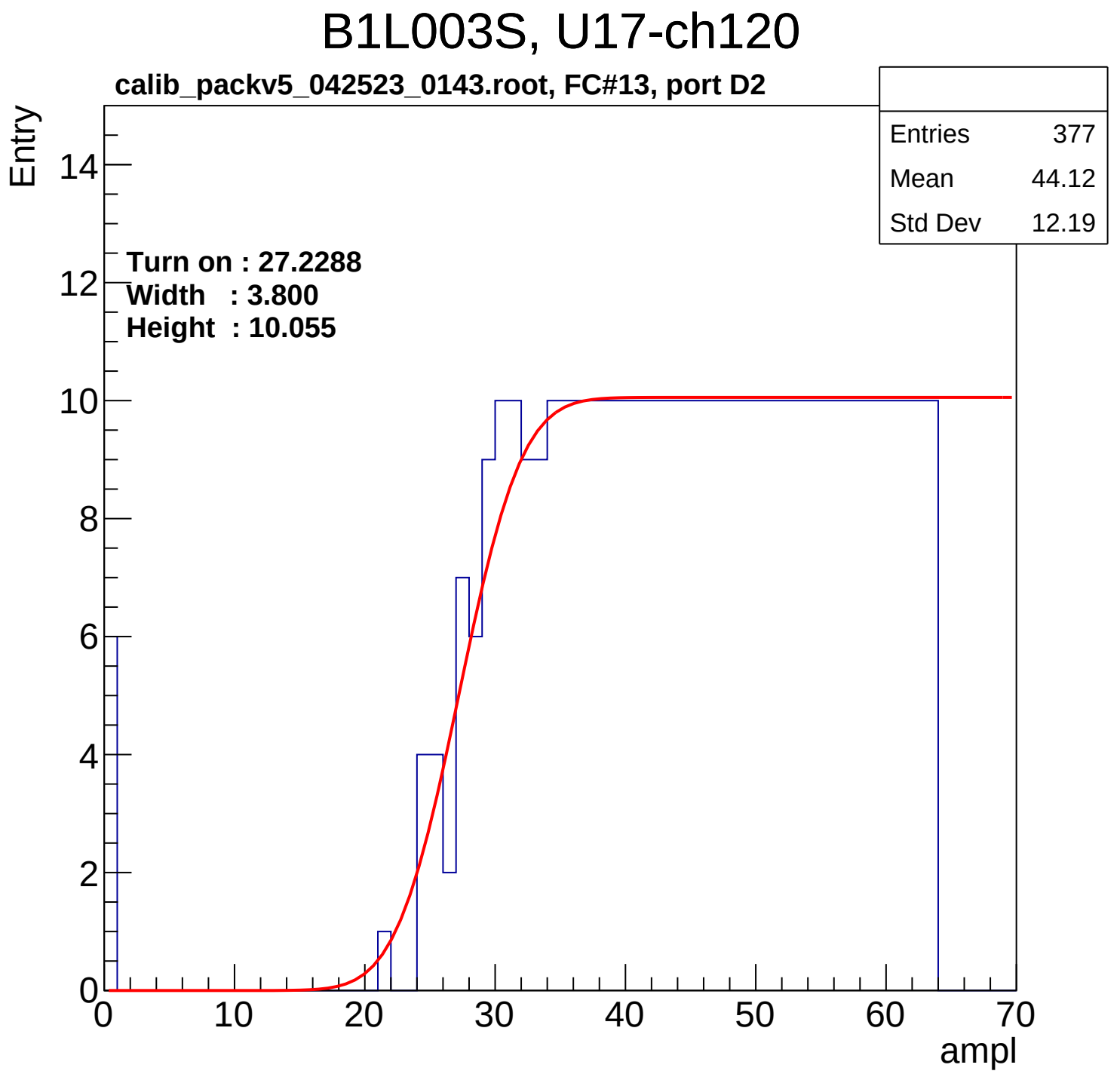
B1L003S, U17-ch120
calib_packv5_042523_0143.root, FC#13, port D2
Entries 377
Mean 44.12
Std Dev 12.19
Turn on : 27.2288
Width : 3.800
Height : 10.055
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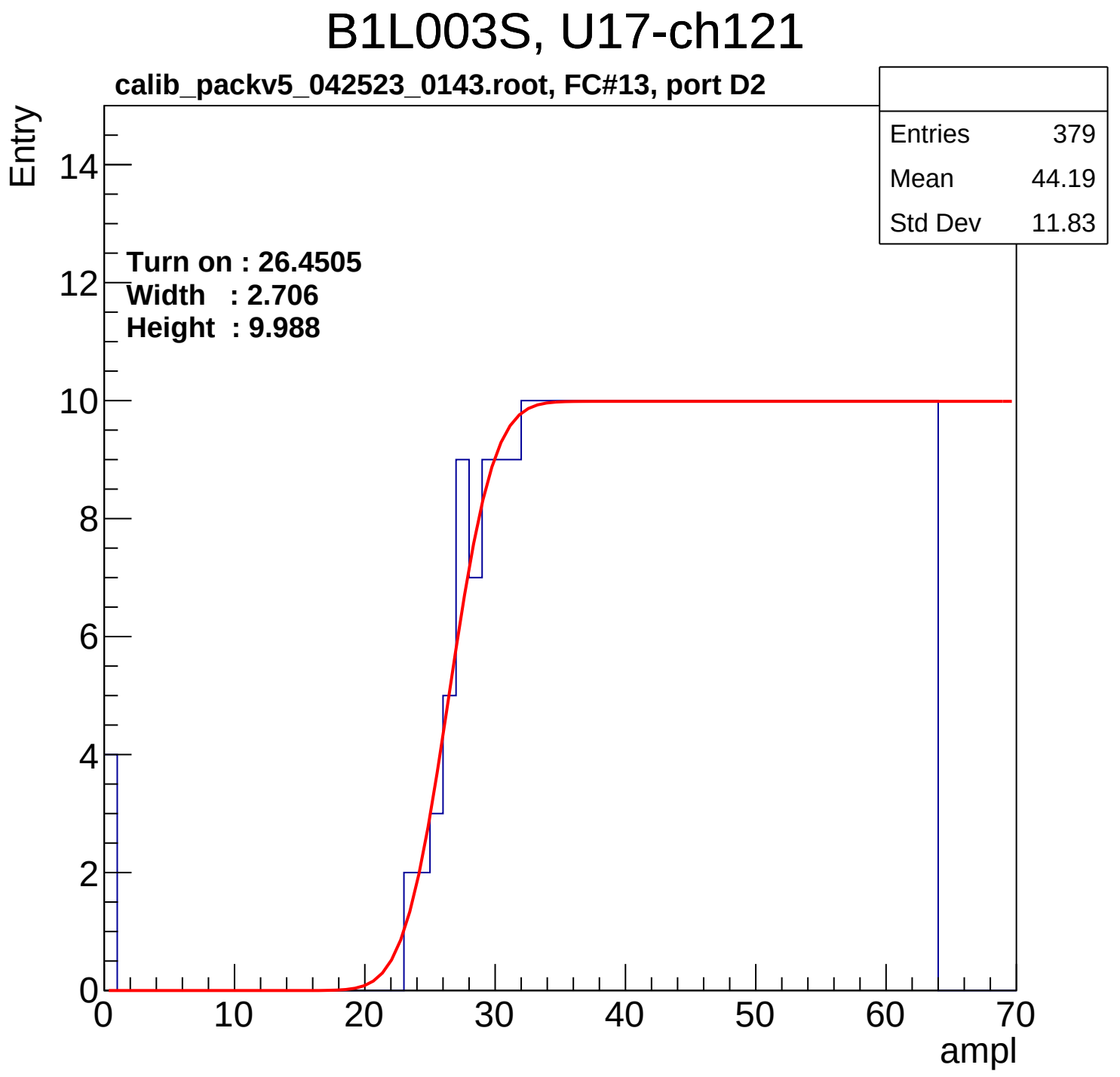
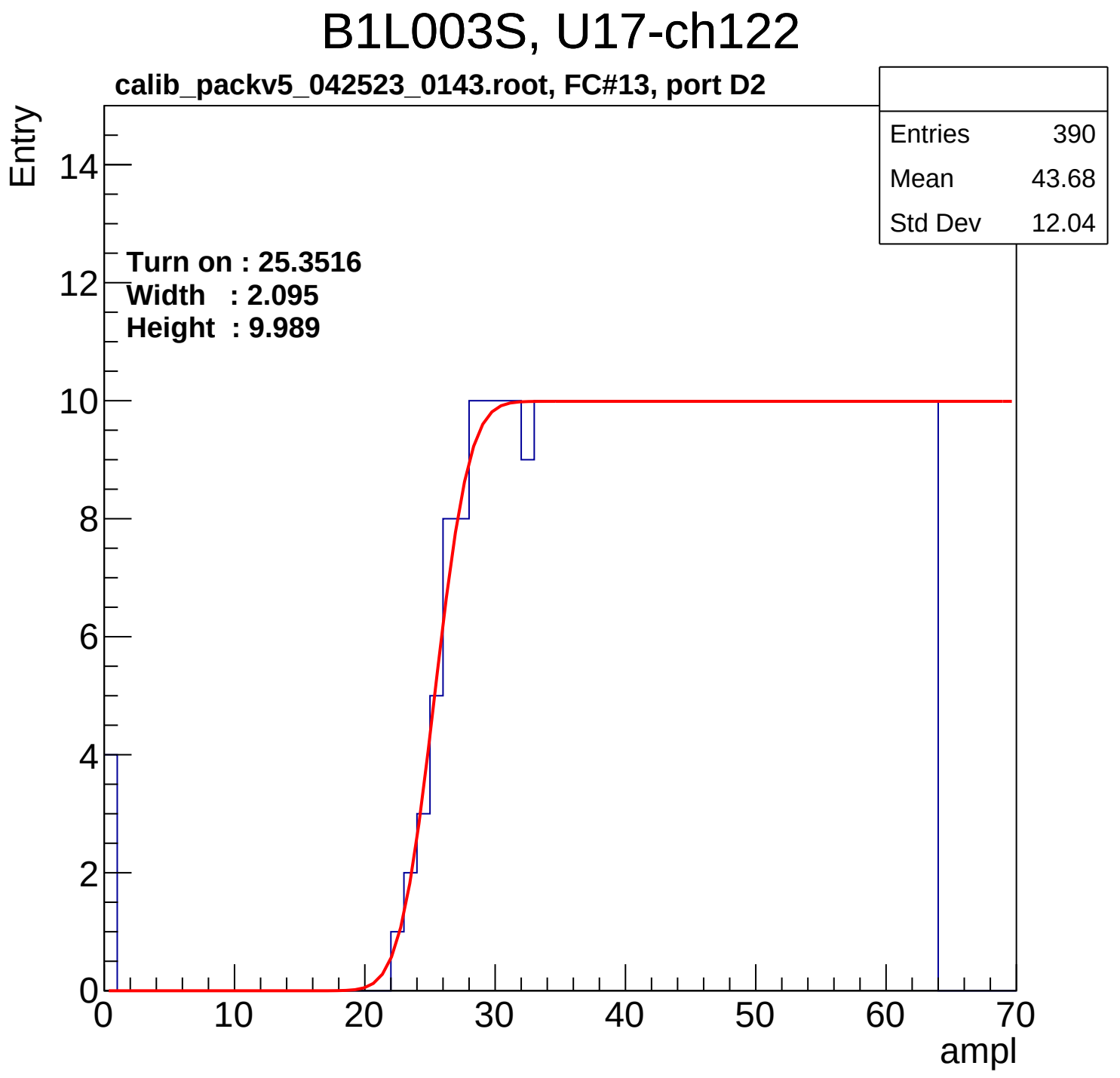
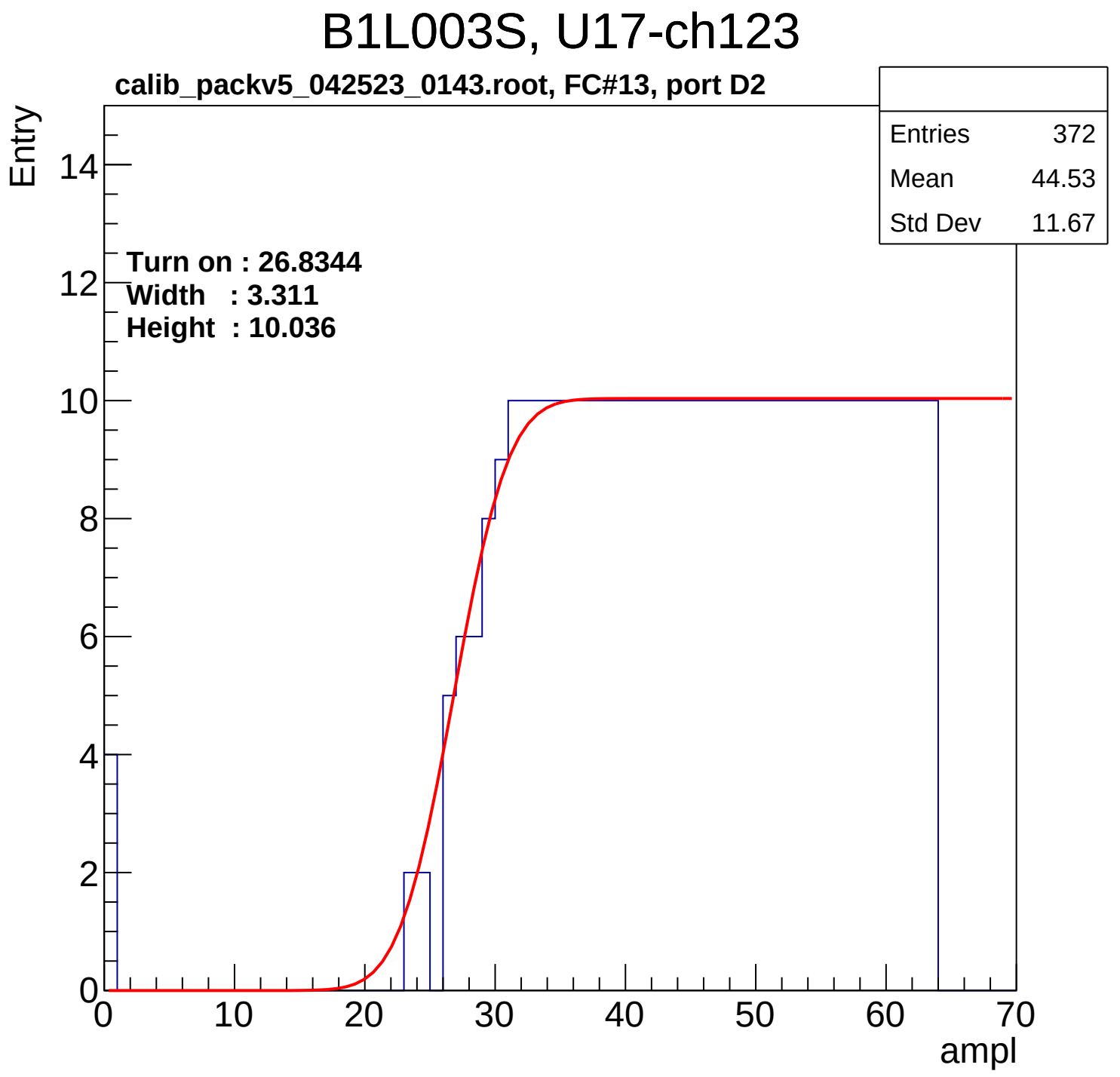
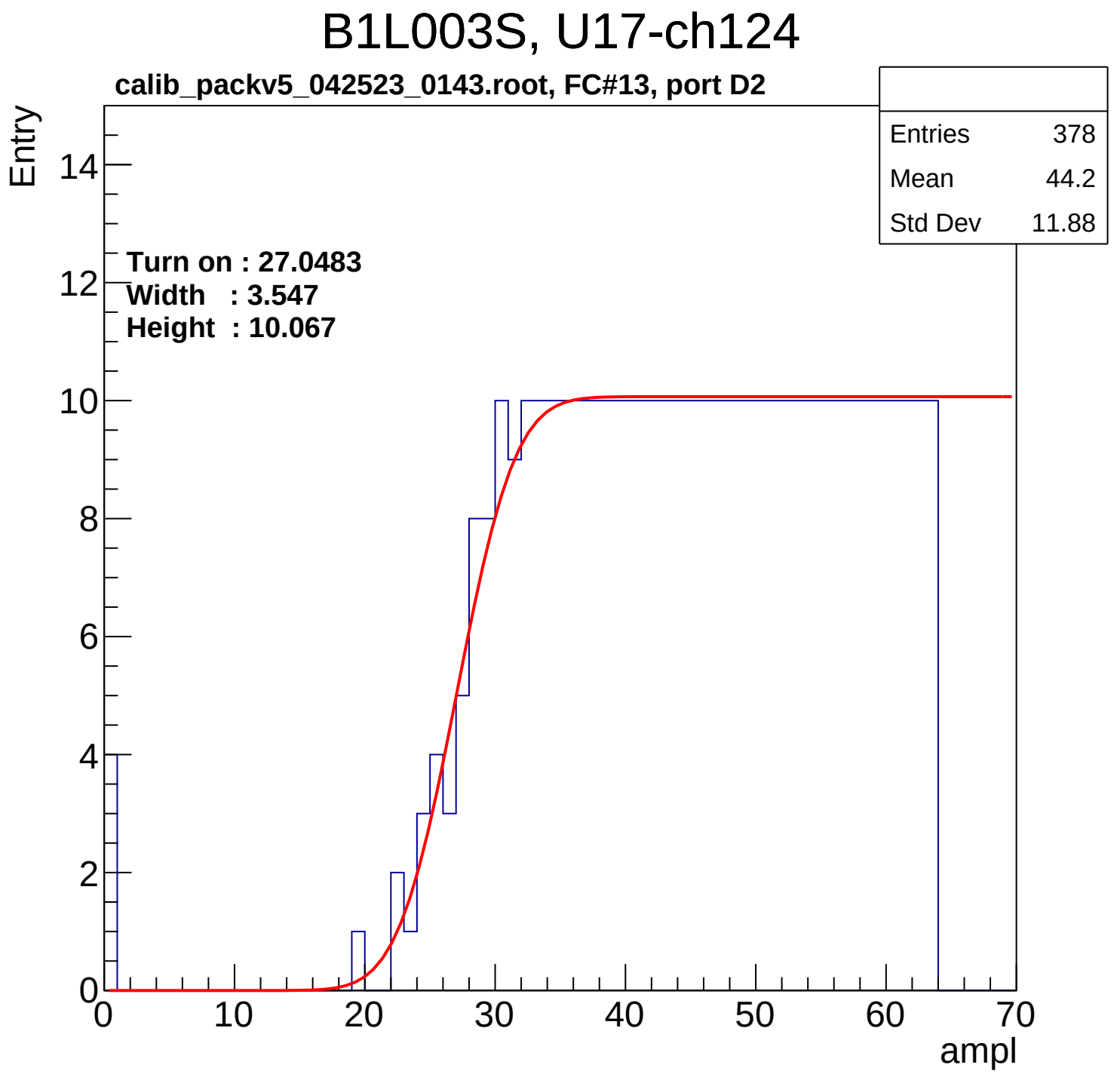
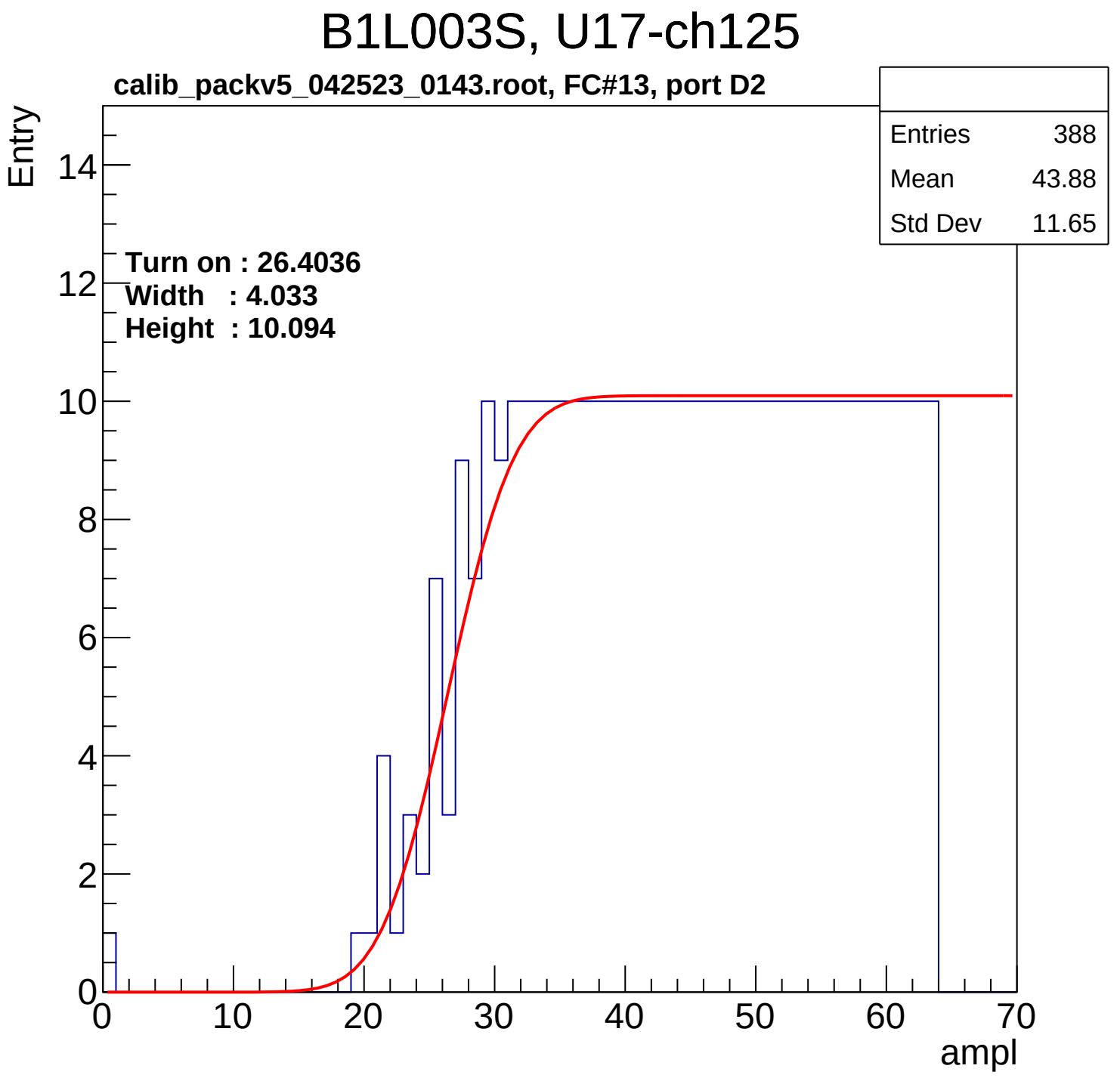
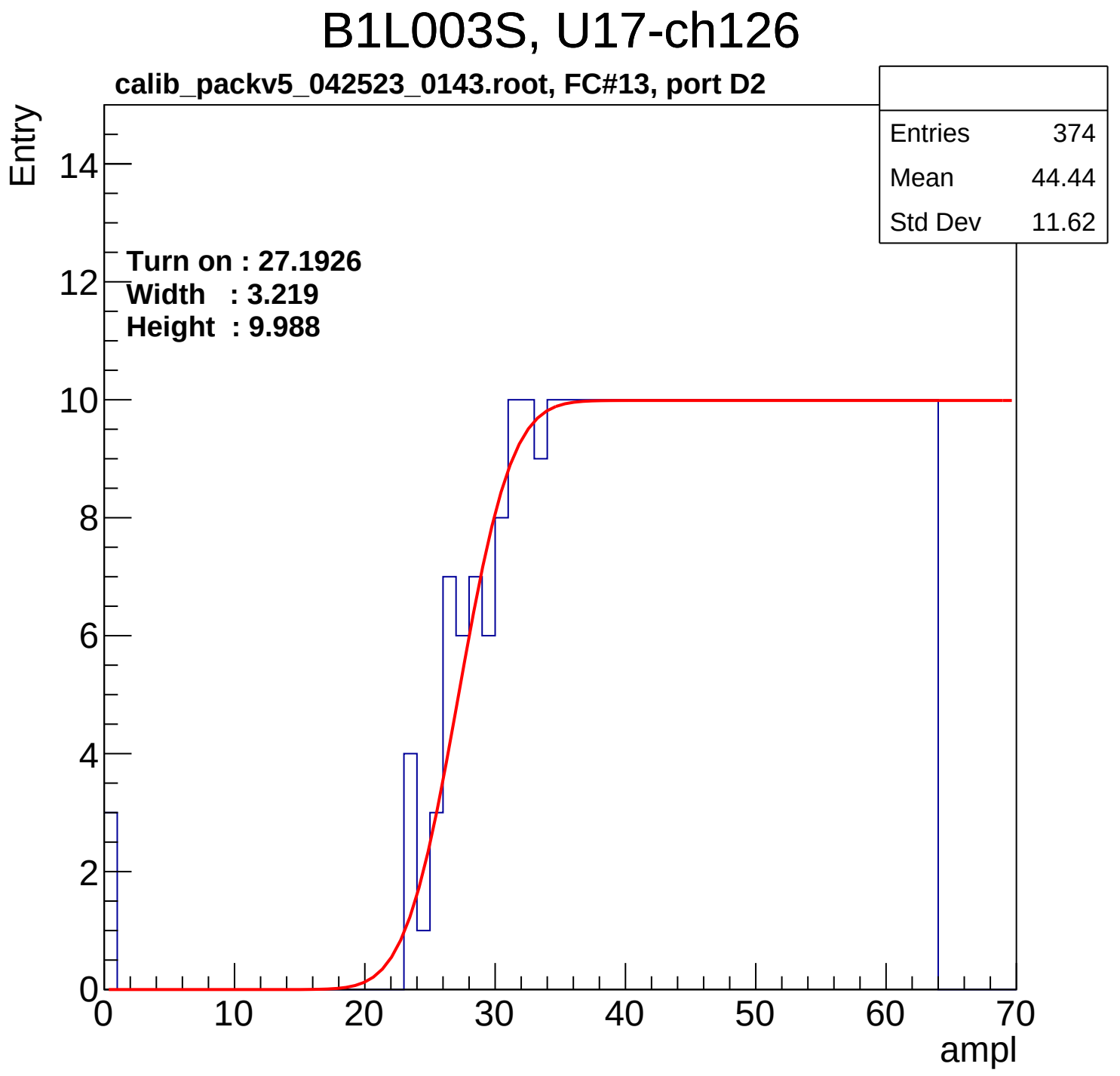

B1L003S, U17-ch121
calib_packv5_042523_0143.root, FC#13, port D2
Entries 379
Mean 44.19
Std Dev 11.83
Turn on : 26.4505
Width : 2.706
Height : 9.988
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

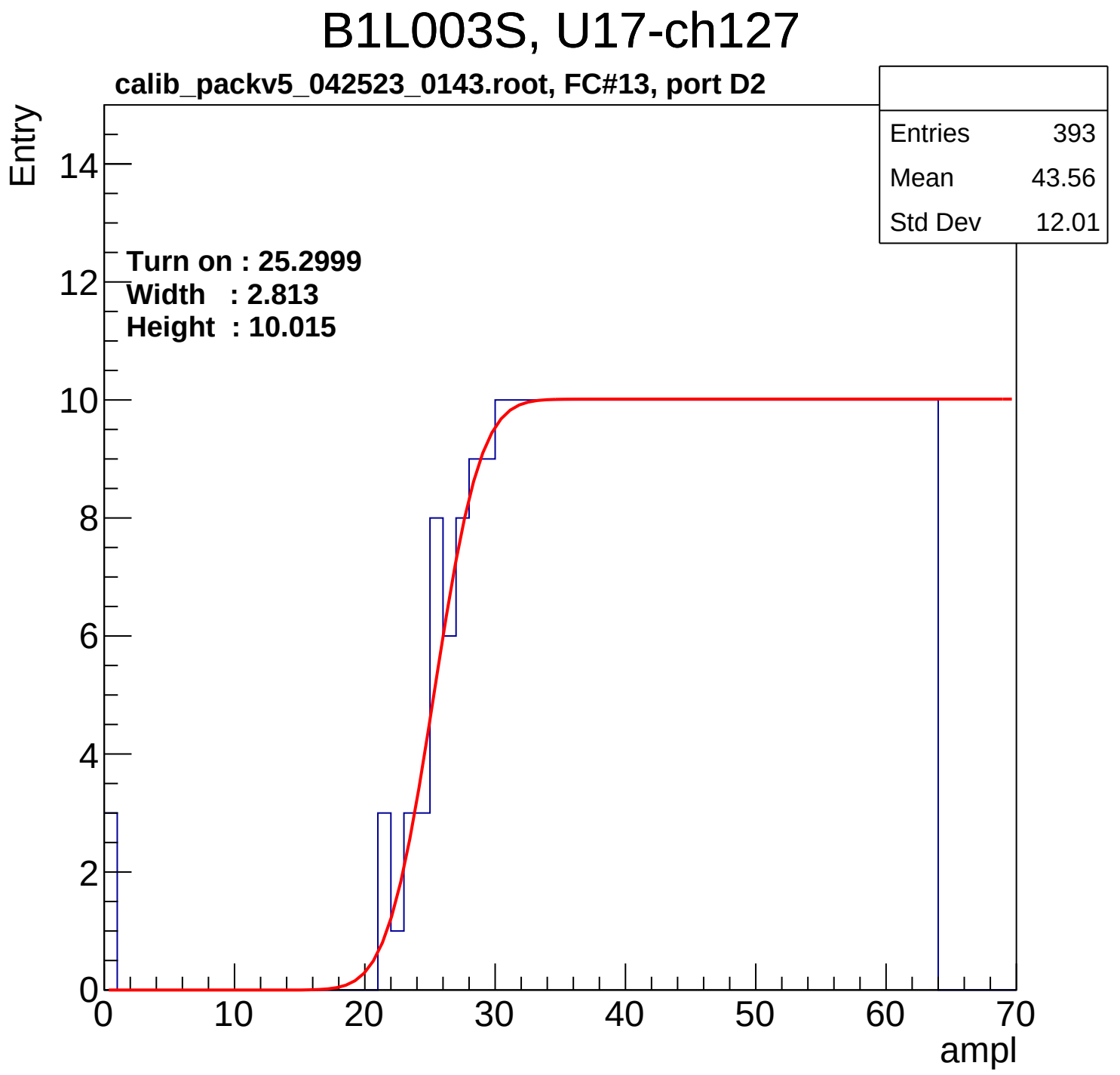

B1L003S, U17-ch122
calib_packv5_042523_0143.root, FC#13, port D2
Entries 390
Mean 43.68
Std Dev 12.04
Turn on : 25.3516
Width : 2.095
Height : 9.989
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

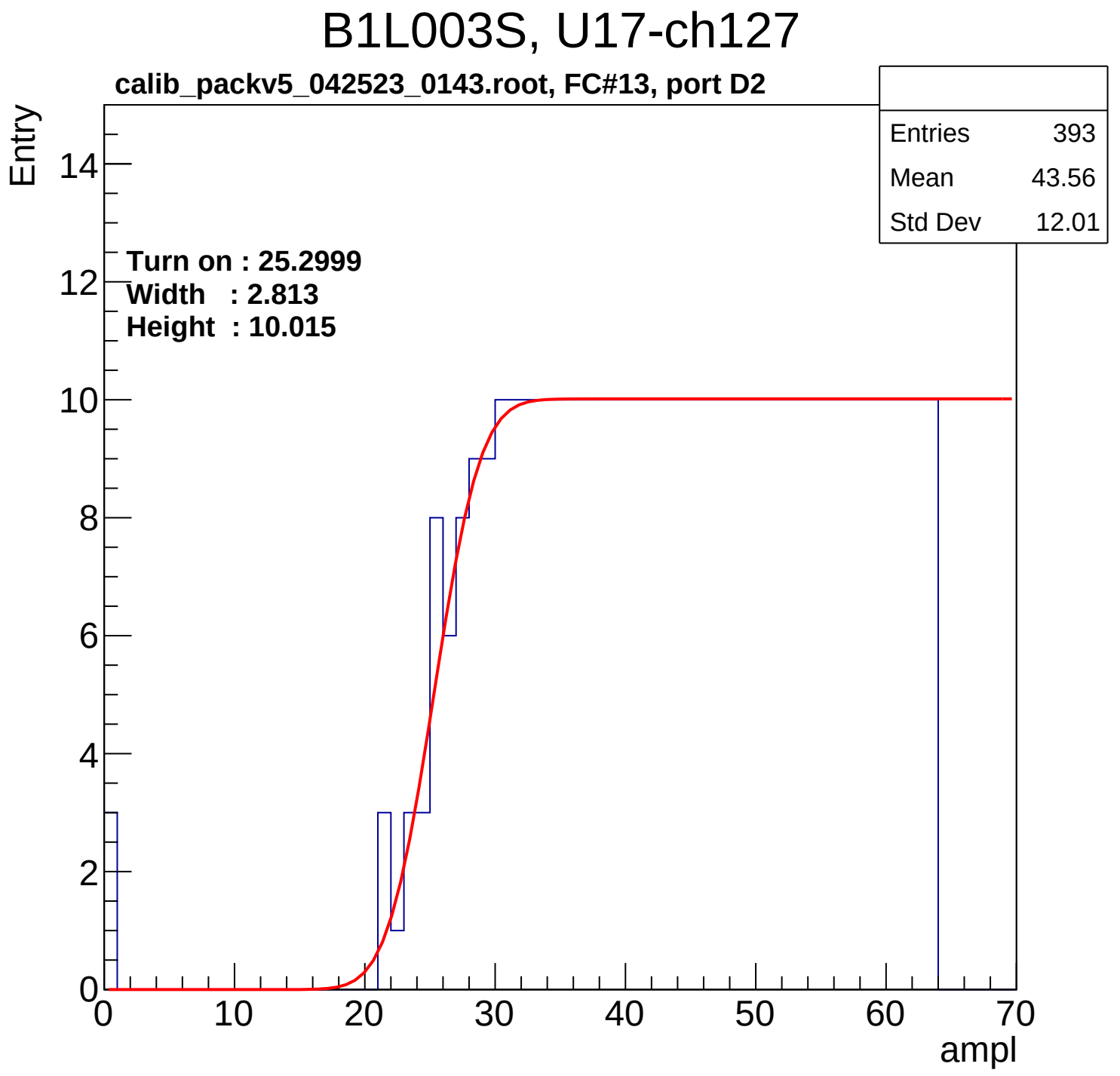

B1L003S, U17-ch123
calib_packv5_042523_0143.root, FC#13, port D2
Entries 372
Mean 44.53
Std Dev 11.67
Turn on : 26.8344
Width : 3.311
Height : 10.036
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L003S, U17-ch124
calib_packv5_042523_0143.root, FC#13, port D2
Entries 378
Mean 44.2
Std Dev 11.88
Turn on : 27.0483
Width : 3.547
Height : 10.067
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L003S, U17-ch125
calib_packv5_042523_0143.root, FC#13, port D2
Entries 388
Mean 43.88
Std Dev 11.65
Turn on : 26.4036
Width : 4.033
Height : 10.094
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L003S, U17-ch126
calib_packv5_042523_0143.root, FC#13, port D2
Entries 374
Mean 44.44
Std Dev 11.62
Turn on : 27.1926
Width : 3.219
Height : 9.988
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L003S, U17-ch127
calib_packv5_042523_0143.root, FC#13, port D2
Entries 393
Mean 43.56
Std Dev 12.01
Turn on : 25.2999
Width : 2.813
Height : 10.015
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L003S, U17-ch127
calib_packv5_042523_0143.root, FC#13, port D2
Entries 393
Mean 43.56
Std Dev 12.01
Turn on : 25.2999
Width : 2.813
Height : 10.015
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70