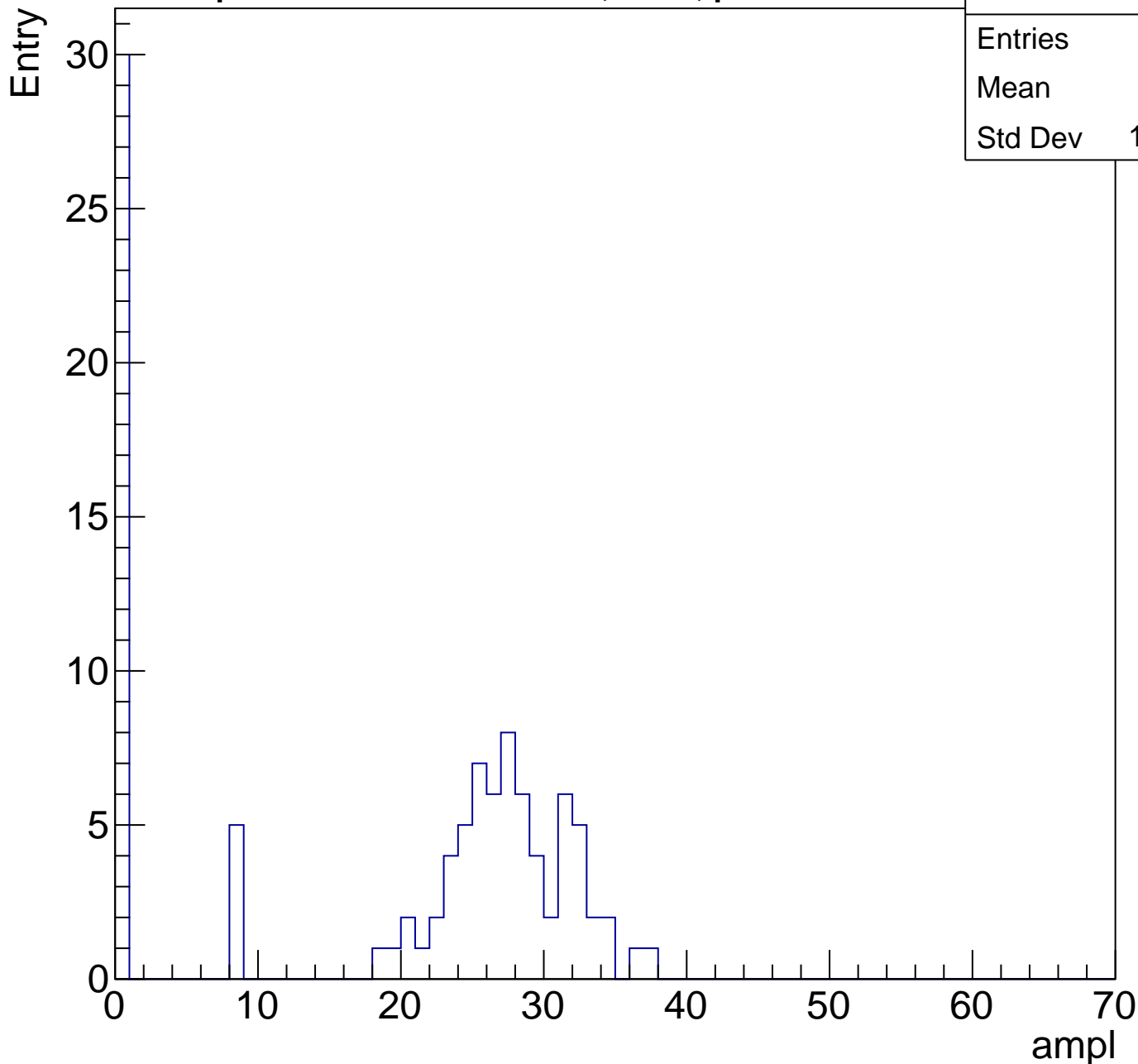




# B1L103S, U25-ch0, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	101
Mean	18.2
Std Dev	12.95

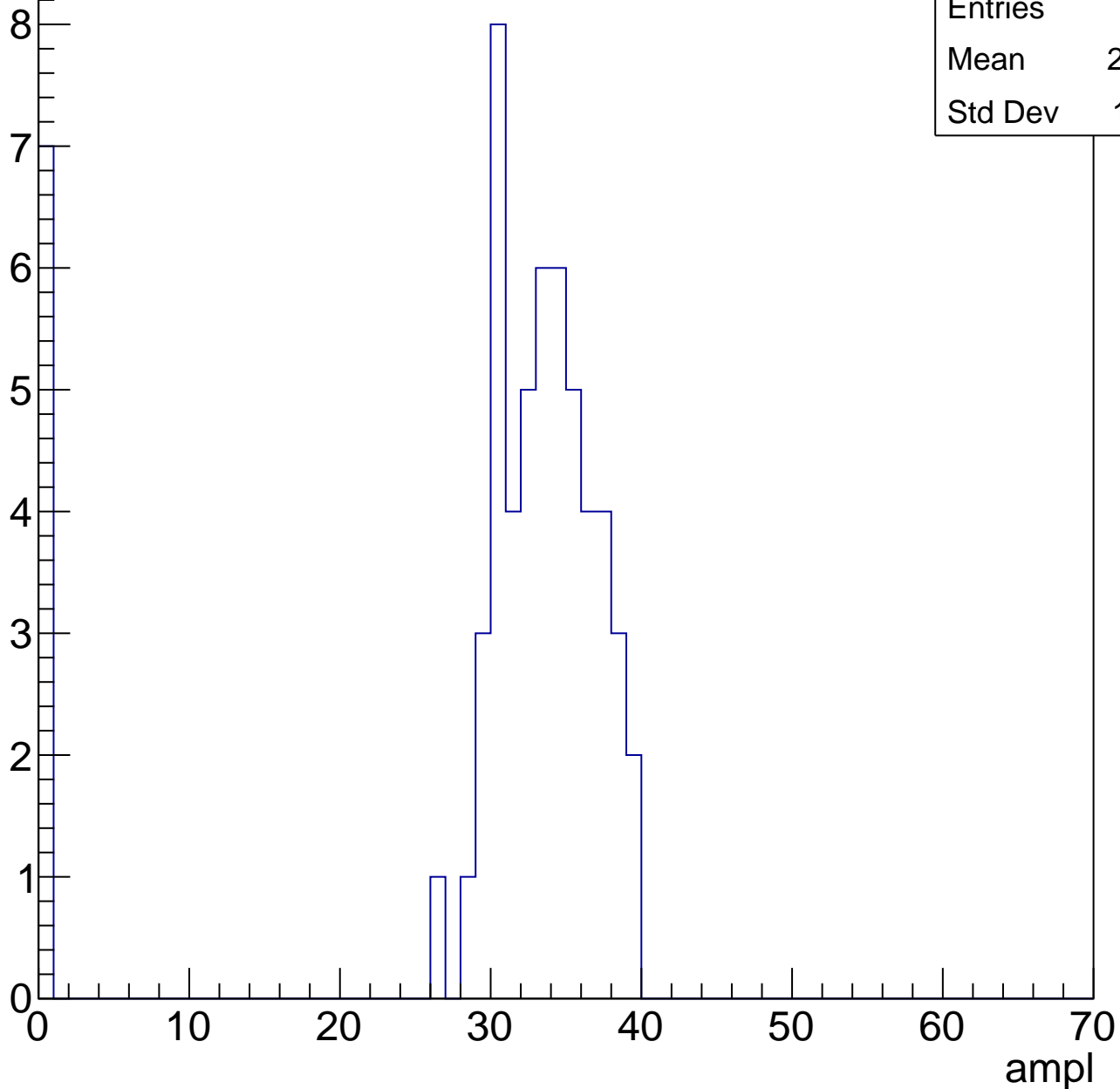


# B1L103S, U25-ch0, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	59
Mean	29.25
Std Dev	11.11

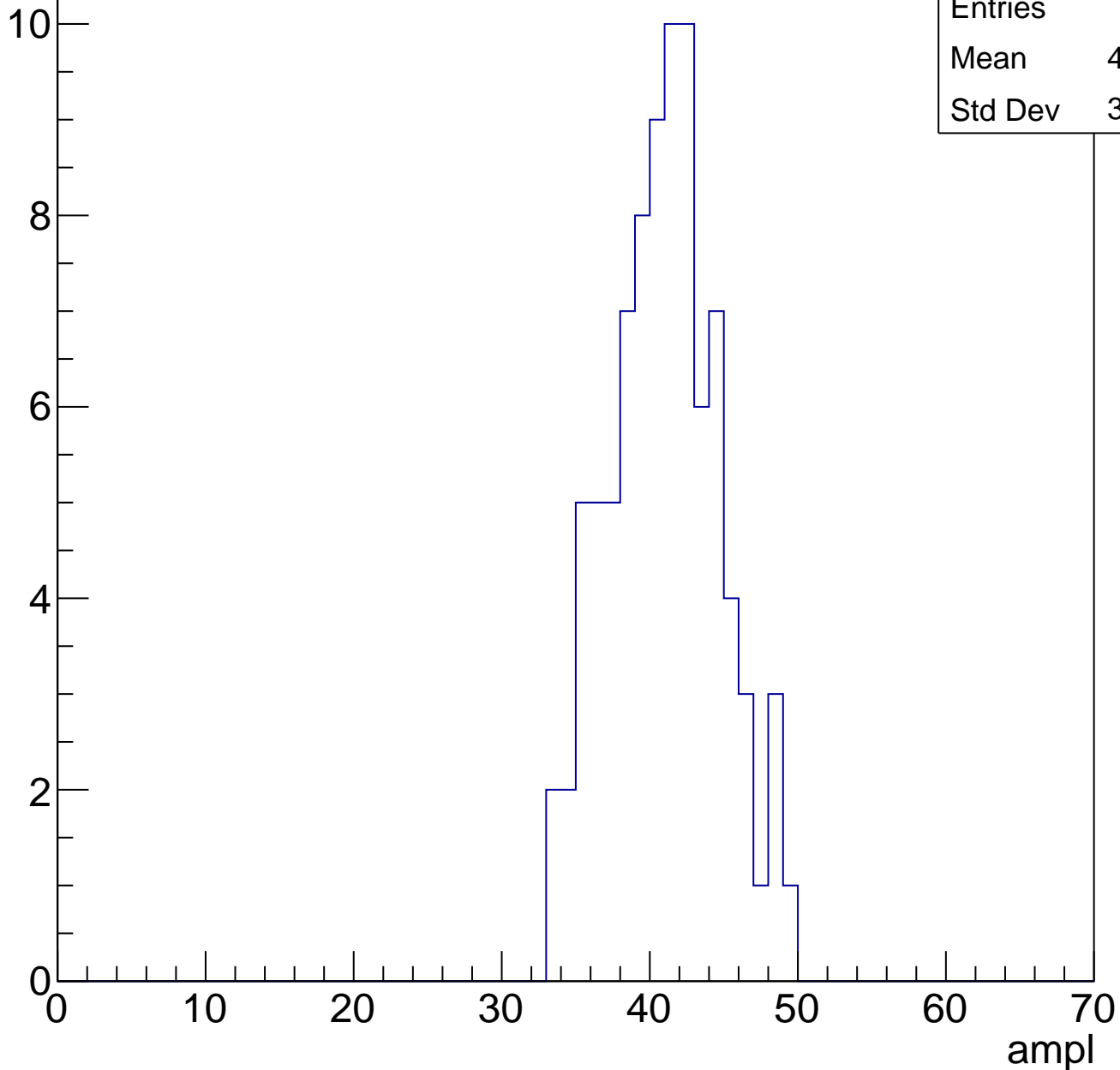


# B1L103S, U25-ch0, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

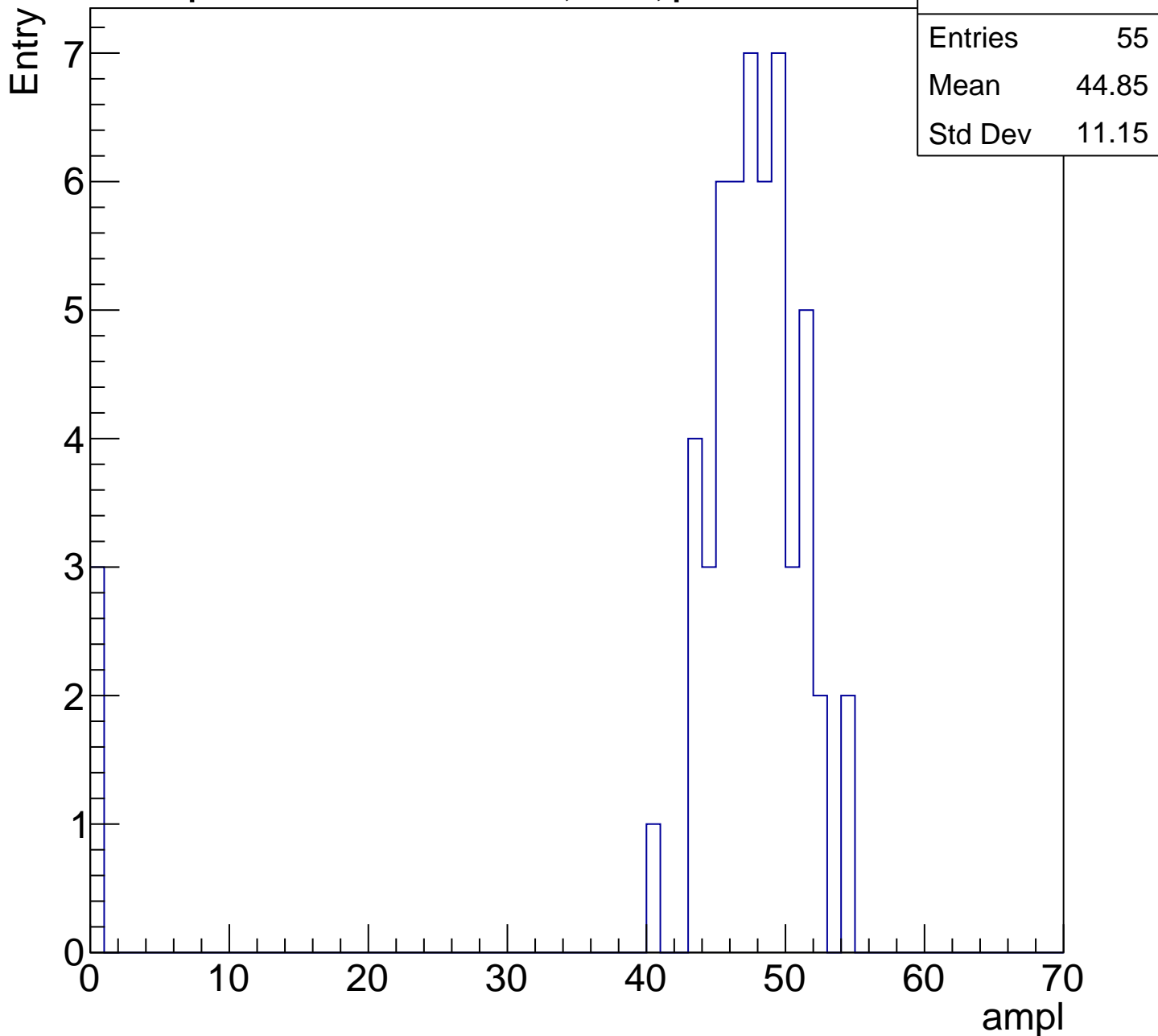
Entries	88
Mean	40.52
Std Dev	3.659

Entry



# B1L103S, U25-ch0, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2



# B1L103S, U25-ch0, adc4

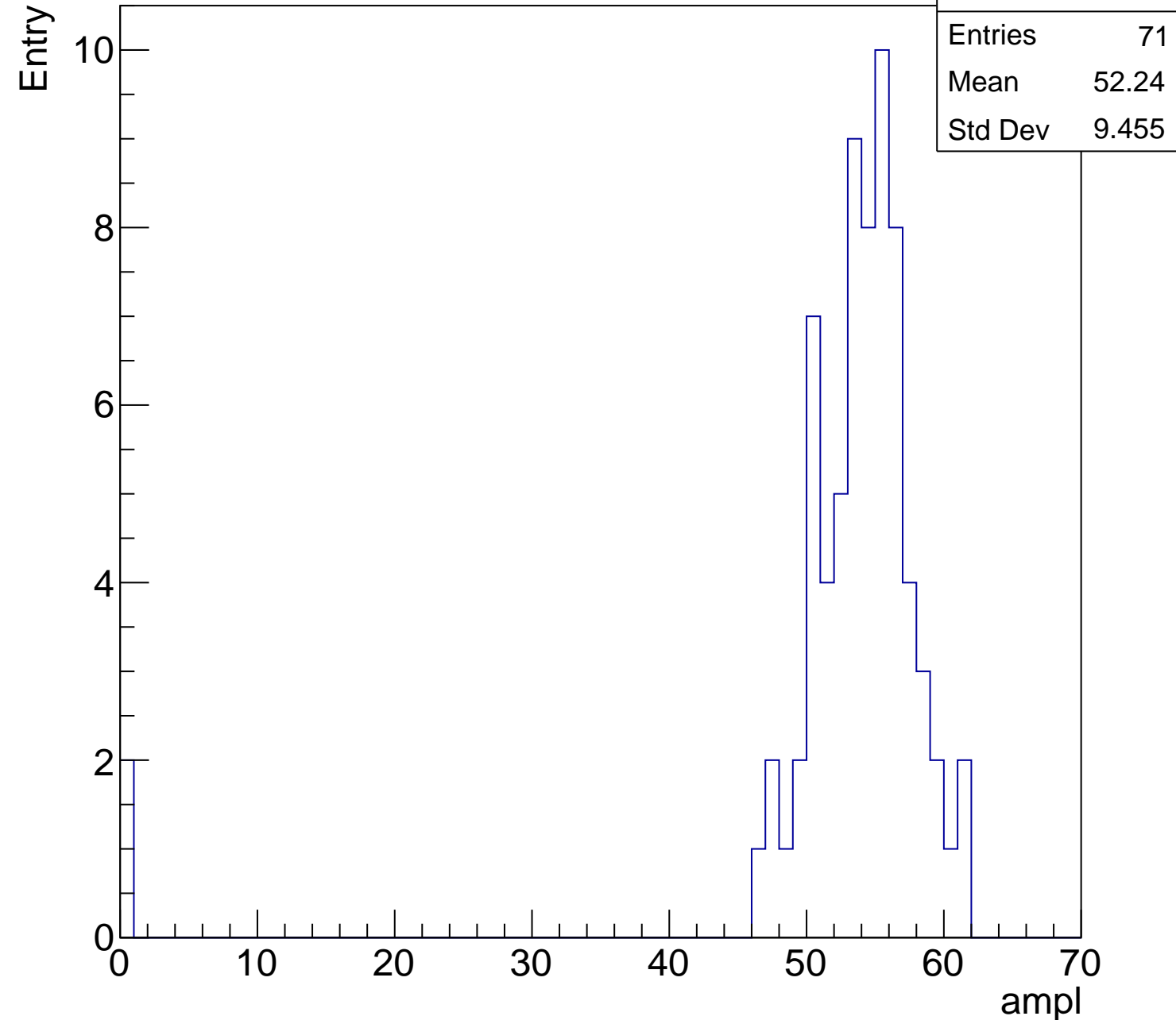
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	71
Mean	52.24
Std Dev	9.455

Entry

10  
8  
6  
4  
2  
0

ampl

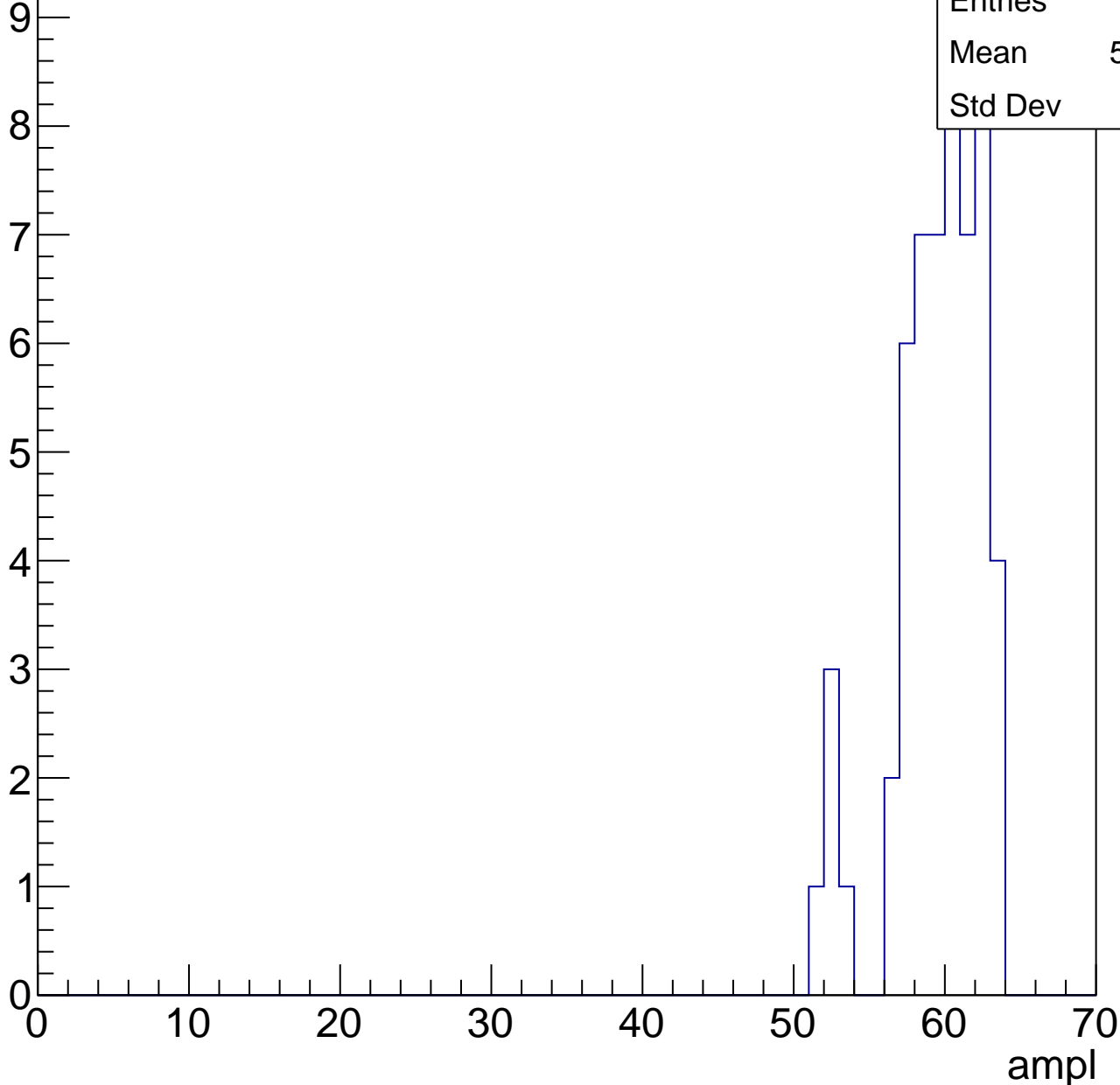


# B1L103S, U25-ch0, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	55
Mean	59.05
Std Dev	2.92

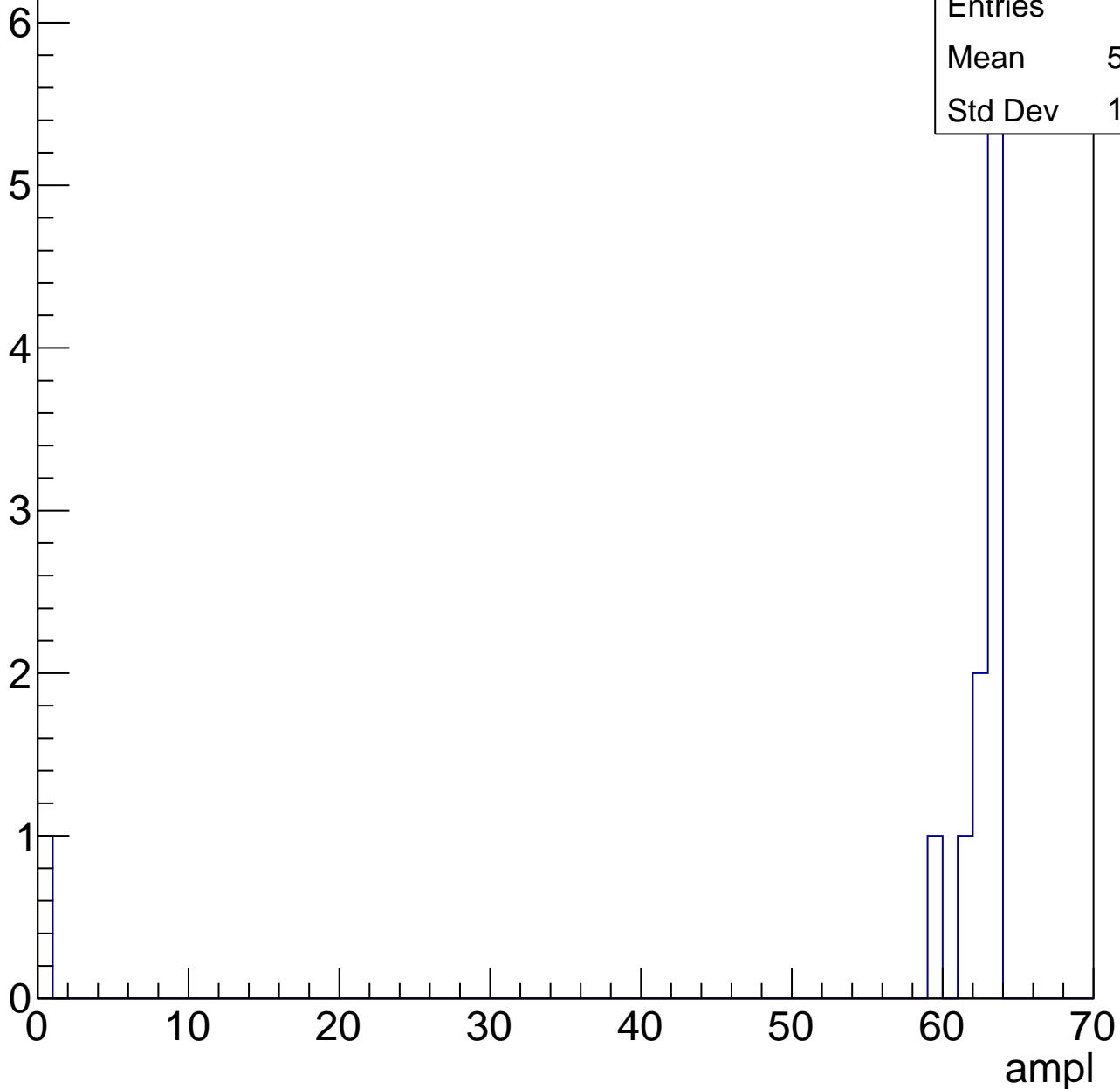


# B1L103S, U25-ch0, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	11
Mean	56.55
Std Dev	17.92





# B1L103S, U25-ch0, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

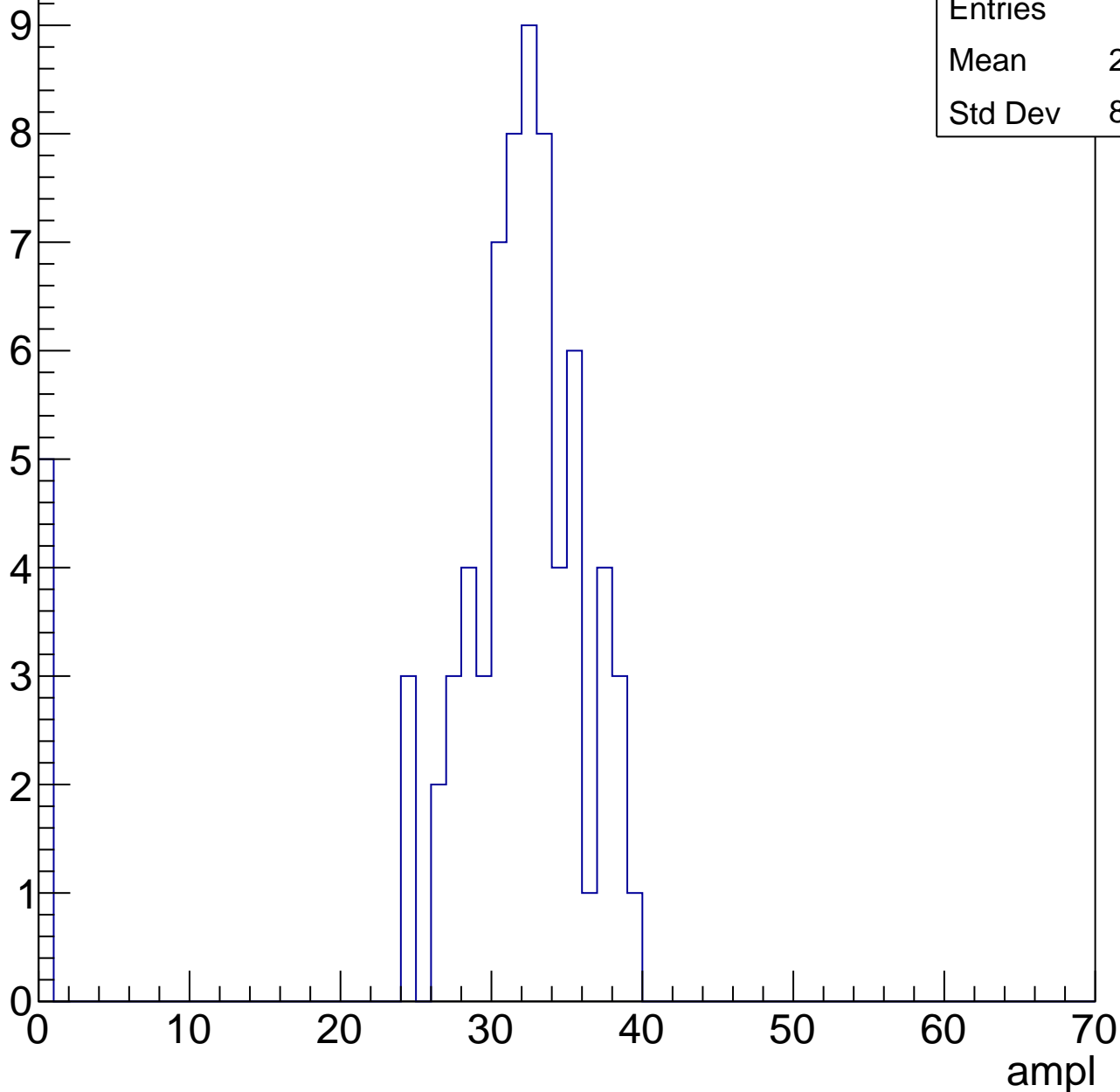


# B1L103S, U25-ch1, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

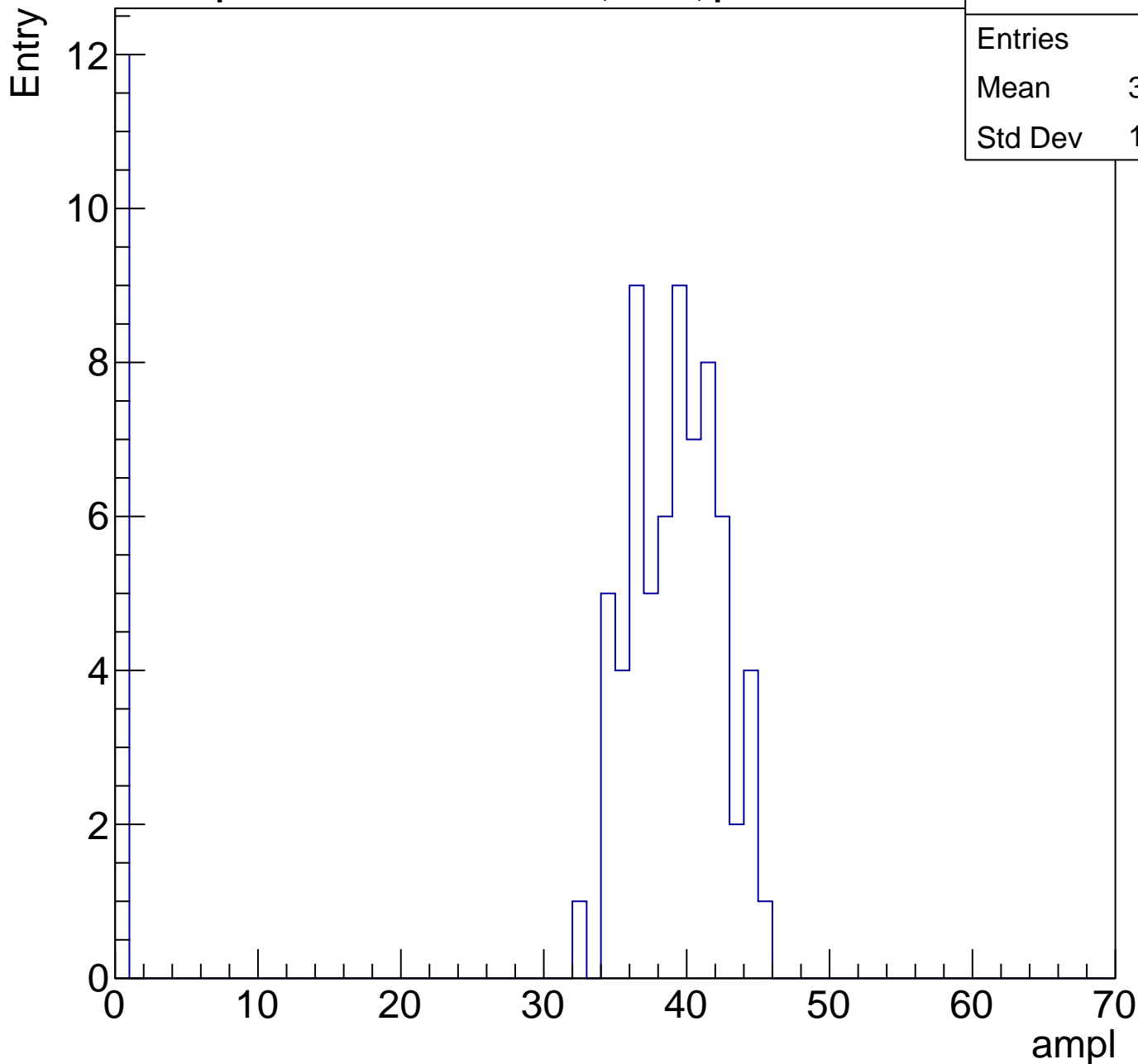
Entries	71
Mean	29.54
Std Dev	8.806



# B1L103S, U25-ch1, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	79
Mean	32.87
Std Dev	14.18

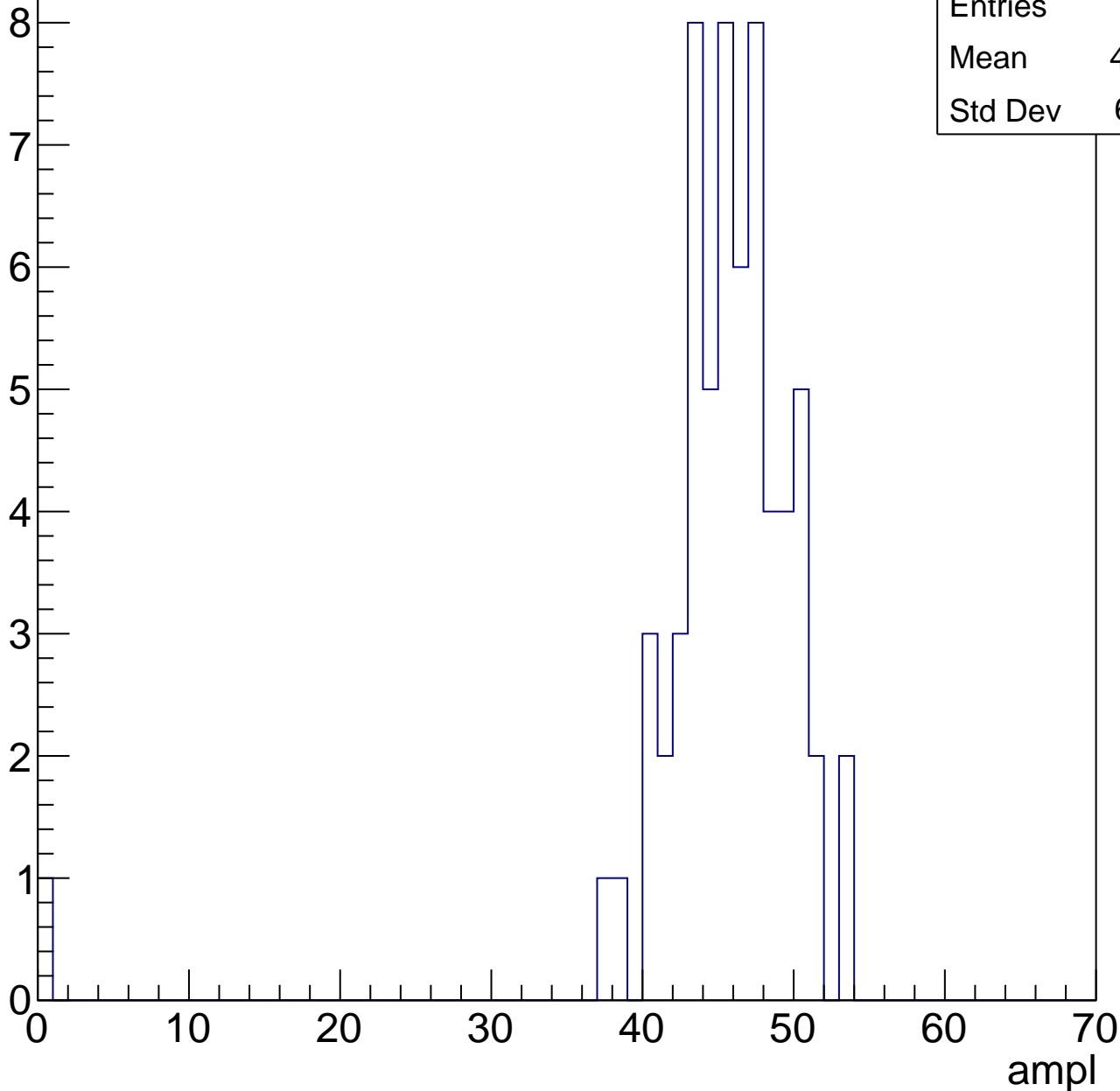


# B1L103S, U25-ch1, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

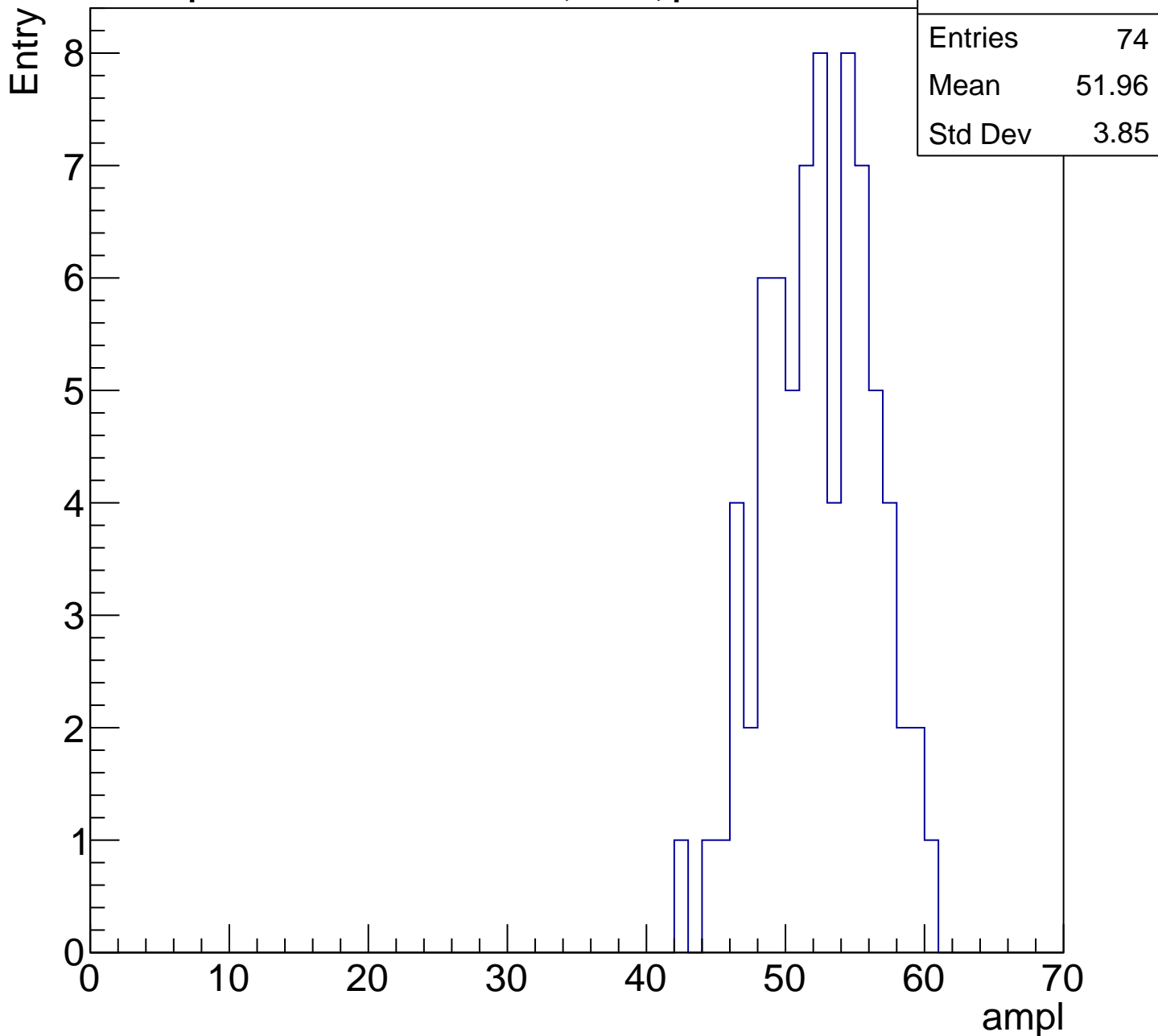
Entry

Entries	63
Mean	44.84
Std Dev	6.631



# B1L103S, U25-ch1, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

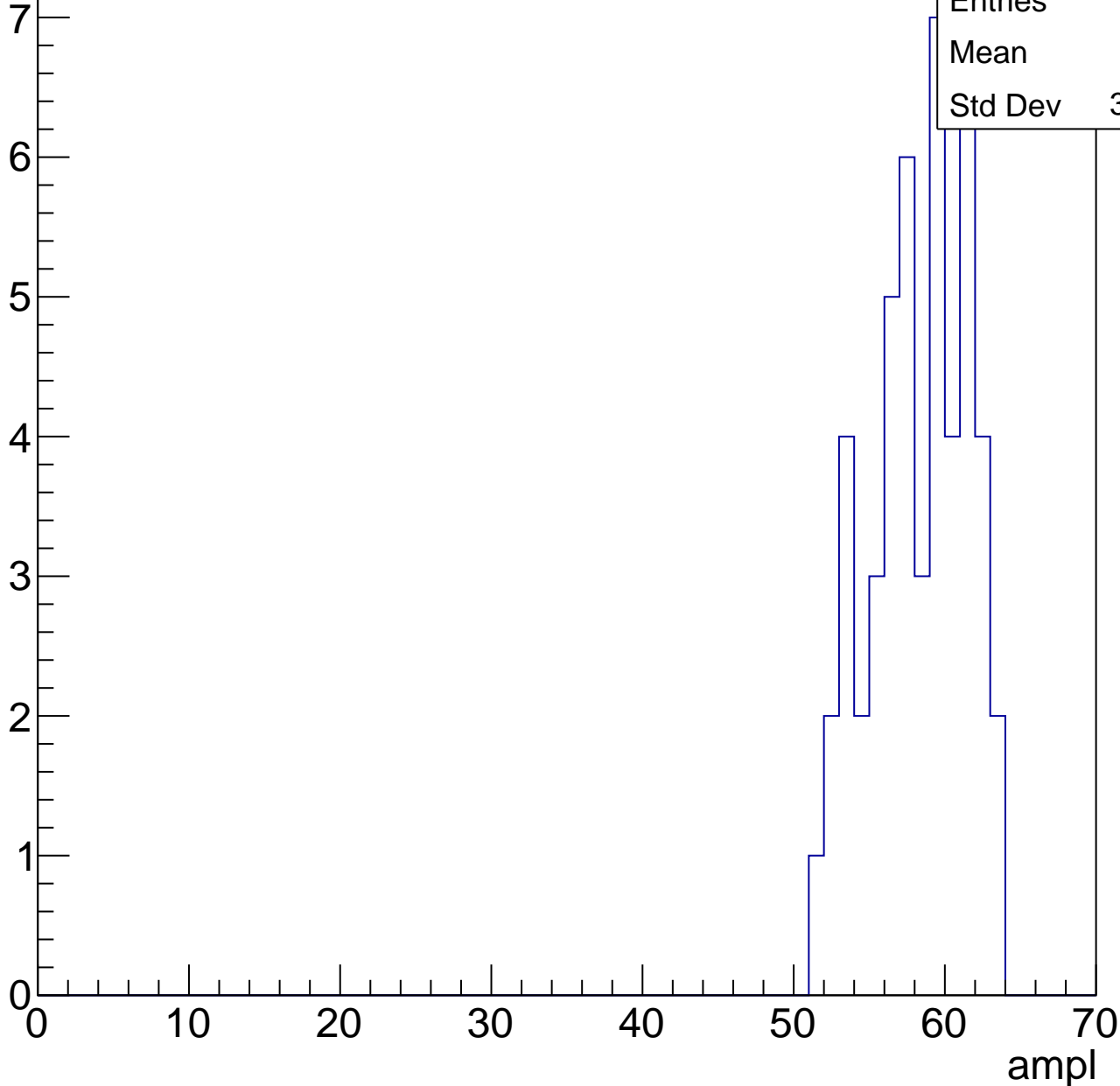


# B1L103S, U25-ch1, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	50
Mean	57.8
Std Dev	3.175

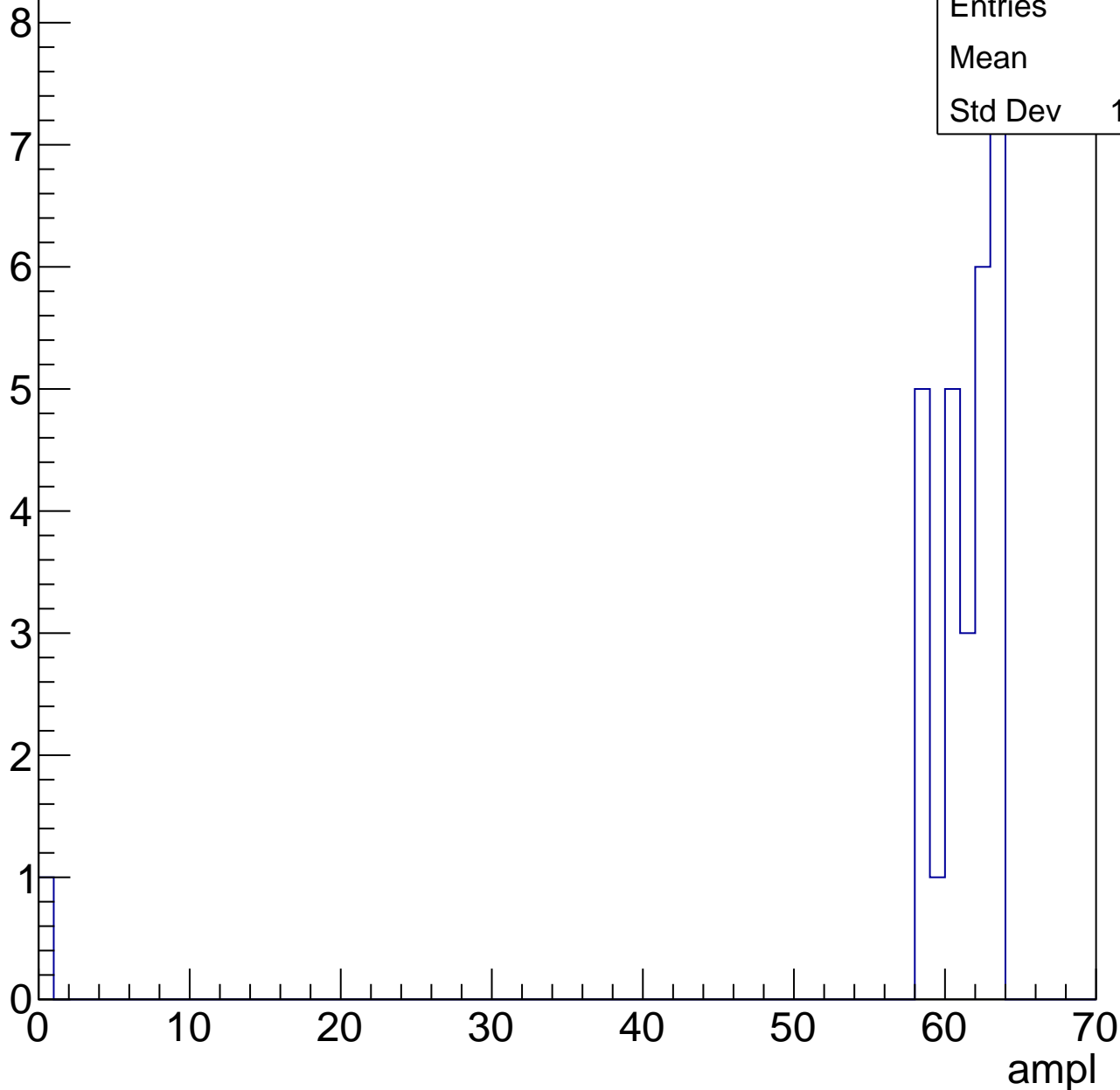


# B1L103S, U25-ch1, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	29
Mean	58.9
Std Dev	11.27



# B1L103S, U25-ch1, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L103S, U25-ch1, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

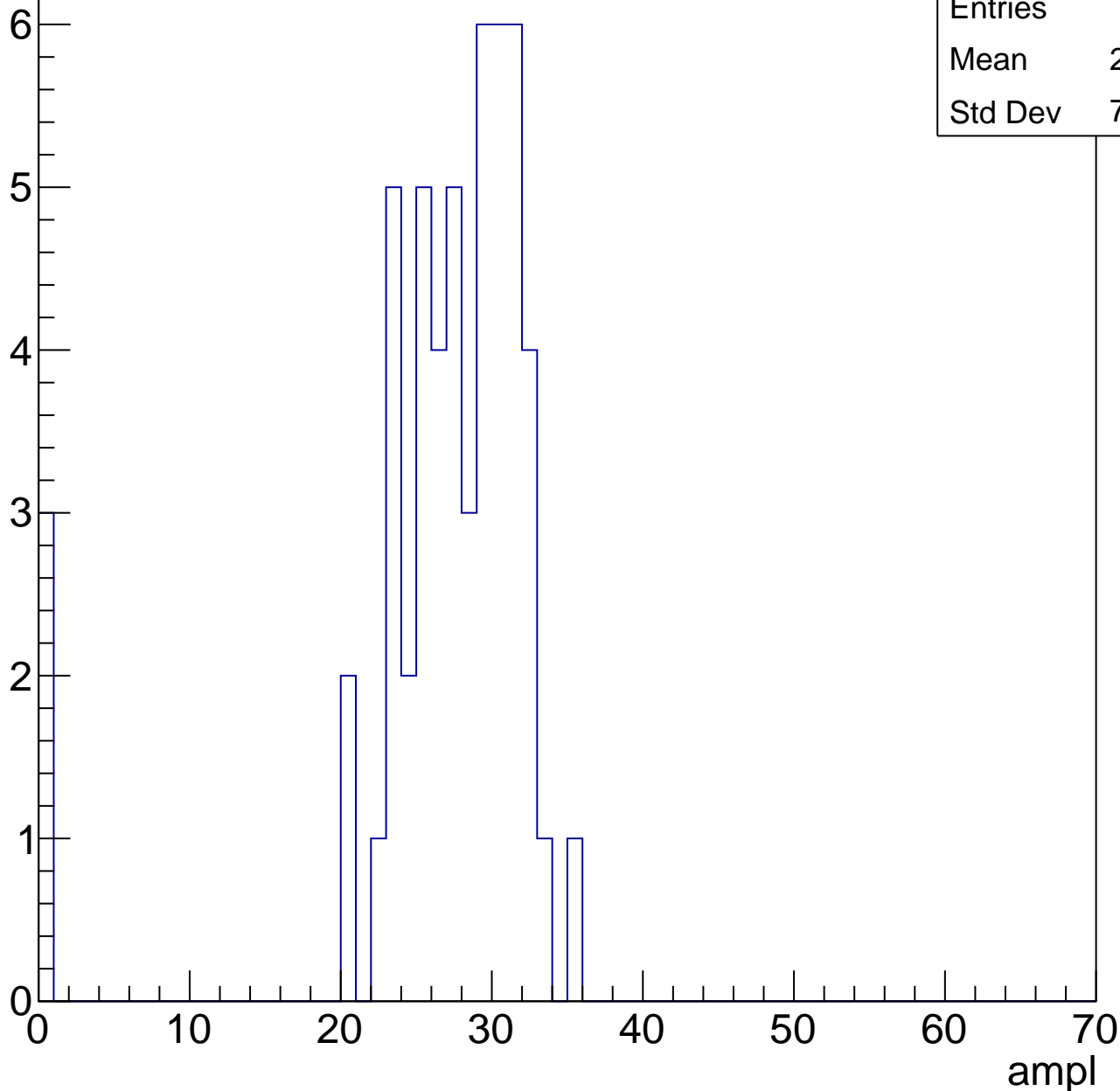
Entries	19
Mean	0
Std Dev	0

# B1L103S, U25-ch2, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	54
Mean	26.09
Std Dev	7.155

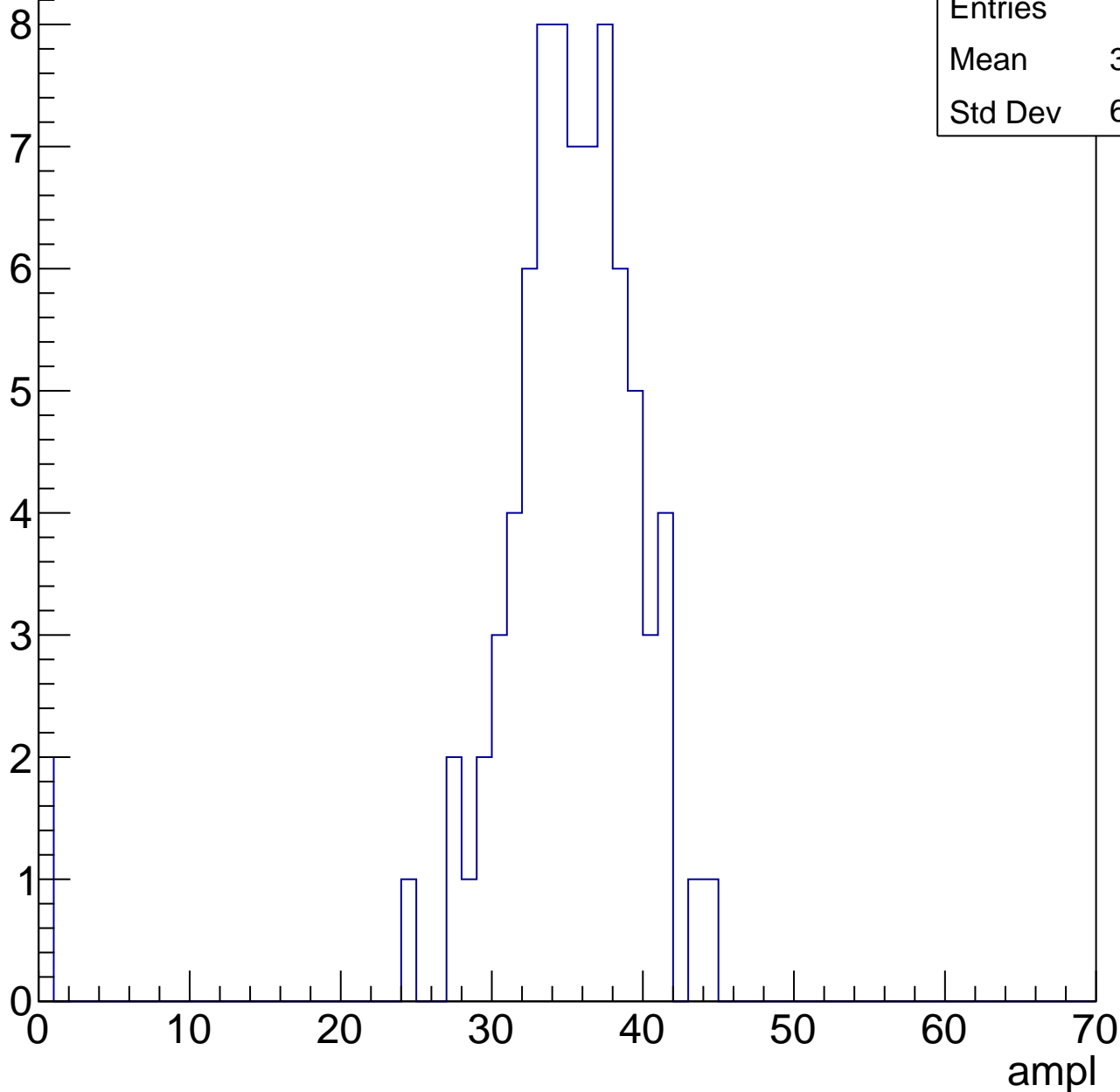


# B1L103S, U25-ch2, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	79
Mean	34.09
Std Dev	6.679

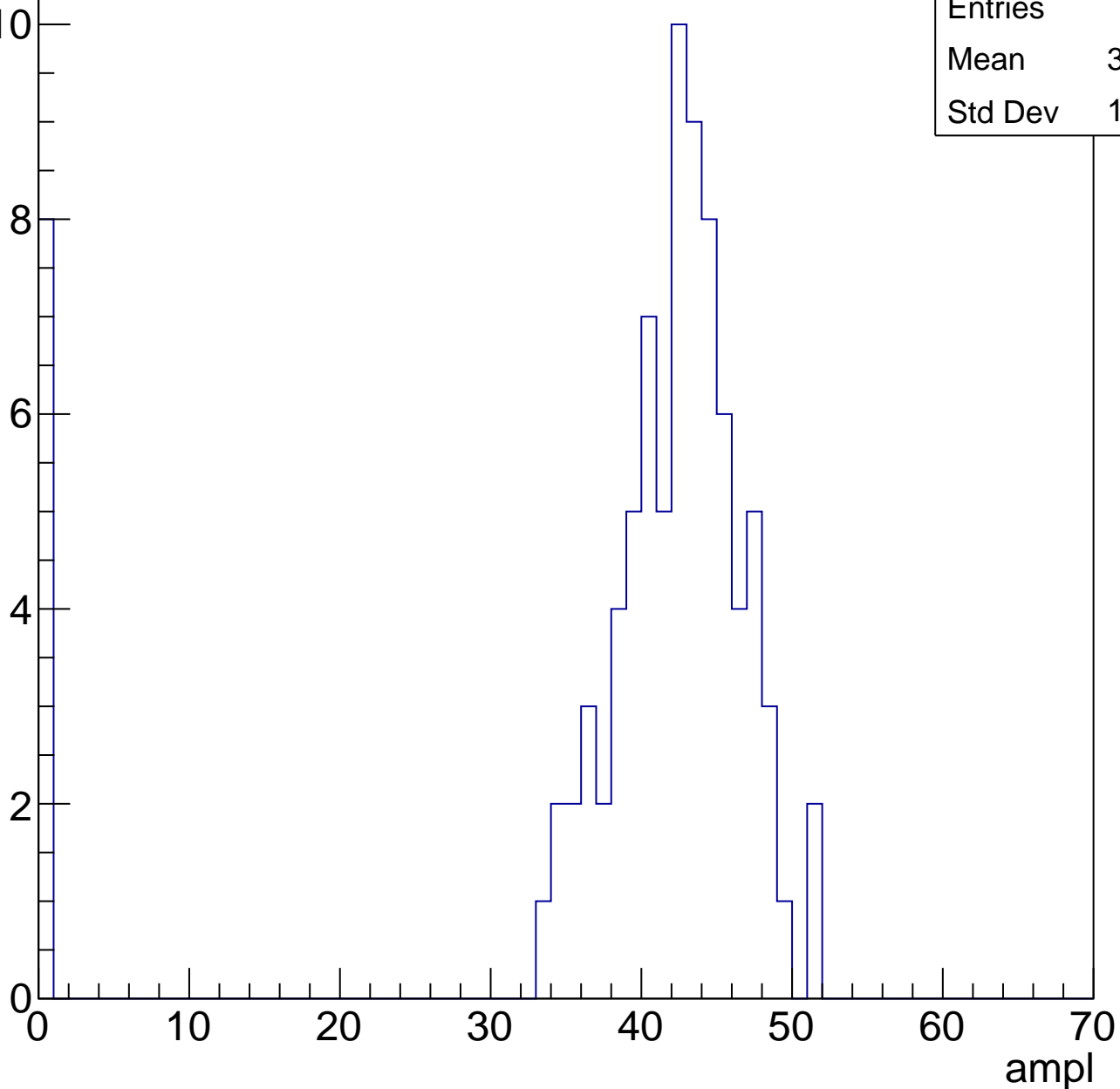


# B1L103S, U25-ch2, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

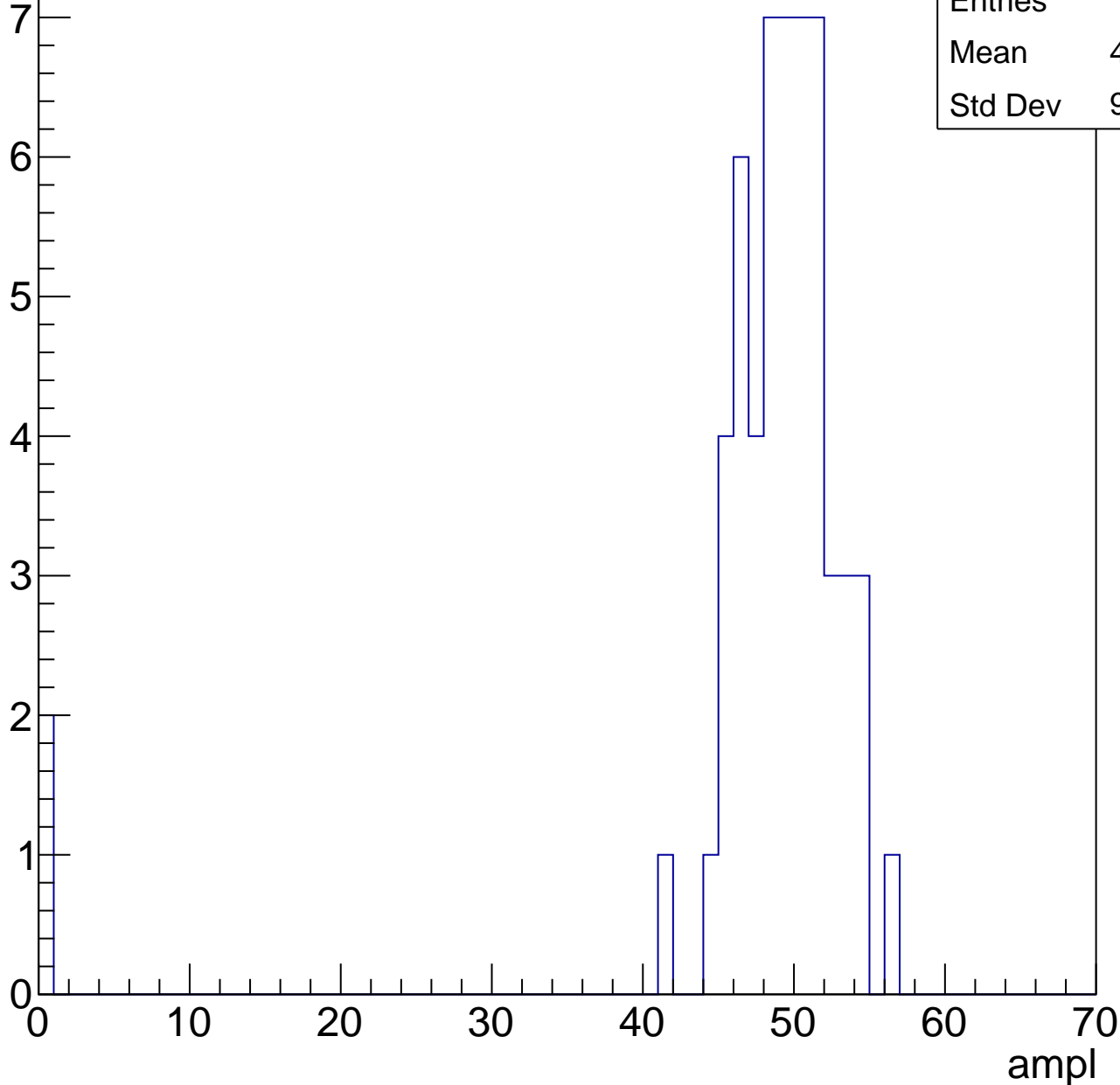
Entries	87
Mean	38.25
Std Dev	12.73



# B1L103S, U25-ch2, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

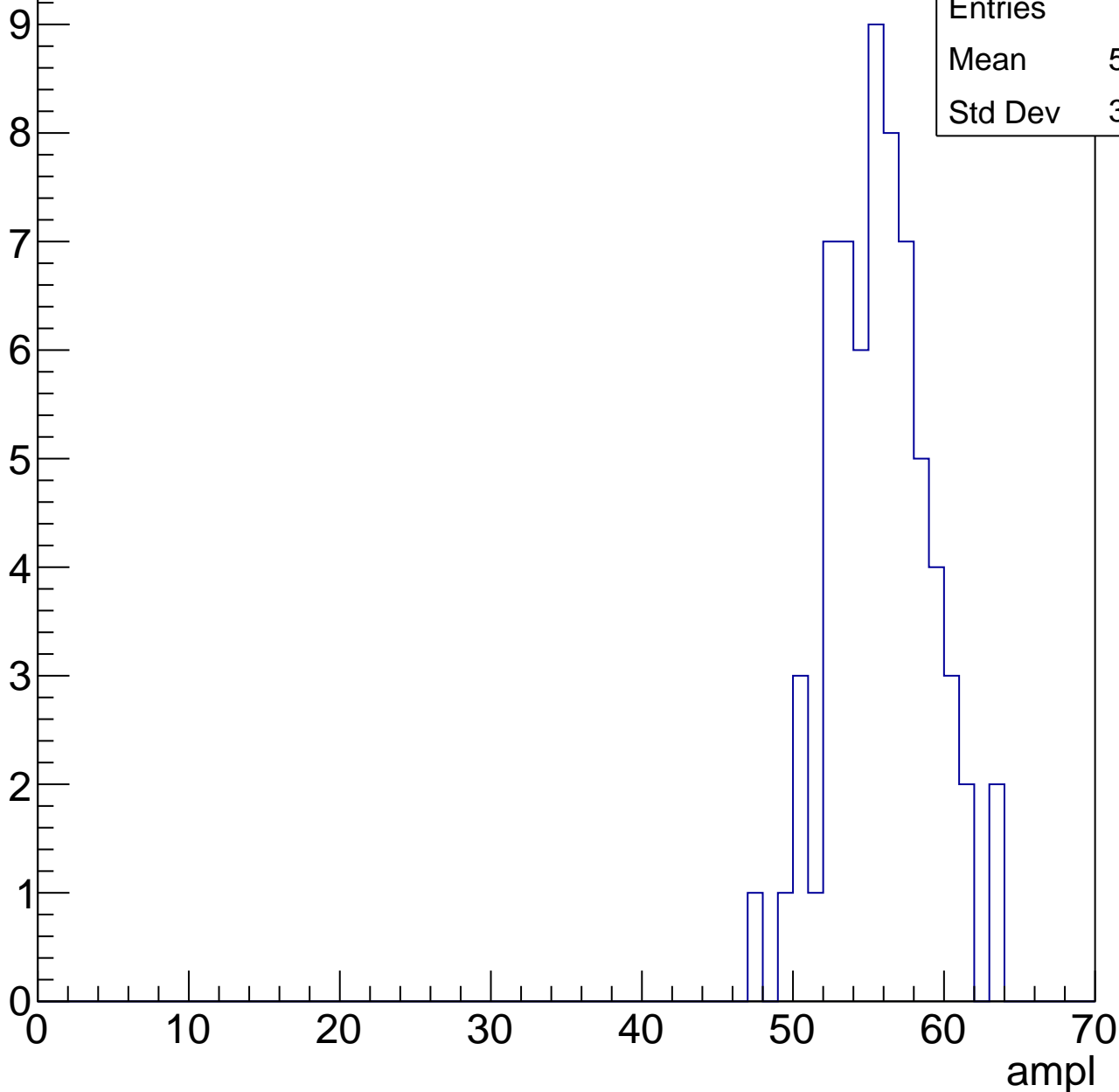


# B1L103S, U25-ch2, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	66
Mean	55.33
Std Dev	3.258

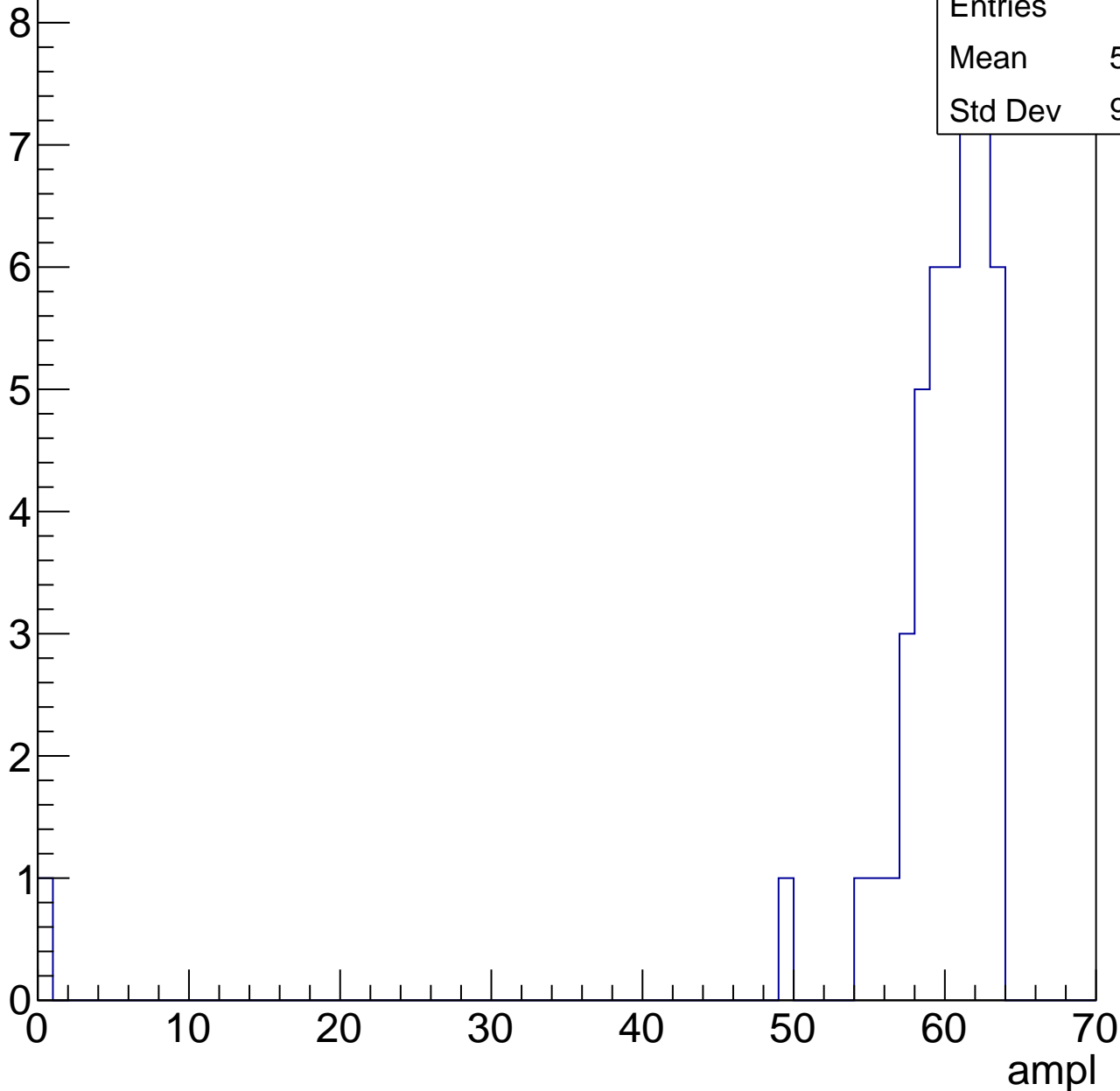


# B1L103S, U25-ch2, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	47
Mean	58.53
Std Dev	9.043



# B1L103S, U25-ch2, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

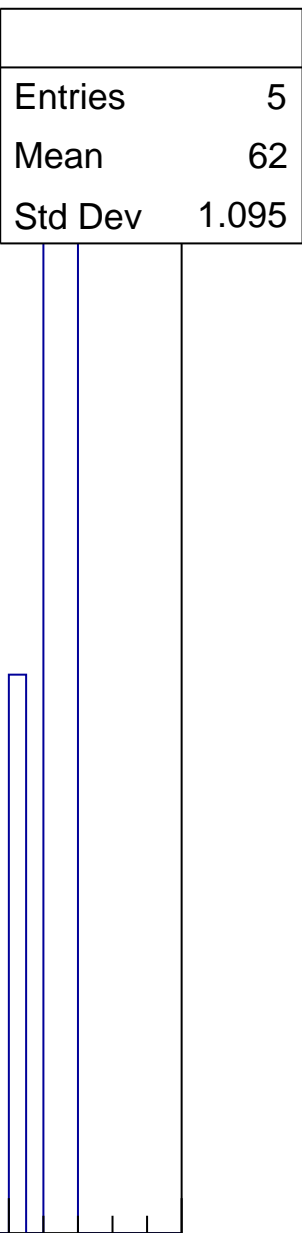
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	62
Std Dev	1.095

0 10 20 30 40 50 60 70

ampl





# B1L103S, U25-ch2, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

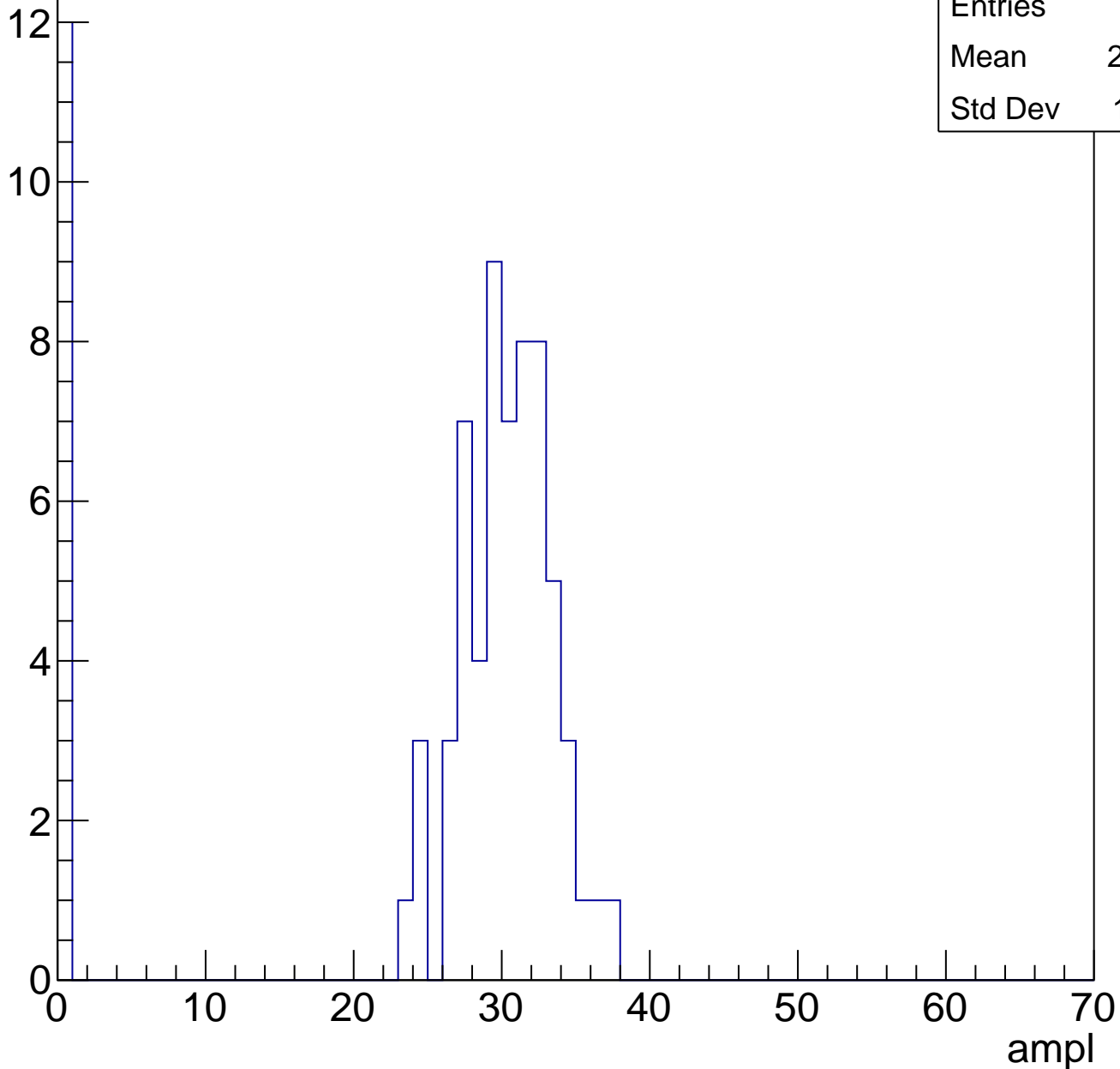


# B1L103S, U25-ch3, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	73
Mean	24.99
Std Dev	11.41

Entry



# B1L103S, U25-ch3, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	92
Mean	32.88
Std Dev	12.52

Entry

10

8

6

4

2

0

0

10

20

30

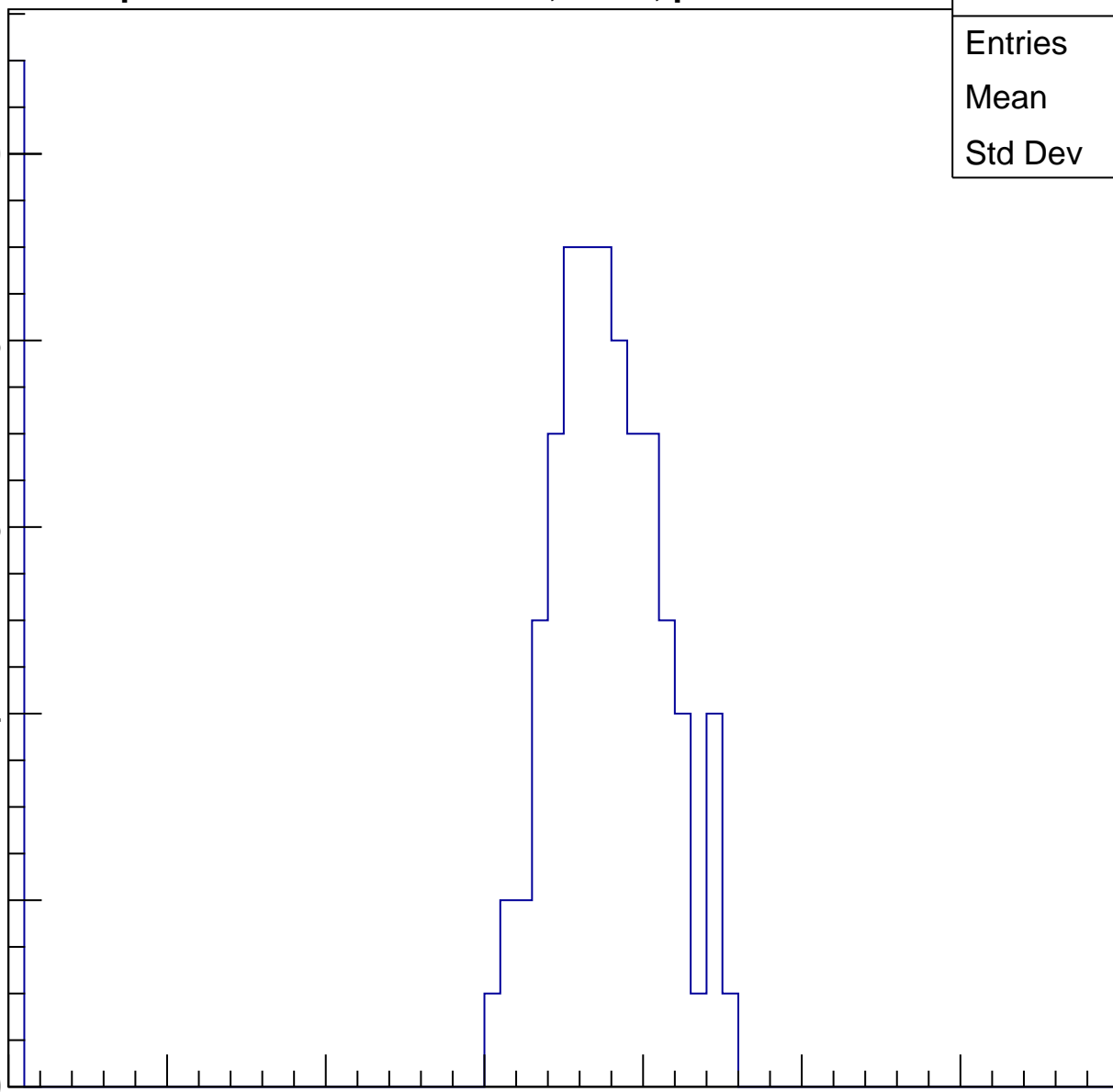
40

50

60

70

ampl

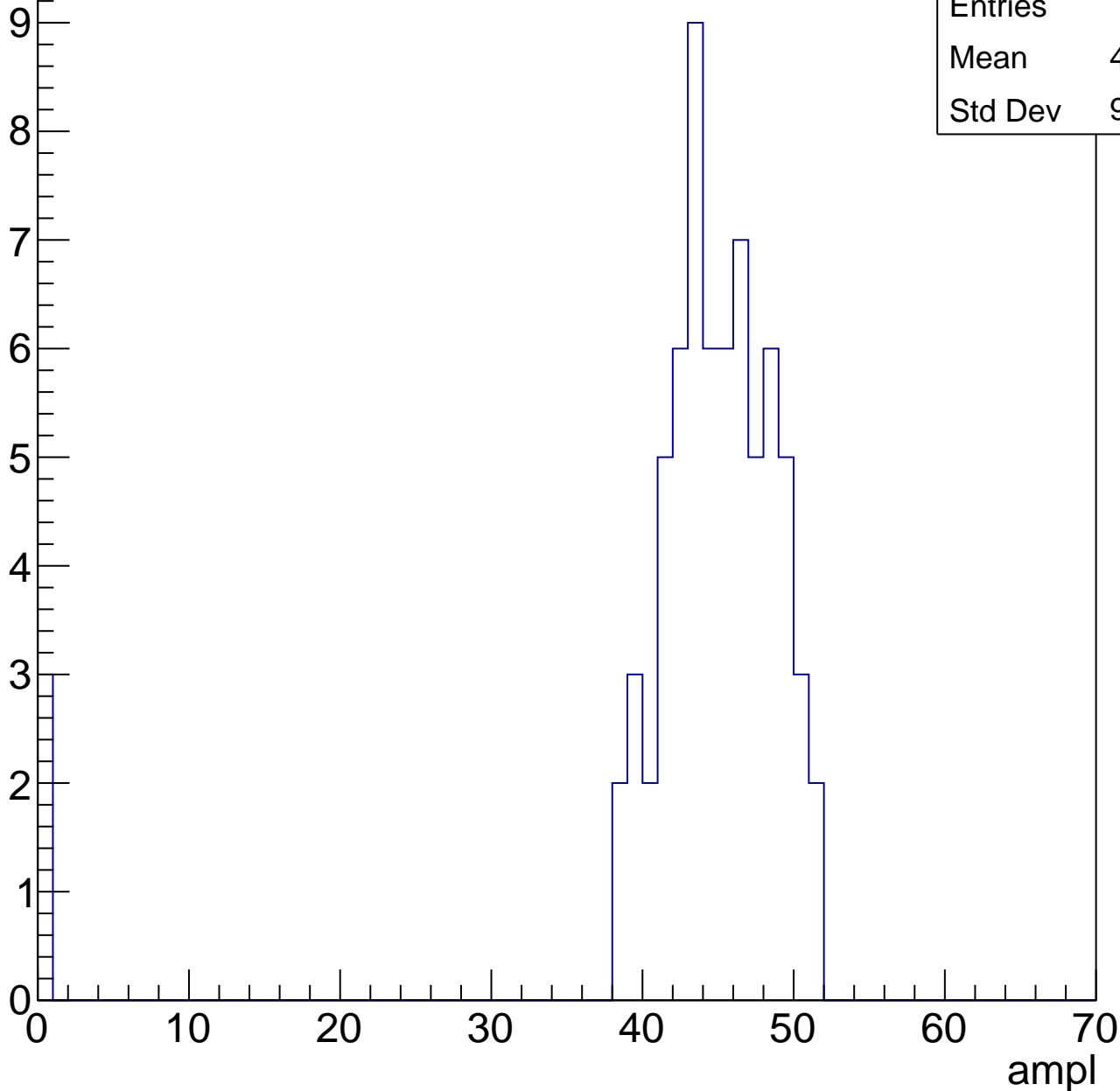


# B1L103S, U25-ch3, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

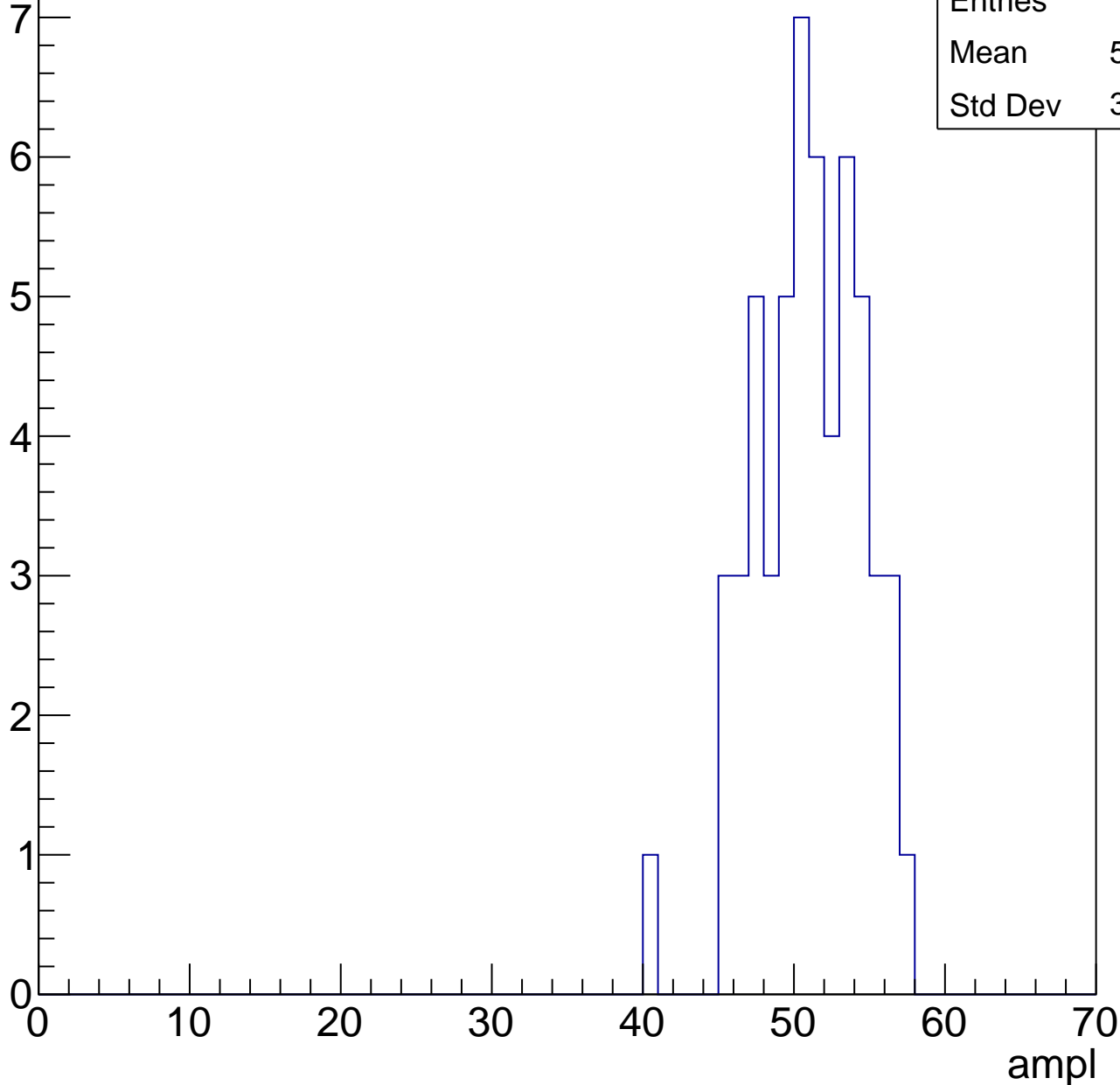
Entries	70
Mean	42.76
Std Dev	9.609



# B1L103S, U25-ch3, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



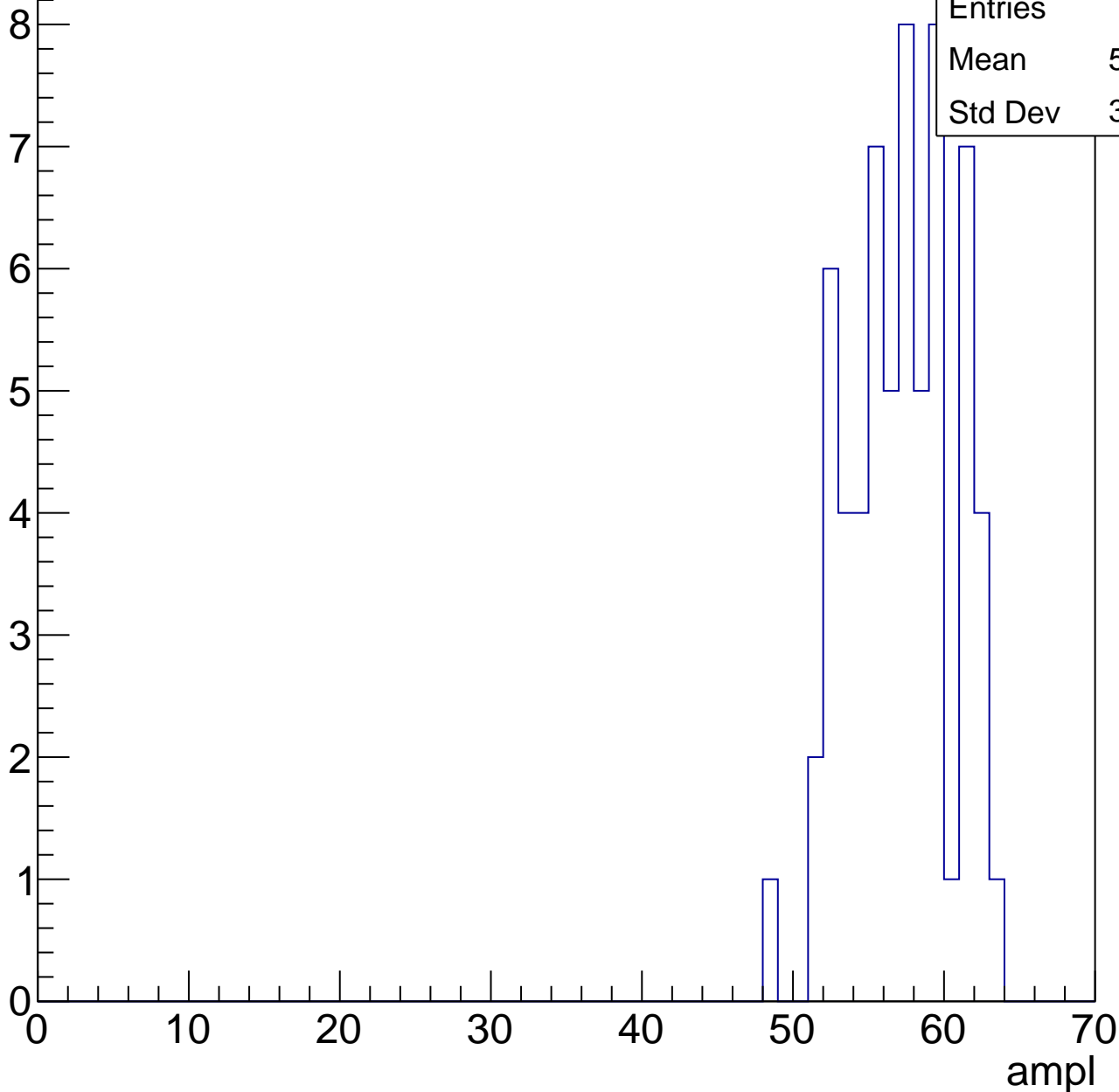
Entries	55
Mean	50.53
Std Dev	3.458

# B1L103S, U25-ch3, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

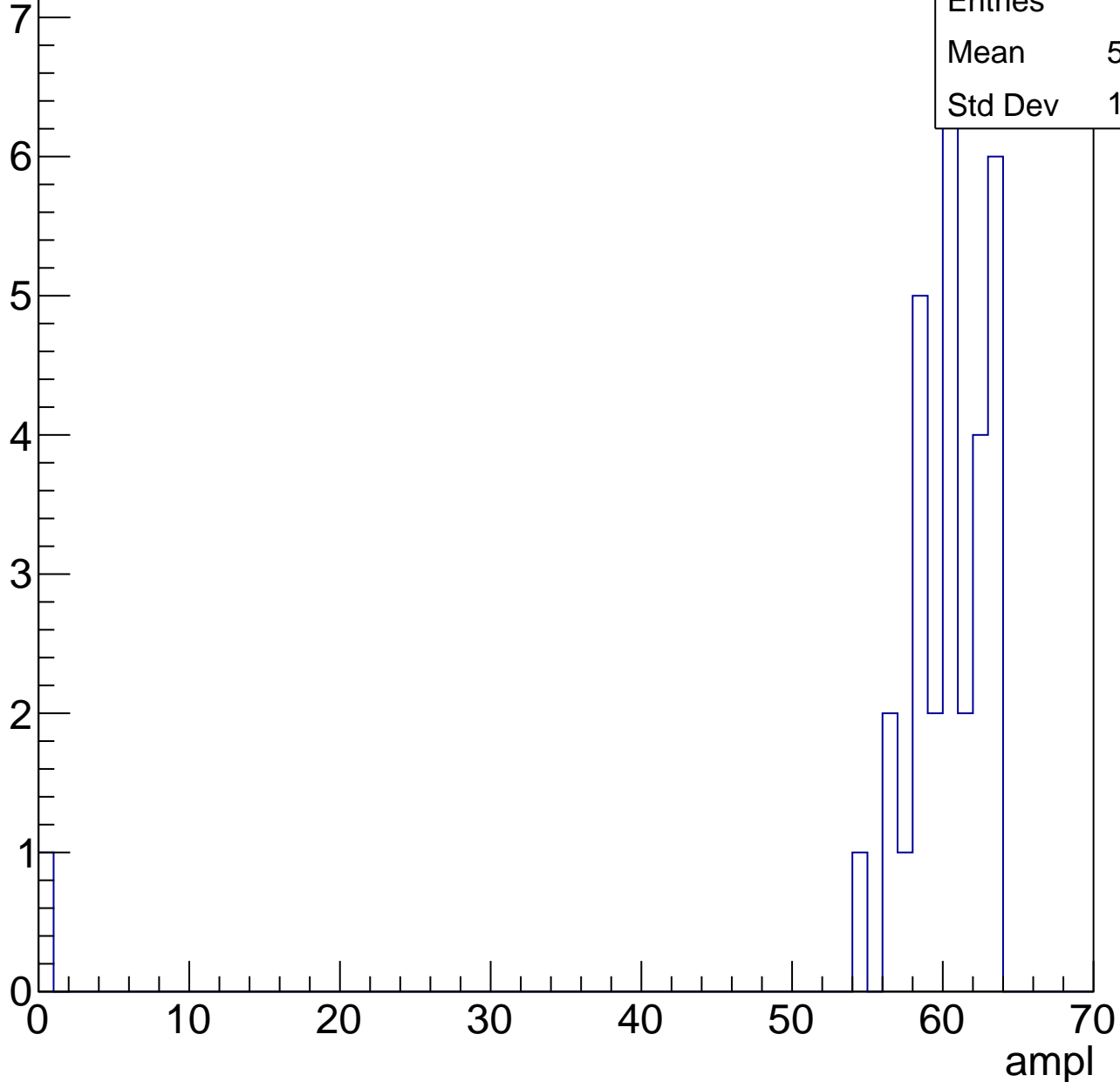
Entries	63
Mean	56.68
Std Dev	3.389



# B1L103S, U25-ch3, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

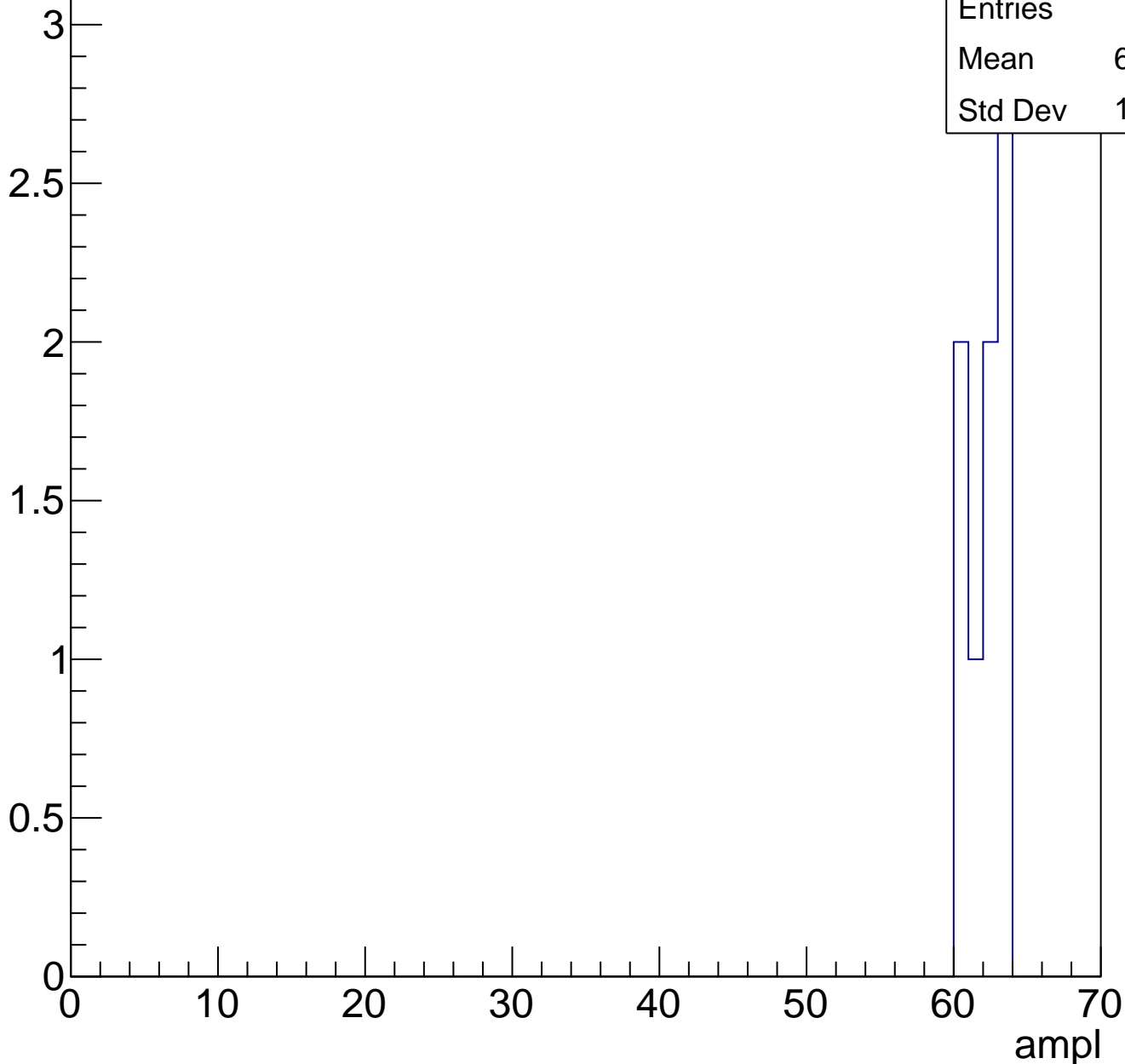
Entry



# B1L103S, U25-ch3, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U25-ch3, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U25-ch4, adc0

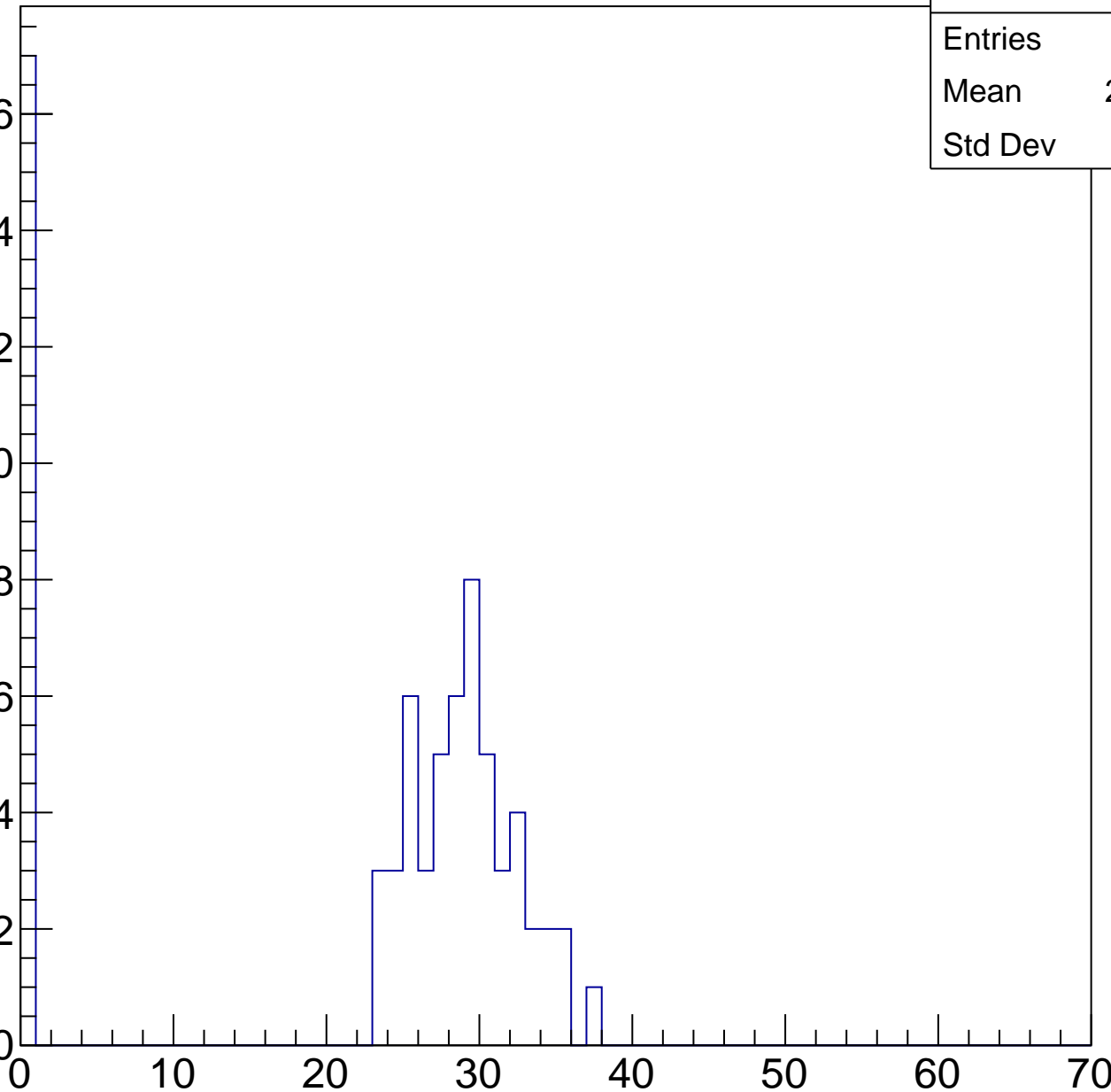
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	70
Mean	21.66
Std Dev	12.61

Entry

16  
14  
12  
10  
8  
6  
4  
2  
0

ampl

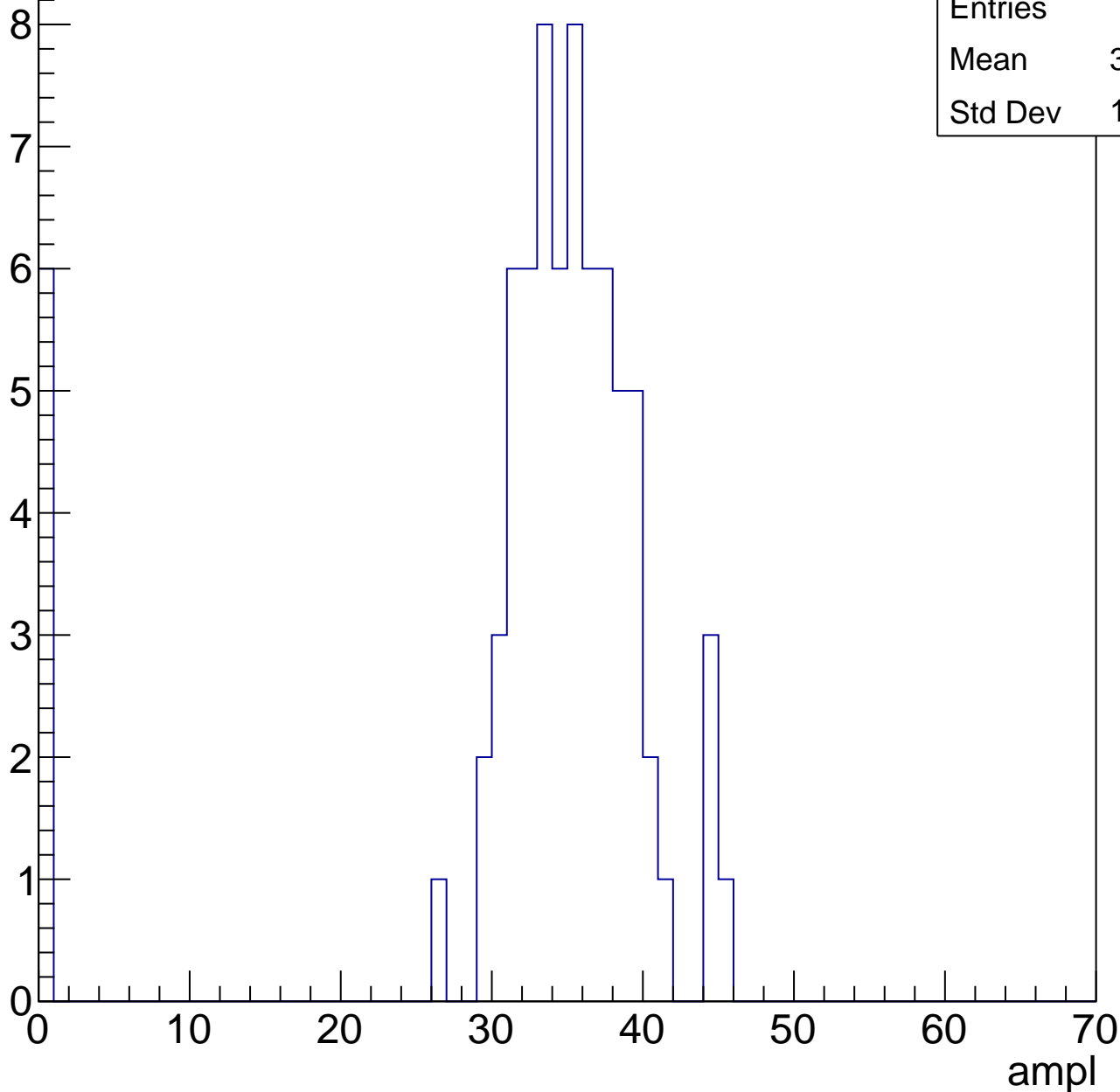


# B1L103S, U25-ch4, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	75
Mean	32.28
Std Dev	10.19



# B1L103S, U25-ch4, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	102
Mean	38.05
Std Dev	13.73

Entry

10

8

6

4

2

0

0

10

20

30

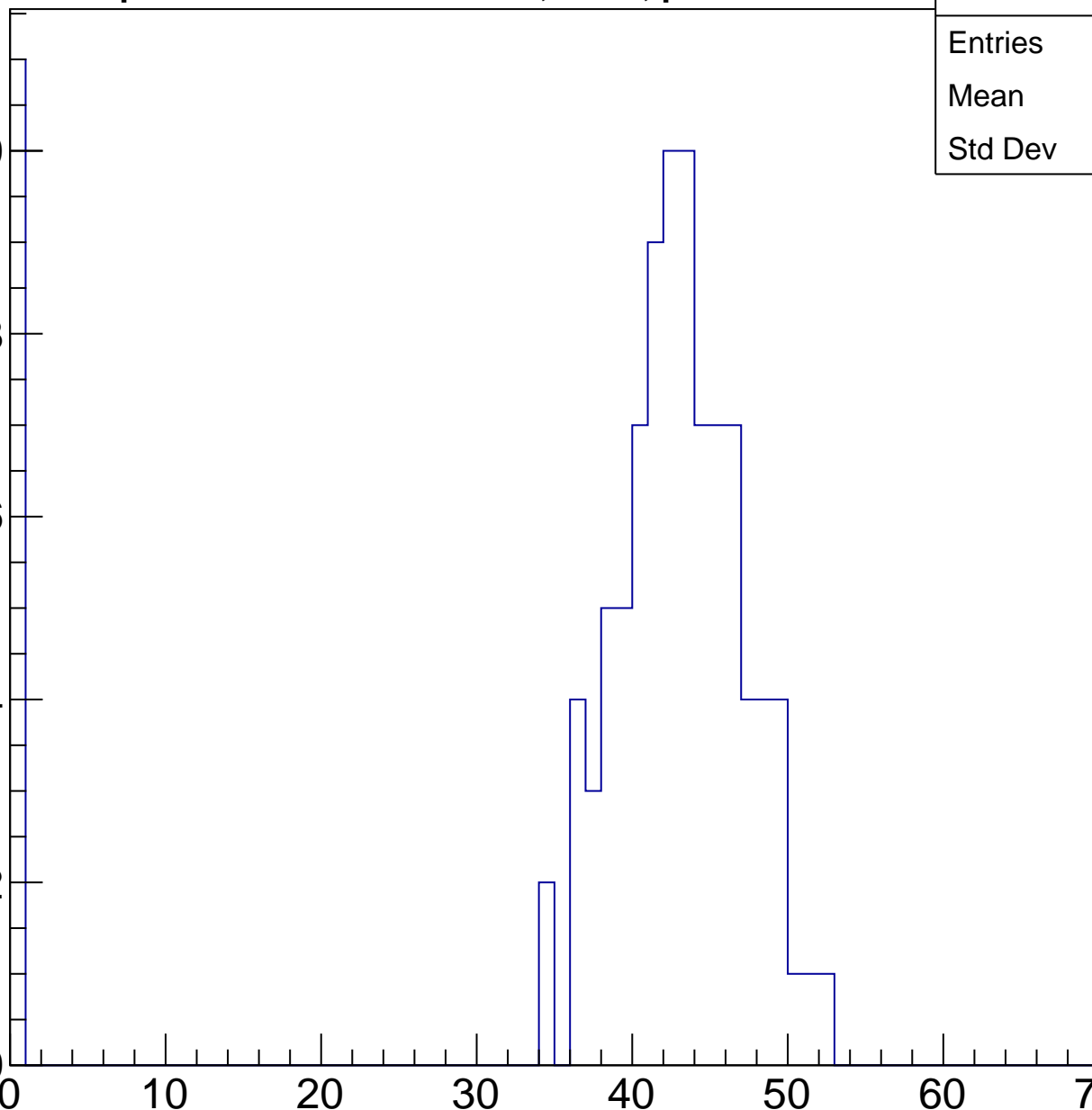
40

50

60

70

ampl

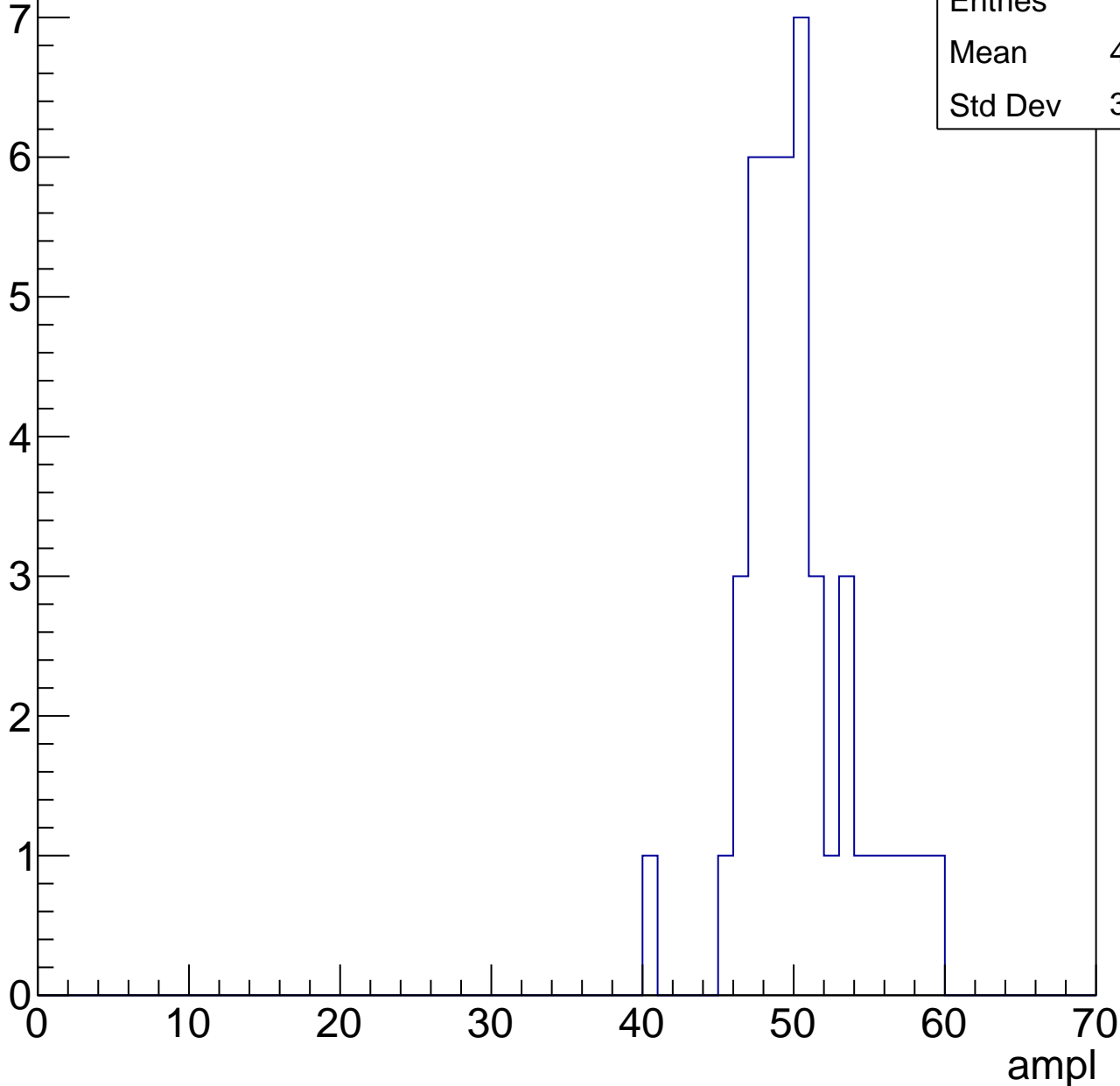


# B1L103S, U25-ch4, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	43
Mean	49.77
Std Dev	3.608

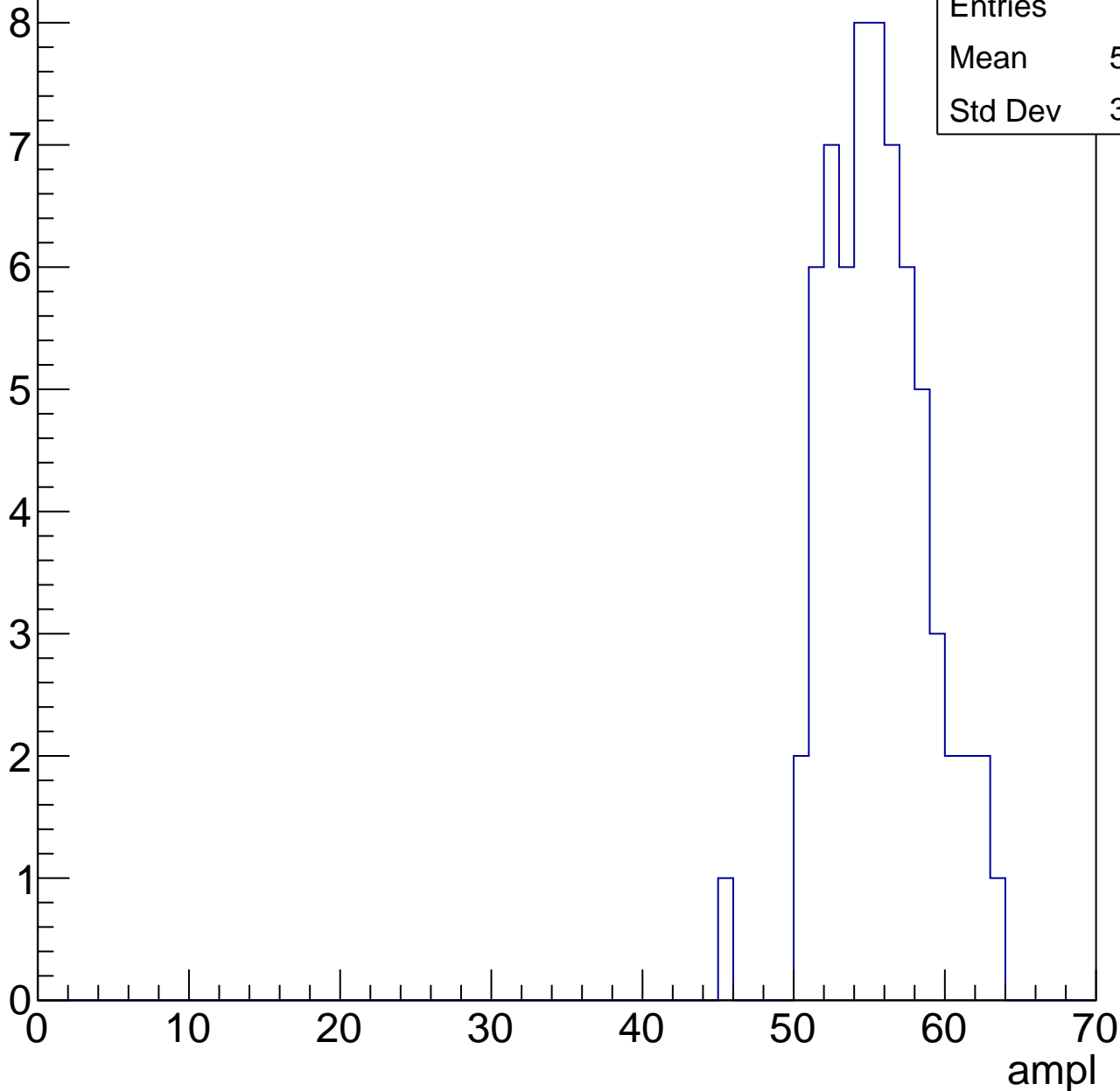


# B1L103S, U25-ch4, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	66
Mean	55.08
Std Dev	3.368

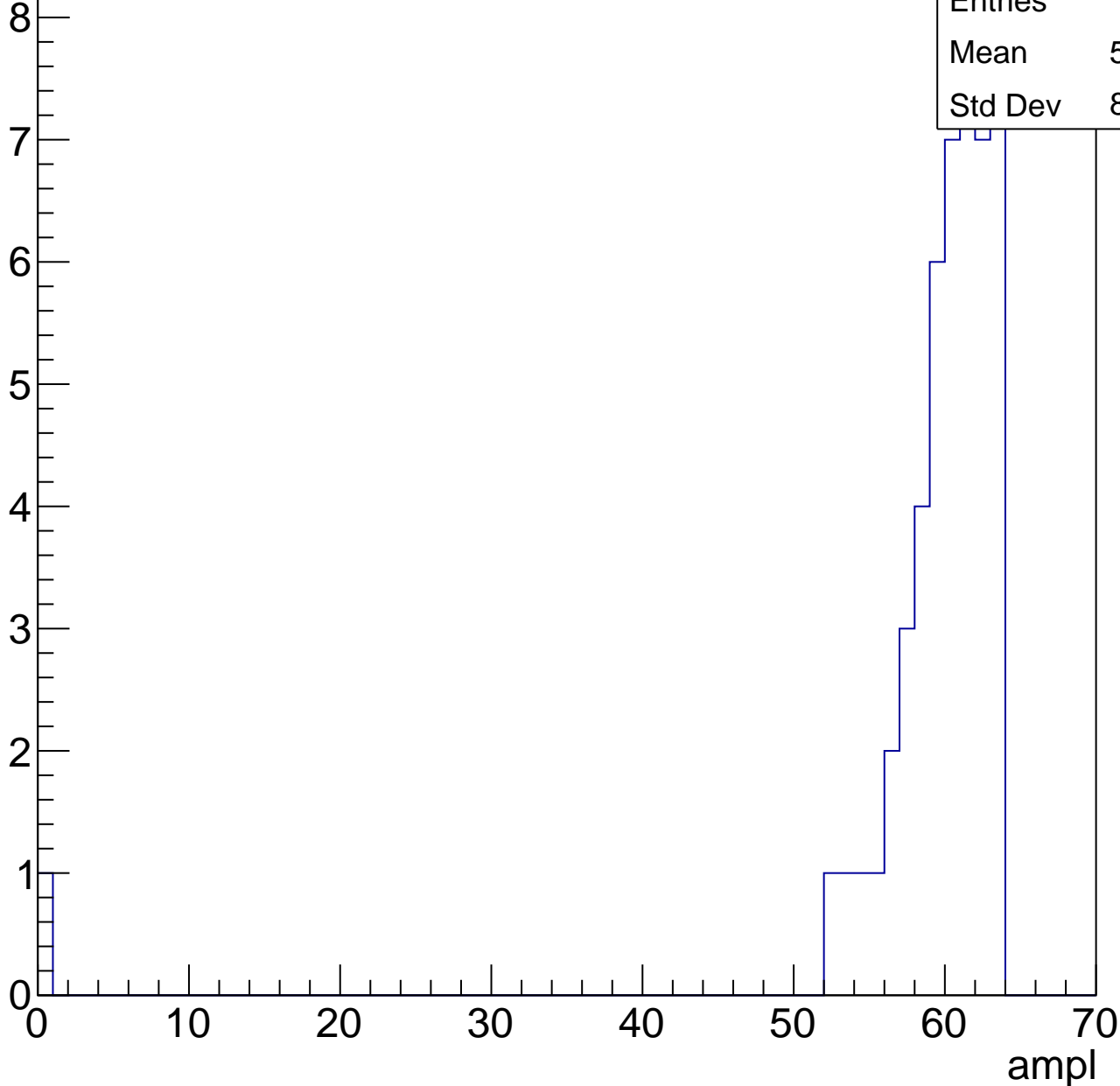


# B1L103S, U25-ch4, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	50
Mean	58.58
Std Dev	8.789



# B1L103S, U25-ch4, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U25-ch4, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

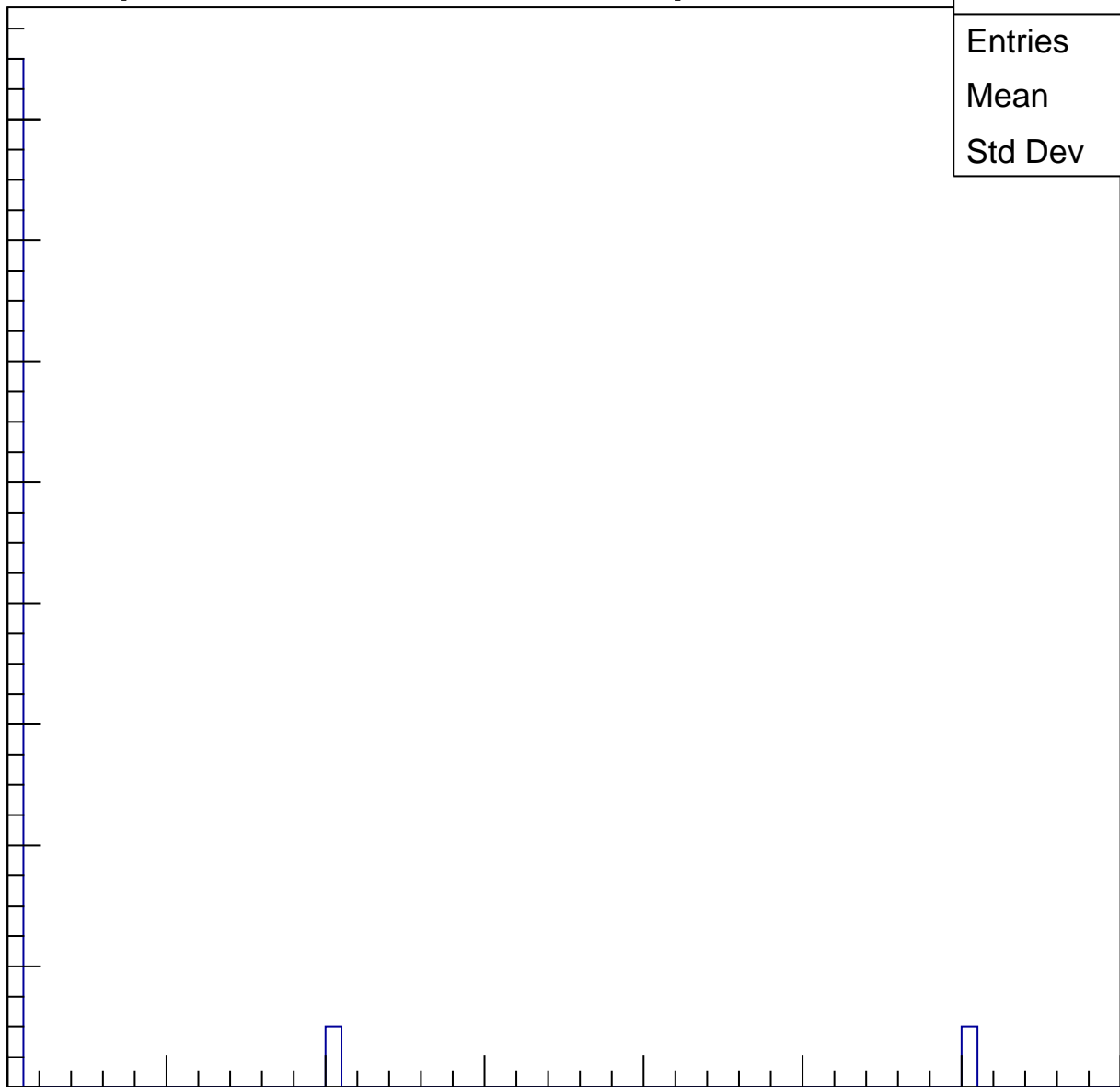
Entries	19
Mean	4.211
Std Dev	13.89

Entry

16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

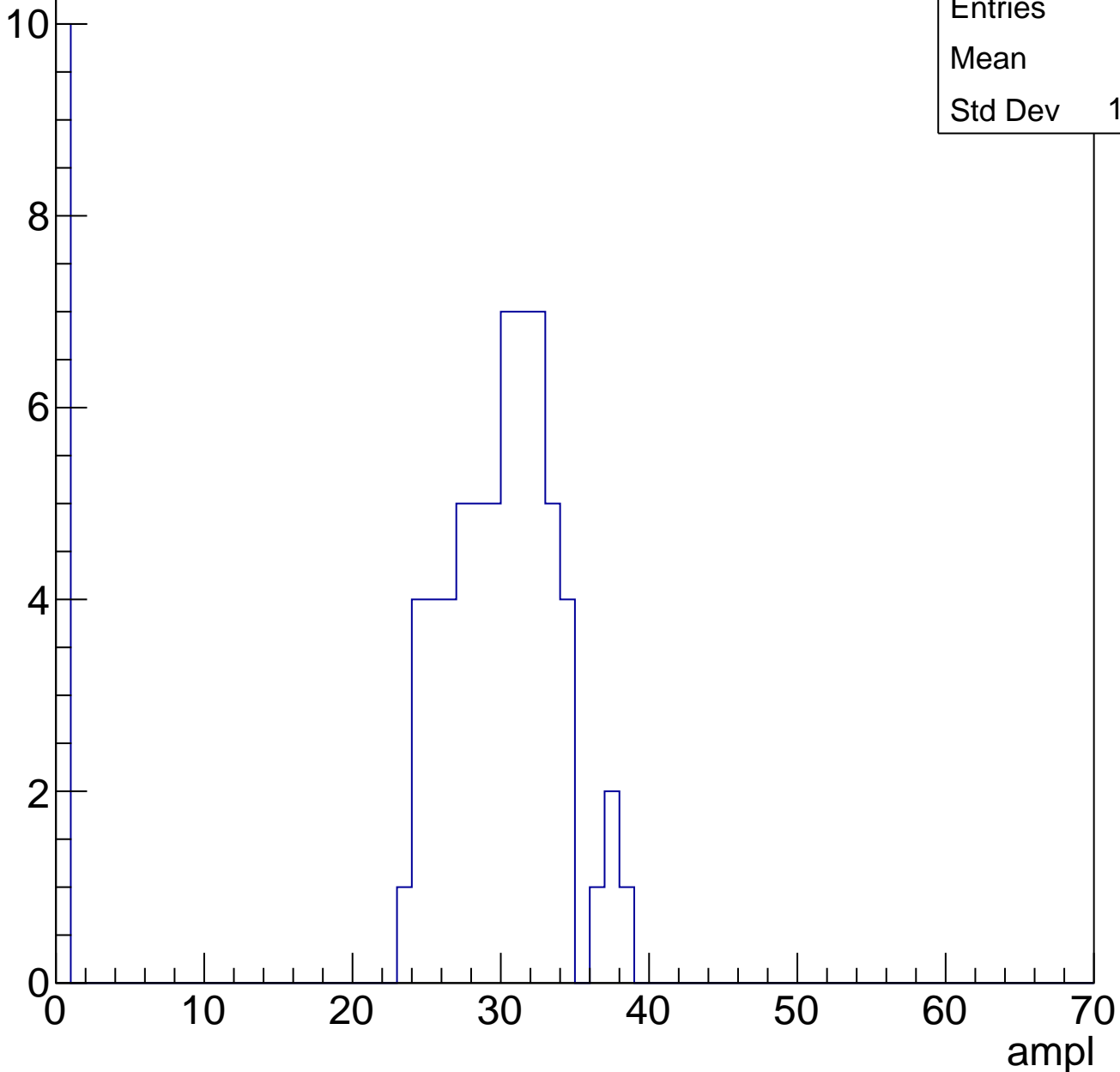


# B1L103S, U25-ch5, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	72
Mean	25.6
Std Dev	10.78

Entry



# B1L103S, U25-ch5, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

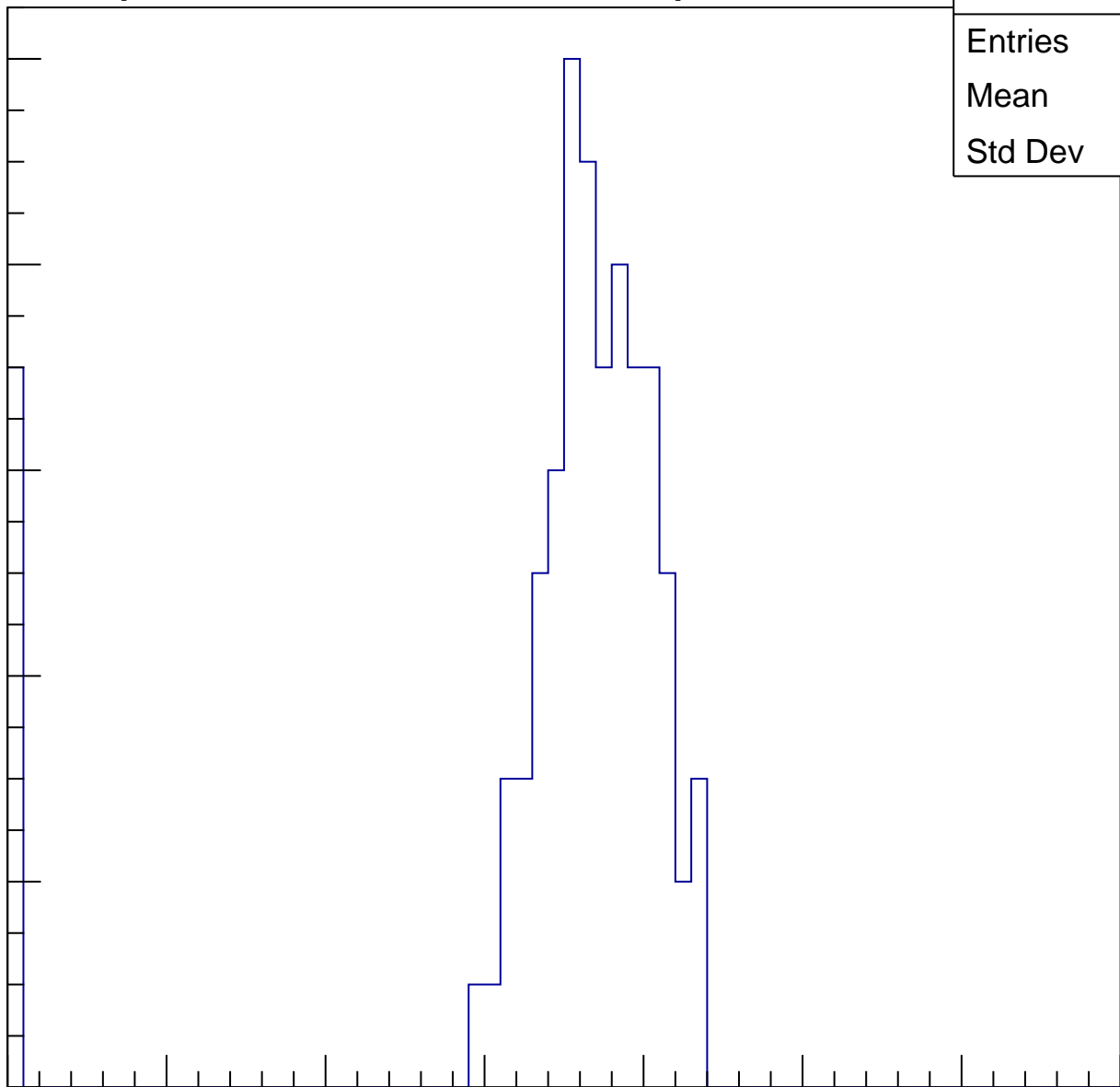
Entries	84
Mean	33.63
Std Dev	10.6

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

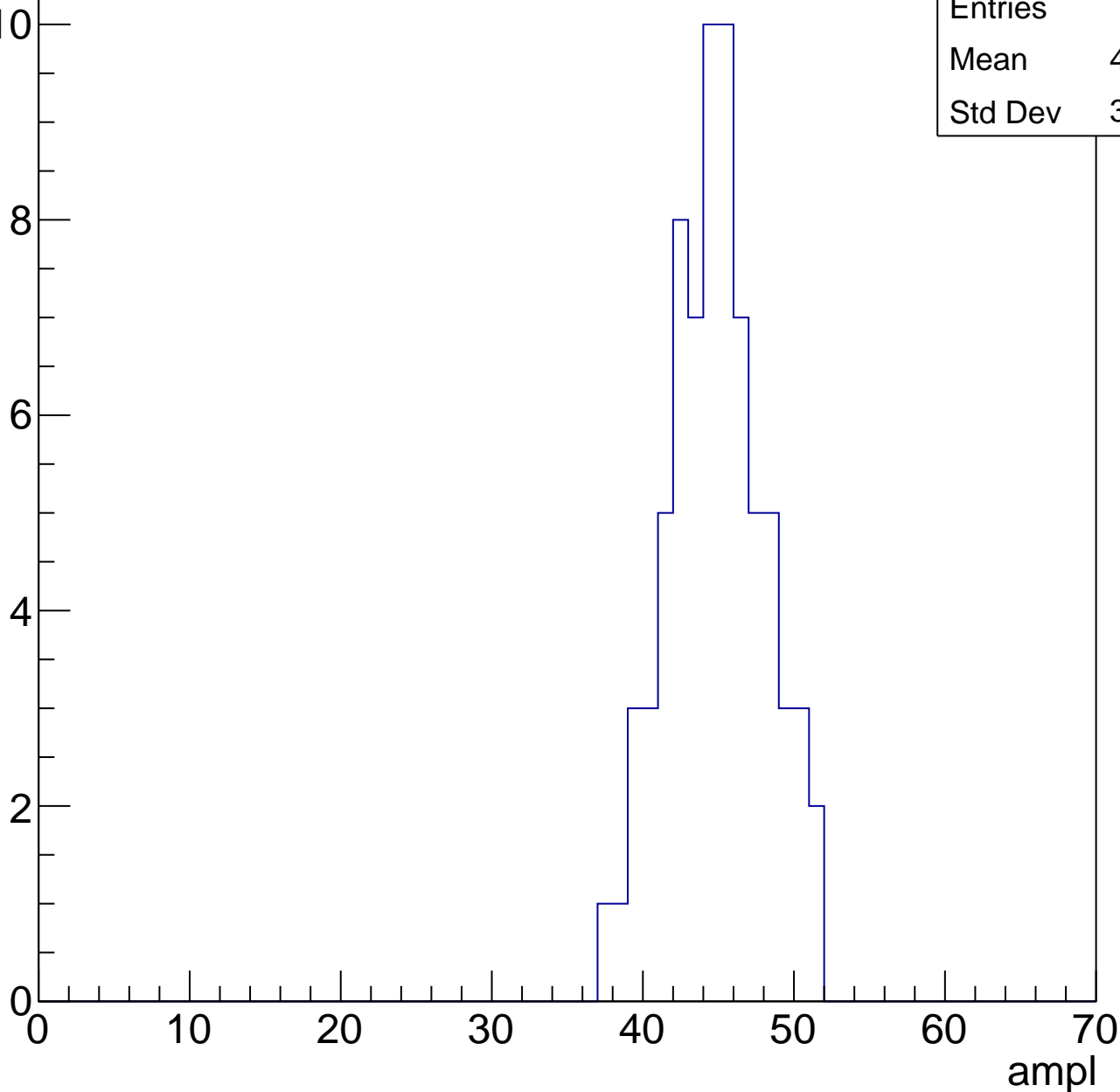


# B1L103S, U25-ch5, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	73
Mean	44.38
Std Dev	3.152

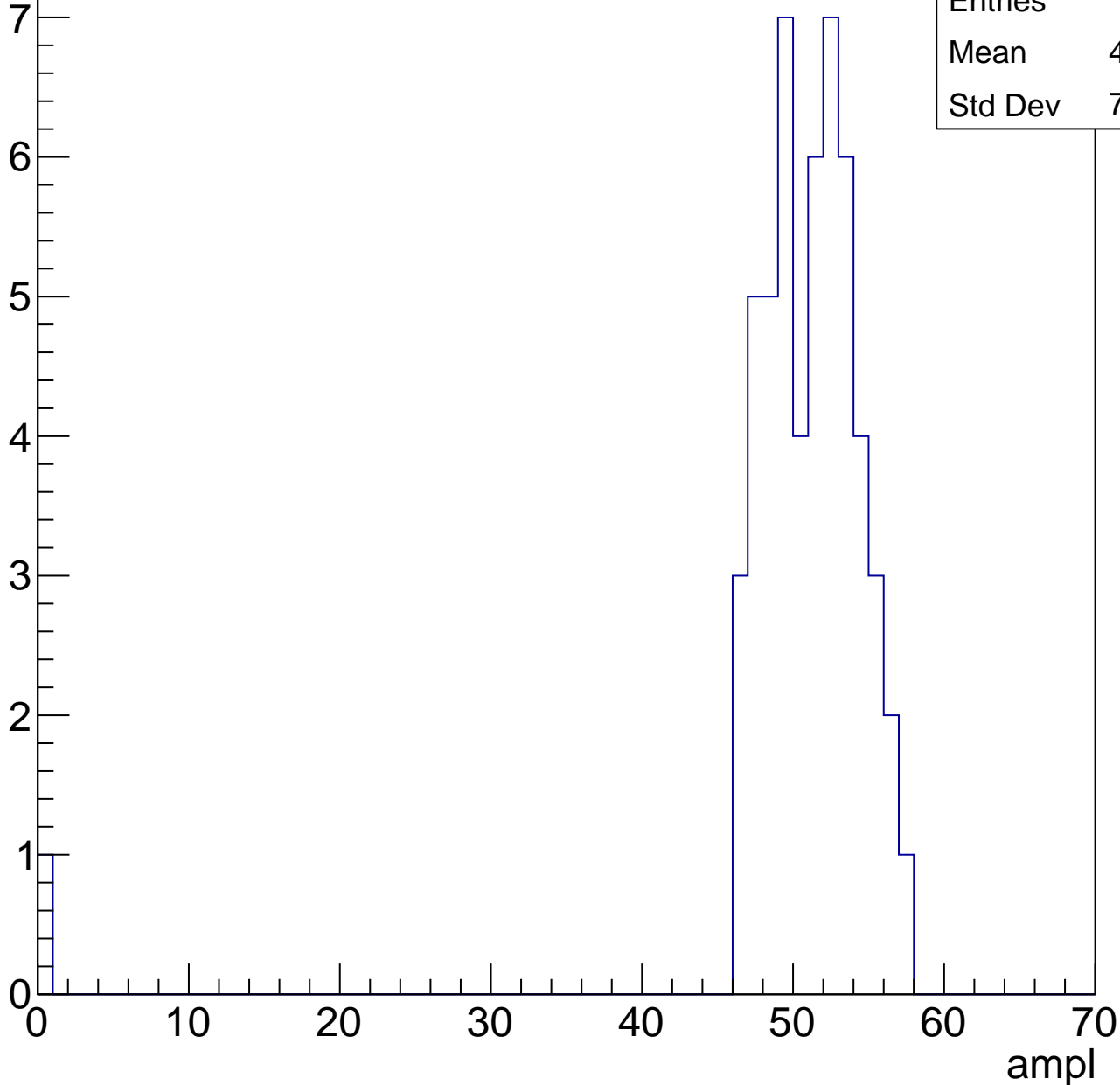


# B1L103S, U25-ch5, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	54
Mean	49.89
Std Dev	7.413

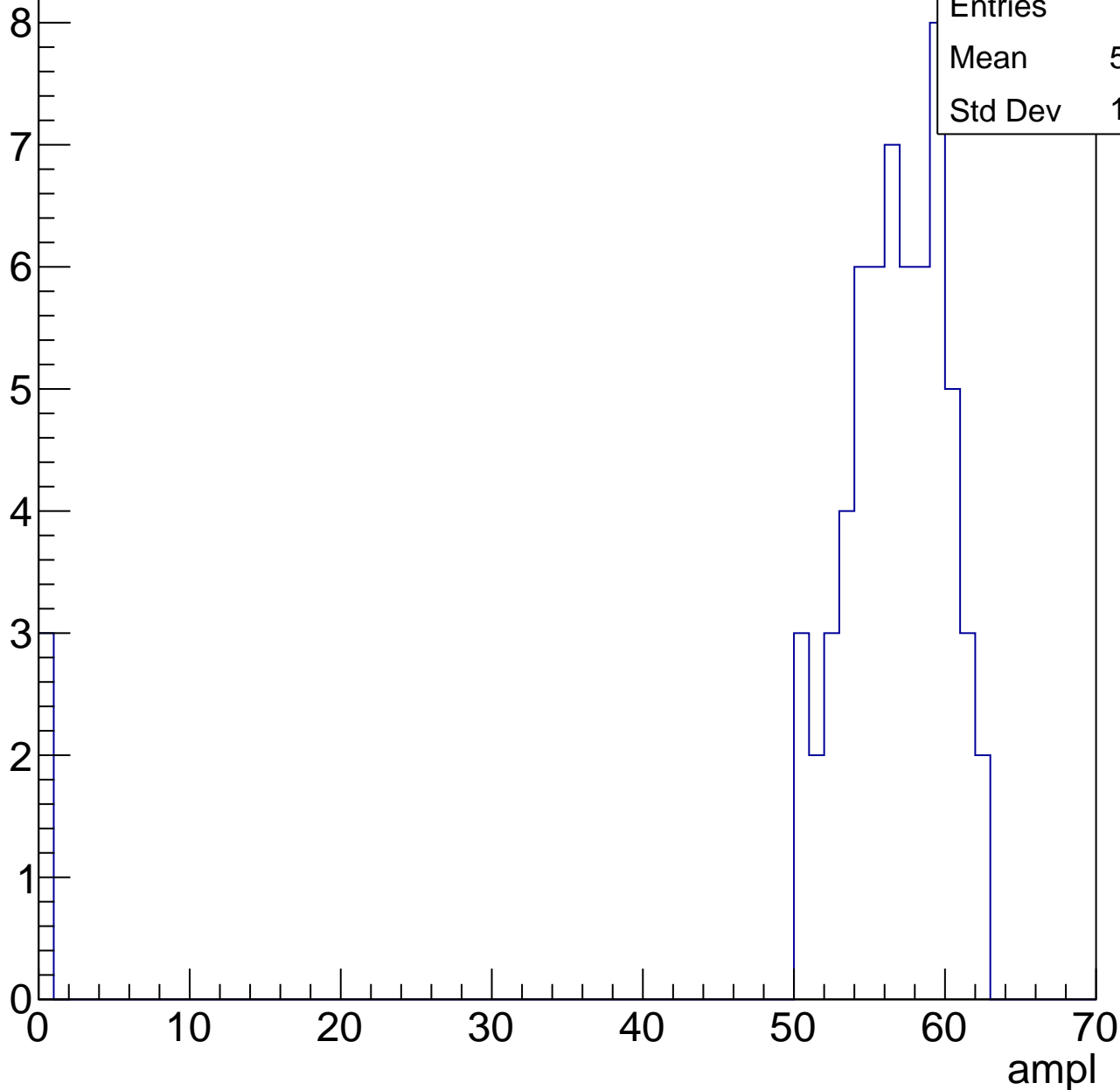


# B1L103S, U25-ch5, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	64
Mean	53.67
Std Dev	12.29



# B1L103S, U25-ch5, adc5

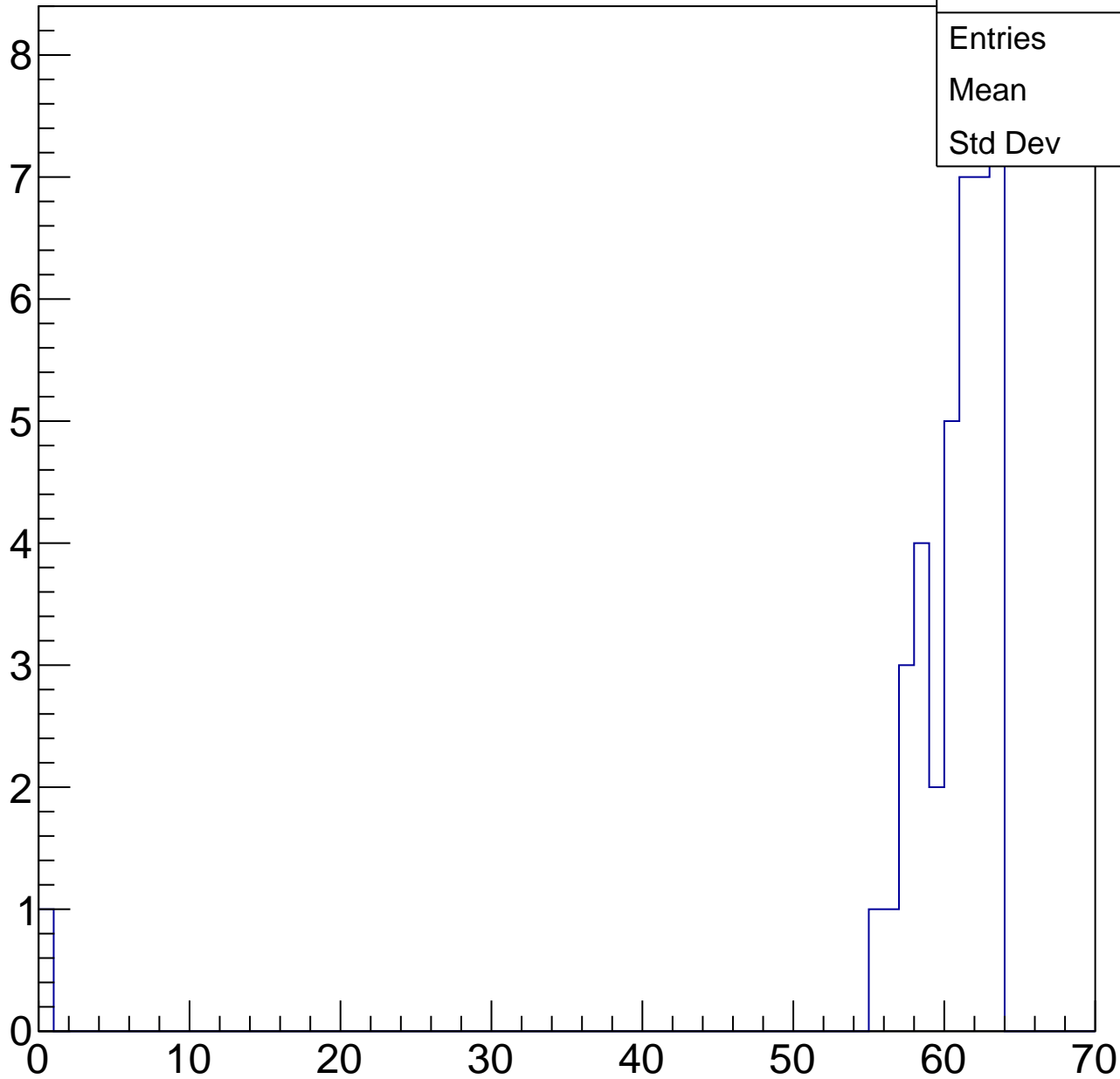
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	39
Mean	58.9
Std Dev	9.8

ampl



# B1L103S, U25-ch5, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.67
Std Dev	0.4714

ampl

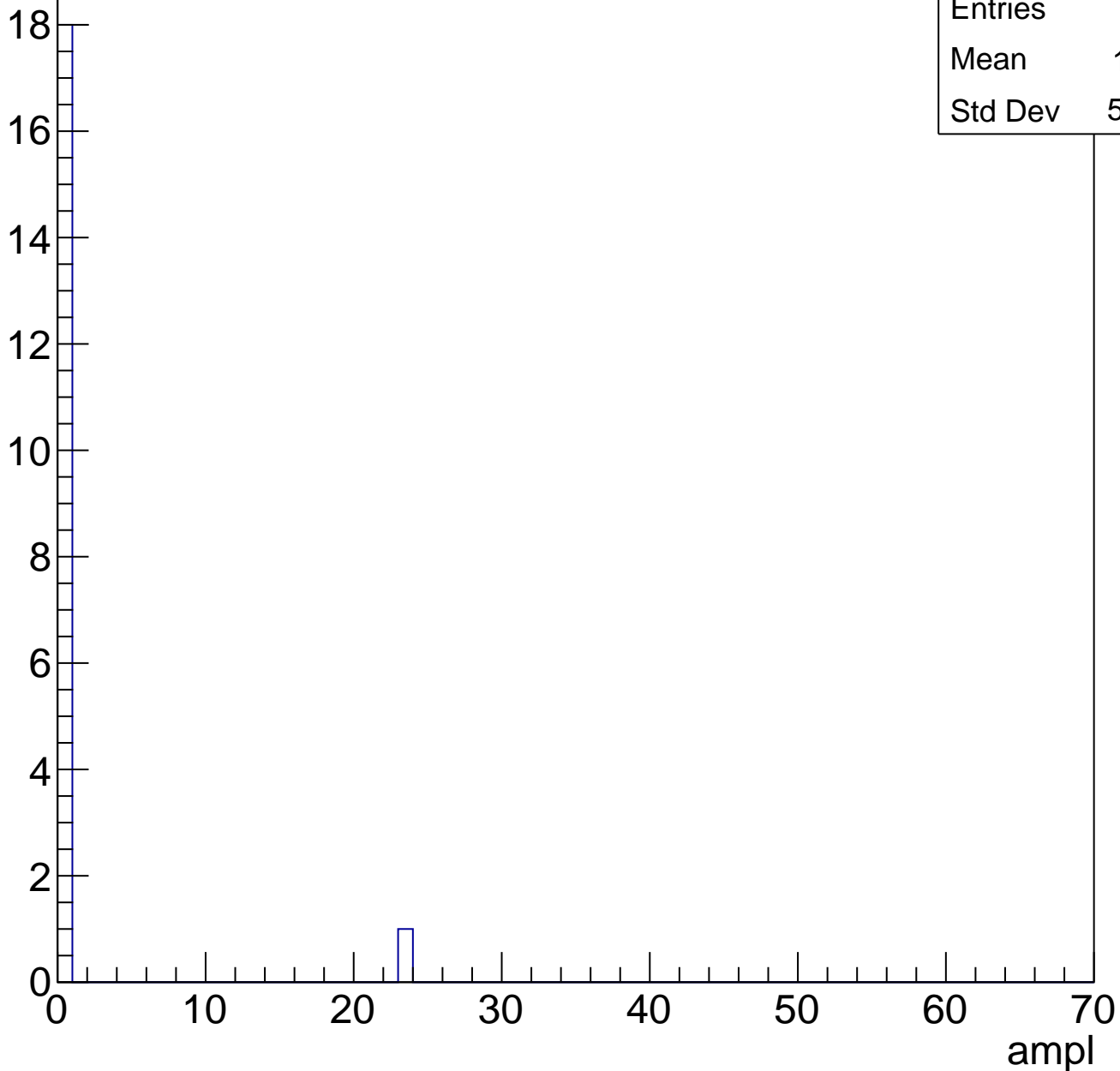
0 10 20 30 40 50 60 70



# B1L103S, U25-ch5, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U25-ch6, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

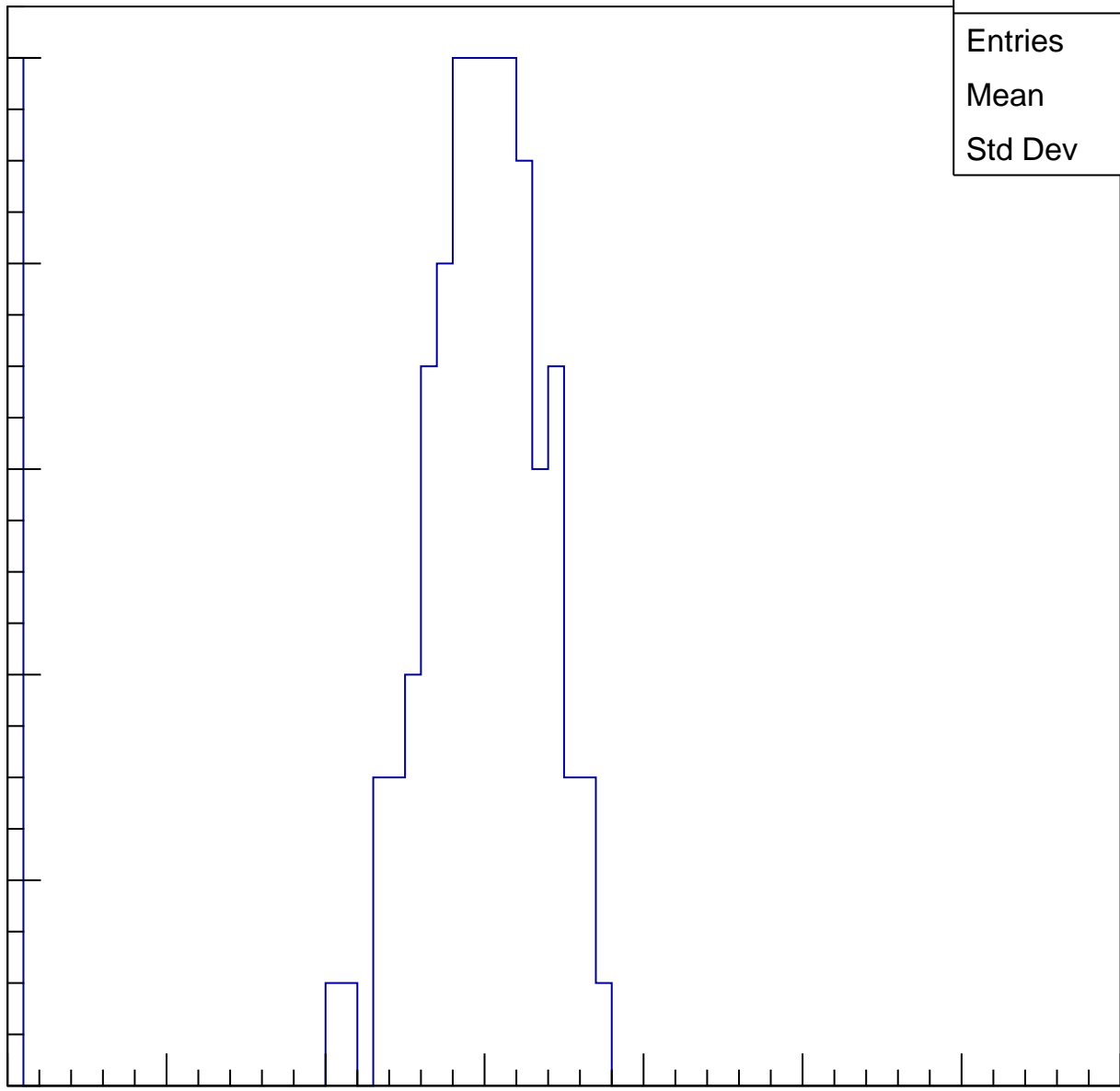
Entries	106
Mean	26.74
Std Dev	9.258

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

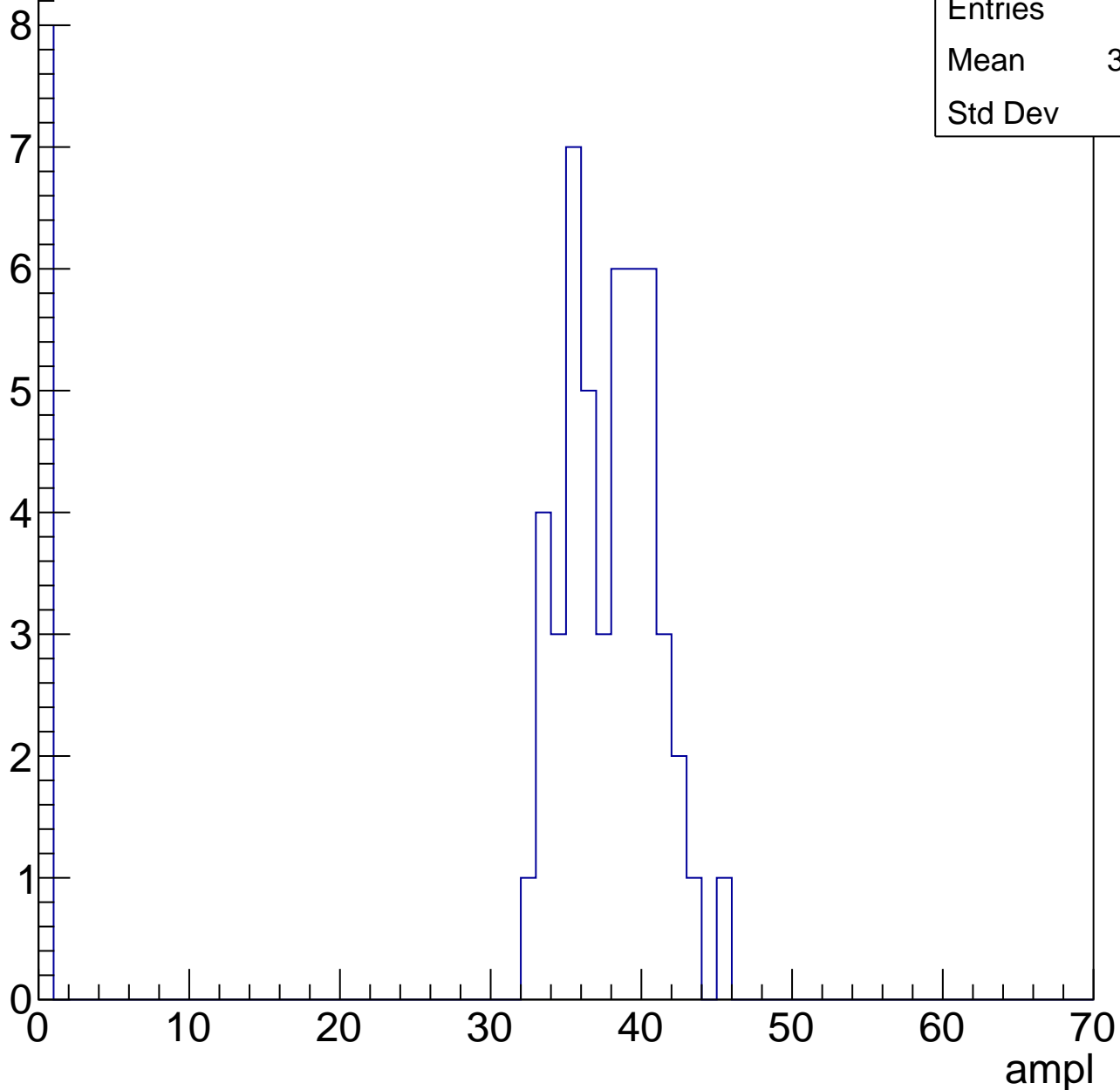


# B1L103S, U25-ch6, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	56
Mean	32.12
Std Dev	13.4

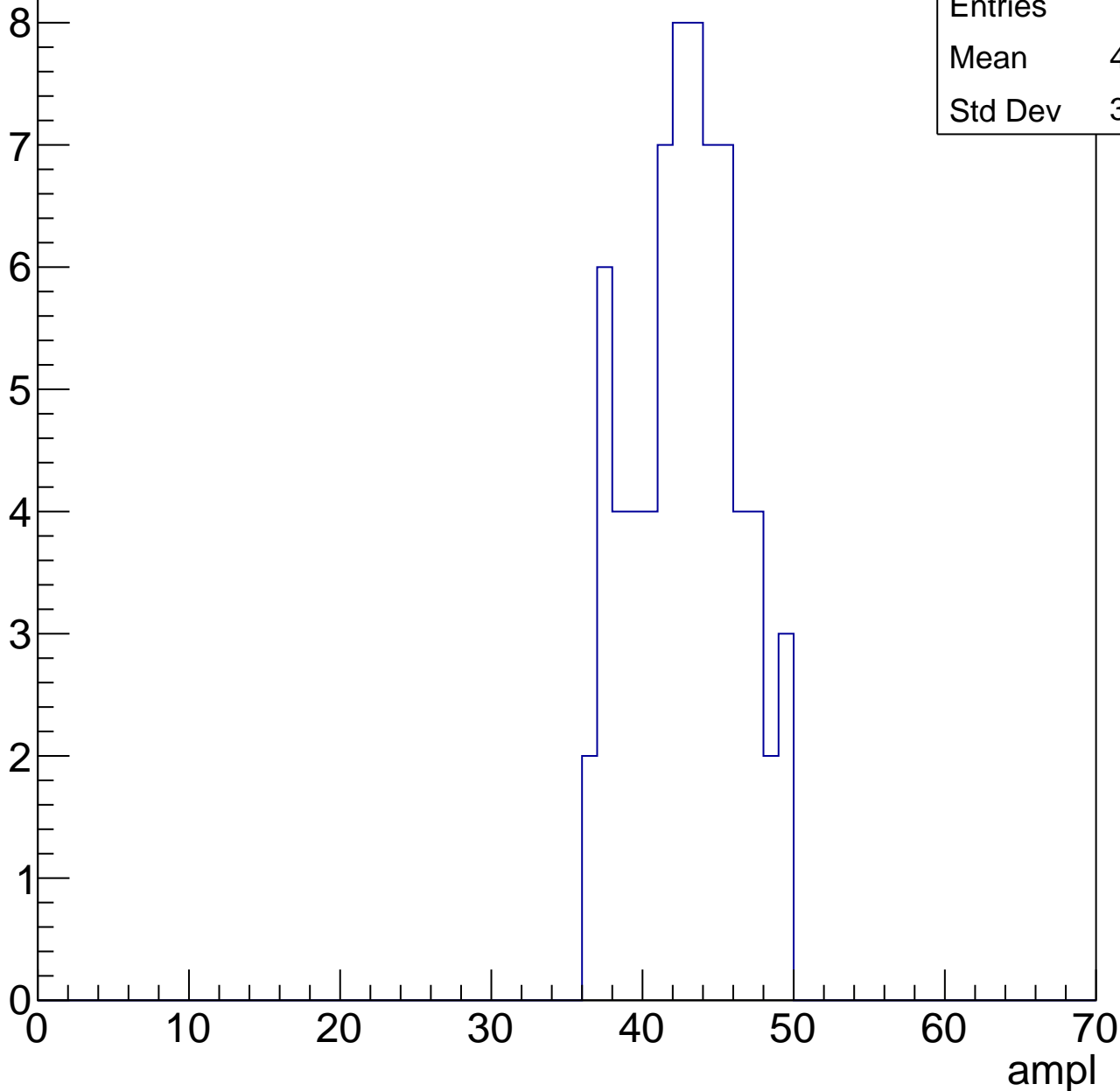


# B1L103S, U25-ch6, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	70
Mean	42.39
Std Dev	3.415

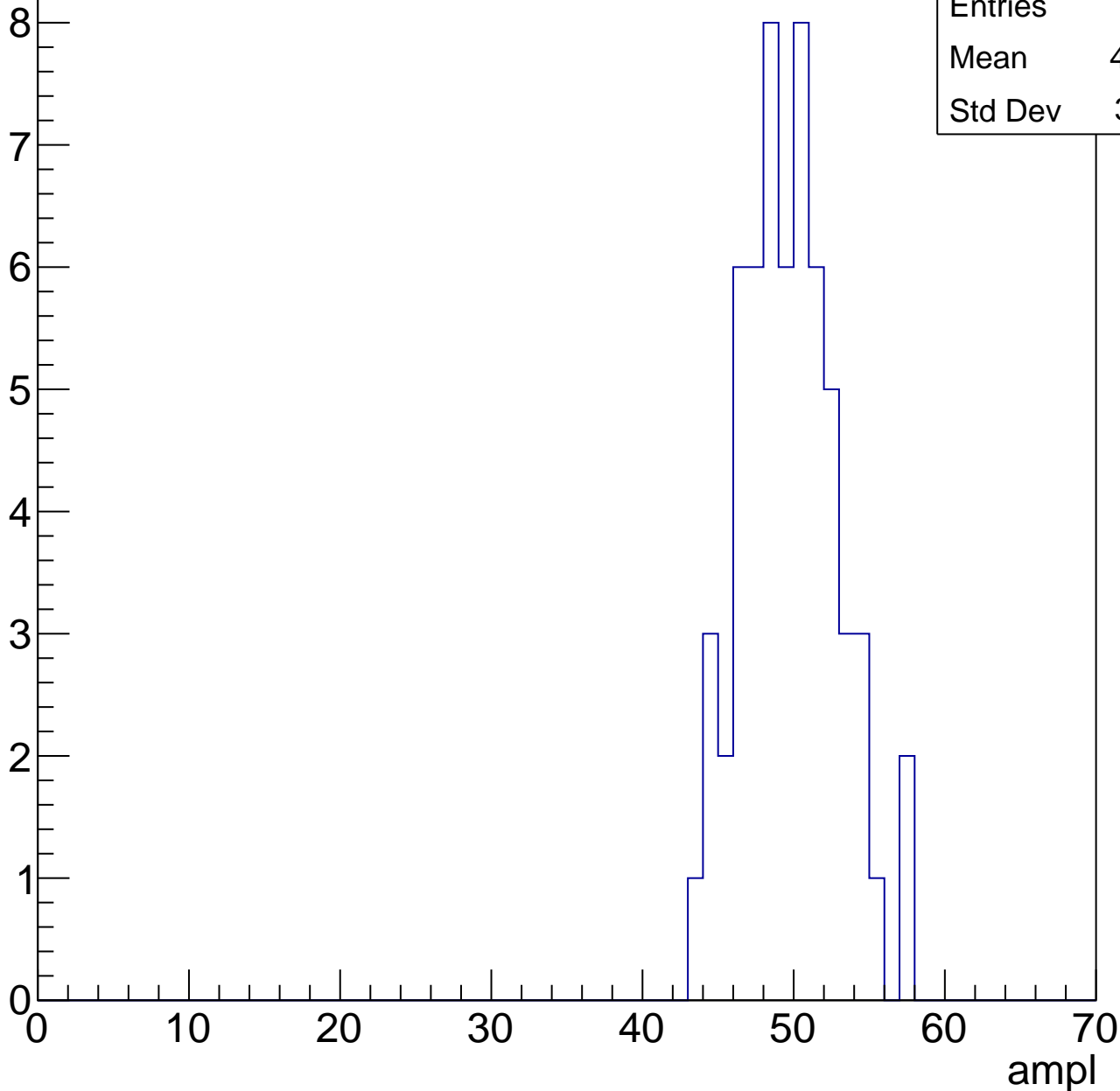


# B1L103S, U25-ch6, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

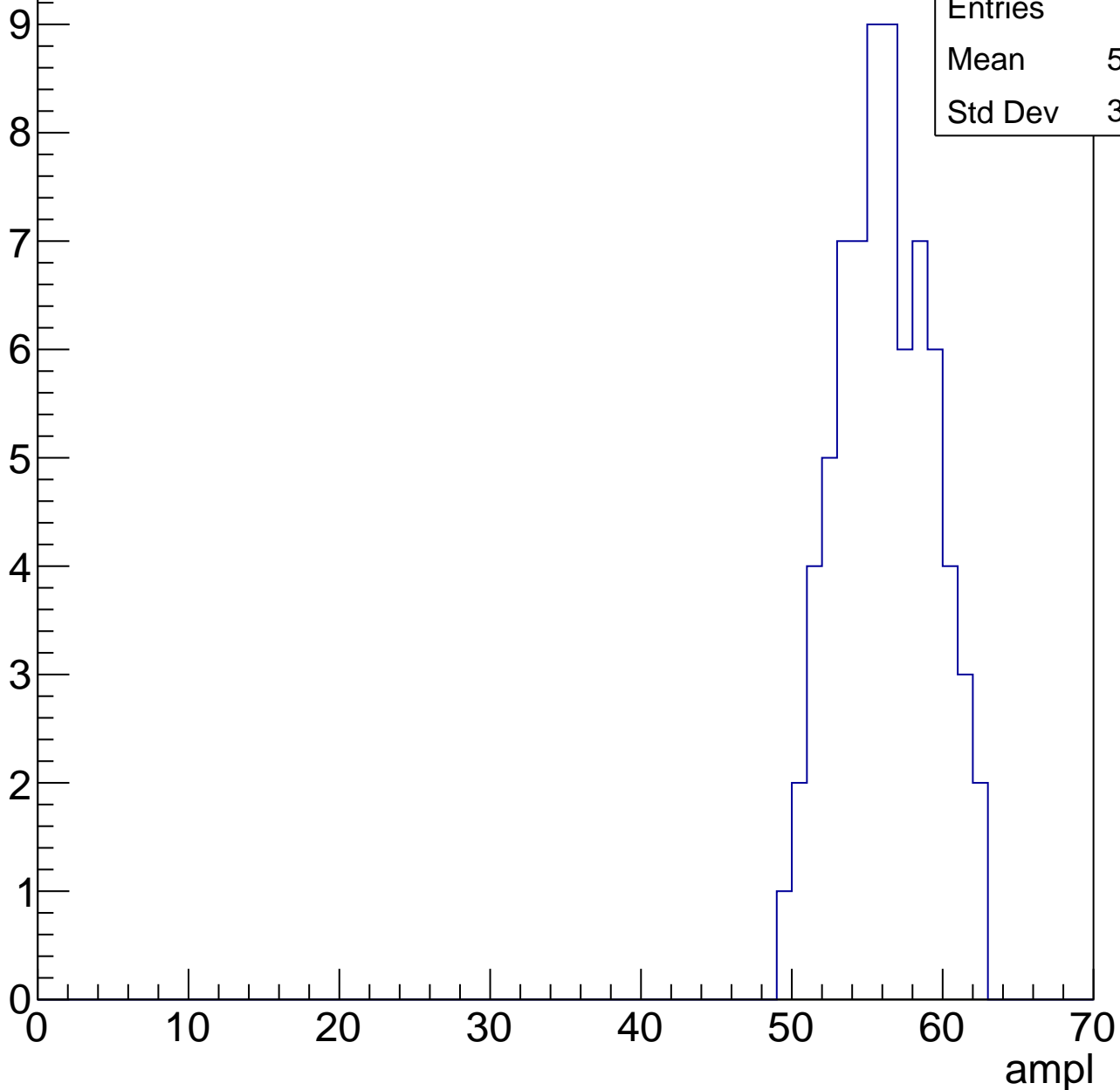
Entries	60
Mean	49.28
Std Dev	3.131



# B1L103S, U25-ch6, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

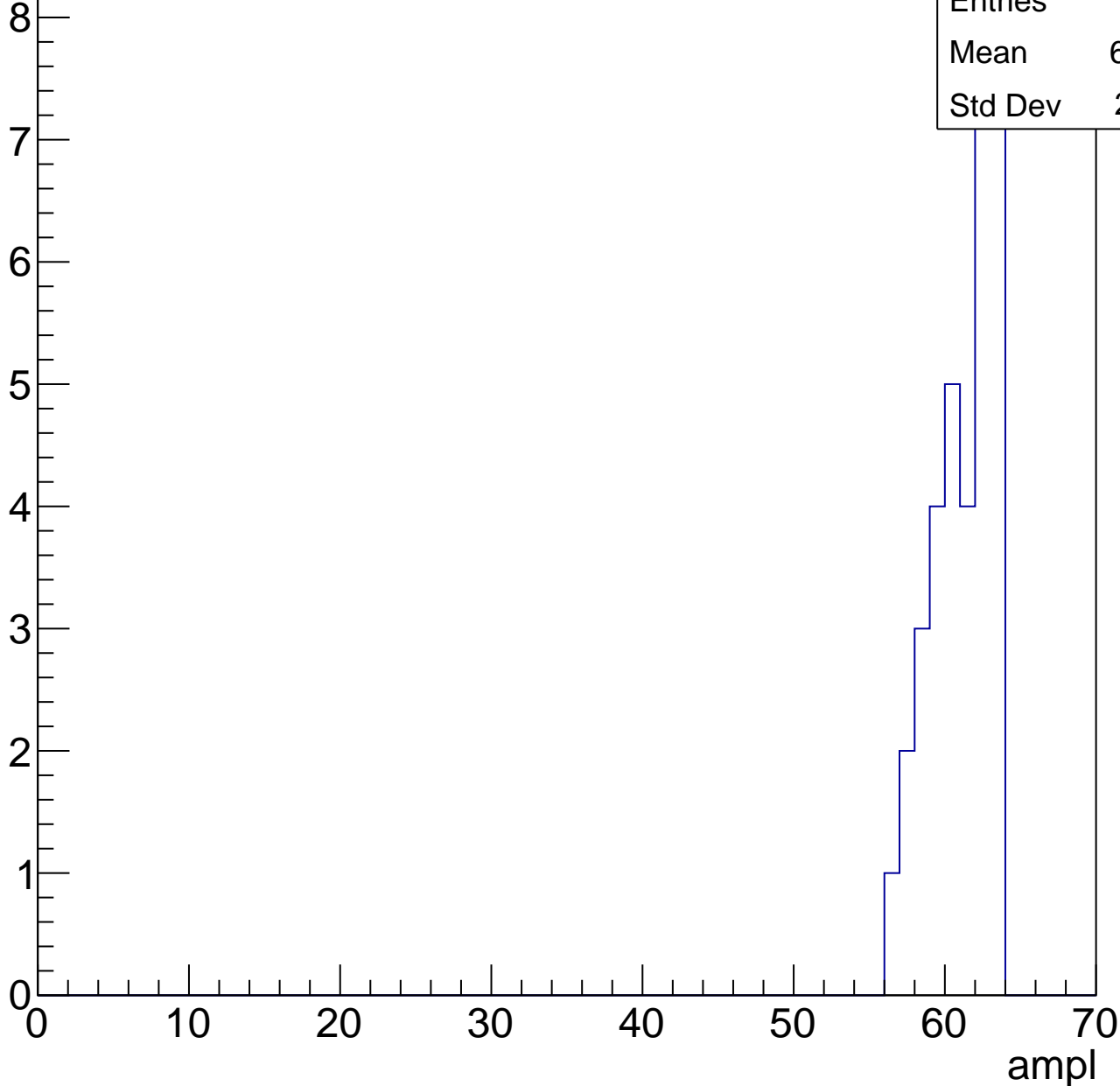


# B1L103S, U25-ch6, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

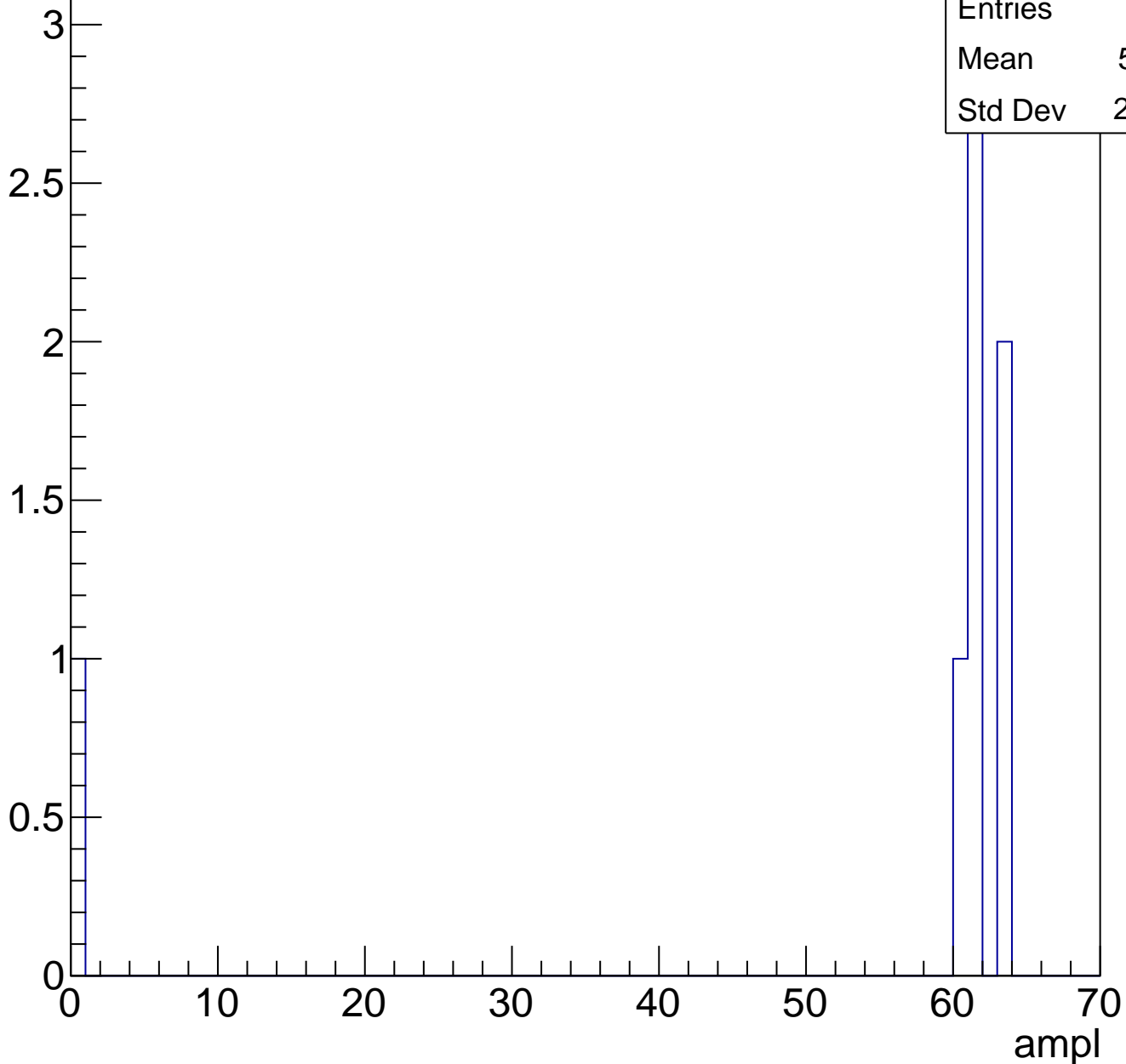
Entries	35
Mean	60.69
Std Dev	2.011



# B1L103S, U25-ch6, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	7
Mean	52.71
Std Dev	21.55



# B1L103S, U25-ch6, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

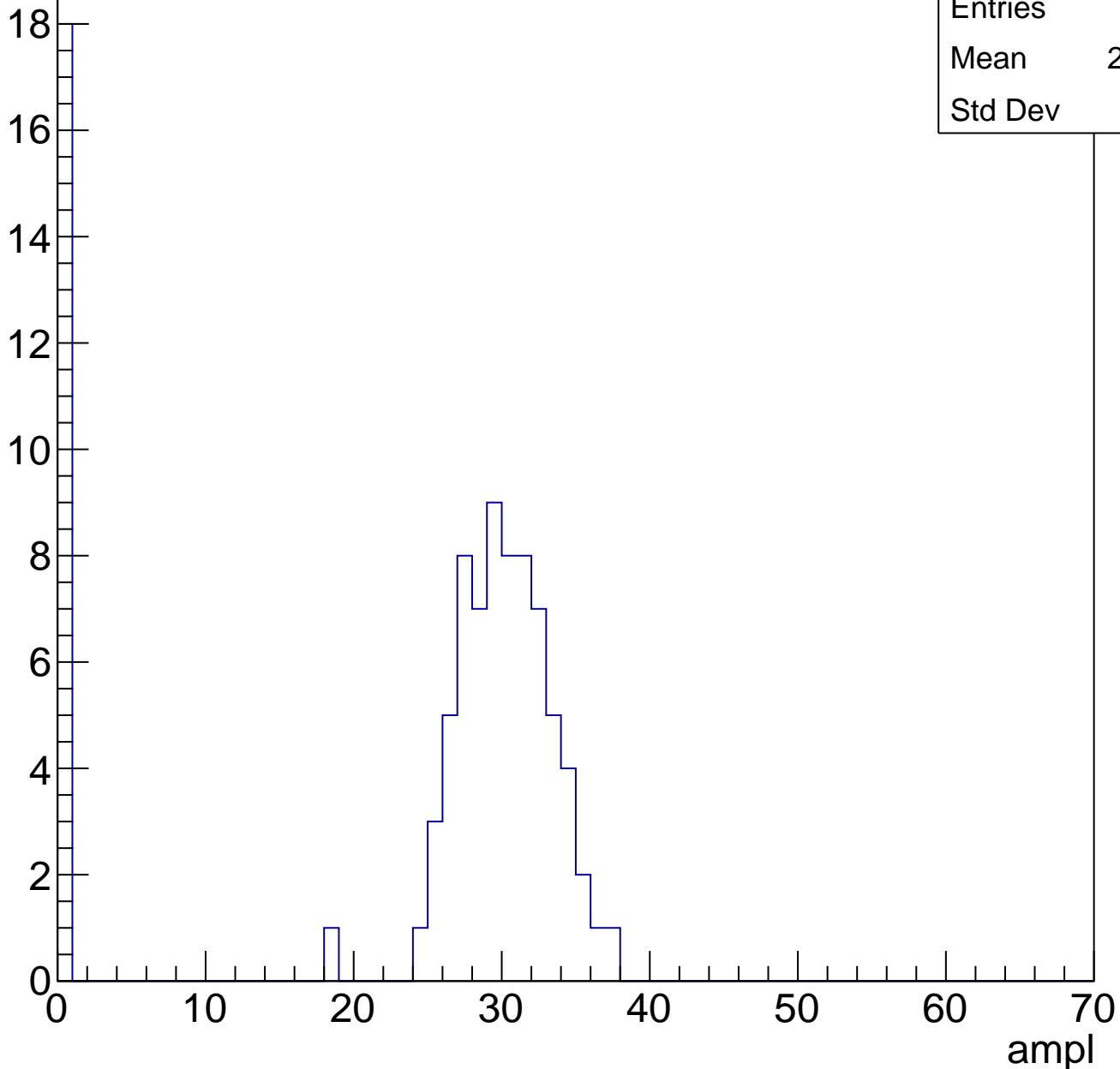


# B1L103S, U25-ch7, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	88
Mean	23.59
Std Dev	12.3

Entry

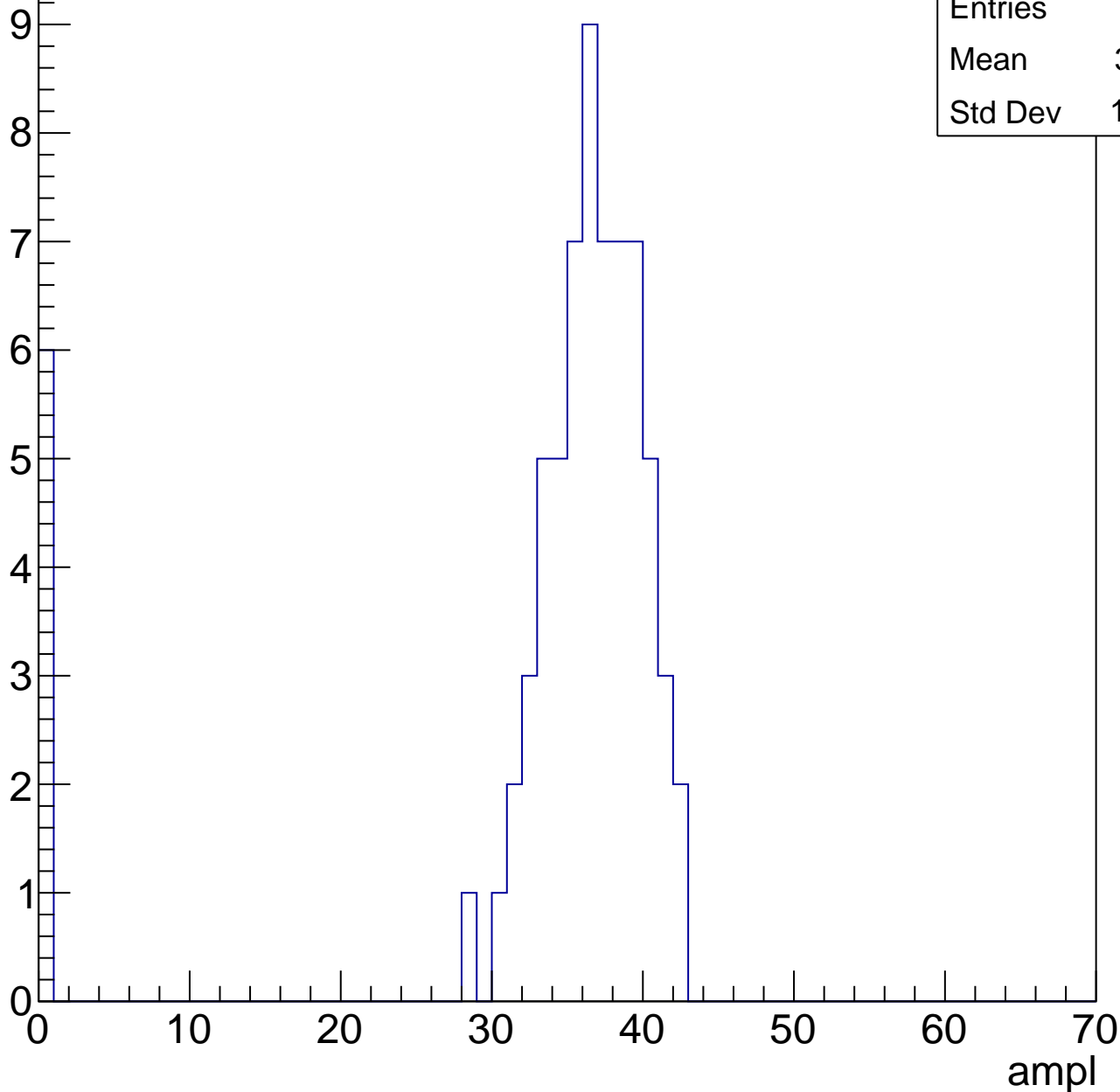


# B1L103S, U25-ch7, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	70
Mean	33.21
Std Dev	10.57

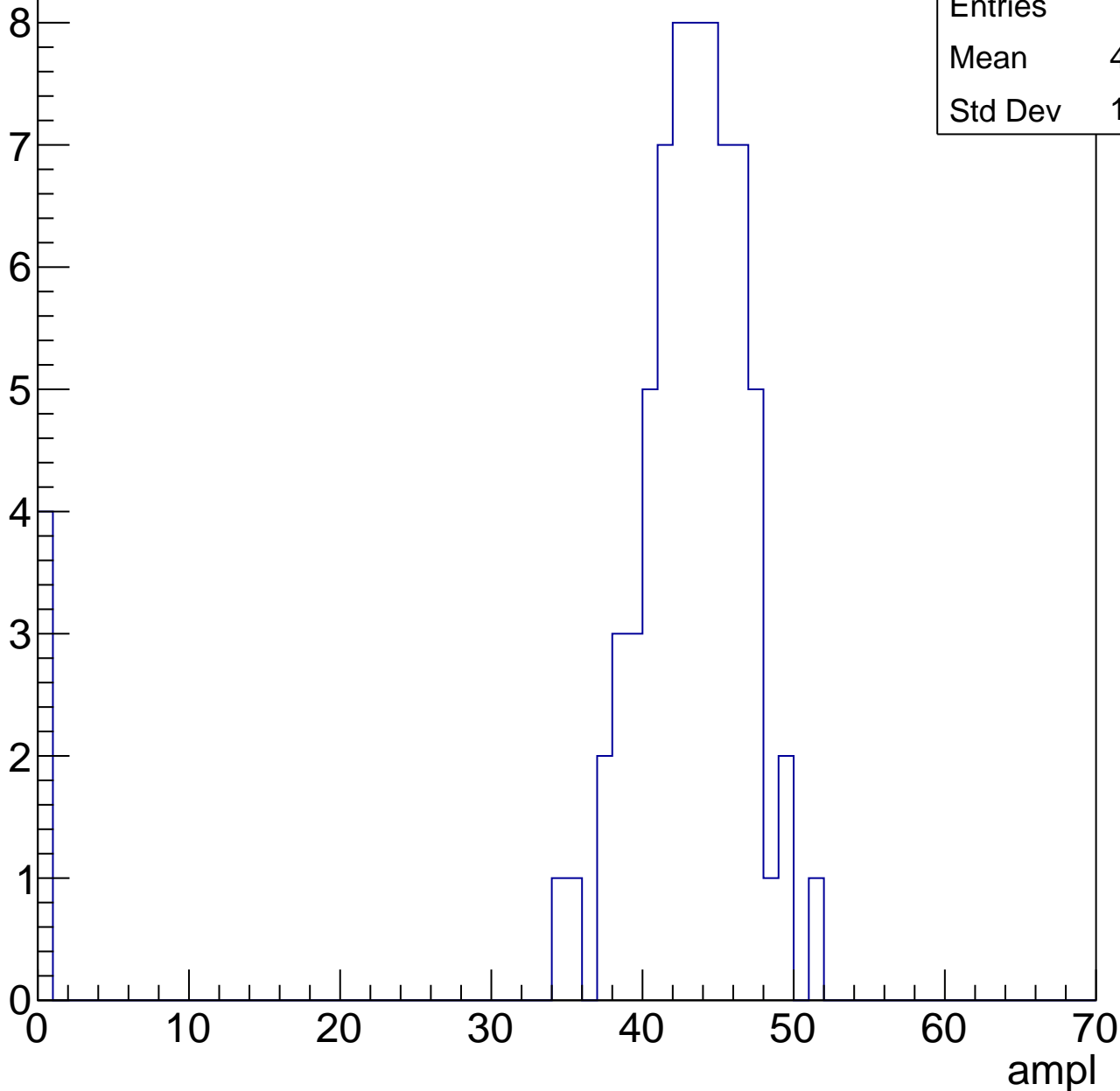


# B1L103S, U25-ch7, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	73
Mean	40.58
Std Dev	10.29

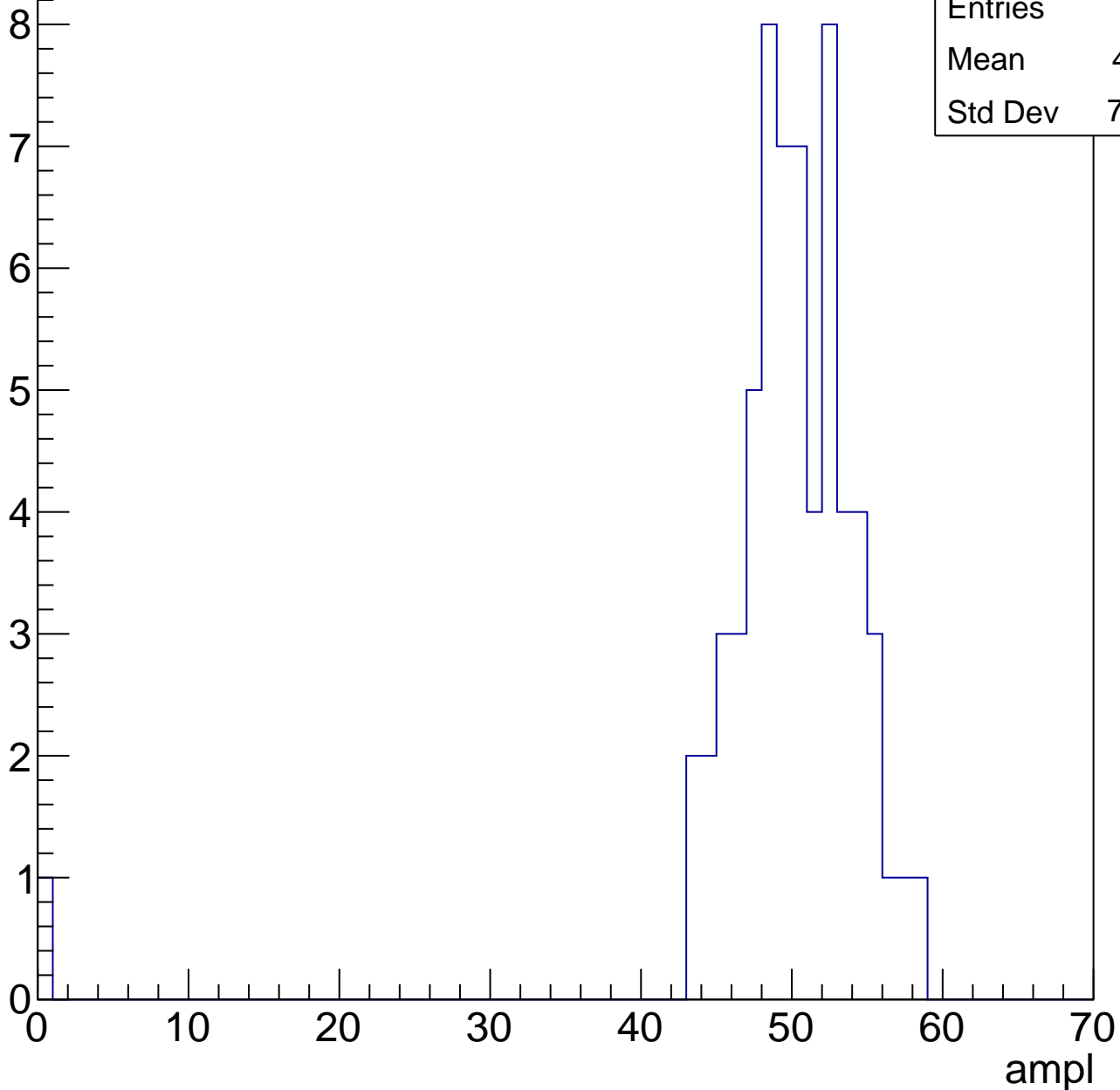


# B1L103S, U25-ch7, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	64
Mean	49.11
Std Dev	7.056

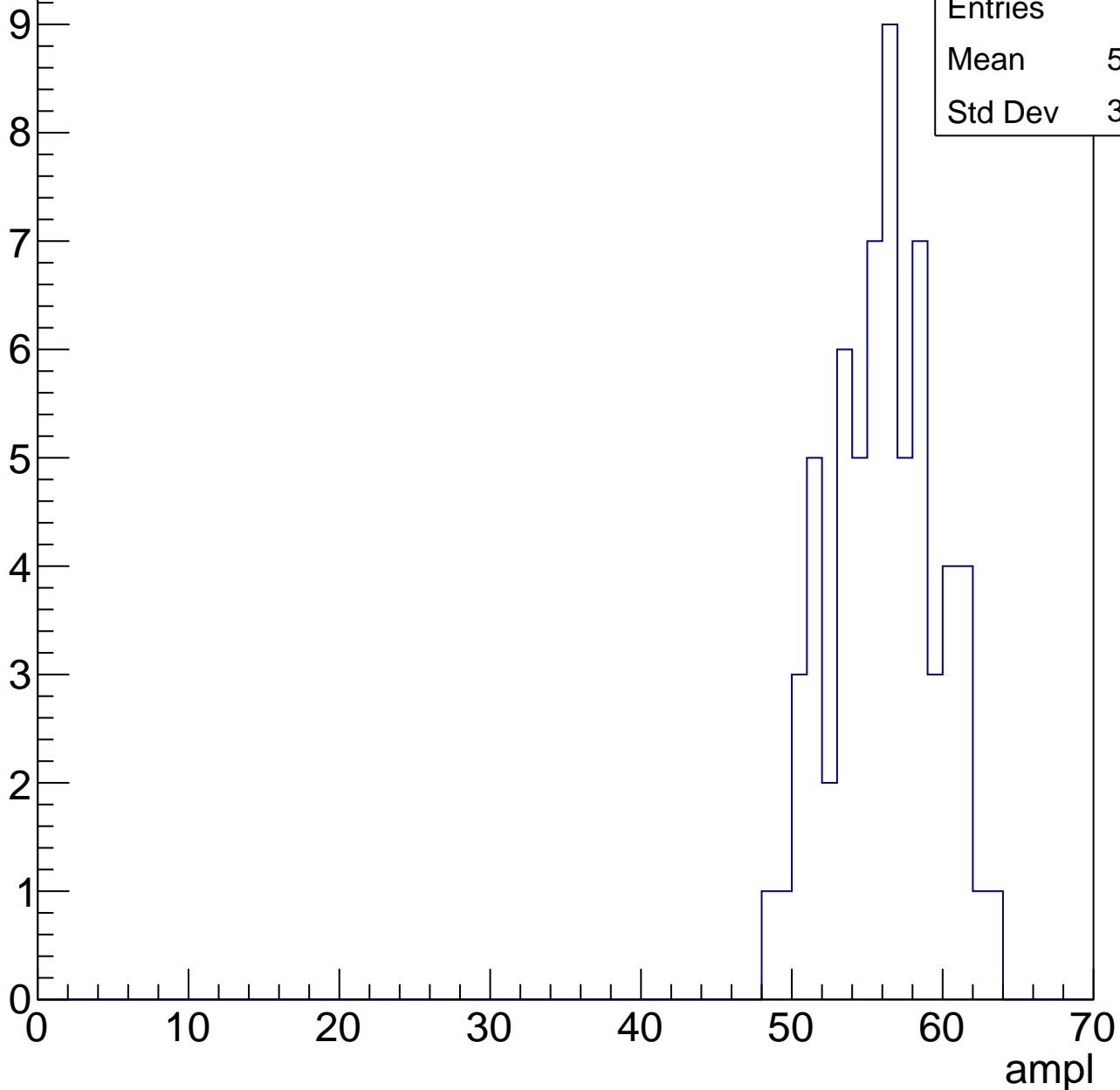


# B1L103S, U25-ch7, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	64
Mean	55.62
Std Dev	3.444

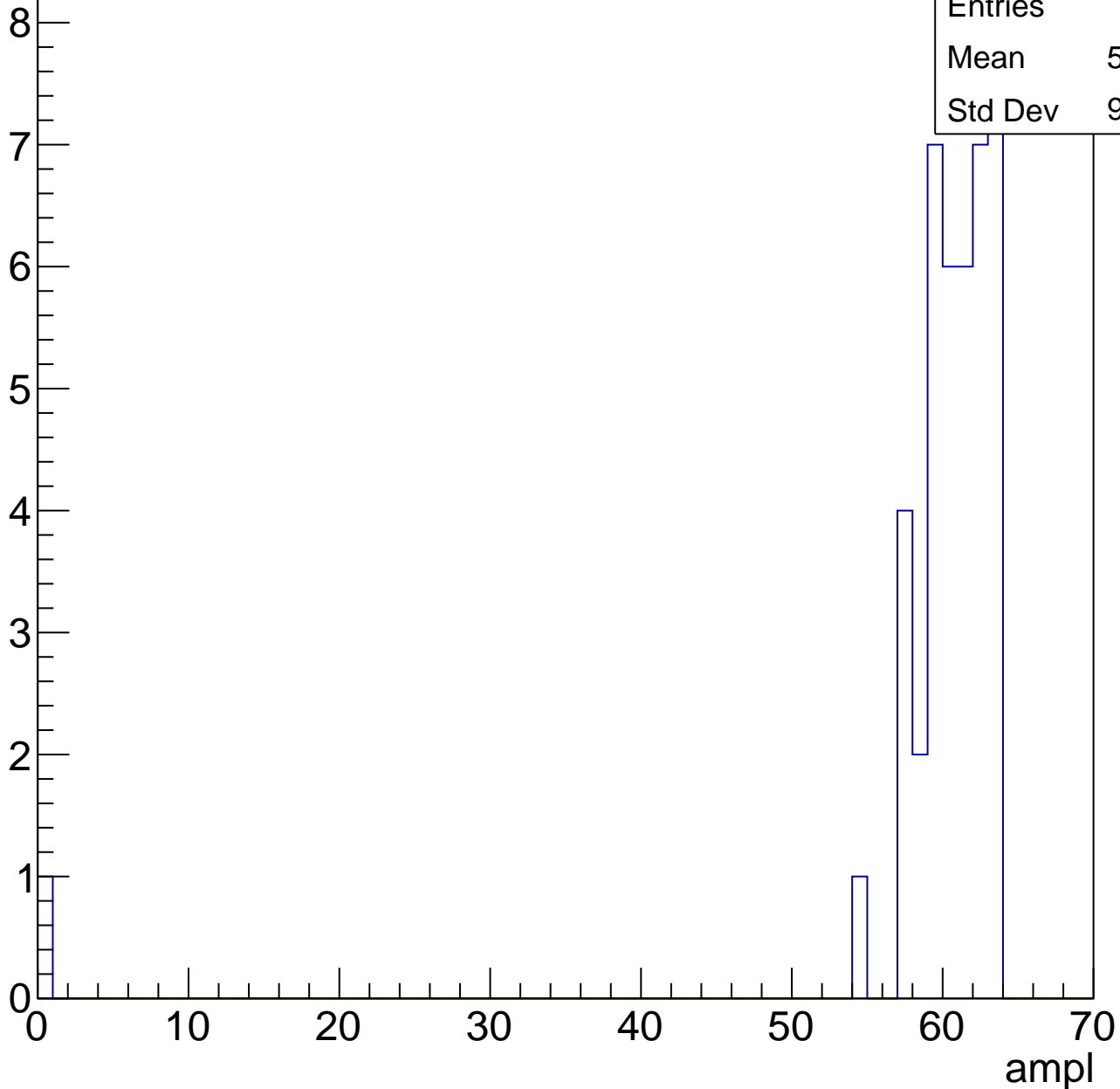


# B1L103S, U25-ch7, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	42
Mean	58.93
Std Dev	9.443



# B1L103S, U25-ch7, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.33
Std Dev	0.4714

ampl

0 10 20 30 40 50 60 70



# B1L103S, U25-ch7, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

# B1L103S, U25-ch8, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

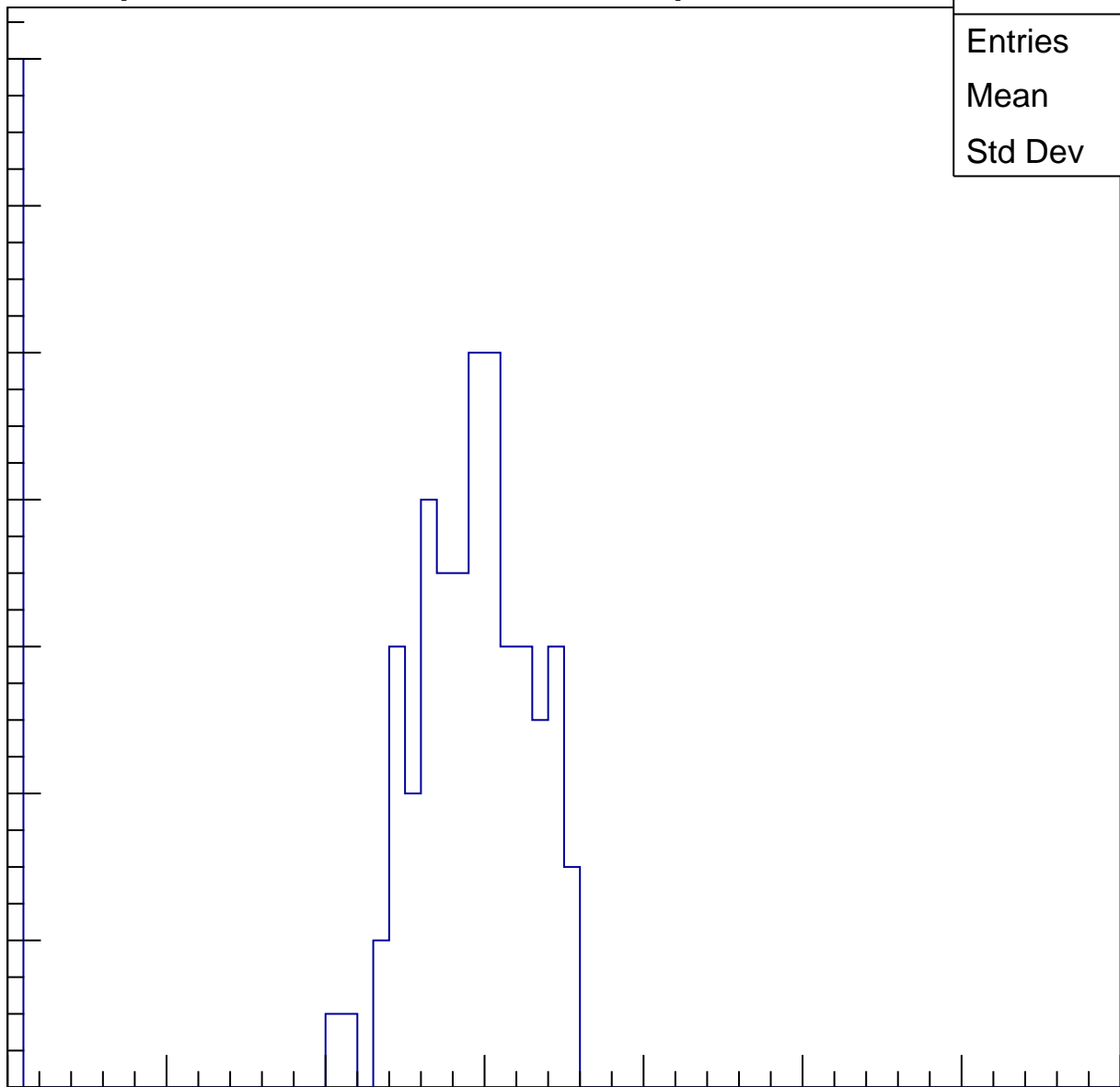
Entries	96
Mean	24.65
Std Dev	10.66

Entry

14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

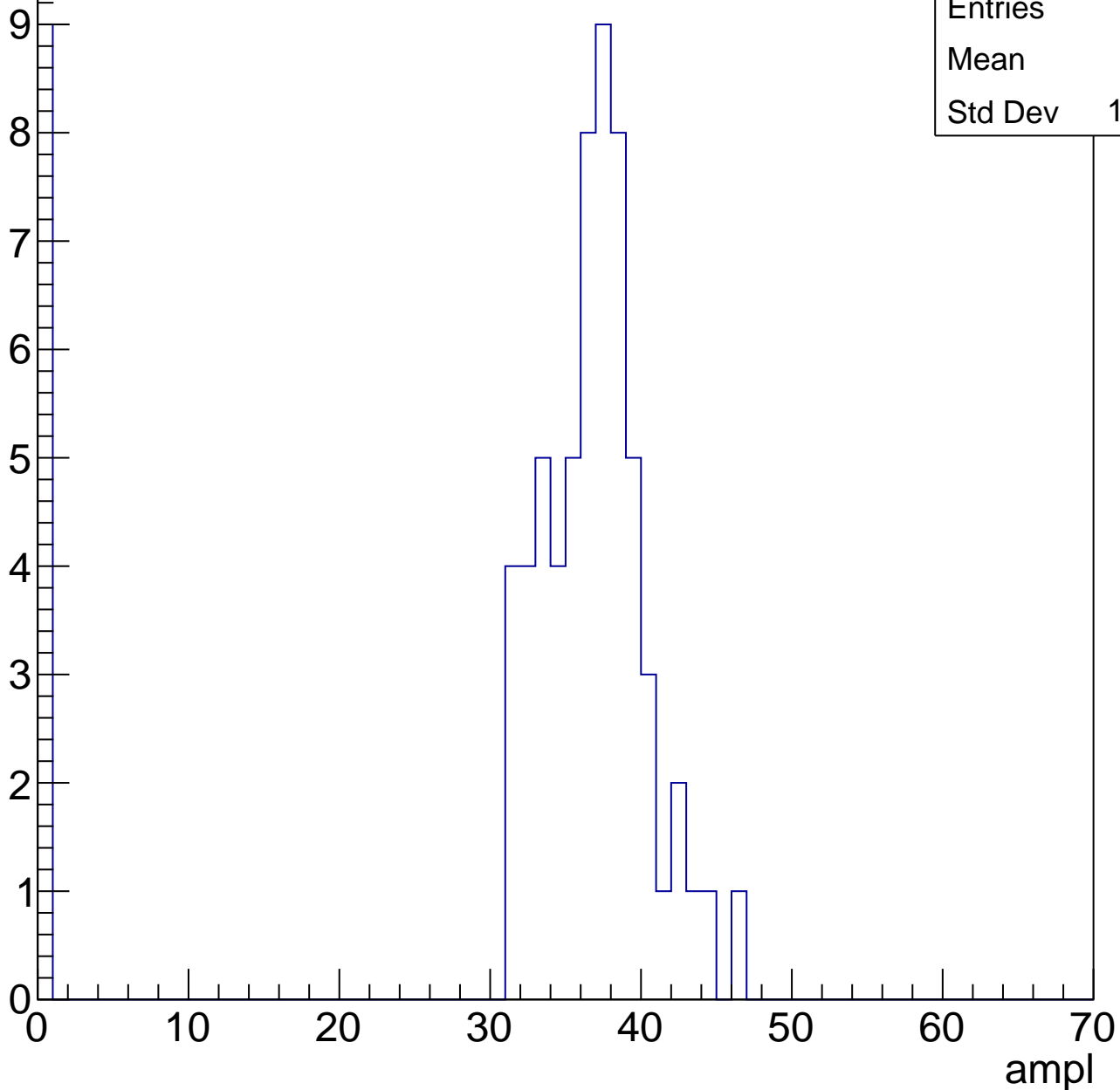


# B1L103S, U25-ch8, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	70
Mean	31.8
Std Dev	12.59

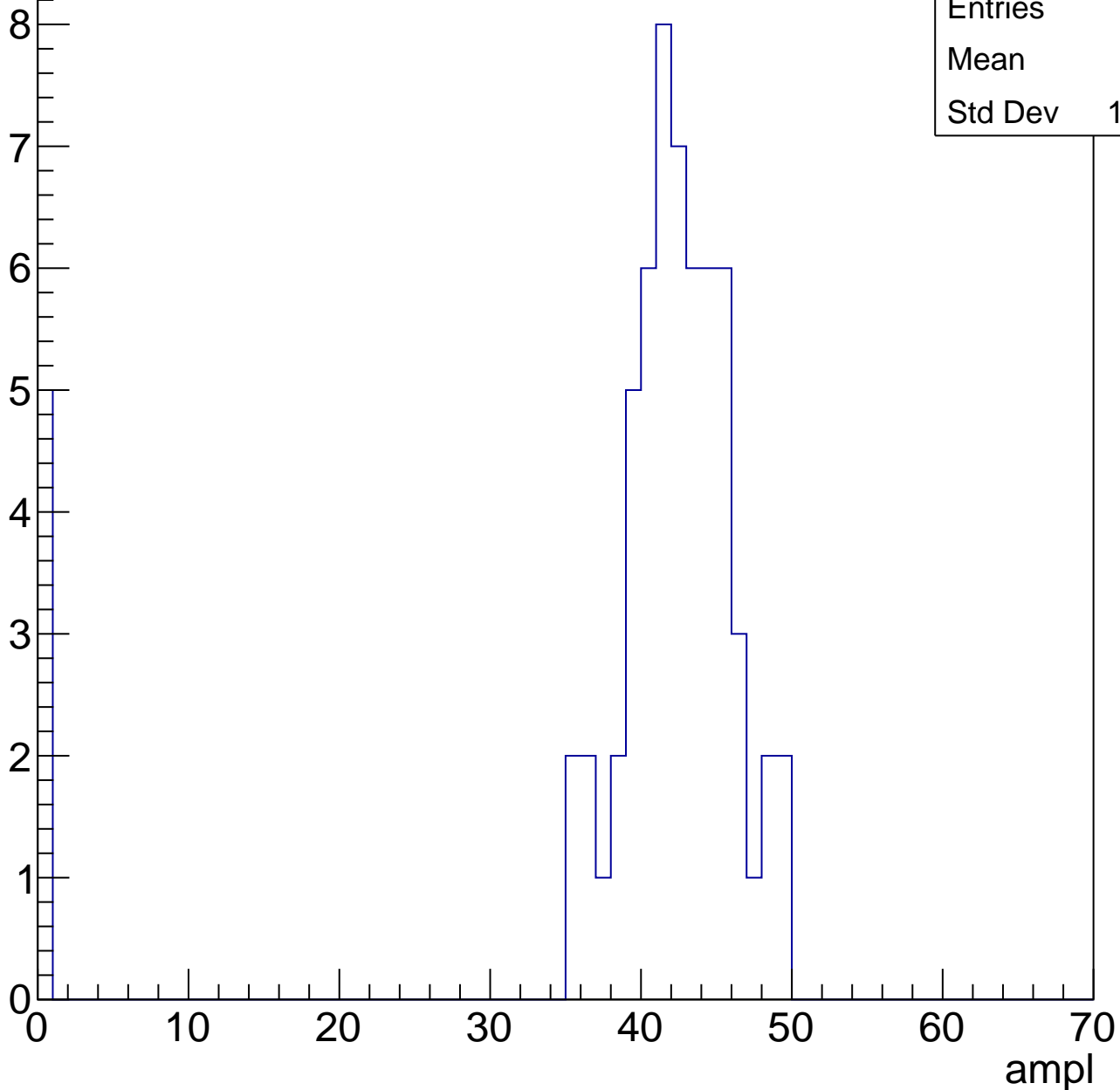


# B1L103S, U25-ch8, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

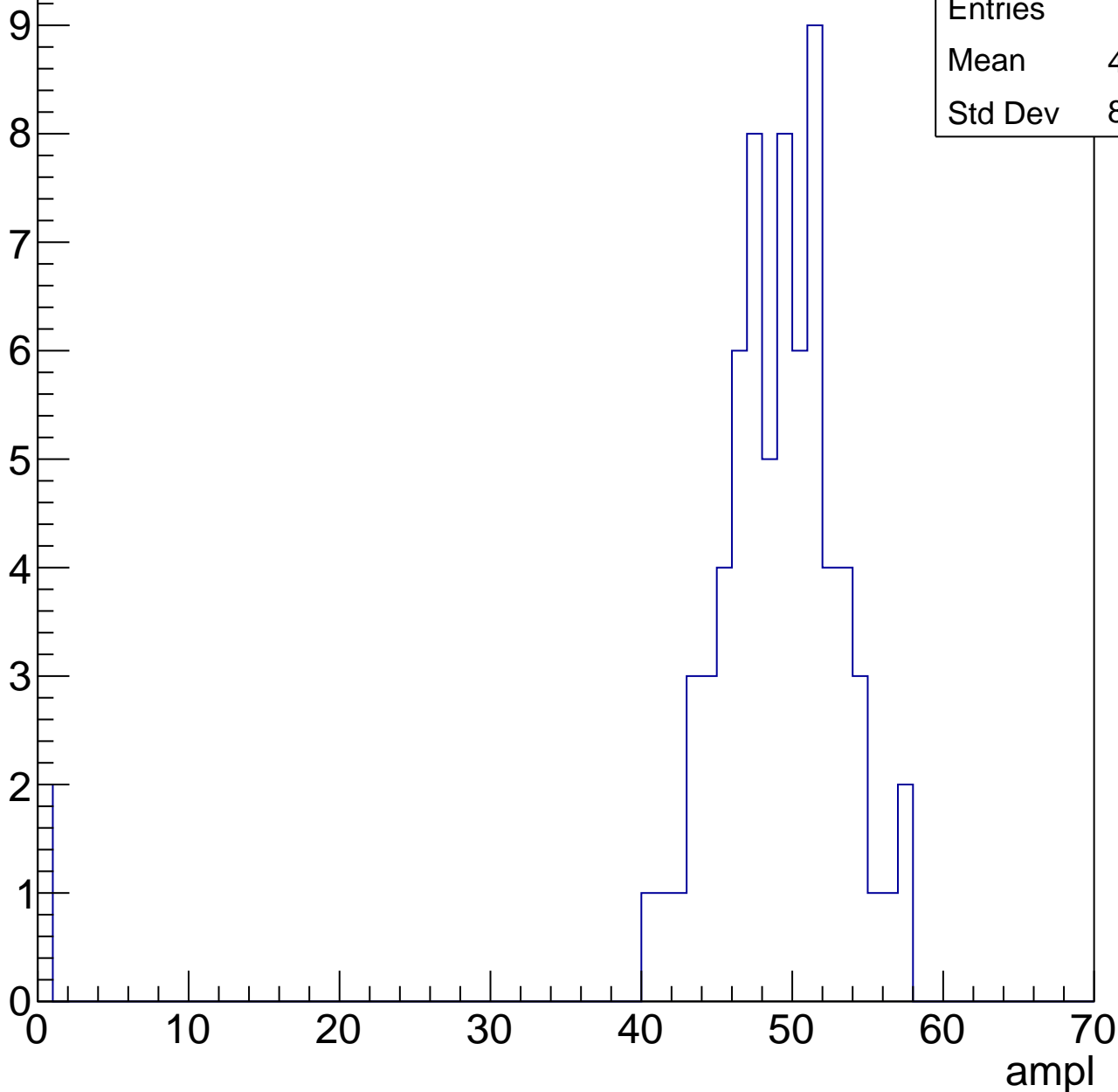
Entries	64
Mean	38.8
Std Dev	11.72



# B1L103S, U25-ch8, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

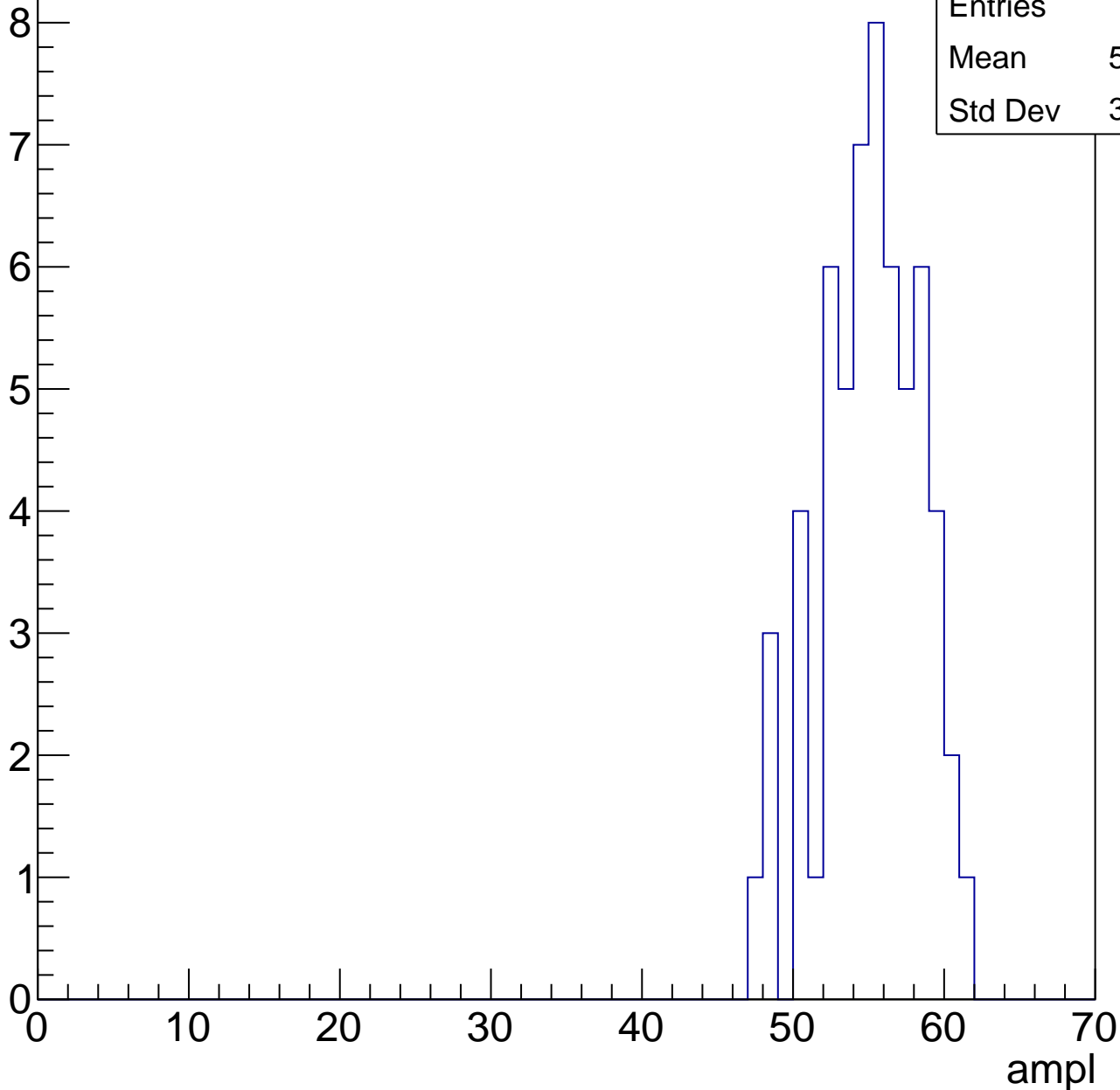


# B1L103S, U25-ch8, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	59
Mean	54.63
Std Dev	3.267

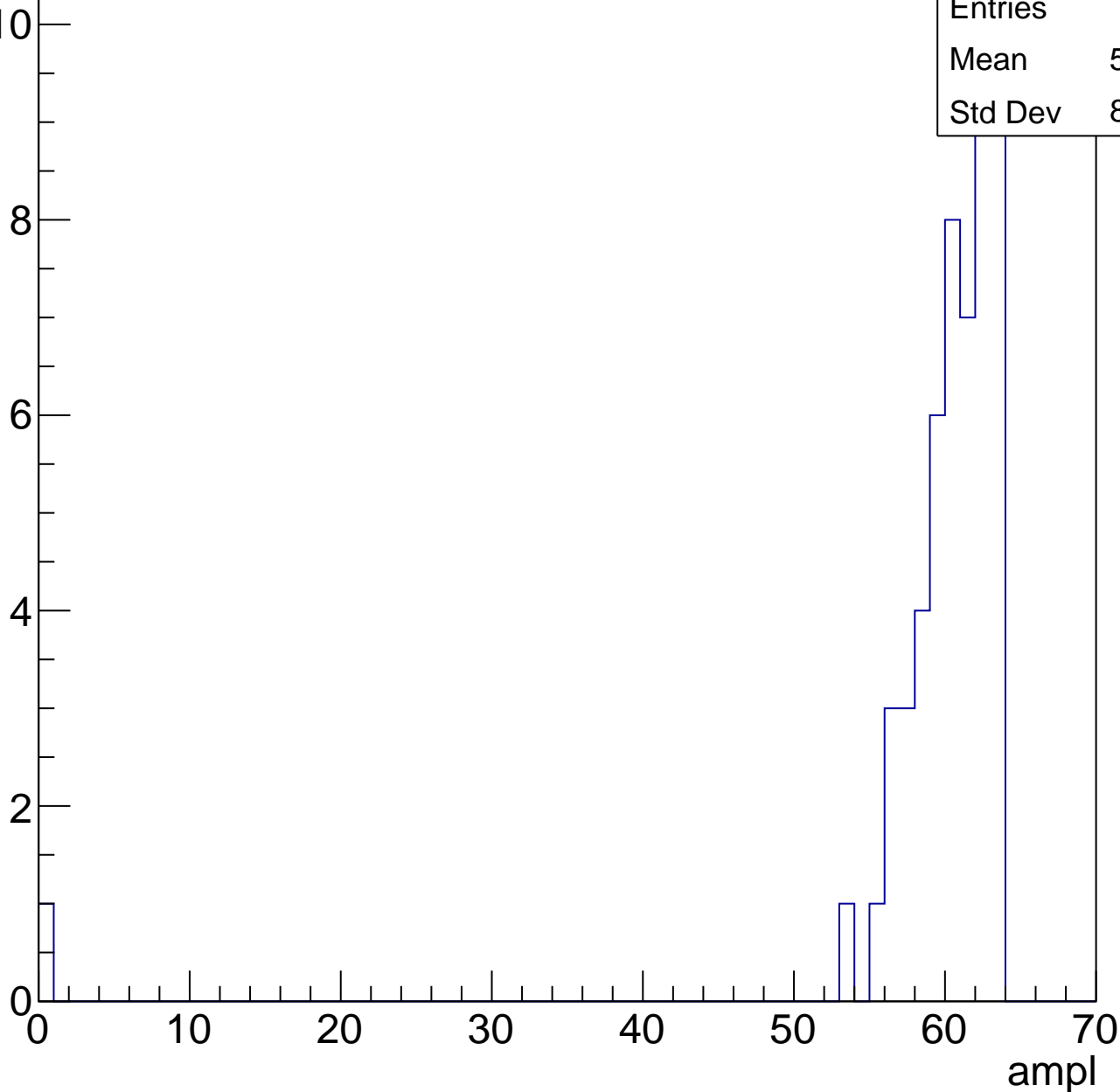


# B1L103S, U25-ch8, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	53
Mean	59.02
Std Dev	8.526



# B1L103S, U25-ch8, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

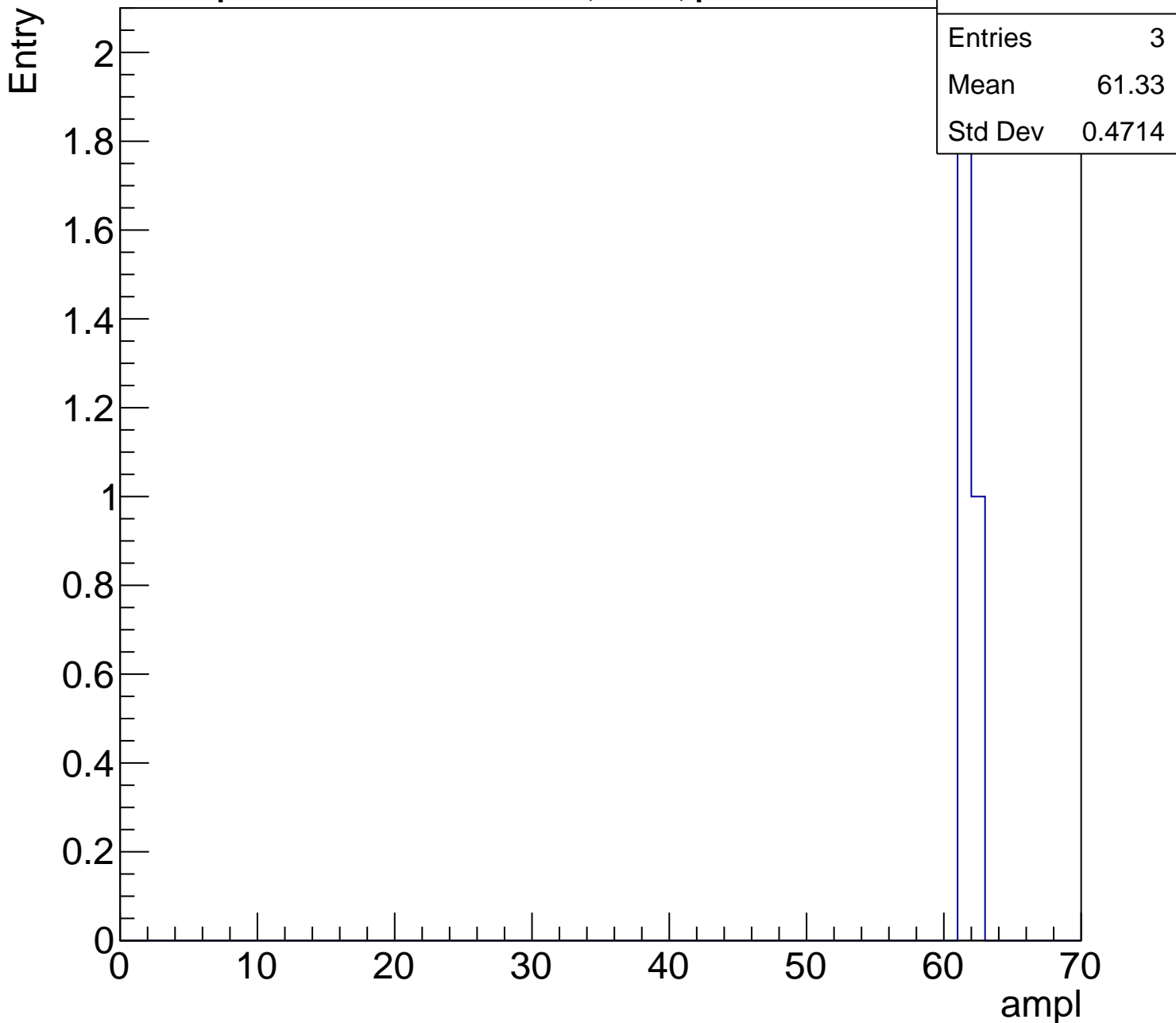
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	61.33
Std Dev	0.4714

0 10 20 30 40 50 60 70

ampl





# B1L103S, U25-ch8, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

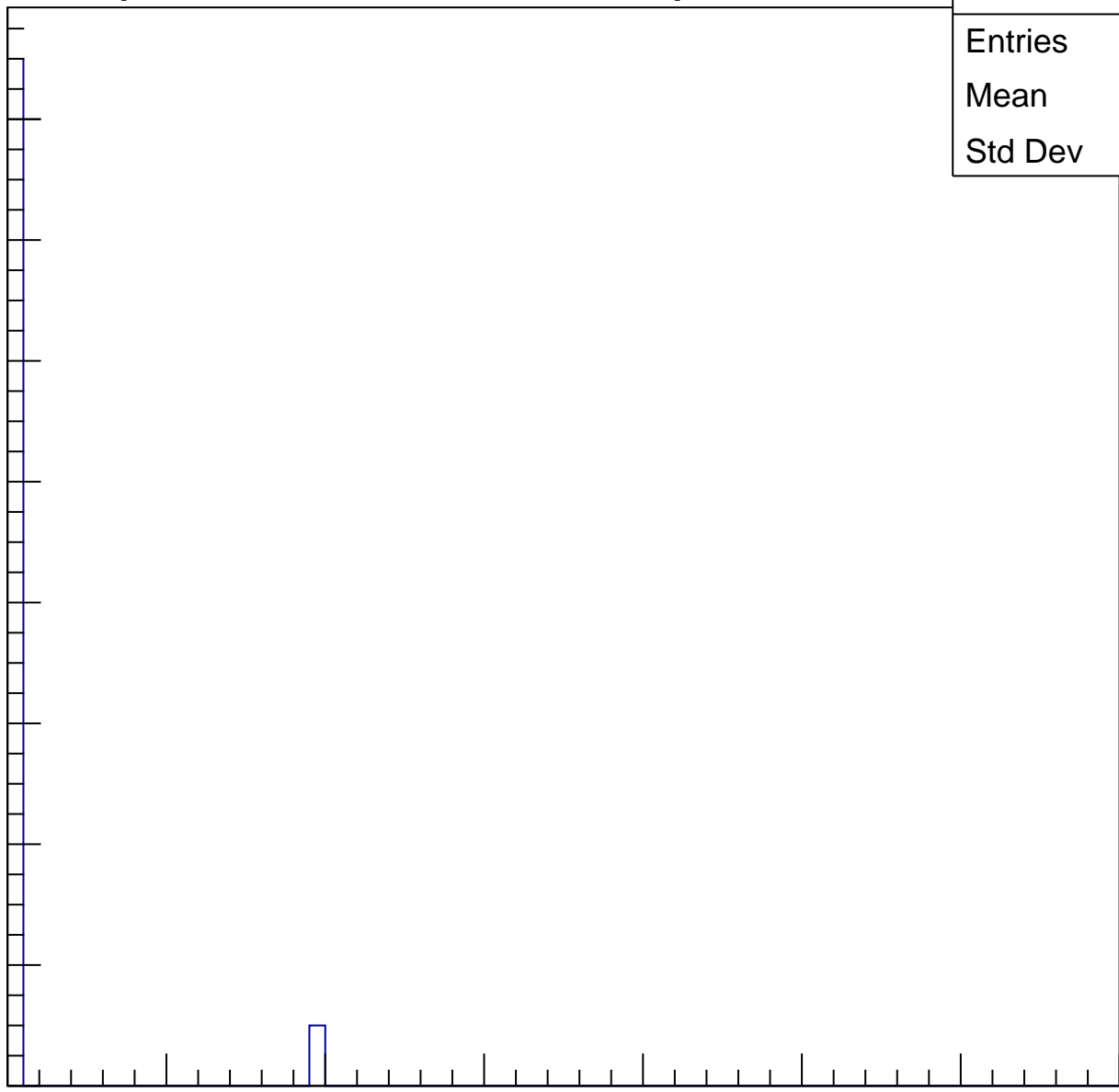
Entries	18
Mean	1.056
Std Dev	4.352

Entry

16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

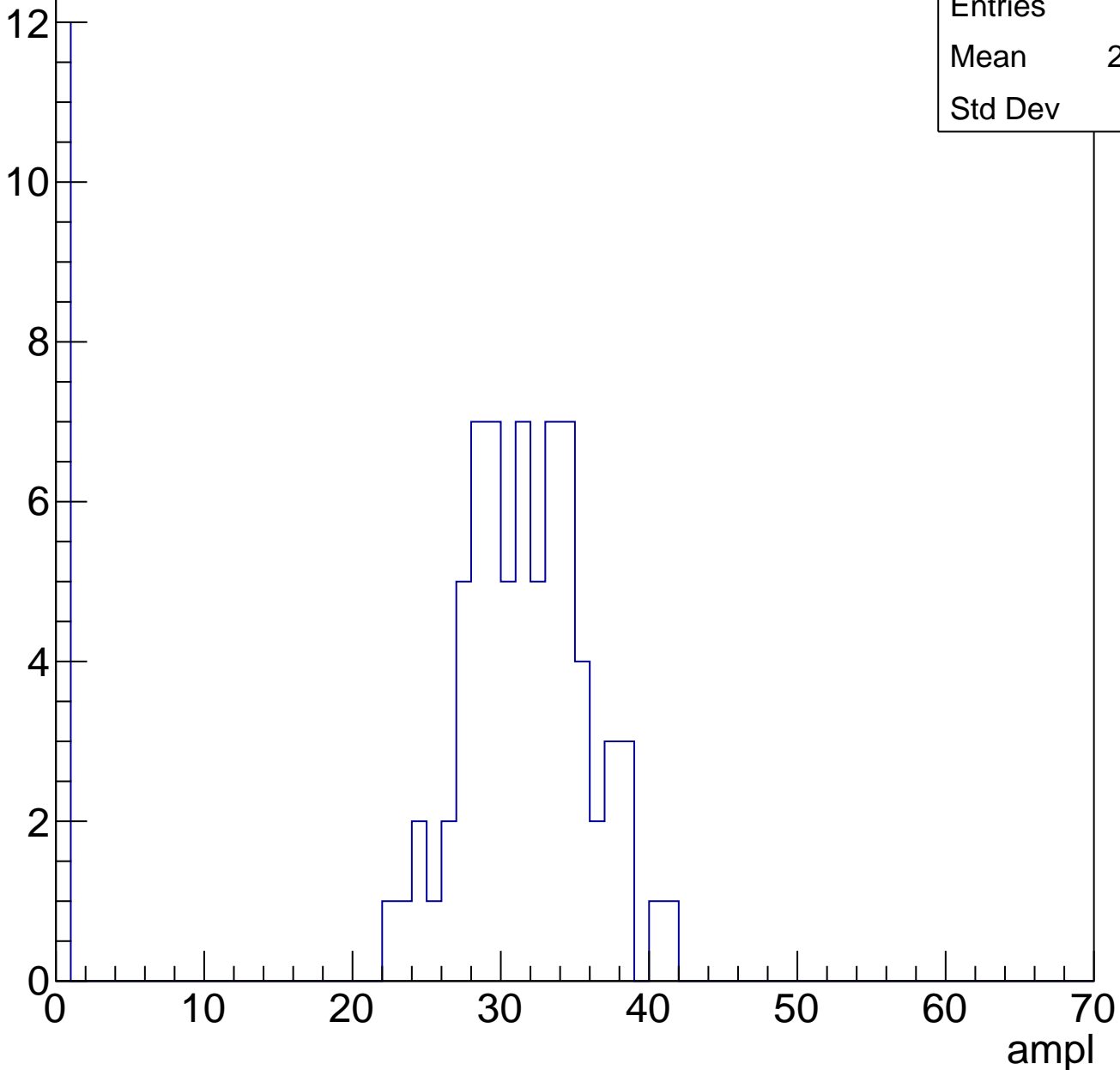


# B1L103S, U25-ch9, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	83
Mean	26.72
Std Dev	11.6

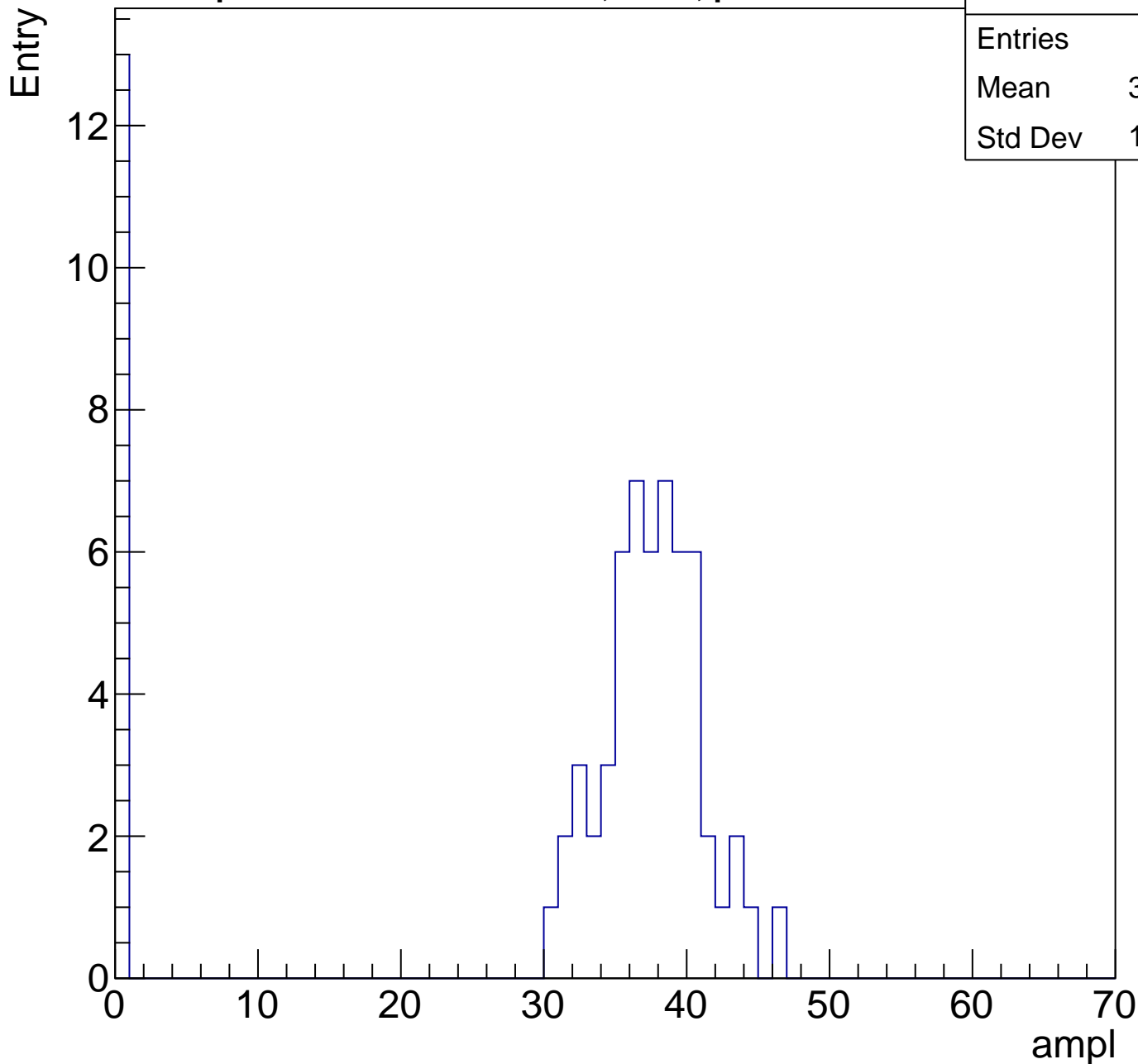
Entry



# B1L103S, U25-ch9, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	69
Mean	30.14
Std Dev	14.83

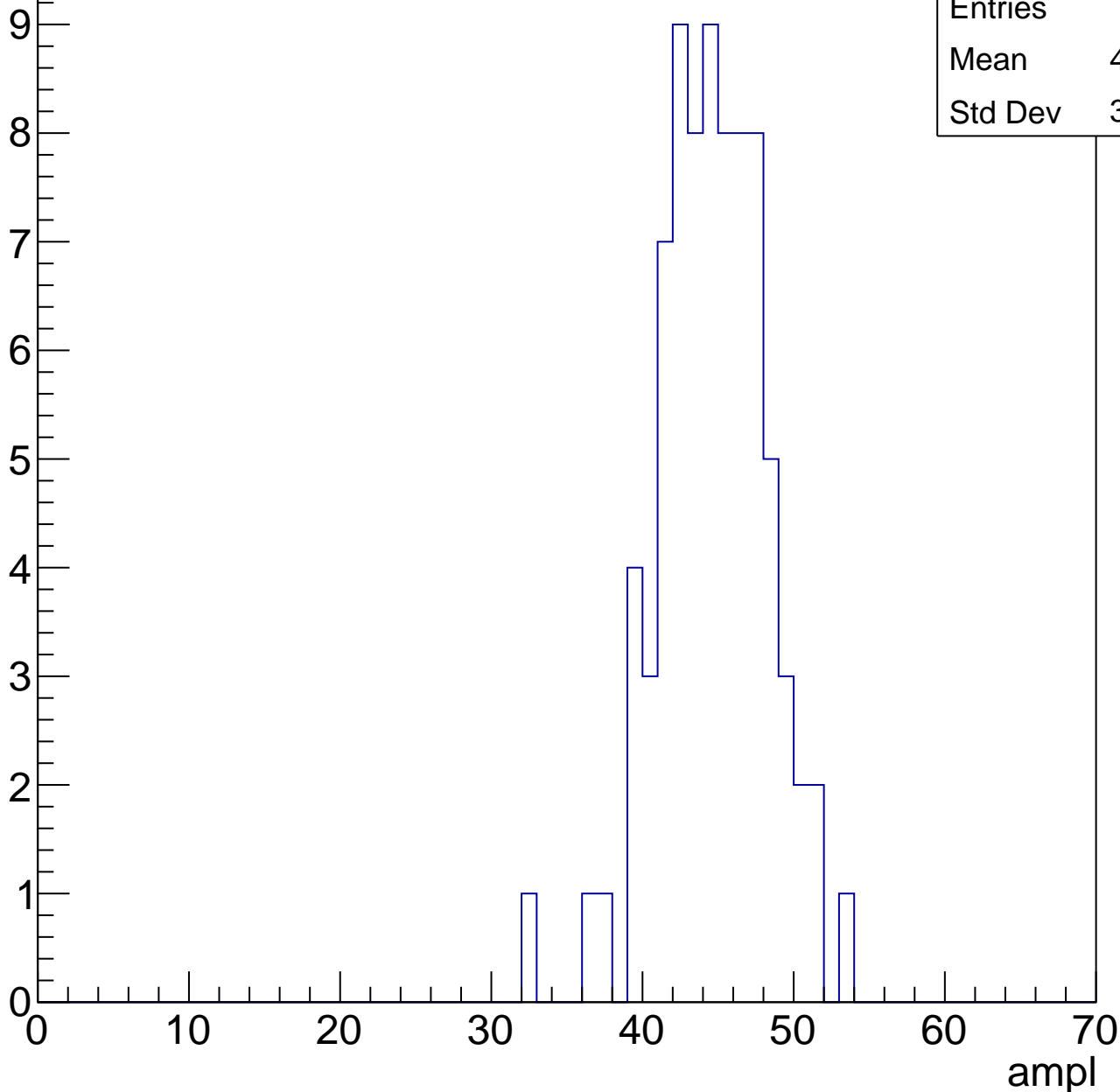


# B1L103S, U25-ch9, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	80
Mean	44.15
Std Dev	3.585

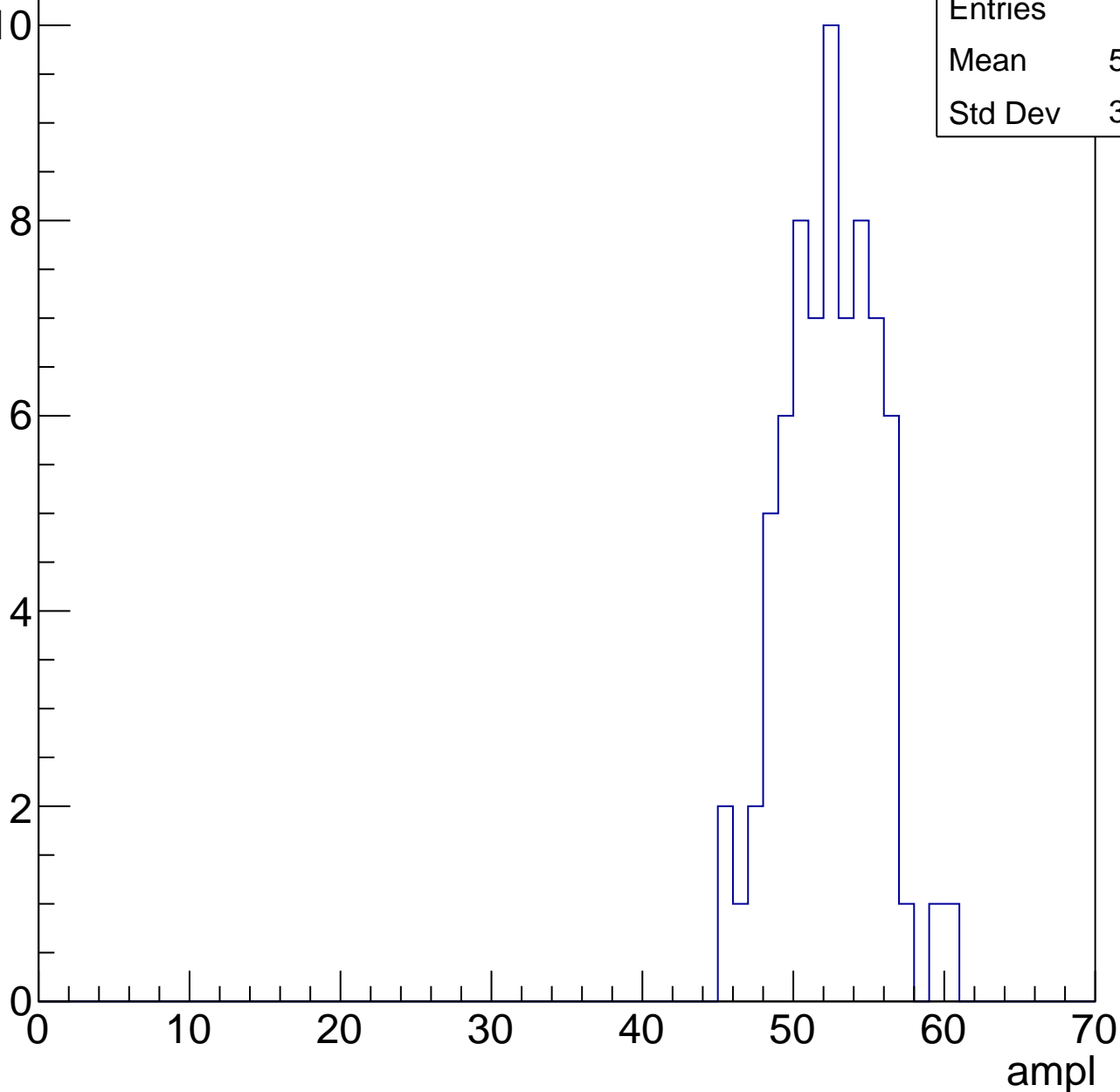


# B1L103S, U25-ch9, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	72
Mean	51.96
Std Dev	3.102

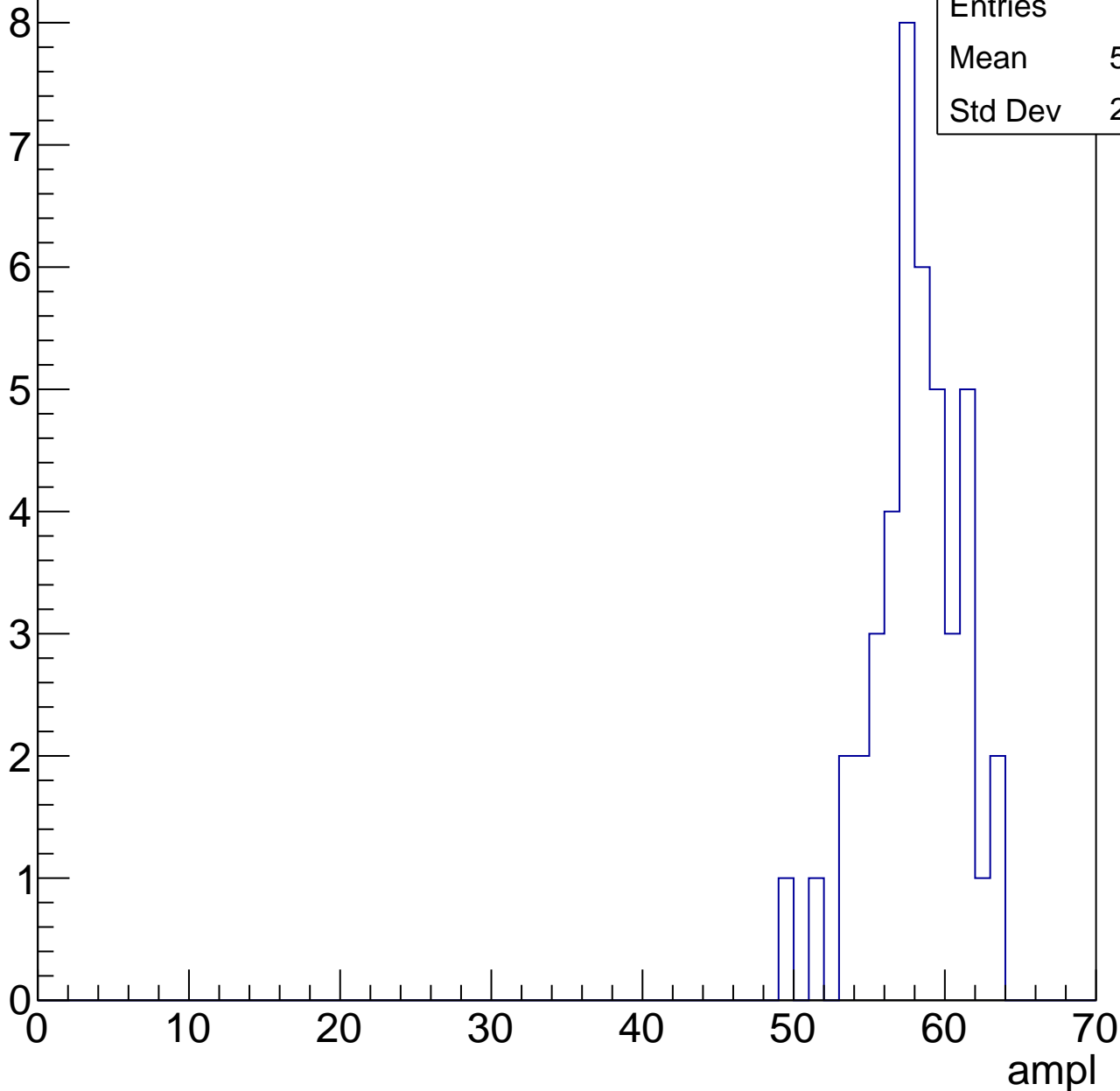


# B1L103S, U25-ch9, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	43
Mean	57.56
Std Dev	2.983

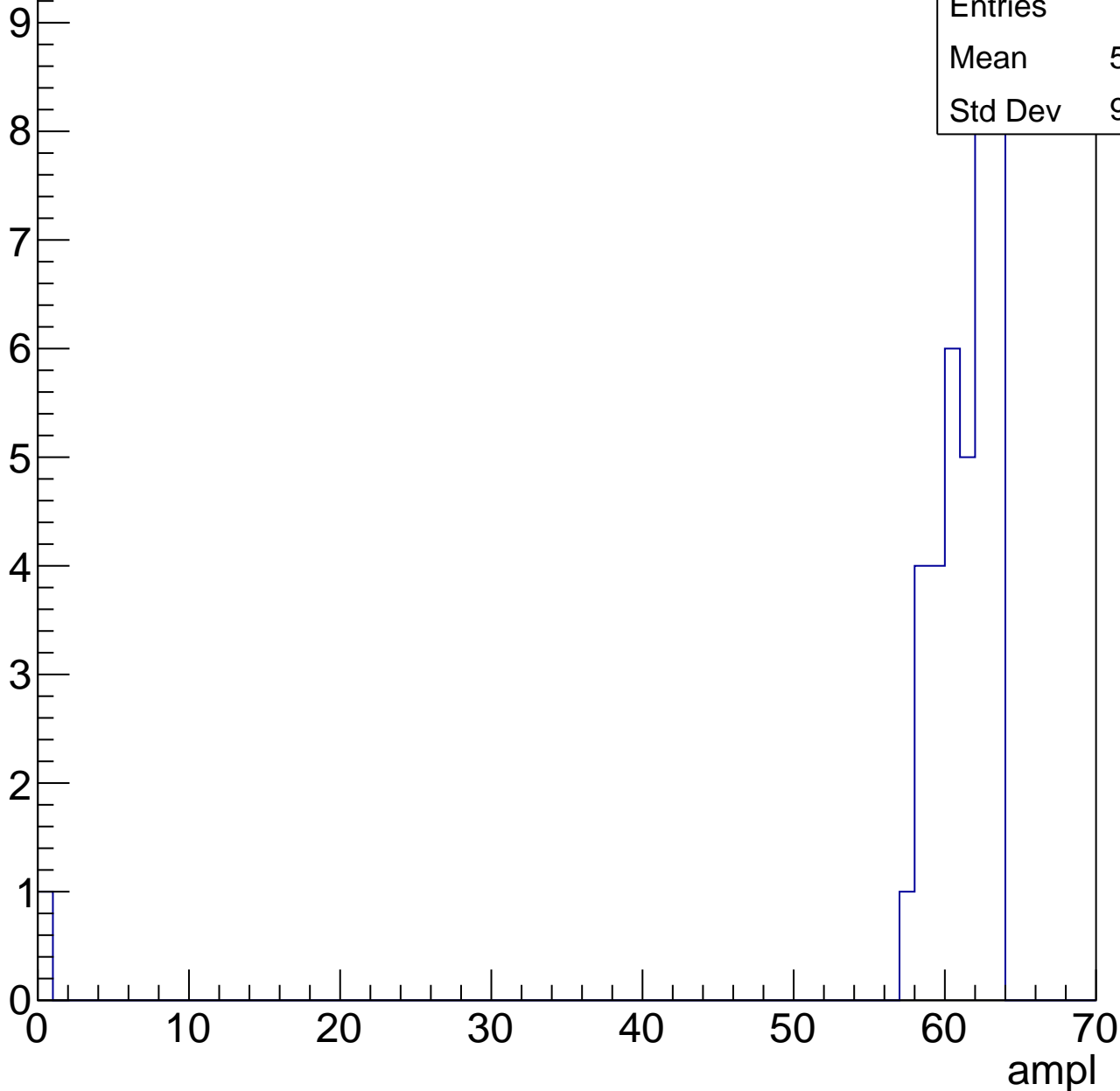


# B1L103S, U25-ch9, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	38
Mean	59.26
Std Dev	9.896



# B1L103S, U25-ch9, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L103S, U25-ch9, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

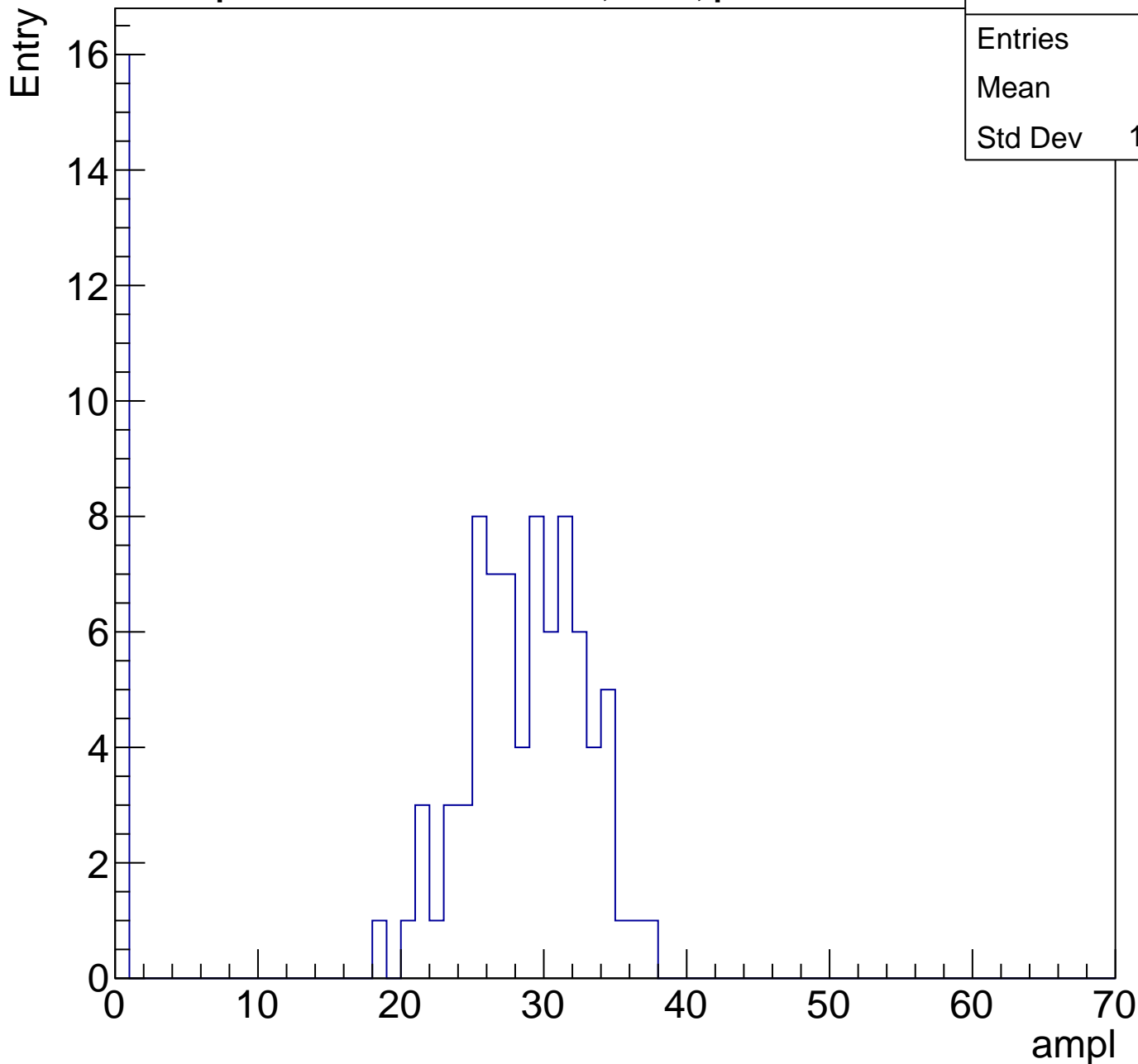
Entries	19
Mean	0
Std Dev	0

ampl

# B1L103S, U25-ch10, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	94
Mean	23.5
Std Dev	11.25

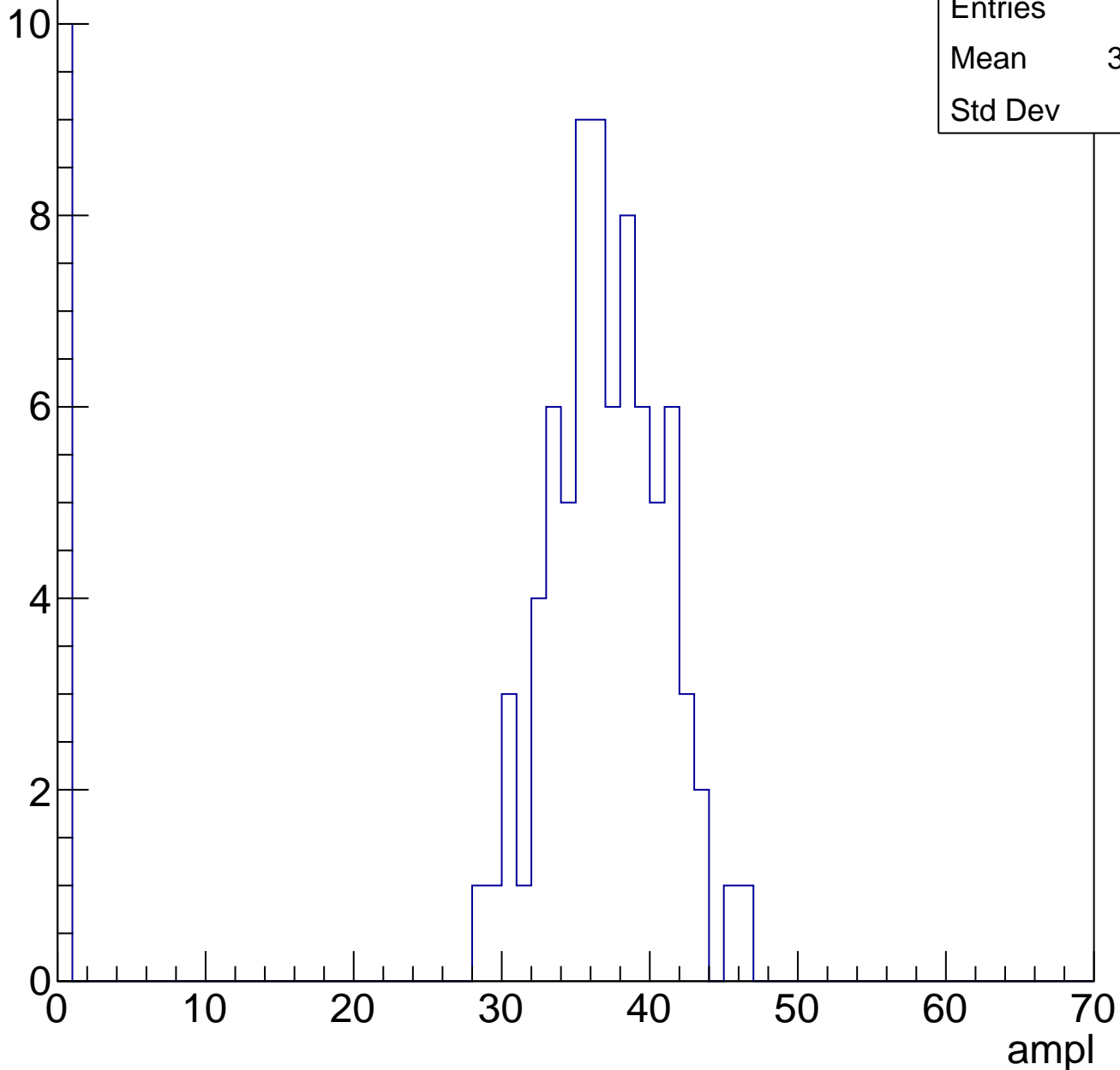


# B1L103S, U25-ch10, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	87
Mean	32.44
Std Dev	12.2

Entry

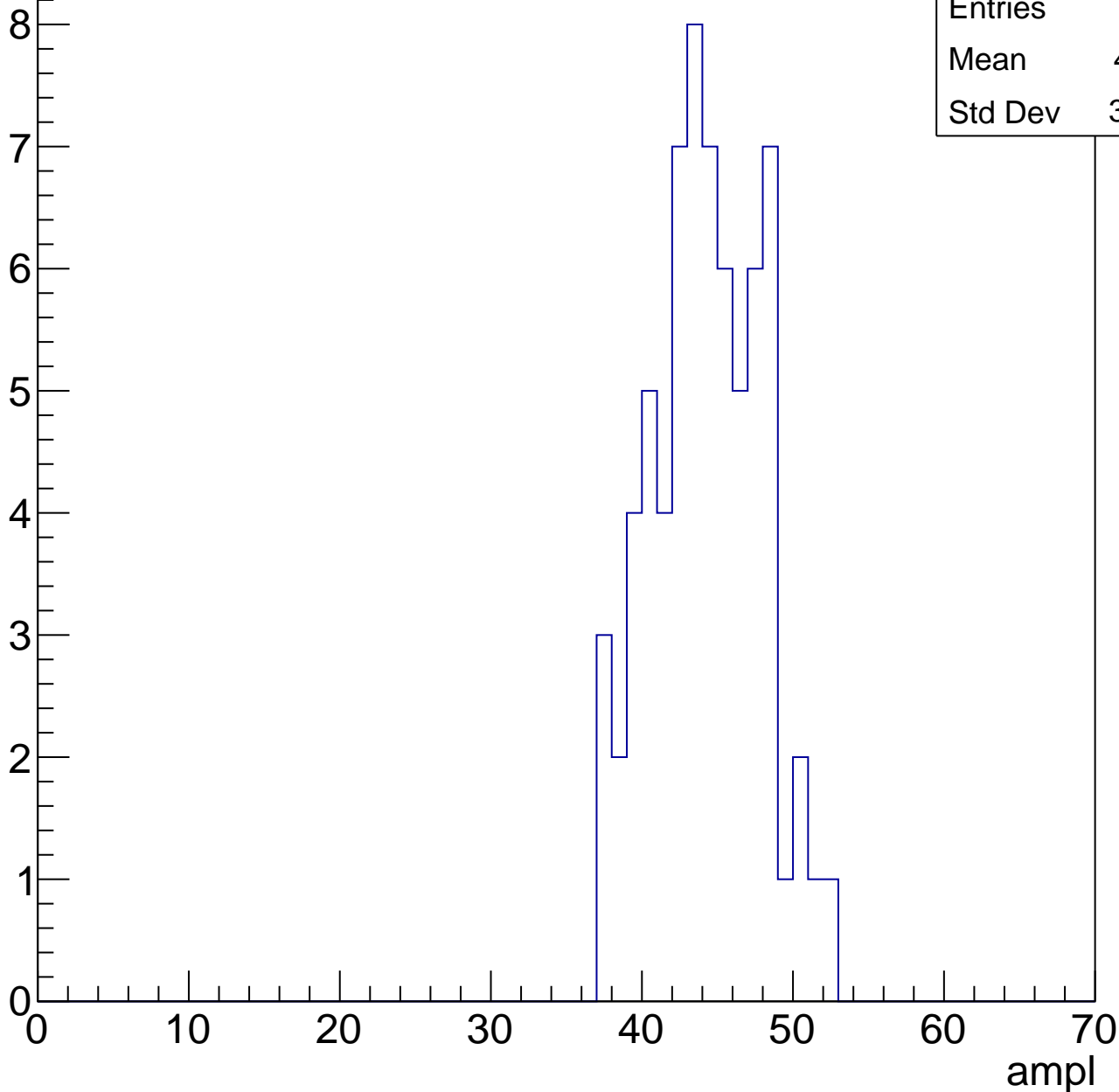


# B1L103S, U25-ch10, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	69
Mean	43.81
Std Dev	3.552

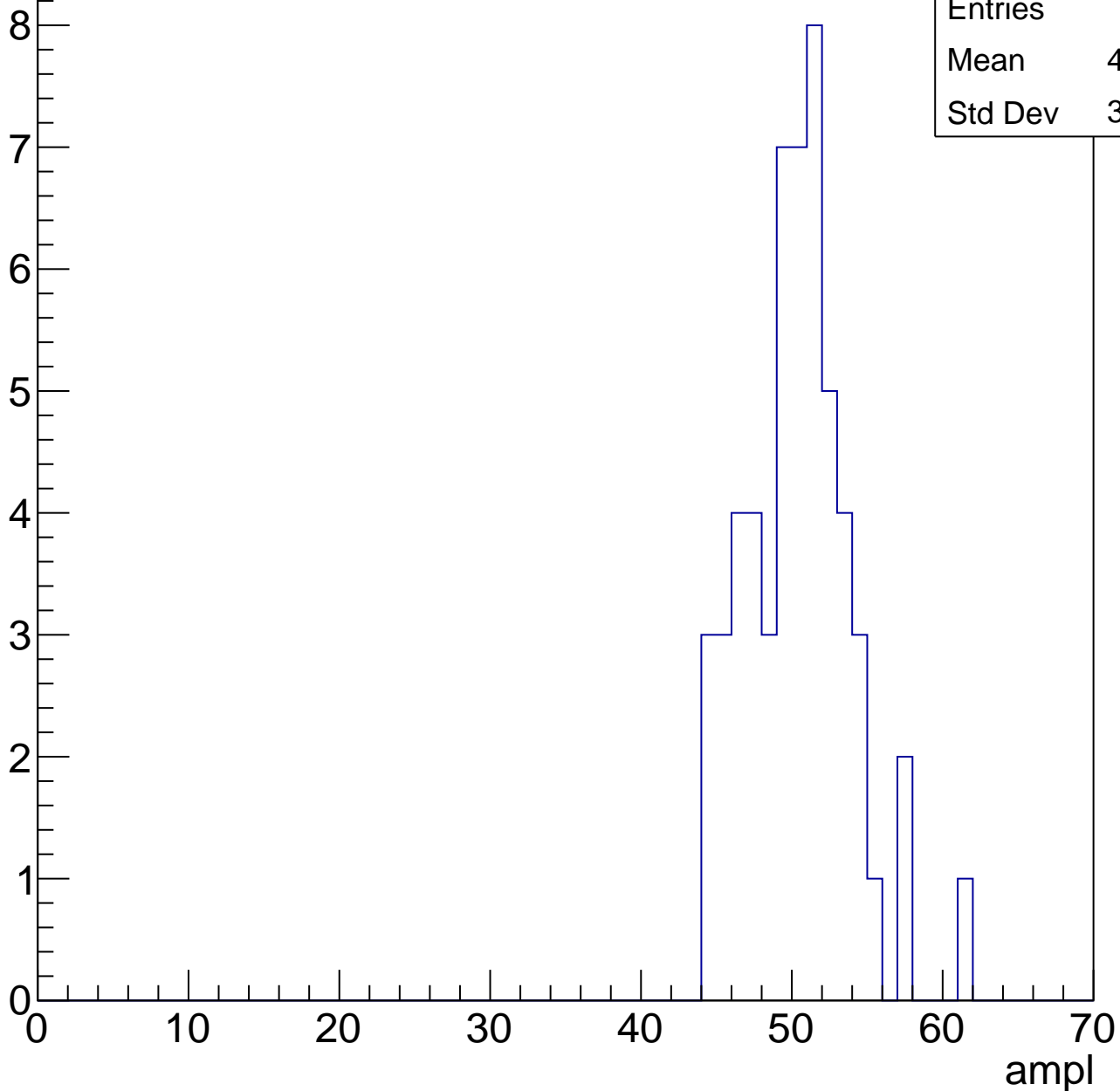


# B1L103S, U25-ch10, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	55
Mean	49.96
Std Dev	3.459



# B1L103S, U25-ch10, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

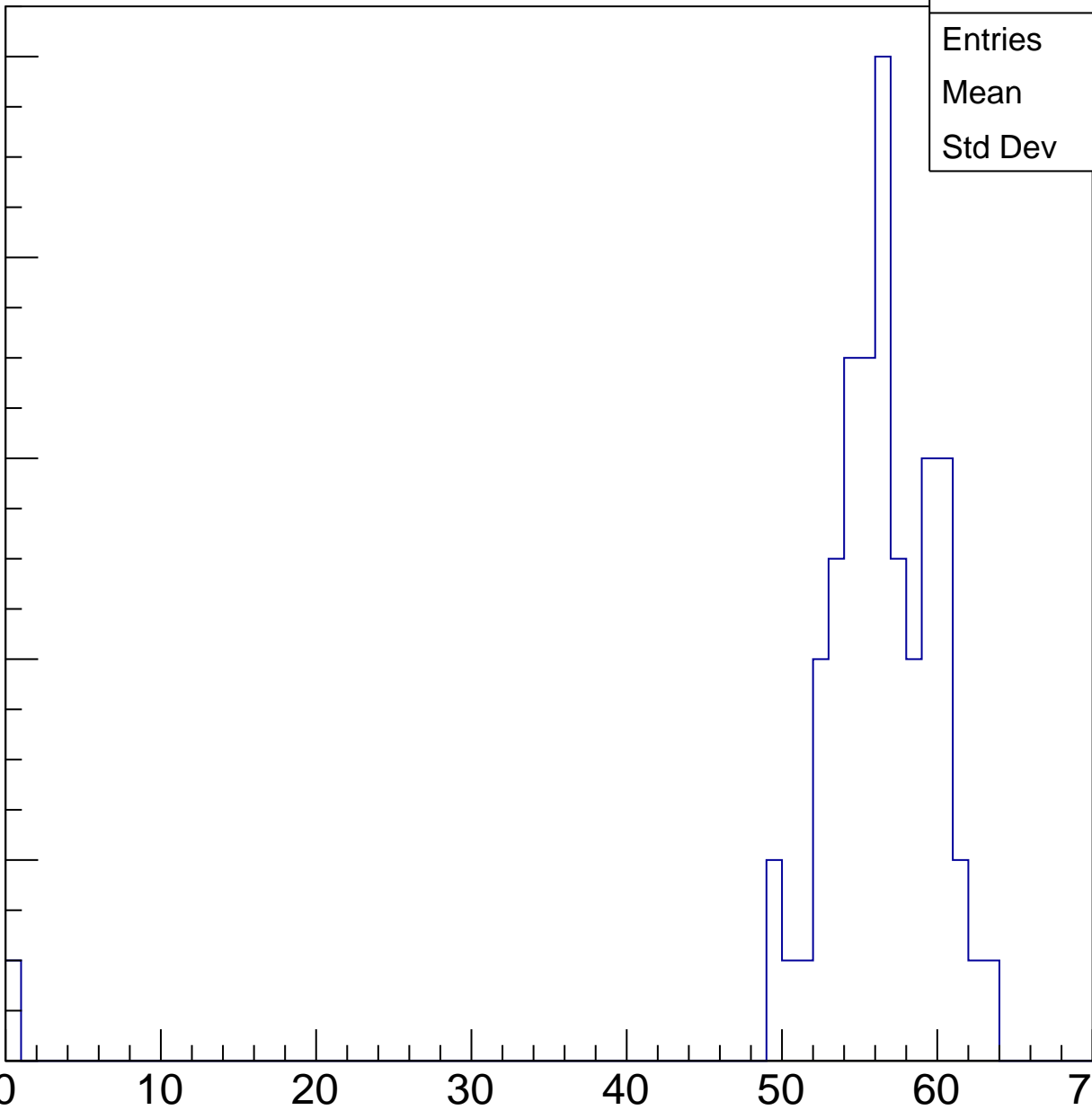
Entries	63
Mean	55.13
Std Dev	7.66

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

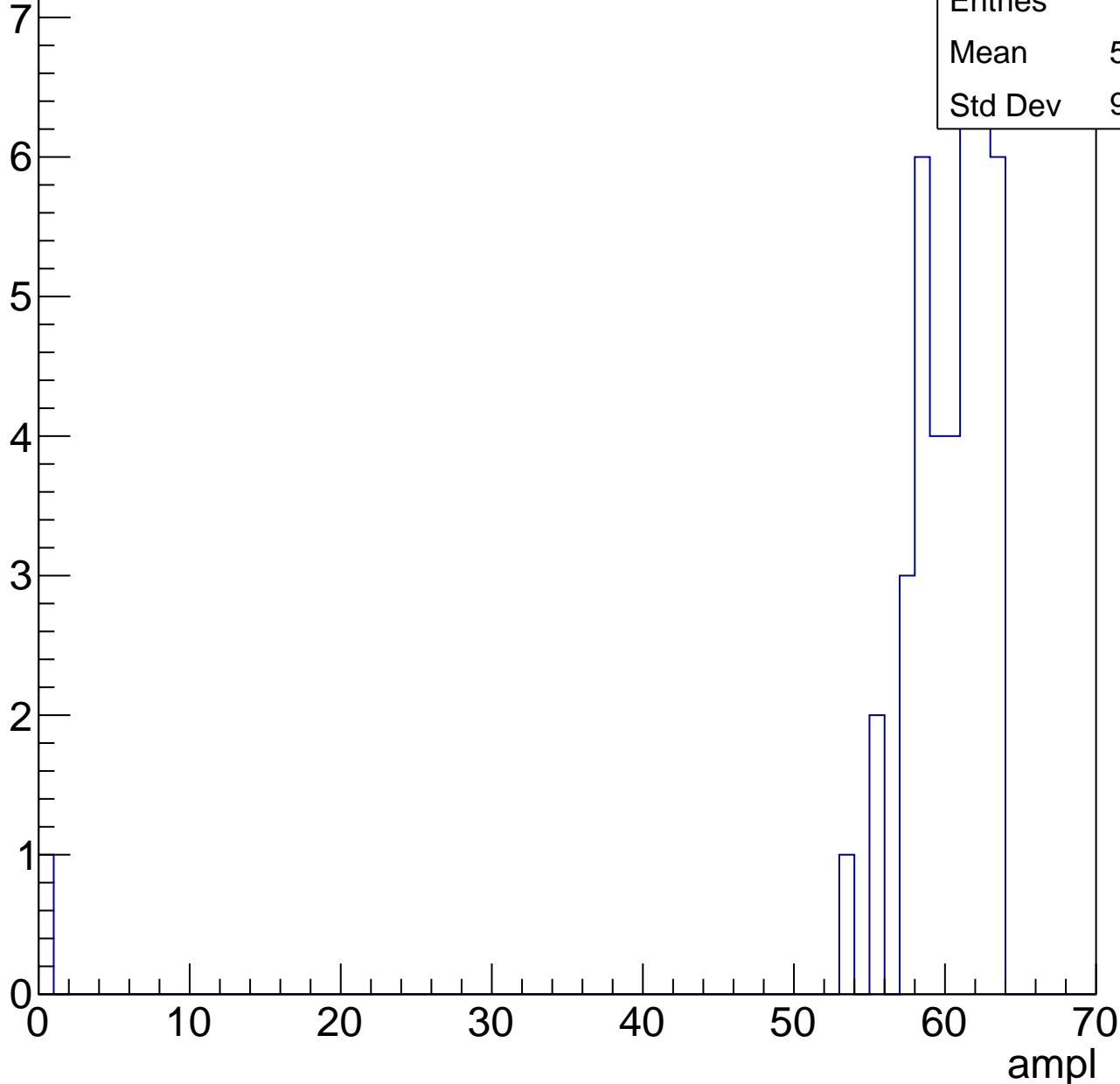


# B1L103S, U25-ch10, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	41
Mean	58.46
Std Dev	9.559



# B1L103S, U25-ch10, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U25-ch10, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

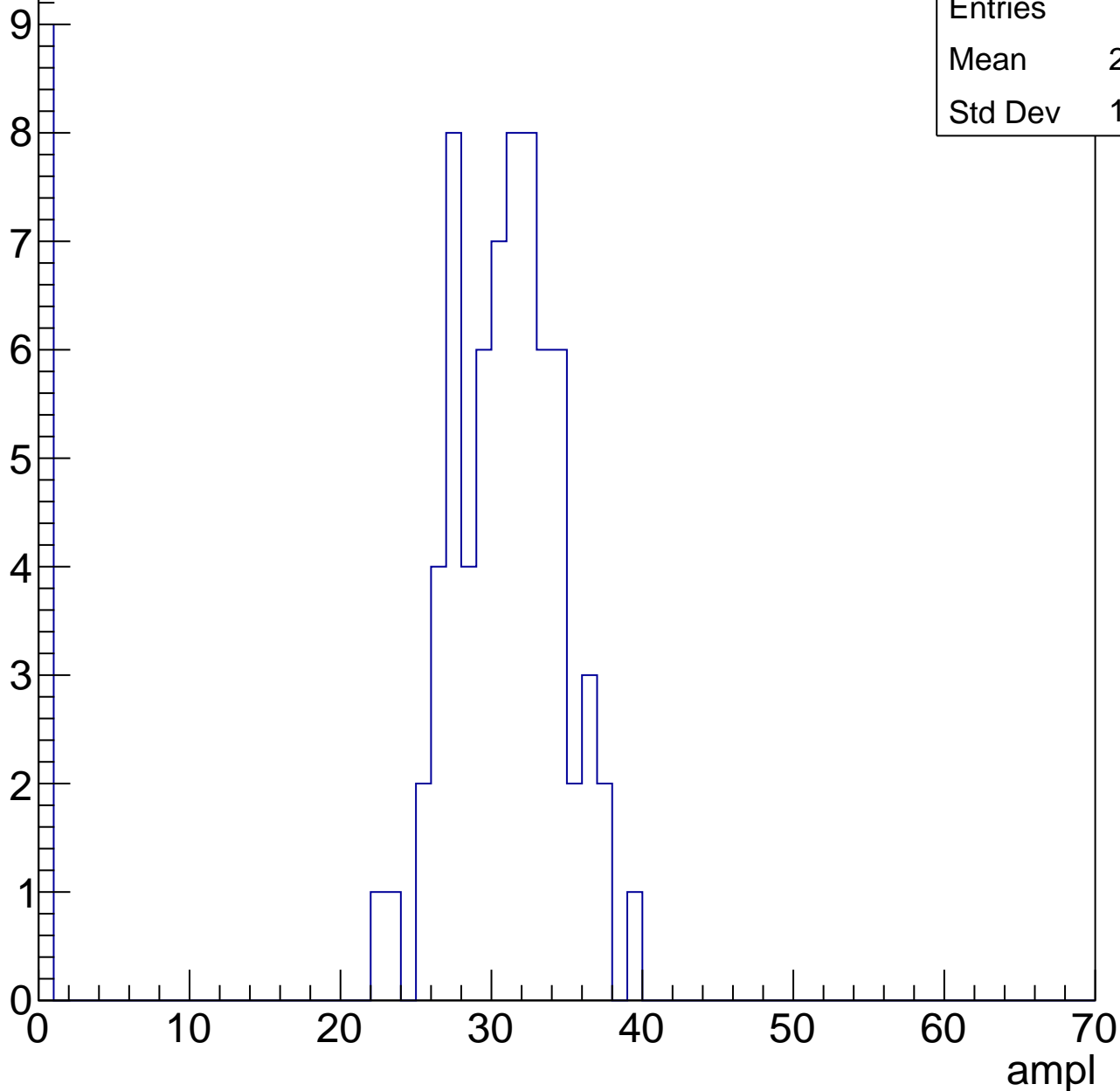


# B1L103S, U25-ch11, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

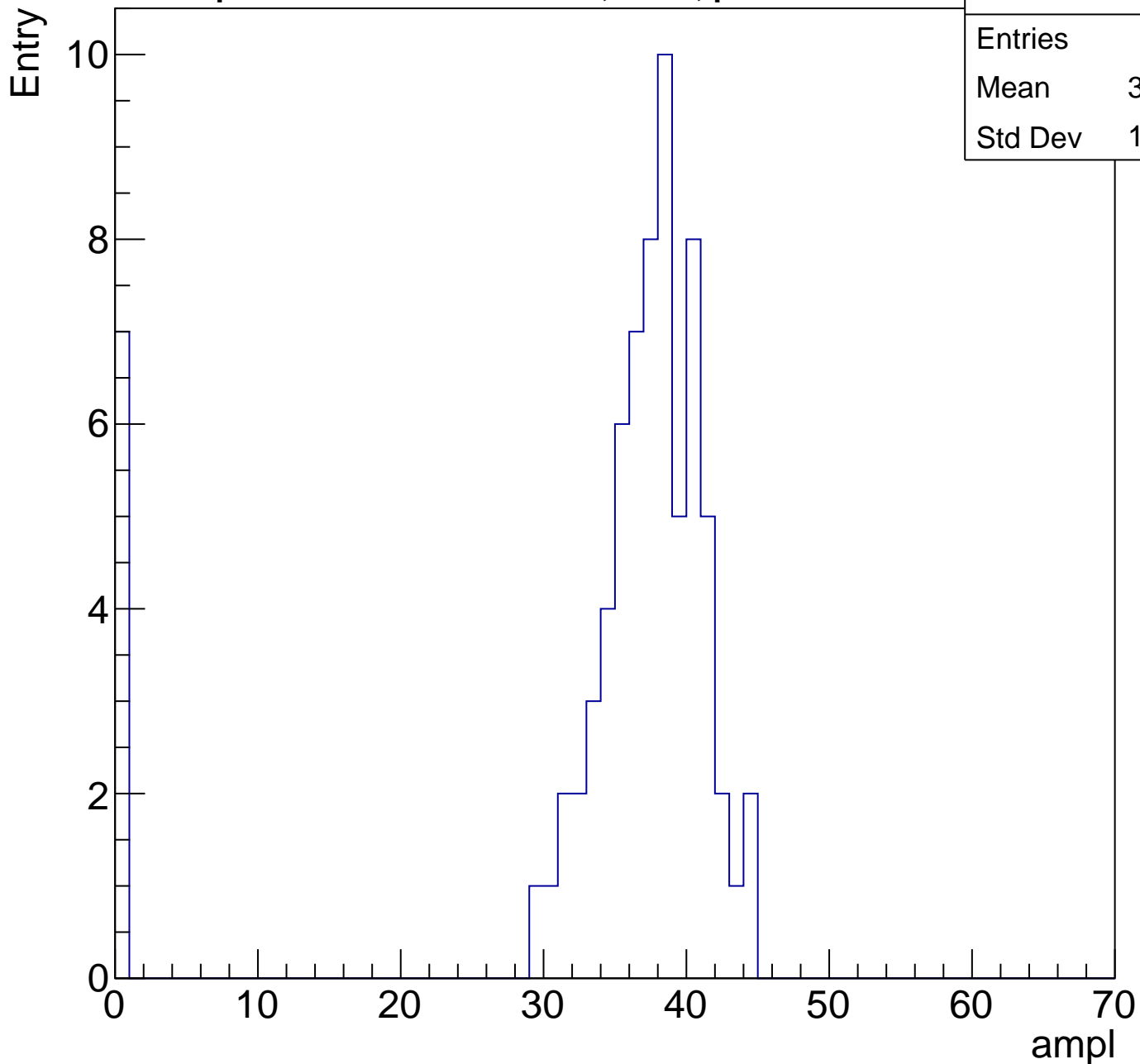
Entries	78
Mean	27.03
Std Dev	10.29



# B1L103S, U25-ch11, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	74
Mean	33.69
Std Dev	11.32

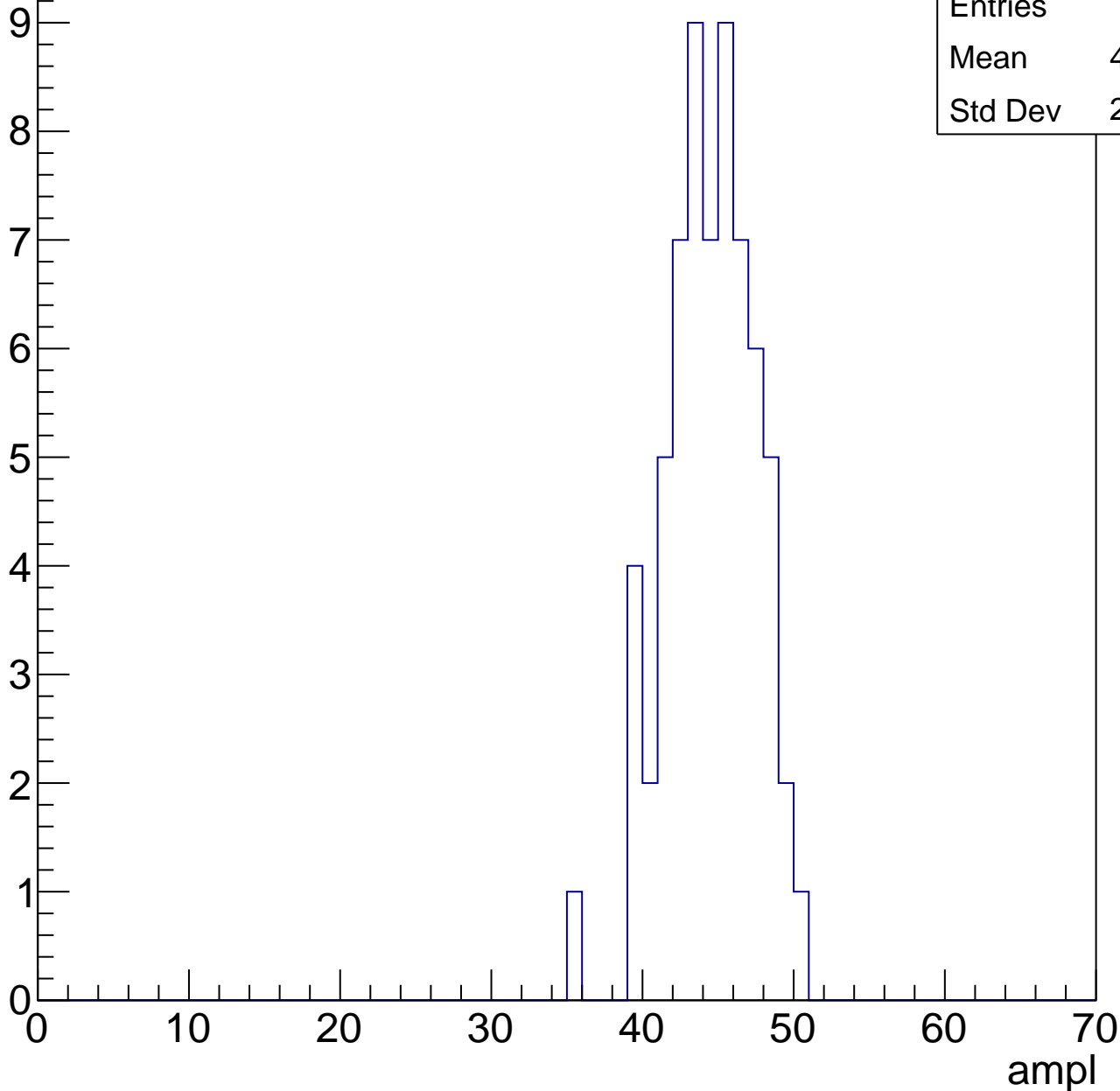


# B1L103S, U25-ch11, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	65
Mean	44.03
Std Dev	2.914

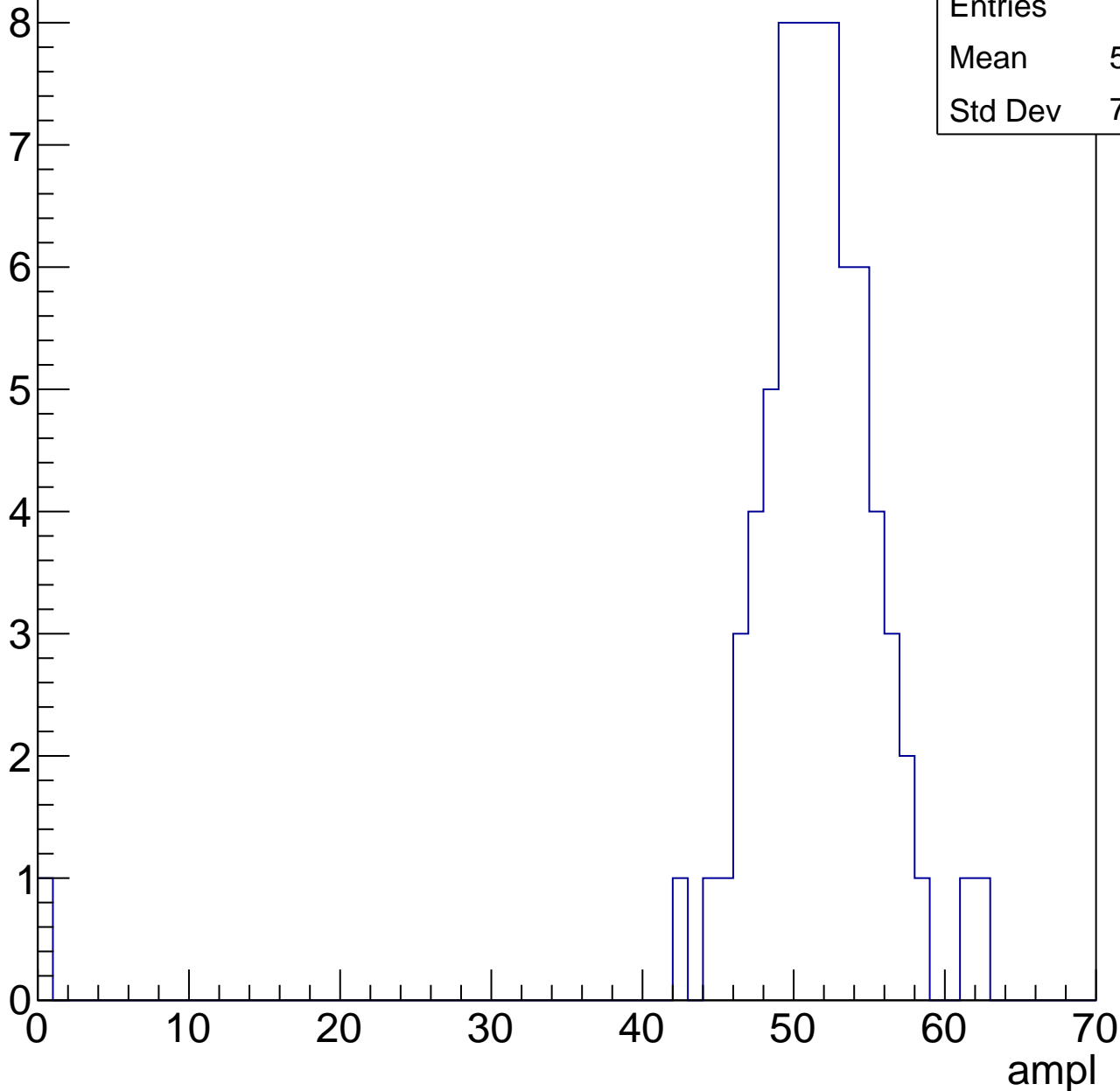


# B1L103S, U25-ch11, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	72
Mean	50.53
Std Dev	7.014

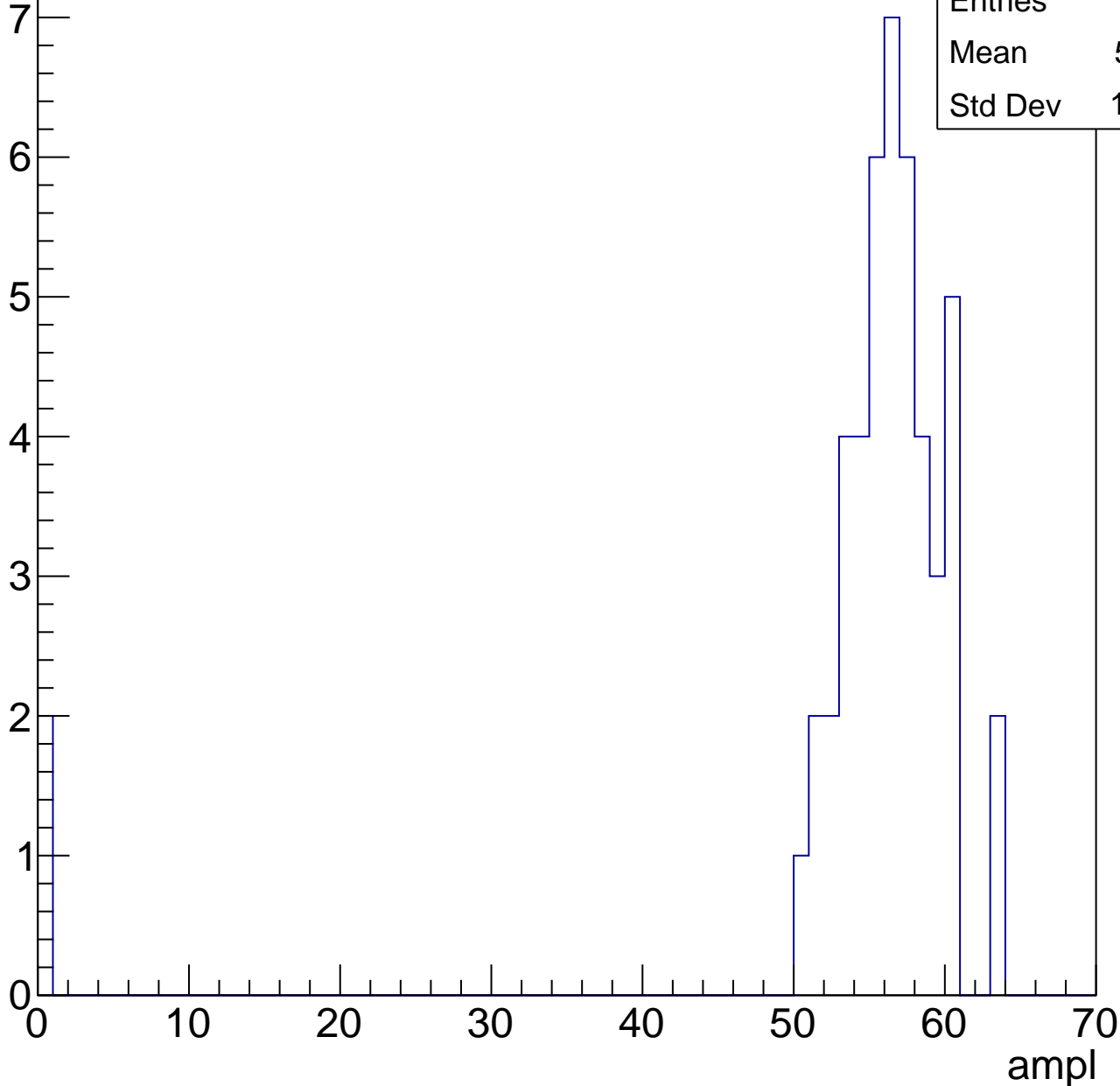


# B1L103S, U25-ch11, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	48
Mean	53.81
Std Dev	11.59

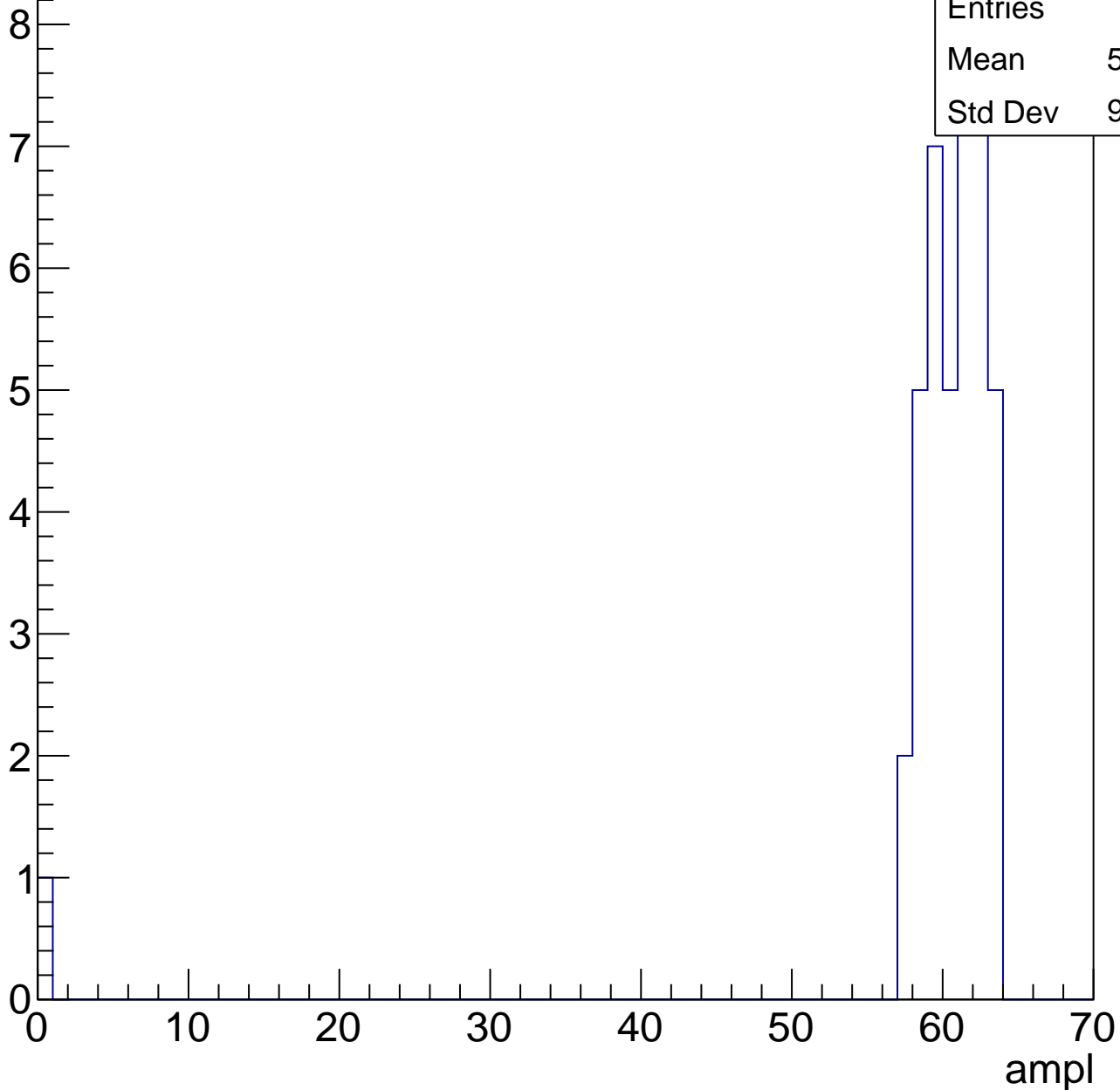


# B1L103S, U25-ch11, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	41
Mean	58.93
Std Dev	9.478



# B1L103S, U25-ch11, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	5
Mean	62.4
Std Dev	0.8



# B1L103S, U25-ch11, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

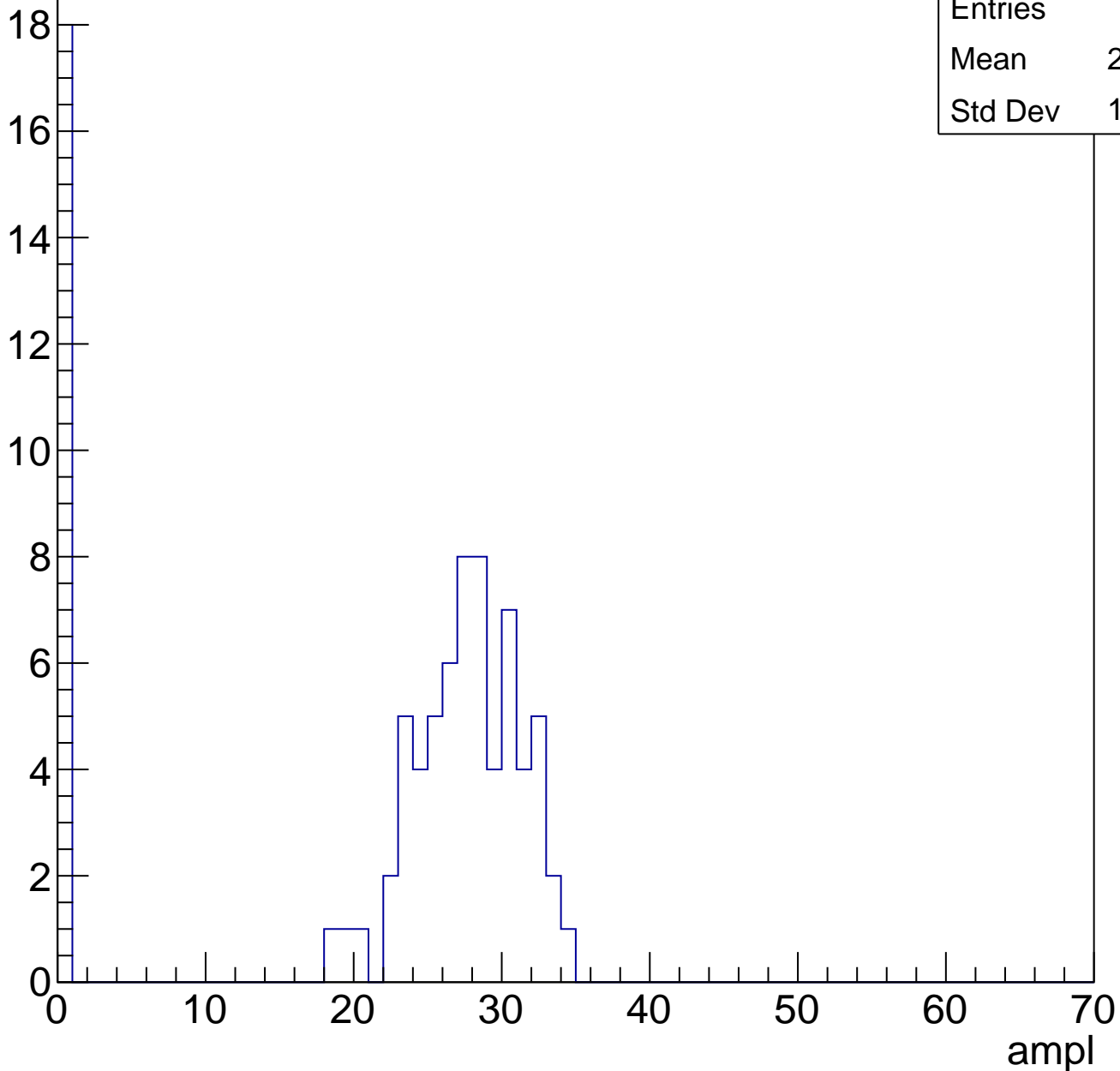
Entries	19
Mean	0
Std Dev	0

# B1L103S, U25-ch12, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	82
Mean	21.26
Std Dev	11.69

Entry

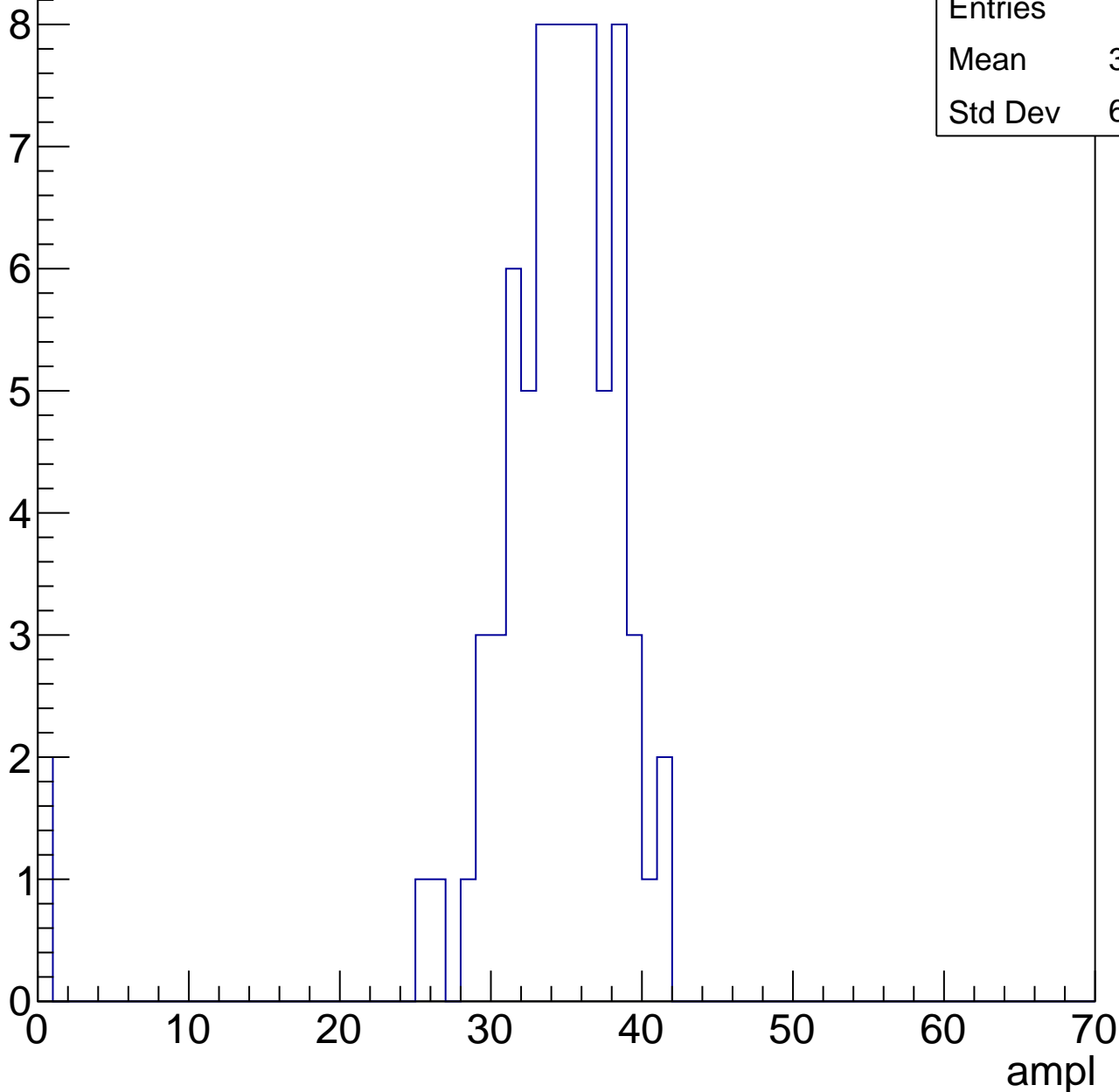


# B1L103S, U25-ch12, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

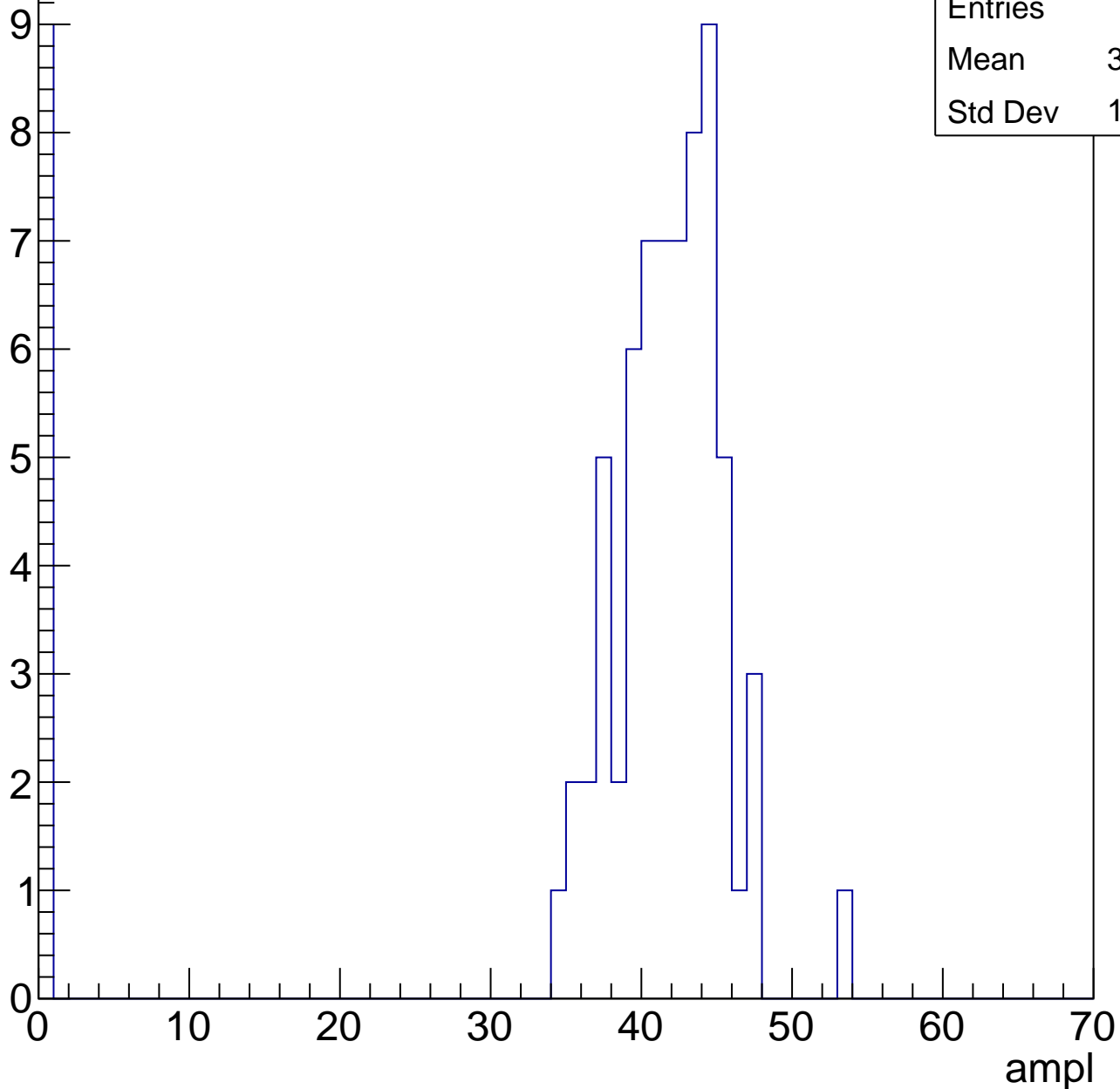
Entries	73
Mean	33.34
Std Dev	6.504



# B1L103S, U25-ch12, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U25-ch12, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

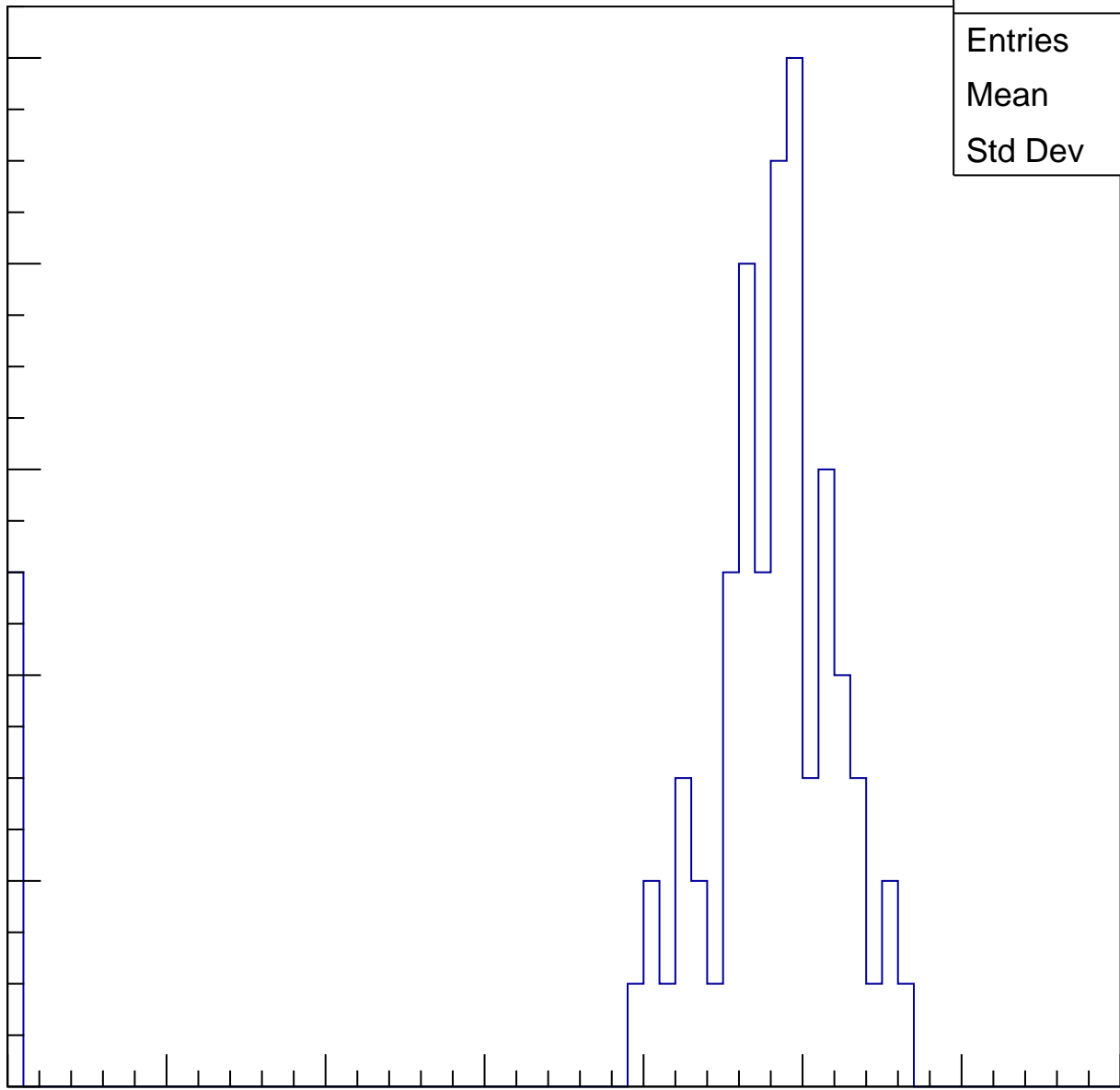
Entries	72
Mean	44.57
Std Dev	12.69

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

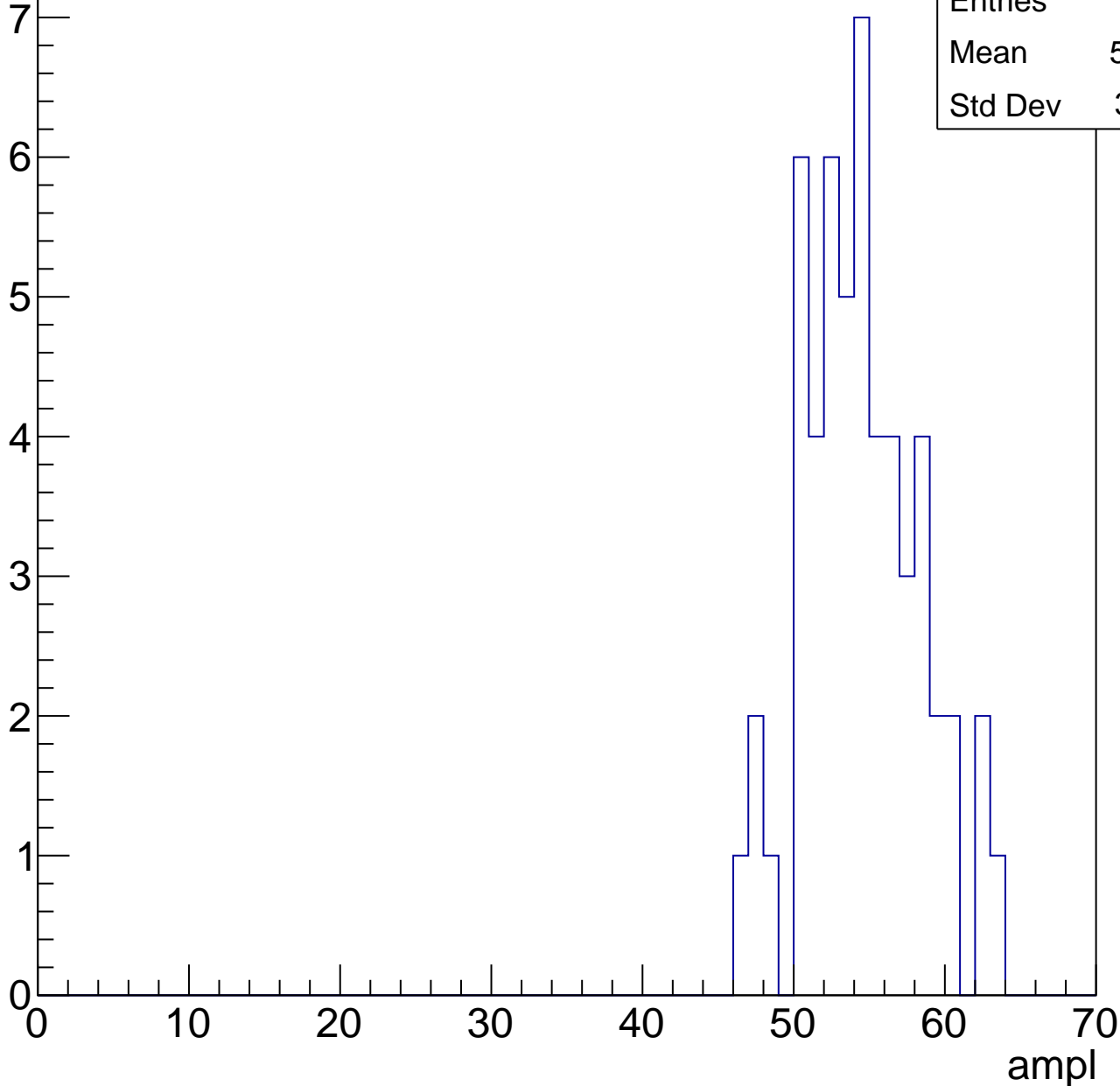


# B1L103S, U25-ch12, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

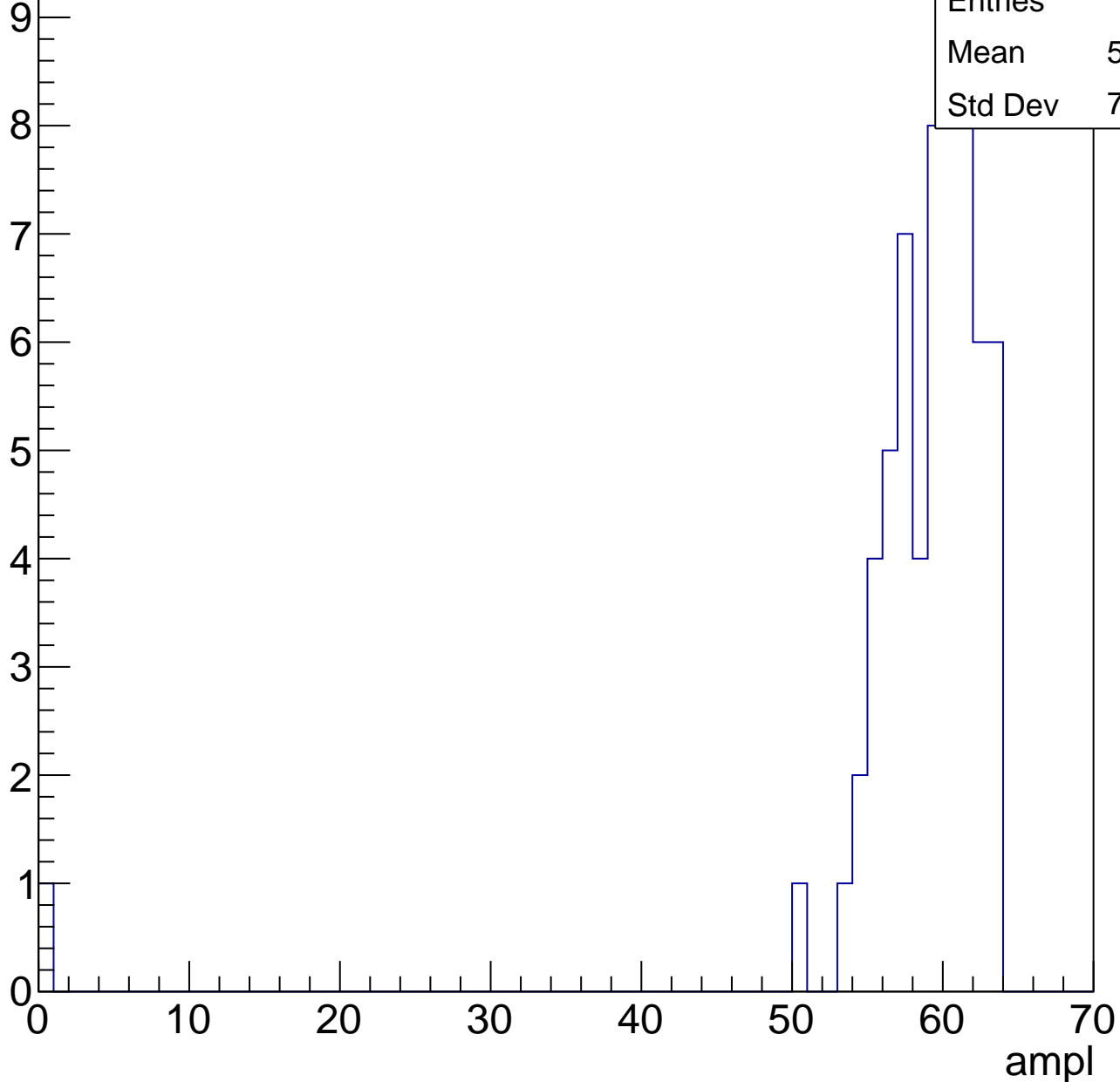
Entries	54
Mean	54.06
Std Dev	3.851



# B1L103S, U25-ch12, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

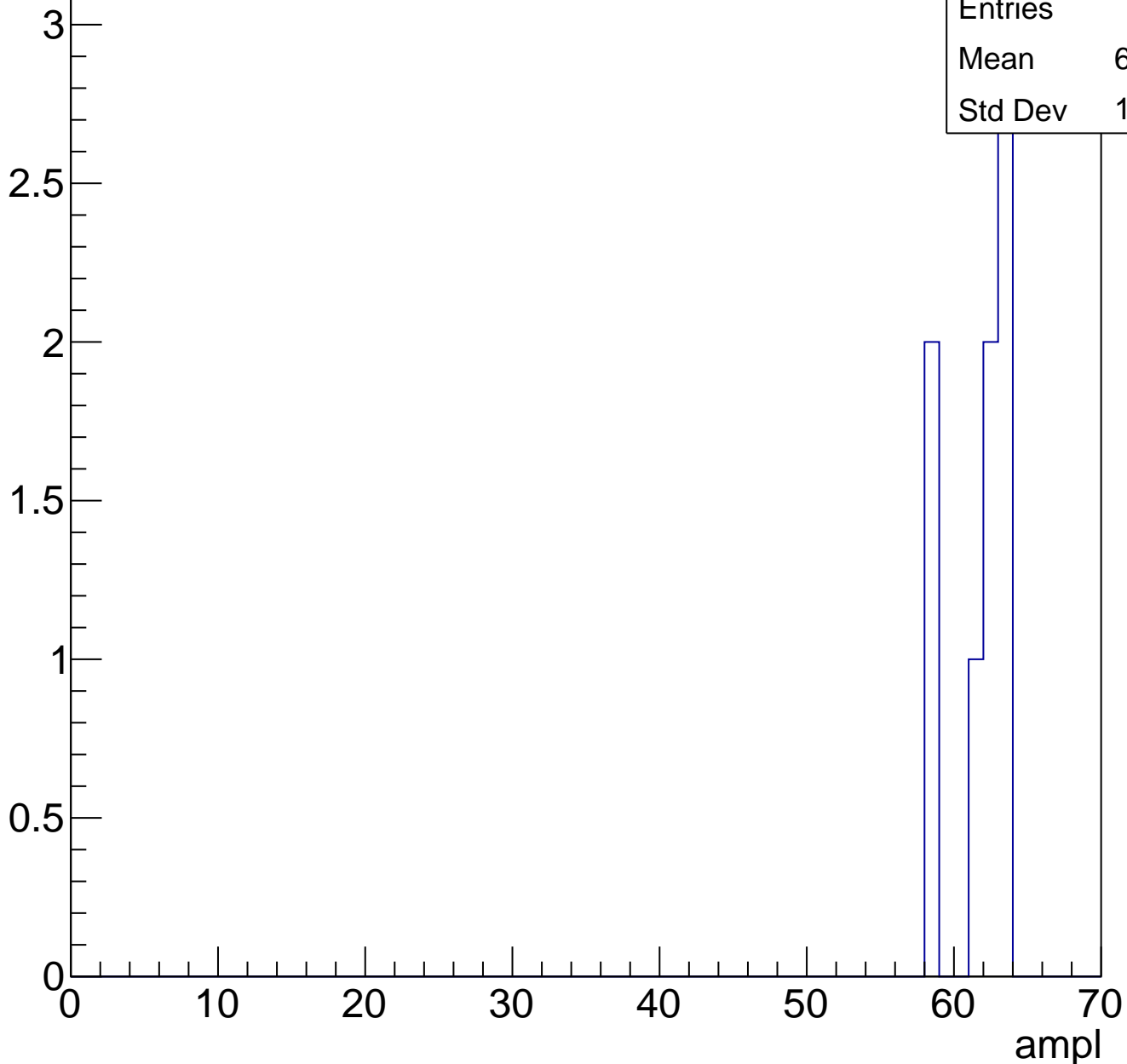
Entry



# B1L103S, U25-ch12, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U25-ch12, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Entries	19
Mean	0
Std Dev	0

ampl

# B1L103S, U25-ch13, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	86
Mean	26.5
Std Dev	10.54

Entry

10

8

6

4

2

0

ampl

0

10

20

30

40

50

60

70

B1L103S, U25-ch13, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	86
Mean	26.5
Std Dev	10.54

Entry

10

8

6

4

2

0

ampl

0

10

20

30

40

50

60

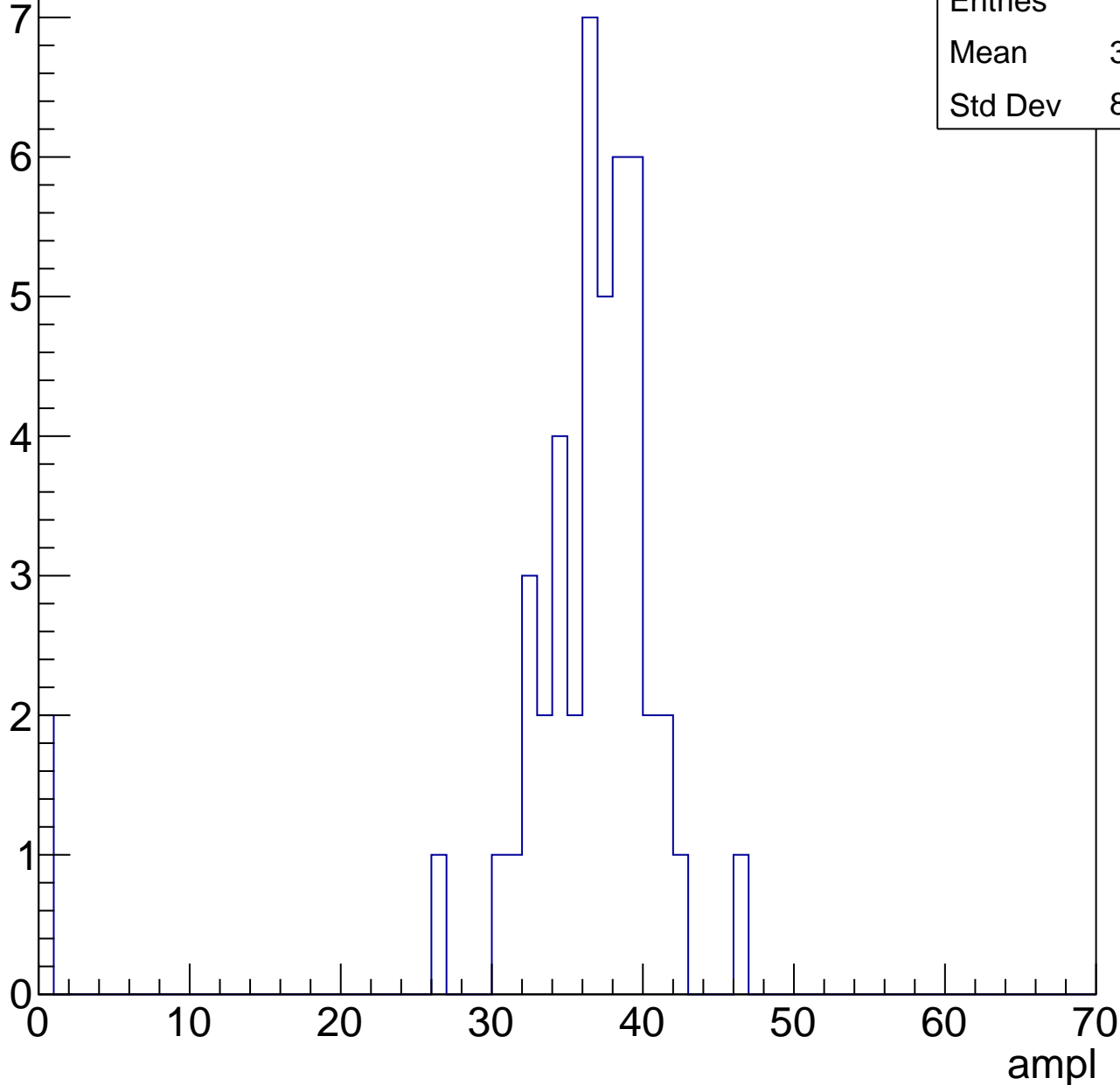
70

# B1L103S, U25-ch13, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	46
Mean	34.87
Std Dev	8.182

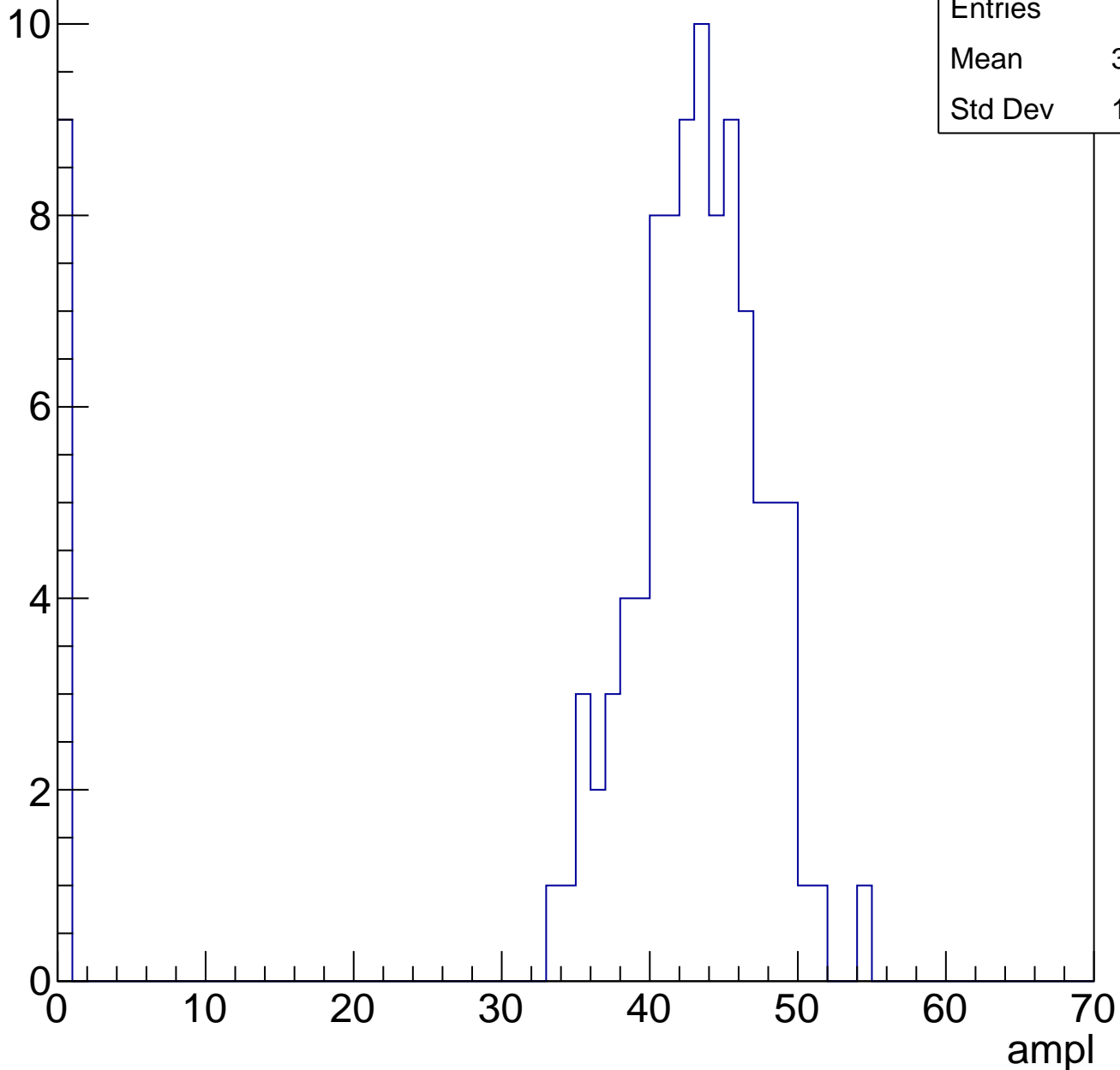


# B1L103S, U25-ch13, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	104
Mean	39.16
Std Dev	12.67

Entry

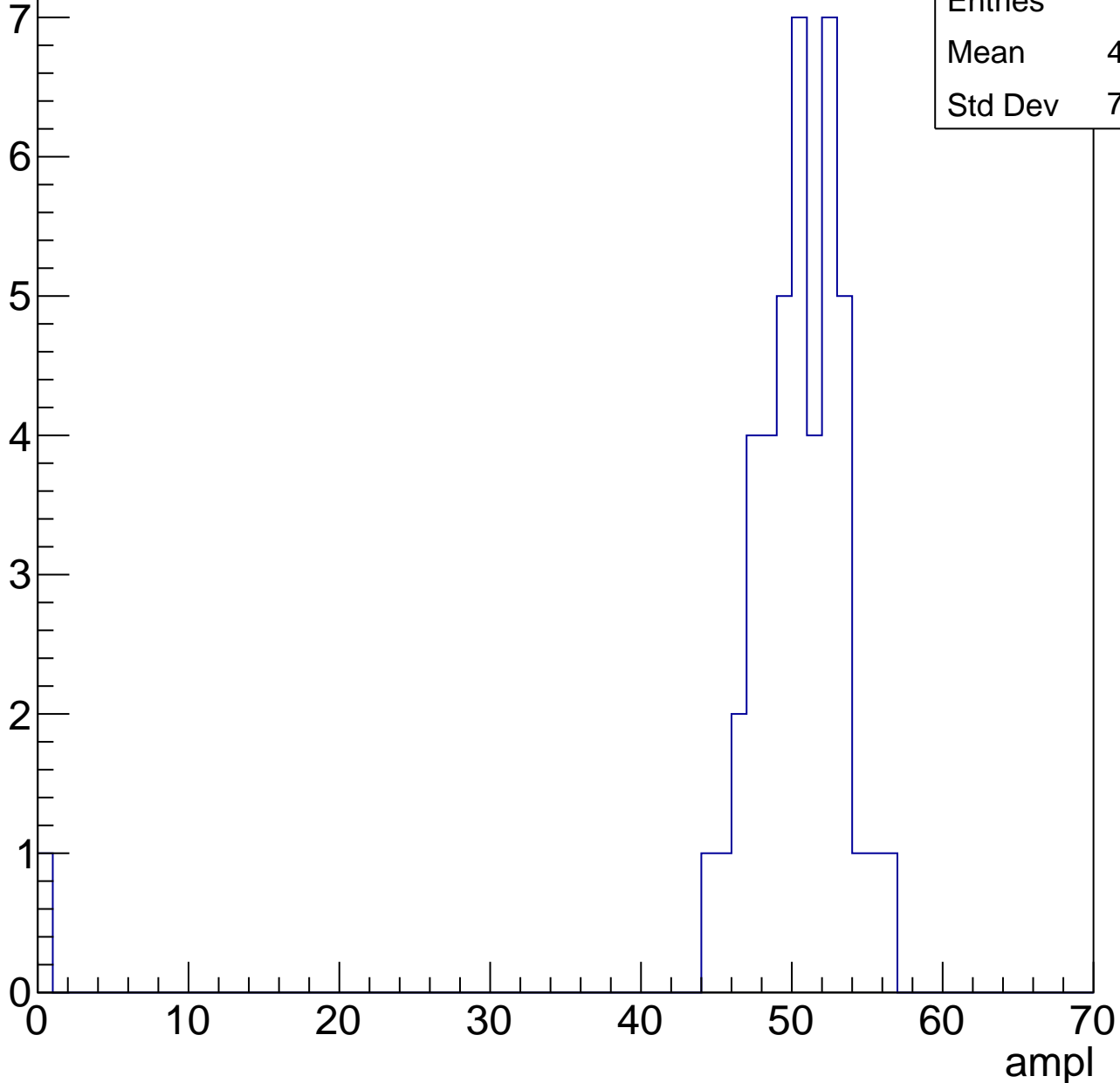


# B1L103S, U25-ch13, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	44
Mean	48.95
Std Dev	7.914

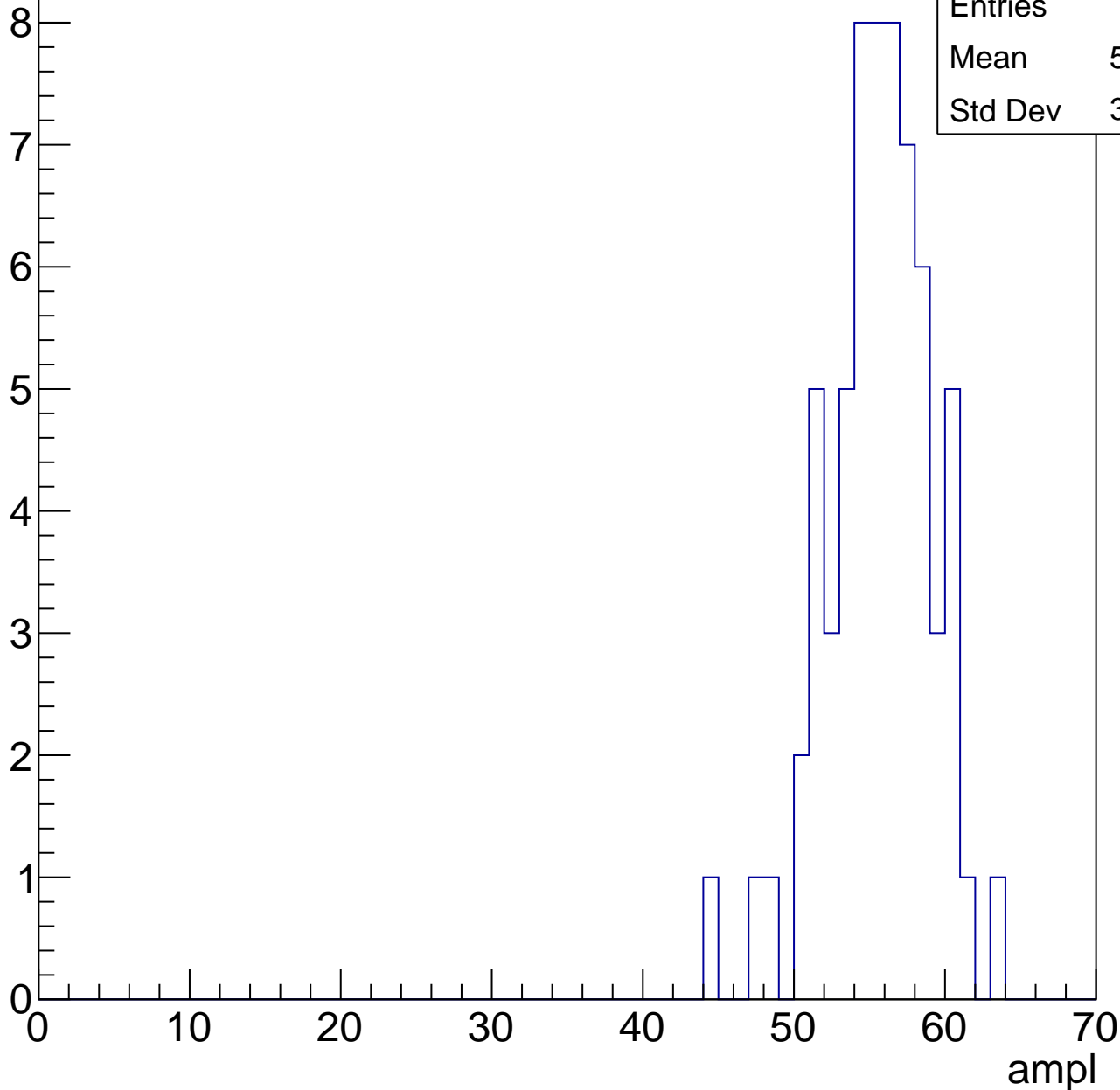


# B1L103S, U25-ch13, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	65
Mean	55.12
Std Dev	3.466

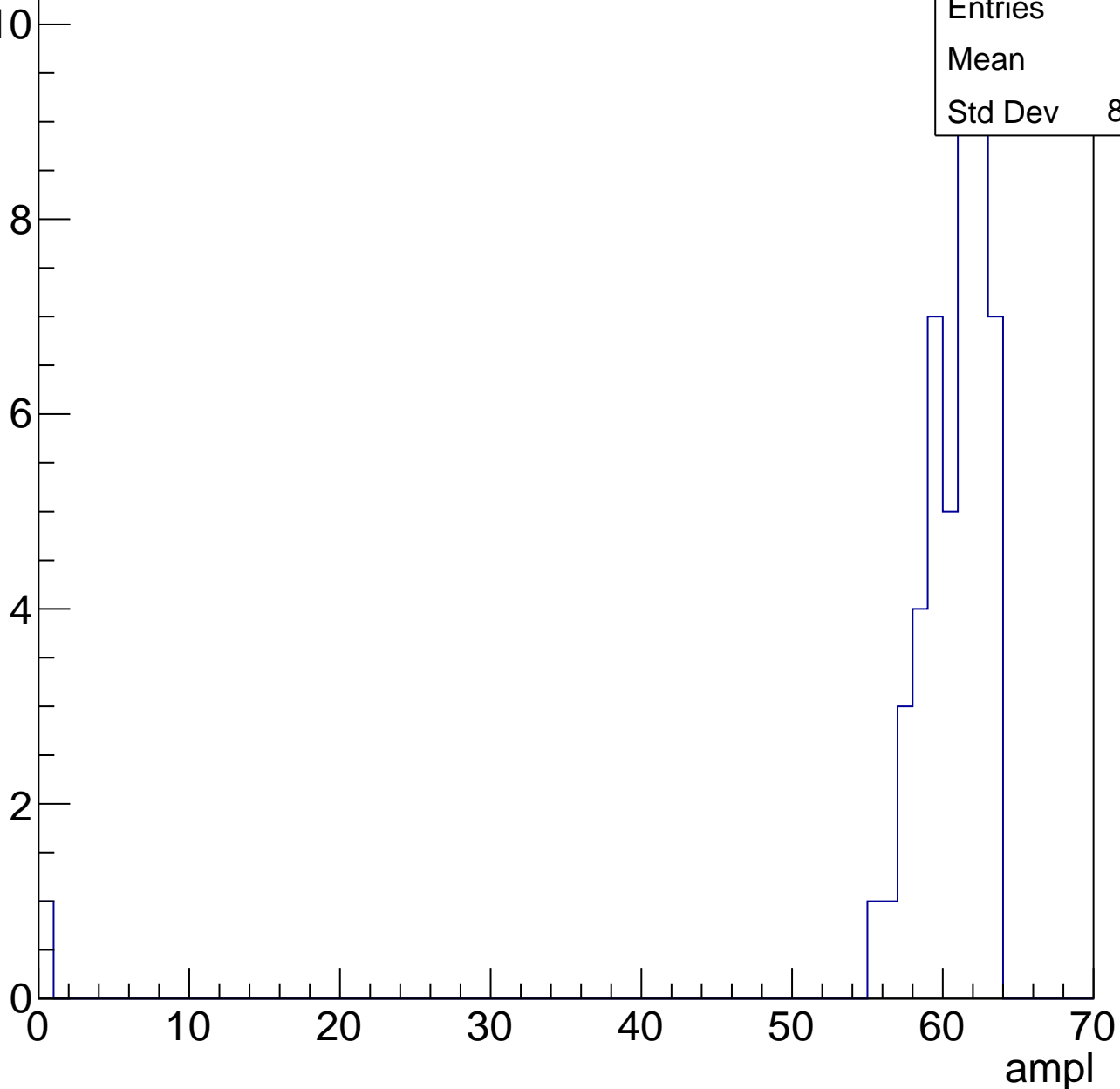


# B1L103S, U25-ch13, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	48
Mean	59.1
Std Dev	8.856



# B1L103S, U25-ch13, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U25-ch13, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

# B1L103S, U25-ch14, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	98
Mean	25.26
Std Dev	10.36

Entry

12

10

8

6

4

2

0

0

10

20

30

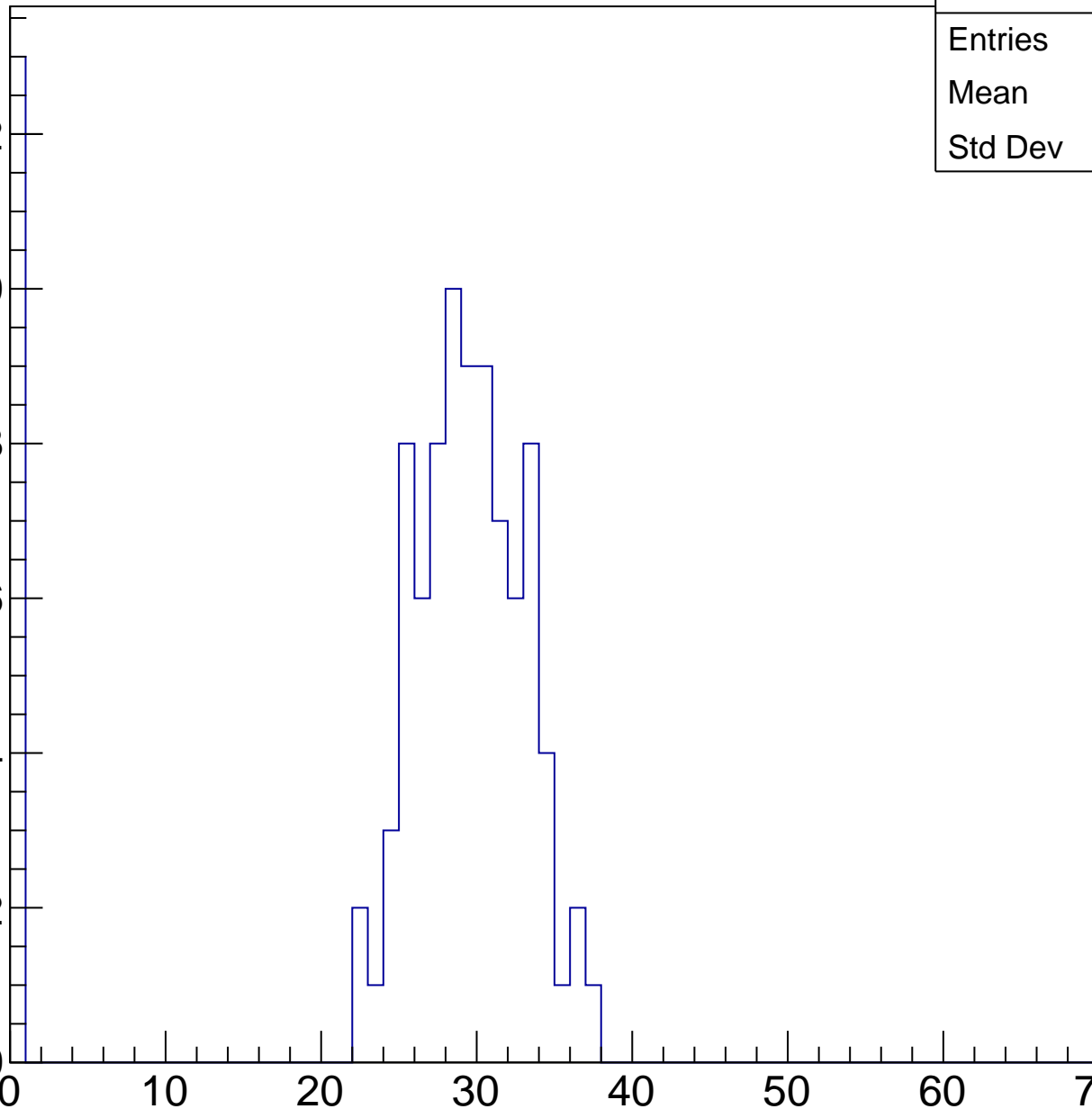
40

50

60

70

ampl

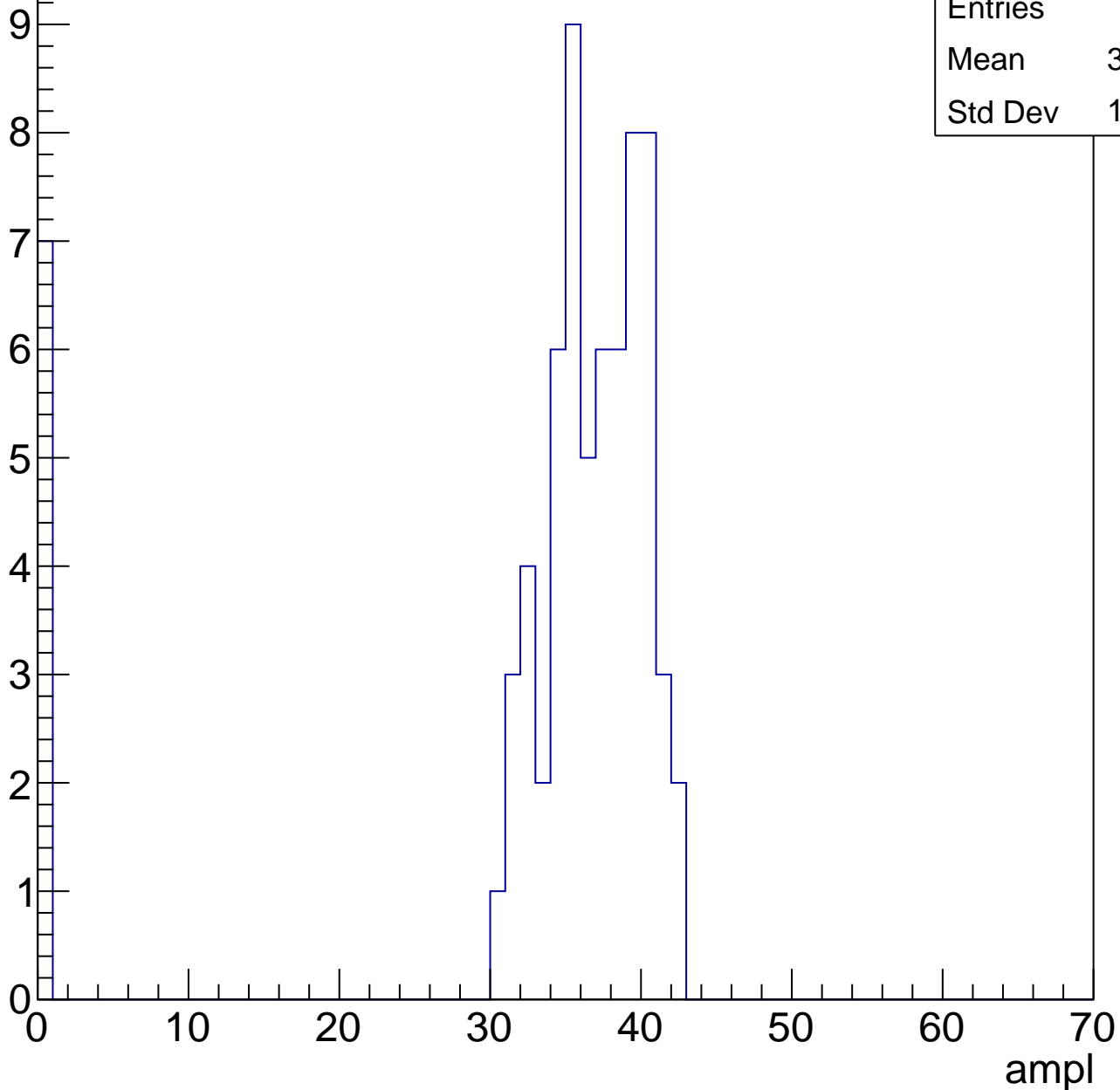


# B1L103S, U25-ch14, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	70
Mean	32.93
Std Dev	11.35

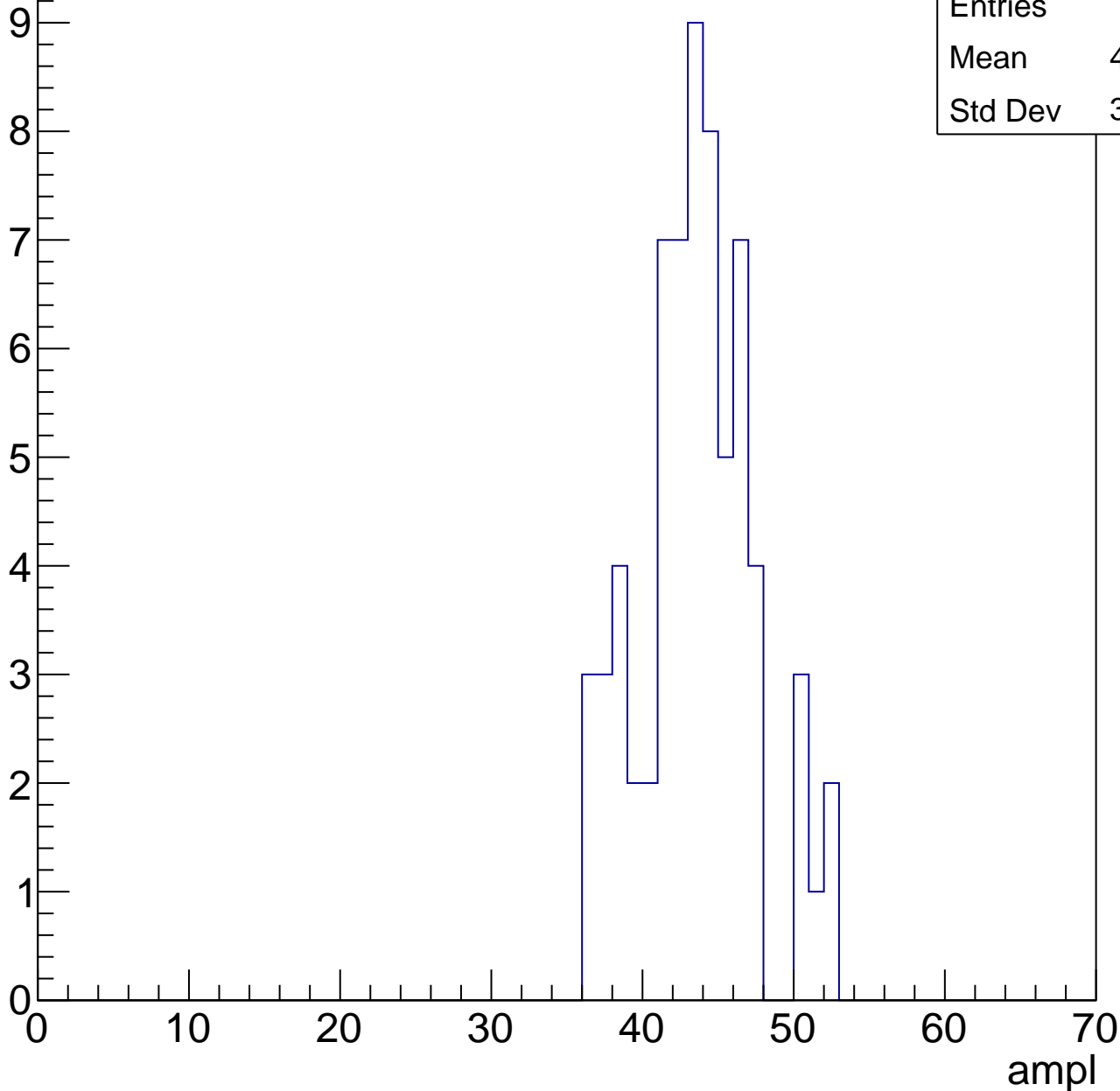


# B1L103S, U25-ch14, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	67
Mean	43.12
Std Dev	3.799



# B1L103S, U25-ch14, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

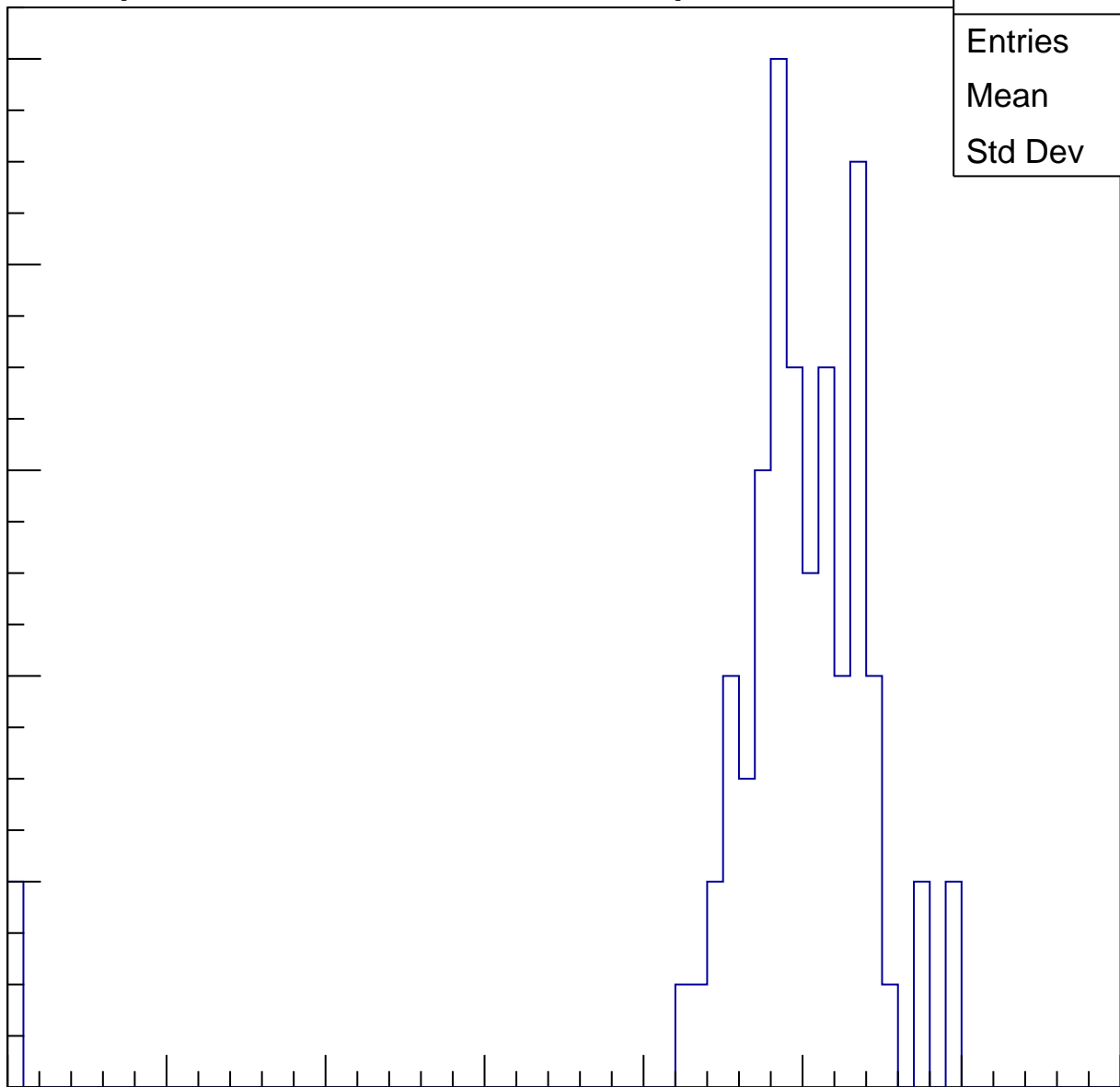
Entries	70
Mean	48.44
Std Dev	9.037

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

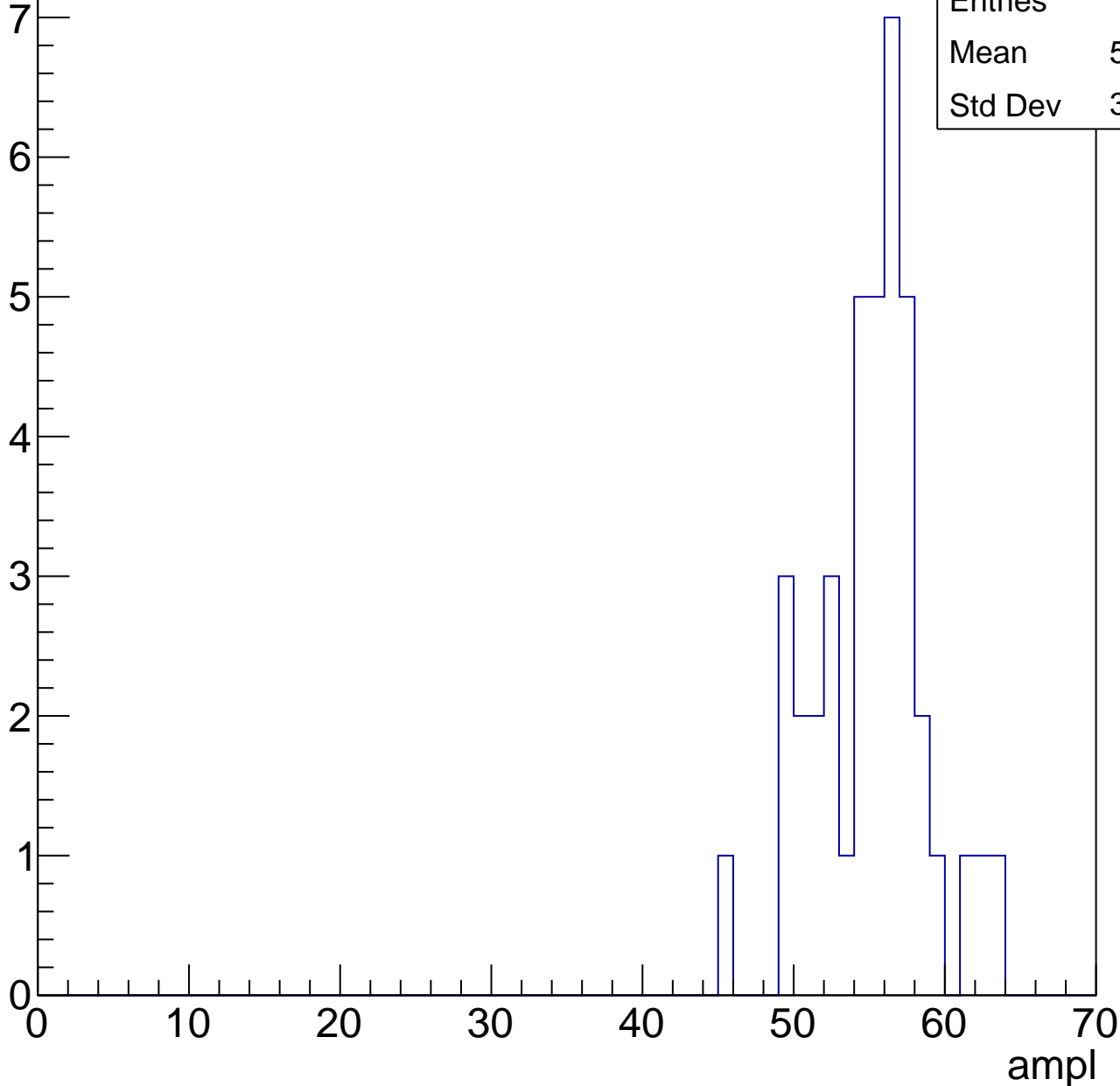


# B1L103S, U25-ch14, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	40
Mean	54.65
Std Dev	3.644

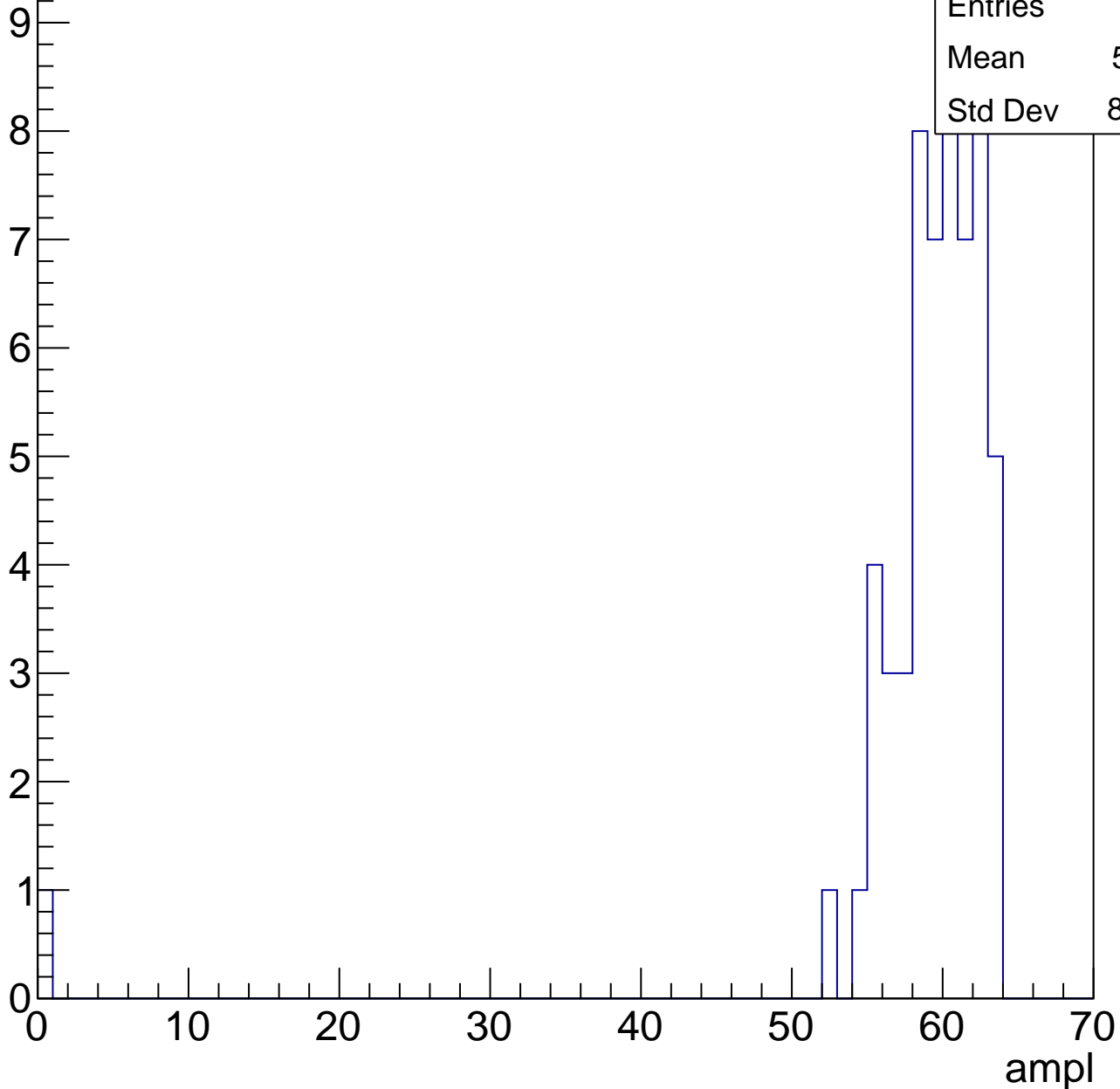


# B1L103S, U25-ch14, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

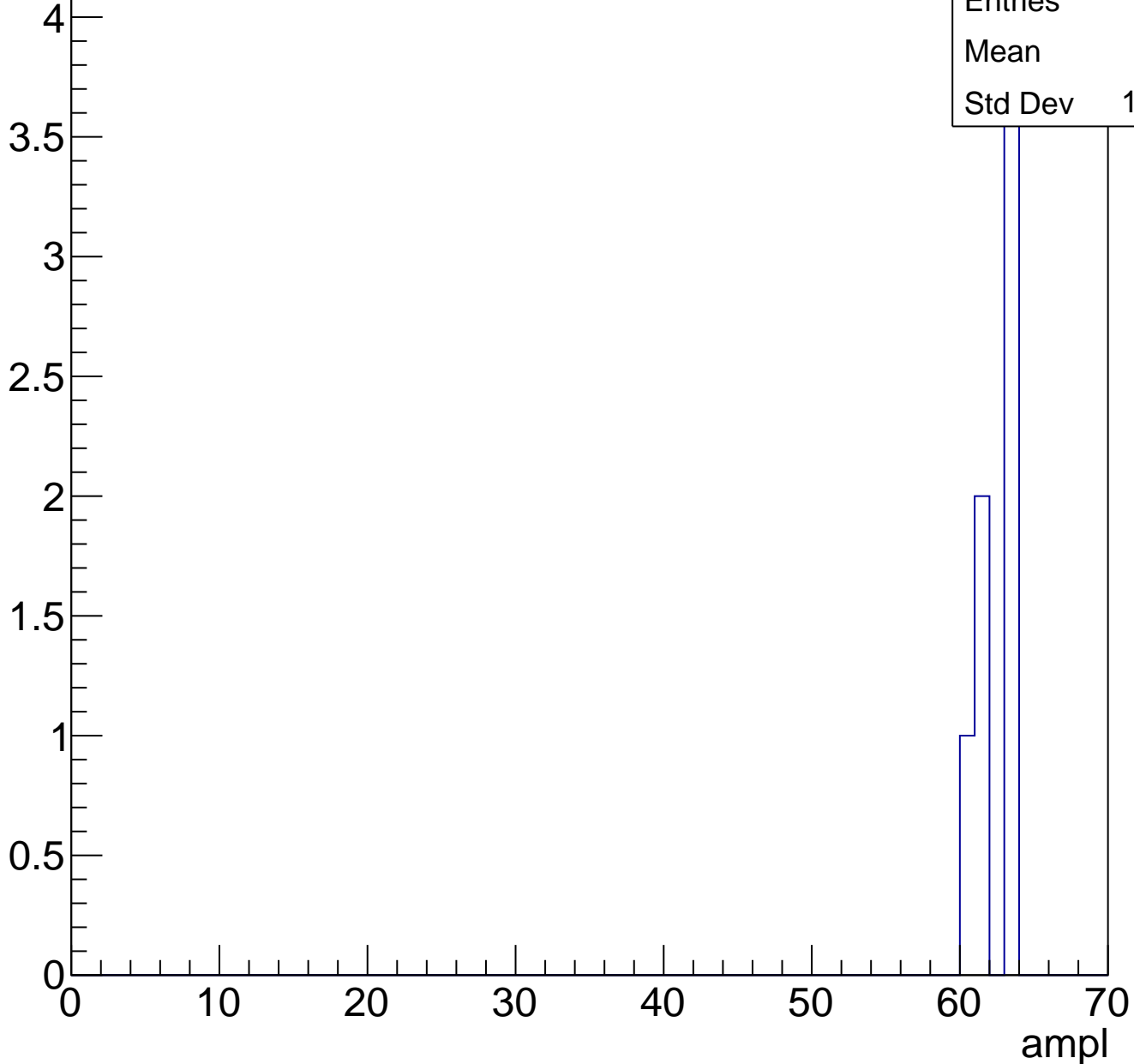
Entries	58
Mean	58.31
Std Dev	8.133



# B1L103S, U25-ch14, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



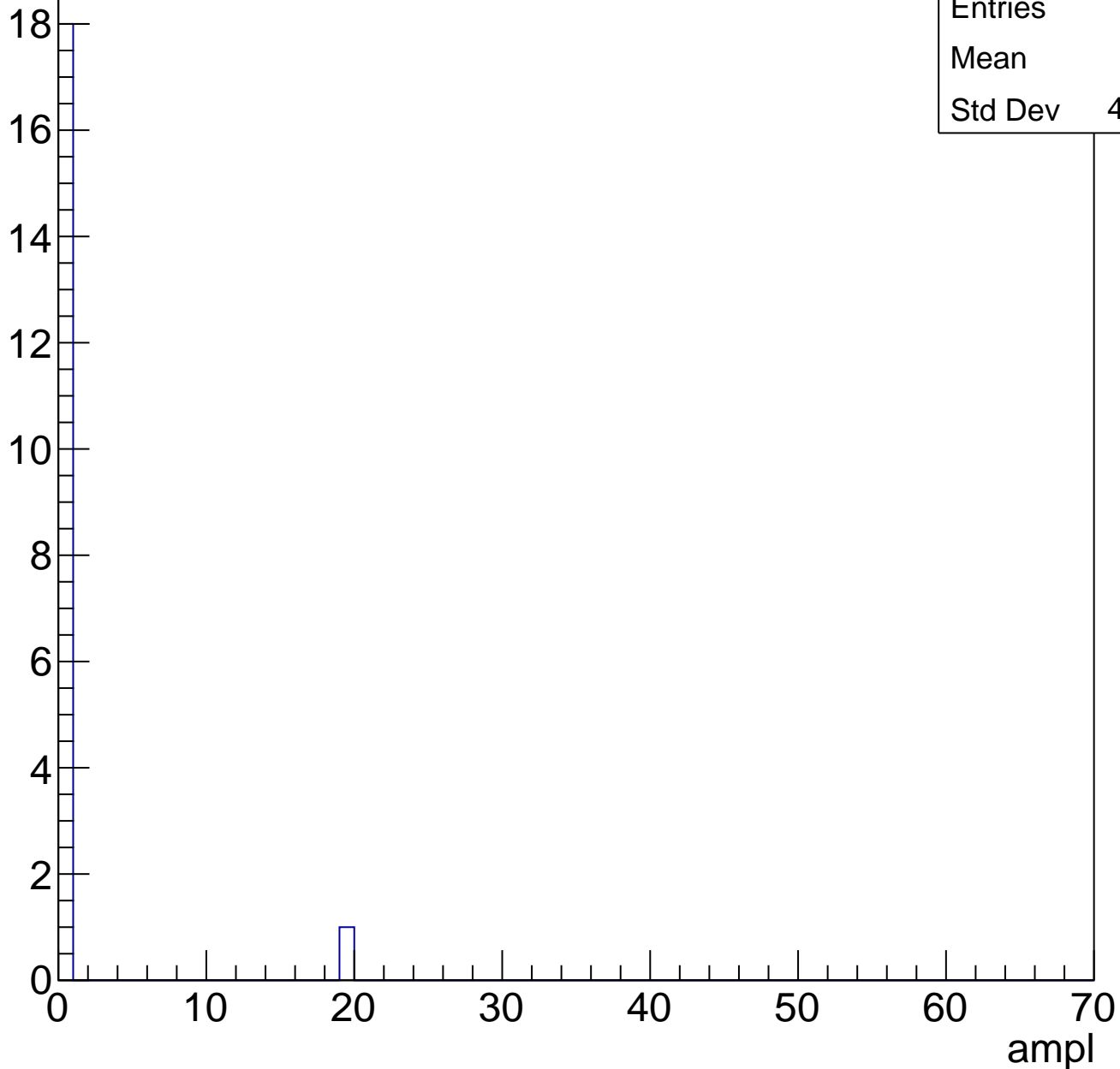


# B1L103S, U25-ch14, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	19
Mean	1
Std Dev	4.243

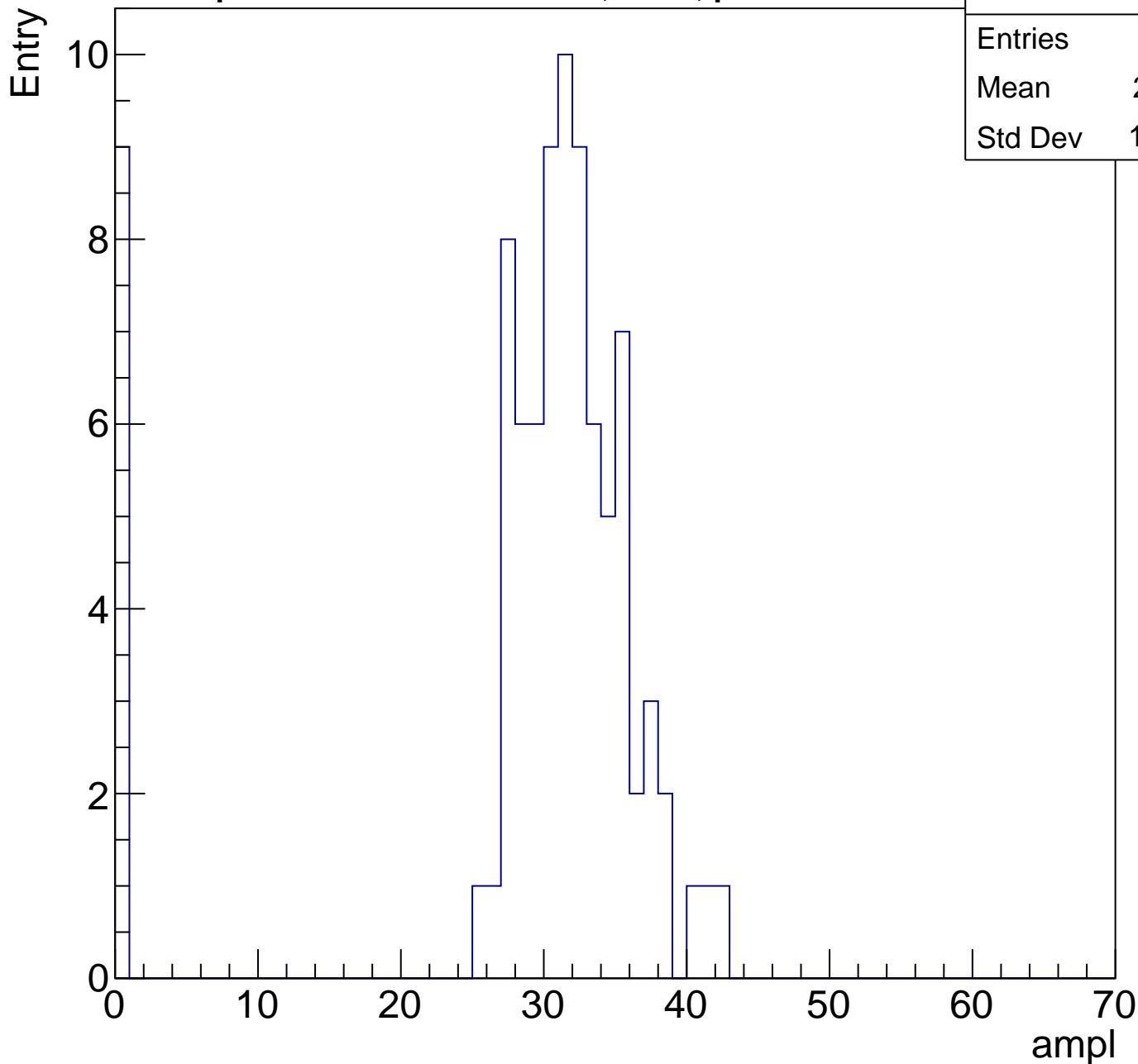
Entry



# B1L103S, U25-ch15, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	87
Mean	28.41
Std Dev	10.22



# B1L103S, U25-ch15, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	88
Mean	33.93
Std Dev	13.26

Entry

10

8

6

4

2

0

0

10

20

30

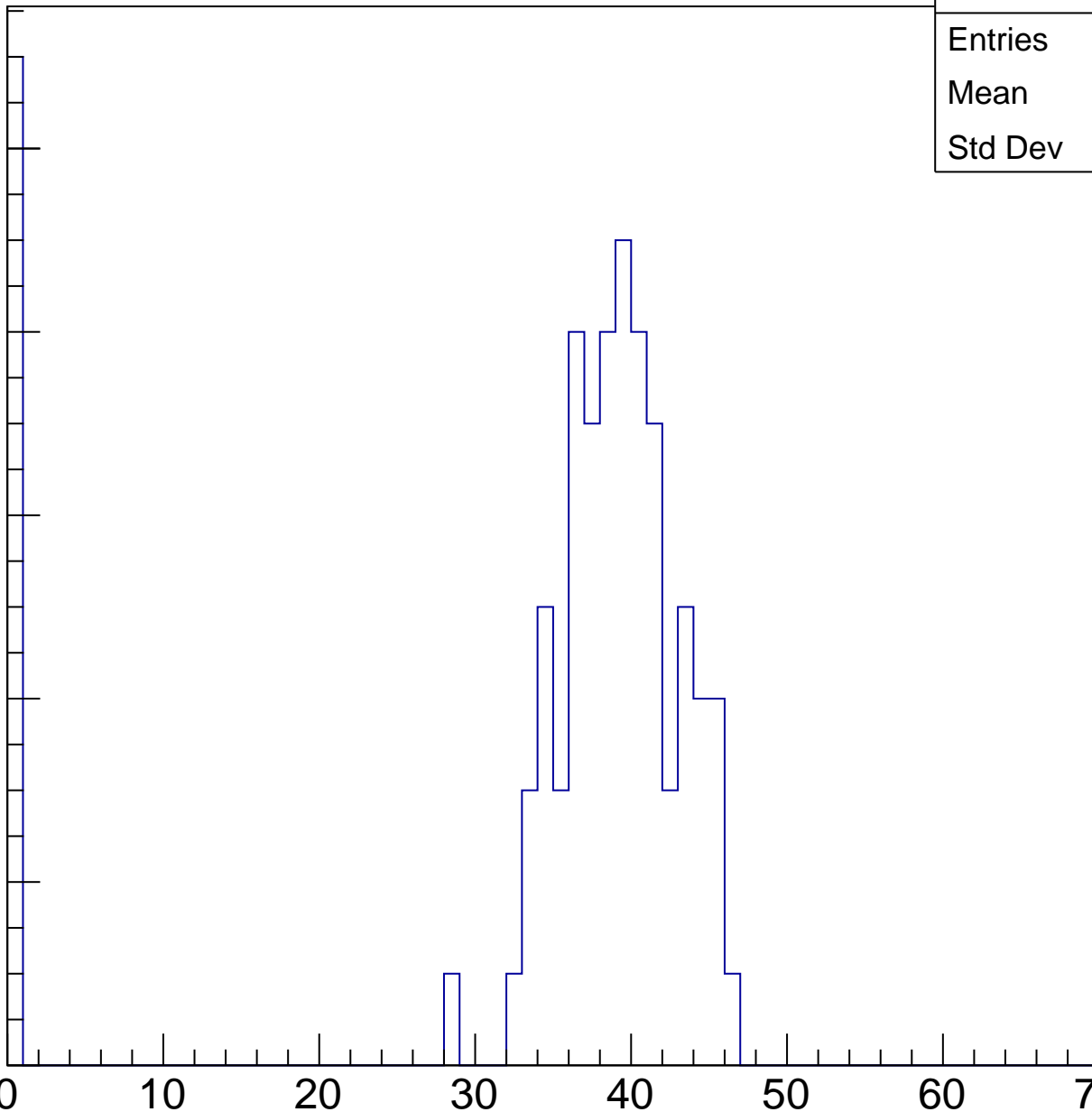
40

50

60

70

ampl

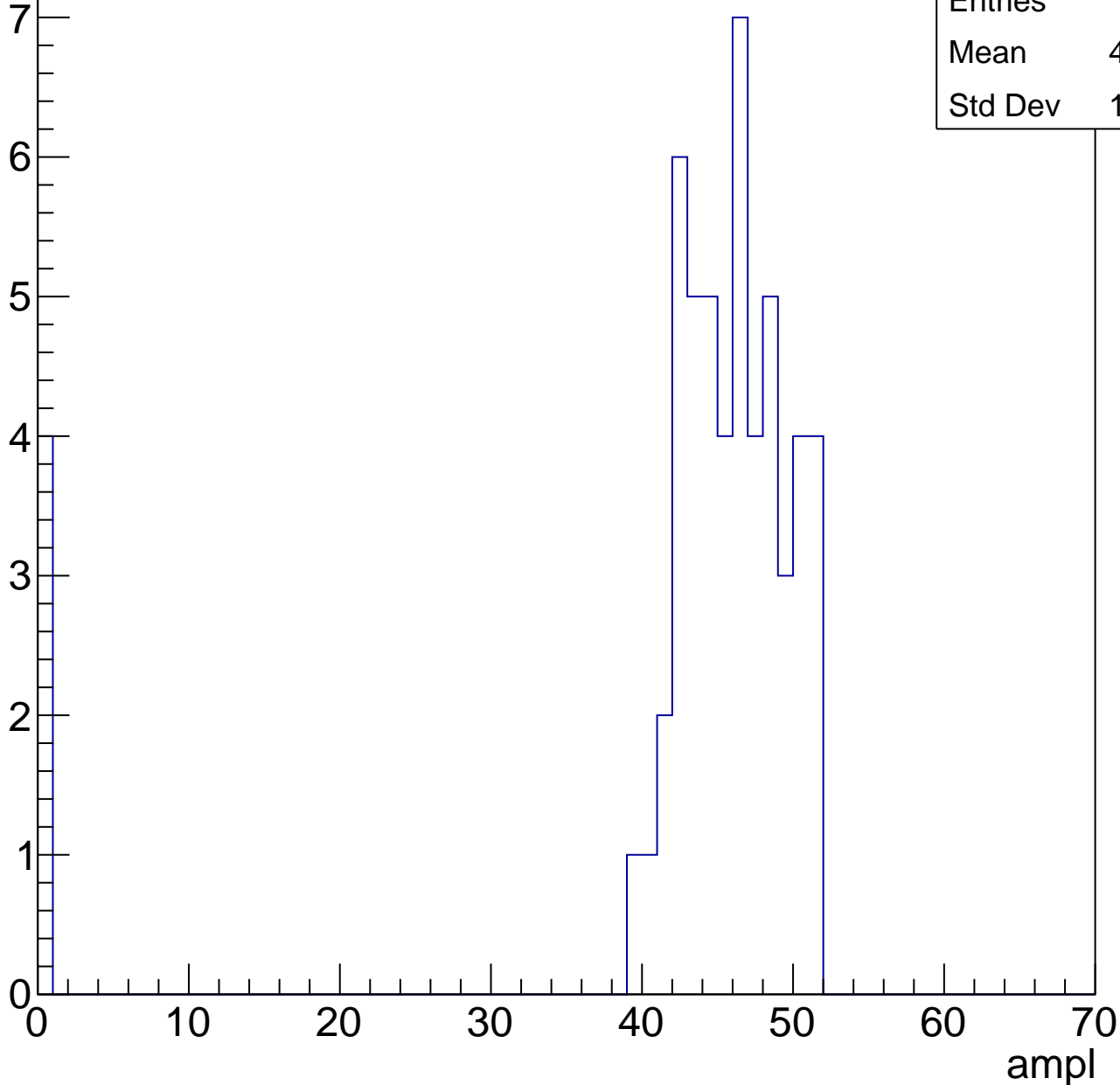


# B1L103S, U25-ch15, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	55
Mean	42.35
Std Dev	12.24

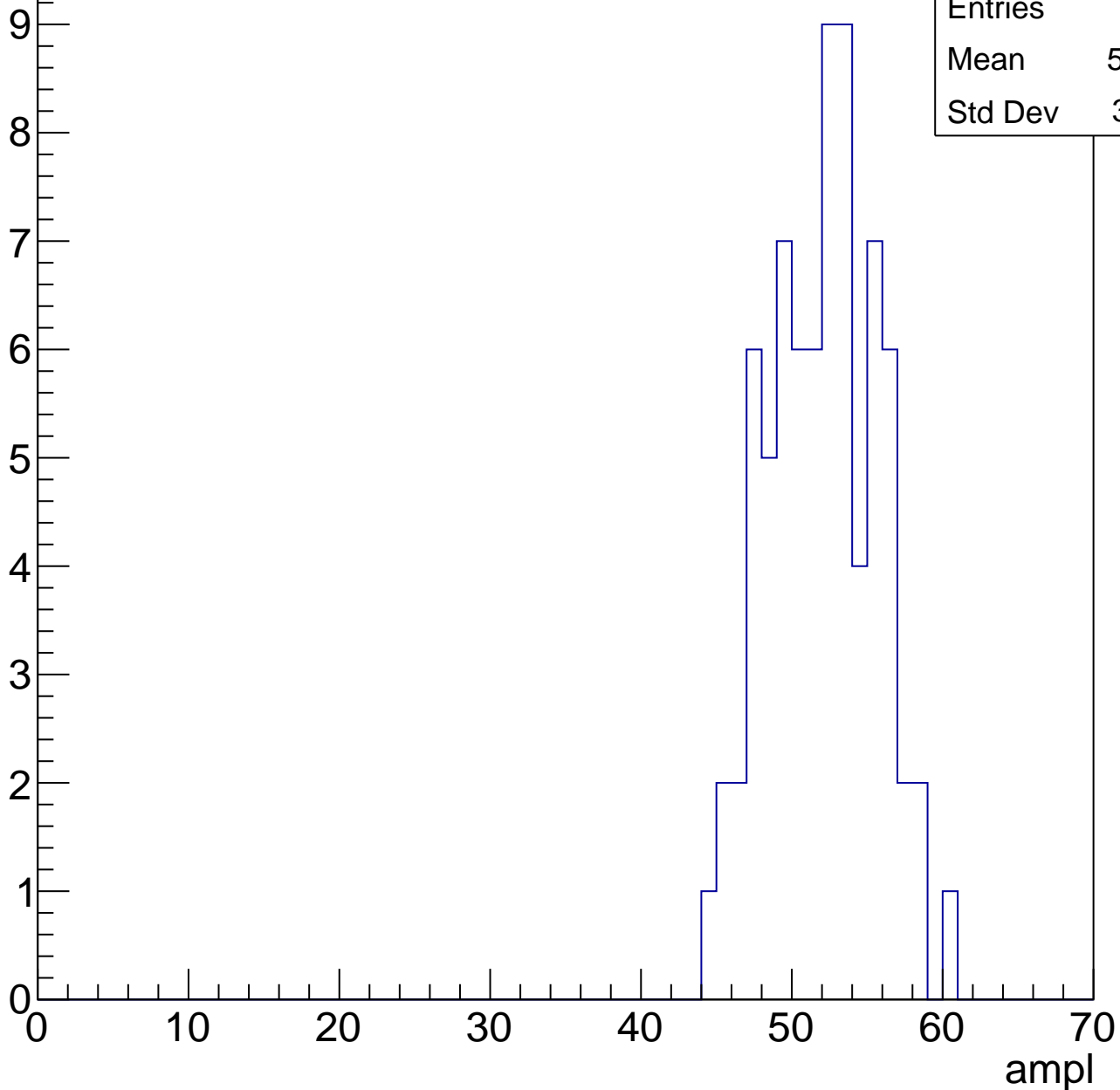


# B1L103S, U25-ch15, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

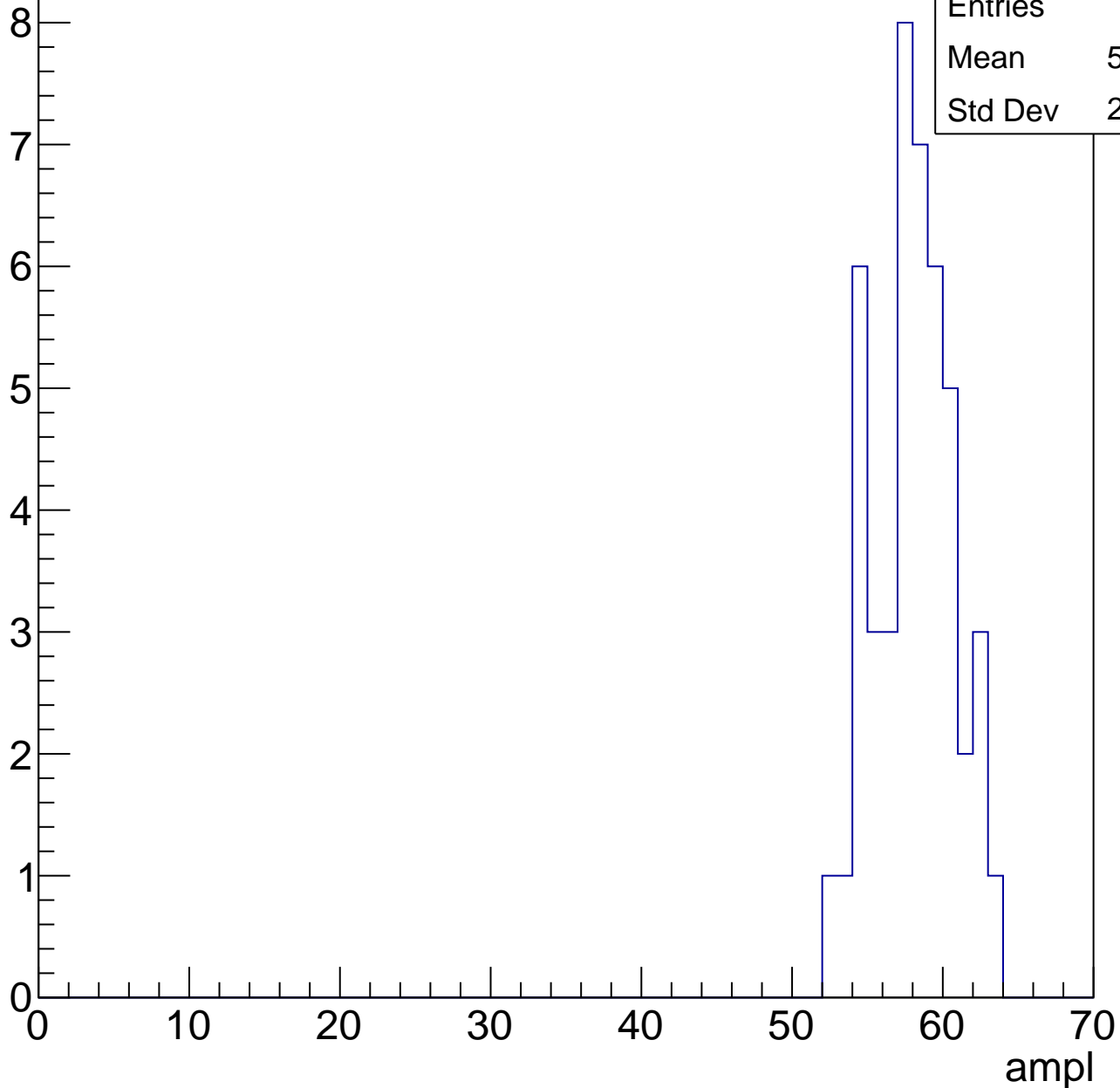
Entries	75
Mean	51.59
Std Dev	3.491



# B1L103S, U25-ch15, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



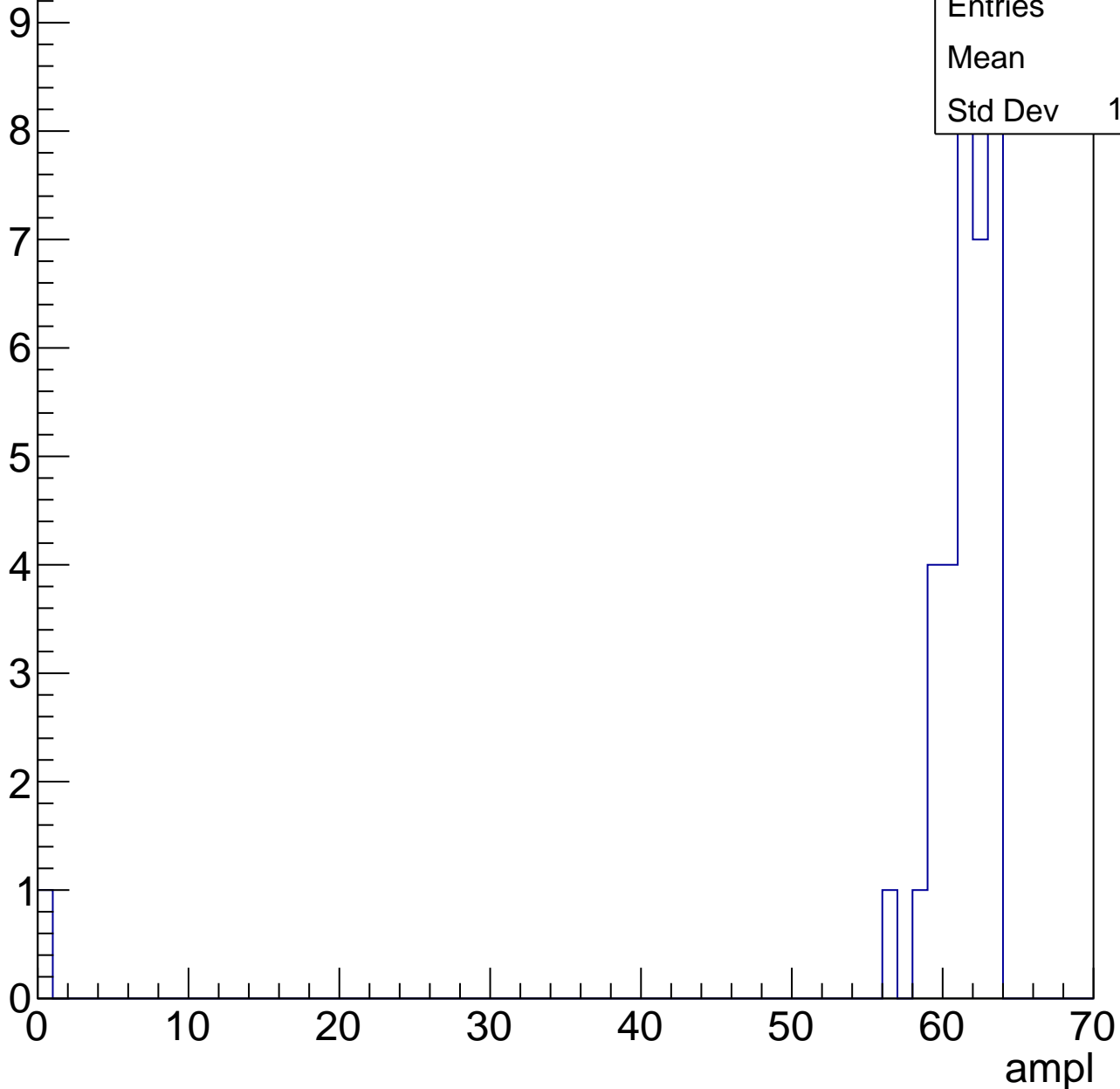
Entries	46
Mean	57.59
Std Dev	2.609

# B1L103S, U25-ch15, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	35
Mean	59.4
Std Dev	10.32



# B1L103S, U25-ch15, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L103S, U25-ch15, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

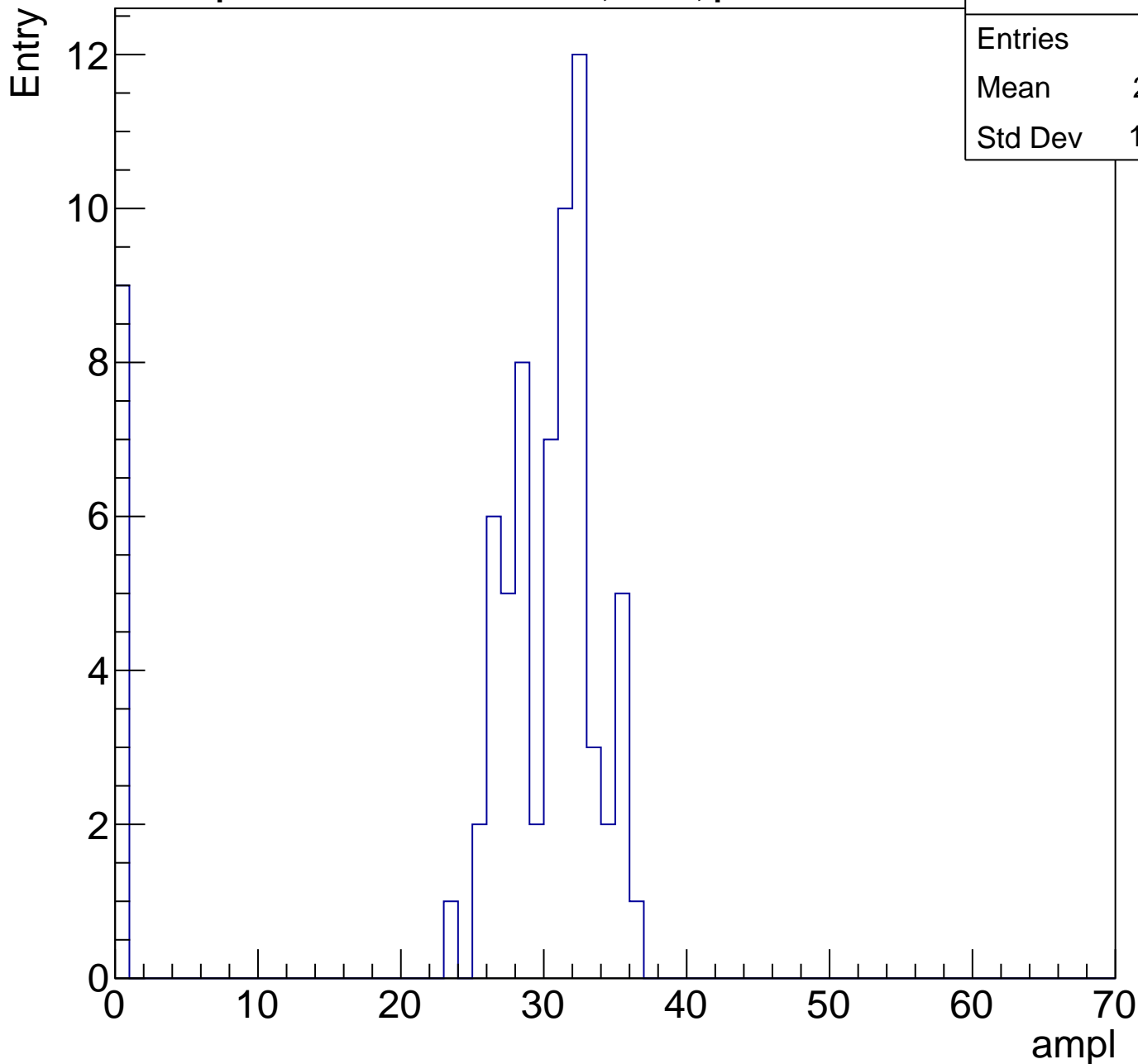
ampl

Entries	19
Mean	0
Std Dev	0

# B1L103S, U25-ch16, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	73
Mean	26.41
Std Dev	10.28



# B1L103S, U25-ch16, adc1

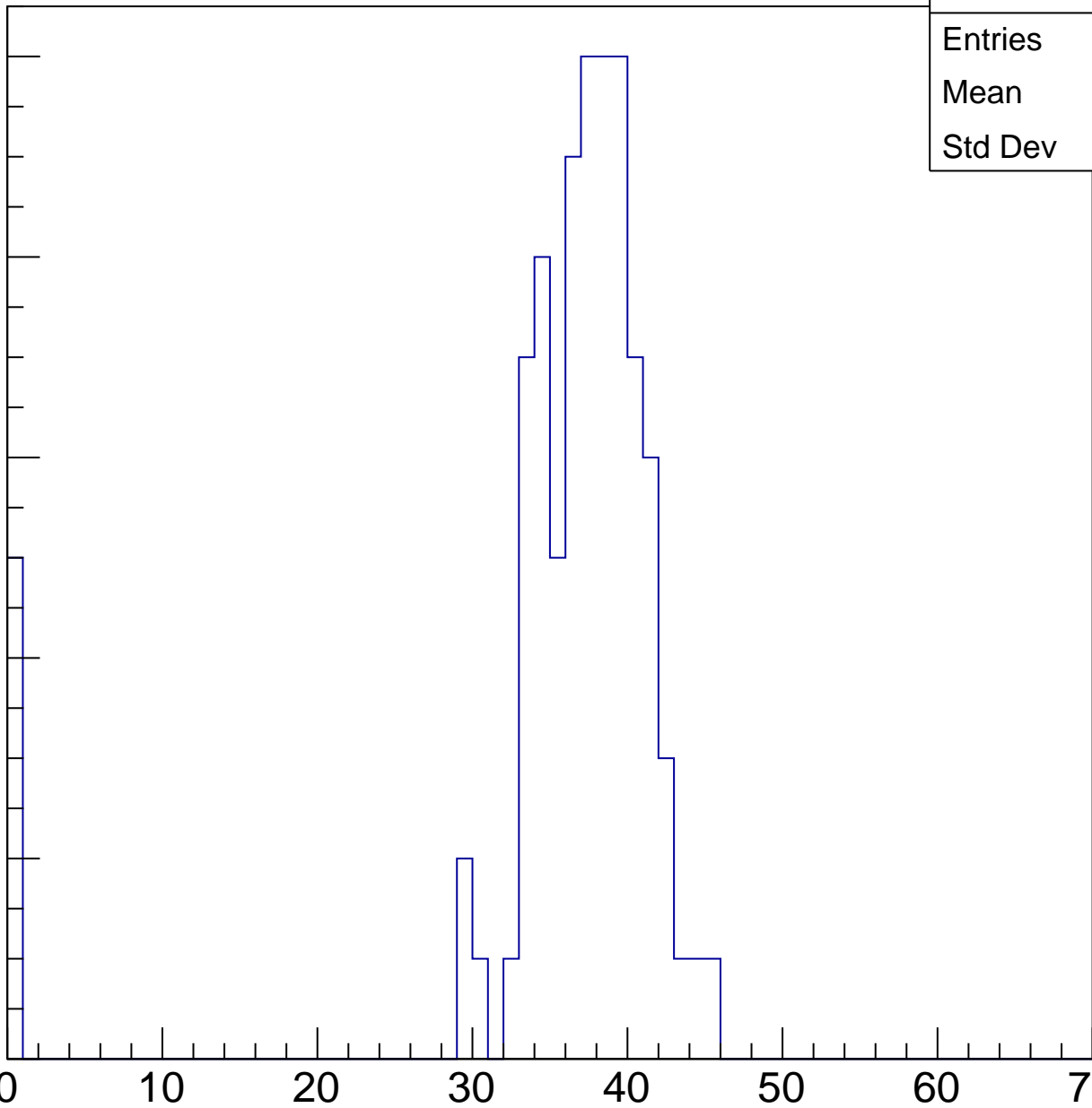
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	87
Mean	35.01
Std Dev	9.191

Entry

10  
8  
6  
4  
2  
0

ampl

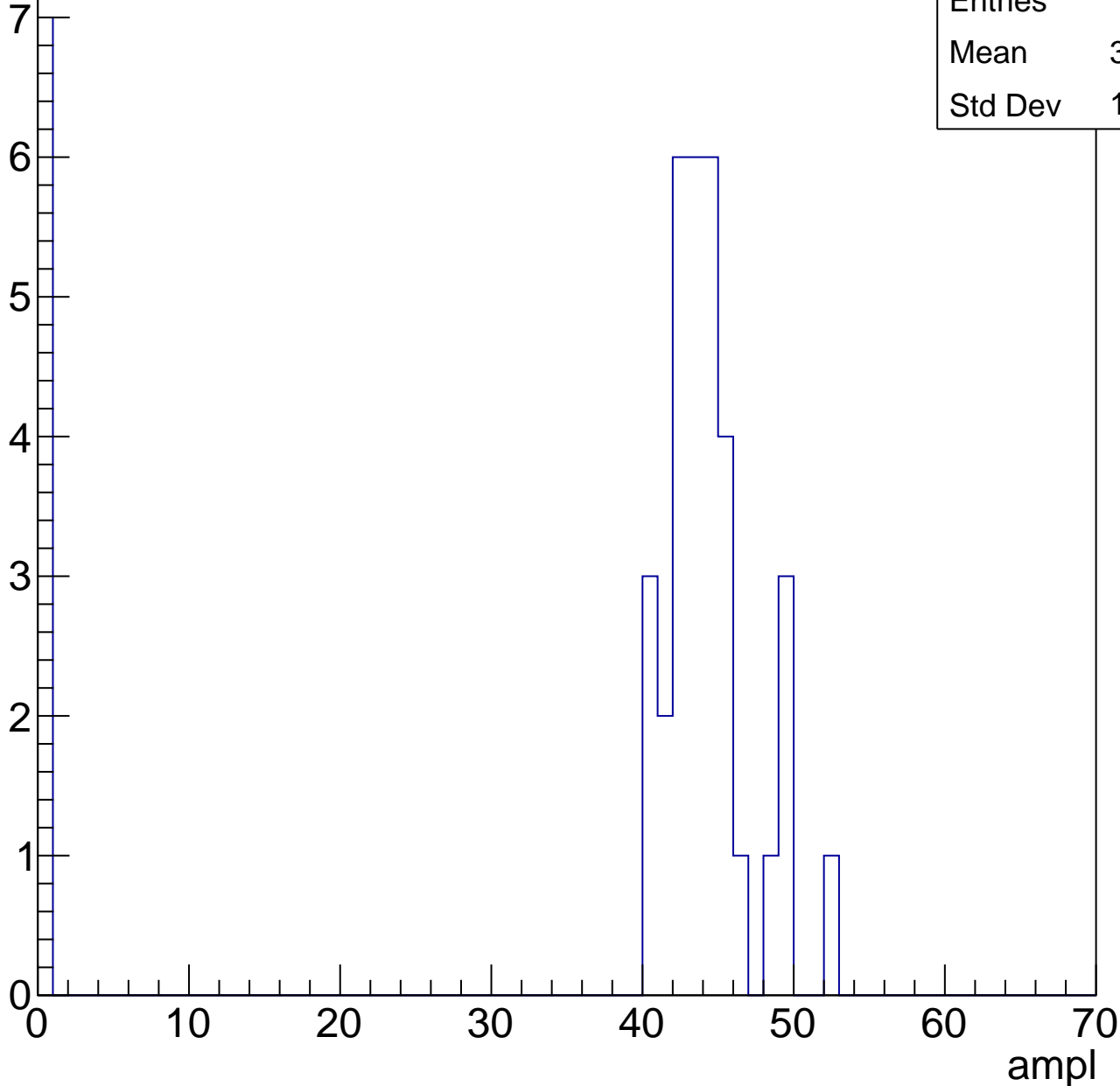


# B1L103S, U25-ch16, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	40
Mean	36.23
Std Dev	16.88



# B1L103S, U25-ch16, adc3

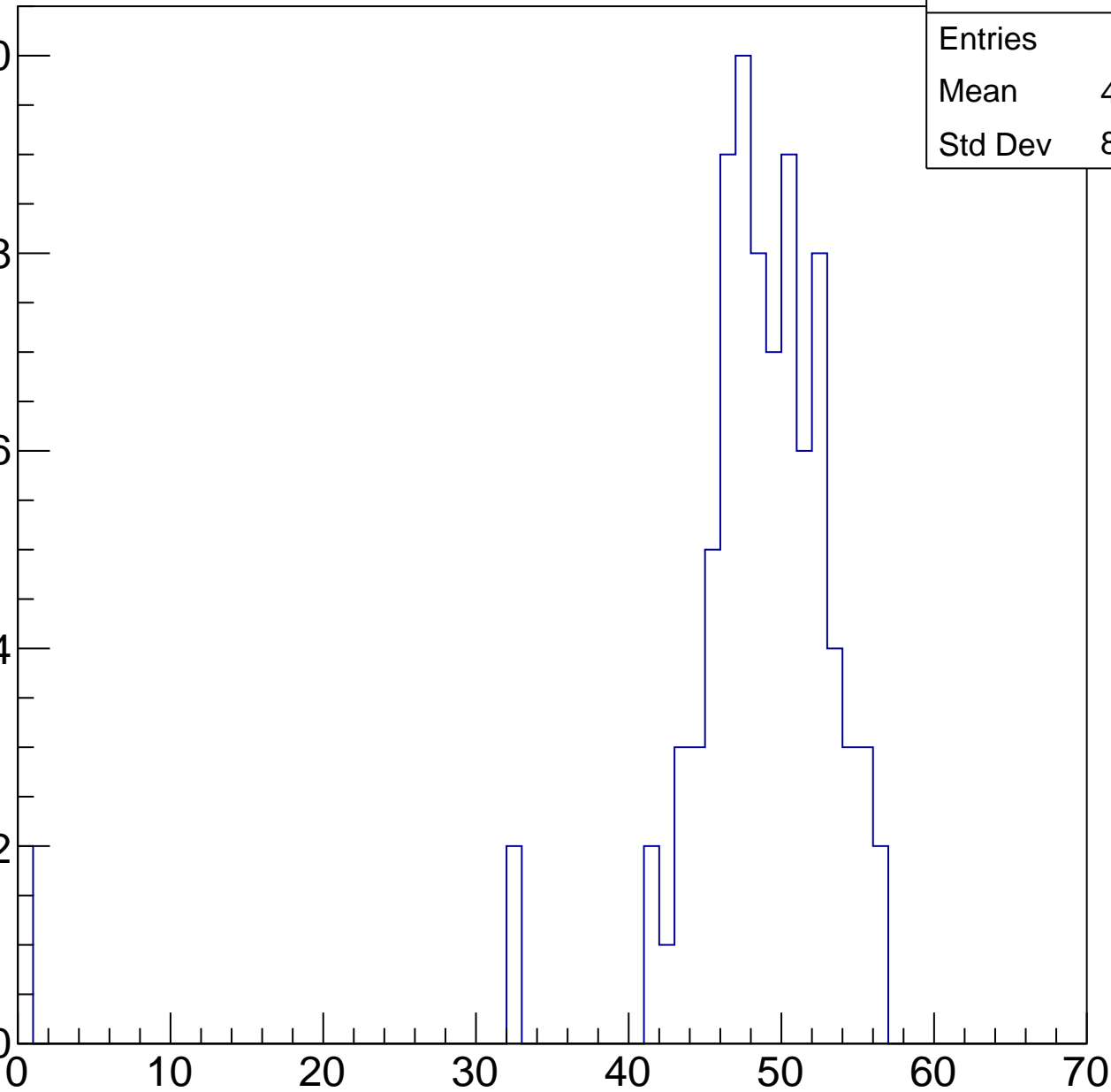
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	87
Mean	47.22
Std Dev	8.389

Entry

10  
8  
6  
4  
2  
0

ampl

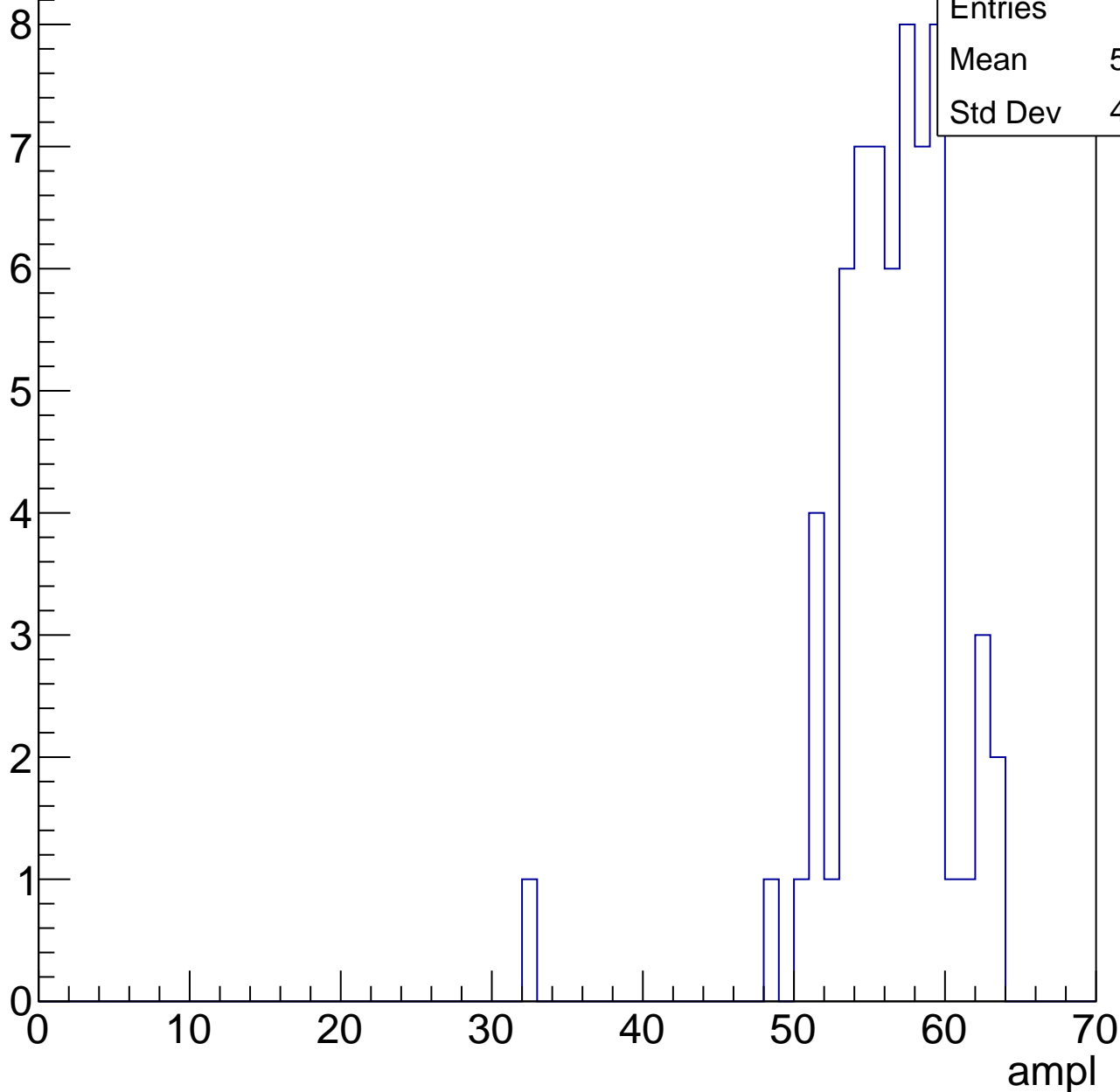


# B1L103S, U25-ch16, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	64
Mean	55.78
Std Dev	4.389



# B1L103S, U25-ch16, adc5

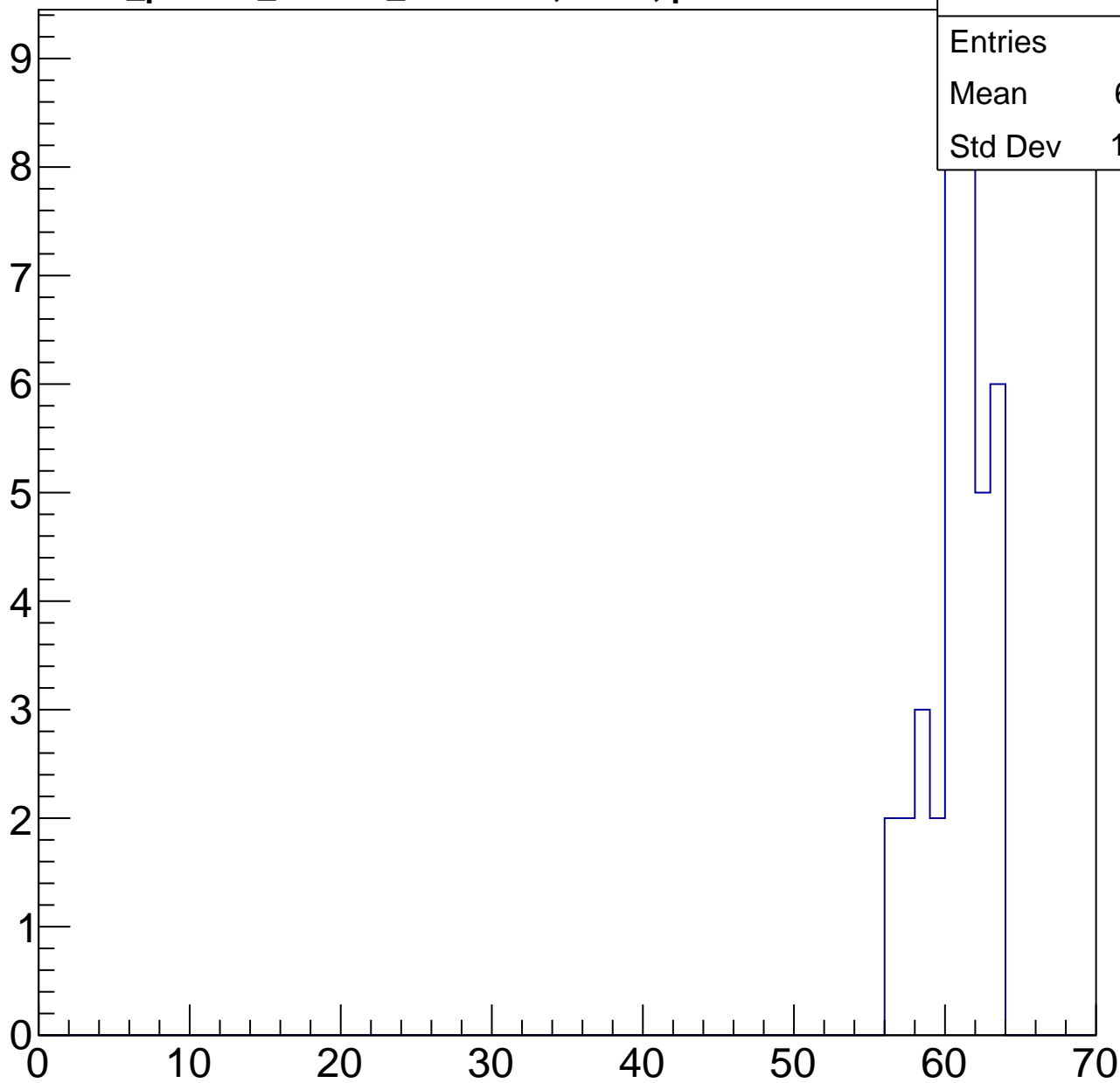
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	37
Mean	60.41
Std Dev	1.952

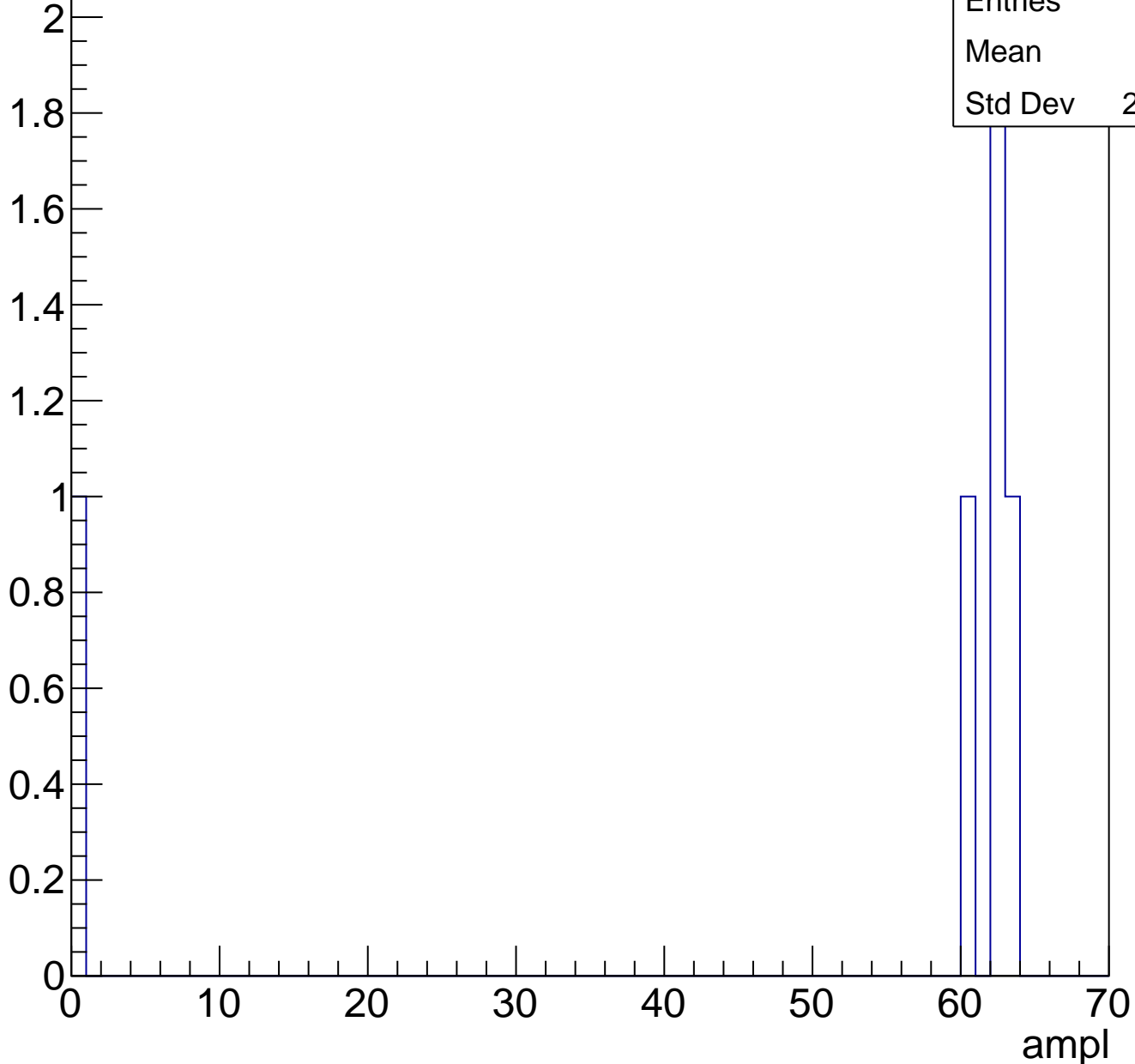
ampl



# B1L103S, U25-ch16, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U25-ch16, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	19
Mean	3.316
Std Dev	14.07

Entry



# B1L103S, U25-ch17, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

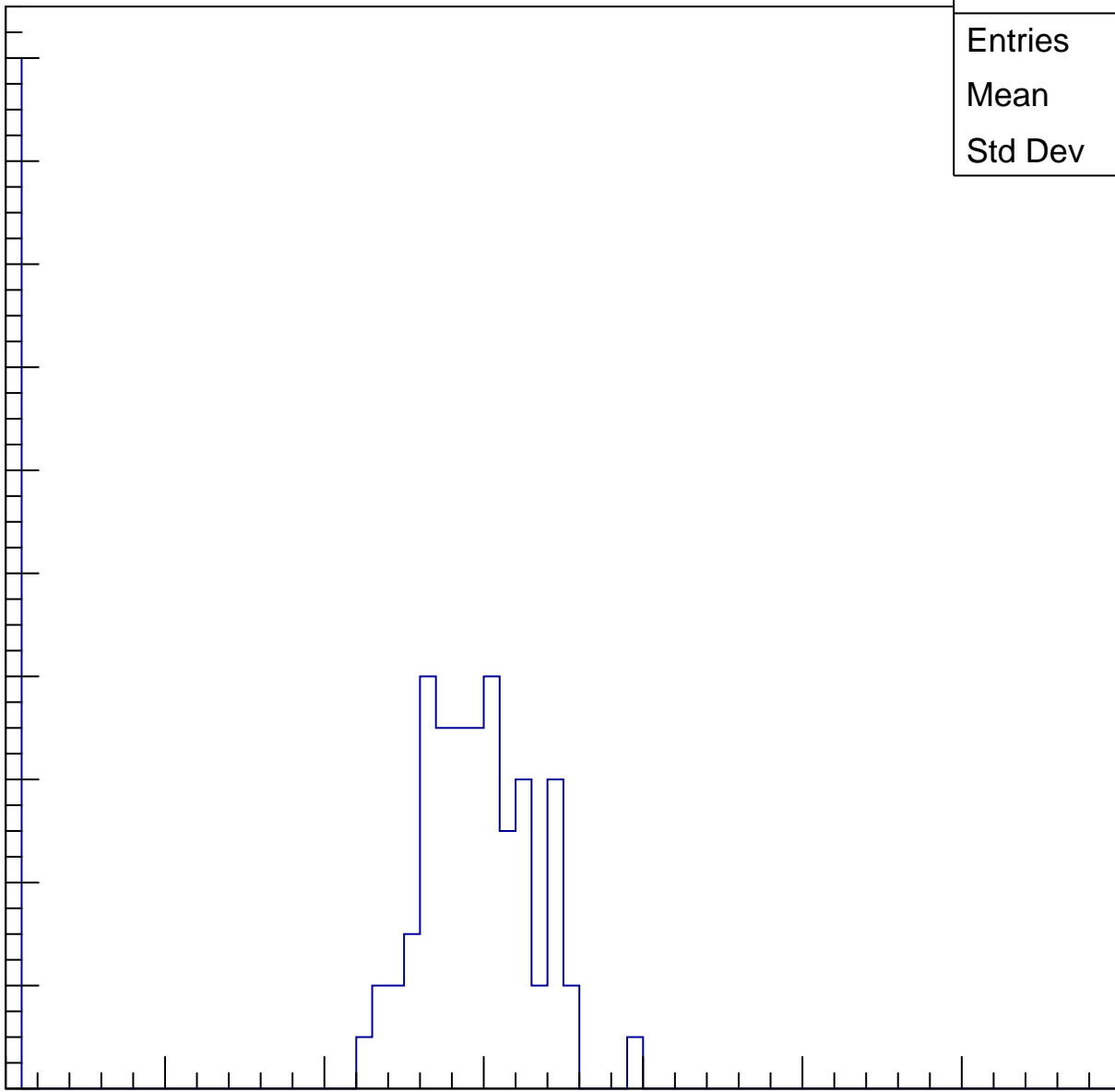
Entries	87
Mean	22.45
Std Dev	12.62

Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

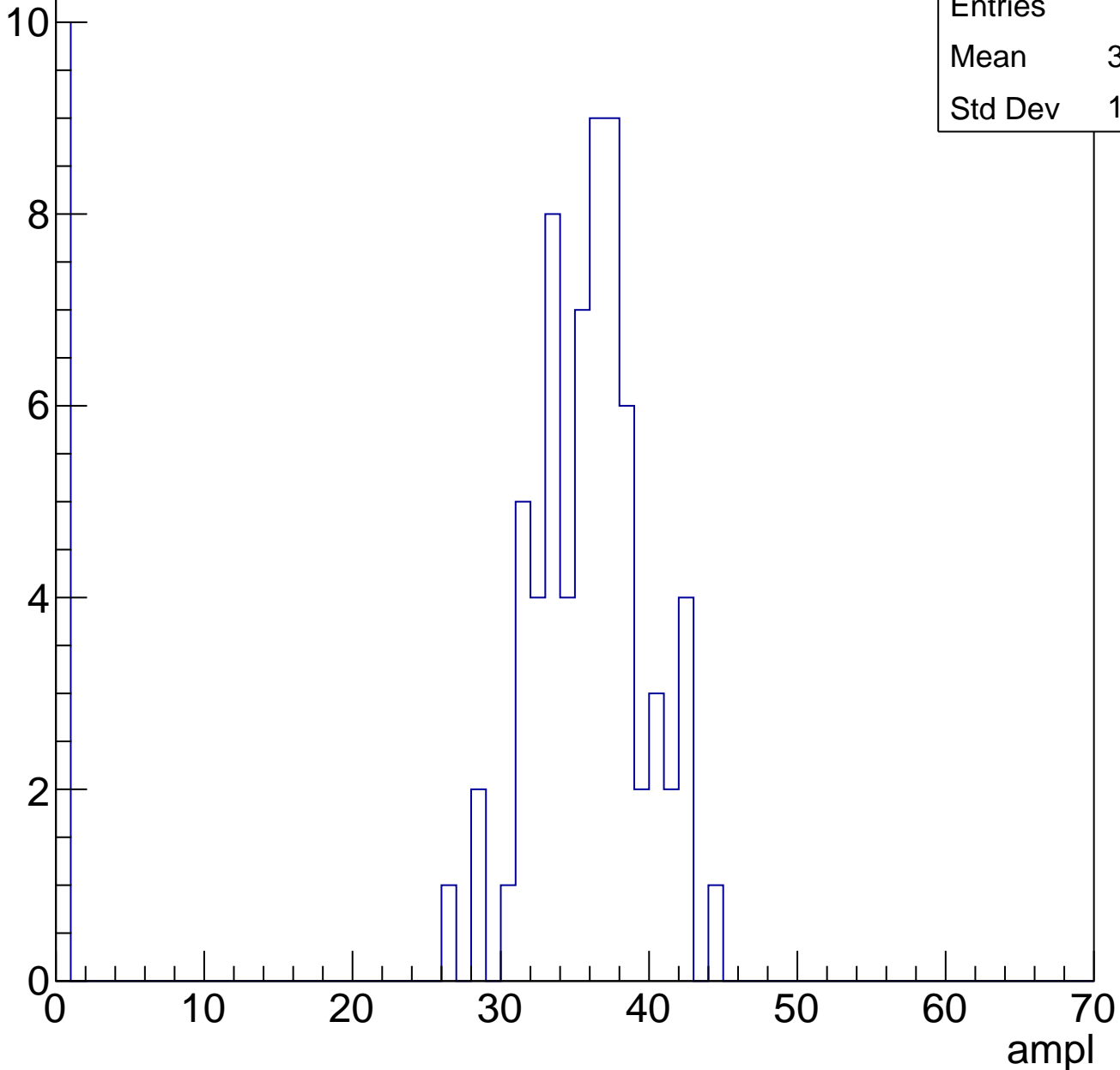


# B1L103S, U25-ch17, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	78
Mean	30.99
Std Dev	12.35

Entry

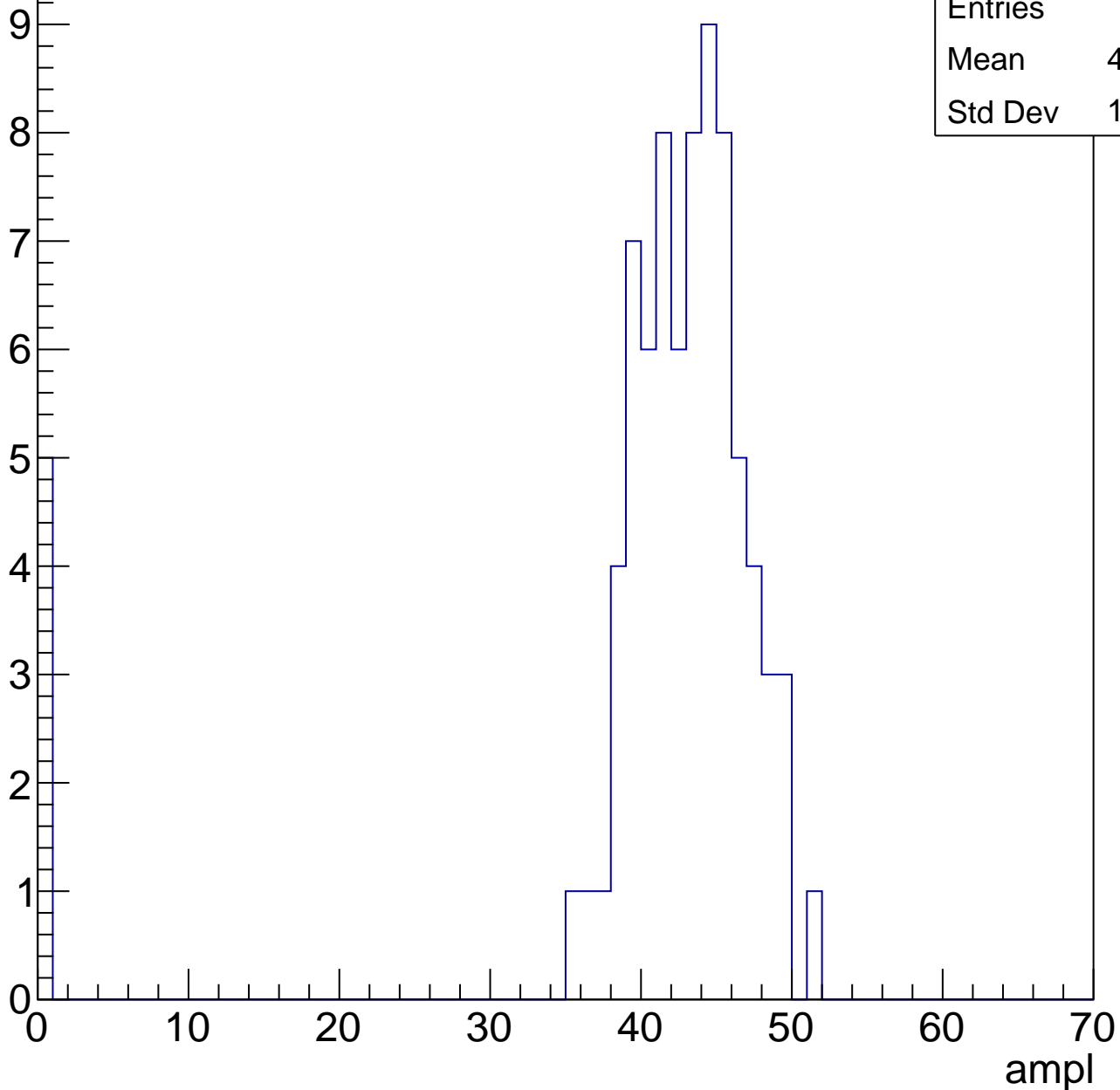


# B1L103S, U25-ch17, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	80
Mean	40.16
Std Dev	10.87

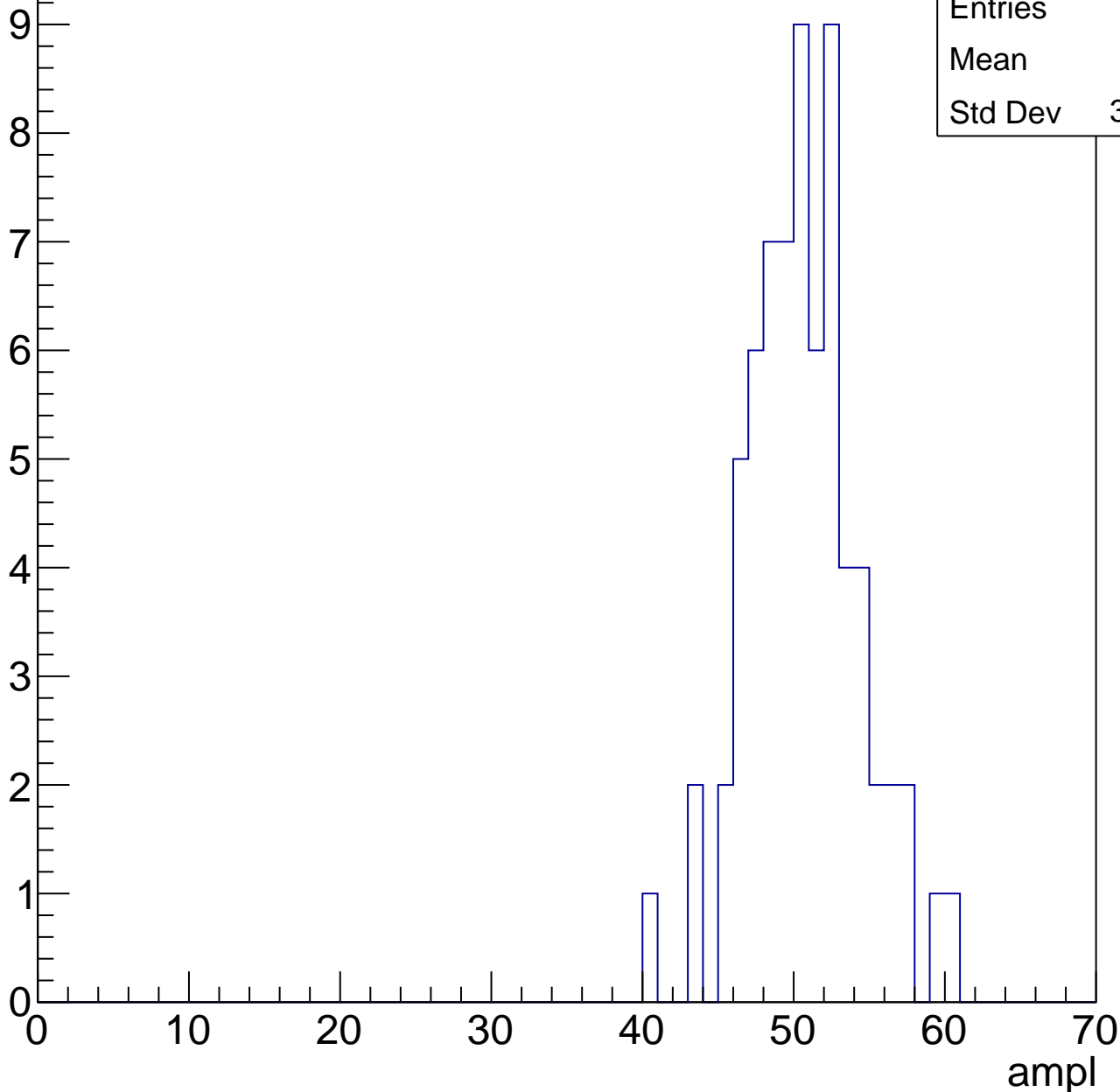


# B1L103S, U25-ch17, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	70
Mean	50.2
Std Dev	3.698

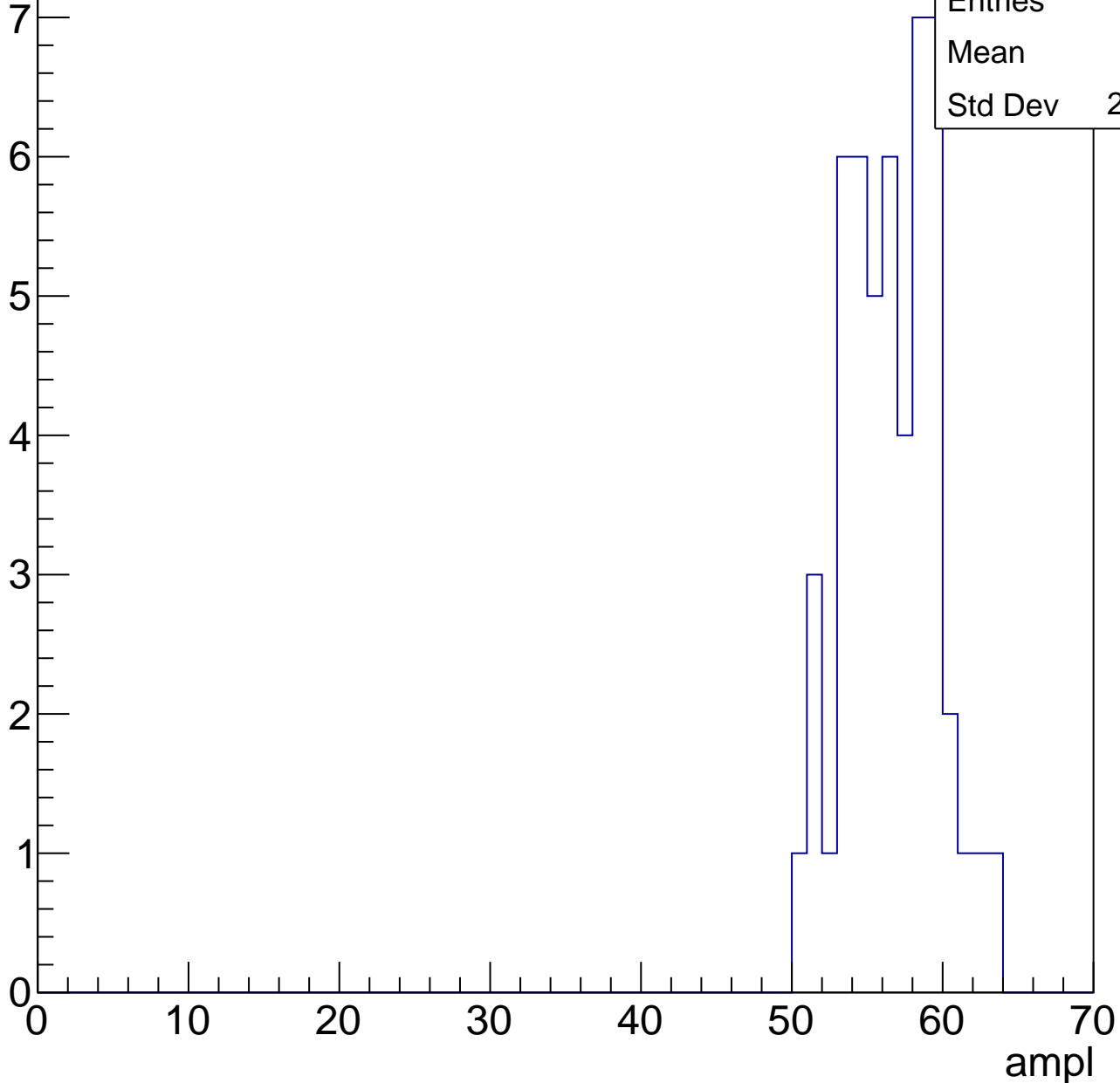


# B1L103S, U25-ch17, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	51
Mean	56.1
Std Dev	2.959

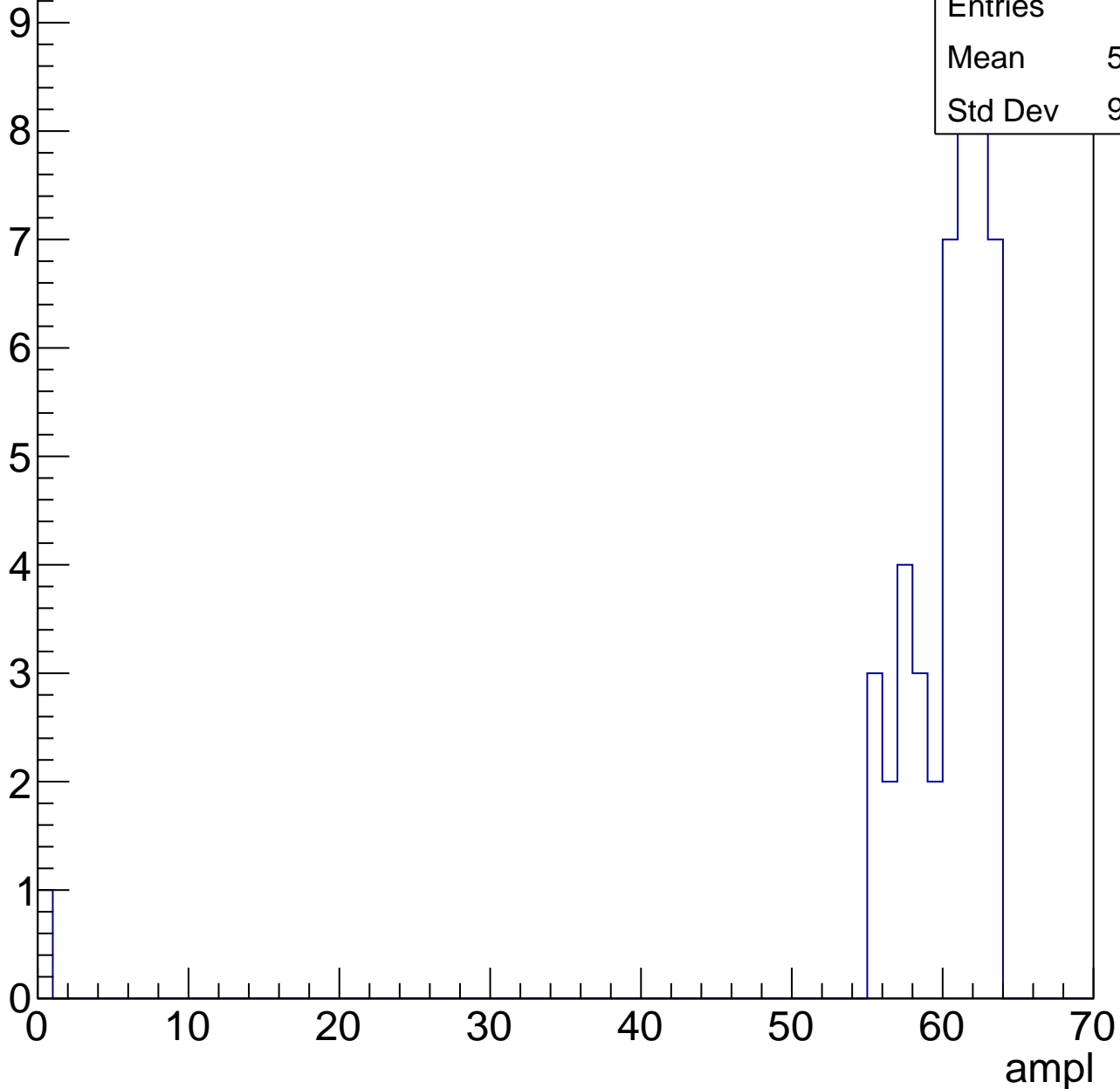


# B1L103S, U25-ch17, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	46
Mean	58.78
Std Dev	9.084



# B1L103S, U25-ch17, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	3
Mean	62.33
Std Dev	0.9428



# B1L103S, U25-ch17, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

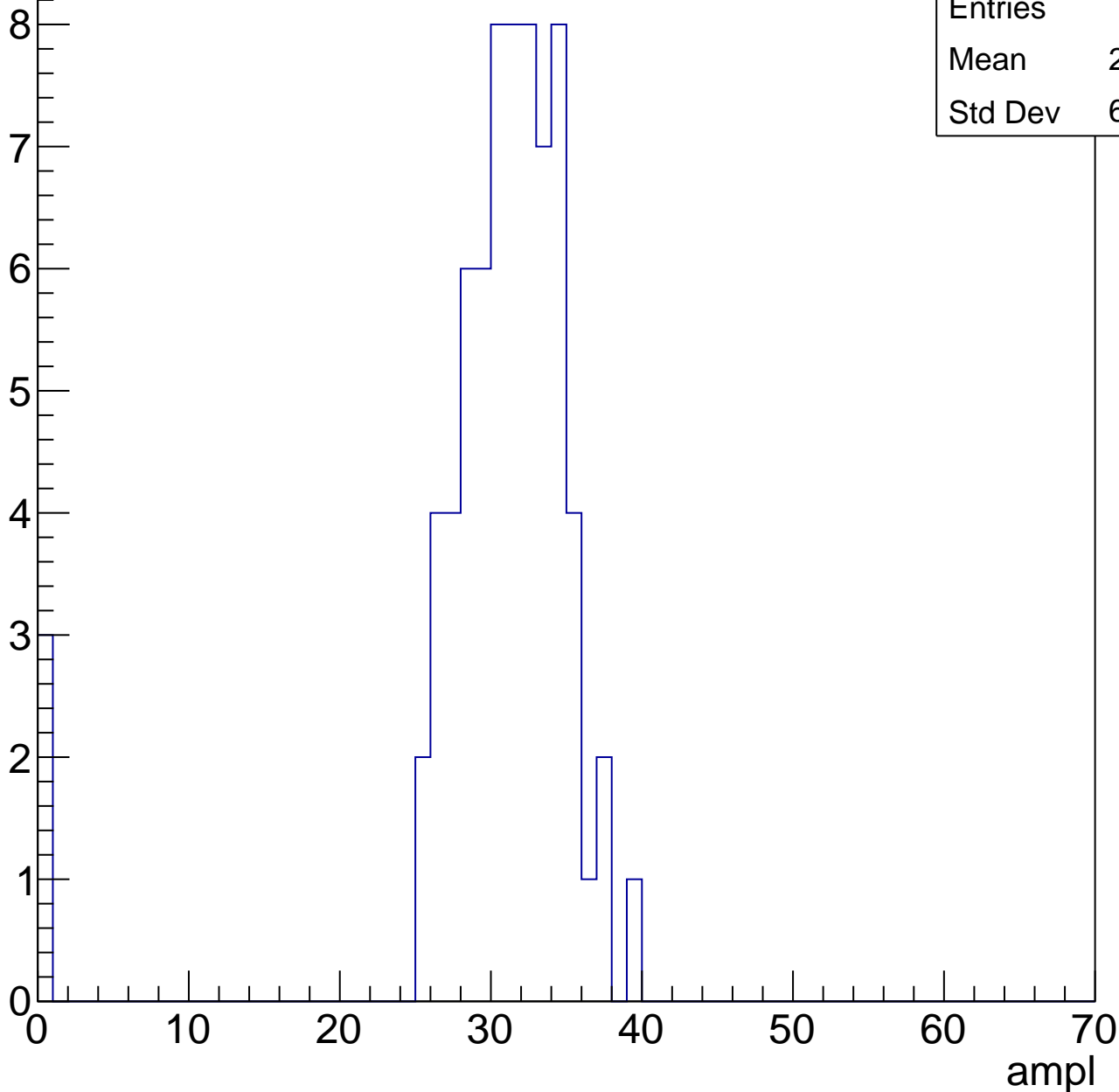


# B1L103S, U25-ch18, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	72
Mean	29.72
Std Dev	6.892

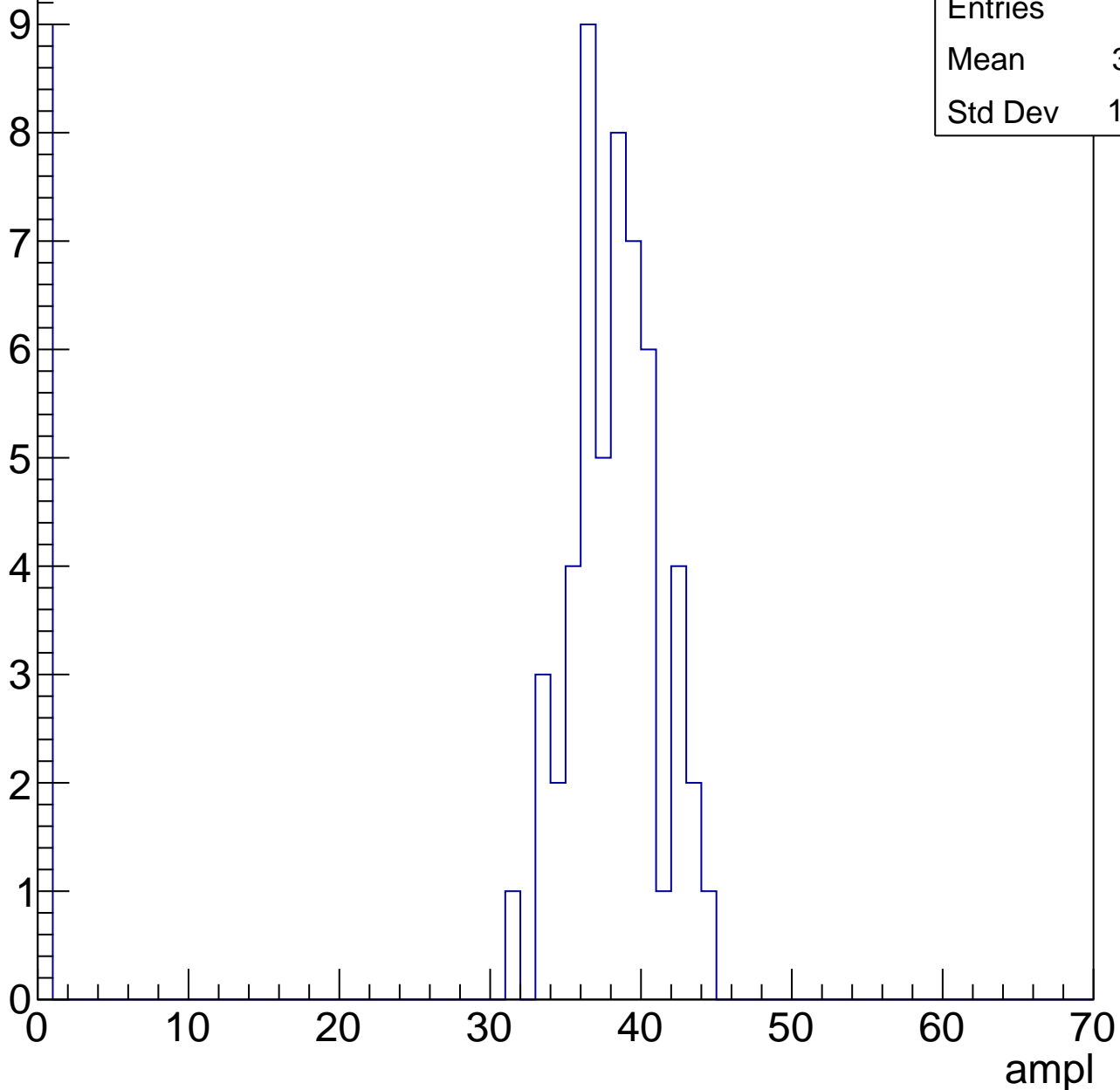


# B1L103S, U25-ch18, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	62
Mean	32.31
Std Dev	13.57

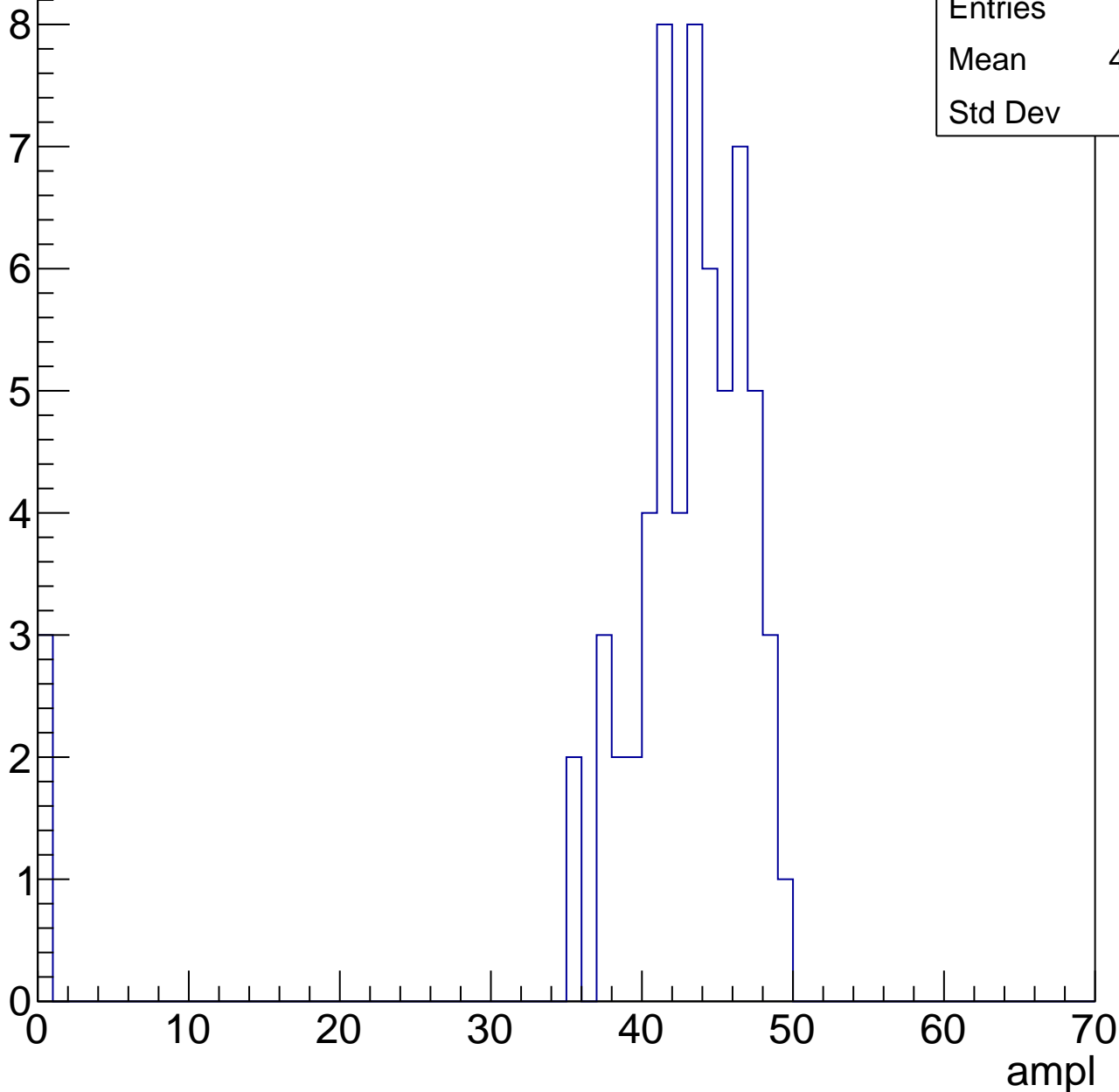


# B1L103S, U25-ch18, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	63
Mean	40.86
Std Dev	9.7

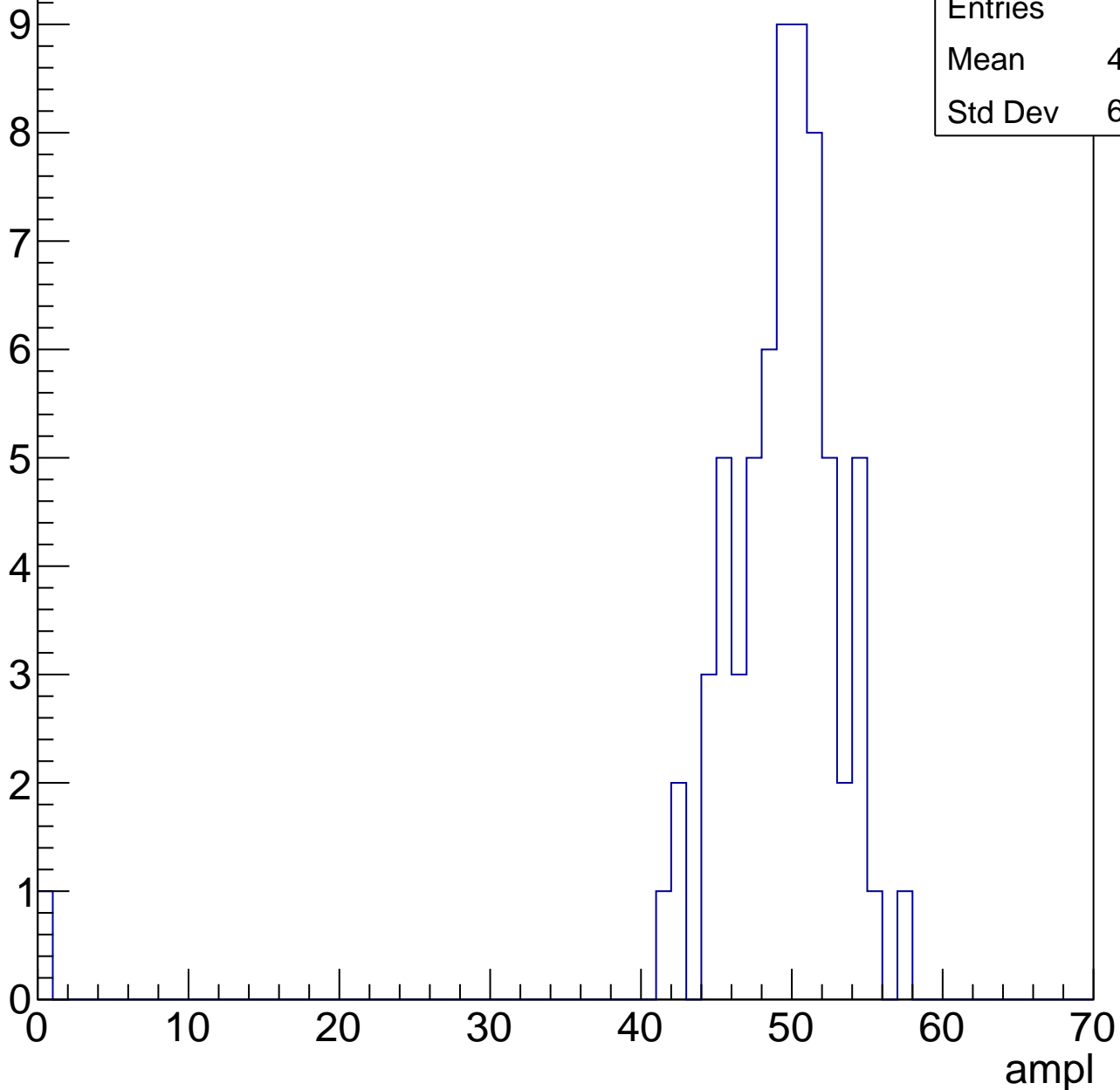


# B1L103S, U25-ch18, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

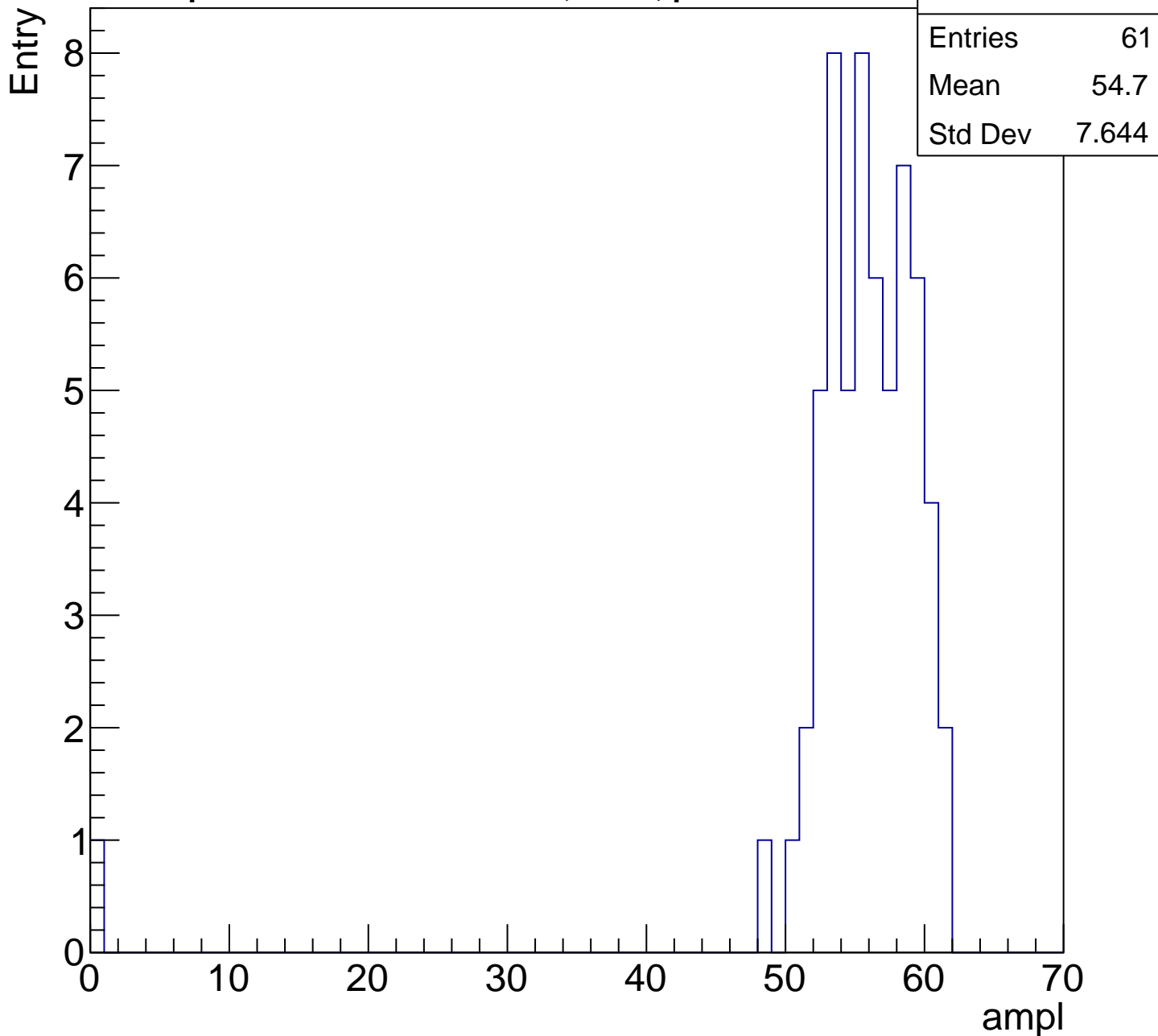
Entry

Entries	66
Mean	48.33
Std Dev	6.836



# B1L103S, U25-ch18, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

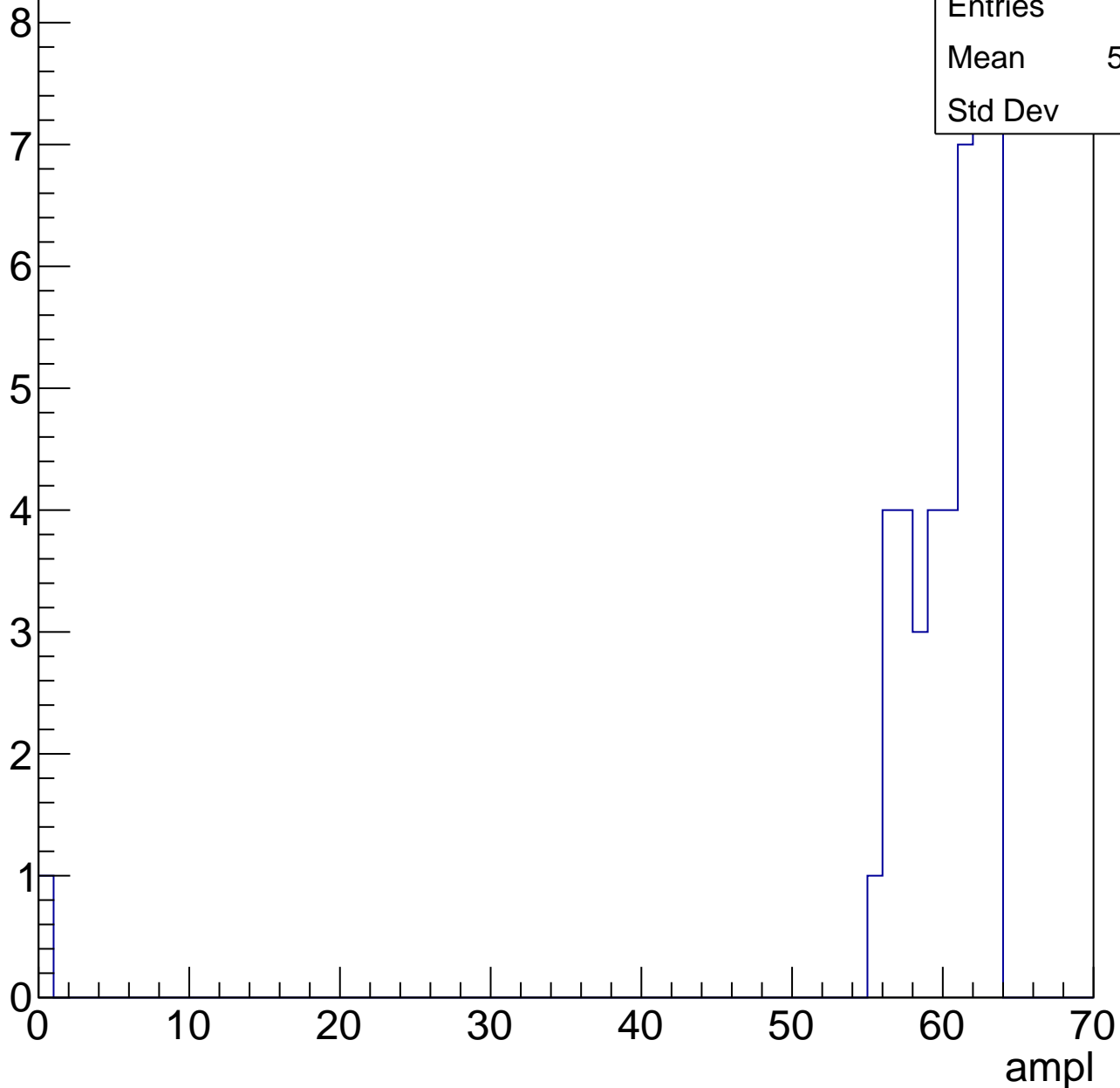


# B1L103S, U25-ch18, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	44
Mean	58.73
Std Dev	9.27



# B1L103S, U25-ch18, adc6

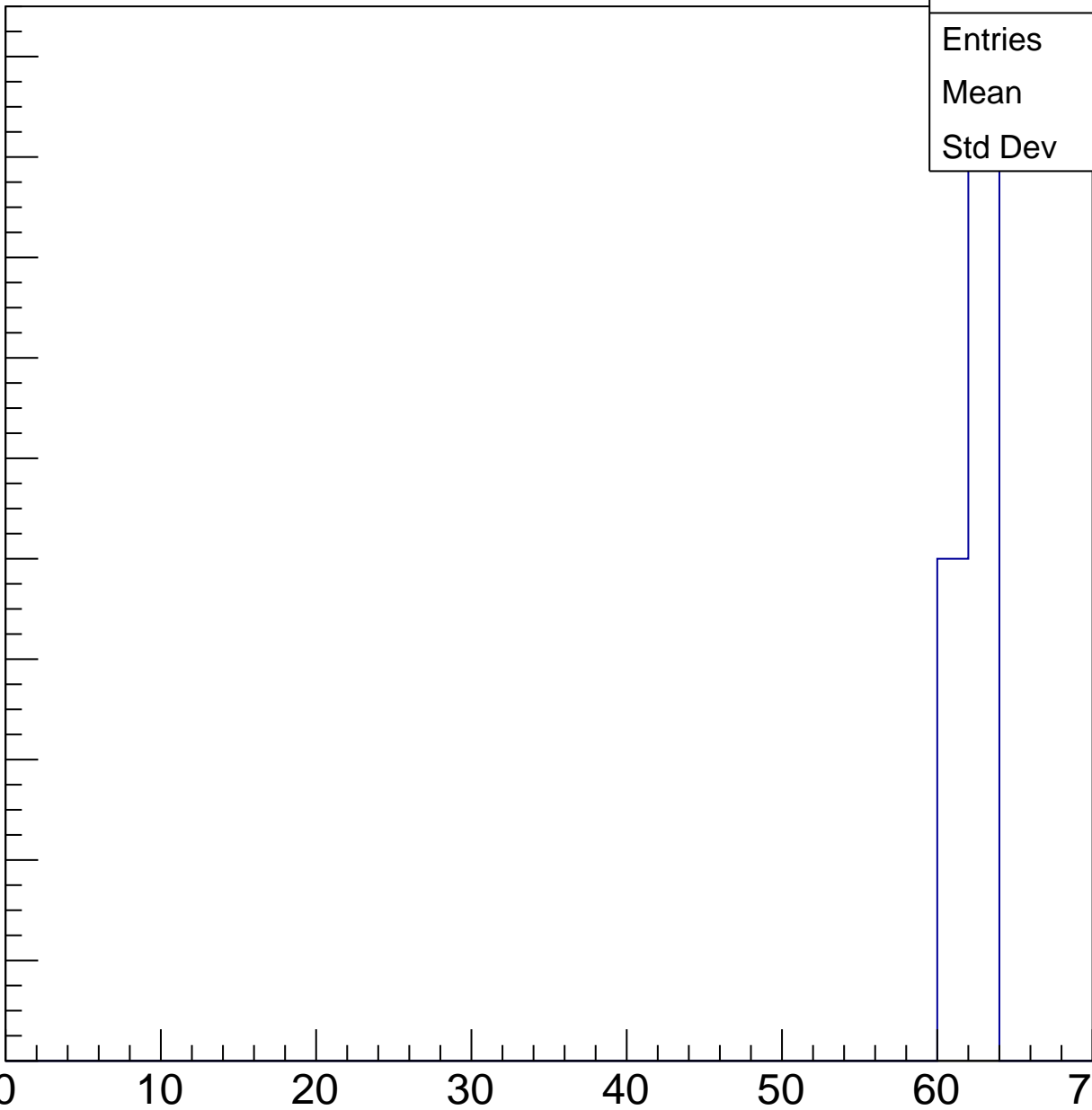
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	61.83
Std Dev	1.067

ampl

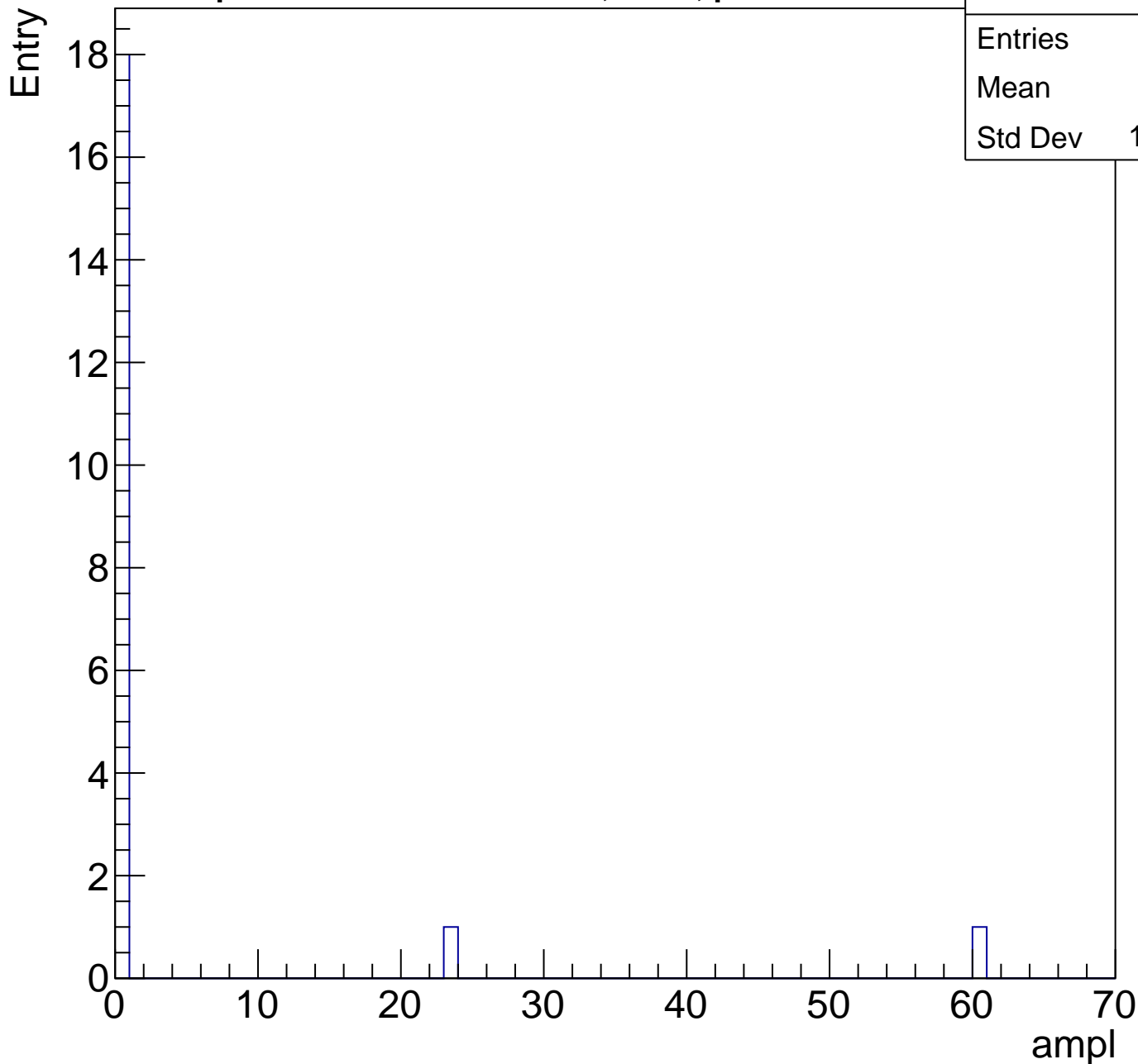




# B1L103S, U25-ch18, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	20
Mean	4.15
Std Dev	13.76



# B1L103S, U25-ch19, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	82
Mean	25.16
Std Dev	11.27

Entry

12

10

8

6

4

2

0

0

10

20

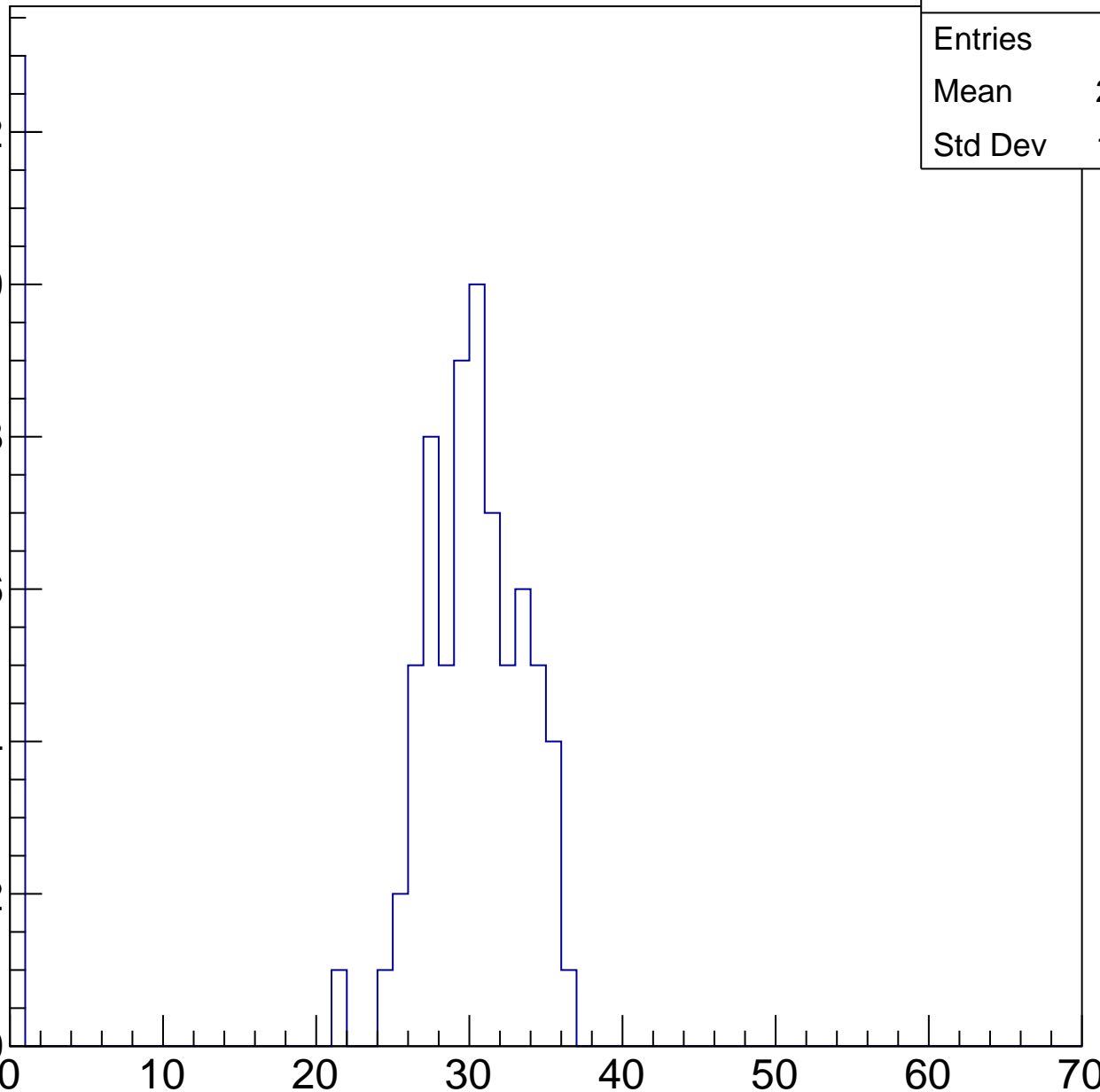
30

40

50

60

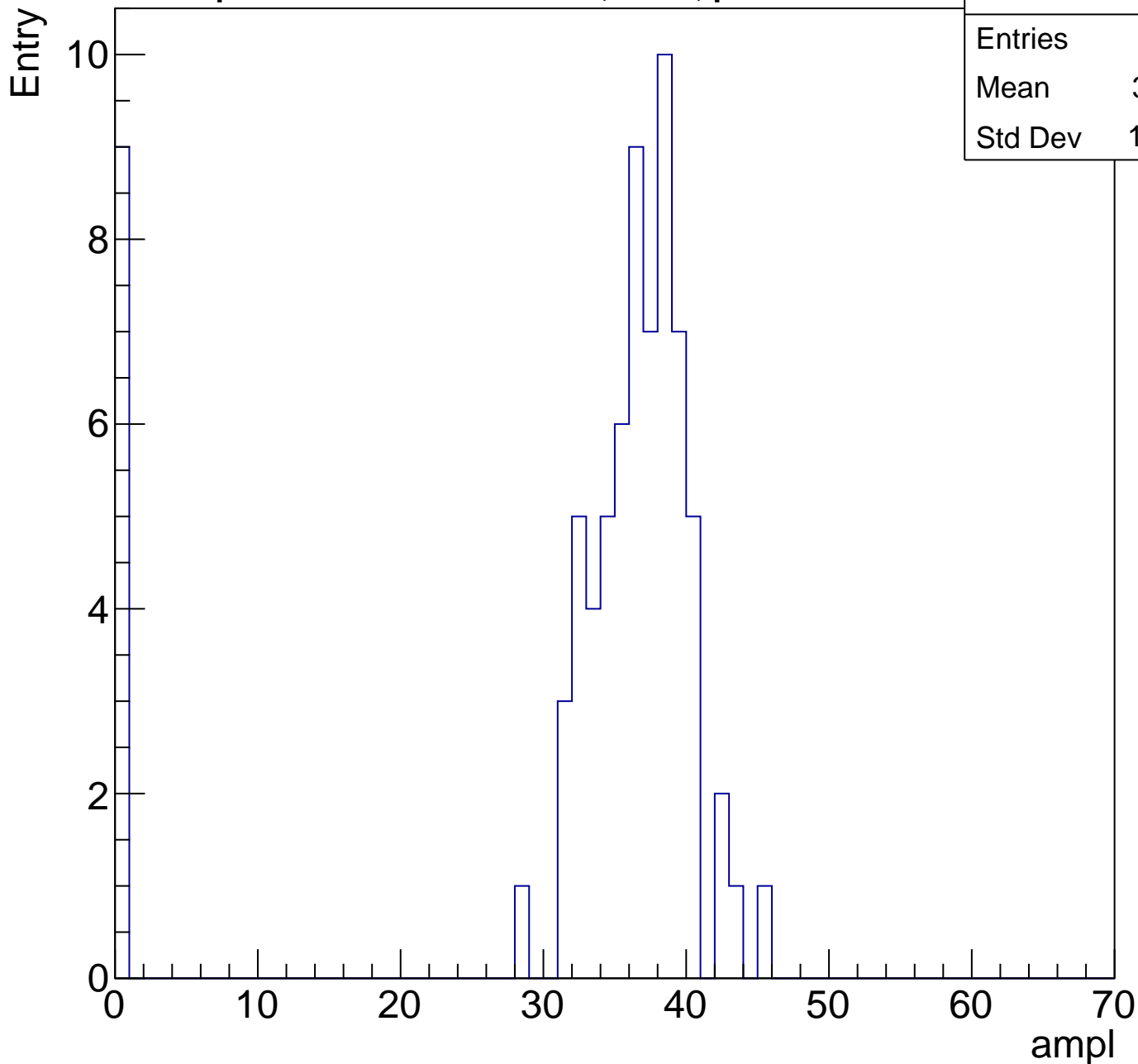
ampl



# B1L103S, U25-ch19, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	75
Mean	32.01
Std Dev	12.19



# B1L103S, U25-ch19, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	64
Mean	42.47
Std Dev	6.174

Entry

10

8

6

4

2

0

0

10

20

30

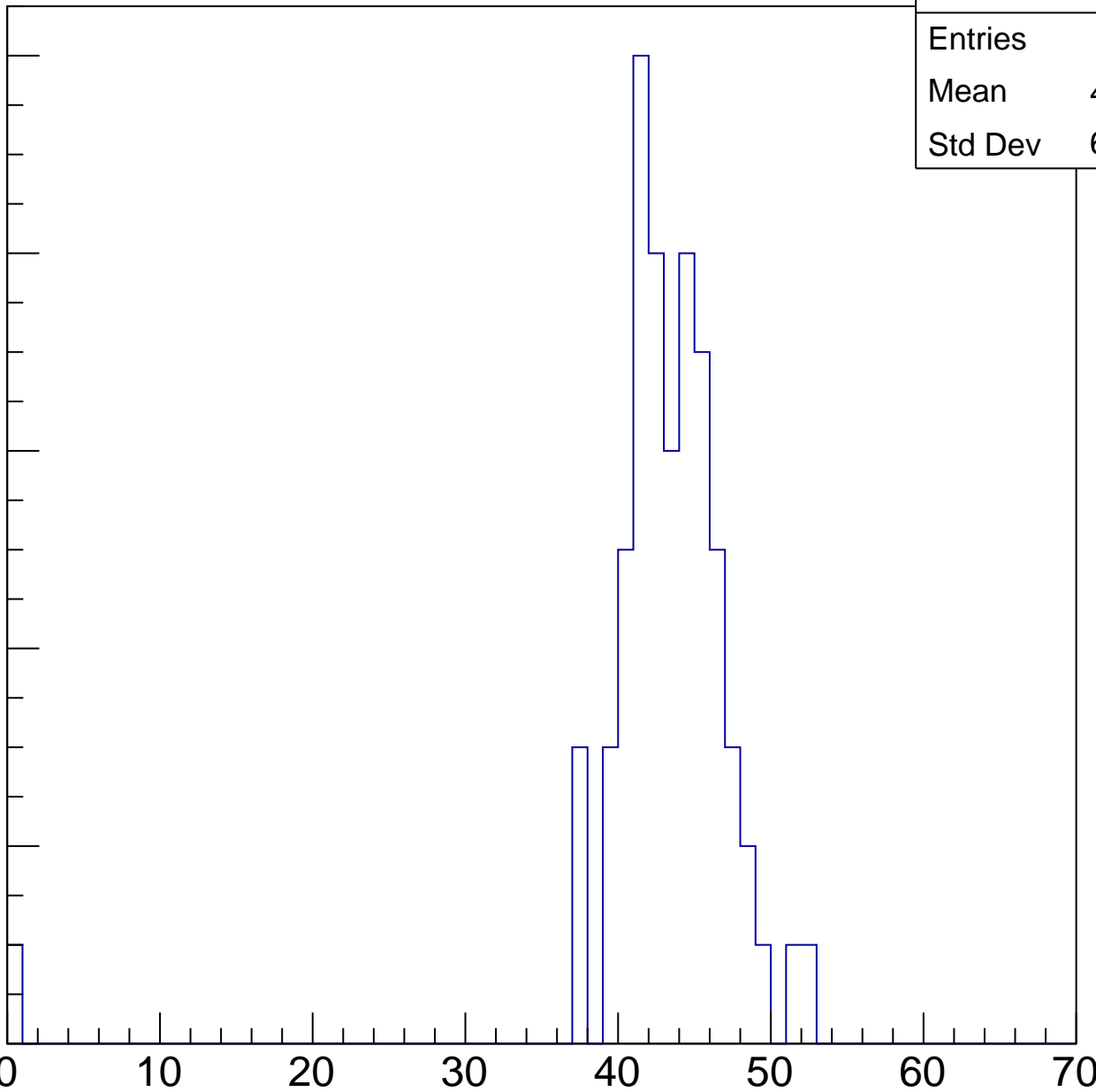
40

50

60

70

ampl

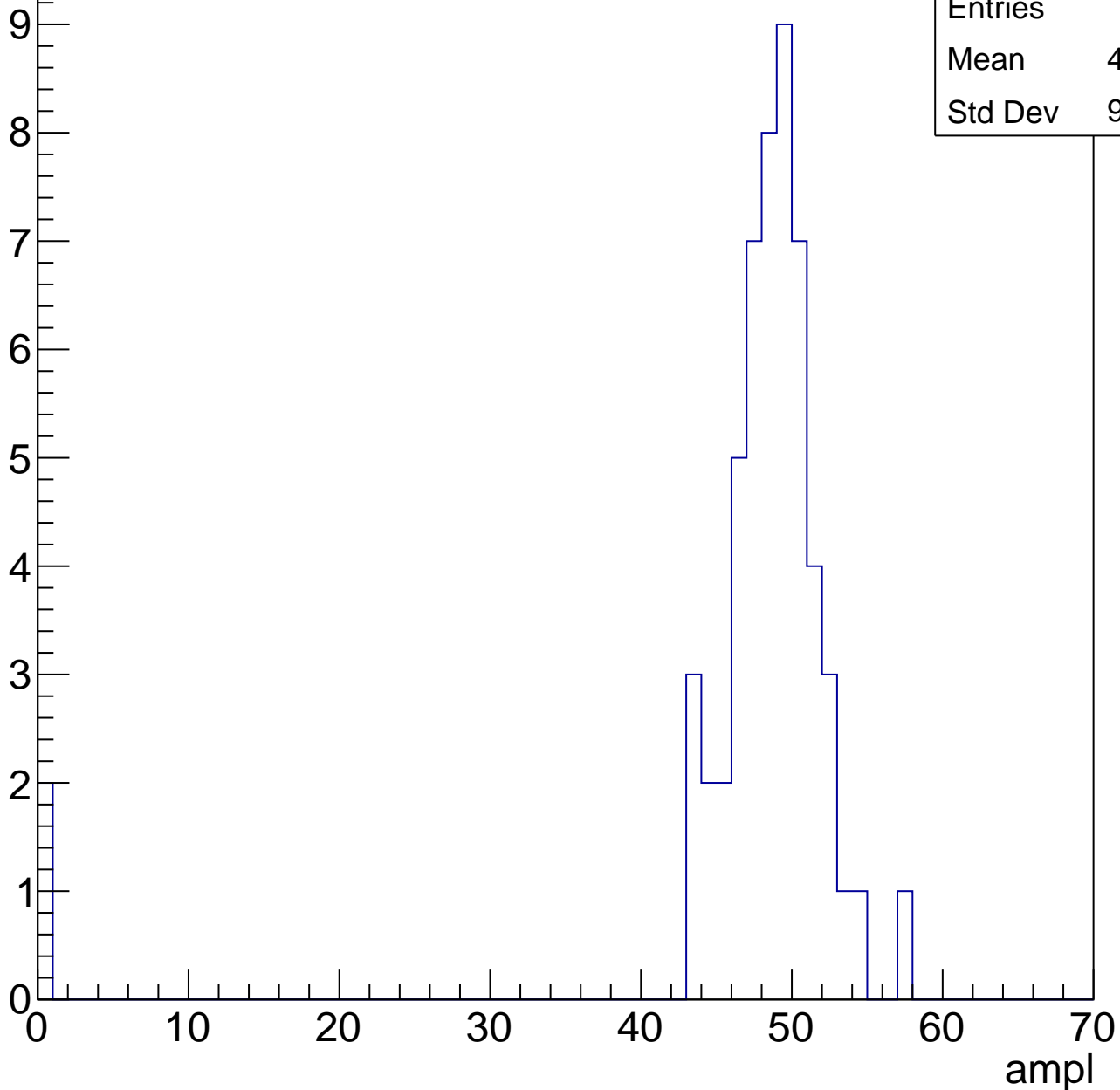


# B1L103S, U25-ch19, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

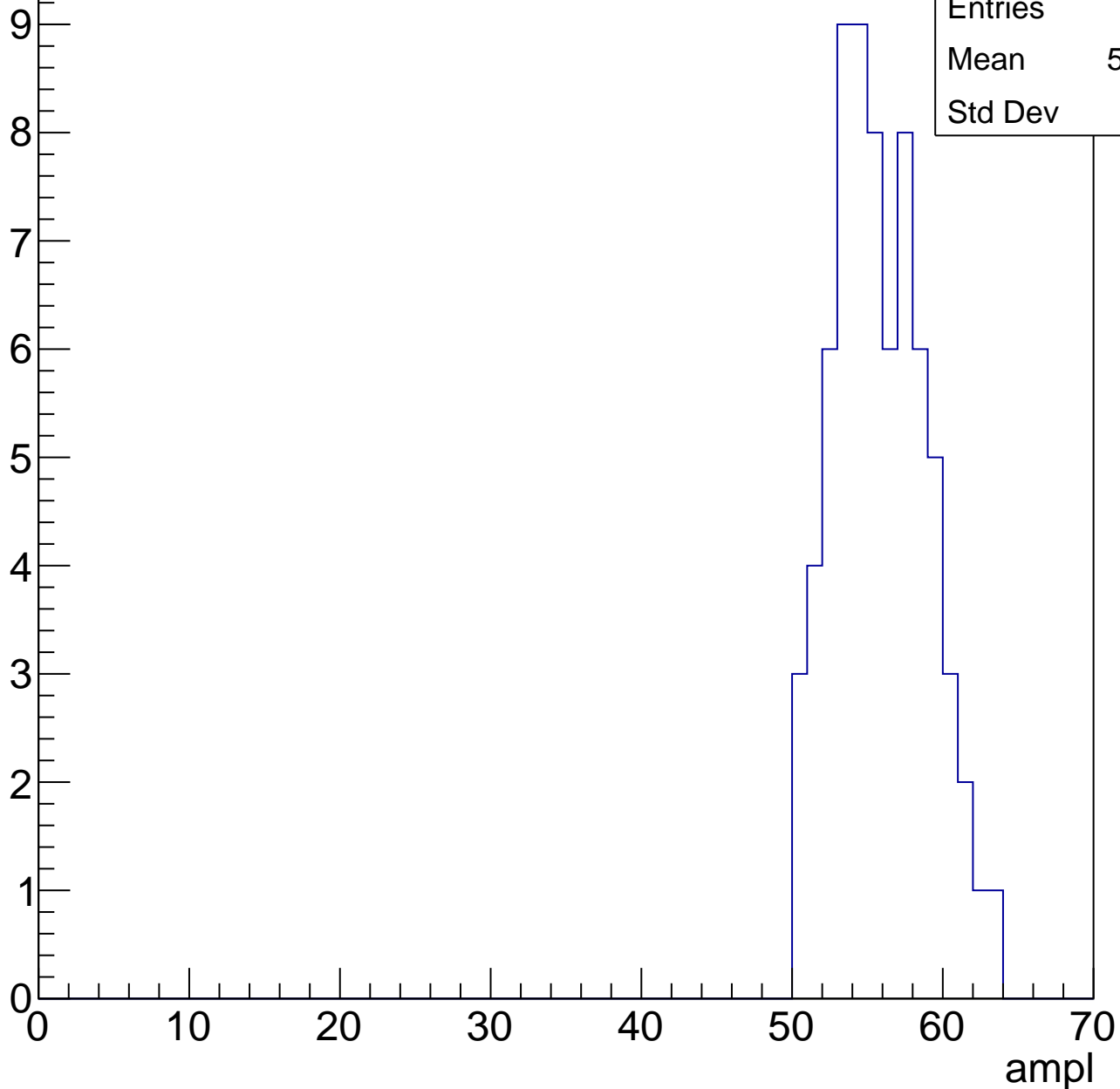
Entries	55
Mean	46.64
Std Dev	9.459



# B1L103S, U25-ch19, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



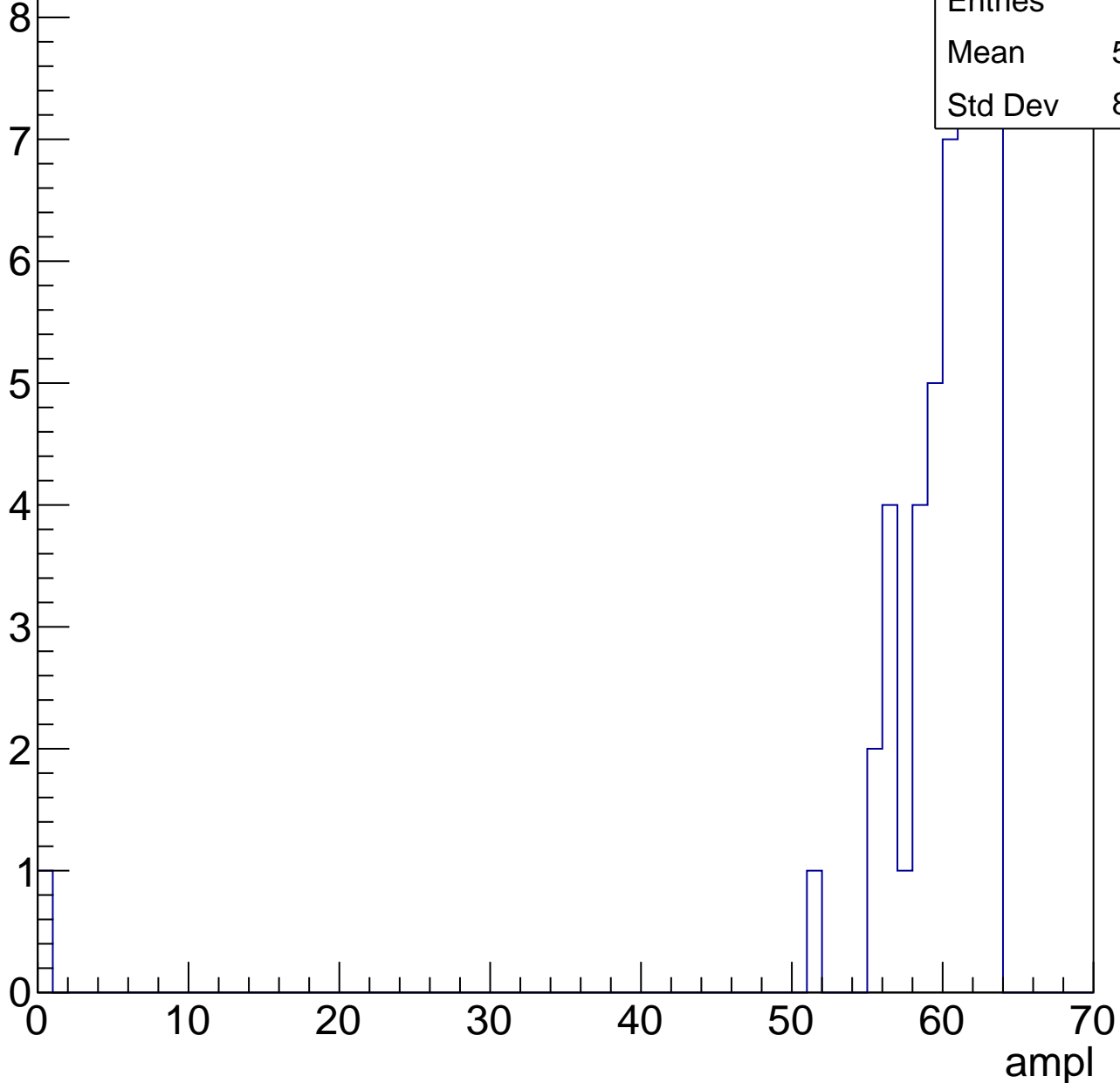
Entries	71
Mean	55.37
Std Dev	3.05

# B1L103S, U25-ch19, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	49
Mean	58.71
Std Dev	8.871



# B1L103S, U25-ch19, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U25-ch19, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

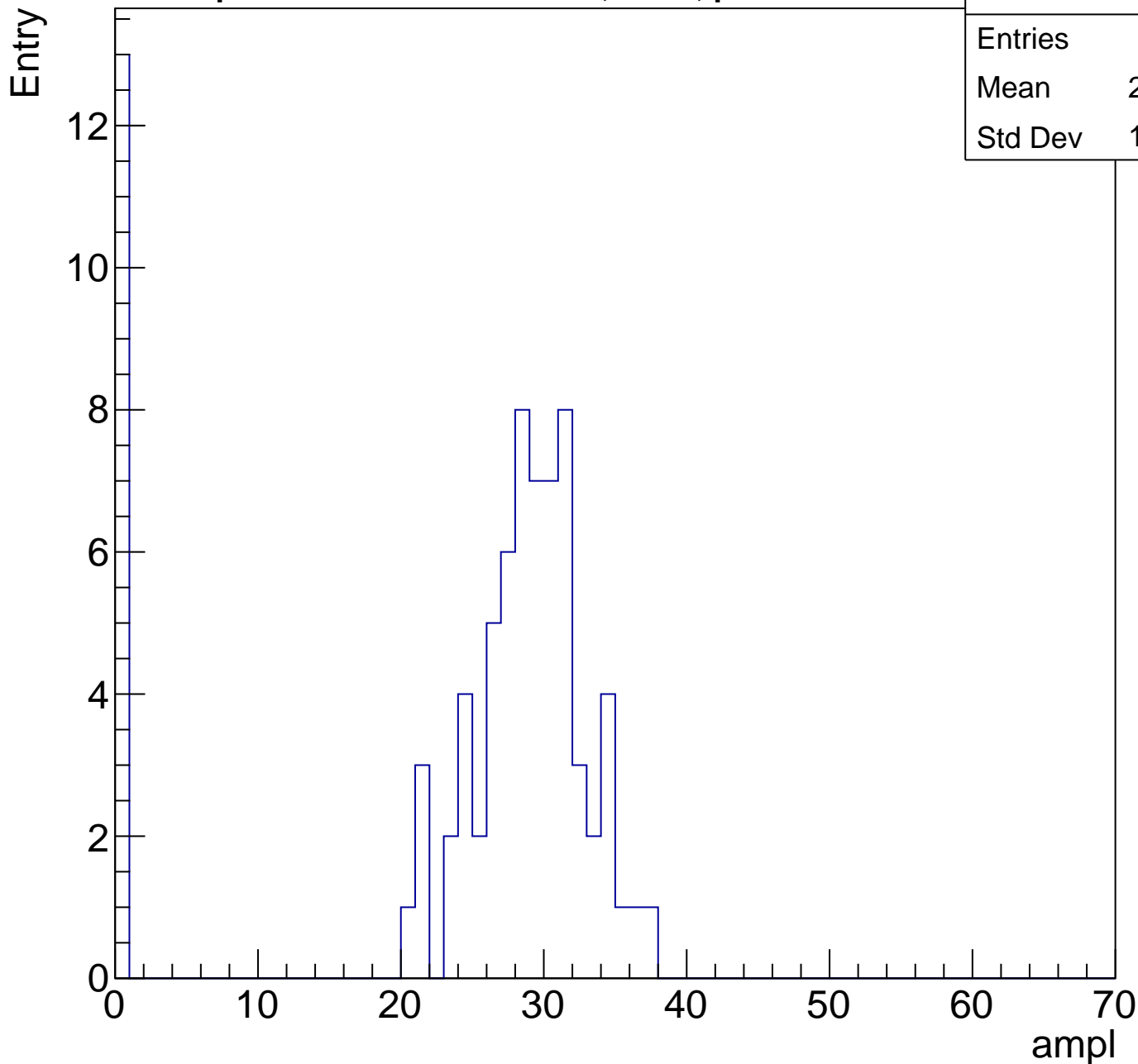
Entry



# B1L103S, U25-ch20, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

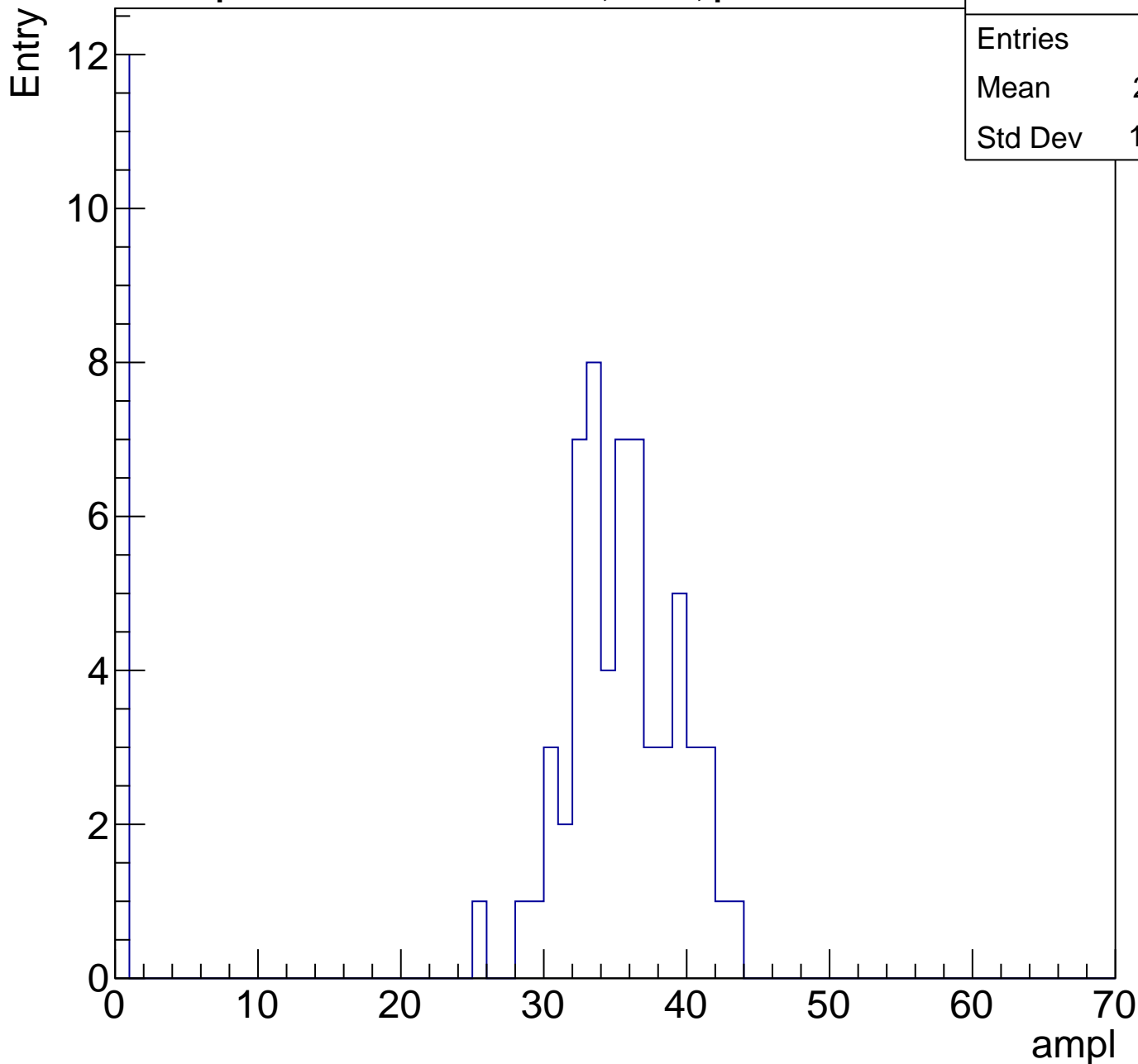
Entries	78
Mean	23.82
Std Dev	11.18



# B1L103S, U25-ch20, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	72
Mean	29.21
Std Dev	13.49

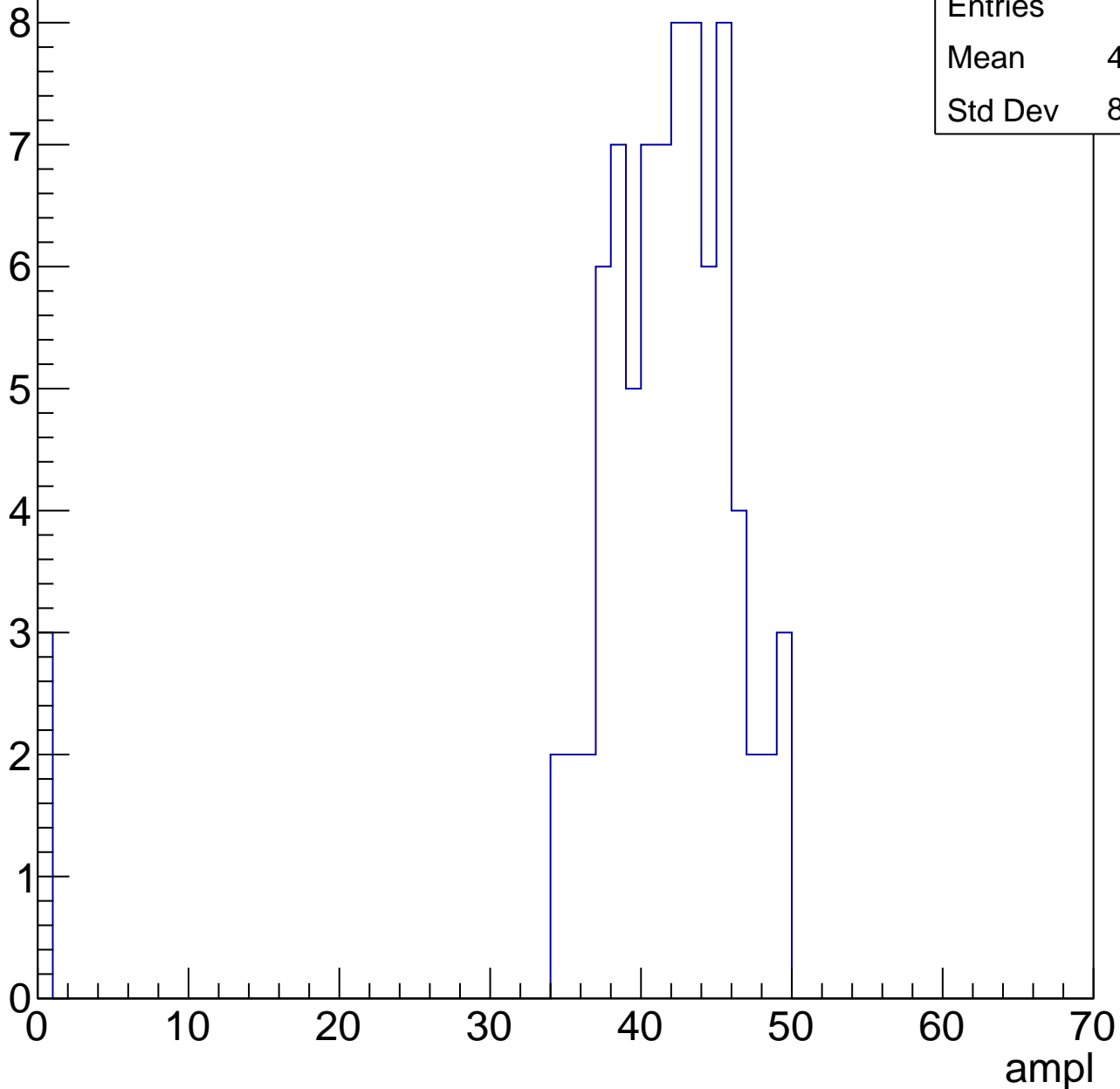


# B1L103S, U25-ch20, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	82
Mean	40.06
Std Dev	8.597

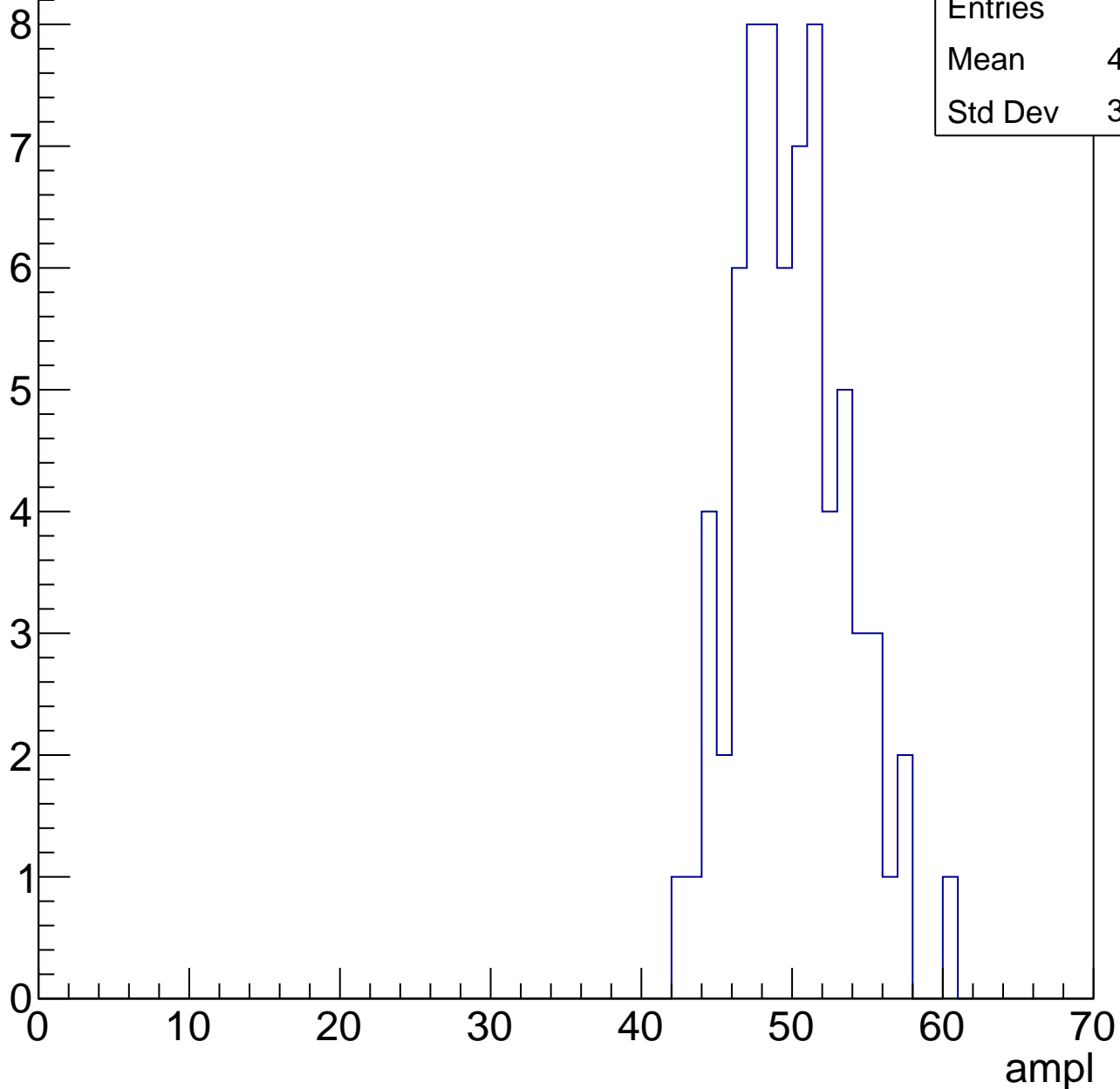


# B1L103S, U25-ch20, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	70
Mean	49.56
Std Dev	3.636

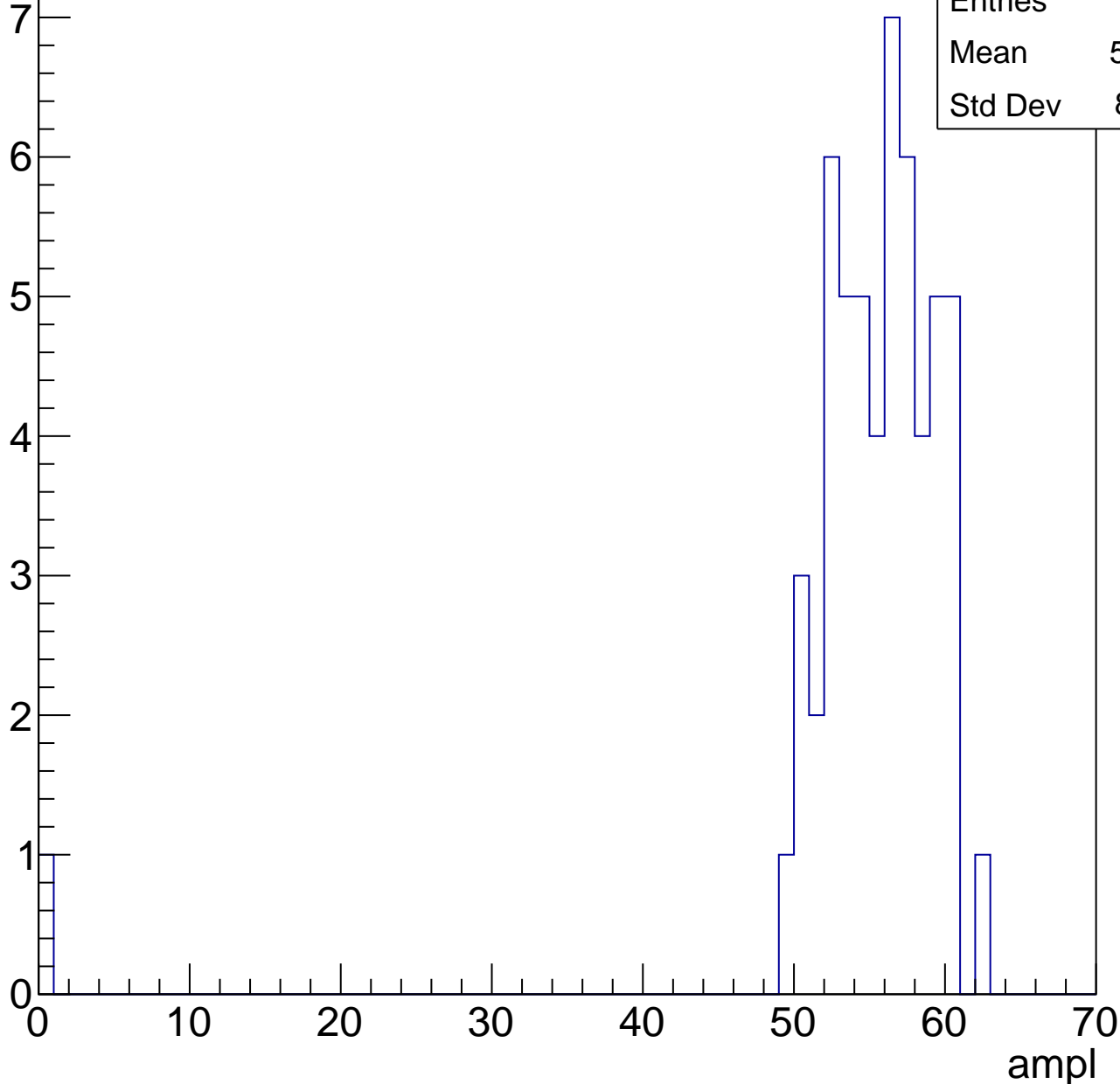


# B1L103S, U25-ch20, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	55
Mean	54.38
Std Dev	8.031

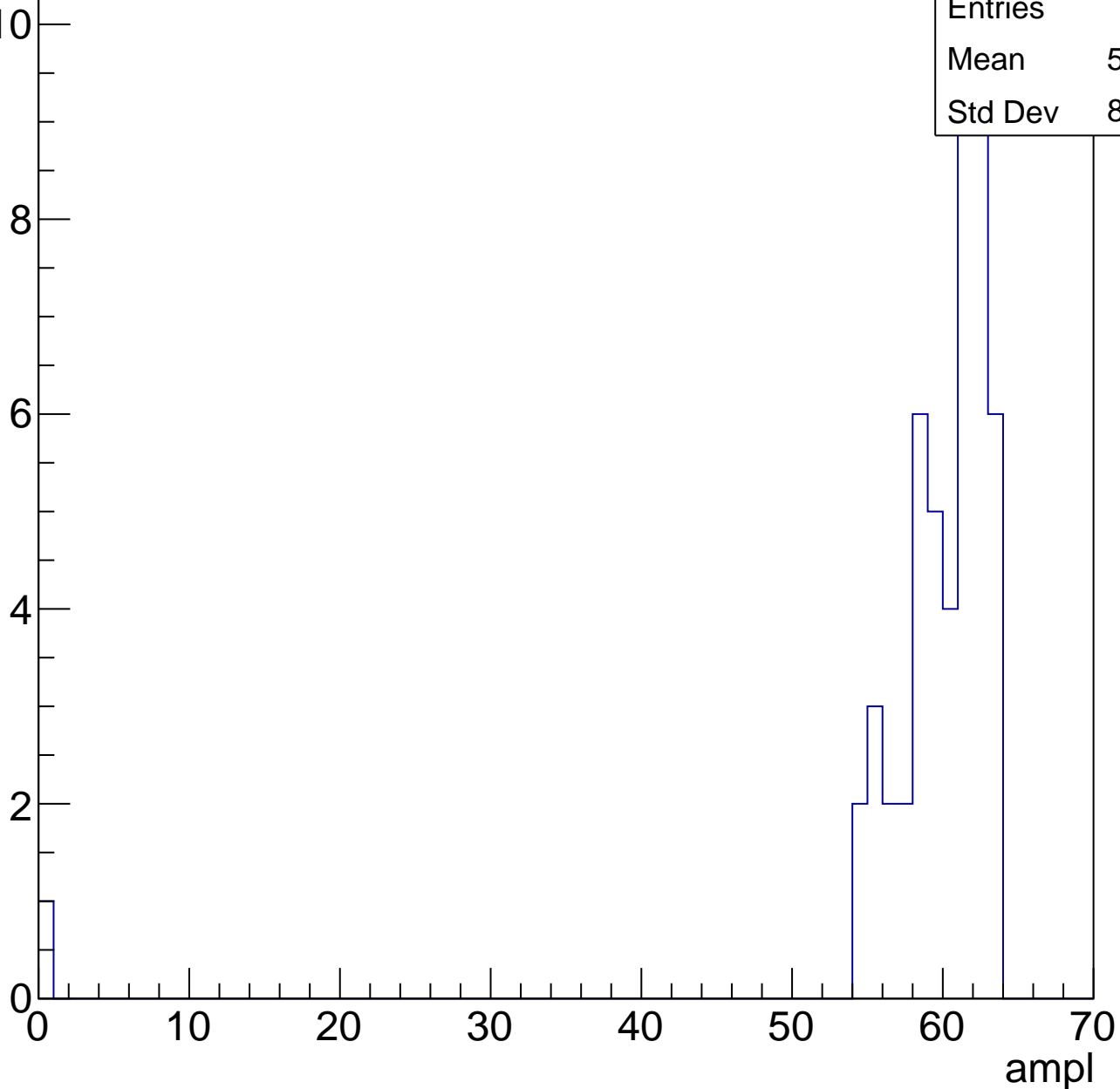


# B1L103S, U25-ch20, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	50
Mean	58.56
Std Dev	8.743



# B1L103S, U25-ch20, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U25-ch20, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

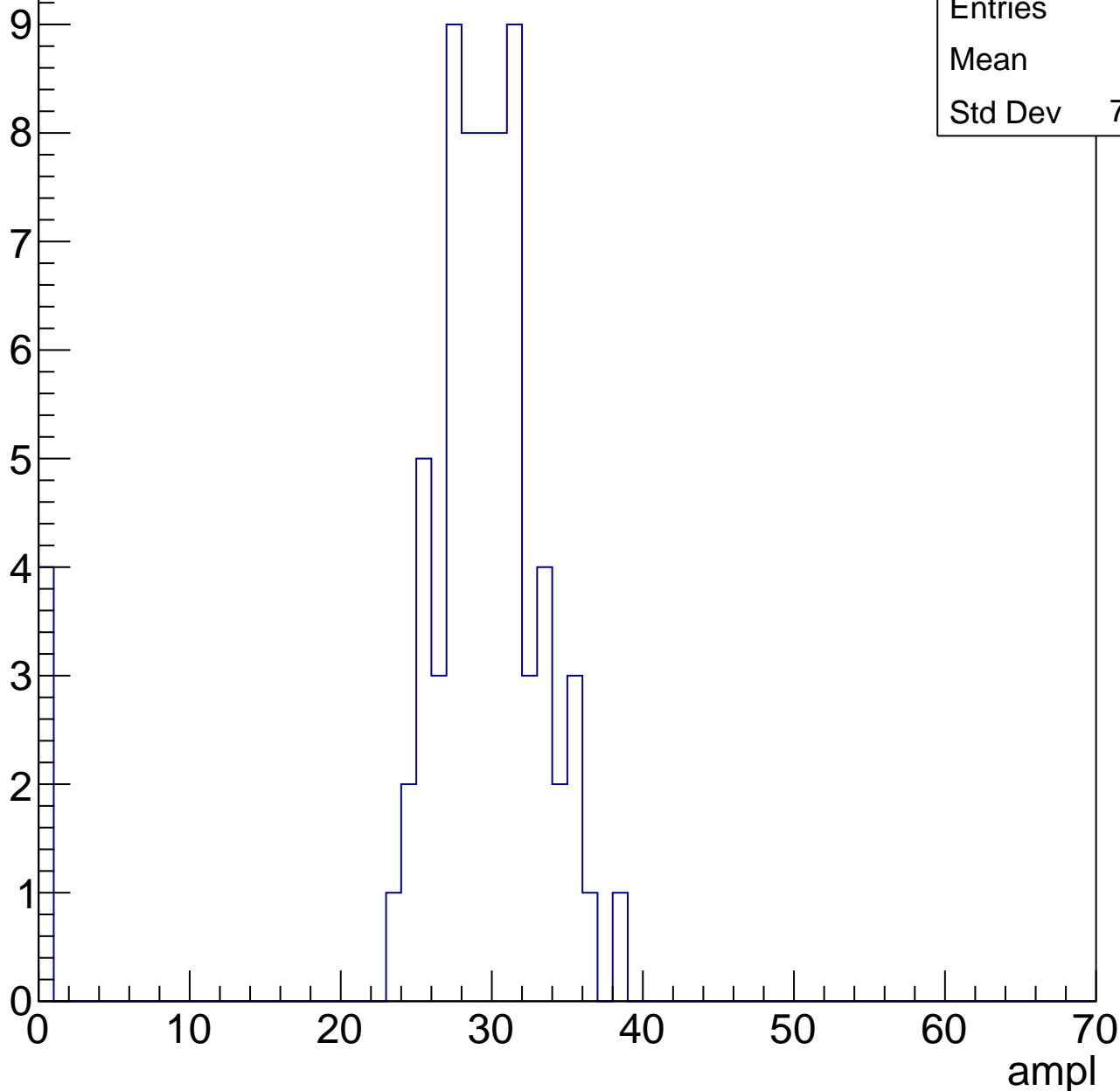
Entries	19
Mean	0
Std Dev	0

# B1L103S, U25-ch21, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	71
Mean	27.7
Std Dev	7.416



# B1L103S, U25-ch21, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

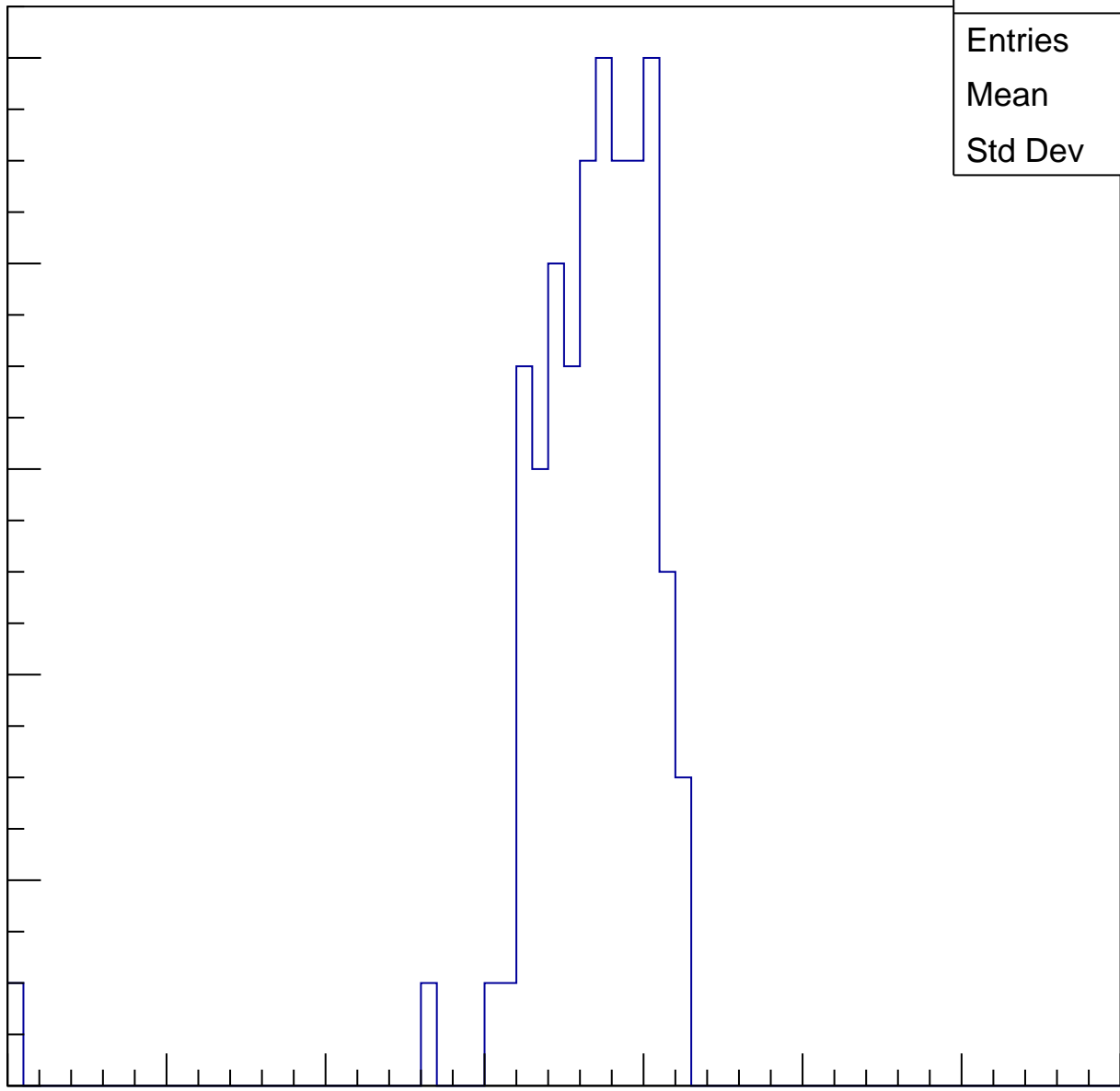
Entries	87
Mean	36.14
Std Dev	5.006

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

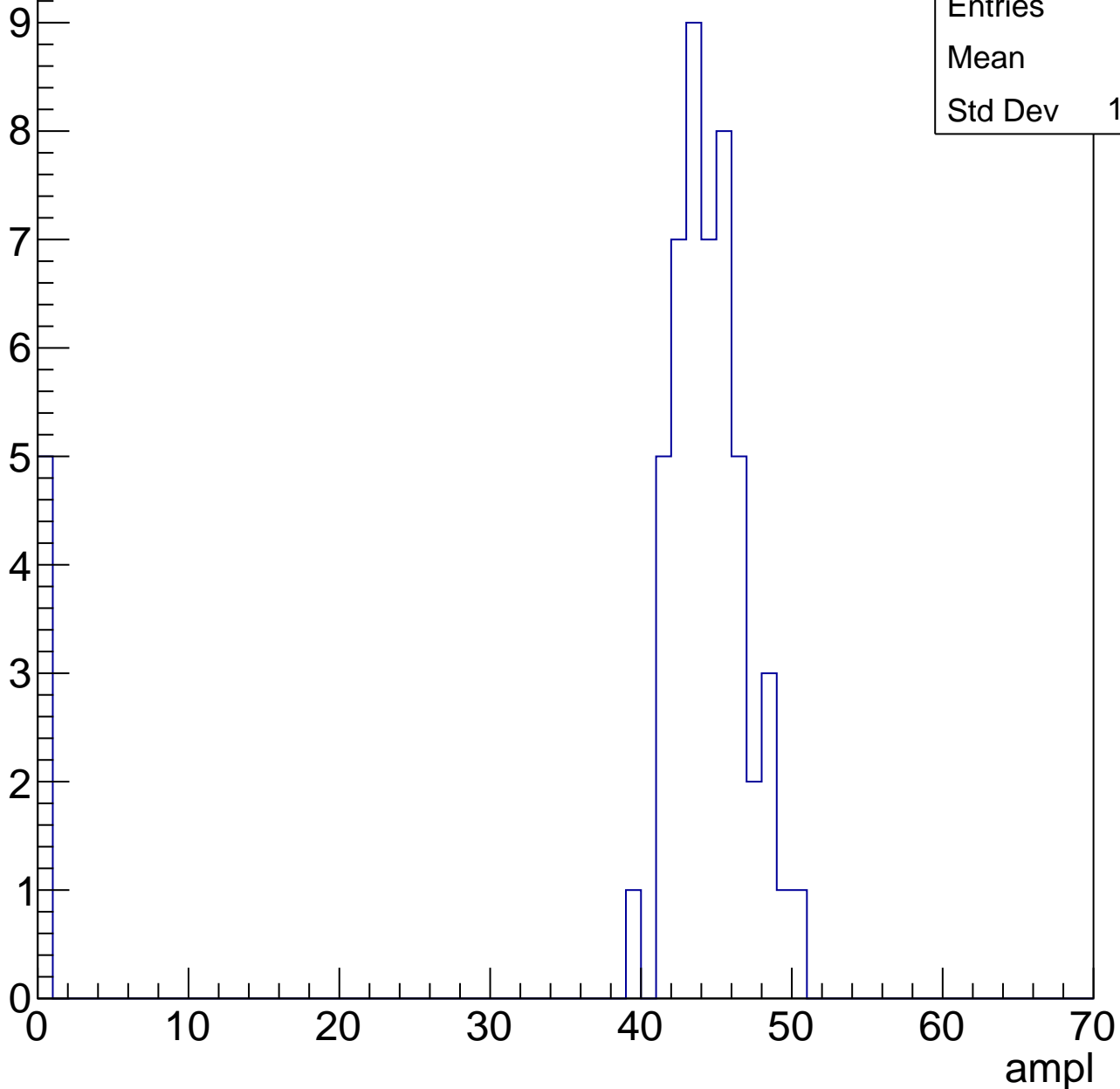


# B1L103S, U25-ch21, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	54
Mean	40
Std Dev	12.97

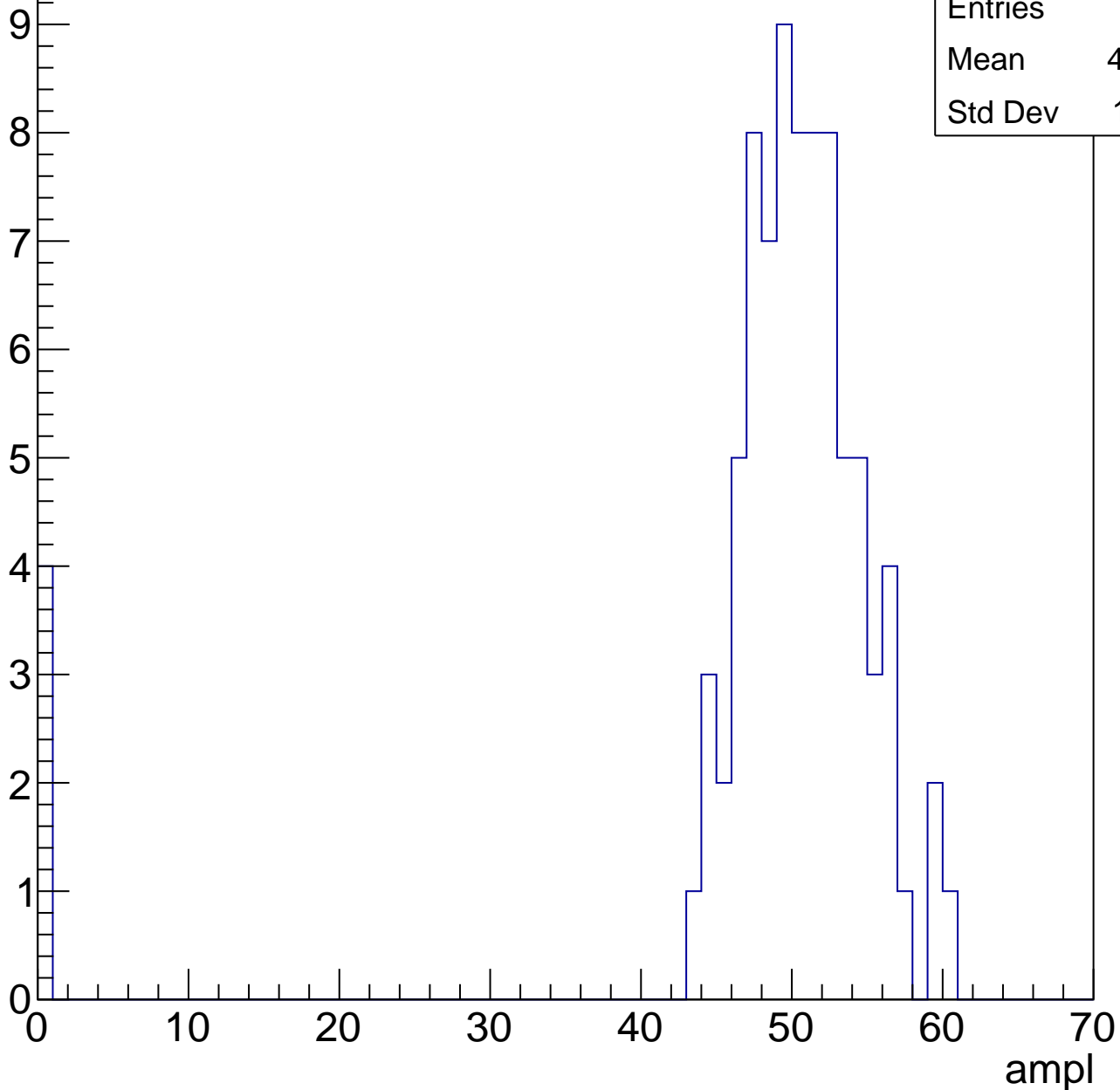


# B1L103S, U25-ch21, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	84
Mean	47.99
Std Dev	11.31

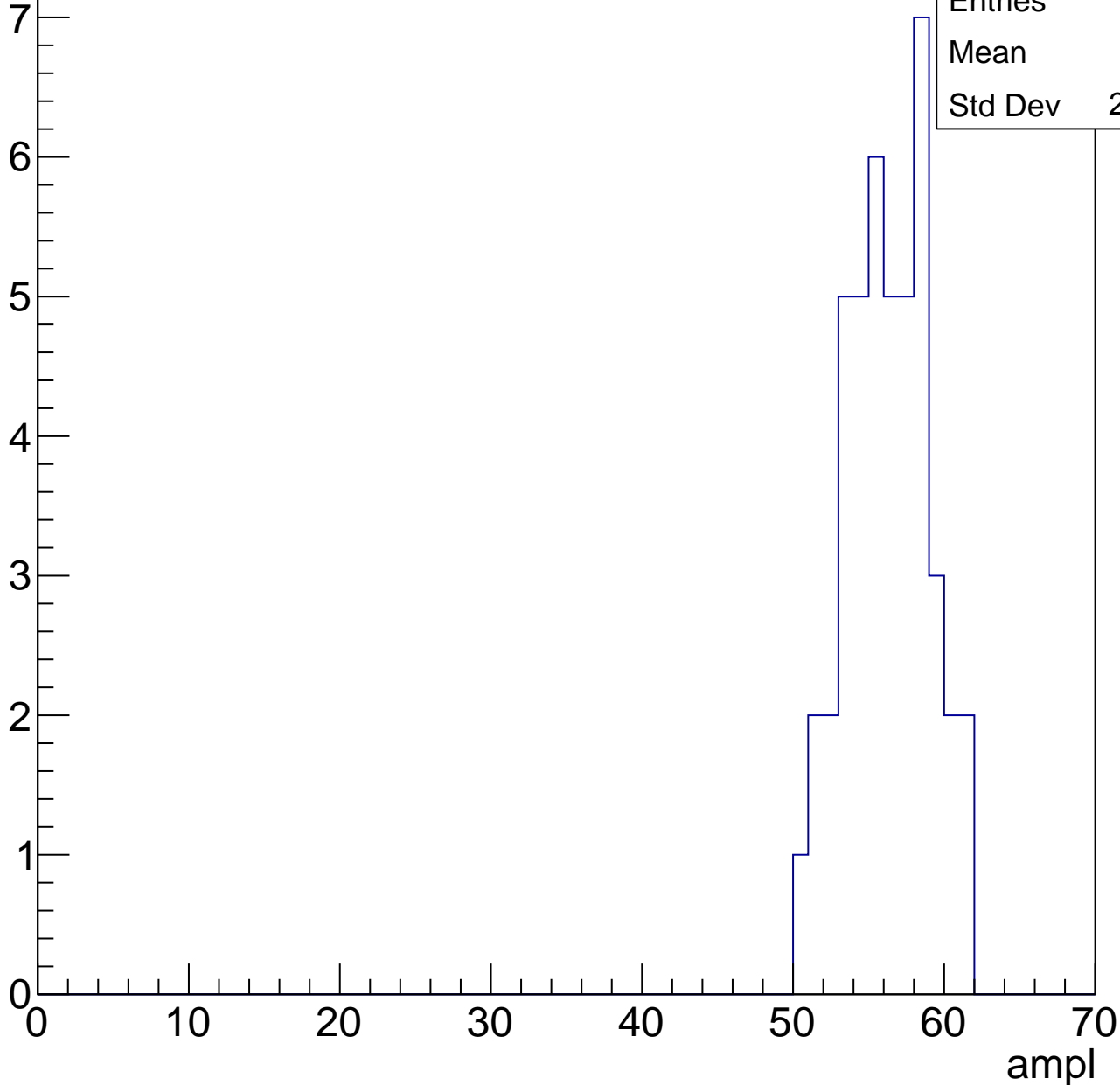


# B1L103S, U25-ch21, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	45
Mean	55.8
Std Dev	2.705

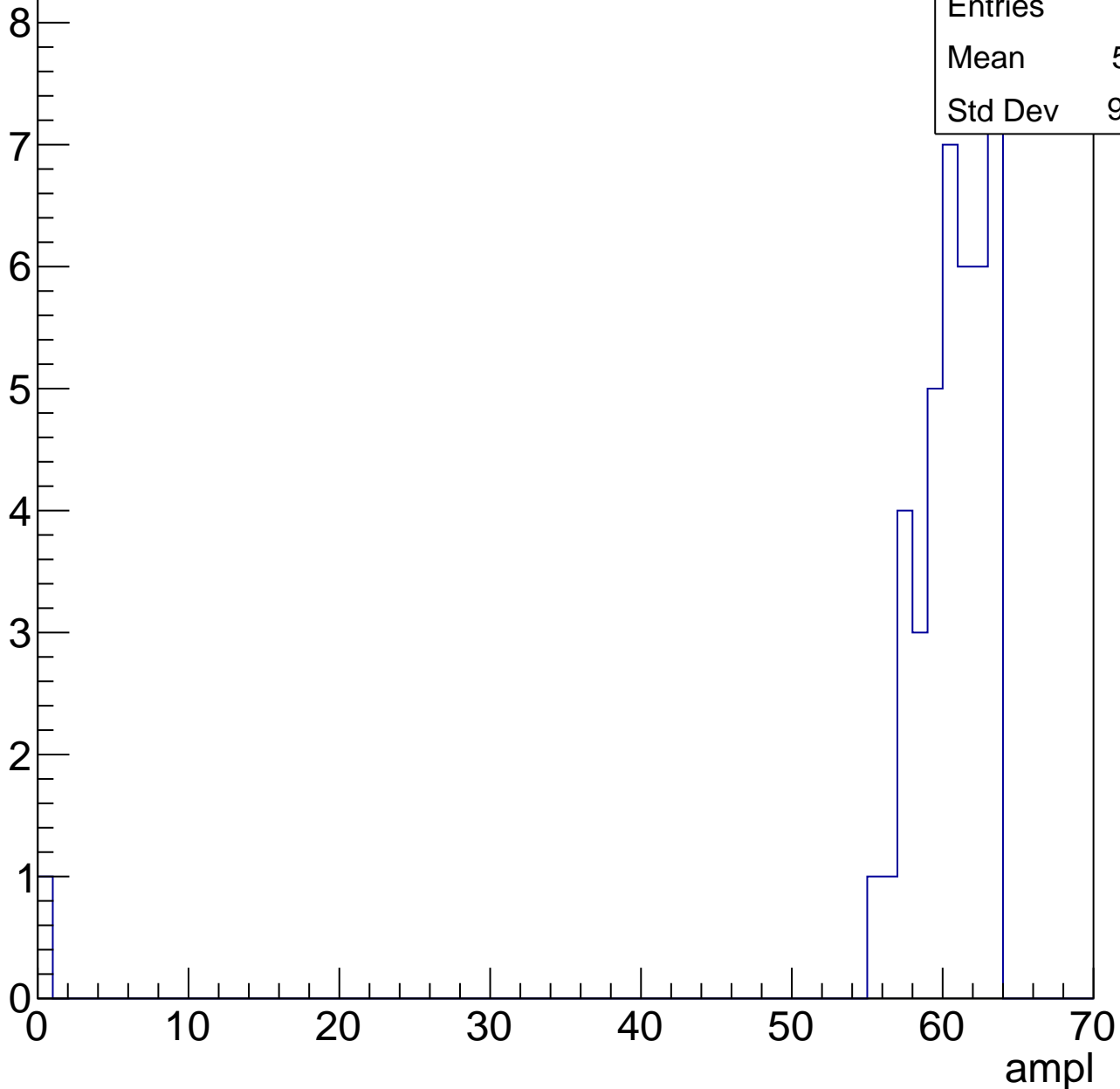


# B1L103S, U25-ch21, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

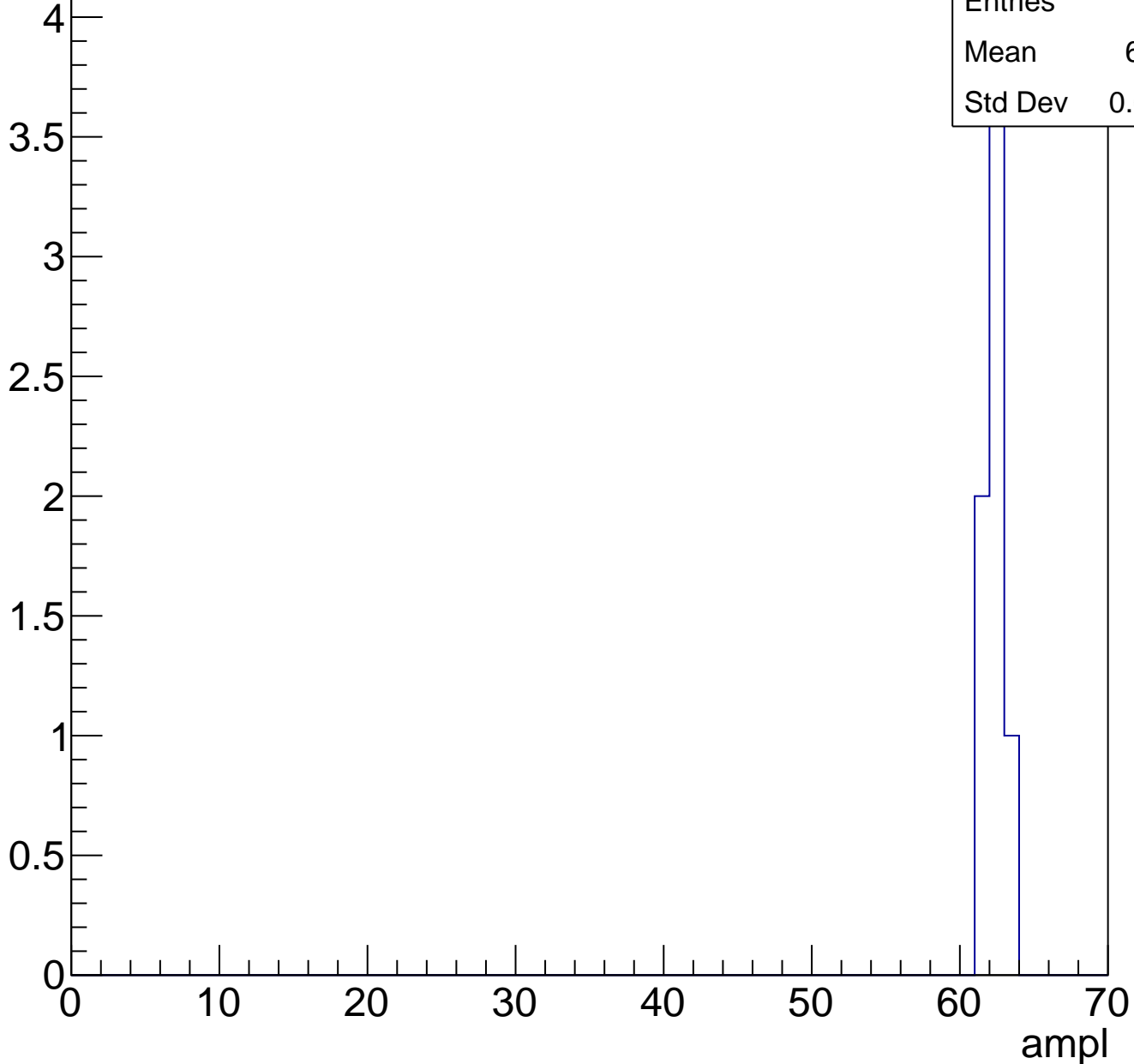
Entries	42
Mean	58.81
Std Dev	9.432



# B1L103S, U25-ch21, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



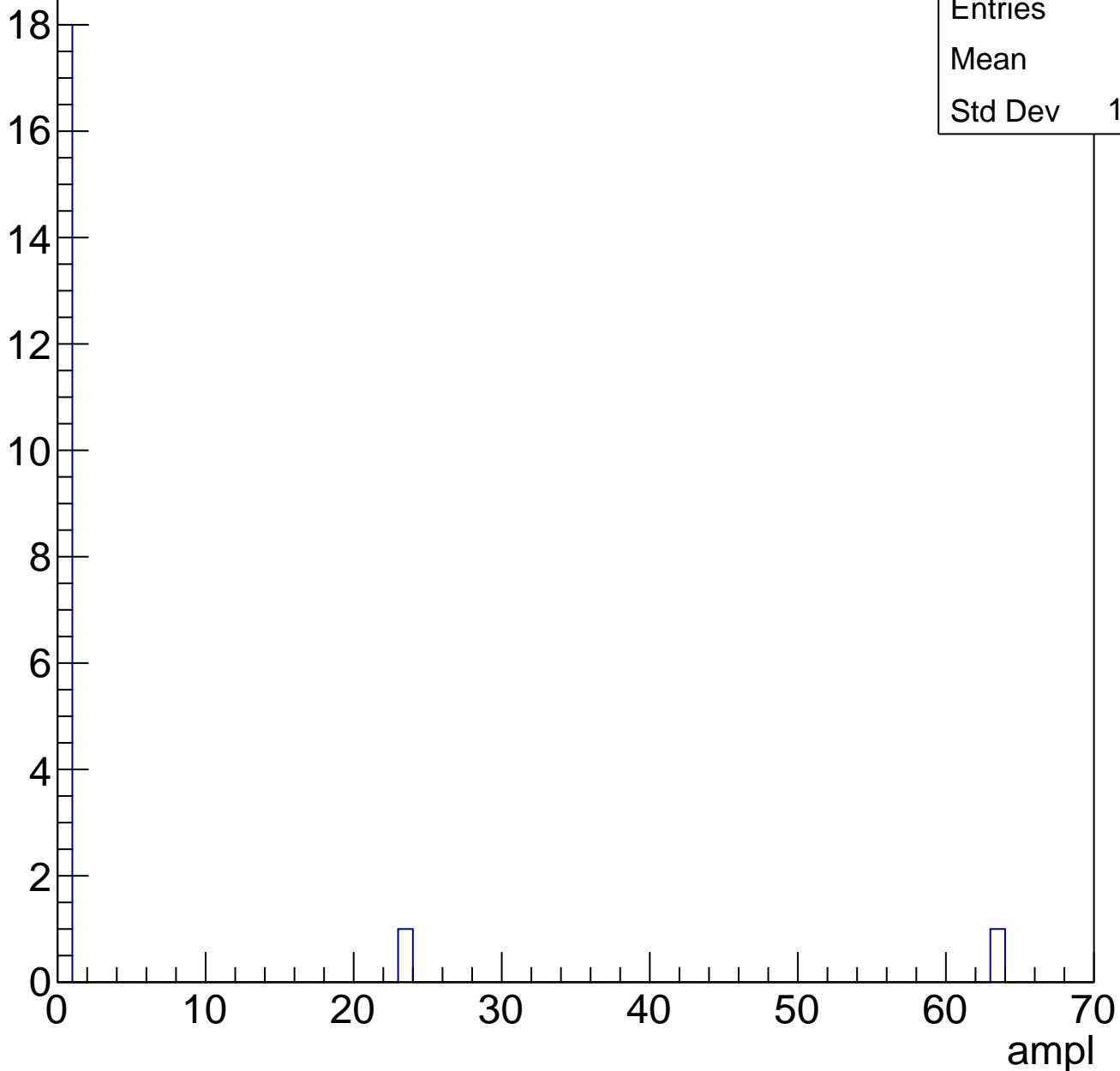


# B1L103S, U25-ch21, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	20
Mean	4.3
Std Dev	14.37

Entry

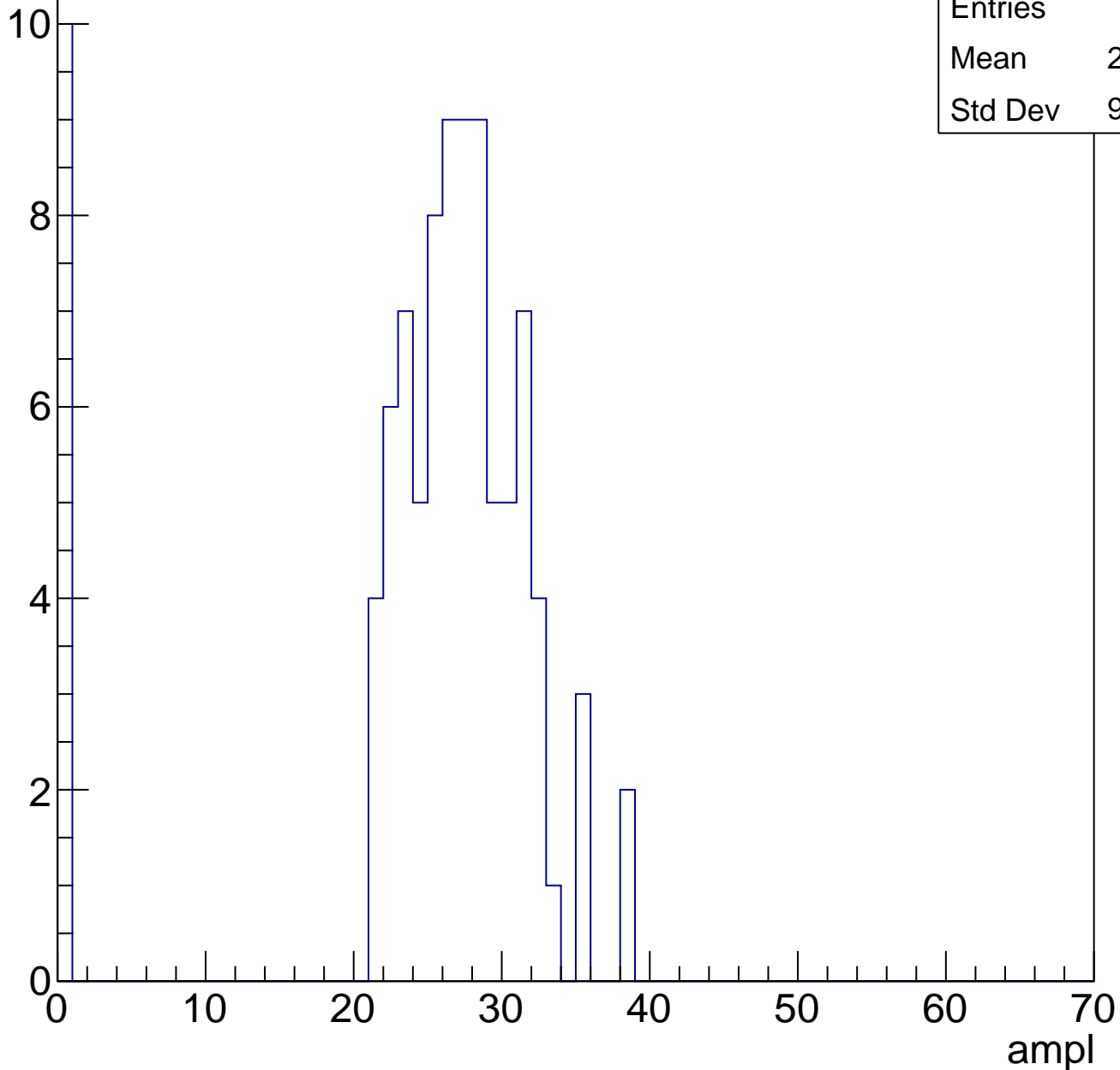


# B1L103S, U25-ch22, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	94
Mean	24.26
Std Dev	9.127

Entry

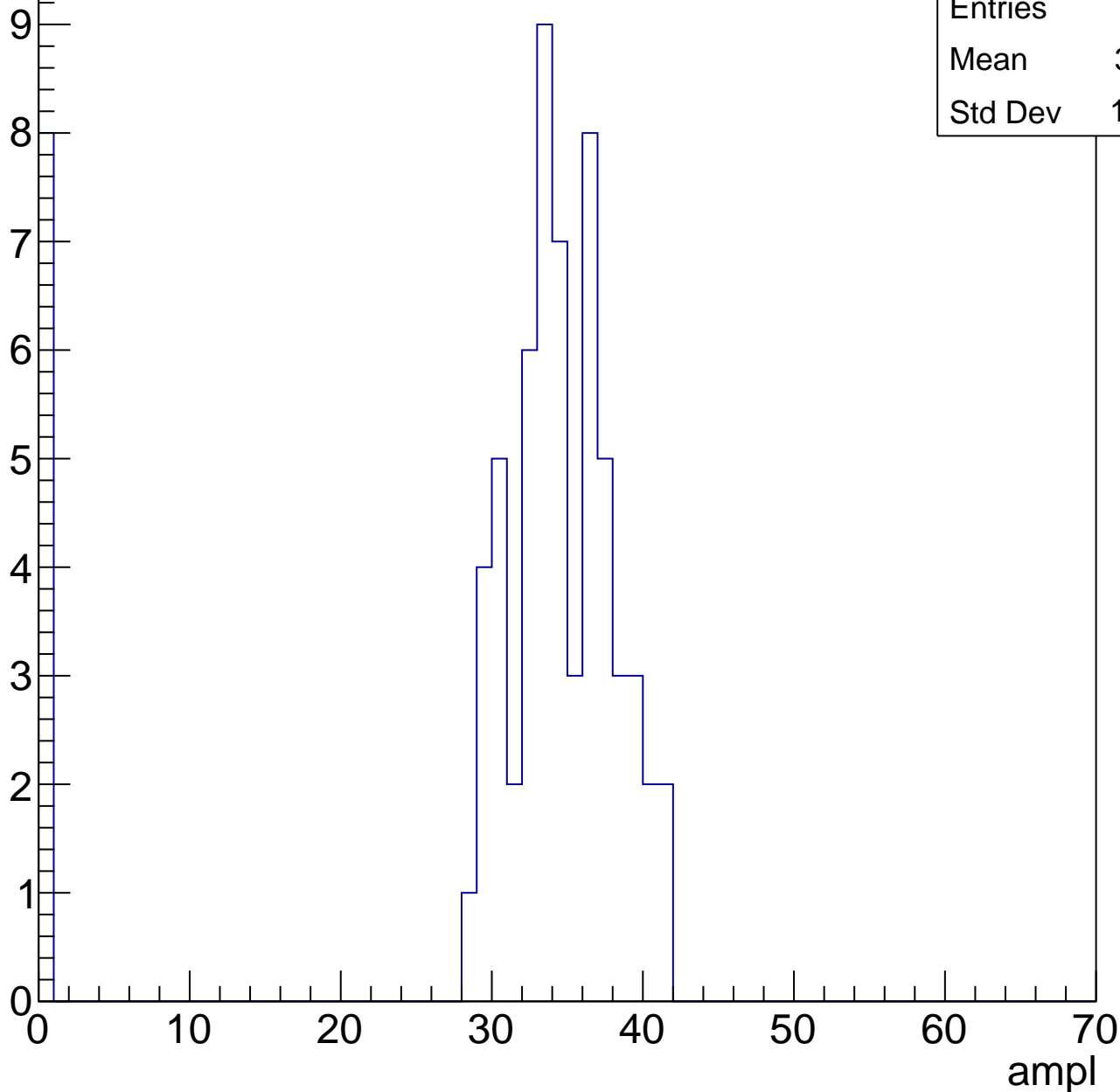


# B1L103S, U25-ch22, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	68
Mean	30.21
Std Dev	11.45

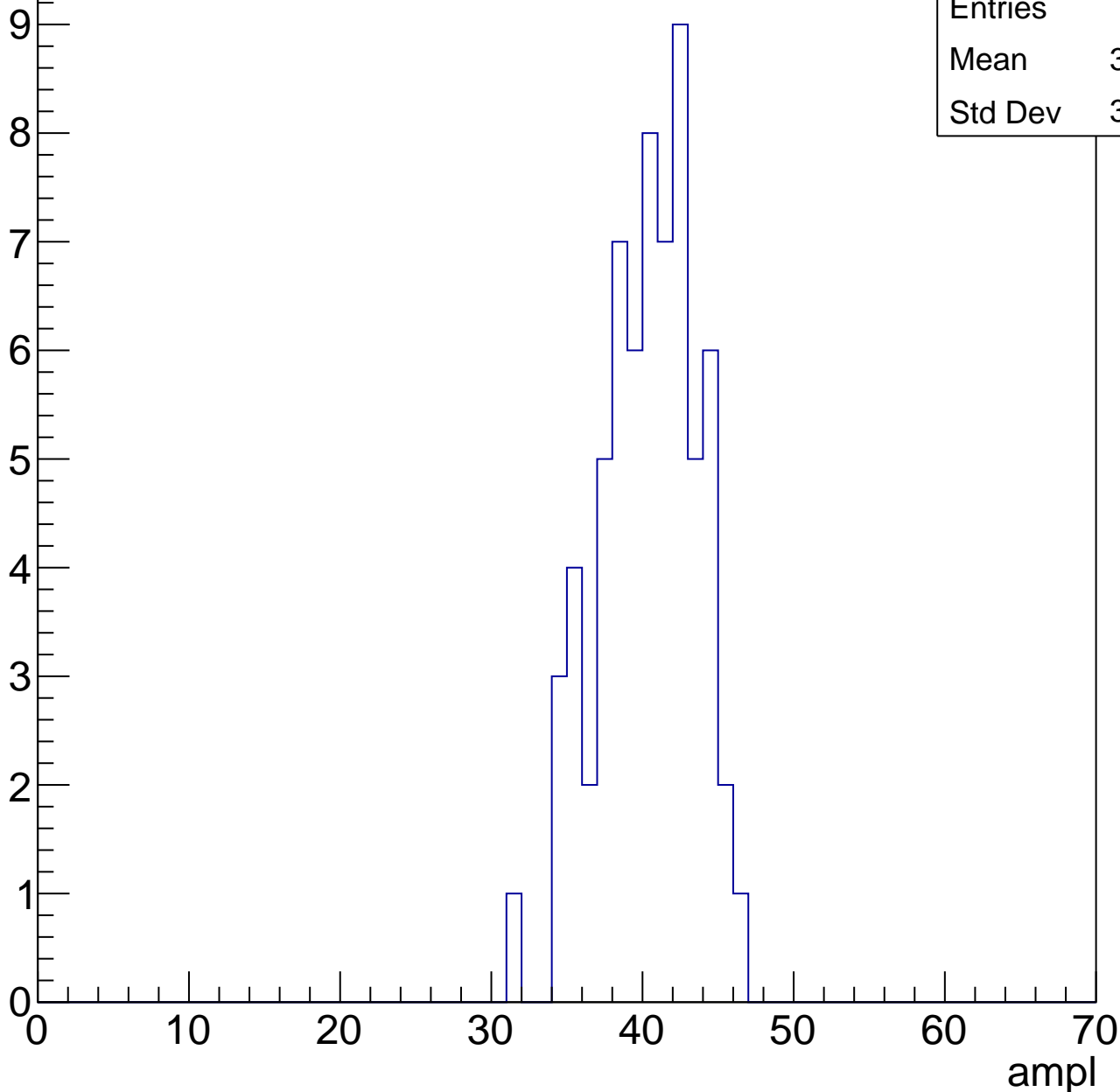


# B1L103S, U25-ch22, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	66
Mean	39.85
Std Dev	3.183

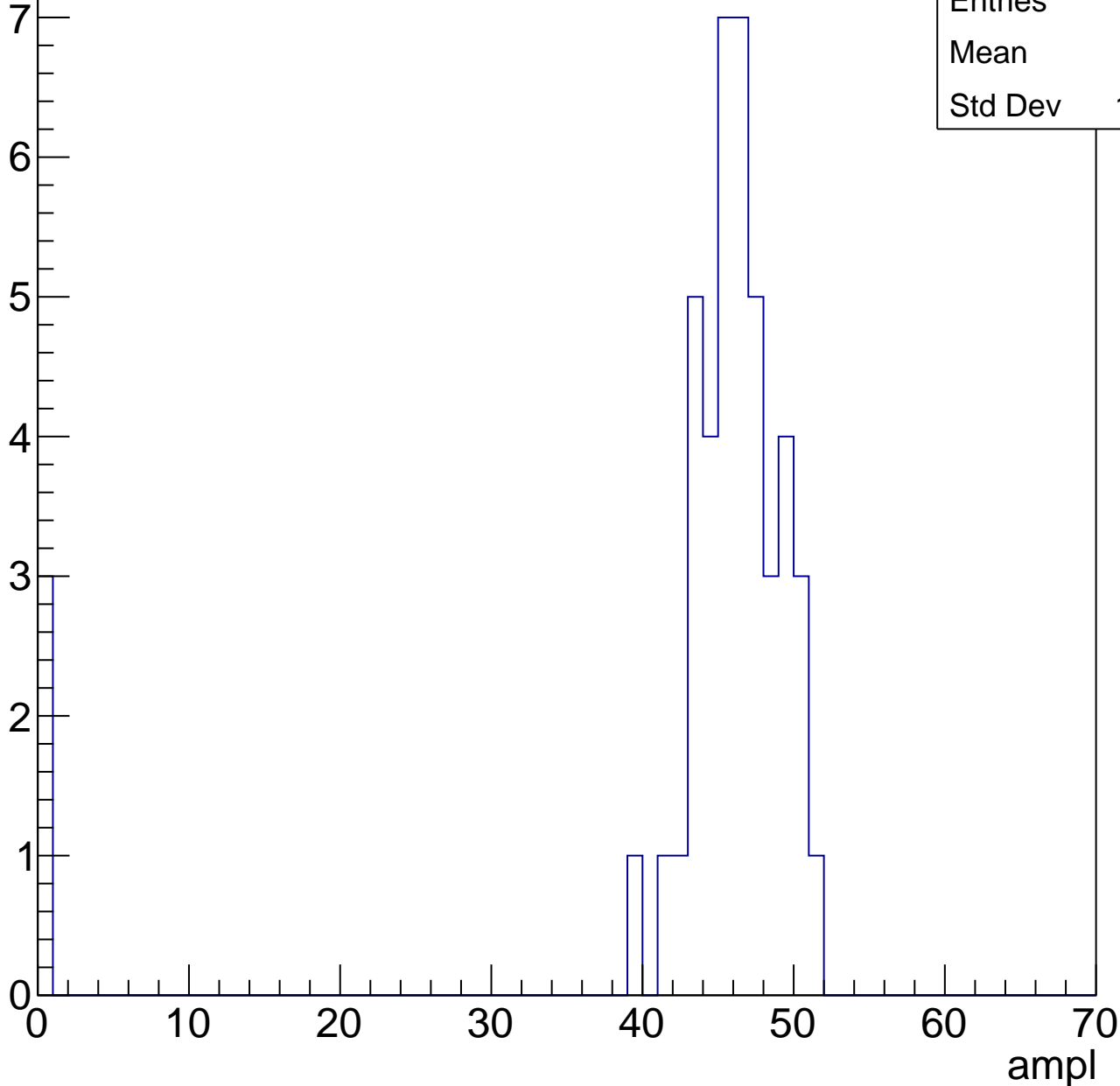


# B1L103S, U25-ch22, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	45
Mean	42.8
Std Dev	11.71



# B1L103S, U25-ch22, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

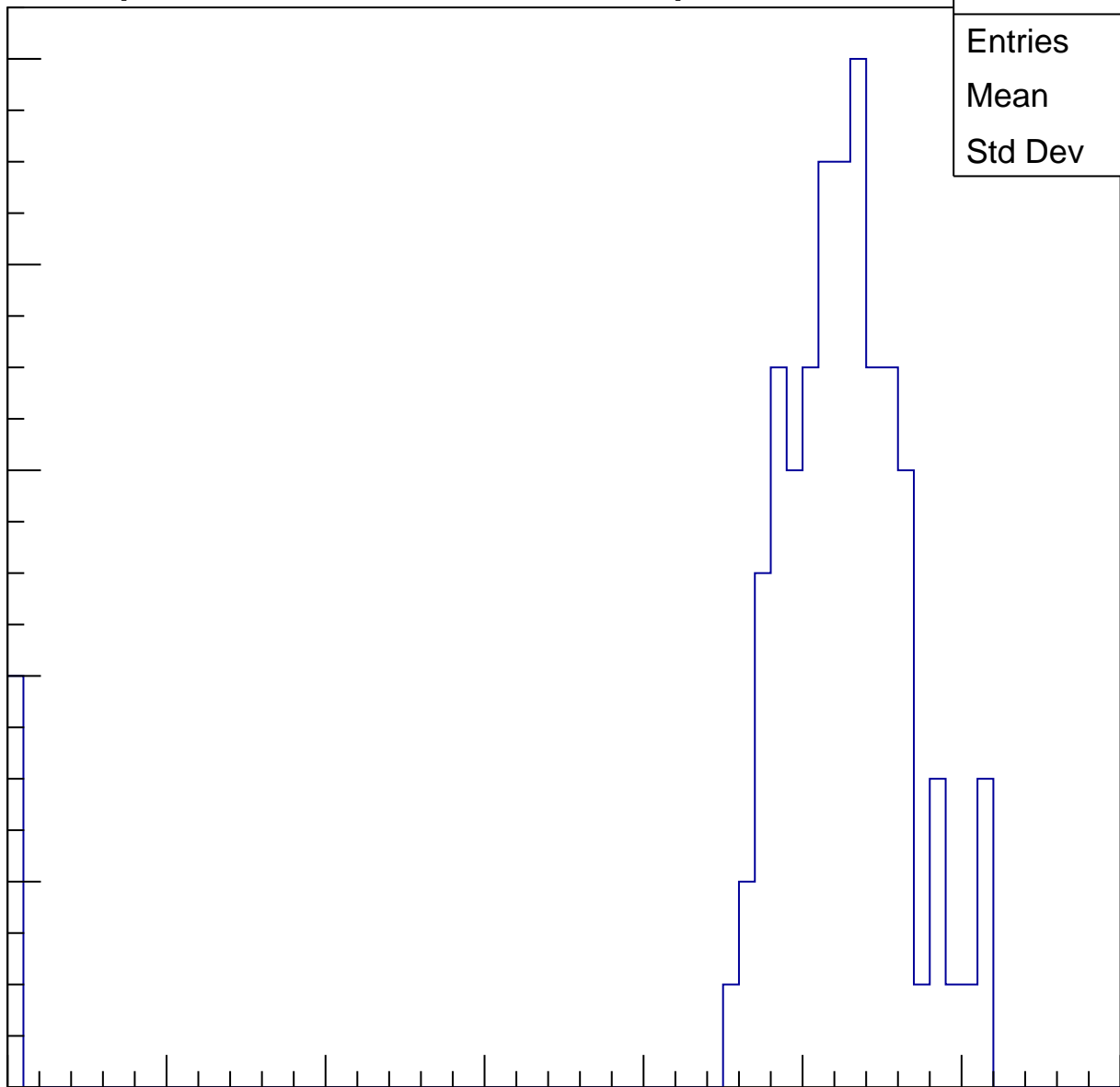
Entries	89
Mean	49.9
Std Dev	11.4

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

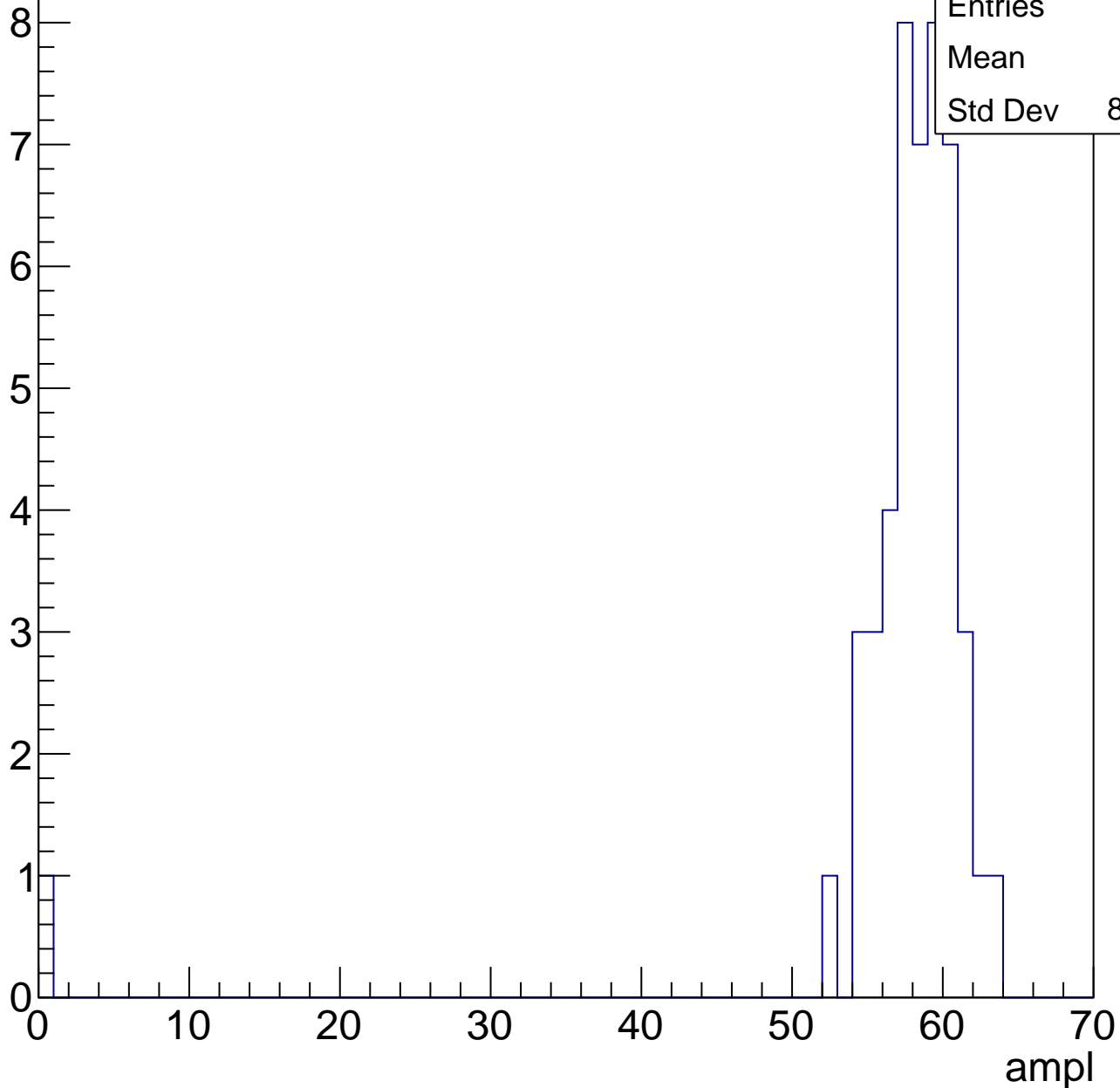
ampl



# B1L103S, U25-ch22, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

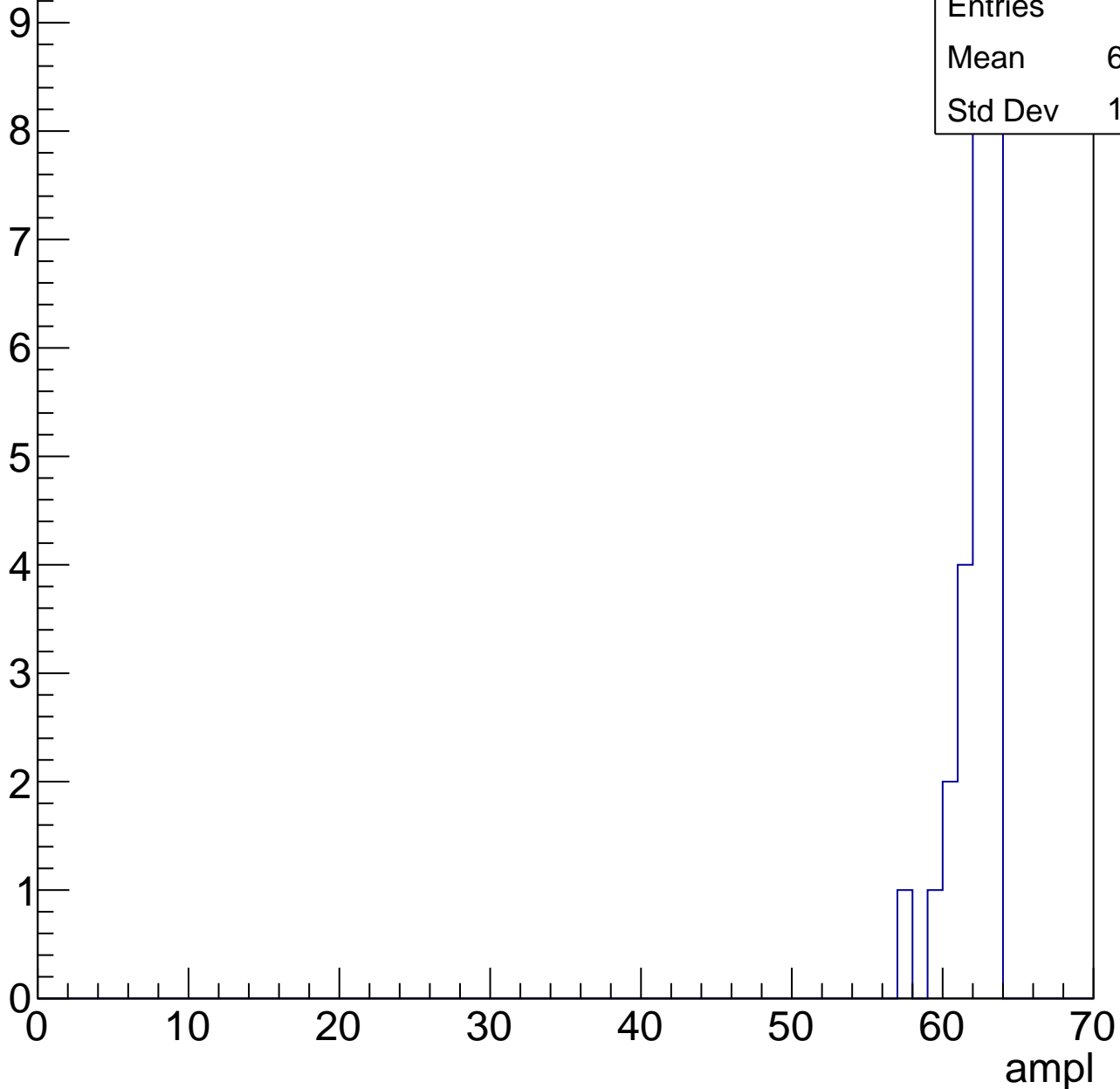


# B1L103S, U25-ch22, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	25
Mean	61.72
Std Dev	1.457





# B1L103S, U25-ch22, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	19
Mean	3.263
Std Dev	13.84

Entry



# B1L103S, U25-ch23, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

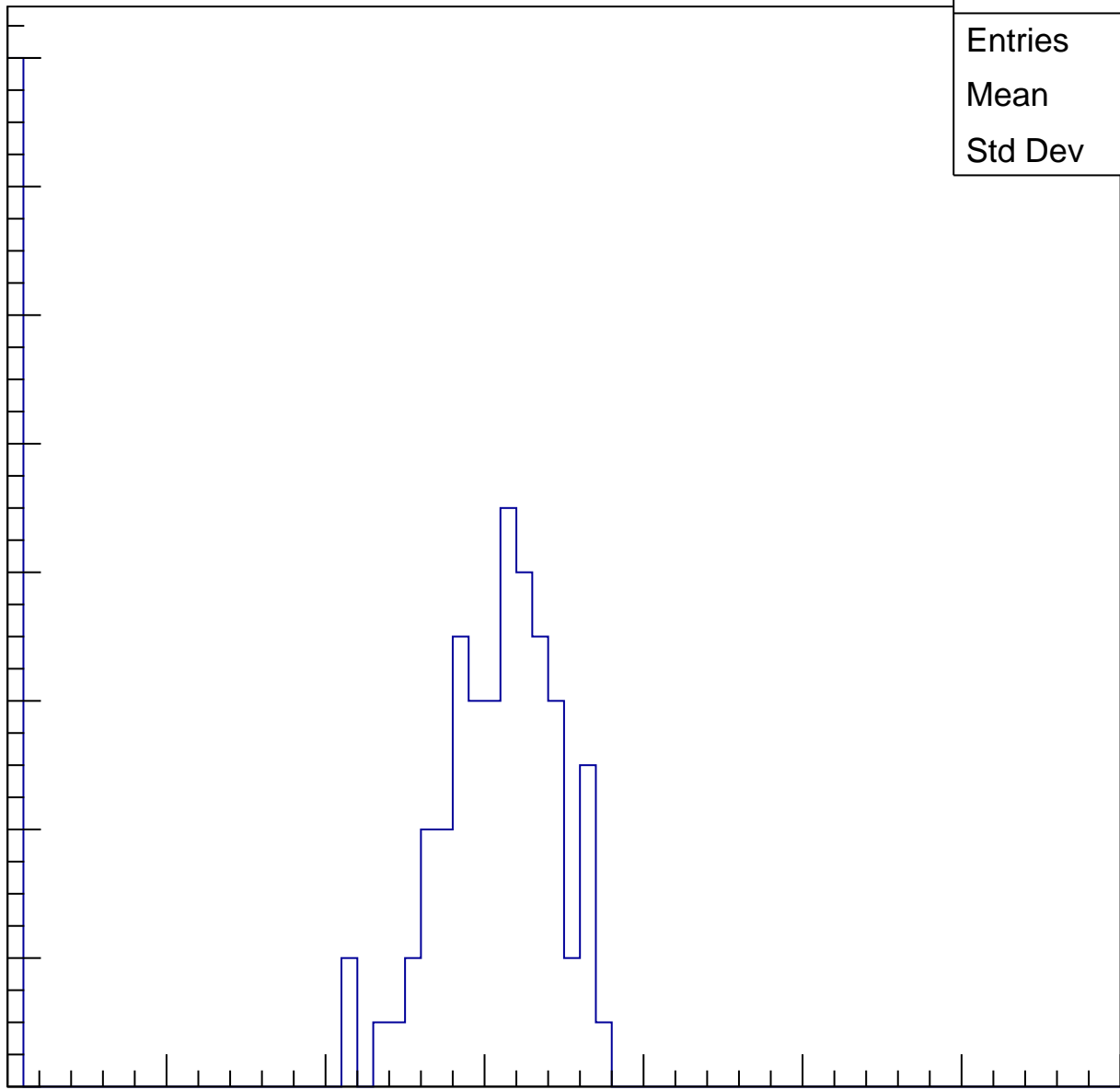
Entries	87
Mean	24.8
Std Dev	12.21

Entry

16  
14  
12  
10  
8  
6  
4  
2  
0

ampl

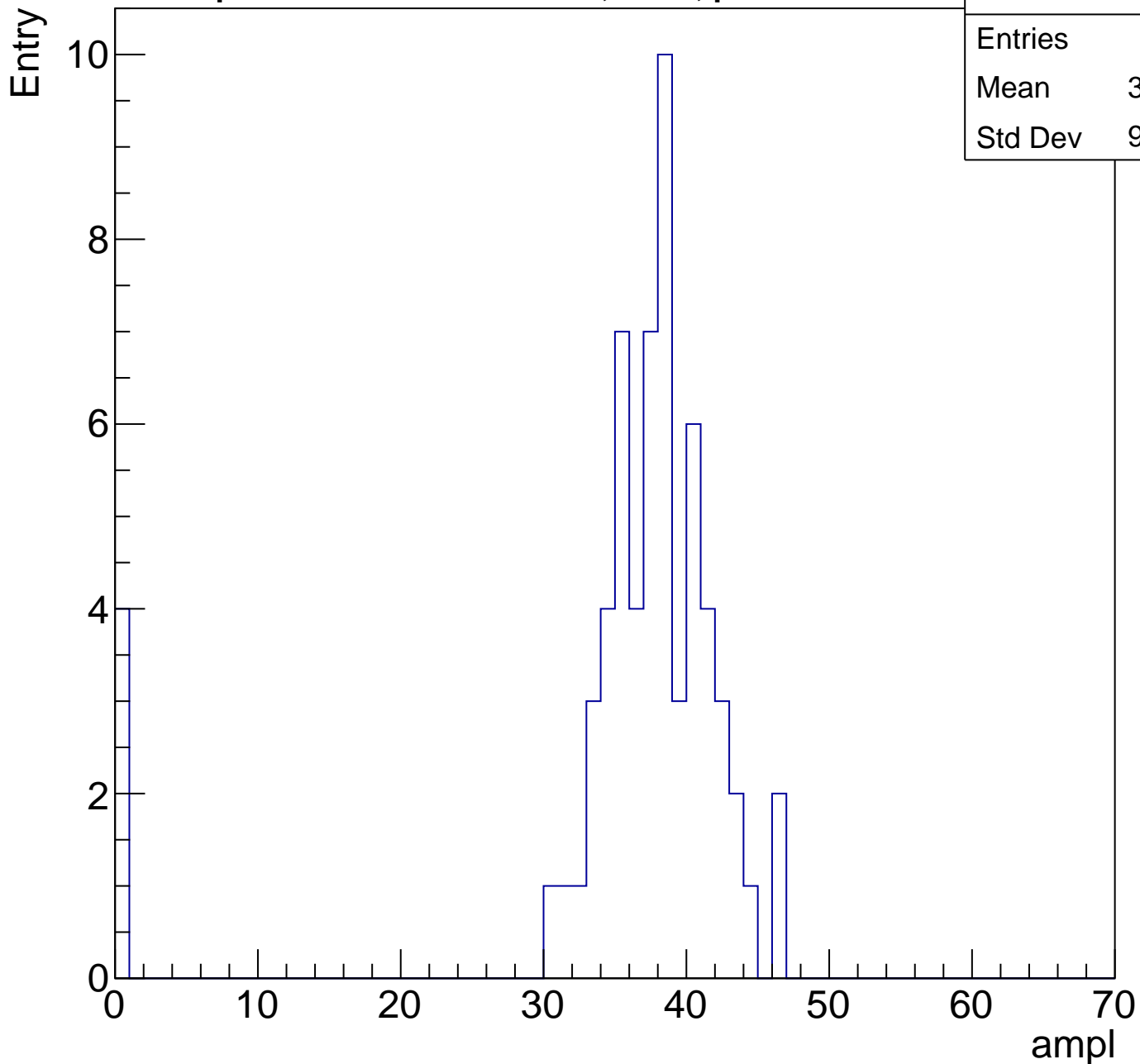
0 10 20 30 40 50 60 70



# B1L103S, U25-ch23, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

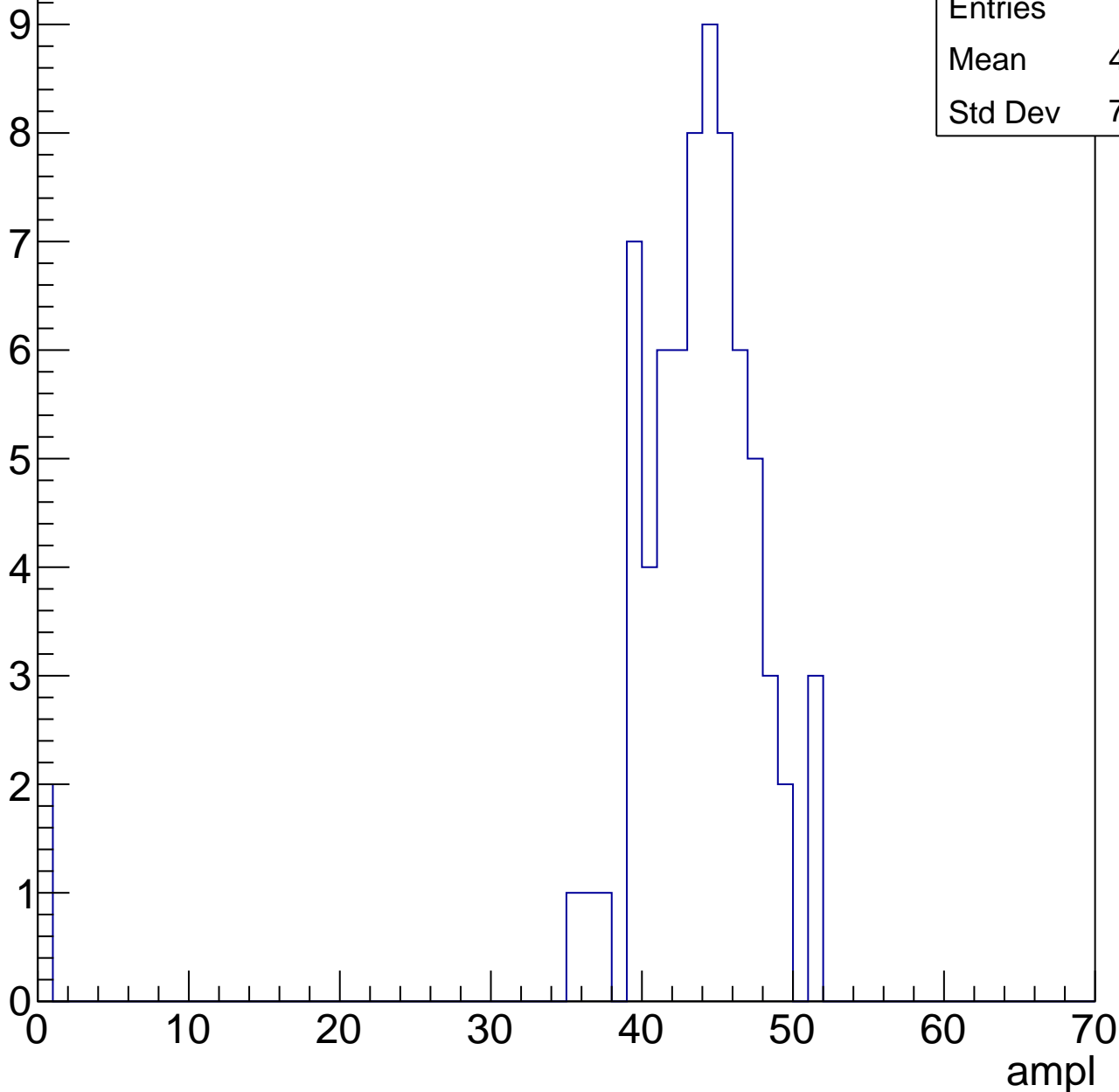
Entries	63
Mean	35.32
Std Dev	9.777



# B1L103S, U25-ch23, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

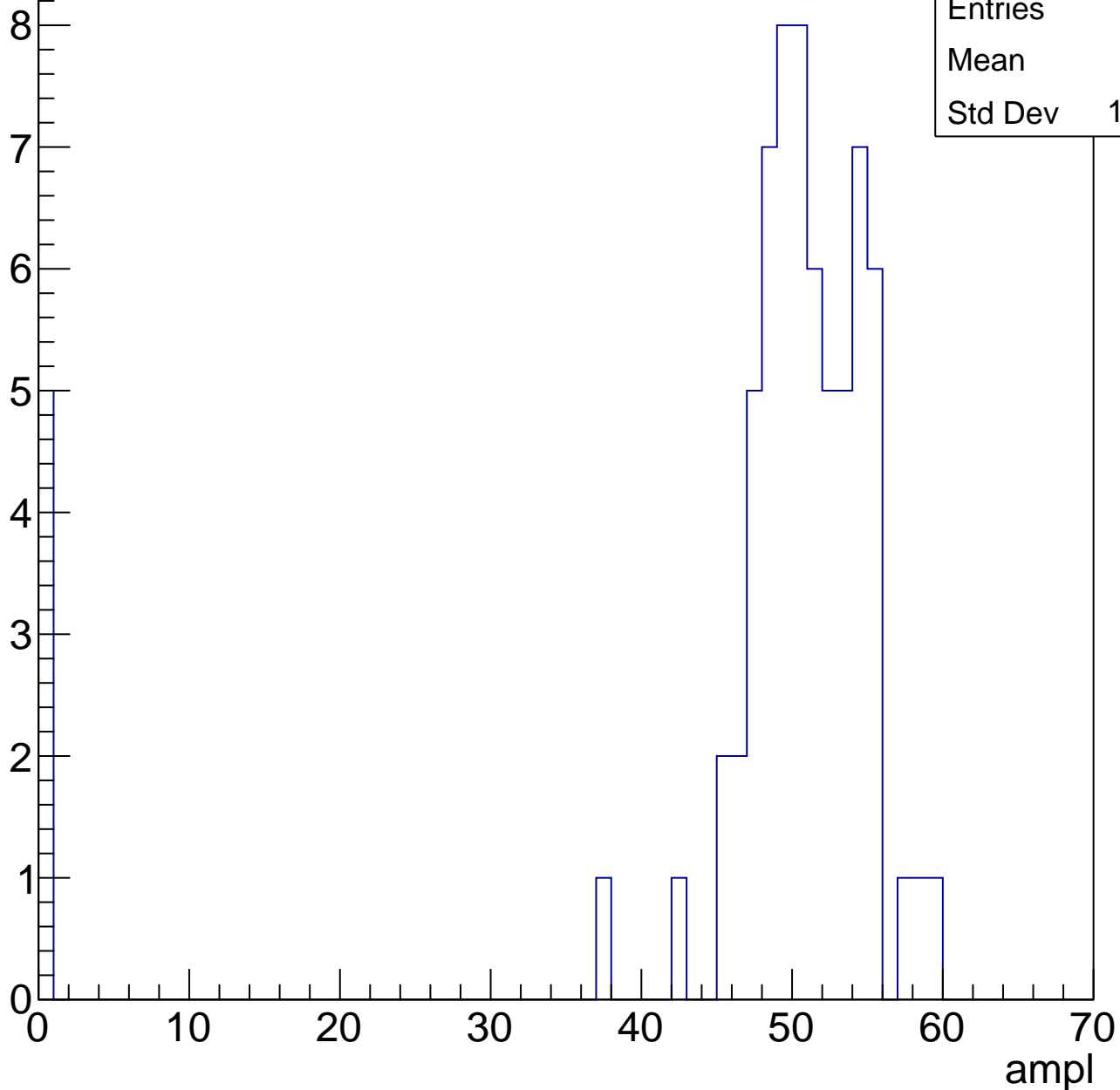


# B1L103S, U25-ch23, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

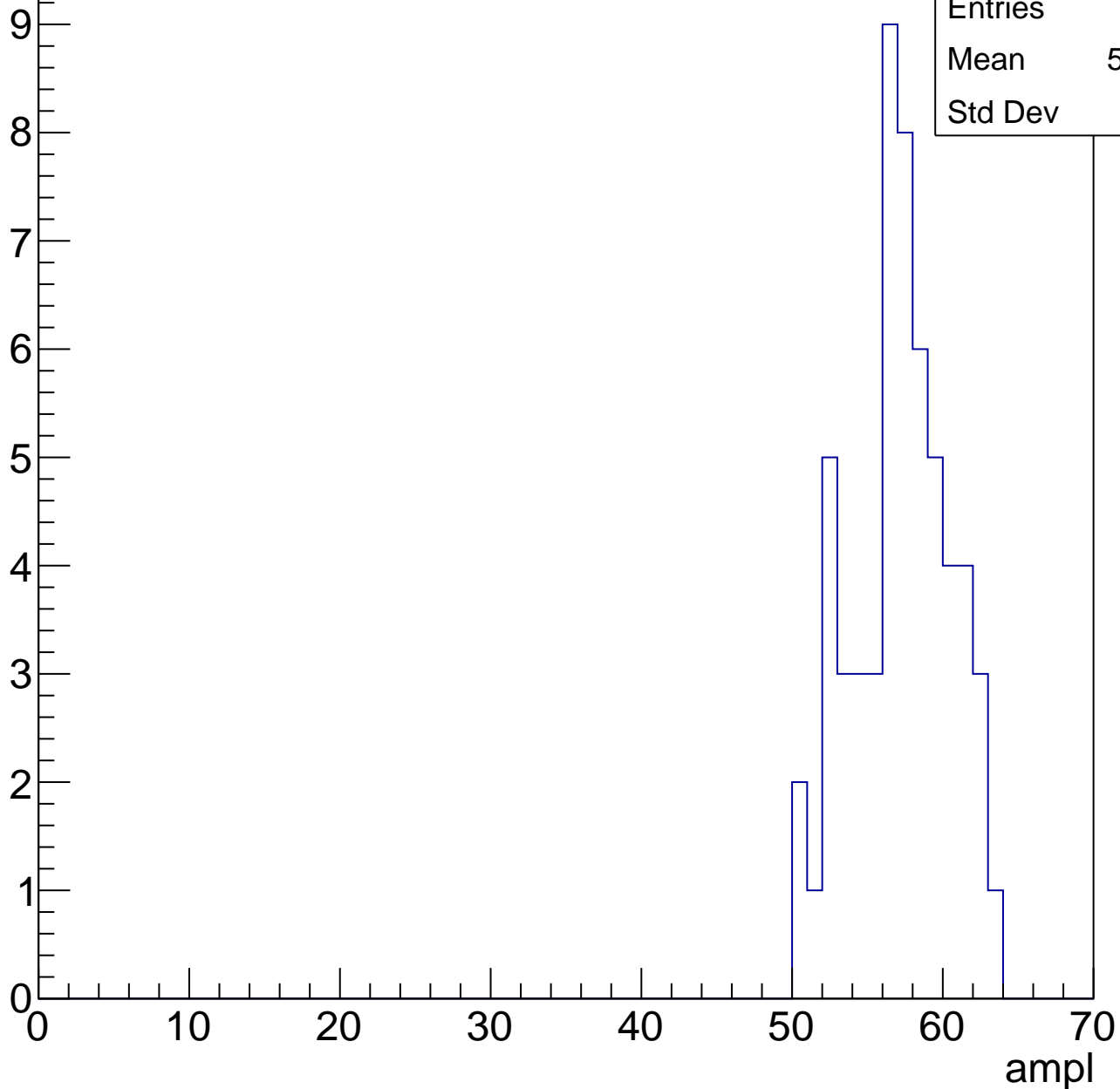
Entries	71
Mean	47
Std Dev	13.42



# B1L103S, U25-ch23, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

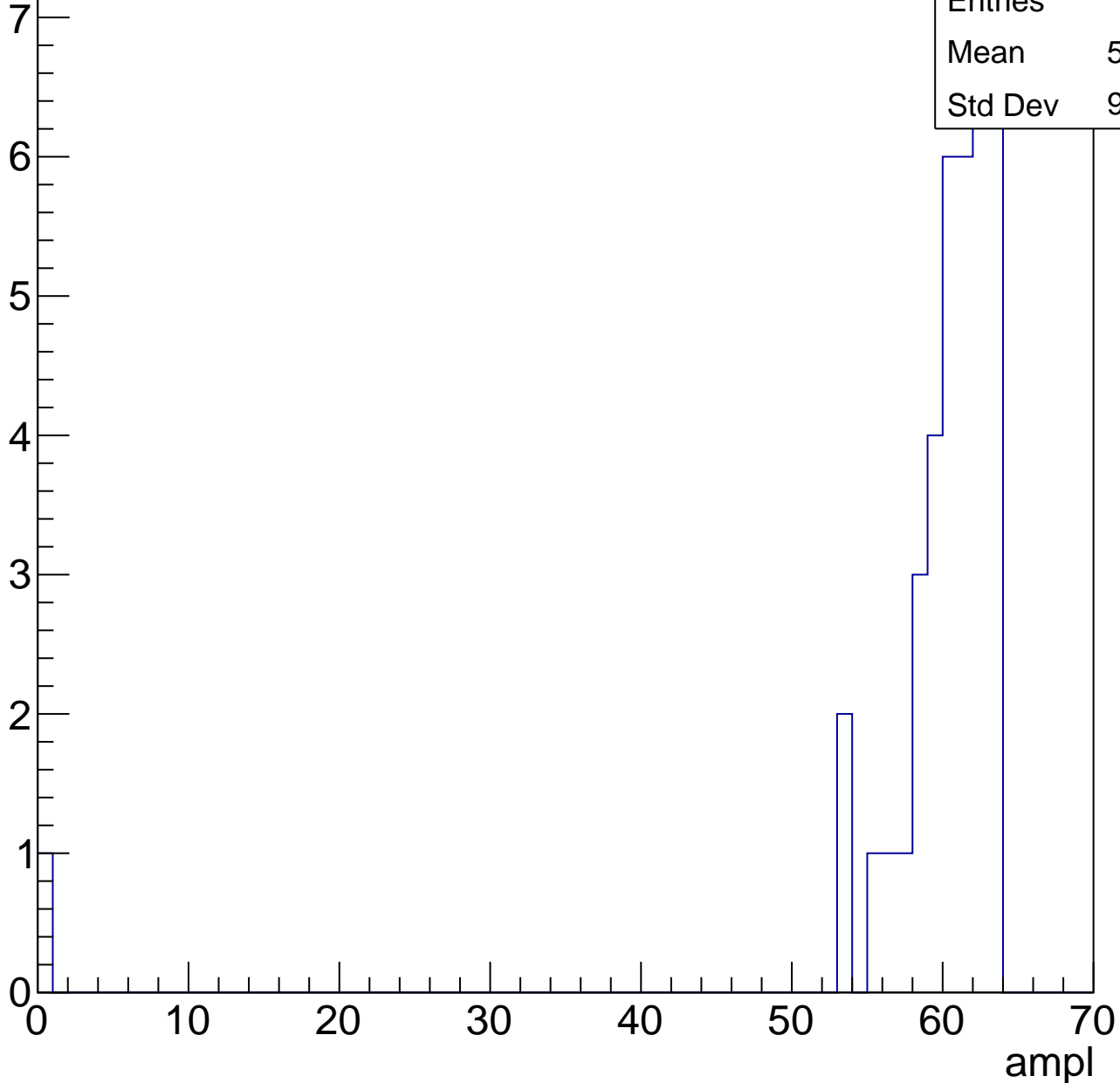


# B1L103S, U25-ch23, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	39
Mean	58.59
Std Dev	9.849



# B1L103S, U25-ch23, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U25-ch23, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

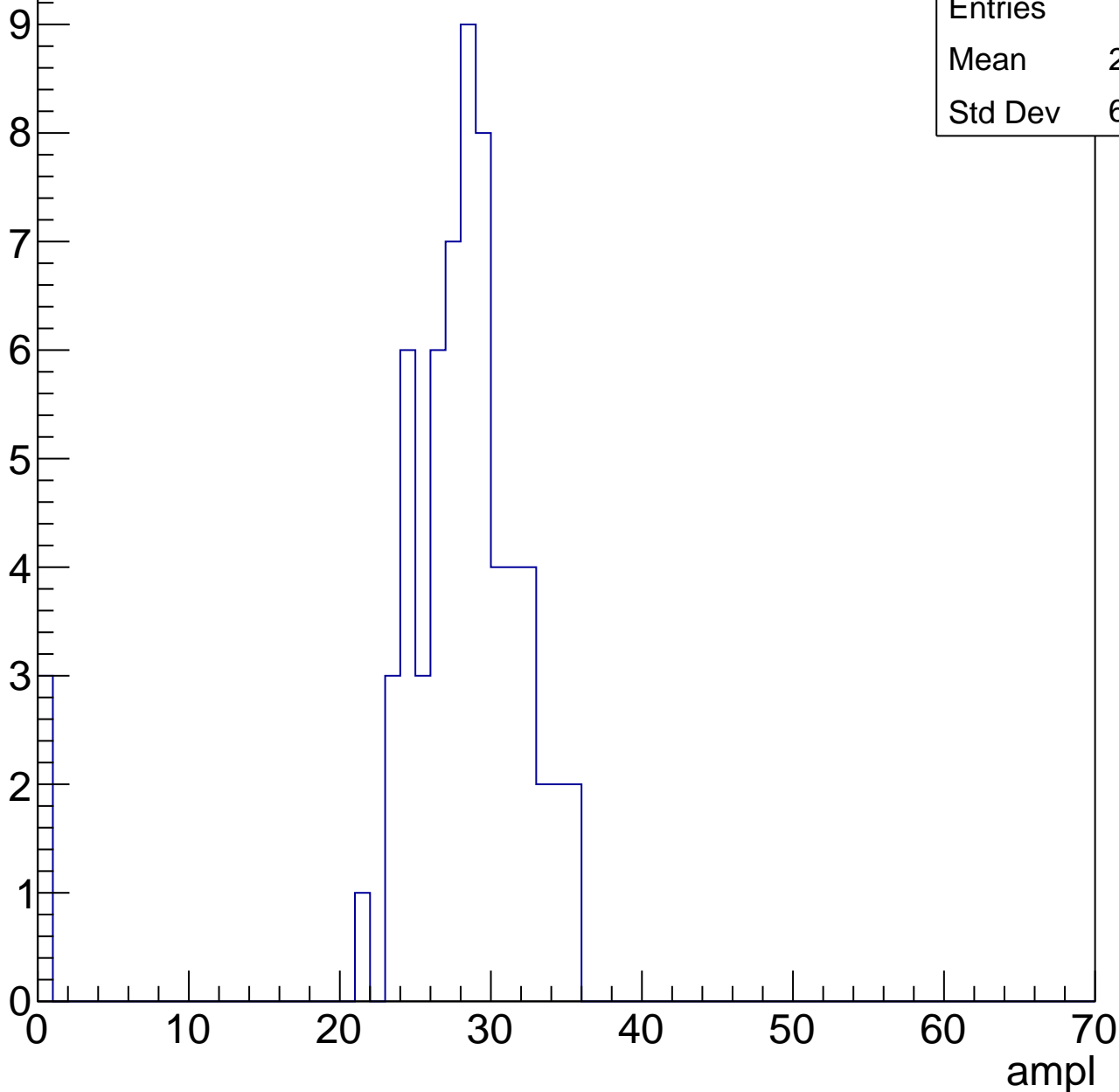


# B1L103S, U25-ch24, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

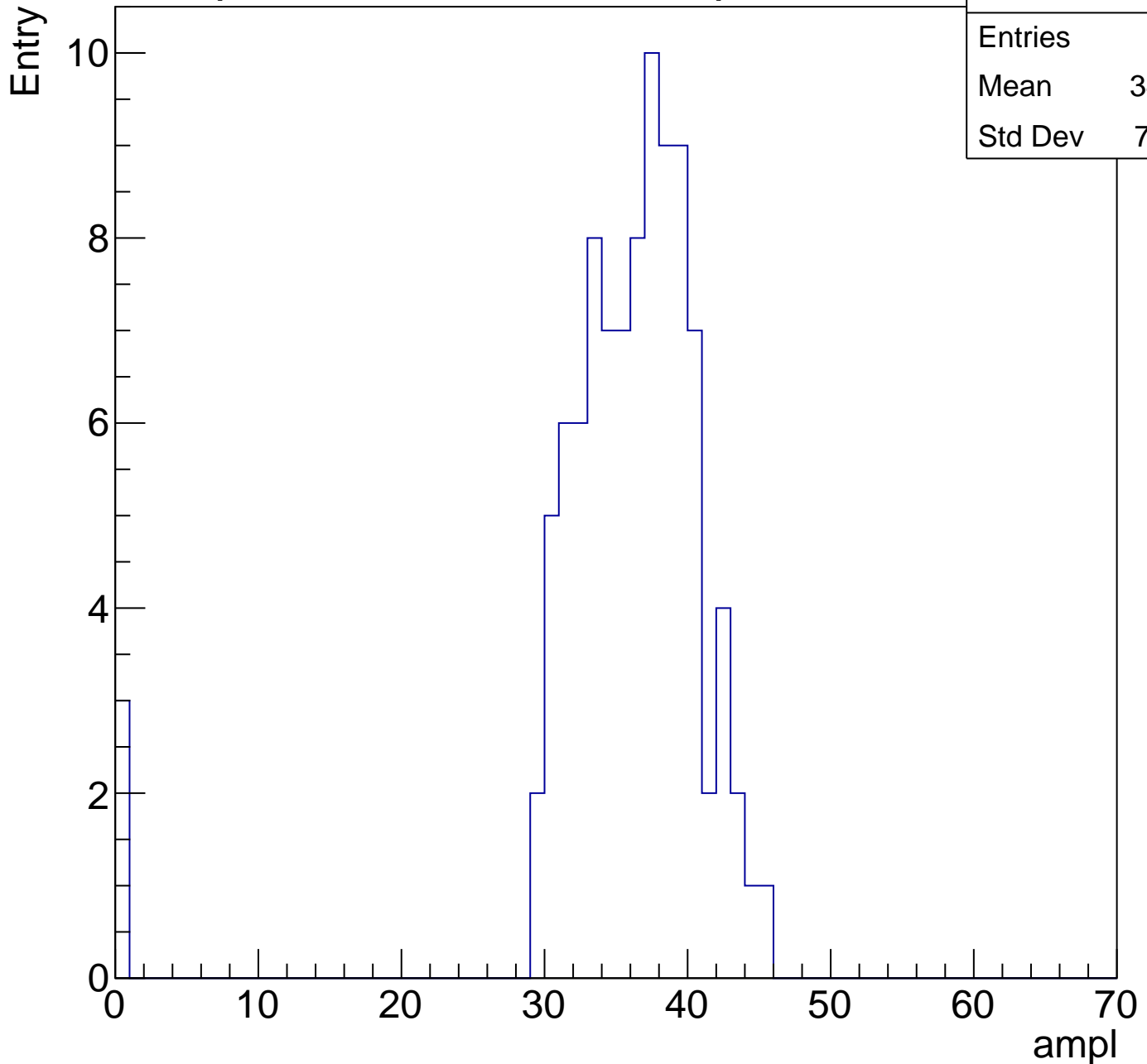
Entries	64
Mean	26.78
Std Dev	6.707



# B1L103S, U25-ch24, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	97
Mean	34.94
Std Dev	7.241

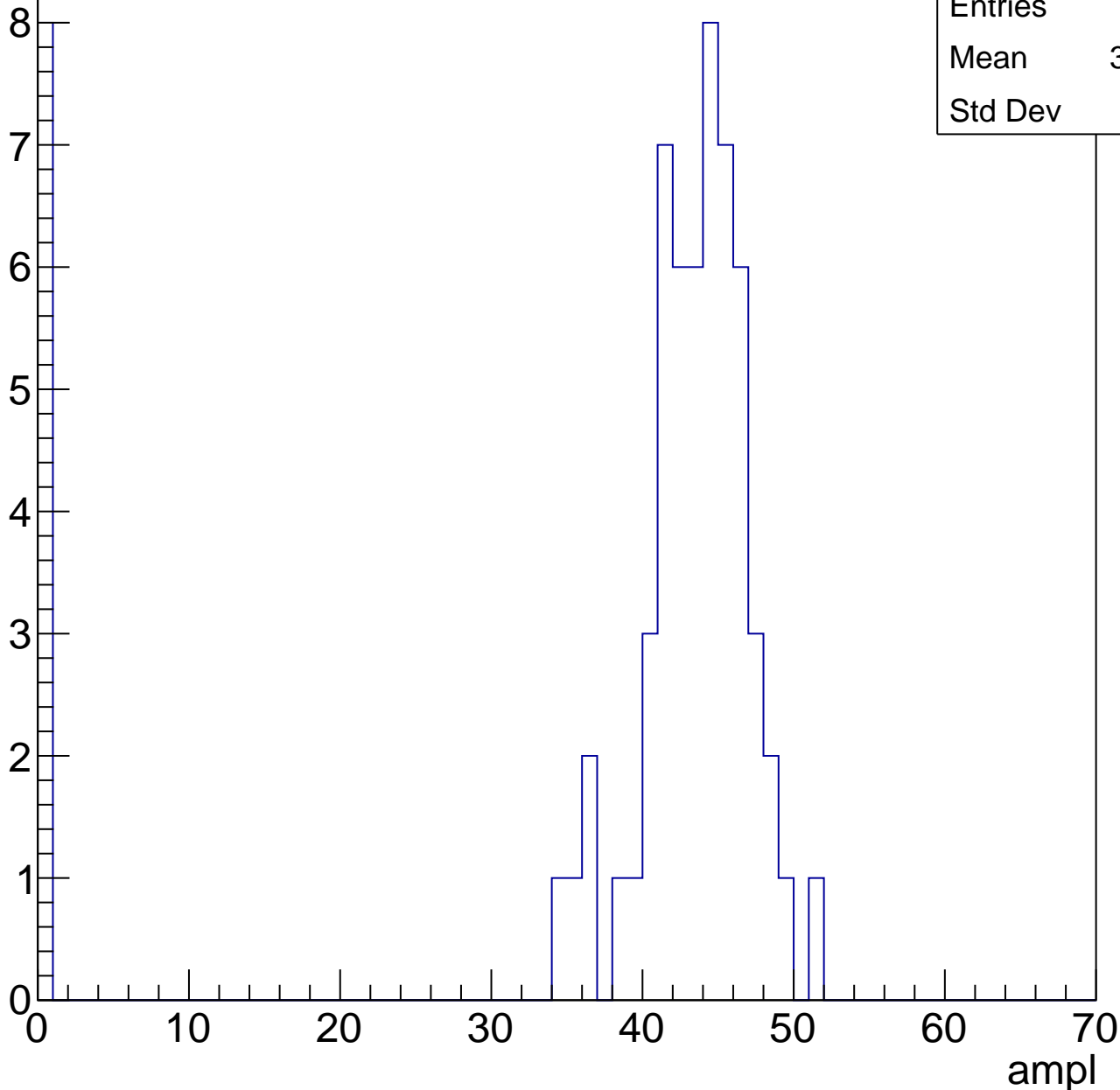


# B1L103S, U25-ch24, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	64
Mean	37.73
Std Dev	14.6

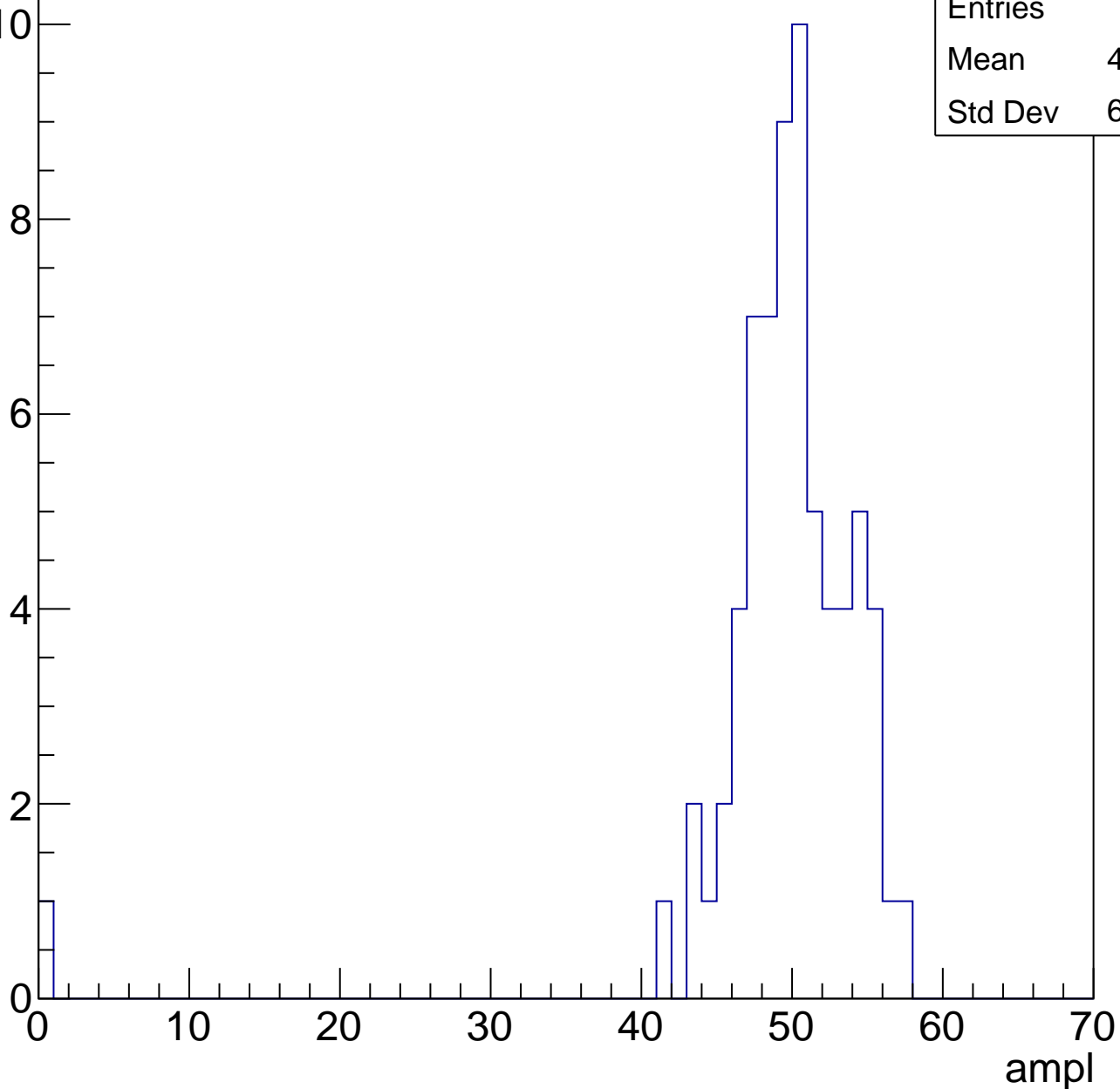


# B1L103S, U25-ch24, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	68
Mean	48.96
Std Dev	6.835

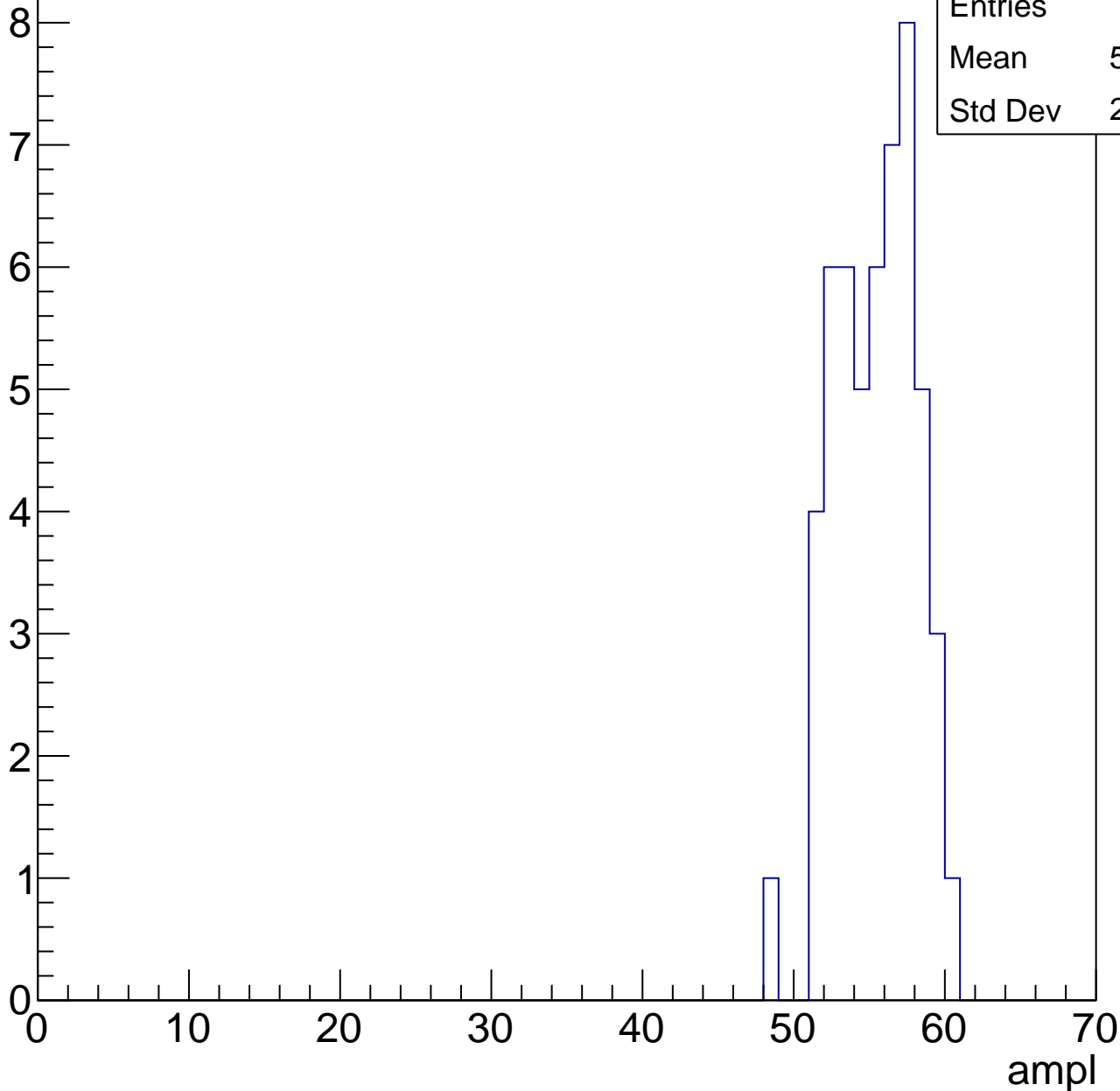


# B1L103S, U25-ch24, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	52
Mean	54.94
Std Dev	2.605

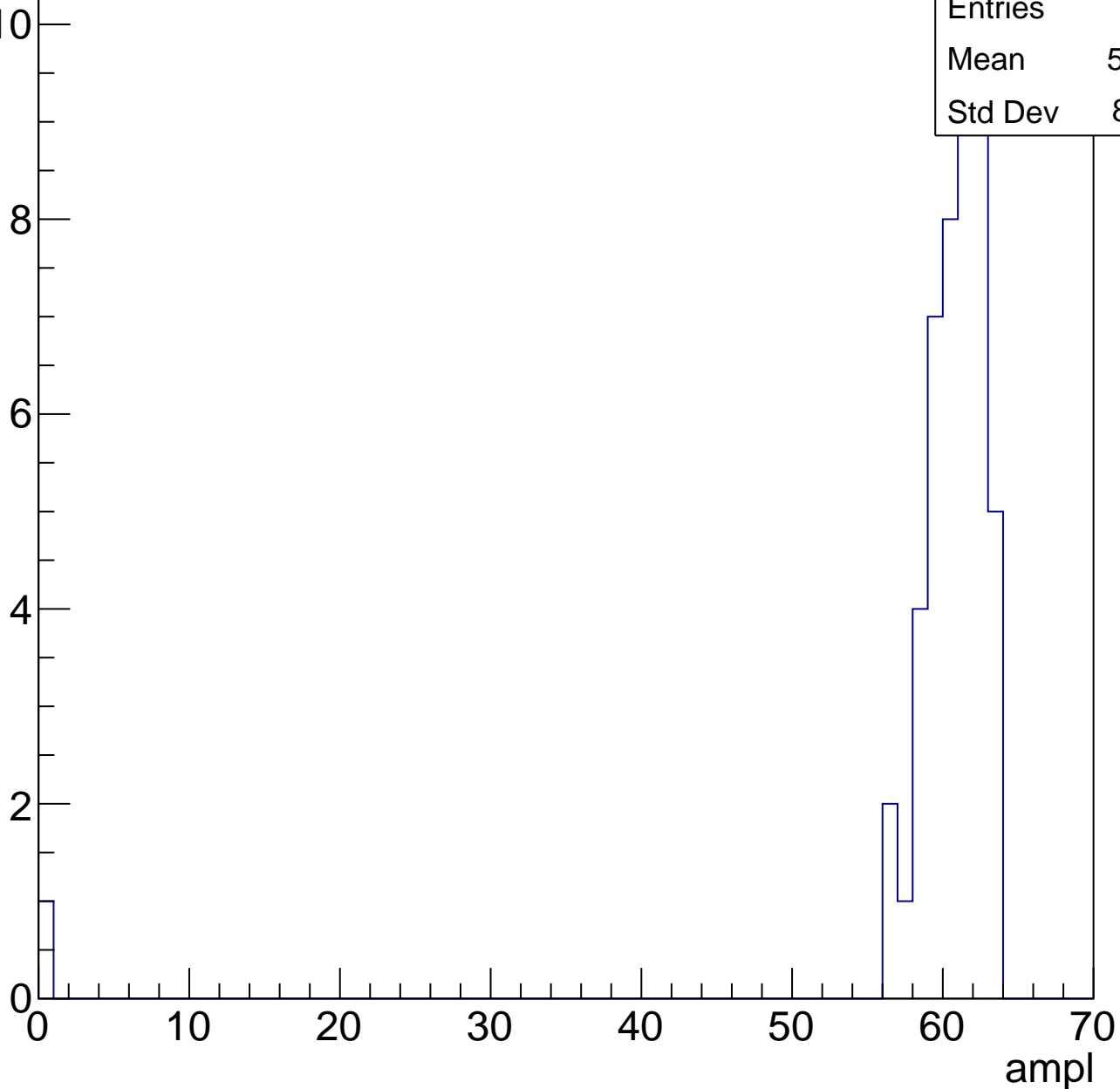


# B1L103S, U25-ch24, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	47
Mean	59.09
Std Dev	8.891

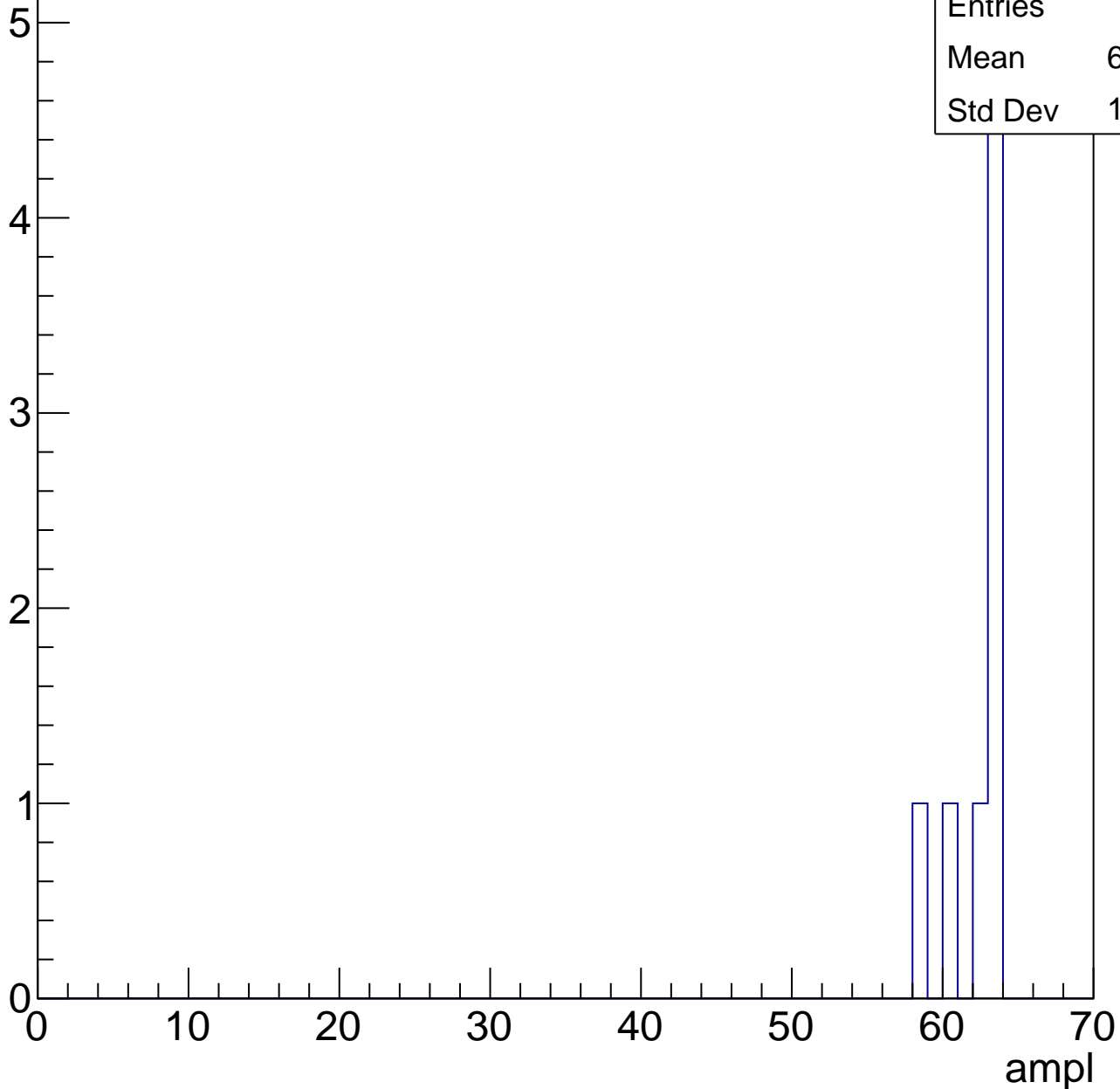


# B1L103S, U25-ch24, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	8
Mean	61.88
Std Dev	1.763





# B1L103S, U25-ch24, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

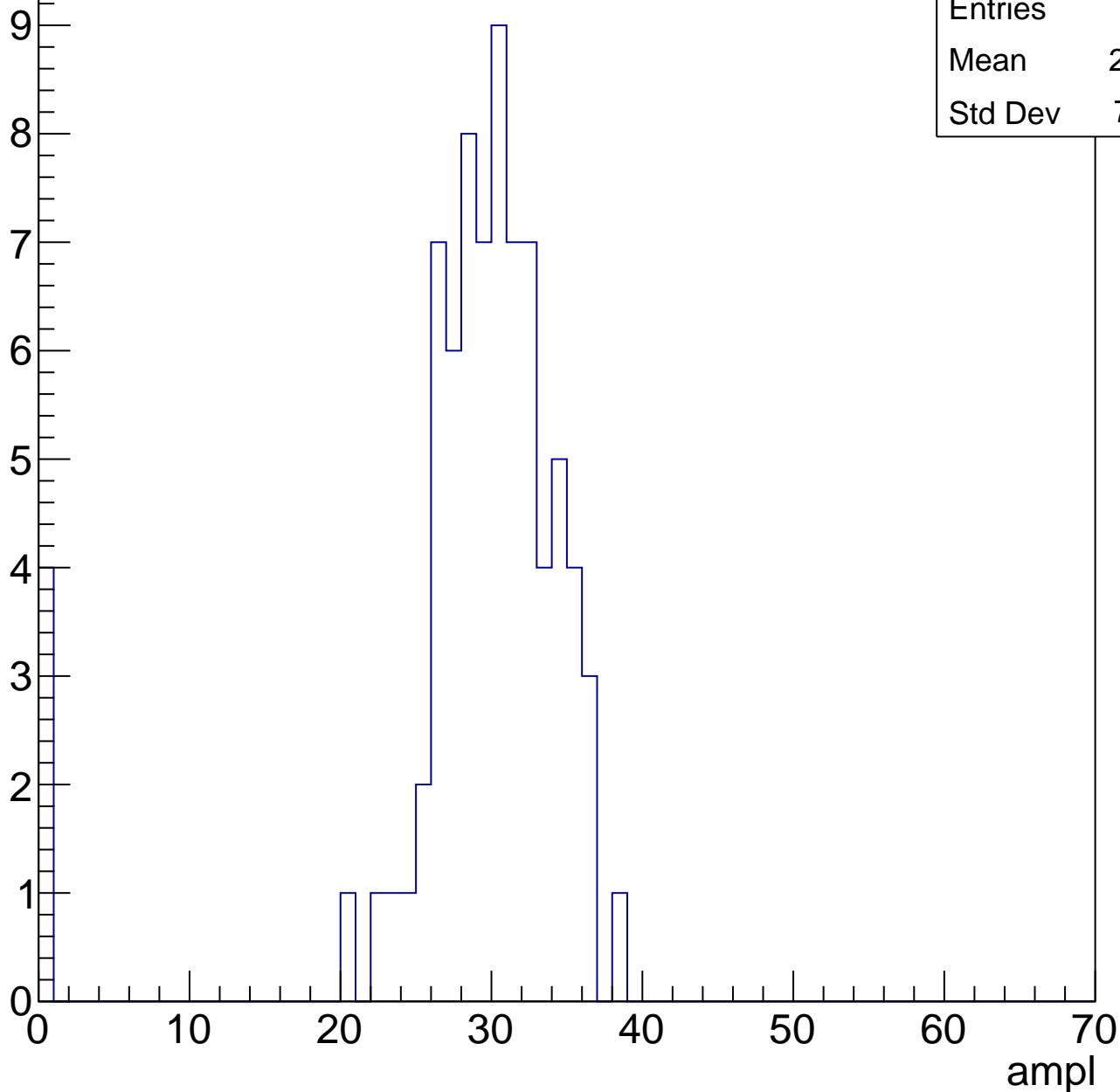


# B1L103S, U25-ch25, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	78
Mean	28.32
Std Dev	7.431

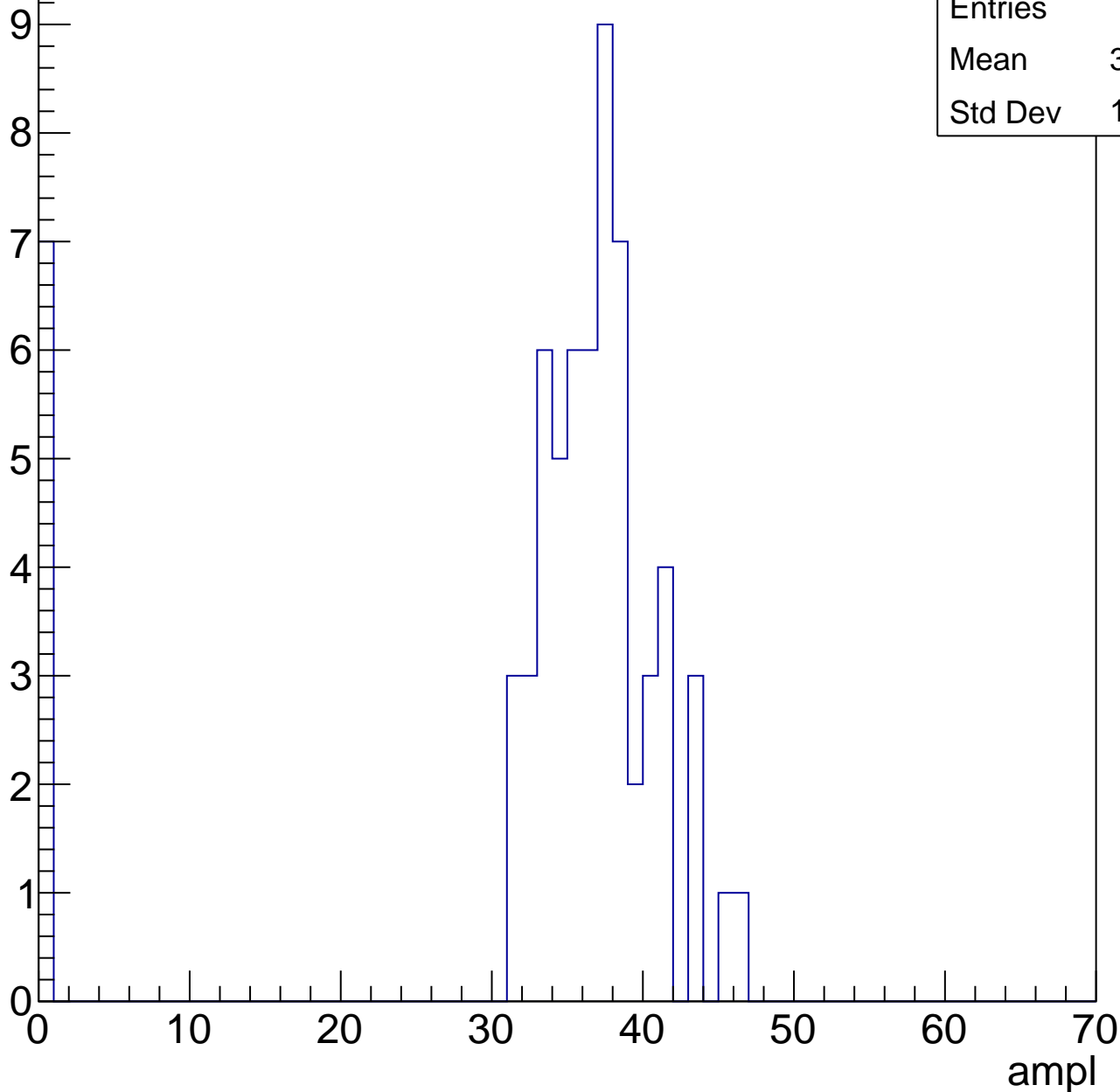


# B1L103S, U25-ch25, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	66
Mean	32.79
Std Dev	11.76



# B1L103S, U25-ch25, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	70
Mean	40.09
Std Dev	10.29

Entry

10

8

6

4

2

0

0

10

20

30

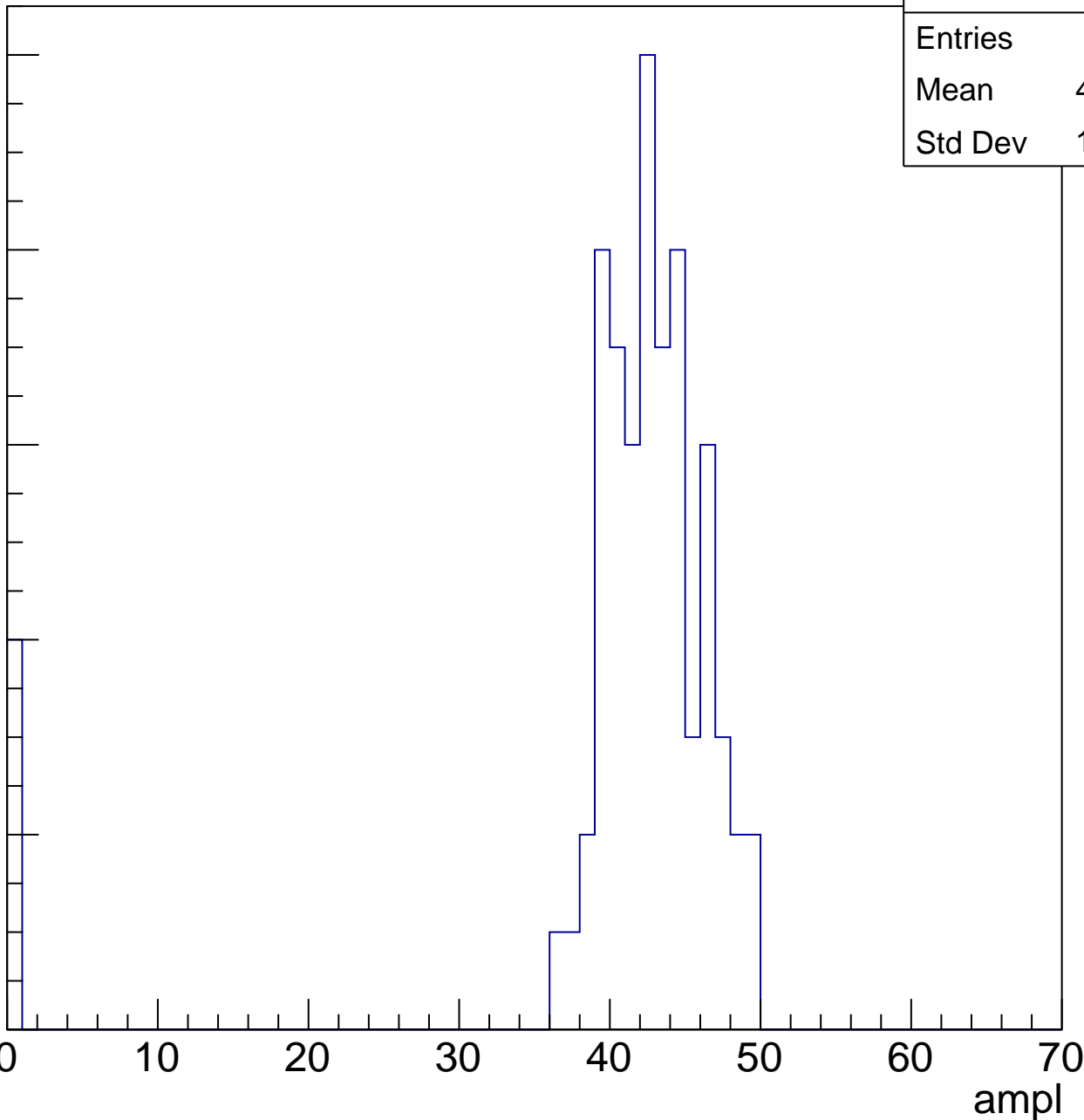
40

50

60

70

ampl

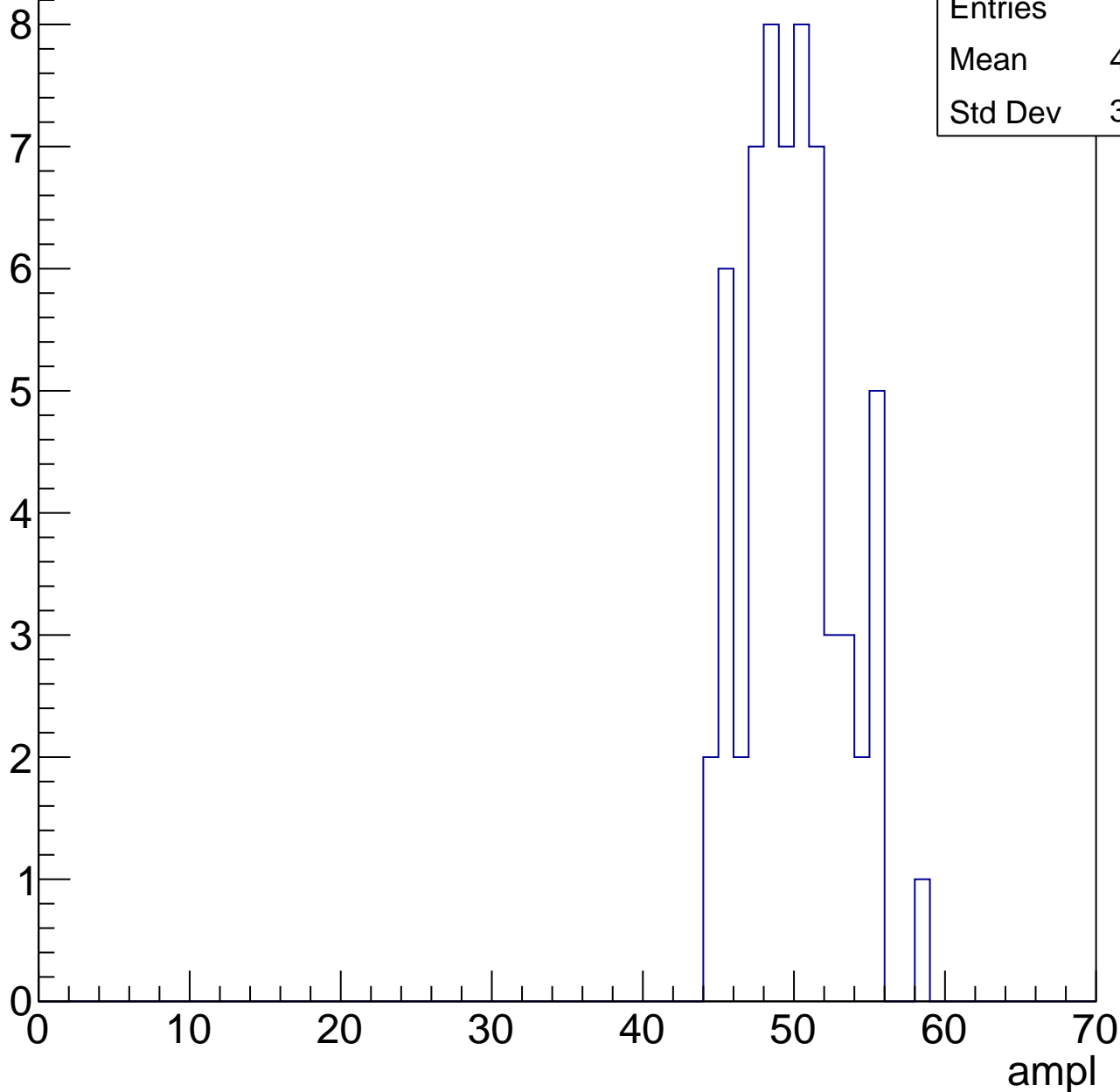


# B1L103S, U25-ch25, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	61
Mean	49.49
Std Dev	3.155



# B1L103S, U25-ch25, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	67
Mean	55.31
Std Dev	3.293

Entry

10

8

6

4

2

0

0

10

20

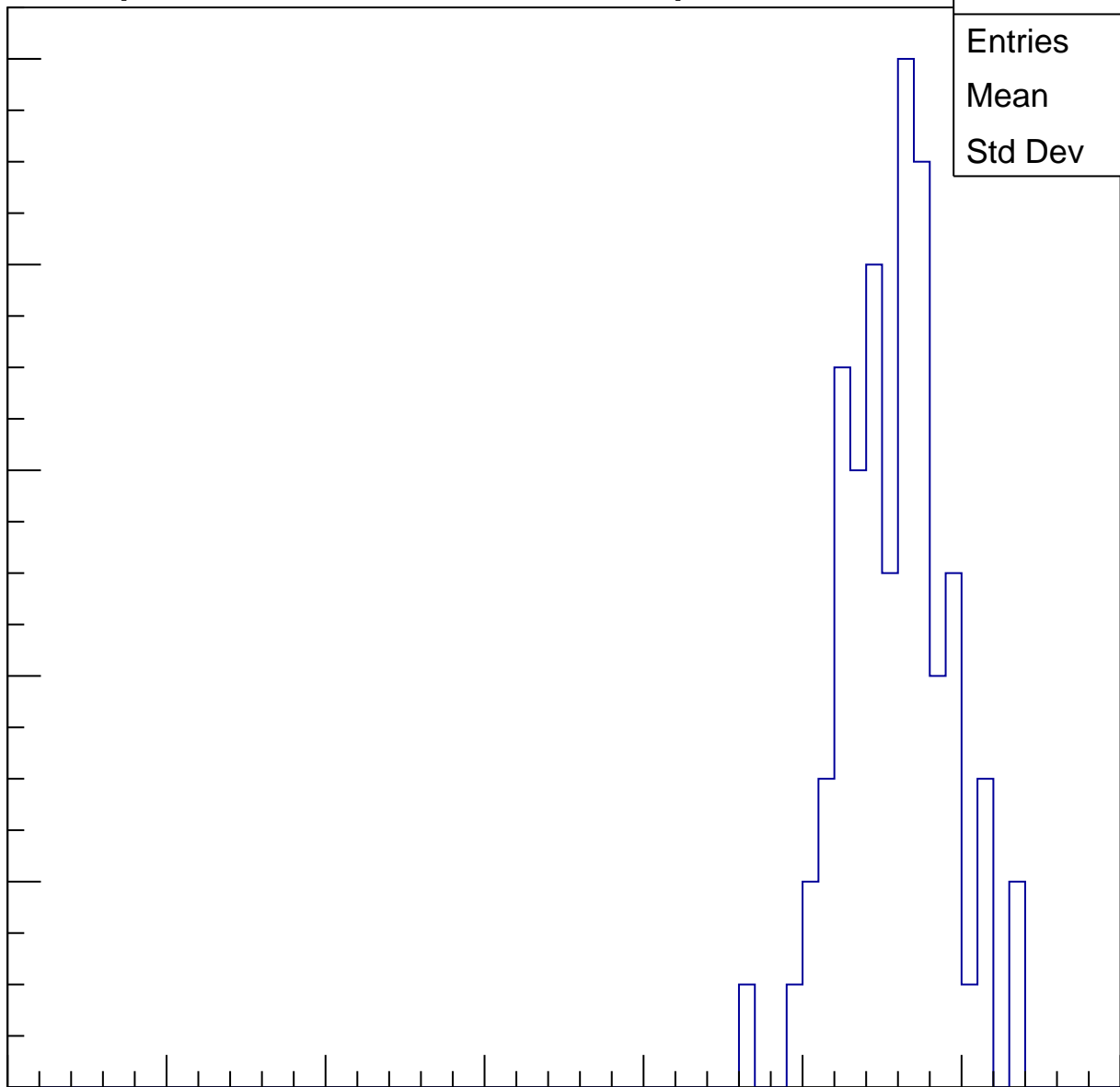
30

40

50

60

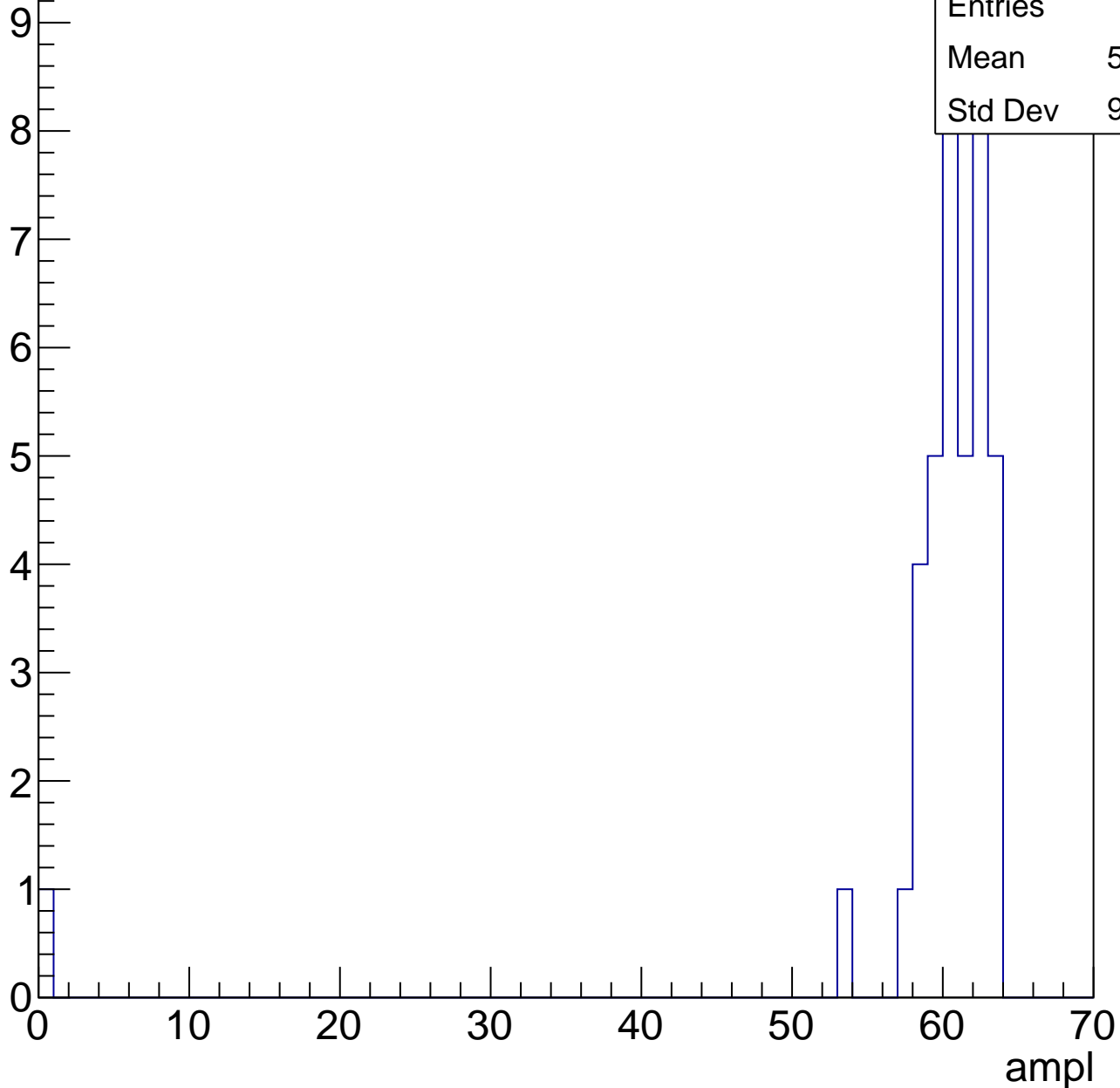
ampl



# B1L103S, U25-ch25, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

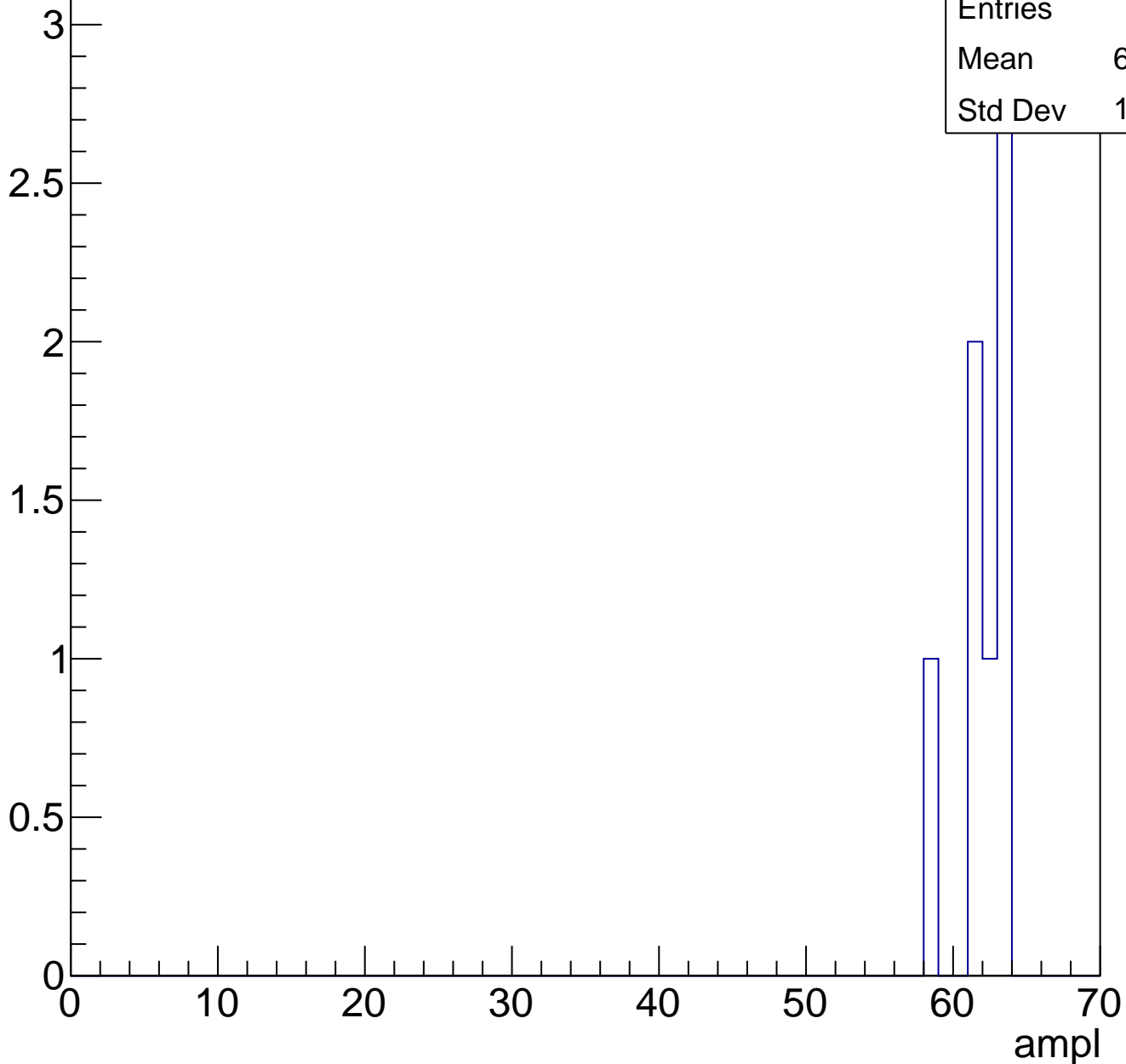
Entry



# B1L103S, U25-ch25, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



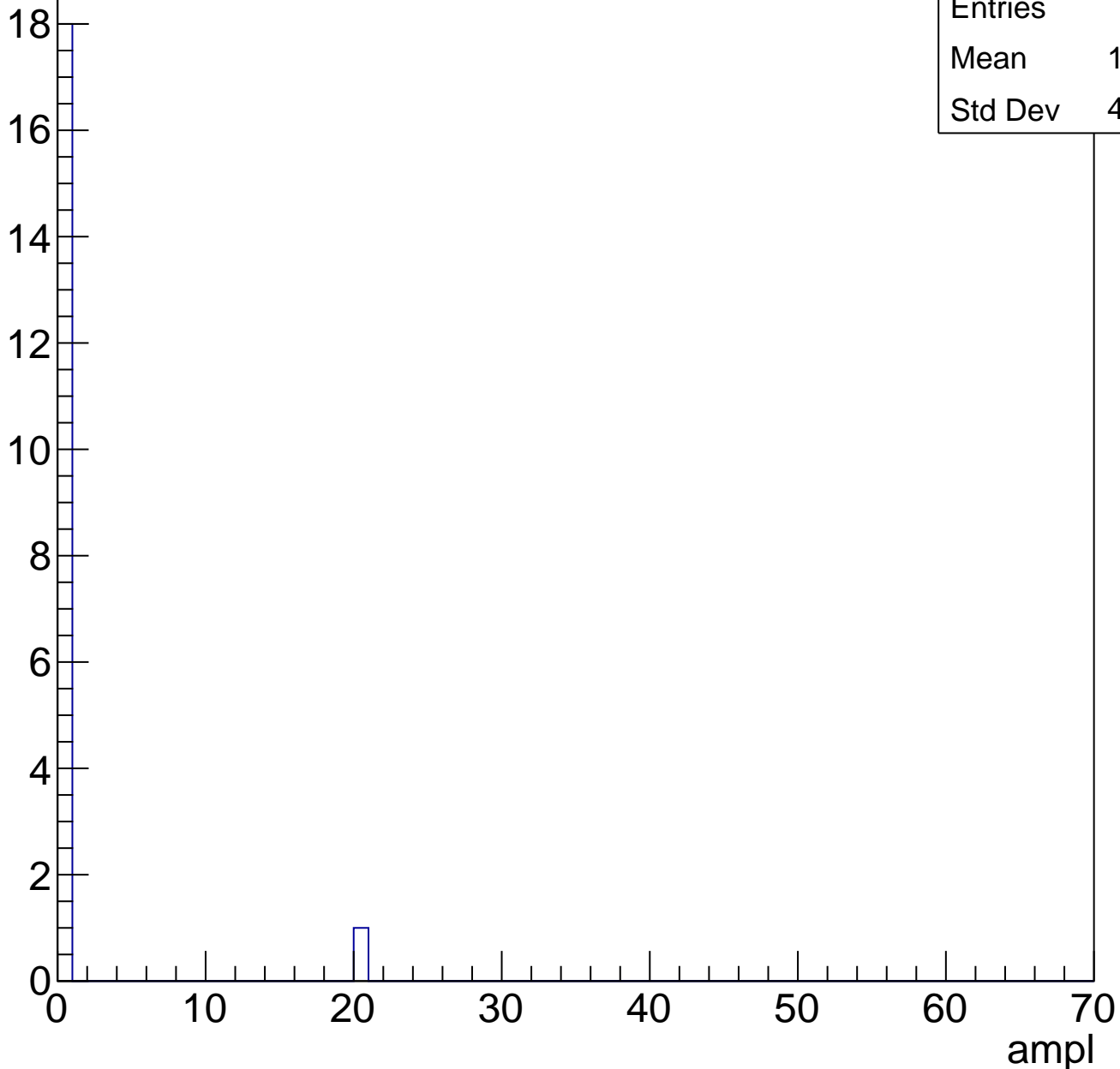


# B1L103S, U25-ch25, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	19
Mean	1.053
Std Dev	4.466

Entry

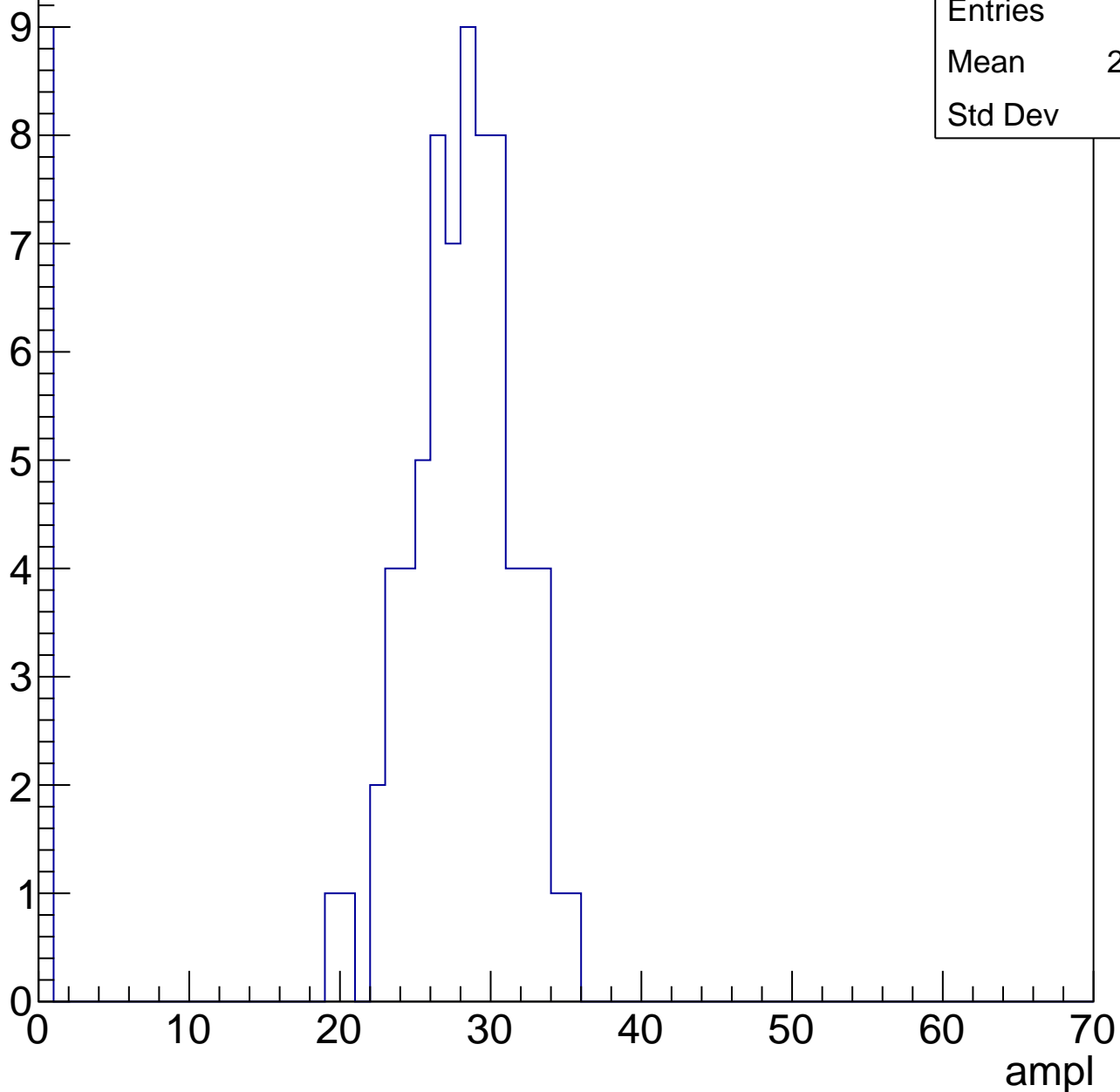


# B1L103S, U25-ch26, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	80
Mean	24.62
Std Dev	9.31

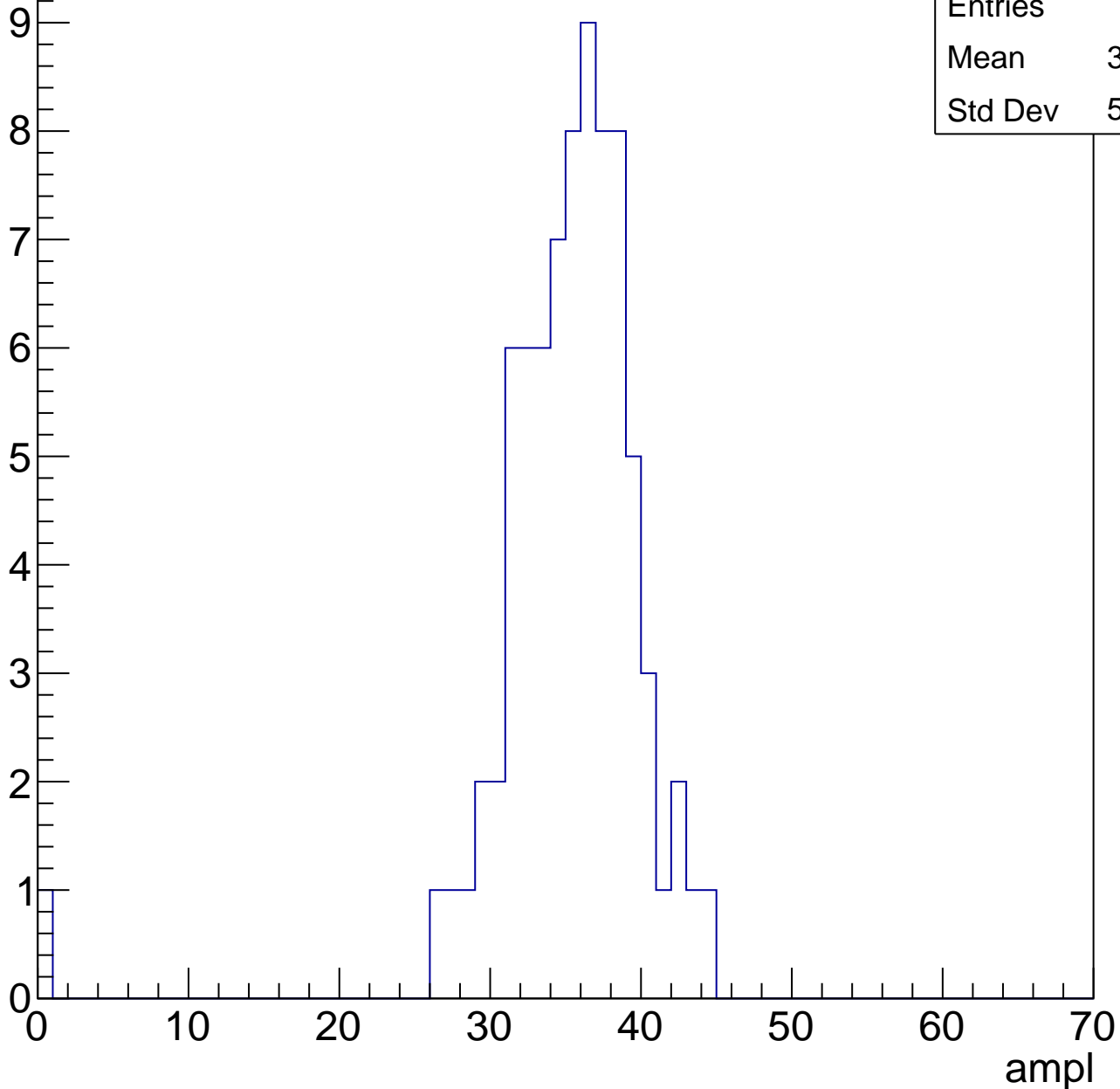


# B1L103S, U25-ch26, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

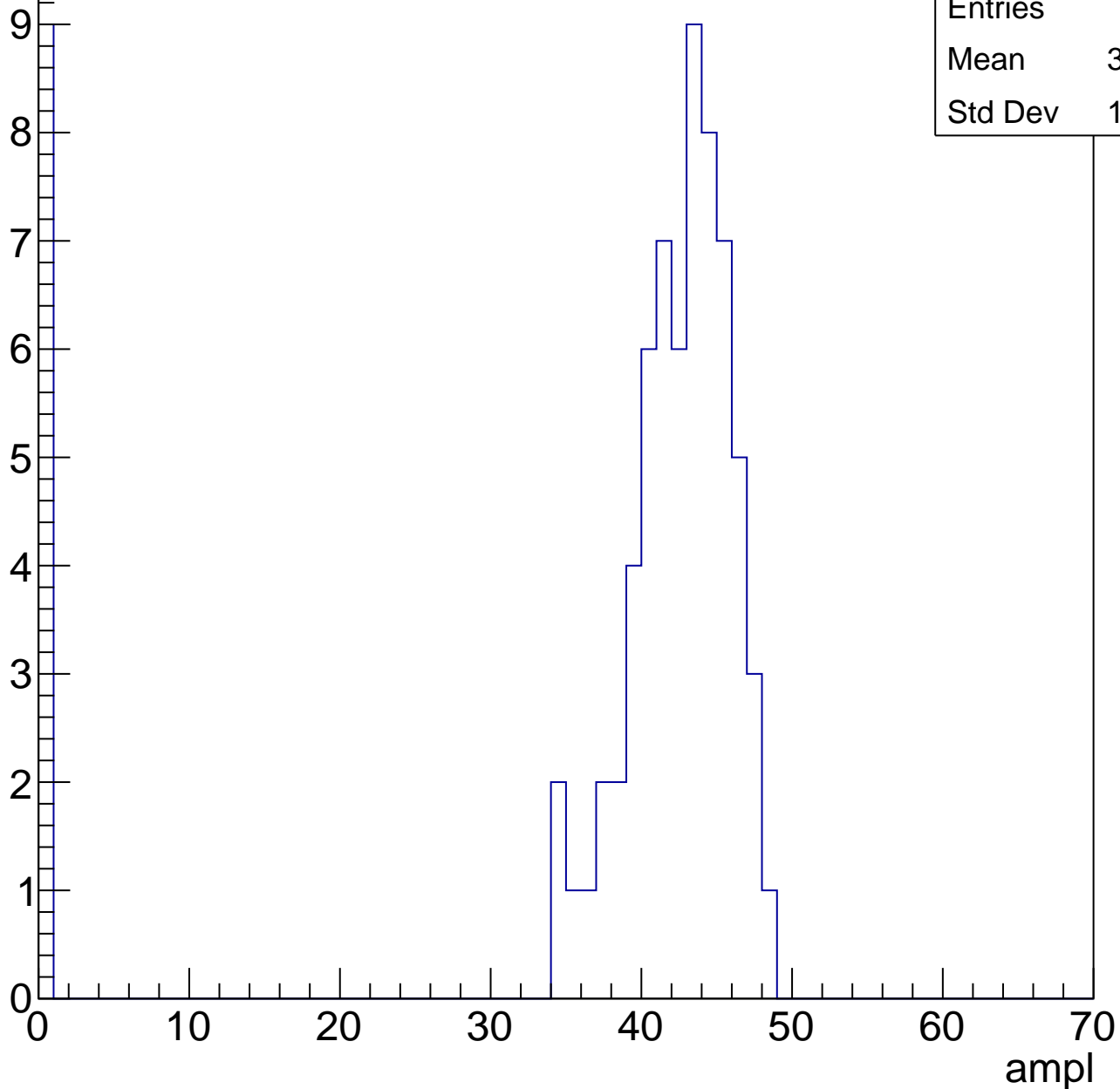
Entries	79
Mean	34.73
Std Dev	5.353



# B1L103S, U25-ch26, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



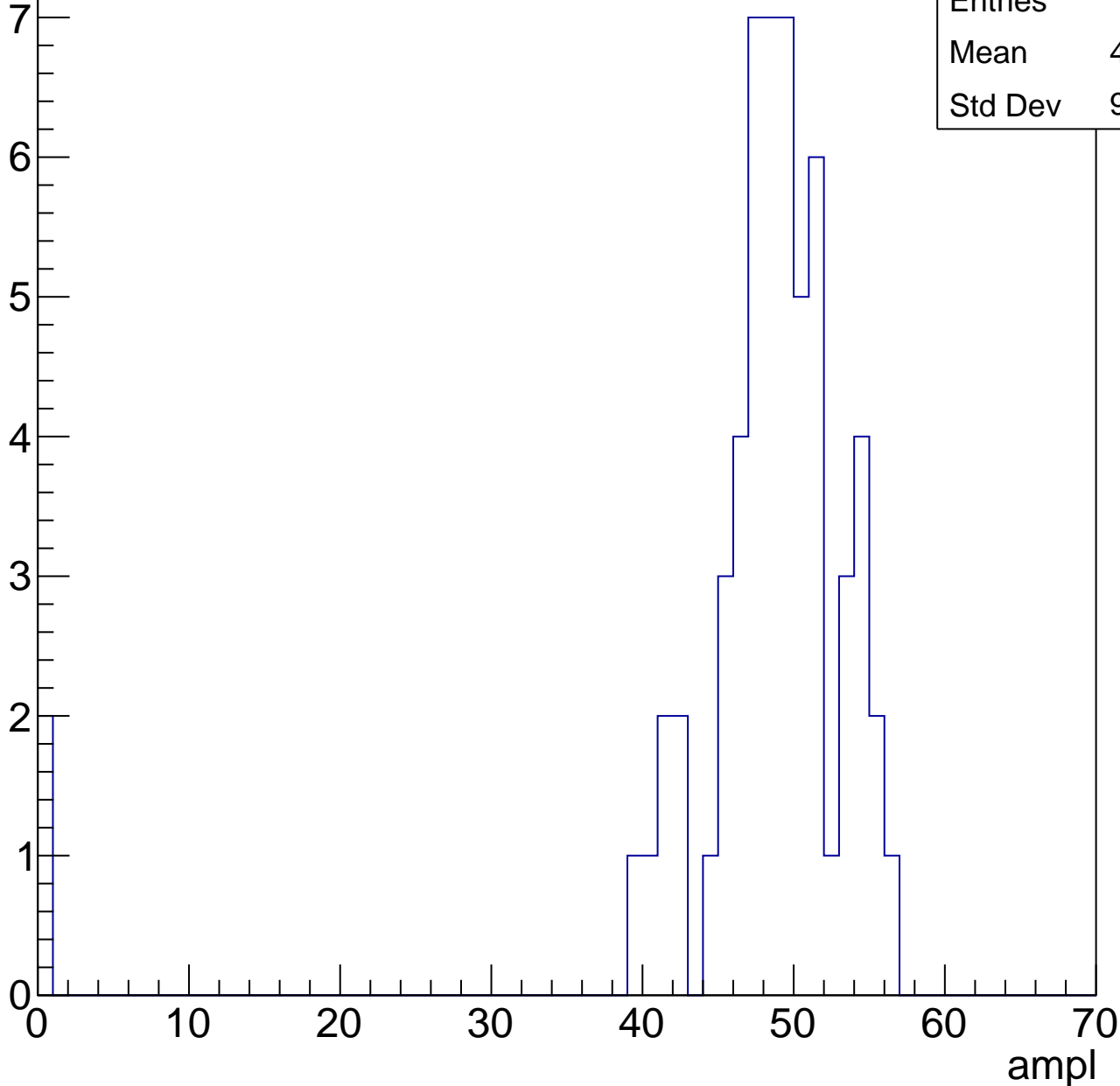
Entries	73
Mean	36.95
Std Dev	14.17

# B1L103S, U25-ch26, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	59
Mean	46.86
Std Dev	9.559

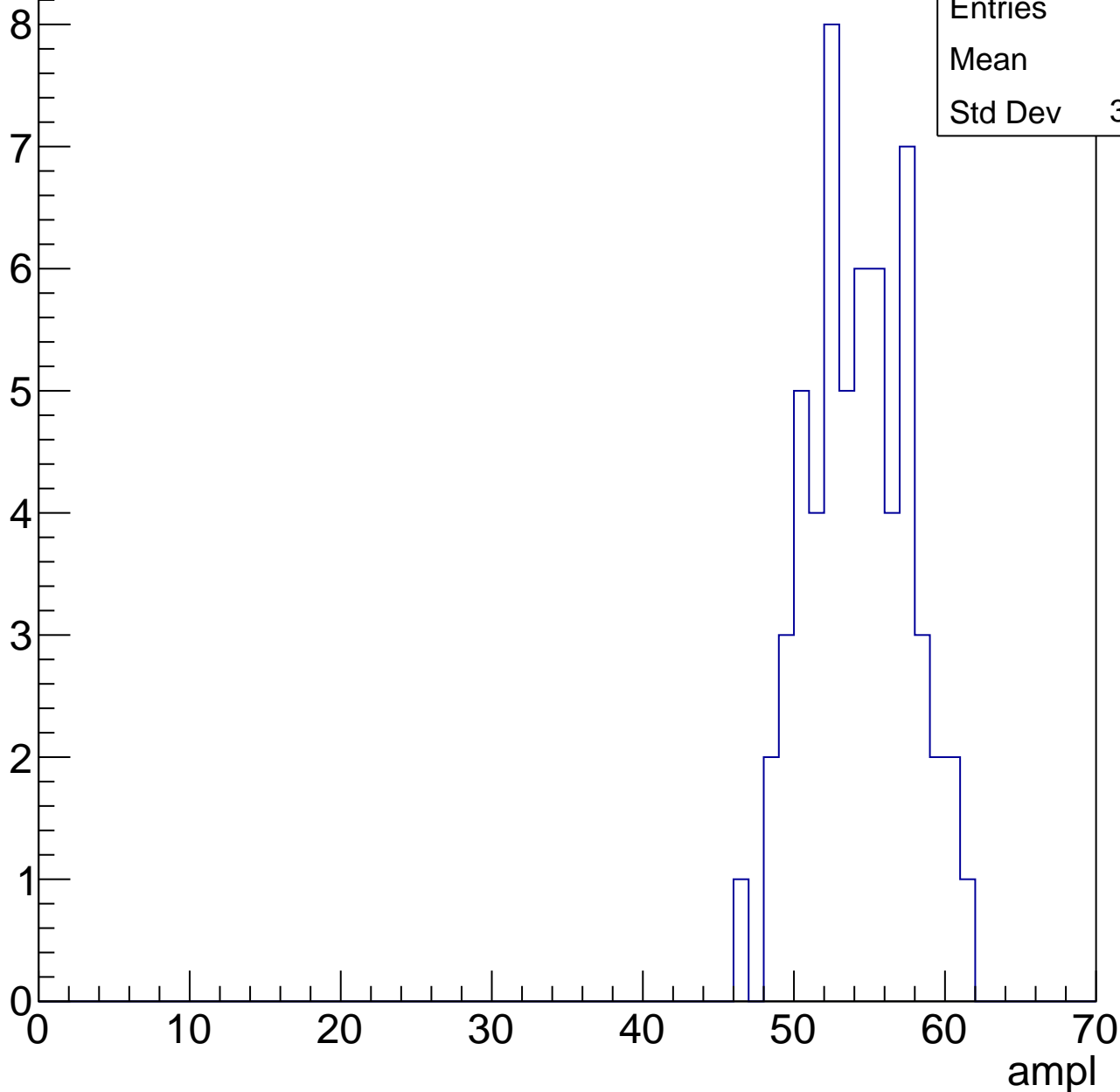


# B1L103S, U25-ch26, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	59
Mean	53.8
Std Dev	3.359

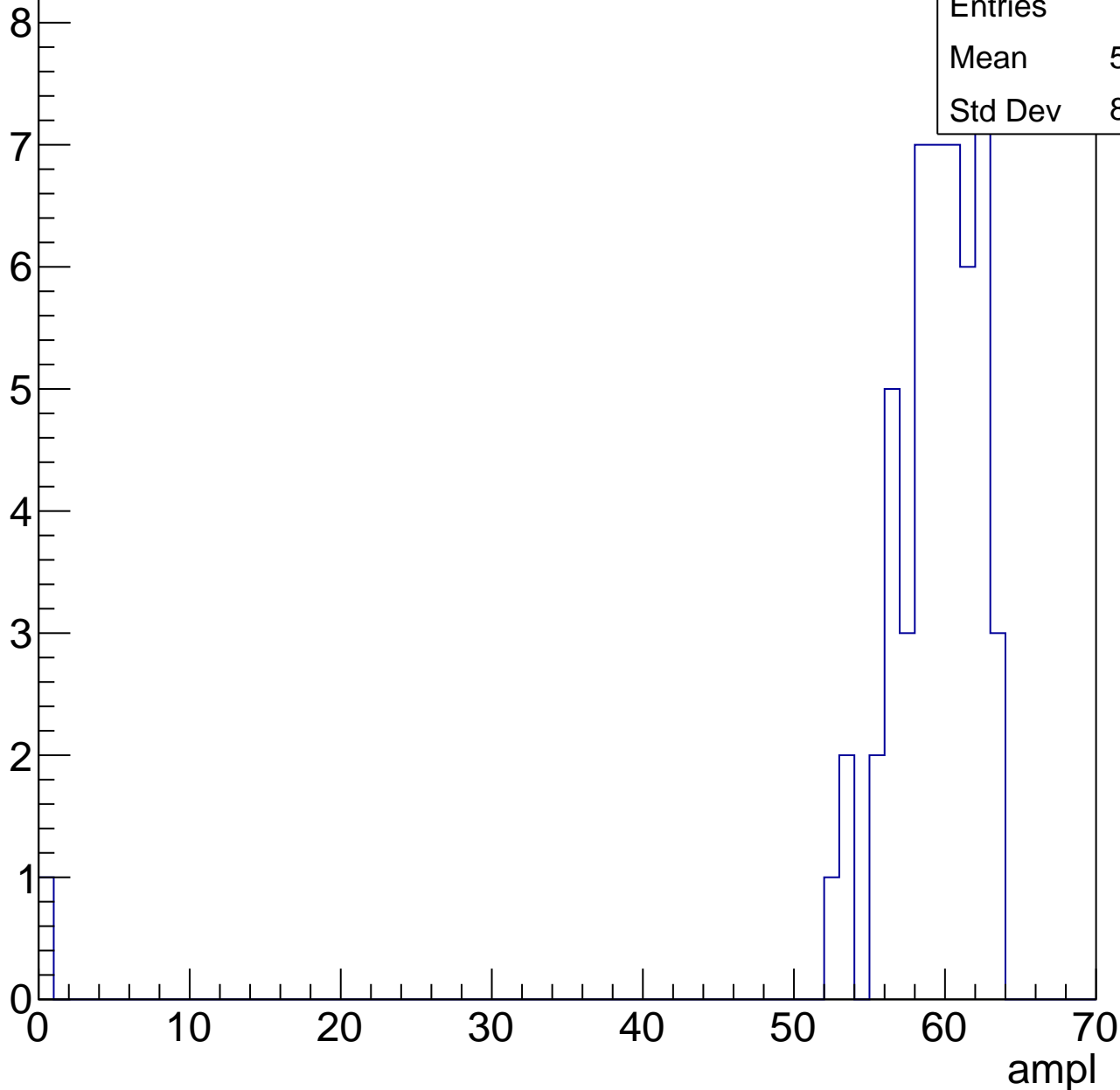


# B1L103S, U25-ch26, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	52
Mean	57.87
Std Dev	8.528

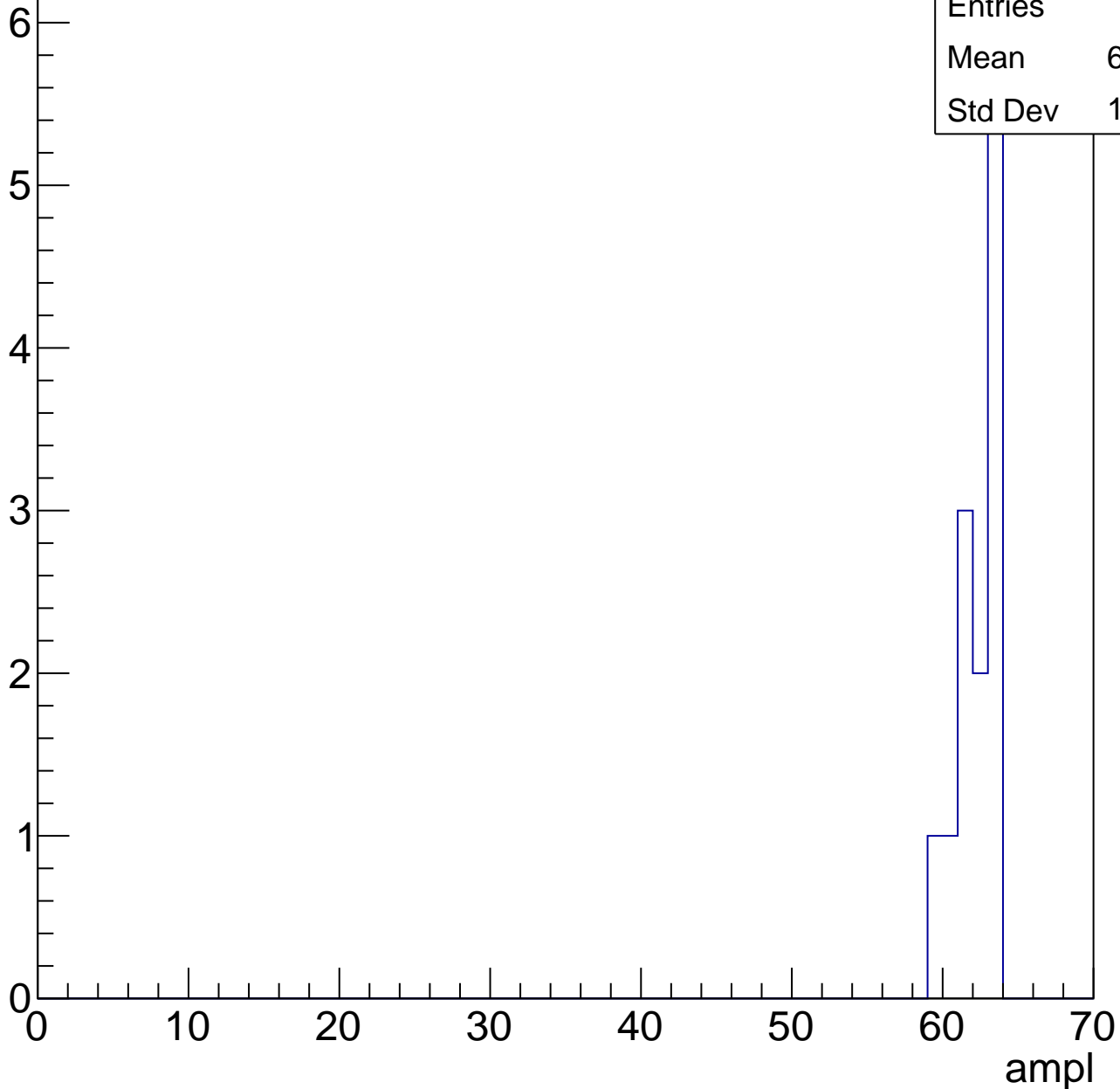


# B1L103S, U25-ch26, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	13
Mean	61.85
Std Dev	1.292





# B1L103S, U25-ch26, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	20
Mean	3.15
Std Dev	13.73

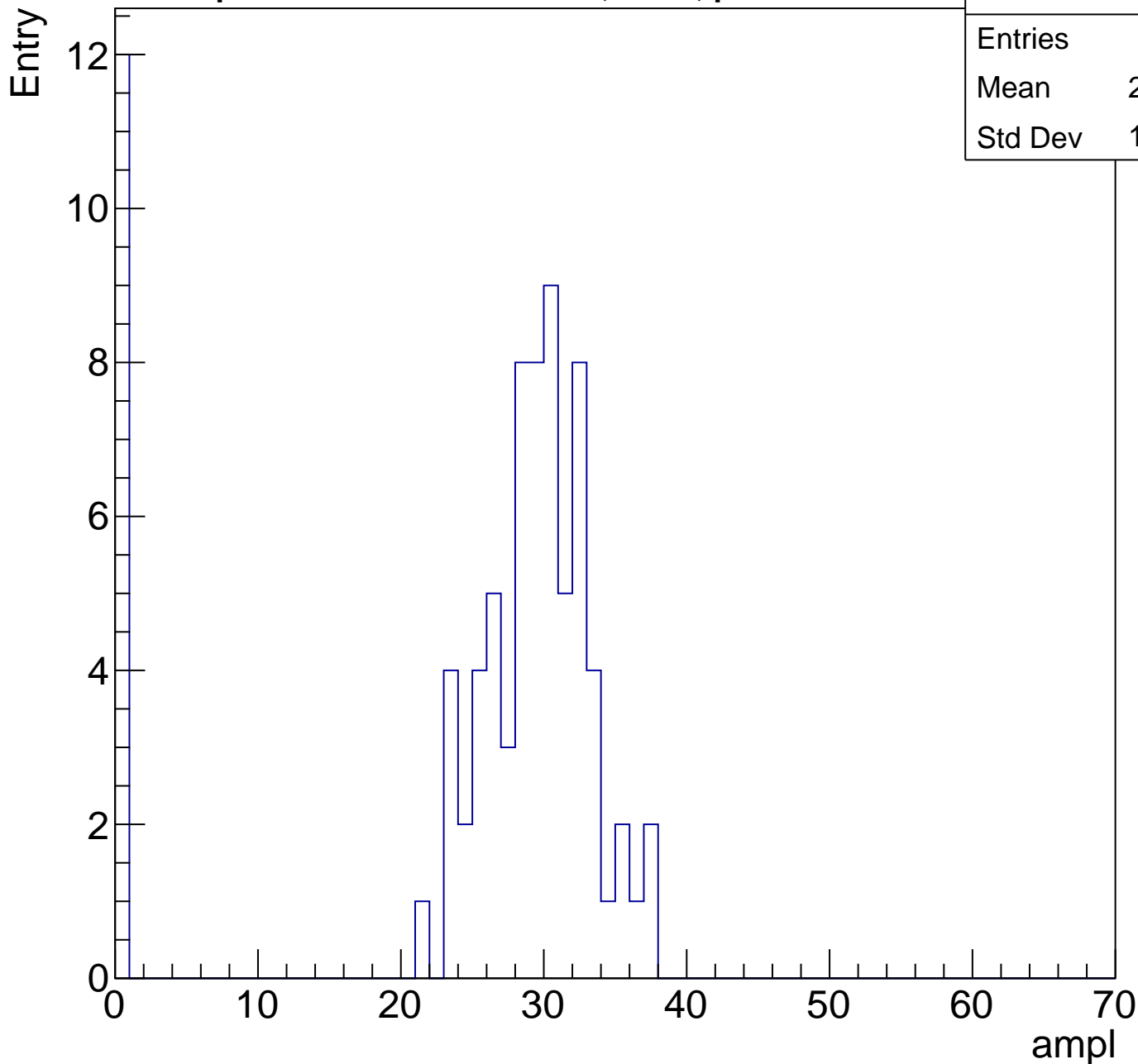
Entry



# B1L103S, U25-ch27, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	79
Mean	24.75
Std Dev	10.96

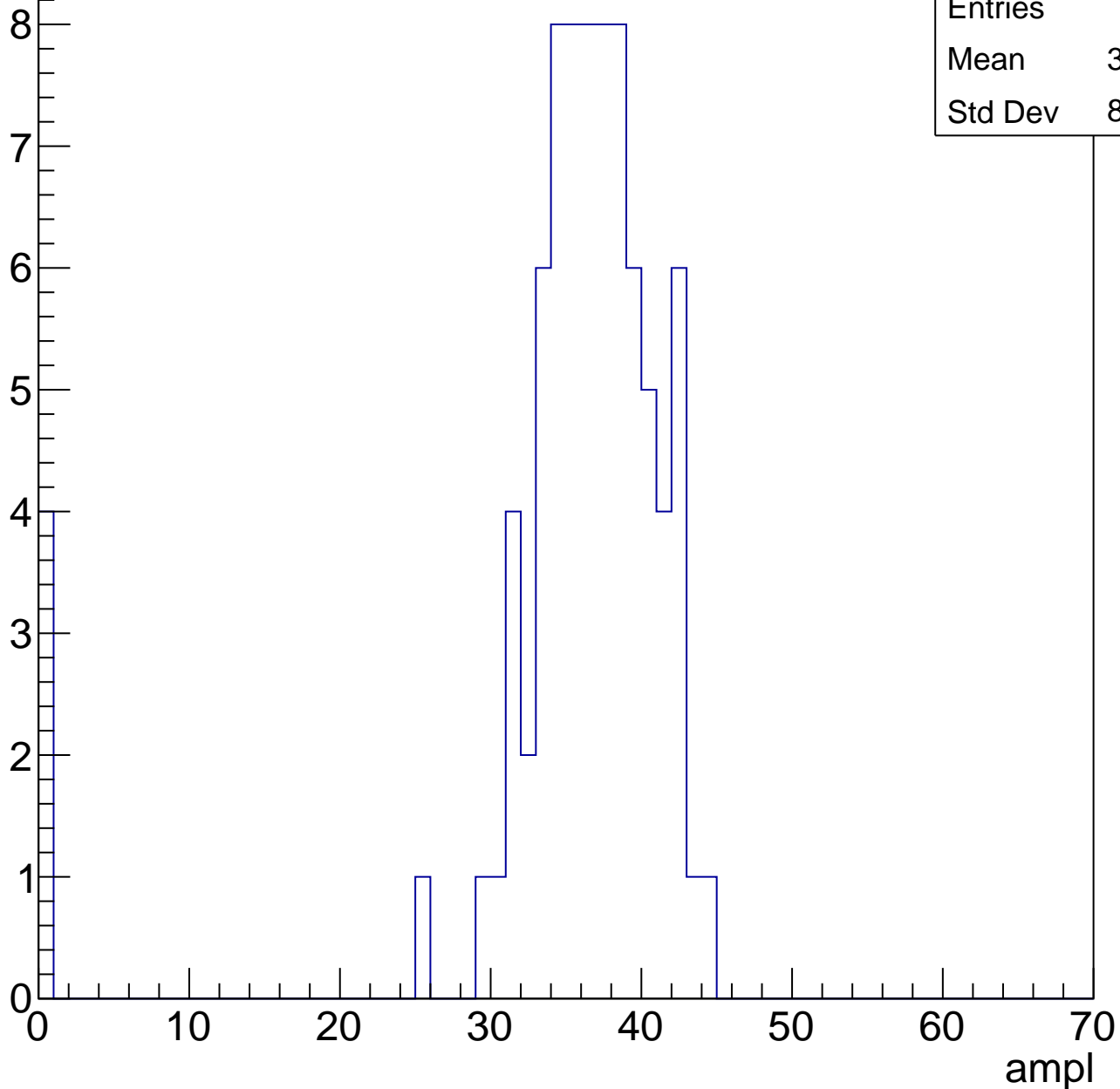


# B1L103S, U25-ch27, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	82
Mean	34.72
Std Dev	8.614



# B1L103S, U25-ch27, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

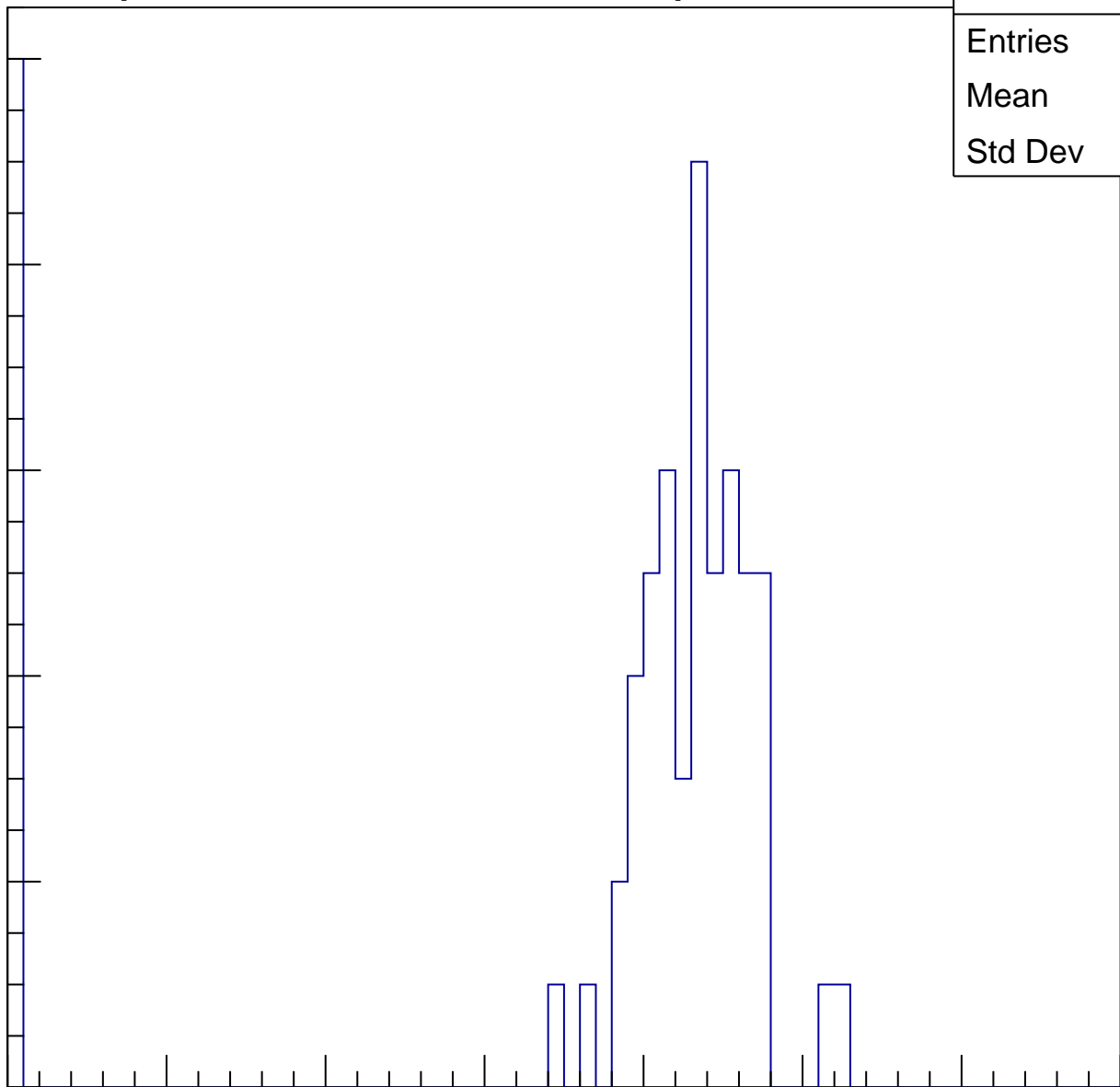
Entries	64
Mean	36.23
Std Dev	15.9

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

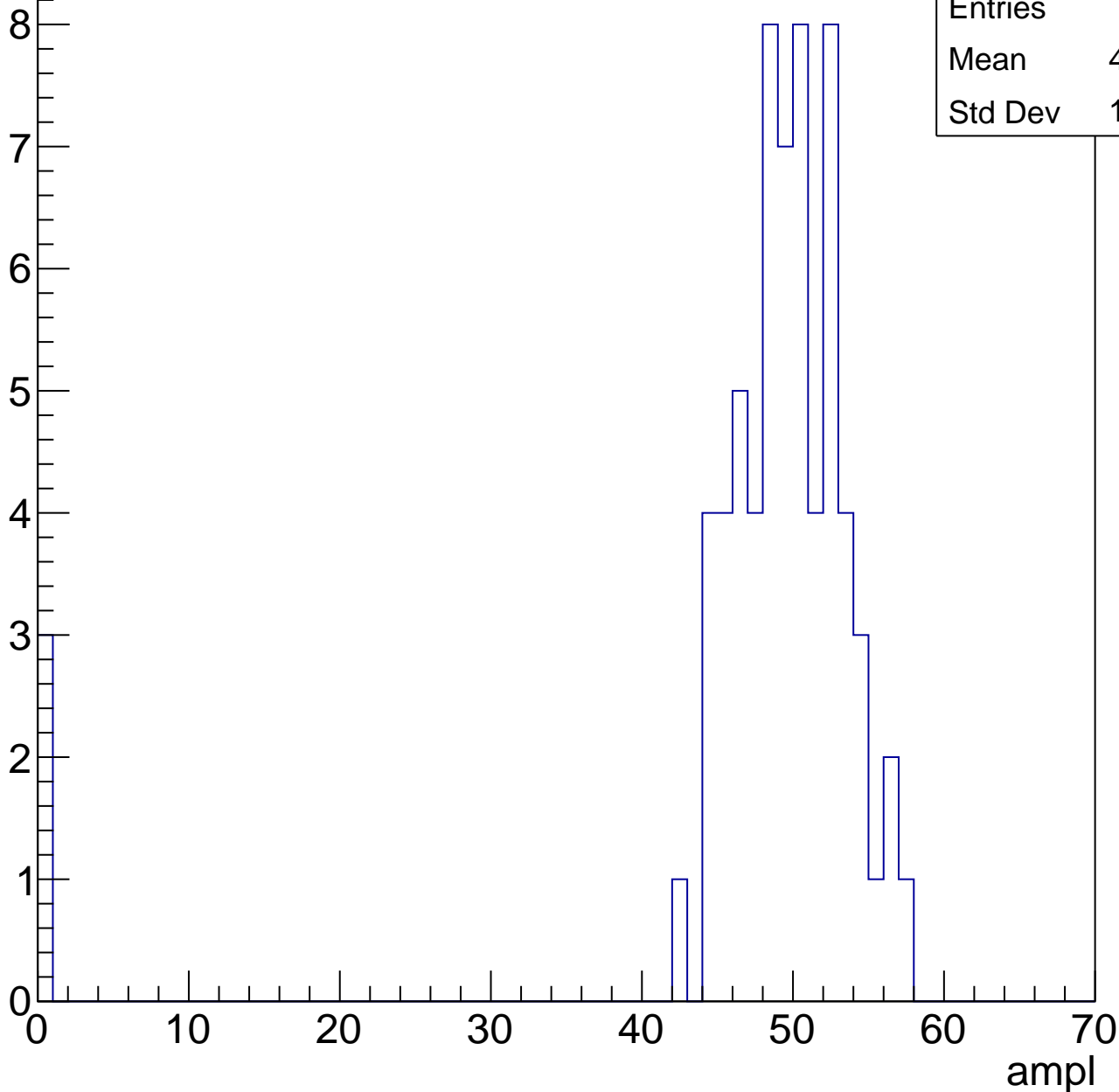


# B1L103S, U25-ch27, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	67
Mean	47.18
Std Dev	10.72

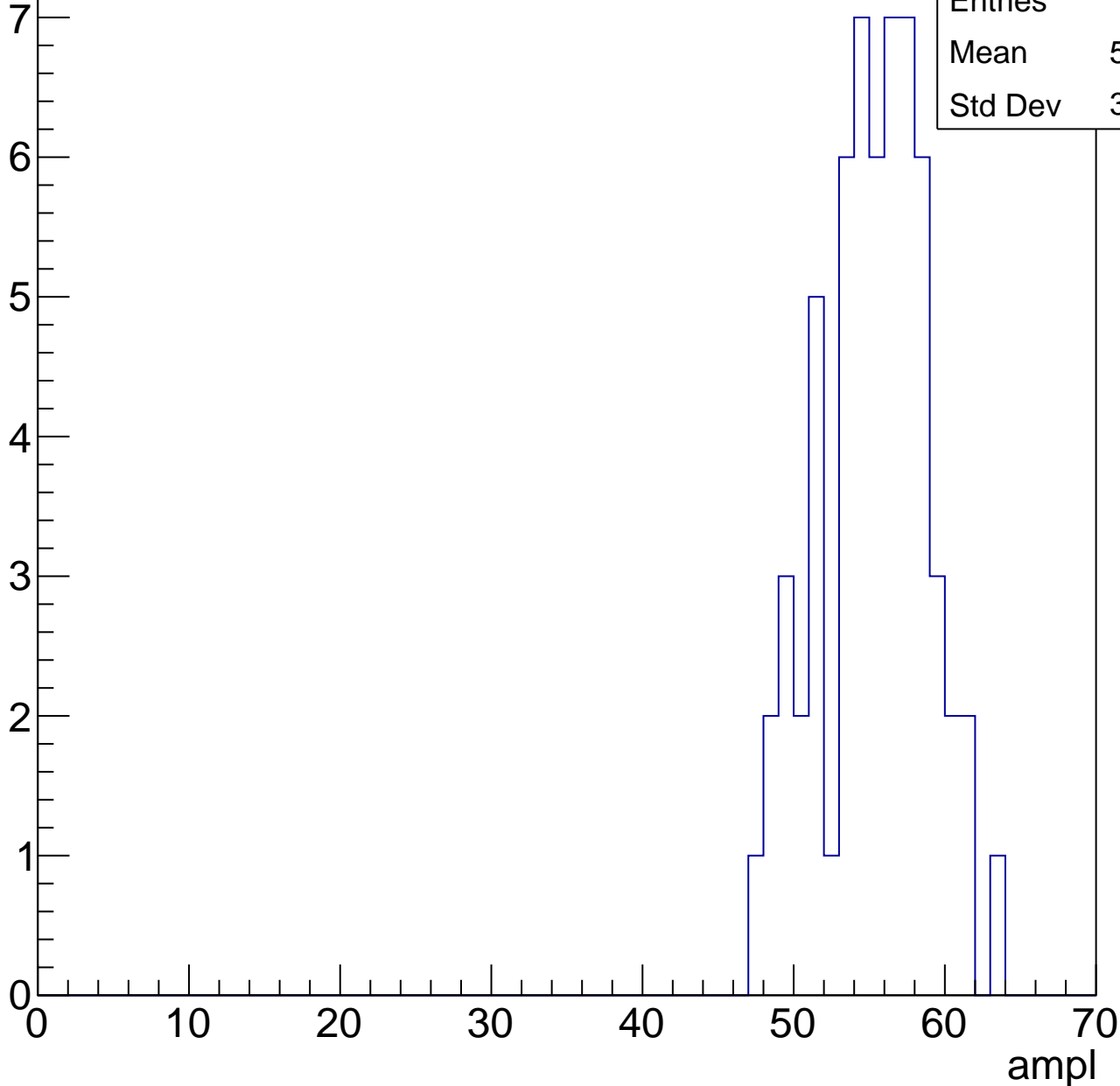


# B1L103S, U25-ch27, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	61
Mean	54.82
Std Dev	3.532

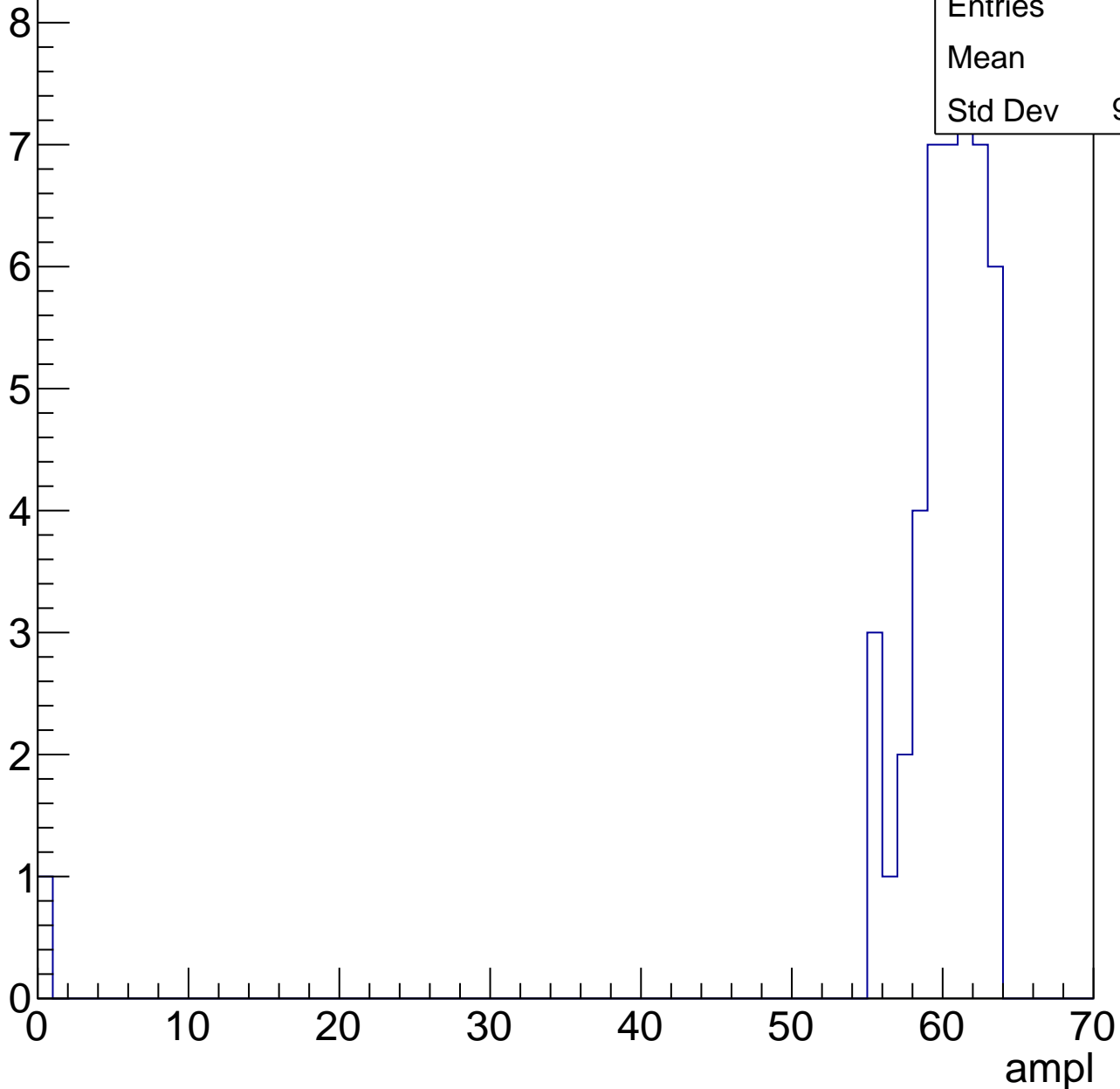


# B1L103S, U25-ch27, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

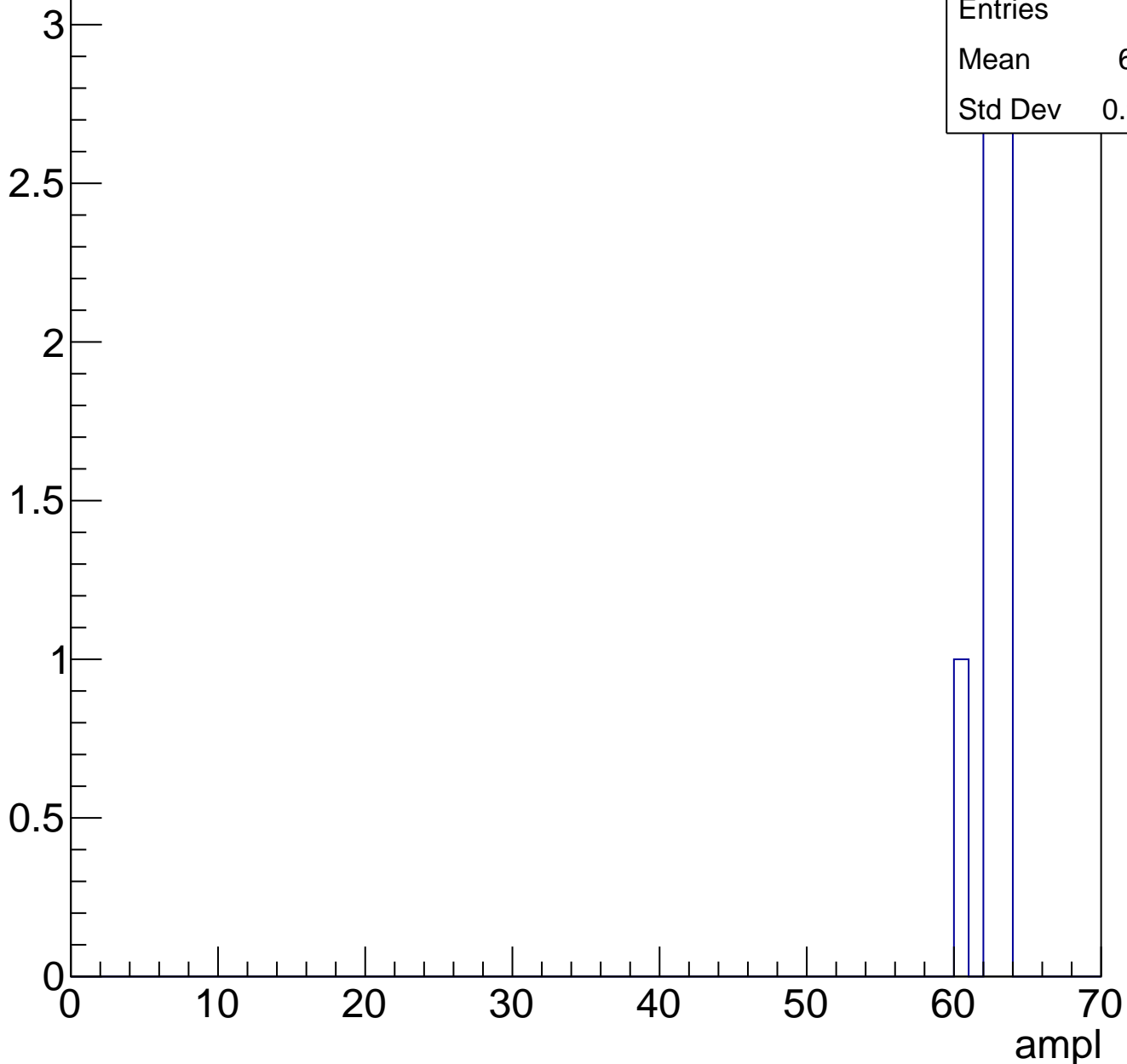
Entries	46
Mean	58.7
Std Dev	9.021



# B1L103S, U25-ch27, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U25-ch27, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

# B1L103S, U25-ch28, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	75
Mean	24.21
Std Dev	10.57

Entry

10

8

6

4

2

0

0

10

20

30

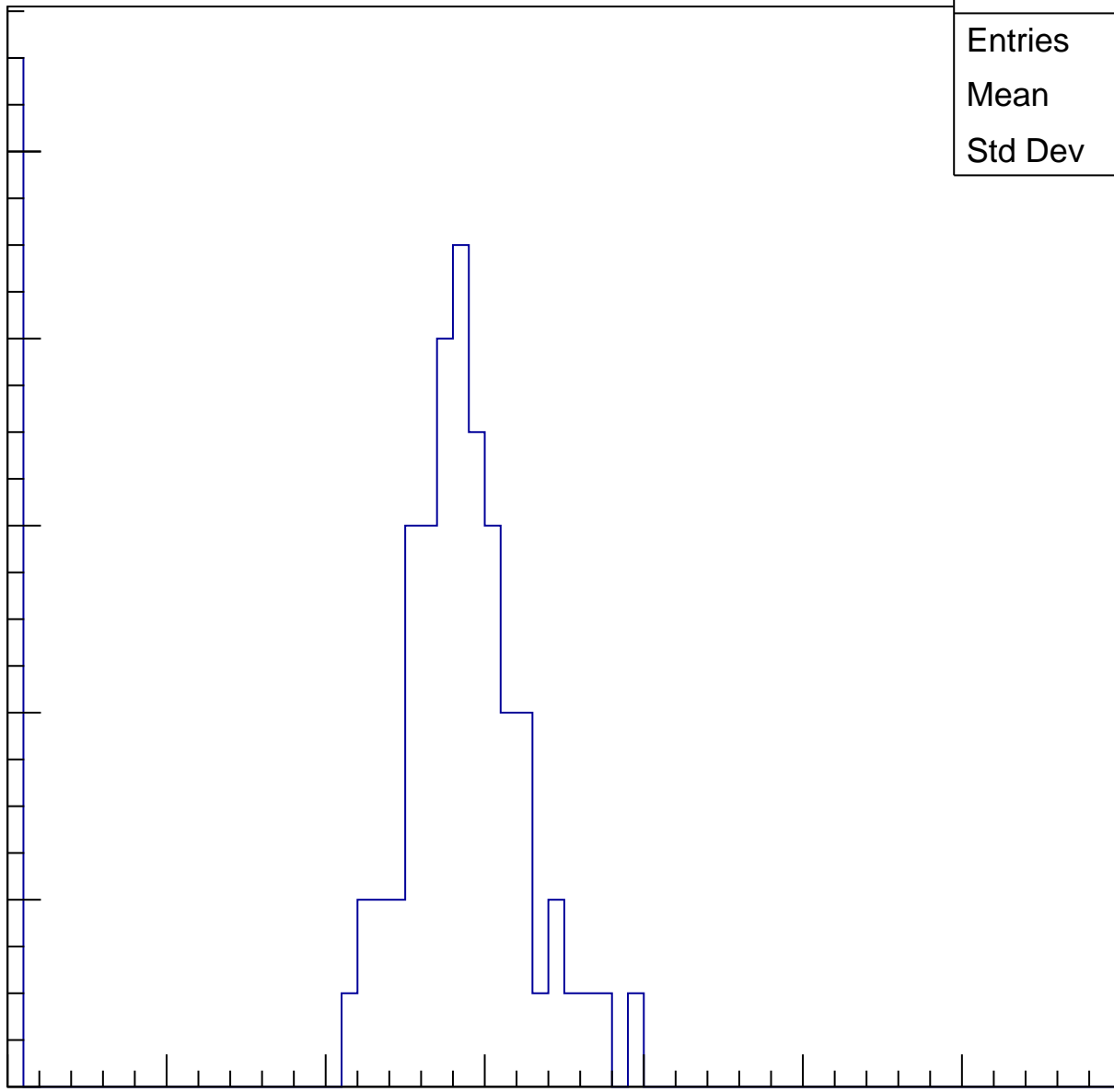
40

50

60

70

ampl

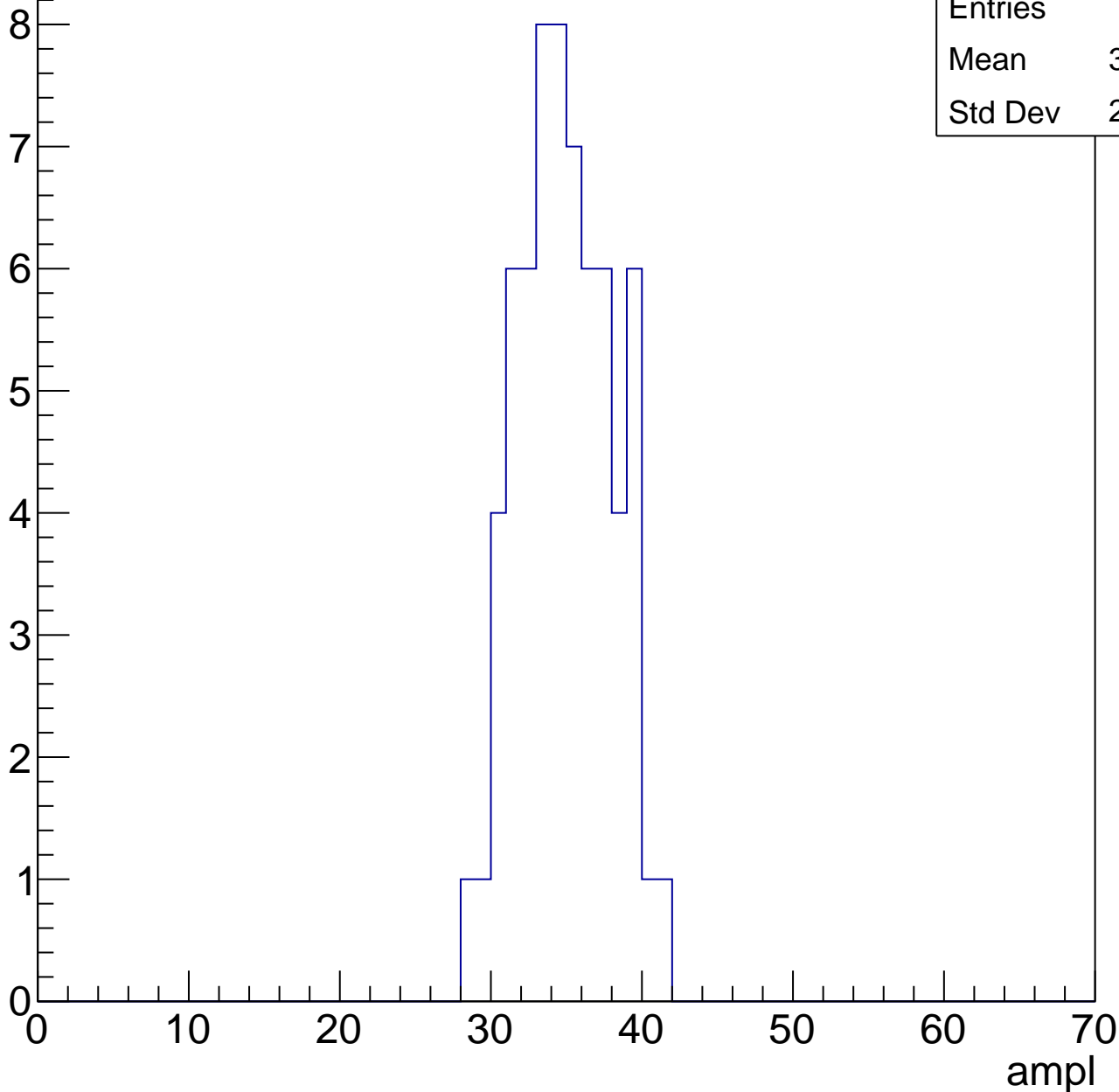


# B1L103S, U25-ch28, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	65
Mean	34.48
Std Dev	2.988



# B1L103S, U25-ch28, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	91
Mean	35.86
Std Dev	15

Entry

12

10

8

6

4

2

0

0

10

20

30

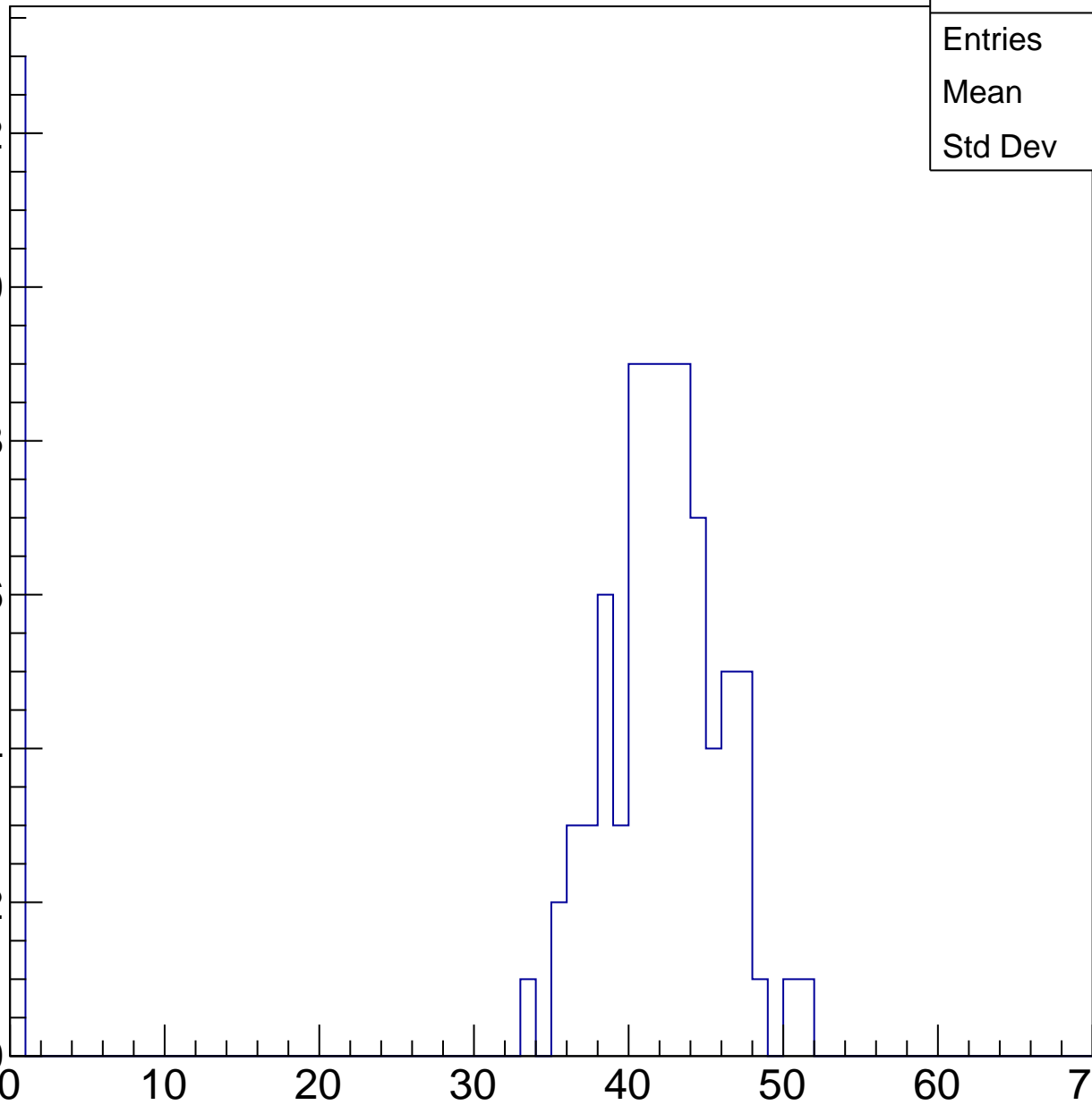
40

50

60

70

ampl

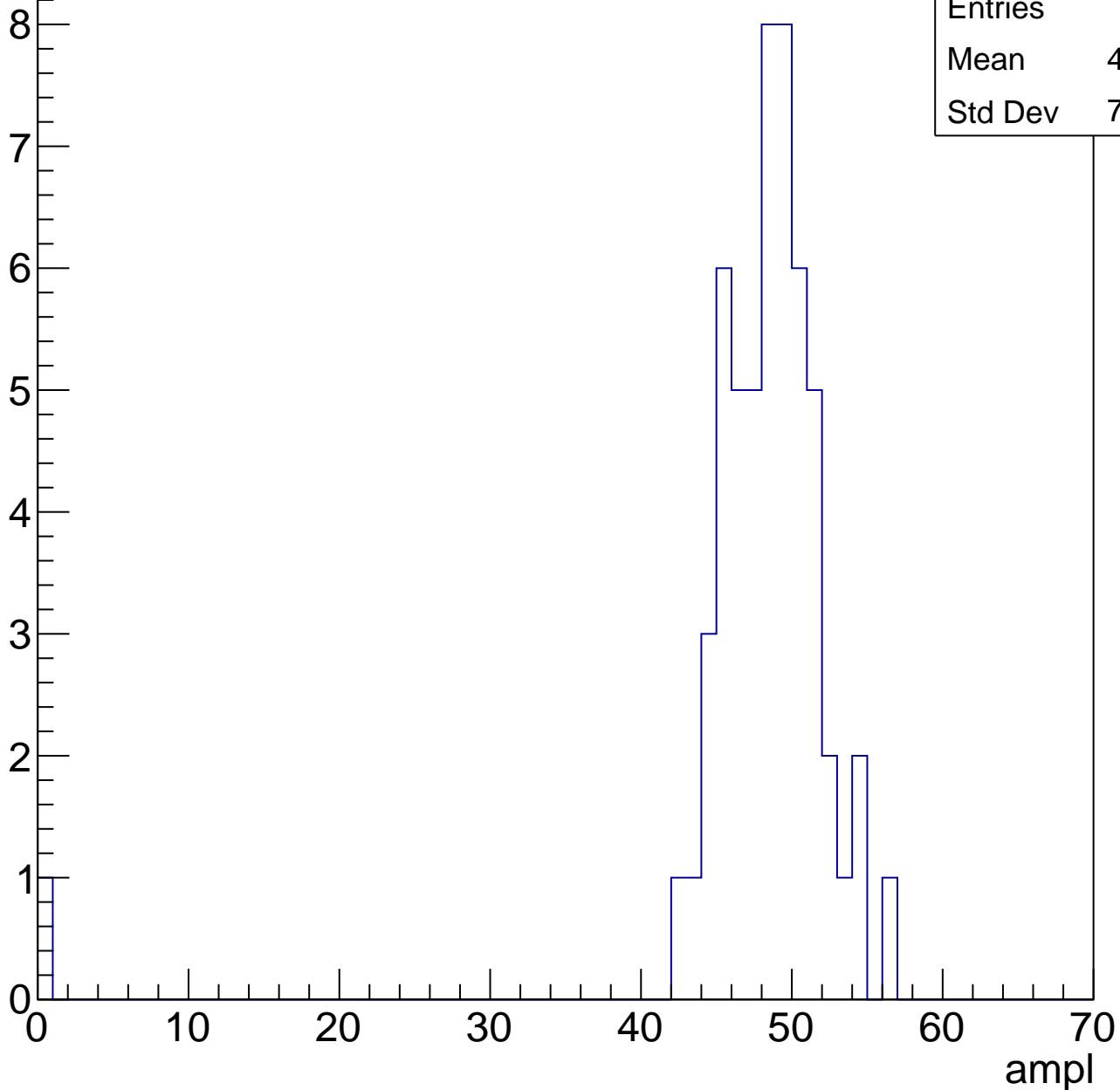


# B1L103S, U25-ch28, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

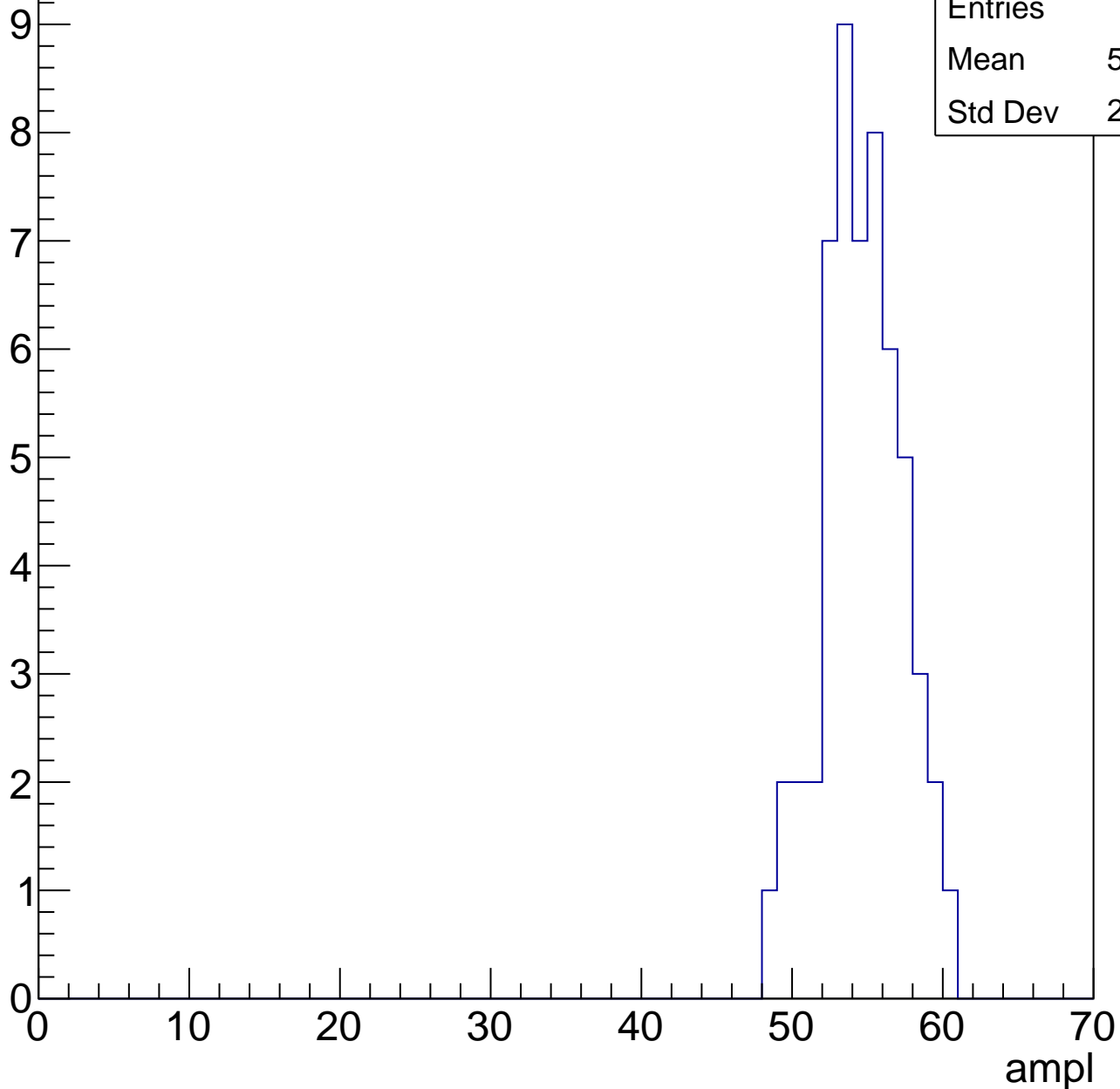
Entries	55
Mean	47.35
Std Dev	7.056



# B1L103S, U25-ch28, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



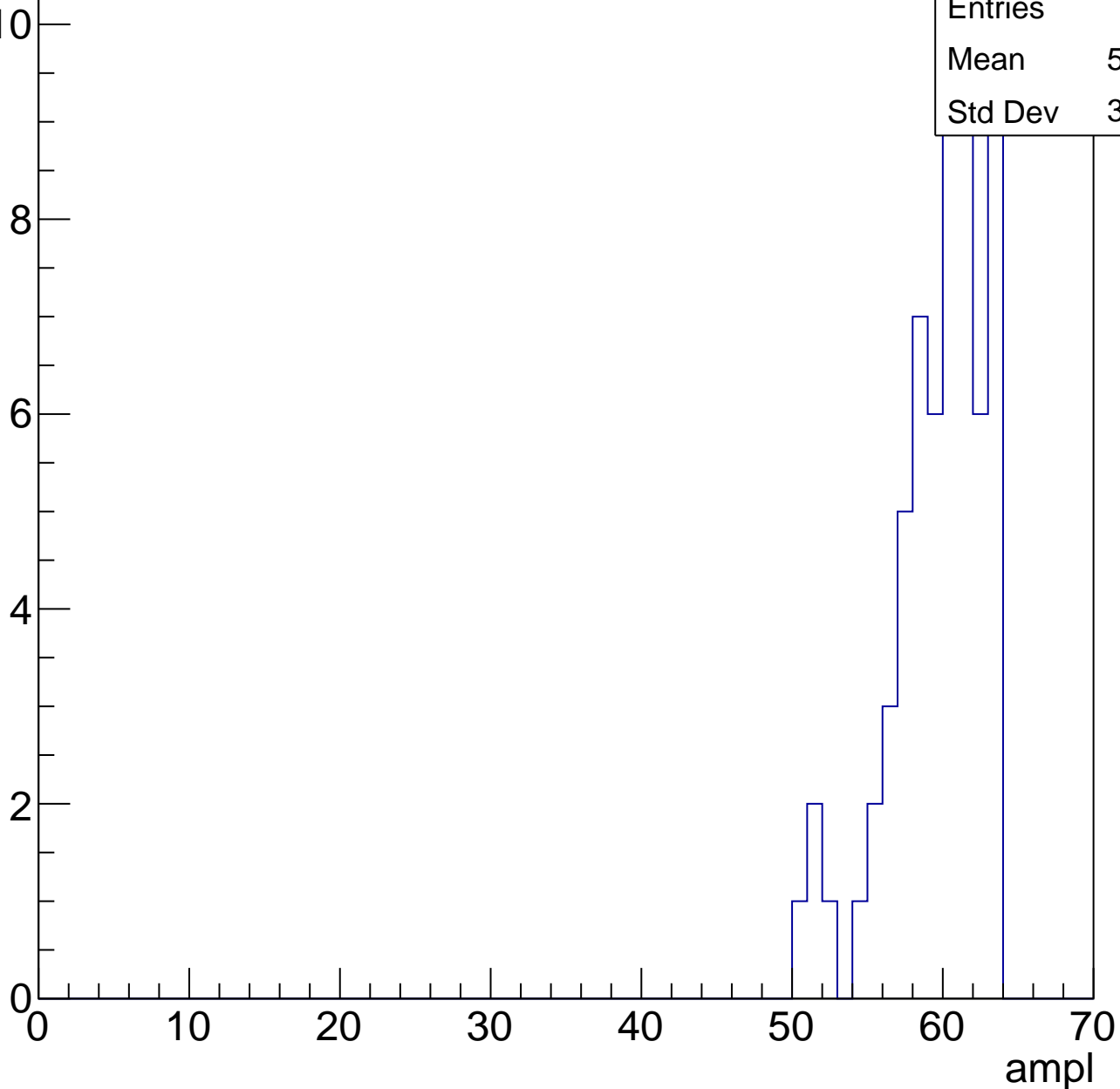
Entries	55
Mean	54.18
Std Dev	2.636

# B1L103S, U25-ch28, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

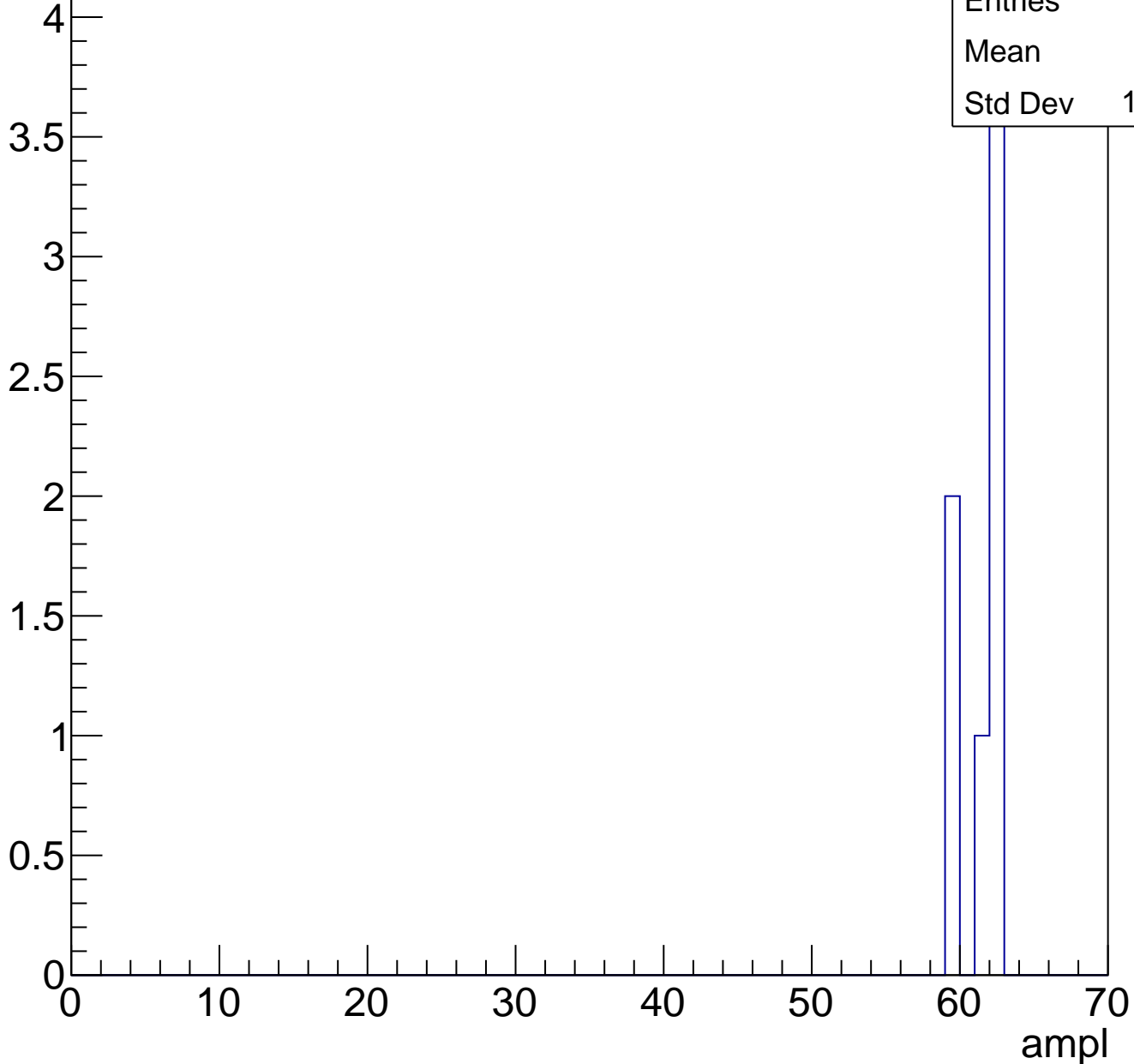
Entries	62
Mean	59.23
Std Dev	3.175



# B1L103S, U25-ch28, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	7
Mean	61
Std Dev	1.309

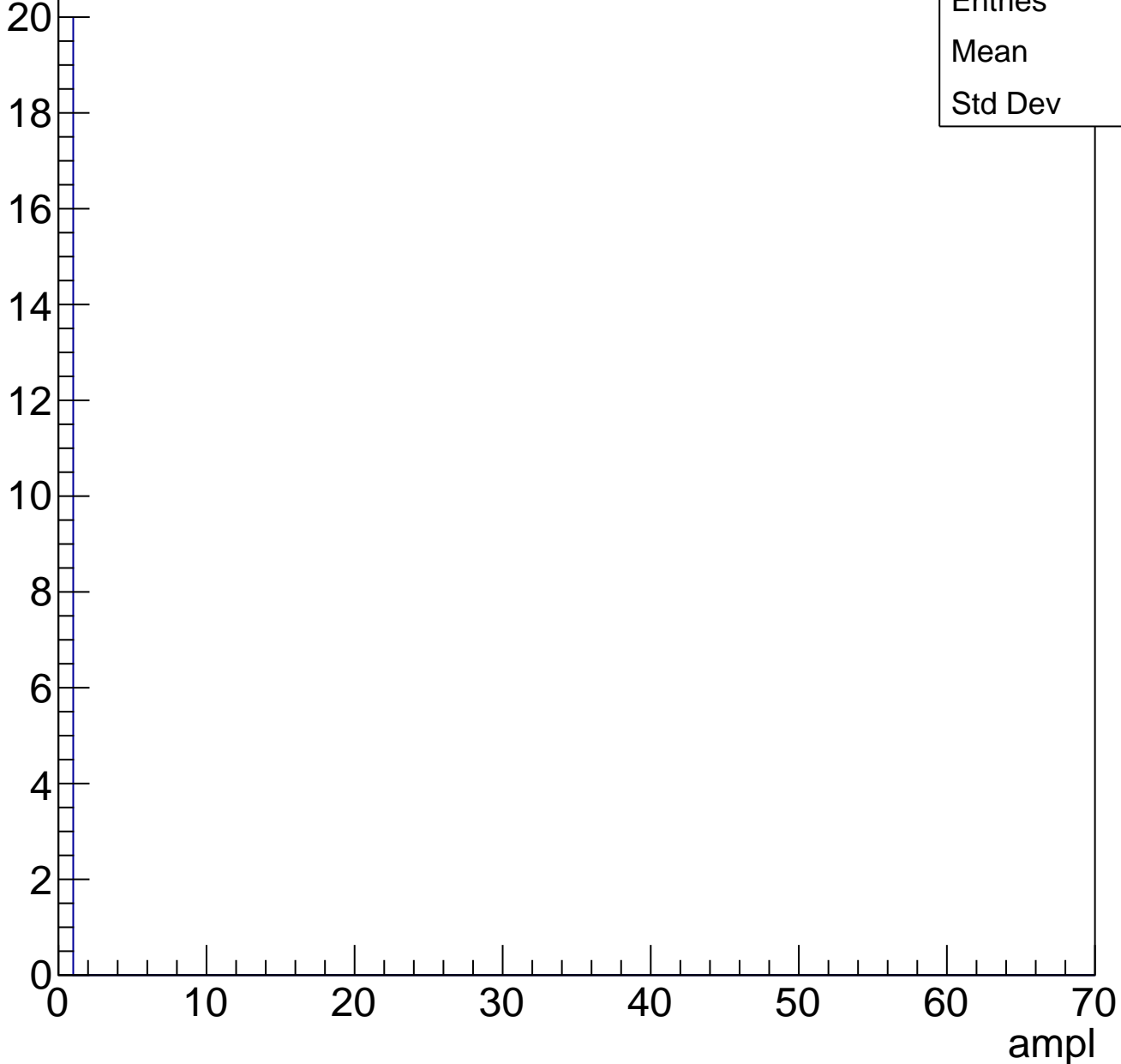


# B1L103S, U25-ch28, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	20
Mean	0
Std Dev	0

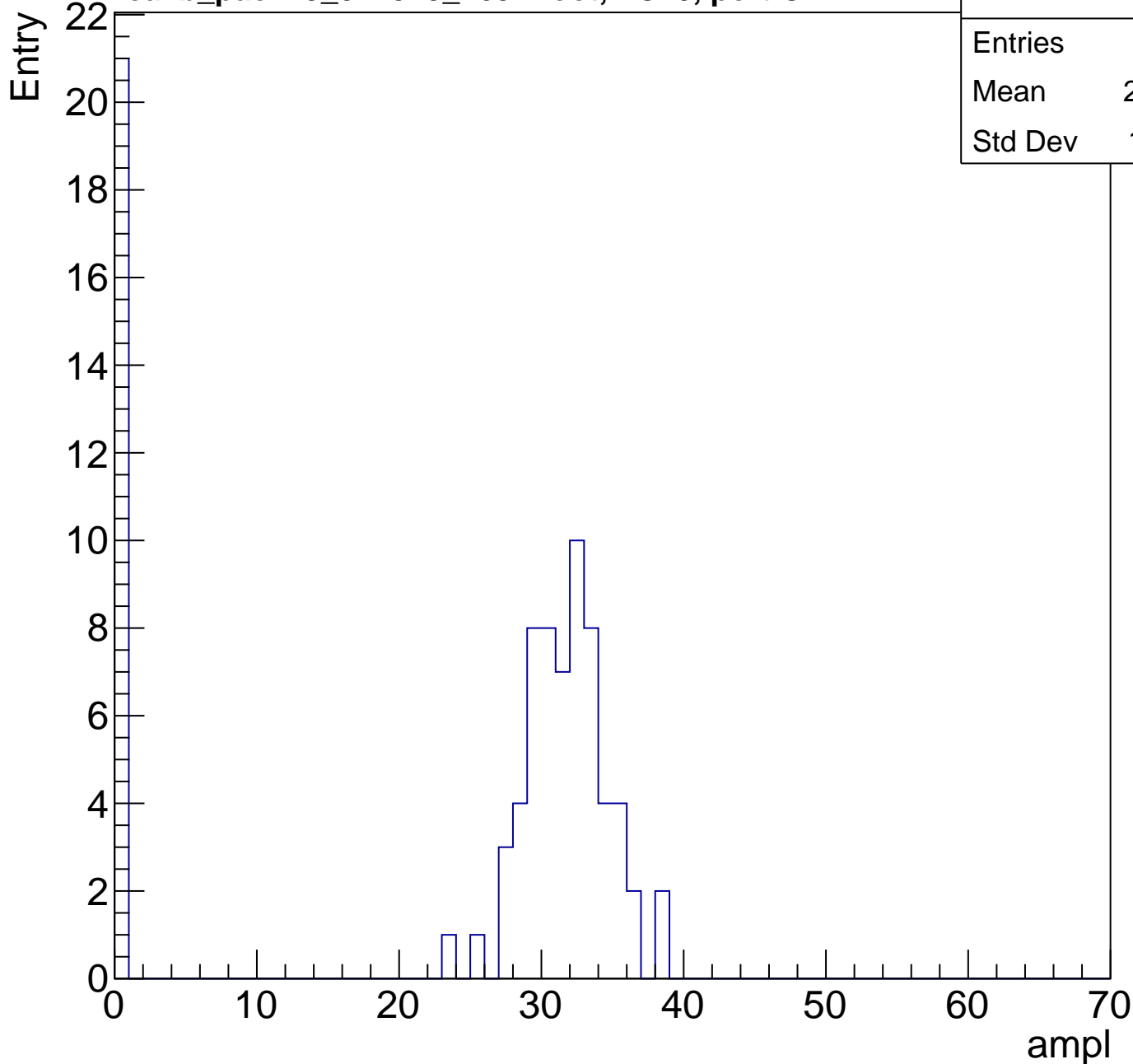
Entry



# B1L103S, U25-ch29, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	83
Mean	23.35
Std Dev	13.81

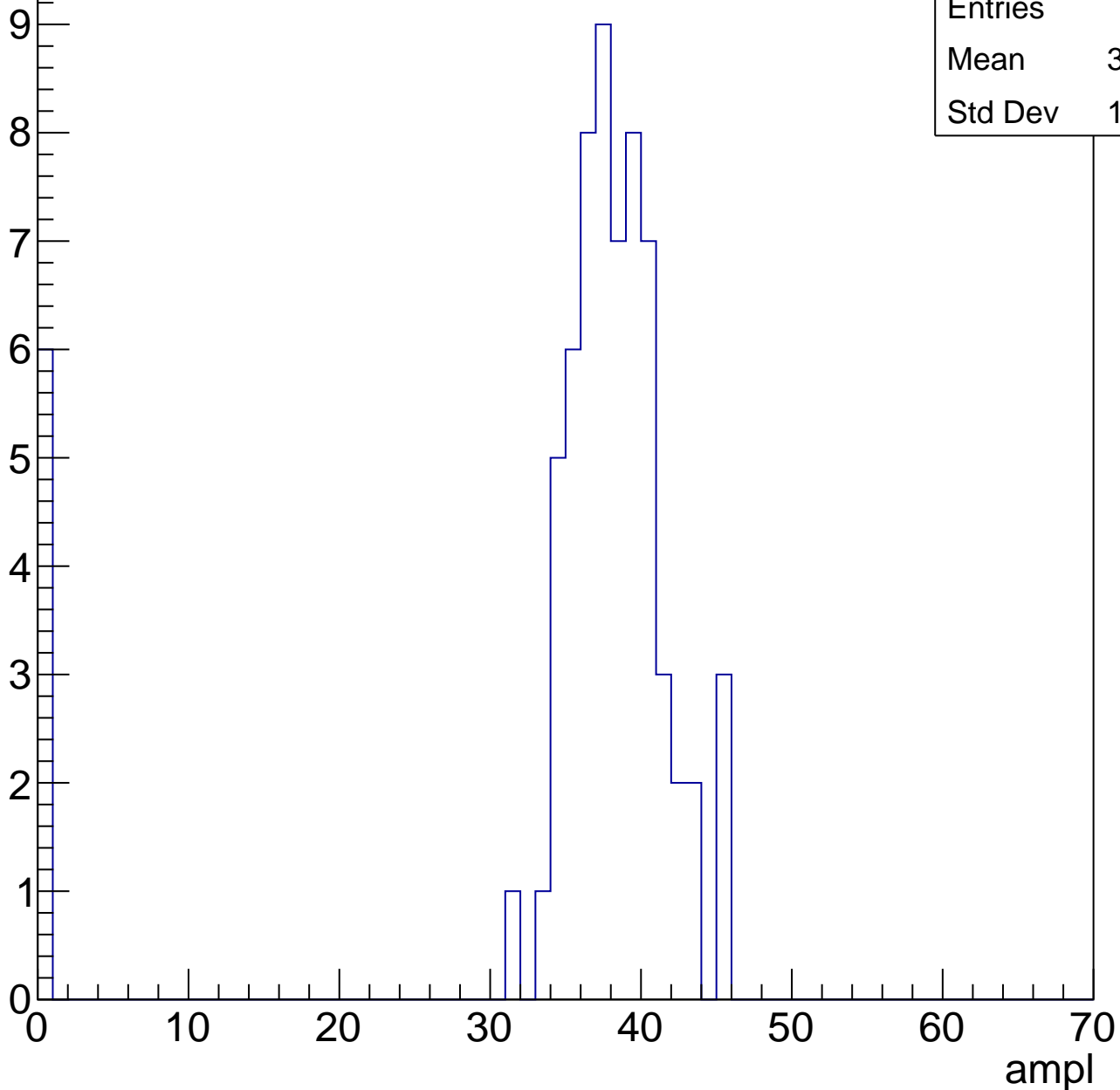


# B1L103S, U25-ch29, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	68
Mean	34.57
Std Dev	11.12

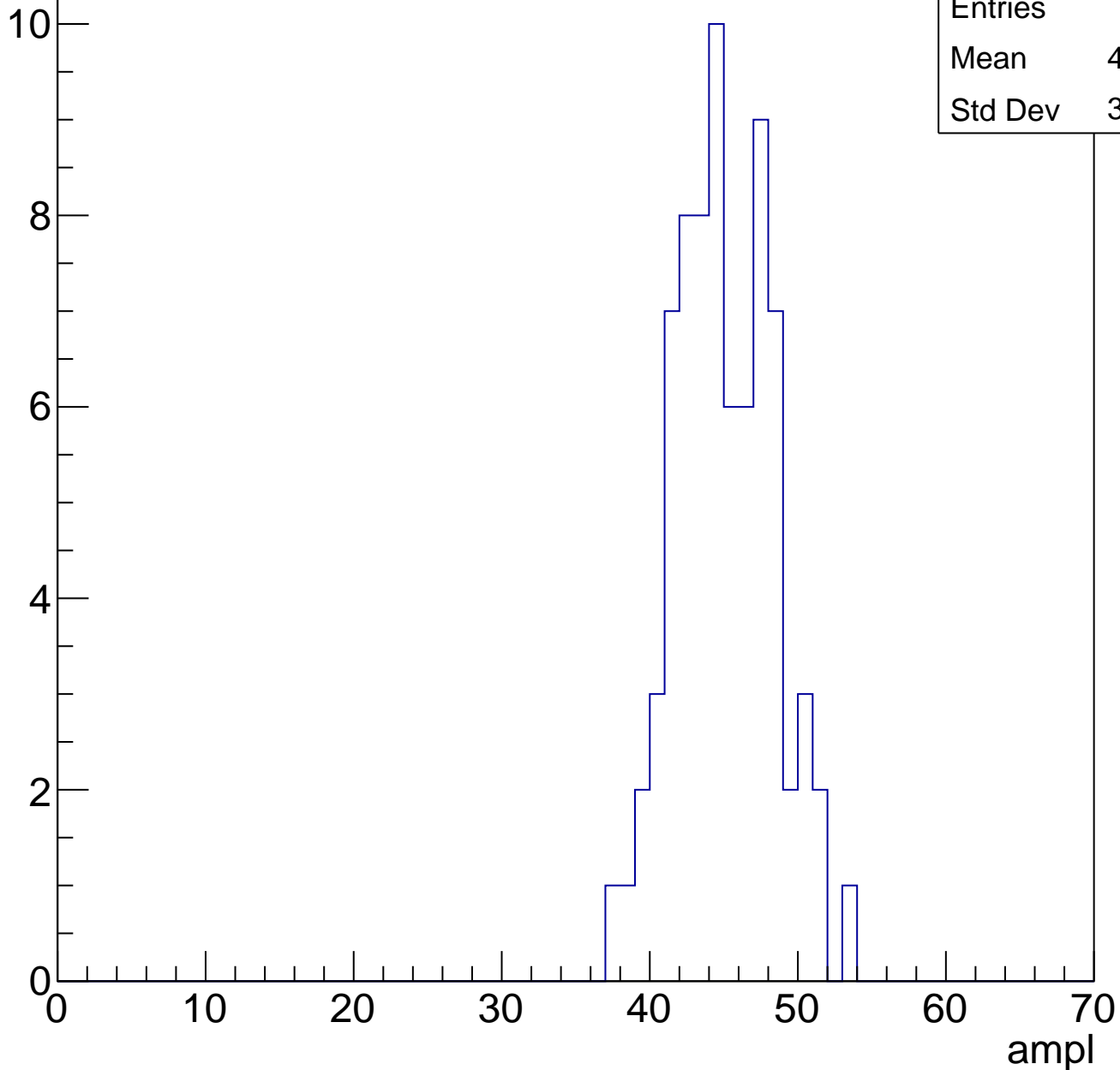


# B1L103S, U25-ch29, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	76
Mean	44.58
Std Dev	3.286

Entry

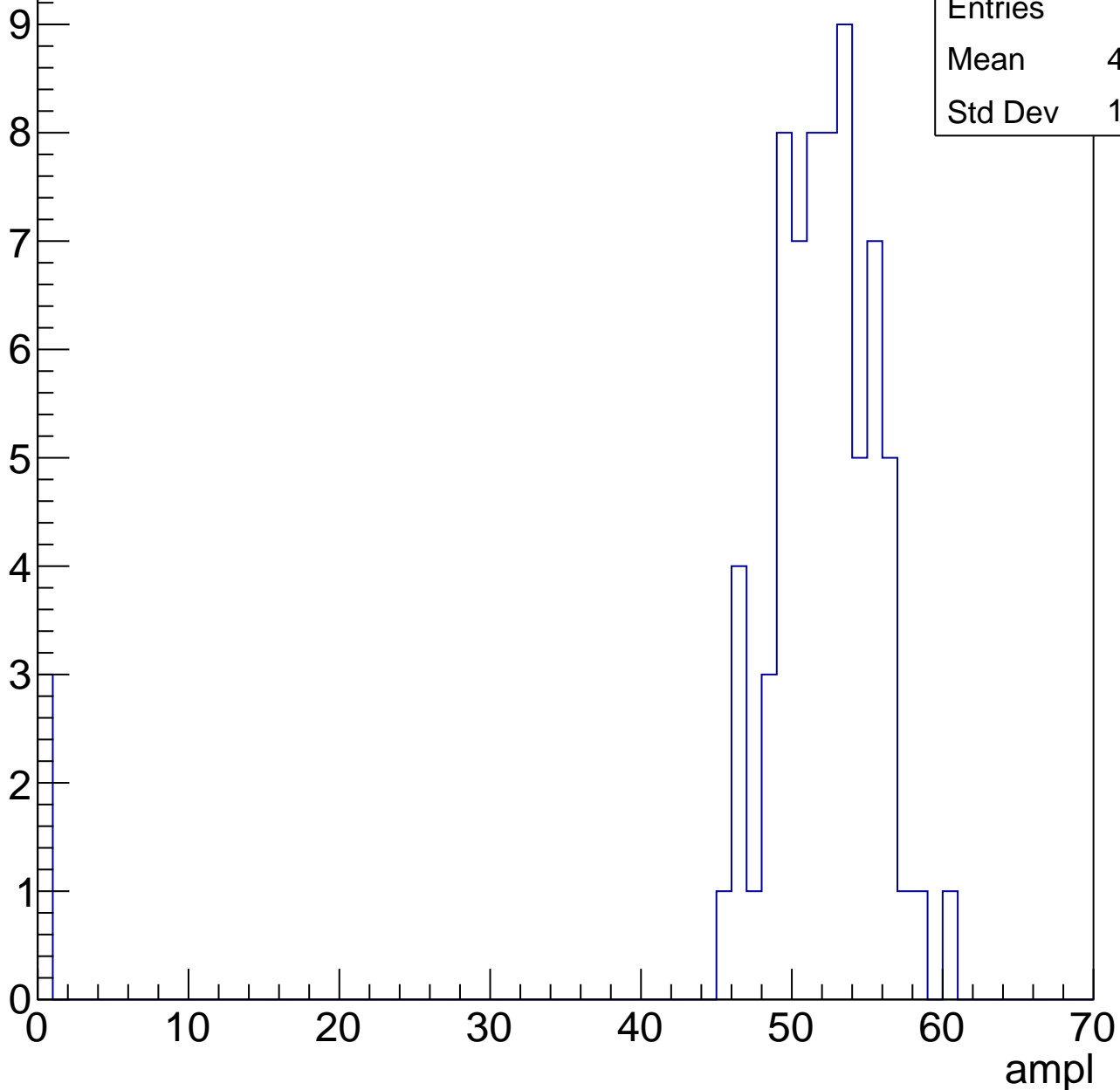


# B1L103S, U25-ch29, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	72
Mean	49.62
Std Dev	10.79

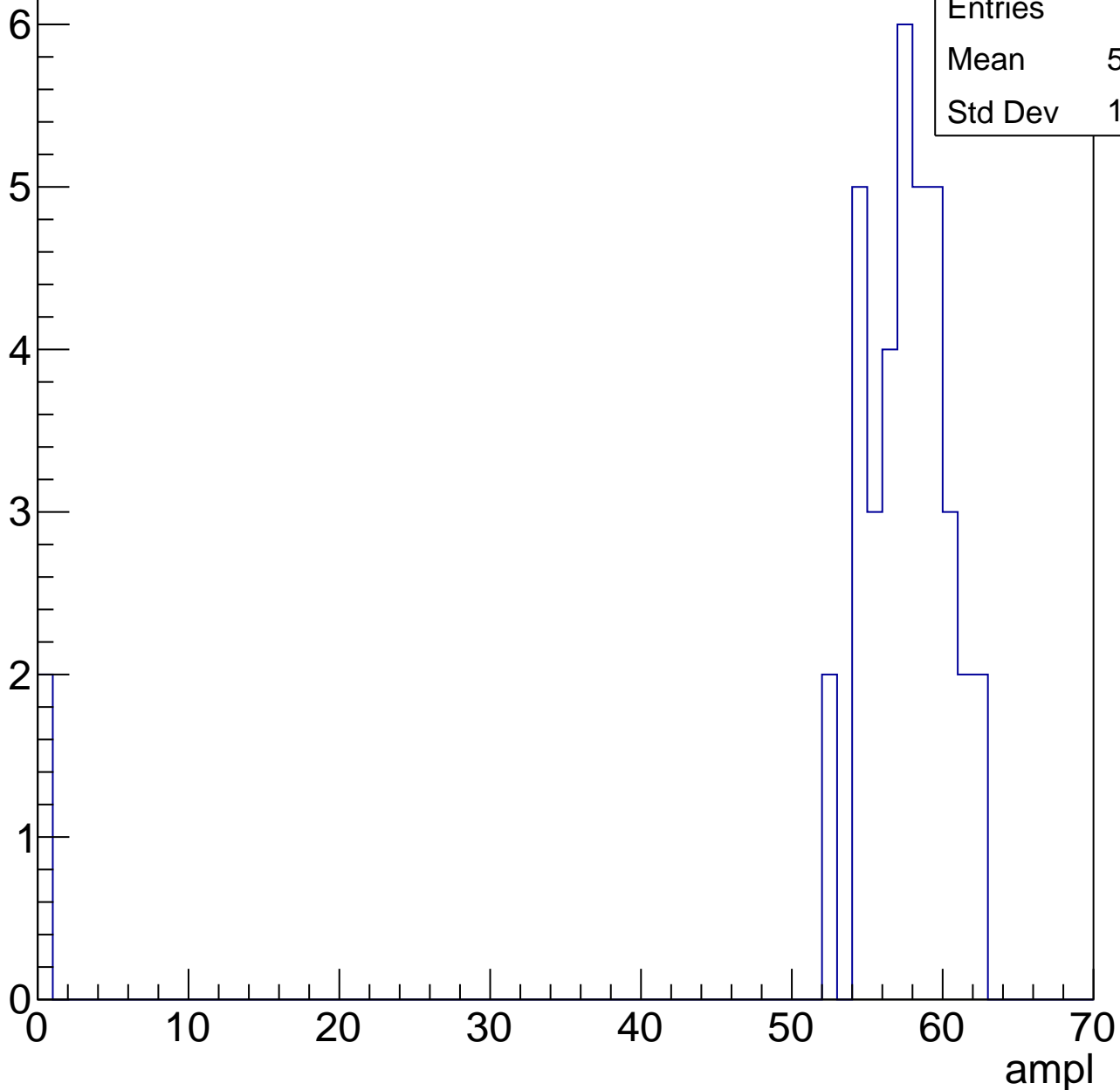


# B1L103S, U25-ch29, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	39
Mean	54.26
Std Dev	12.86

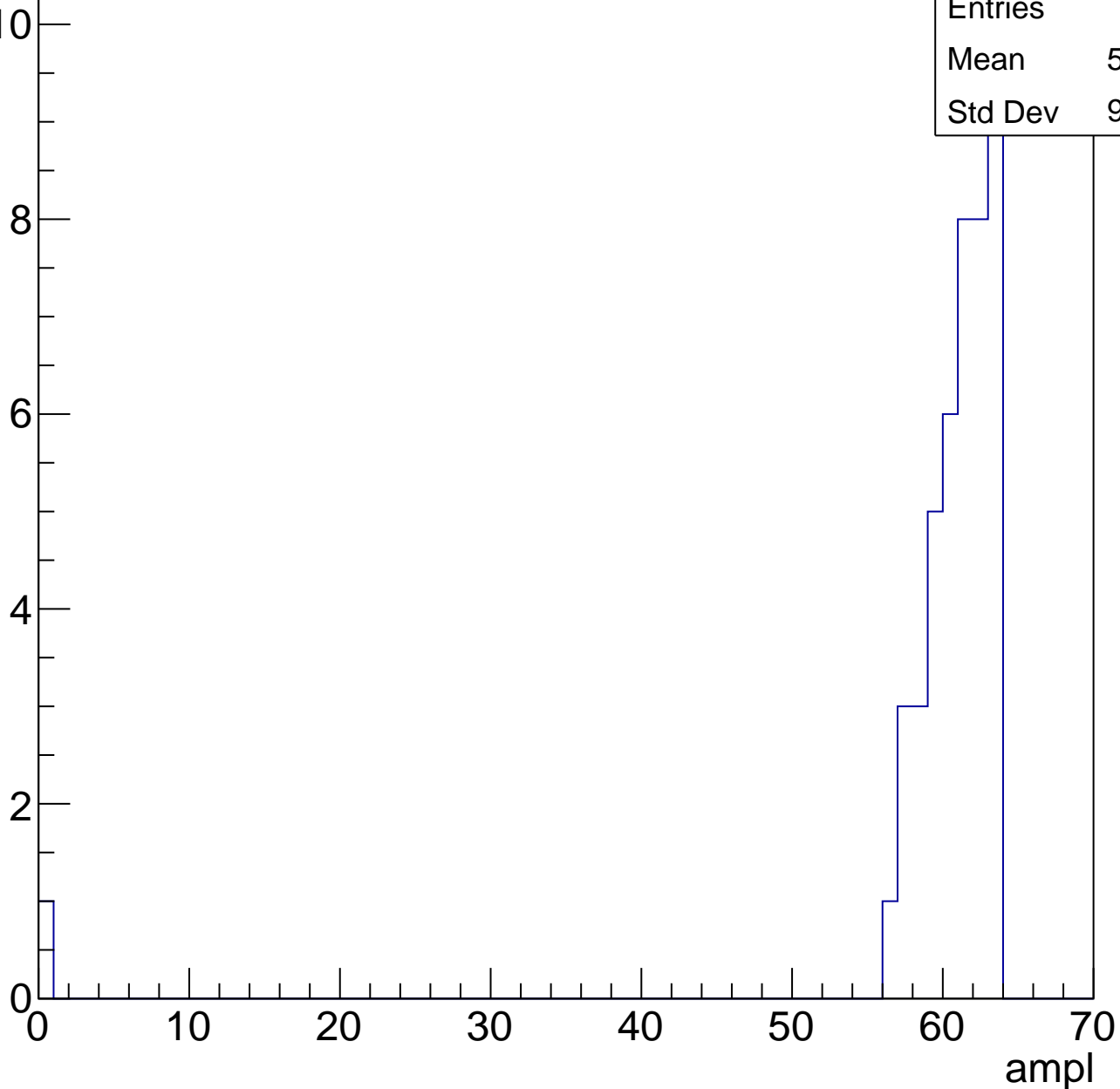


# B1L103S, U25-ch29, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

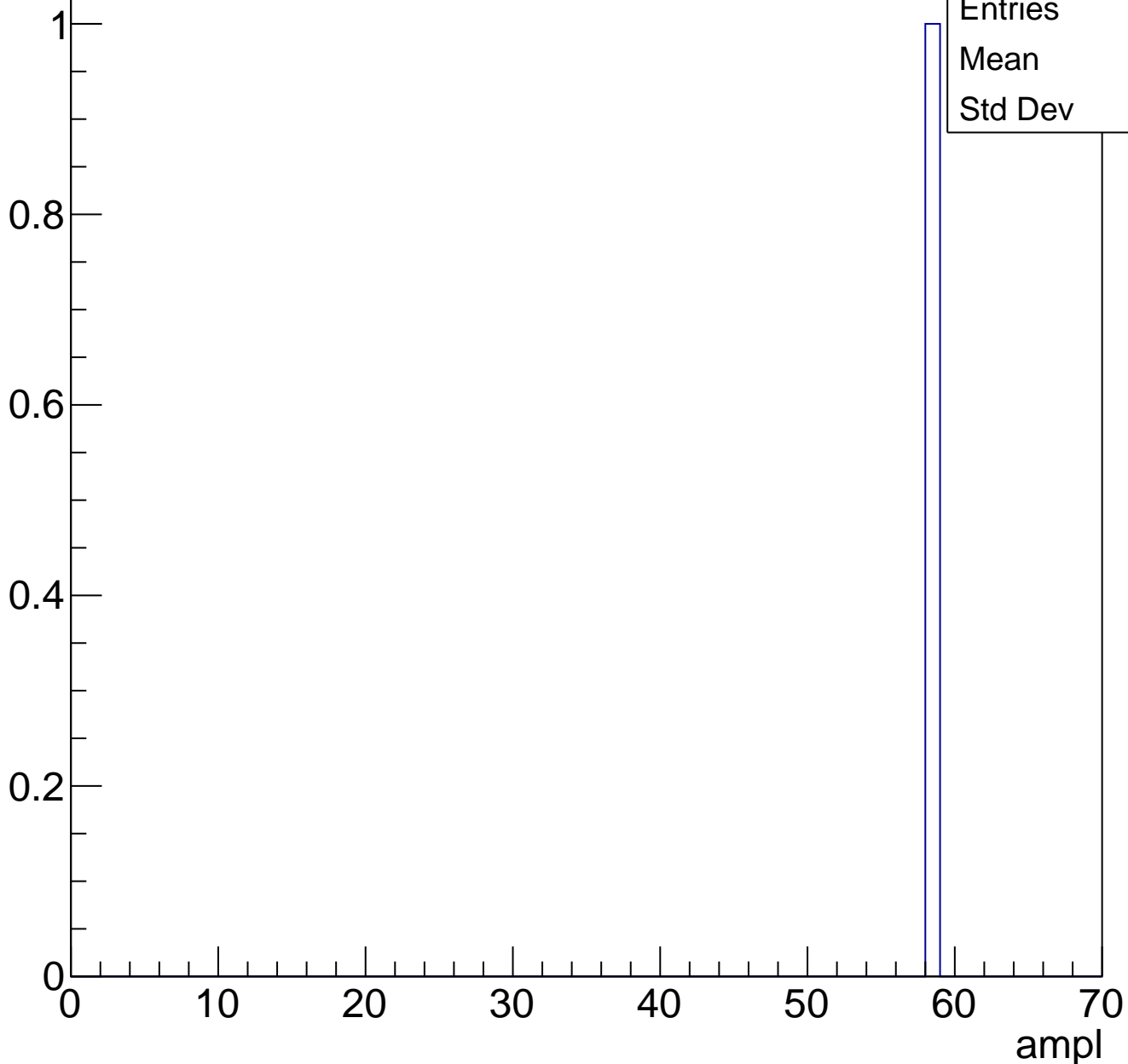
Entries	45
Mean	59.33
Std Dev	9.153



# B1L103S, U25-ch29, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	1
Mean	58
Std Dev	0



# B1L103S, U25-ch29, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

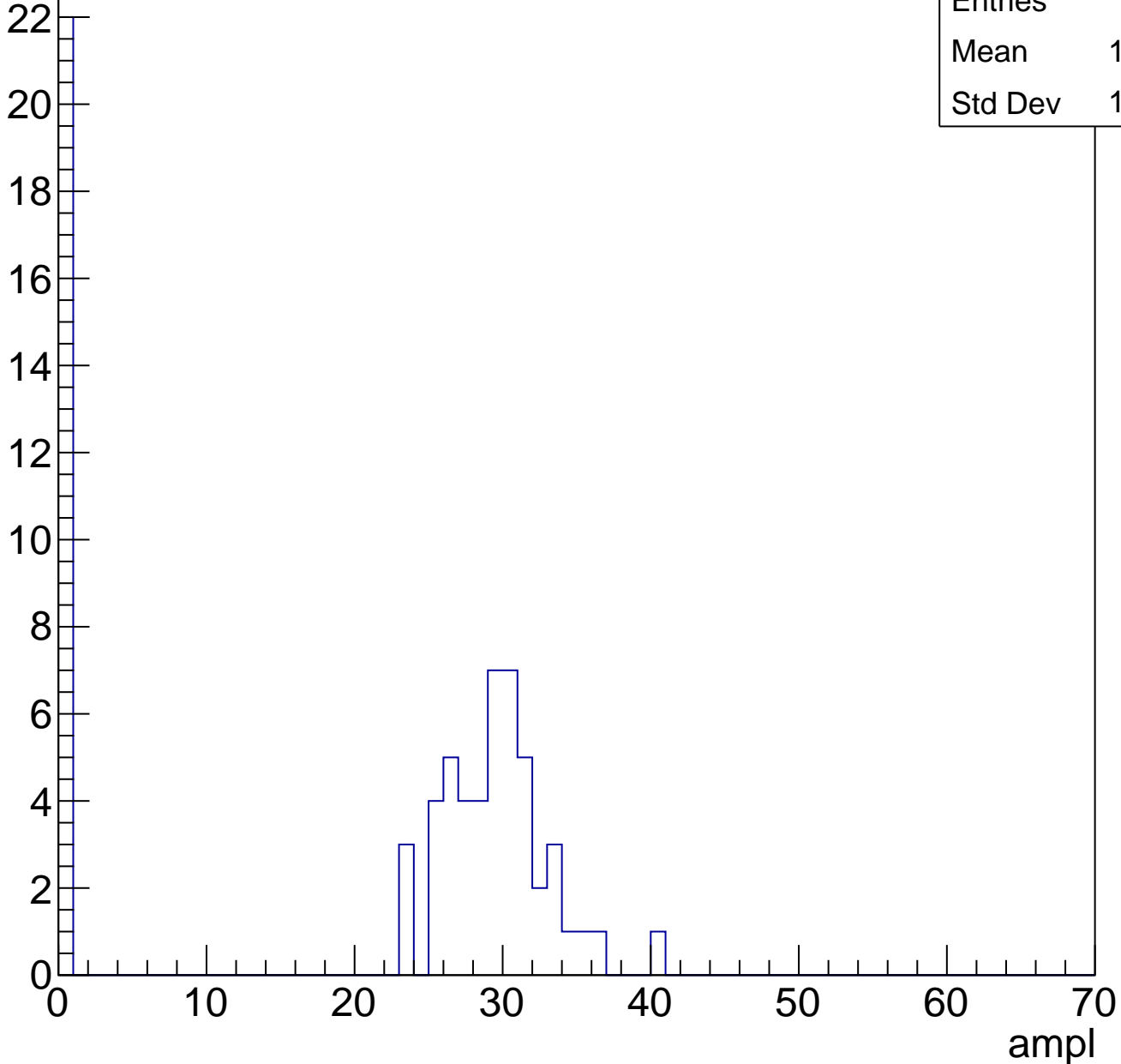
Entries	19
Mean	0
Std Dev	0

# B1L103S, U25-ch30, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	70
Mean	19.93
Std Dev	13.79

Entry



# B1L103S, U25-ch30, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	83
Mean	29.52
Std Dev	13.09

Entry

12

10

8

6

4

2

0

0

10

20

30

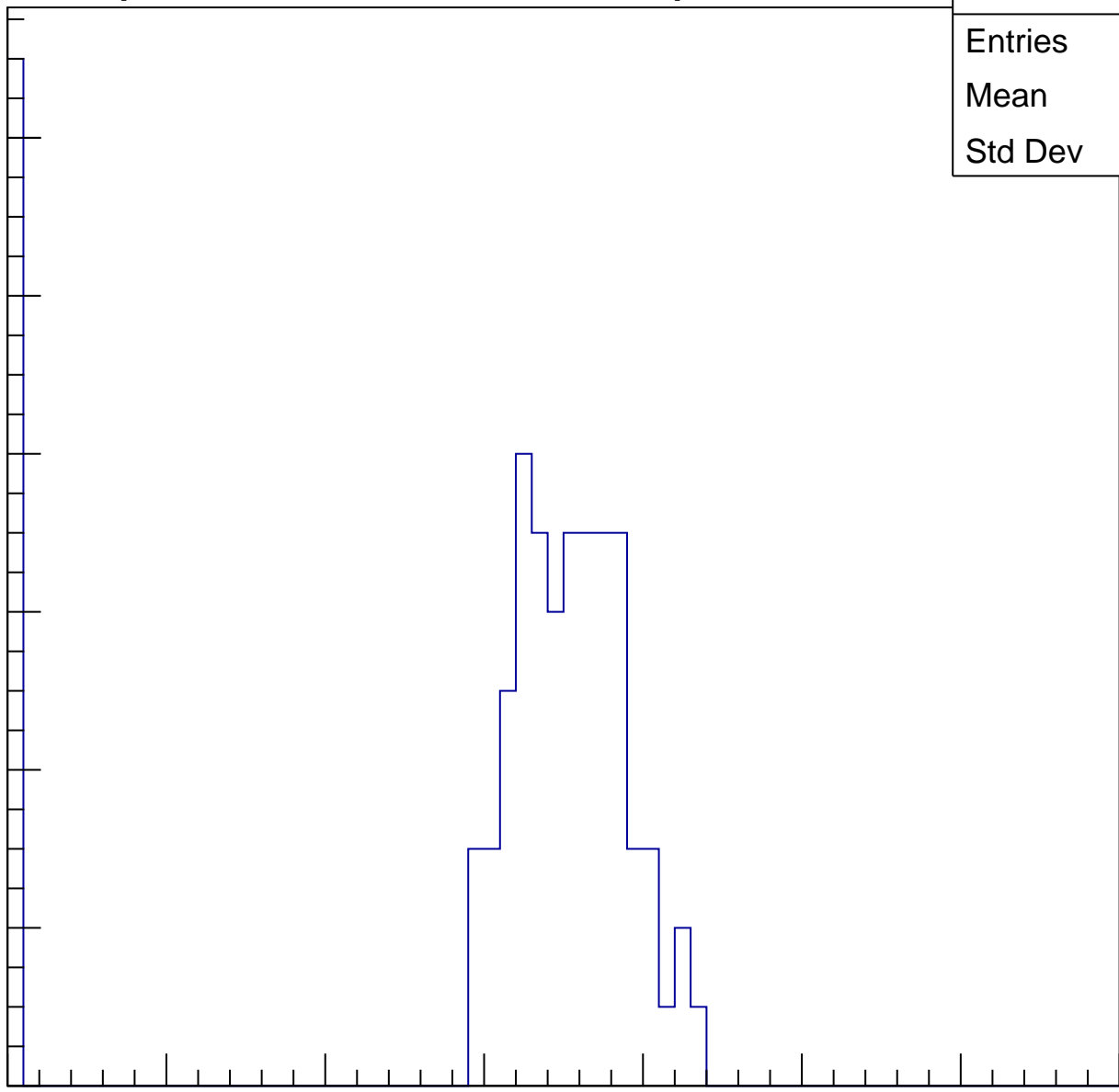
40

50

60

70

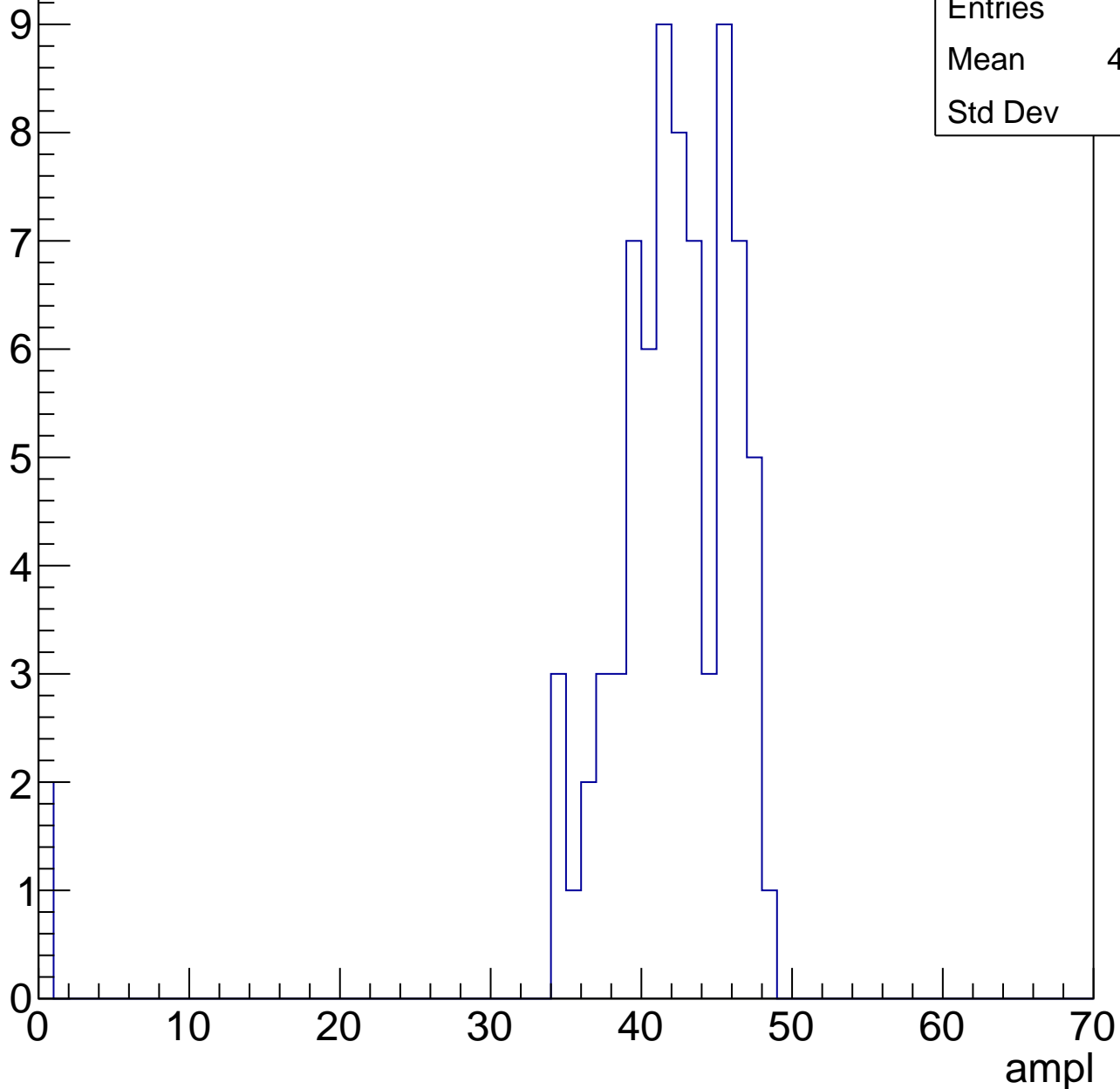
ampl



# B1L103S, U25-ch30, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U25-ch30, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

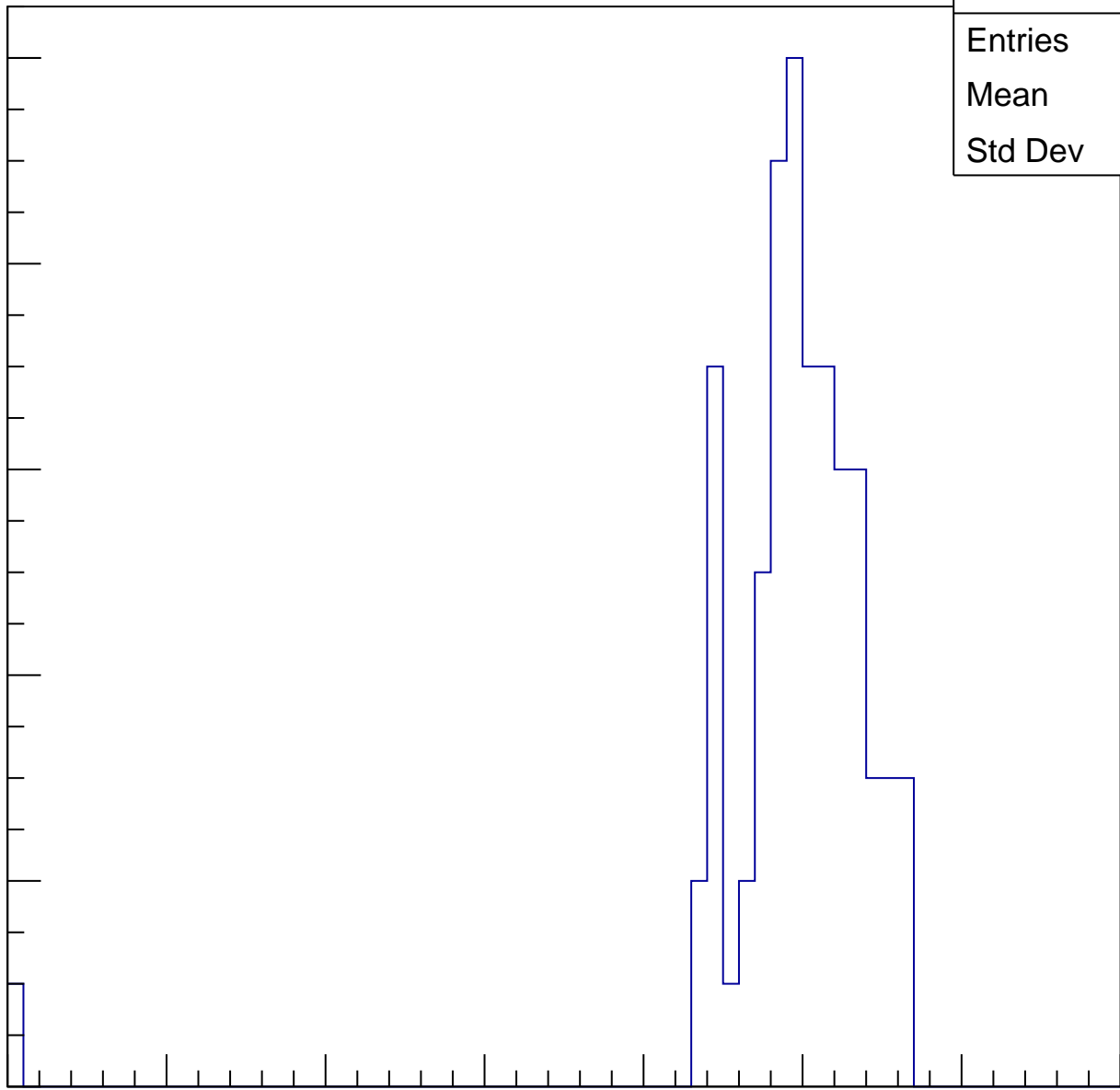
Entries	72
Mean	48.89
Std Dev	6.693

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

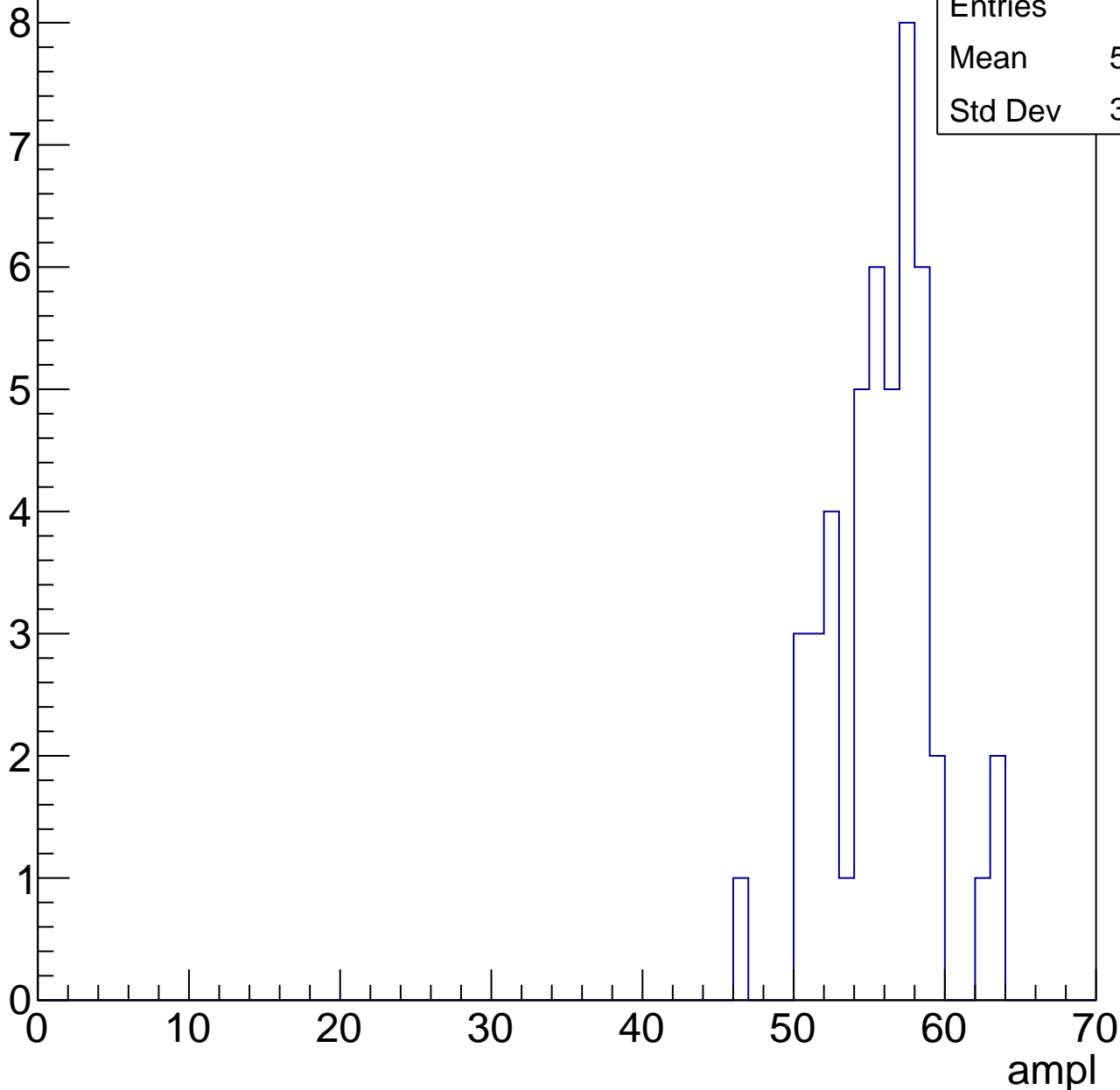


# B1L103S, U25-ch30, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

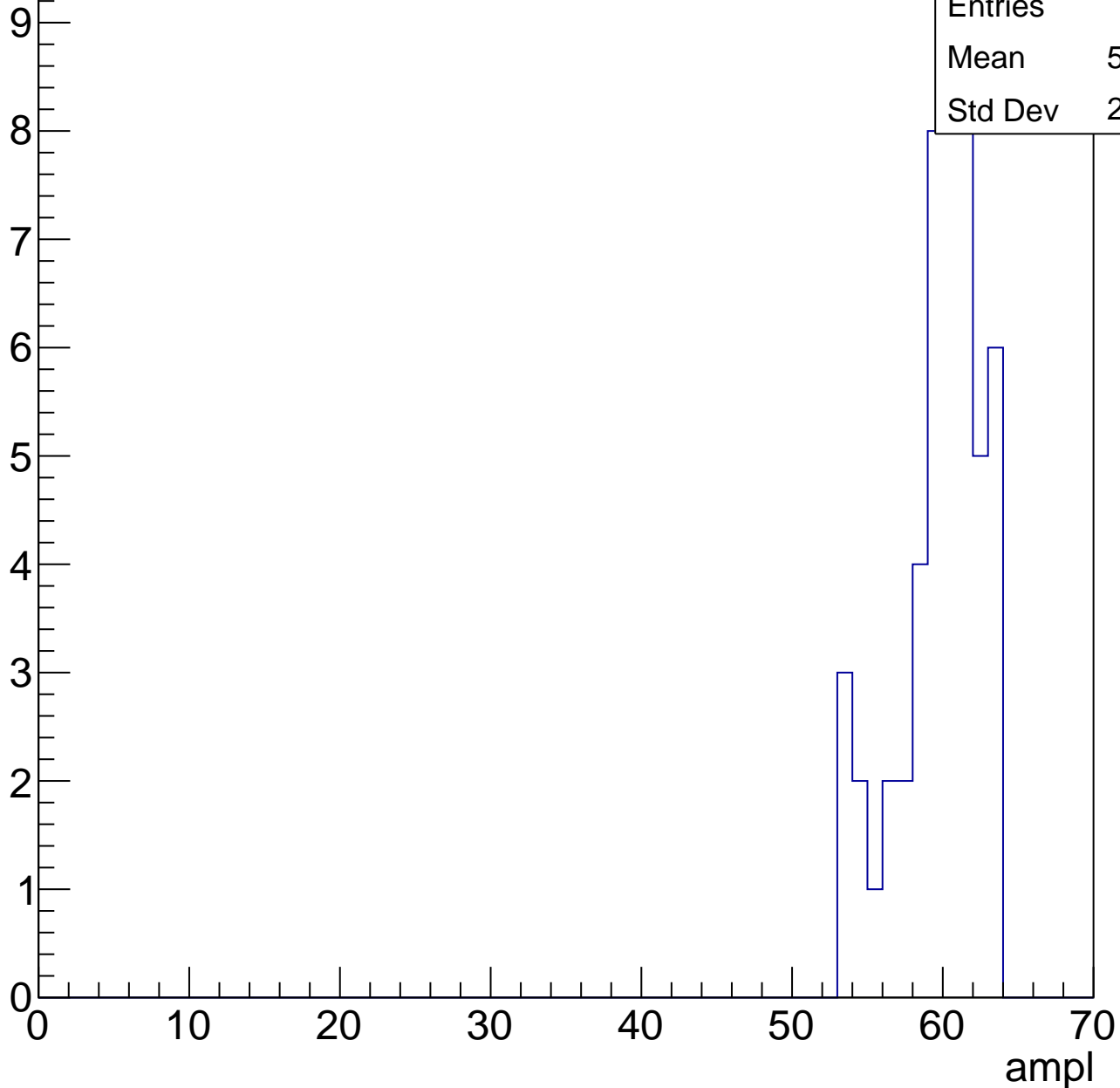
Entries	47
Mean	55.32
Std Dev	3.403



# B1L103S, U25-ch30, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

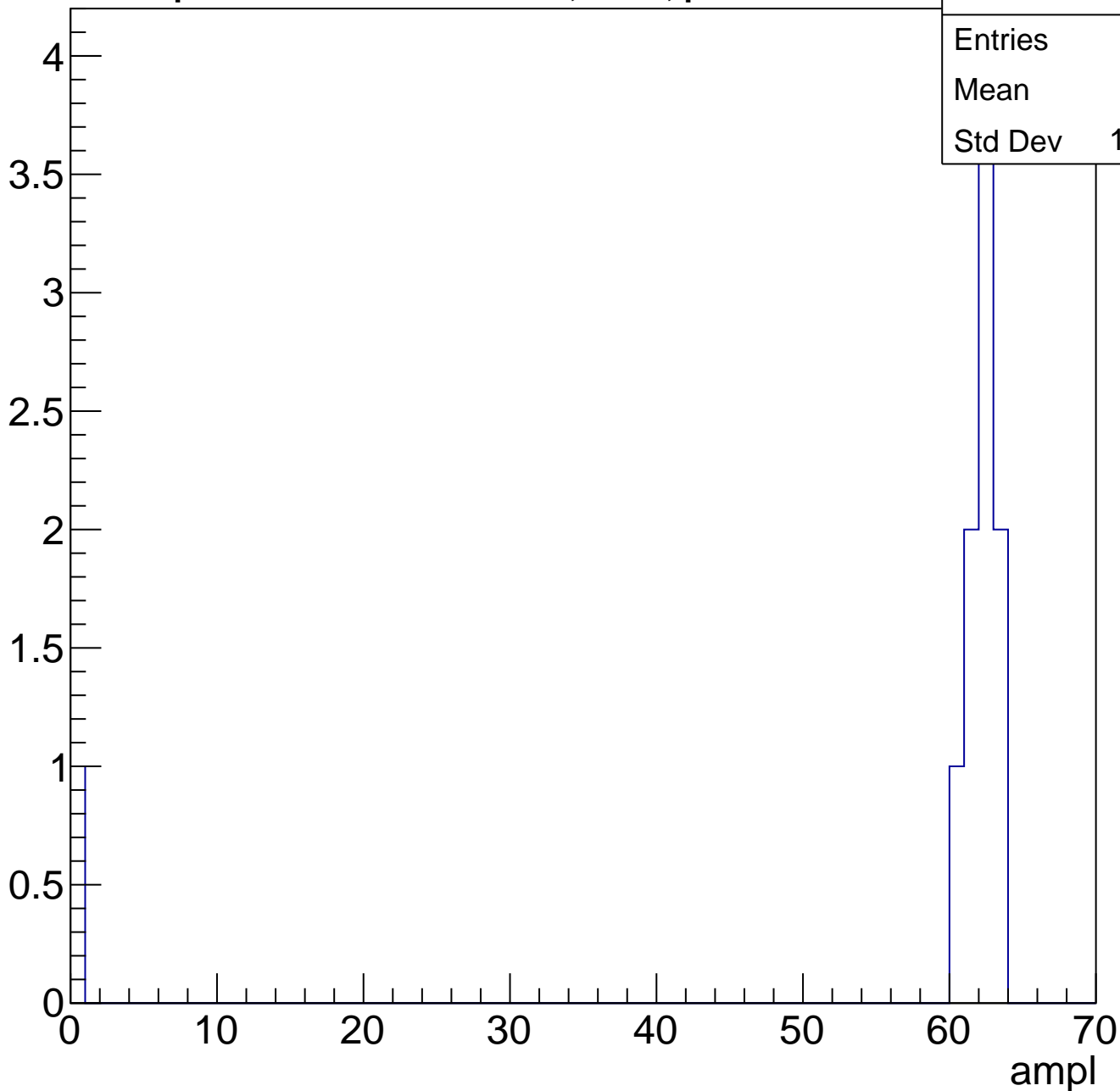
Entry



# B1L103S, U25-ch30, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U25-ch30, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U25-ch31, adc0

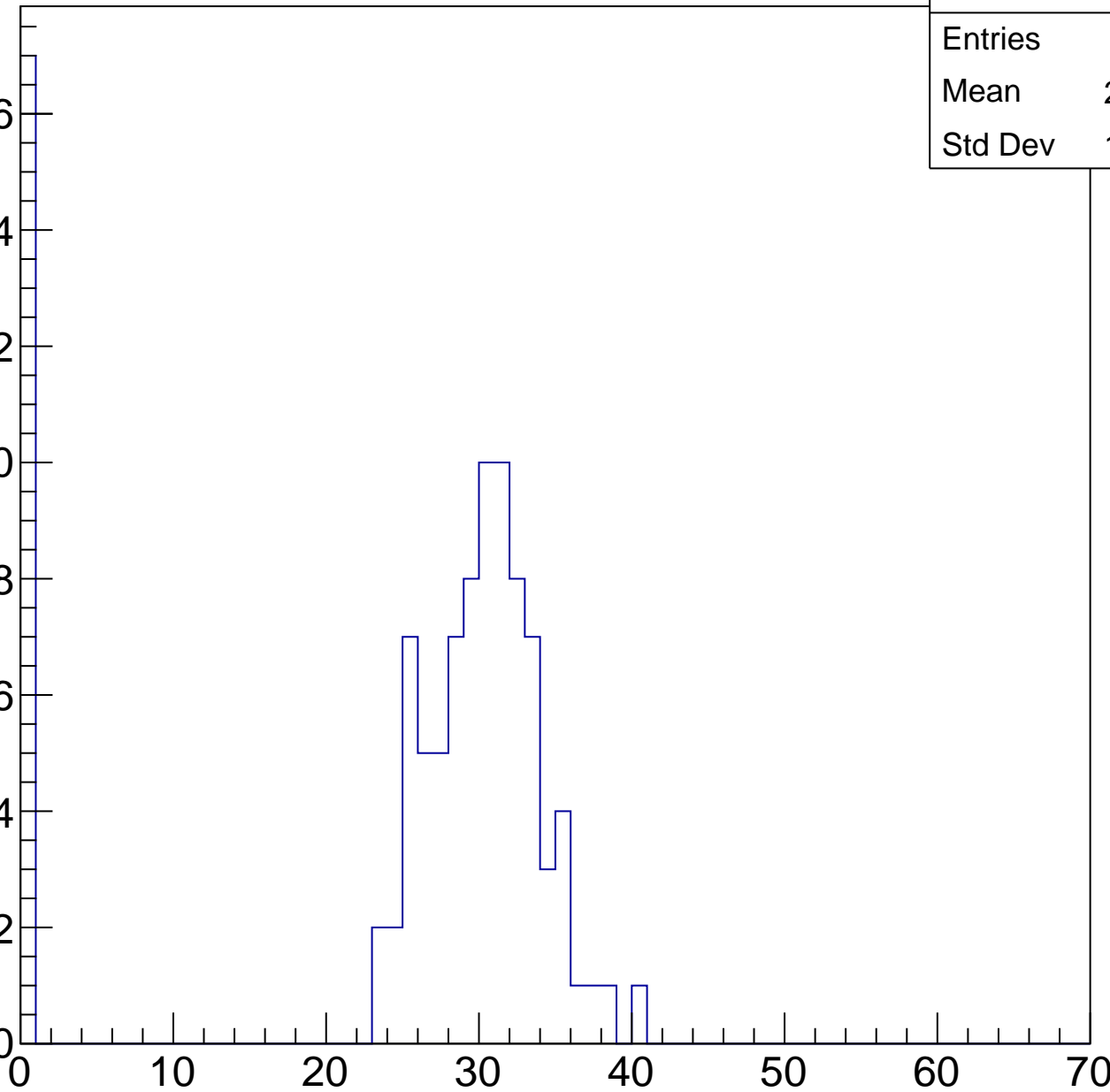
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	99
Mean	24.77
Std Dev	11.72

Entry

16  
14  
12  
10  
8  
6  
4  
2  
0

ampl

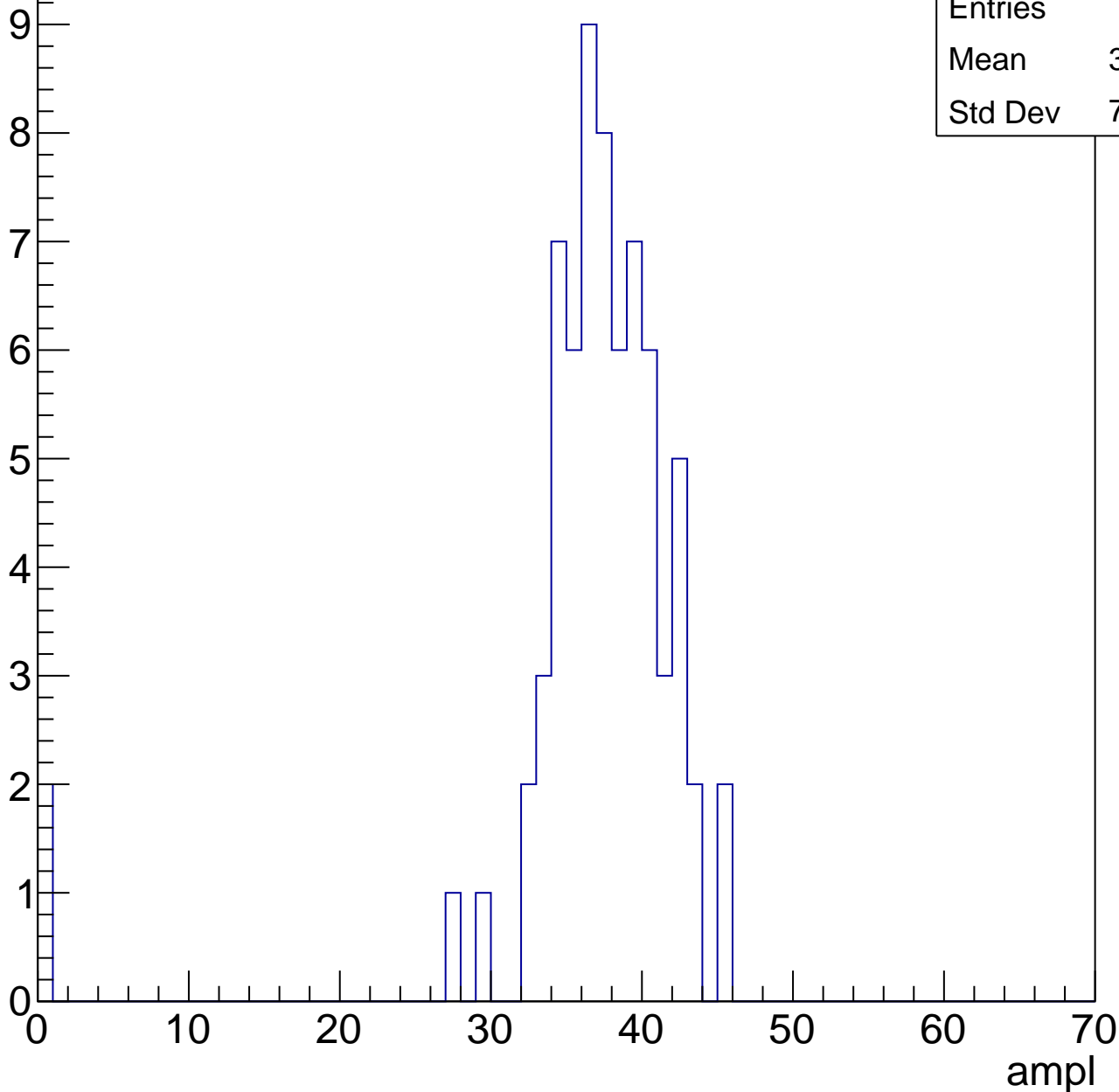


# B1L103S, U25-ch31, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	70
Mean	36.24
Std Dev	7.088



# B1L103S, U25-ch31, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

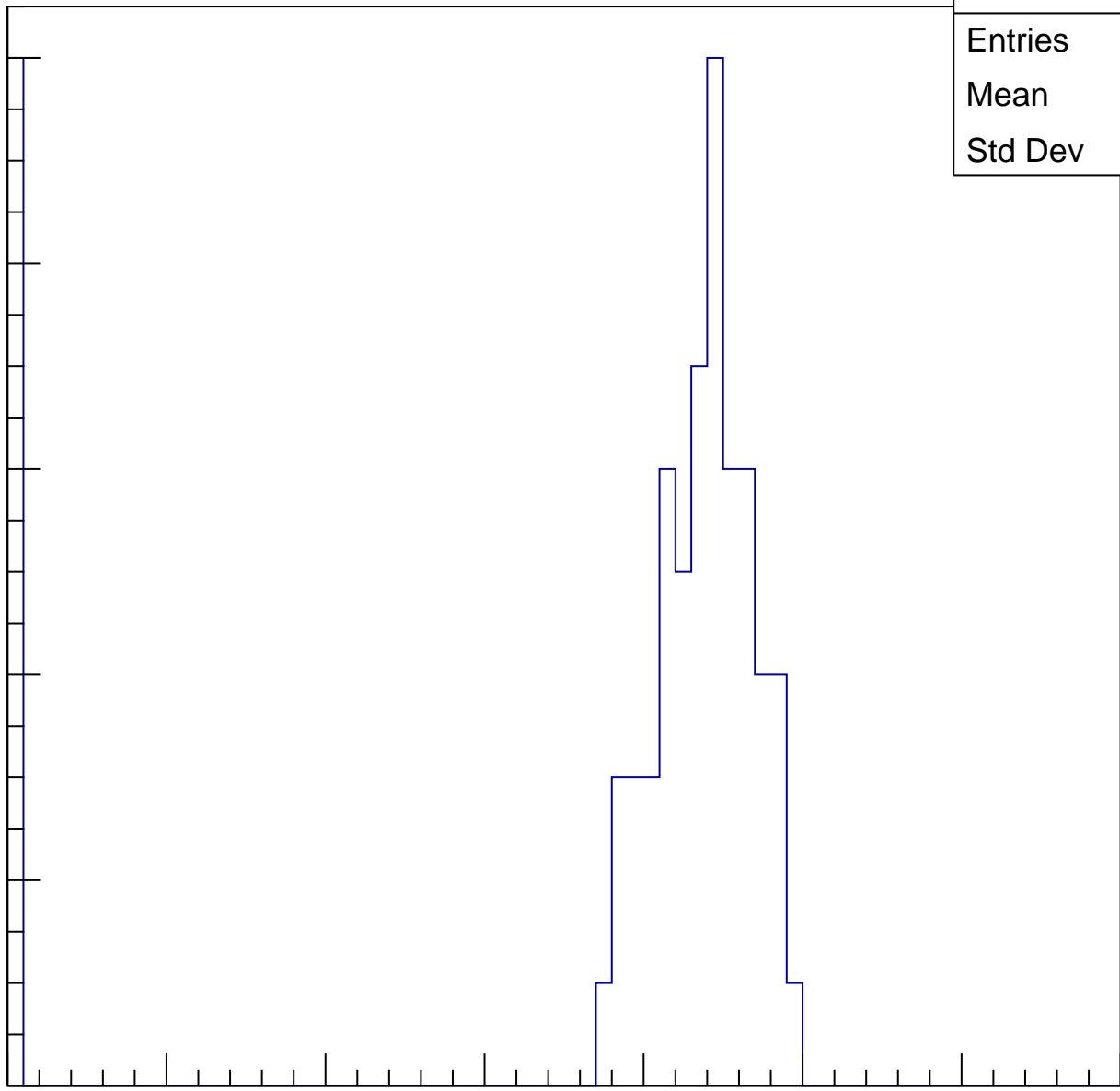
Entries	69
Mean	37.1
Std Dev	15.51

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L103S, U25-ch31, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	73
Mean	48.33
Std Dev	10.53

Entry

10

8

6

4

2

0

0

10

20

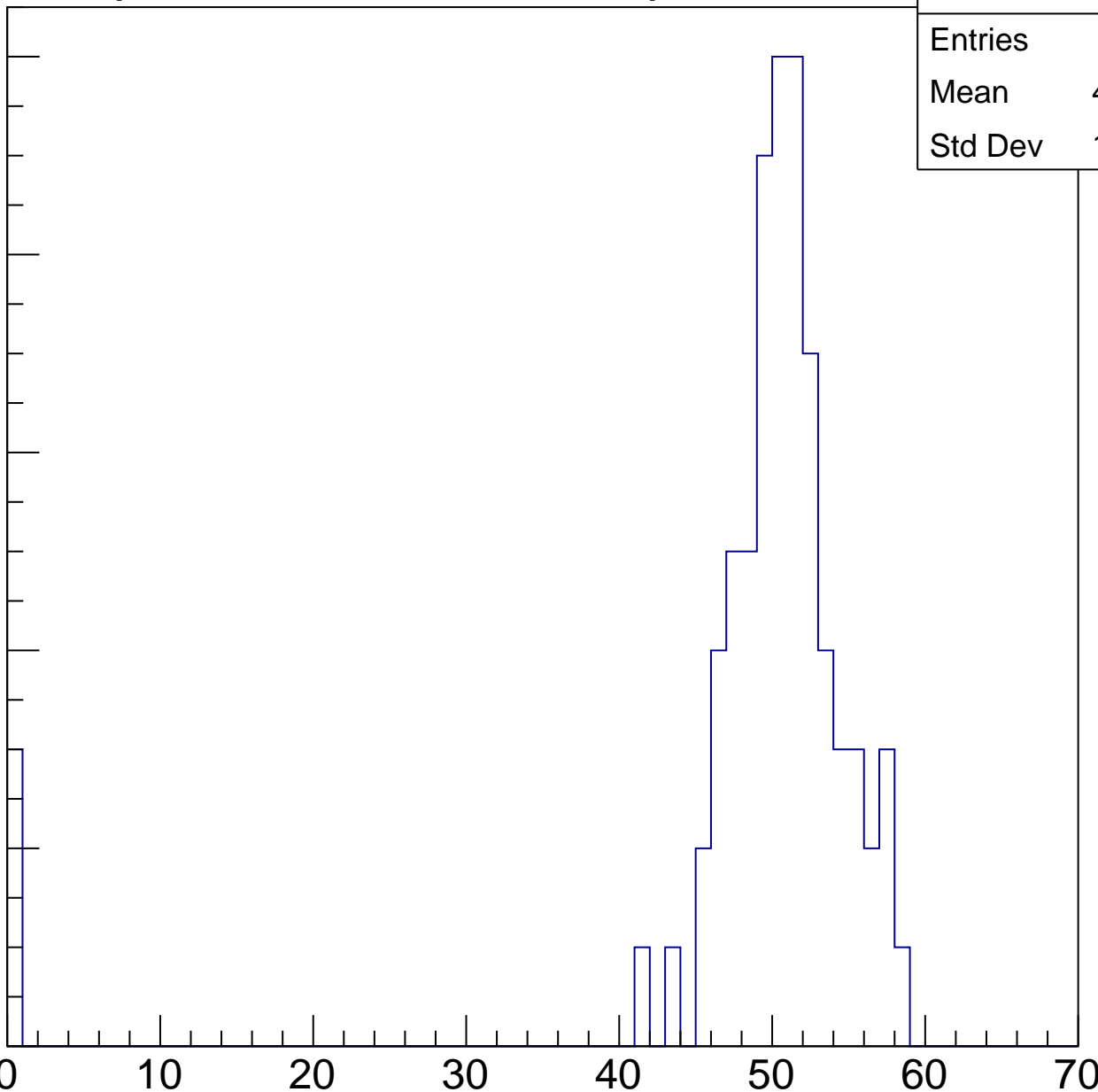
30

40

50

60

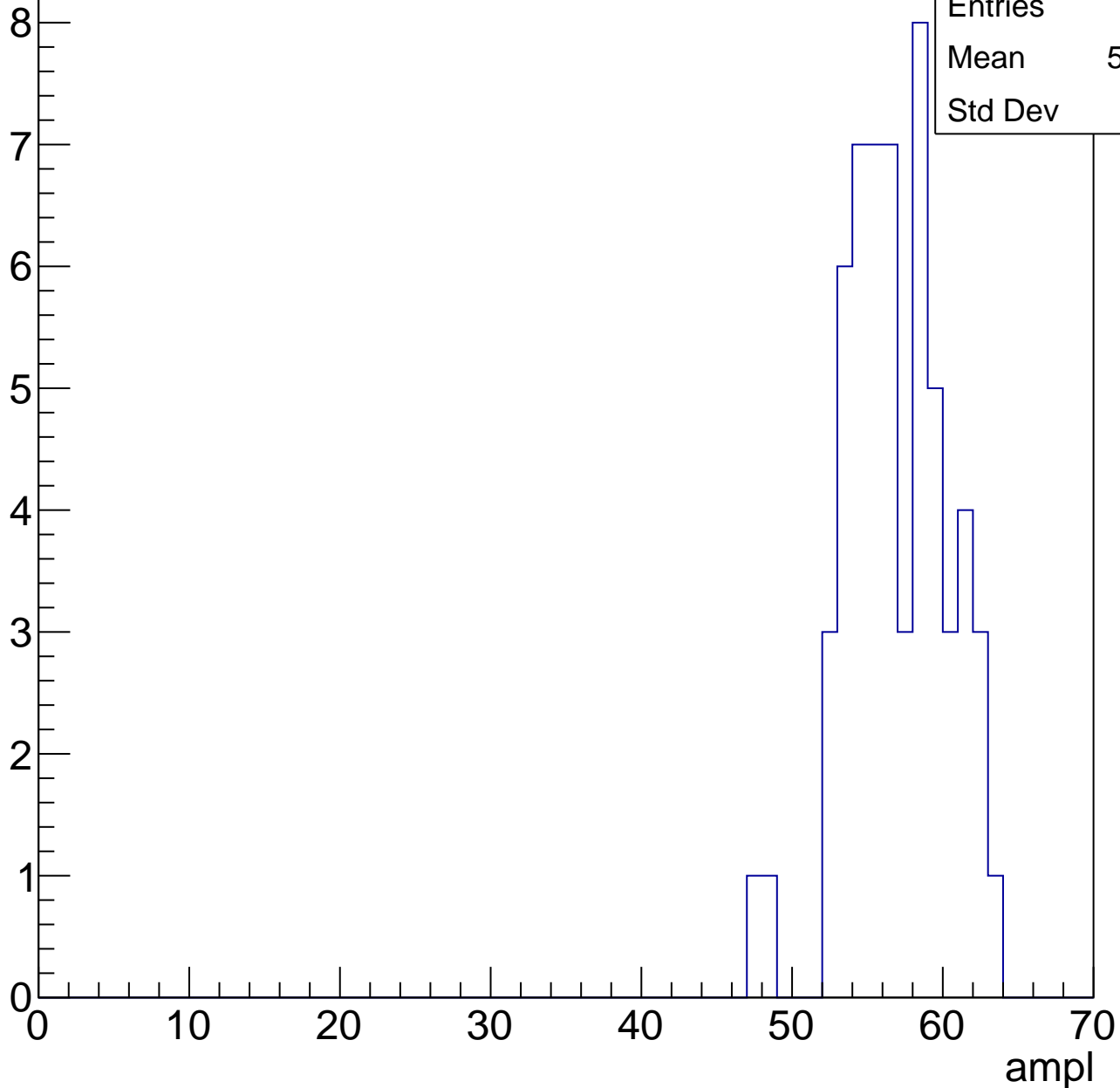
ampl



# B1L103S, U25-ch31, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U25-ch31, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

7

6

5

4

3

2

1

0

Entries	38
Mean	58.87
Std Dev	9.879

ampl

# B1L103S, U25-ch31, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U25-ch31, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

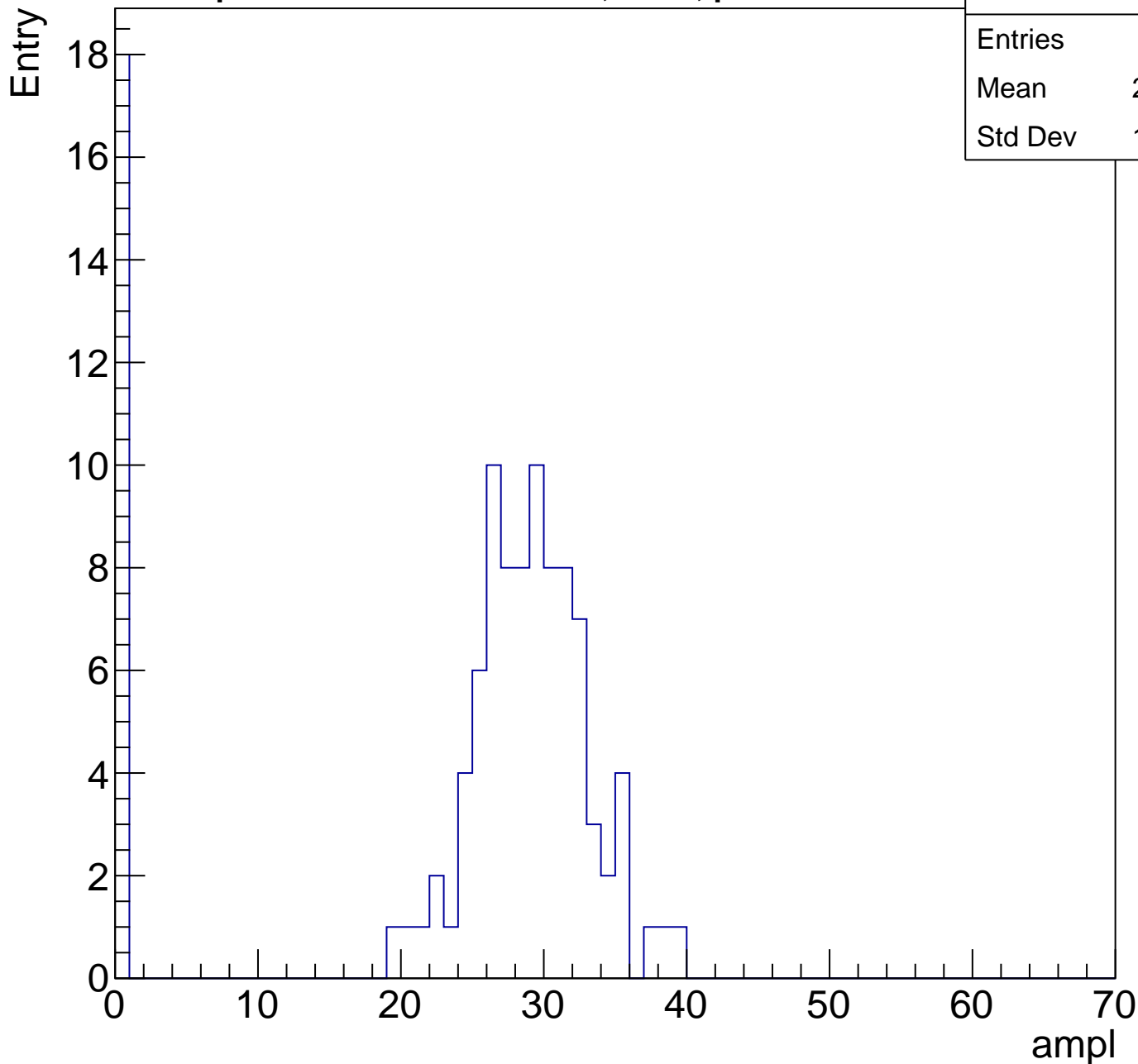
ampl

Entries	19
Mean	0
Std Dev	0

# B1L103S, U25-ch32, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	105
Mean	23.77
Std Dev	11.37

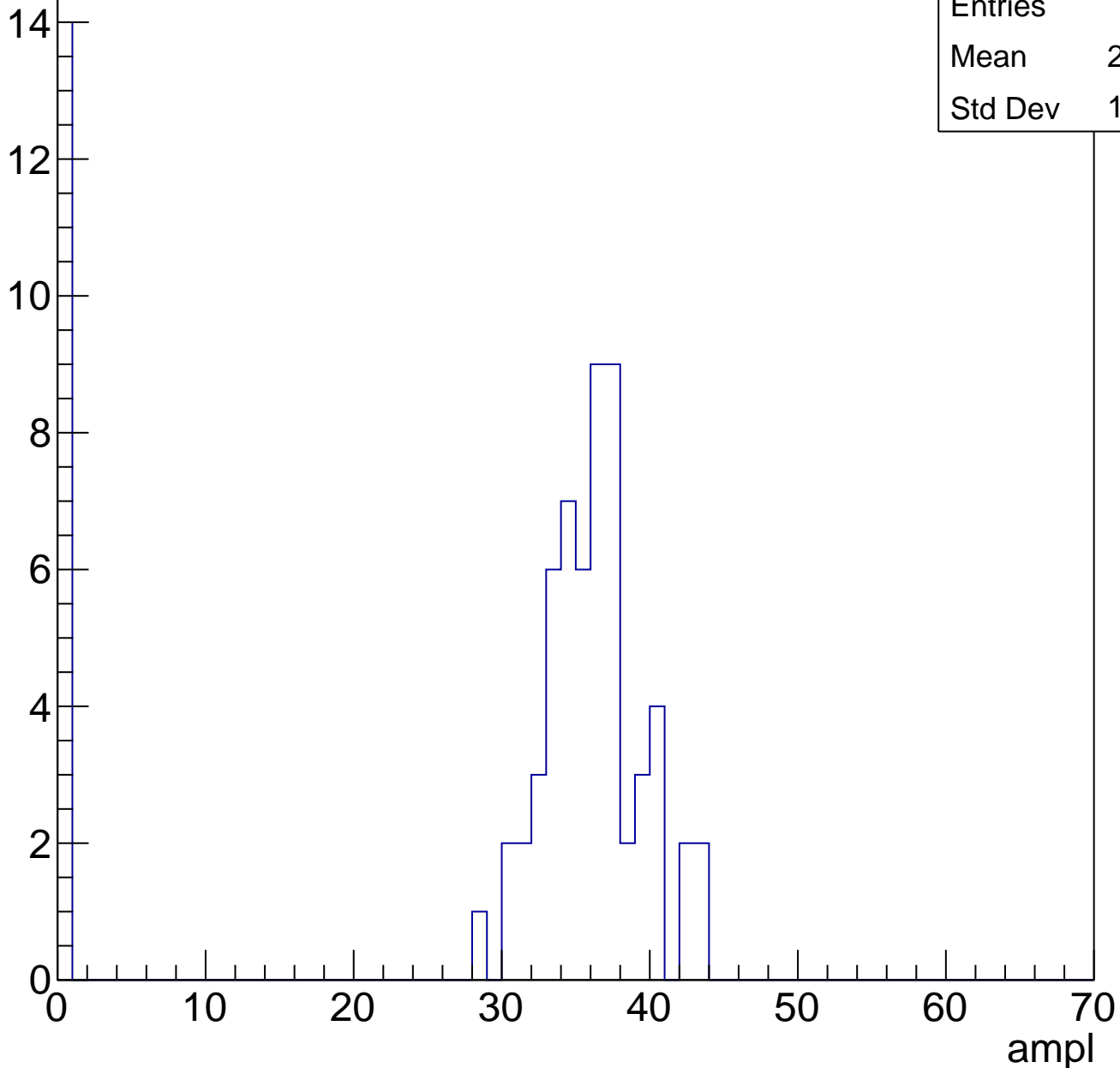


# B1L103S, U25-ch32, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	72
Mean	28.78
Std Dev	14.43

Entry

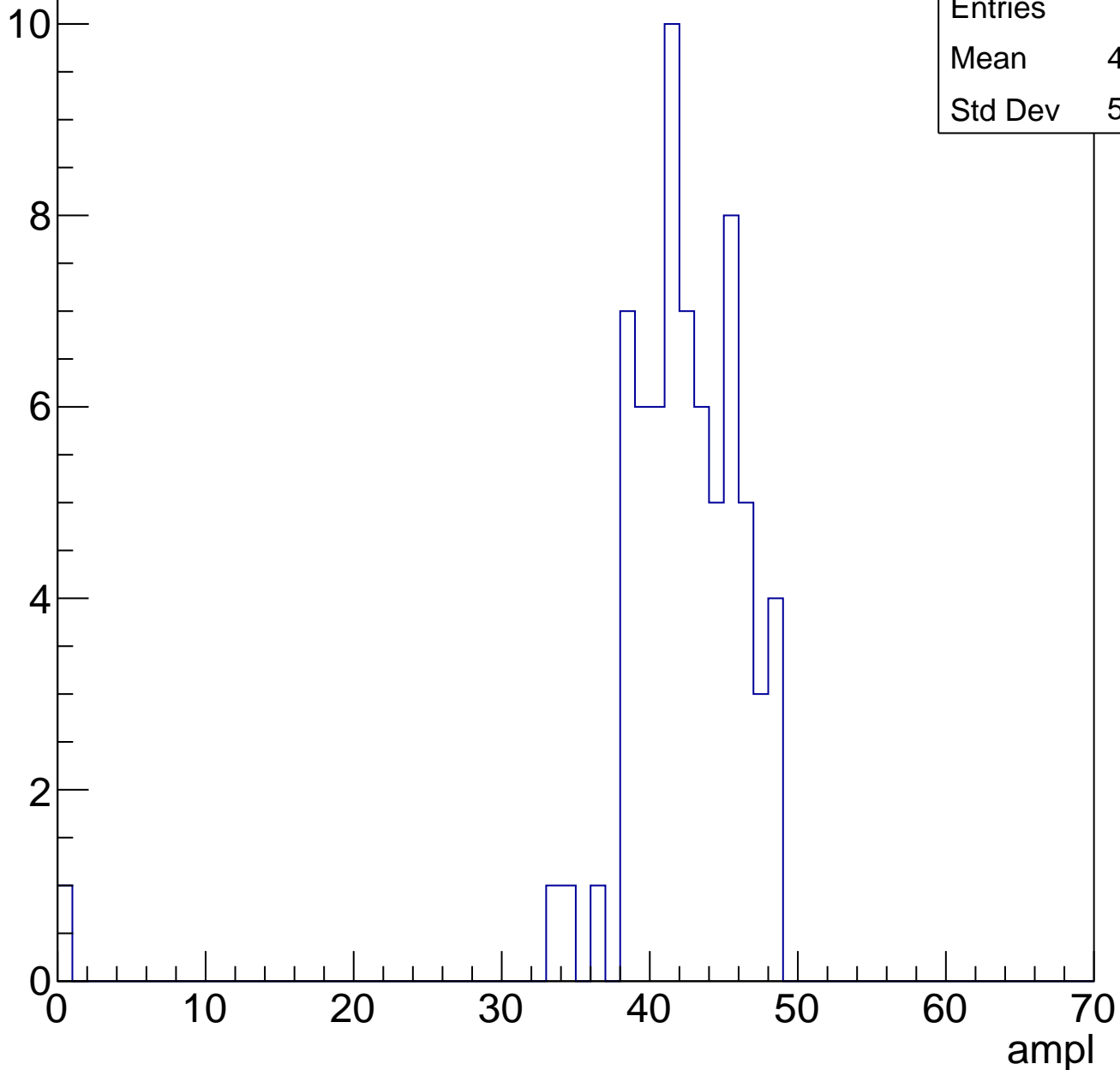


# B1L103S, U25-ch32, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	71
Mean	41.52
Std Dev	5.964

Entry

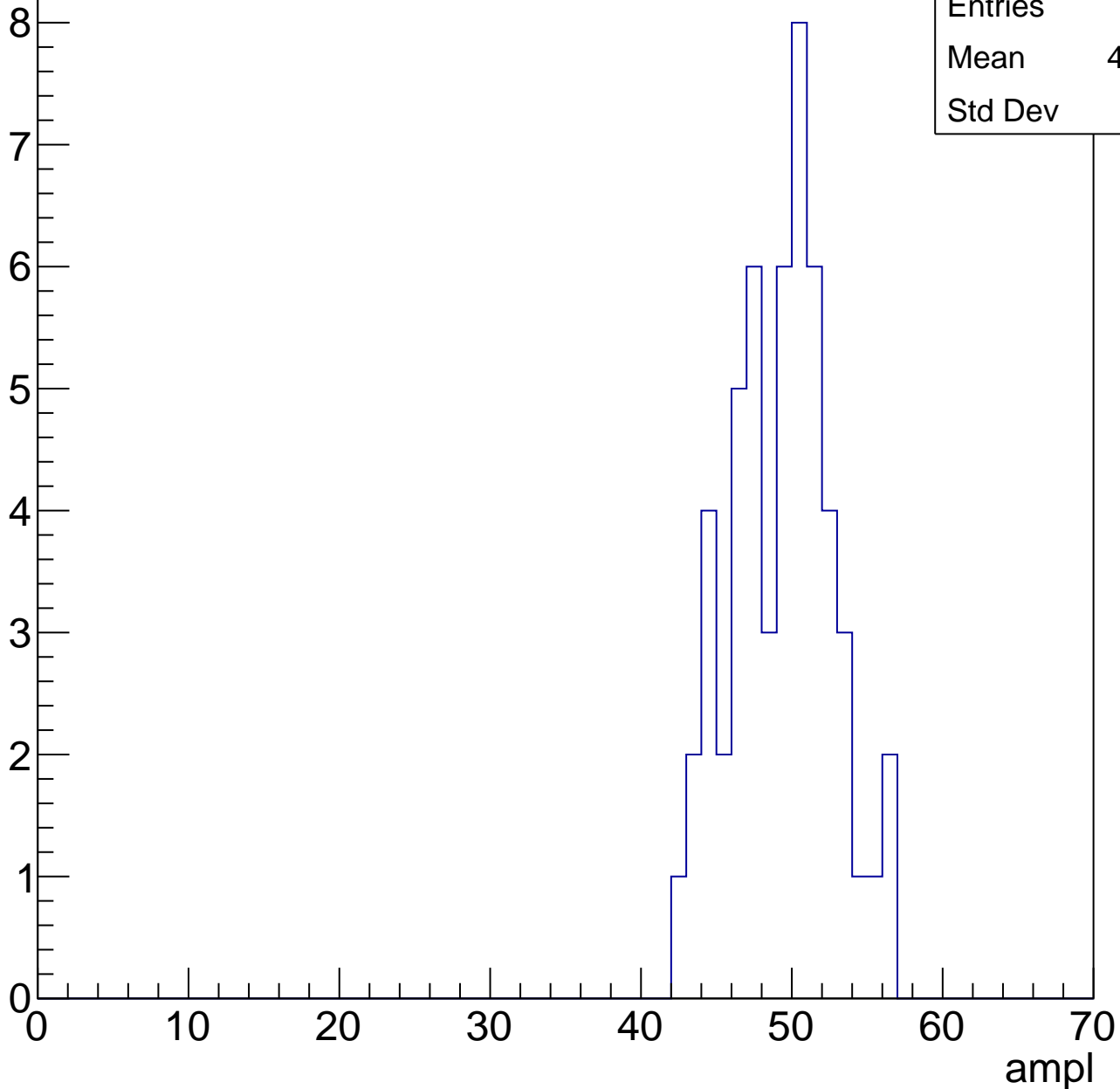


# B1L103S, U25-ch32, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	54
Mean	48.85
Std Dev	3.33

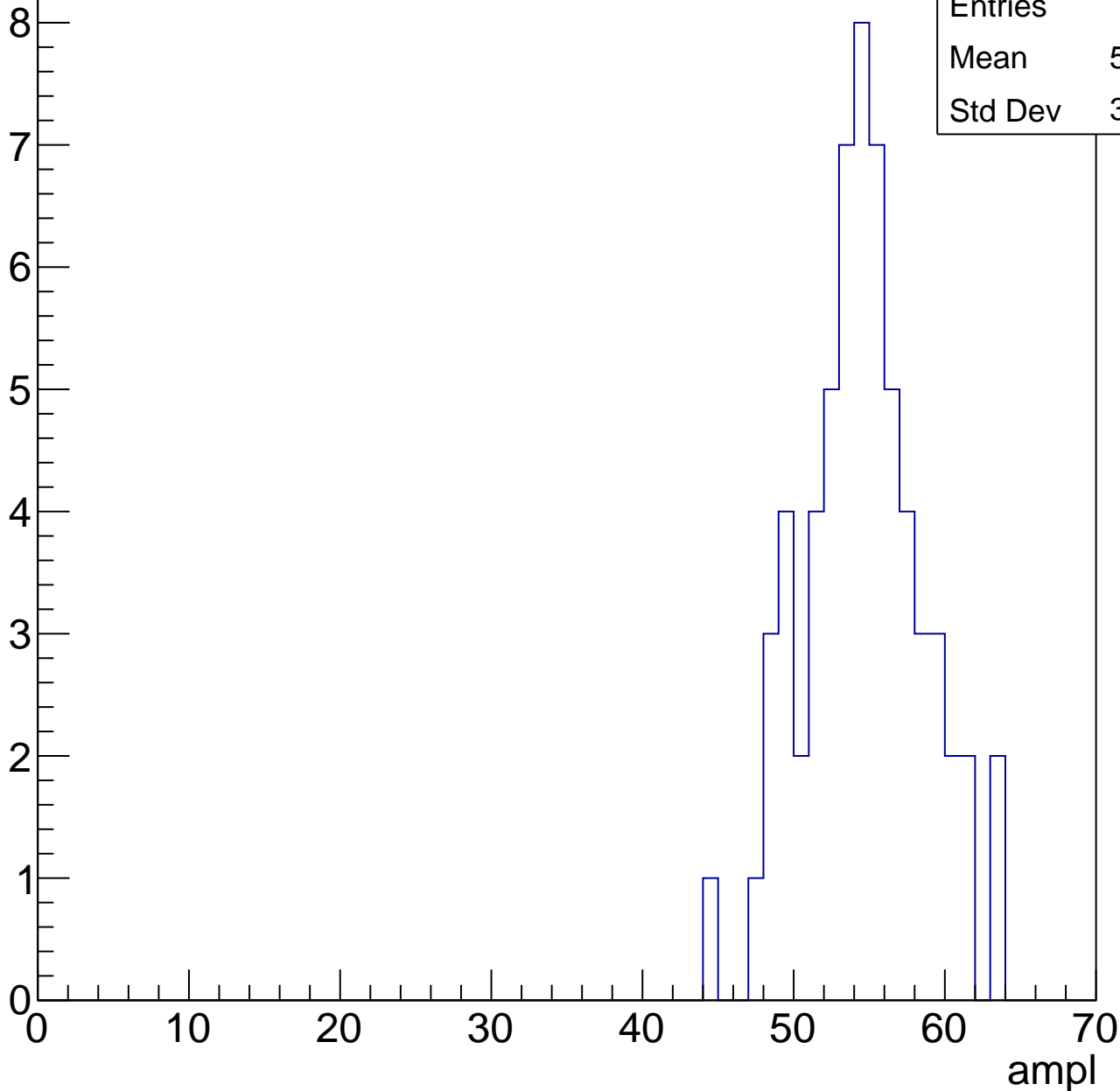


# B1L103S, U25-ch32, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	63
Mean	54.13
Std Dev	3.922



# B1L103S, U25-ch32, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

7

6

5

4

3

2

1

0

Entries 50

Mean 57.9

Std Dev 8.645

ampl

0

10

20

30

40

50

60

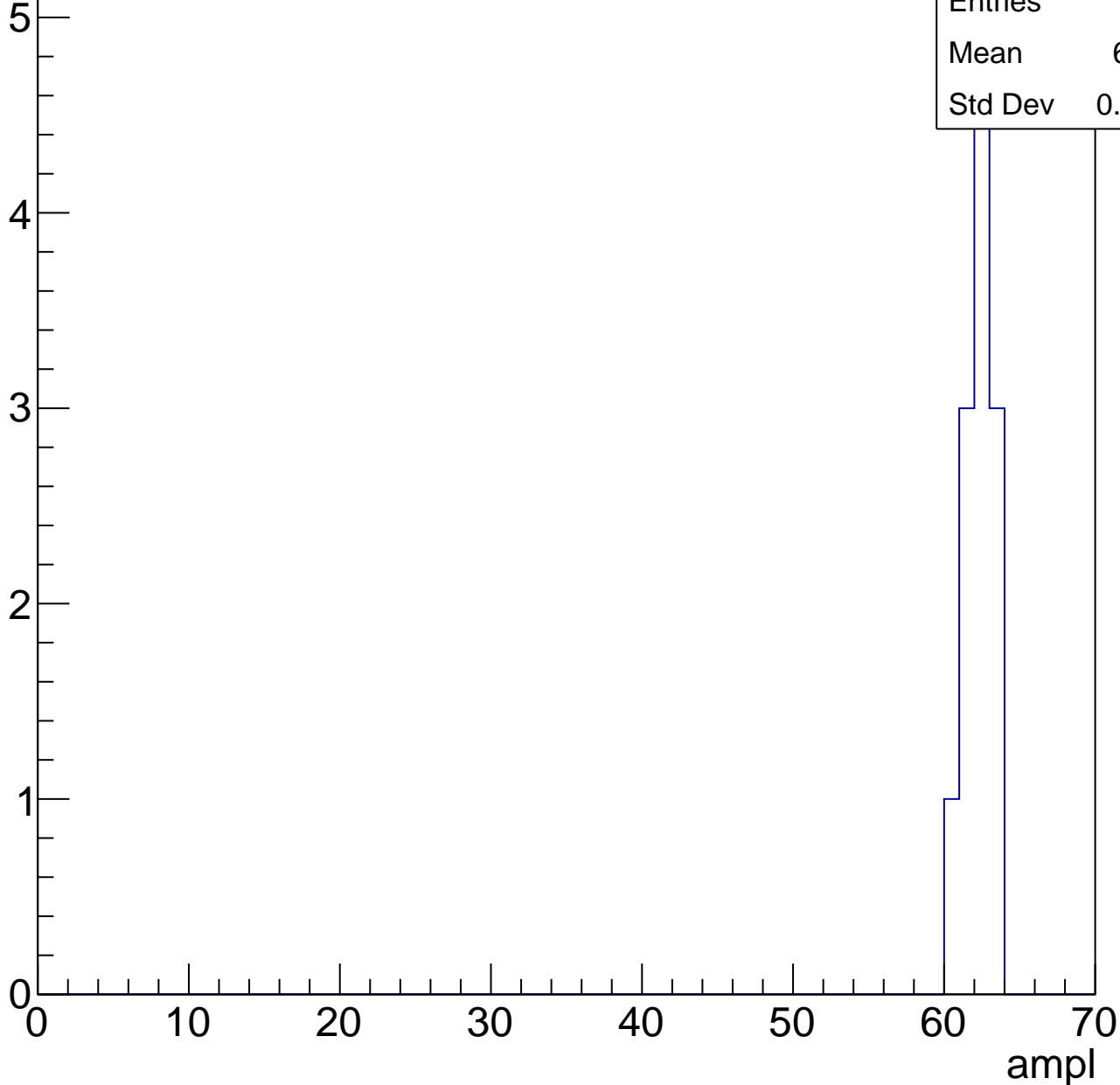
70

# B1L103S, U25-ch32, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	12
Mean	61.83
Std Dev	0.8975





# B1L103S, U25-ch32, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

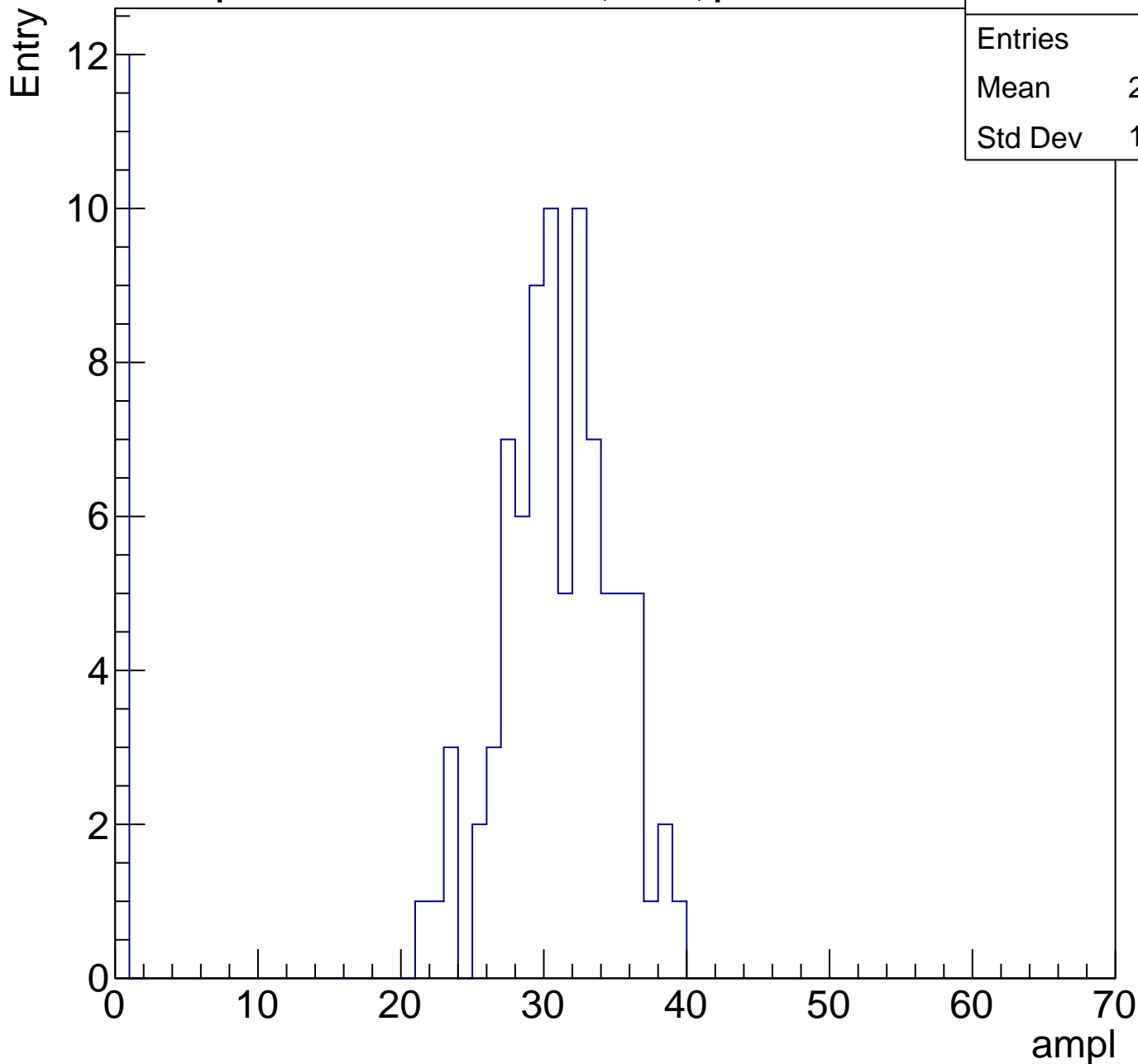
Entry



# B1L103S, U25-ch33, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	95
Mean	26.75
Std Dev	10.78

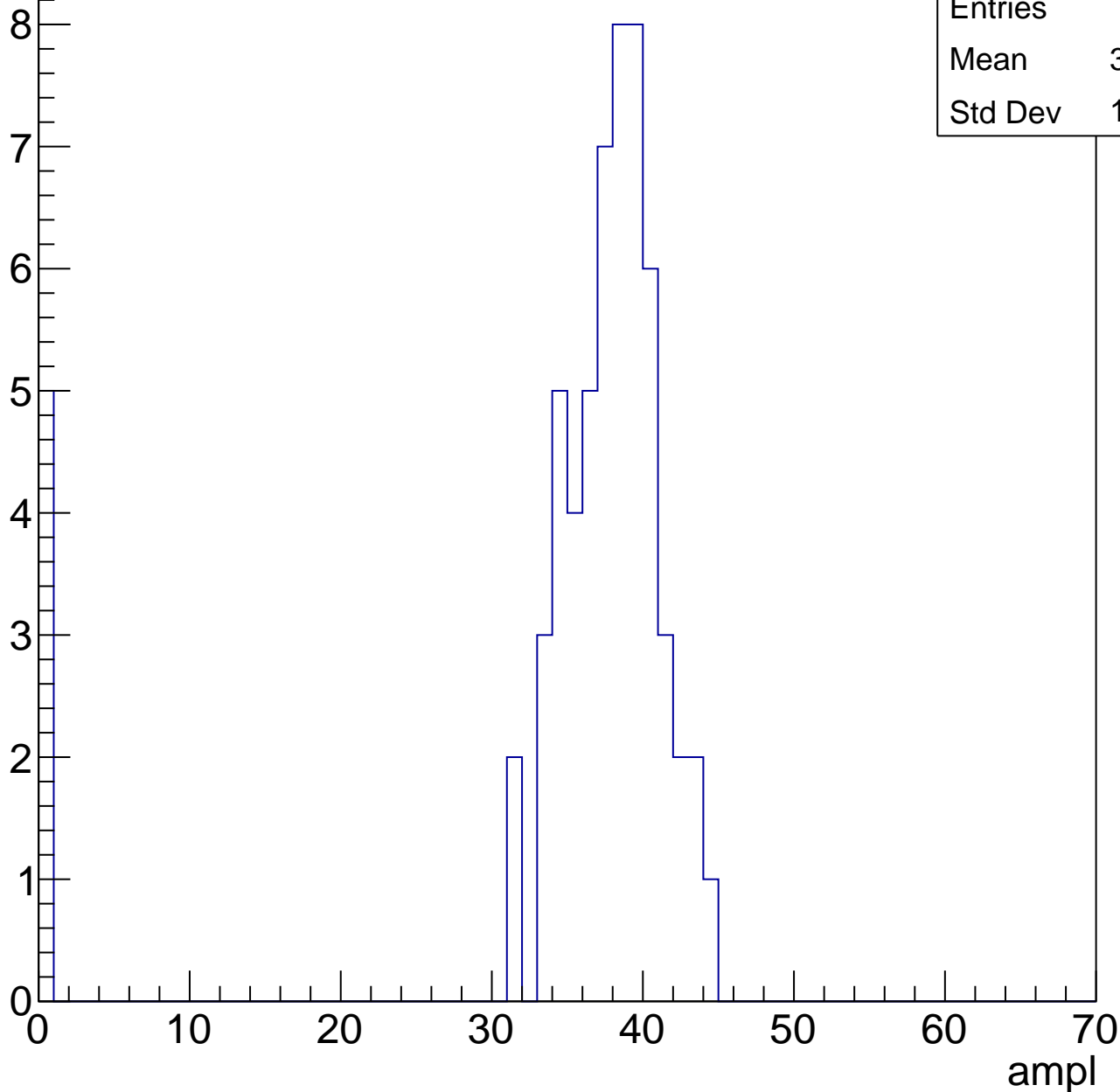


# B1L103S, U25-ch33, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	61
Mean	34.48
Std Dev	10.68

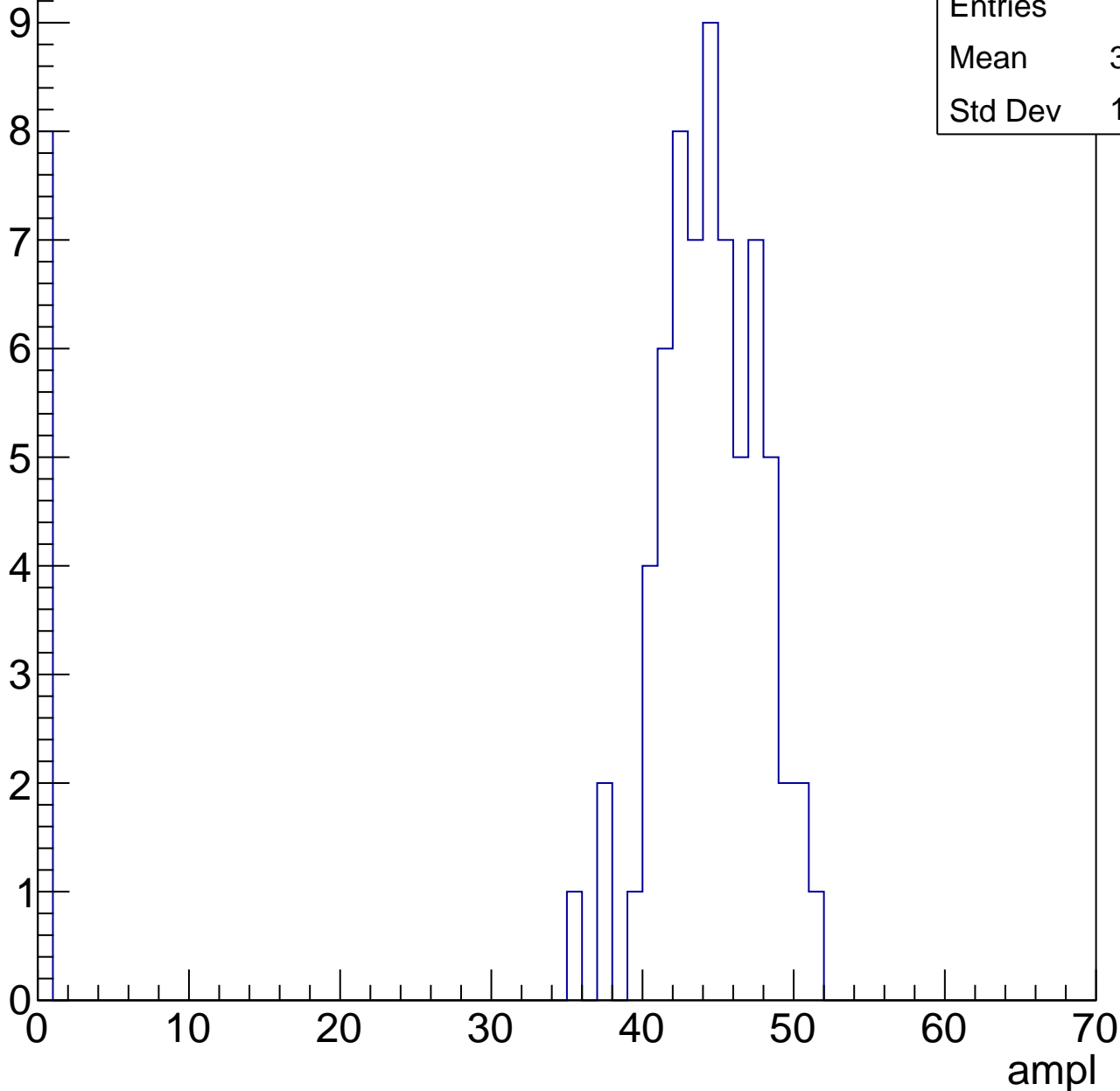


# B1L103S, U25-ch33, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	75
Mean	39.33
Std Dev	13.93

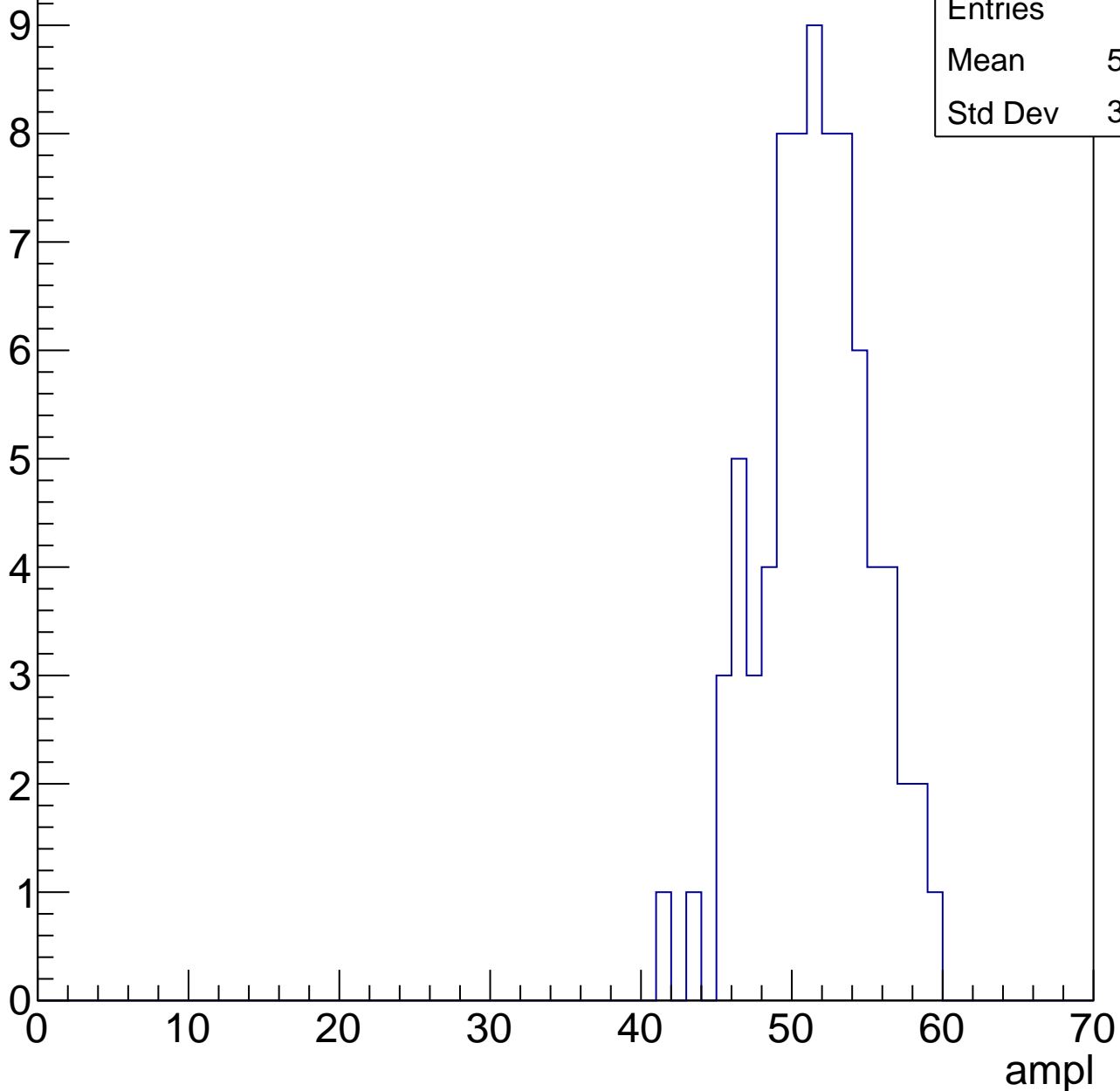


# B1L103S, U25-ch33, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	77
Mean	51.04
Std Dev	3.627

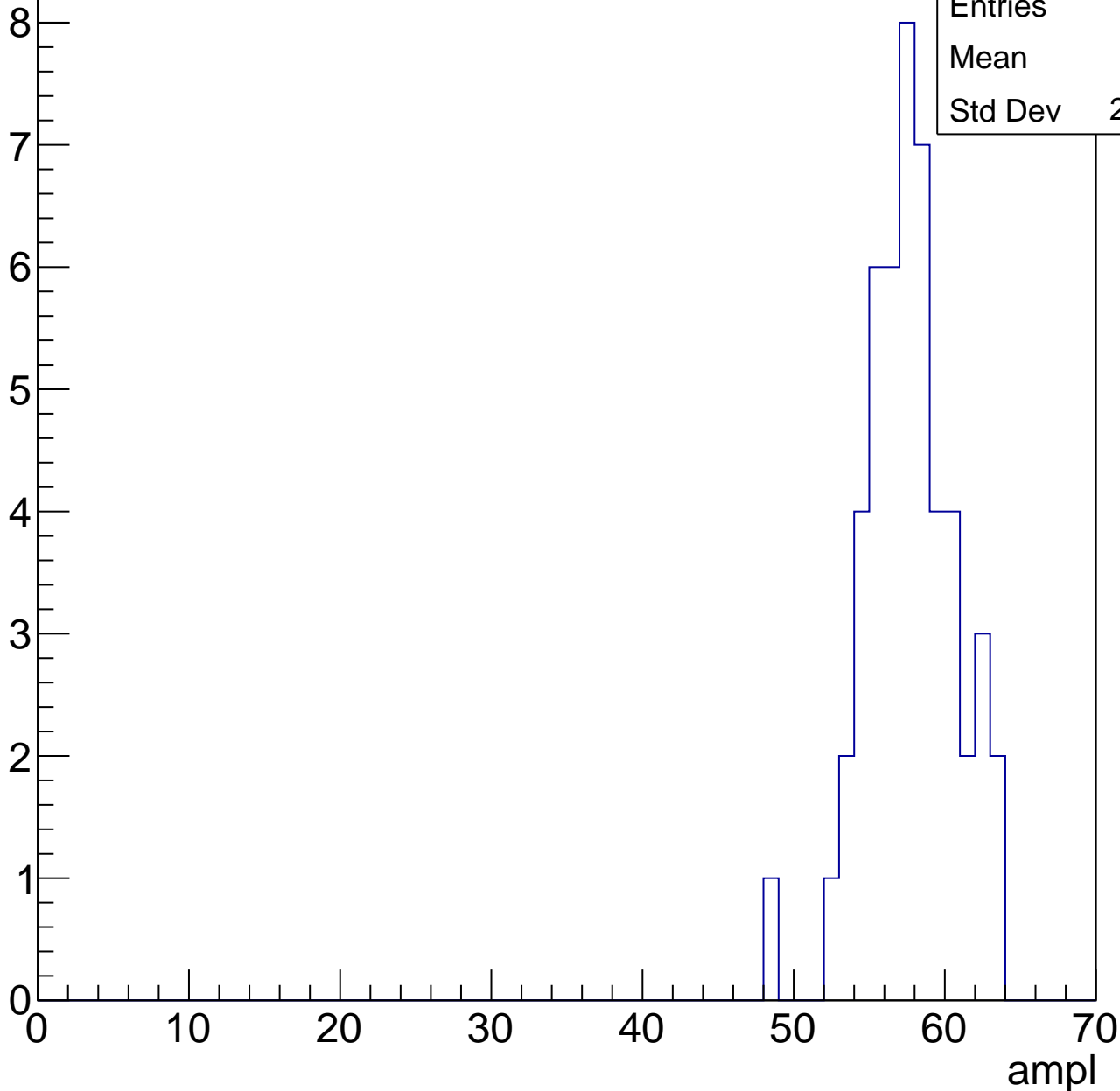


# B1L103S, U25-ch33, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	50
Mean	57.2
Std Dev	2.966

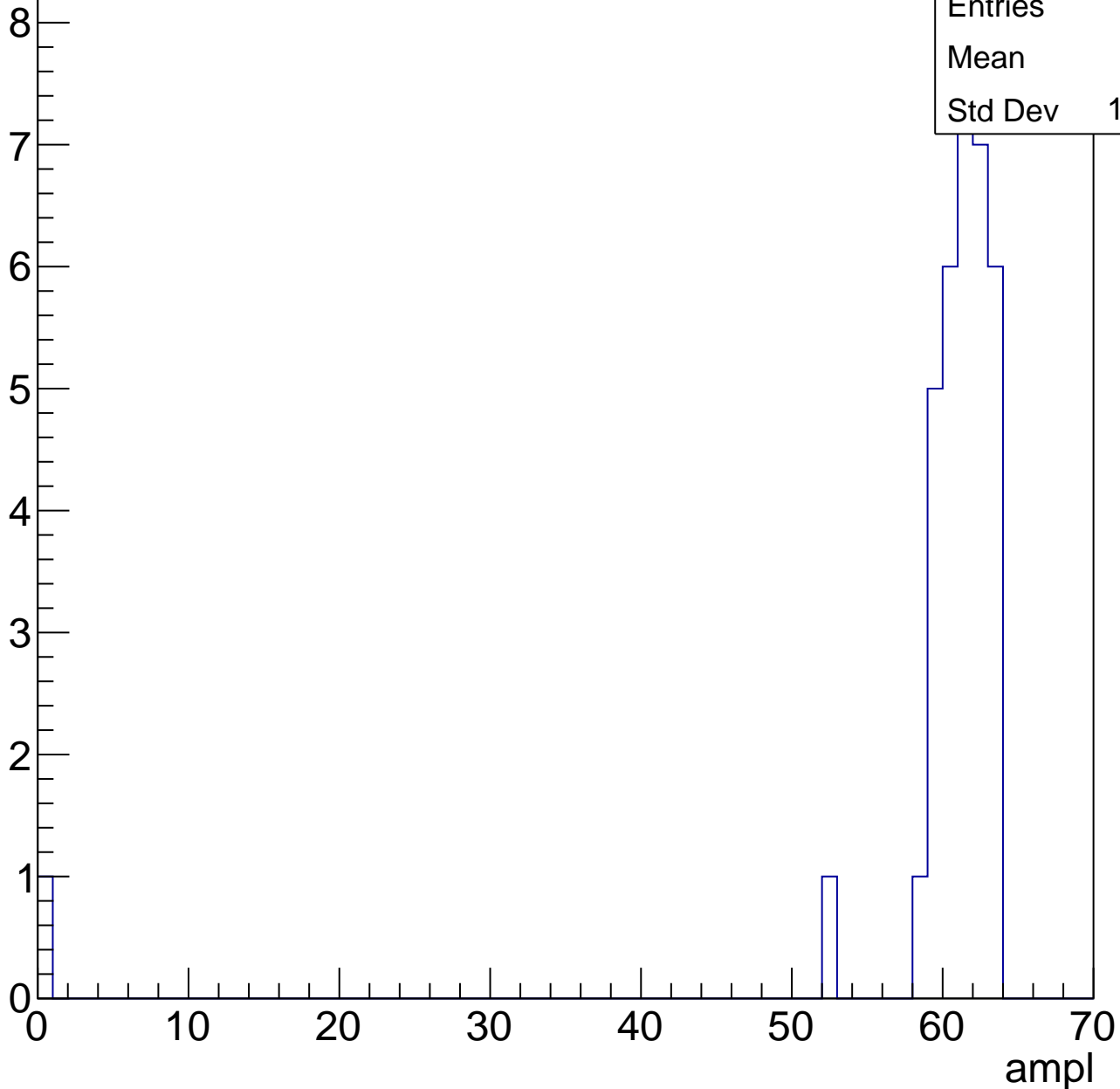


# B1L103S, U25-ch33, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	35
Mean	59
Std Dev	10.32



# B1L103S, U25-ch33, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	63
Std Dev	0

0 10 20 30 40 50 60 70

ampl



# B1L103S, U25-ch33, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

# B1L103S, U25-ch34, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

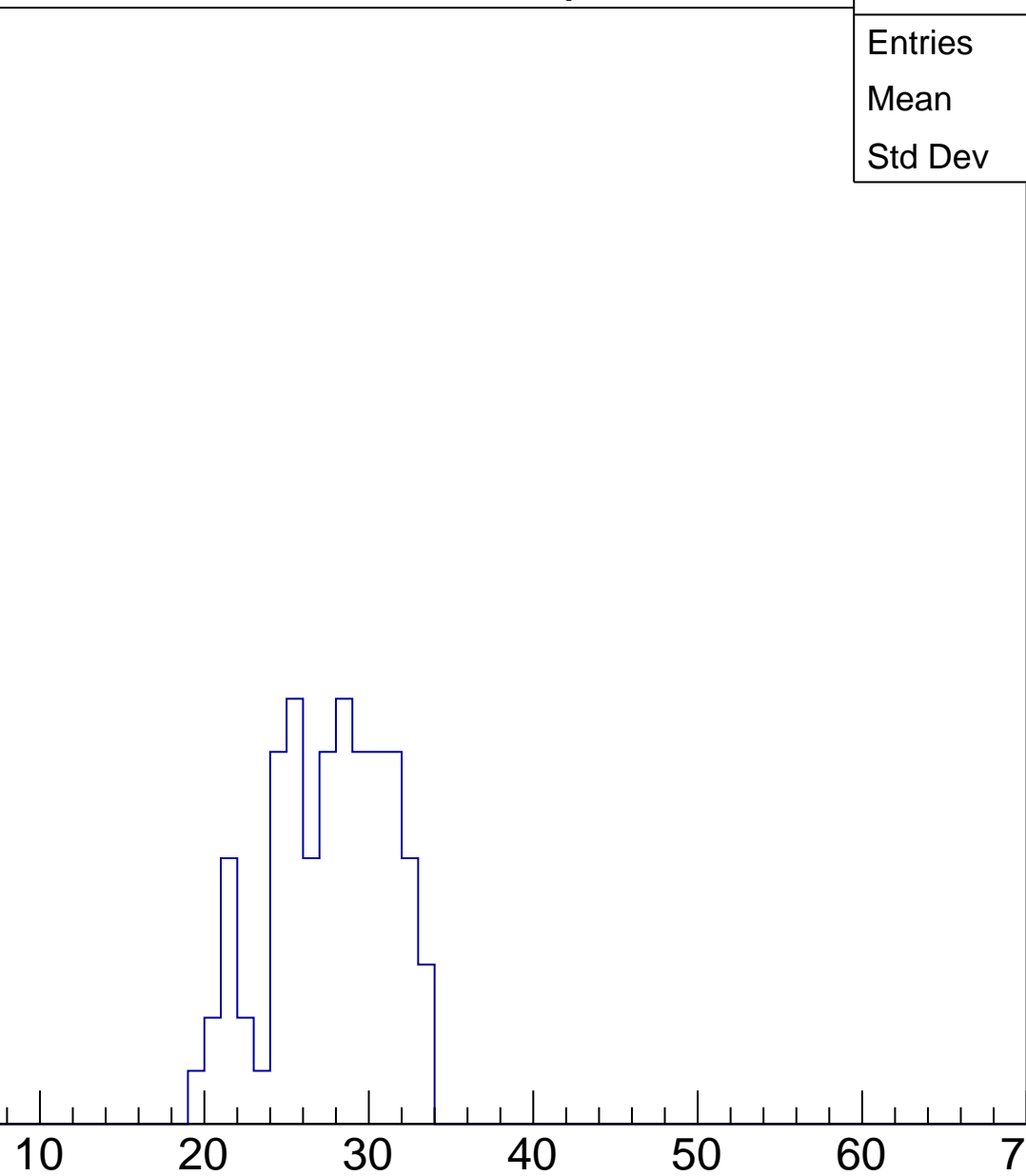
Entries	95
Mean	21.38
Std Dev	11.48

Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

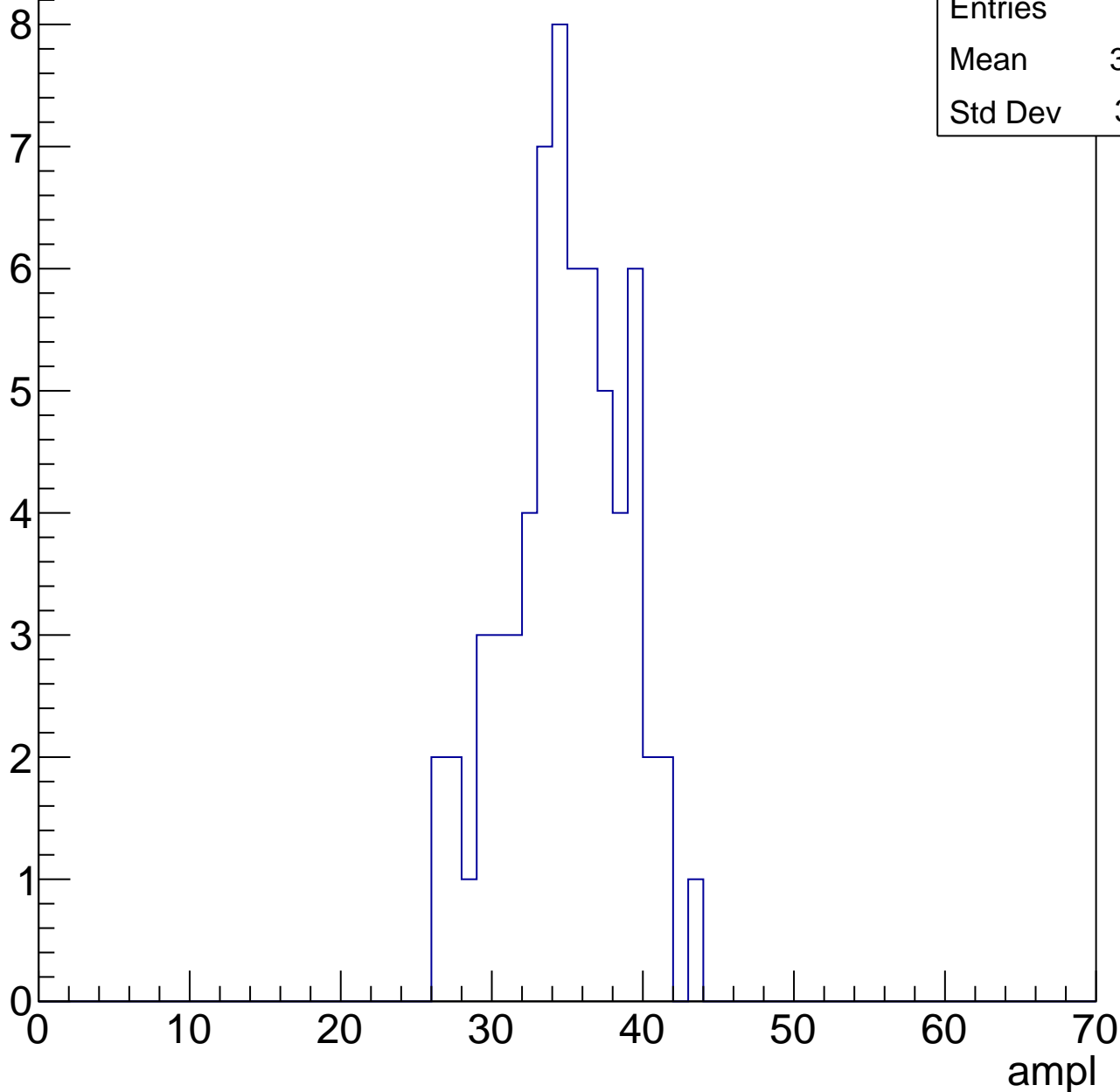


# B1L103S, U25-ch34, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	65
Mean	34.42
Std Dev	3.851

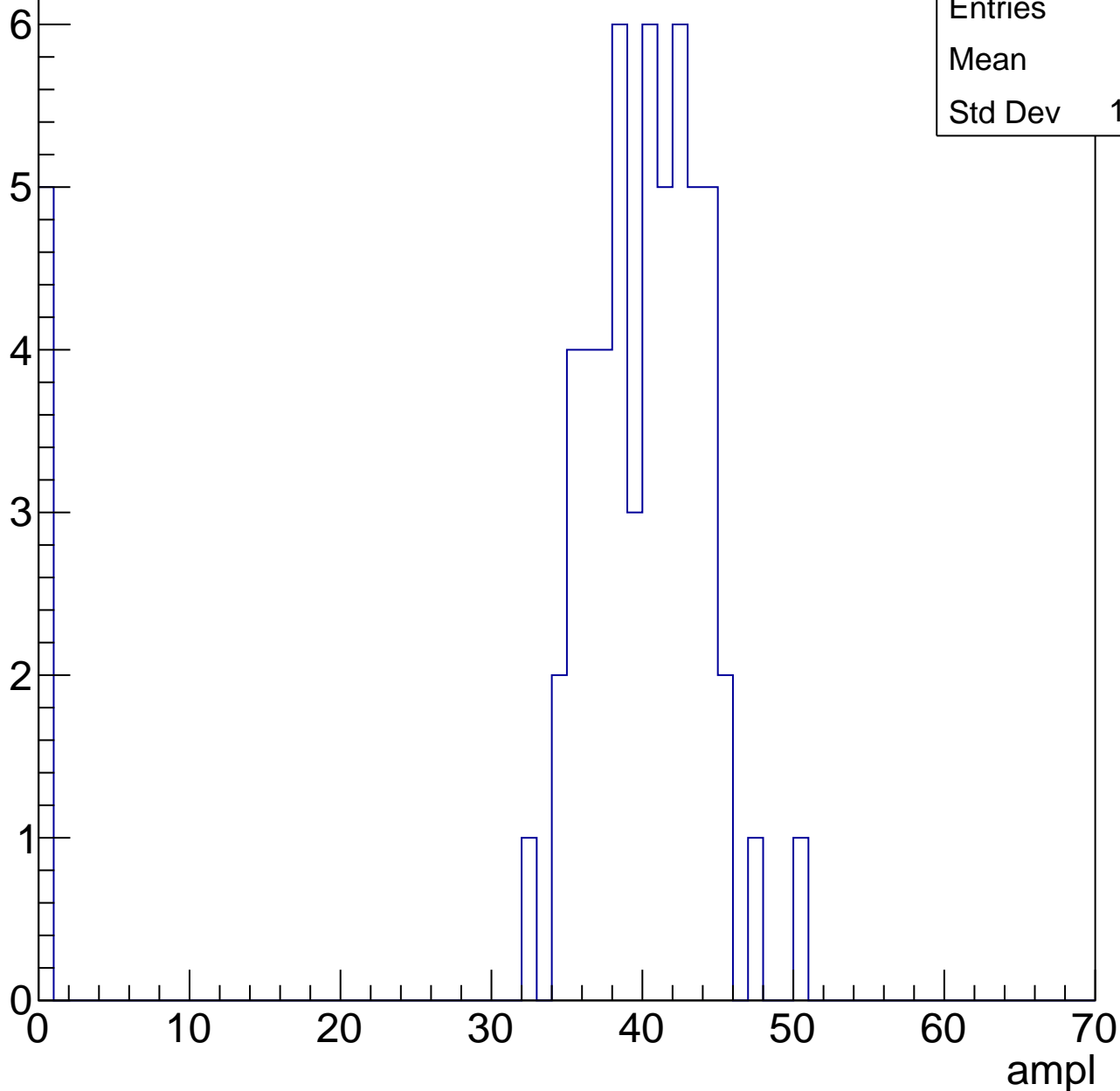


# B1L103S, U25-ch34, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	60
Mean	36.6
Std Dev	11.56



# B1L103S, U25-ch34, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	78
Mean	39.49
Std Dev	16.3

Entry

10

8

6

4

2

0

0

10

20

30

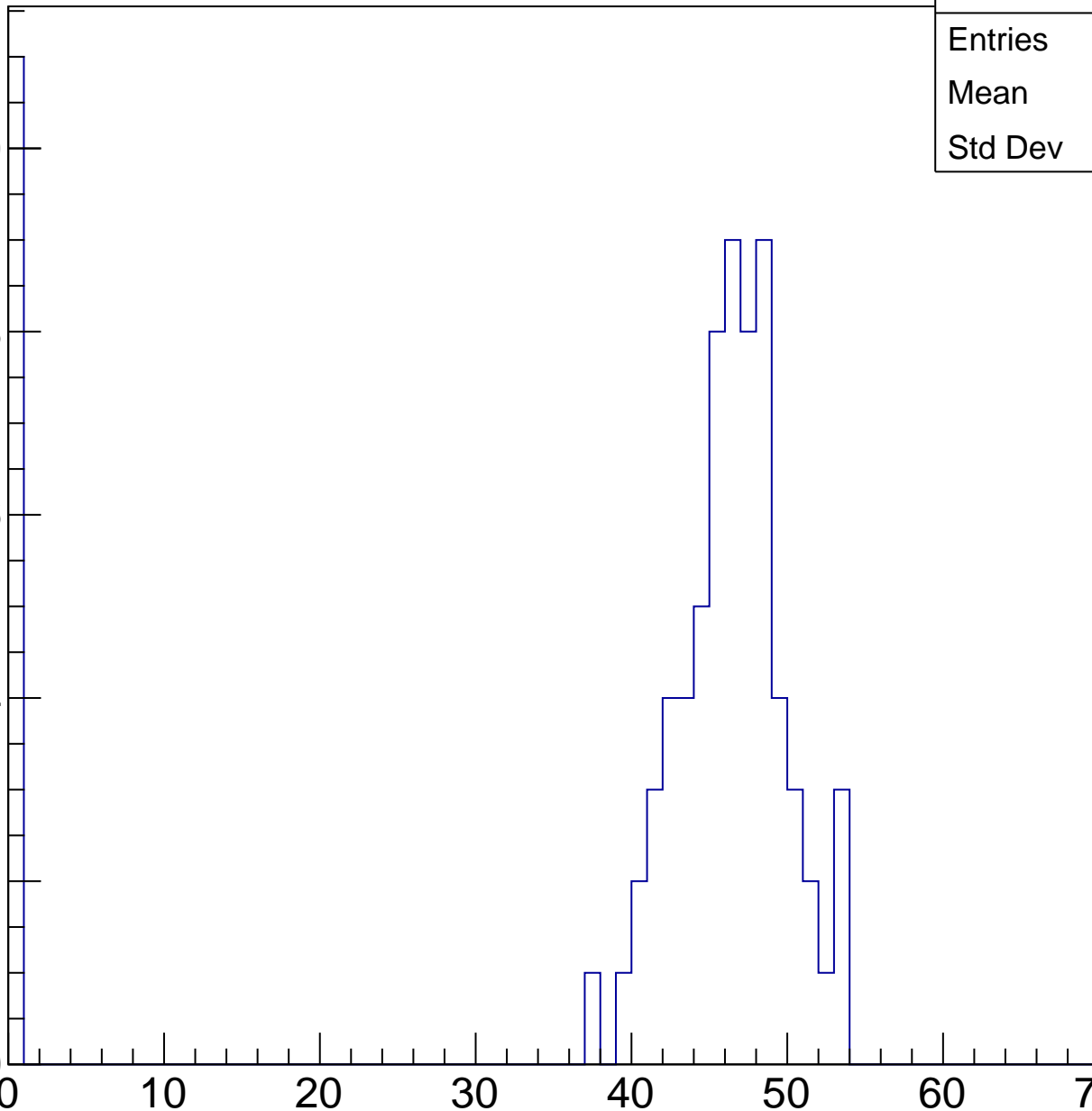
40

50

60

70

ampl

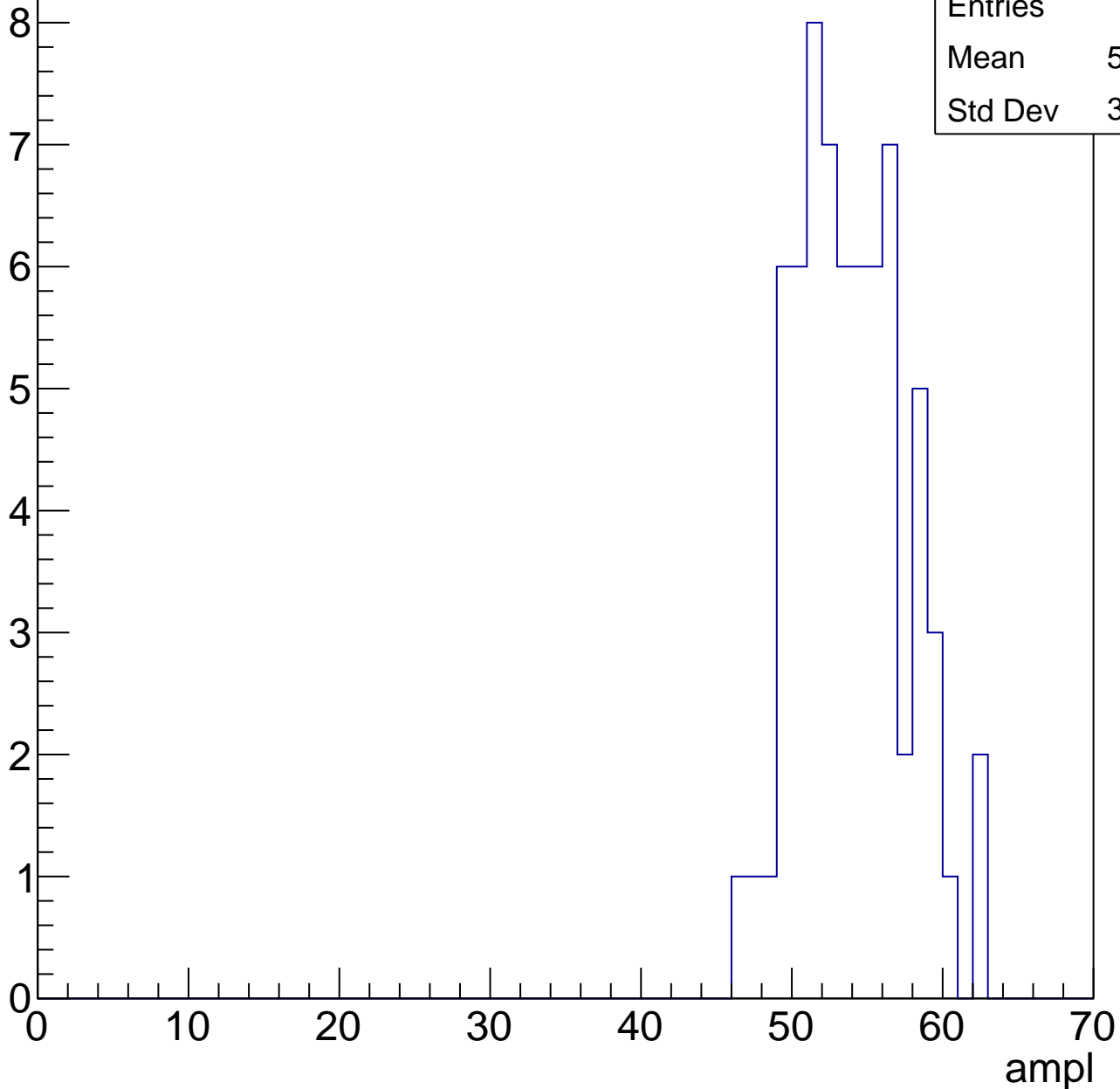


# B1L103S, U25-ch34, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	68
Mean	53.47
Std Dev	3.542

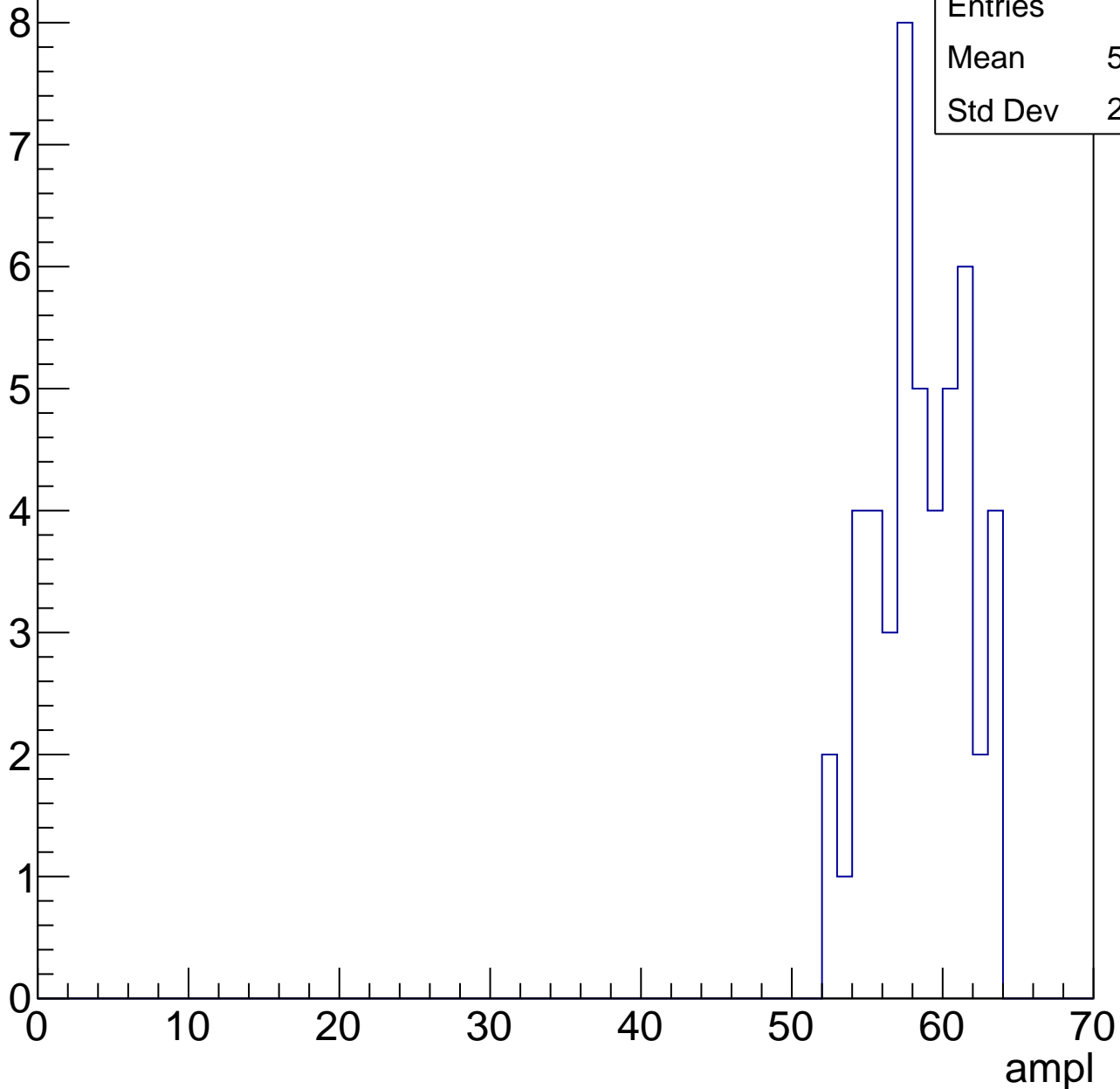


# B1L103S, U25-ch34, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	48
Mean	58.02
Std Dev	2.983

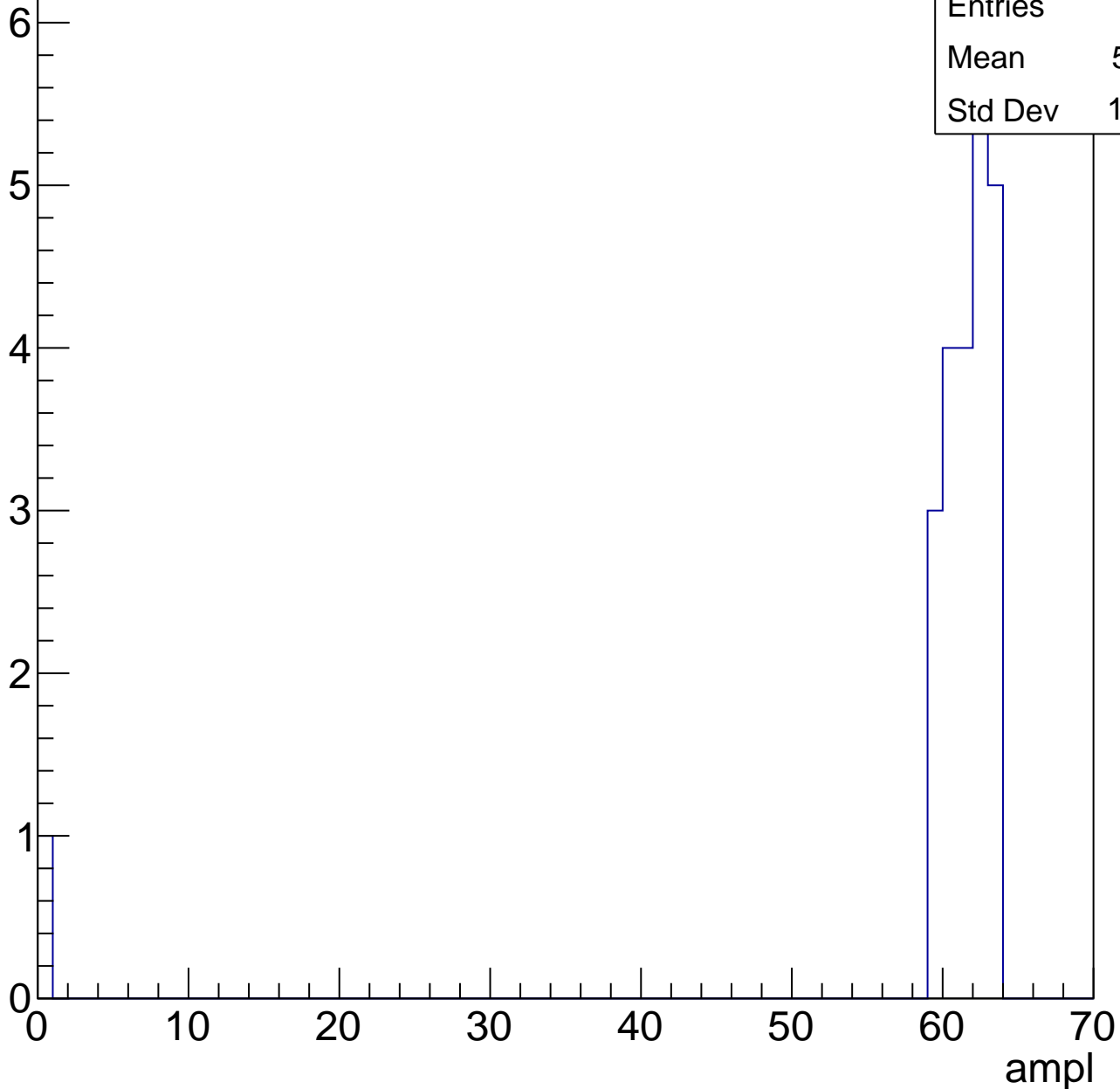


# B1L103S, U25-ch34, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	23
Mean	58.61
Std Dev	12.57





# B1L103S, U25-ch34, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	19
Mean	3.316
Std Dev	14.07

Entry



# B1L103S, U25-ch35, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	74
Mean	24.15
Std Dev	11.45

Entry

12

10

8

6

4

2

0

0

10

20

30

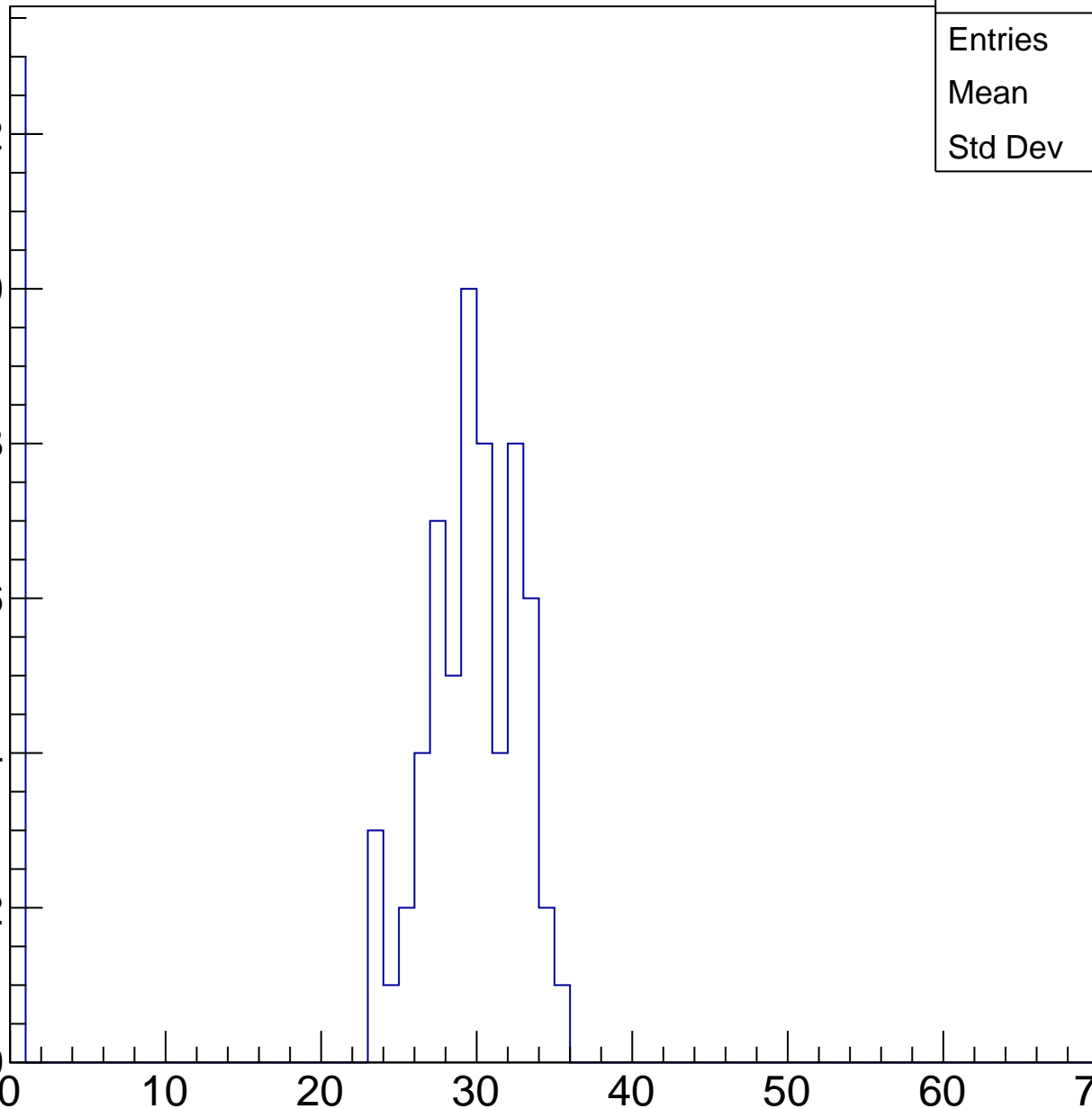
40

50

60

70

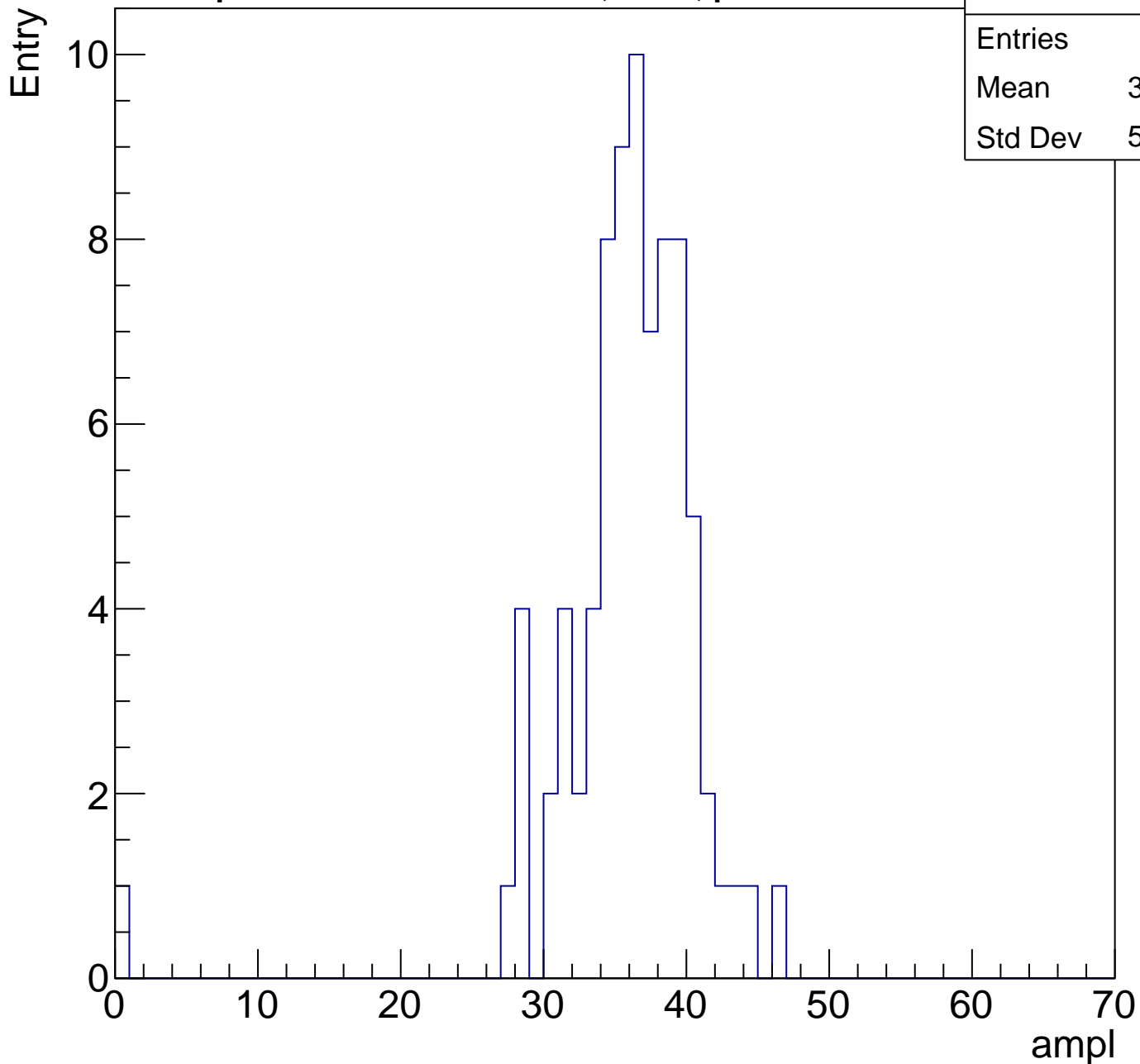
ampl



# B1L103S, U25-ch35, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	79
Mean	35.42
Std Dev	5.486

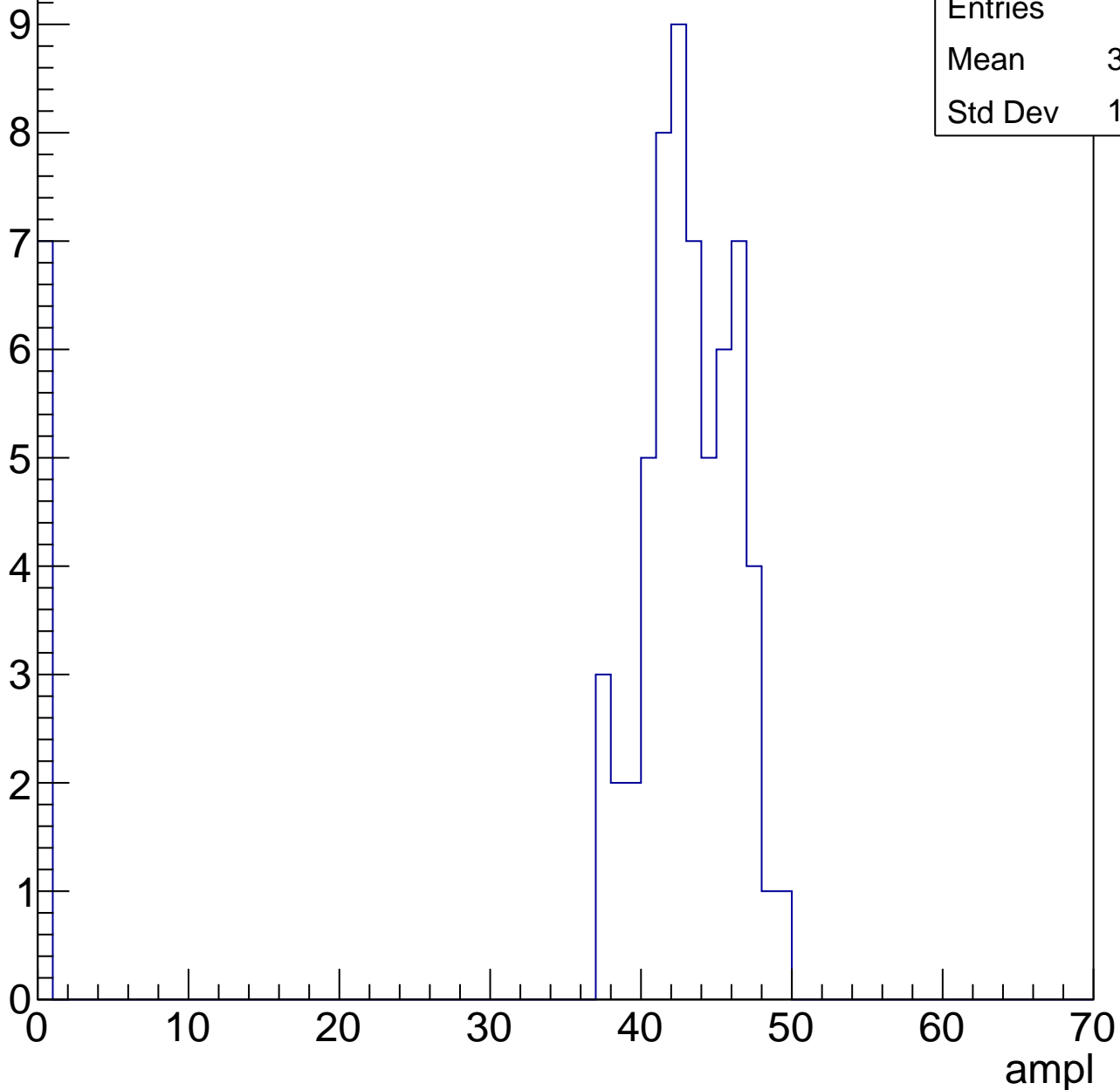


# B1L103S, U25-ch35, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	67
Mean	38.34
Std Dev	13.37



# B1L103S, U25-ch35, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	78
Mean	48.51
Std Dev	8.575

Entry

10

8

6

4

2

0

0

10

20

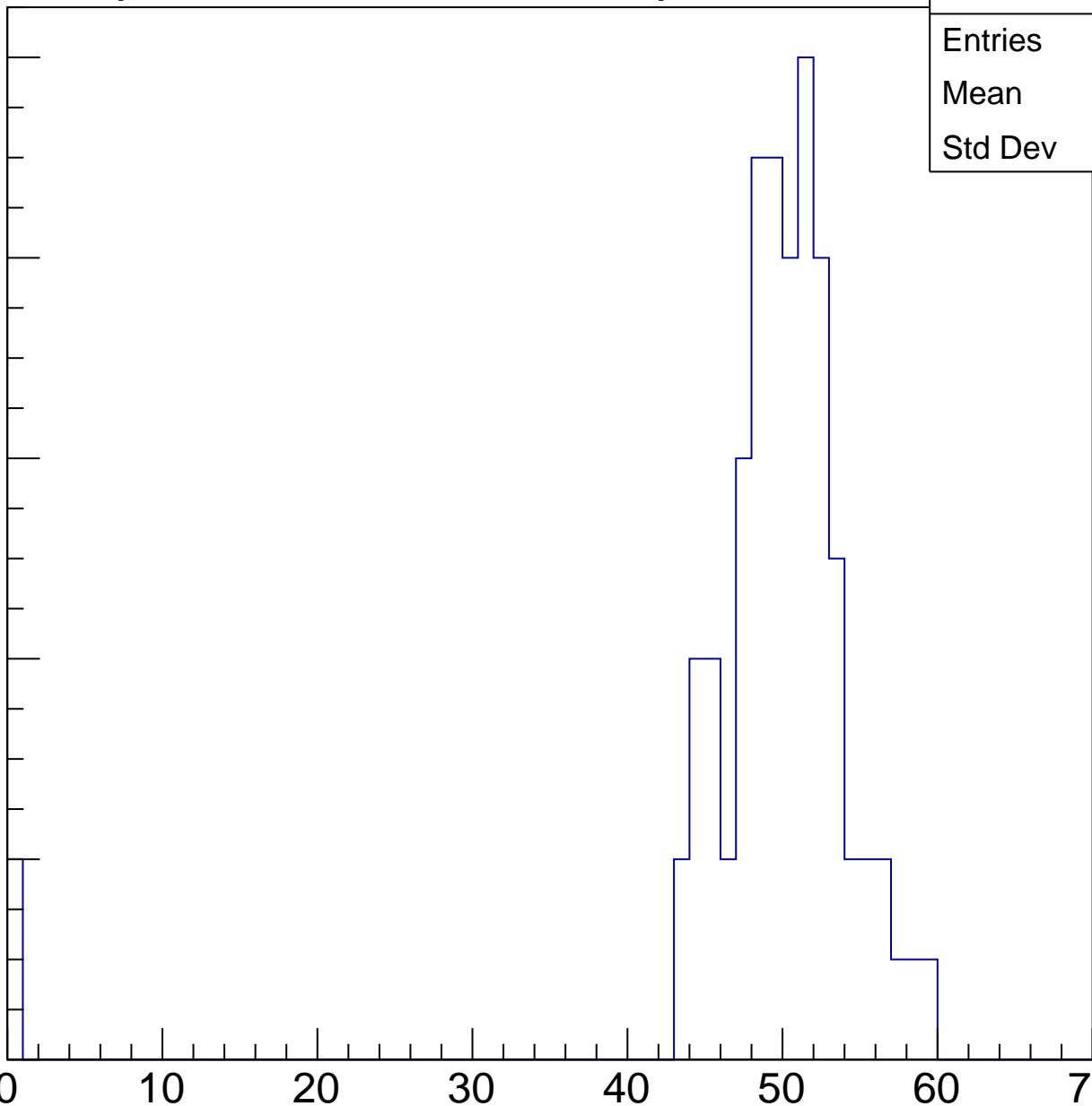
30

40

50

60

ampl

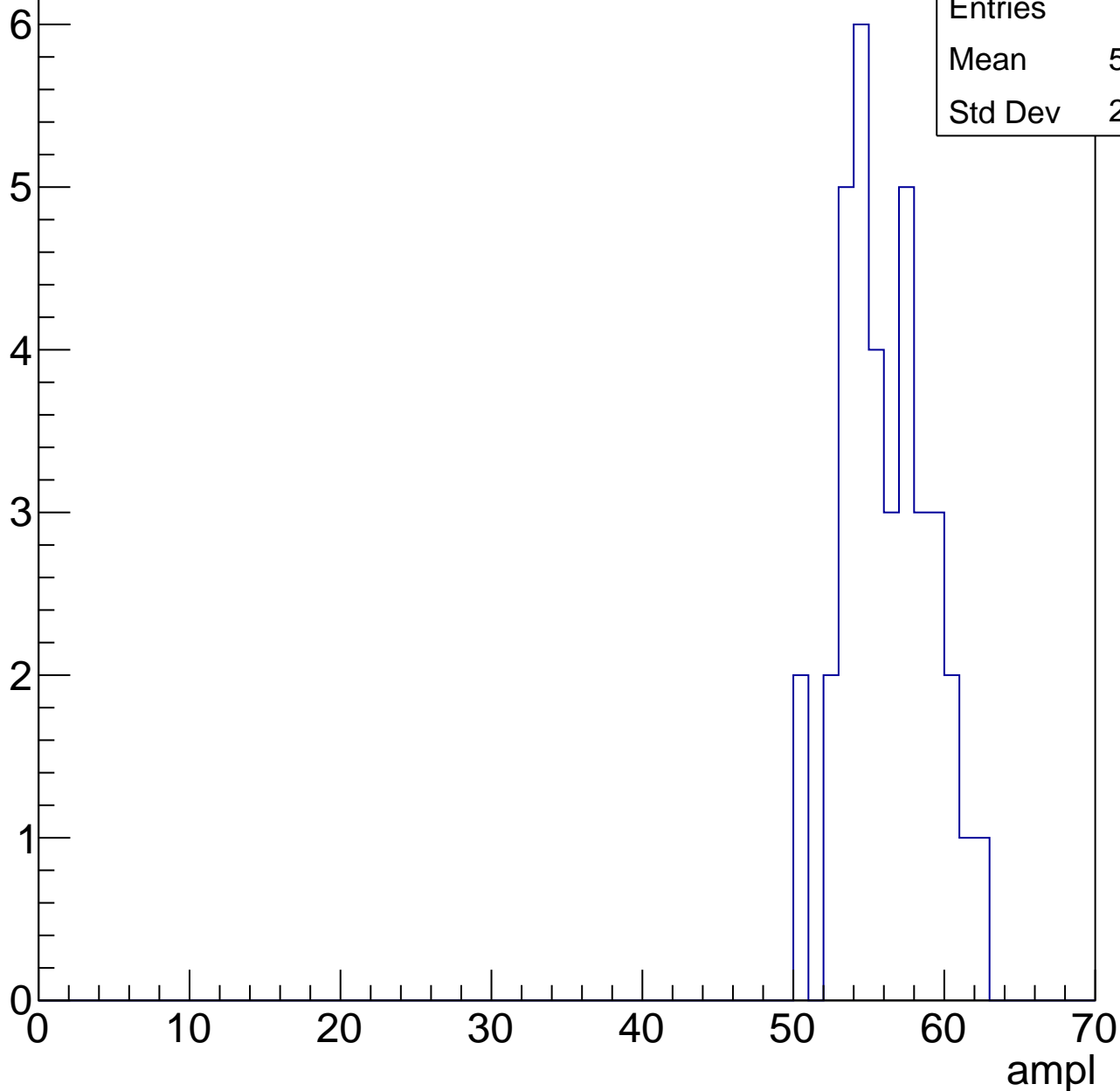


# B1L103S, U25-ch35, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

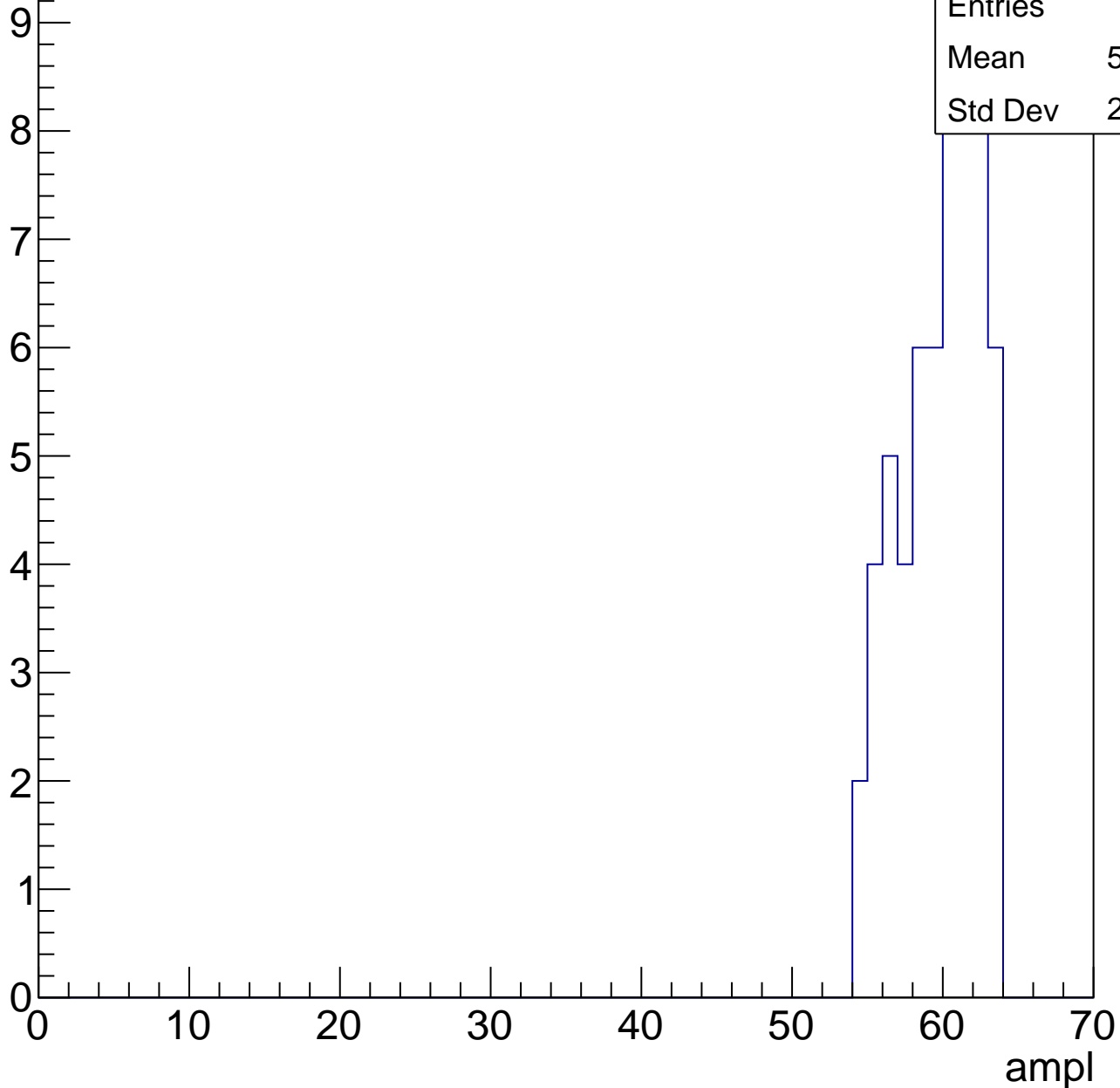
Entries	37
Mean	55.68
Std Dev	2.895



# B1L103S, U25-ch35, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

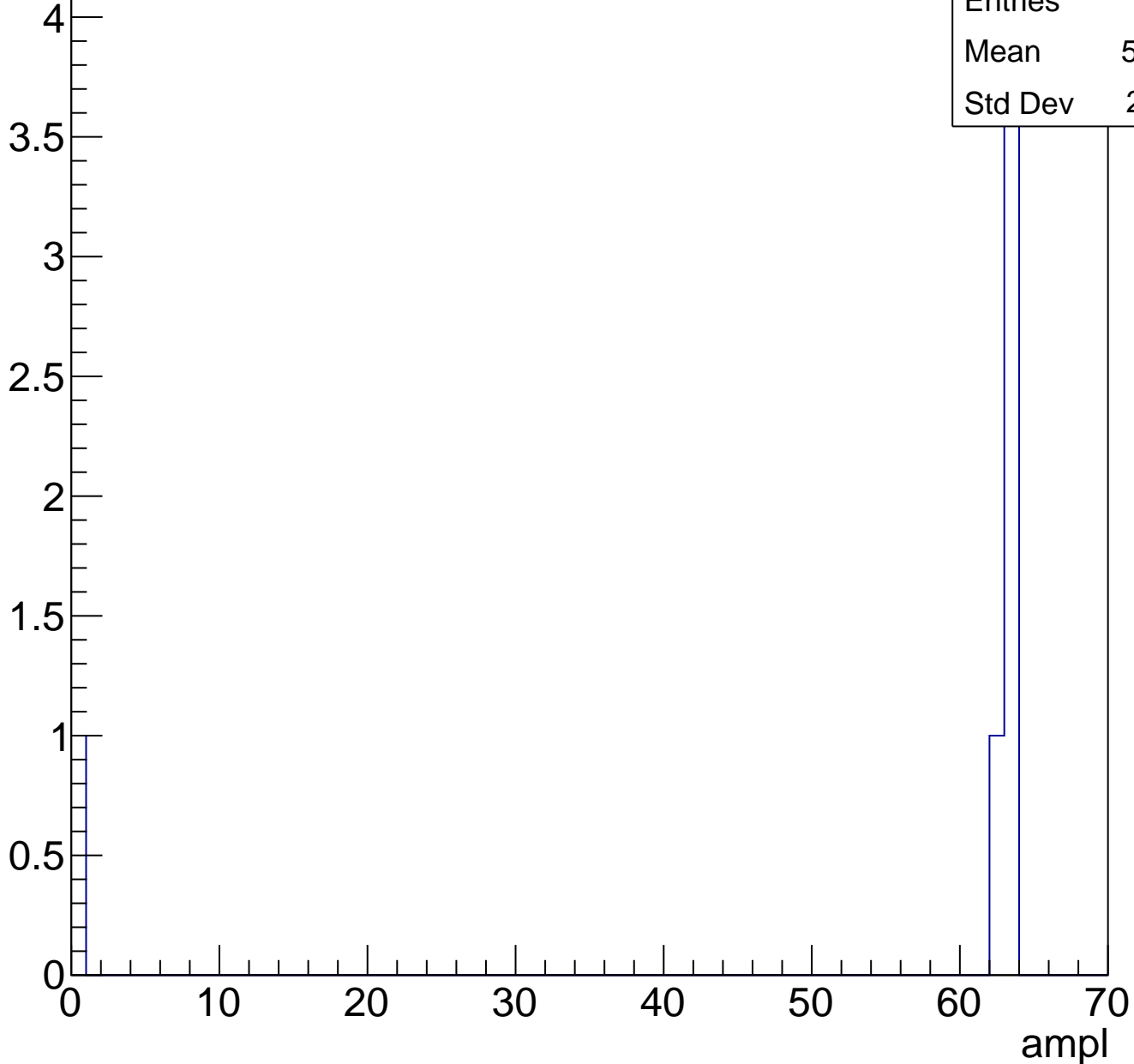
Entry



# B1L103S, U25-ch35, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	6
Mean	52.33
Std Dev	23.41



# B1L103S, U25-ch35, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

# B1L103S, U25-ch36, adc0

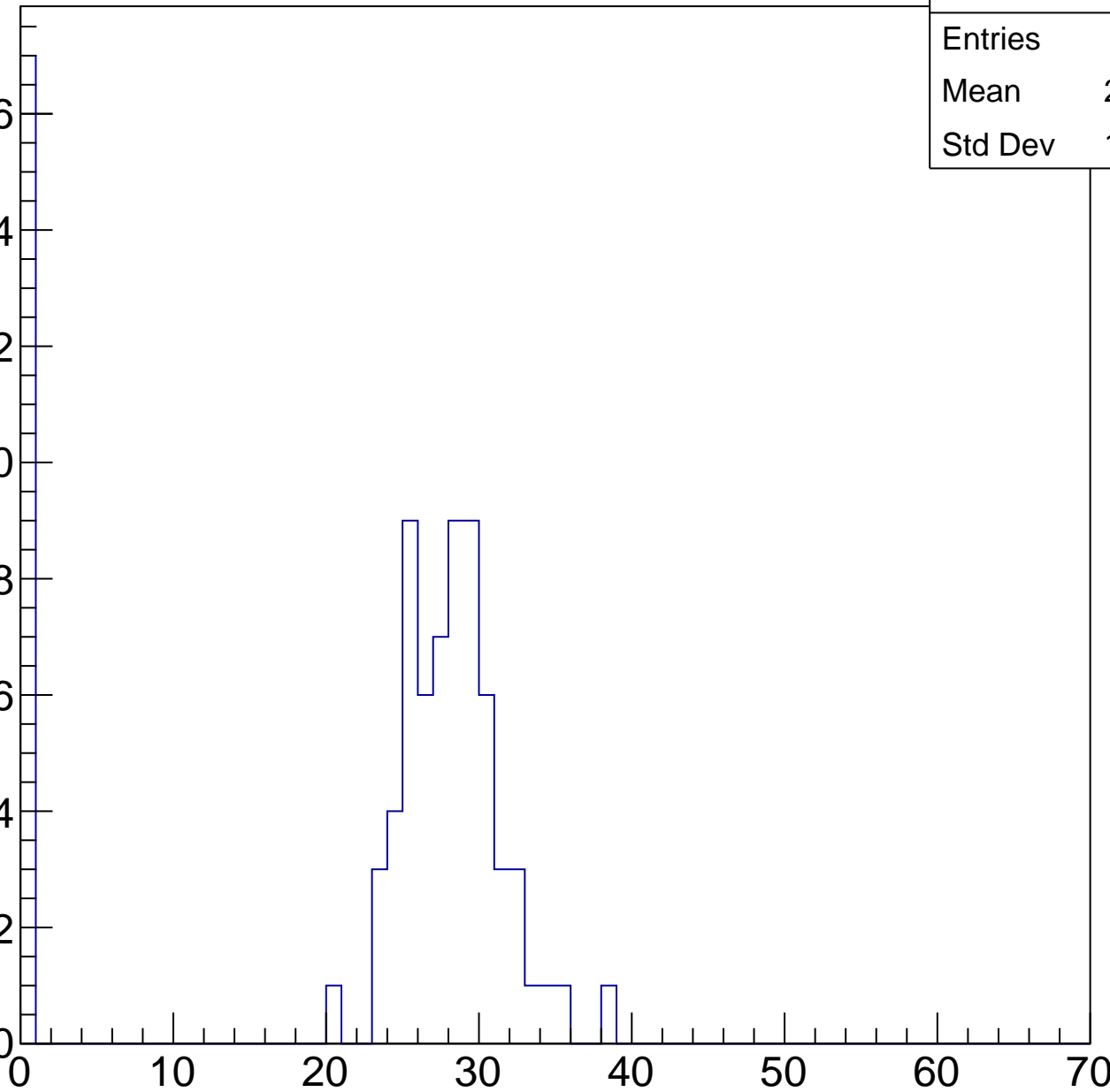
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	81
Mean	21.94
Std Dev	11.65

Entry

16  
14  
12  
10  
8  
6  
4  
2  
0

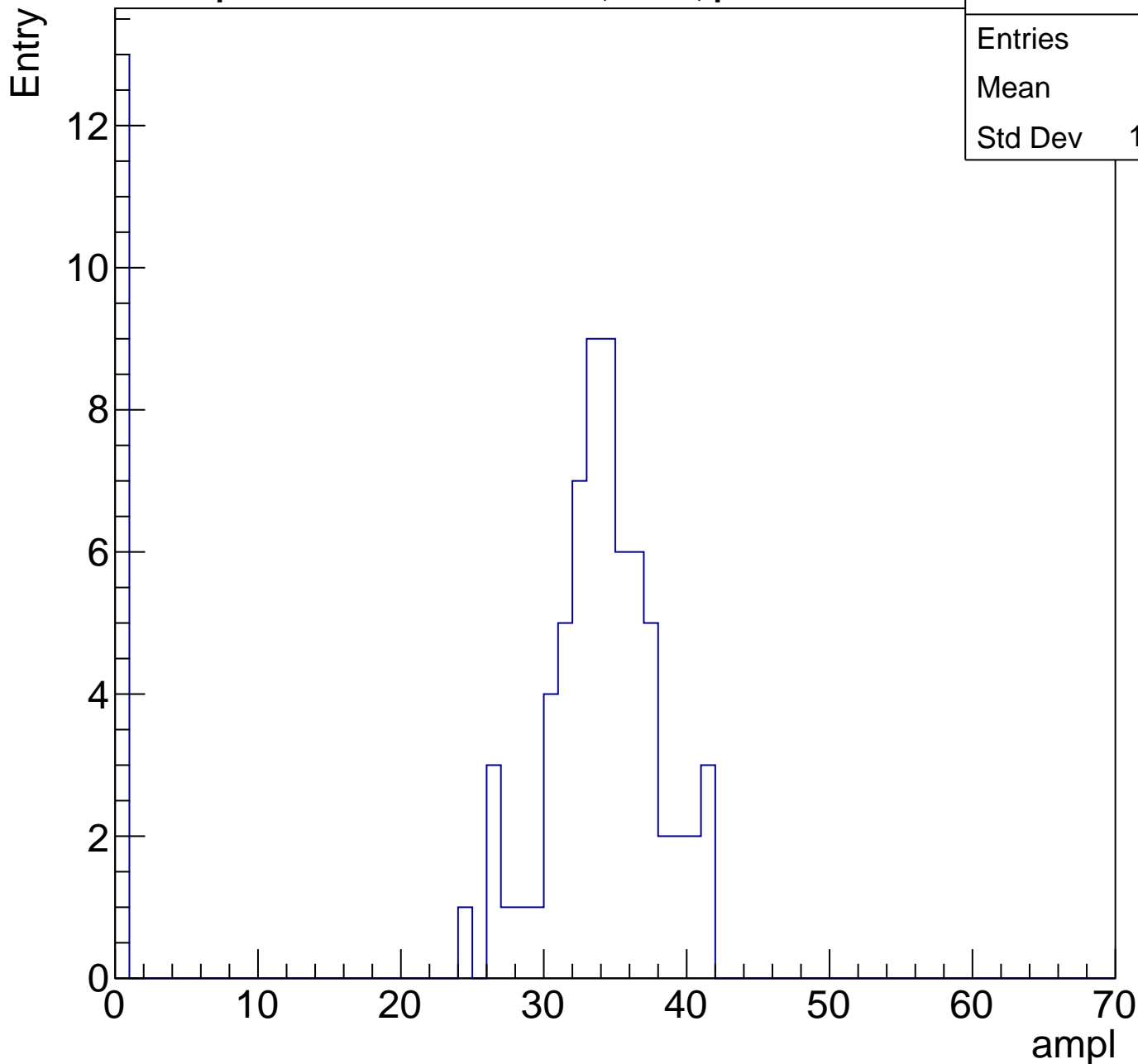
ampl



# B1L103S, U25-ch36, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	80
Mean	28.2
Std Dev	12.87

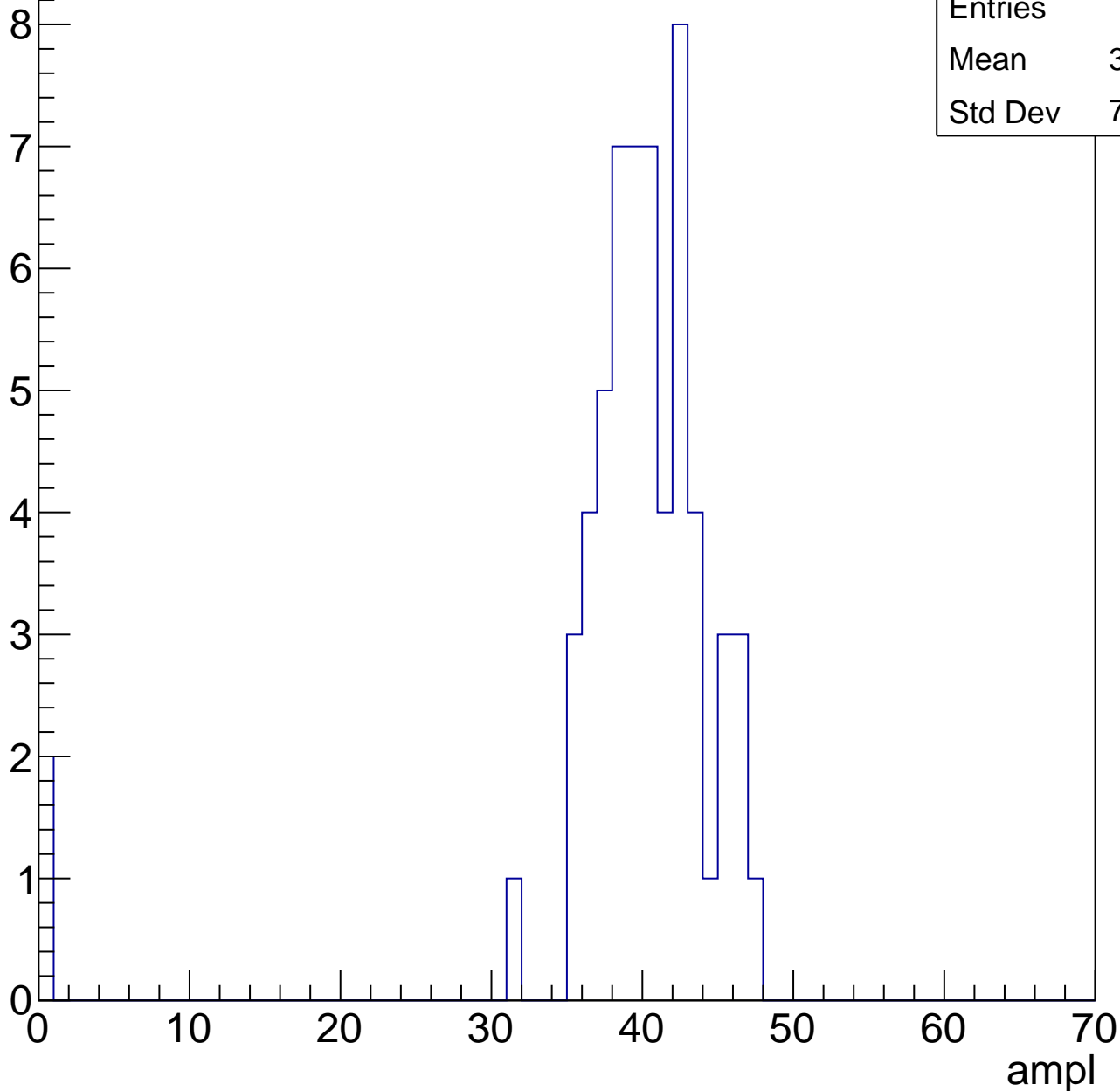


# B1L103S, U25-ch36, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	60
Mean	38.67
Std Dev	7.867

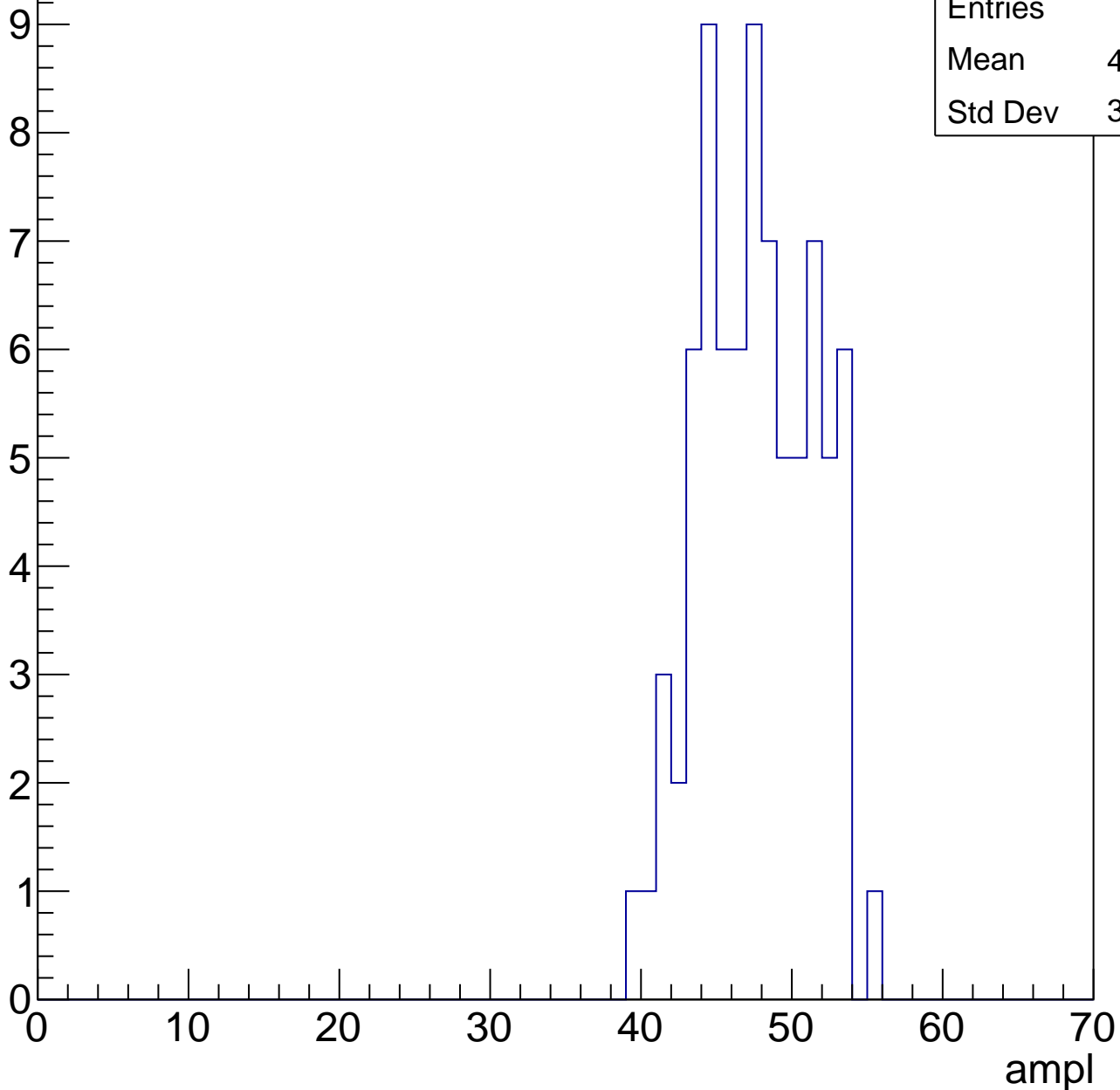


# B1L103S, U25-ch36, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	79
Mean	47.22
Std Dev	3.669

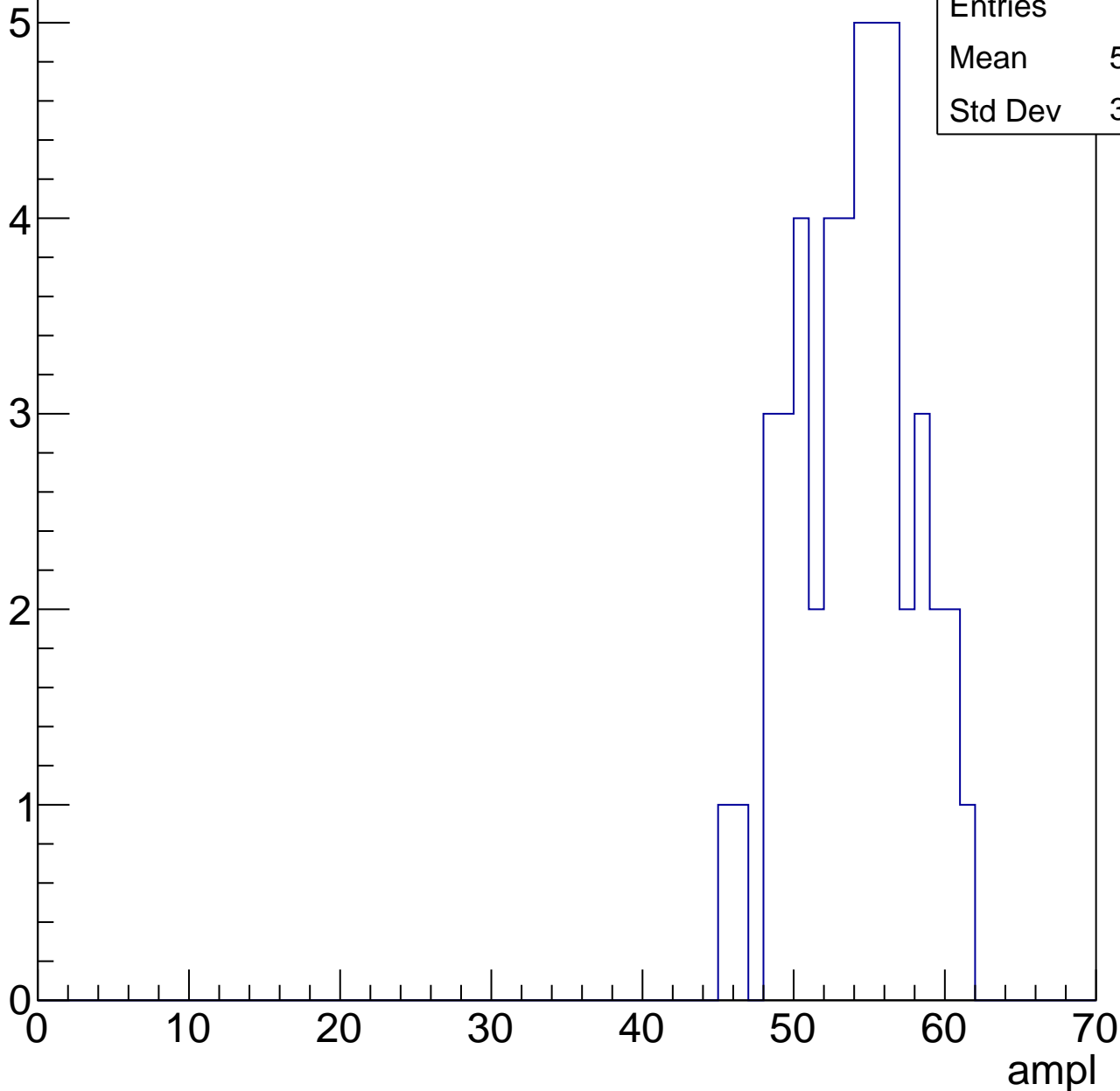


# B1L103S, U25-ch36, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

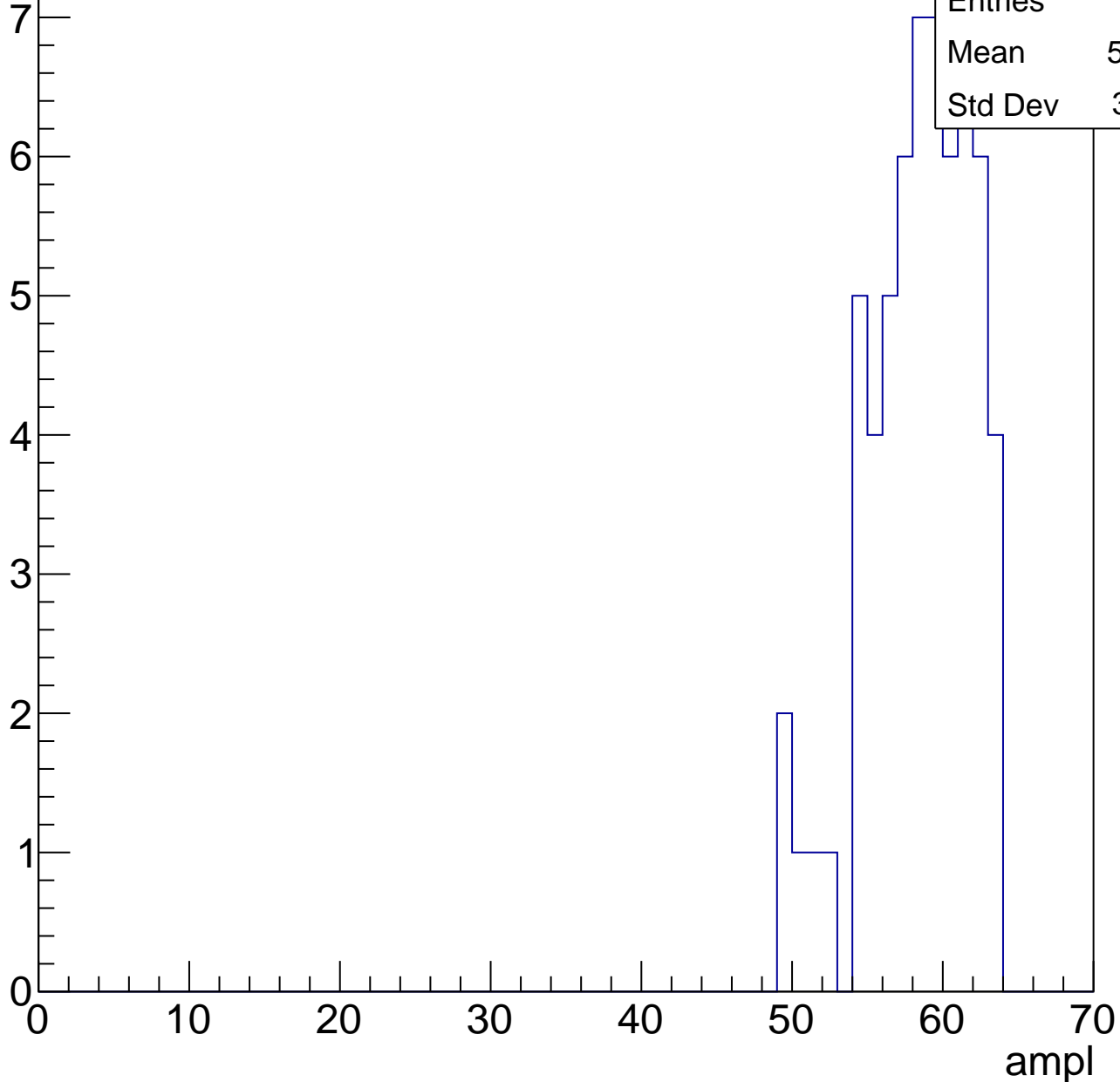
Entries	47
Mean	53.53
Std Dev	3.808



# B1L103S, U25-ch36, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

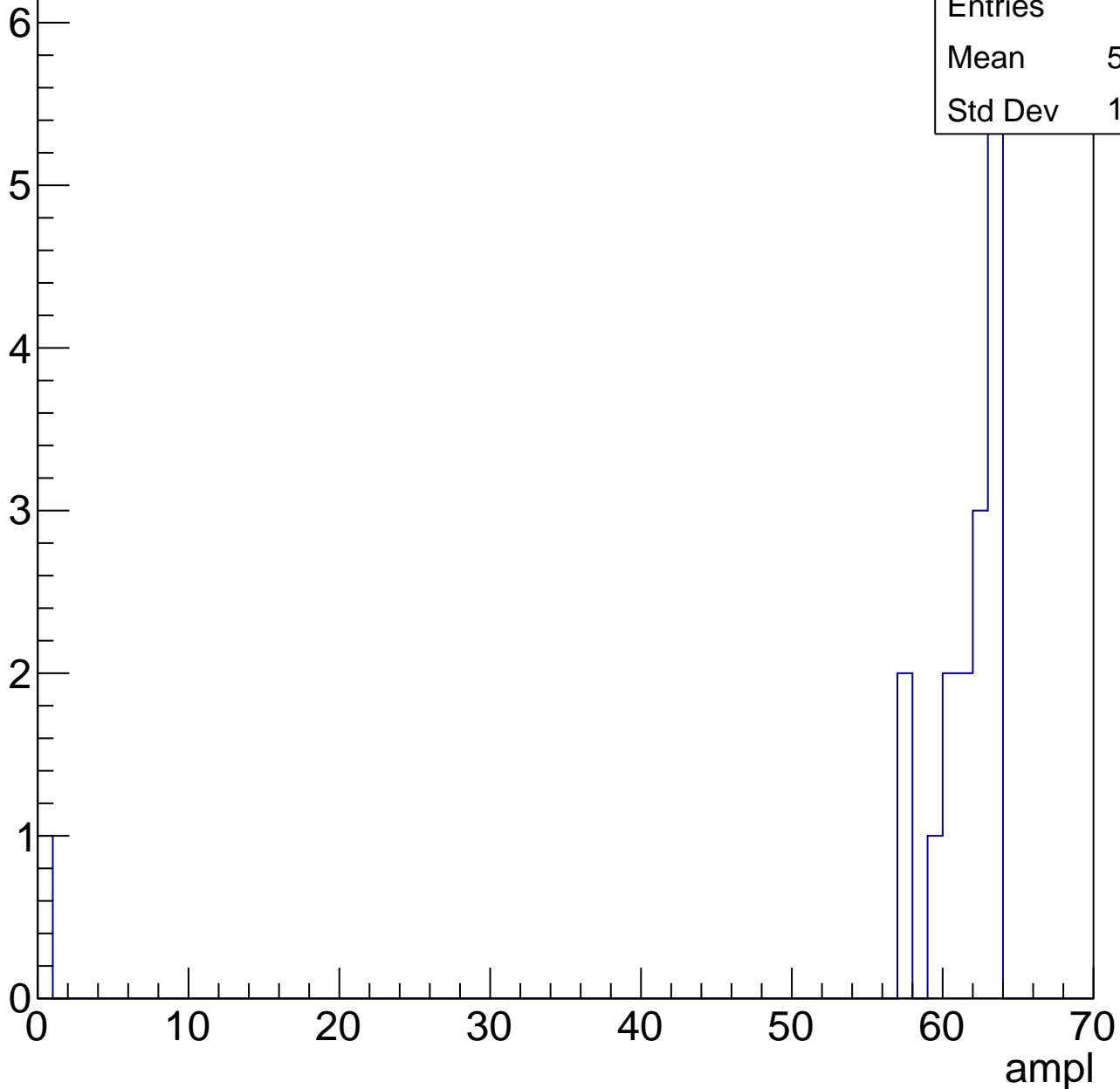


# B1L103S, U25-ch36, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	17
Mean	57.59
Std Dev	14.53





# B1L103S, U25-ch36, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	20
Mean	5.95
Std Dev	15.85

Entry

16

14

12

10

8

6

4

2

0

0

10

20

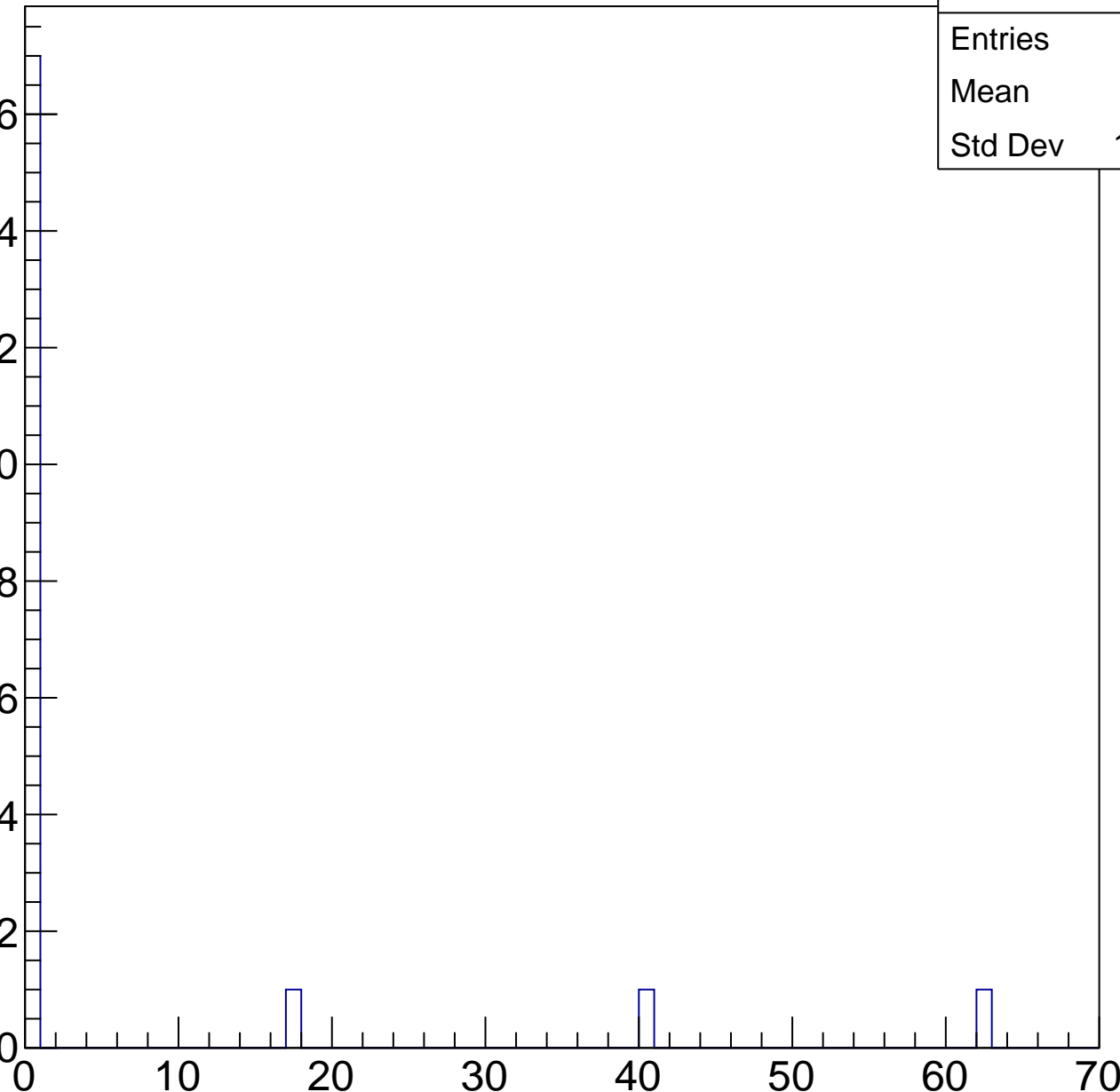
30

40

50

60

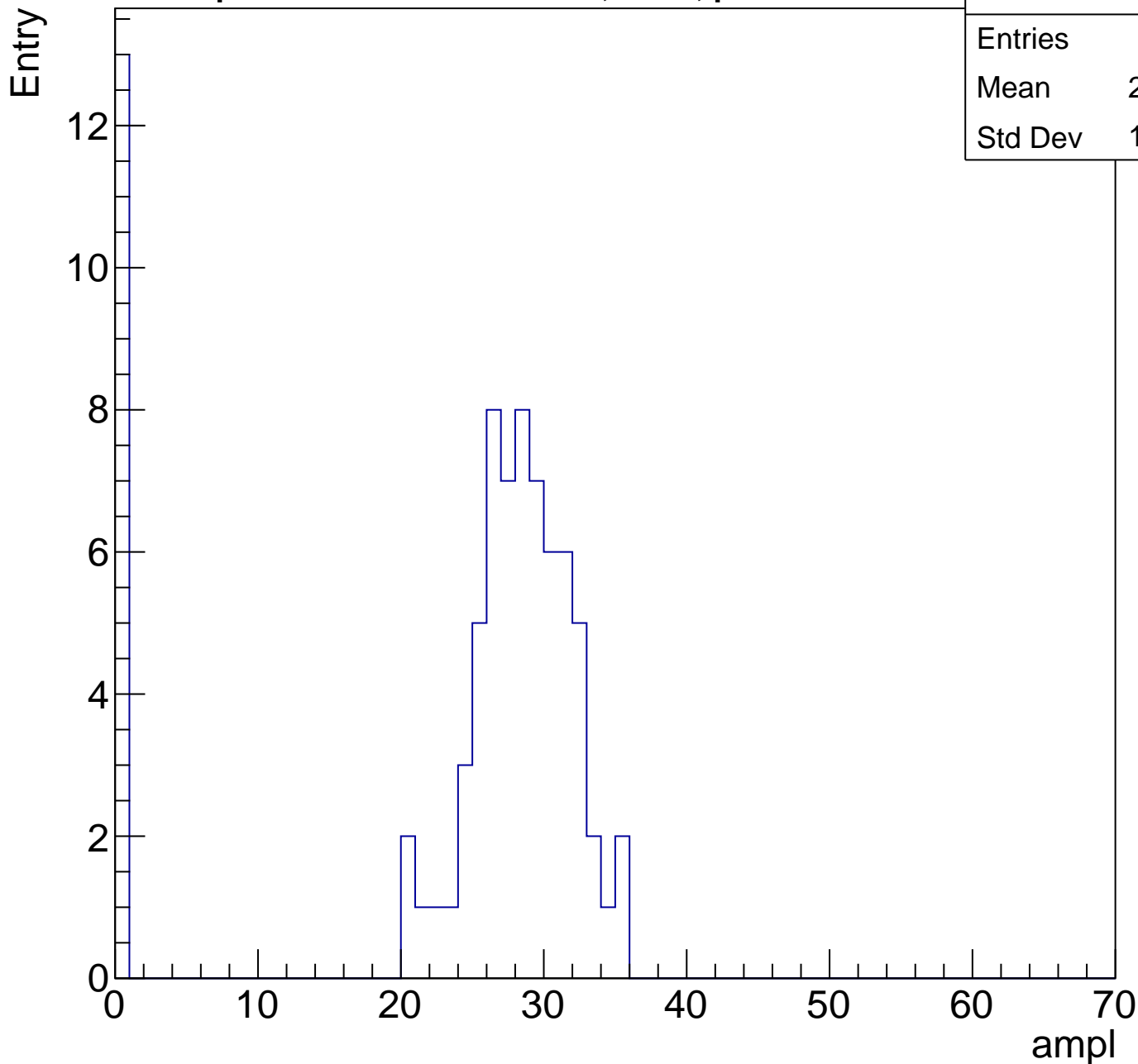
ampl



# B1L103S, U25-ch37, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

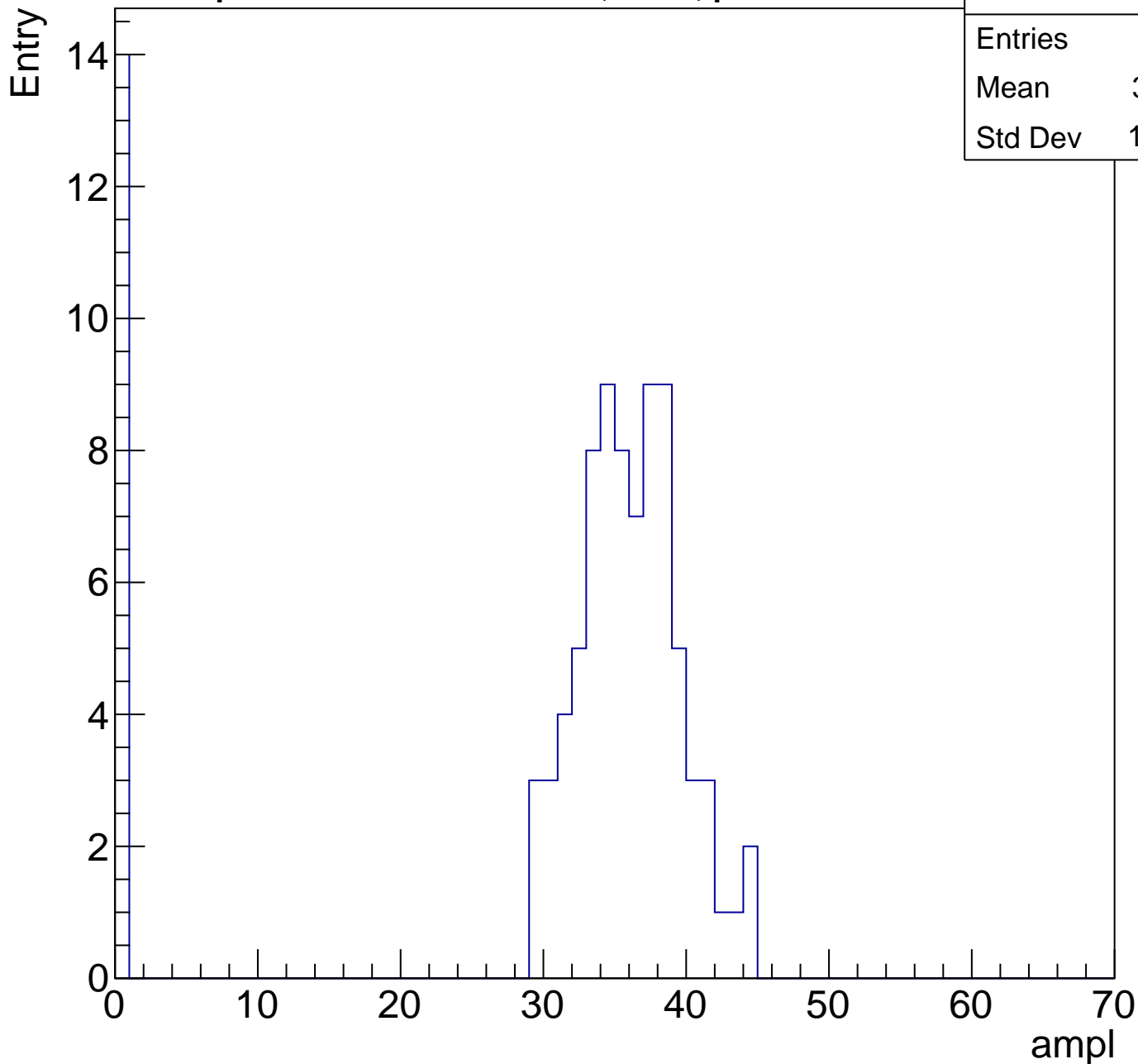
Entries	78
Mean	23.37
Std Dev	10.88



# B1L103S, U25-ch37, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	94
Mean	30.31
Std Dev	13.08

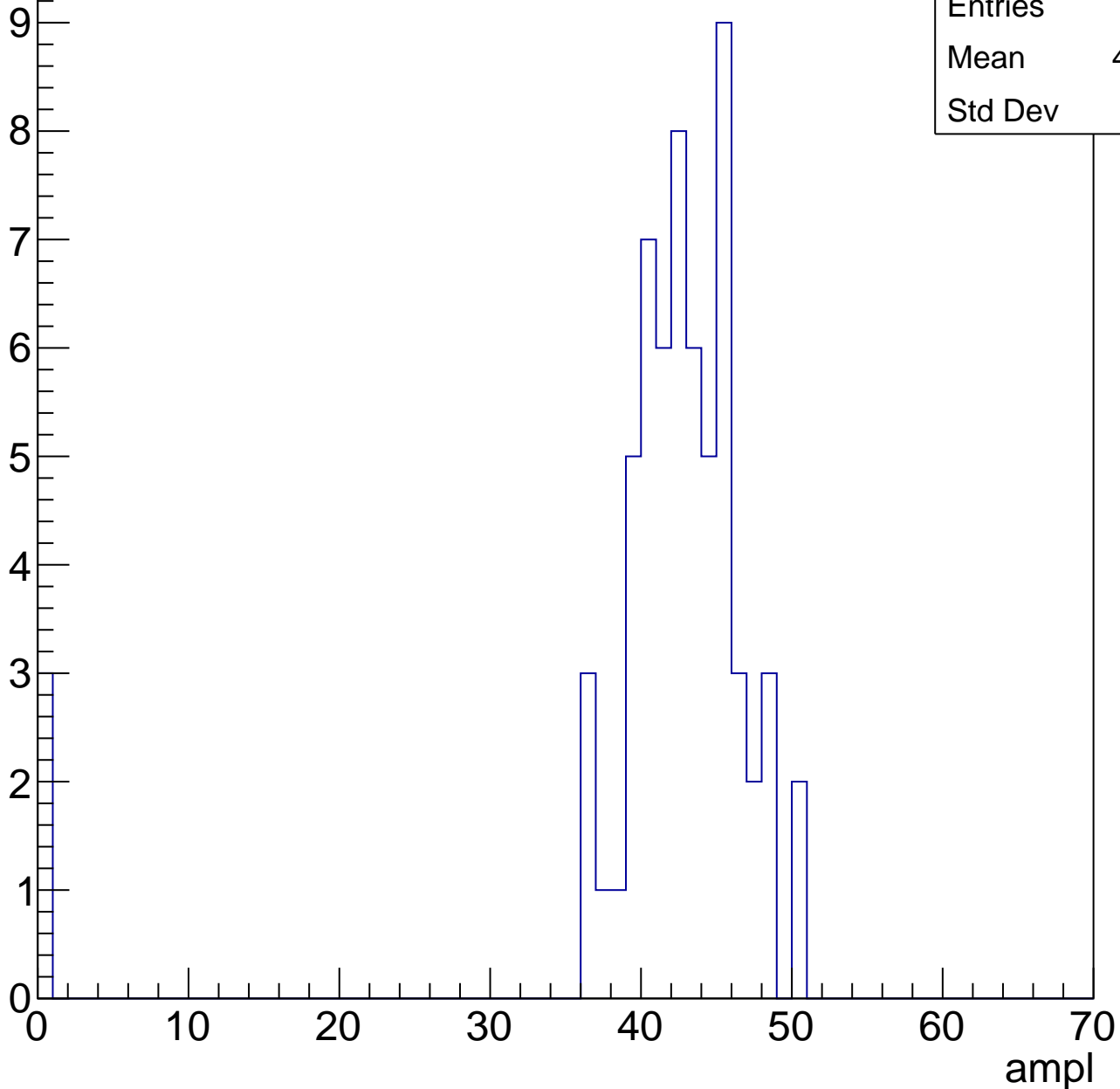


# B1L103S, U25-ch37, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

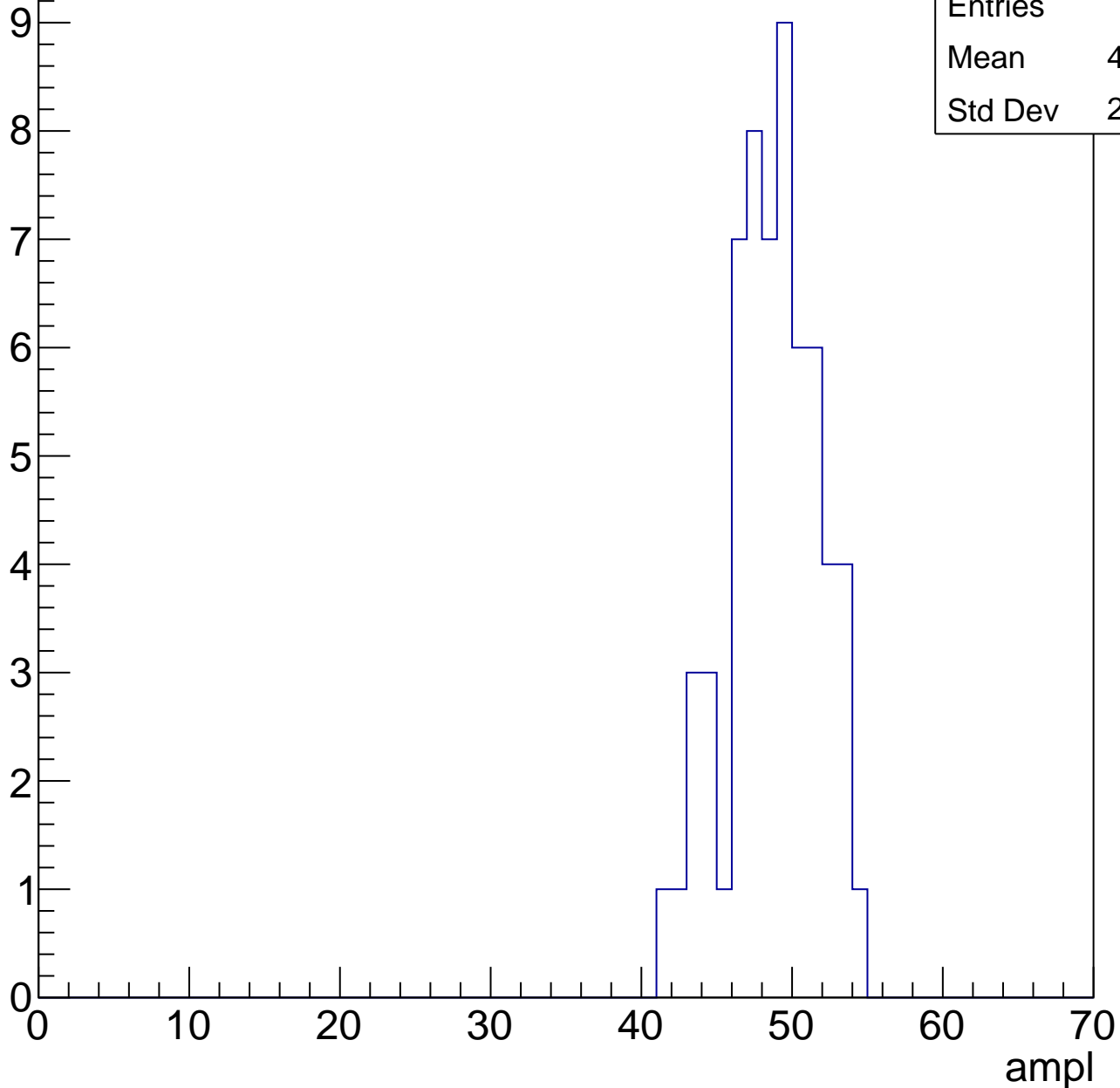
Entries	64
Mean	40.61
Std Dev	9.55



# B1L103S, U25-ch37, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



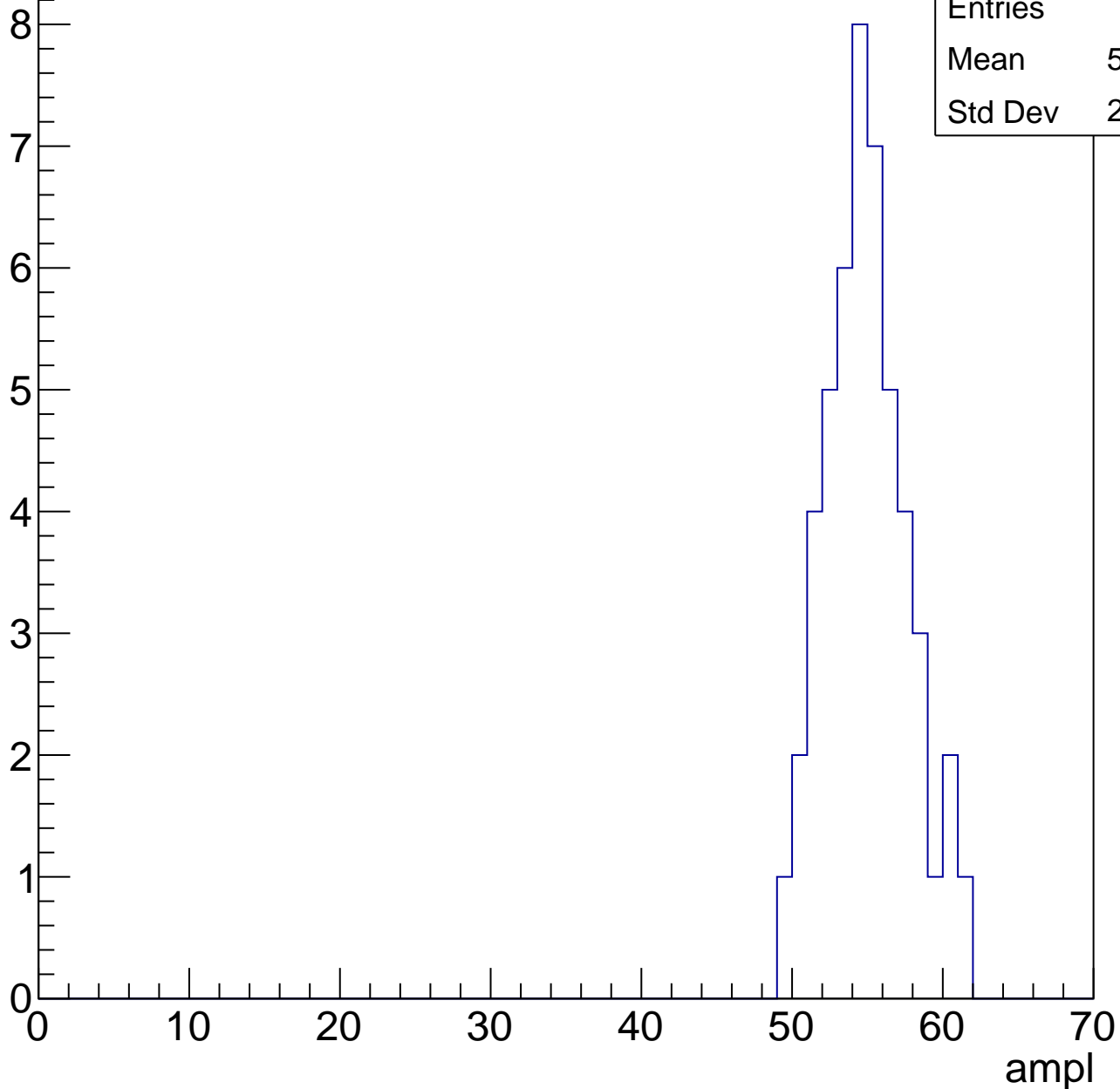
Entries	61
Mean	48.26
Std Dev	2.964

# B1L103S, U25-ch37, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

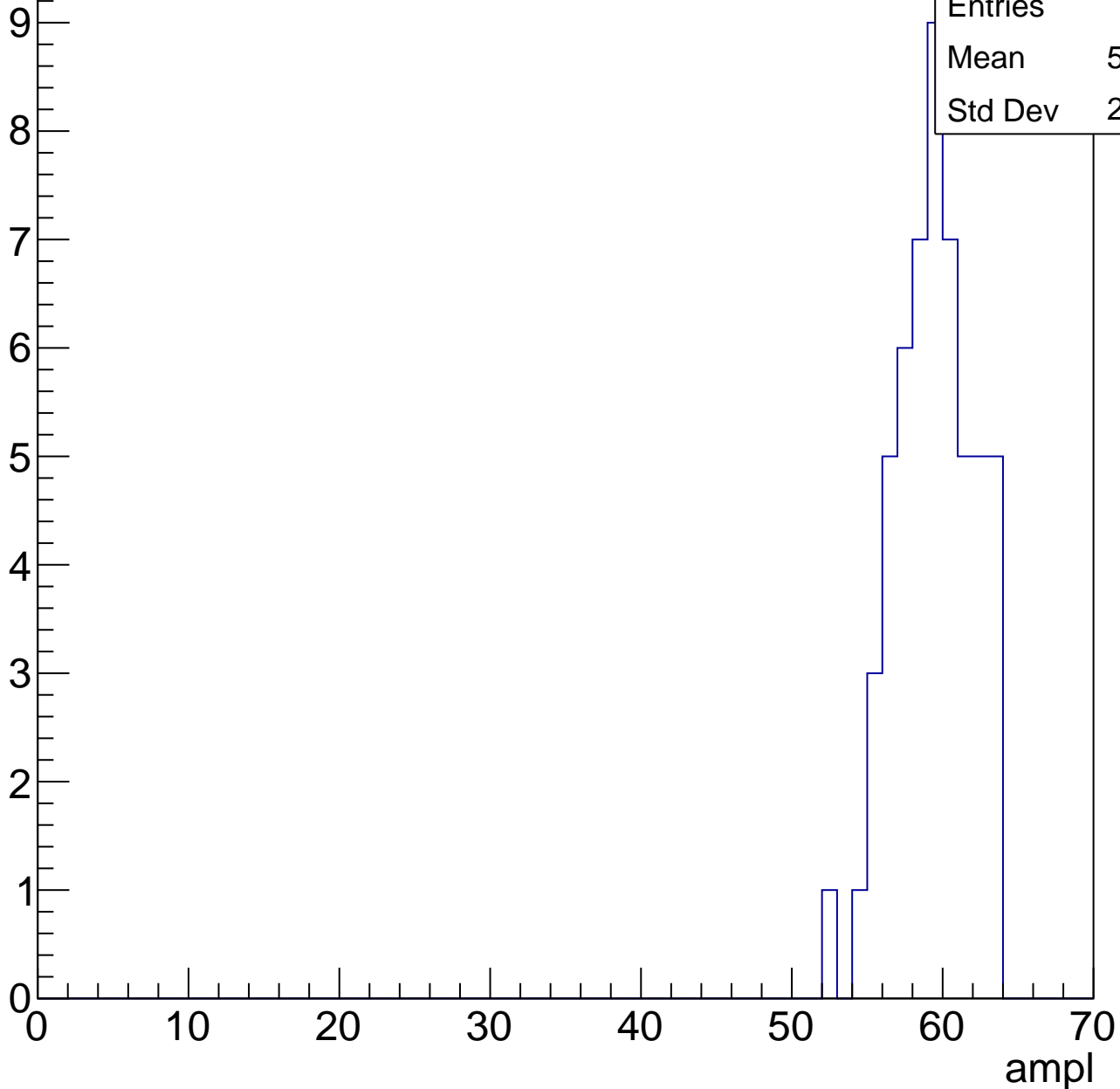
Entries	49
Mean	54.49
Std Dev	2.726



# B1L103S, U25-ch37, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

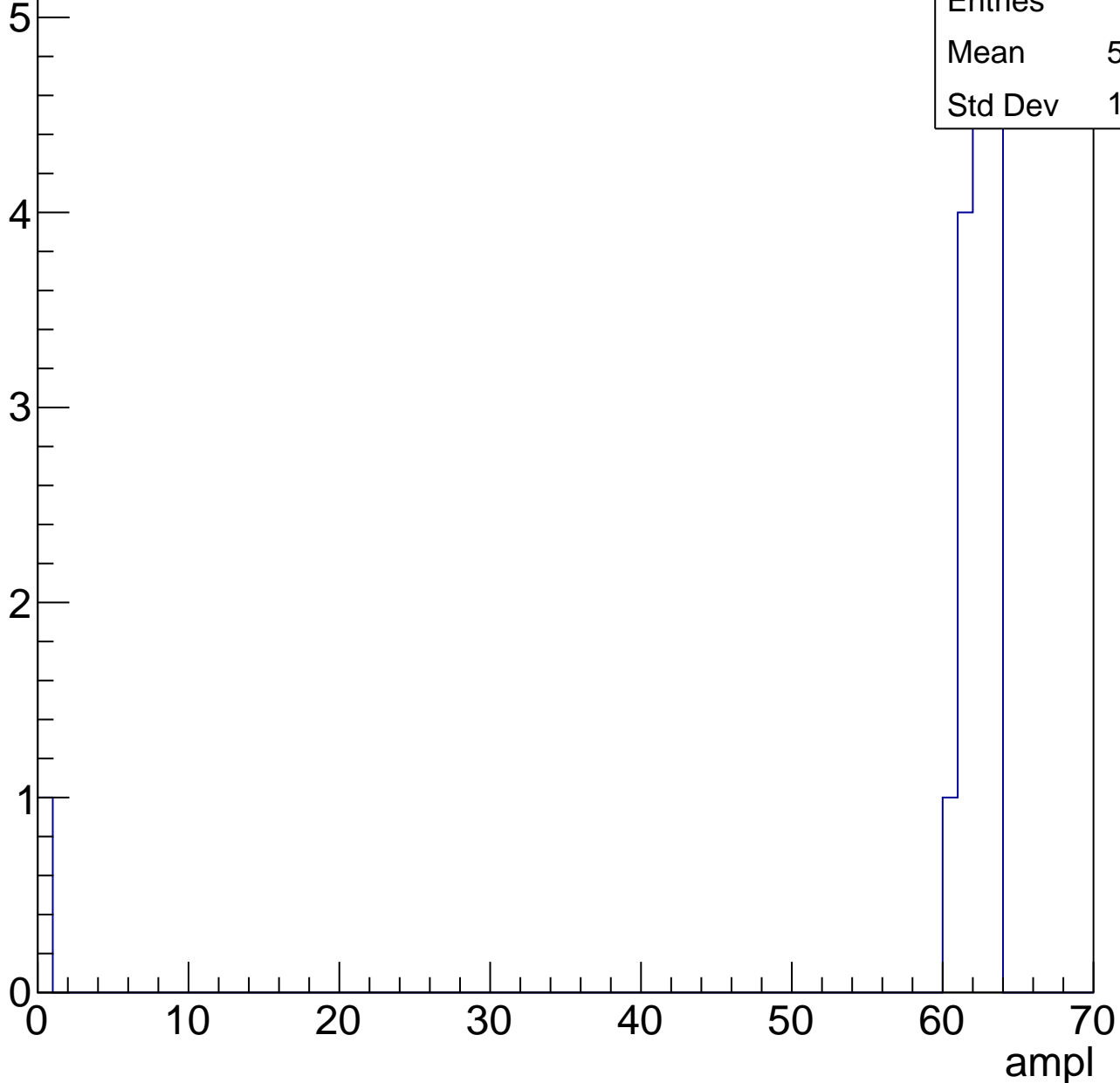


# B1L103S, U25-ch37, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	16
Mean	58.06
Std Dev	15.02





# B1L103S, U25-ch37, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

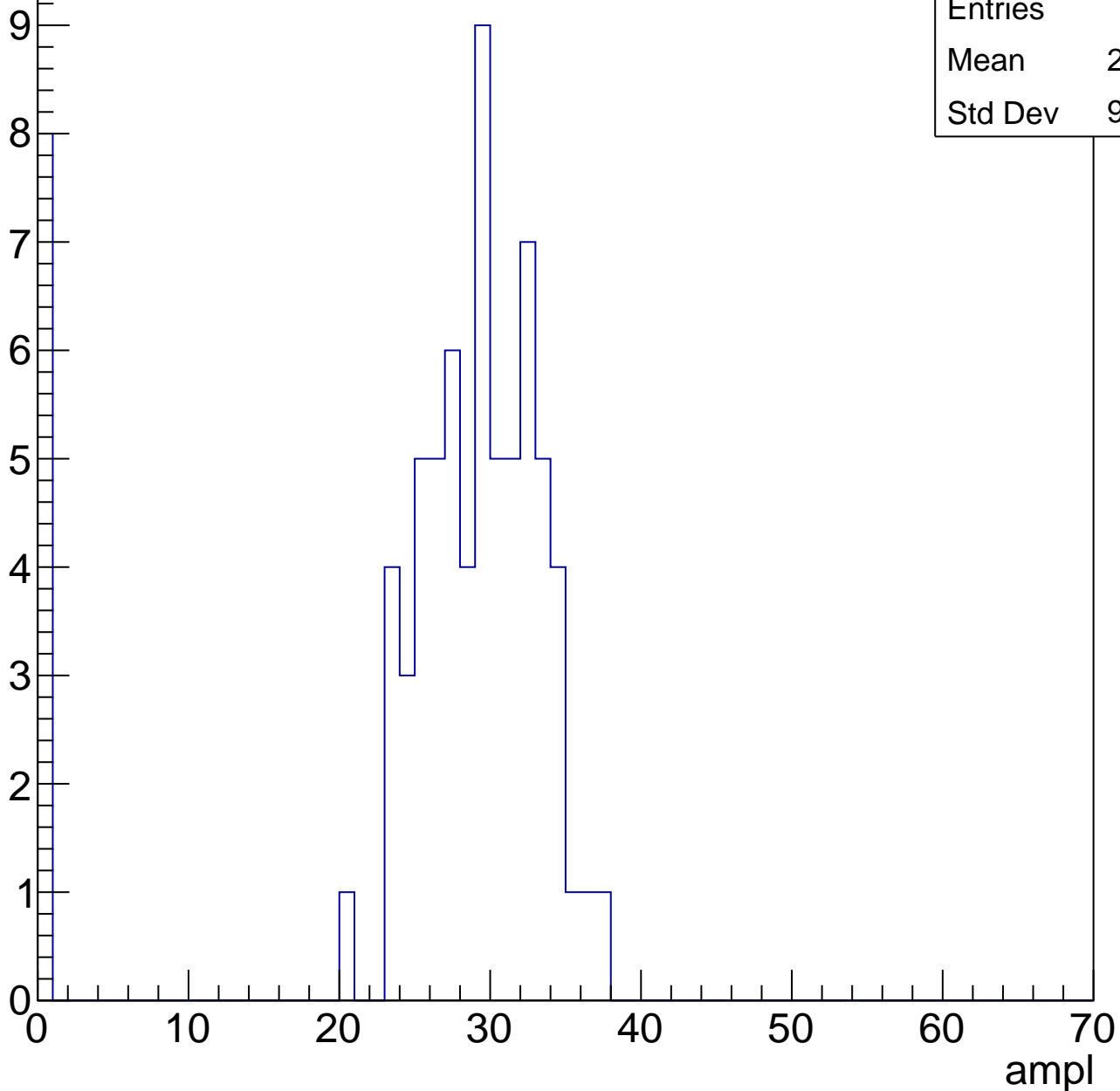


# B1L103S, U25-ch38, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	74
Mean	25.84
Std Dev	9.627

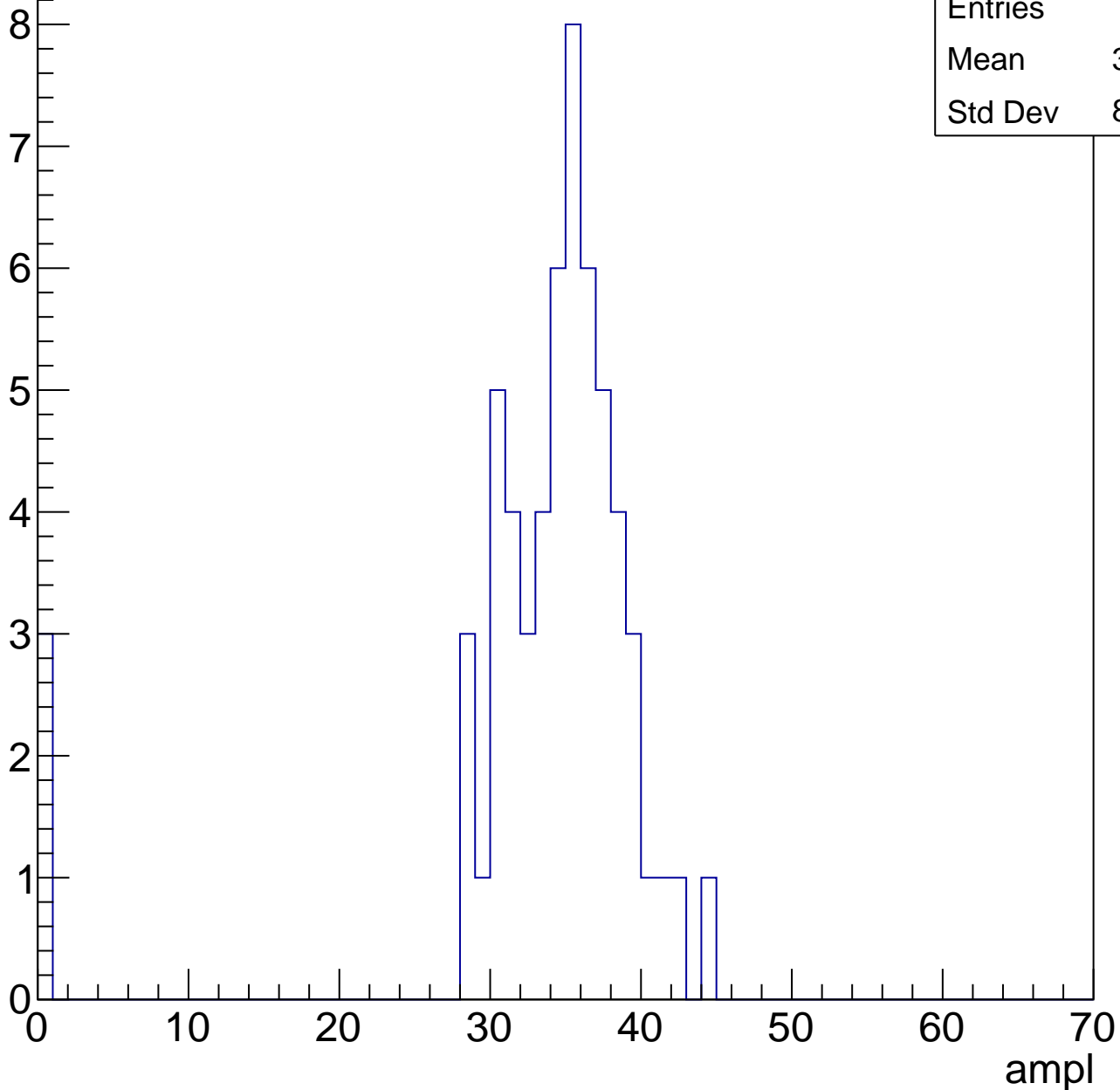


# B1L103S, U25-ch38, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	59
Mean	32.81
Std Dev	8.351

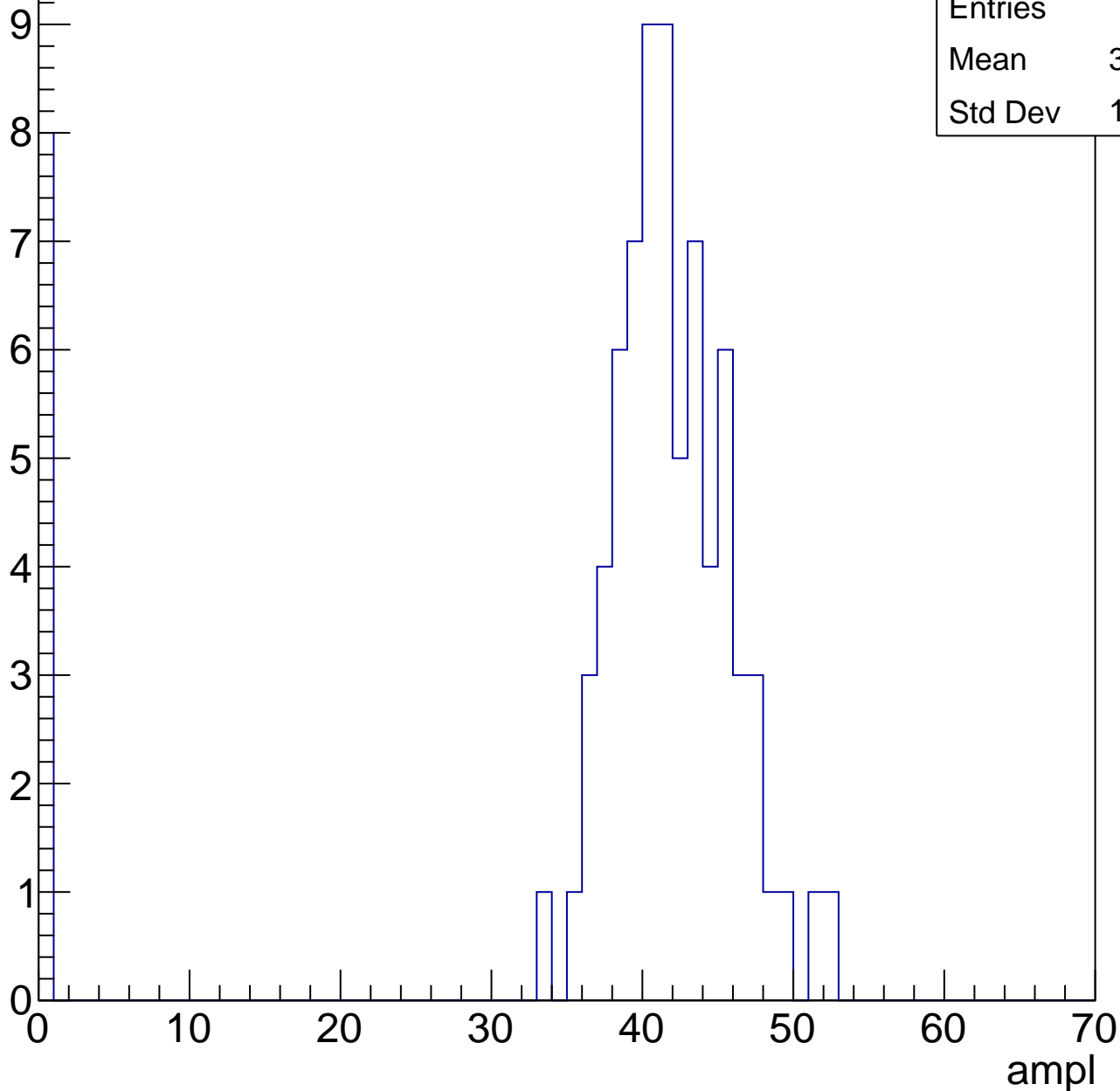


# B1L103S, U25-ch38, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	80
Mean	37.38
Std Dev	12.95

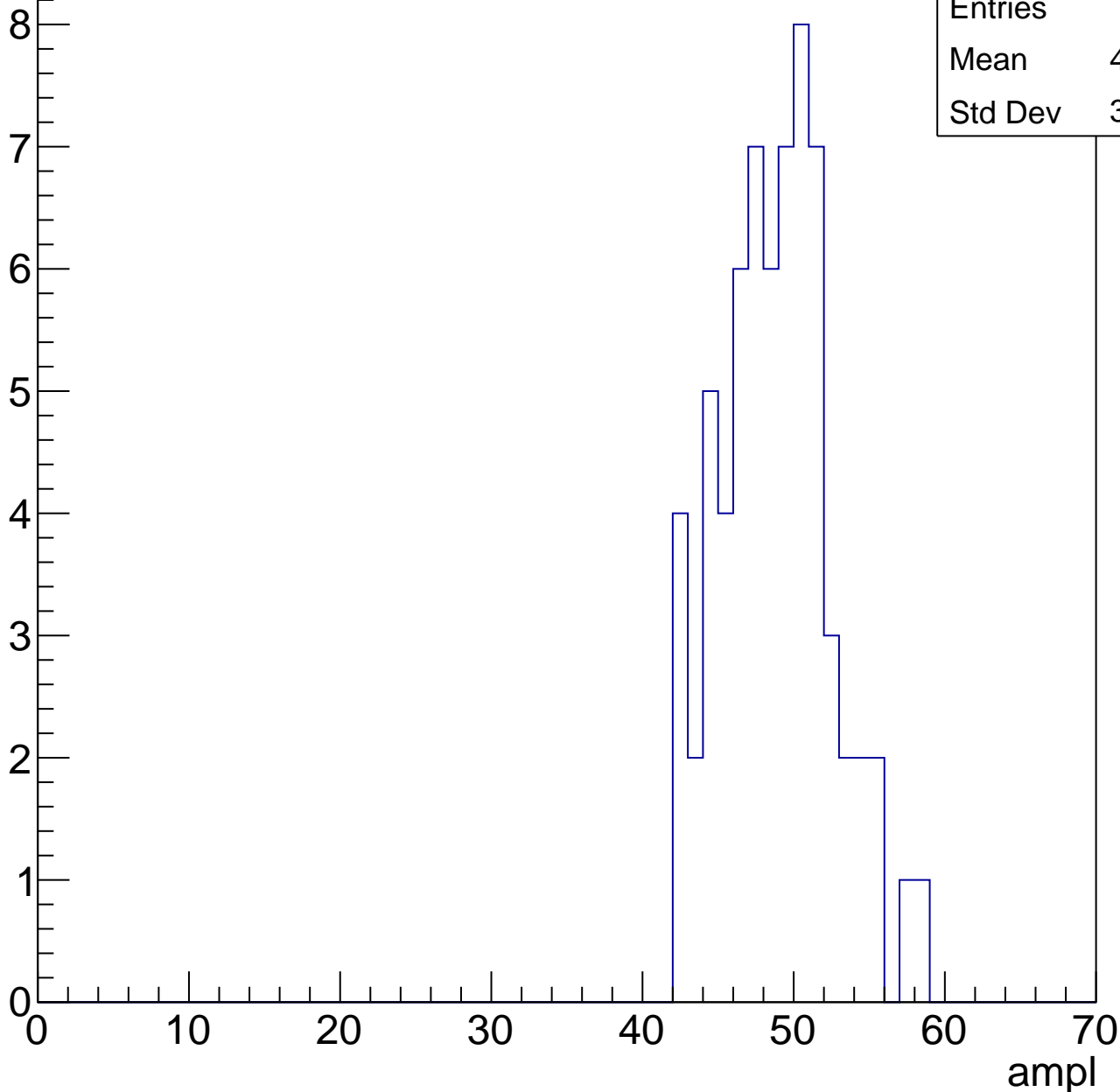


# B1L103S, U25-ch38, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	67
Mean	48.39
Std Dev	3.628

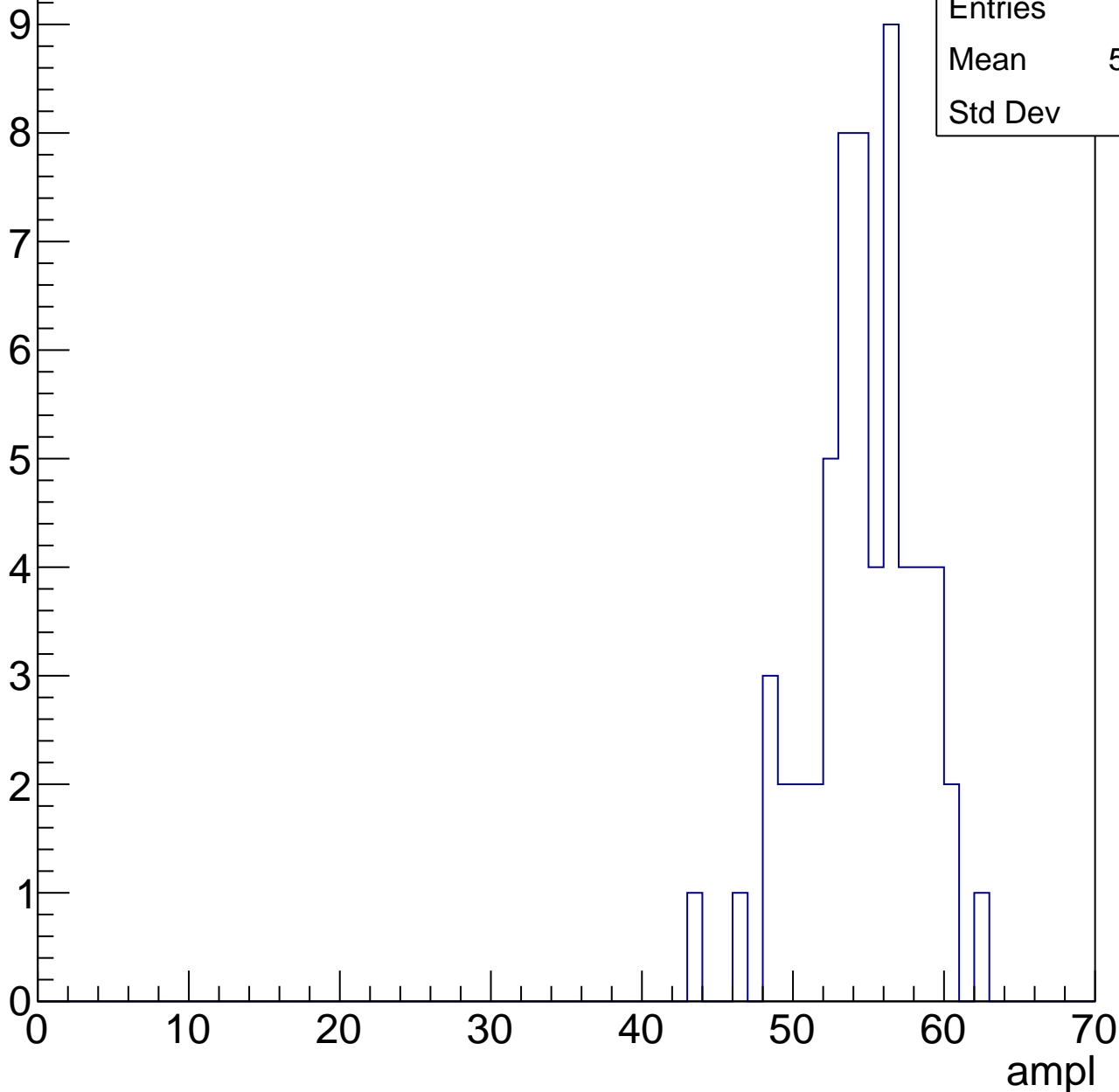


# B1L103S, U25-ch38, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	60
Mean	54.18
Std Dev	3.64

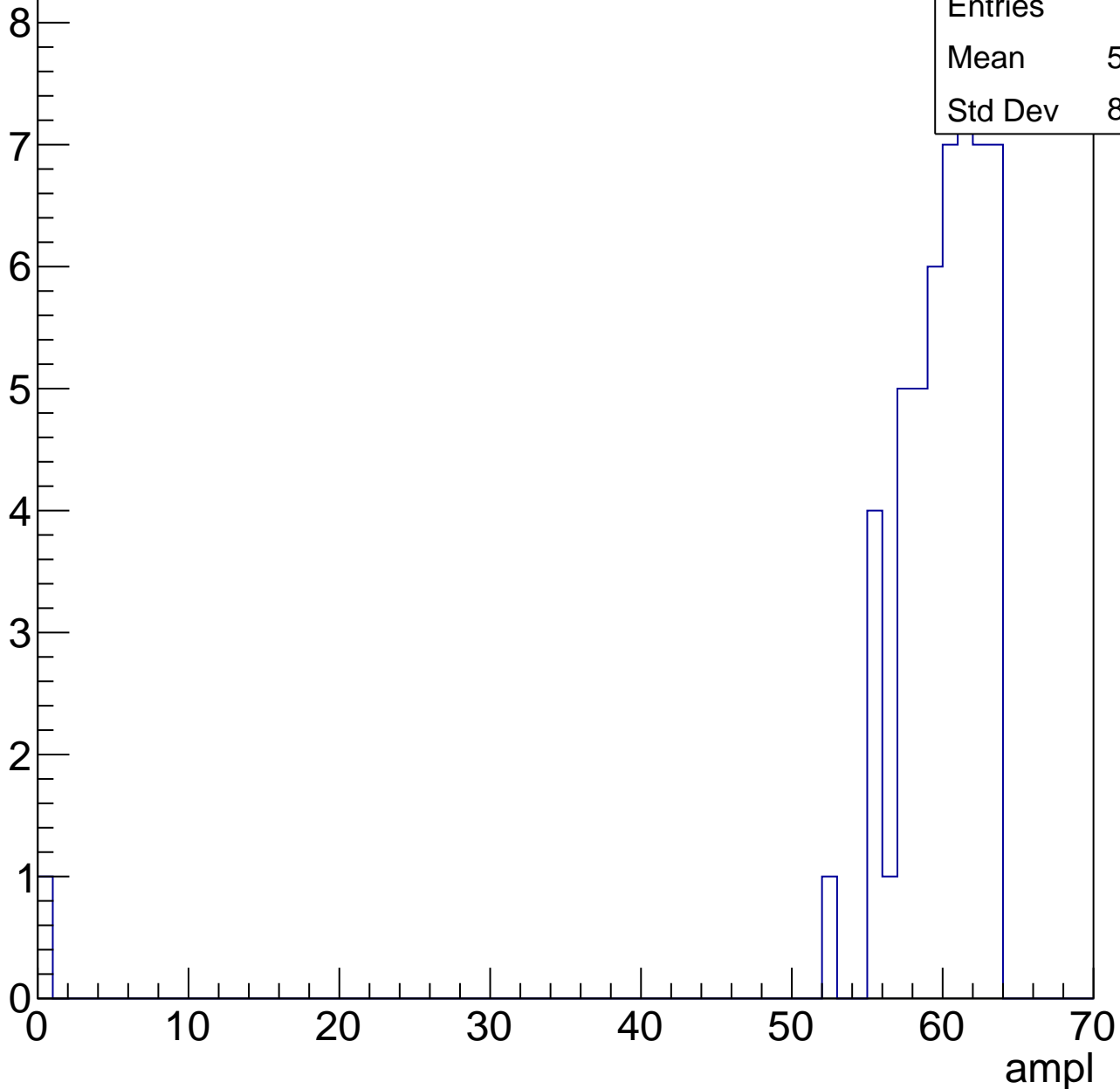


# B1L103S, U25-ch38, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	52
Mean	58.46
Std Dev	8.579



# B1L103S, U25-ch38, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

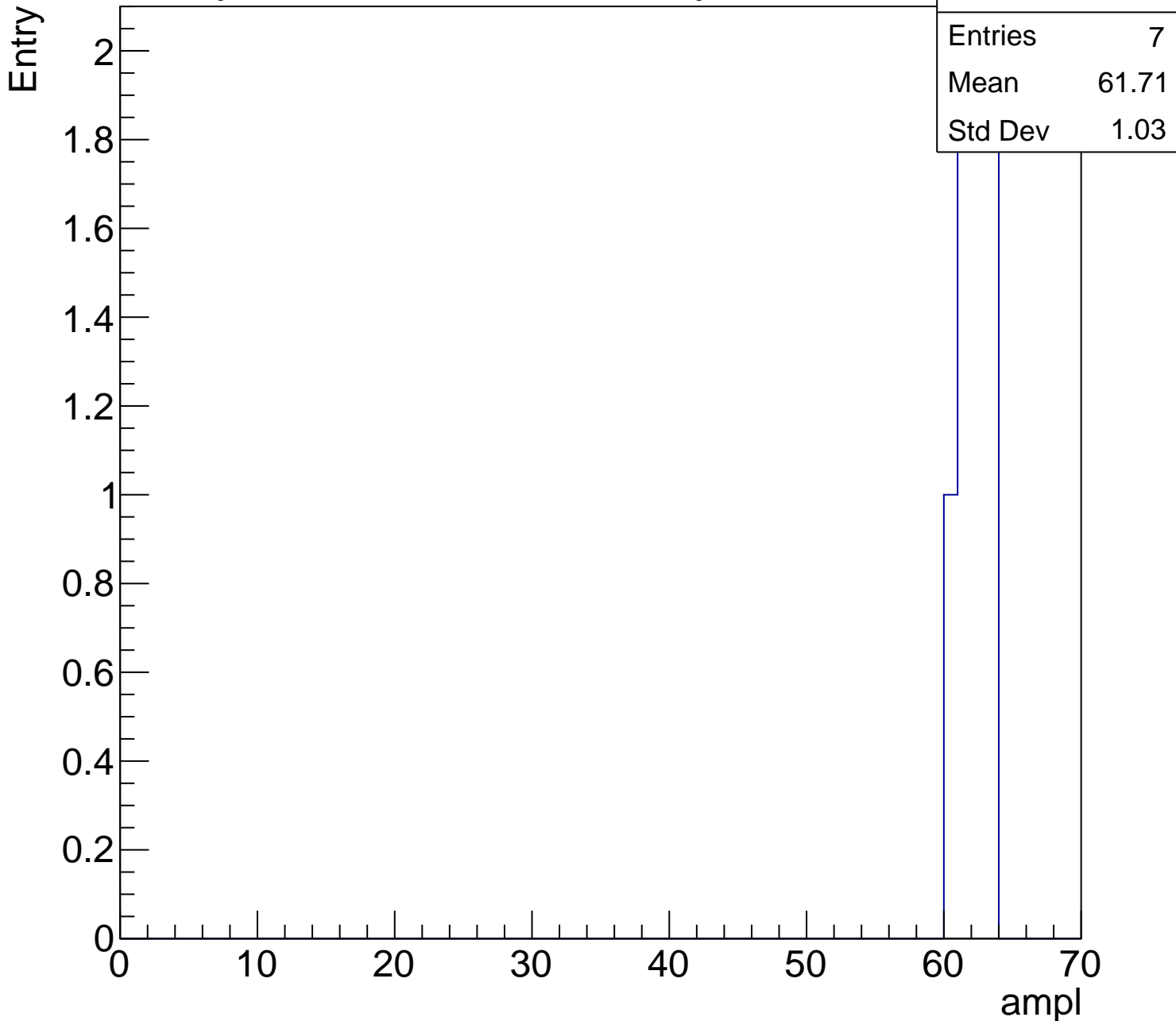
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	7
Mean	61.71
Std Dev	1.03

0 10 20 30 40 50 60 70

ampl



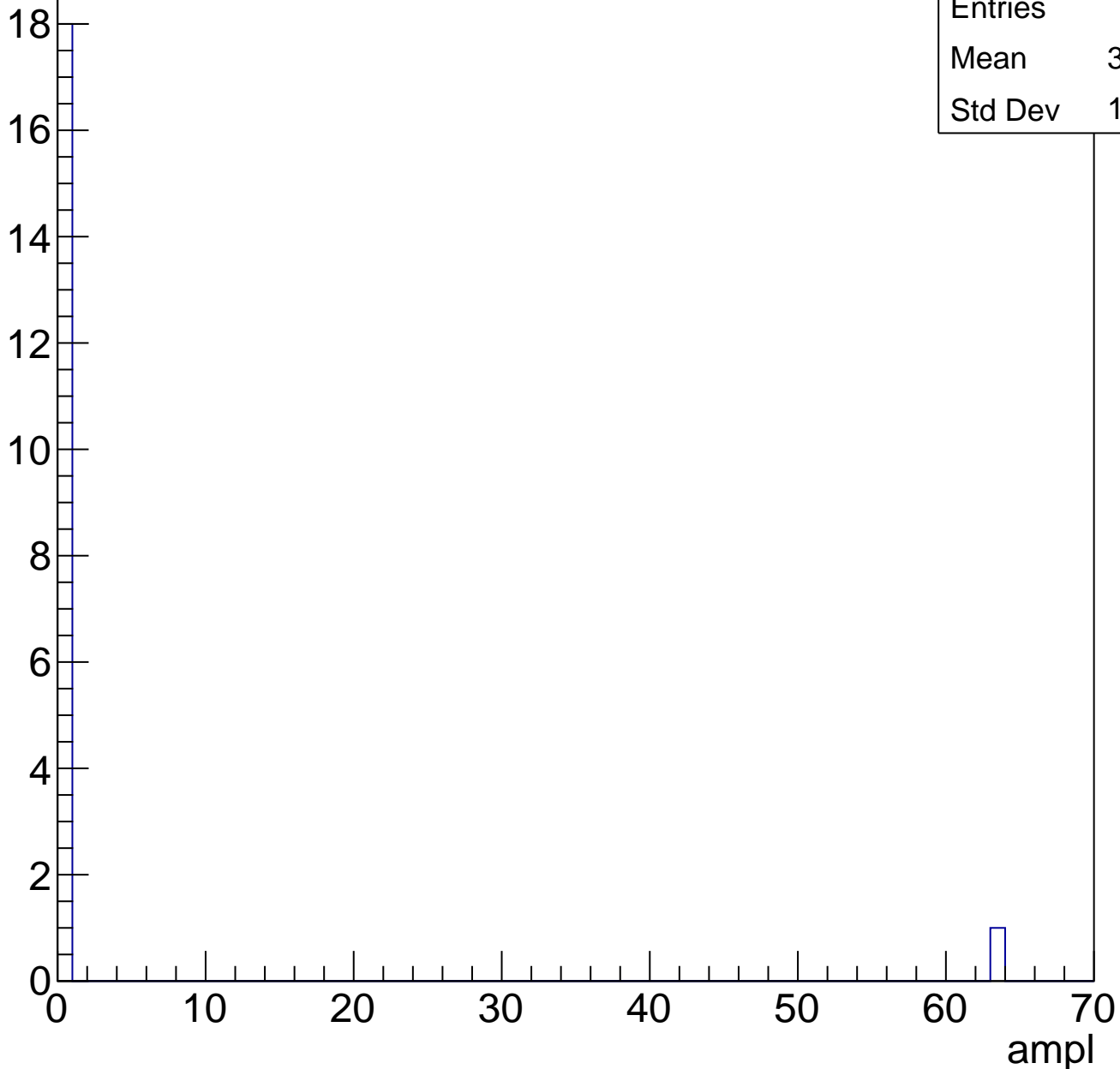


# B1L103S, U25-ch38, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	19
Mean	3.316
Std Dev	14.07

Entry

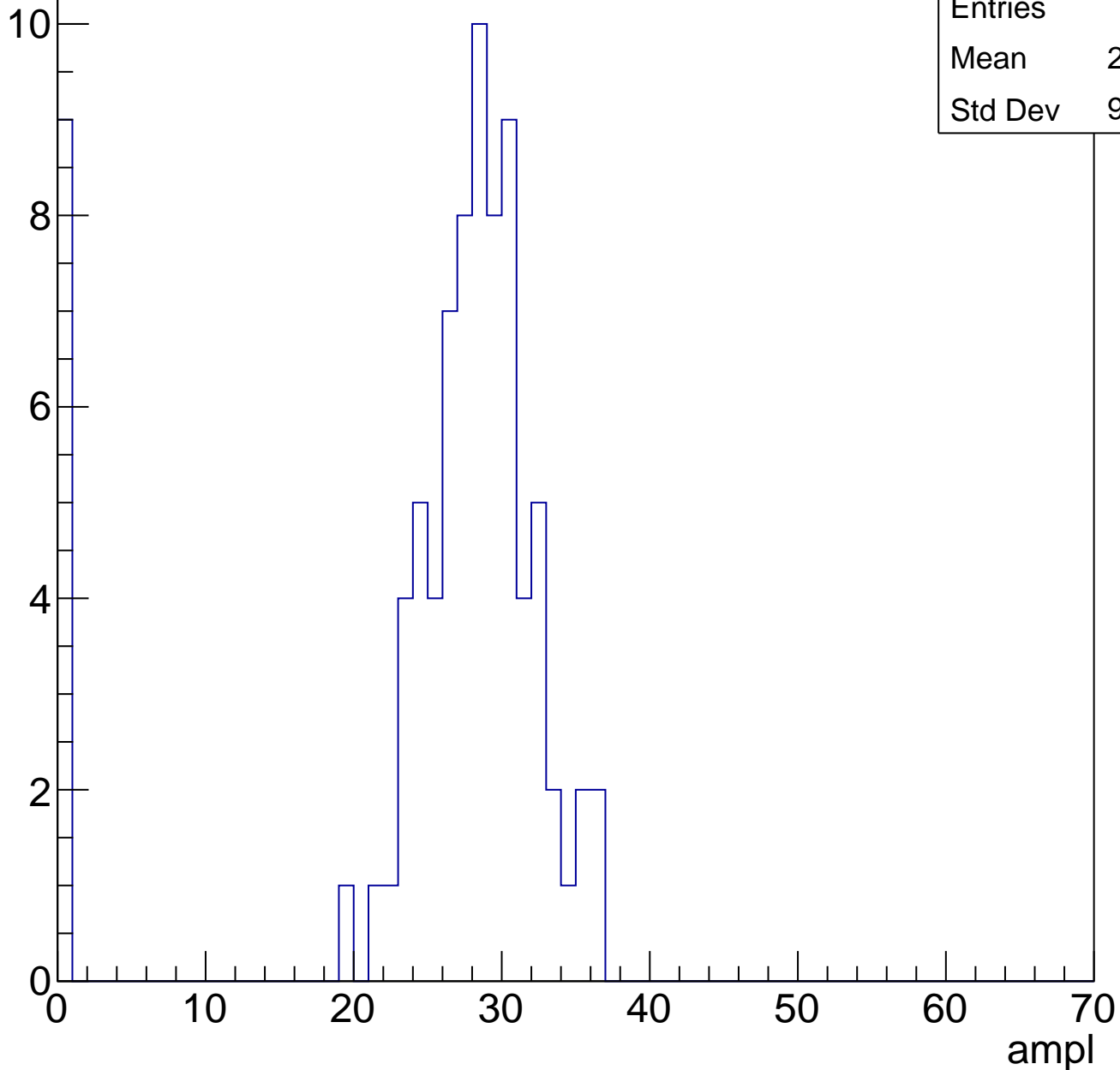


# B1L103S, U25-ch39, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	83
Mean	25.06
Std Dev	9.332

Entry

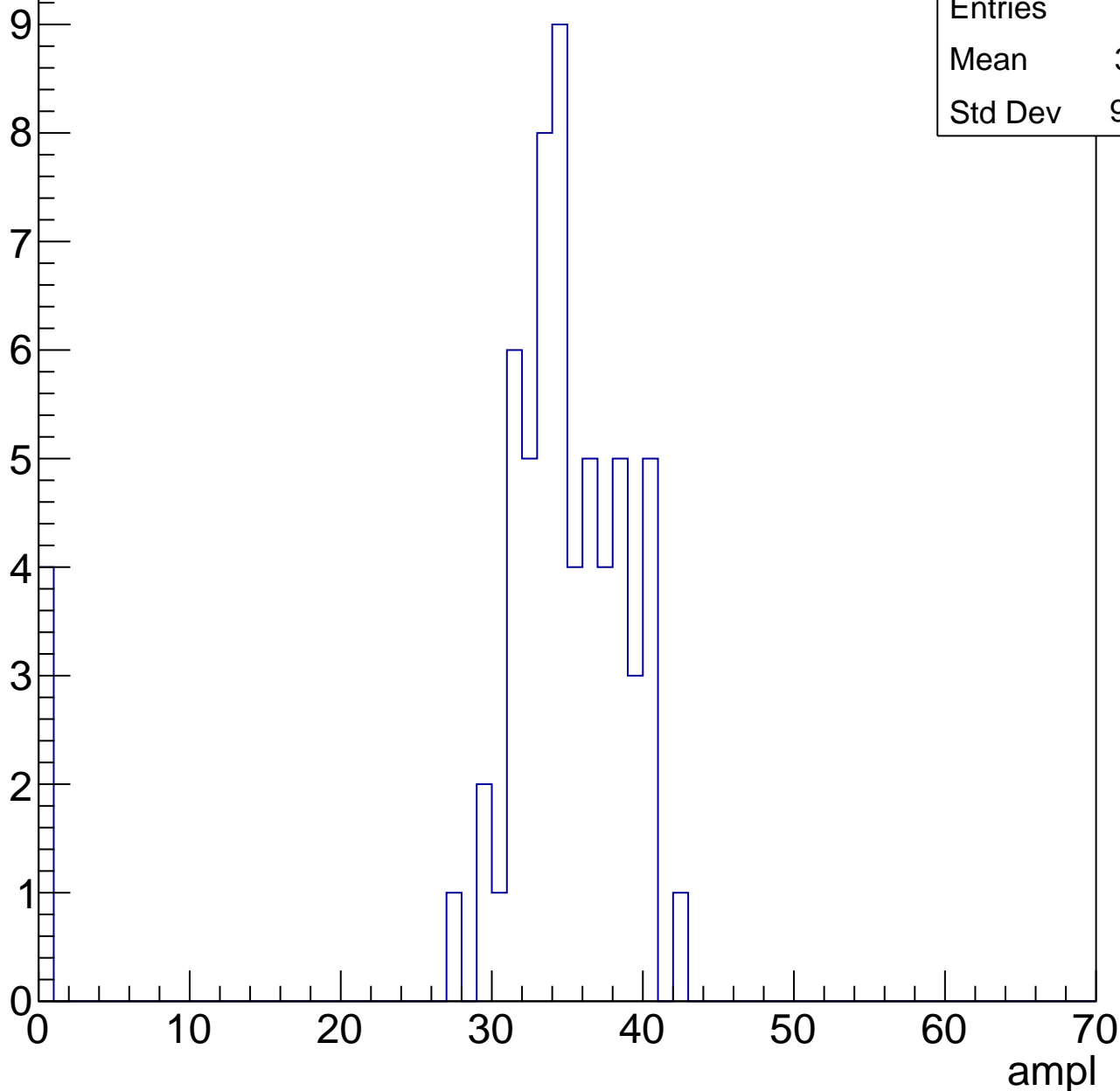


# B1L103S, U25-ch39, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	63
Mean	32.51
Std Dev	9.032



# B1L103S, U25-ch39, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	94
Mean	36.71
Std Dev	13.76

Entry

10

8

6

4

2

0

0

10

20

30

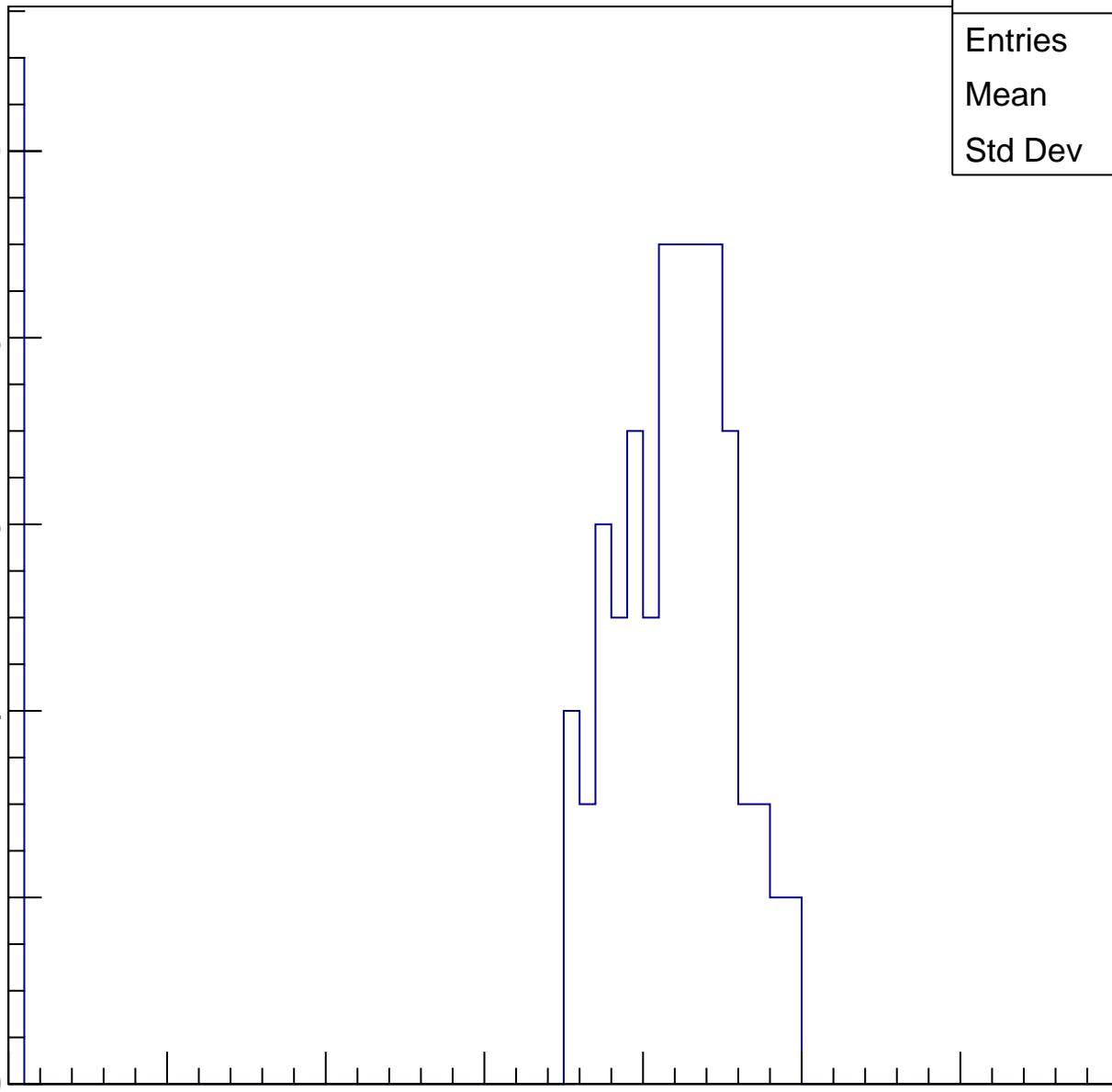
40

50

60

70

ampl

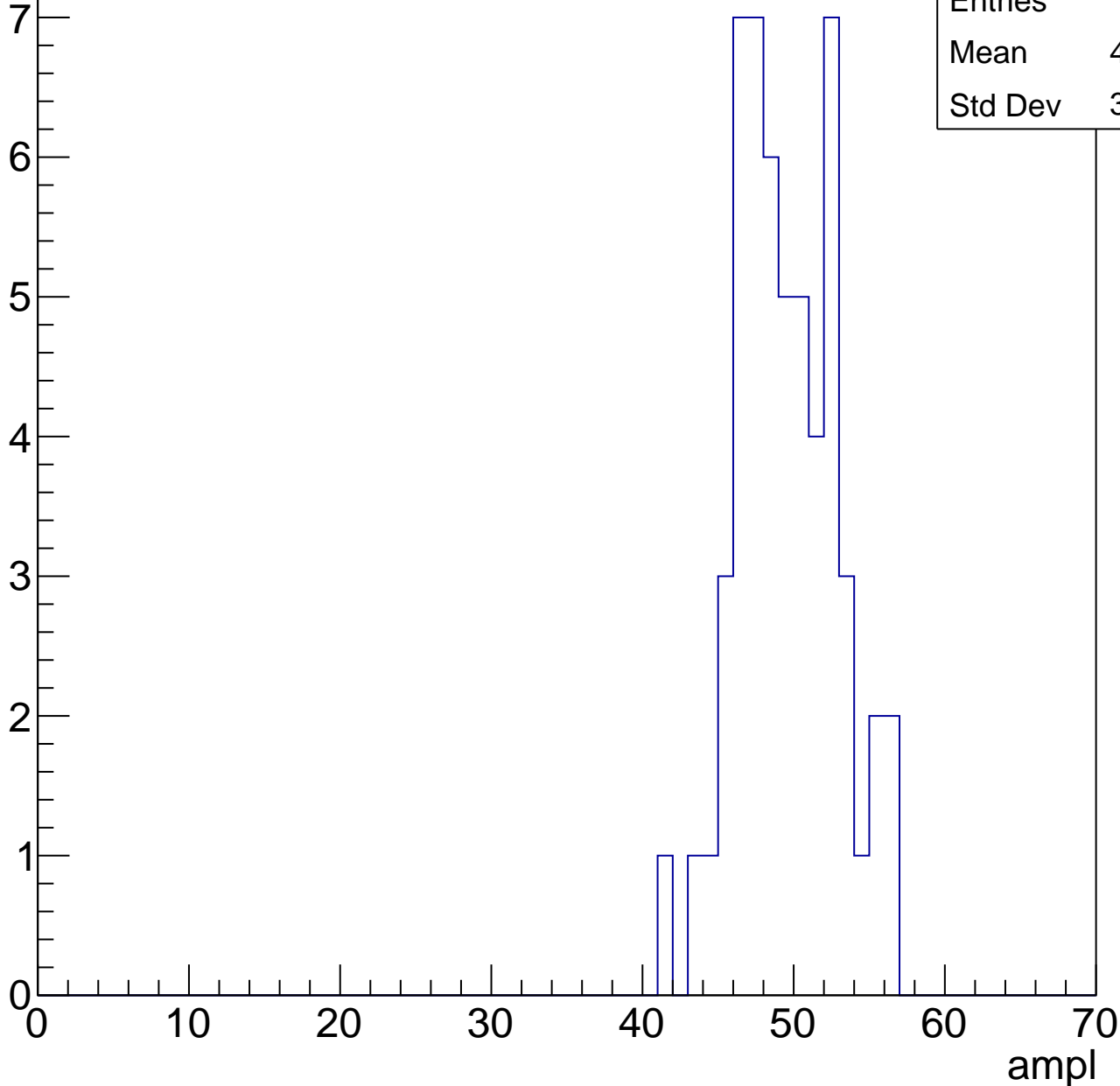


# B1L103S, U25-ch39, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	55
Mean	49.09
Std Dev	3.293

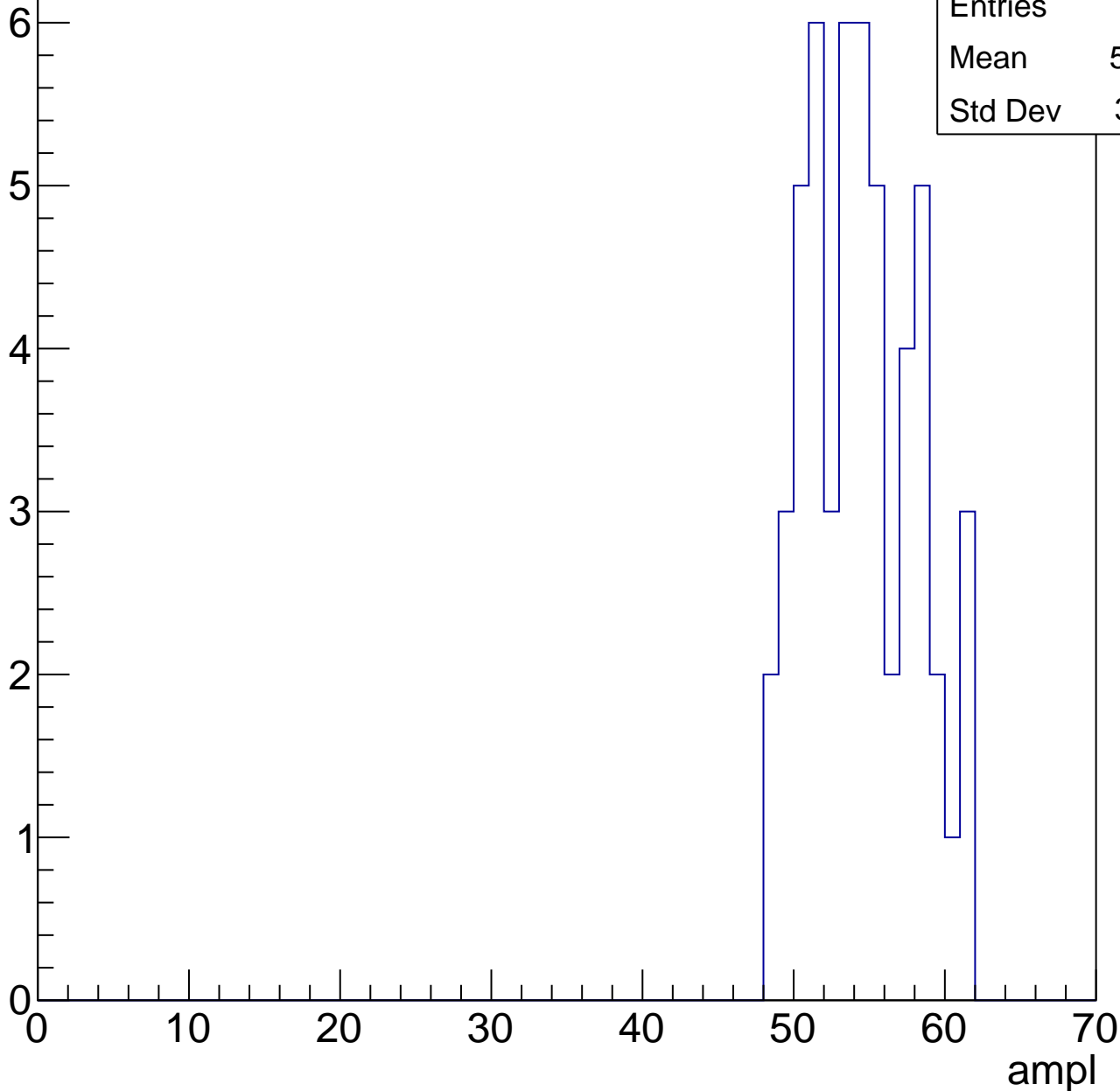


# B1L103S, U25-ch39, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	53
Mean	54.02
Std Dev	3.531

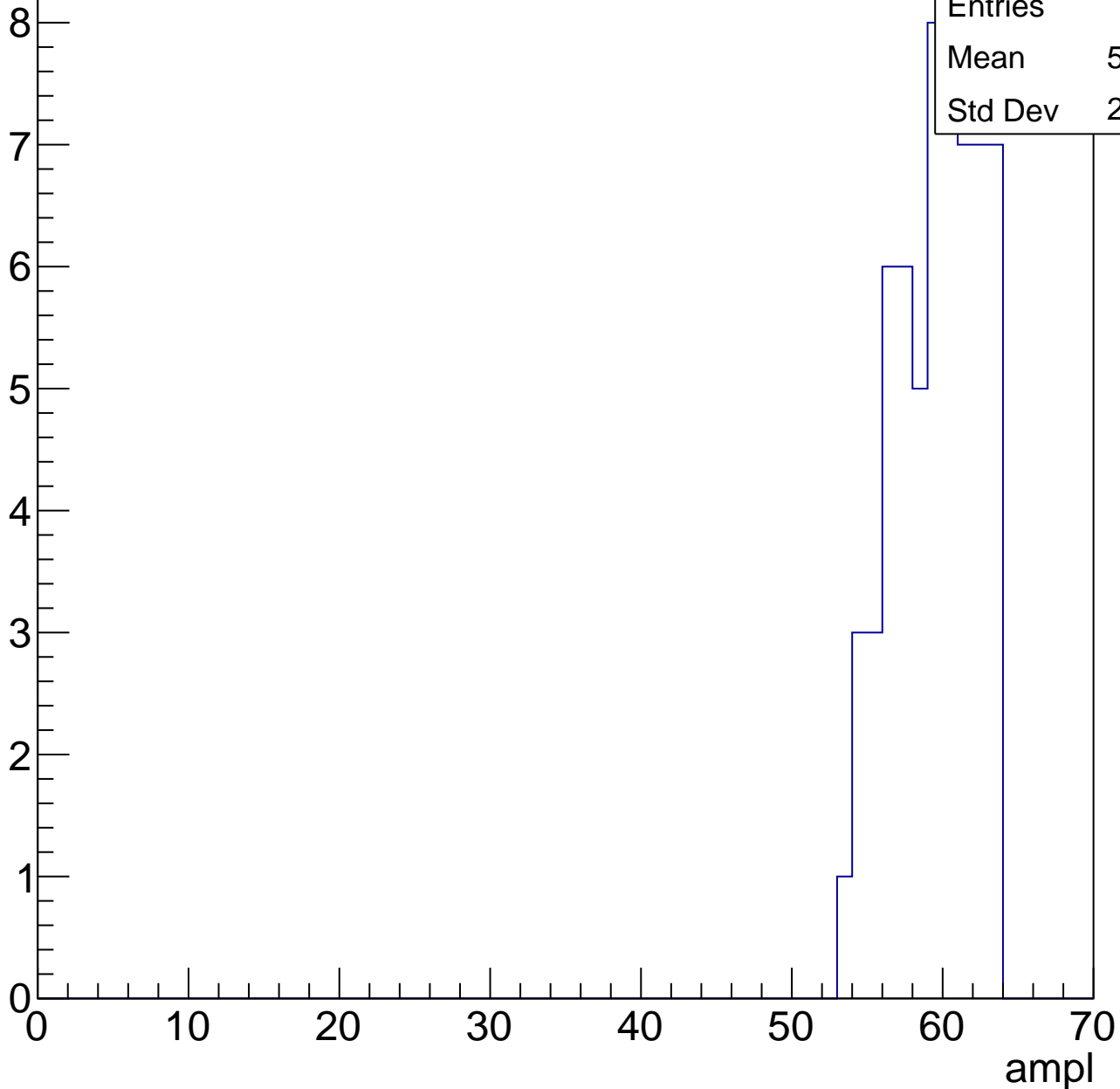


# B1L103S, U25-ch39, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

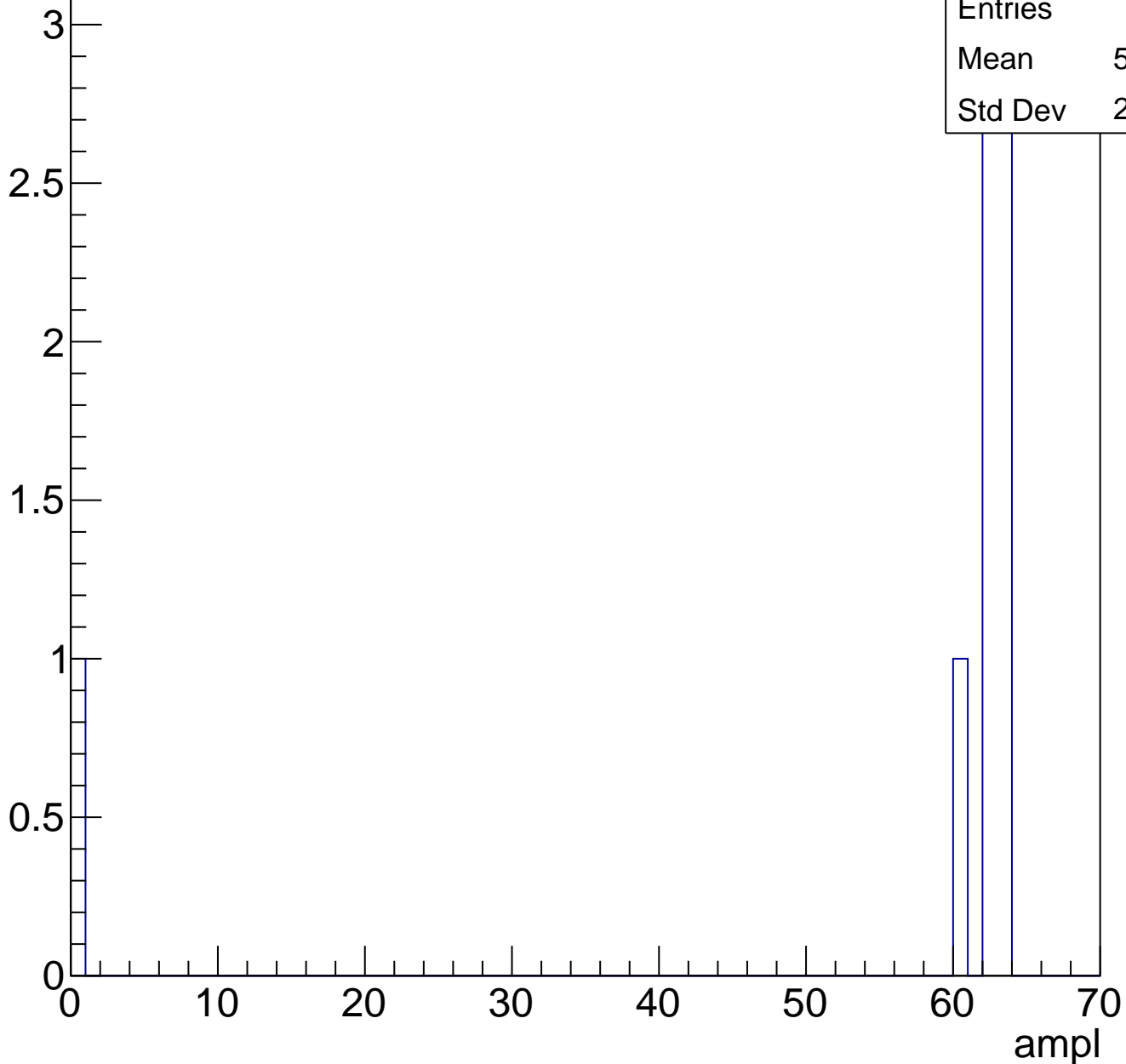
Entries	61
Mean	59.05
Std Dev	2.725



# B1L103S, U25-ch39, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U25-ch39, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

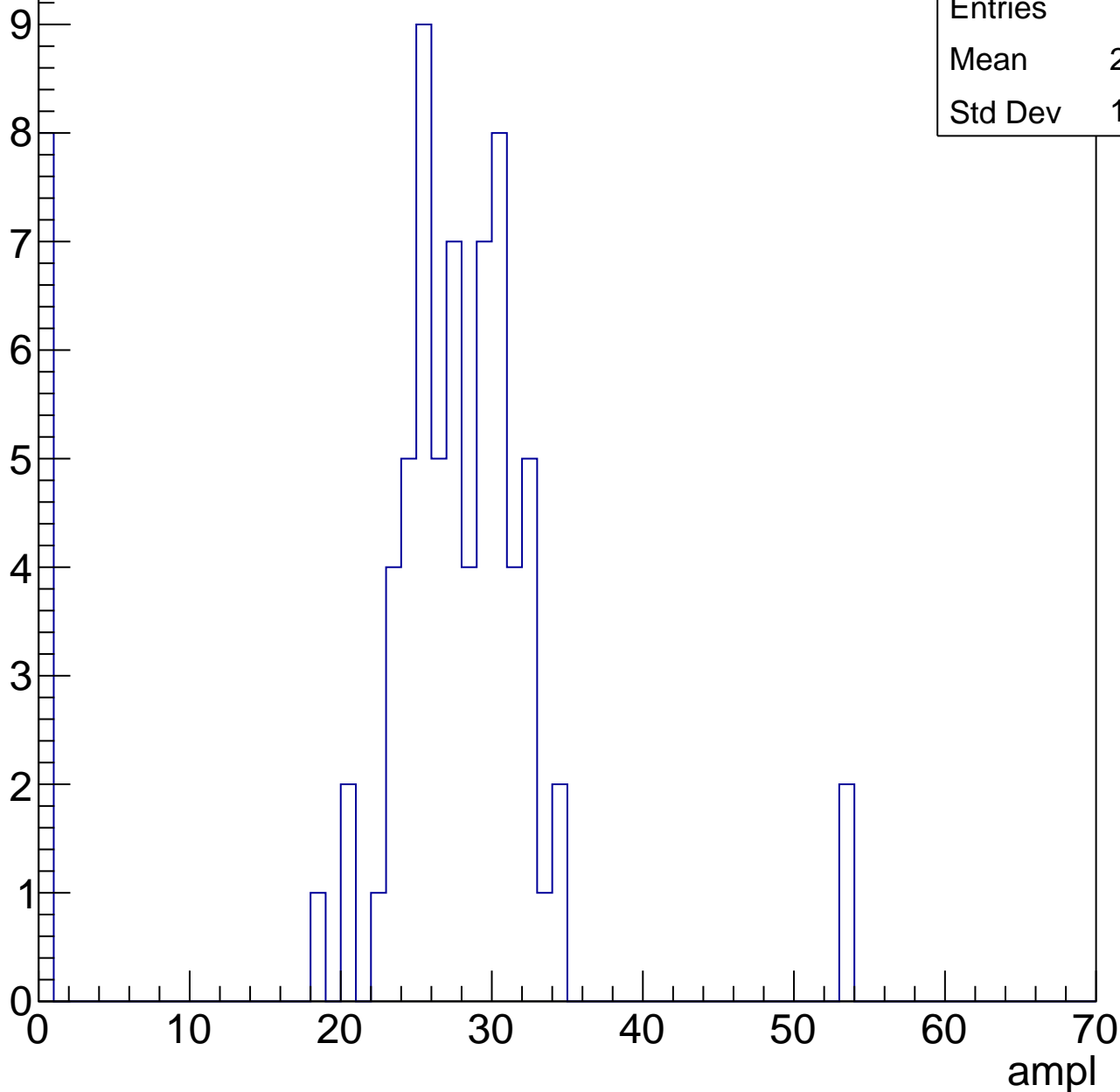


# B1L103S, U25-ch40, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	75
Mean	25.09
Std Dev	10.13

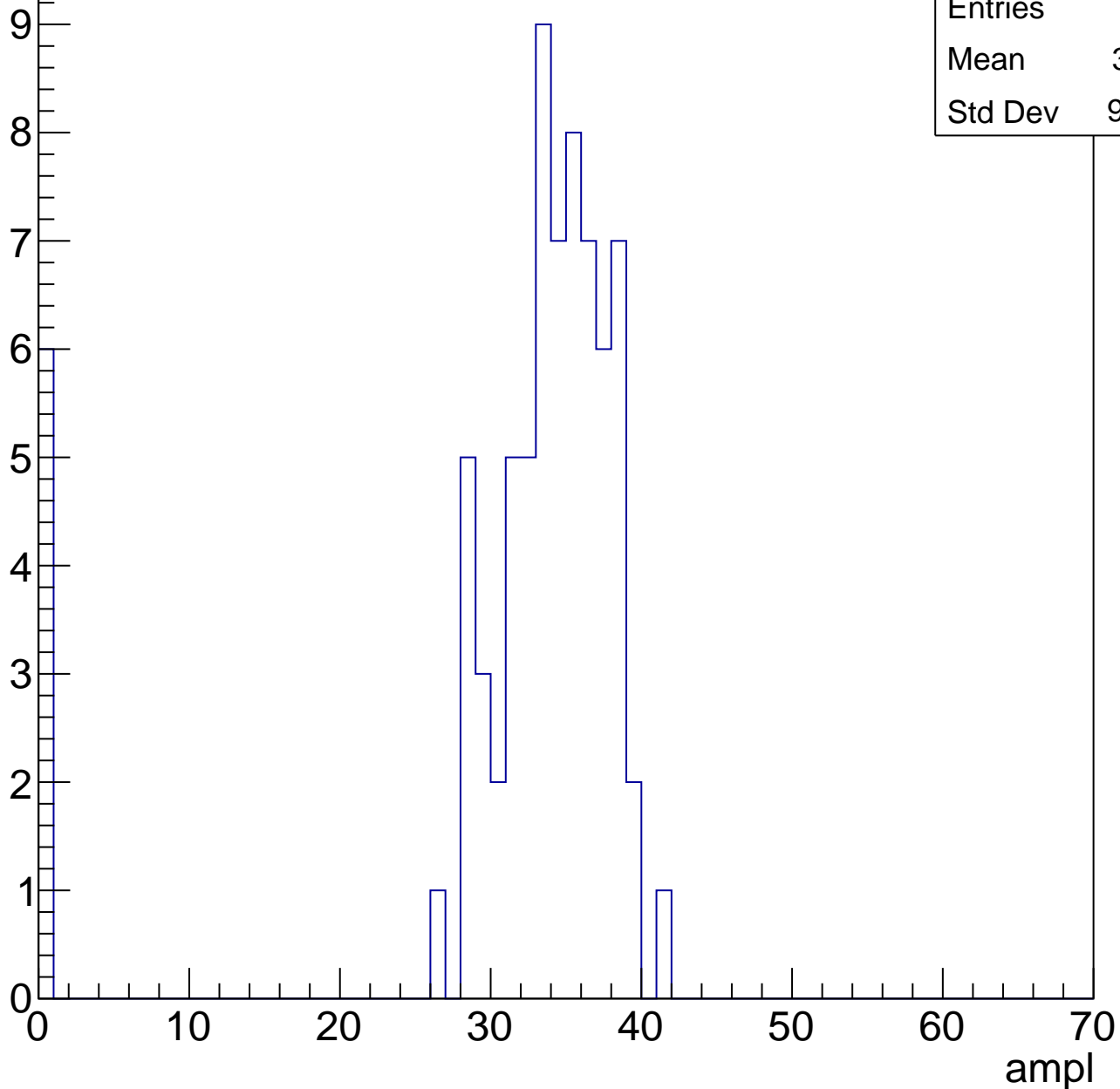


# B1L103S, U25-ch40, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	74
Mean	31.11
Std Dev	9.756

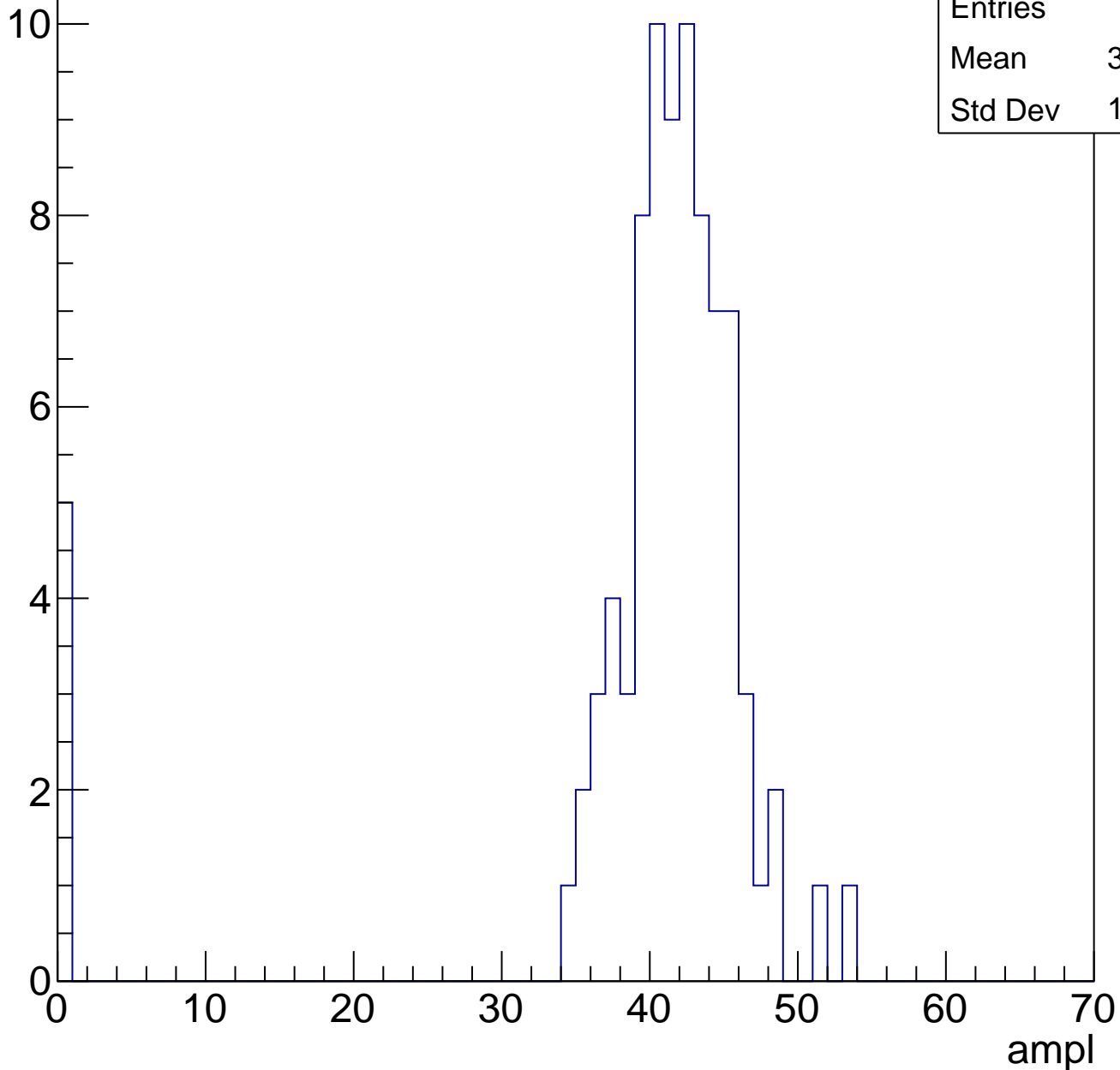


# B1L103S, U25-ch40, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	85
Mean	39.14
Std Dev	10.35

Entry



# B1L103S, U25-ch40, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

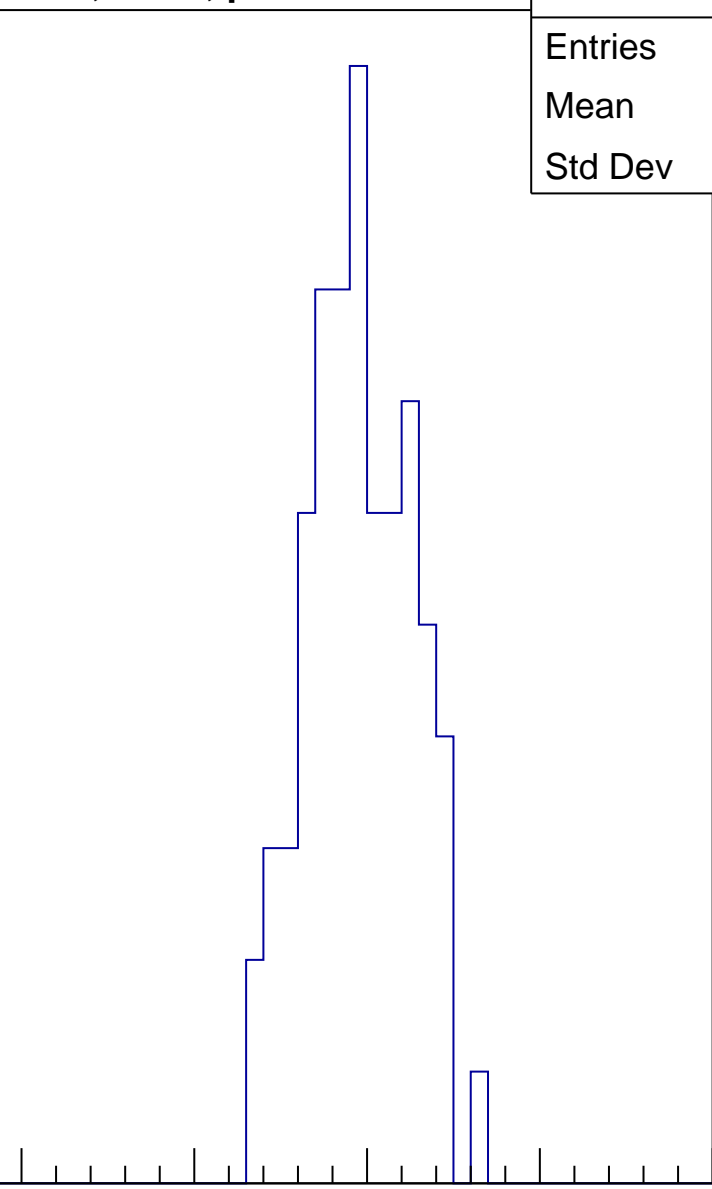
Entries	69
Mean	49.07
Std Dev	2.975

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

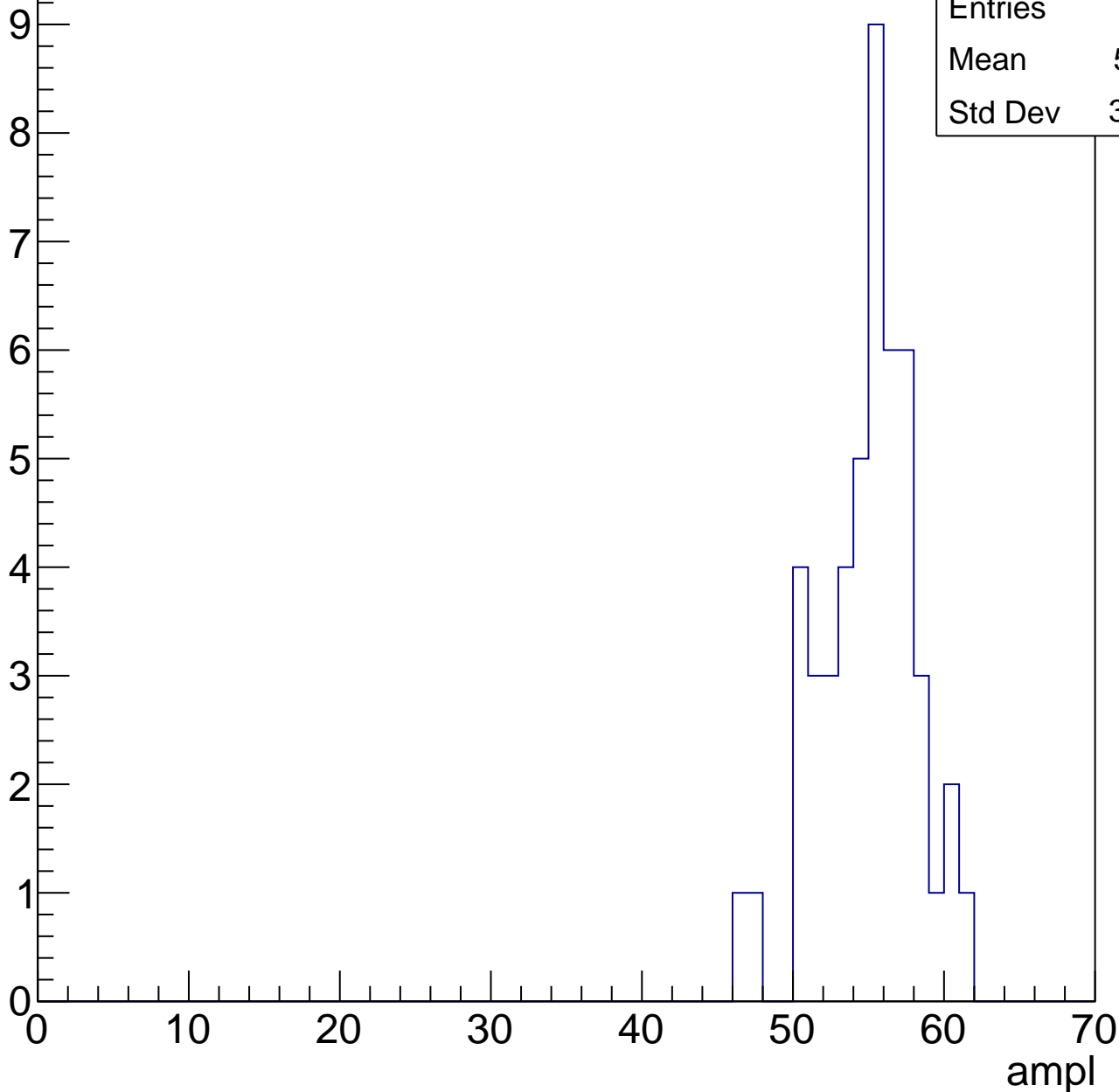


# B1L103S, U25-ch40, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	49
Mean	54.51
Std Dev	3.157

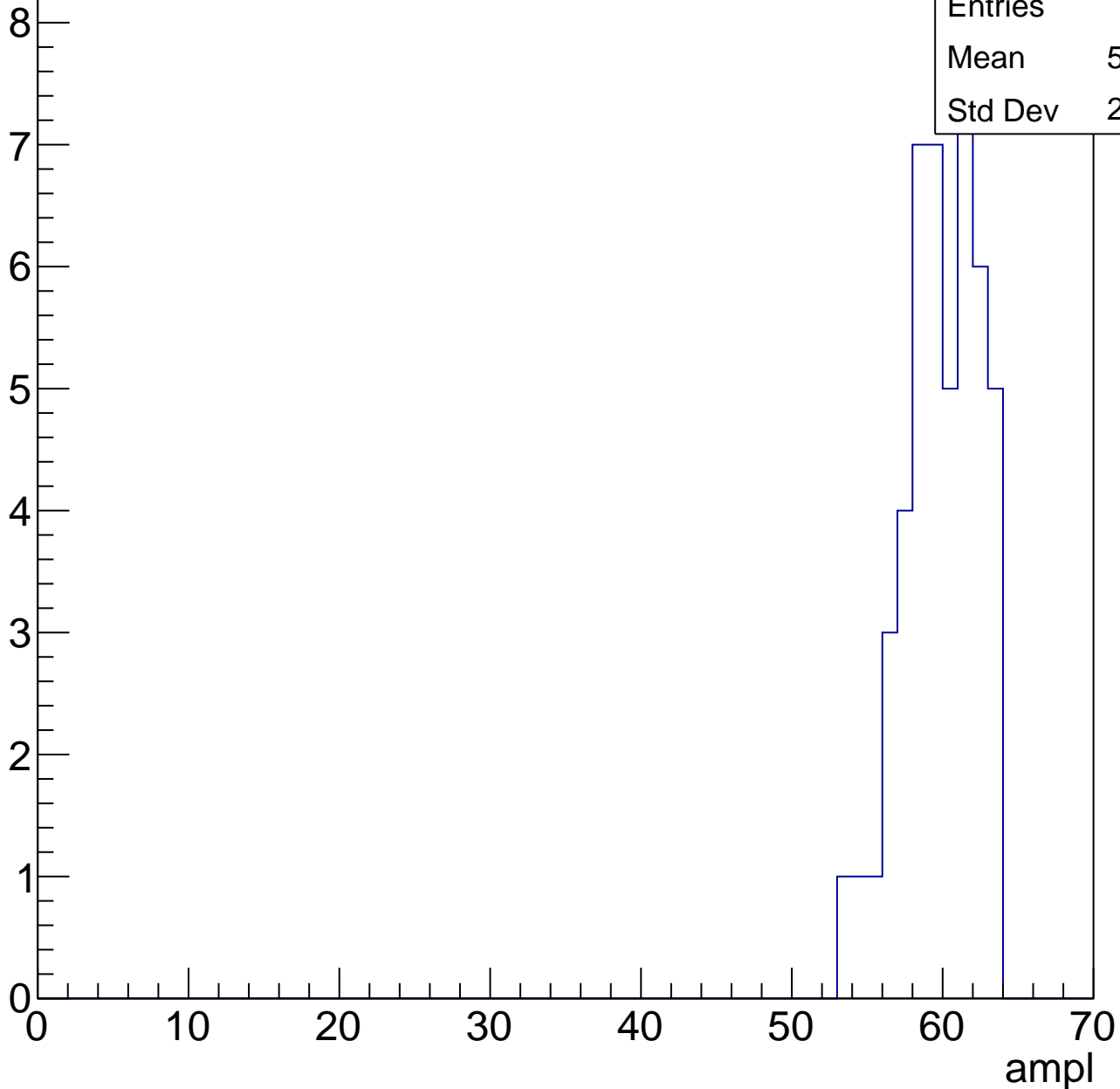


# B1L103S, U25-ch40, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	48
Mean	59.42
Std Dev	2.457

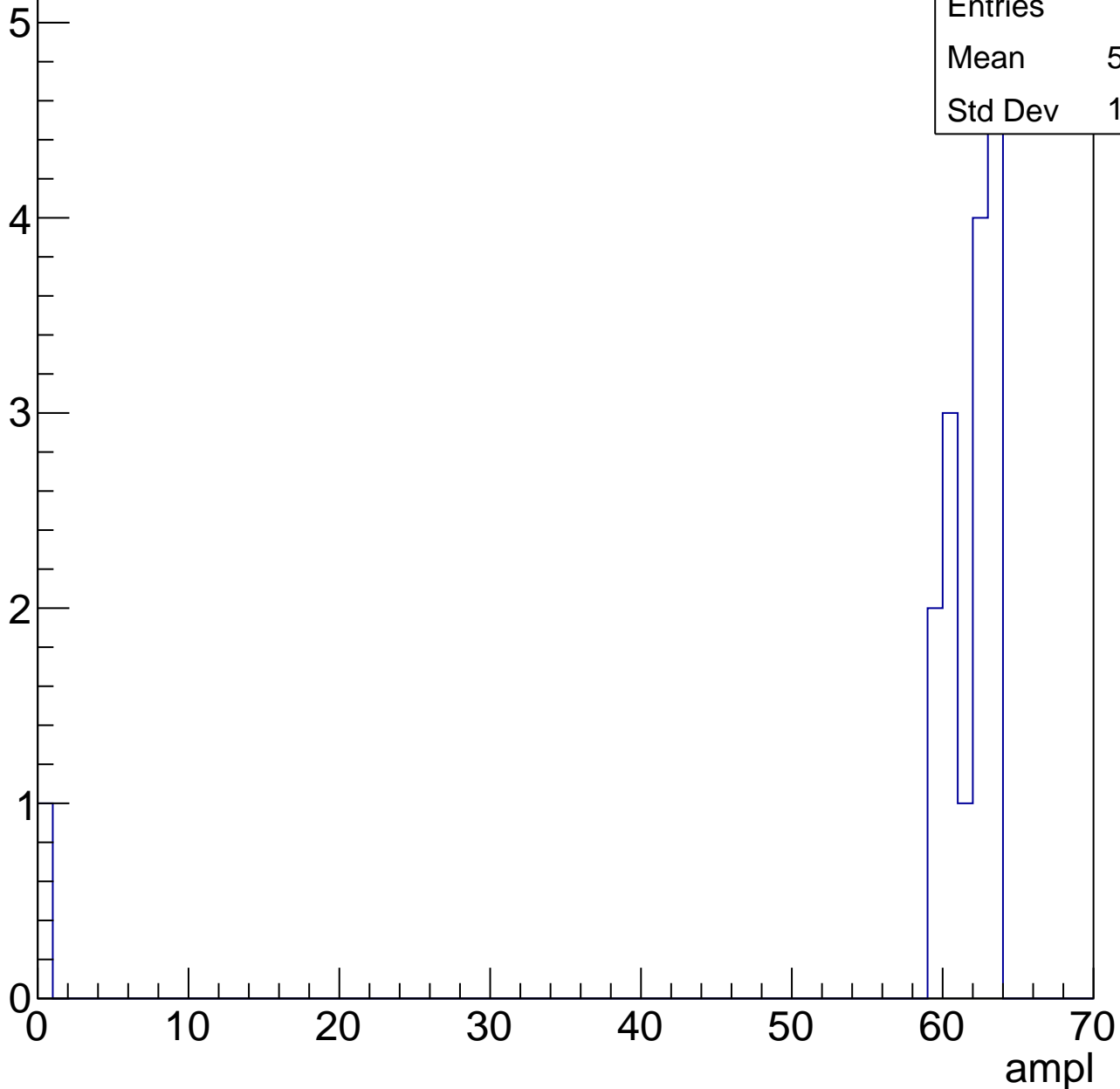


# B1L103S, U25-ch40, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	16
Mean	57.62
Std Dev	14.95





# B1L103S, U25-ch40, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

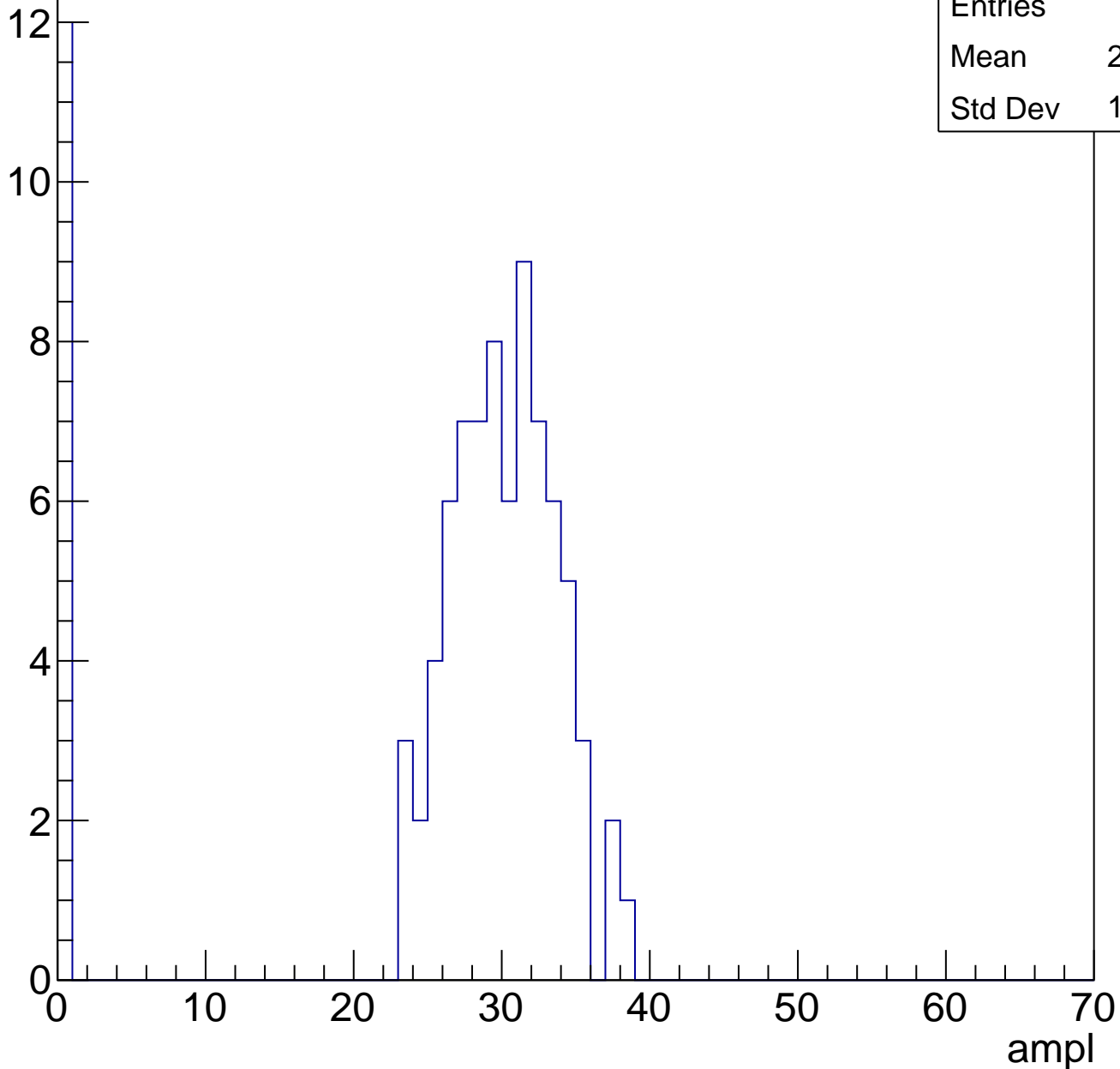
Entries	19
Mean	0
Std Dev	0

# B1L103S, U25-ch41, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	88
Mean	25.66
Std Dev	10.69

Entry



# B1L103S, U25-ch41, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	85
Mean	31.79
Std Dev	13.84

Entry

12

10

8

6

4

2

0

0

10

20

30

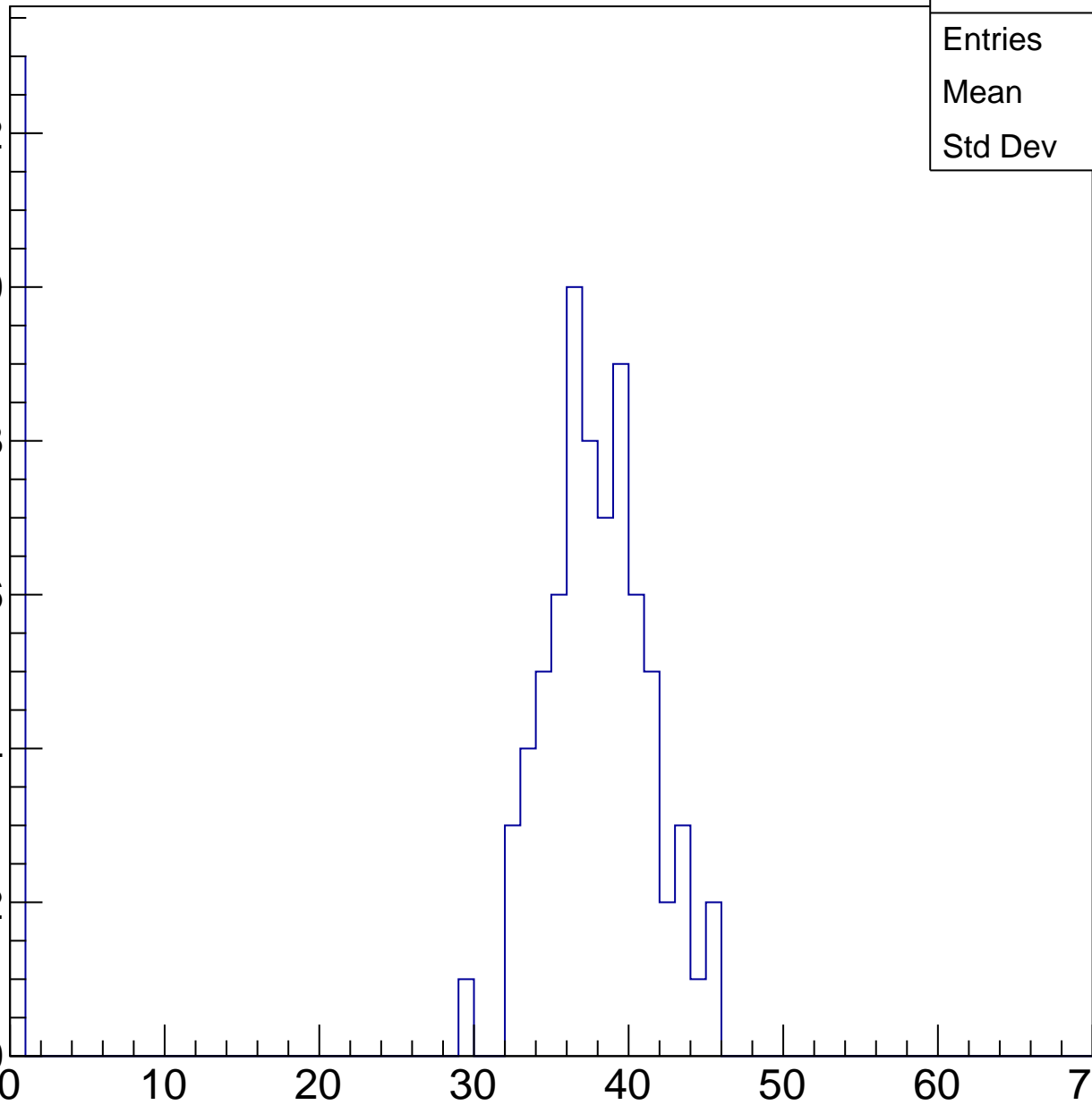
40

50

60

70

ampl

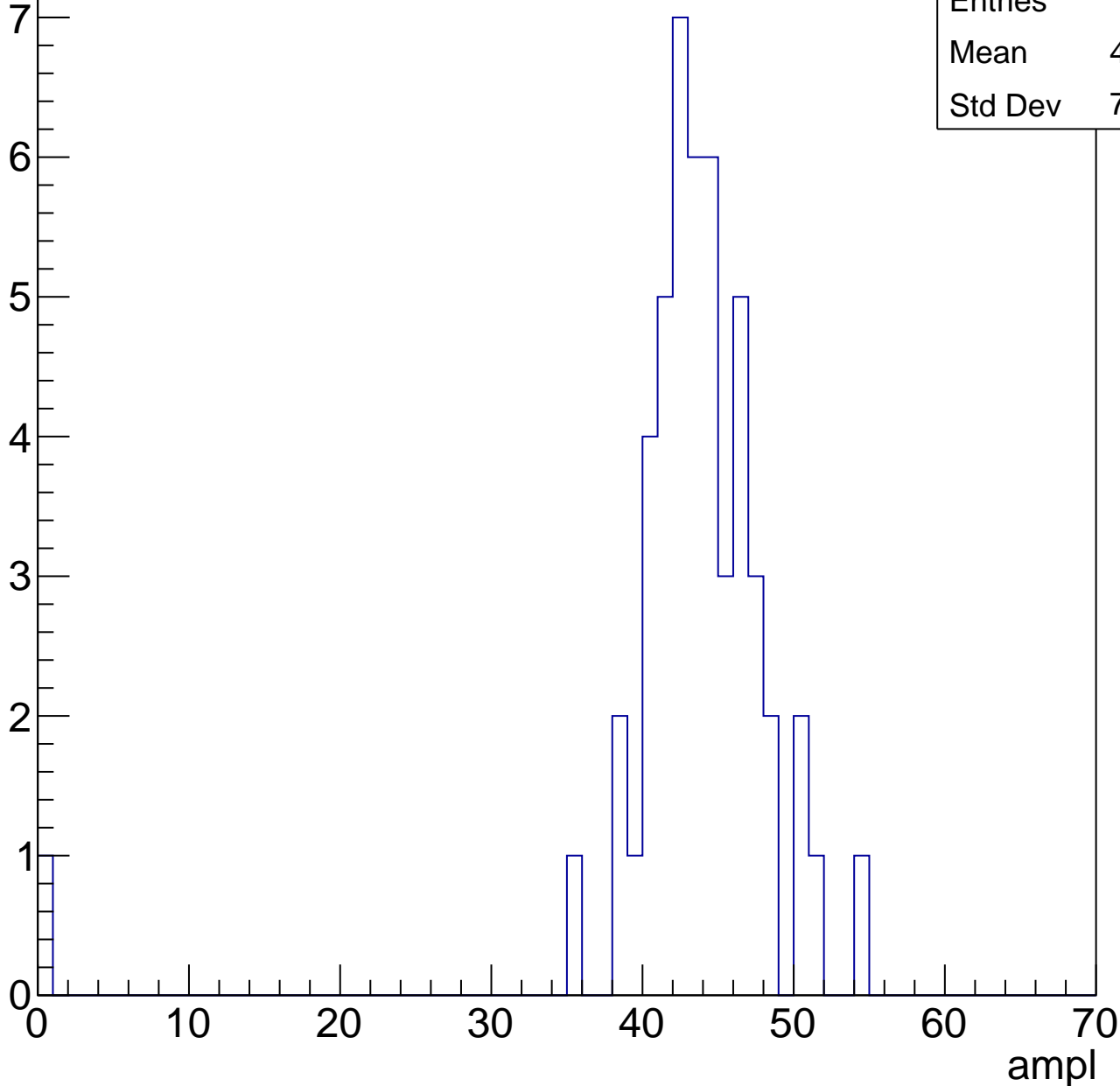


# B1L103S, U25-ch41, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	50
Mean	42.76
Std Dev	7.047

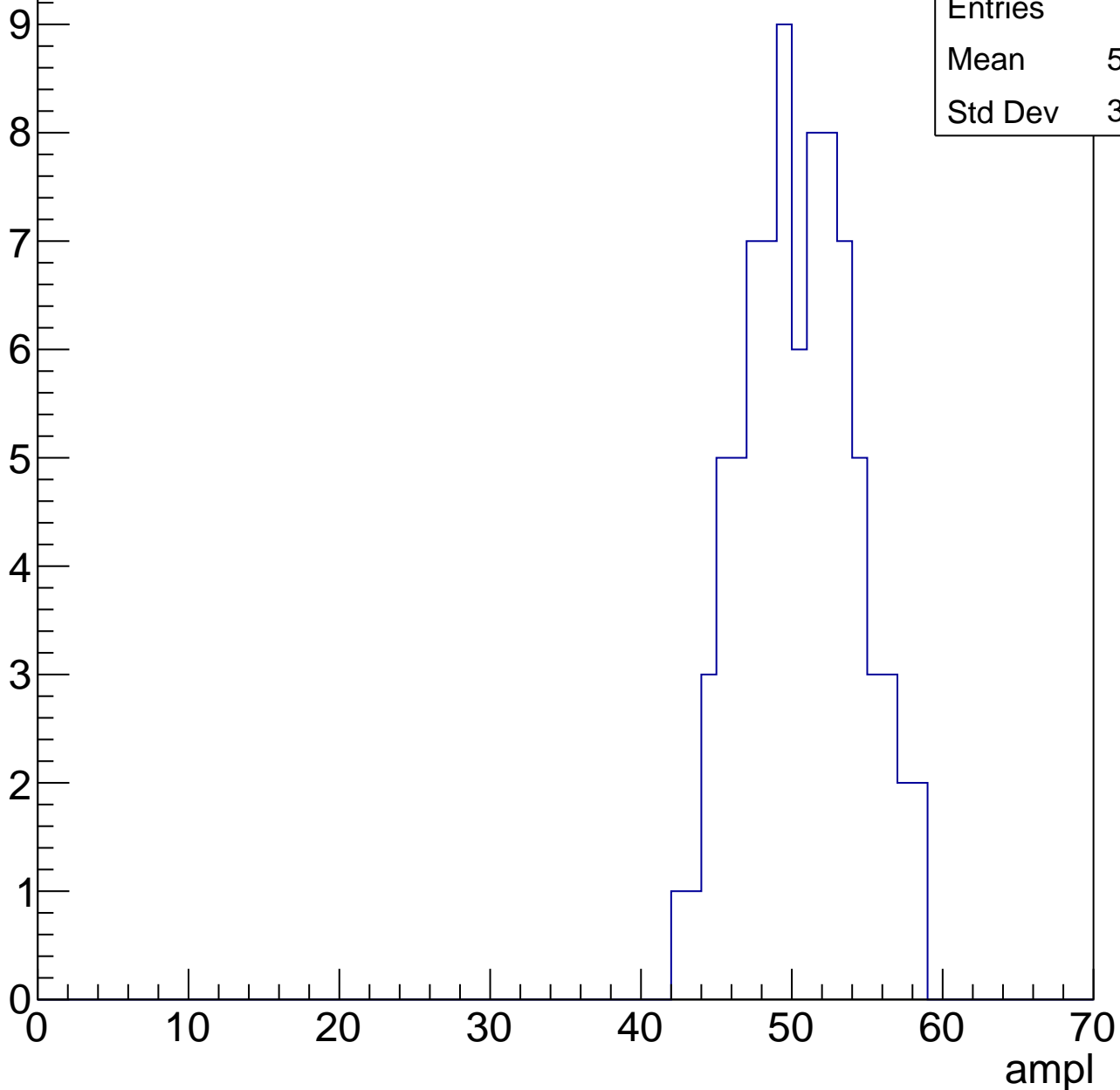


# B1L103S, U25-ch41, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	82
Mean	50.07
Std Dev	3.692

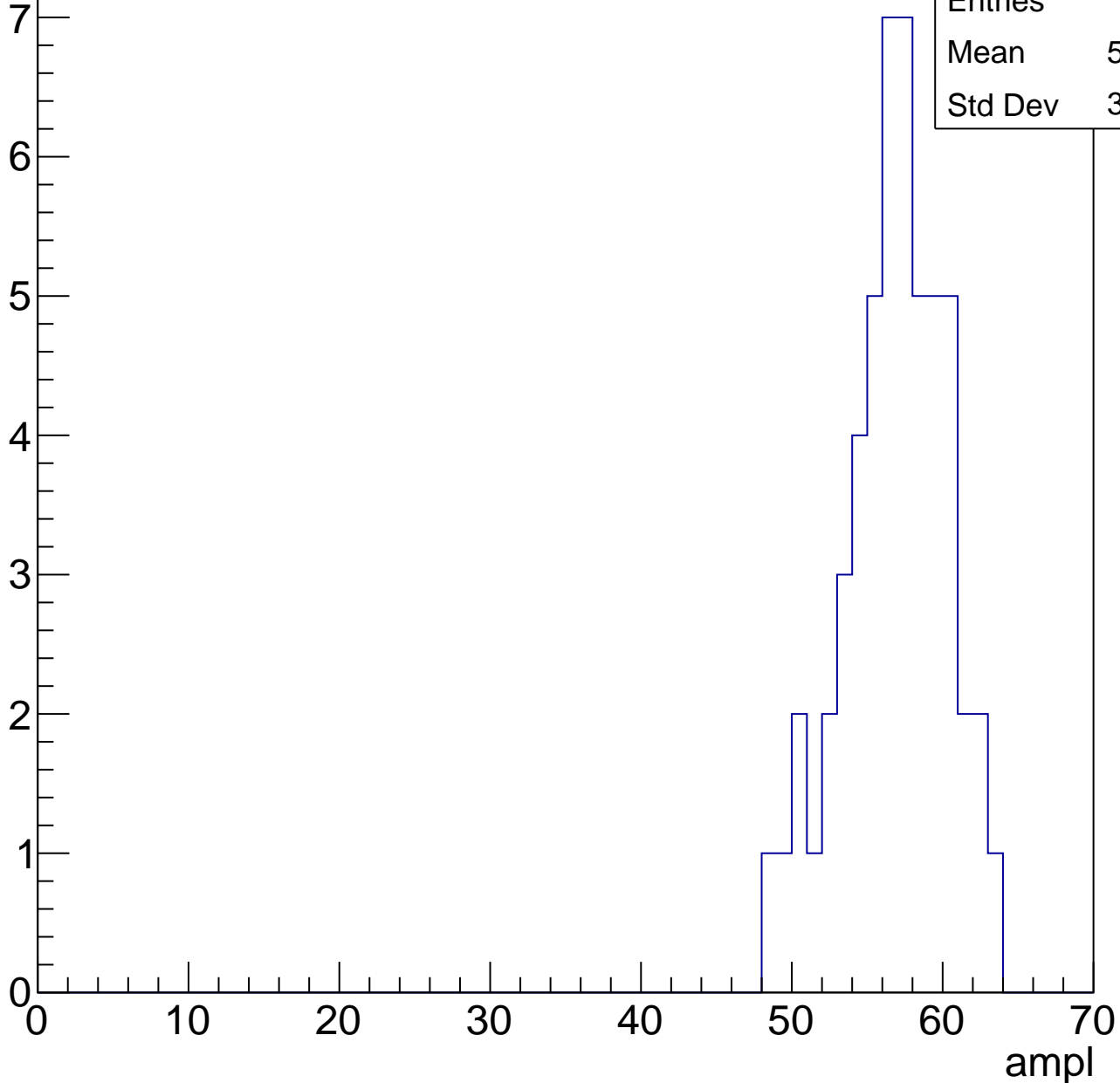


# B1L103S, U25-ch41, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	53
Mean	56.36
Std Dev	3.382

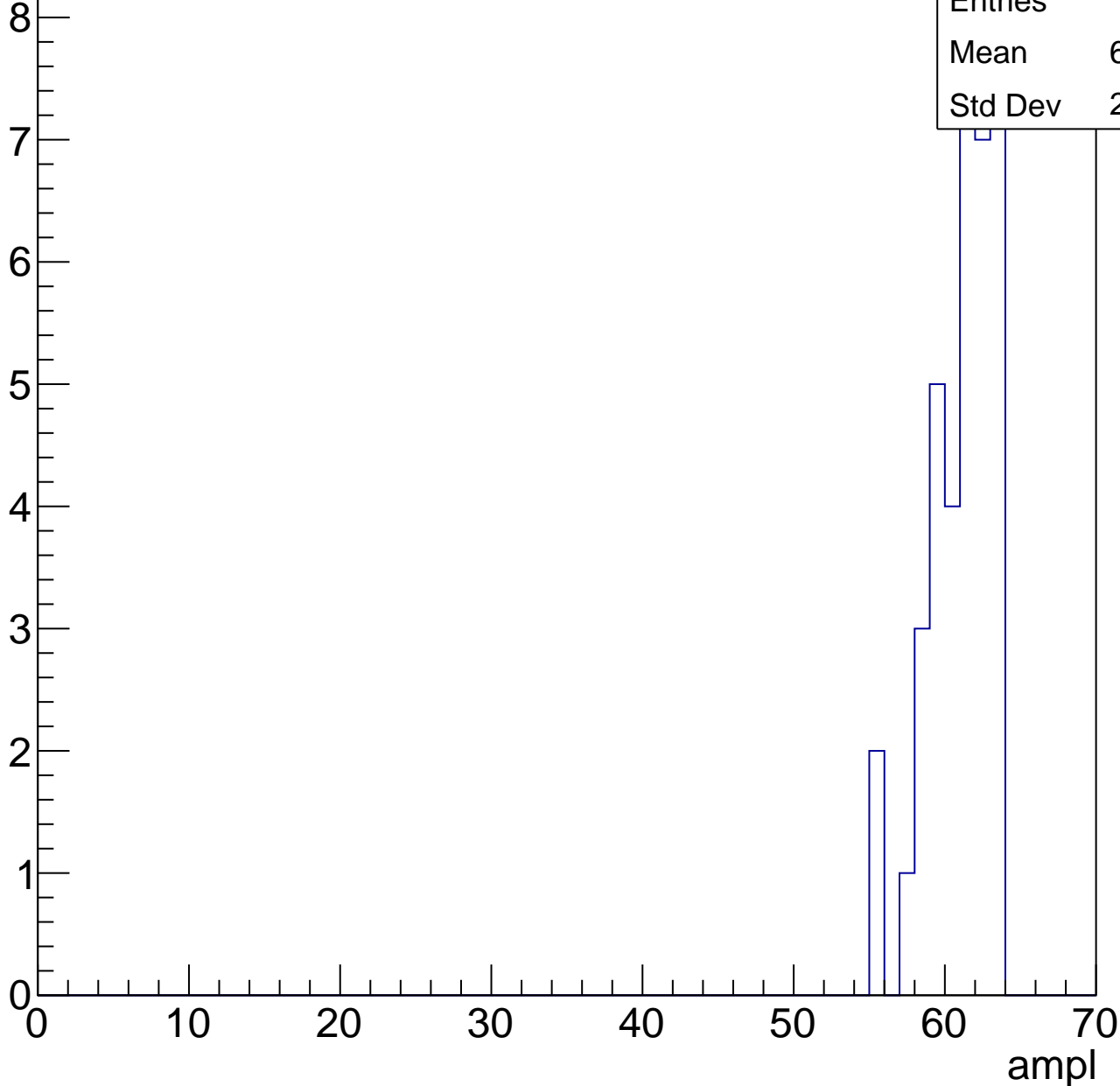


# B1L103S, U25-ch41, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

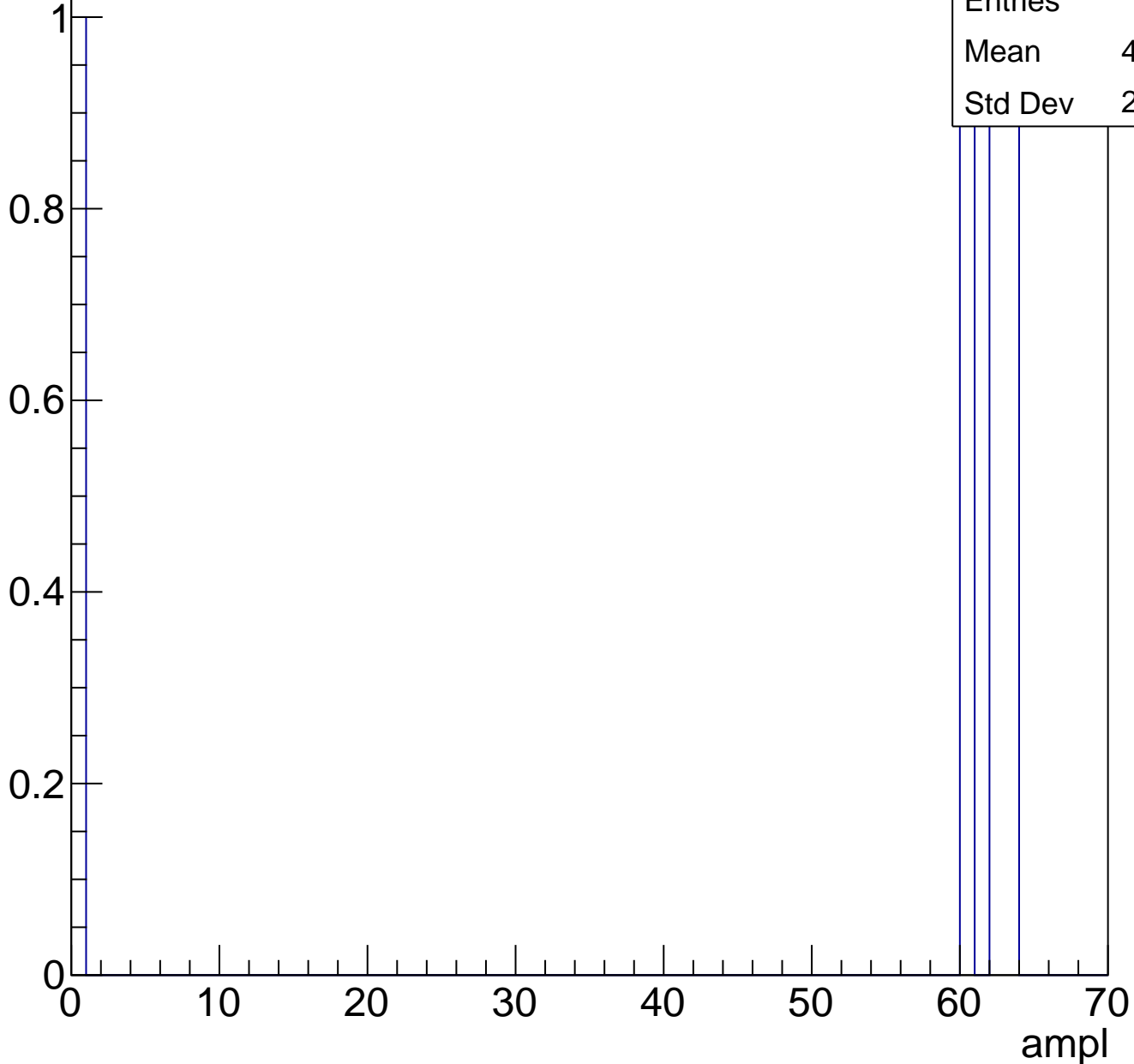
Entries	38
Mean	60.58
Std Dev	2.123



# B1L103S, U25-ch41, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U25-ch41, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

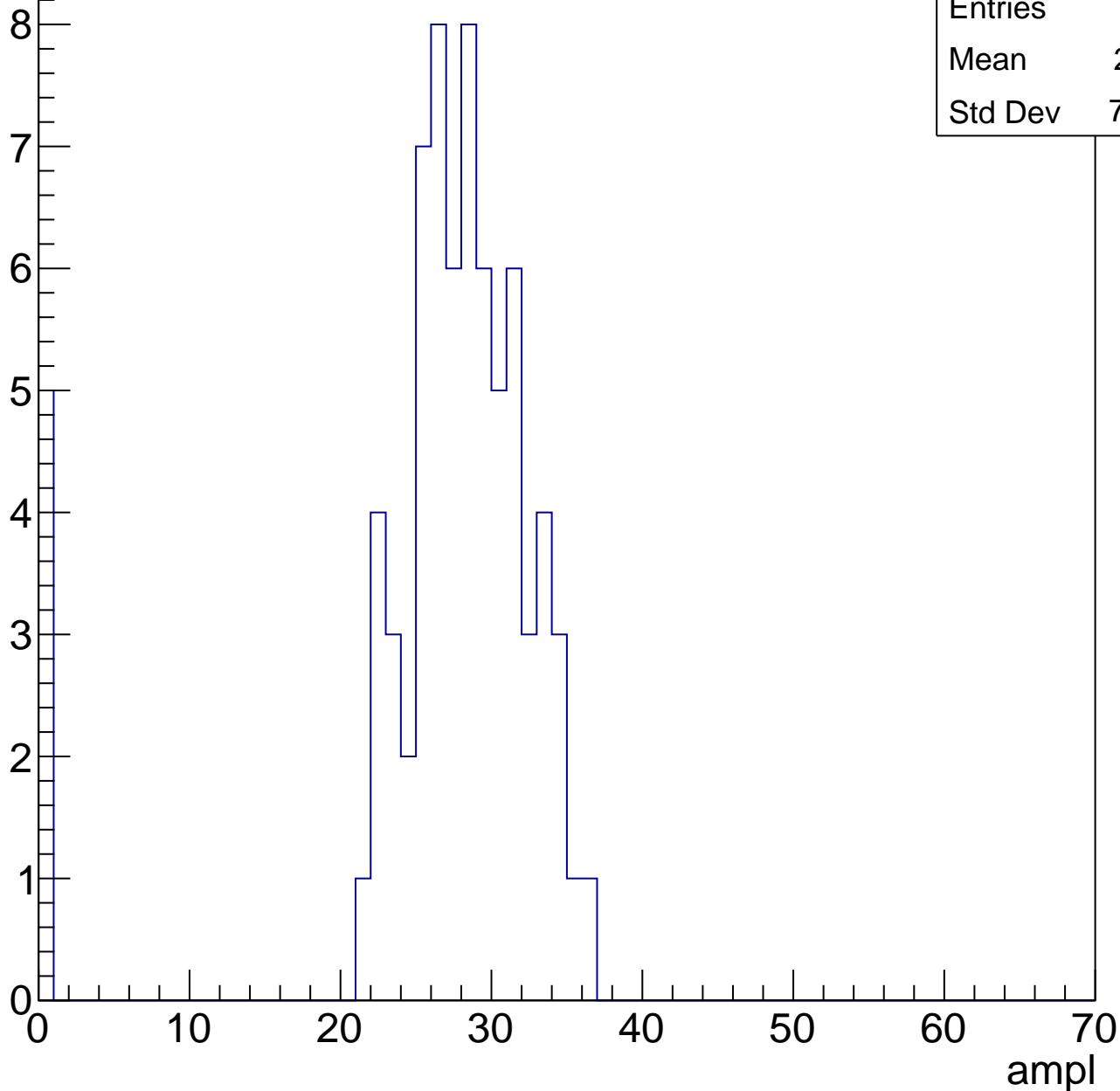
Entries	19
Mean	0
Std Dev	0

# B1L103S, U25-ch42, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	73
Mean	26.11
Std Dev	7.859

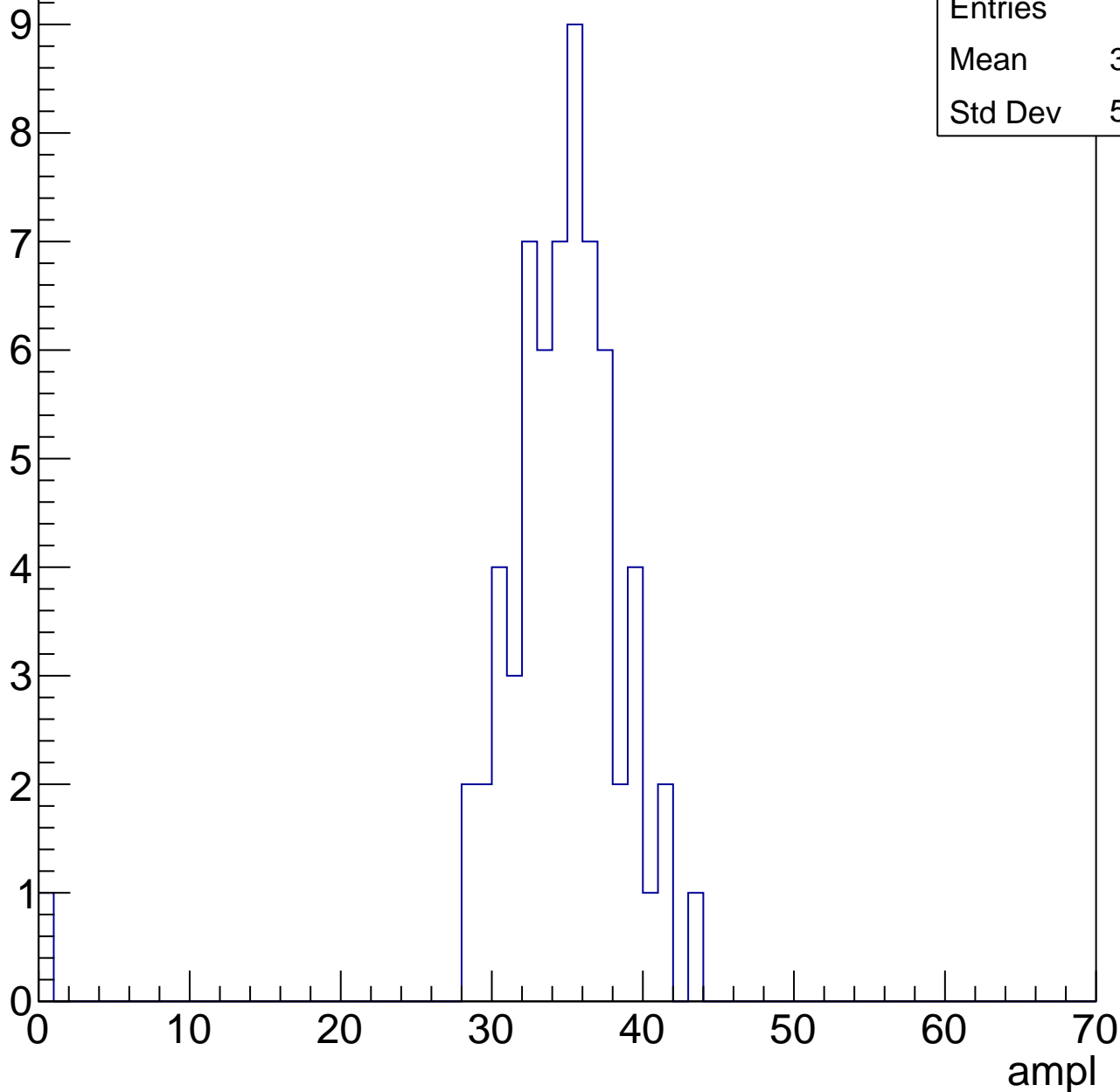


# B1L103S, U25-ch42, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	64
Mean	33.95
Std Dev	5.363

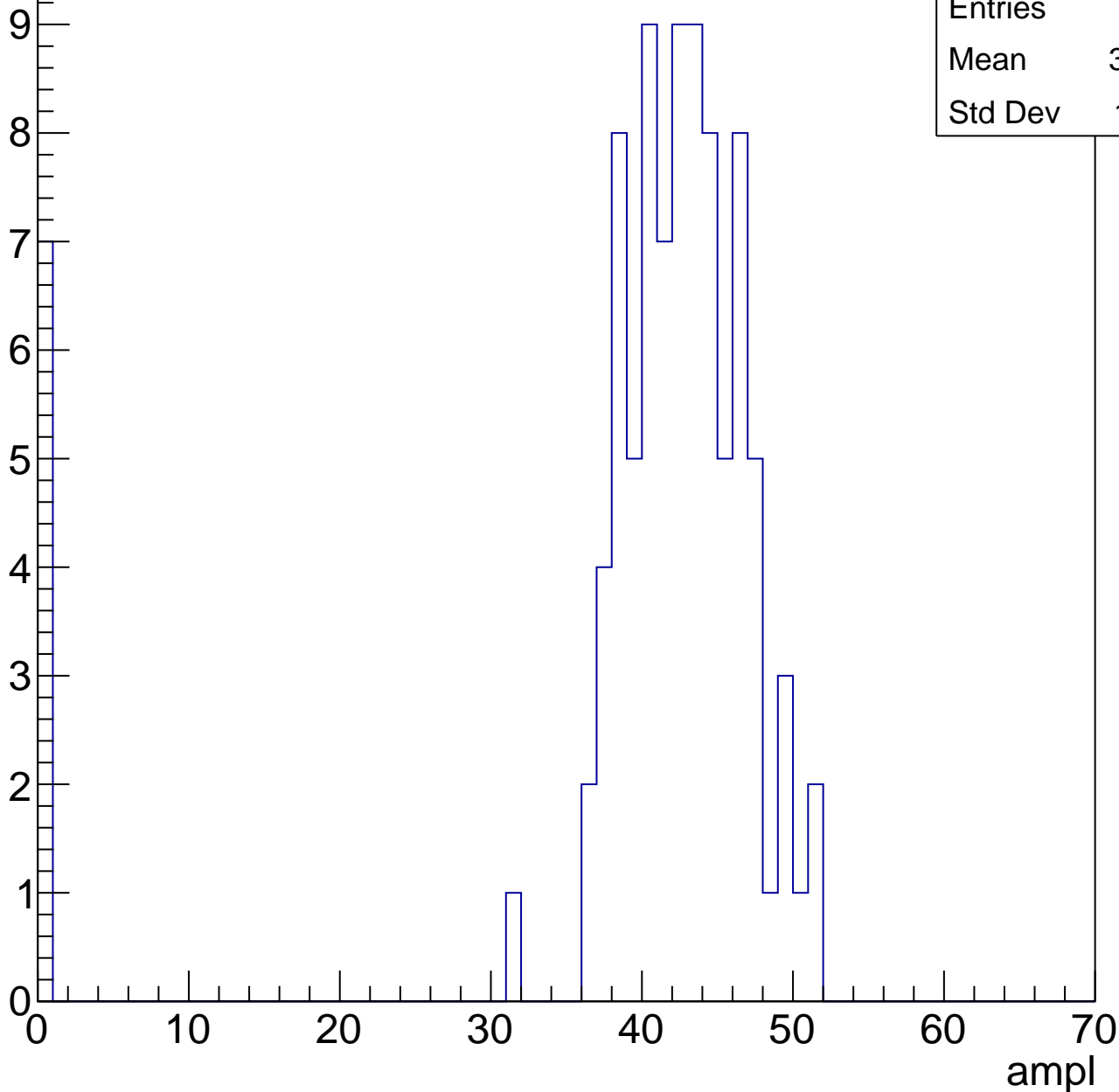


# B1L103S, U25-ch42, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	94
Mean	39.24
Std Dev	11.71

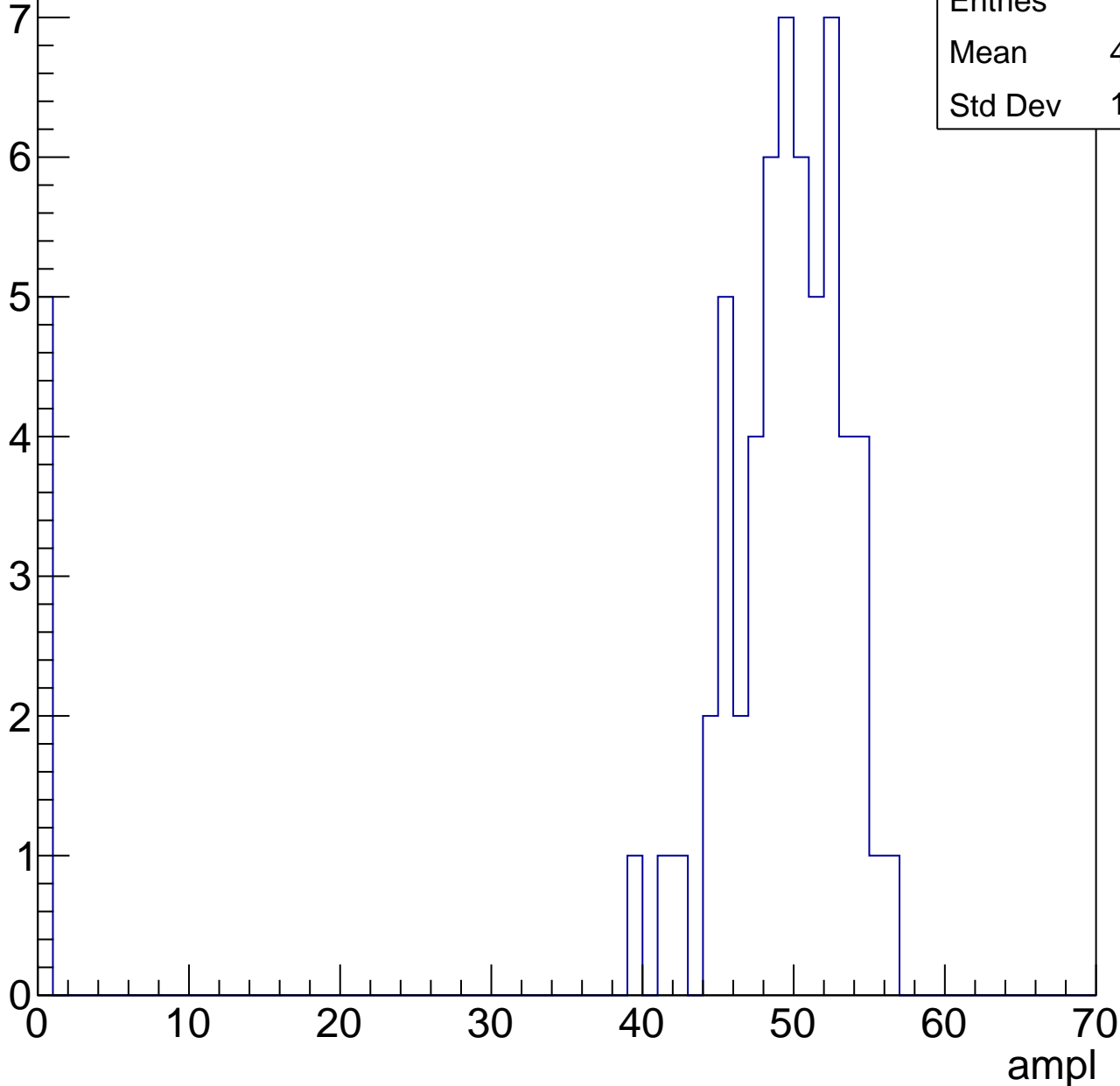


# B1L103S, U25-ch42, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	62
Mean	45.23
Std Dev	13.82

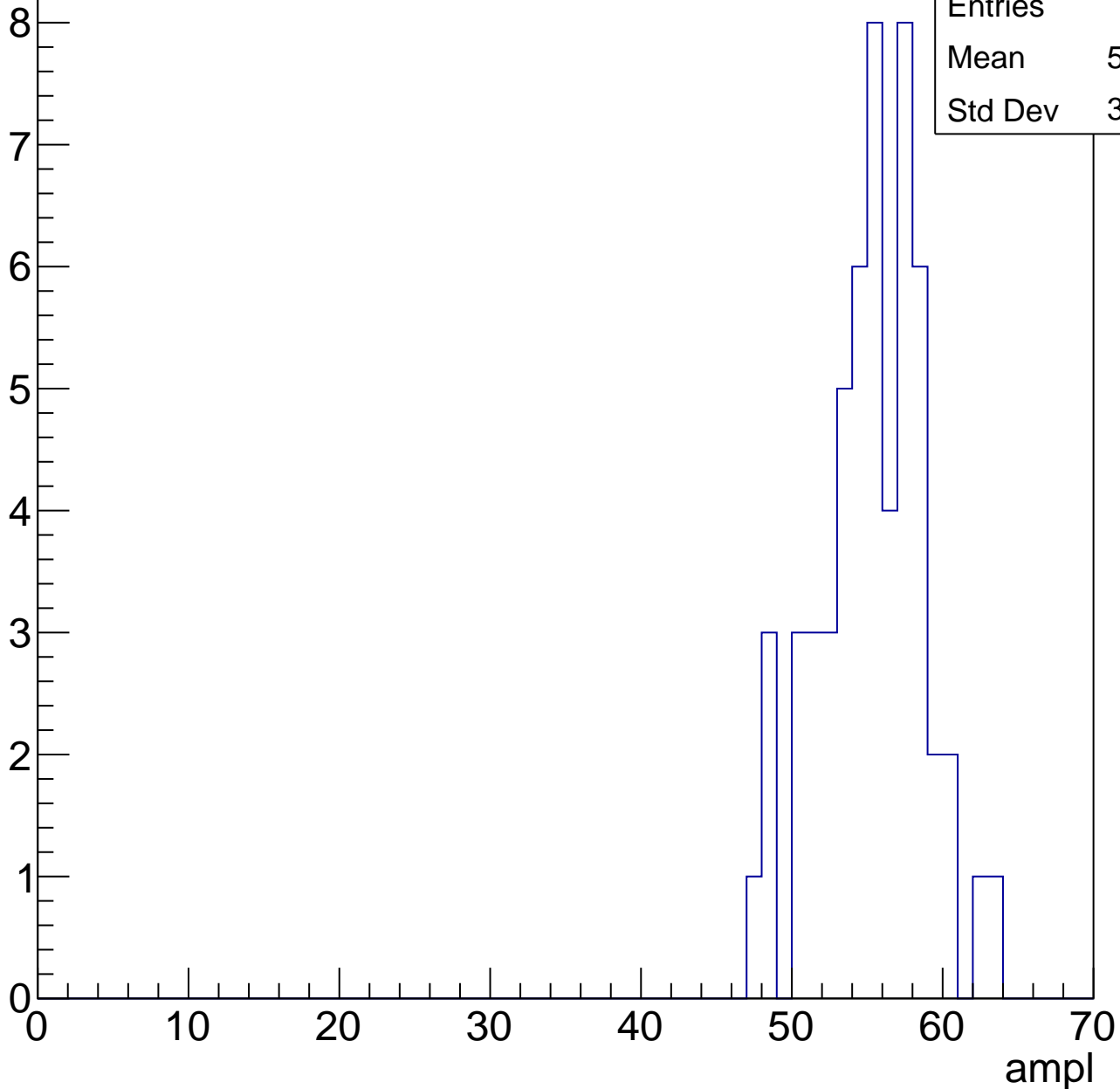


# B1L103S, U25-ch42, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	56
Mean	54.82
Std Dev	3.459

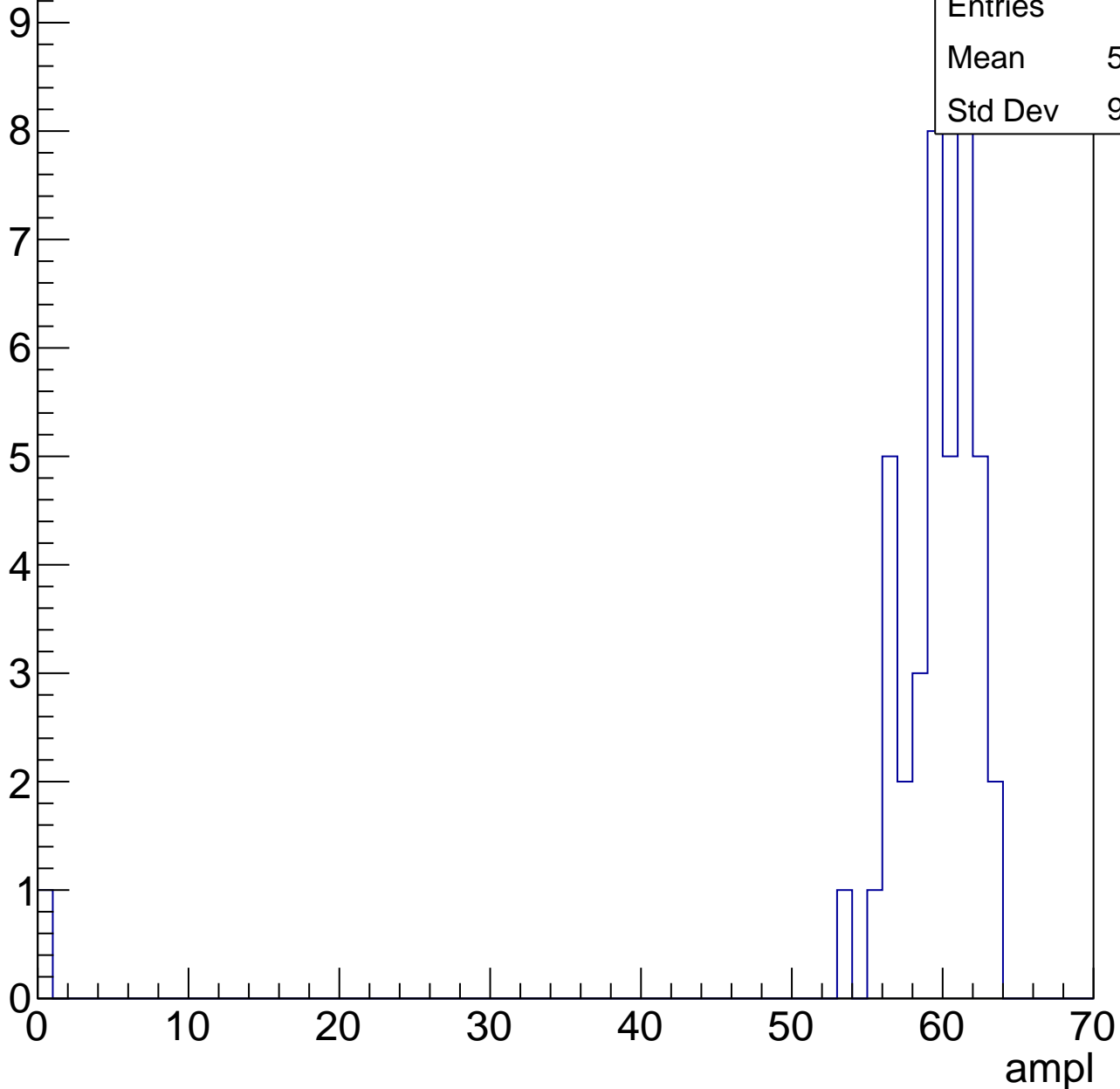


# B1L103S, U25-ch42, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	42
Mean	57.93
Std Dev	9.333

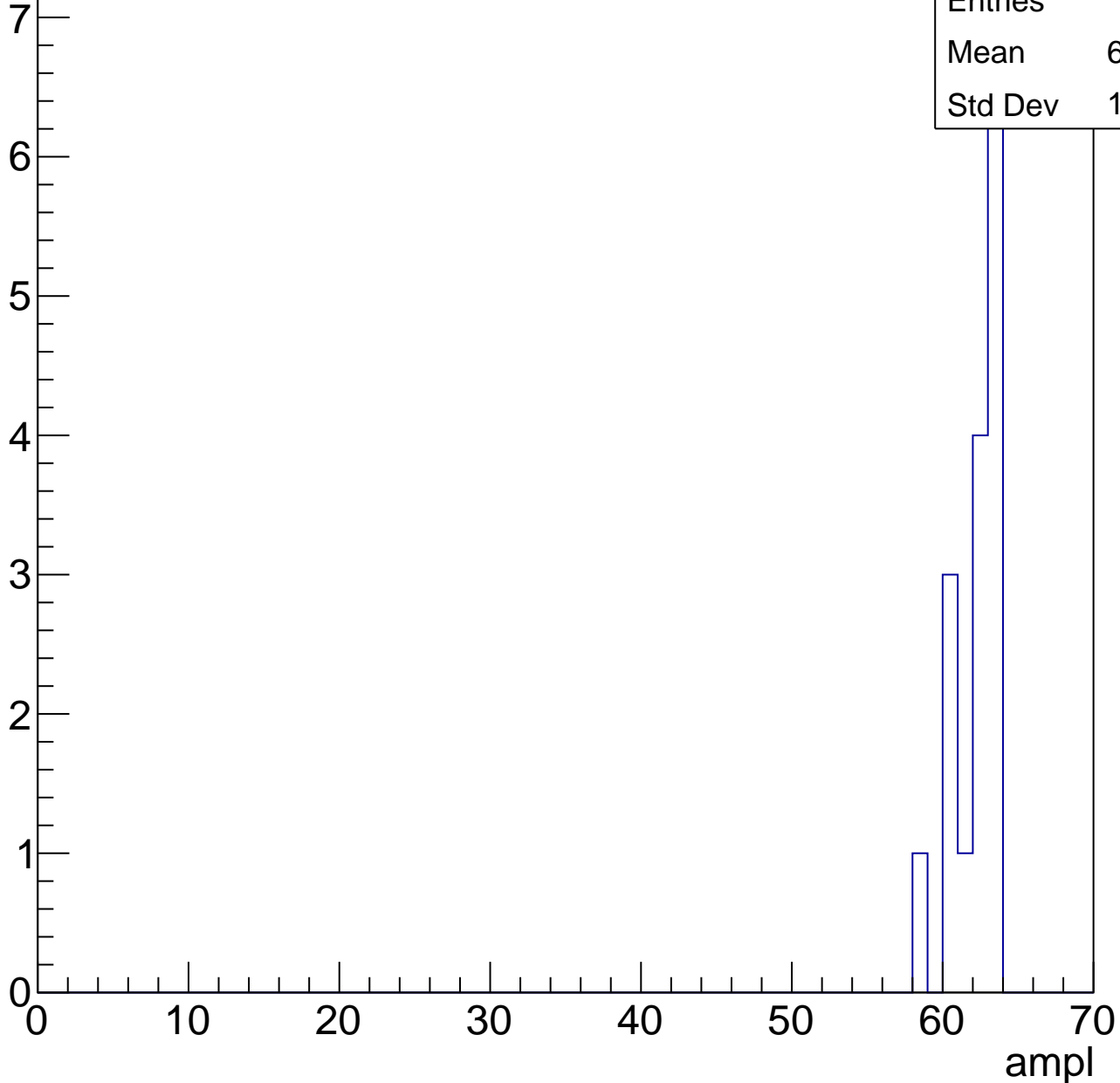


# B1L103S, U25-ch42, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	16
Mean	61.75
Std Dev	1.479





# B1L103S, U25-ch42, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

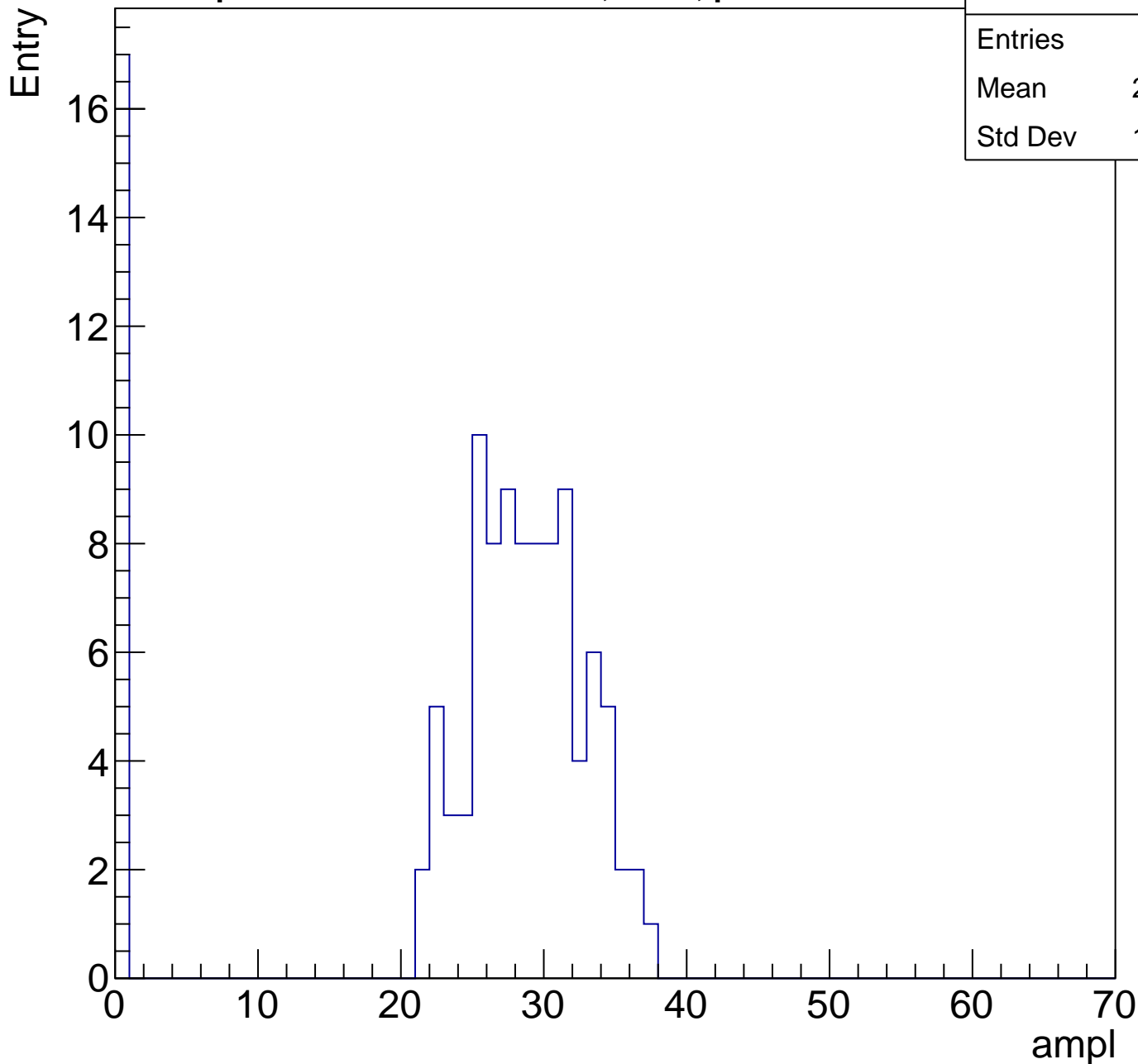
Entry



# B1L103S, U25-ch43, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	110
Mean	24.04
Std Dev	10.85

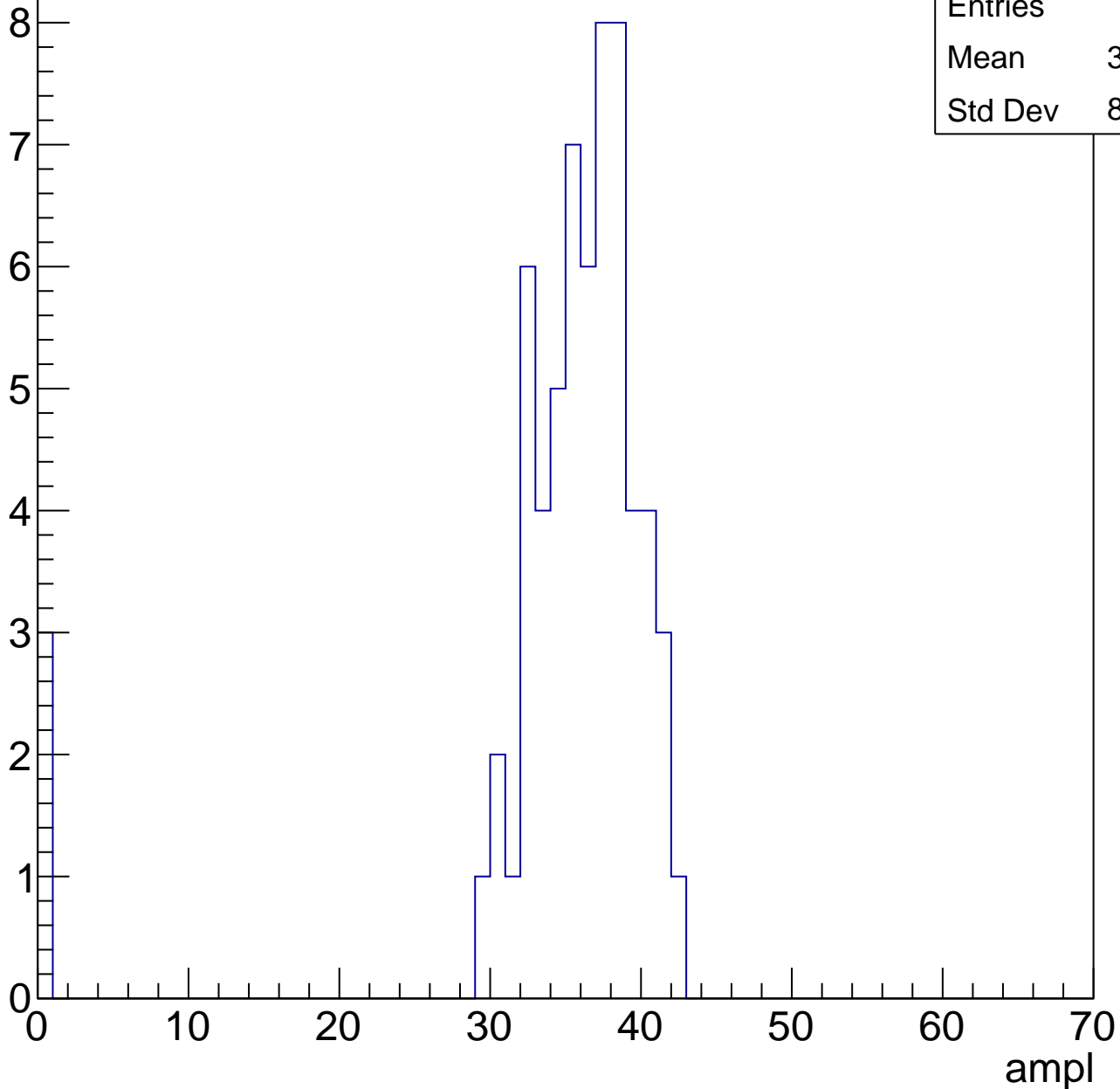


# B1L103S, U25-ch43, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	63
Mean	34.22
Std Dev	8.208



# B1L103S, U25-ch43, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	81
Mean	36.99
Std Dev	14.99

Entry

10

8

6

4

2

0

0

10

20

30

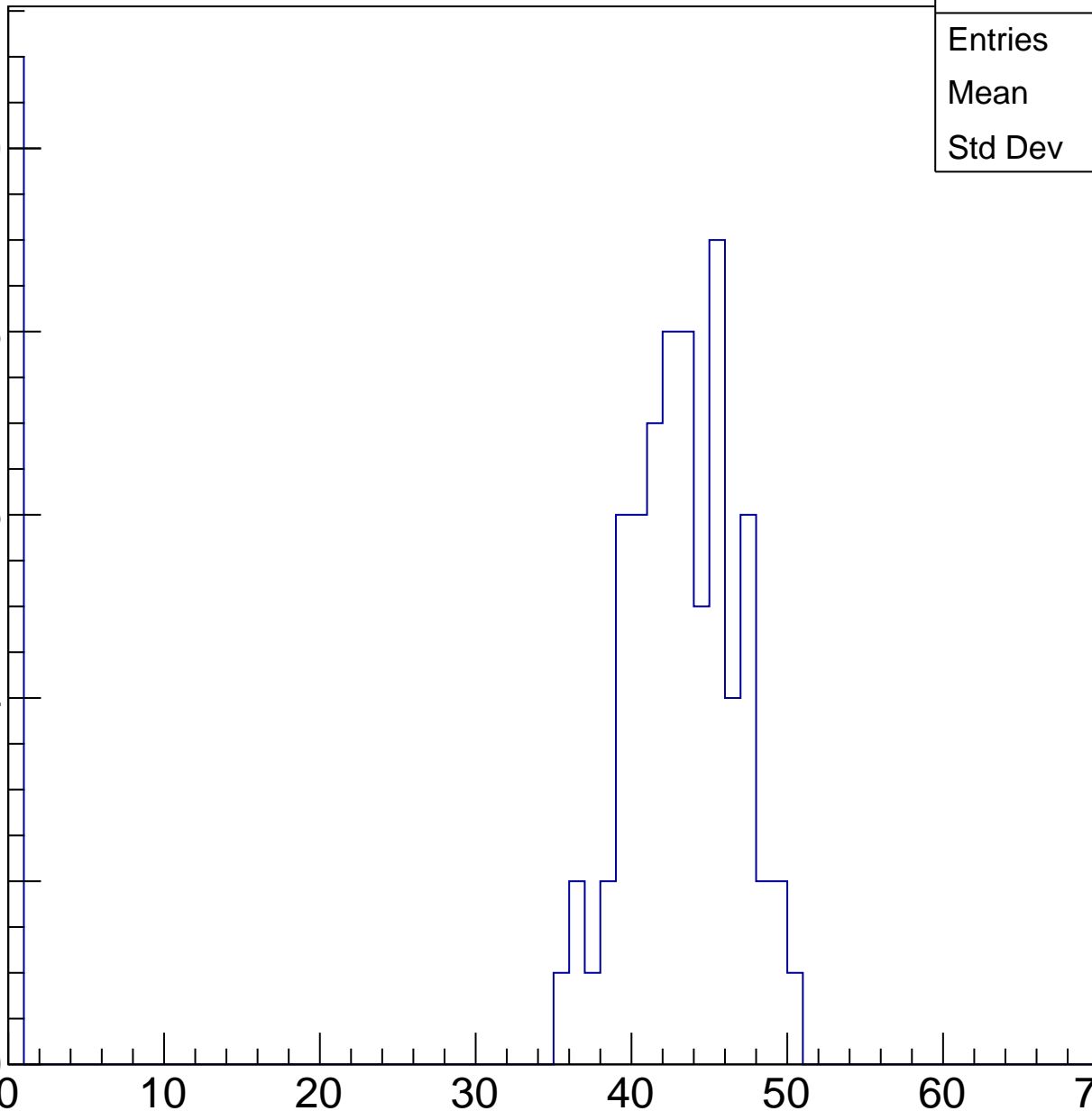
40

50

60

70

ampl

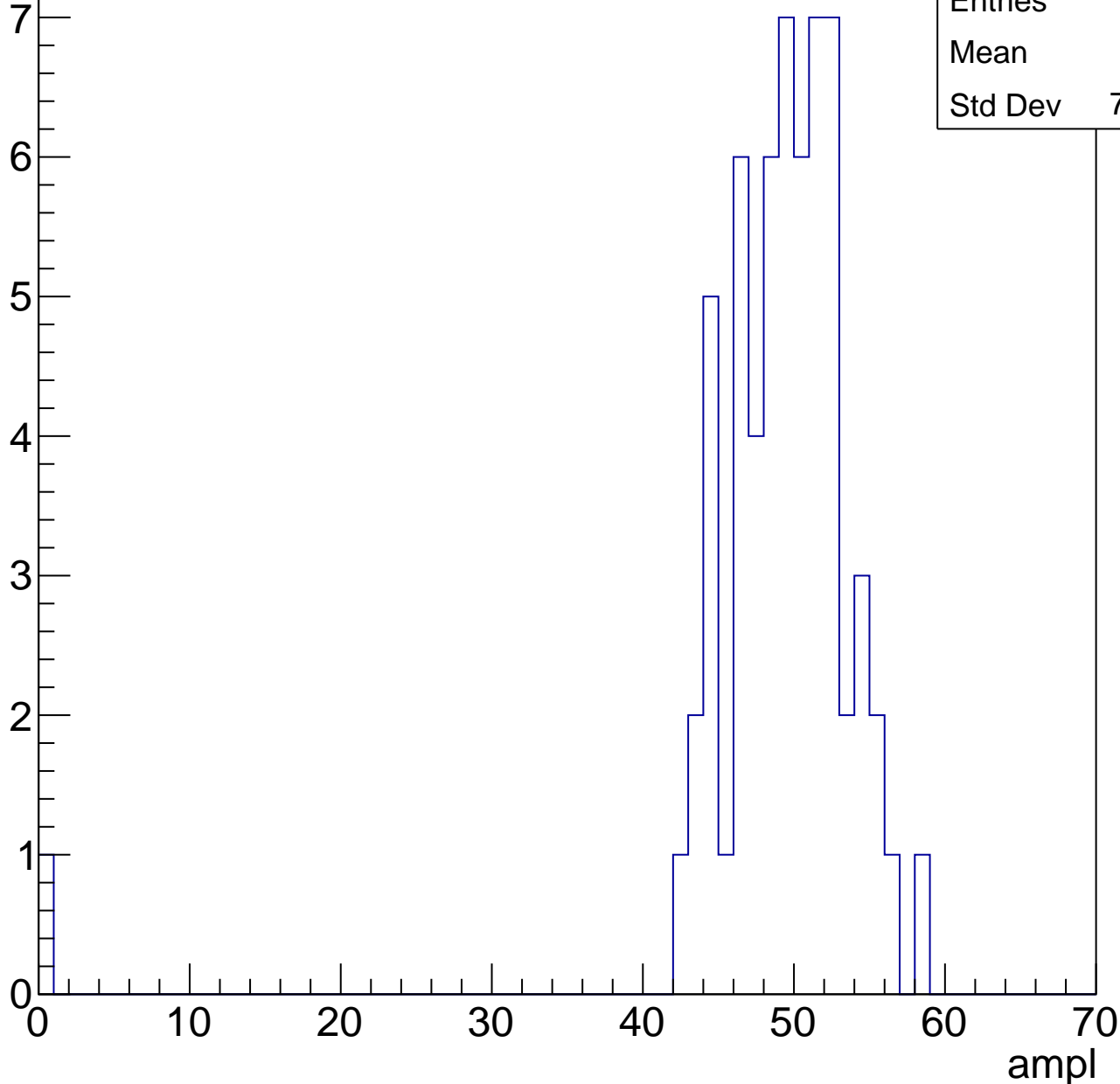


# B1L103S, U25-ch43, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	62
Mean	48.4
Std Dev	7.097

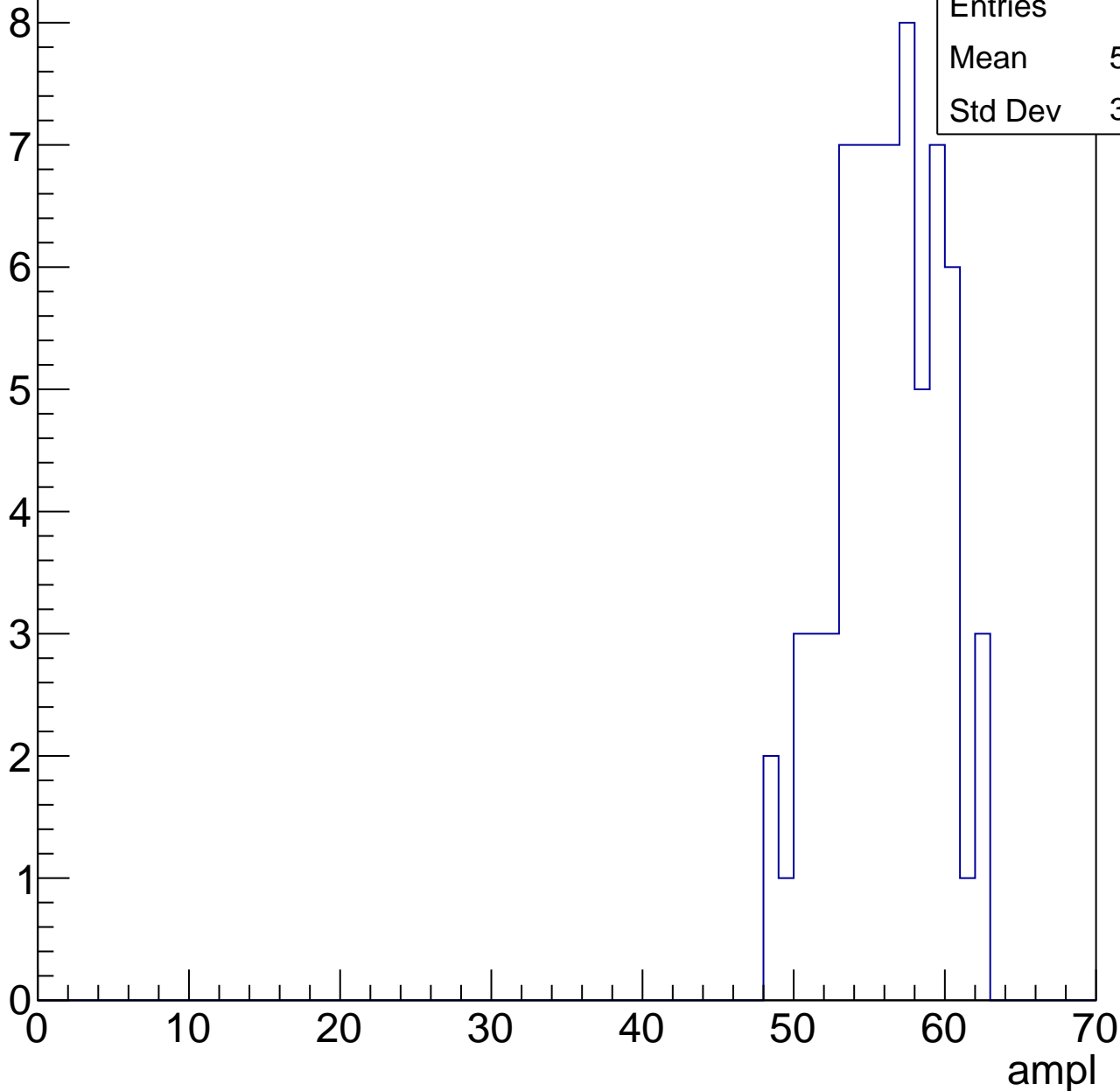


# B1L103S, U25-ch43, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	70
Mean	55.66
Std Dev	3.418

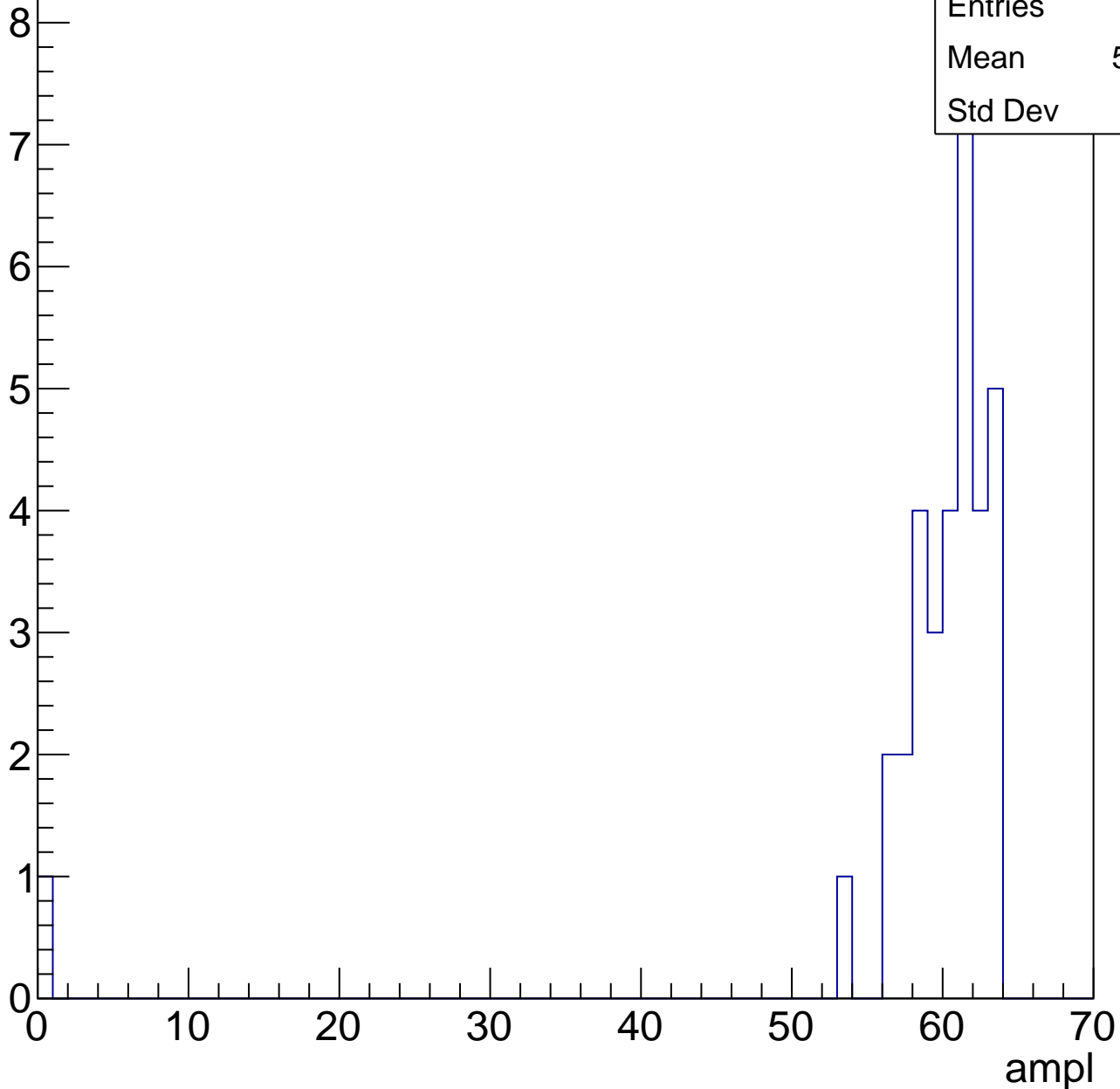


# B1L103S, U25-ch43, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	34
Mean	58.21
Std Dev	10.4

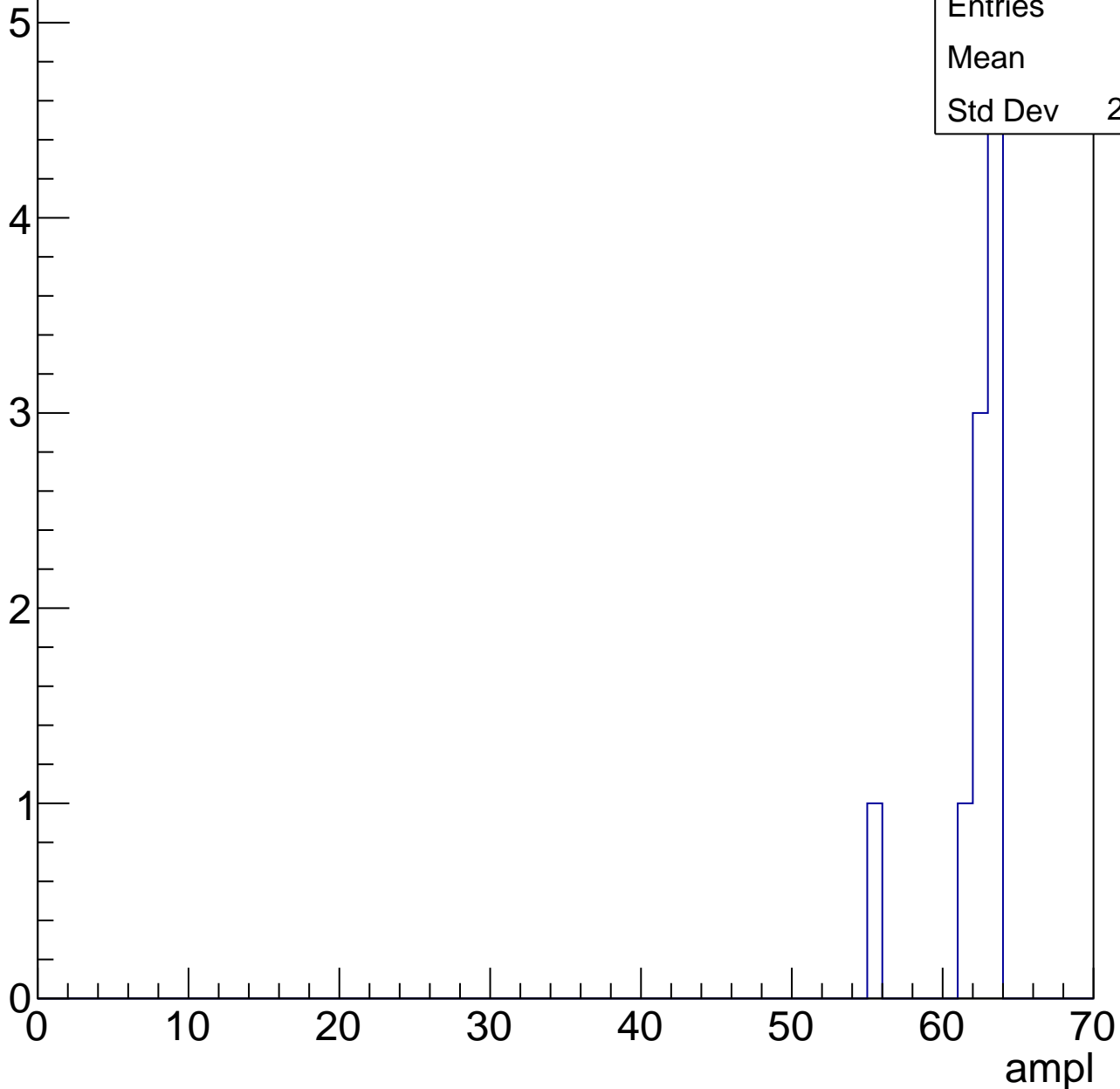


# B1L103S, U25-ch43, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	10
Mean	61.7
Std Dev	2.326





# B1L103S, U25-ch43, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U25-ch44, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	82
Mean	22.44
Std Dev	10.3

Entry

12

10

8

6

4

2

0

0

10

20

30

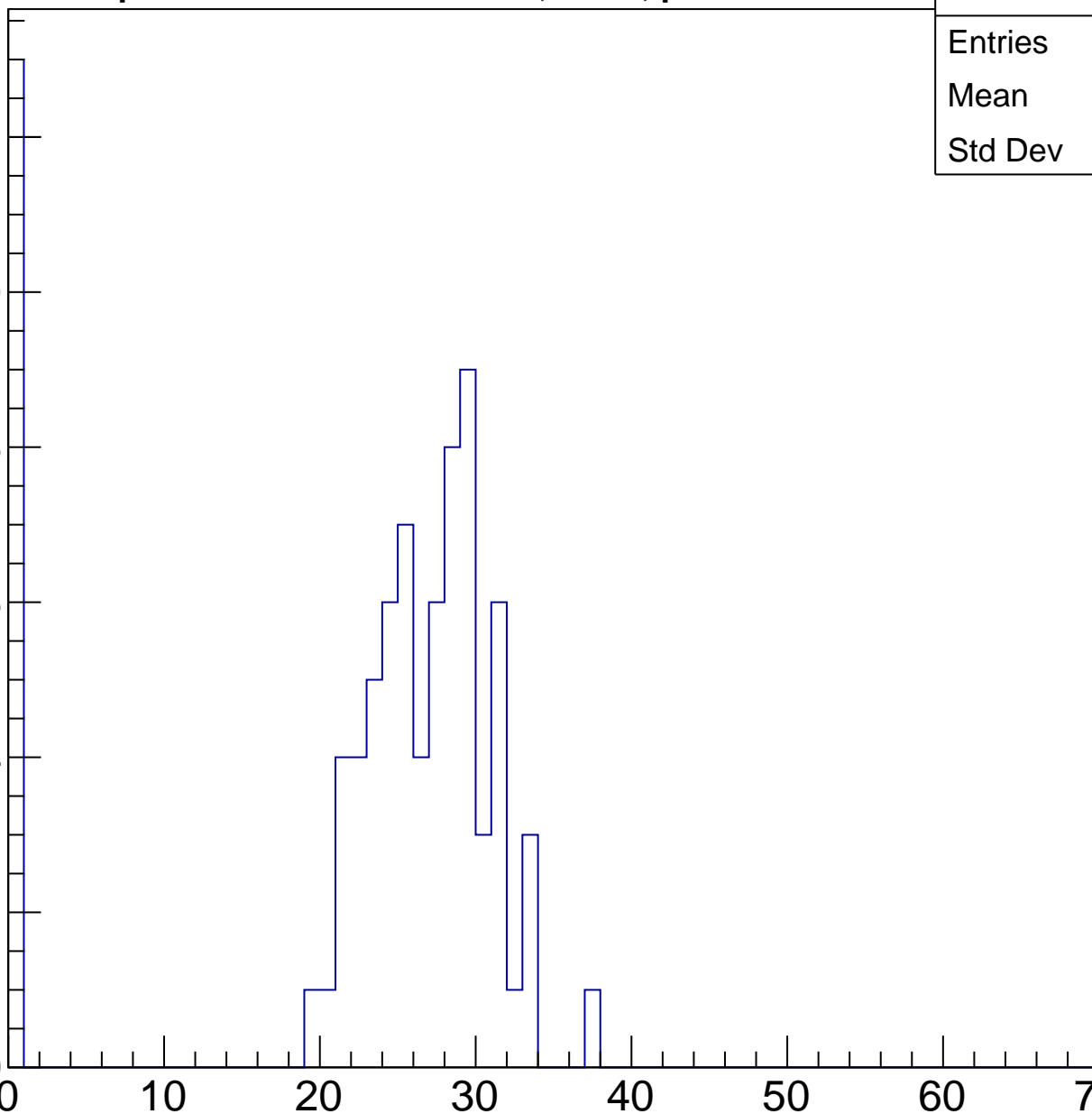
40

50

60

70

ampl

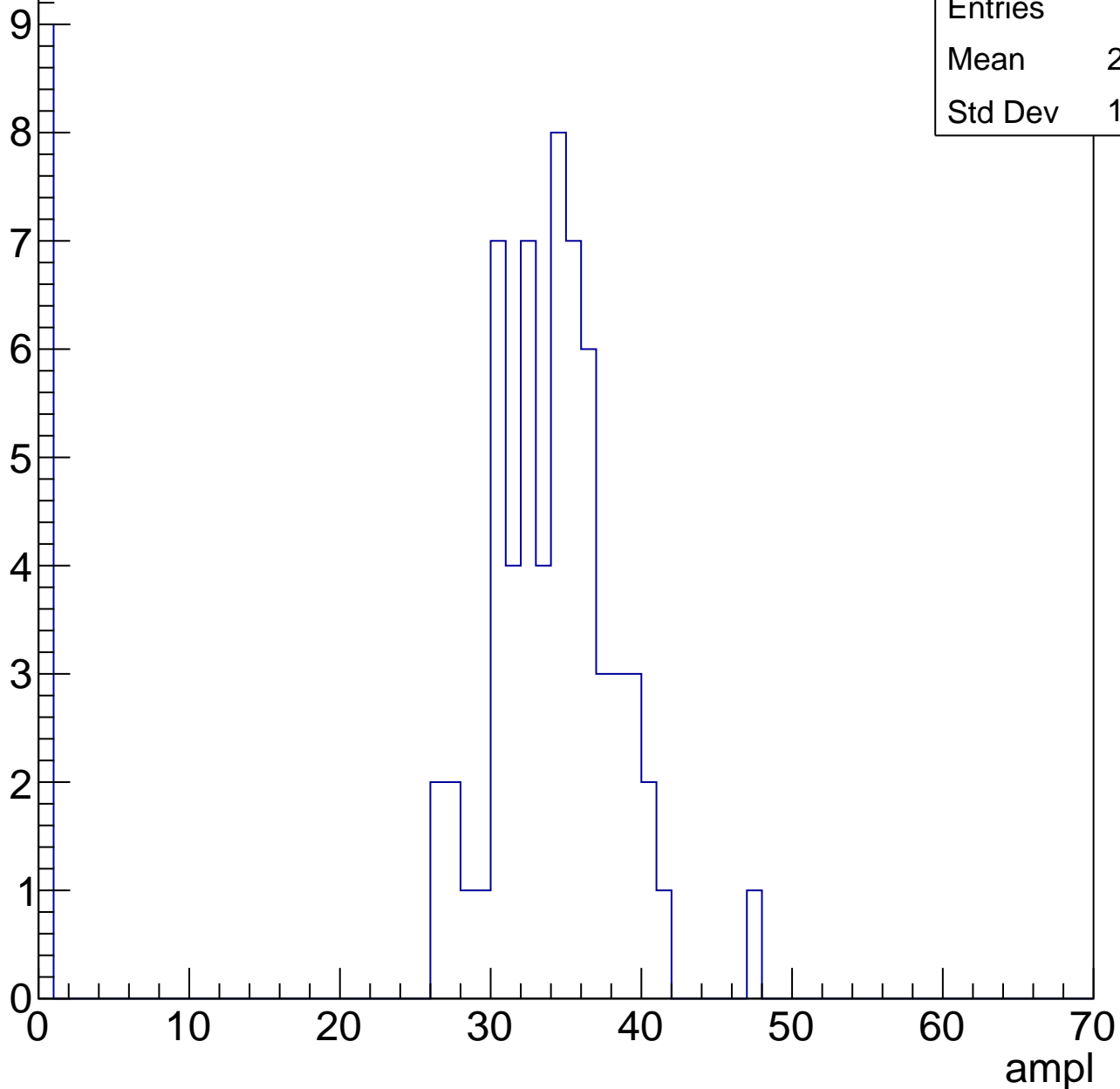


# B1L103S, U25-ch44, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	71
Mean	29.52
Std Dev	11.82

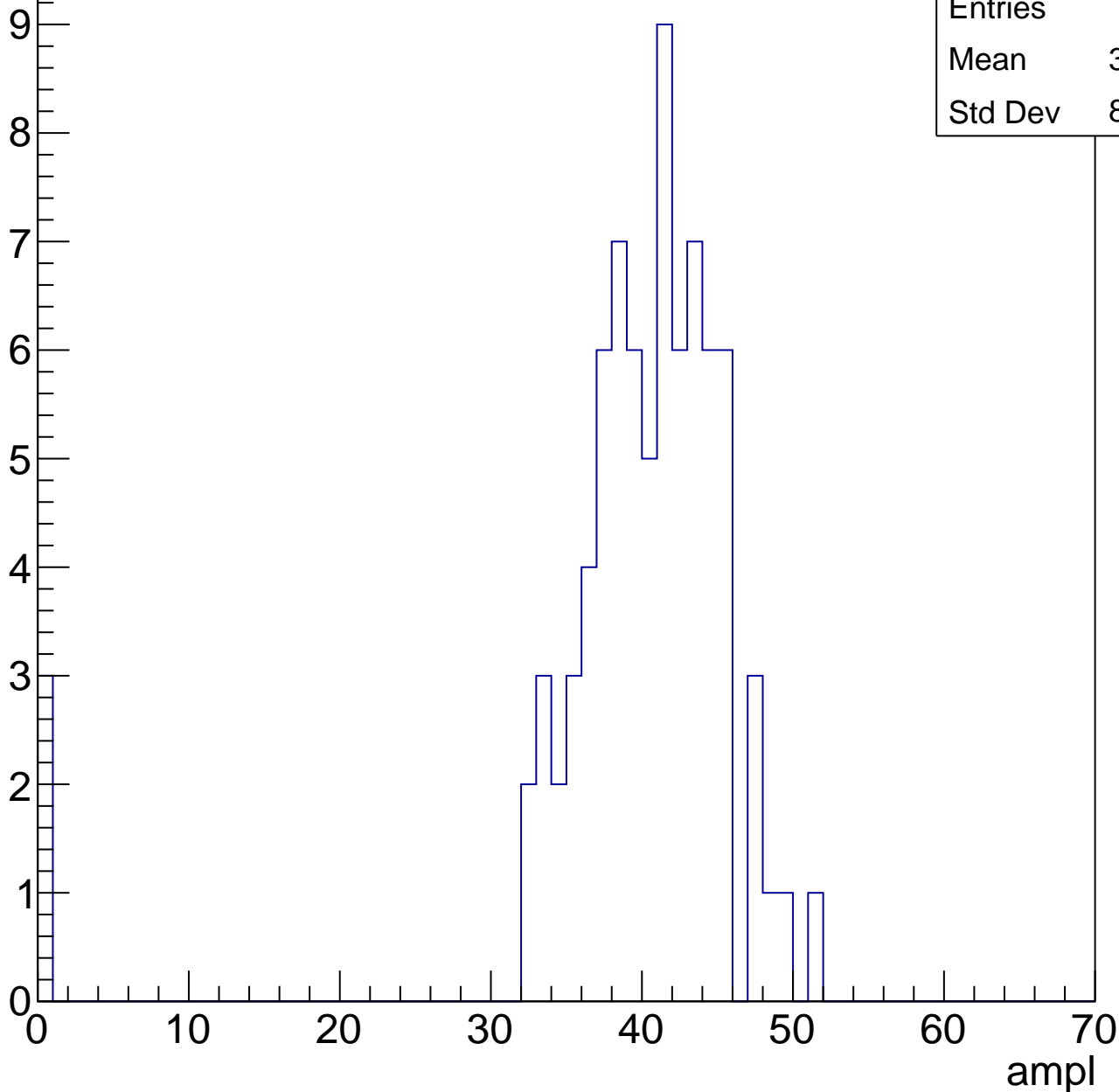


# B1L103S, U25-ch44, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	81
Mean	38.85
Std Dev	8.623

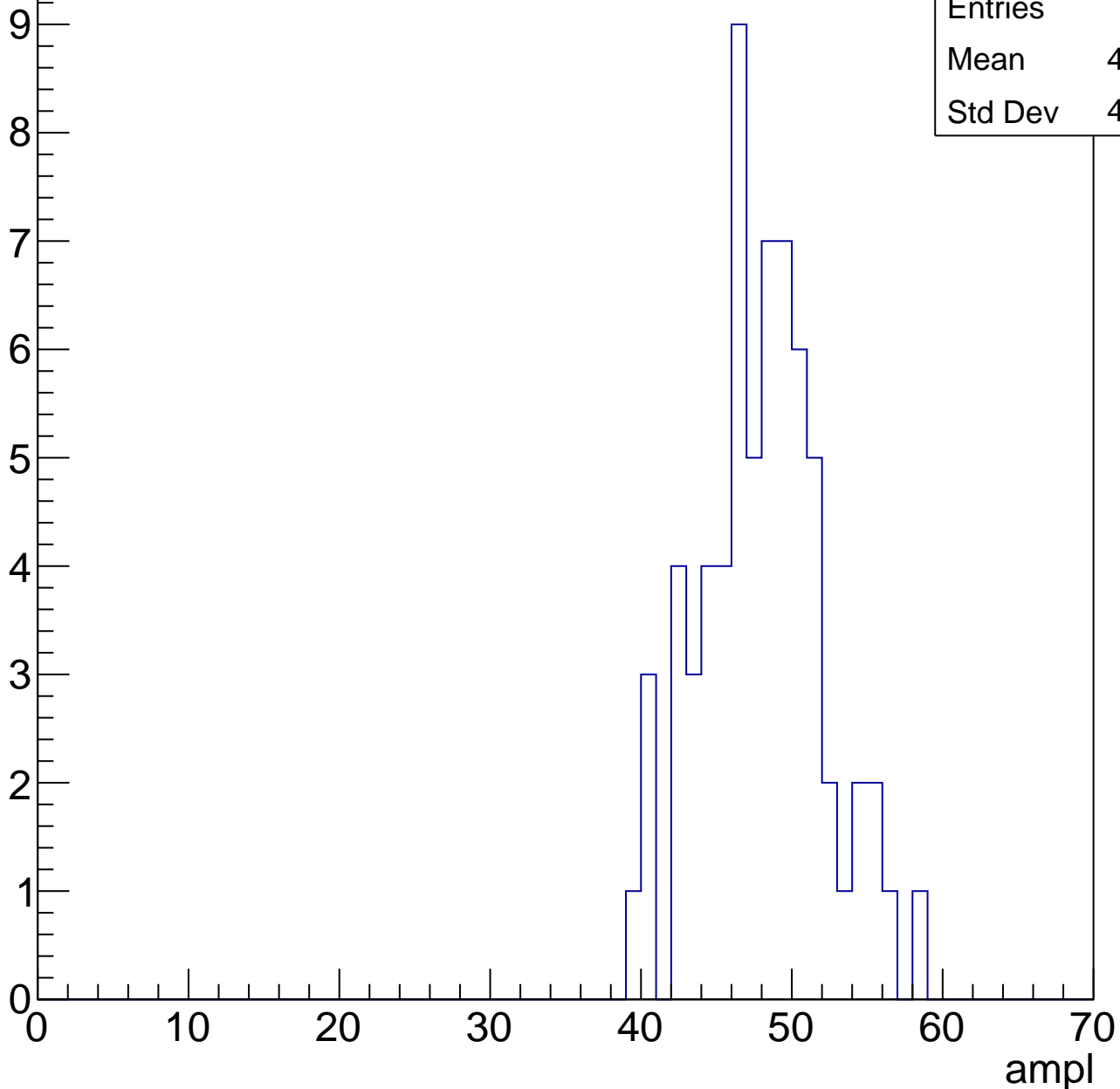


# B1L103S, U25-ch44, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	67
Mean	47.52
Std Dev	4.024

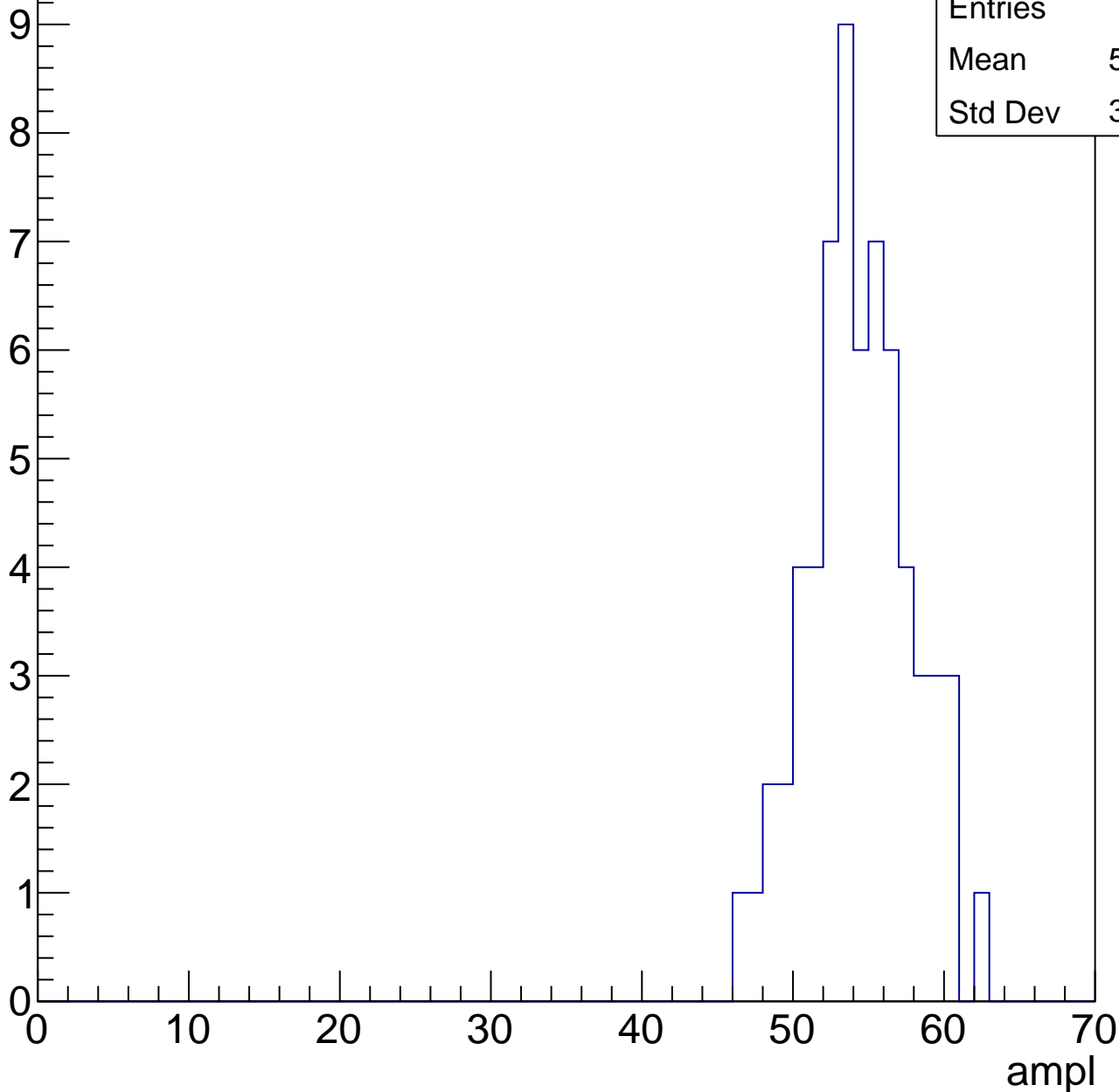


# B1L103S, U25-ch44, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	63
Mean	53.94
Std Dev	3.413

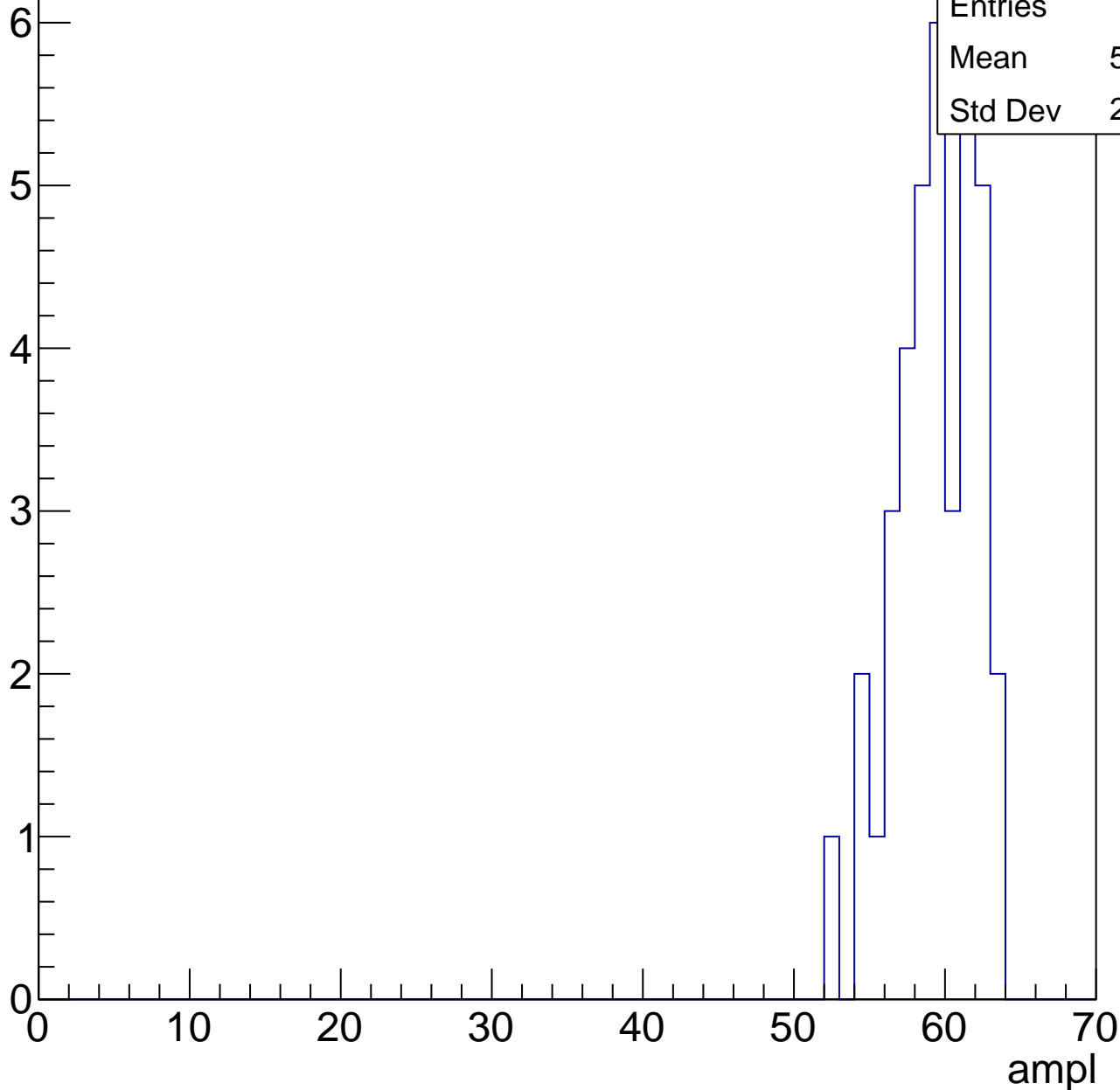


# B1L103S, U25-ch44, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	38
Mean	58.87
Std Dev	2.647

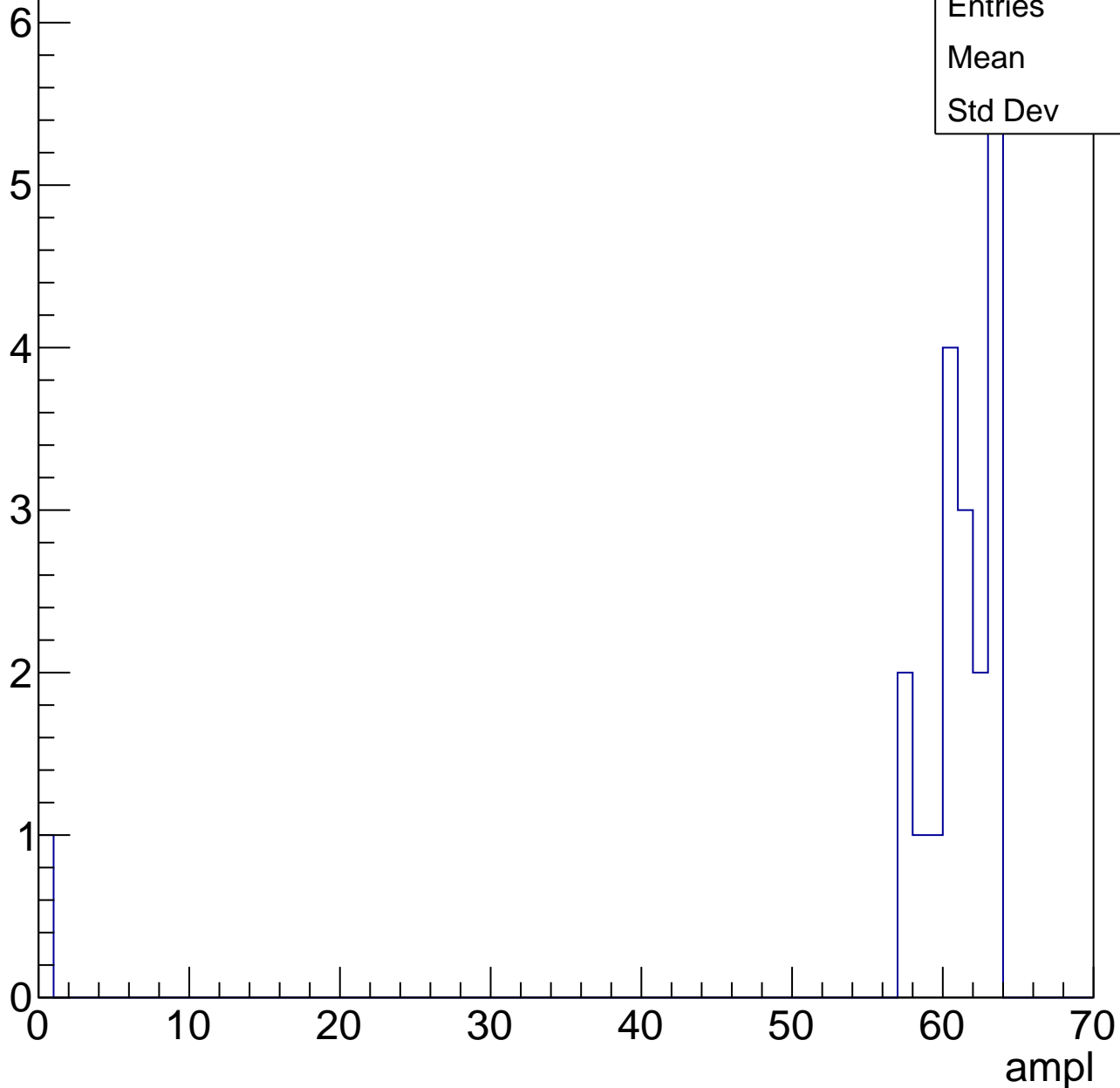


# B1L103S, U25-ch44, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	20
Mean	57.8
Std Dev	13.4



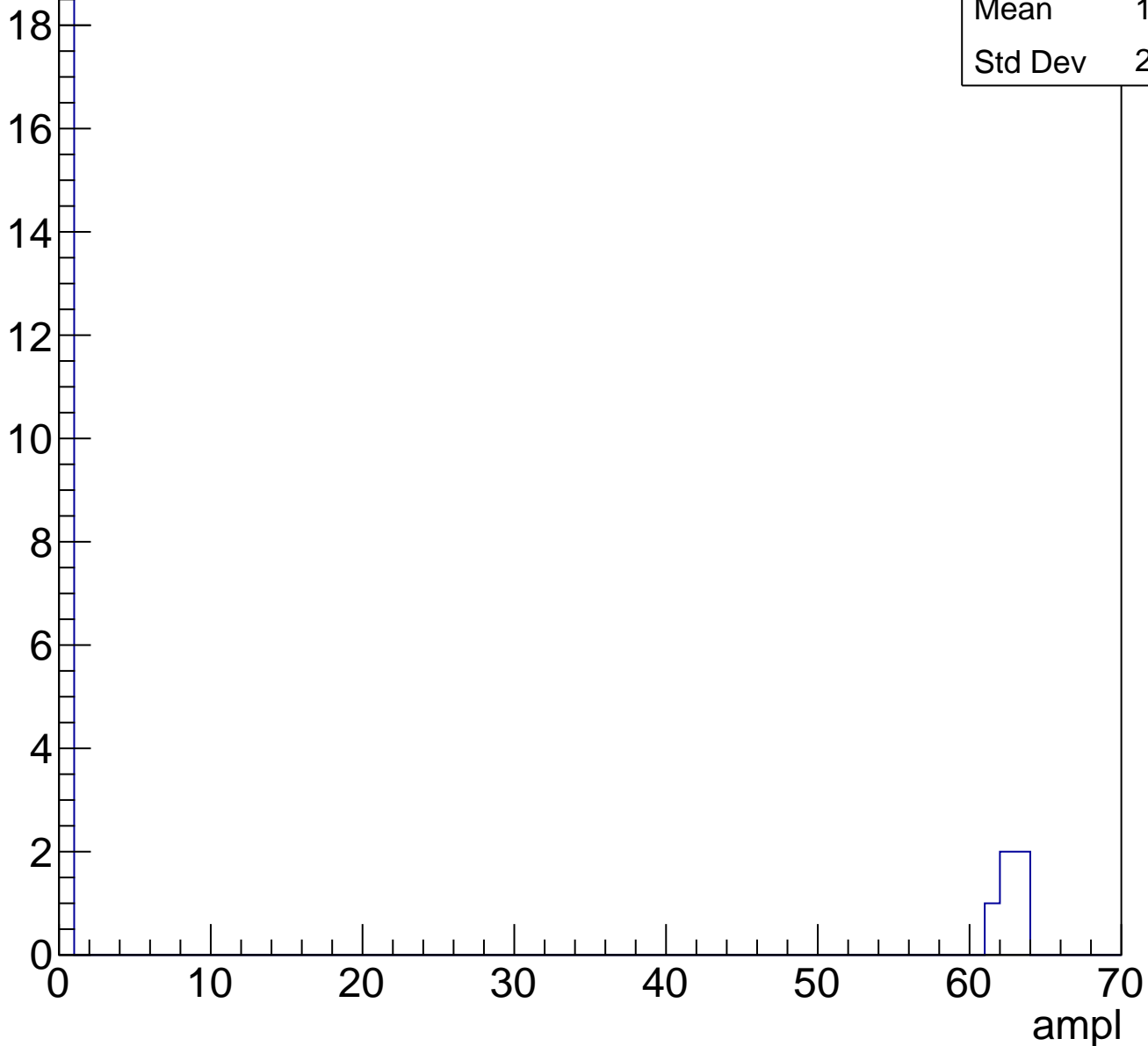


# B1L103S, U25-ch44, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	24
Mean	12.96
Std Dev	25.26

Entry

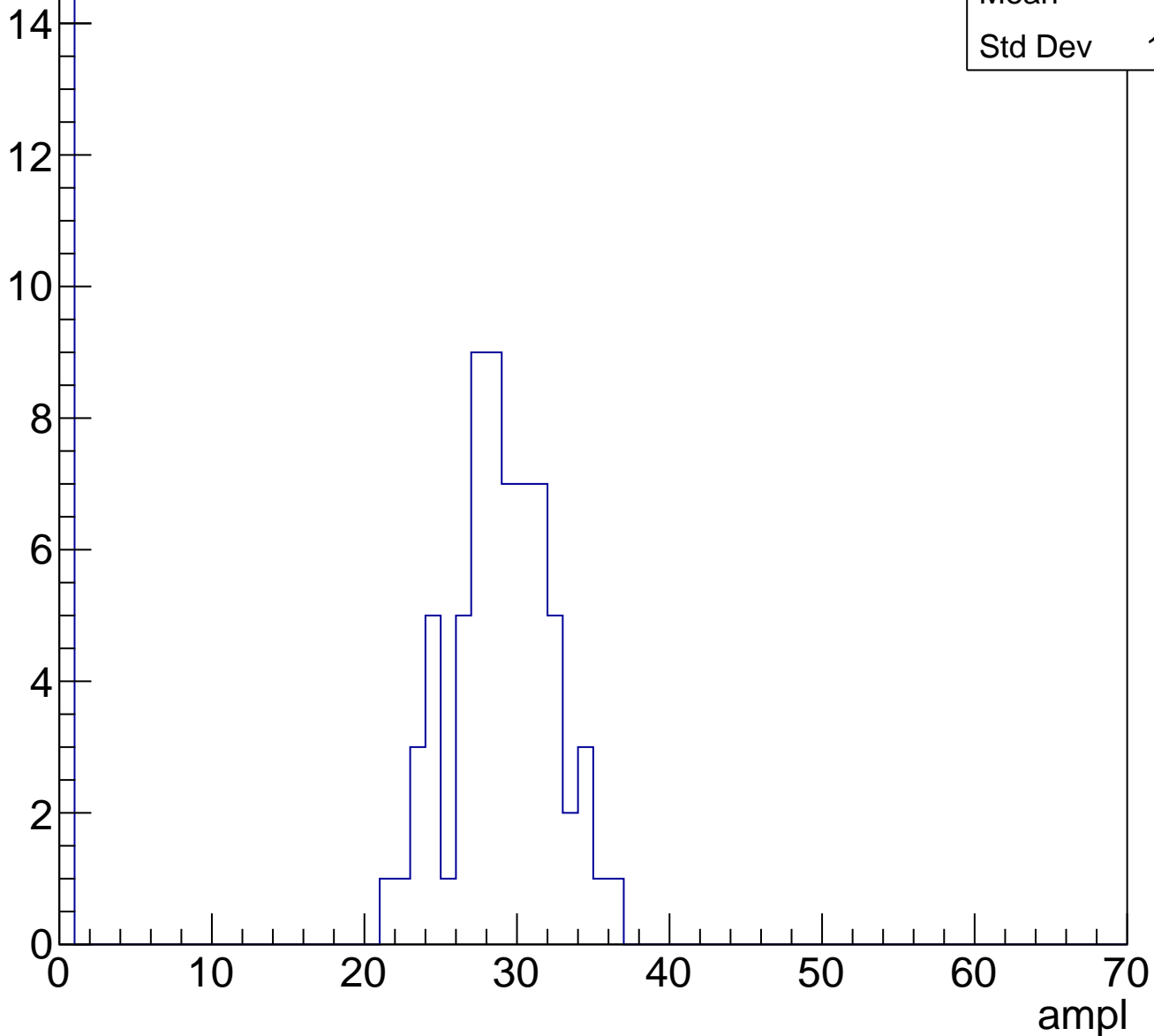


# B1L103S, U25-ch45, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	82
Mean	23.3
Std Dev	11.41

Entry

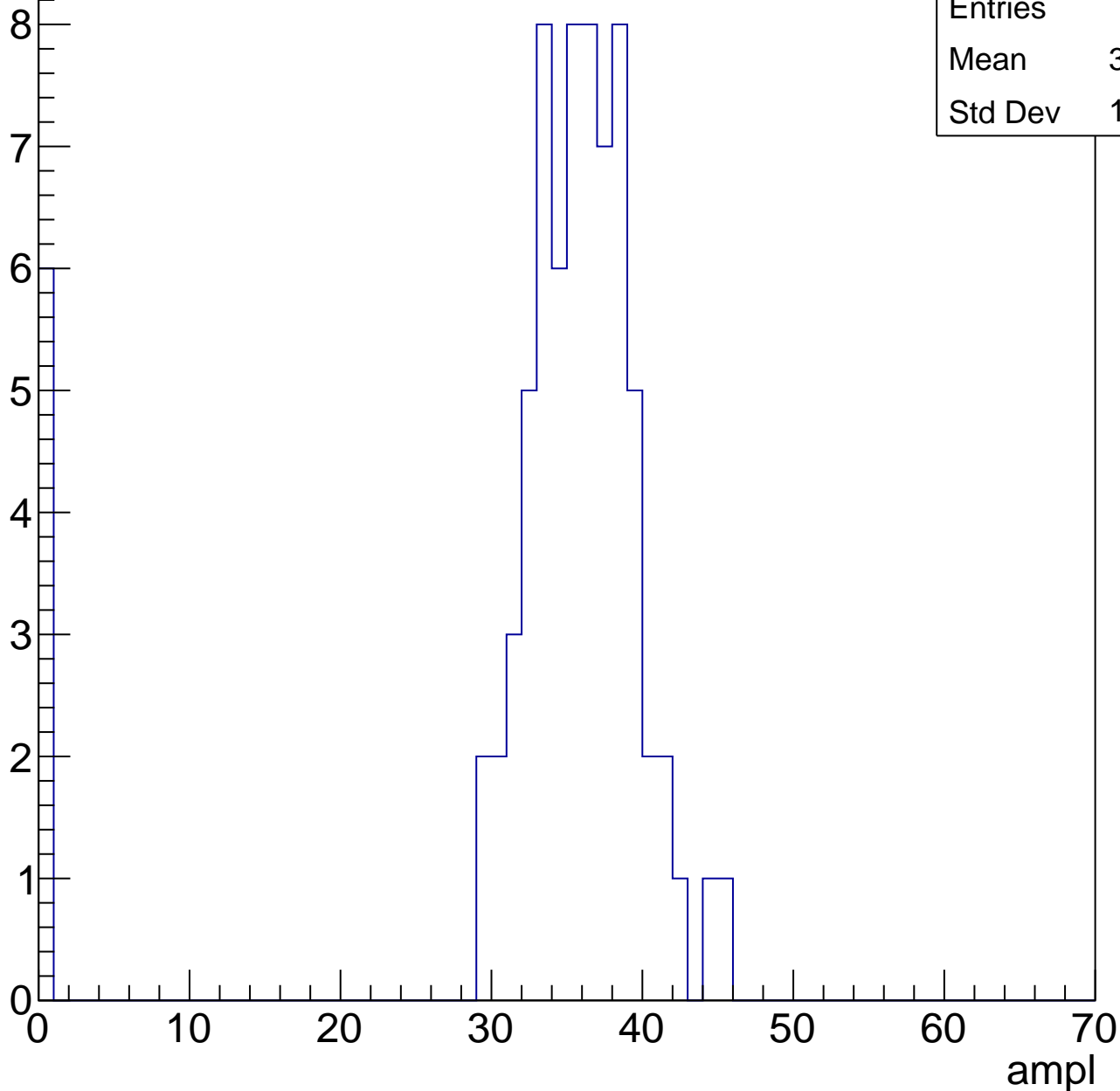


# B1L103S, U25-ch45, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	75
Mean	32.77
Std Dev	10.18

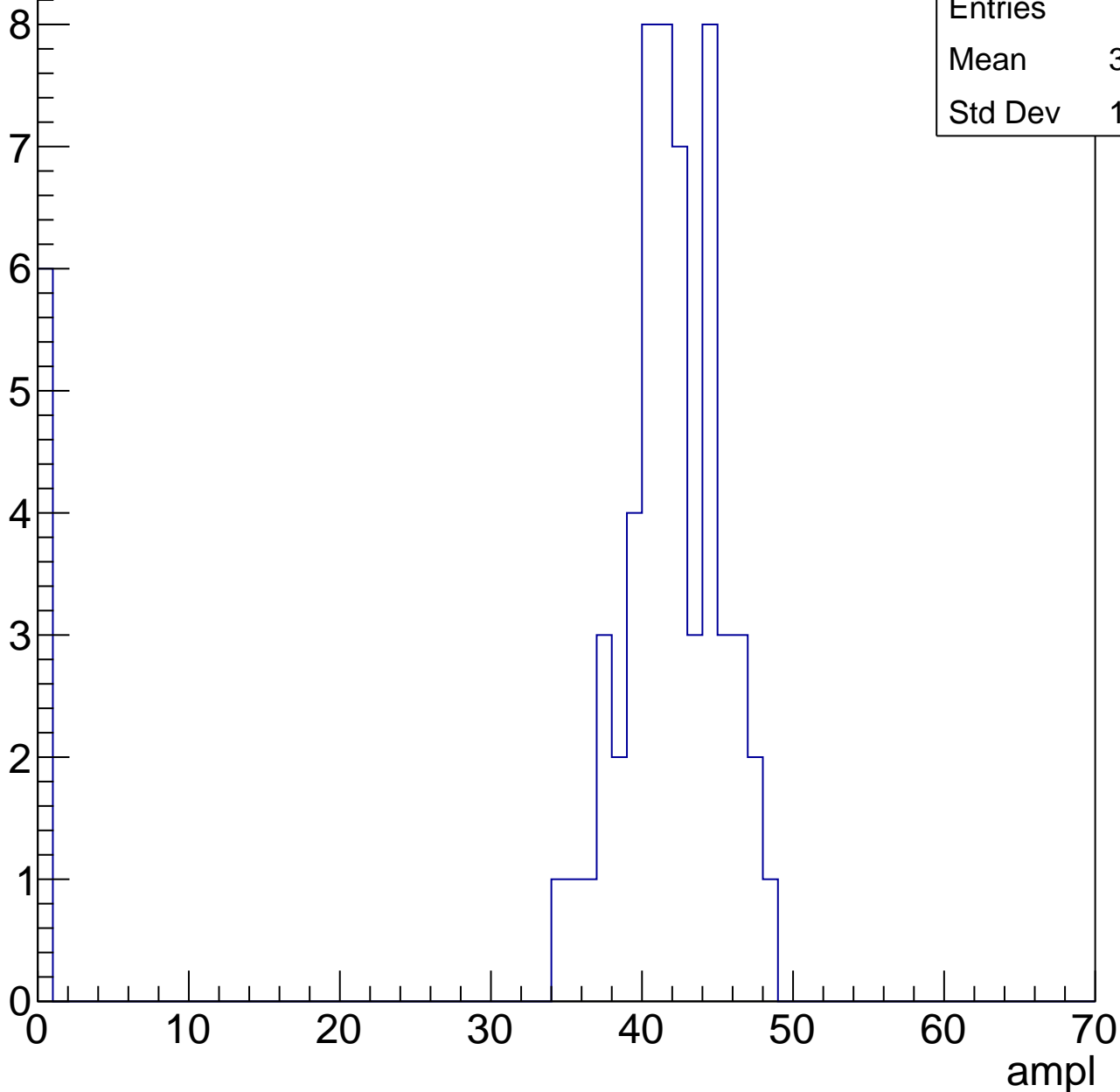


# B1L103S, U25-ch45, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	61
Mean	37.48
Std Dev	12.72

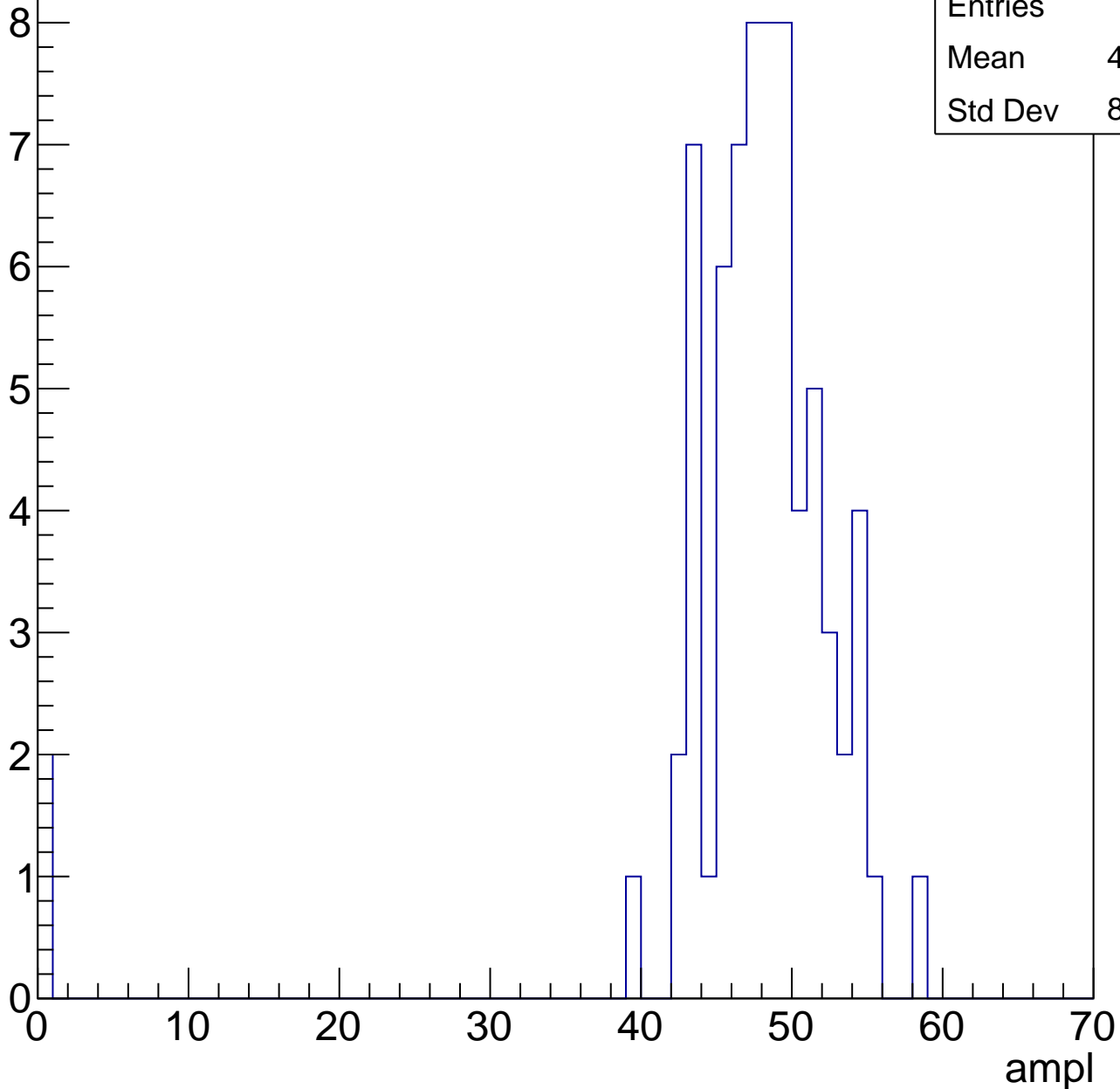


# B1L103S, U25-ch45, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	70
Mean	46.54
Std Dev	8.745

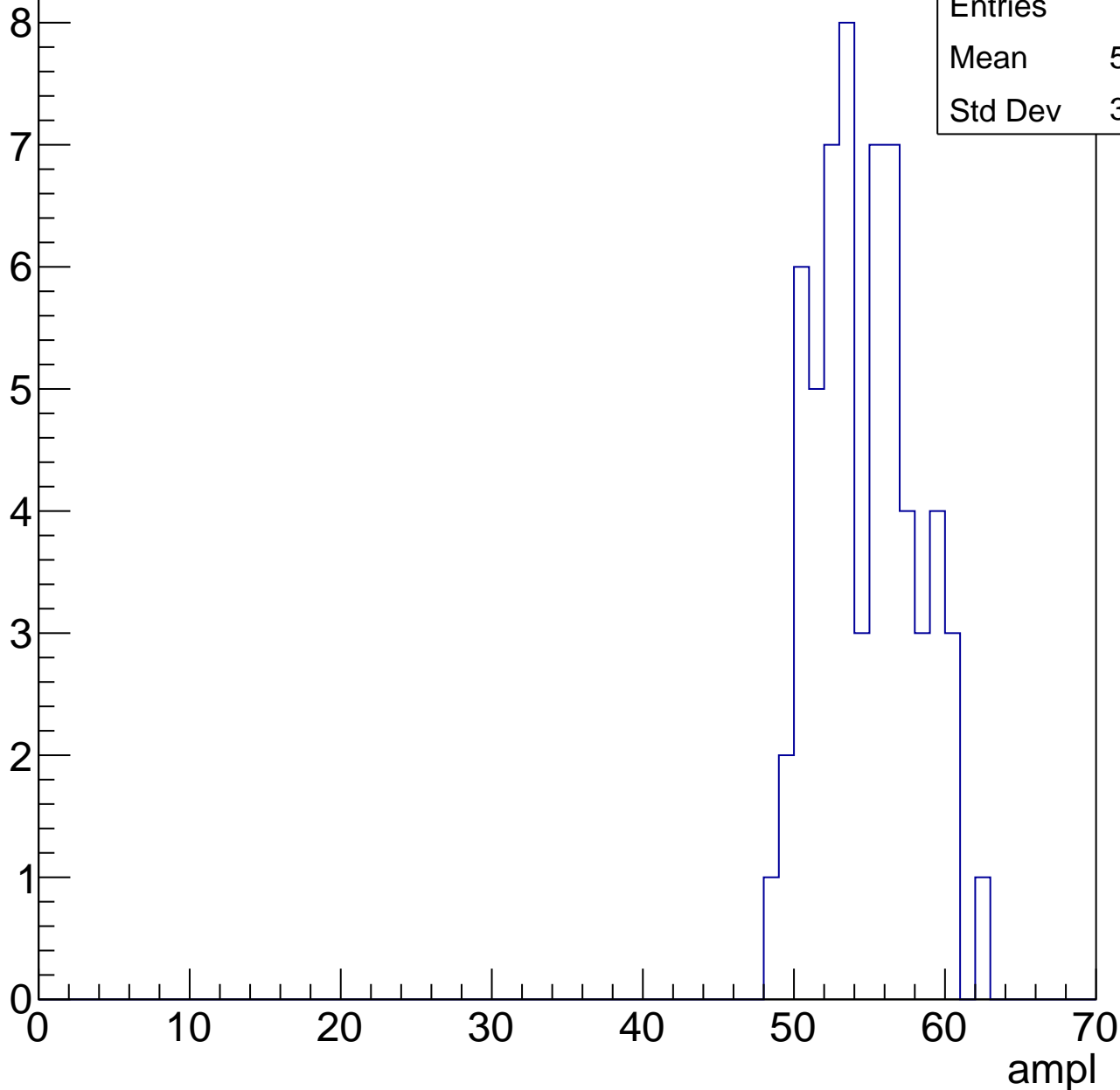


# B1L103S, U25-ch45, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

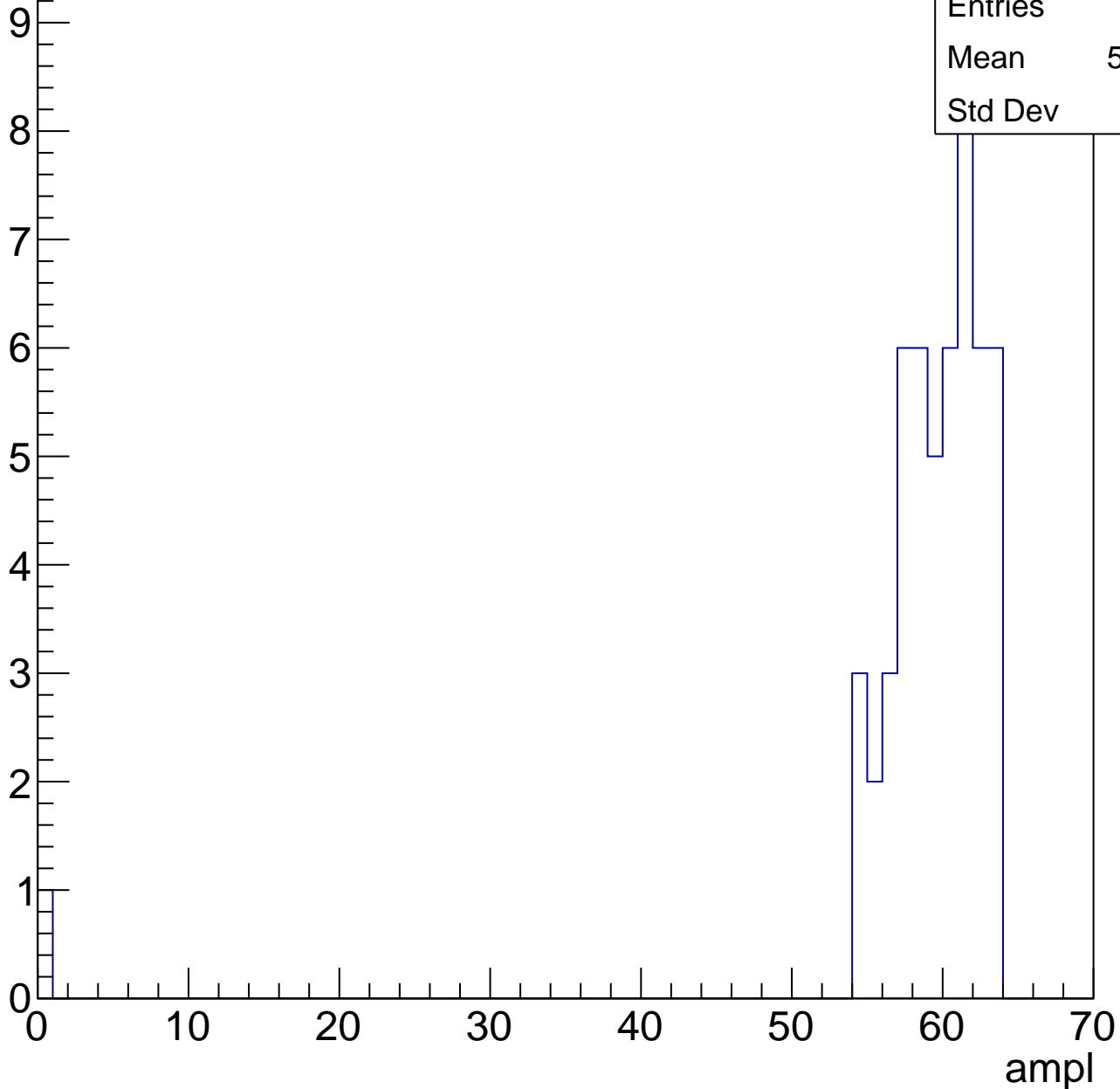
Entries	61
Mean	54.23
Std Dev	3.266



# B1L103S, U25-ch45, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

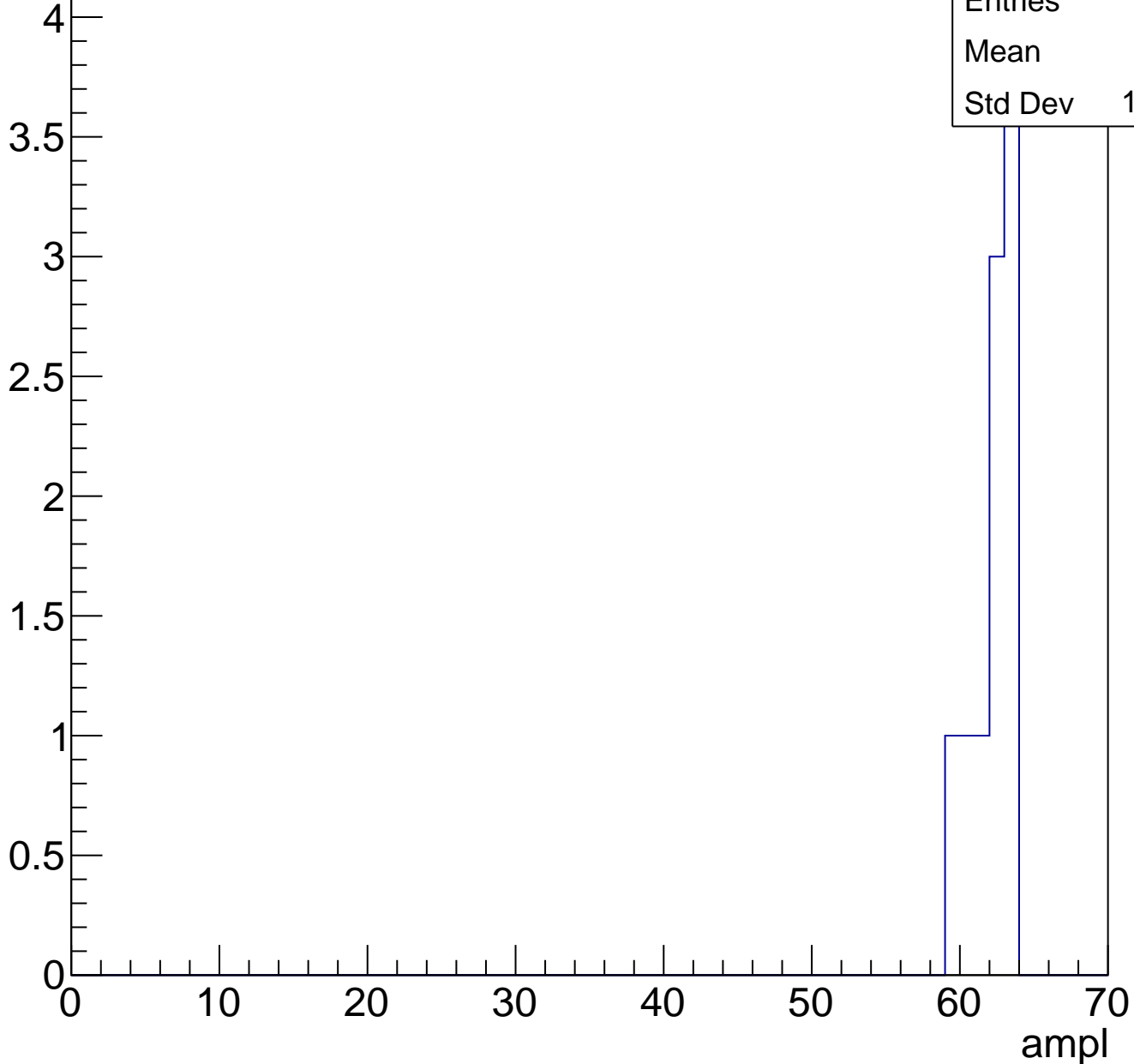
Entry



# B1L103S, U25-ch45, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	10
Mean	61.8
Std Dev	1.327



# B1L103S, U25-ch45, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

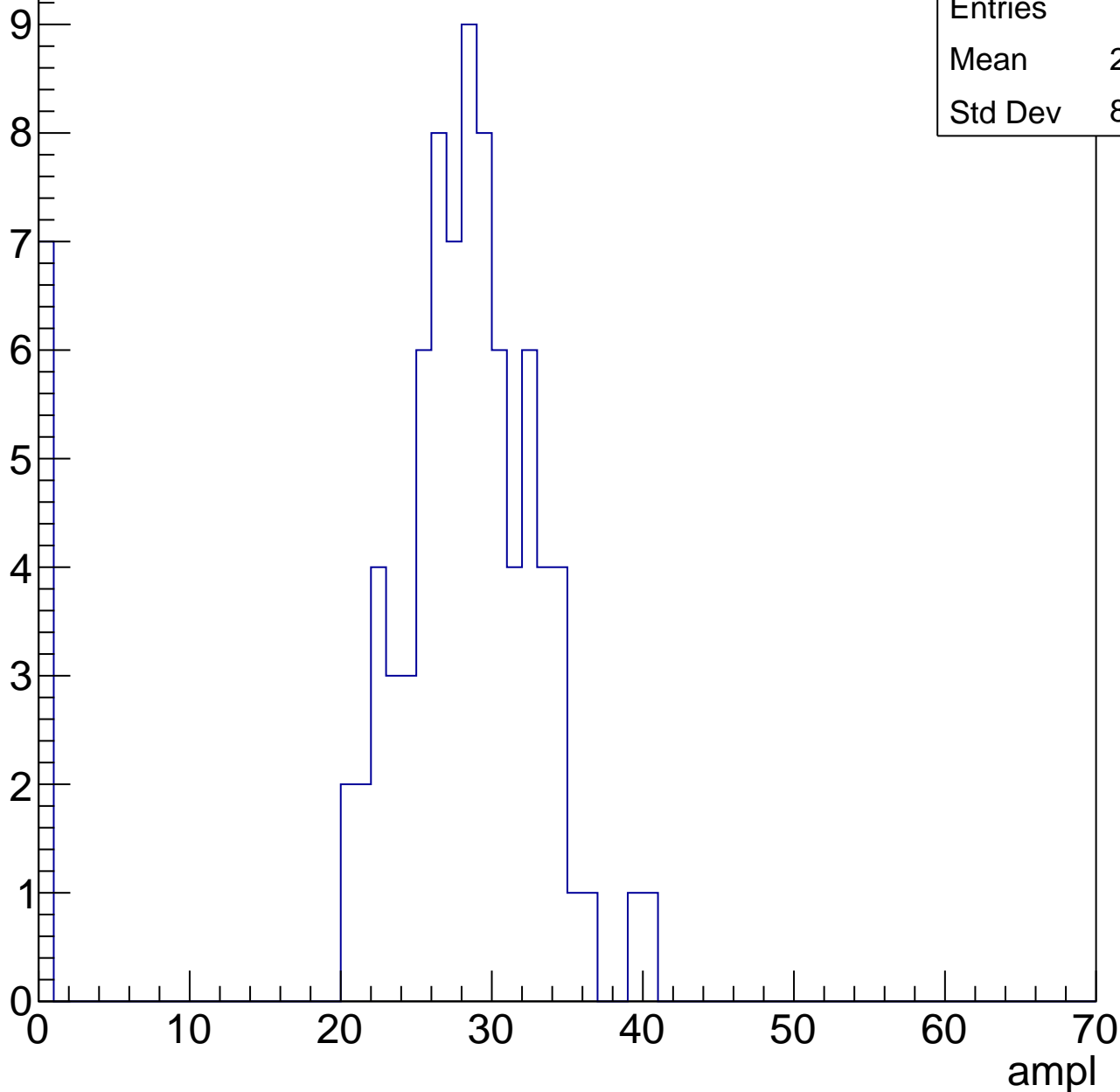
Entries	19
Mean	0
Std Dev	0

# B1L103S, U25-ch46, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	87
Mean	25.93
Std Dev	8.635

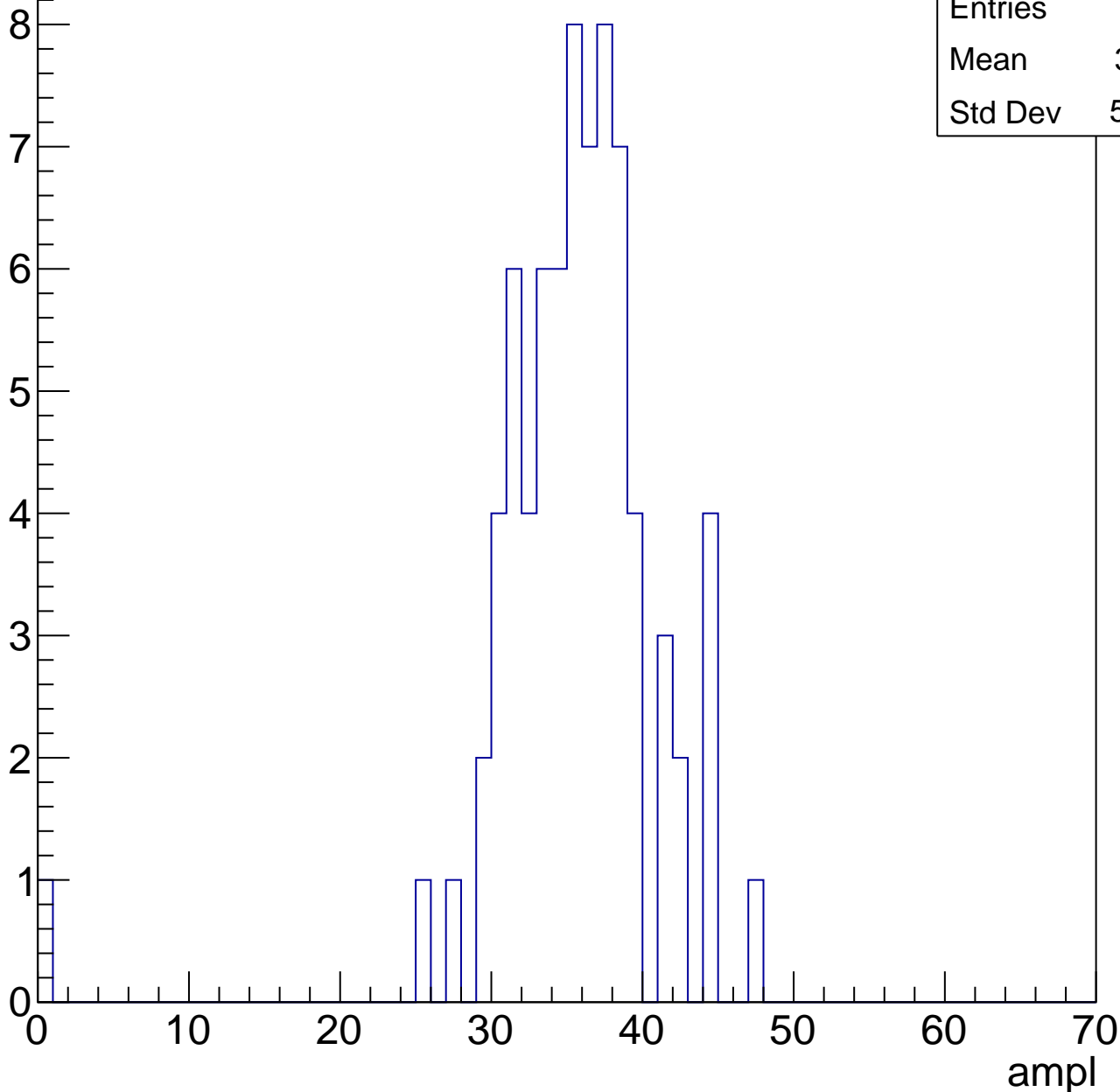


# B1L103S, U25-ch46, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	75
Mean	35.01
Std Dev	5.846



# B1L103S, U25-ch46, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

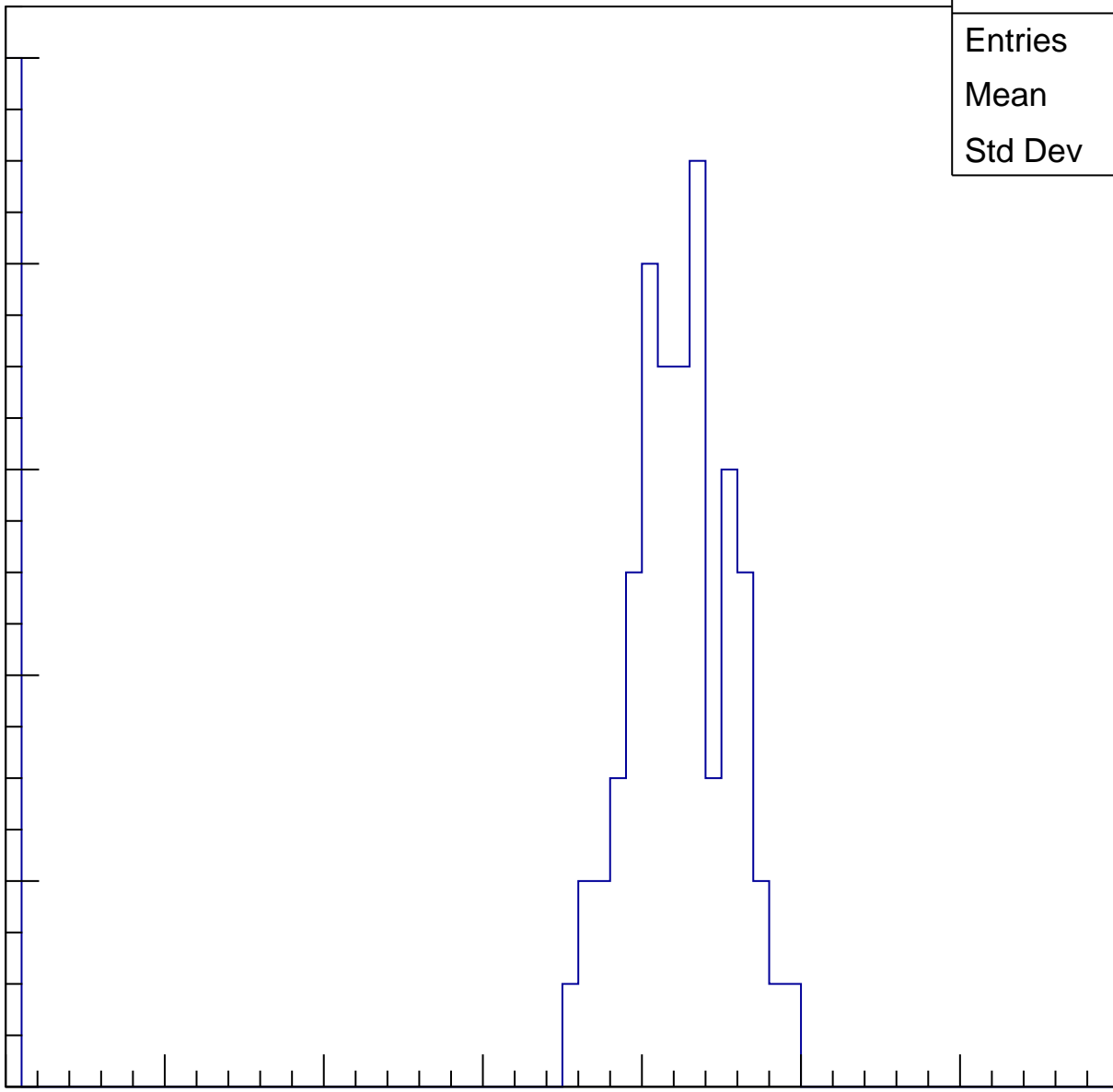
Entries	72
Mean	36.12
Std Dev	14.79

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

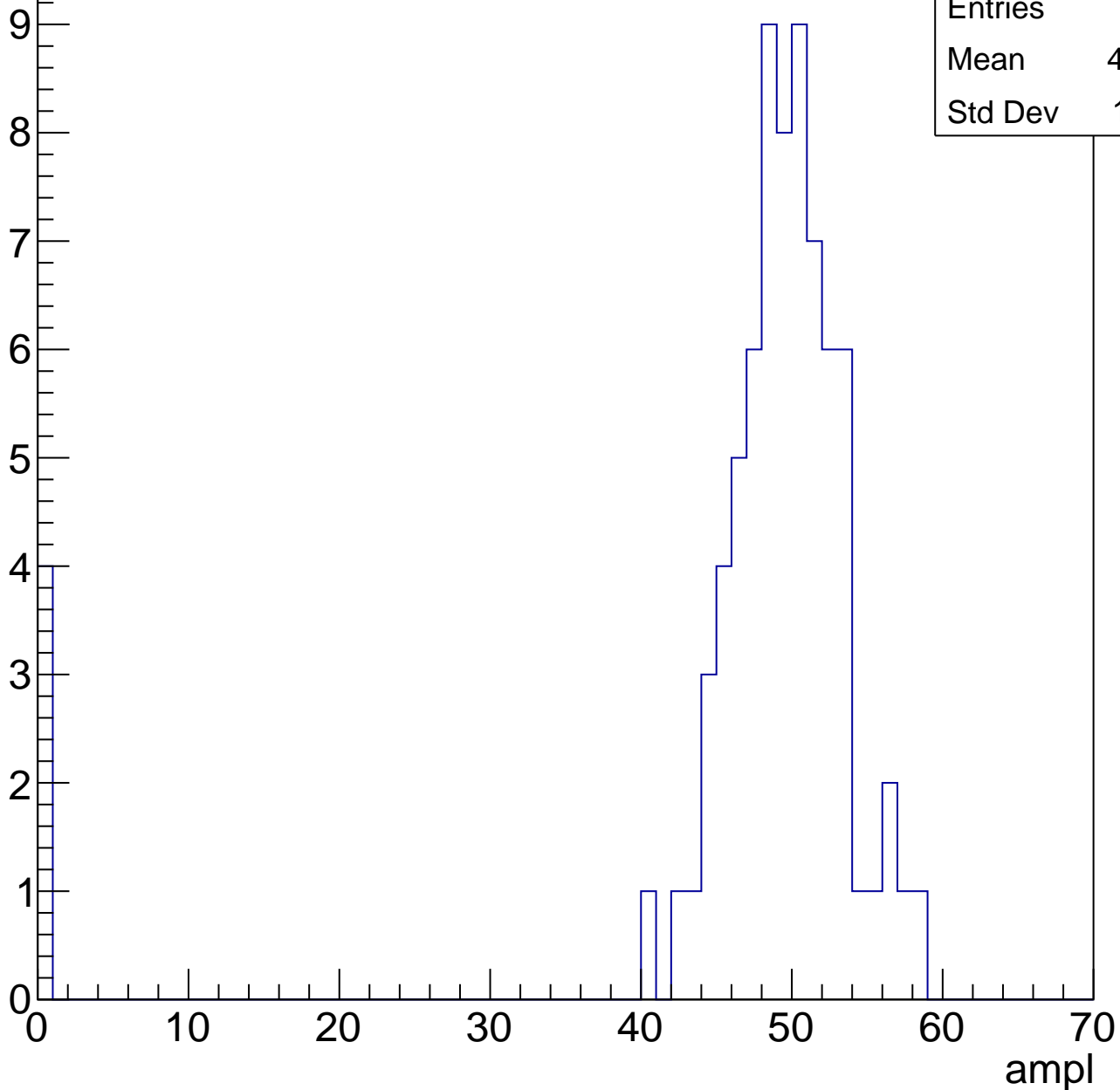


# B1L103S, U25-ch46, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

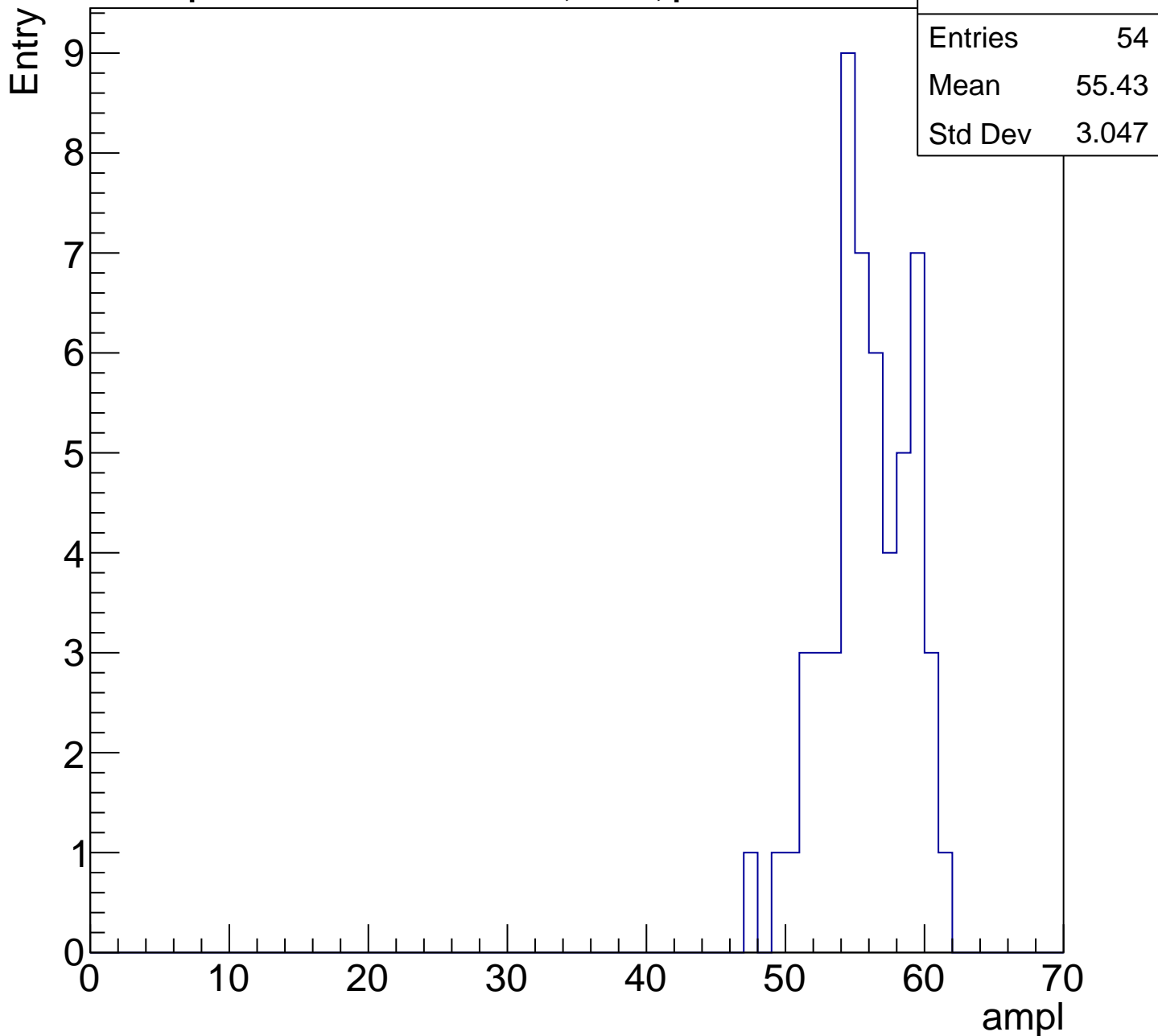
Entry

Entries	76
Mean	46.66
Std Dev	11.51



# B1L103S, U25-ch46, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

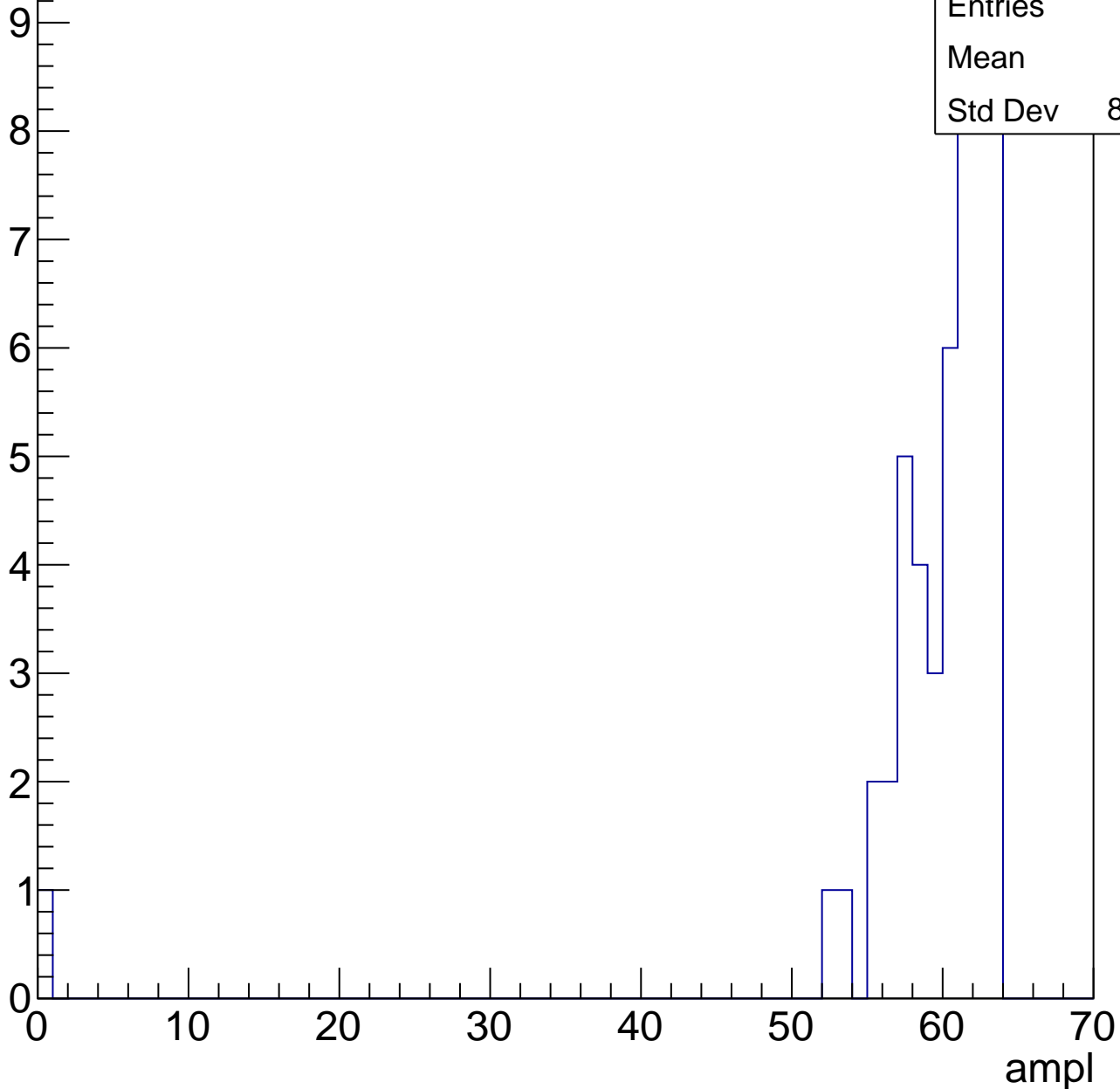


# B1L103S, U25-ch46, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	50
Mean	58.6
Std Dev	8.802



# B1L103S, U25-ch46, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	5
Mean	62
Std Dev	1.095



# B1L103S, U25-ch46, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	18
Mean	0
Std Dev	0

# B1L103S, U25-ch47, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	75
Mean	24.04
Std Dev	11.45

Entry

12

10

8

6

4

2

0

0

10

20

30

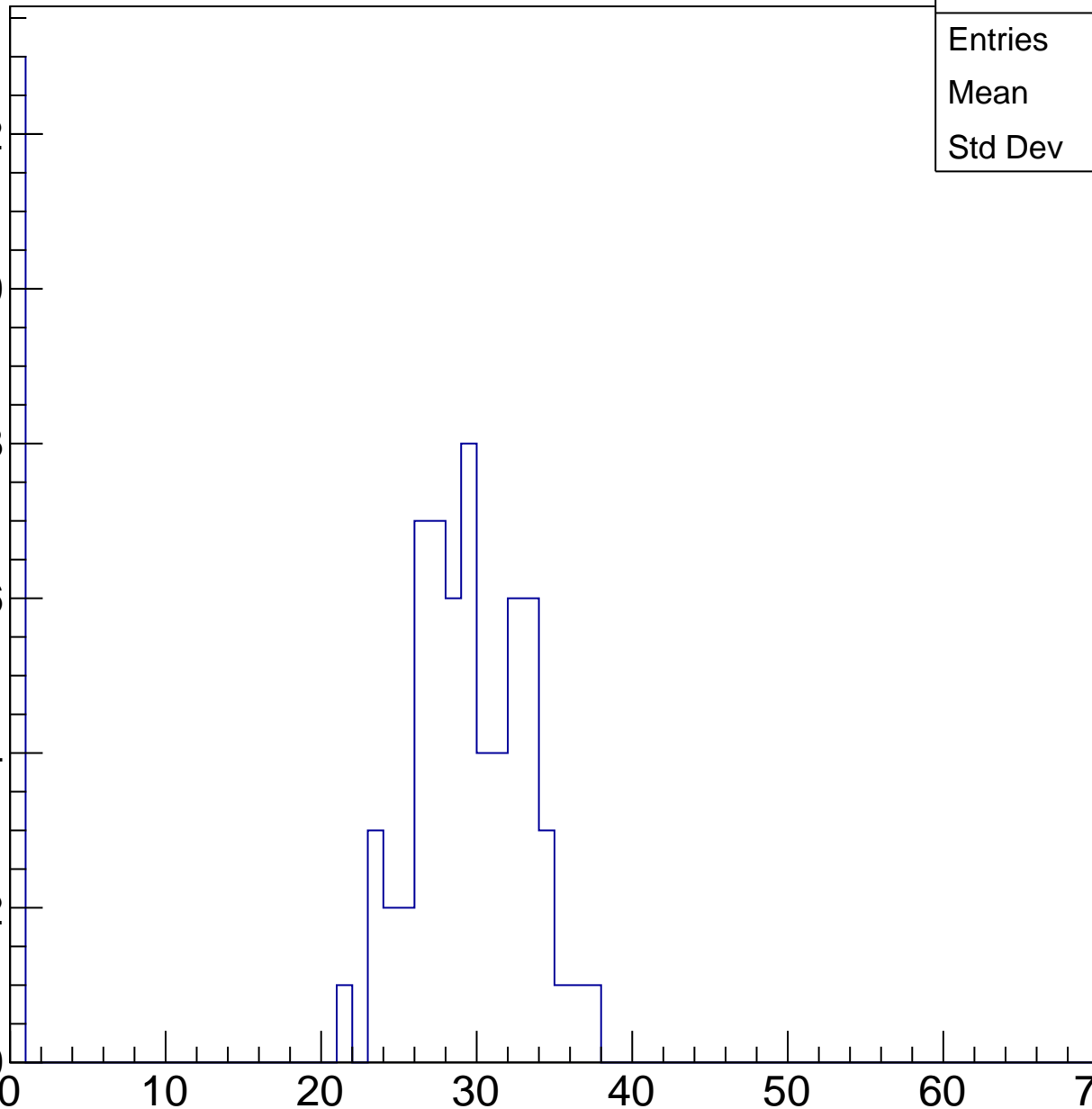
40

50

60

70

ampl

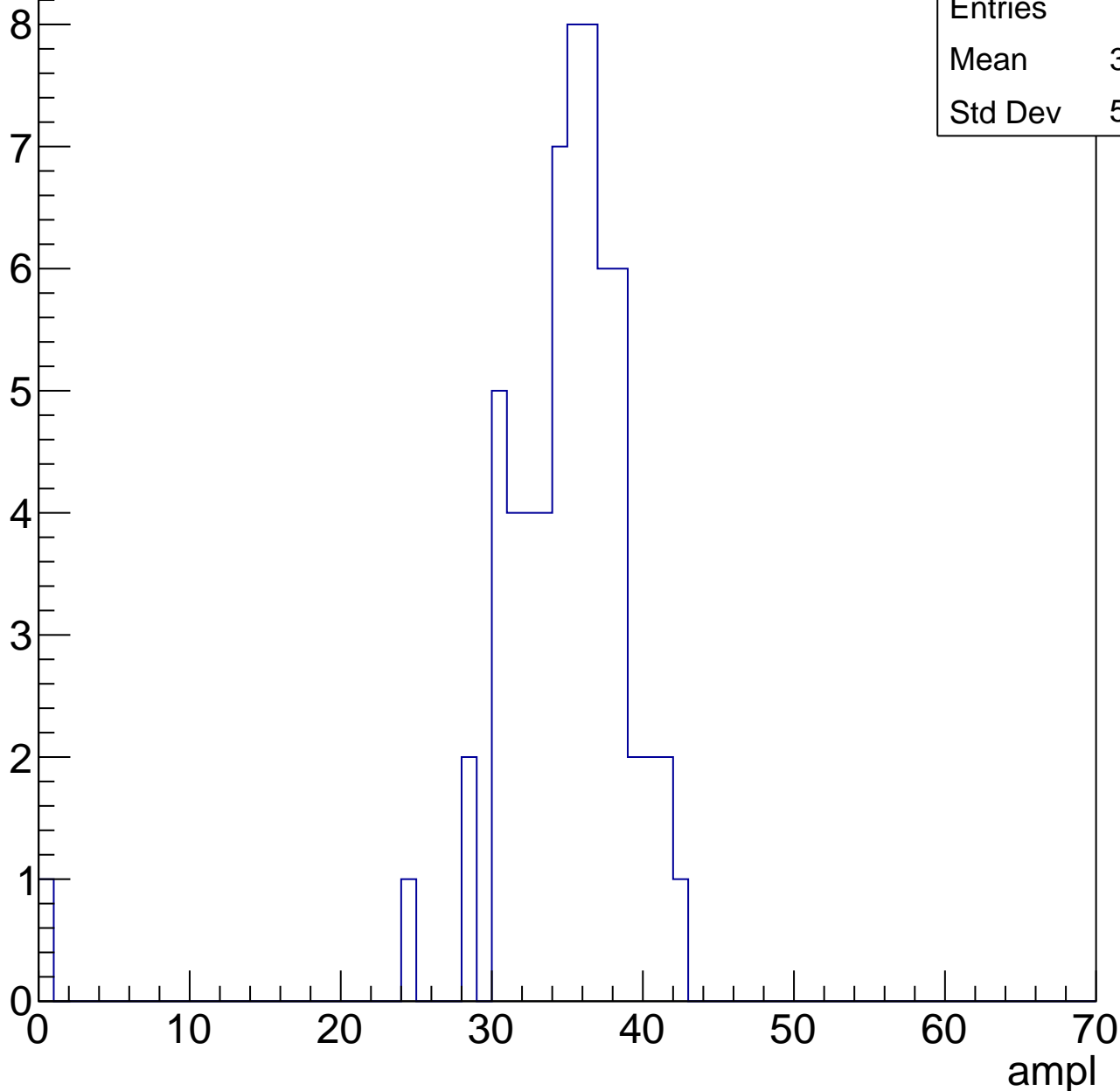


# B1L103S, U25-ch47, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

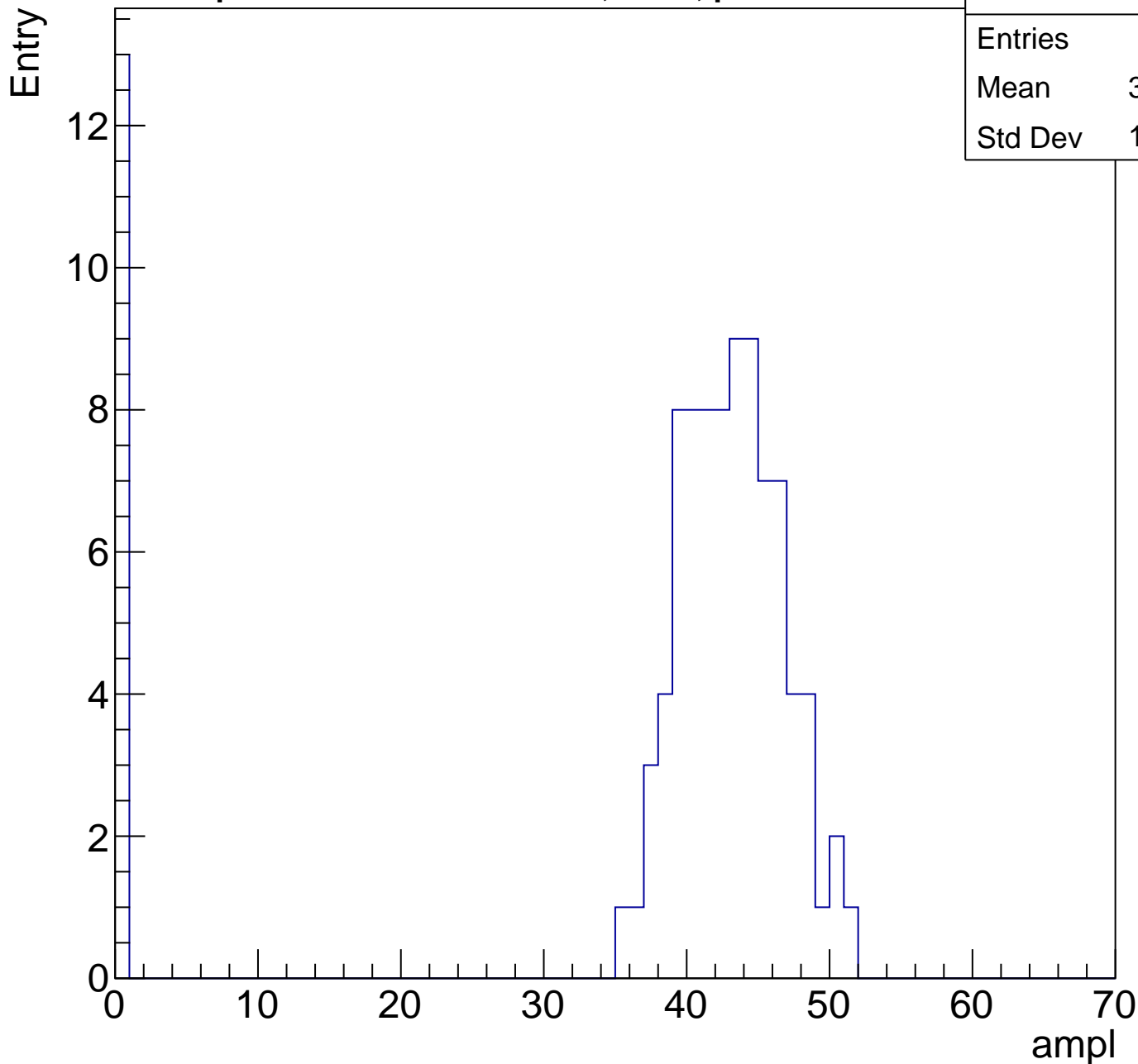
Entries	63
Mean	34.16
Std Dev	5.544



# B1L103S, U25-ch47, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	98
Mean	37.04
Std Dev	14.84

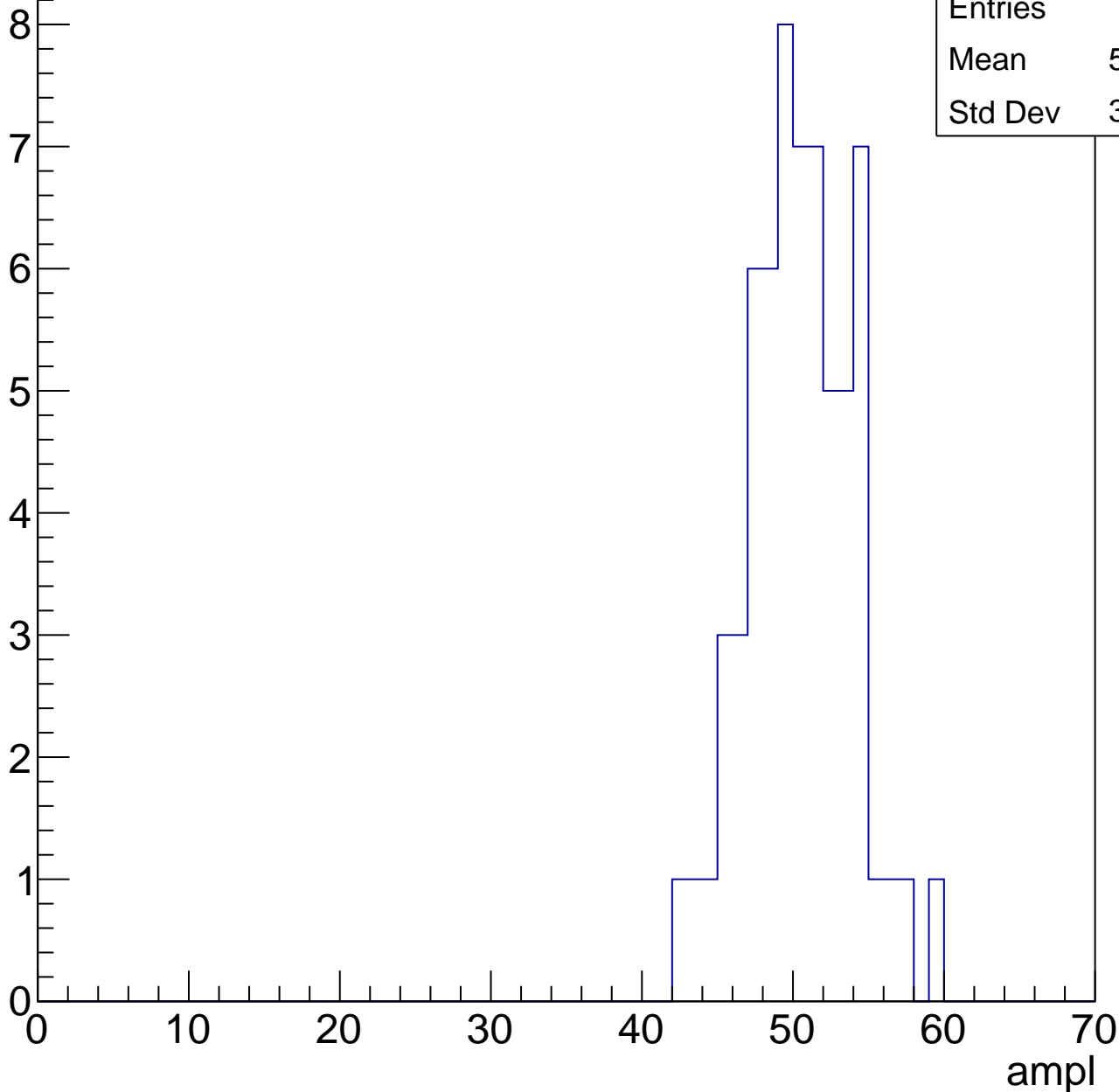


# B1L103S, U25-ch47, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	64
Mean	50.02
Std Dev	3.384

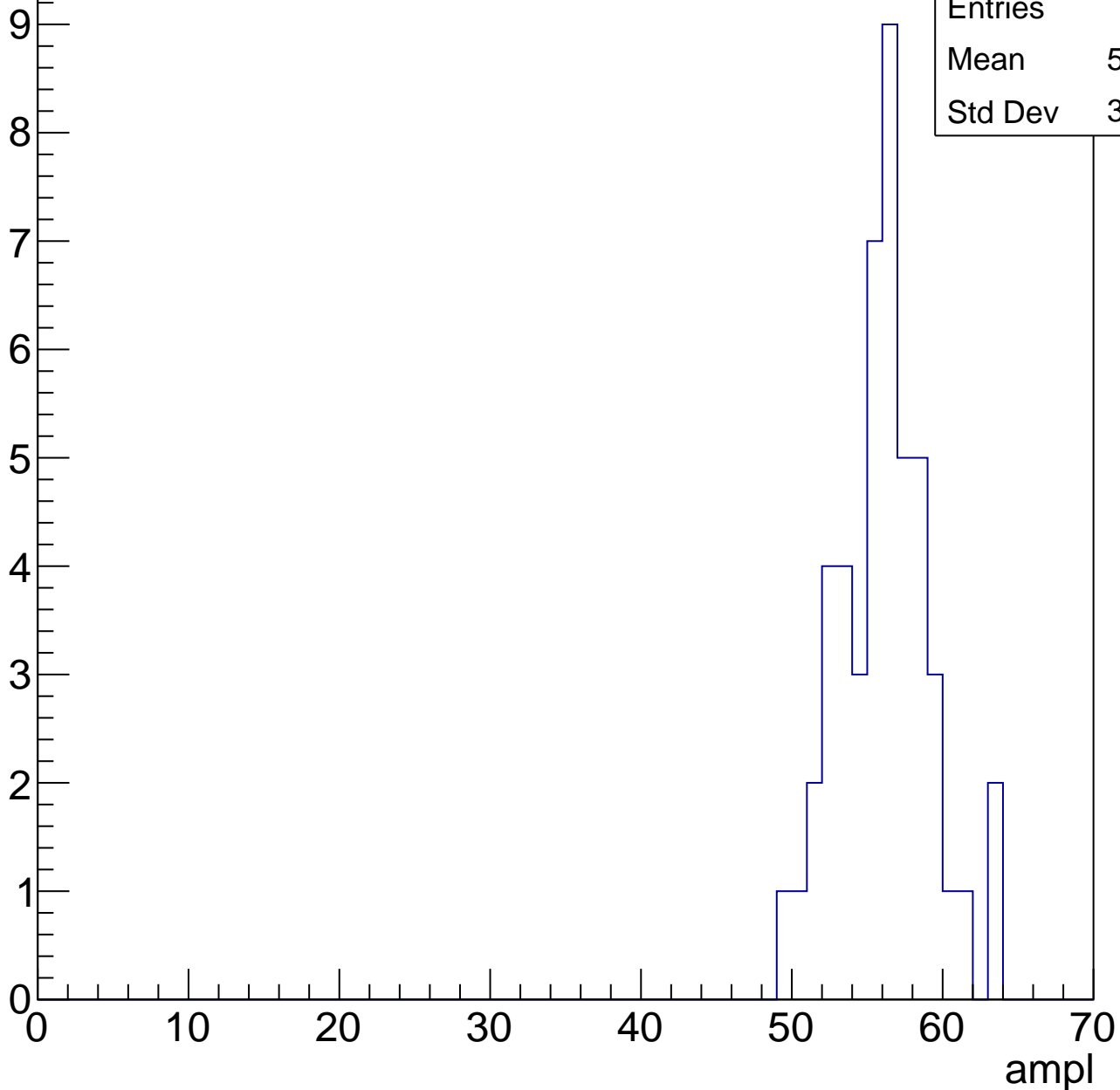


# B1L103S, U25-ch47, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	48
Mean	55.65
Std Dev	3.024

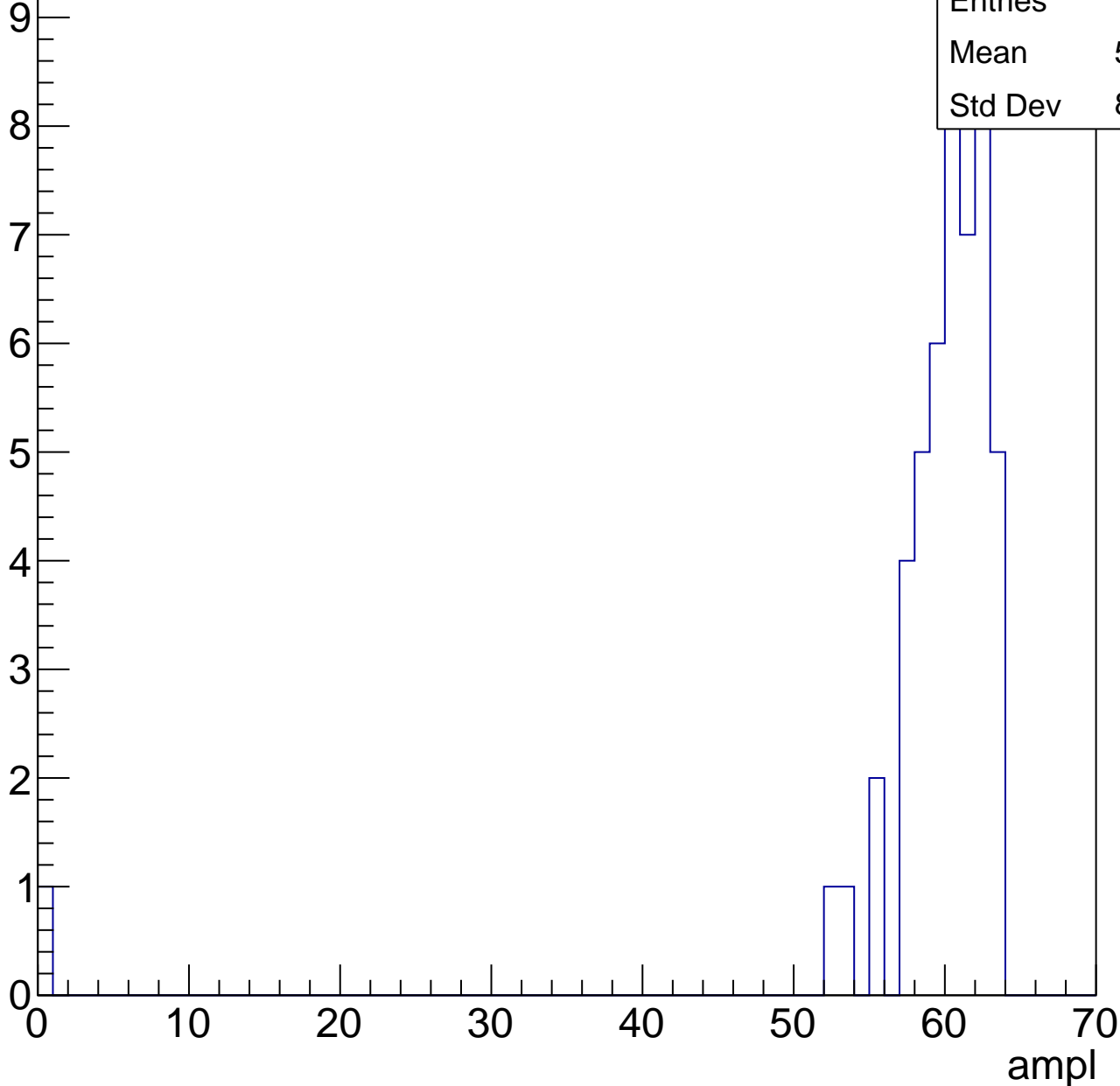


# B1L103S, U25-ch47, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	49
Mean	58.51
Std Dev	8.811



# B1L103S, U25-ch47, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	7
Mean	61.86
Std Dev	1.125



# B1L103S, U25-ch47, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U25-ch48, adc0

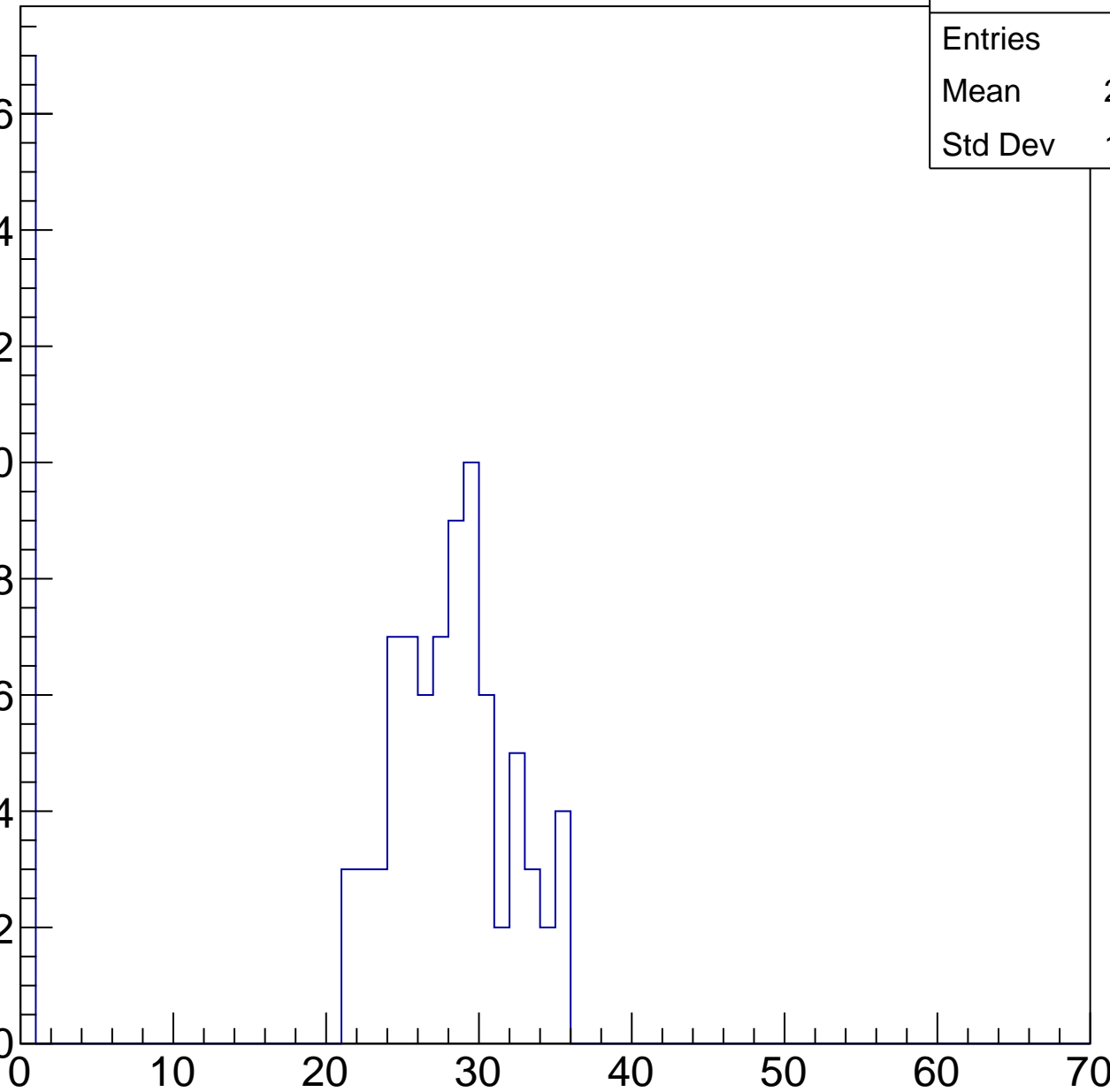
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	94
Mean	22.73
Std Dev	11.17

Entry

16  
14  
12  
10  
8  
6  
4  
2  
0

ampl

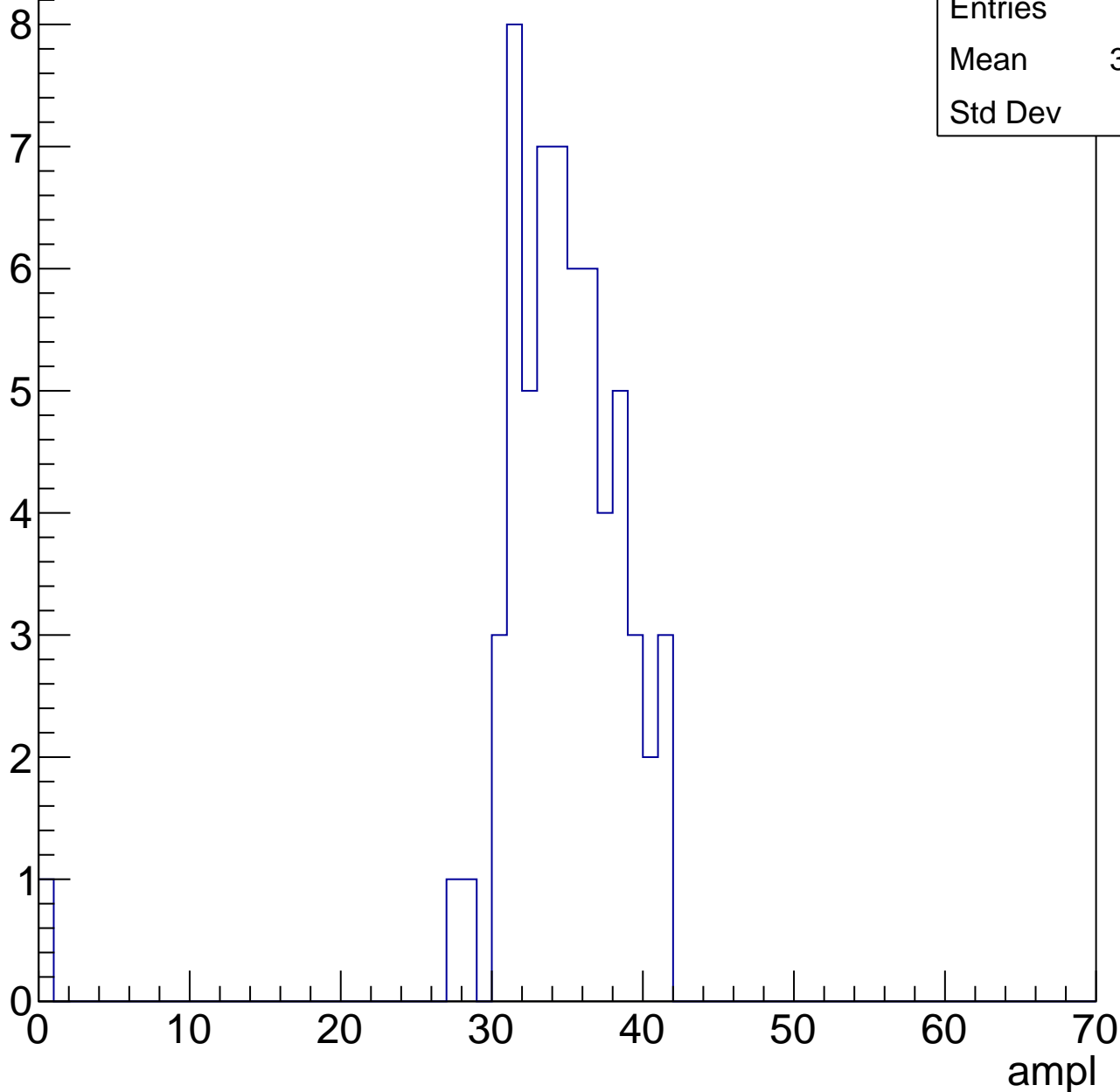


# B1L103S, U25-ch48, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	62
Mean	33.97
Std Dev	5.43

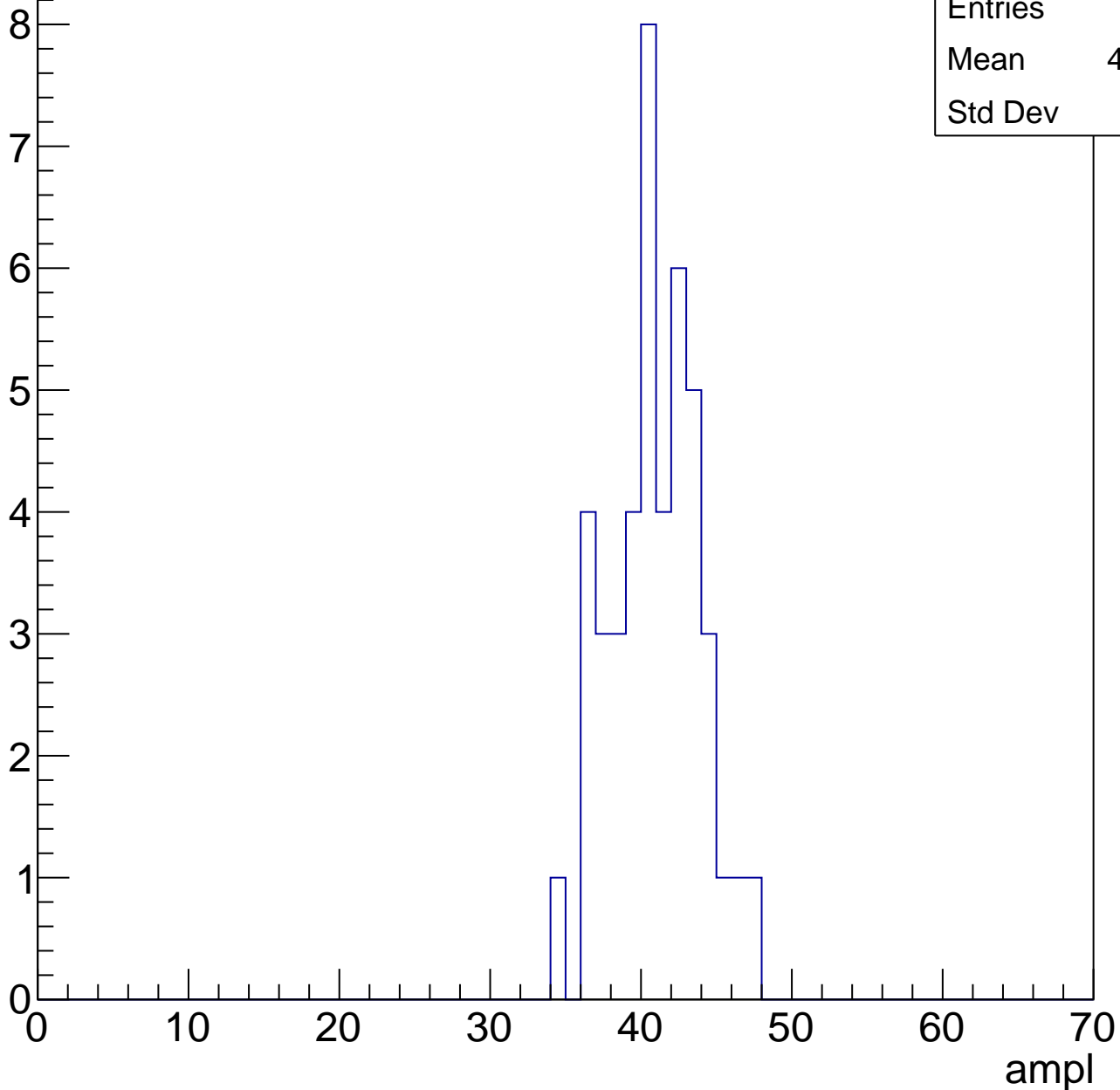


# B1L103S, U25-ch48, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	44
Mean	40.45
Std Dev	2.88

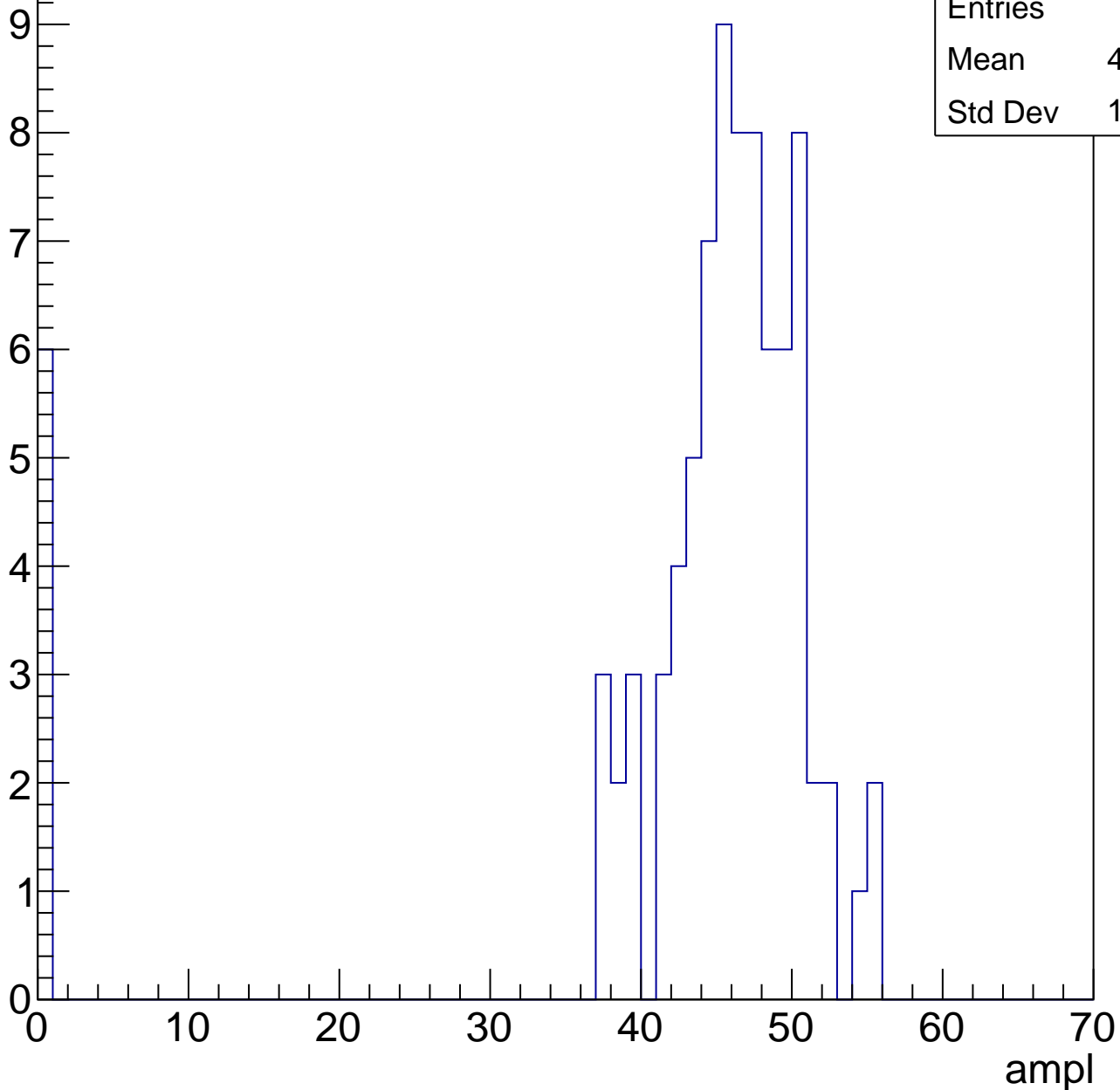


# B1L103S, U25-ch48, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	85
Mean	42.58
Std Dev	12.37

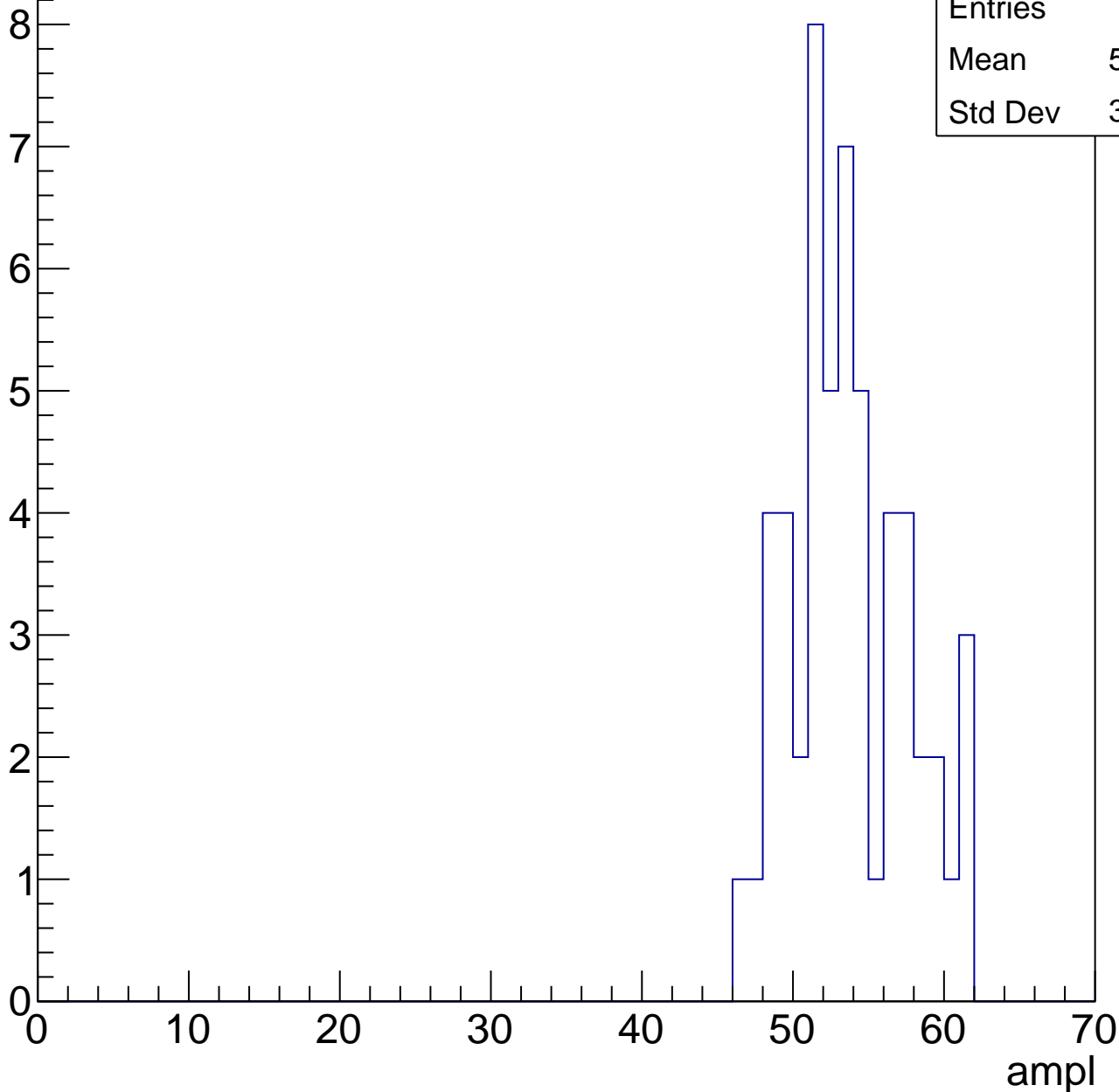


# B1L103S, U25-ch48, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	54
Mean	53.22
Std Dev	3.784

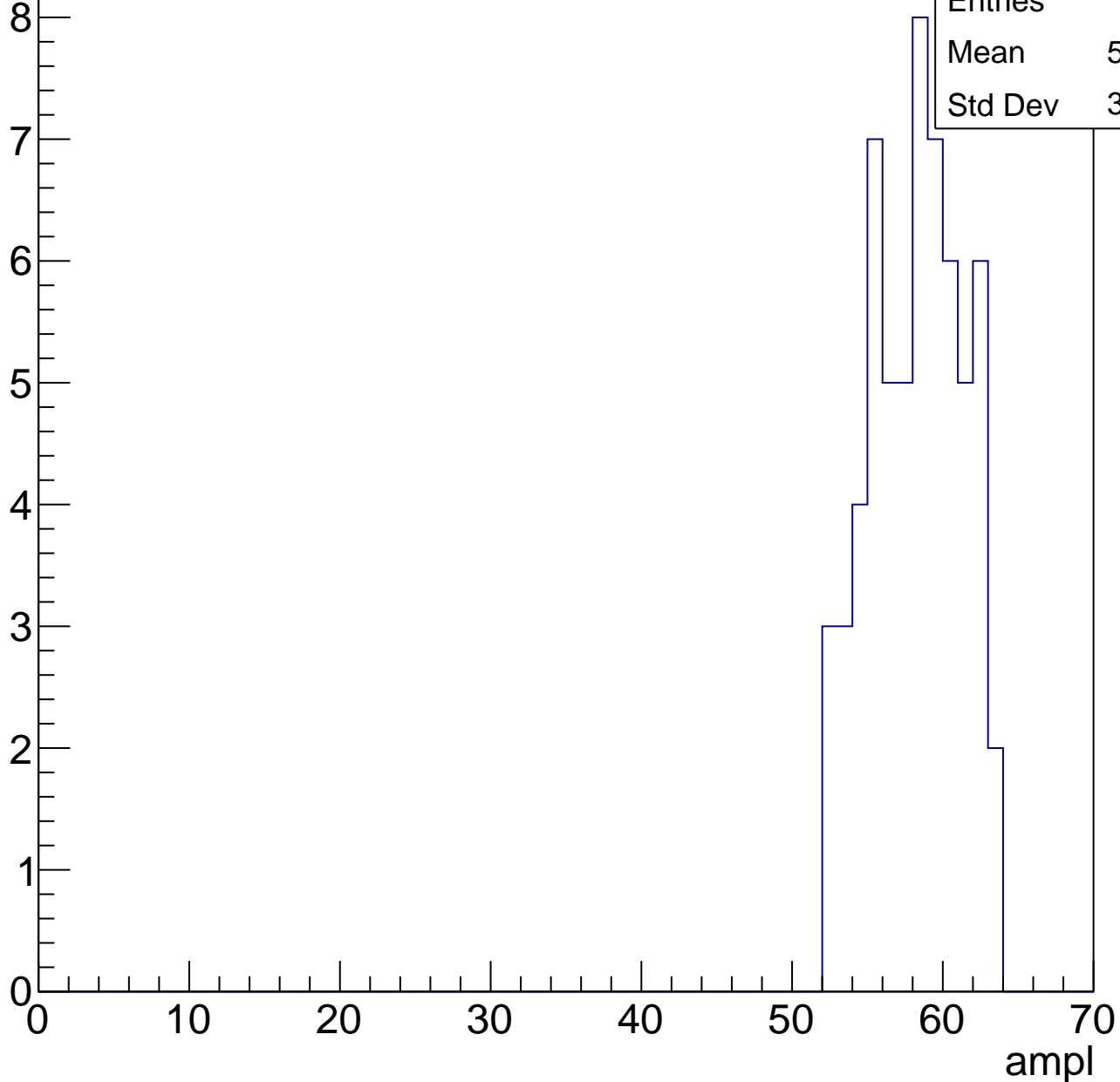


# B1L103S, U25-ch48, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	61
Mean	57.72
Std Dev	3.009

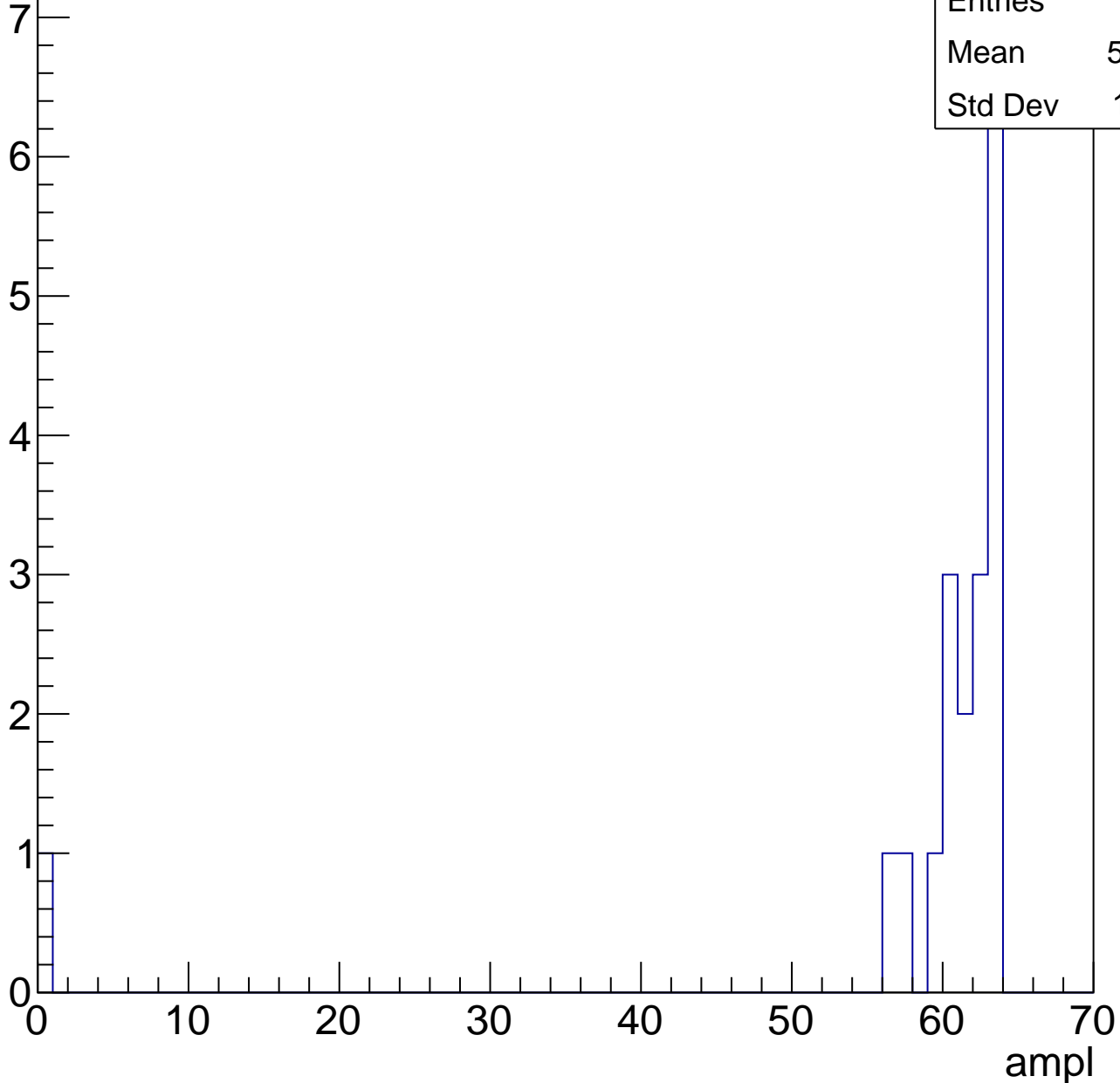


# B1L103S, U25-ch48, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	19
Mean	57.95
Std Dev	13.81





# B1L103S, U25-ch48, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	21
Mean	5.952
Std Dev	18.35

Entry

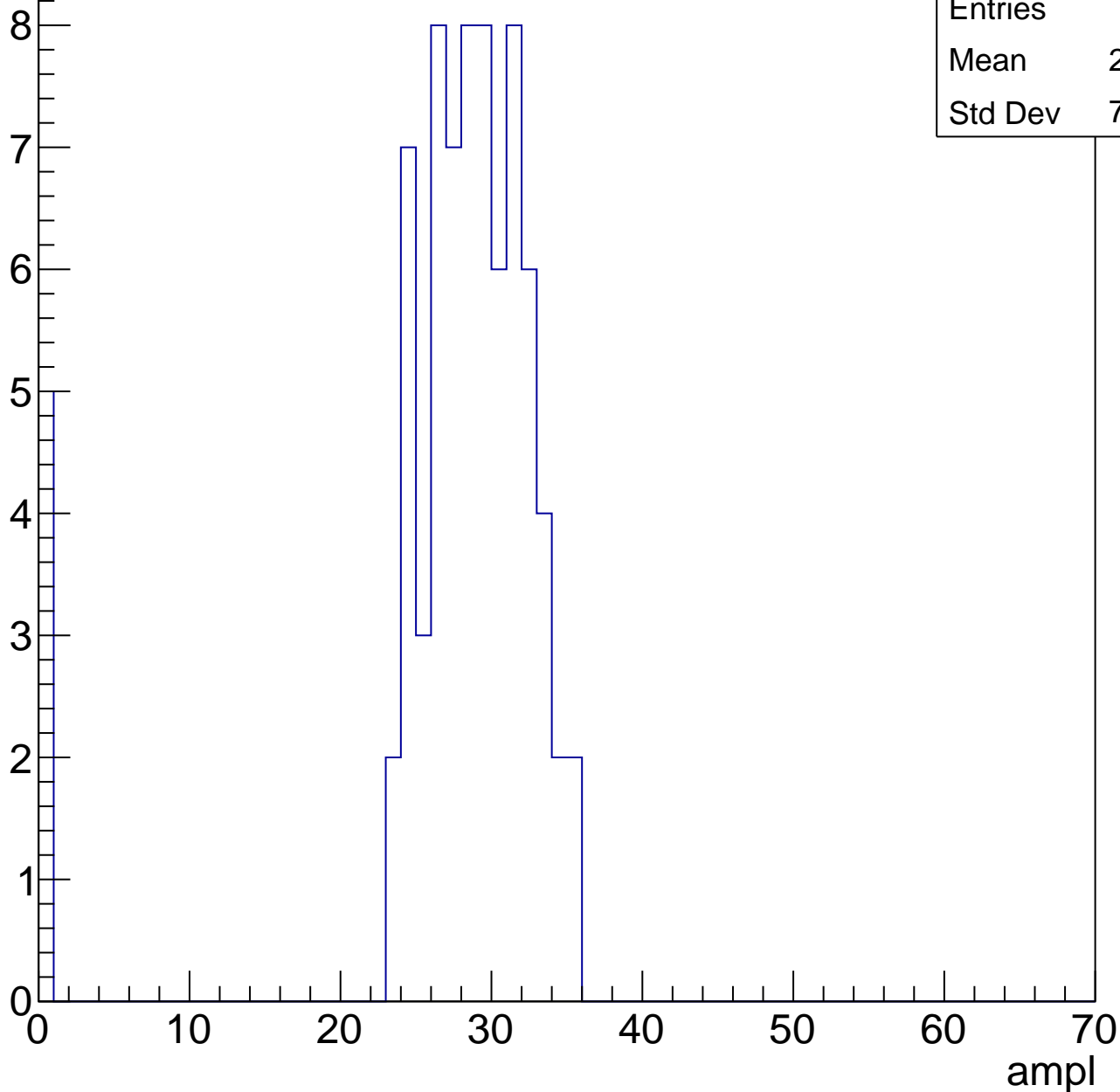


# B1L103S, U25-ch49, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

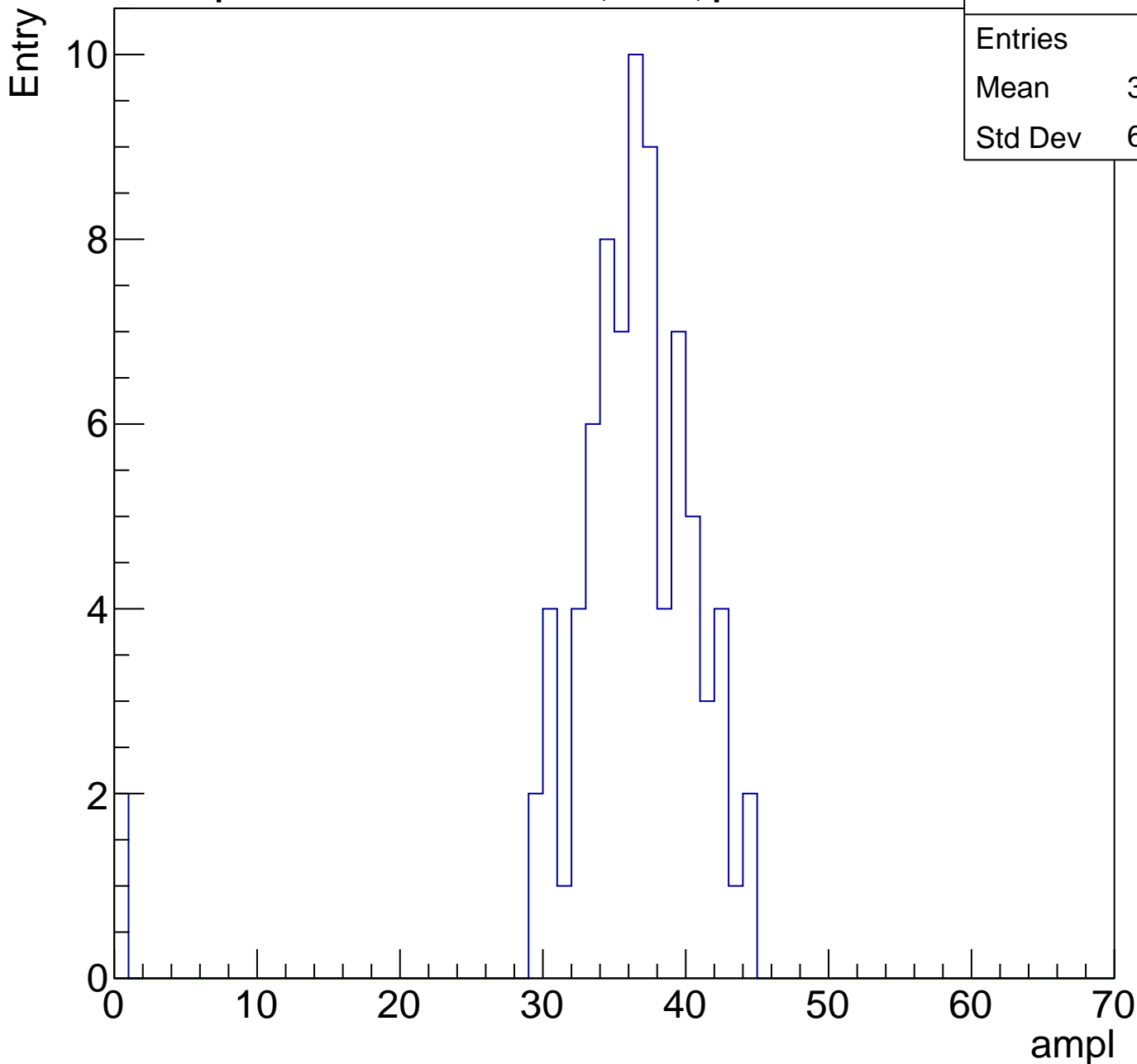
Entries	76
Mean	26.74
Std Dev	7.692



# B1L103S, U25-ch49, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	79
Mean	35.34
Std Dev	6.699

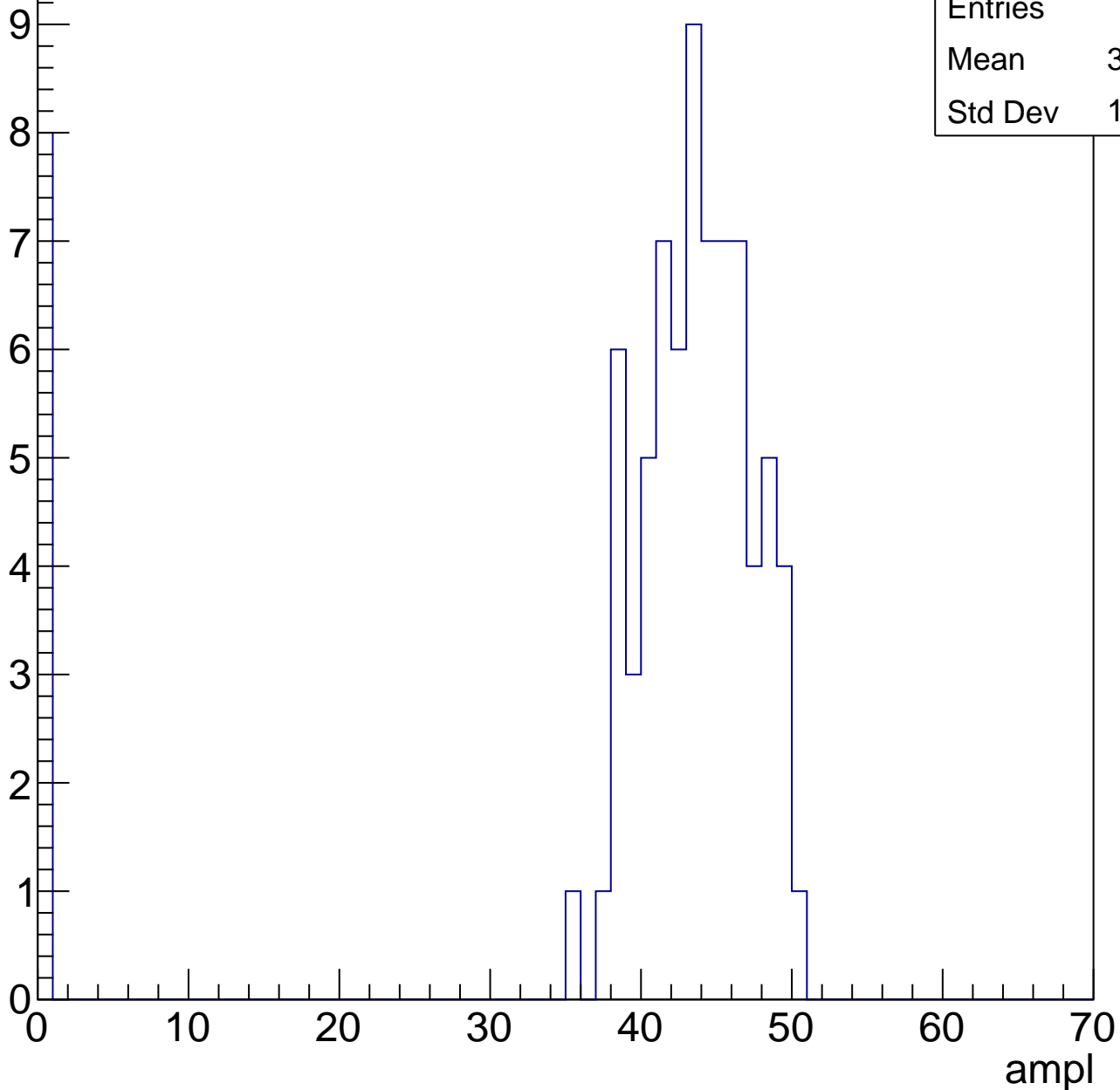


# B1L103S, U25-ch49, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	81
Mean	39.04
Std Dev	13.32

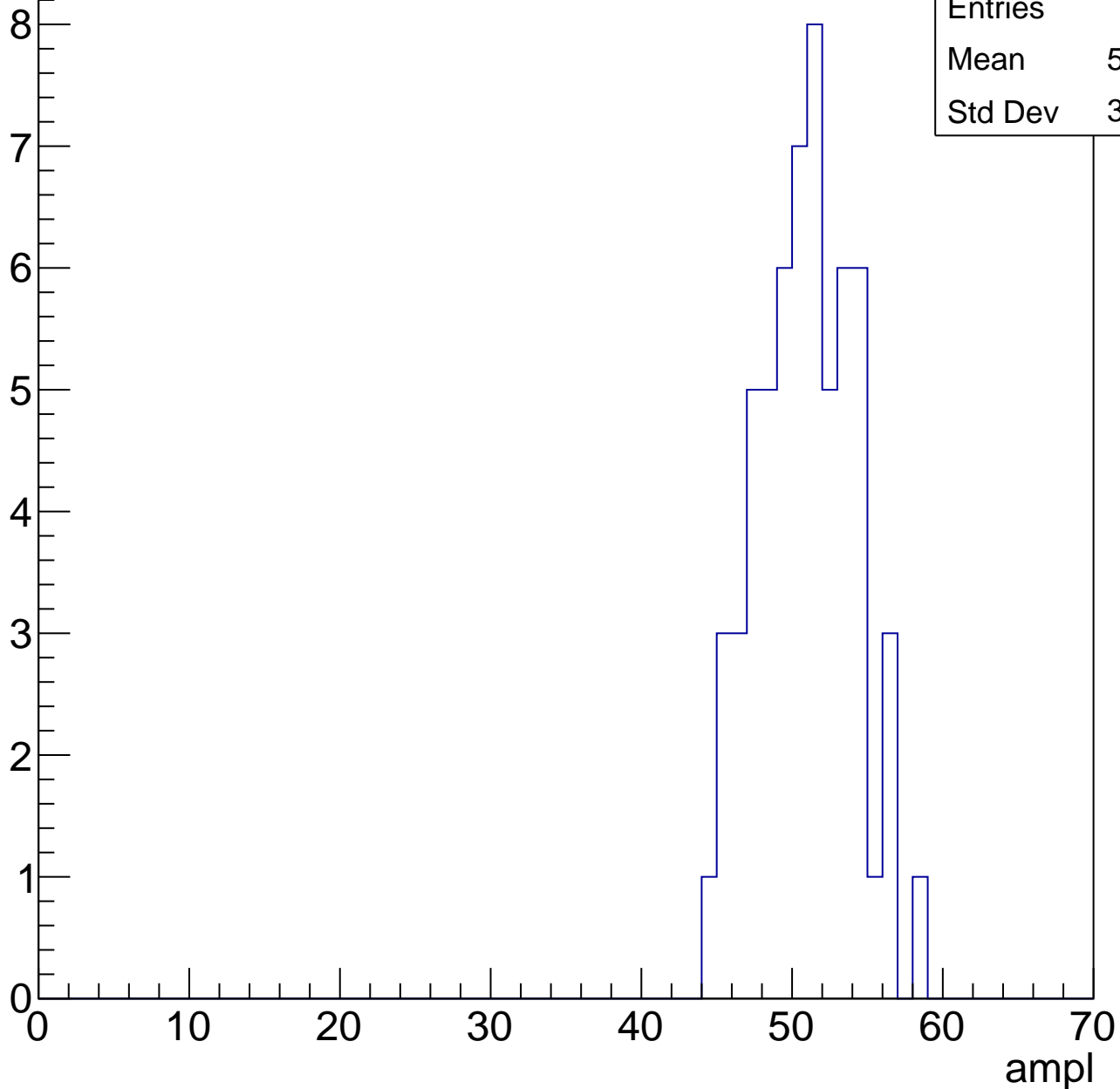


# B1L103S, U25-ch49, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	60
Mean	50.45
Std Dev	3.143

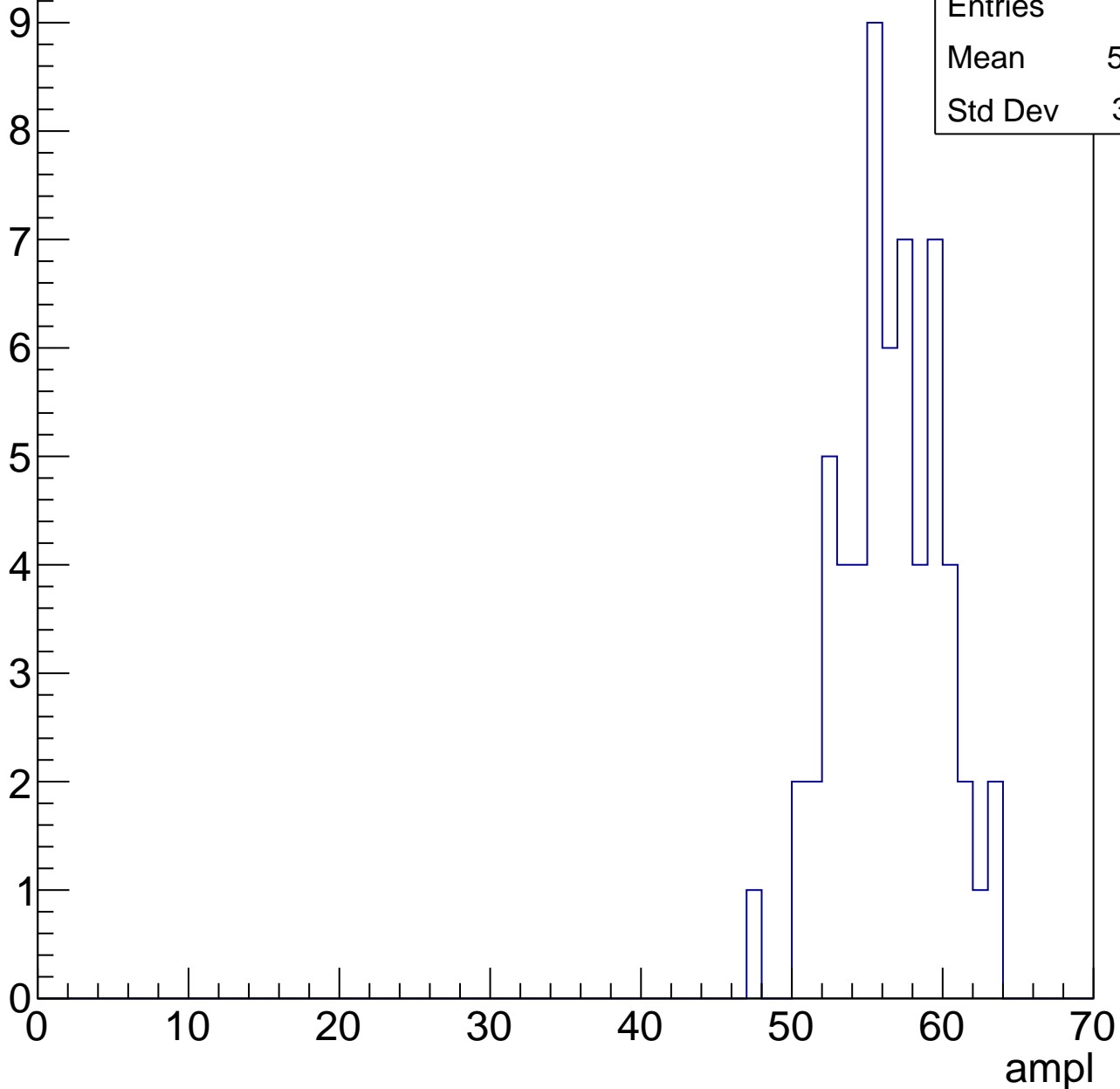


# B1L103S, U25-ch49, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	60
Mean	56.03
Std Dev	3.361

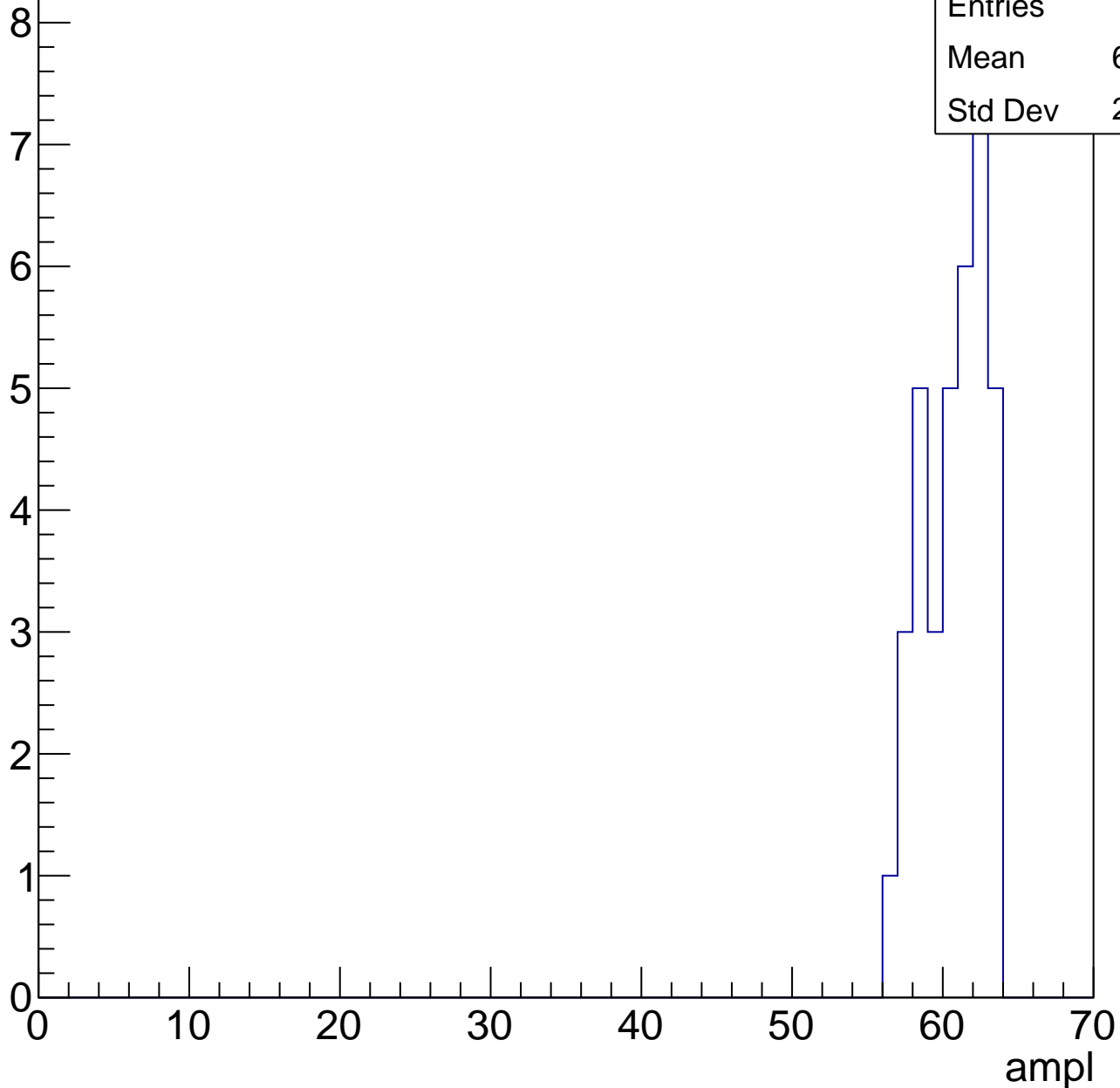


# B1L103S, U25-ch49, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

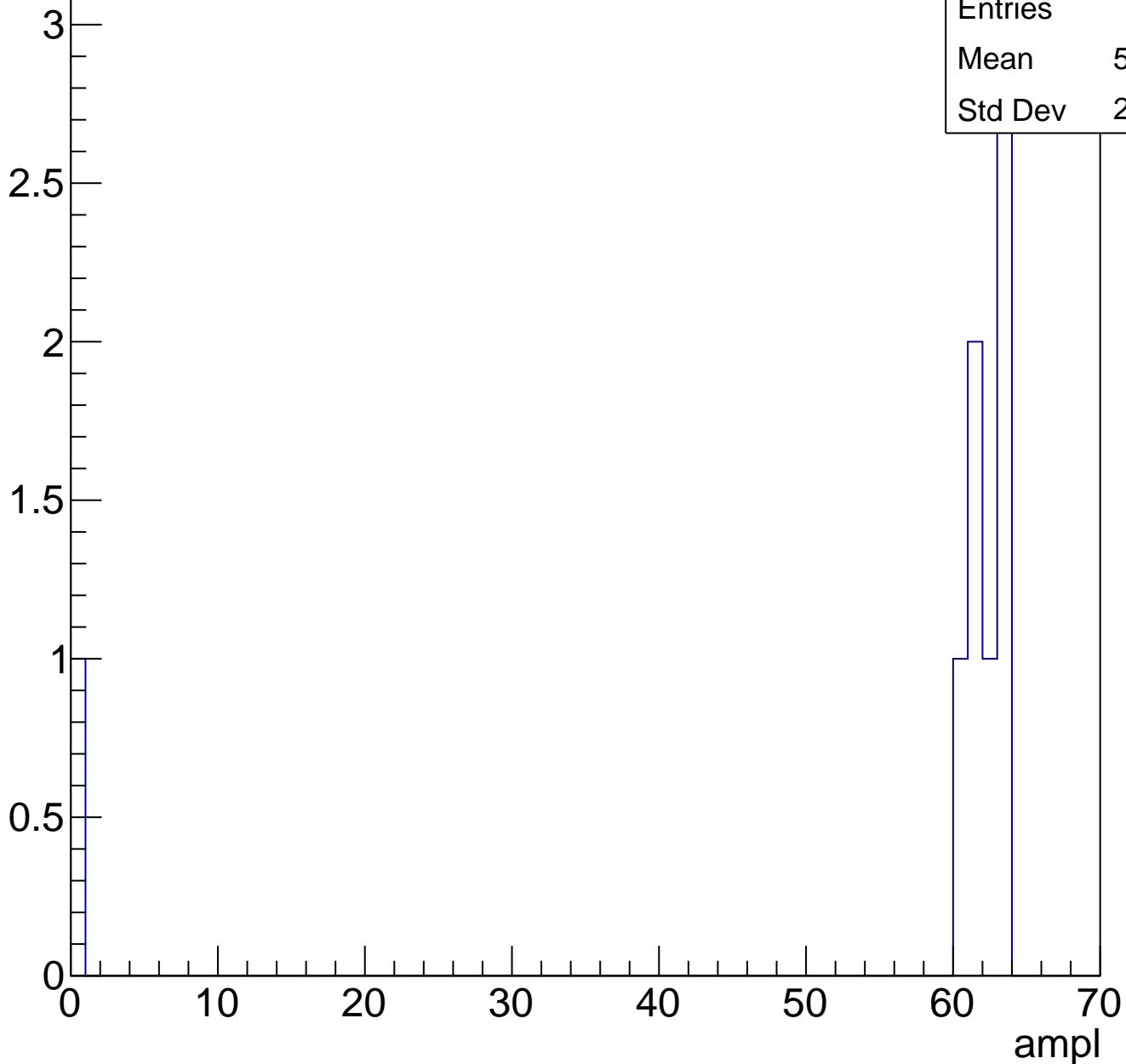
Entries	36
Mean	60.31
Std Dev	2.011



# B1L103S, U25-ch49, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U25-ch49, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

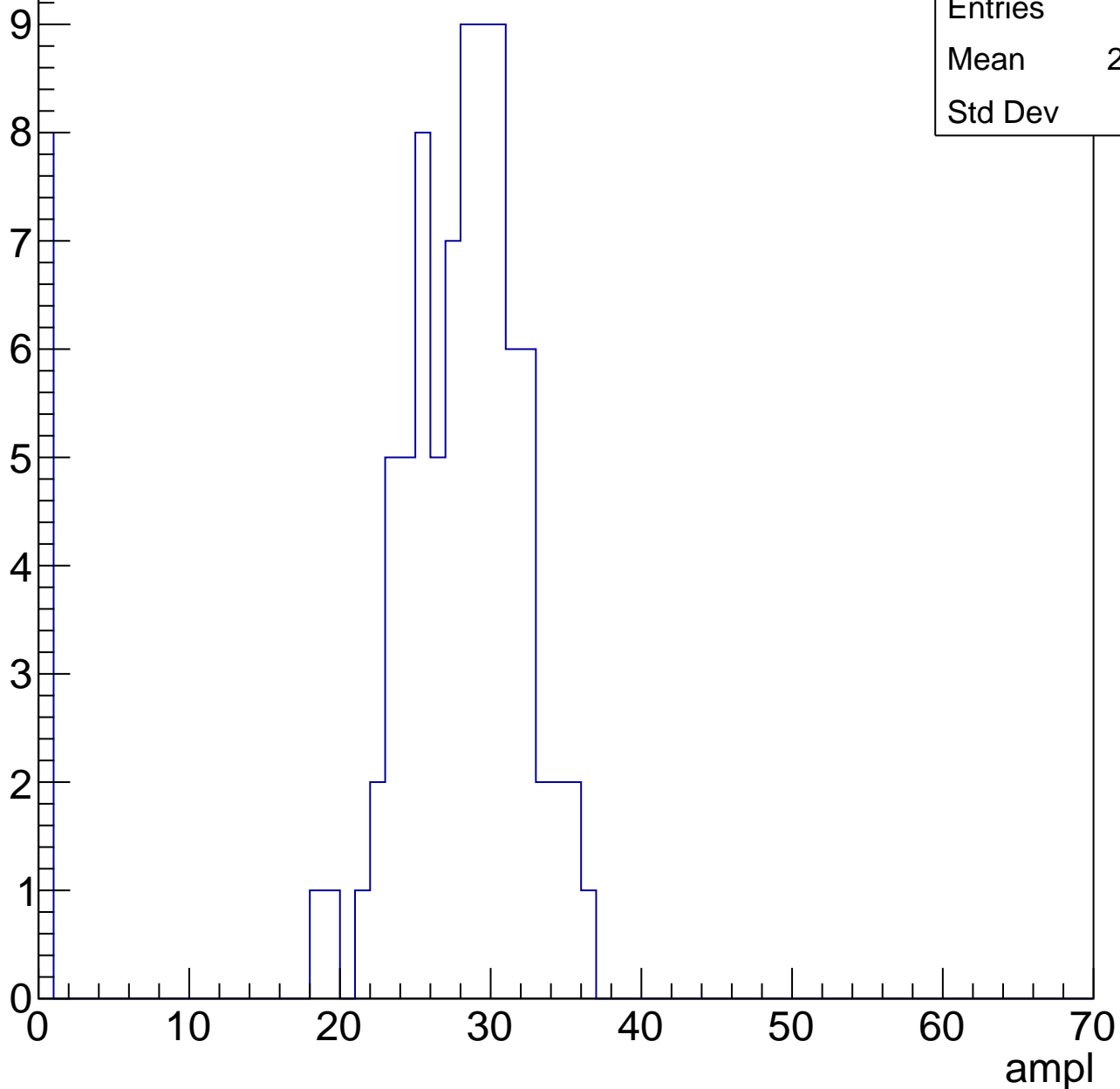
ampl

Entries	19
Mean	0
Std Dev	0

# B1L103S, U25-ch50, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

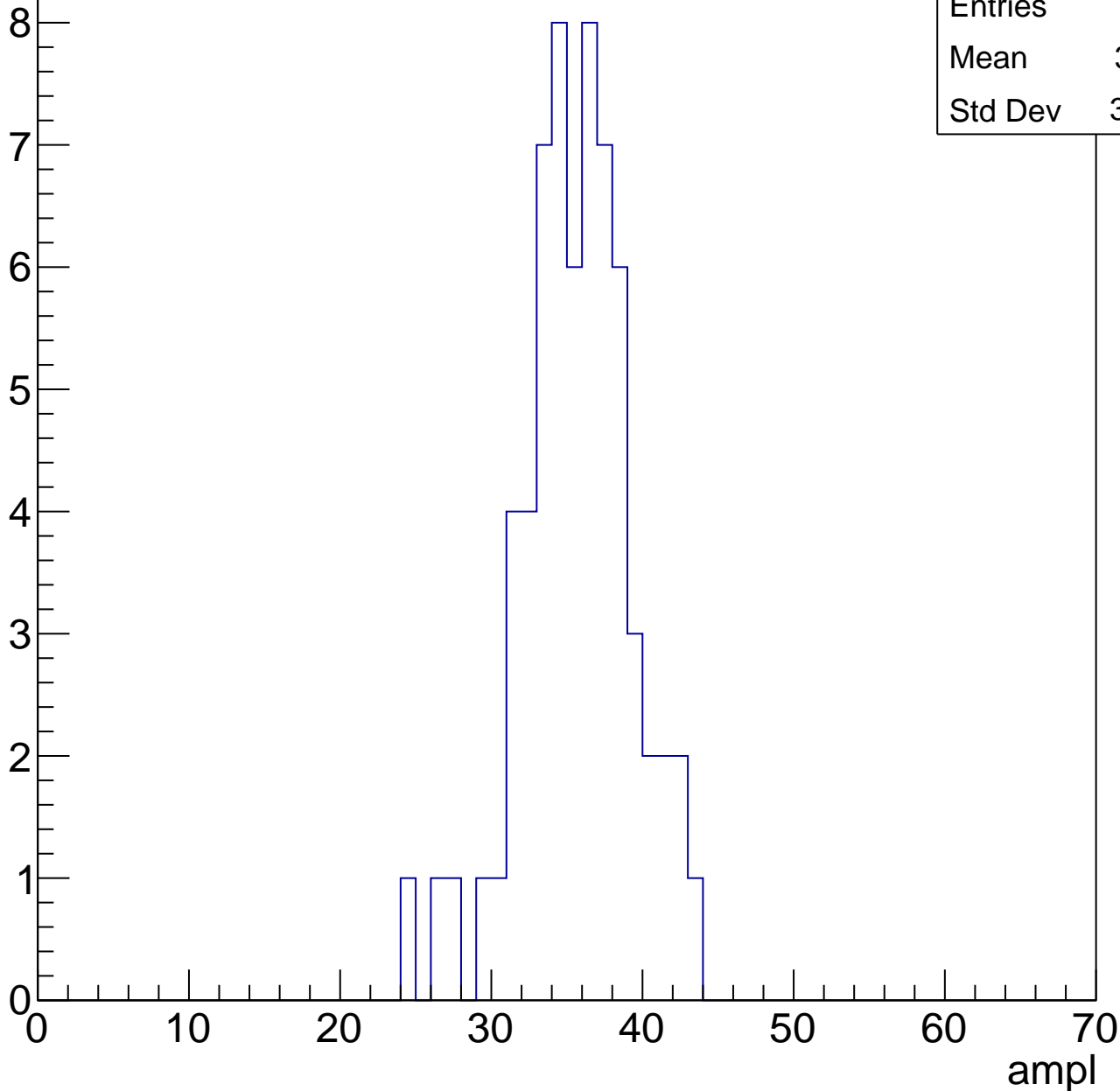


# B1L103S, U25-ch50, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	65
Mean	35.11
Std Dev	3.688

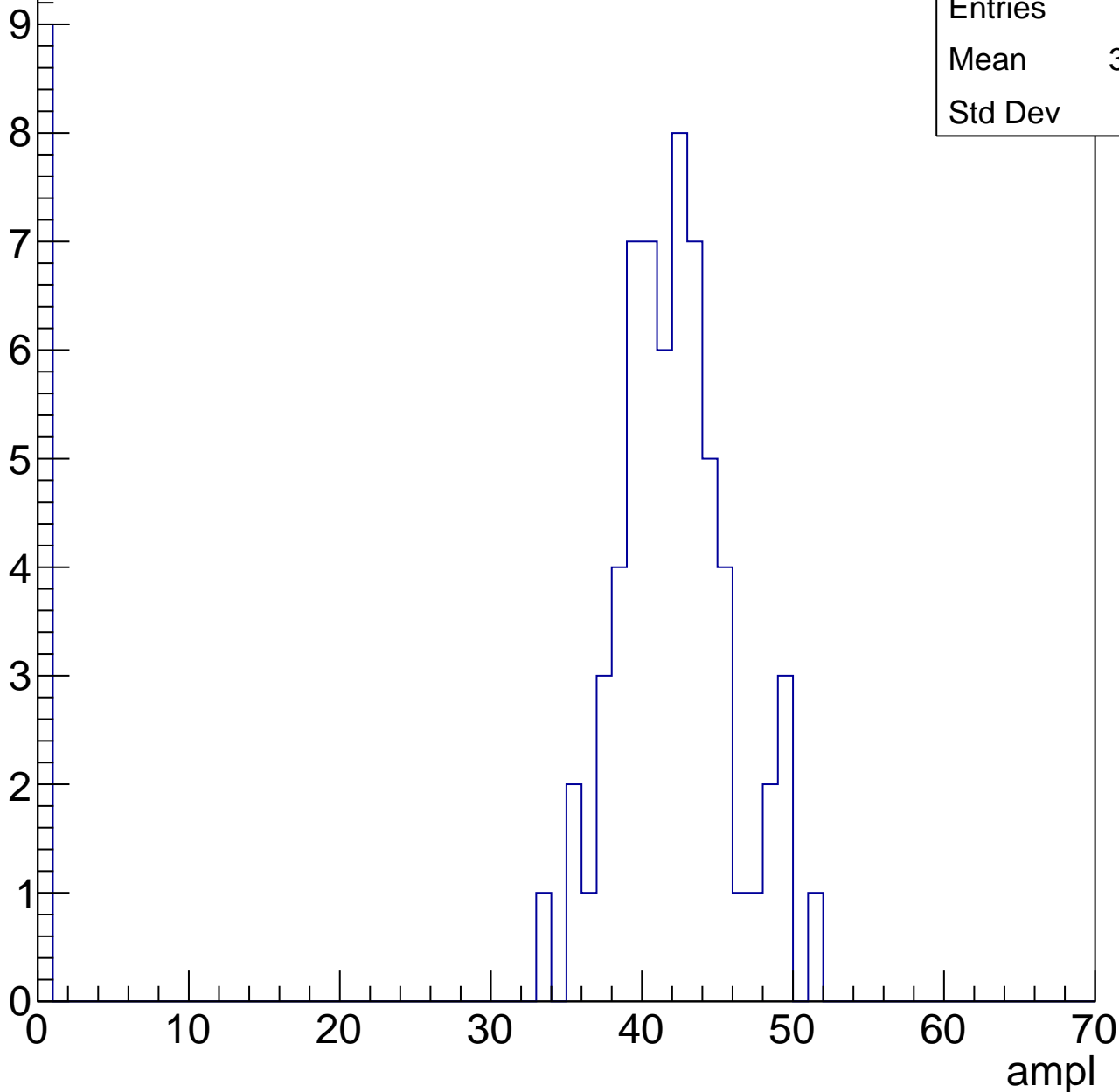


# B1L103S, U25-ch50, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	72
Mean	36.46
Std Dev	14.2

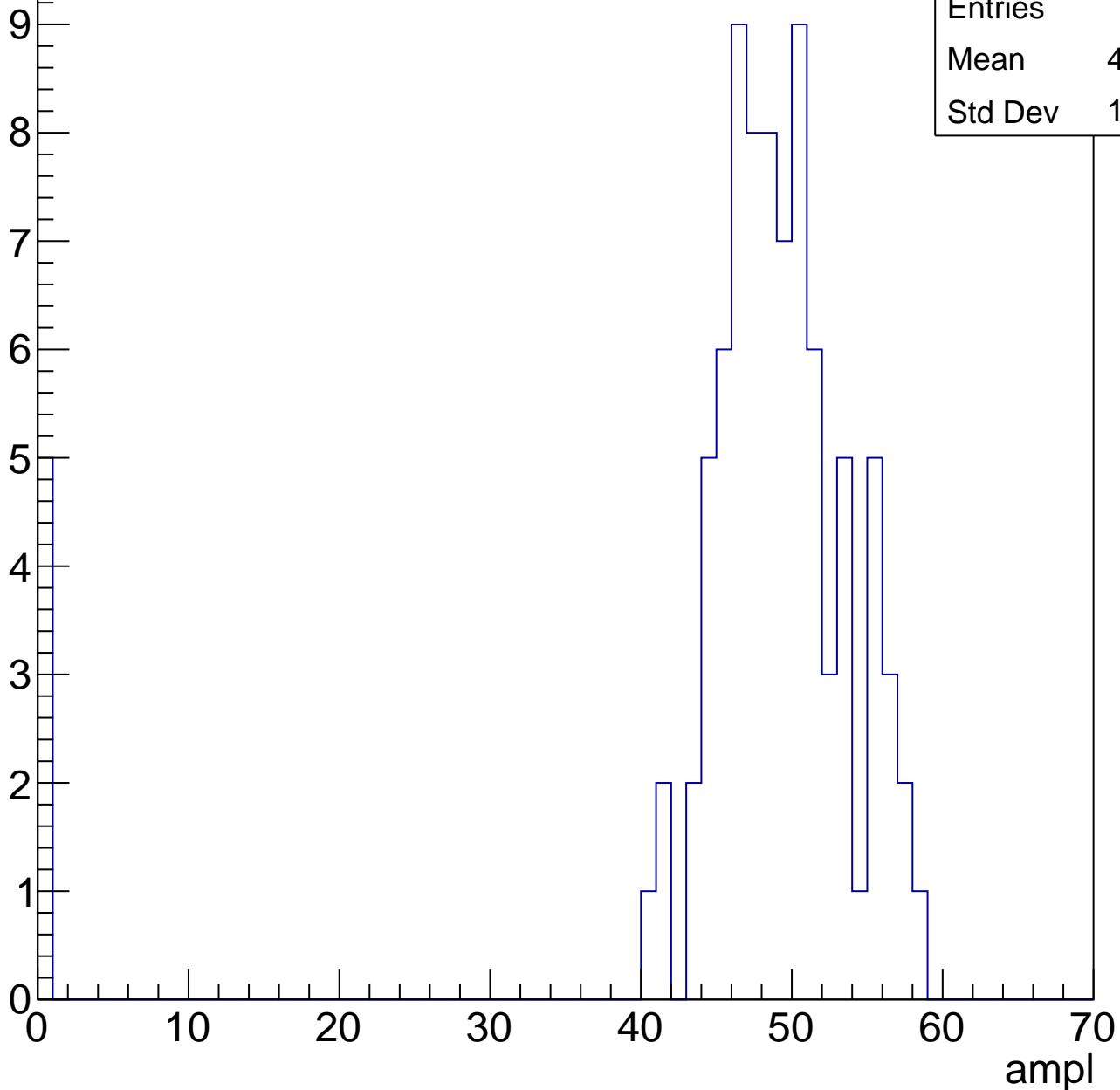


# B1L103S, U25-ch50, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	88
Mean	46.15
Std Dev	11.97

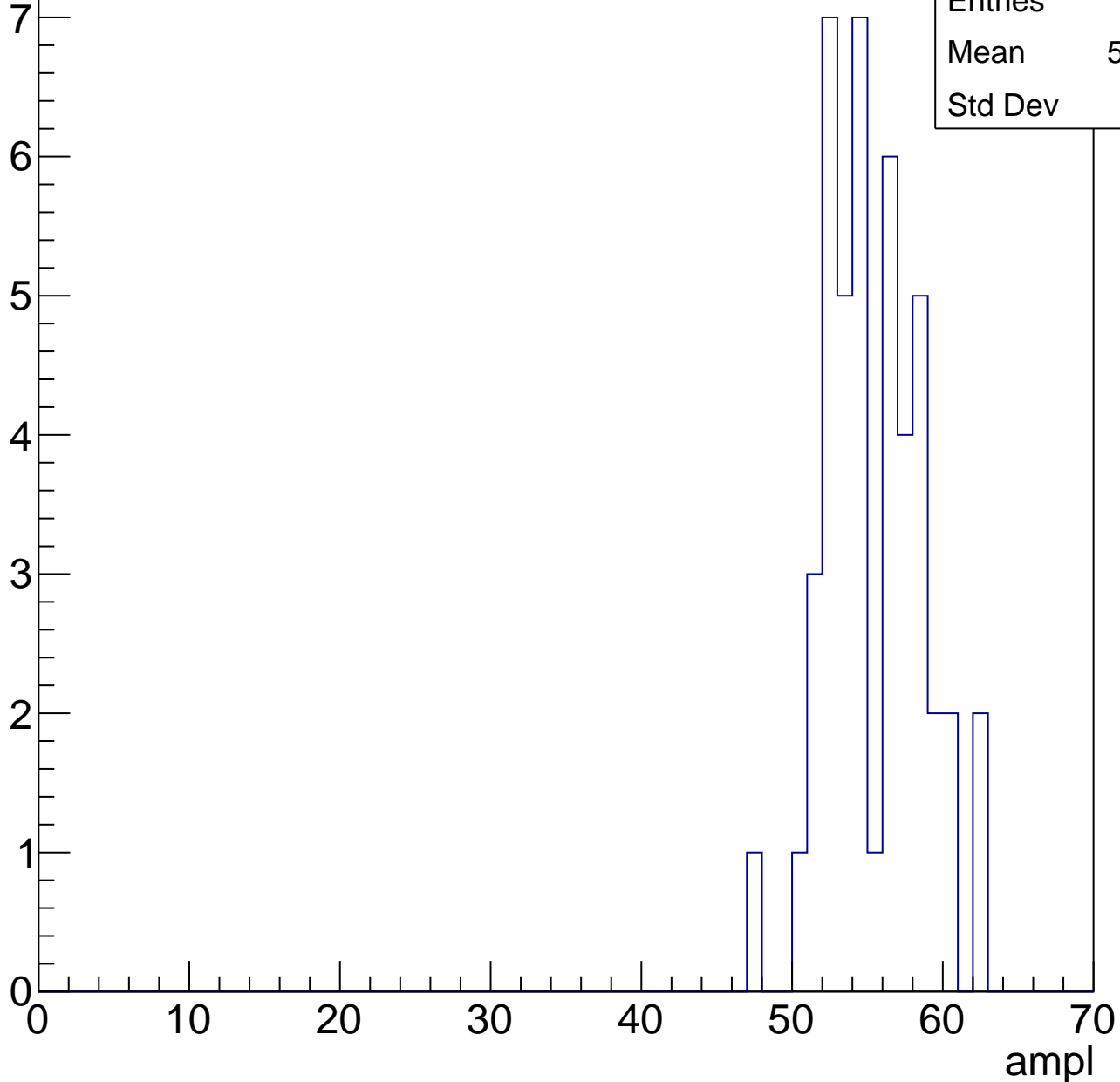


# B1L103S, U25-ch50, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

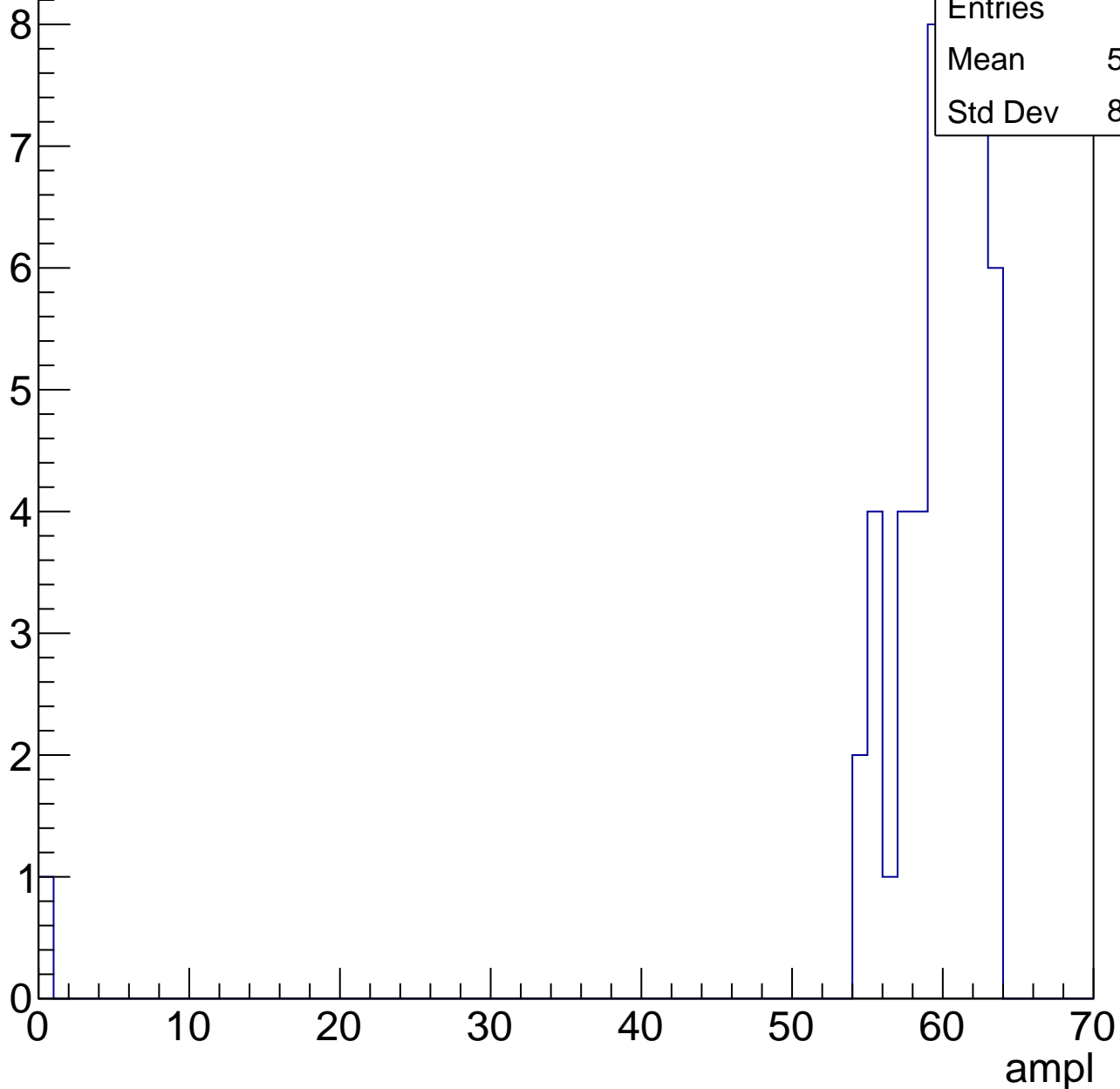
Entries	46
Mean	54.96
Std Dev	3.21



# B1L103S, U25-ch50, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

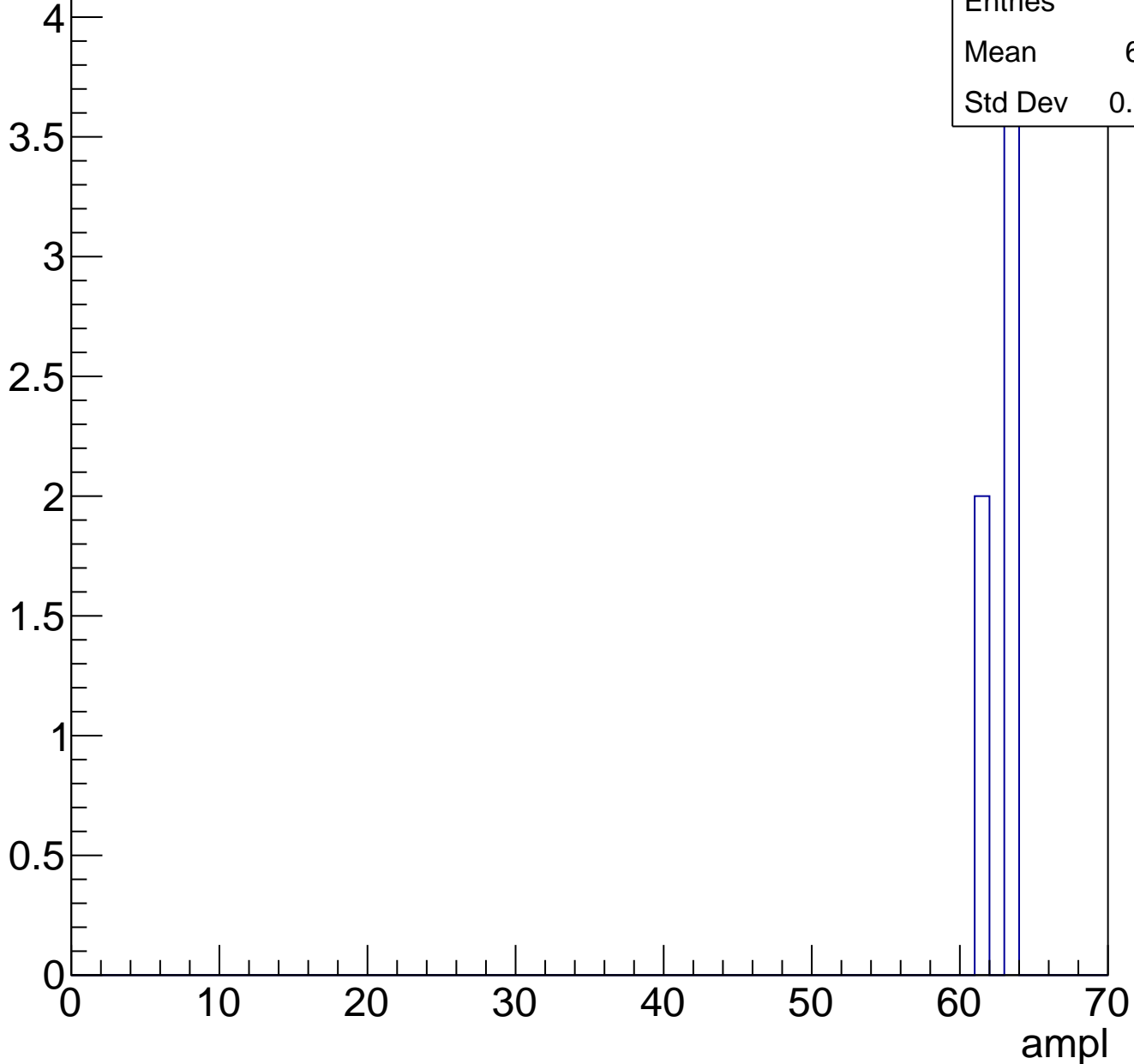
Entry



# B1L103S, U25-ch50, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U25-ch50, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

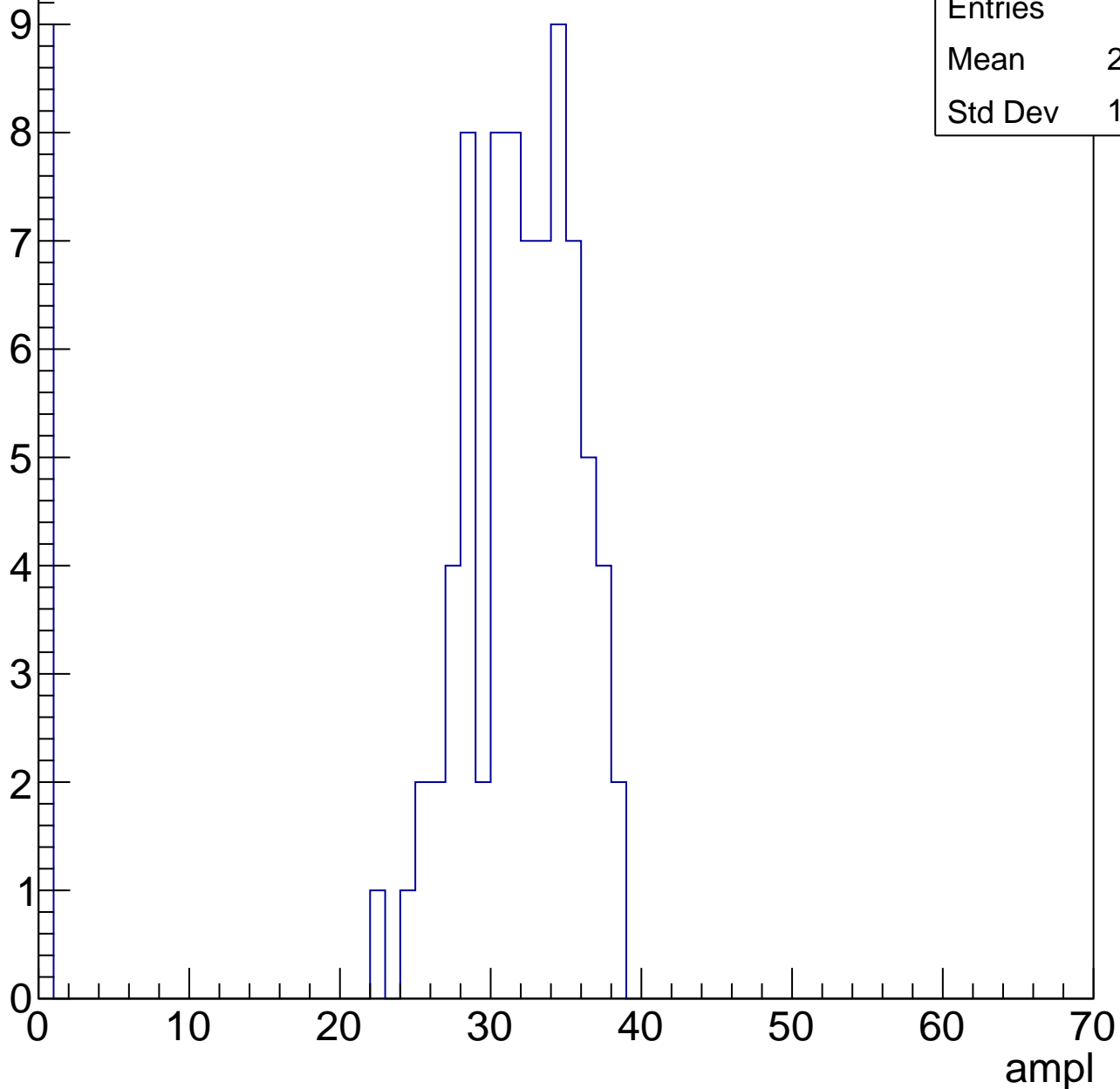
Entries	19
Mean	0
Std Dev	0

ampl

# B1L103S, U25-ch51, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

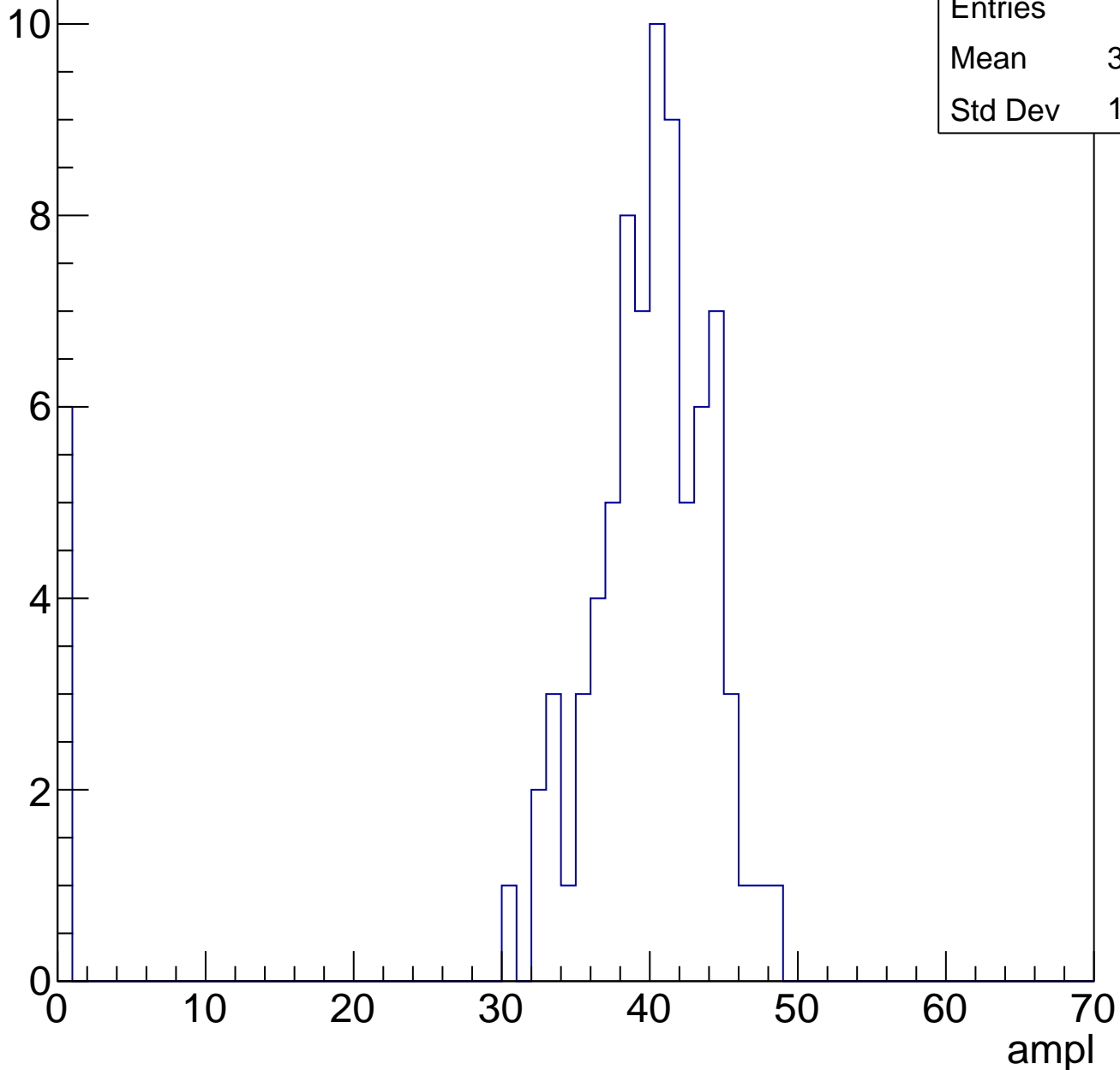


# B1L103S, U25-ch51, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	83
Mean	36.86
Std Dev	10.88

Entry

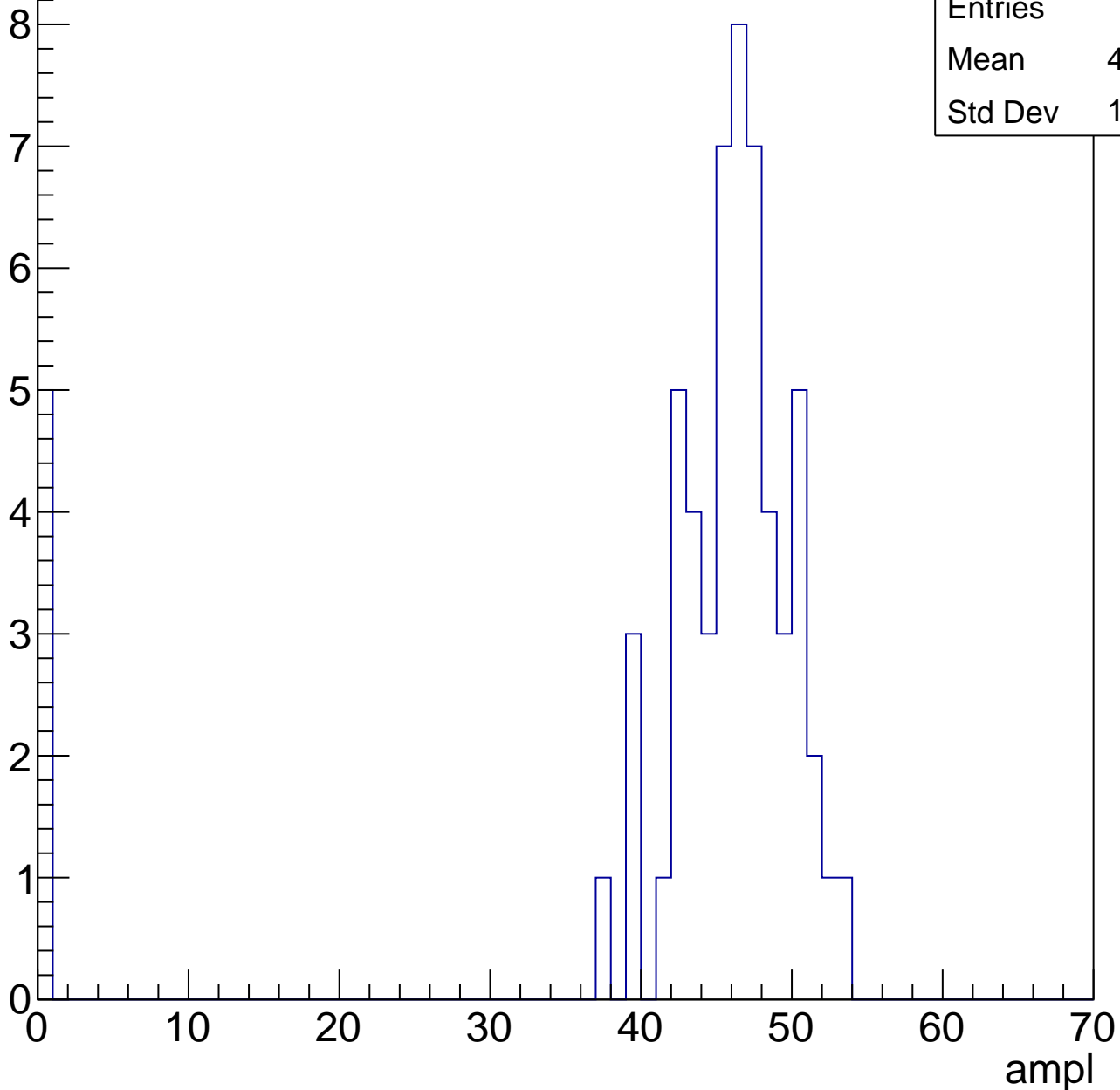


# B1L103S, U25-ch51, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	60
Mean	41.95
Std Dev	13.07

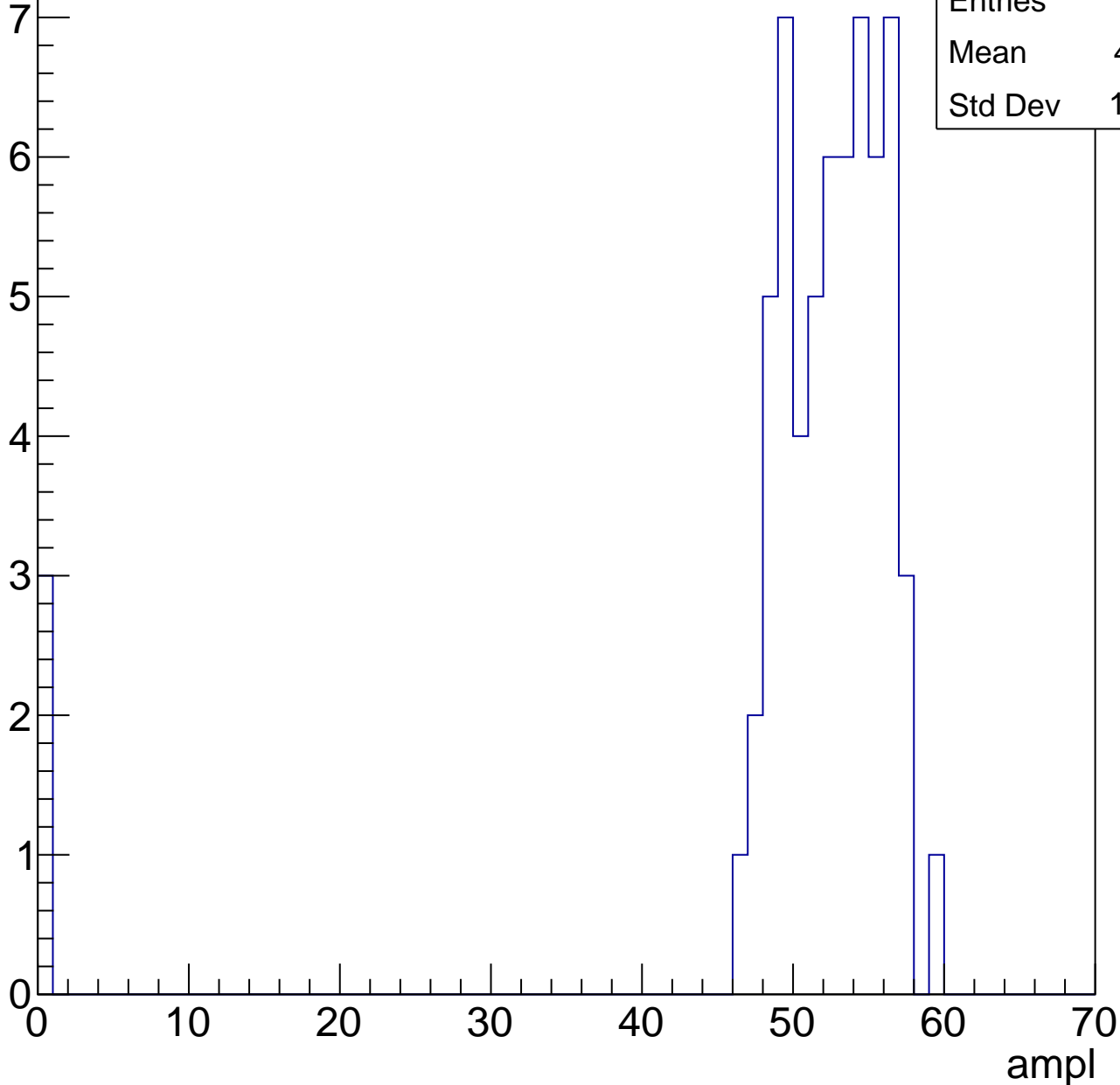


# B1L103S, U25-ch51, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	63
Mean	49.81
Std Dev	11.54

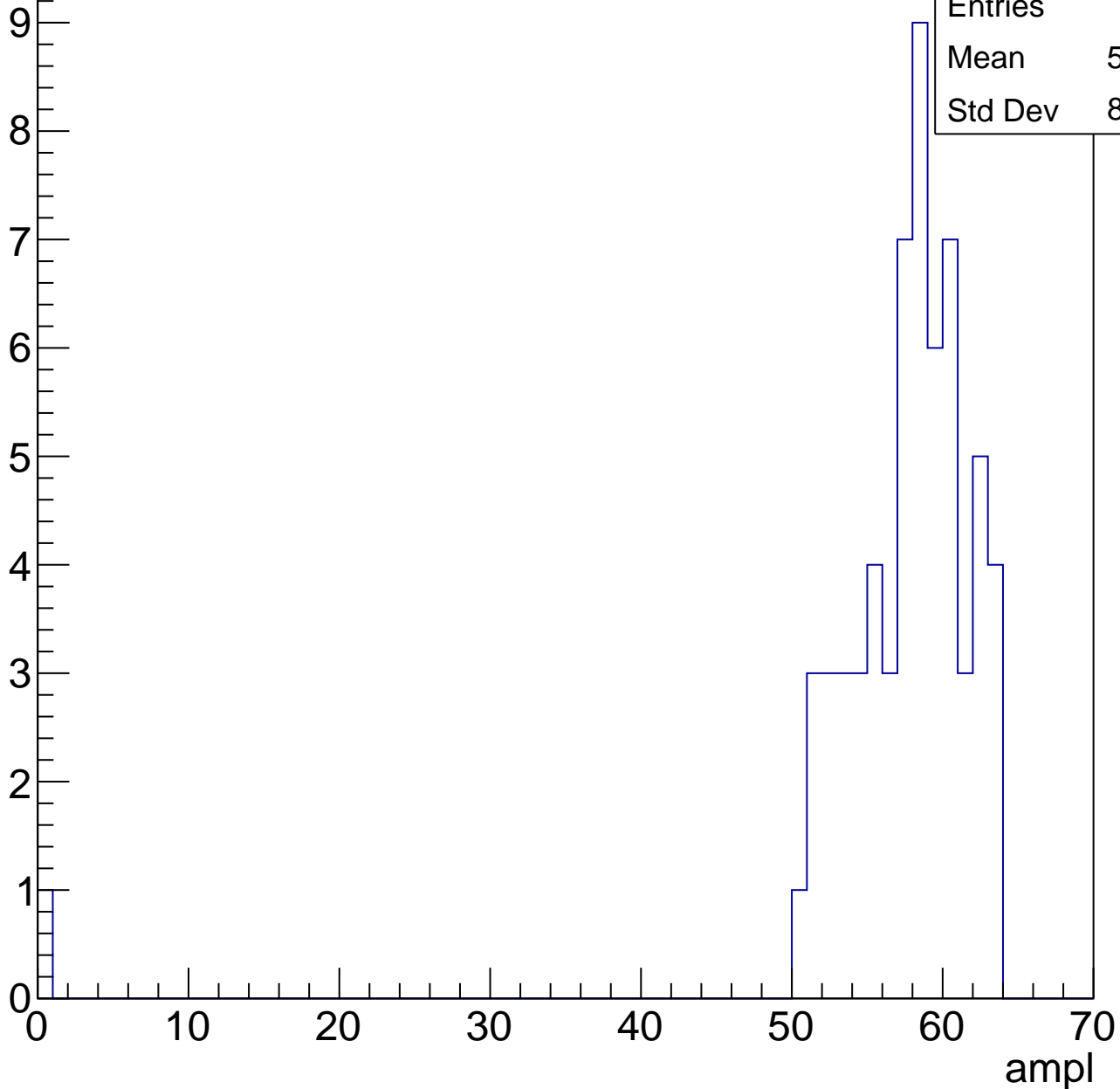


# B1L103S, U25-ch51, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

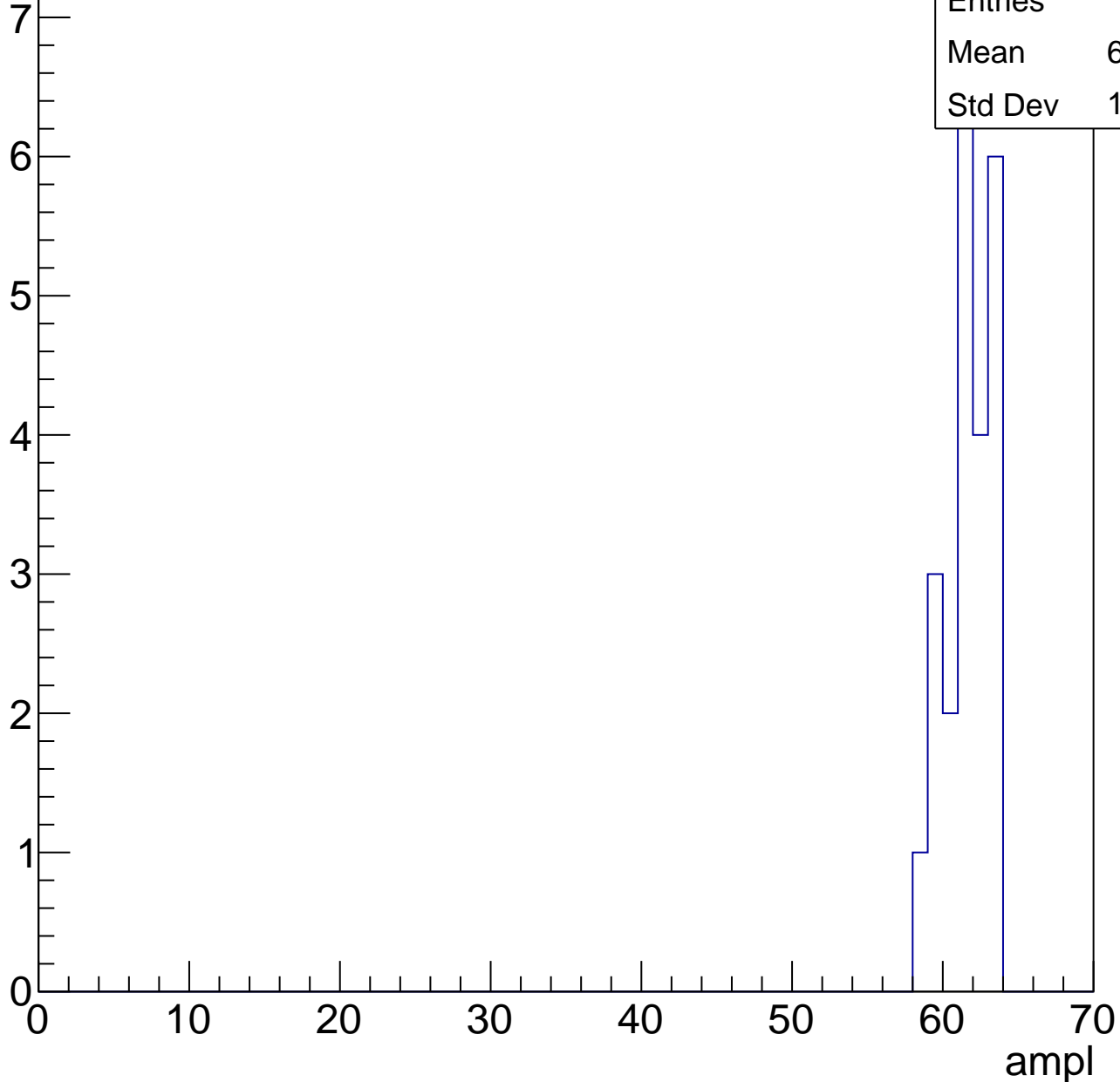
Entries	62
Mean	56.58
Std Dev	8.009



# B1L103S, U25-ch51, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

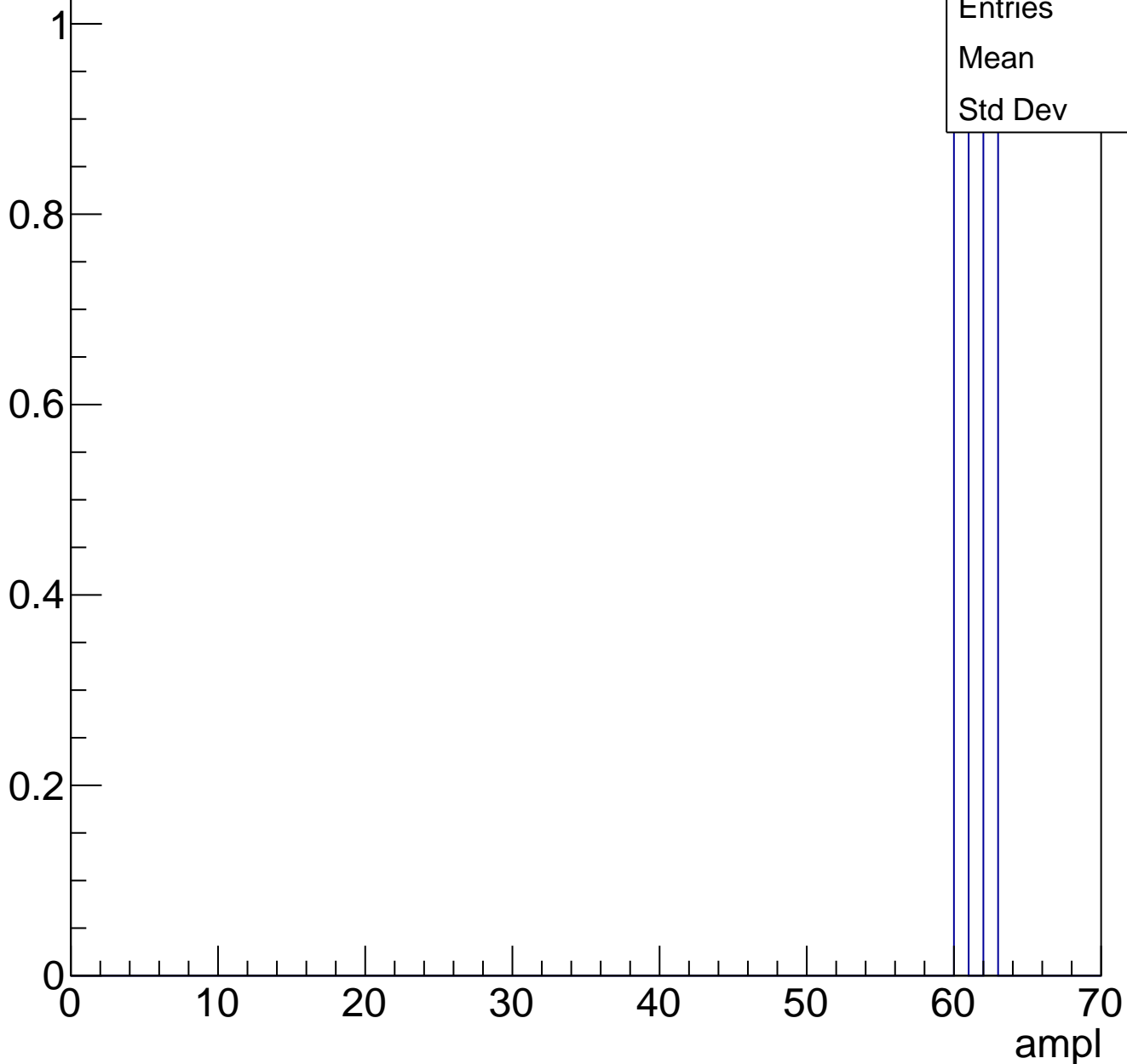
Entry



# B1L103S, U25-ch51, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U25-ch51, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

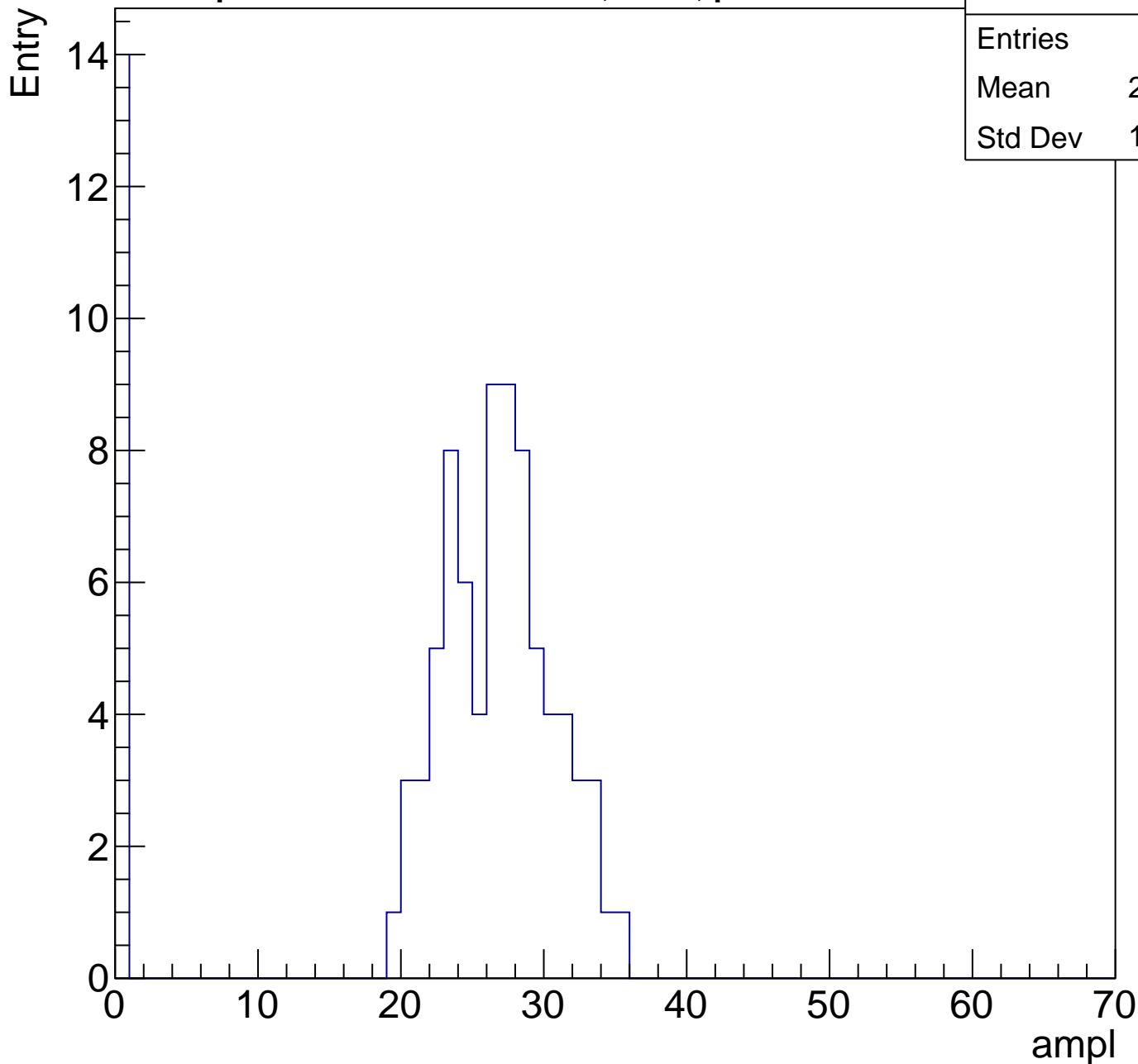
Entries	19
Mean	0
Std Dev	0

ampl

# B1L103S, U25-ch52, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	91
Mean	22.35
Std Dev	10.12

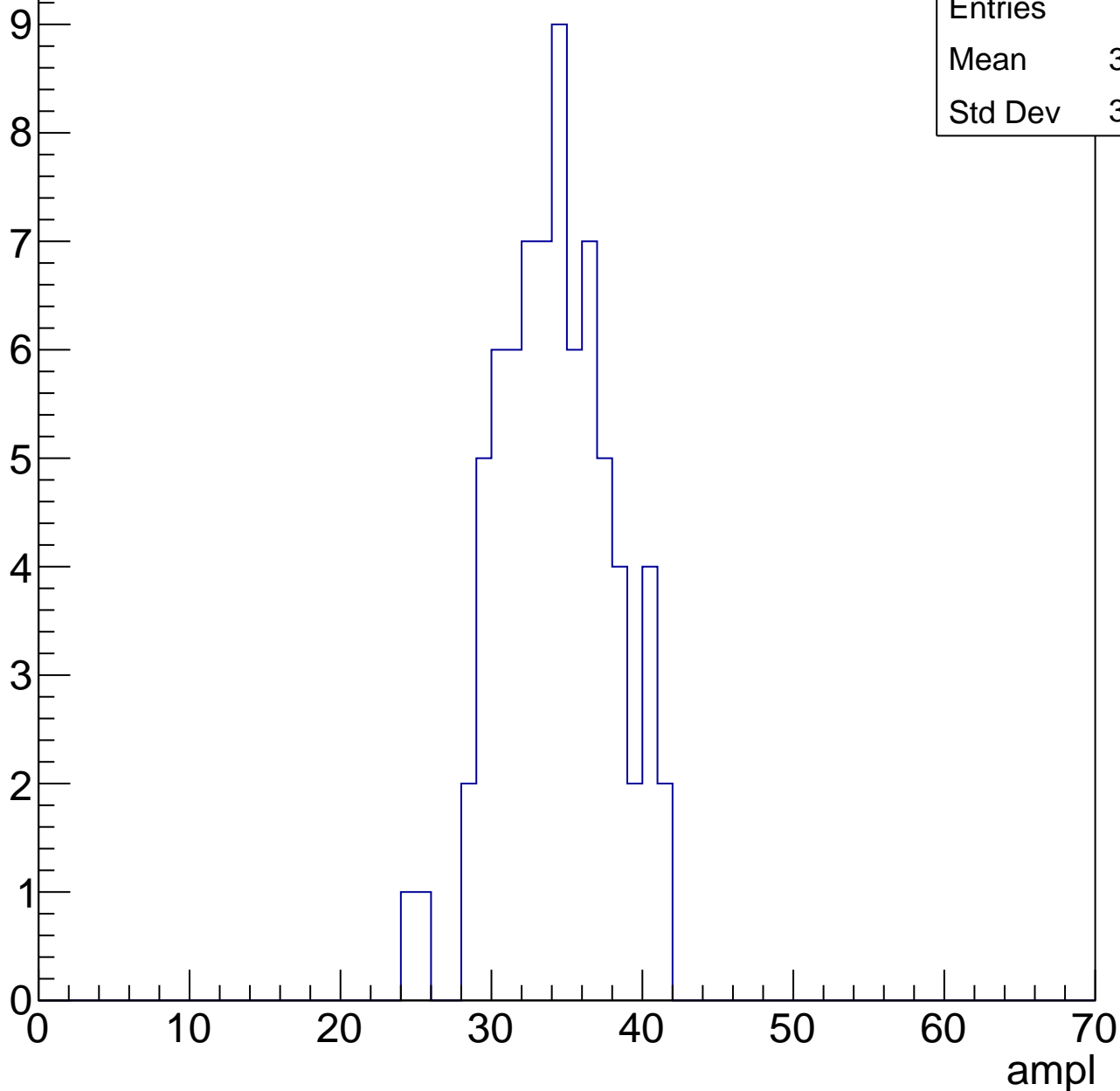


# B1L103S, U25-ch52, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	74
Mean	33.73
Std Dev	3.662

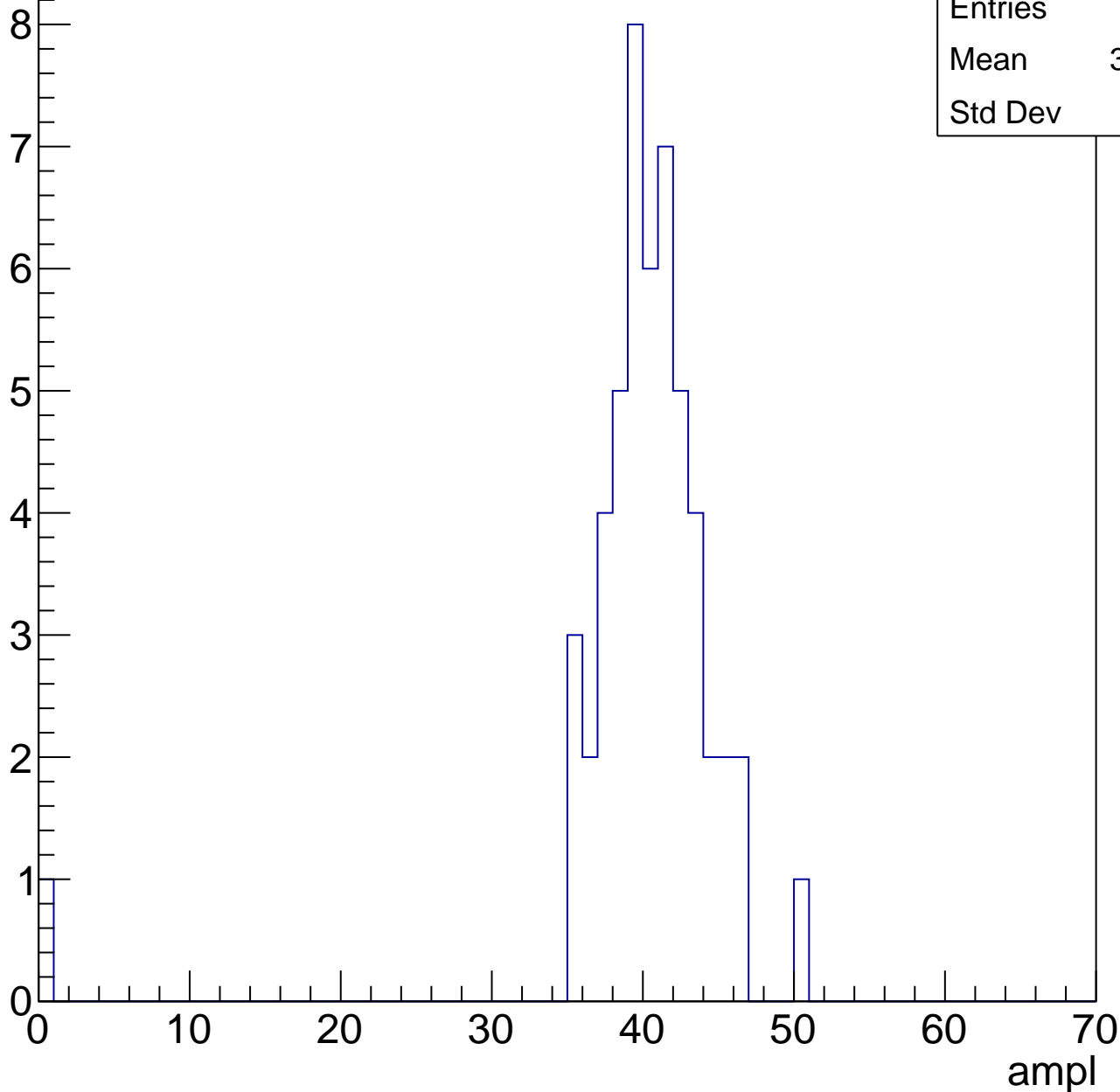


# B1L103S, U25-ch52, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	52
Mean	39.54
Std Dev	6.32



# B1L103S, U25-ch52, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	80
Mean	39.74
Std Dev	16.21

Entry

10

8

6

4

2

0

0

10

20

30

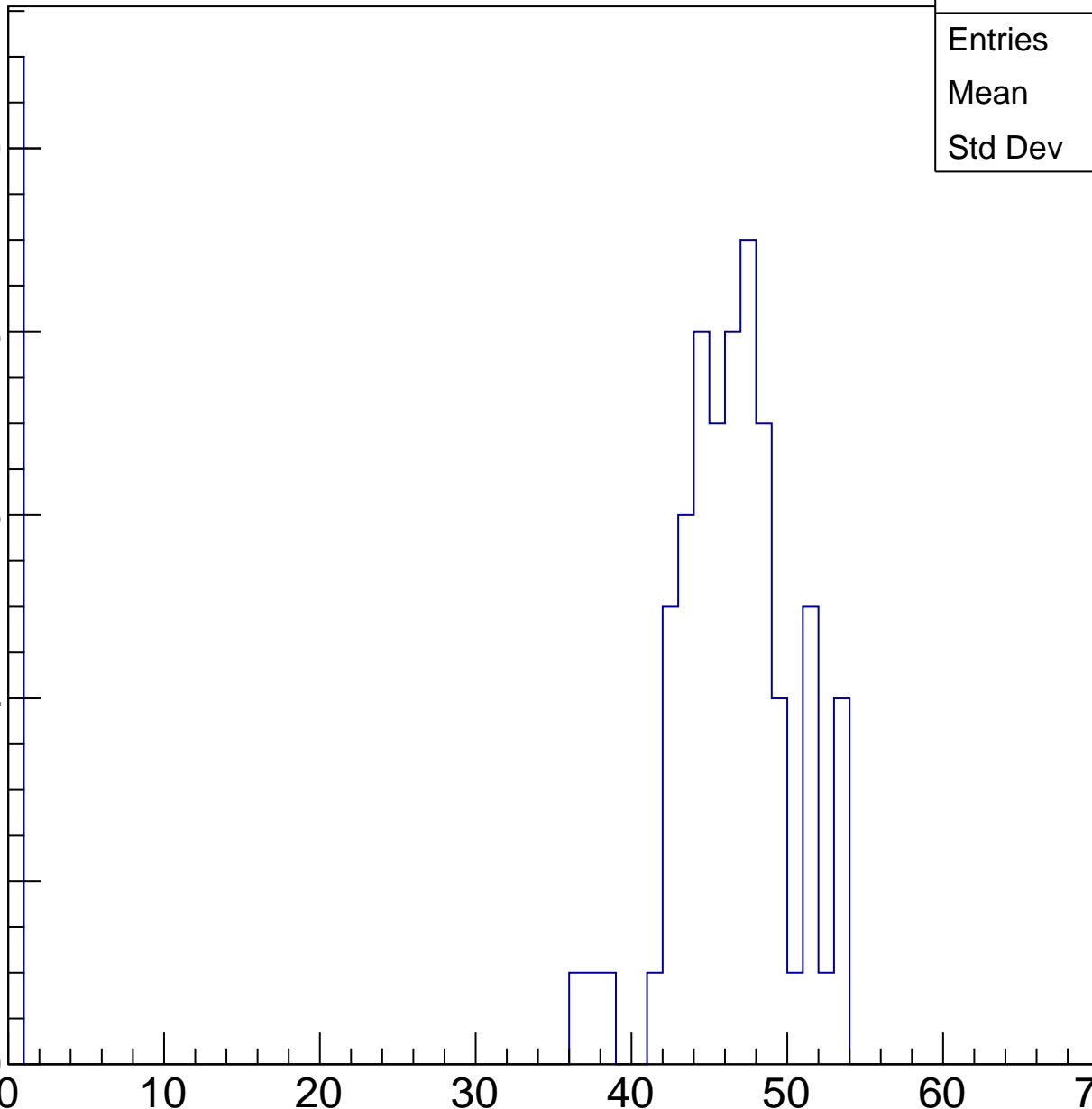
40

50

60

70

ampl

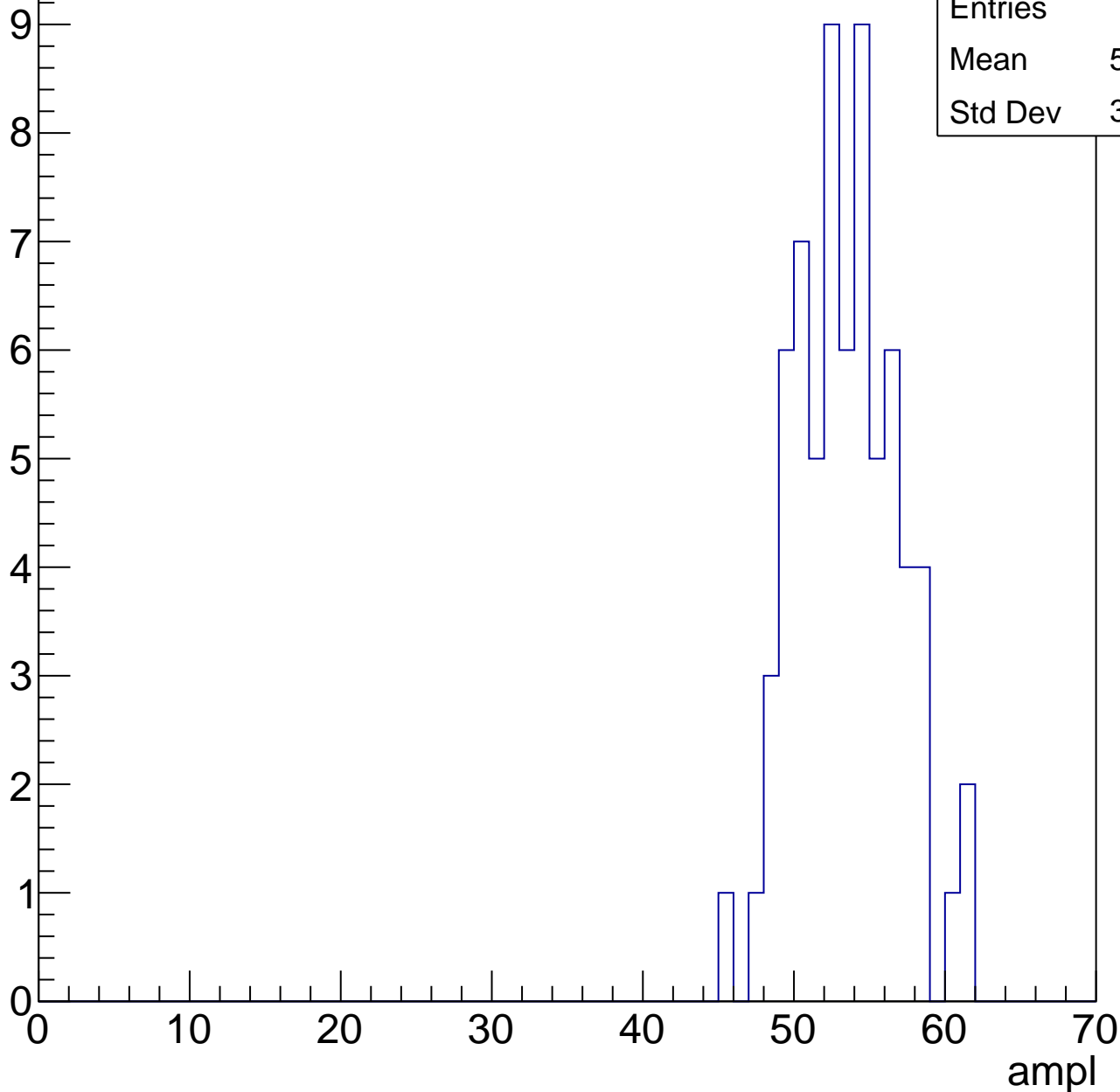


# B1L103S, U25-ch52, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	69
Mean	53.04
Std Dev	3.377

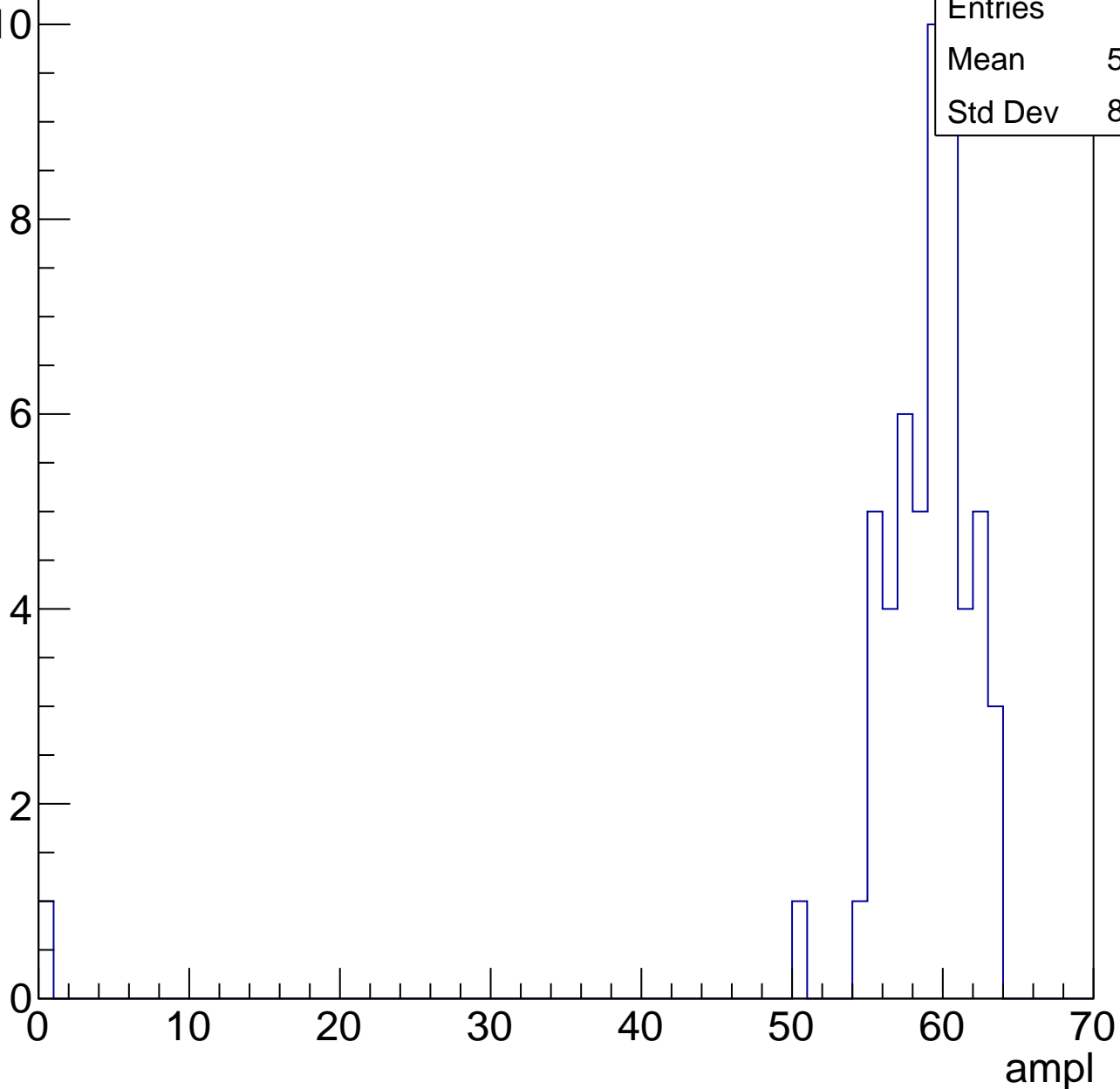


# B1L103S, U25-ch52, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	54
Mean	57.56
Std Dev	8.319

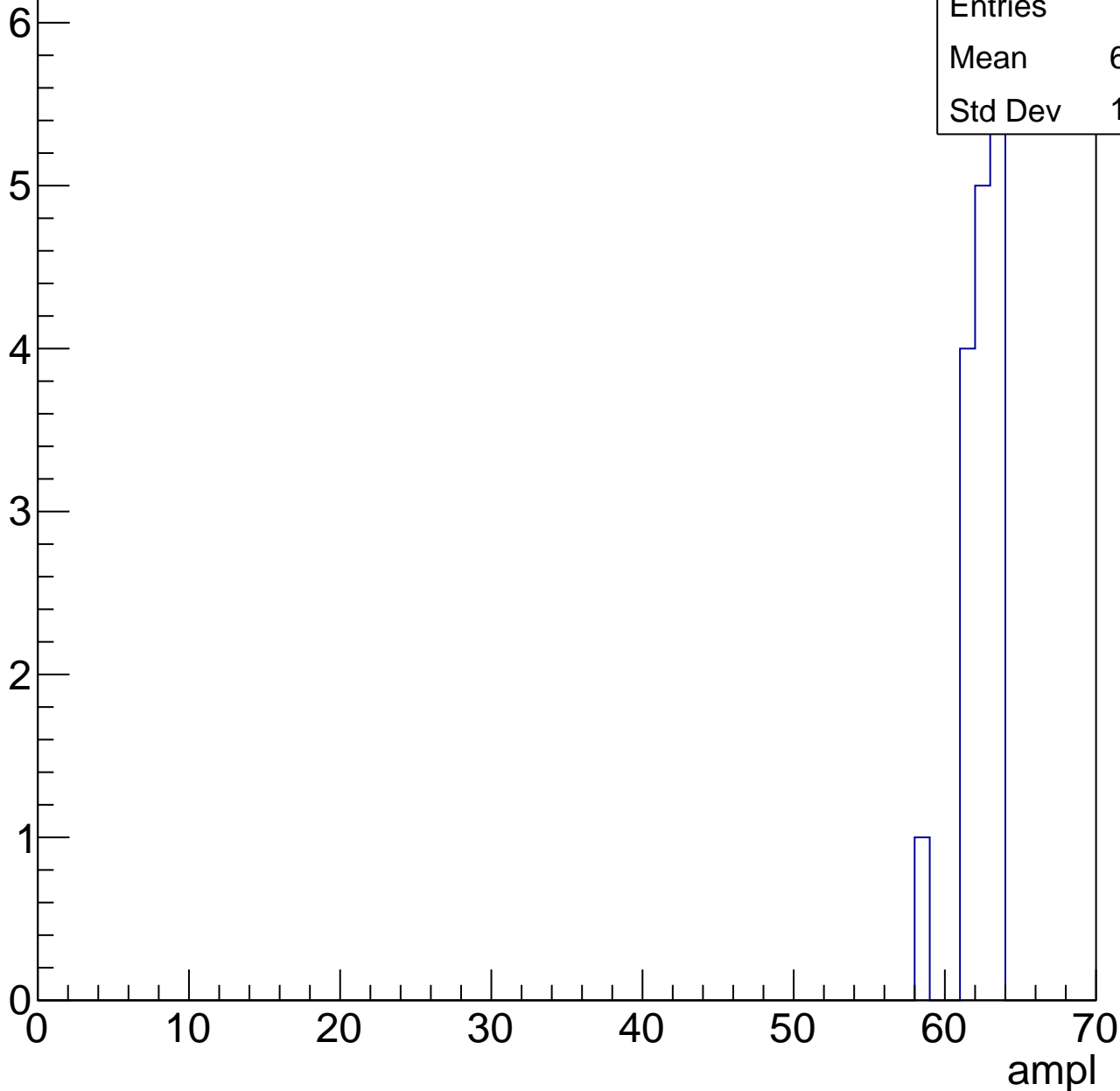


# B1L103S, U25-ch52, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	16
Mean	61.88
Std Dev	1.269





# B1L103S, U25-ch52, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	19
Mean	3.316
Std Dev	14.07

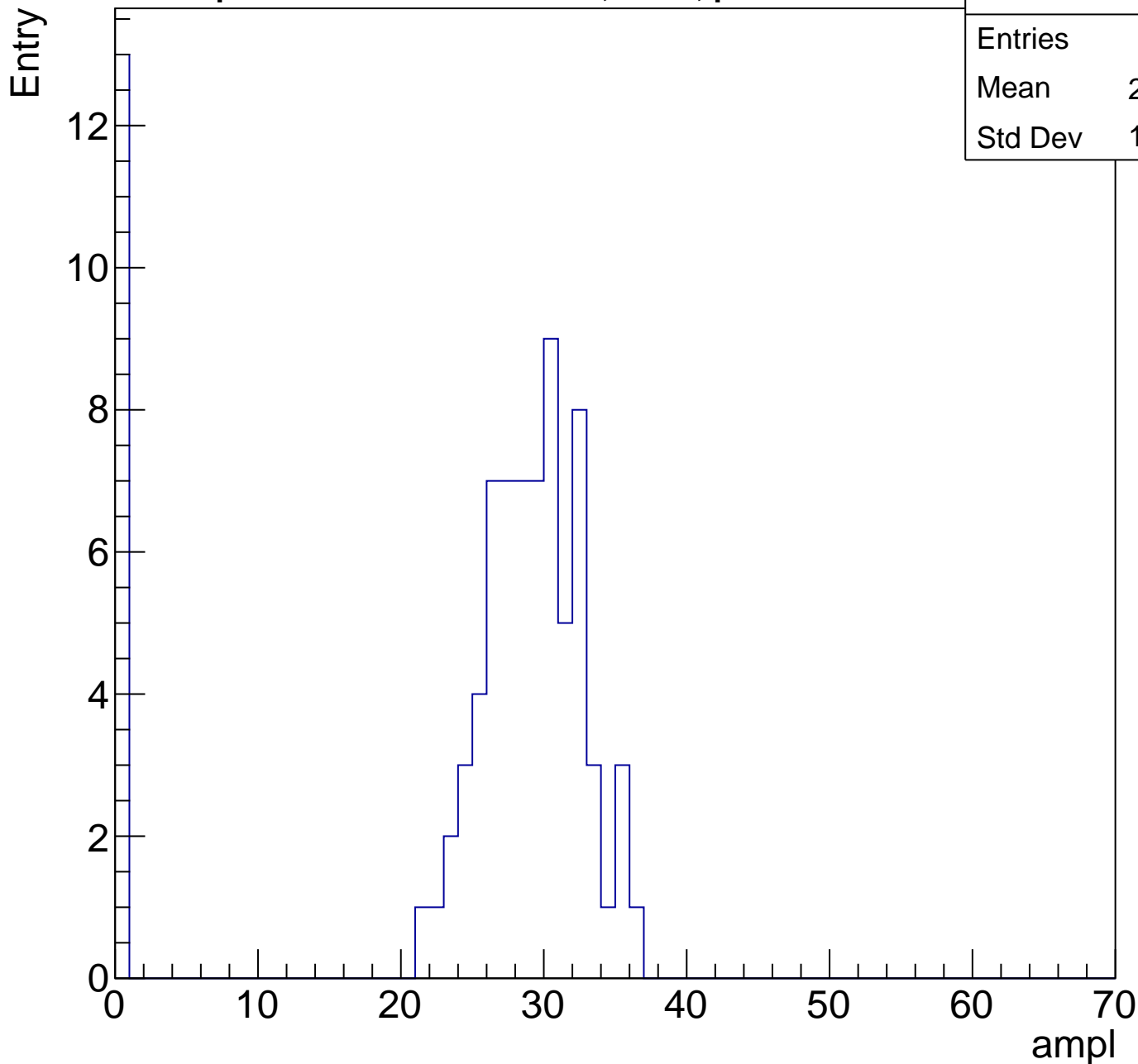
Entry



# B1L103S, U25-ch53, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

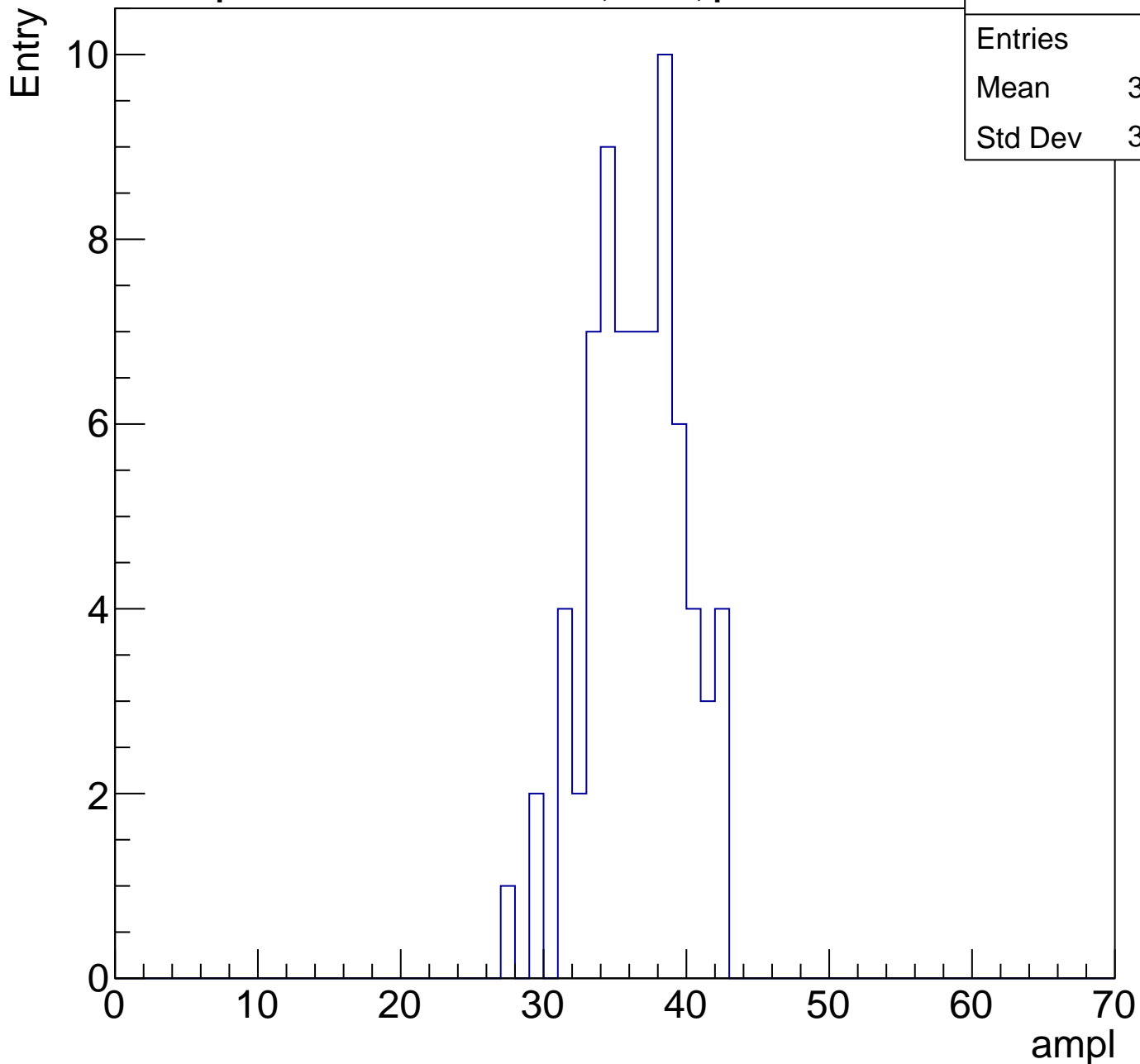
Entries	82
Mean	24.22
Std Dev	10.94



# B1L103S, U25-ch53, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	73
Mean	36.04
Std Dev	3.312

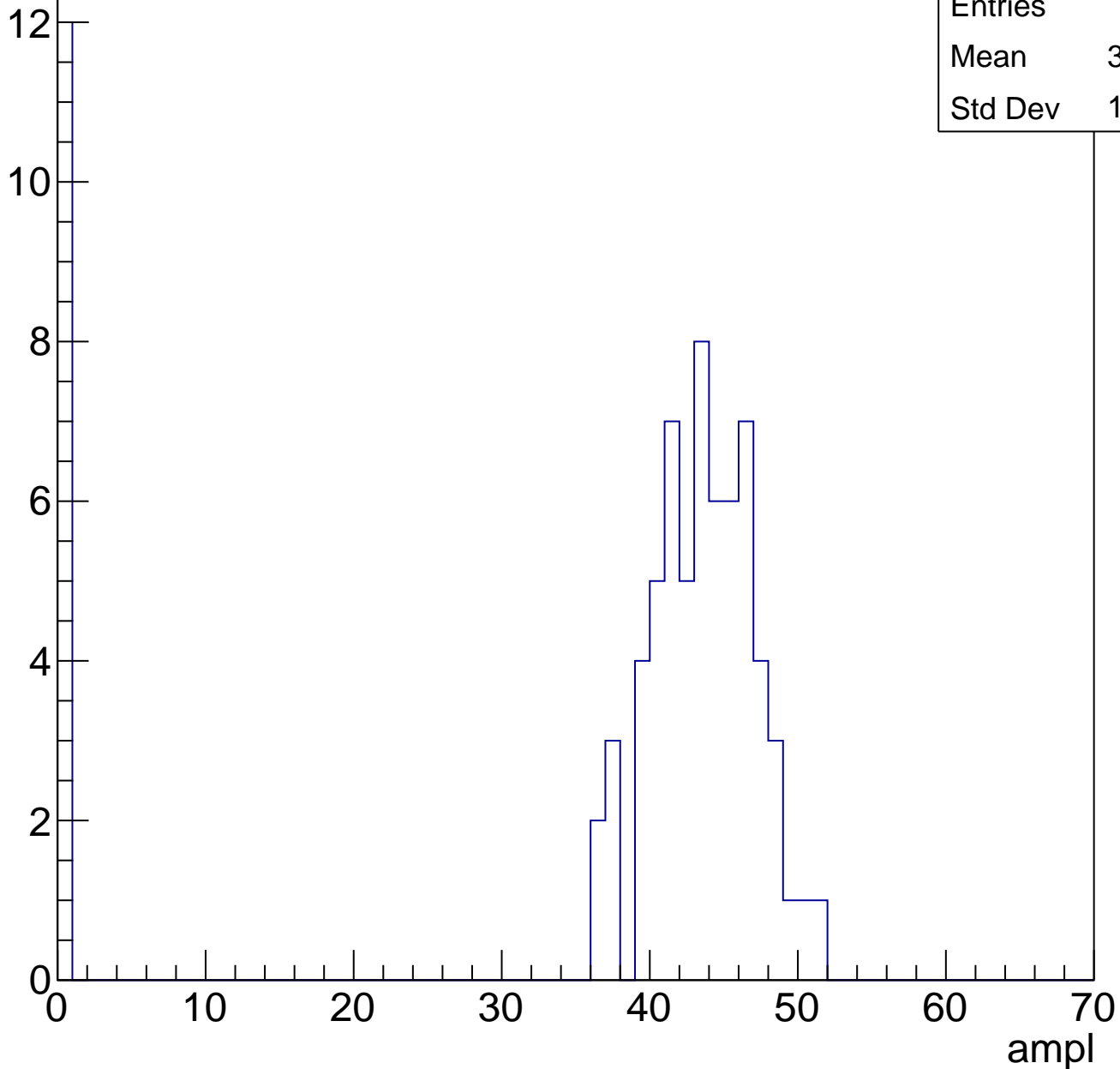


# B1L103S, U25-ch53, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	75
Mean	36.24
Std Dev	16.12

Entry

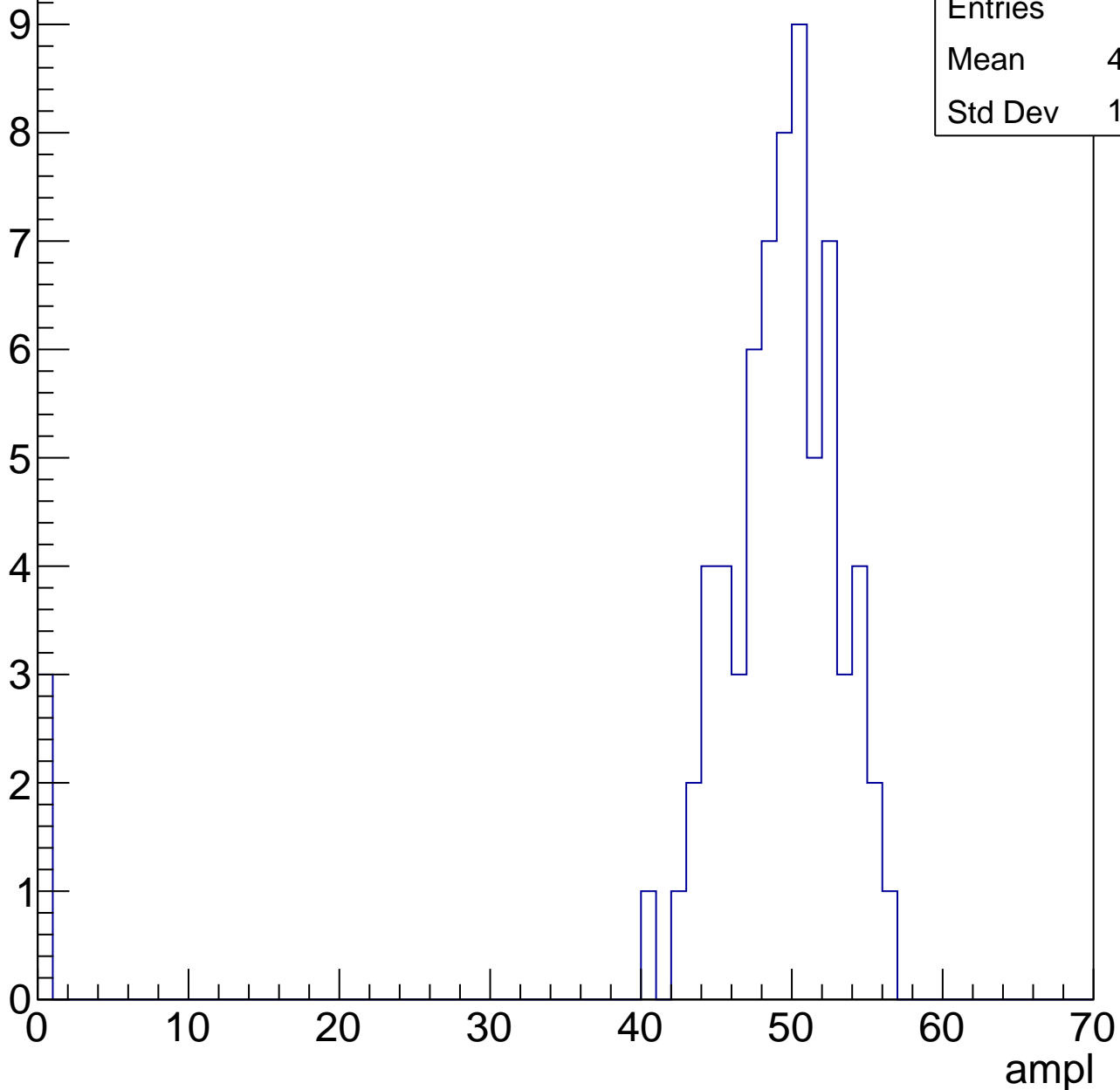


# B1L103S, U25-ch53, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	70
Mean	46.89
Std Dev	10.47

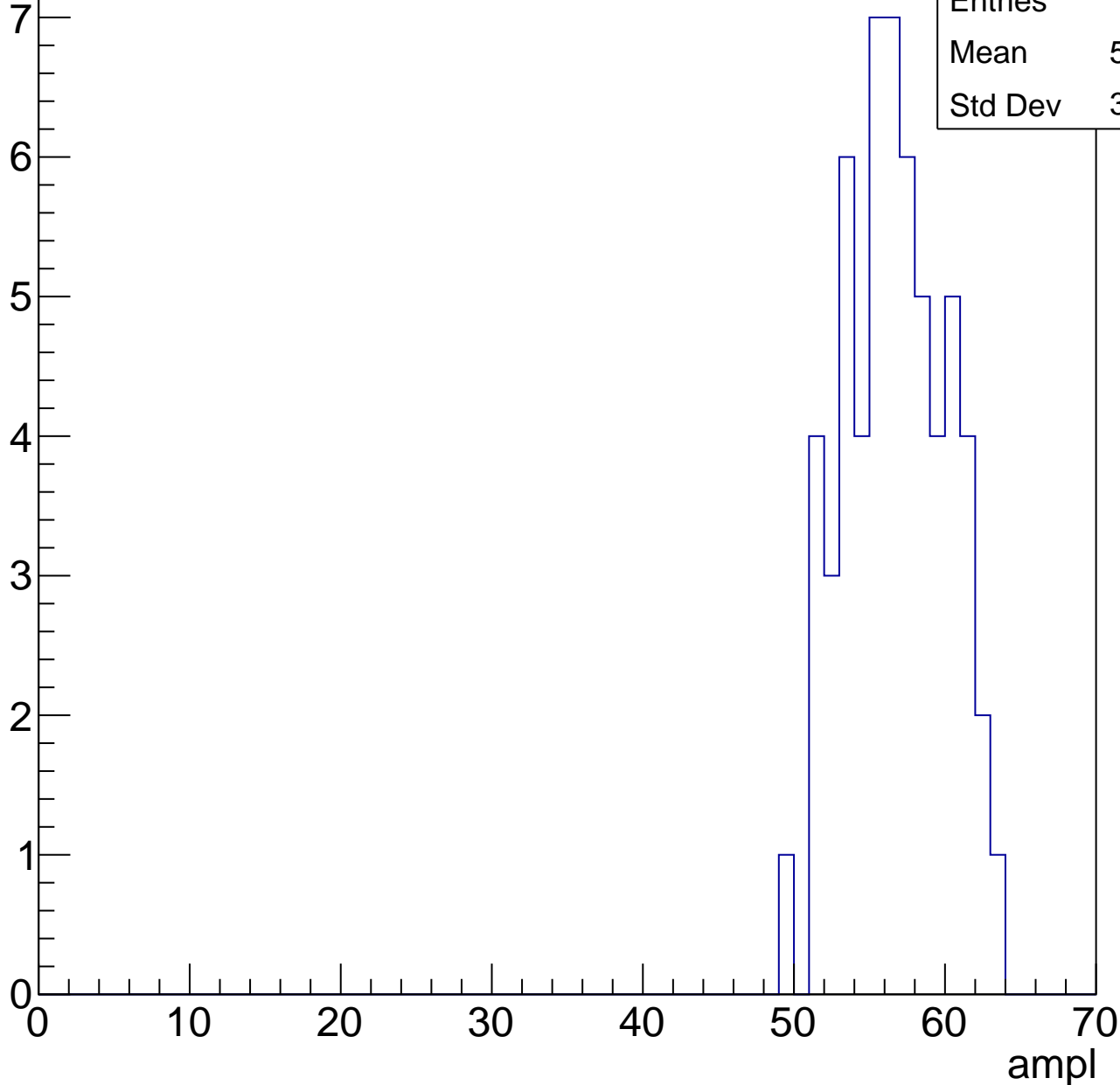


# B1L103S, U25-ch53, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	59
Mean	56.25
Std Dev	3.276

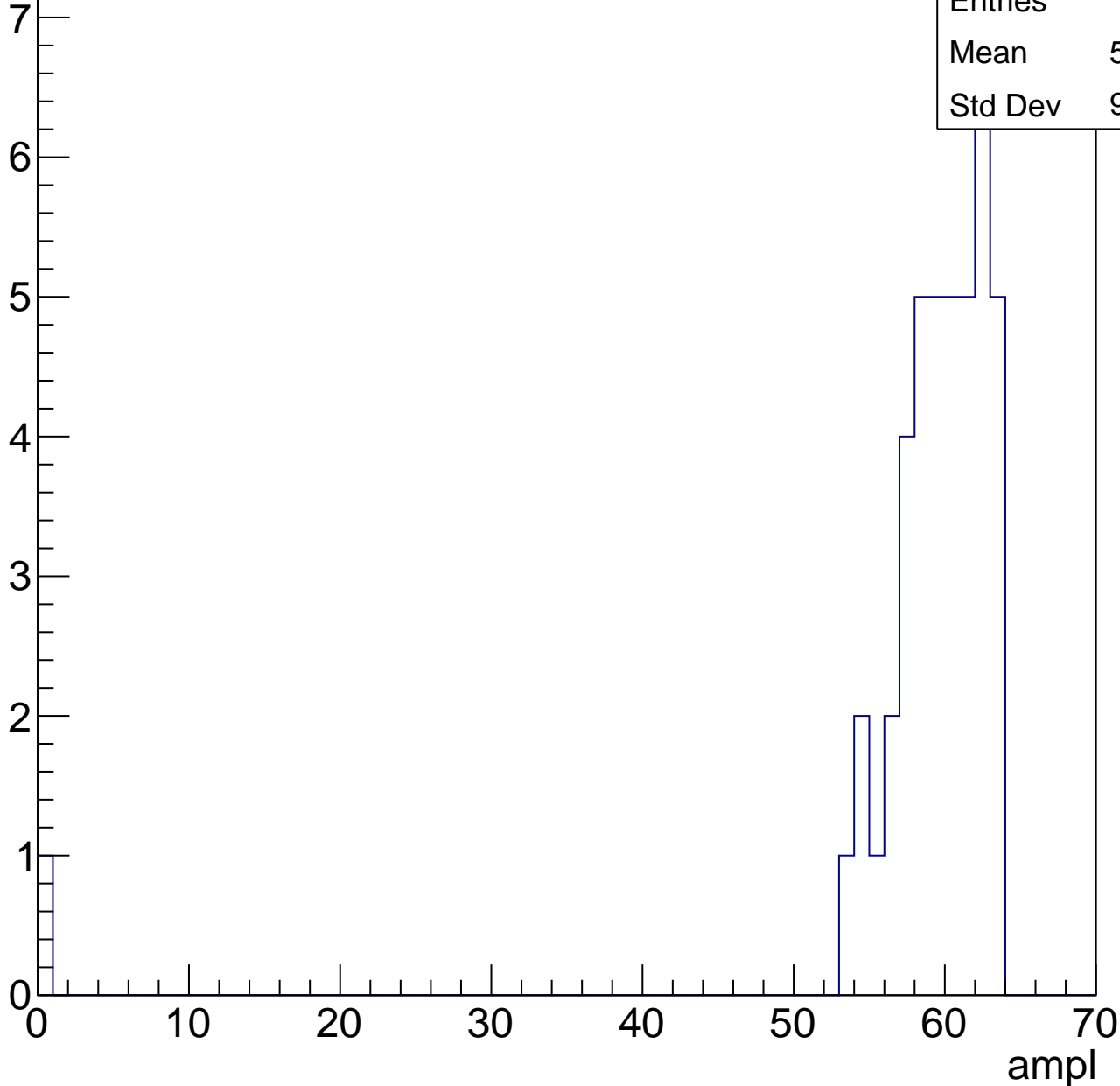


# B1L103S, U25-ch53, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

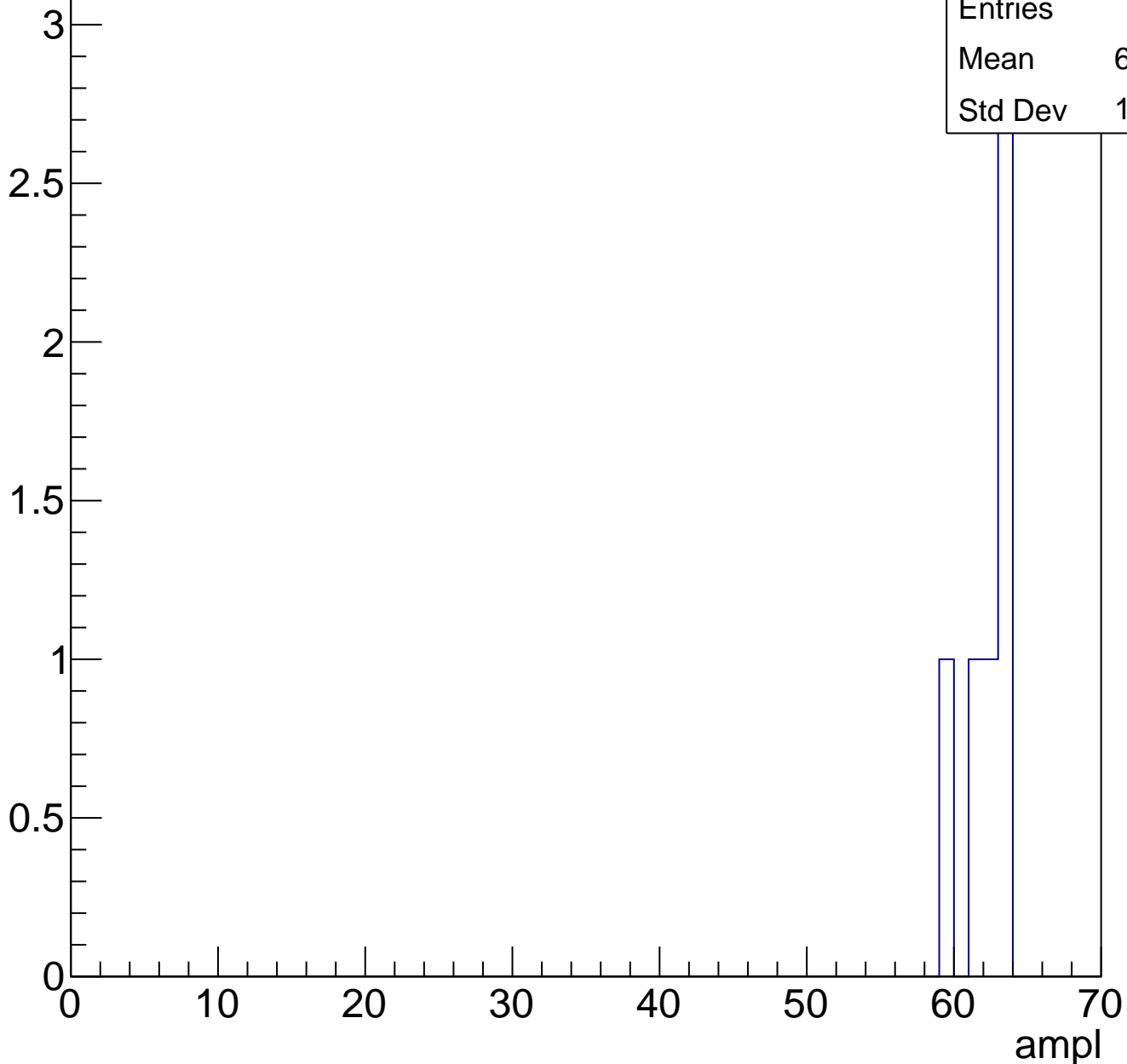
Entries	43
Mean	58.02
Std Dev	9.337



# B1L103S, U25-ch53, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



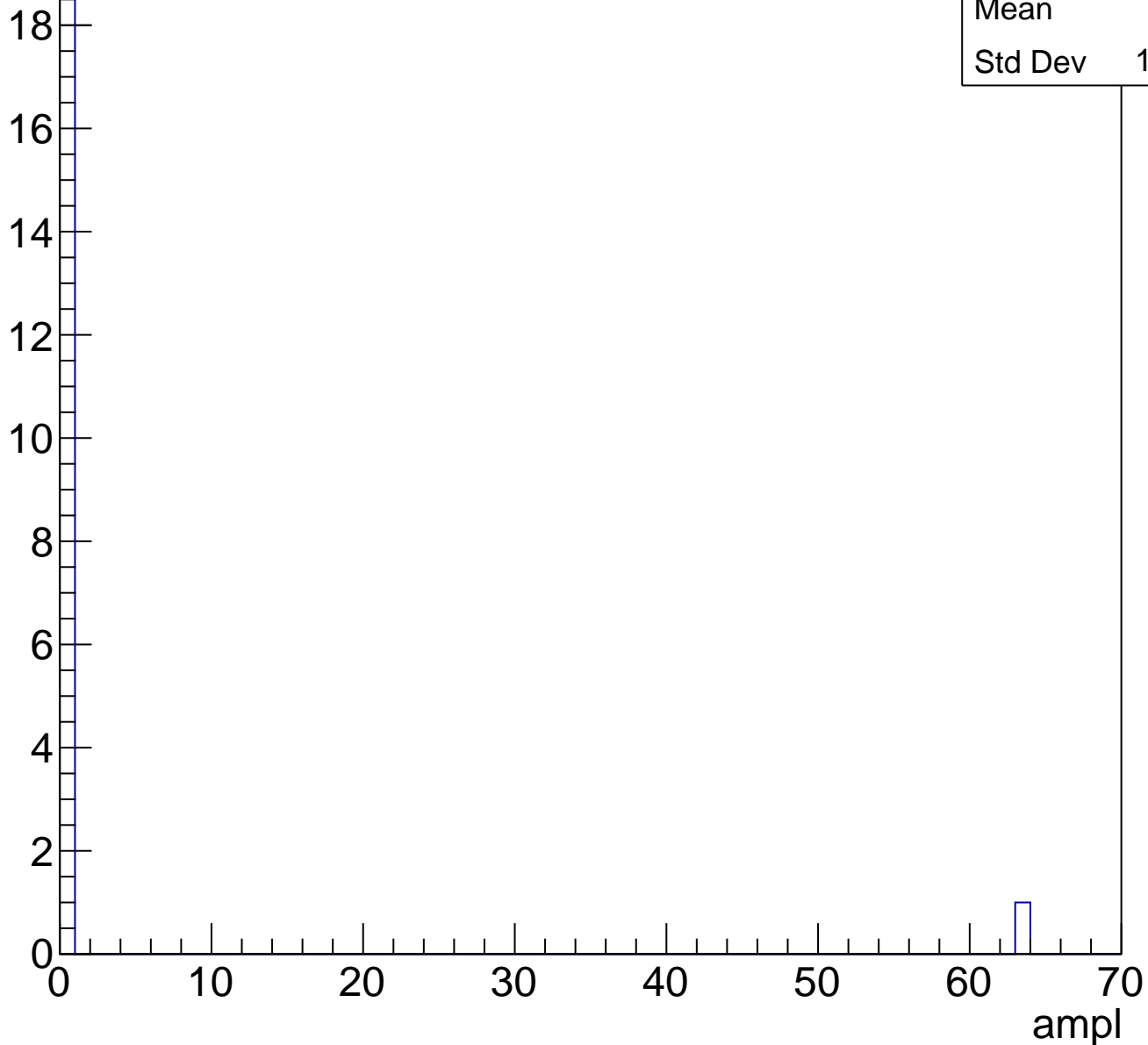


# B1L103S, U25-ch53, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	20
Mean	3.15
Std Dev	13.73

Entry



# B1L103S, U25-ch54, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

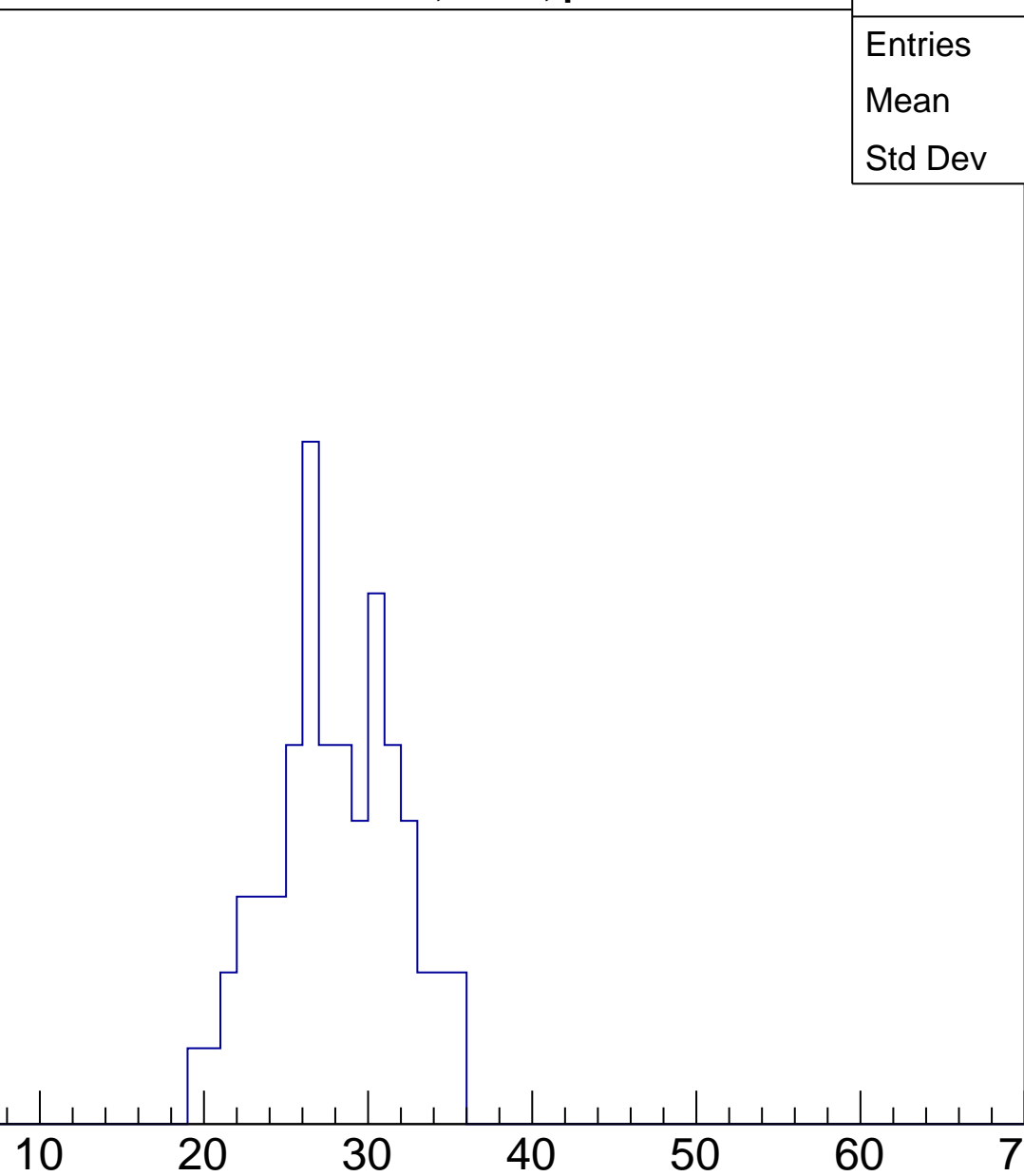
Entries	77
Mean	22.53
Std Dev	11.16

Entry

14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L103S, U25-ch54, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	81
Mean	29.91
Std Dev	12.45

Entry

10

8

6

4

2

0

0

10

20

30

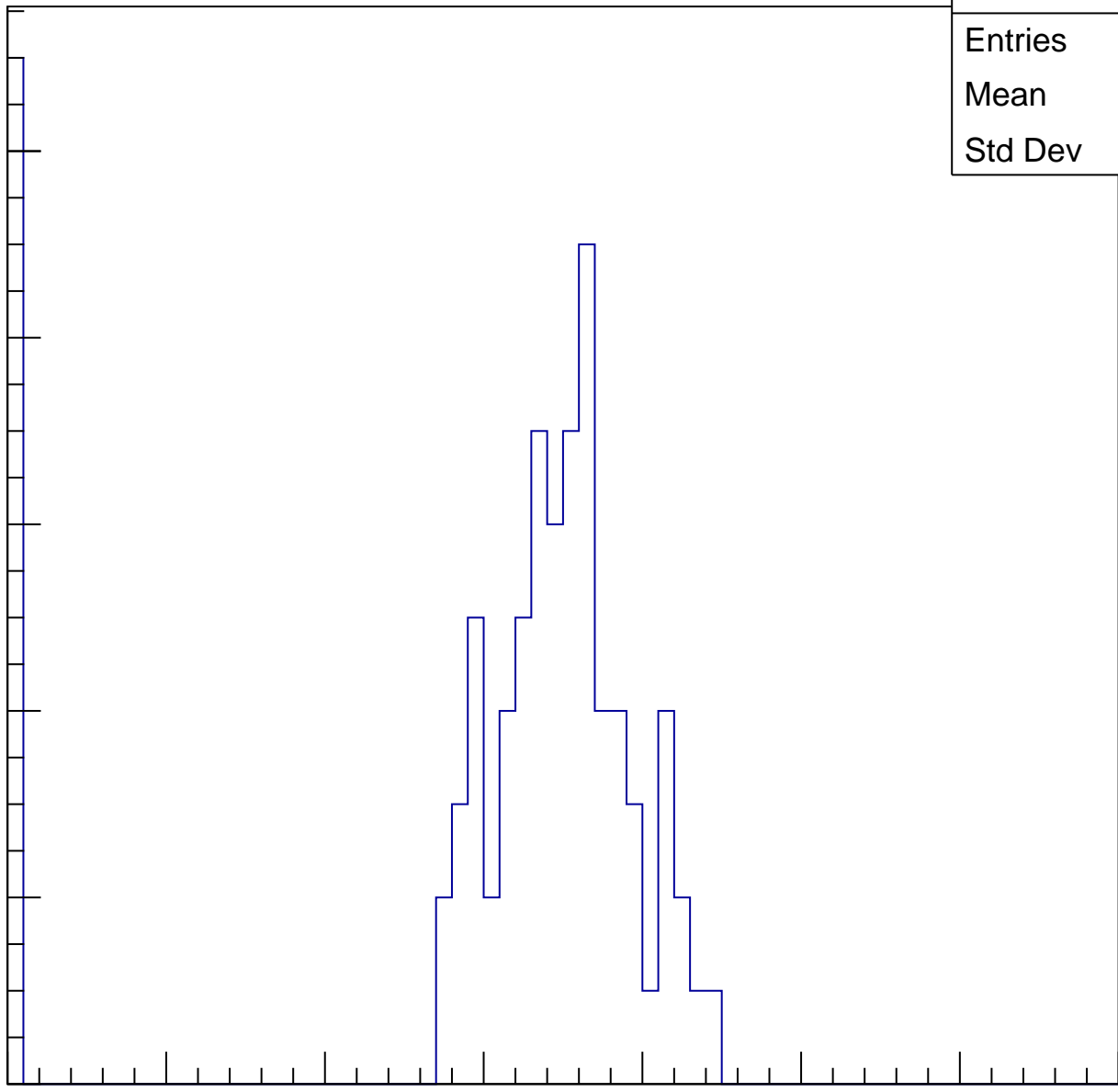
40

50

60

70

ampl

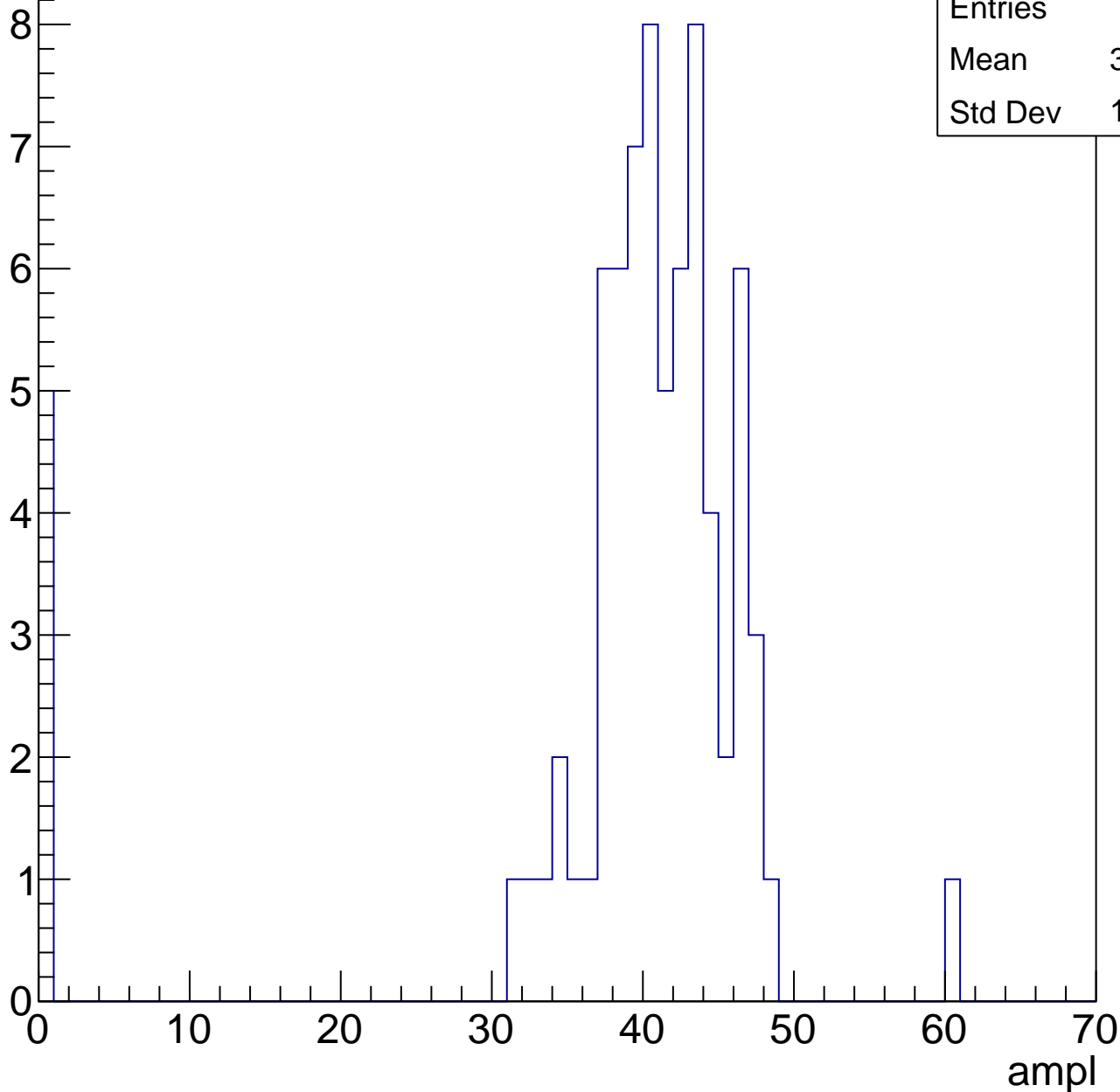


# B1L103S, U25-ch54, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	75
Mean	38.27
Std Dev	11.08

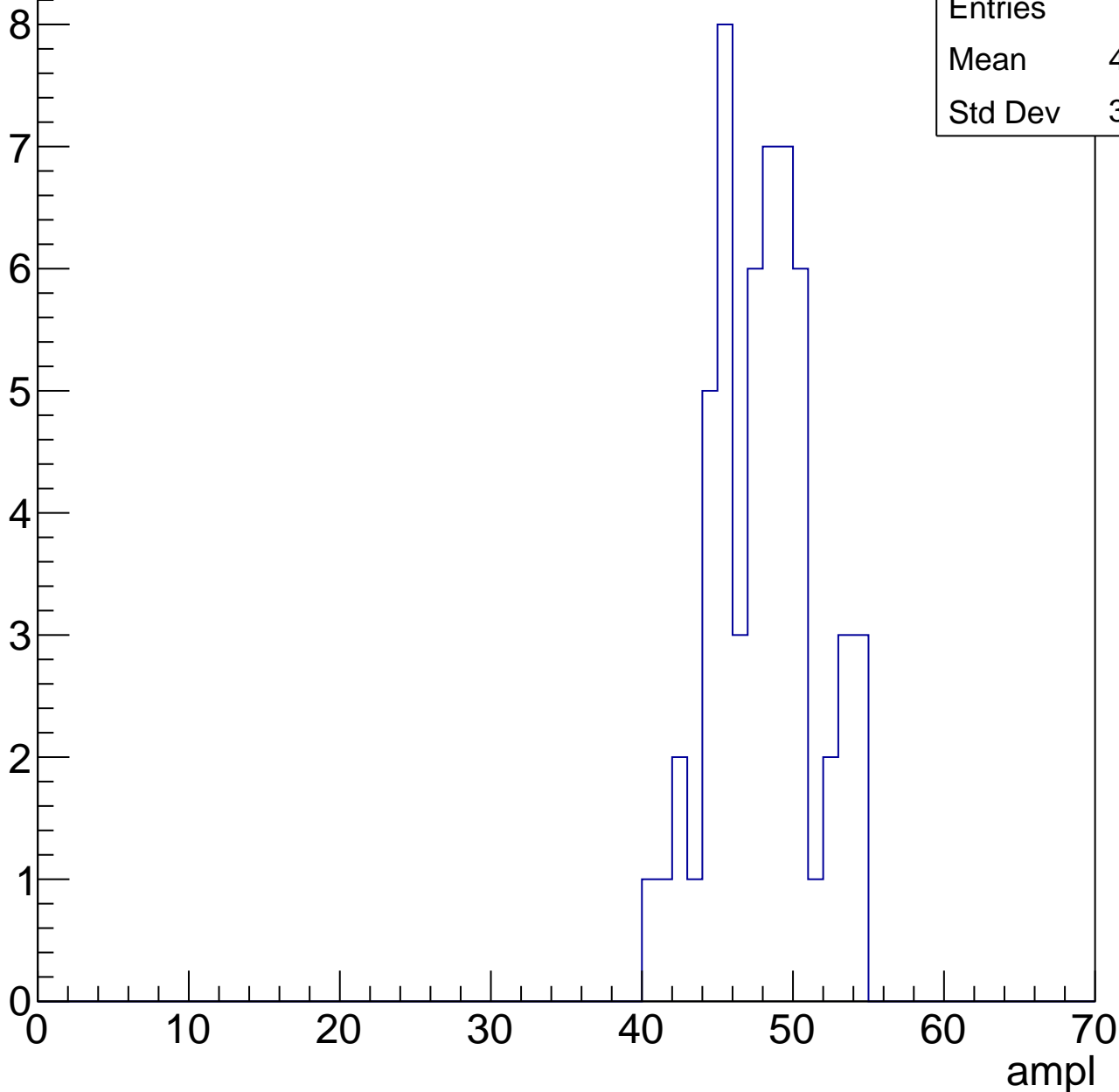


# B1L103S, U25-ch54, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	56
Mean	47.55
Std Dev	3.338

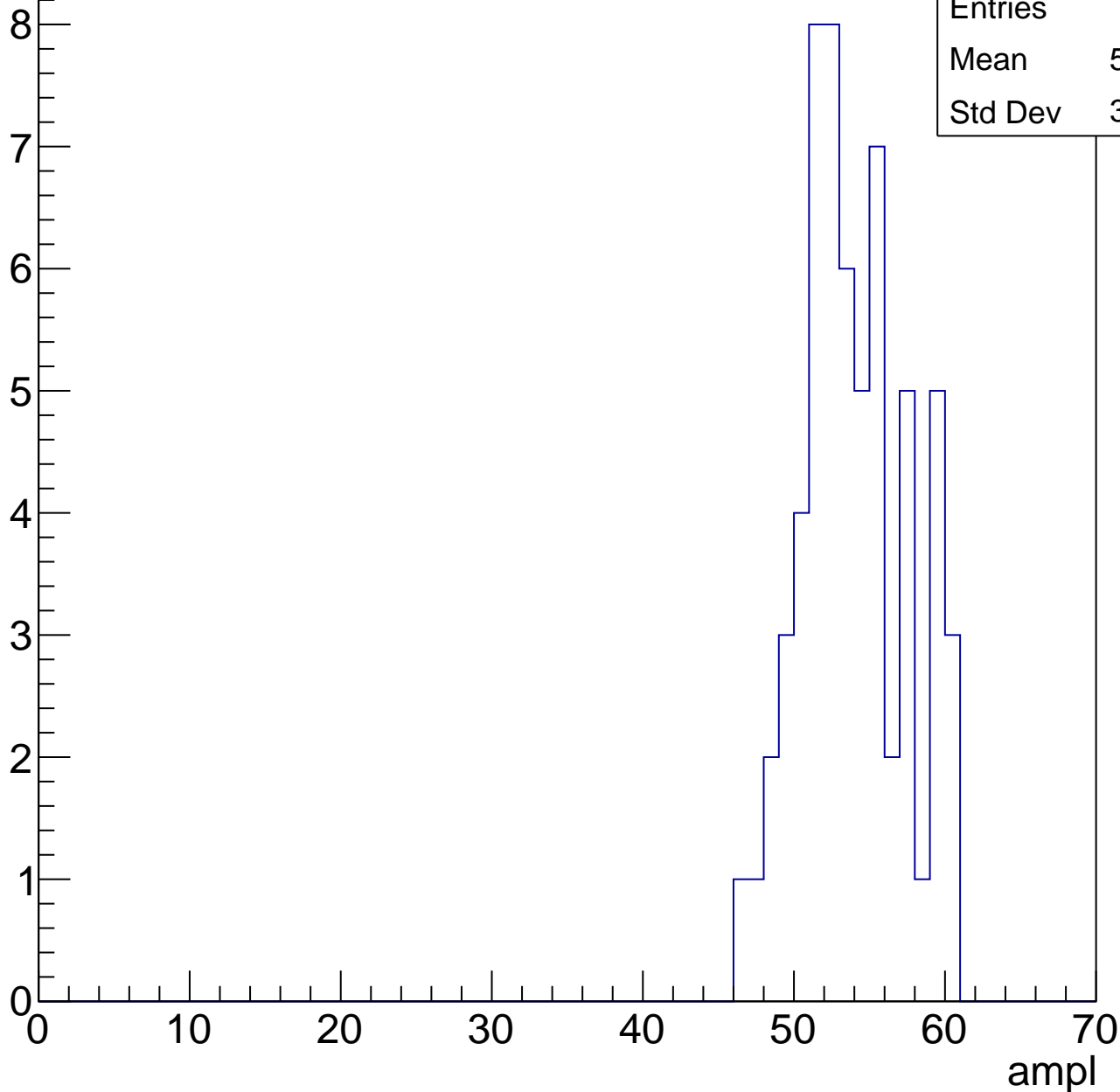


# B1L103S, U25-ch54, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

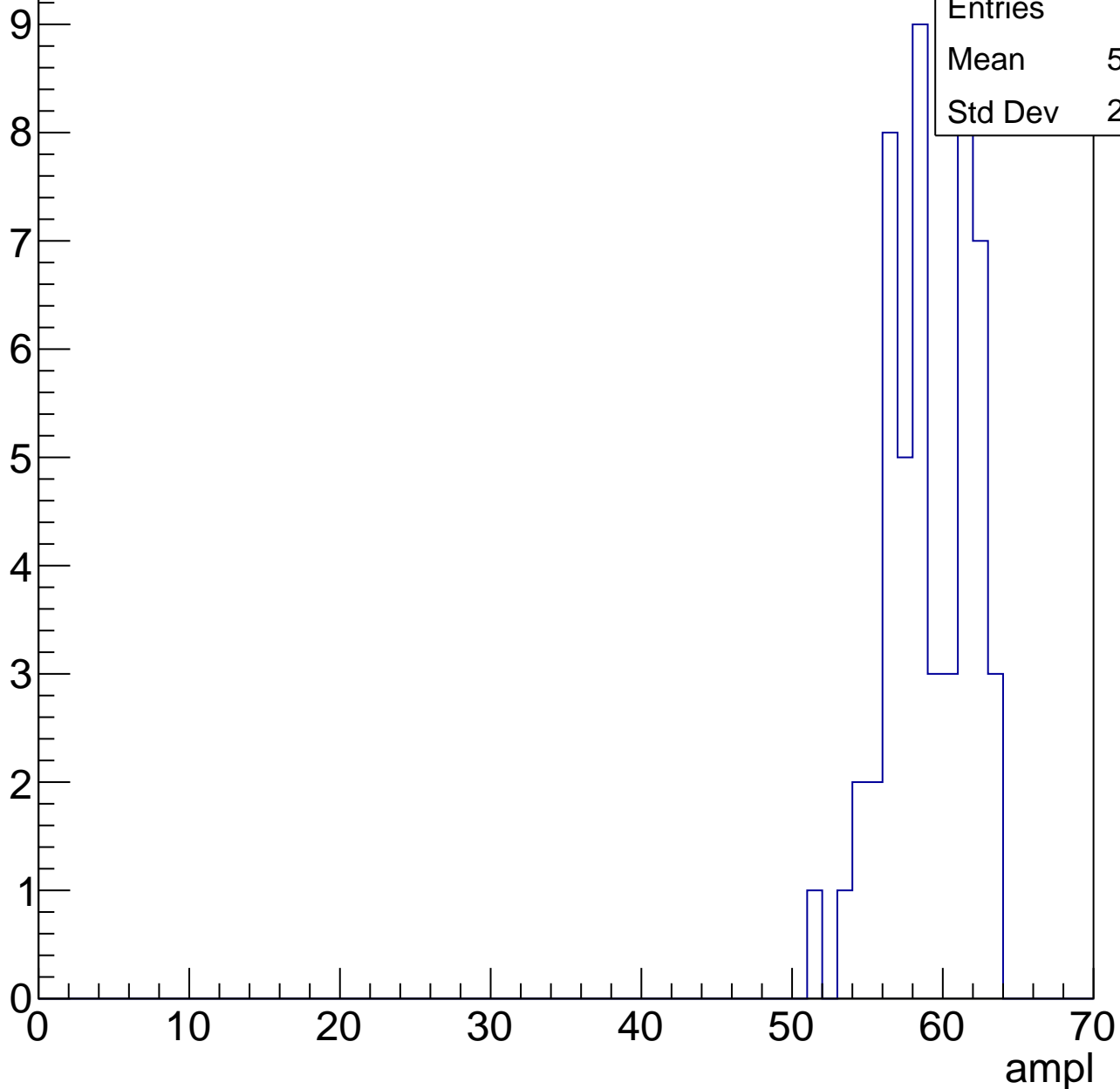
Entries	61
Mean	53.49
Std Dev	3.453



# B1L103S, U25-ch54, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

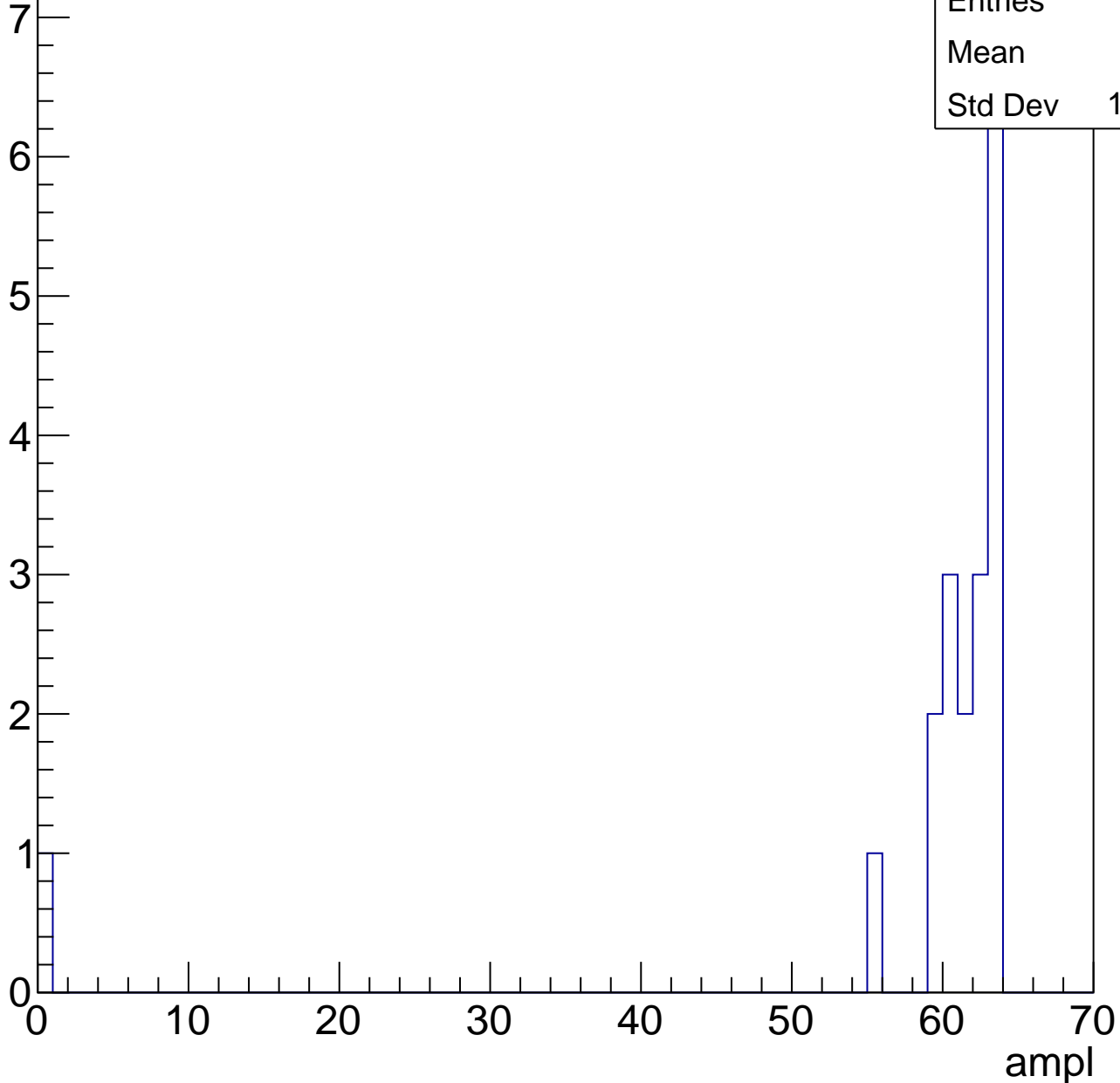


# B1L103S, U25-ch54, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	19
Mean	58
Std Dev	13.82





# B1L103S, U25-ch54, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

# B1L103S, U25-ch55, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	93
Mean	28.51
Std Dev	7.681

Entry

10

8

6

4

2

0

0

10

20

30

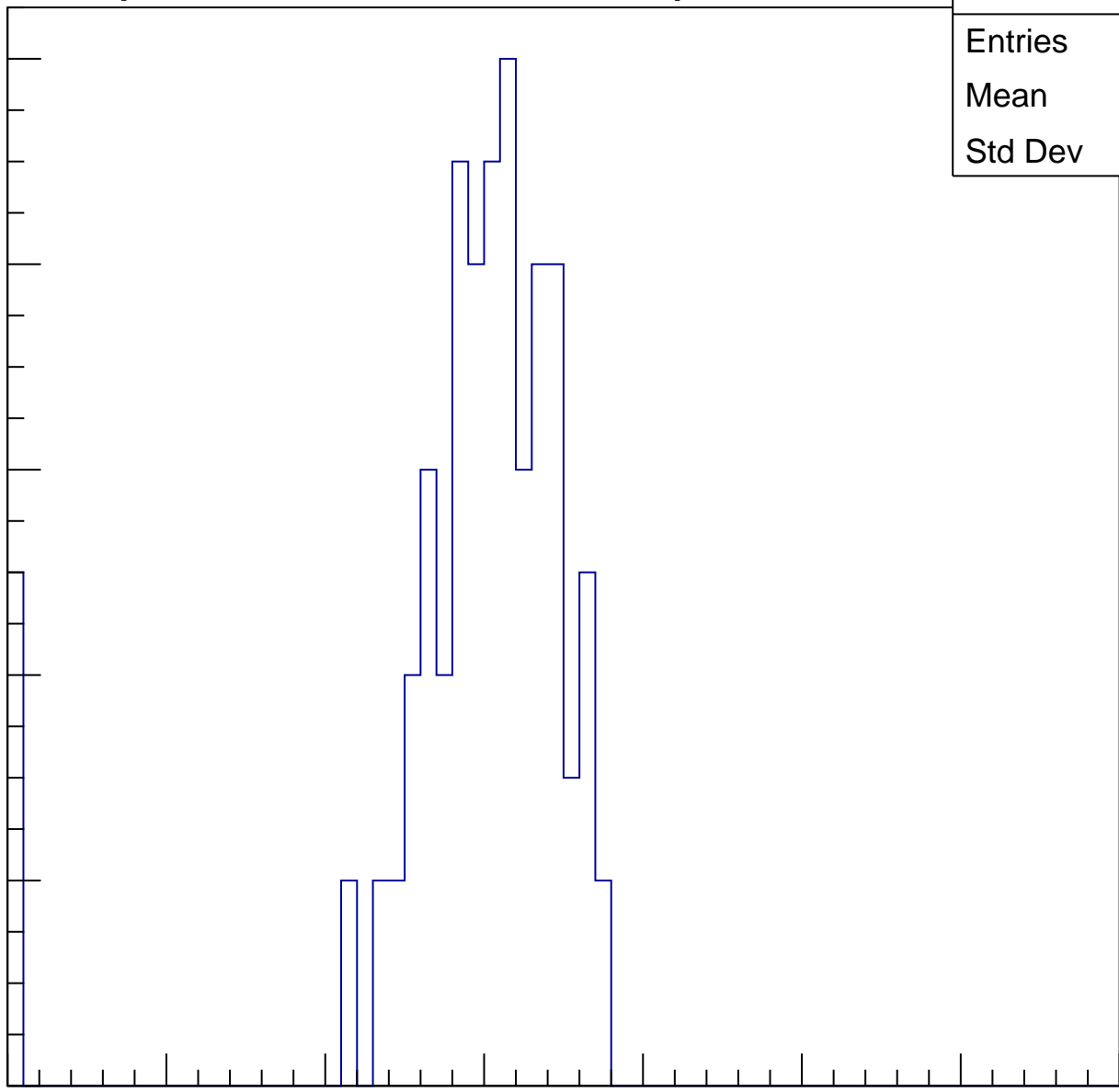
40

50

60

70

ampl

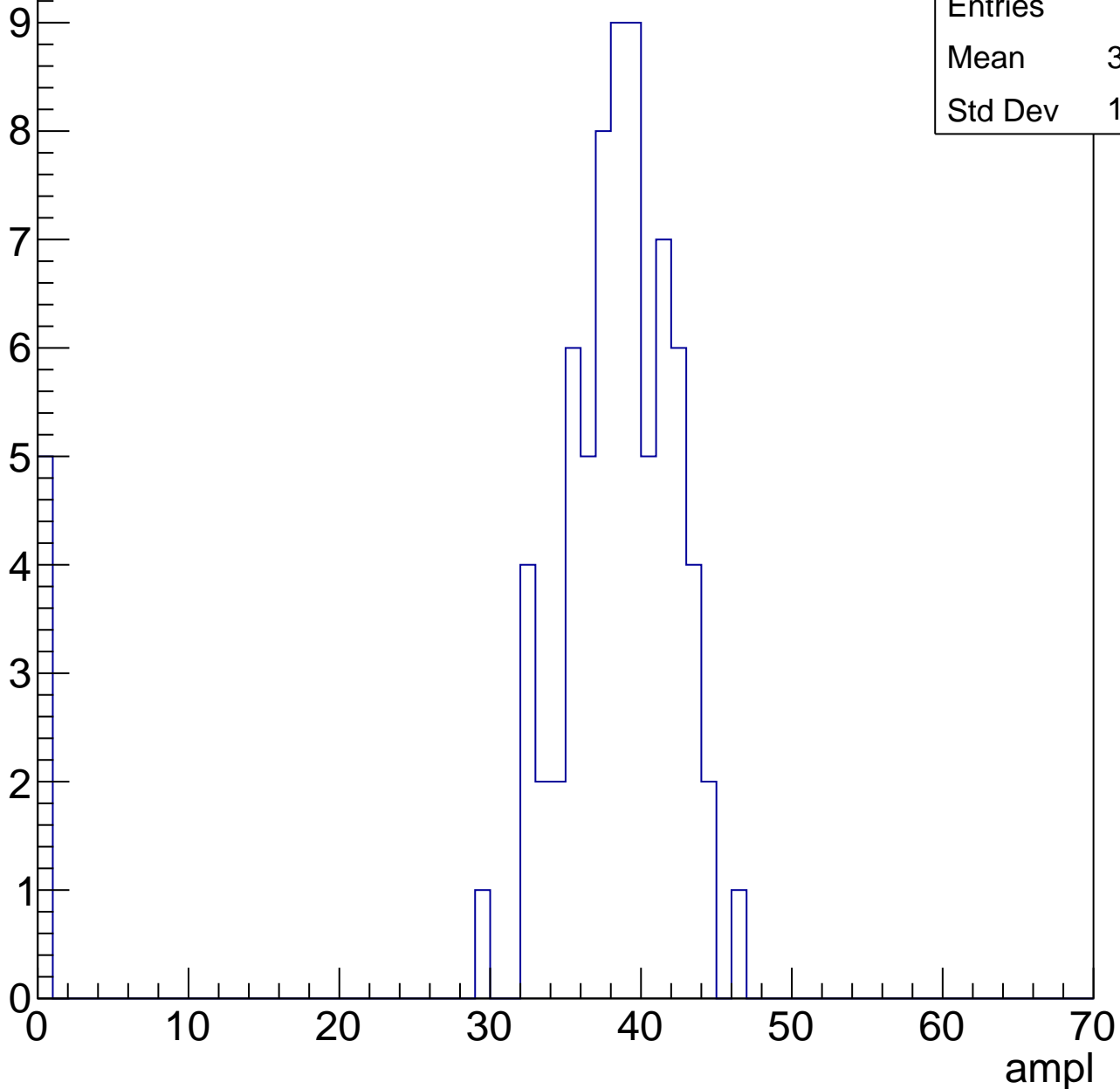


# B1L103S, U25-ch55, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	76
Mean	35.72
Std Dev	10.03

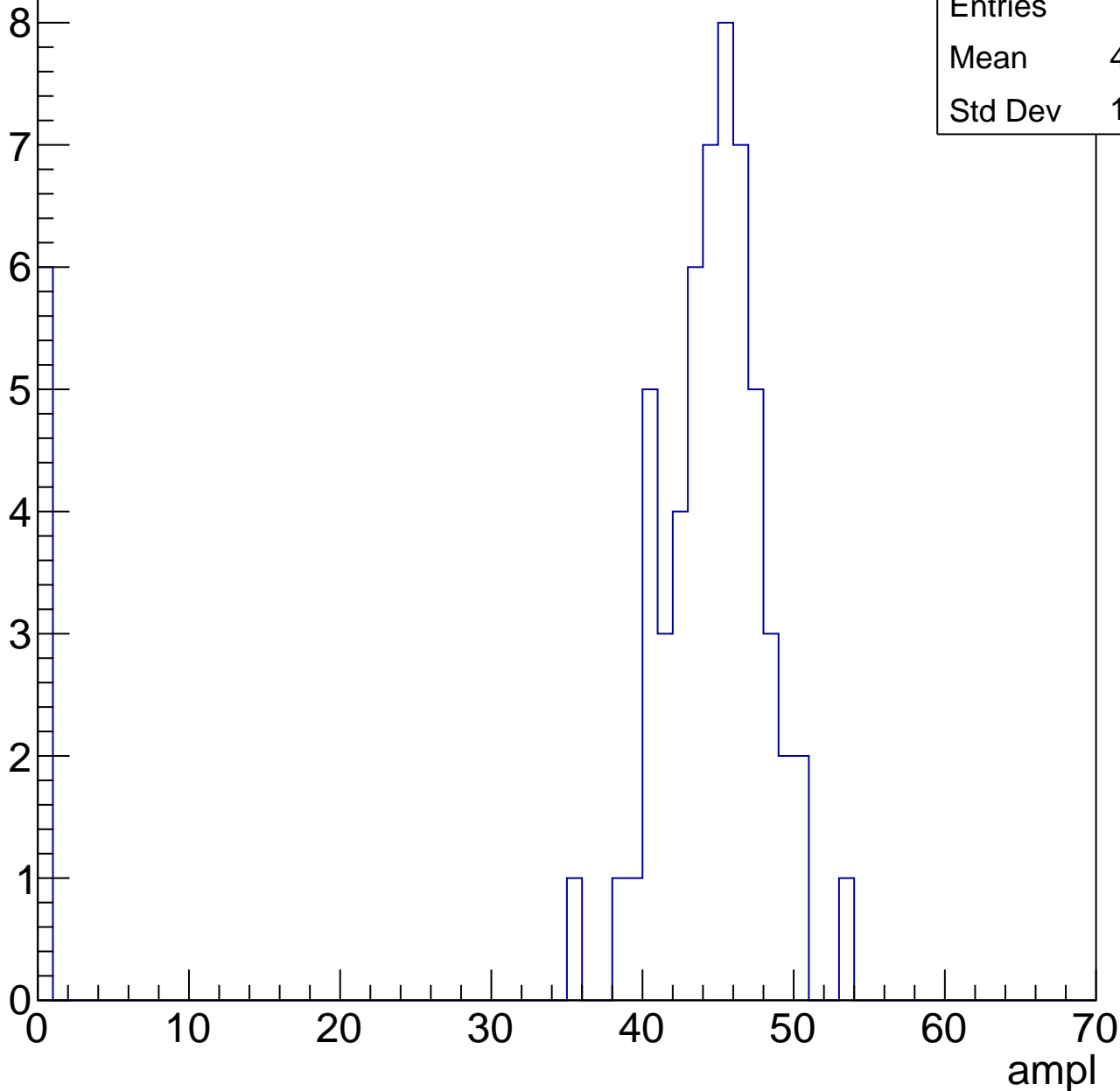


# B1L103S, U25-ch55, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

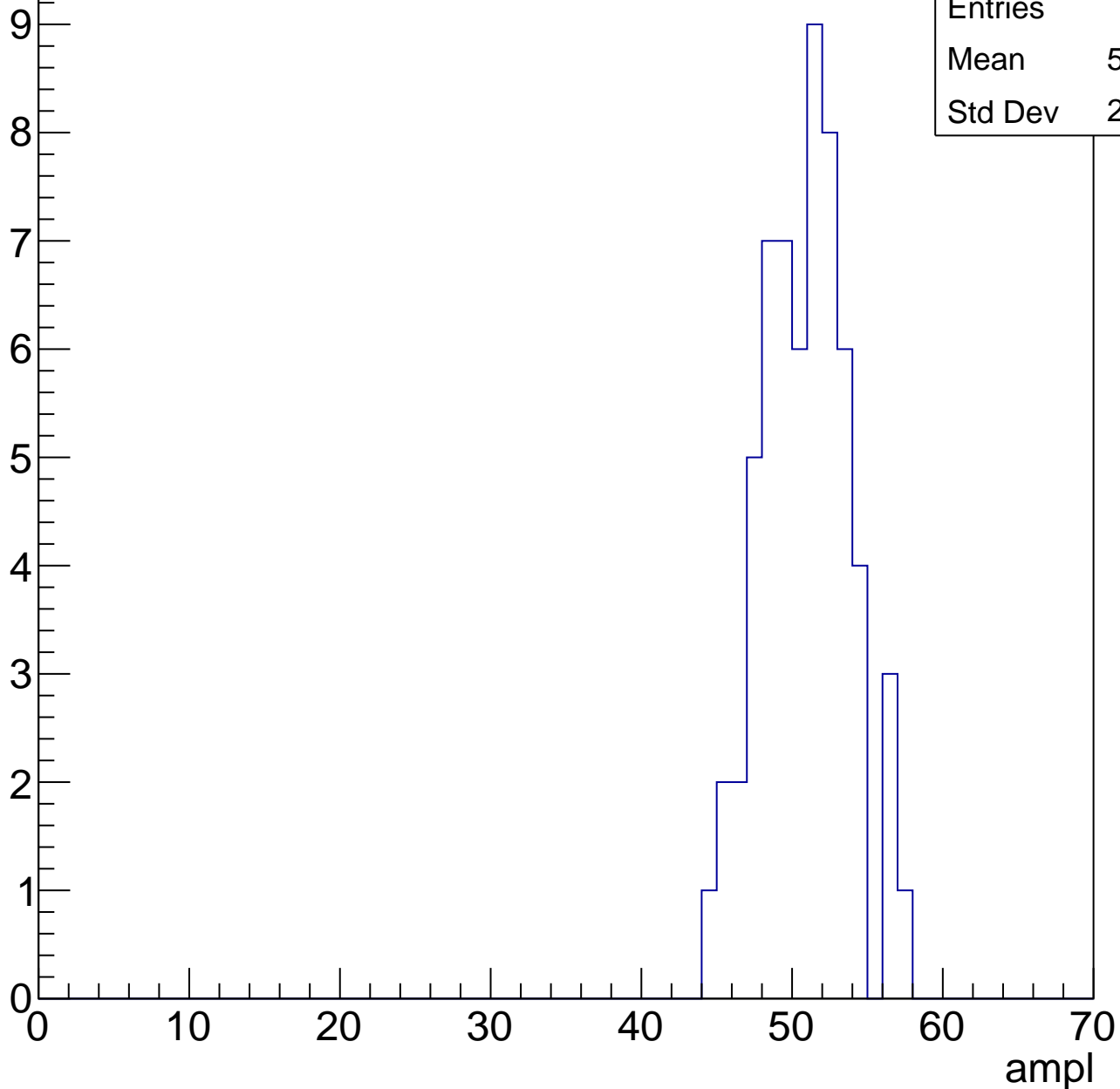
Entries	62
Mean	40.02
Std Dev	13.46



# B1L103S, U25-ch55, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U25-ch55, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	60
Mean	56.4
Std Dev	2.996

Entry

10

8

6

4

2

0

0

10

20

30

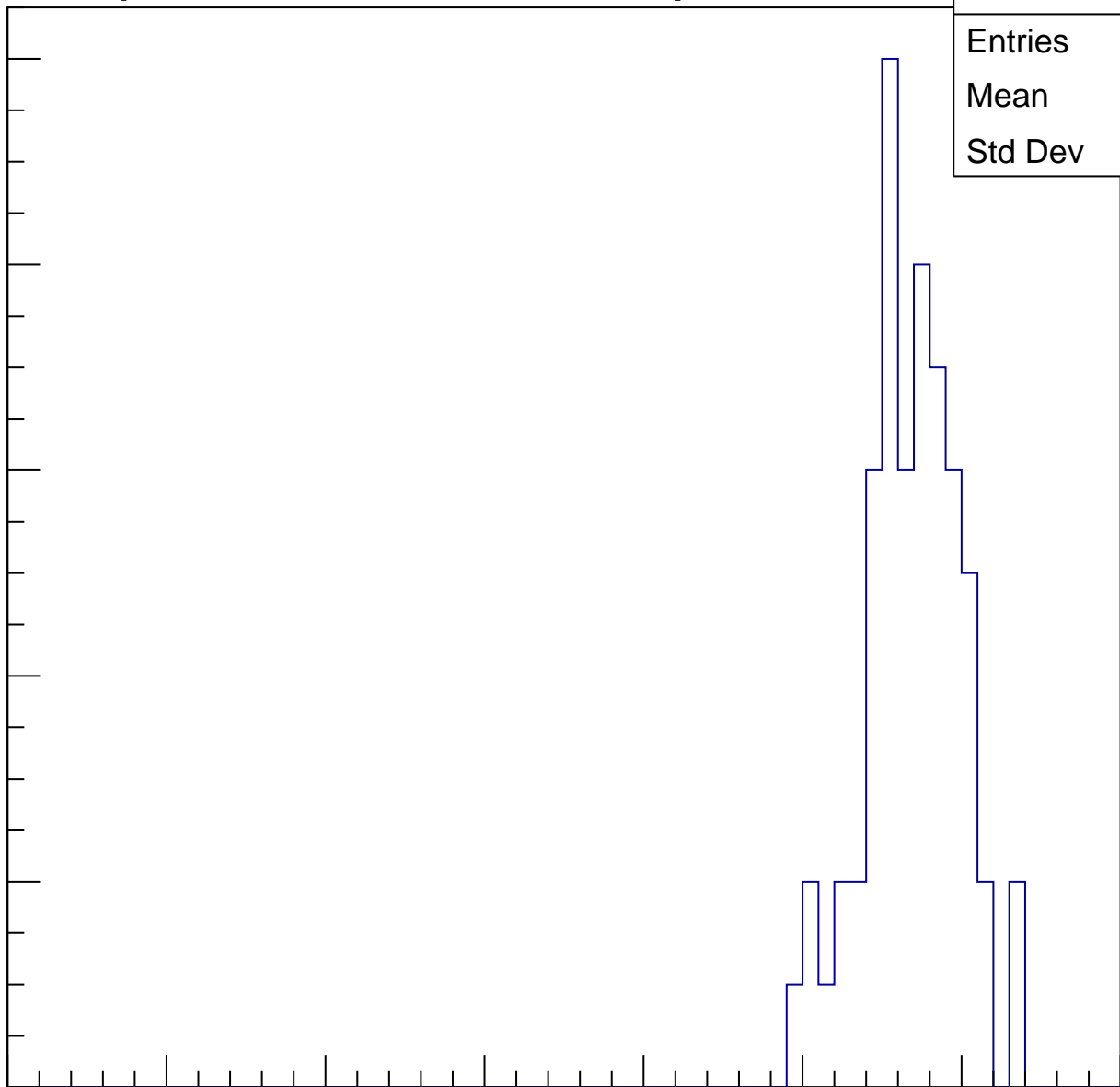
40

50

60

ampl

70

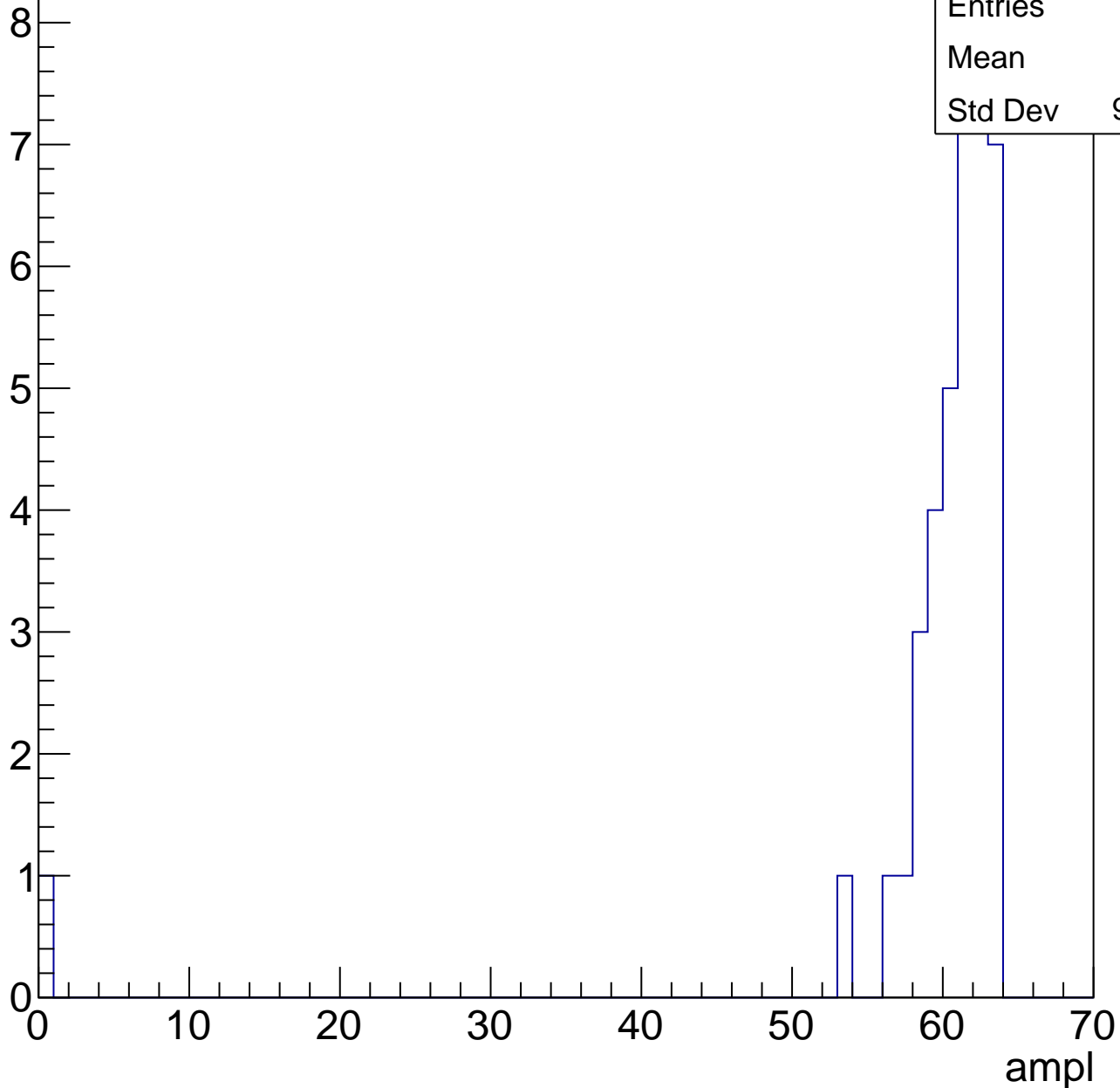


# B1L103S, U25-ch55, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	39
Mean	59
Std Dev	9.811



# B1L103S, U25-ch55, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.33
Std Dev	0.4714

ampl



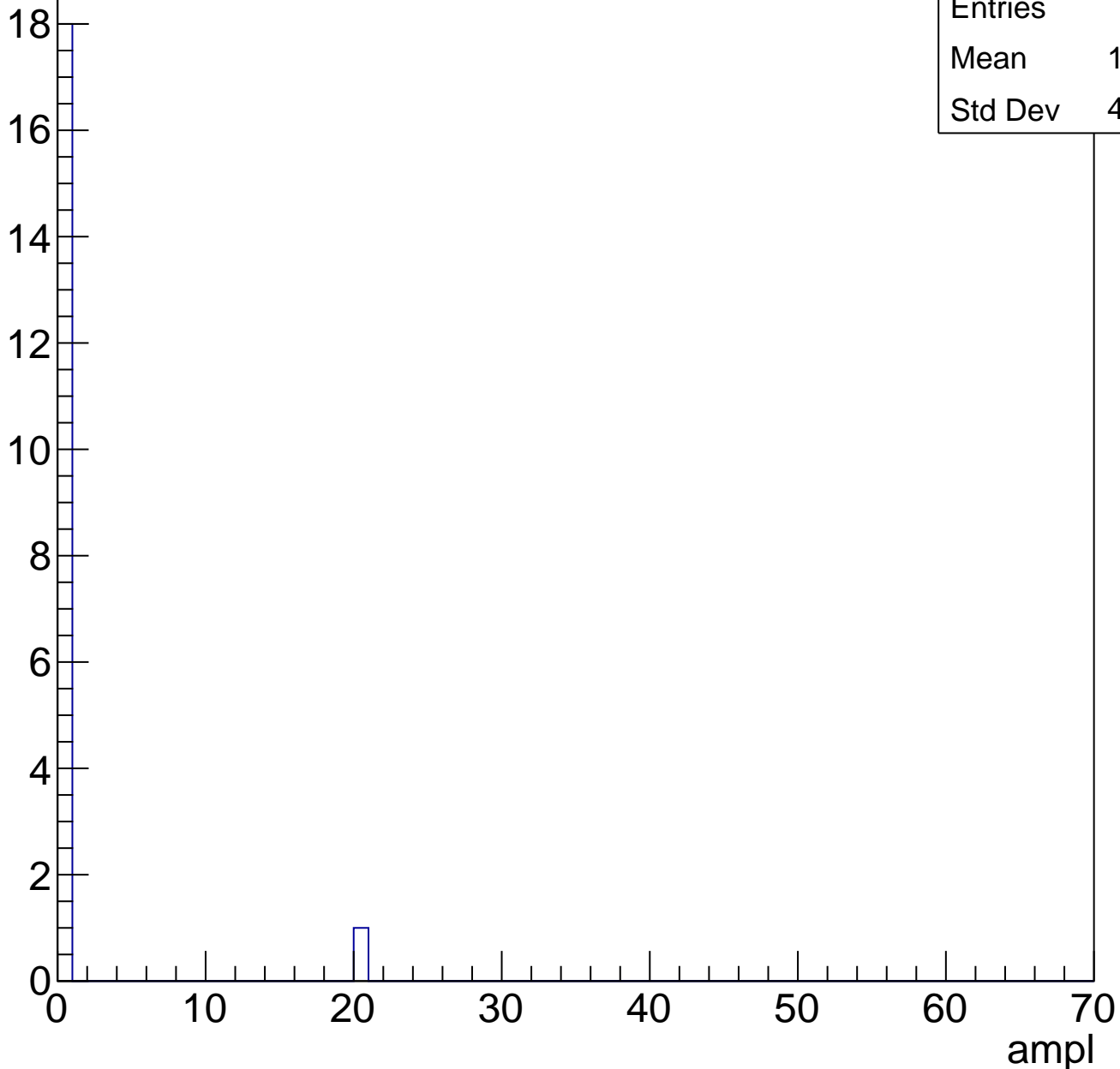


# B1L103S, U25-ch55, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	19
Mean	1.053
Std Dev	4.466

Entry



# B1L103S, U25-ch56, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

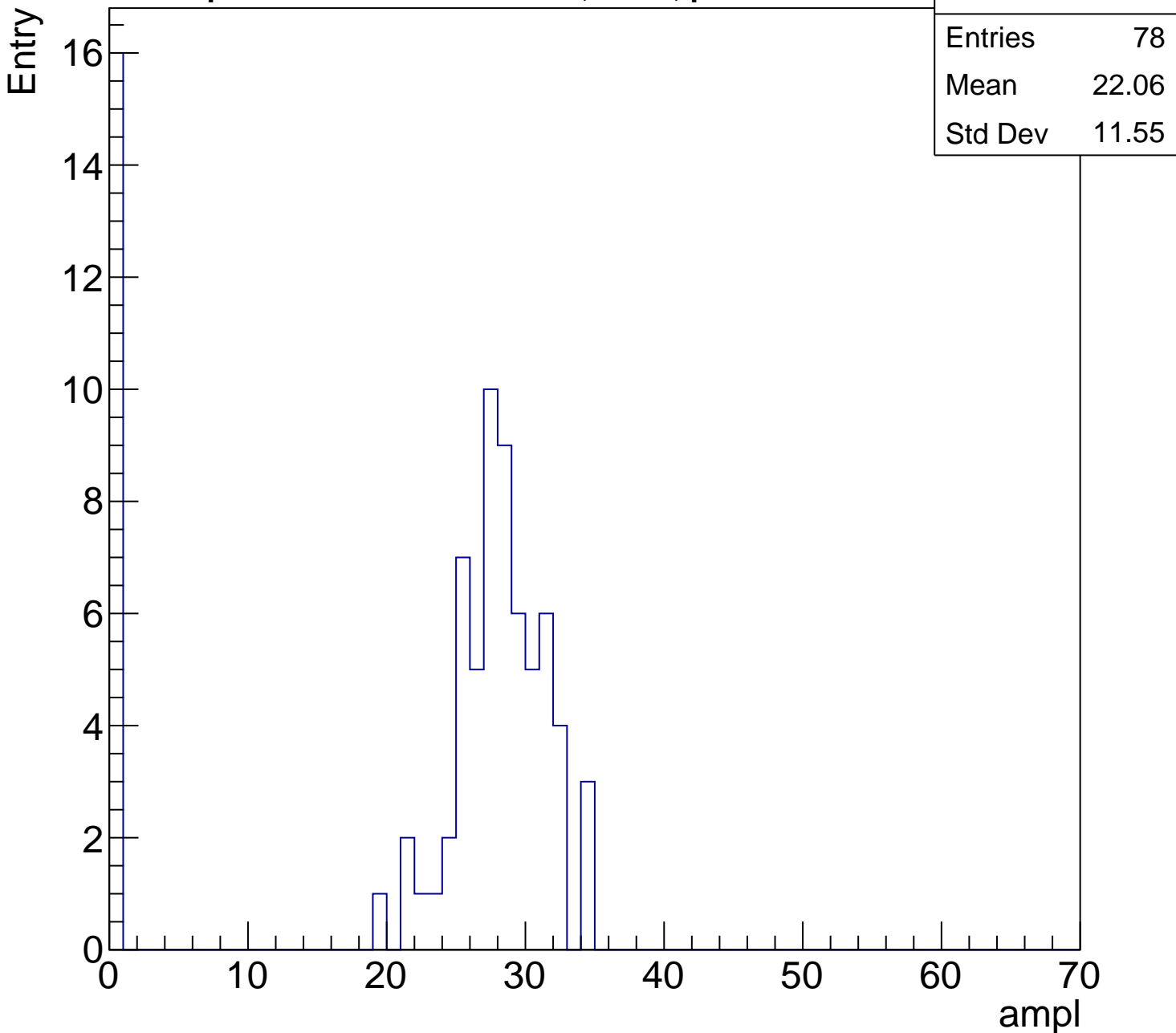
Entries	78
Mean	22.06
Std Dev	11.55

Entry

16  
14  
12  
10  
8  
6  
4  
2  
0

ampl

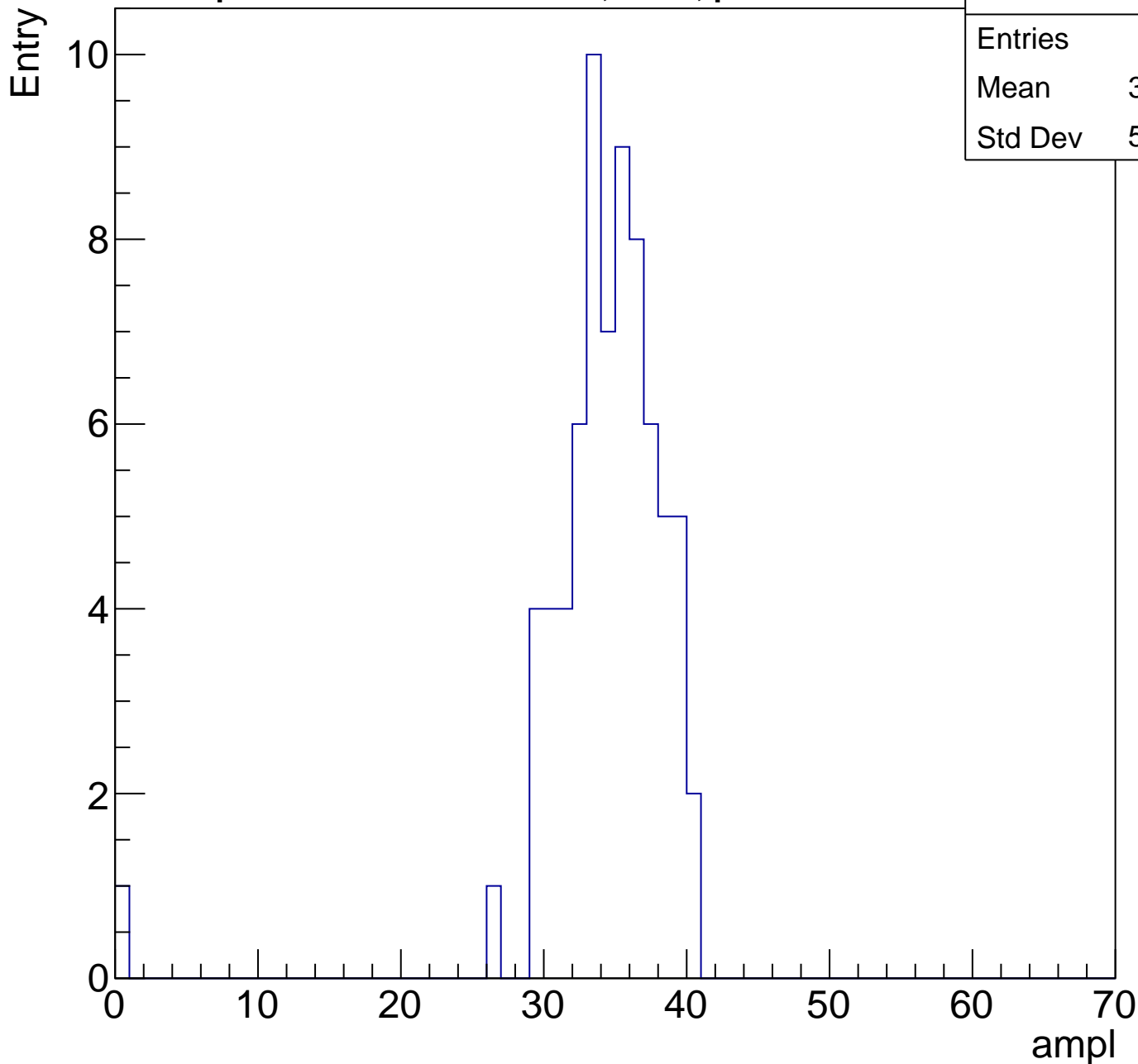
0 10 20 30 40 50 60 70



# B1L103S, U25-ch56, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	72
Mean	33.83
Std Dev	5.033



# B1L103S, U25-ch56, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

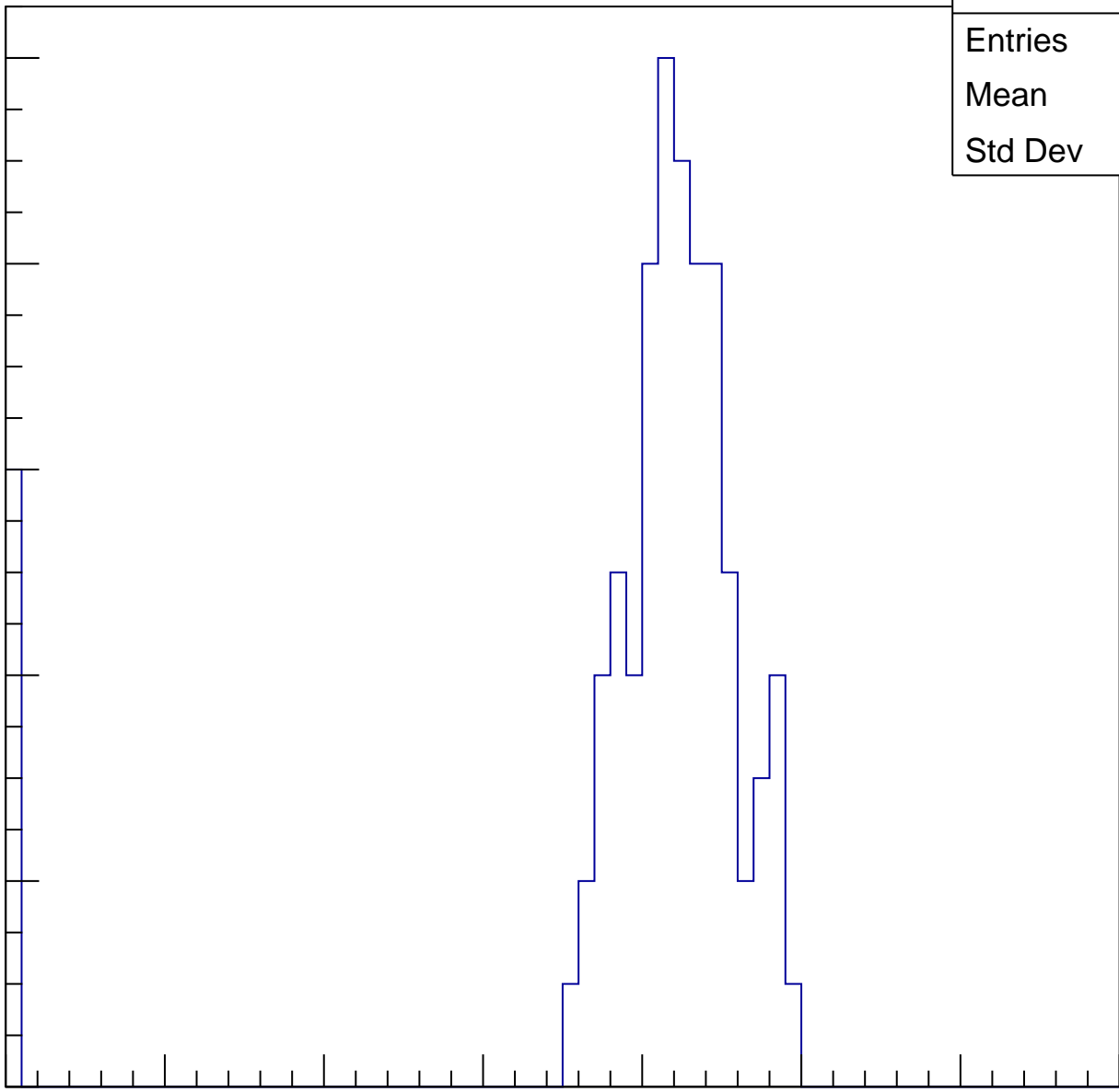
Entries	80
Mean	38.8
Std Dev	11.47

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

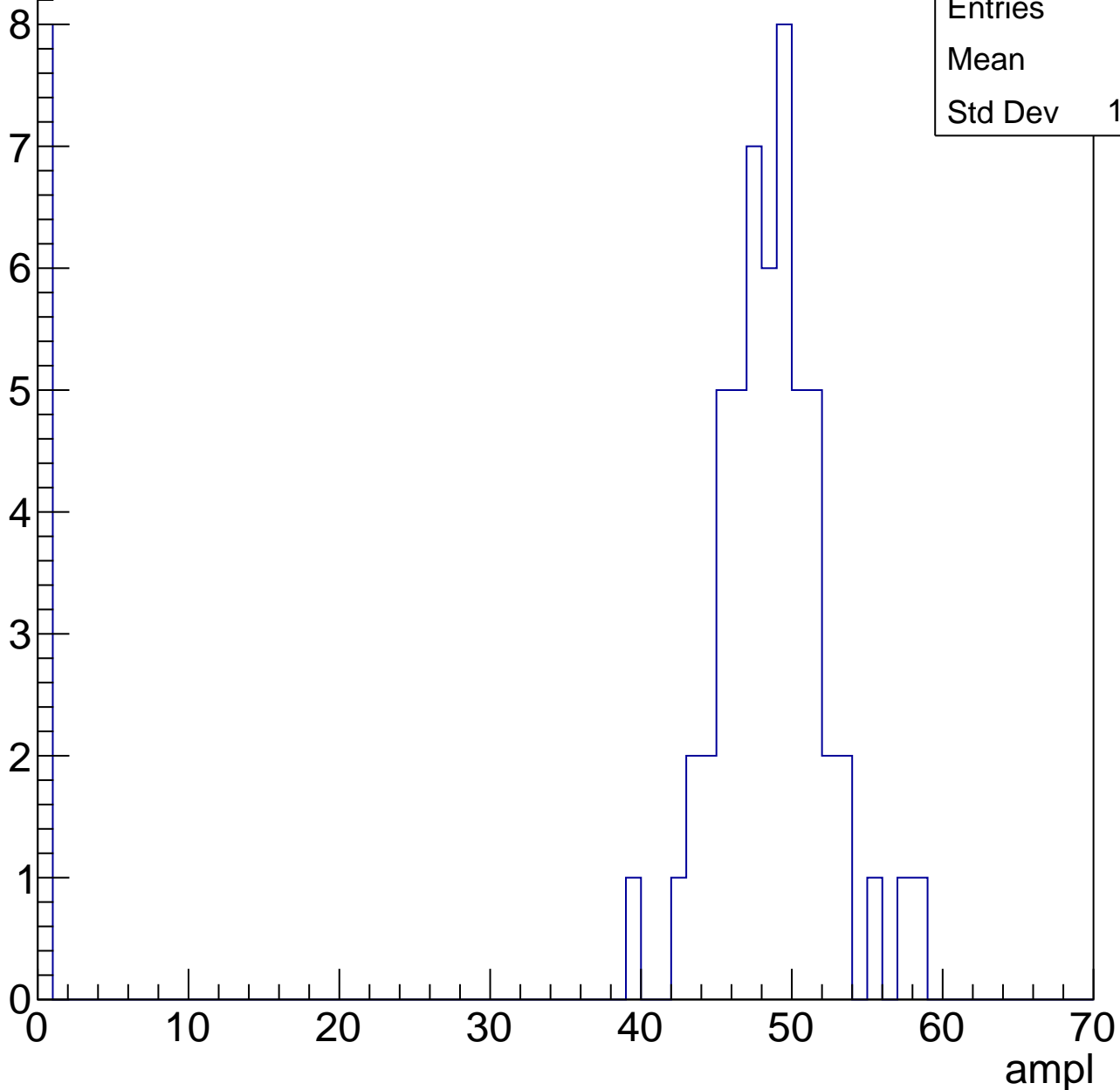


# B1L103S, U25-ch56, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	62
Mean	42
Std Dev	16.49

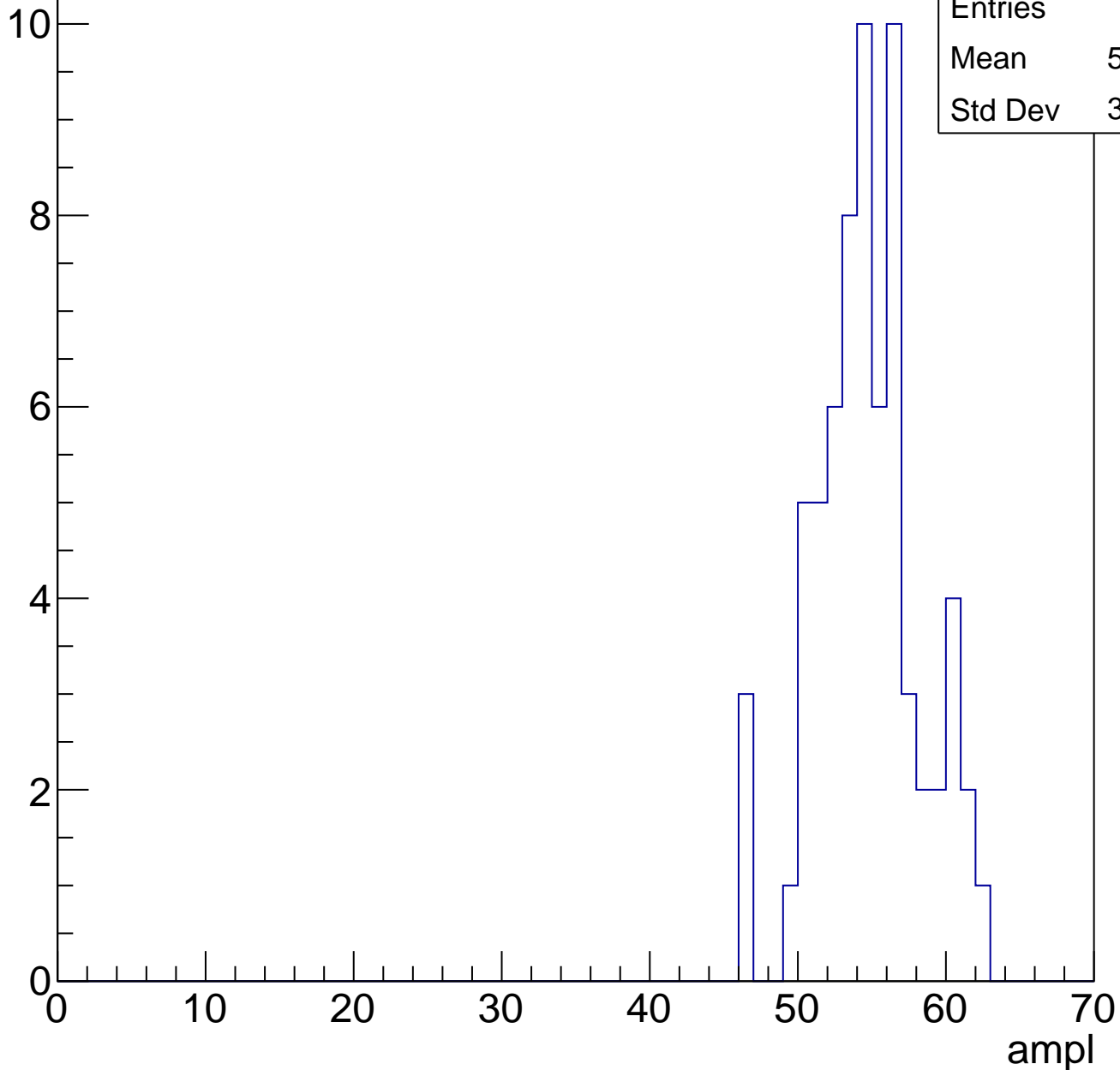


# B1L103S, U25-ch56, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	68
Mean	54.22
Std Dev	3.497

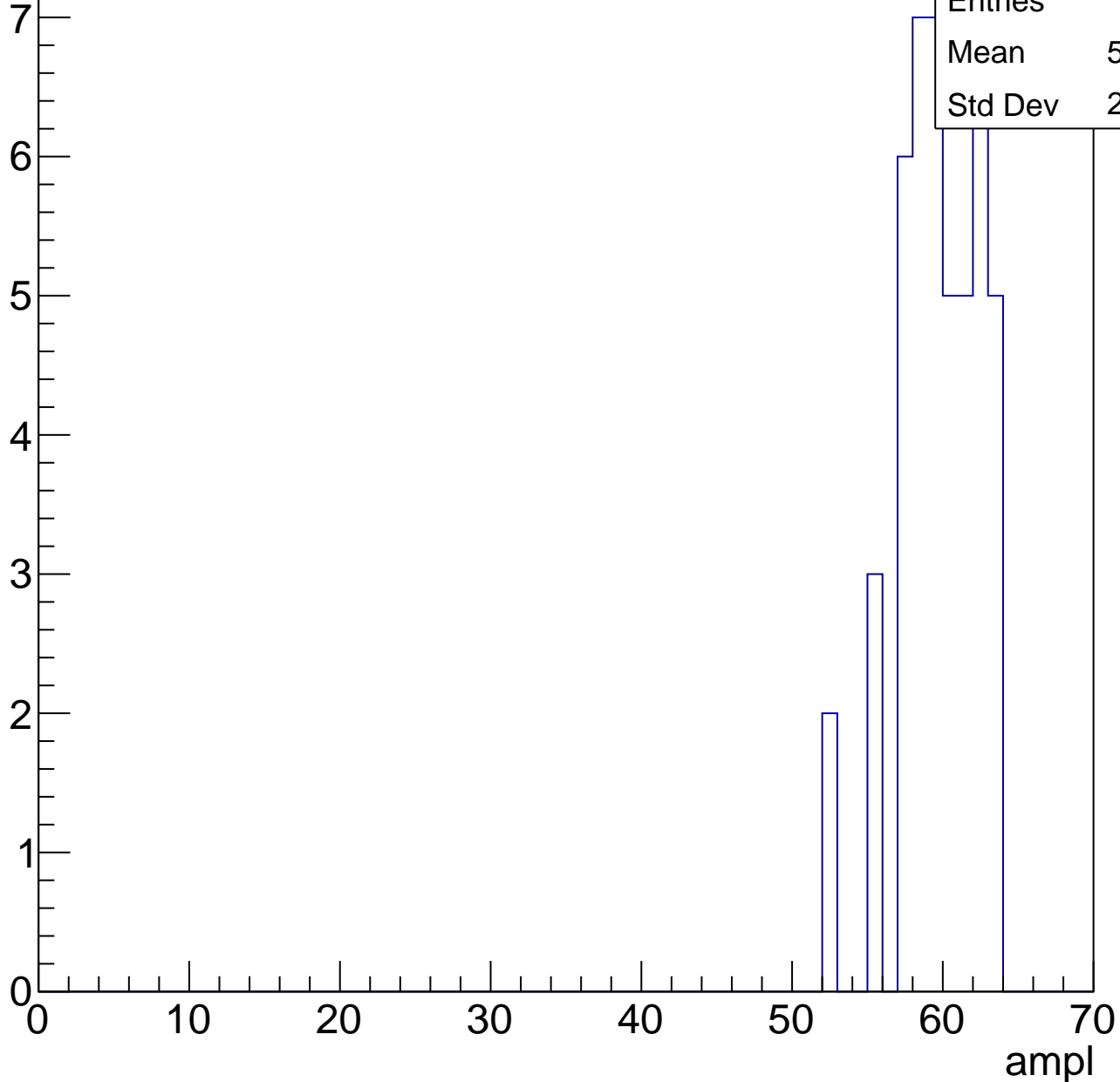
Entry



# B1L103S, U25-ch56, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

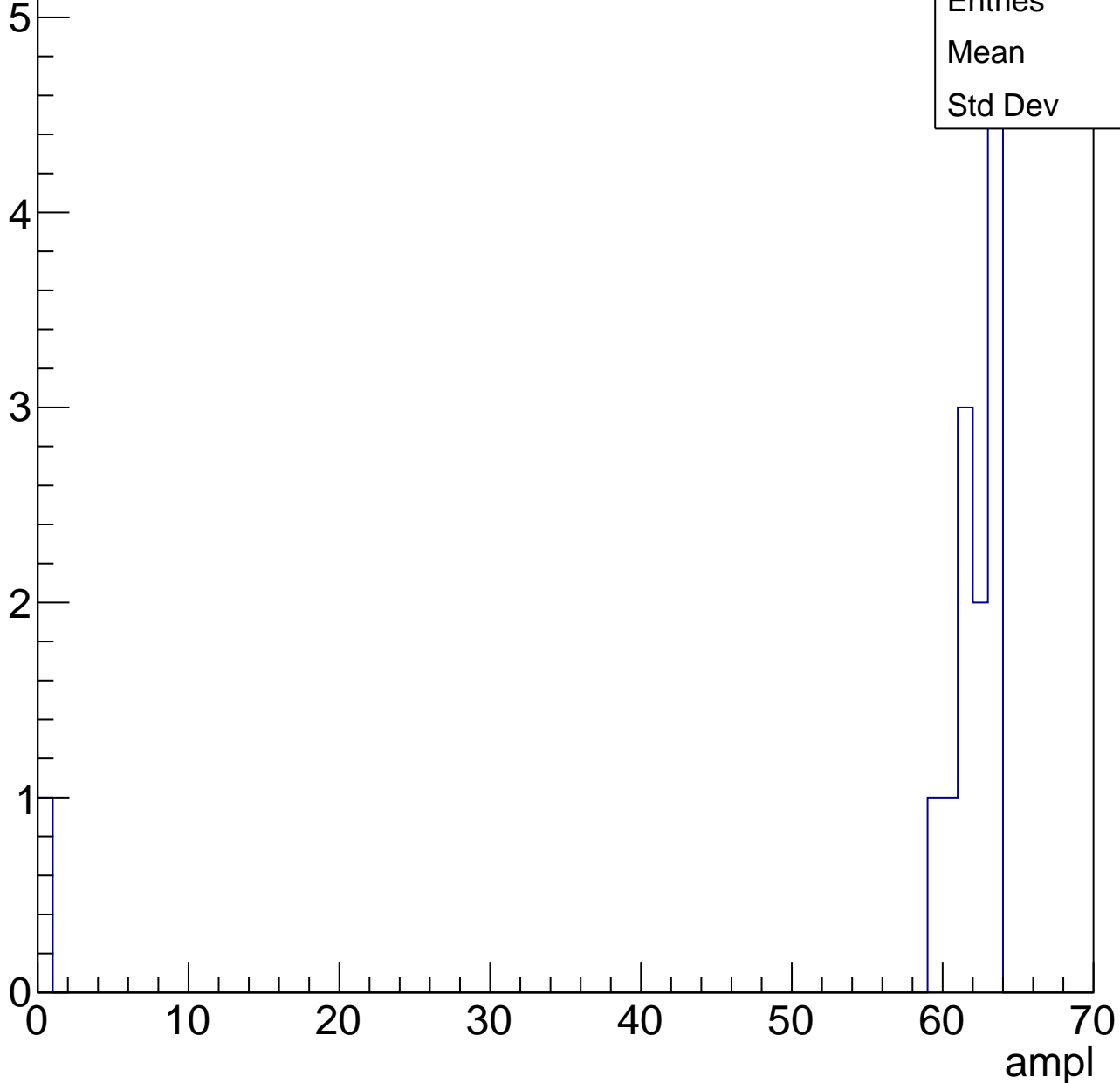


# B1L103S, U25-ch56, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	13
Mean	57
Std Dev	16.5





# B1L103S, U25-ch56, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

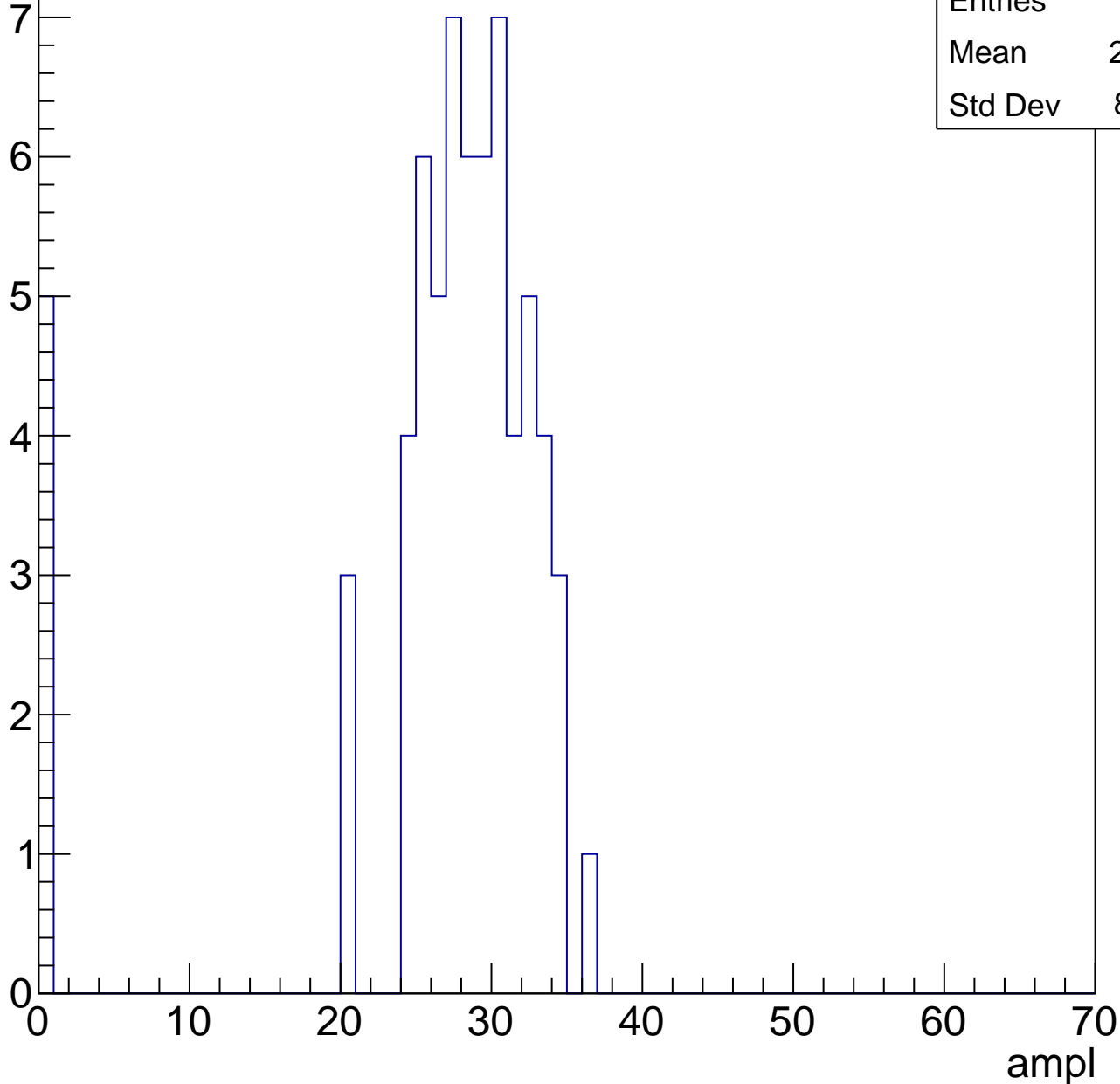
Entries	19
Mean	0
Std Dev	0

# B1L103S, U25-ch57, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	66
Mean	26.23
Std Dev	8.231

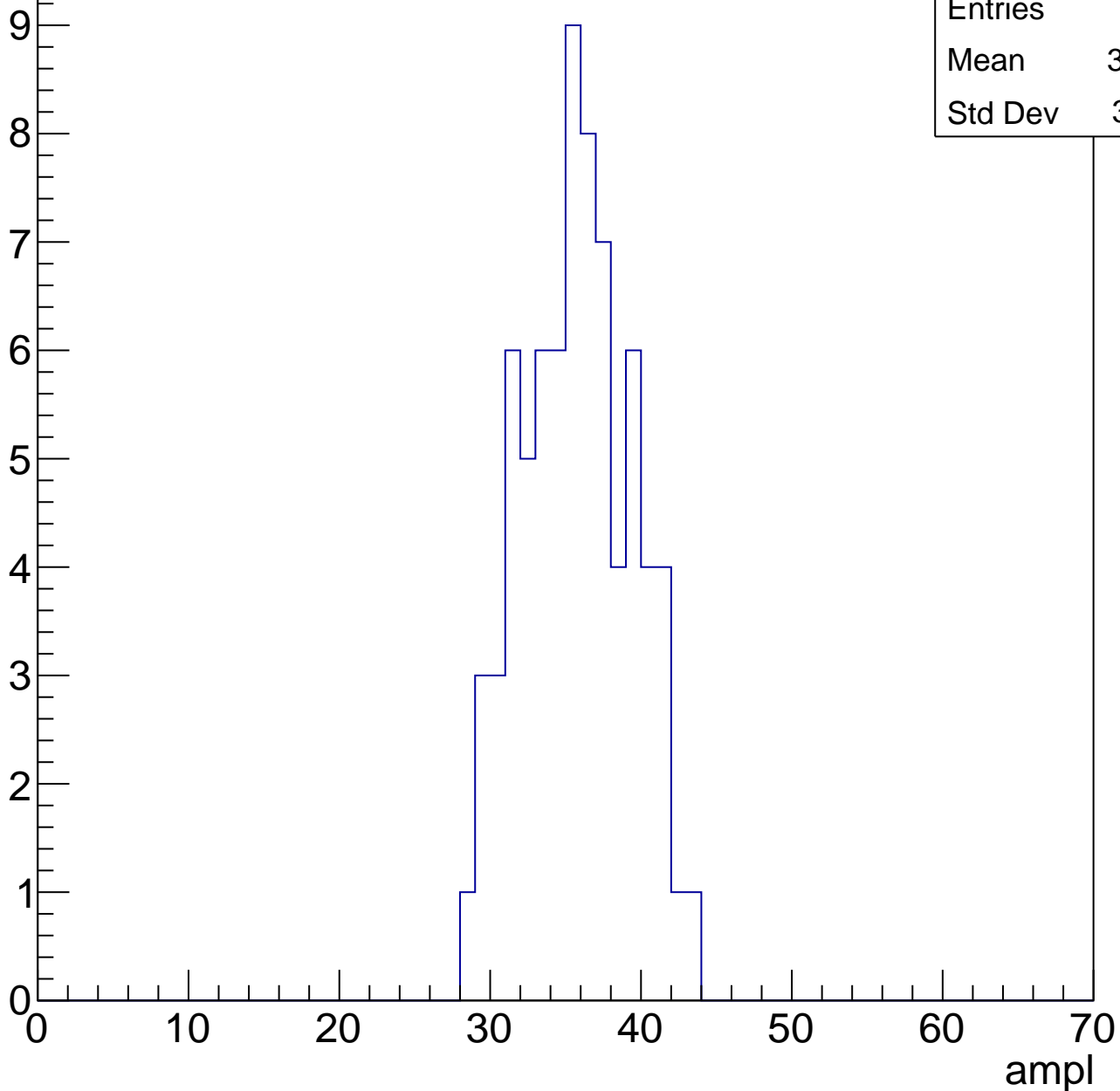


# B1L103S, U25-ch57, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	74
Mean	35.27
Std Dev	3.531

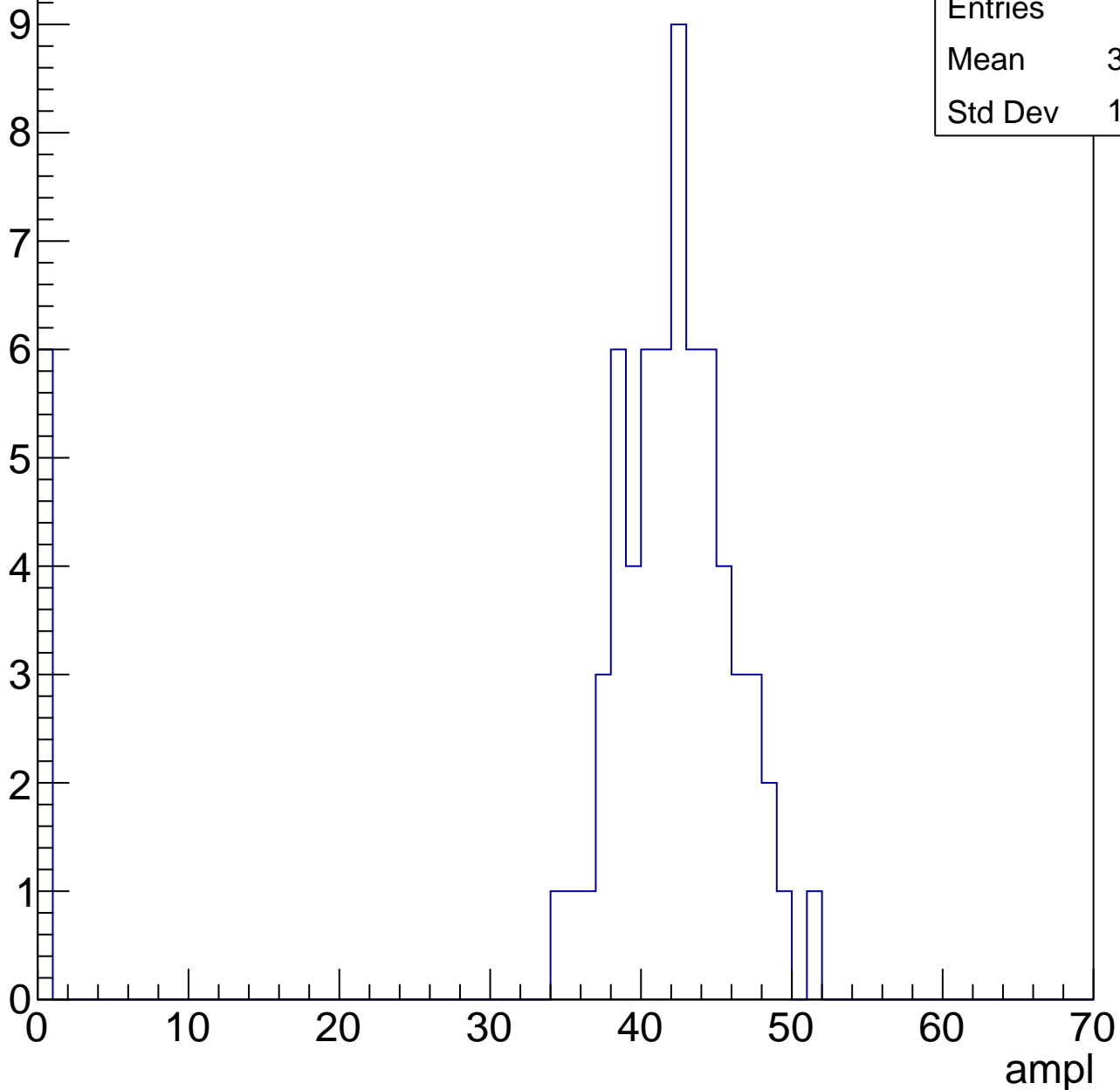


# B1L103S, U25-ch57, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	69
Mean	38.28
Std Dev	12.28

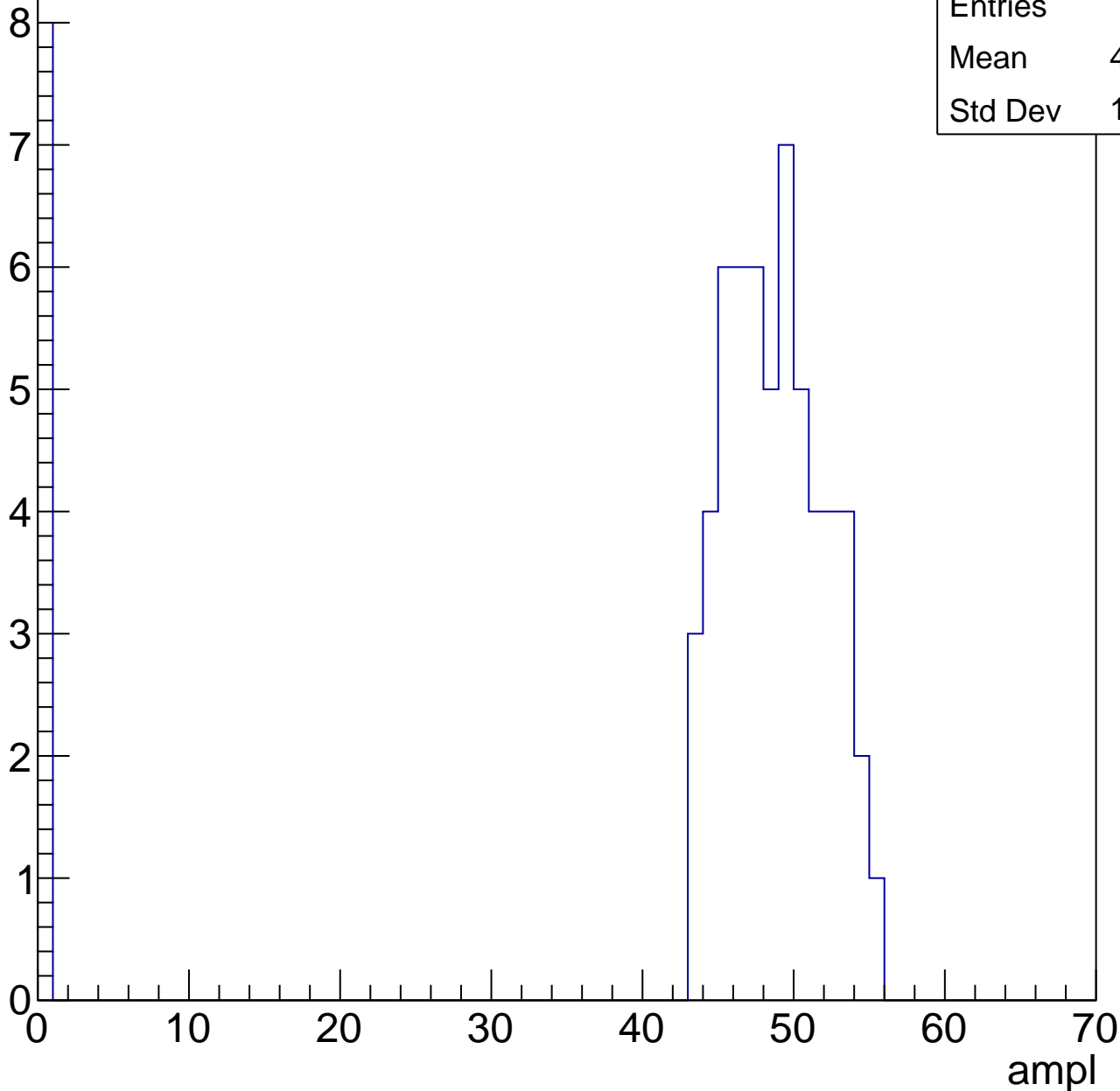


# B1L103S, U25-ch57, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	65
Mean	42.35
Std Dev	16.14

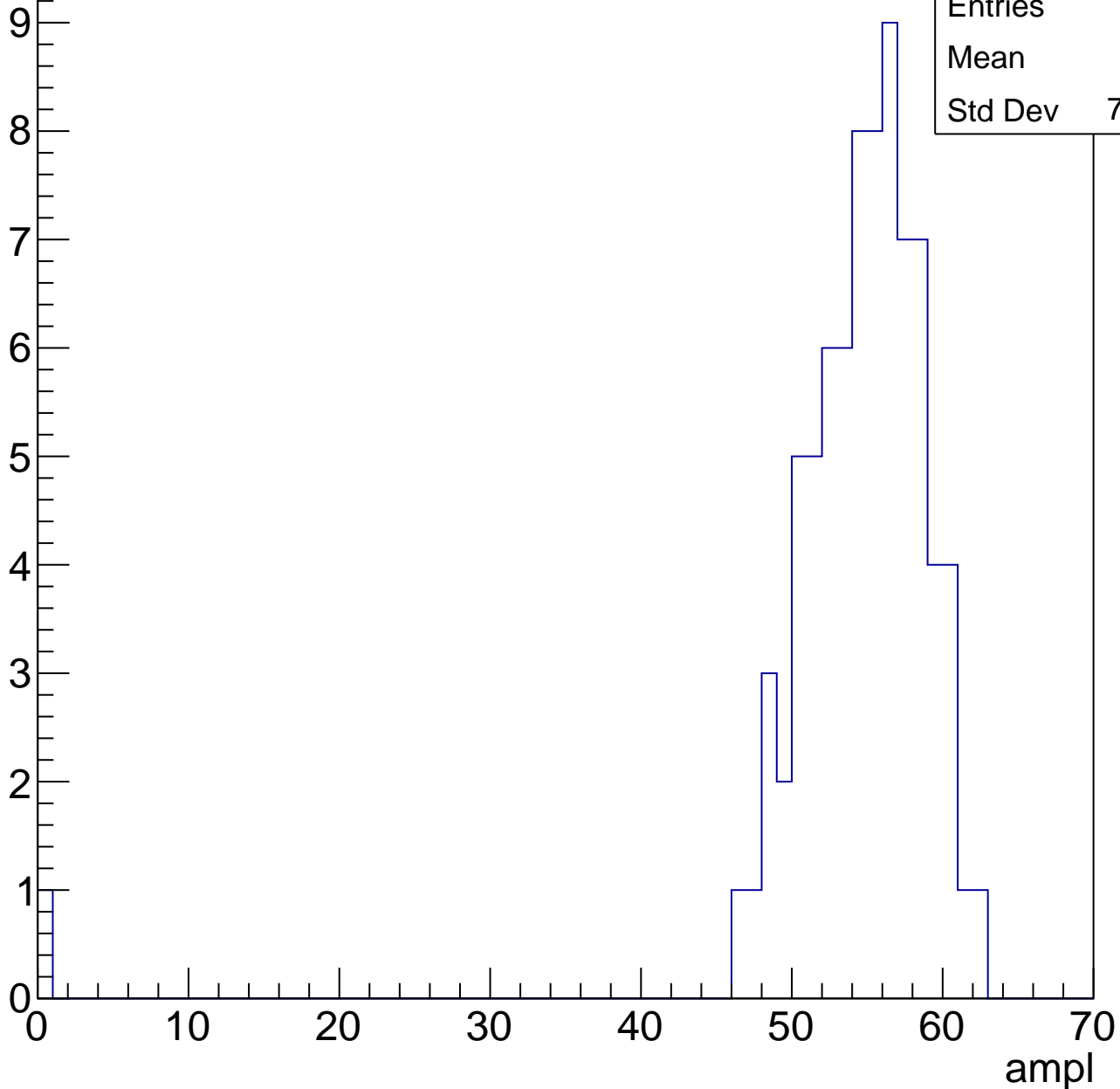


# B1L103S, U25-ch57, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	79
Mean	53.8
Std Dev	7.039

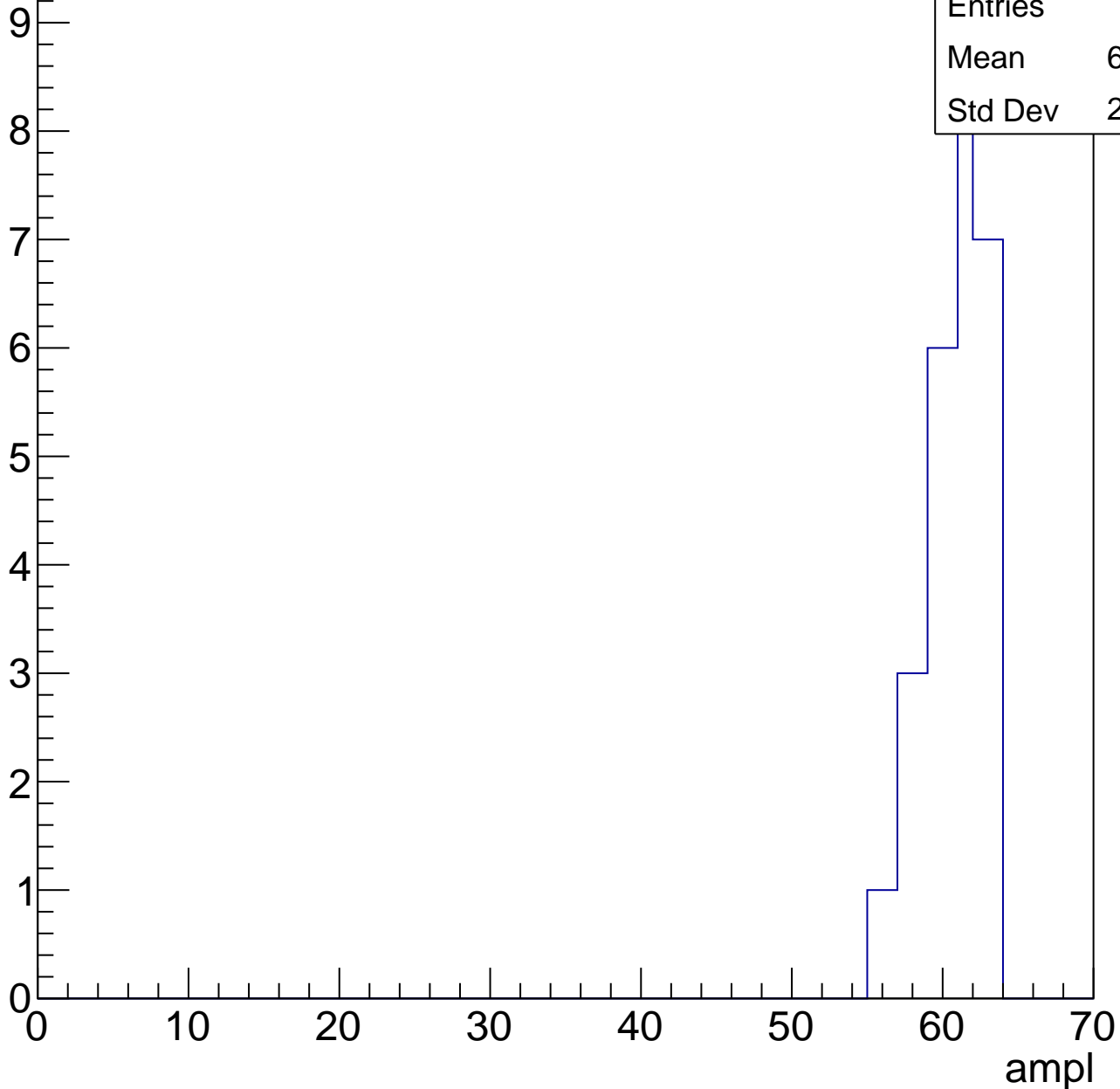


# B1L103S, U25-ch57, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	43
Mean	60.33
Std Dev	2.054



# B1L103S, U25-ch57, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U25-ch57, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

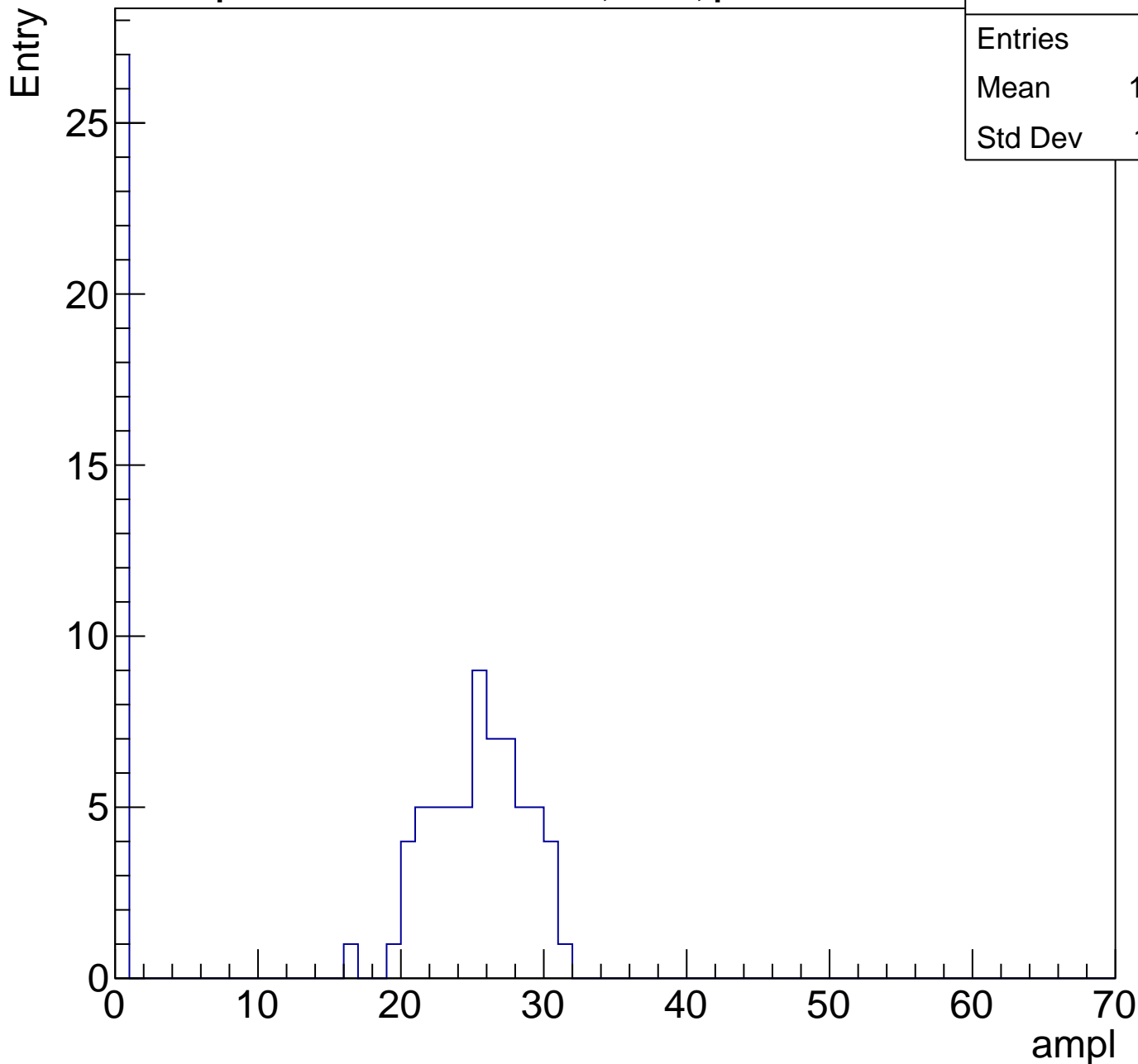
Entry



# B1L103S, U25-ch58, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	91
Mean	17.55
Std Dev	11.71

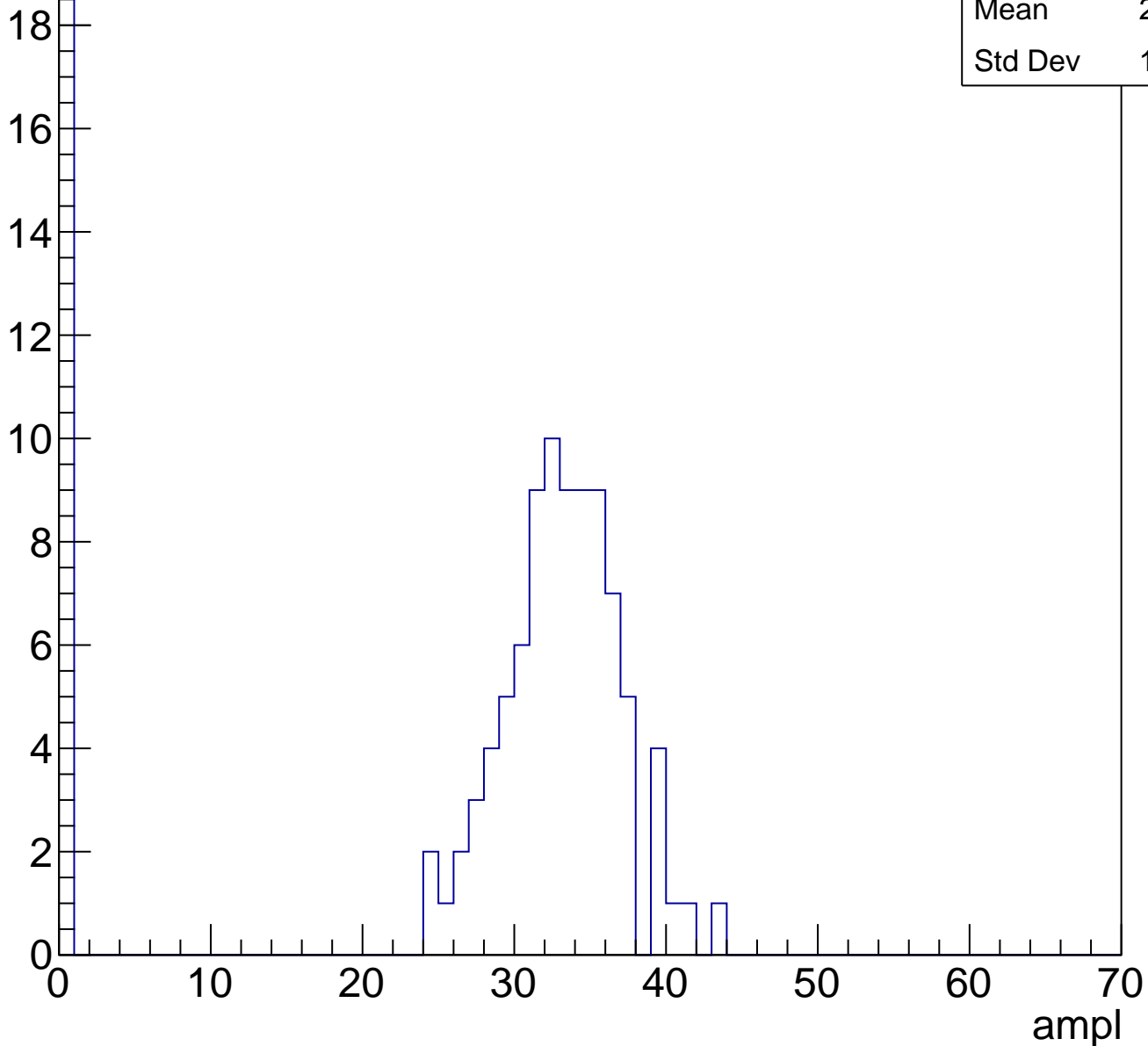


# B1L103S, U25-ch58, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	107
Mean	26.89
Std Dev	12.95

Entry

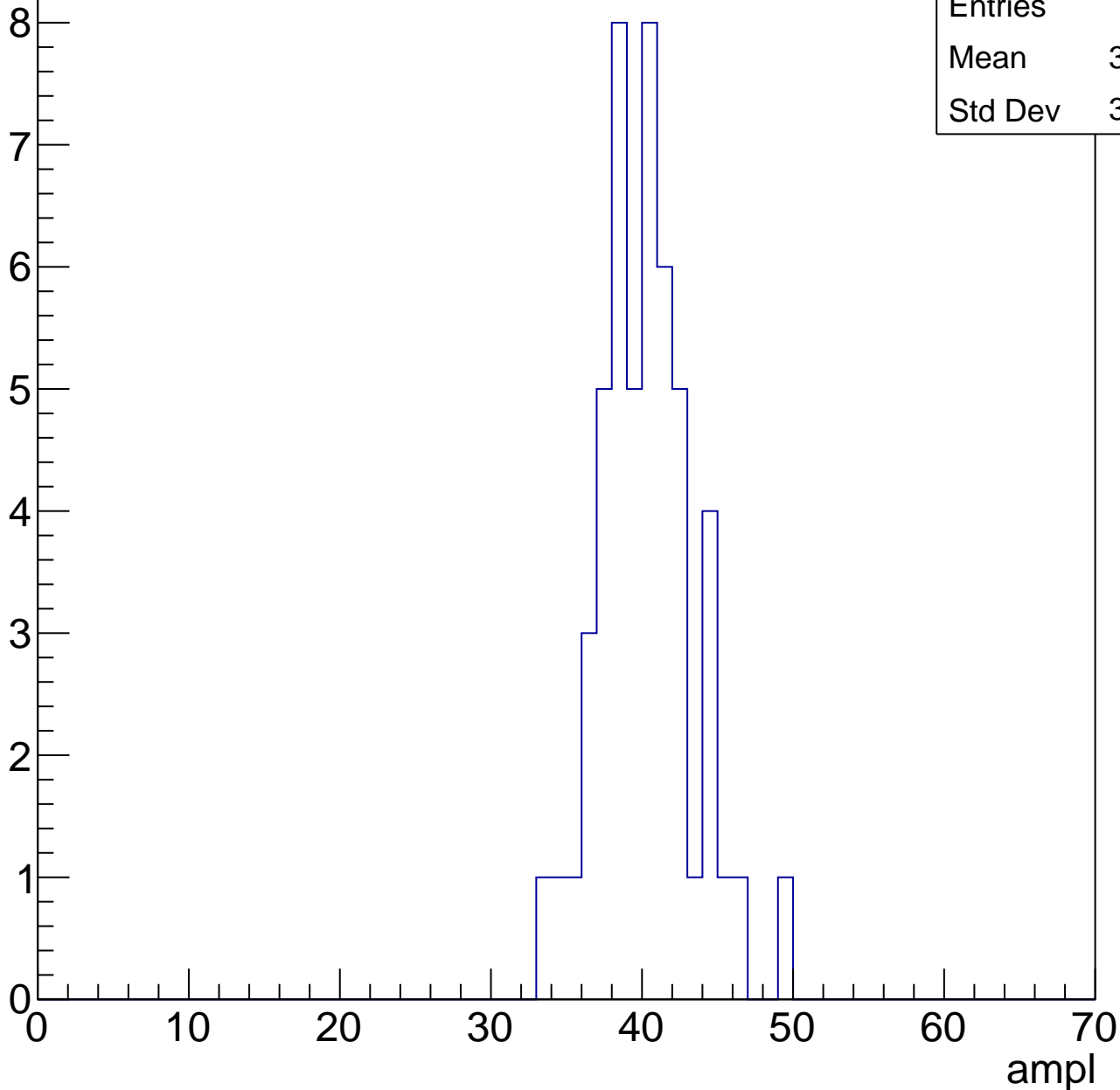


# B1L103S, U25-ch58, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

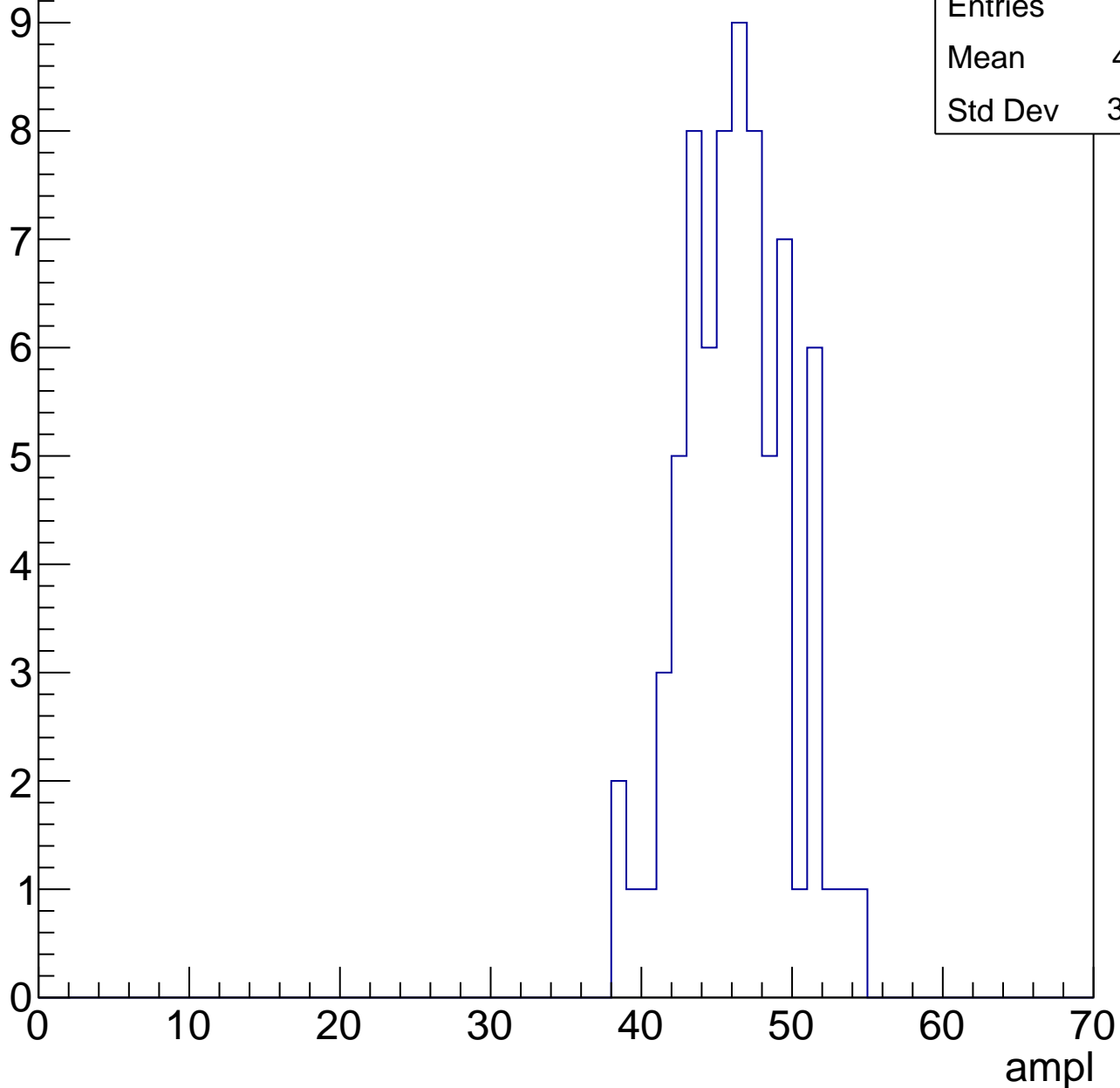
Entries	51
Mean	39.78
Std Dev	3.063



# B1L103S, U25-ch58, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

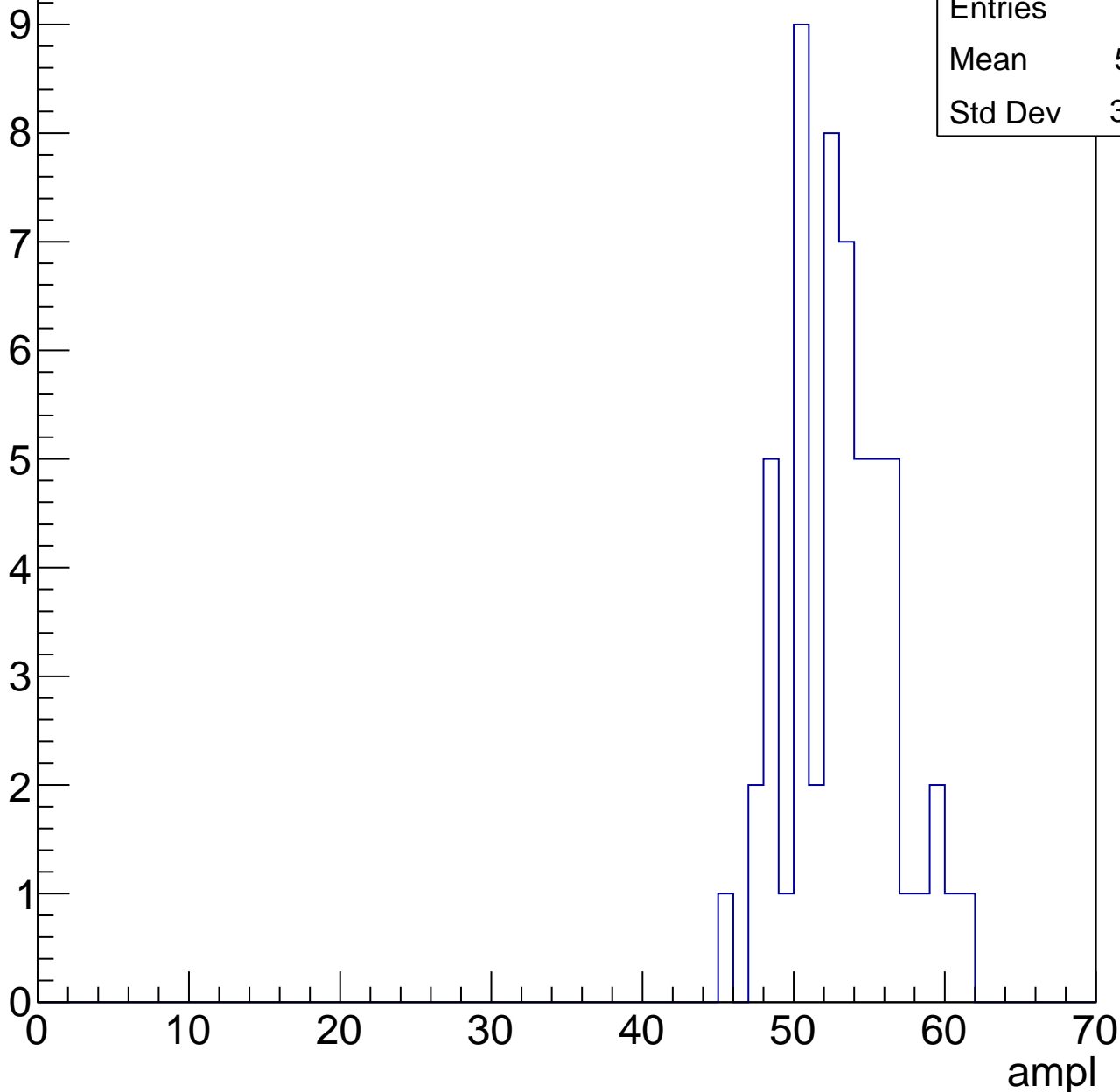


# B1L103S, U25-ch58, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

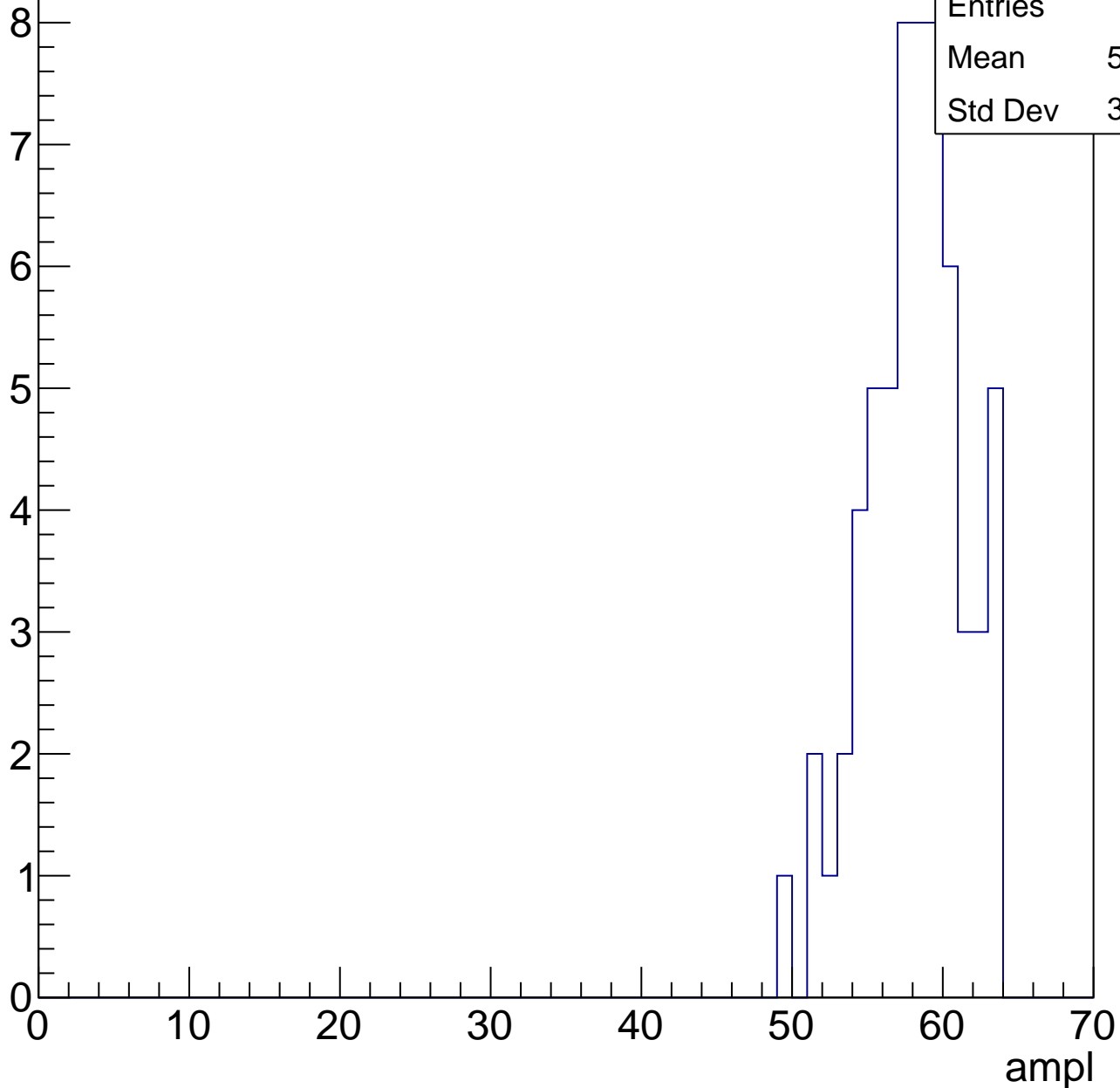
Entries	56
Mean	52.61
Std Dev	3.437



# B1L103S, U25-ch58, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



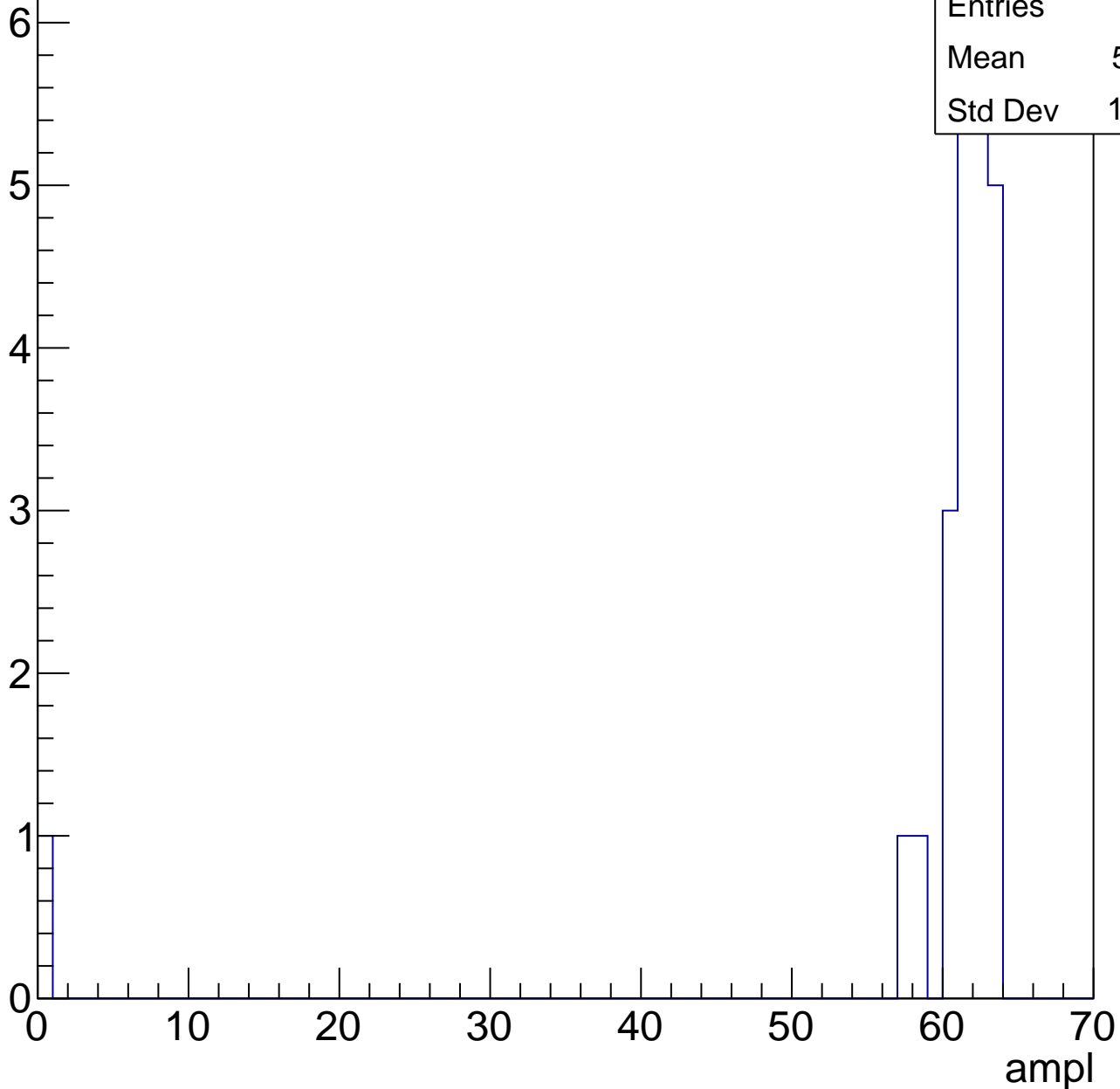
Entries	61
Mean	57.64
Std Dev	3.204

# B1L103S, U25-ch58, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	23
Mean	58.61
Std Dev	12.59





# B1L103S, U25-ch58, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	20
Mean	3.1
Std Dev	13.51

Entry

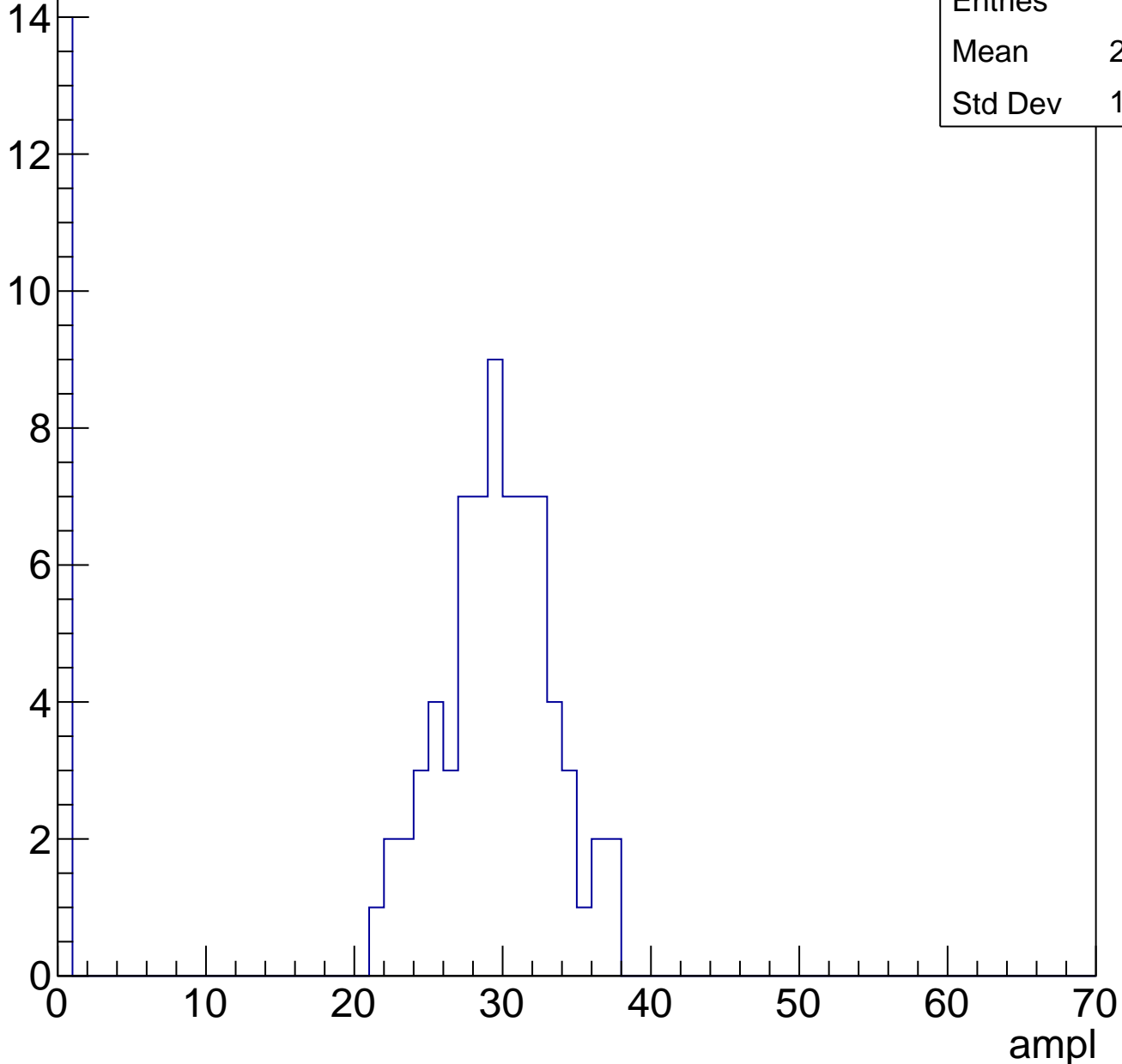


# B1L103S, U25-ch59, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	85
Mean	24.39
Std Dev	11.32

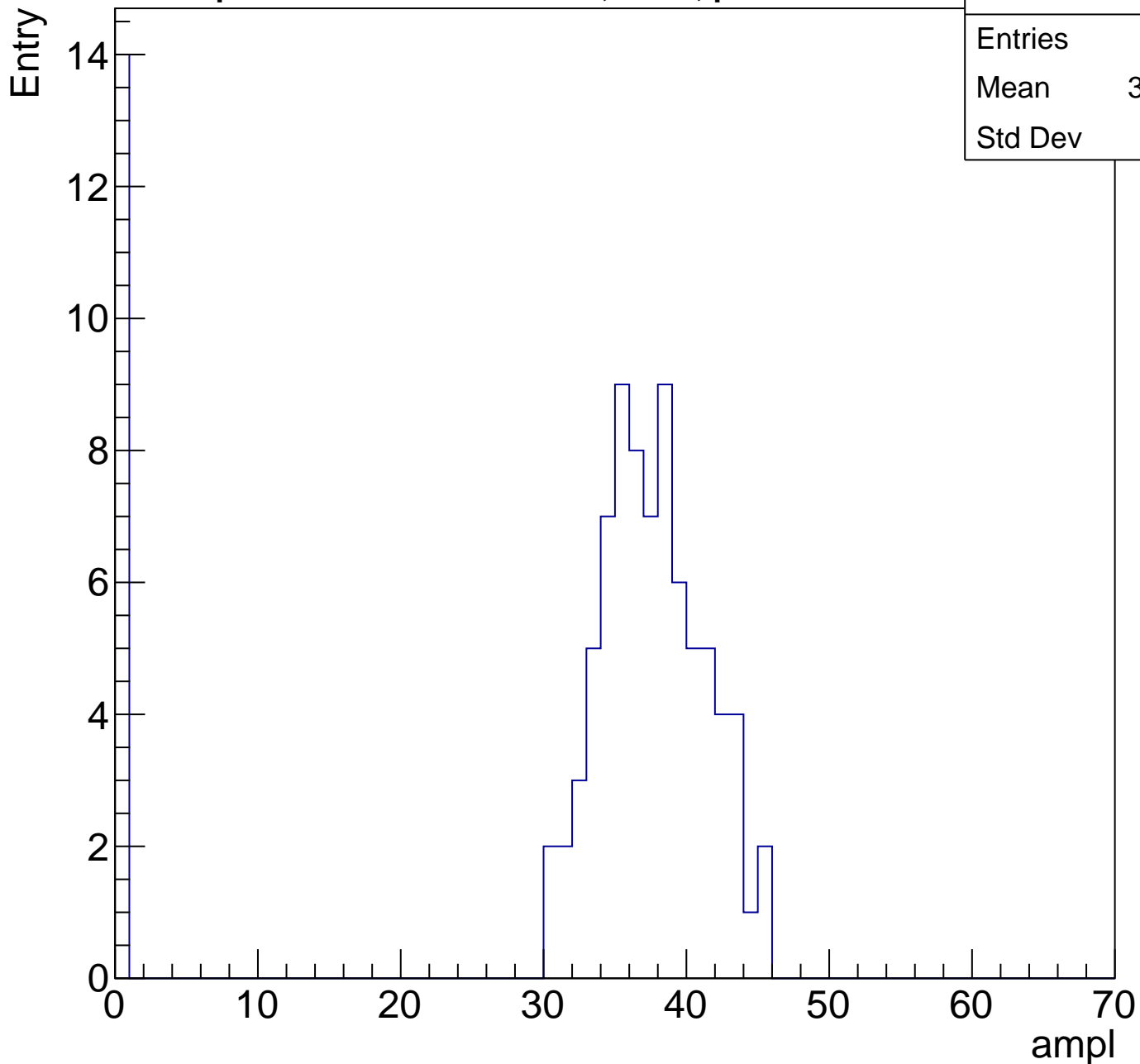
Entry



# B1L103S, U25-ch59, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

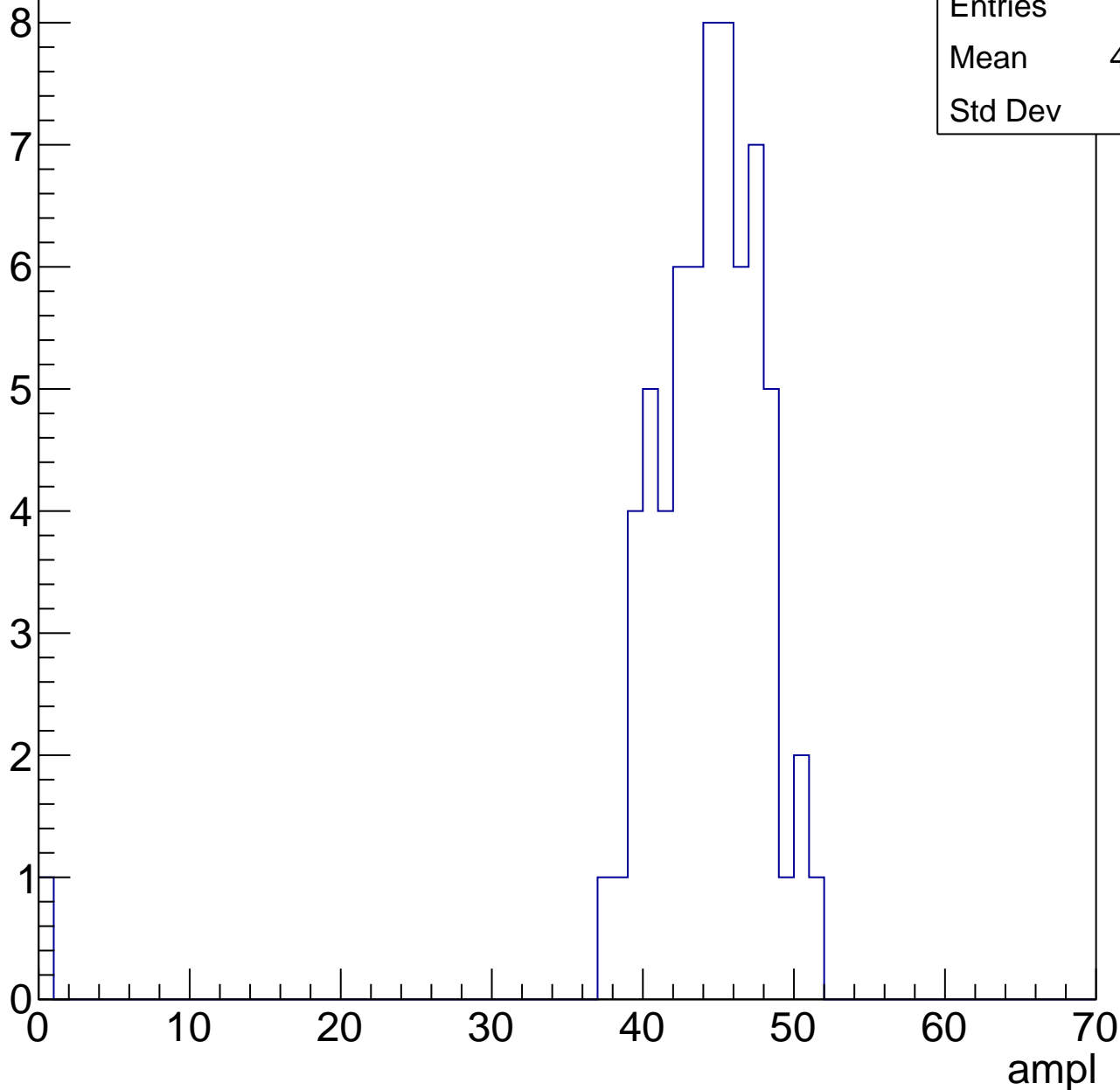
Entries	93
Mean	31.59
Std Dev	13.7



# B1L103S, U25-ch59, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

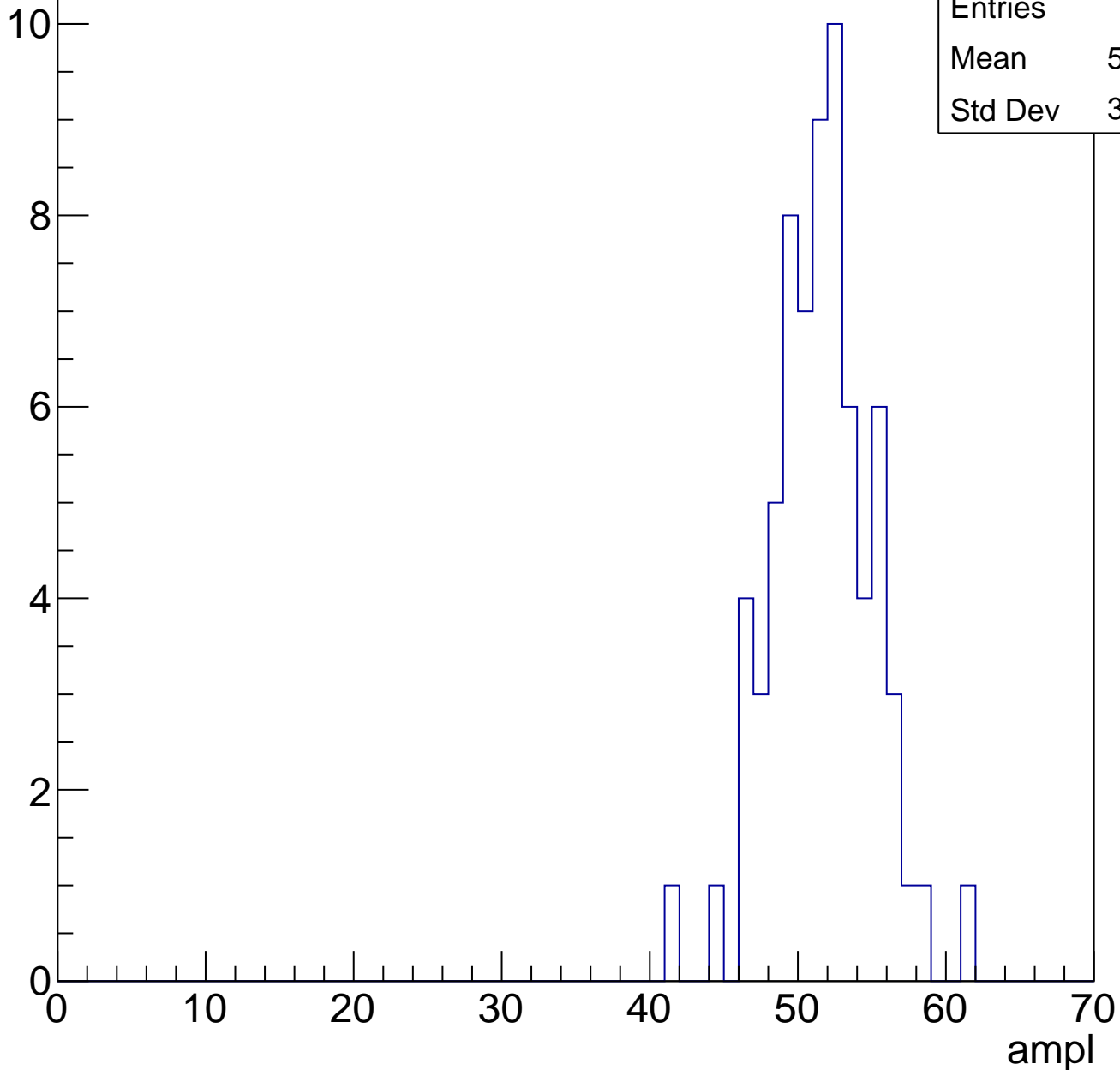


# B1L103S, U25-ch59, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	70
Mean	51.13
Std Dev	3.393

Entry

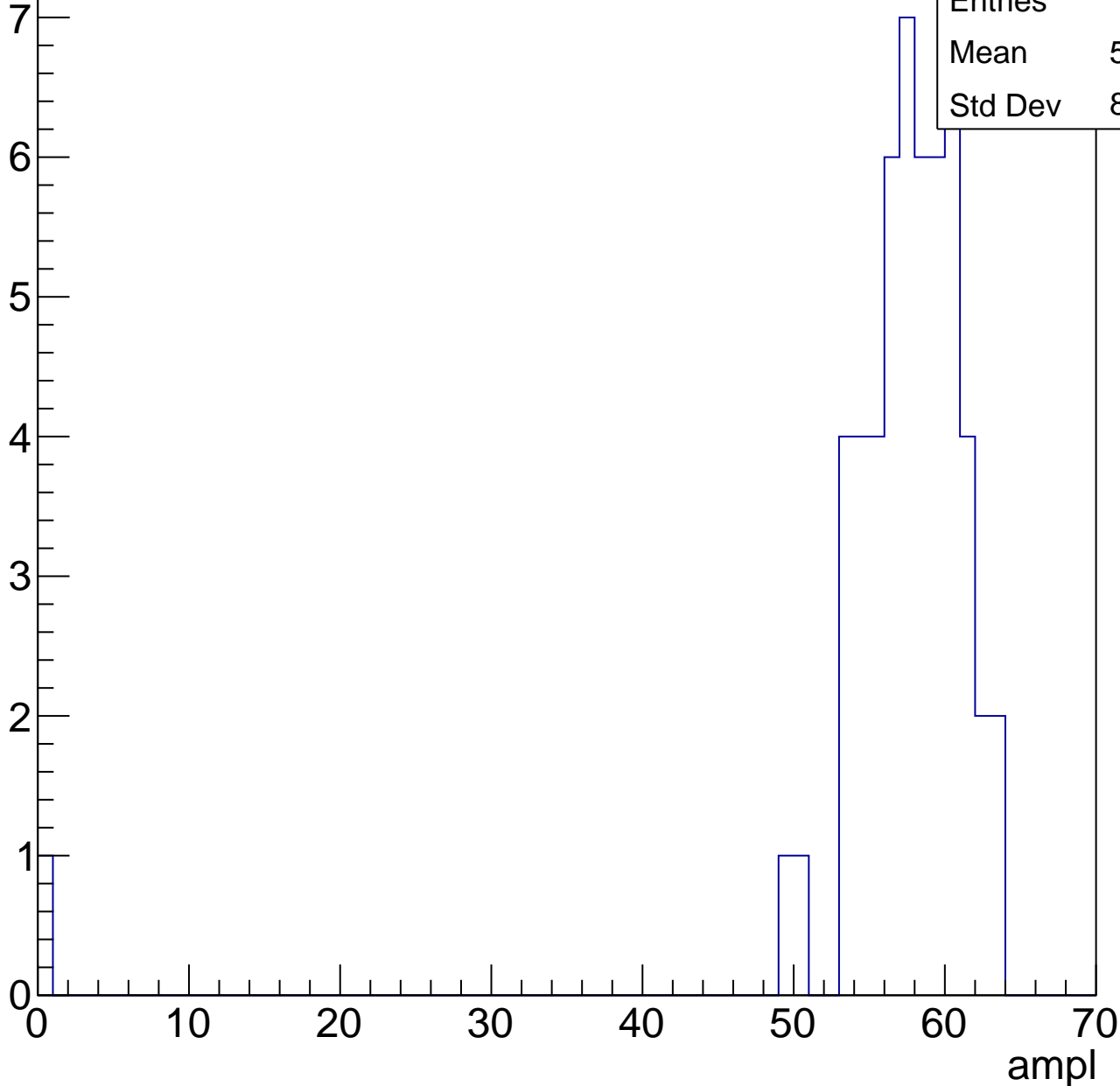


# B1L103S, U25-ch59, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	55
Mean	56.33
Std Dev	8.244

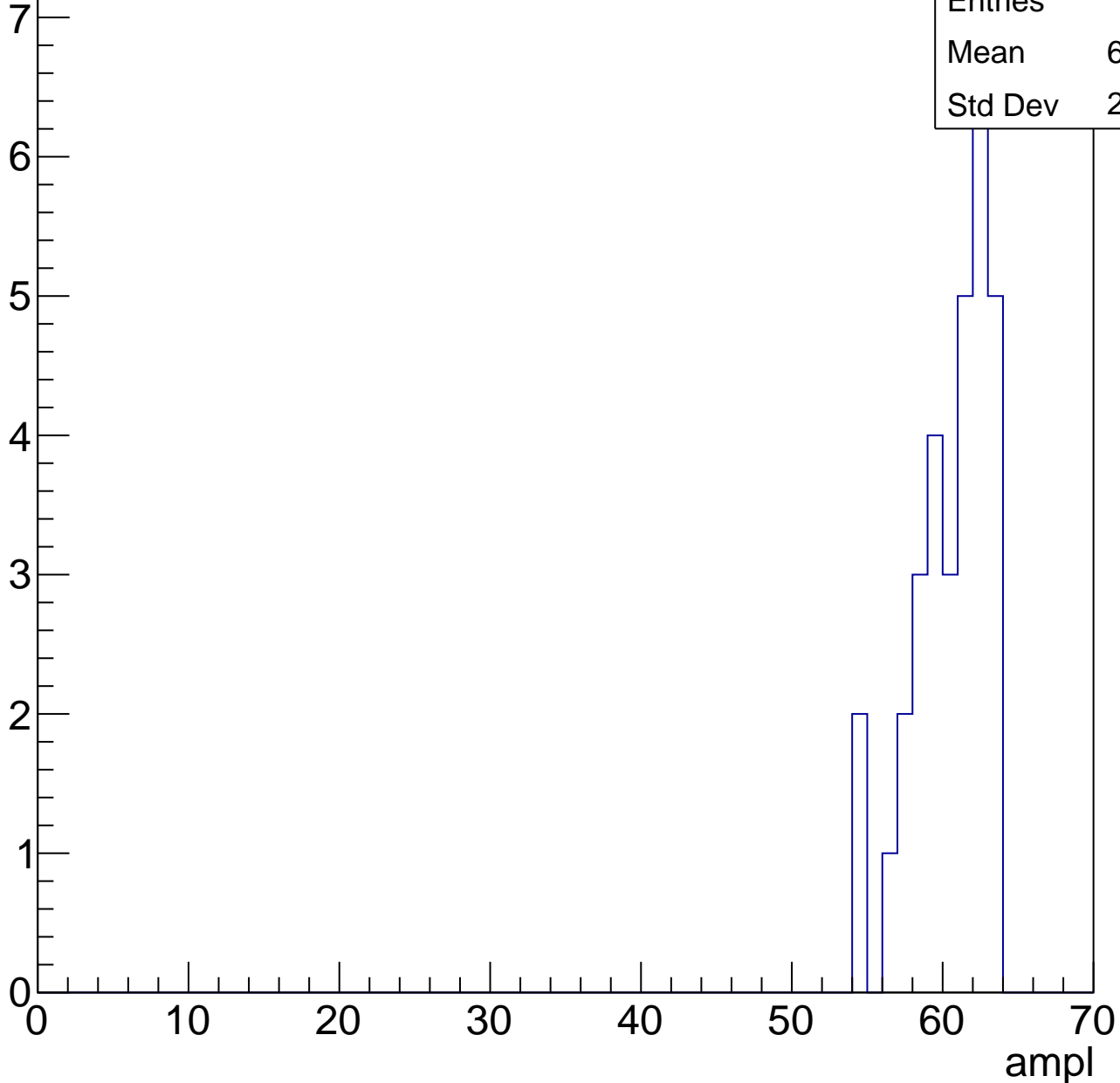


# B1L103S, U25-ch59, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	32
Mean	60.06
Std Dev	2.499



# B1L103S, U25-ch59, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U25-ch59, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

# B1L103S, U25-ch60, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	103
Mean	24.67
Std Dev	9.198

Entry

10

8

6

4

2

0

0

10

20

30

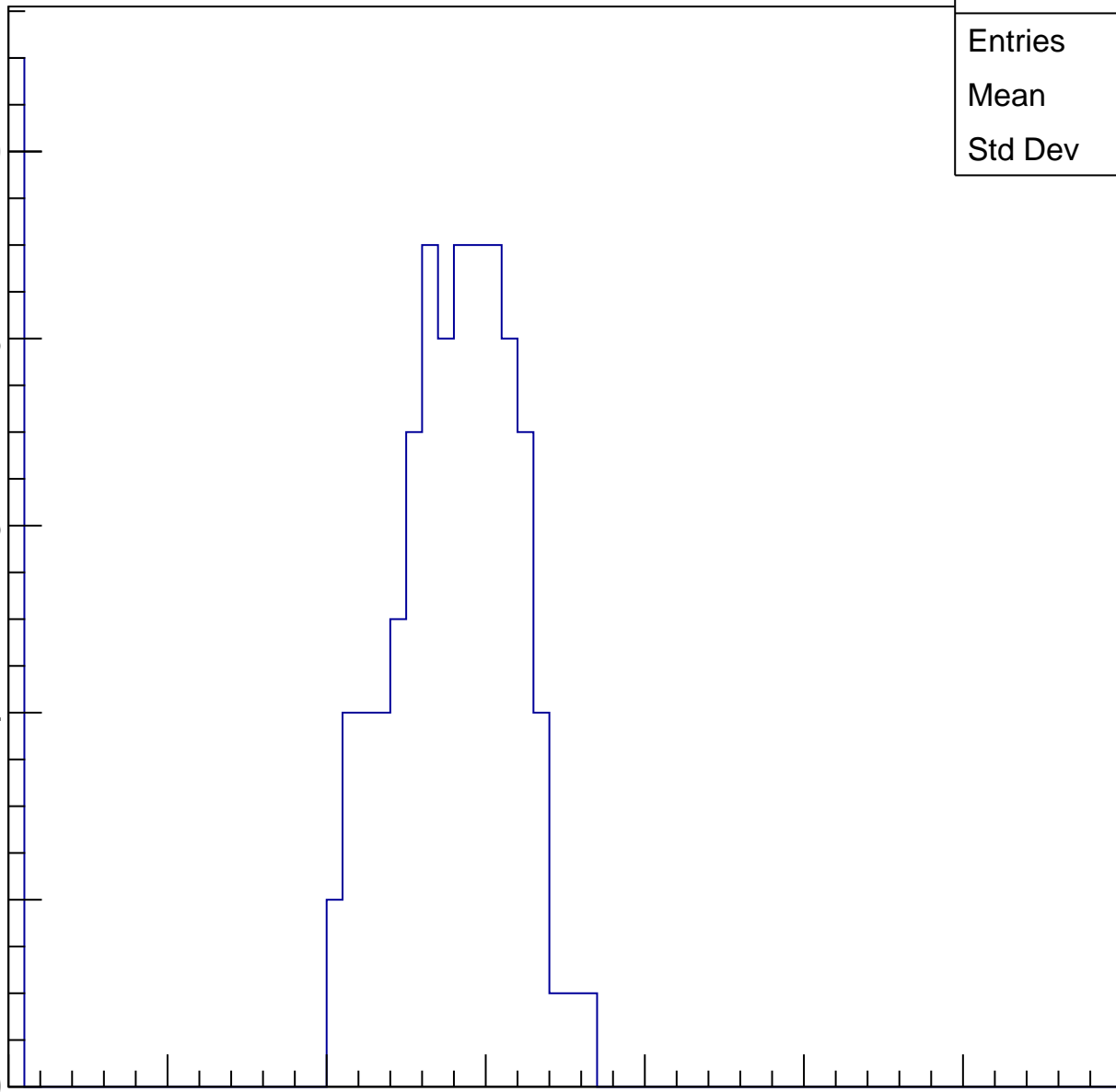
40

50

60

70

ampl

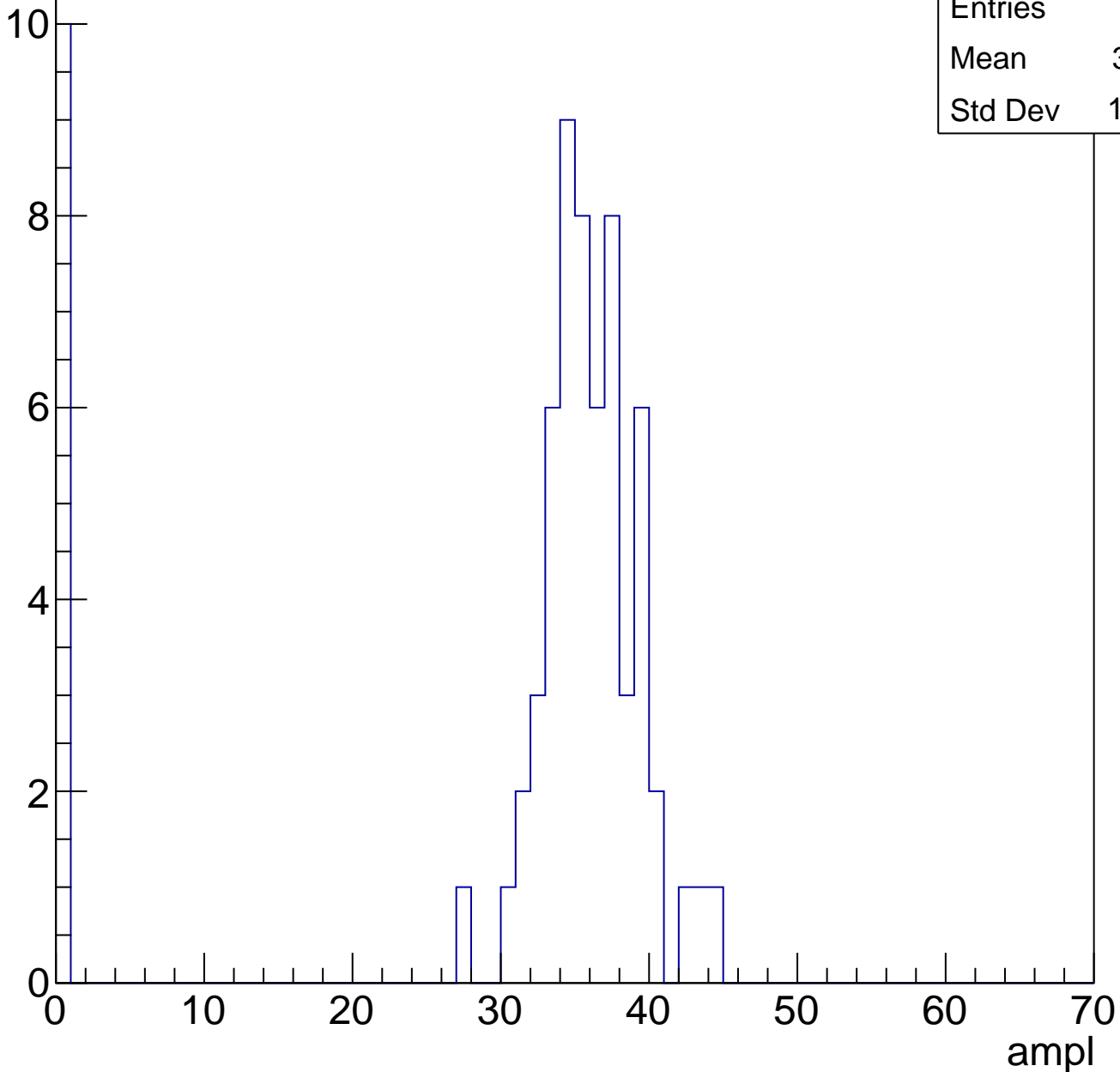


# B1L103S, U25-ch60, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	68
Mean	30.41
Std Dev	12.95

Entry

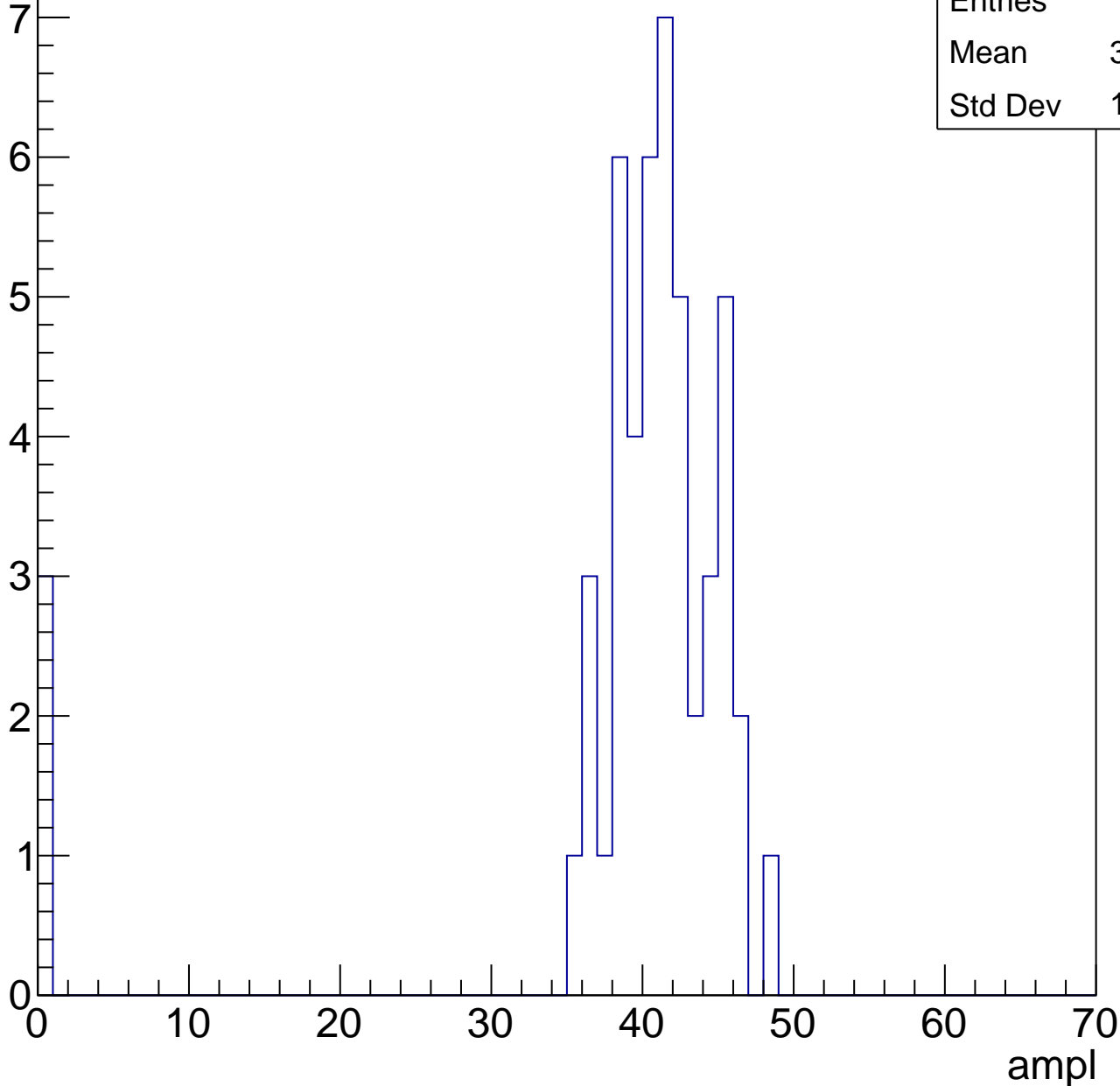


# B1L103S, U25-ch60, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	49
Mean	38.45
Std Dev	10.25

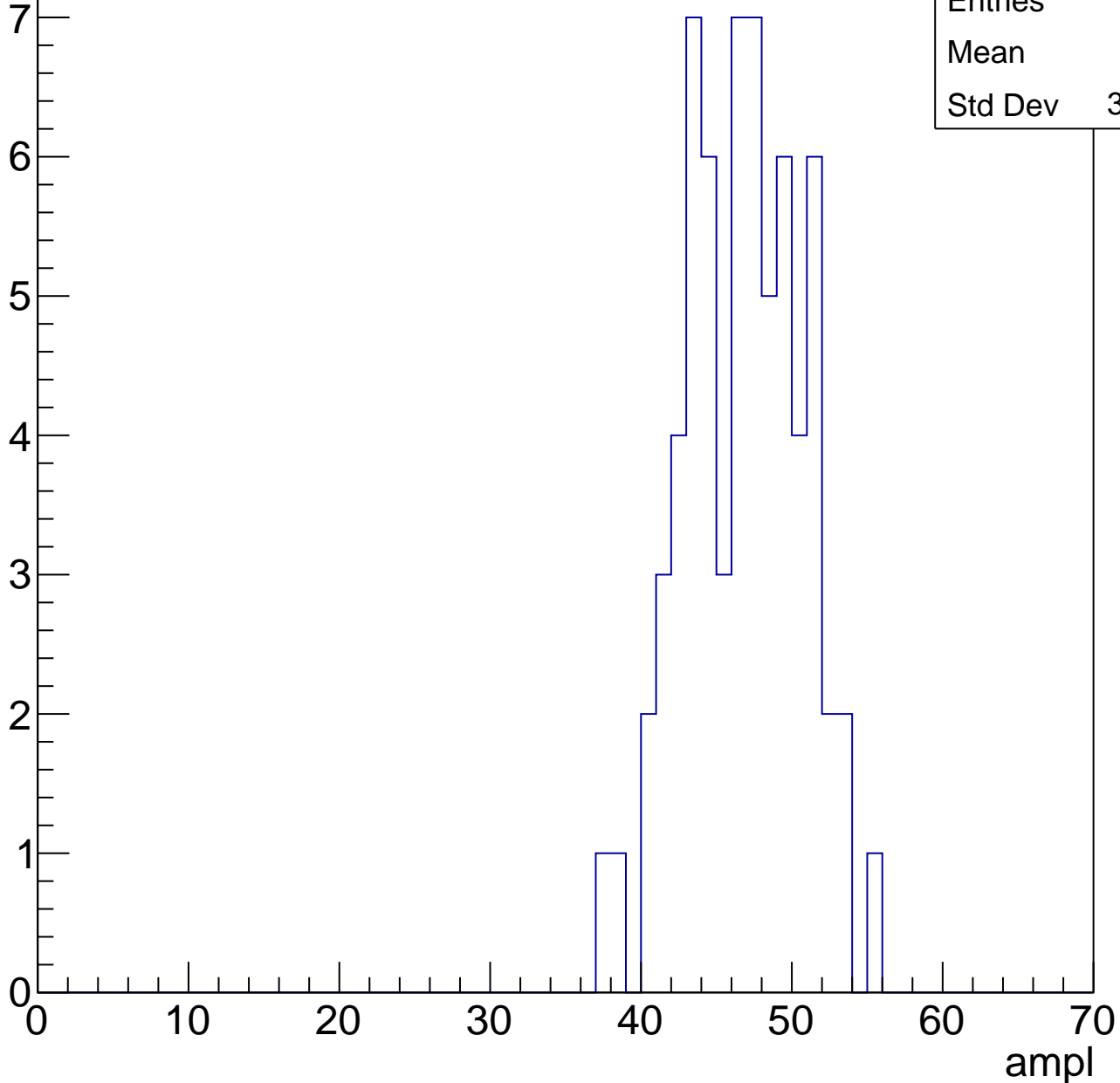


# B1L103S, U25-ch60, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	67
Mean	46.3
Std Dev	3.836

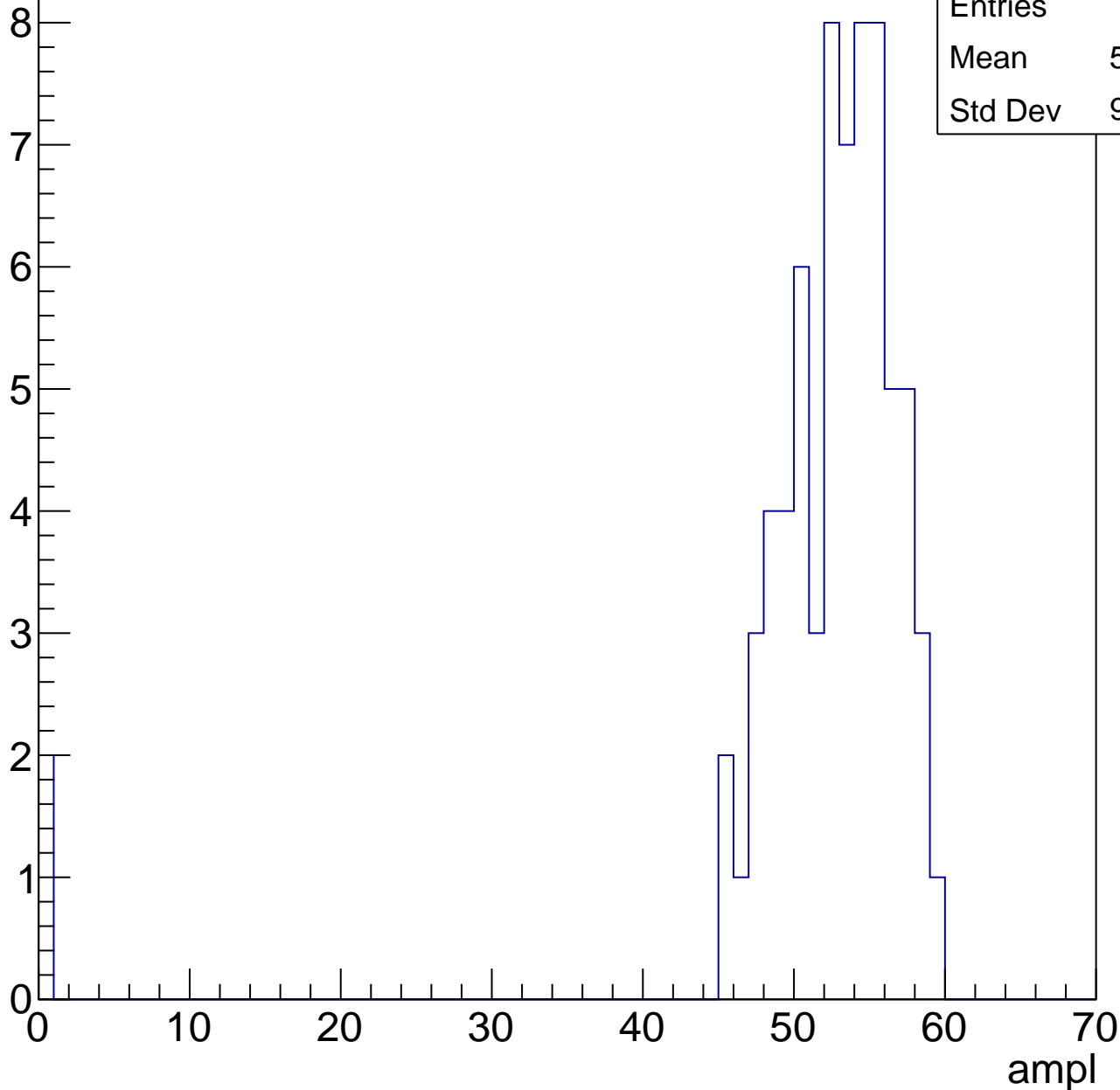


# B1L103S, U25-ch60, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	70
Mean	51.07
Std Dev	9.378

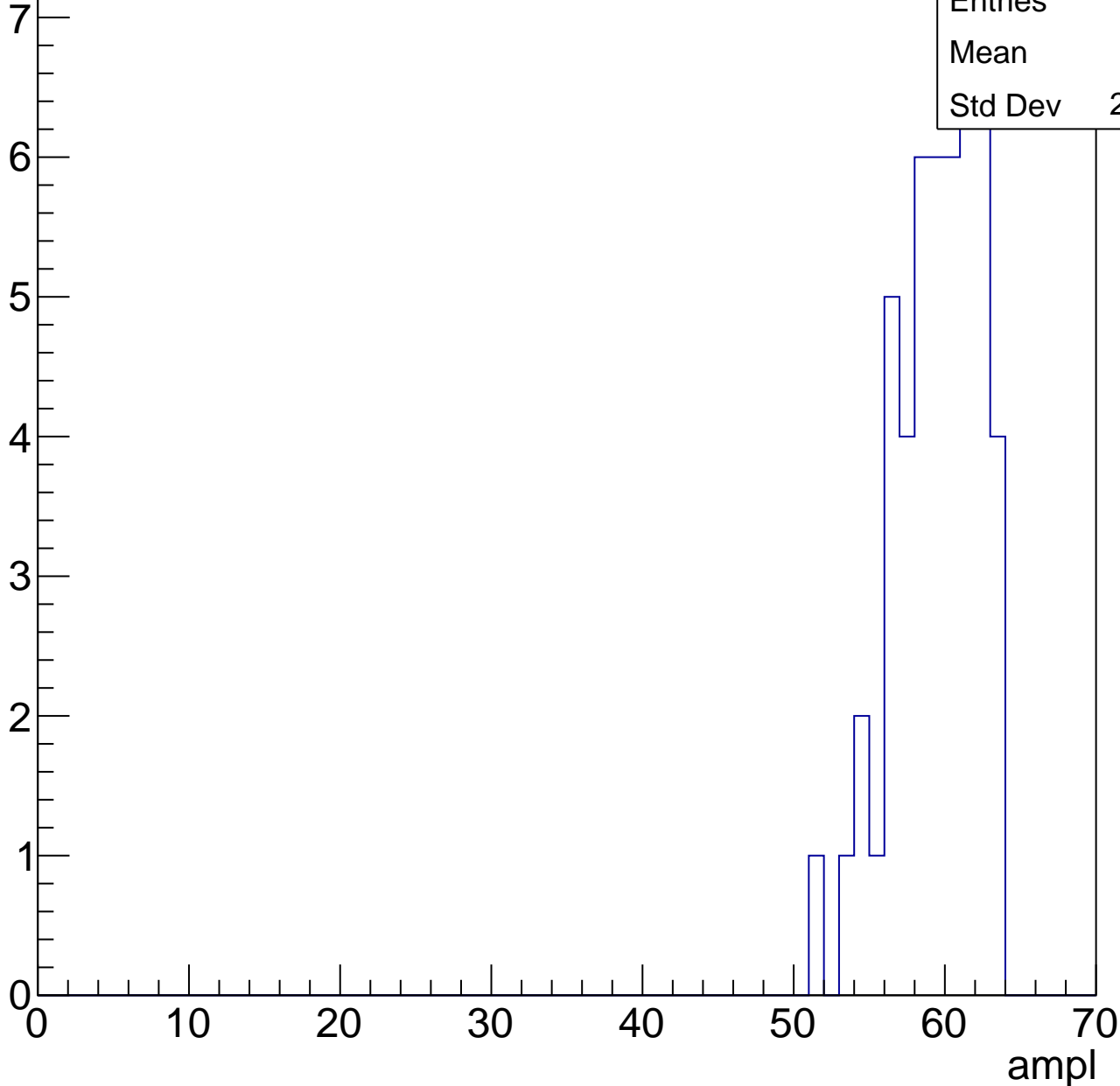


# B1L103S, U25-ch60, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	50
Mean	59
Std Dev	2.807

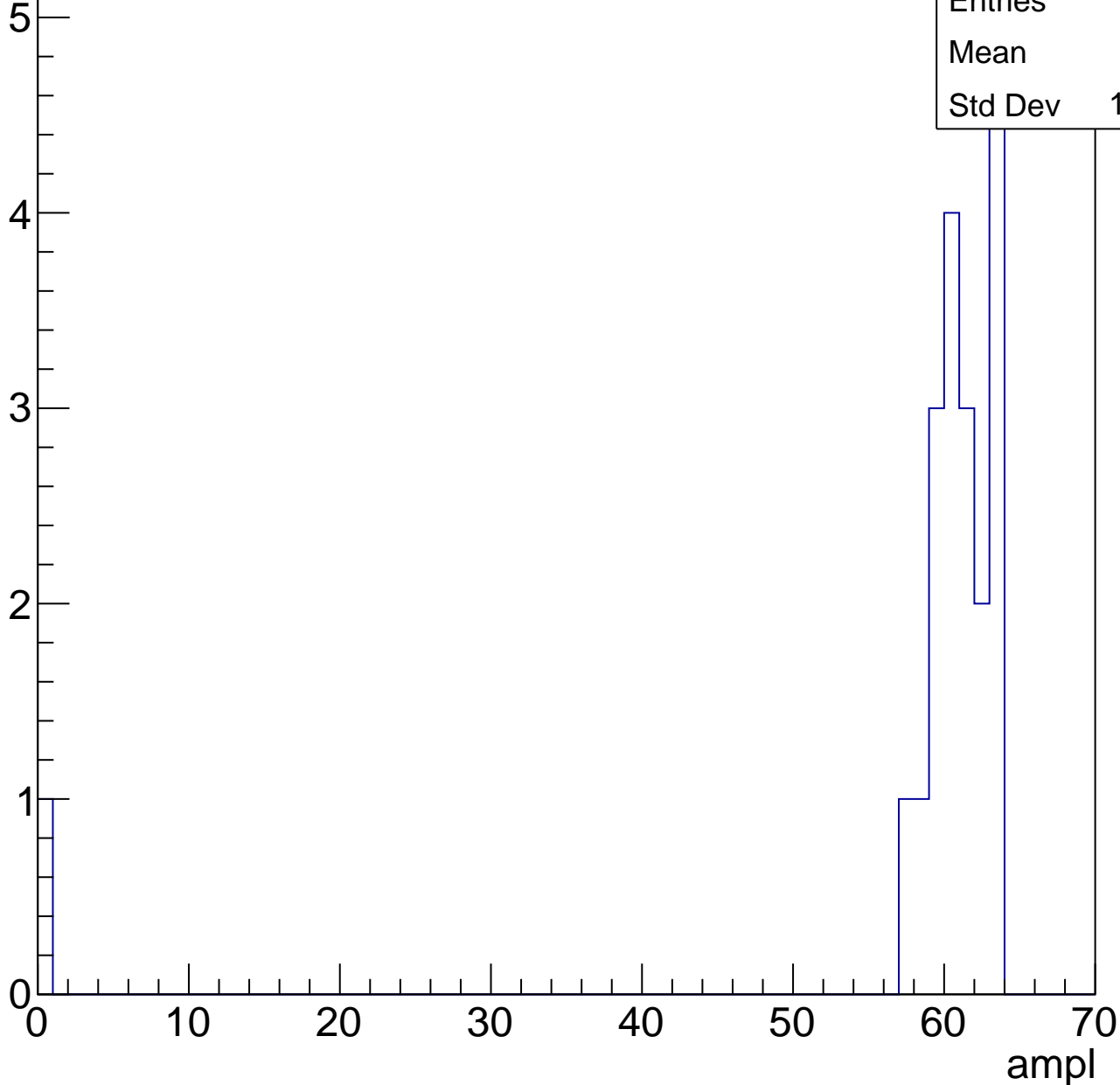


# B1L103S, U25-ch60, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	20
Mean	57.7
Std Dev	13.35





# B1L103S, U25-ch60, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	21
Mean	5.952
Std Dev	18.35

Entry

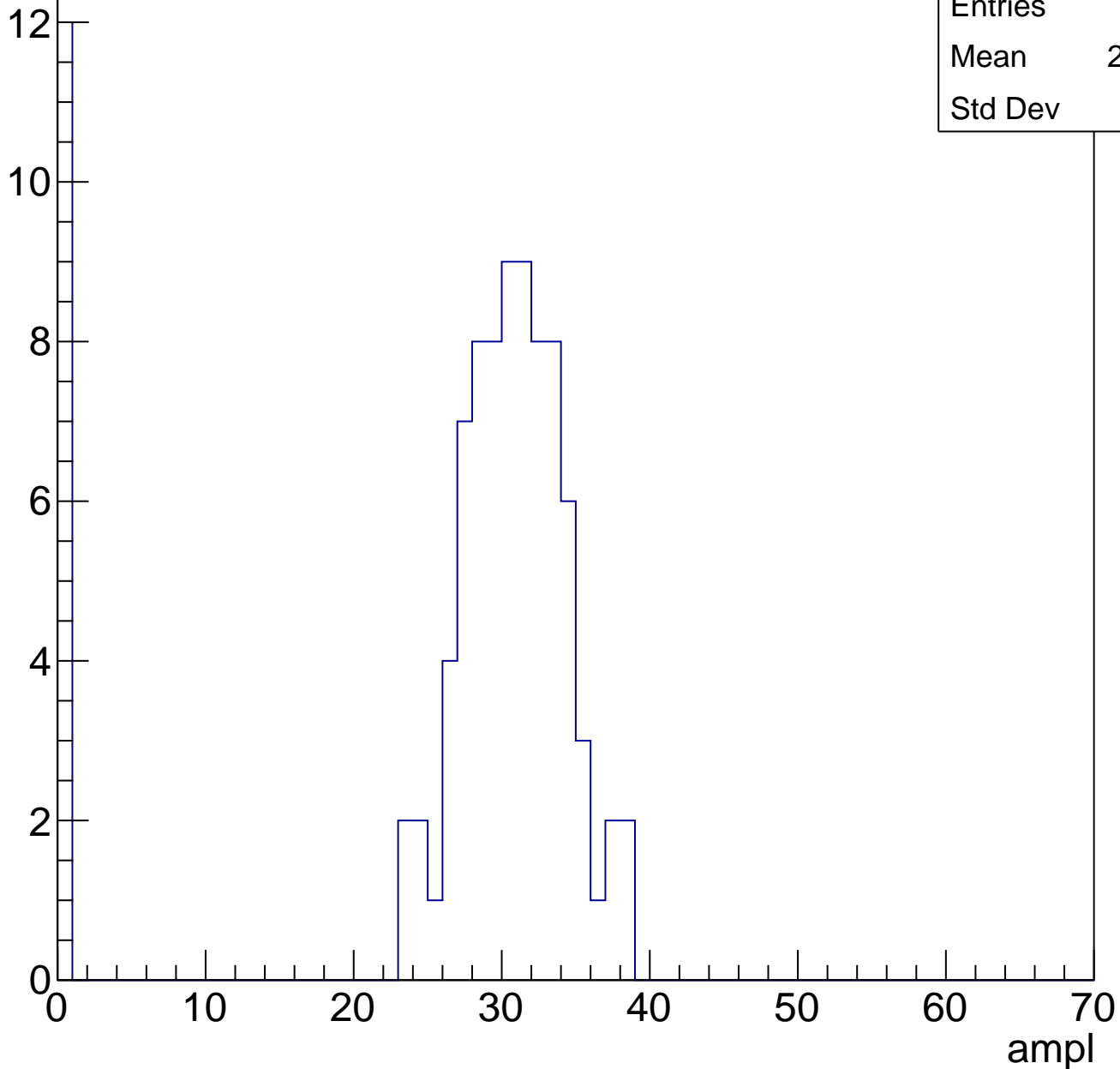


# B1L103S, U25-ch61, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	92
Mean	26.43
Std Dev	10.7

Entry

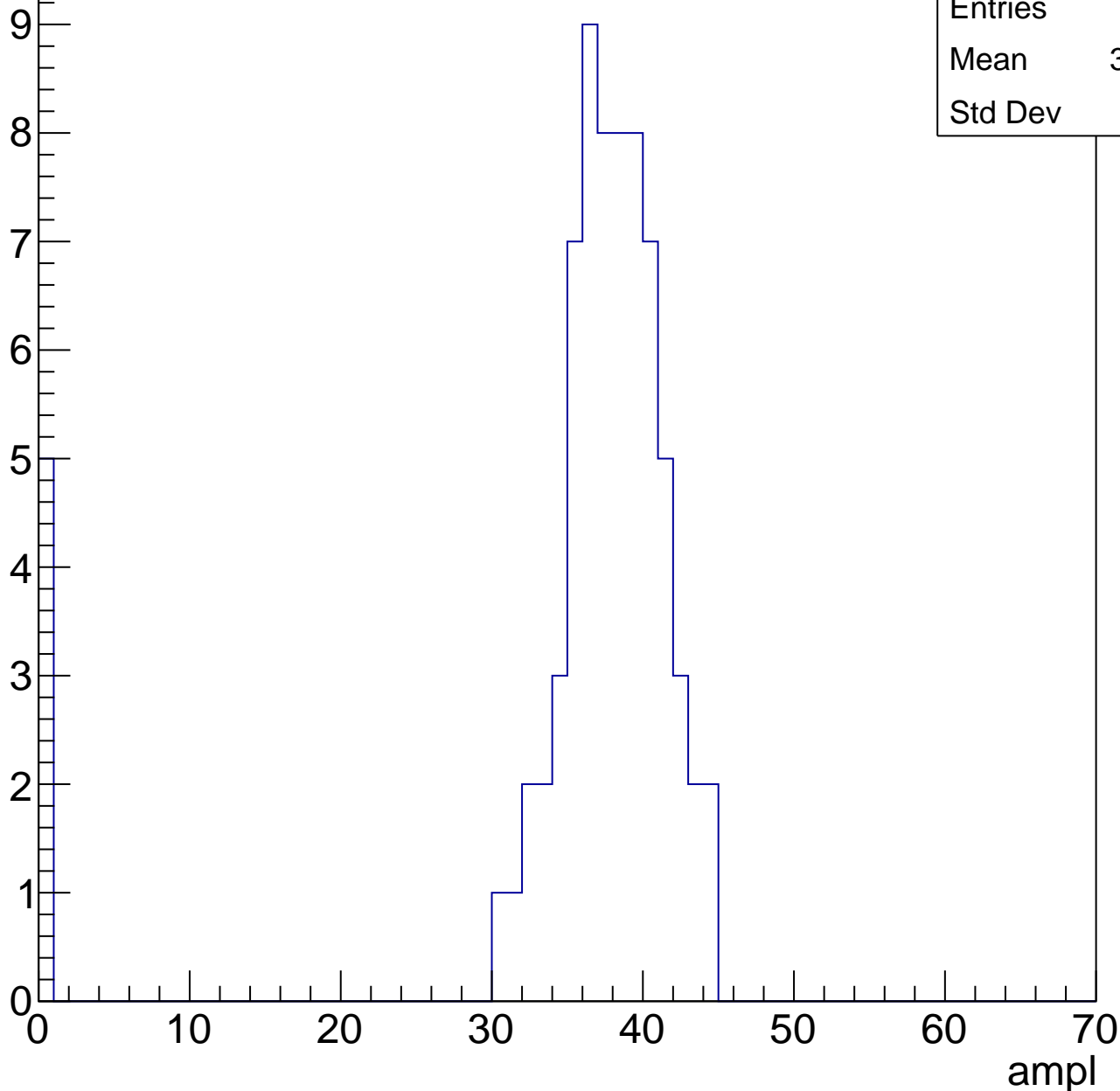


# B1L103S, U25-ch61, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	73
Mean	35.05
Std Dev	9.95

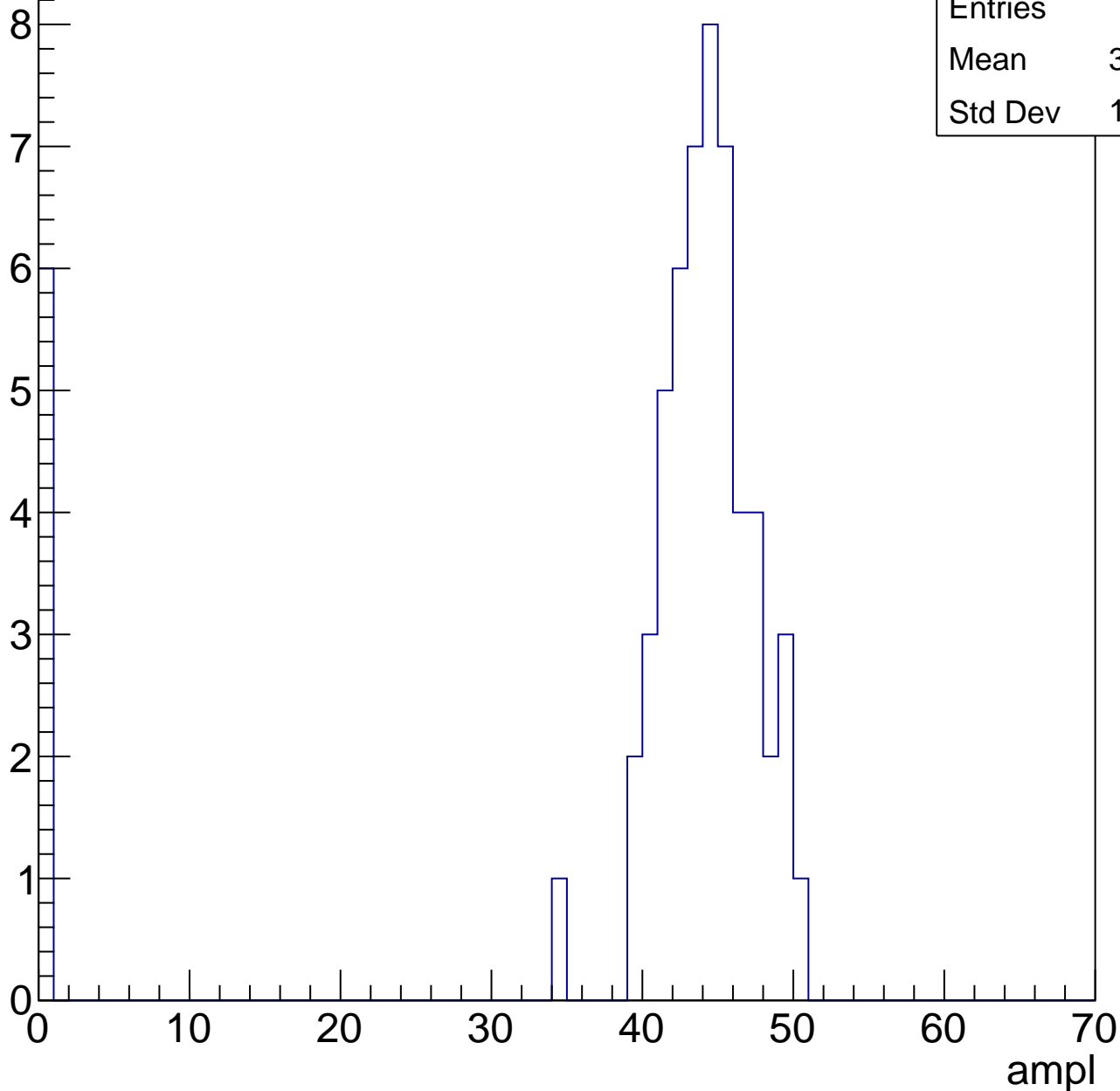


# B1L103S, U25-ch61, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

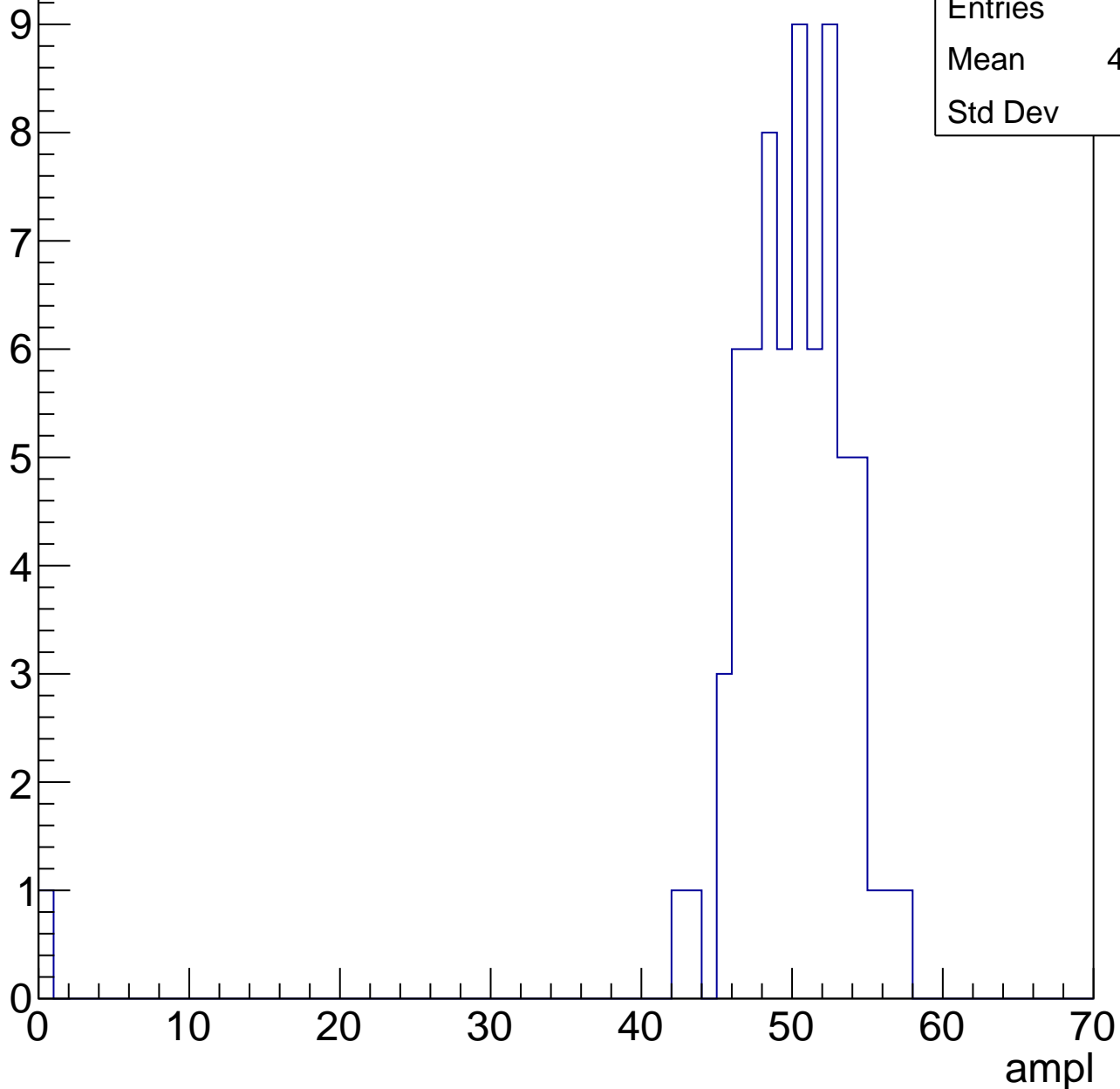
Entries	59
Mean	39.36
Std Dev	13.54



# B1L103S, U25-ch61, adc3

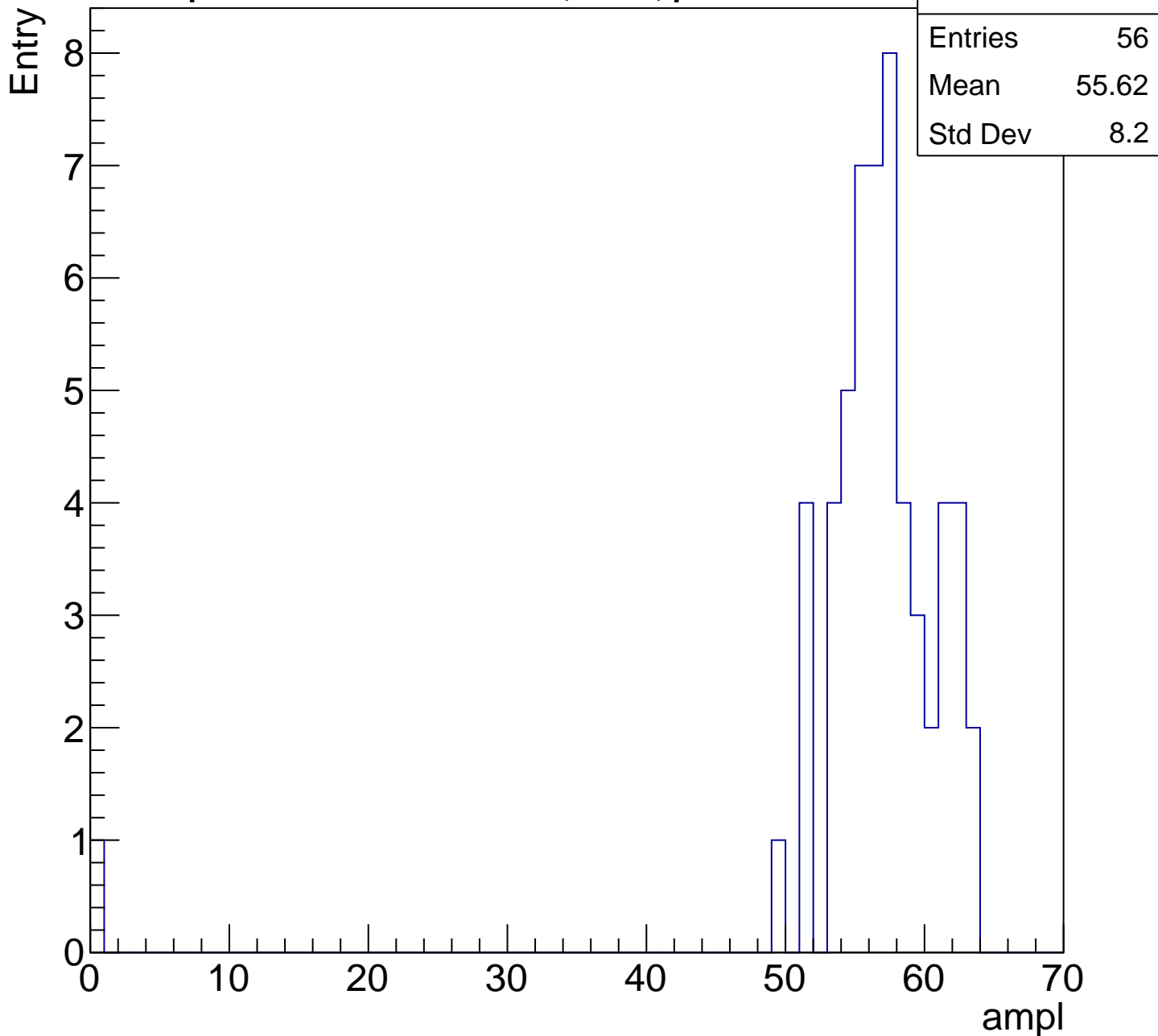
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U25-ch61, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

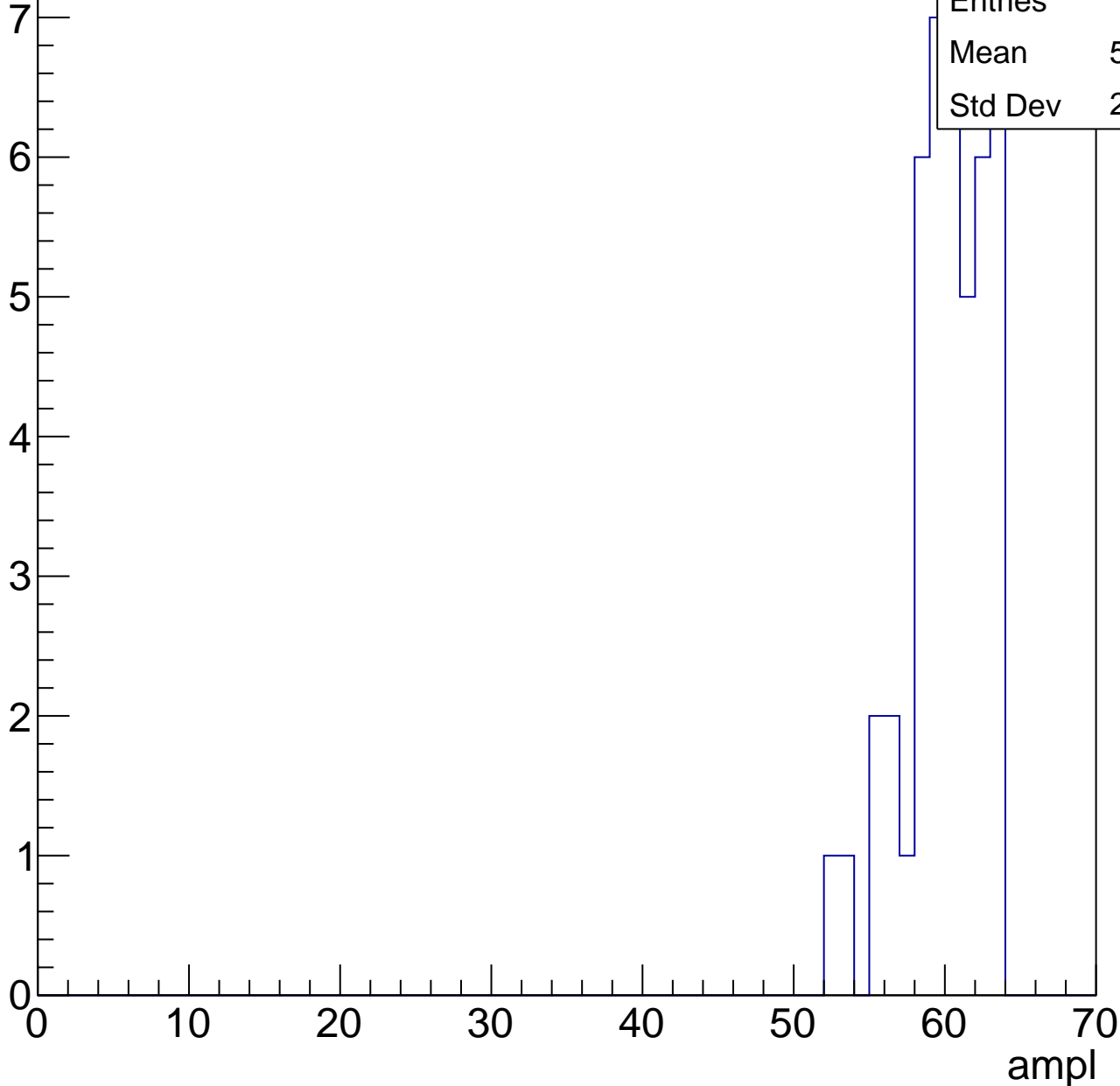


# B1L103S, U25-ch61, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

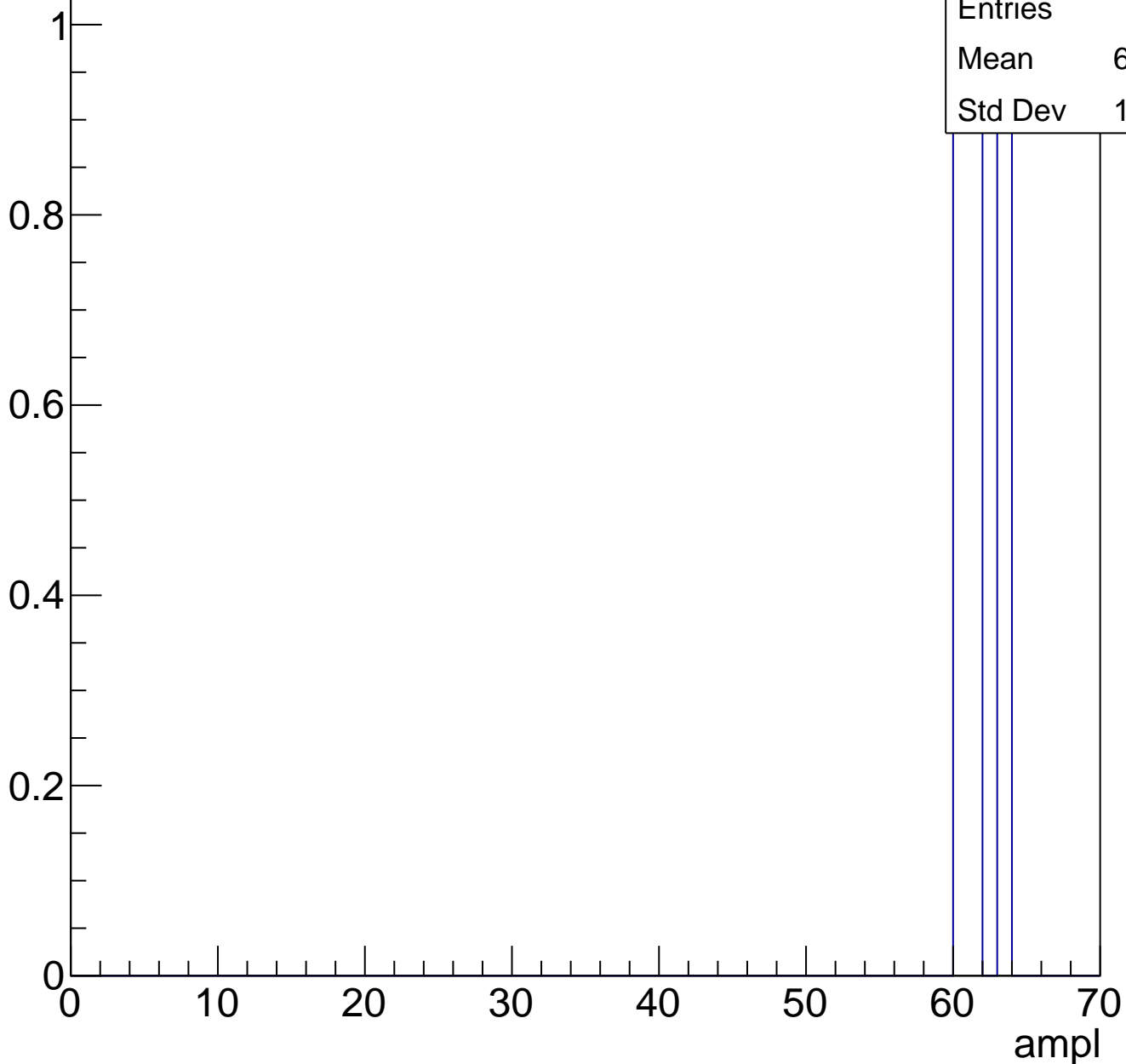
Entries	45
Mean	59.62
Std Dev	2.669



# B1L103S, U25-ch61, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U25-ch61, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

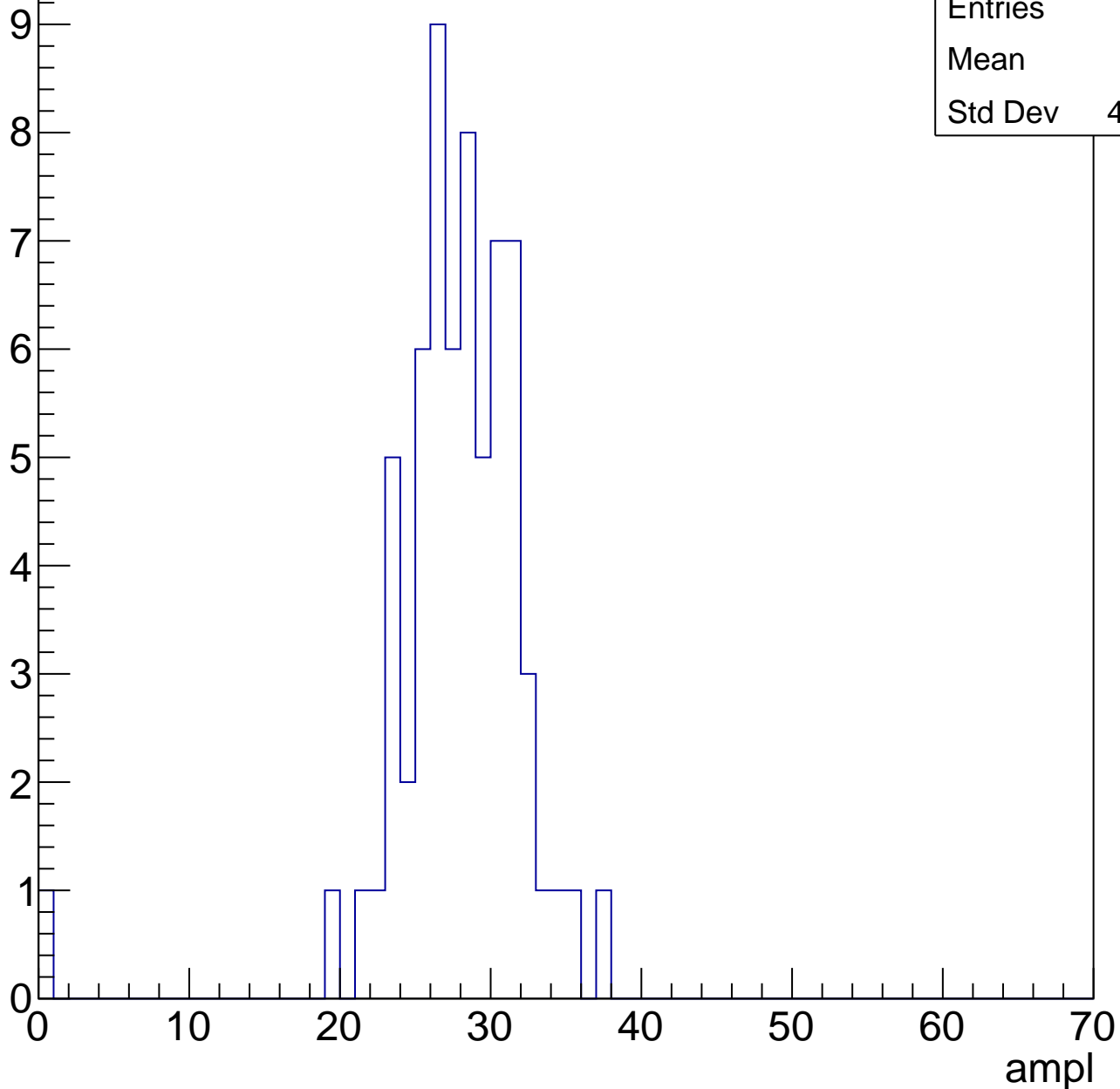
Entries	19
Mean	0
Std Dev	0

# B1L103S, U25-ch62, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

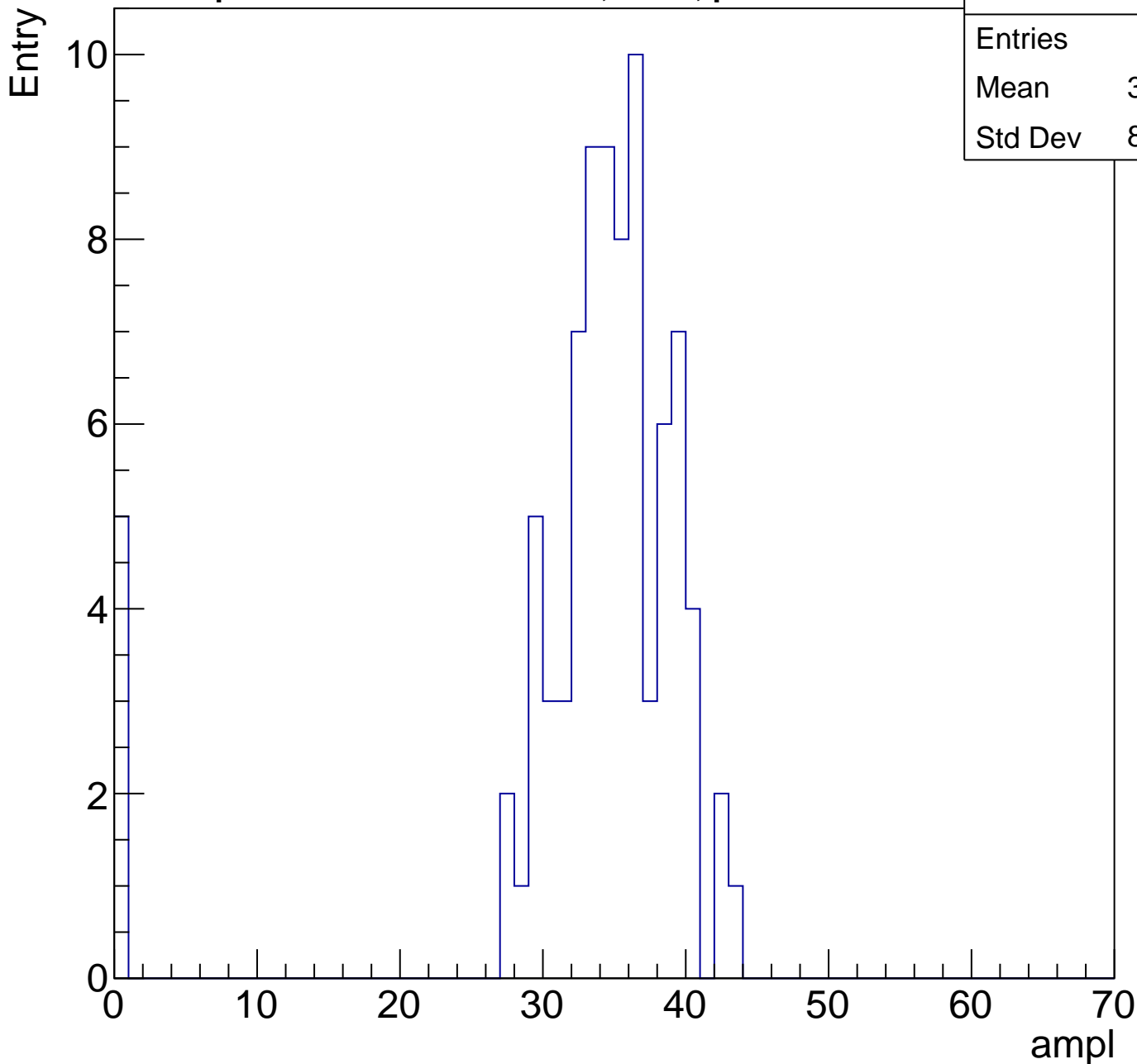
Entries	66
Mean	27.3
Std Dev	4.777



# B1L103S, U25-ch62, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	85
Mean	32.66
Std Dev	8.876

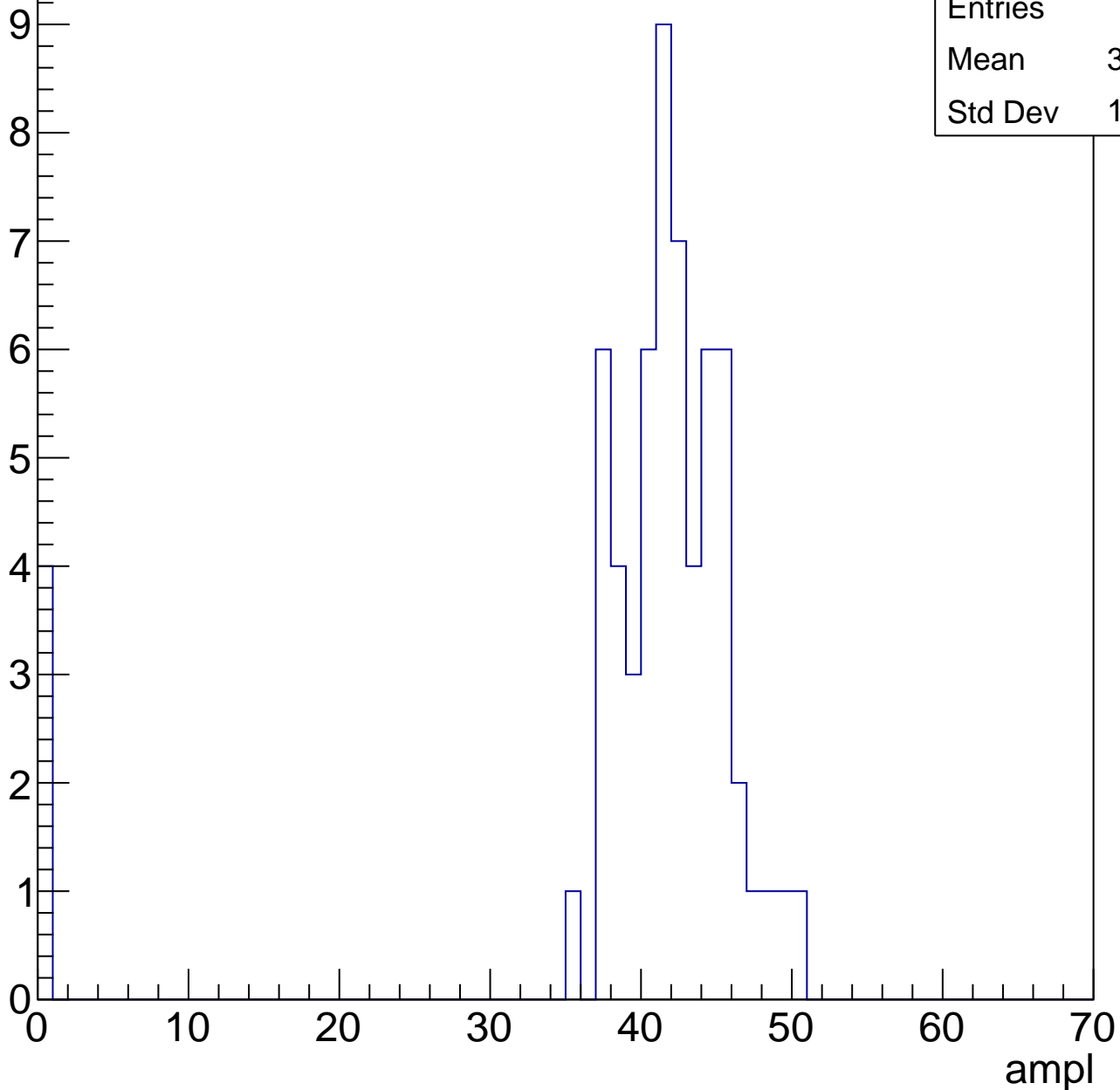


# B1L103S, U25-ch62, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	62
Mean	39.05
Std Dev	10.72

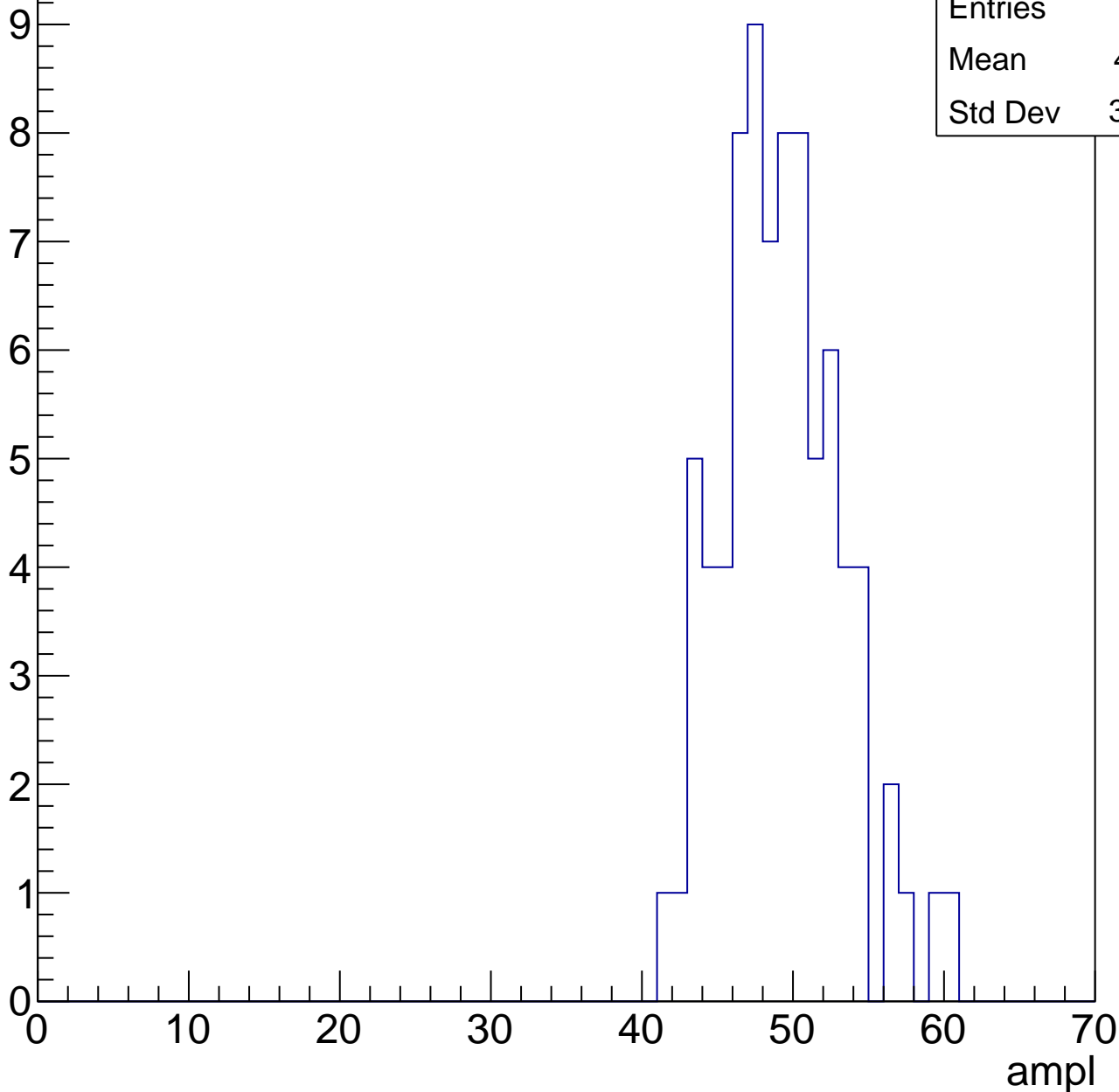


# B1L103S, U25-ch62, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	79
Mean	48.81
Std Dev	3.894

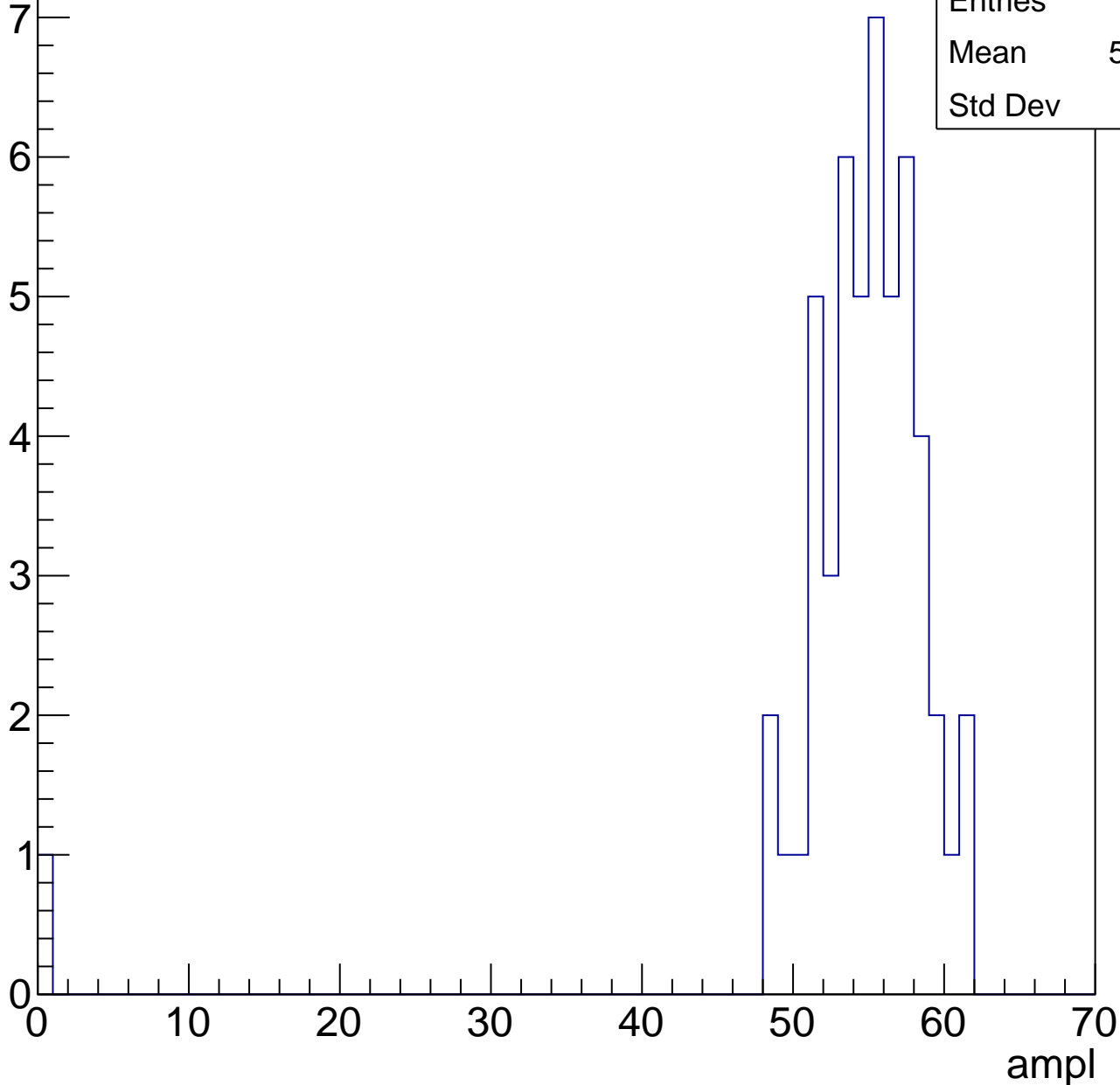


# B1L103S, U25-ch62, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	51
Mean	53.59
Std Dev	8.18



# B1L103S, U25-ch62, adc5

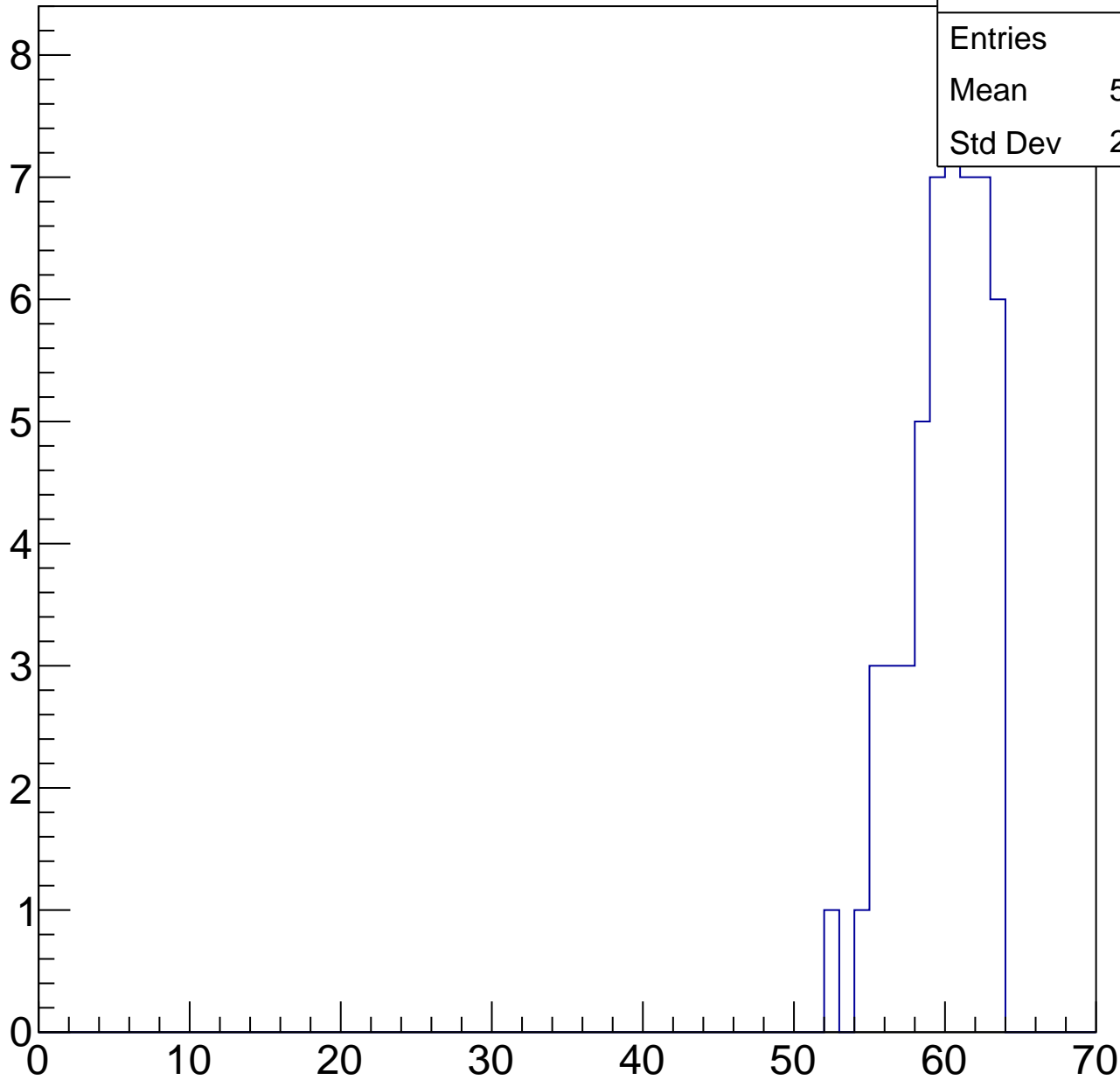
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	51
Mean	59.45
Std Dev	2.622

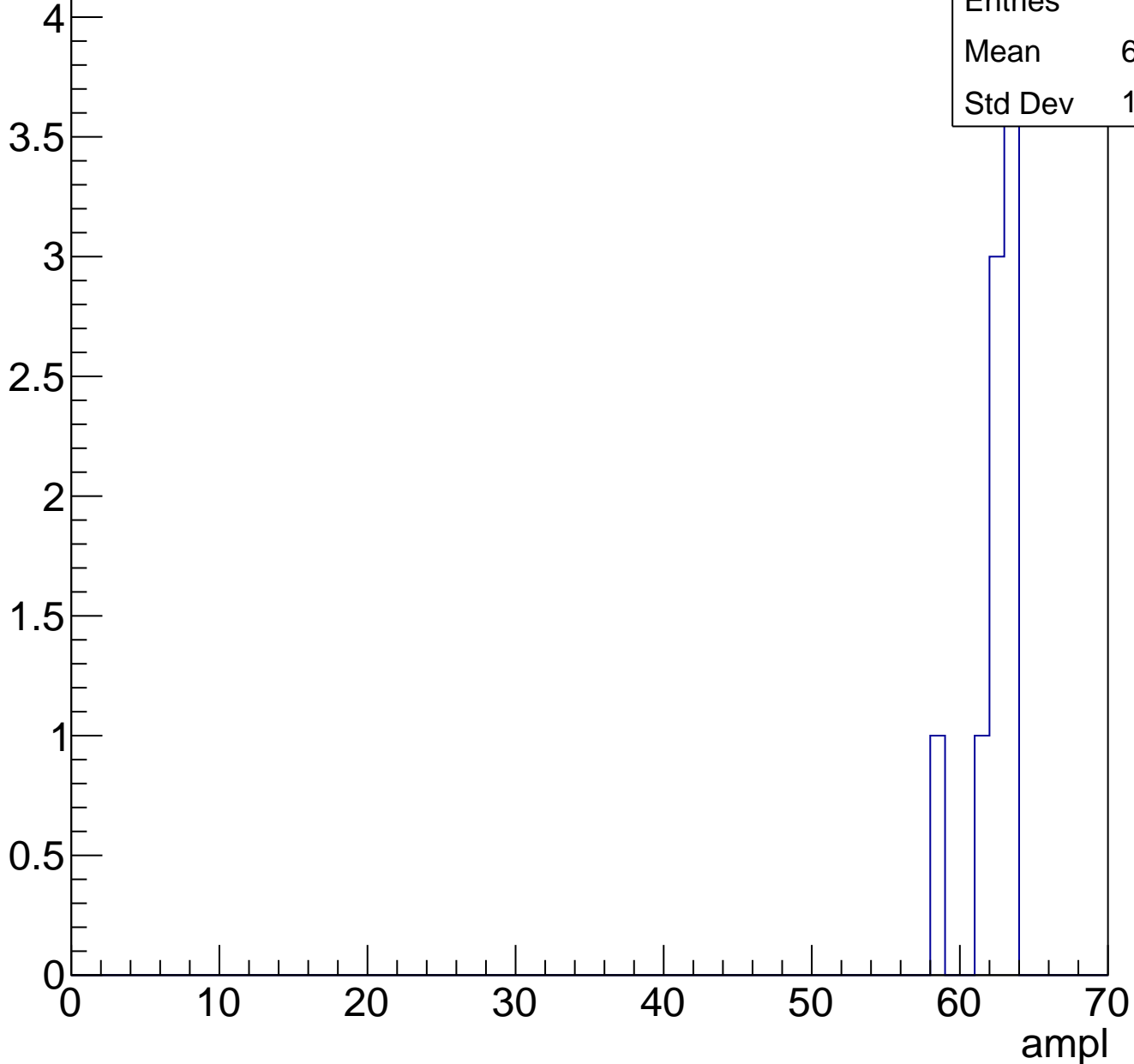
ampl



# B1L103S, U25-ch62, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U25-ch62, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

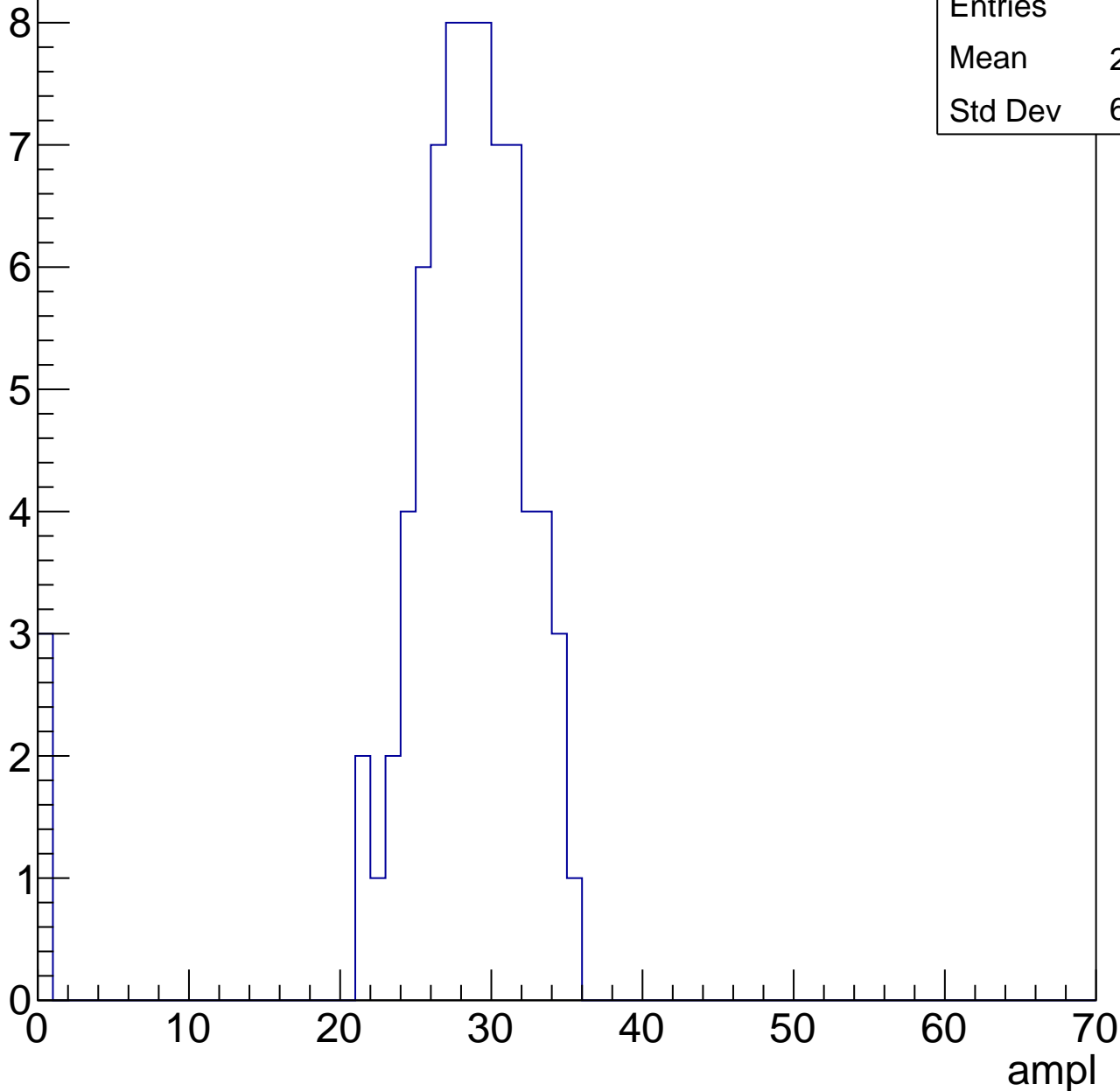


# B1L103S, U25-ch63, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	75
Mean	27.12
Std Dev	6.379

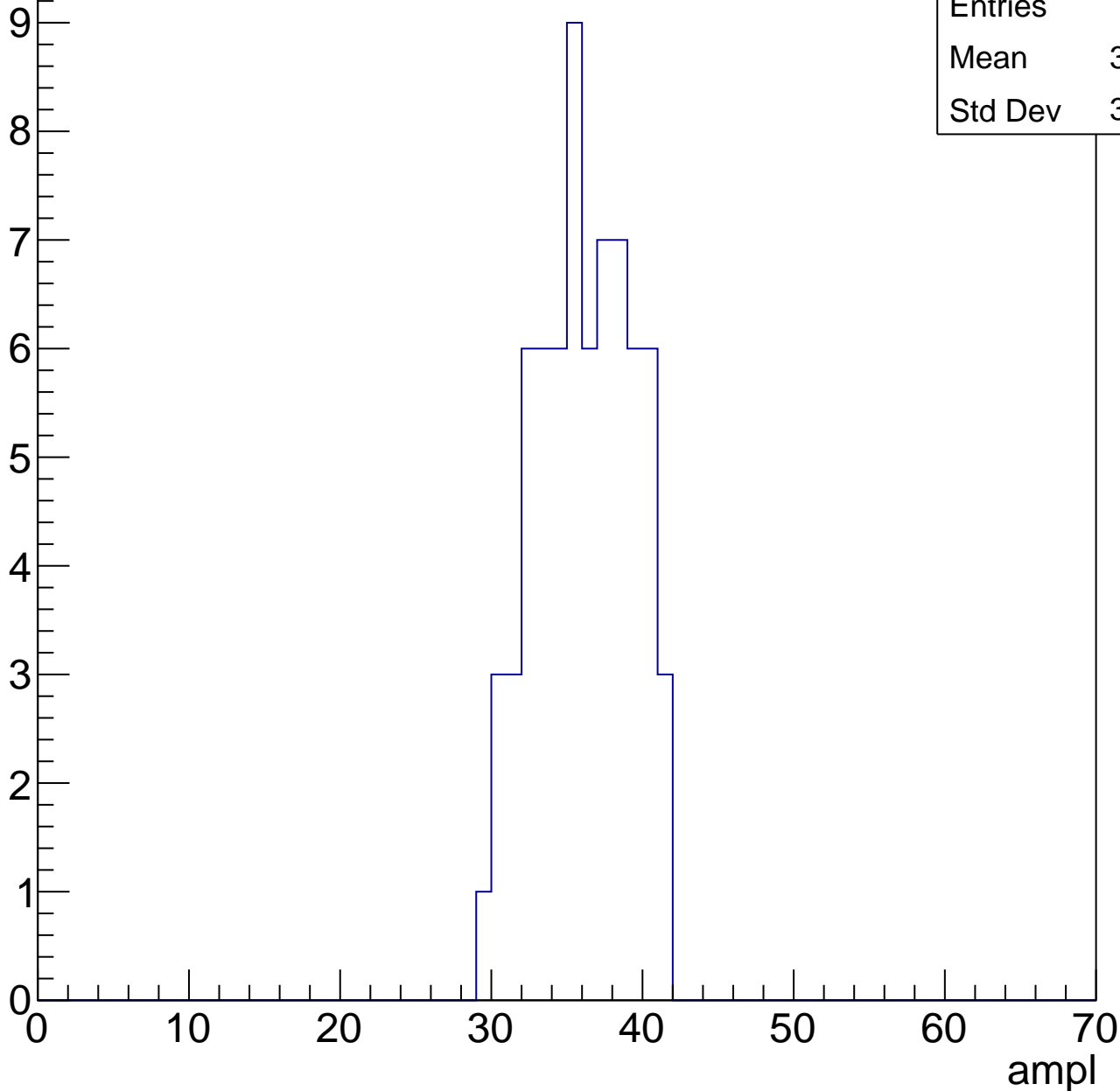


# B1L103S, U25-ch63, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

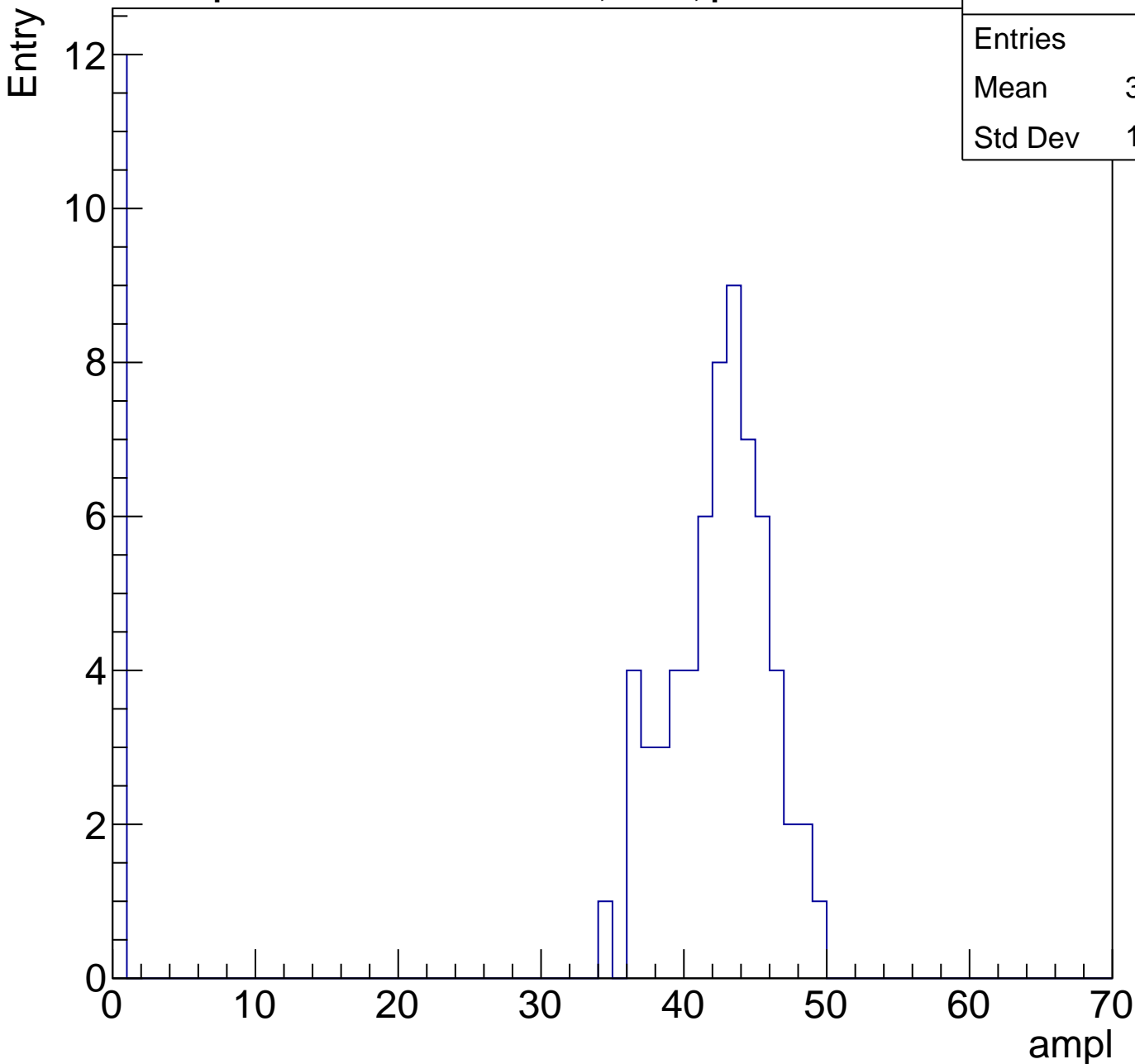
Entries	69
Mean	35.64
Std Dev	3.107



# B1L103S, U25-ch63, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	76
Mean	35.38
Std Dev	15.62

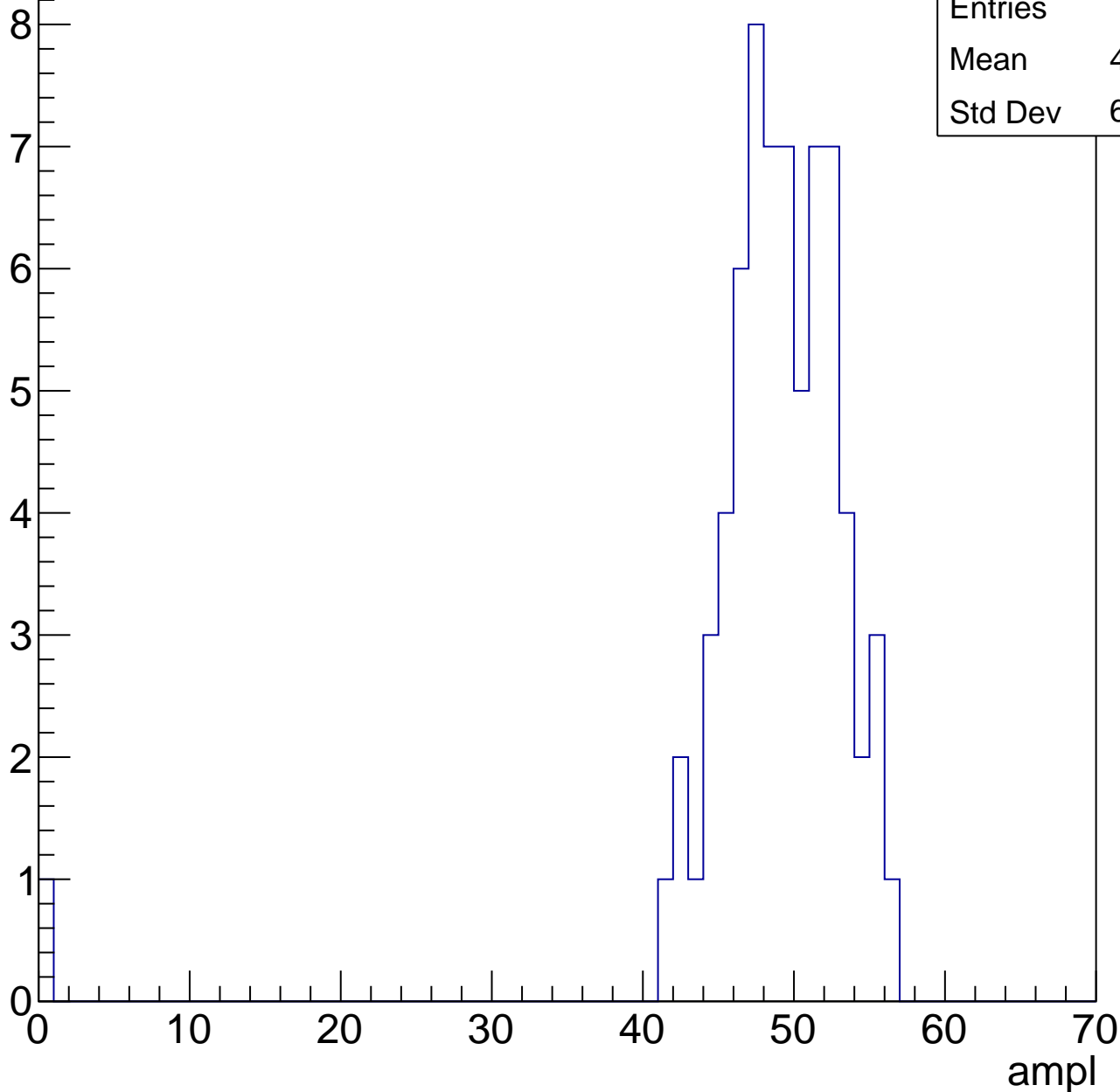


# B1L103S, U25-ch63, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	69
Mean	48.16
Std Dev	6.756

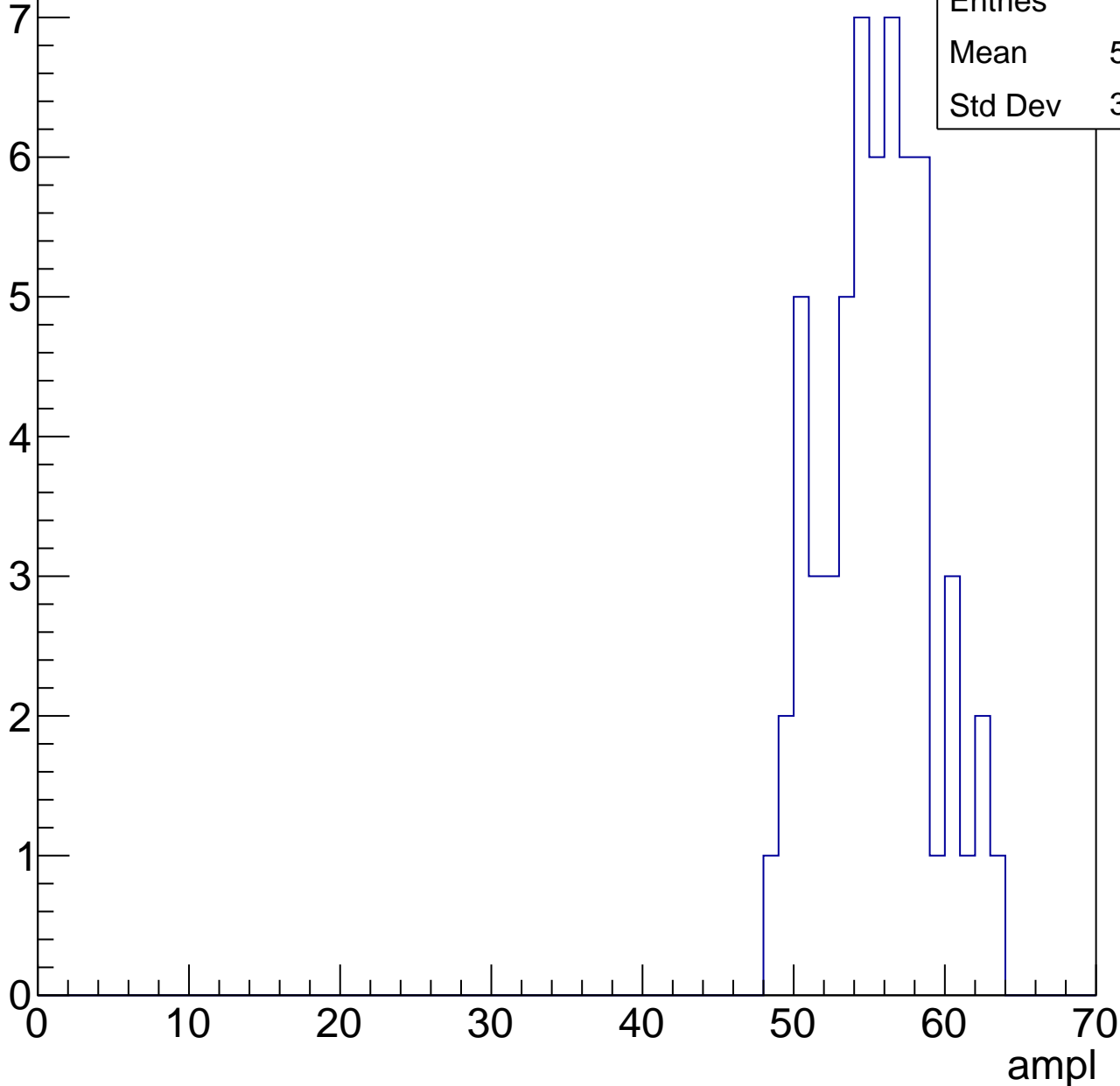


# B1L103S, U25-ch63, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	59
Mean	55.03
Std Dev	3.498



# B1L103S, U25-ch63, adc5

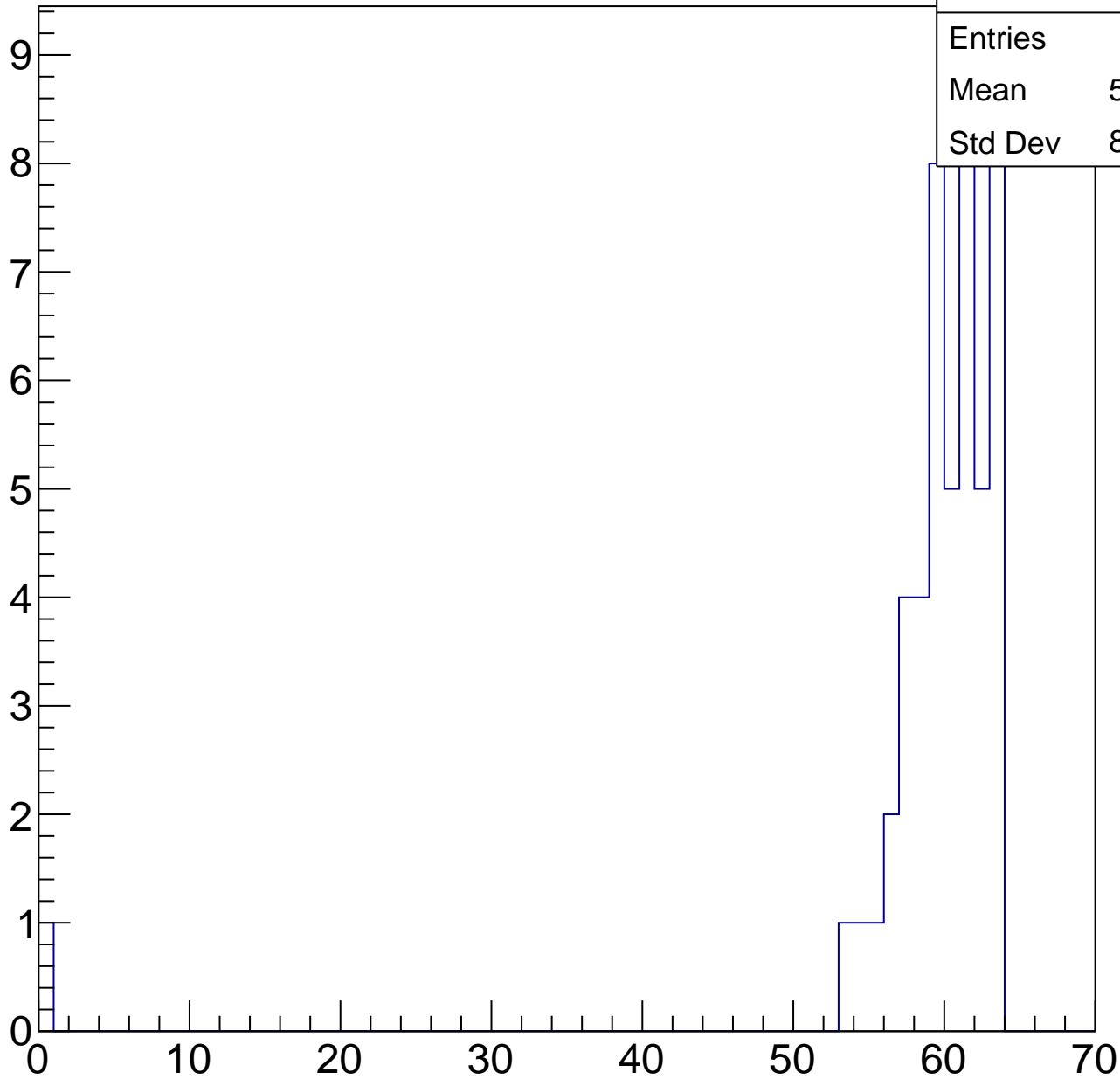
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	49
Mean	58.59
Std Dev	8.822

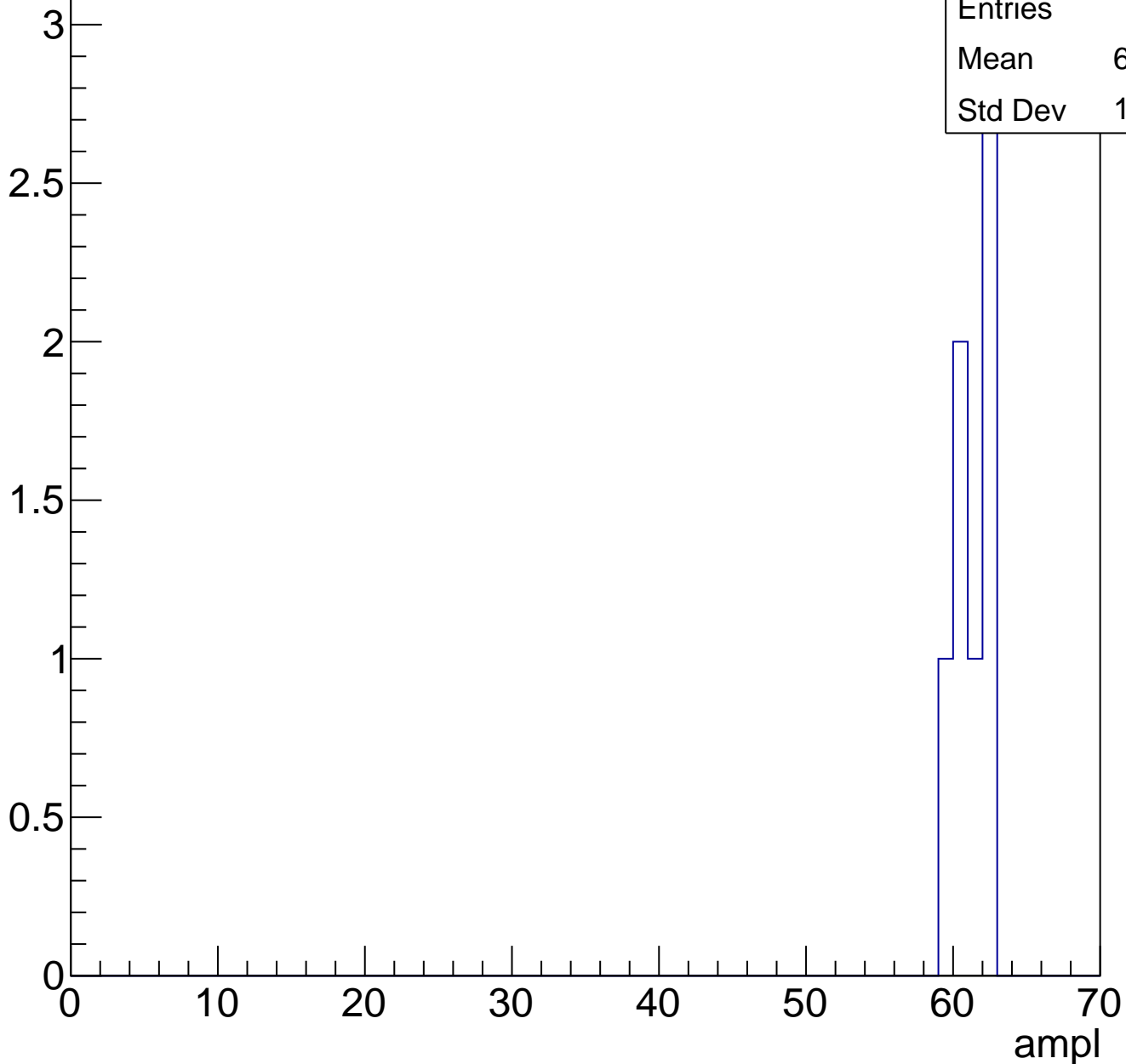
ampl



# B1L103S, U25-ch63, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U25-ch63, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

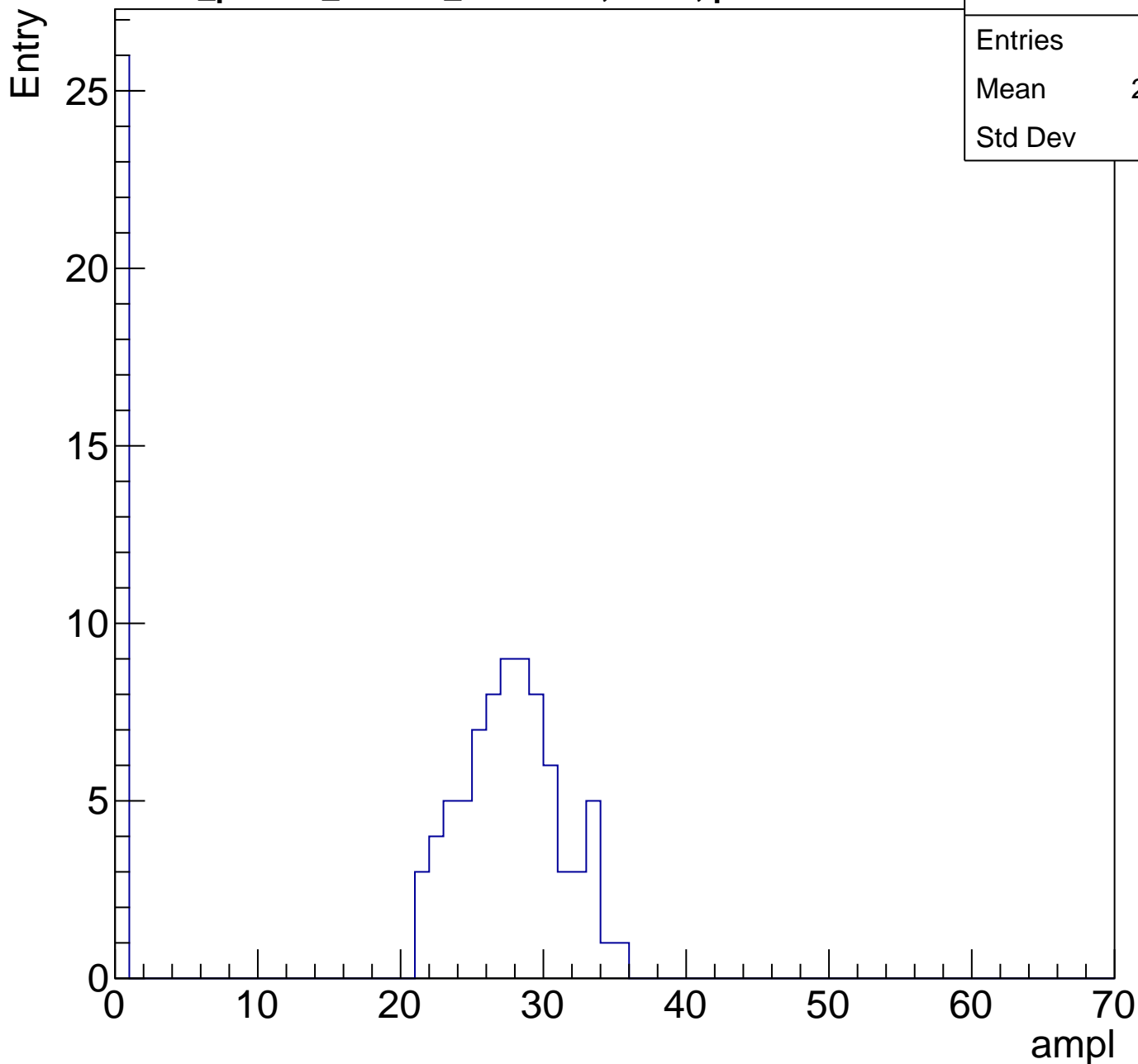
ampl

Entries	19
Mean	0
Std Dev	0

# B1L103S, U25-ch64, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	103
Mean	20.38
Std Dev	12.2

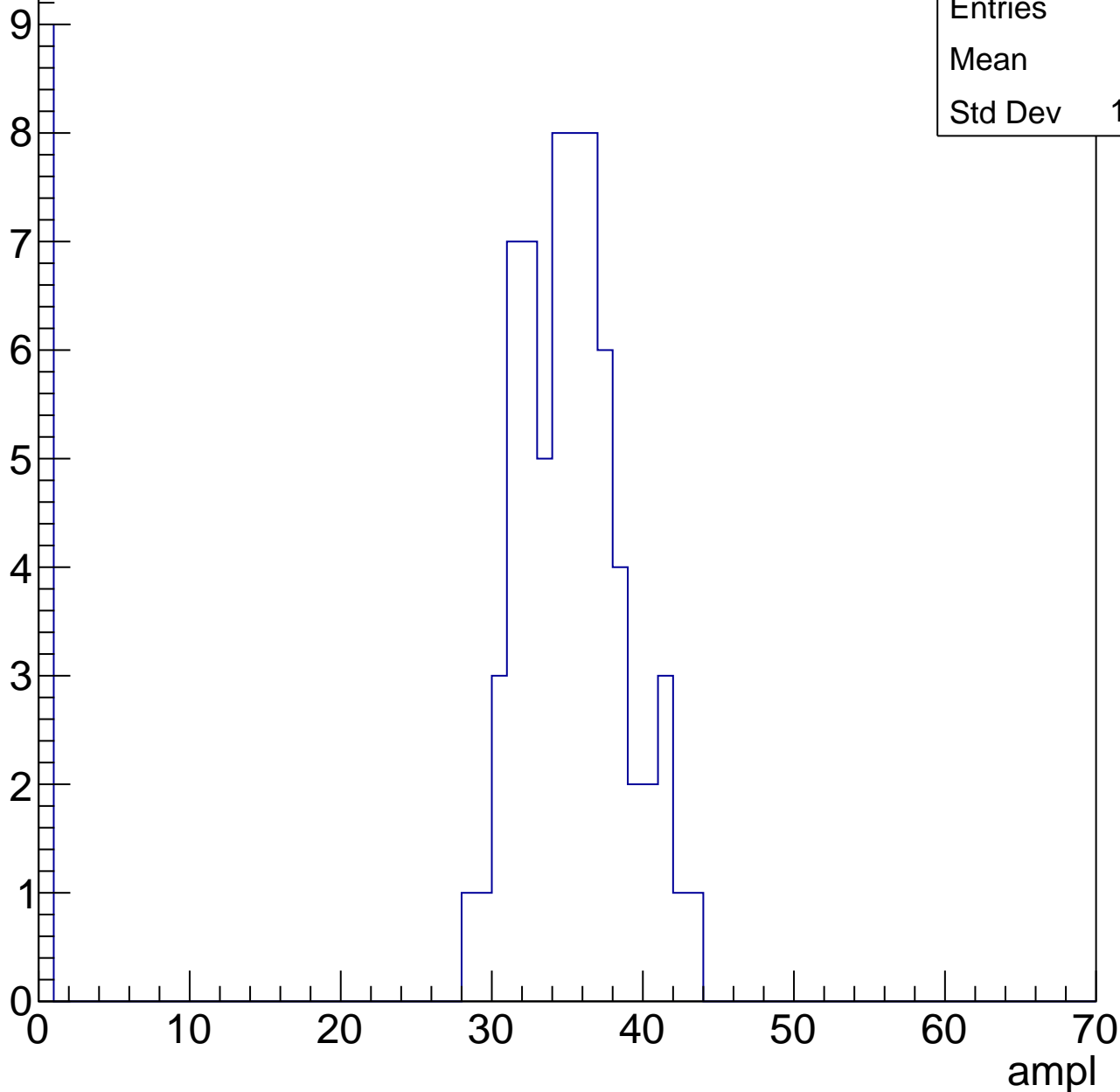


# B1L103S, U25-ch64, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	76
Mean	30.7
Std Dev	11.67

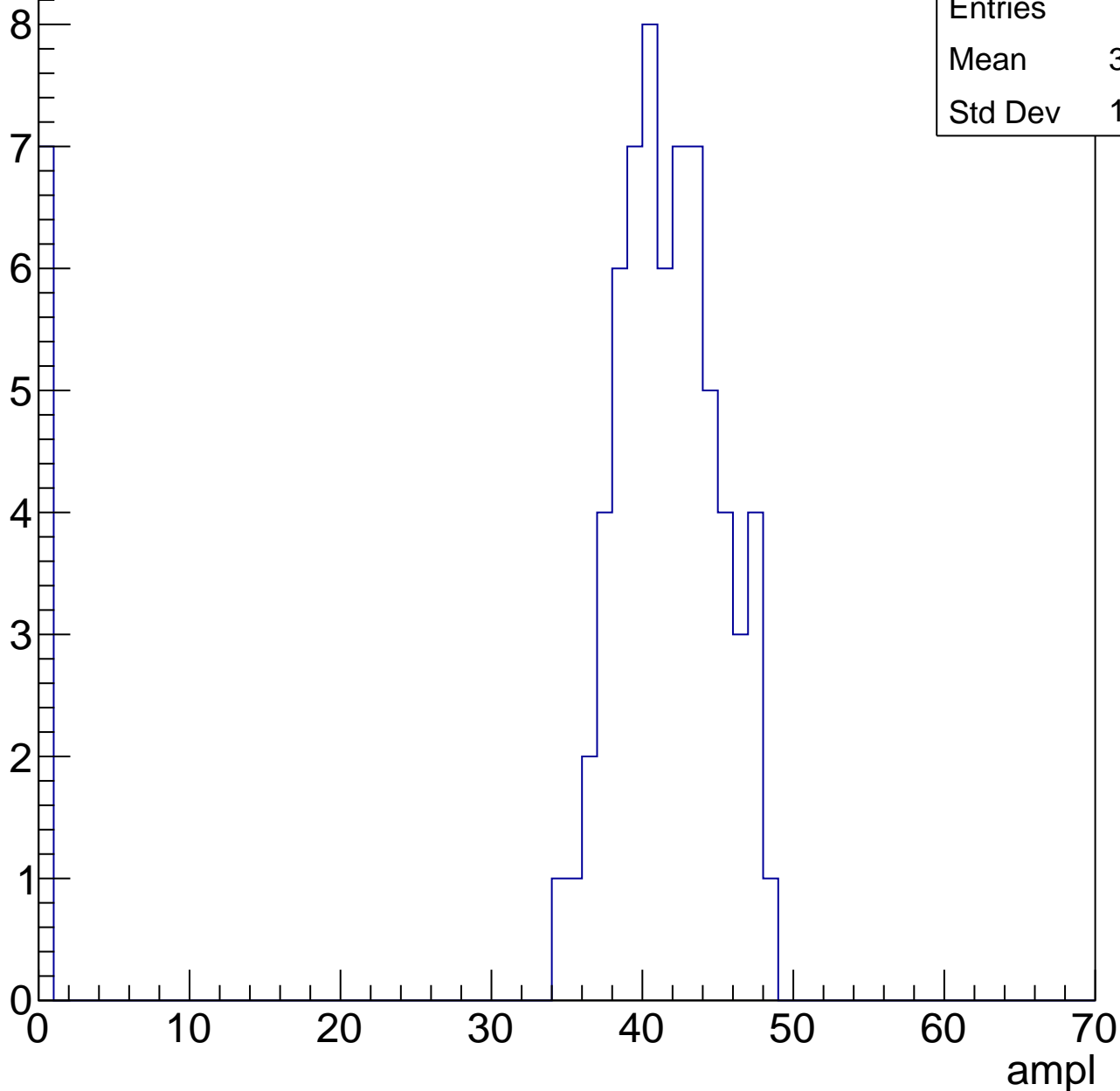


# B1L103S, U25-ch64, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	73
Mean	37.33
Std Dev	12.54

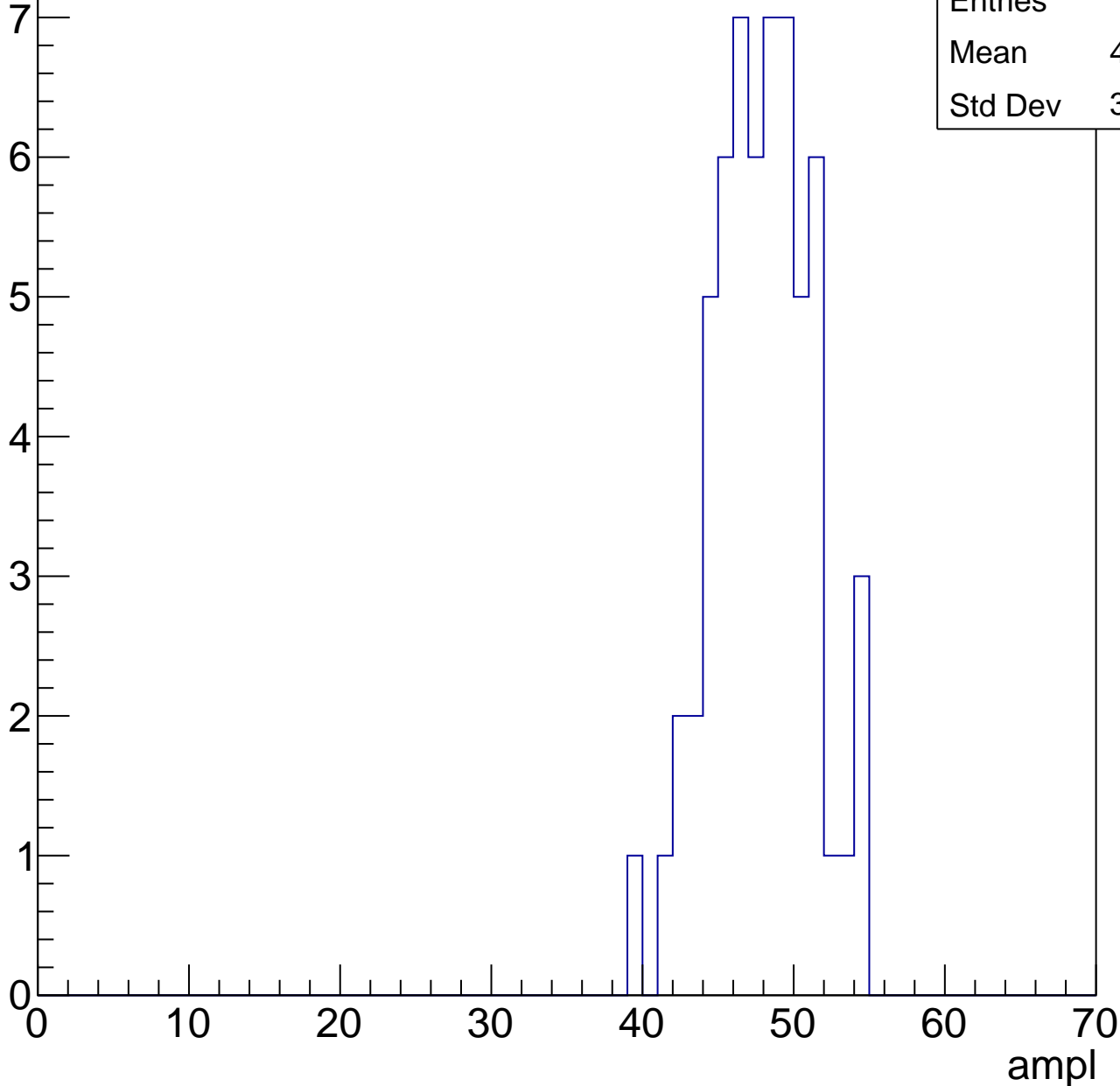


# B1L103S, U25-ch64, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	60
Mean	47.43
Std Dev	3.242

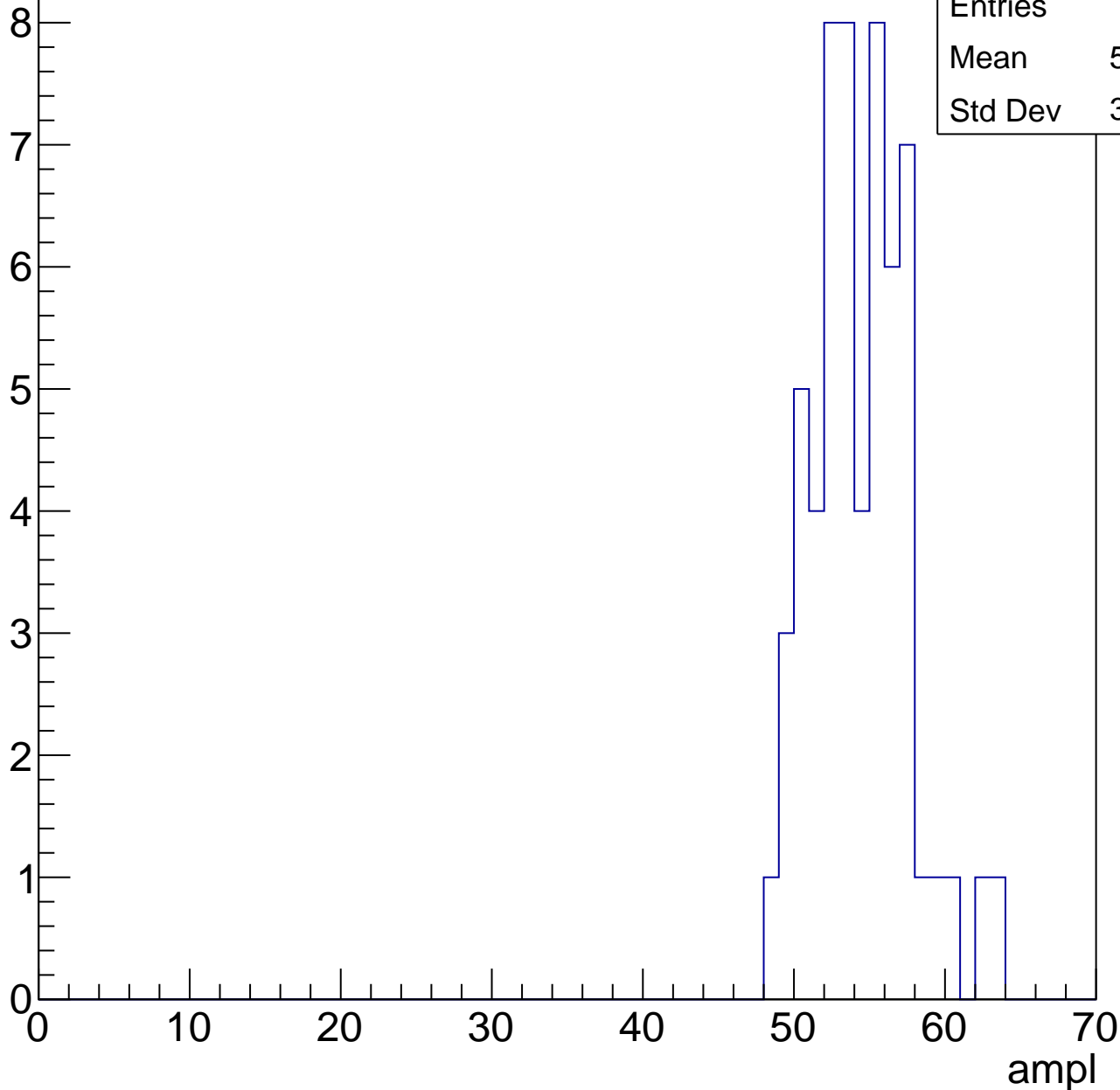


# B1L103S, U25-ch64, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	59
Mean	53.93
Std Dev	3.145



# B1L103S, U25-ch64, adc5

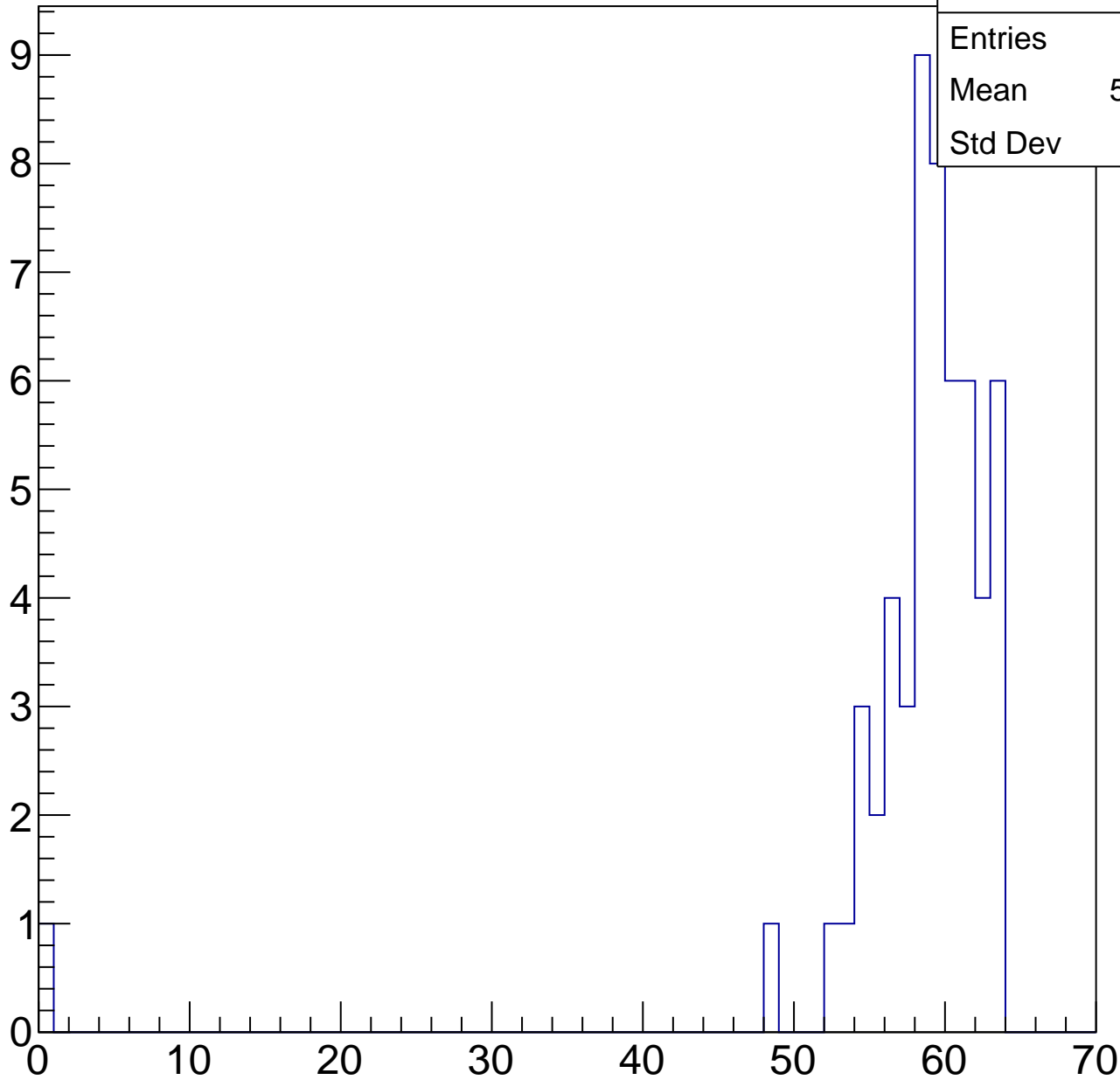
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	55
Mean	57.56
Std Dev	8.42

ampl

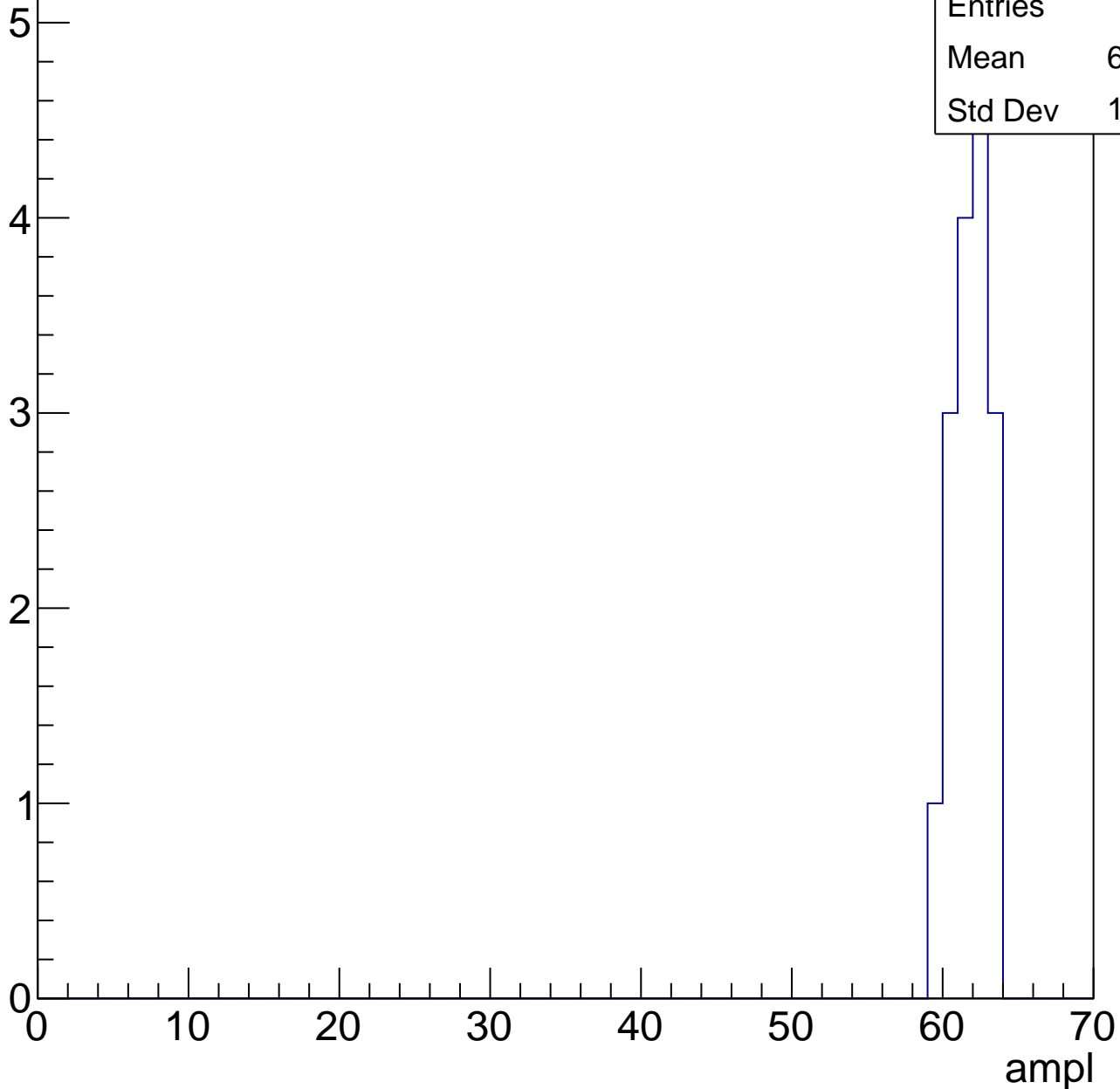


# B1L103S, U25-ch64, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	16
Mean	61.38
Std Dev	1.166





# B1L103S, U25-ch64, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U25-ch65, adc0

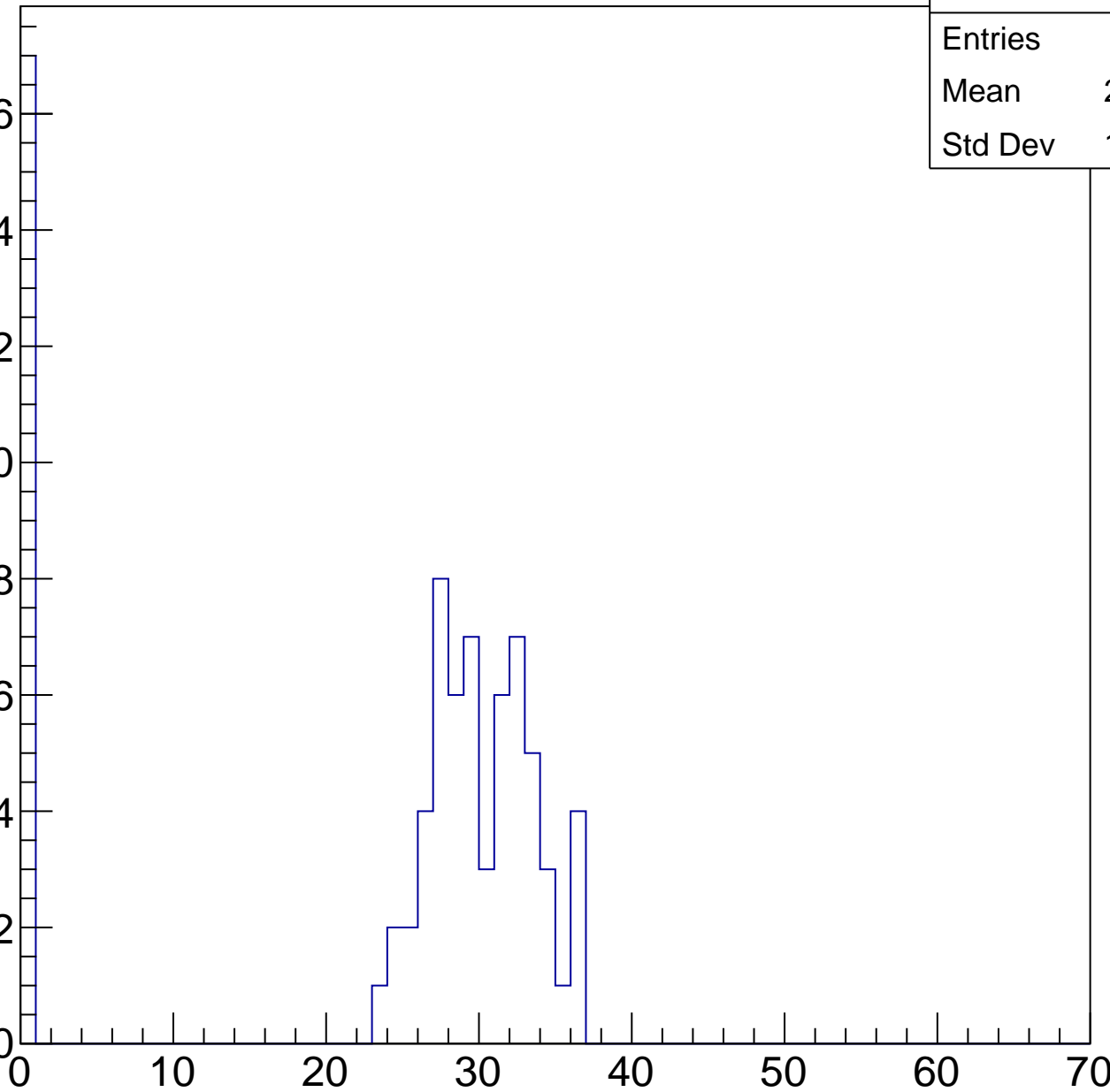
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	76
Mean	23.13
Std Dev	12.75

Entry

16  
14  
12  
10  
8  
6  
4  
2  
0

ampl

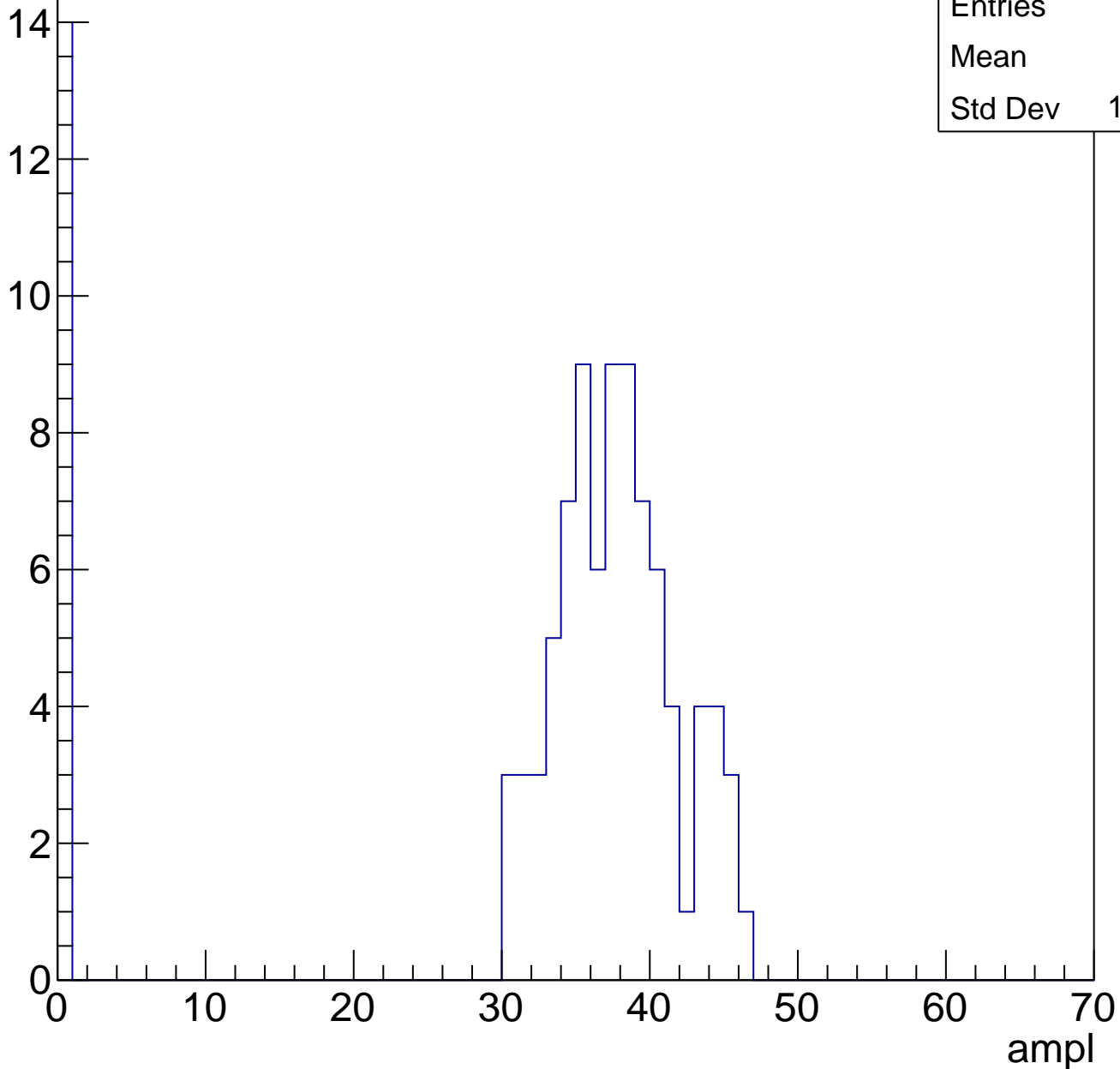


# B1L103S, U25-ch65, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	98
Mean	32
Std Dev	13.56

Entry

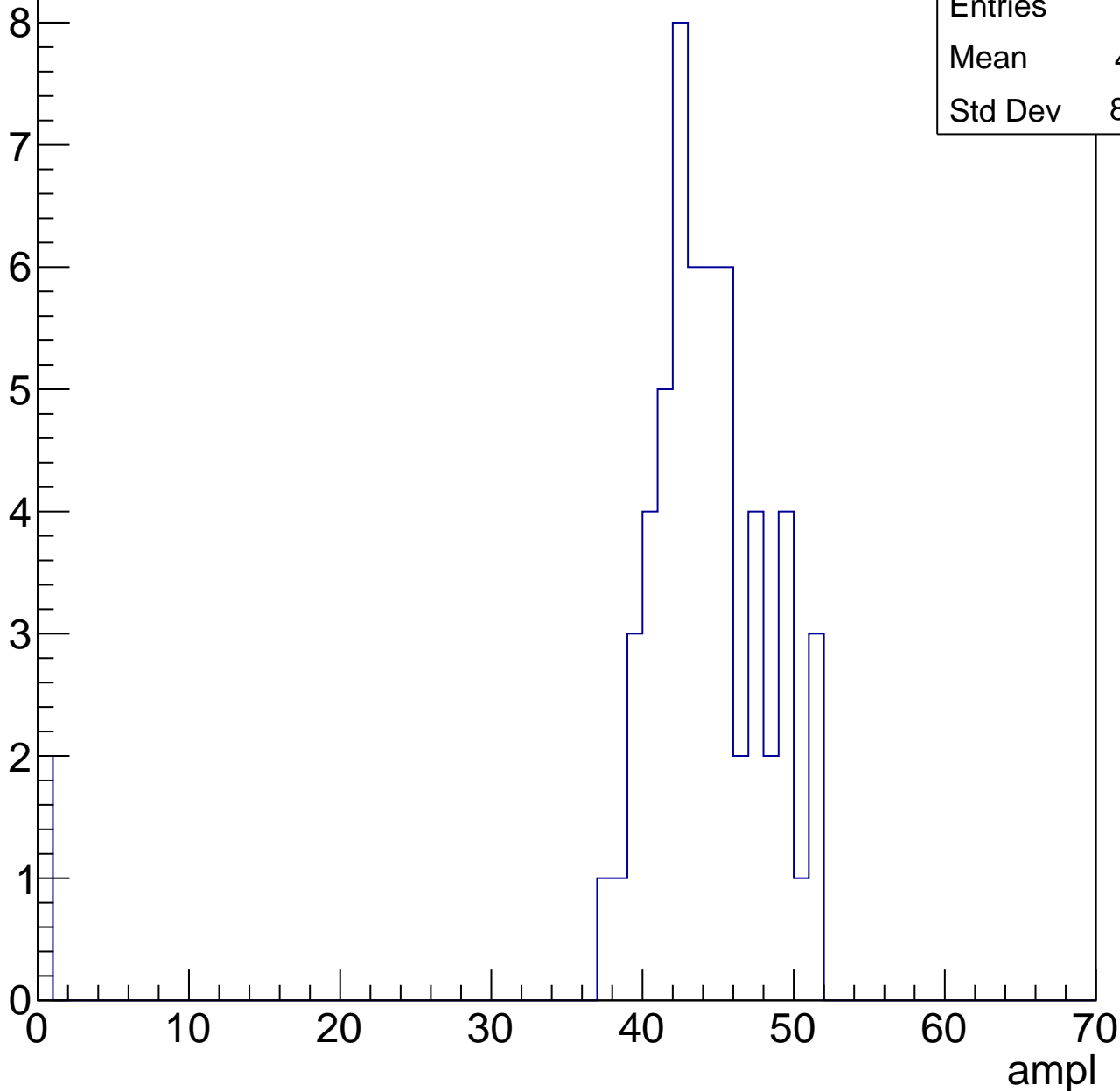


# B1L103S, U25-ch65, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	58
Mean	42.41
Std Dev	8.708

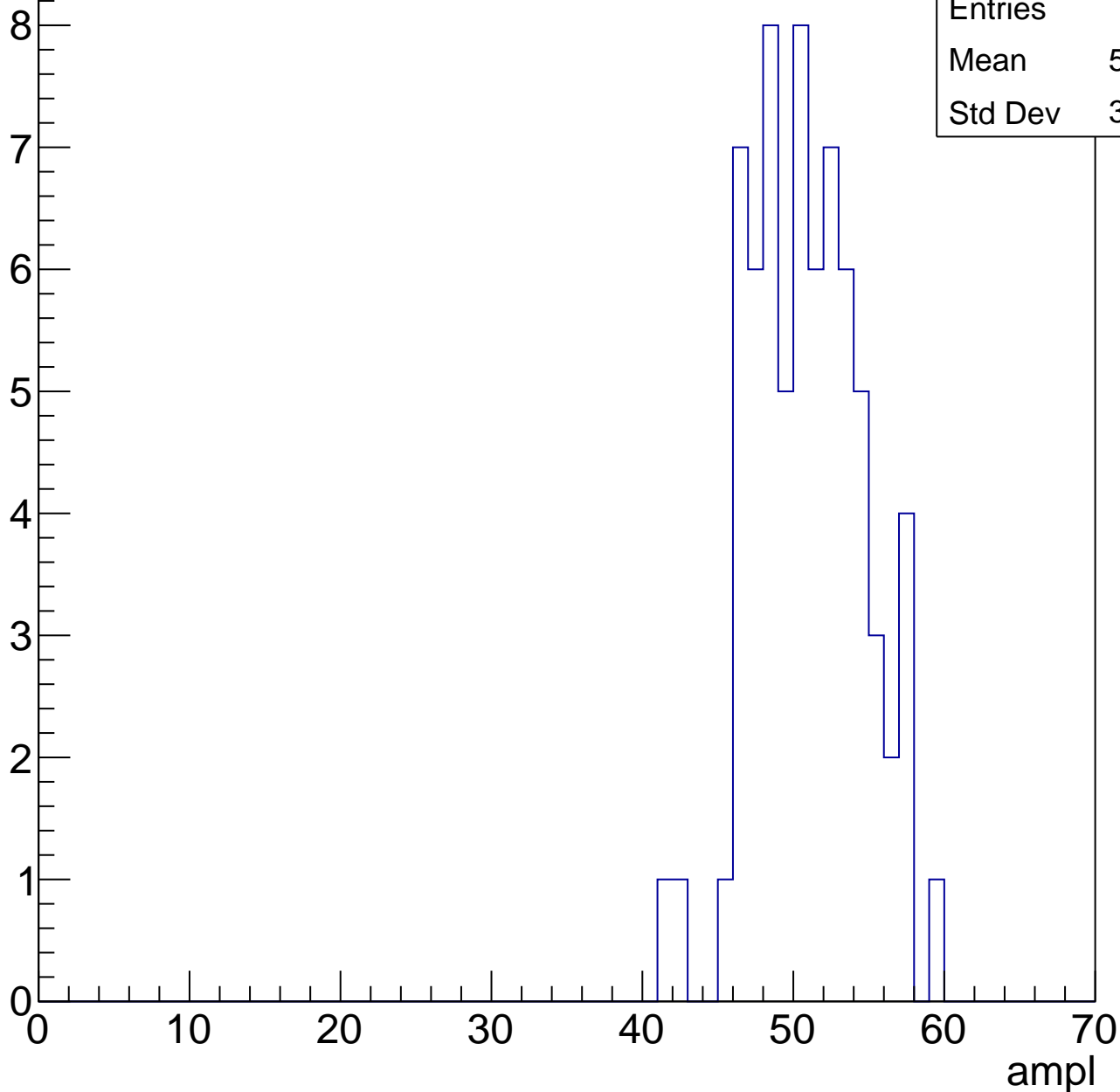


# B1L103S, U25-ch65, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	71
Mean	50.46
Std Dev	3.657

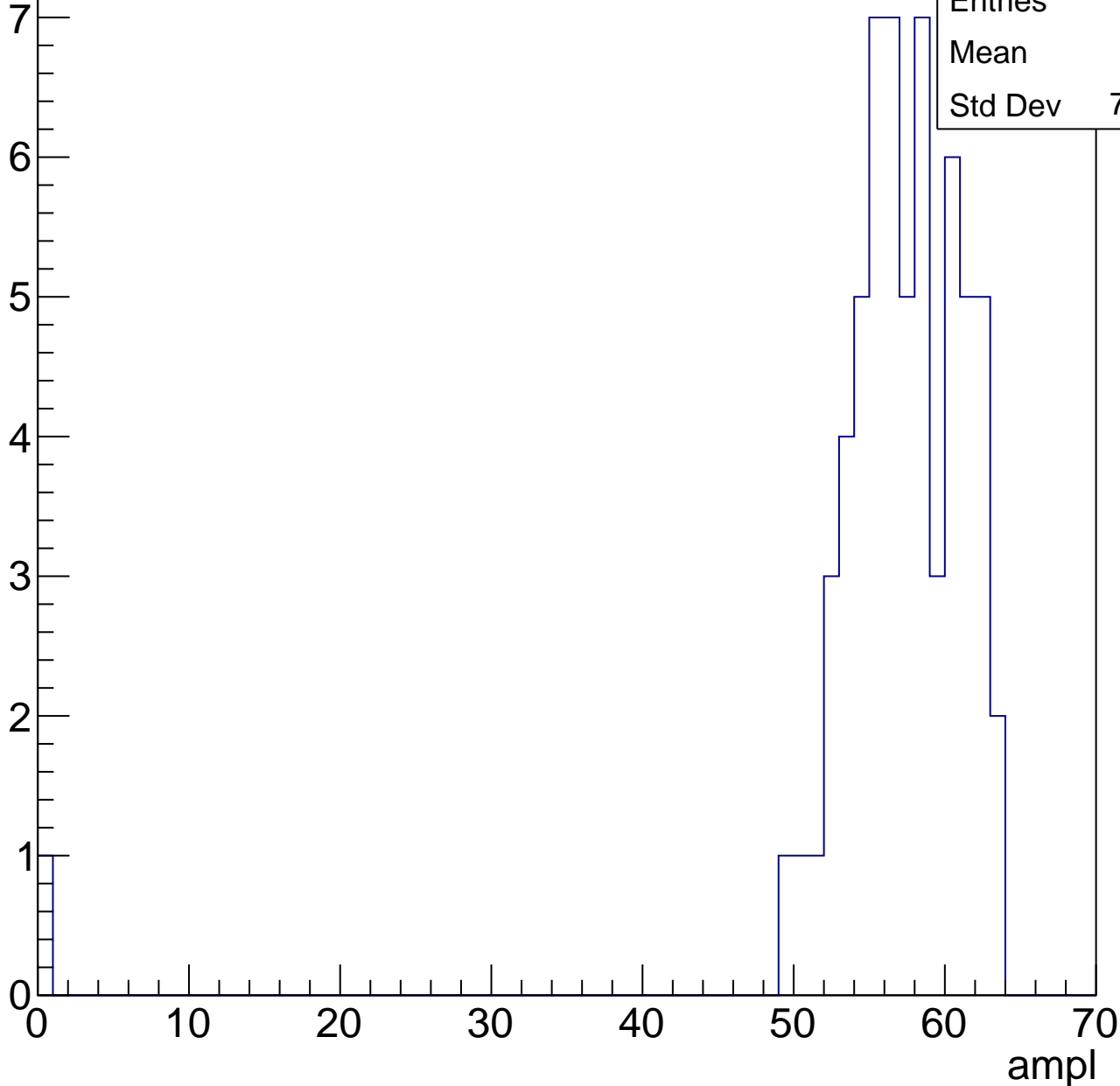


# B1L103S, U25-ch65, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	63
Mean	56.1
Std Dev	7.884

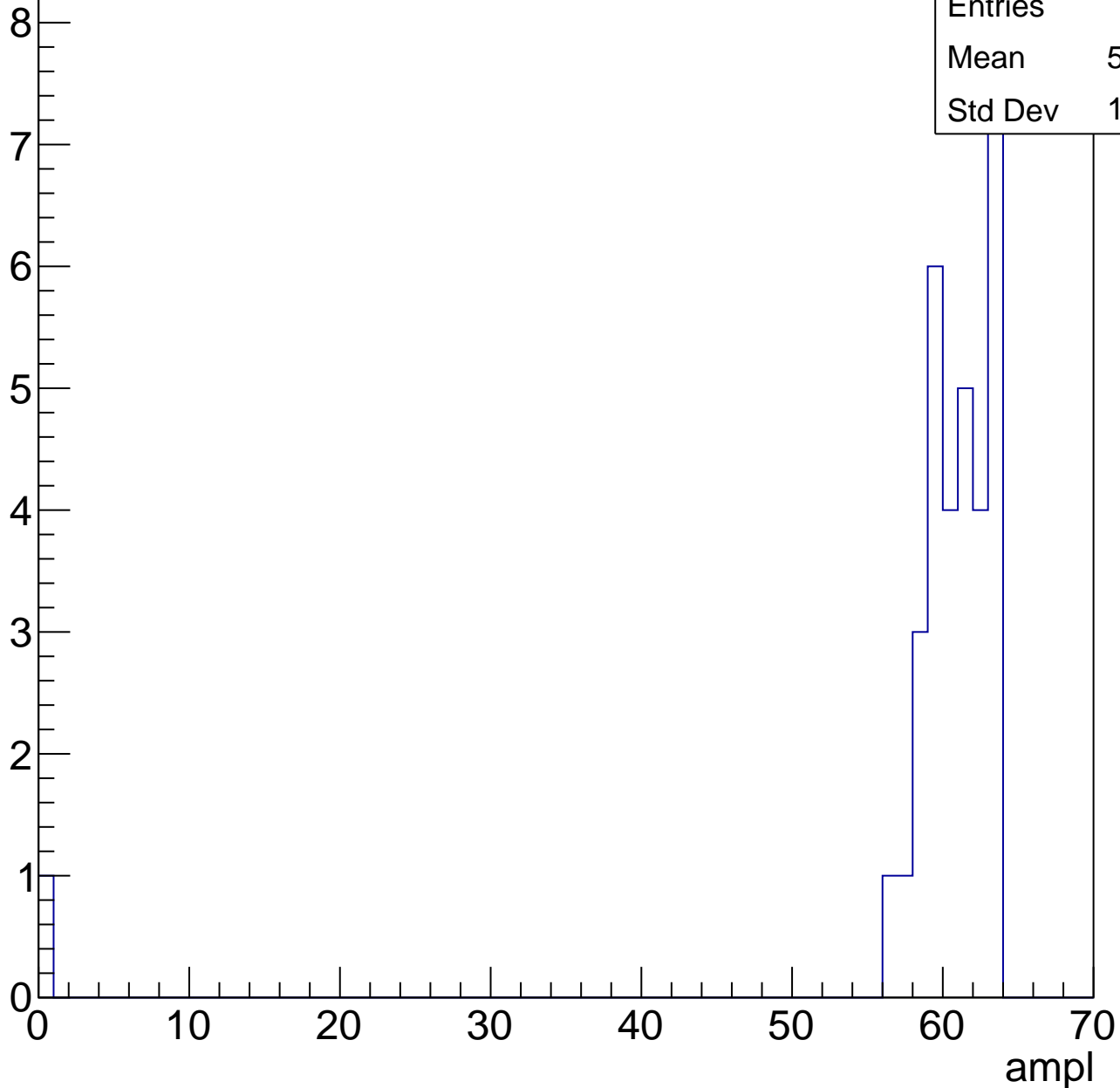


# B1L103S, U25-ch65, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	33
Mean	58.73
Std Dev	10.56



# B1L103S, U25-ch65, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	1
Mean	62
Std Dev	0

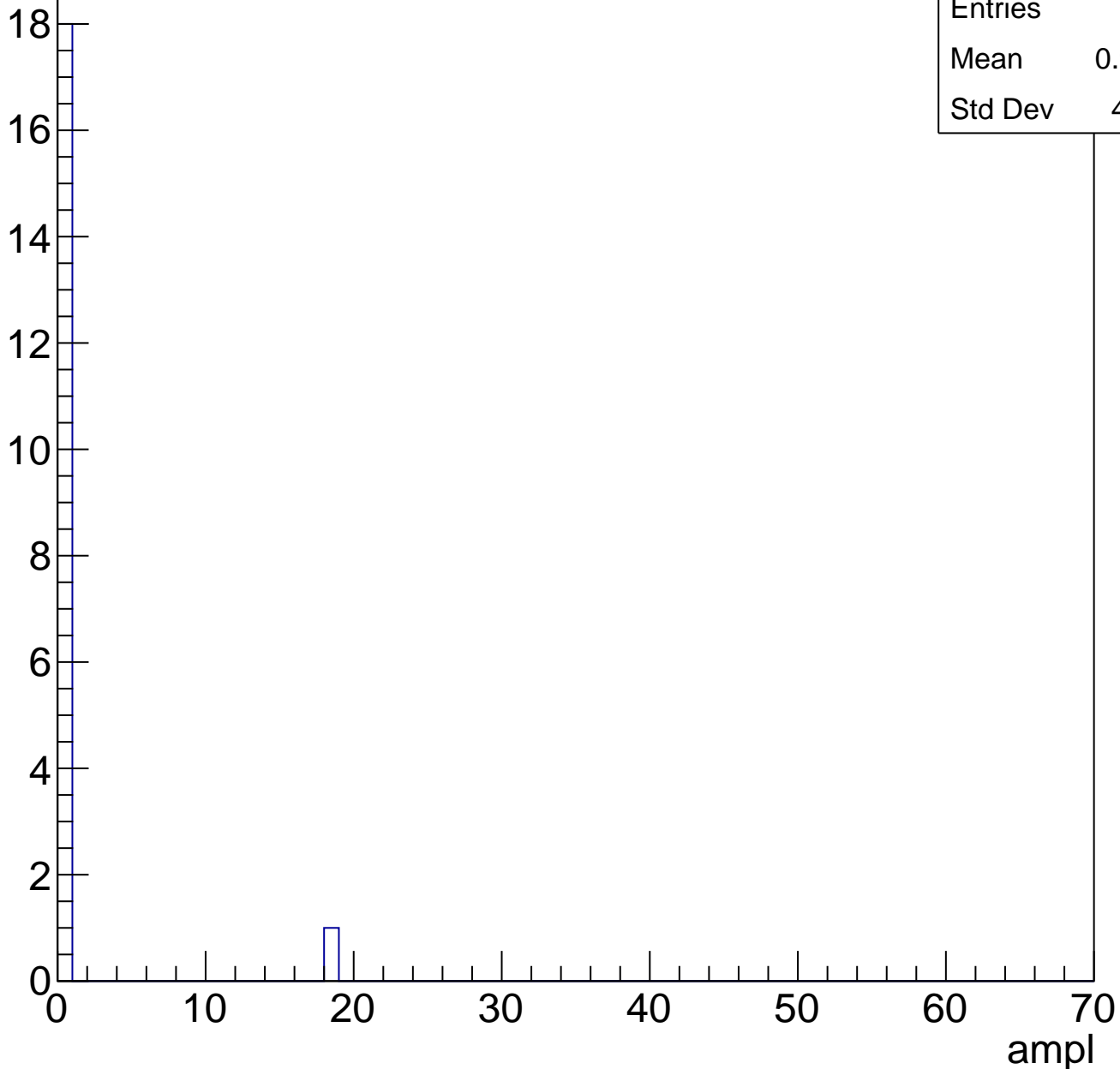


# B1L103S, U25-ch65, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	19
Mean	0.9474
Std Dev	4.019

Entry

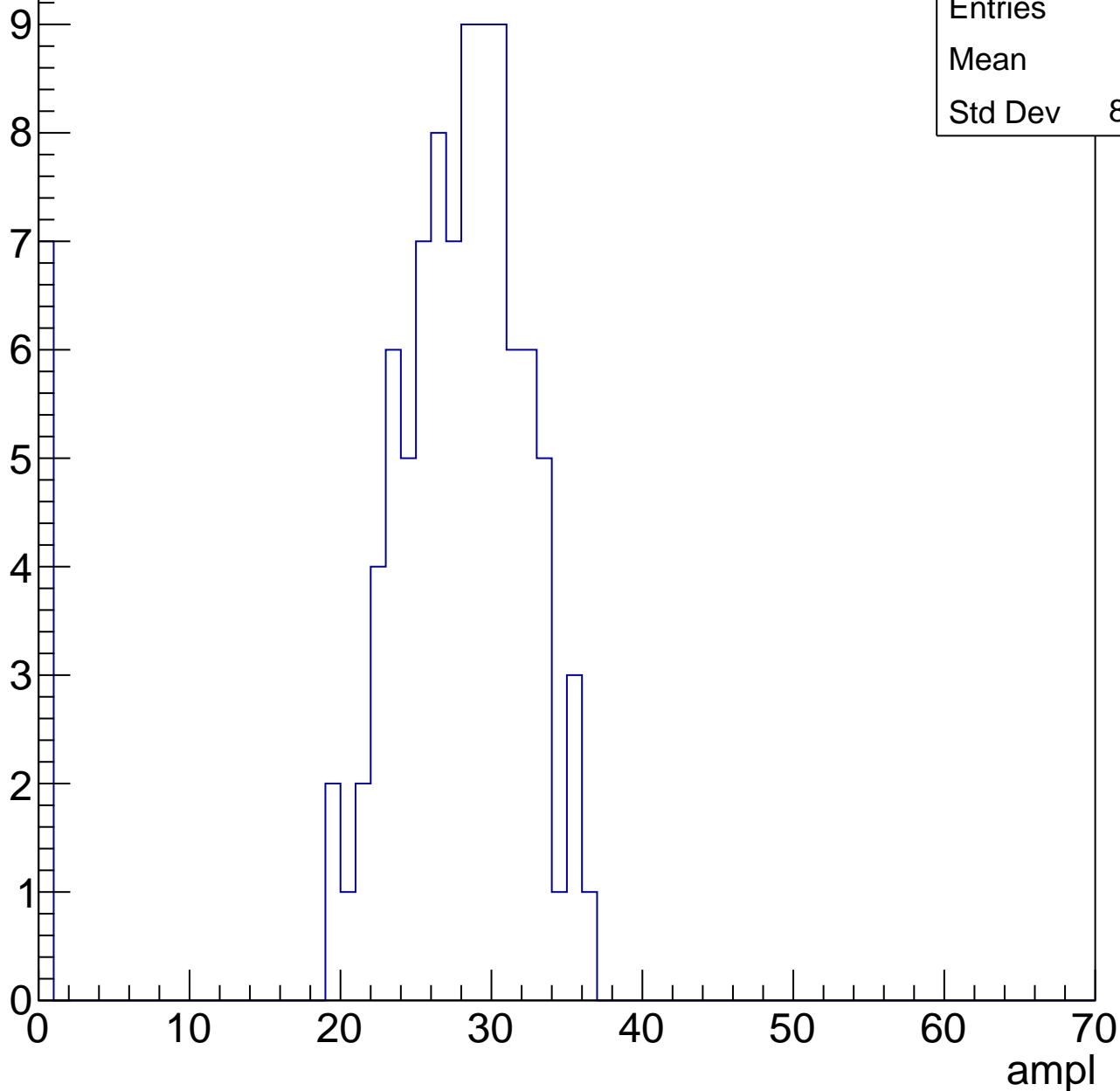


# B1L103S, U25-ch66, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	98
Mean	25.7
Std Dev	8.042

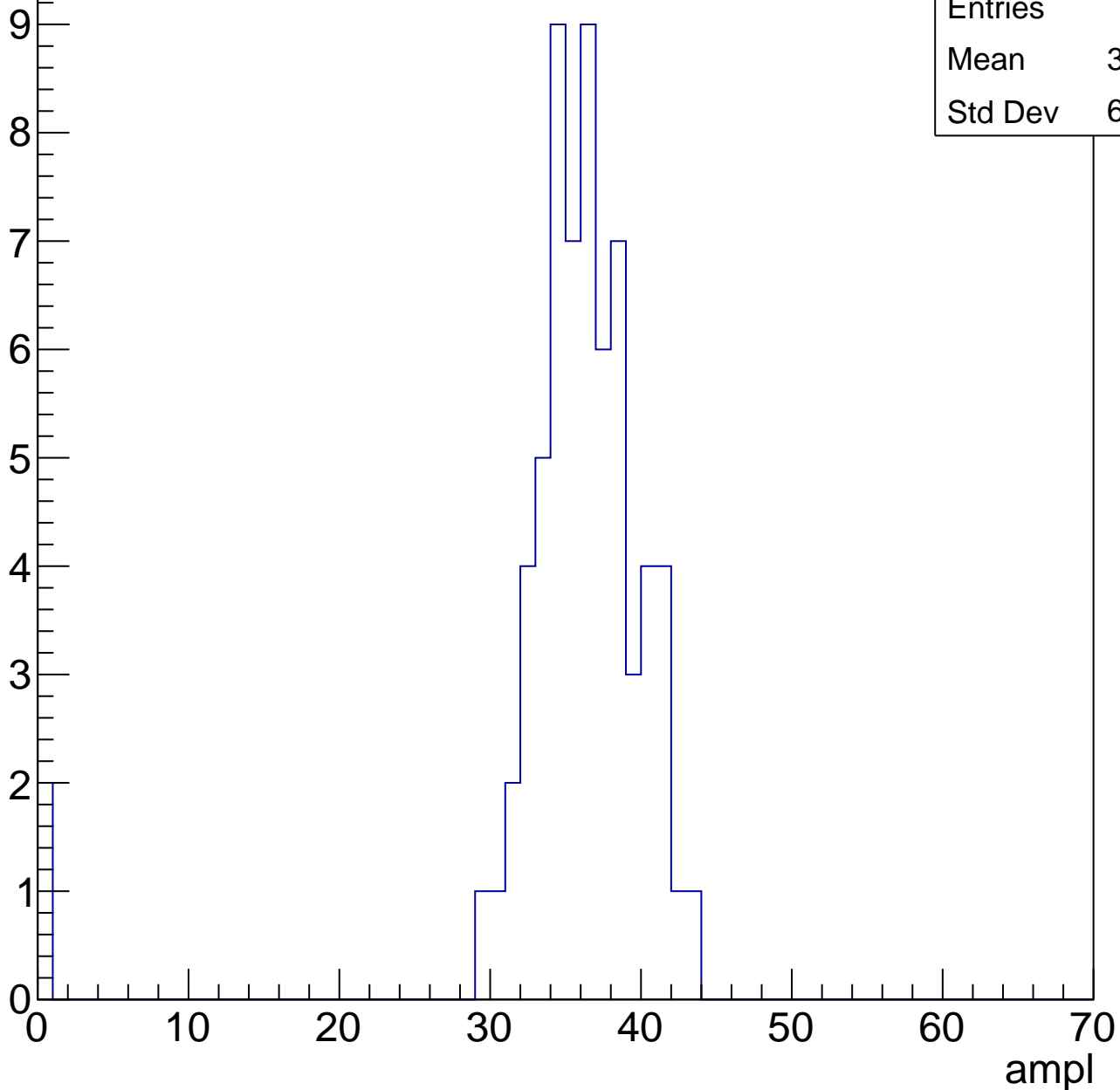


# B1L103S, U25-ch66, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

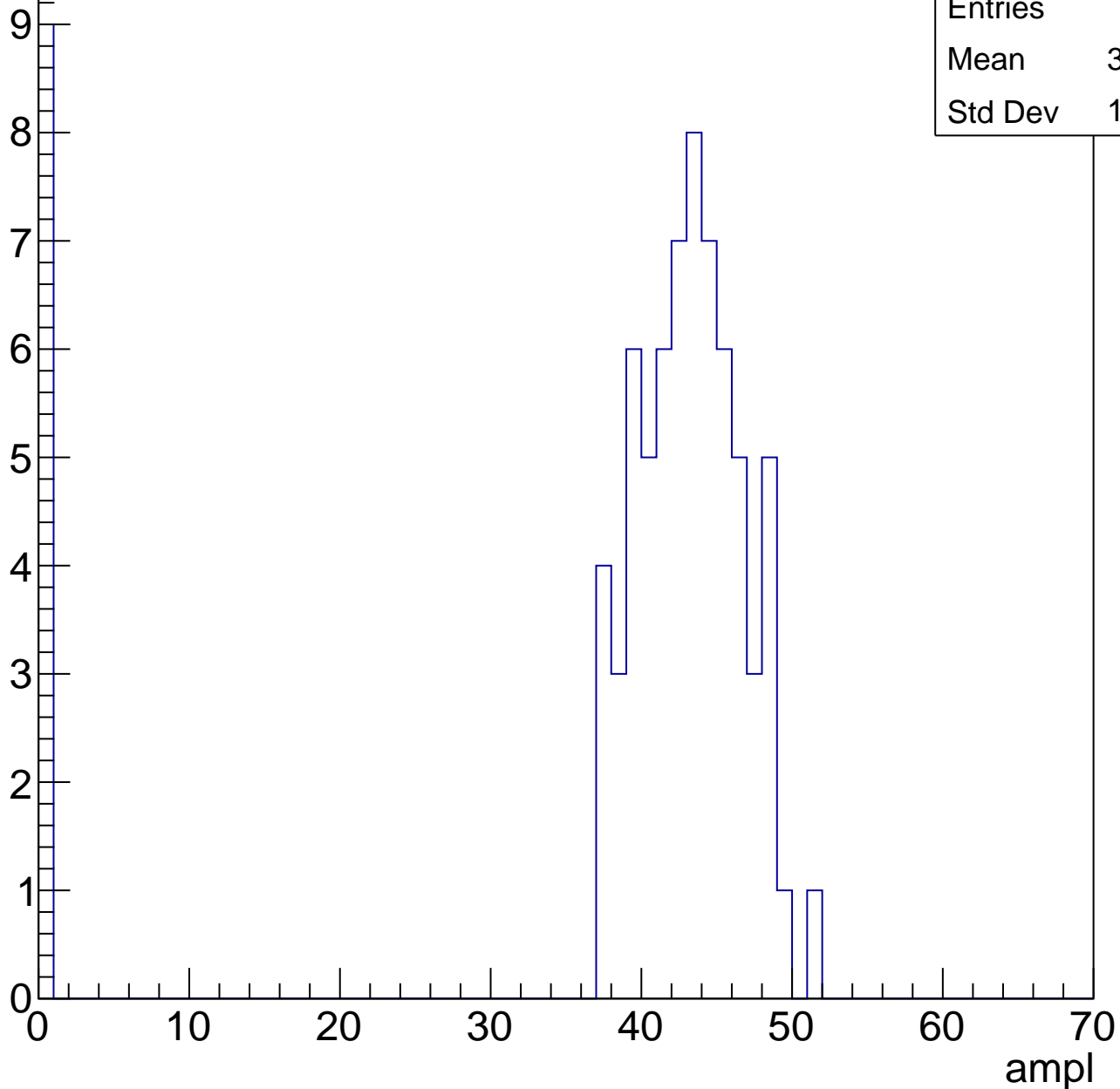
Entries	66
Mean	34.89
Std Dev	6.863



# B1L103S, U25-ch66, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

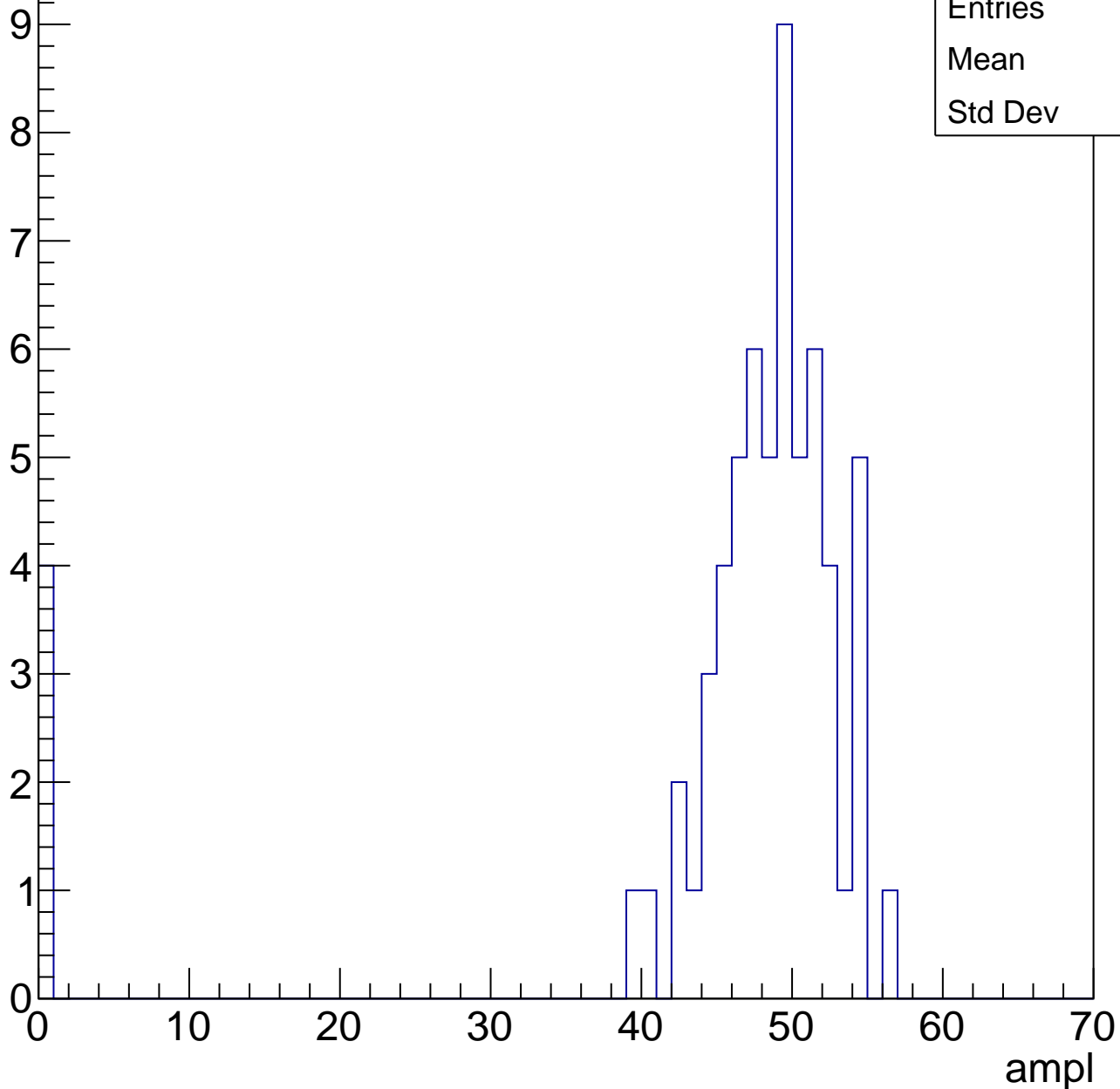
Entry



# B1L103S, U25-ch66, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

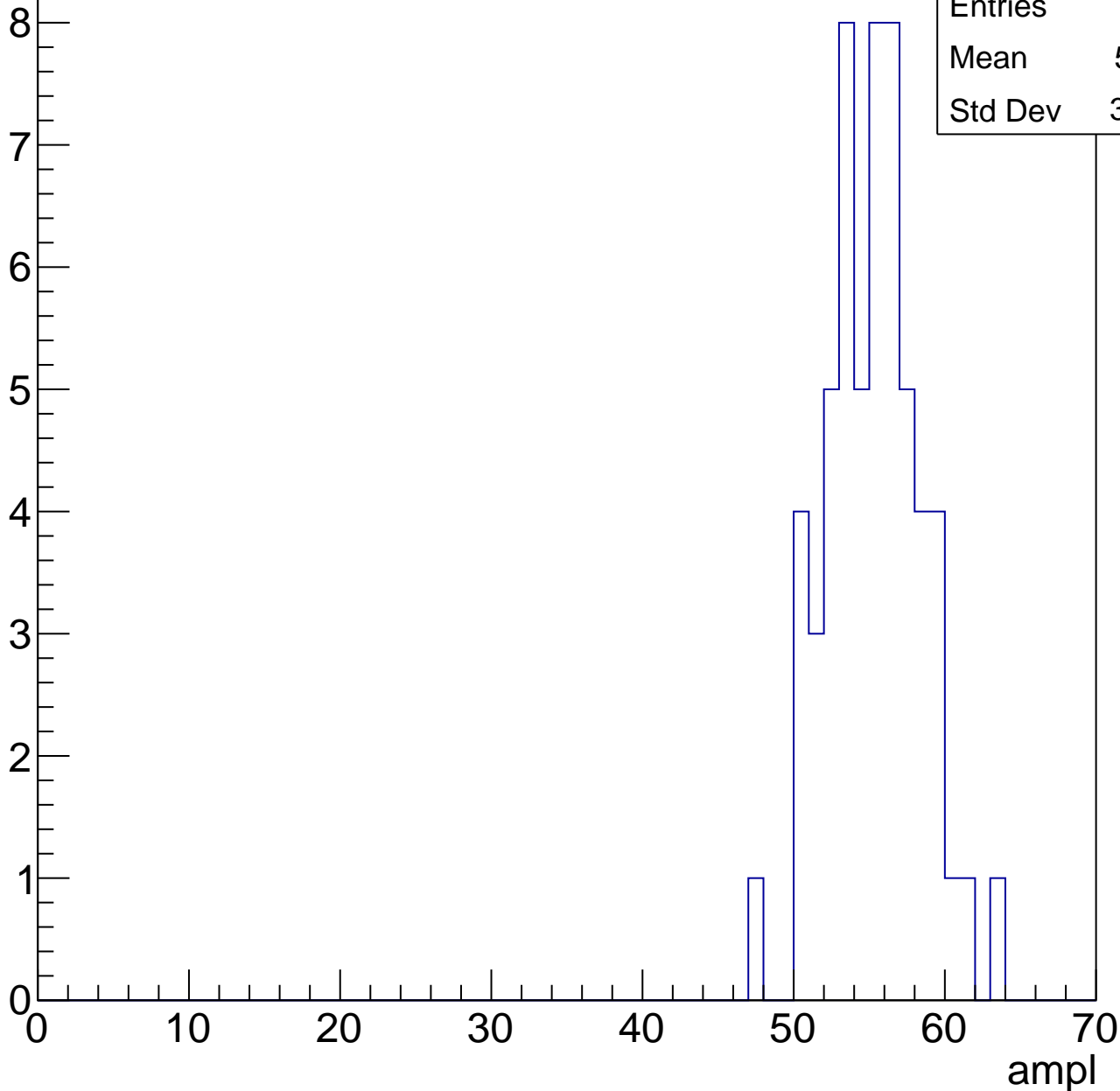


# B1L103S, U25-ch66, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	58
Mean	54.81
Std Dev	3.065

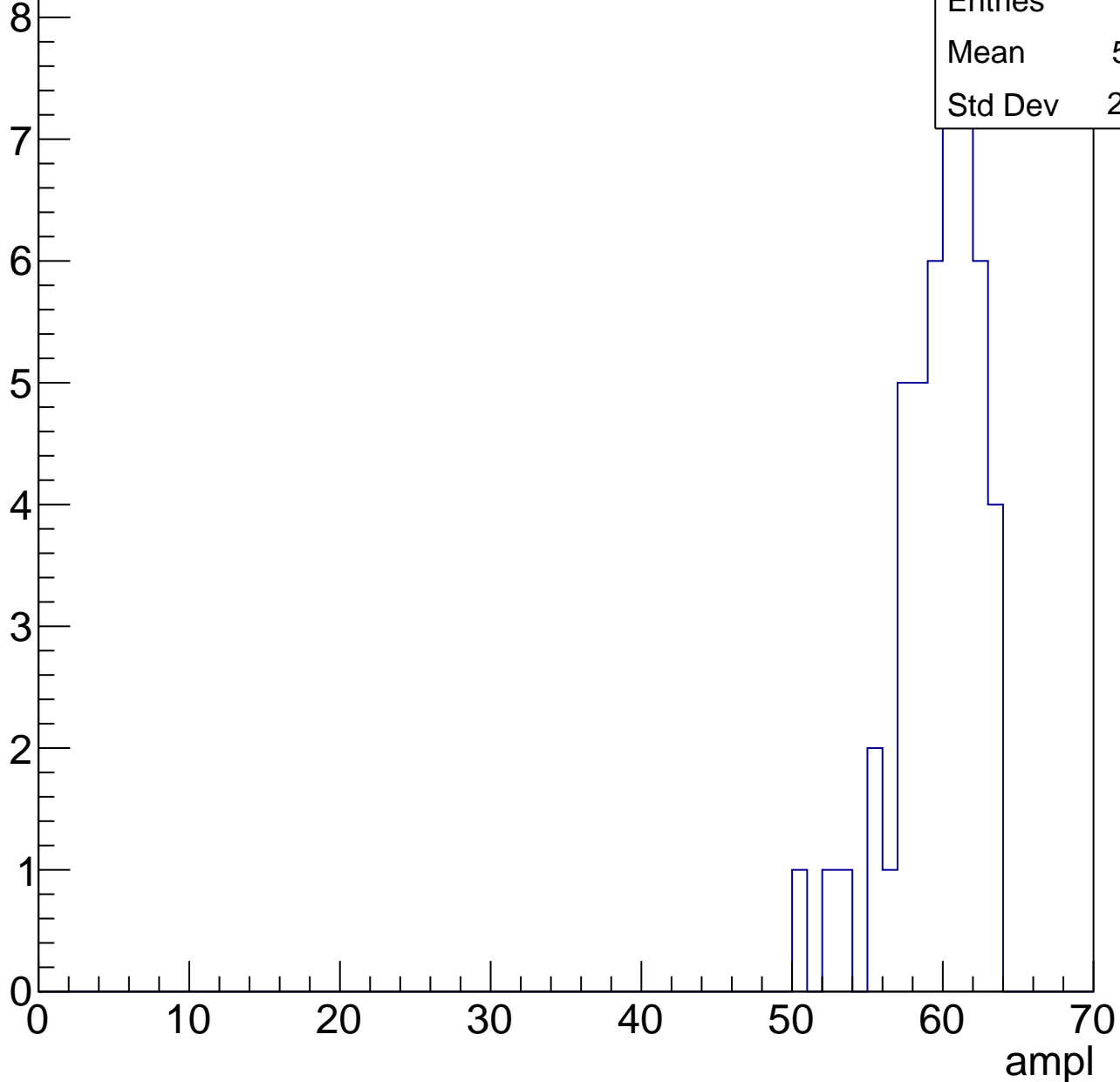


# B1L103S, U25-ch66, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	48
Mean	59.21
Std Dev	2.843

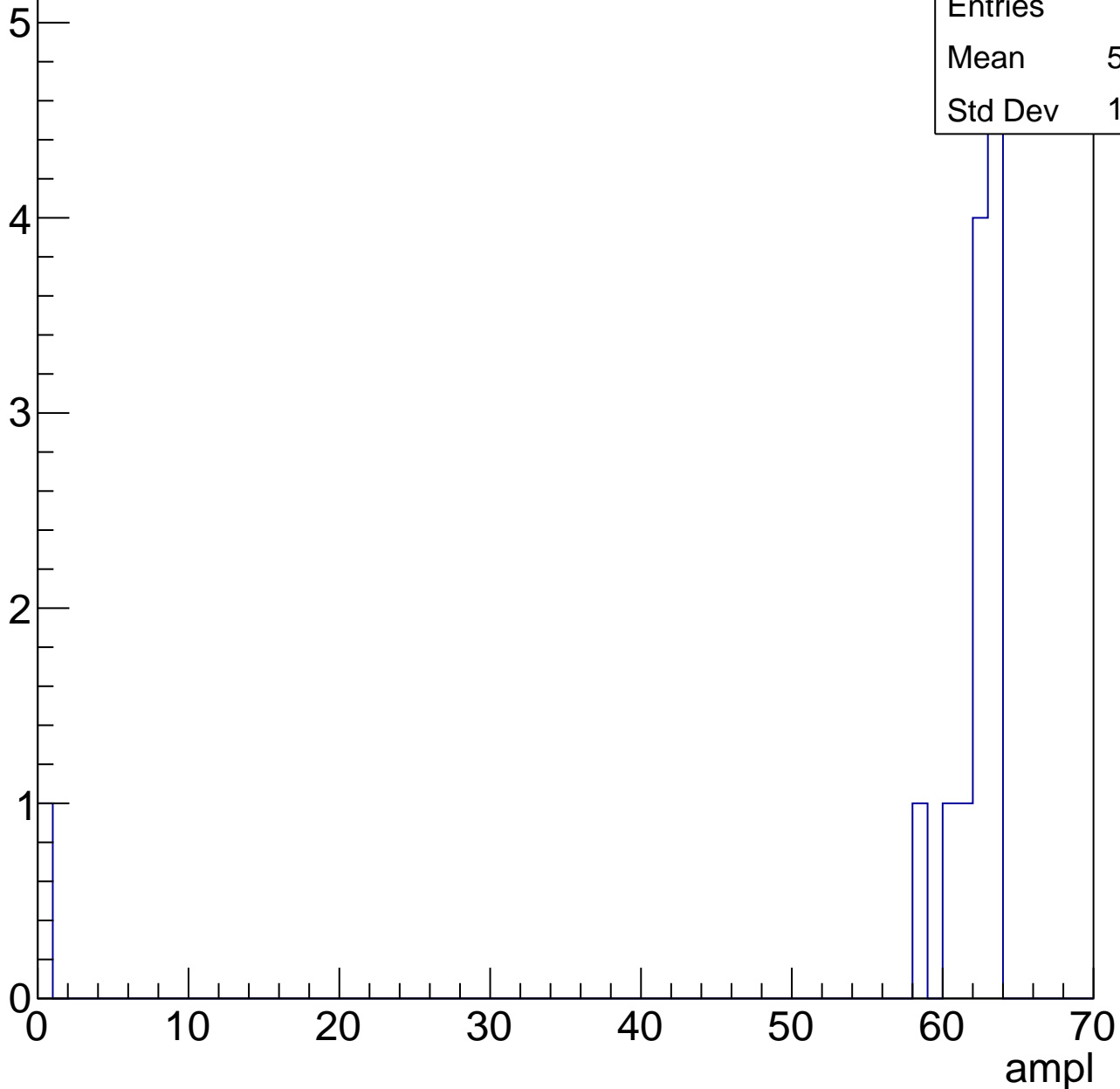


# B1L103S, U25-ch66, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	13
Mean	57.08
Std Dev	16.54



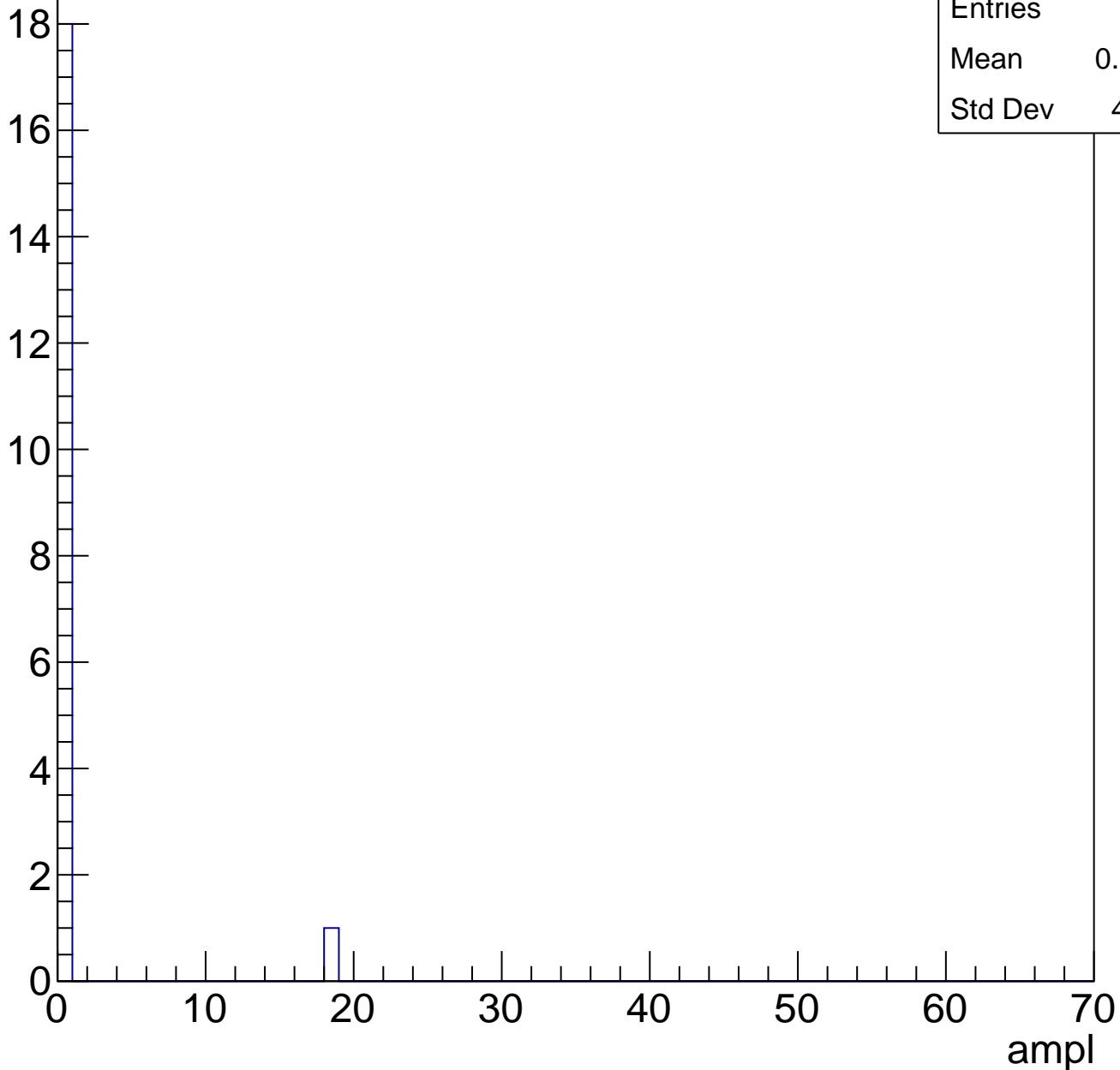


# B1L103S, U25-ch66, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	19
Mean	0.9474
Std Dev	4.019

Entry

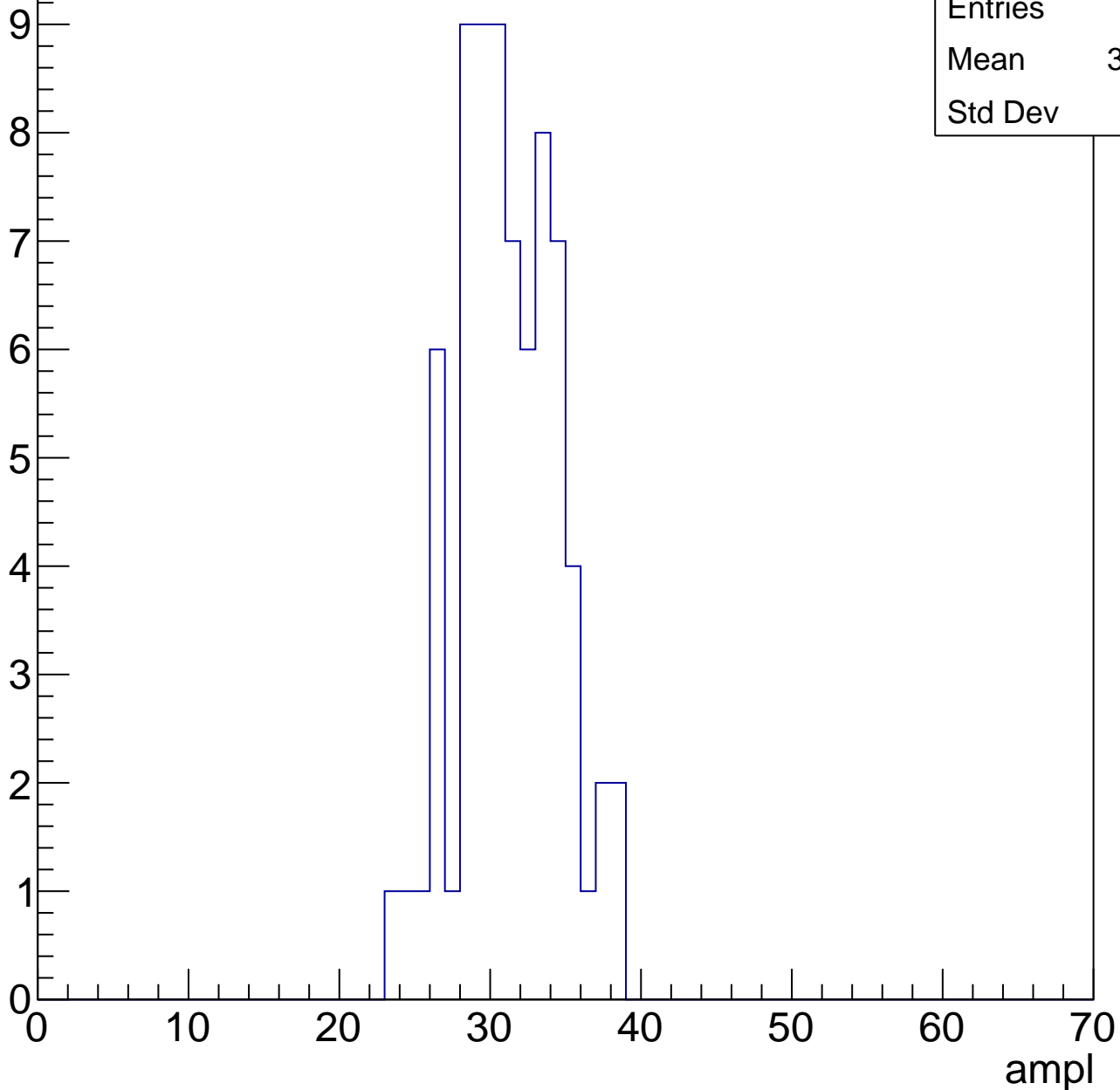


# B1L103S, U25-ch67, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	74
Mean	30.74
Std Dev	3.28

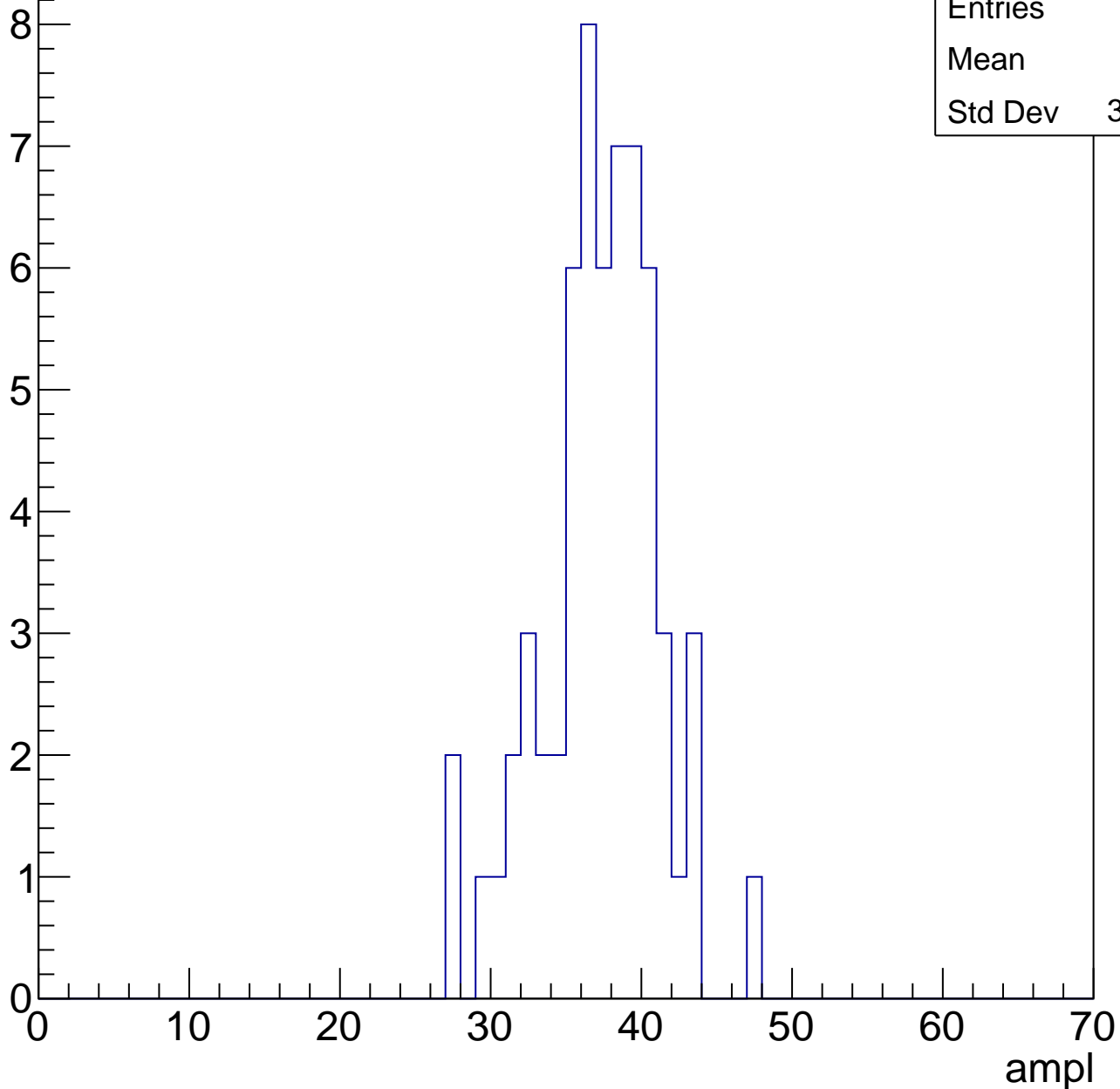


# B1L103S, U25-ch67, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	61
Mean	36.8
Std Dev	3.862

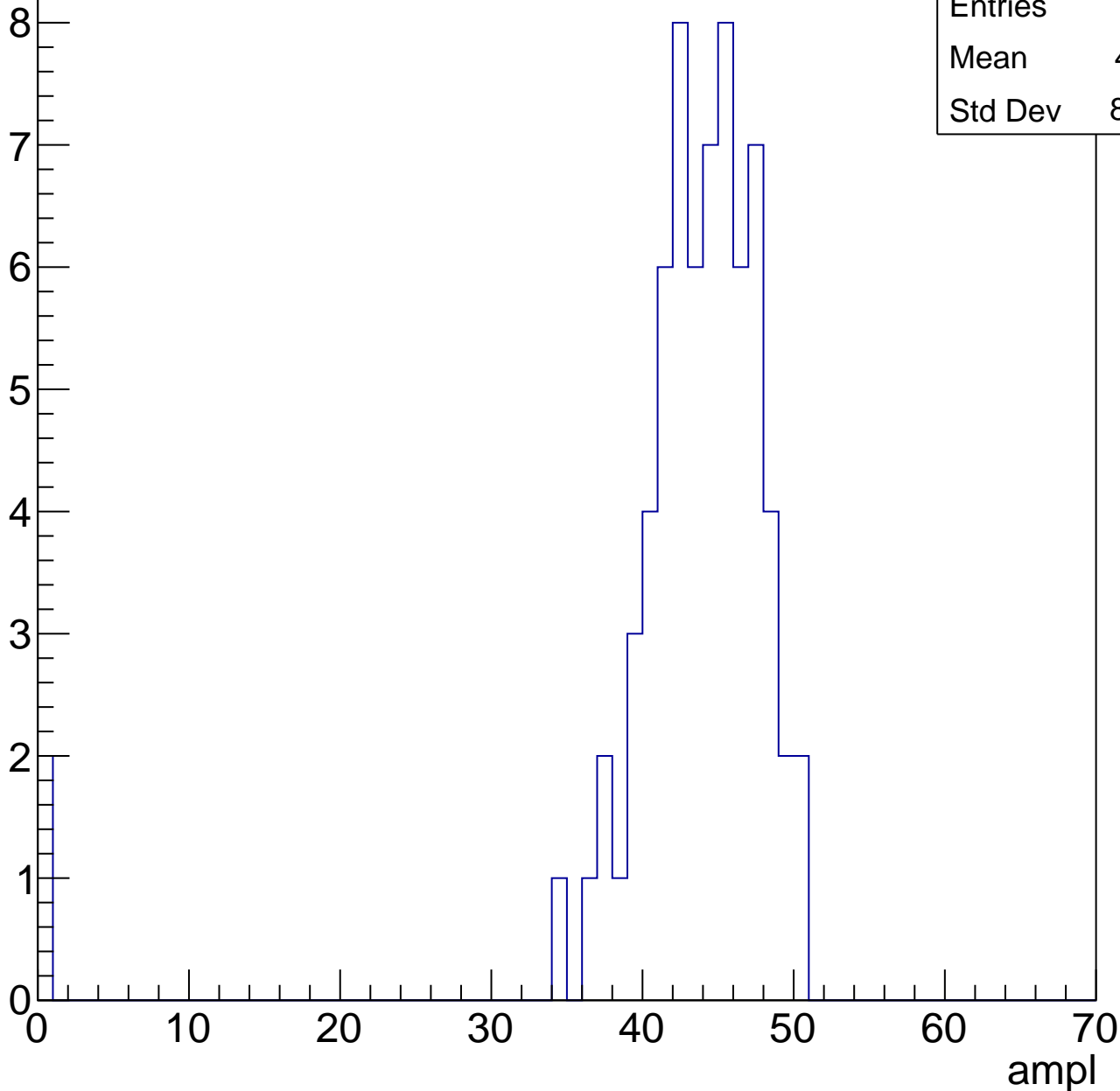


# B1L103S, U25-ch67, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	70
Mean	42.31
Std Dev	8.003

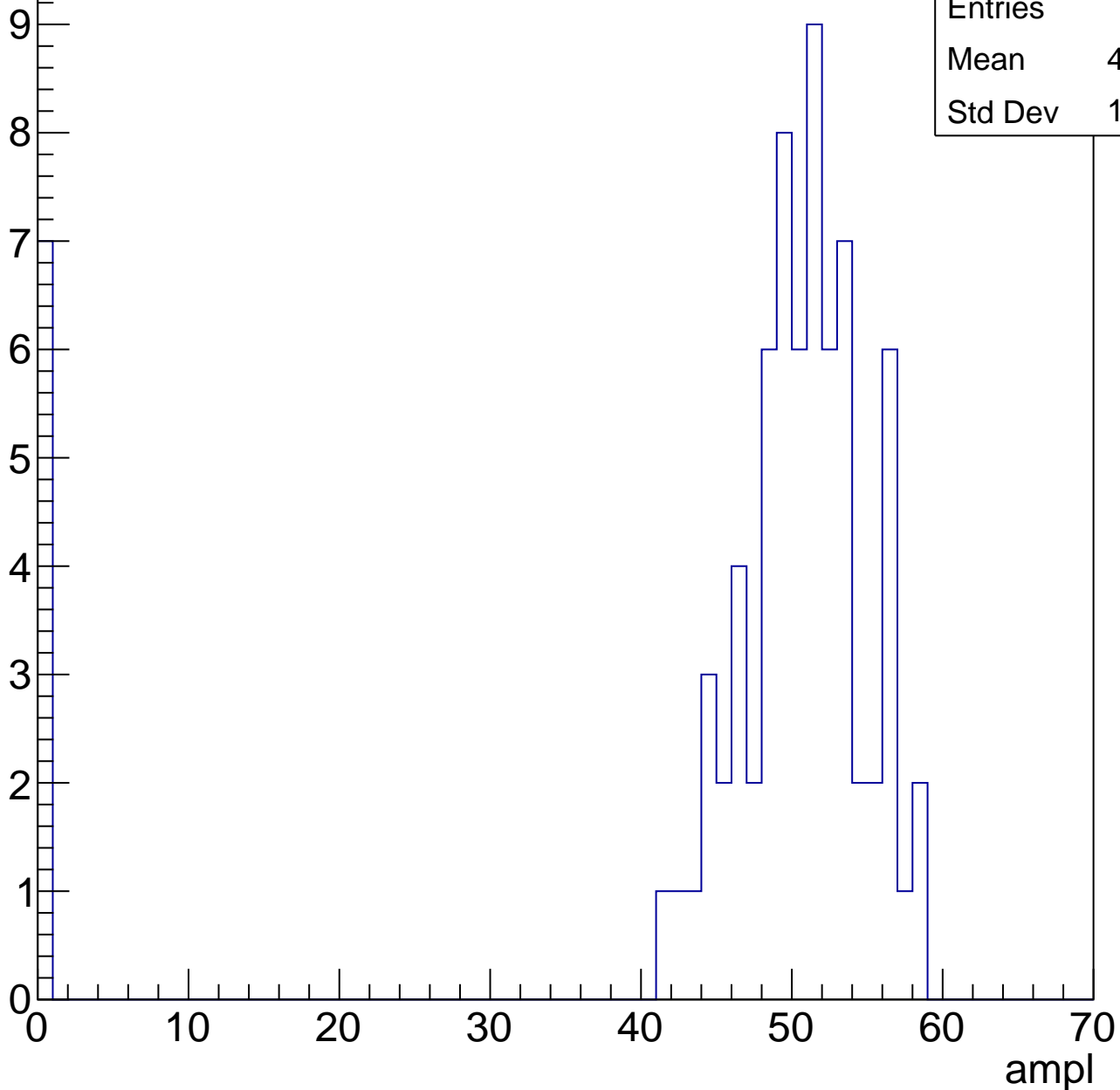


# B1L103S, U25-ch67, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	76
Mean	45.72
Std Dev	15.02

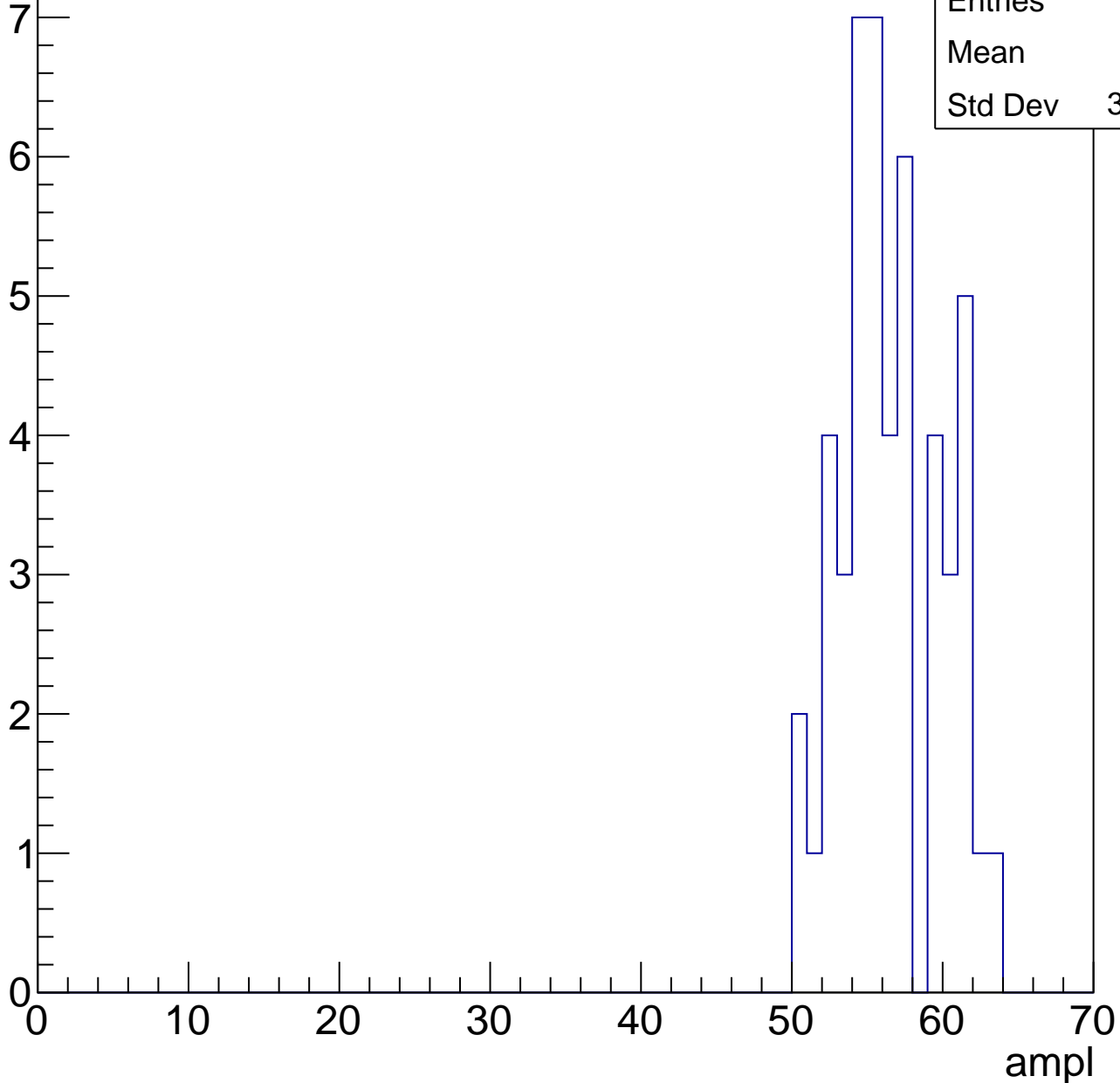


# B1L103S, U25-ch67, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

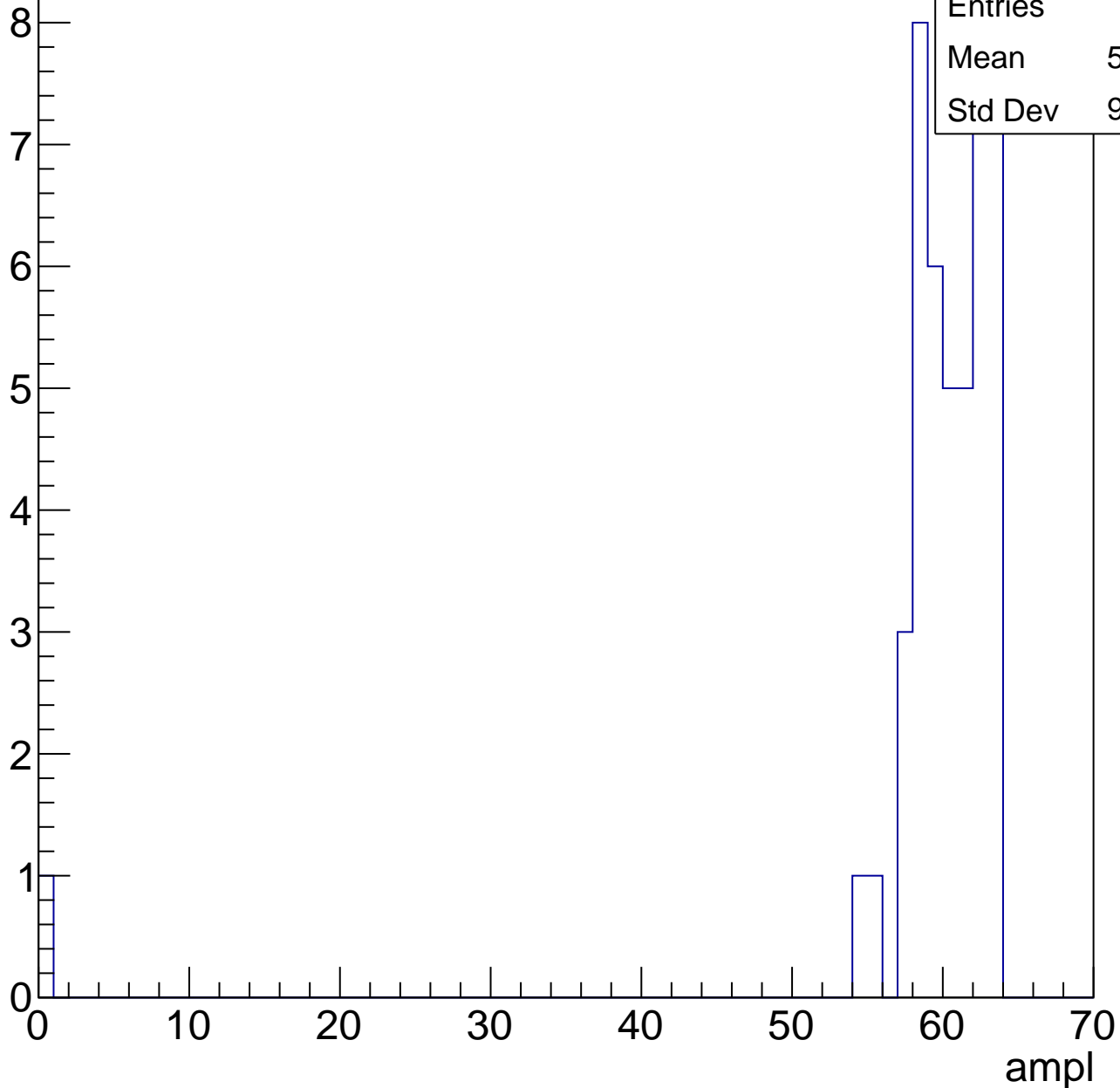
Entries	48
Mean	56.1
Std Dev	3.299



# B1L103S, U25-ch67, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U25-ch67, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	61.25
Std Dev	1.299

ampl

0 10 20 30 40 50 60 70

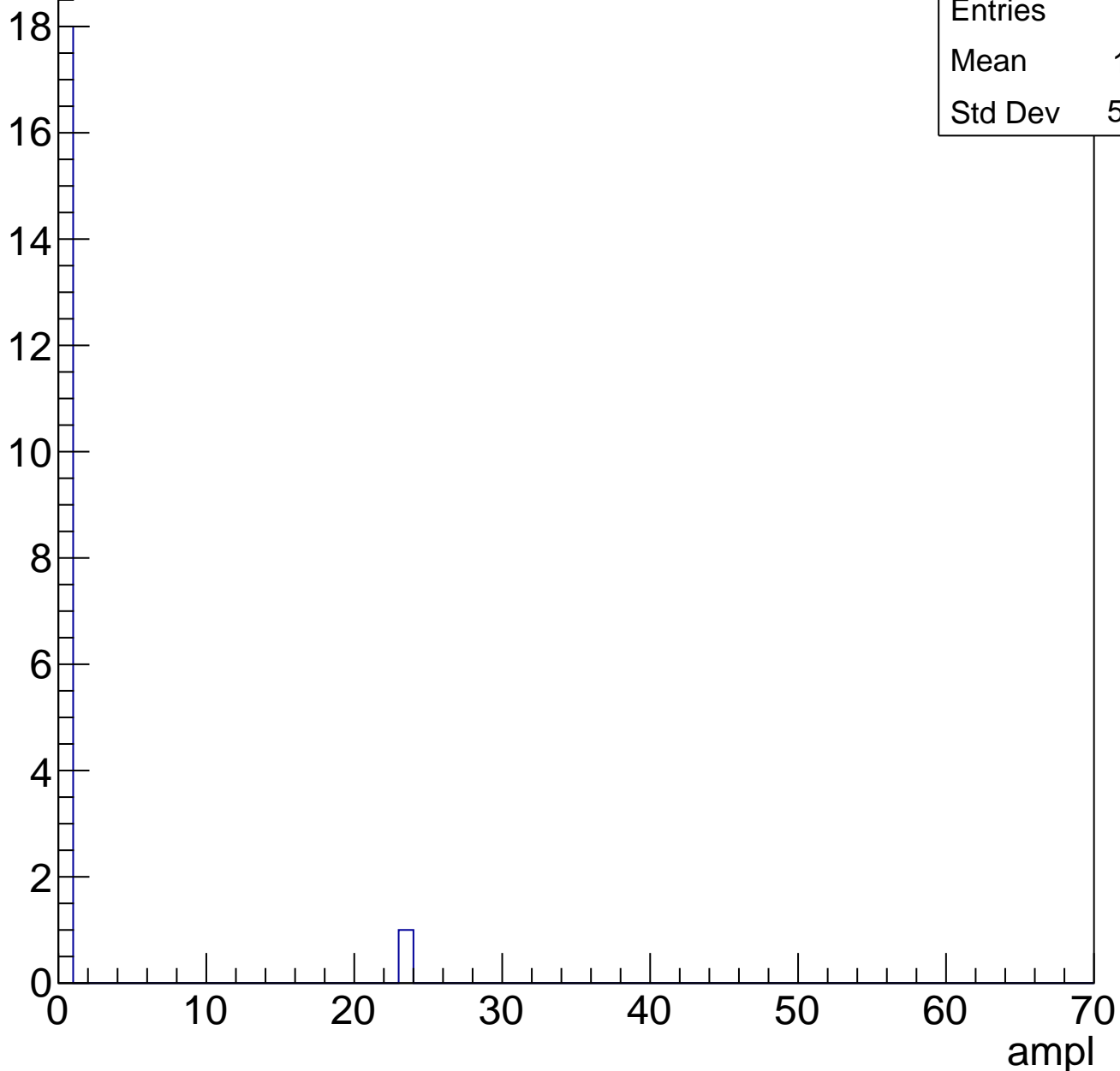


# B1L103S, U25-ch67, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	19
Mean	1.211
Std Dev	5.136

Entry



# B1L103S, U25-ch68, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	76
Mean	20.58
Std Dev	11.04

Entry

16  
14  
12  
10  
8  
6  
4  
2  
0

0

10

20

30

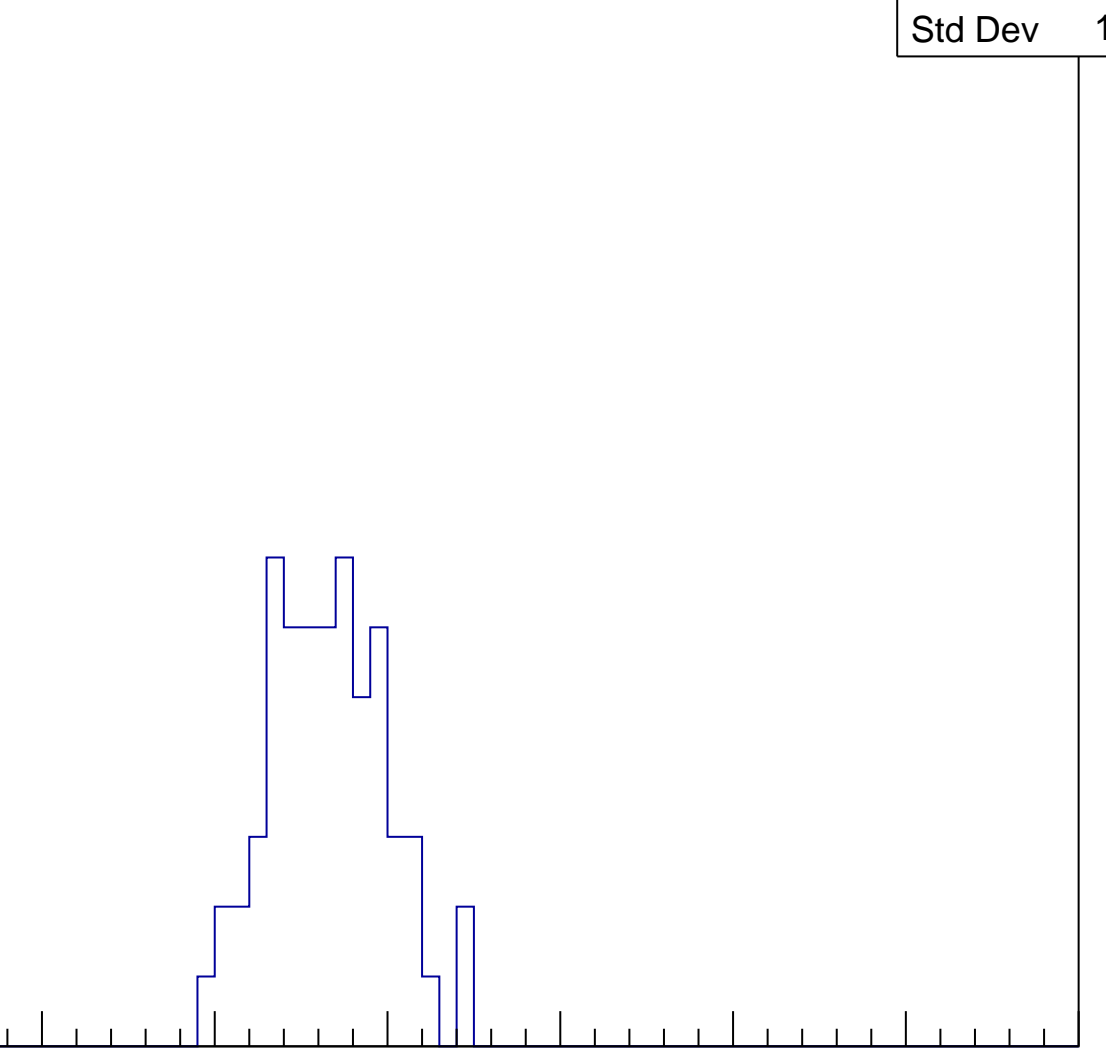
40

50

60

70

ampl

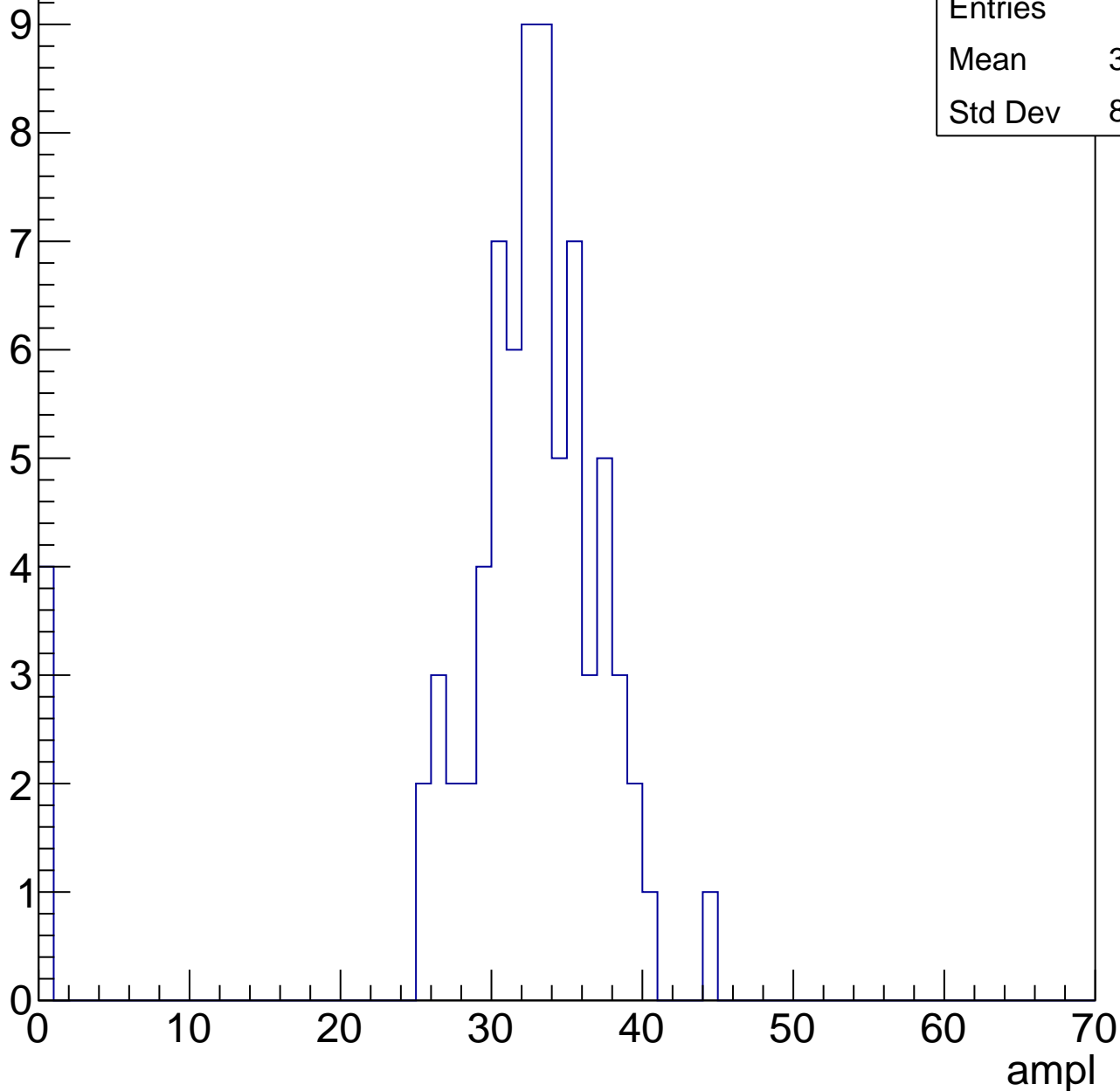


# B1L103S, U25-ch68, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	75
Mean	30.92
Std Dev	8.202

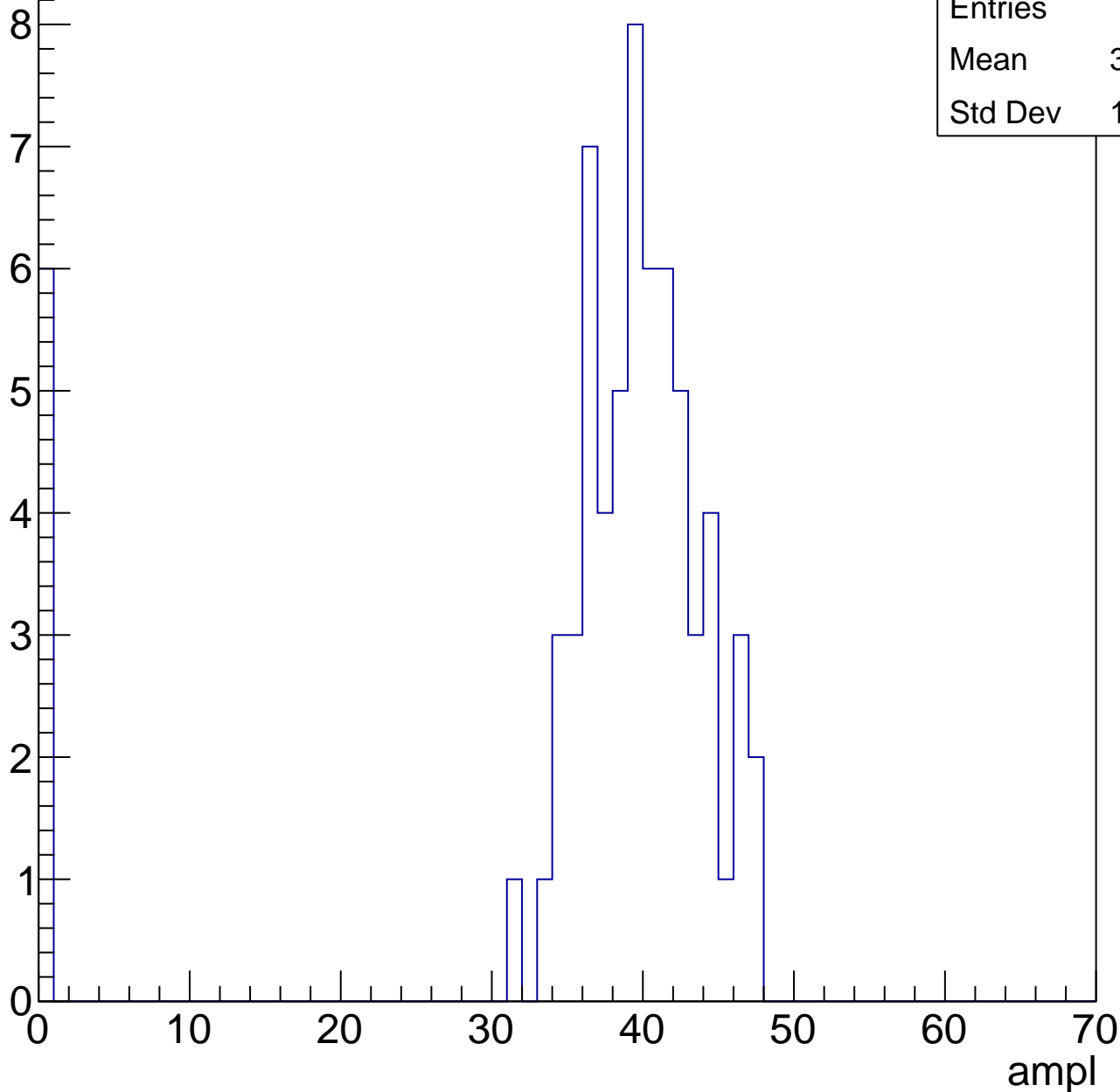


# B1L103S, U25-ch68, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	68
Mean	36.04
Std Dev	11.74

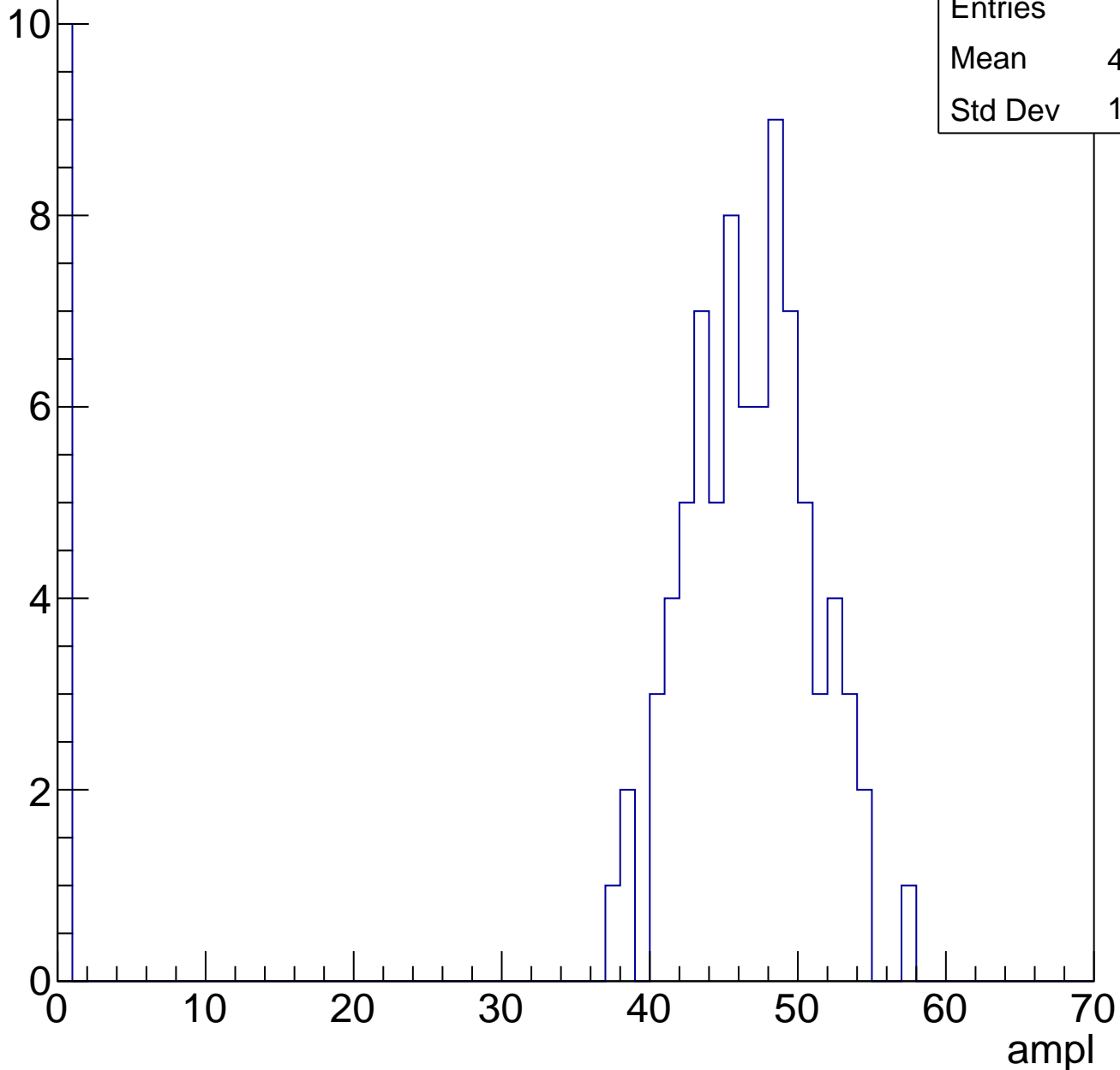


# B1L103S, U25-ch68, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	91
Mean	41.27
Std Dev	15.02

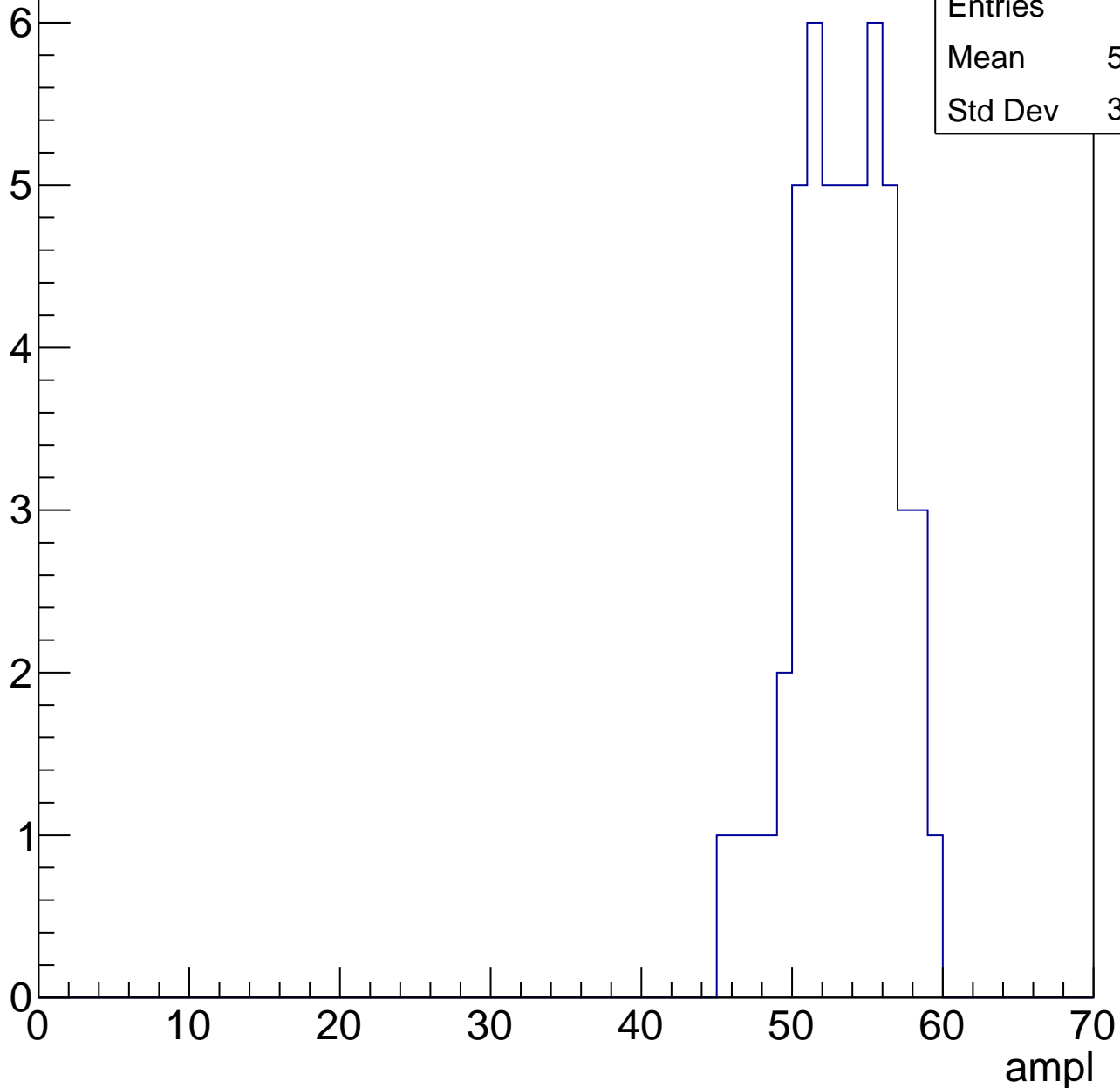
Entry



# B1L103S, U25-ch68, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



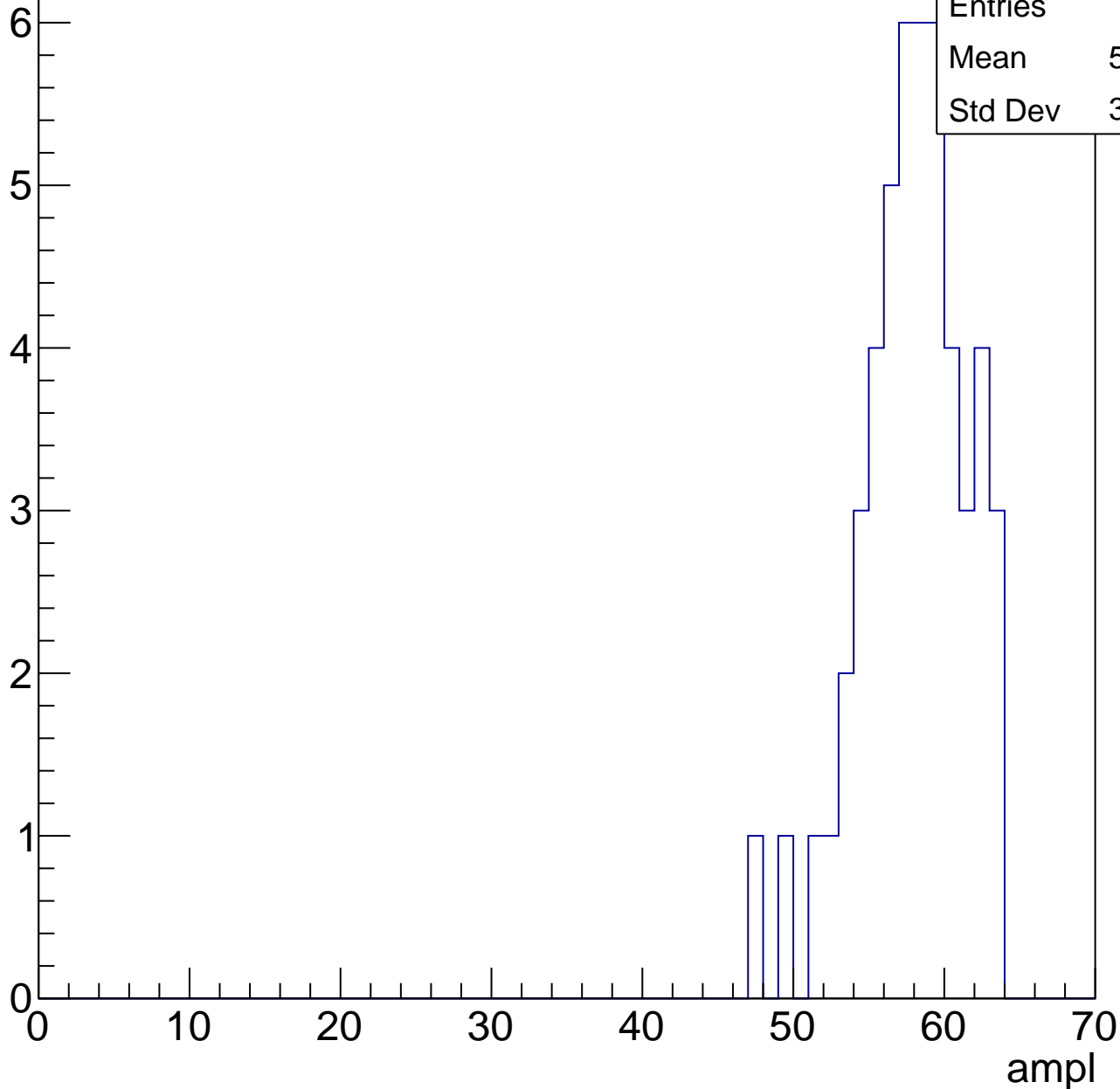
Entries	50
Mean	52.98
Std Dev	3.203

# B1L103S, U25-ch68, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

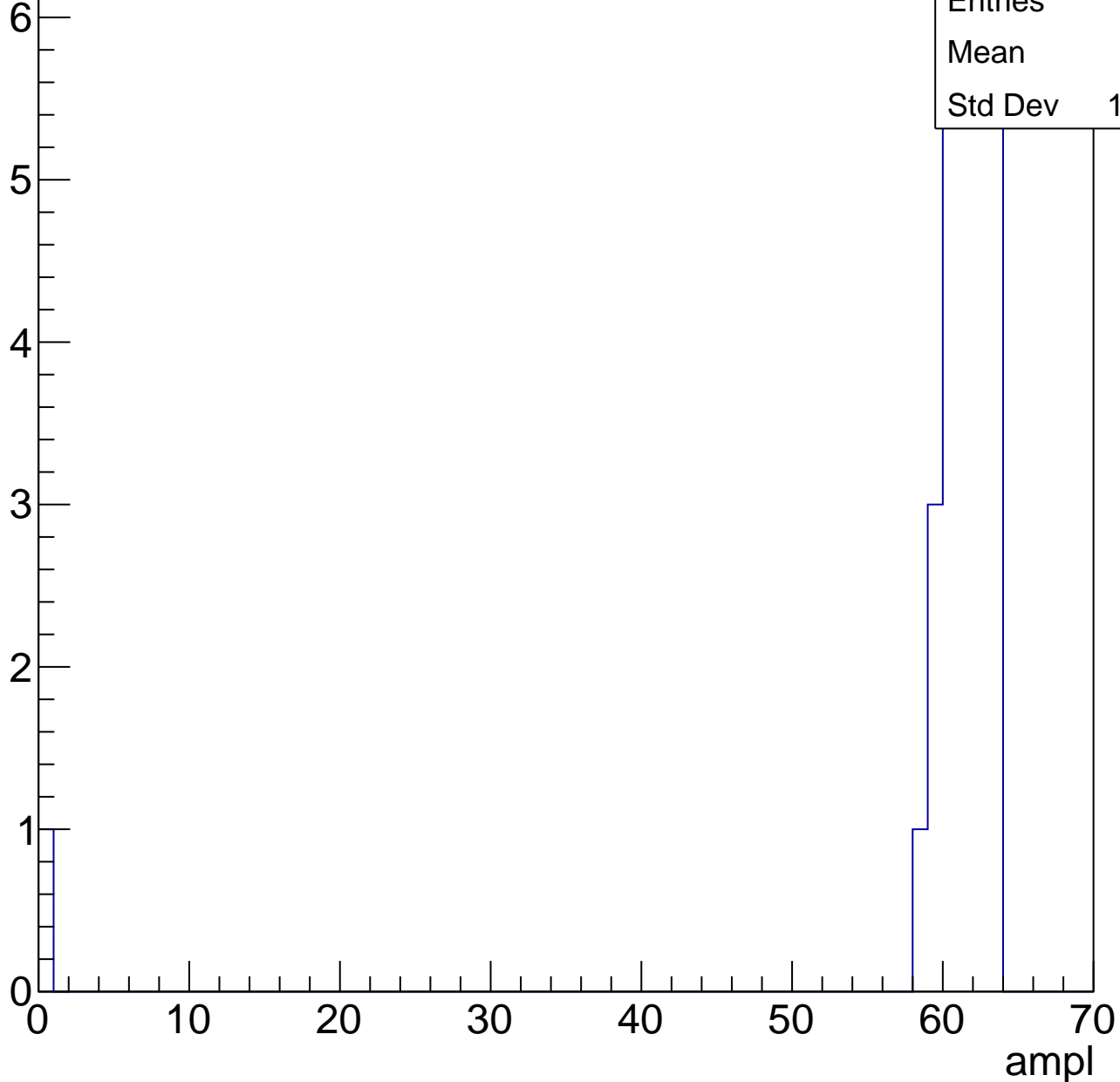
Entries	50
Mean	57.42
Std Dev	3.516



# B1L103S, U25-ch68, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U25-ch68, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	21
Mean	5.905
Std Dev	18.2

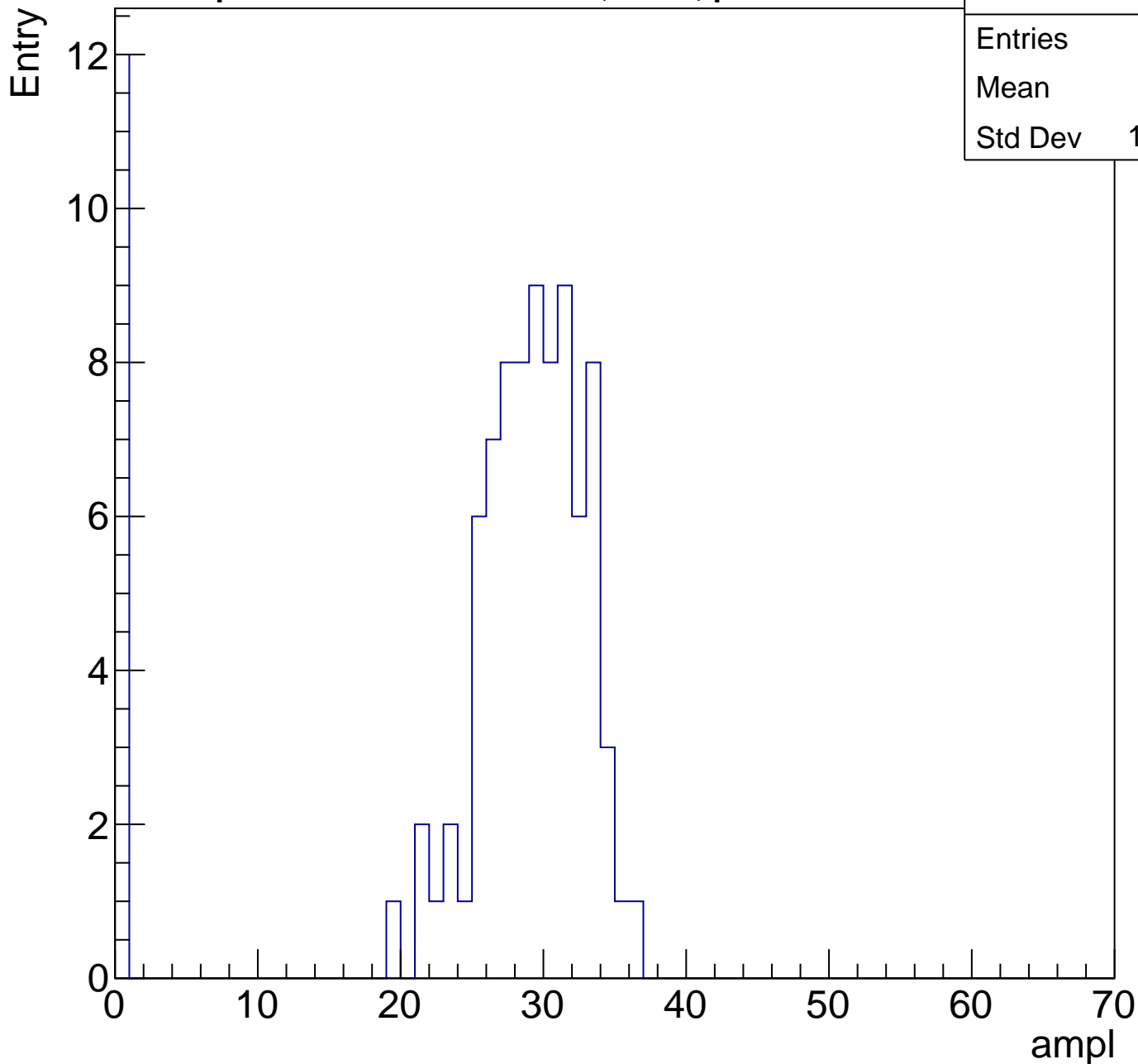
Entry



# B1L103S, U25-ch69, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	93
Mean	25.1
Std Dev	10.18

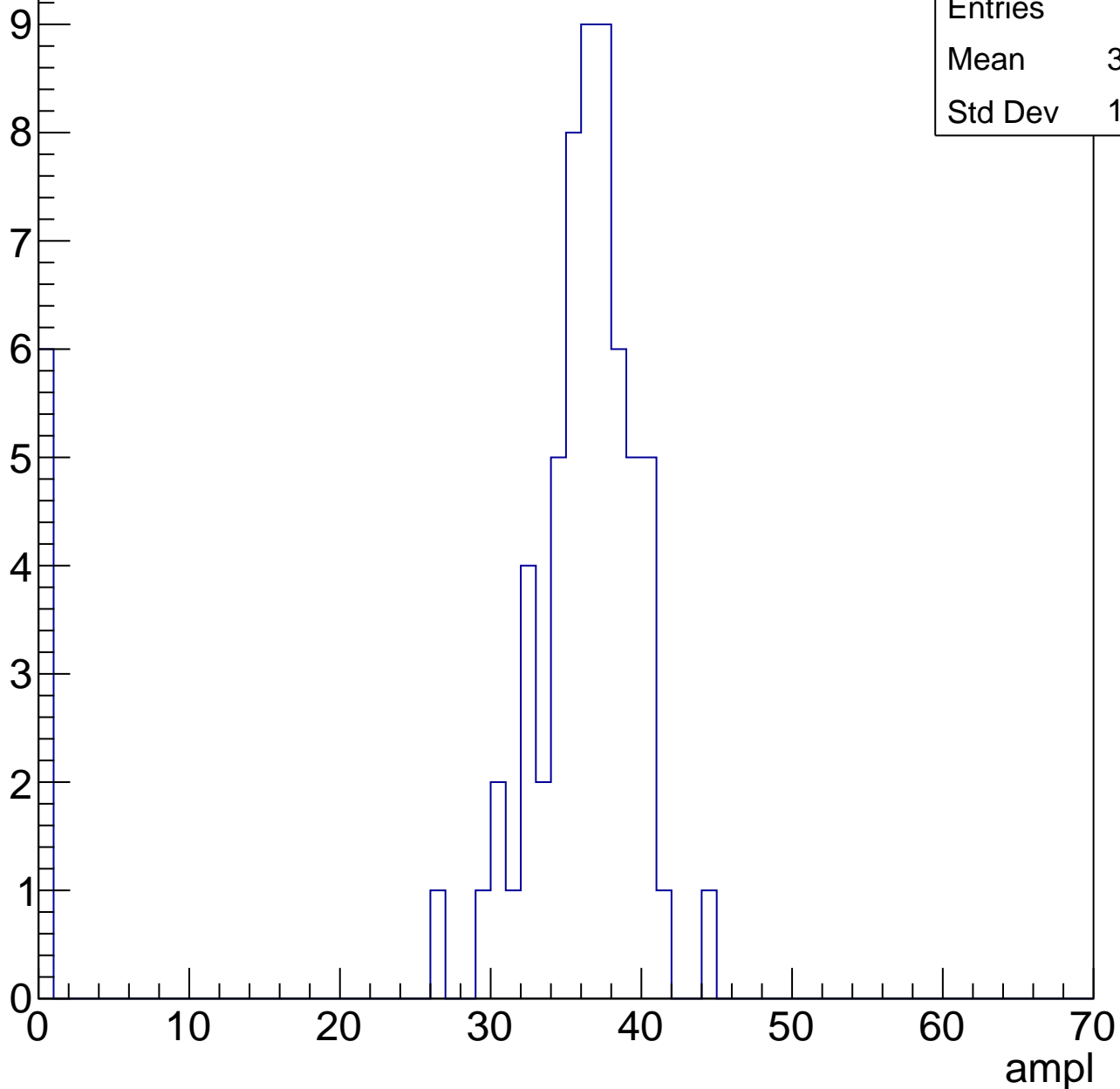


# B1L103S, U25-ch69, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	66
Mean	32.65
Std Dev	10.76

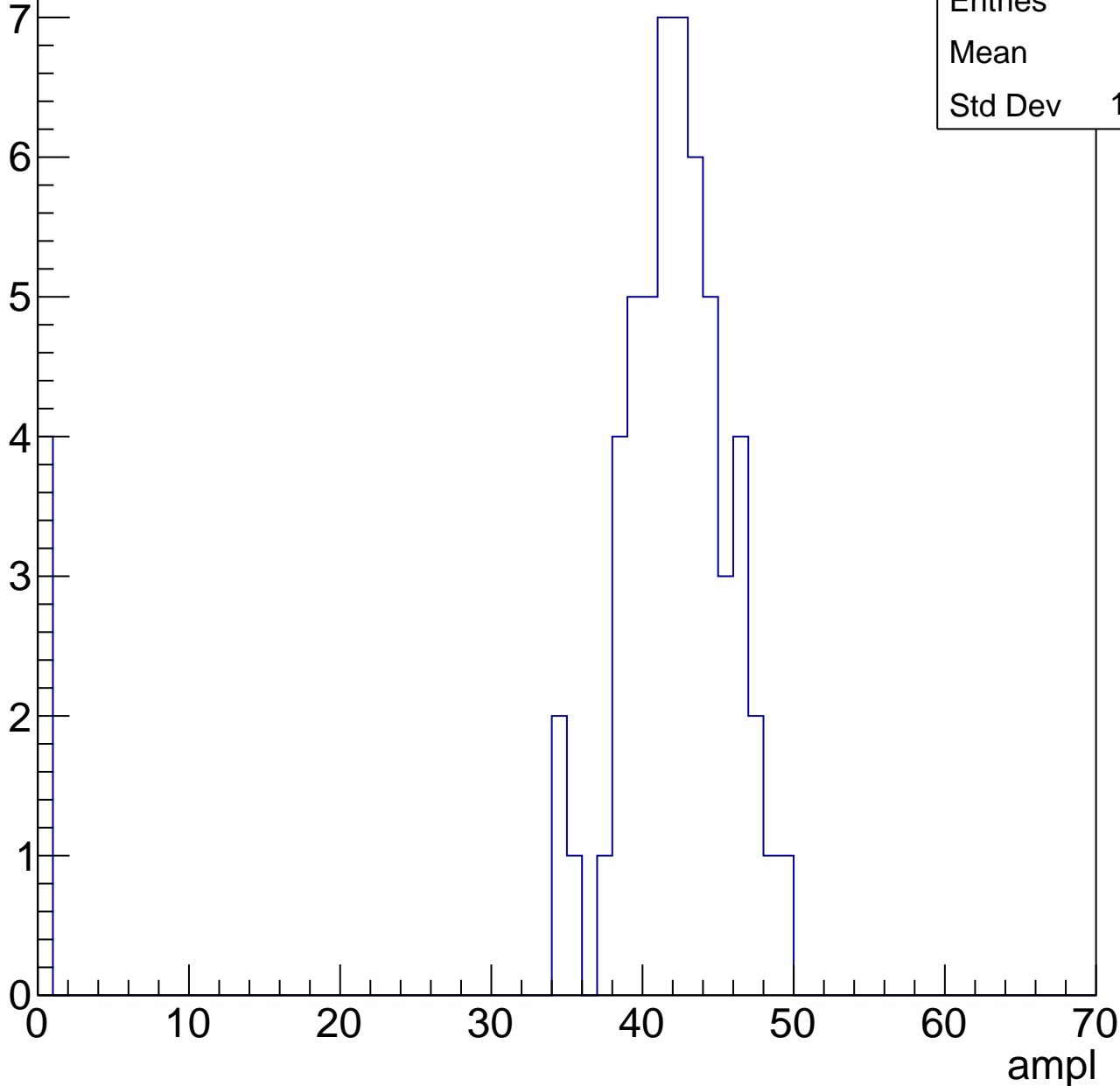


# B1L103S, U25-ch69, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	58
Mean	38.9
Std Dev	11.05

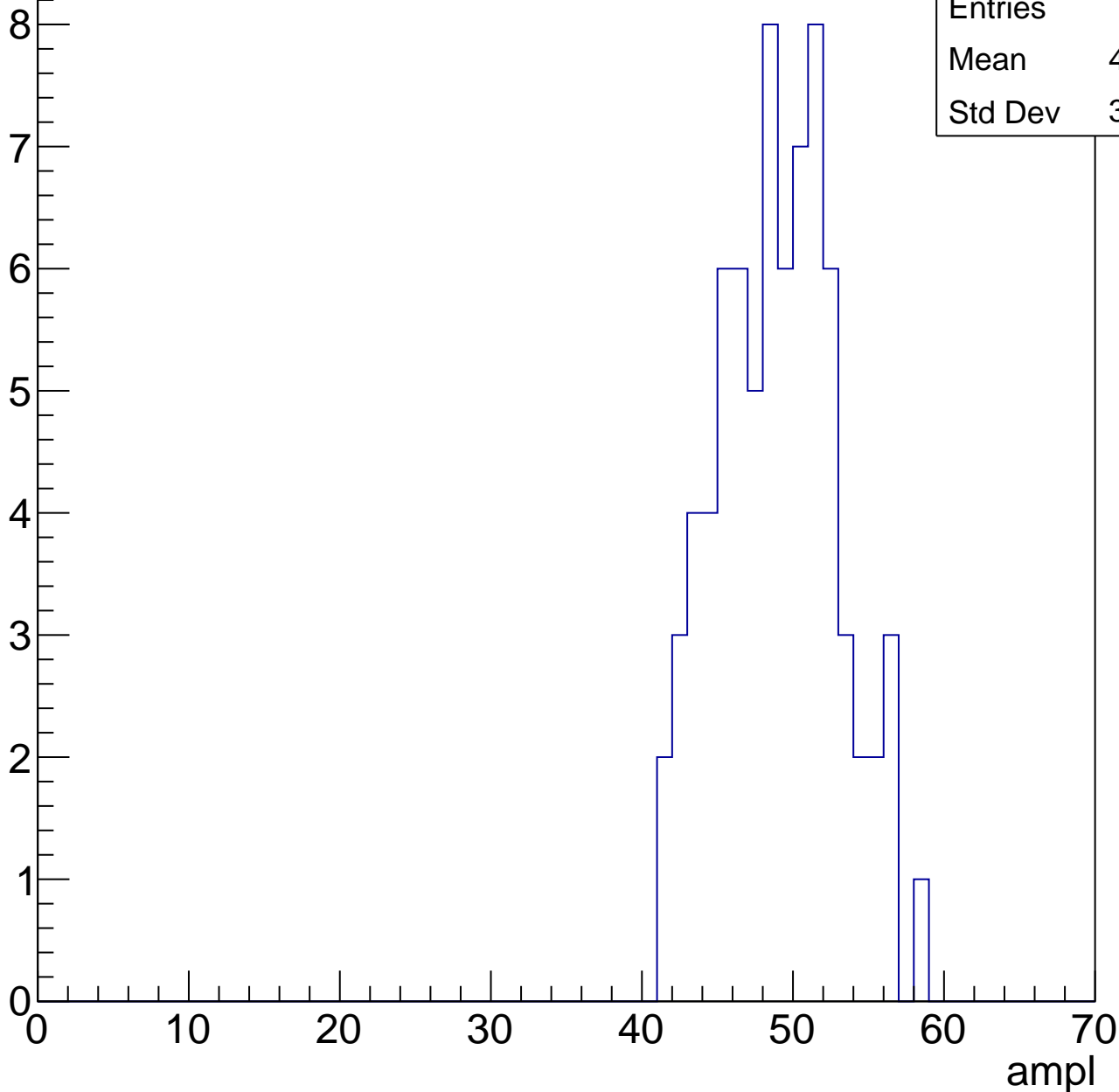


# B1L103S, U25-ch69, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	76
Mean	48.53
Std Dev	3.925

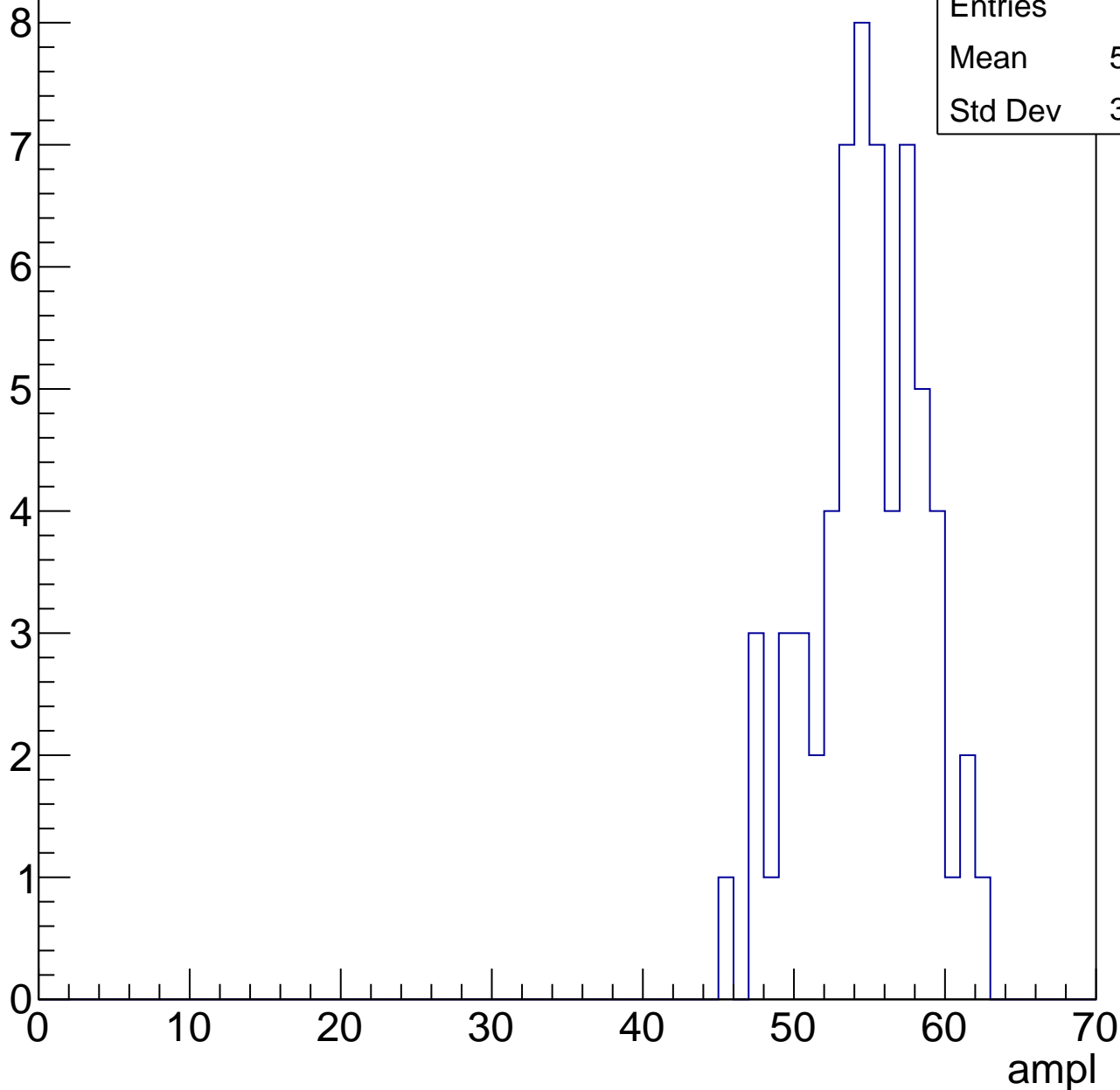


# B1L103S, U25-ch69, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

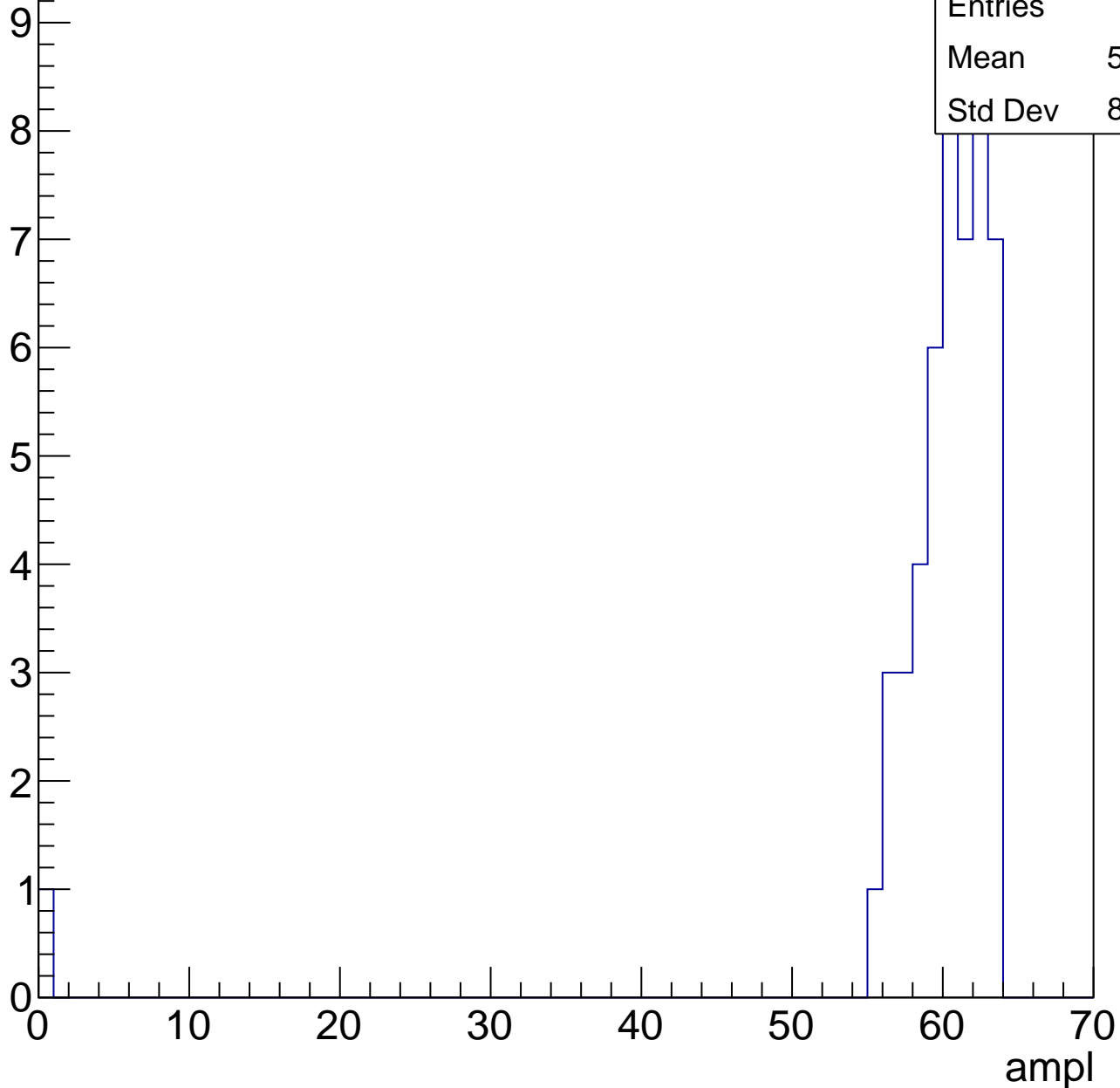
Entries	63
Mean	54.32
Std Dev	3.749



# B1L103S, U25-ch69, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U25-ch69, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U25-ch69, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

# B1L103S, U25-ch70, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	85
Mean	23.29
Std Dev	9.645

Entry

10

8

6

4

2

0

0

10

20

30

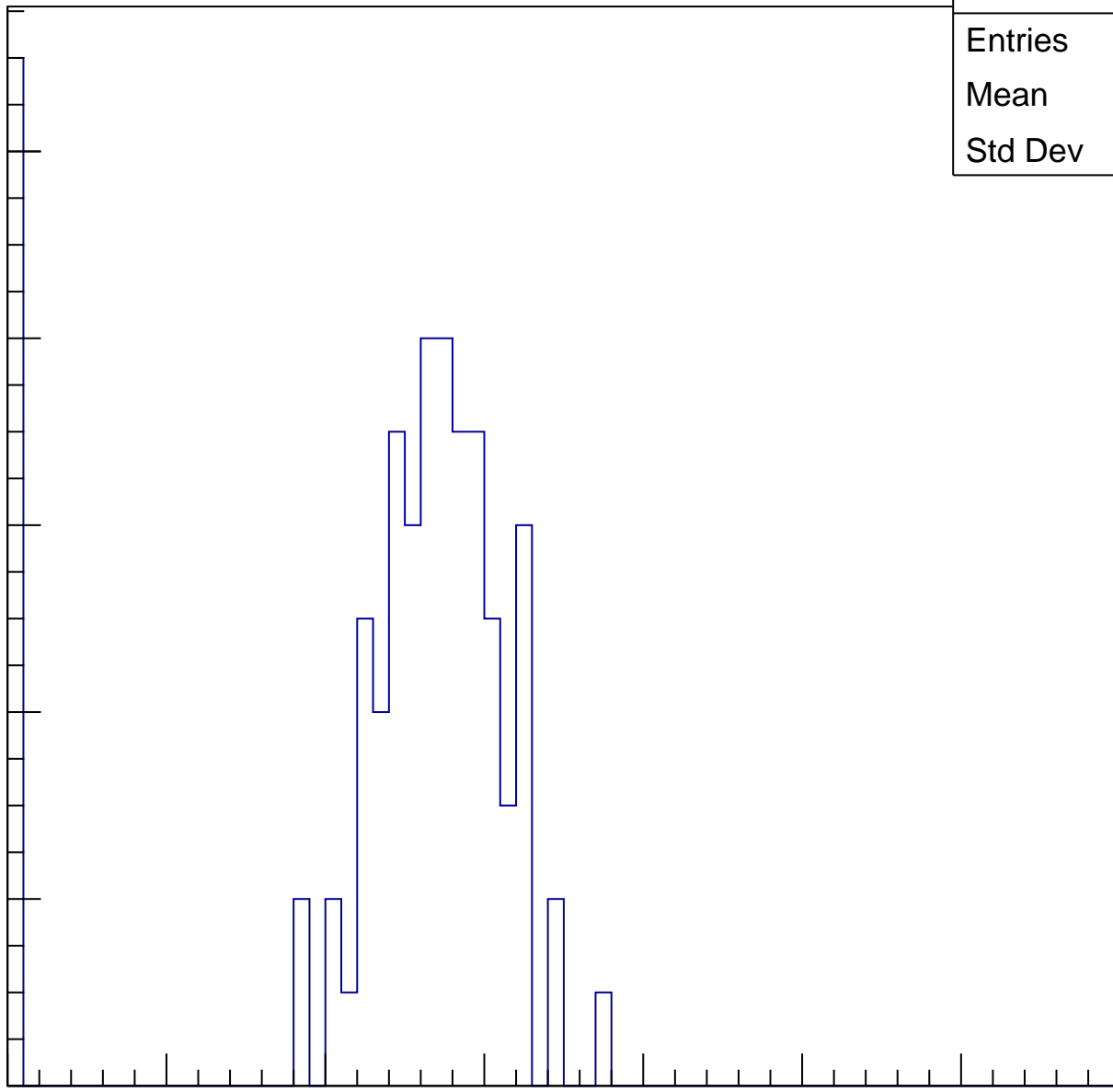
40

50

60

70

ampl

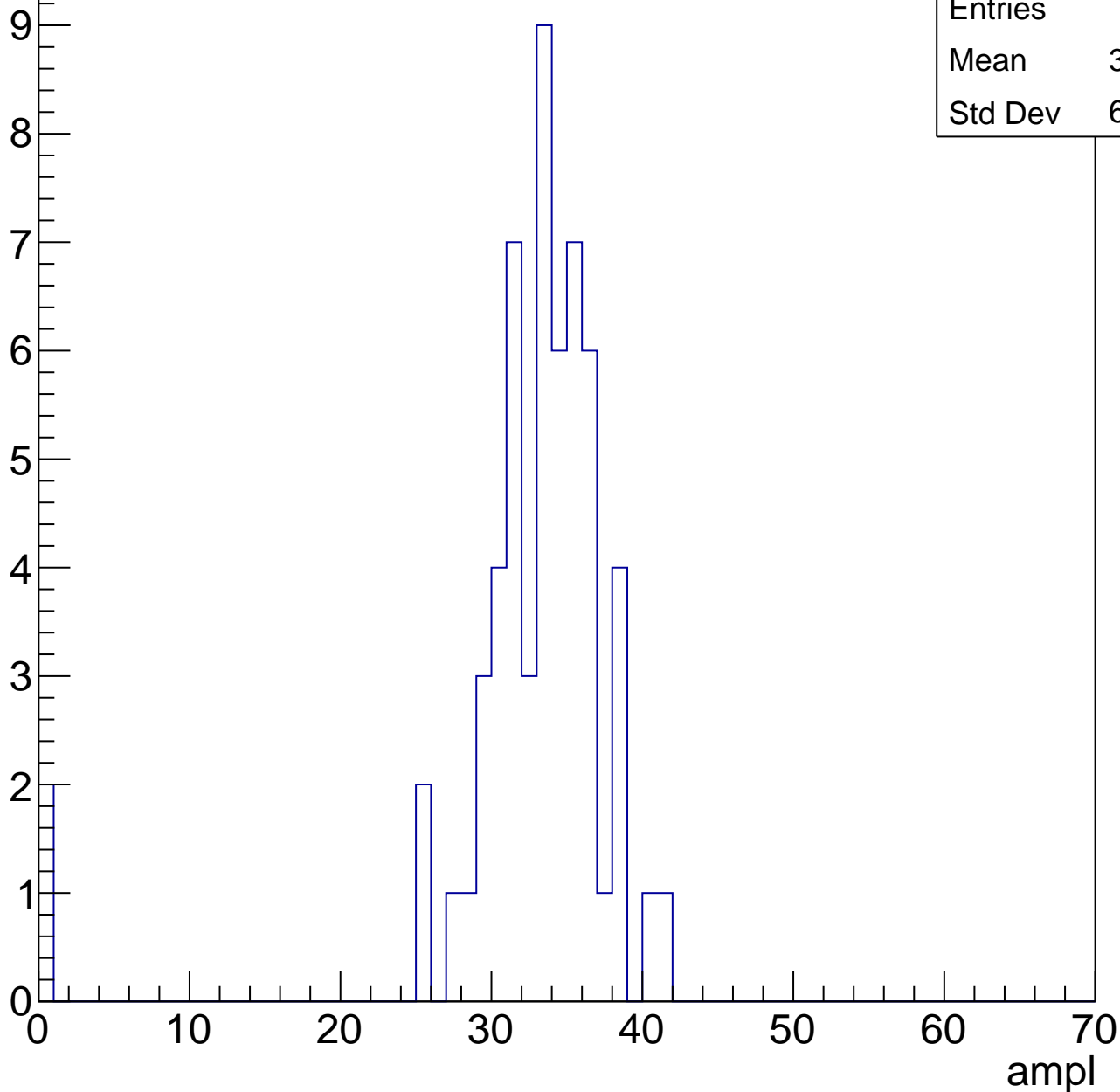


# B1L103S, U25-ch70, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	58
Mean	32.02
Std Dev	6.877

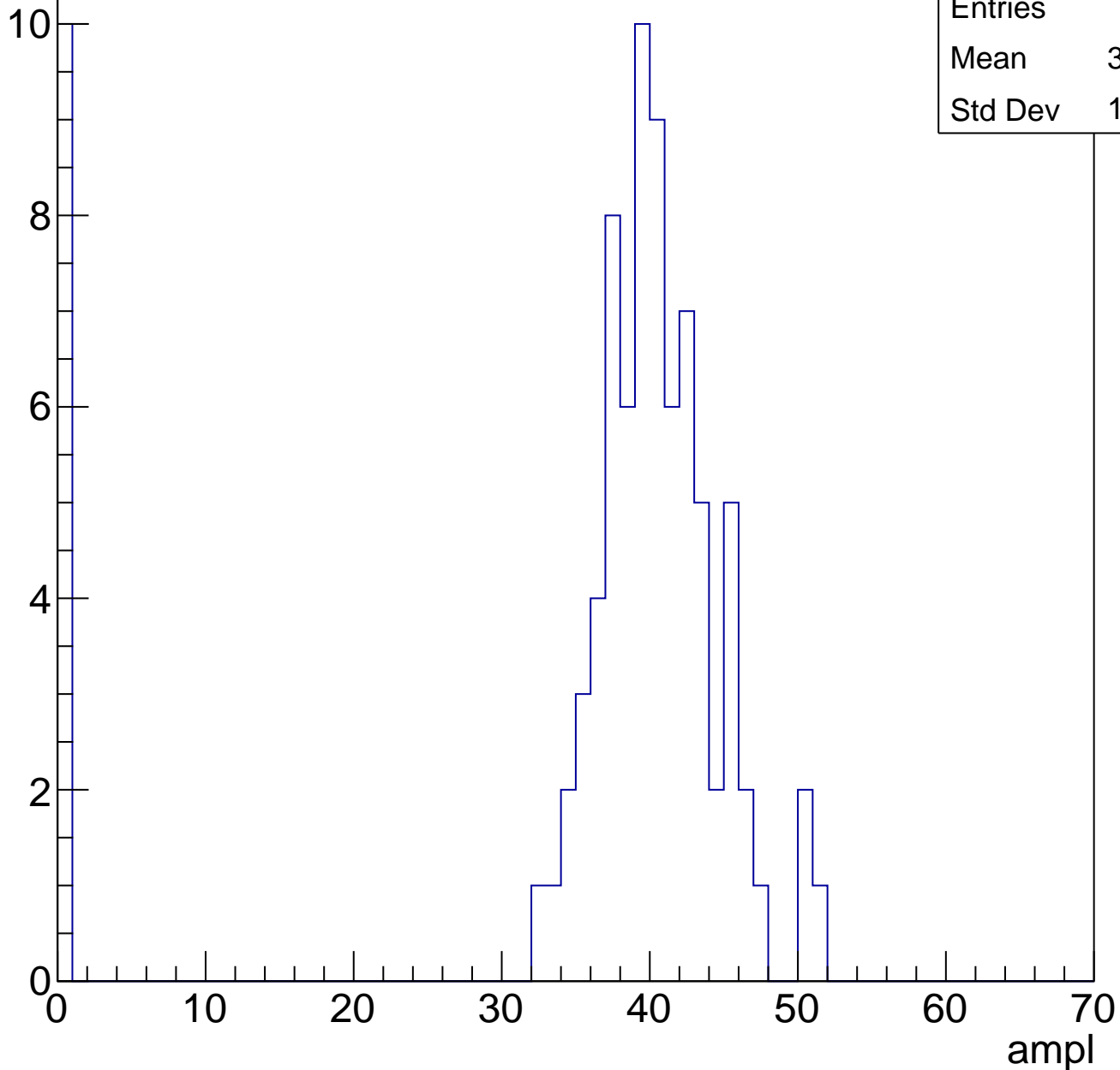


# B1L103S, U25-ch70, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	85
Mean	35.46
Std Dev	13.44

Entry

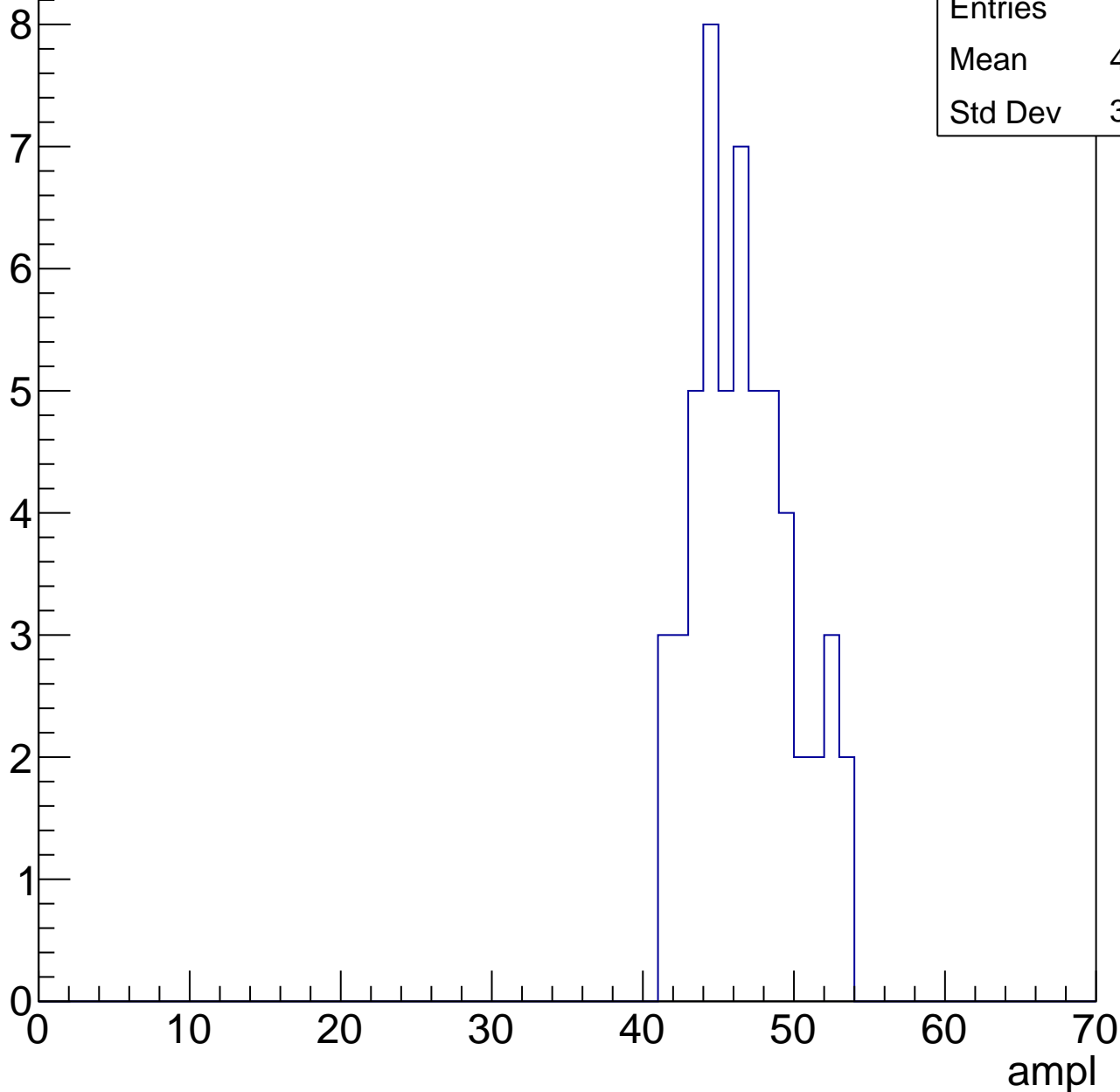


# B1L103S, U25-ch70, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	54
Mean	46.26
Std Dev	3.192

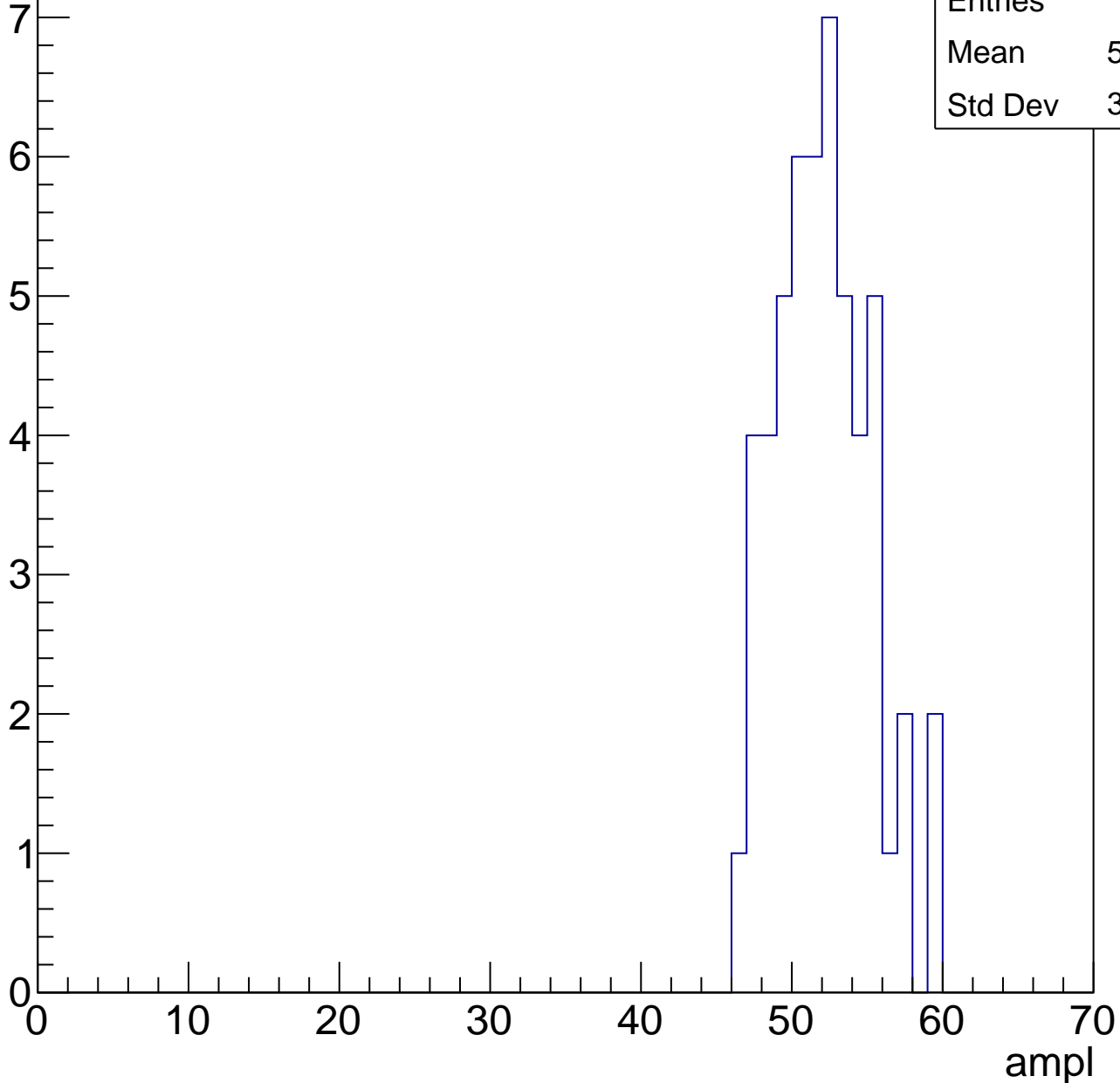


# B1L103S, U25-ch70, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	52
Mean	51.63
Std Dev	3.095

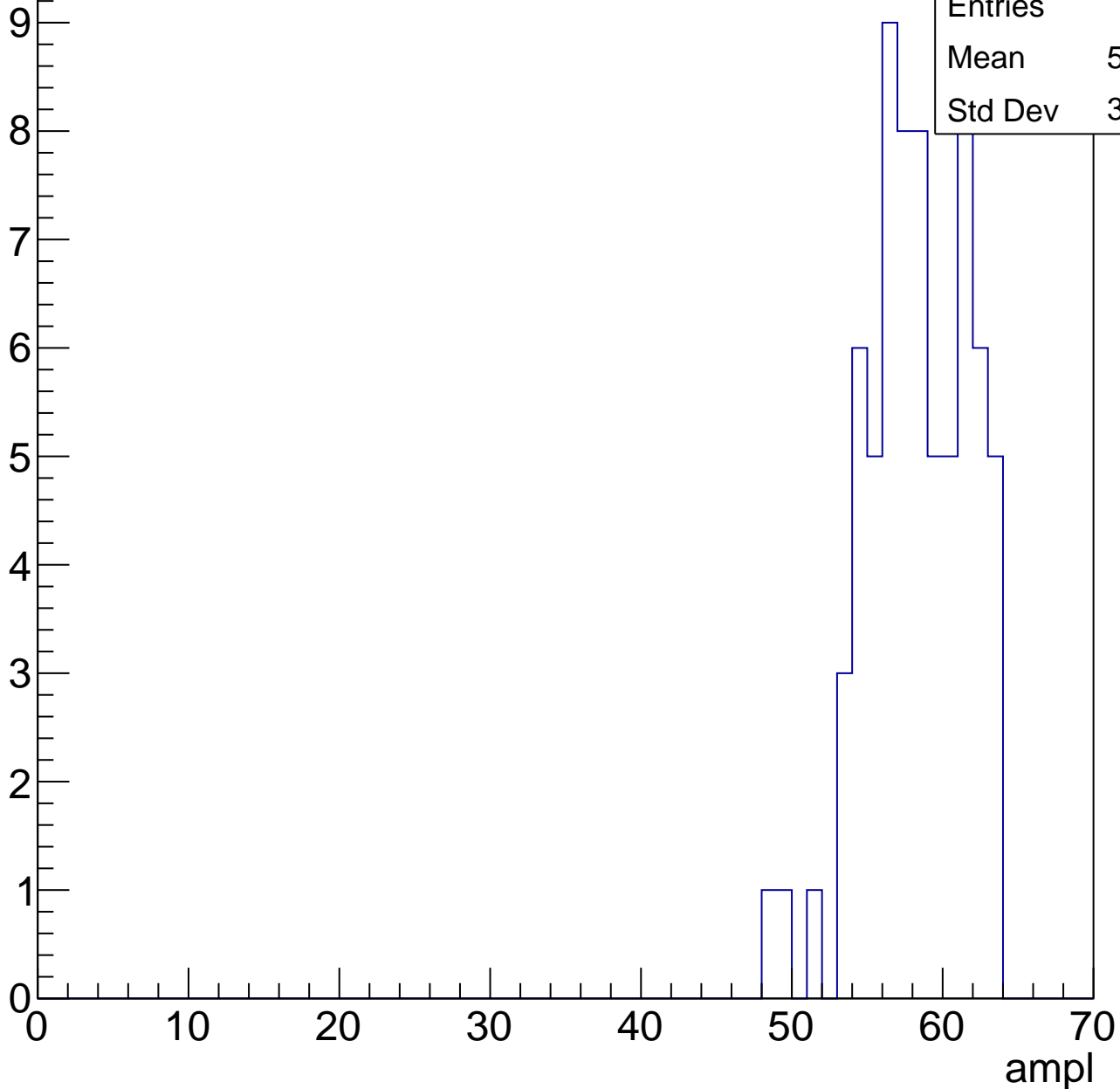


# B1L103S, U25-ch70, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	71
Mean	57.75
Std Dev	3.364

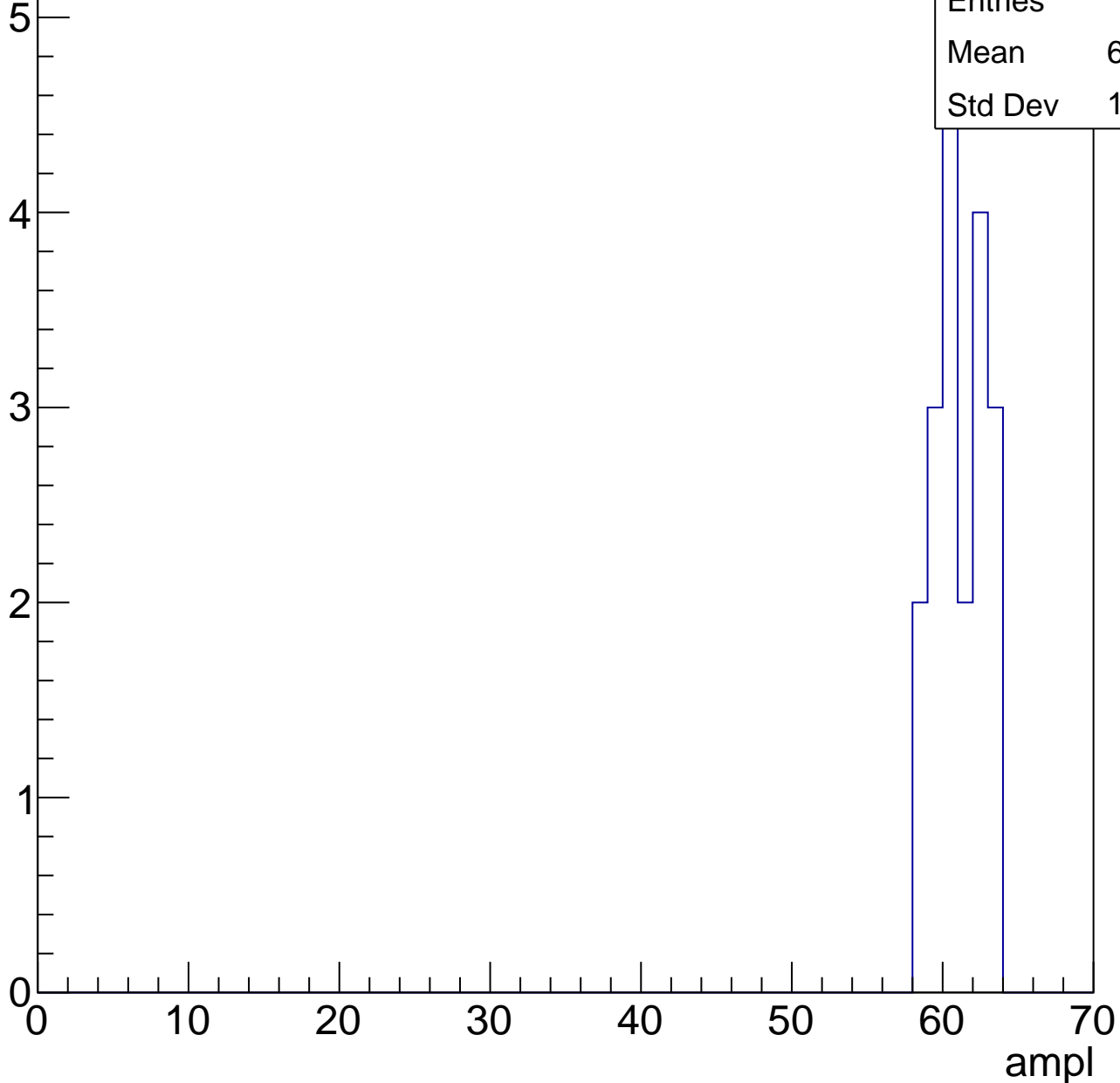


# B1L103S, U25-ch70, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	19
Mean	60.63
Std Dev	1.596





# B1L103S, U25-ch70, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	21
Mean	6
Std Dev	18.49

Entry



# B1L103S, U25-ch71, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	94
Mean	25.83
Std Dev	9.187

Entry

10  
8  
6  
4  
2  
0

0

10

20

30

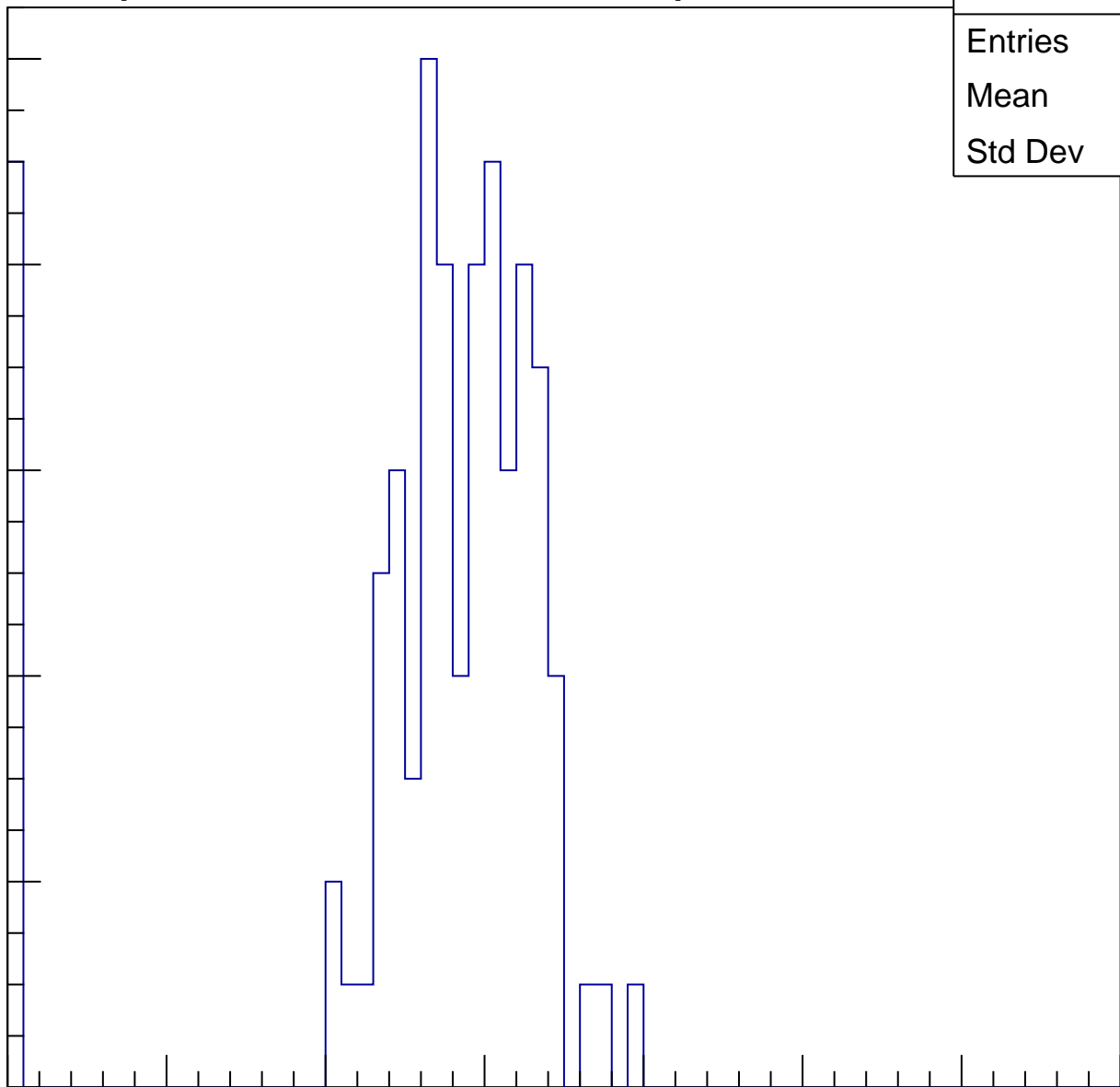
40

50

60

70

ampl

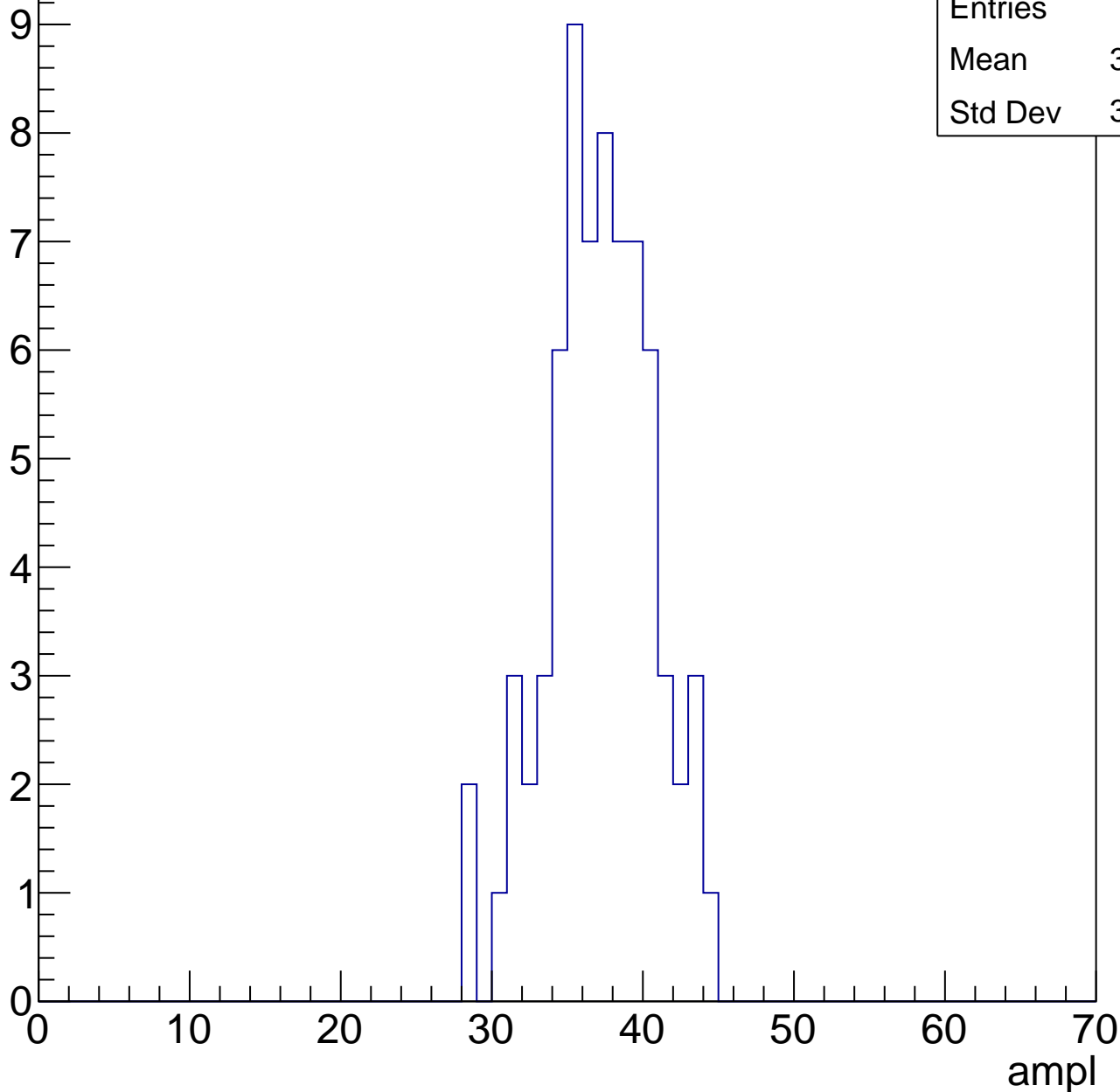


# B1L103S, U25-ch71, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	70
Mean	36.69
Std Dev	3.487

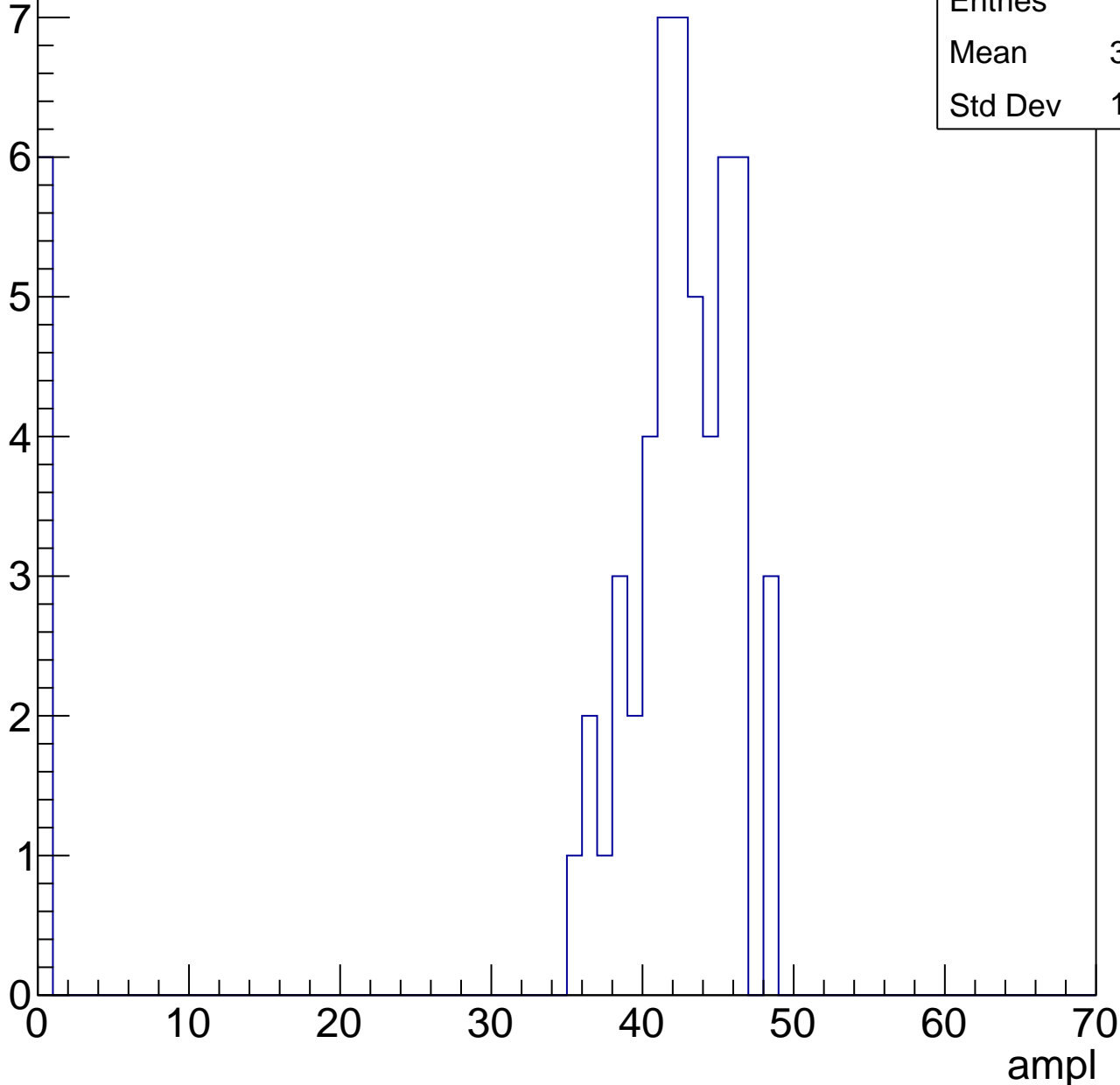


# B1L103S, U25-ch71, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

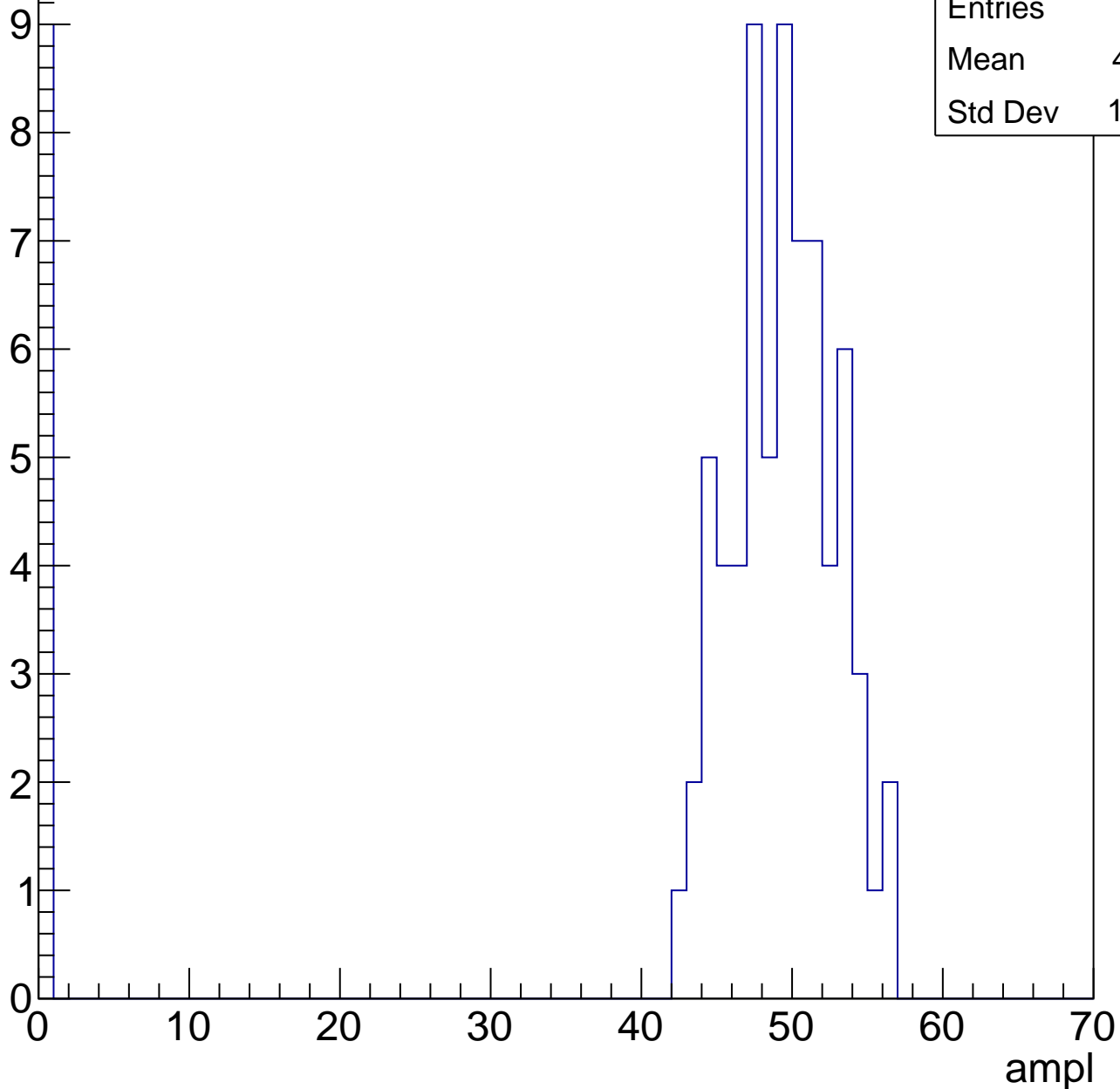
Entries	57
Mean	37.86
Std Dev	13.33



# B1L103S, U25-ch71, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



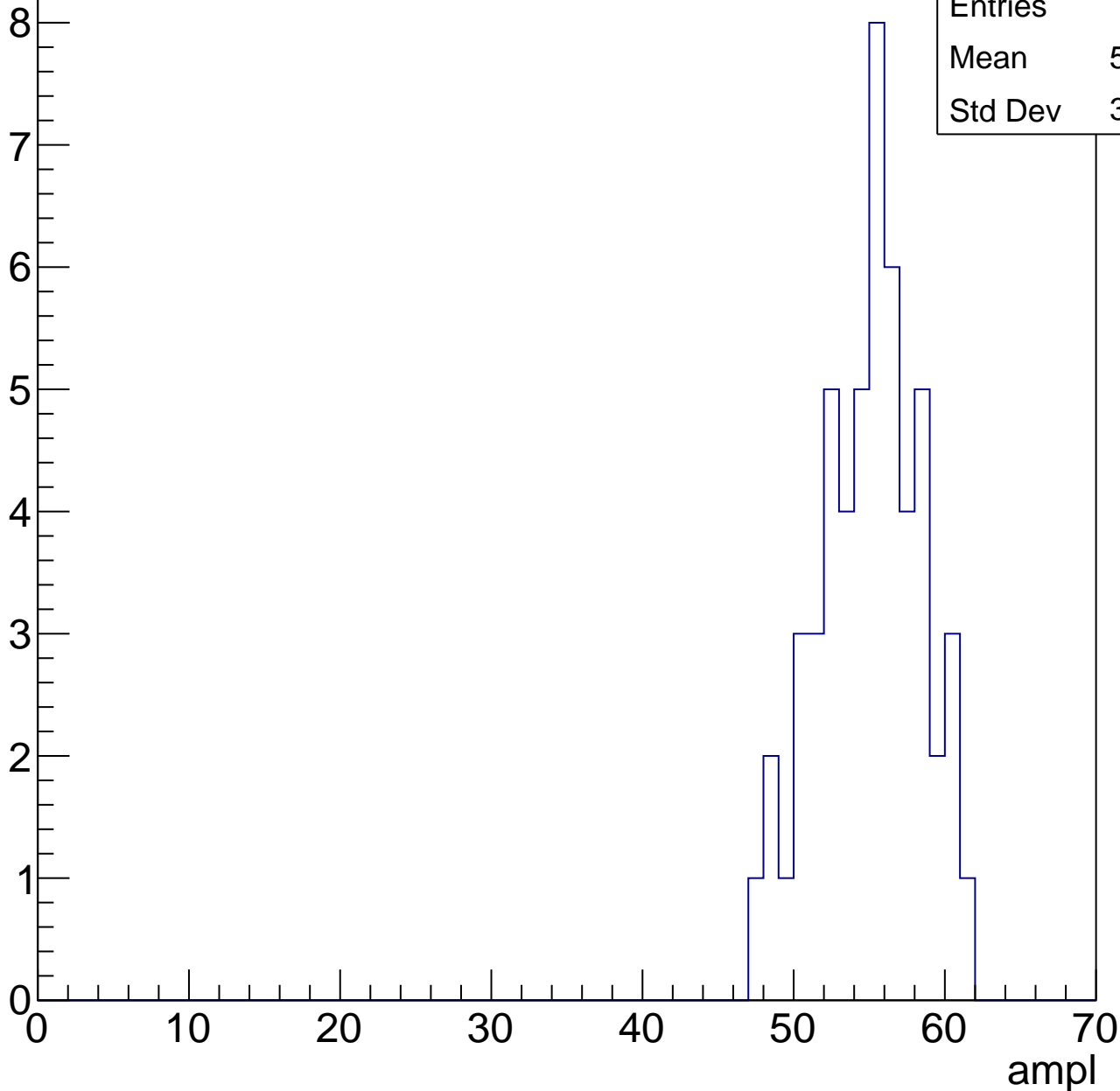
Entries	78
Mean	43.31
Std Dev	15.95

# B1L103S, U25-ch71, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

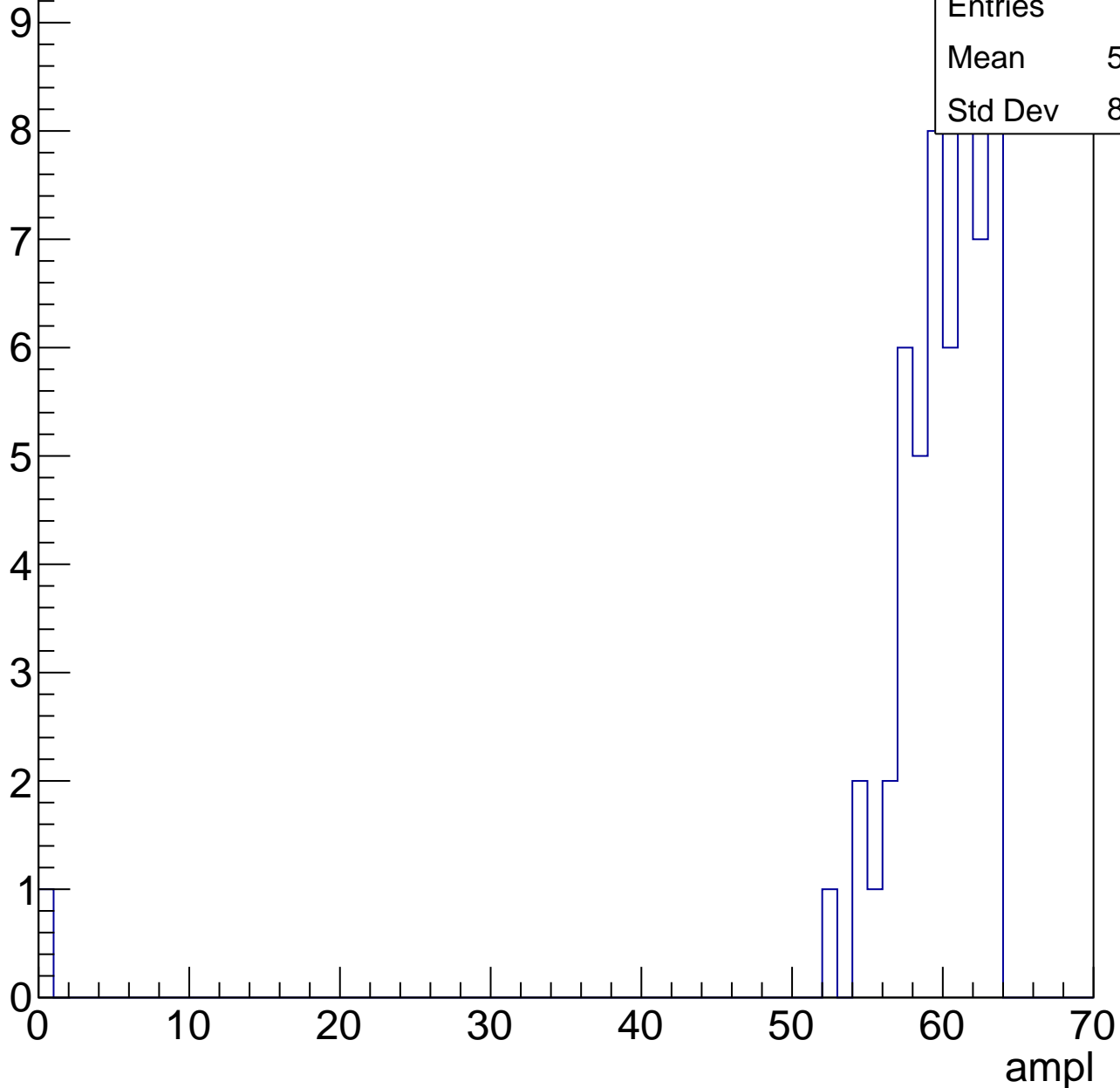
Entries	53
Mean	54.53
Std Dev	3.323



# B1L103S, U25-ch71, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	56
Mean	58.54
Std Dev	8.307

# B1L103S, U25-ch71, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U25-ch71, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	19
Mean	3.263
Std Dev	13.84

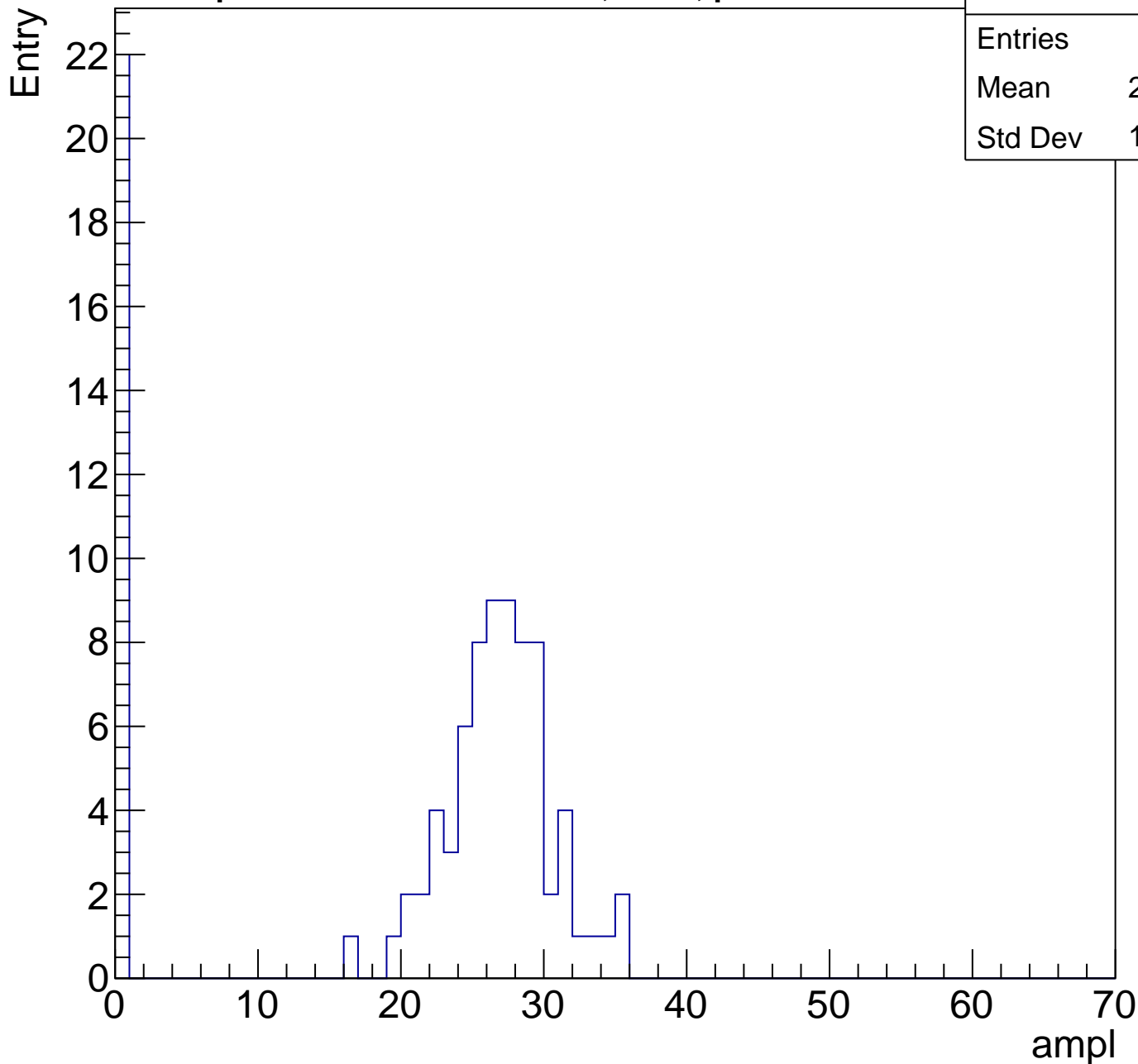
Entry



# B1L103S, U25-ch72, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	94
Mean	20.26
Std Dev	11.63

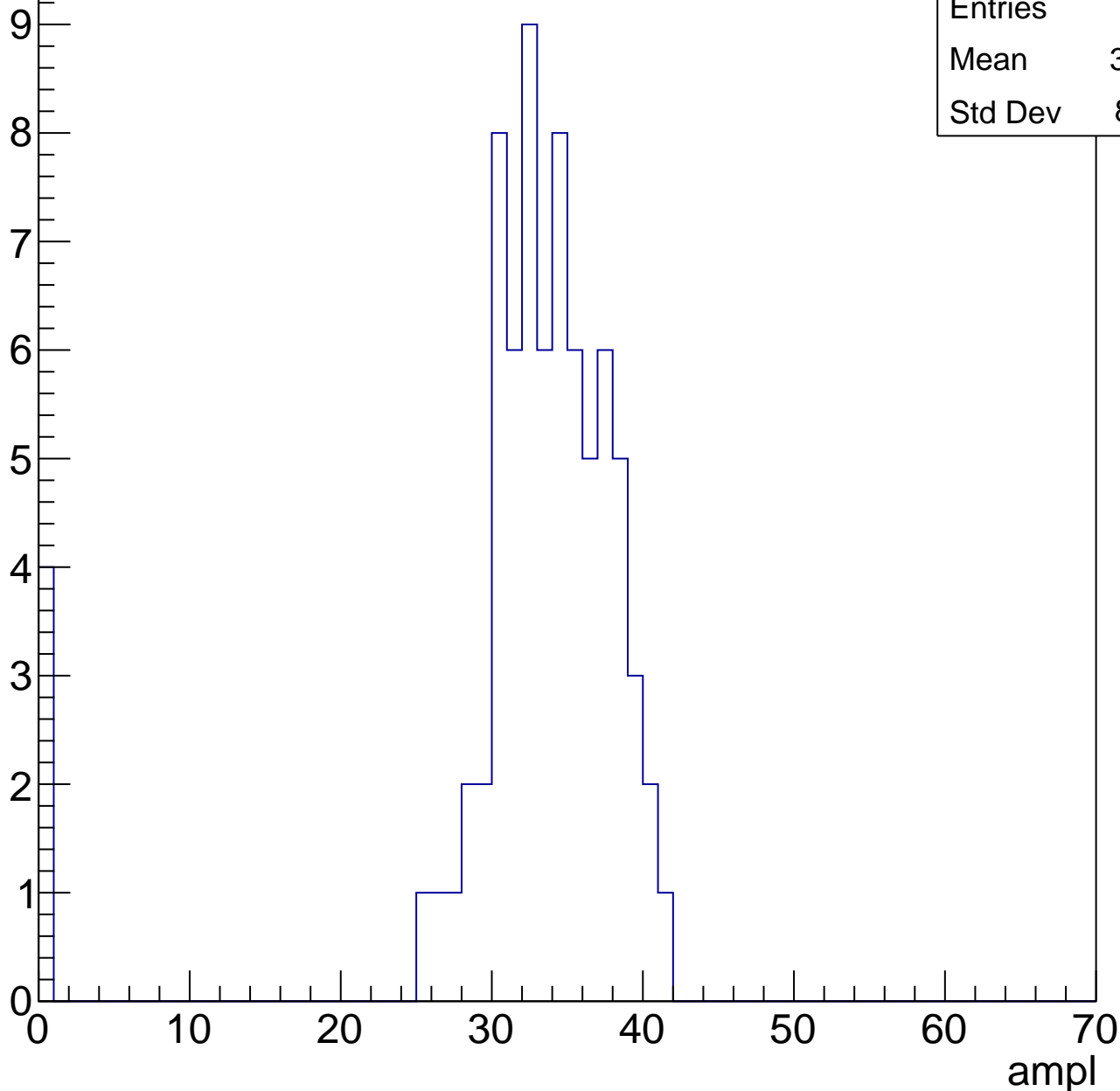


# B1L103S, U25-ch72, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	76
Mean	31.79
Std Dev	8.231

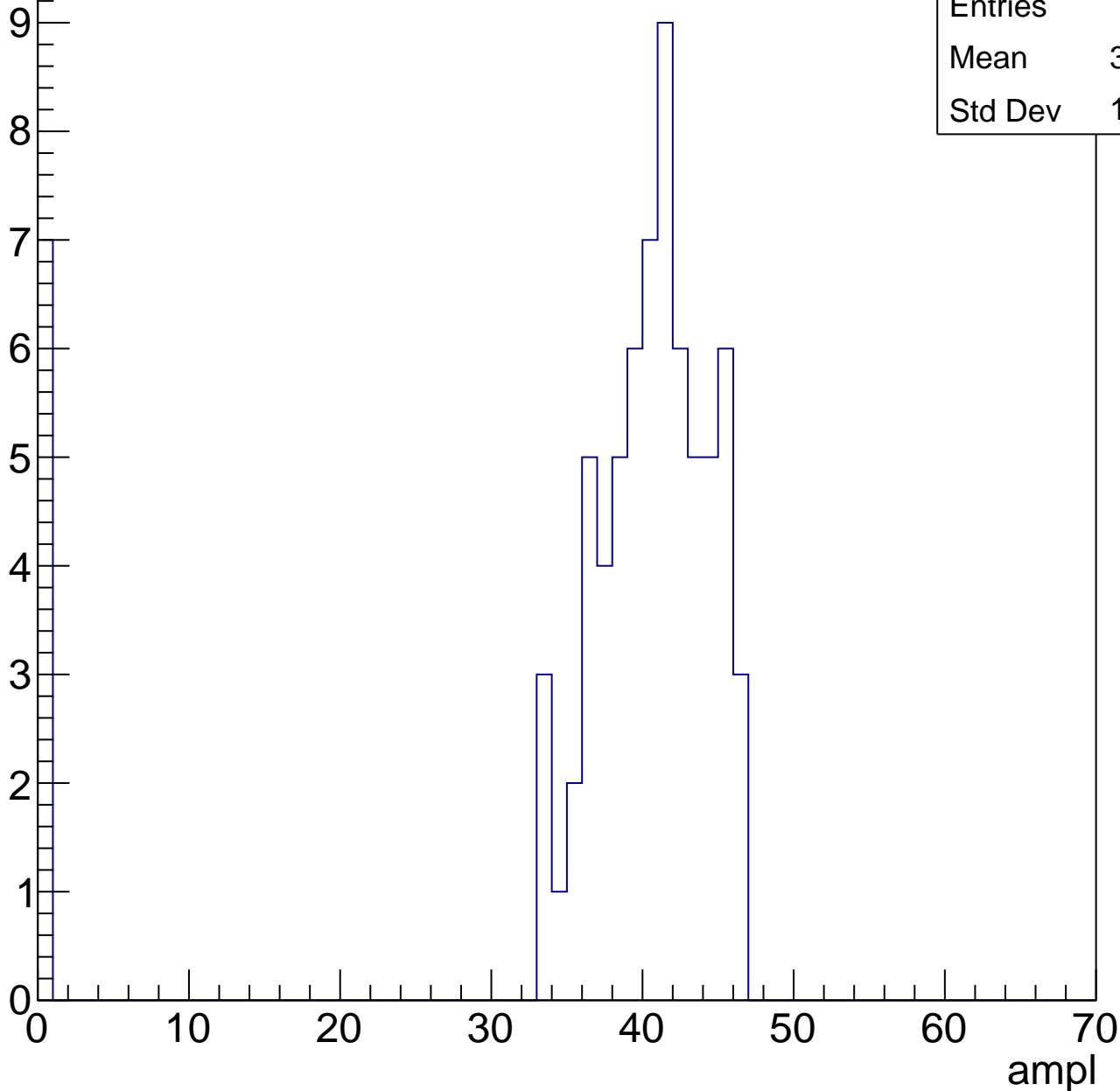


# B1L103S, U25-ch72, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	74
Mean	36.47
Std Dev	12.23

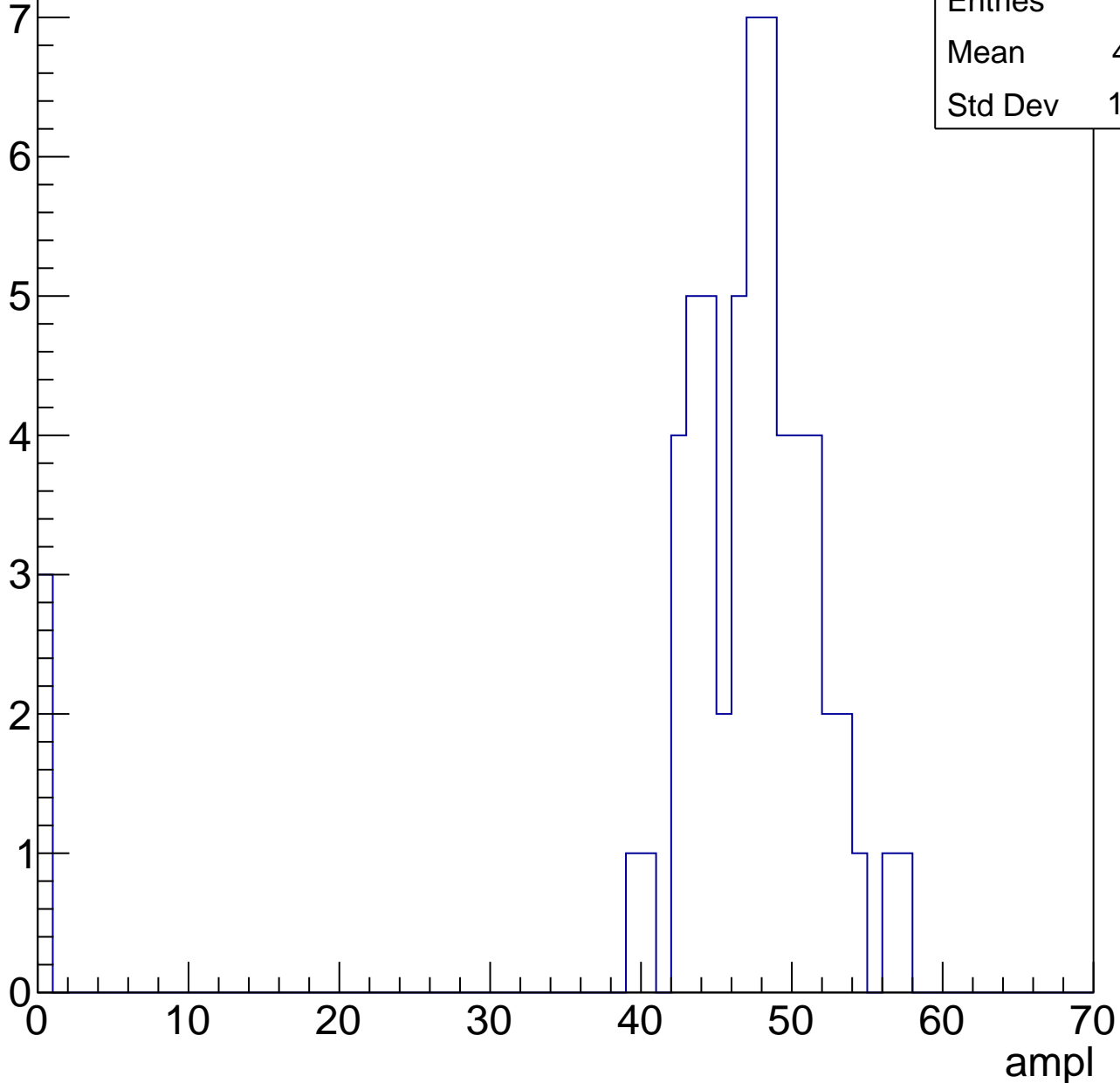


# B1L103S, U25-ch72, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	59
Mean	44.81
Std Dev	11.02

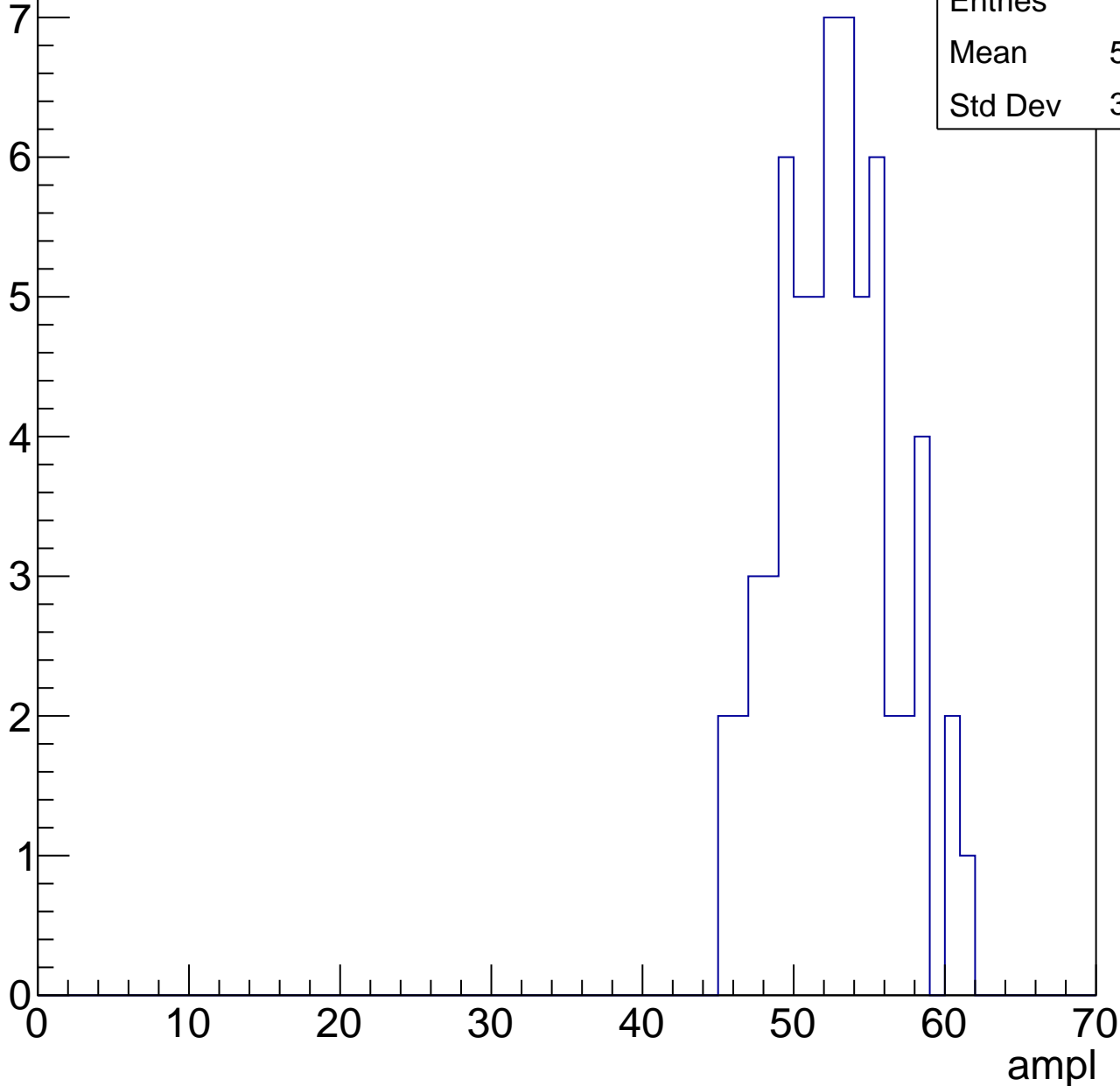


# B1L103S, U25-ch72, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

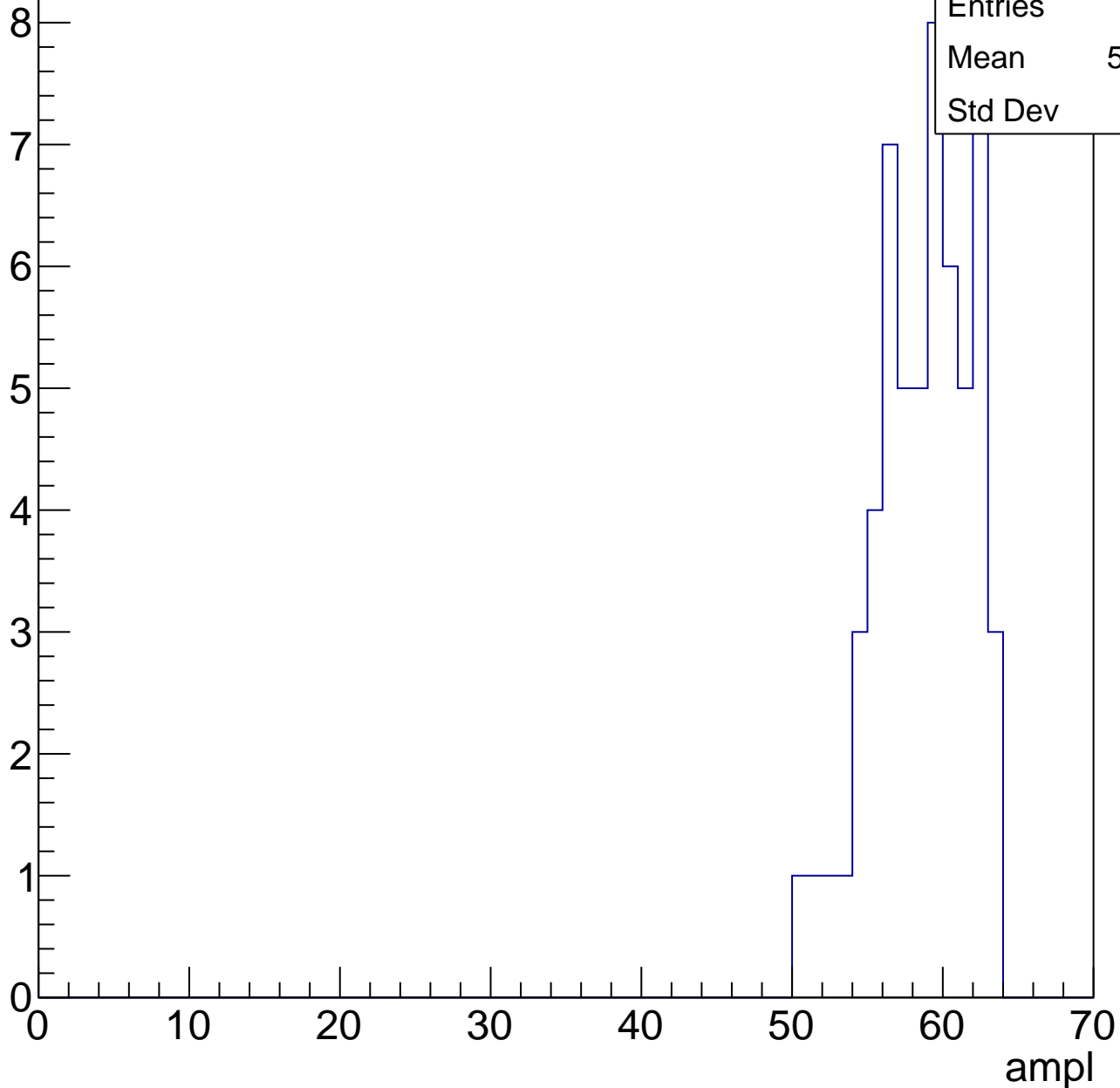
Entries	62
Mean	52.26
Std Dev	3.776



# B1L103S, U25-ch72, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



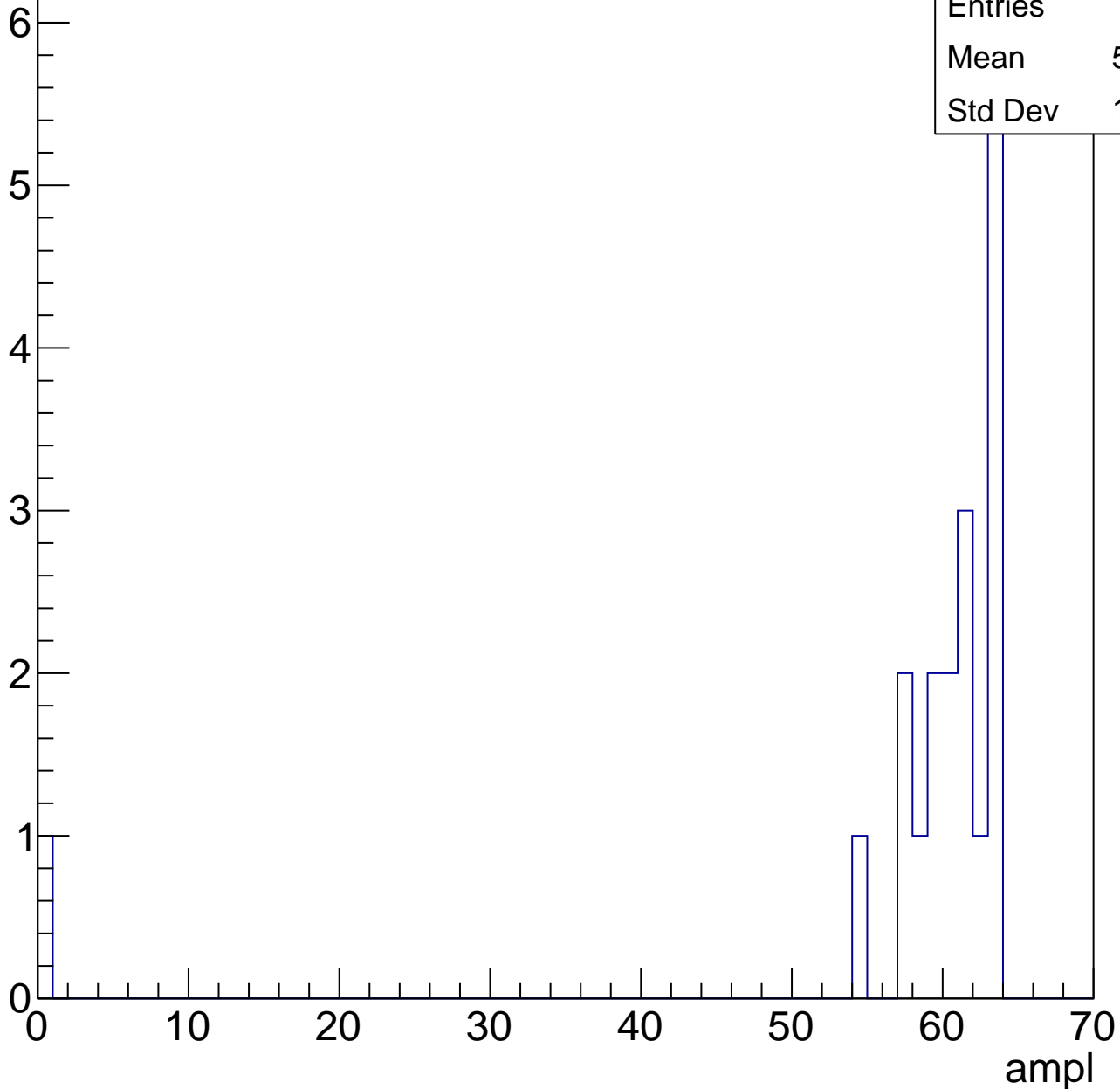
Entries	58
Mean	58.22
Std Dev	3.13

# B1L103S, U25-ch72, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	19
Mean	57.21
Std Dev	13.71



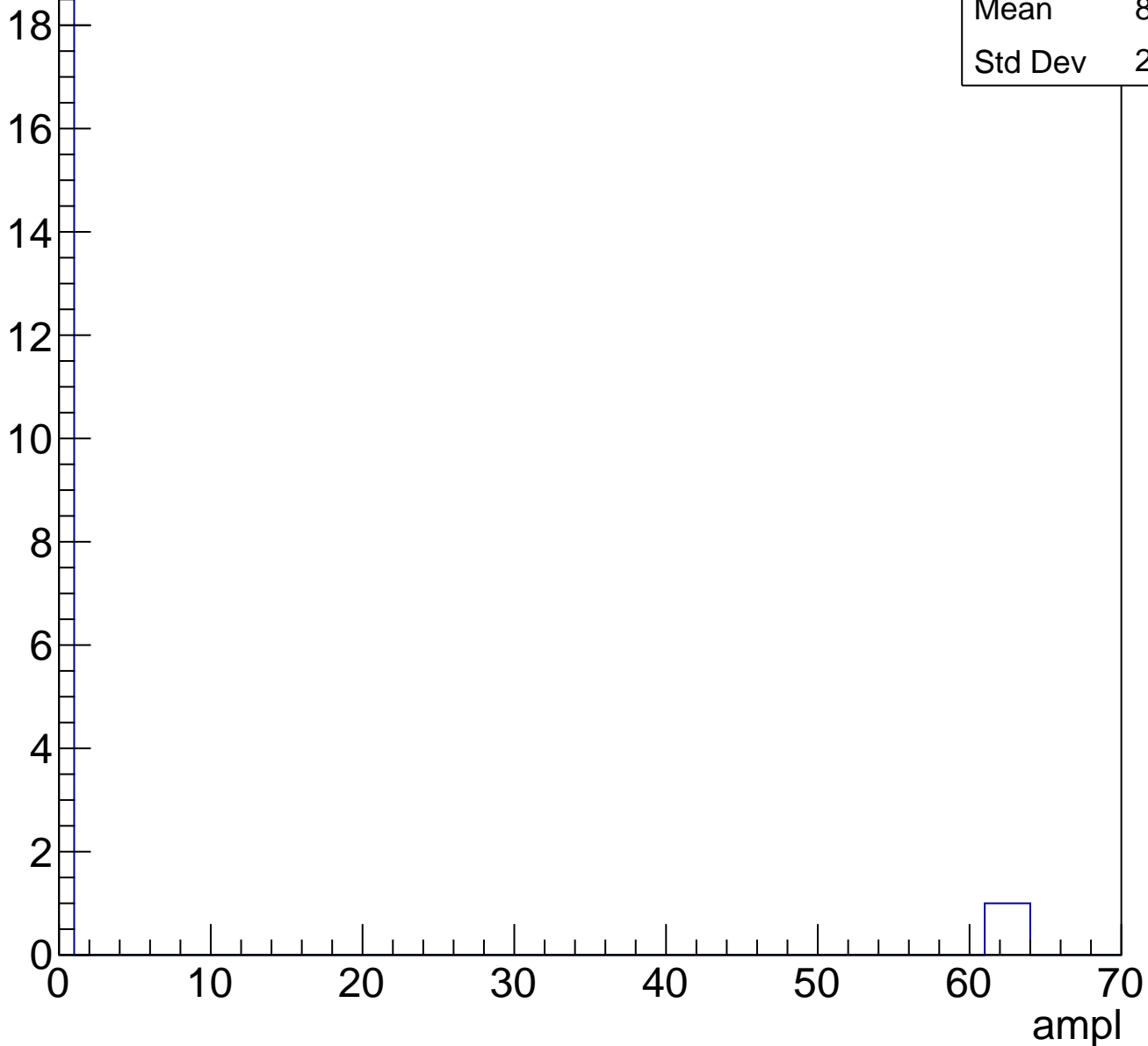


# B1L103S, U25-ch72, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	22
Mean	8.455
Std Dev	21.28

Entry



# B1L103S, U25-ch73, adc0

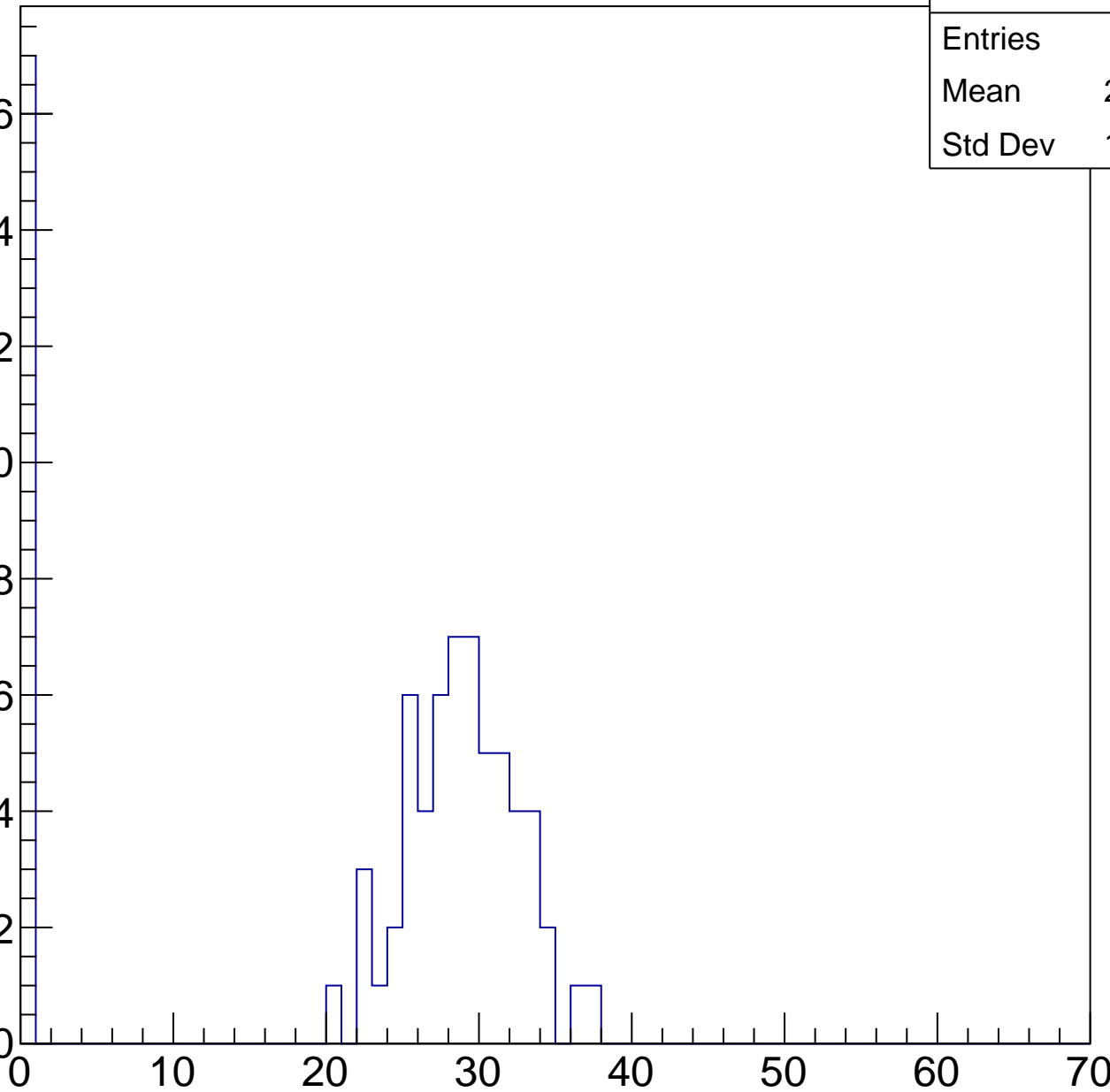
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	76
Mean	22.08
Std Dev	12.26

Entry

16  
14  
12  
10  
8  
6  
4  
2  
0

ampl

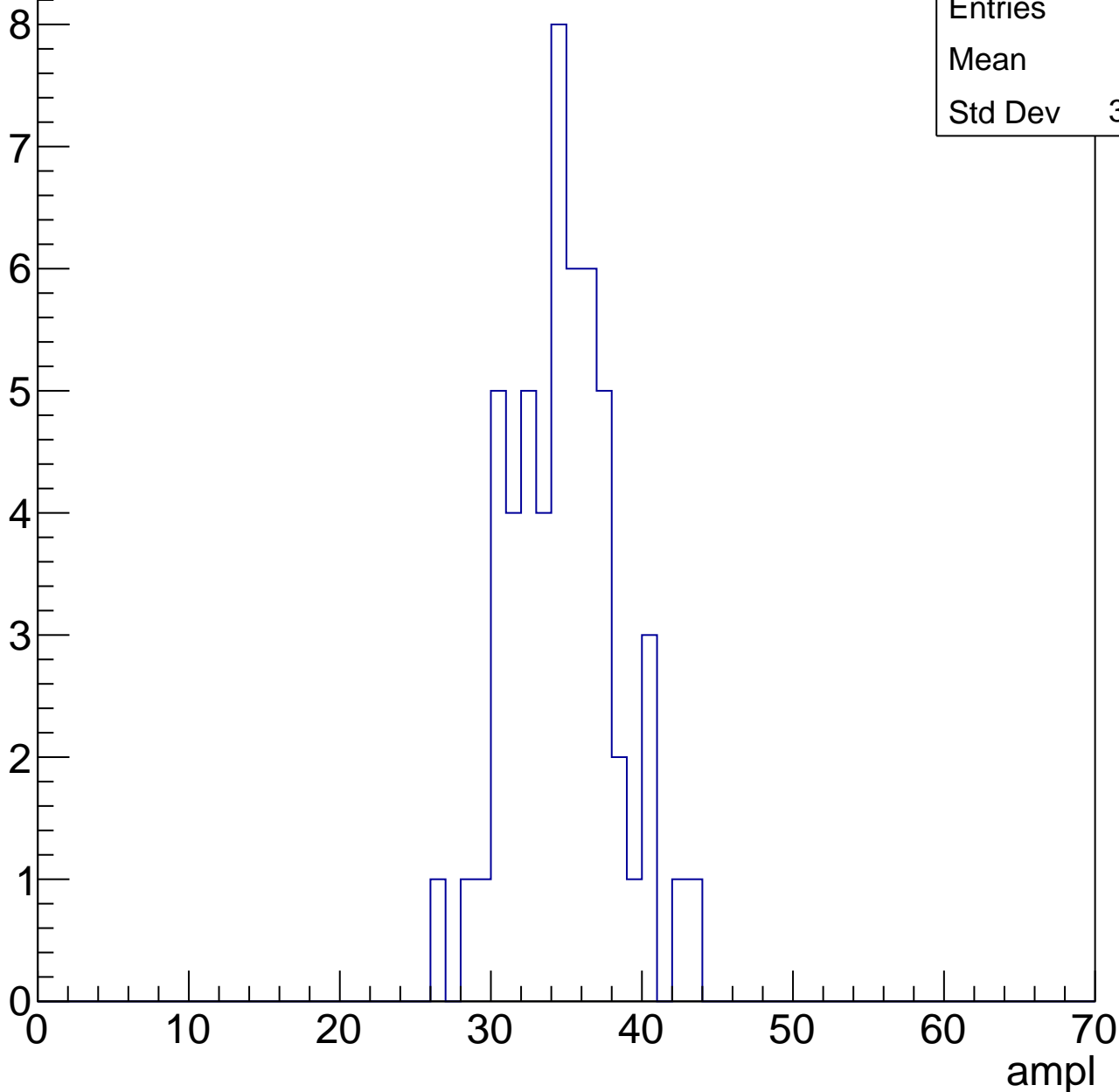


# B1L103S, U25-ch73, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	54
Mean	34.3
Std Dev	3.457

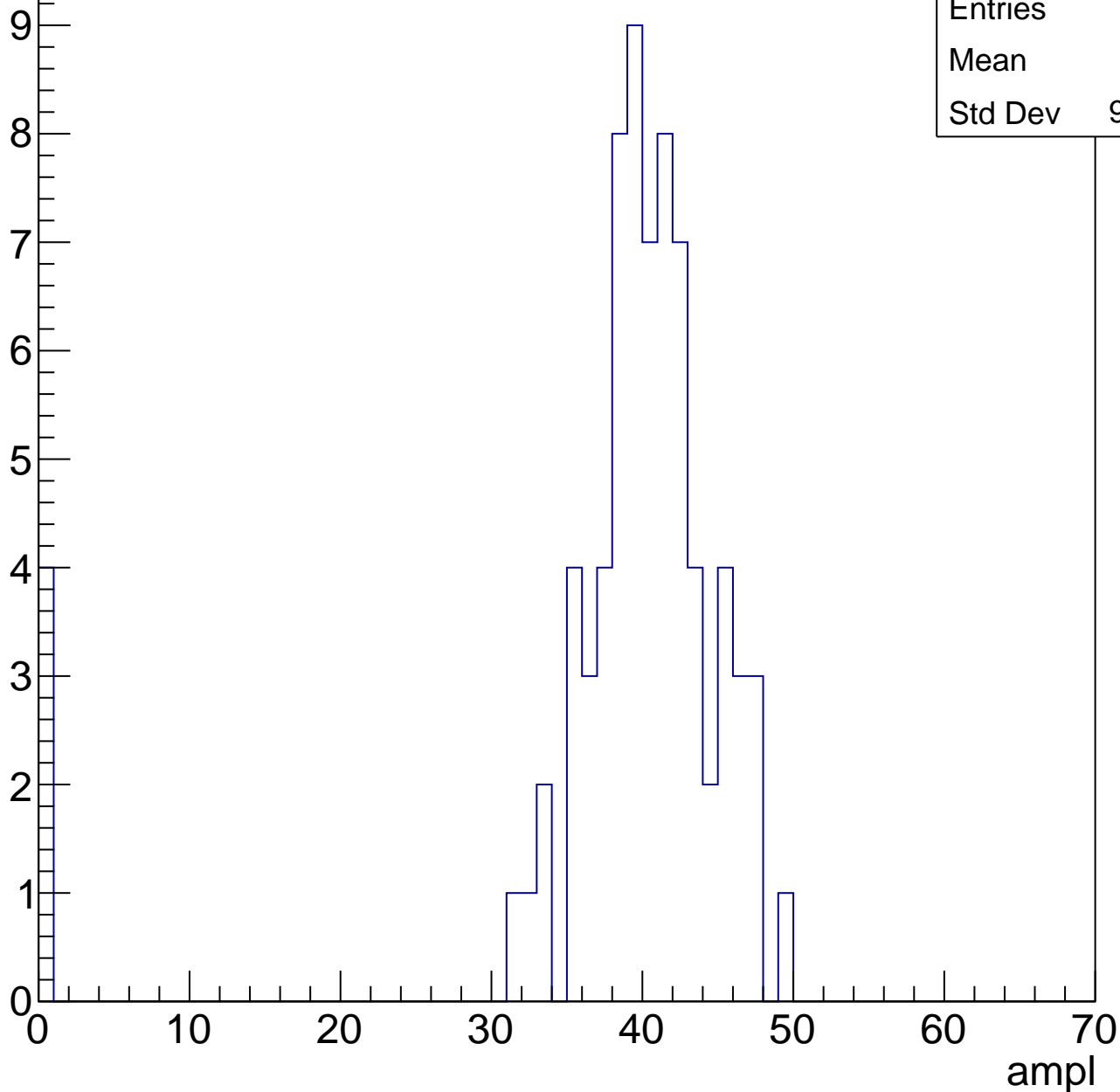


# B1L103S, U25-ch73, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	75
Mean	38
Std Dev	9.735



# B1L103S, U25-ch73, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	88
Mean	42.09
Std Dev	16.32

Entry

10

8

6

4

2

0

0

10

20

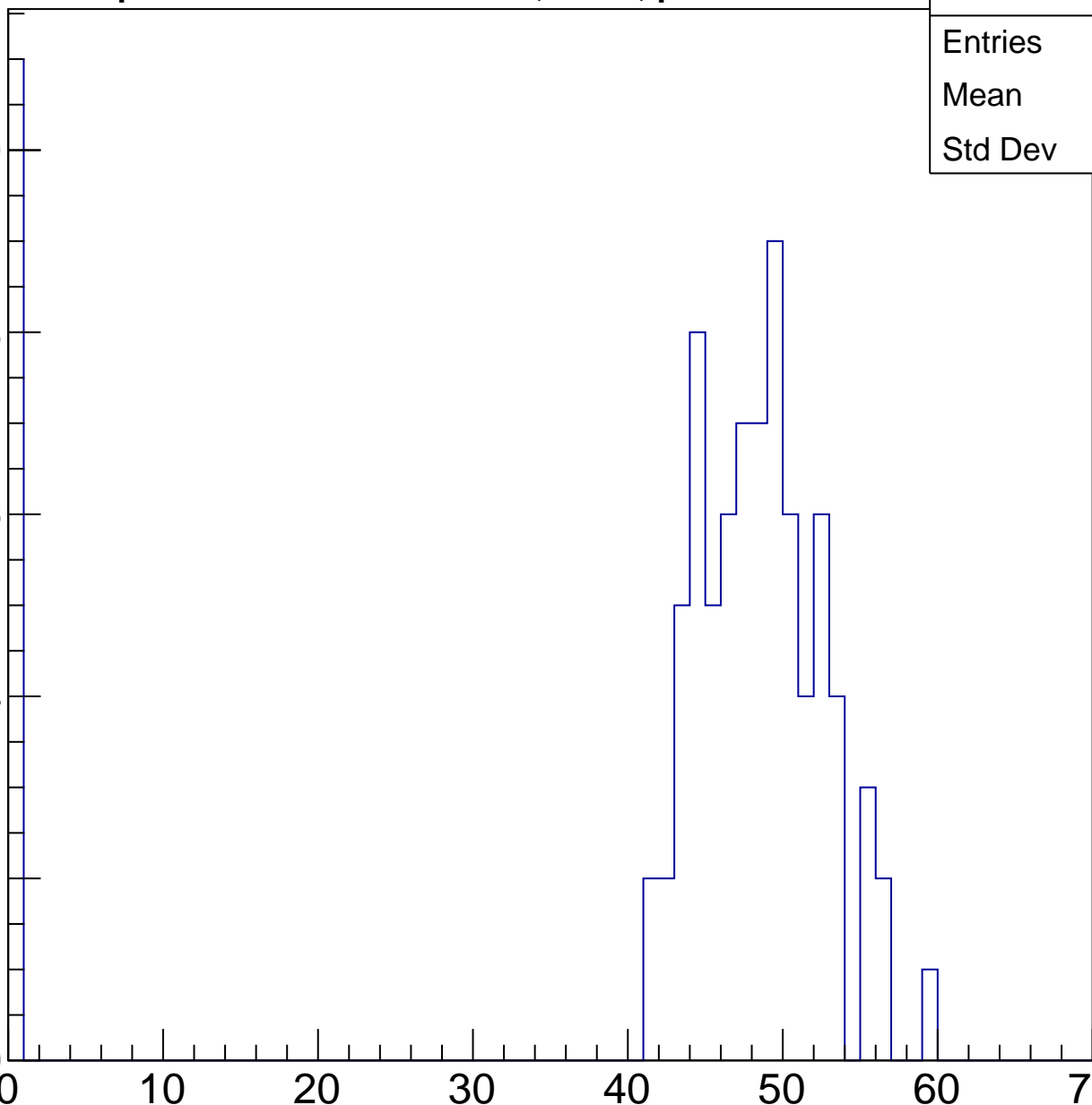
30

40

50

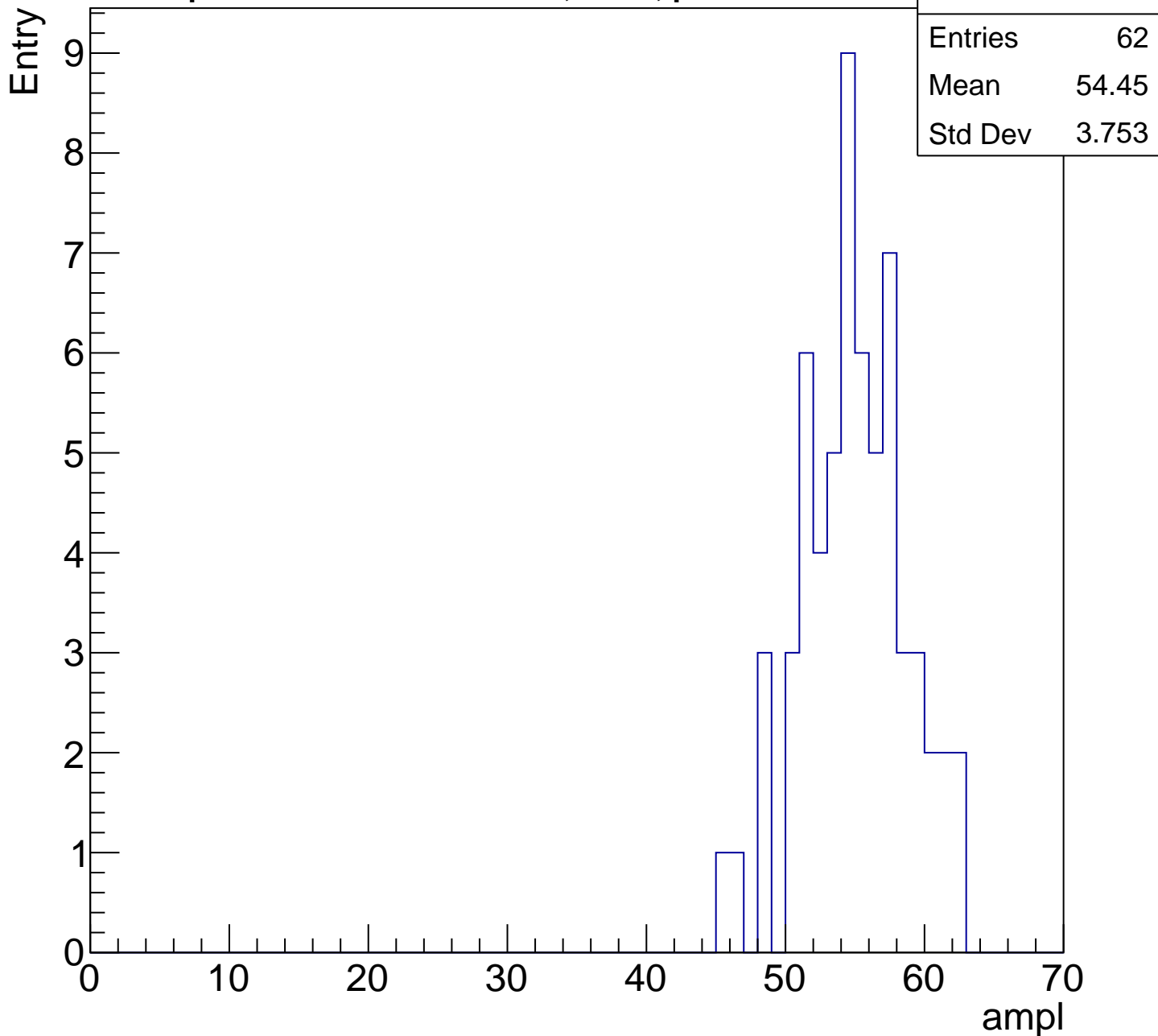
60

ampl



# B1L103S, U25-ch73, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2



# B1L103S, U25-ch73, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

6

5

4

3

2

1

0

Entries	43
Mean	59.28
Std Dev	2.888

ampl

10

20

30

40

50

60

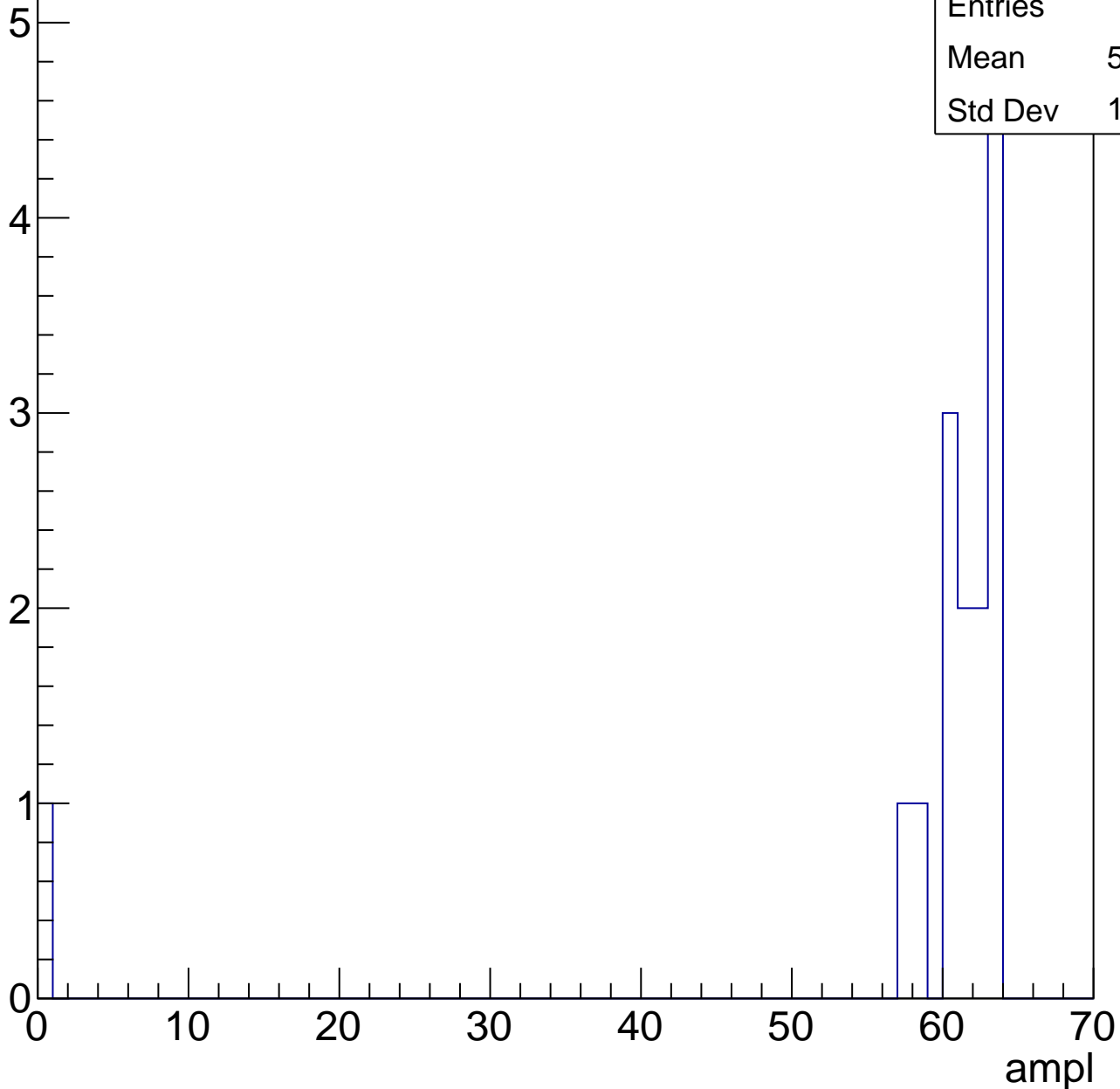
70

# B1L103S, U25-ch73, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	15
Mean	57.07
Std Dev	15.36





# B1L103S, U25-ch73, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U25-ch74, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

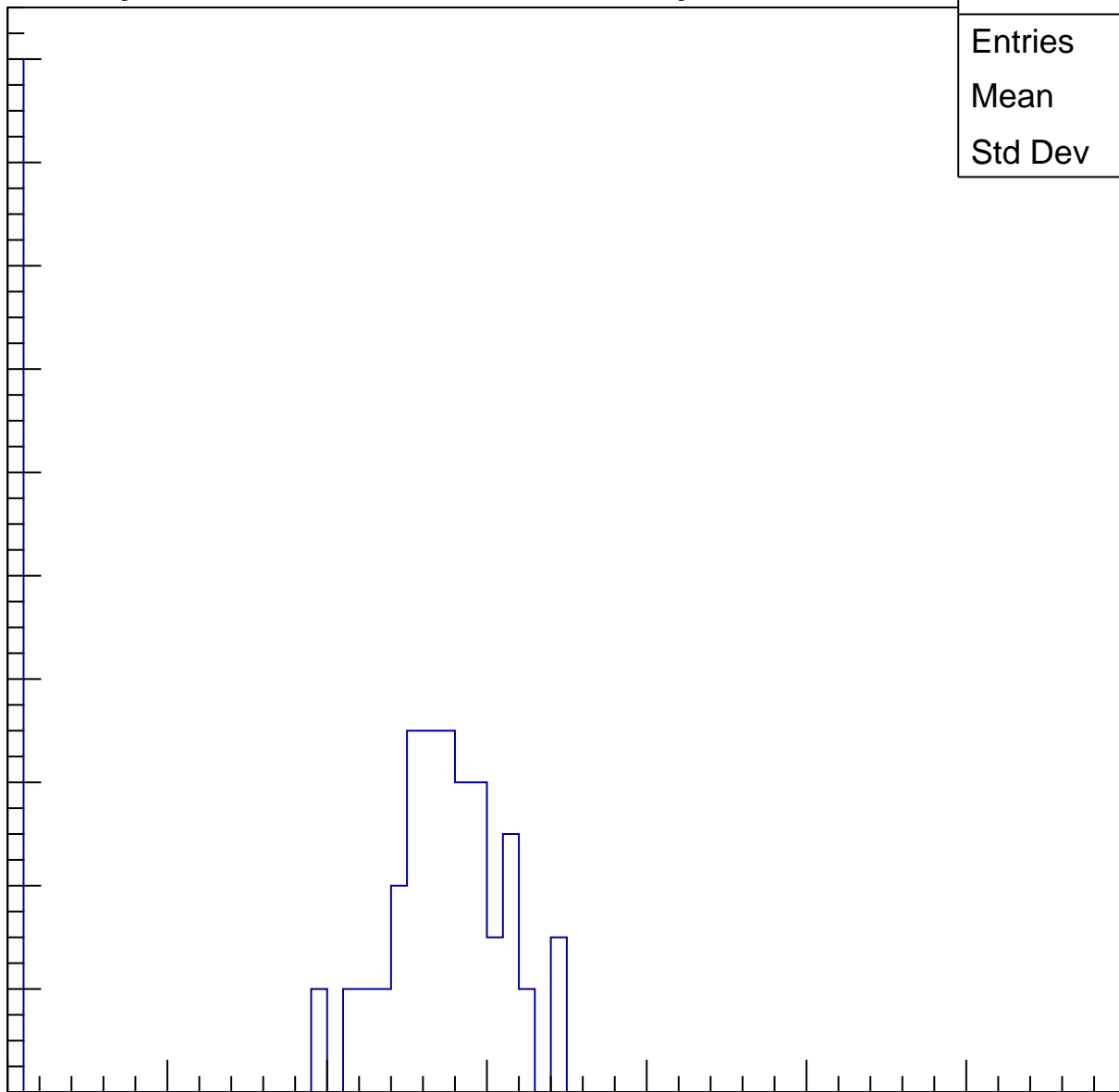
Entries	78
Mean	20.06
Std Dev	12.15

Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L103S, U25-ch74, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	95
Mean	29.09
Std Dev	12.08

Entry

12

10

8

6

4

2

0

0

10

20

30

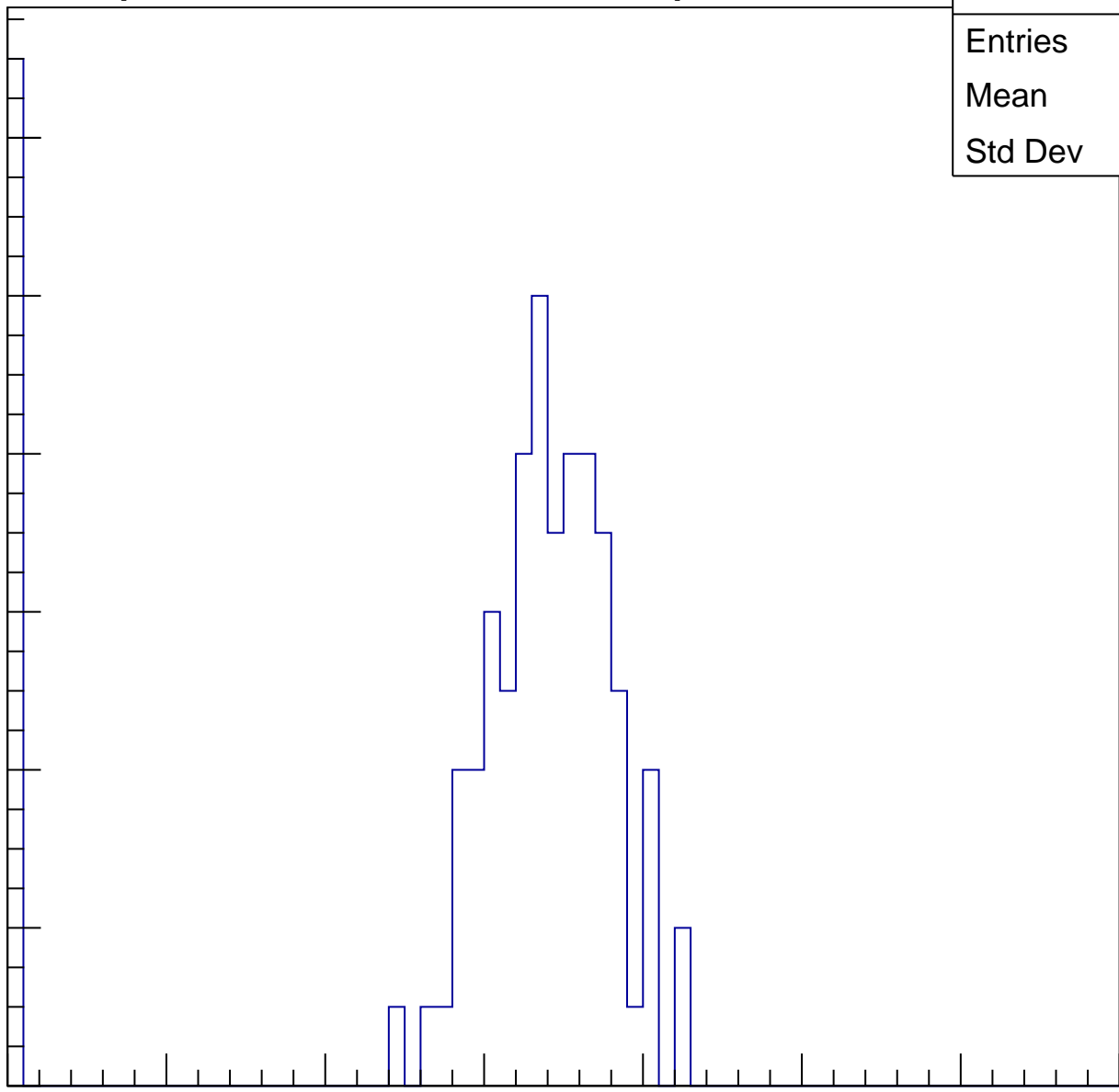
40

50

60

70

ampl

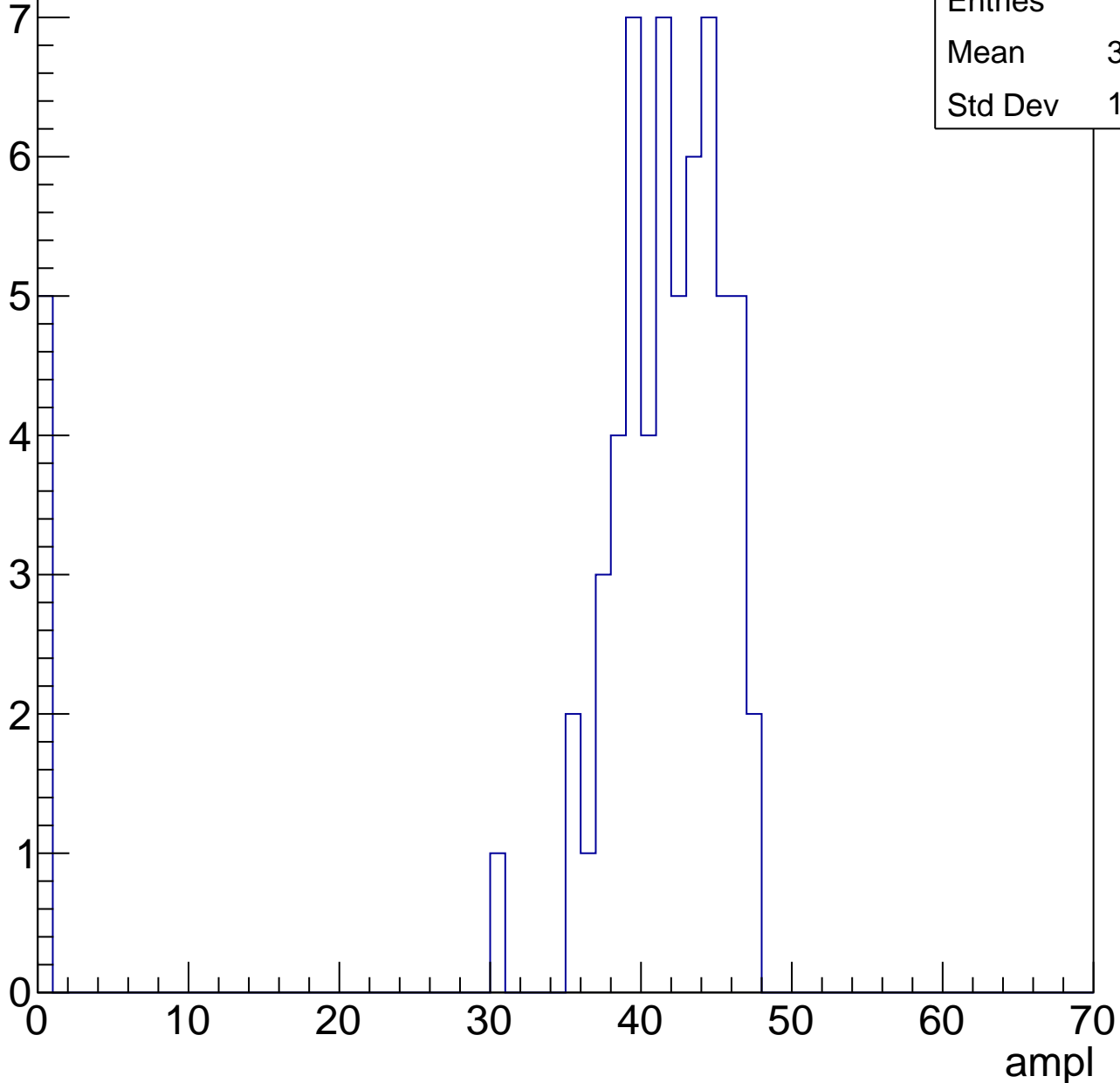


# B1L103S, U25-ch74, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	64
Mean	38.19
Std Dev	11.59

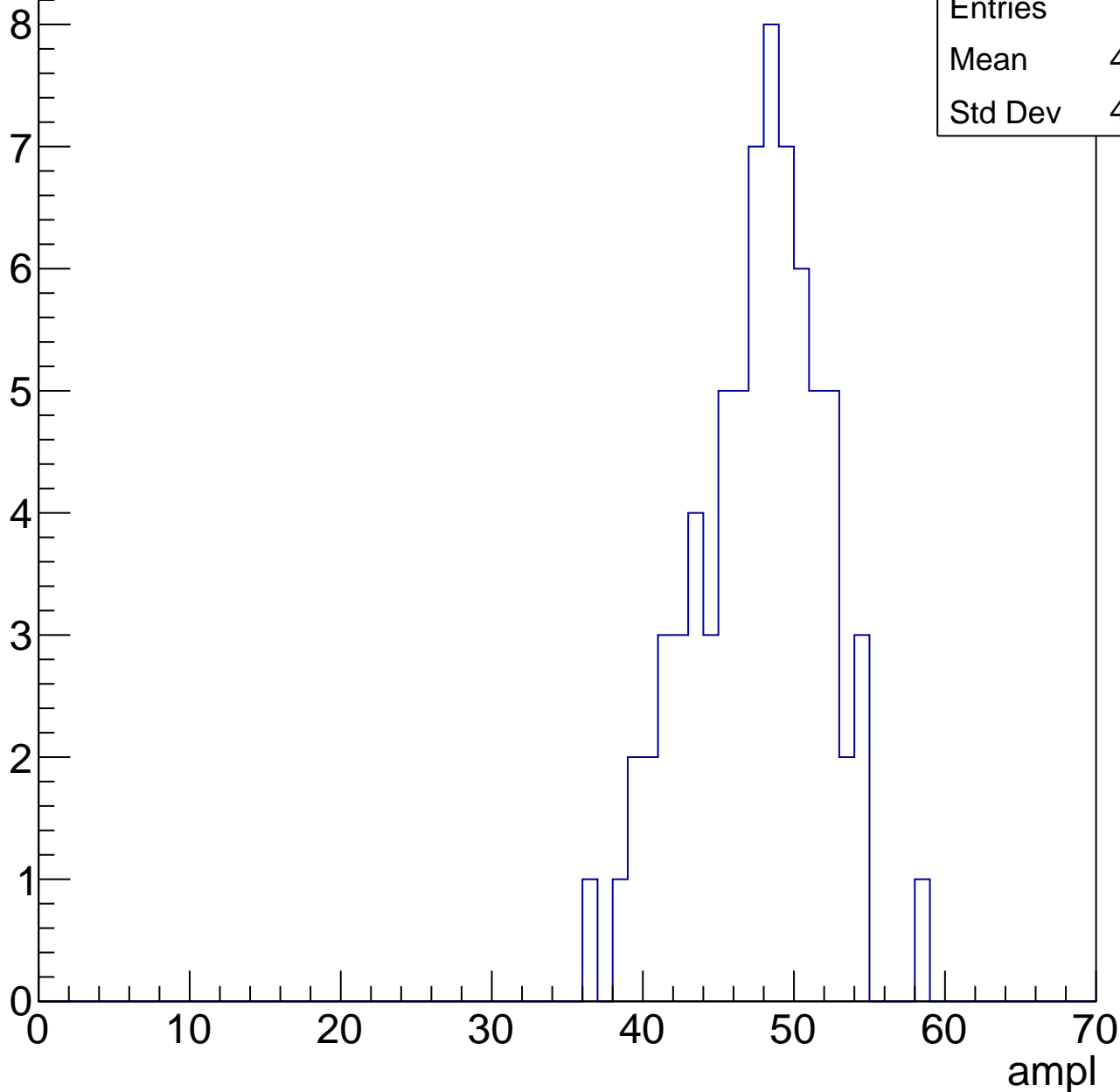


# B1L103S, U25-ch74, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	73
Mean	47.08
Std Dev	4.319

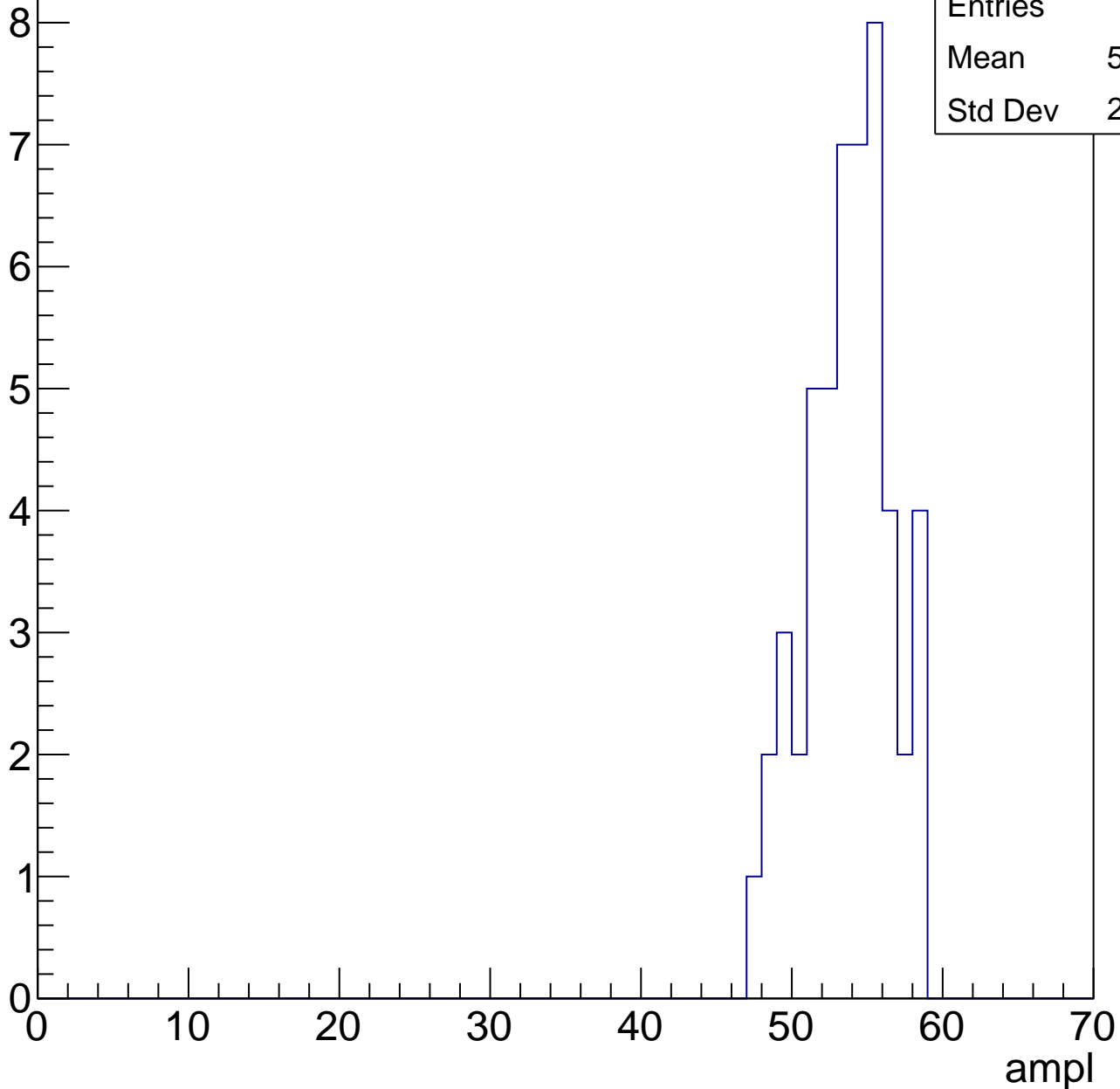


# B1L103S, U25-ch74, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	50
Mean	53.28
Std Dev	2.757

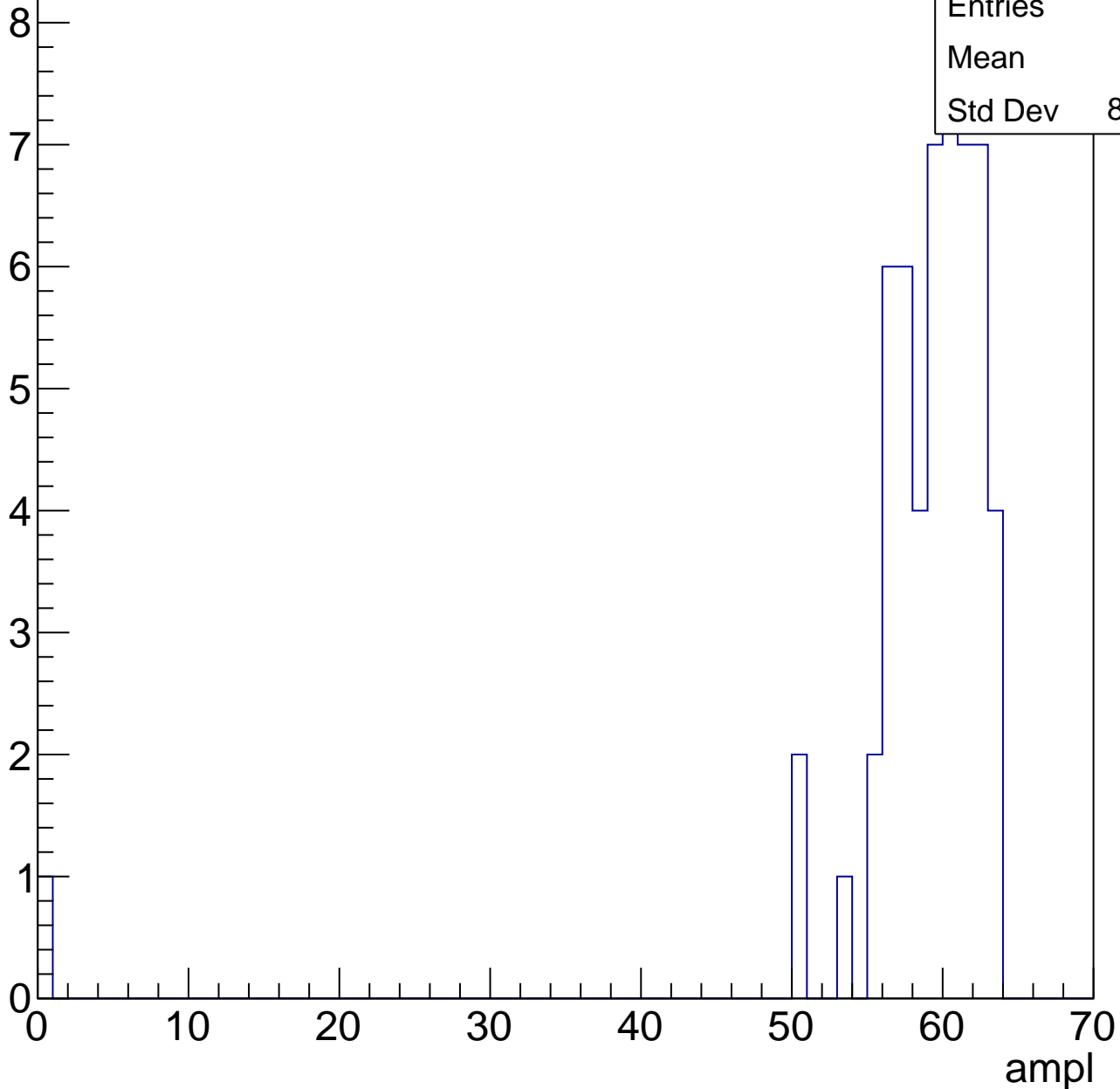


# B1L103S, U25-ch74, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

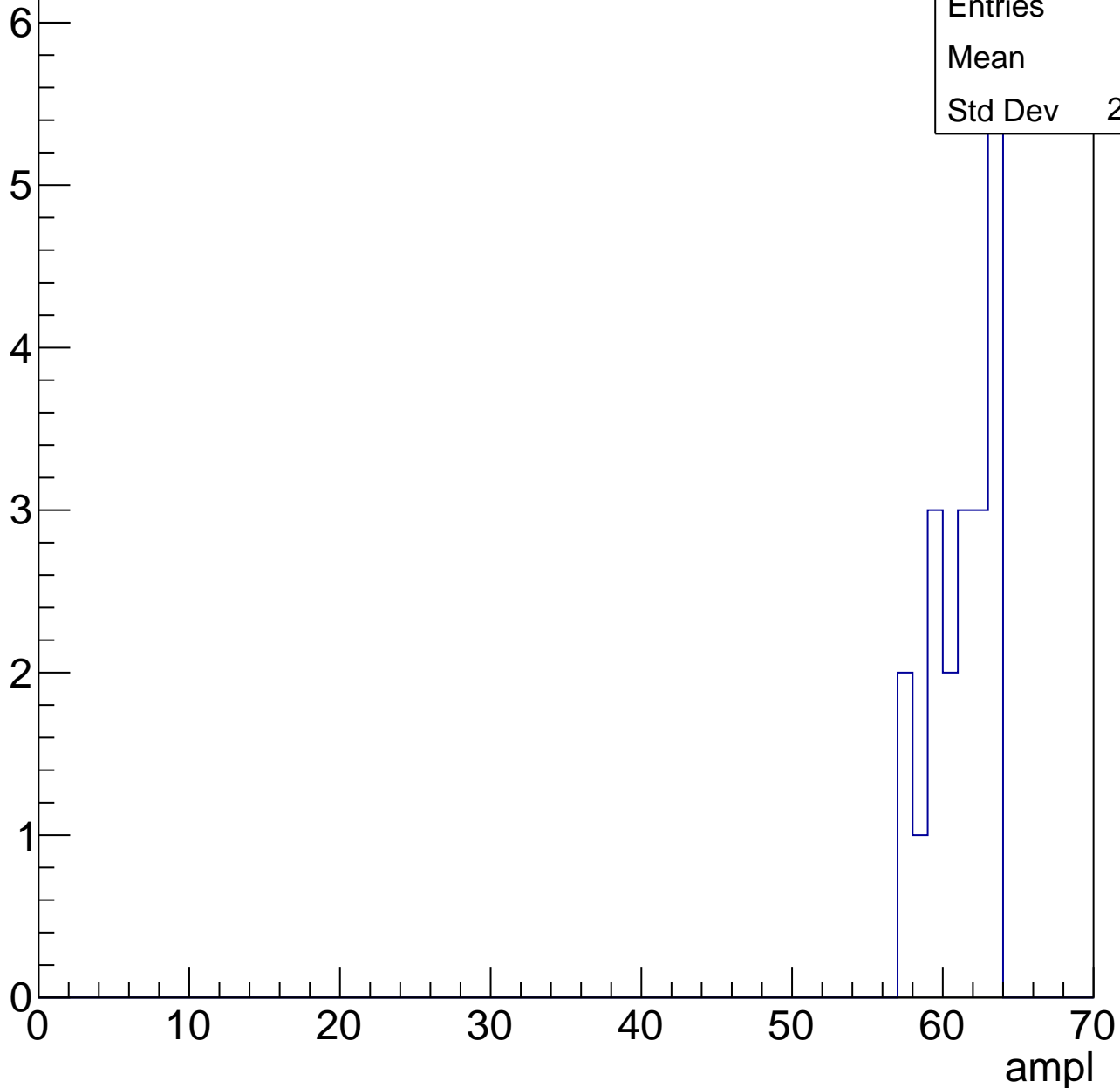
Entries	55
Mean	57.8
Std Dev	8.396



# B1L103S, U25-ch74, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



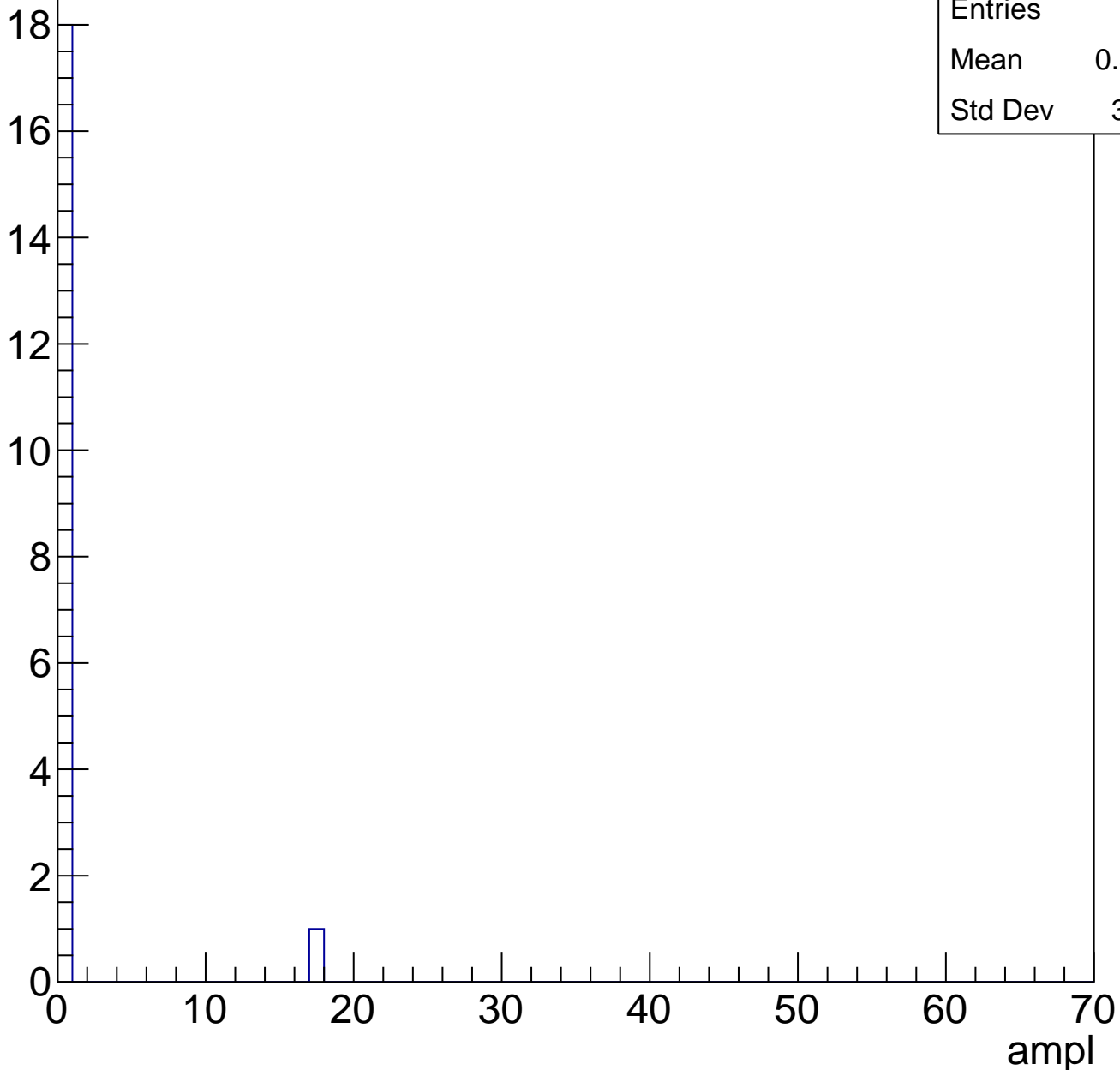


# B1L103S, U25-ch74, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	19
Mean	0.8947
Std Dev	3.796

Entry



# B1L103S, U25-ch75, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

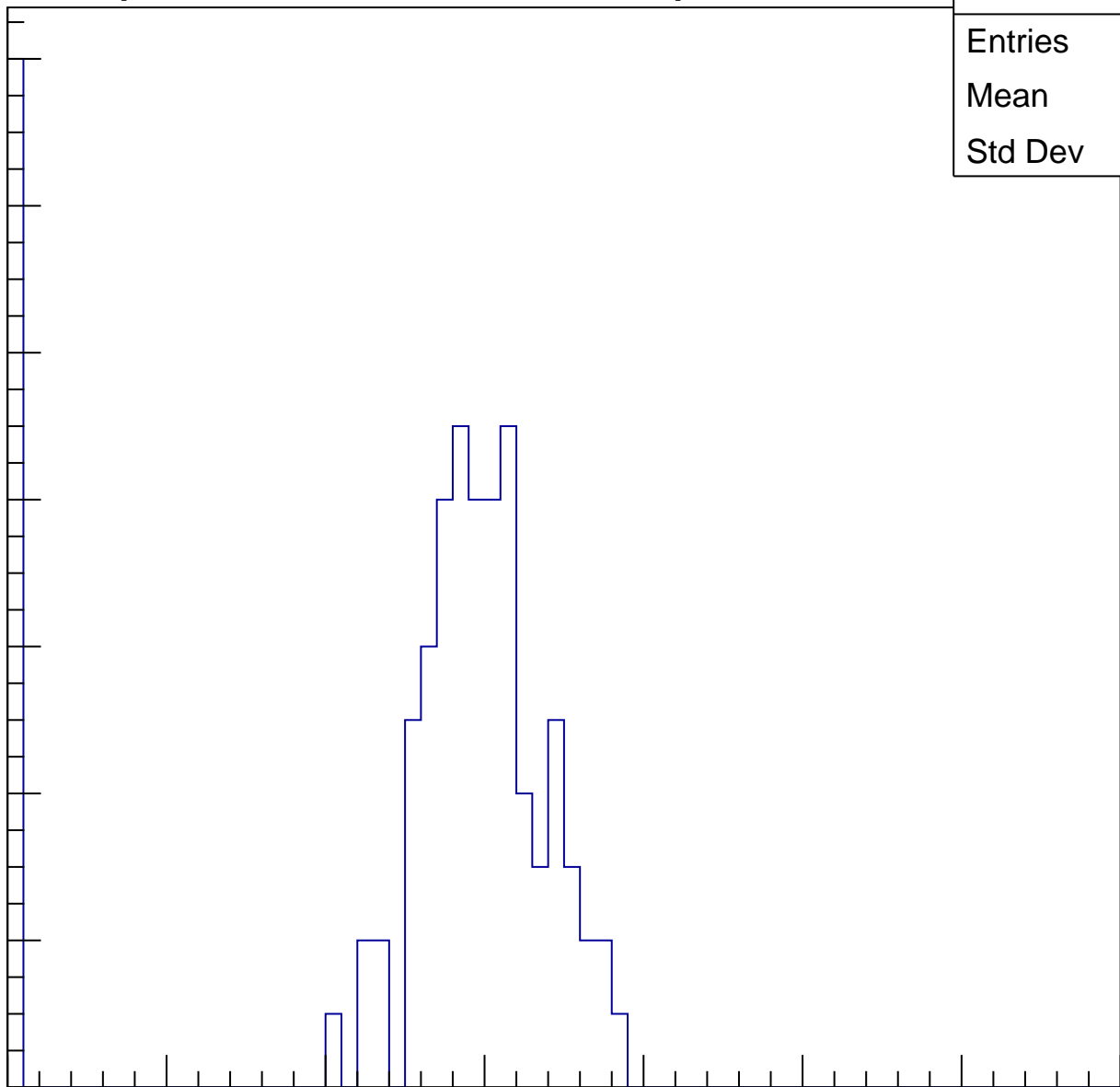
Entries	92
Mean	24.96
Std Dev	11.11

Entry

14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

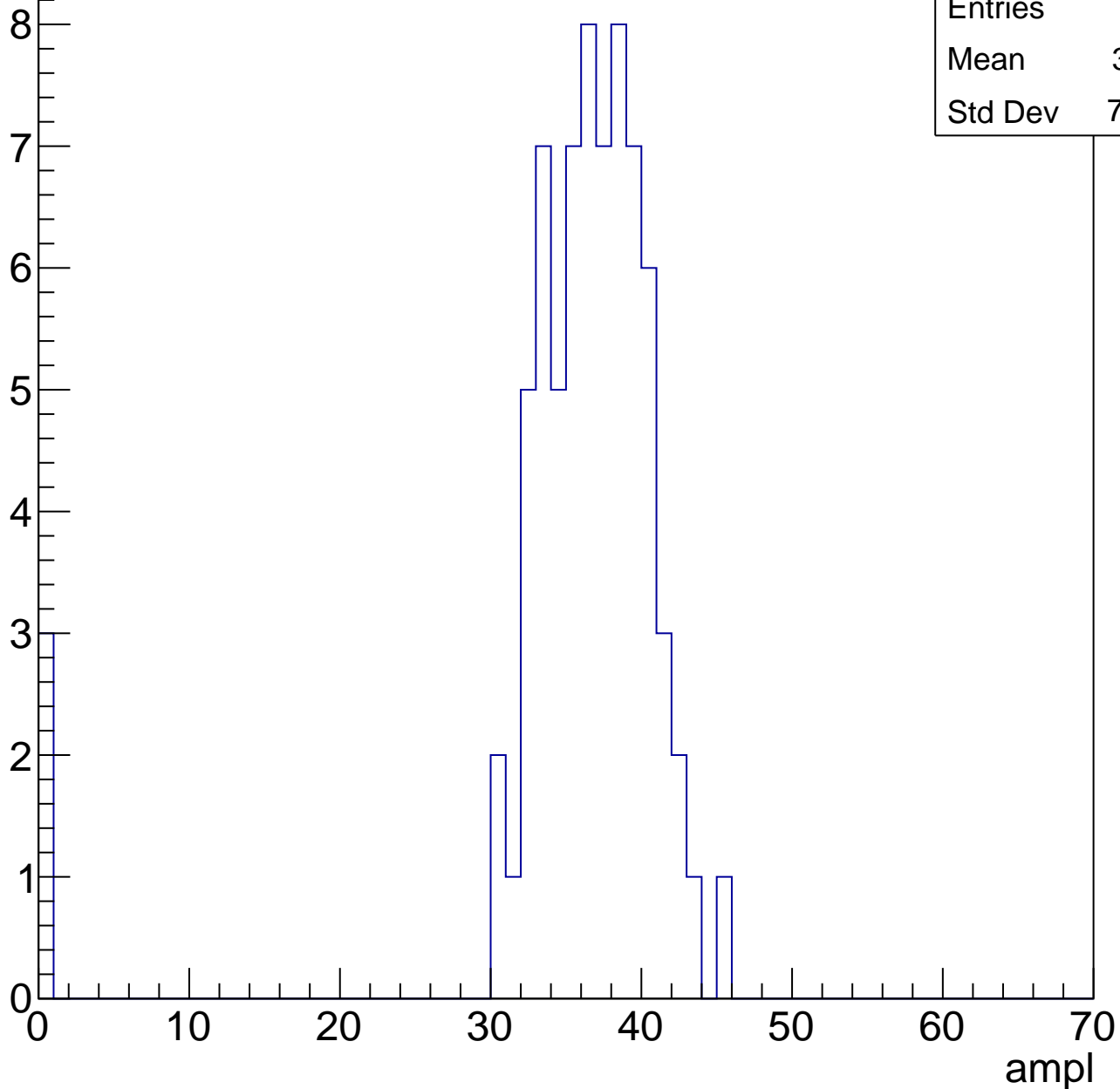


# B1L103S, U25-ch75, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	73
Mean	35.01
Std Dev	7.903

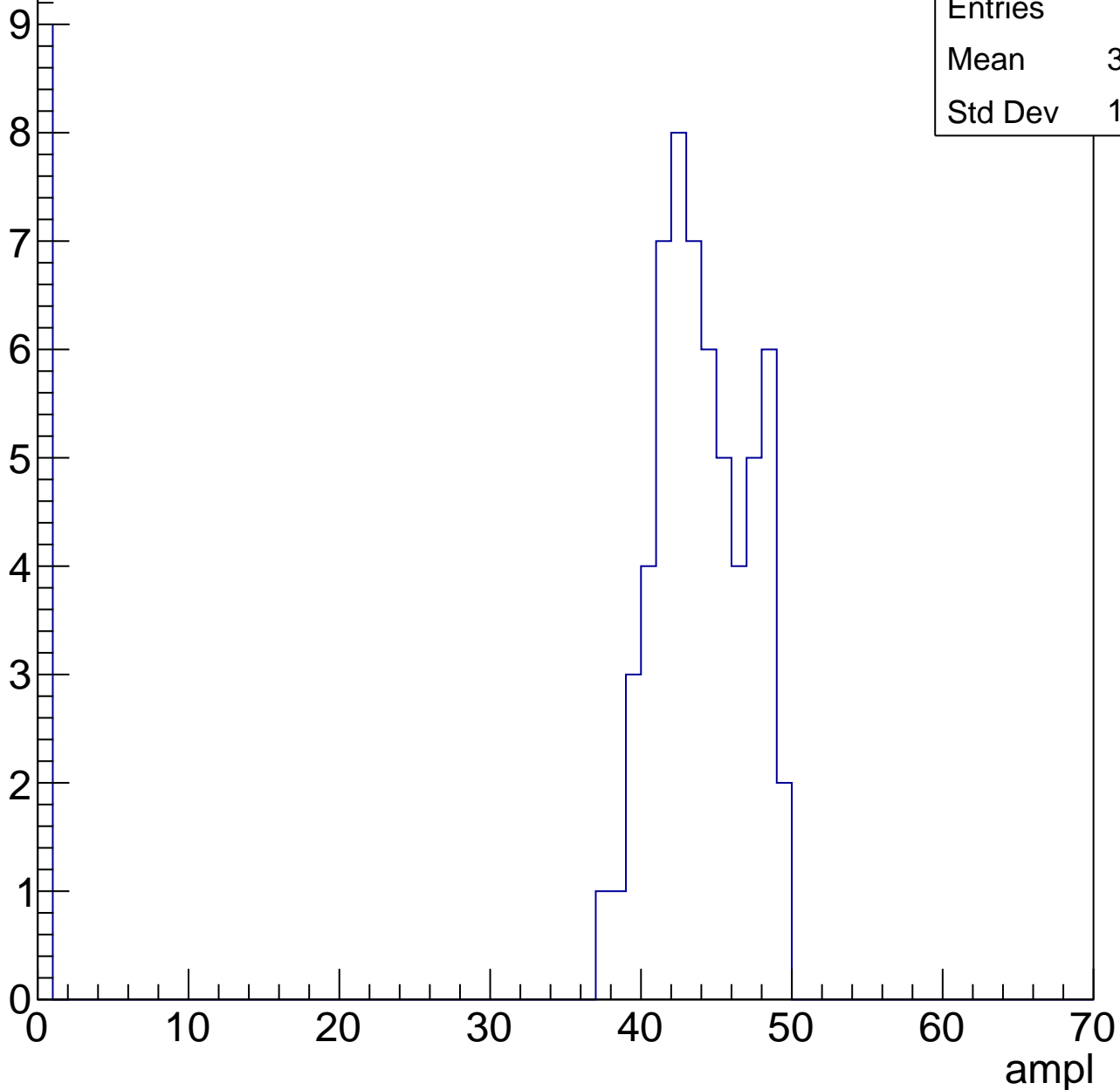


# B1L103S, U25-ch75, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	68
Mean	37.79
Std Dev	15.02

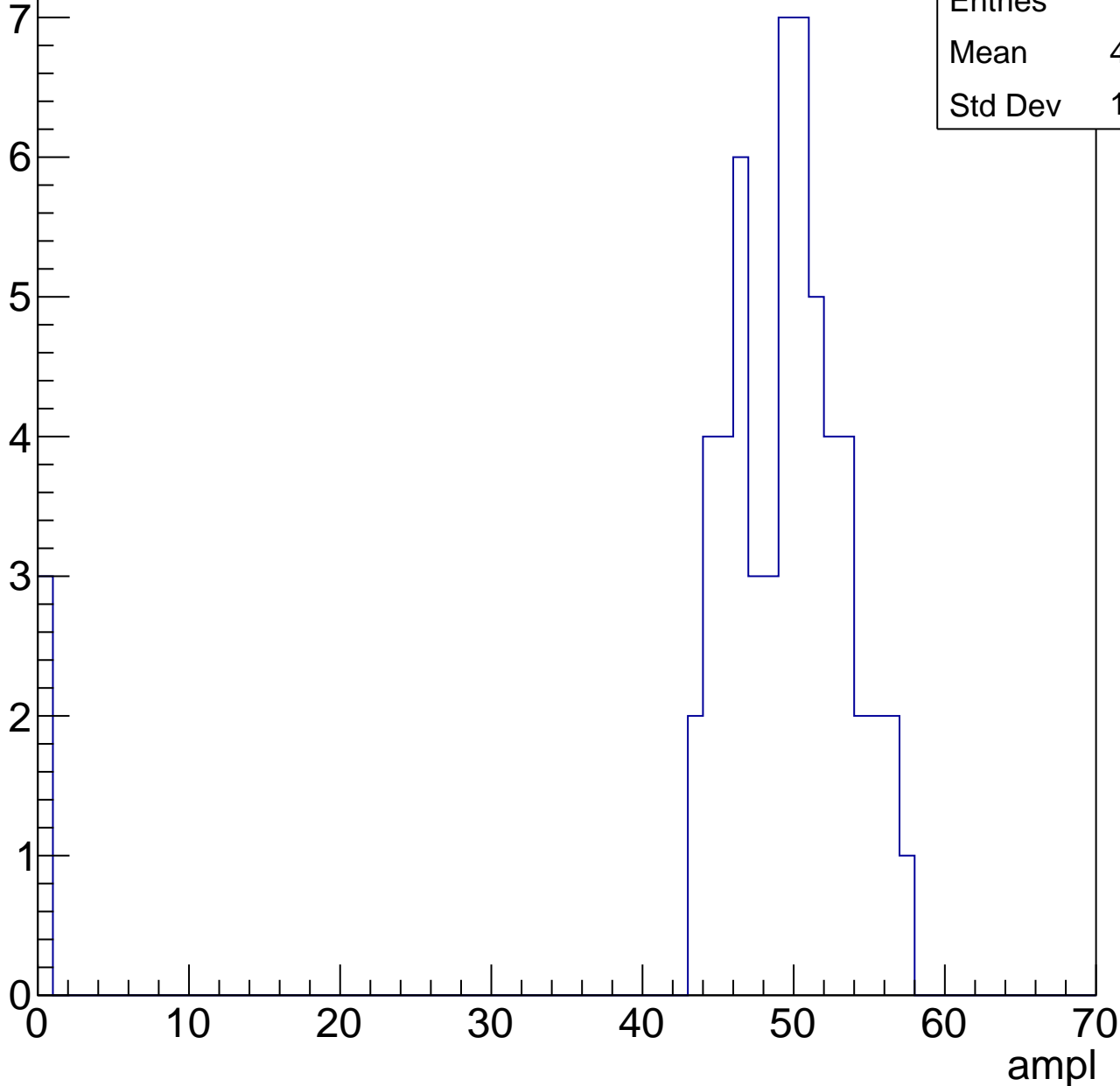


# B1L103S, U25-ch75, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	59
Mean	46.75
Std Dev	11.36

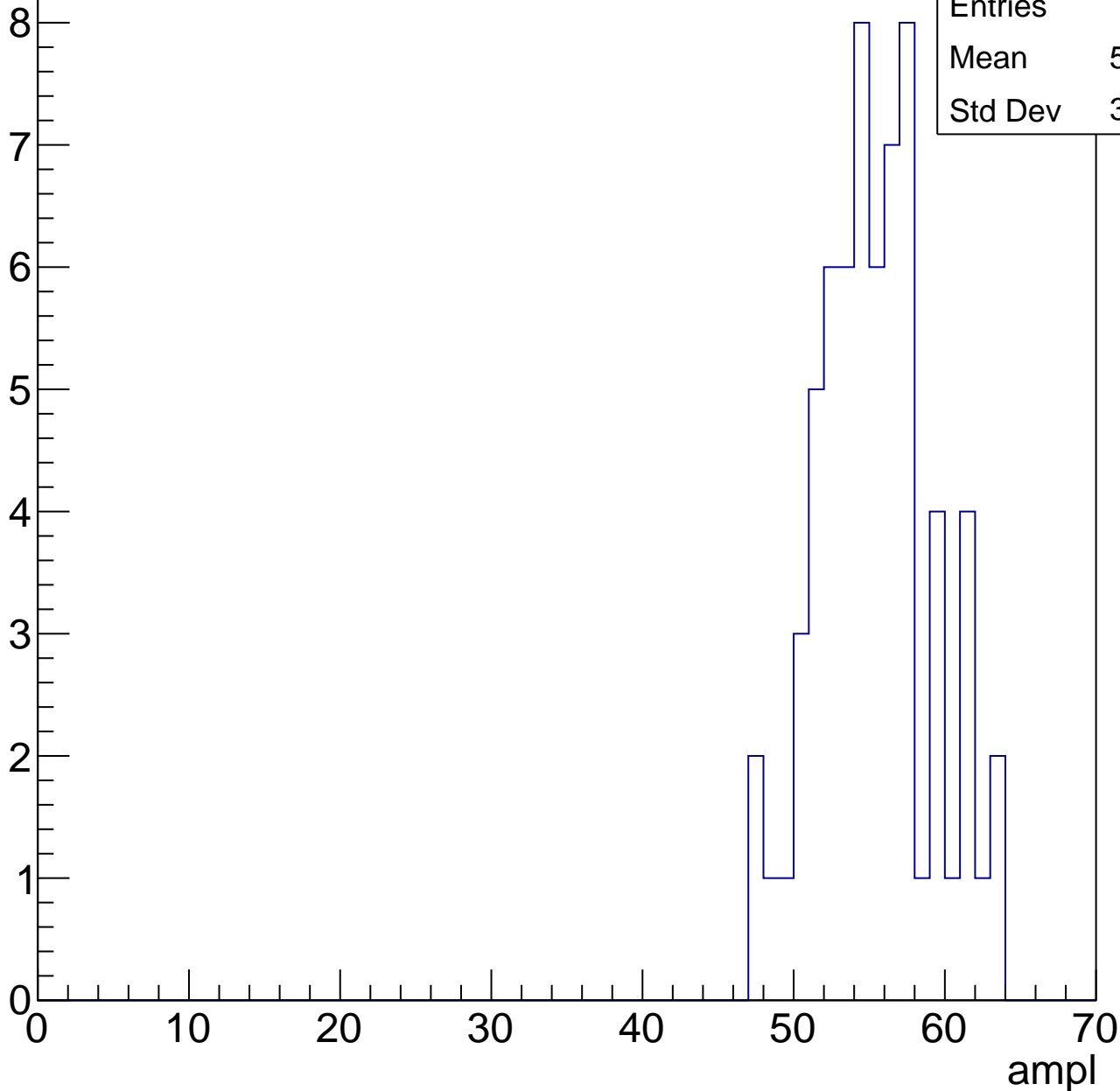


# B1L103S, U25-ch75, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

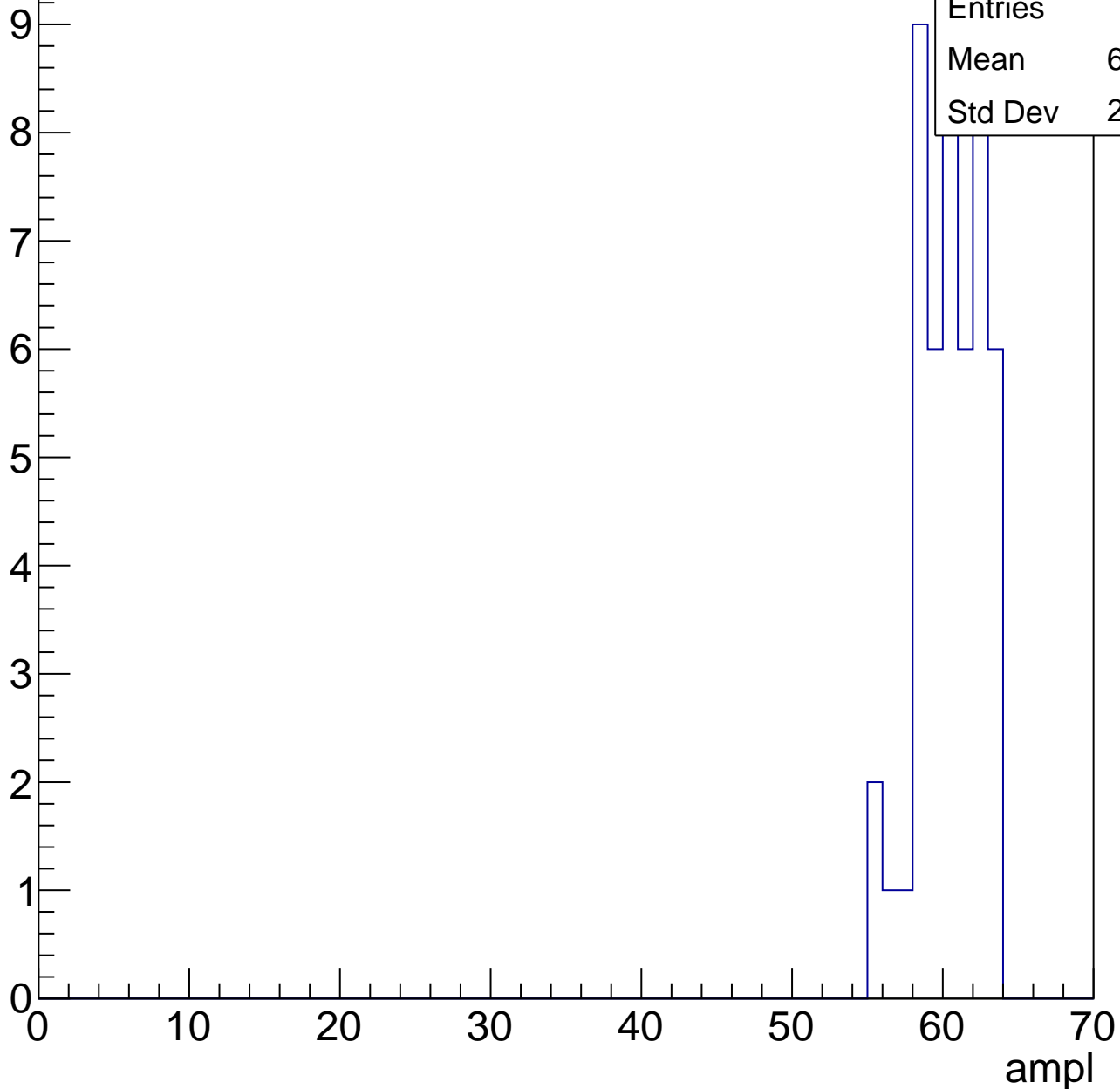
Entries	66
Mean	54.88
Std Dev	3.715



# B1L103S, U25-ch75, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U25-ch75, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U25-ch75, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

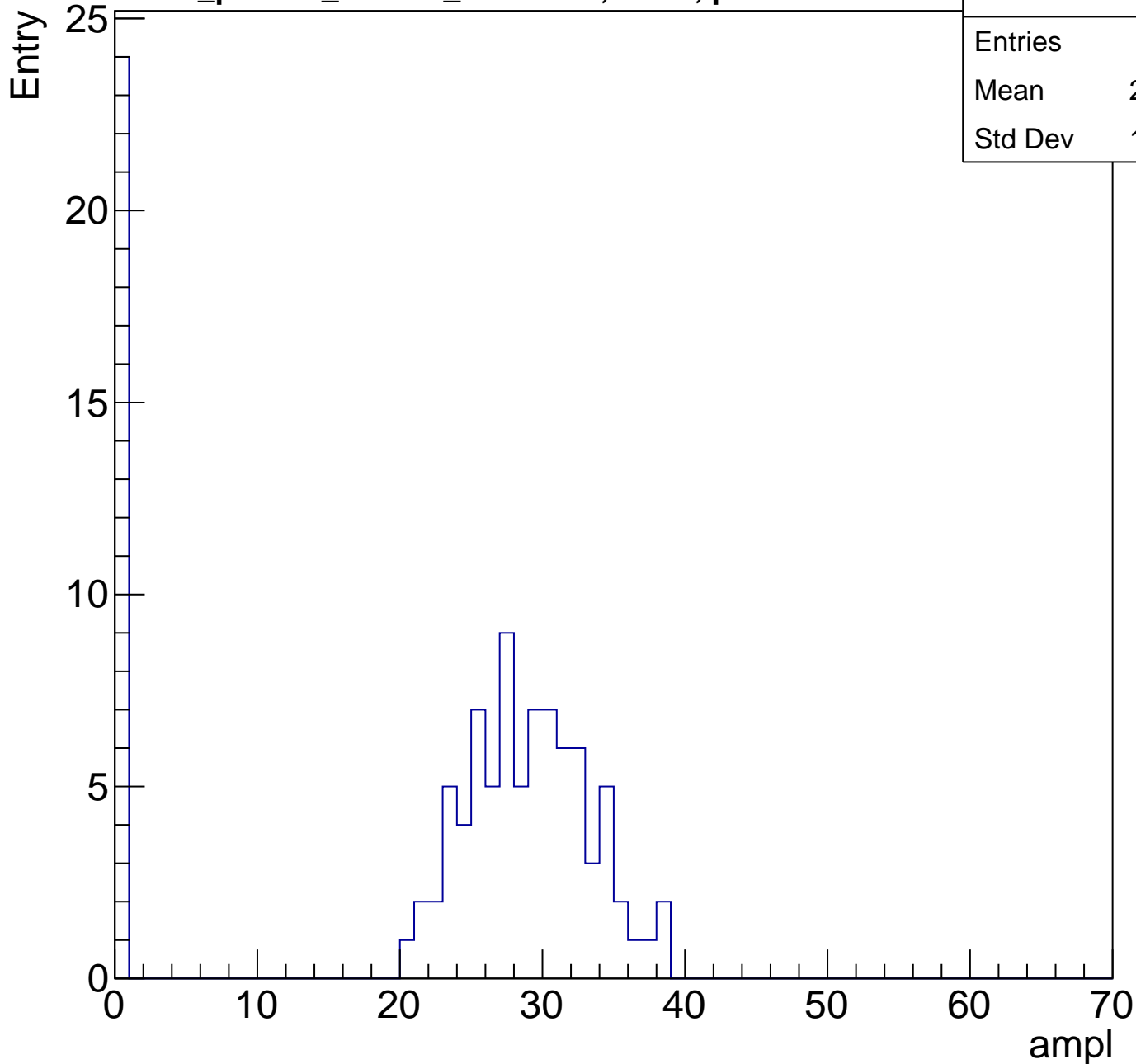
Entry



# B1L103S, U25-ch76, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	104
Mean	21.96
Std Dev	12.57

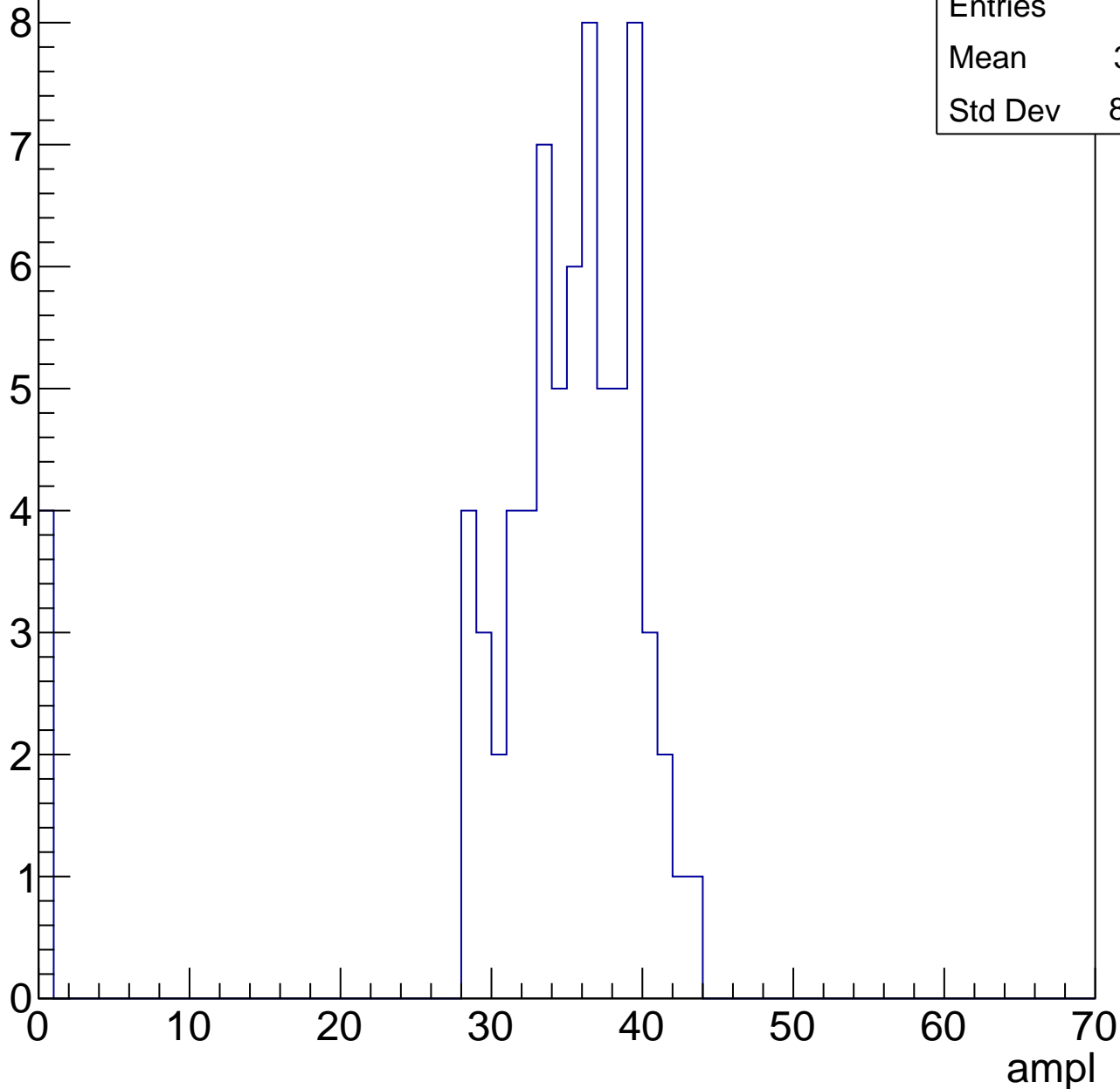


# B1L103S, U25-ch76, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	72
Mean	33.11
Std Dev	8.812

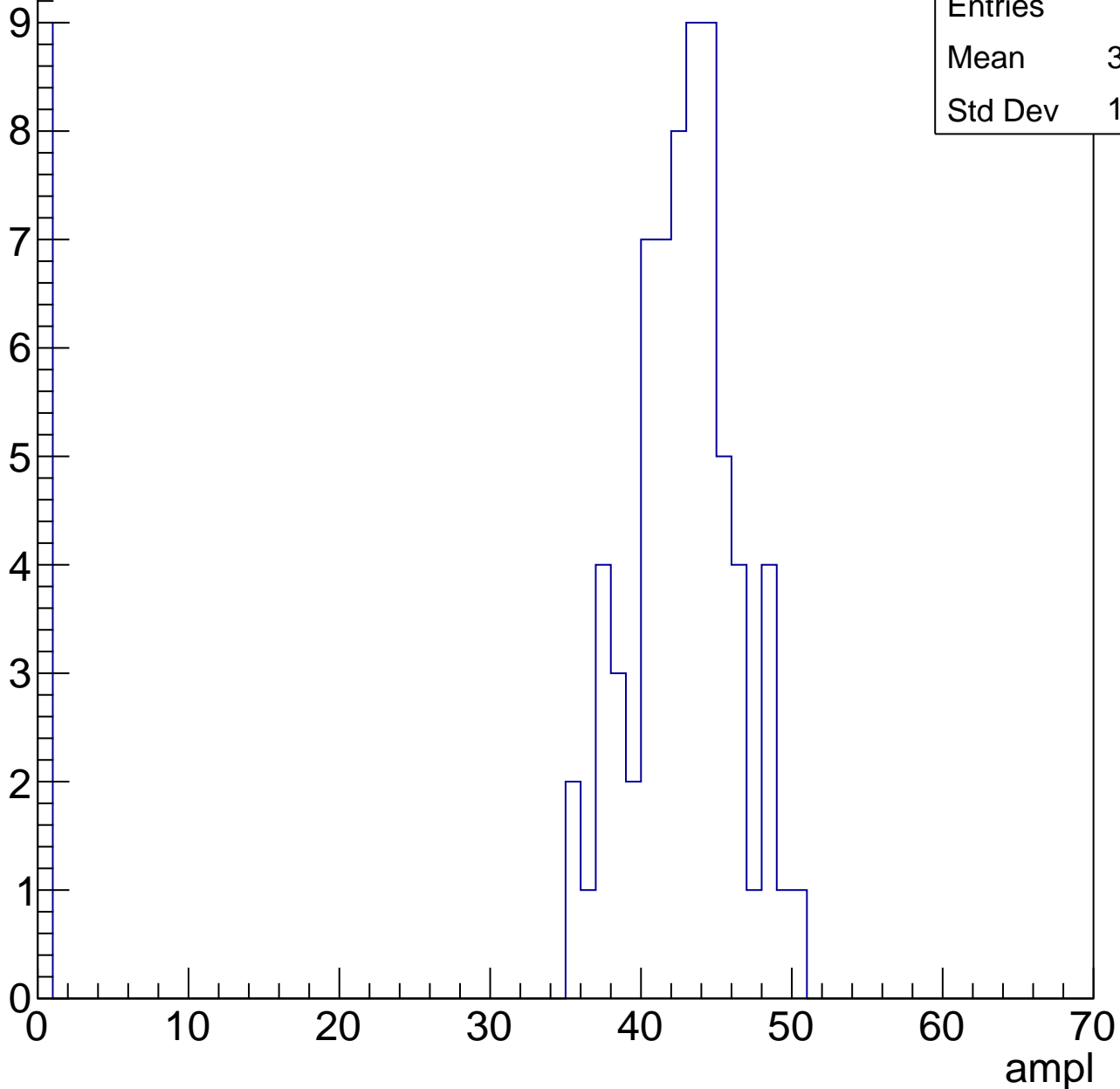


# B1L103S, U25-ch76, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	77
Mean	37.39
Std Dev	13.96

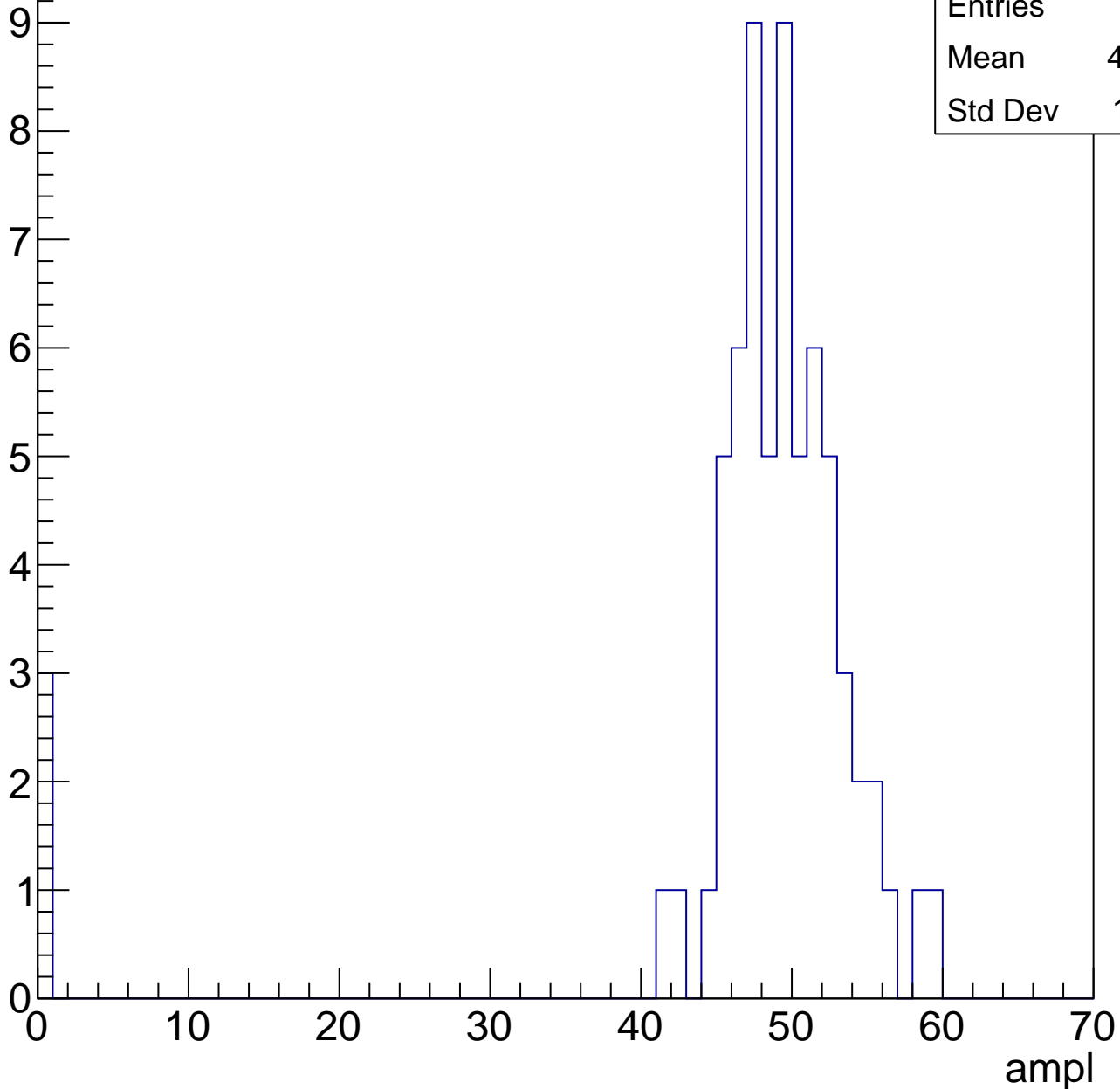


# B1L103S, U25-ch76, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	66
Mean	46.94
Std Dev	10.81

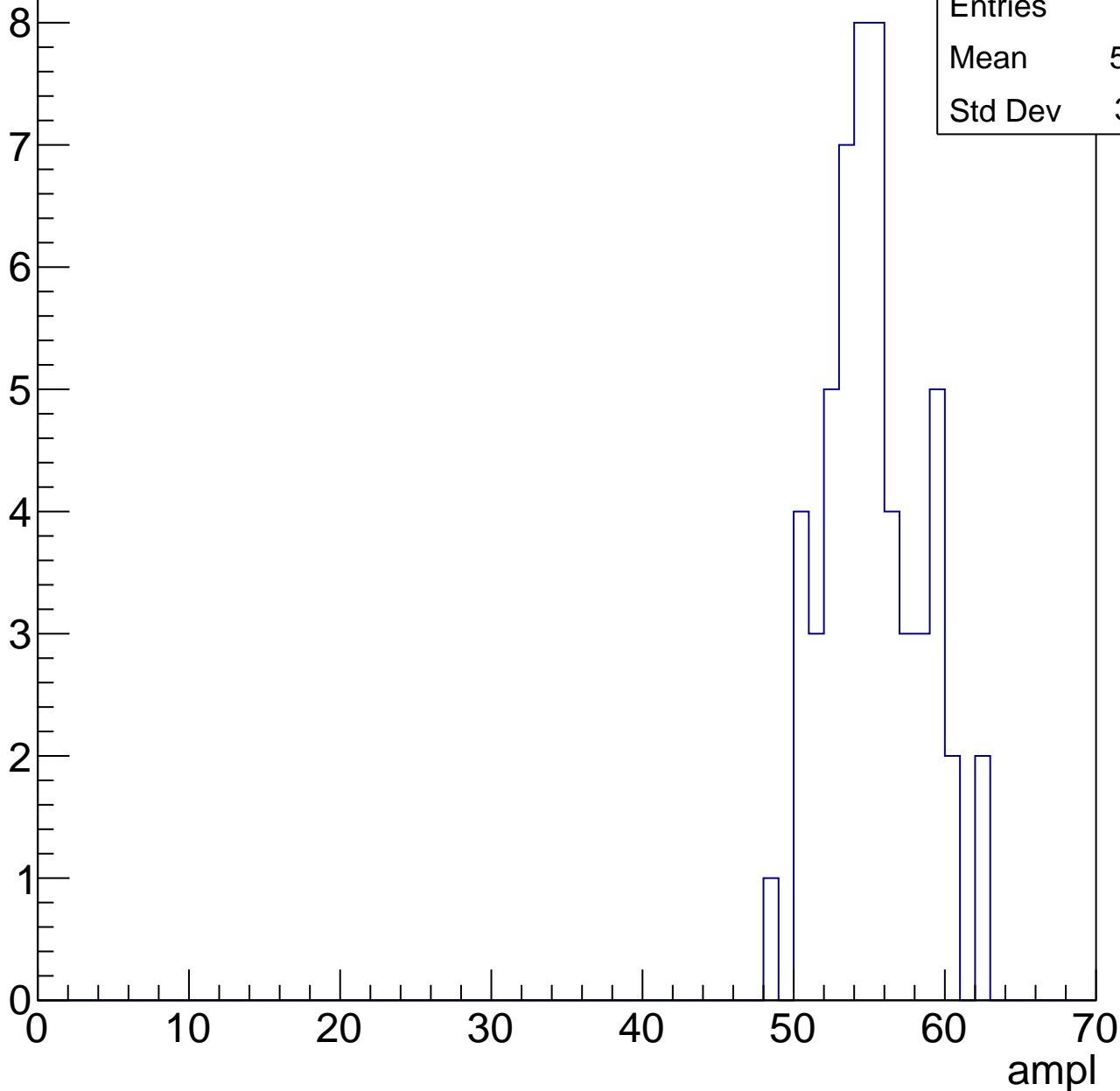


# B1L103S, U25-ch76, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	55
Mean	54.76
Std Dev	3.151

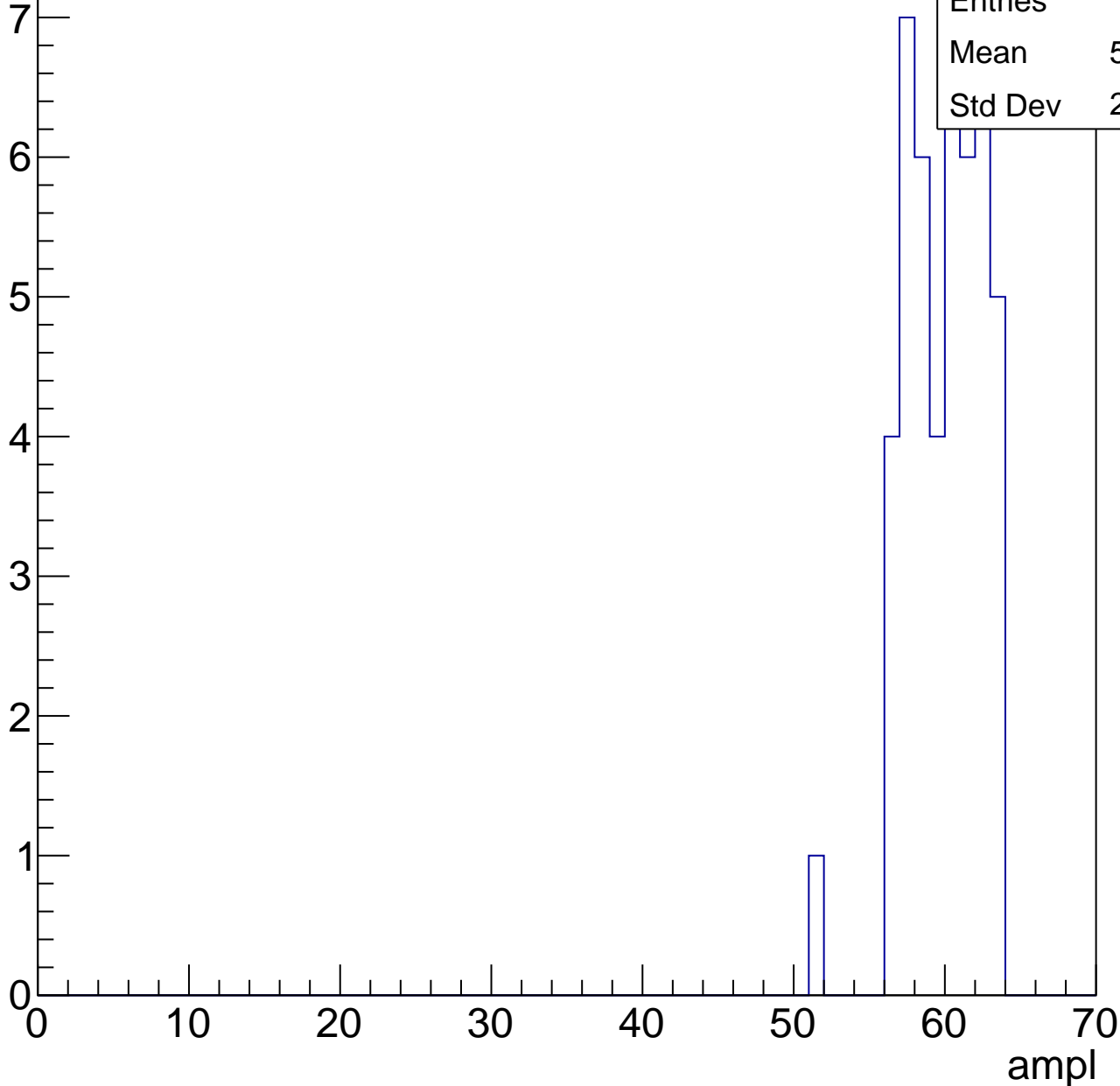


# B1L103S, U25-ch76, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	47
Mean	59.43
Std Dev	2.524

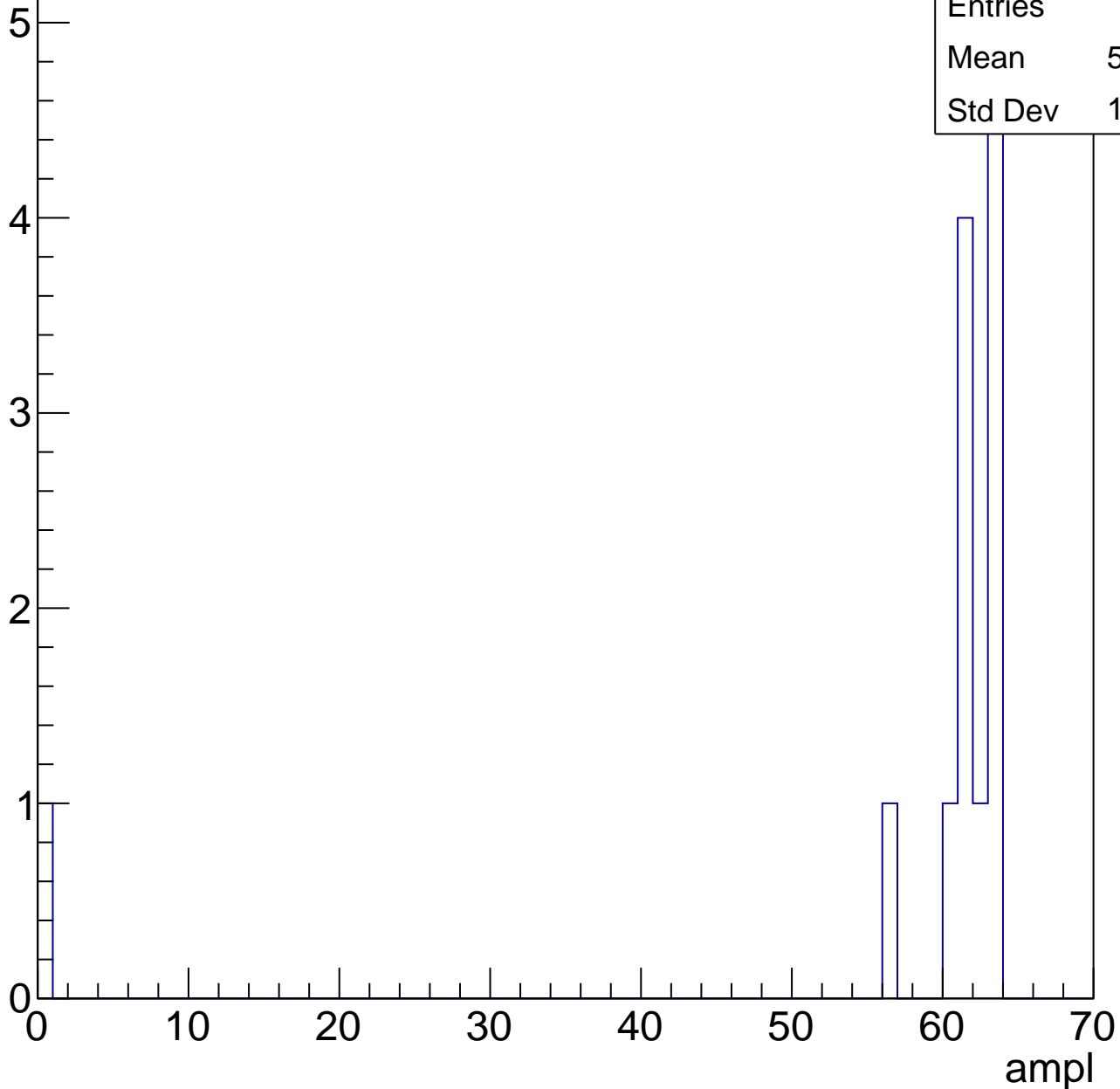


# B1L103S, U25-ch76, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	13
Mean	56.69
Std Dev	16.47





# B1L103S, U25-ch76, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

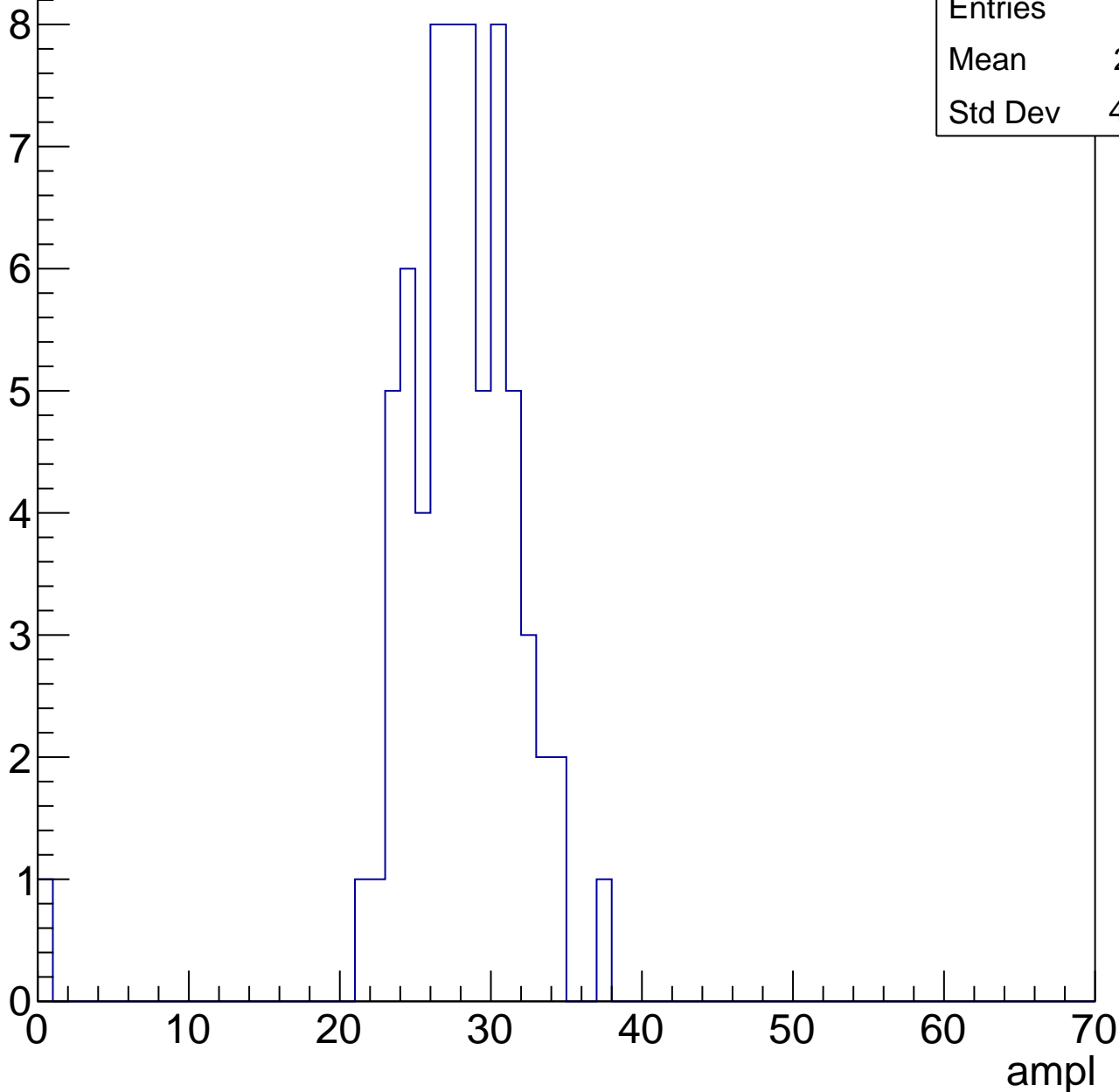
Entries	19
Mean	0
Std Dev	0

# B1L103S, U25-ch77, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	68
Mean	27.31
Std Dev	4.644

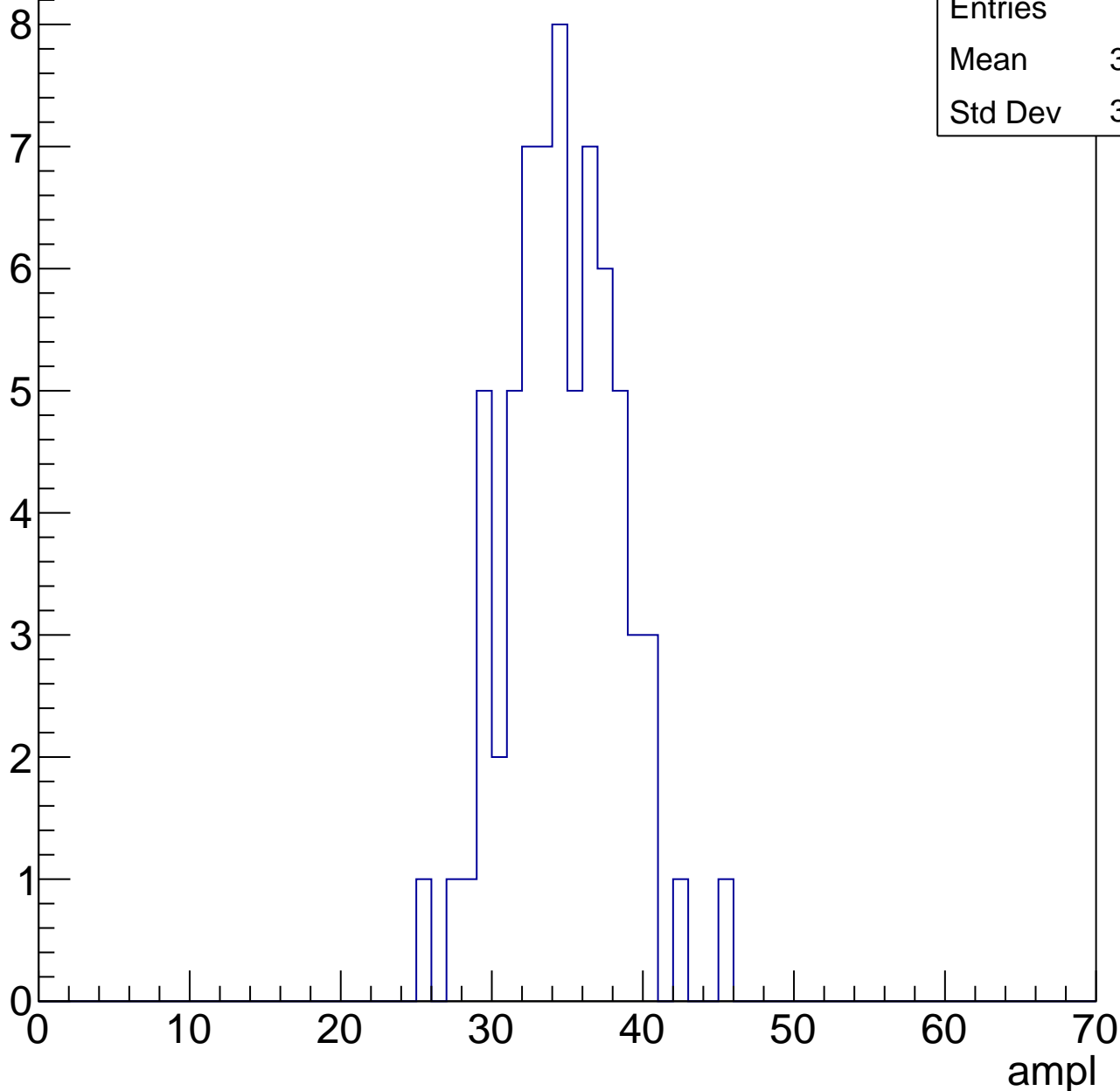


# B1L103S, U25-ch77, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	68
Mean	34.26
Std Dev	3.705

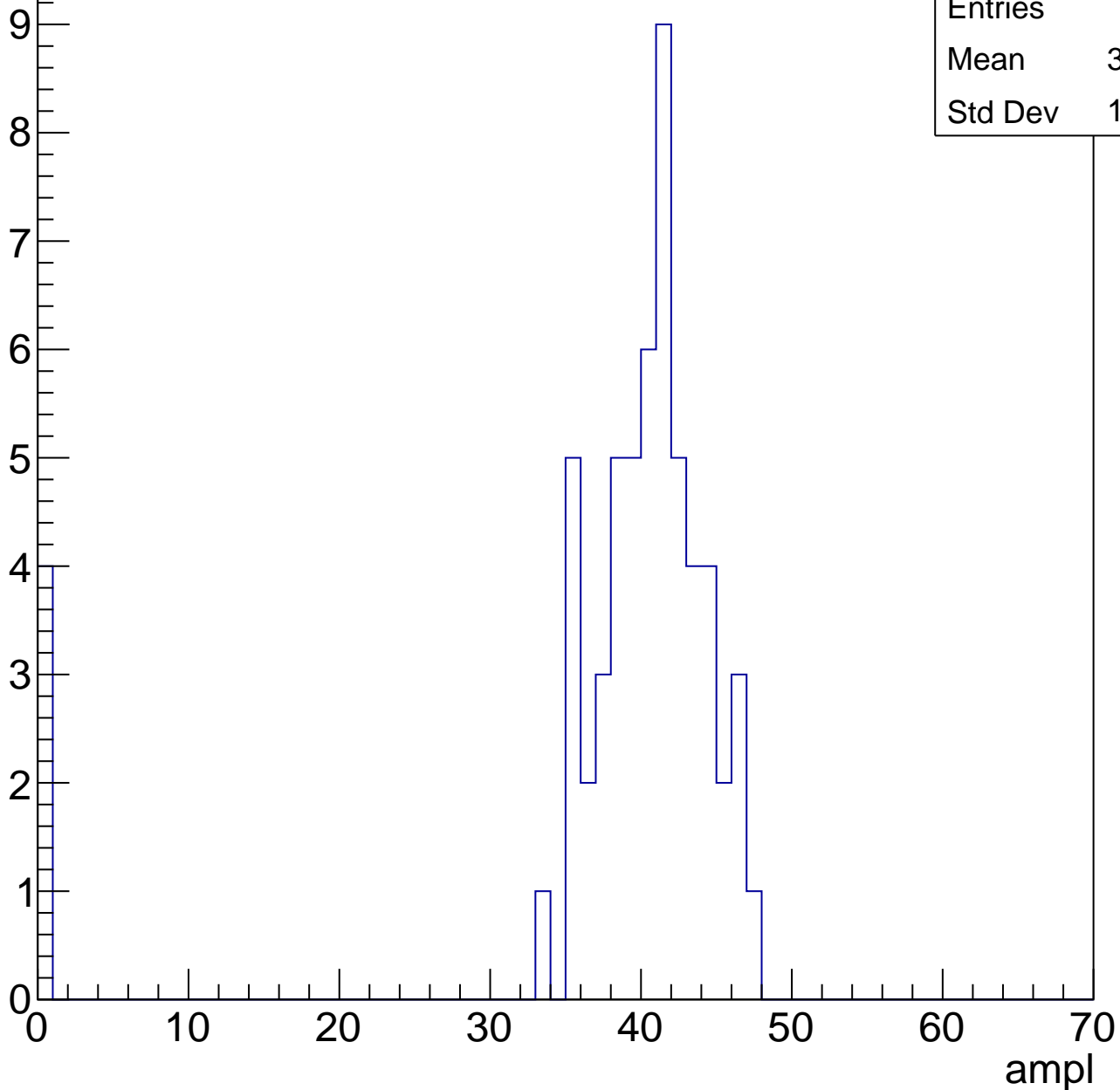


# B1L103S, U25-ch77, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	59
Mean	37.59
Std Dev	10.62

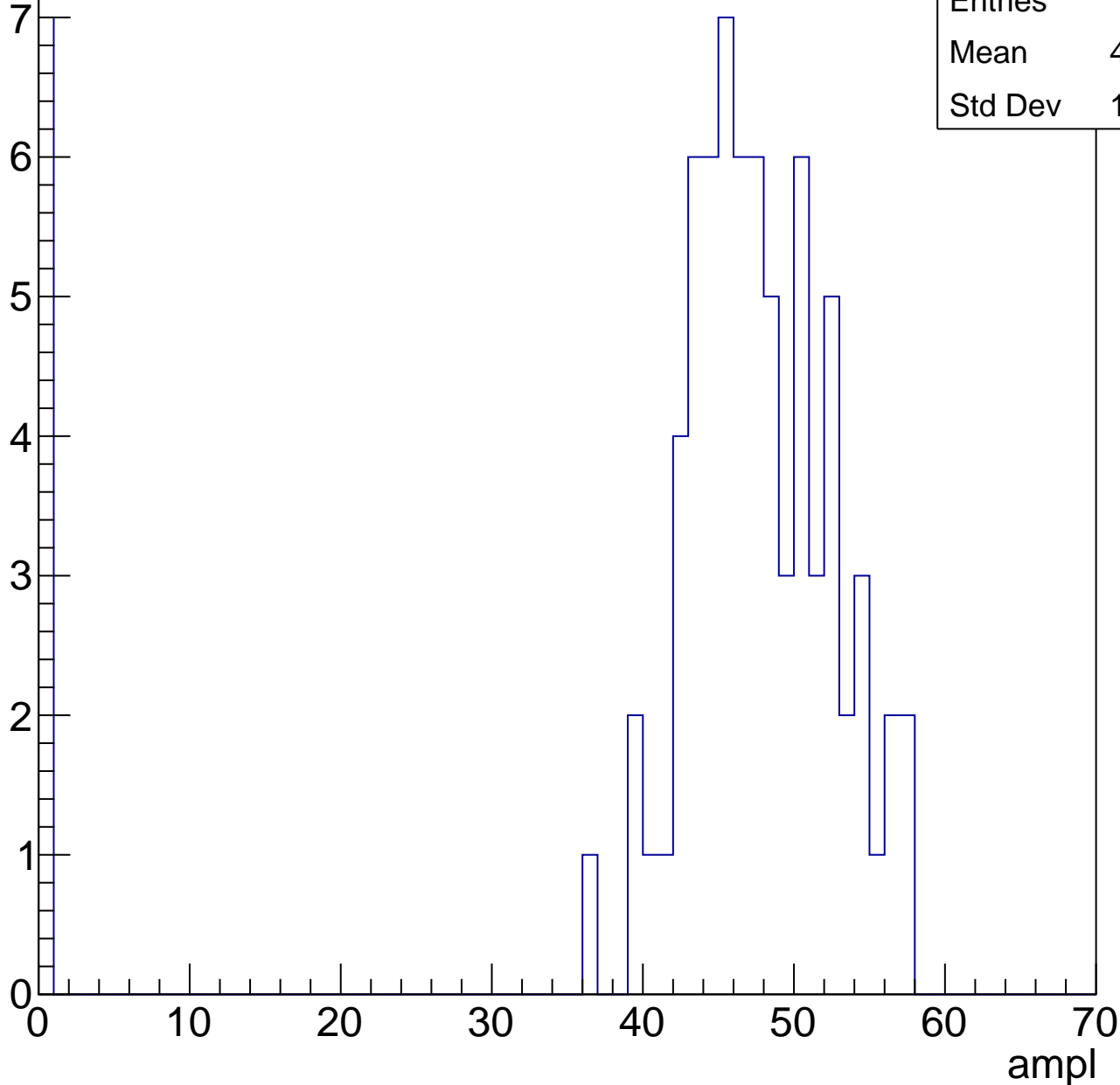


# B1L103S, U25-ch77, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	79
Mean	43.13
Std Dev	14.14

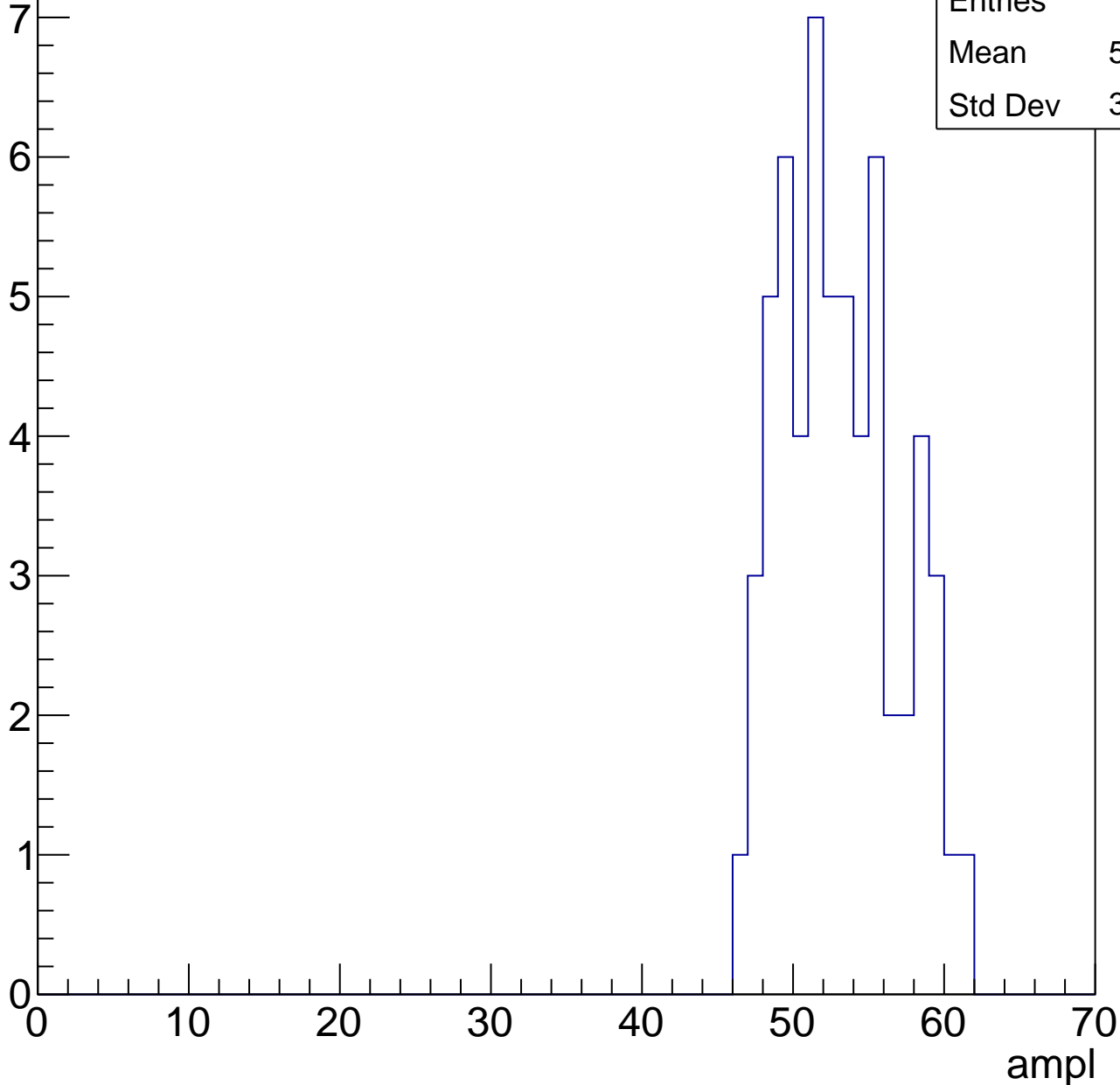


# B1L103S, U25-ch77, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	59
Mean	52.63
Std Dev	3.768



# B1L103S, U25-ch77, adc5

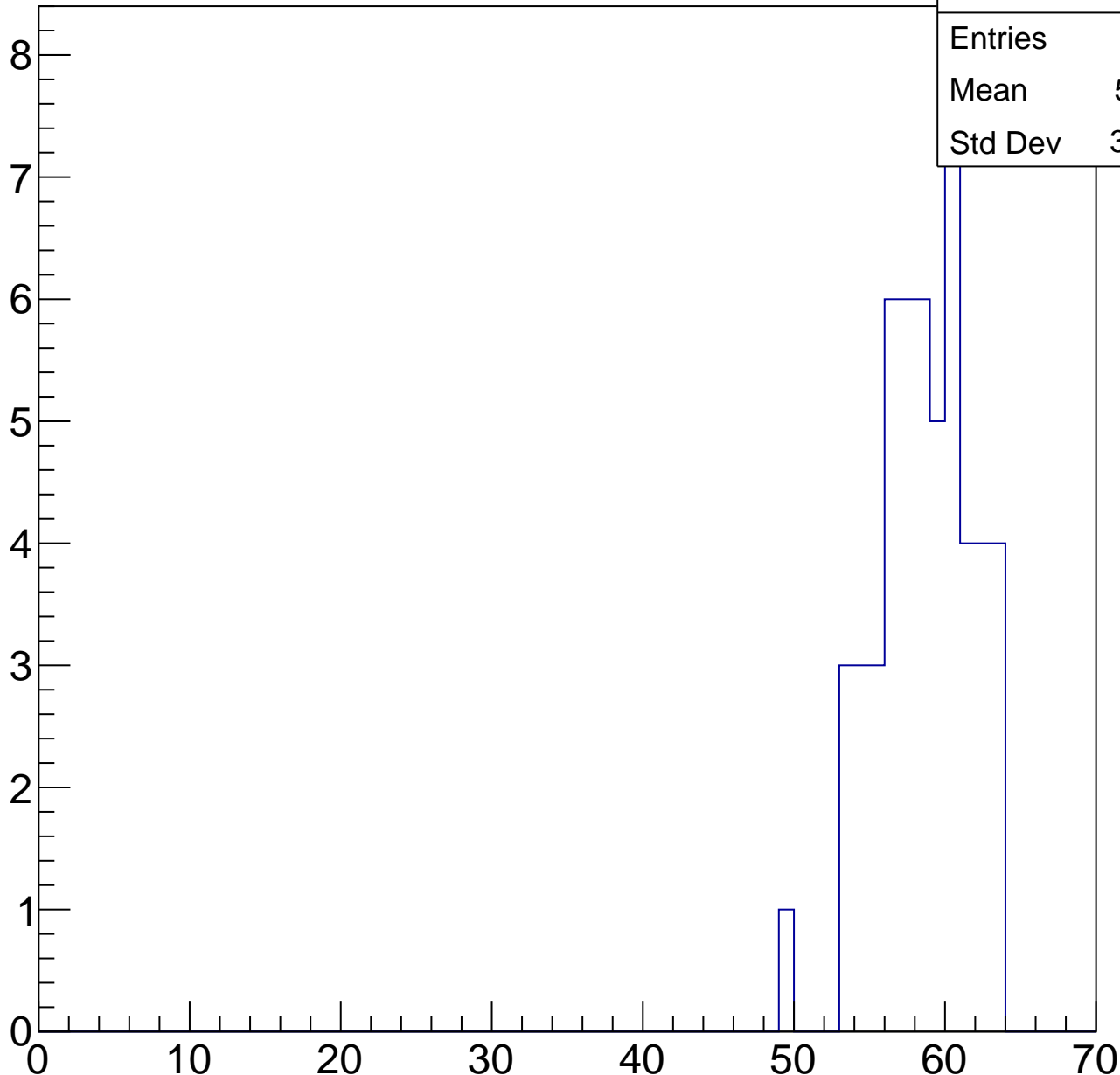
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	53
Mean	58.11
Std Dev	3.063

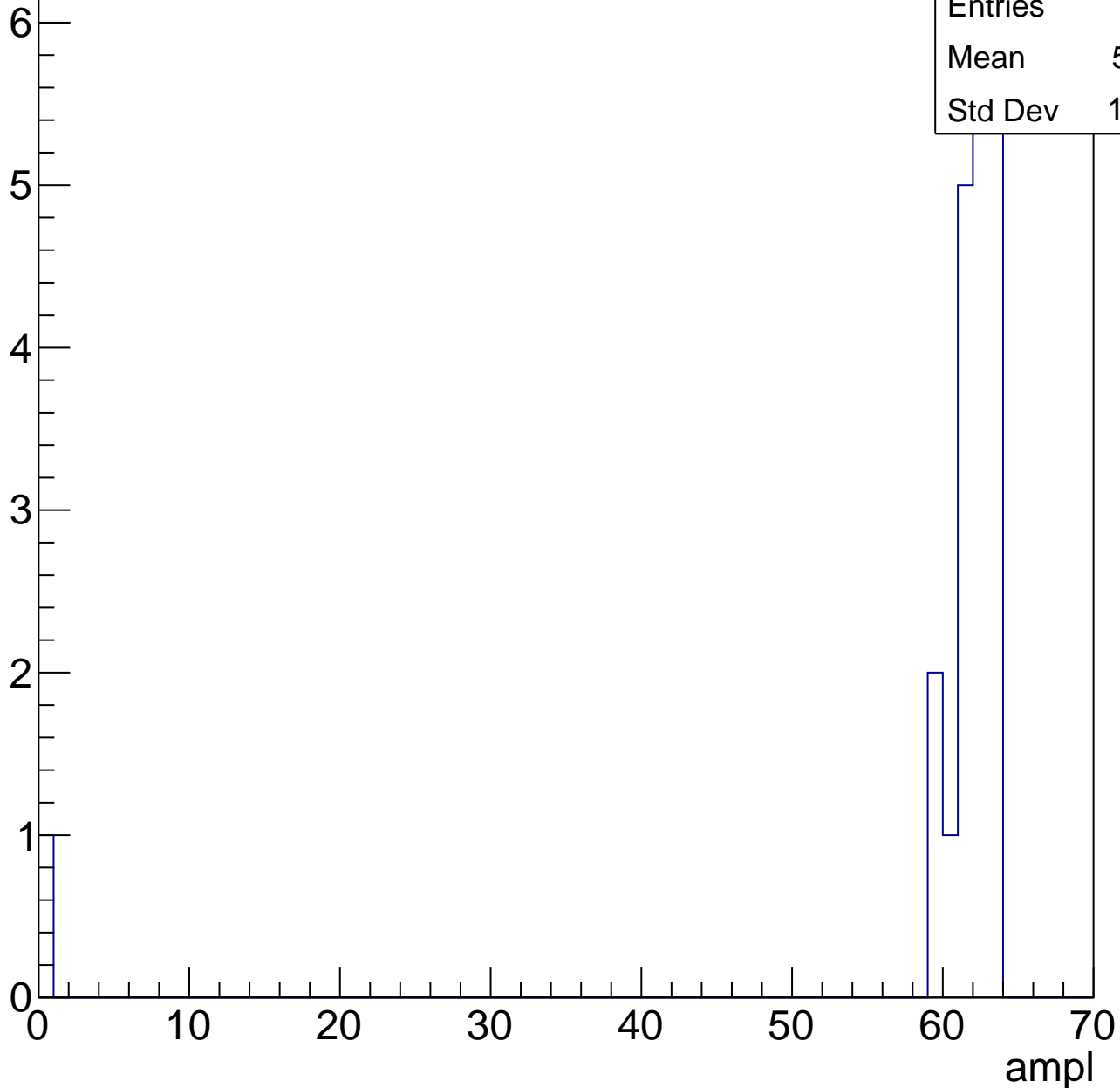
ampl



# B1L103S, U25-ch77, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



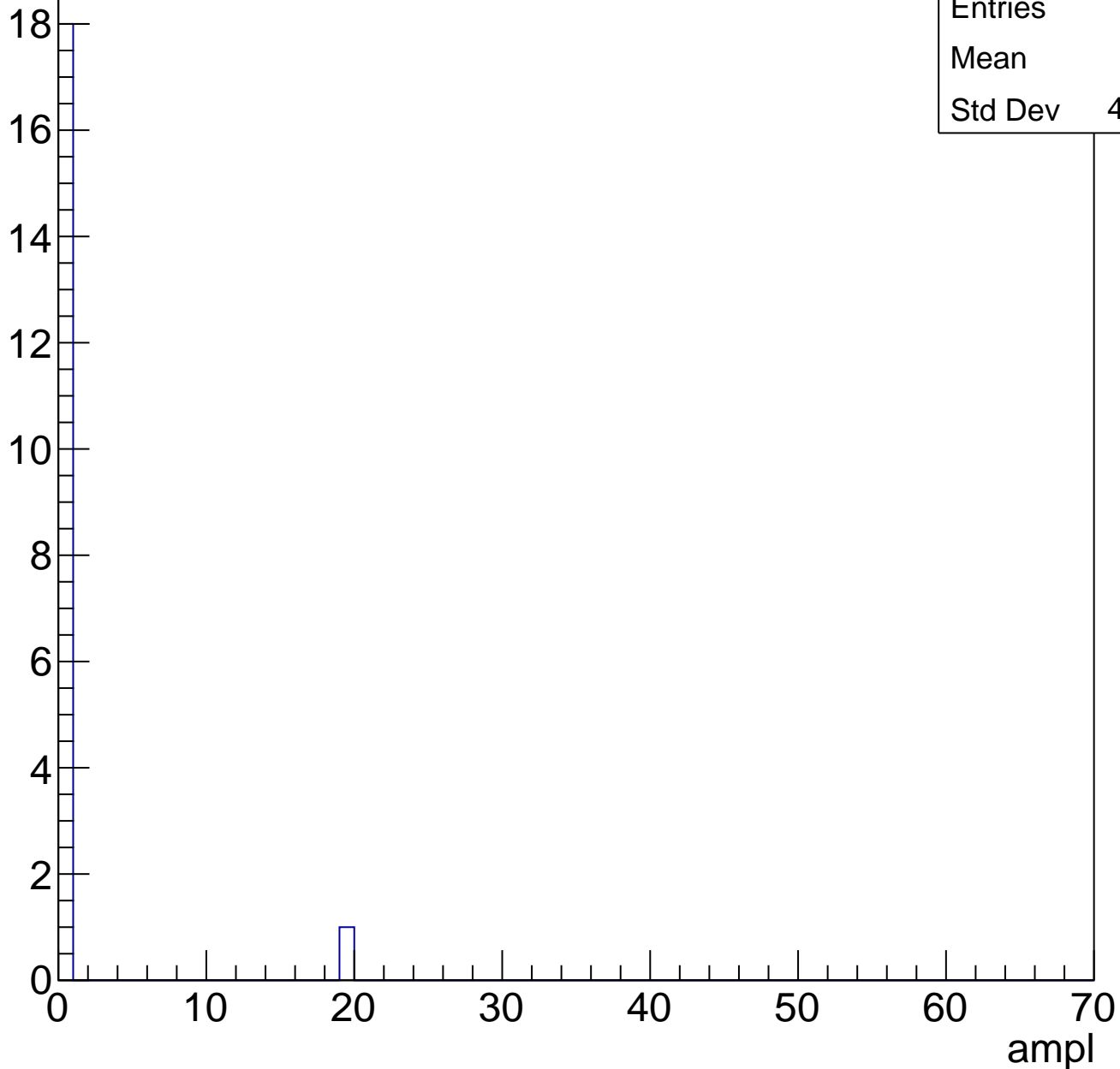


# B1L103S, U25-ch77, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	19
Mean	1
Std Dev	4.243

Entry



# B1L103S, U25-ch78, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

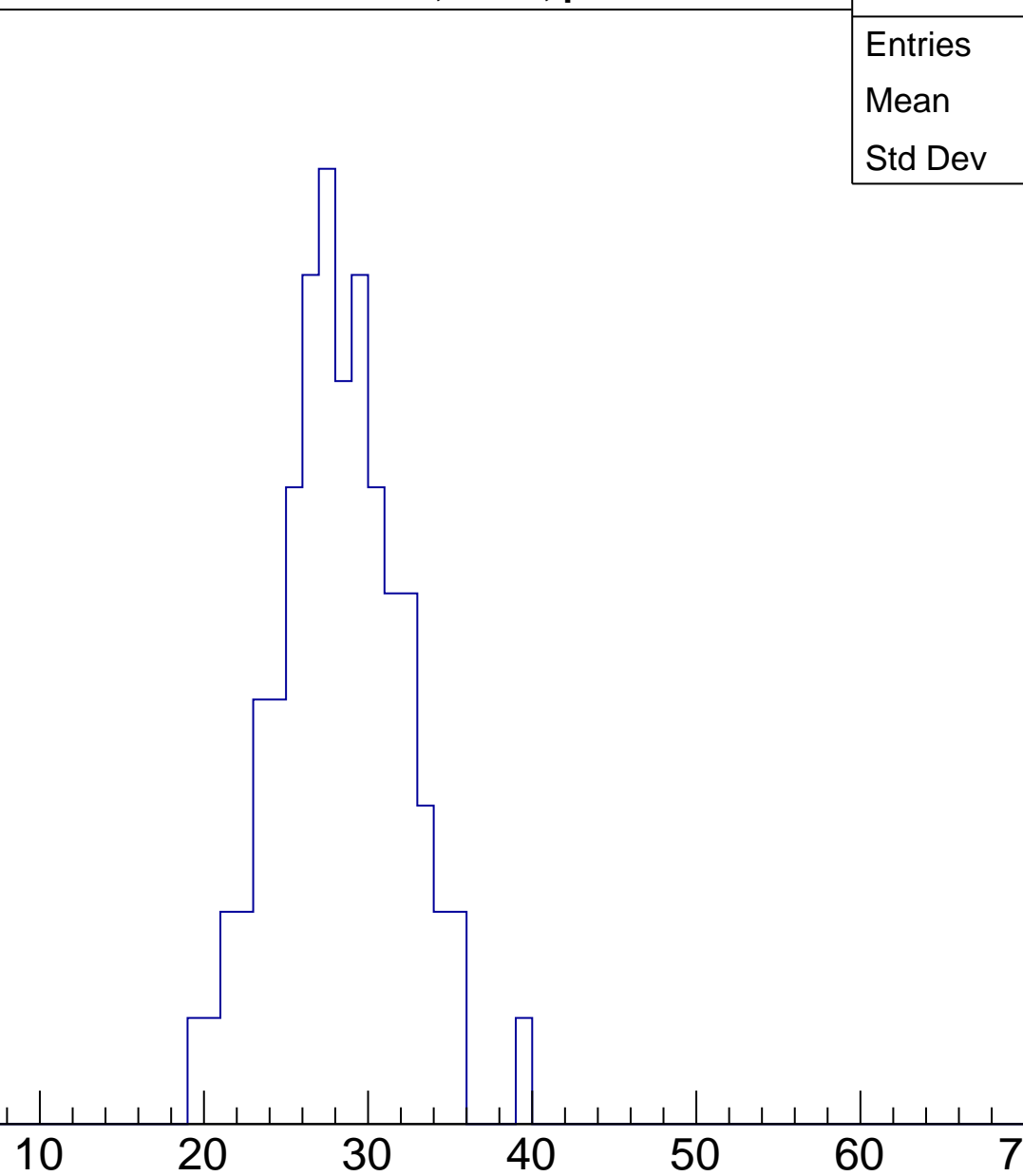
Entries	86
Mean	24.57
Std Dev	9.6

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

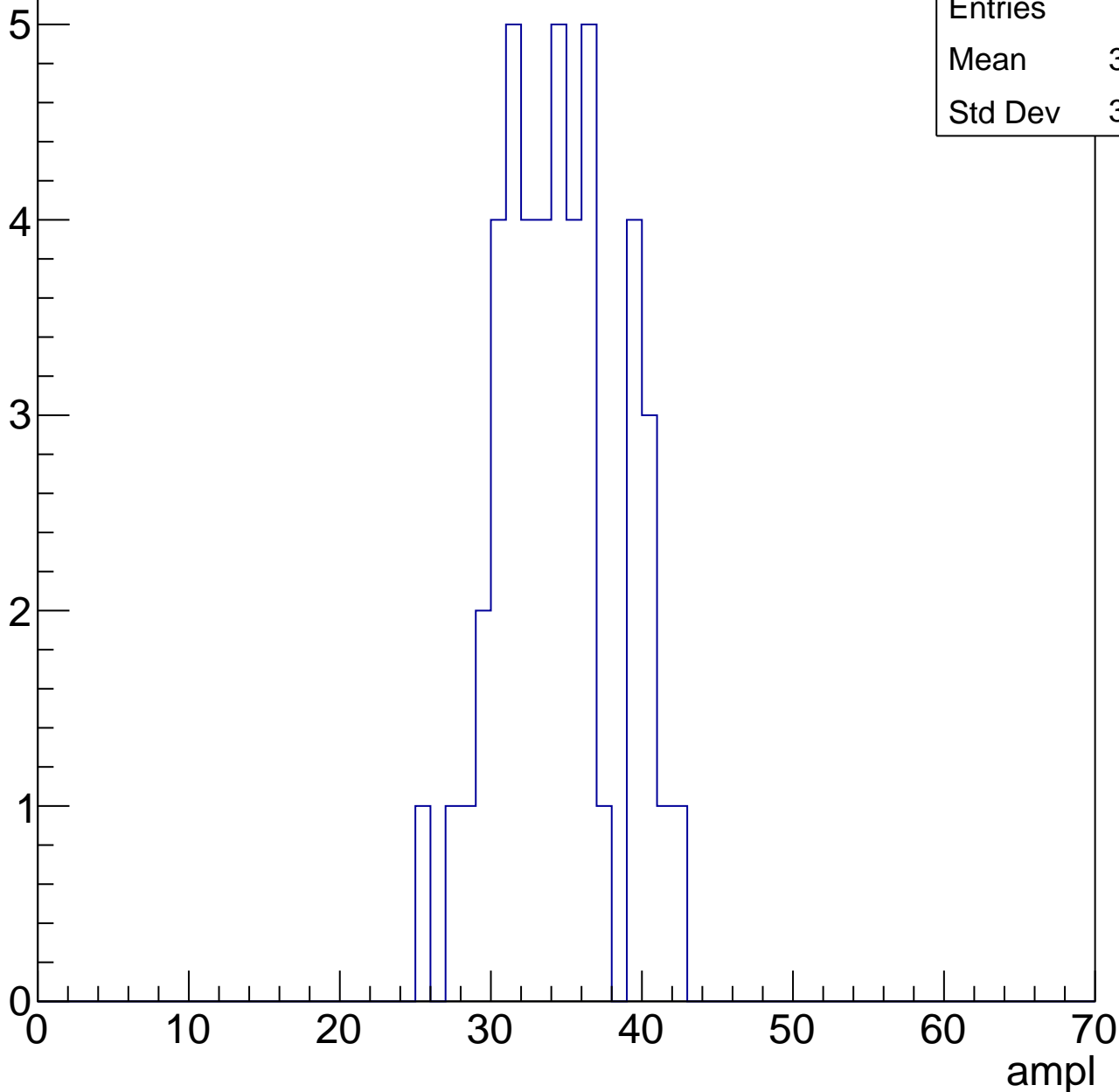


# B1L103S, U25-ch78, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

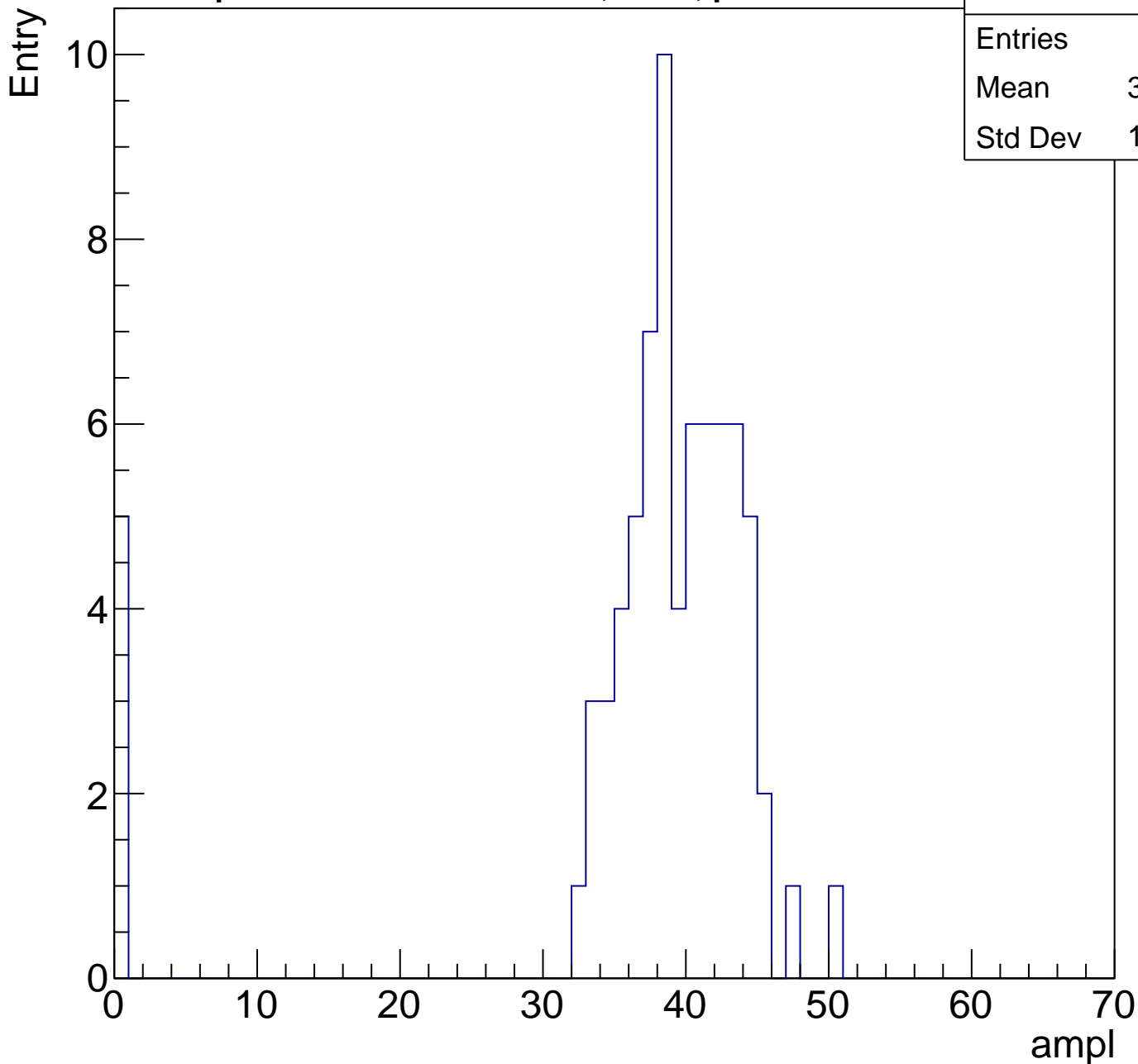
Entries	46
Mean	33.89
Std Dev	3.897



# B1L103S, U25-ch78, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	75
Mean	36.68
Std Dev	10.42

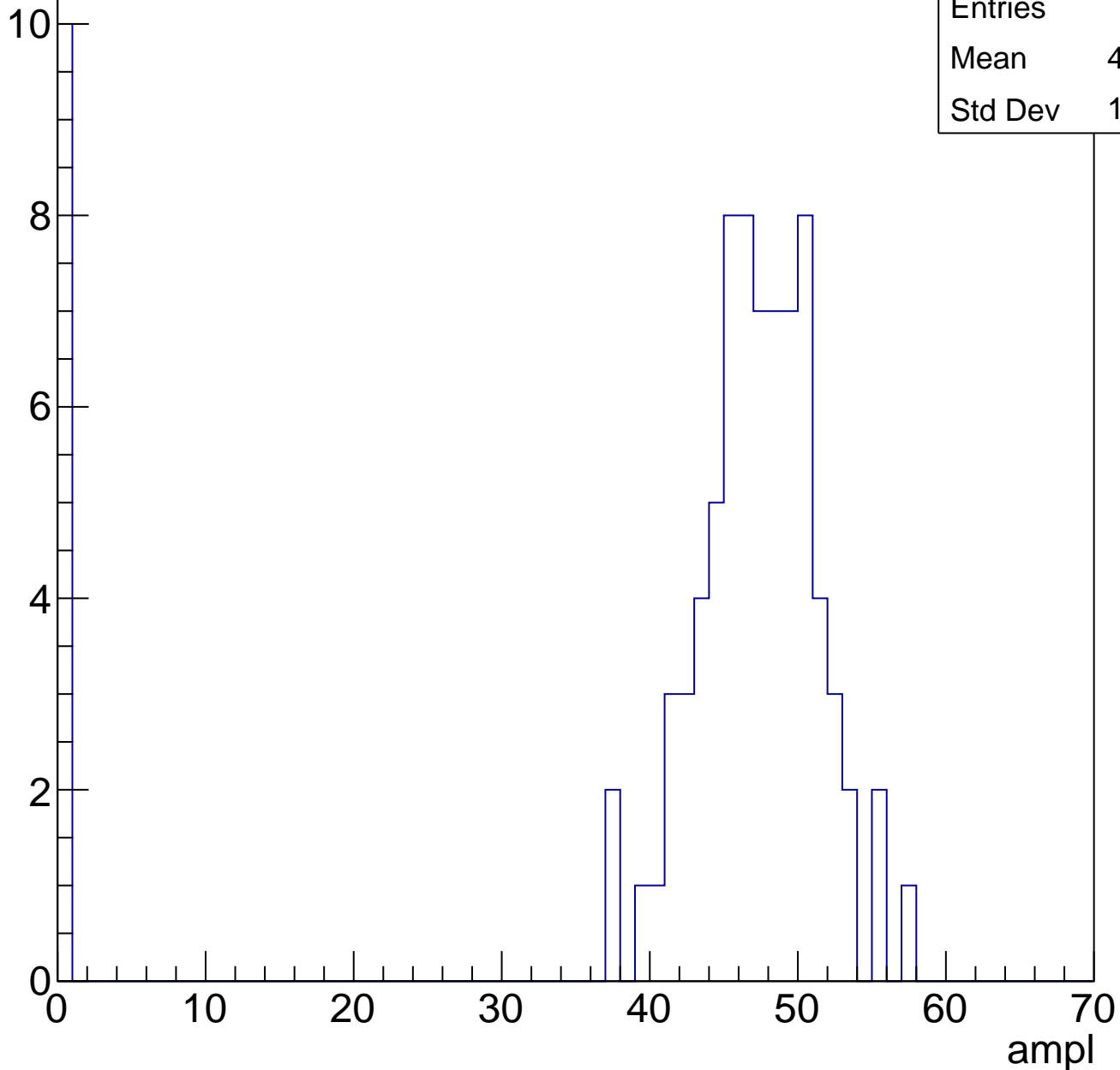


# B1L103S, U25-ch78, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	86
Mean	41.43
Std Dev	15.48

Entry

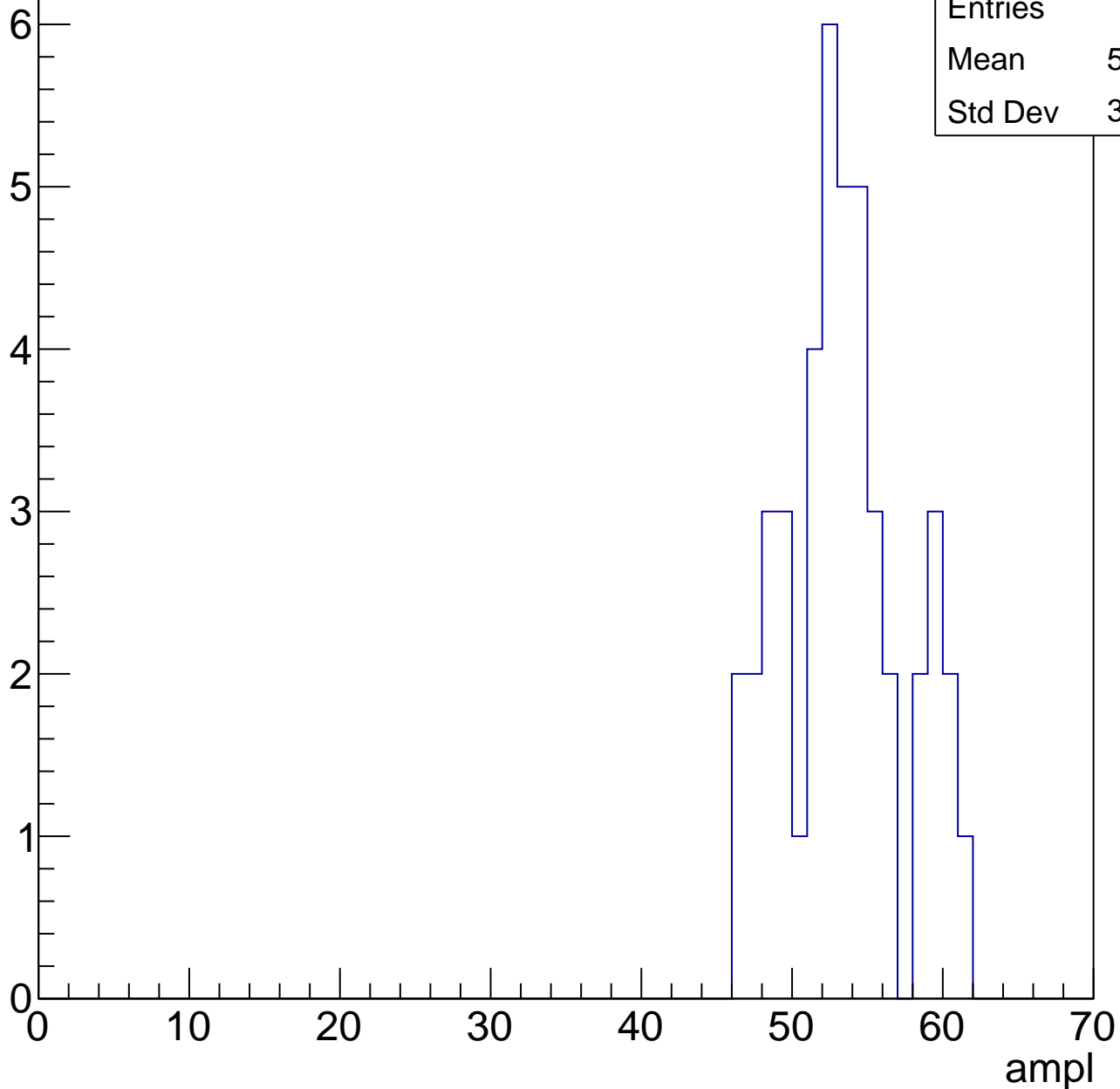


# B1L103S, U25-ch78, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

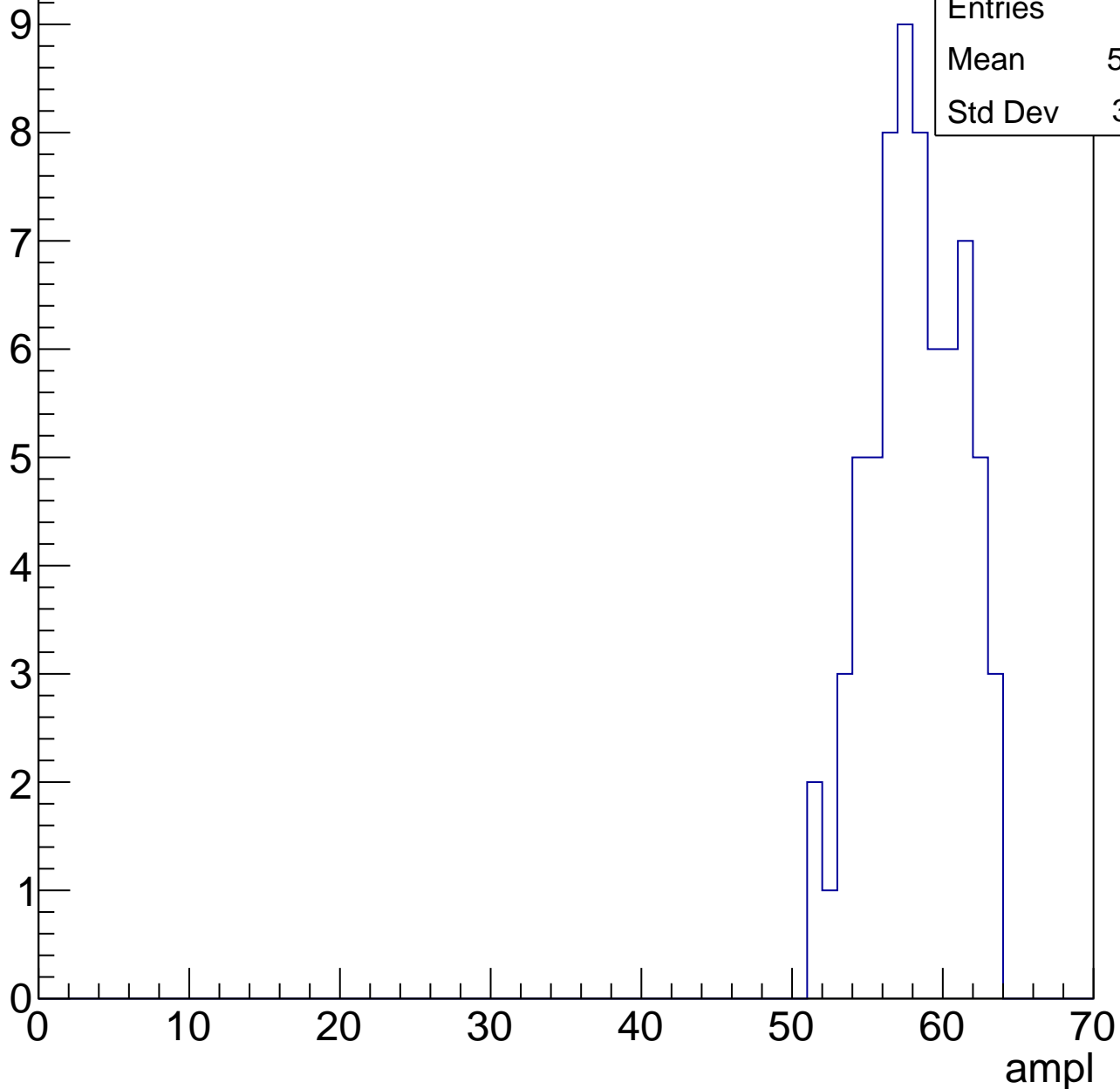
Entries	44
Mean	52.93
Std Dev	3.928



# B1L103S, U25-ch78, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



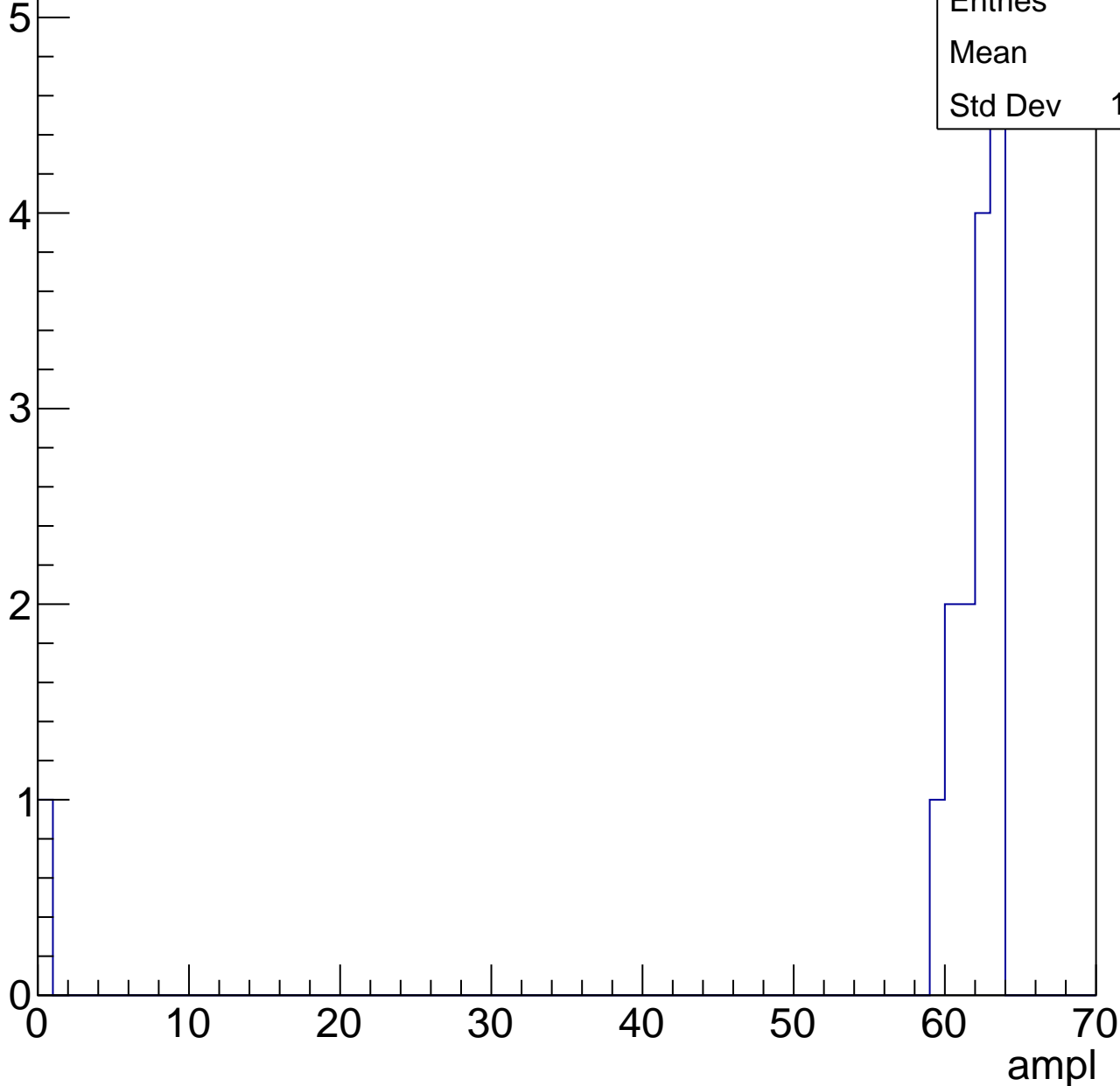
Entries	68
Mean	57.69
Std Dev	3.011

# B1L103S, U25-ch78, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	15
Mean	57.6
Std Dev	15.44





# B1L103S, U25-ch78, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	22
Mean	8.545
Std Dev	21.51

Entry



# B1L103S, U25-ch79, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

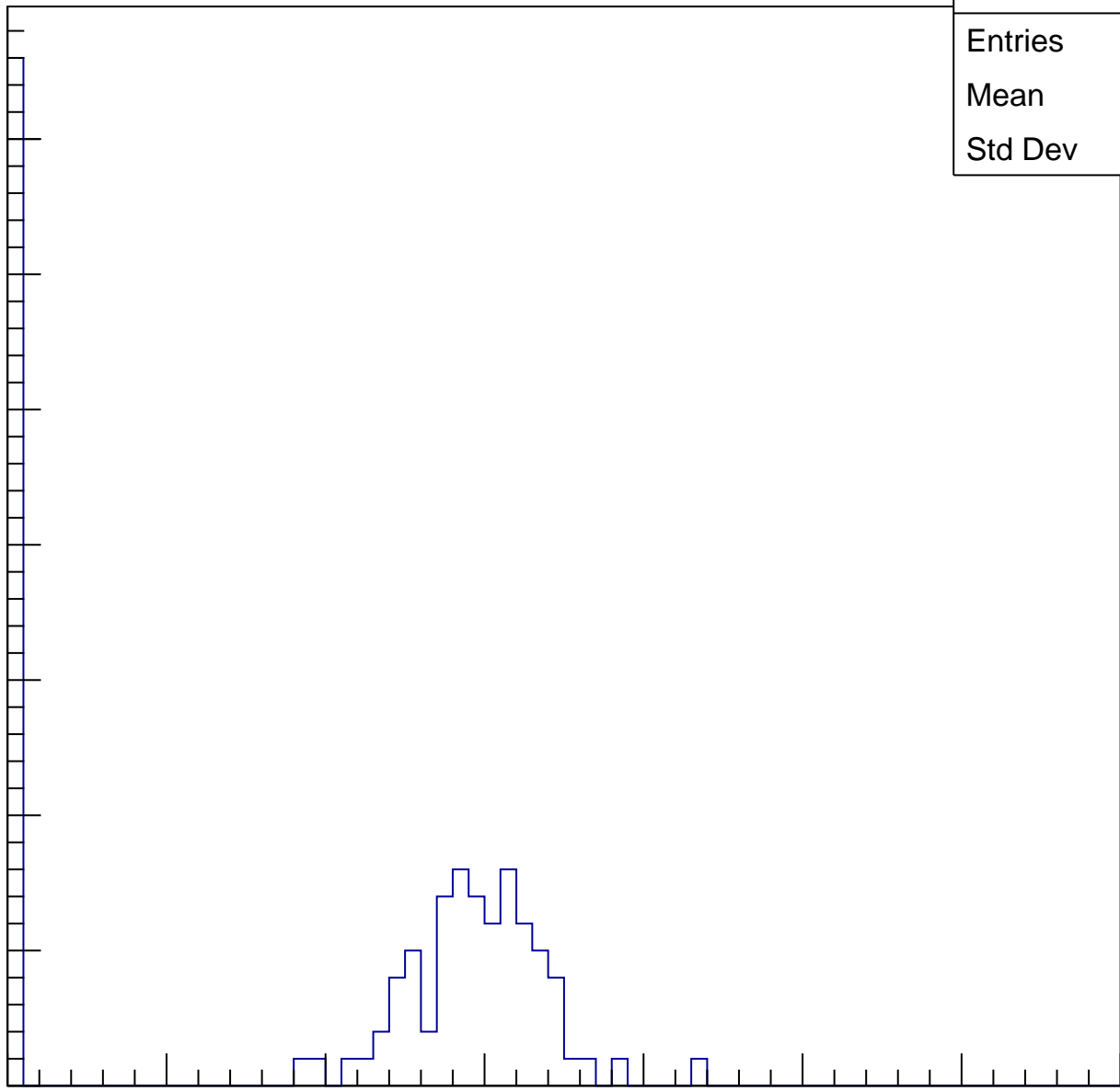
Entries	110
Mean	18.98
Std Dev	14.2

Entry

35  
30  
25  
20  
15  
10  
5  
0

0 10 20 30 40 50 60 70

ampl



# B1L103S, U25-ch79, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	75
Mean	30.64
Std Dev	13.1

Entry

10

8

6

4

2

0

0

10

20

30

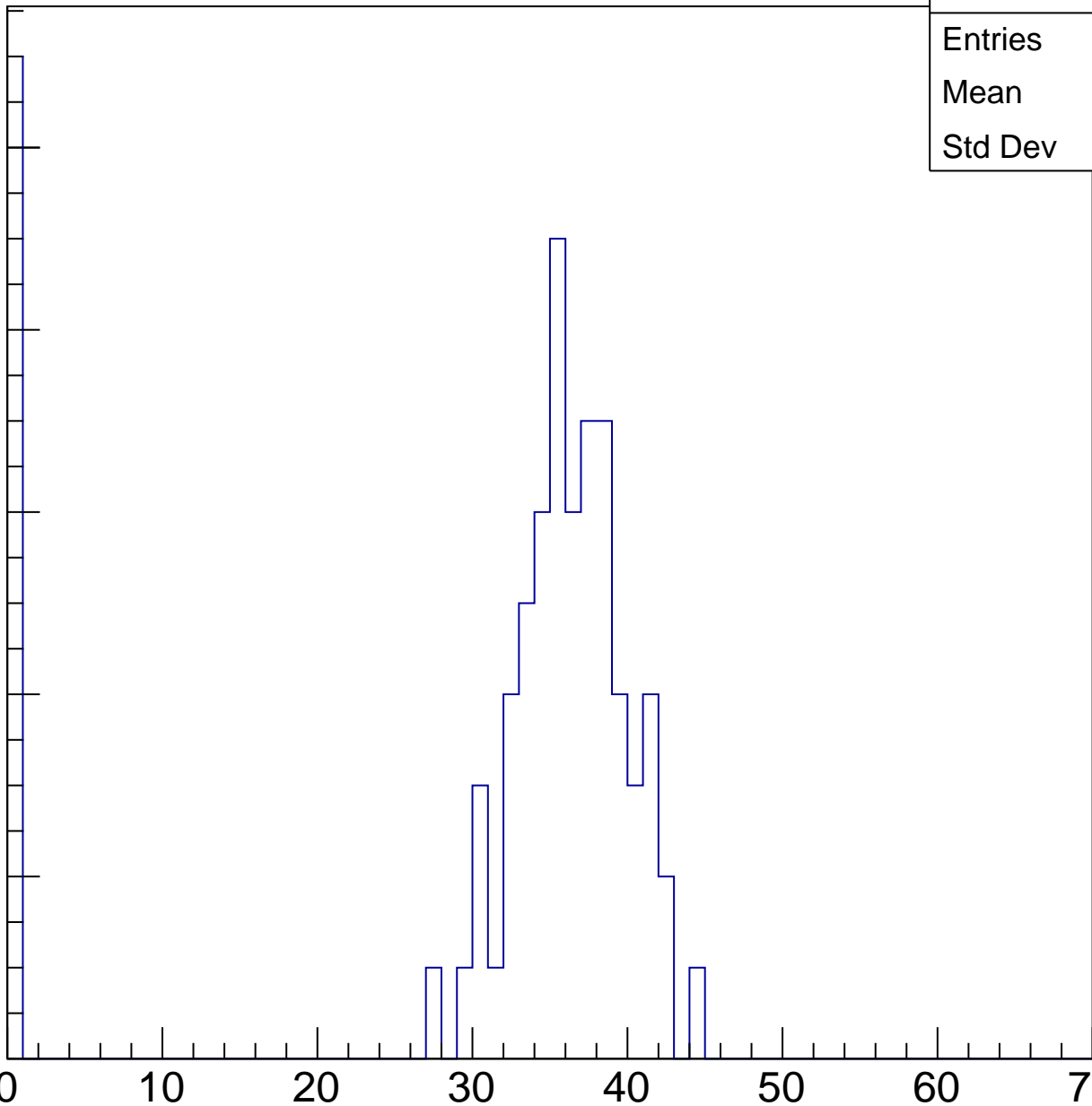
40

50

60

70

ampl

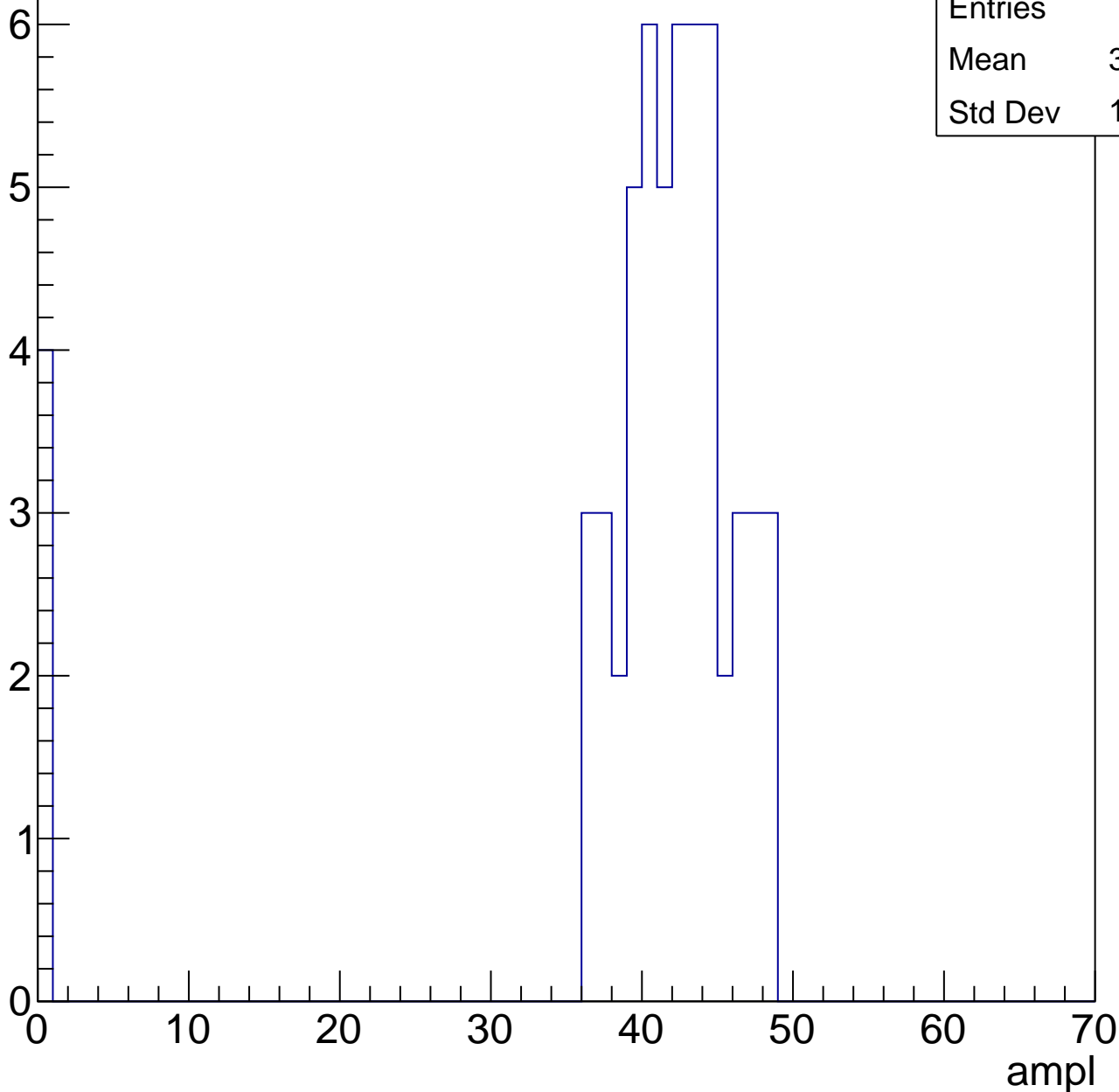


# B1L103S, U25-ch79, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	57
Mean	38.98
Std Dev	11.16



# B1L103S, U25-ch79, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

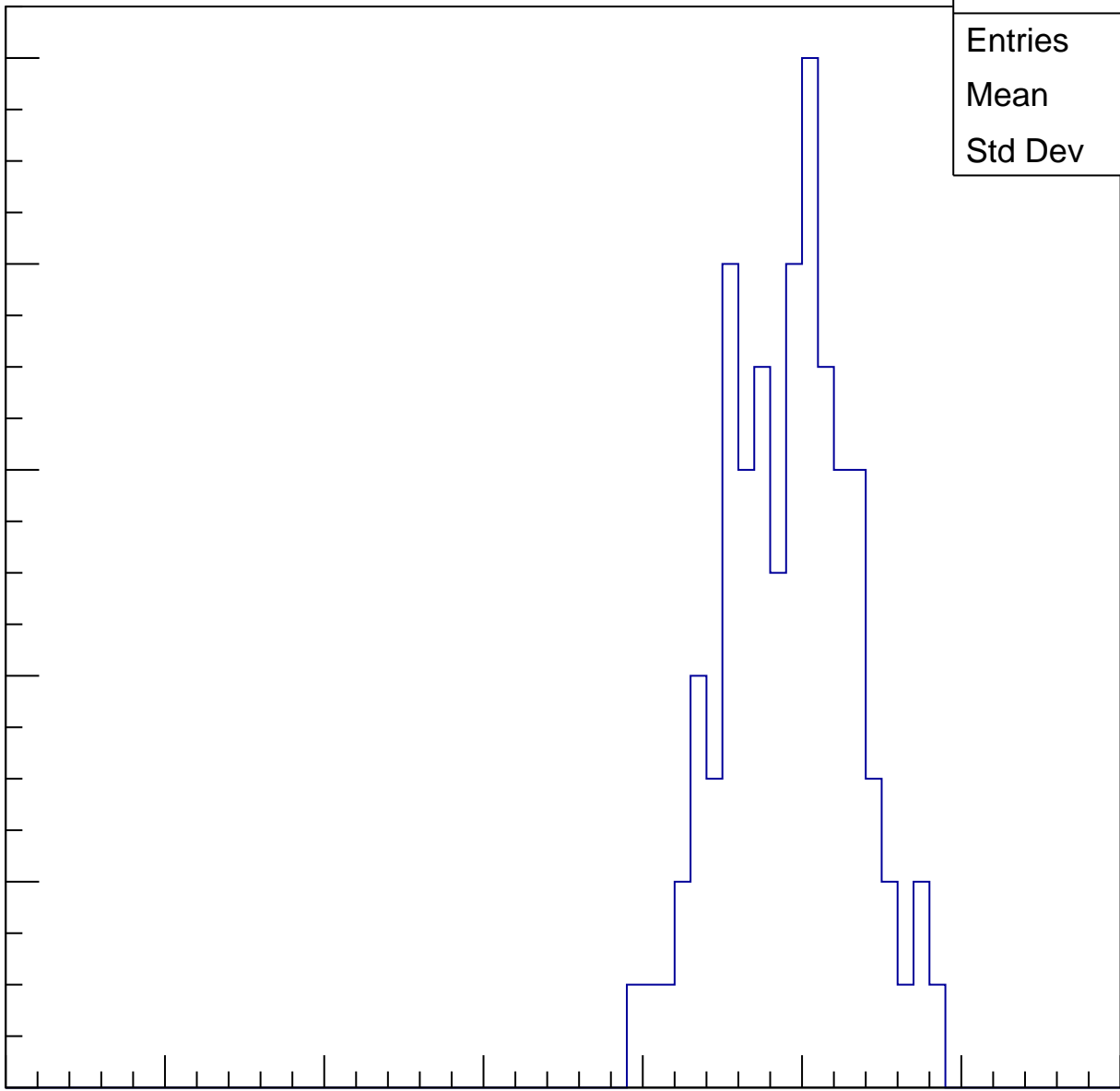
Entries	84
Mean	48.71
Std Dev	4.028

Entry

10  
8  
6  
4  
2  
0

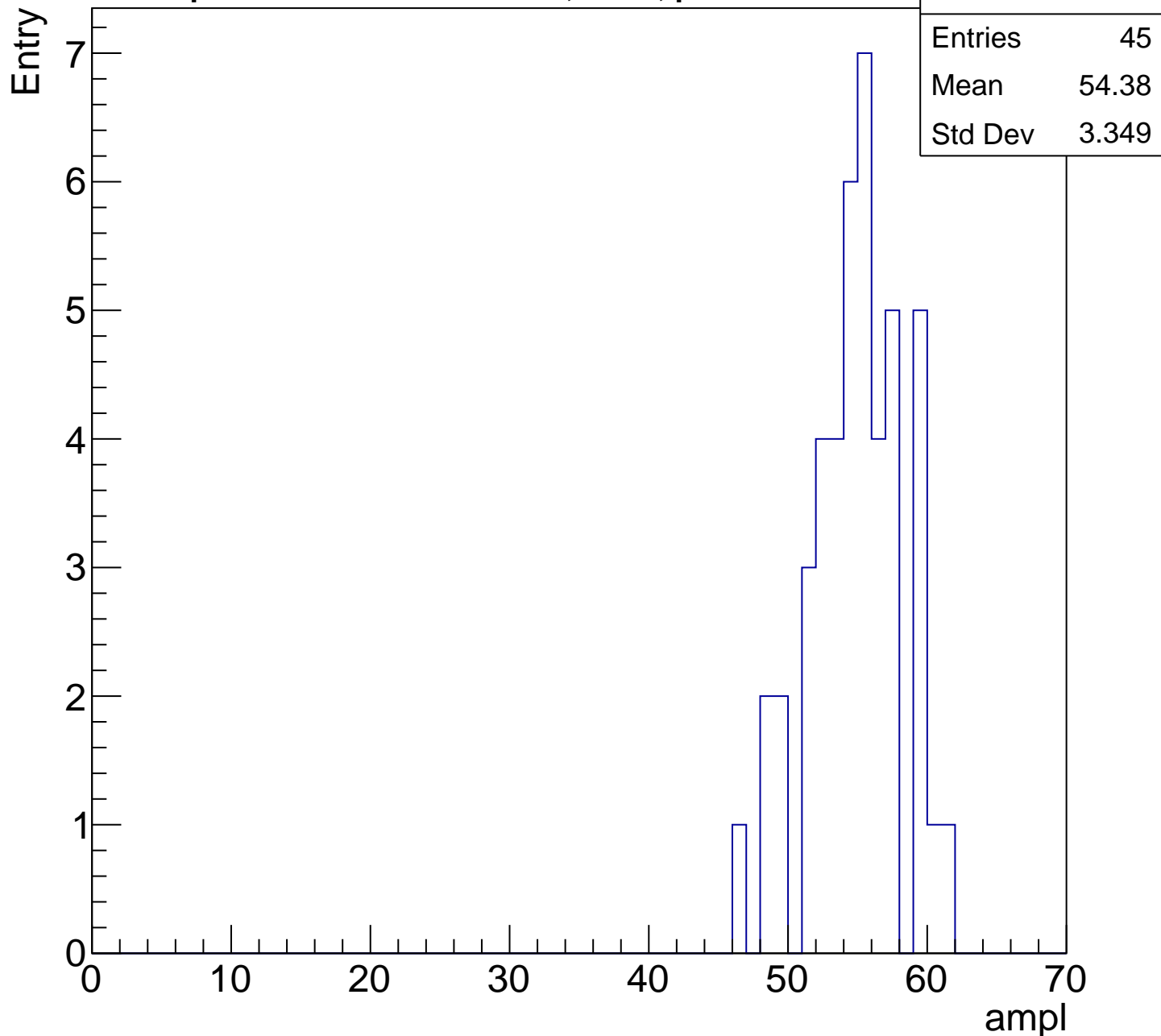
ampl

0 10 20 30 40 50 60 70



# B1L103S, U25-ch79, adc4

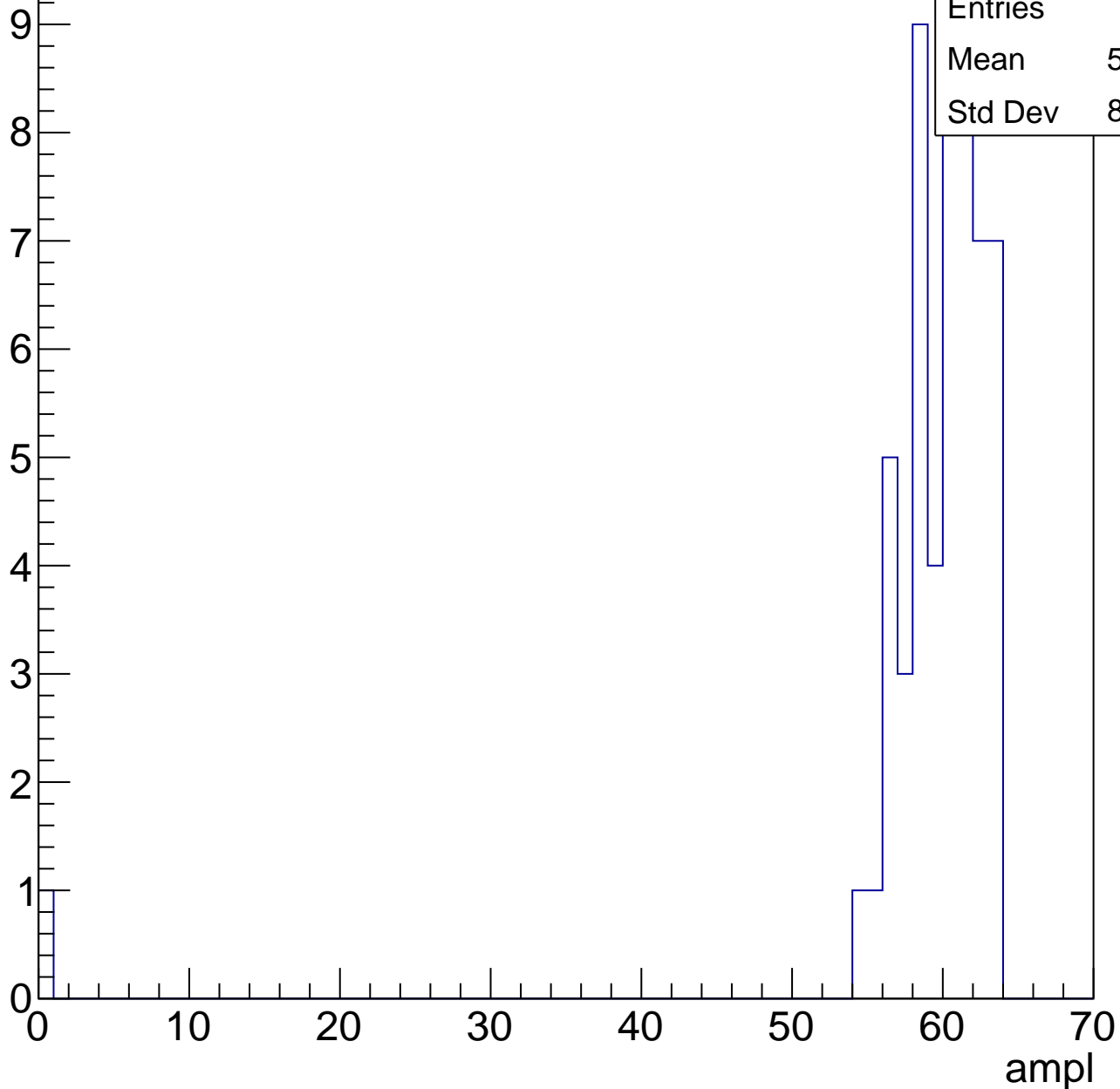
calib\_packv5\_041523\_1651.root, FC#0, port C2



# B1L103S, U25-ch79, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

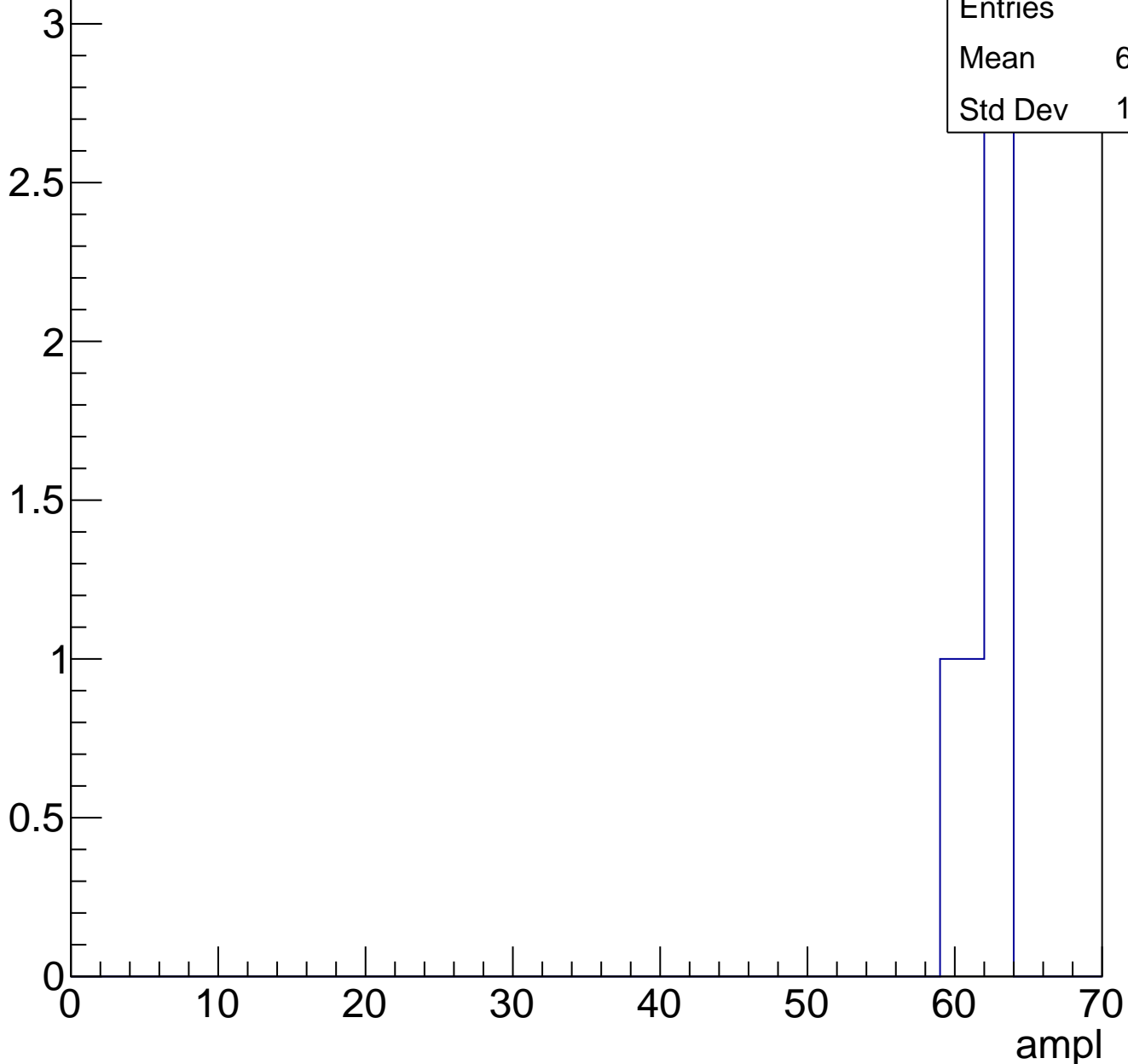


Entries	54
Mean	58.54
Std Dev	8.379

# B1L103S, U25-ch79, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U25-ch79, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

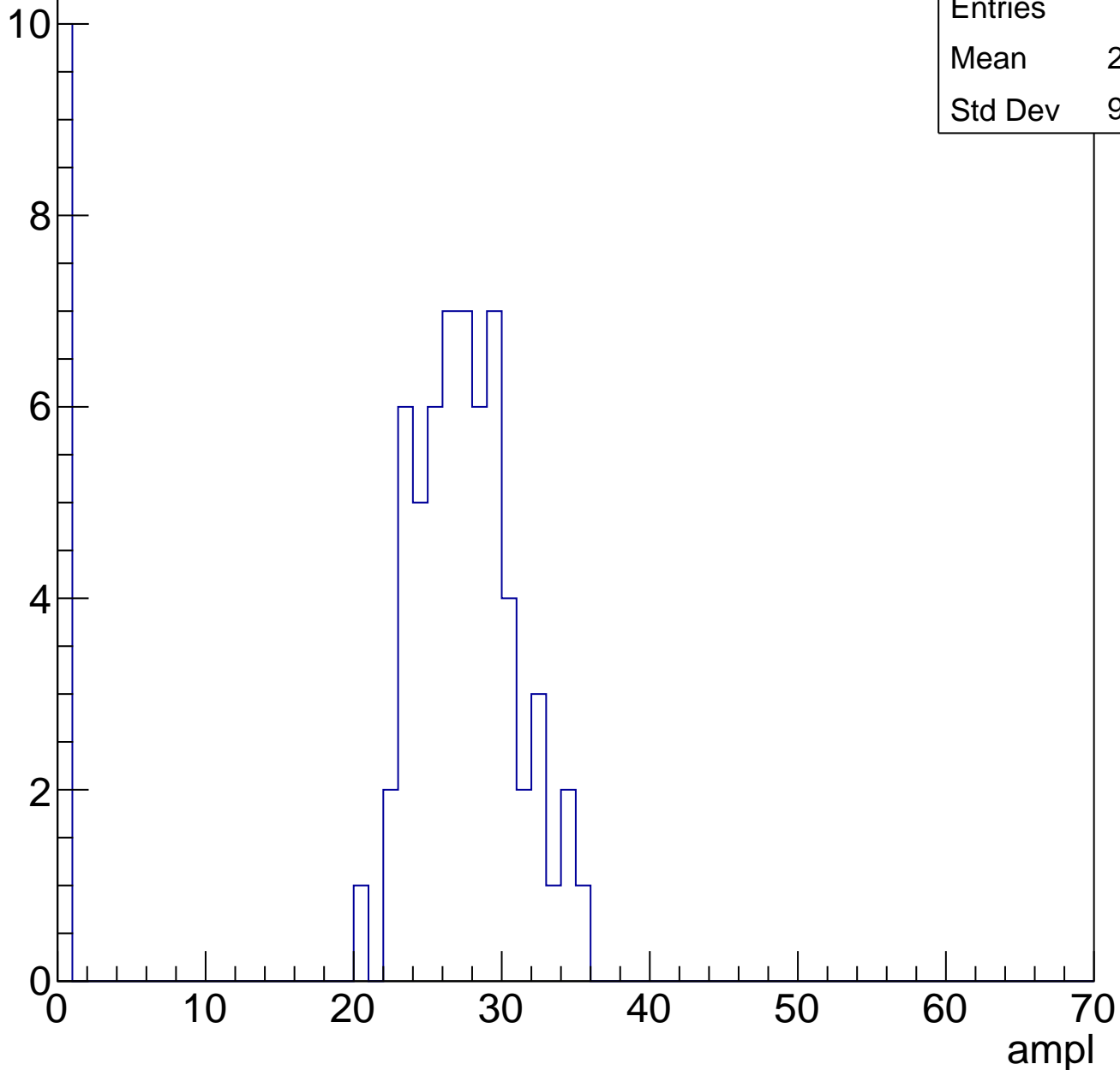
Entries	19
Mean	0
Std Dev	0

# B1L103S, U25-ch80, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	70
Mean	23.26
Std Dev	9.968

Entry

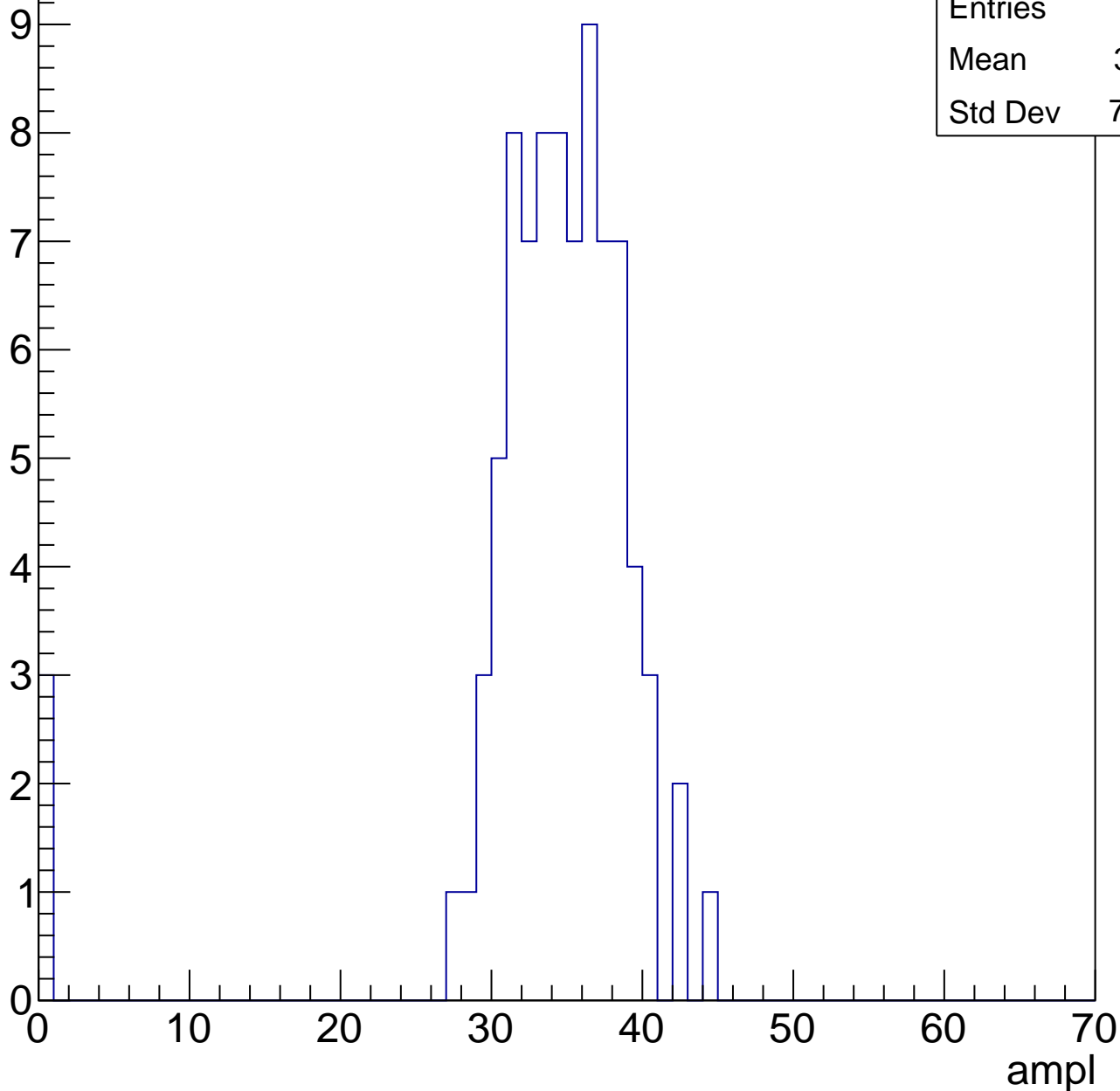


# B1L103S, U25-ch80, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	84
Mean	33.31
Std Dev	7.262

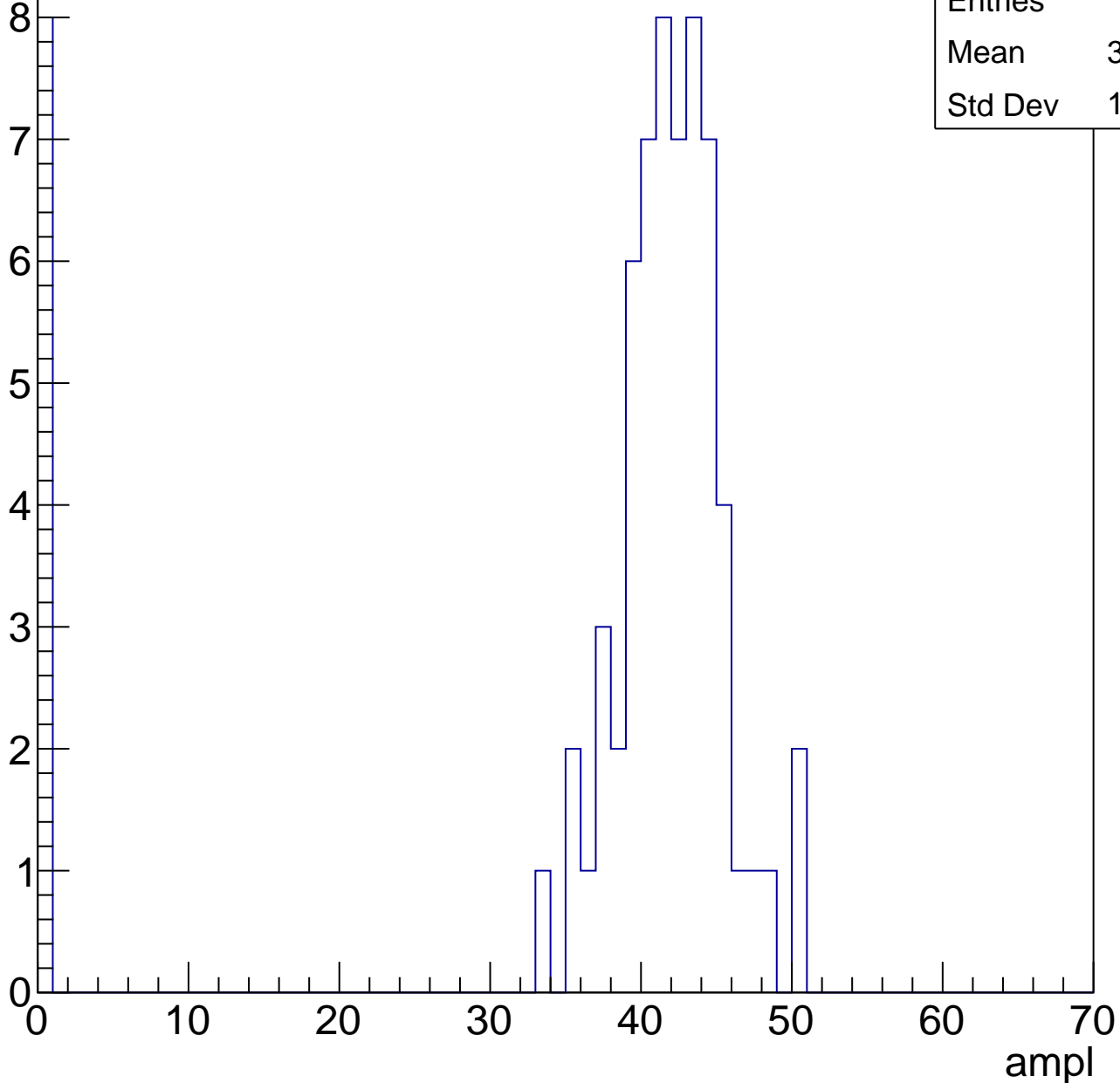


# B1L103S, U25-ch80, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	69
Mean	36.74
Std Dev	13.67

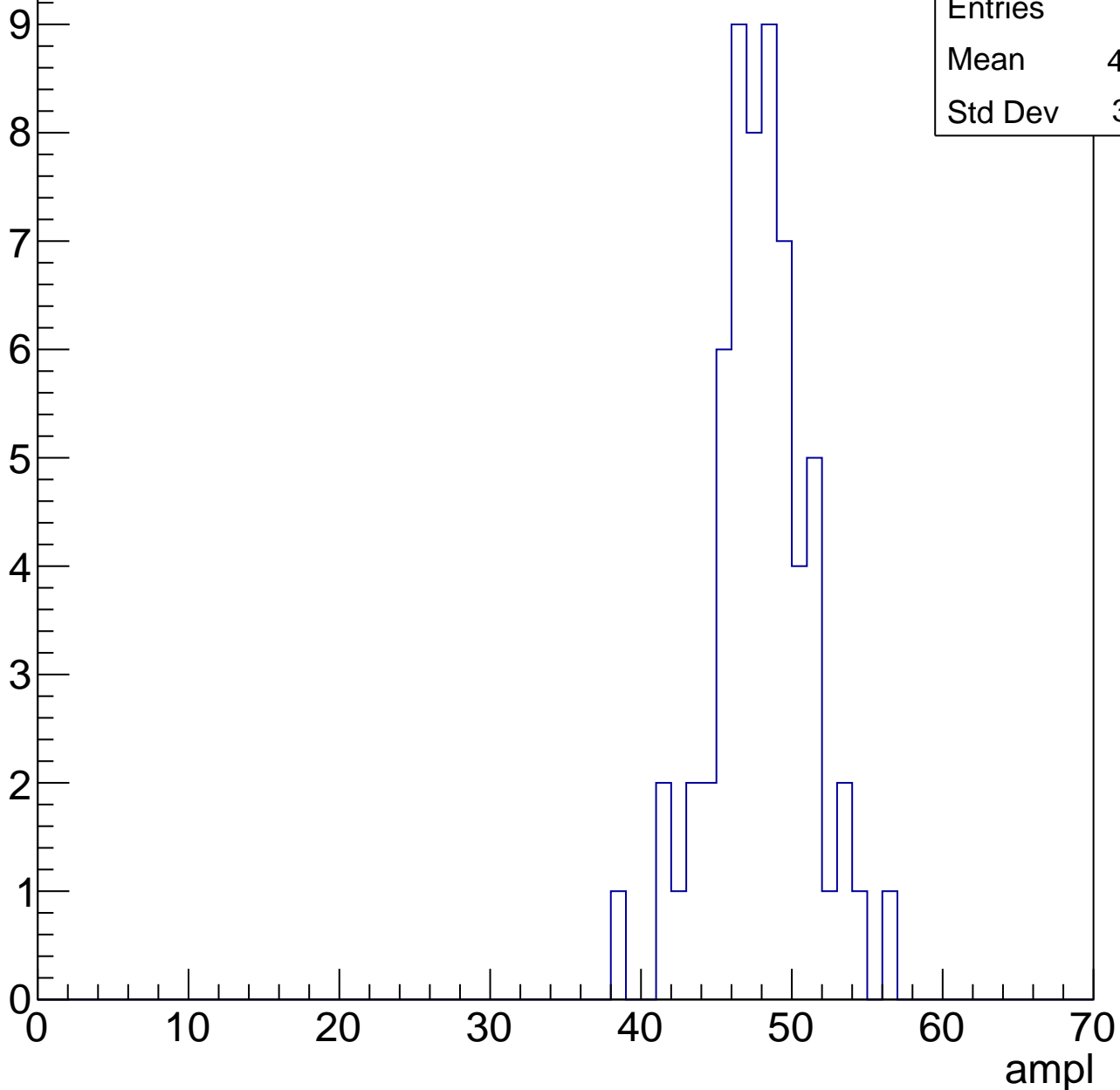


# B1L103S, U25-ch80, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	61
Mean	47.44
Std Dev	3.211

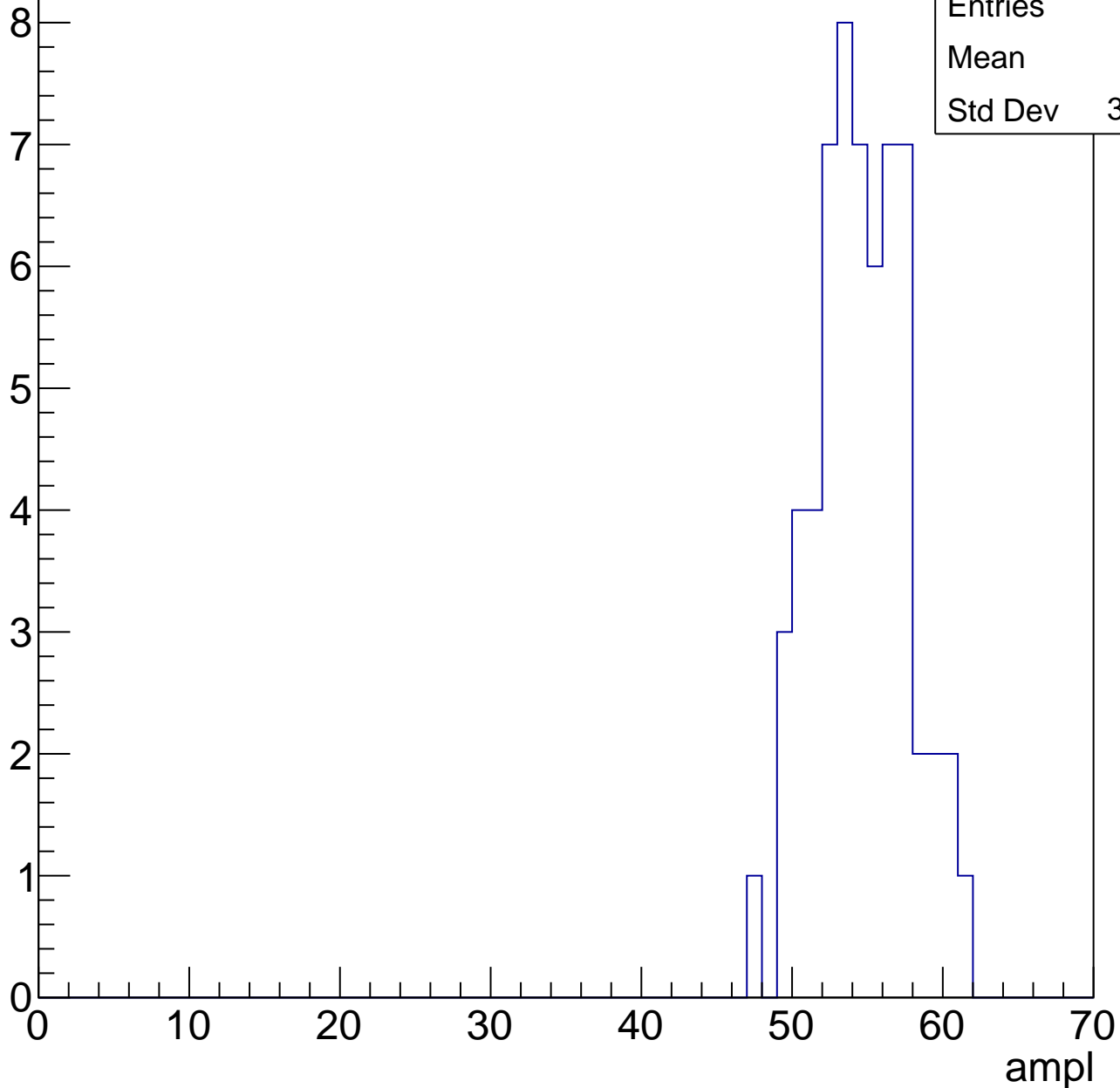


# B1L103S, U25-ch80, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	61
Mean	54.1
Std Dev	3.028

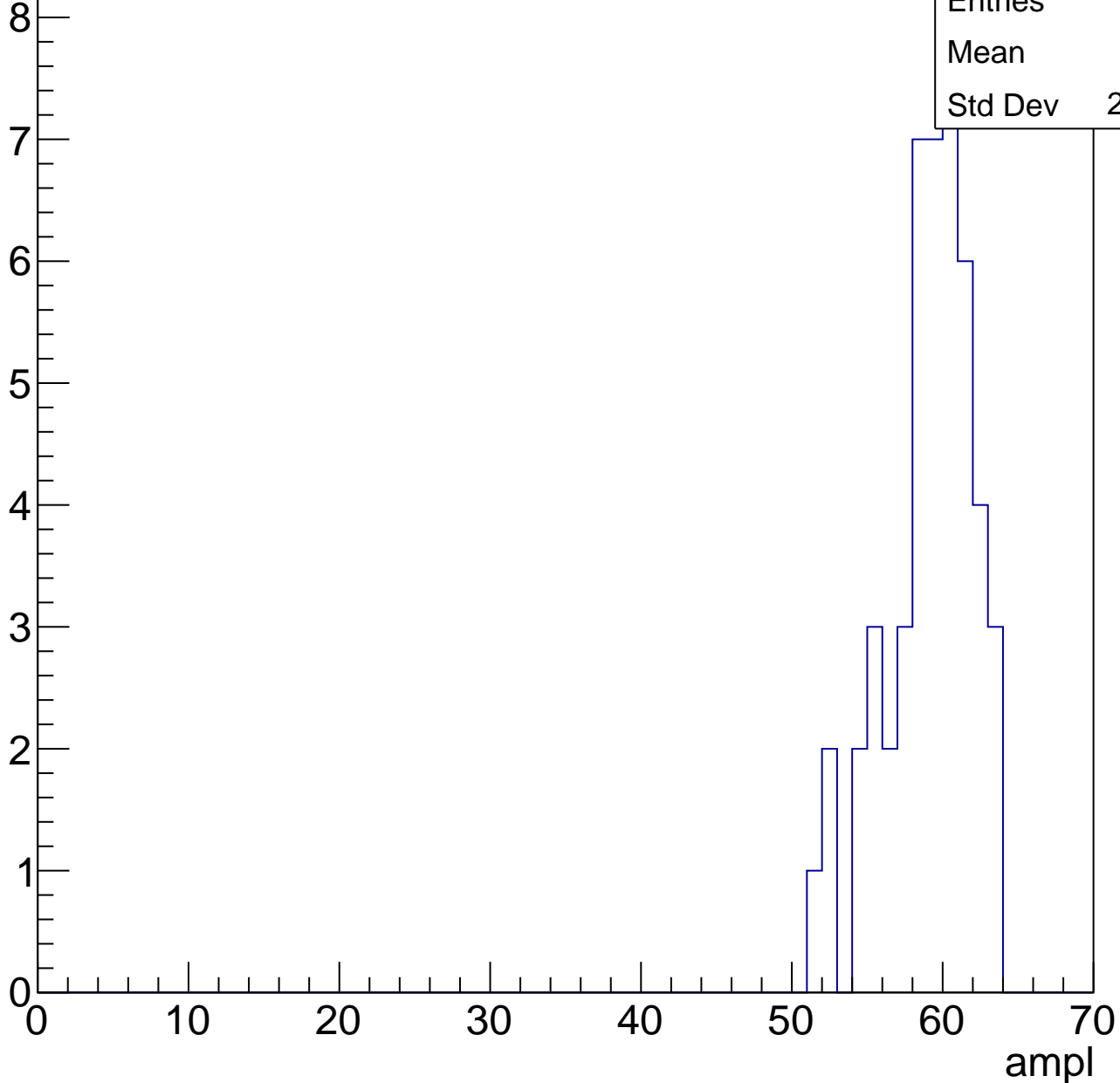


# B1L103S, U25-ch80, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	48
Mean	58.6
Std Dev	2.906

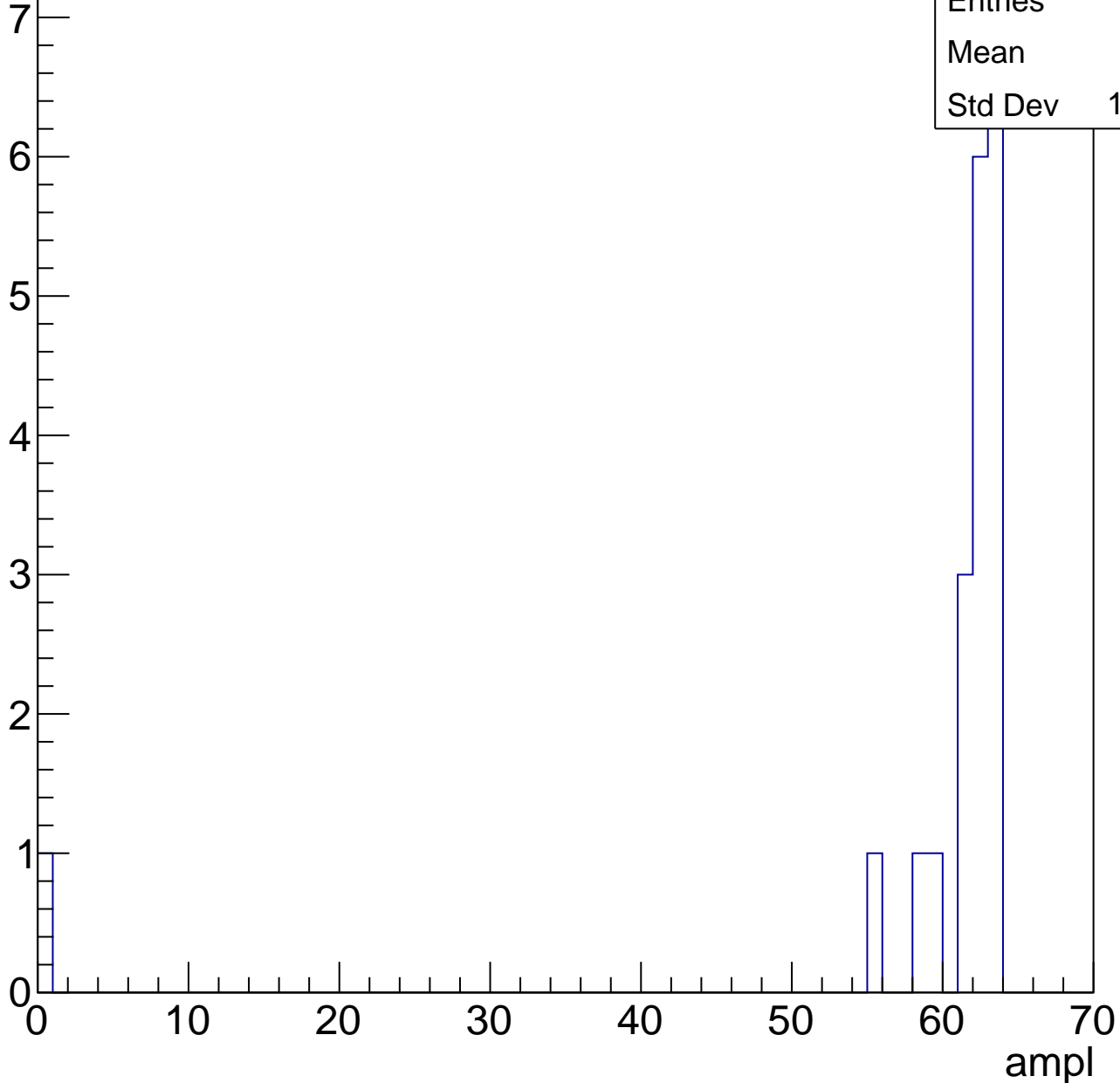


# B1L103S, U25-ch80, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	20
Mean	58.4
Std Dev	13.54



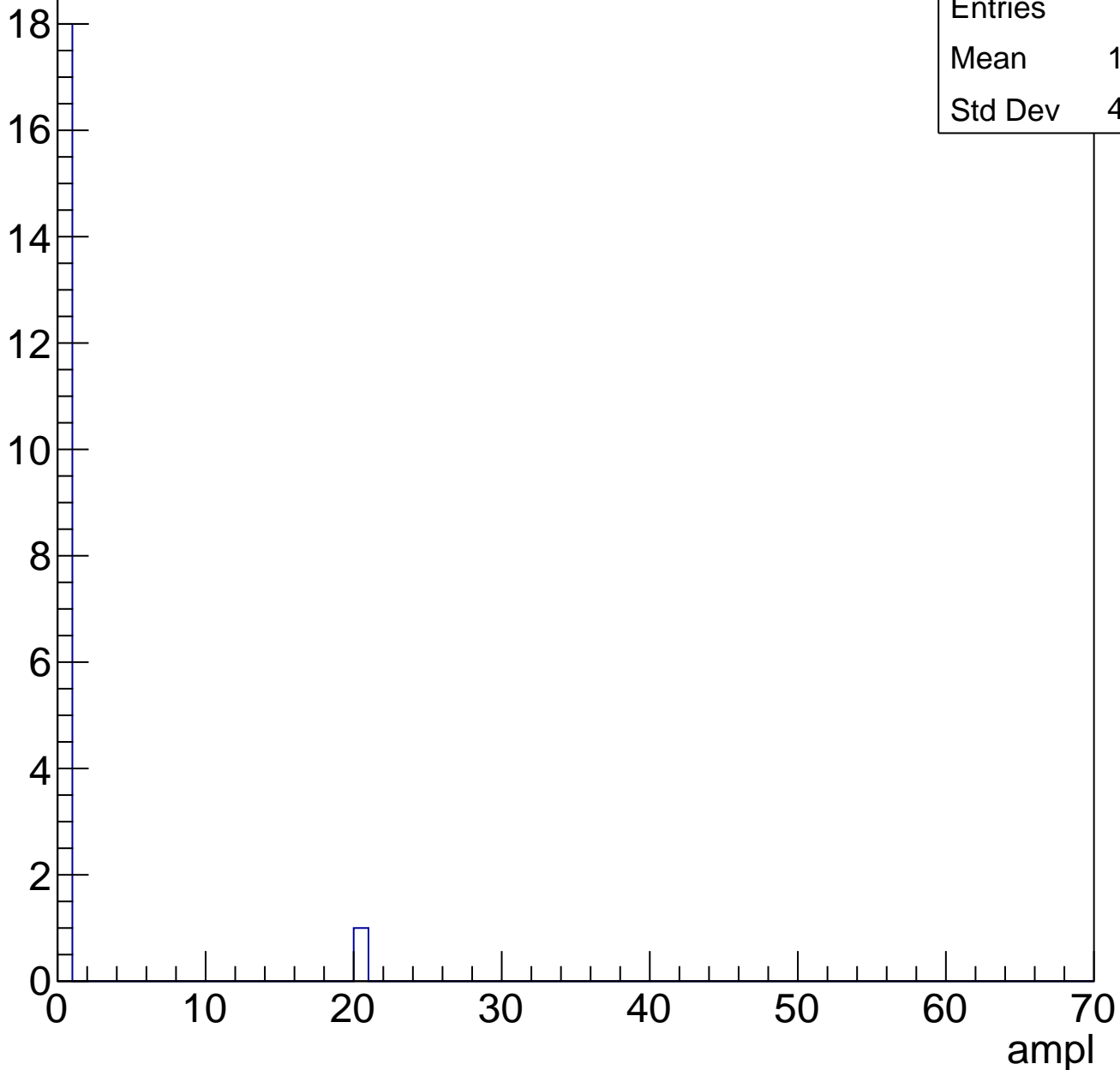


# B1L103S, U25-ch80, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	19
Mean	1.053
Std Dev	4.466

Entry

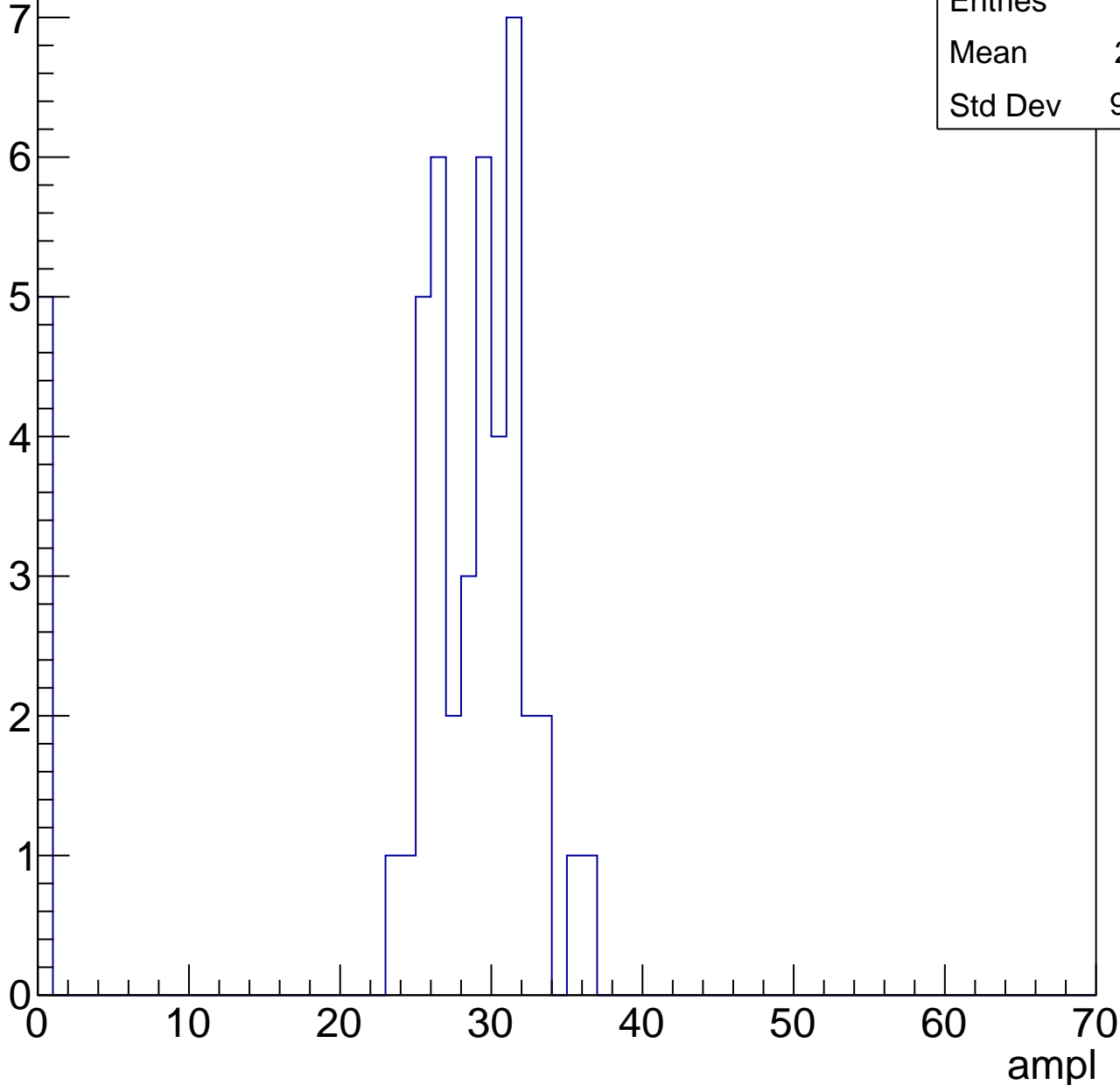


# B1L103S, U25-ch81, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	46
Mean	25.61
Std Dev	9.382

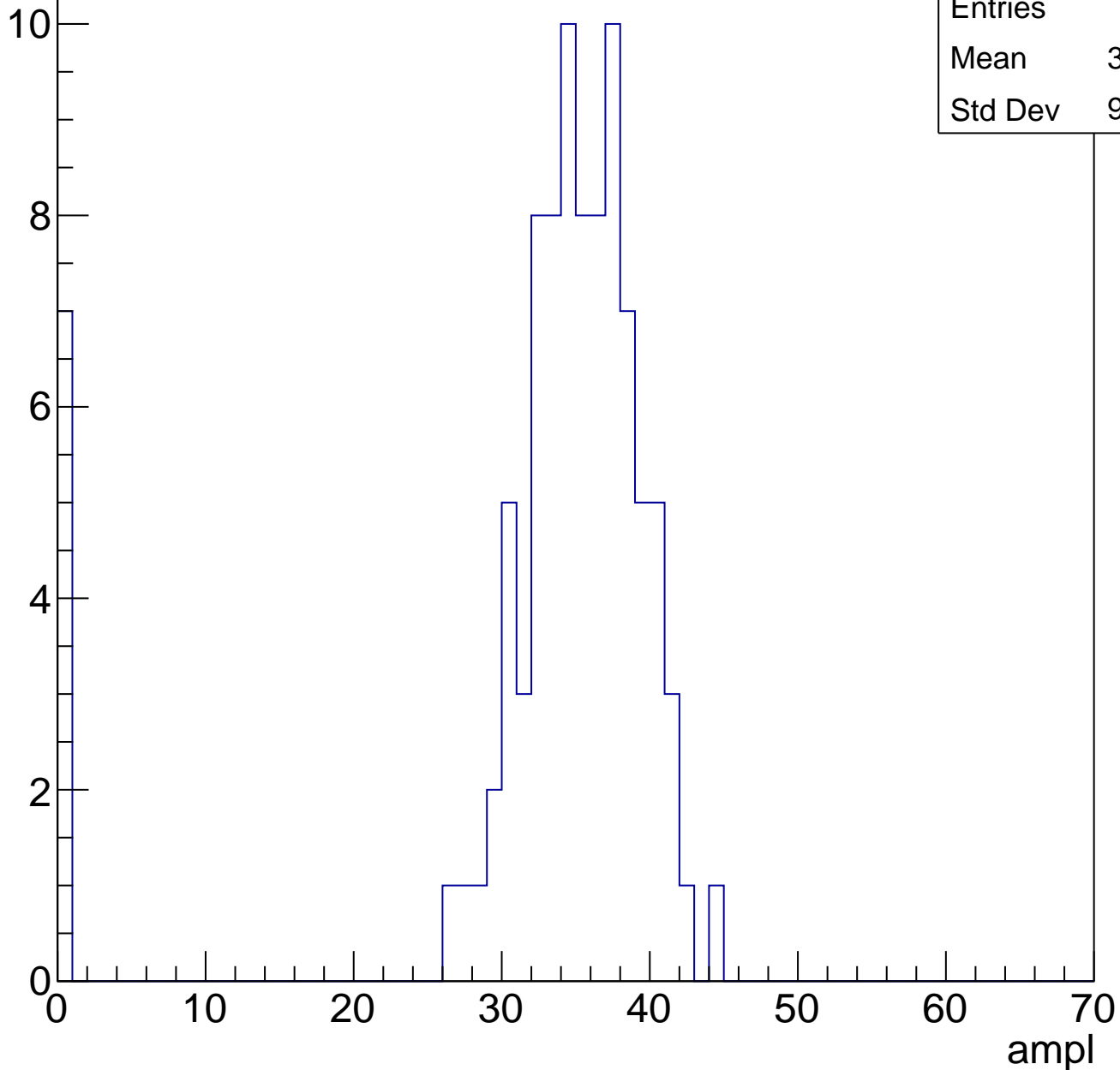


# B1L103S, U25-ch81, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	94
Mean	32.45
Std Dev	9.822

Entry

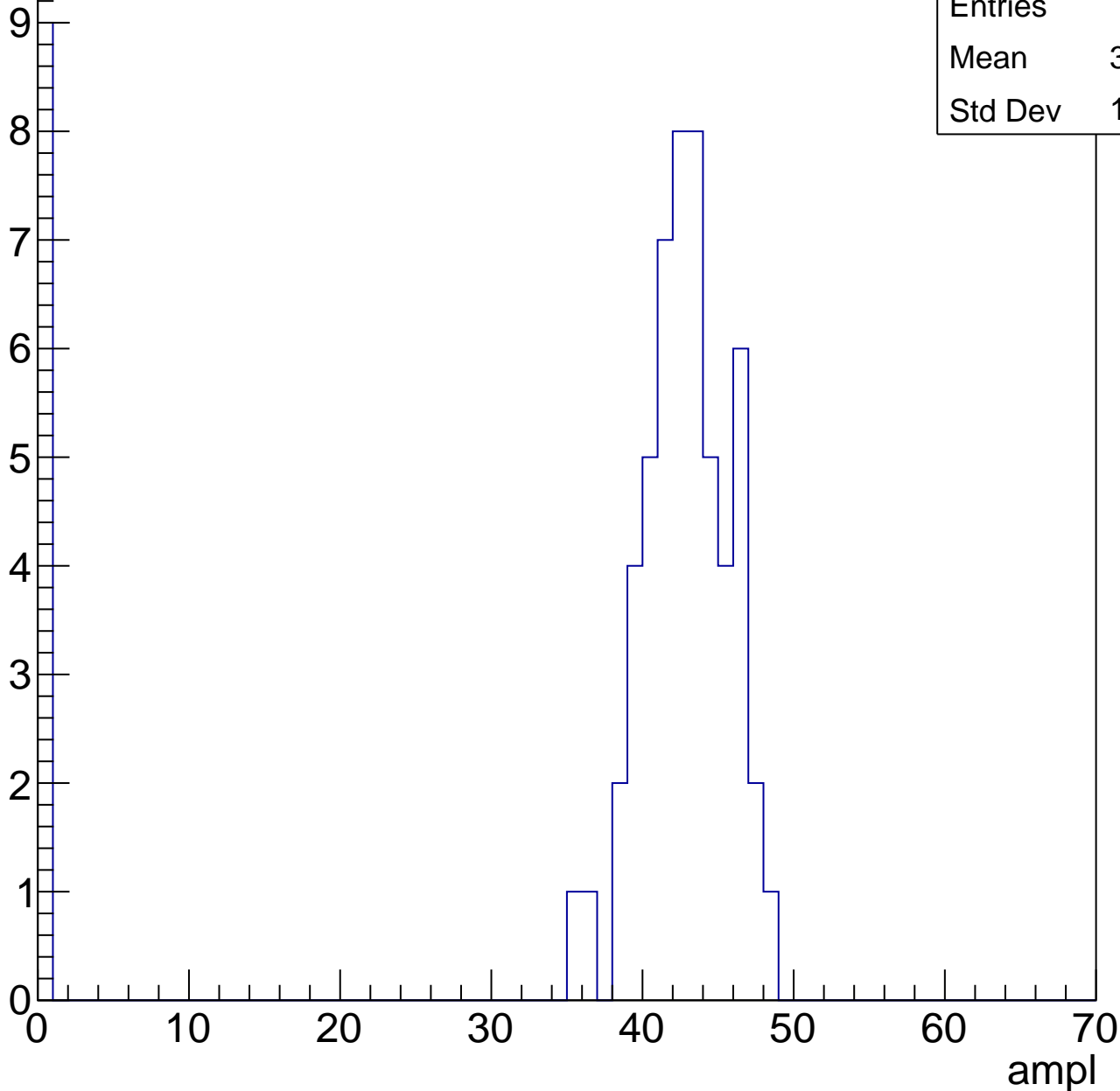


# B1L103S, U25-ch81, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	63
Mean	36.32
Std Dev	15.05

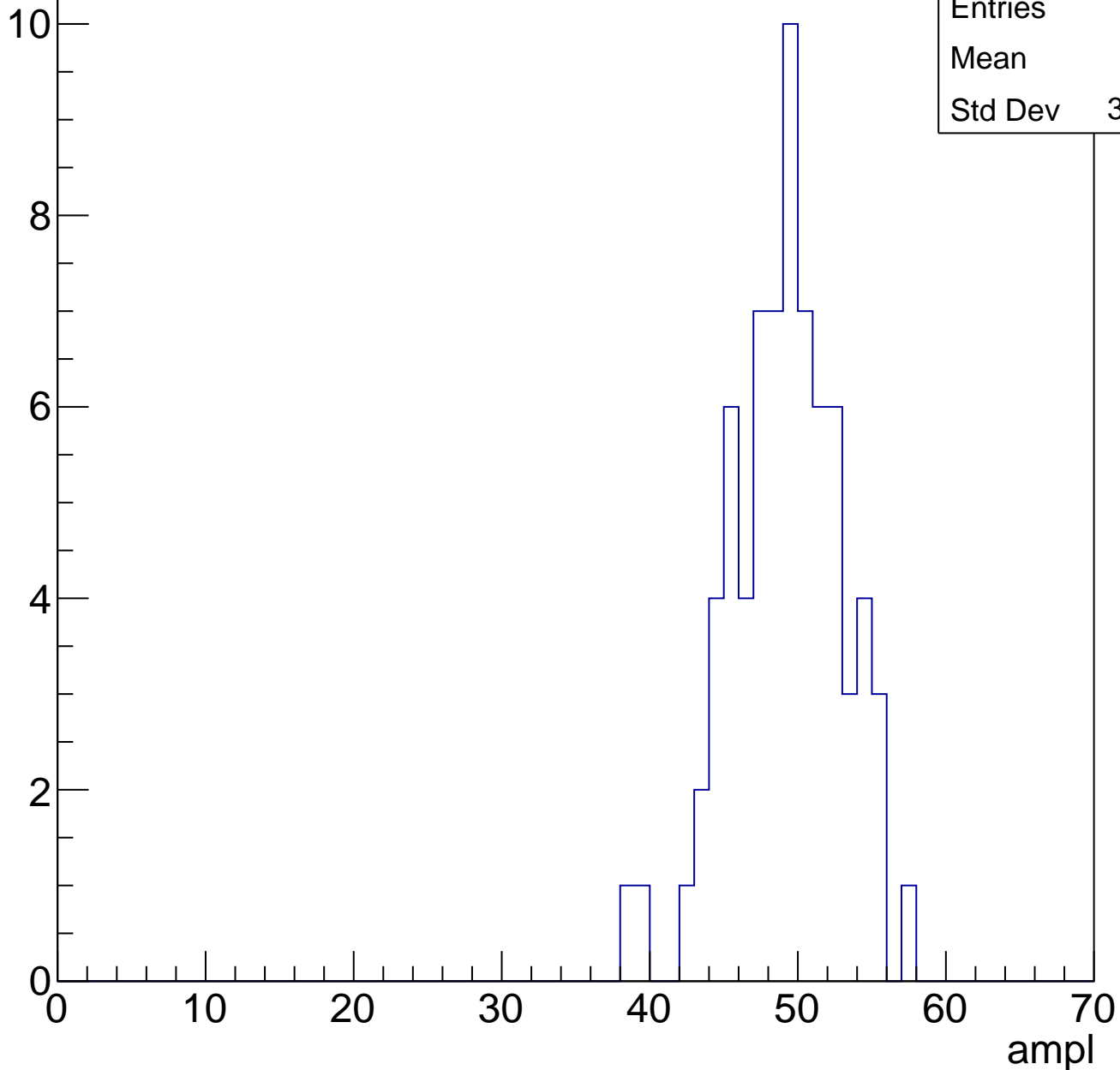


# B1L103S, U25-ch81, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	73
Mean	48.7
Std Dev	3.715

Entry

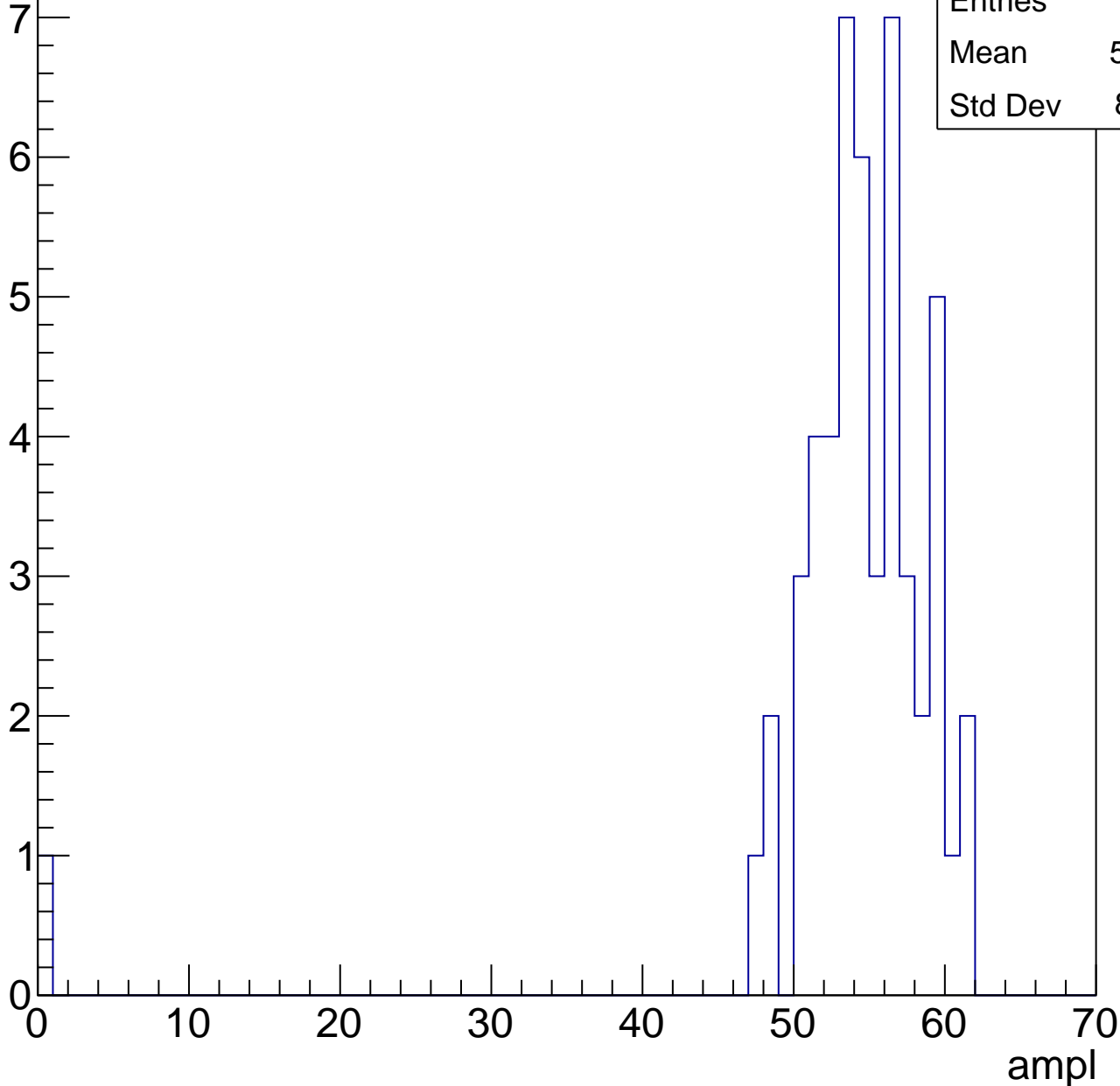


# B1L103S, U25-ch81, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

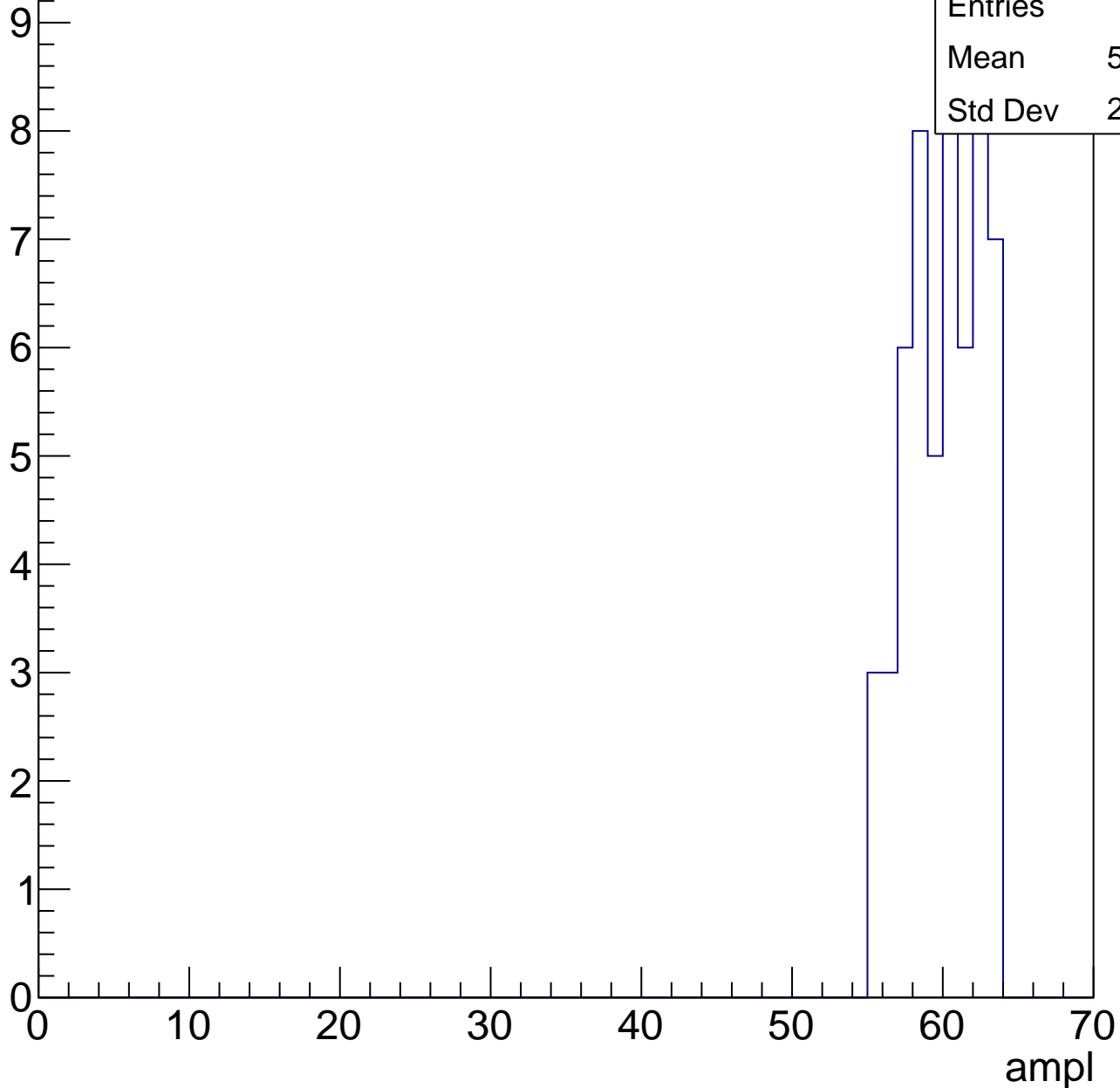
Entries	51
Mean	53.35
Std Dev	8.251



# B1L103S, U25-ch81, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

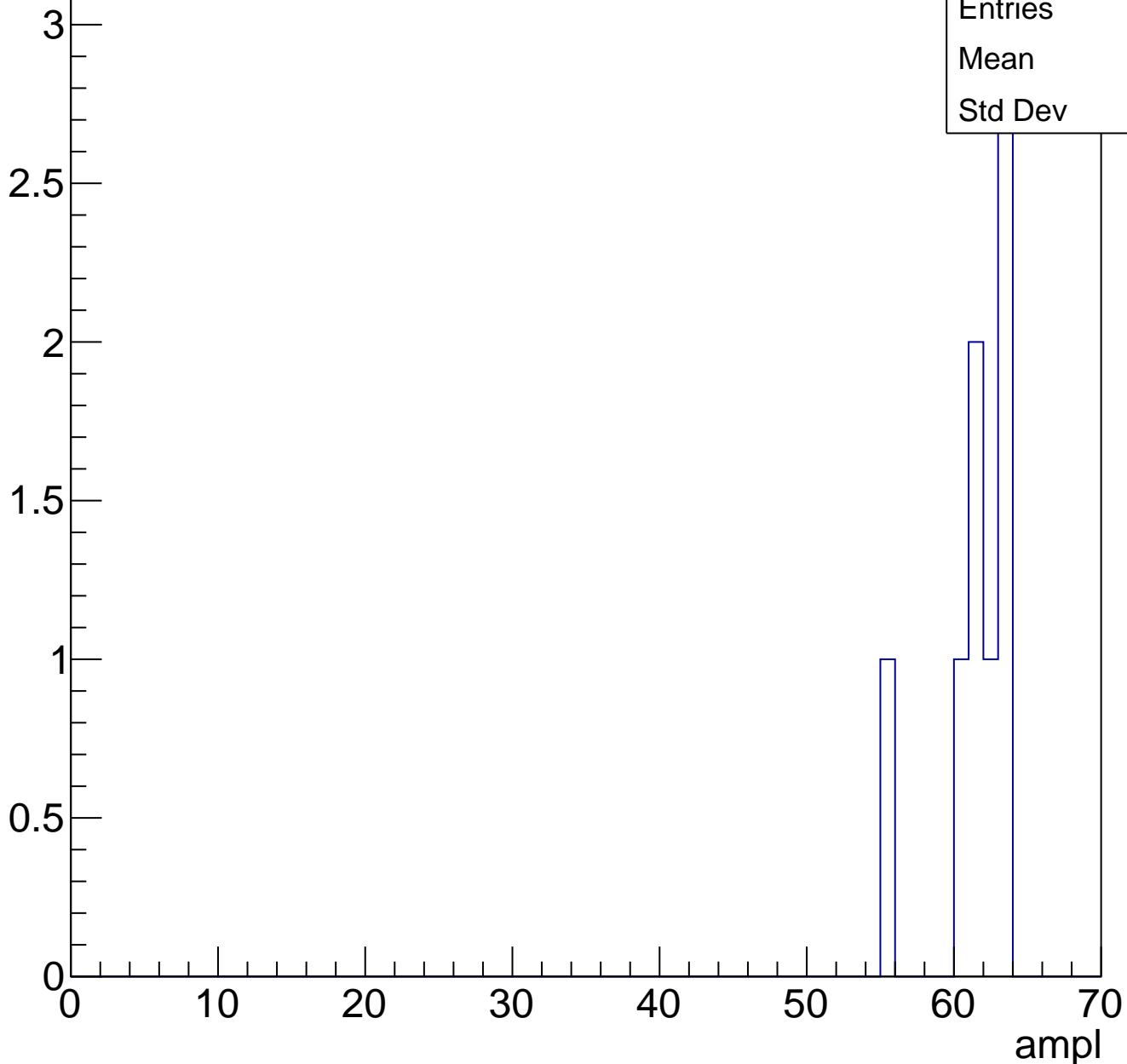


Entries	55
Mean	59.62
Std Dev	2.378

# B1L103S, U25-ch81, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



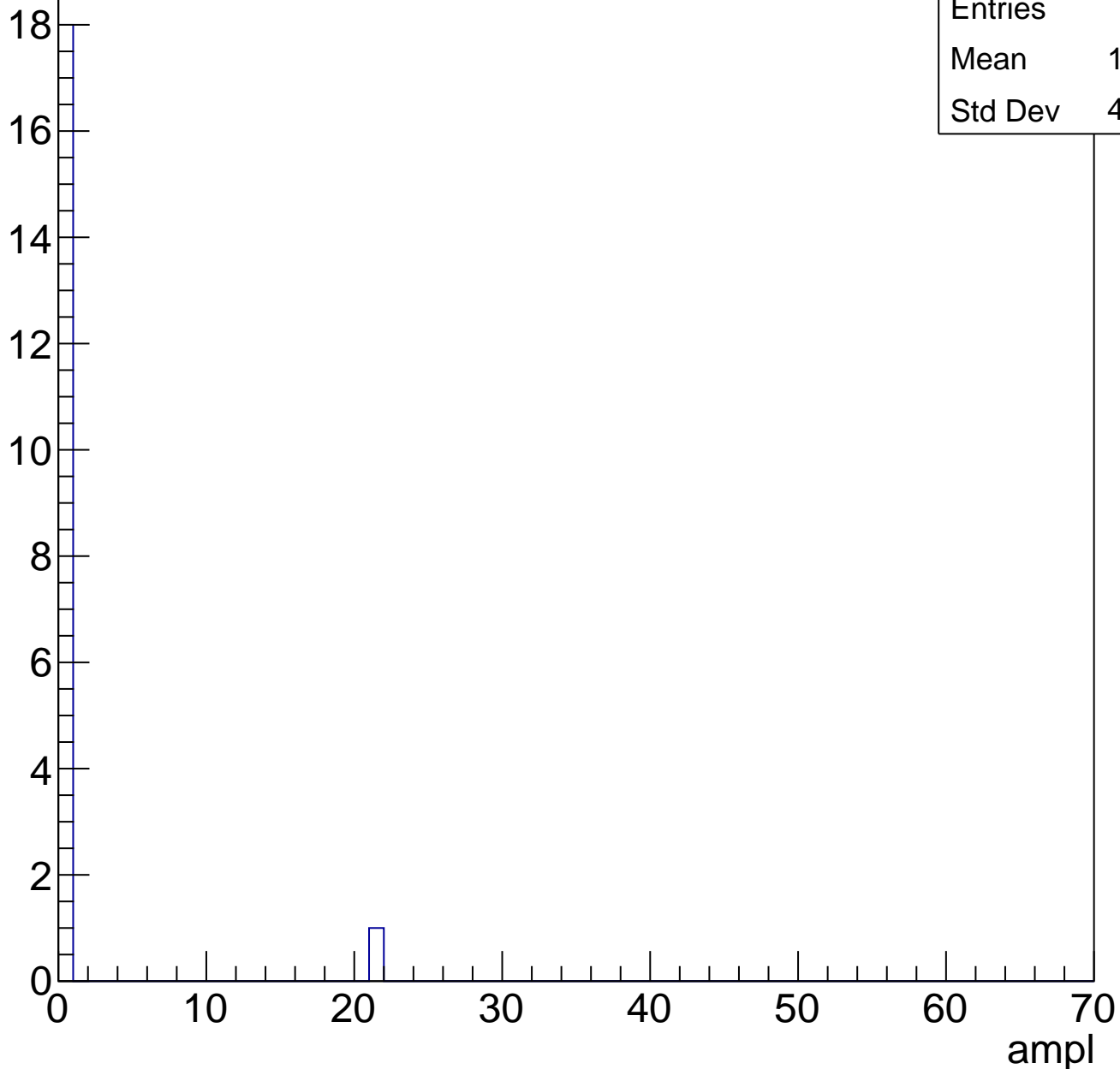


# B1L103S, U25-ch81, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	19
Mean	1.105
Std Dev	4.689

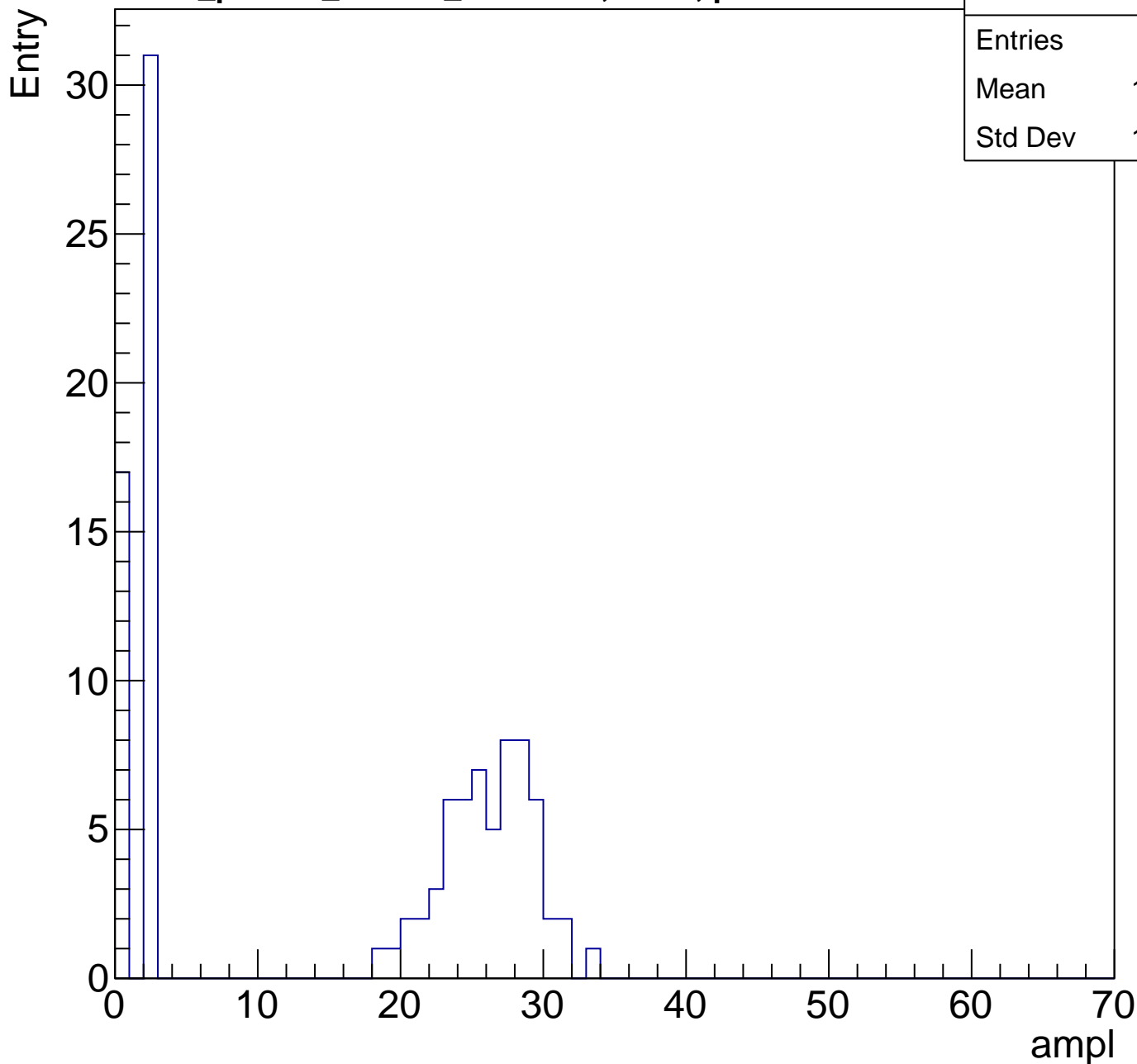
Entry



# B1L103S, U25-ch82, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

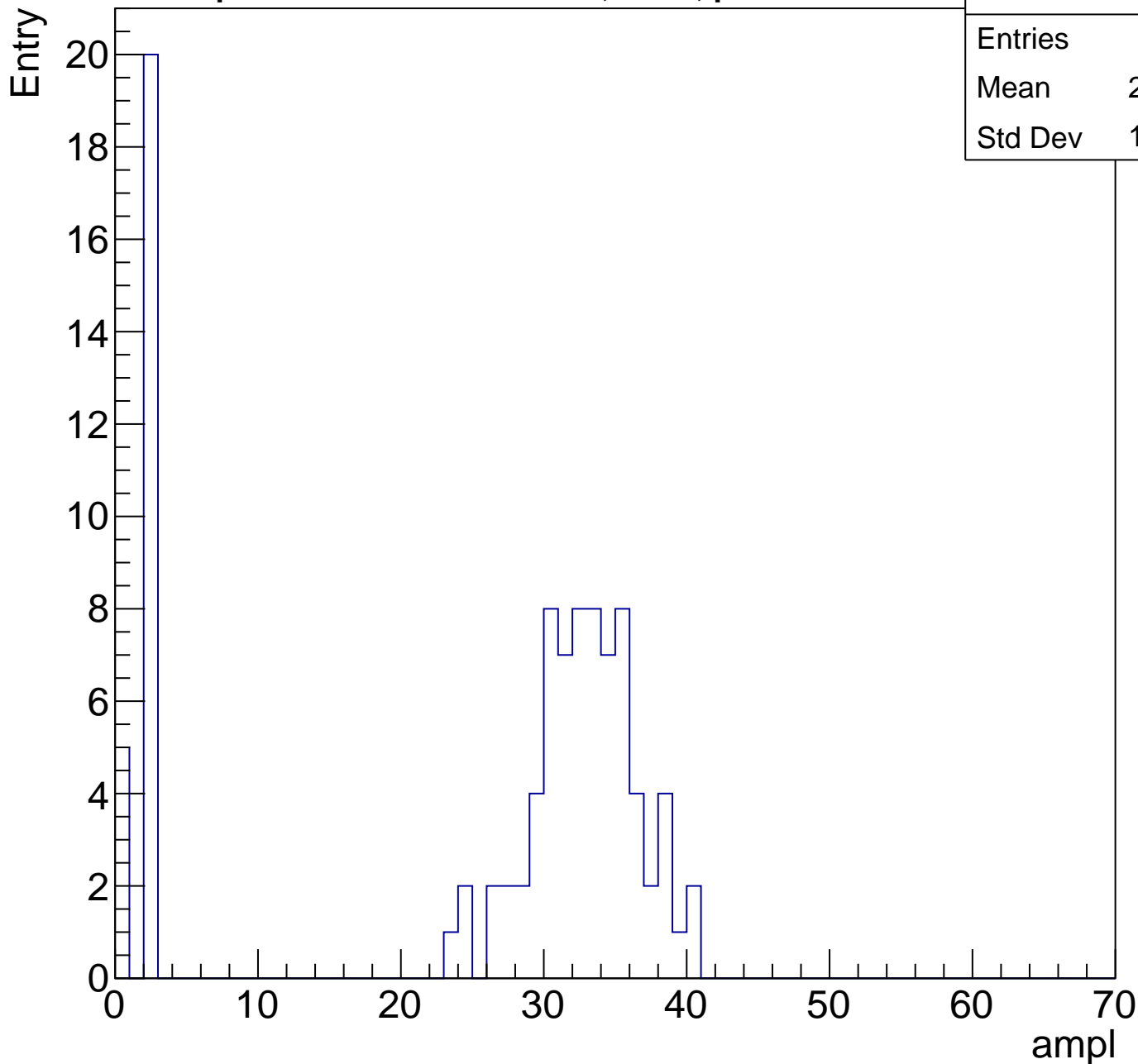
Entries	108
Mean	14.84
Std Dev	12.36



# B1L103S, U25-ch82, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	97
Mean	24.46
Std Dev	13.84

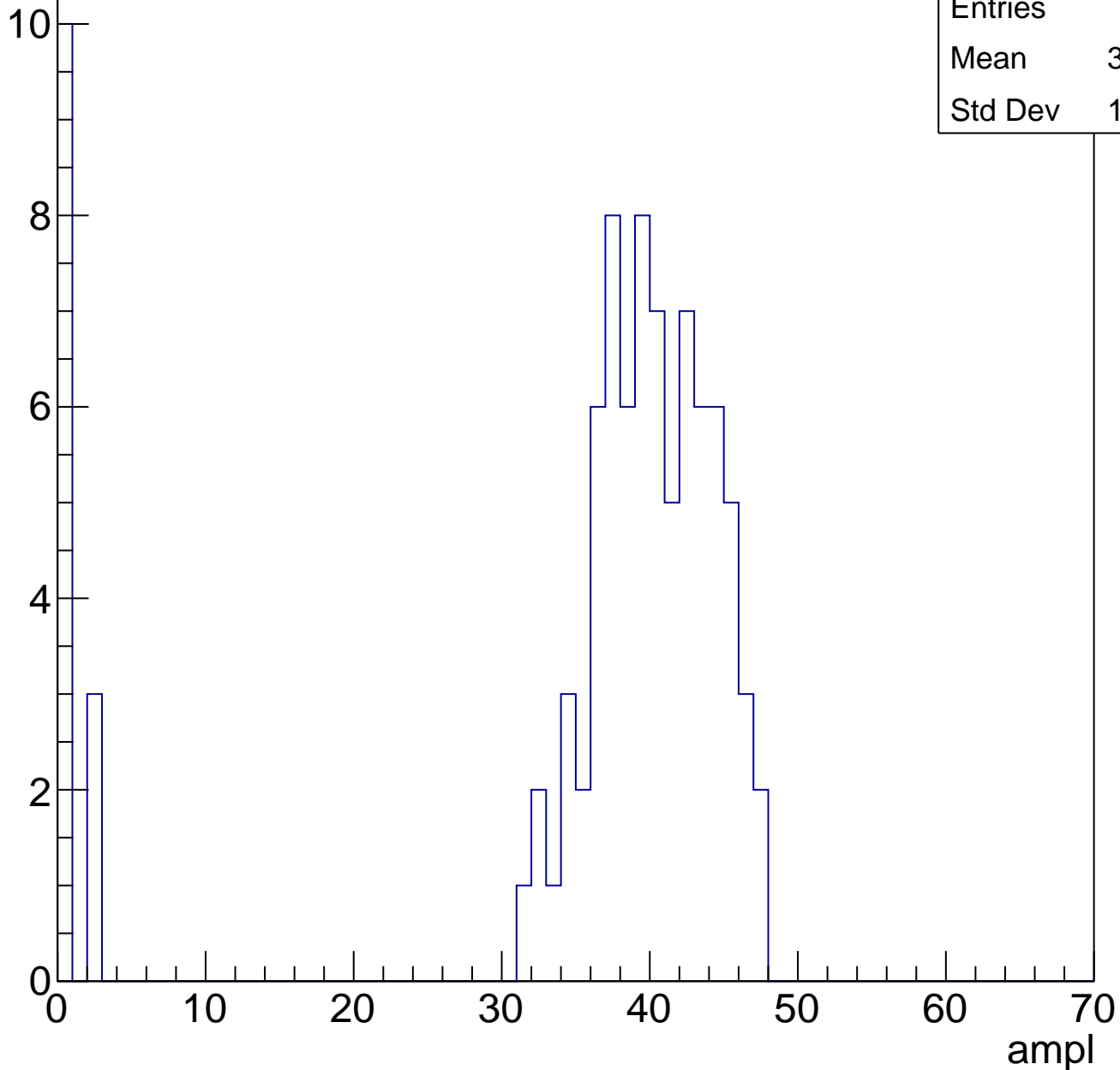


# B1L103S, U25-ch82, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	91
Mean	34.24
Std Dev	14.24

Entry

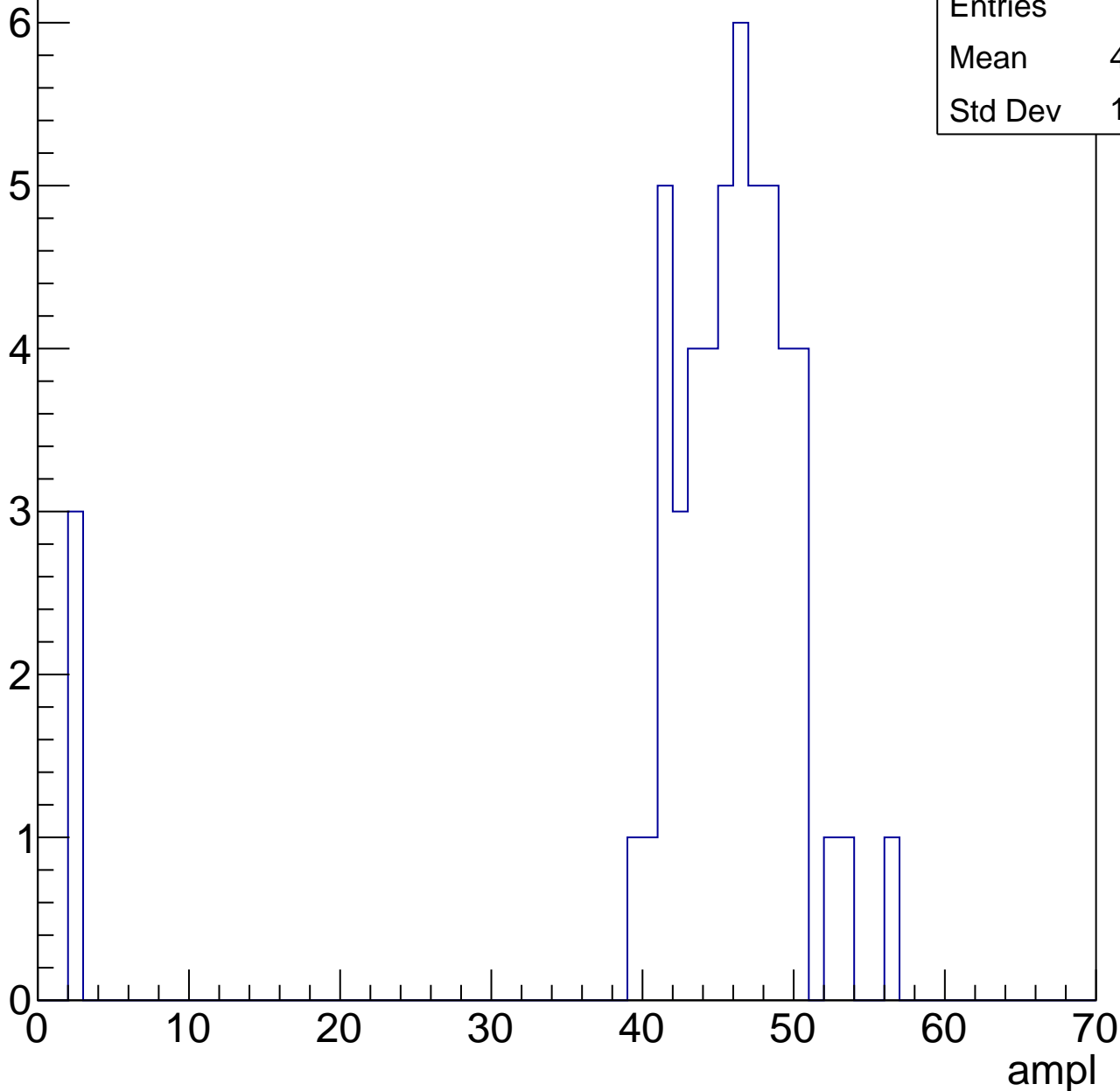


# B1L103S, U25-ch82, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	53
Mean	43.34
Std Dev	10.69

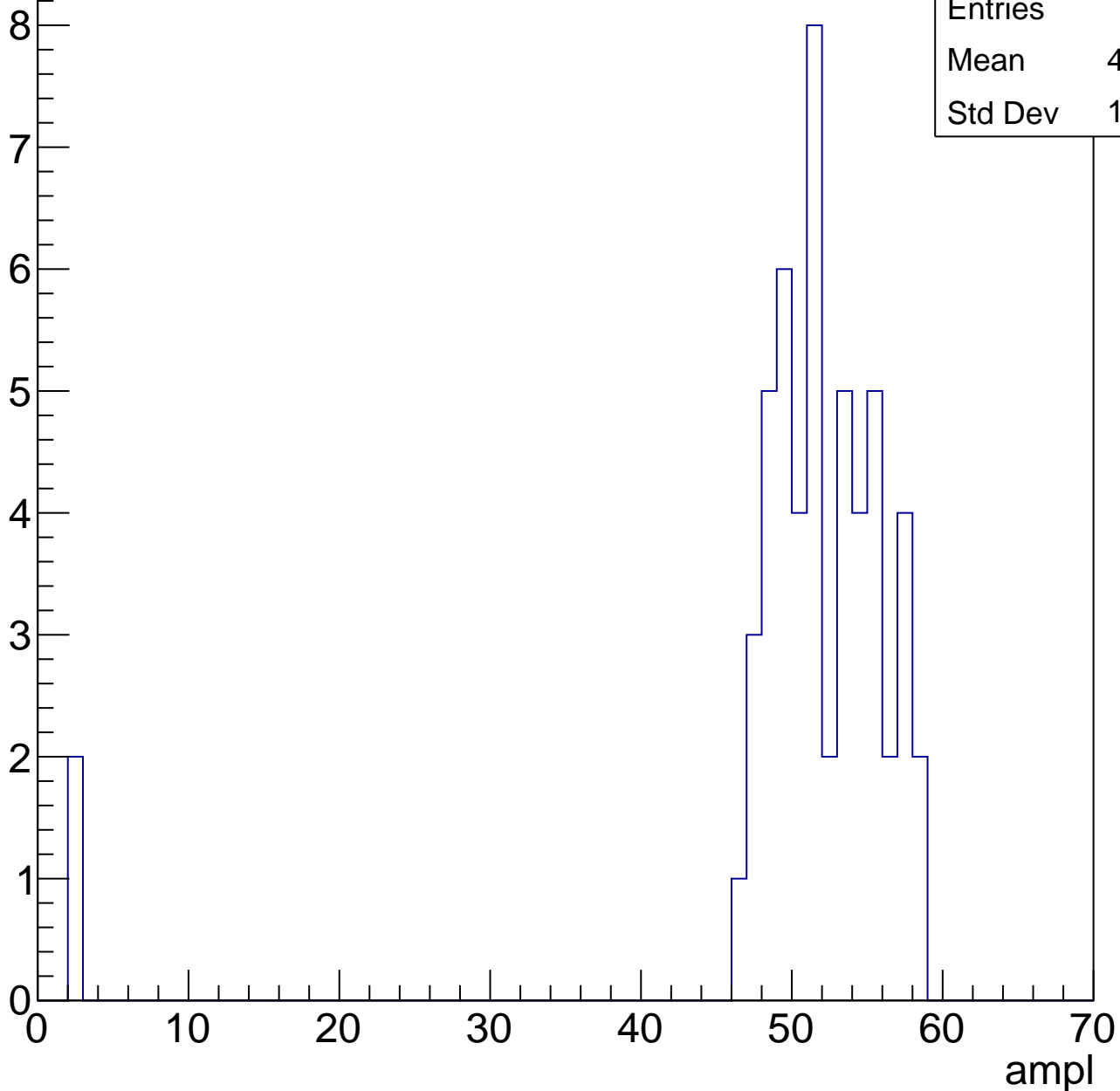


# B1L103S, U25-ch82, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	53
Mean	49.98
Std Dev	10.02

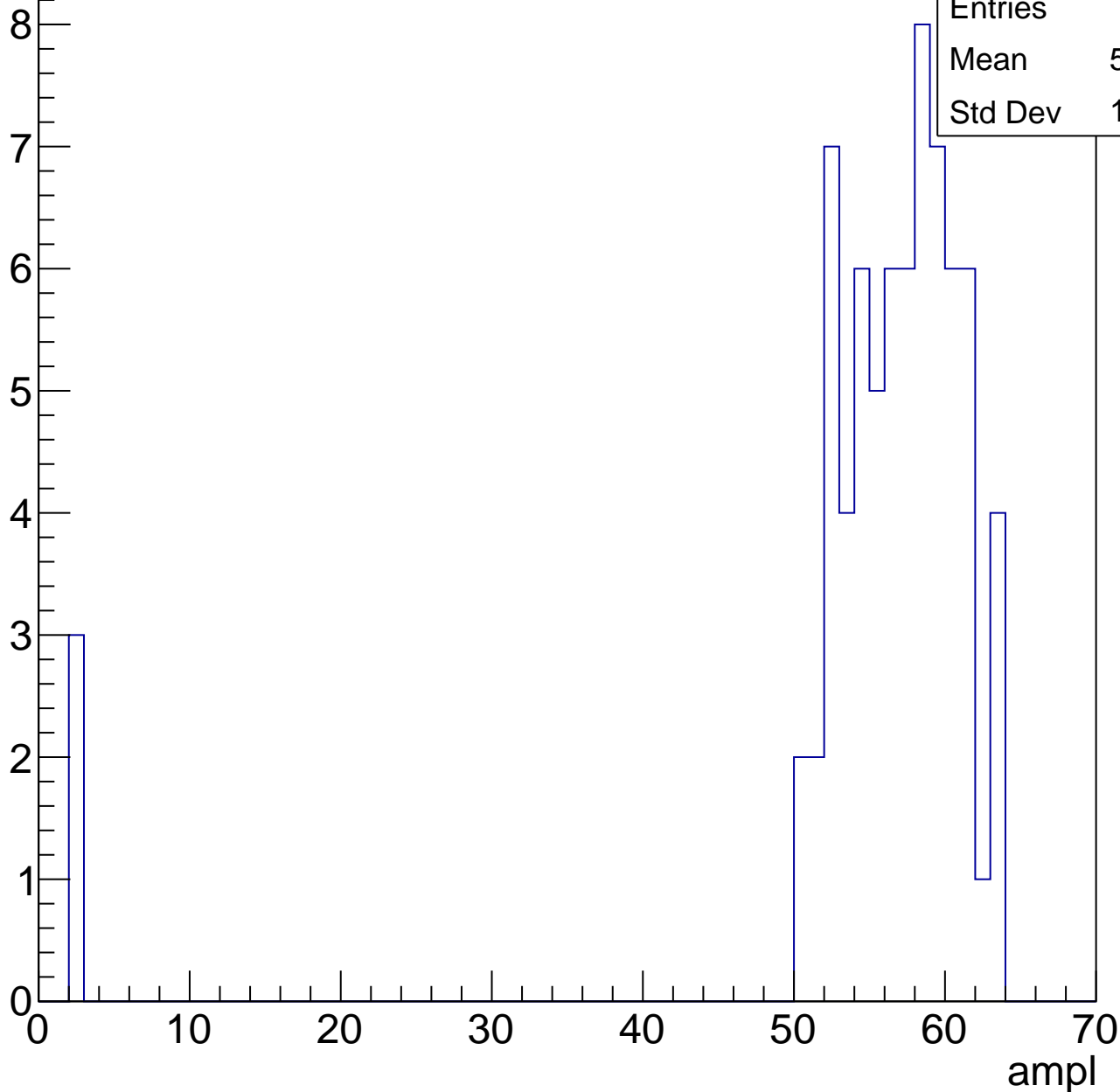


# B1L103S, U25-ch82, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	73
Mean	54.49
Std Dev	11.38

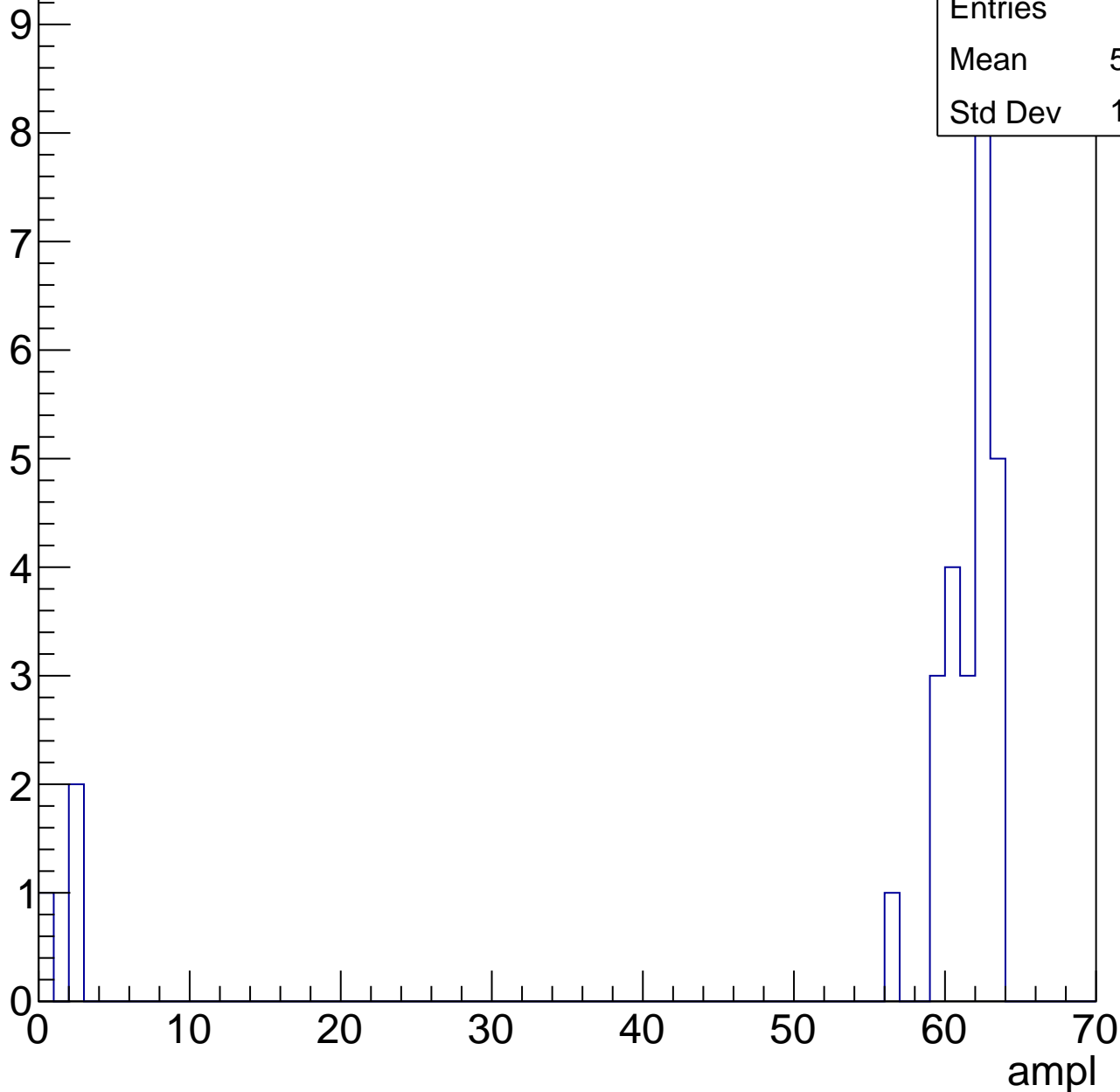


# B1L103S, U25-ch82, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	28
Mean	54.75
Std Dev	18.57



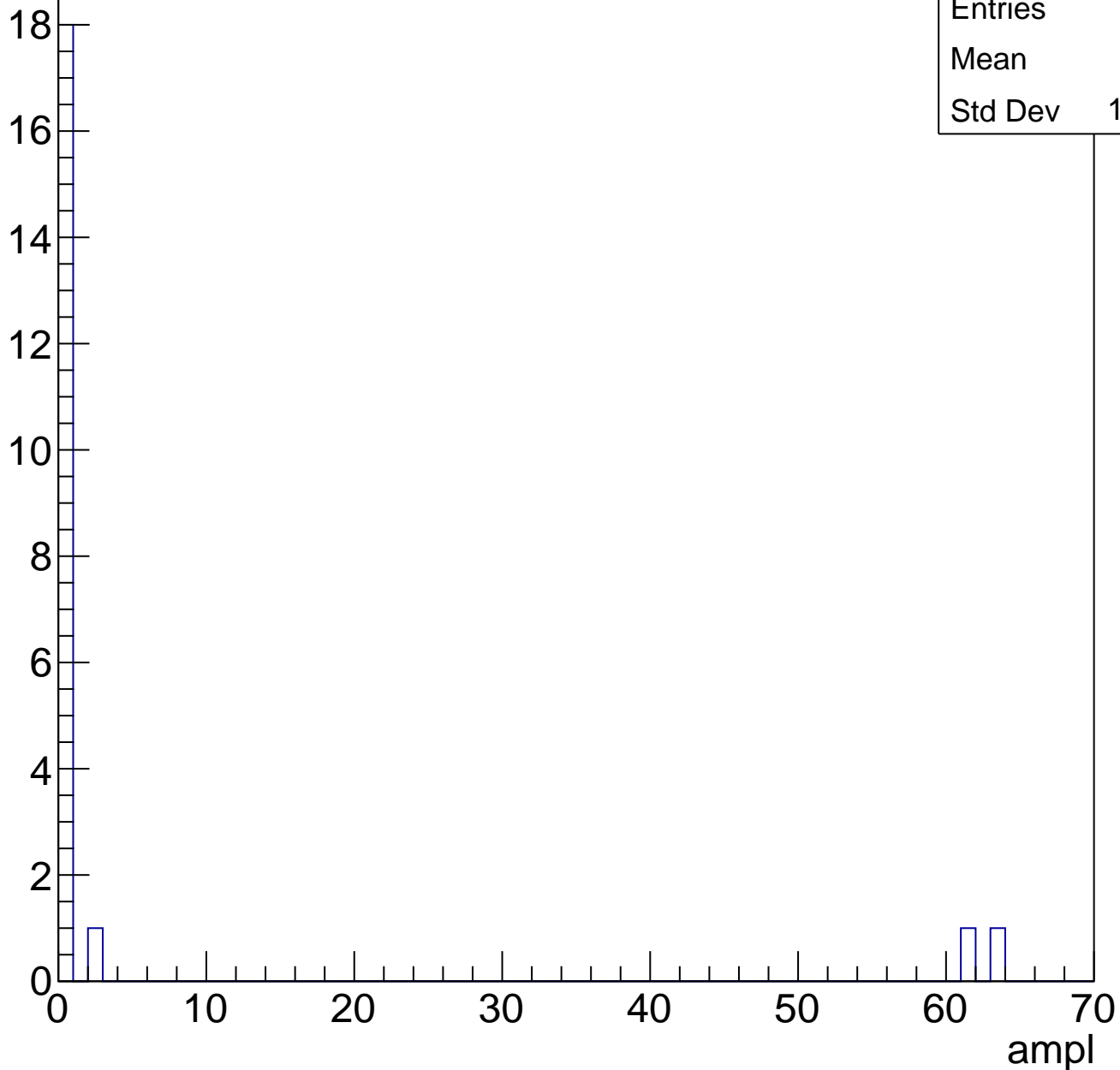


# B1L103S, U25-ch82, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	21
Mean	6
Std Dev	18.18

Entry

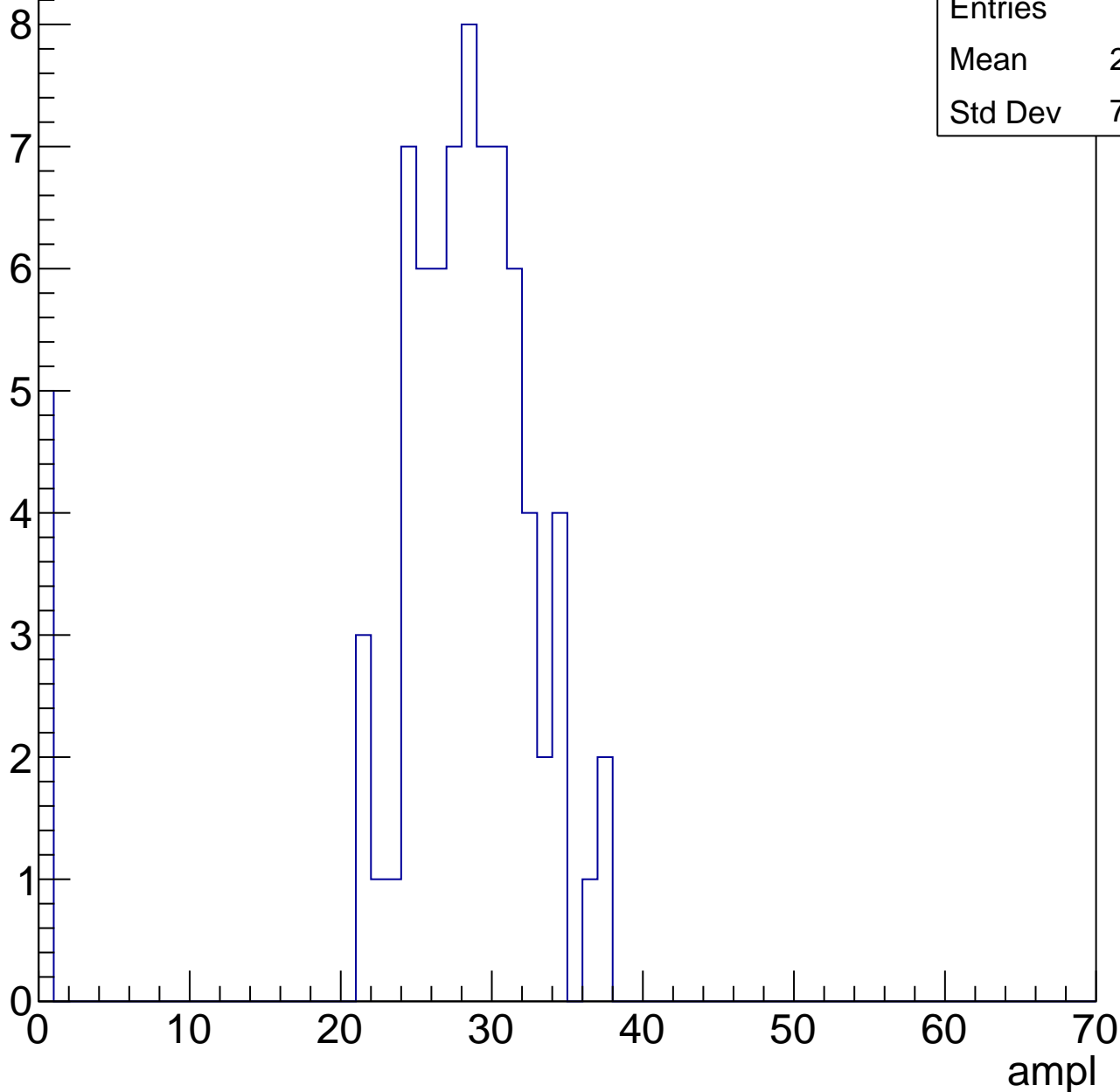


# B1L103S, U25-ch83, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	77
Mean	26.42
Std Dev	7.817

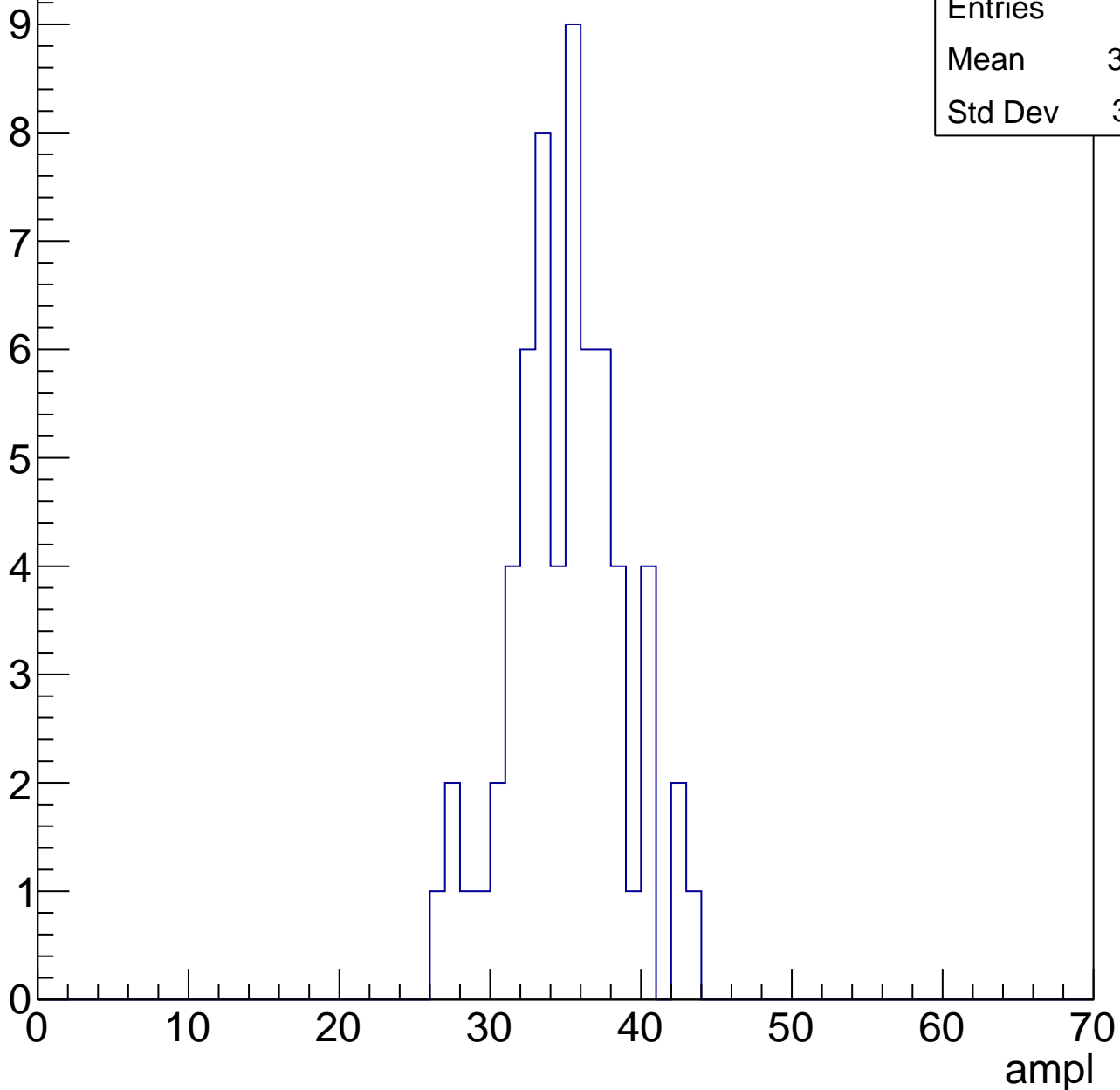


# B1L103S, U25-ch83, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	62
Mean	34.58
Std Dev	3.661

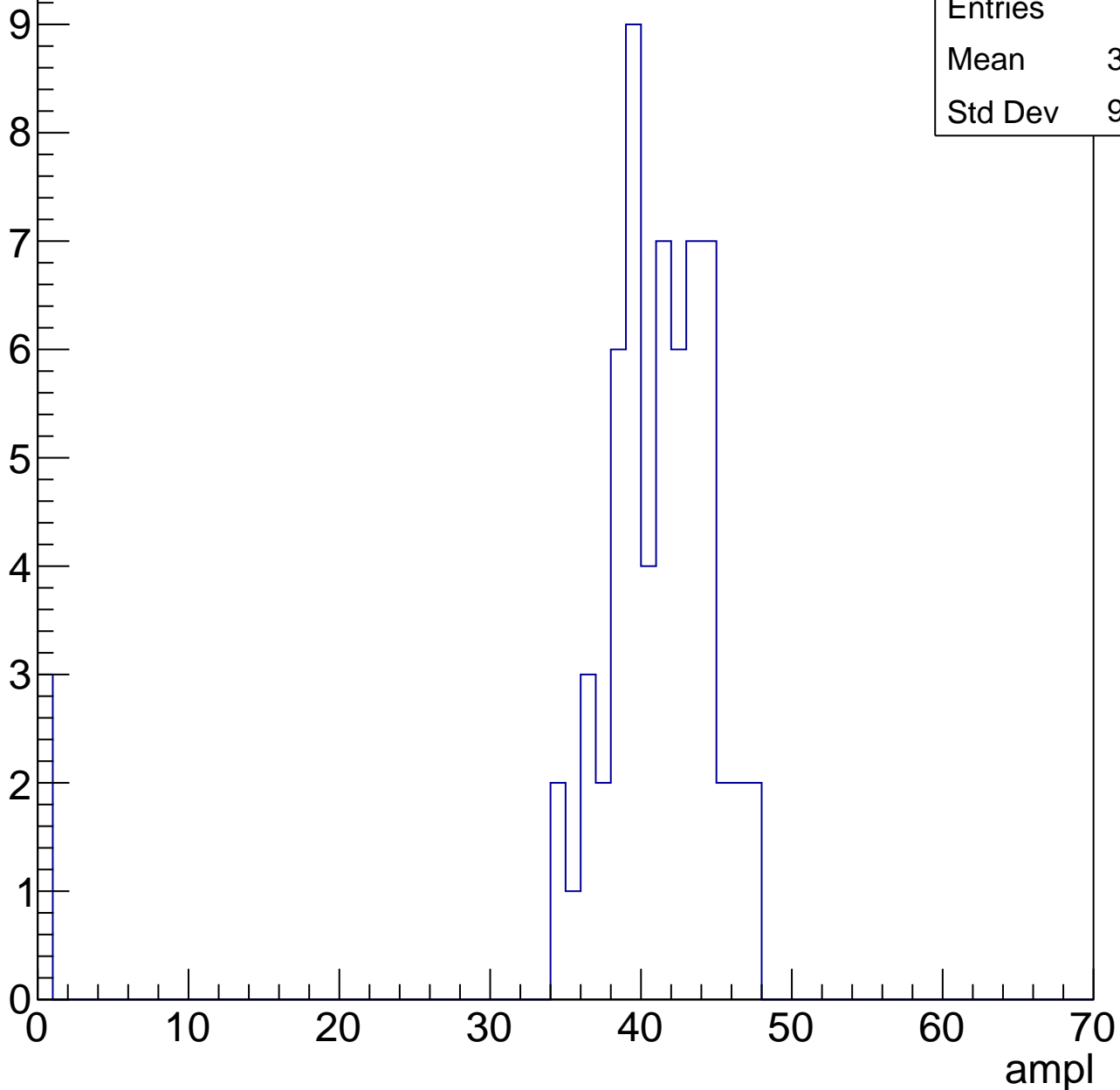


# B1L103S, U25-ch83, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	63
Mean	38.86
Std Dev	9.206



# B1L103S, U25-ch83, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	92
Mean	45.4
Std Dev	12.57

Entry

10

8

6

4

2

0

ampl

0

10

20

30

40

50

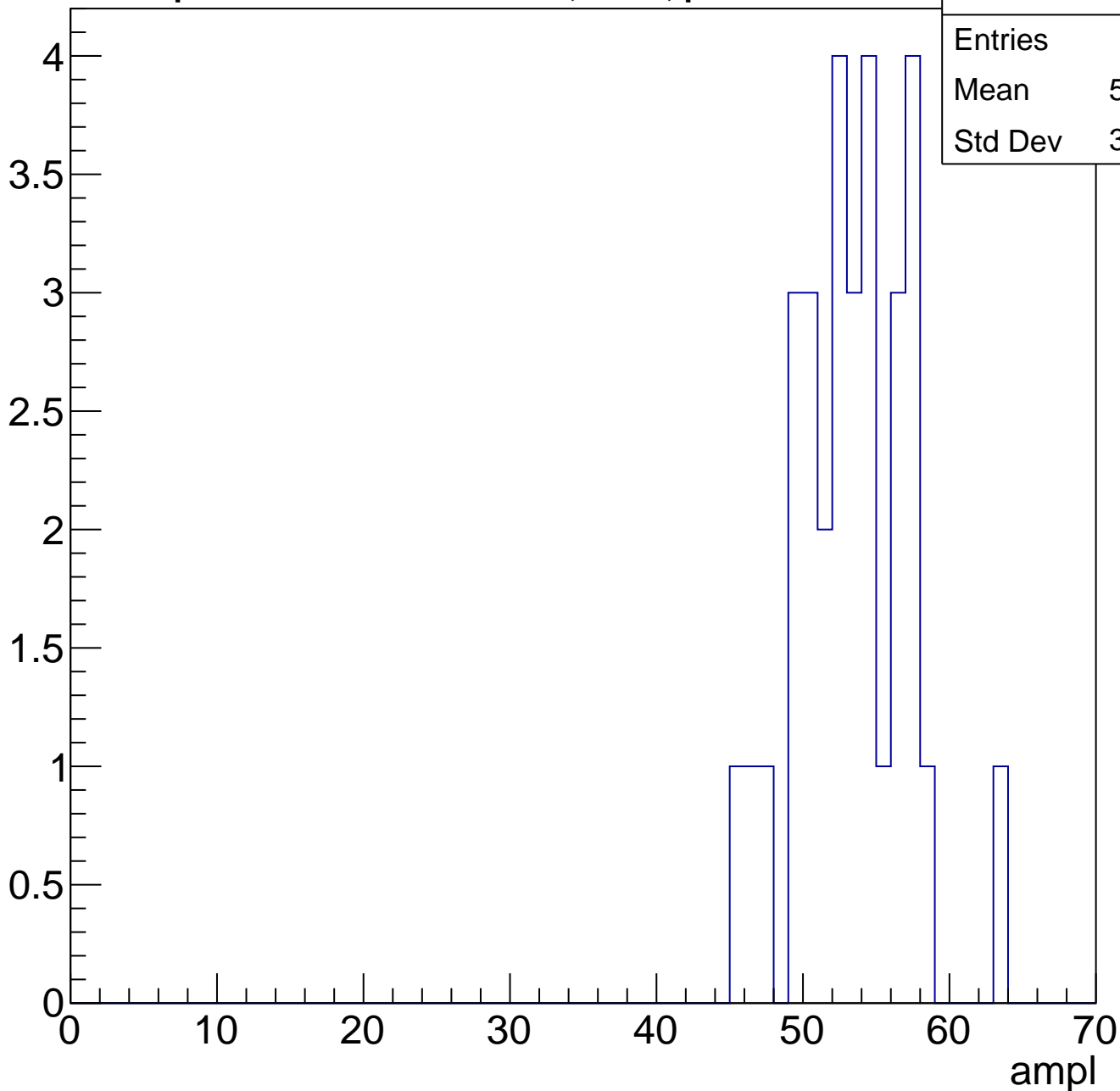
60

70

# B1L103S, U25-ch83, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



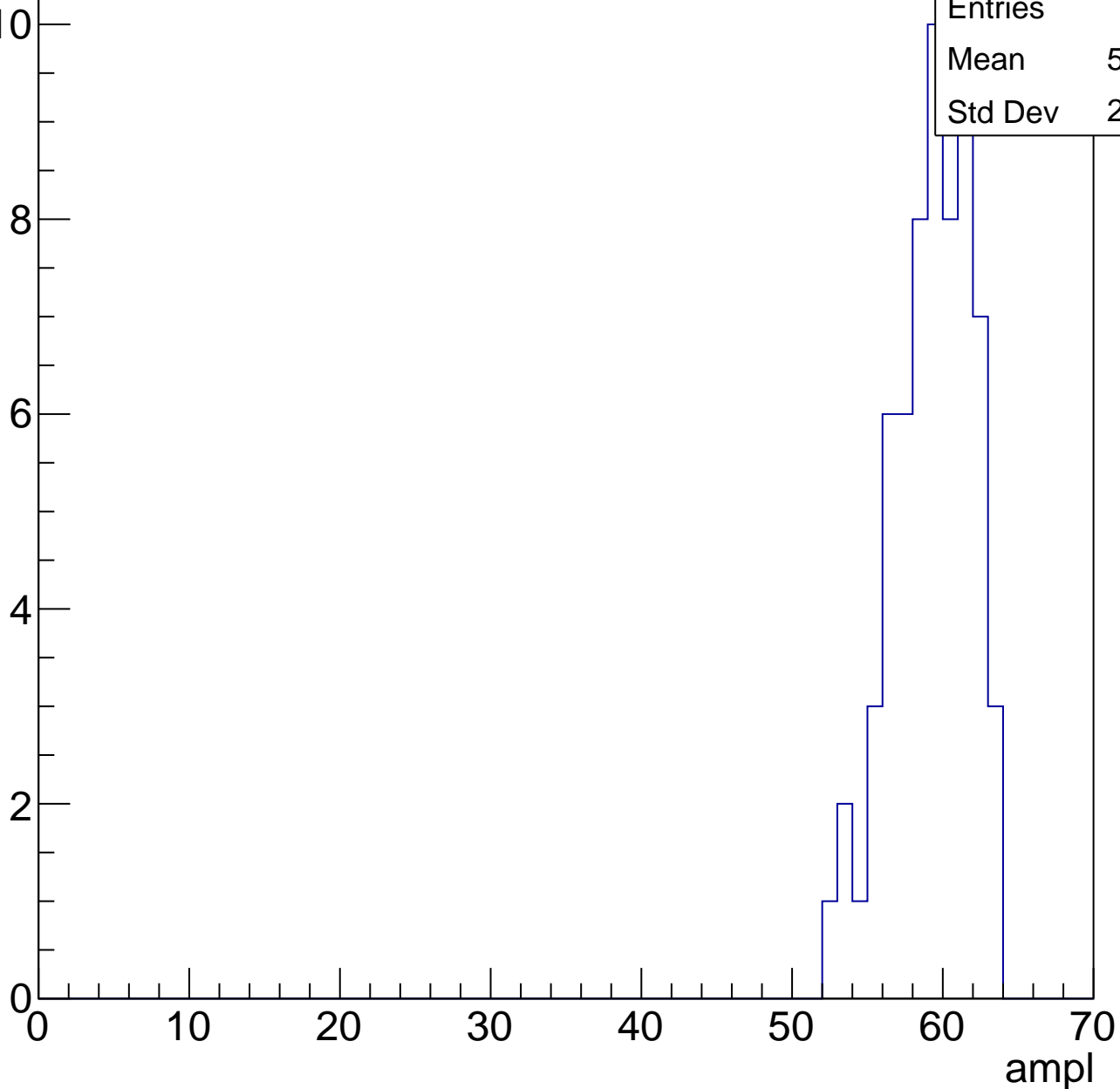
Entries	32
Mean	52.88
Std Dev	3.789

# B1L103S, U25-ch83, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	64
Mean	58.77
Std Dev	2.597

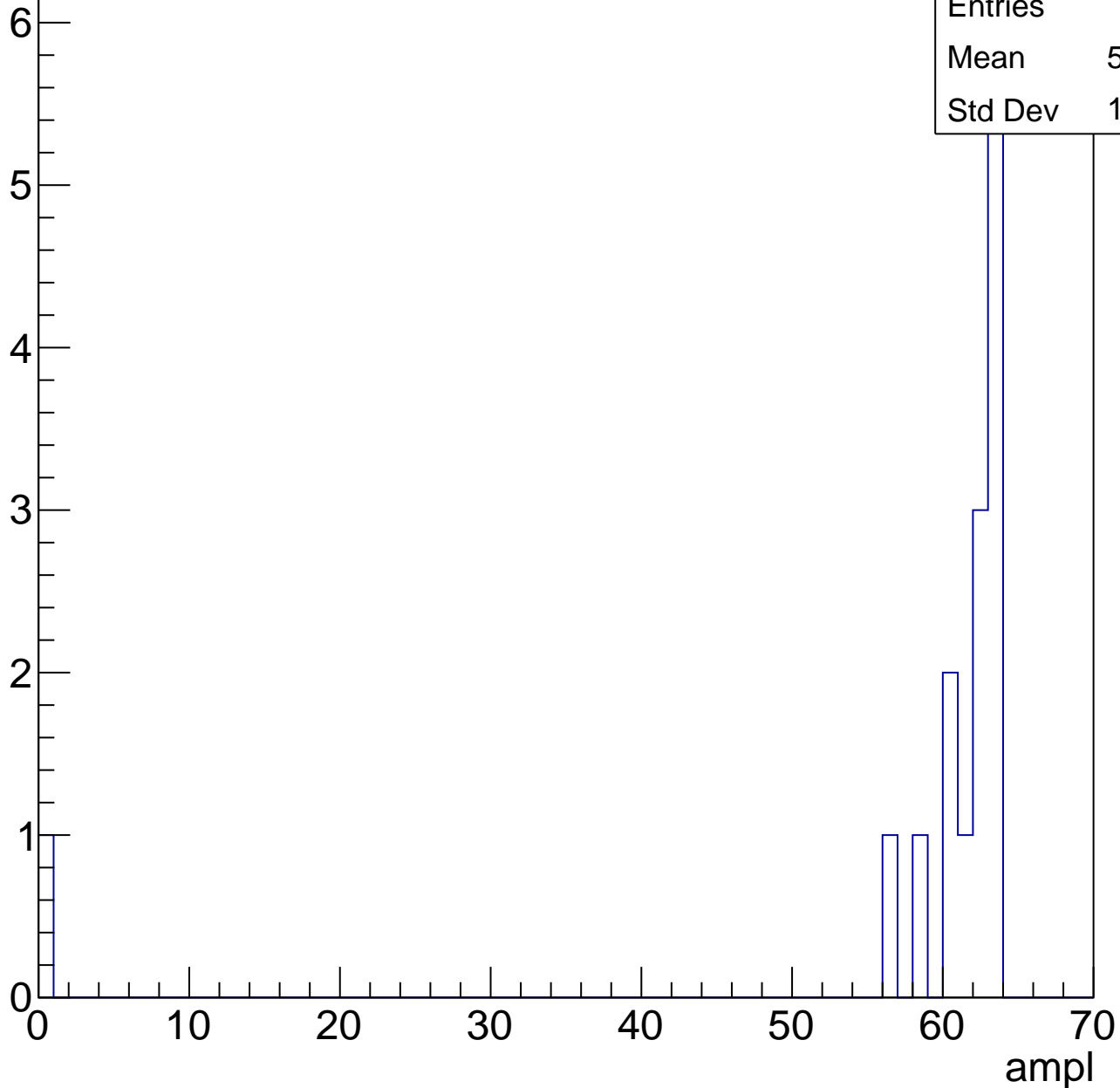


# B1L103S, U25-ch83, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	15
Mean	57.27
Std Dev	15.44

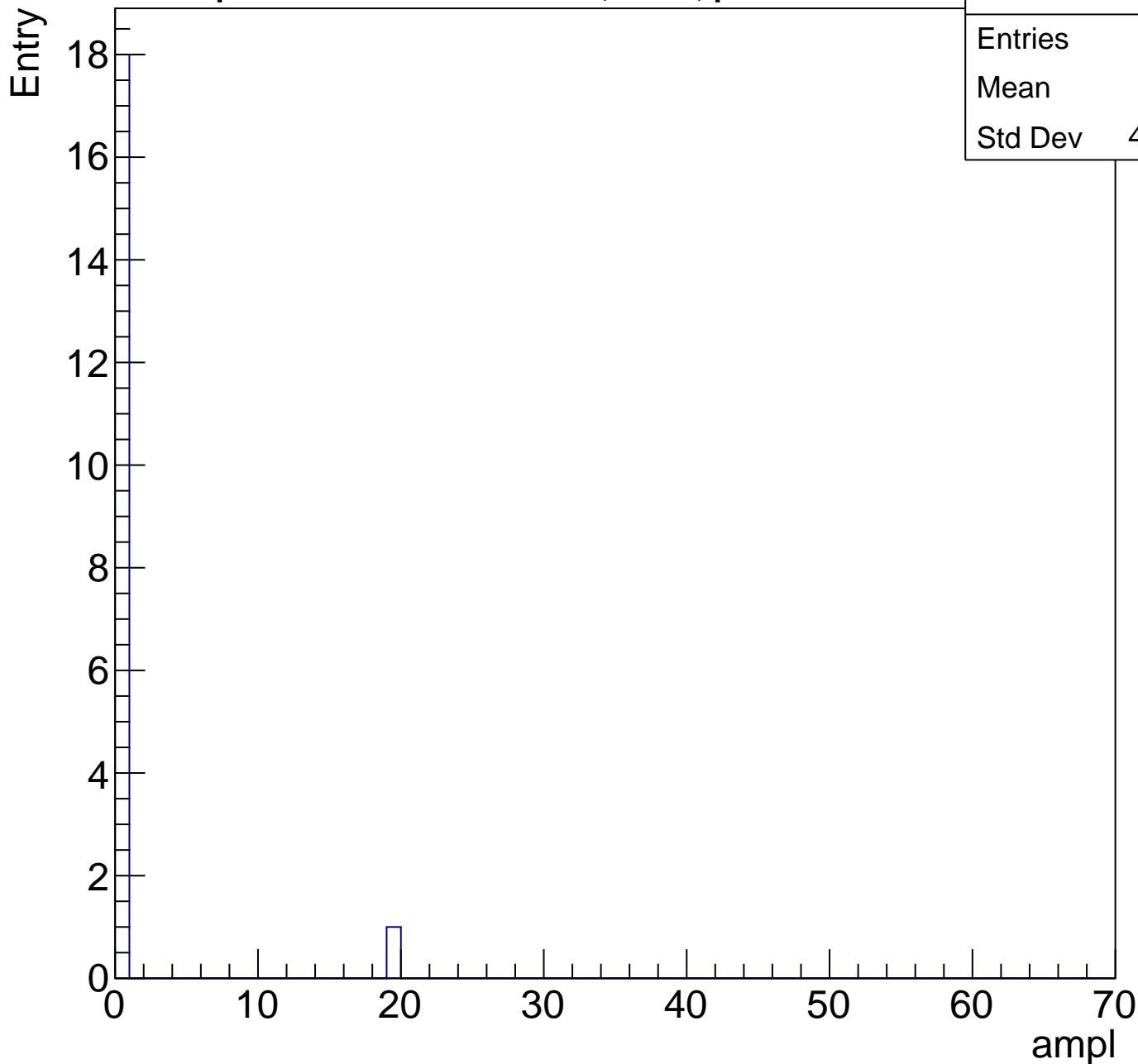




# B1L103S, U25-ch83, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	19
Mean	1
Std Dev	4.243

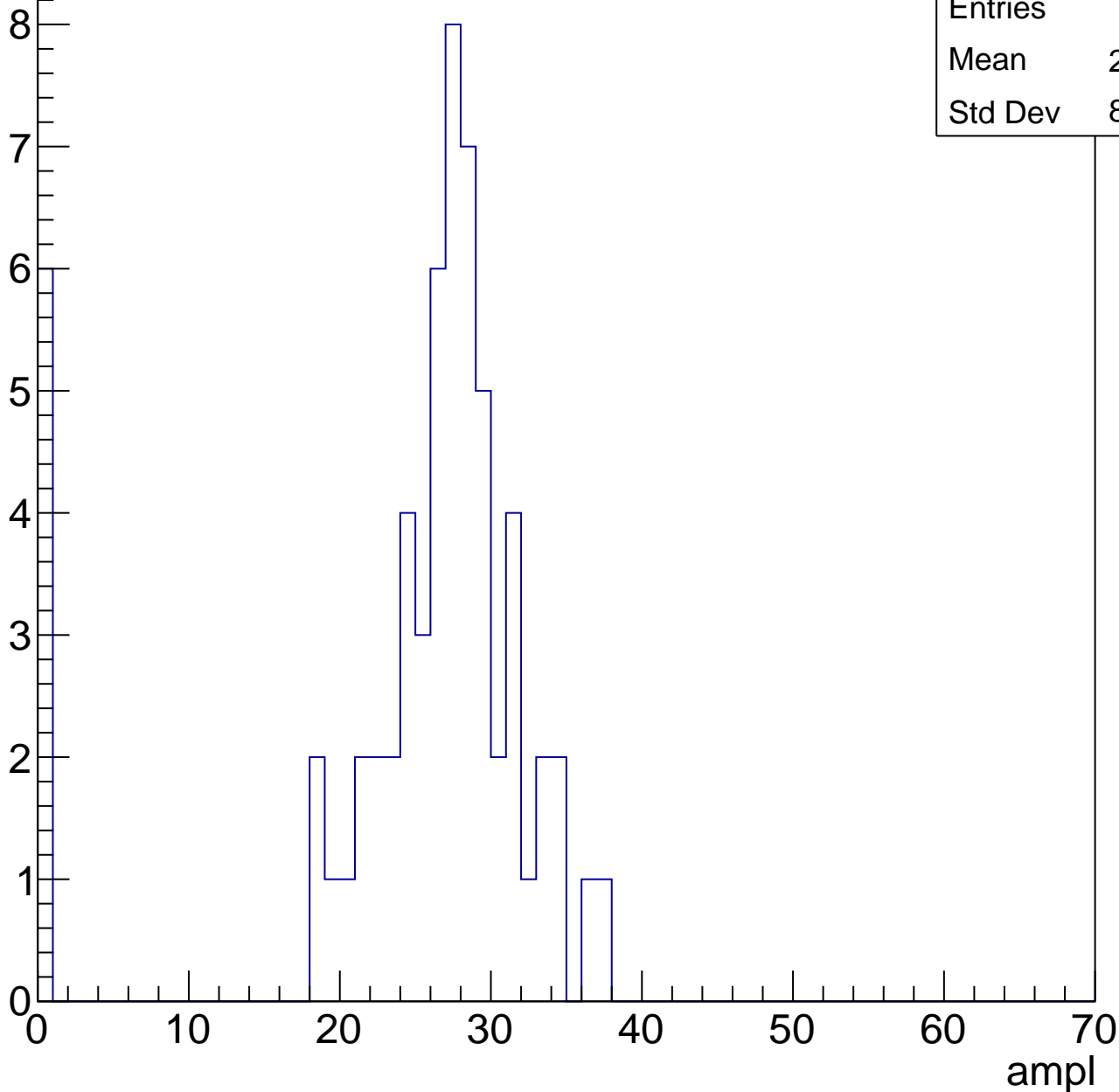


# B1L103S, U25-ch84, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	62
Mean	24.42
Std Dev	8.916

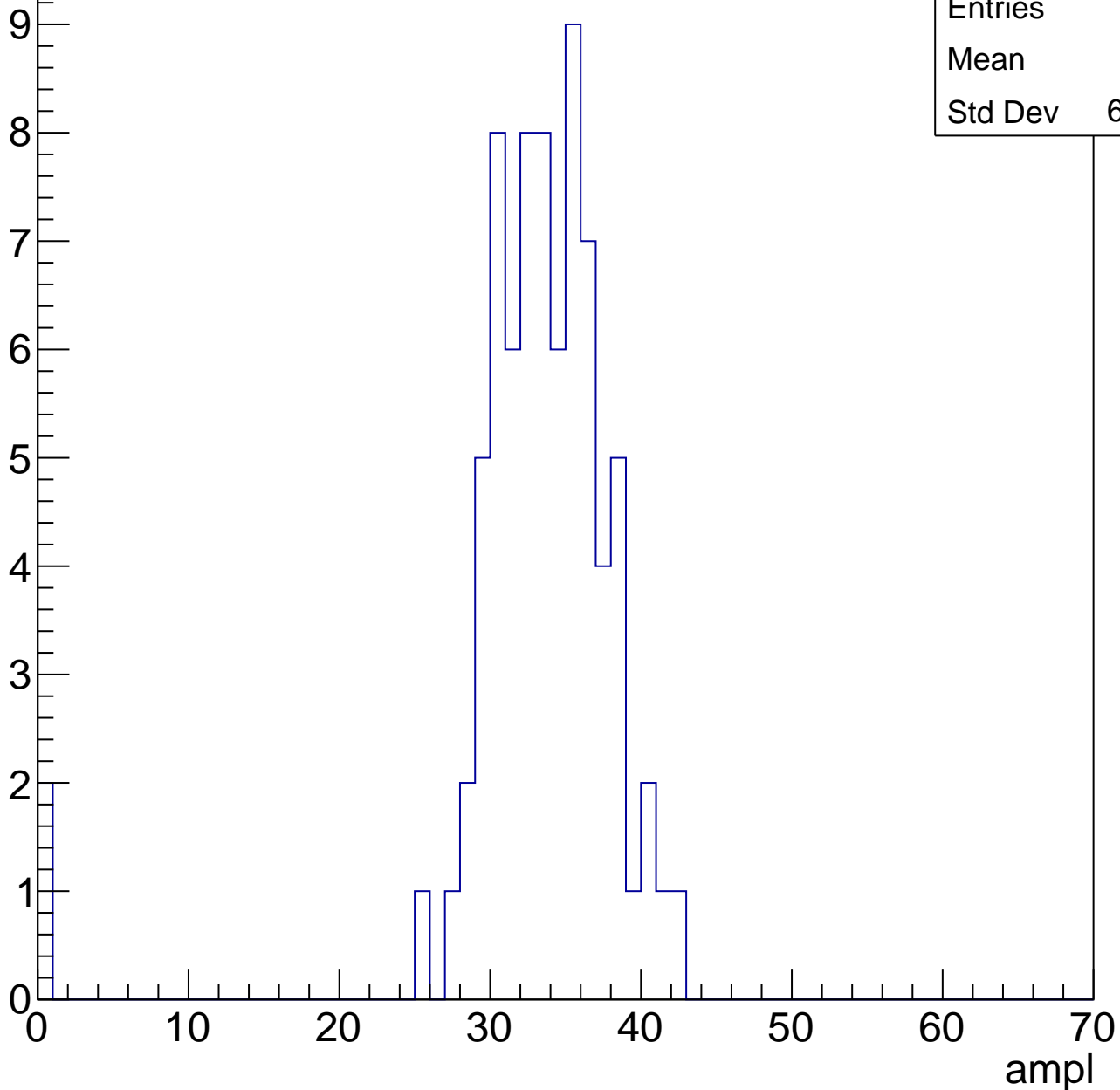


# B1L103S, U25-ch84, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

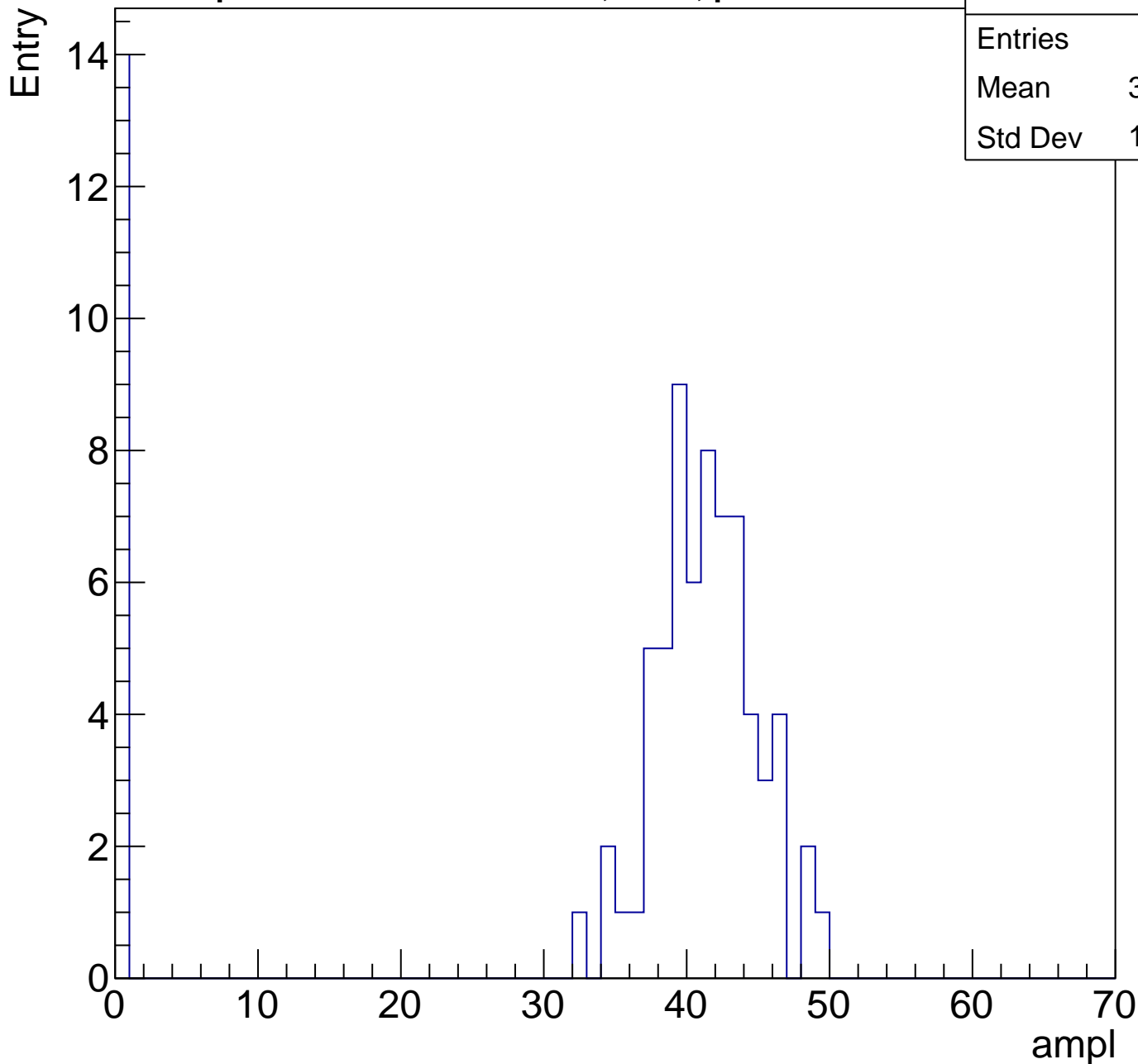
Entries	77
Mean	32.6
Std Dev	6.317



# B1L103S, U25-ch84, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	80
Mean	33.75
Std Dev	15.86

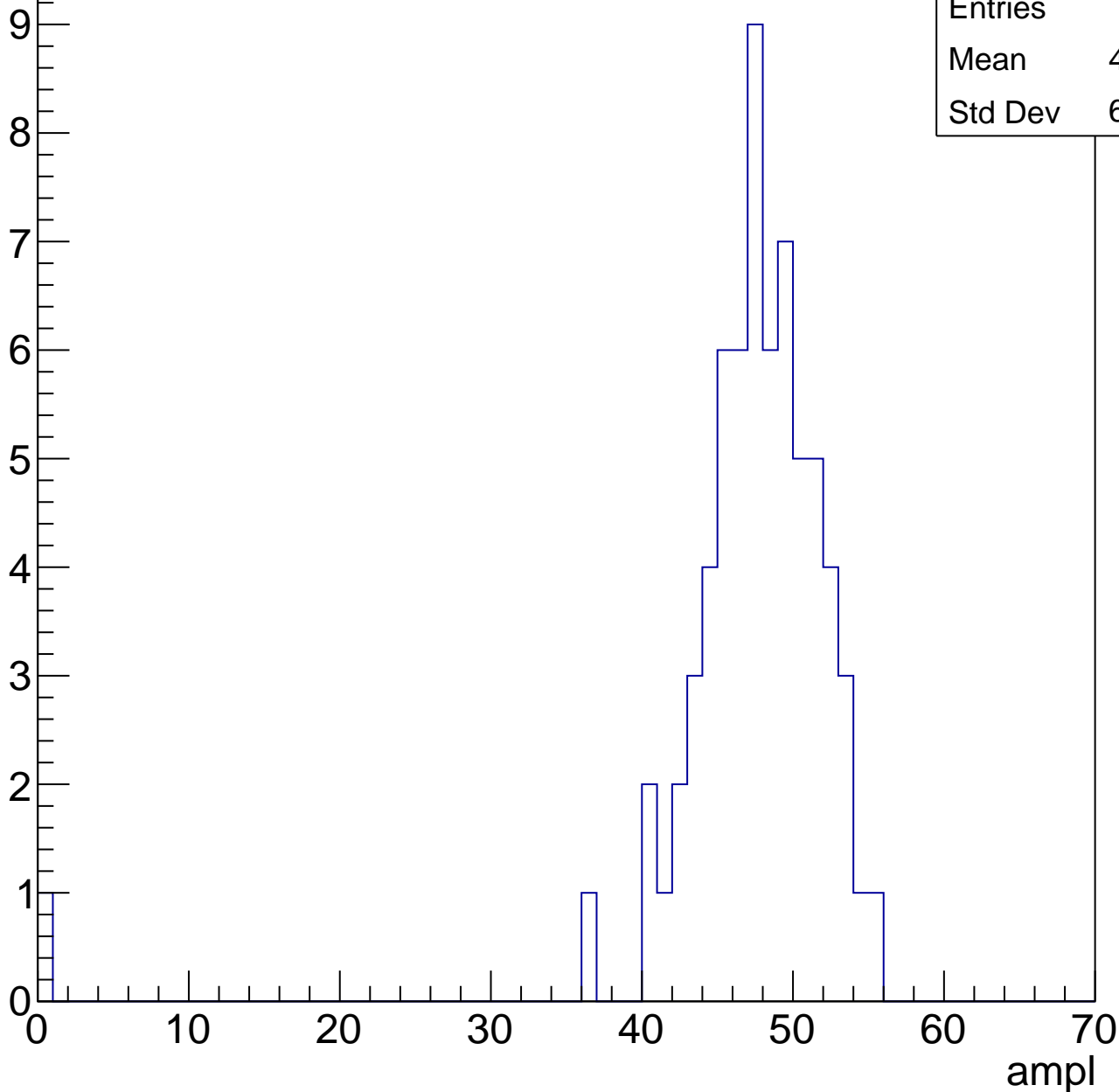


# B1L103S, U25-ch84, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	67
Mean	46.67
Std Dev	6.803

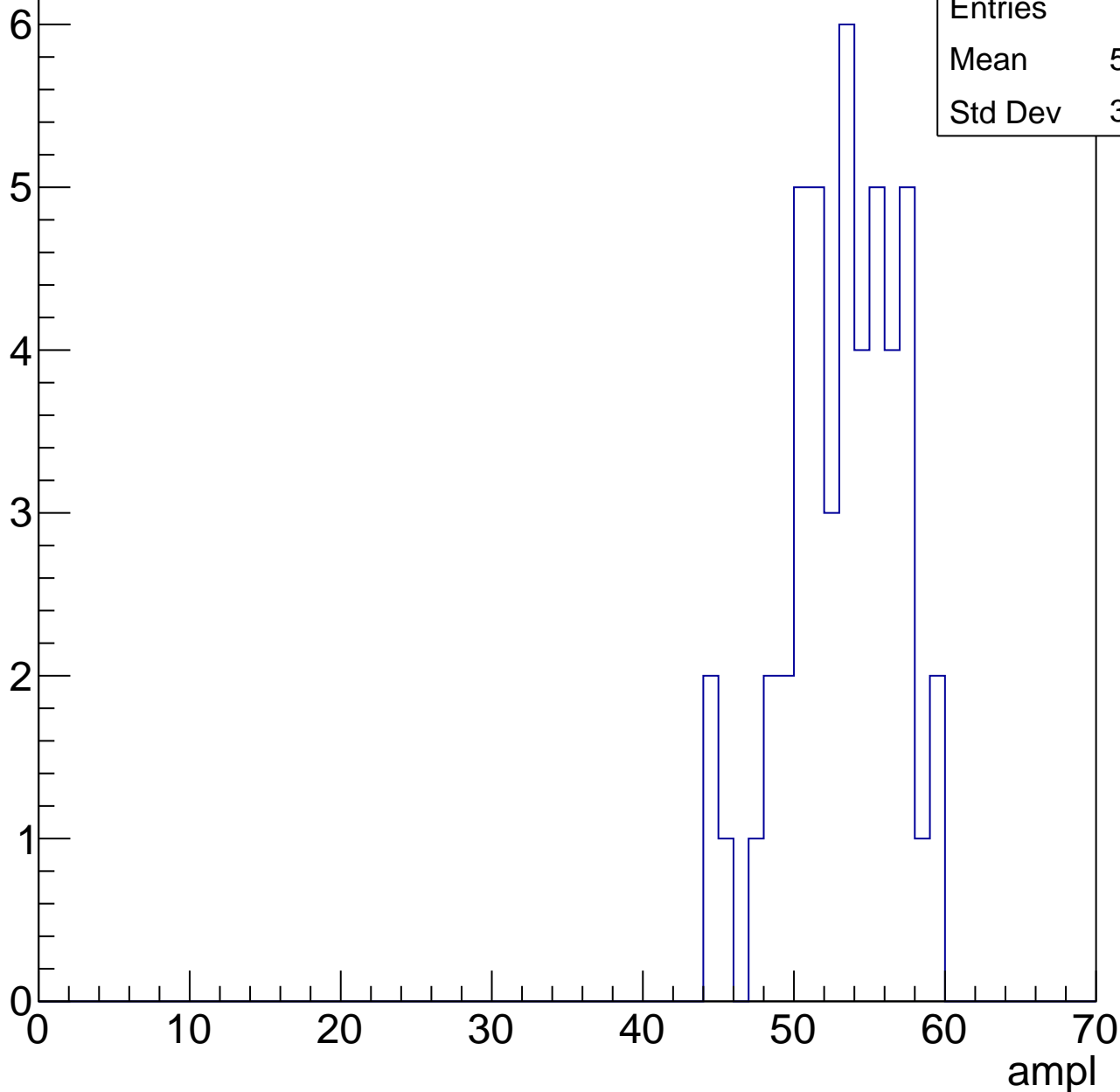


# B1L103S, U25-ch84, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

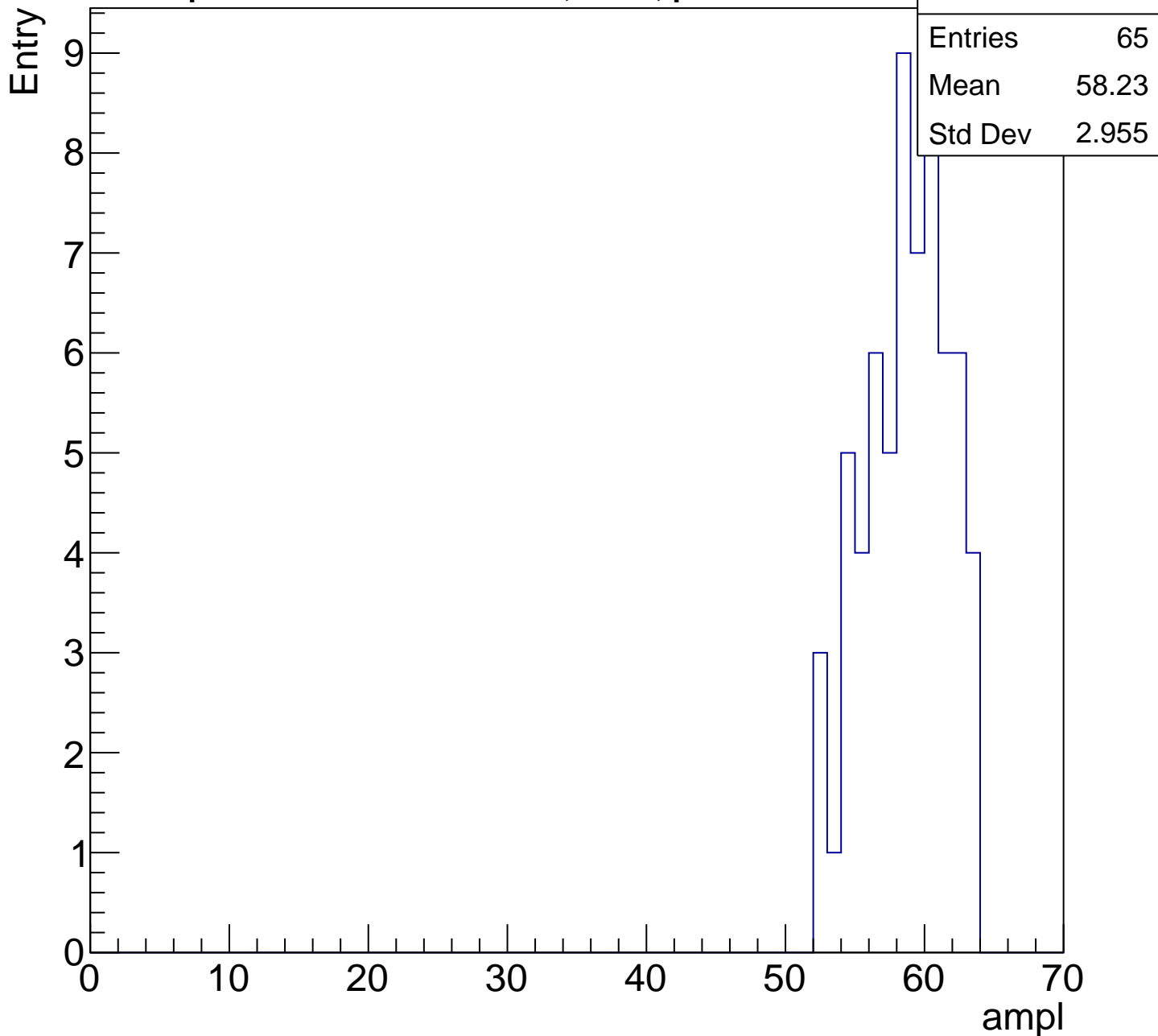
Entry

Entries	48
Mean	52.69
Std Dev	3.664



# B1L103S, U25-ch84, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

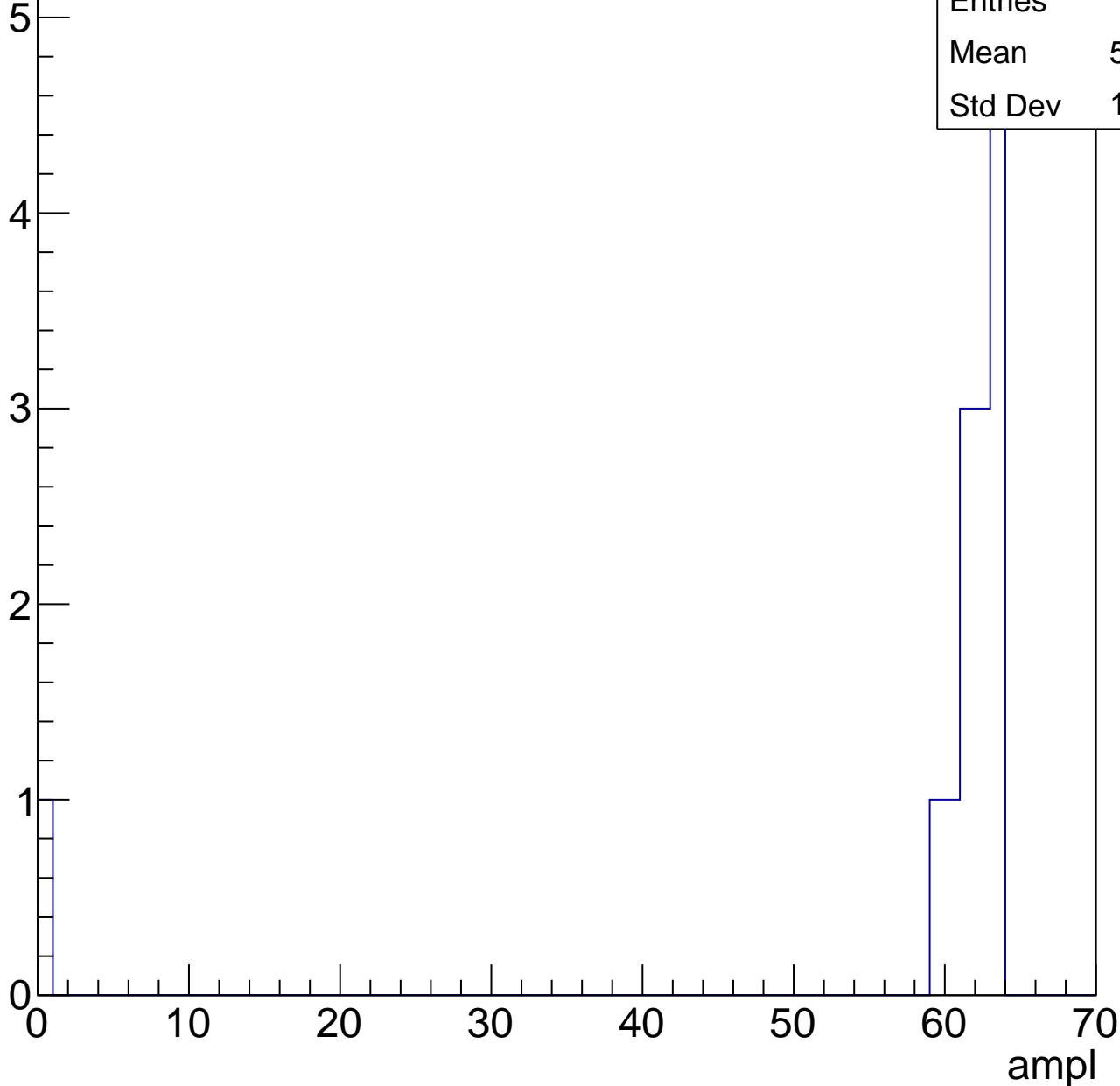


# B1L103S, U25-ch84, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	14
Mean	57.36
Std Dev	15.95



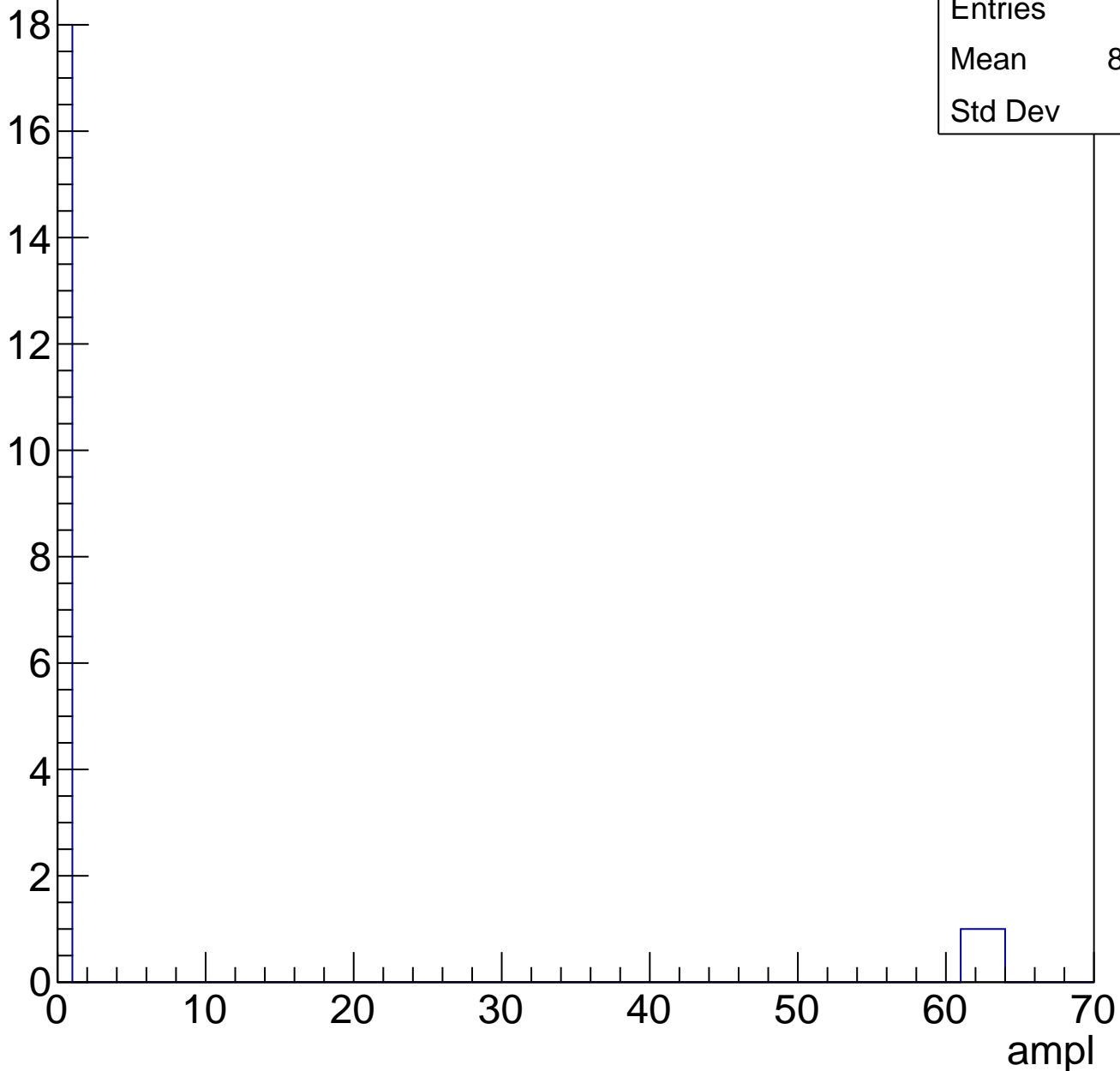


# B1L103S, U25-ch84, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	21
Mean	8.857
Std Dev	21.7

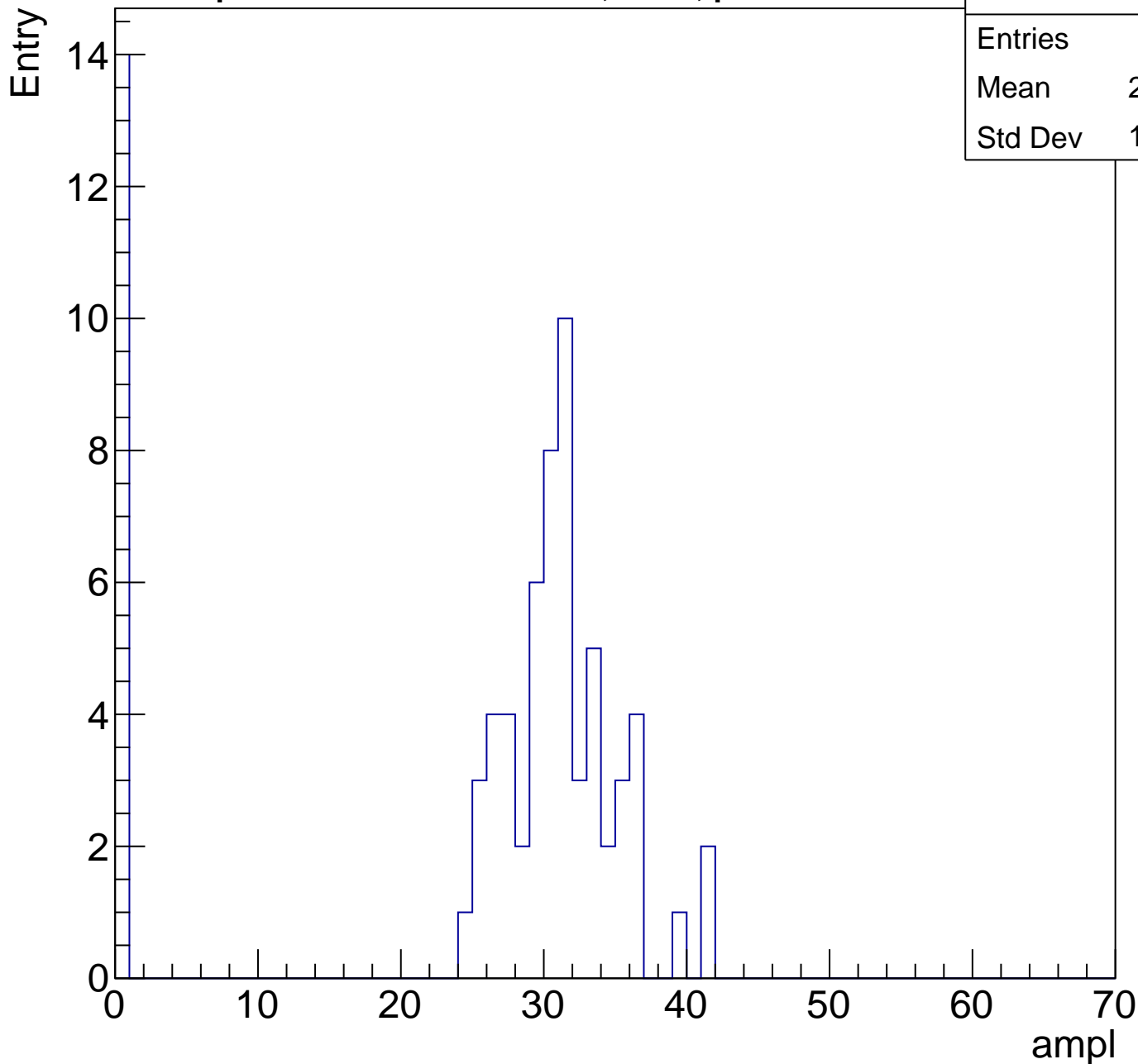
Entry



# B1L103S, U25-ch85, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	72
Mean	24.86
Std Dev	12.67

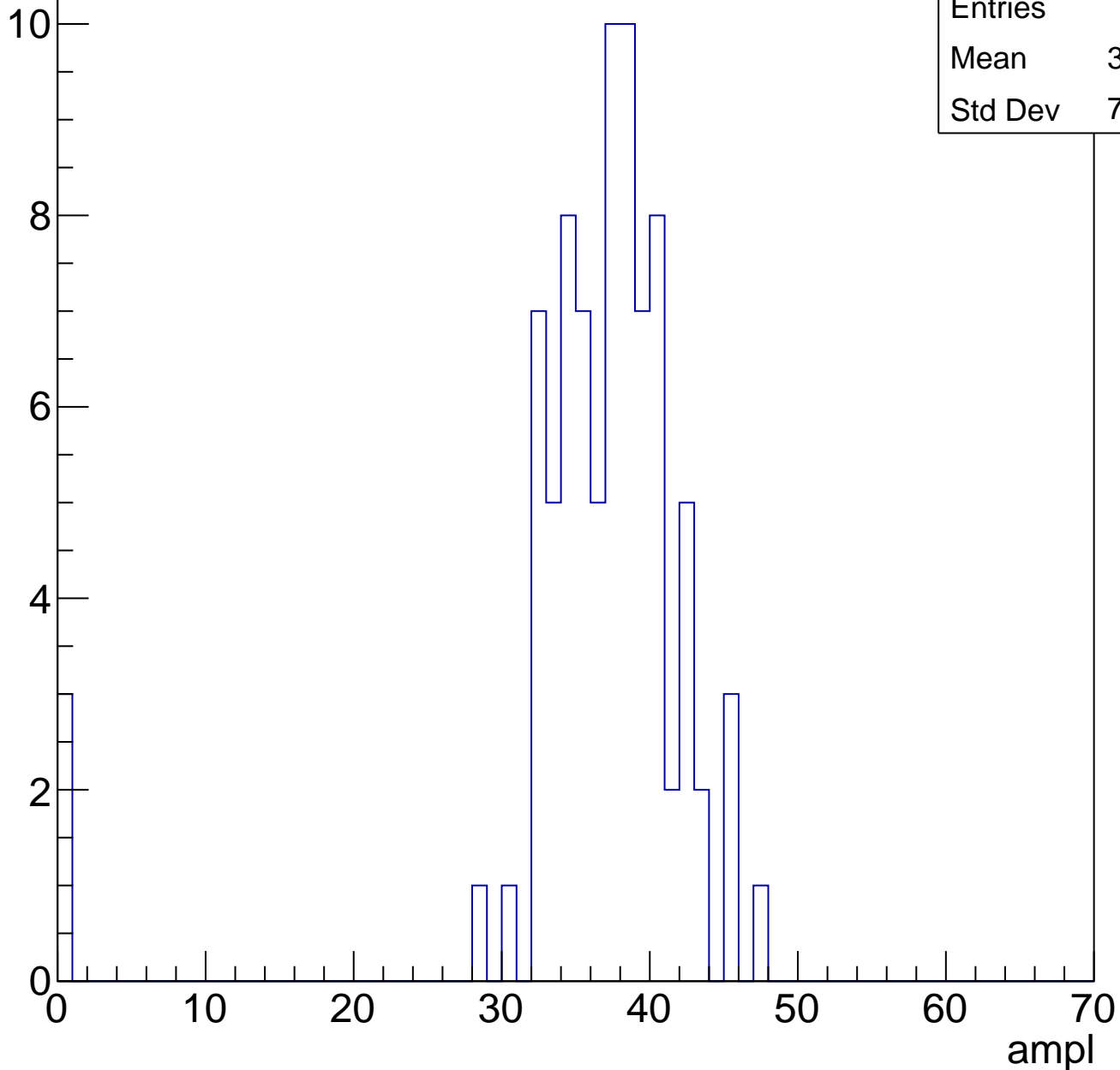


# B1L103S, U25-ch85, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	85
Mean	35.85
Std Dev	7.757

Entry



# B1L103S, U25-ch85, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	73
Mean	37.81
Std Dev	16.2

Entry

10

8

6

4

2

0

0

10

20

30

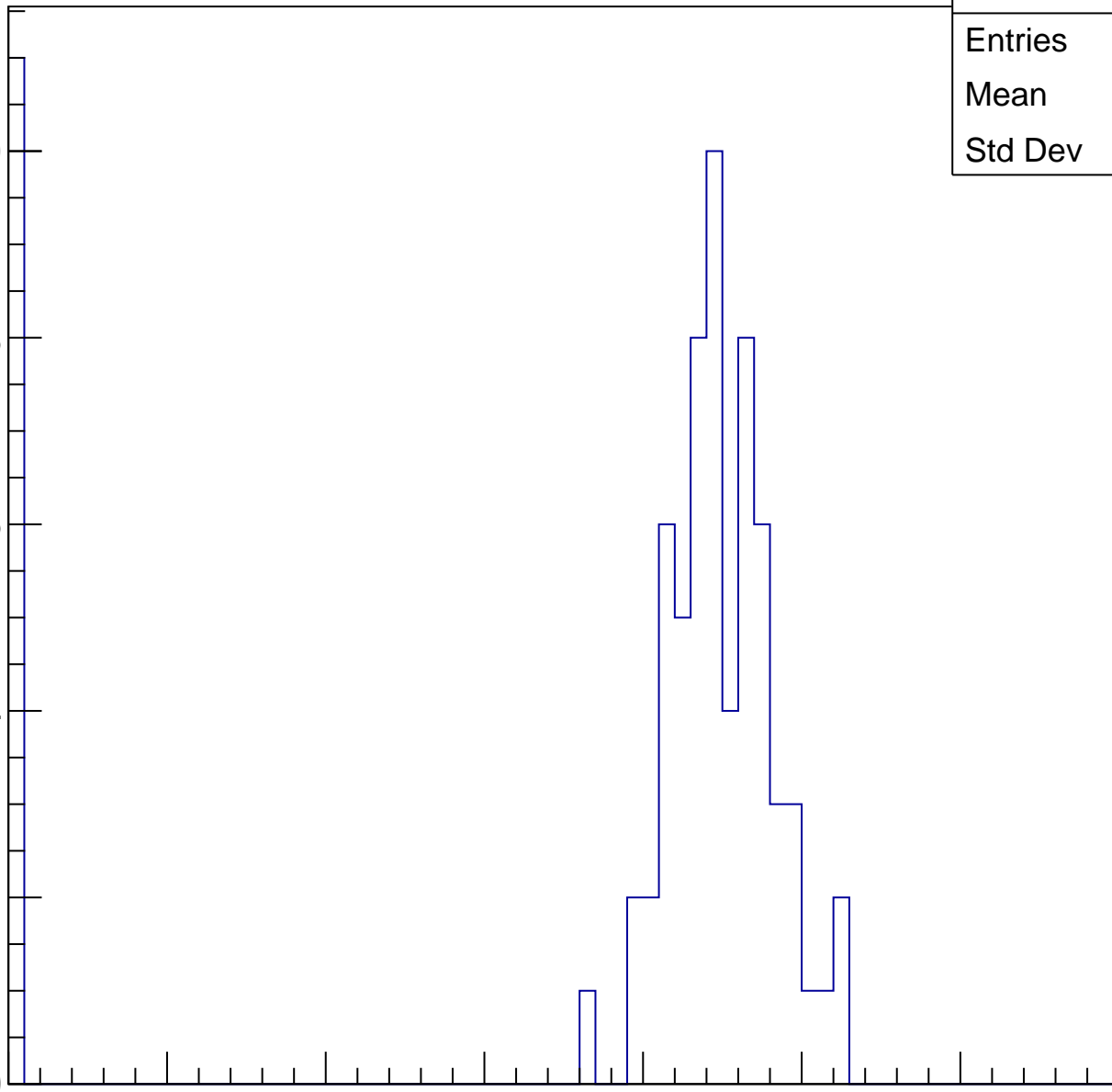
40

50

60

70

ampl

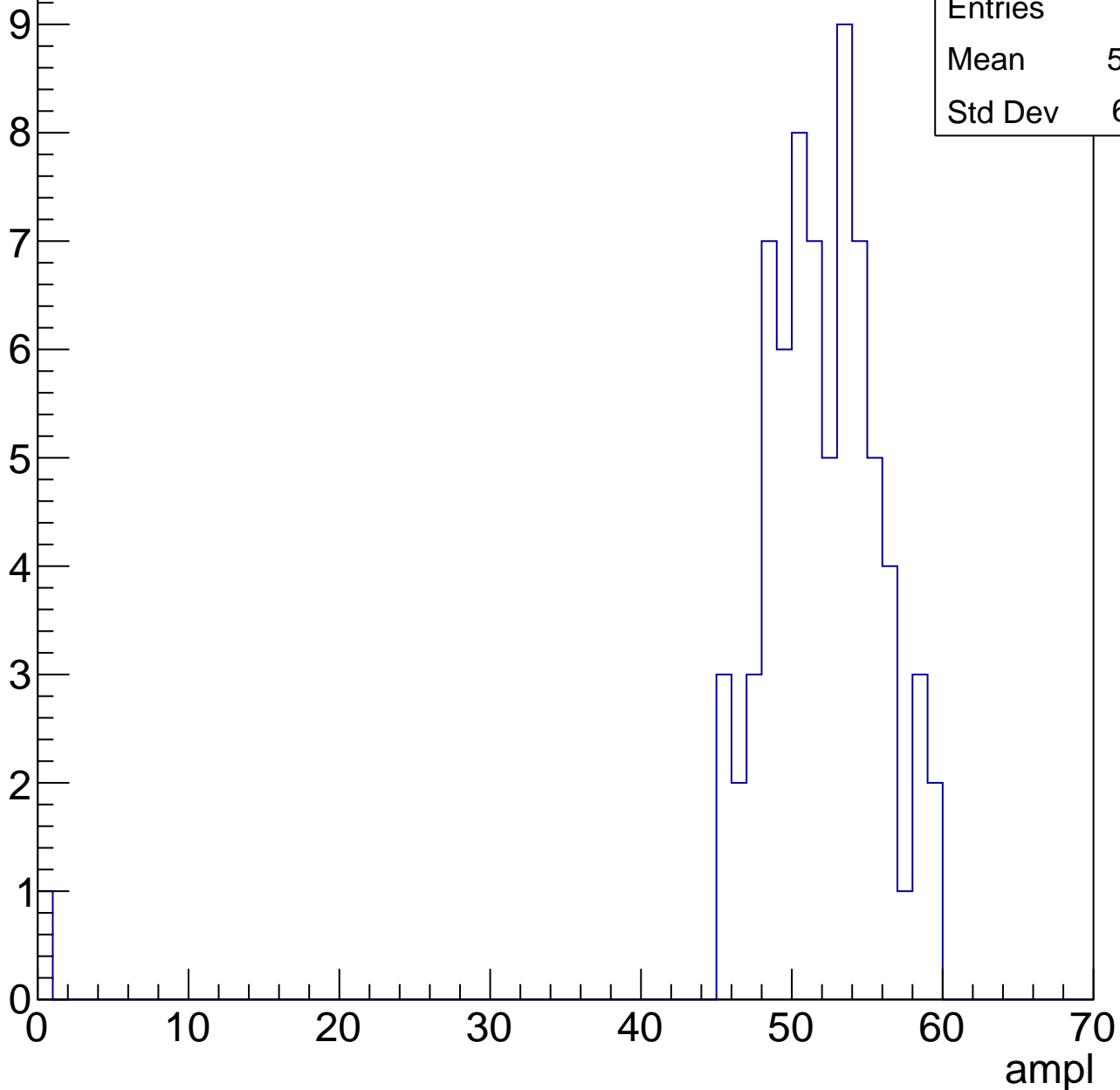


# B1L103S, U25-ch85, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	73
Mean	50.93
Std Dev	6.921

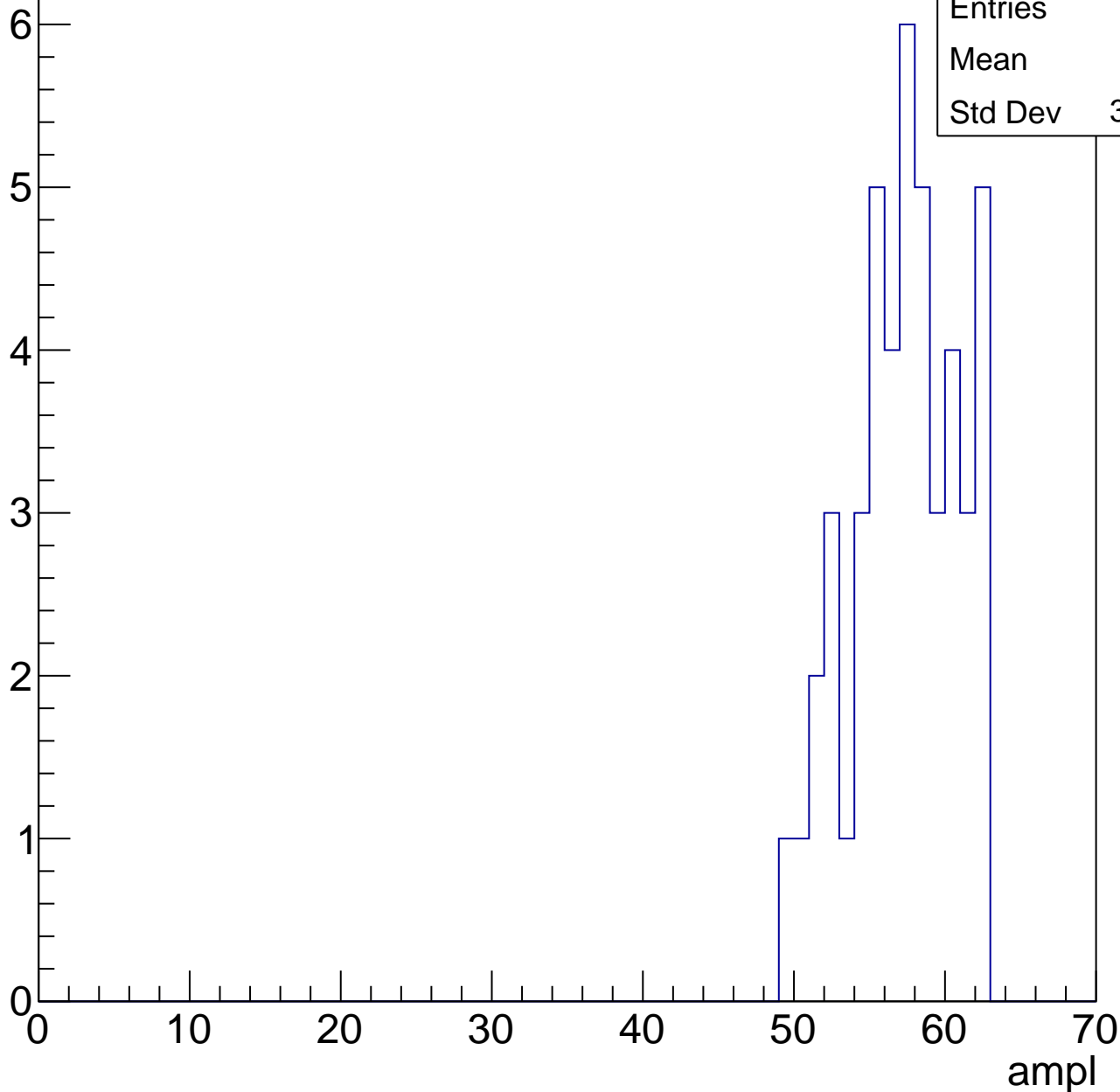


# B1L103S, U25-ch85, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	46
Mean	56.8
Std Dev	3.462

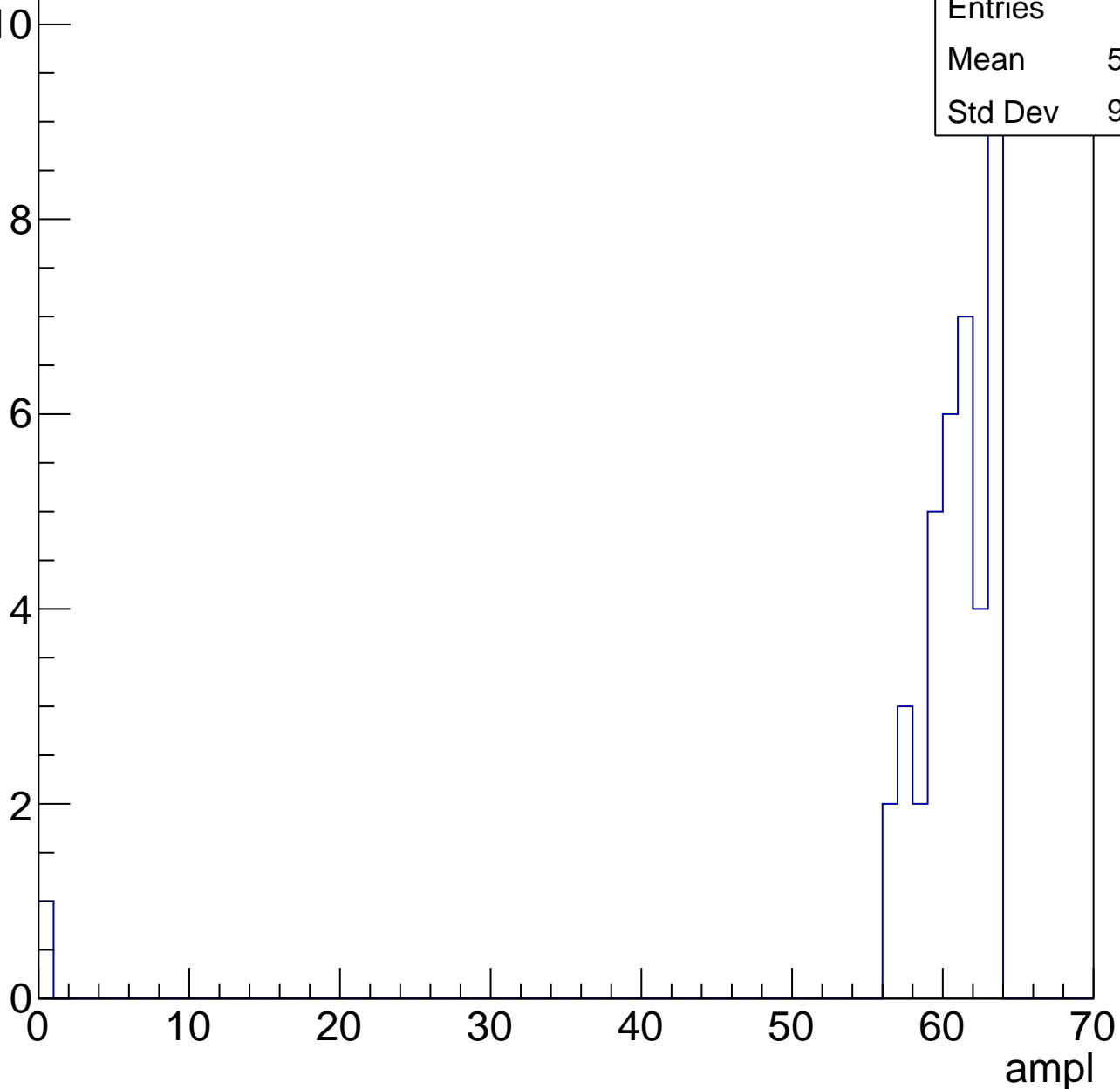


# B1L103S, U25-ch85, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	40
Mean	58.98
Std Dev	9.673



# B1L103S, U25-ch85, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U25-ch85, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

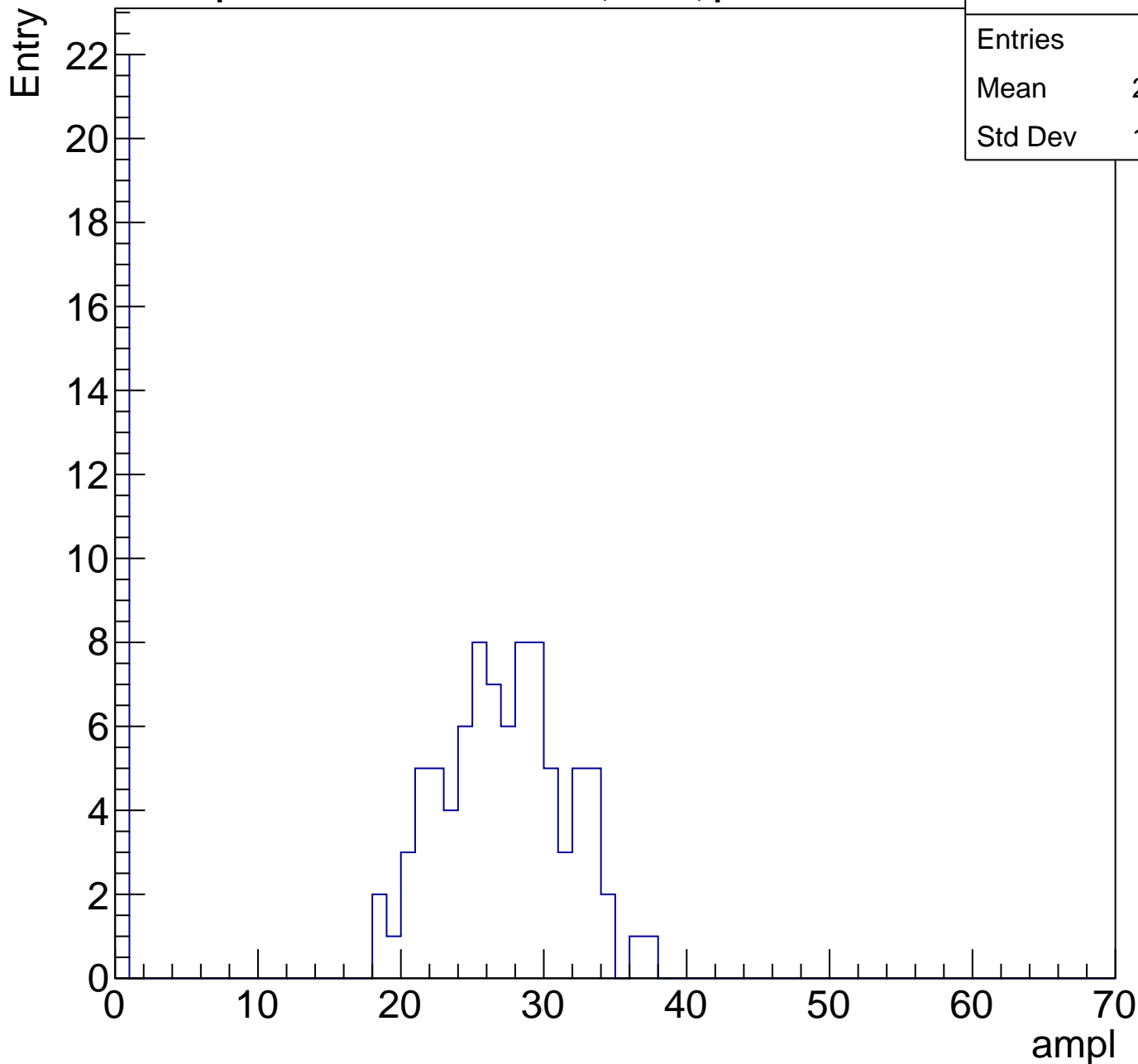
ampl

Entries	19
Mean	0
Std Dev	0

# B1L103S, U25-ch86, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	107
Mean	21.26
Std Dev	11.47

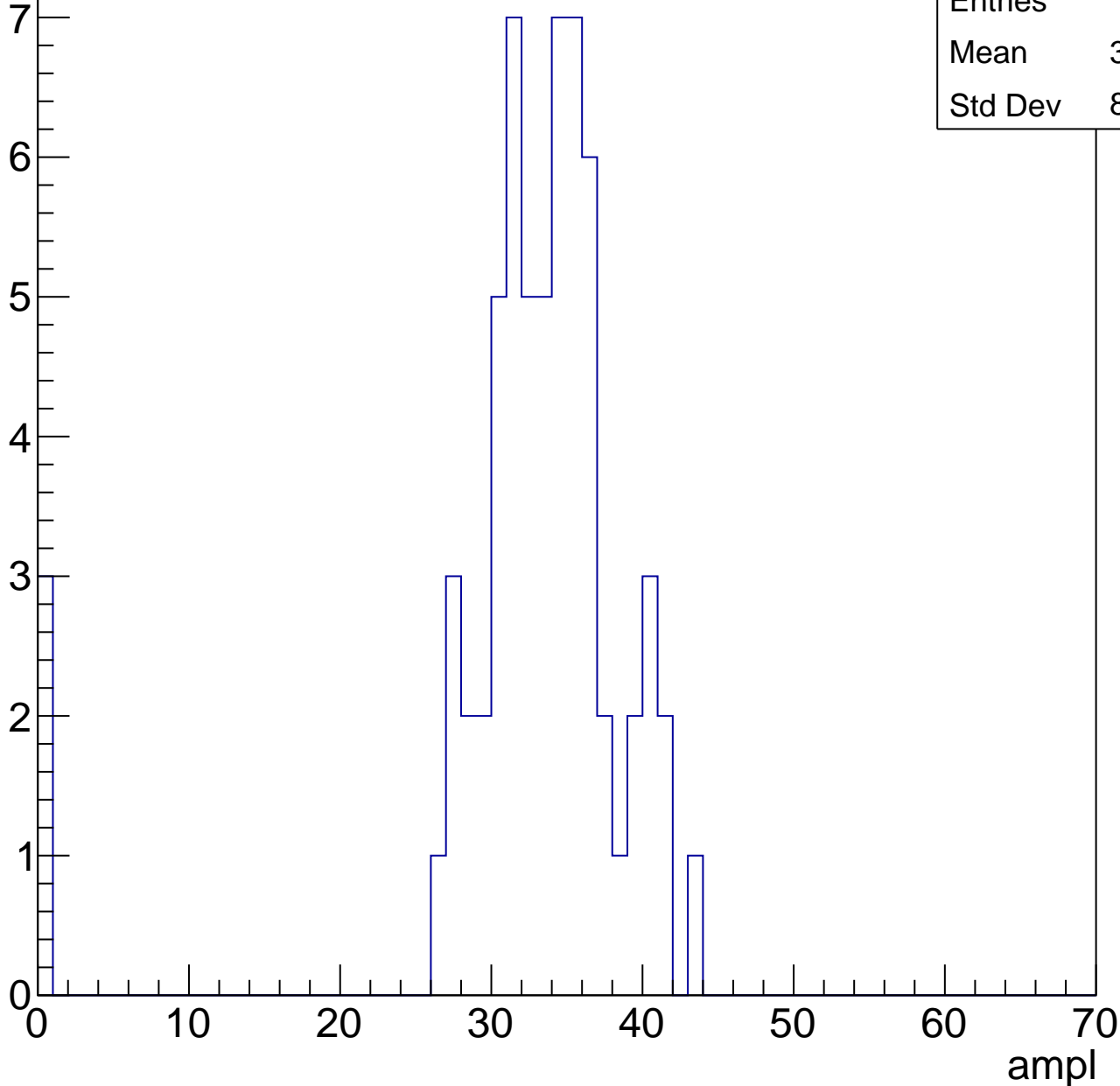


# B1L103S, U25-ch86, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	64
Mean	31.98
Std Dev	8.015

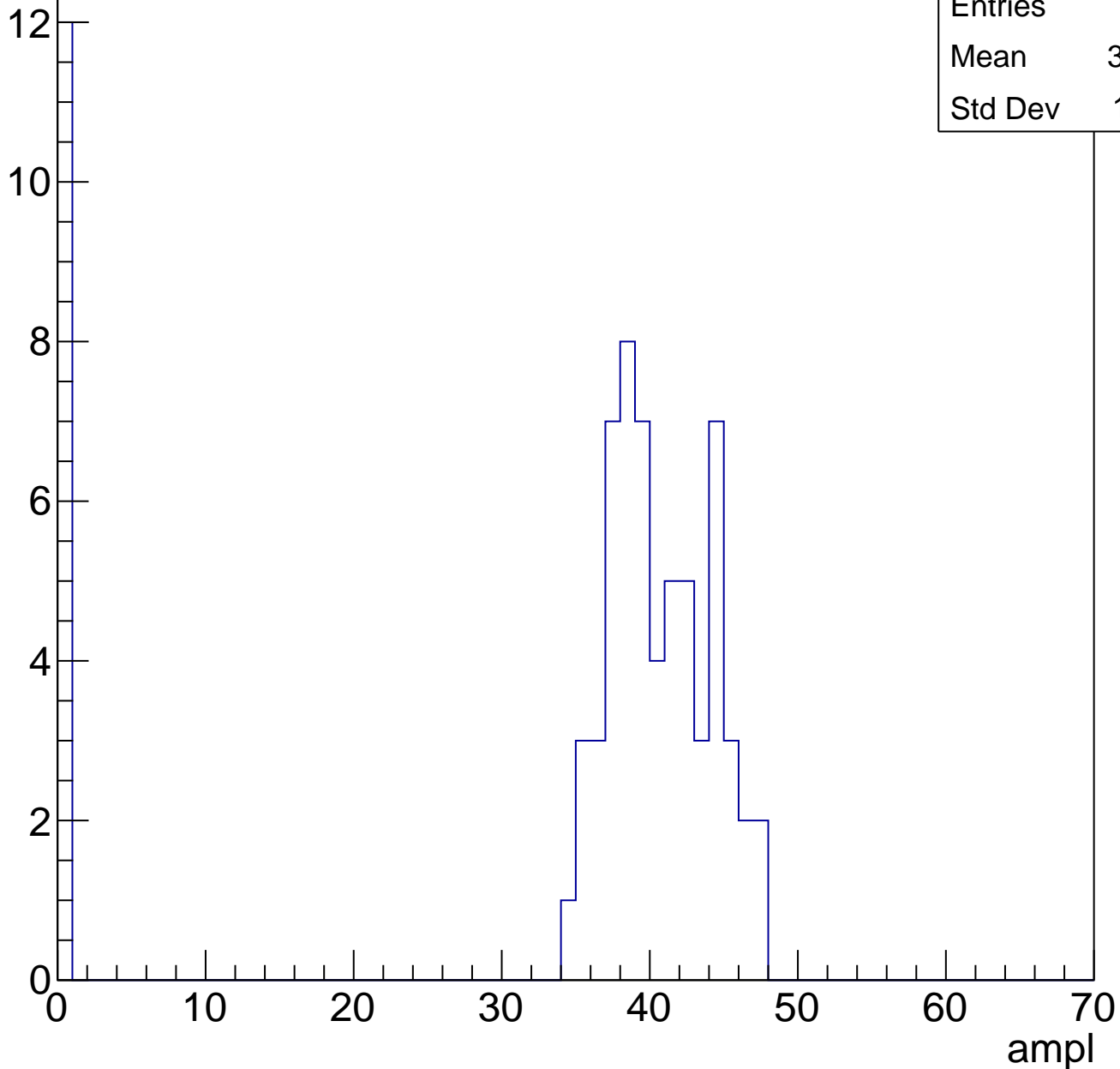


# B1L103S, U25-ch86, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	72
Mean	33.56
Std Dev	15.31

Entry

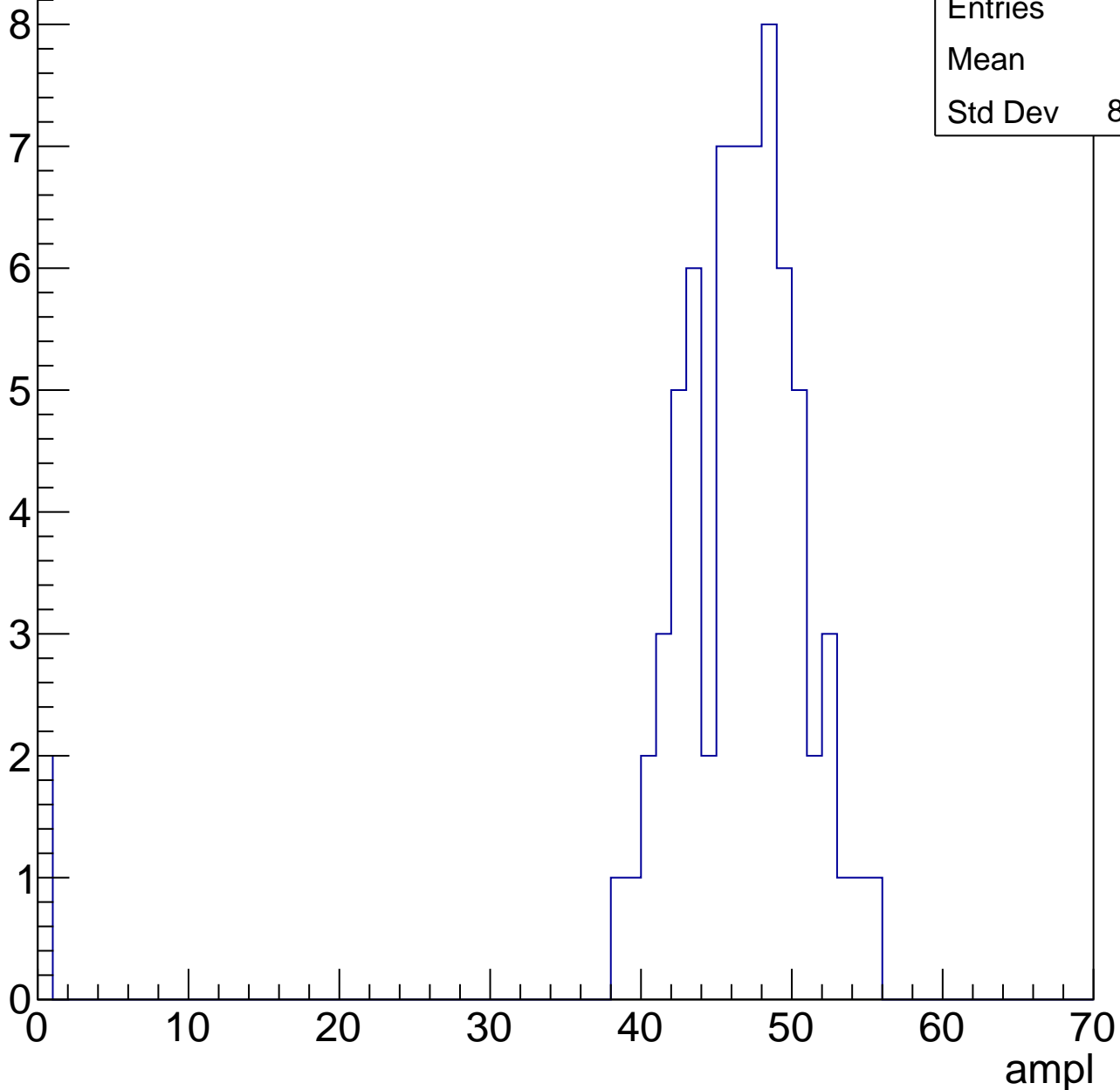


# B1L103S, U25-ch86, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	70
Mean	45
Std Dev	8.532

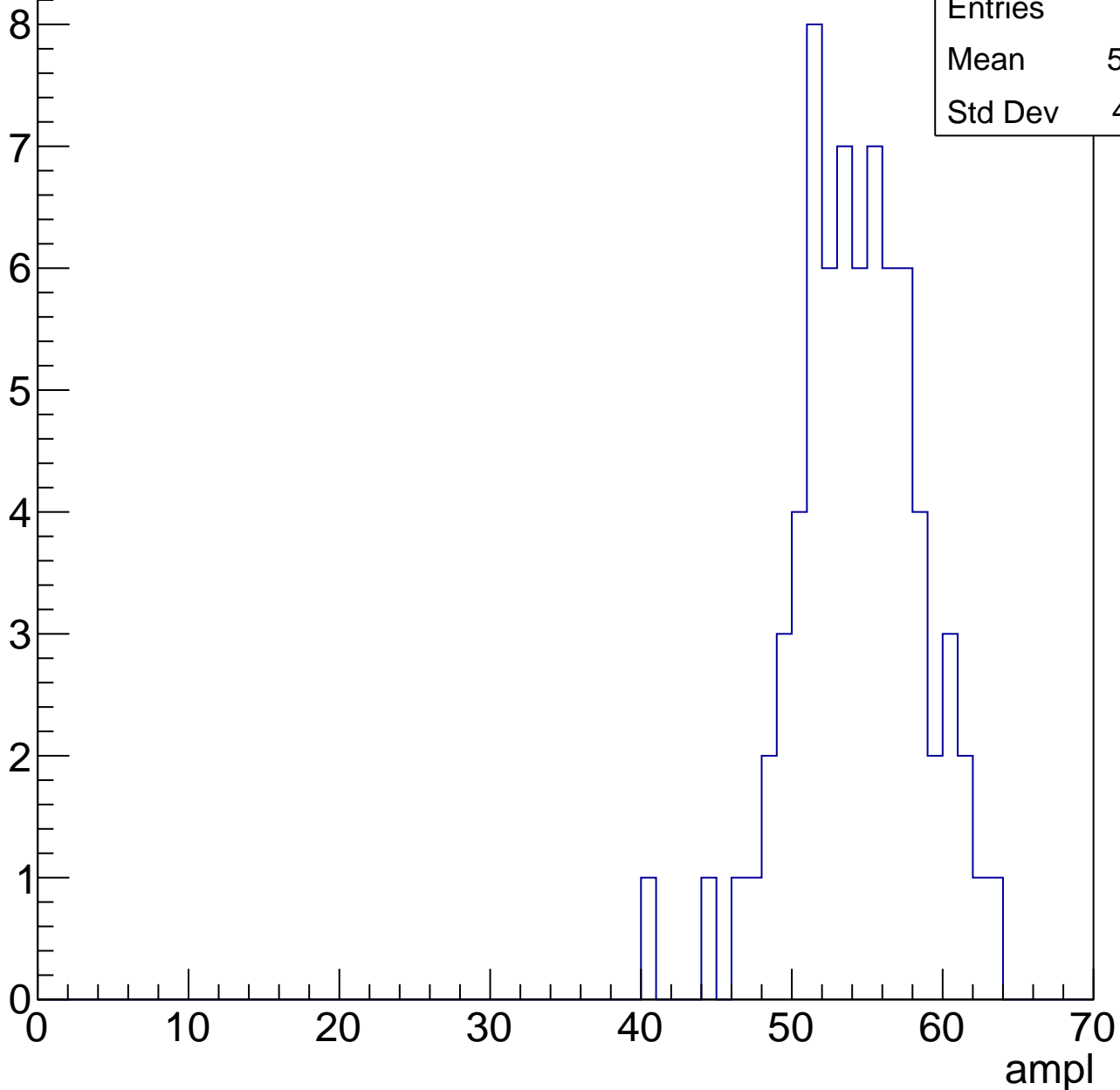


# B1L103S, U25-ch86, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	72
Mean	53.82
Std Dev	4.201

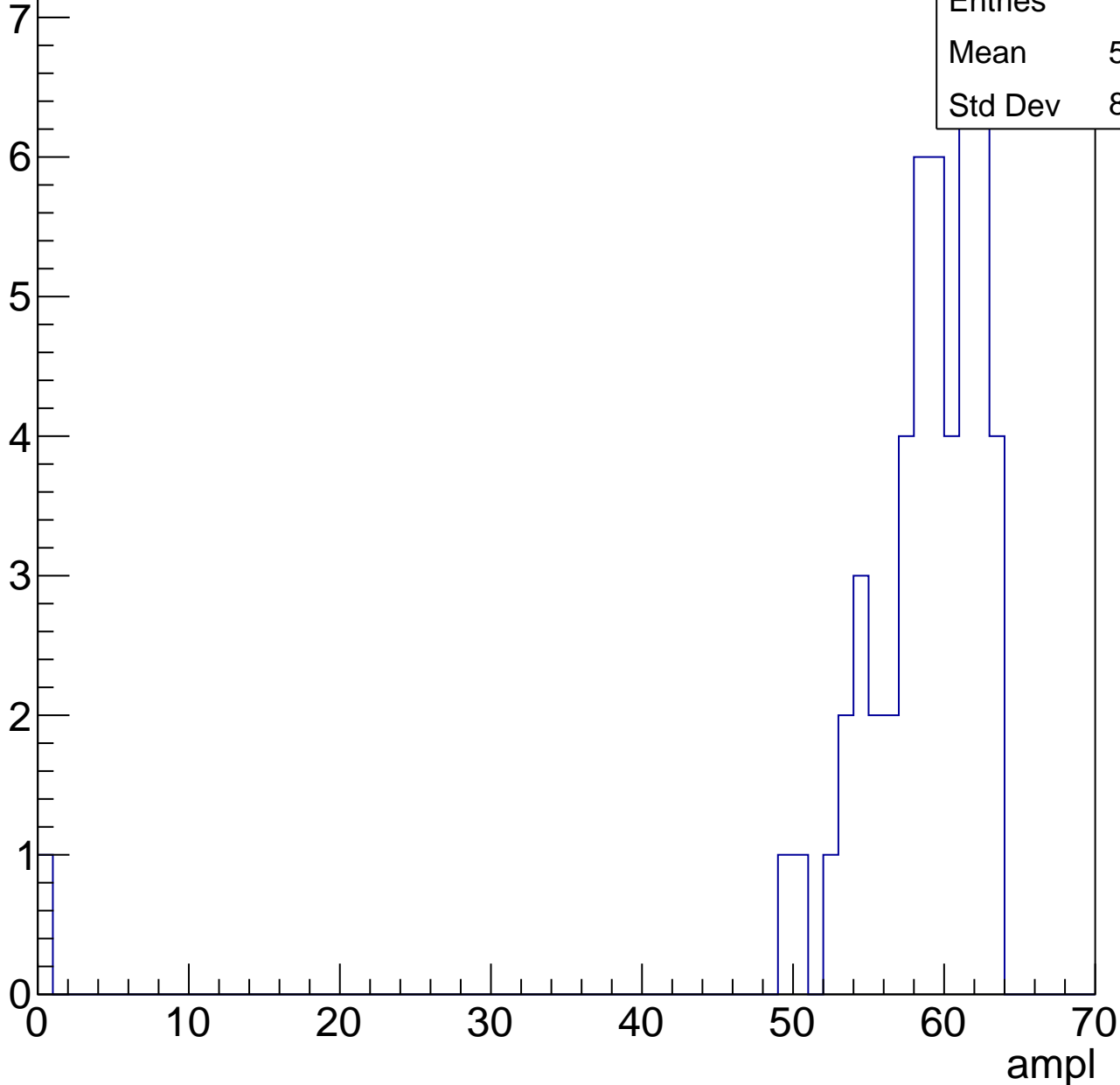


# B1L103S, U25-ch86, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

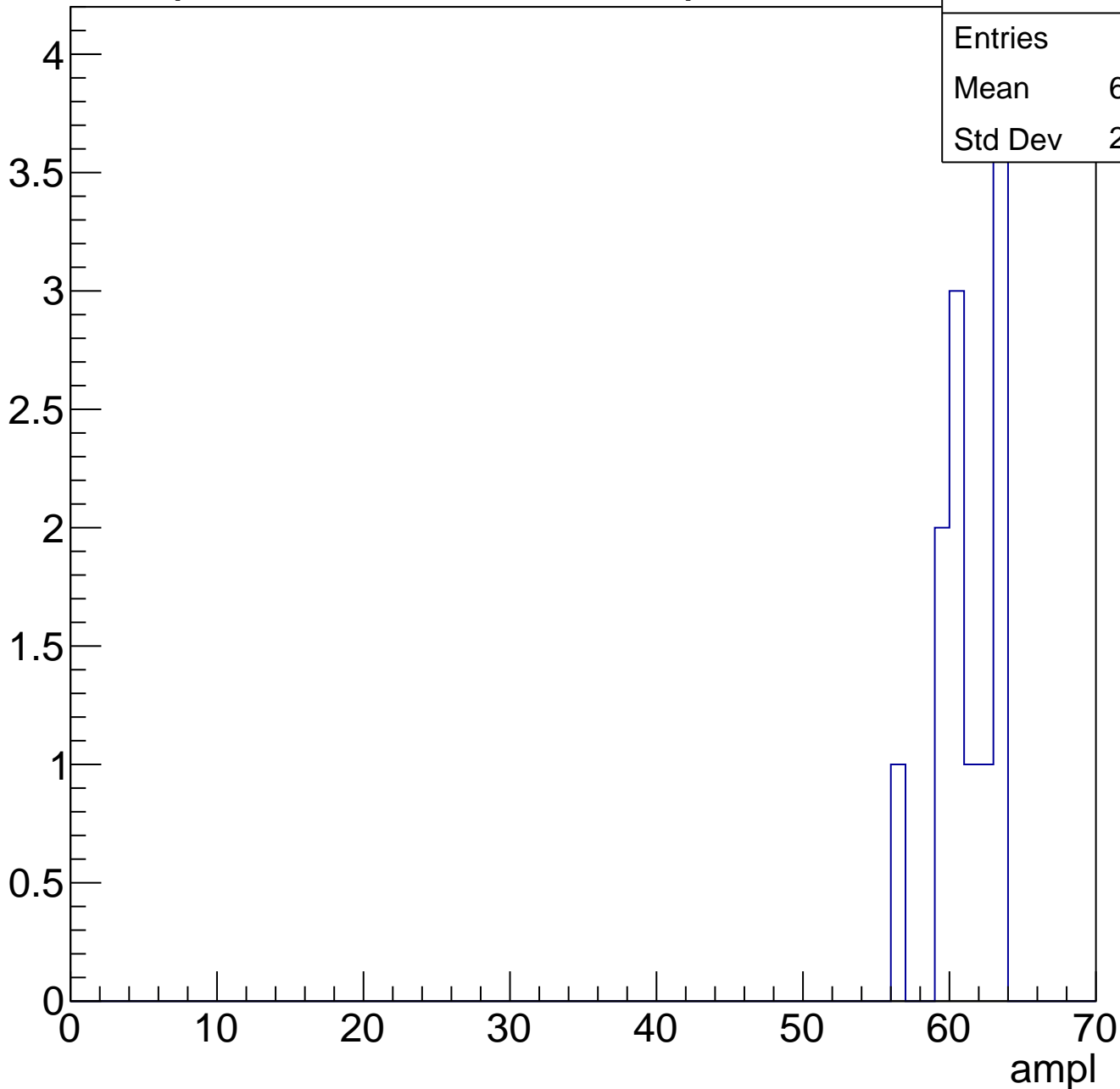
Entries	51
Mean	57.33
Std Dev	8.798



# B1L103S, U25-ch86, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



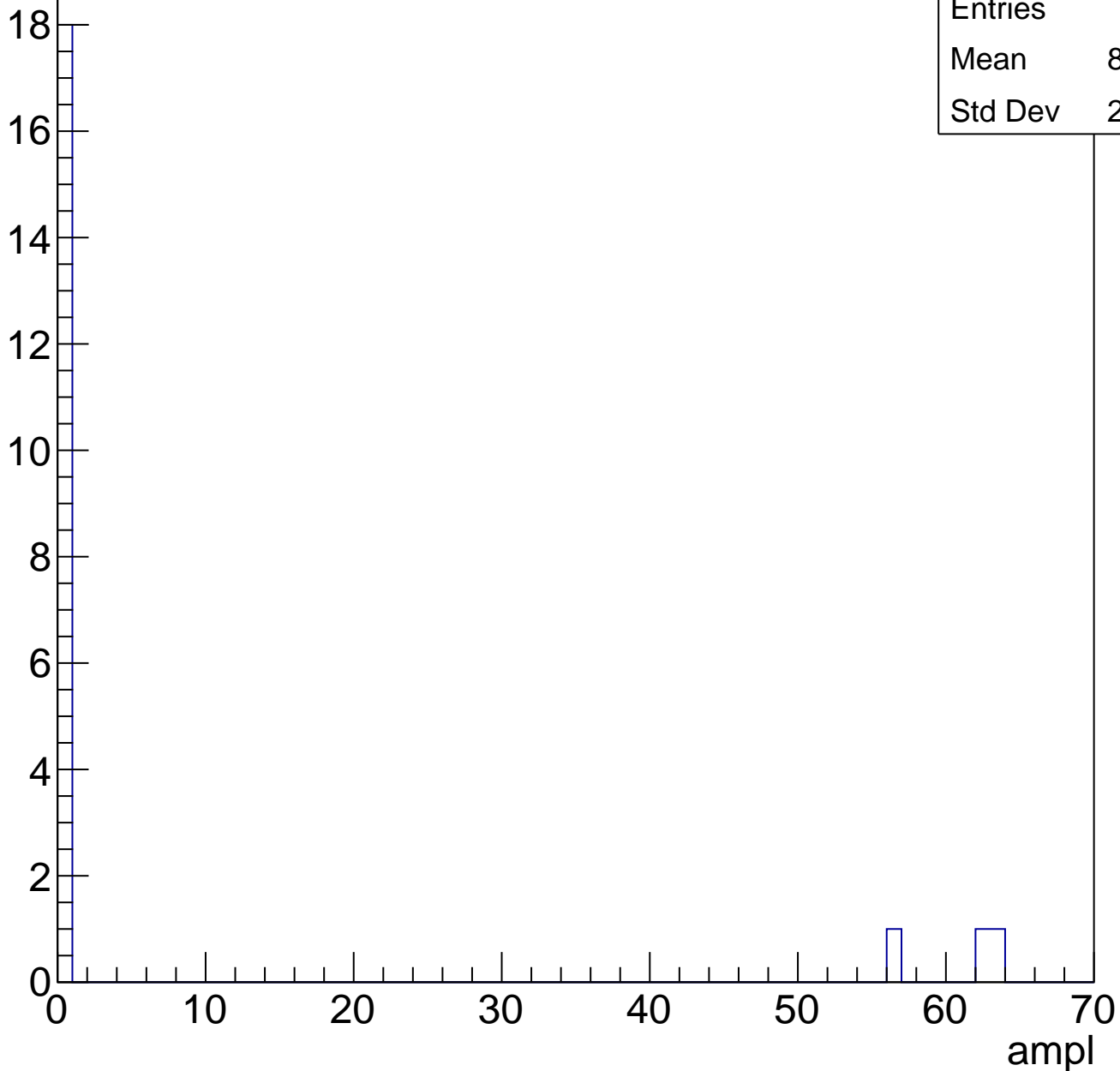


# B1L103S, U25-ch86, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	21
Mean	8.619
Std Dev	21.14

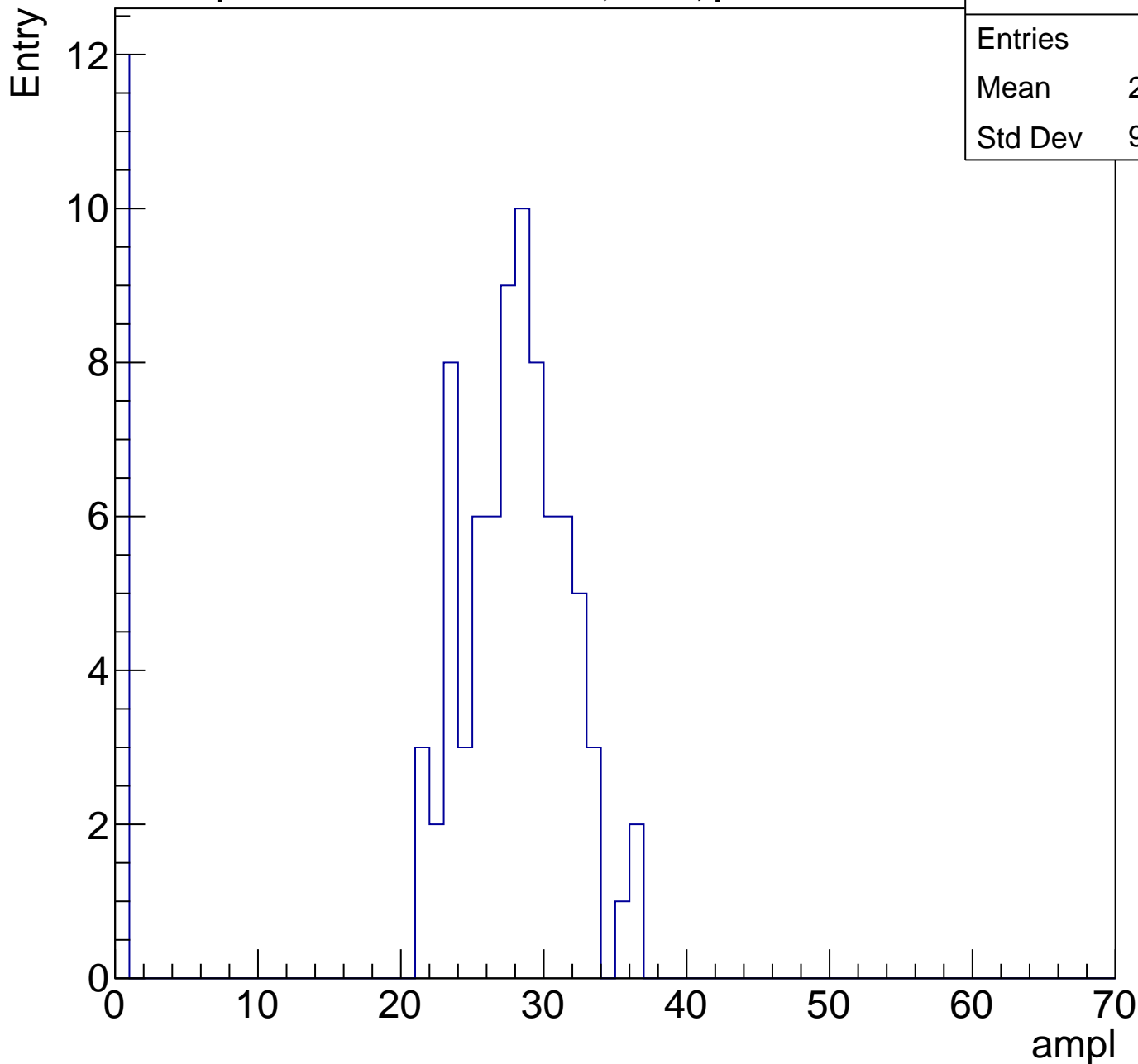
Entry



# B1L103S, U25-ch87, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

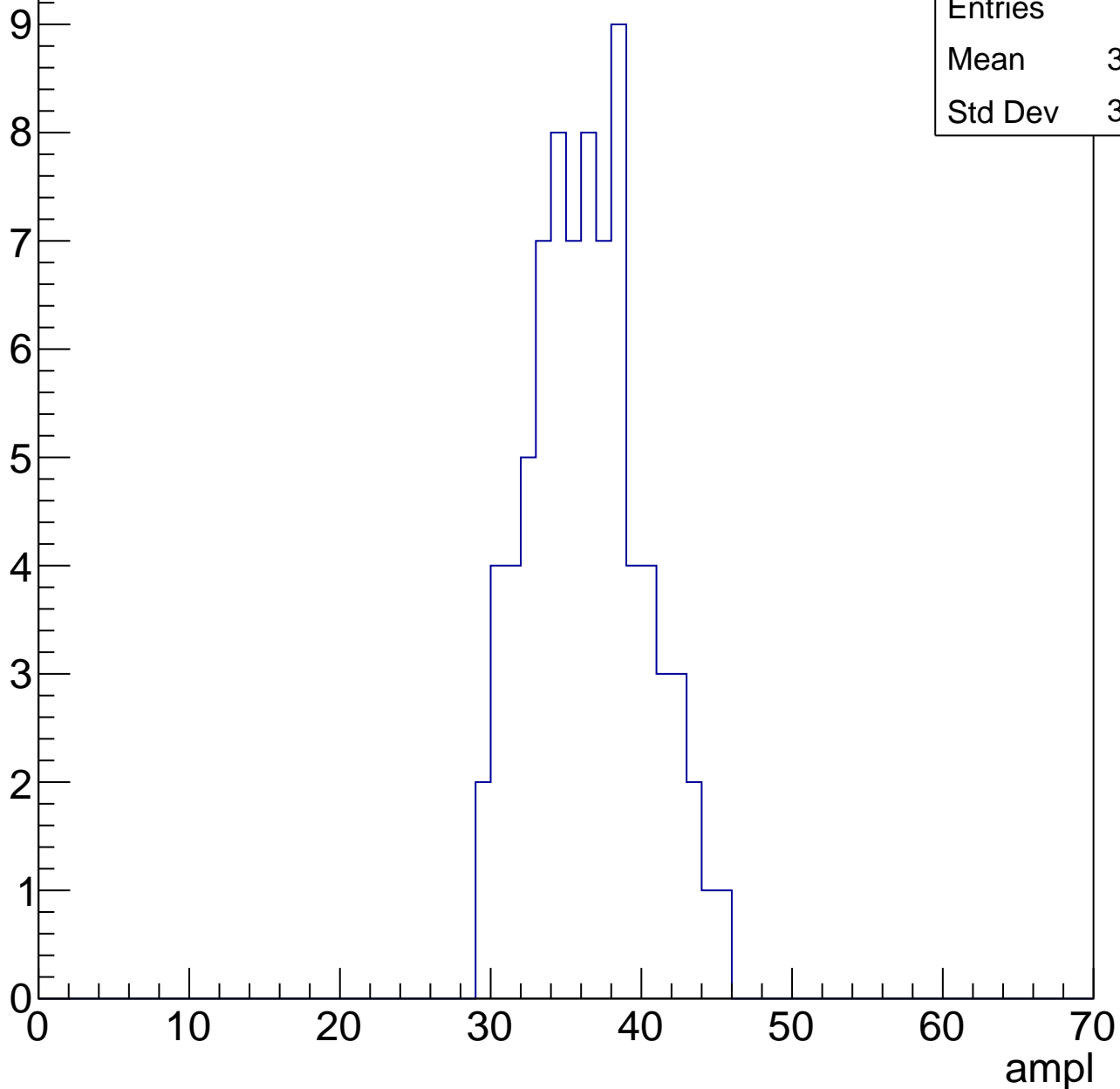
Entries	90
Mean	23.96
Std Dev	9.949



# B1L103S, U25-ch87, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

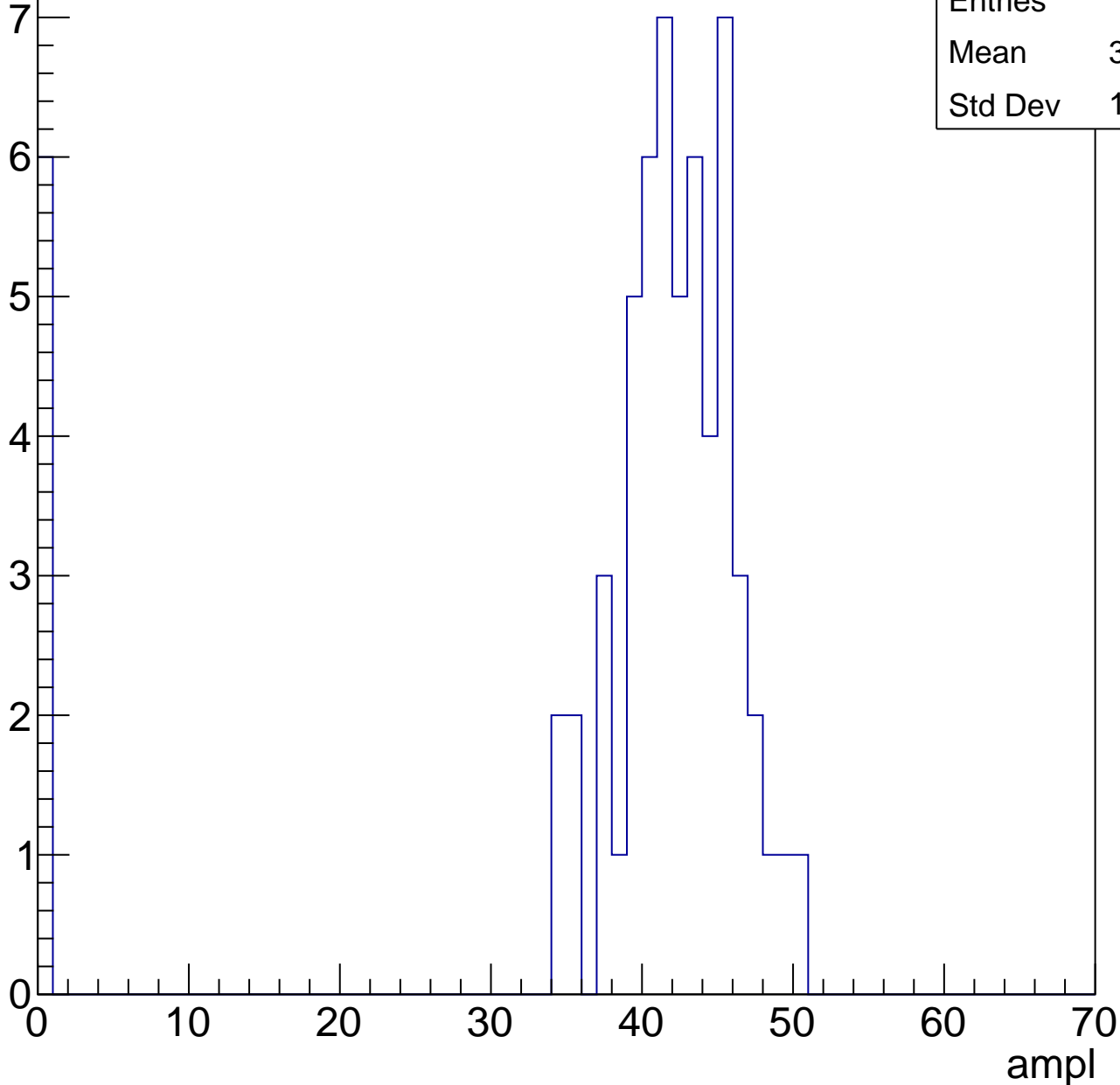


# B1L103S, U25-ch87, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	62
Mean	37.85
Std Dev	12.85

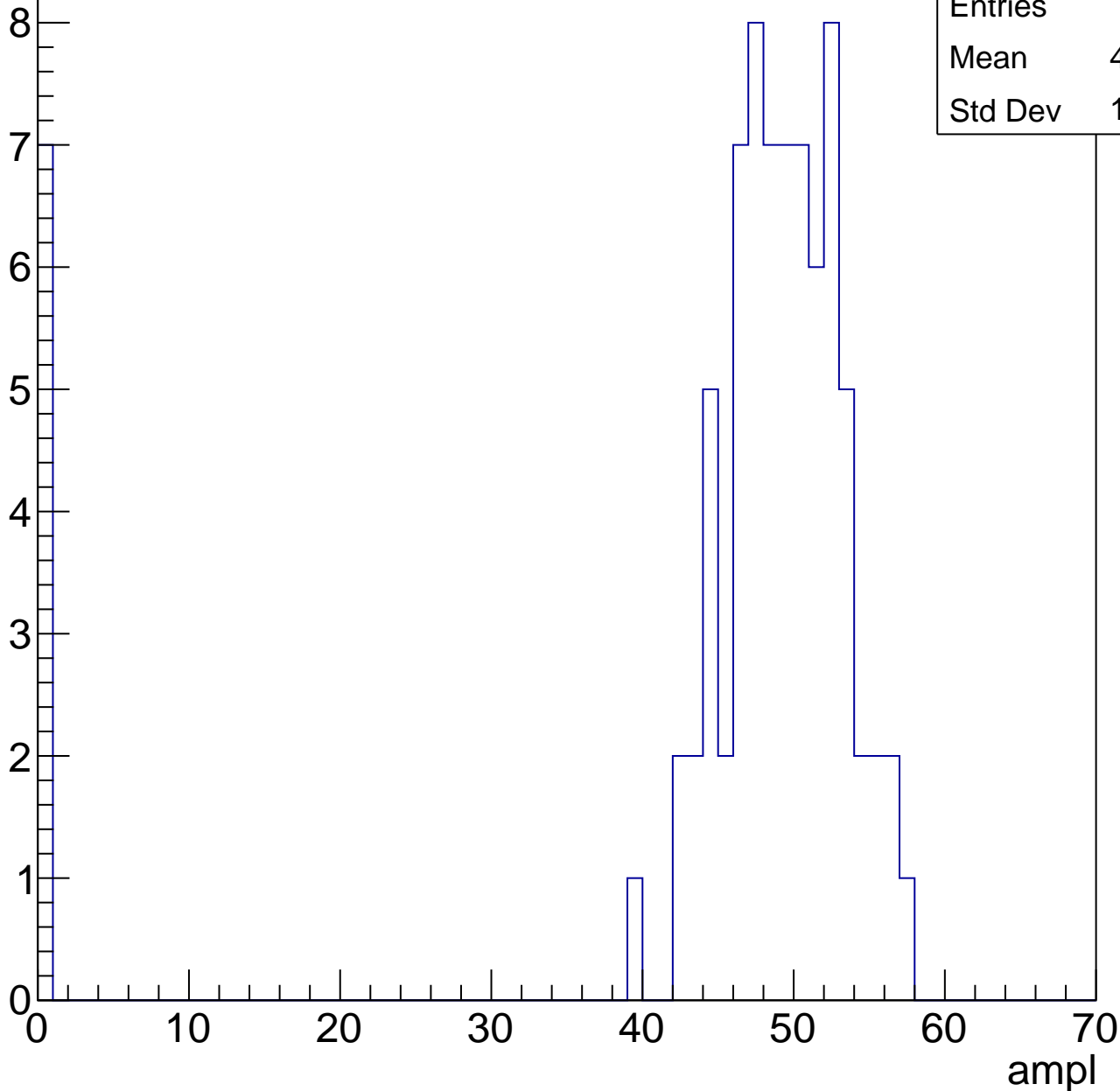


# B1L103S, U25-ch87, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	81
Mean	44.69
Std Dev	14.19

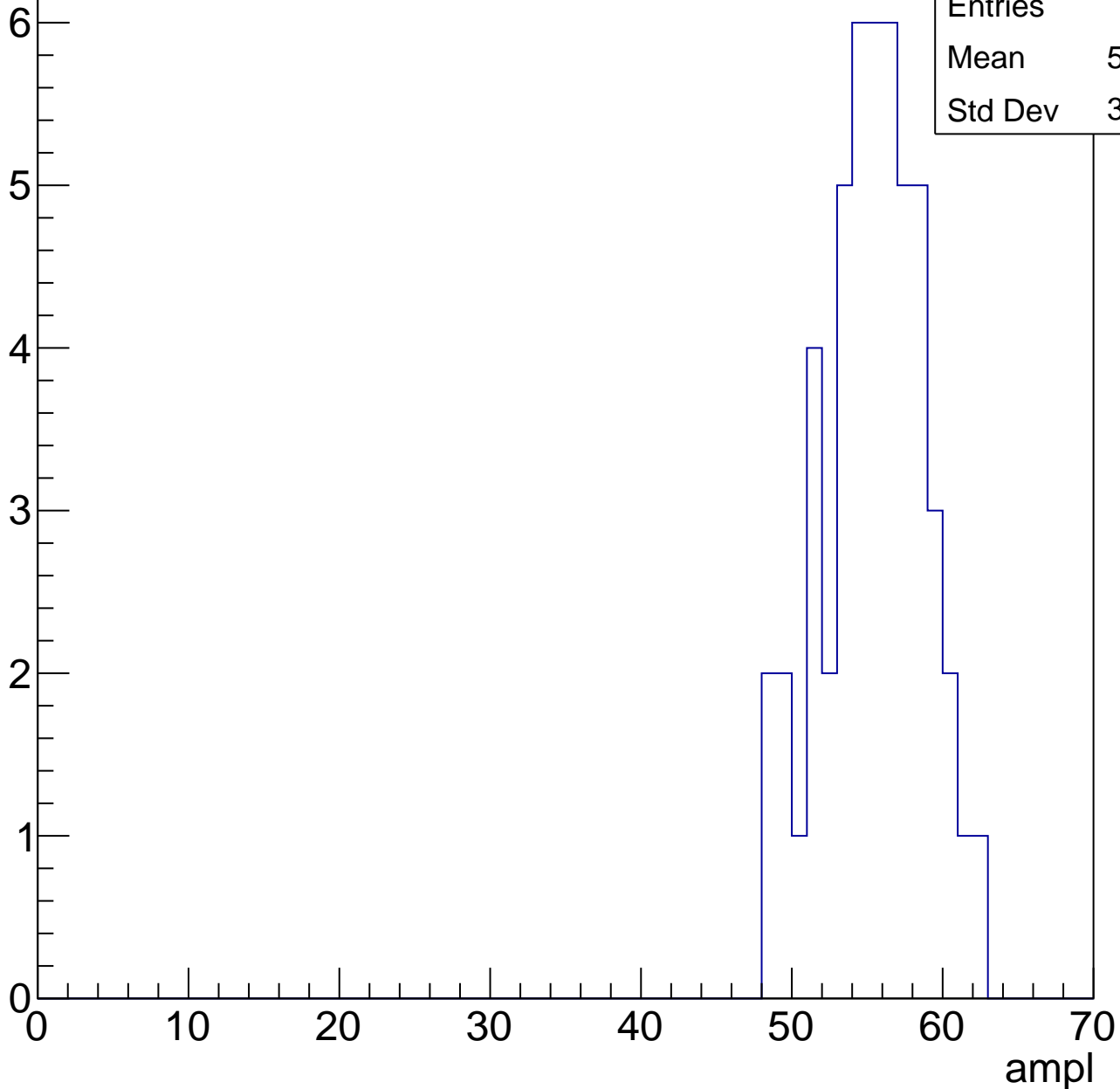


# B1L103S, U25-ch87, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	51
Mean	54.94
Std Dev	3.304

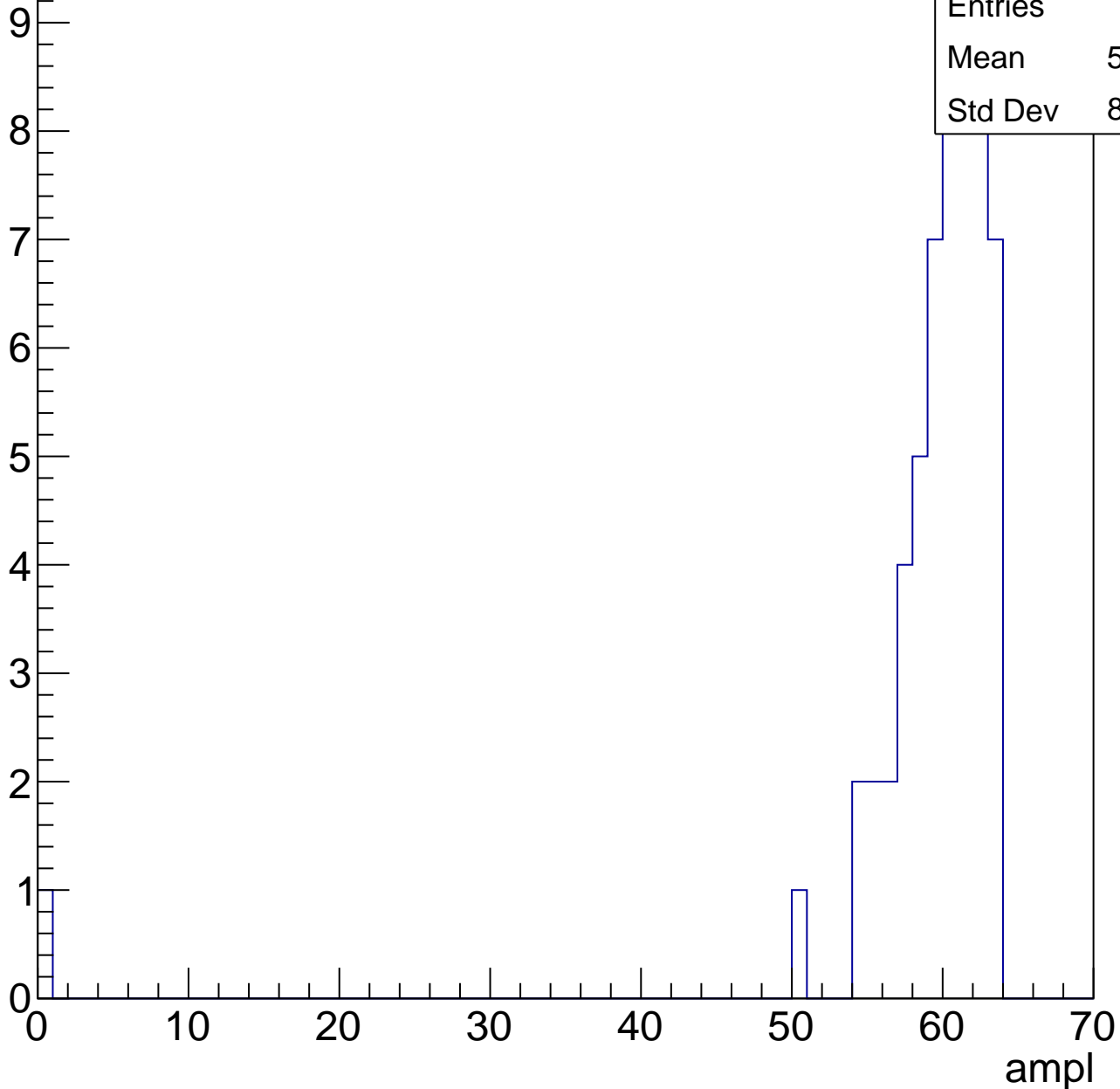


# B1L103S, U25-ch87, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	57
Mean	58.58
Std Dev	8.282



# B1L103S, U25-ch87, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U25-ch87, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U25-ch88, adc0

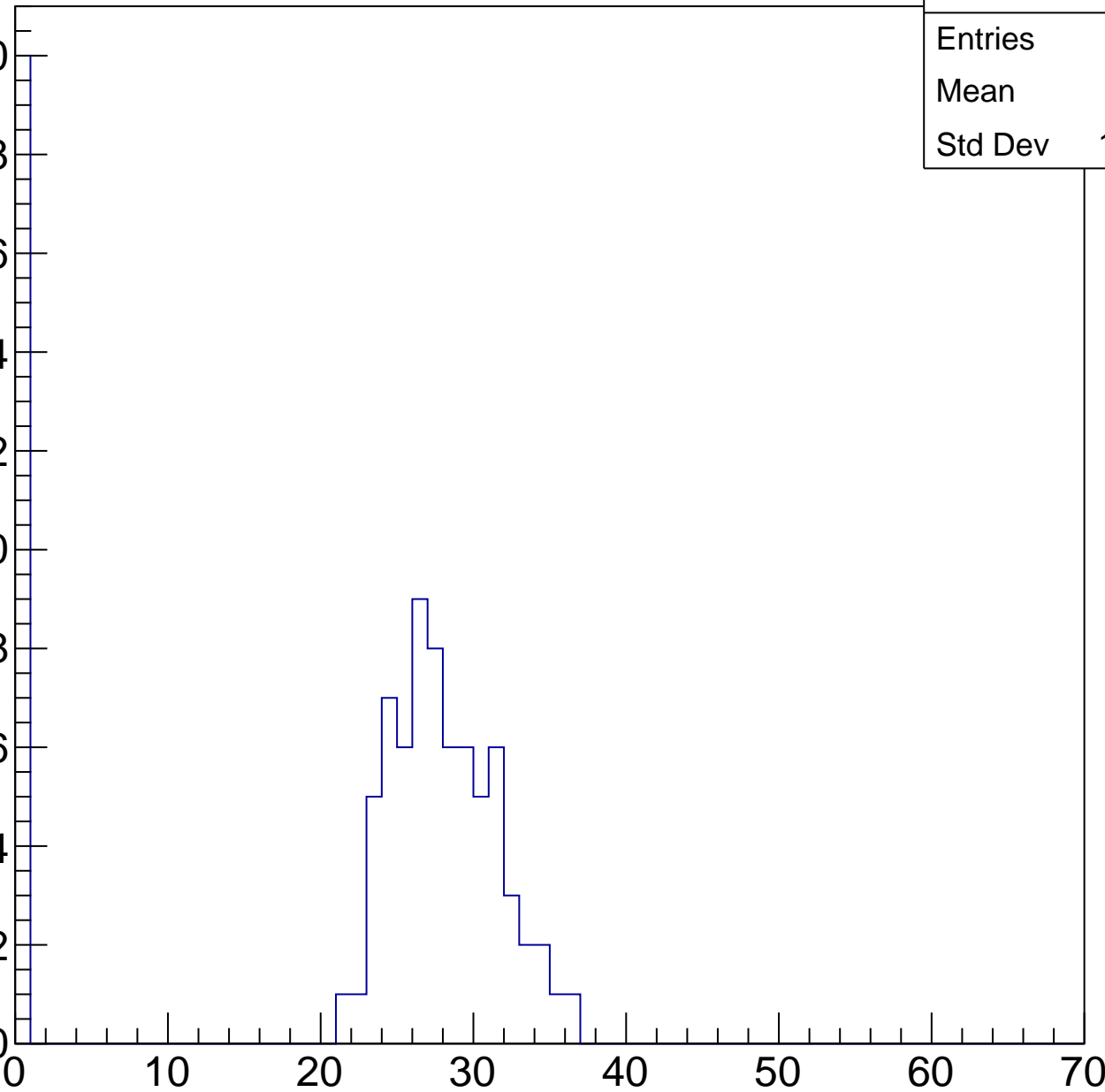
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	89
Mean	21.4
Std Dev	11.89

Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

ampl

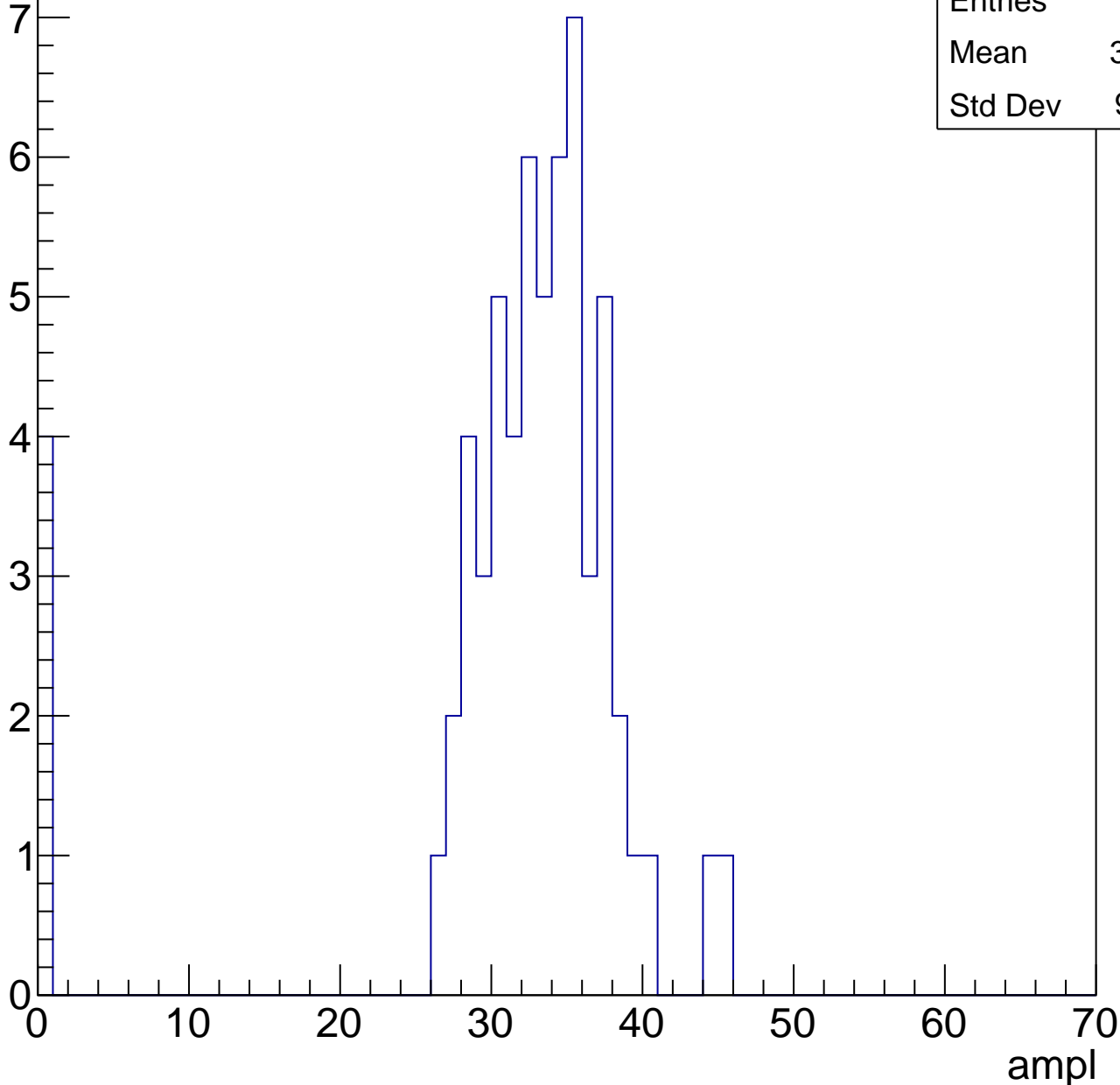


# B1L103S, U25-ch88, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	61
Mean	31.08
Std Dev	9.061

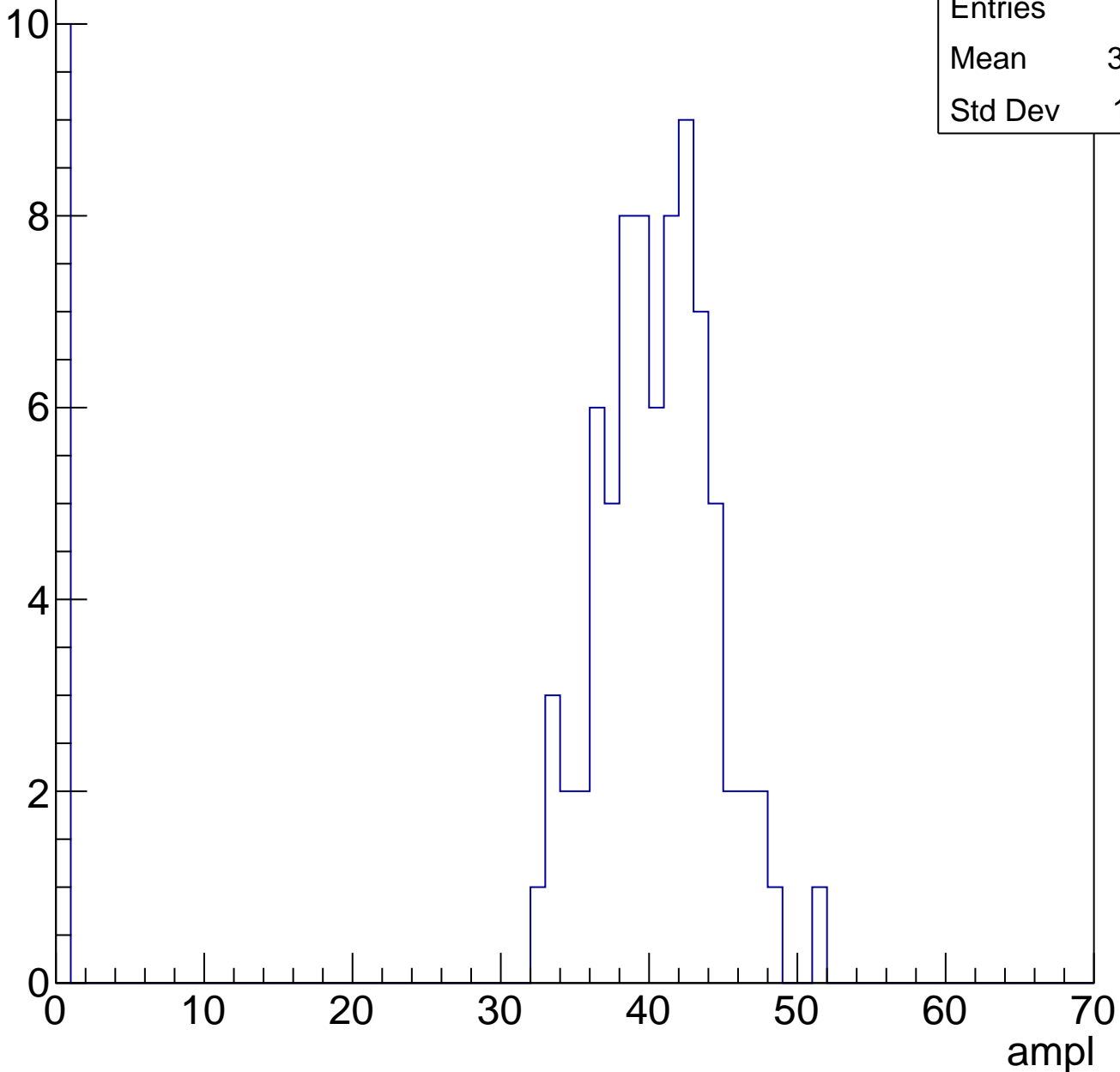


# B1L103S, U25-ch88, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	88
Mean	35.55
Std Dev	13.21

Entry

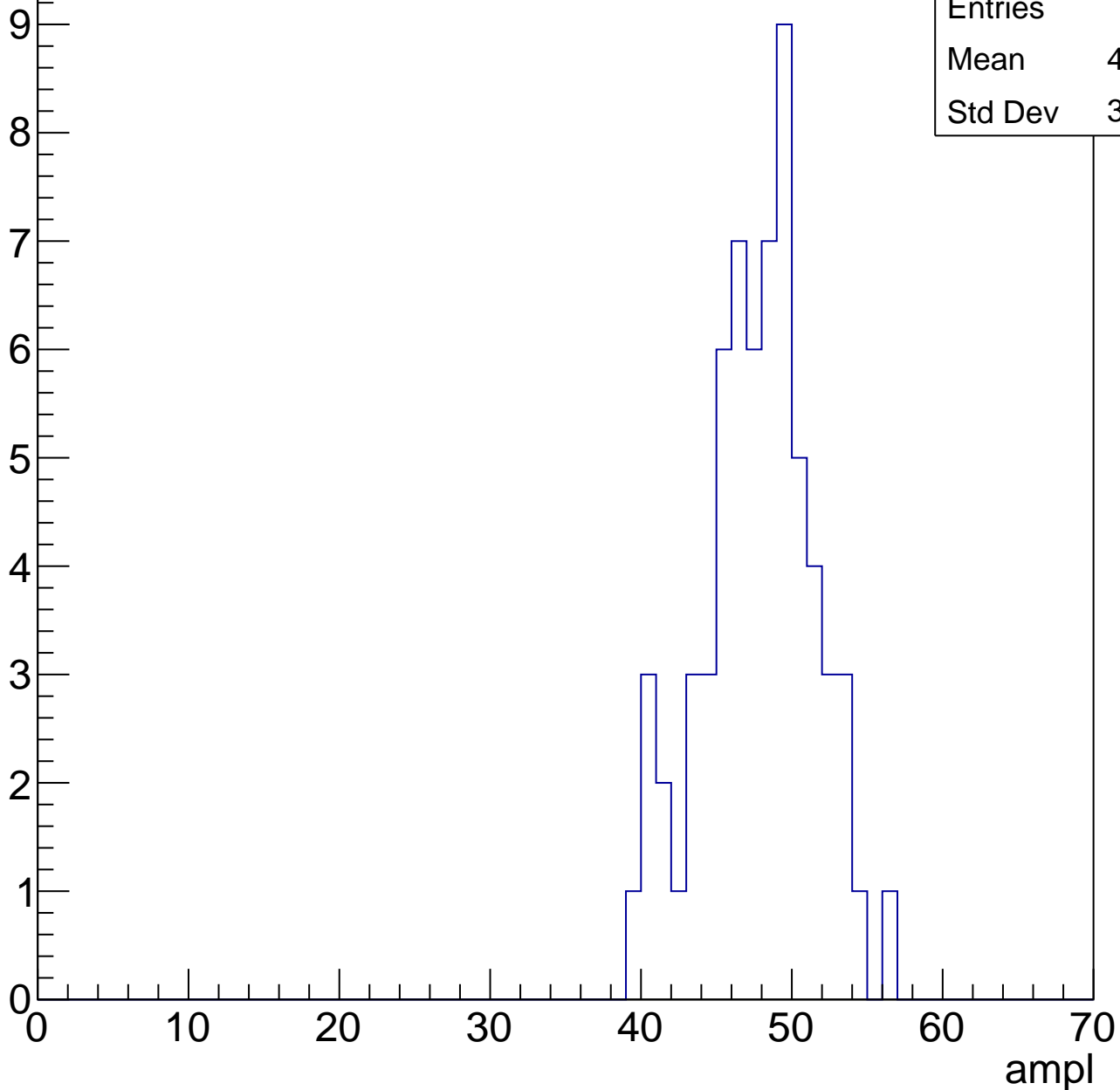


# B1L103S, U25-ch88, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	65
Mean	47.29
Std Dev	3.666

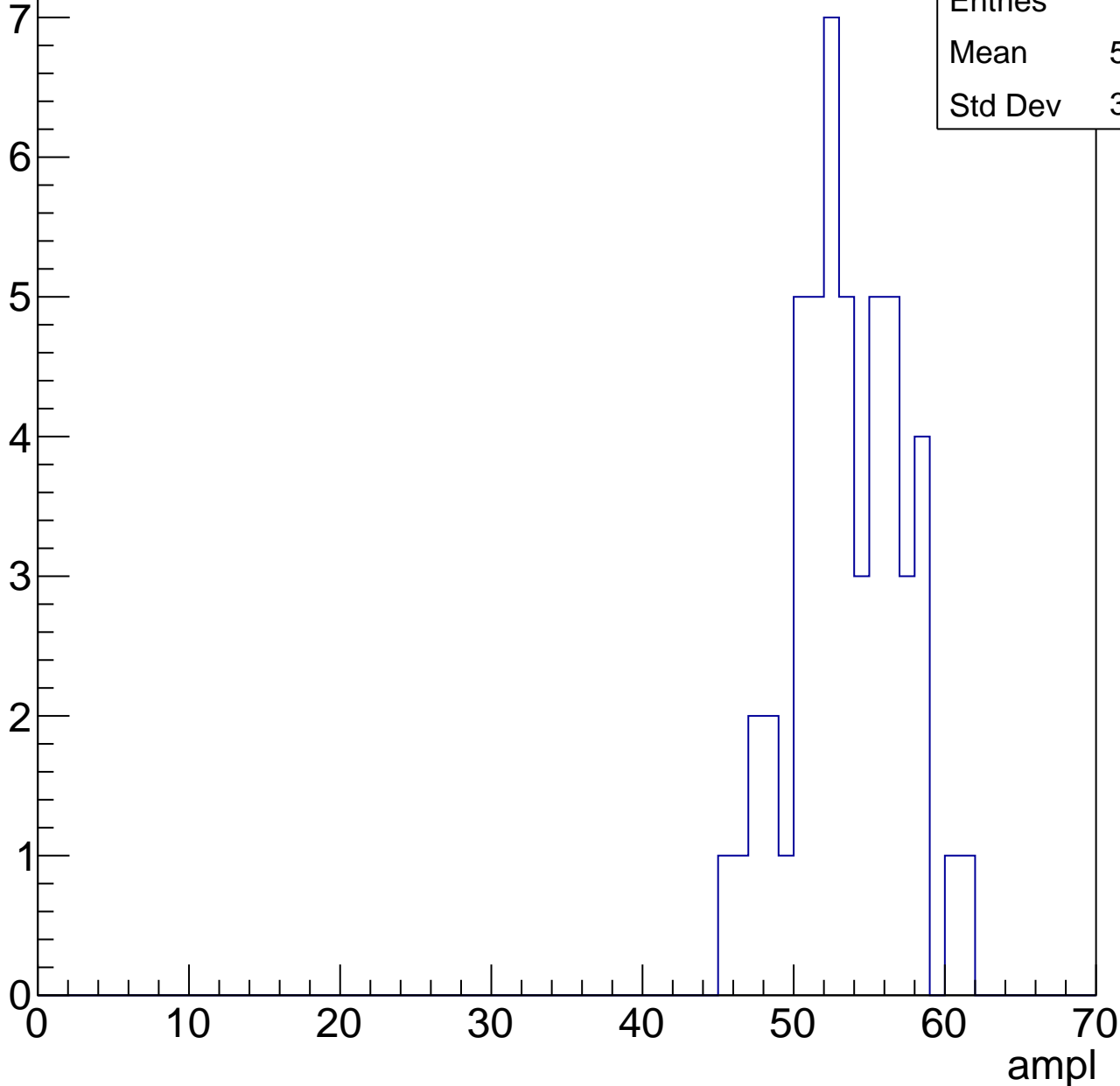


# B1L103S, U25-ch88, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

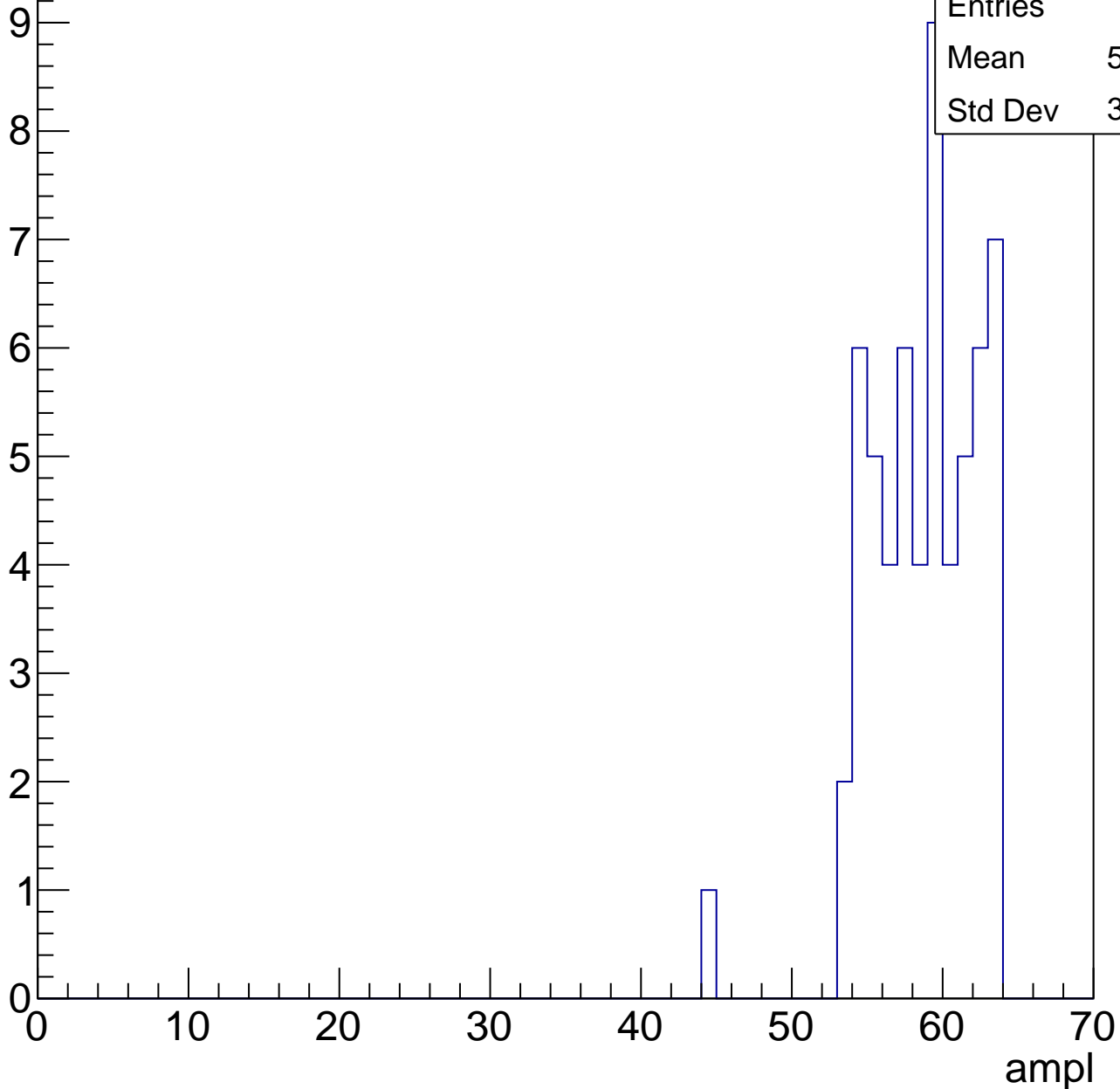
Entries	51
Mean	53.04
Std Dev	3.575



# B1L103S, U25-ch88, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

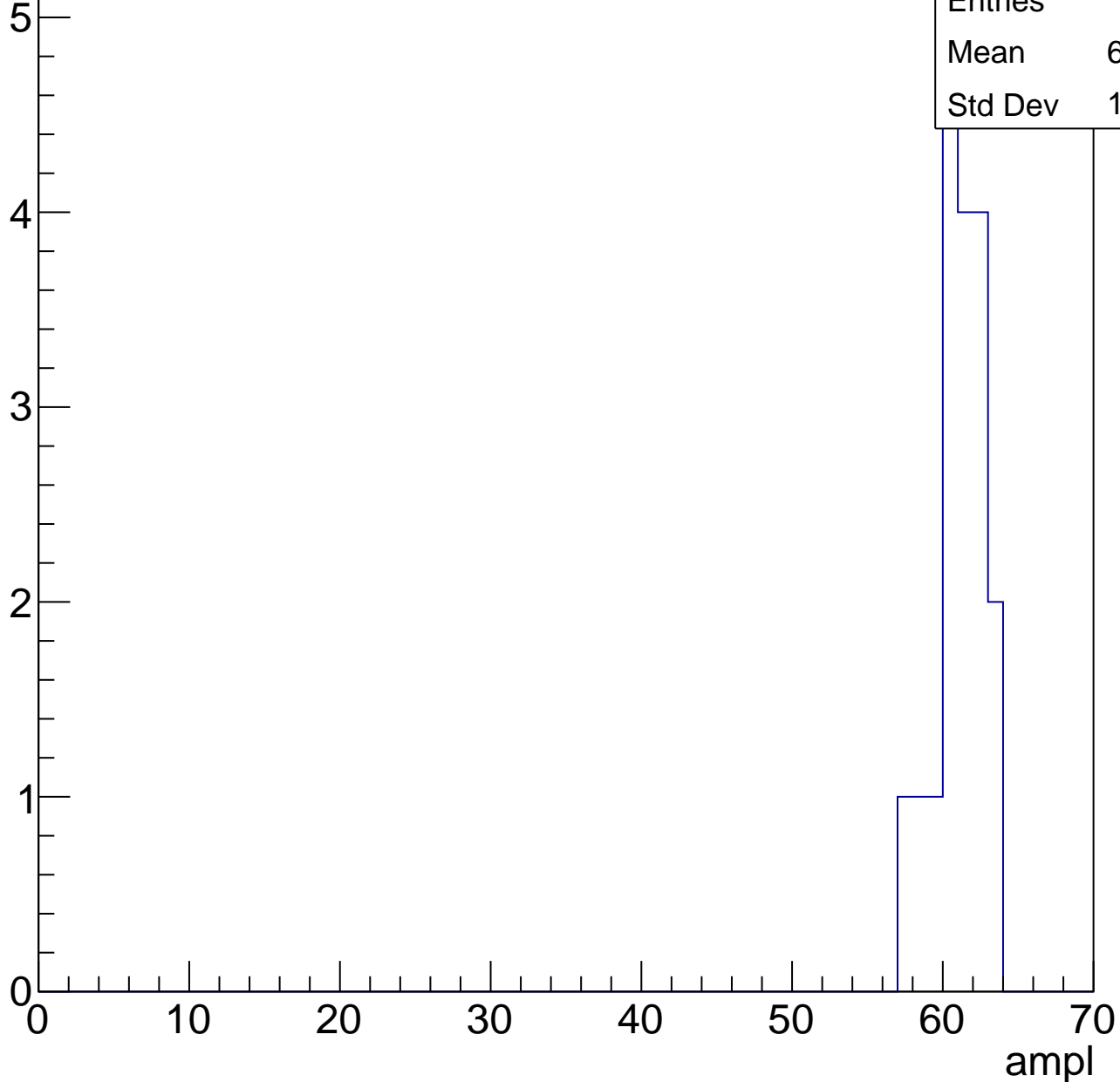
Entry



# B1L103S, U25-ch88, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	18
Mean	60.67
Std Dev	1.563

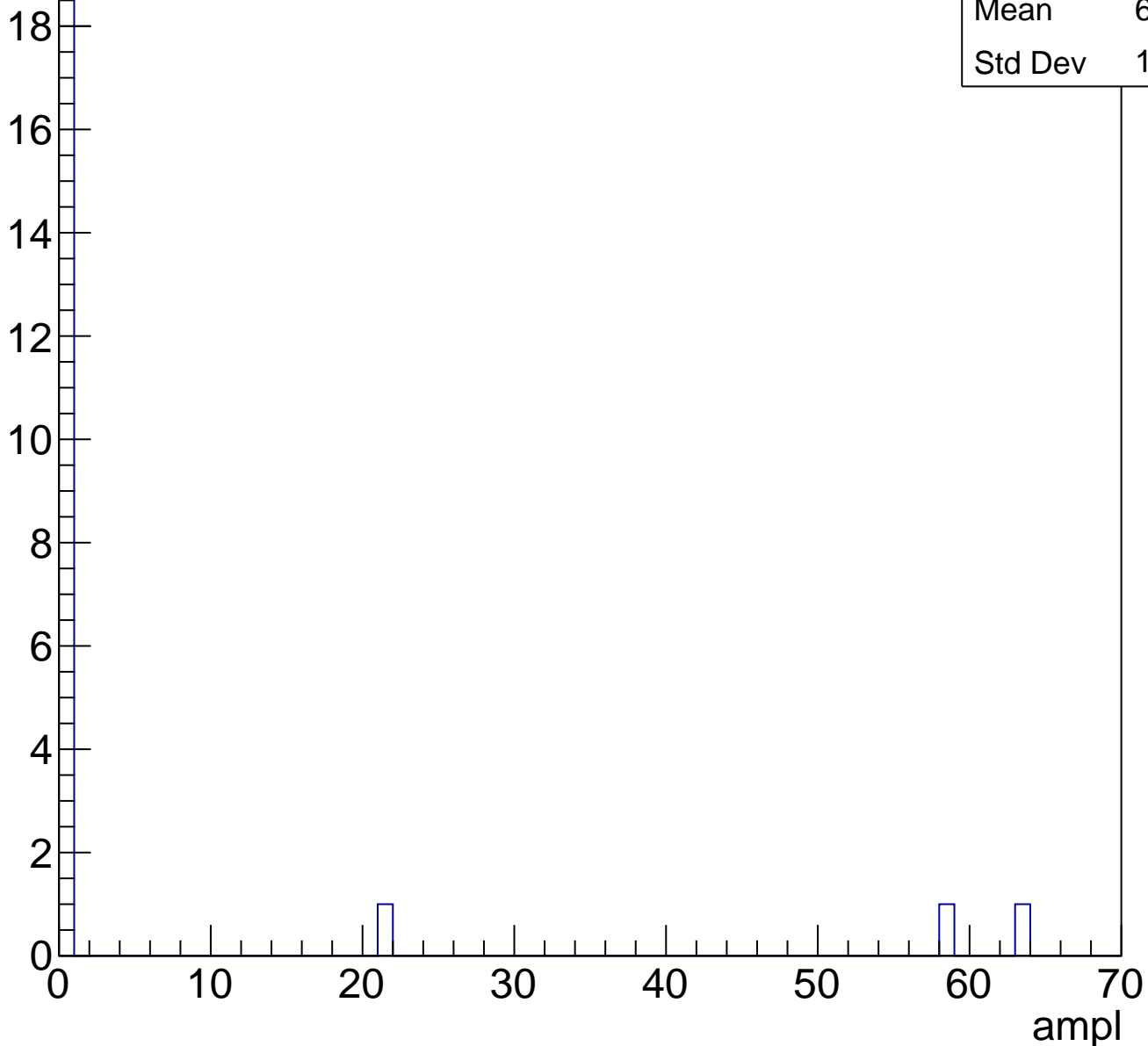


# B1L103S, U25-ch88, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	22
Mean	6.455
Std Dev	17.66

Entry

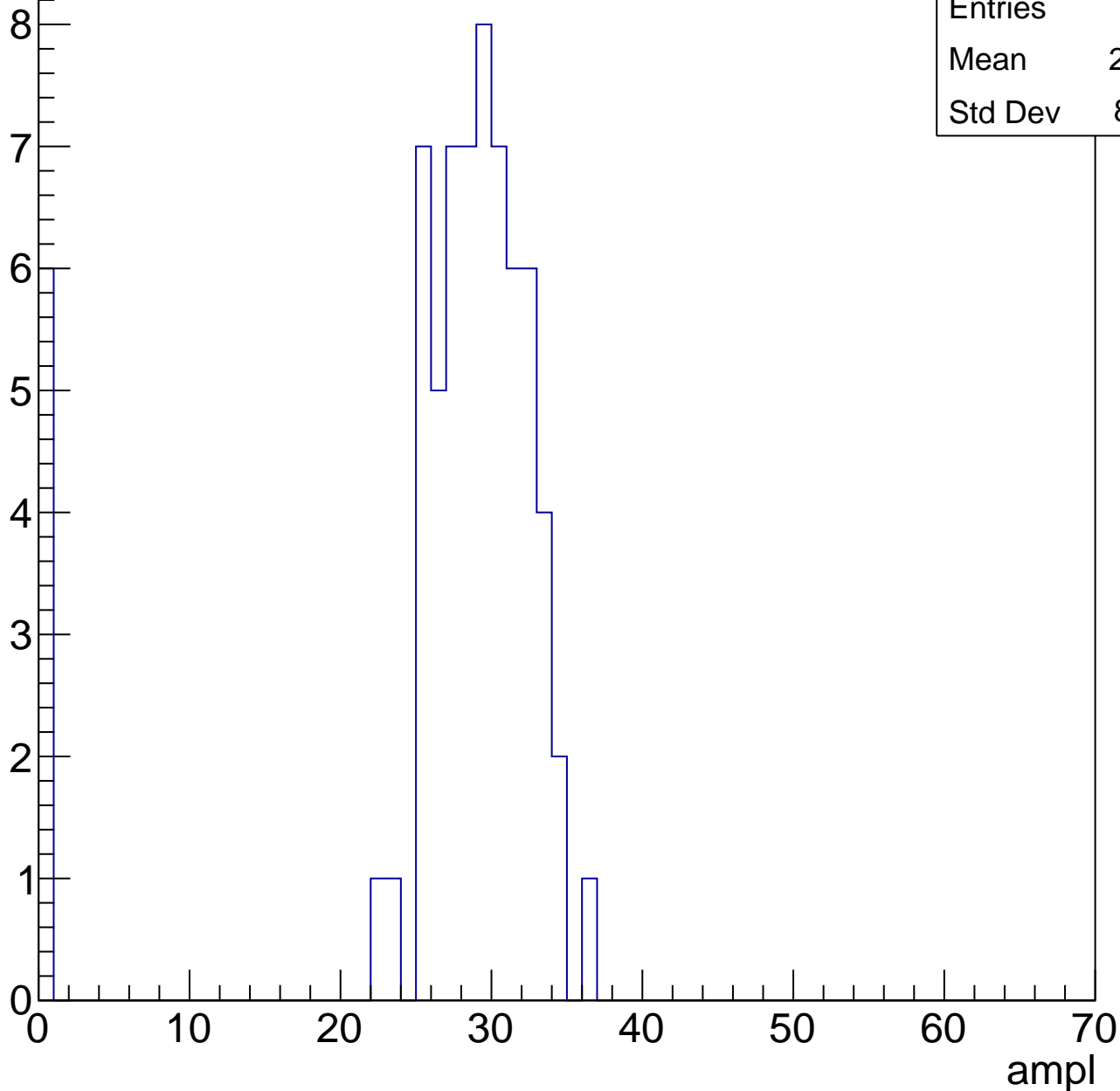


# B1L103S, U25-ch89, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	68
Mean	26.34
Std Dev	8.651

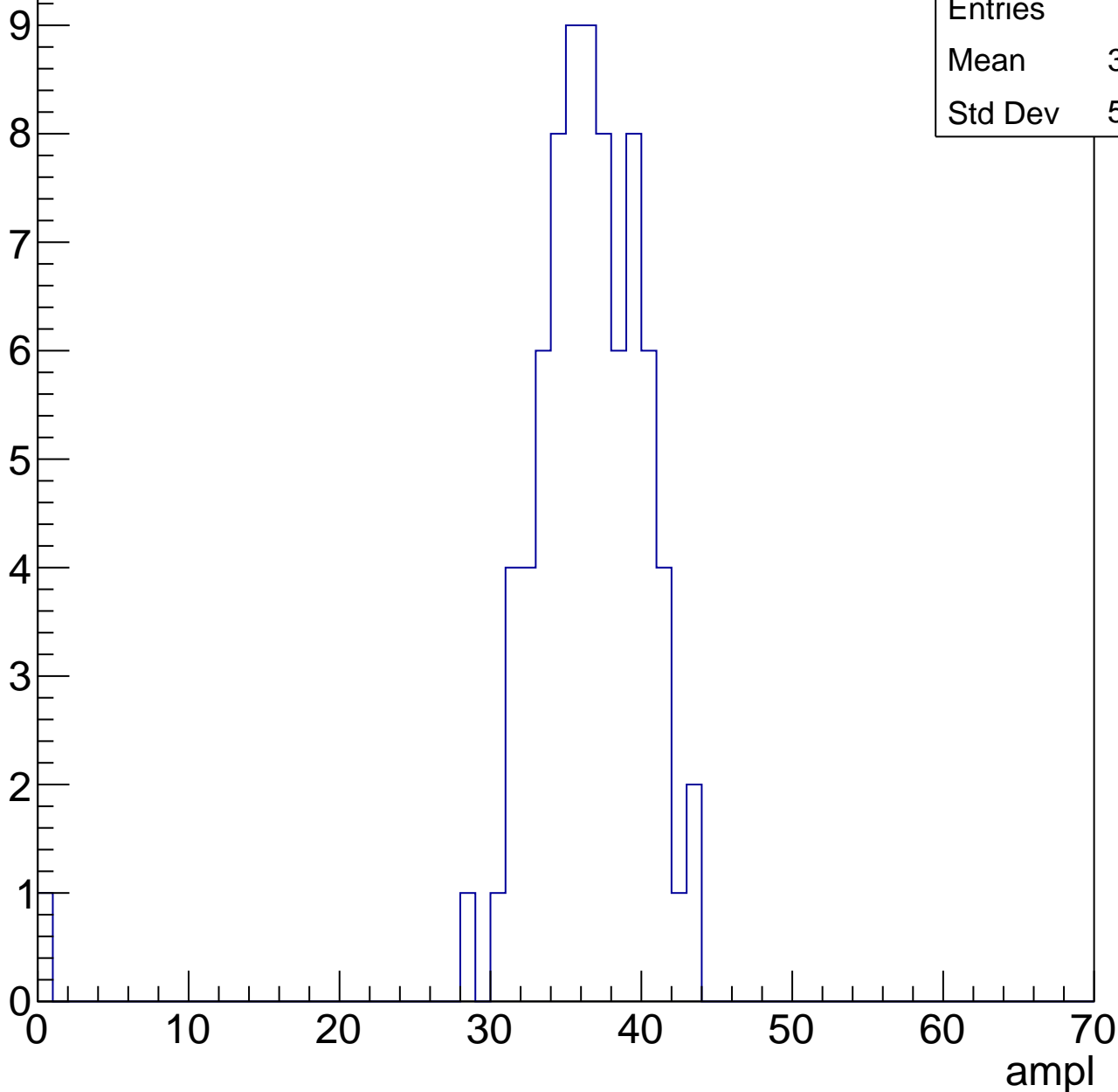


# B1L103S, U25-ch89, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	78
Mean	35.73
Std Dev	5.168

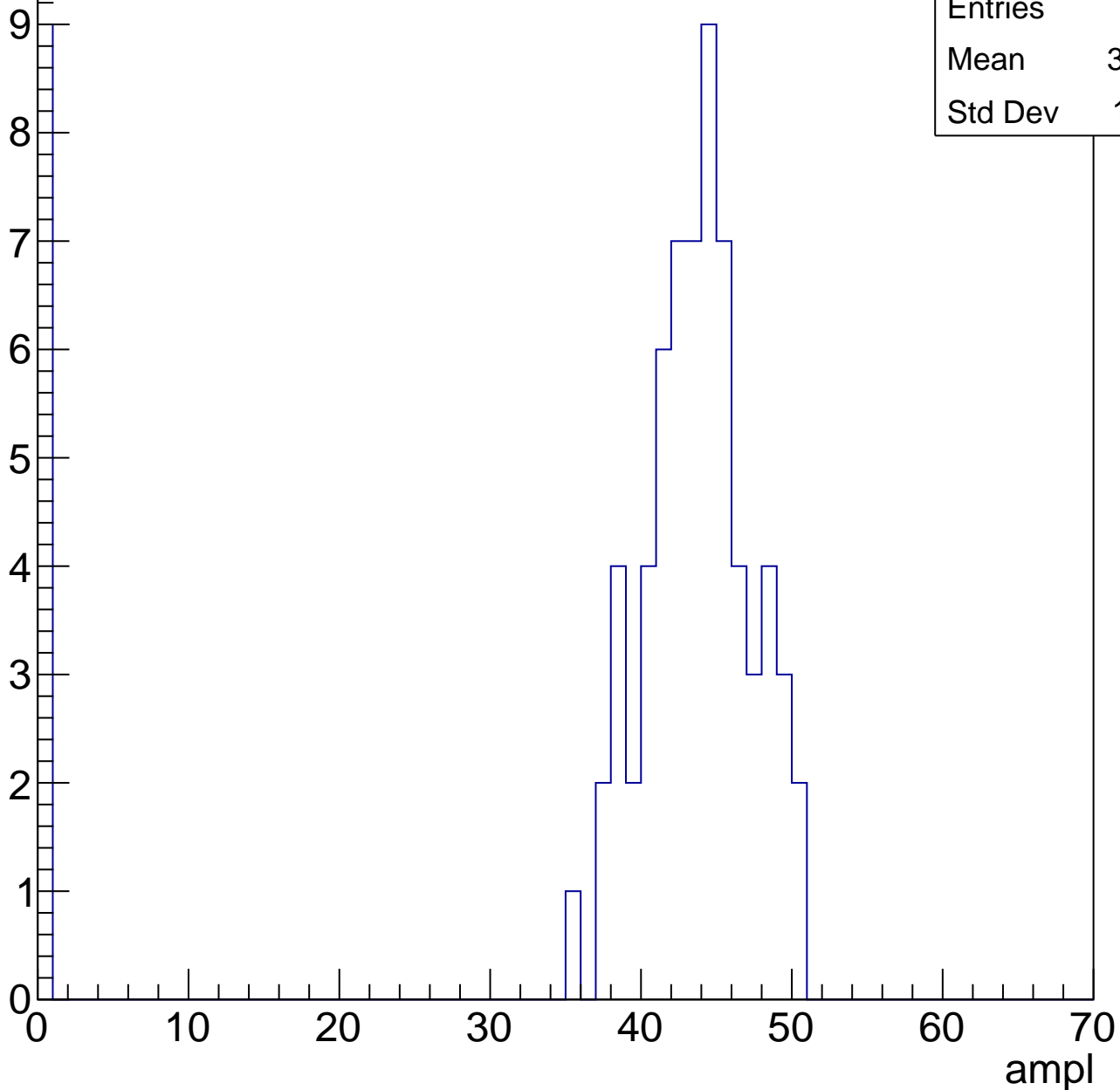


# B1L103S, U25-ch89, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	74
Mean	38.04
Std Dev	14.51

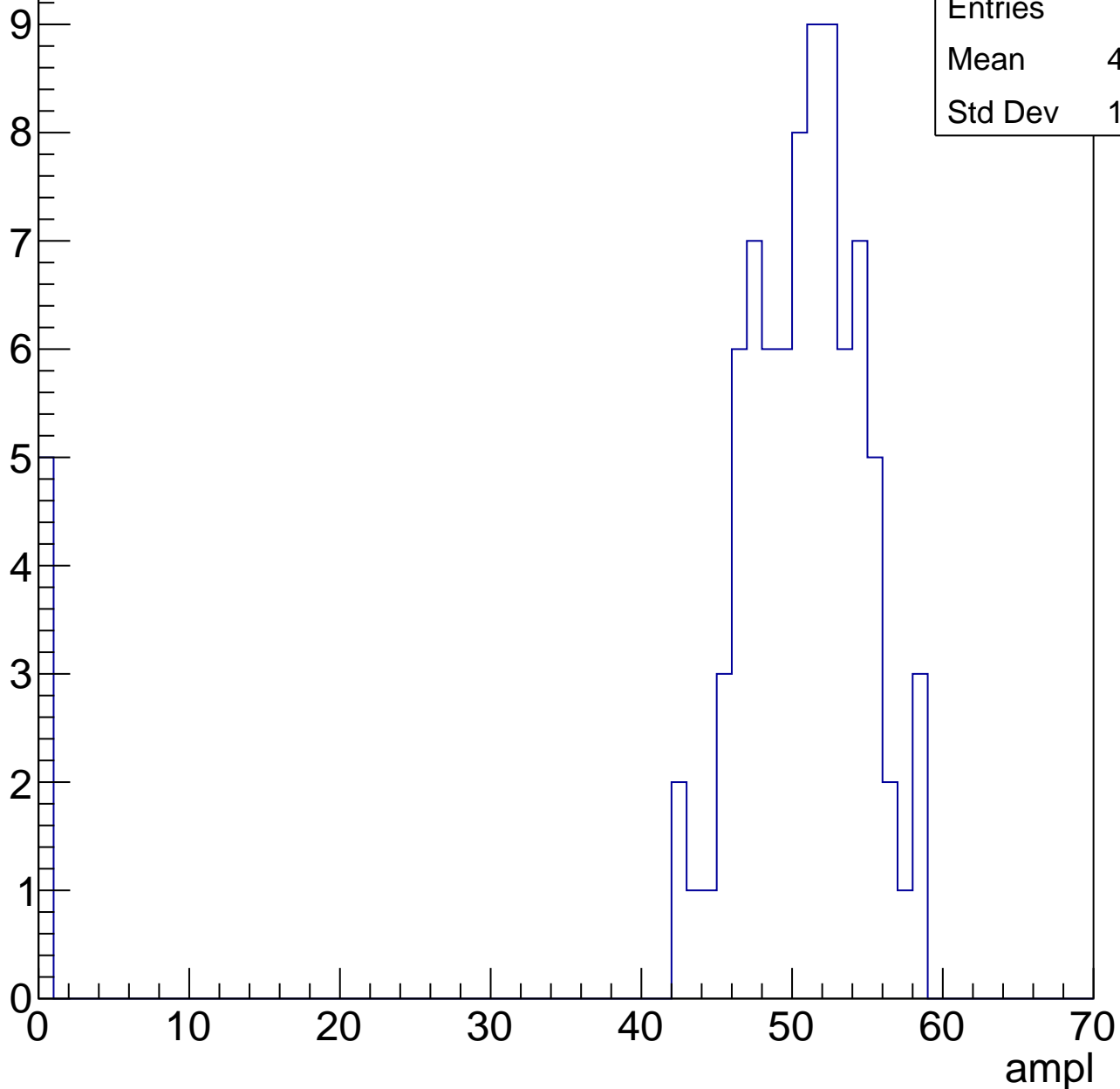


# B1L103S, U25-ch89, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	87
Mean	47.52
Std Dev	12.27

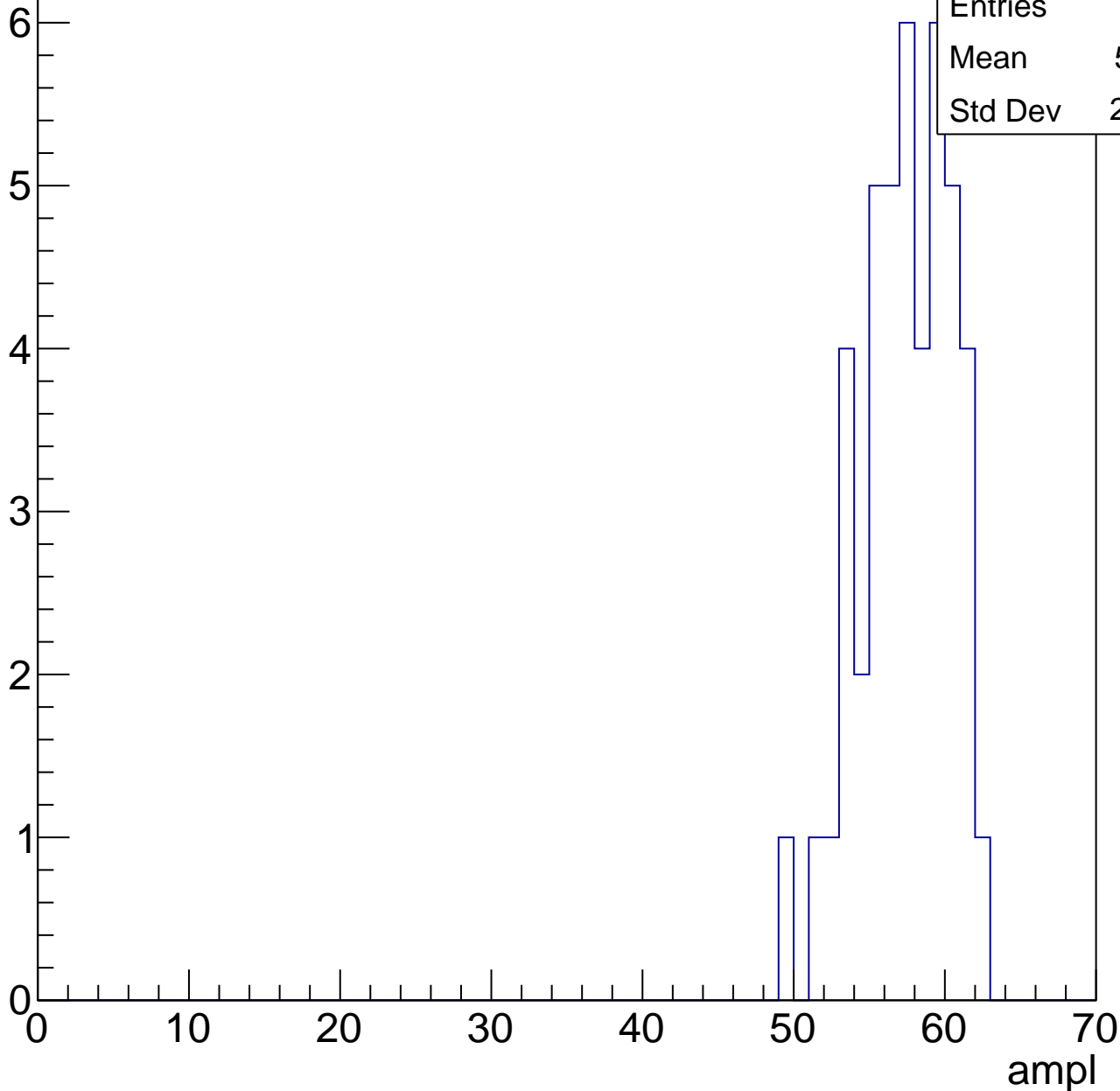


# B1L103S, U25-ch89, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	45
Mean	56.91
Std Dev	2.958

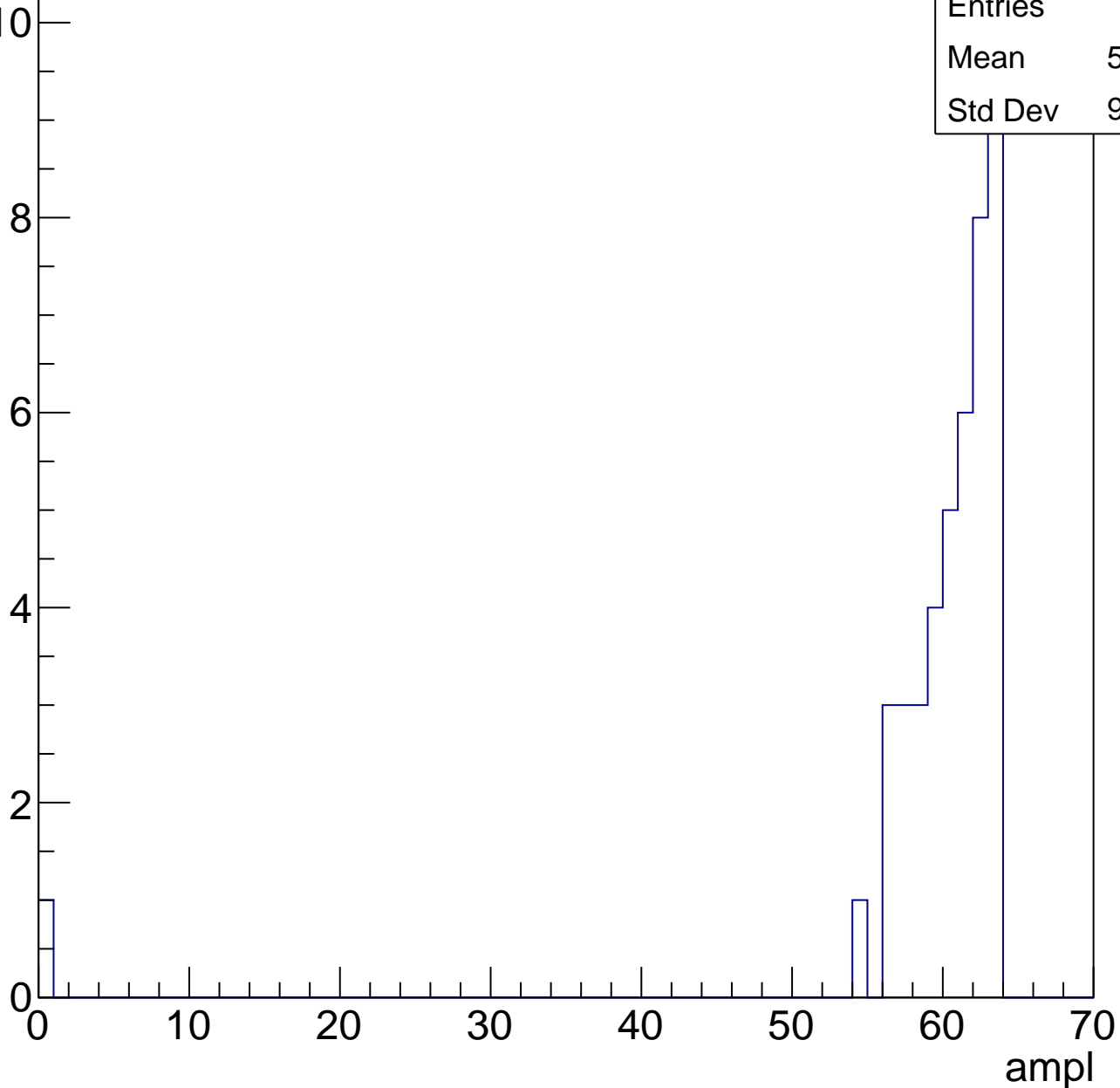


# B1L103S, U25-ch89, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	44
Mean	58.98
Std Dev	9.304



# B1L103S, U25-ch89, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U25-ch89, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

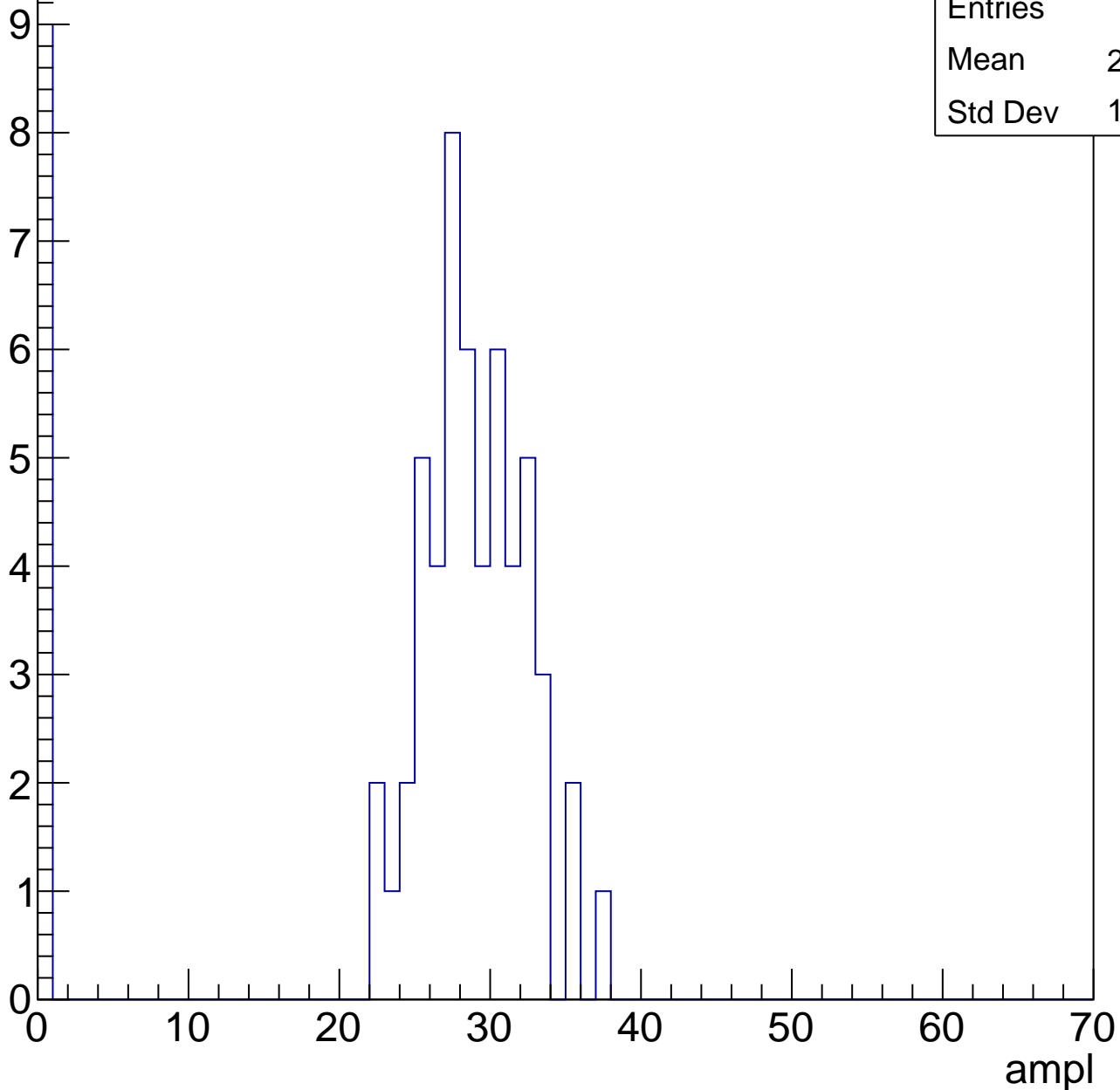
Entries	19
Mean	0
Std Dev	0

# B1L103S, U25-ch90, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	62
Mean	24.42
Std Dev	10.52

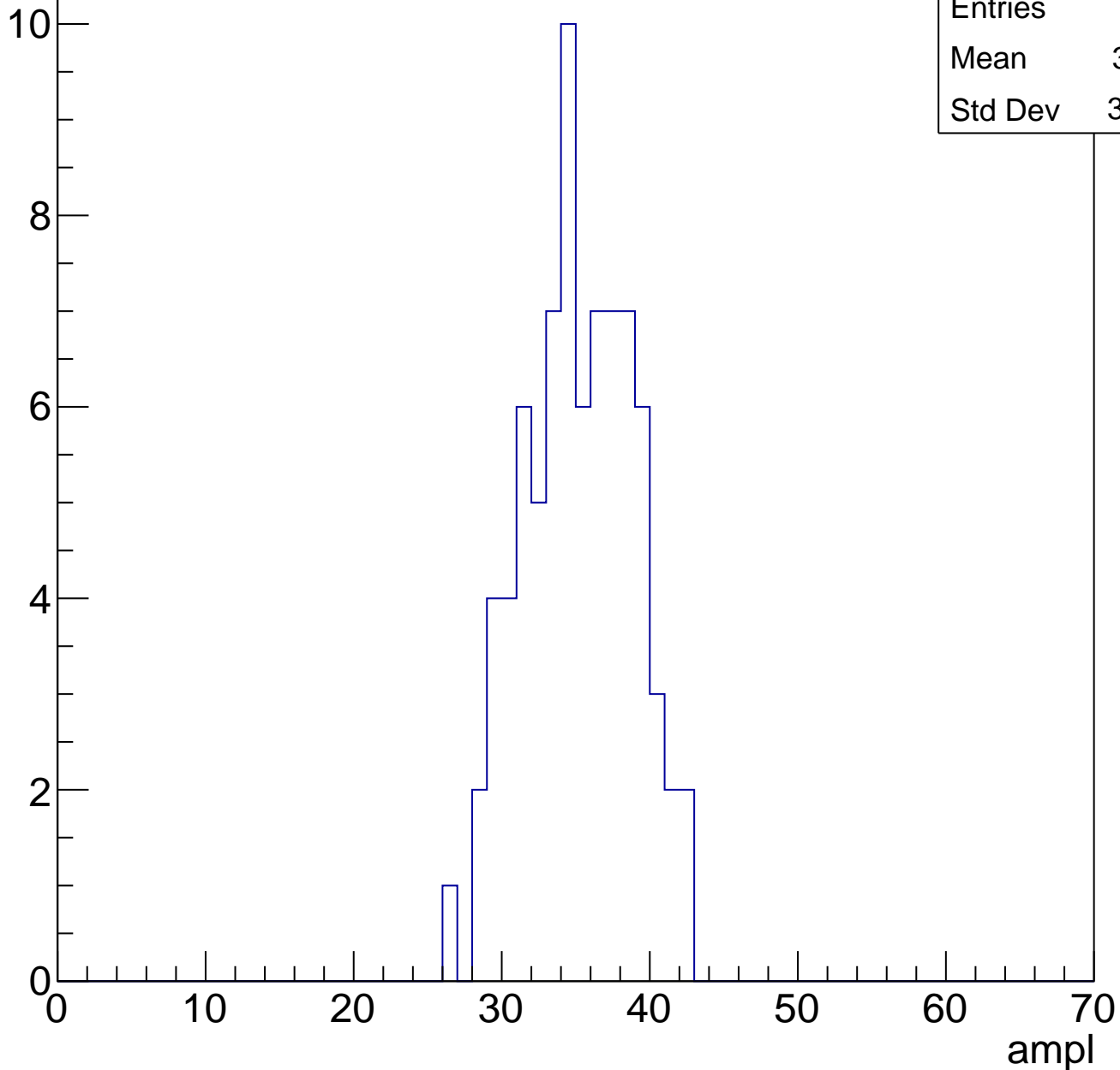


# B1L103S, U25-ch90, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	79
Mean	34.71
Std Dev	3.618

Entry

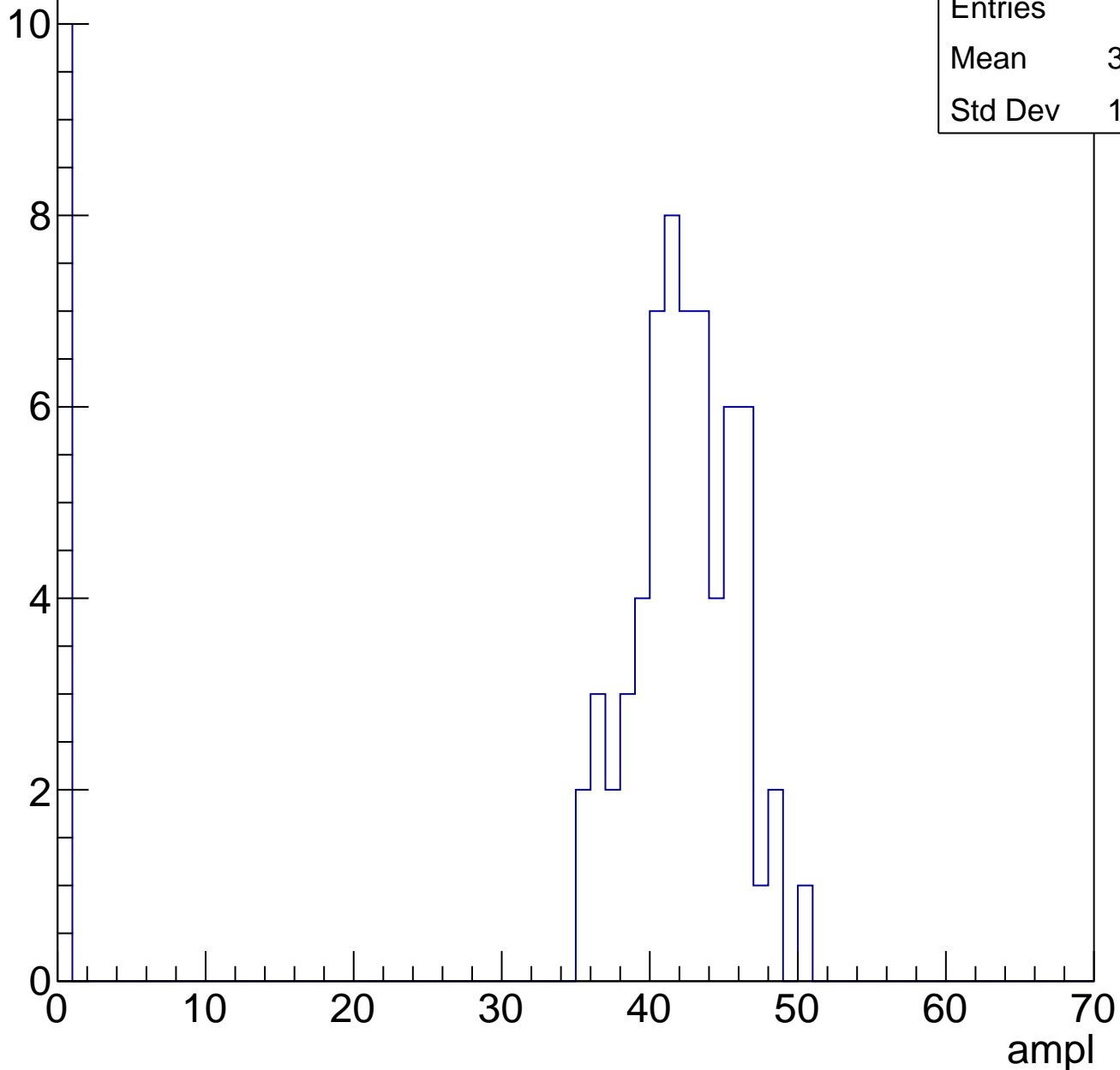


# B1L103S, U25-ch90, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	73
Mean	36.16
Std Dev	14.74

Entry

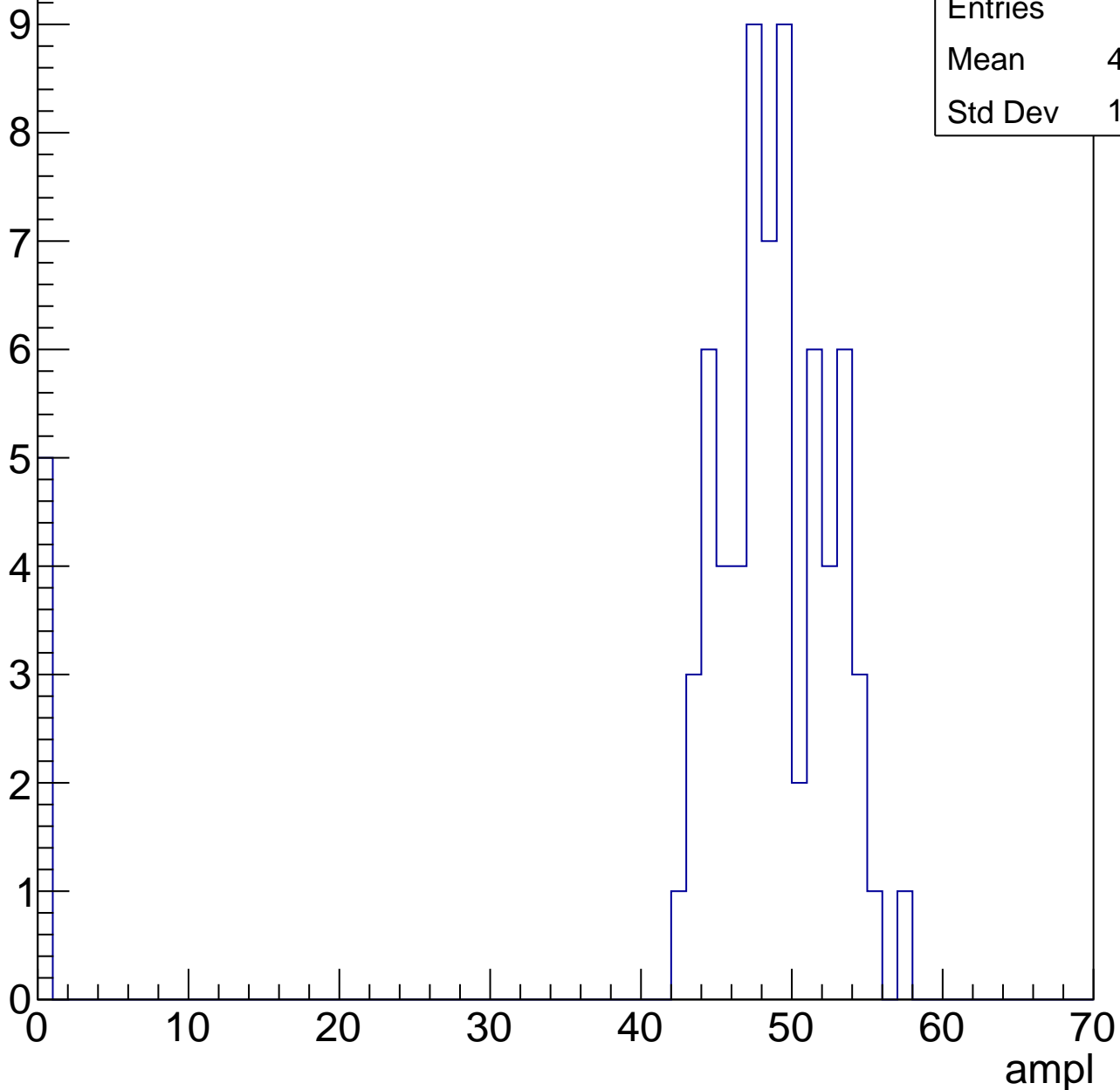


# B1L103S, U25-ch90, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	71
Mean	45.14
Std Dev	12.85

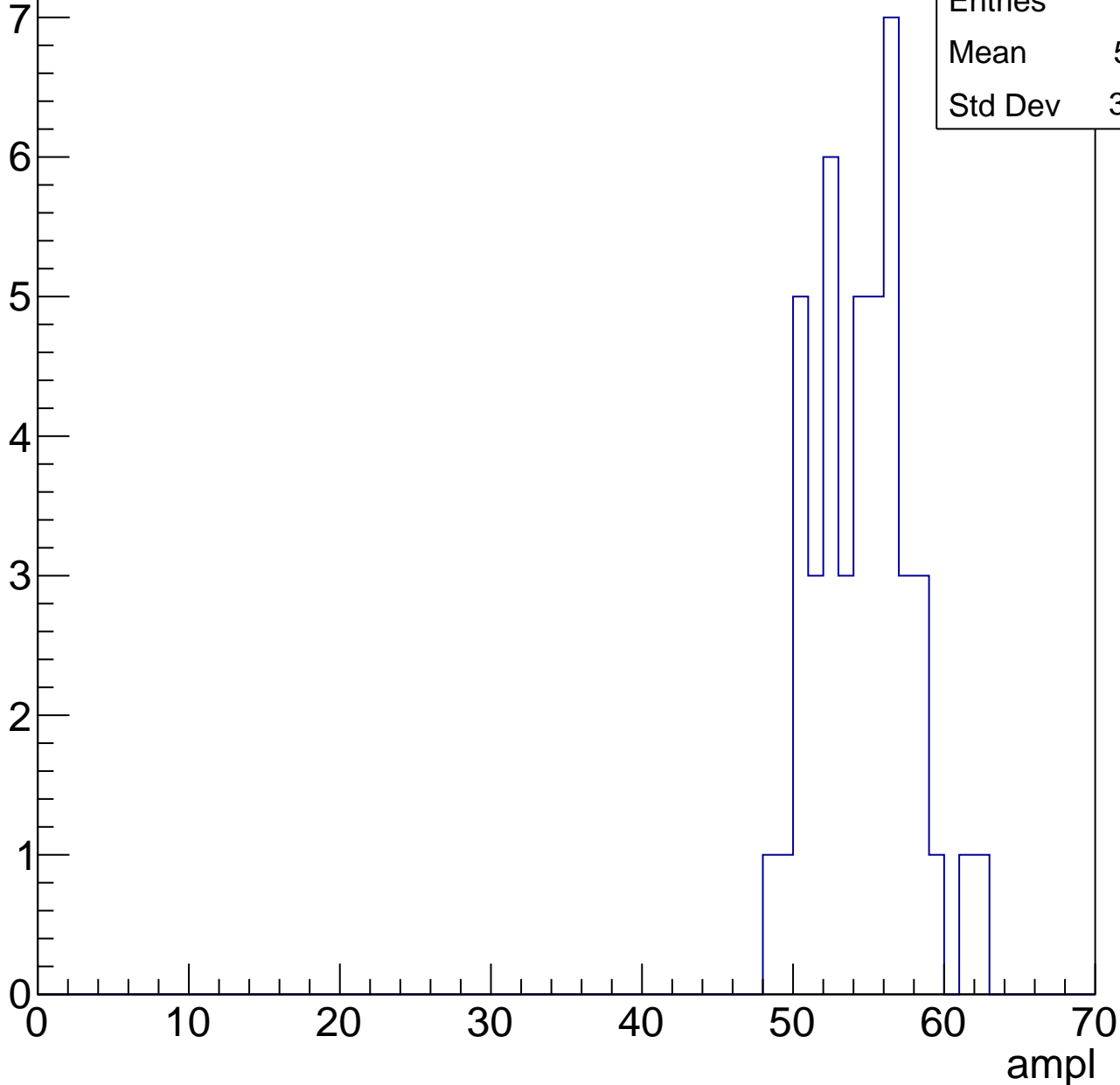


# B1L103S, U25-ch90, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	45
Mean	54.11
Std Dev	3.129

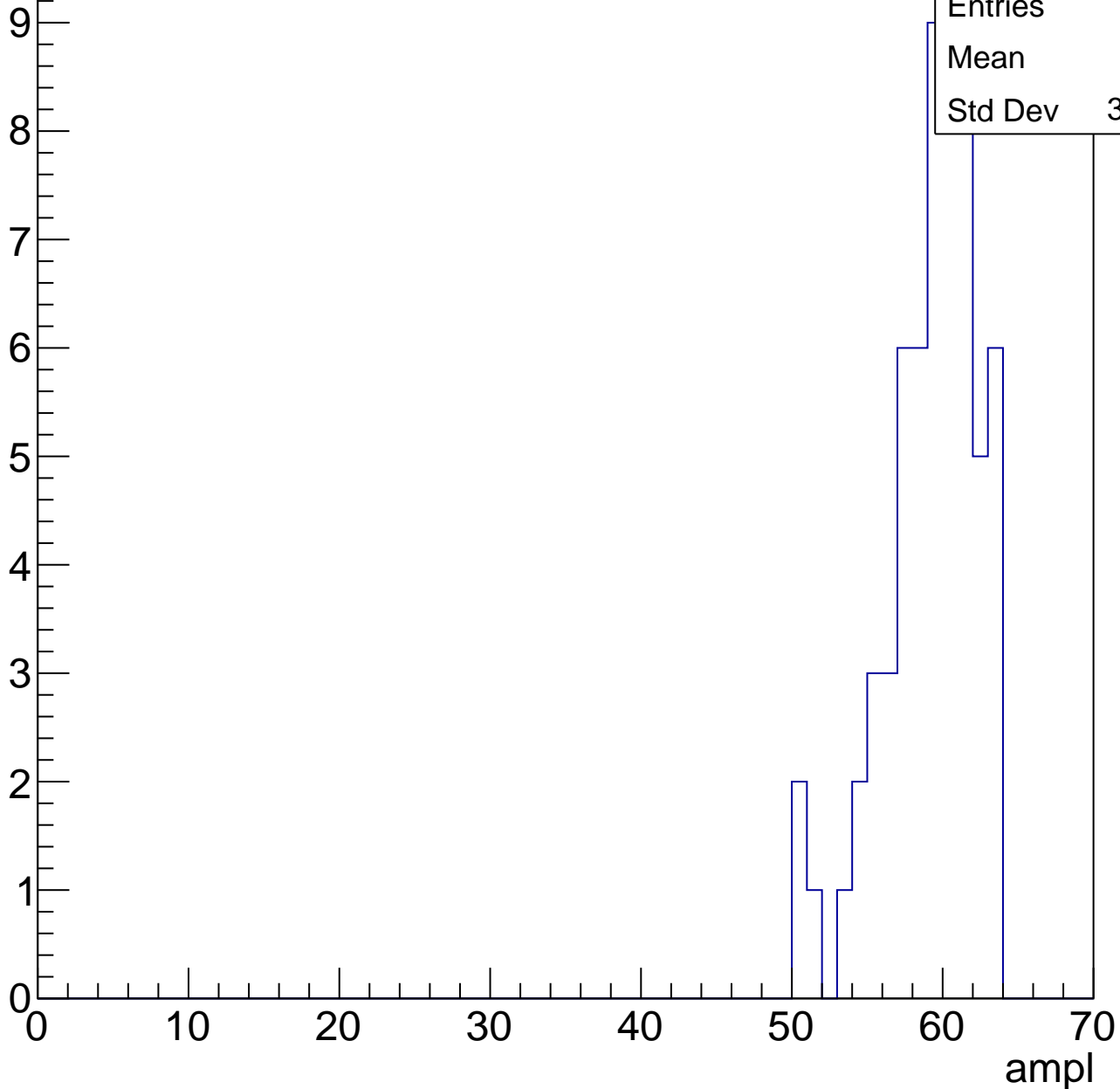


# B1L103S, U25-ch90, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

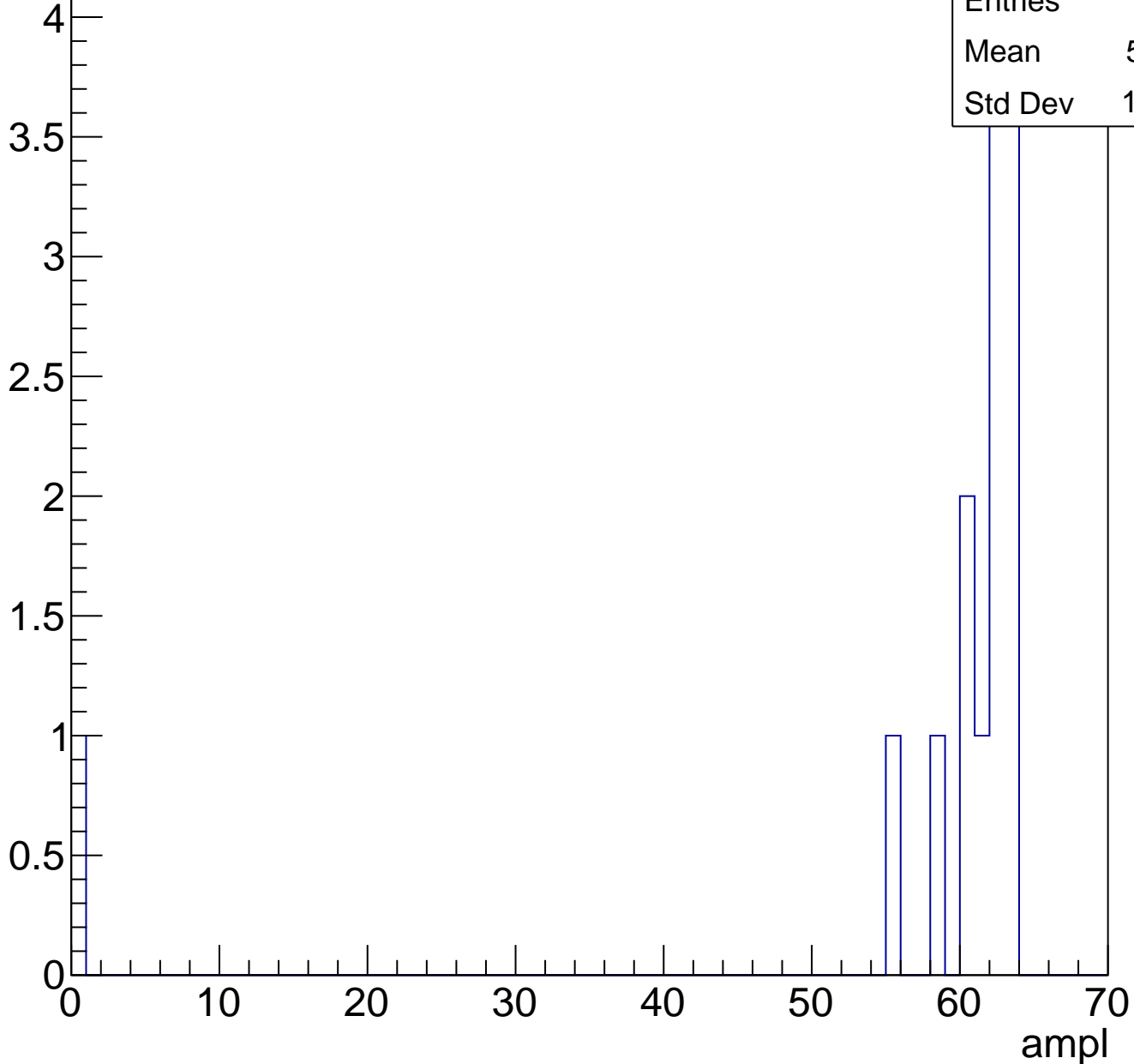
Entries	60
Mean	58.7
Std Dev	3.143



# B1L103S, U25-ch90, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



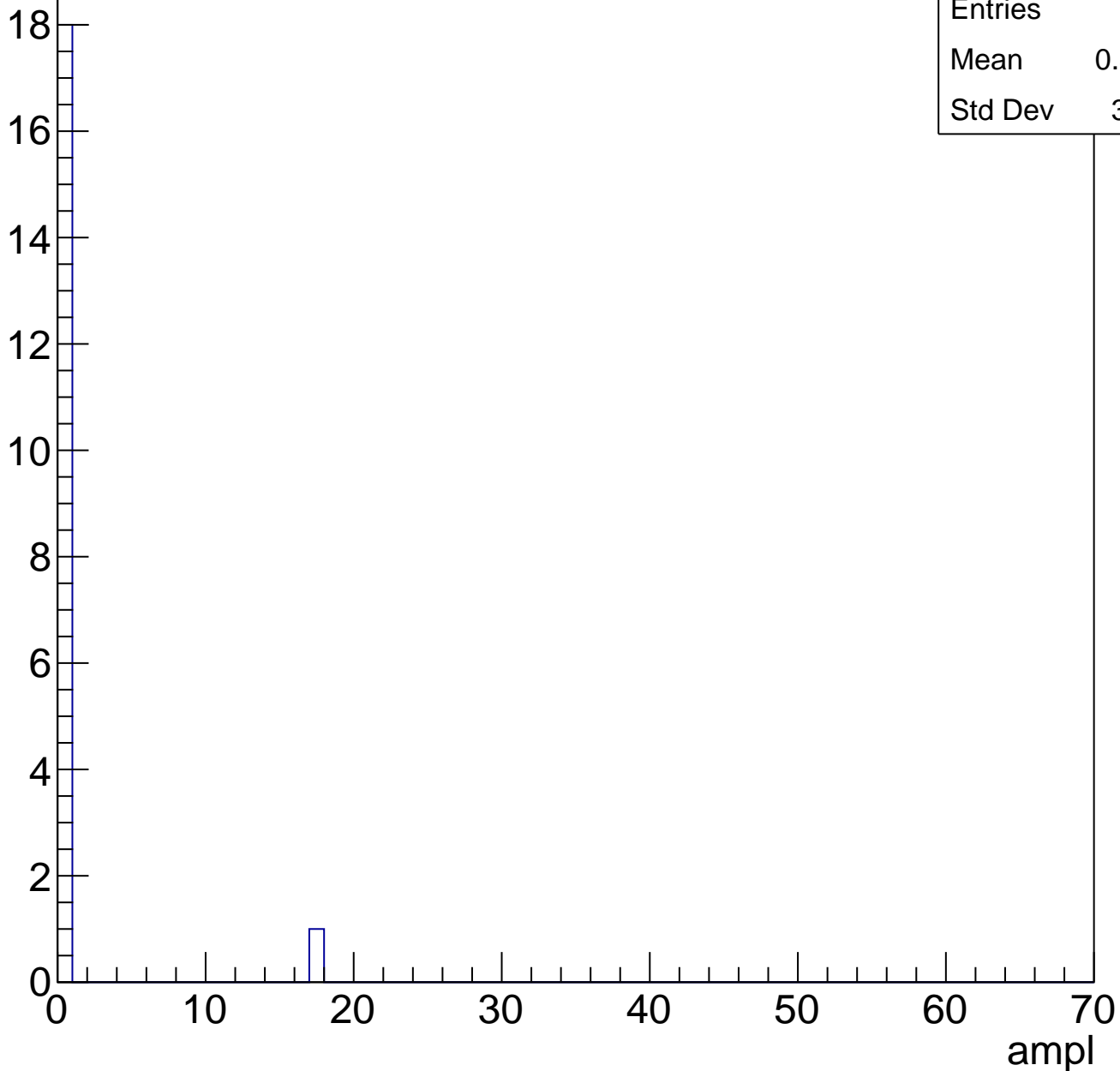


# B1L103S, U25-ch90, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	19
Mean	0.8947
Std Dev	3.796

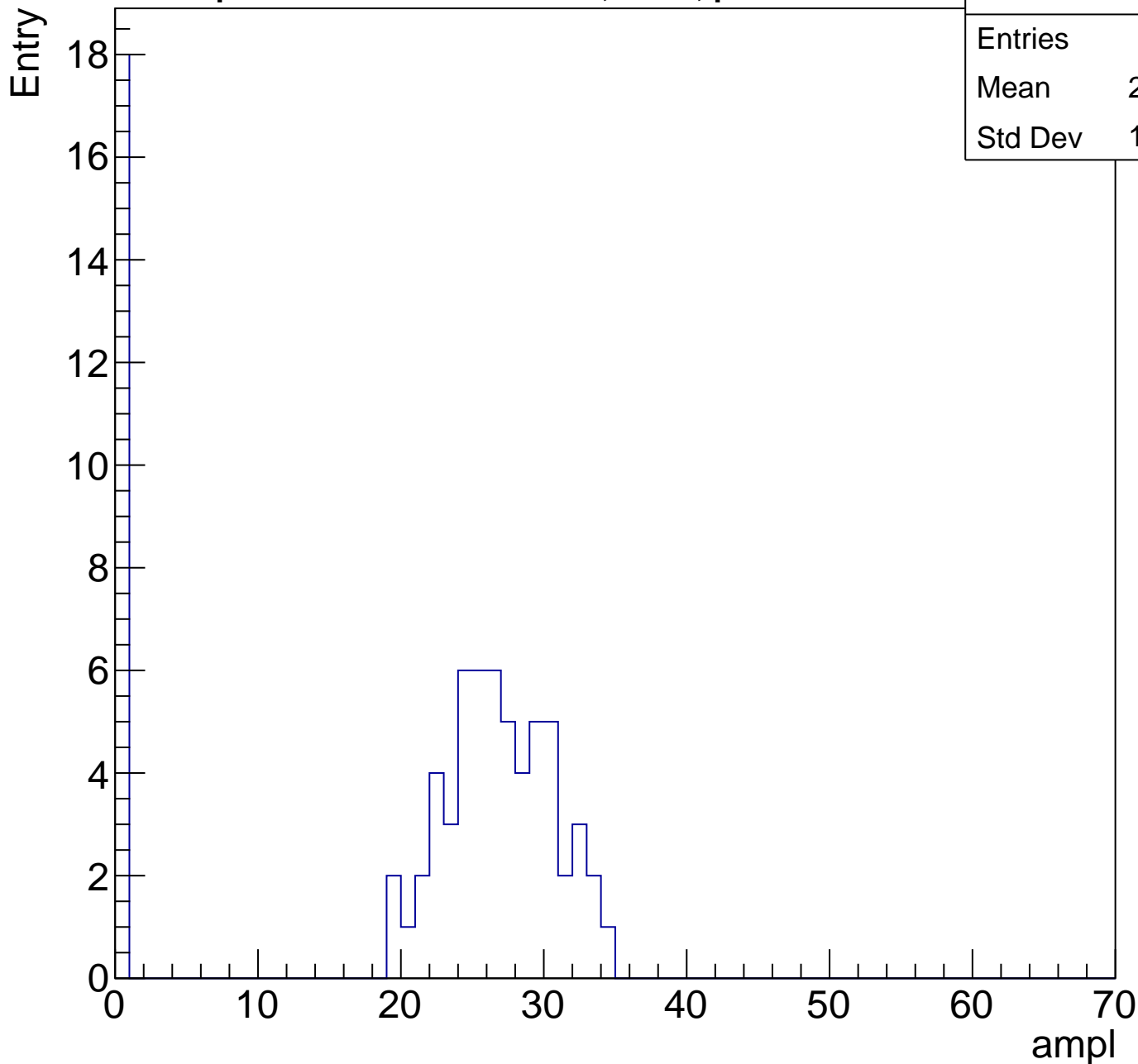
Entry



# B1L103S, U25-ch91, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	75
Mean	20.09
Std Dev	11.73

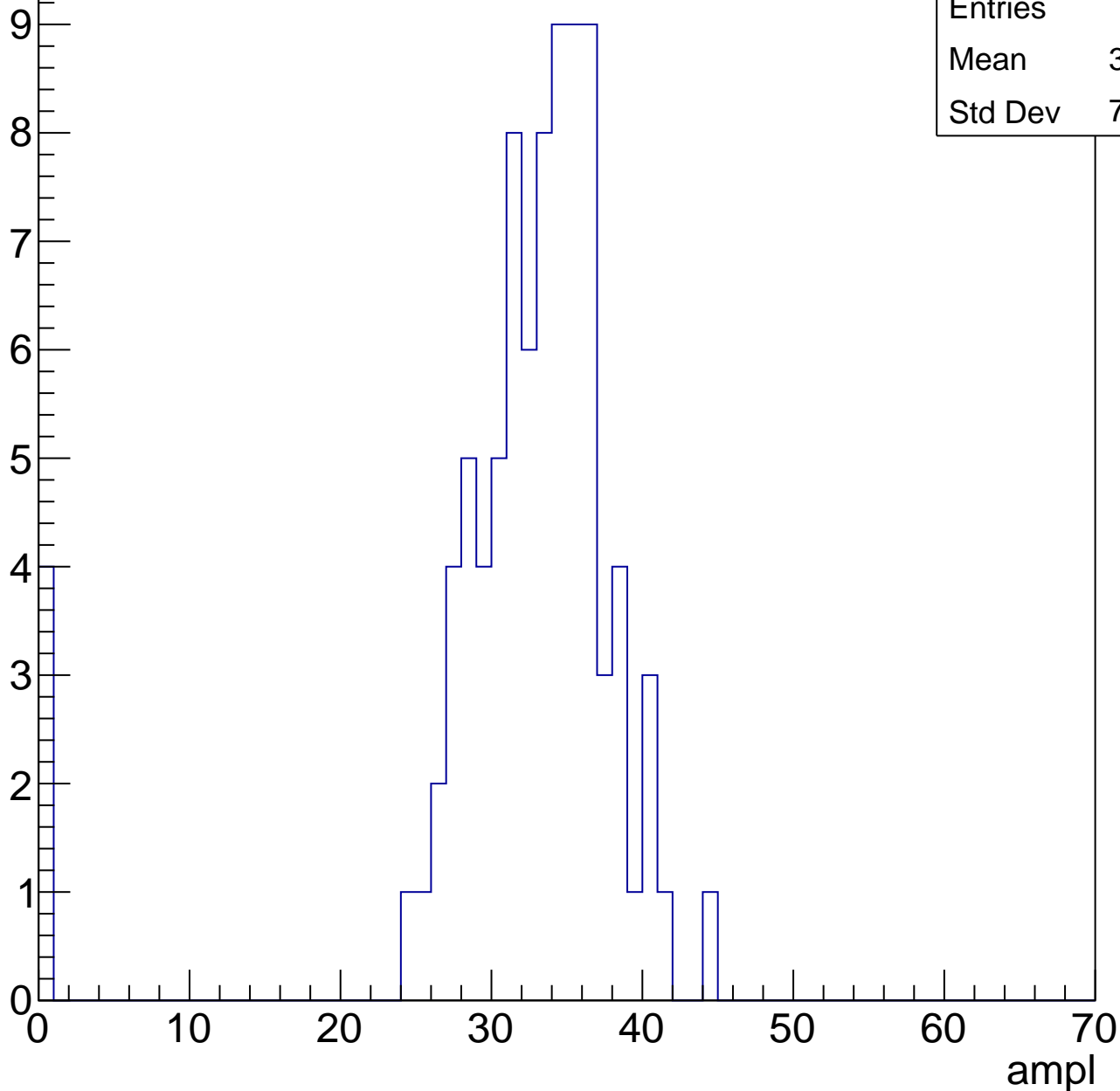


# B1L103S, U25-ch91, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	88
Mean	31.49
Std Dev	7.874



# B1L103S, U25-ch91, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	86
Mean	35.94
Std Dev	14.21

Entry

10

8

6

4

2

0

0

10

20

30

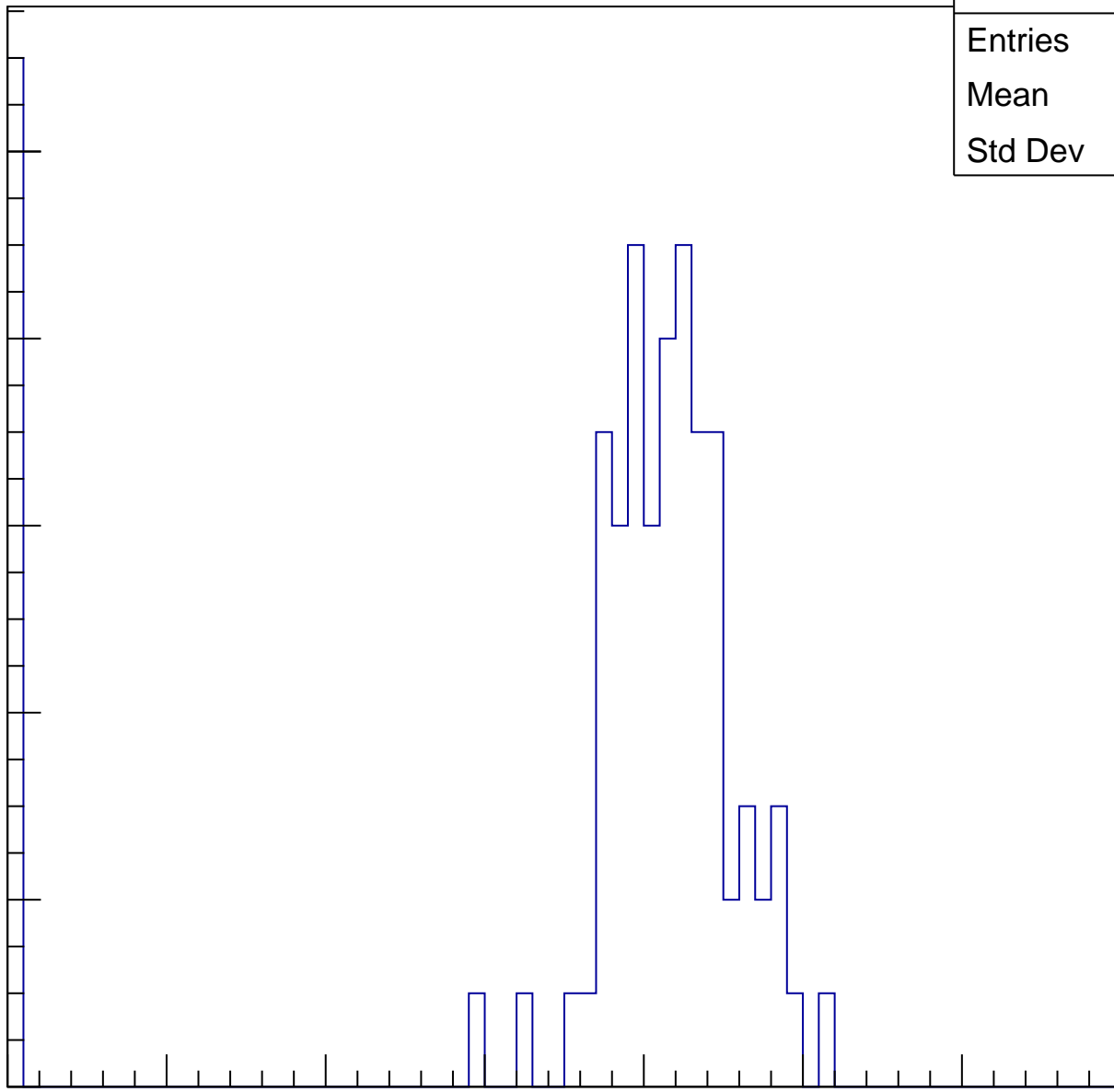
40

50

60

70

ampl

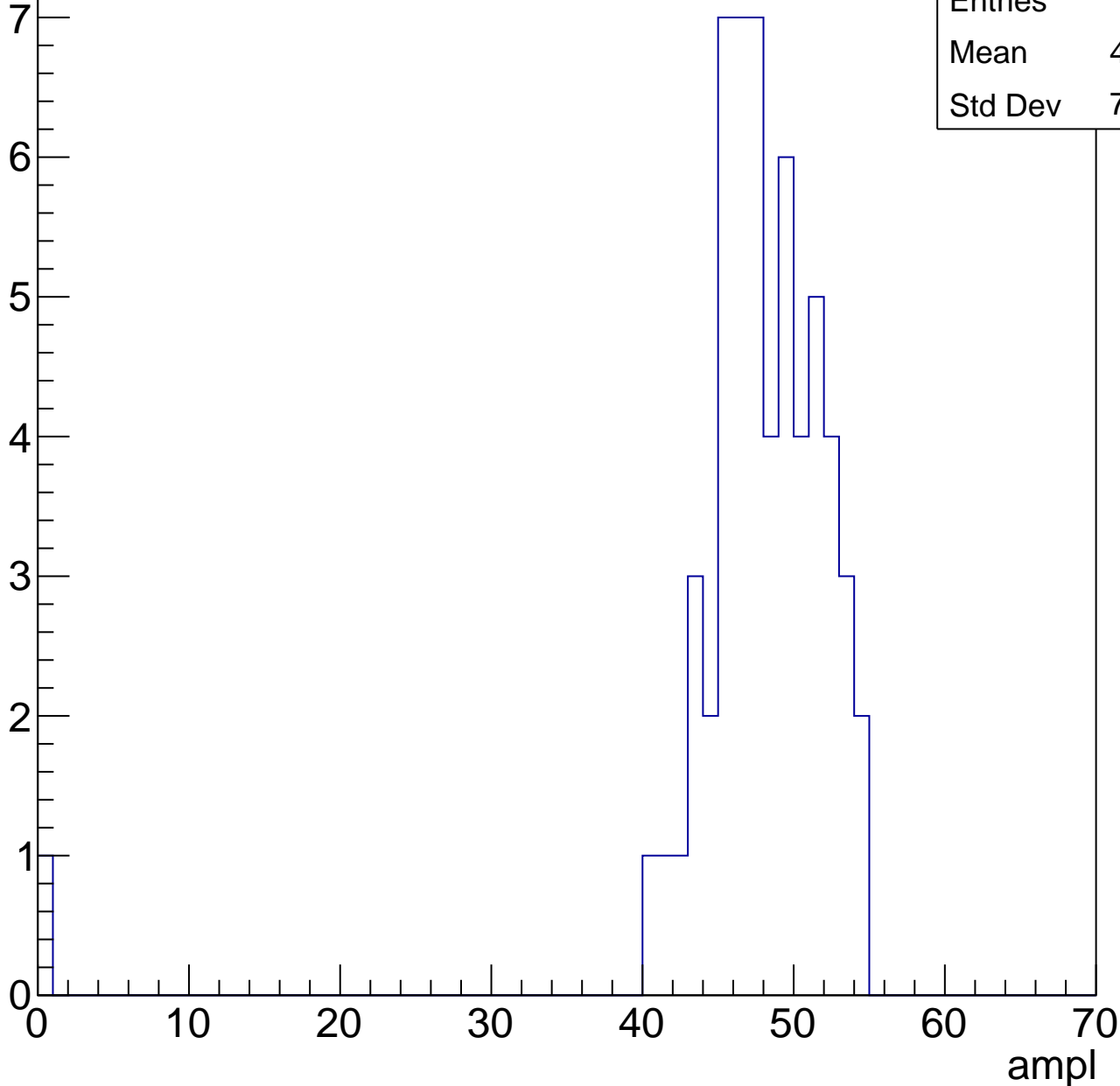


# B1L103S, U25-ch91, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	58
Mean	46.93
Std Dev	7.034

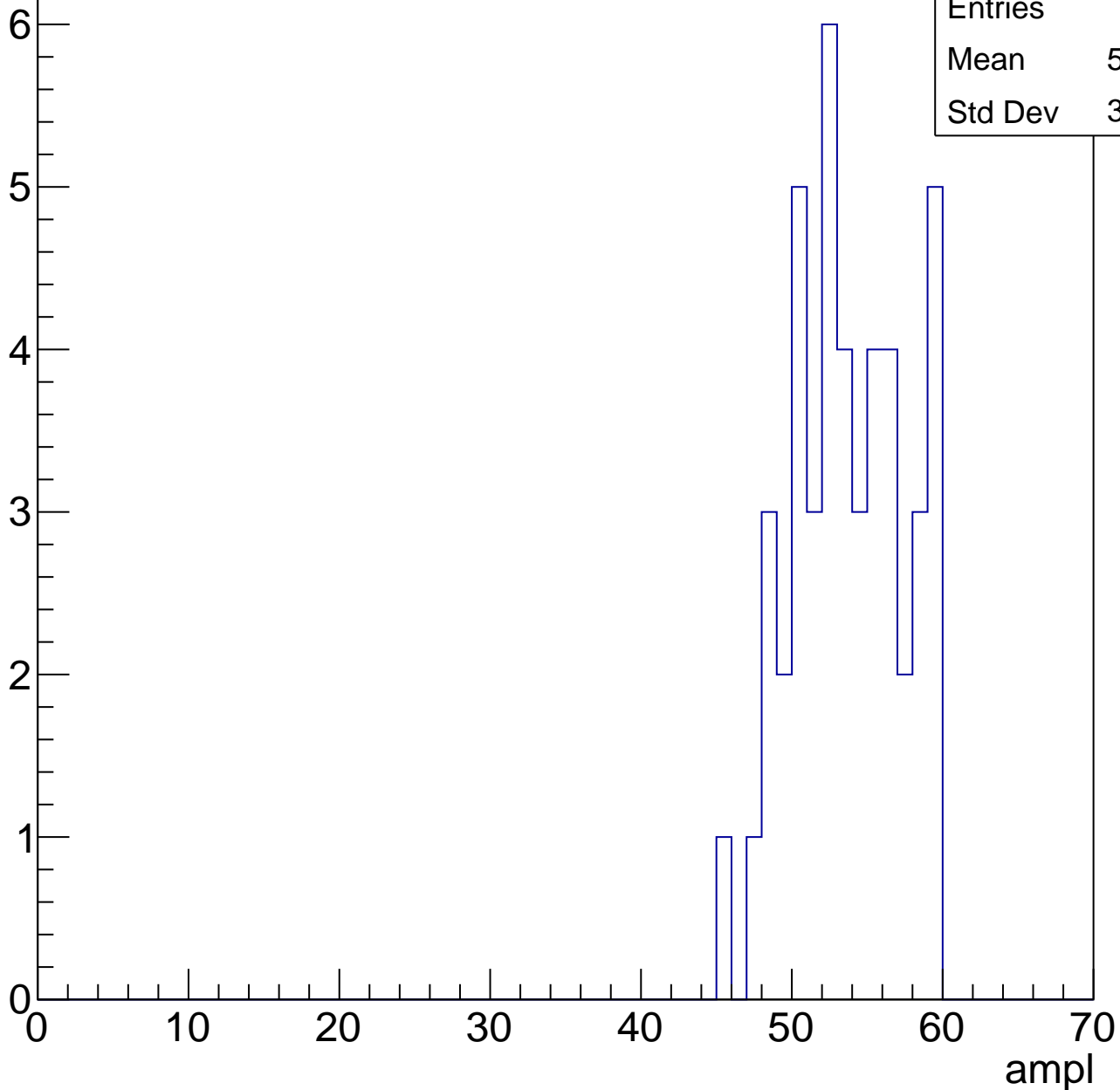


# B1L103S, U25-ch91, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	46
Mean	53.26
Std Dev	3.638

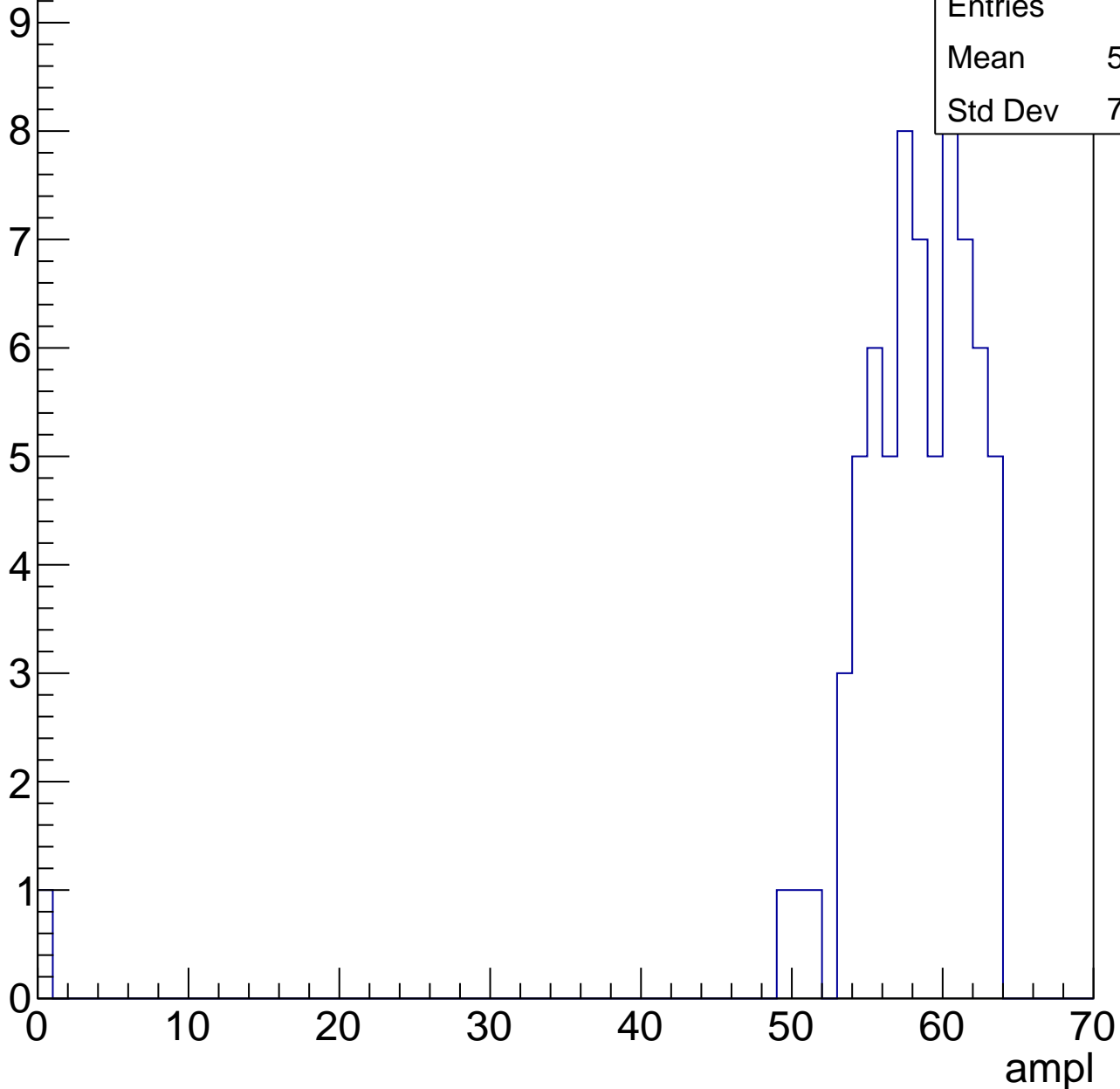


# B1L103S, U25-ch91, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	70
Mean	57.14
Std Dev	7.624

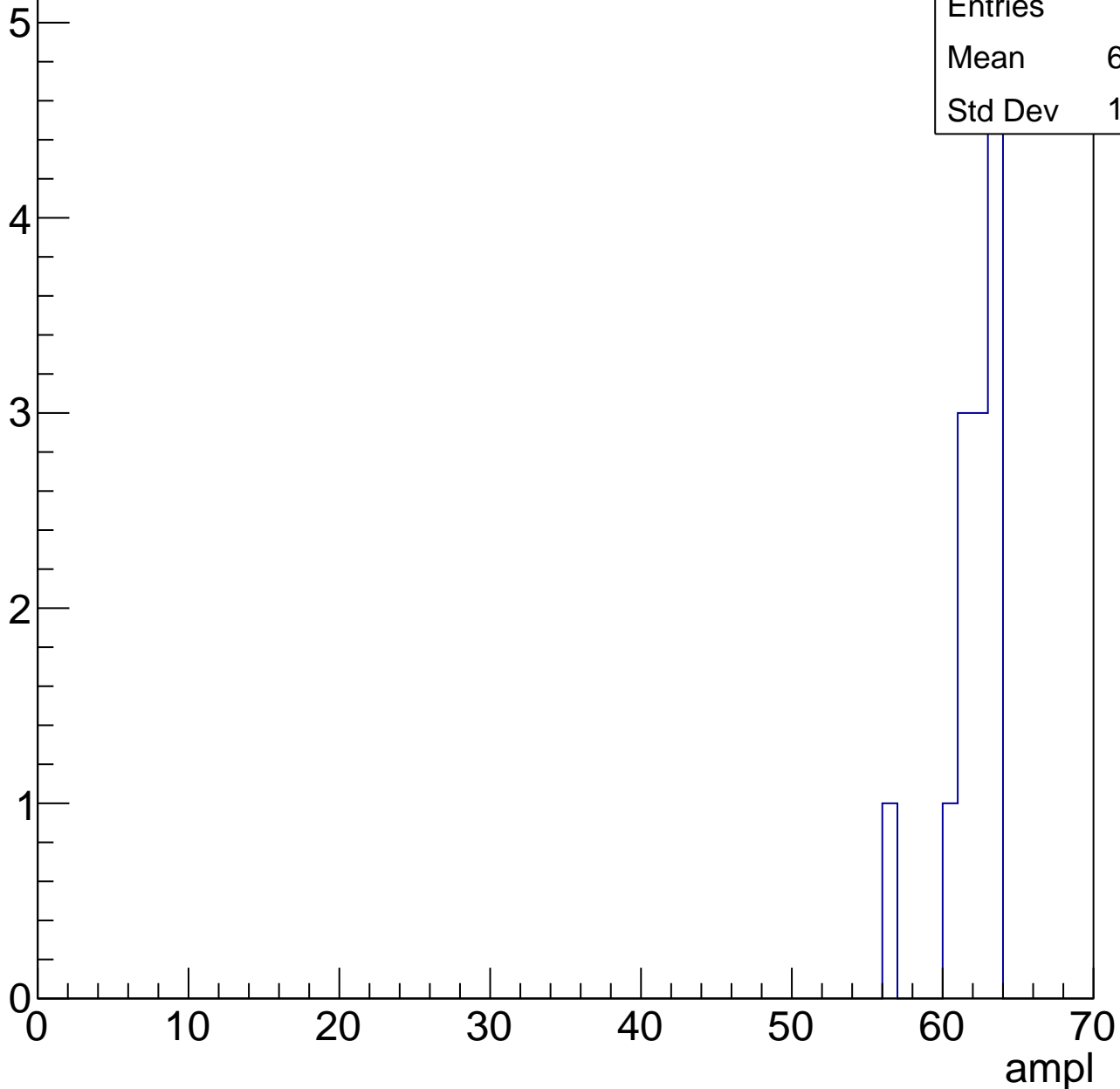


# B1L103S, U25-ch91, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	13
Mean	61.54
Std Dev	1.865



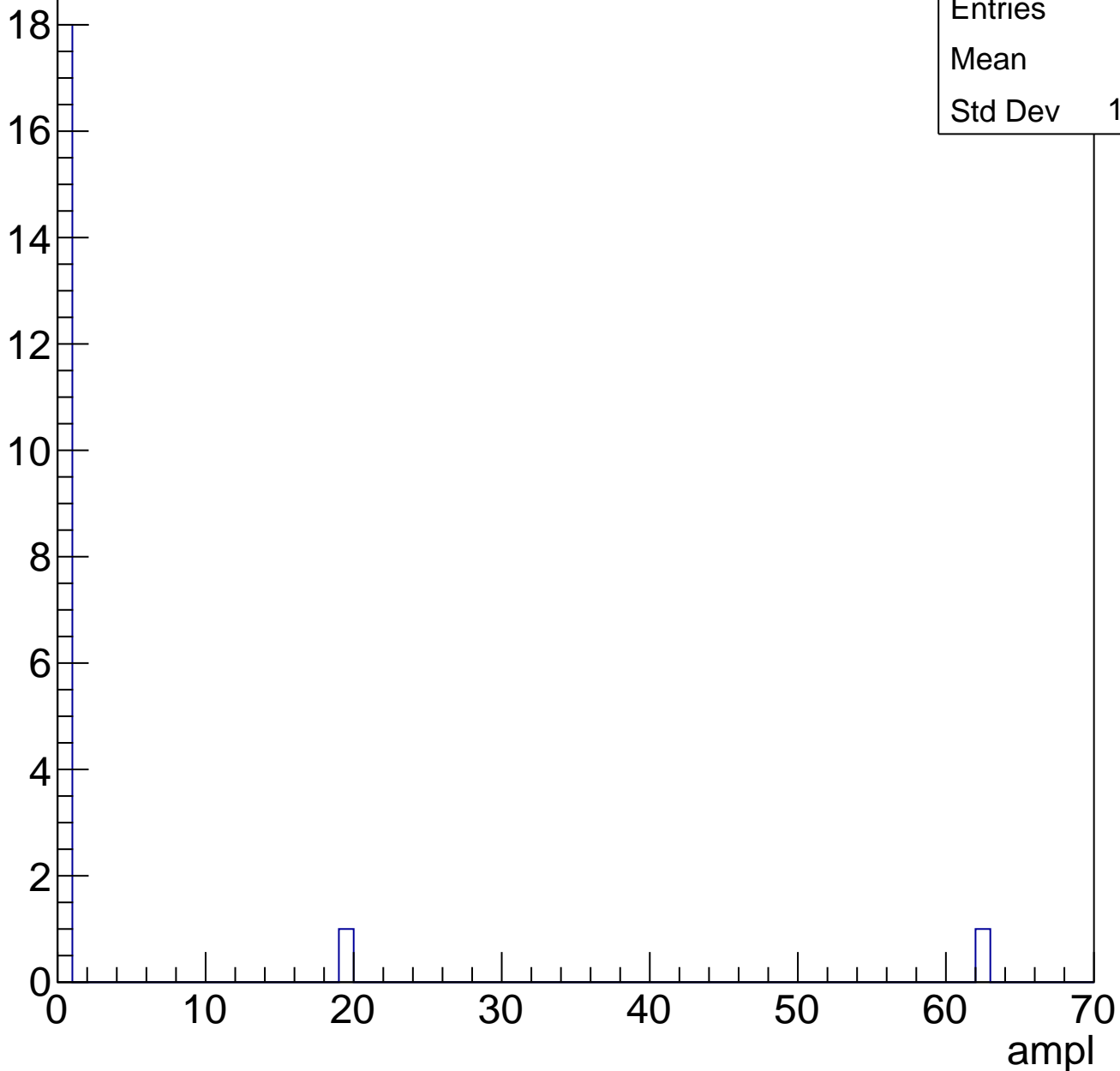


# B1L103S, U25-ch91, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	20
Mean	4.05
Std Dev	13.92

Entry

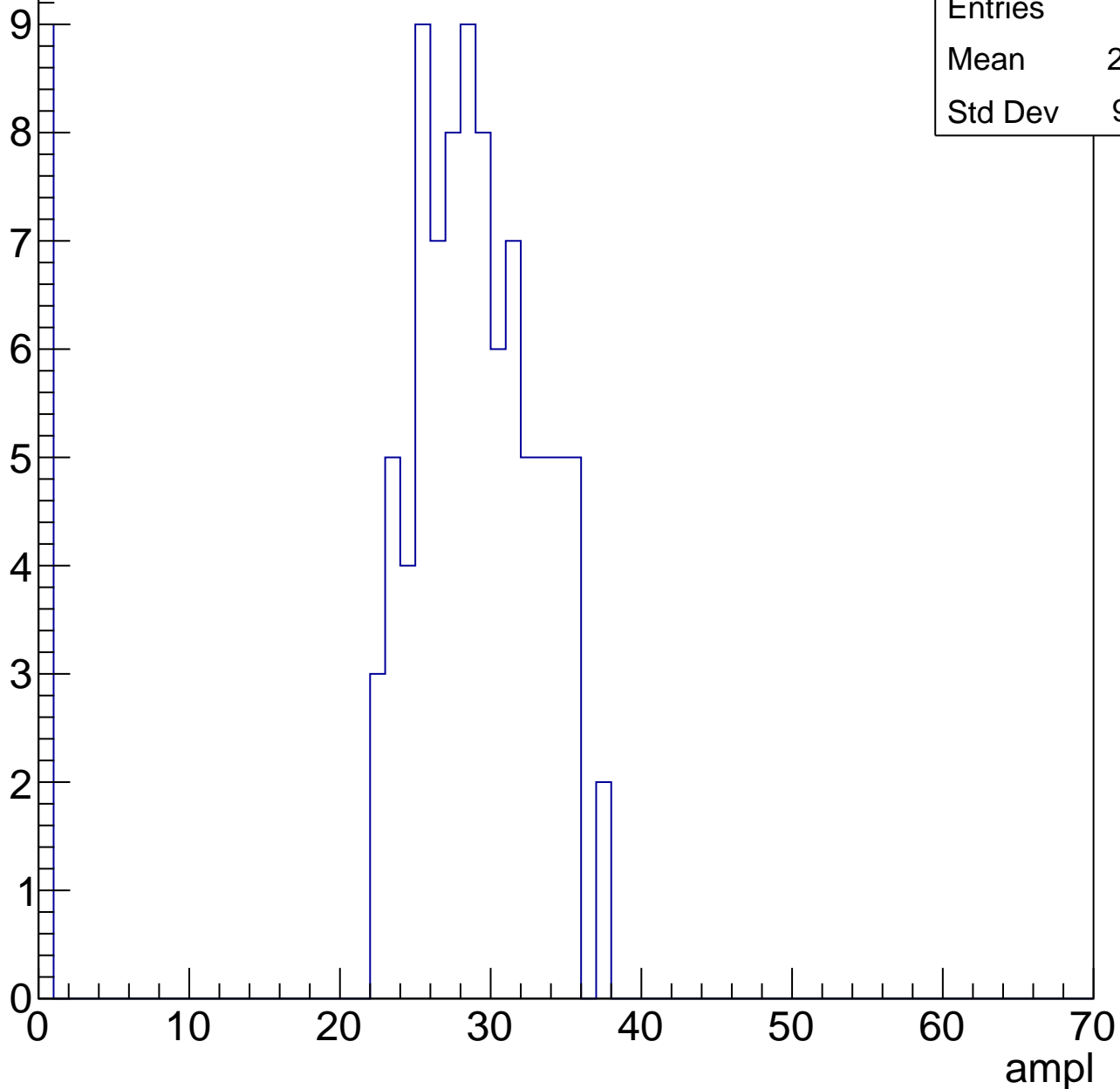


# B1L103S, U25-ch92, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	97
Mean	26.03
Std Dev	9.071

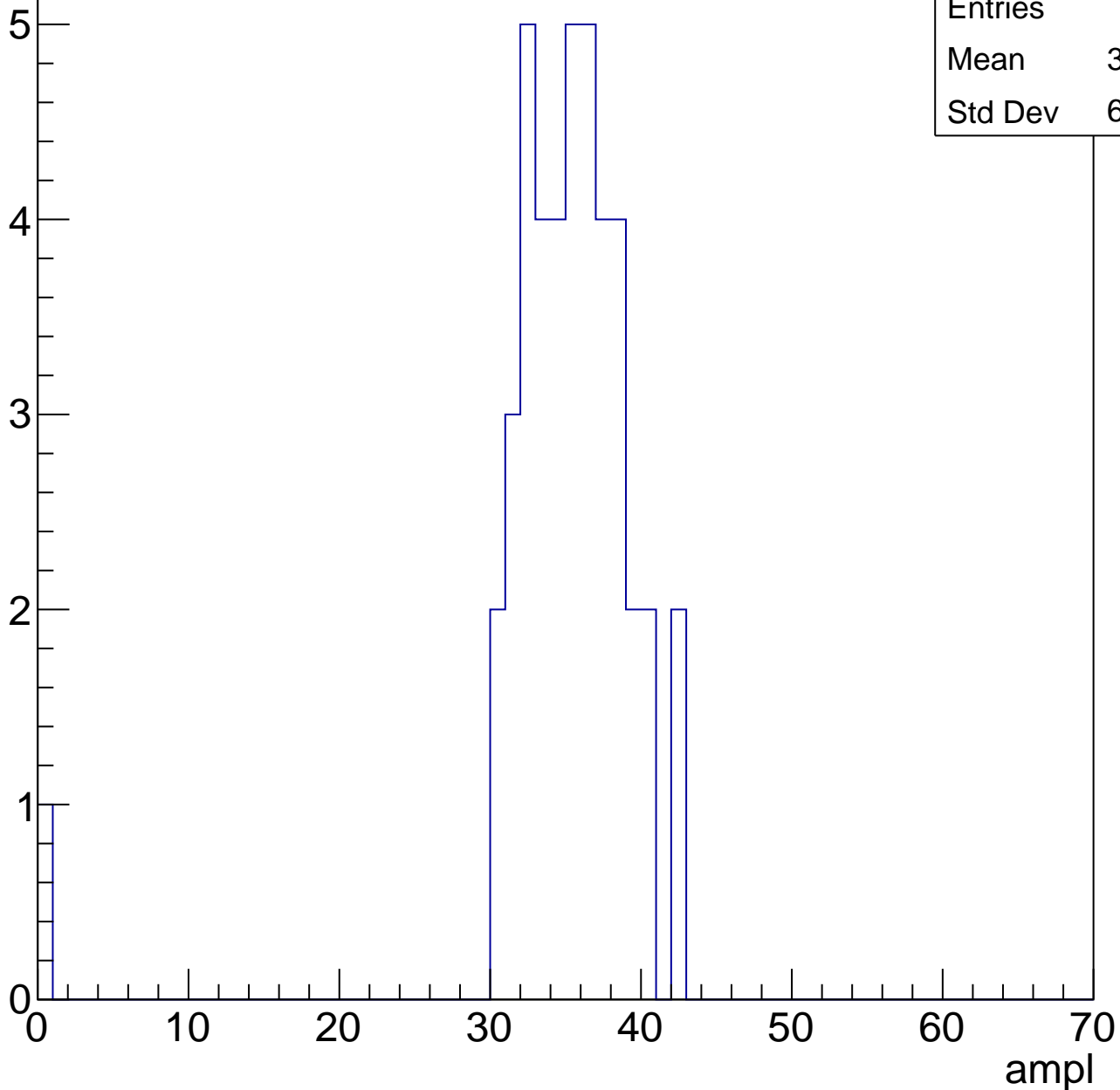


# B1L103S, U25-ch92, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	43
Mean	34.37
Std Dev	6.115

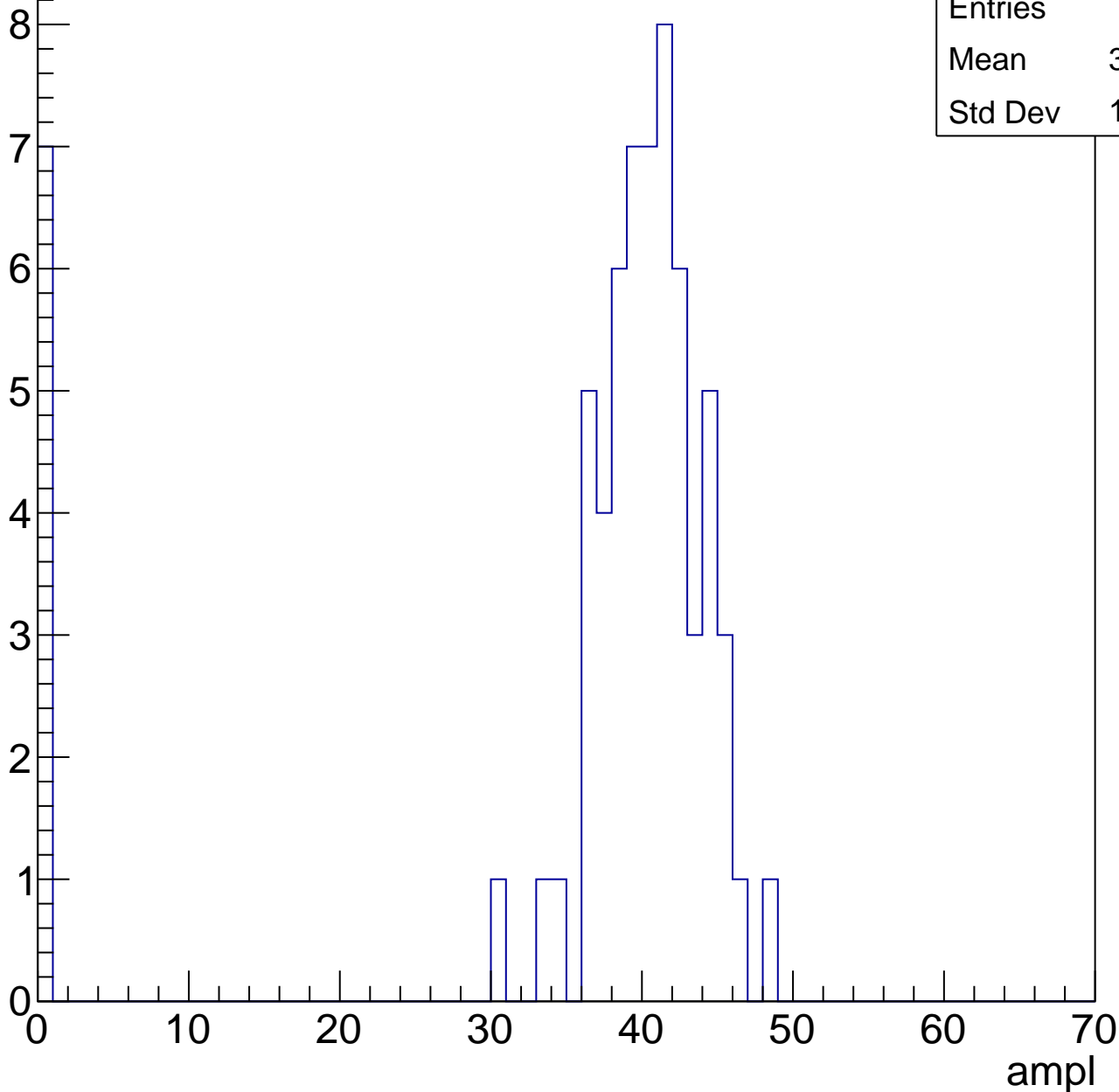


# B1L103S, U25-ch92, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	66
Mean	35.82
Std Dev	12.73

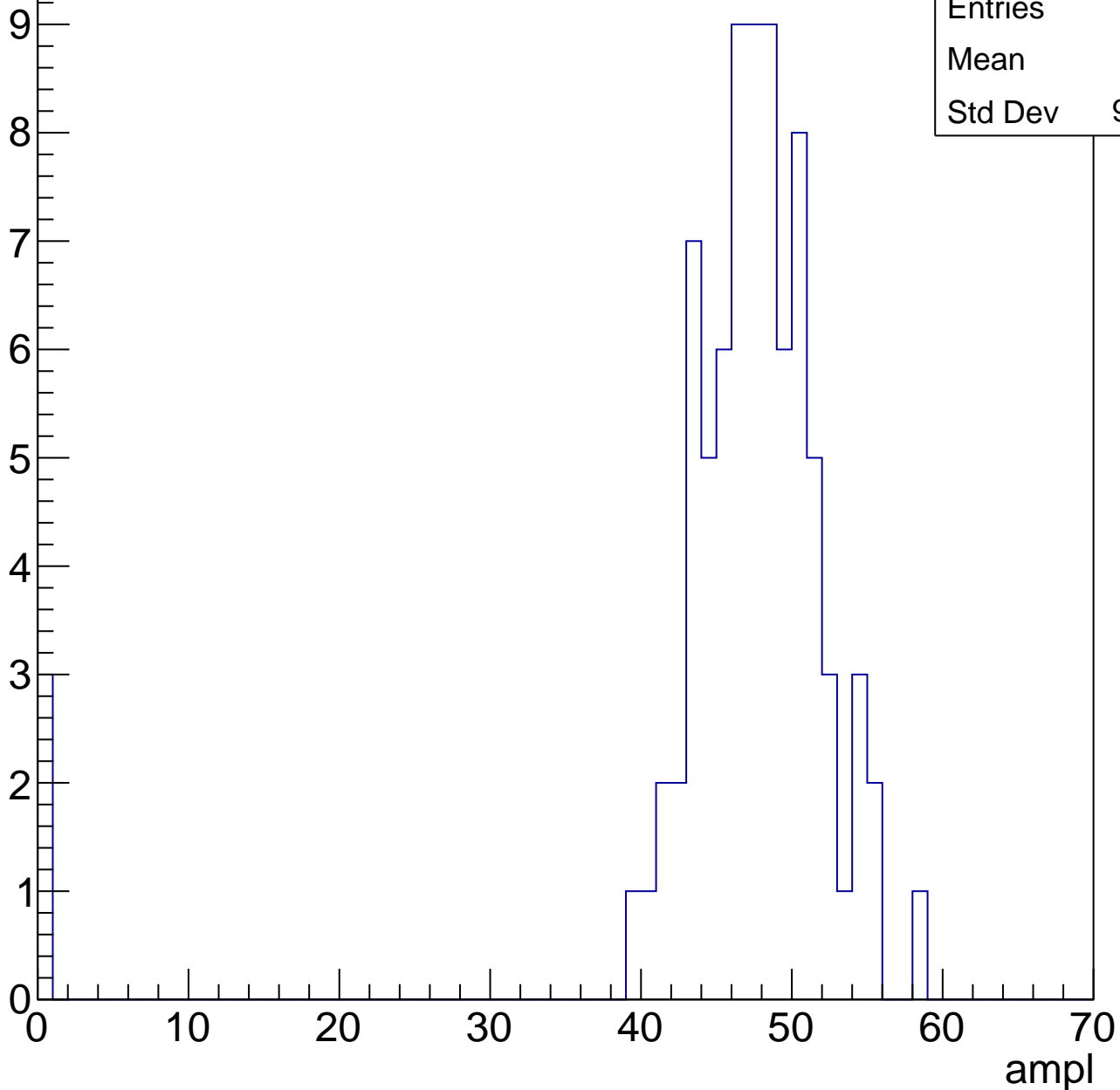


# B1L103S, U25-ch92, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

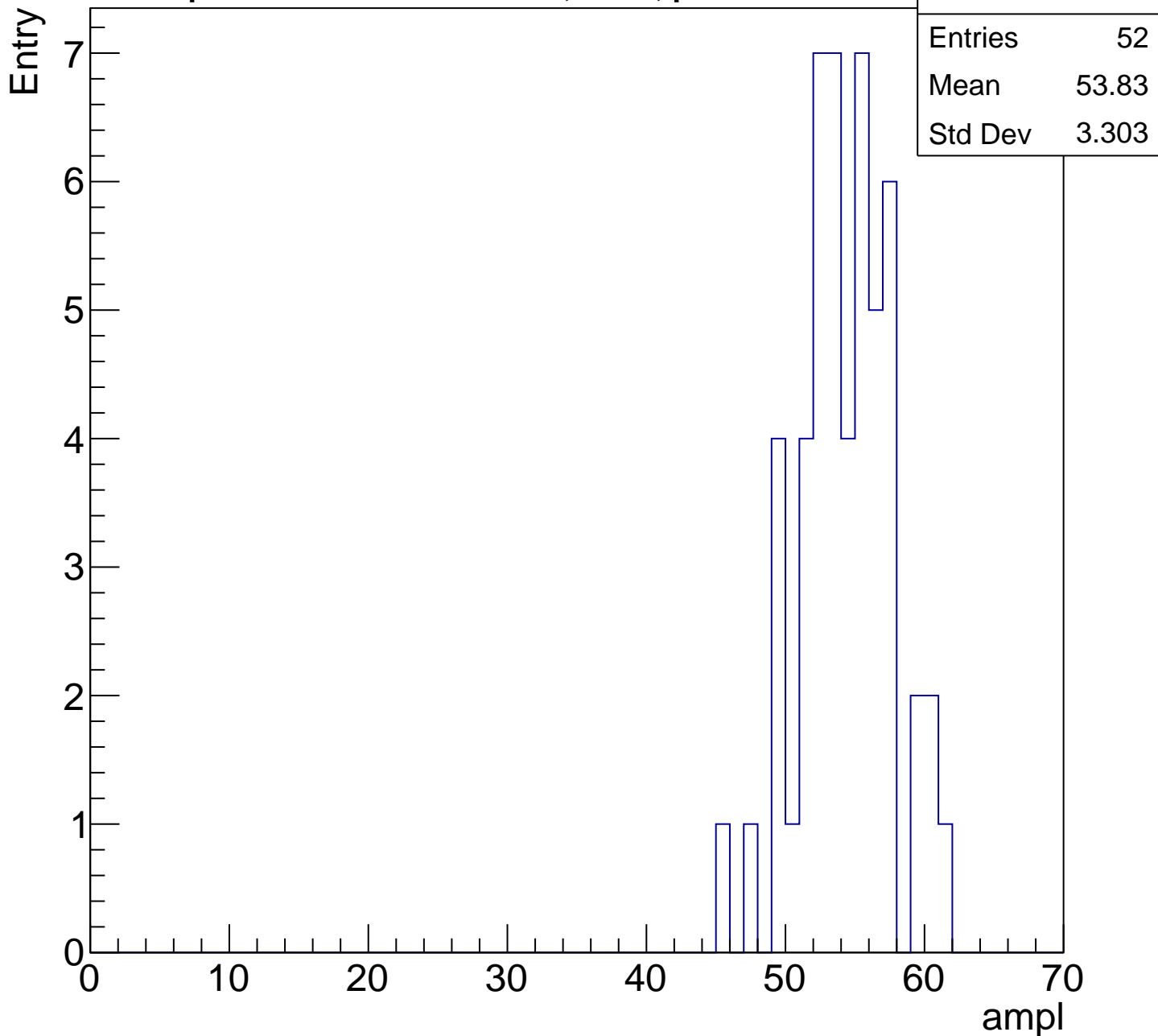
Entry

Entries	83
Mean	45.7
Std Dev	9.571



# B1L103S, U25-ch92, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

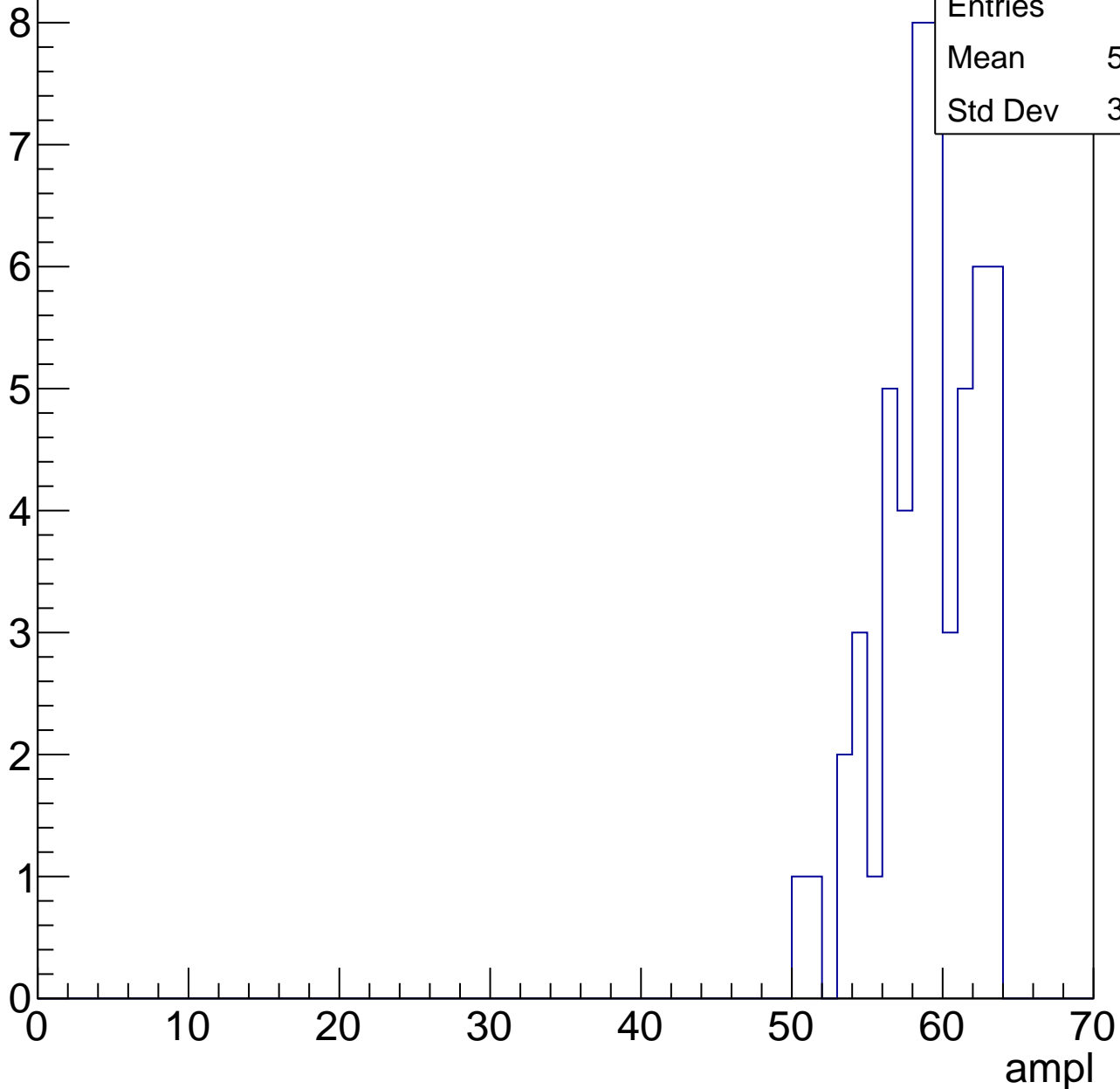


# B1L103S, U25-ch92, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

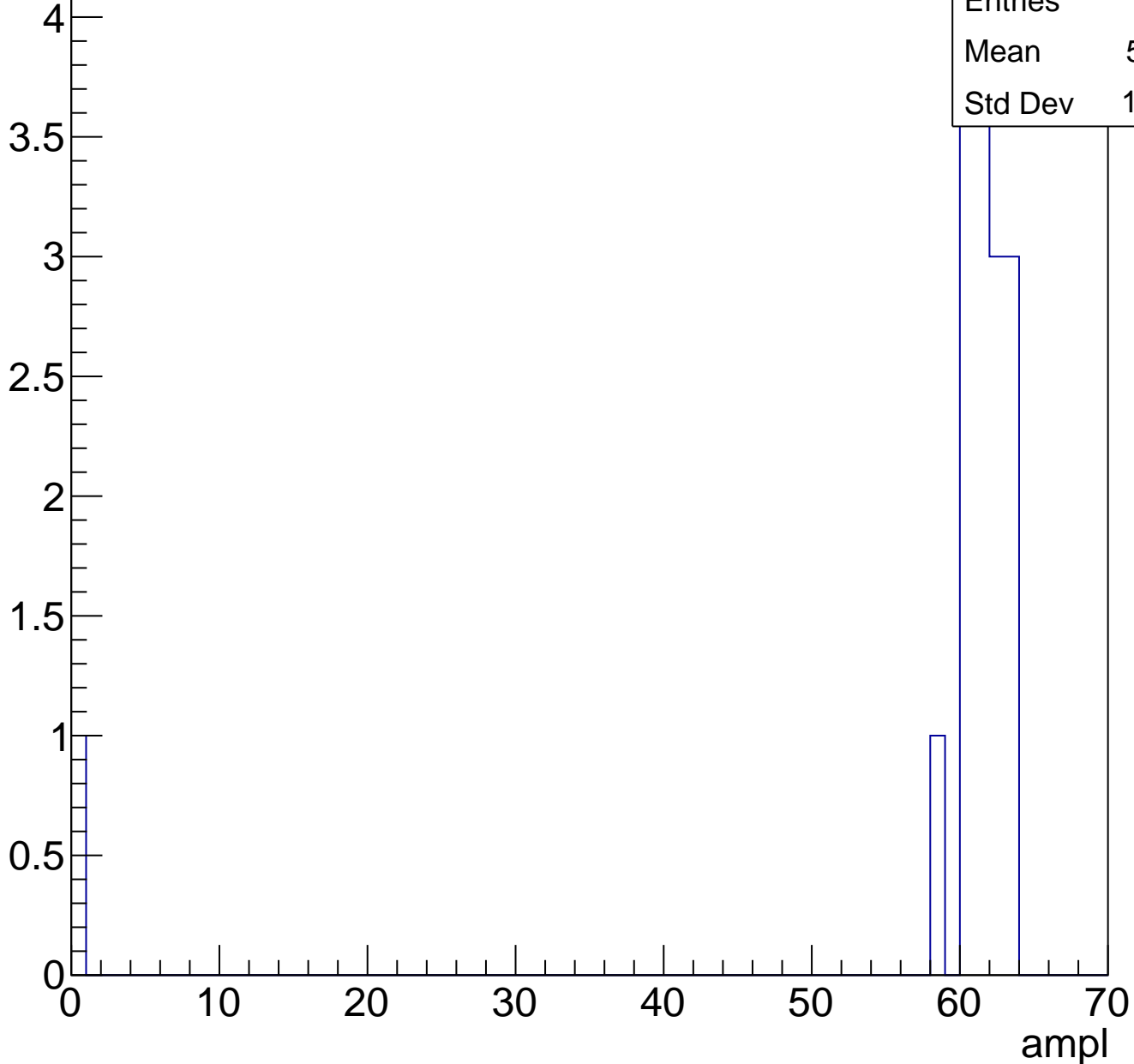
Entries	53
Mean	58.55
Std Dev	3.189



# B1L103S, U25-ch92, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	16
Mean	57.31
Std Dev	14.86

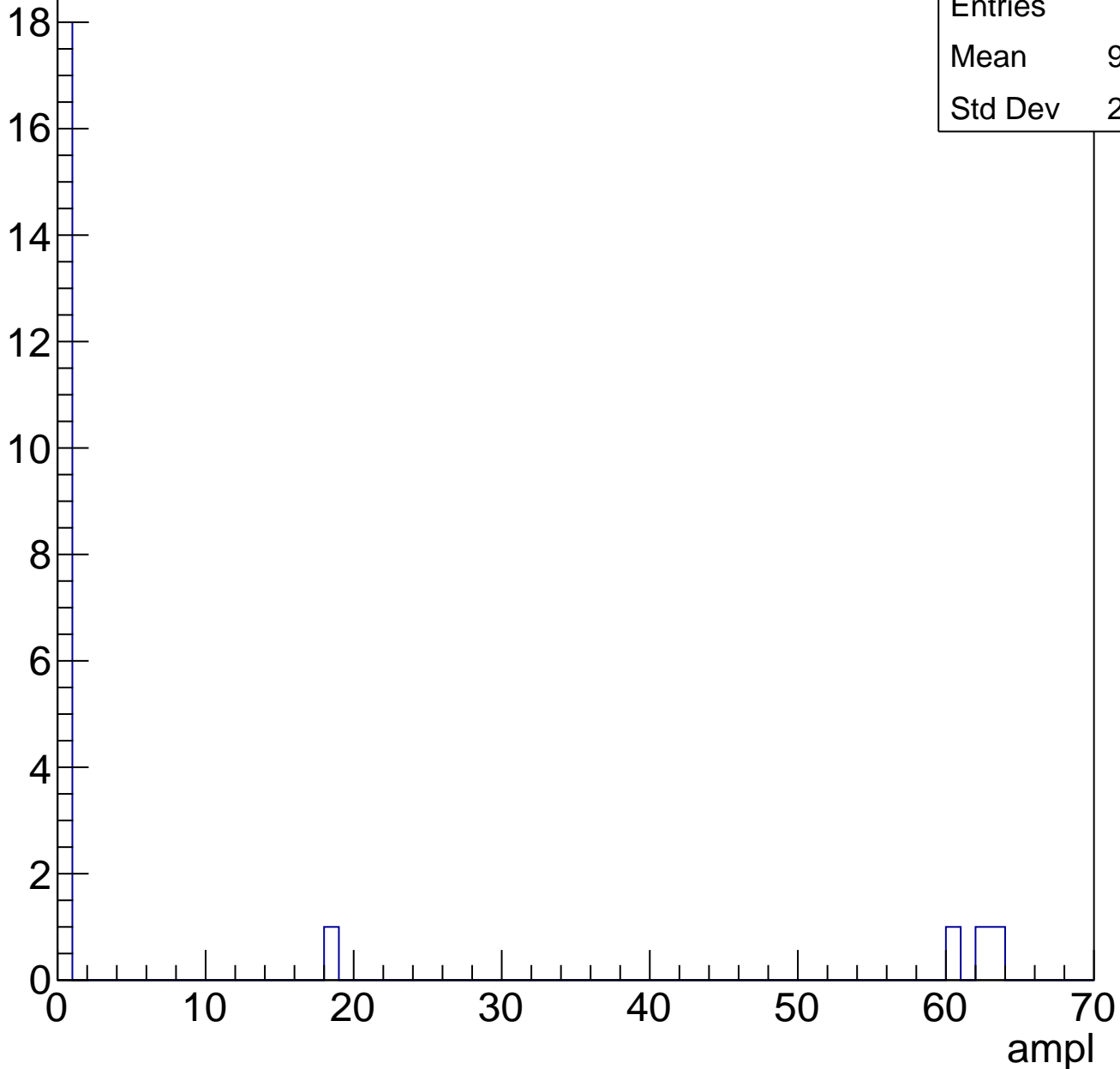


# B1L103S, U25-ch92, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	22
Mean	9.227
Std Dev	21.17

Entry

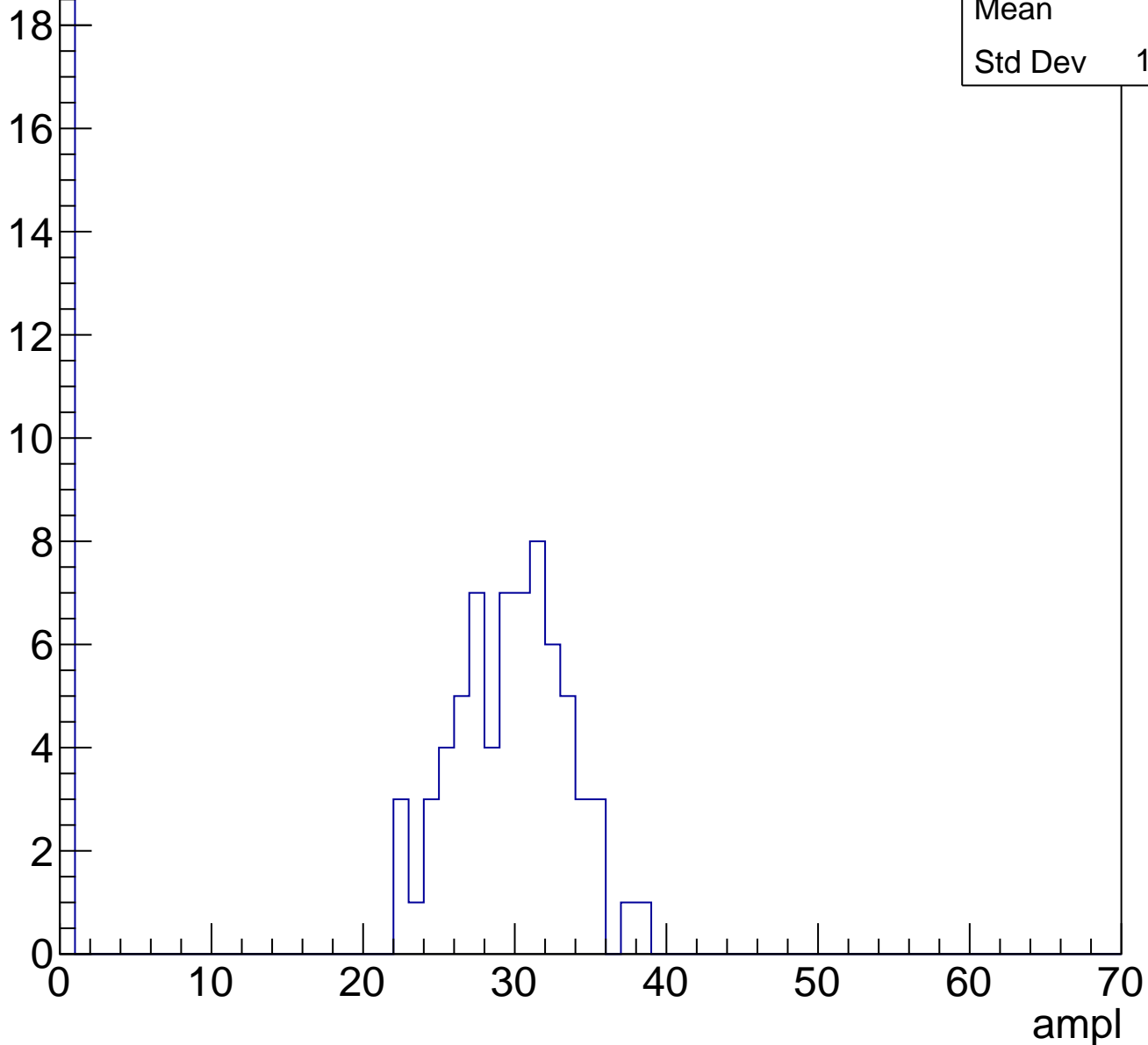


# B1L103S, U25-ch93, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	87
Mean	22.9
Std Dev	12.52

Entry

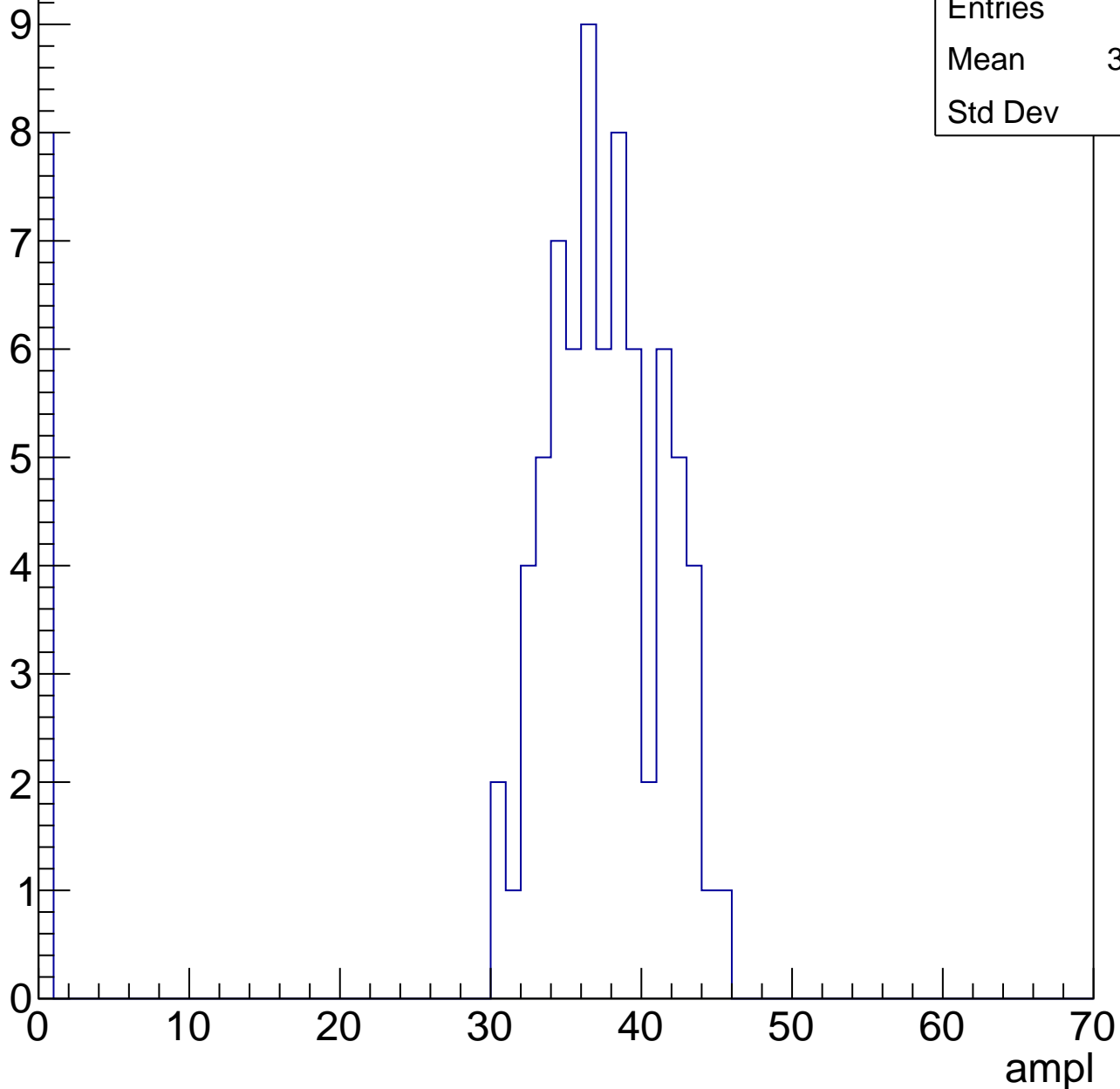


# B1L103S, U25-ch93, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	81
Mean	33.49
Std Dev	11.6

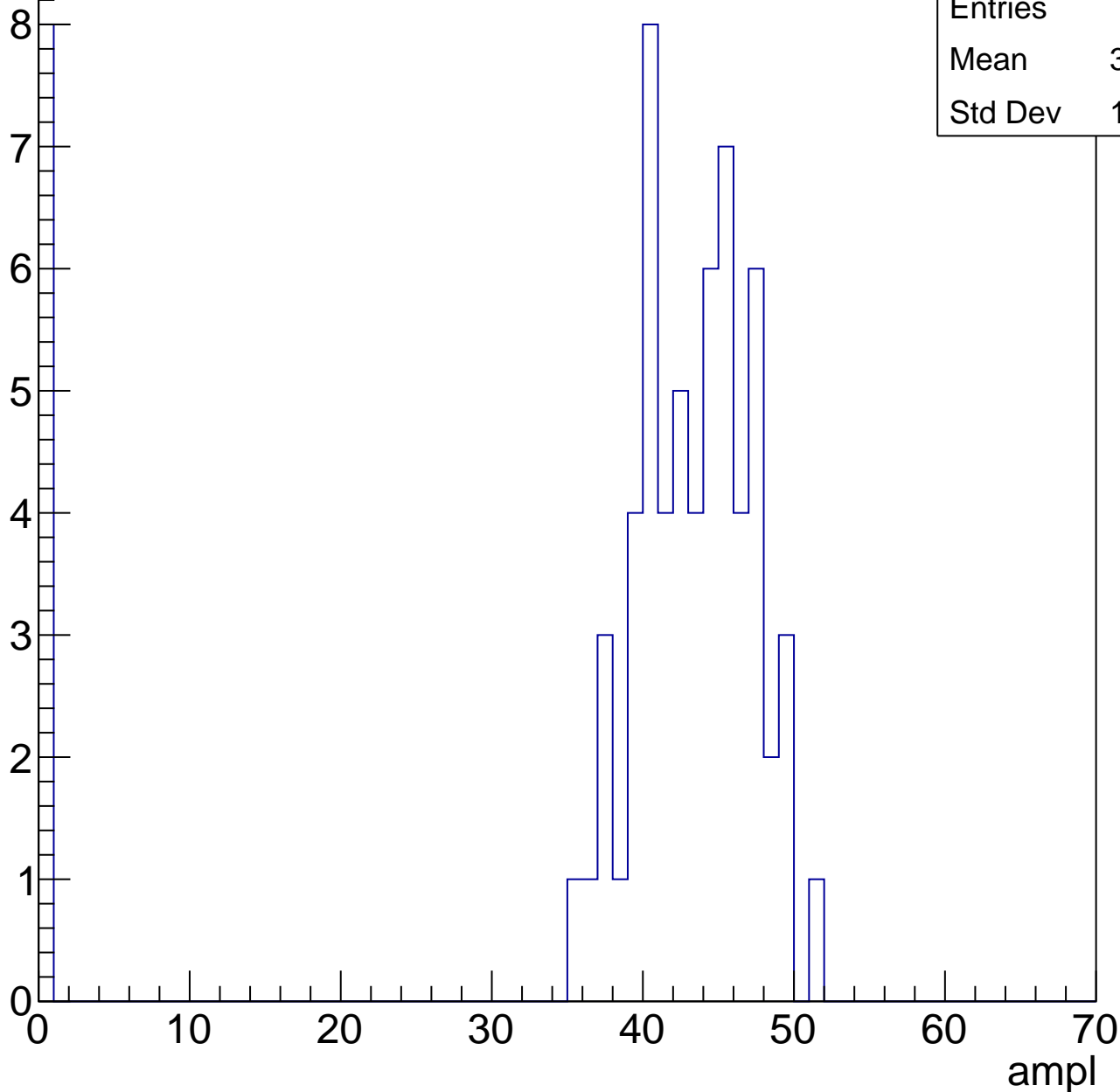


# B1L103S, U25-ch93, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	68
Mean	37.96
Std Dev	14.27

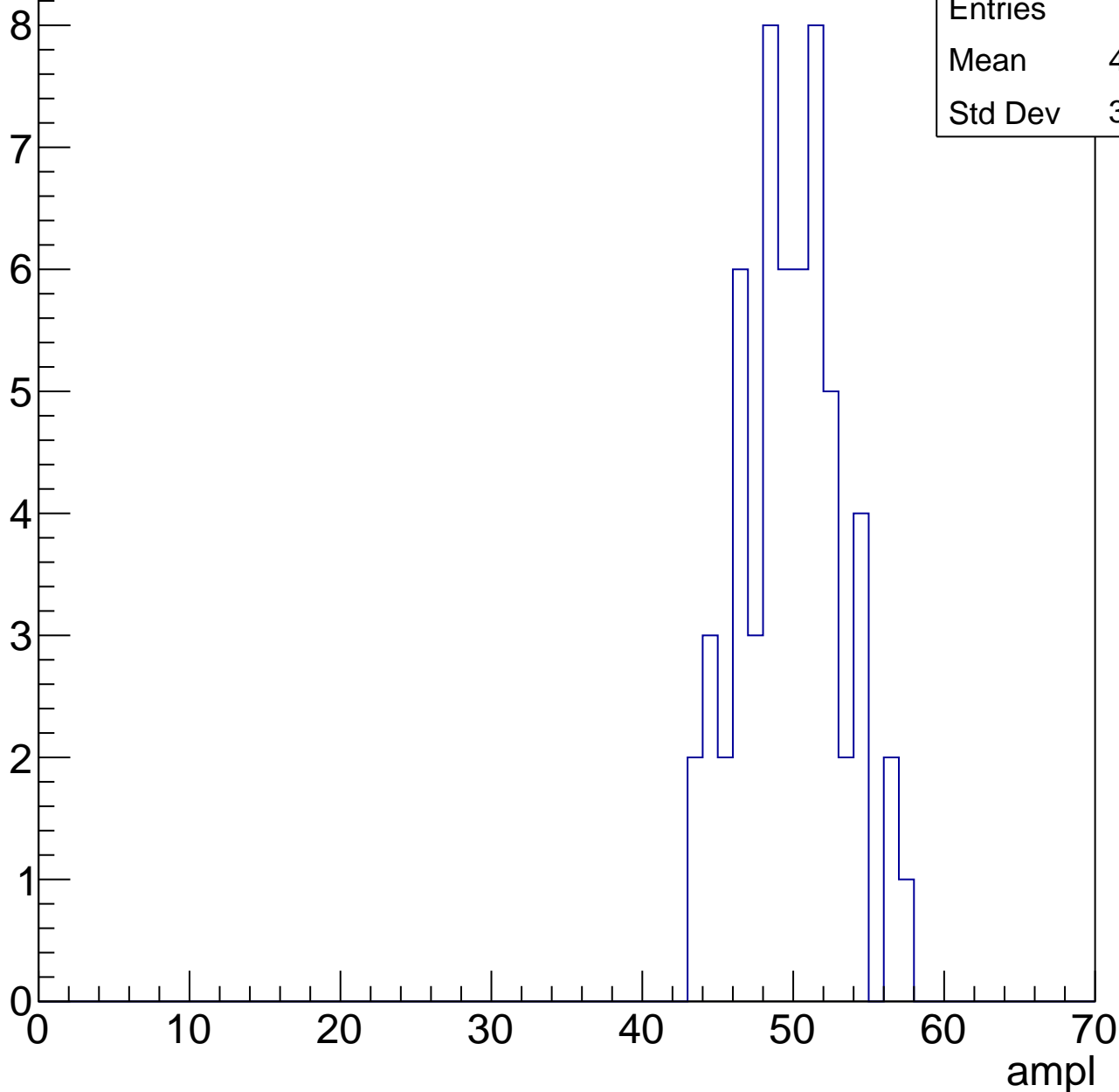


# B1L103S, U25-ch93, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	58
Mean	49.34
Std Dev	3.278

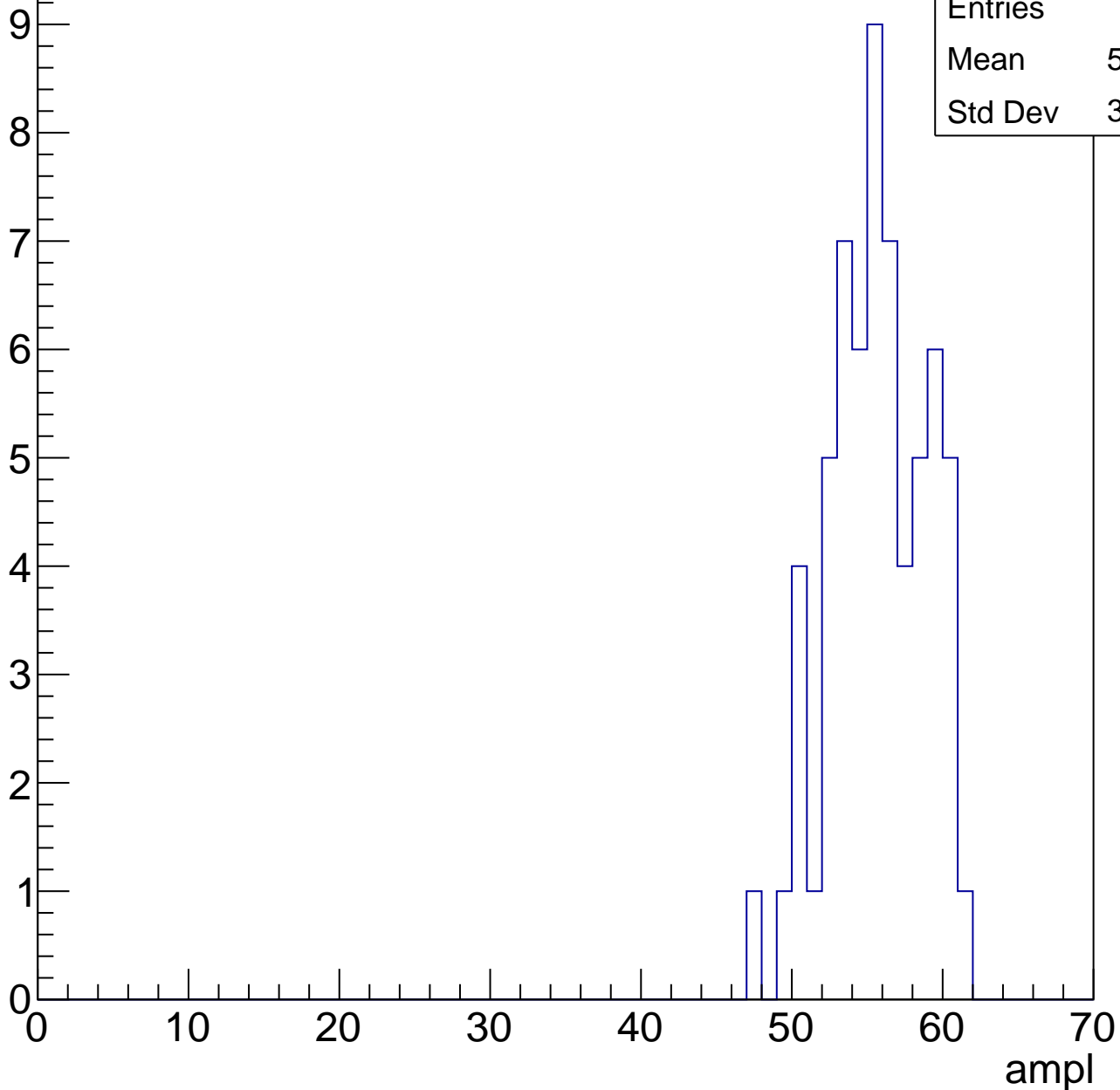


# B1L103S, U25-ch93, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

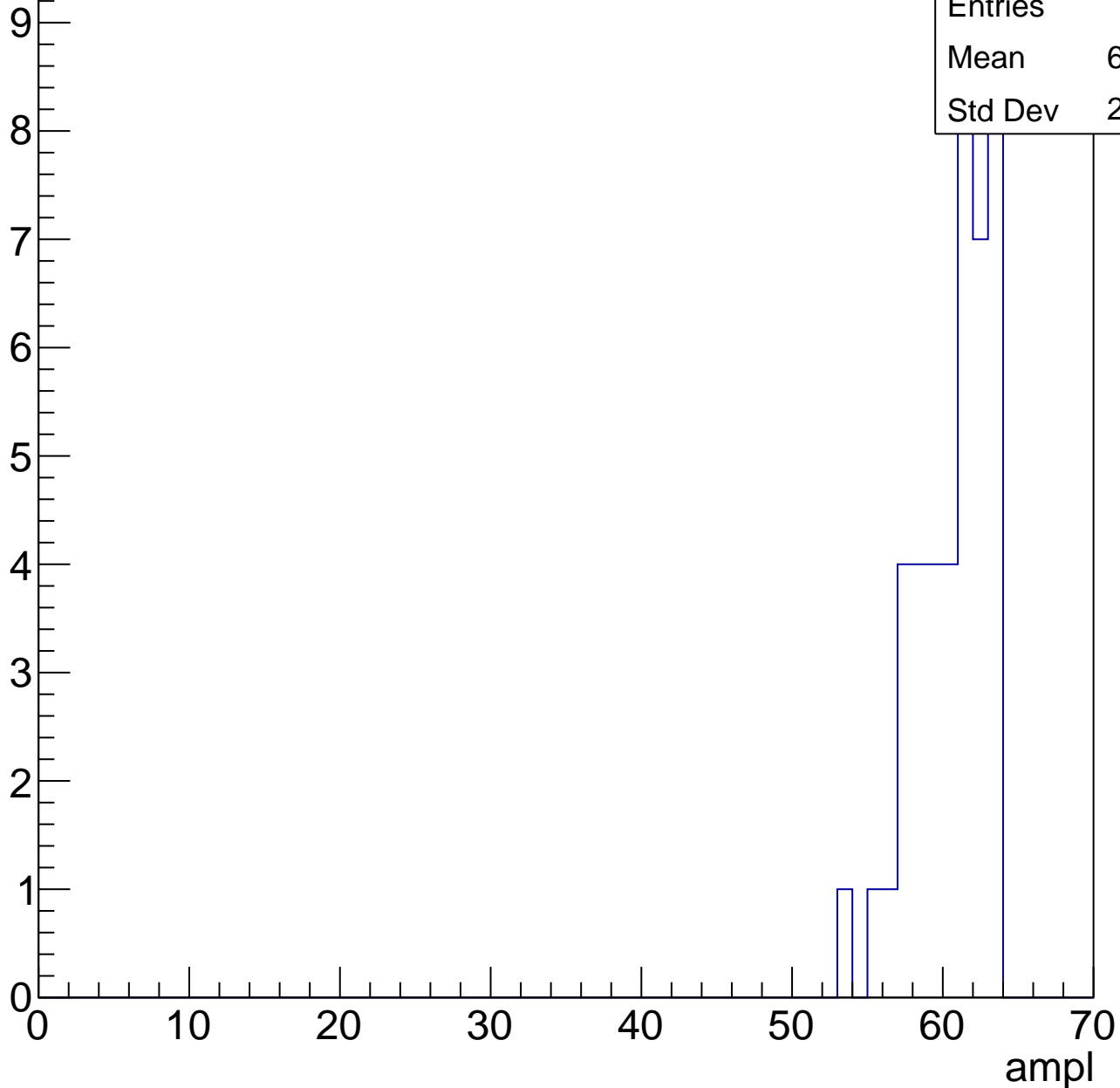
Entries	62
Mean	55.19
Std Dev	3.156



# B1L103S, U25-ch93, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

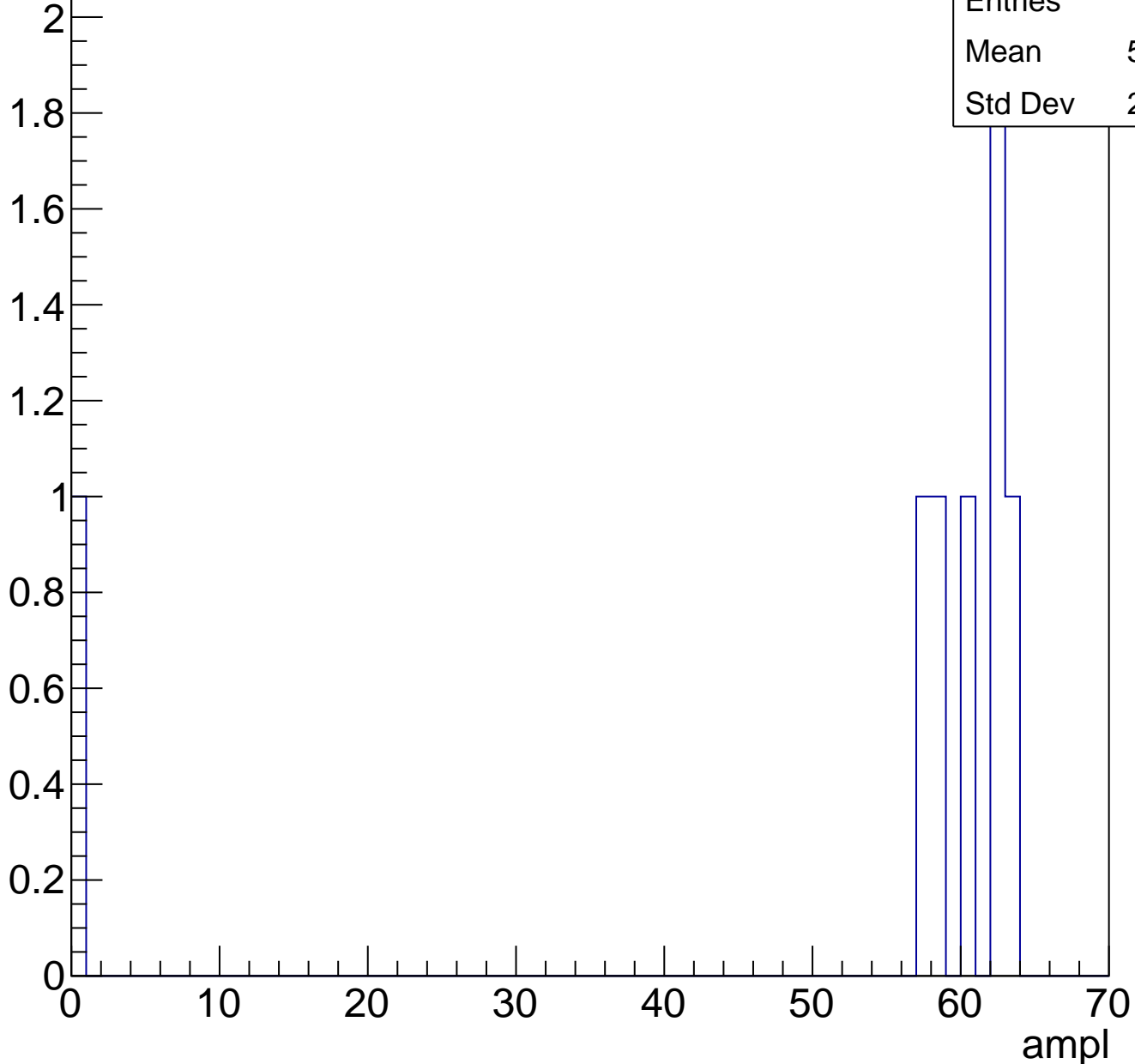
Entry



# B1L103S, U25-ch93, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U25-ch93, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	20
Mean	3.1
Std Dev	13.51

Entry

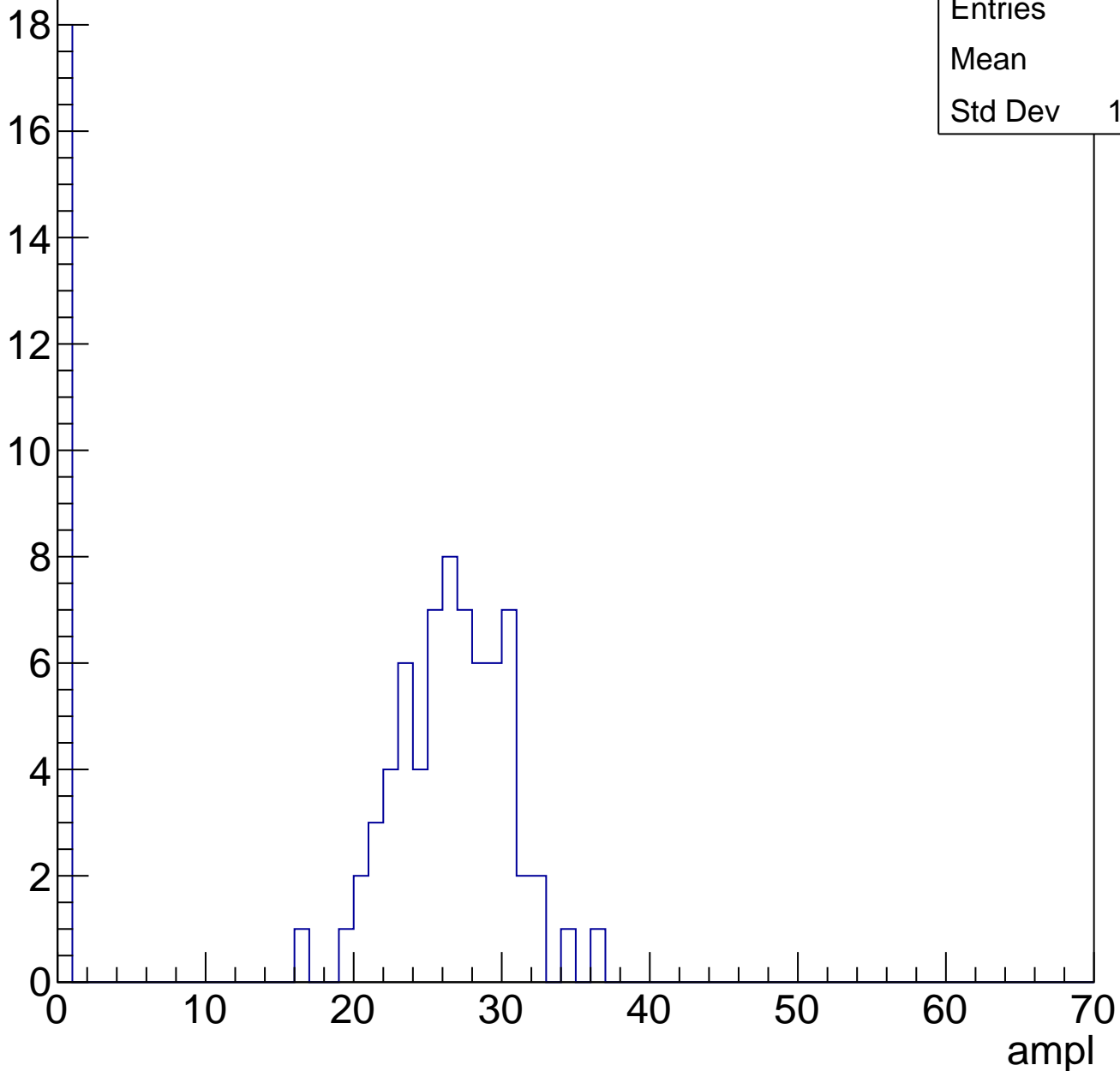


# B1L103S, U25-ch94, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	86
Mean	20.7
Std Dev	11.14

Entry

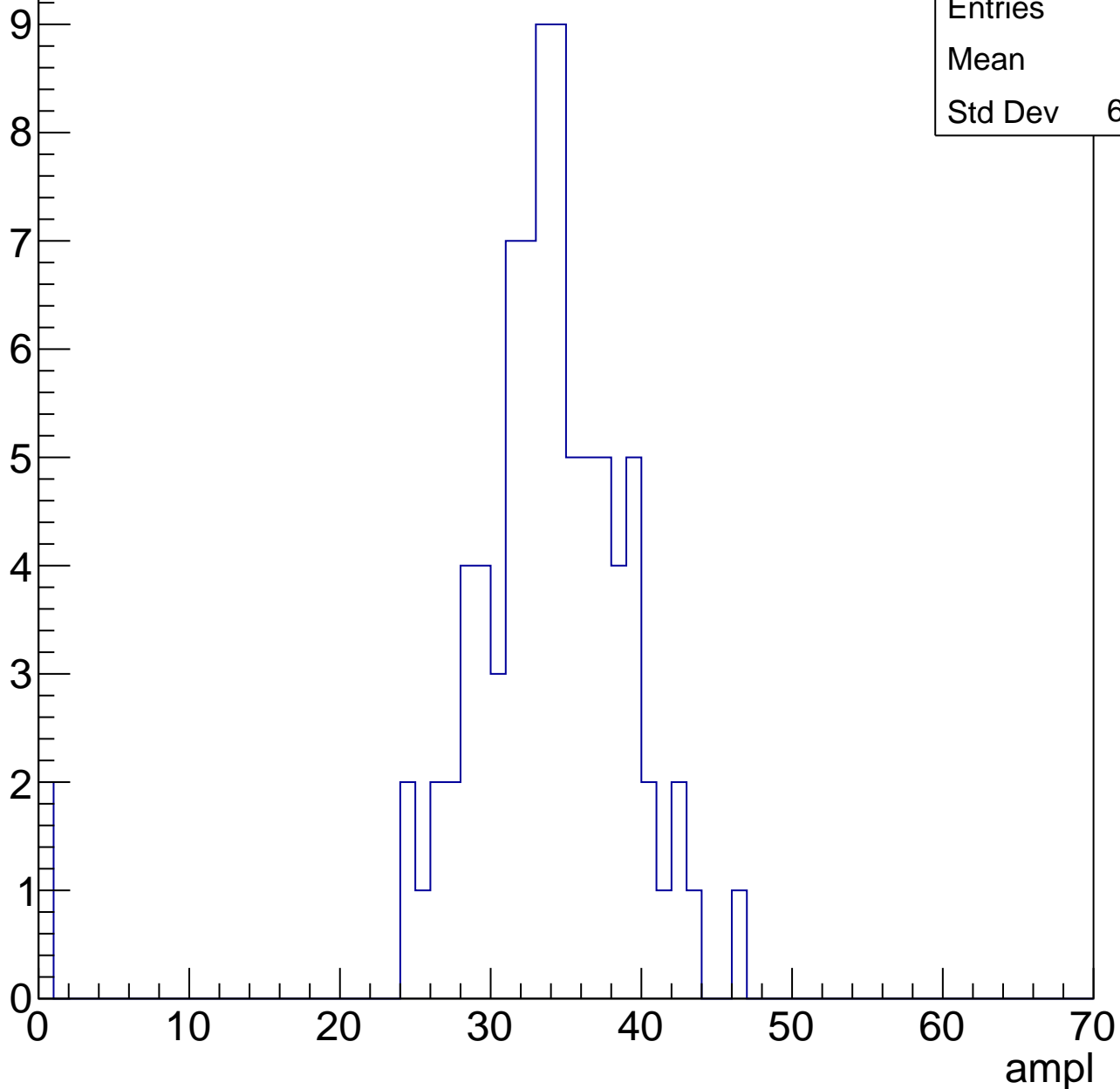


# B1L103S, U25-ch94, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	83
Mean	32.8
Std Dev	6.787

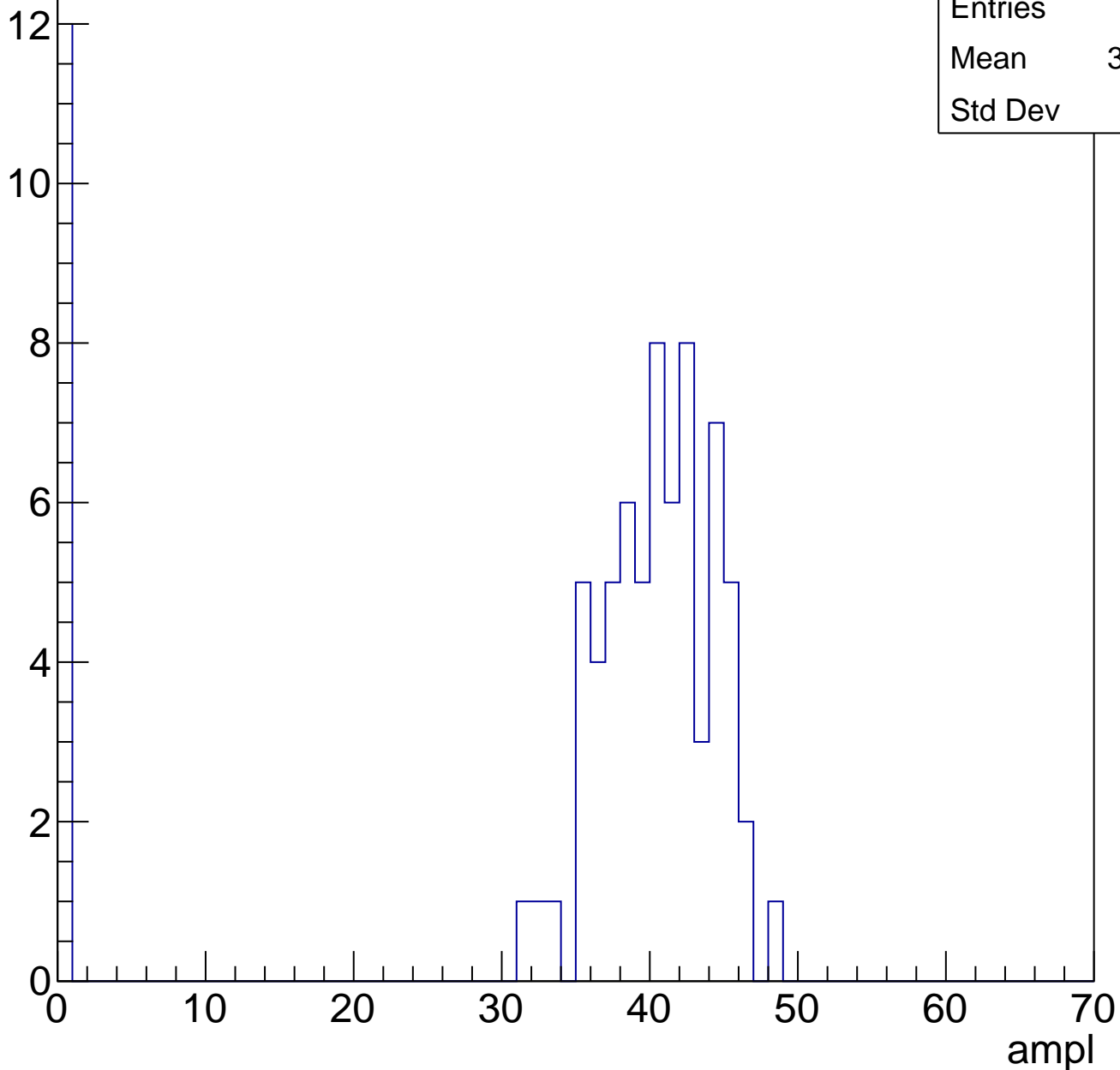


# B1L103S, U25-ch94, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	80
Mean	34.09
Std Dev	14.7

Entry

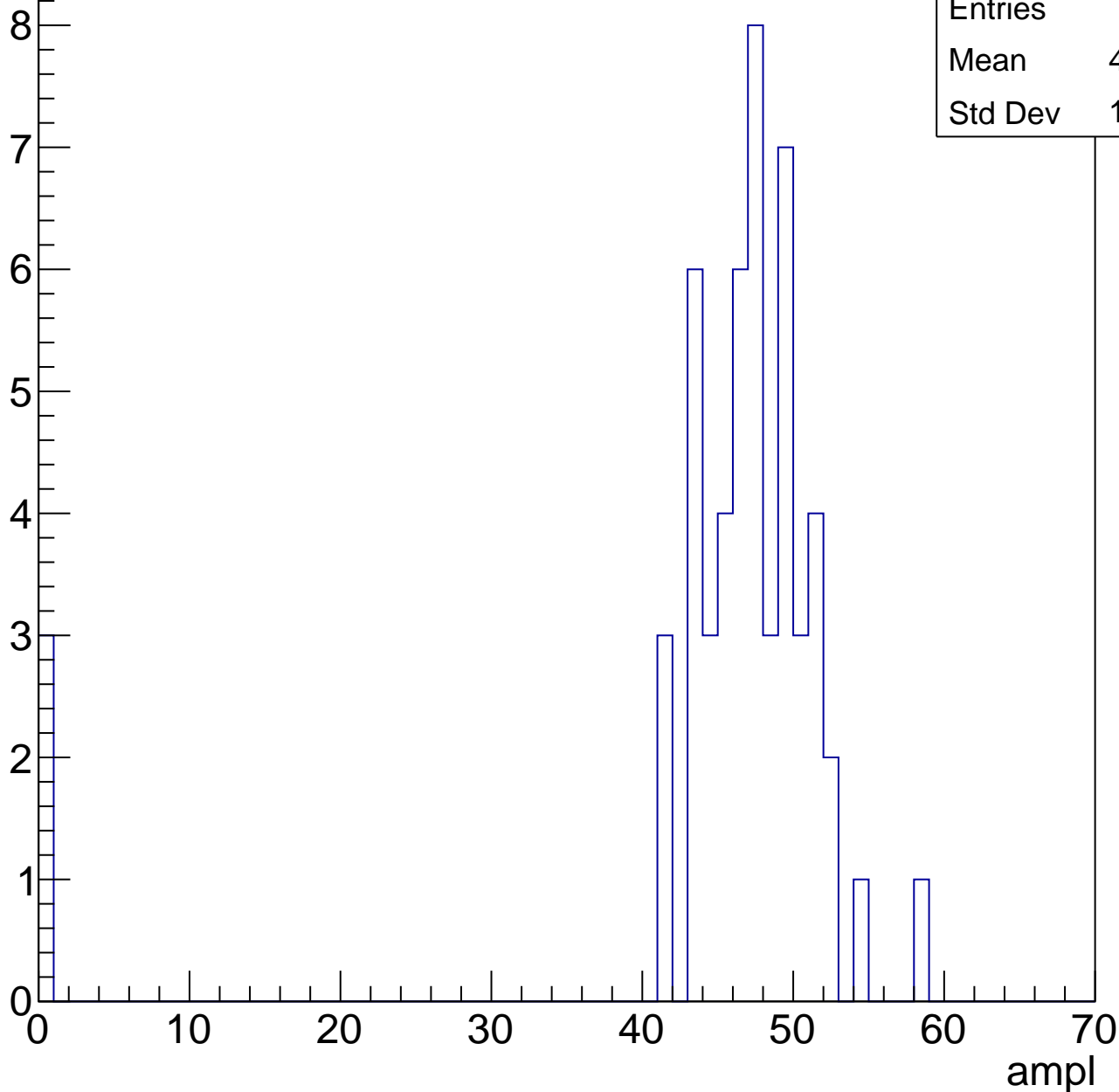


# B1L103S, U25-ch94, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	54
Mean	44.48
Std Dev	11.29

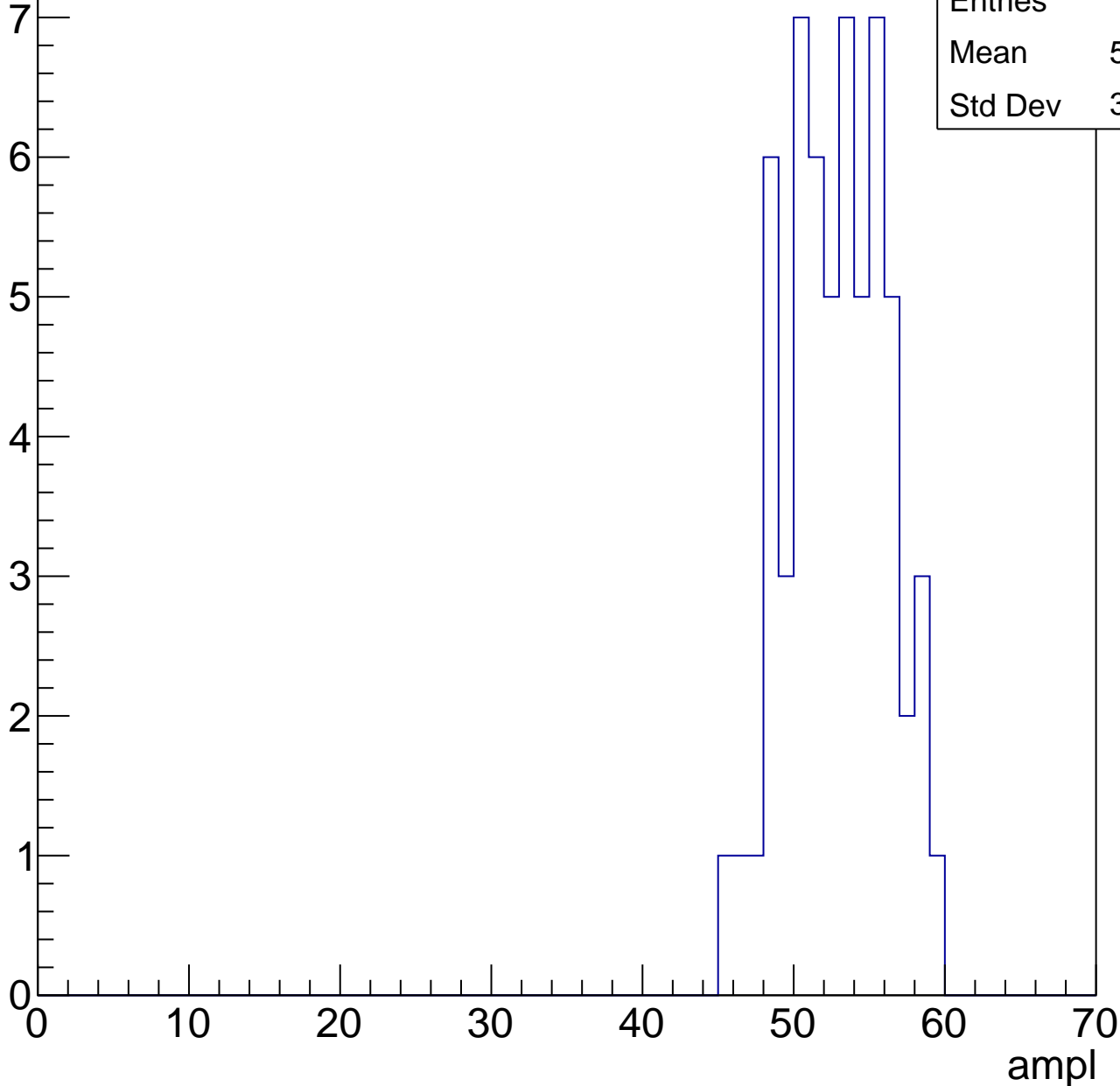


# B1L103S, U25-ch94, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	60
Mean	52.37
Std Dev	3.256



# B1L103S, U25-ch94, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

7

6

5

4

3

2

1

0

Entries 54

Mean 57.56

Std Dev 3.365

ampl

0

10

20

30

40

50

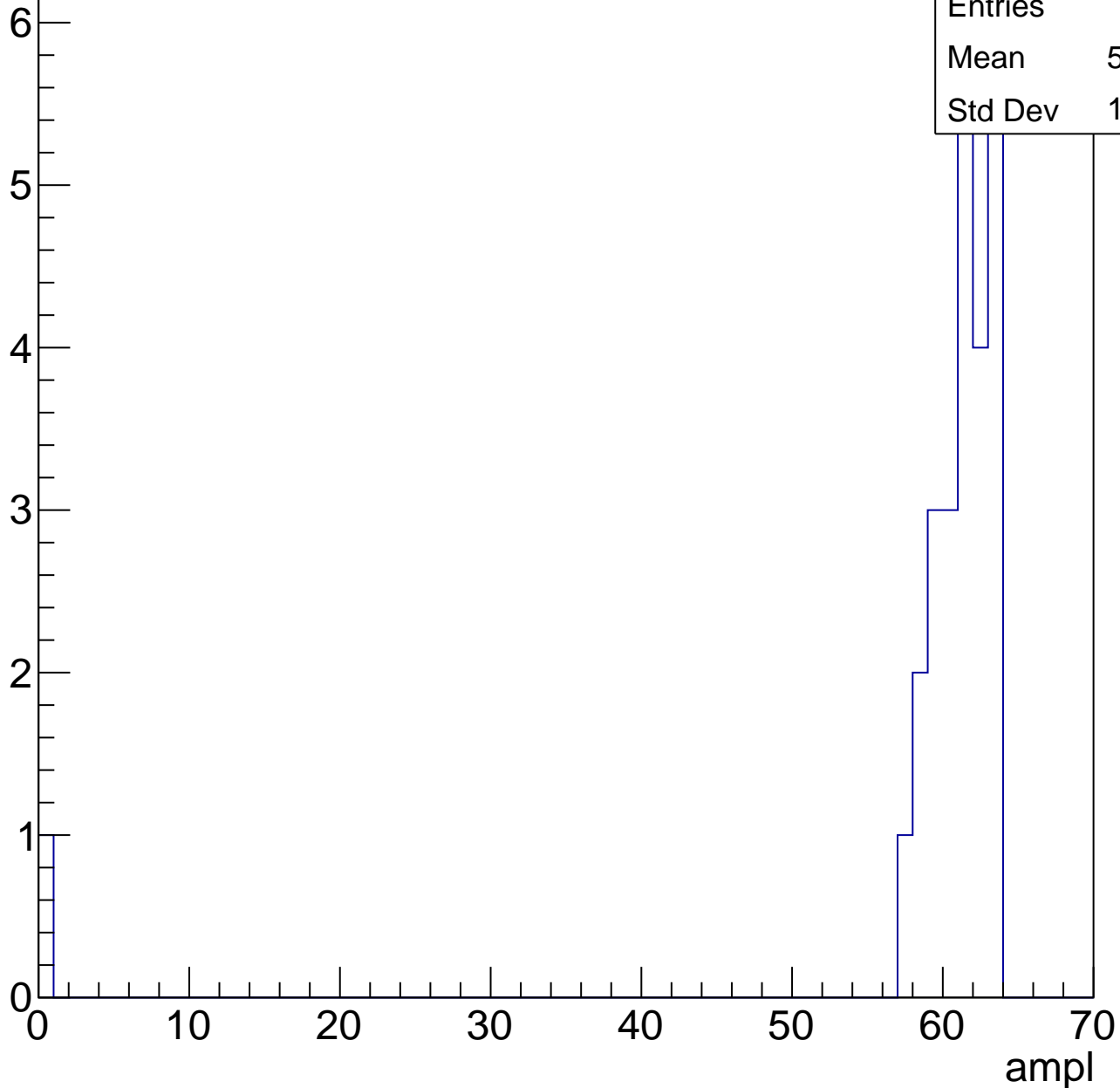
60

70

# B1L103S, U25-ch94, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



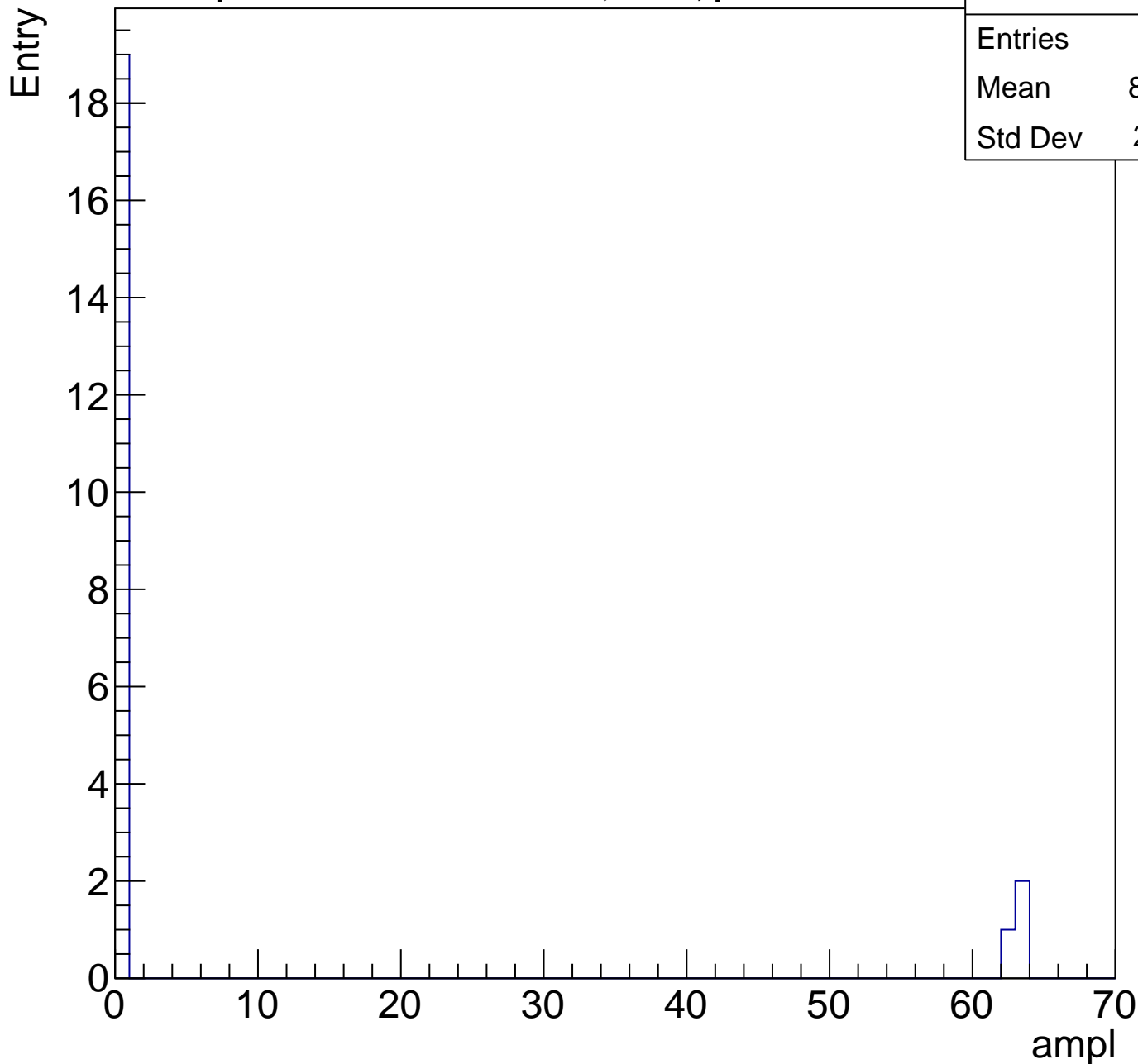
Entries	26
Mean	58.54
Std Dev	11.83



# B1L103S, U25-ch94, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	22
Mean	8.545
Std Dev	21.51

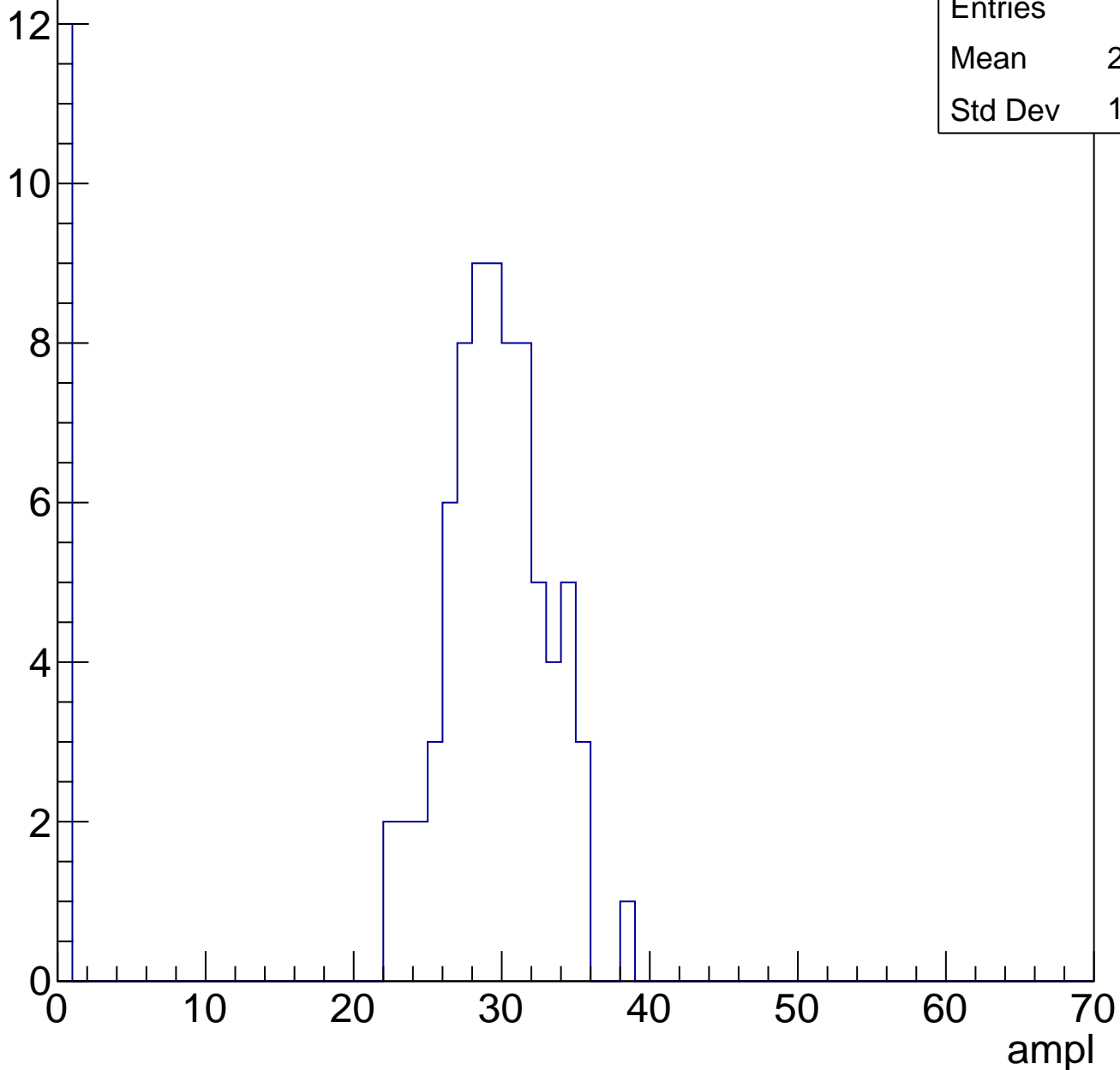


# B1L103S, U25-ch95, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	87
Mean	25.18
Std Dev	10.53

Entry

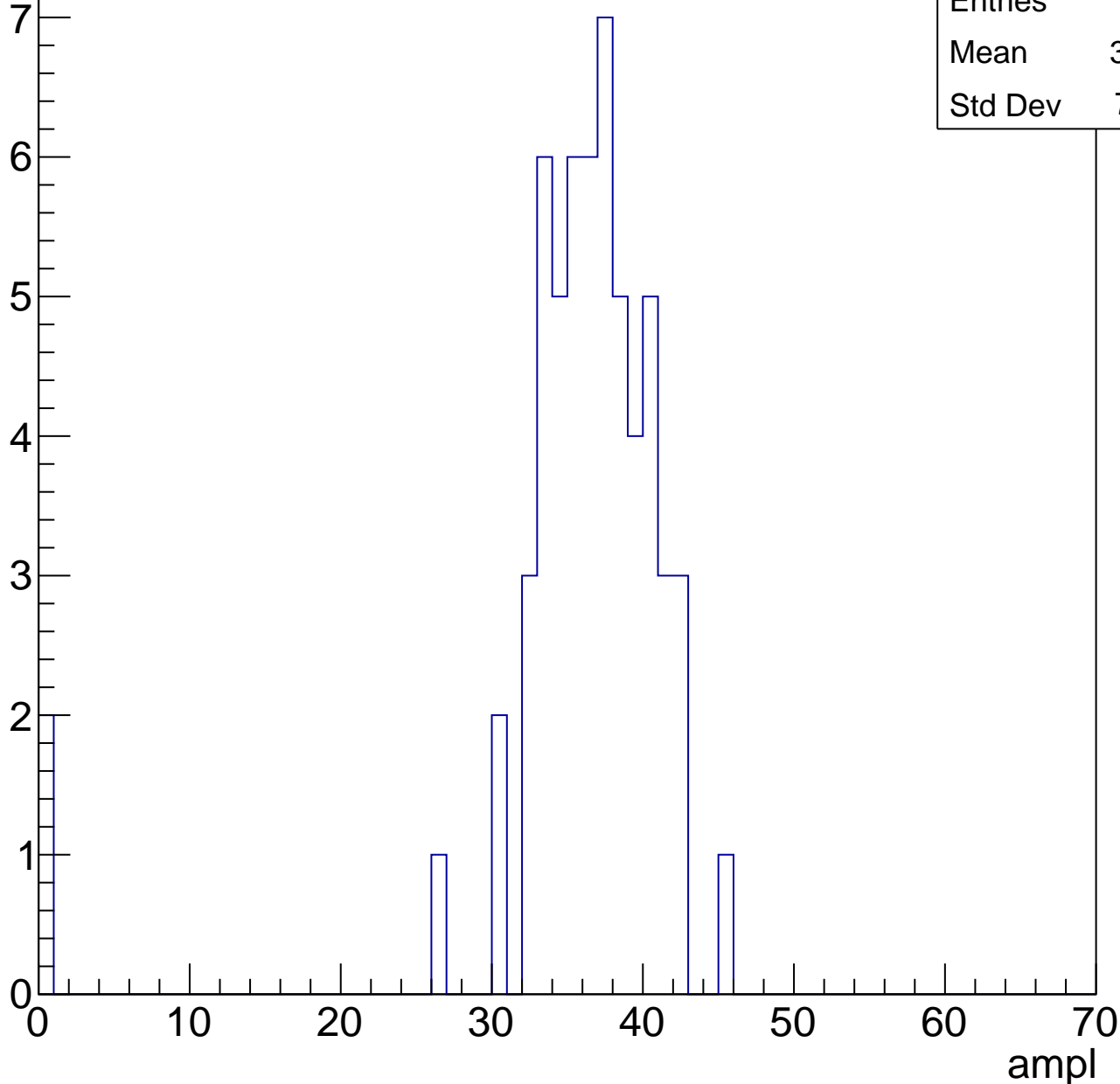


# B1L103S, U25-ch95, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	59
Mean	35.17
Std Dev	7.431

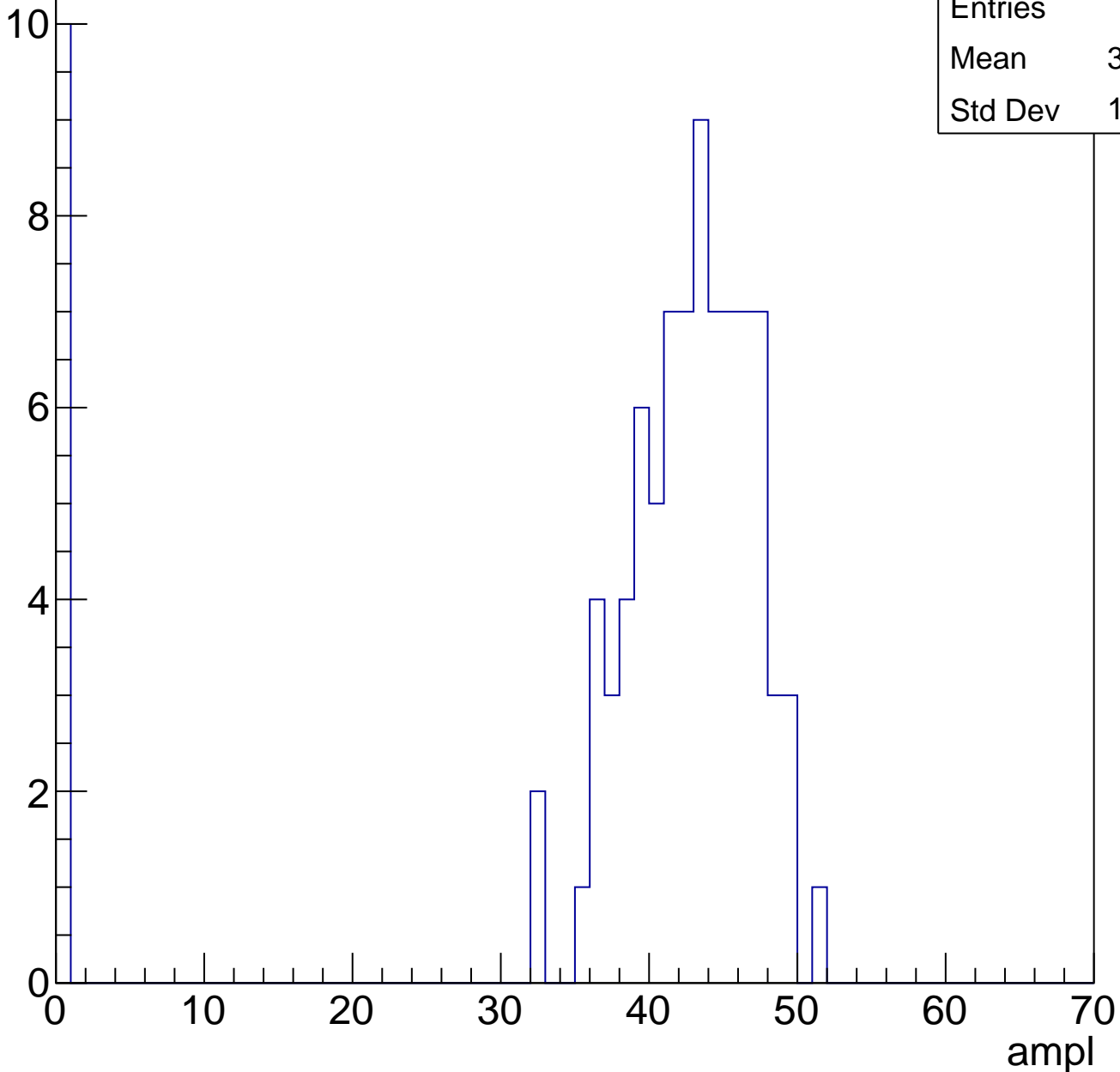


# B1L103S, U25-ch95, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	93
Mean	37.89
Std Dev	13.68

Entry

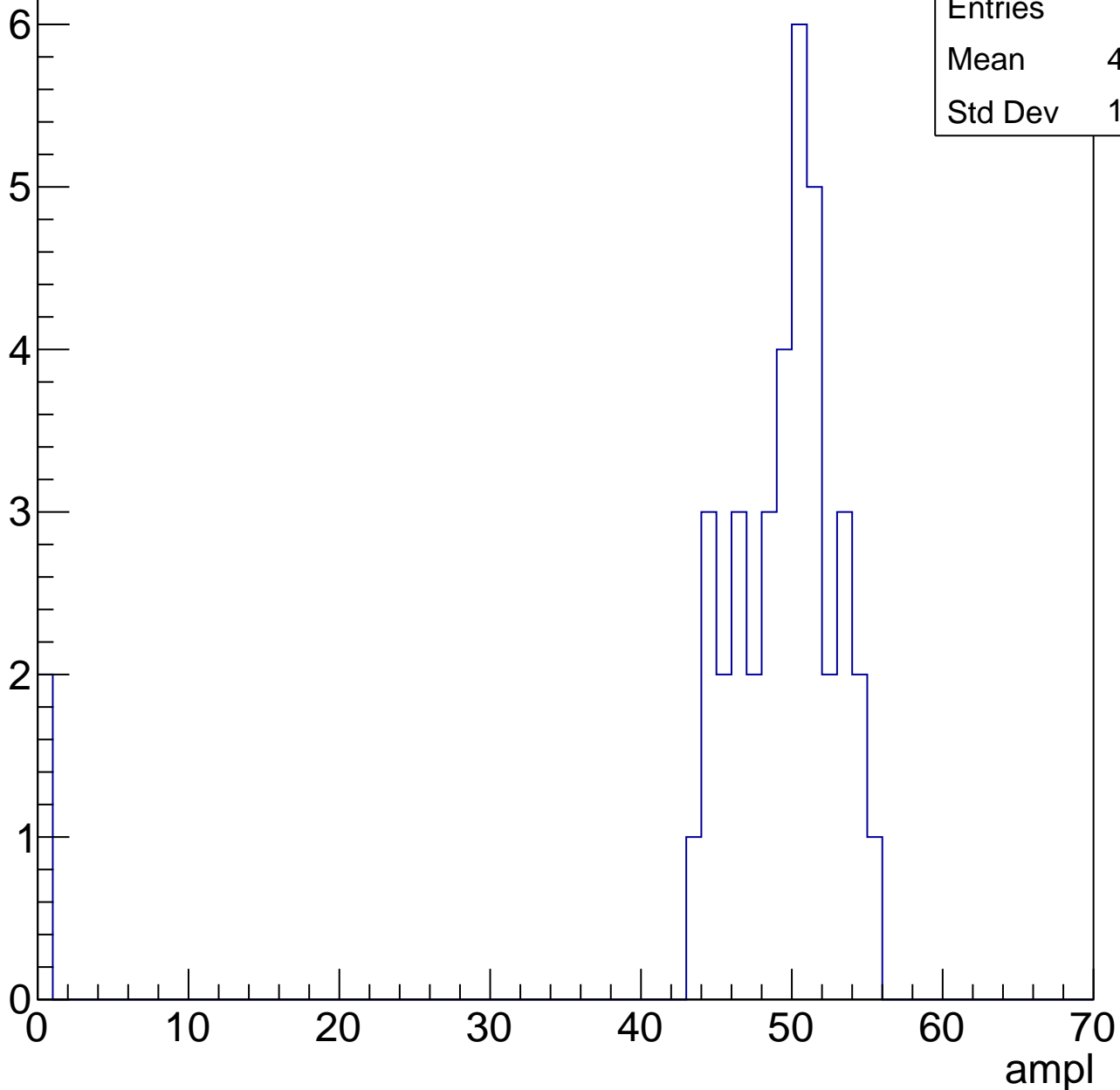


# B1L103S, U25-ch95, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	39
Mean	46.62
Std Dev	11.25

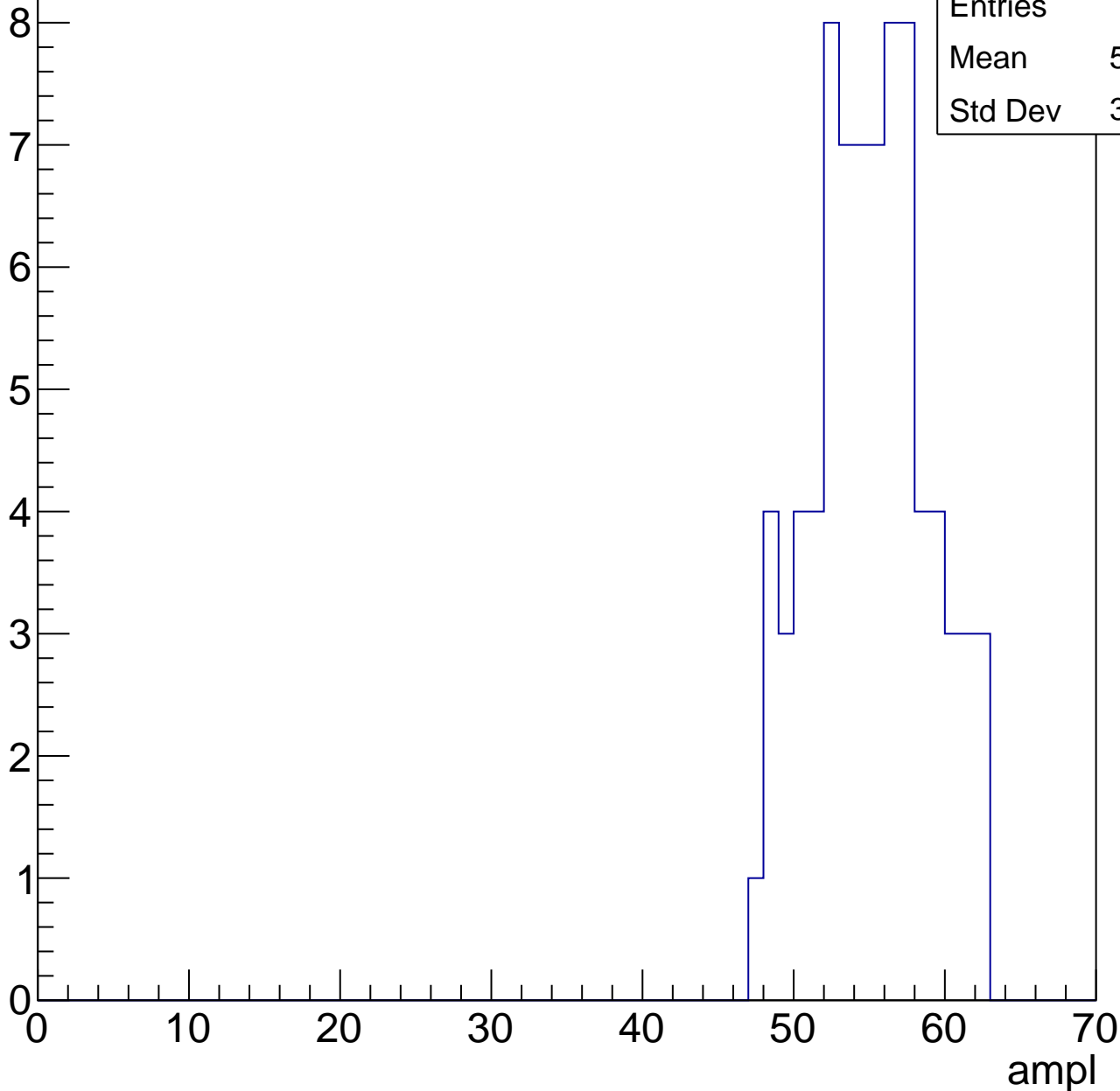


# B1L103S, U25-ch95, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	78
Mean	54.63
Std Dev	3.752

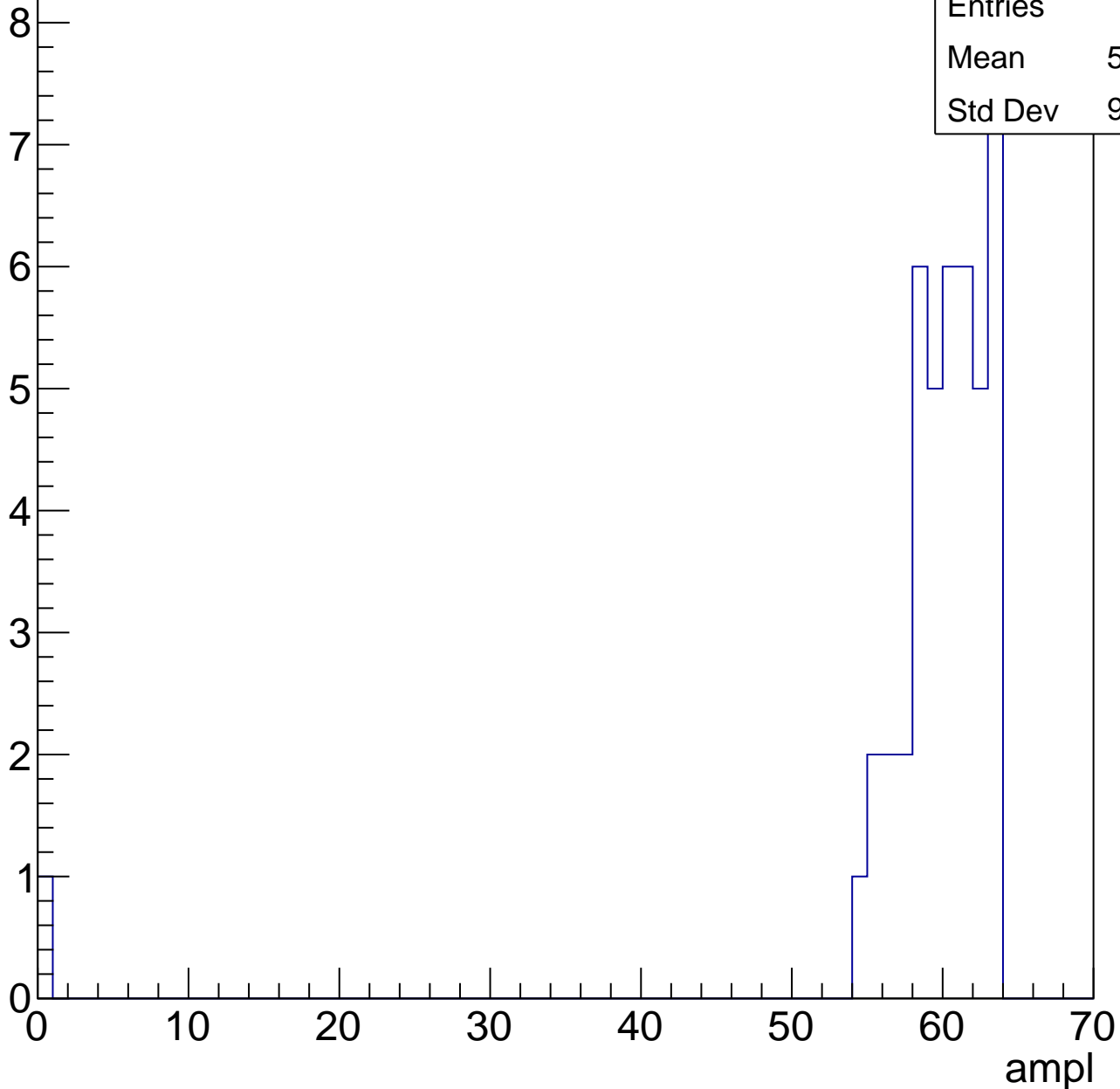


# B1L103S, U25-ch95, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

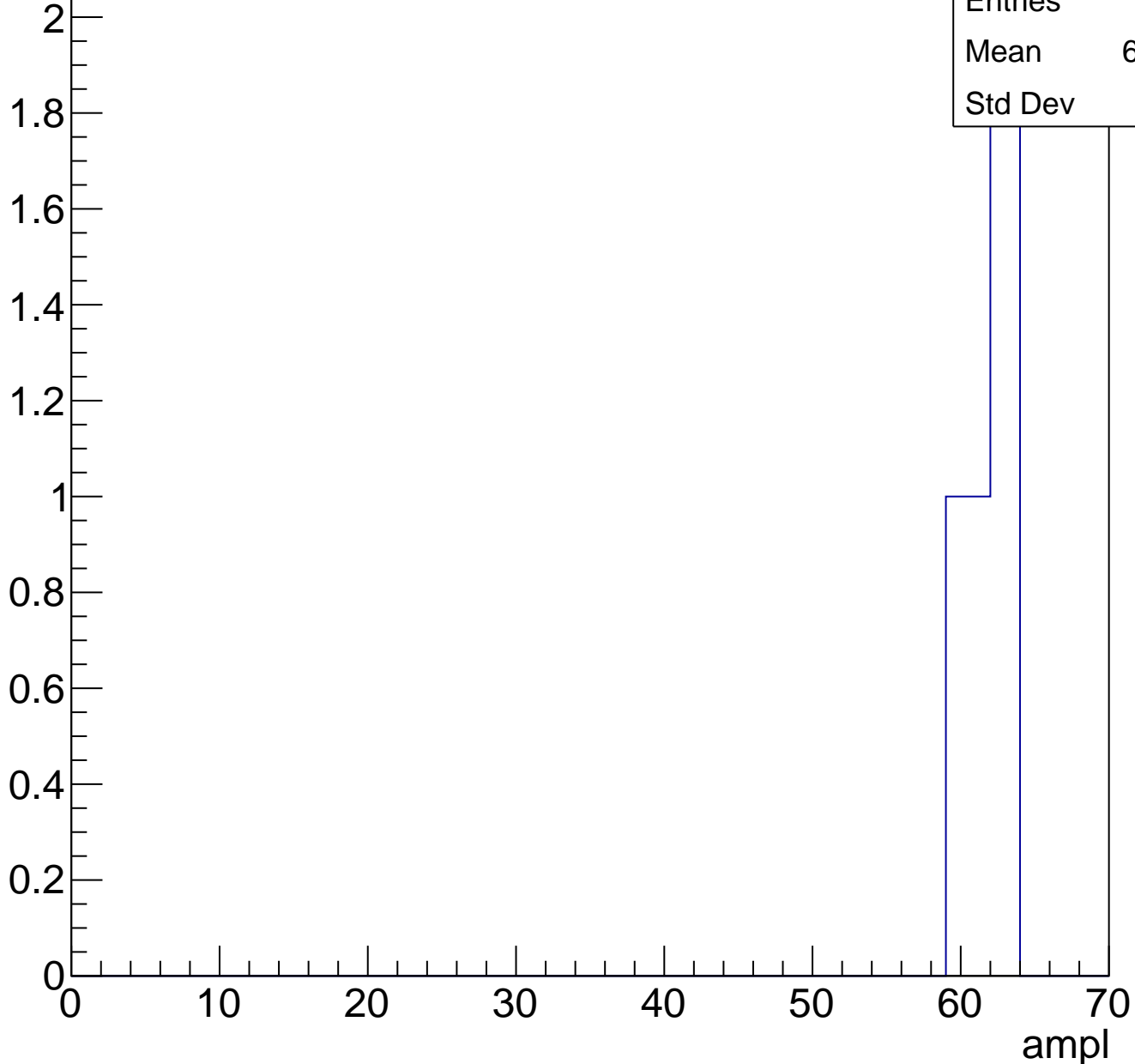
Entries	44
Mean	58.48
Std Dev	9.245



# B1L103S, U25-ch95, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



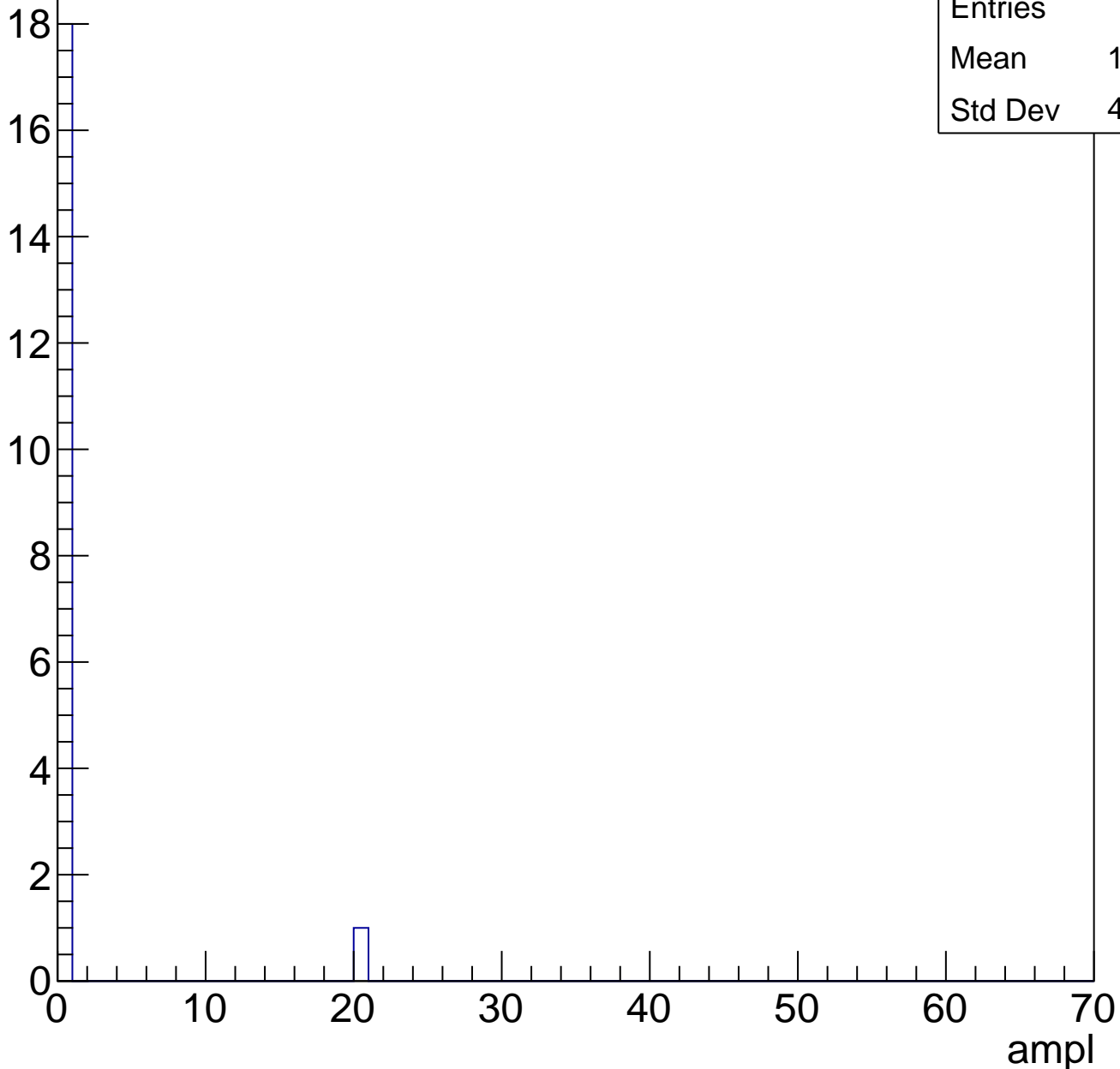


# B1L103S, U25-ch95, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	19
Mean	1.053
Std Dev	4.466

Entry

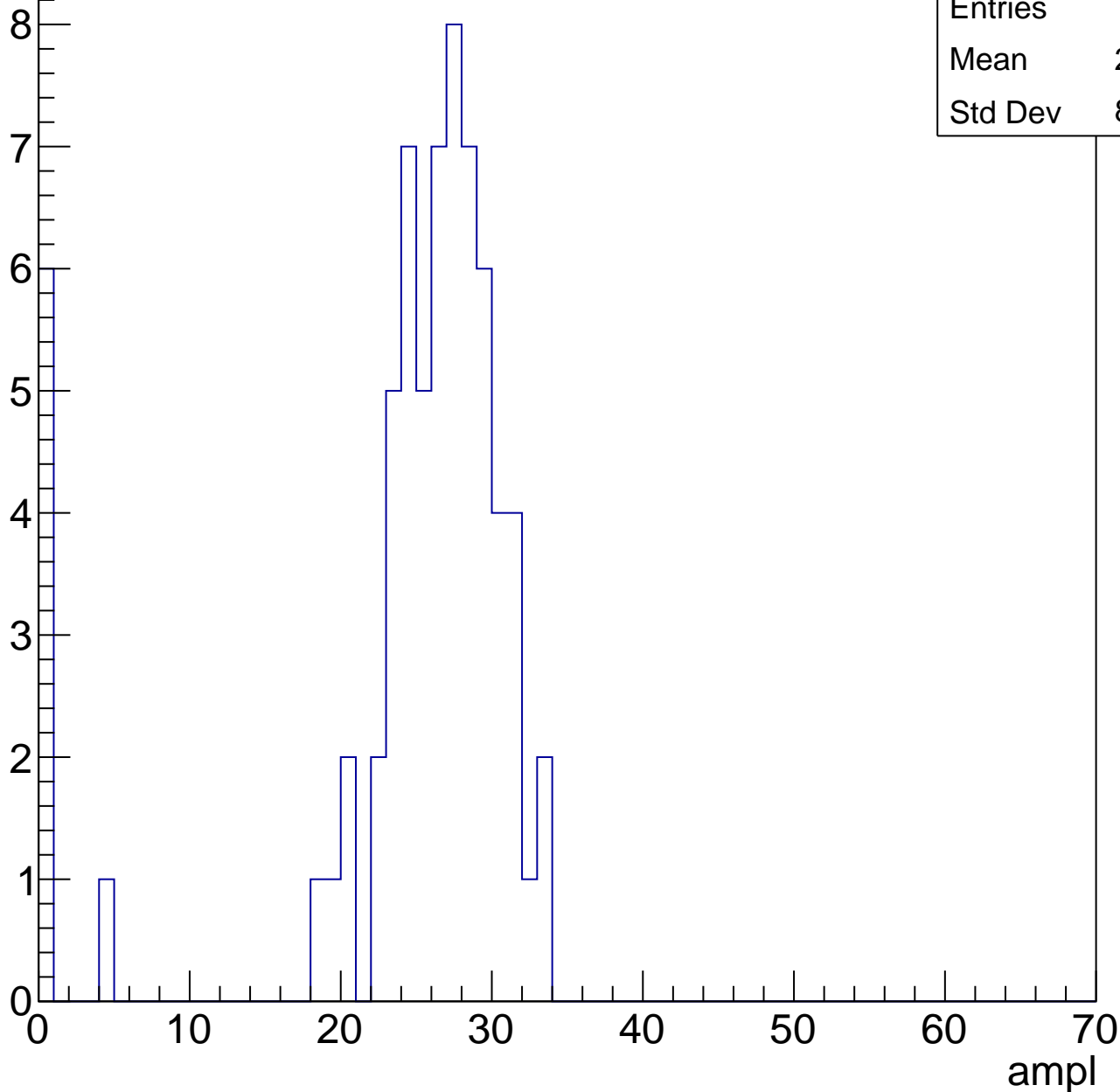


# B1L103S, U25-ch96, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	69
Mean	23.81
Std Dev	8.421

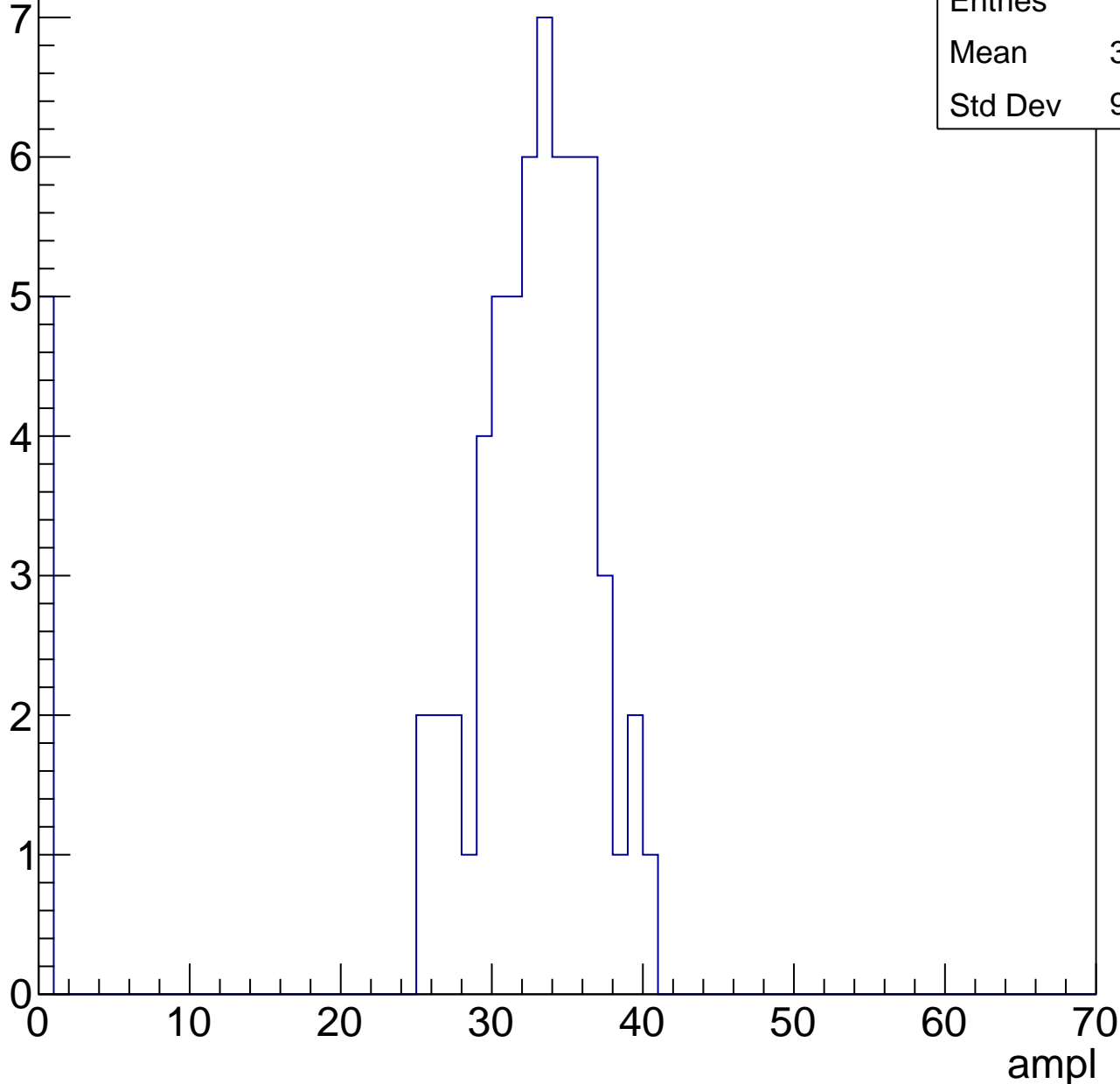


# B1L103S, U25-ch96, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	64
Mean	30.08
Std Dev	9.383

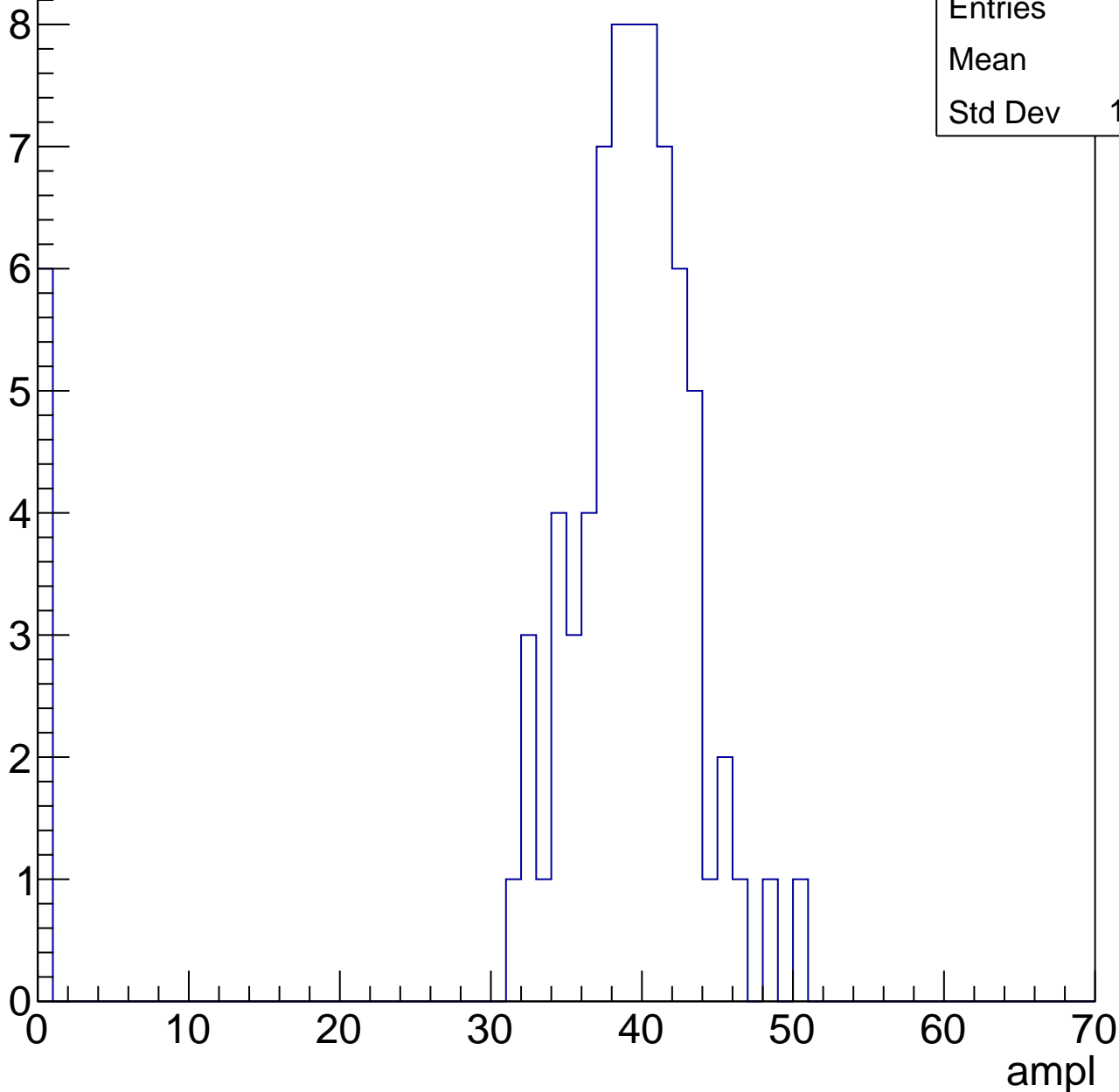


# B1L103S, U25-ch96, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	77
Mean	36
Std Dev	11.06

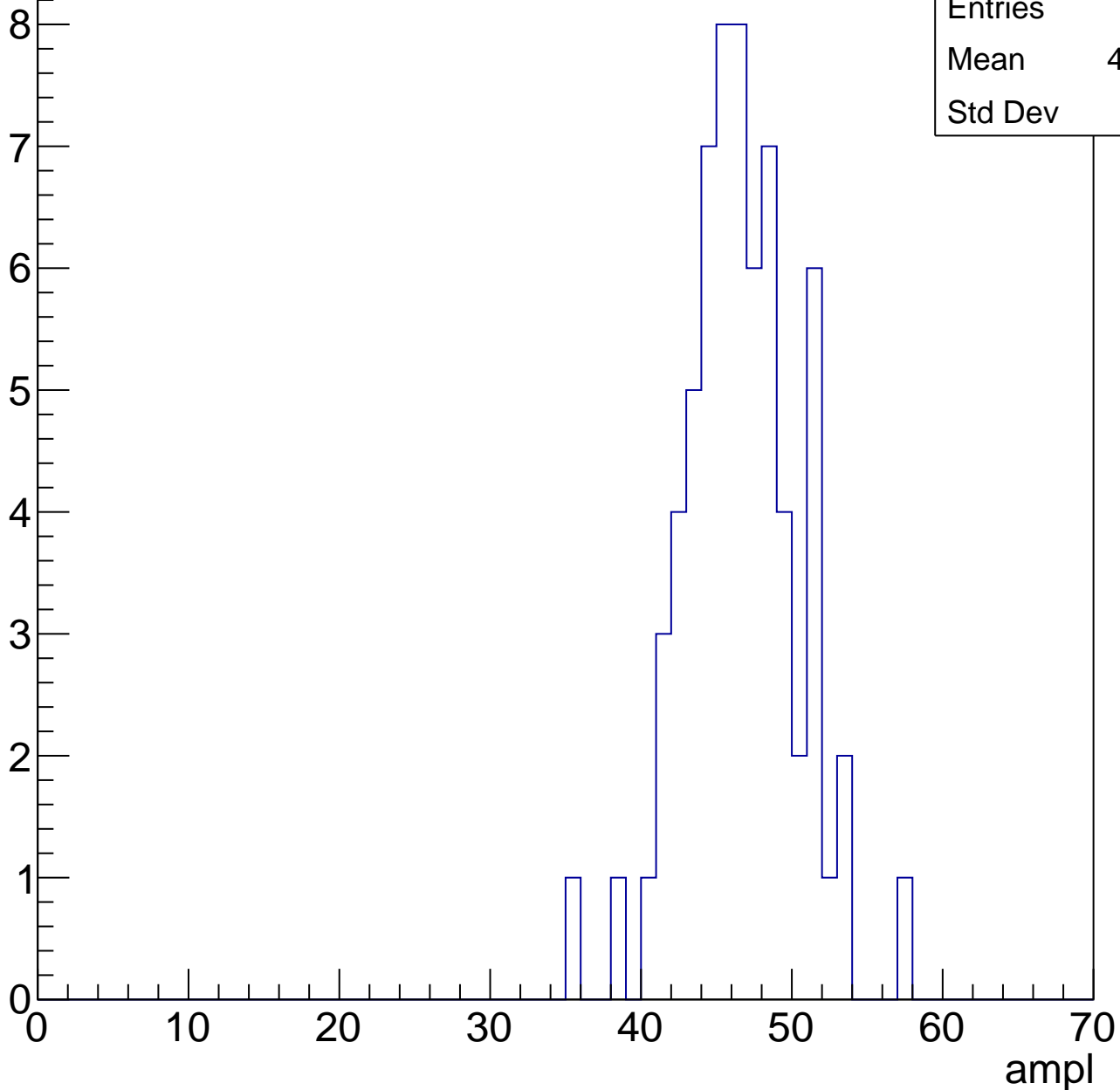


# B1L103S, U25-ch96, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	67
Mean	46.12
Std Dev	3.76

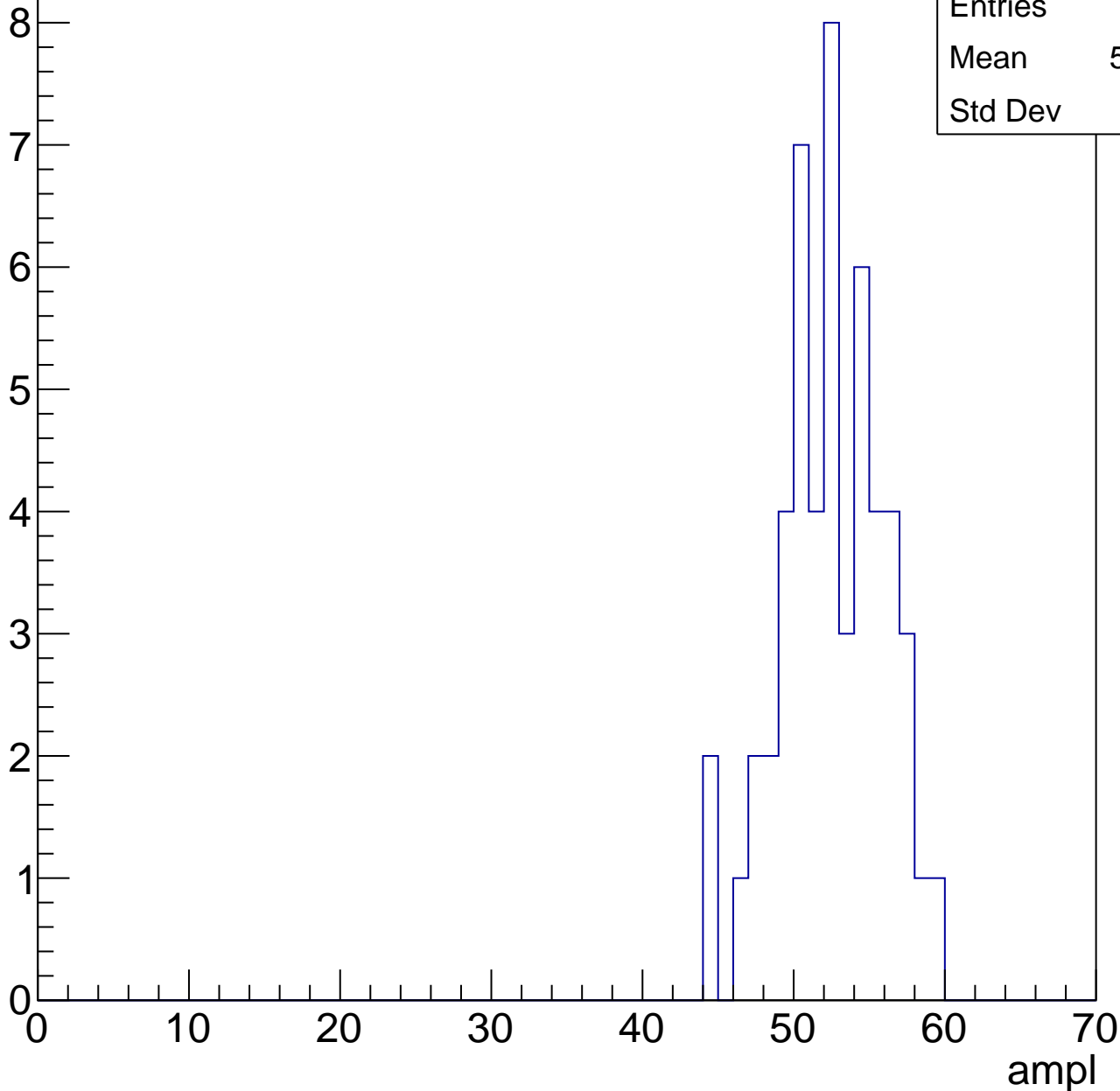


# B1L103S, U25-ch96, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	52
Mean	52.02
Std Dev	3.4

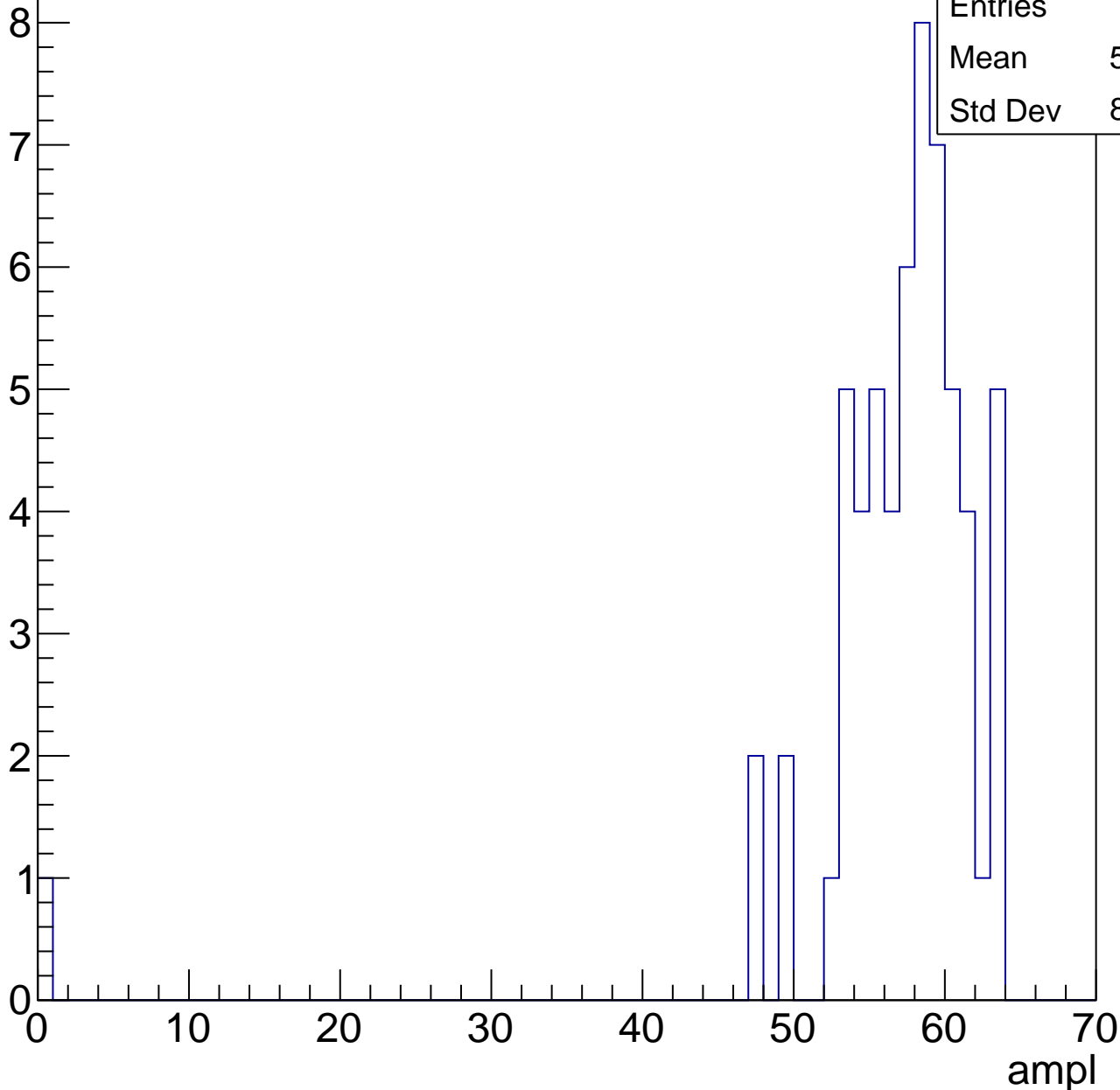


# B1L103S, U25-ch96, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	60
Mean	56.07
Std Dev	8.205

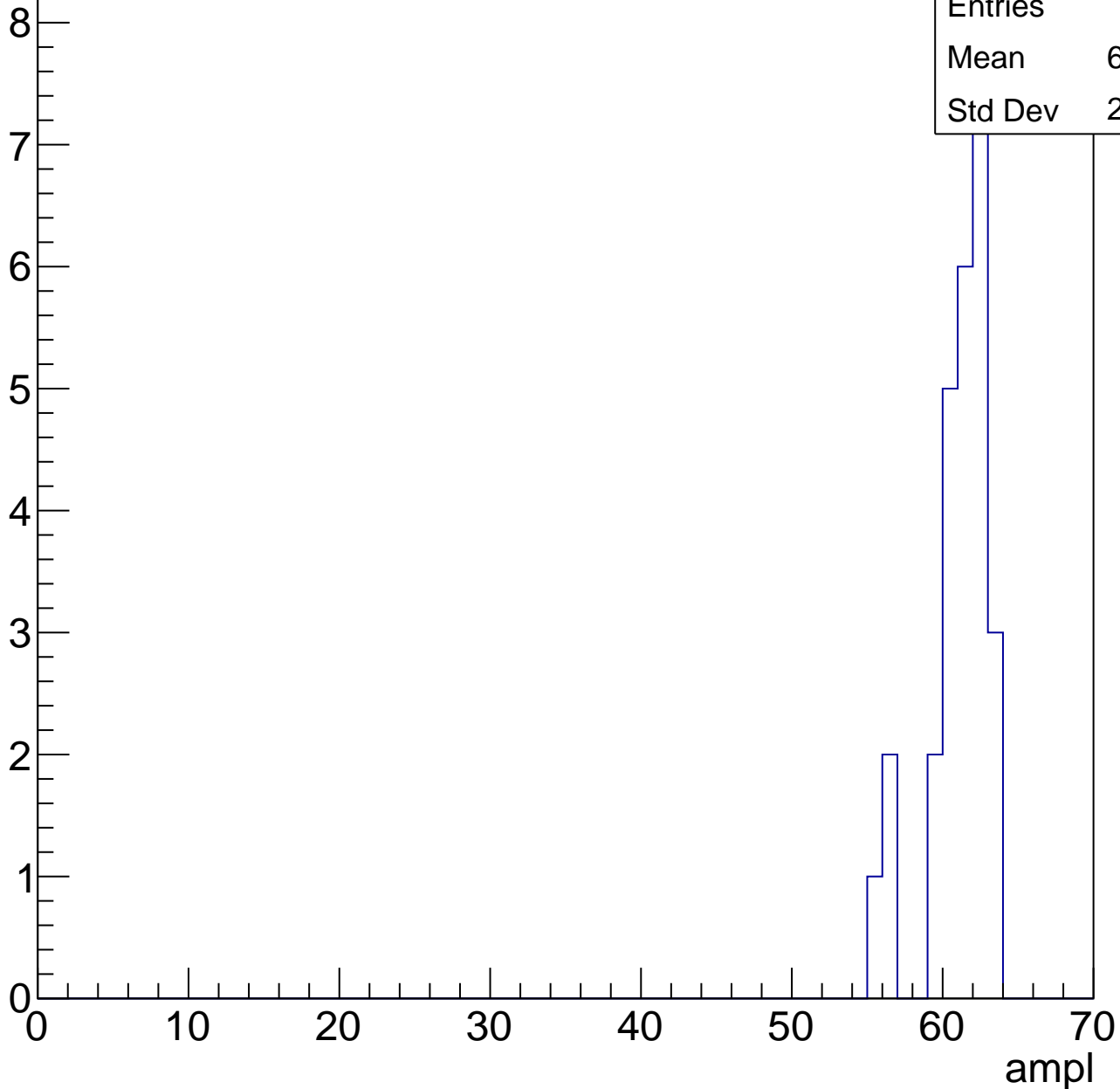


# B1L103S, U25-ch96, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	27
Mean	60.59
Std Dev	2.059



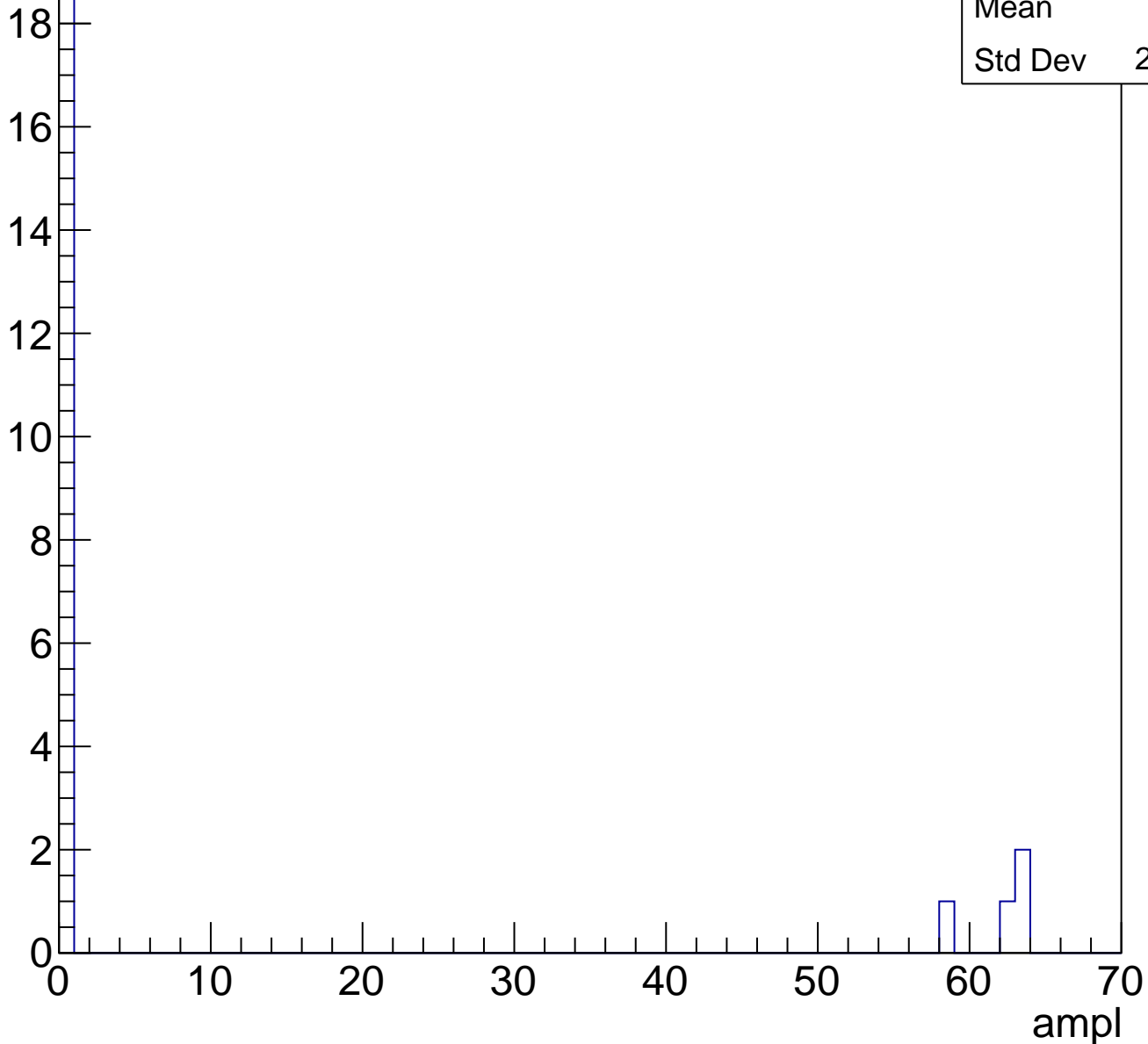


# B1L103S, U25-ch96, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	23
Mean	10.7
Std Dev	23.33

Entry

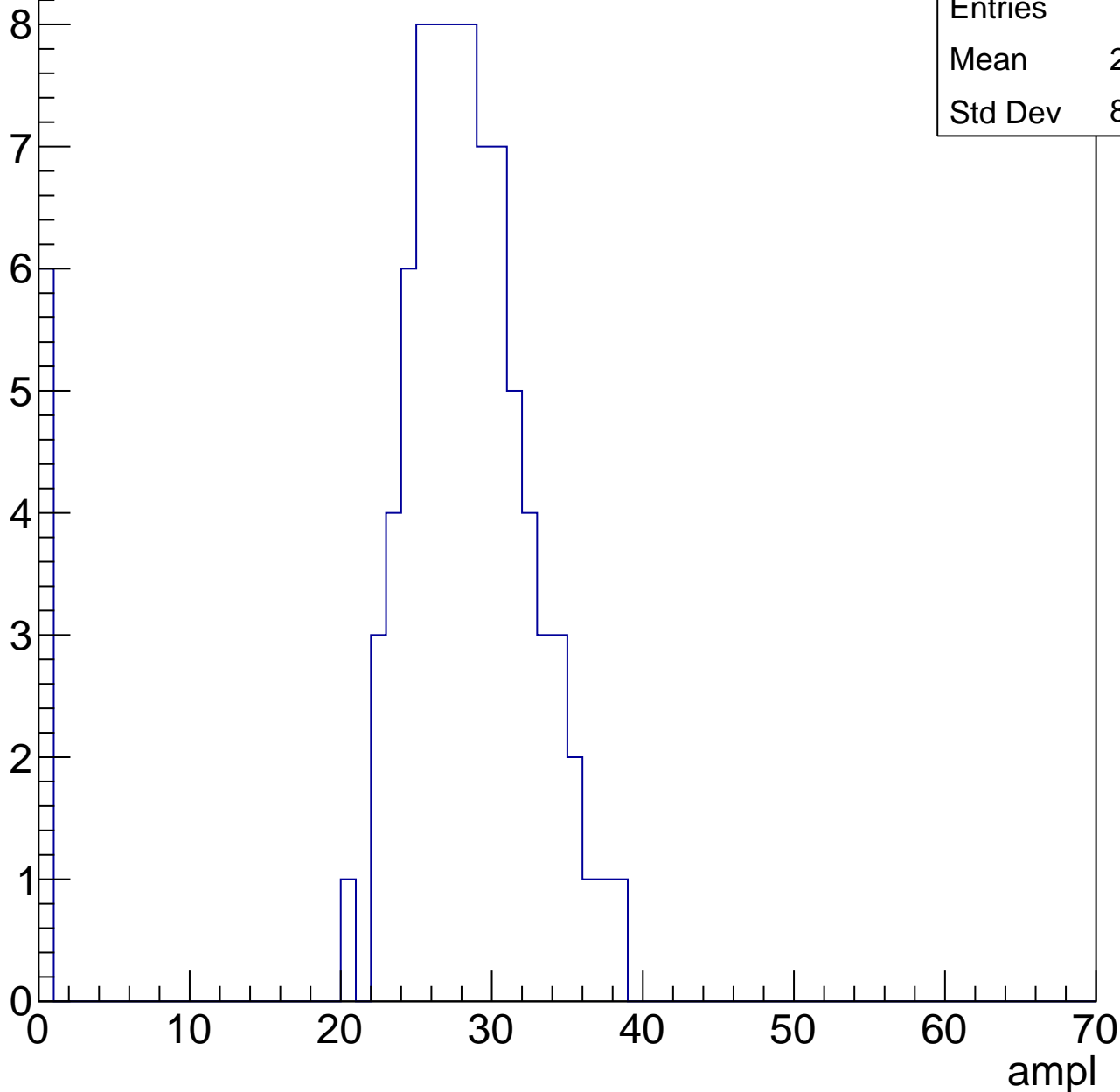


# B1L103S, U25-ch97, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	86
Mean	26.14
Std Dev	8.038

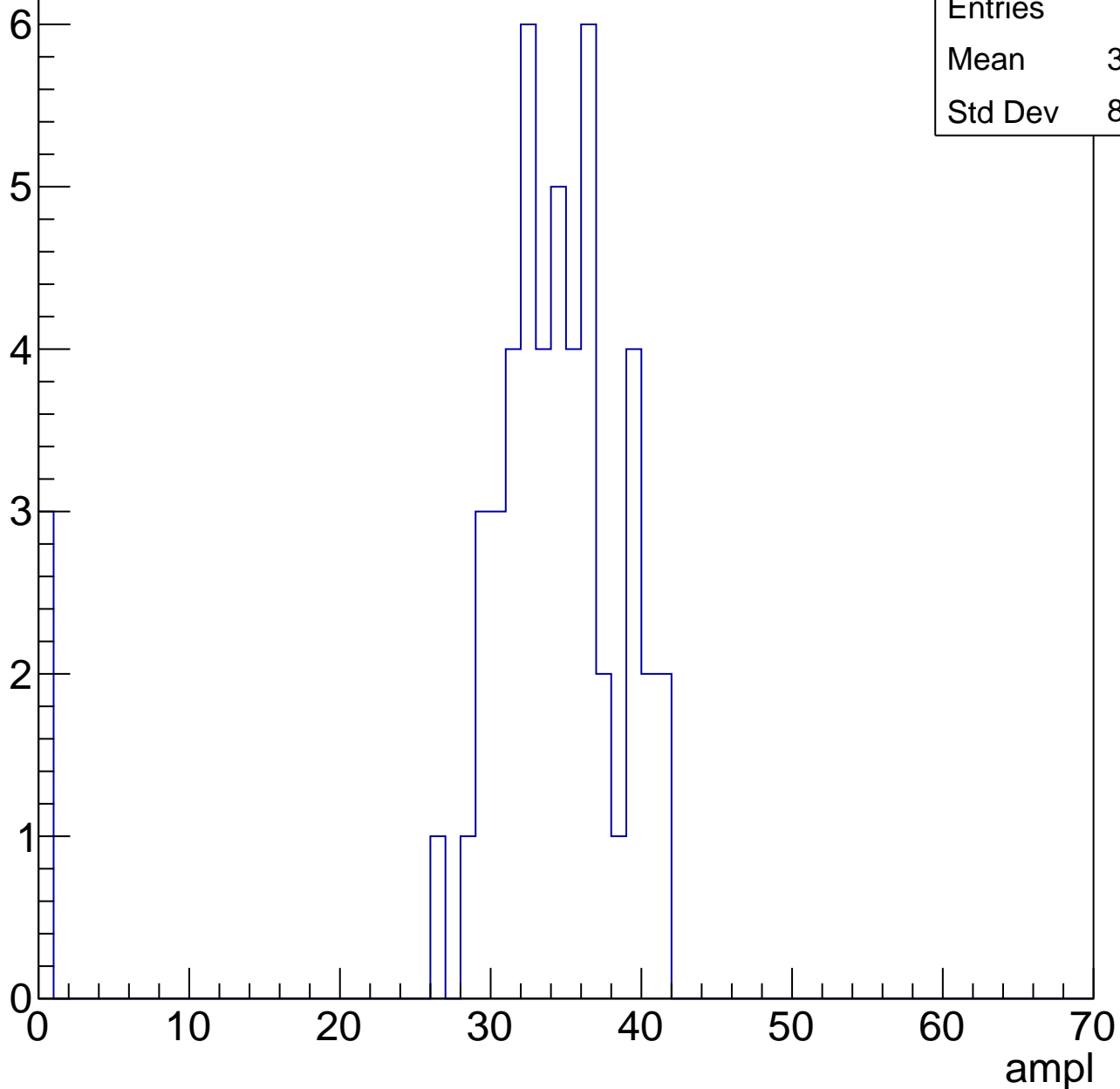


# B1L103S, U25-ch97, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	51
Mean	32.06
Std Dev	8.739

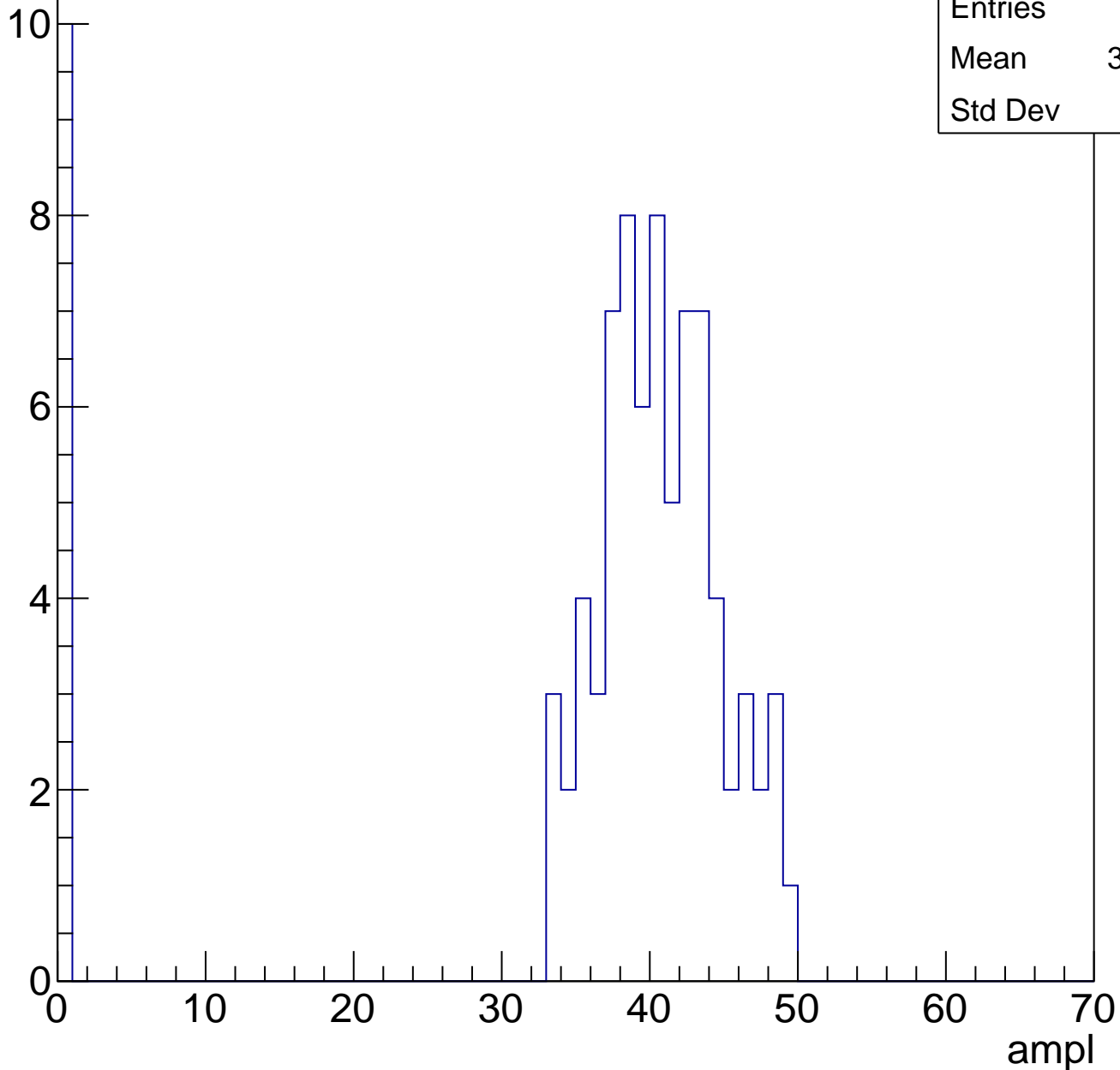


# B1L103S, U25-ch97, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	85
Mean	35.56
Std Dev	13.5

Entry

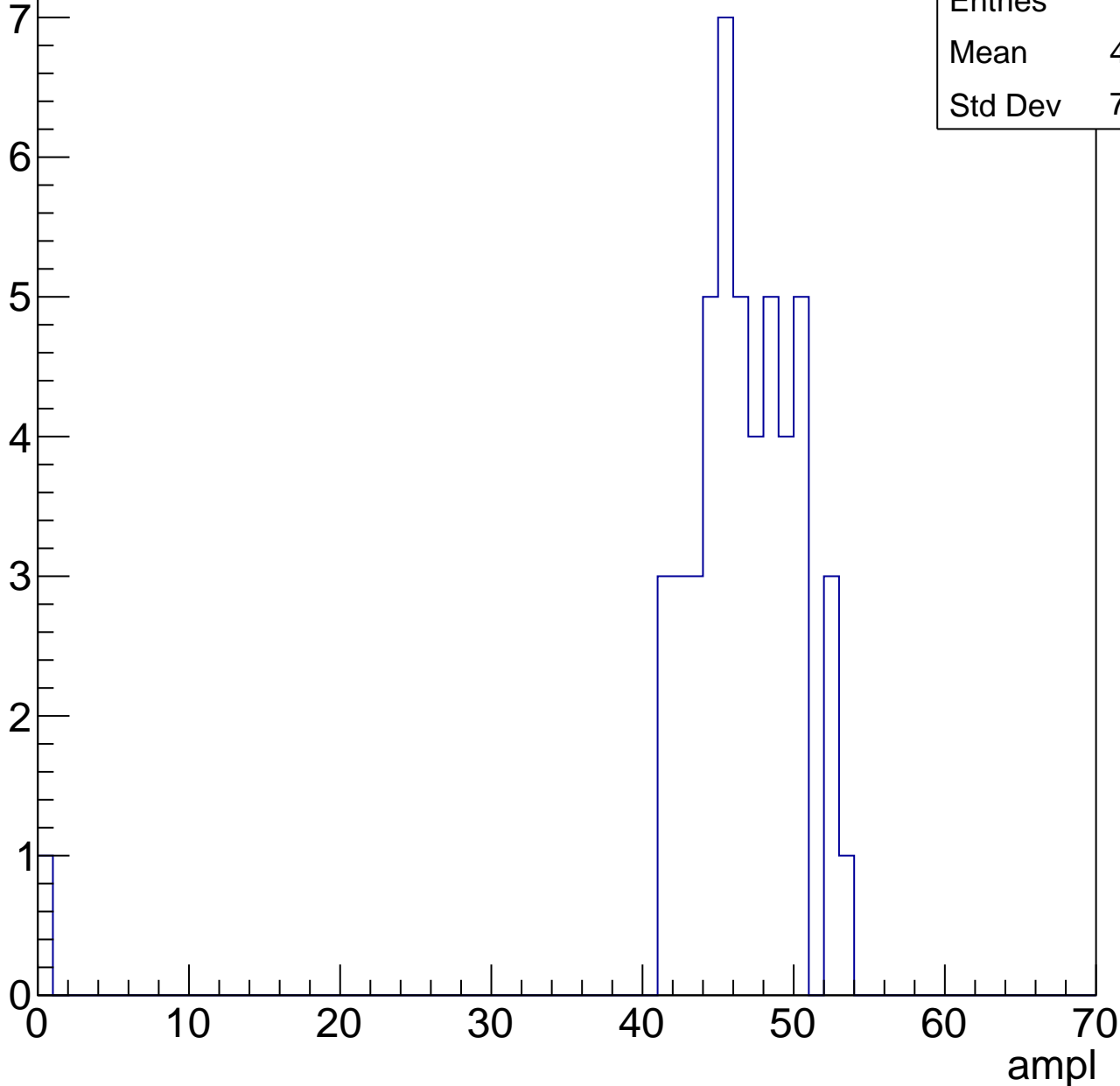


# B1L103S, U25-ch97, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	49
Mean	45.43
Std Dev	7.248

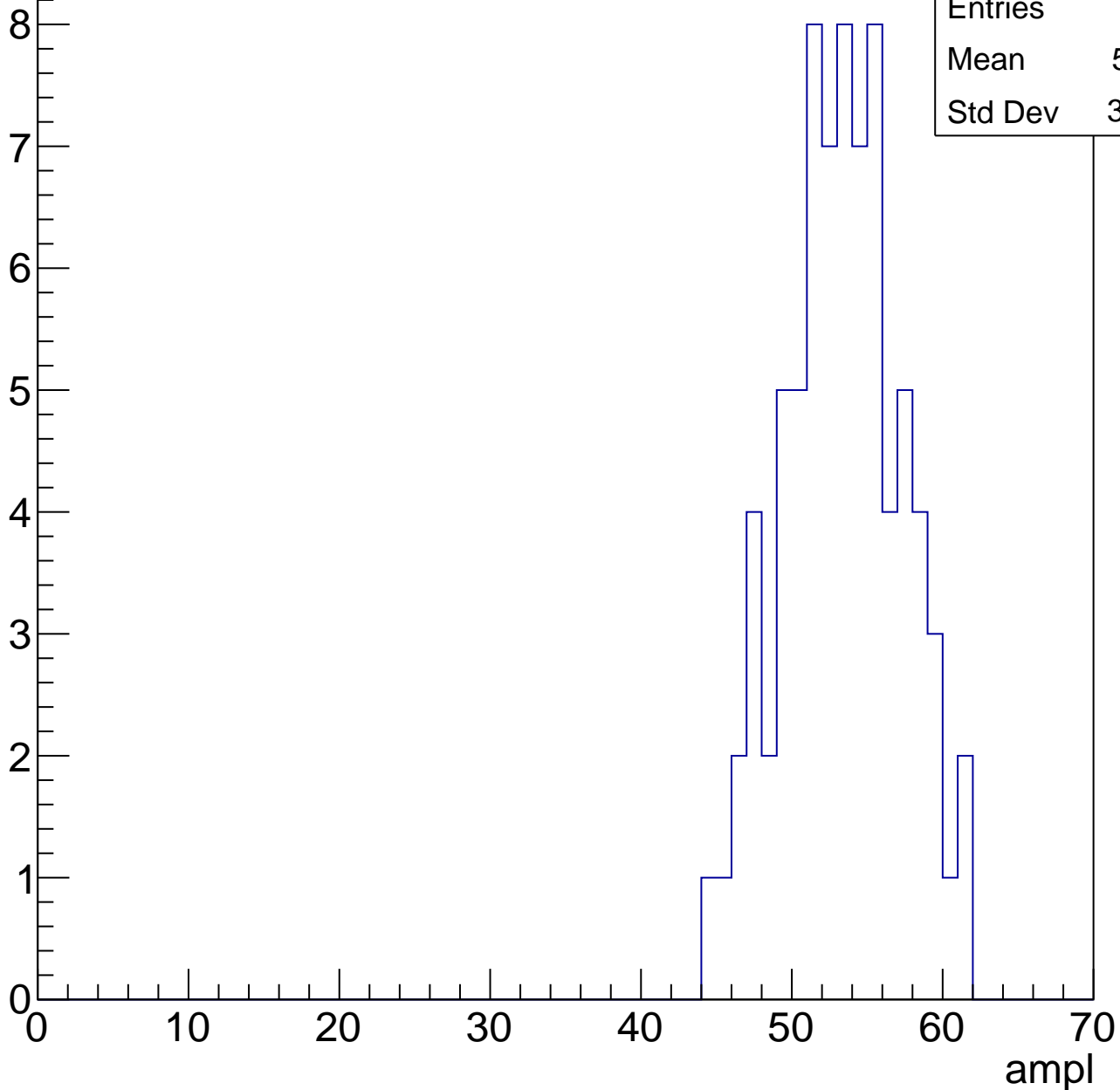


# B1L103S, U25-ch97, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	77
Mean	52.91
Std Dev	3.848

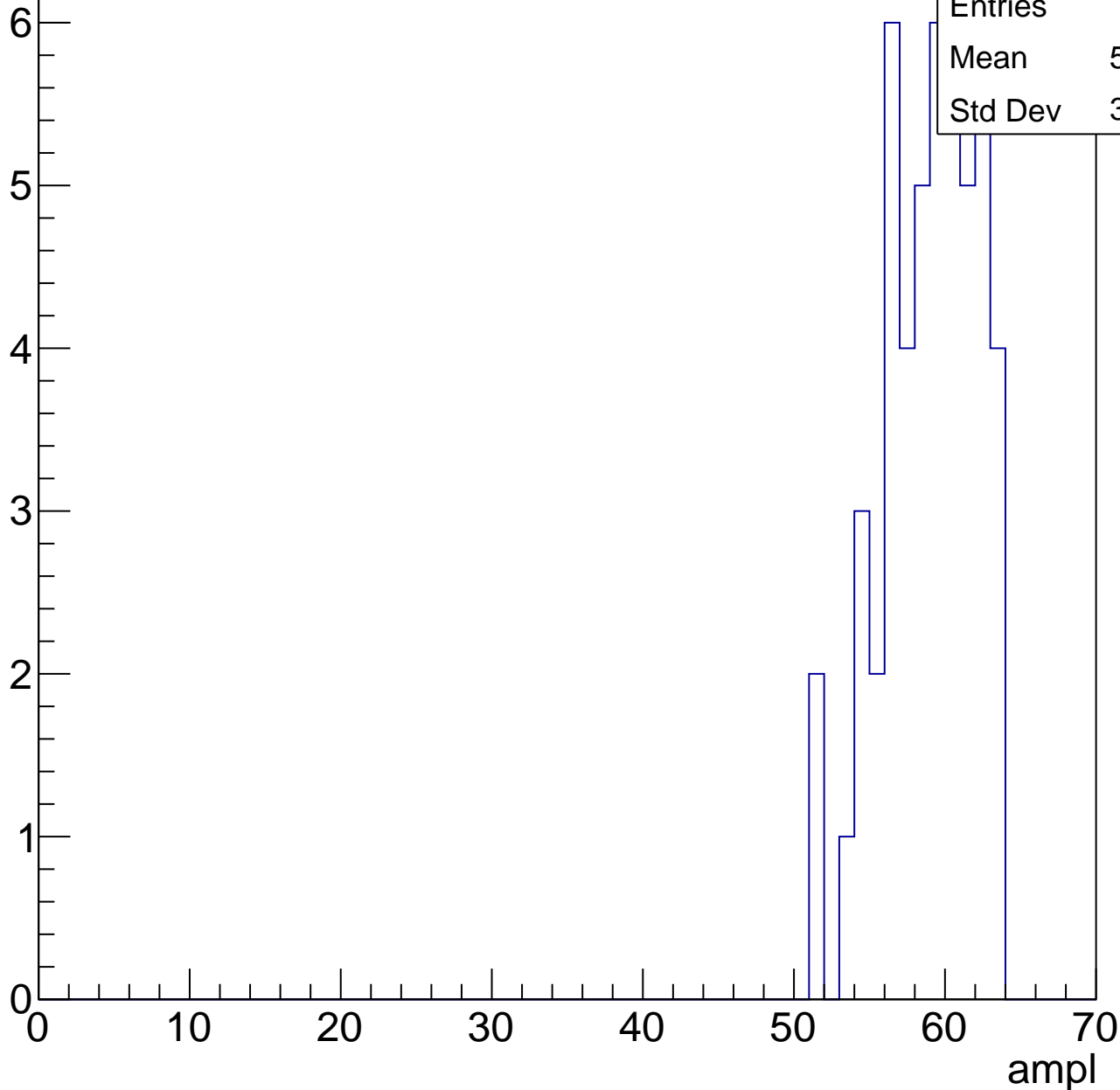


# B1L103S, U25-ch97, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	50
Mean	58.48
Std Dev	3.087

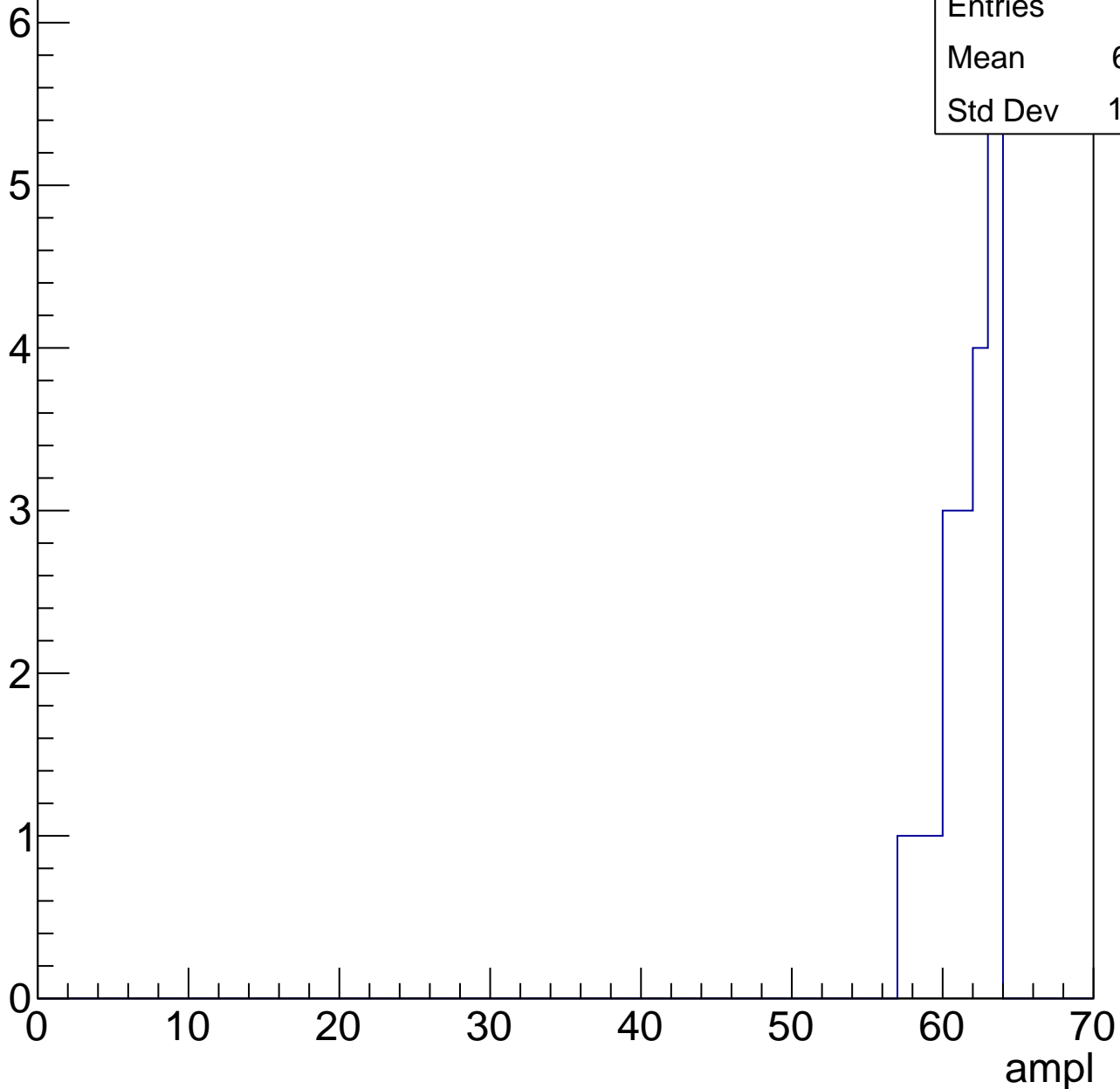


# B1L103S, U25-ch97, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	19
Mean	61.21
Std Dev	1.765



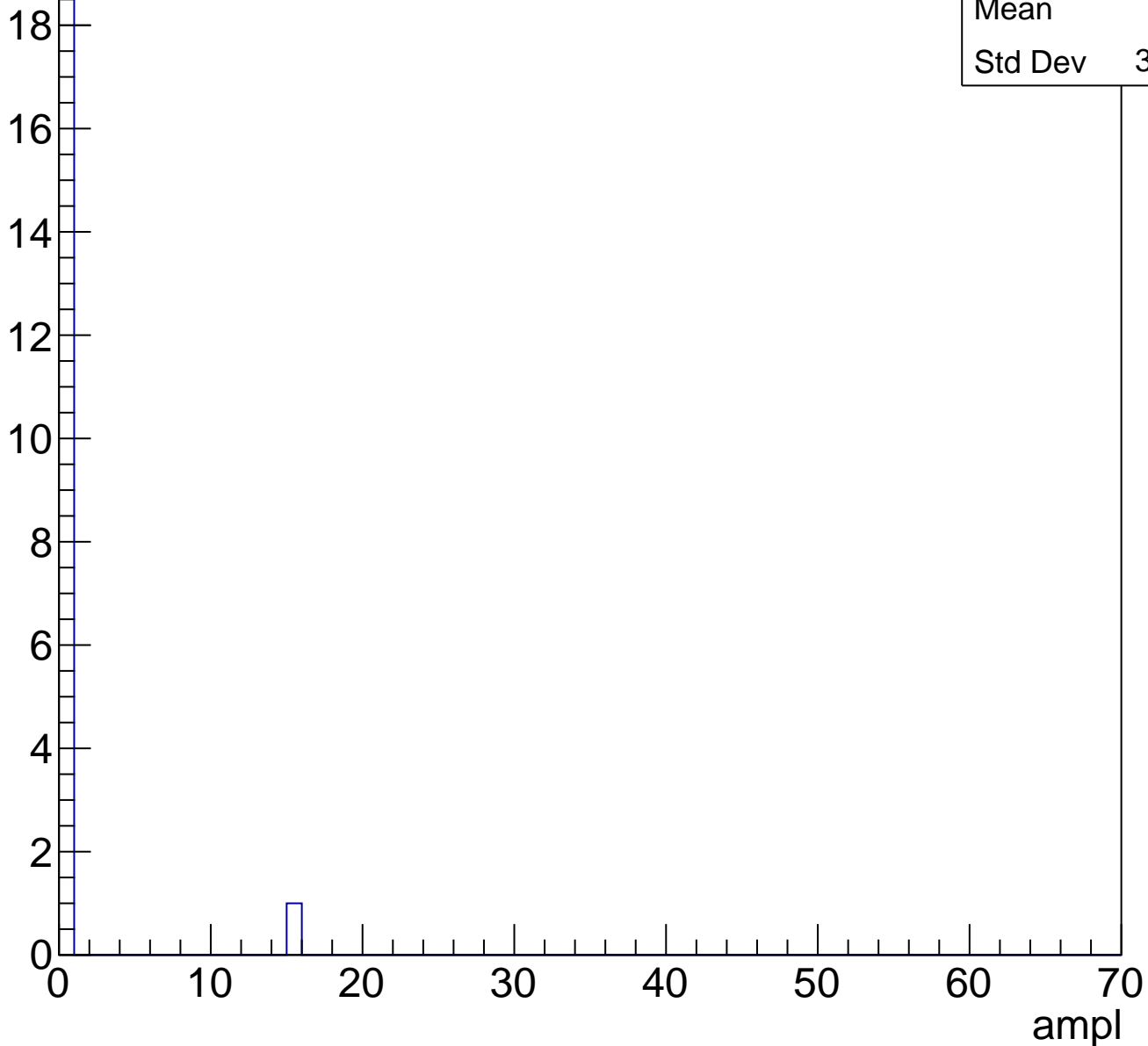


# B1L103S, U25-ch97, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	20
Mean	0.75
Std Dev	3.269

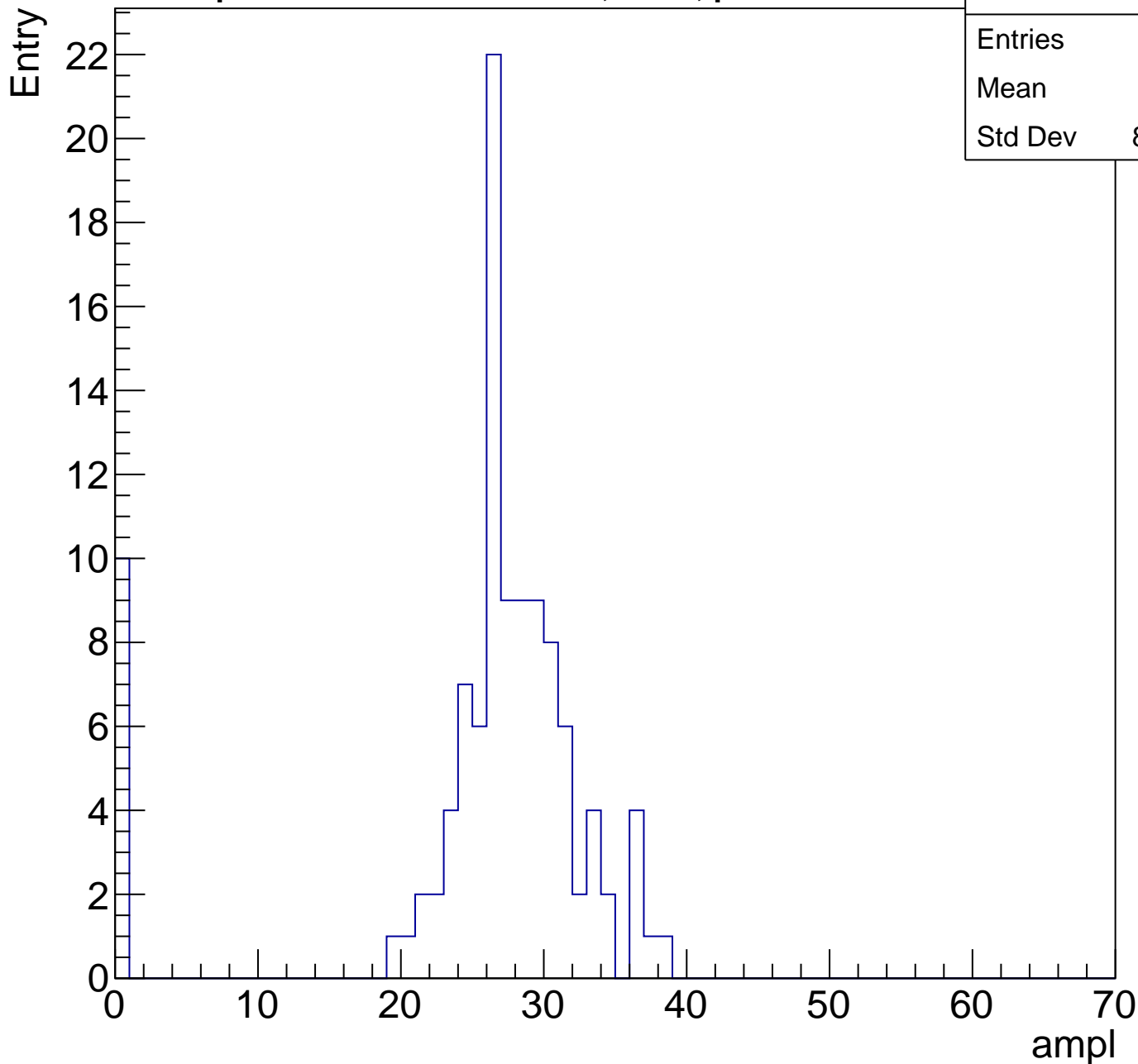
Entry



# B1L103S, U25-ch98, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	110
Mean	25.2
Std Dev	8.734

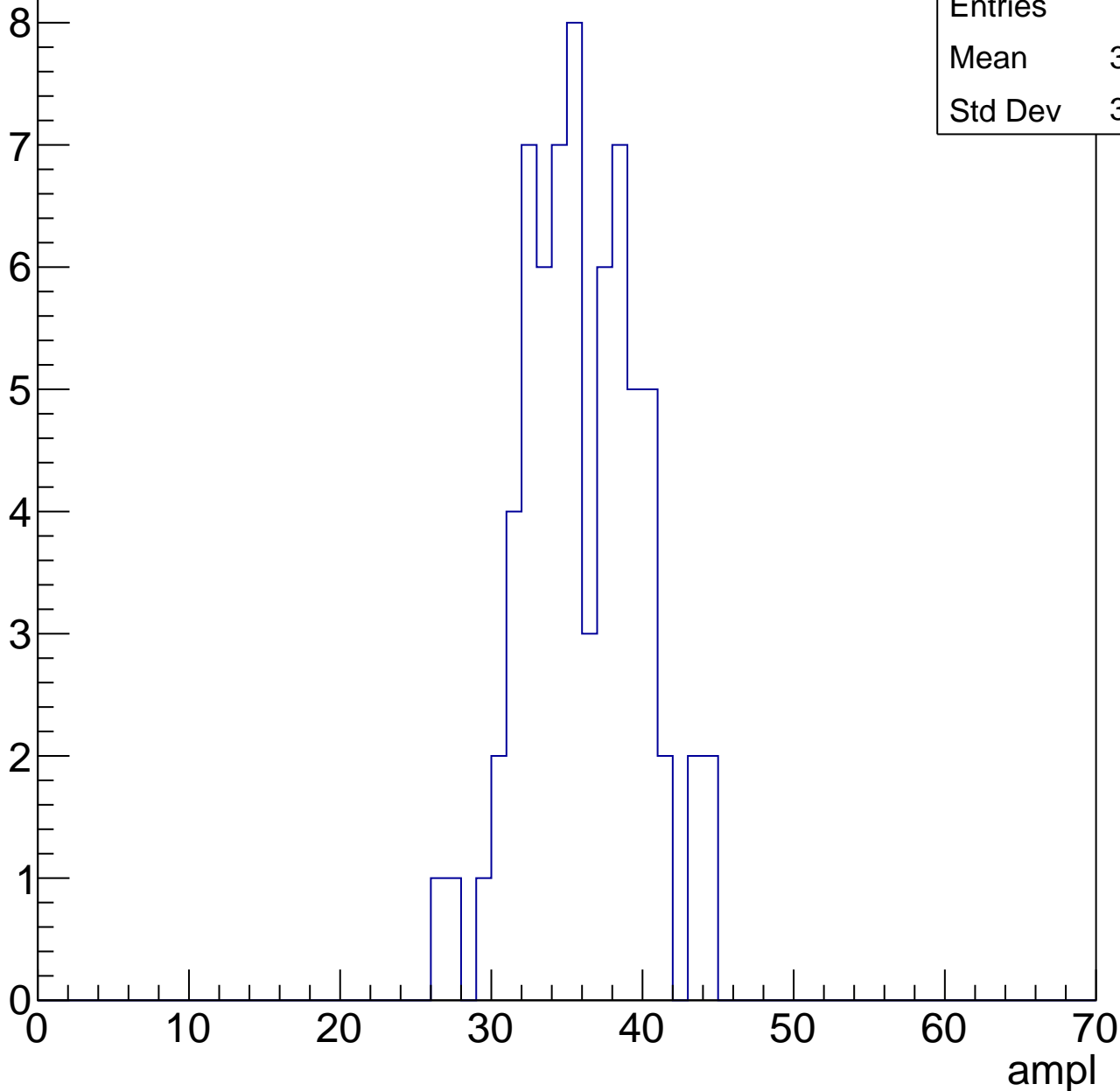


# B1L103S, U25-ch98, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	69
Mean	35.55
Std Dev	3.854



# B1L103S, U25-ch98, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	65
Mean	40.77
Std Dev	4.813

Entry

10

8

6

4

2

0

0

10

20

30

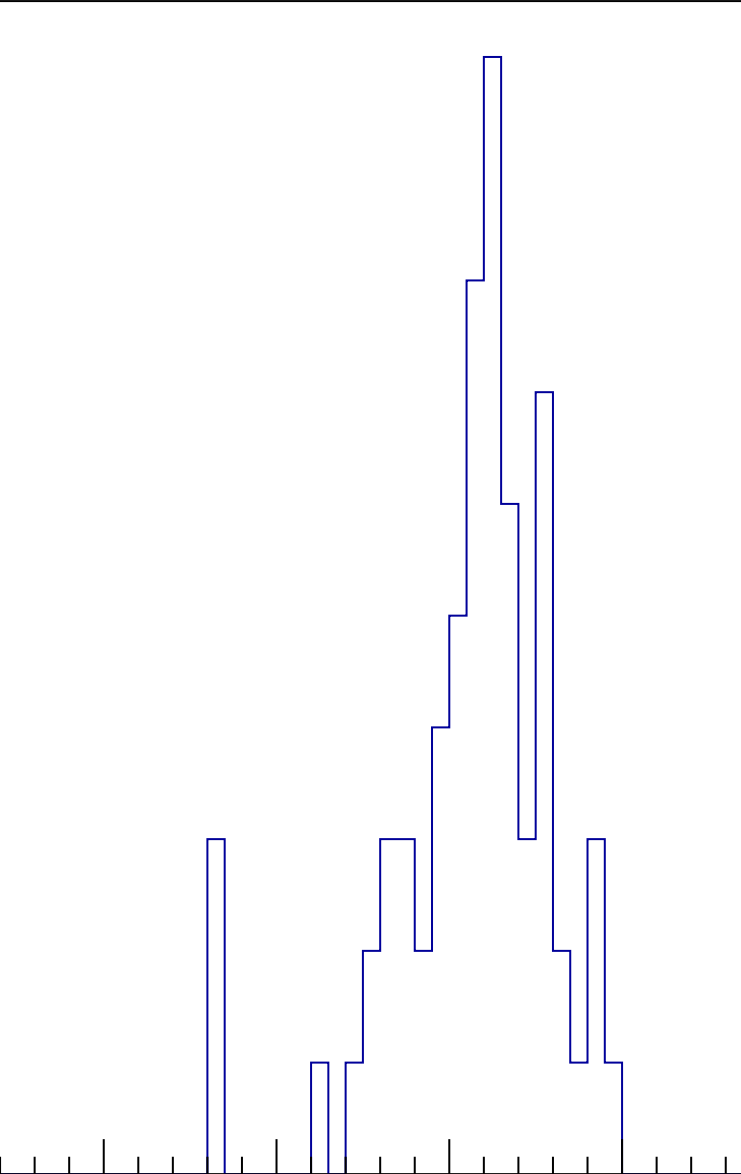
40

50

60

70

ampl

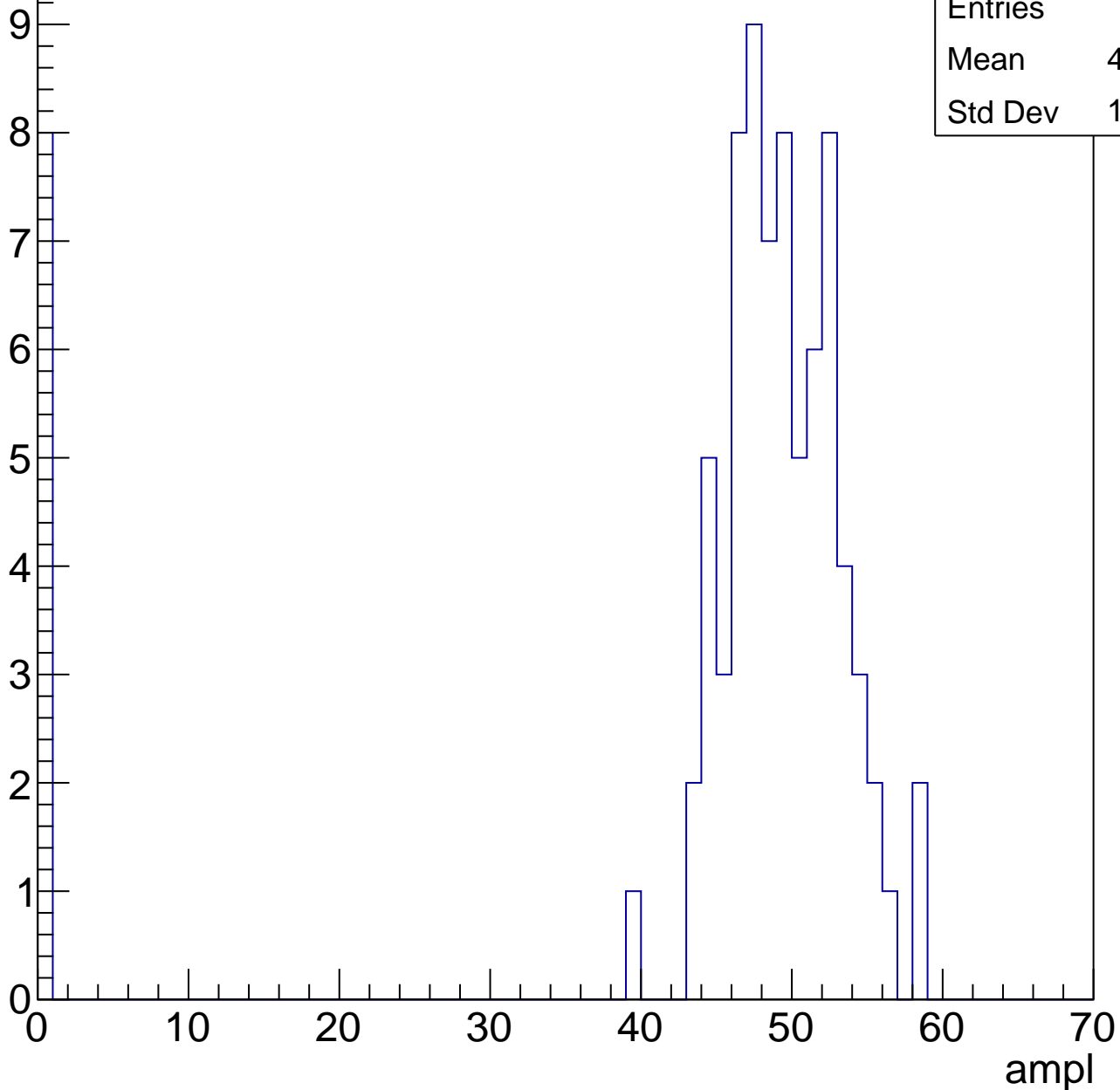


# B1L103S, U25-ch98, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	82
Mean	44.23
Std Dev	14.95

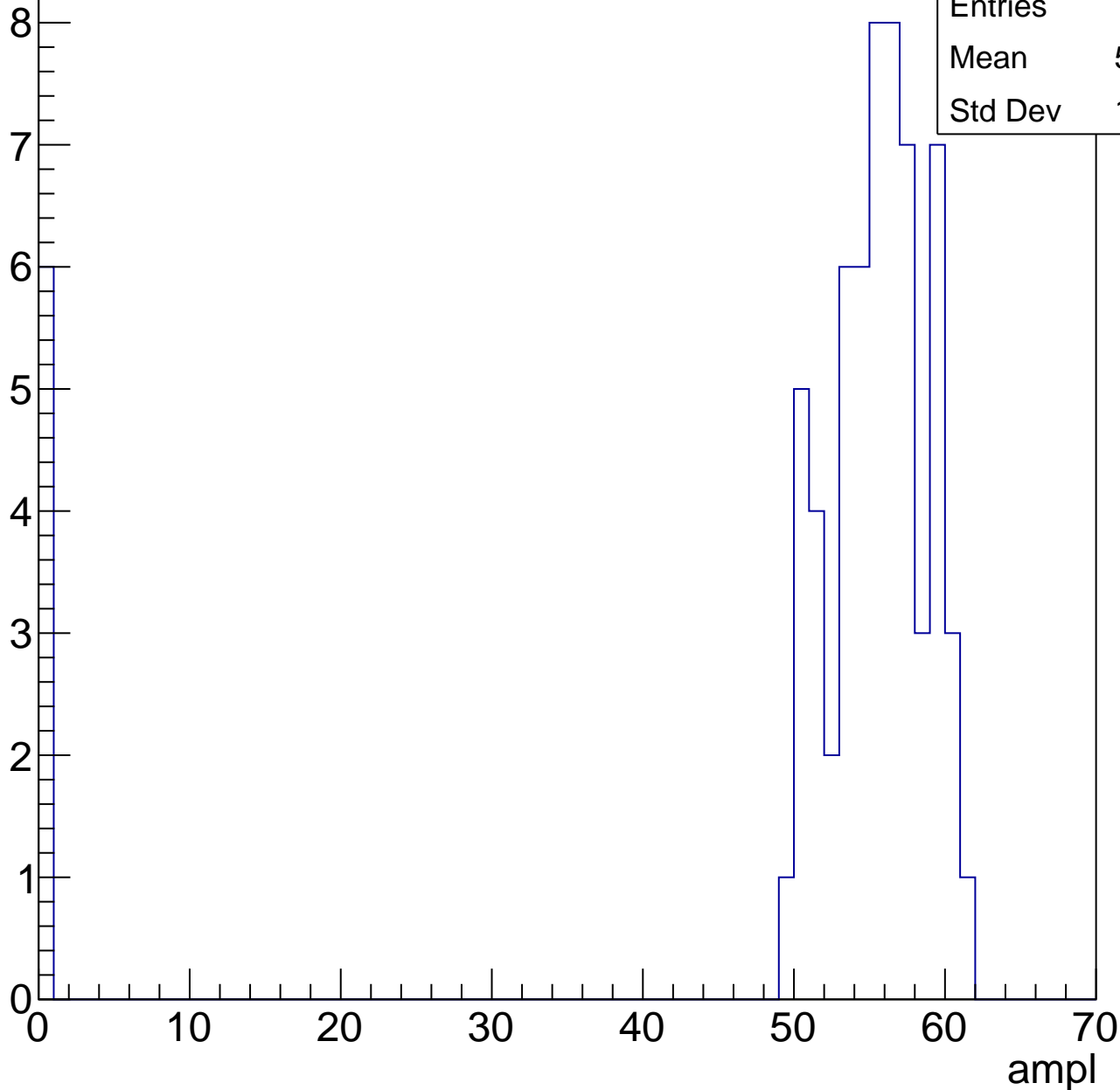


# B1L103S, U25-ch98, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

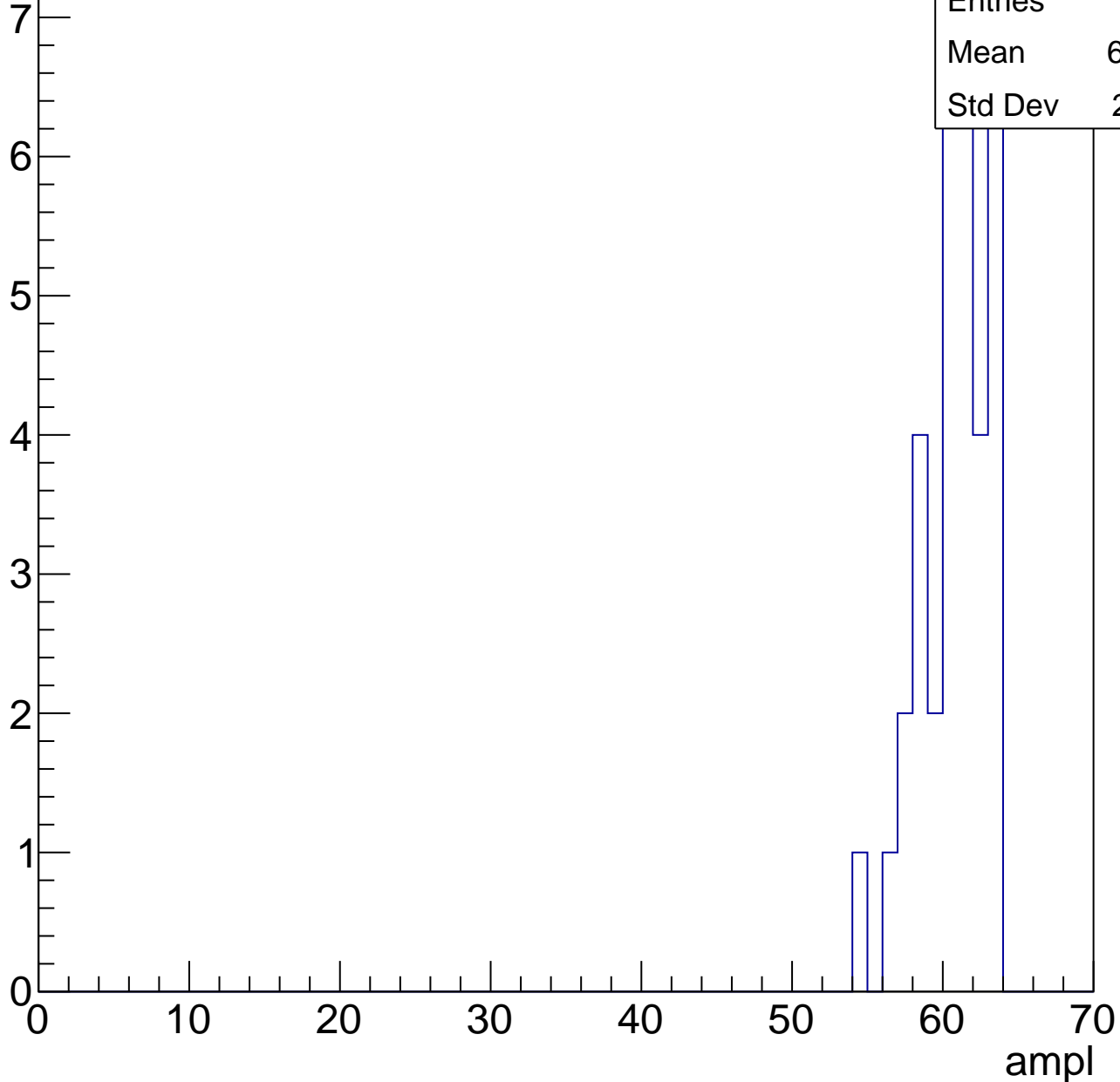
Entries	67
Mean	50.21
Std Dev	16.01



# B1L103S, U25-ch98, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



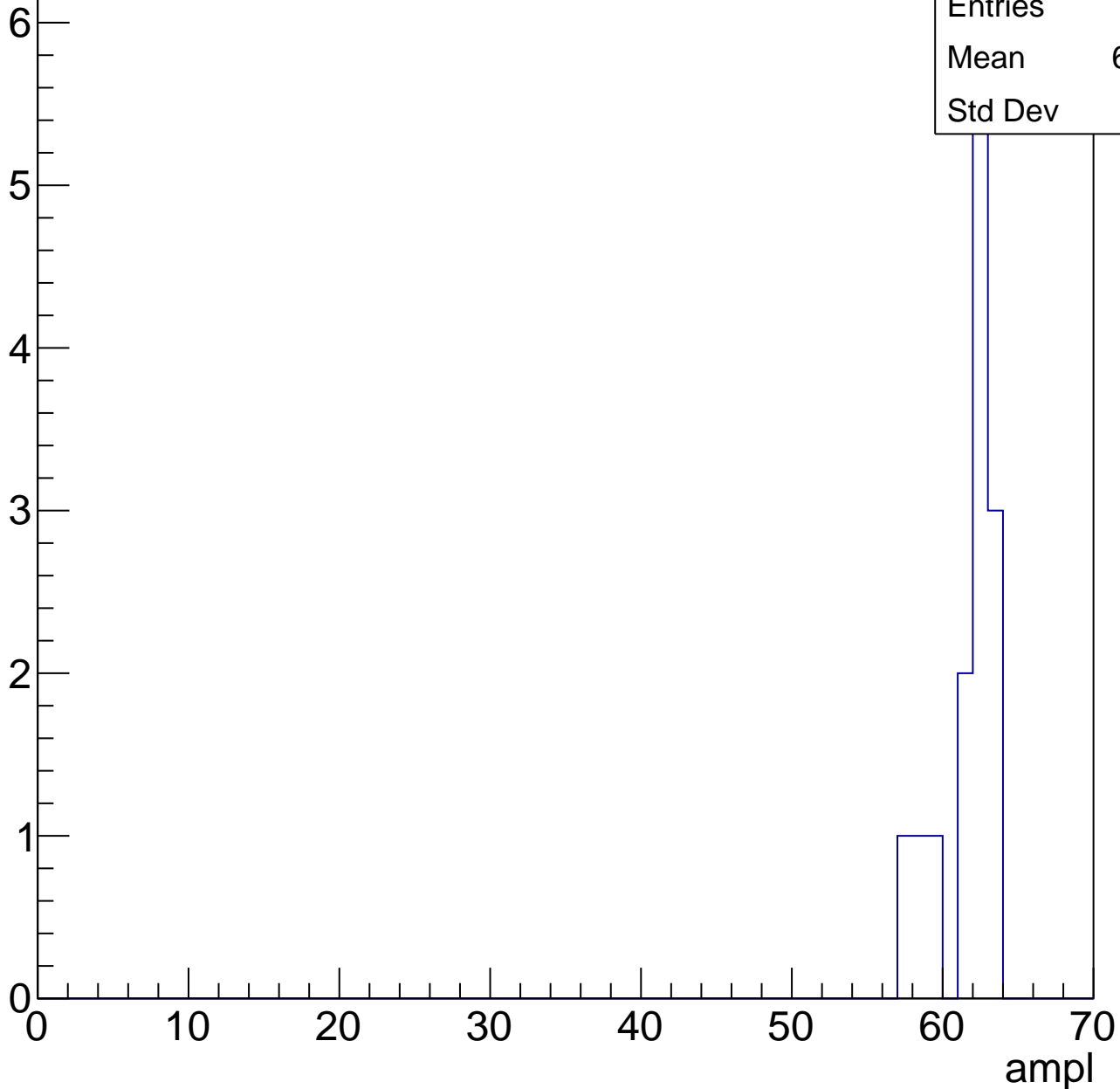
Entries	35
Mean	60.29
Std Dev	2.211

# B1L103S, U25-ch98, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	14
Mean	61.21
Std Dev	1.82



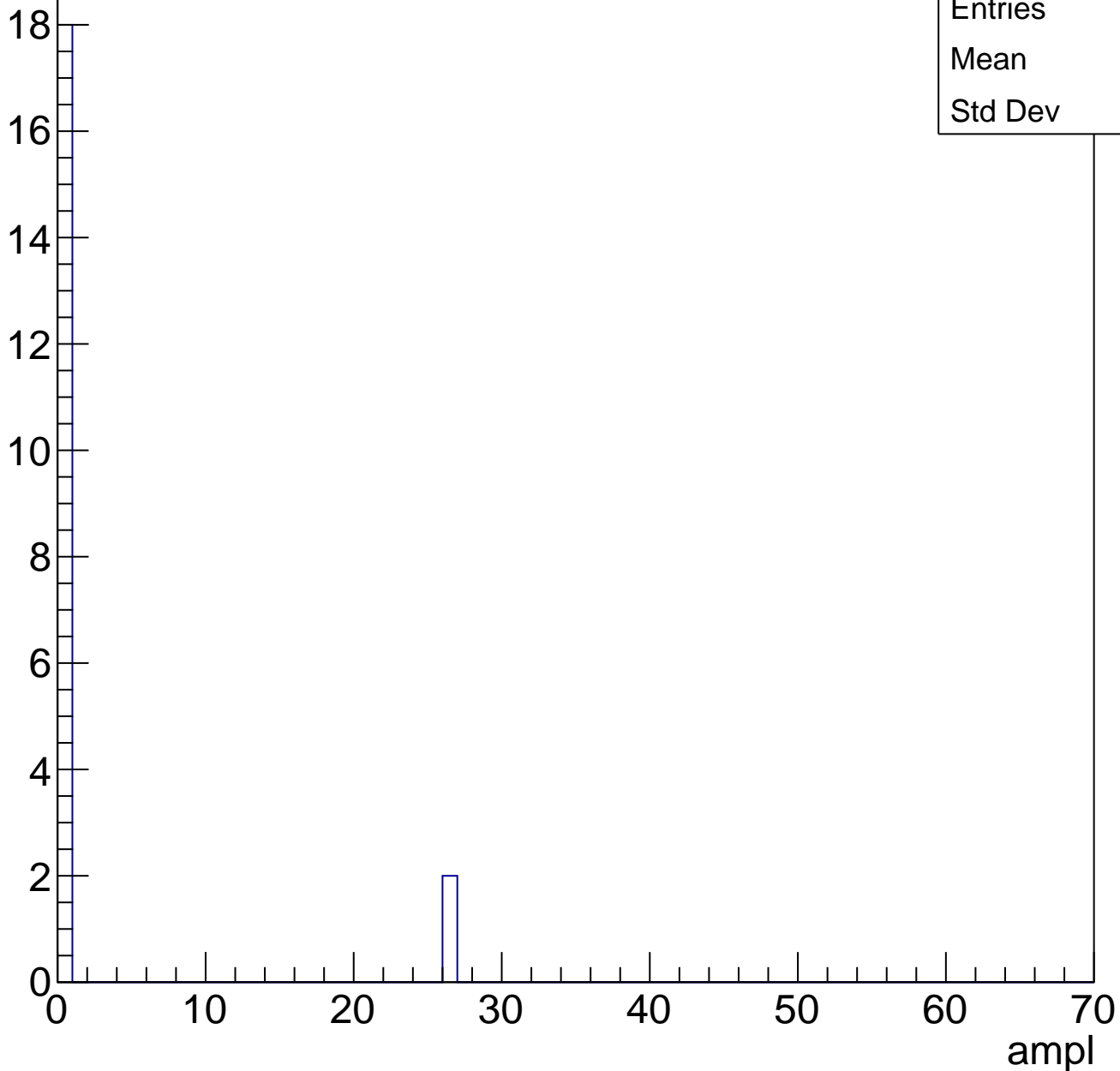


# B1L103S, U25-ch98, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	20
Mean	2.6
Std Dev	7.8

Entry

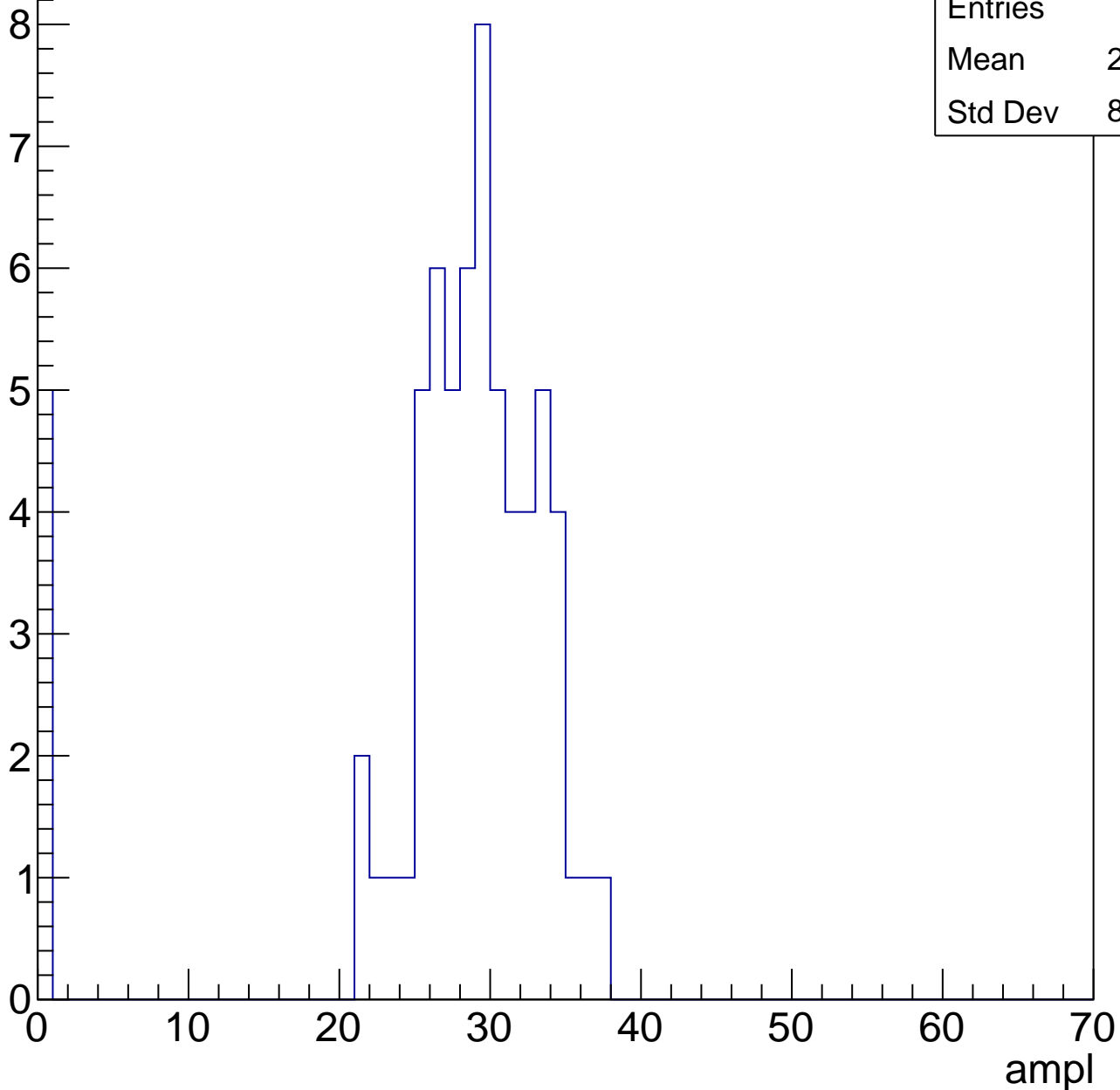


# B1L103S, U25-ch99, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	65
Mean	26.74
Std Dev	8.464

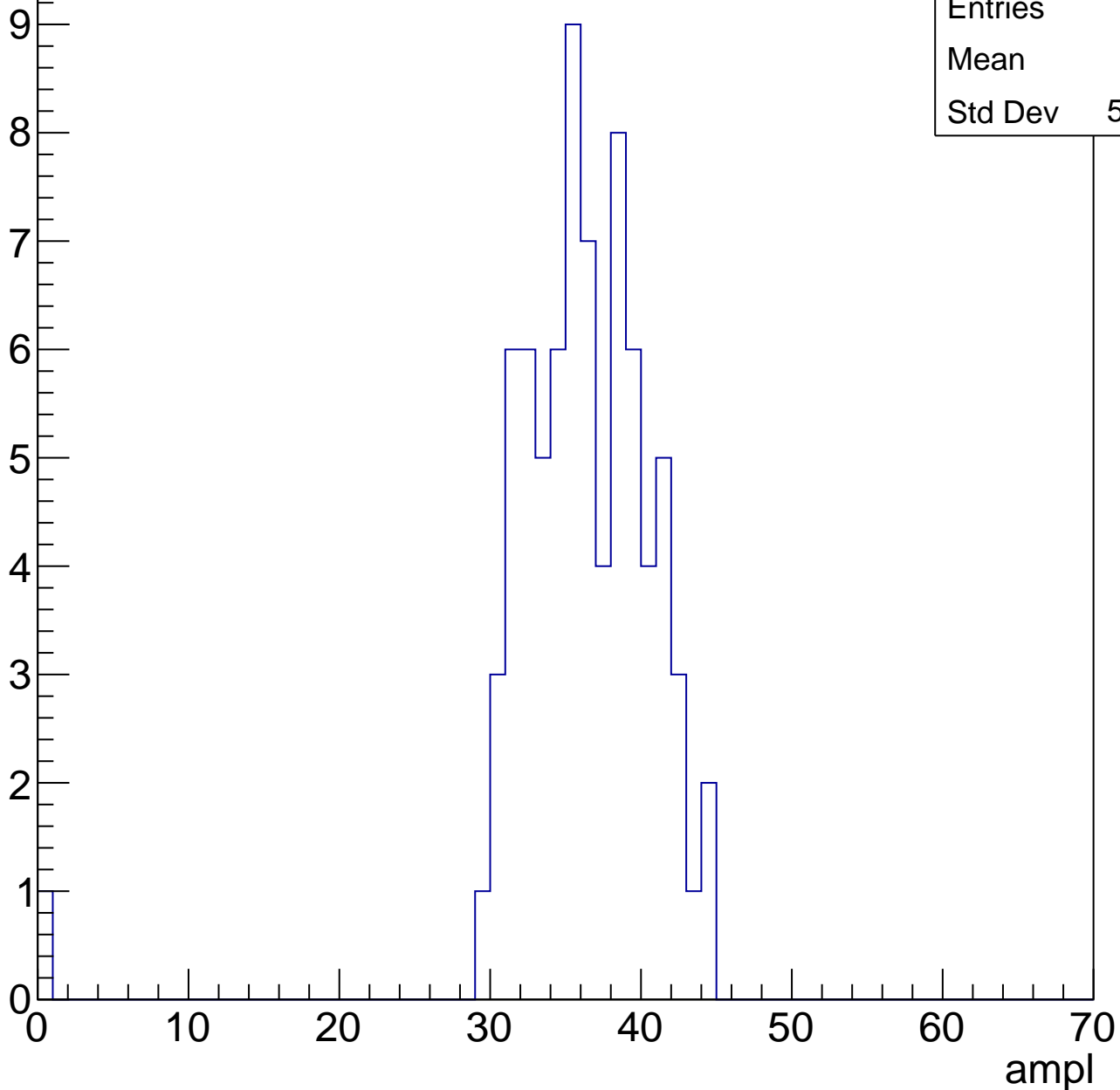


# B1L103S, U25-ch99, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	77
Mean	35.6
Std Dev	5.499

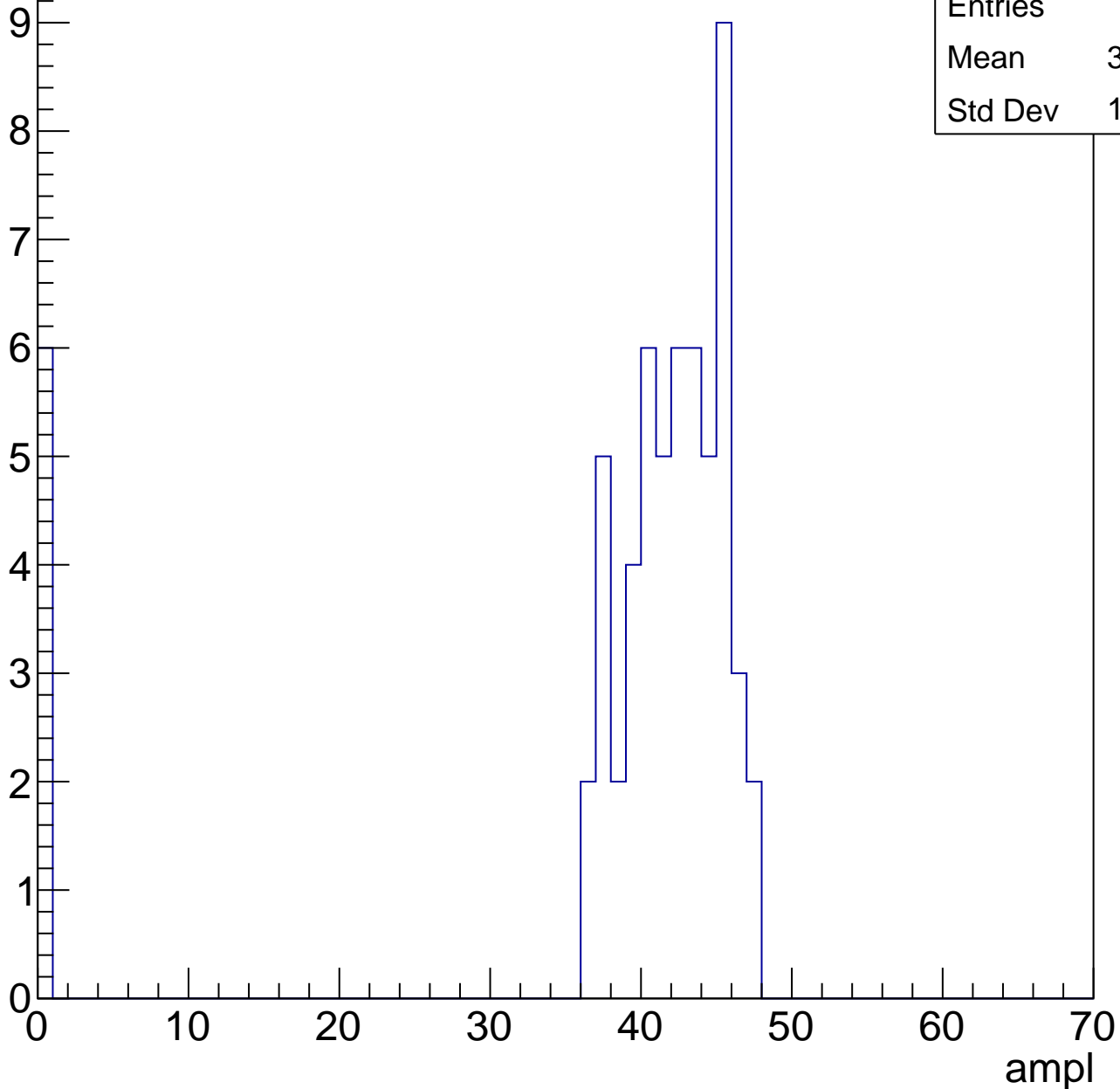


# B1L103S, U25-ch99, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	61
Mean	37.72
Std Dev	12.78

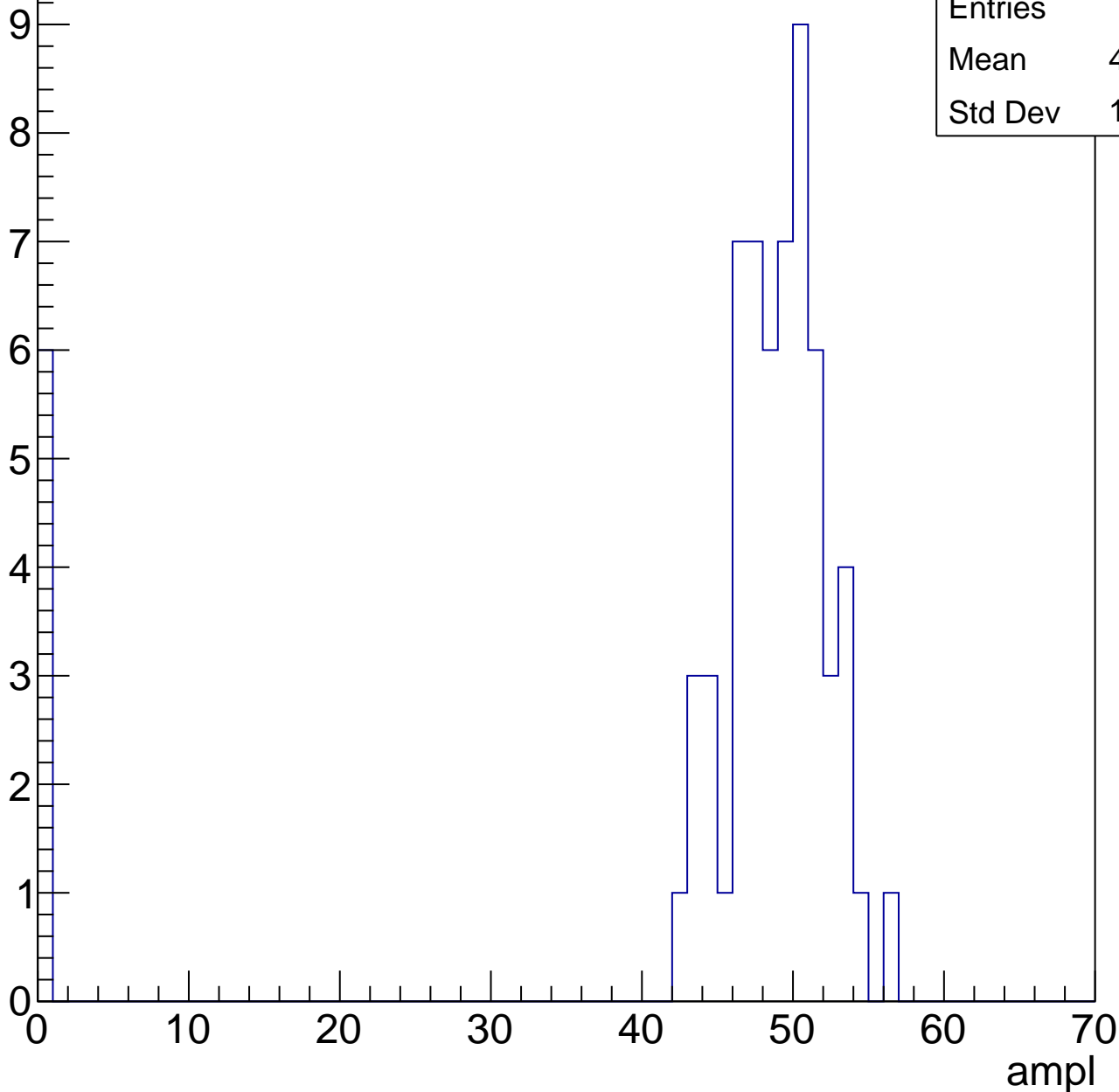


# B1L103S, U25-ch99, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

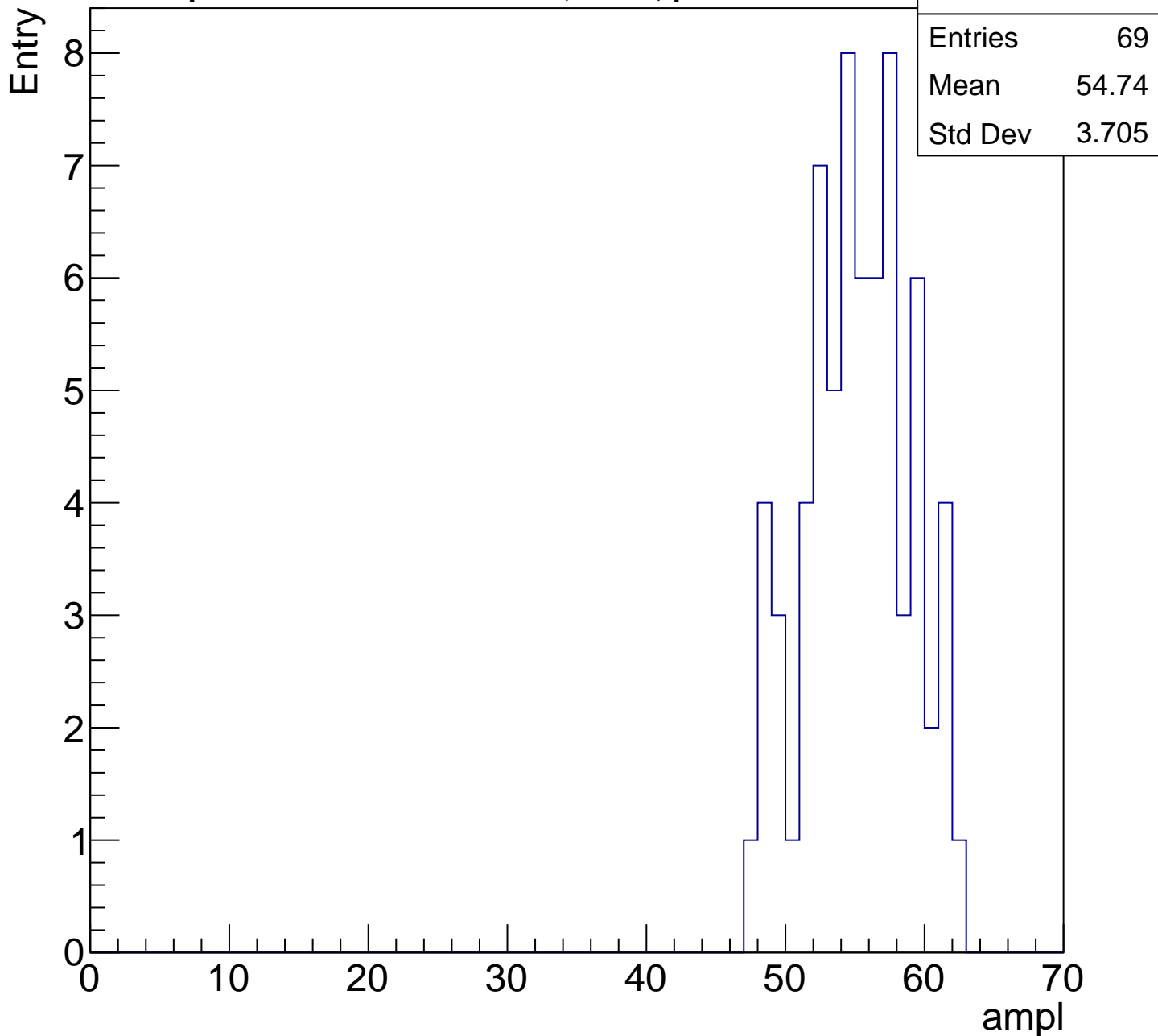
Entry

Entries	65
Mean	44.06
Std Dev	14.34



# B1L103S, U25-ch99, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

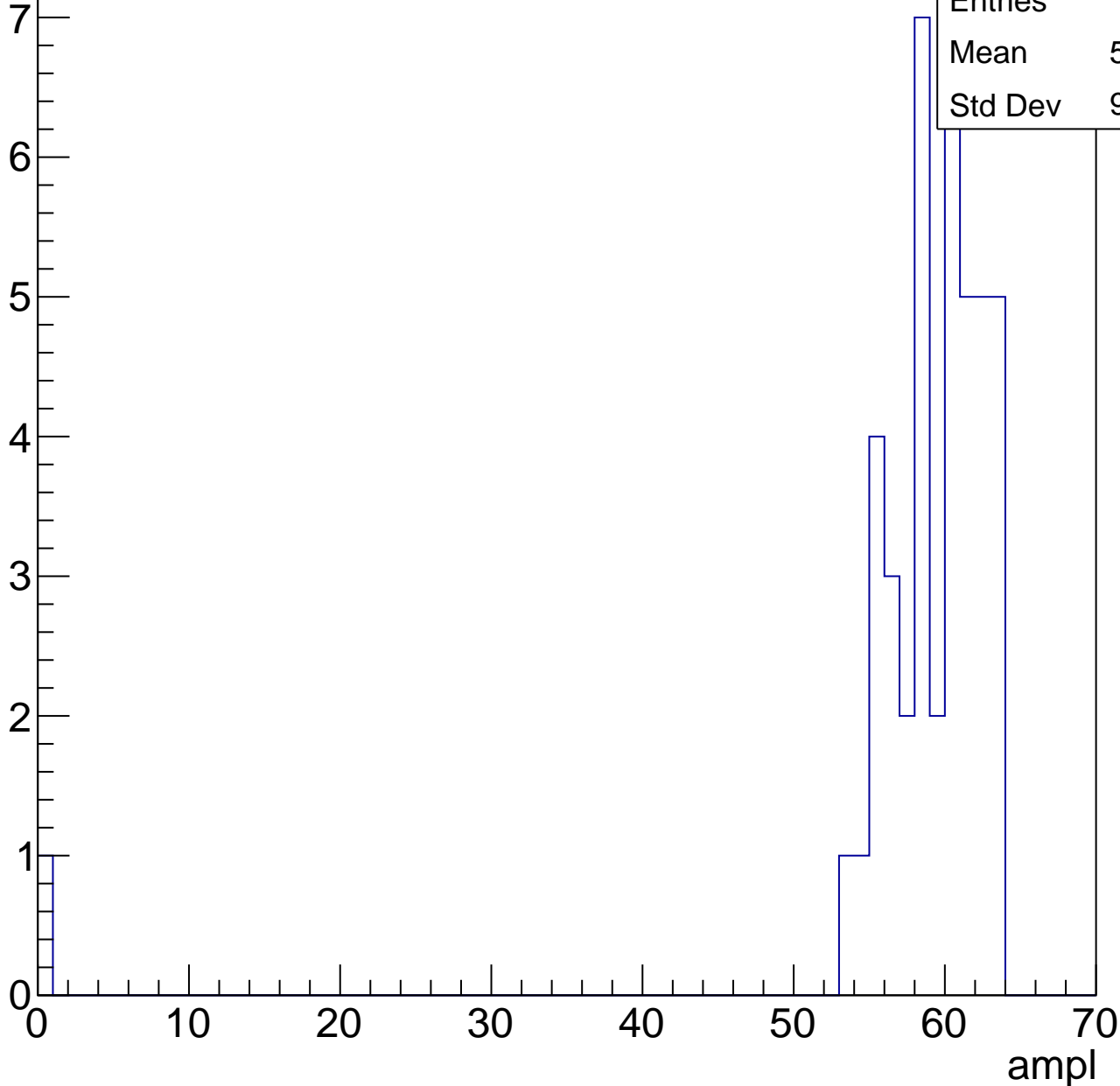


# B1L103S, U25-ch99, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	43
Mean	57.74
Std Dev	9.316

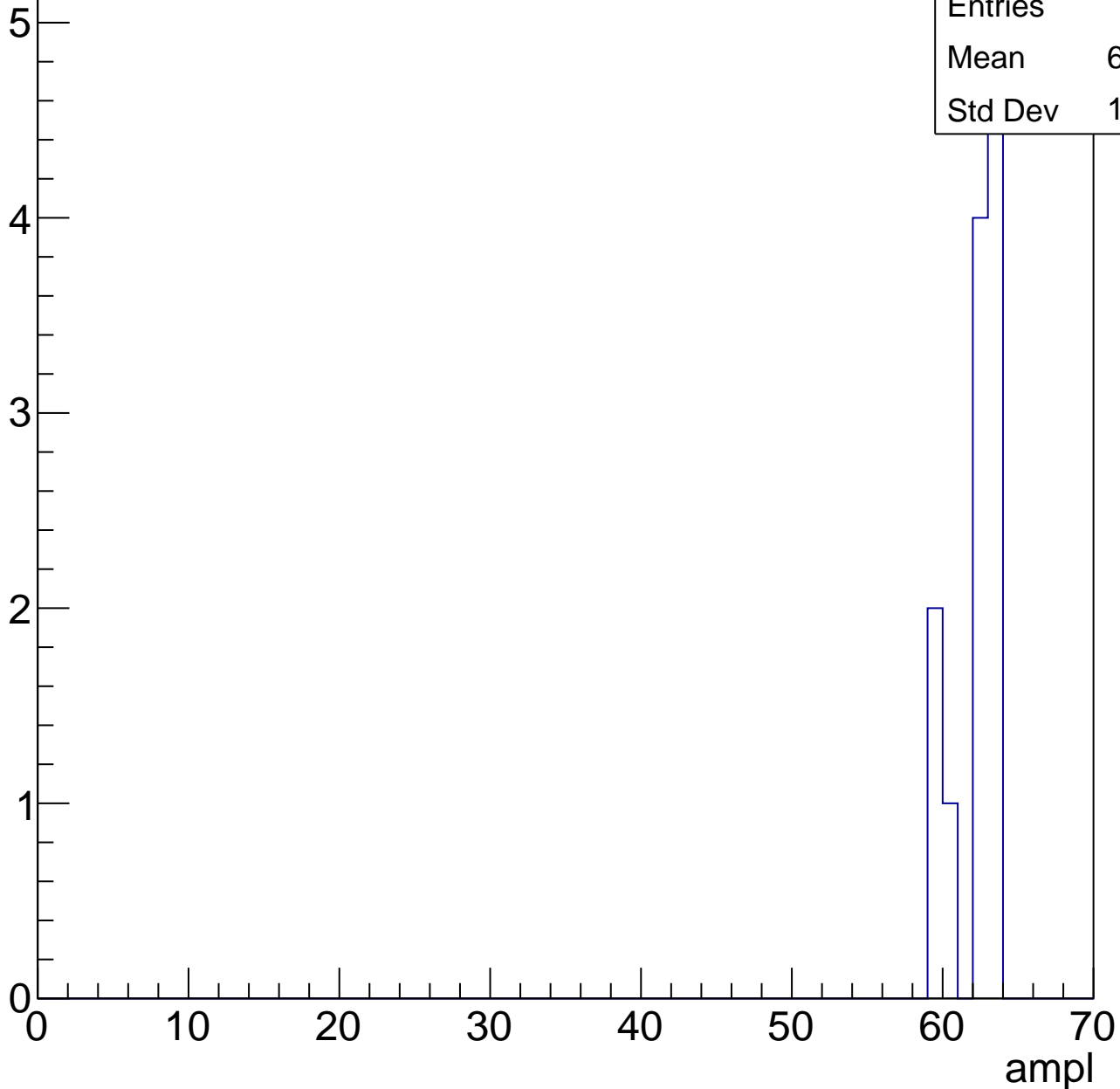


# B1L103S, U25-ch99, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	12
Mean	61.75
Std Dev	1.479





# B1L103S, U25-ch99, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	20
Mean	3.05
Std Dev	13.29

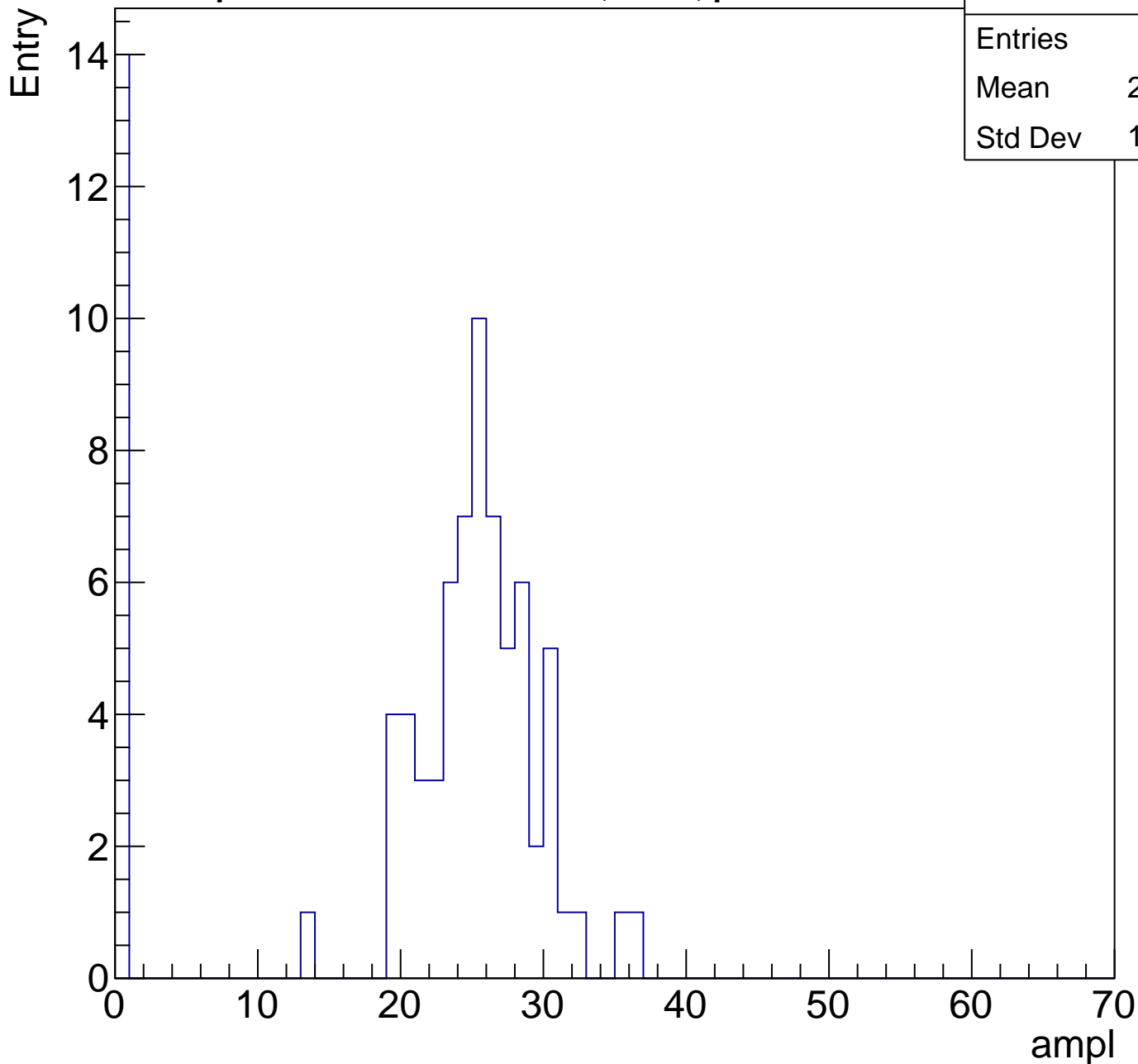
Entry



# B1L103S, U25-ch100, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	81
Mean	20.75
Std Dev	10.14

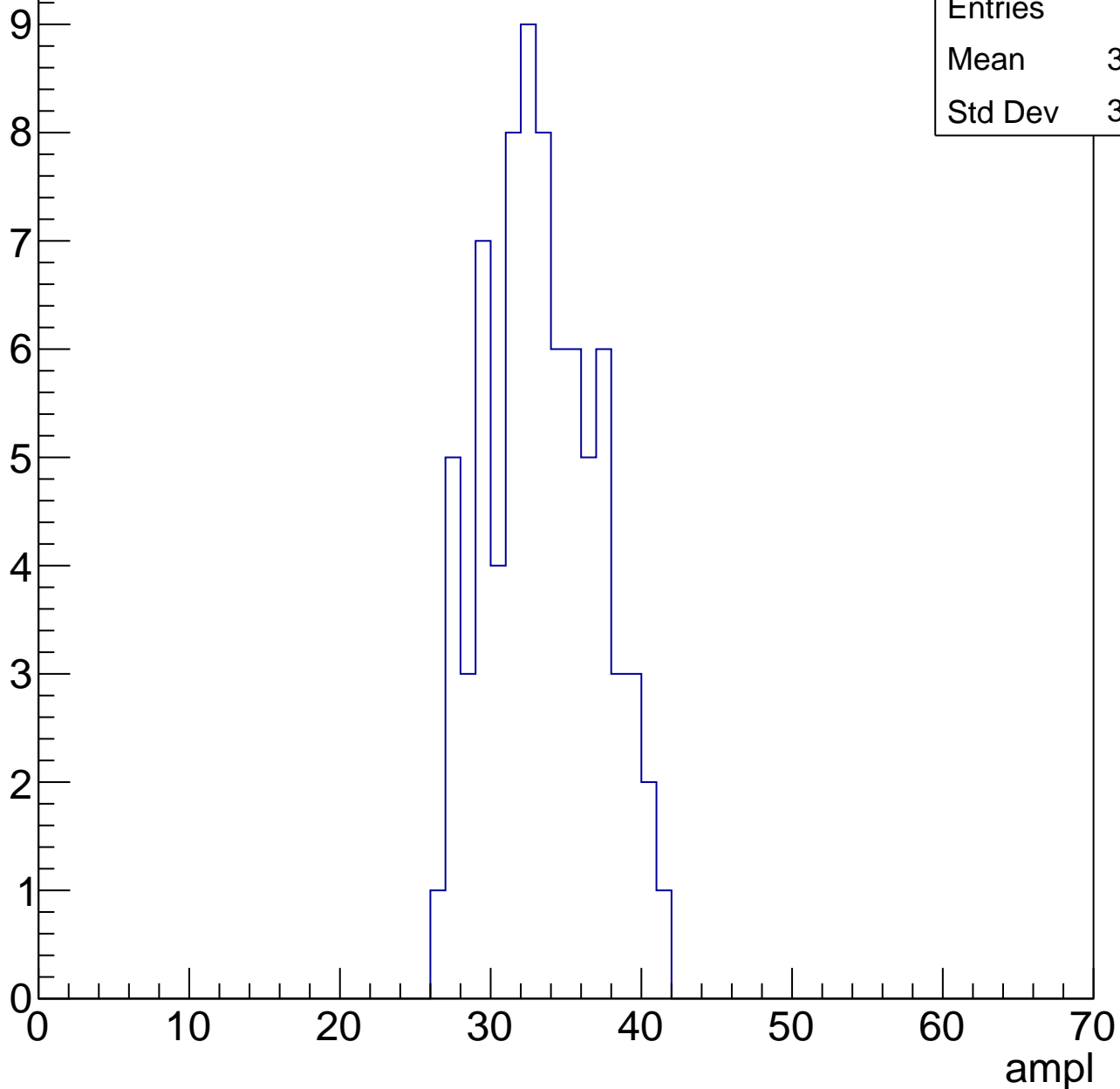


# B1L103S, U25-ch100, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	77
Mean	32.94
Std Dev	3.619

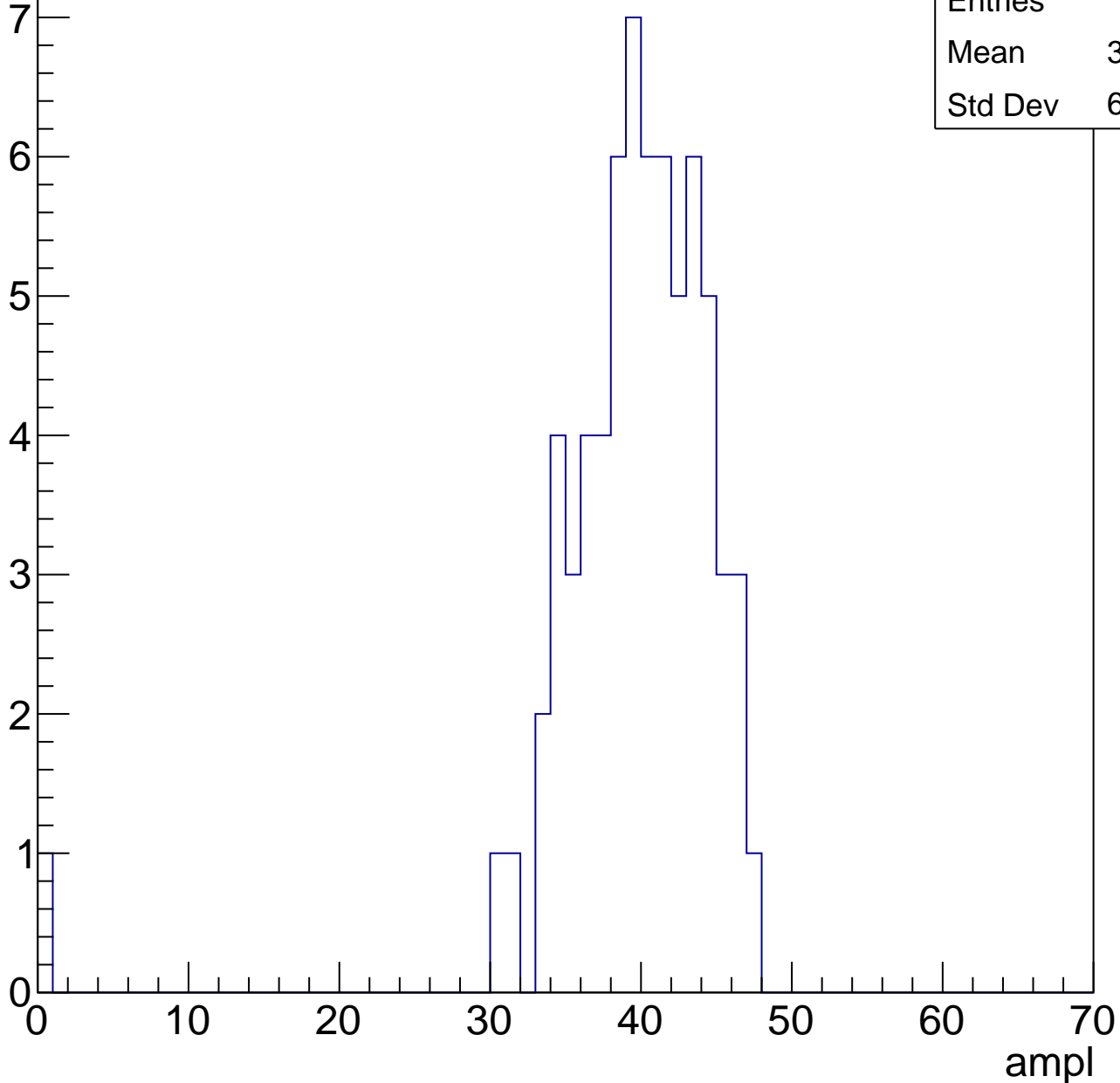


# B1L103S, U25-ch100, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	68
Mean	39.04
Std Dev	6.134

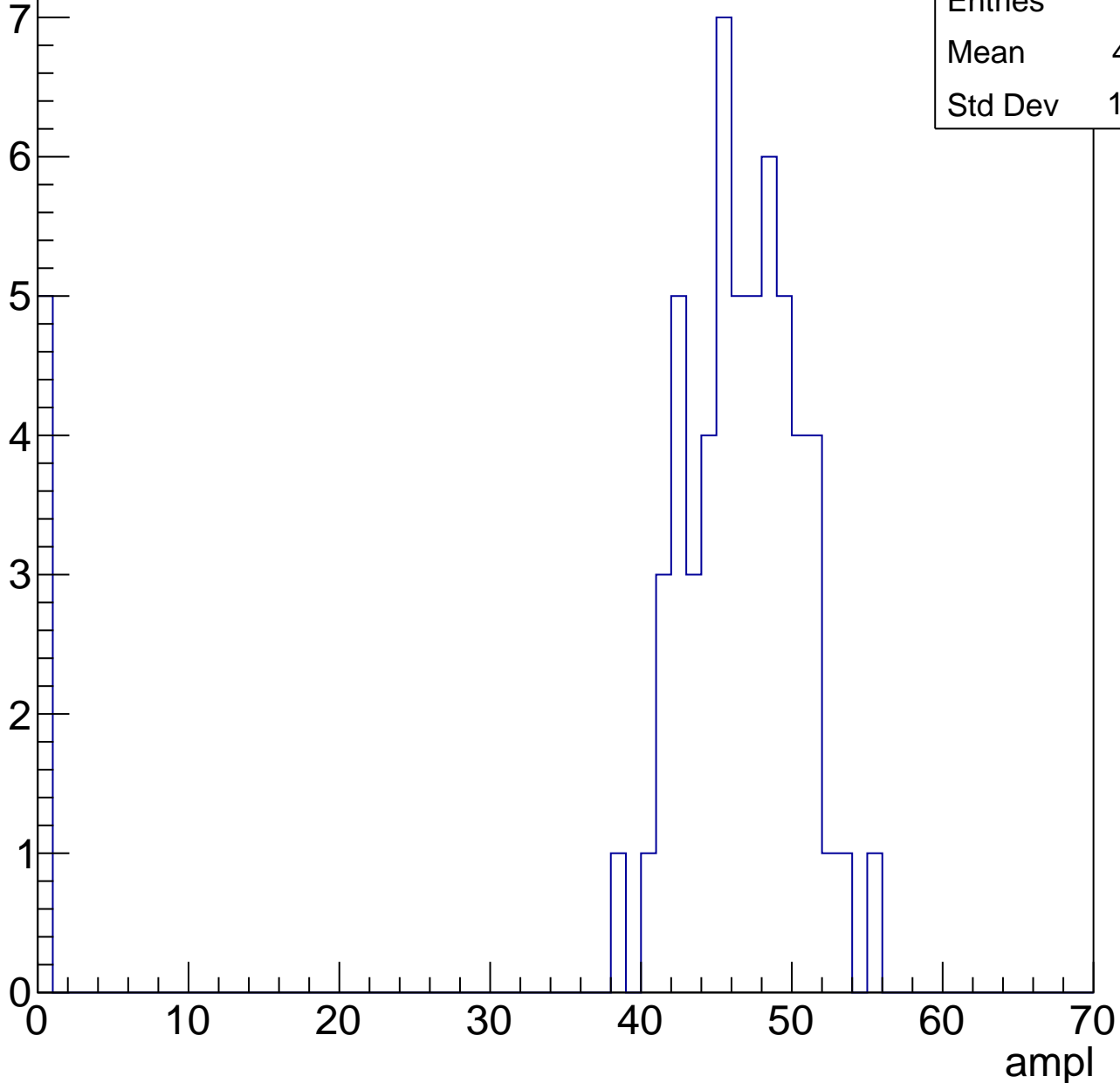


# B1L103S, U25-ch100, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	61
Mean	42.51
Std Dev	13.15

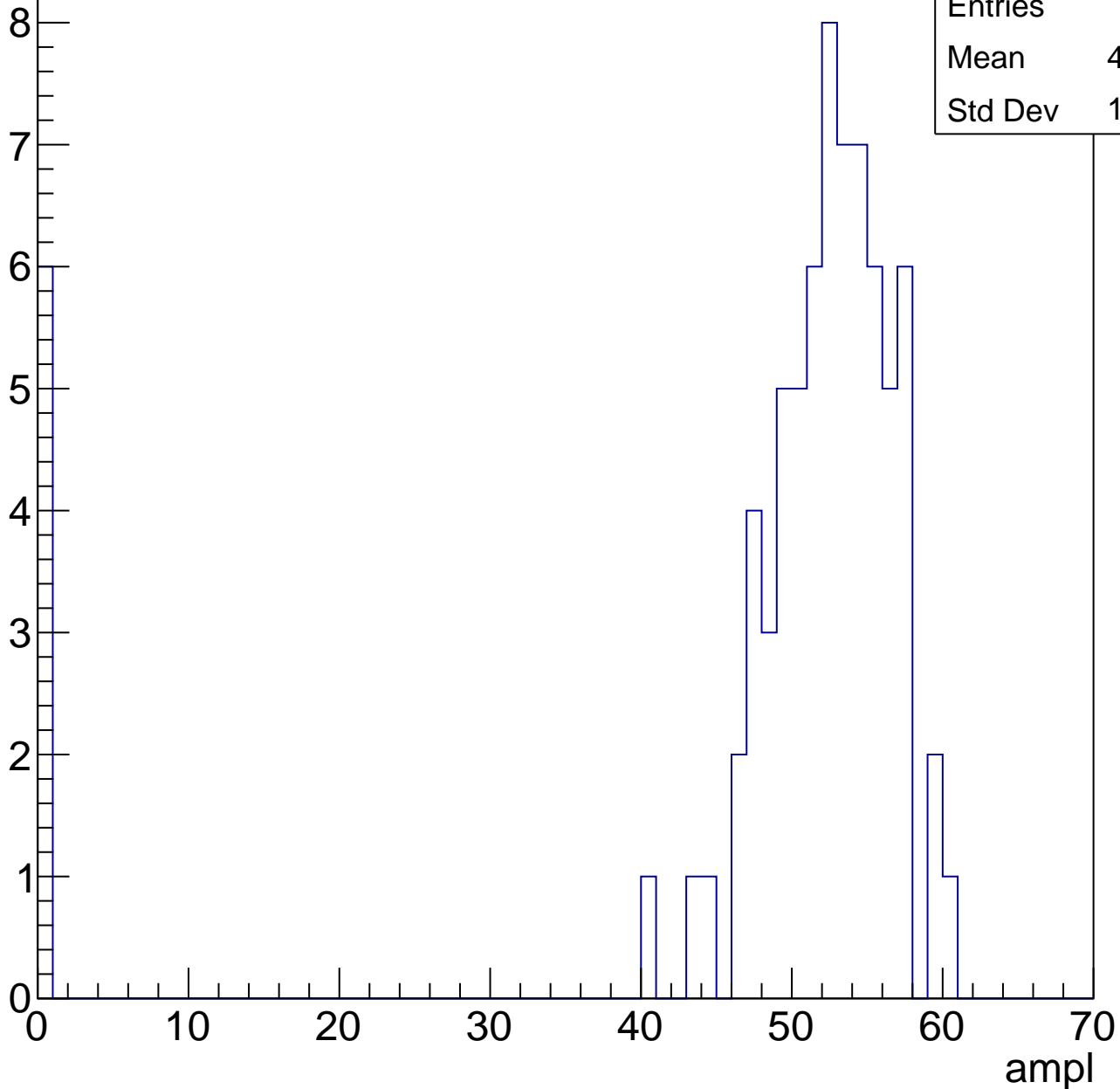


# B1L103S, U25-ch100, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	76
Mean	47.99
Std Dev	14.54

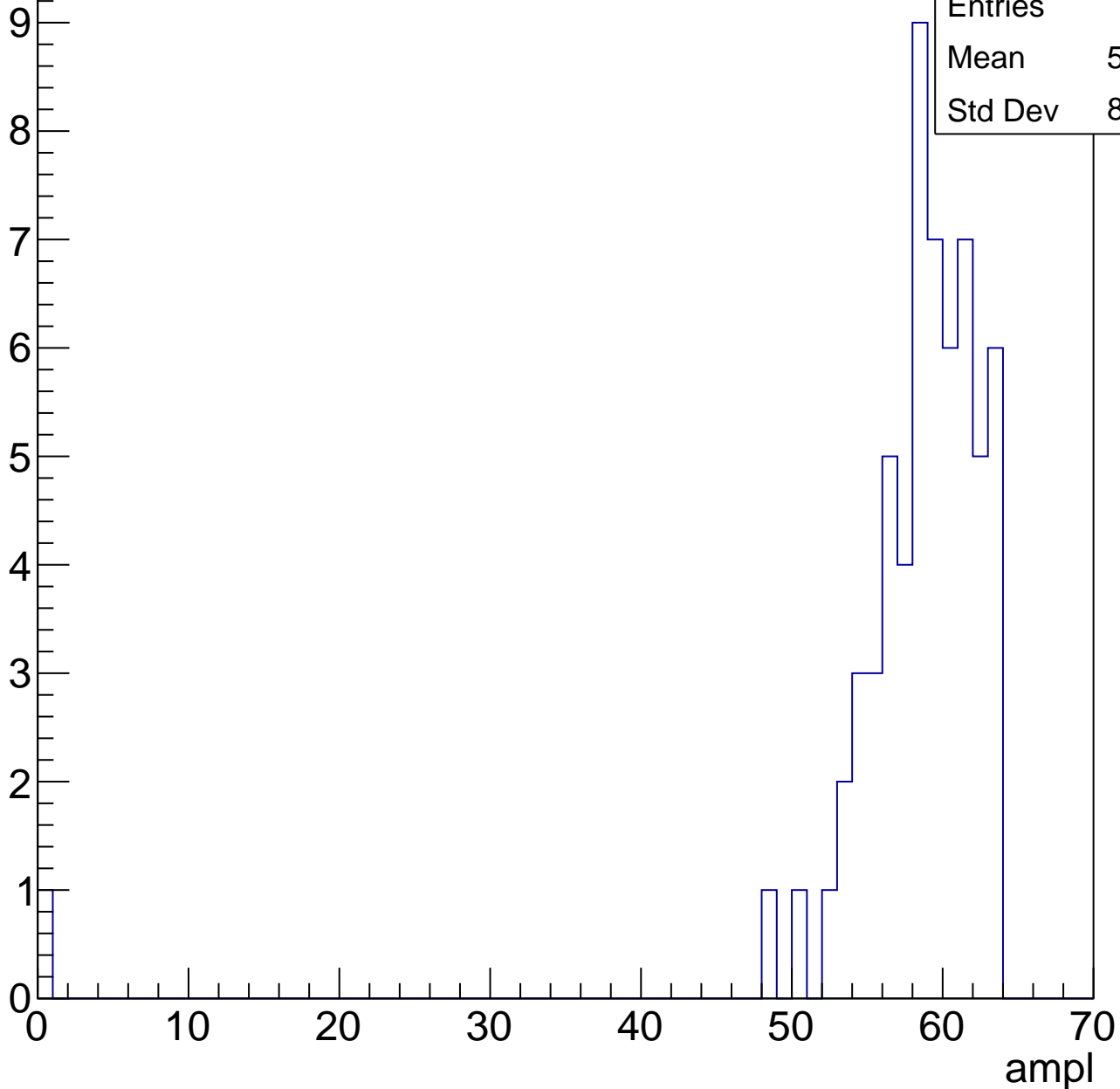


# B1L103S, U25-ch100, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	61
Mean	57.39
Std Dev	8.112



# B1L103S, U25-ch100, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

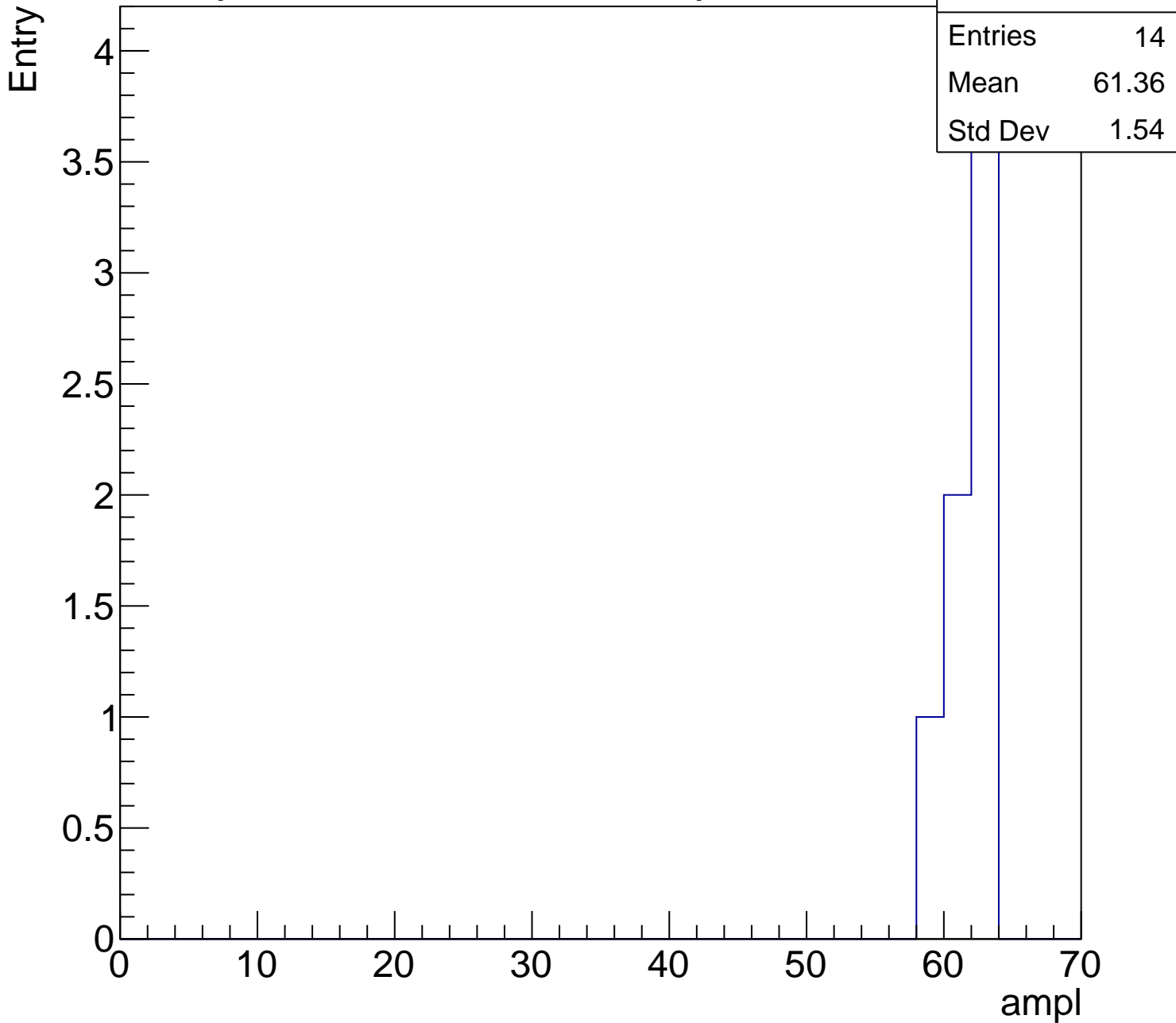
Entry

4  
3.5  
3  
2.5  
2  
1.5  
1  
0.5  
0

Entries	14
Mean	61.36
Std Dev	1.54

ampl

0 10 20 30 40 50 60 70



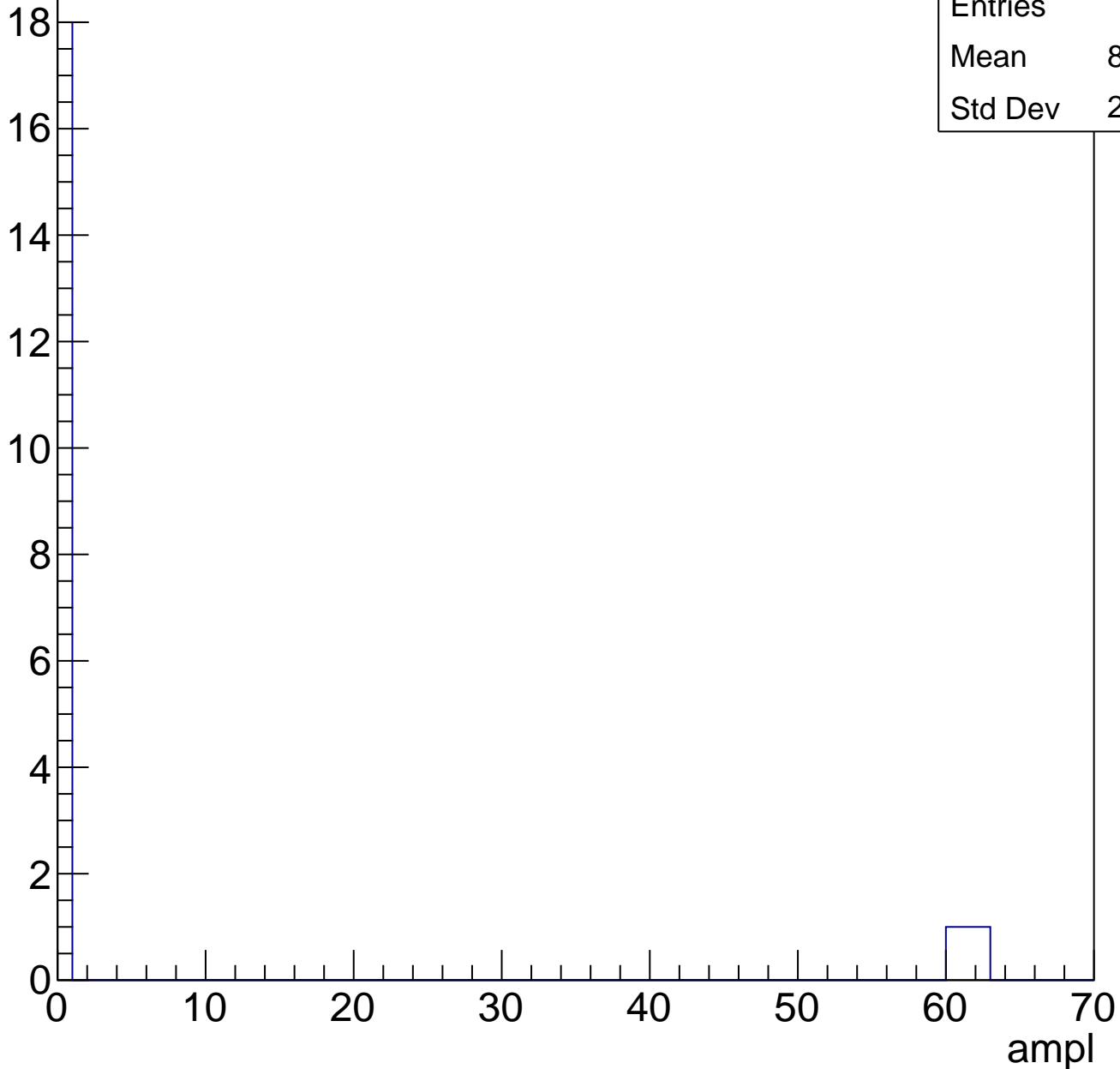


# B1L103S, U25-ch100, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	21
Mean	8.714
Std Dev	21.35

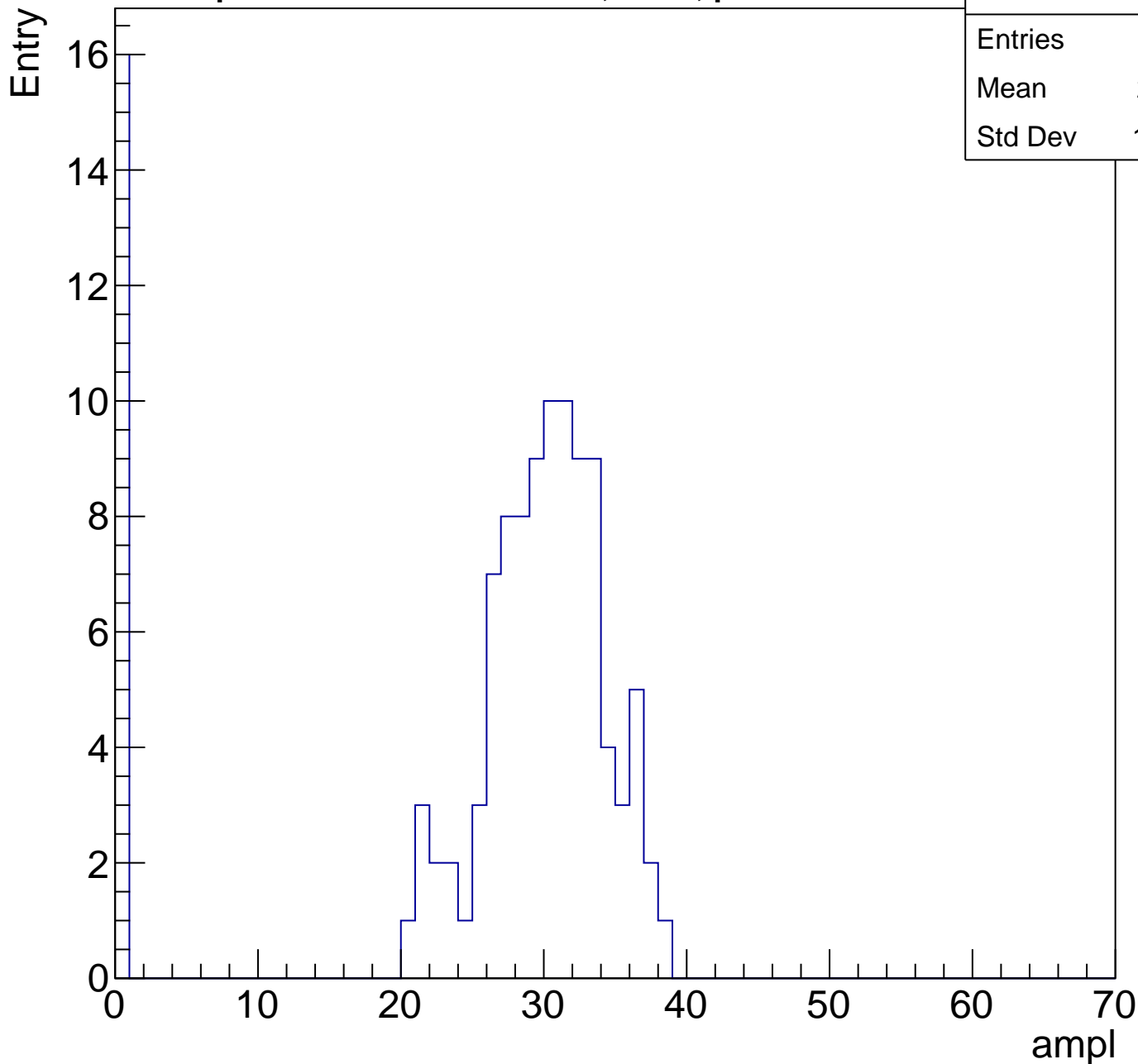
Entry



# B1L103S, U25-ch101, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	113
Mean	25.51
Std Dev	10.99

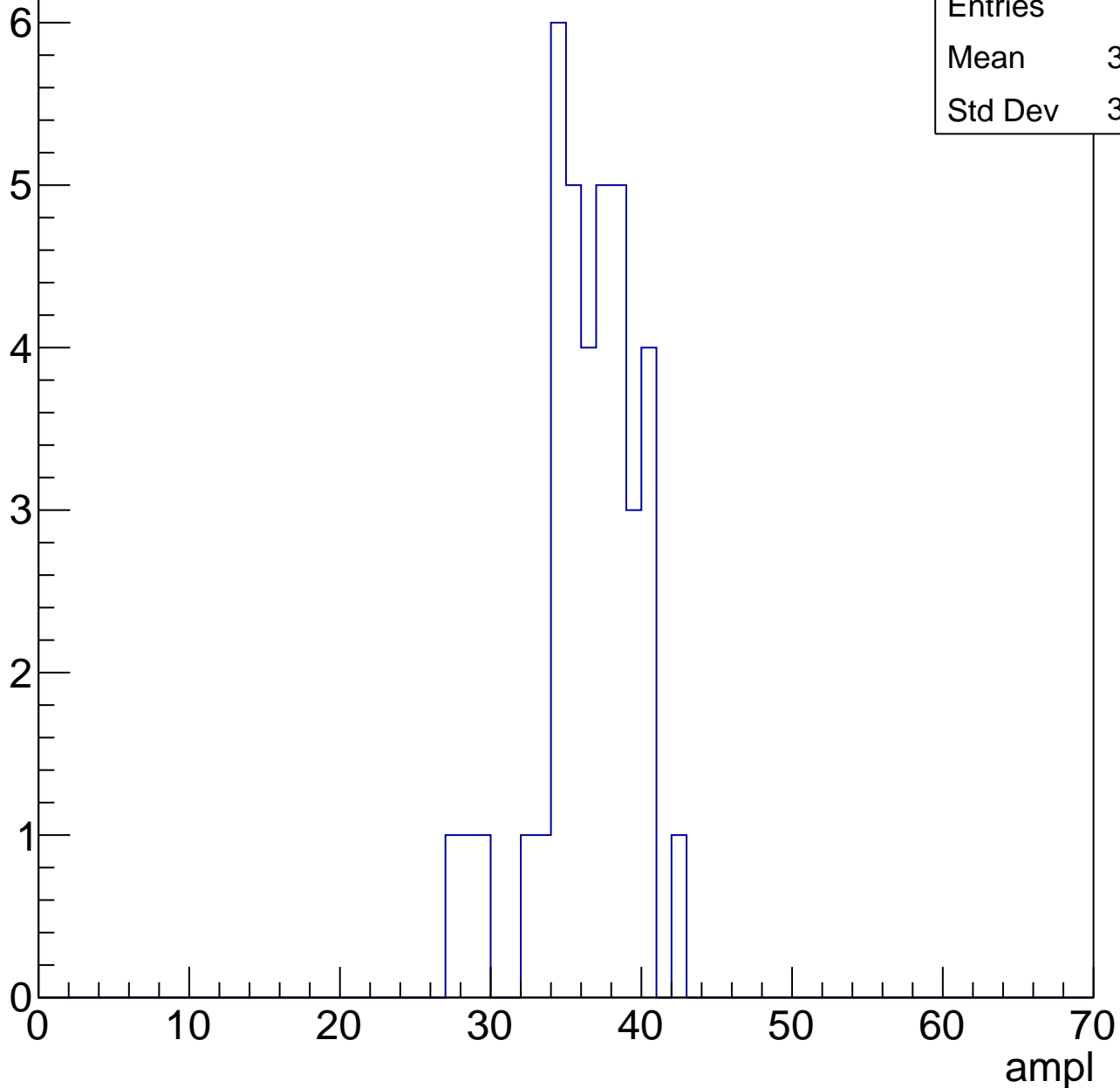


# B1L103S, U25-ch101, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	38
Mean	35.95
Std Dev	3.244



# B1L103S, U25-ch101, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

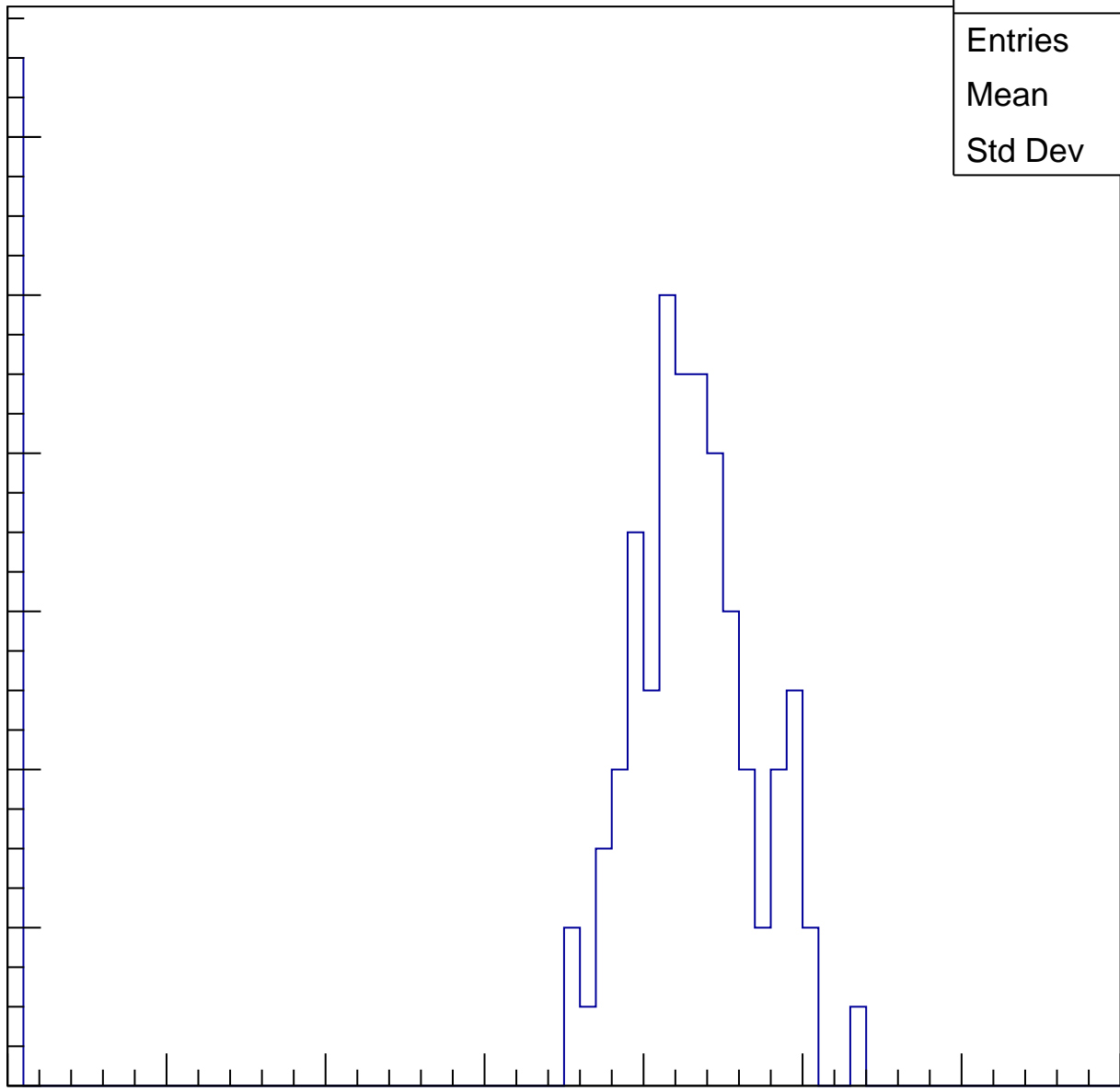
Entries	95
Mean	36.92
Std Dev	15.11

Entry

12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

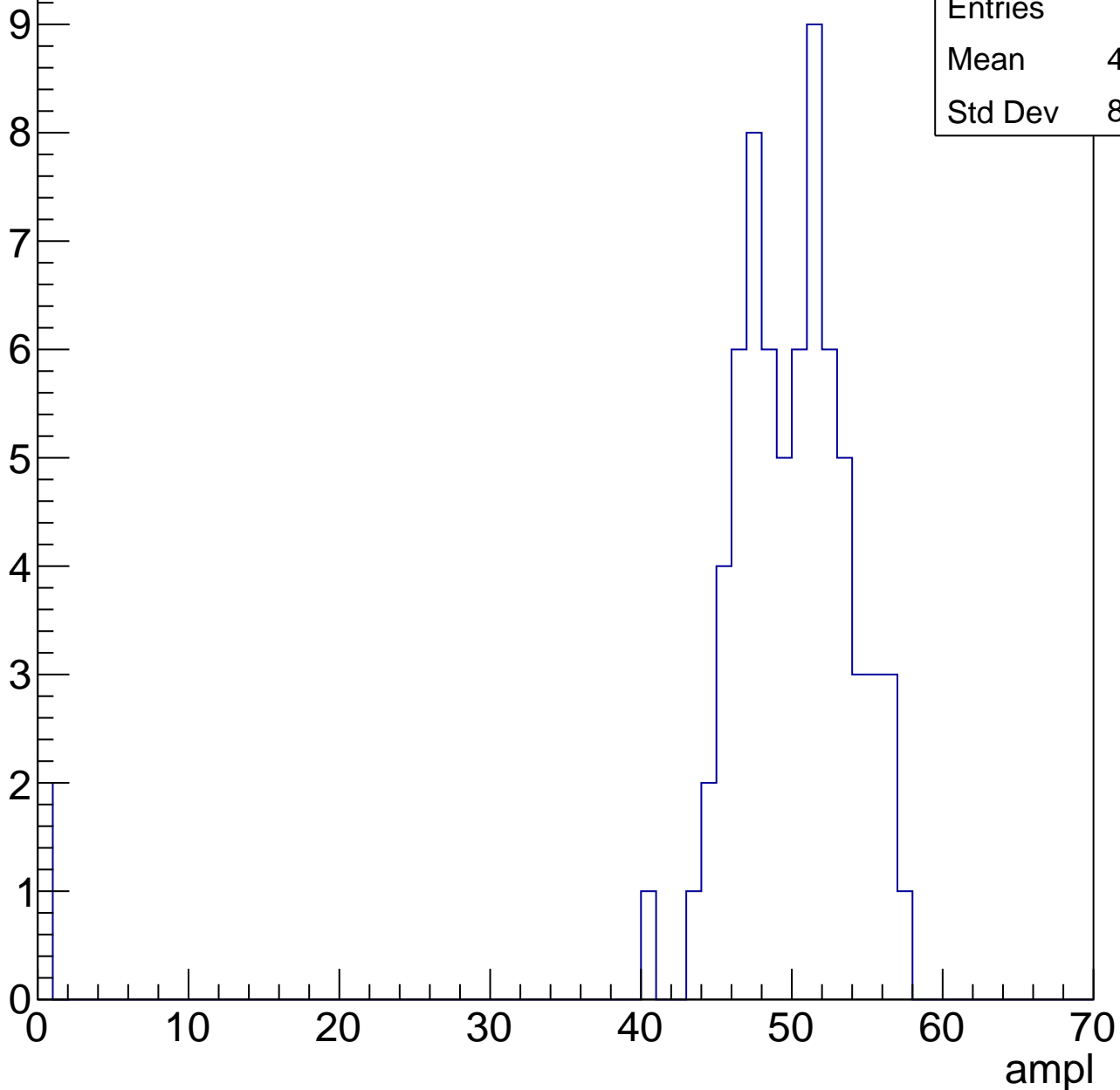


# B1L103S, U25-ch101, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	71
Mean	48.23
Std Dev	8.923

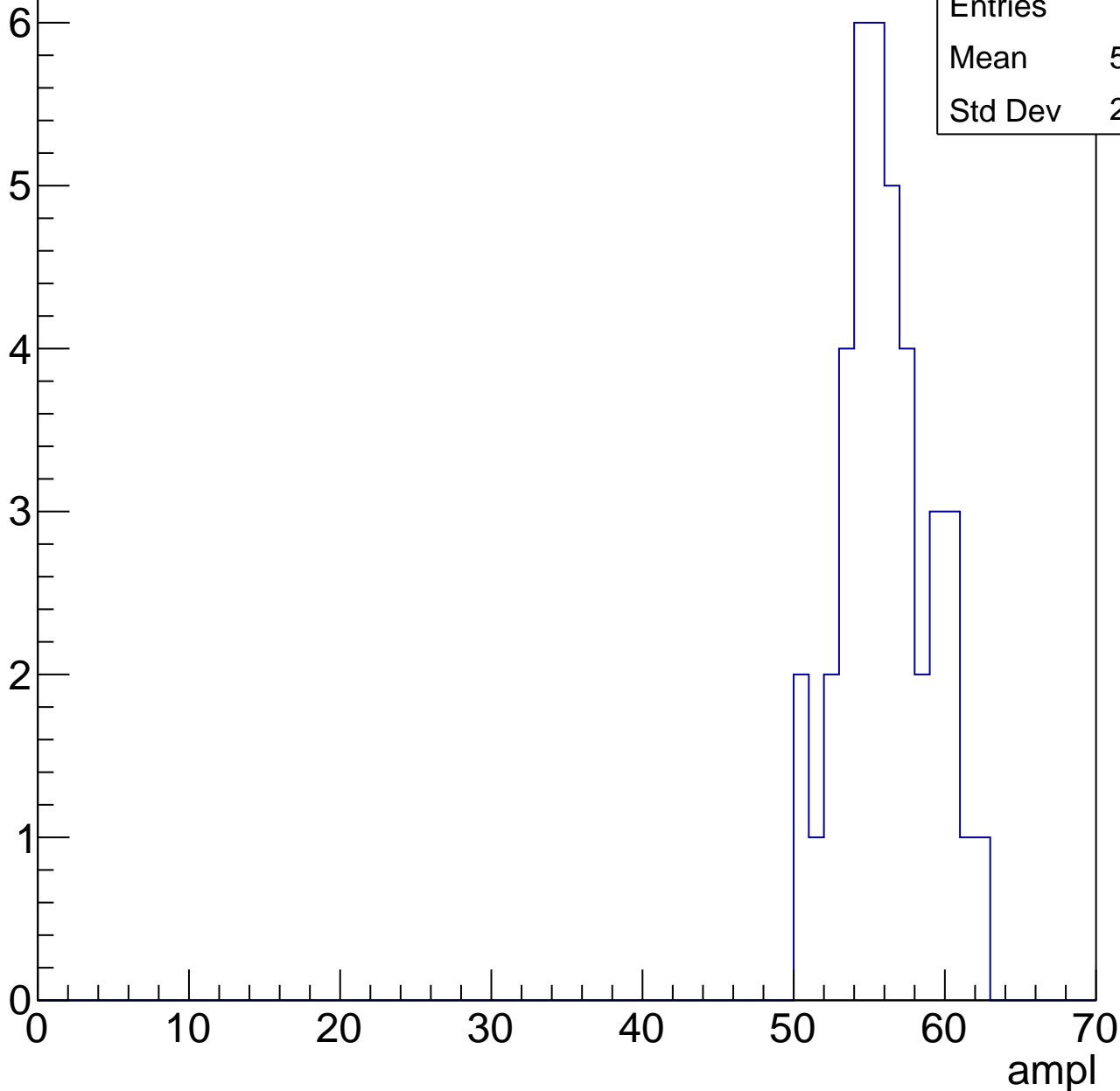


# B1L103S, U25-ch101, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	40
Mean	55.62
Std Dev	2.904

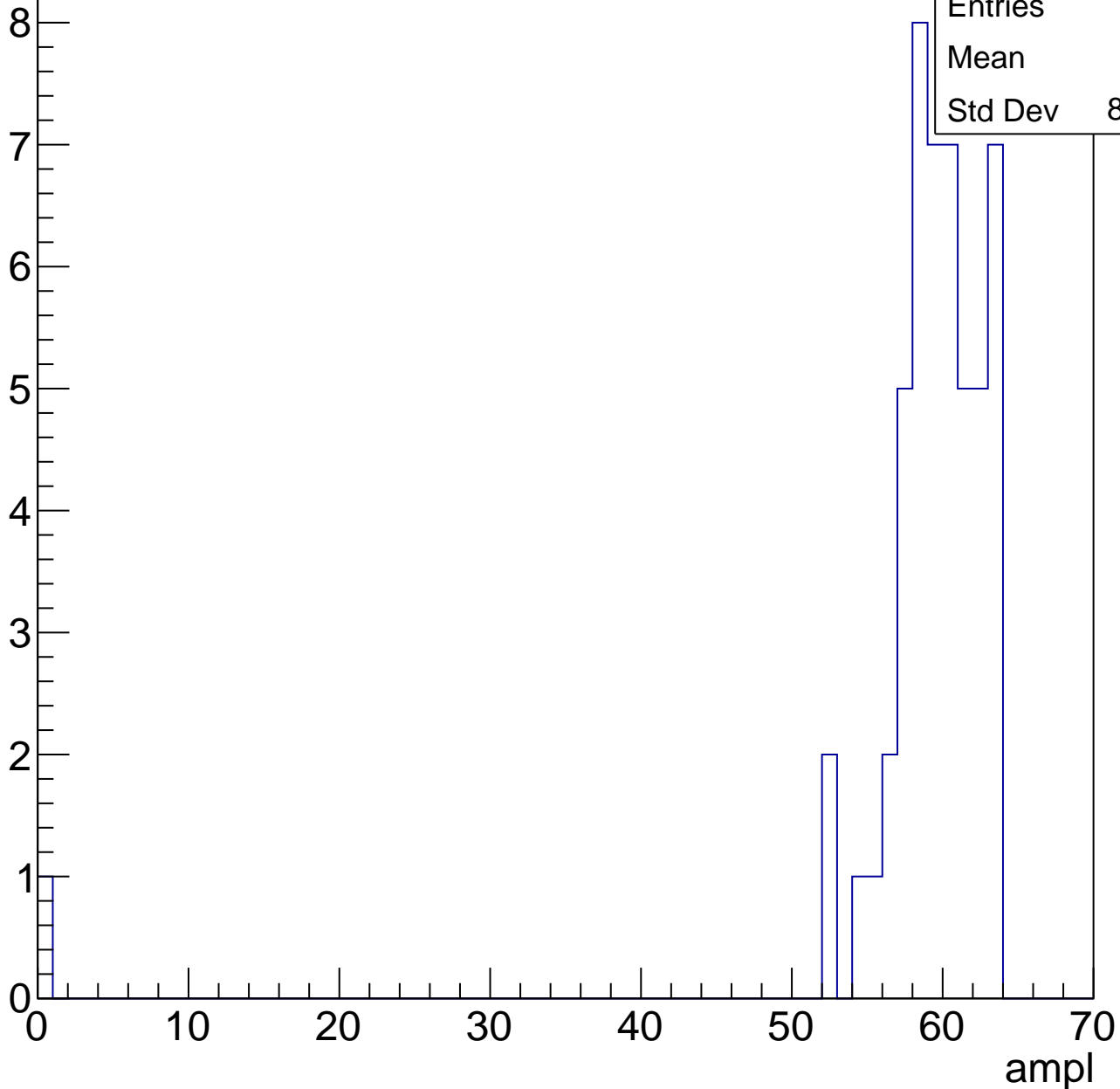


# B1L103S, U25-ch101, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

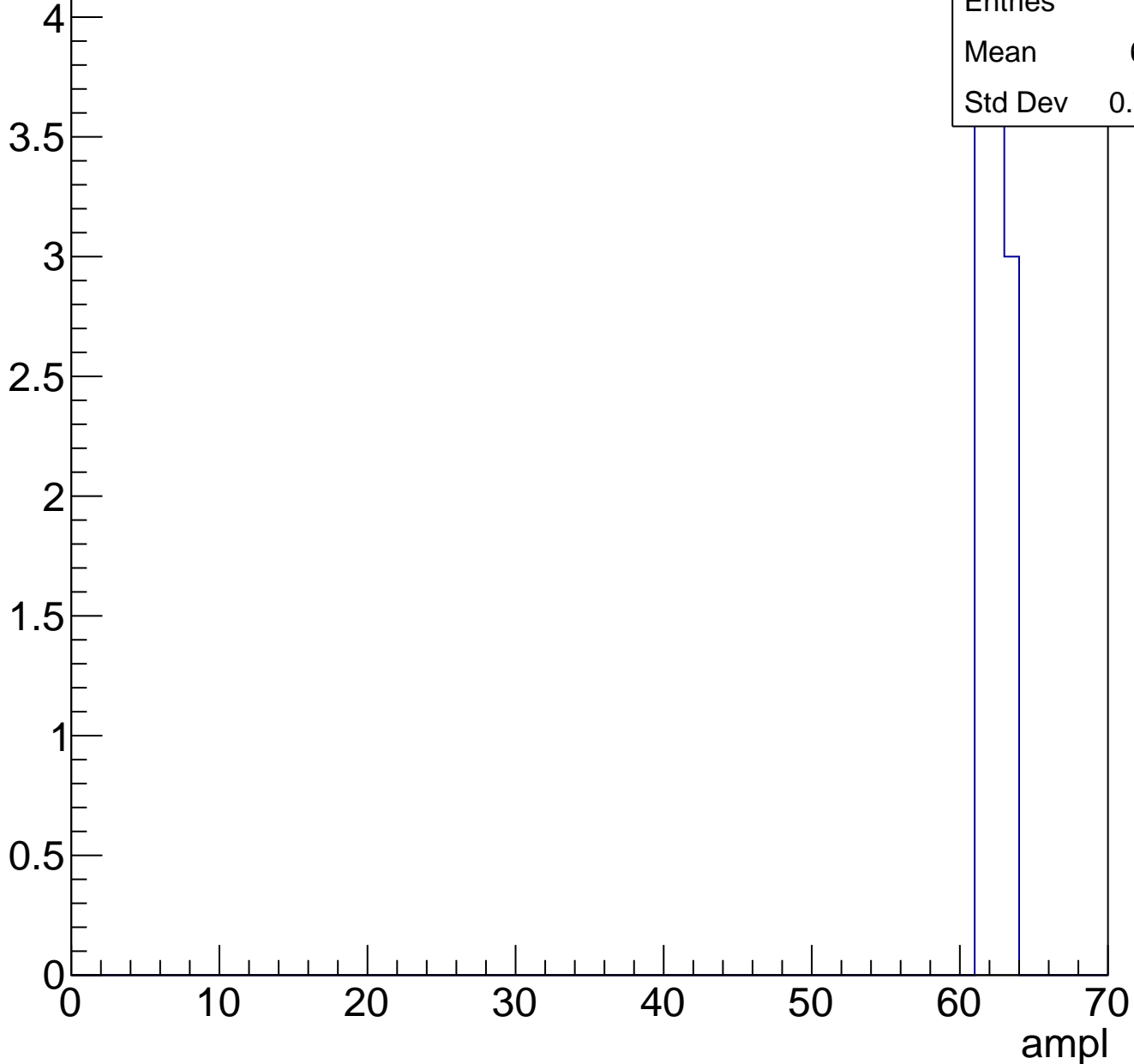
Entries	51
Mean	58.1
Std Dev	8.642



# B1L103S, U25-ch101, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U25-ch101, adc7

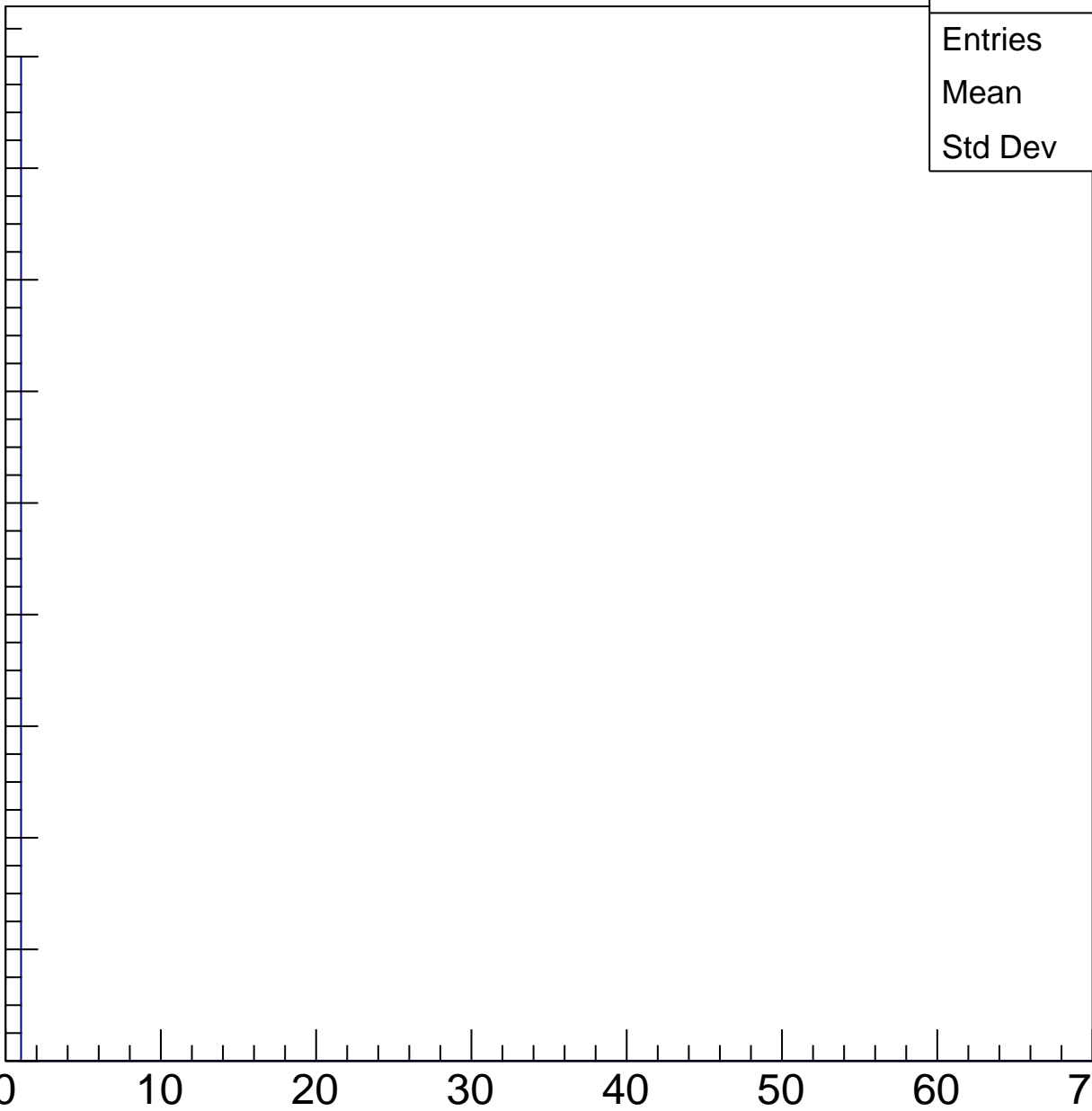
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Entries	18
Mean	0
Std Dev	0

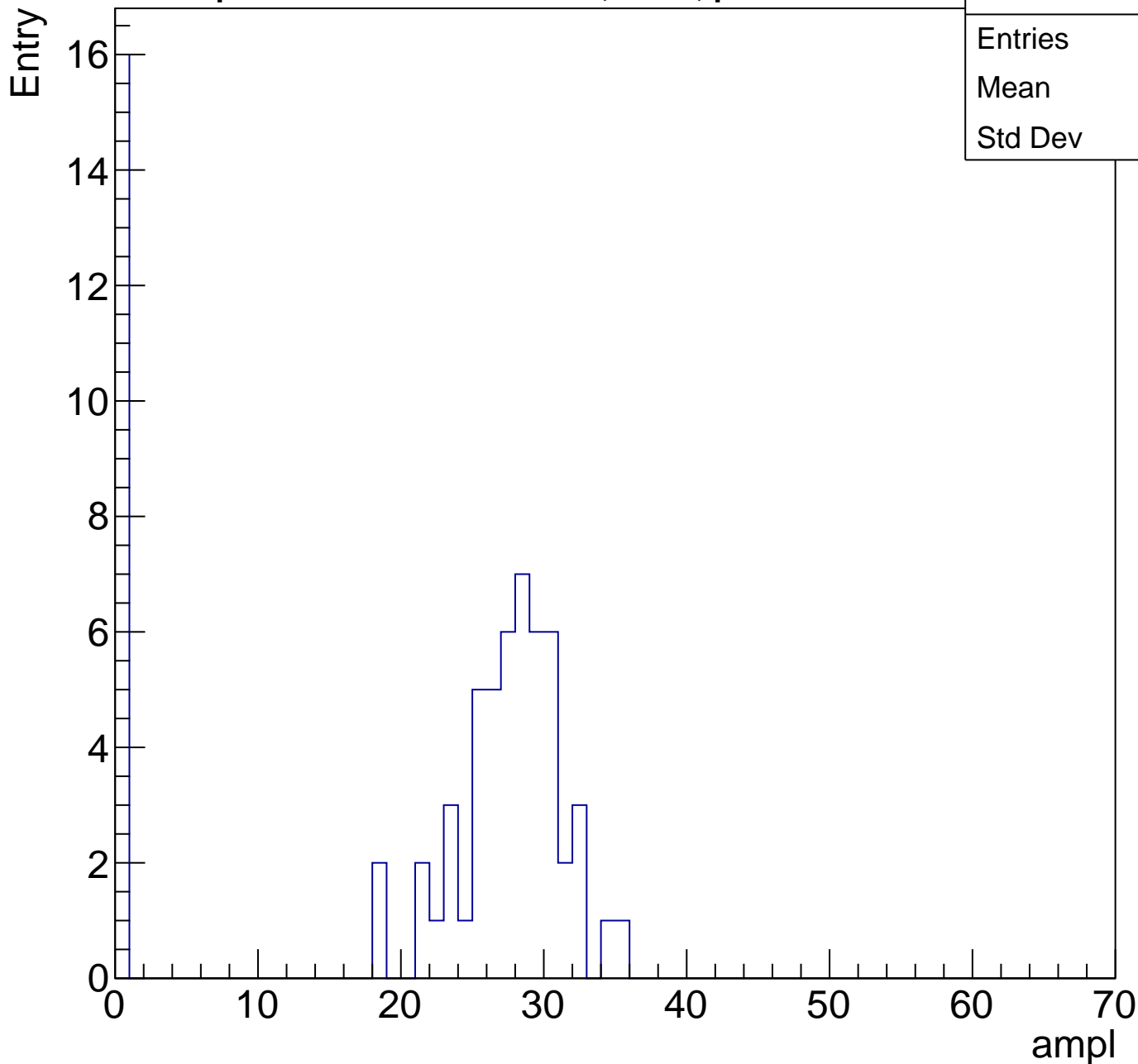
ampl



# B1L103S, U25-ch102, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	67
Mean	20.7
Std Dev	12



# B1L103S, U25-ch102, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

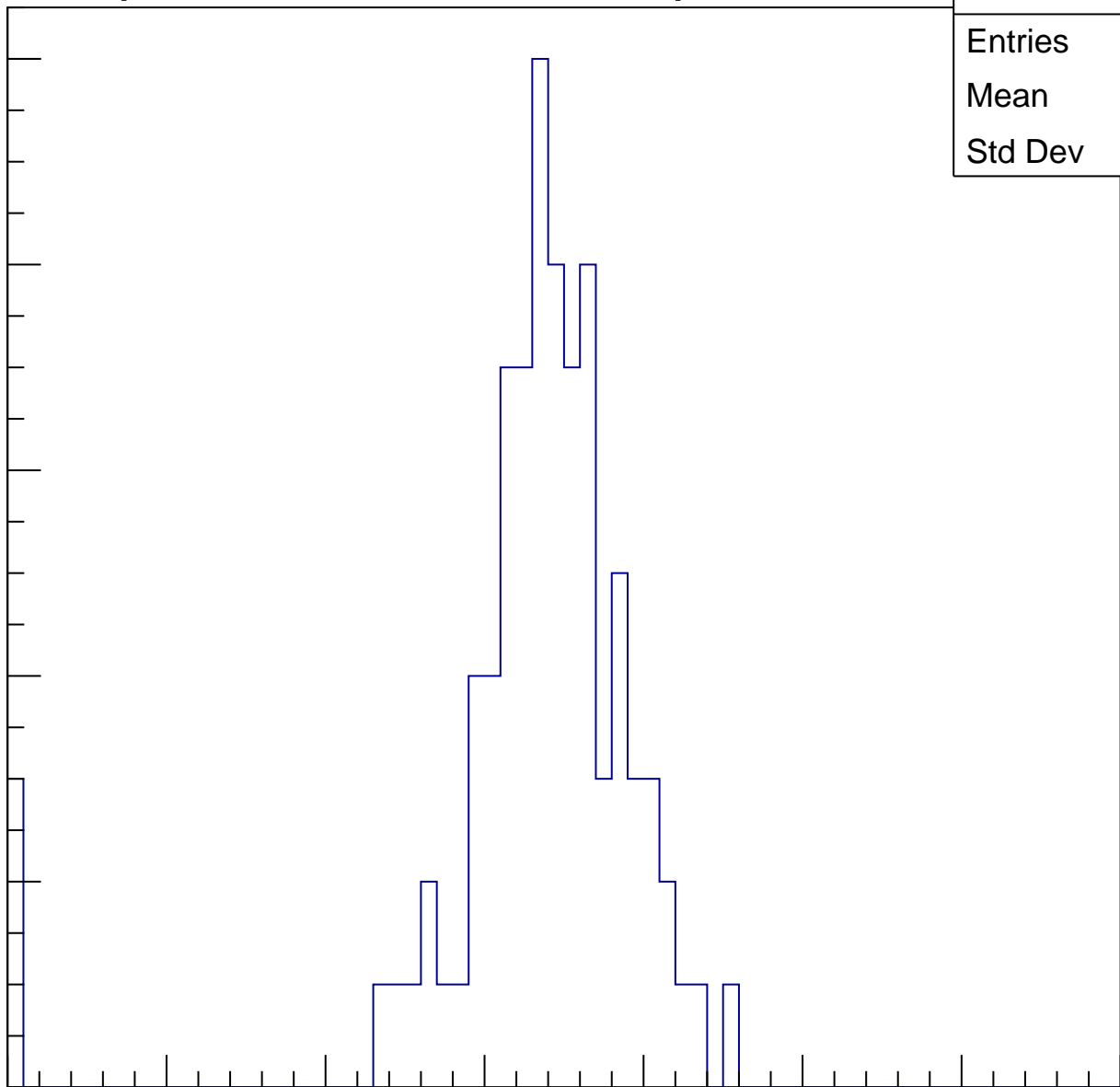
Entries	84
Mean	32.63
Std Dev	7.546

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

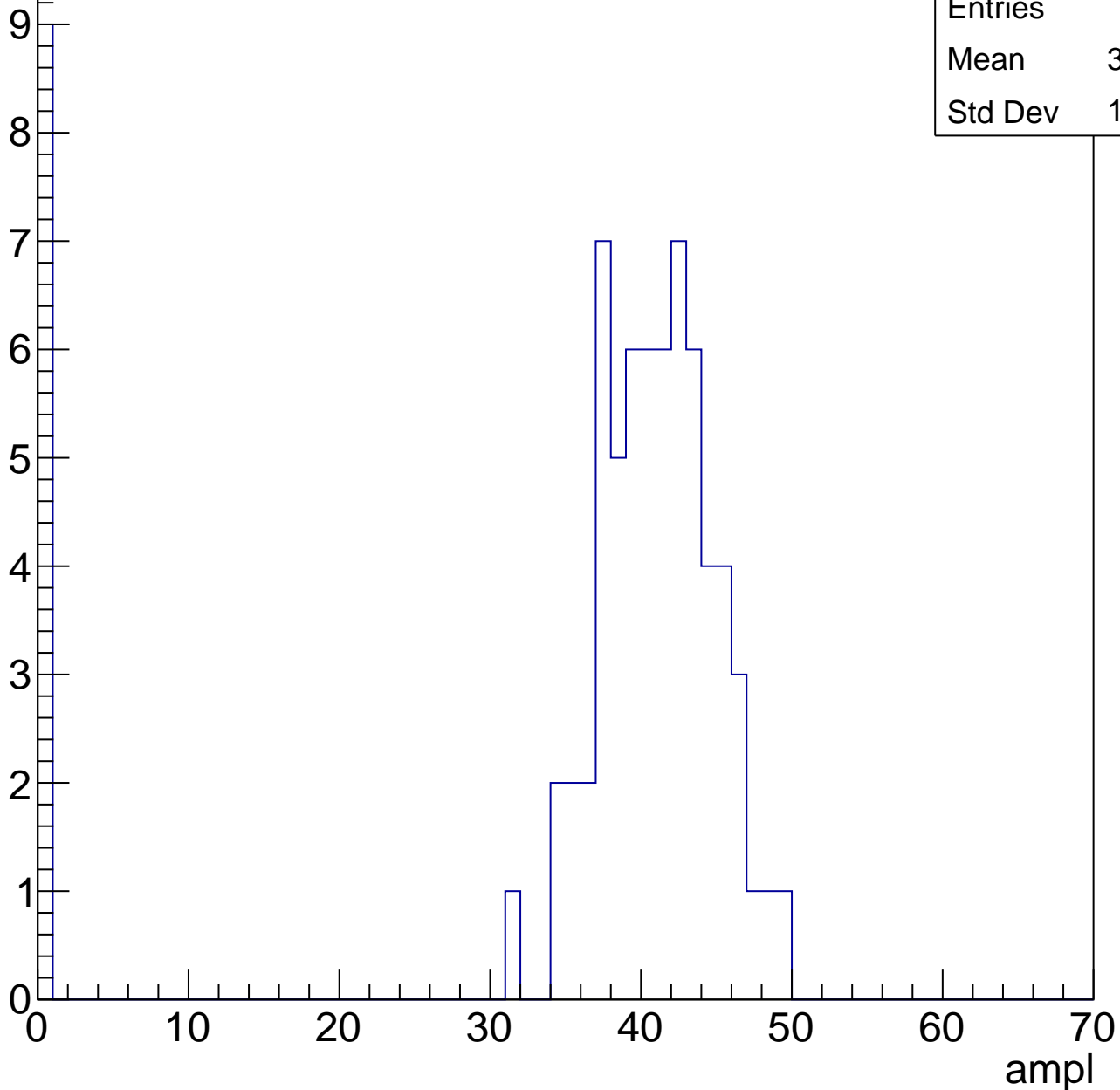


# B1L103S, U25-ch102, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	73
Mean	35.62
Std Dev	13.79

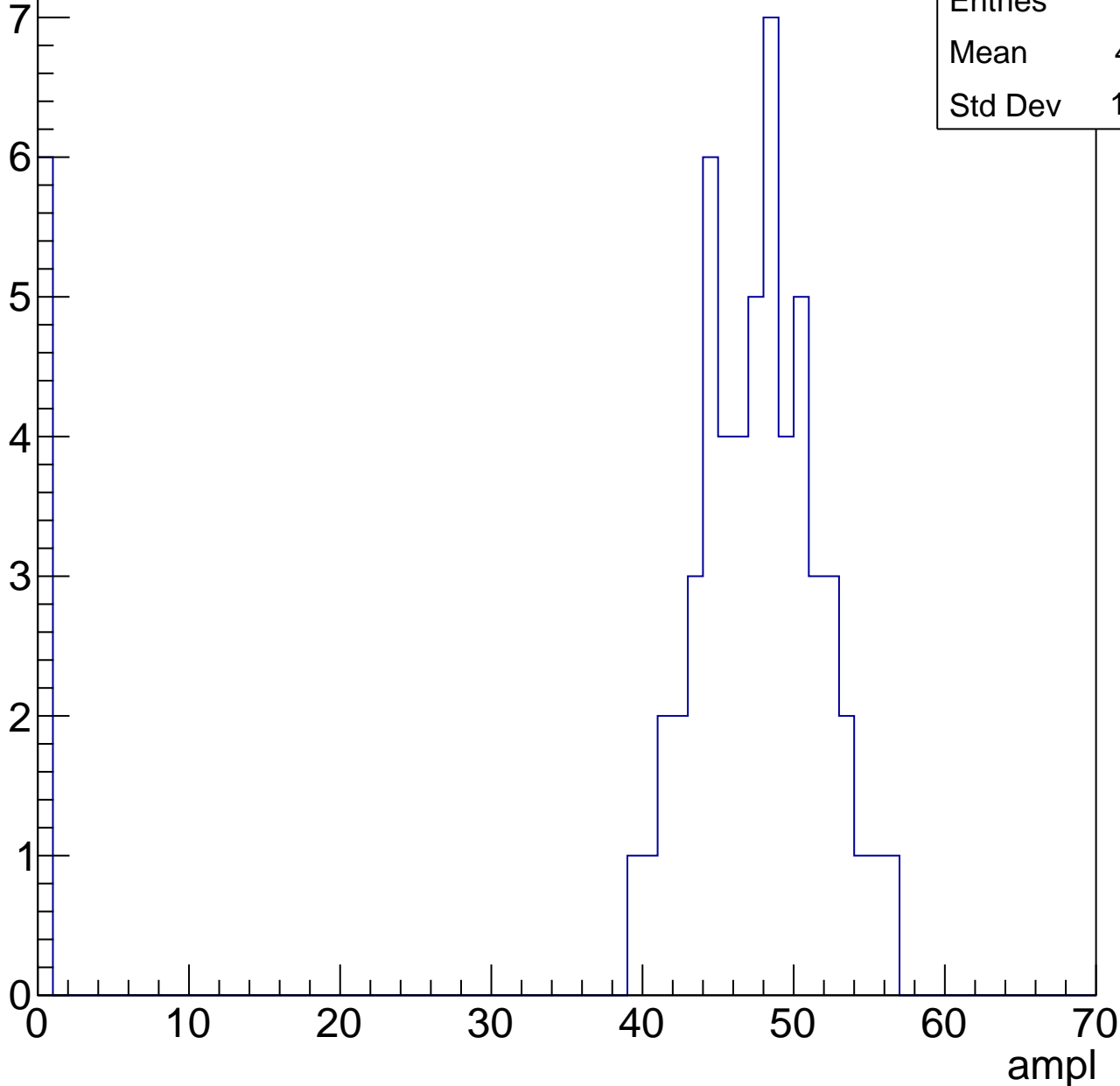


# B1L103S, U25-ch102, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	61
Mean	42.61
Std Dev	14.54

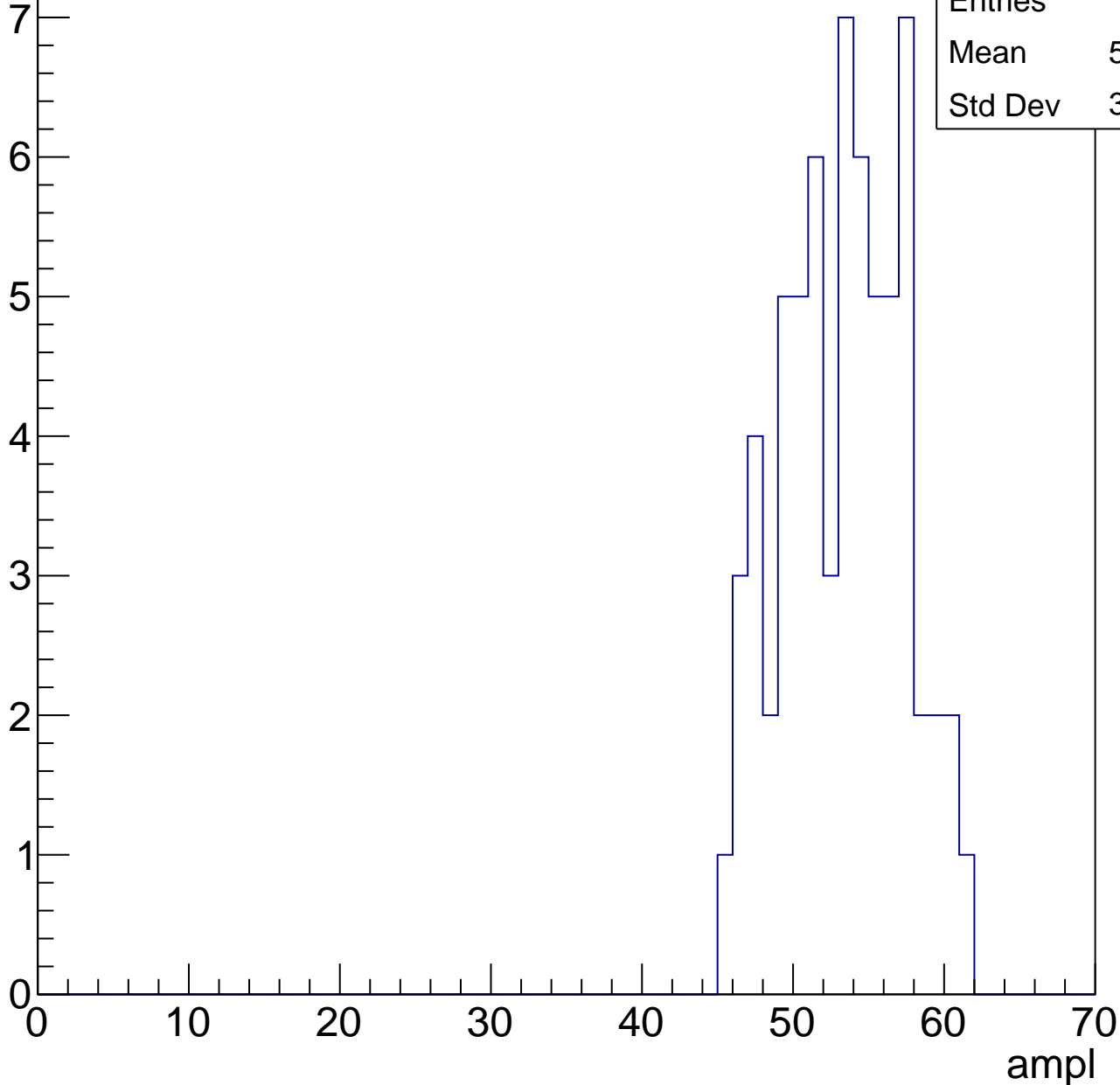


# B1L103S, U25-ch102, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	66
Mean	52.85
Std Dev	3.936

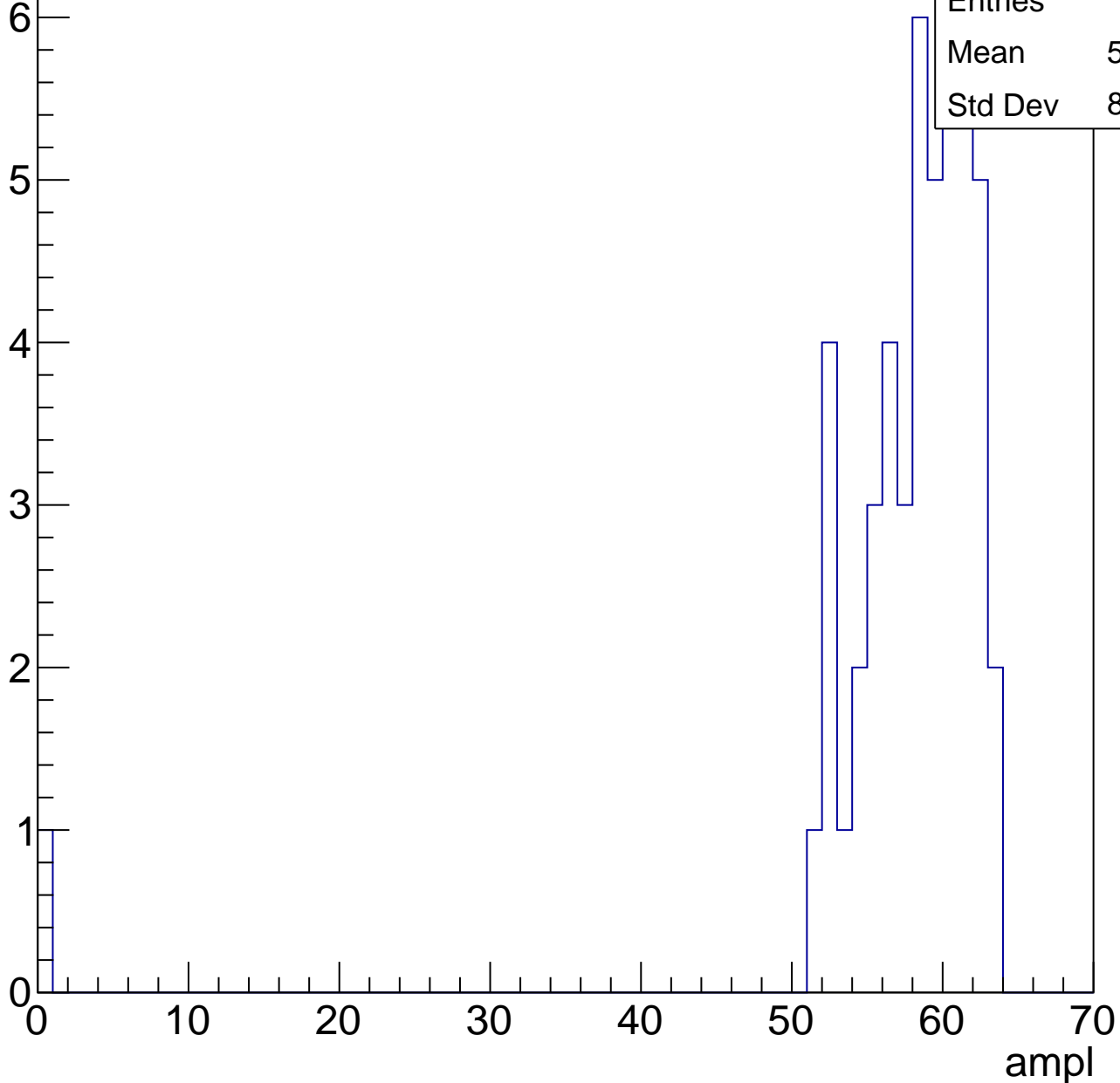


# B1L103S, U25-ch102, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	49
Mean	56.84
Std Dev	8.814

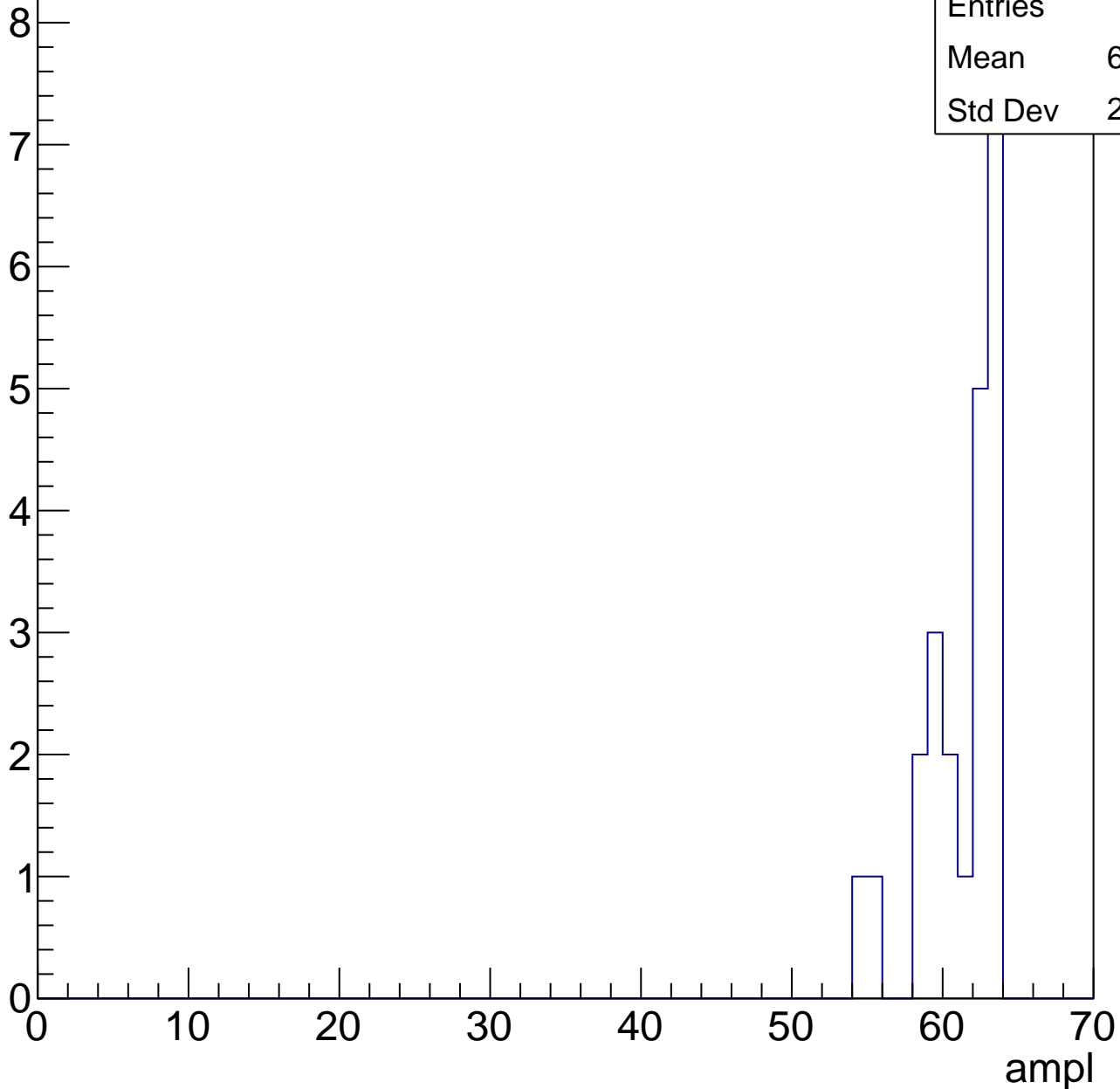


# B1L103S, U25-ch102, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	23
Mean	60.74
Std Dev	2.574

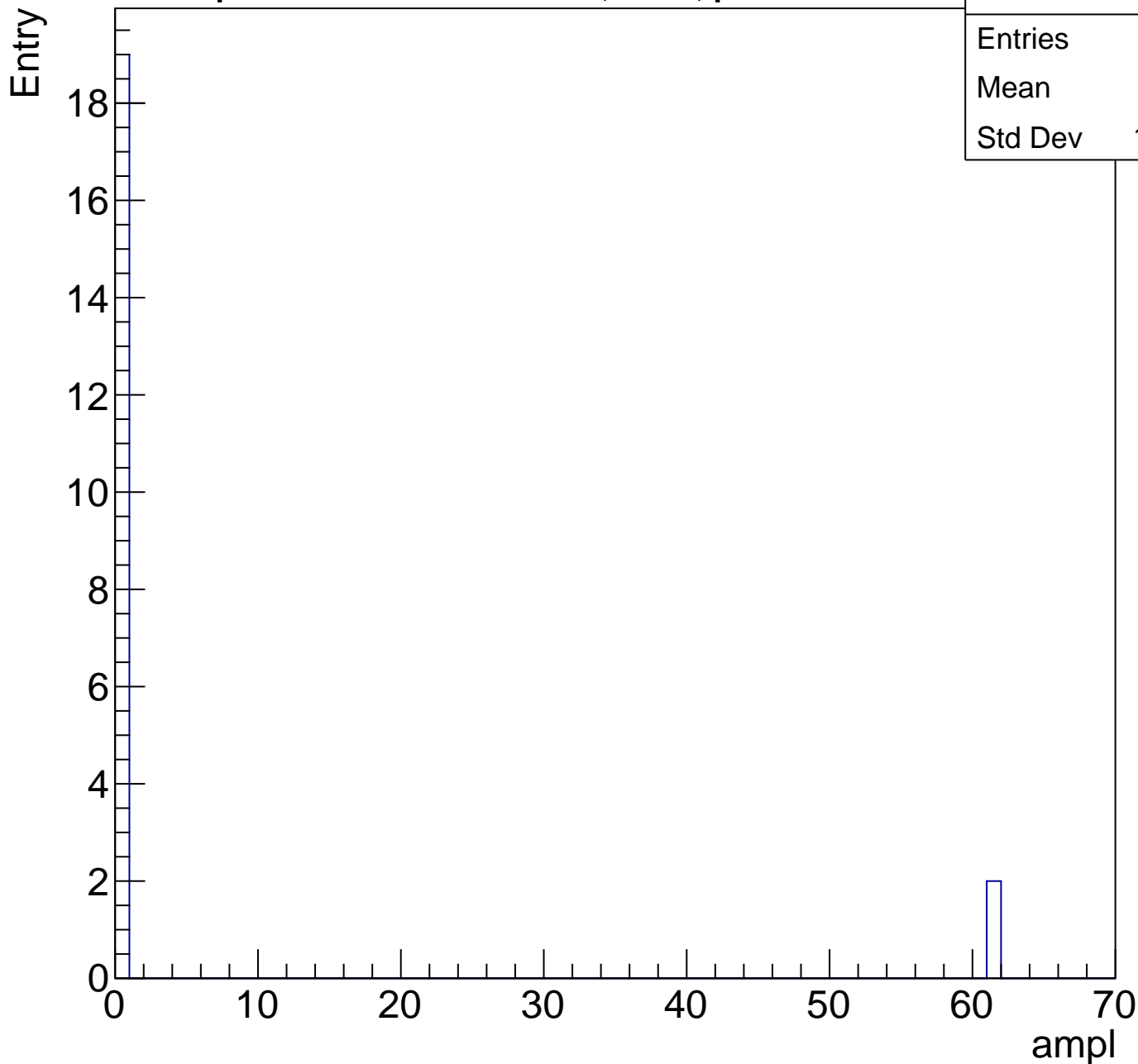




# B1L103S, U25-ch102, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

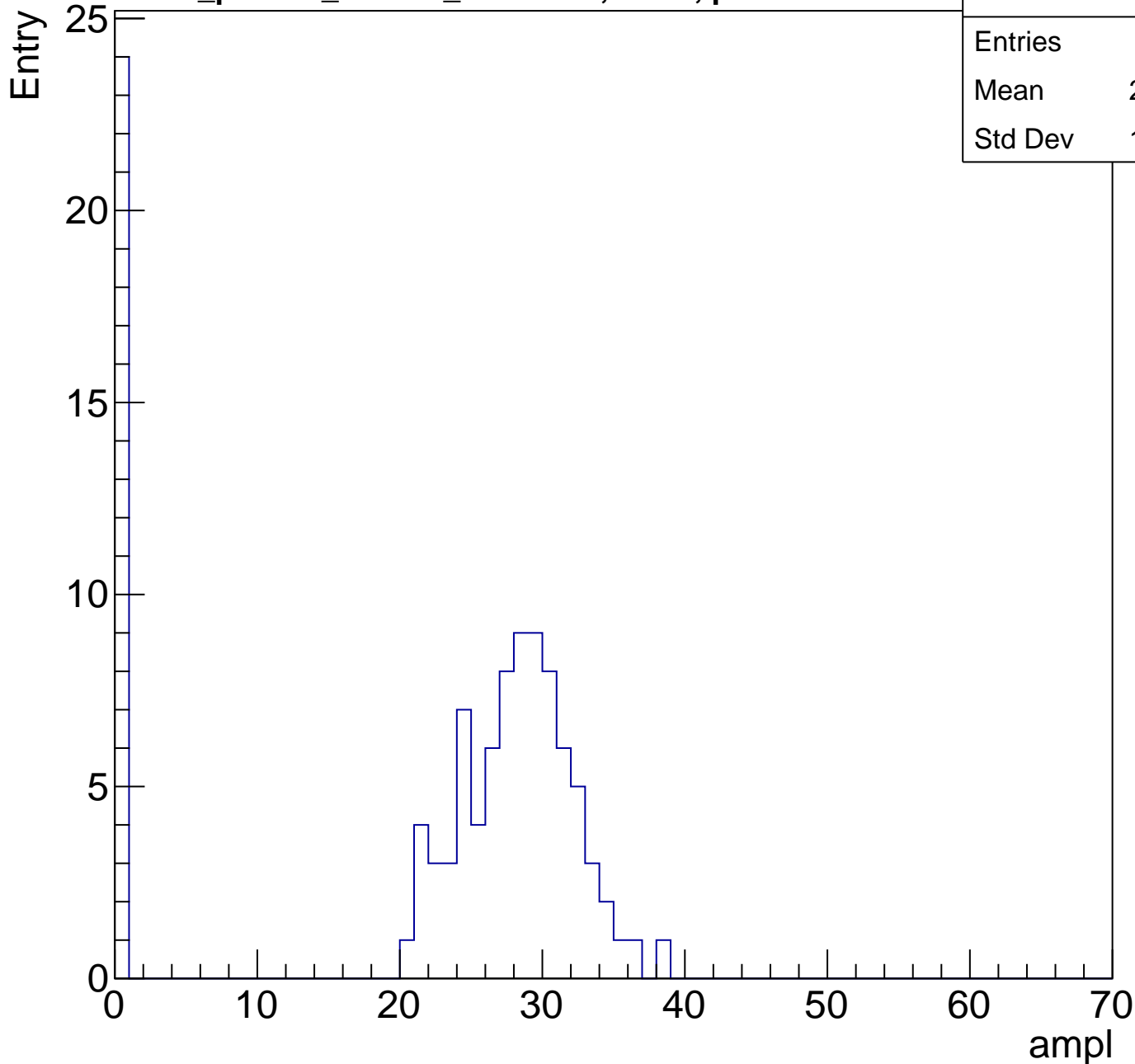
Entries	21
Mean	5.81
Std Dev	17.91



# B1L103S, U25-ch103, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

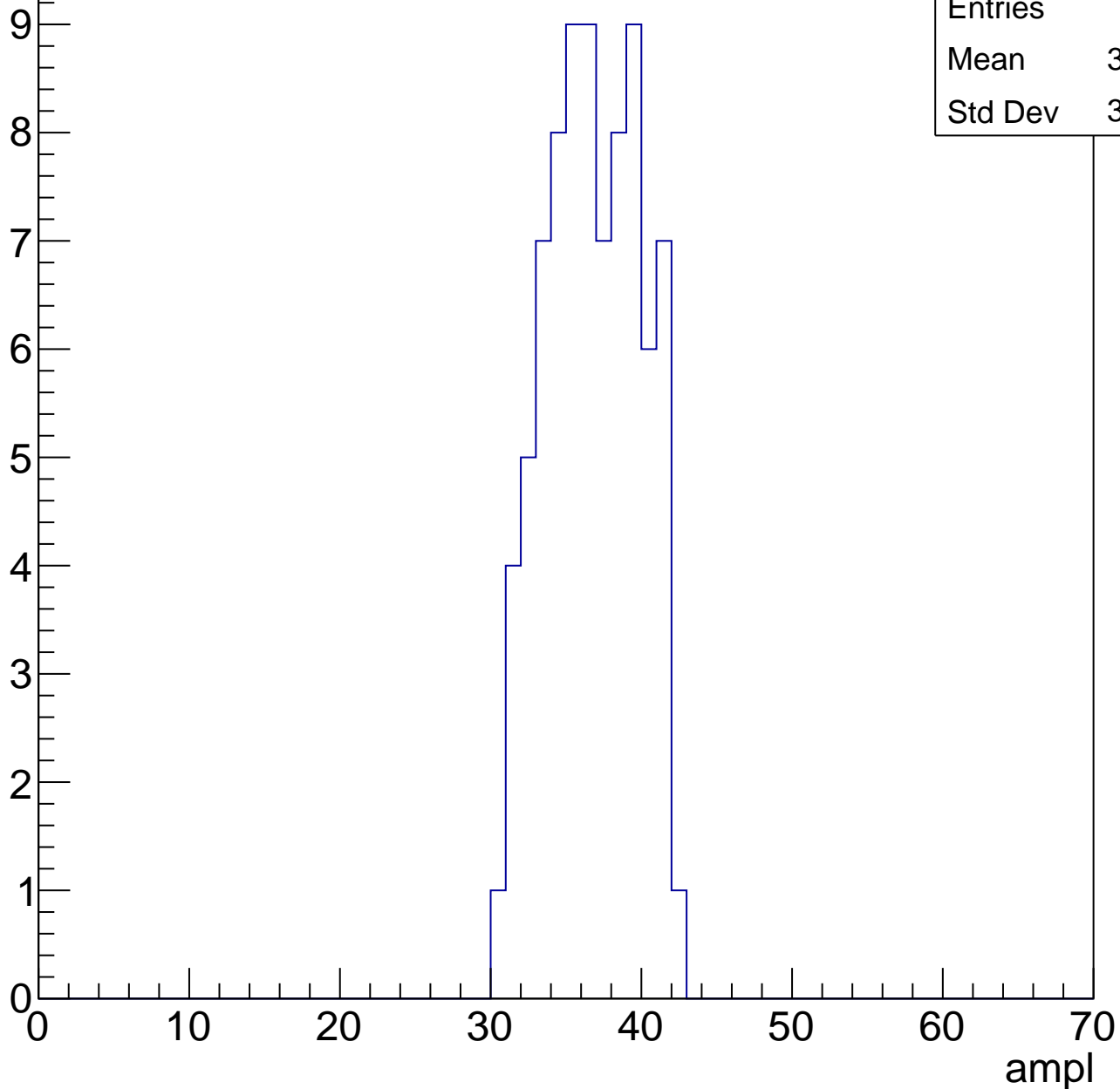
Entries	105
Mean	21.47
Std Dev	12.15



# B1L103S, U25-ch103, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	81
Mean	36.28
Std Dev	3.024

# B1L103S, U25-ch103, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	68
Mean	35.12
Std Dev	17.28

Entry

12

10

8

6

4

2

0

0

10

20

30

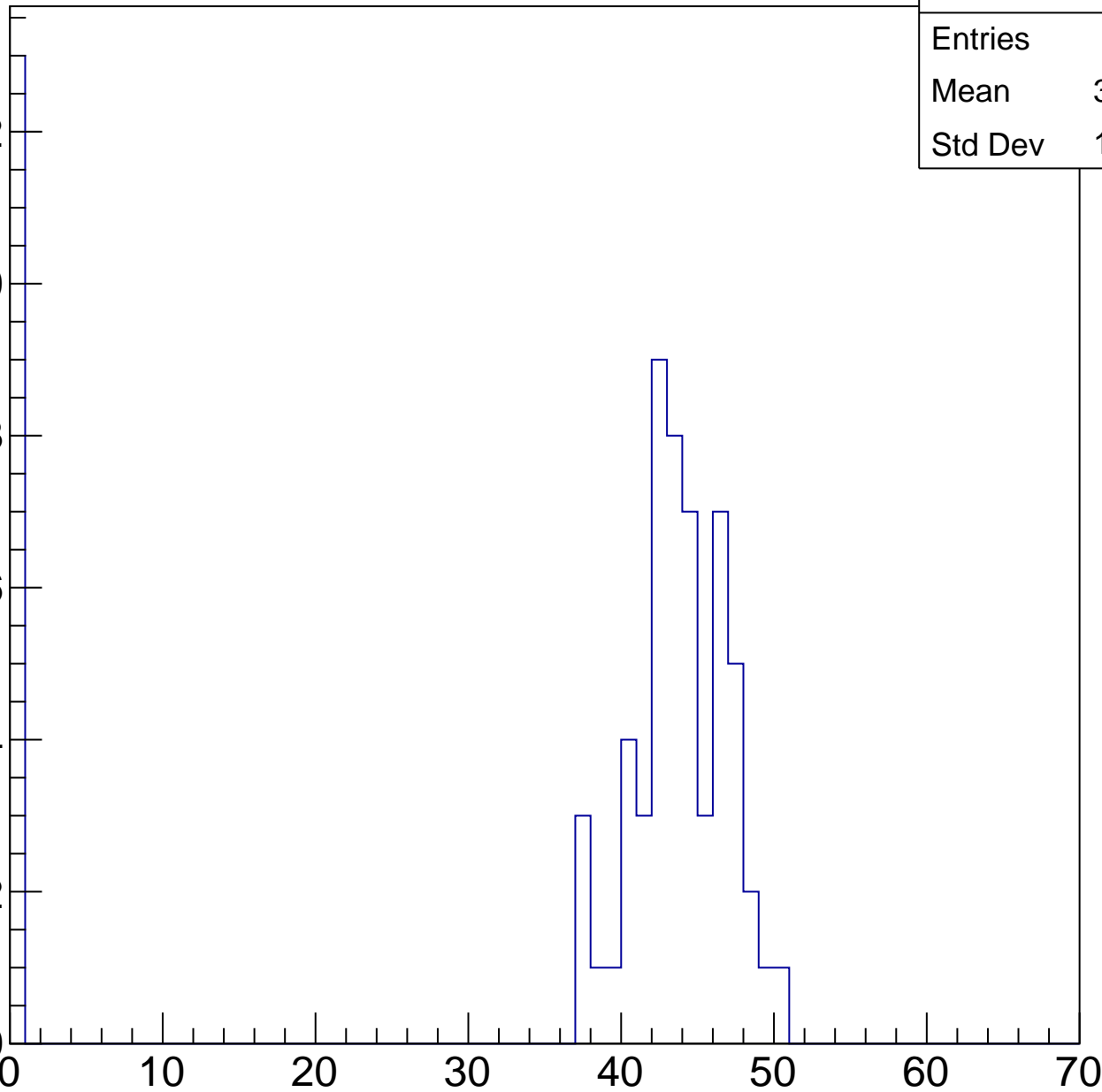
40

50

60

70

ampl

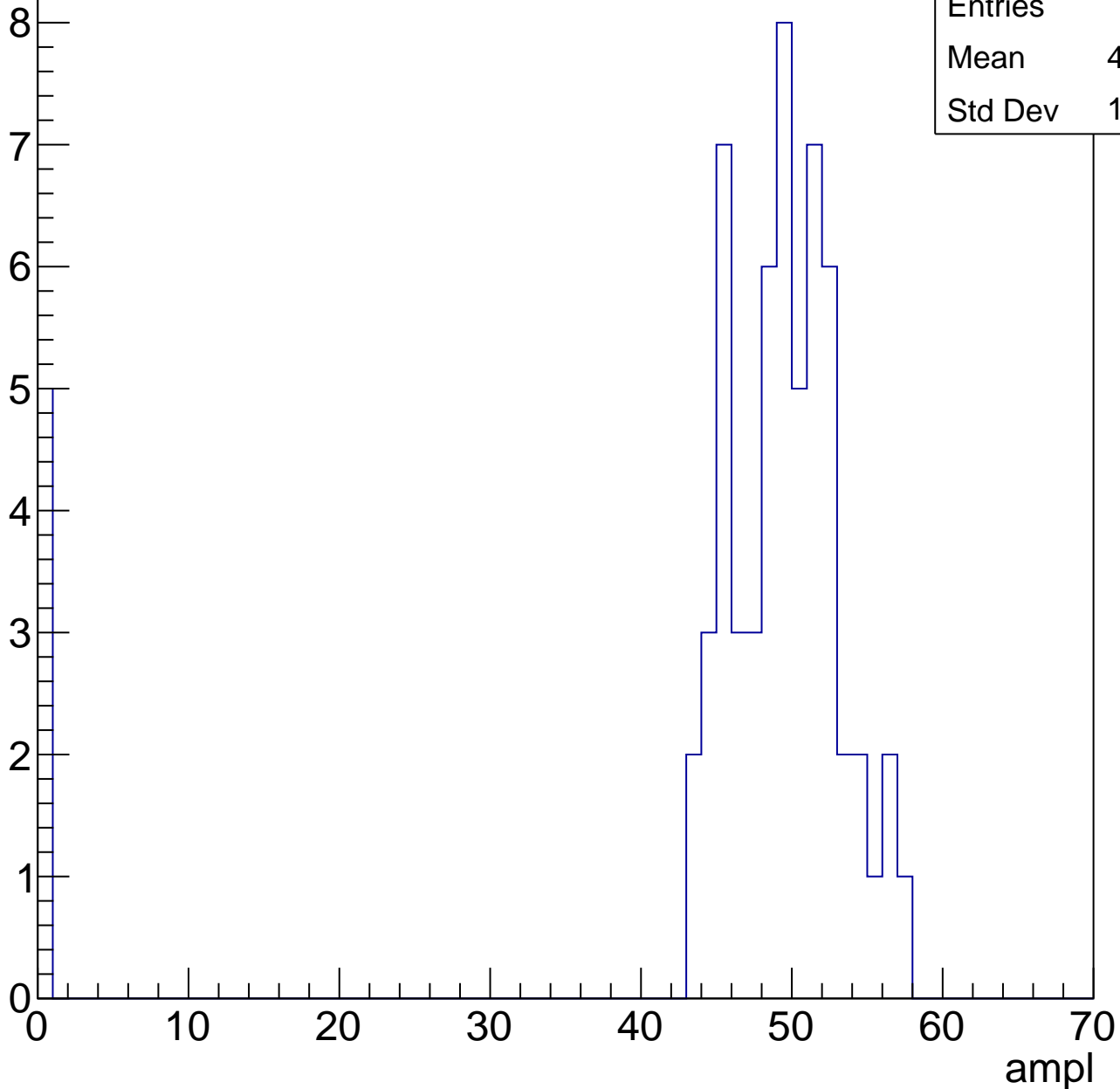


# B1L103S, U25-ch103, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	63
Mean	45.22
Std Dev	13.67

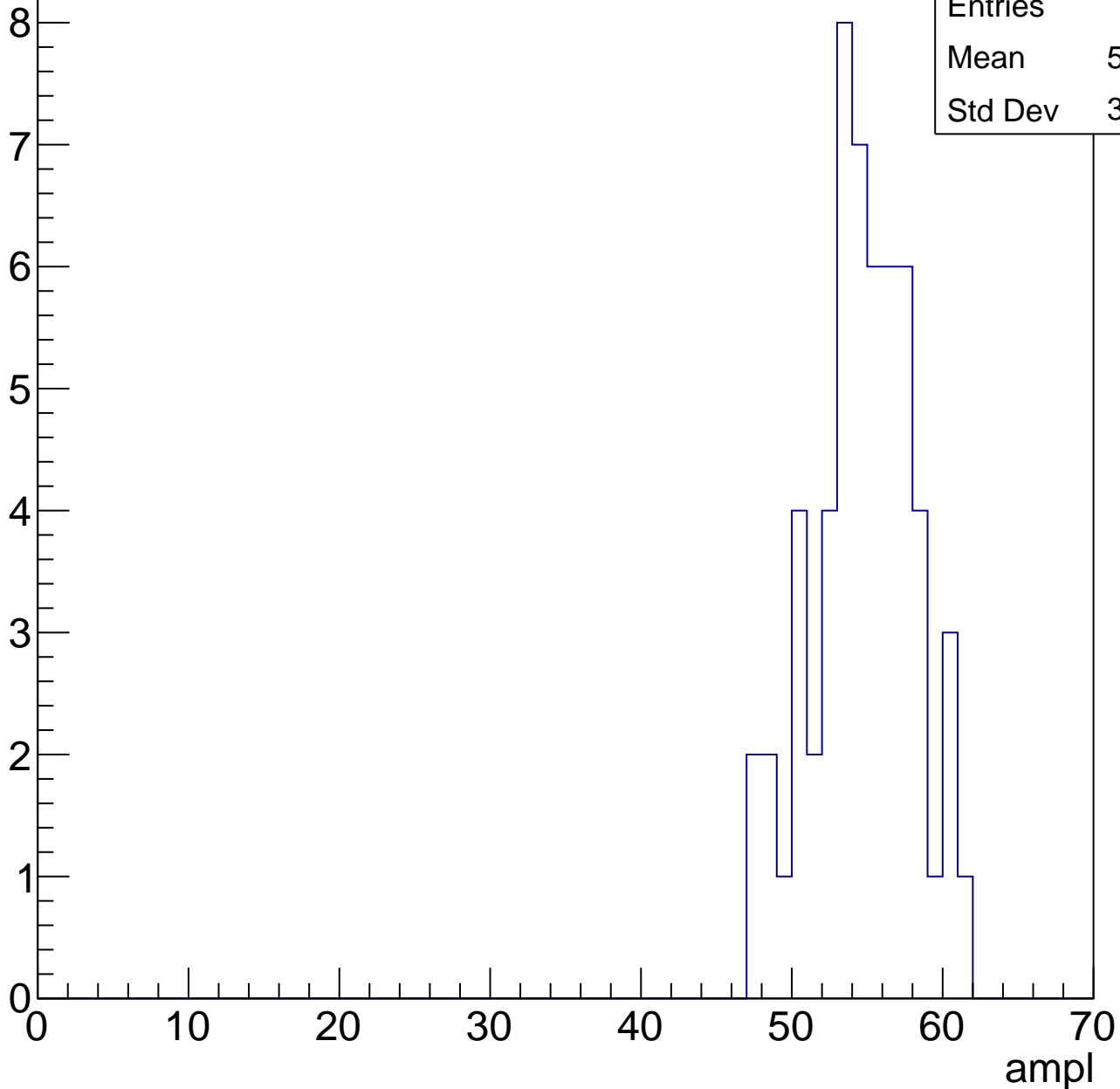


# B1L103S, U25-ch103, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	57
Mean	54.23
Std Dev	3.319

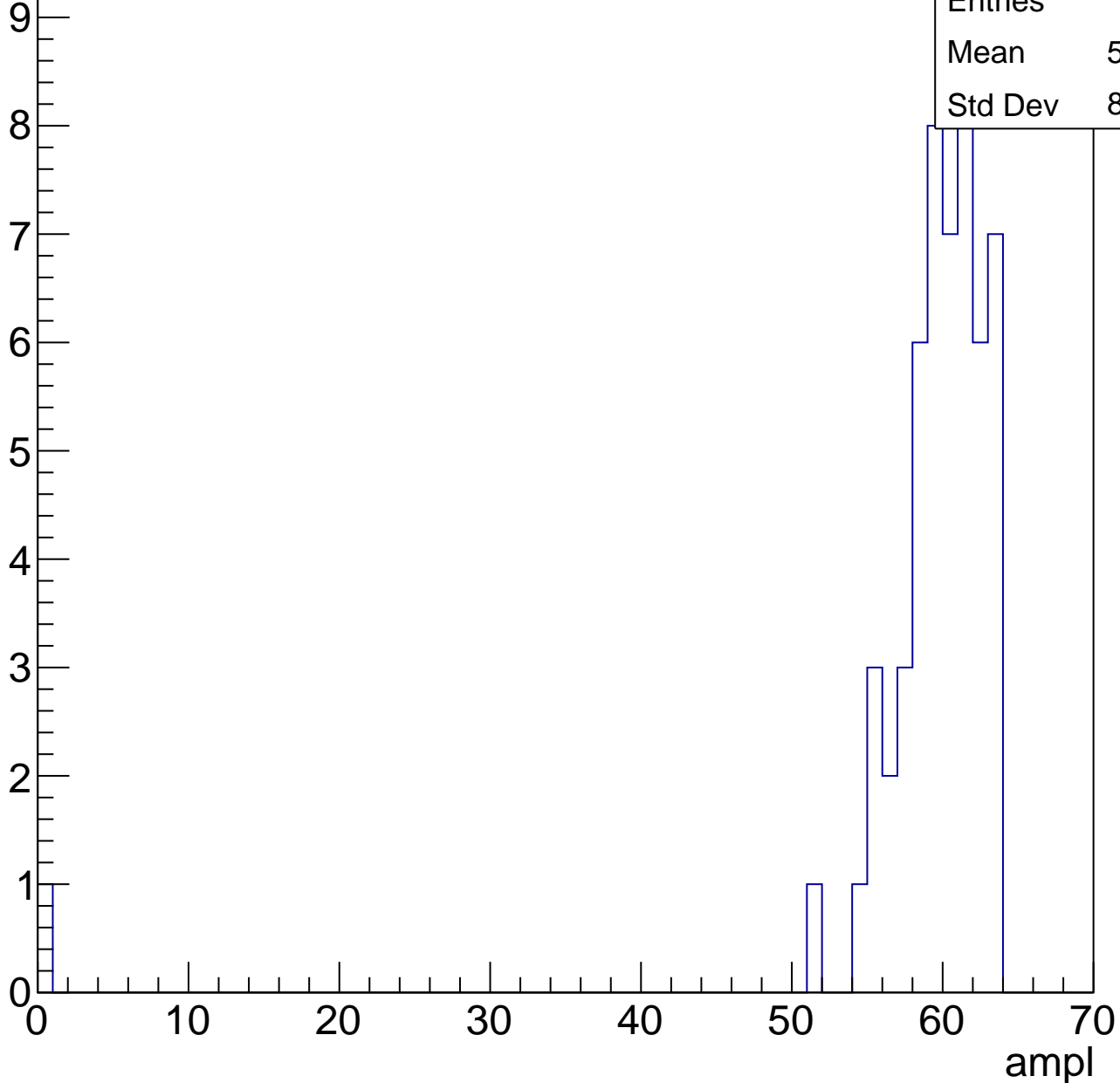


# B1L103S, U25-ch103, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

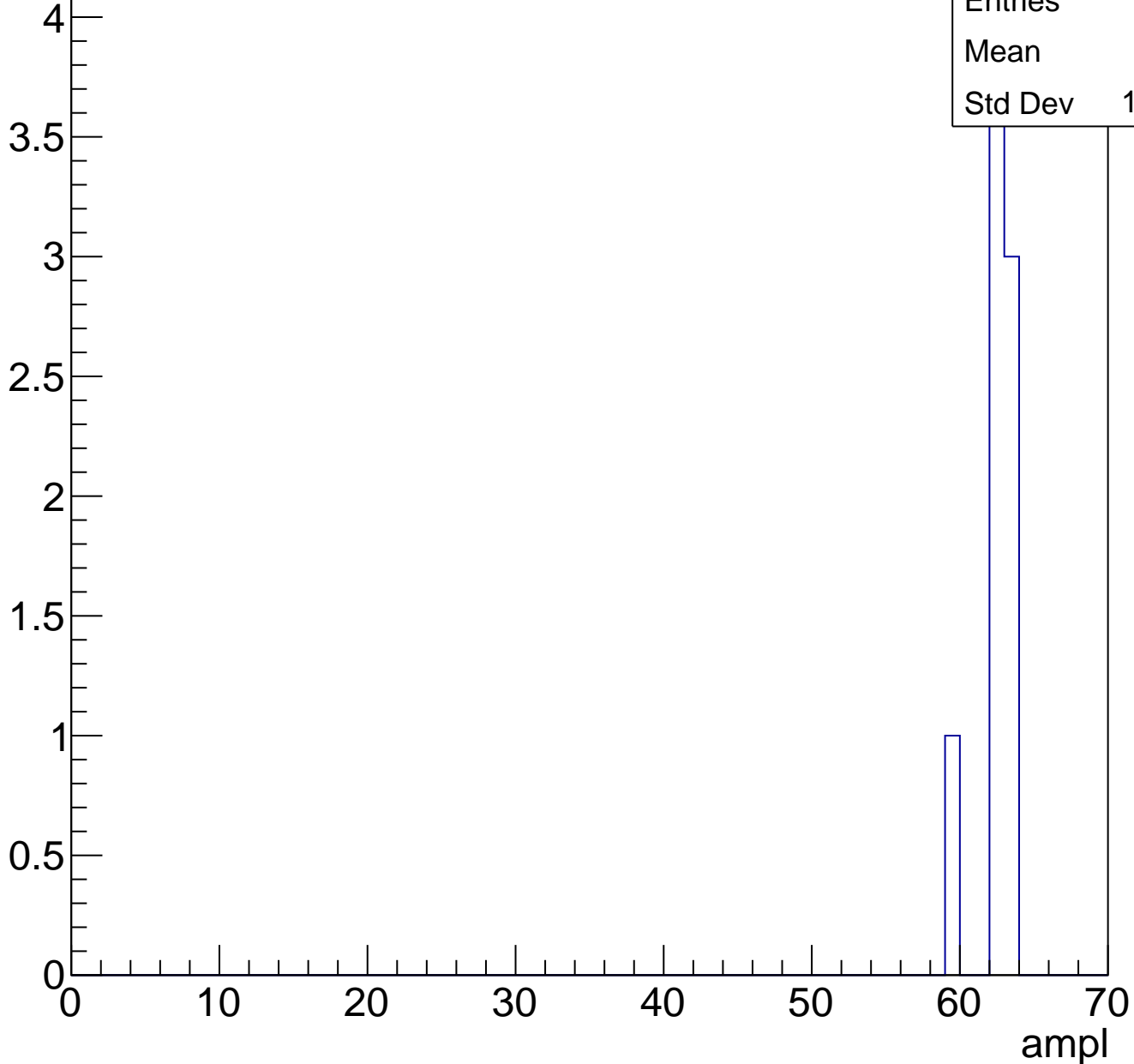
Entries	54
Mean	58.43
Std Dev	8.438



# B1L103S, U25-ch103, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



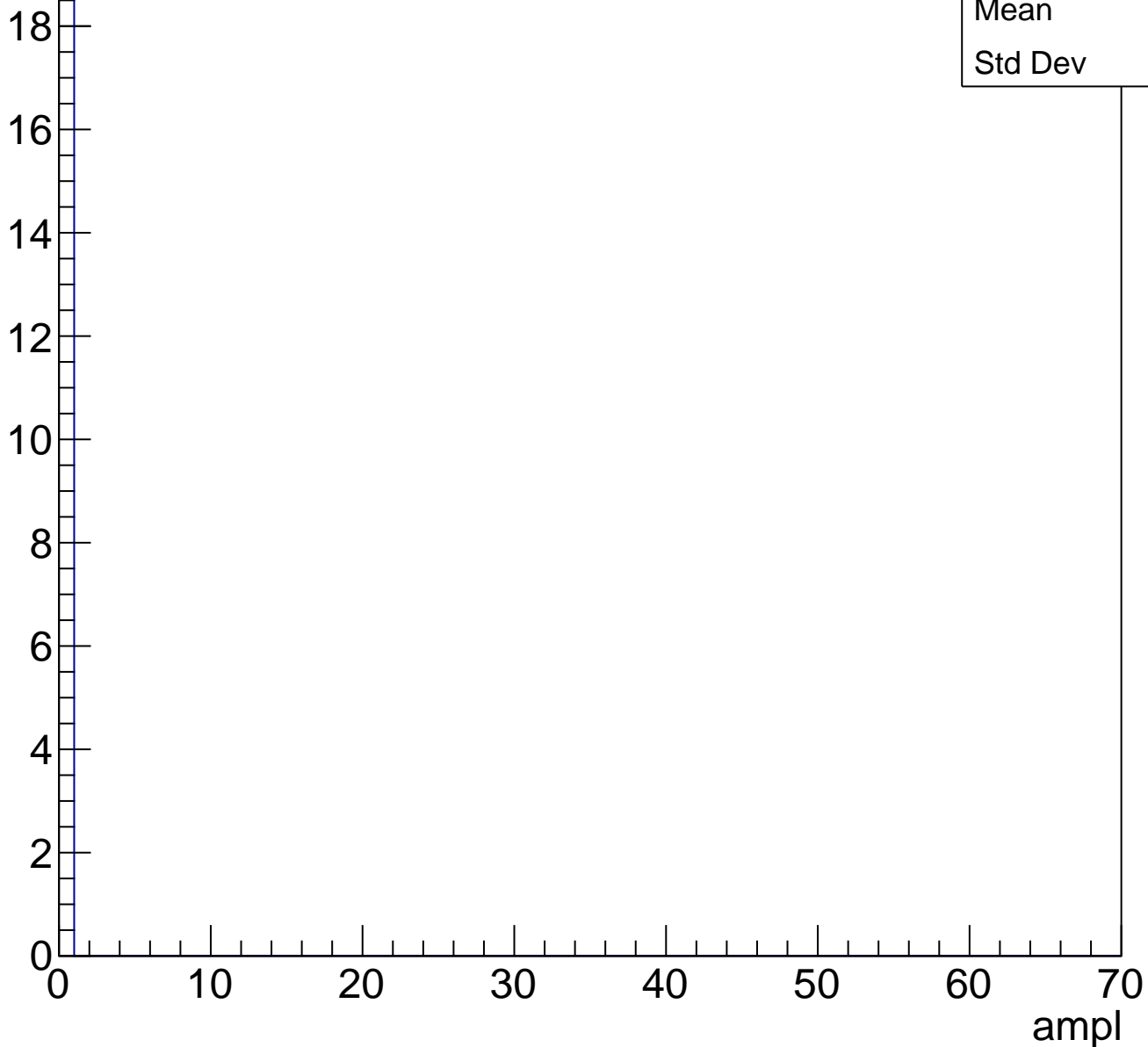


# B1L103S, U25-ch103, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	19
Mean	0
Std Dev	0

Entry



# B1L103S, U25-ch104, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

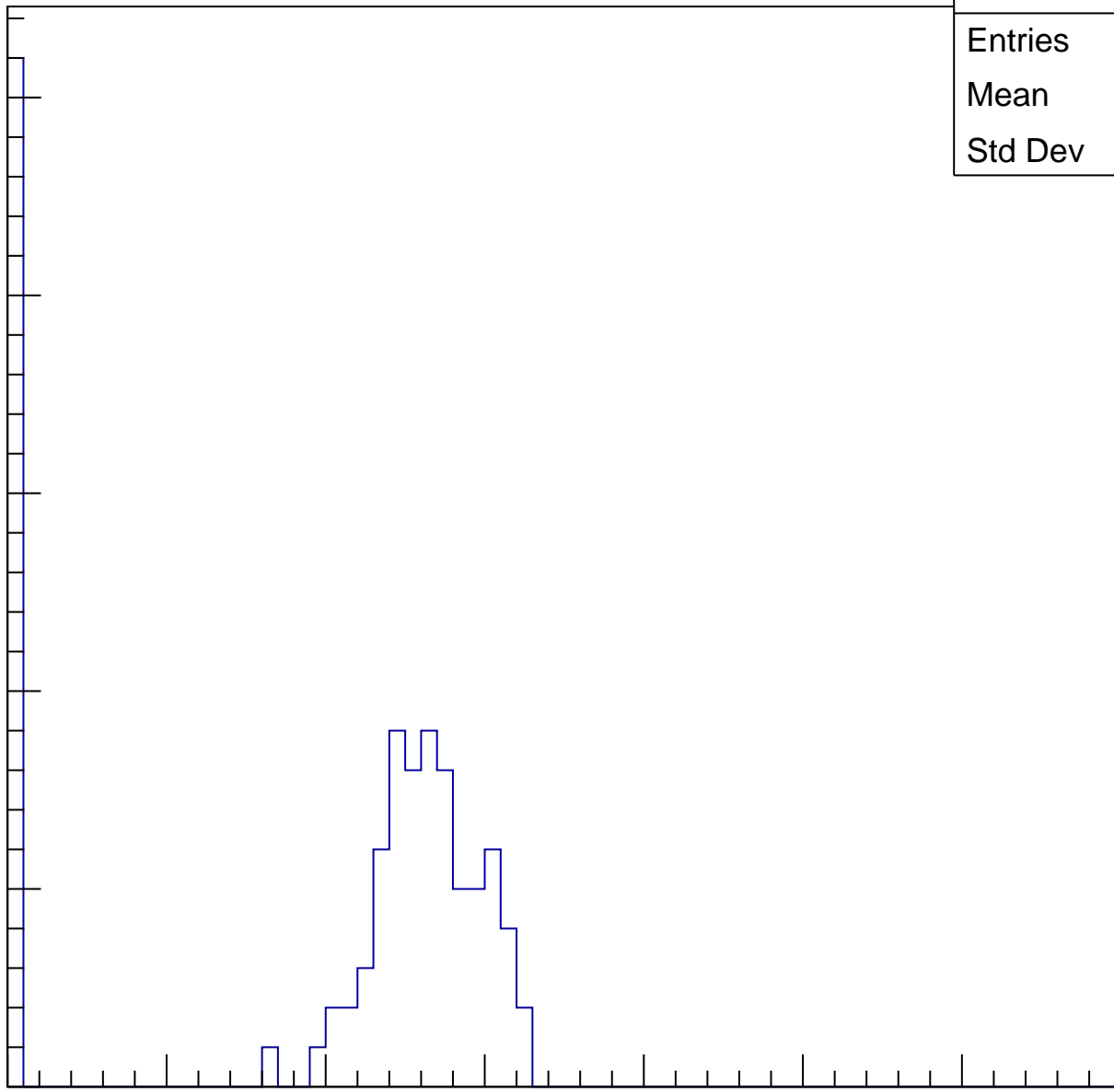
Entries	97
Mean	18.97
Std Dev	11.81

Entry

25  
20  
15  
10  
5  
0

0 10 20 30 40 50 60 70

ampl

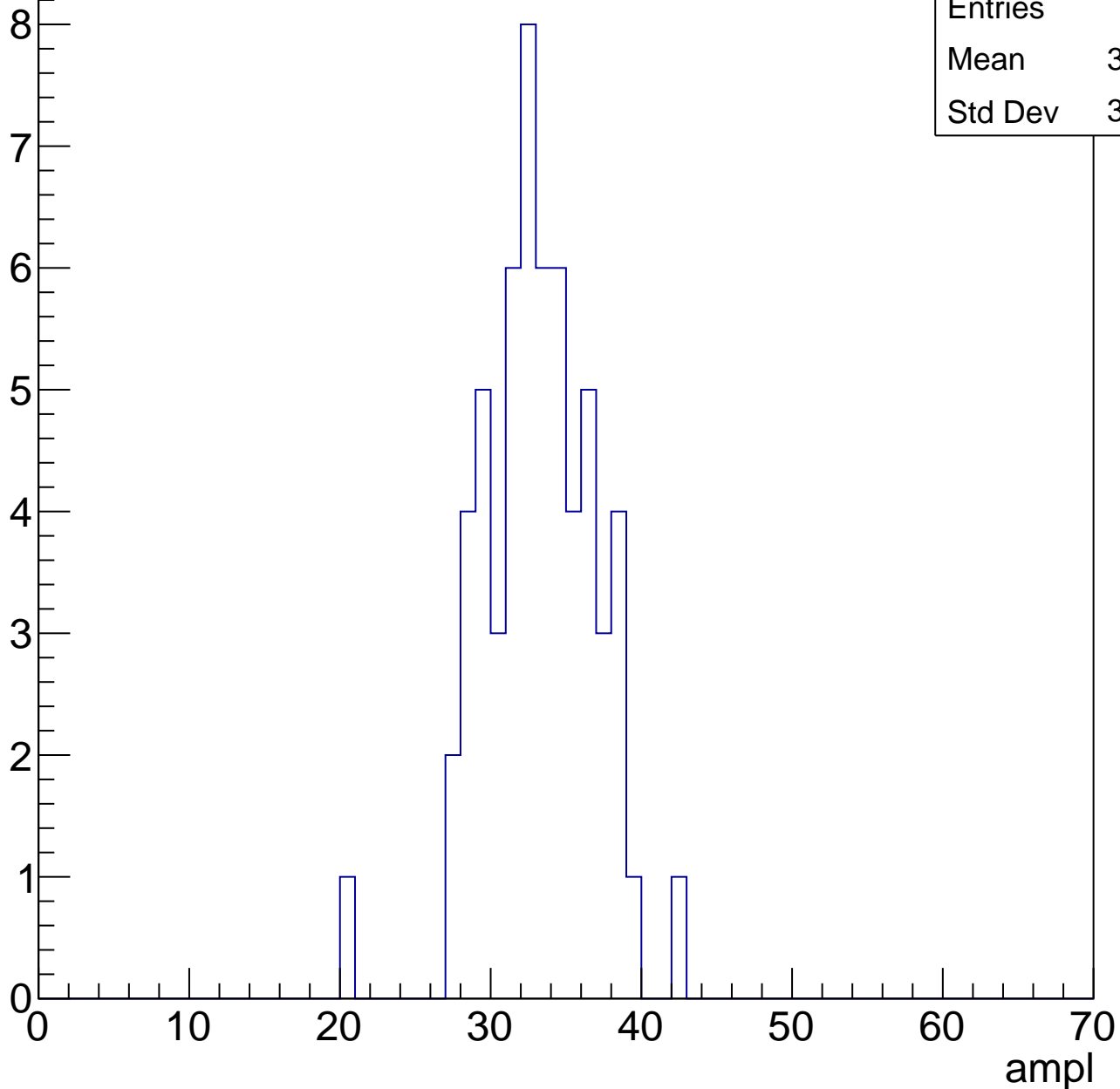


# B1L103S, U25-ch104, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	59
Mean	32.69
Std Dev	3.697

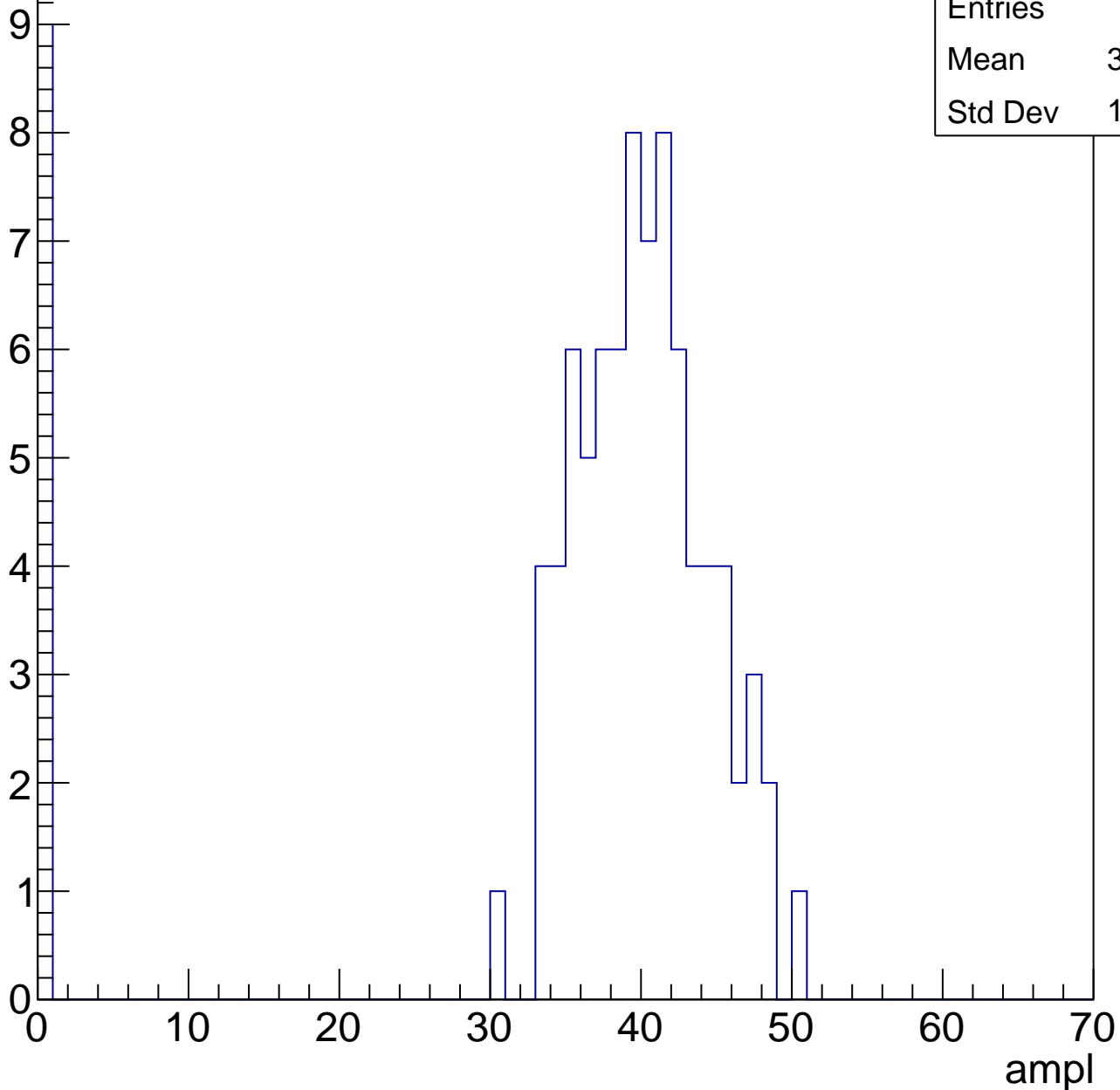


# B1L103S, U25-ch104, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	90
Mean	35.74
Std Dev	12.56

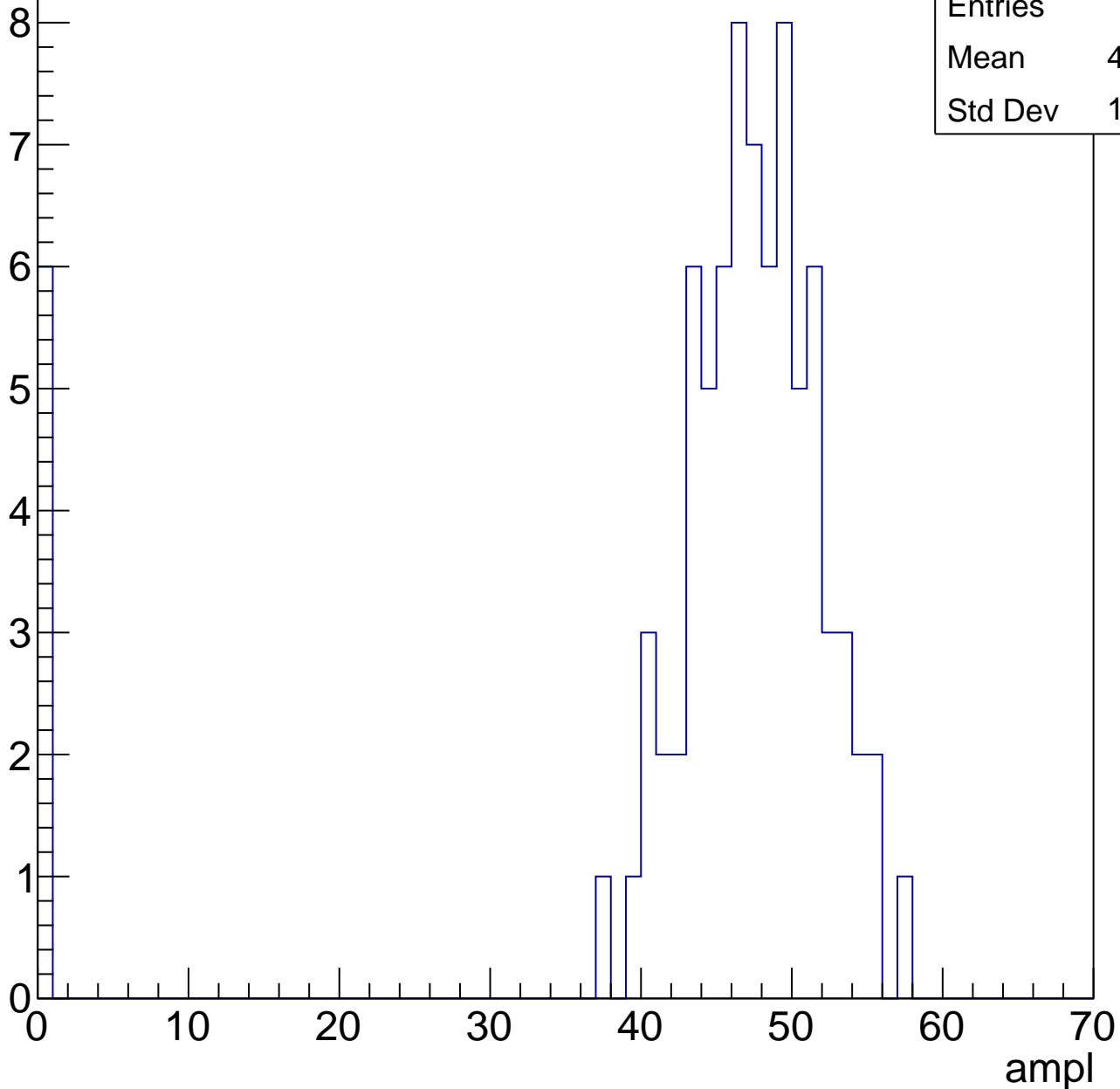


# B1L103S, U25-ch104, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	83
Mean	43.77
Std Dev	12.84

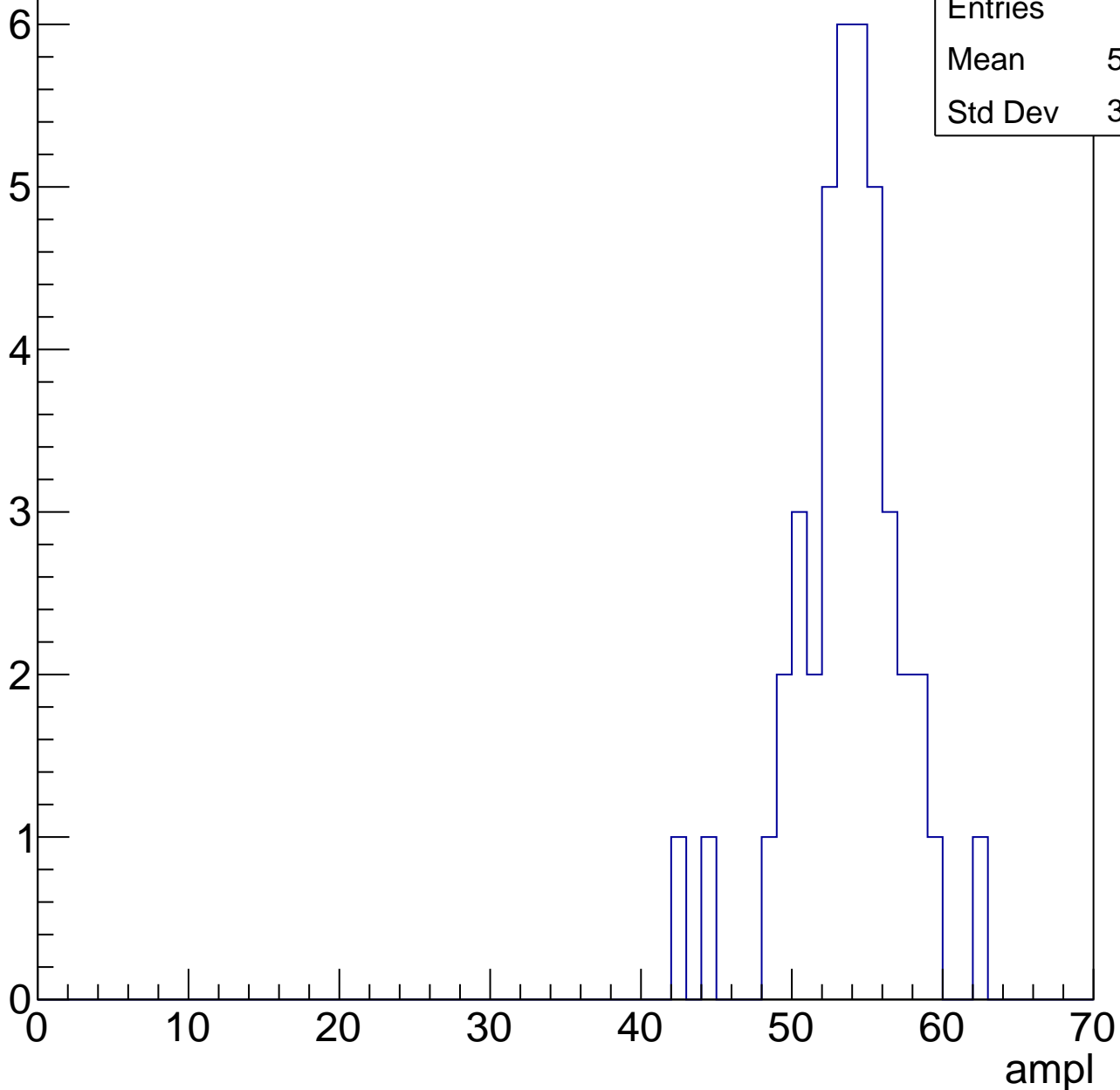


# B1L103S, U25-ch104, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

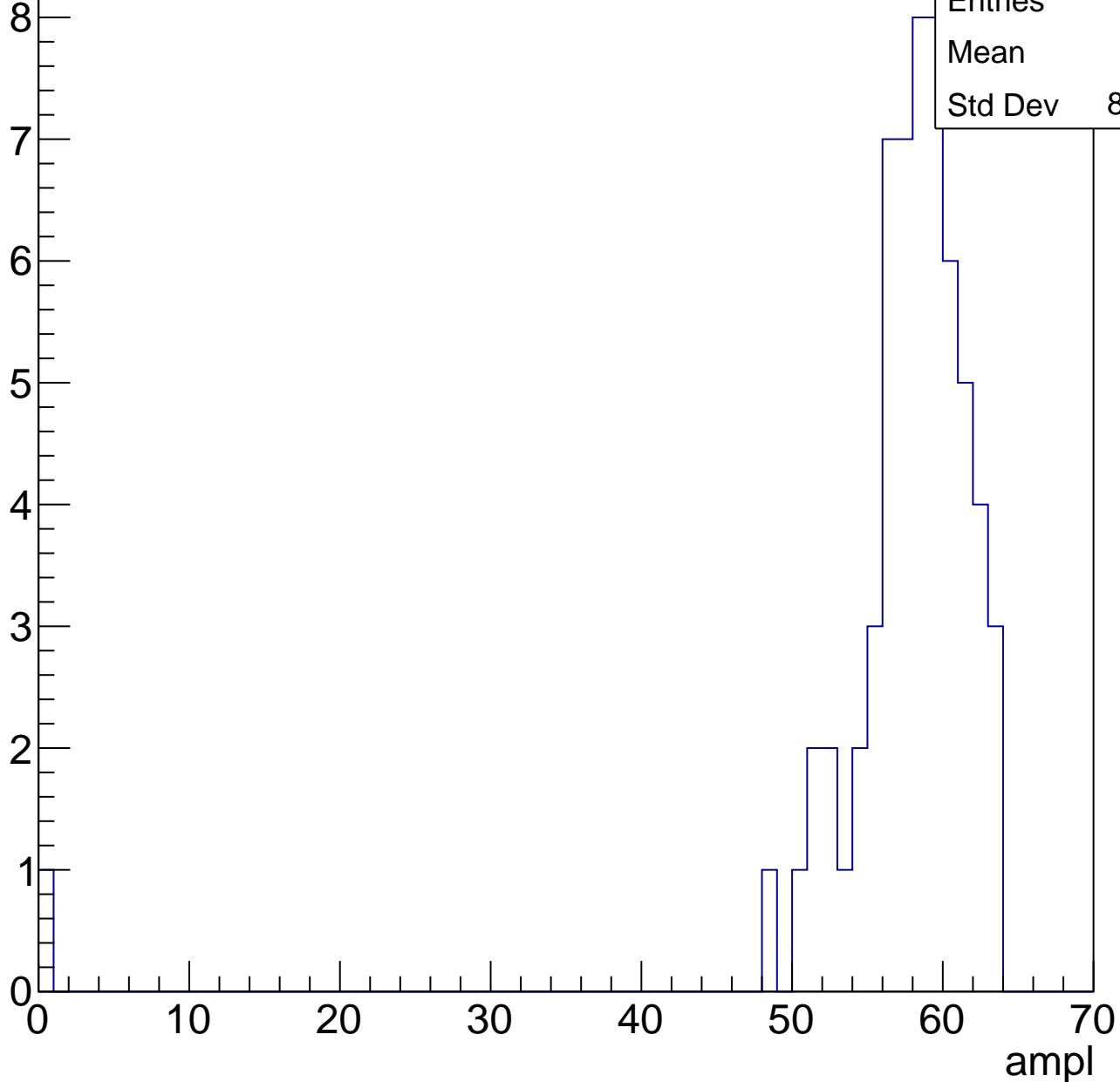
Entries	41
Mean	53.17
Std Dev	3.662



# B1L103S, U25-ch104, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

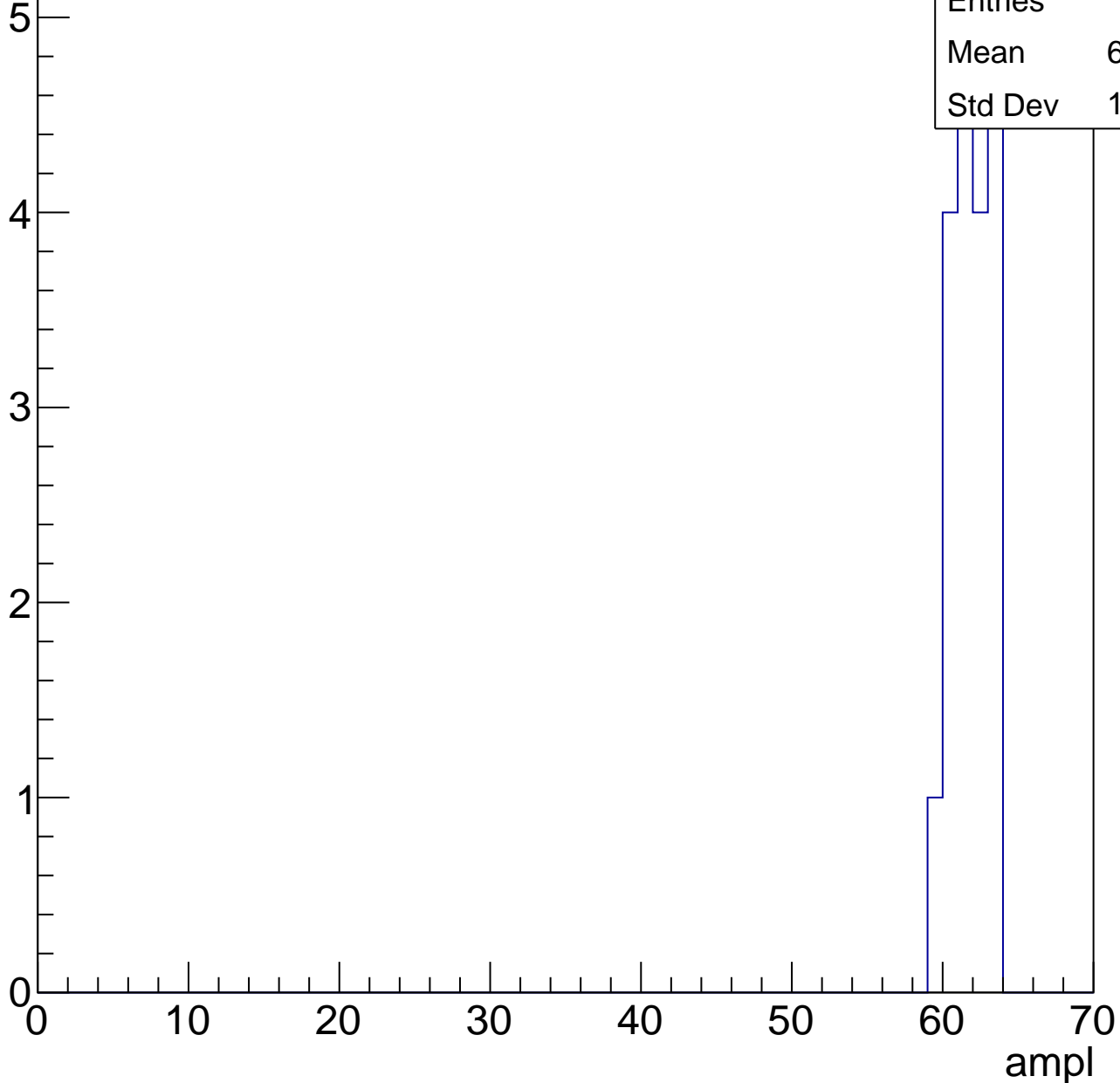


# B1L103S, U25-ch104, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	19
Mean	61.42
Std Dev	1.228





# B1L103S, U25-ch104, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	22
Mean	8.545
Std Dev	21.51

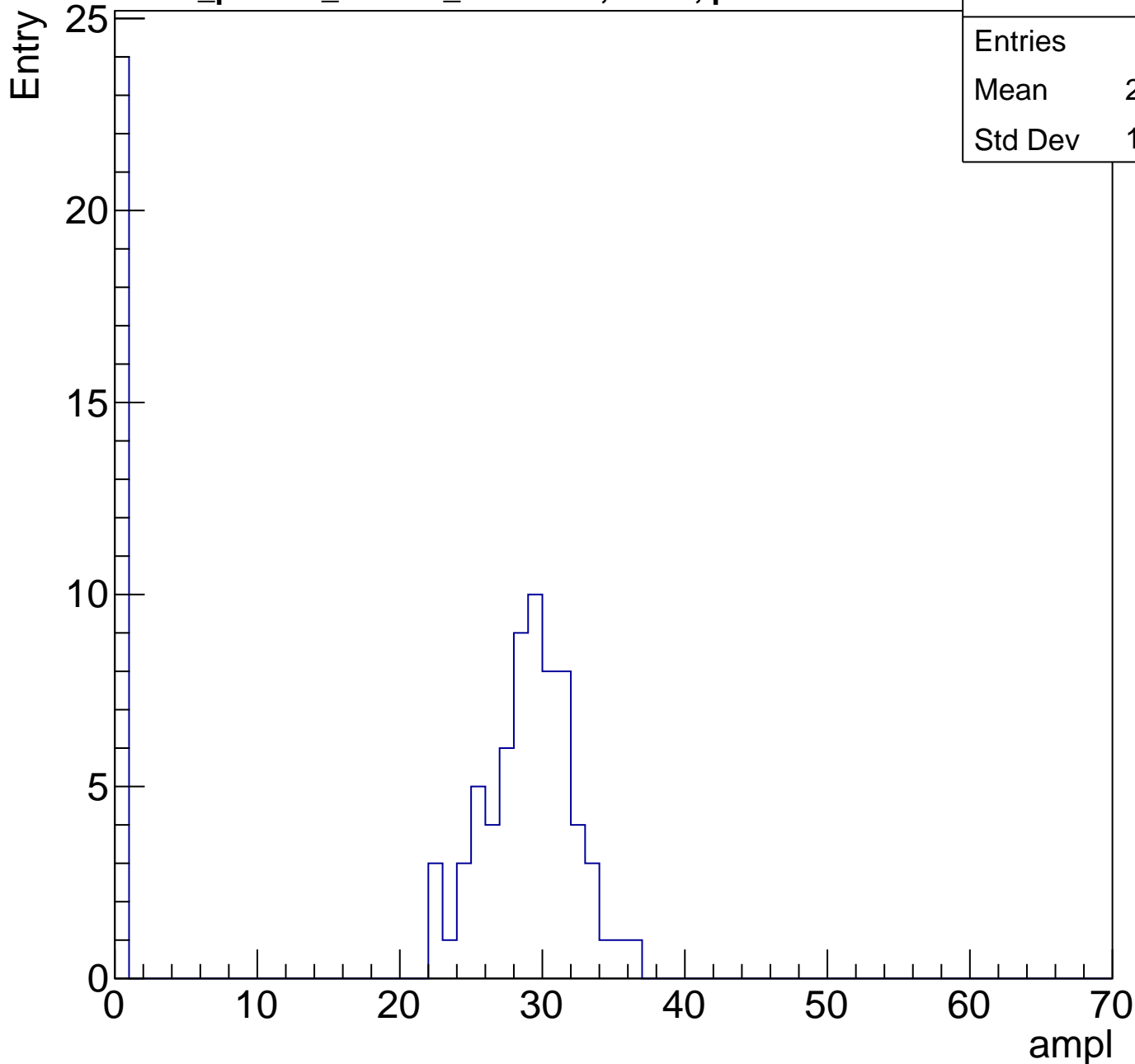
Entry



# B1L103S, U25-ch105, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	91
Mean	21.03
Std Dev	12.86



# B1L103S, U25-ch105, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	91
Mean	32.14
Std Dev	12.4

Entry

10

8

6

4

2

0

ampl

0

10

20

30

40

50

60

70

1

2

1

6

6

9

8

9

7

2

3

3

0

3

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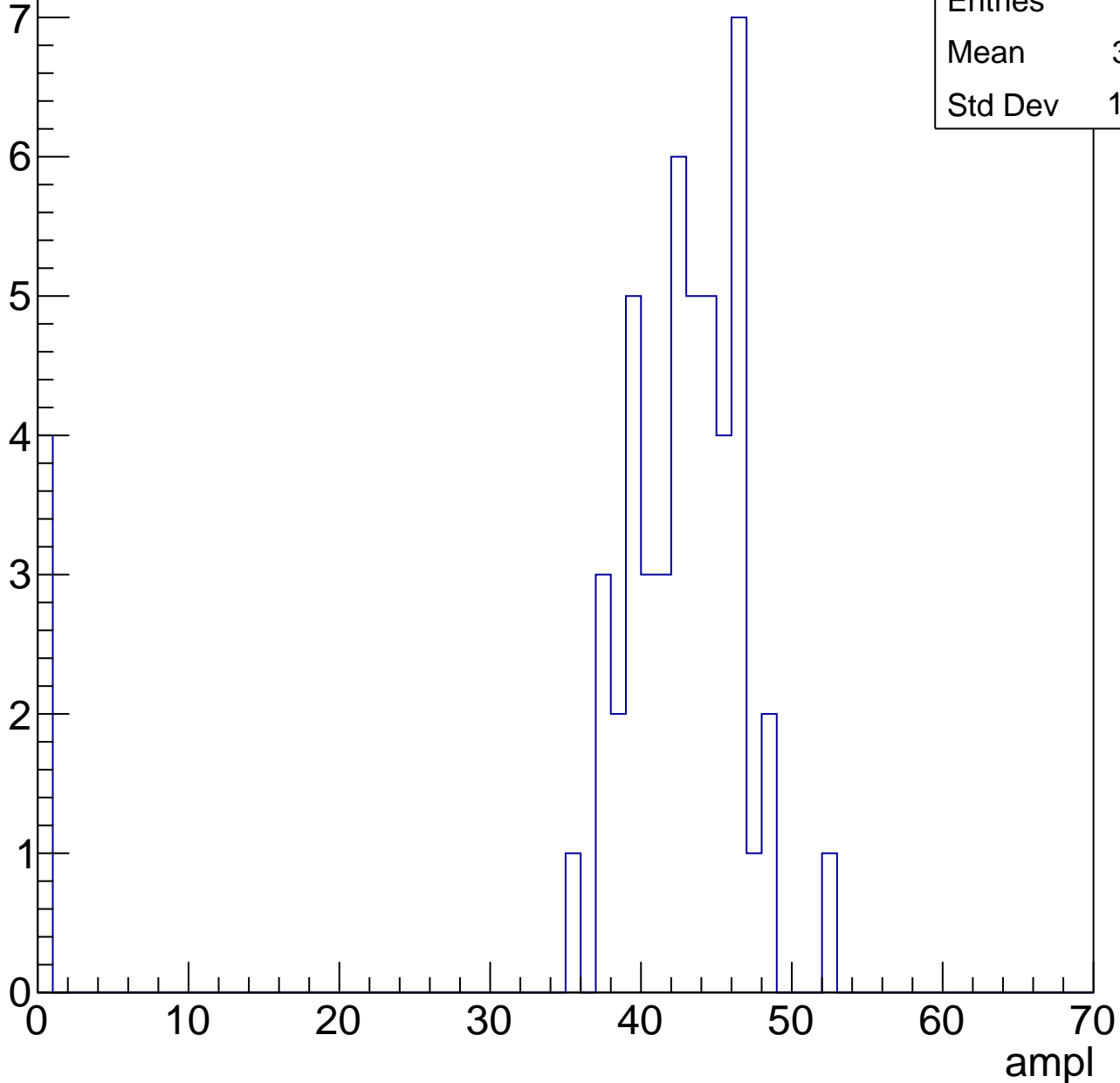
0

# B1L103S, U25-ch105, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	52
Mean	39.31
Std Dev	11.82

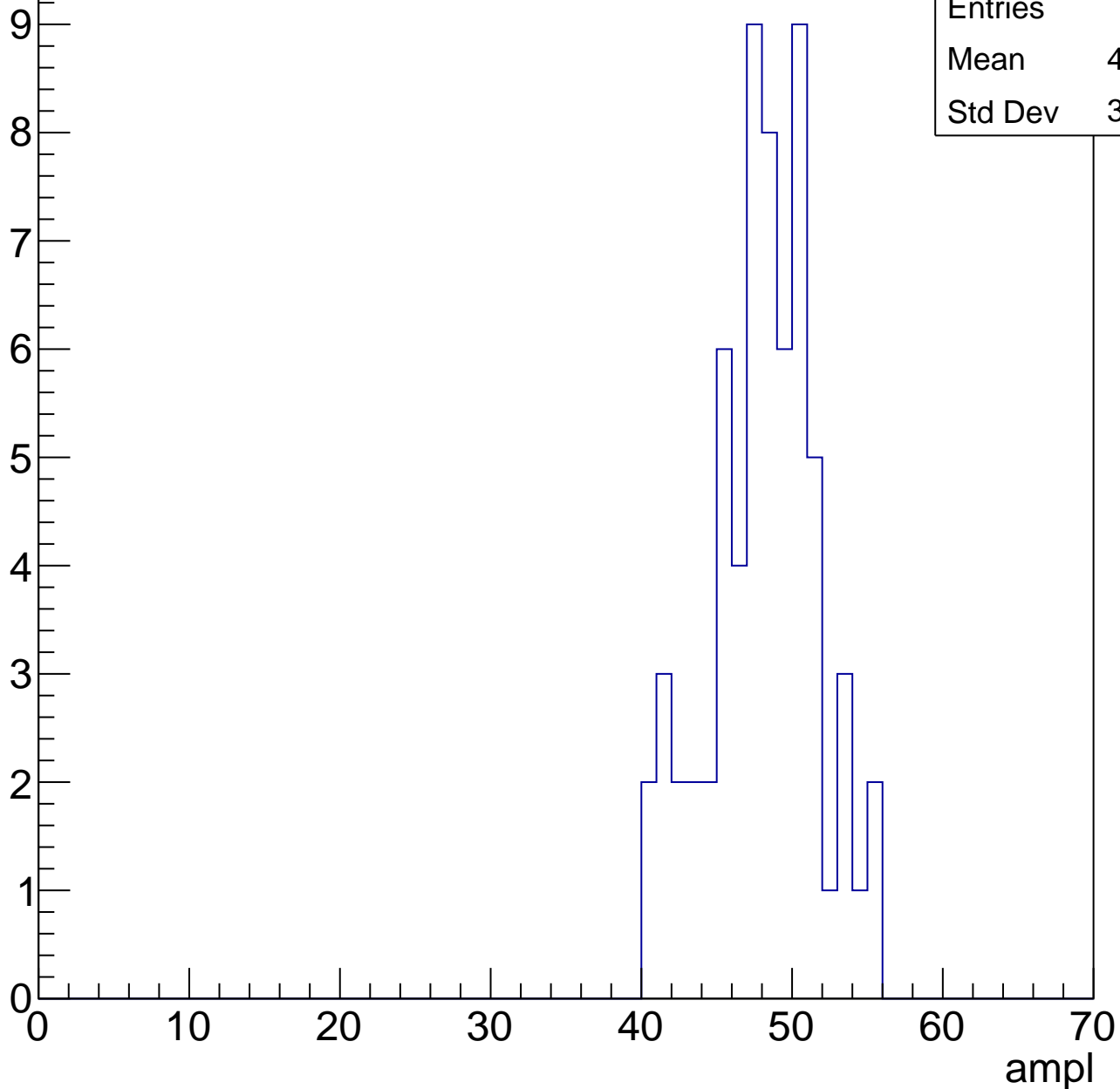


# B1L103S, U25-ch105, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	65
Mean	47.63
Std Dev	3.533

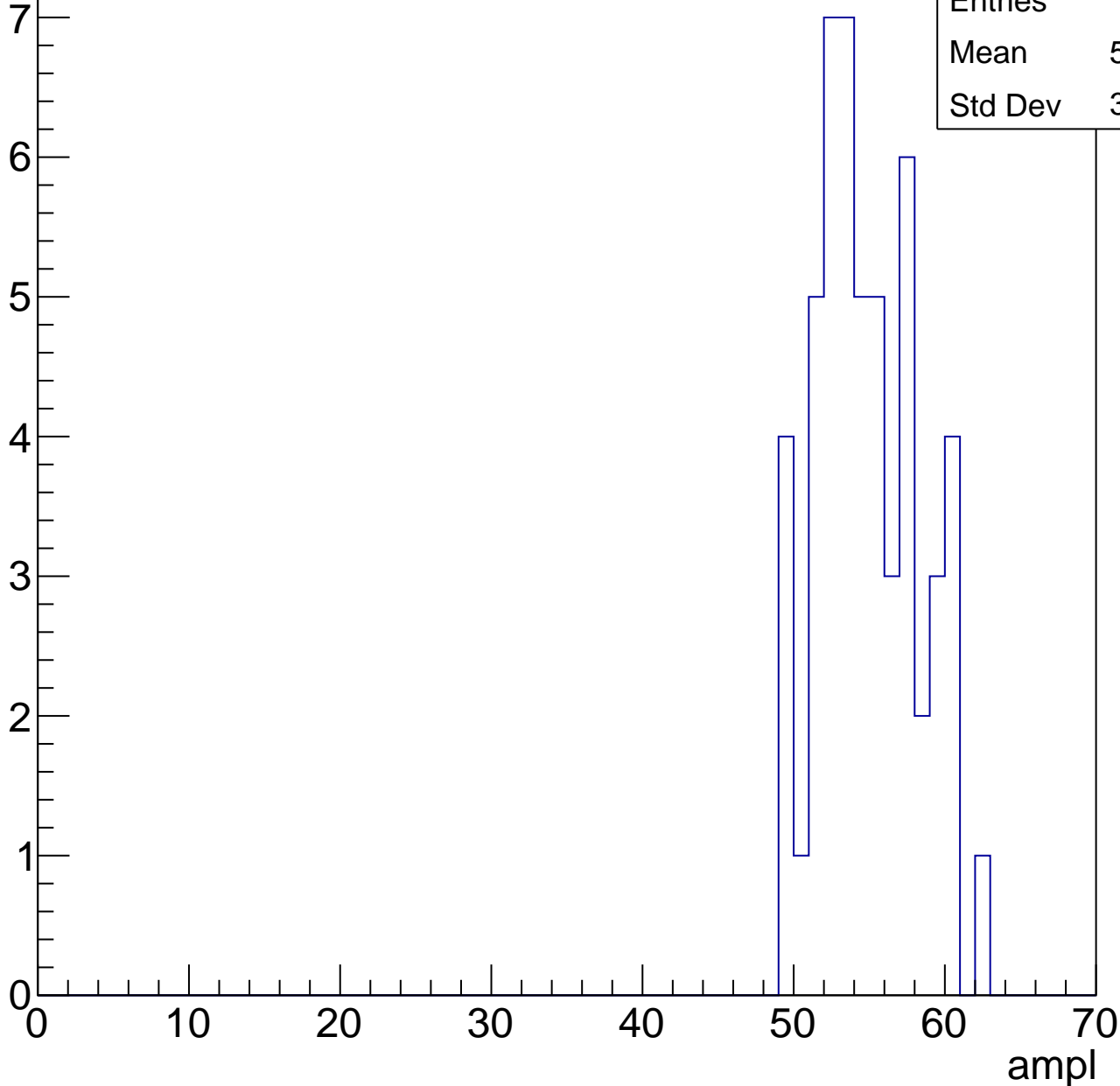


# B1L103S, U25-ch105, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	53
Mean	54.45
Std Dev	3.283



# B1L103S, U25-ch105, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	68
Mean	58.26
Std Dev	7.654

Entry

10

8

6

4

2

0

0

10

20

30

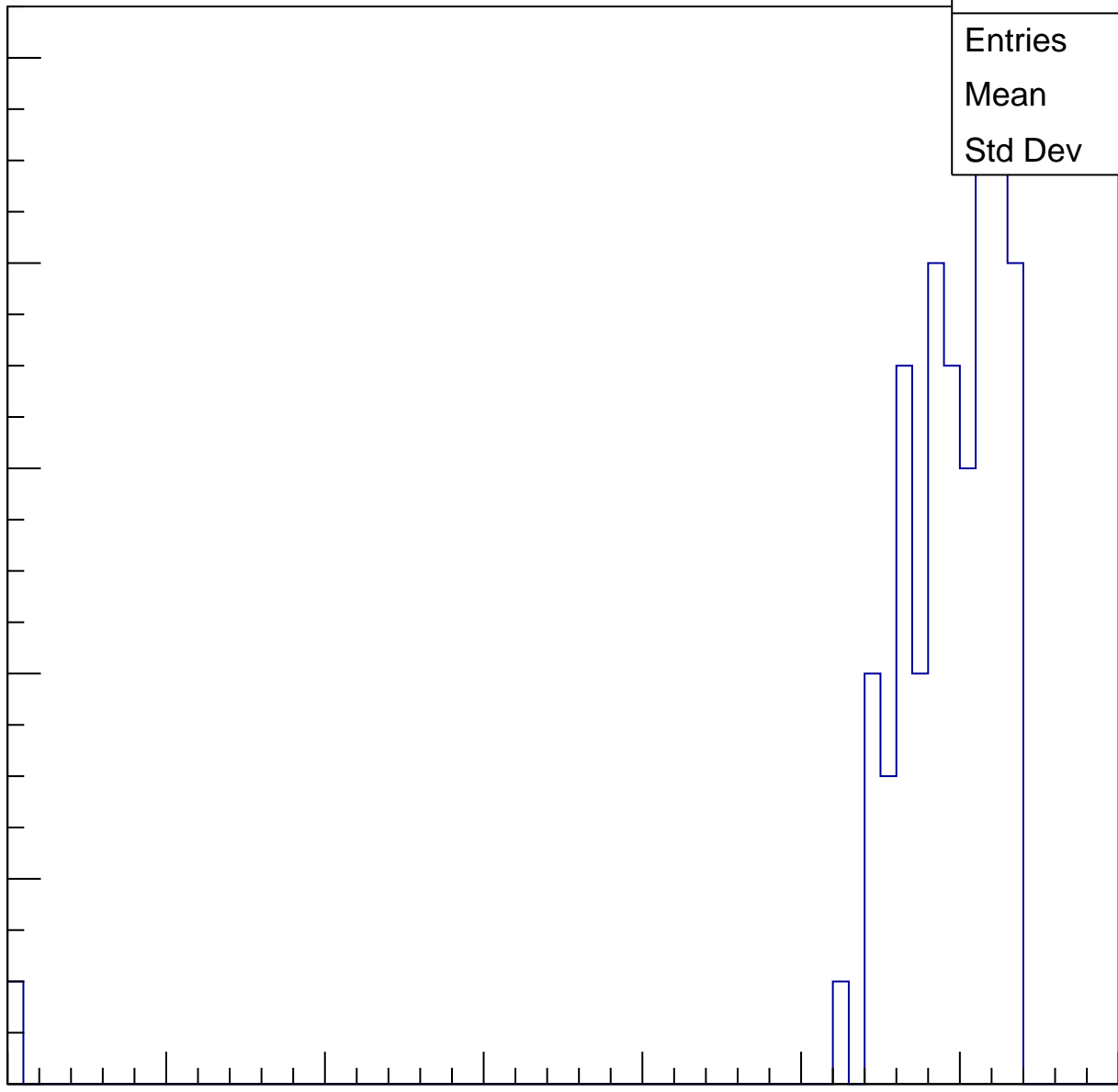
40

50

60

70

ampl



# B1L103S, U25-ch105, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	63
Std Dev	0

ampl



# B1L103S, U25-ch105, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

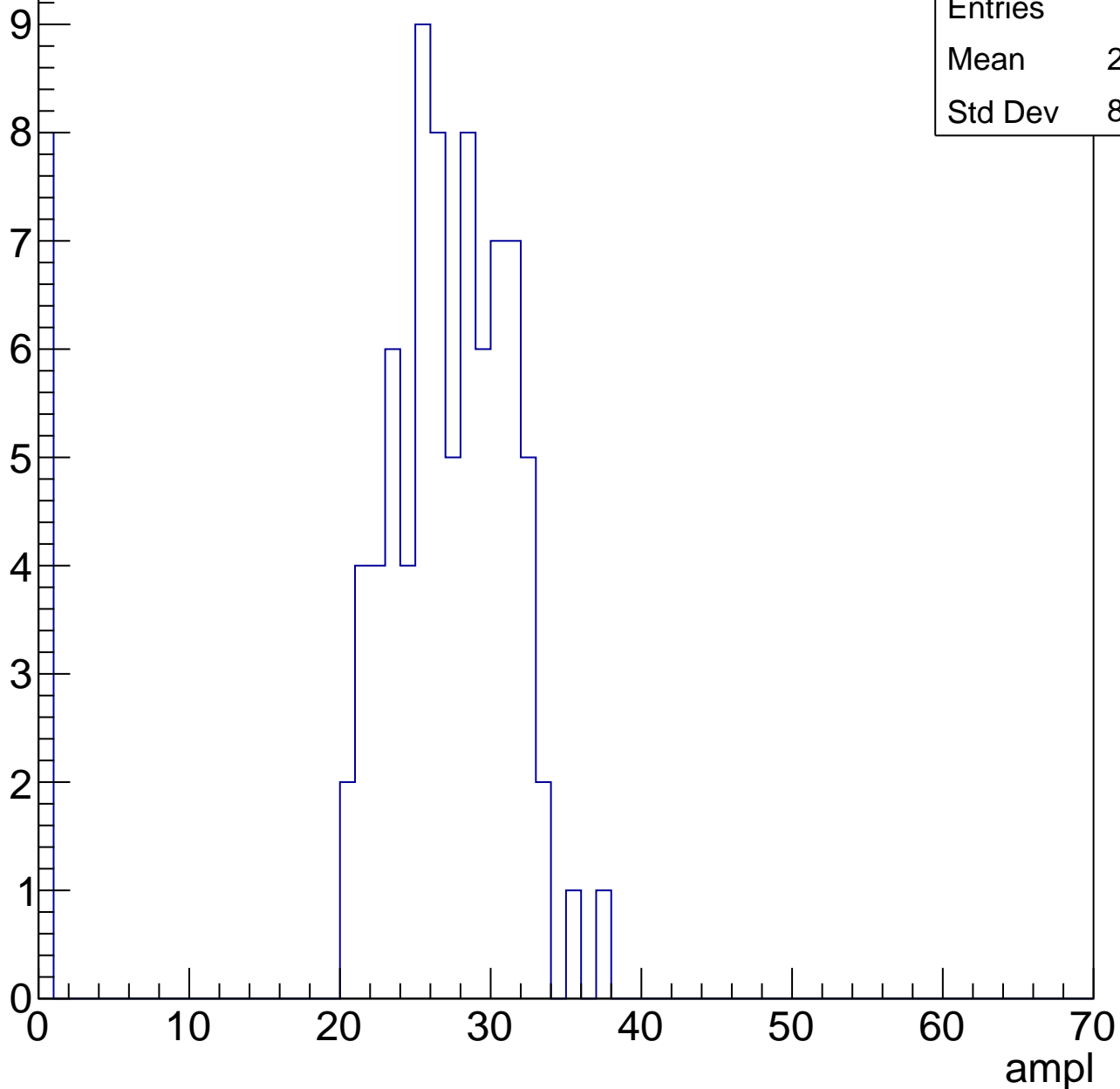
Entries	19
Mean	0
Std Dev	0

# B1L103S, U25-ch106, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	87
Mean	24.56
Std Dev	8.578

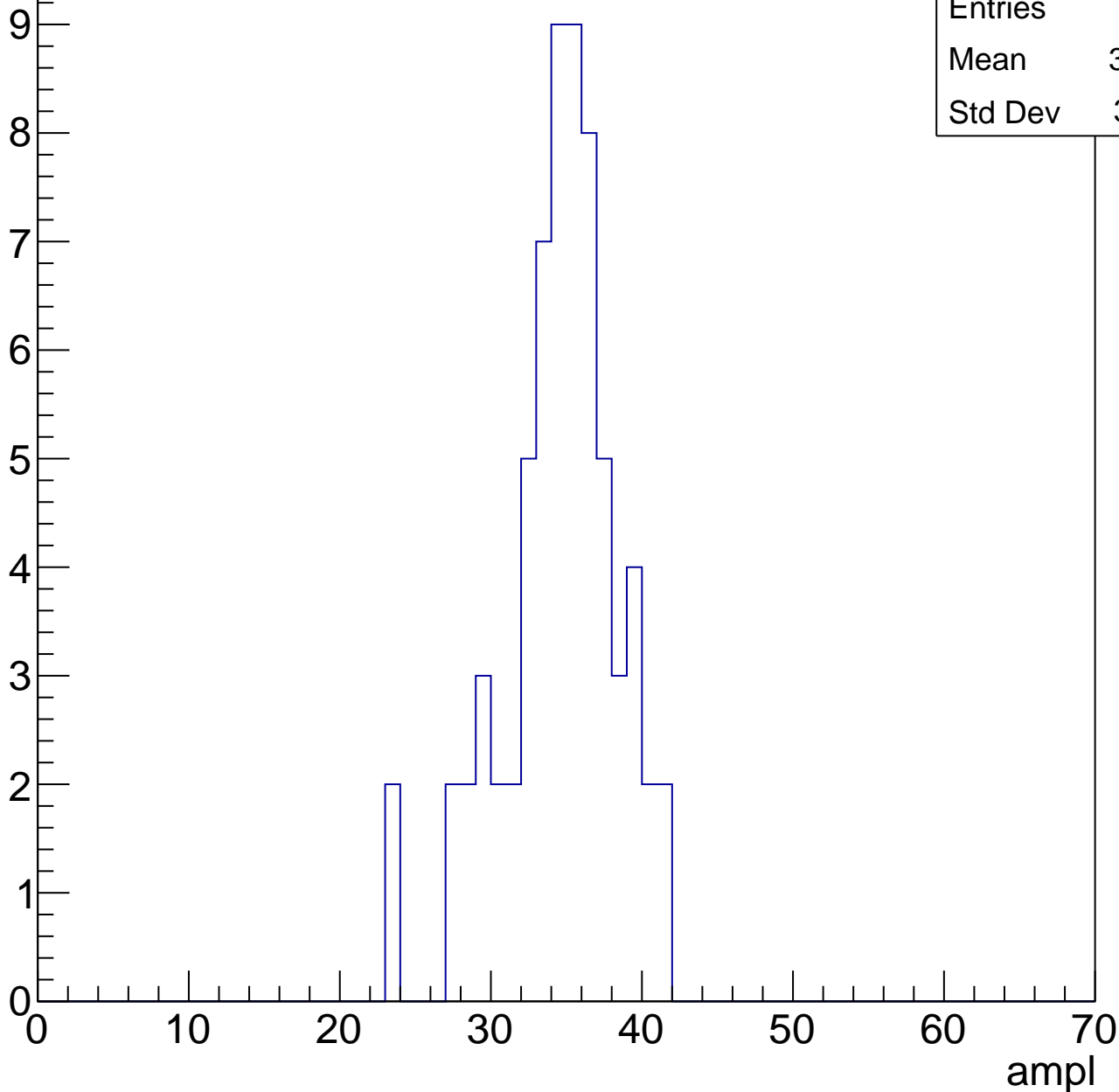


# B1L103S, U25-ch106, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	67
Mean	34.06
Std Dev	3.801

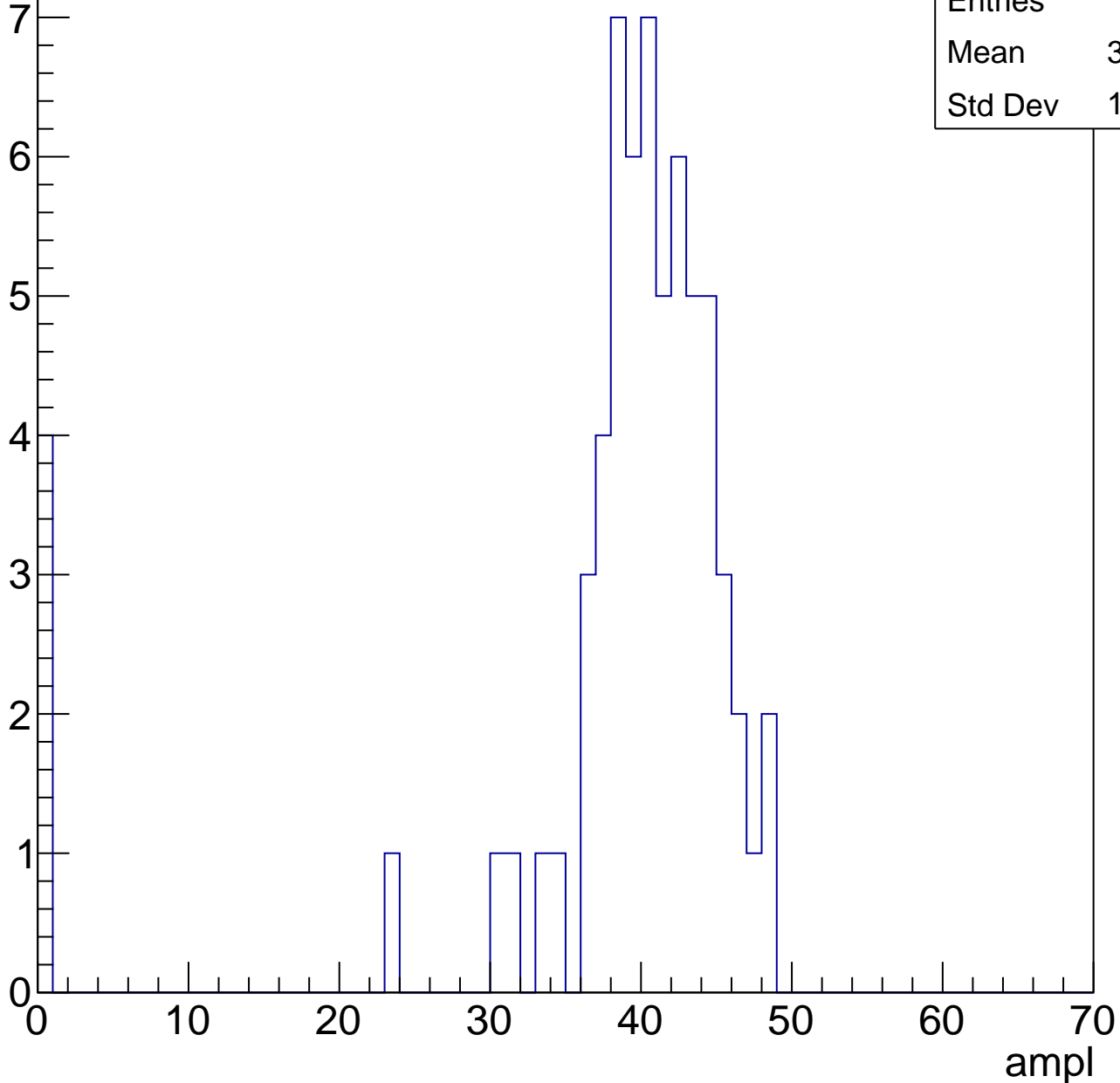


# B1L103S, U25-ch106, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	65
Mean	37.68
Std Dev	10.52



# B1L103S, U25-ch106, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

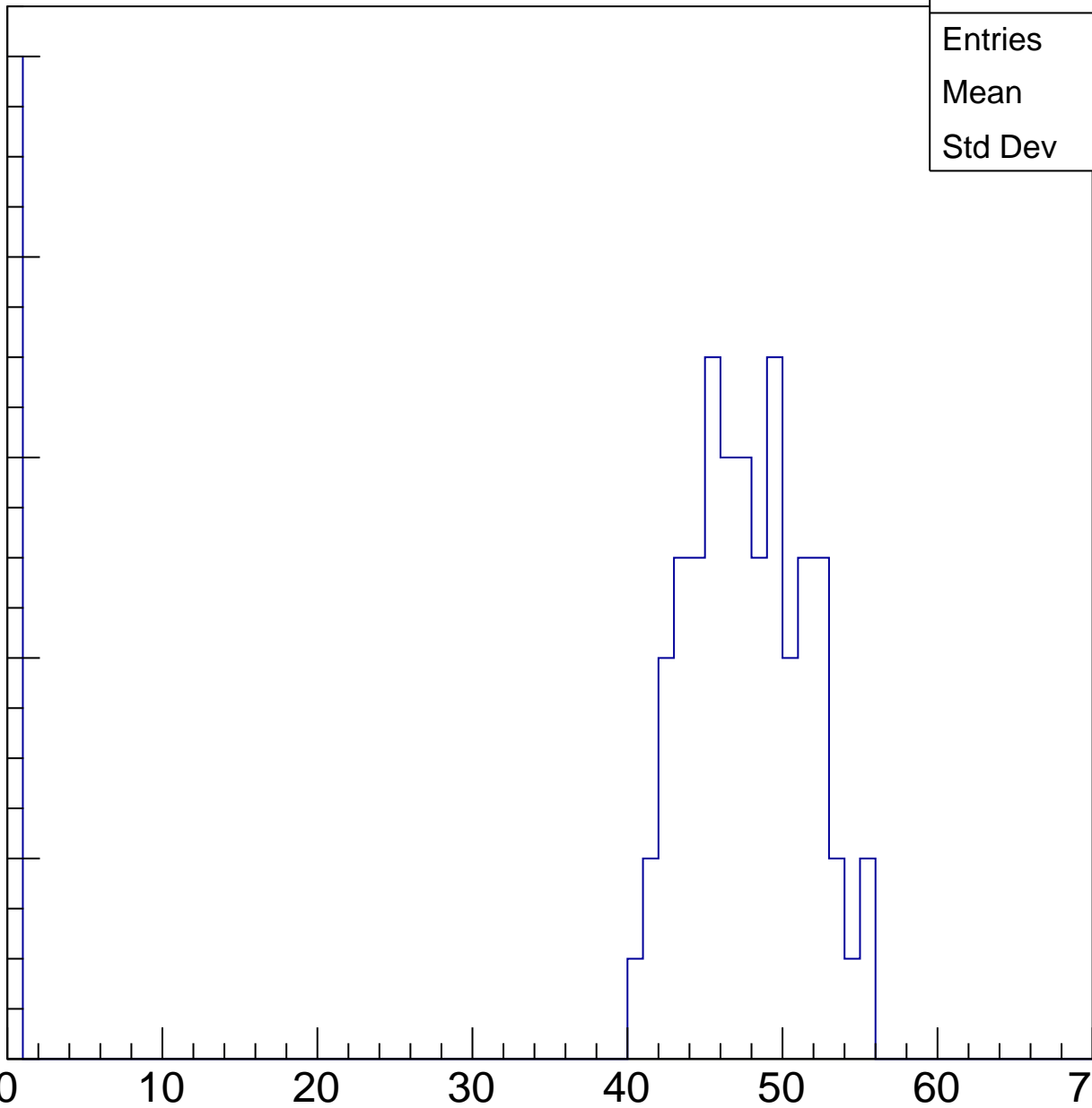
Entries	77
Mean	41.12
Std Dev	16.25

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

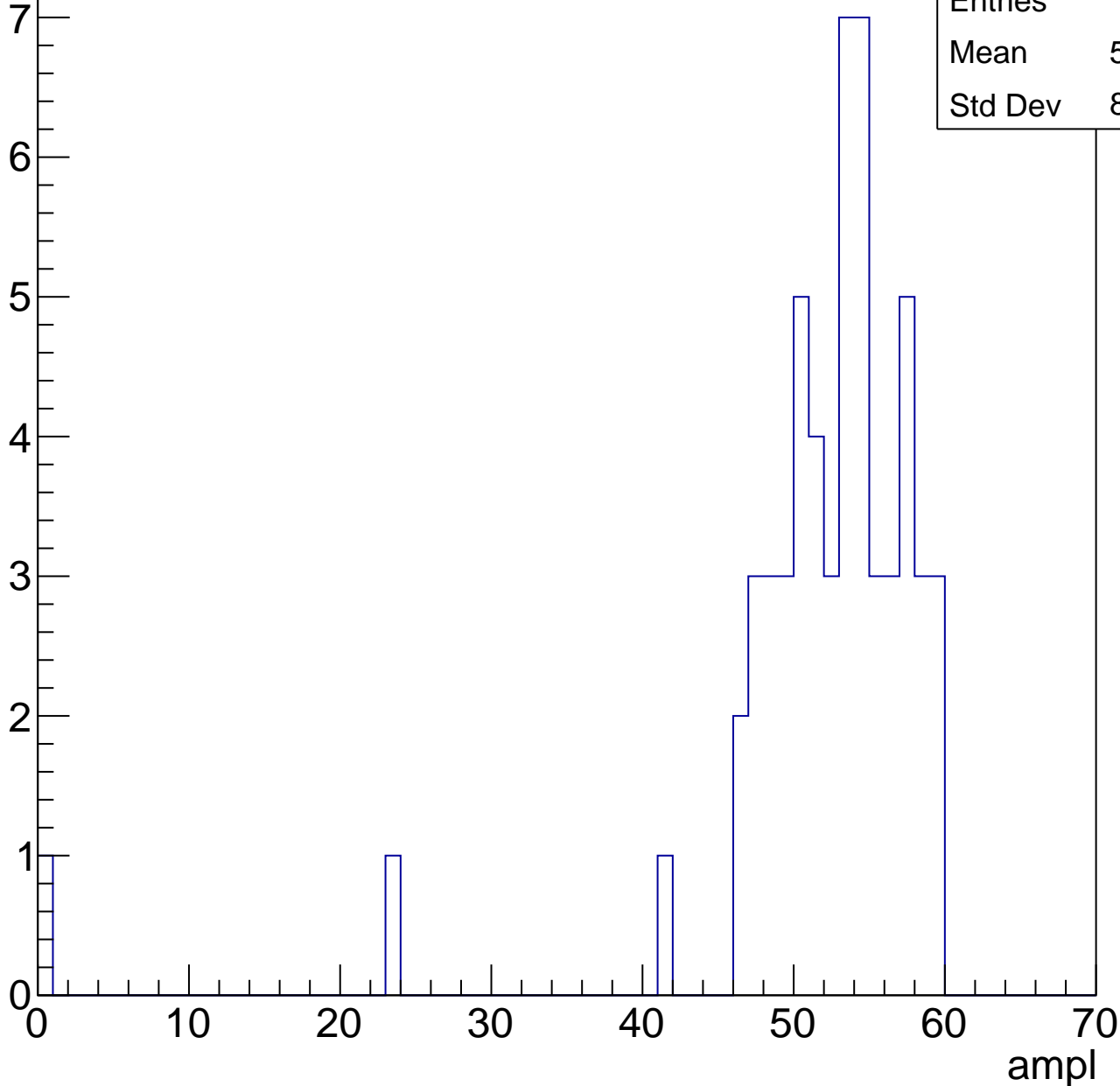


# B1L103S, U25-ch106, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	57
Mean	51.16
Std Dev	8.748

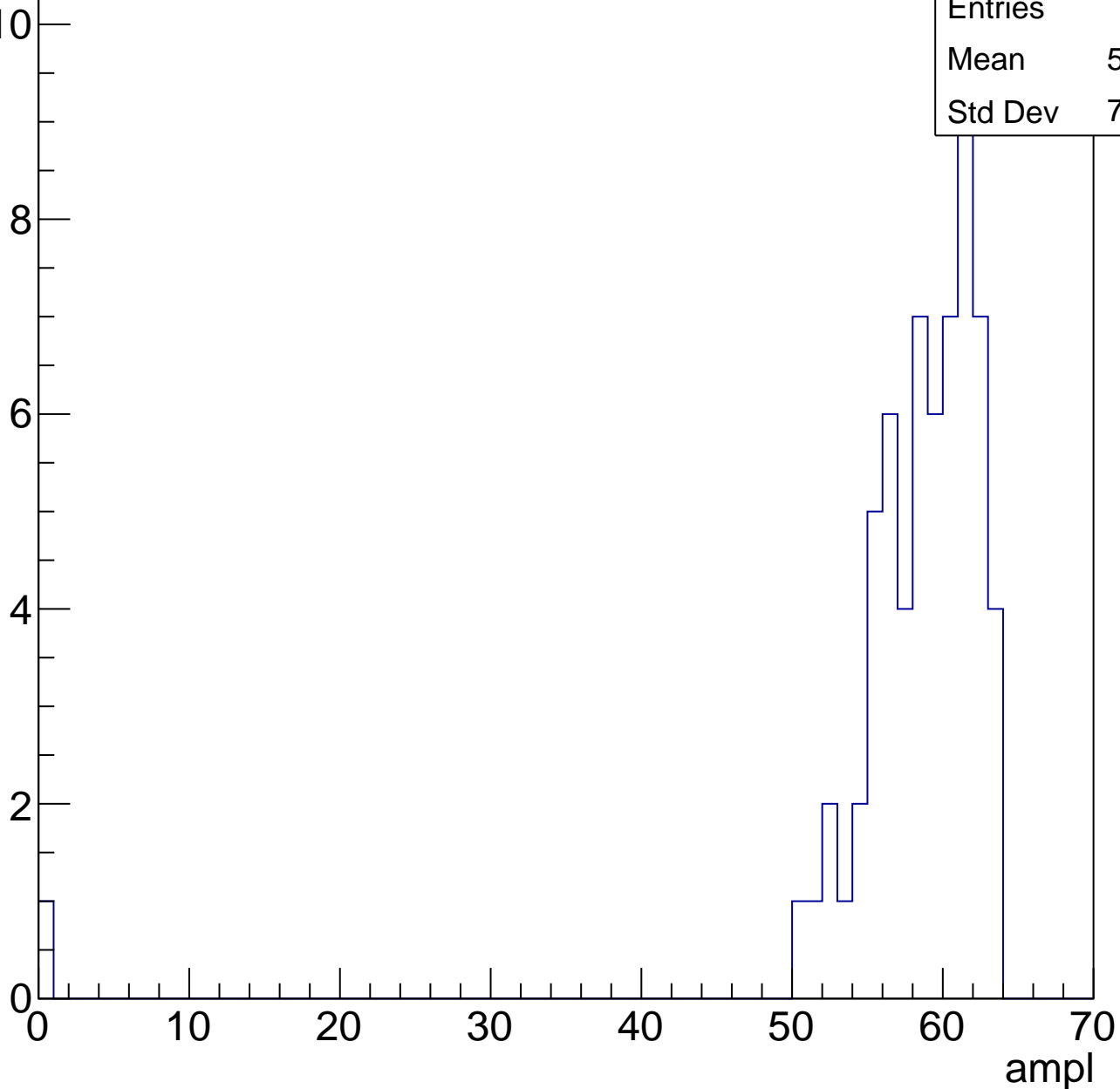


# B1L103S, U25-ch106, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	64
Mean	57.52
Std Dev	7.906

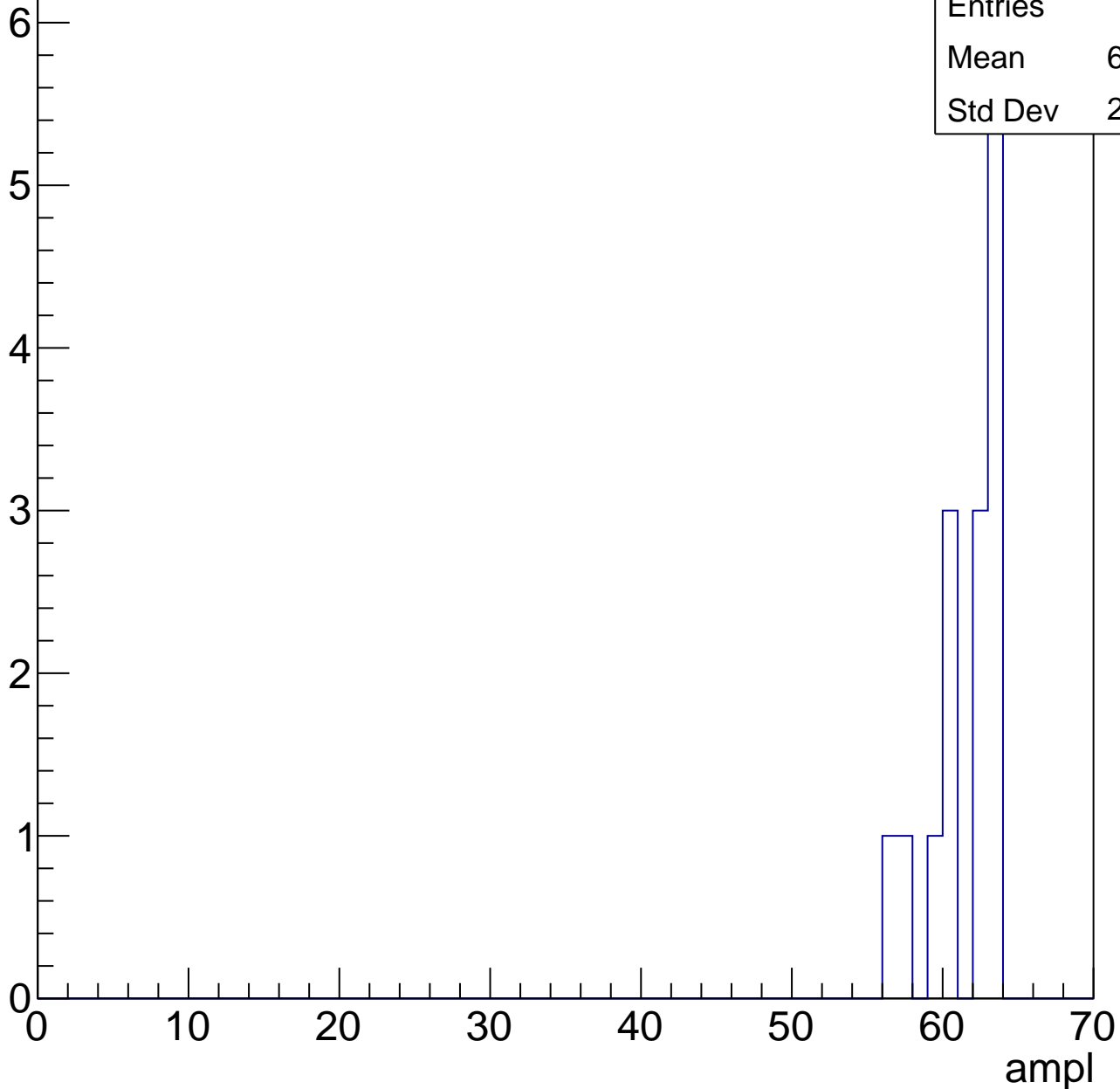


# B1L103S, U25-ch106, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	15
Mean	61.07
Std Dev	2.235



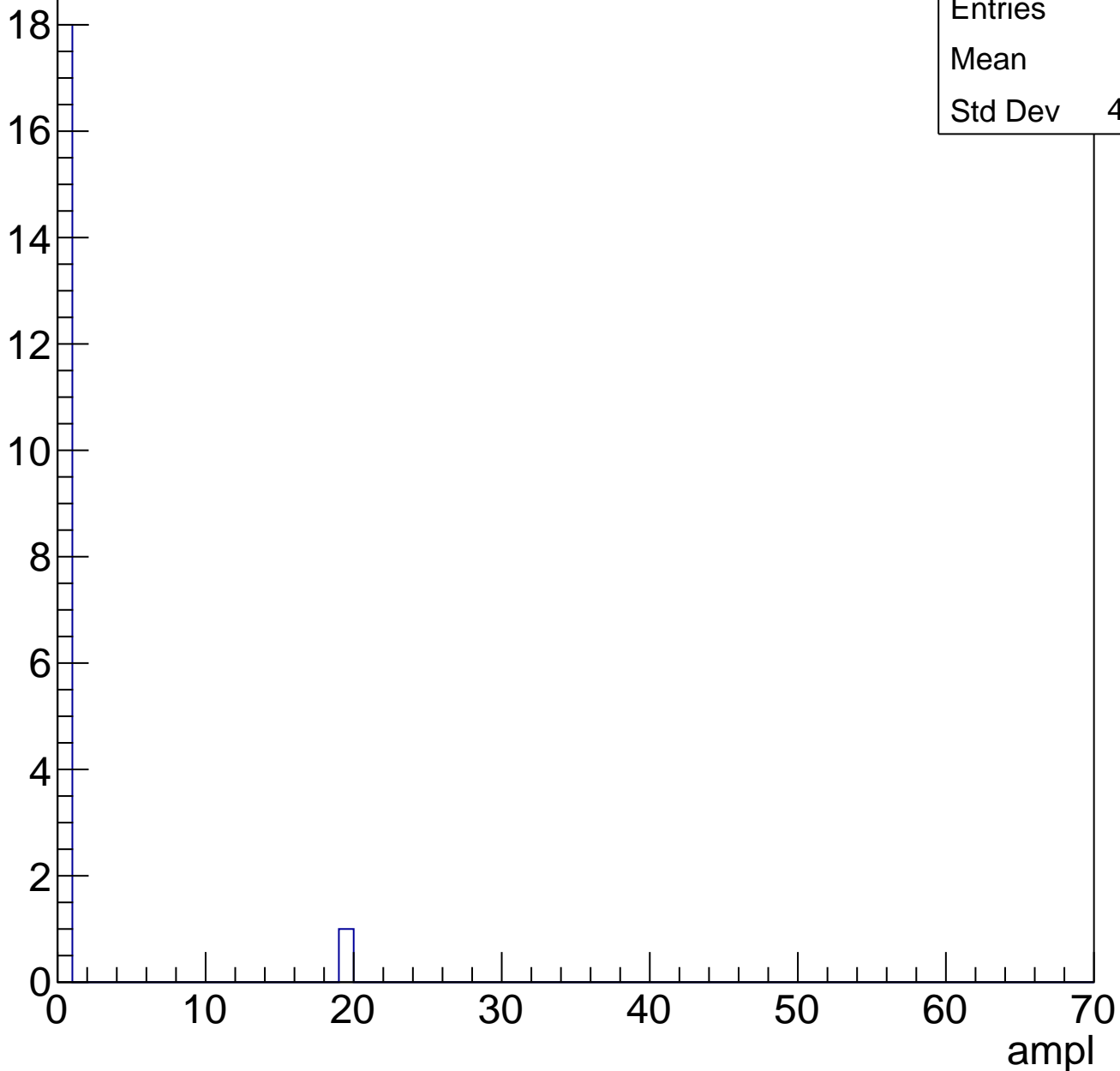


# B1L103S, U25-ch106, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	19
Mean	1
Std Dev	4.243

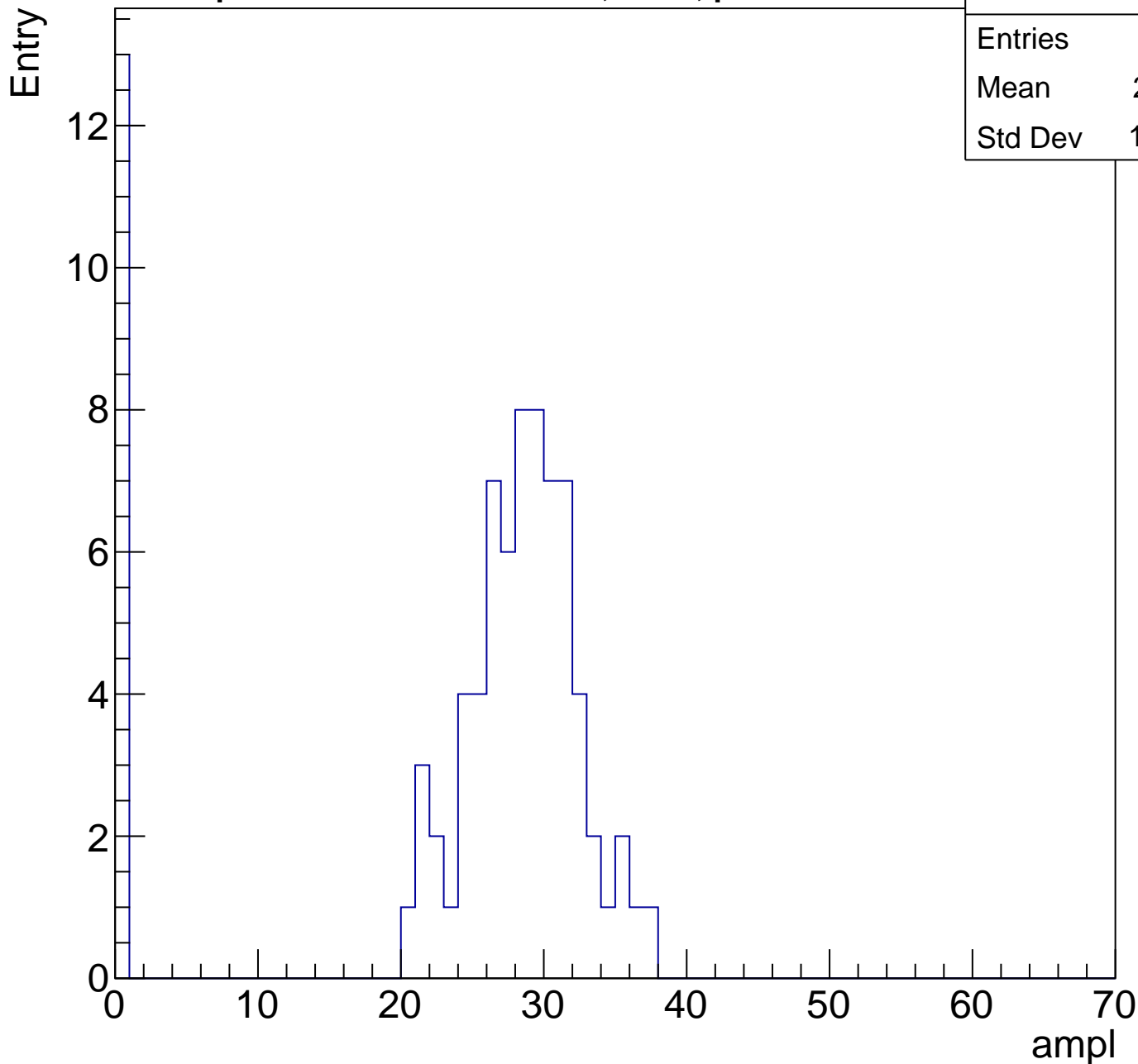
Entry



# B1L103S, U25-ch107, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	82
Mean	23.71
Std Dev	10.83

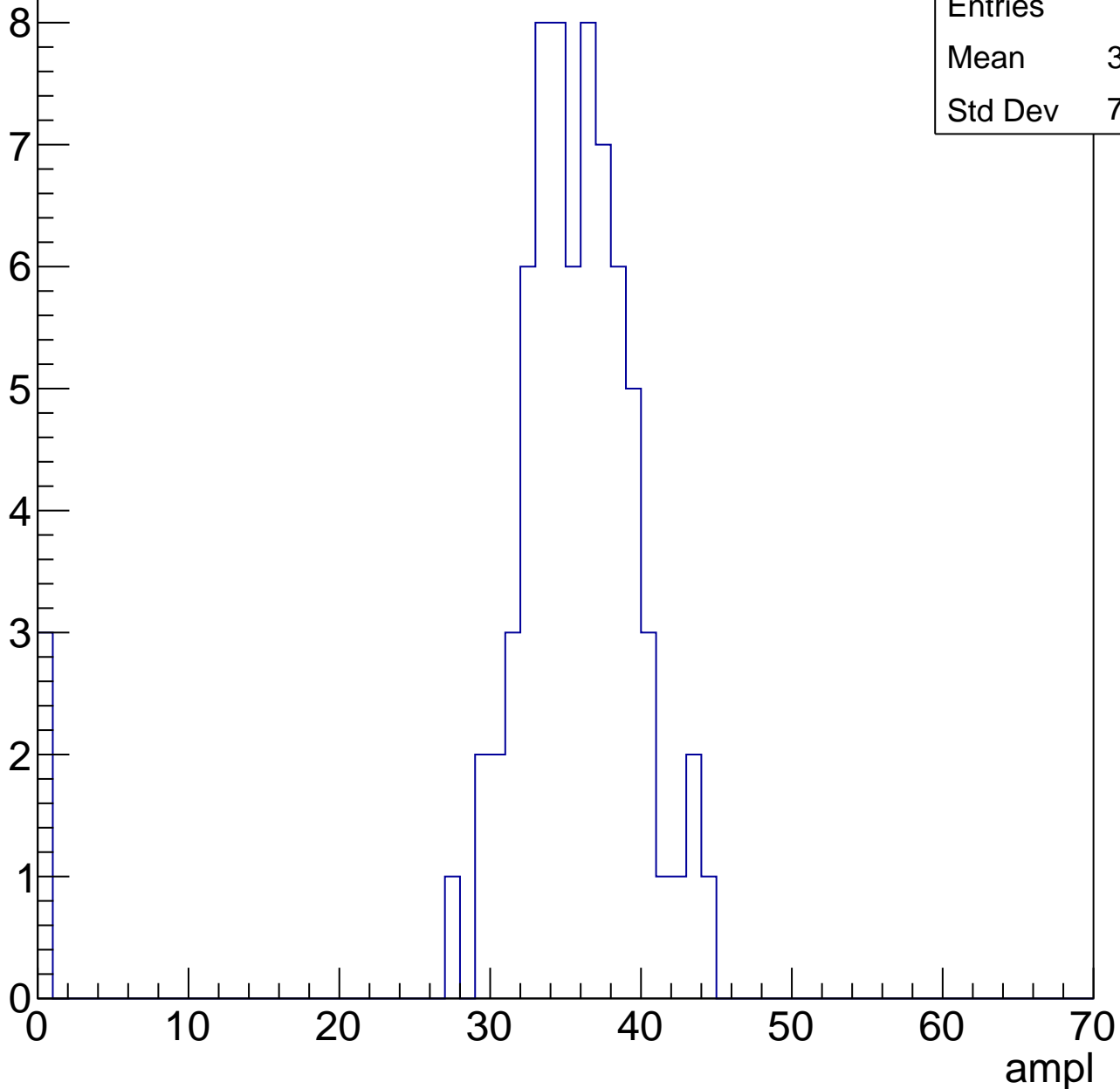


# B1L103S, U25-ch107, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	73
Mean	33.96
Std Dev	7.819

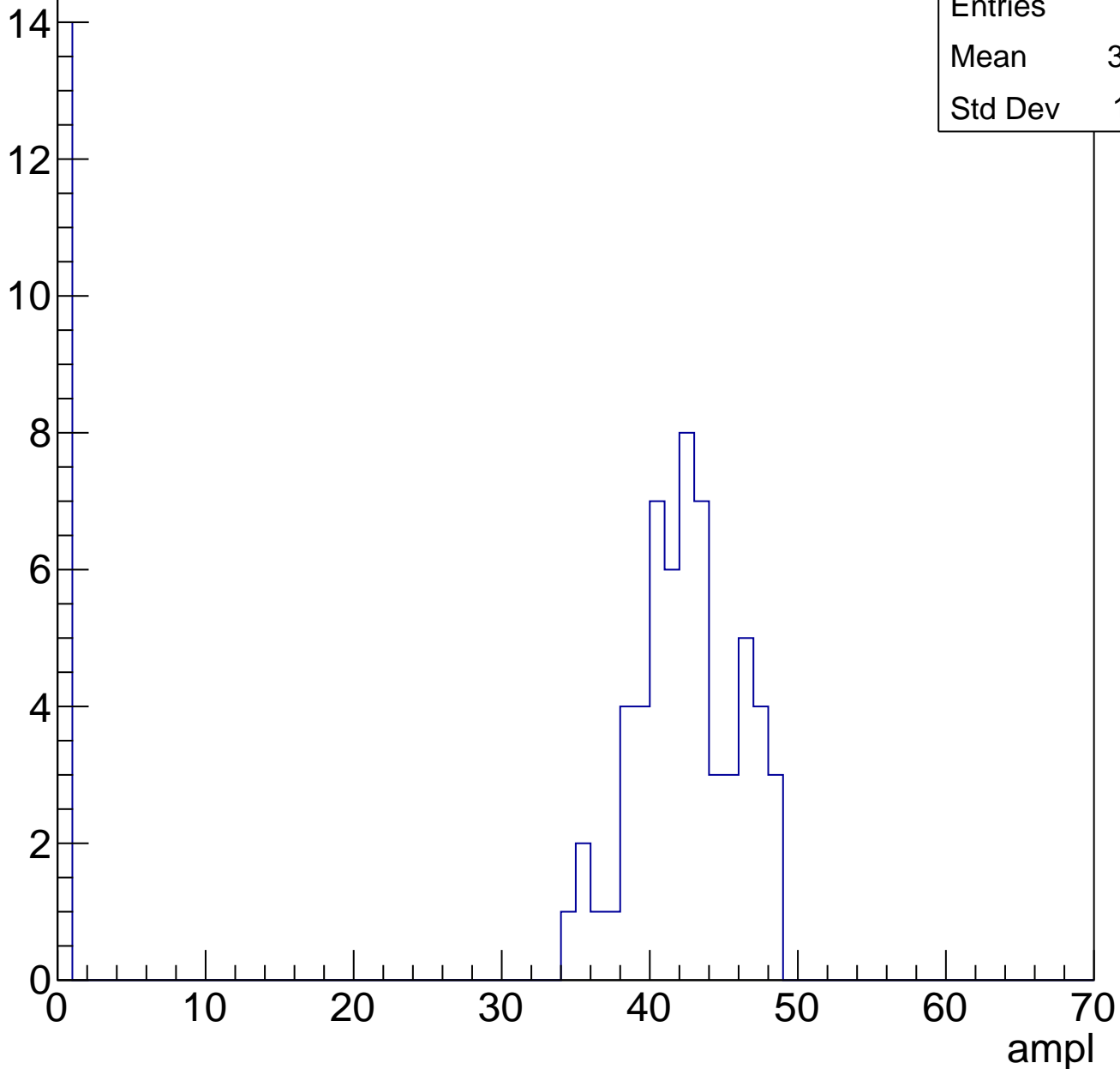


# B1L103S, U25-ch107, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	73
Mean	33.93
Std Dev	16.81

Entry

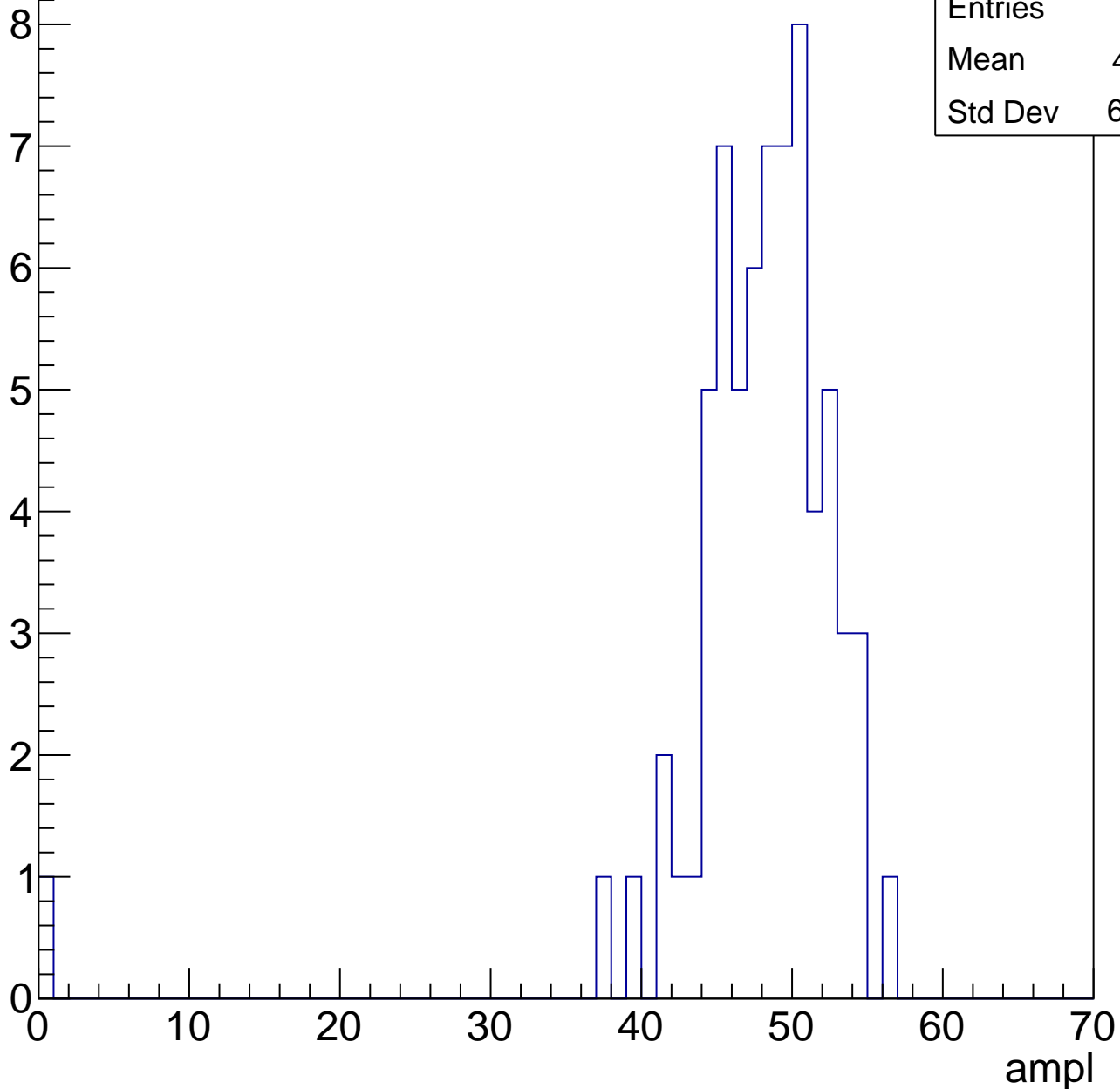


# B1L103S, U25-ch107, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	68
Mean	47.21
Std Dev	6.853

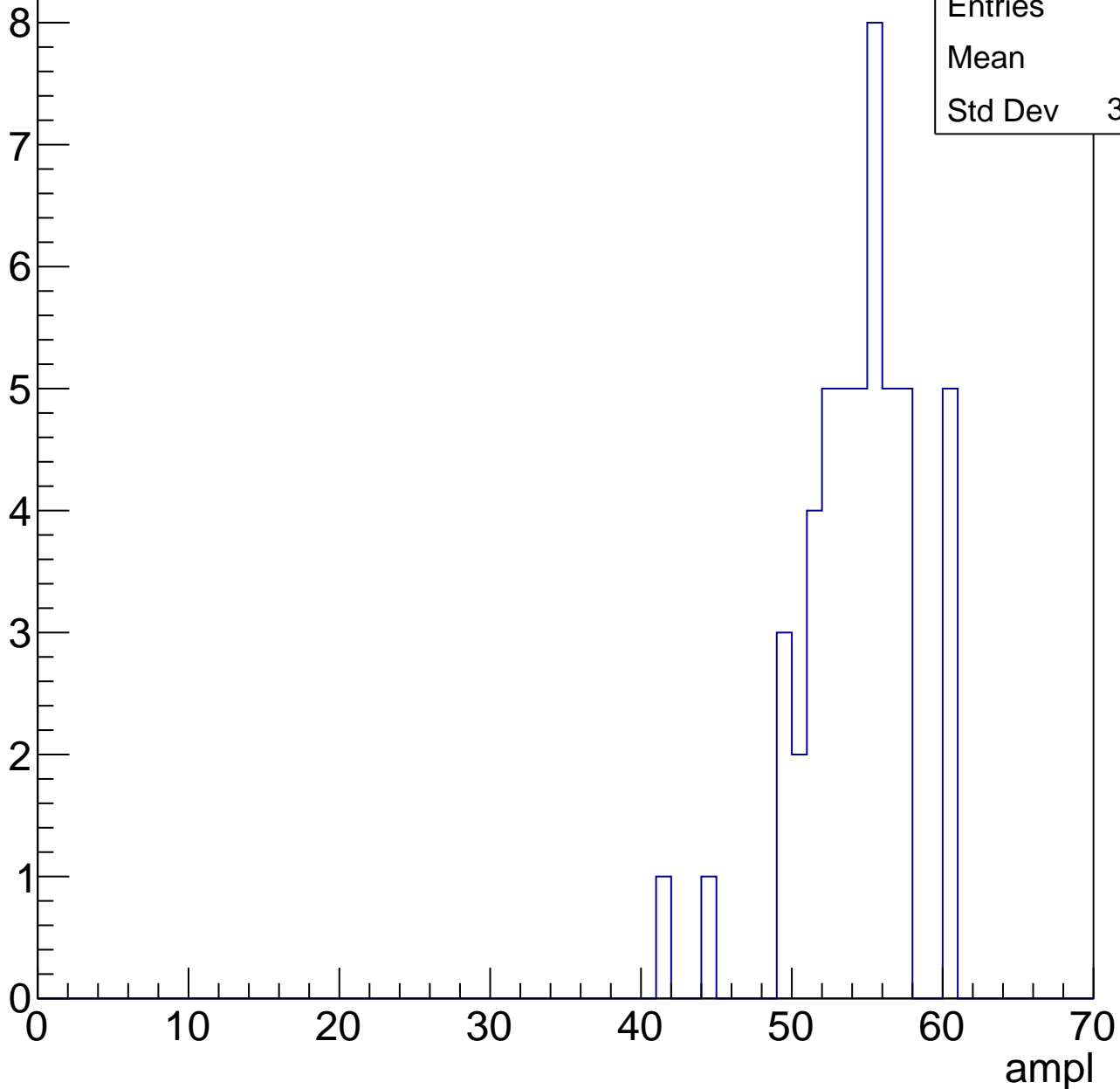


# B1L103S, U25-ch107, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	49
Mean	53.8
Std Dev	3.747

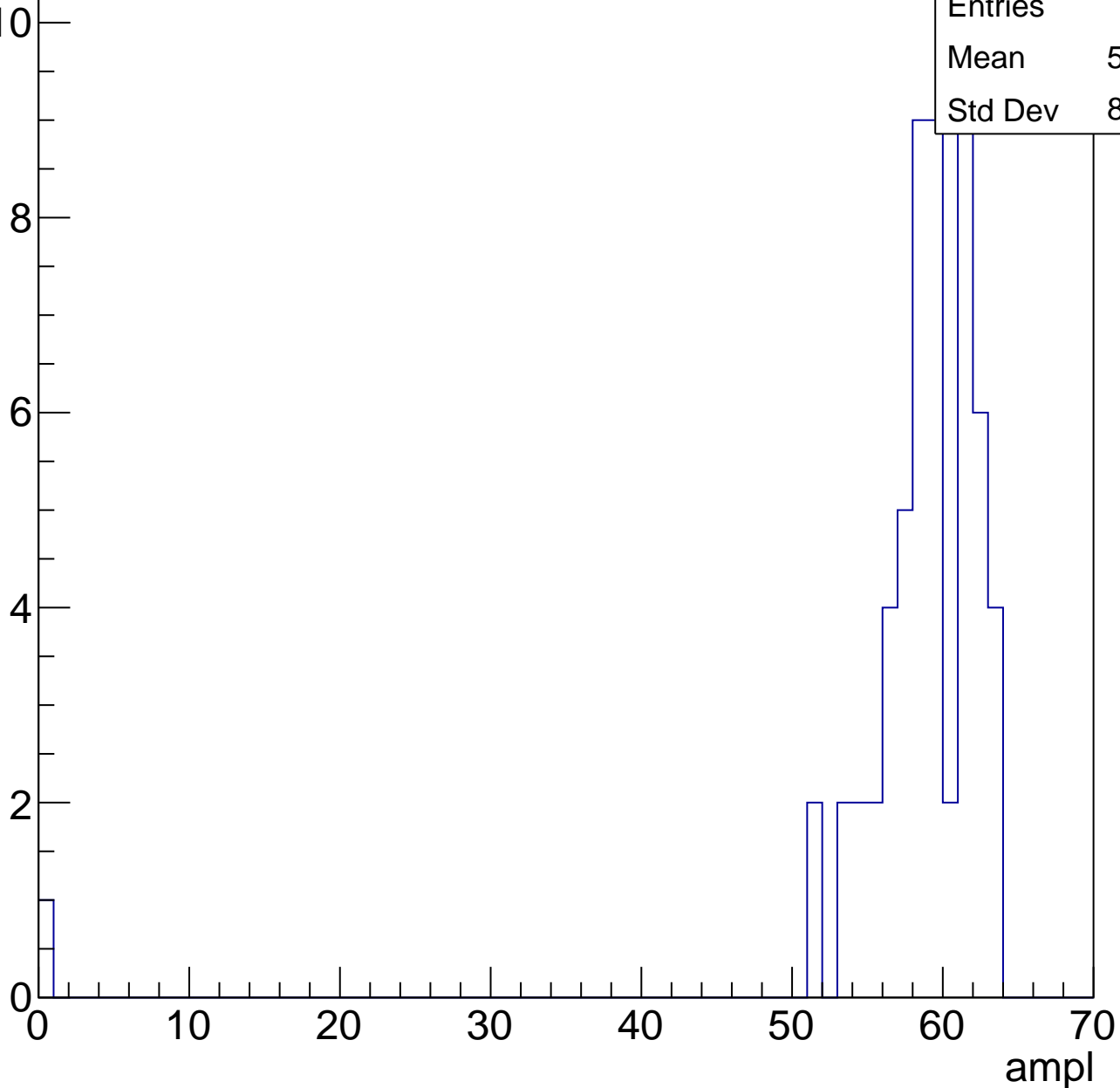


# B1L103S, U25-ch107, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	58
Mean	57.62
Std Dev	8.177

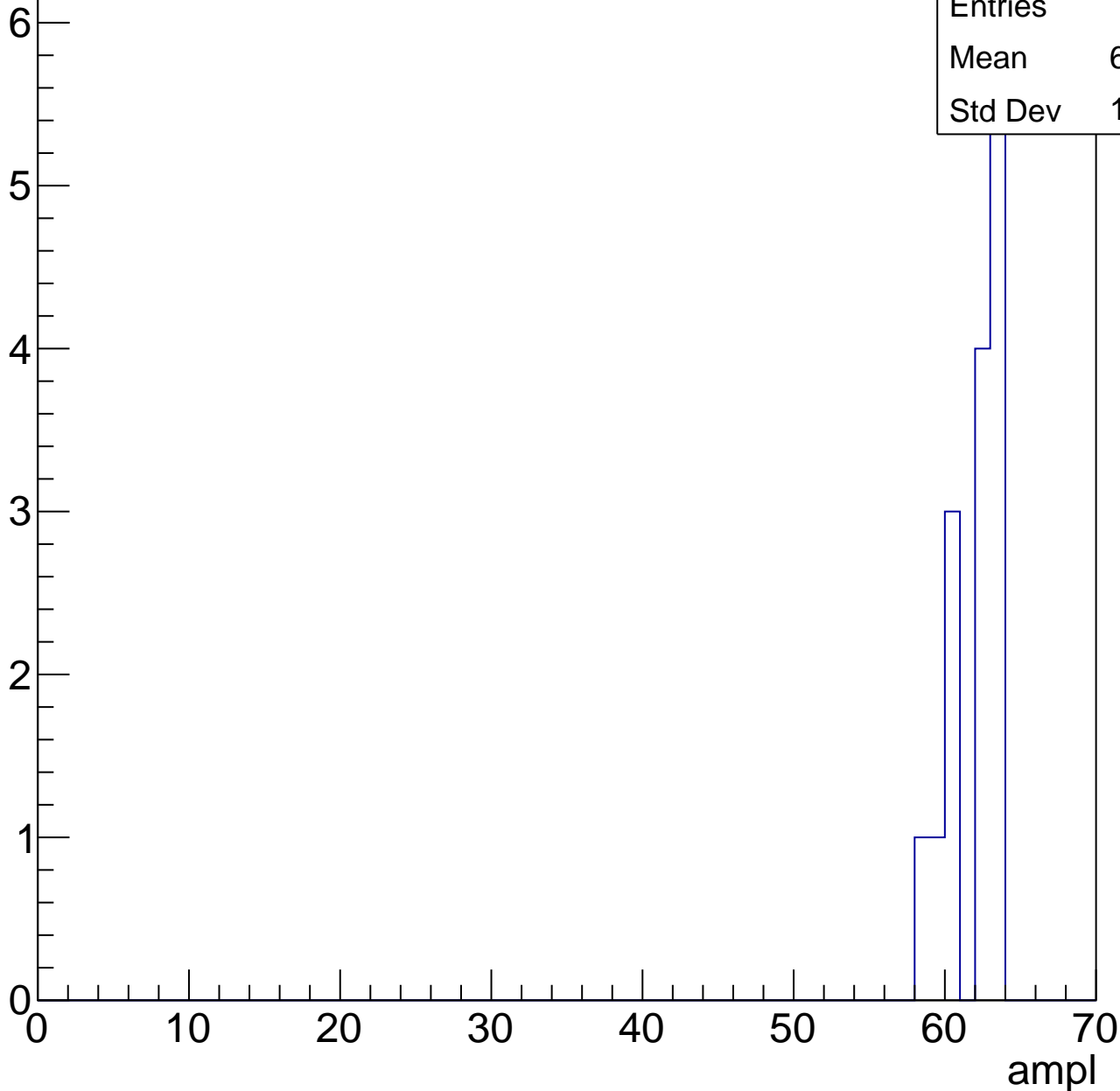


# B1L103S, U25-ch107, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	15
Mean	61.53
Std Dev	1.628

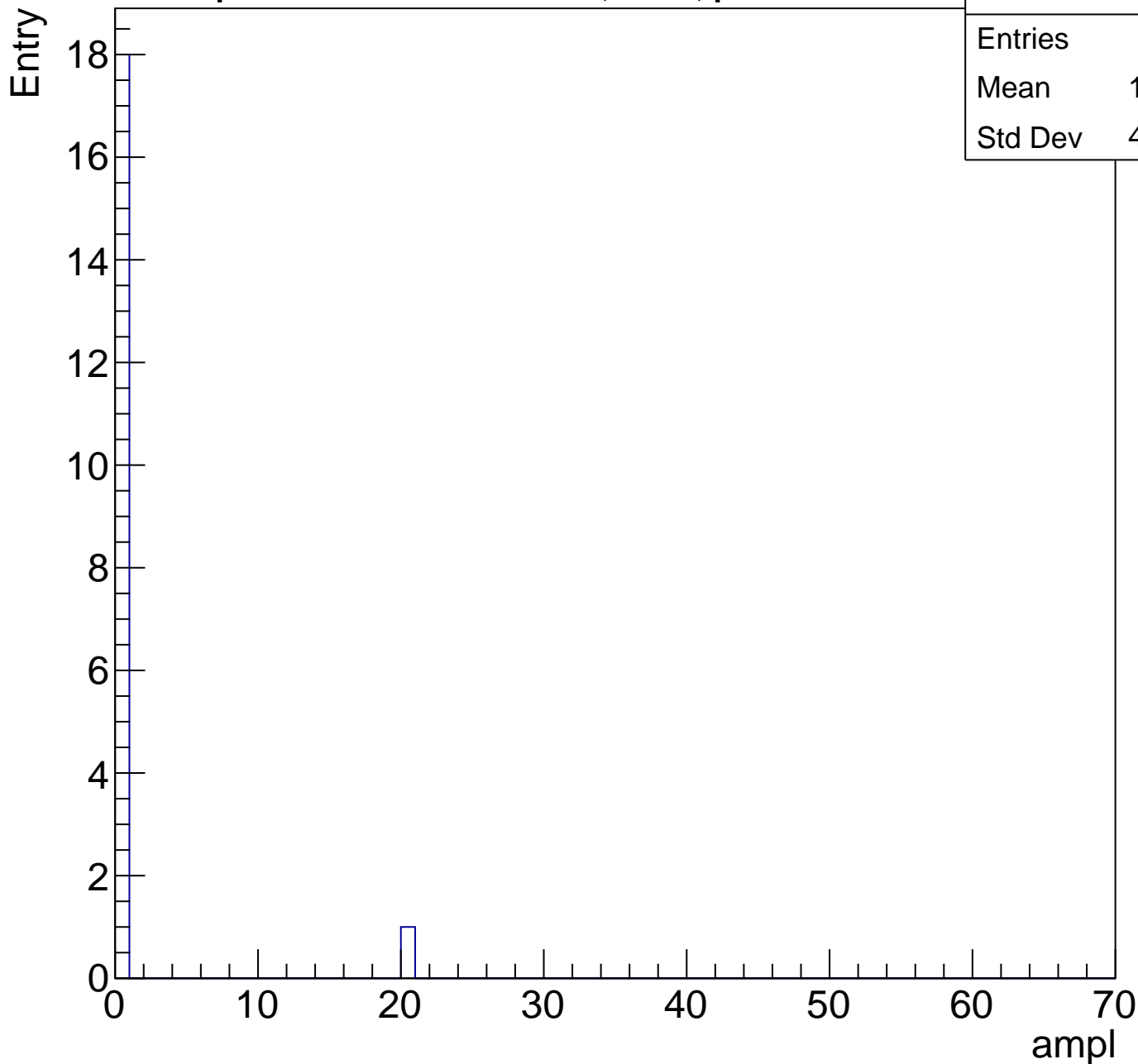




# B1L103S, U25-ch107, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

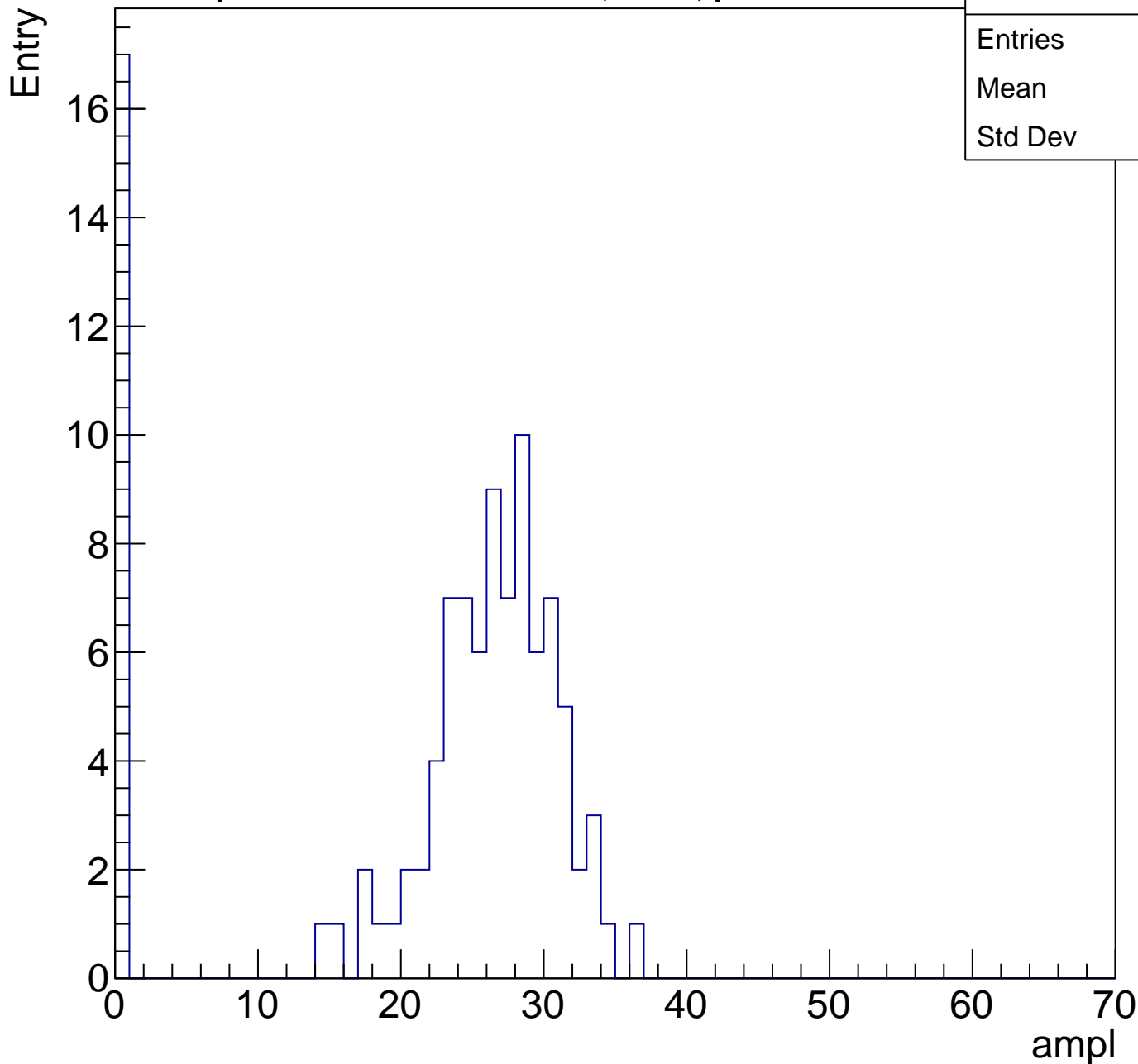
Entries	19
Mean	1.053
Std Dev	4.466



# B1L103S, U25-ch108, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	102
Mean	21.8
Std Dev	10.5

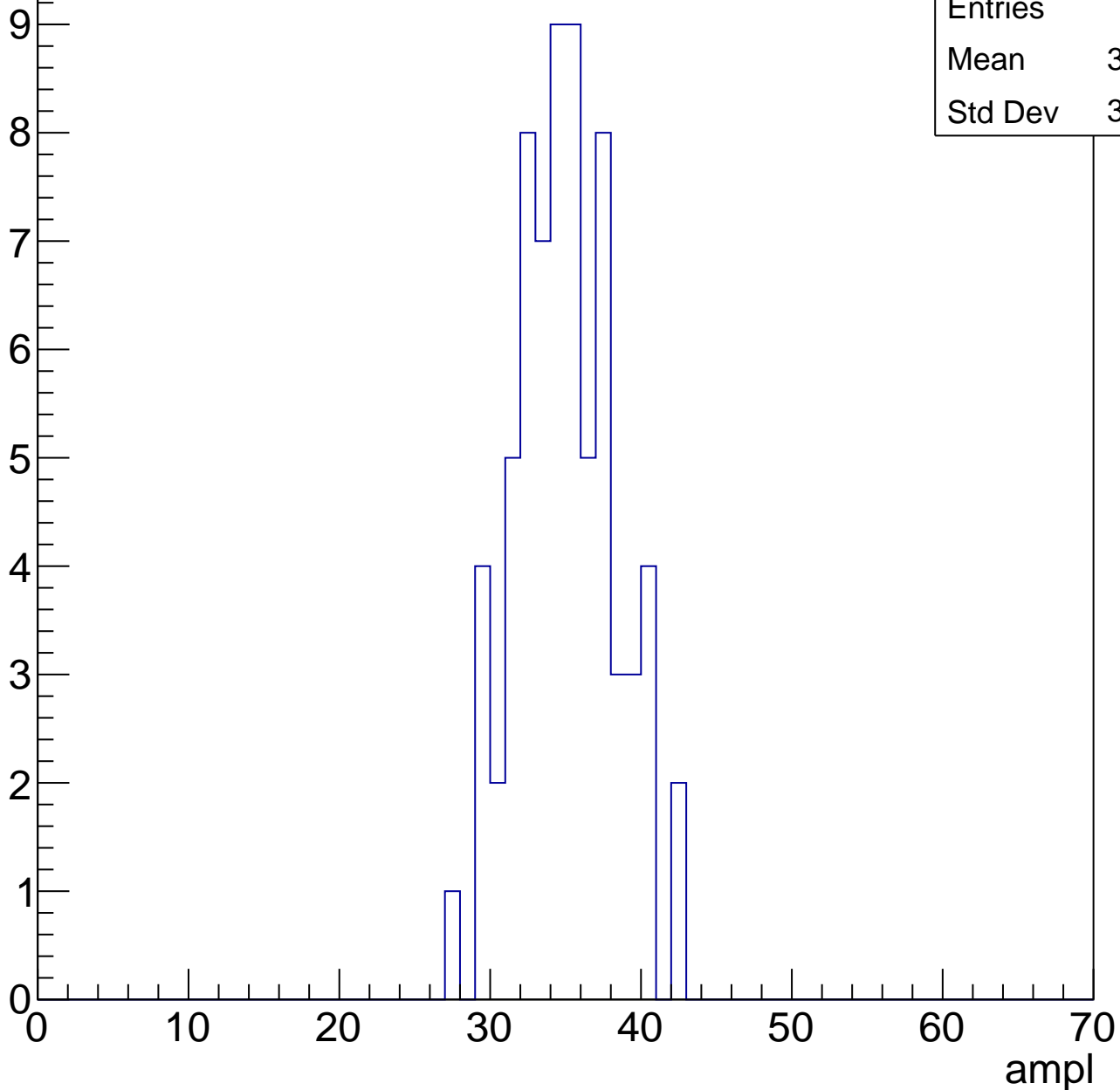


# B1L103S, U25-ch108, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

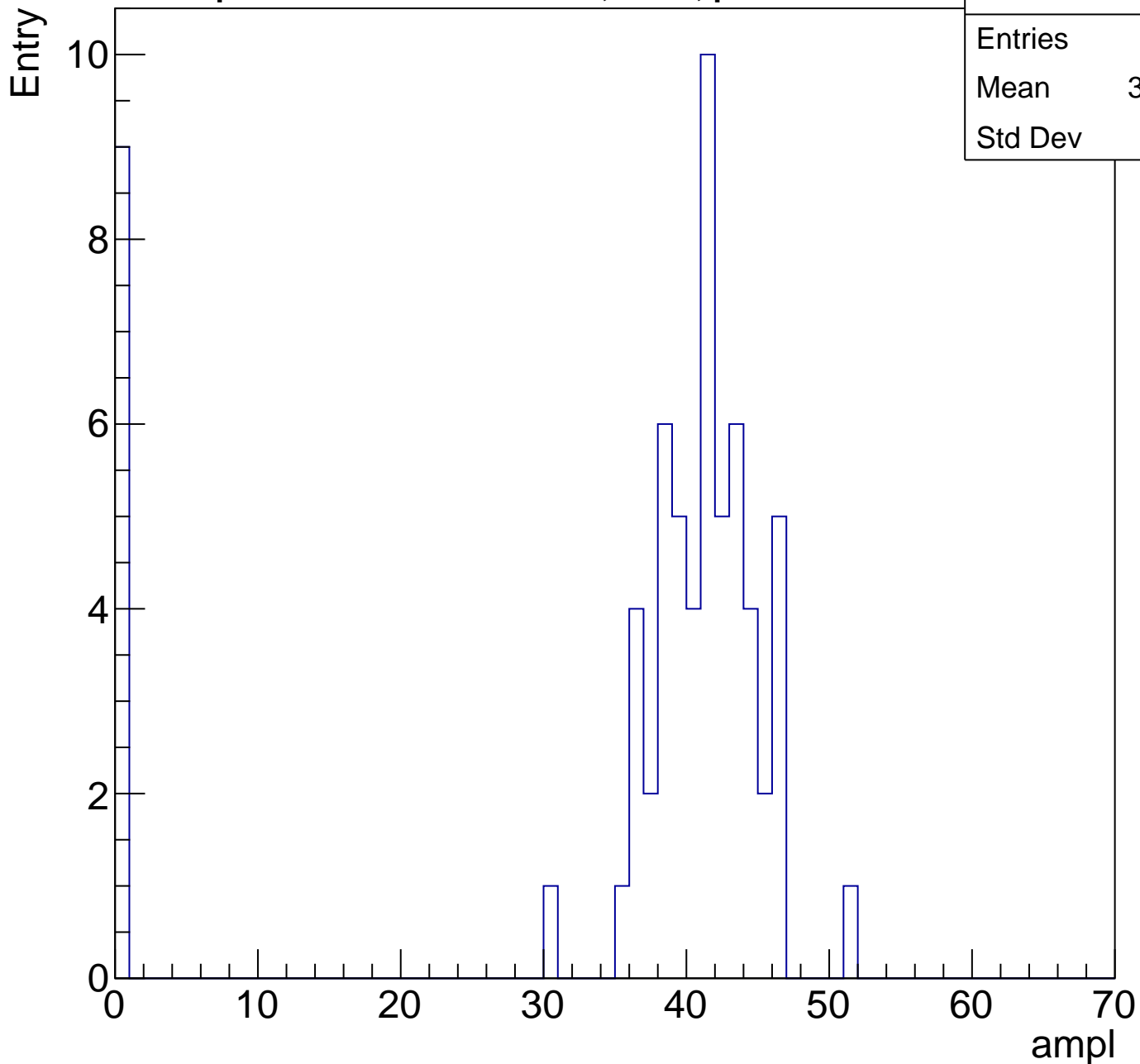
Entries	70
Mean	34.53
Std Dev	3.255



# B1L103S, U25-ch108, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	65
Mean	35.25
Std Dev	14.5

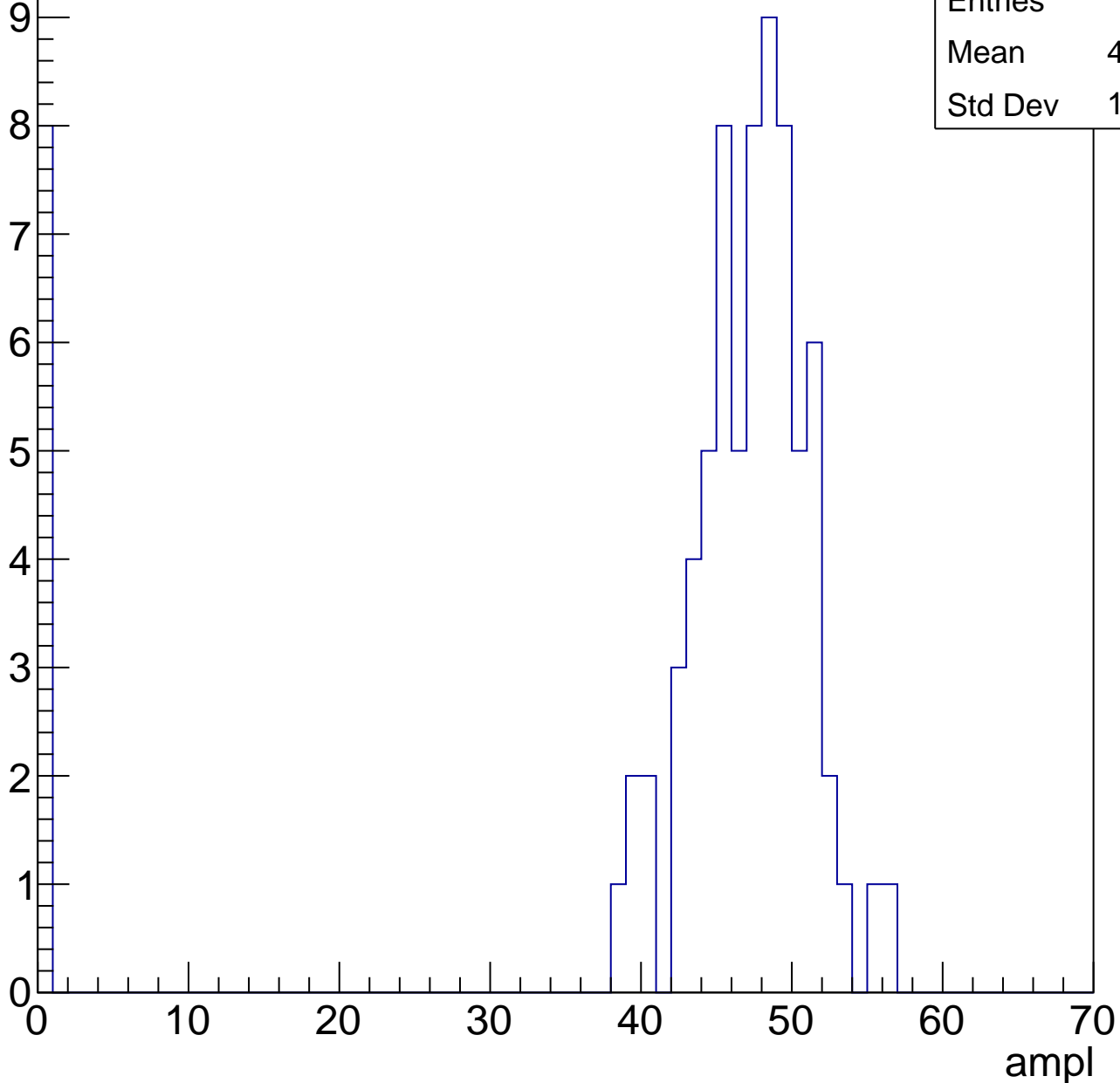


# B1L103S, U25-ch108, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	79
Mean	42.13
Std Dev	14.56

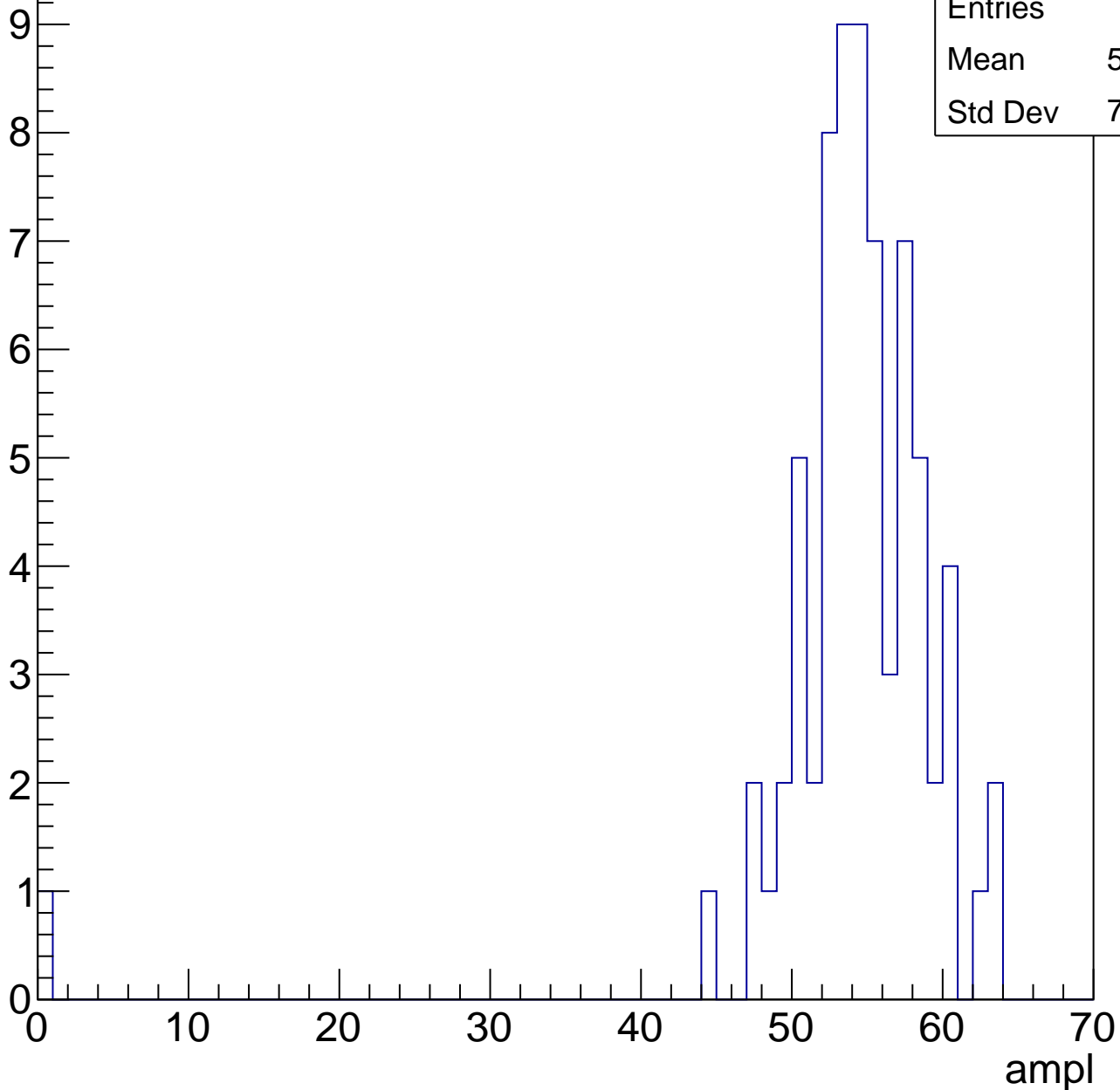


# B1L103S, U25-ch108, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	71
Mean	53.56
Std Dev	7.419

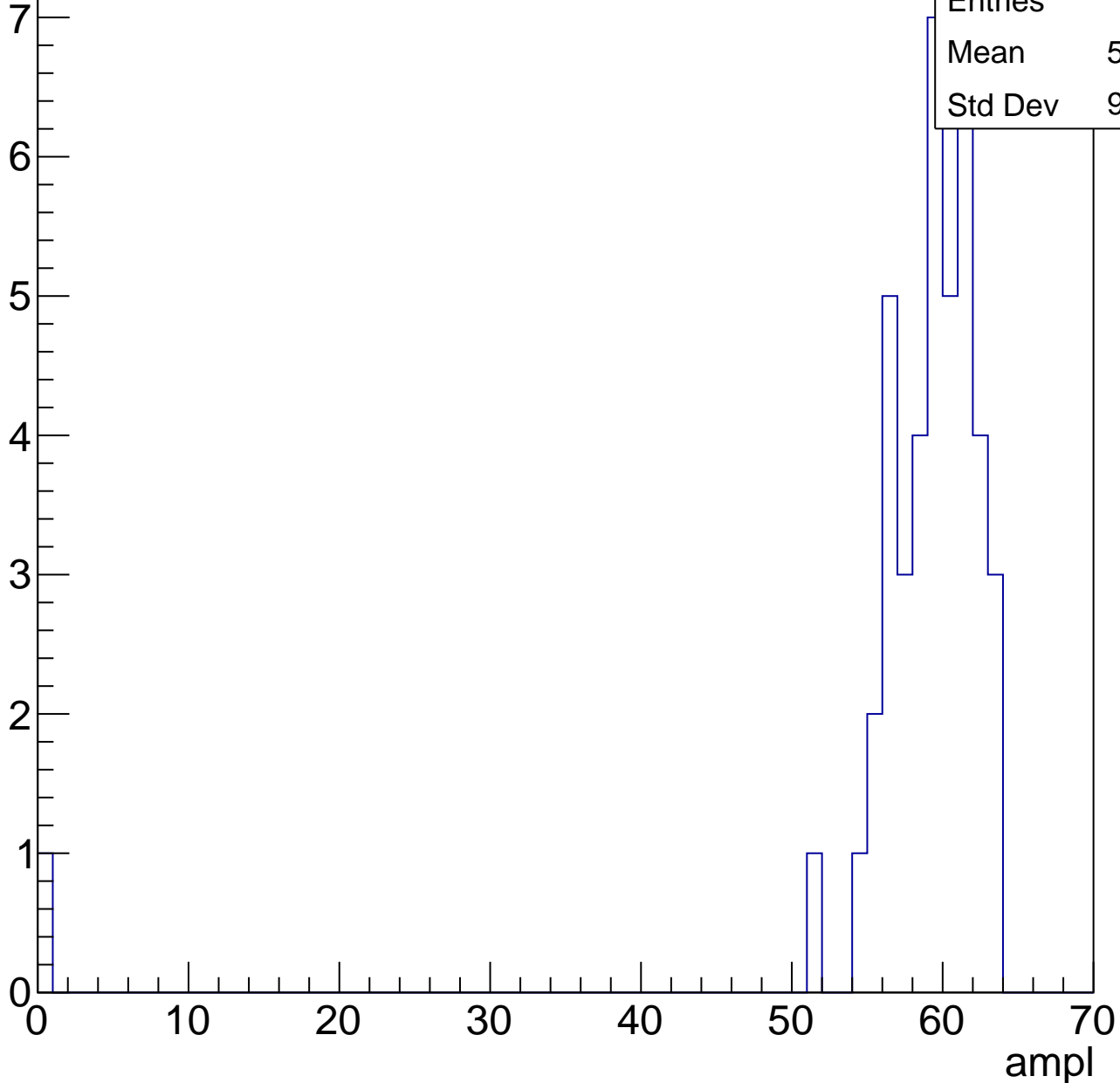


# B1L103S, U25-ch108, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	43
Mean	57.56
Std Dev	9.264

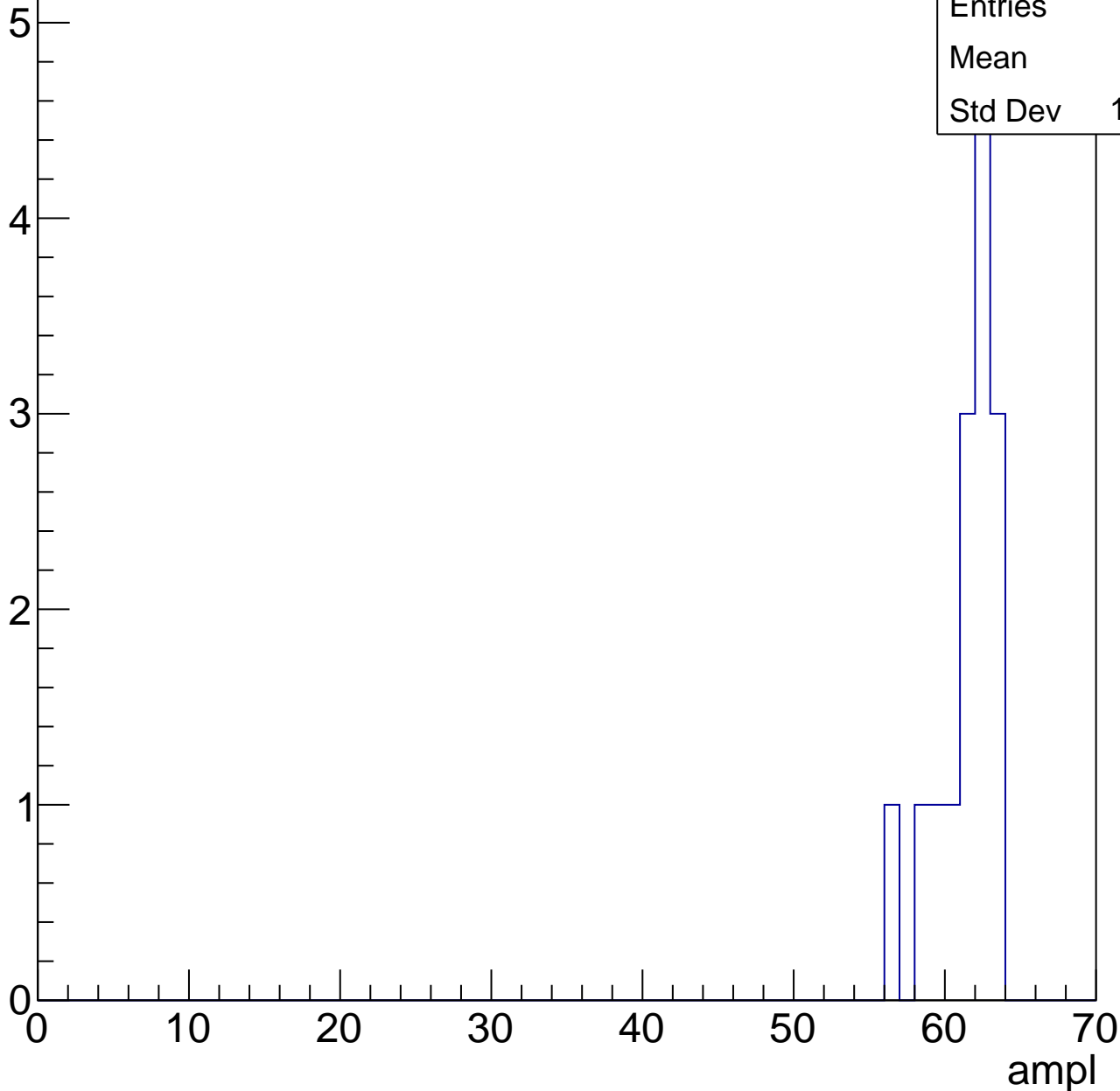


# B1L103S, U25-ch108, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	15
Mean	61
Std Dev	1.932





# B1L103S, U25-ch108, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	21
Mean	6
Std Dev	18.49

Entry



# B1L103S, U25-ch109, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

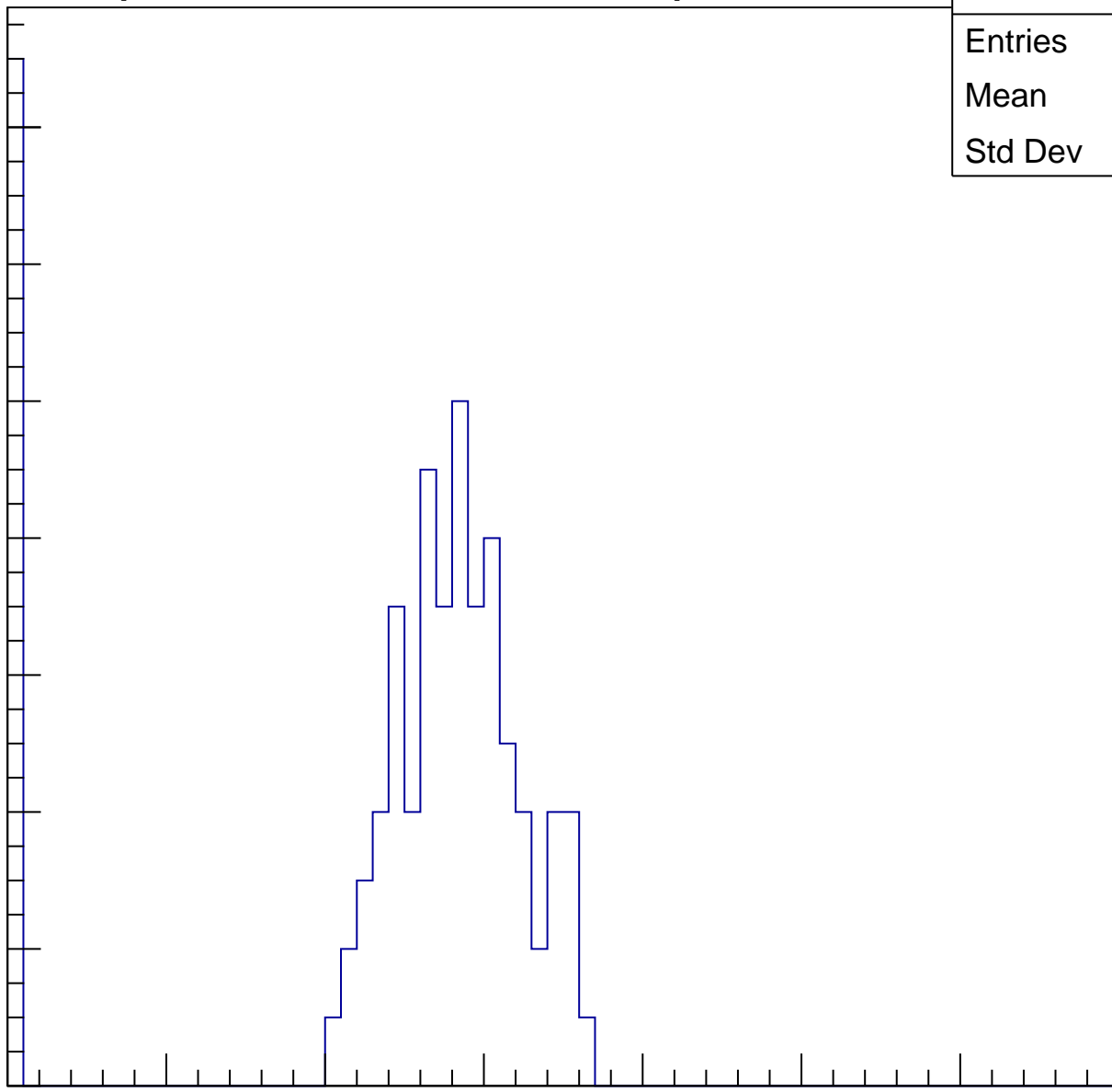
Entries	97
Mean	23.66
Std Dev	10.7

Entry

14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

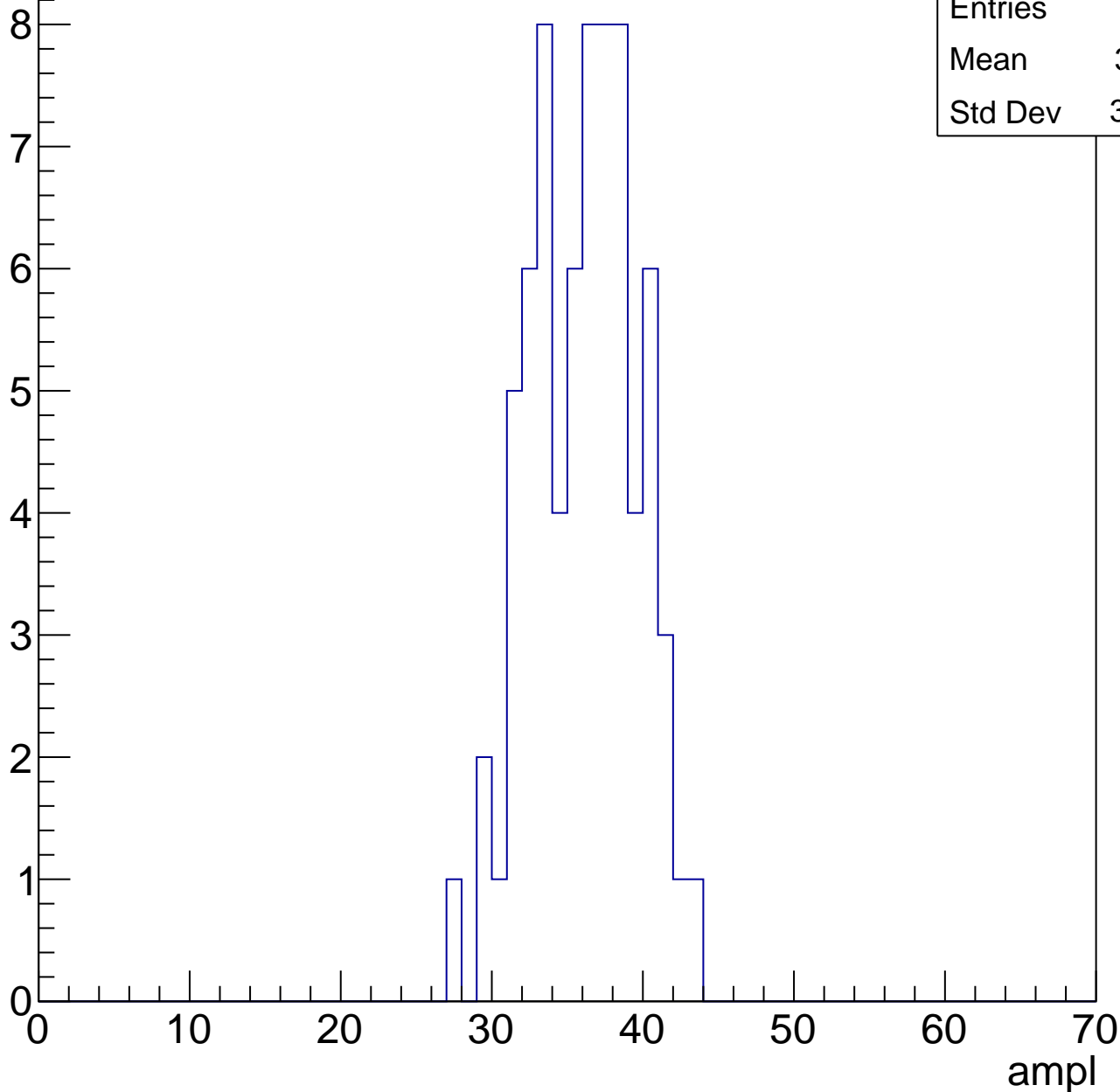


# B1L103S, U25-ch109, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	72
Mean	35.61
Std Dev	3.438

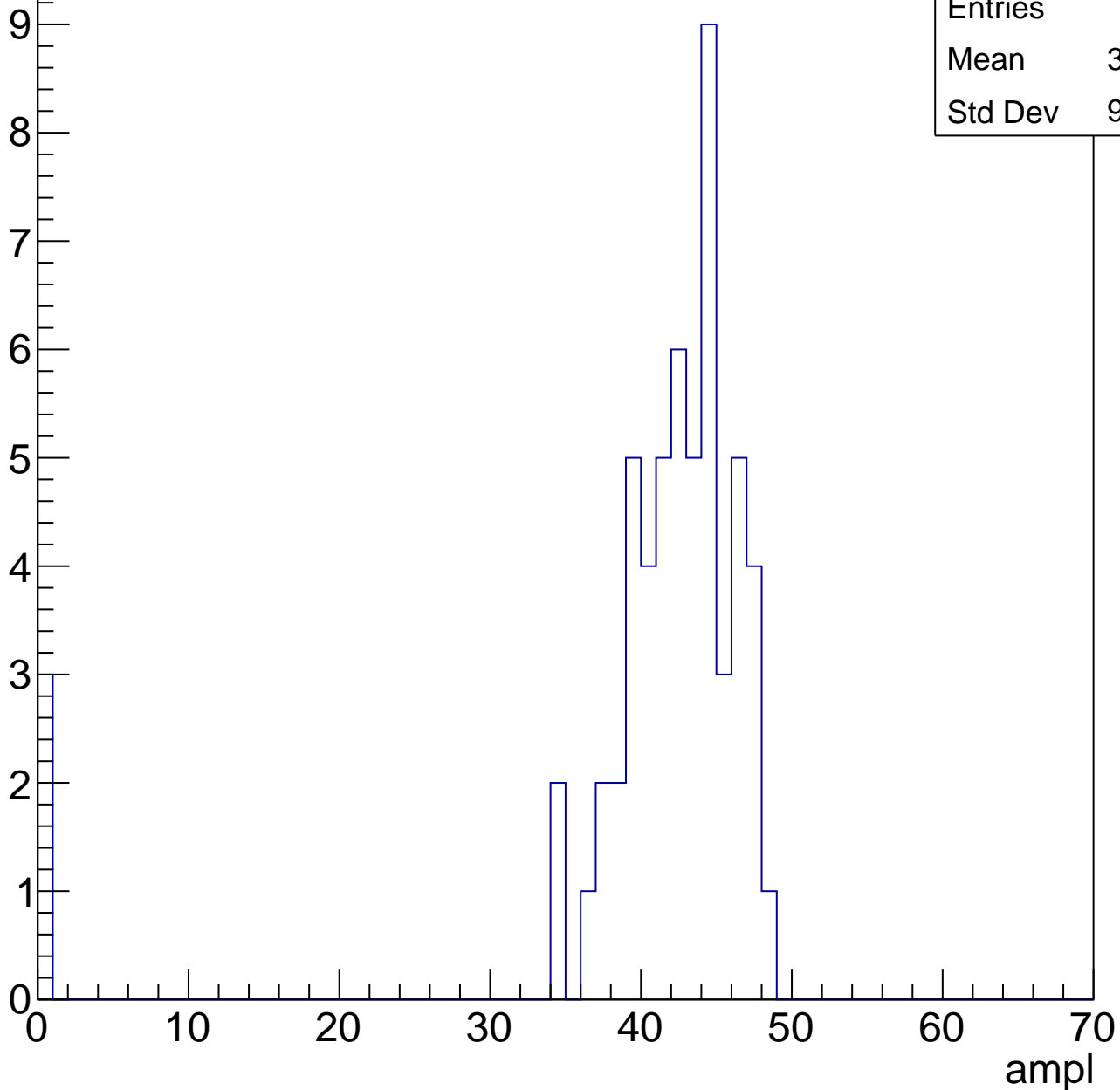


# B1L103S, U25-ch109, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	57
Mean	39.96
Std Dev	9.958

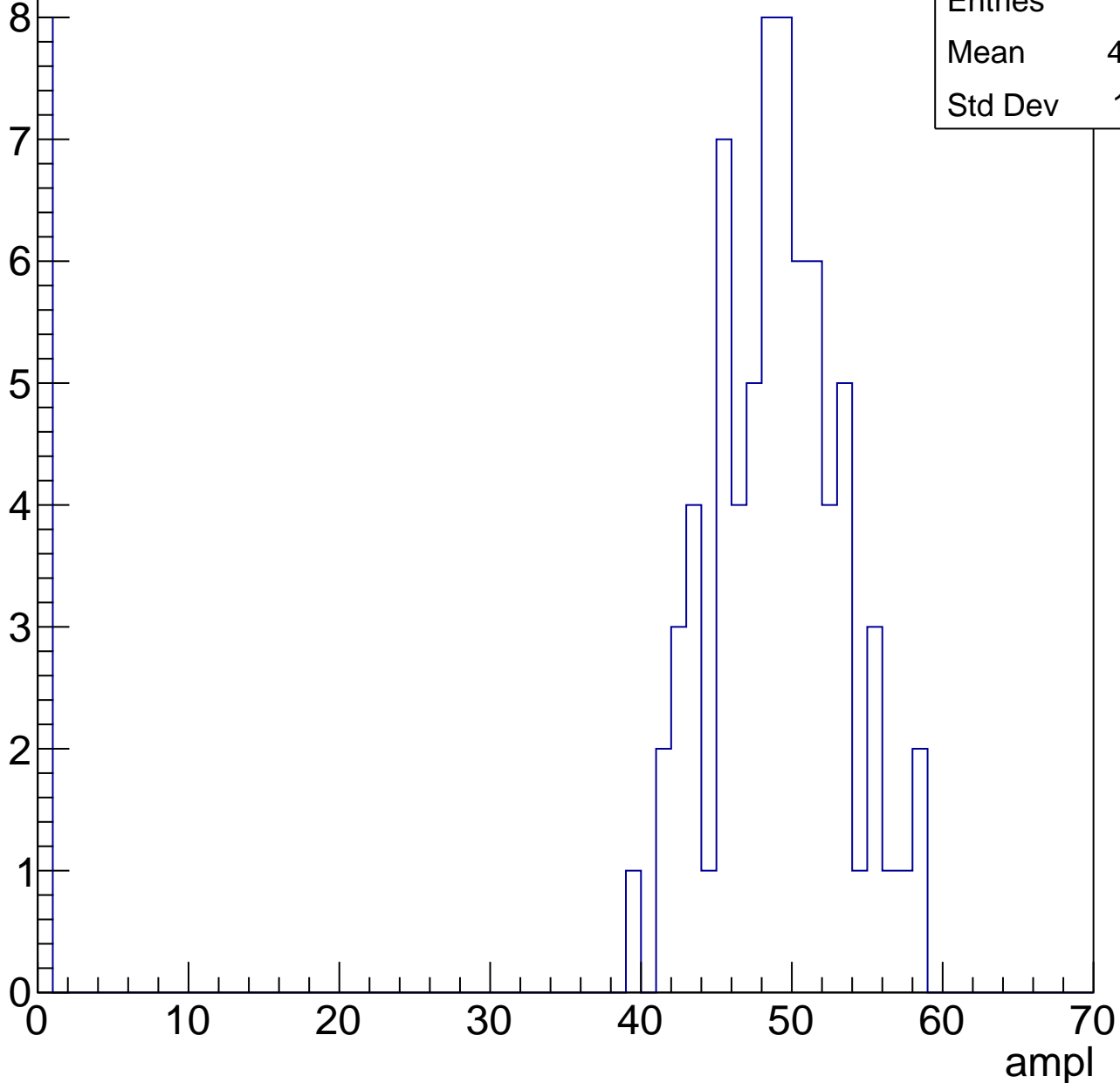


# B1L103S, U25-ch109, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	80
Mean	43.75
Std Dev	15.11

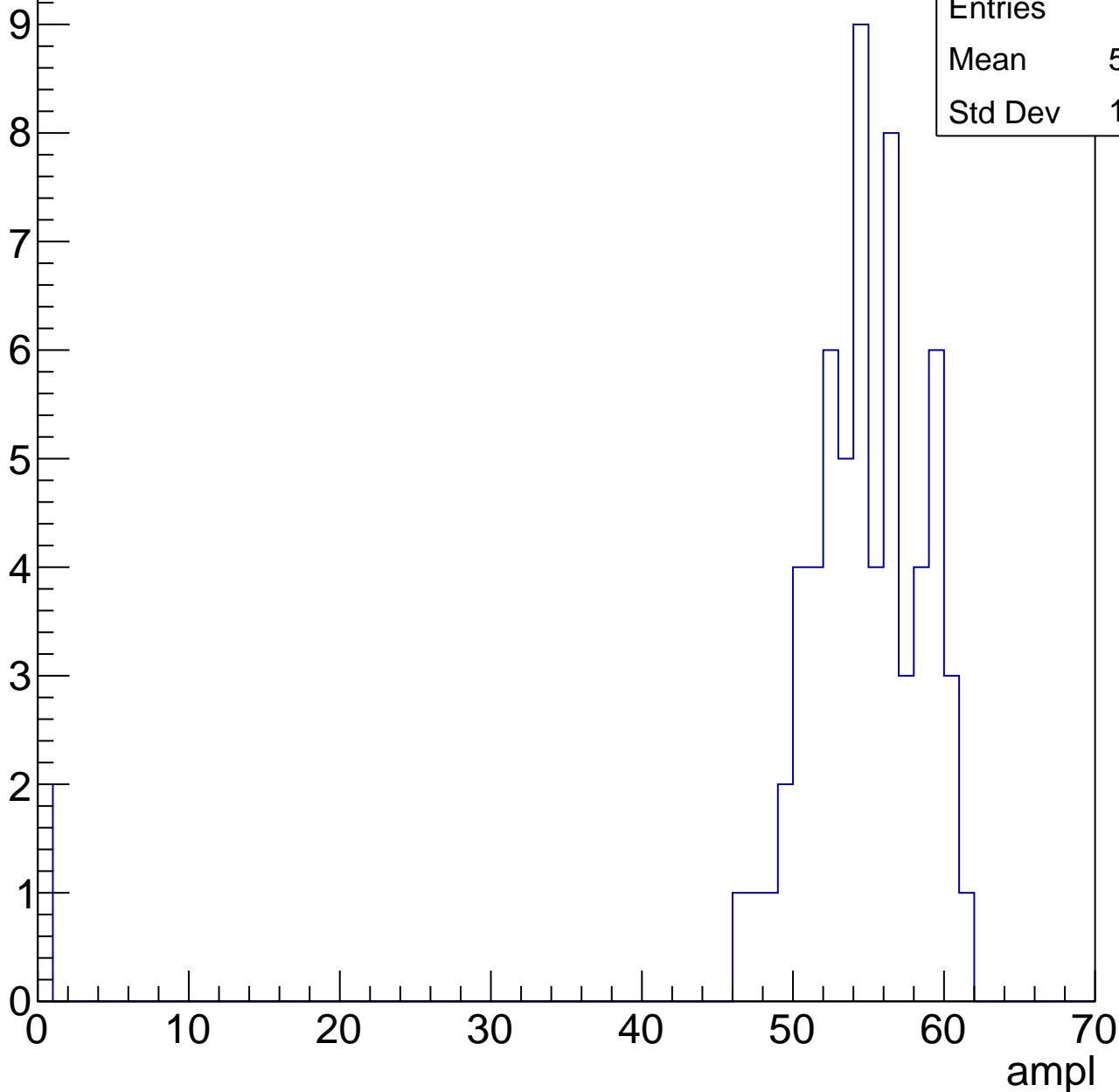


# B1L103S, U25-ch109, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	64
Mean	52.69
Std Dev	10.07

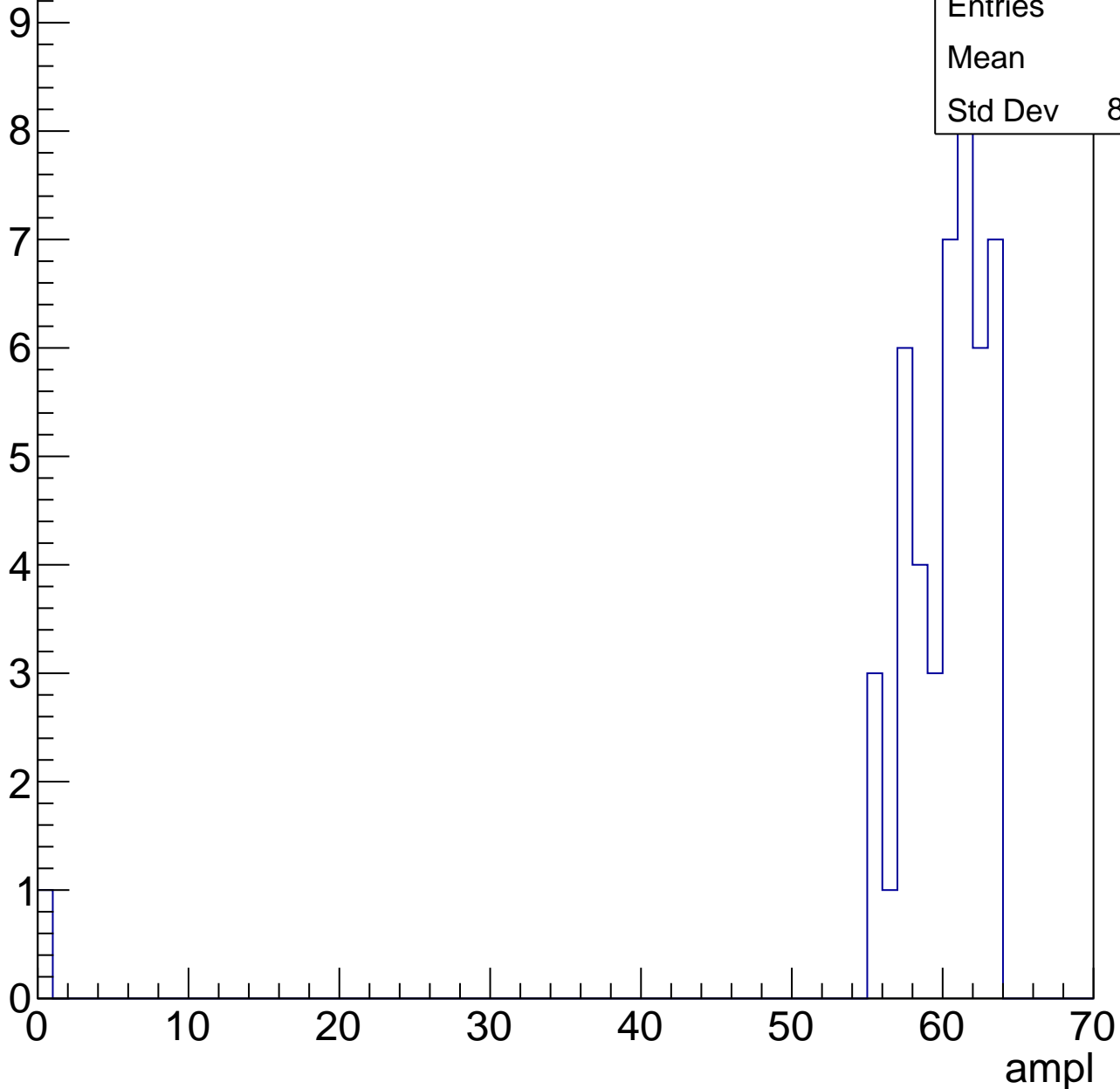


# B1L103S, U25-ch109, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

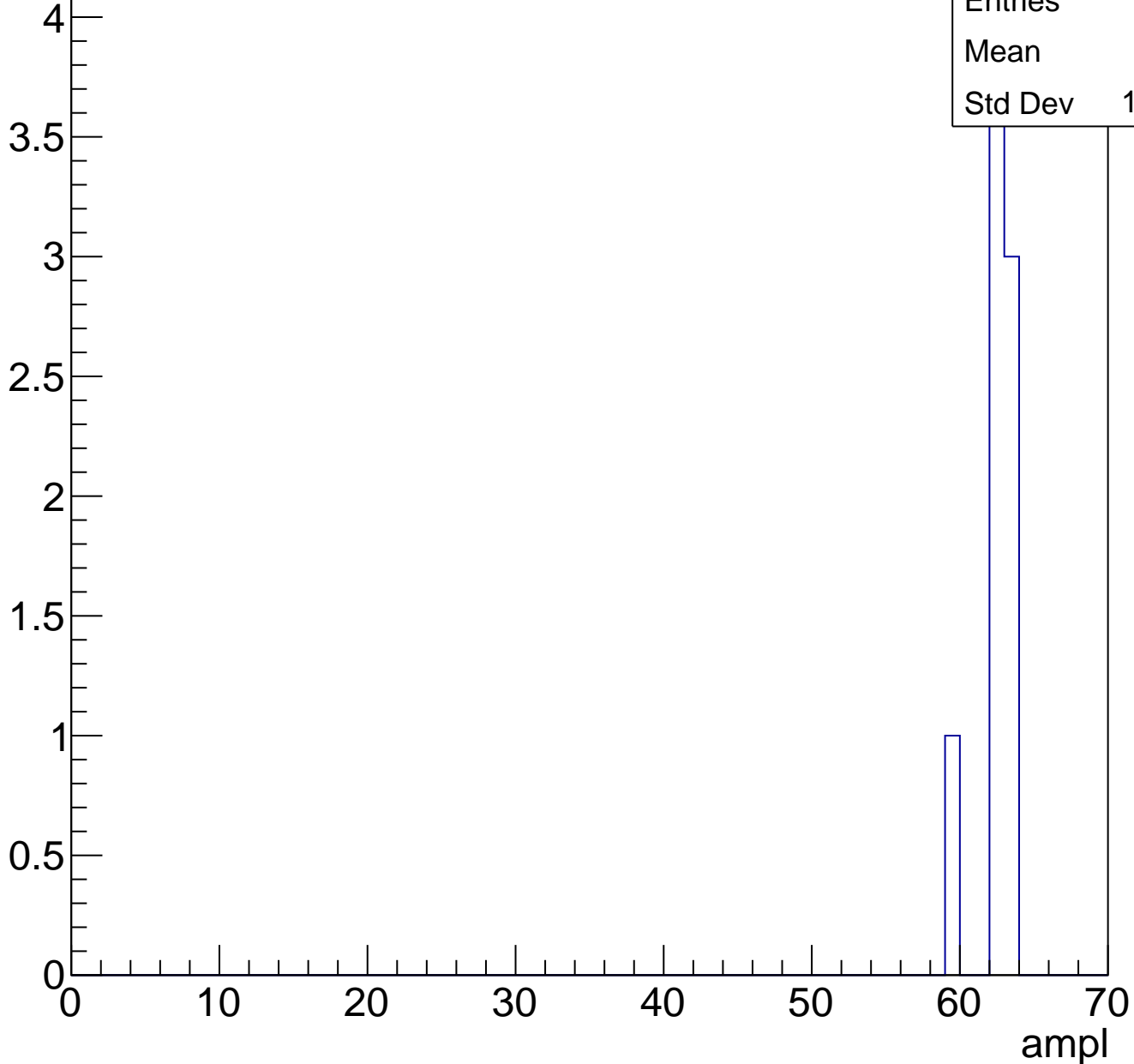
Entries	47
Mean	58.6
Std Dev	8.953



# B1L103S, U25-ch109, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U25-ch109, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

# B1L103S, U25-ch110, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	91
Mean	21.24
Std Dev	9.785

Entry

14  
12  
10  
8  
6  
4  
2  
0

0

10

20

30

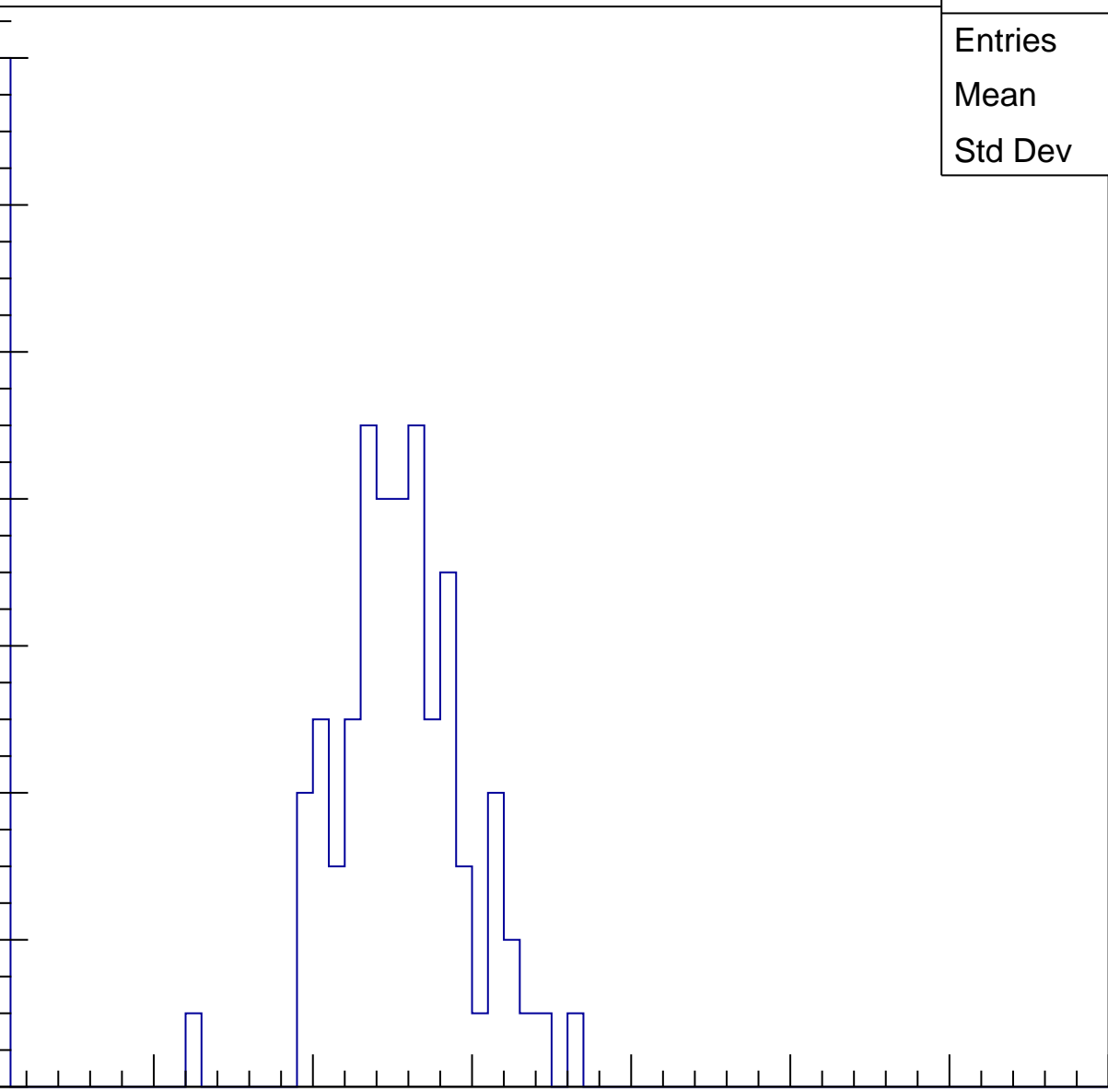
40

50

60

70

ampl

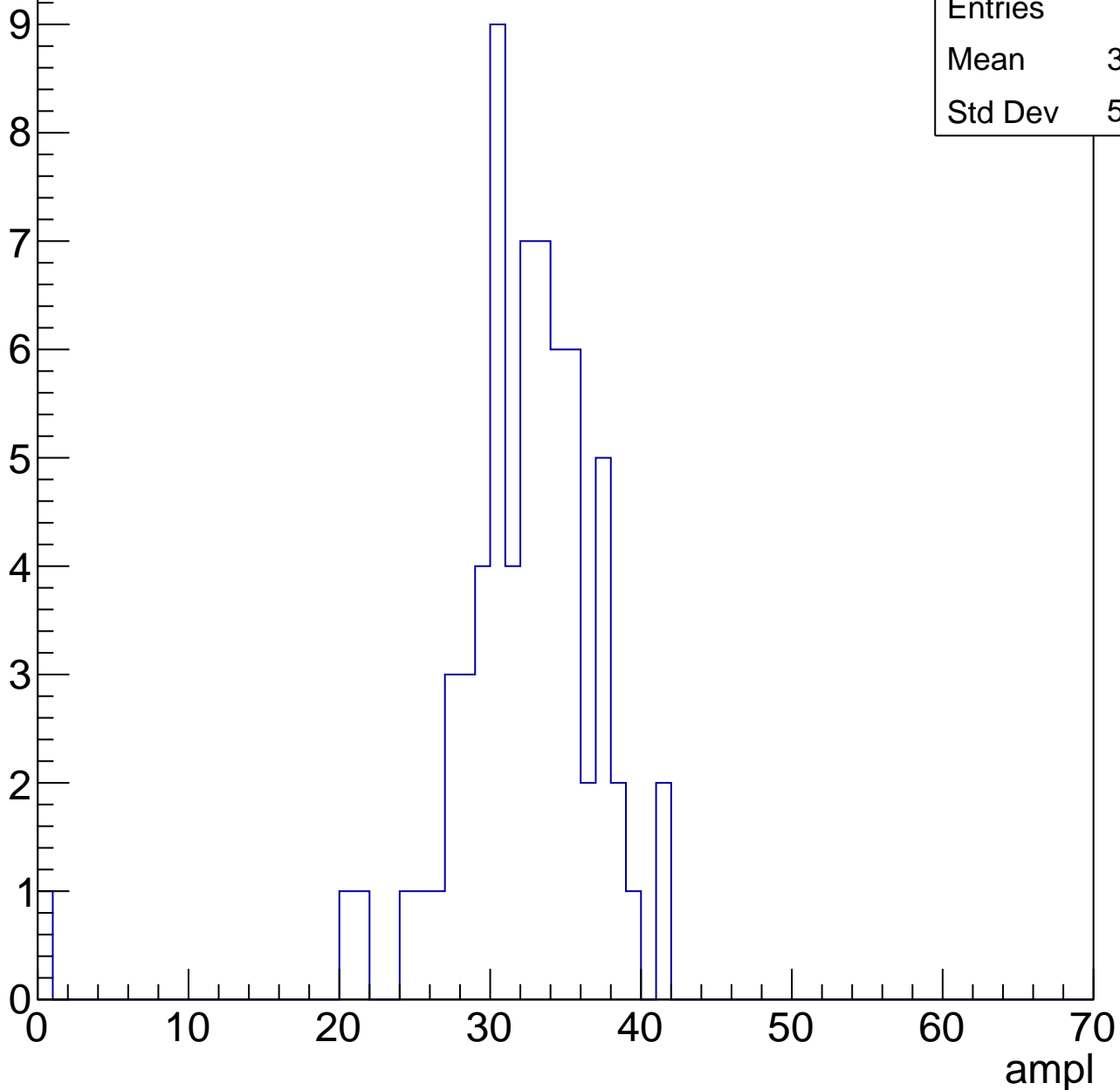


# B1L103S, U25-ch110, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	67
Mean	31.55
Std Dev	5.663

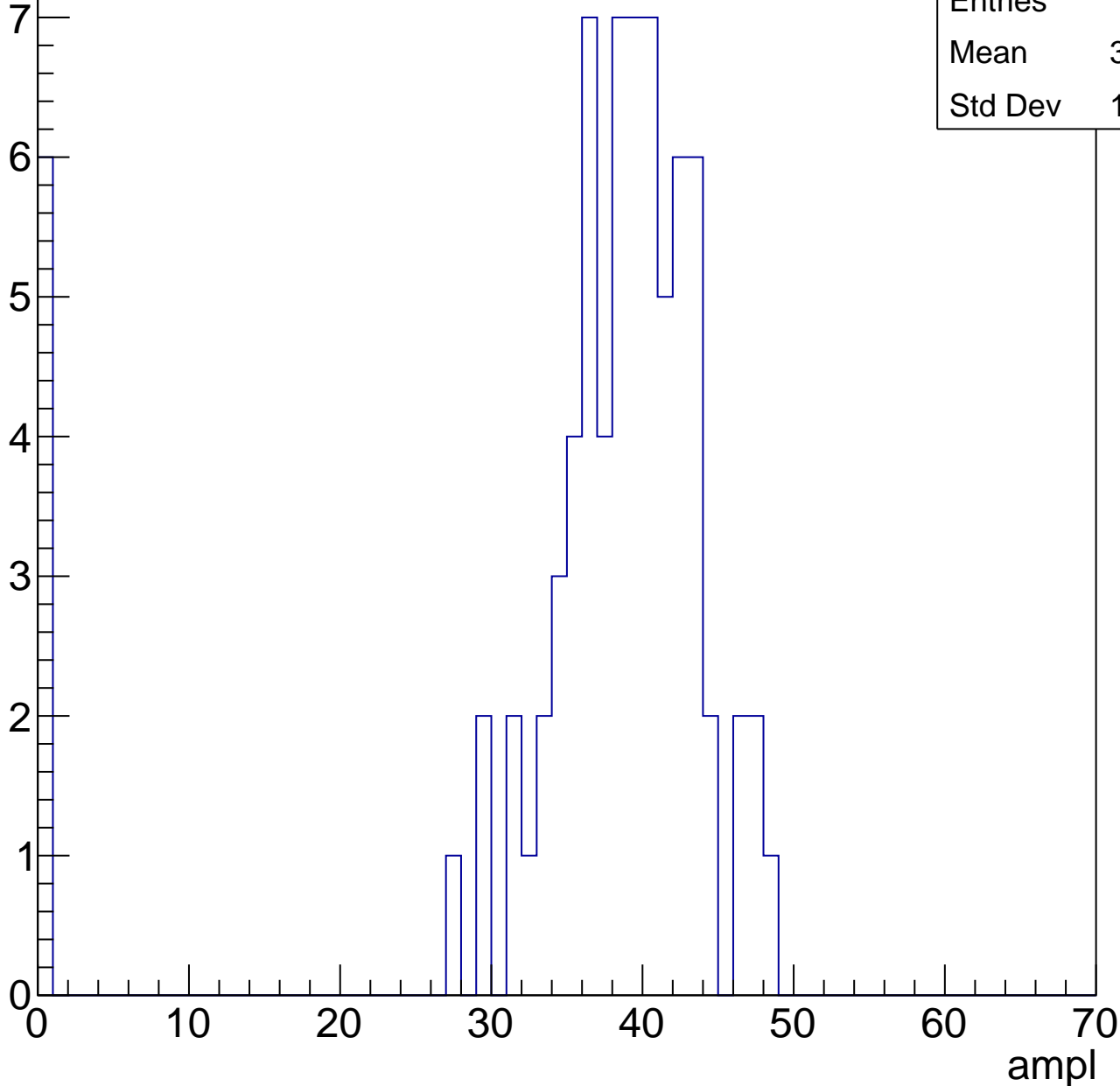


# B1L103S, U25-ch110, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	77
Mean	35.62
Std Dev	11.17



# B1L103S, U25-ch110, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

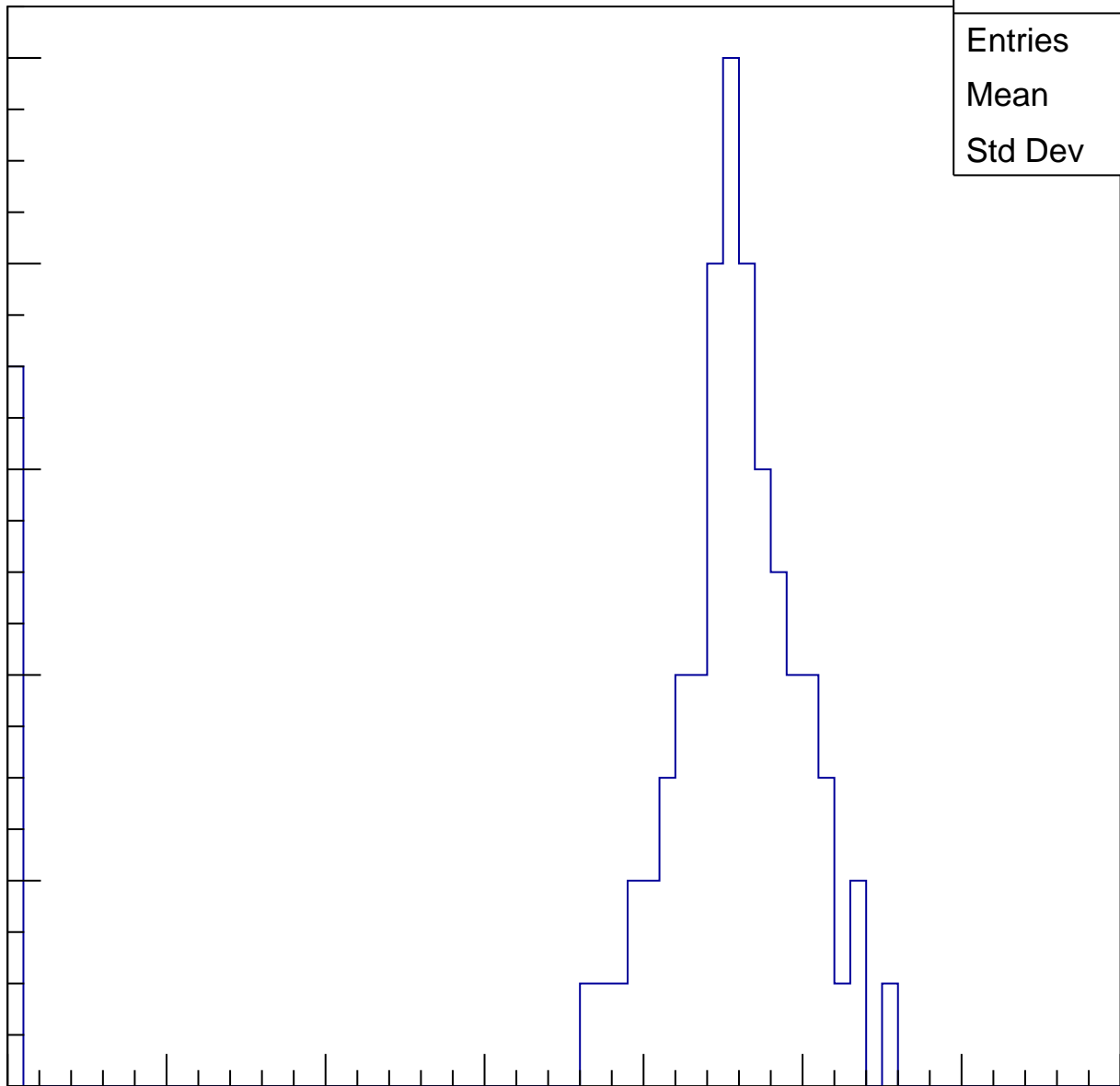
Entries	77
Mean	41.38
Std Dev	13.59

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

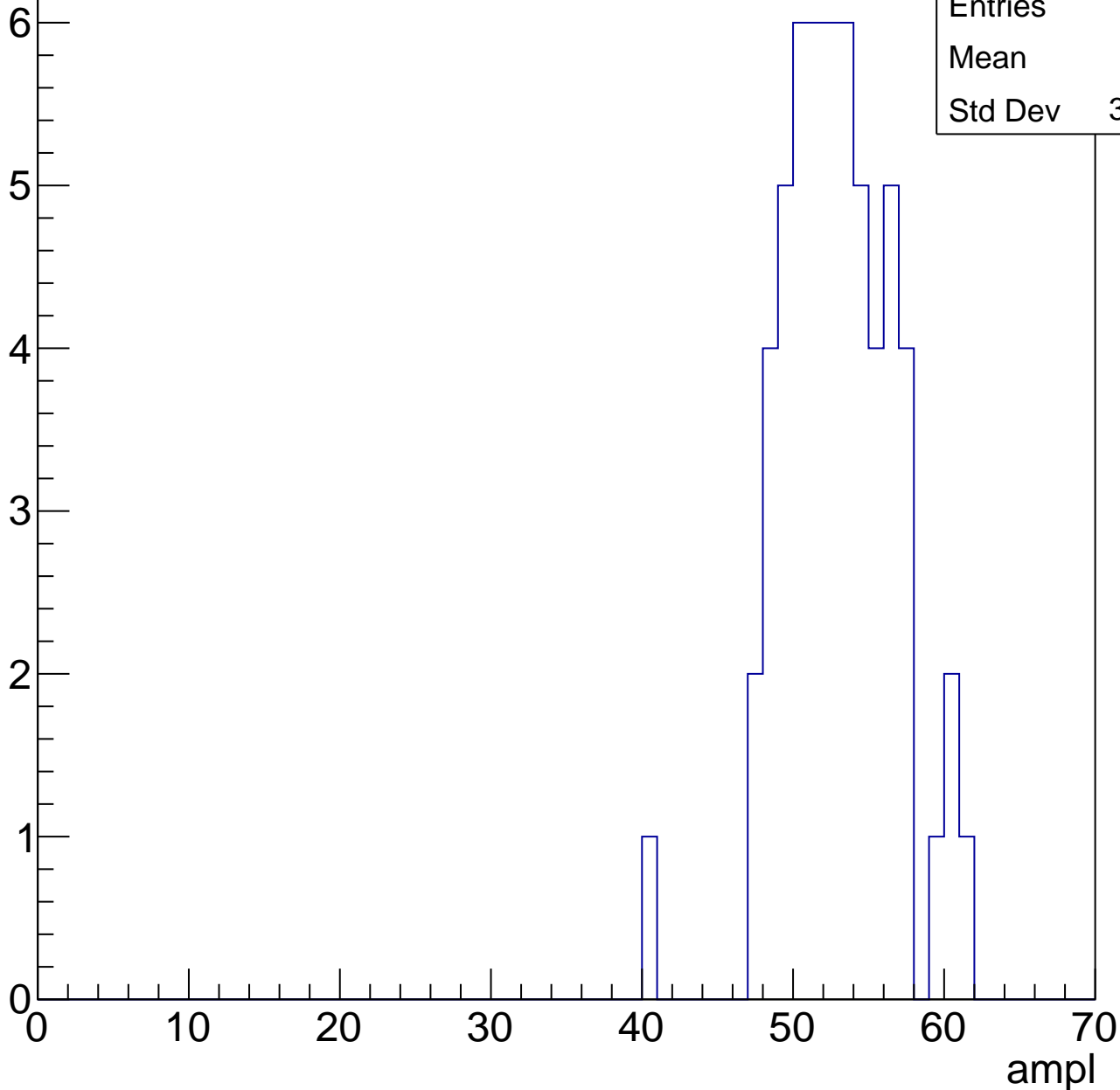


# B1L103S, U25-ch110, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	58
Mean	52.5
Std Dev	3.757

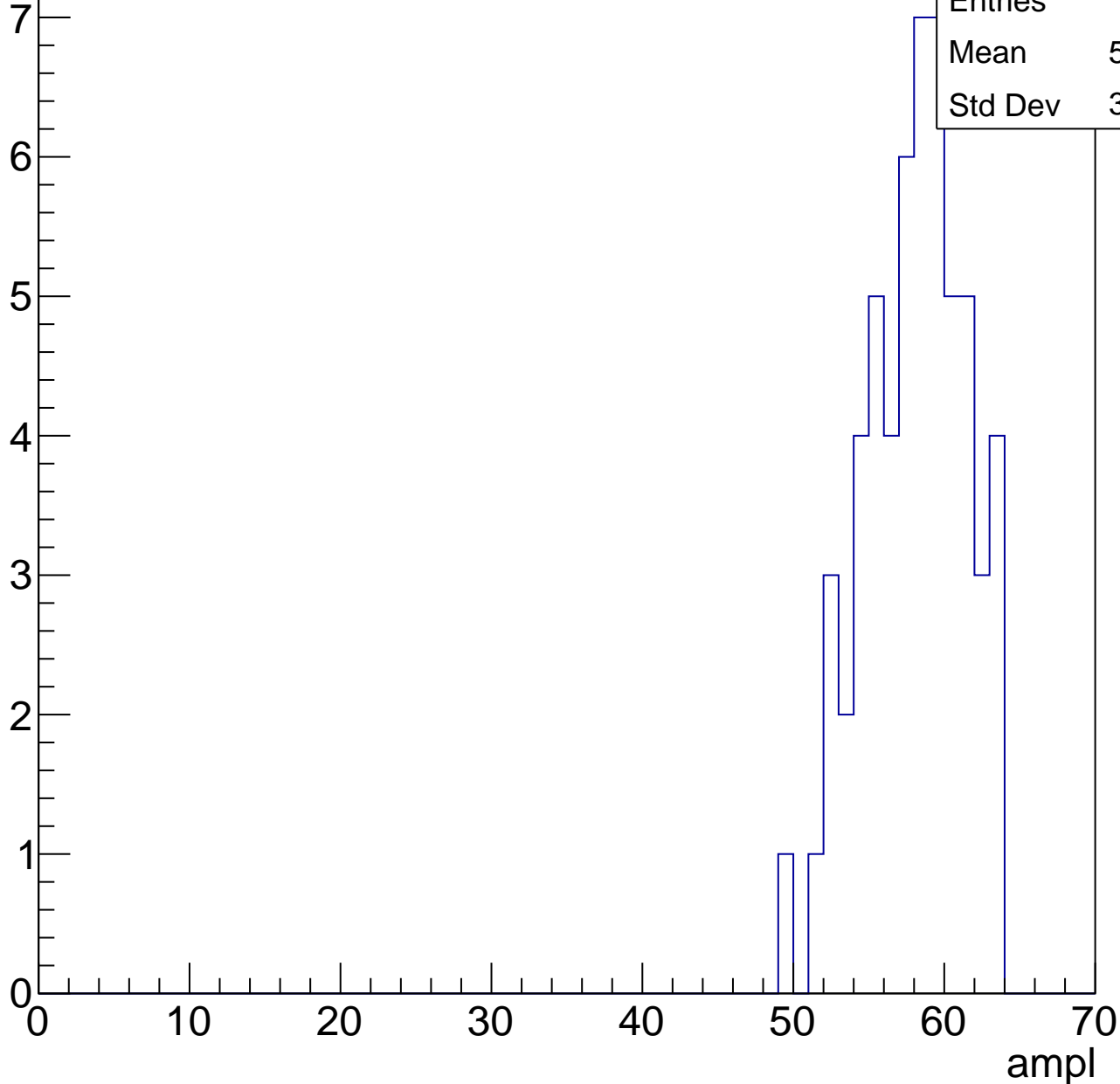


# B1L103S, U25-ch110, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	57
Mean	57.56
Std Dev	3.319

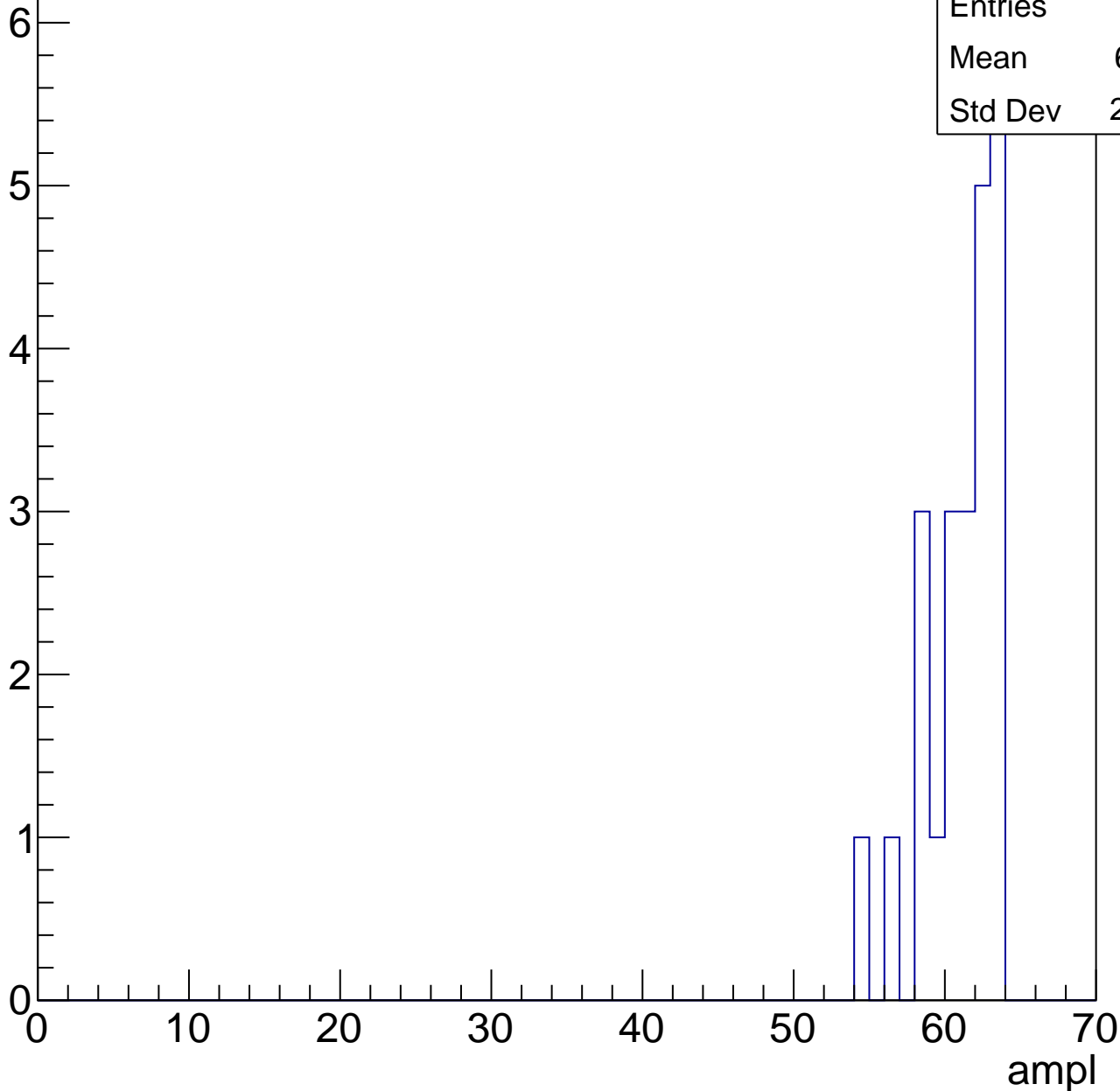


# B1L103S, U25-ch110, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	23
Mean	60.61
Std Dev	2.409





# B1L103S, U25-ch110, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

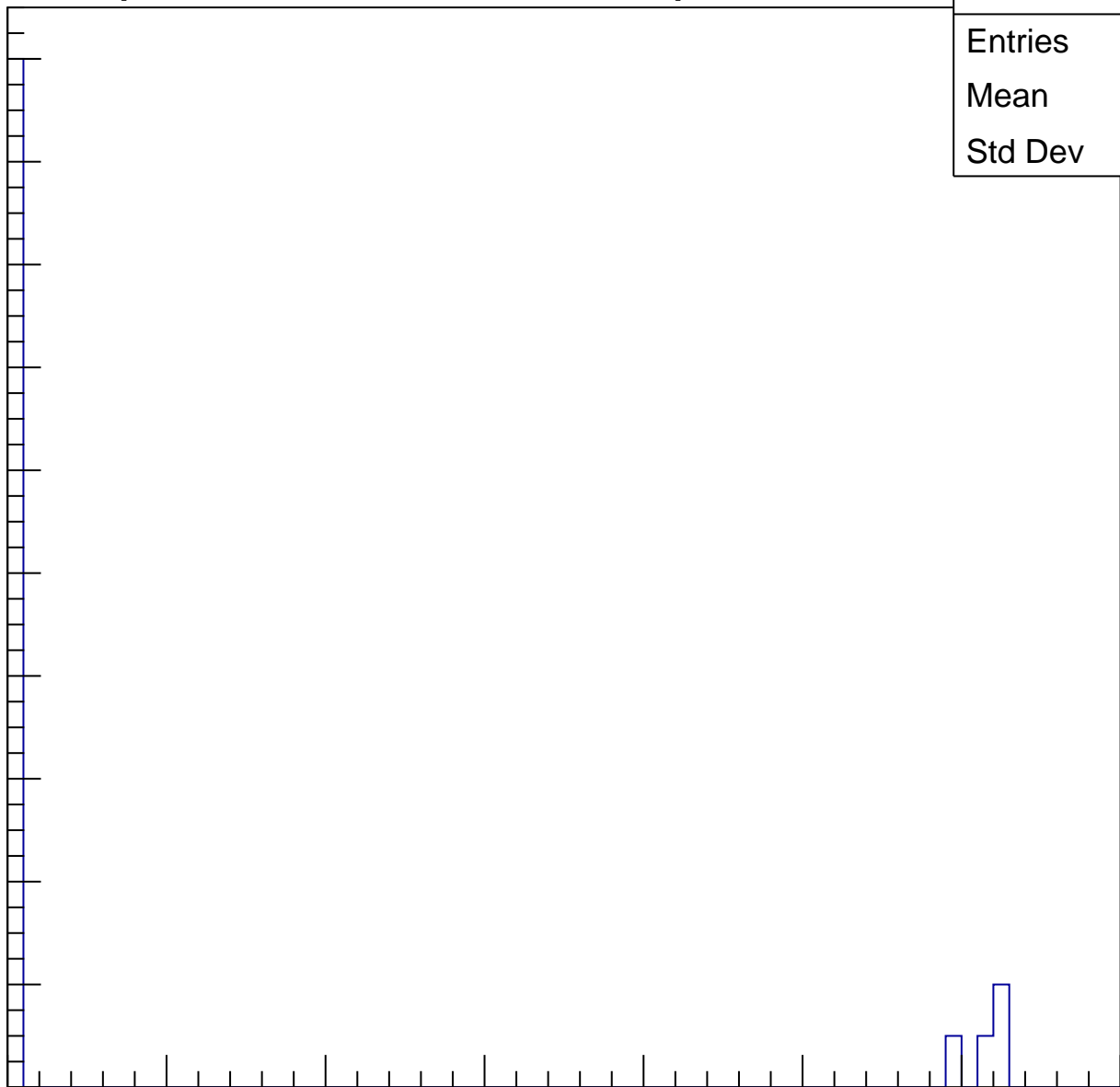
Entries	24
Mean	10.17
Std Dev	22.74

Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L103S, U25-ch111, adc0

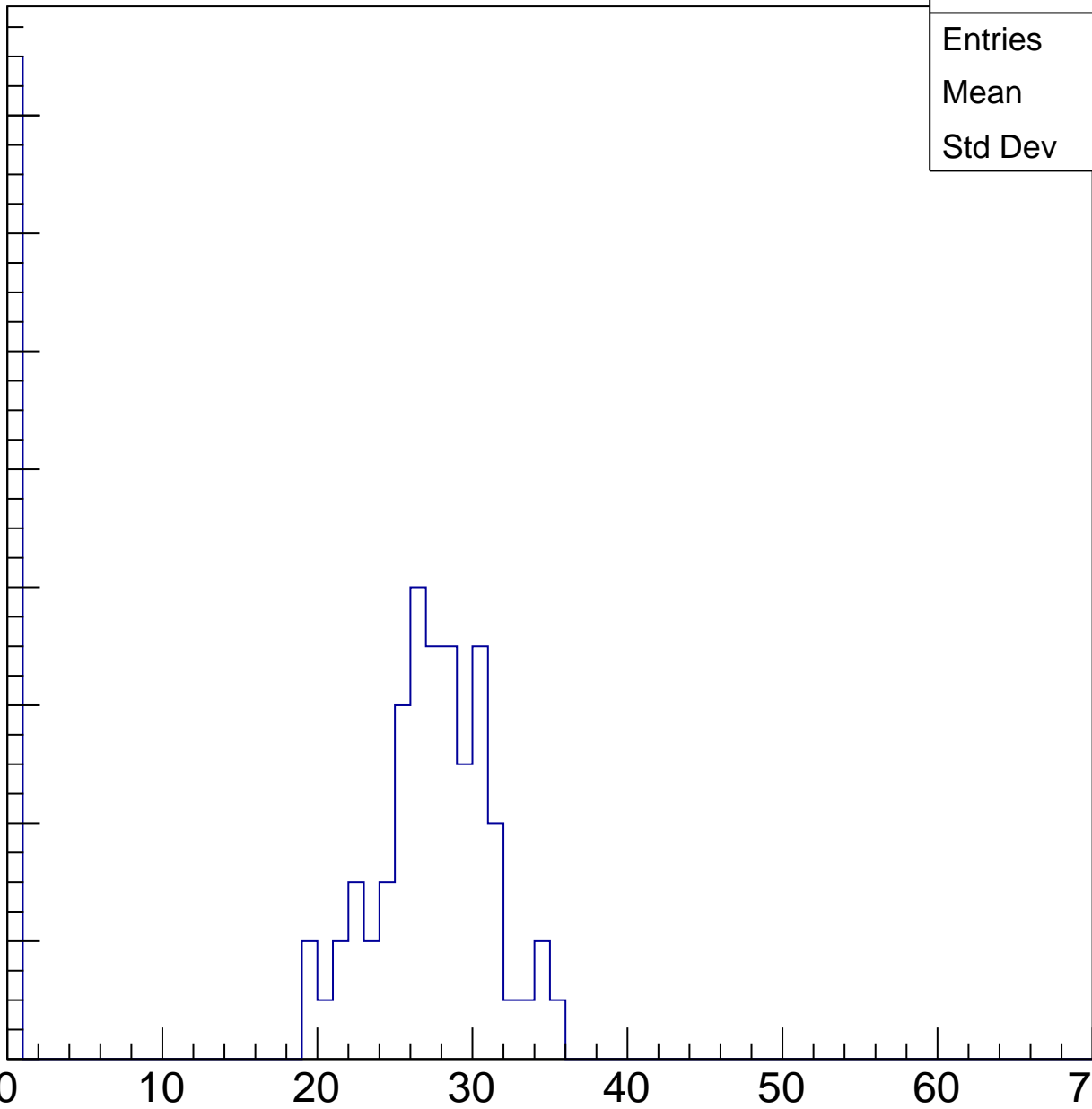
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	79
Mean	21.19
Std Dev	11.54

Entry

16  
14  
12  
10  
8  
6  
4  
2  
0

ampl

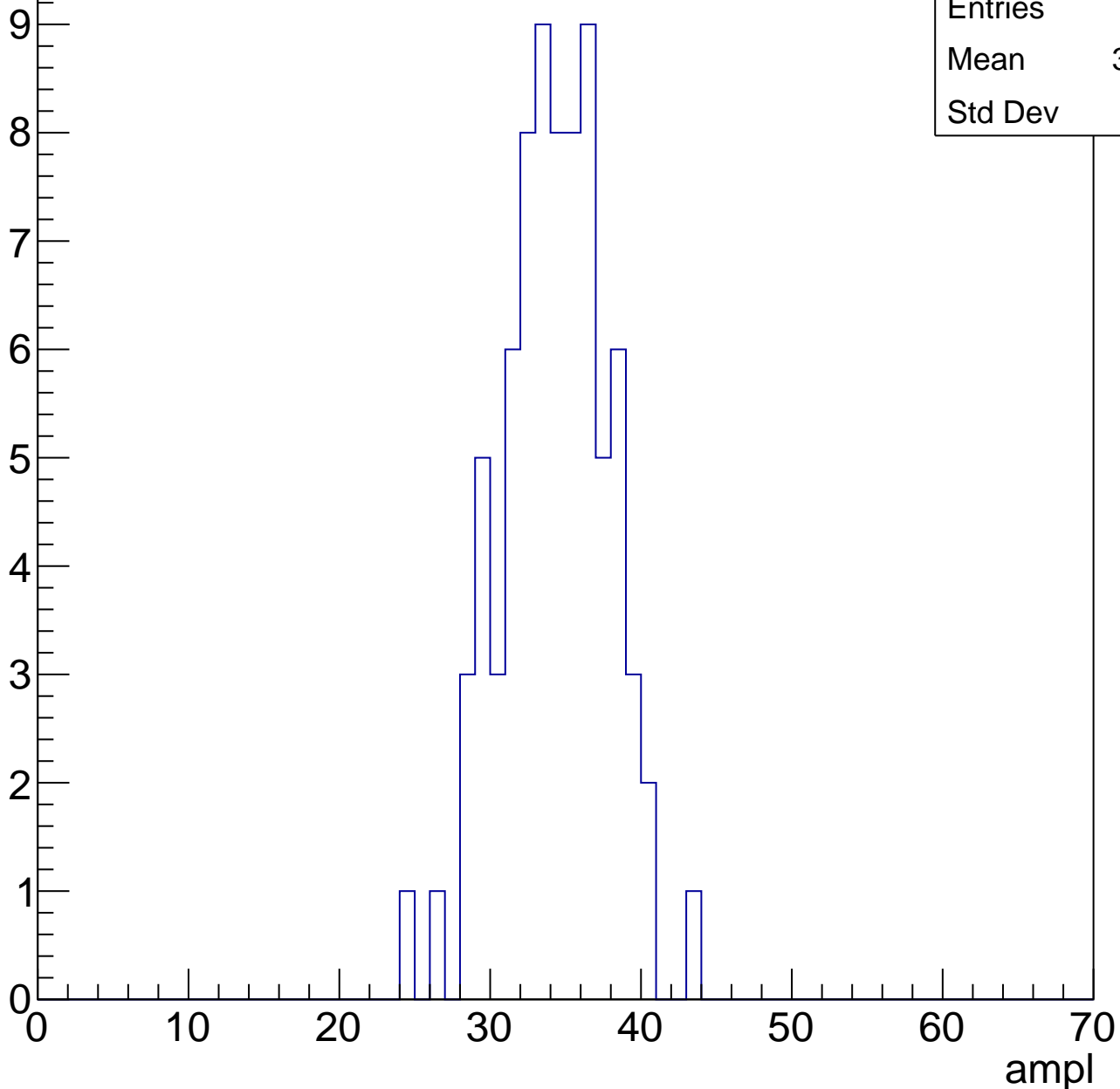


# B1L103S, U25-ch111, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	78
Mean	33.81
Std Dev	3.49

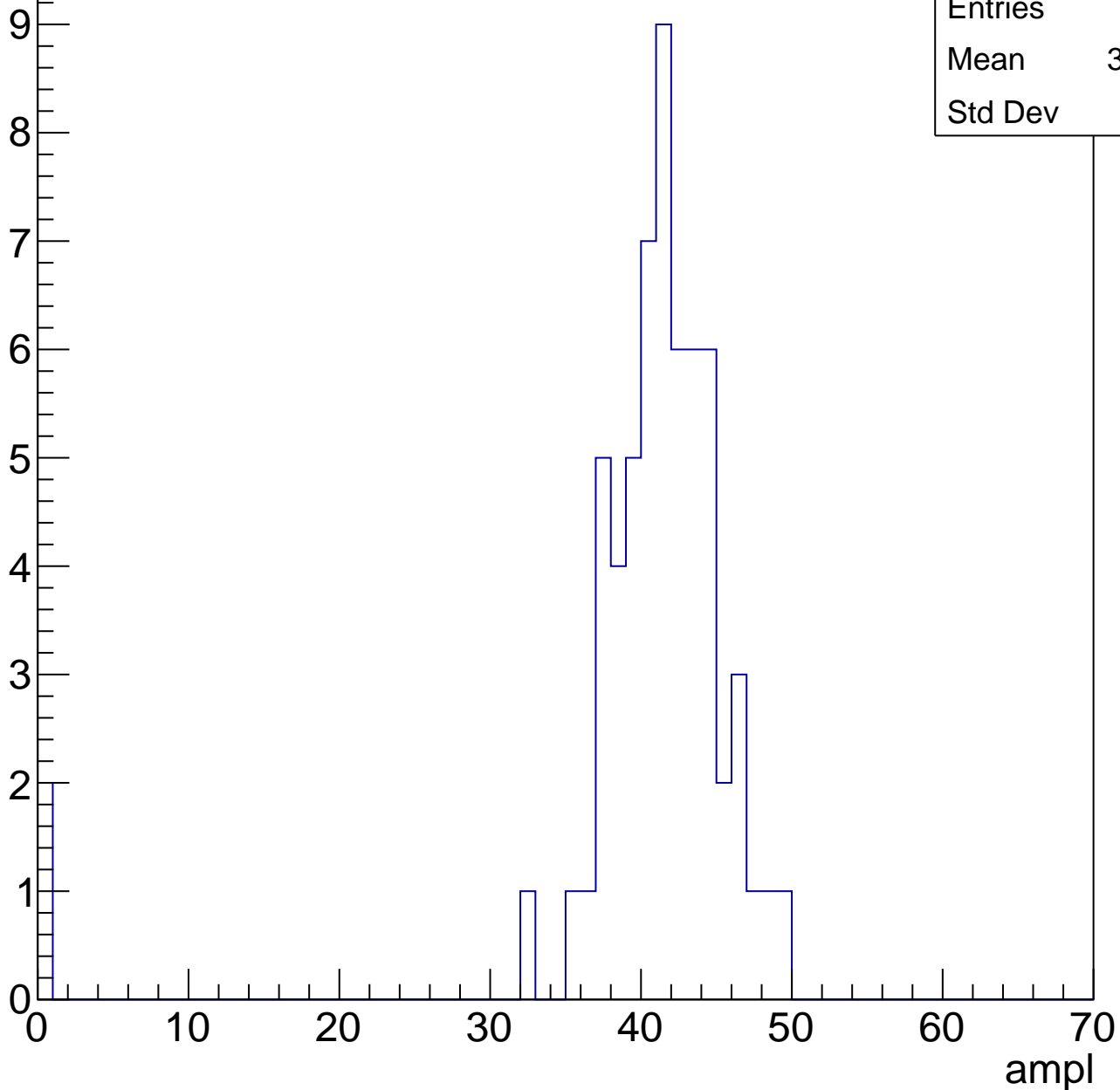


# B1L103S, U25-ch111, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	61
Mean	39.84
Std Dev	8



# B1L103S, U25-ch111, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	85
Mean	40.02
Std Dev	17.33

Entry

12

10

8

6

4

2

0

0

10

20

30

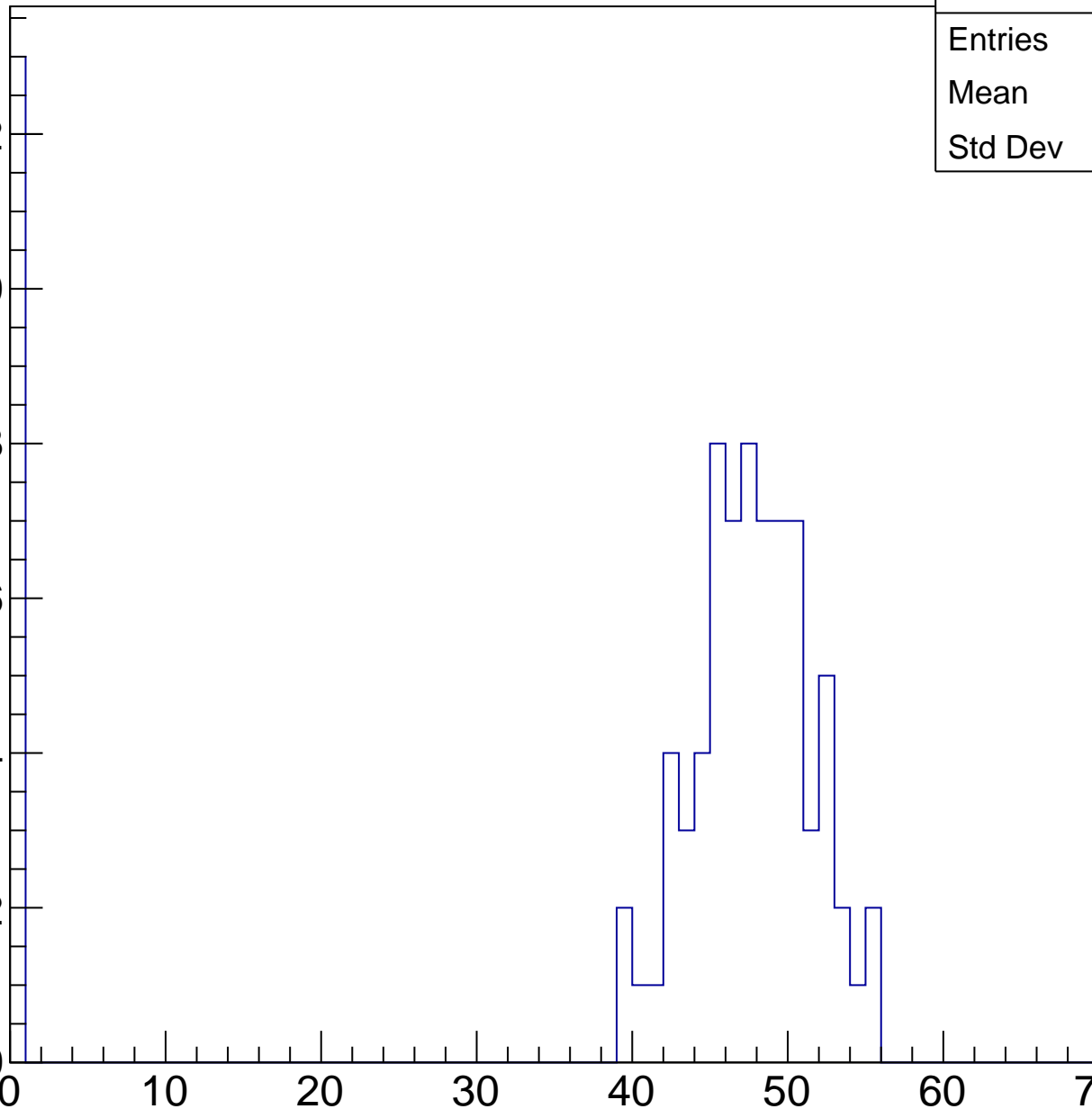
40

50

60

70

ampl

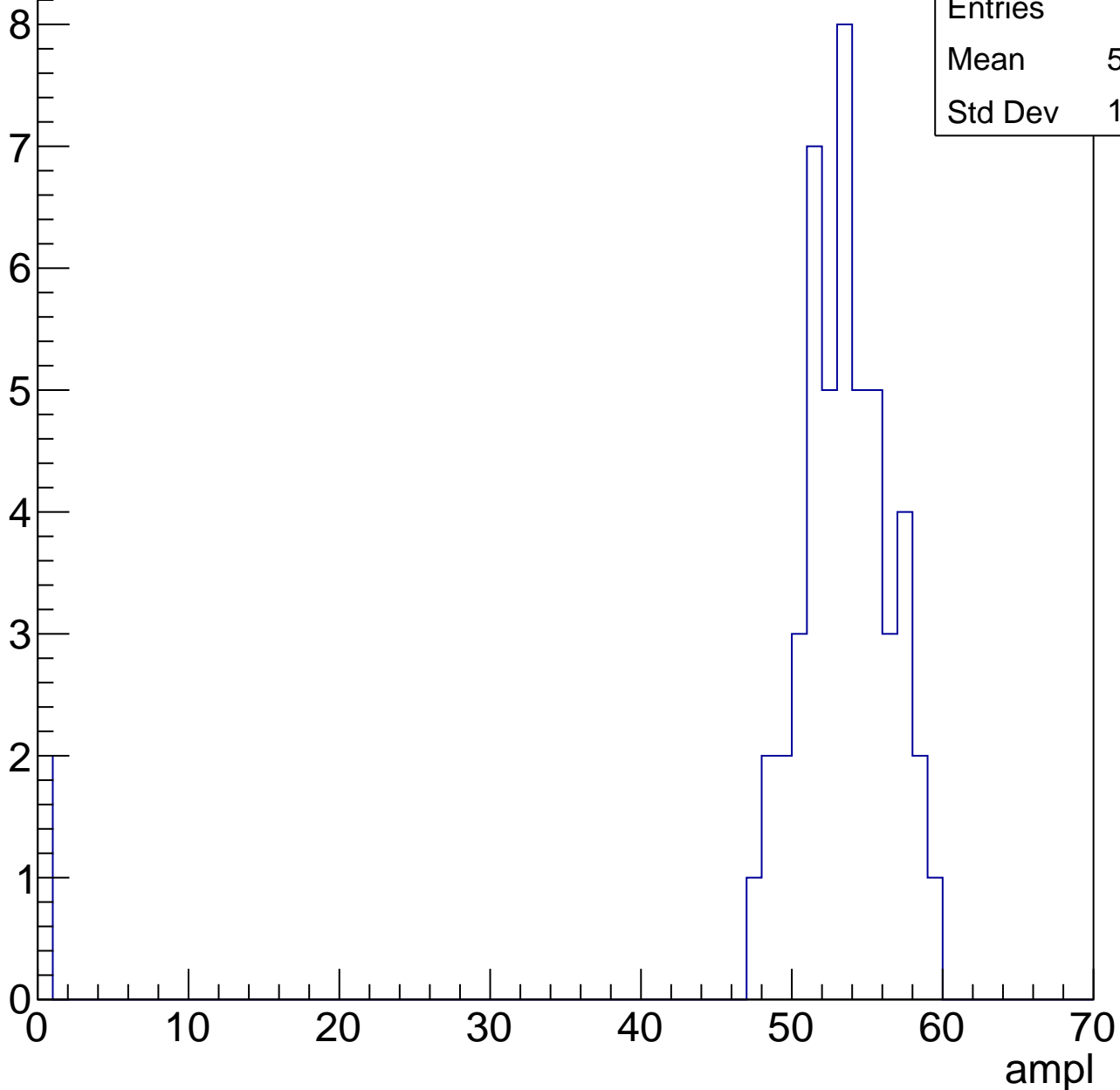


# B1L103S, U25-ch111, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

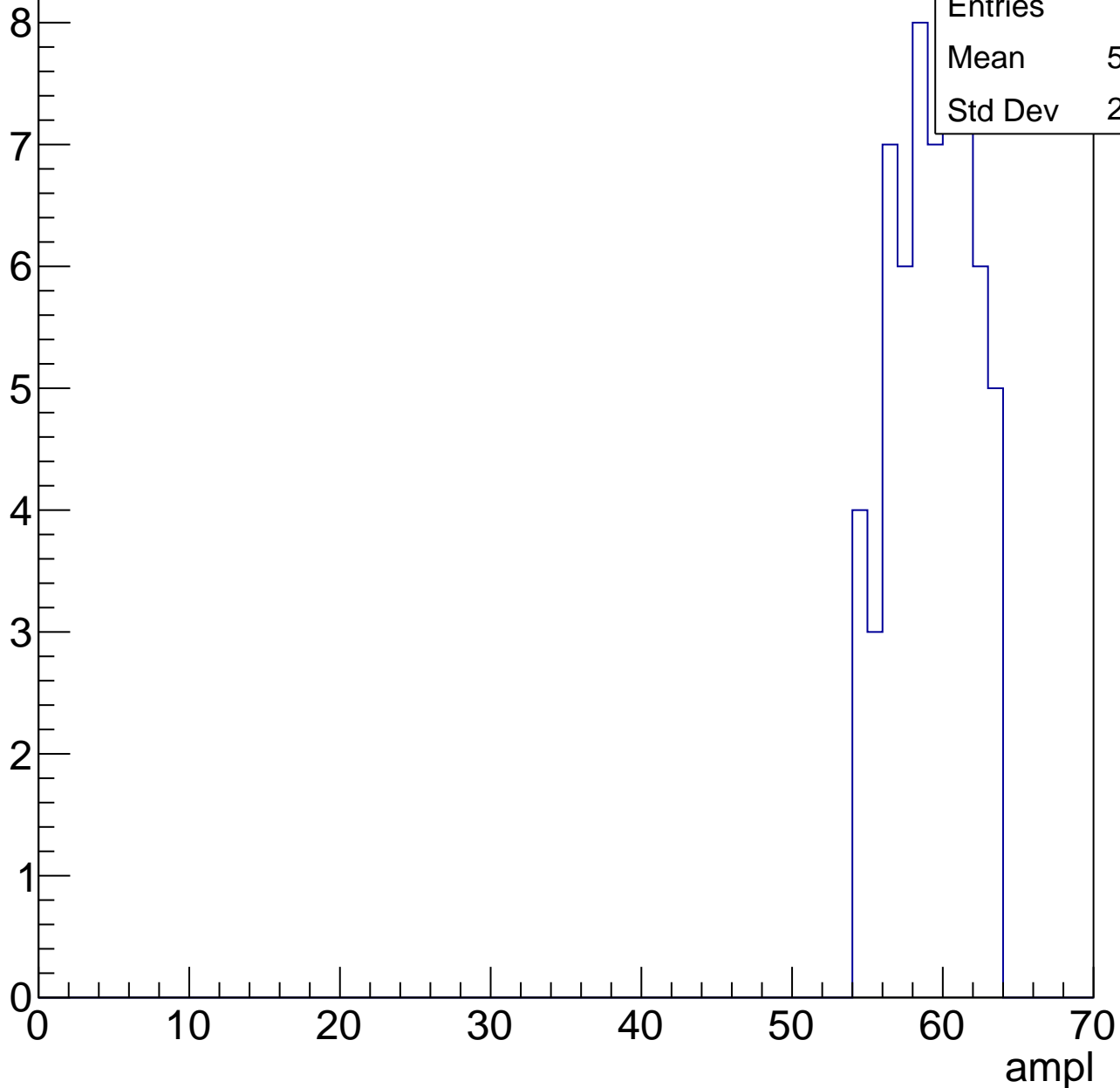
Entries	50
Mean	50.96
Std Dev	10.76



# B1L103S, U25-ch111, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

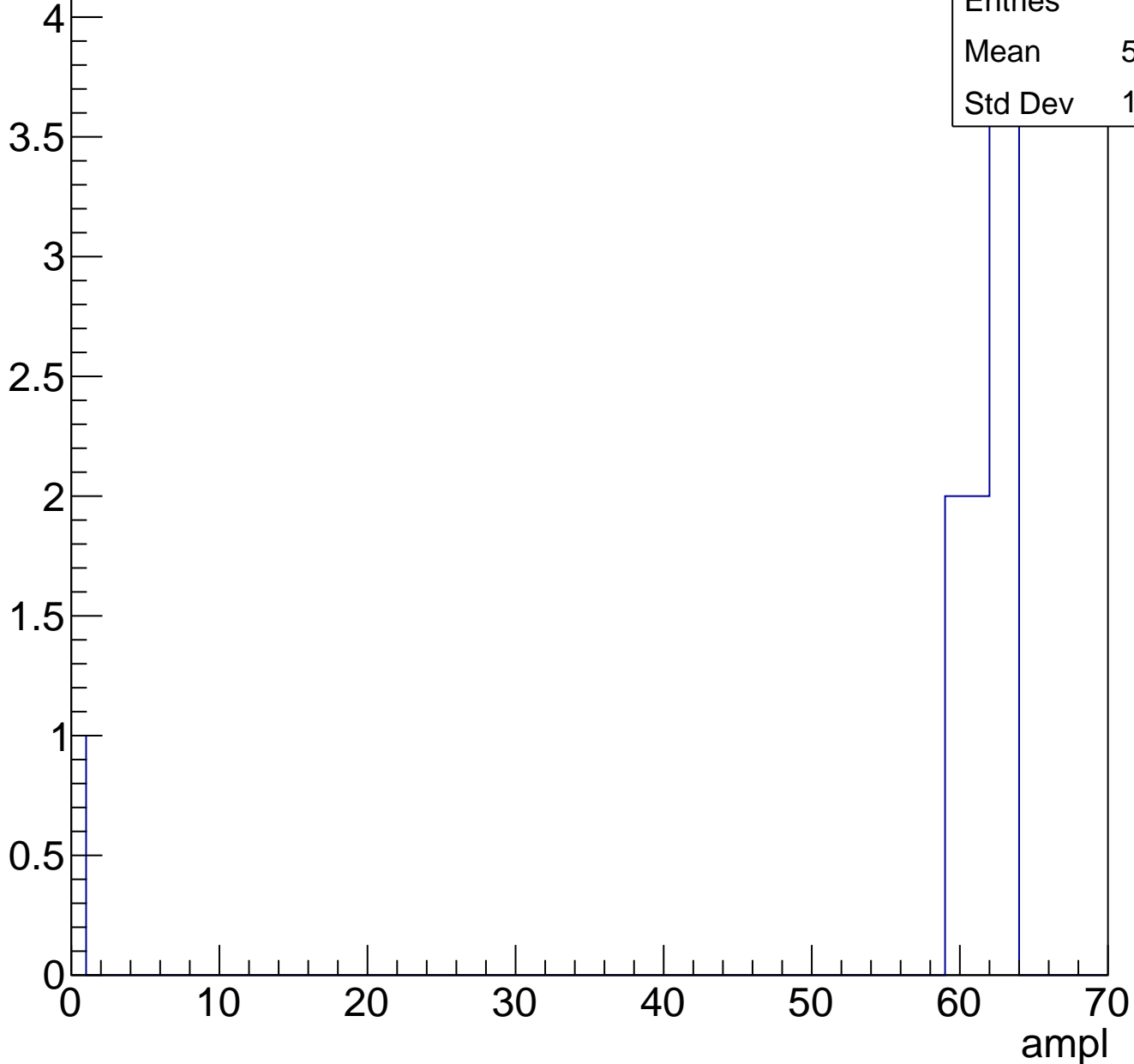
Entry



# B1L103S, U25-ch111, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

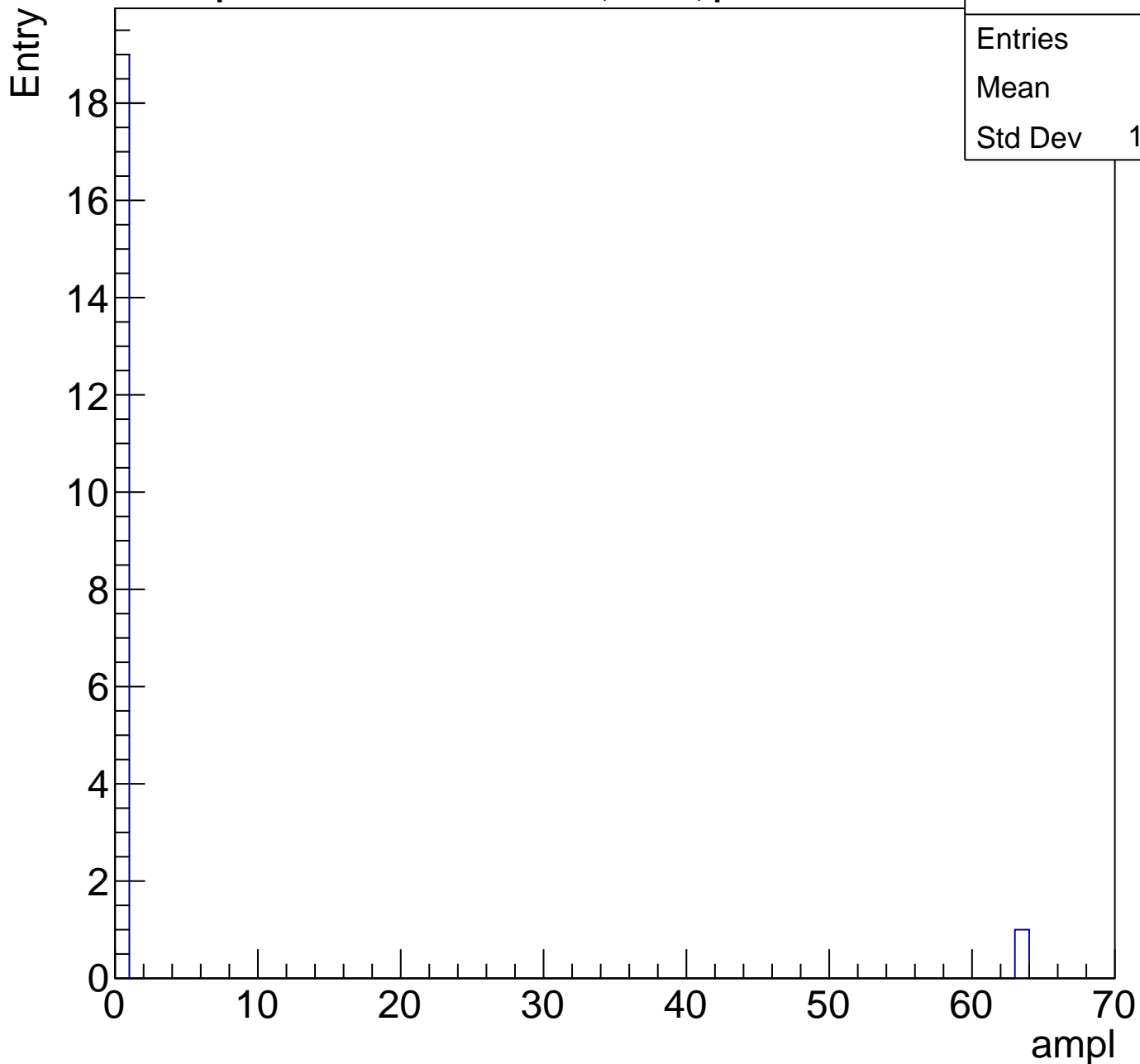




# B1L103S, U25-ch111, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	20
Mean	3.15
Std Dev	13.73



# B1L103S, U25-ch112, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

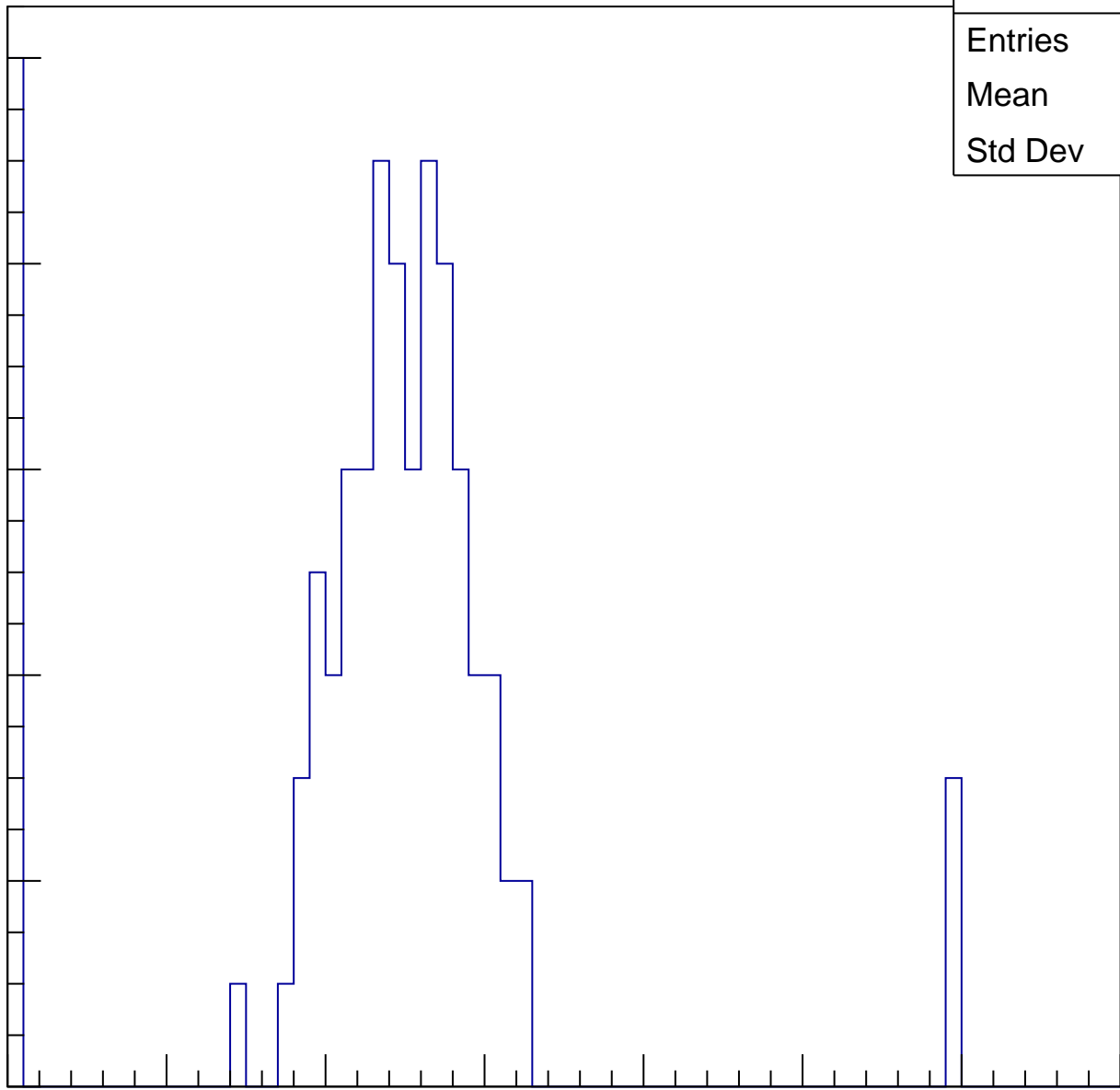
Entries	97
Mean	22.93
Std Dev	10.42

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

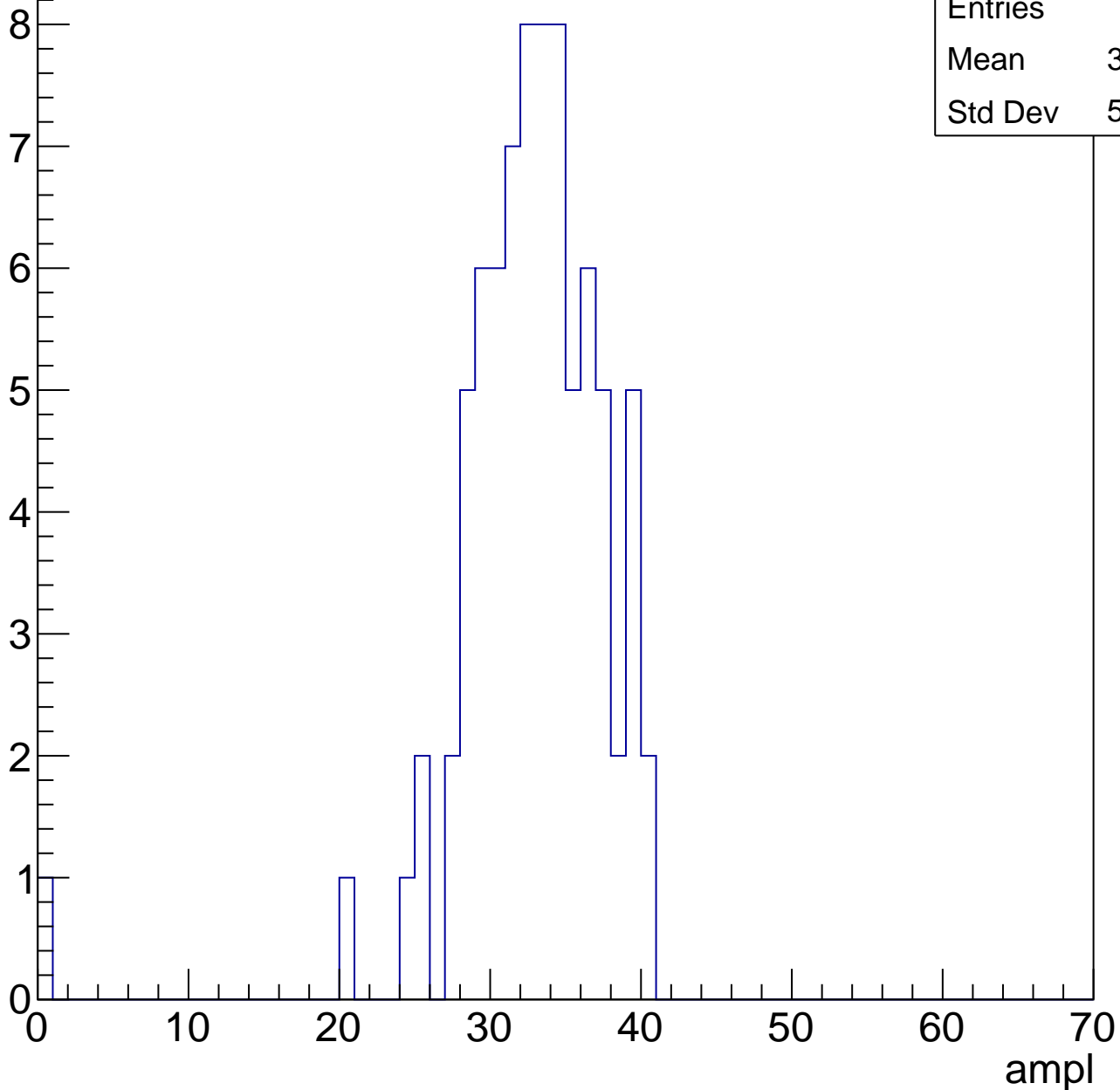


# B1L103S, U25-ch112, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	80
Mean	32.23
Std Dev	5.353

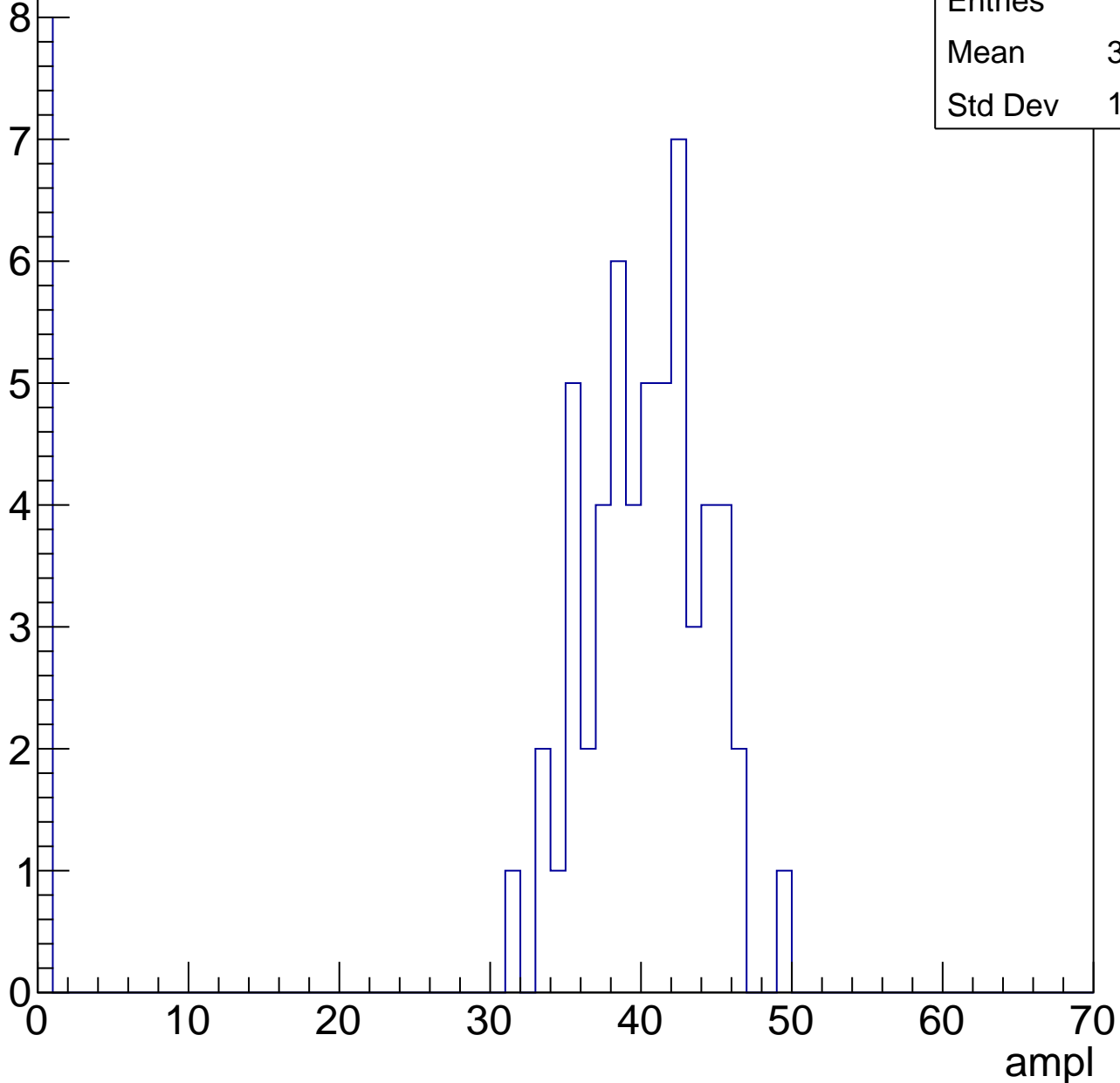


# B1L103S, U25-ch112, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	64
Mean	34.92
Std Dev	13.67

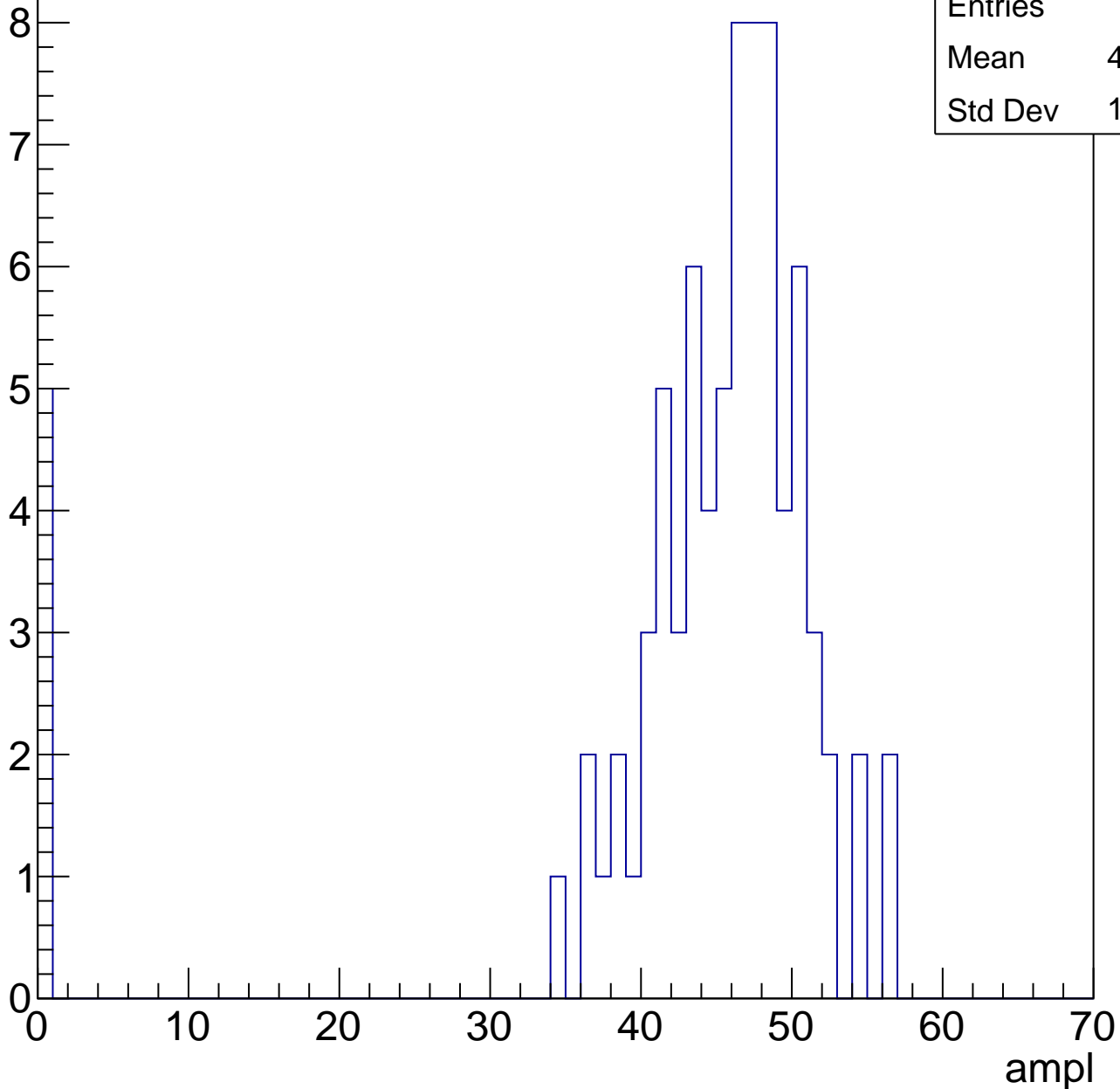


# B1L103S, U25-ch112, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	81
Mean	42.83
Std Dev	11.85

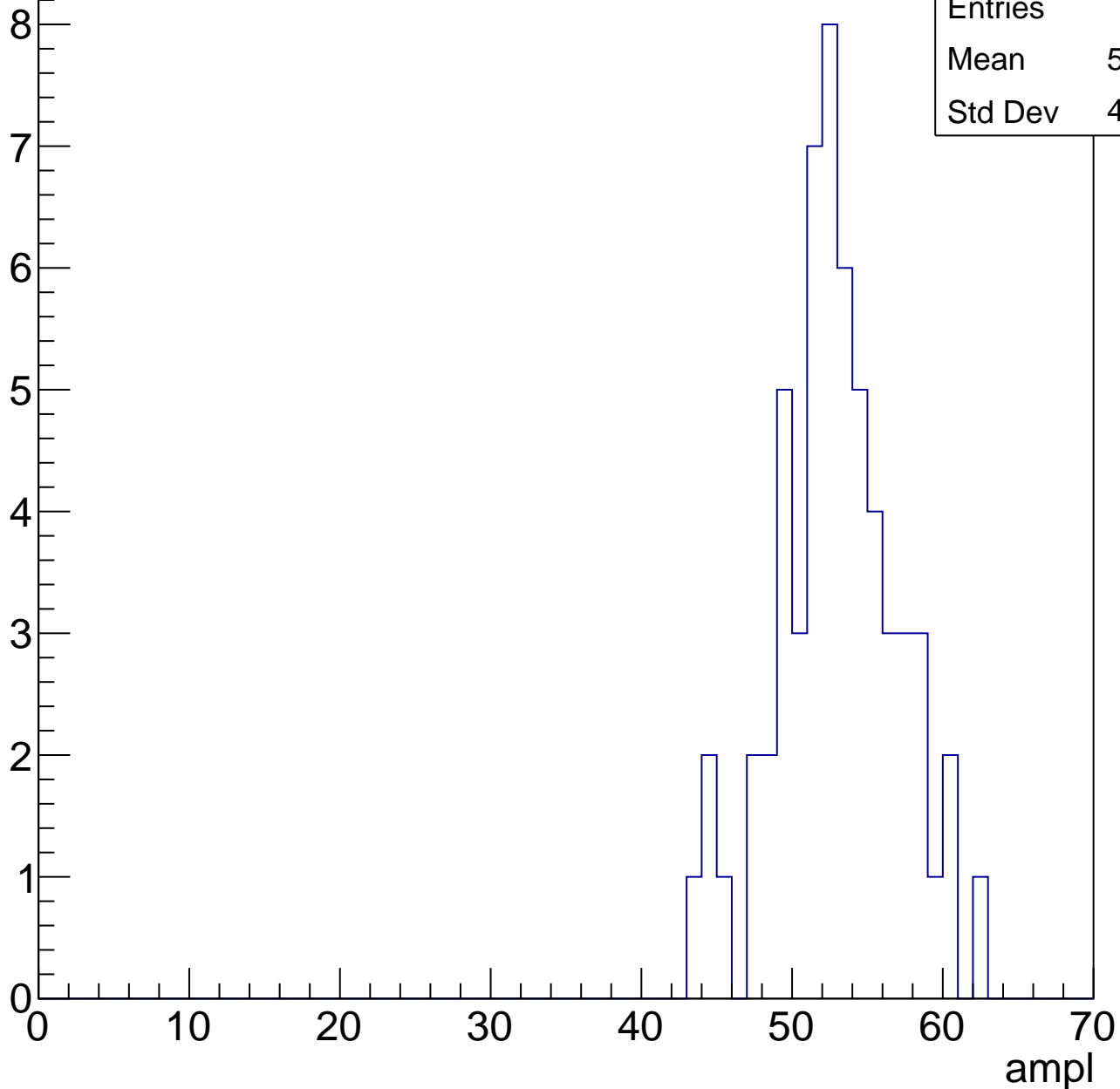


# B1L103S, U25-ch112, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	59
Mean	52.47
Std Dev	4.035

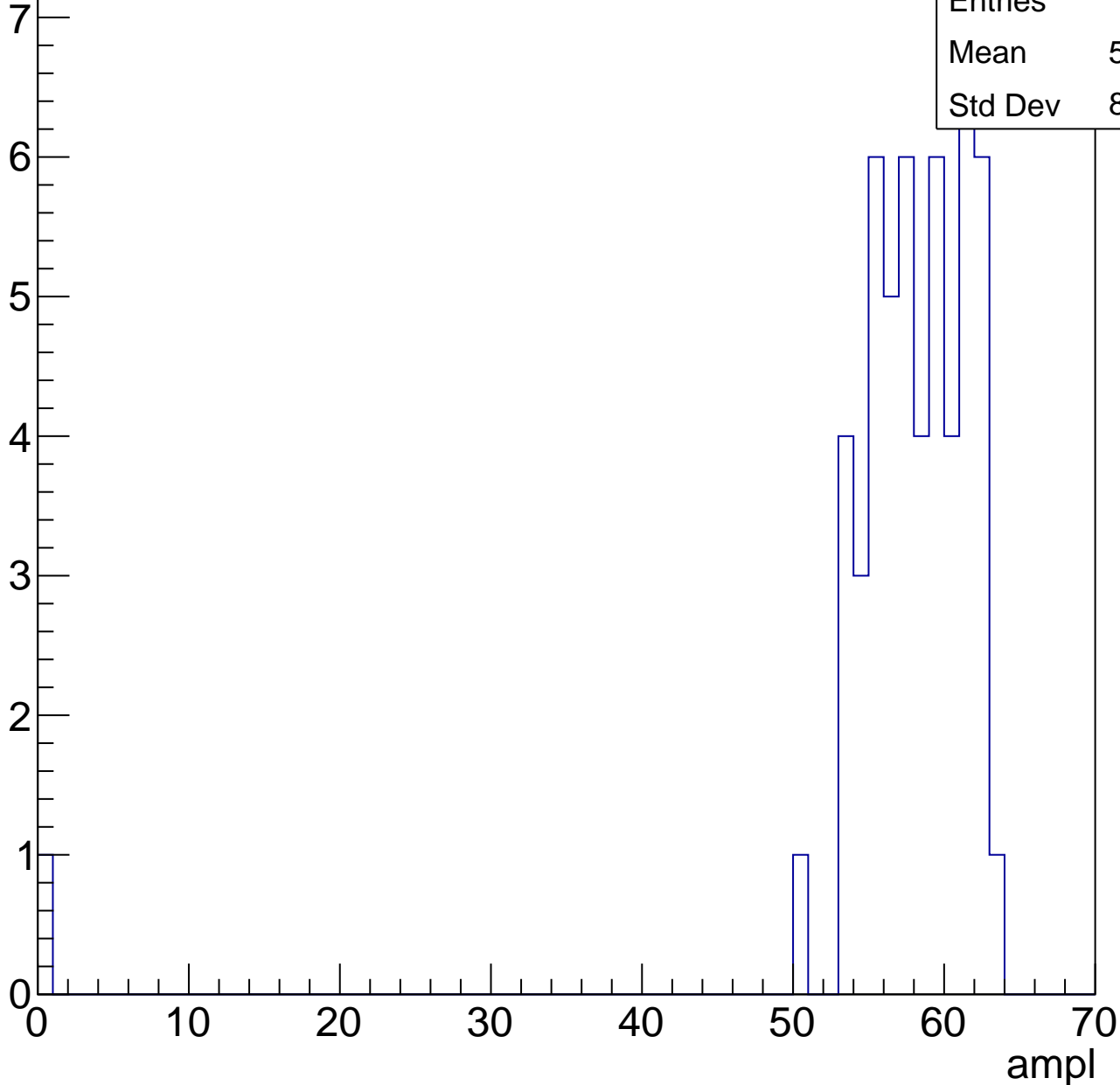


# B1L103S, U25-ch112, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	54
Mean	56.74
Std Dev	8.363

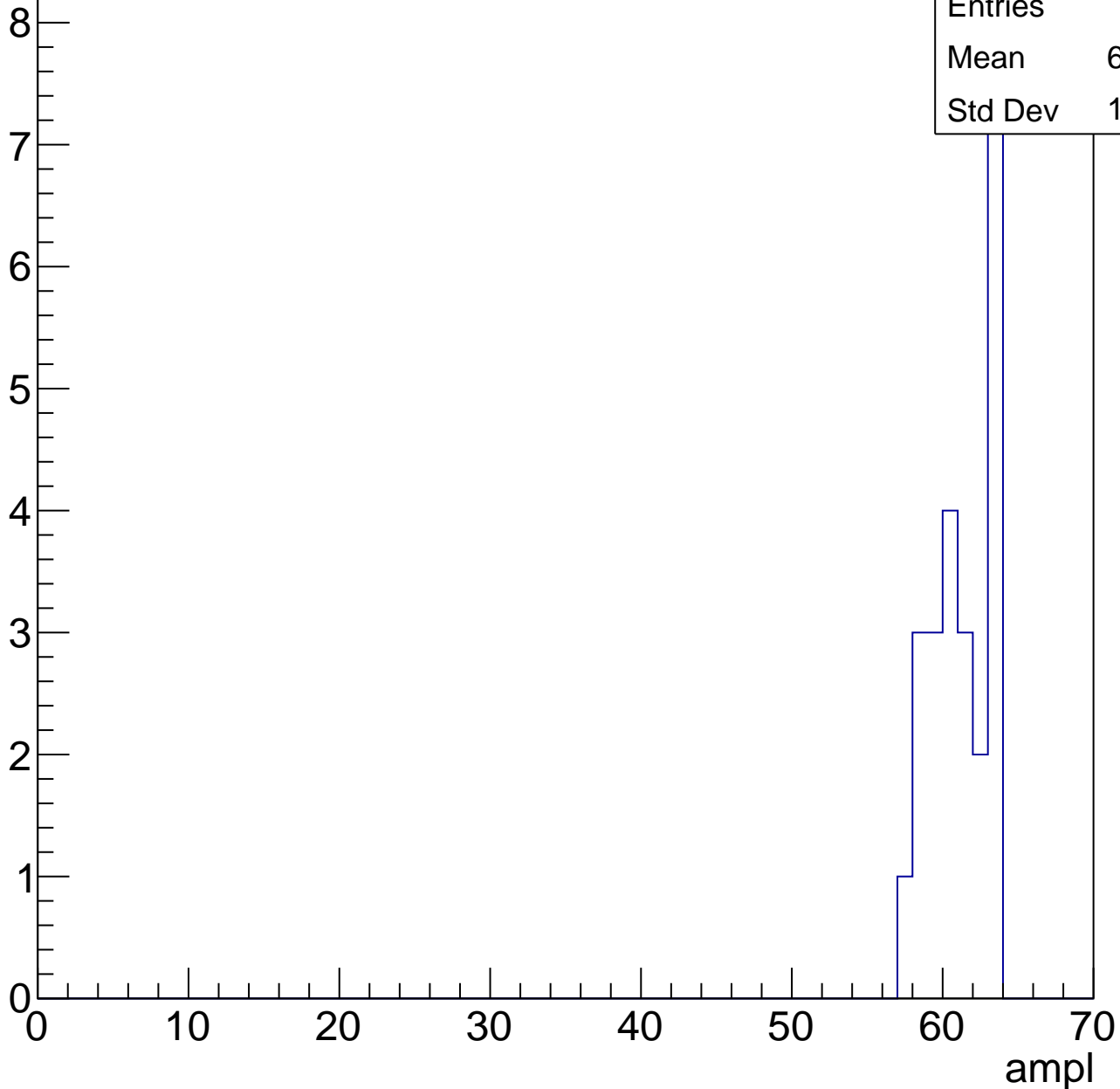


# B1L103S, U25-ch112, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	24
Mean	60.79
Std Dev	1.957

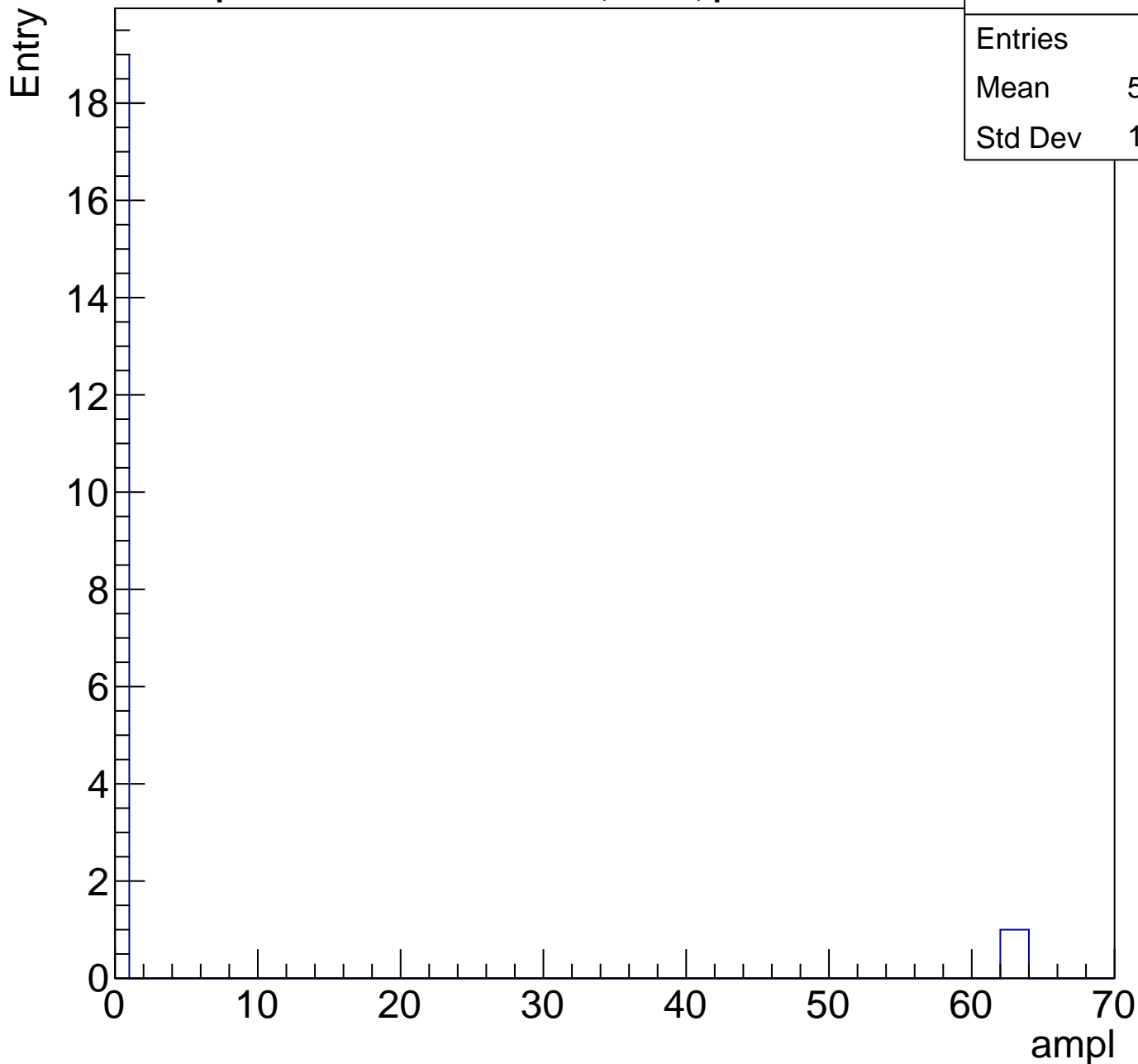




# B1L103S, U25-ch112, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

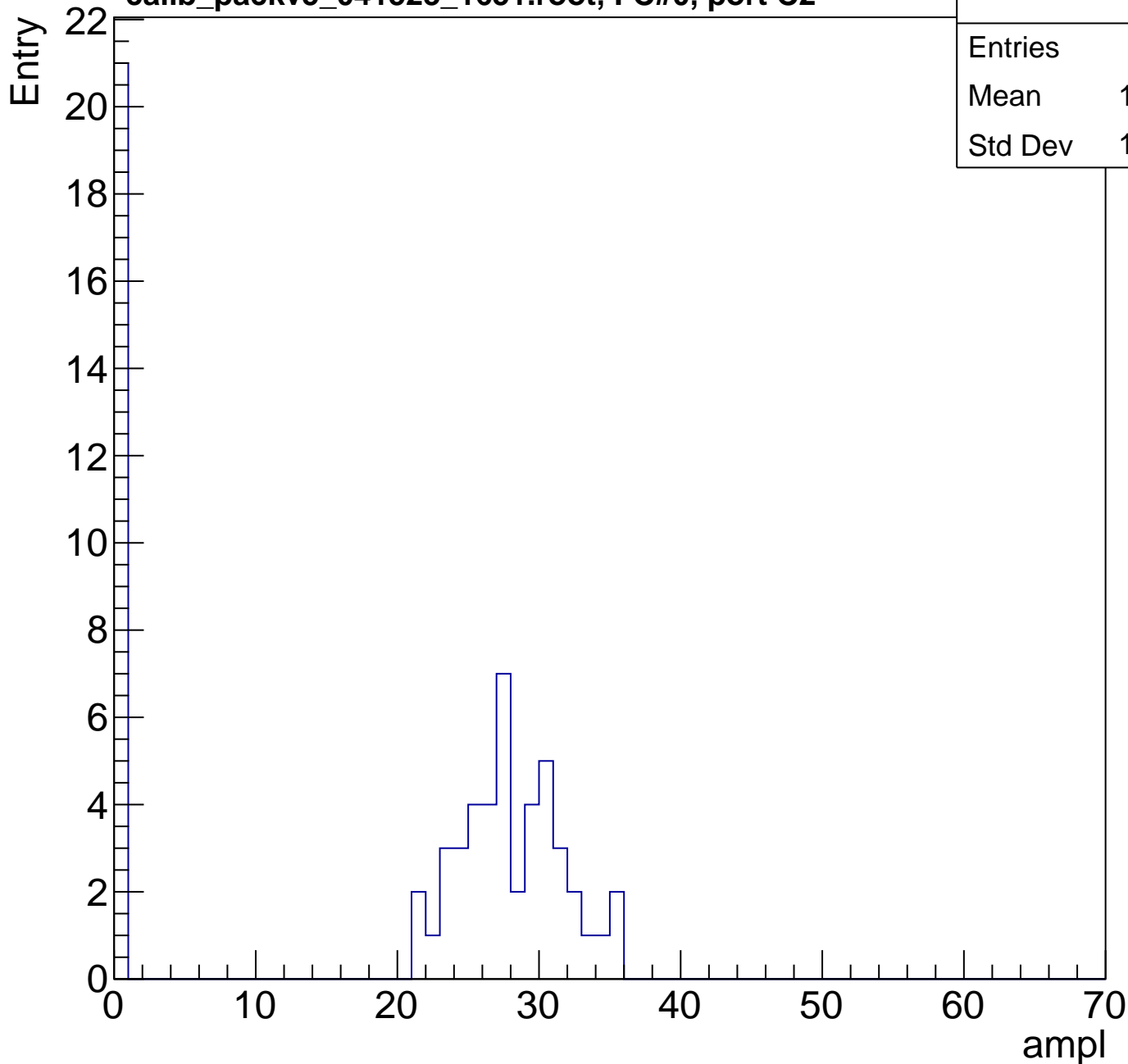
Entries	21
Mean	5.952
Std Dev	18.35



# B1L103S, U25-ch113, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	65
Mean	18.68
Std Dev	13.23

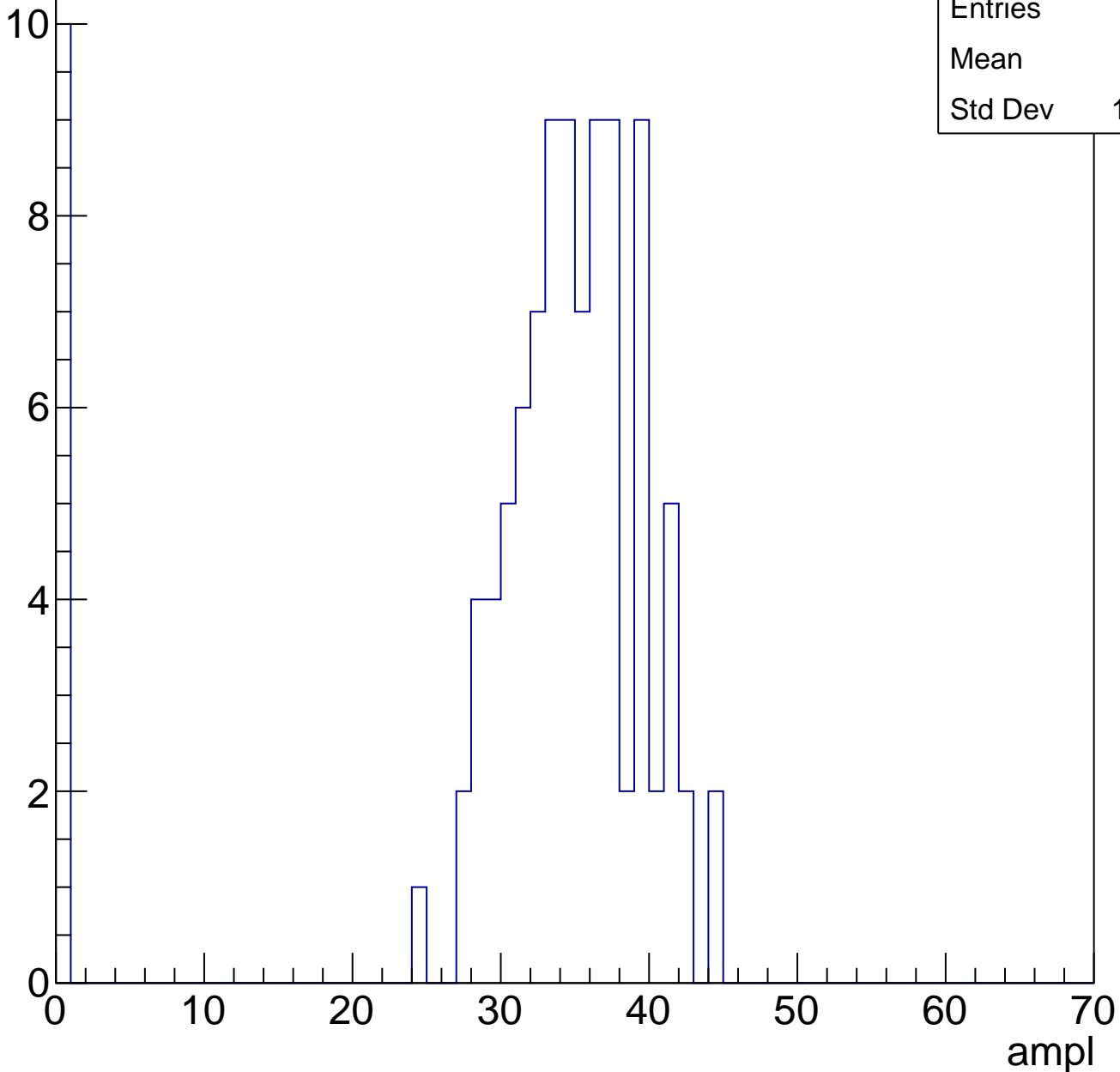


# B1L103S, U25-ch113, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	104
Mean	31.3
Std Dev	10.94

Entry

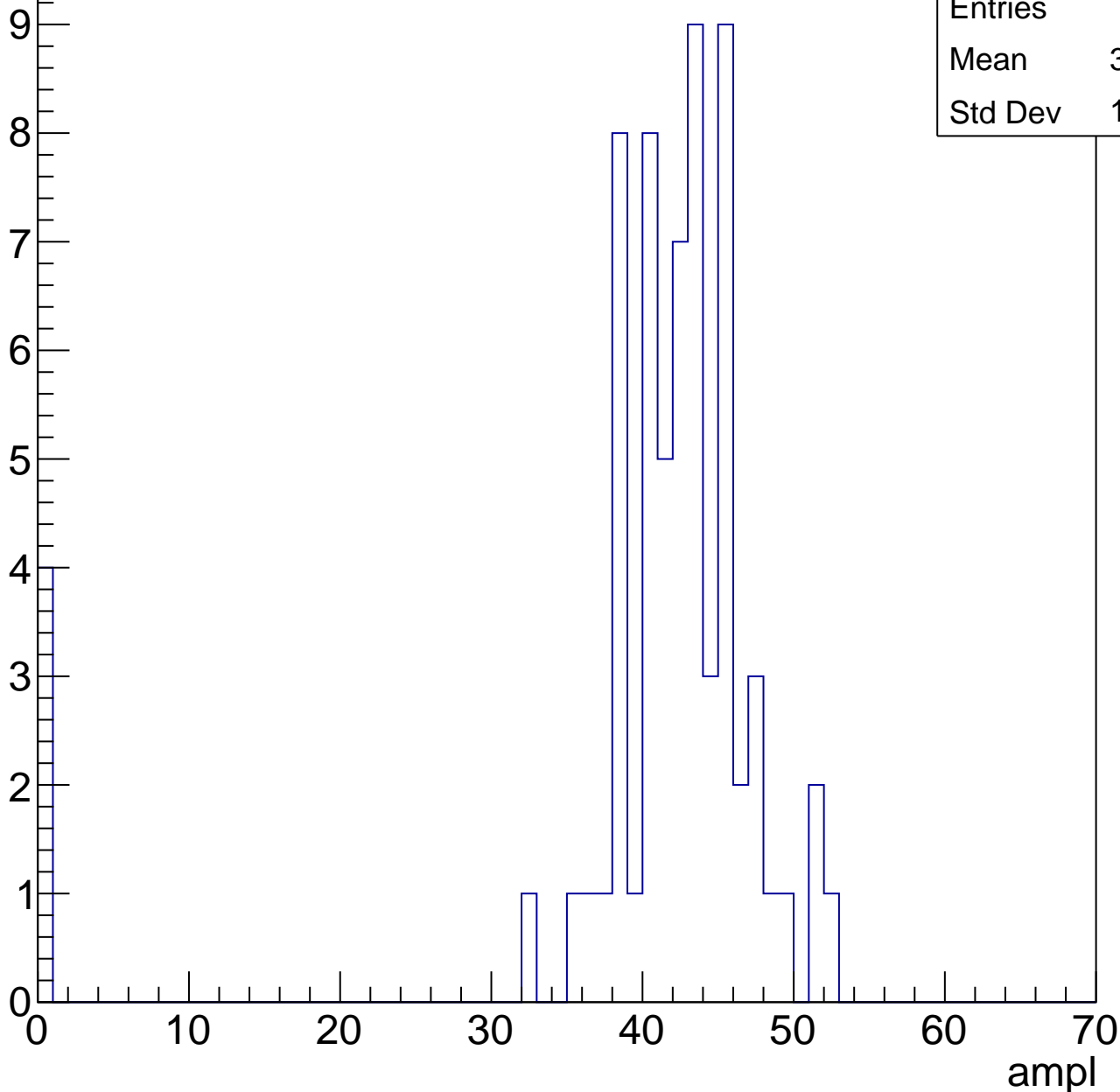


# B1L103S, U25-ch113, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	68
Mean	39.85
Std Dev	10.63

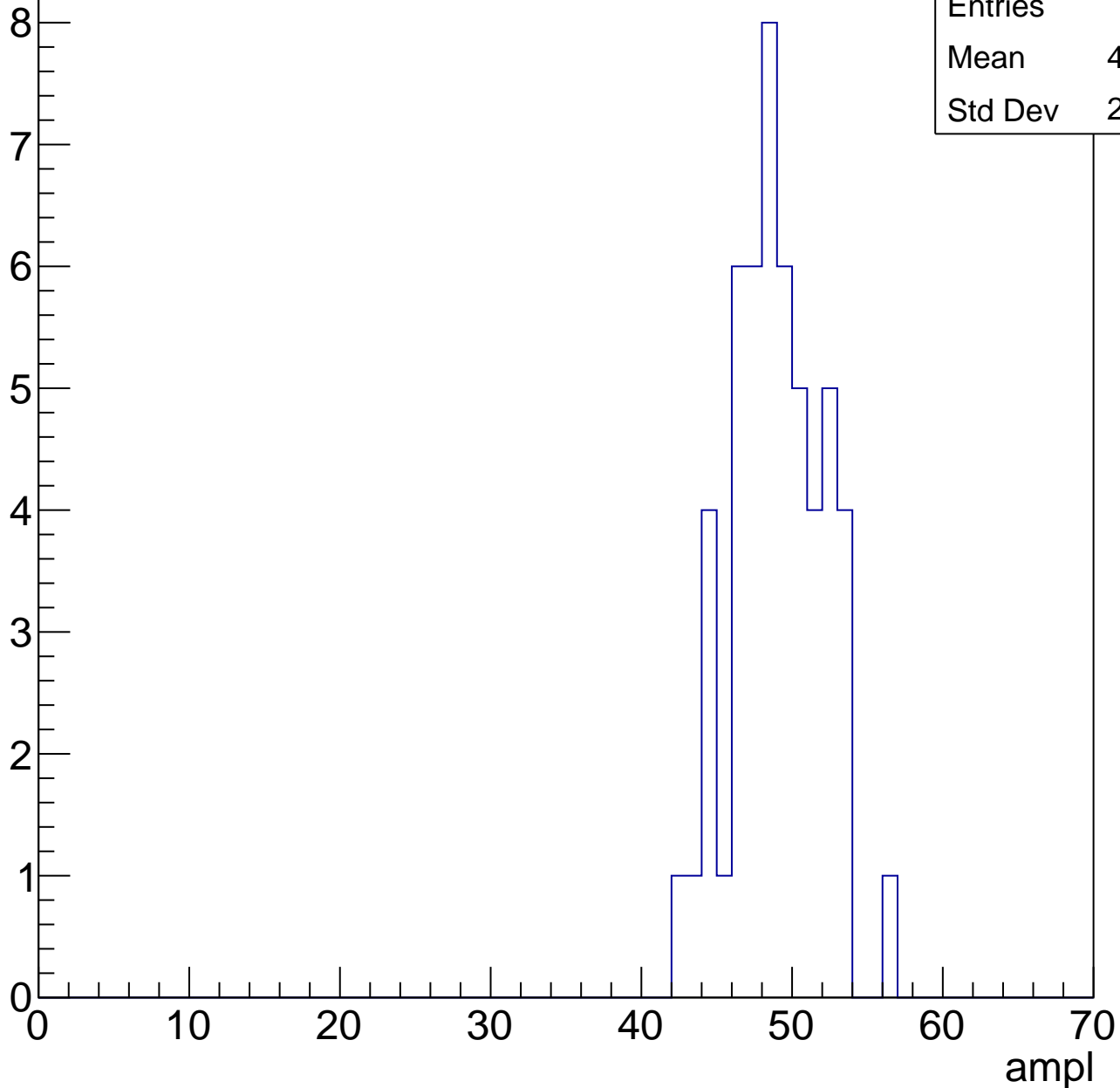


# B1L103S, U25-ch113, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	52
Mean	48.54
Std Dev	2.958

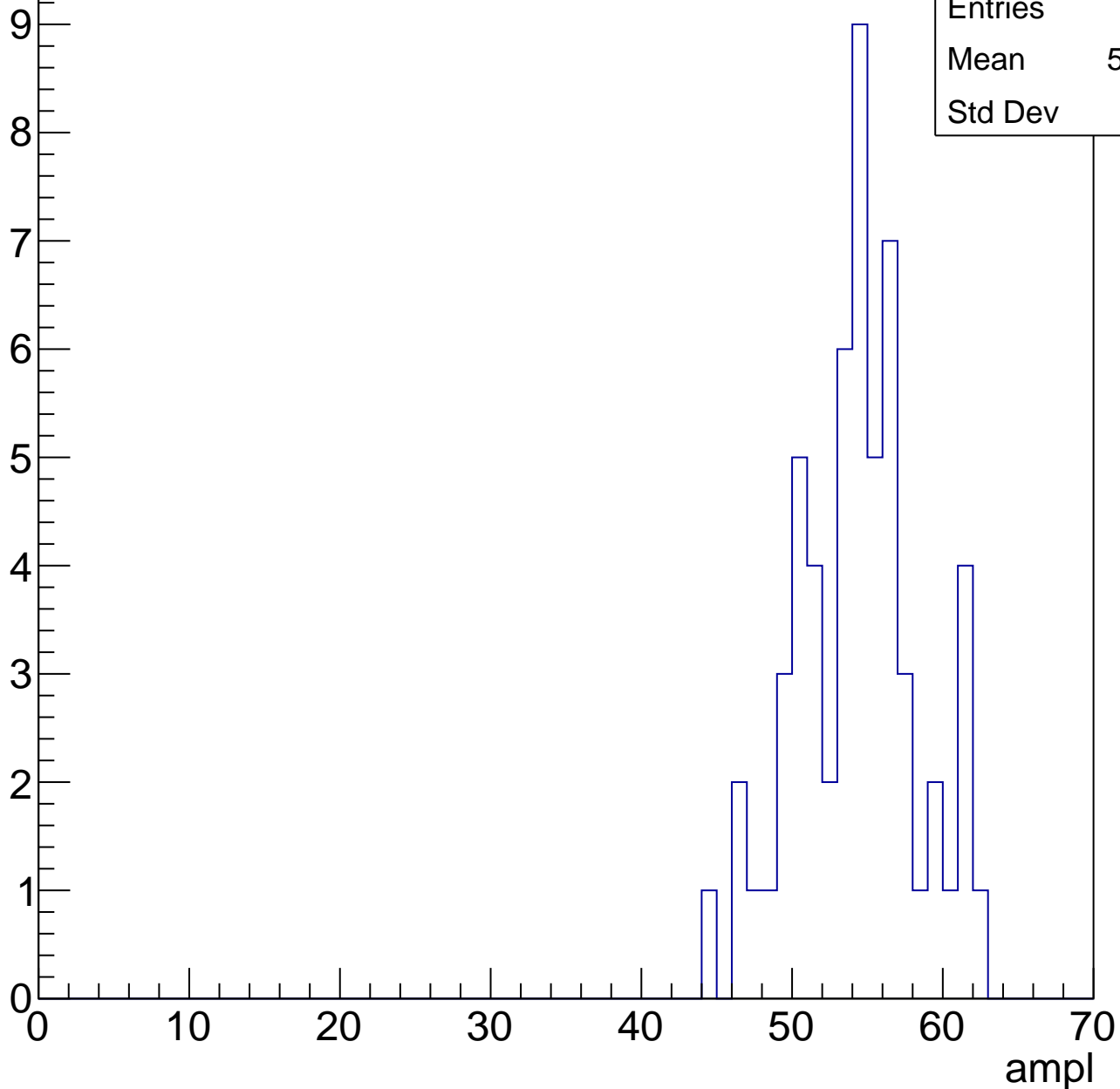


# B1L103S, U25-ch113, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	58
Mean	53.79
Std Dev	4.02

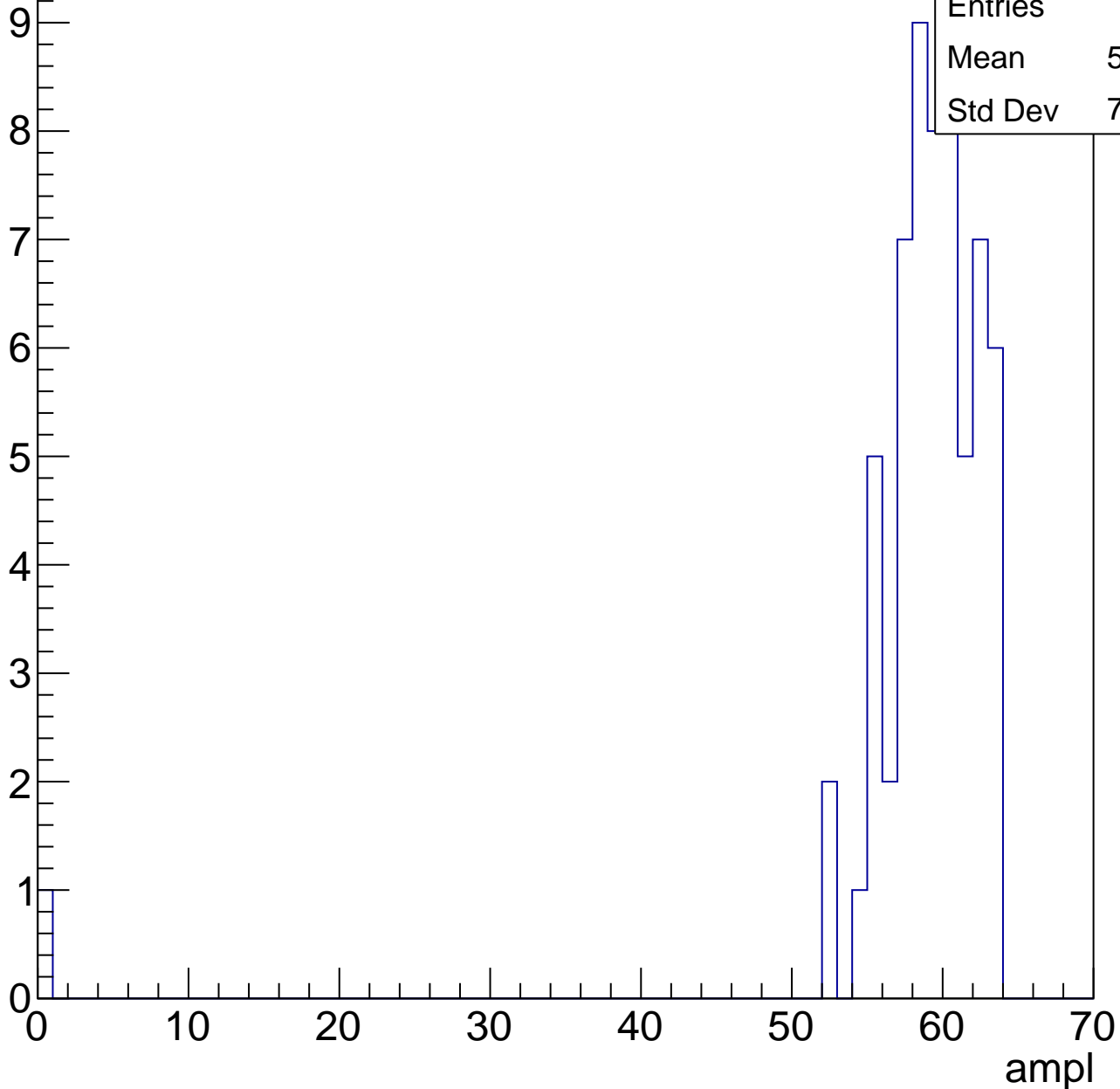


# B1L103S, U25-ch113, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	61
Mean	57.95
Std Dev	7.954



# B1L103S, U25-ch113, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U25-ch113, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

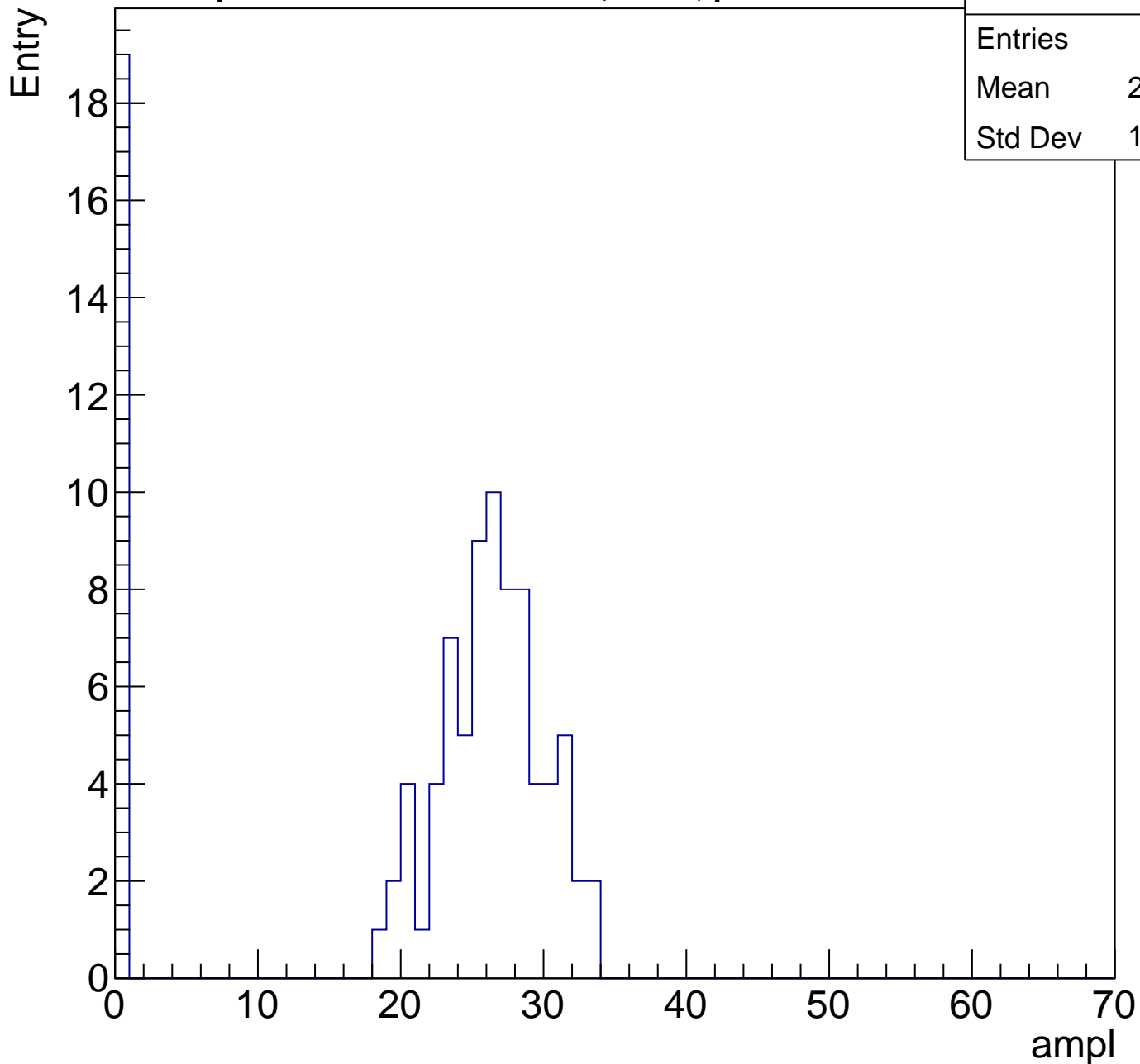
Entries	19
Mean	0
Std Dev	0

ampl

# B1L103S, U25-ch114, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	95
Mean	20.76
Std Dev	10.84

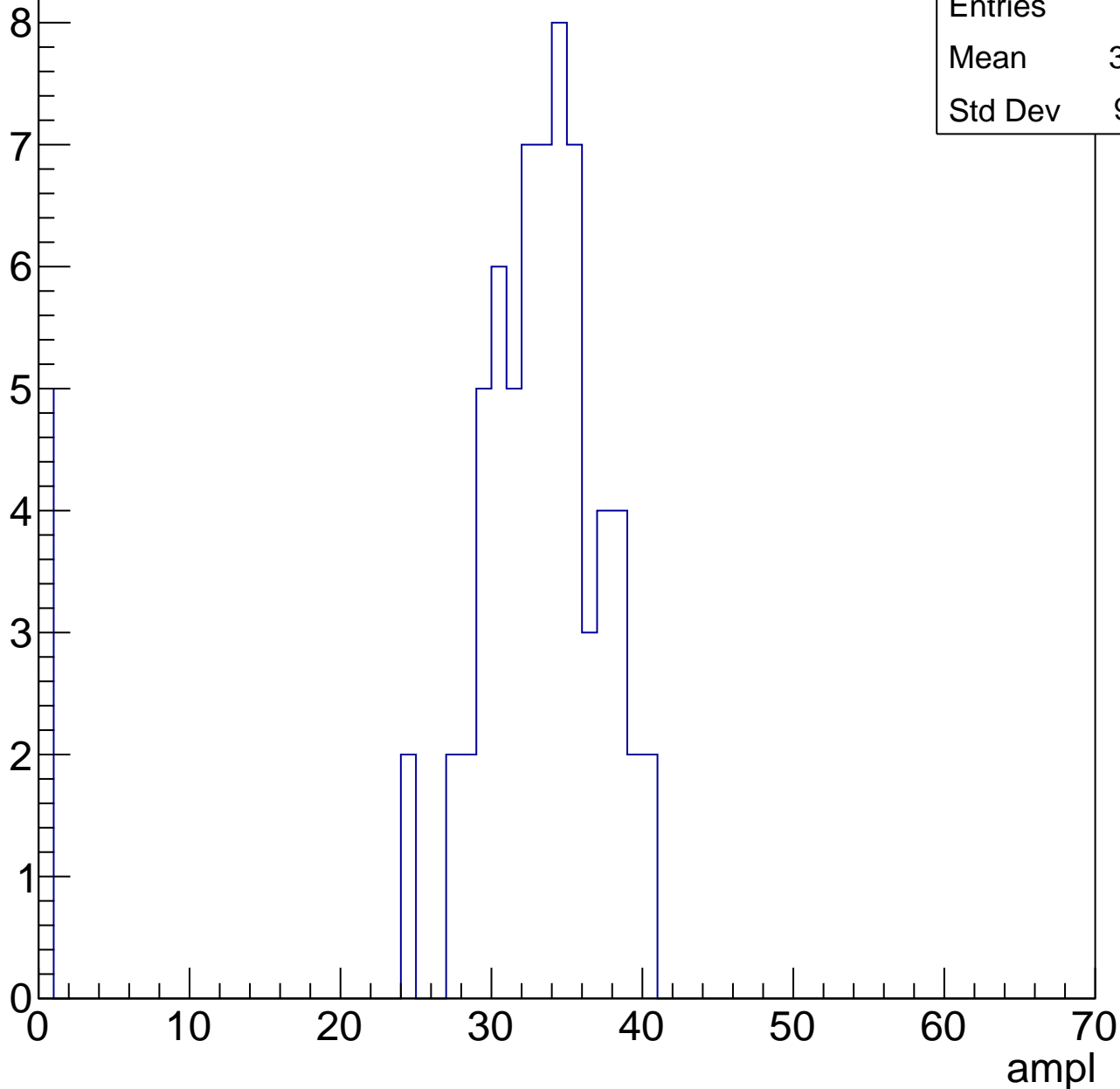


# B1L103S, U25-ch114, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

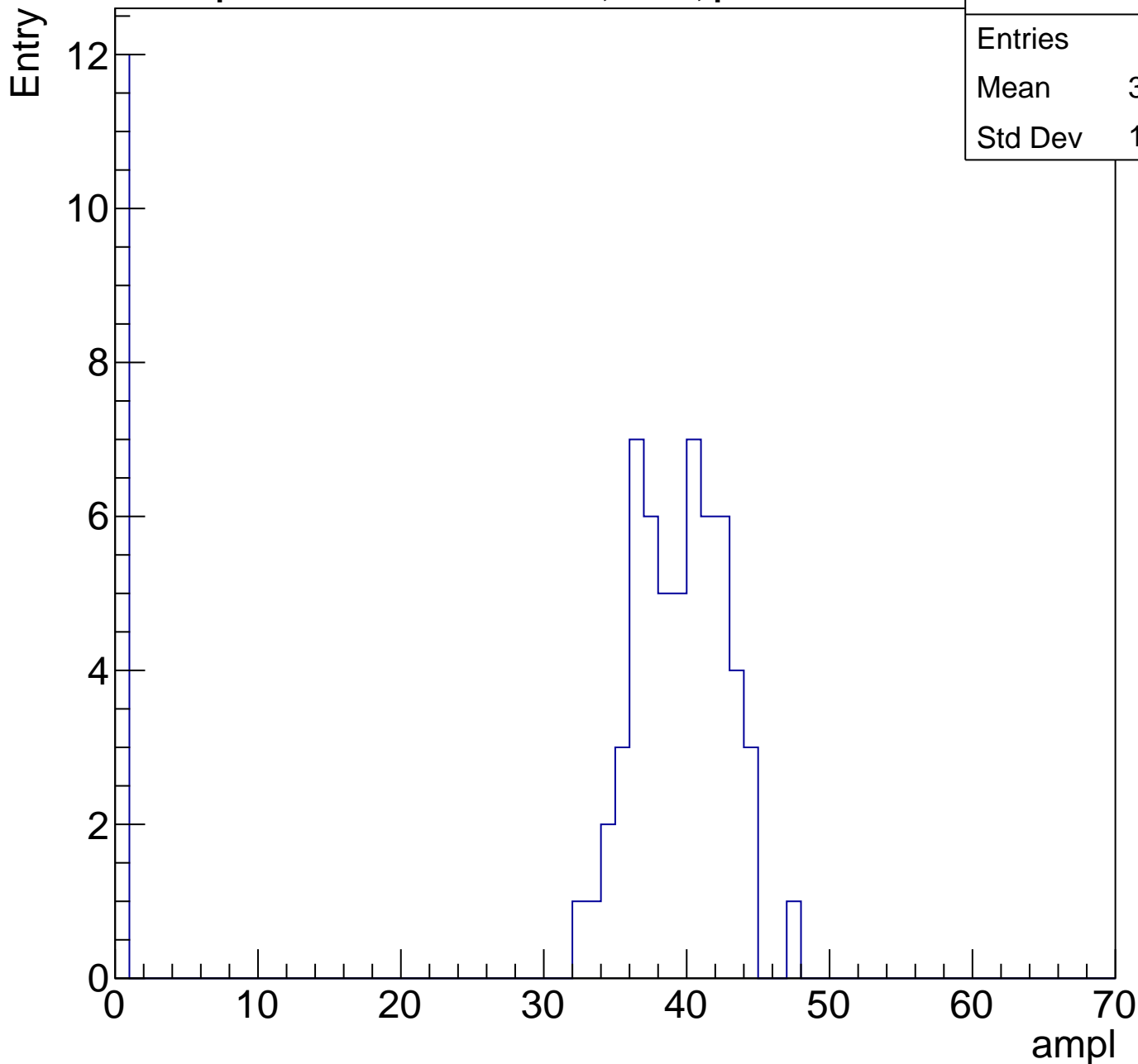
Entries	71
Mean	30.65
Std Dev	9.111



# B1L103S, U25-ch114, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

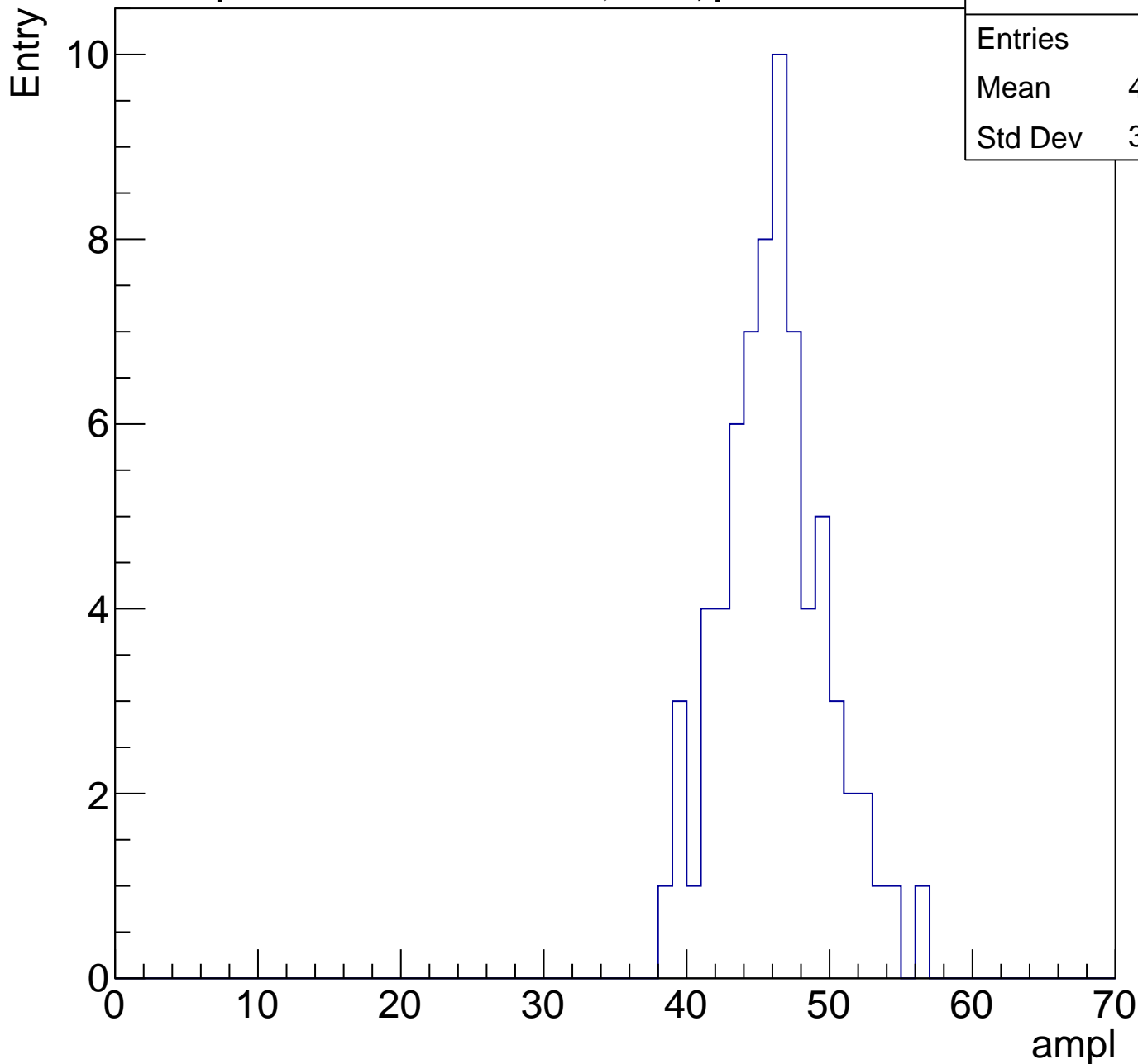
Entries	69
Mean	32.26
Std Dev	15.08



# B1L103S, U25-ch114, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	70
Mean	45.69
Std Dev	3.674

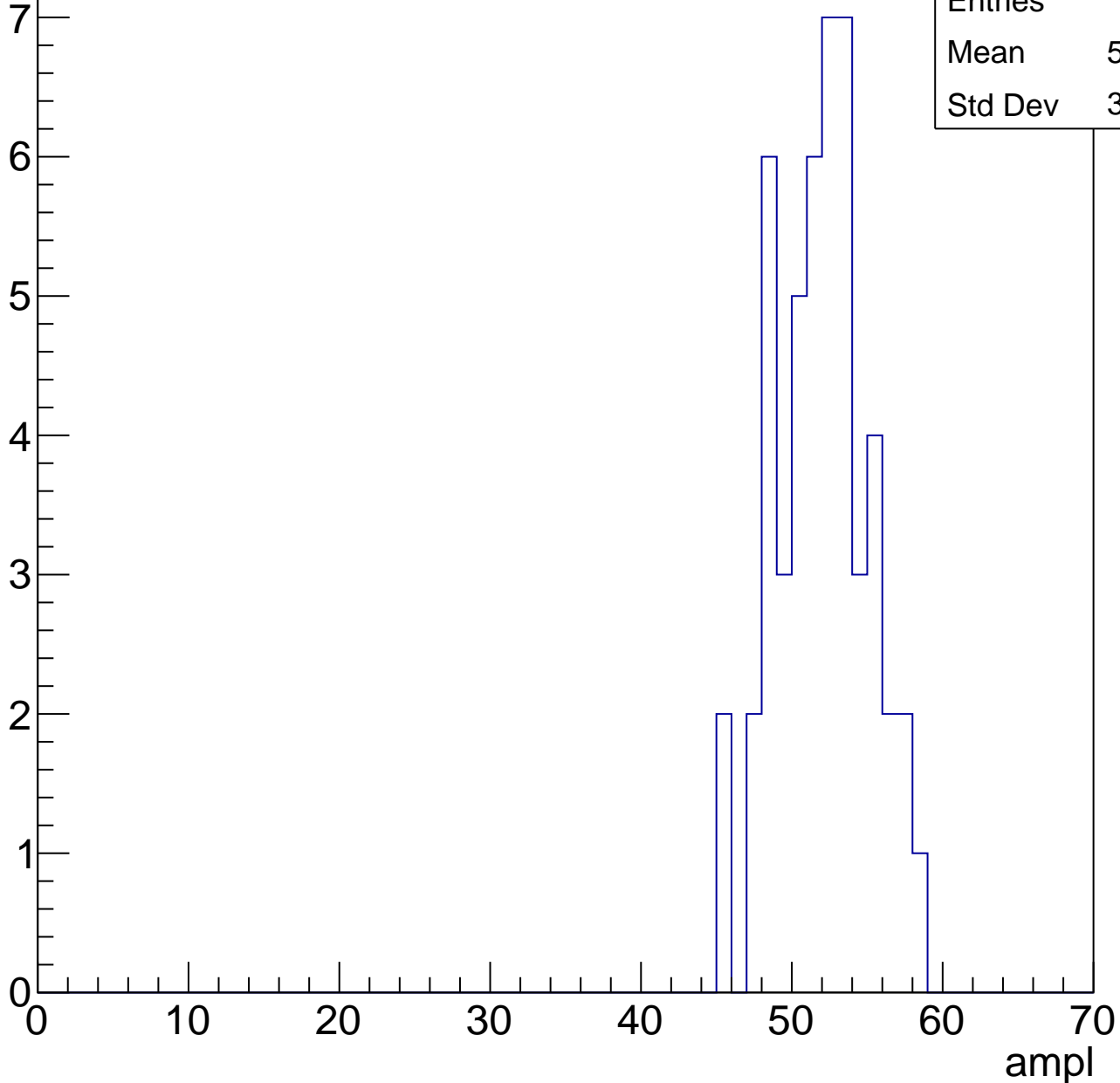


# B1L103S, U25-ch114, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	50
Mean	51.52
Std Dev	3.028

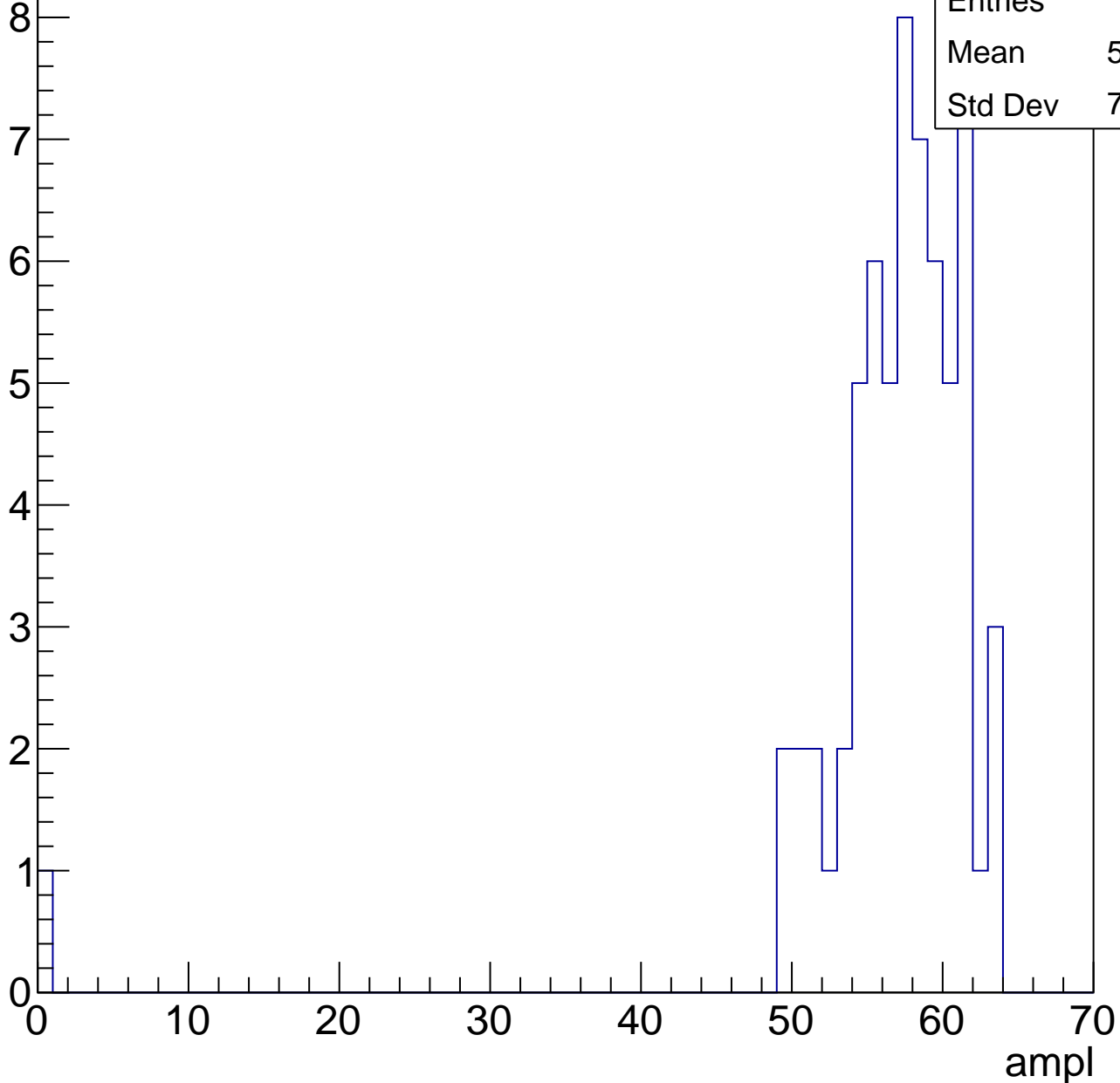


# B1L103S, U25-ch114, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	64
Mean	56.14
Std Dev	7.874

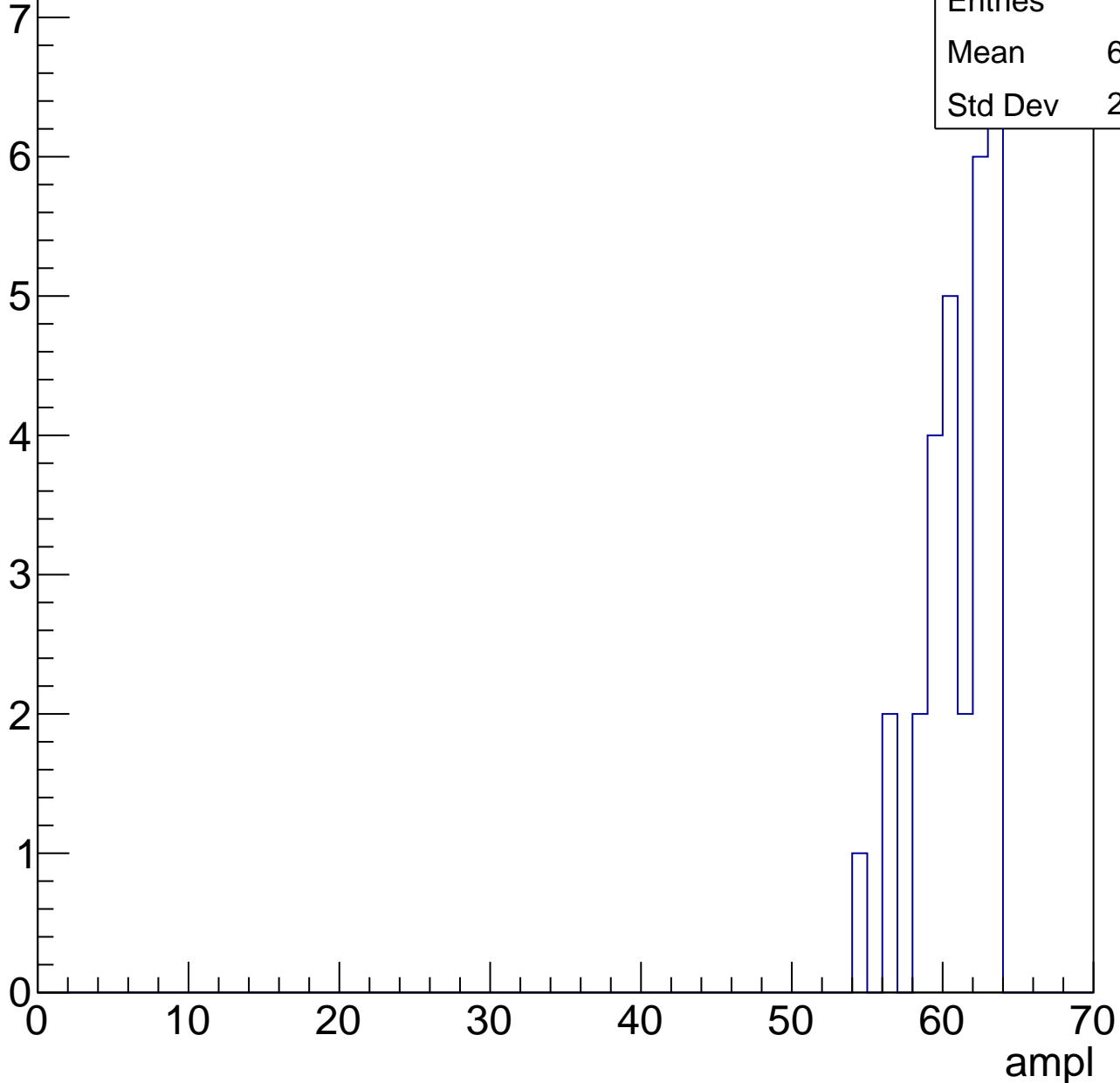


# B1L103S, U25-ch114, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	29
Mean	60.45
Std Dev	2.372



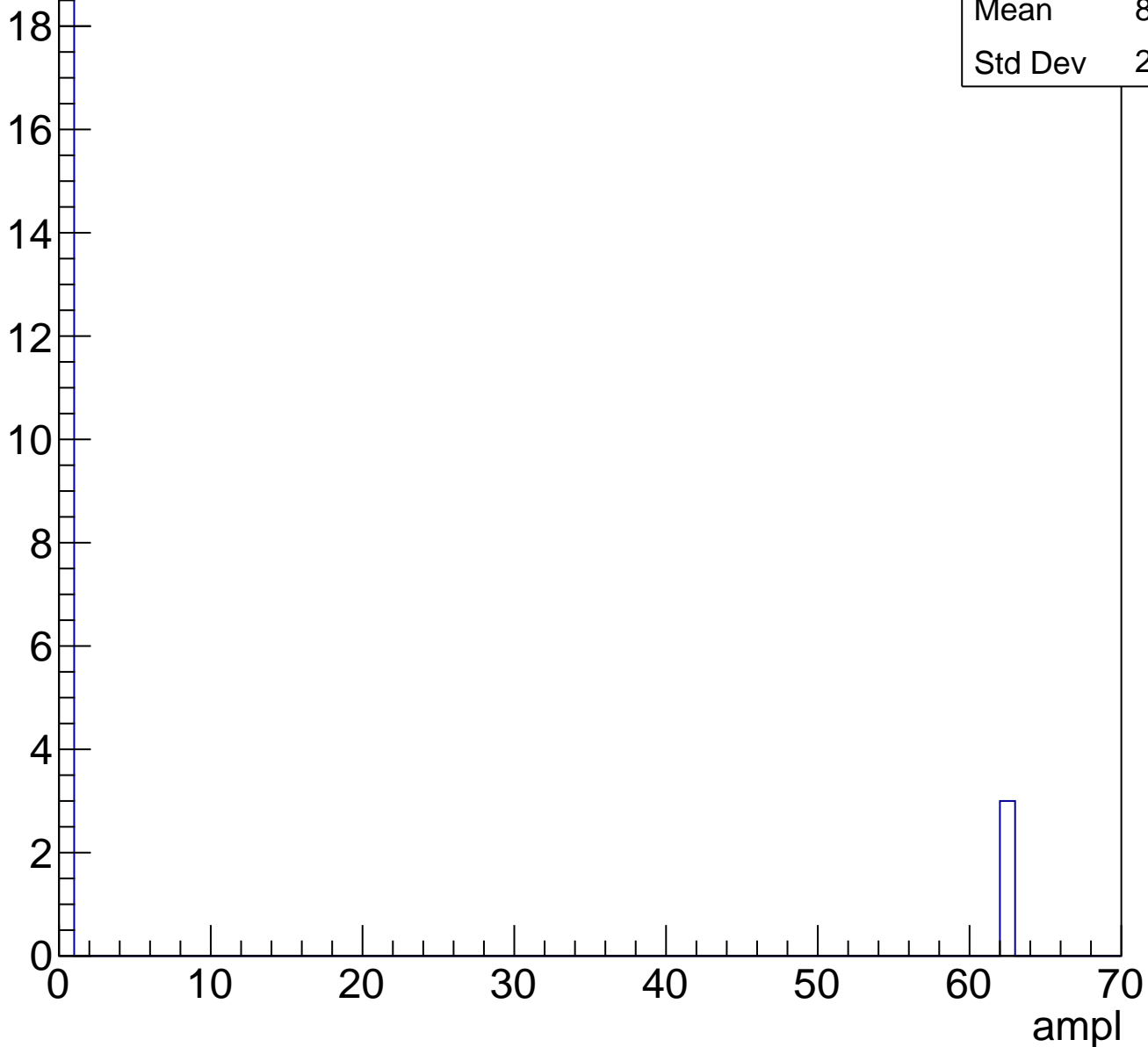


# B1L103S, U25-ch114, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	22
Mean	8.455
Std Dev	21.28

Entry



# B1L103S, U25-ch115, adc0

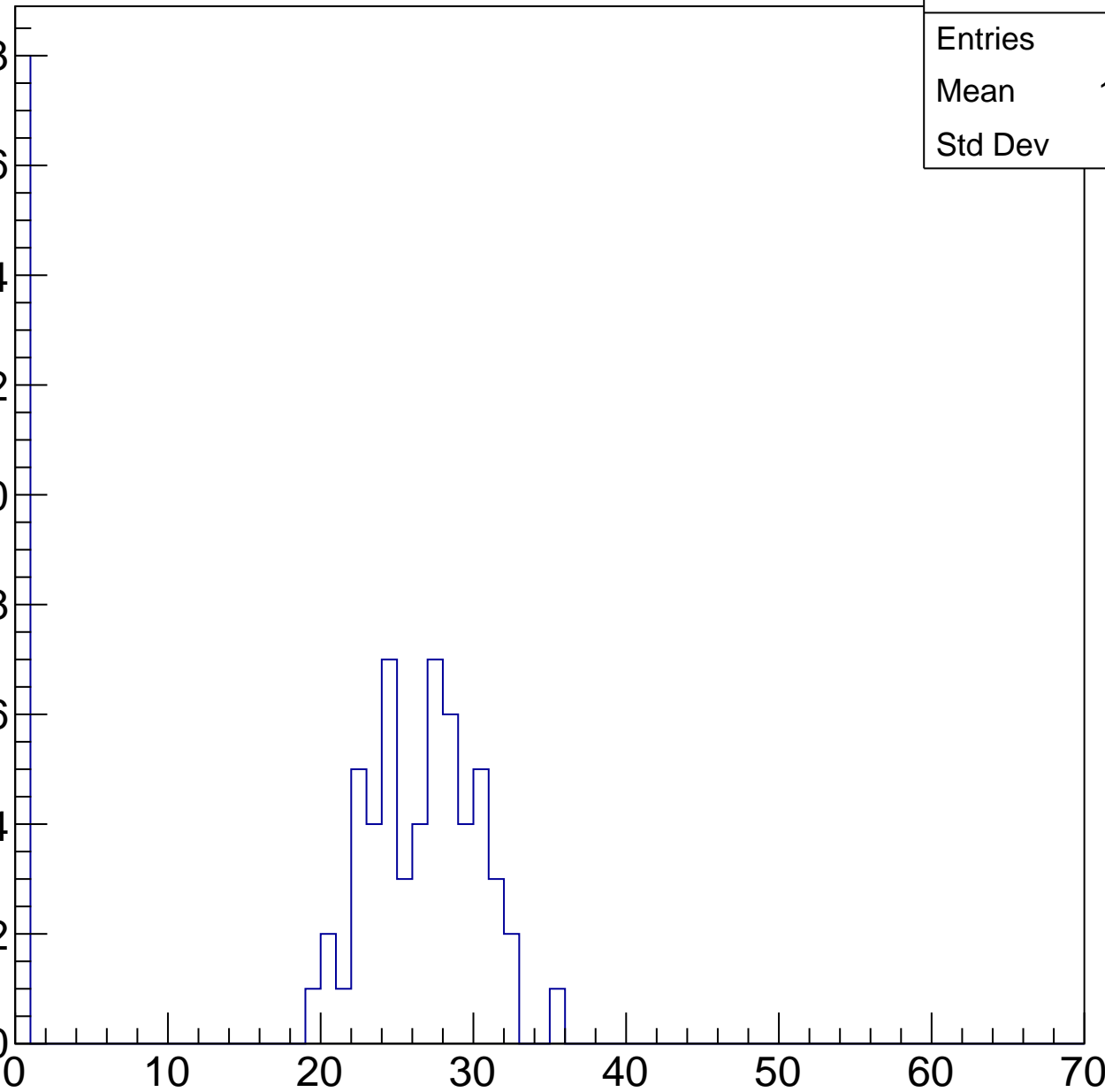
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	73
Mean	19.78
Std Dev	11.71

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

ampl

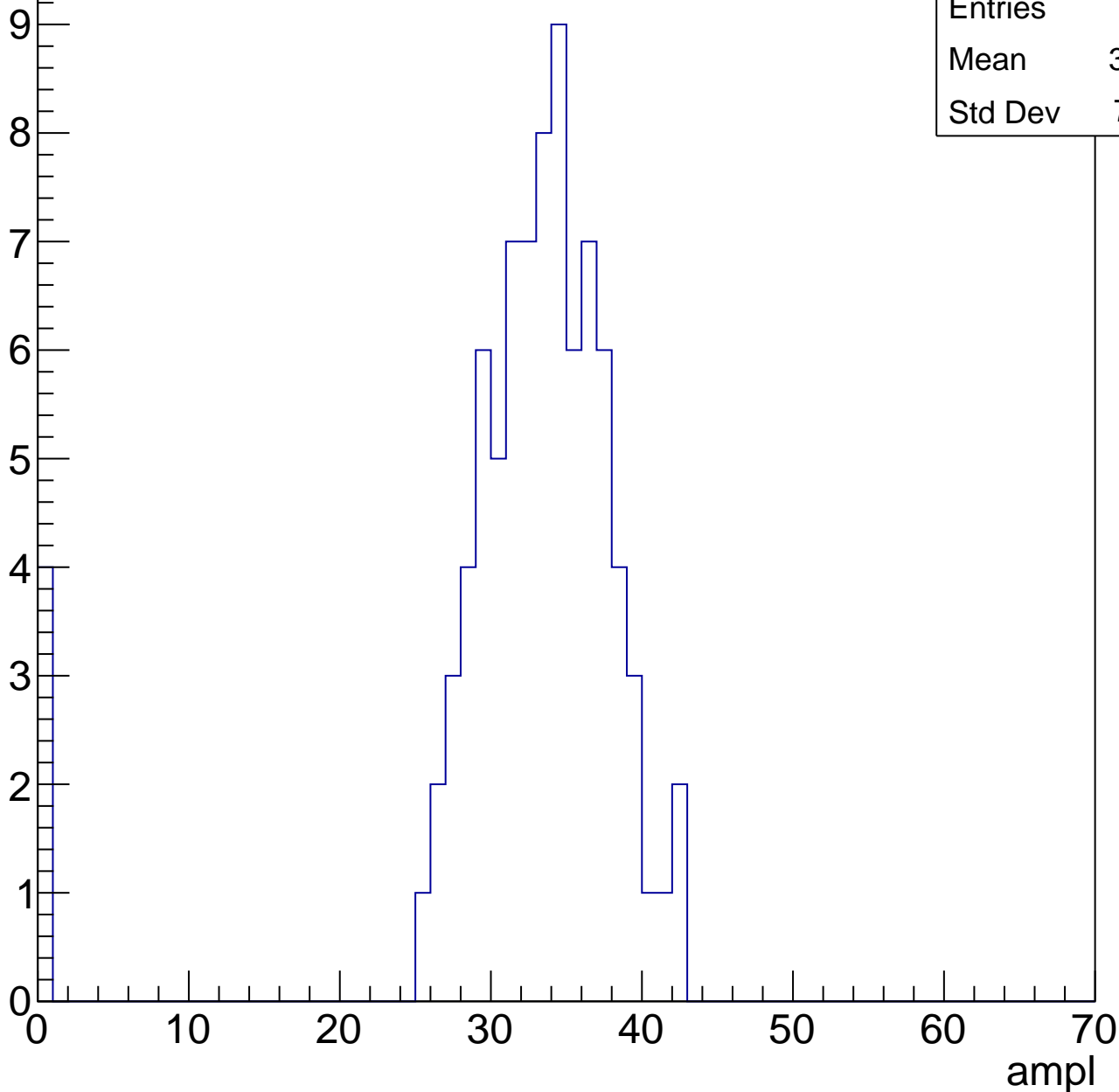


# B1L103S, U25-ch115, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	86
Mean	31.66
Std Dev	7.941

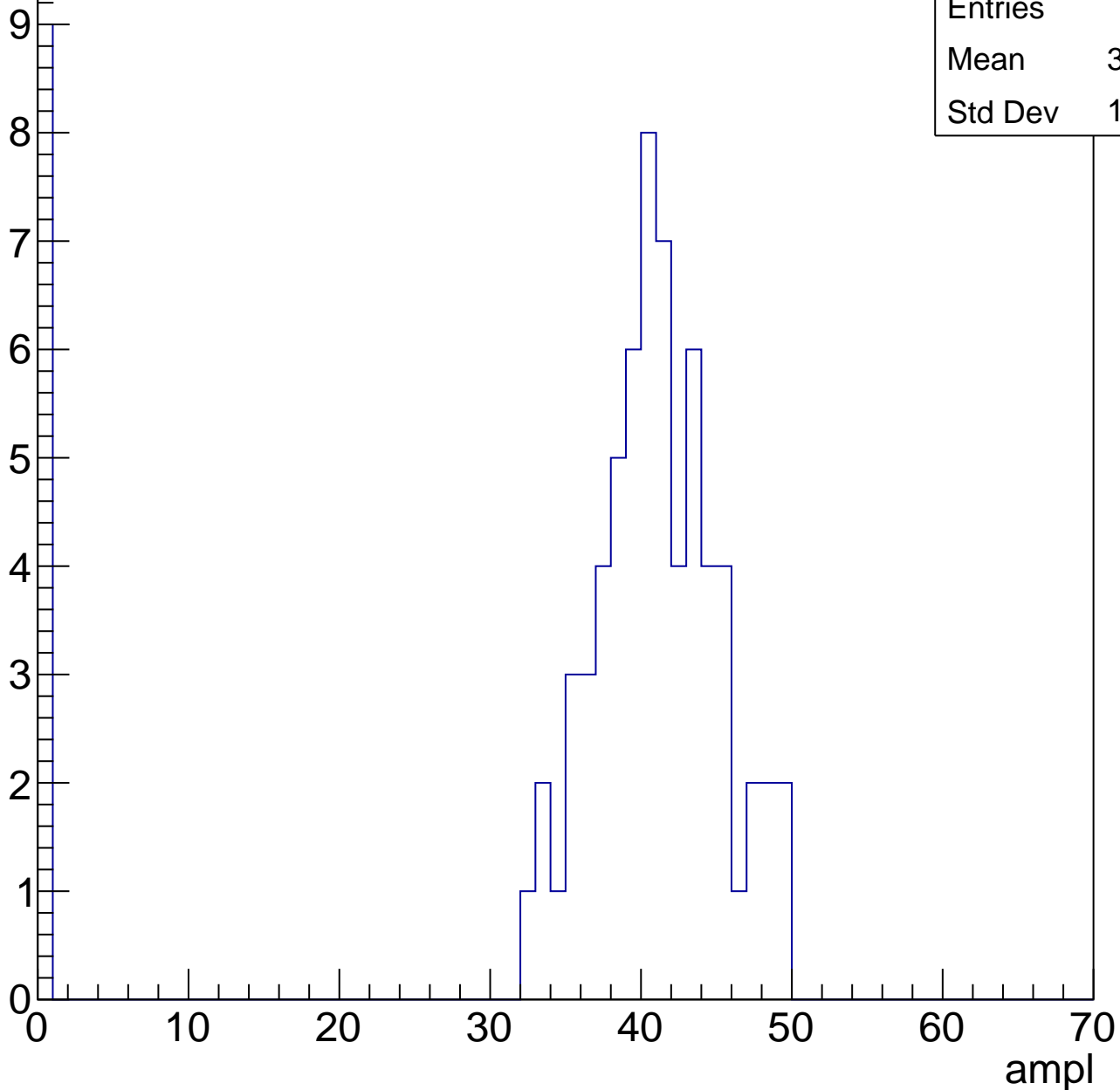


# B1L103S, U25-ch115, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	74
Mean	35.68
Std Dev	13.79

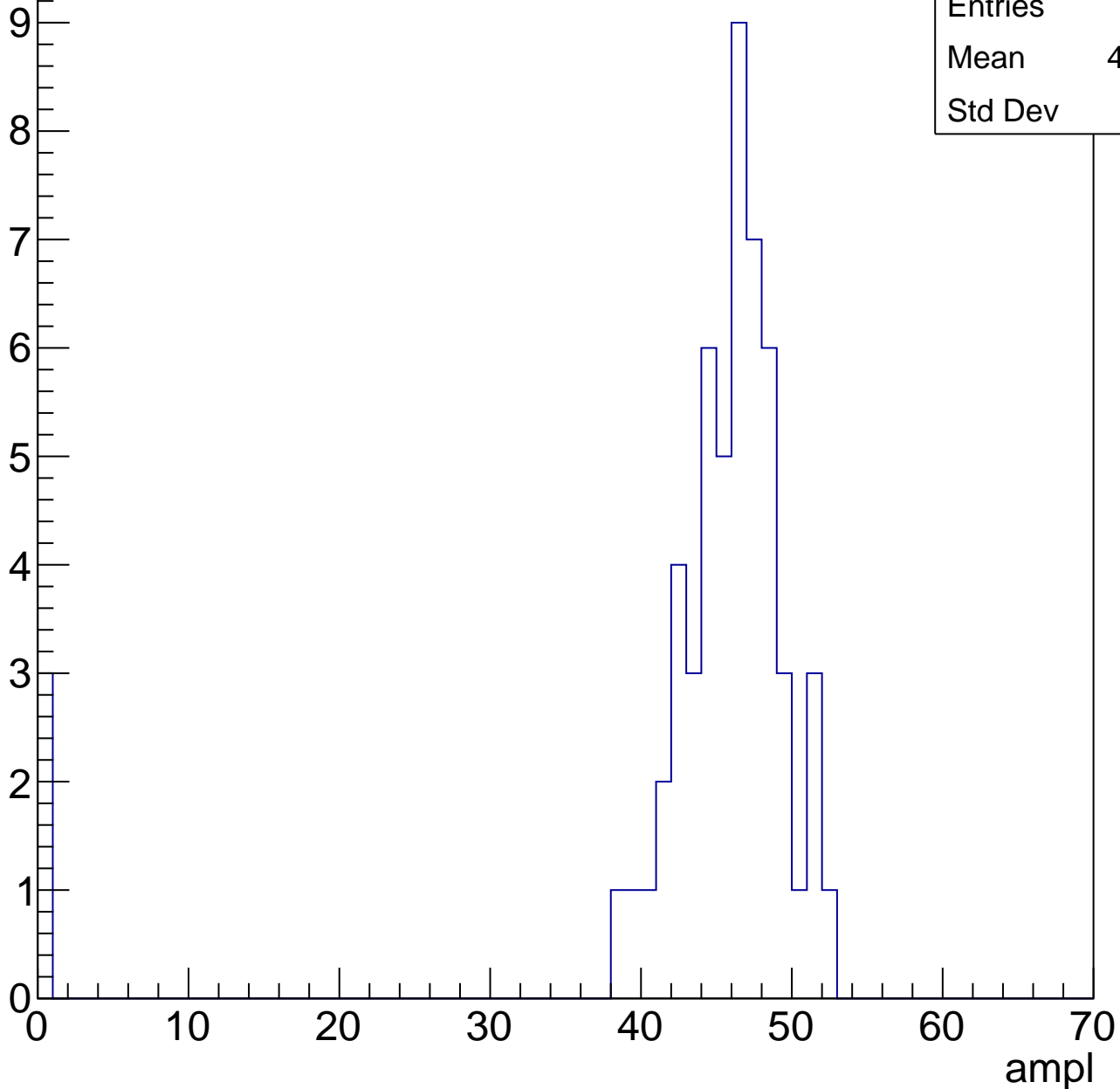


# B1L103S, U25-ch115, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	56
Mean	43.18
Std Dev	10.7

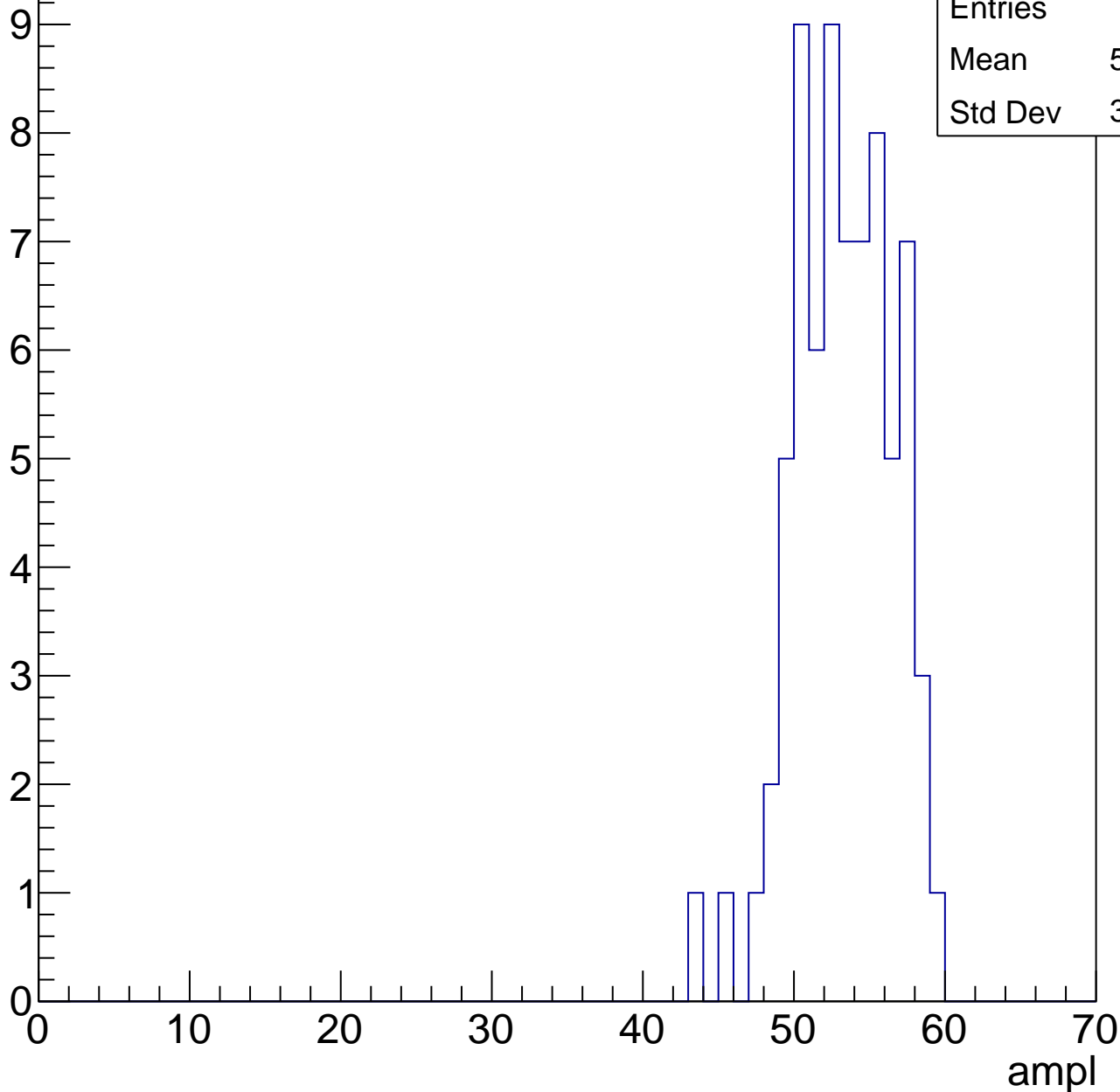


# B1L103S, U25-ch115, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	72
Mean	52.79
Std Dev	3.223

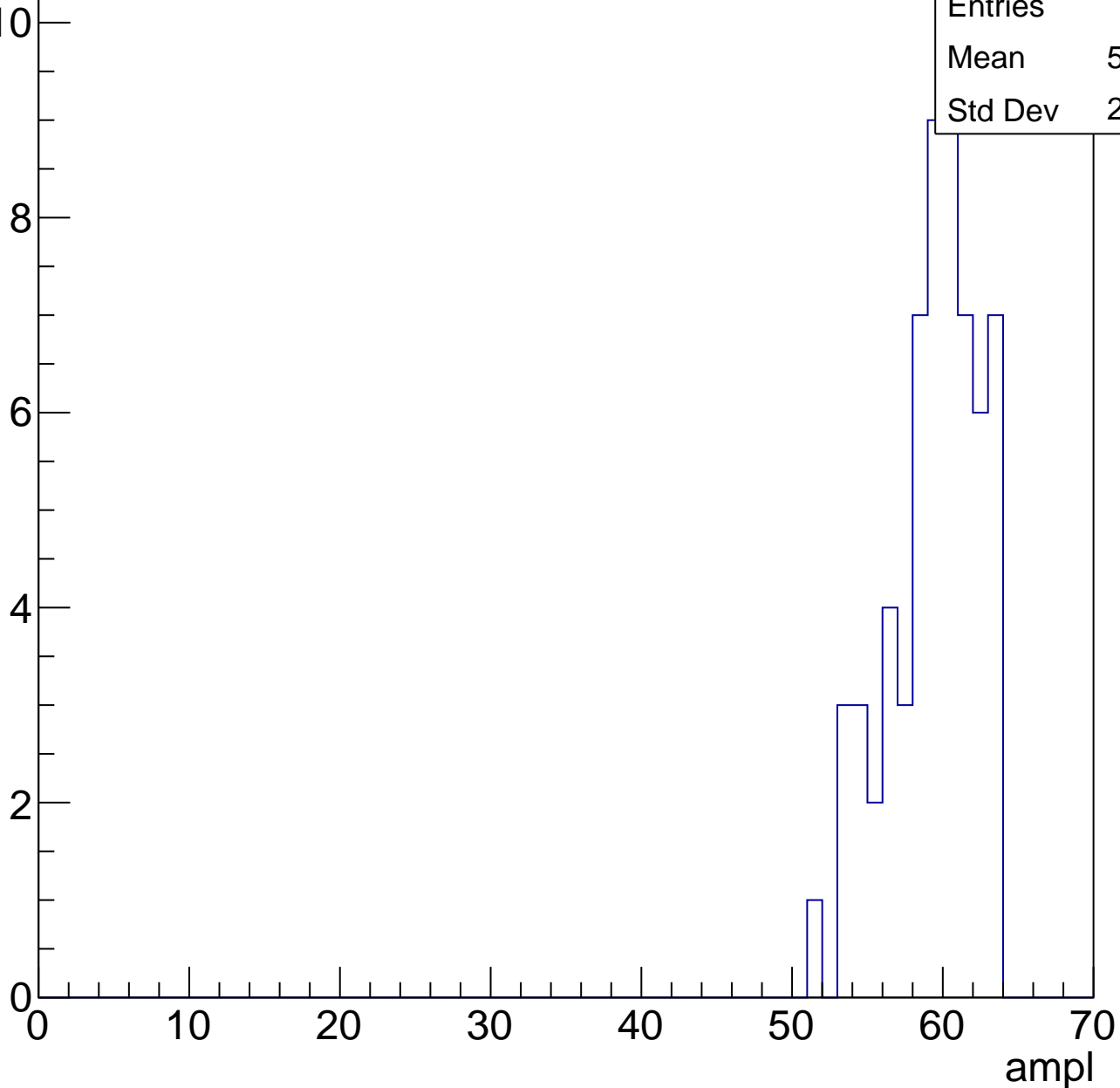


# B1L103S, U25-ch115, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

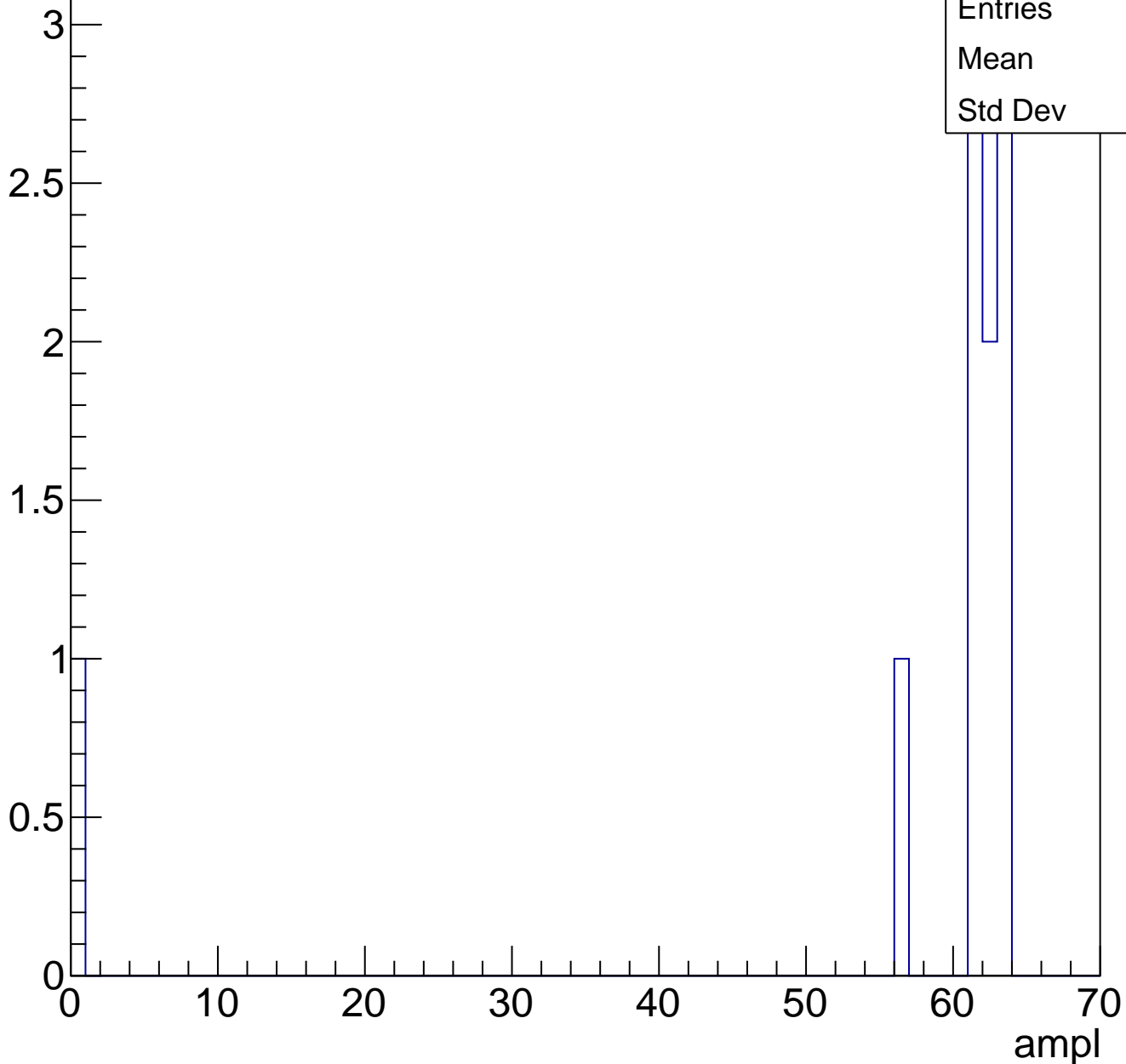
Entries	62
Mean	58.94
Std Dev	2.945



# B1L103S, U25-ch115, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

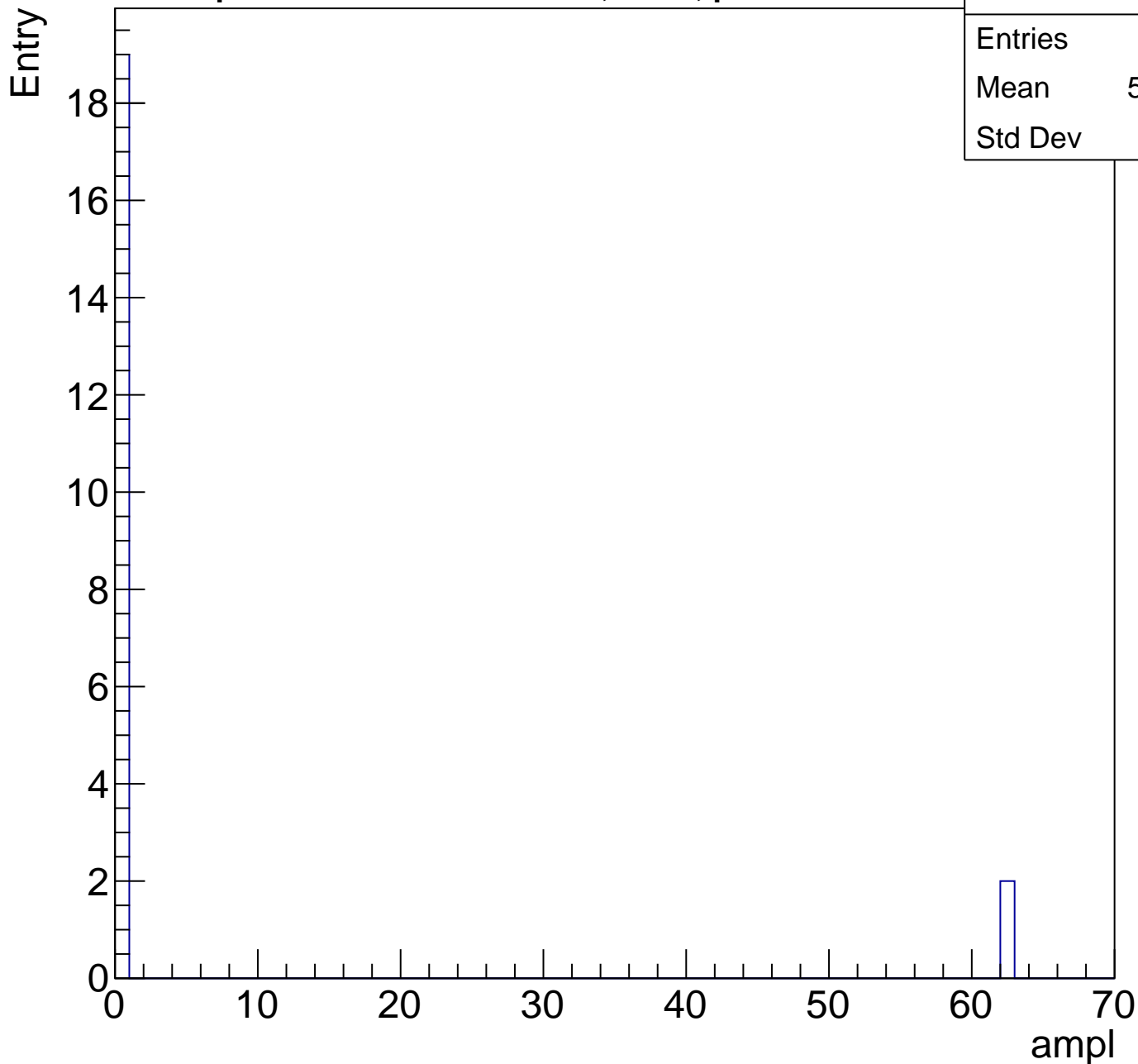




# B1L103S, U25-ch115, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

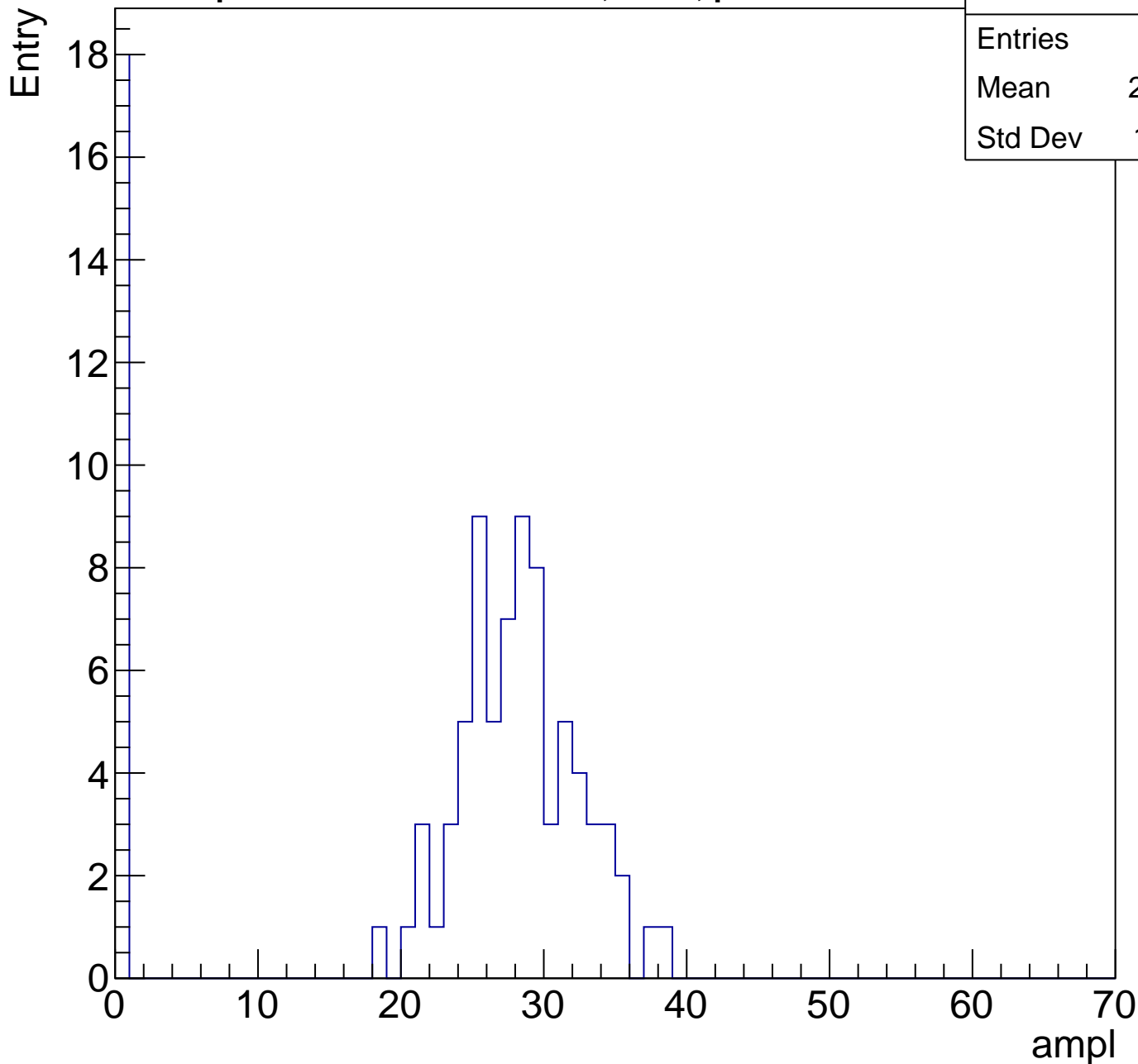
Entries	21
Mean	5.905
Std Dev	18.2



# B1L103S, U25-ch116, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	92
Mean	22.38
Std Dev	11.61

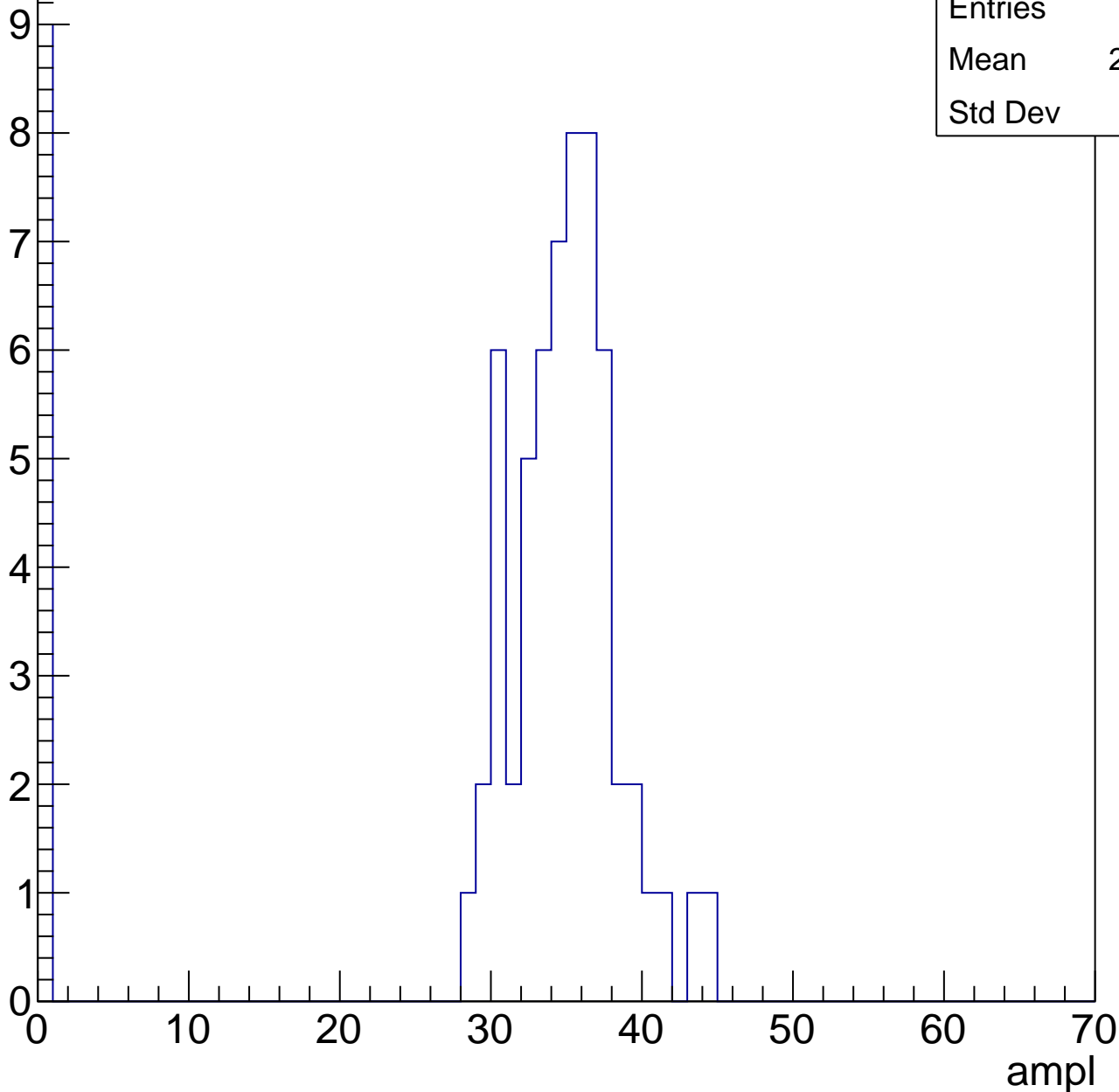


# B1L103S, U25-ch116, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	68
Mean	29.94
Std Dev	12.1

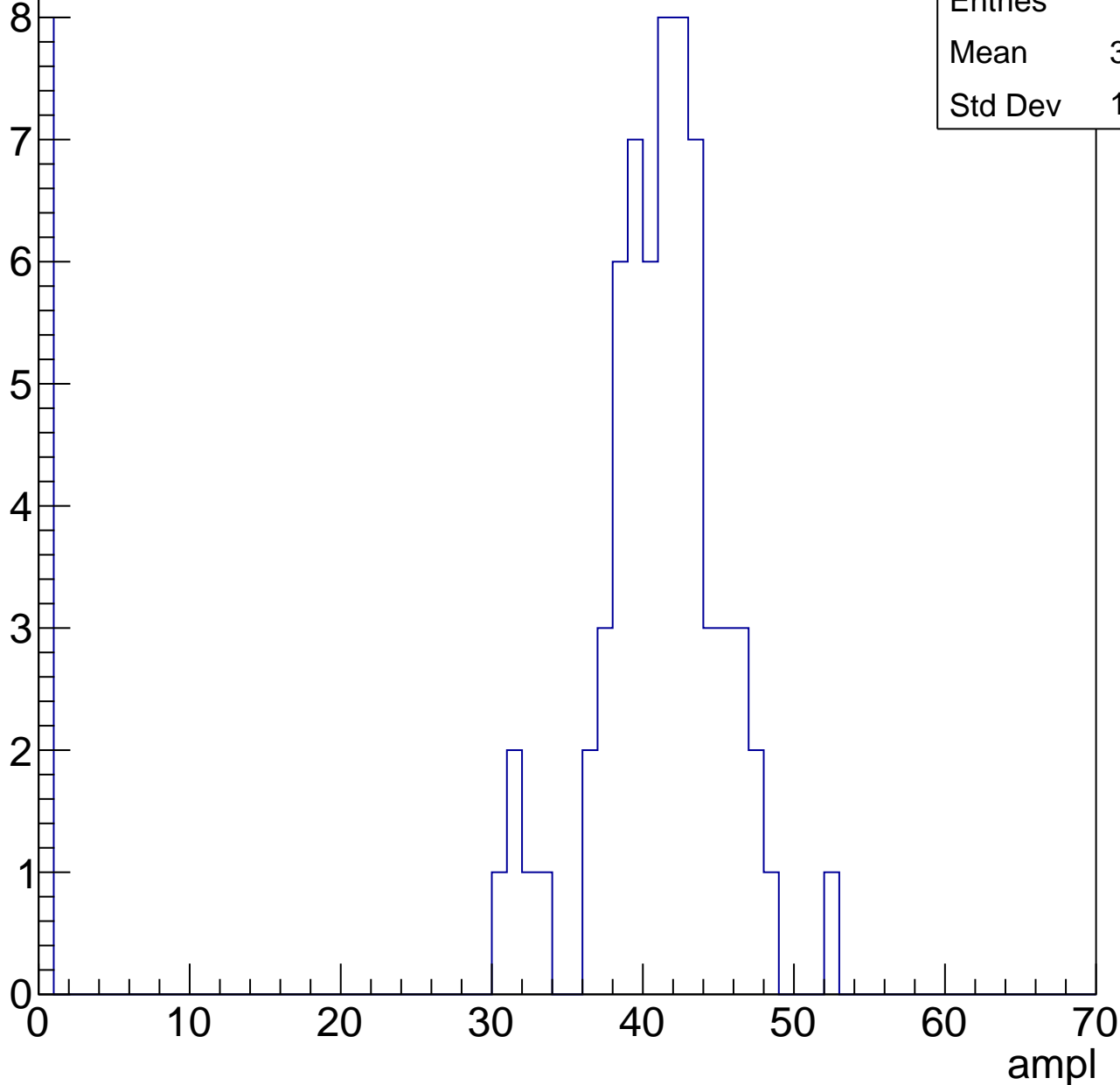


# B1L103S, U25-ch116, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	73
Mean	36.23
Std Dev	13.28

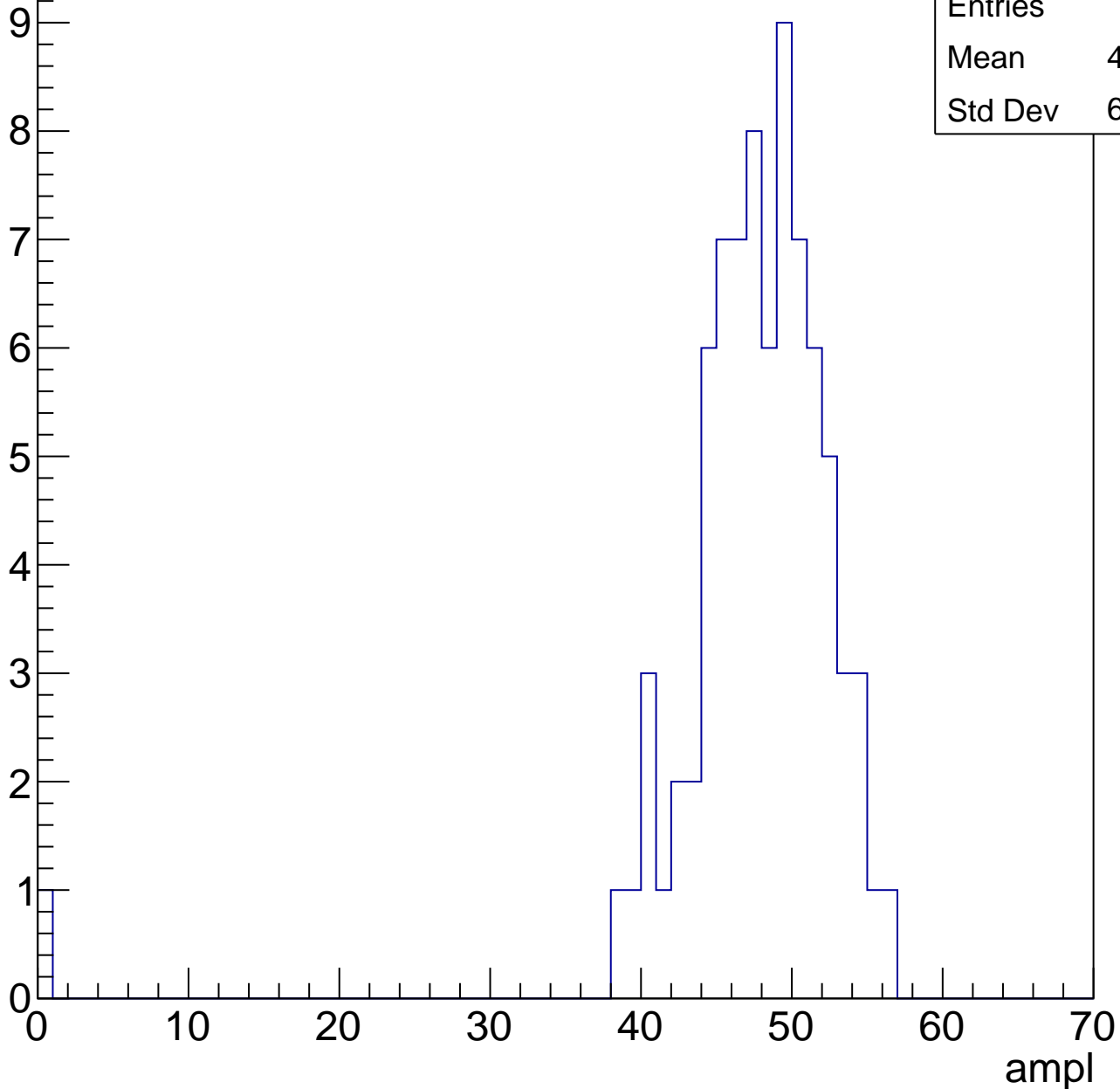


# B1L103S, U25-ch116, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	80
Mean	47.02
Std Dev	6.552

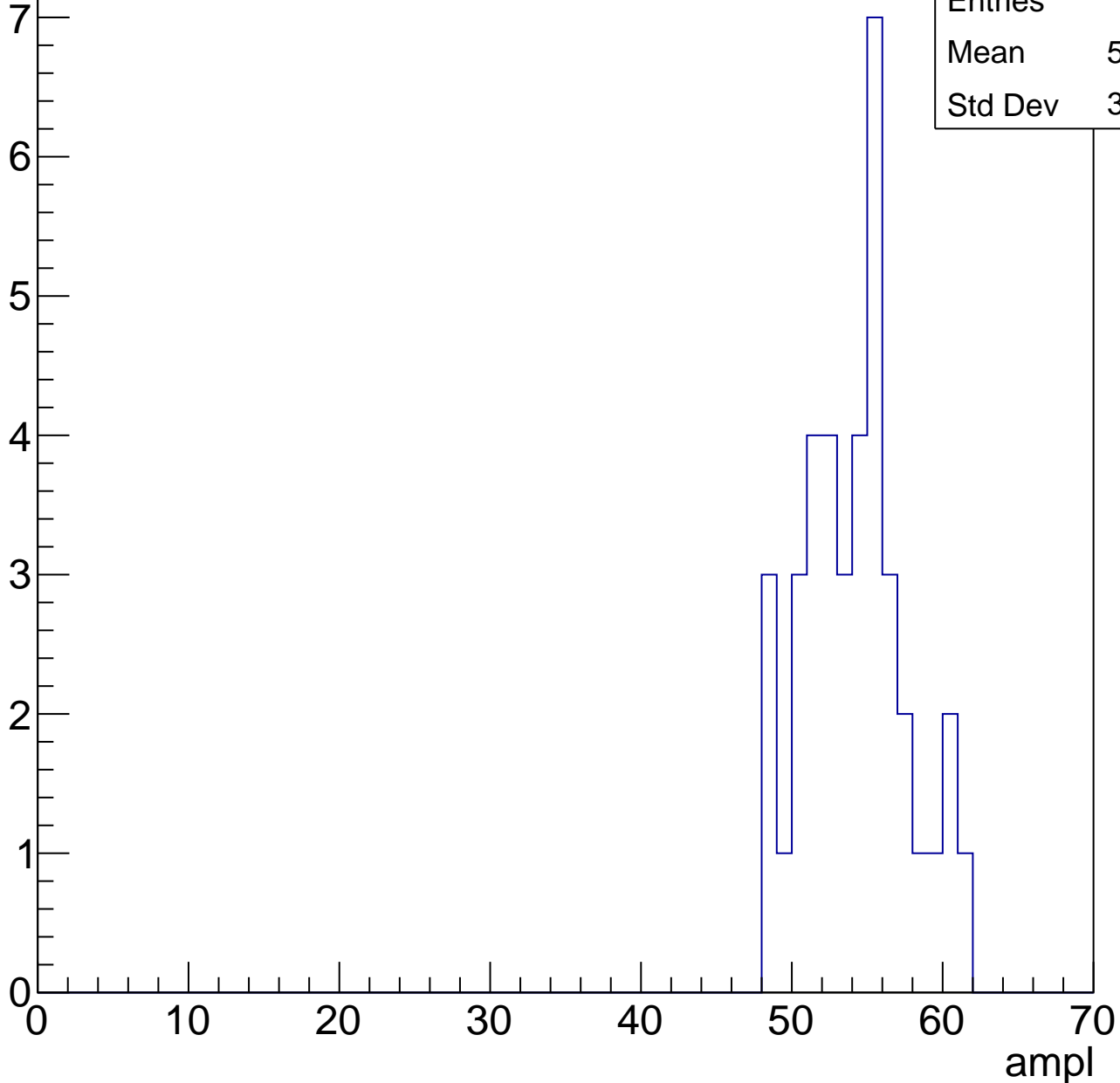


# B1L103S, U25-ch116, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	39
Mean	53.72
Std Dev	3.328

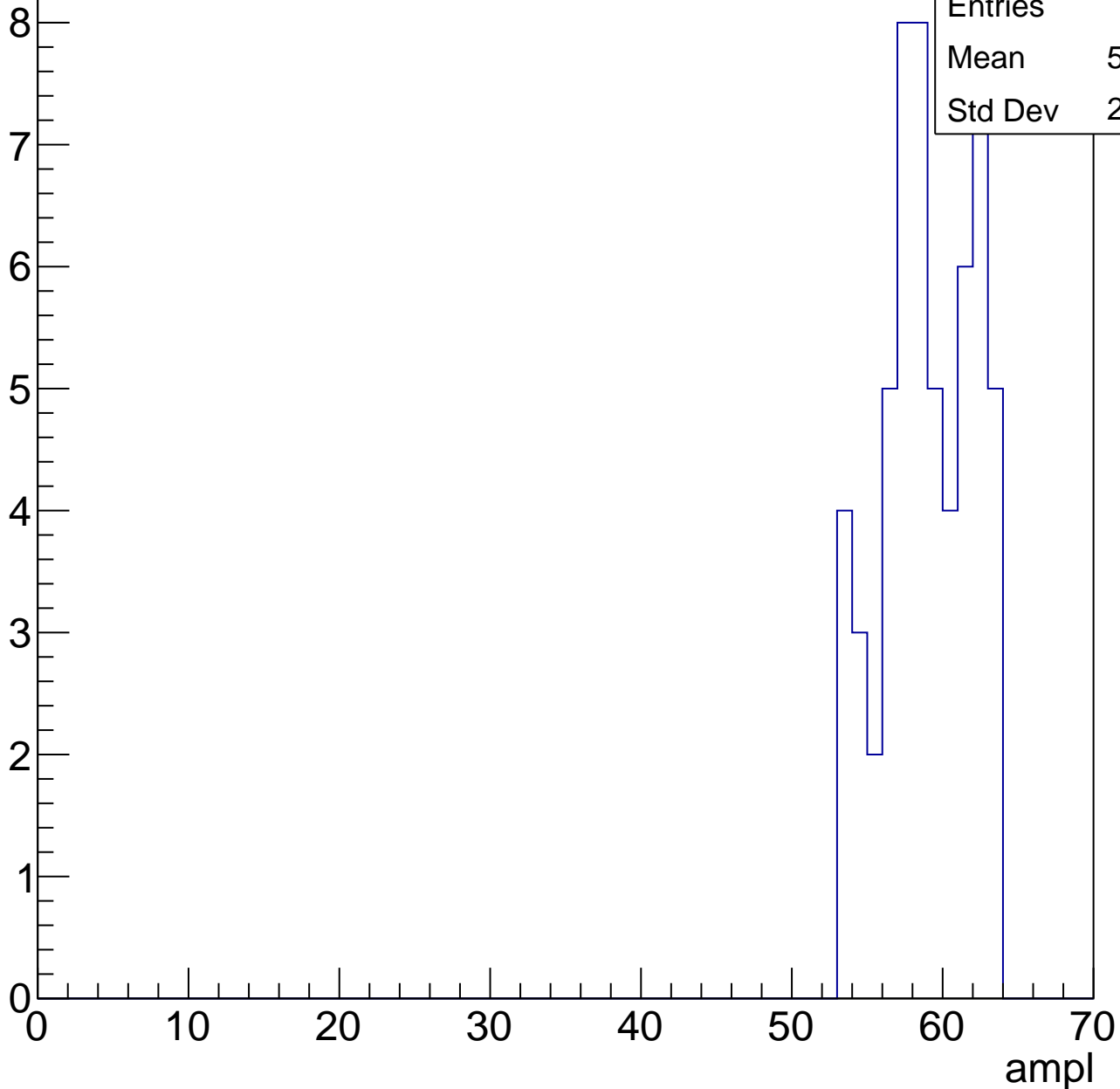


# B1L103S, U25-ch116, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	58
Mean	58.55
Std Dev	2.949

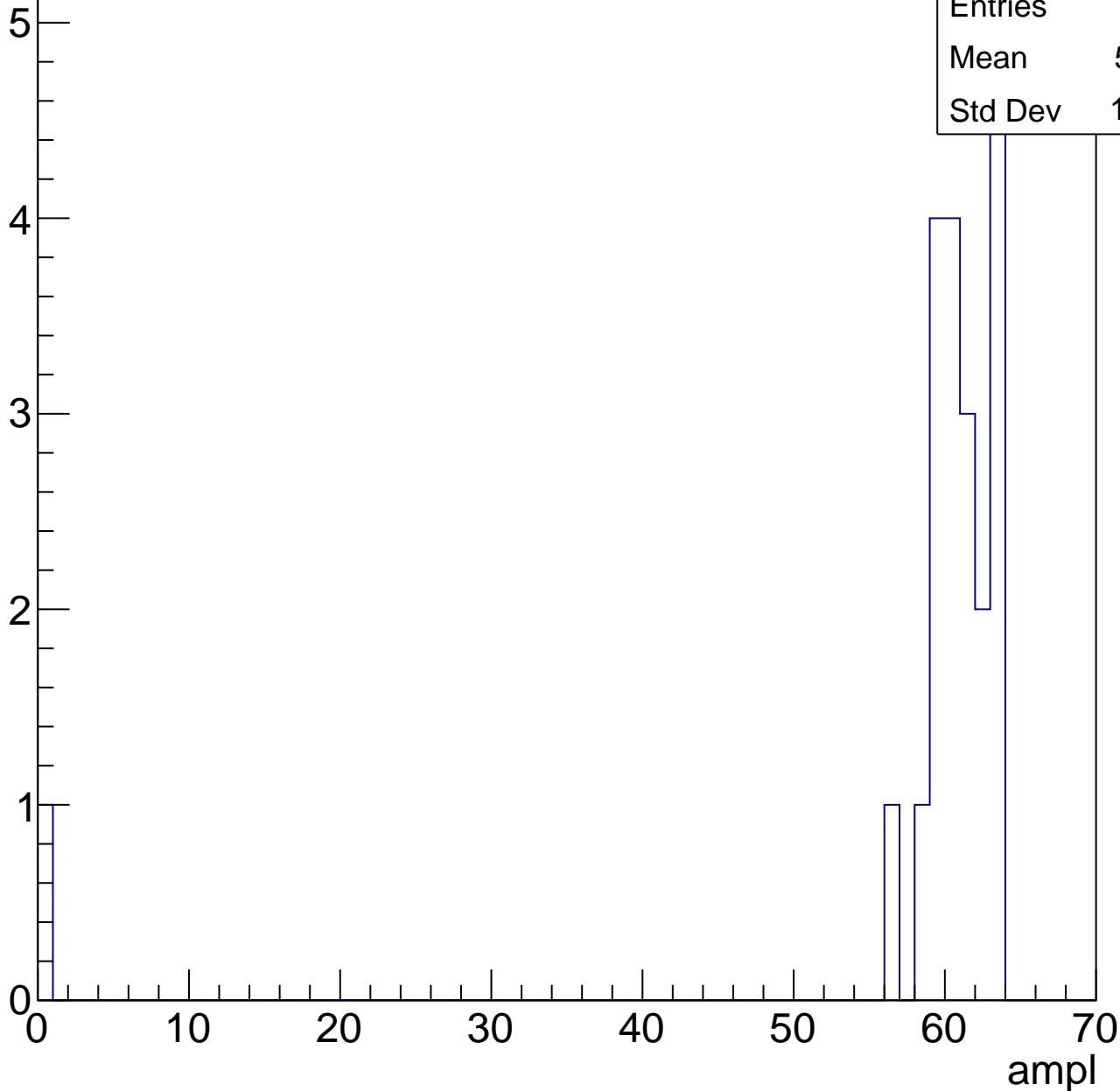


# B1L103S, U25-ch116, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	21
Mean	57.71
Std Dev	13.04





# B1L103S, U25-ch116, adc7

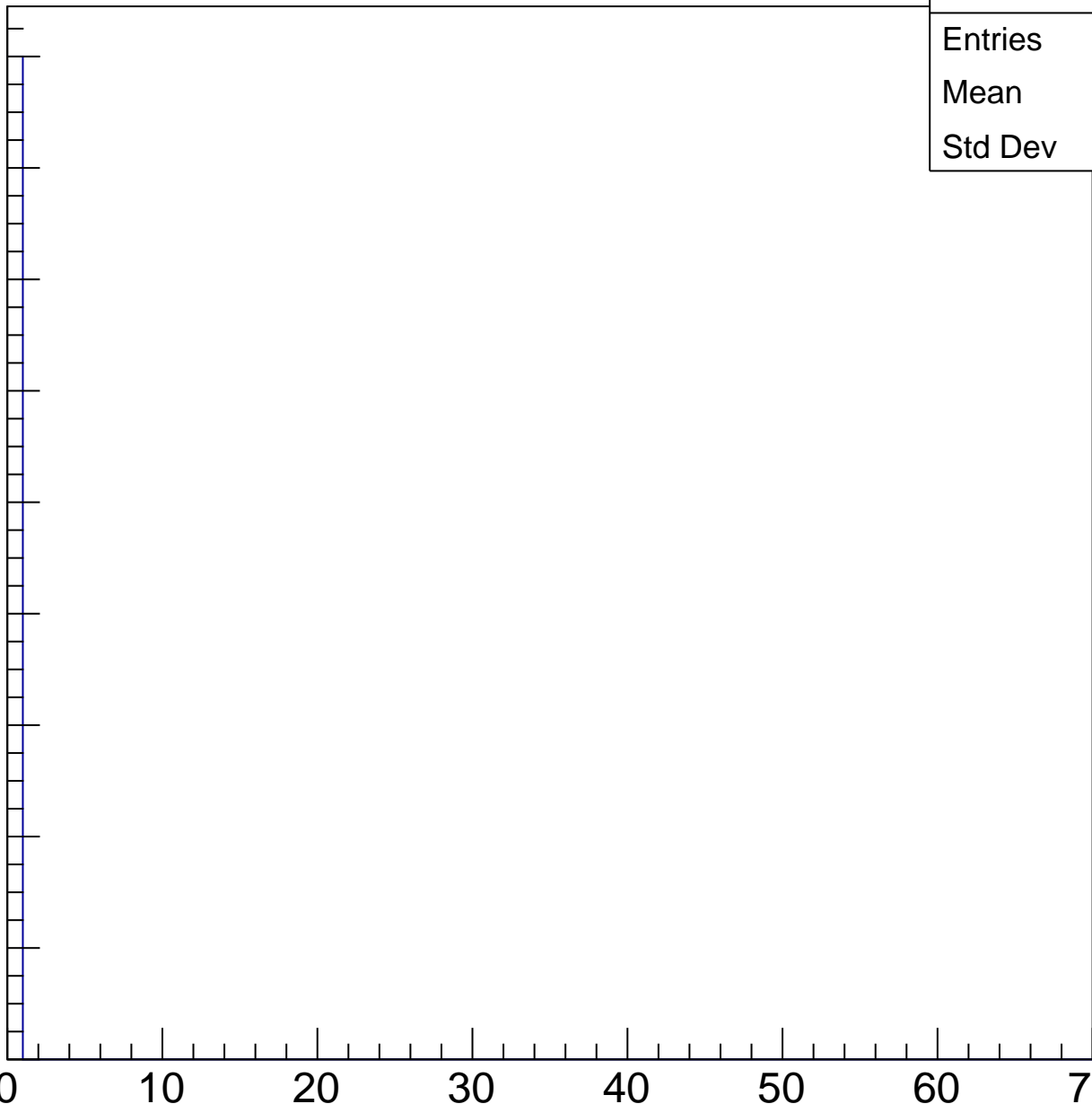
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Entries	18
Mean	0
Std Dev	0

ampl



# B1L103S, U25-ch117, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

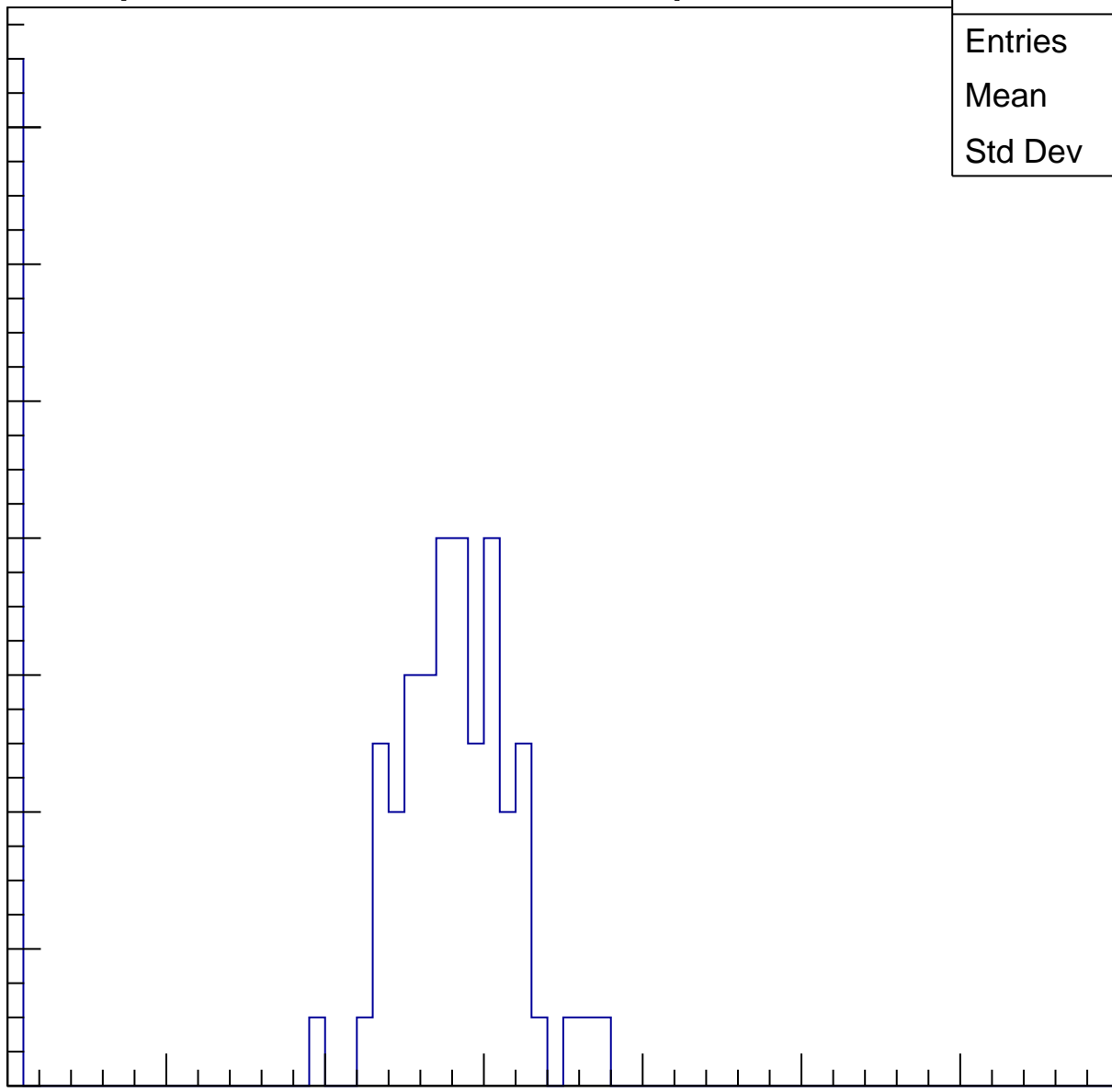
Entries	80
Mean	22.6
Std Dev	11.29

Entry

14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L103S, U25-ch117, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

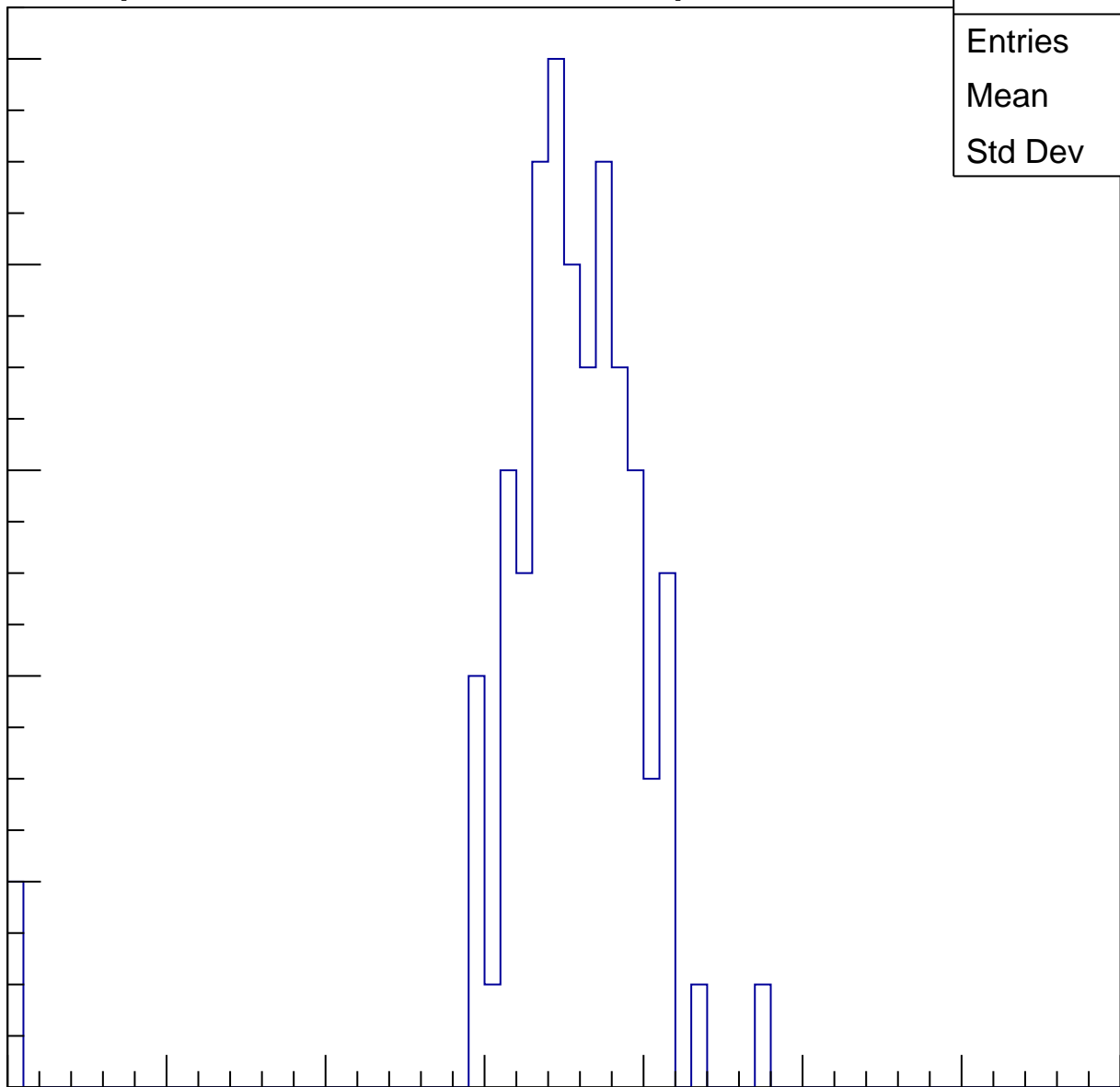
Entries	84
Mean	34.63
Std Dev	6.418

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

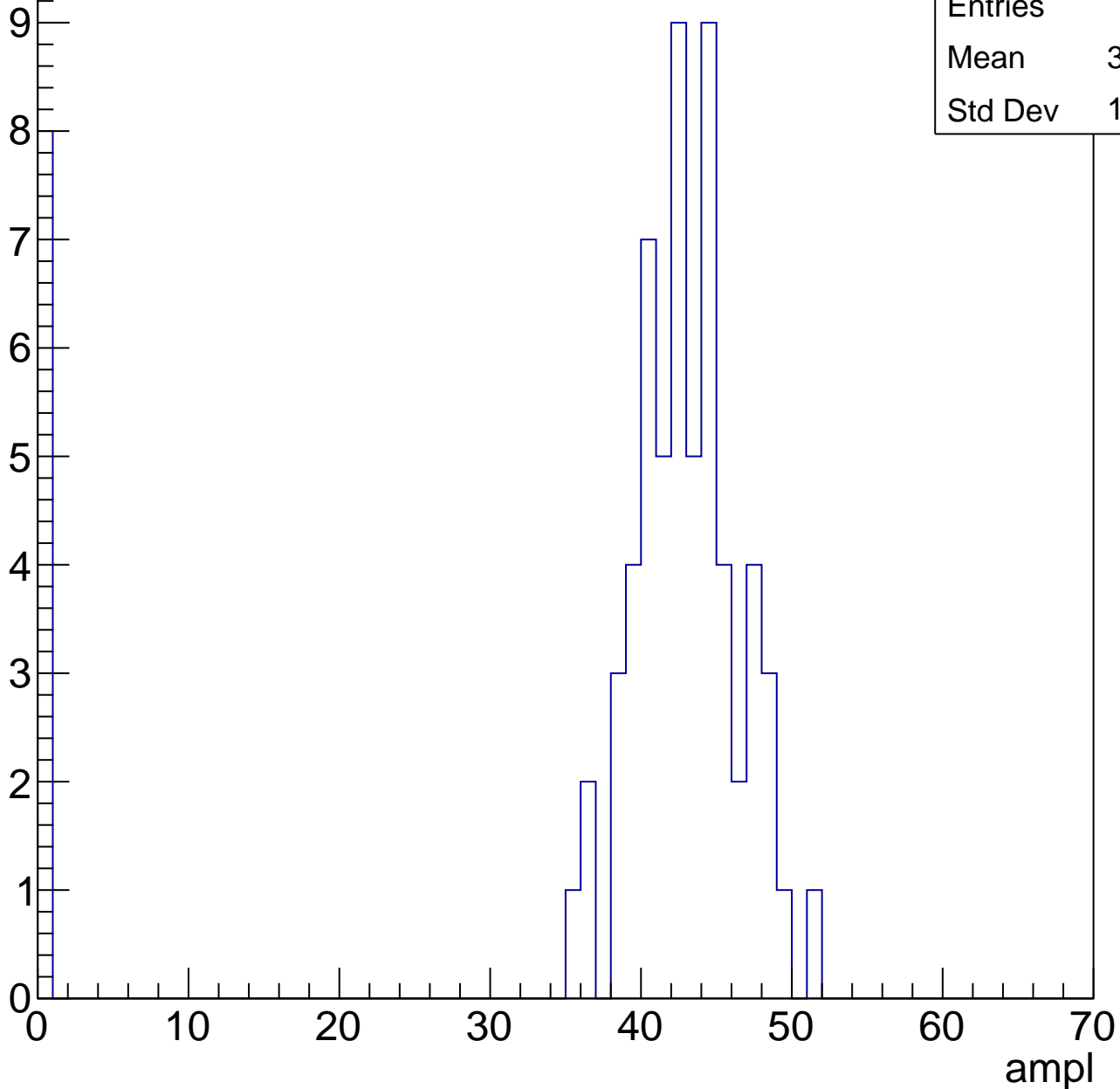


# B1L103S, U25-ch117, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	68
Mean	37.57
Std Dev	14.07

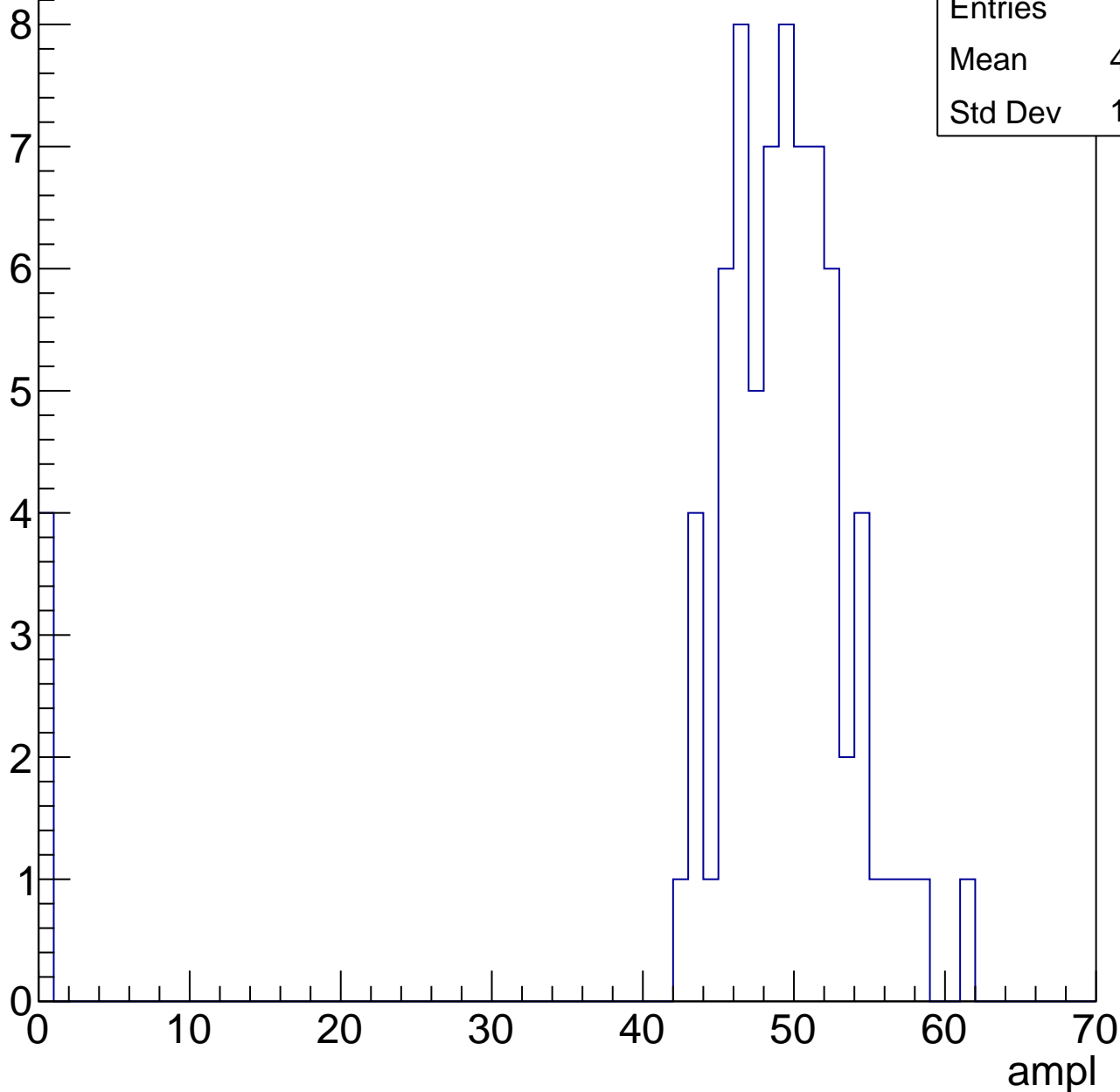


# B1L103S, U25-ch117, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	75
Mean	46.49
Std Dev	11.63

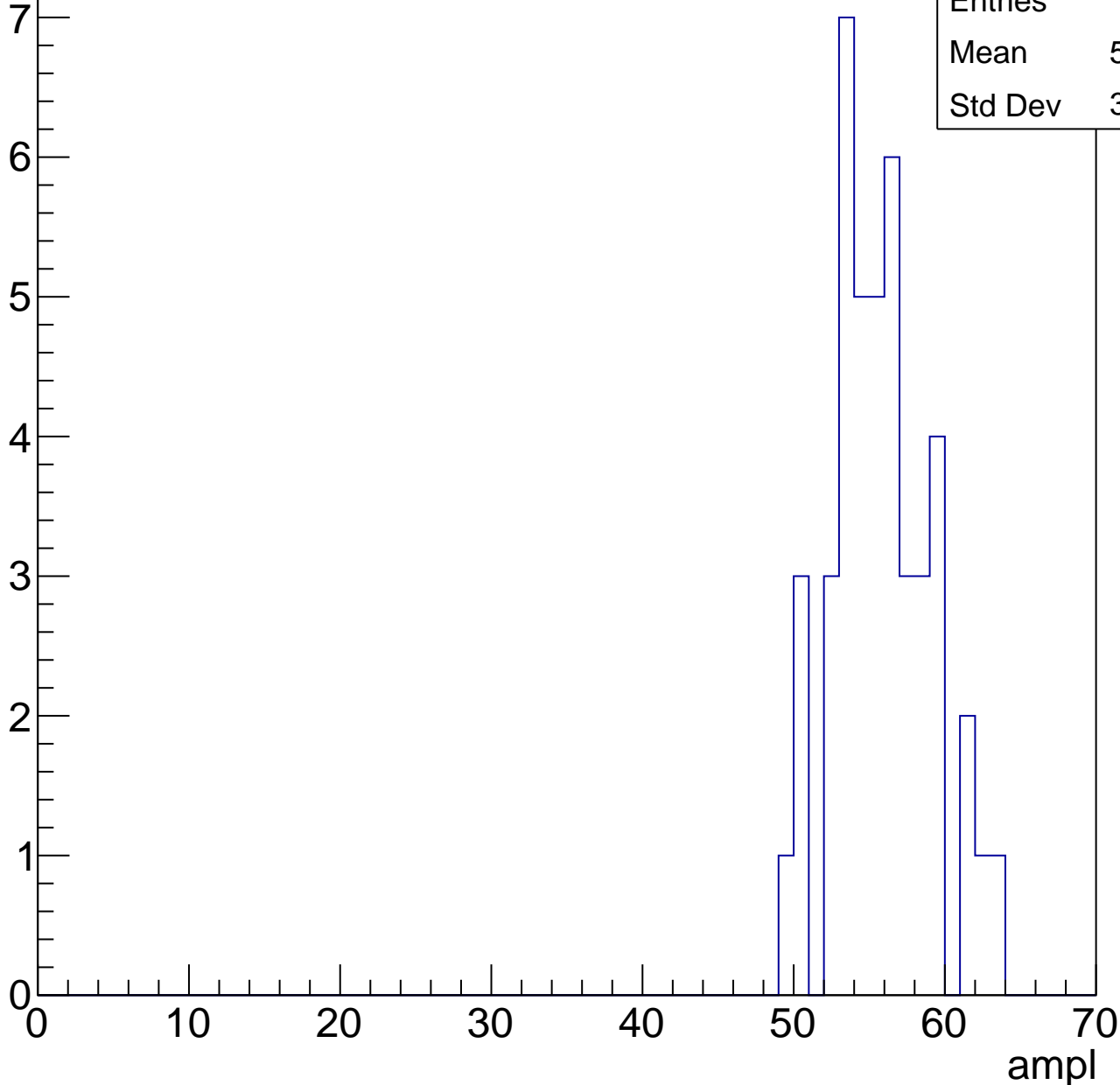


# B1L103S, U25-ch117, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	44
Mean	55.34
Std Dev	3.233



# B1L103S, U25-ch117, adc5

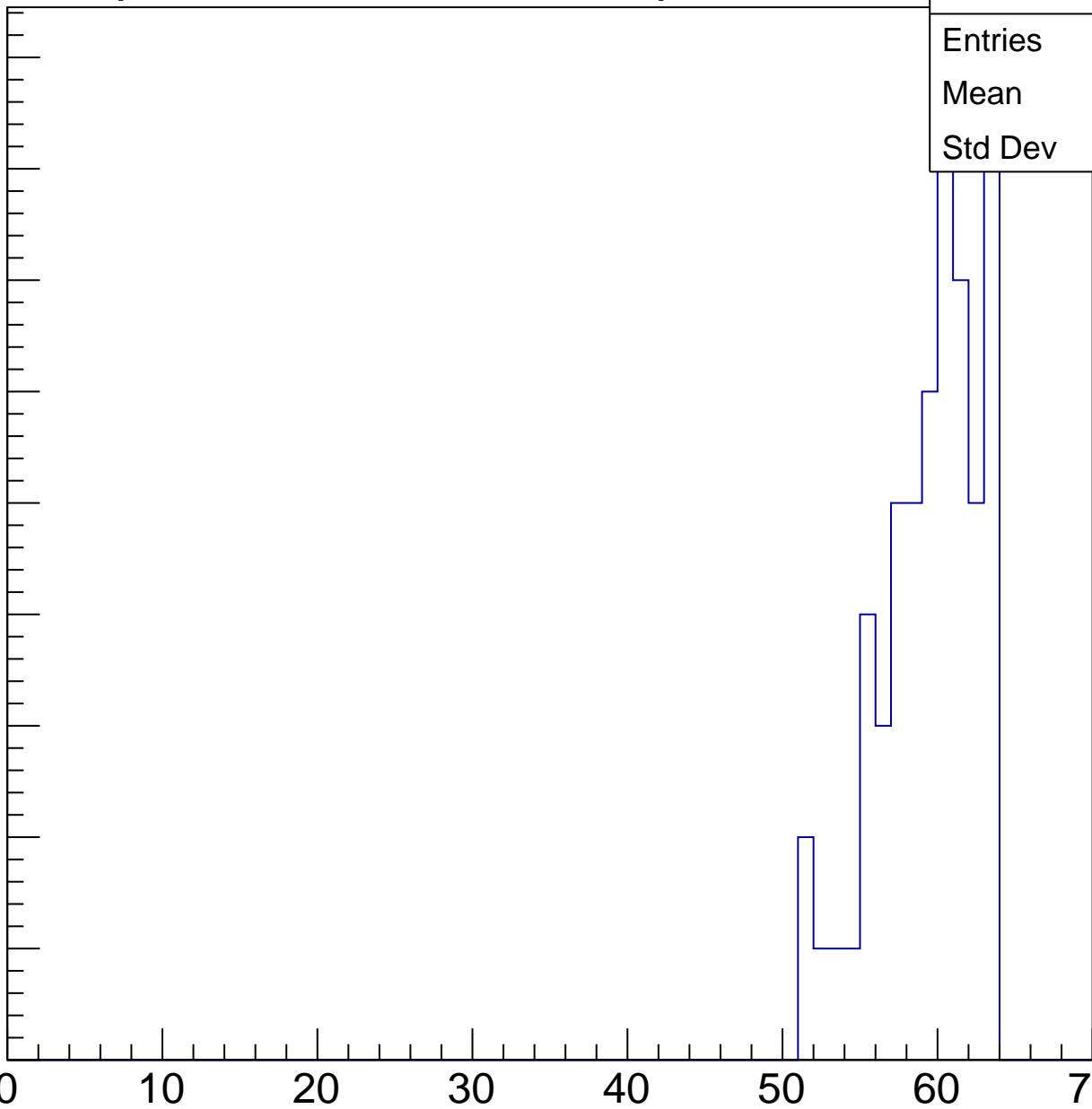
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	57
Mean	58.93
Std Dev	3.145

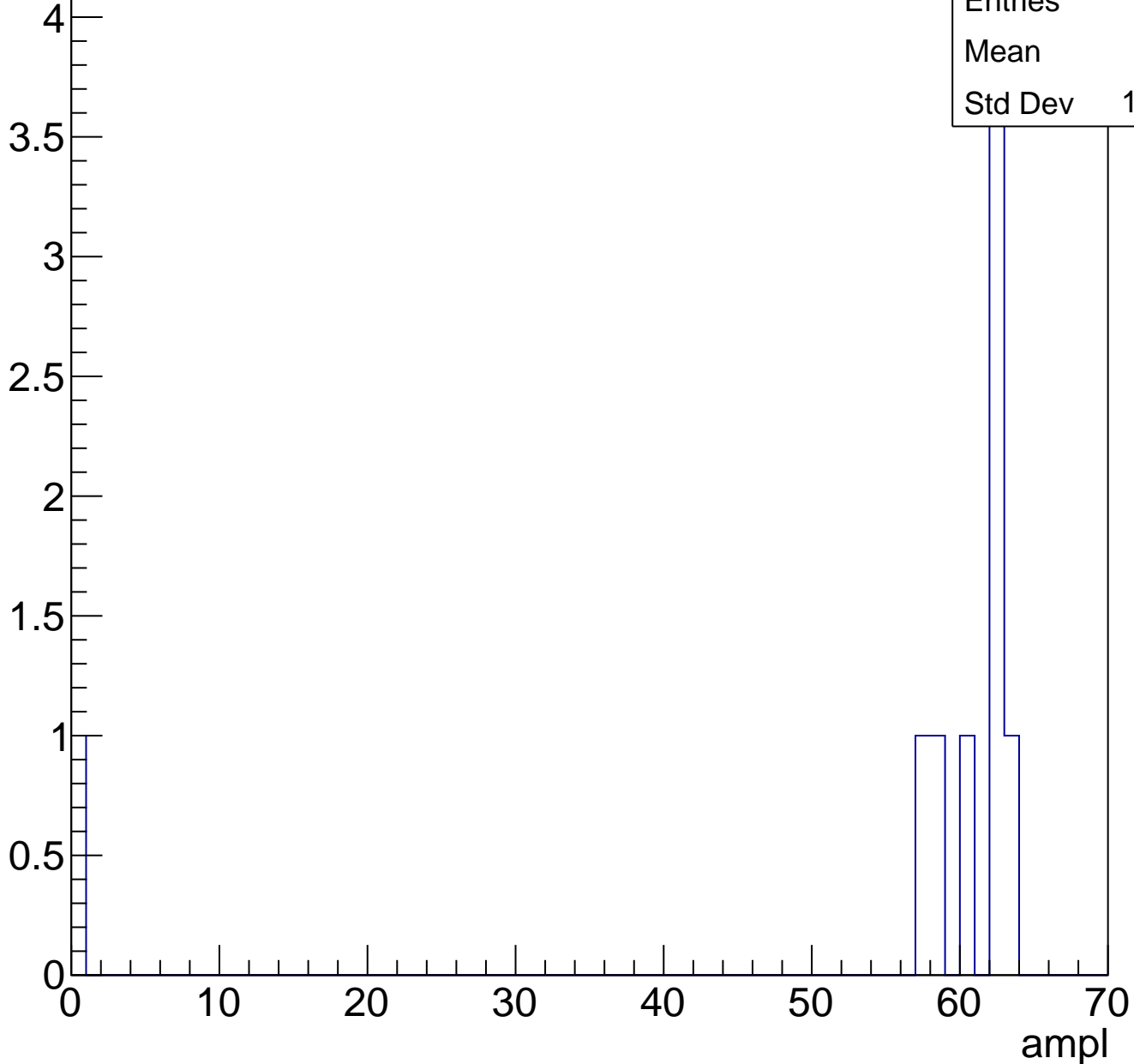
ampl



# B1L103S, U25-ch117, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U25-ch117, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Entries	18
Mean	0
Std Dev	0

ampl

# B1L103S, U25-ch118, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

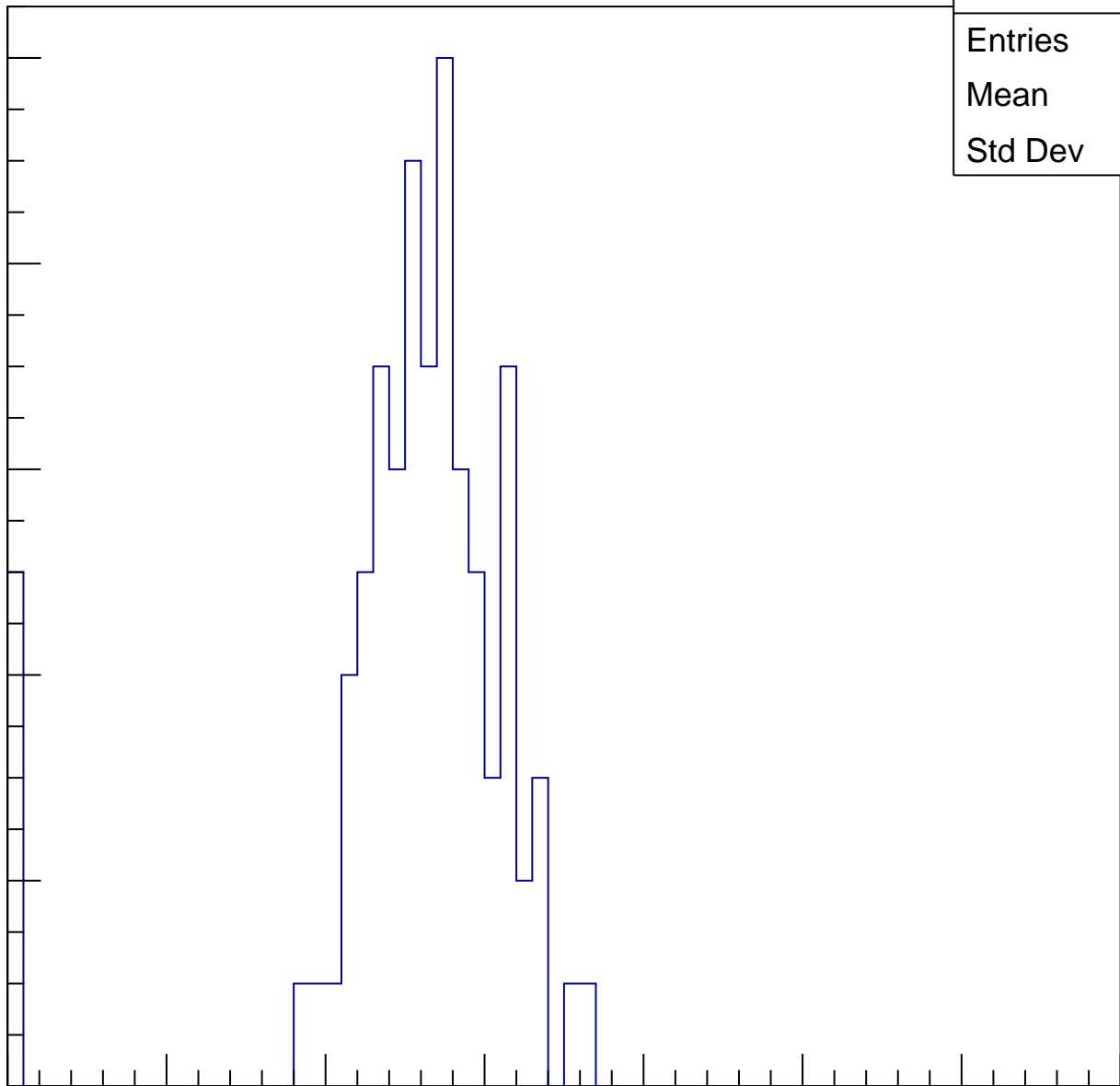
Entries	84
Mean	24.85
Std Dev	7.233

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

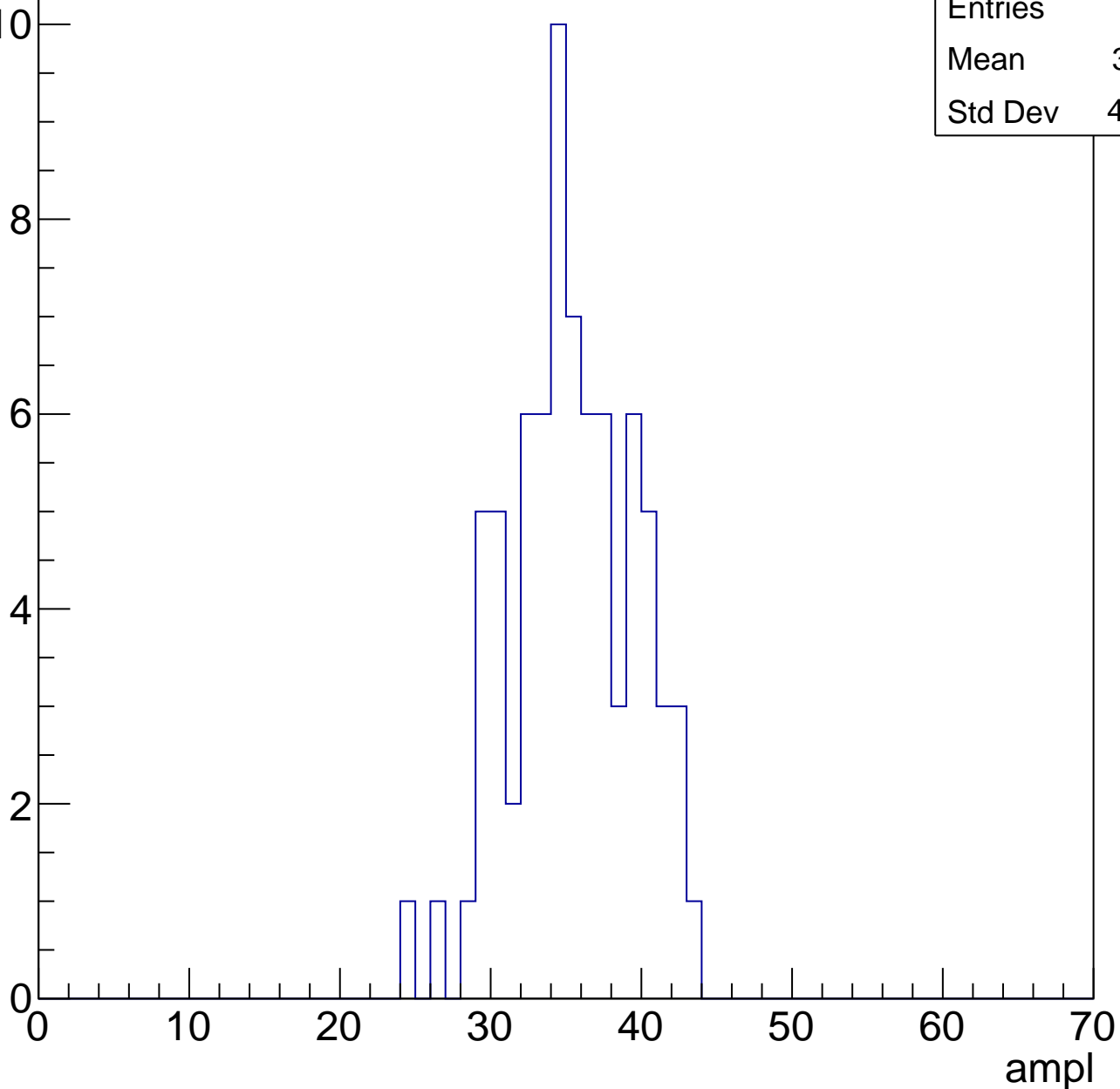


# B1L103S, U25-ch118, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	77
Mean	34.91
Std Dev	4.065

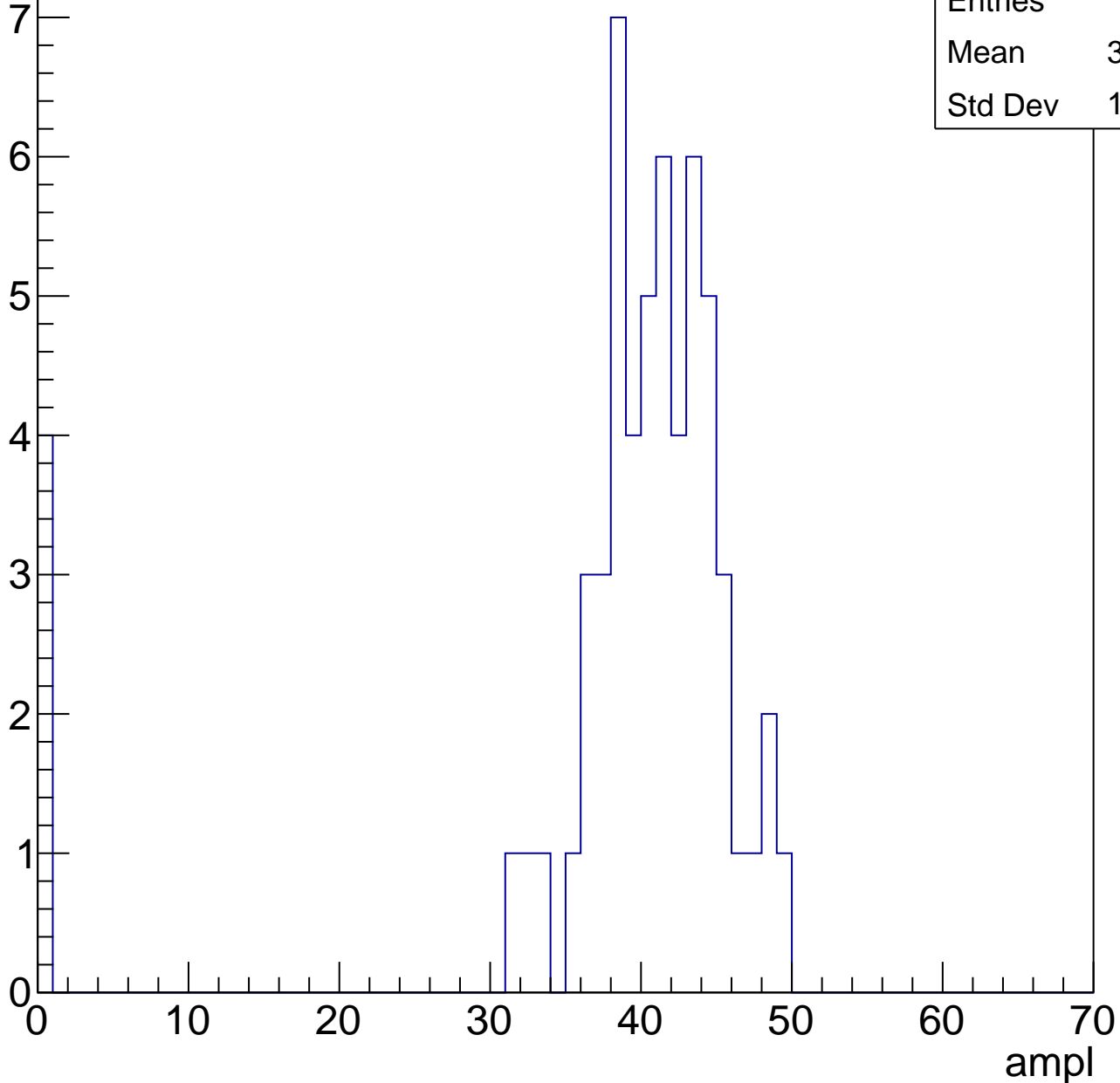


# B1L103S, U25-ch118, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	59
Mean	37.92
Std Dev	10.89

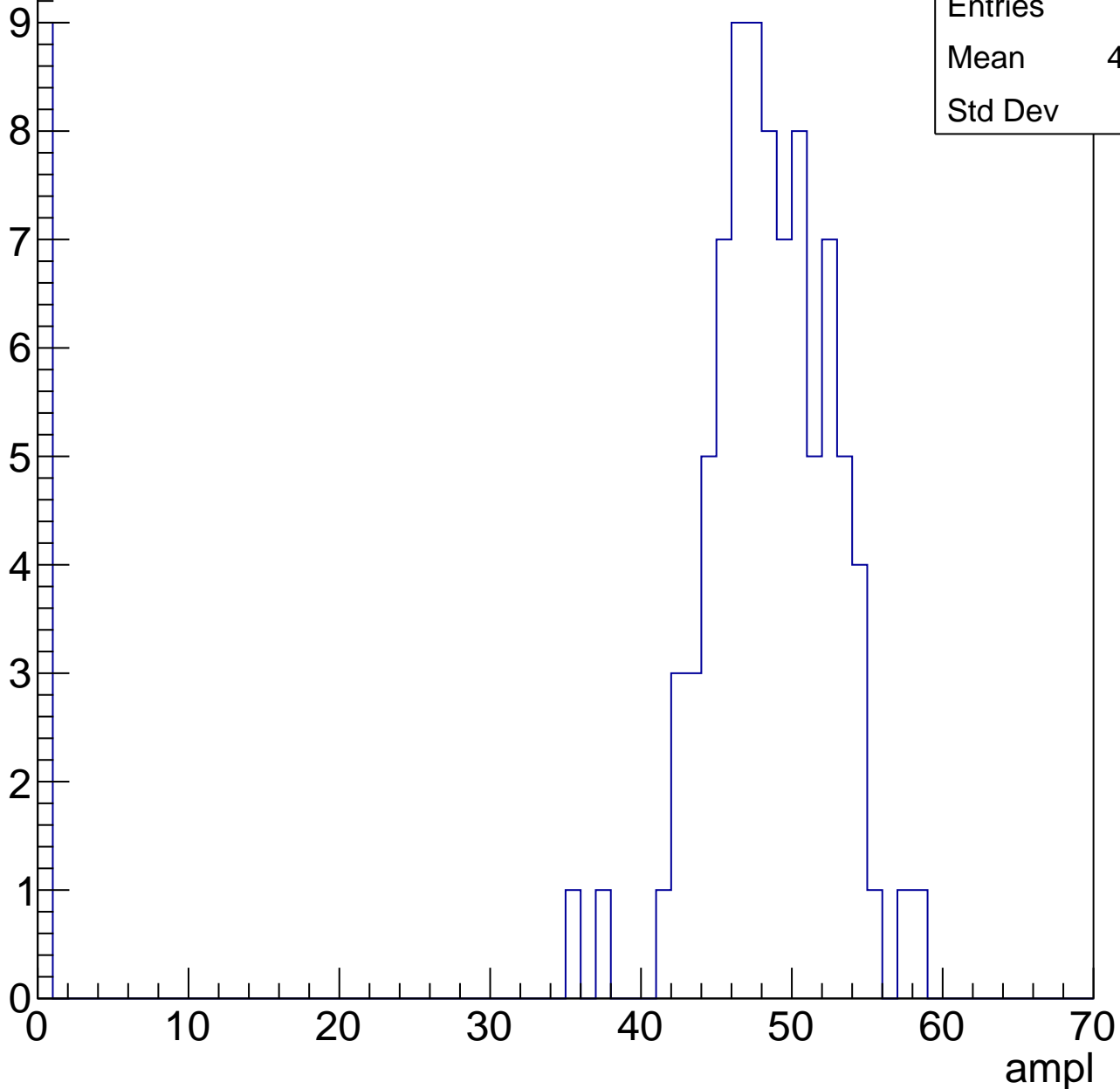


# B1L103S, U25-ch118, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	95
Mean	43.55
Std Dev	14.6

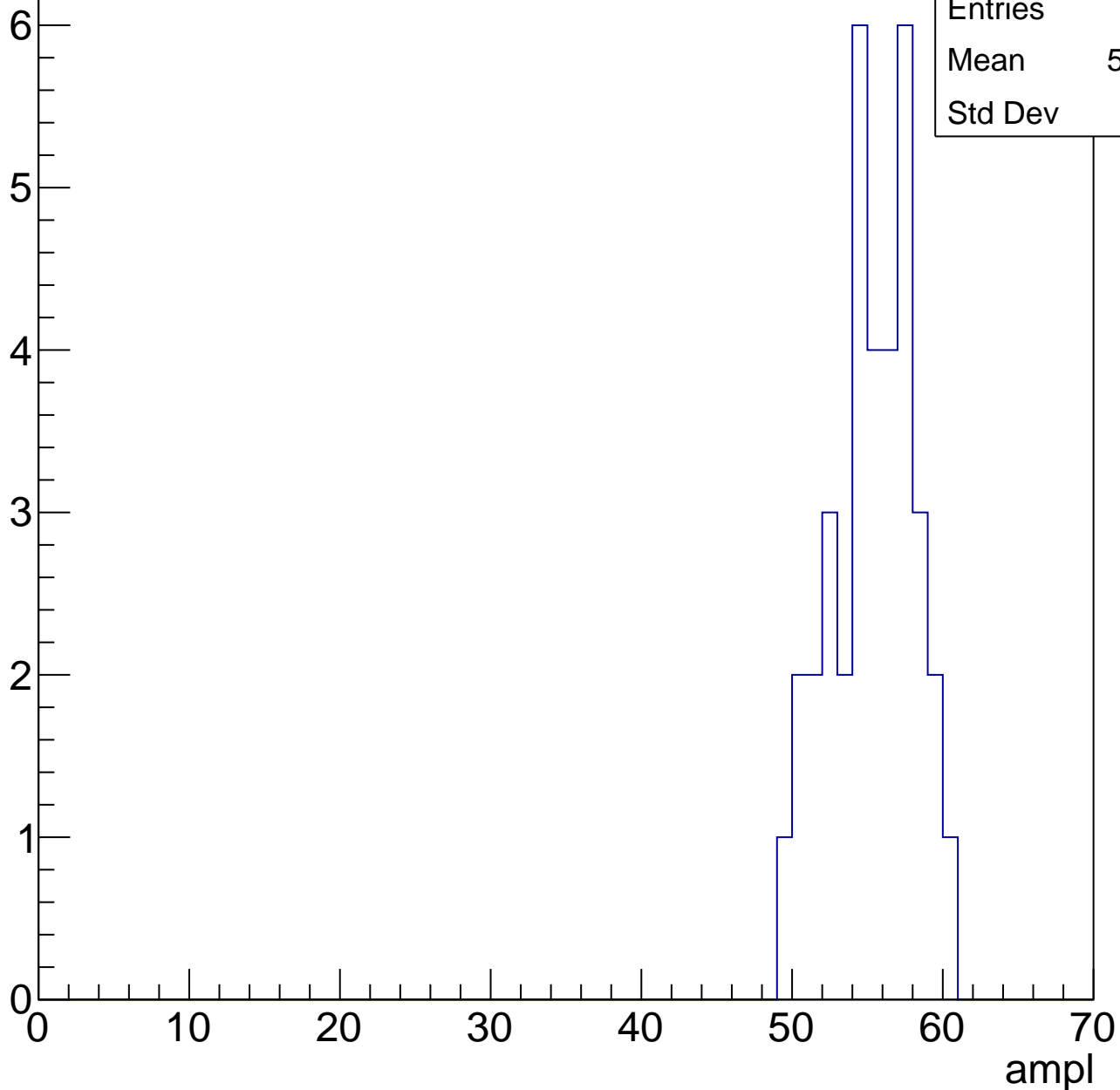


# B1L103S, U25-ch118, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	36
Mean	54.86
Std Dev	2.74



# B1L103S, U25-ch118, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	60
Mean	58.43
Std Dev	3.461

Entry

10

8

6

4

2

0

0

10

20

30

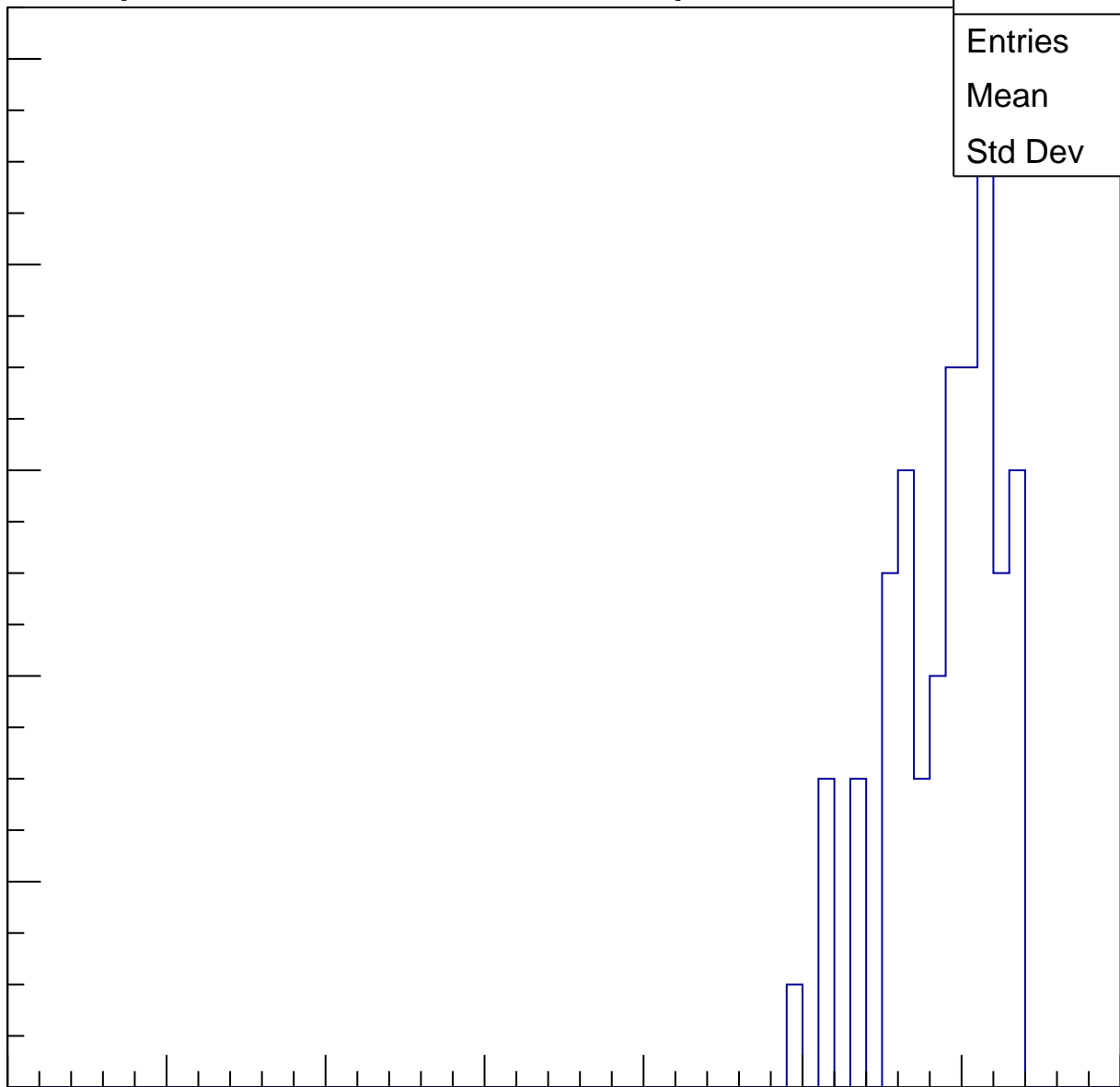
40

50

60

70

ampl

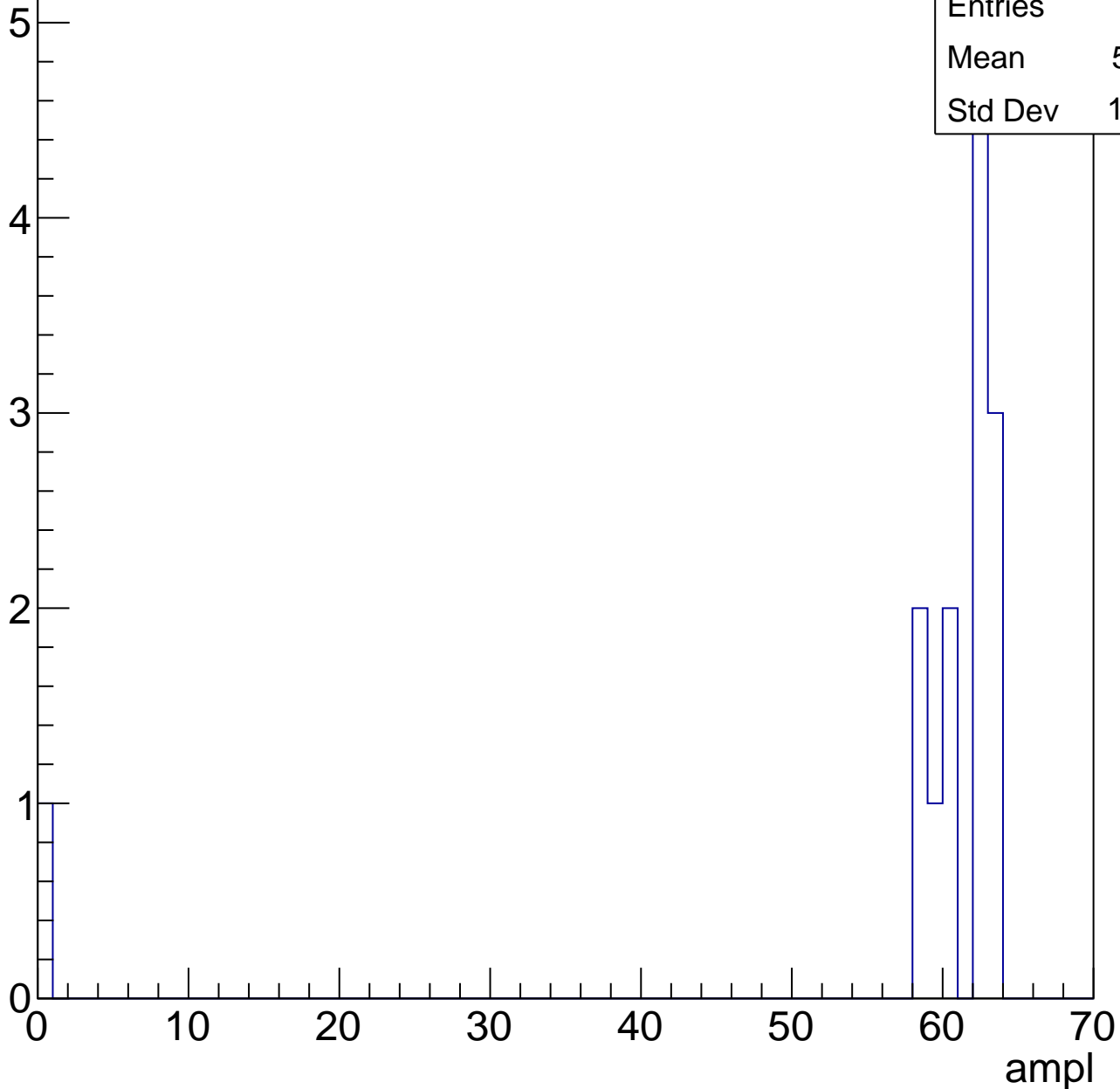


# B1L103S, U25-ch118, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	14
Mean	56.71
Std Dev	15.82





# B1L103S, U25-ch118, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	20
Mean	3.15
Std Dev	13.73

Entry



# B1L103S, U25-ch119, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

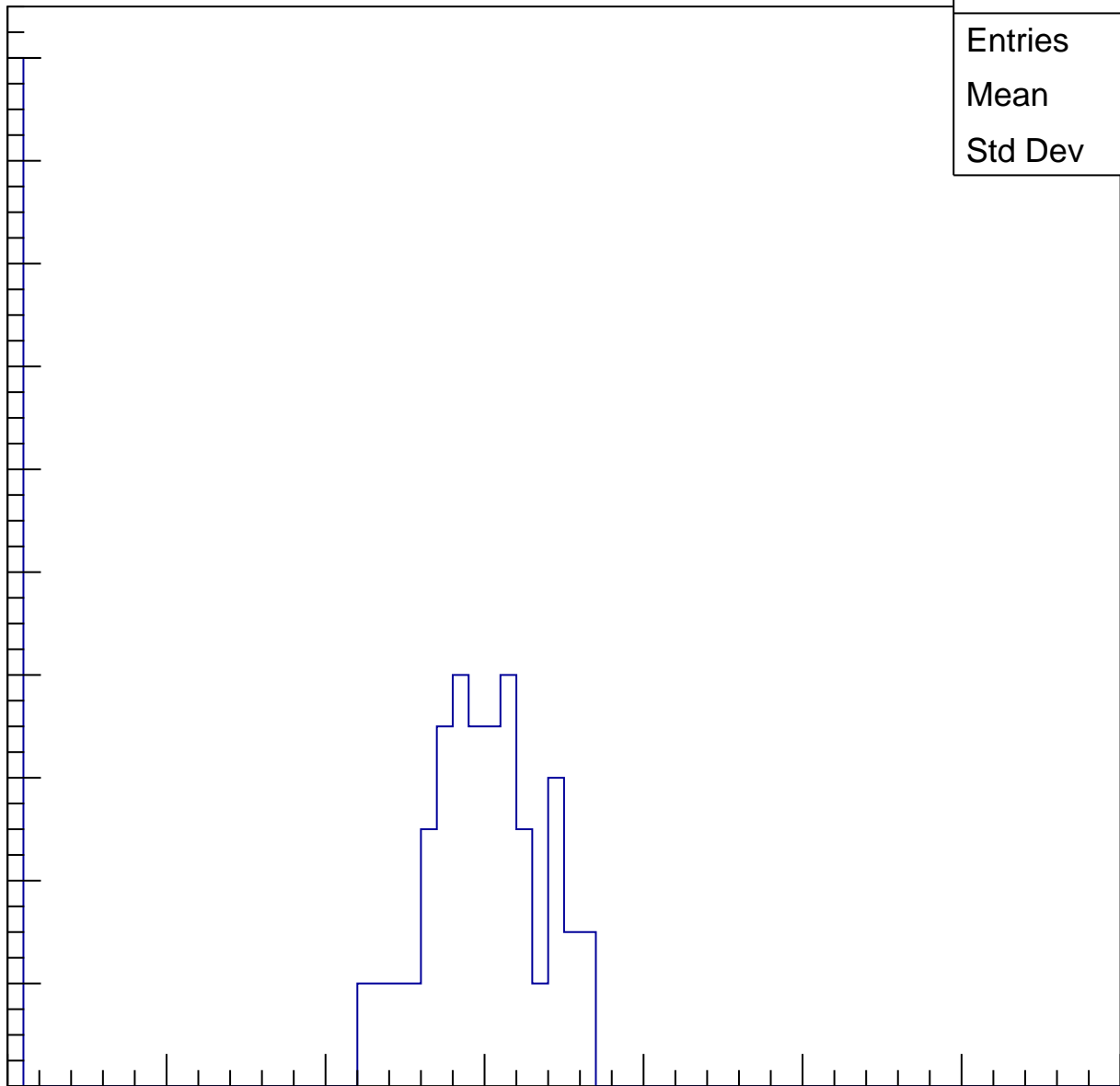
Entries	89
Mean	22.87
Std Dev	12.69

Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U25-ch119, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

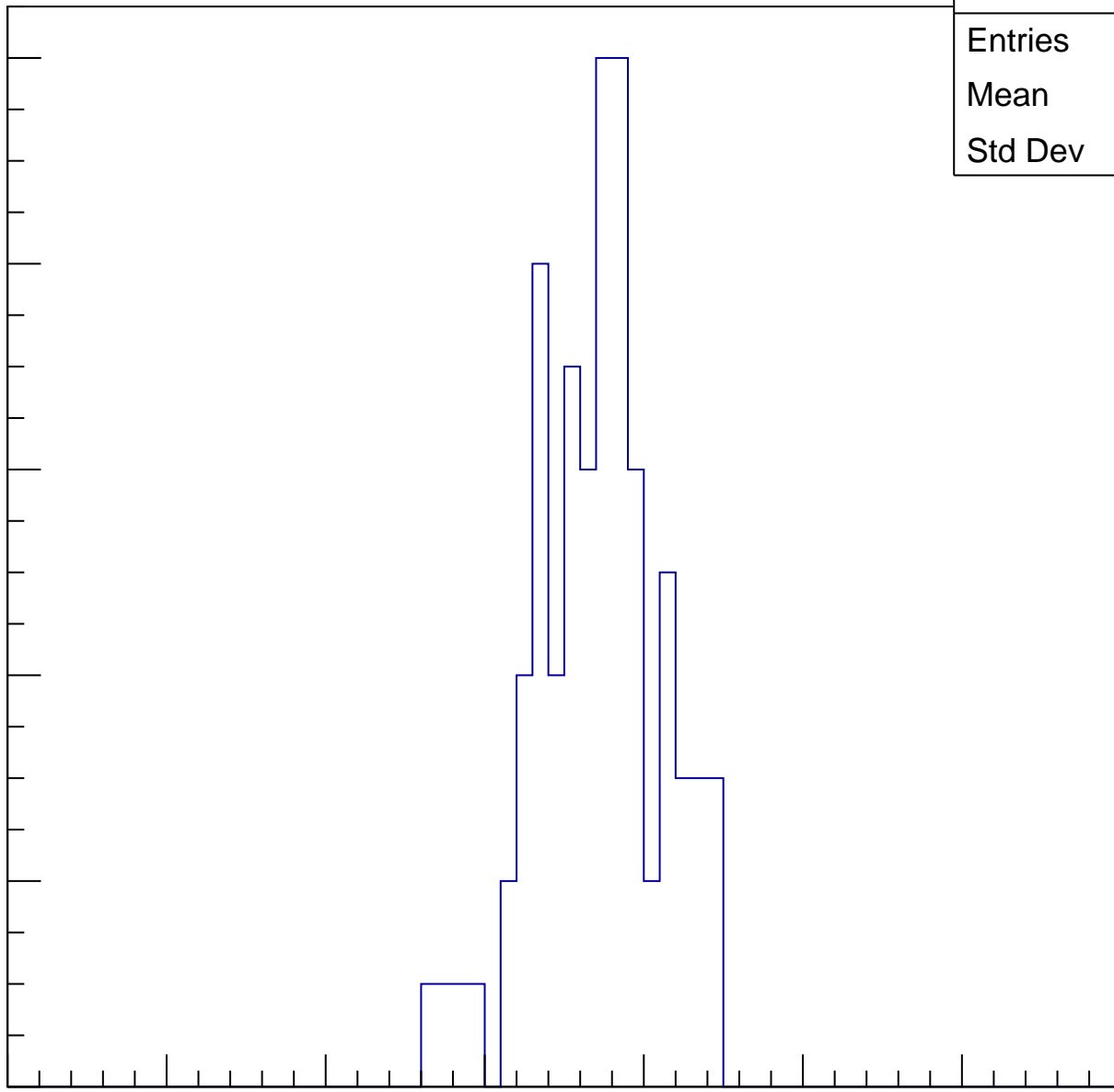
Entries	77
Mean	36.58
Std Dev	3.922

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

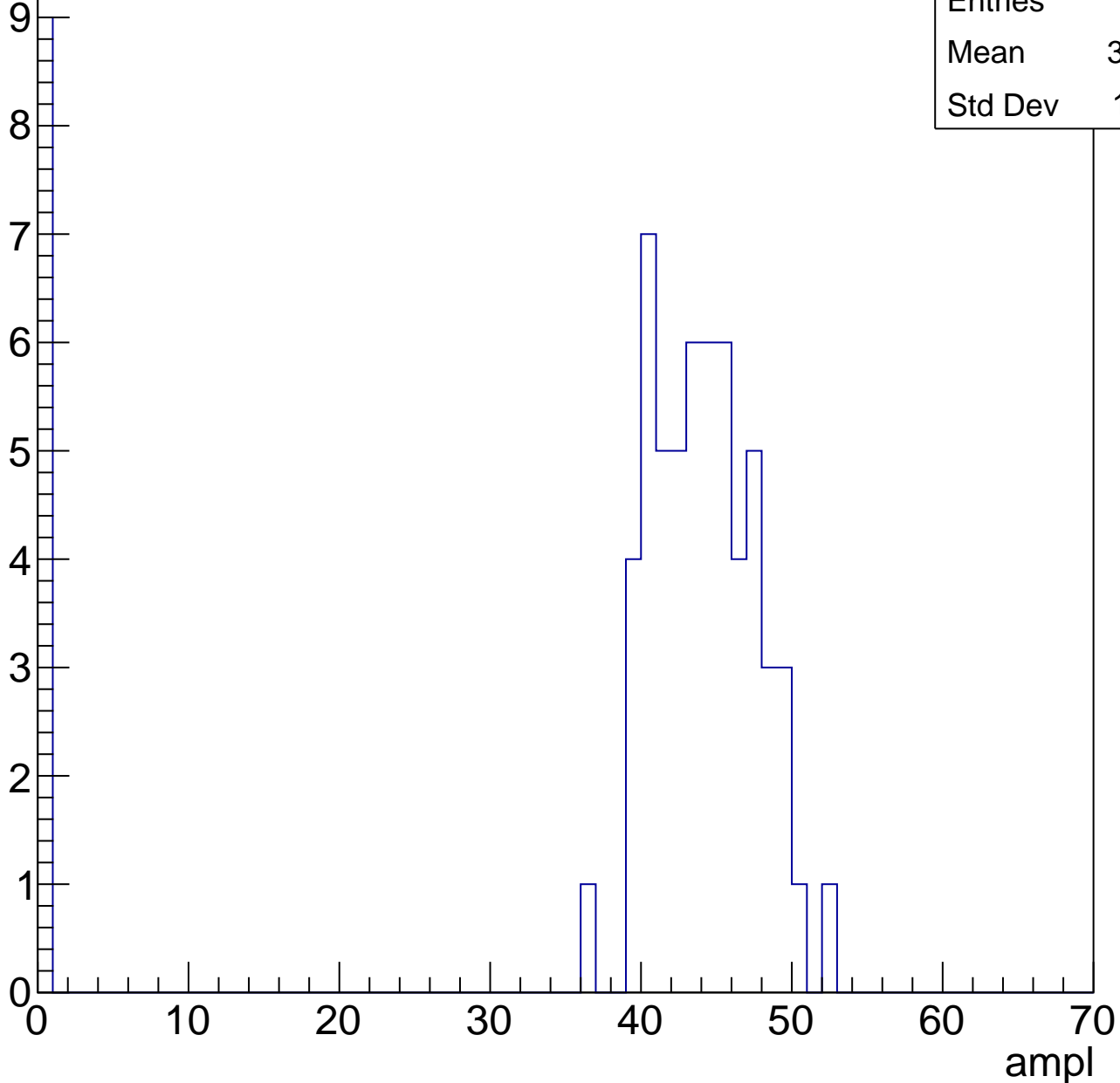


# B1L103S, U25-ch119, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	66
Mean	37.74
Std Dev	15.31

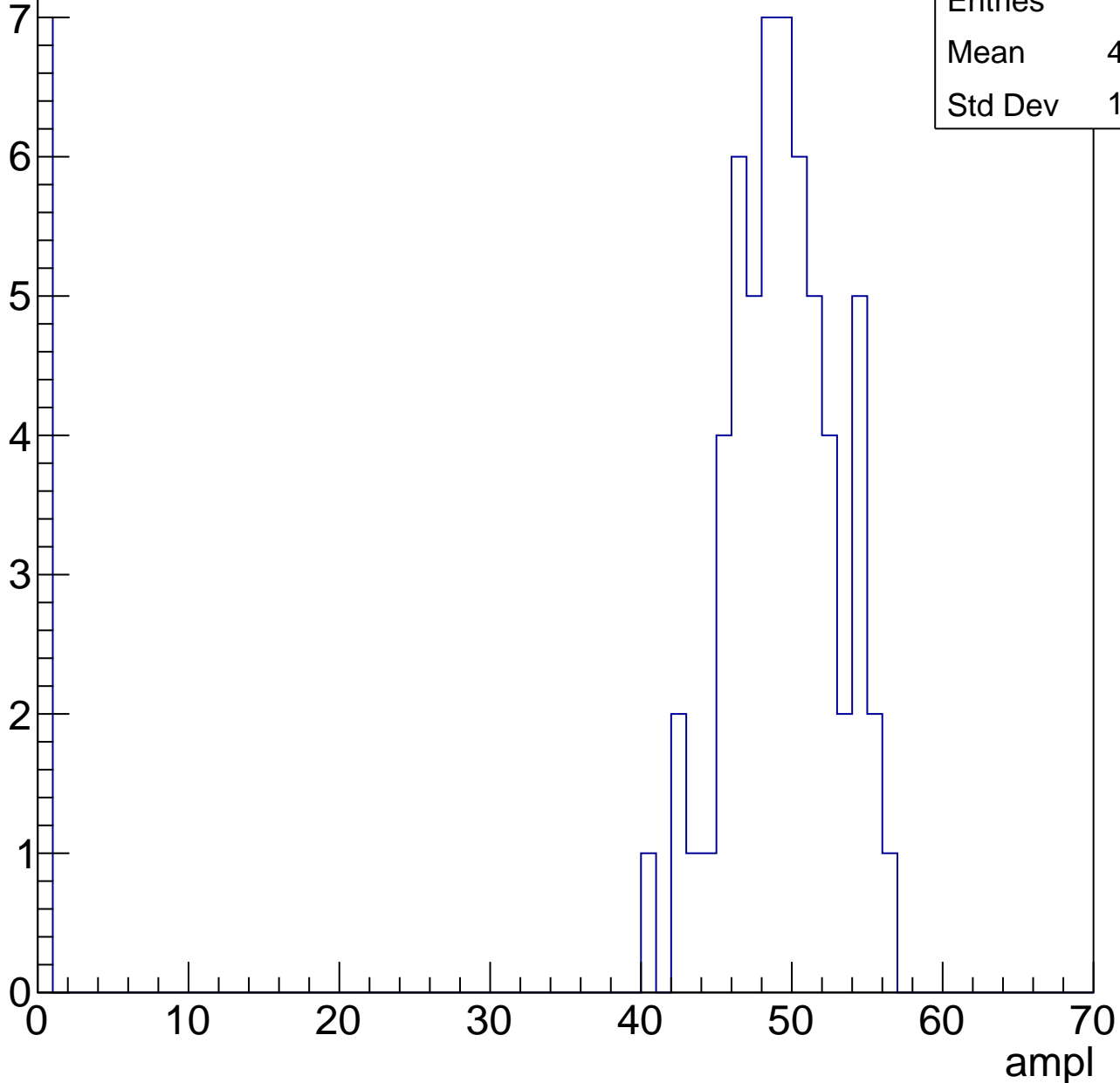


# B1L103S, U25-ch119, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	66
Mean	43.73
Std Dev	15.42

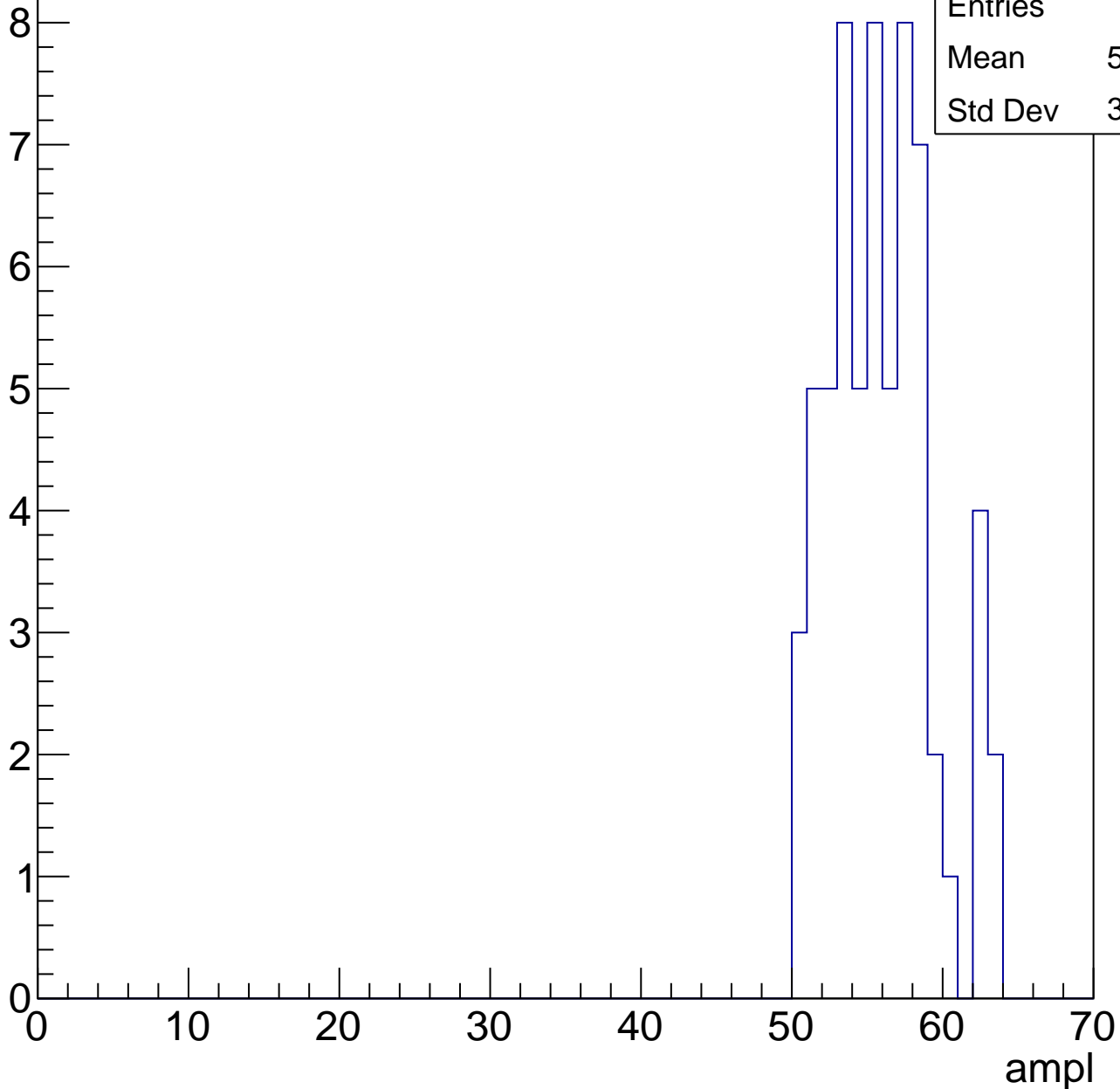


# B1L103S, U25-ch119, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	63
Mean	55.44
Std Dev	3.347

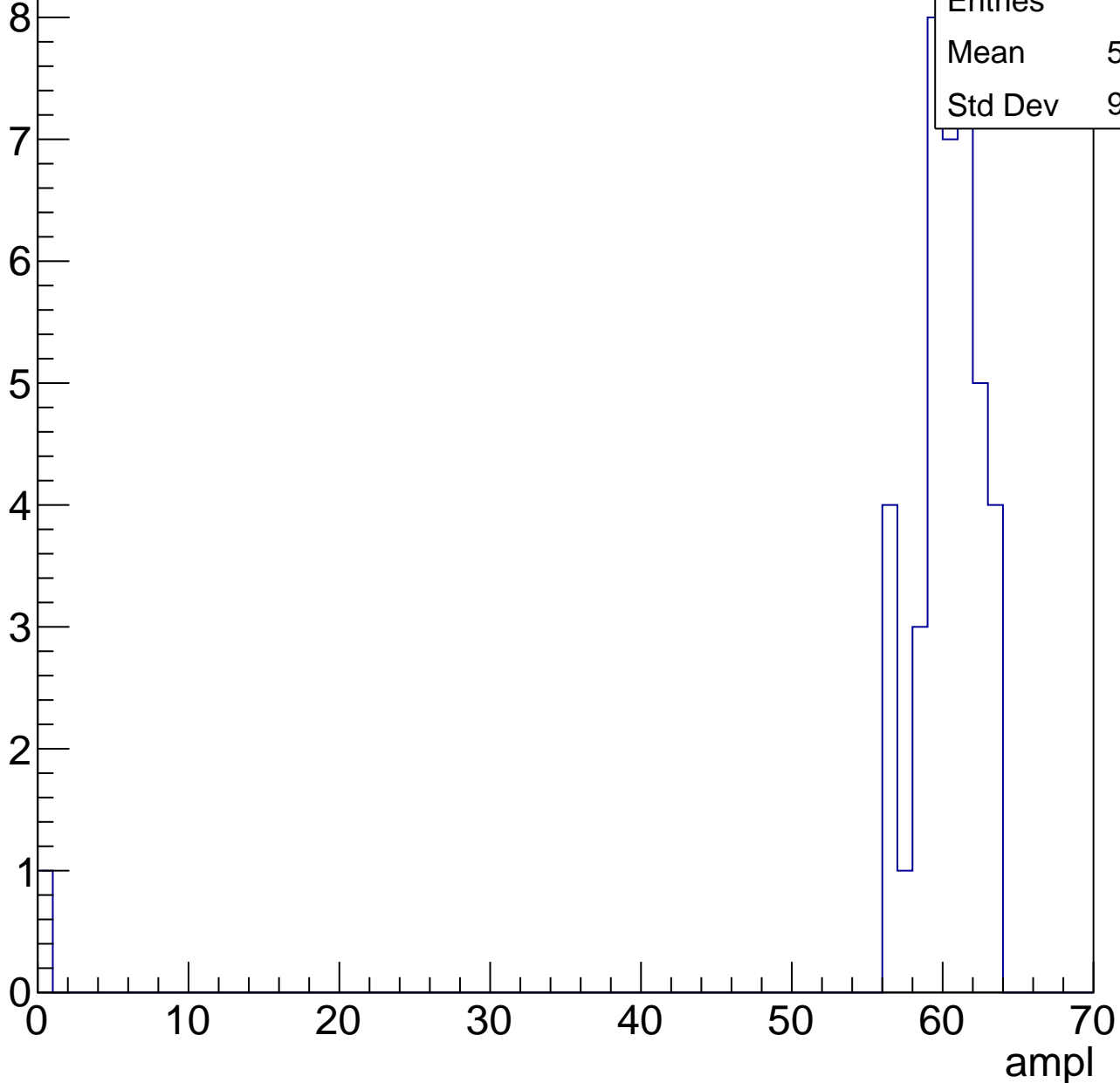


# B1L103S, U25-ch119, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

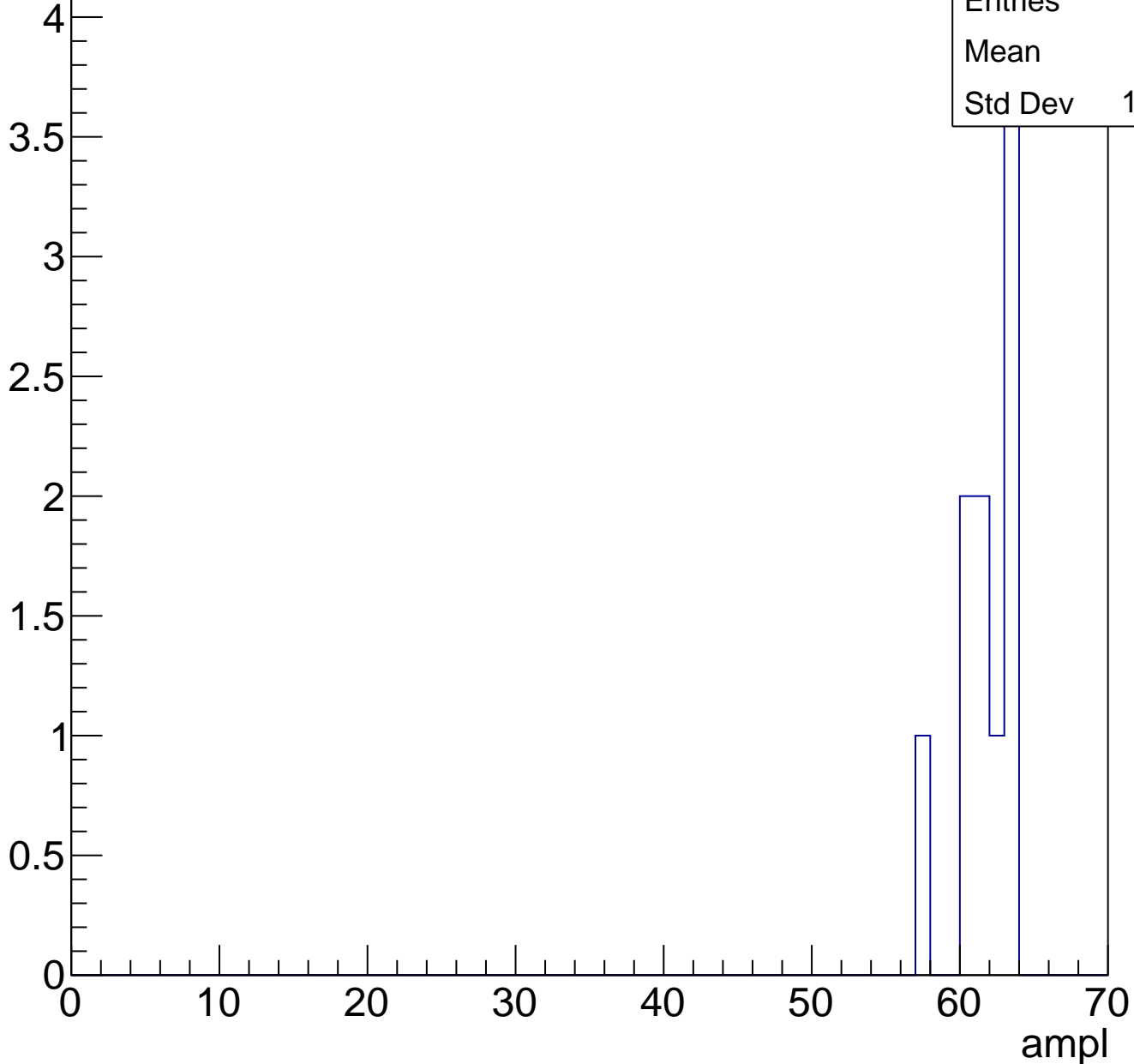
Entries	41
Mean	58.46
Std Dev	9.448



# B1L103S, U25-ch119, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U25-ch119, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Entries	19
Mean	0
Std Dev	0

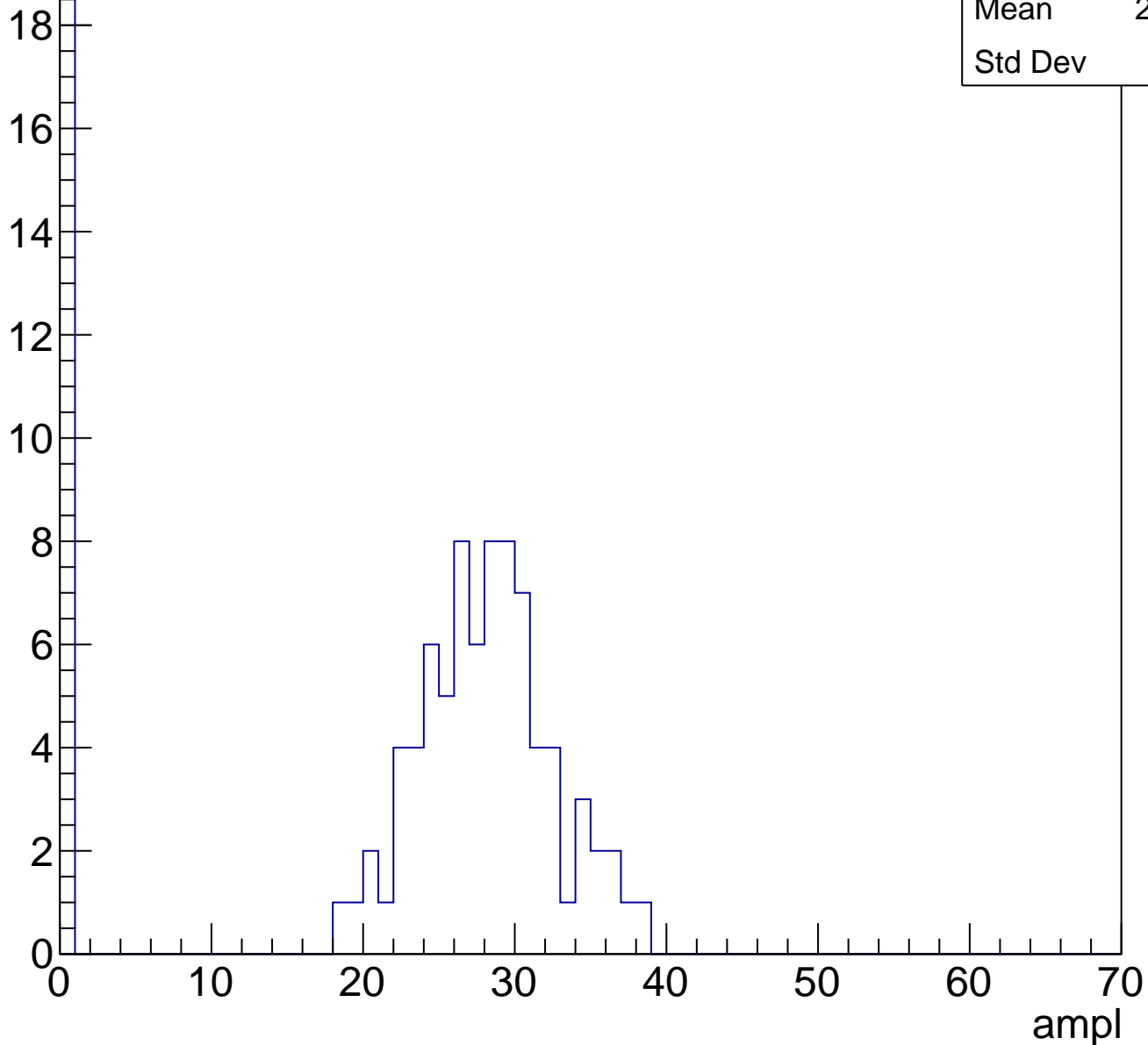
ampl

# B1L103S, U25-ch120, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	98
Mean	22.32
Std Dev	11.6

Entry

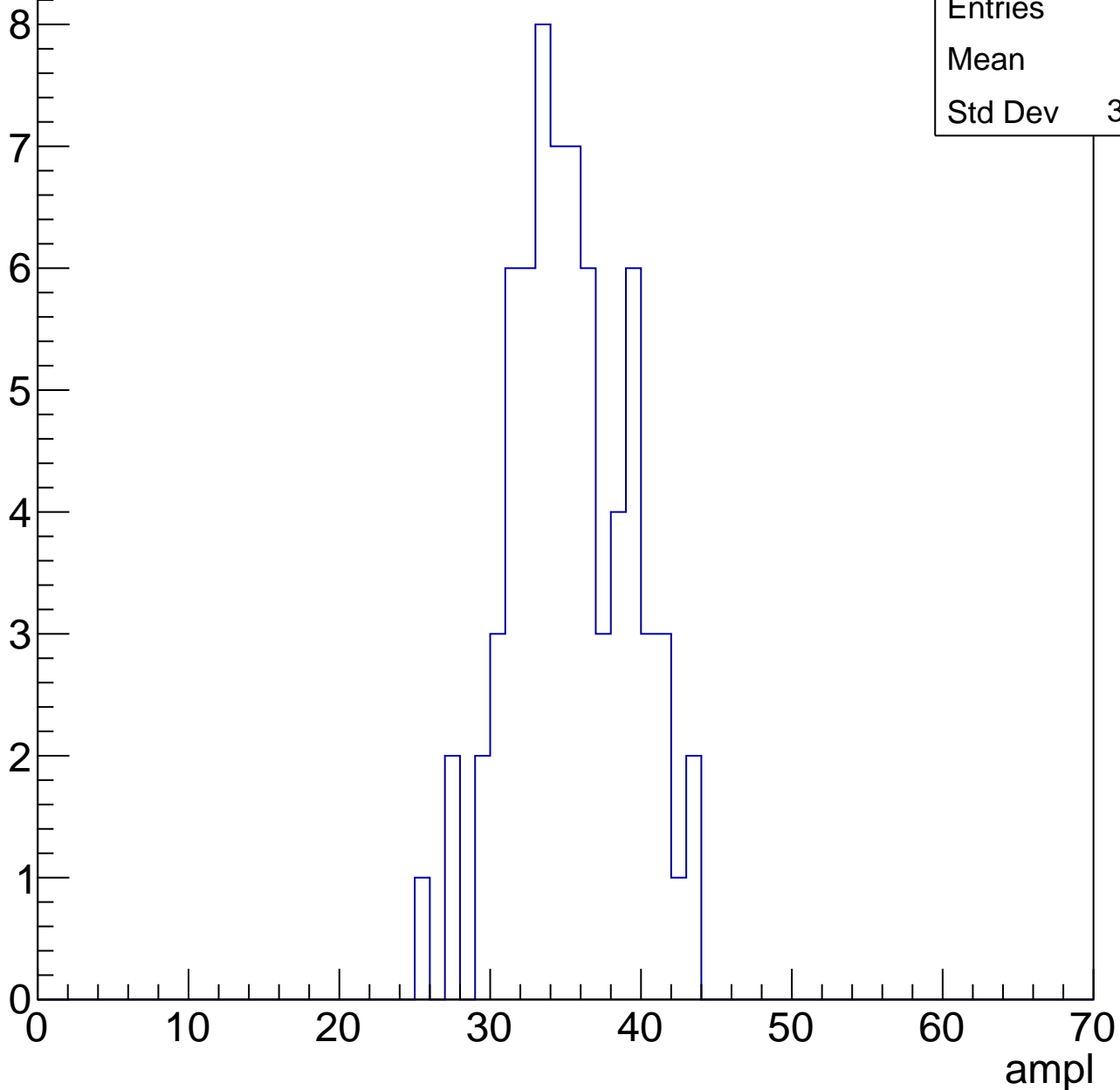


# B1L103S, U25-ch120, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	70
Mean	34.8
Std Dev	3.912

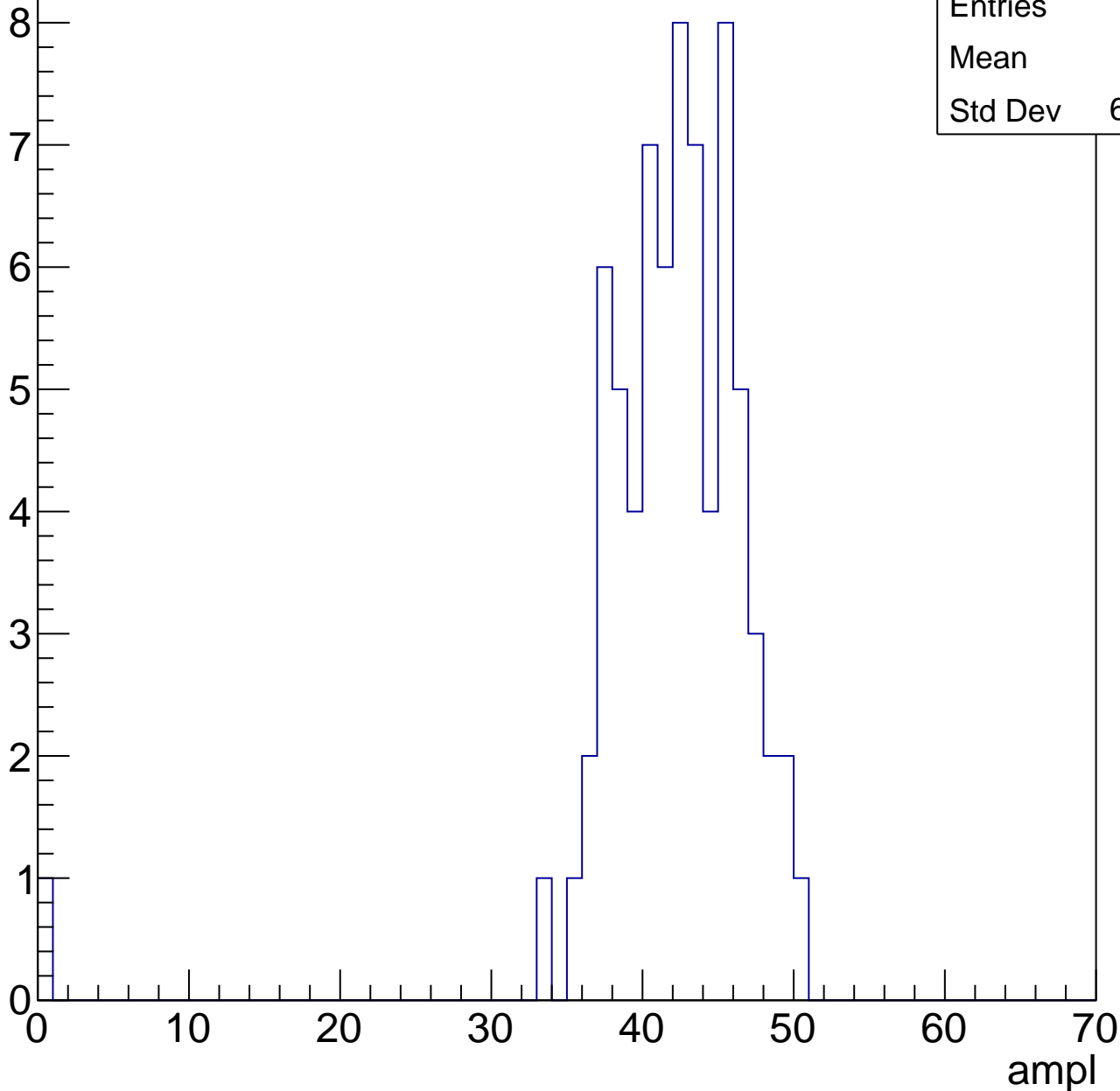


# B1L103S, U25-ch120, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	73
Mean	41.4
Std Dev	6.108

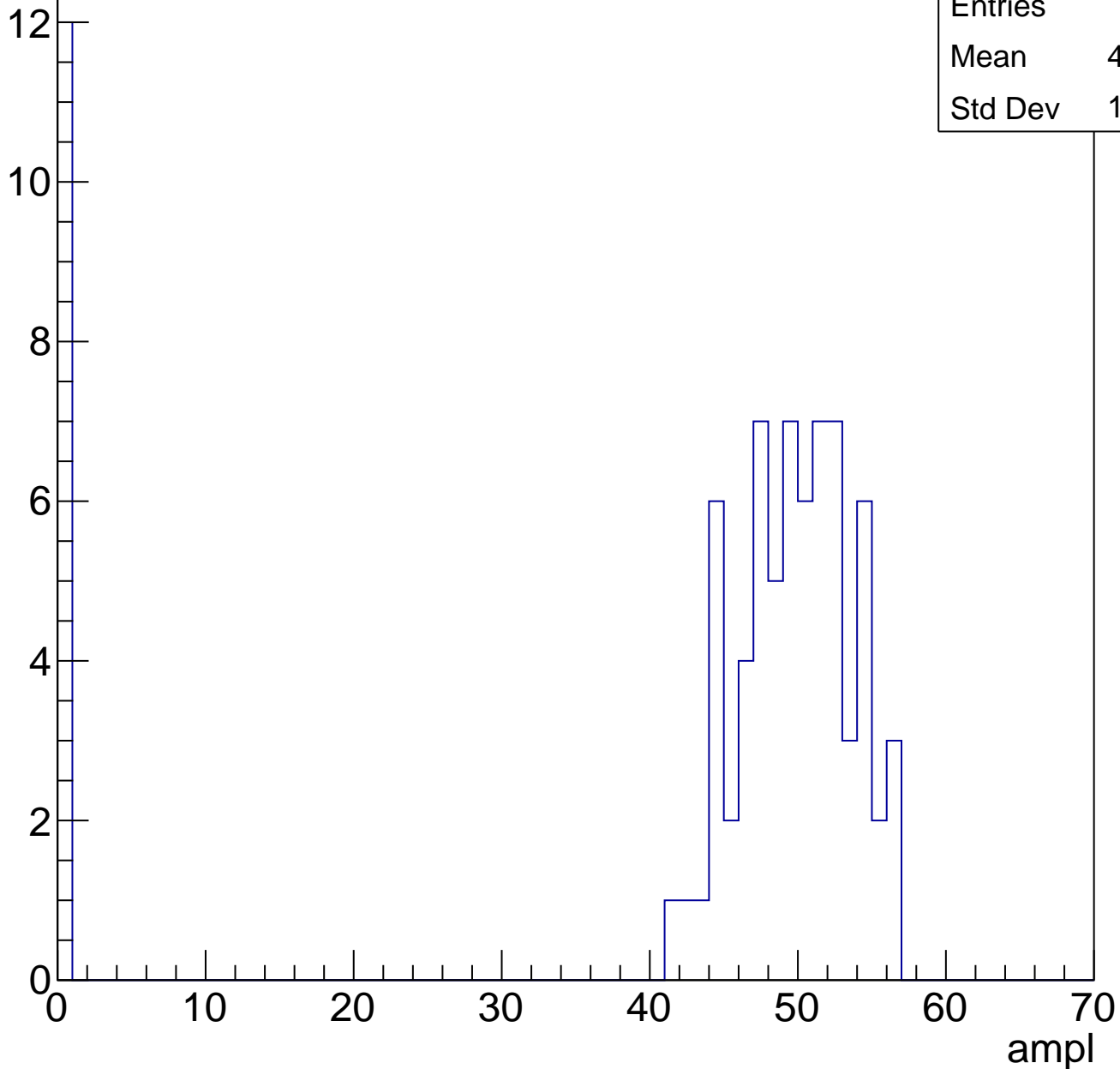


# B1L103S, U25-ch120, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	80
Mean	41.98
Std Dev	17.95

Entry

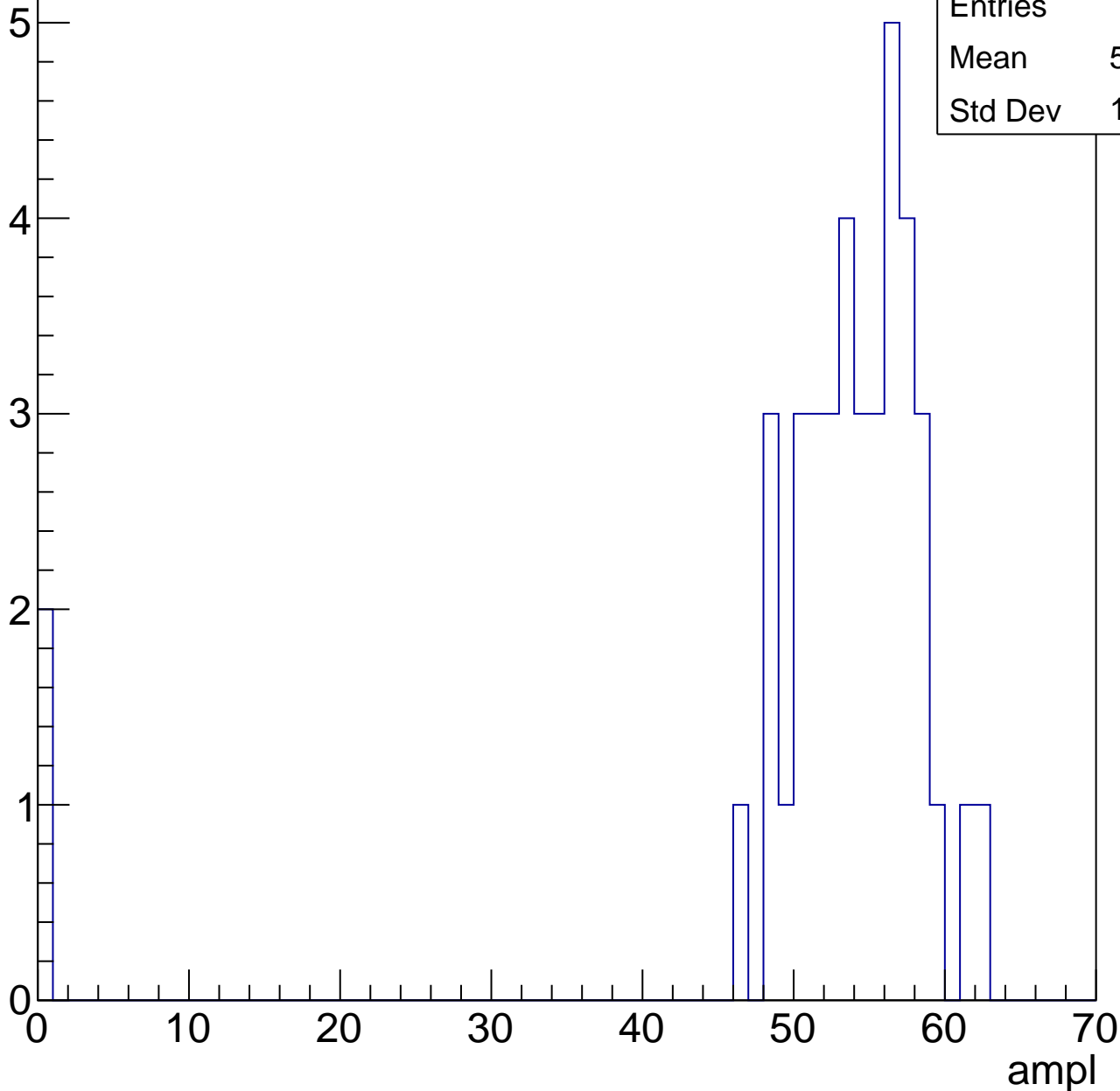


# B1L103S, U25-ch120, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

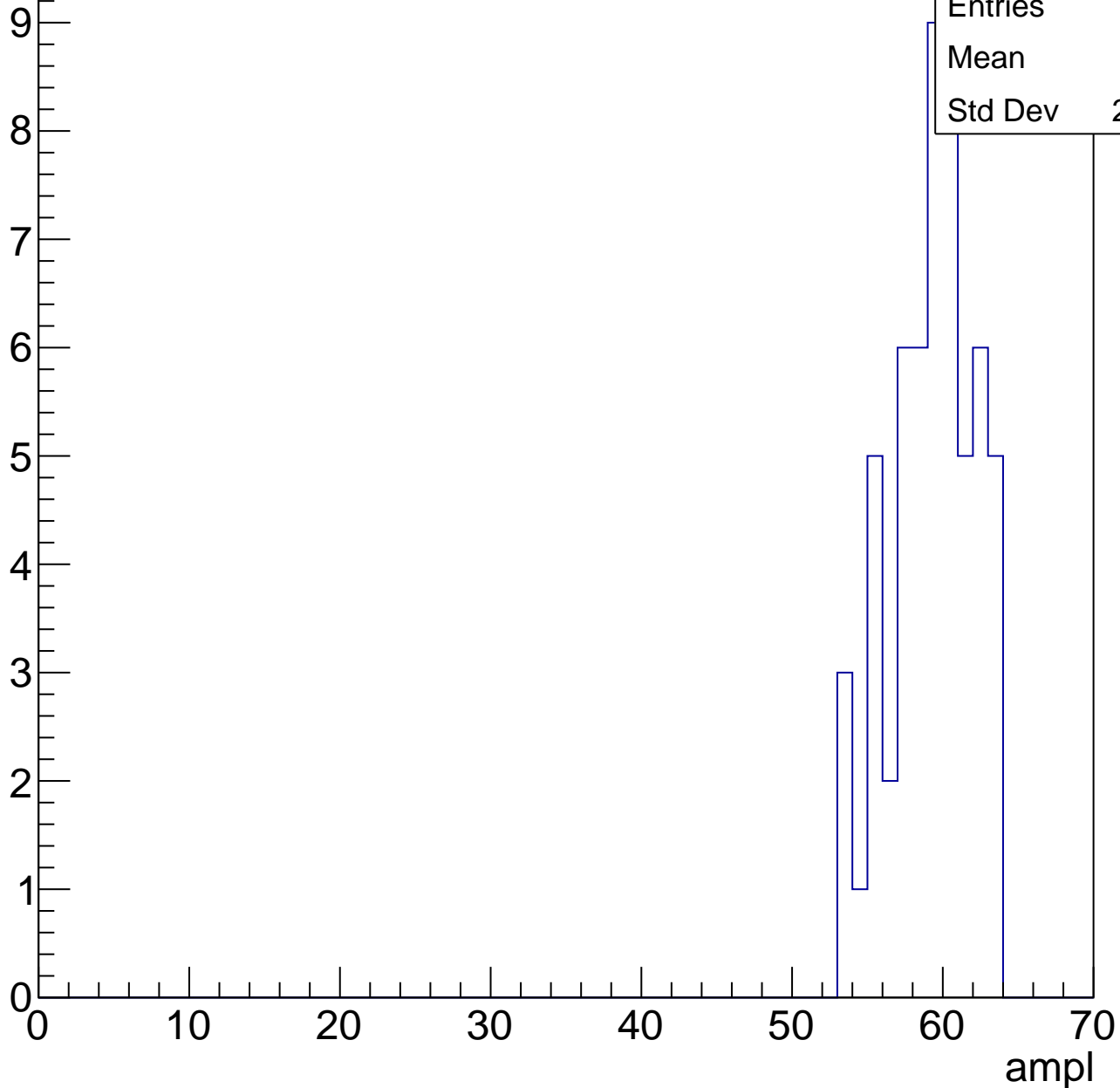
Entries	41
Mean	51.24
Std Dev	12.15



# B1L103S, U25-ch120, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

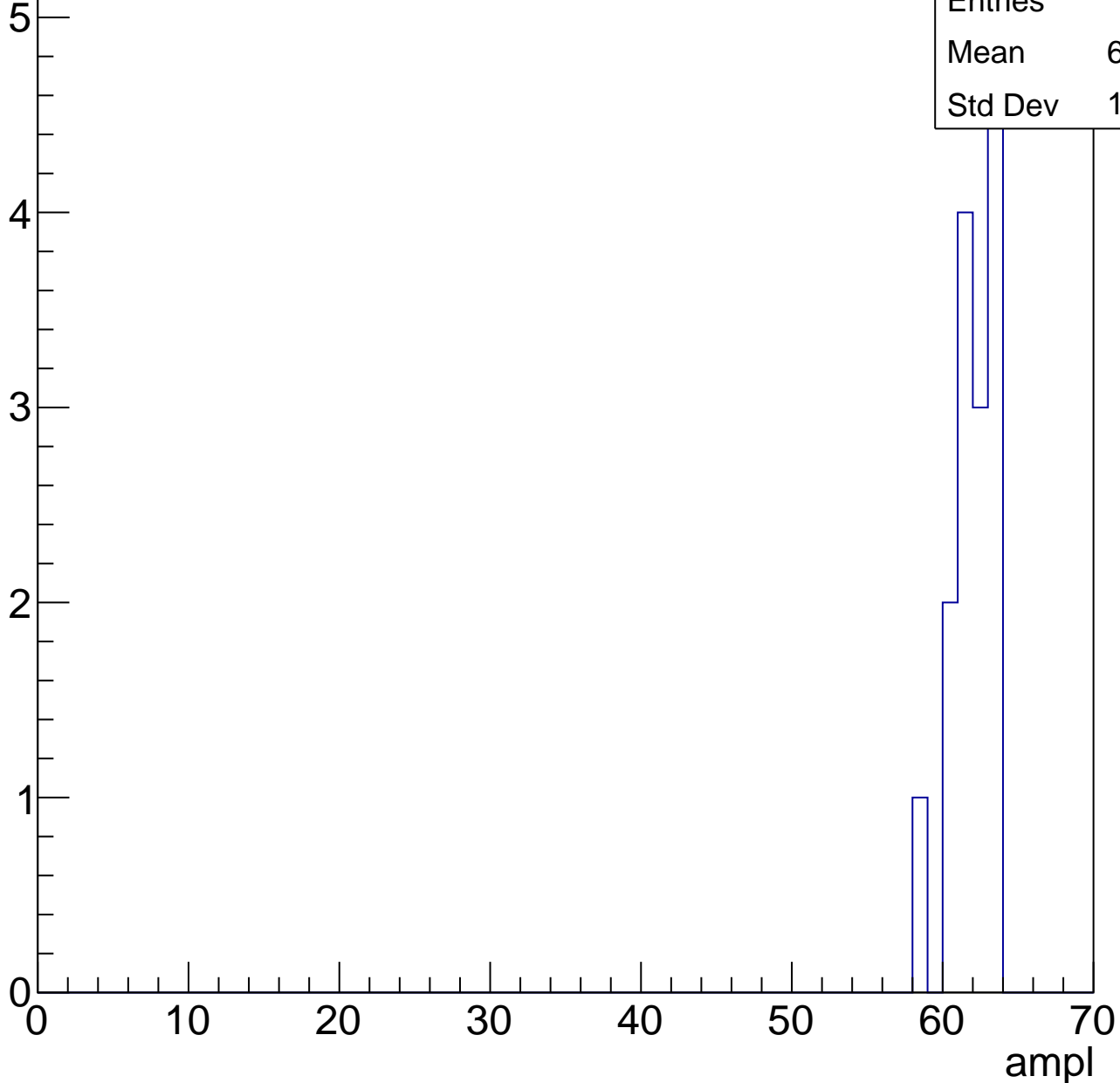


# B1L103S, U25-ch120, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	15
Mean	61.53
Std Dev	1.408





# B1L103S, U25-ch120, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

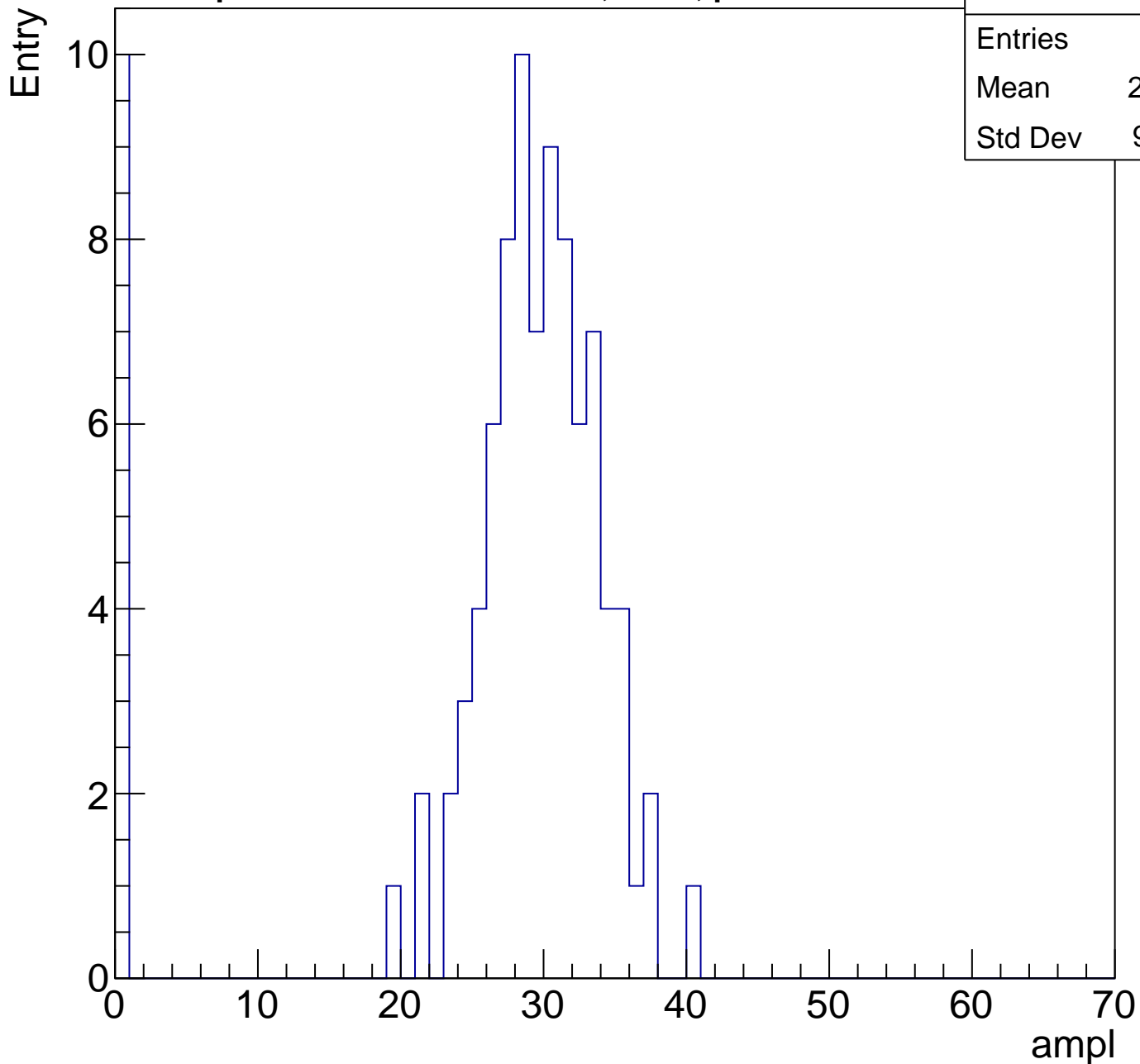
Entries	20
Mean	0
Std Dev	0

ampl

# B1L103S, U25-ch121, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	95
Mean	26.33
Std Dev	9.741

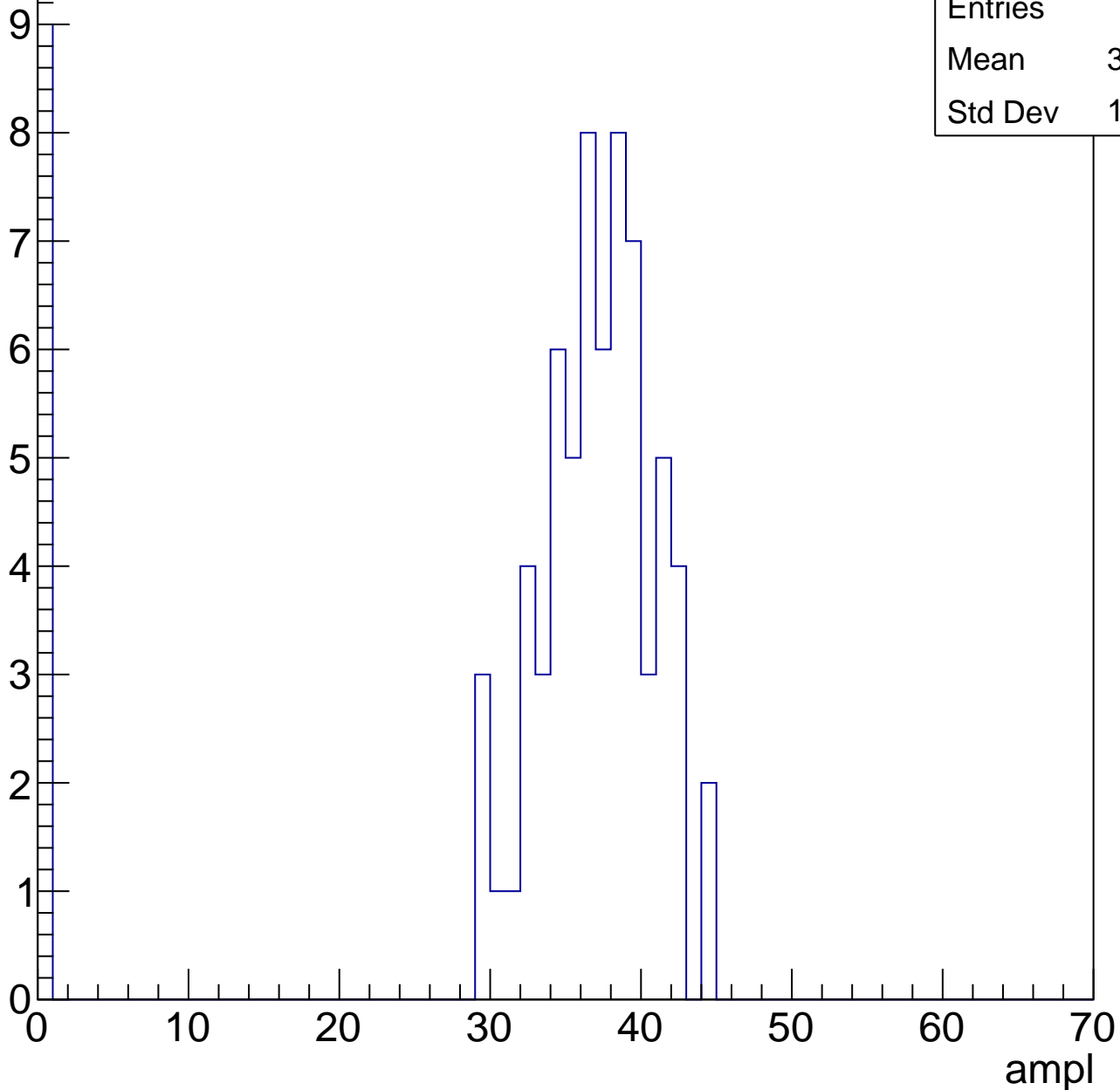


# B1L103S, U25-ch121, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	75
Mean	32.29
Std Dev	12.39

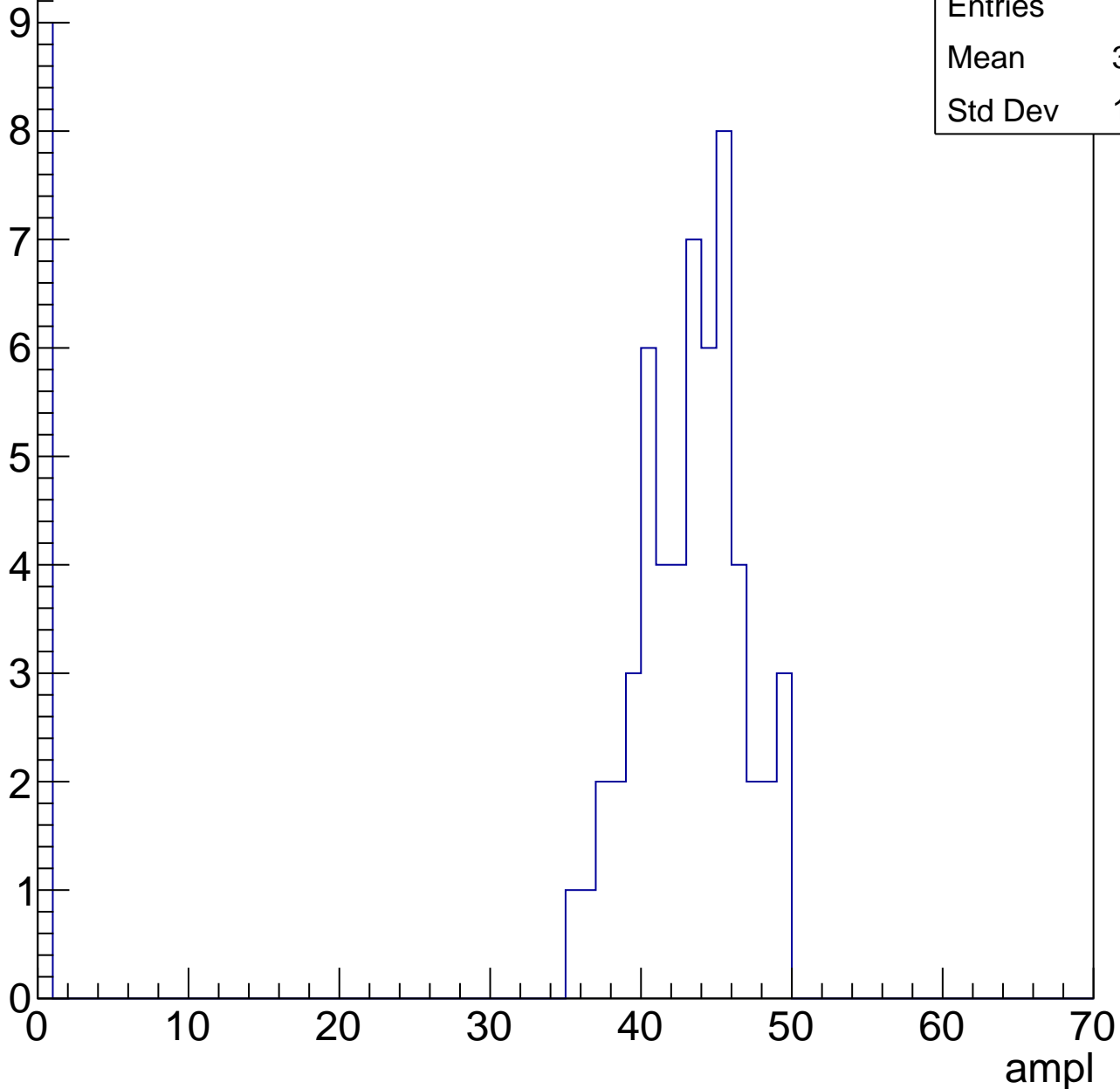


# B1L103S, U25-ch121, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	64
Mean	36.81
Std Dev	15.21

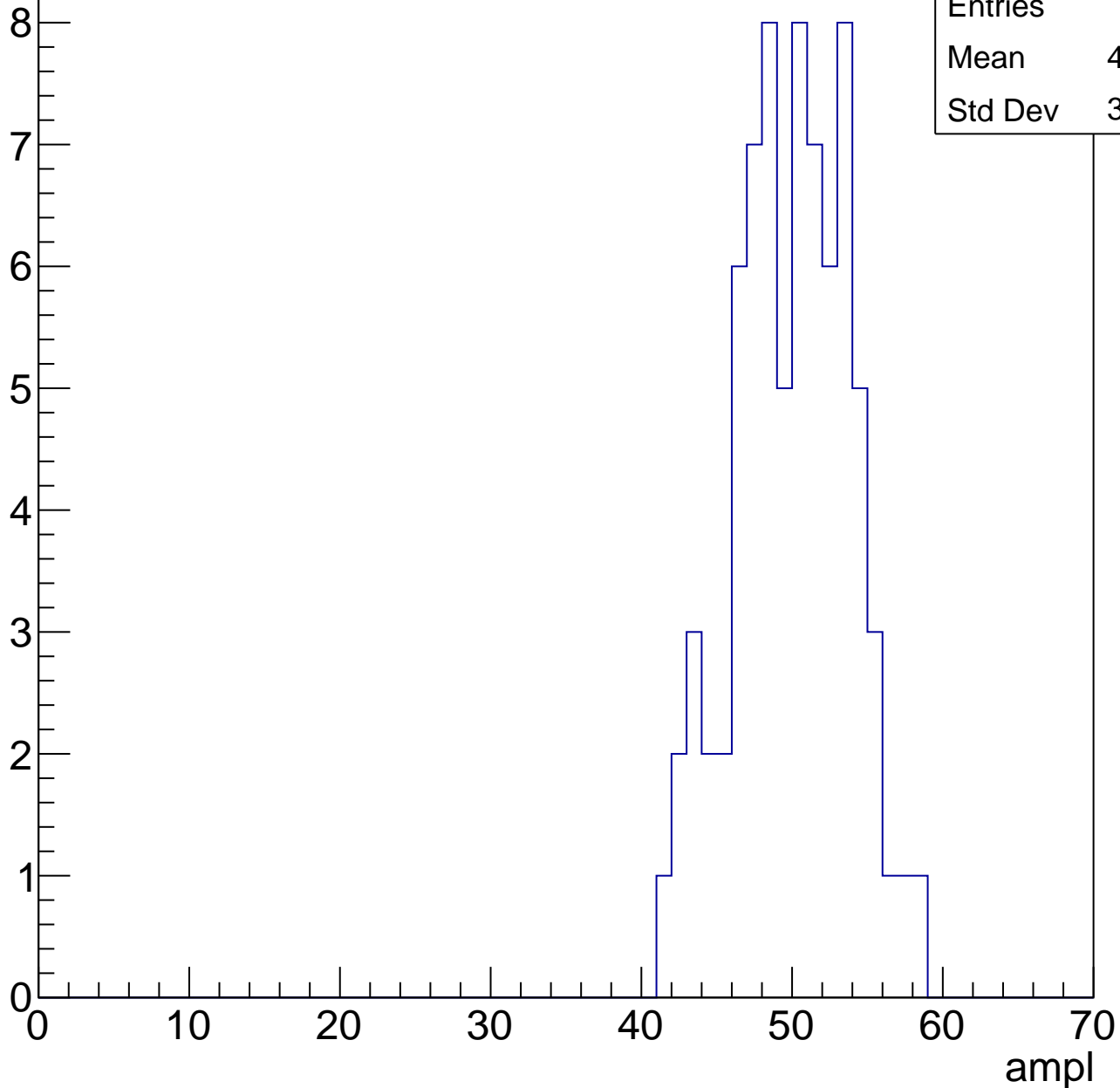


# B1L103S, U25-ch121, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	76
Mean	49.54
Std Dev	3.743

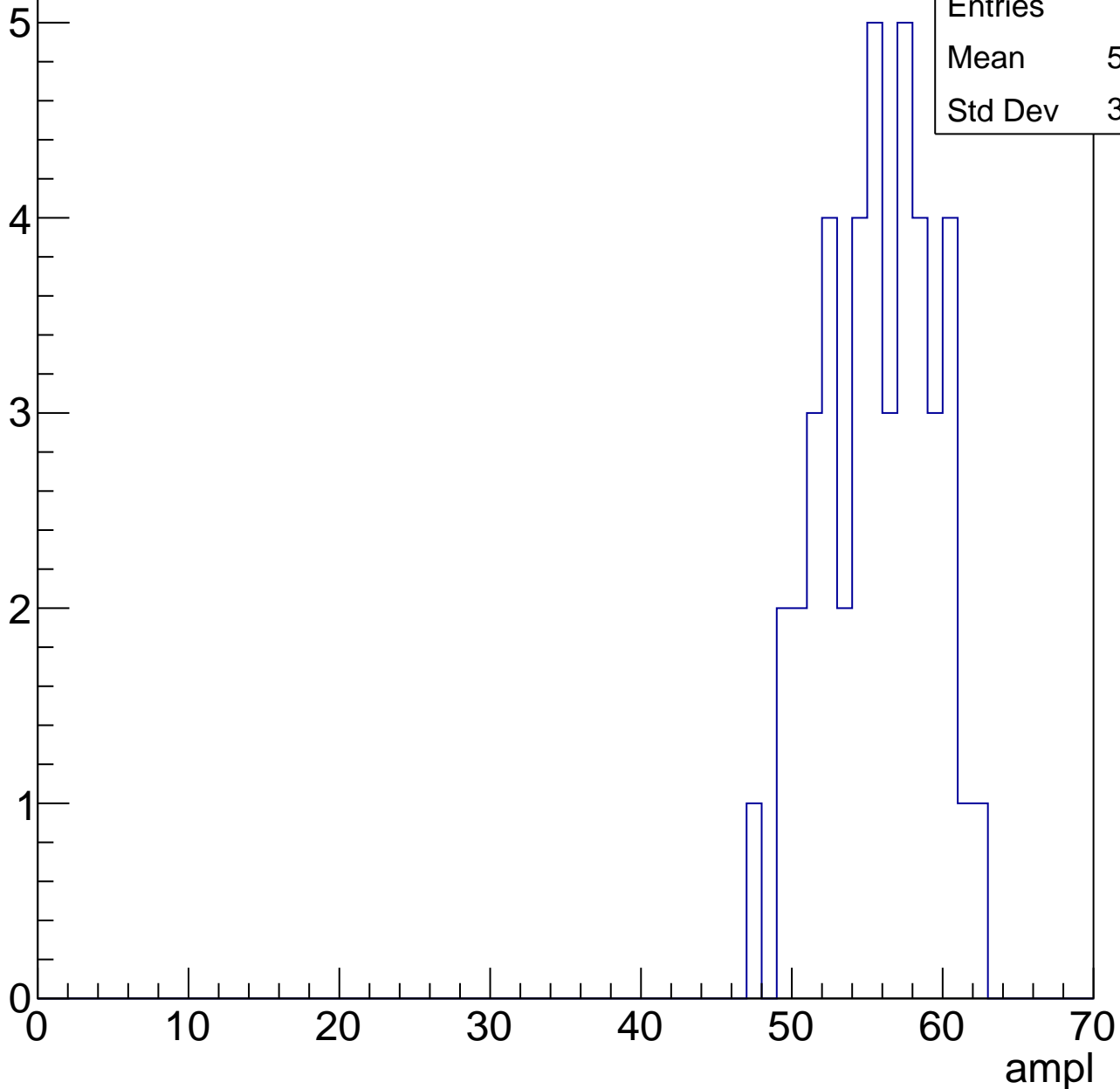


# B1L103S, U25-ch121, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	44
Mean	55.18
Std Dev	3.607

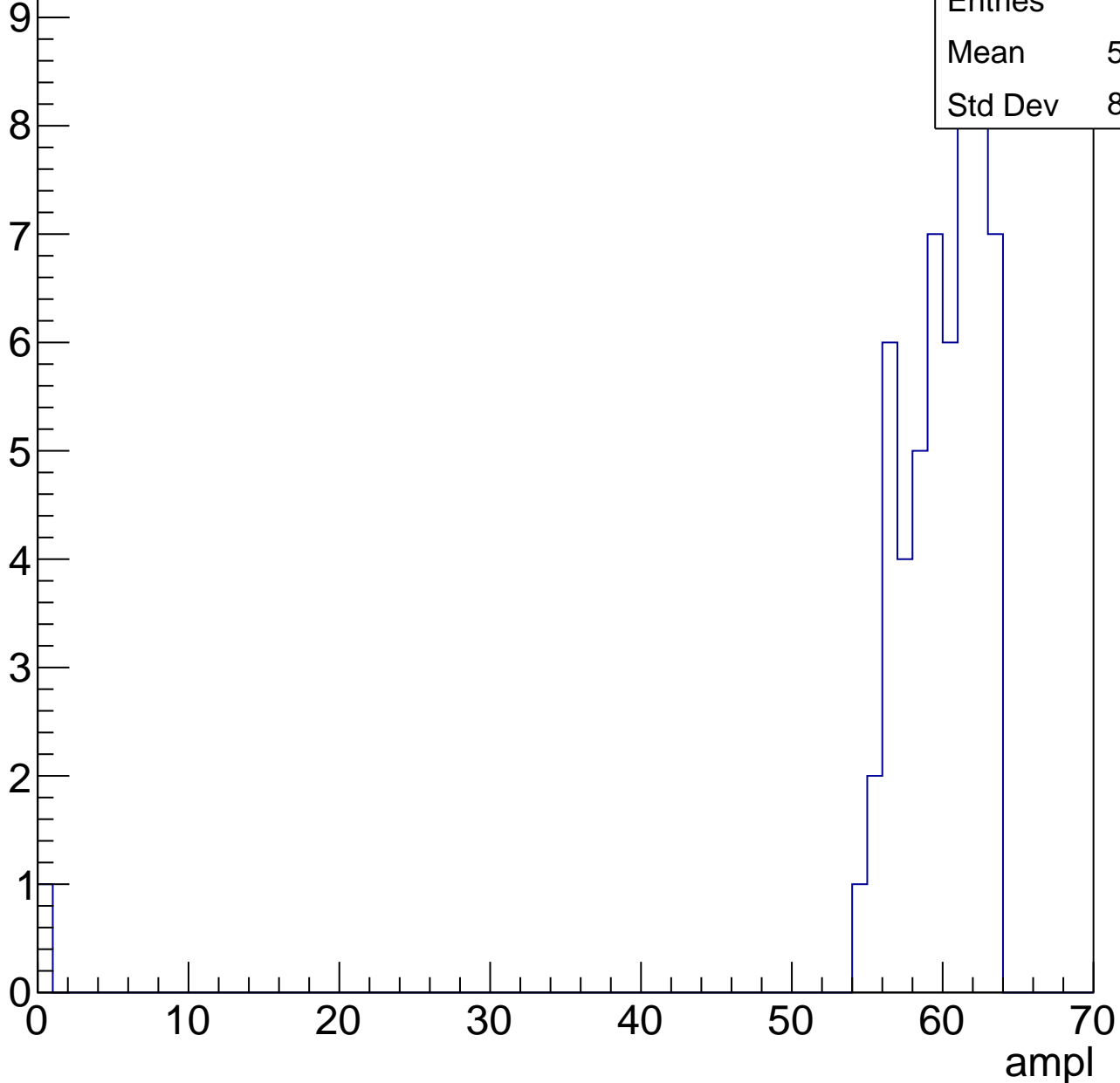


# B1L103S, U25-ch121, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	56
Mean	58.54
Std Dev	8.272



# B1L103S, U25-ch121, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U25-ch121, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

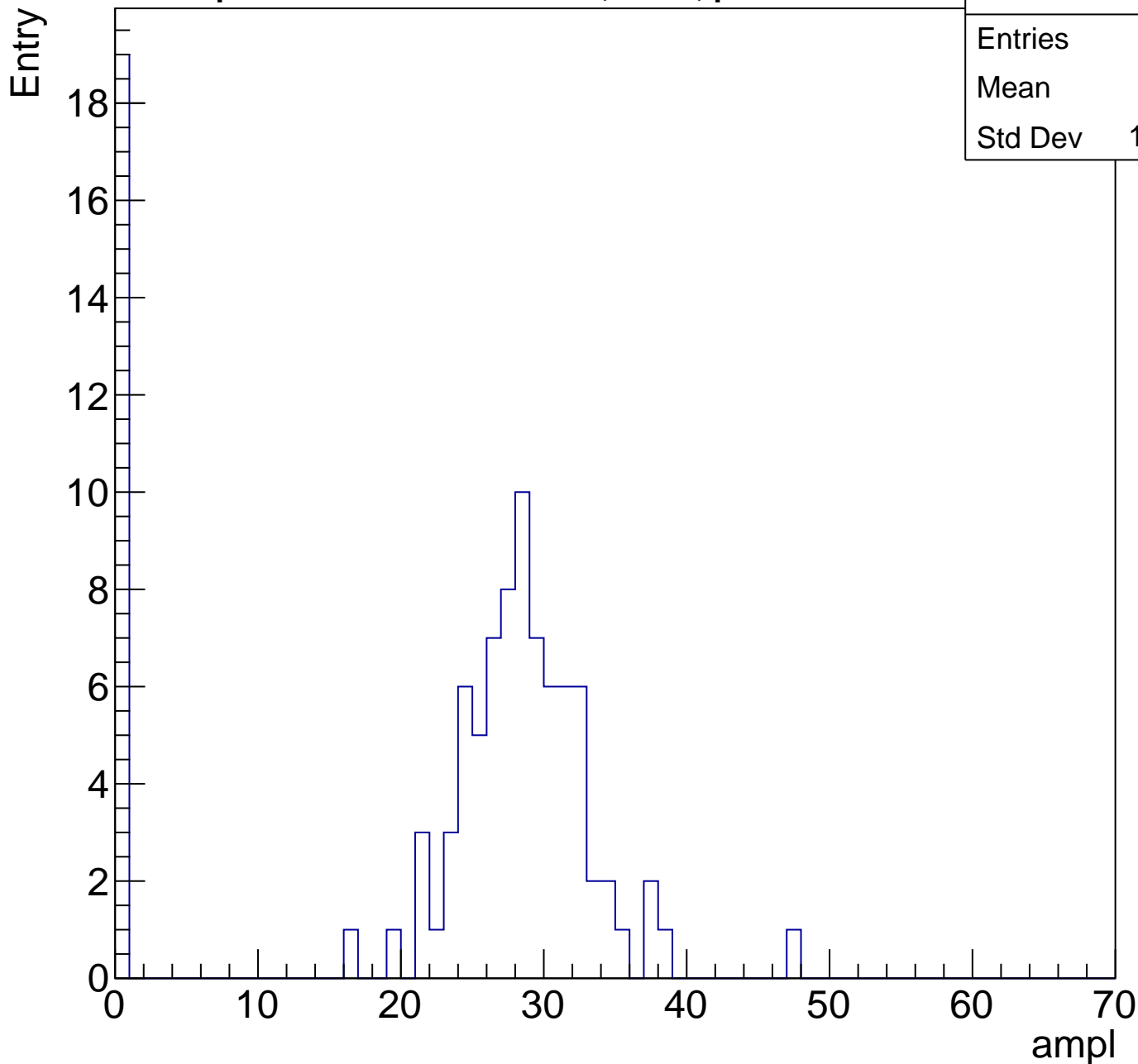
Entry



# B1L103S, U25-ch122, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	98
Mean	22.7
Std Dev	11.86



# B1L103S, U25-ch122, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

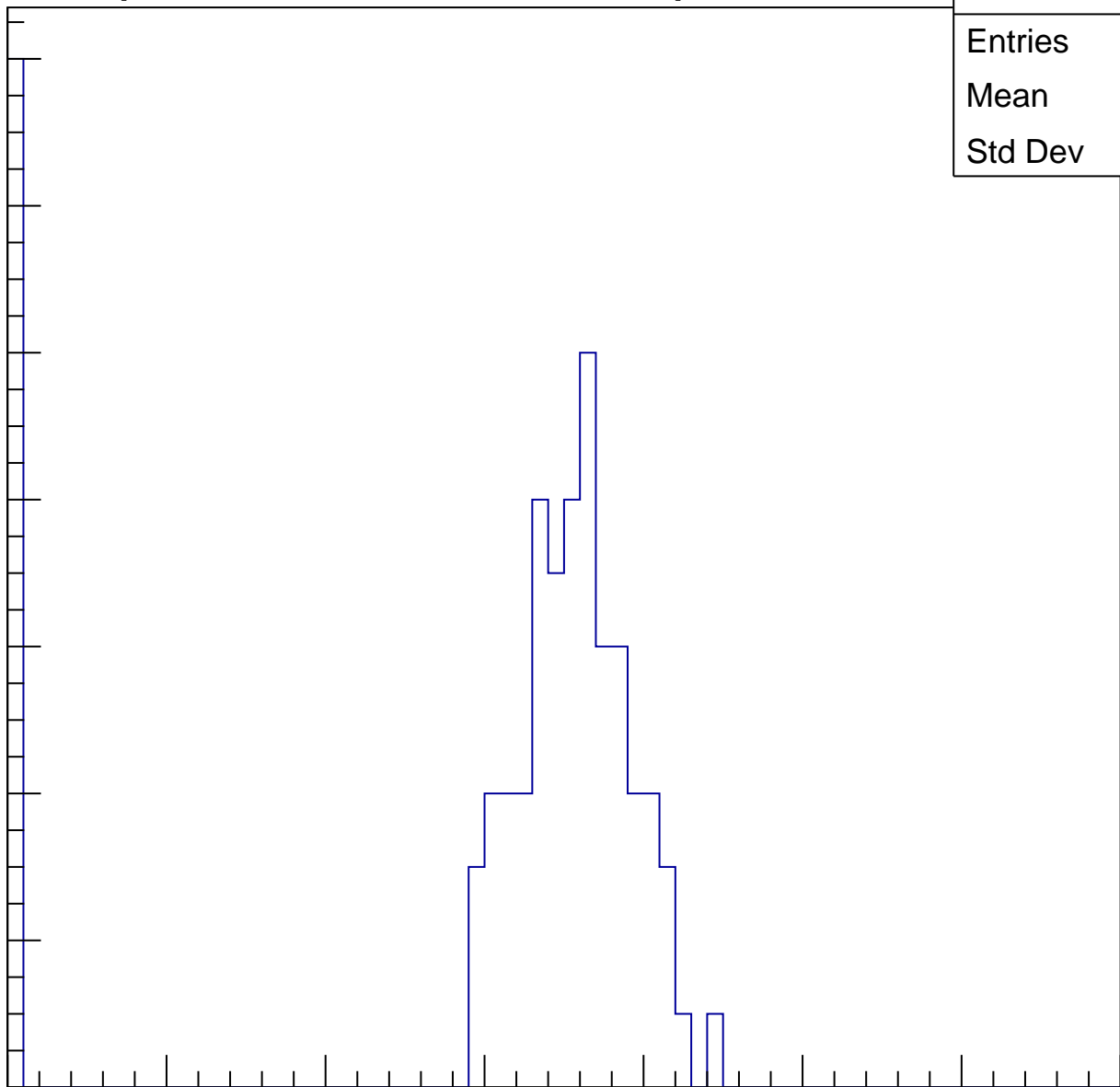
Entries	87
Mean	29.61
Std Dev	13.33

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

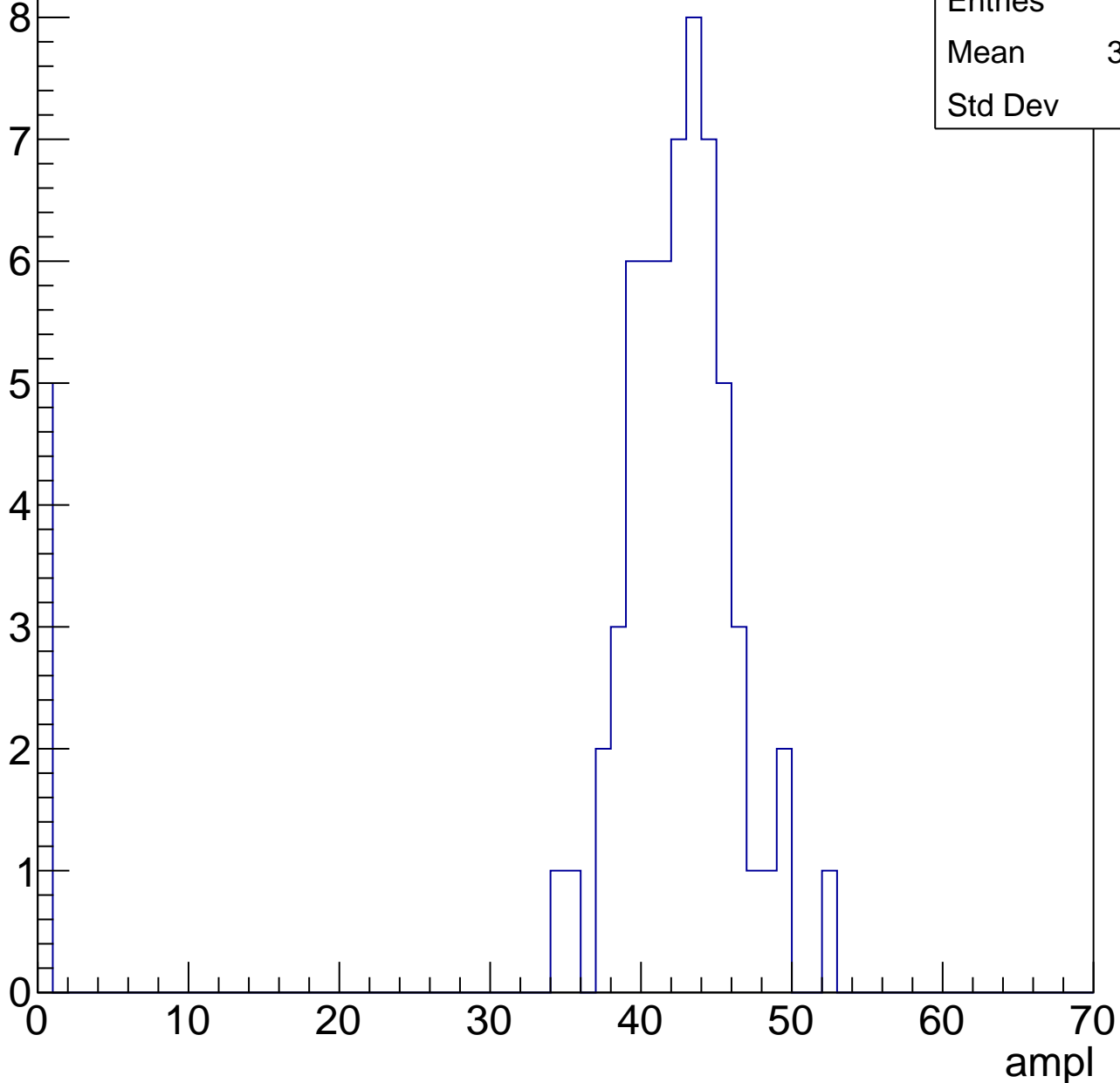


# B1L103S, U25-ch122, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	65
Mean	38.94
Std Dev	11.7

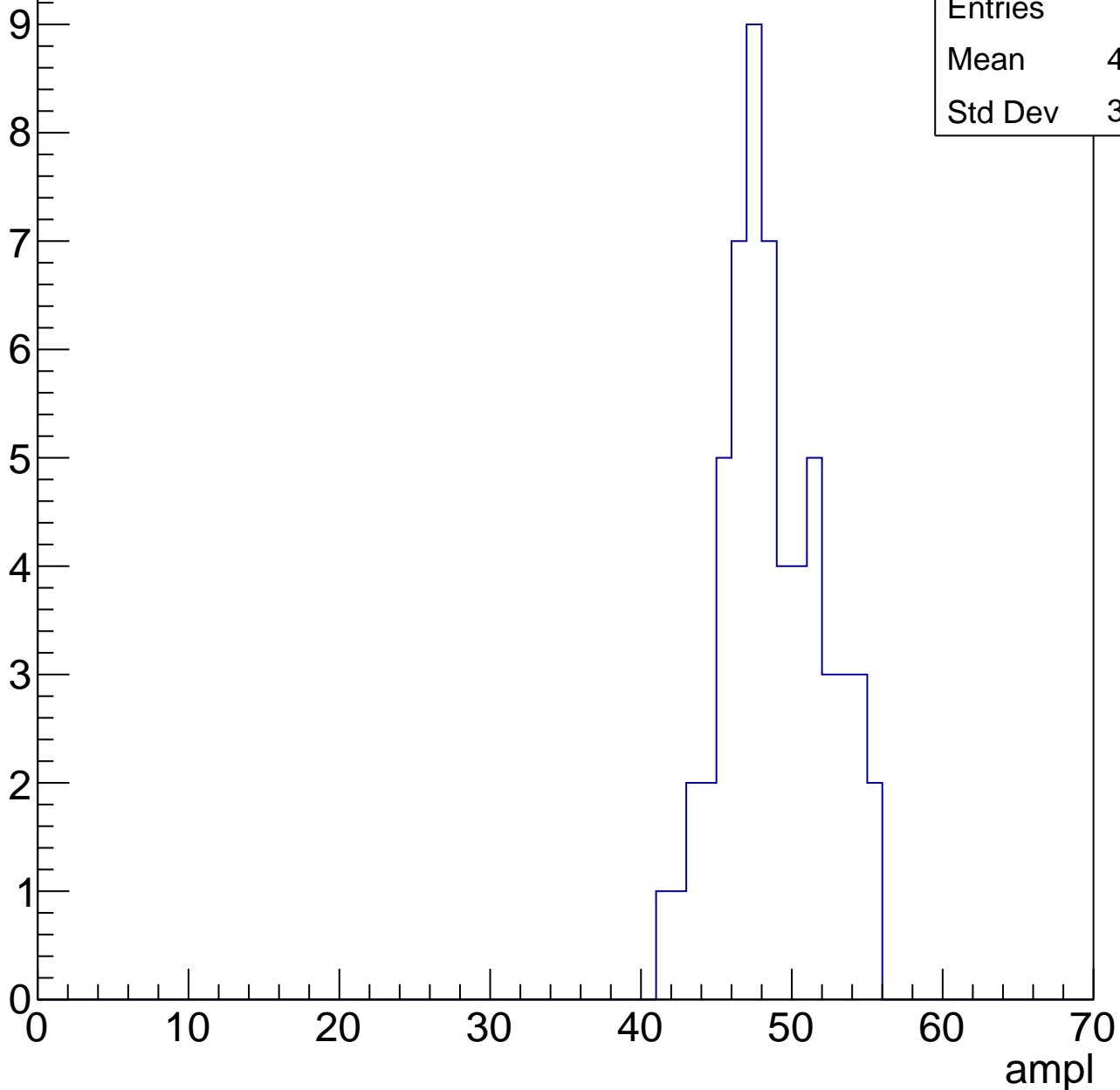


# B1L103S, U25-ch122, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	58
Mean	48.29
Std Dev	3.317

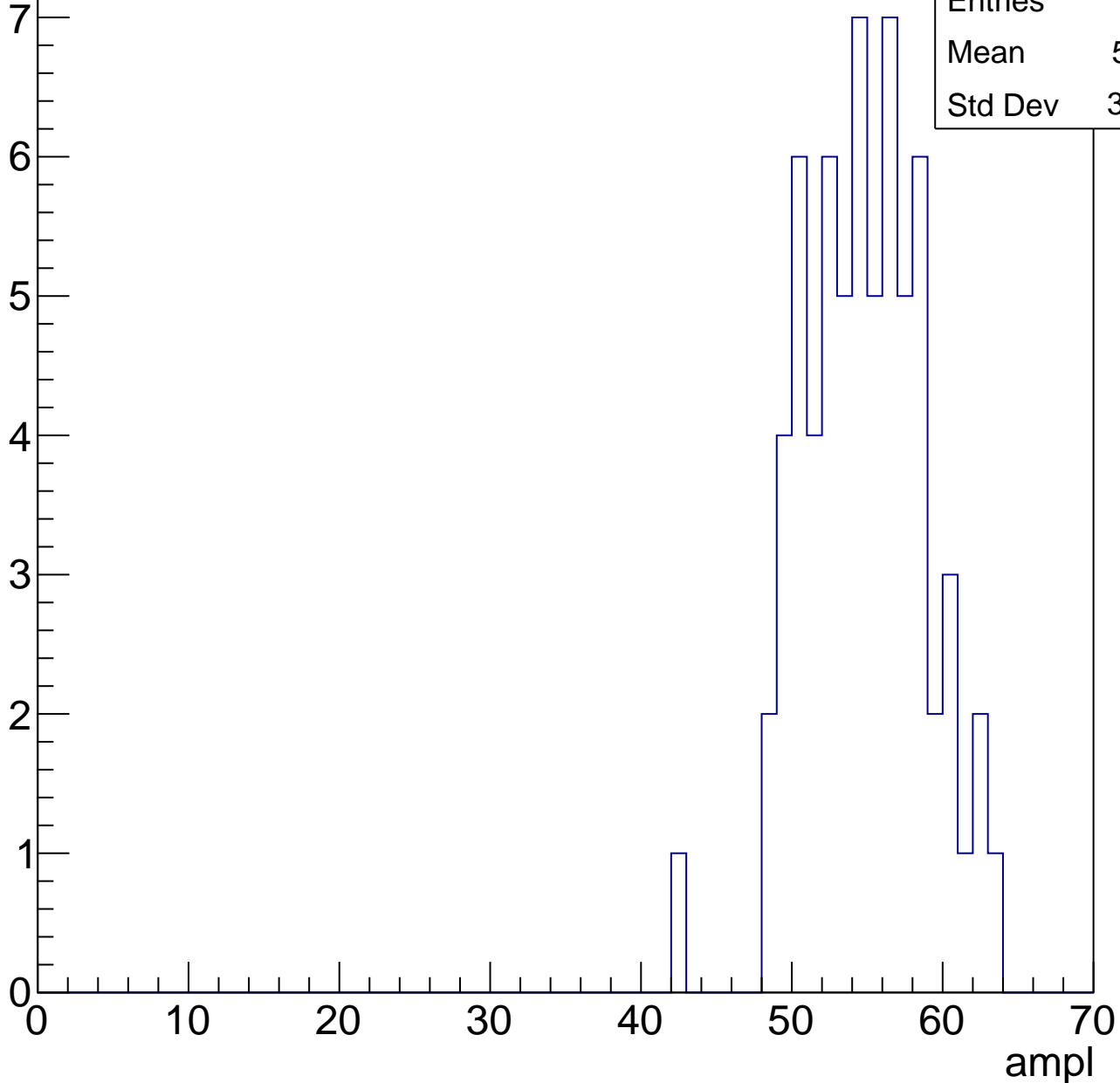


# B1L103S, U25-ch122, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	67
Mean	54.31
Std Dev	3.978

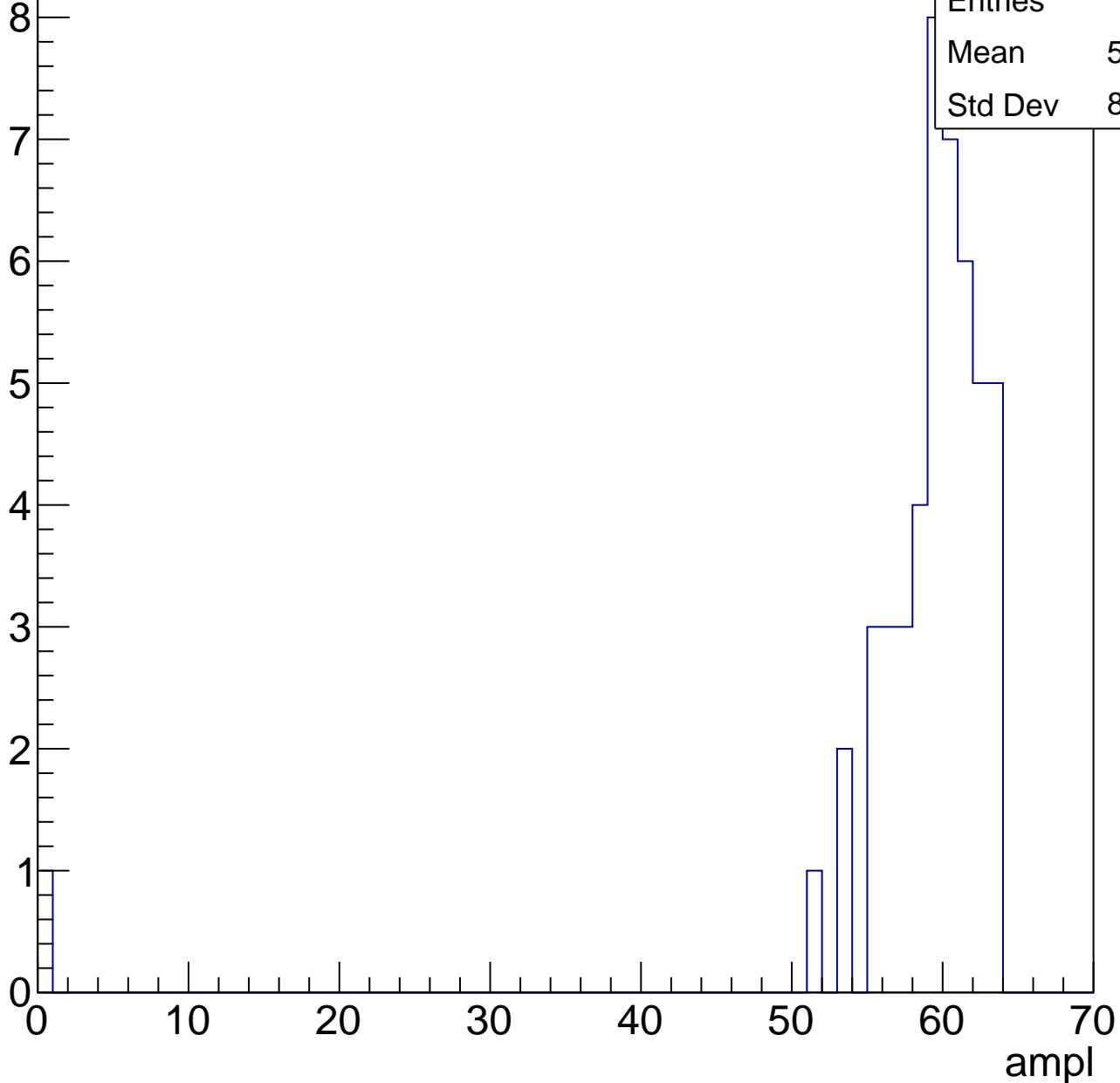


# B1L103S, U25-ch122, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	48
Mean	57.83
Std Dev	8.896



# B1L103S, U25-ch122, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries

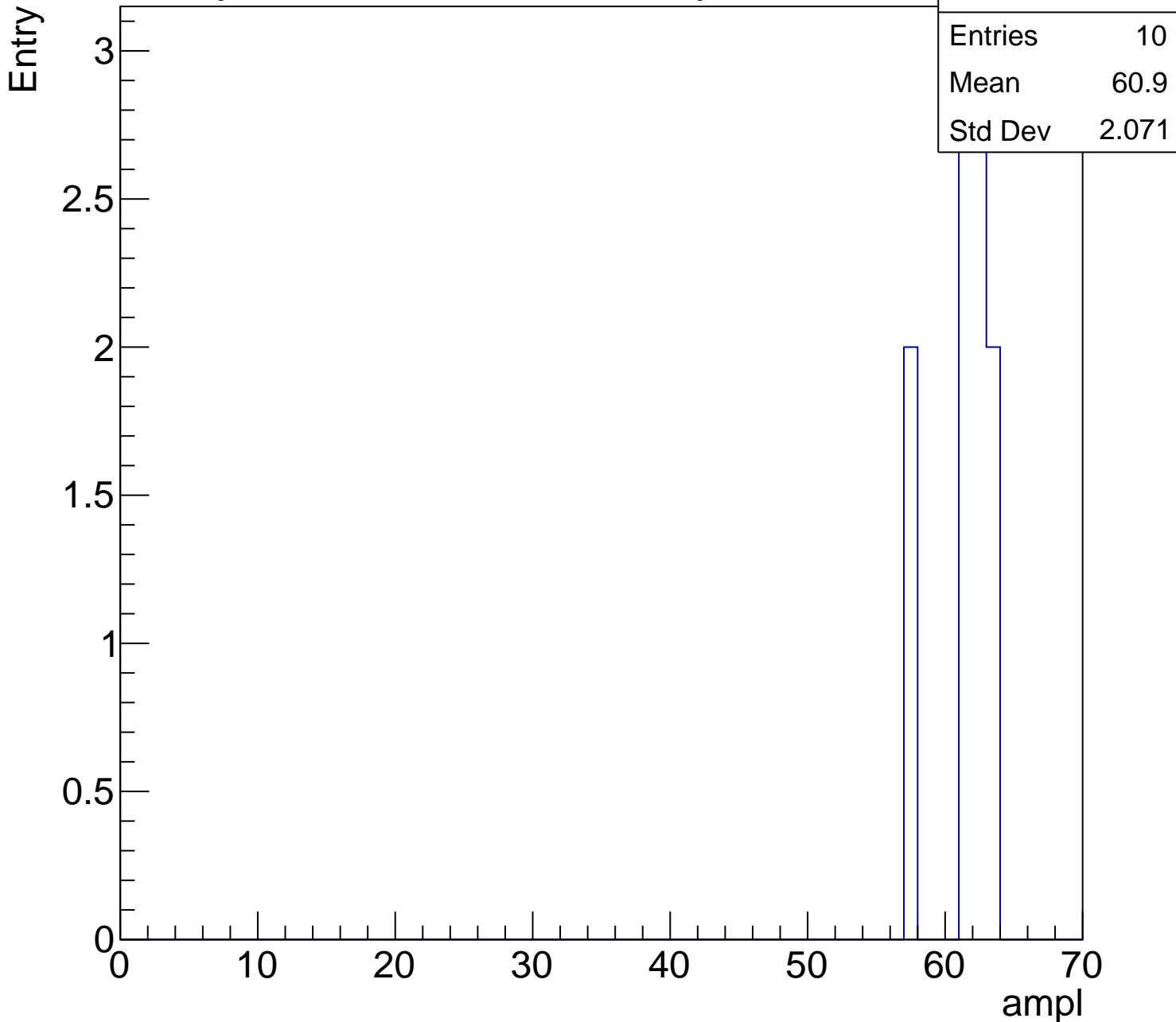
10

Mean

60.9

Std Dev

2.071



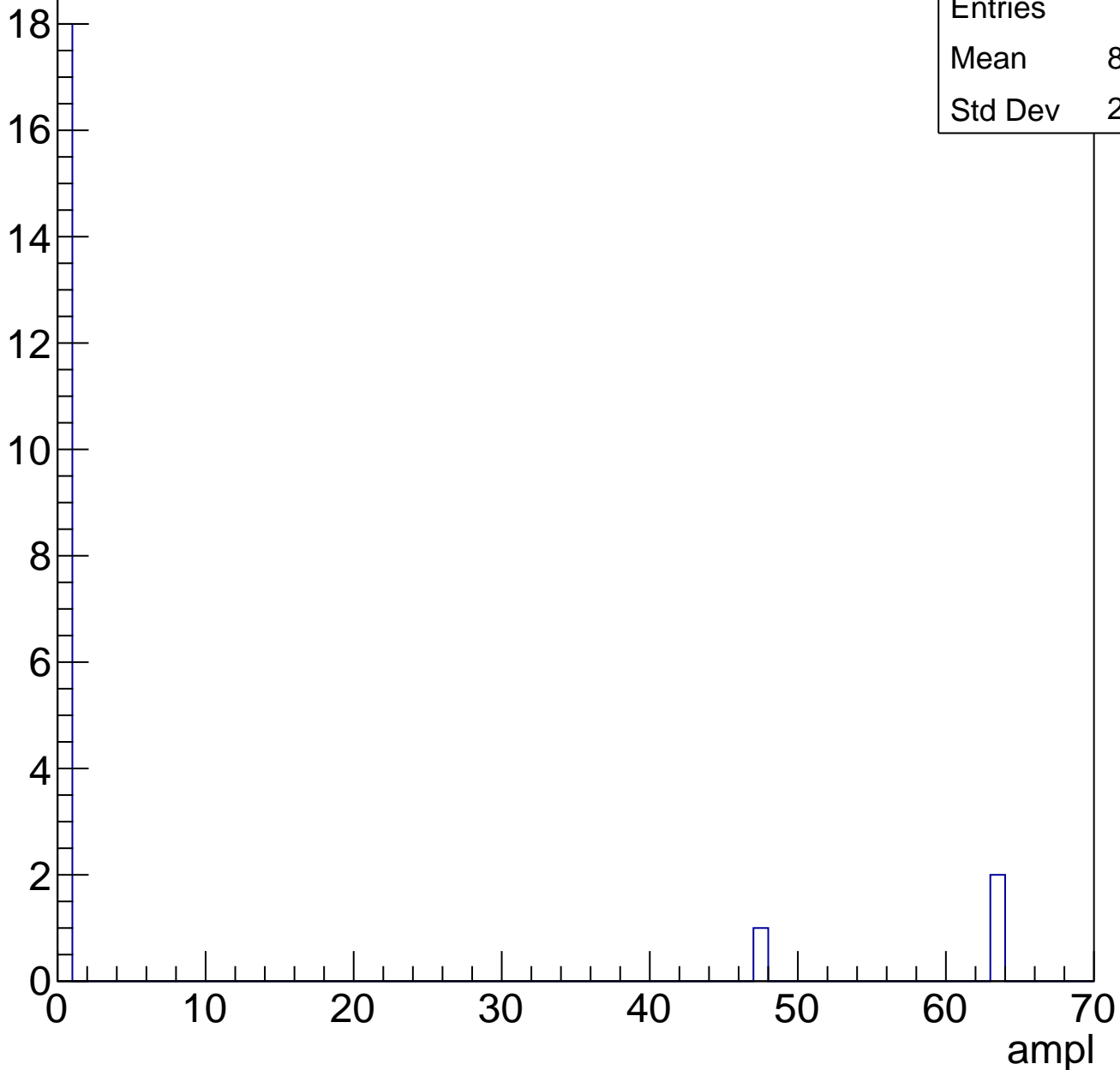


# B1L103S, U25-ch122, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	21
Mean	8.238
Std Dev	20.38

Entry

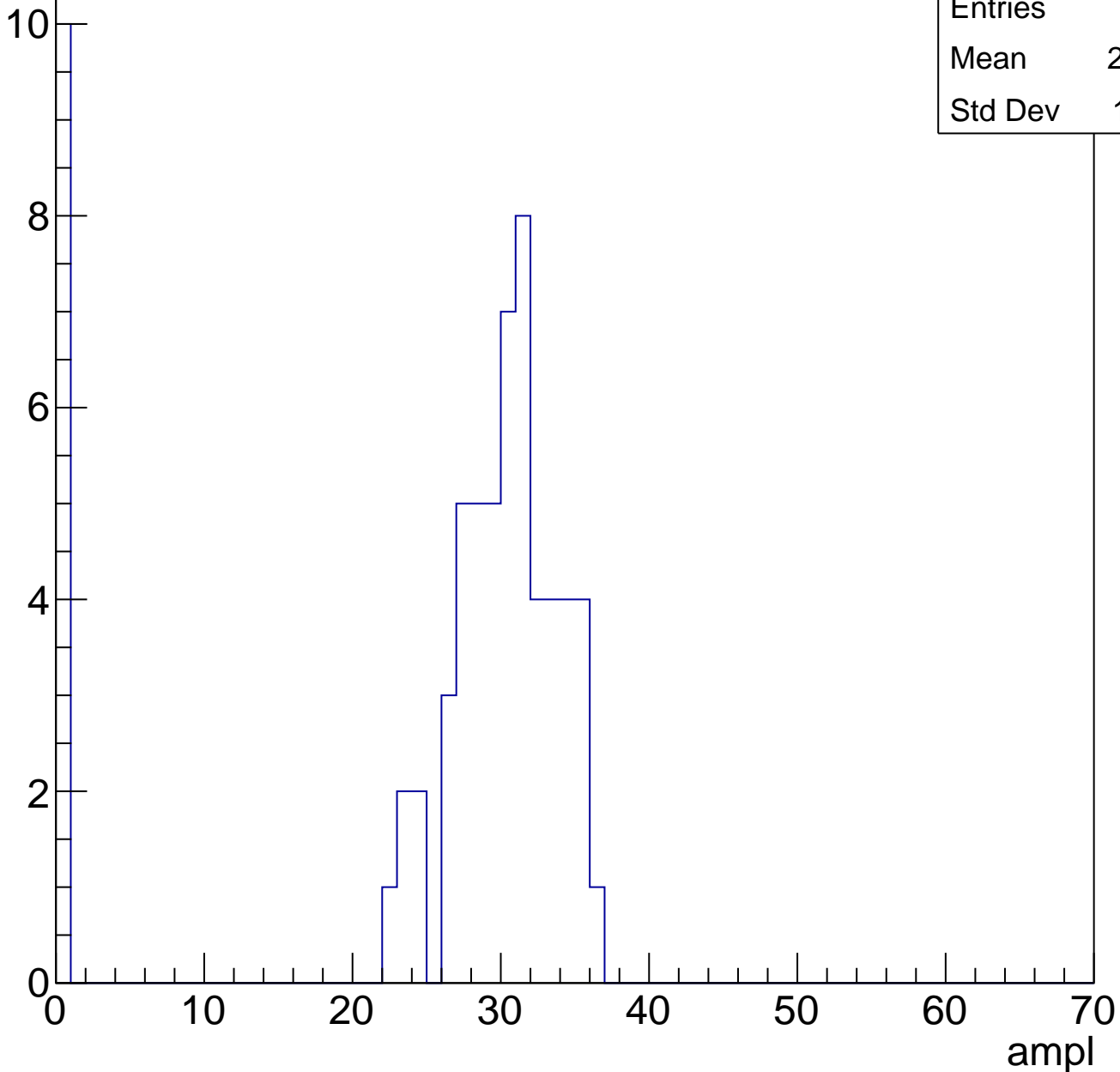


# B1L103S, U25-ch123, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	65
Mean	25.29
Std Dev	11.21

Entry



# B1L103S, U25-ch123, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

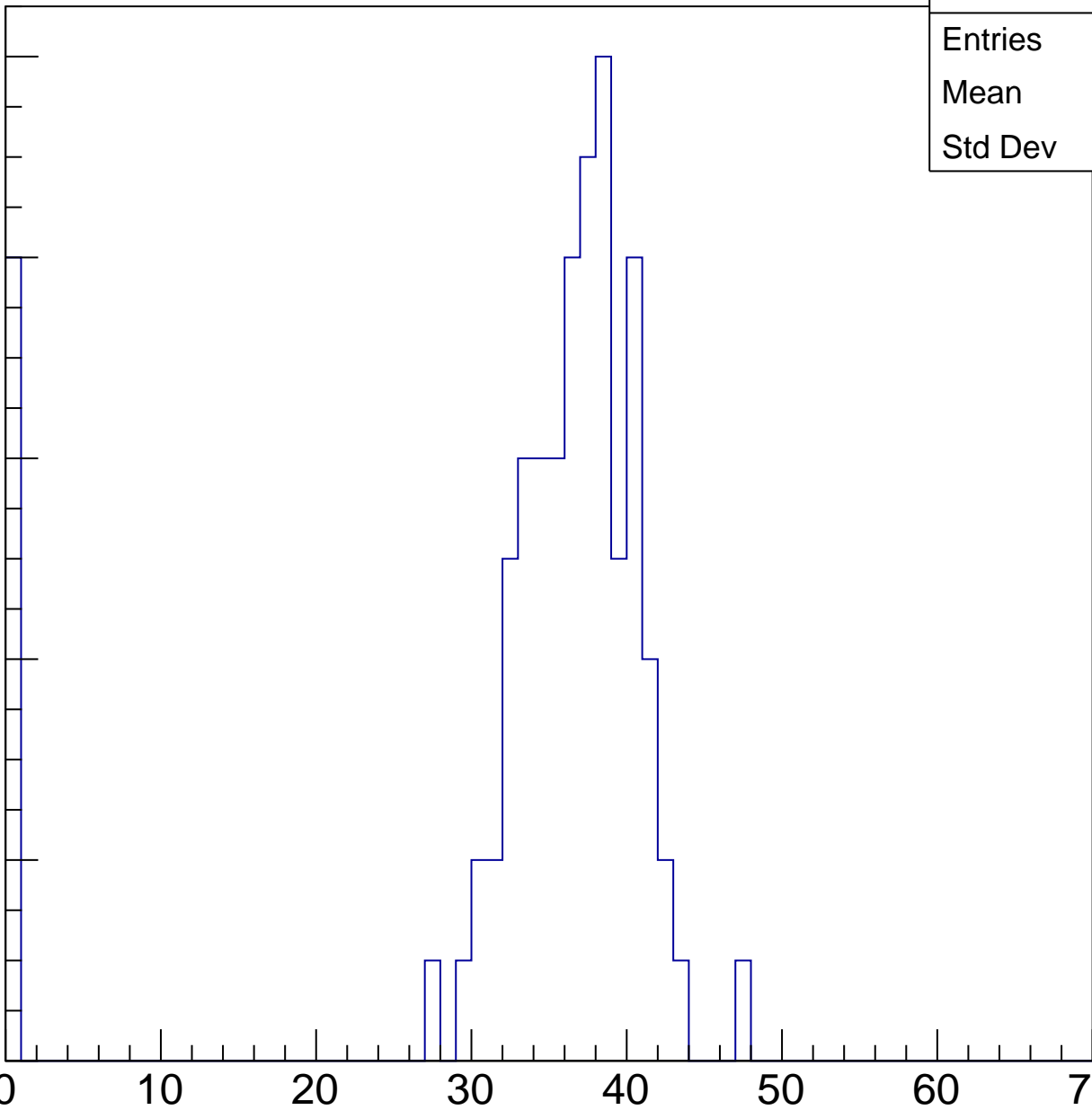
Entries	85
Mean	32.99
Std Dev	11.16

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

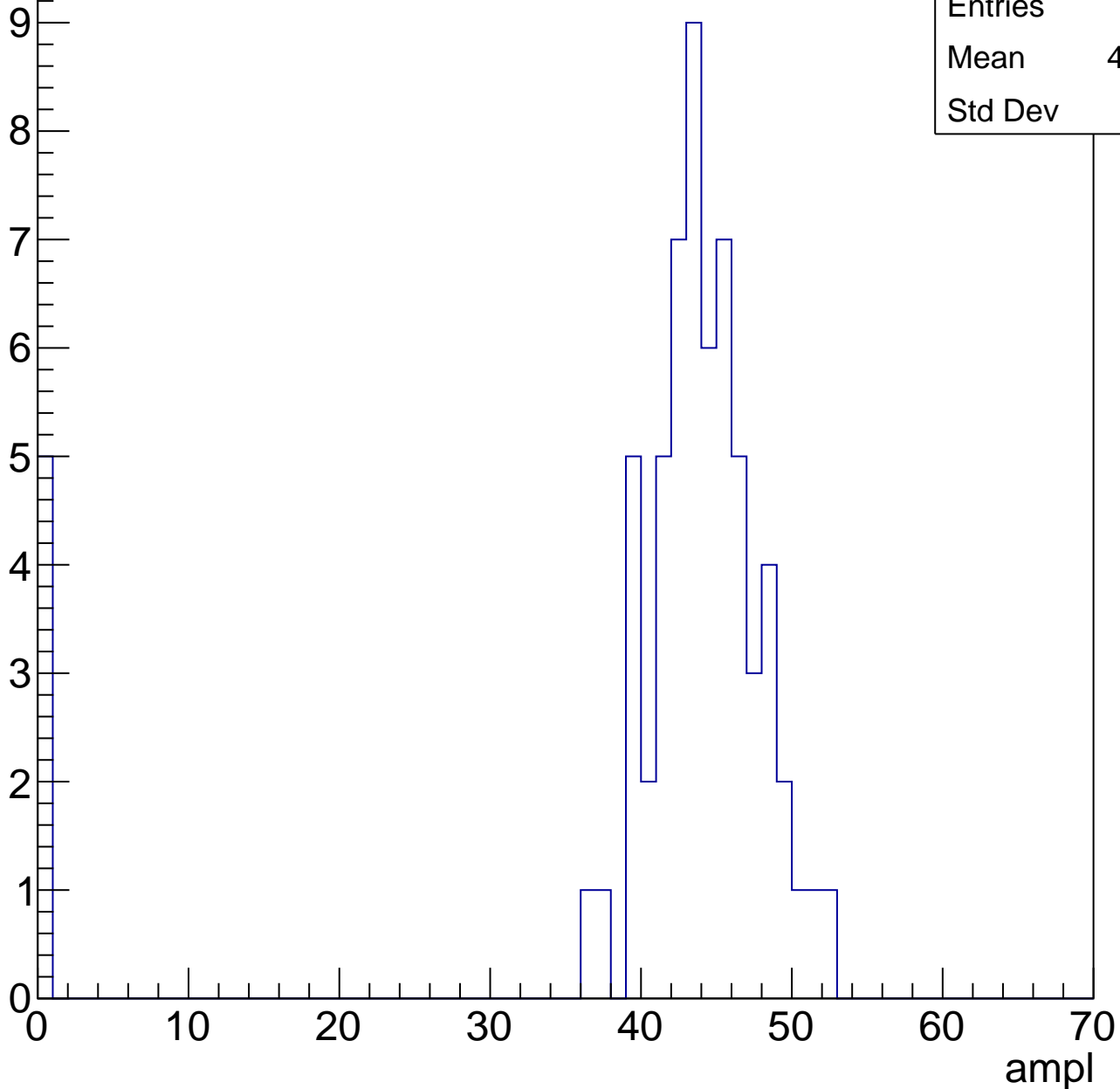


# B1L103S, U25-ch123, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	65
Mean	40.42
Std Dev	12.1

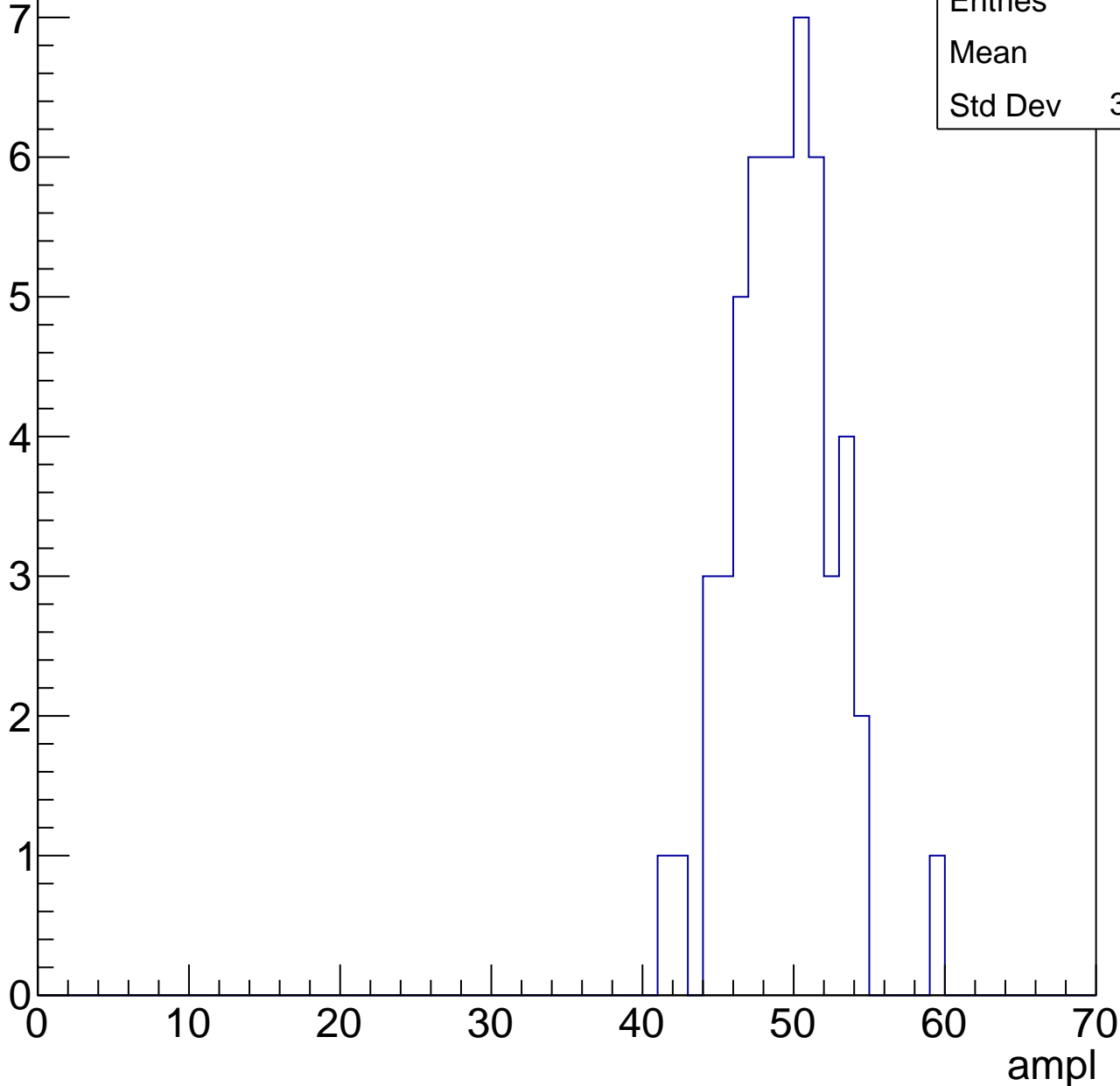


# B1L103S, U25-ch123, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	54
Mean	48.8
Std Dev	3.279

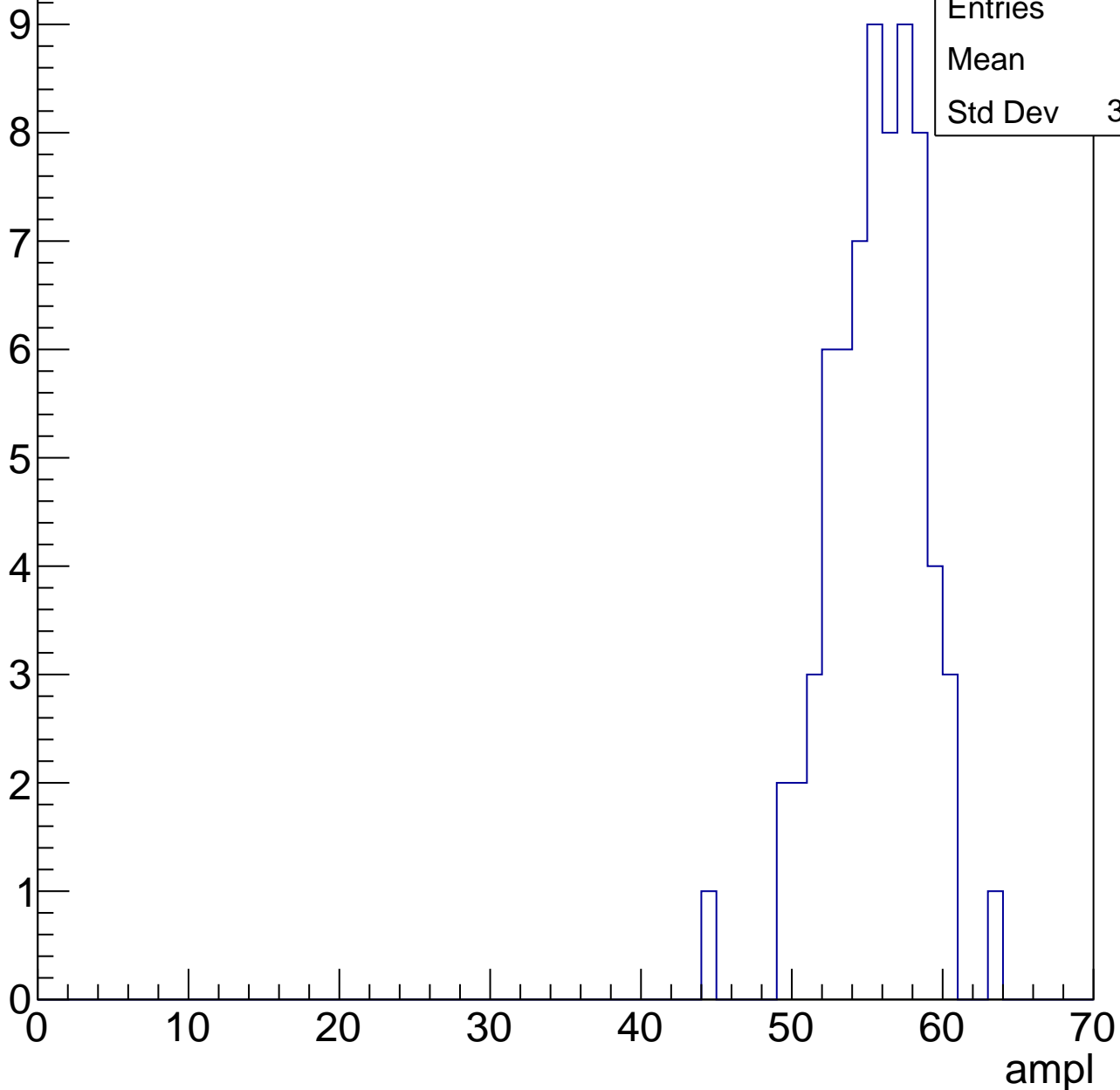


# B1L103S, U25-ch123, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	69
Mean	55.1
Std Dev	3.172



# B1L103S, U25-ch123, adc5

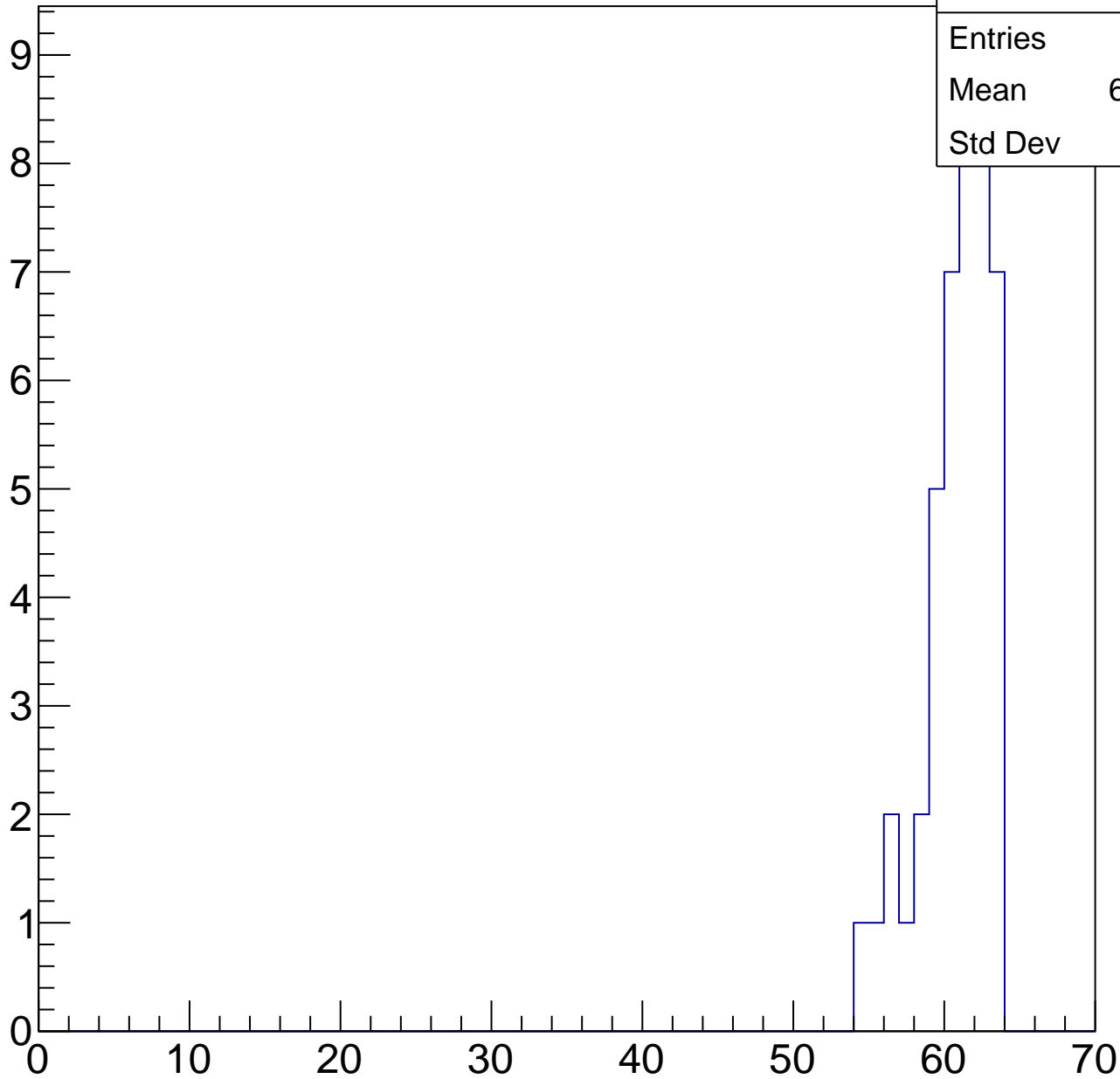
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	43
Mean	60.35
Std Dev	2.23

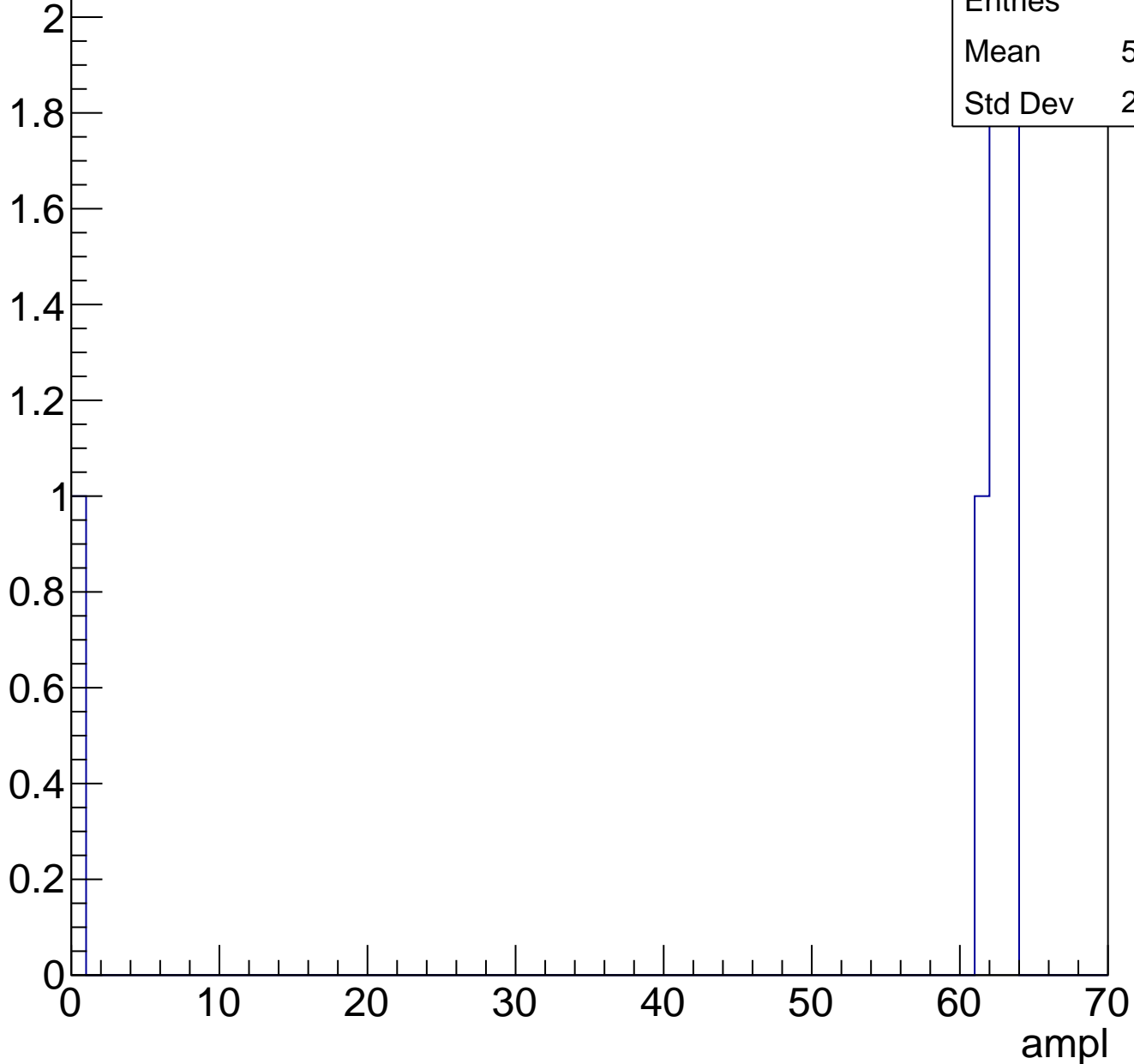
ampl



# B1L103S, U25-ch123, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U25-ch123, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

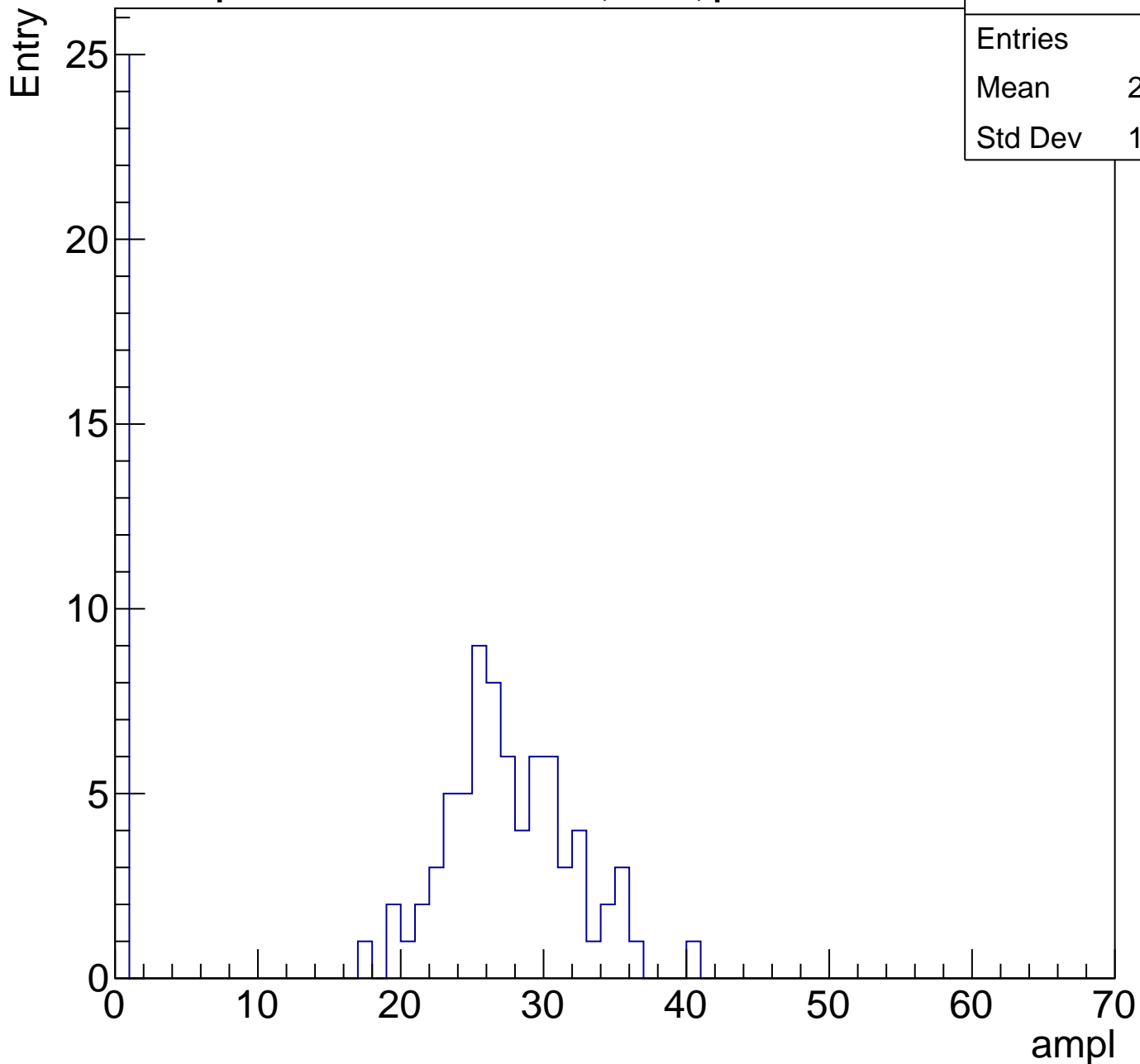
Entries	19
Mean	0
Std Dev	0

ampl

# B1L103S, U25-ch124, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	98
Mean	20.22
Std Dev	12.42

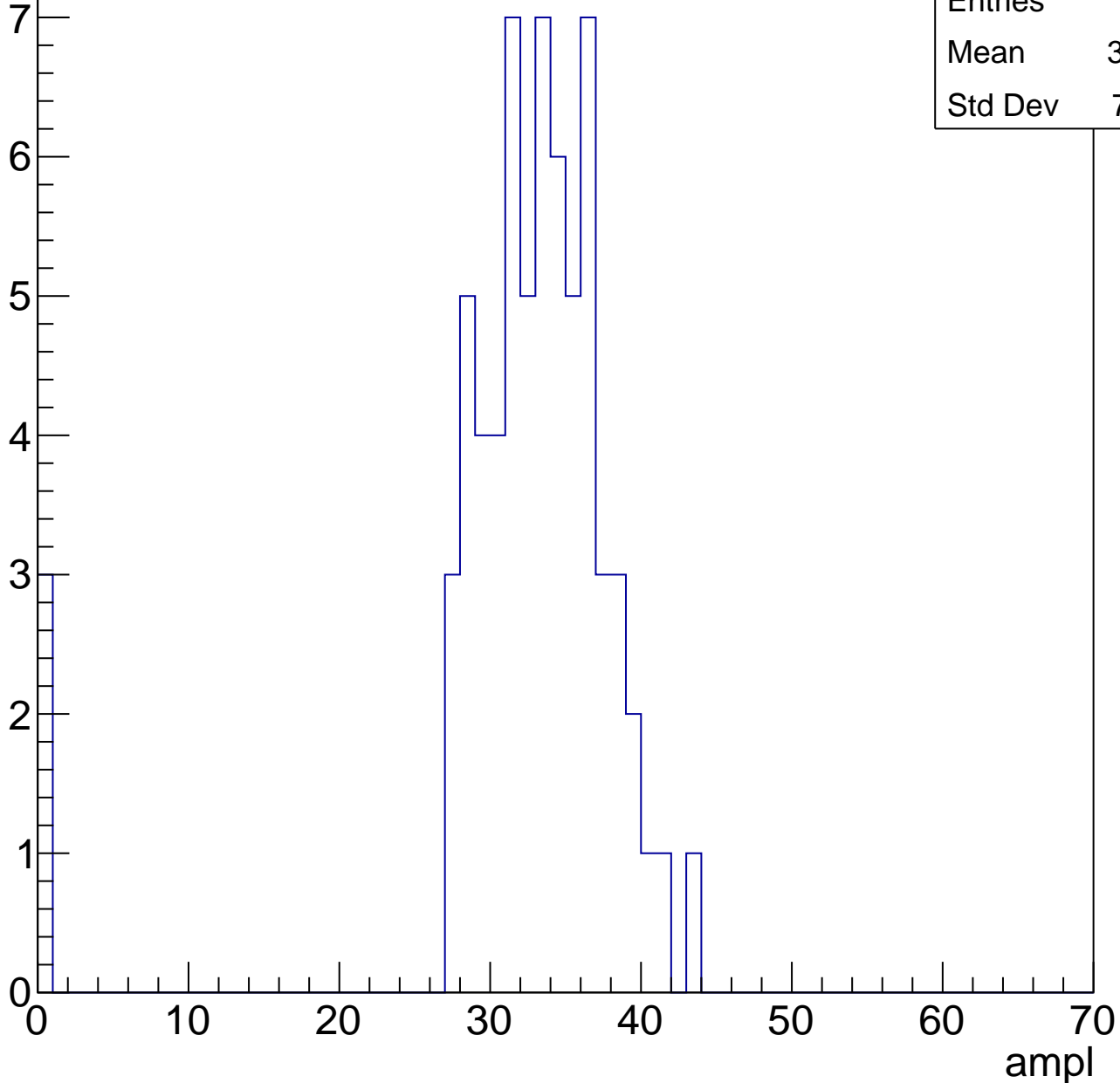


# B1L103S, U25-ch124, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	67
Mean	31.69
Std Dev	7.741

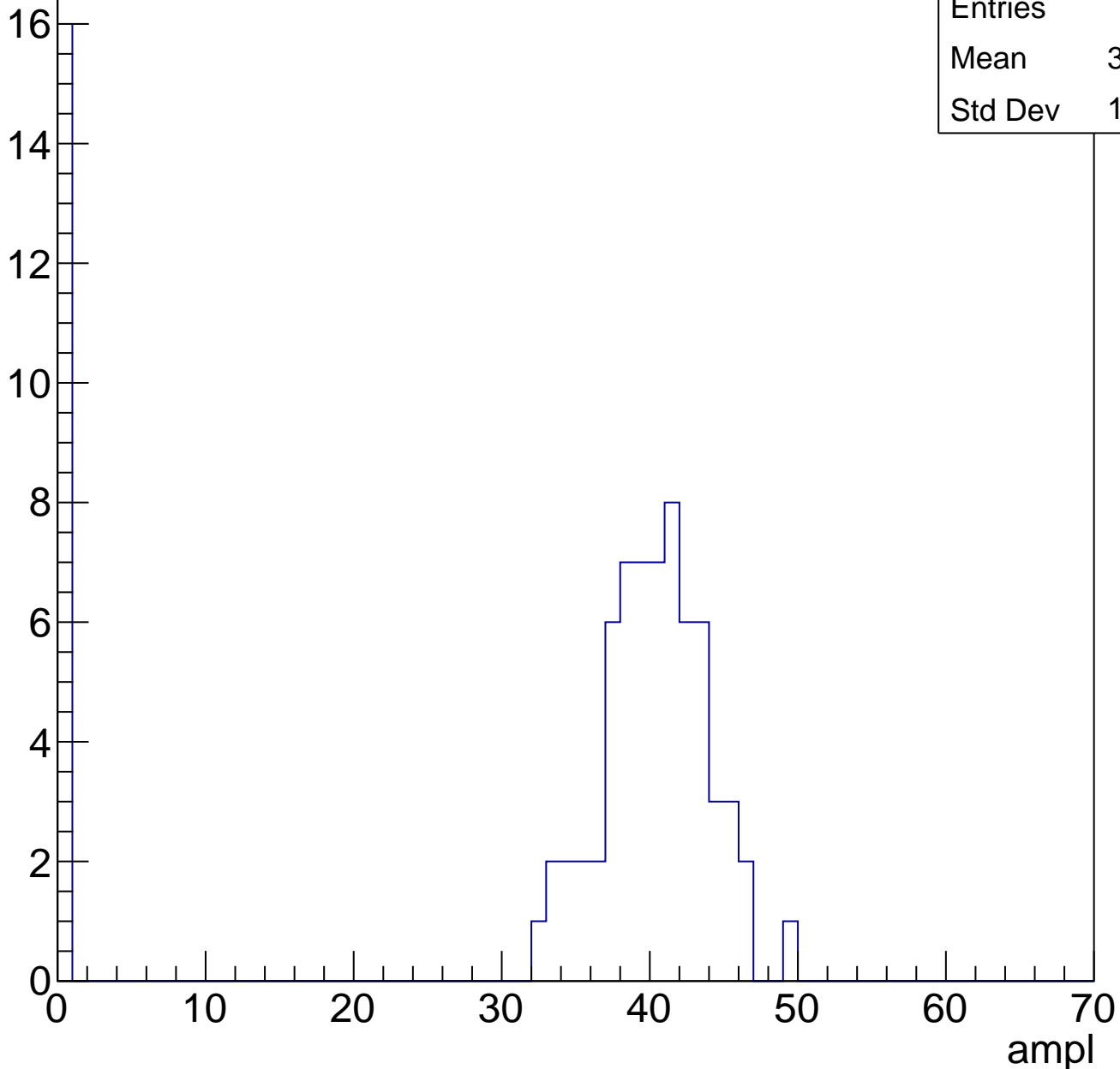


# B1L103S, U25-ch124, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	81
Mean	32.04
Std Dev	16.19

Entry

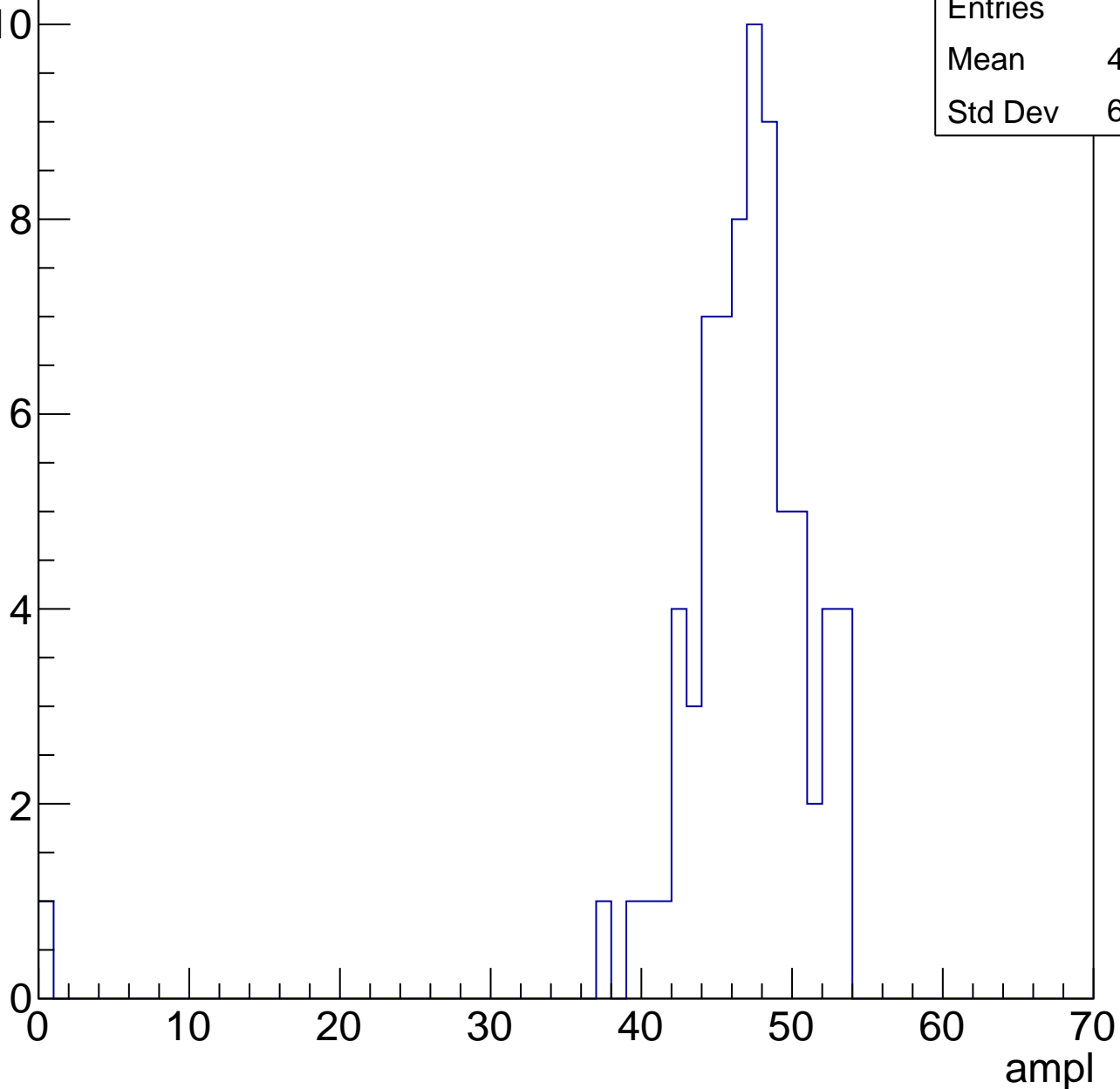


# B1L103S, U25-ch124, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	73
Mean	46.08
Std Dev	6.404

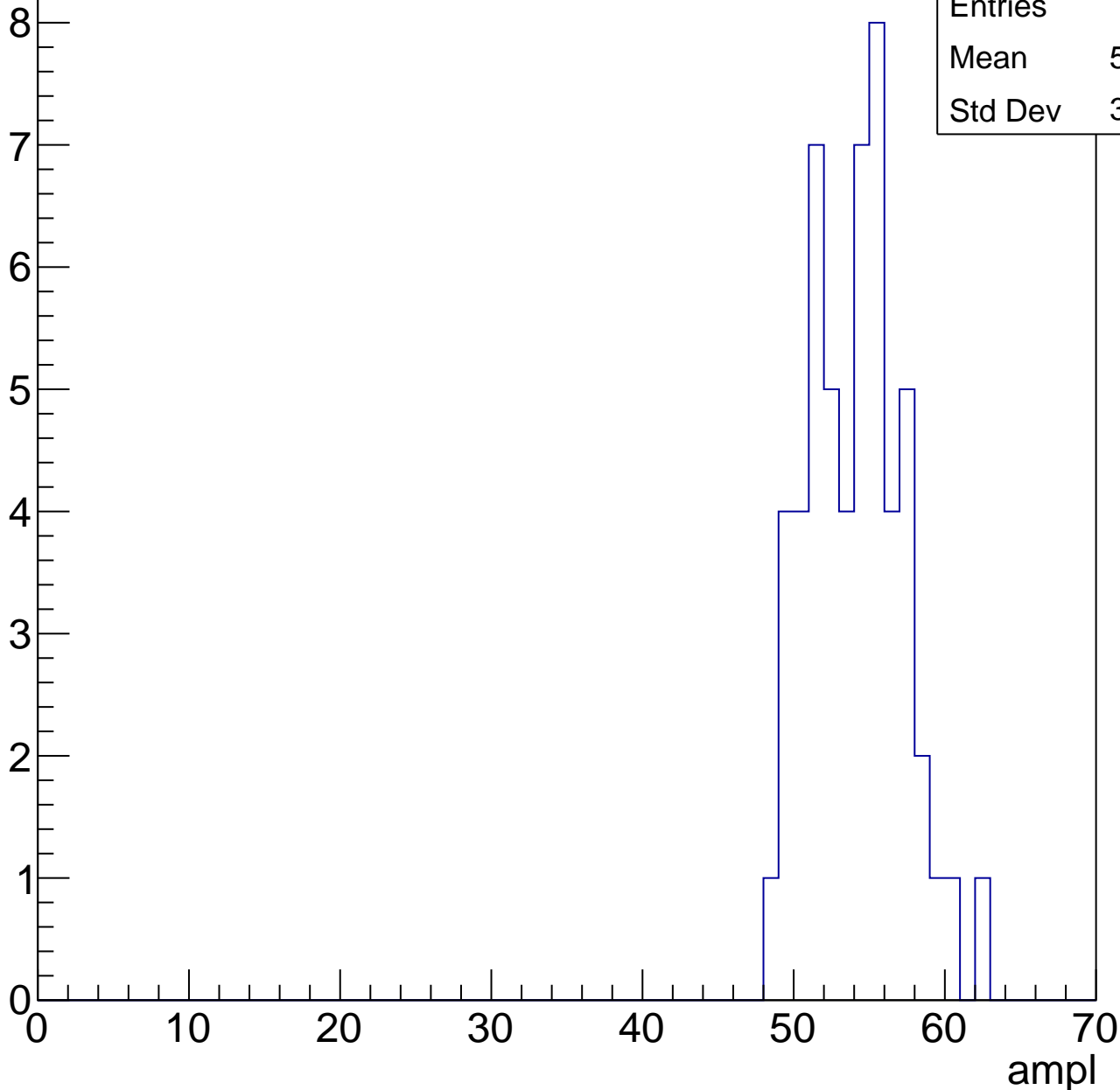


# B1L103S, U25-ch124, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	54
Mean	53.65
Std Dev	3.062

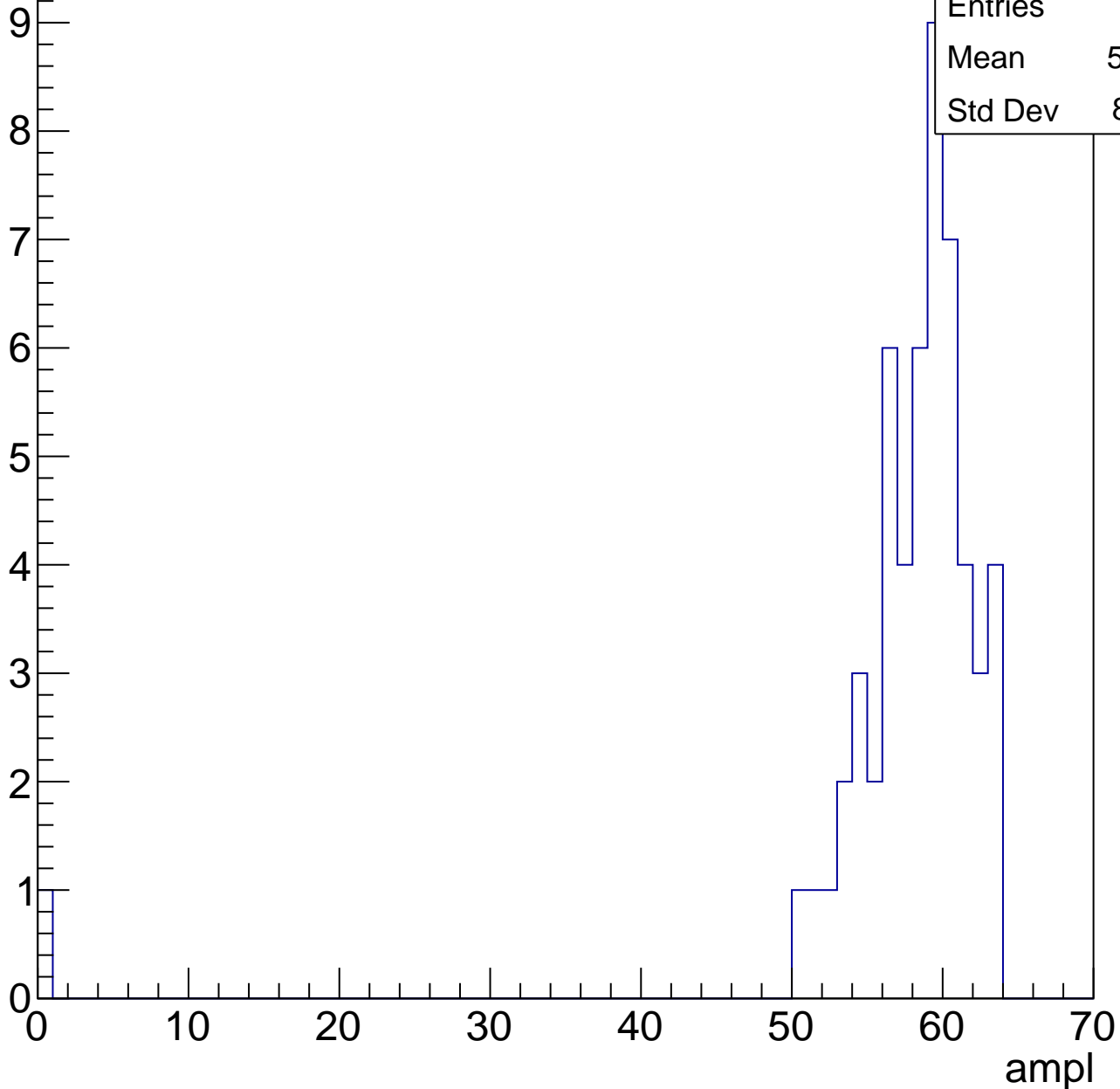


# B1L103S, U25-ch124, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	54
Mean	56.96
Std Dev	8.411

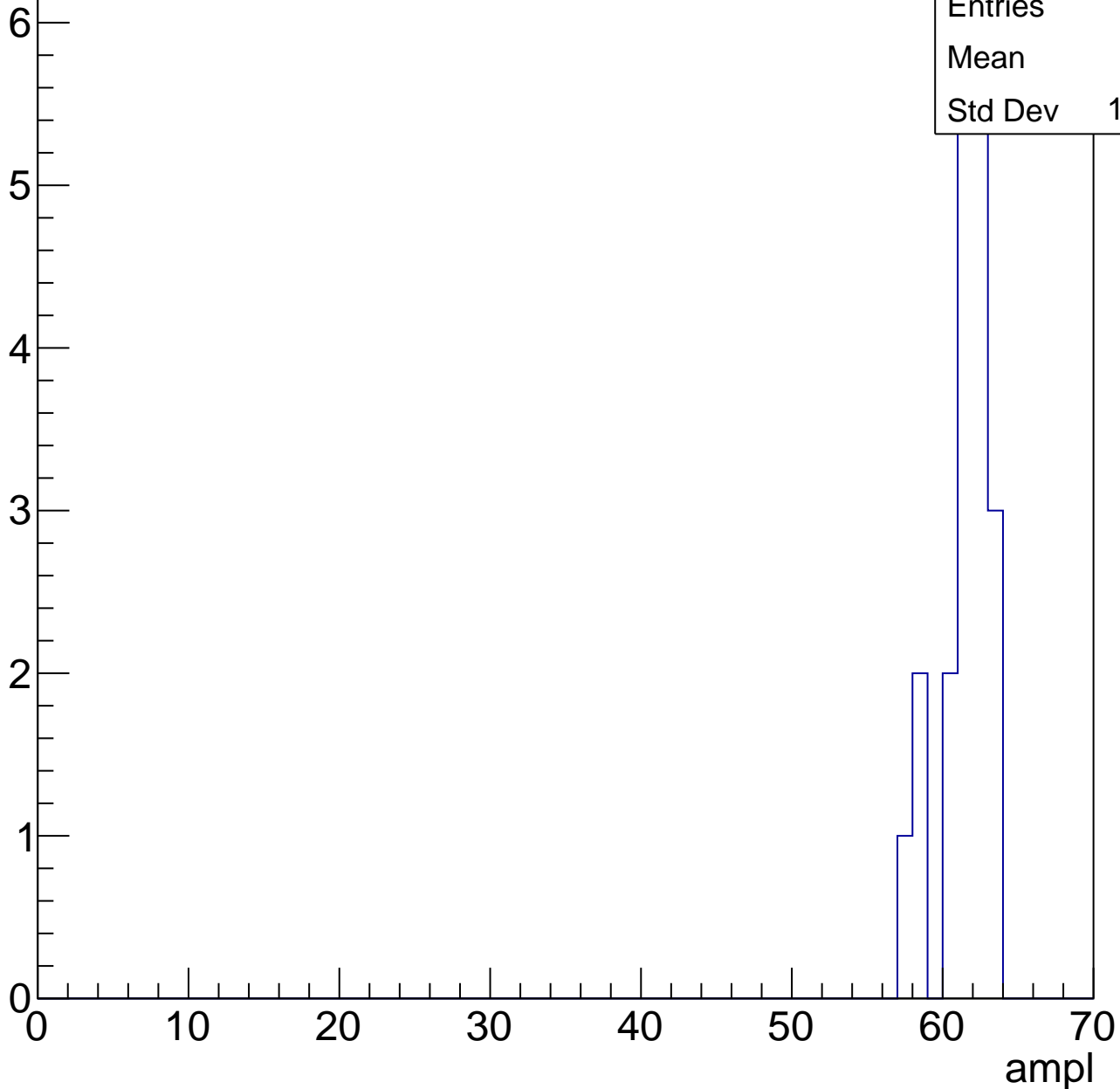


# B1L103S, U25-ch124, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	20
Mean	61
Std Dev	1.643



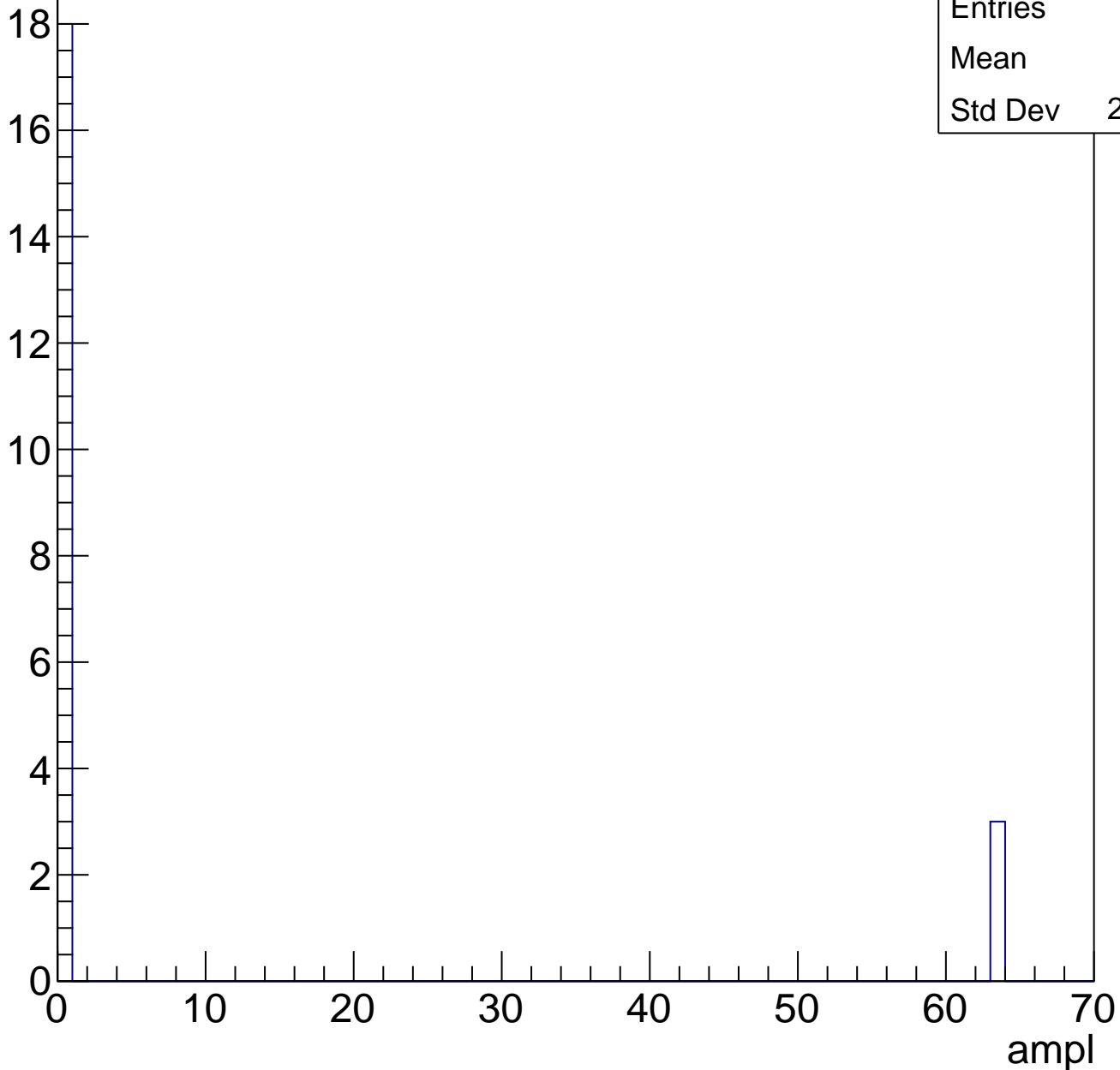


# B1L103S, U25-ch124, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	21
Mean	9
Std Dev	22.05

Entry



# B1L103S, U25-ch125, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	64
Mean	23.88
Std Dev	11.25

Entry

10

8

6

4

2

0

0

10

20

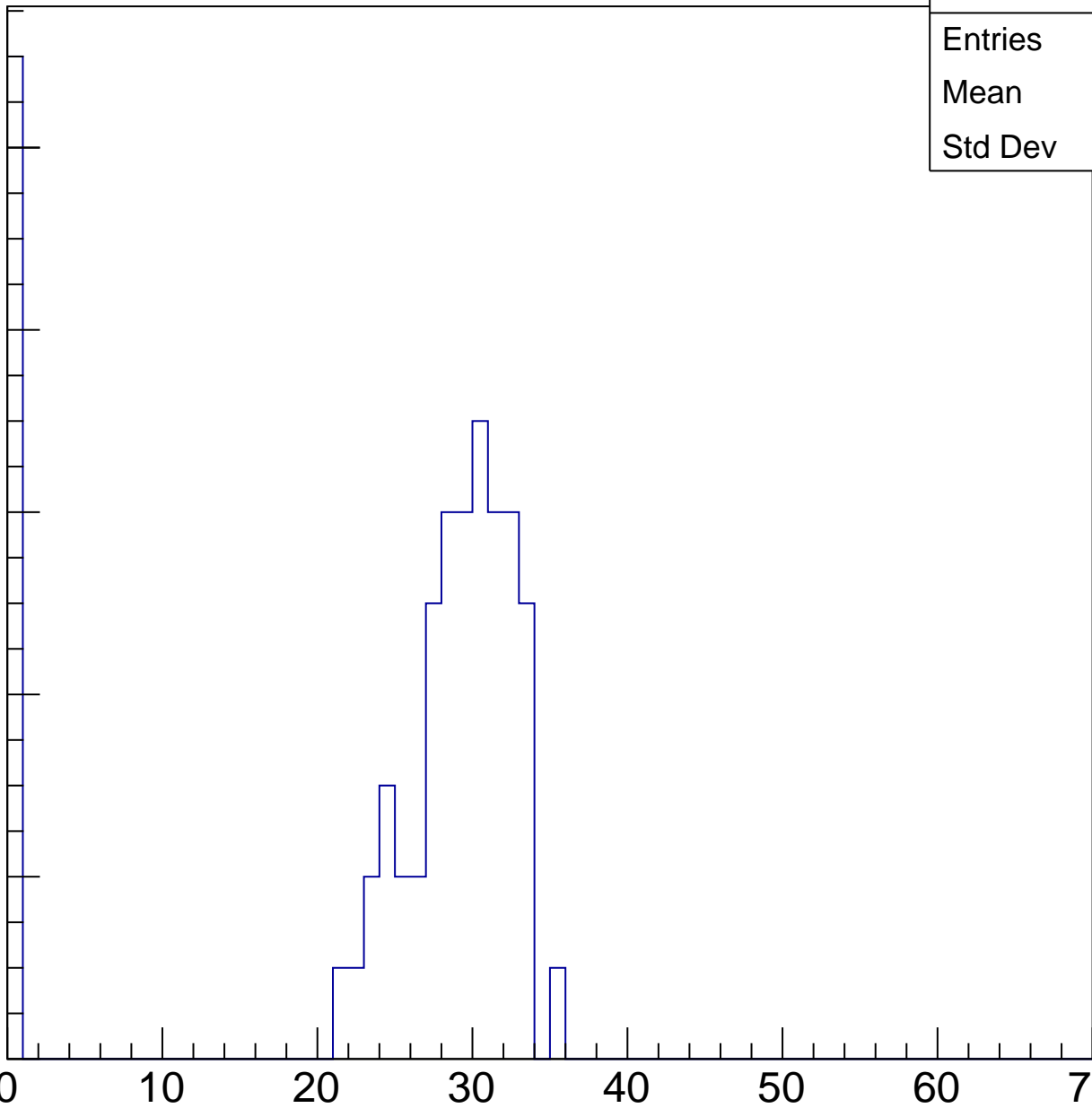
30

40

50

60

ampl



# B1L103S, U25-ch125, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

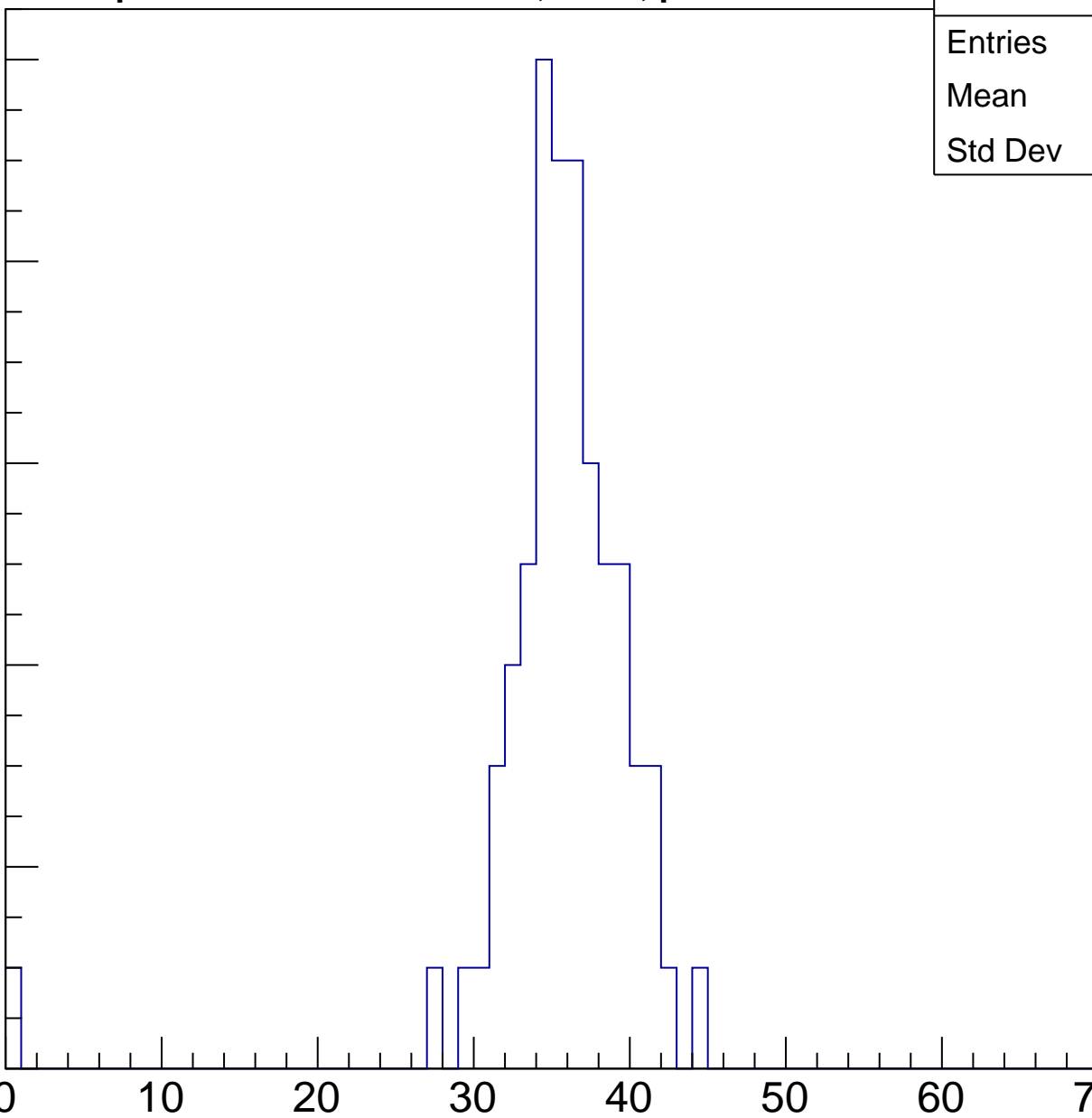
Entries	68
Mean	35.1
Std Dev	5.333

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

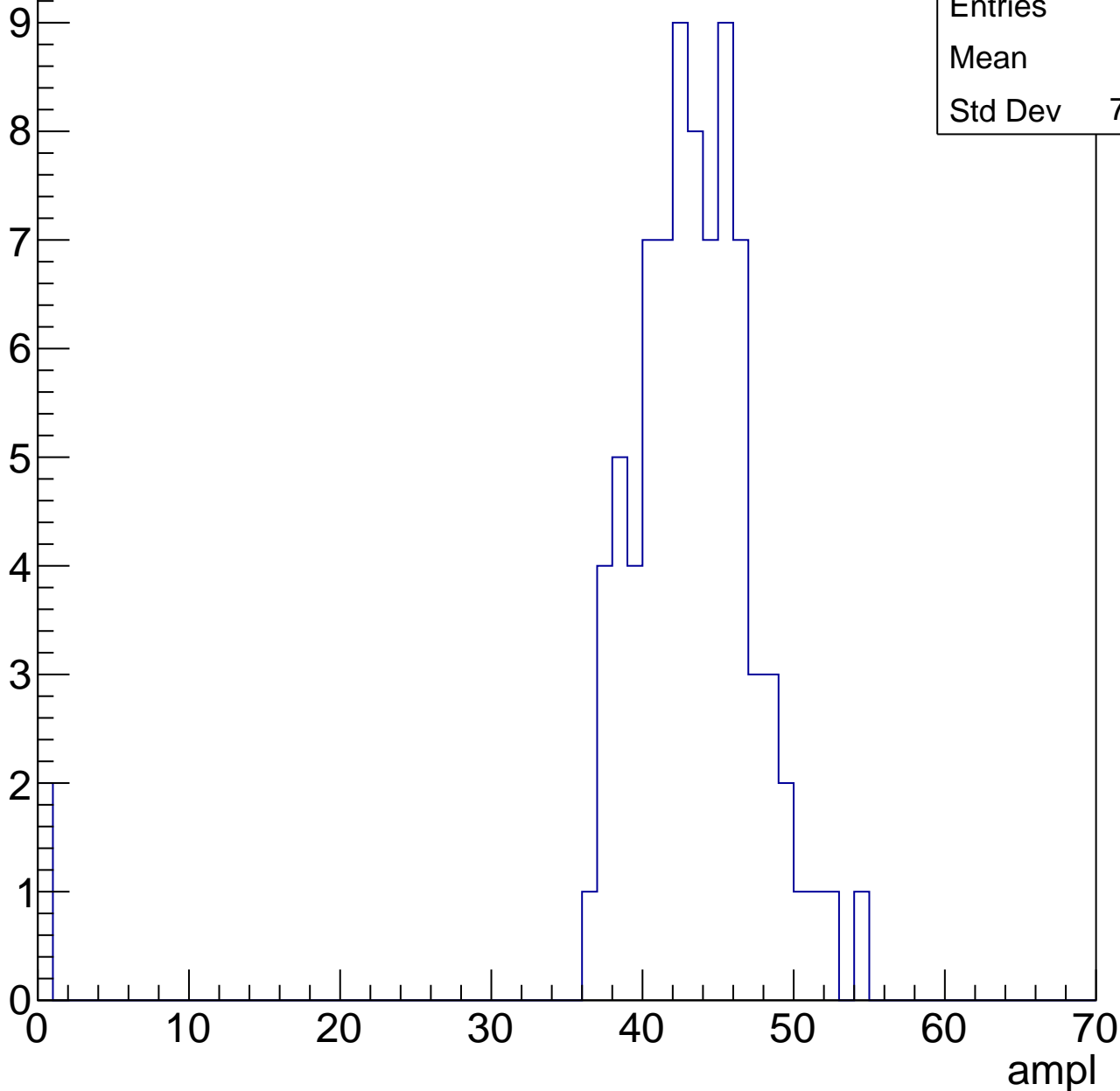


# B1L103S, U25-ch125, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	82
Mean	42
Std Dev	7.582

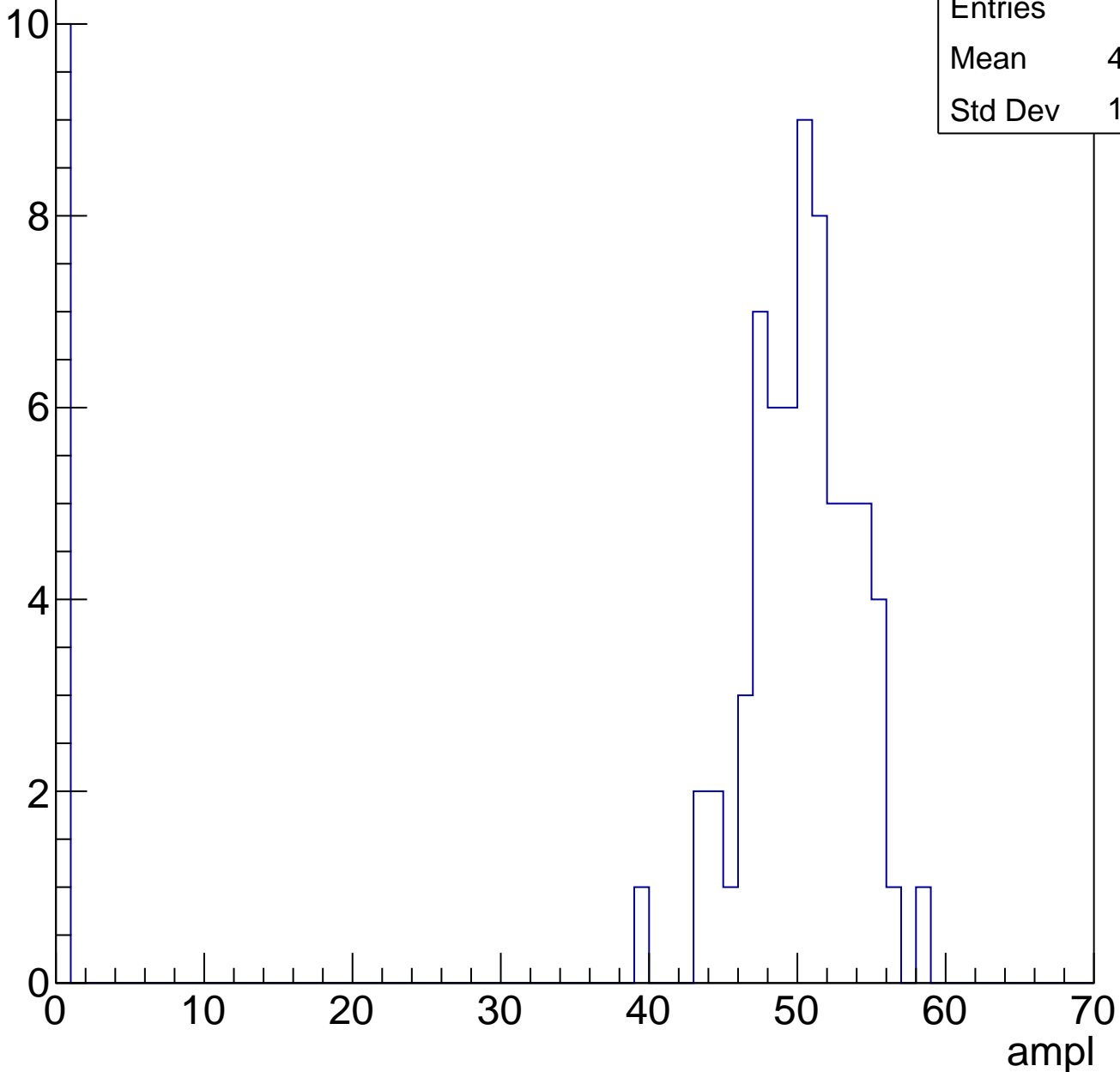


# B1L103S, U25-ch125, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	76
Mean	43.34
Std Dev	17.18

Entry

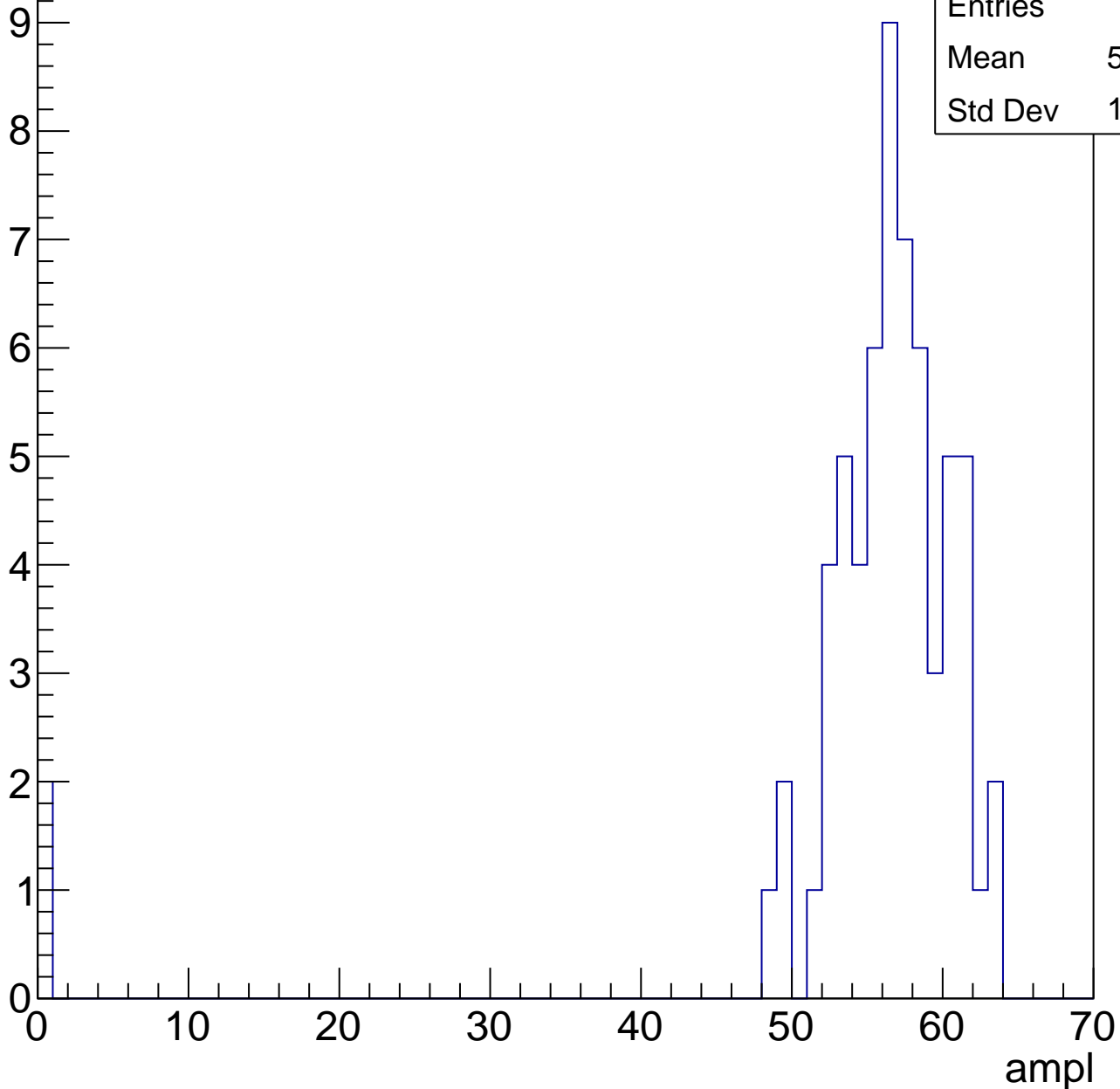


# B1L103S, U25-ch125, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	63
Mean	54.56
Std Dev	10.43

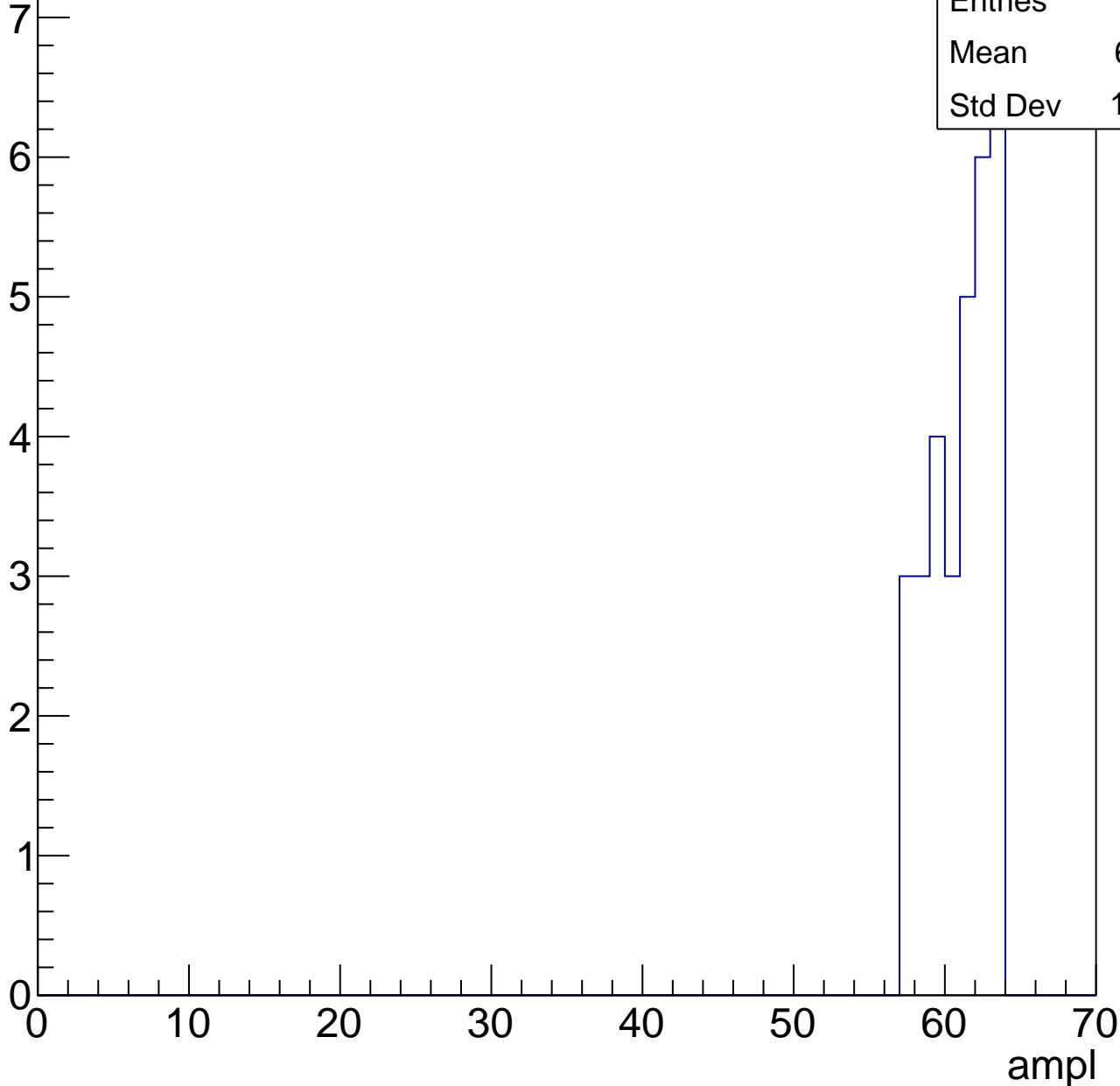


# B1L103S, U25-ch125, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	31
Mean	60.61
Std Dev	1.995



# B1L103S, U25-ch125, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

ampl

Entries

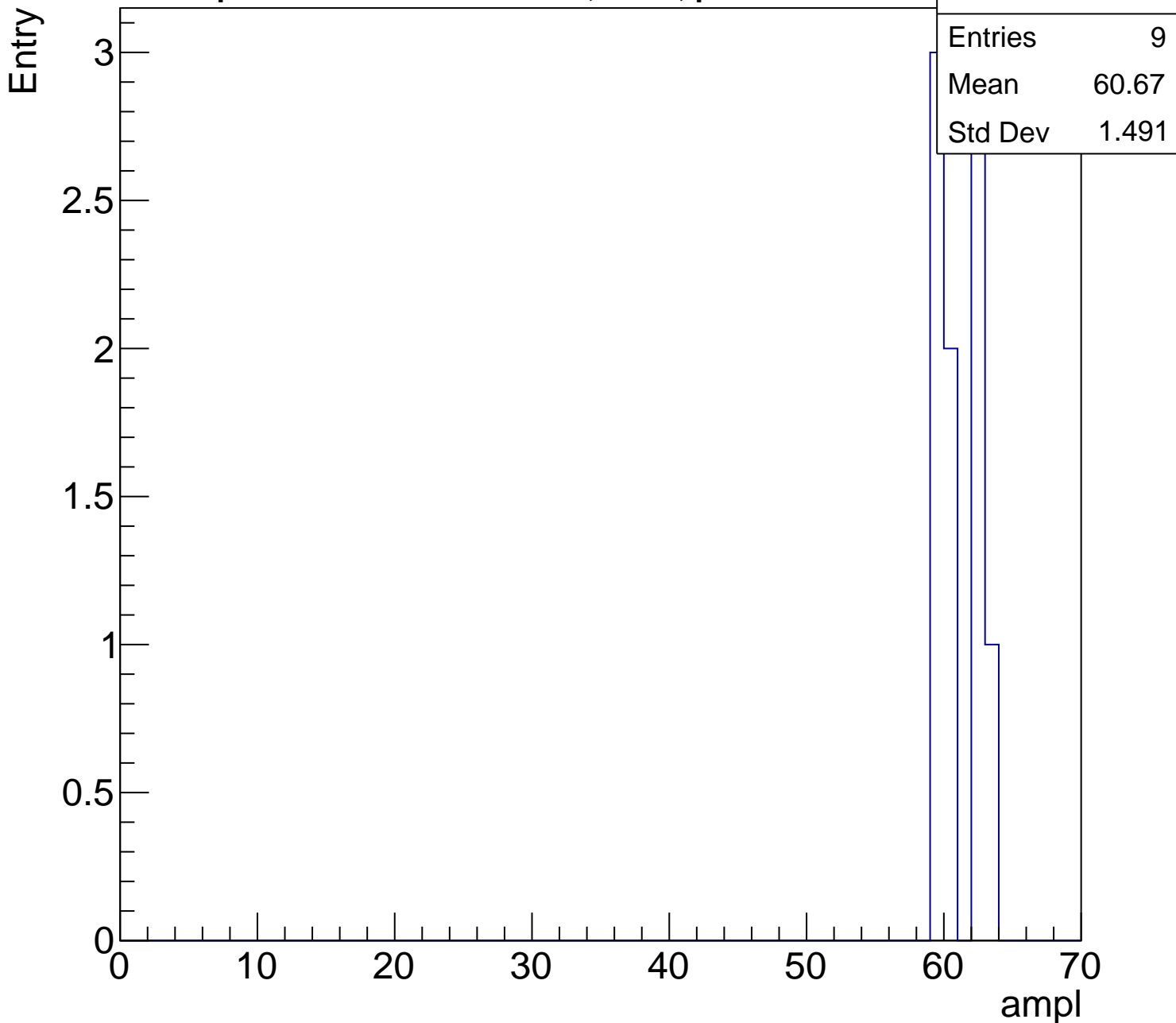
9

Mean

60.67

Std Dev

1.491





# B1L103S, U25-ch125, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

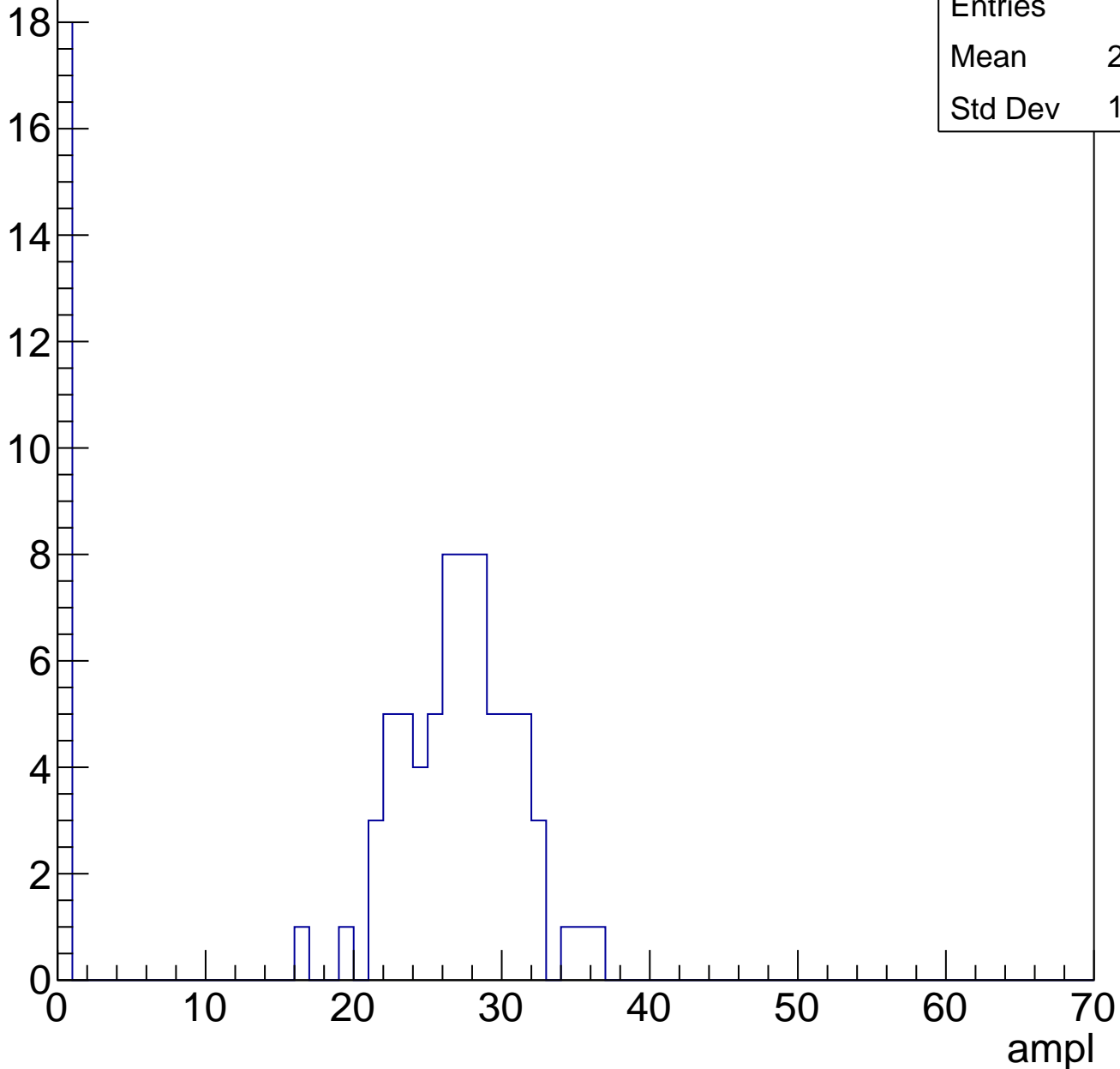
Entries	19
Mean	0
Std Dev	0

# B1L103S, U25-ch126, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	87
Mean	21.18
Std Dev	11.33

Entry

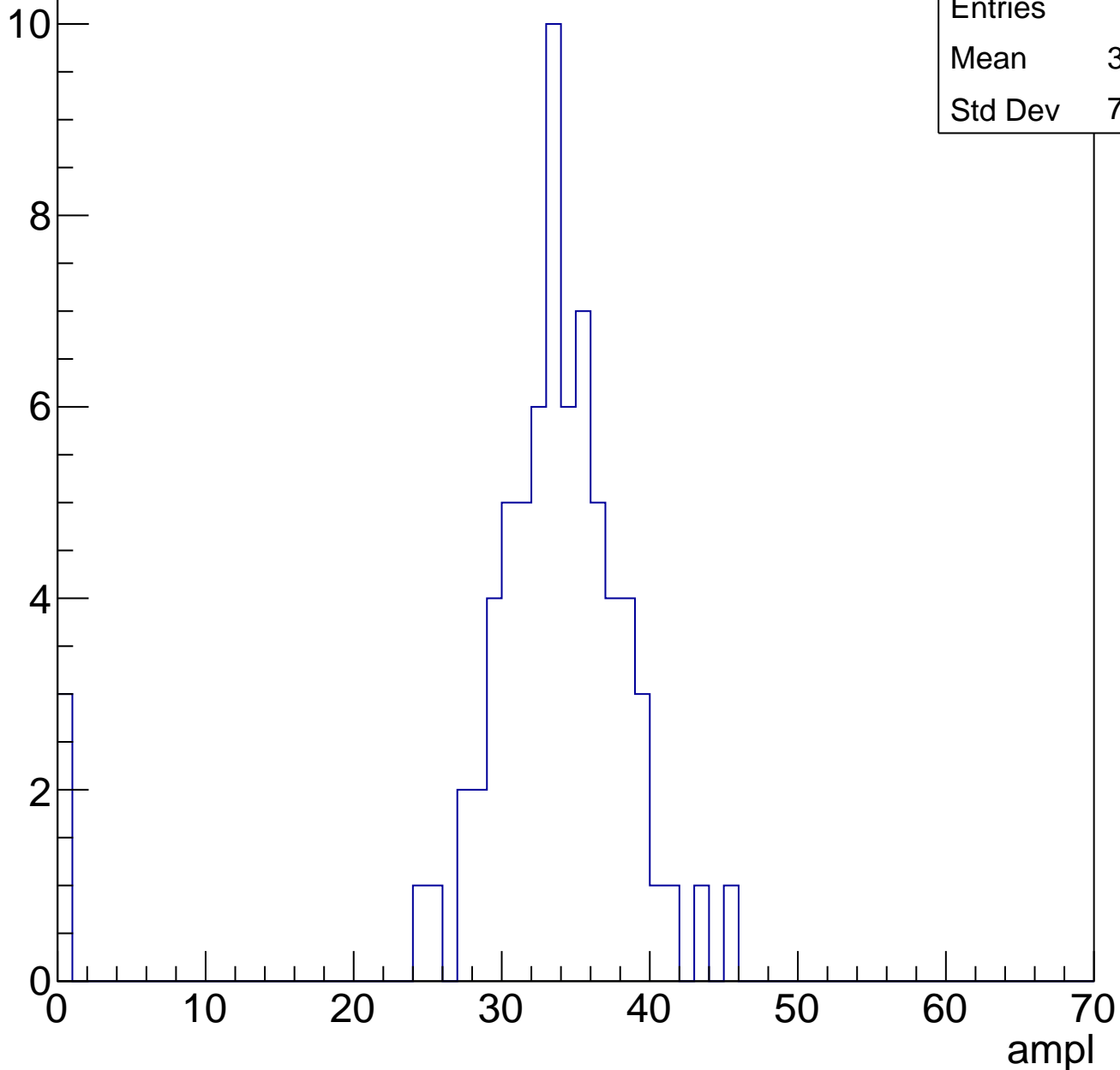


# B1L103S, U25-ch126, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	72
Mean	32.18
Std Dev	7.754

Entry

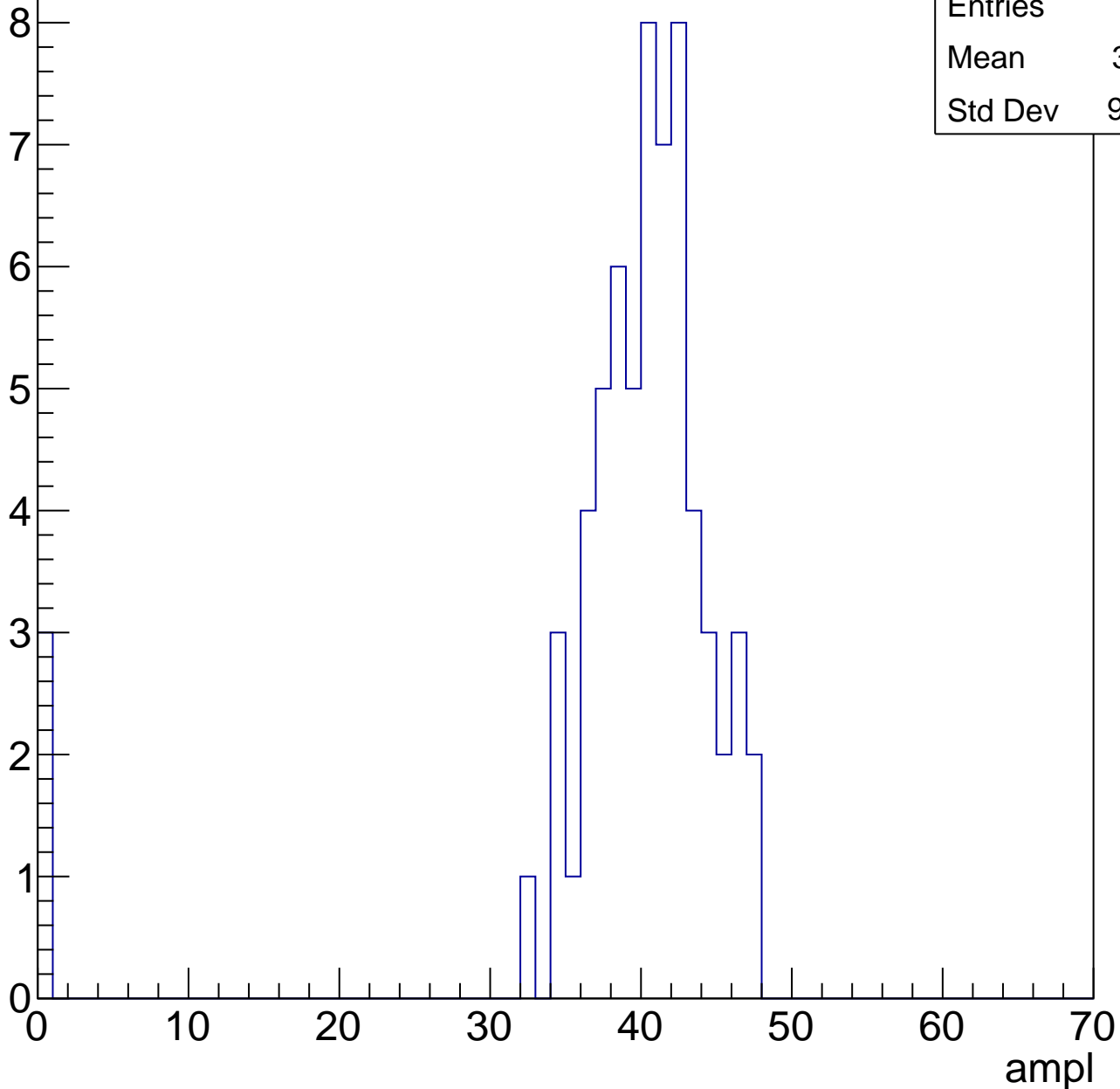


# B1L103S, U25-ch126, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

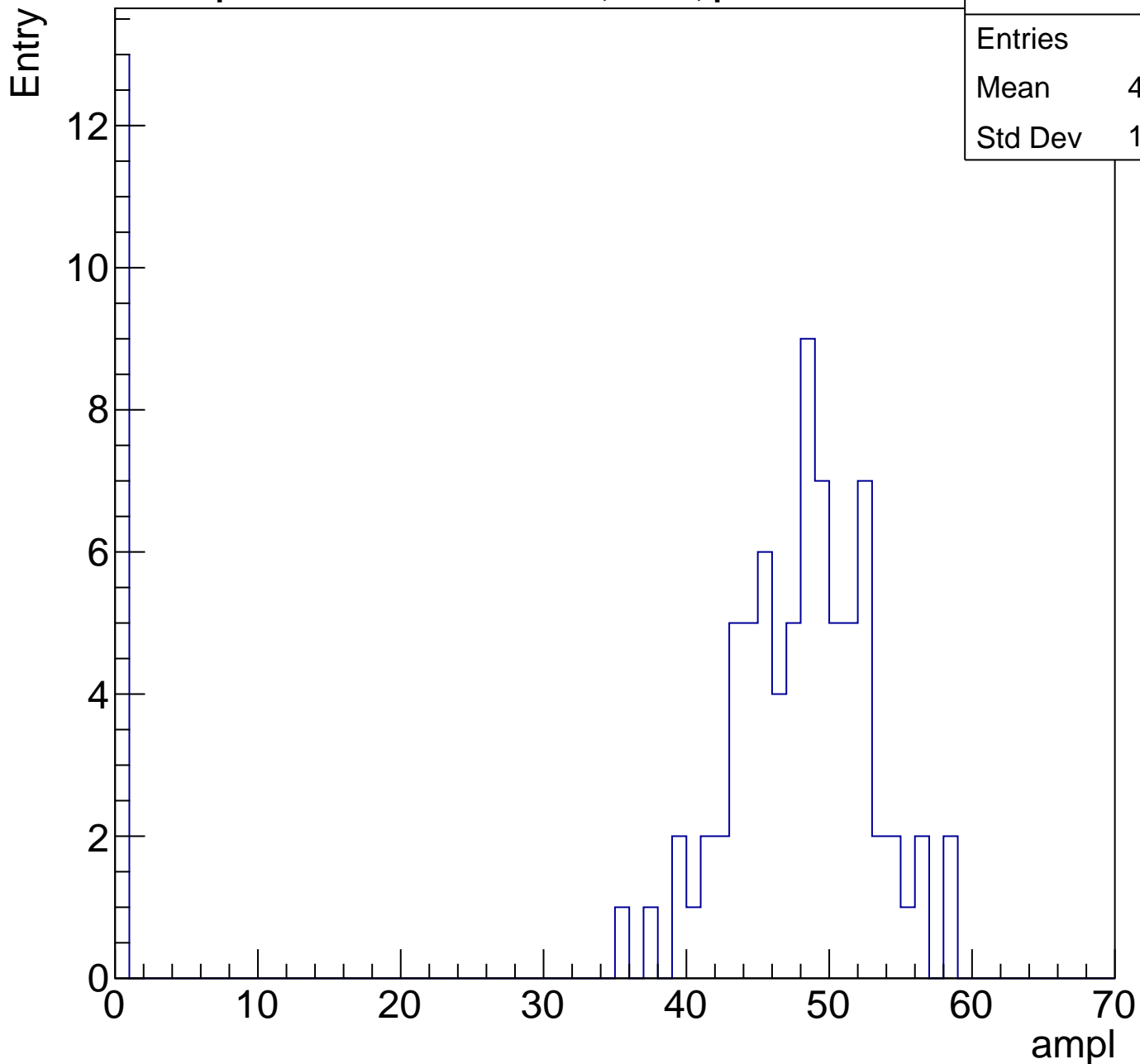
Entries	65
Mean	38.31
Std Dev	9.054



# B1L103S, U25-ch126, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	89
Mean	40.69
Std Dev	17.37

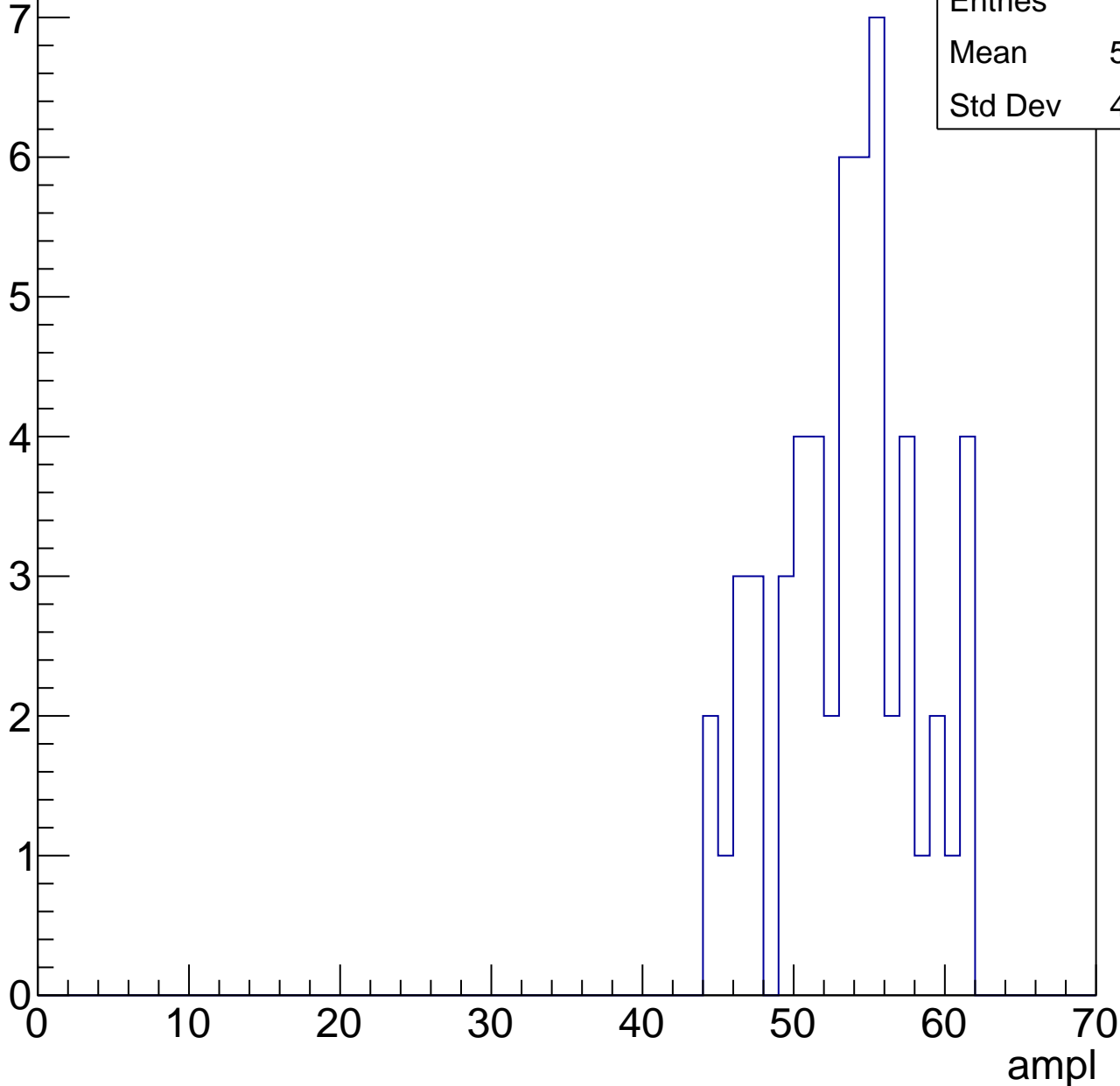


# B1L103S, U25-ch126, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	55
Mean	52.98
Std Dev	4.474

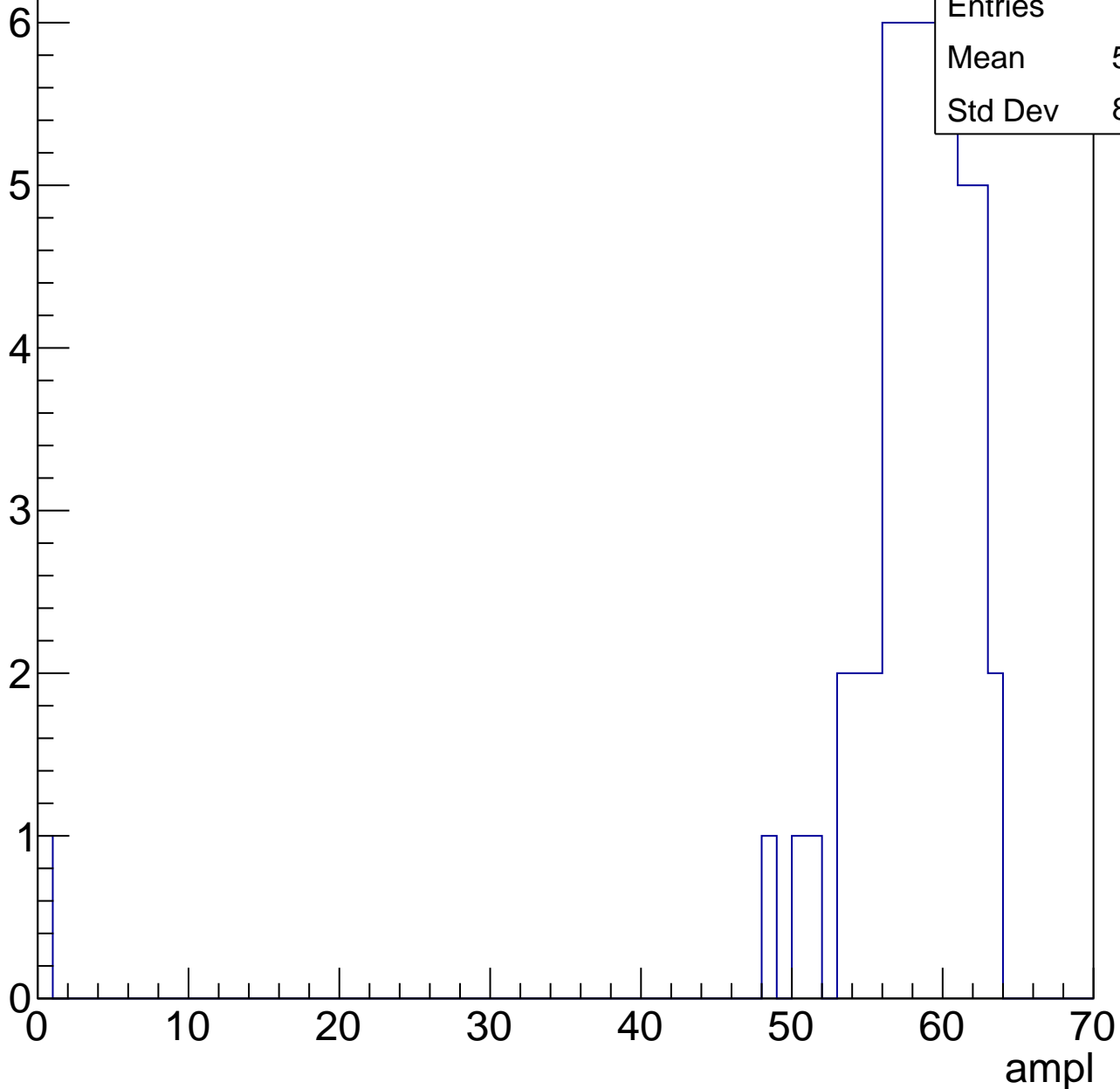


# B1L103S, U25-ch126, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	52
Mean	56.81
Std Dev	8.591

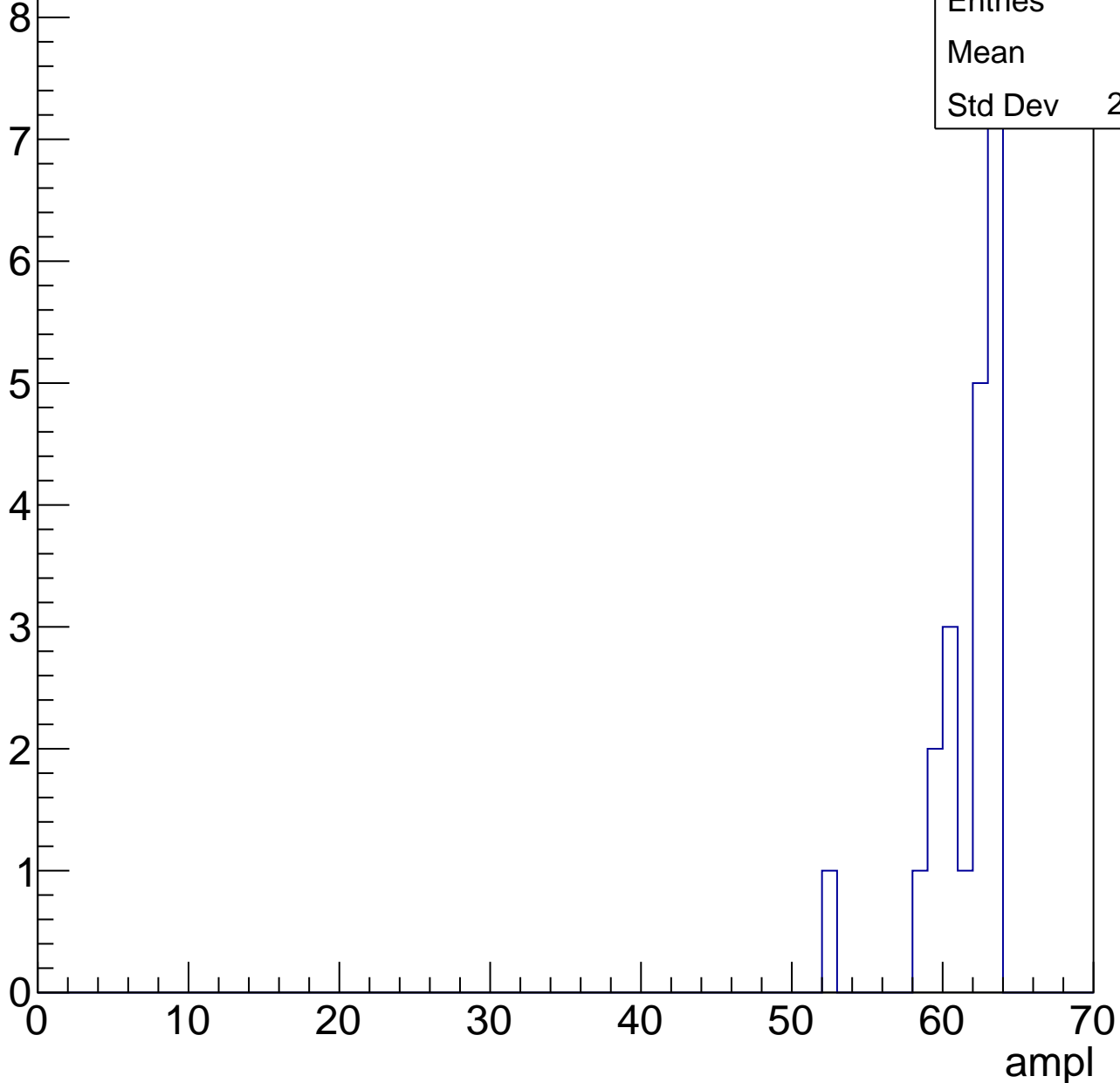


# B1L103S, U25-ch126, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	21
Mean	61.1
Std Dev	2.562





# B1L103S, U25-ch126, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Entries	18
Mean	0
Std Dev	0

ampl

# B1L103S, U25-ch127, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

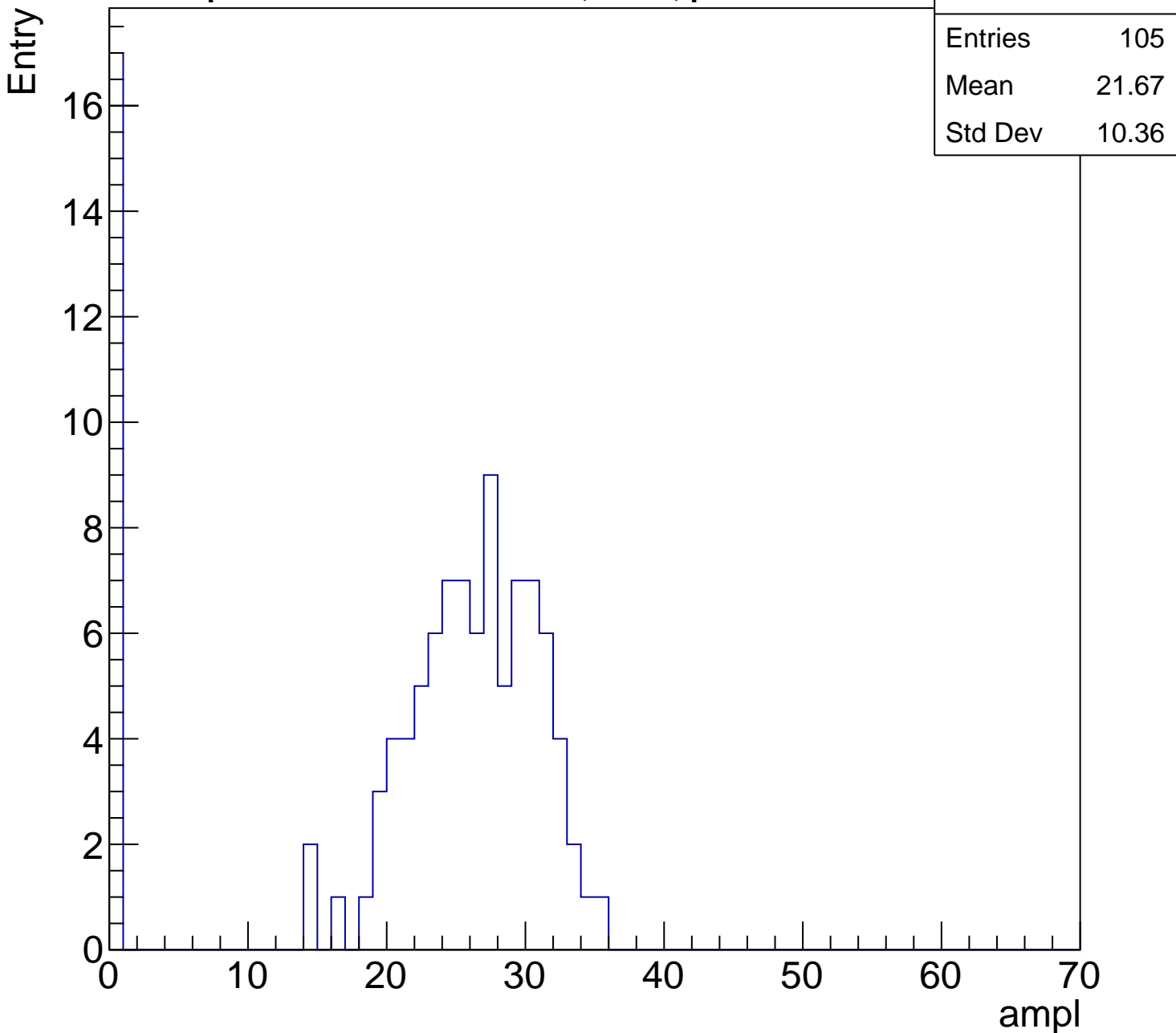
Entries	105
Mean	21.67
Std Dev	10.36

Entry

16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

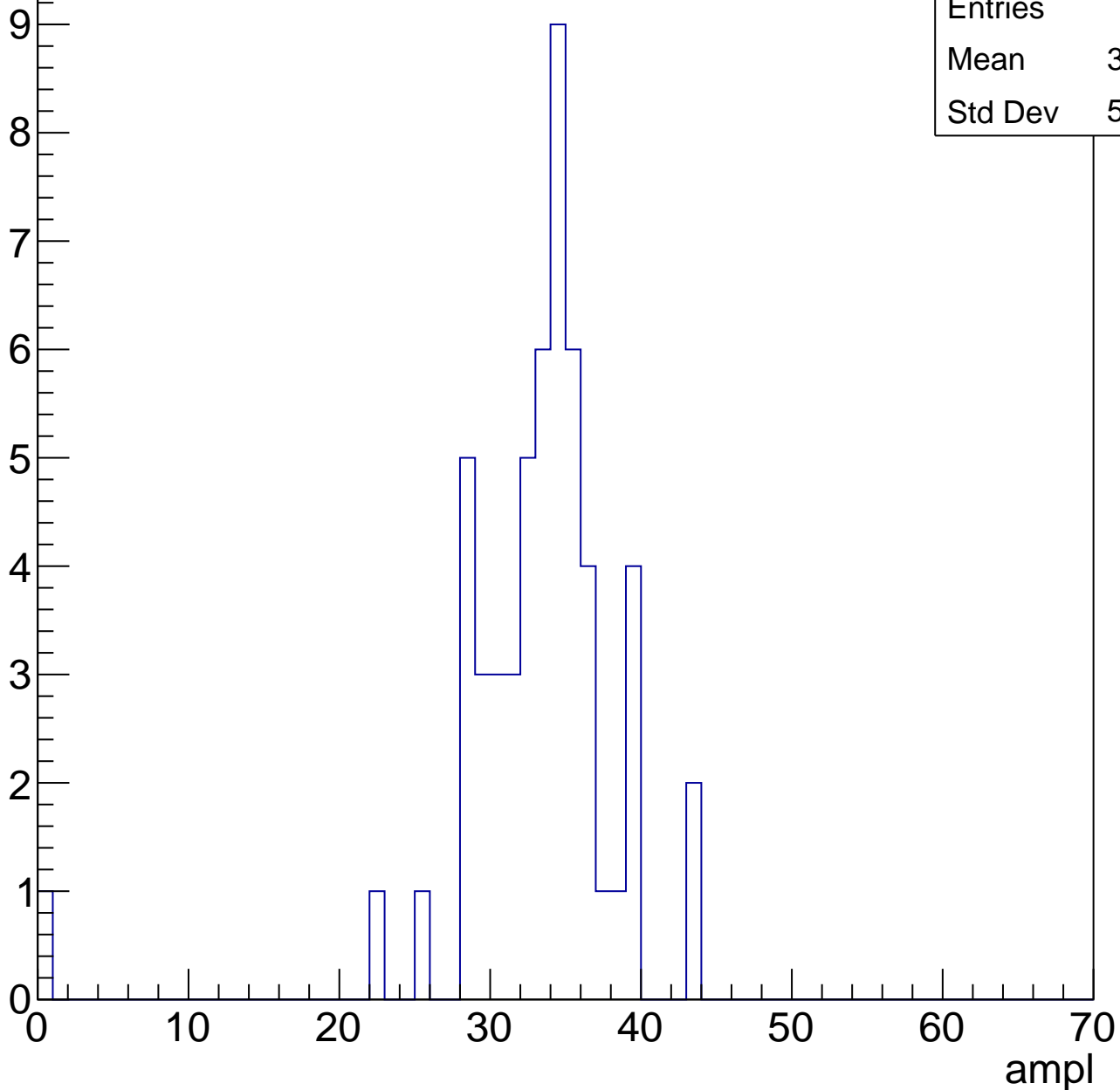


# B1L103S, U25-ch127, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

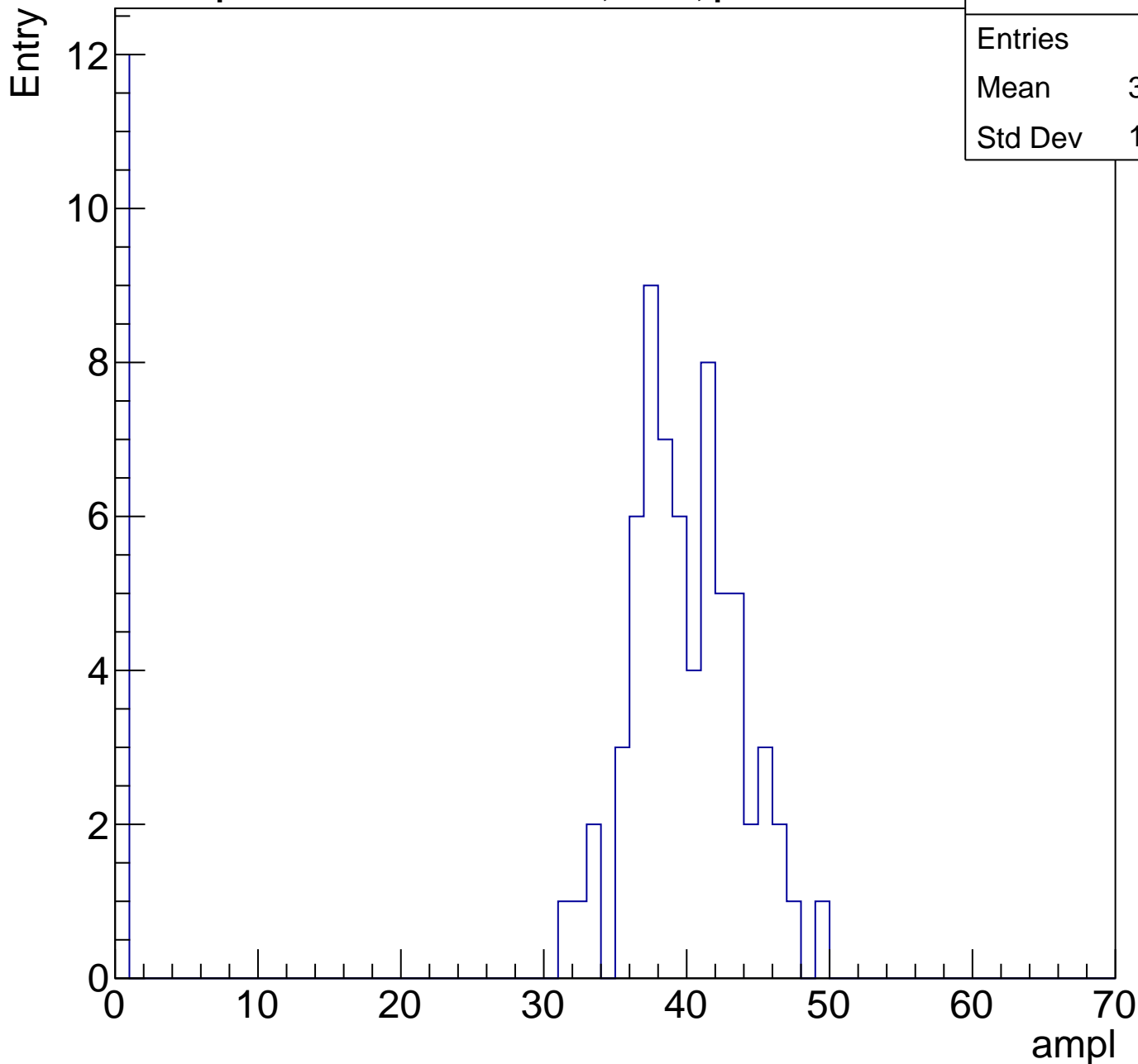
Entries	55
Mean	32.58
Std Dev	5.932



# B1L103S, U25-ch127, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	78
Mean	33.42
Std Dev	14.65

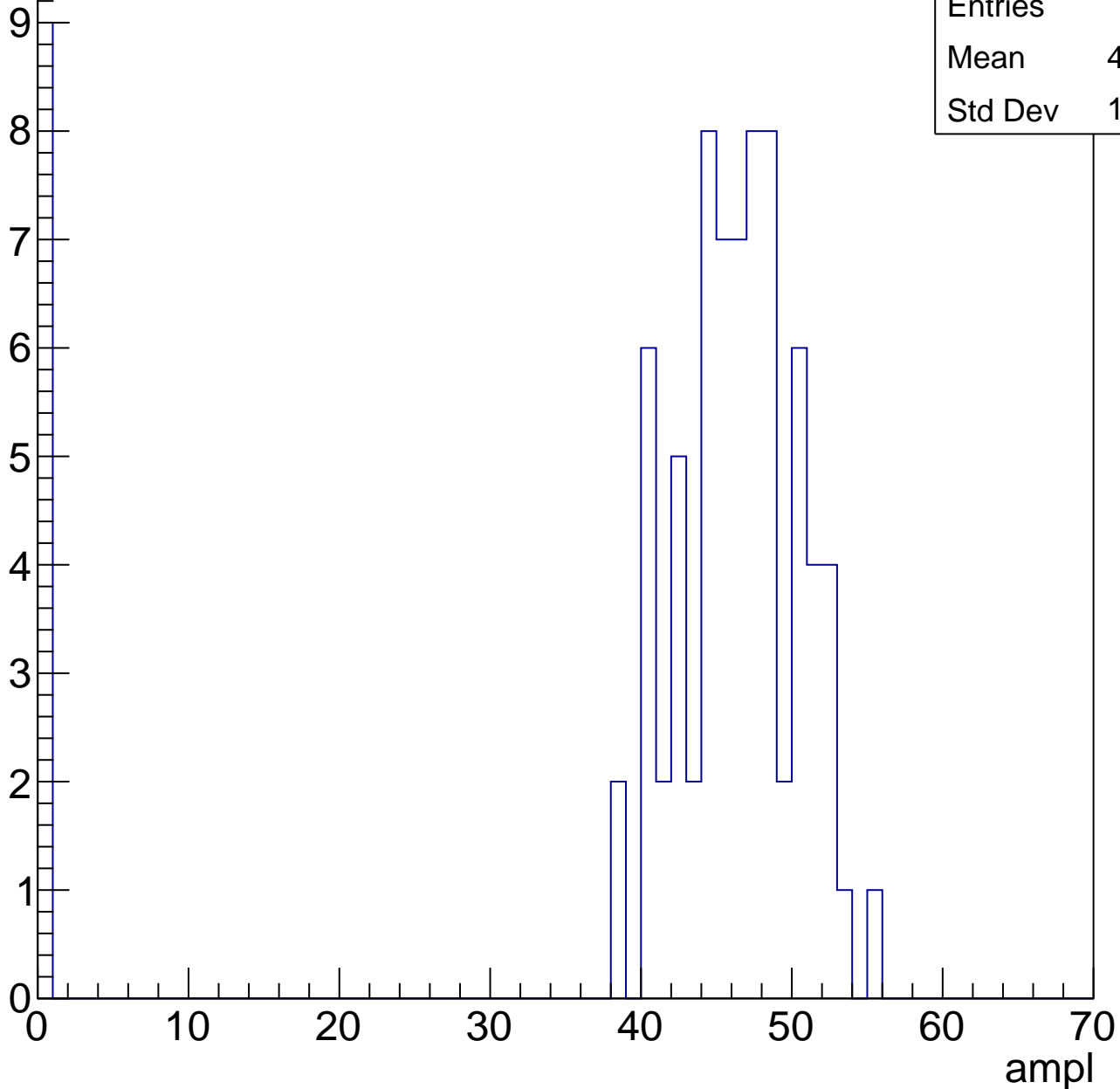


# B1L103S, U25-ch127, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	82
Mean	40.99
Std Dev	14.83

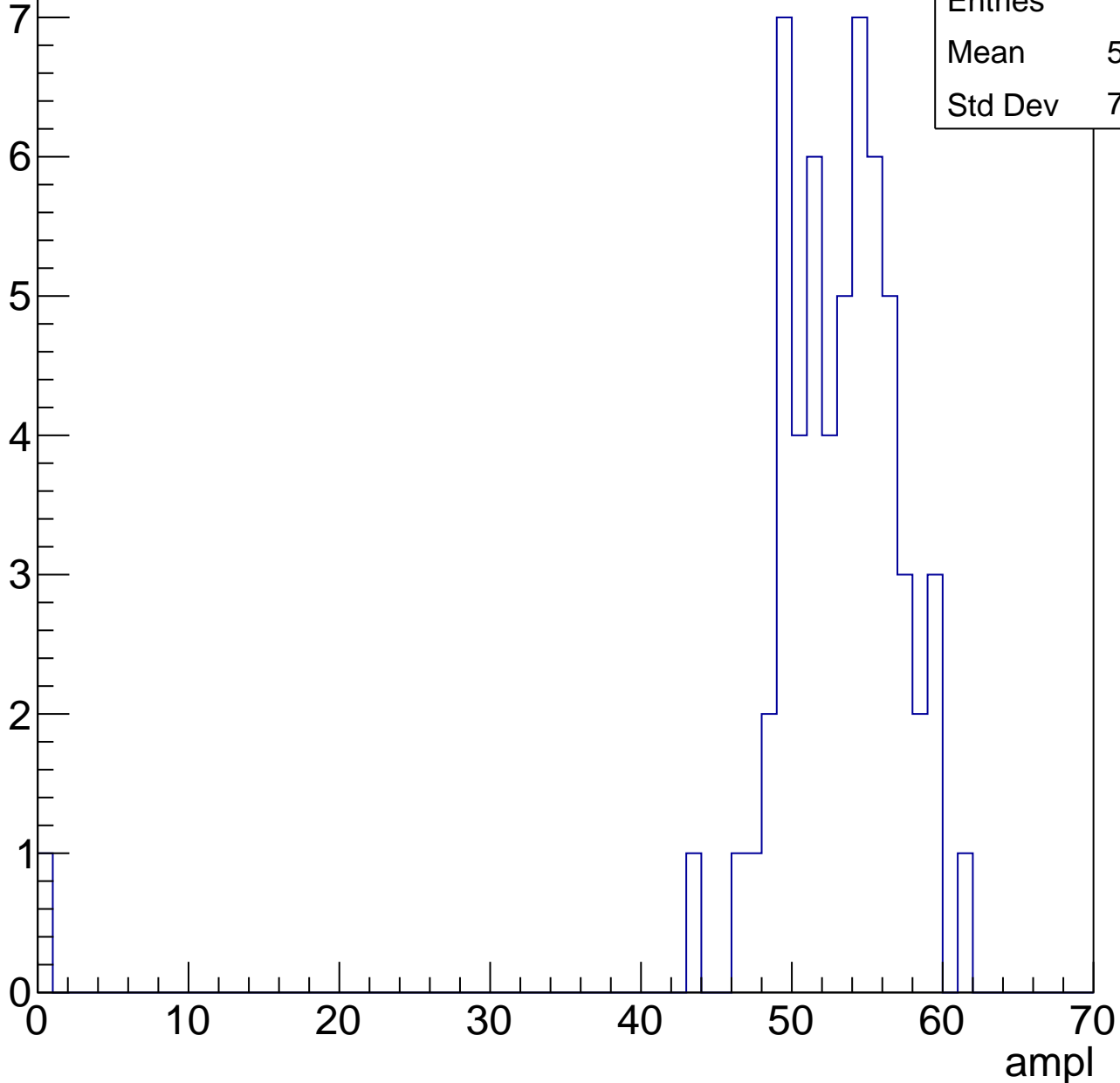


# B1L103S, U25-ch127, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

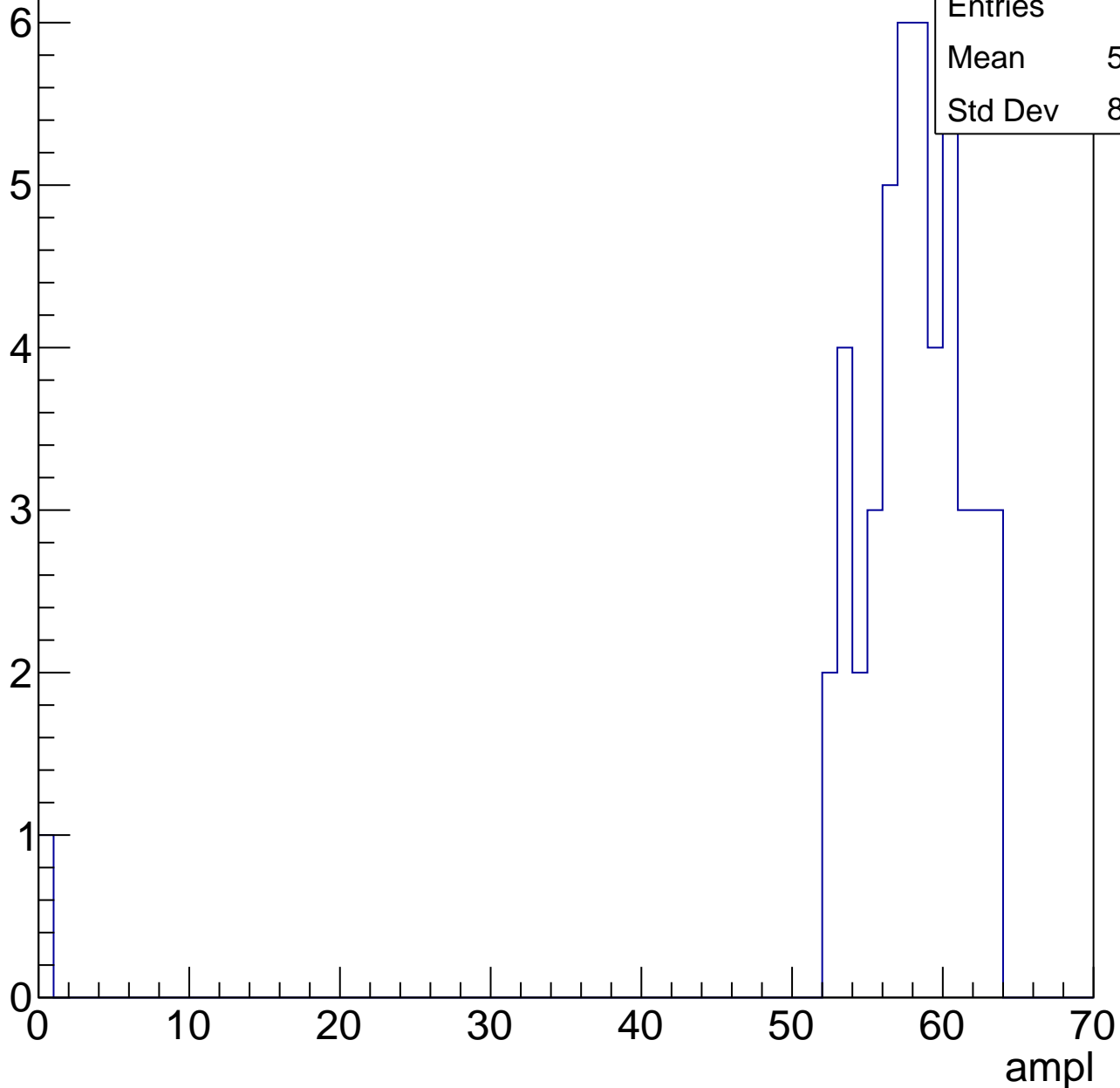
Entries	59
Mean	51.98
Std Dev	7.708



# B1L103S, U25-ch127, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

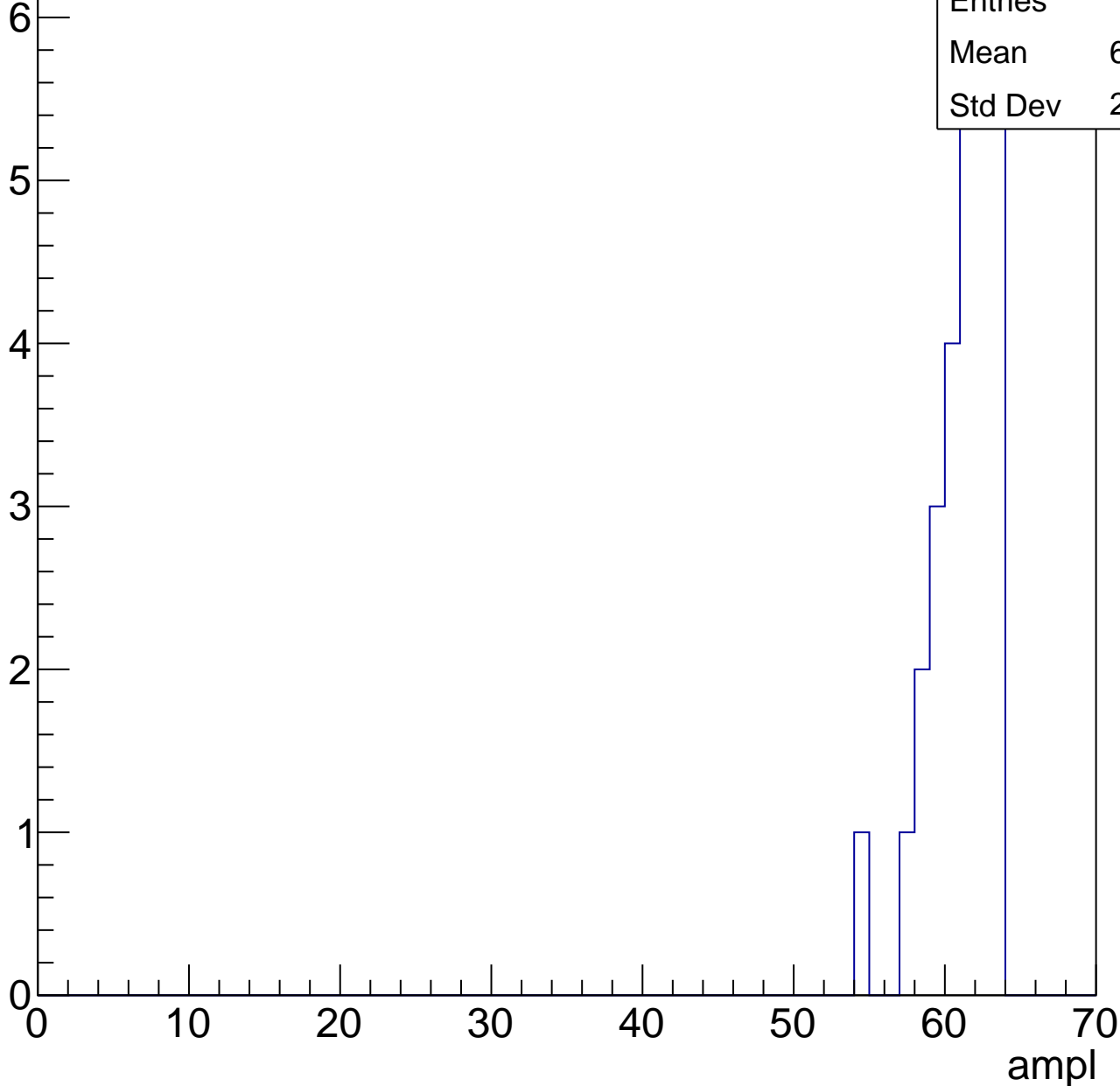


# B1L103S, U25-ch127, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	29
Mean	60.69
Std Dev	2.086

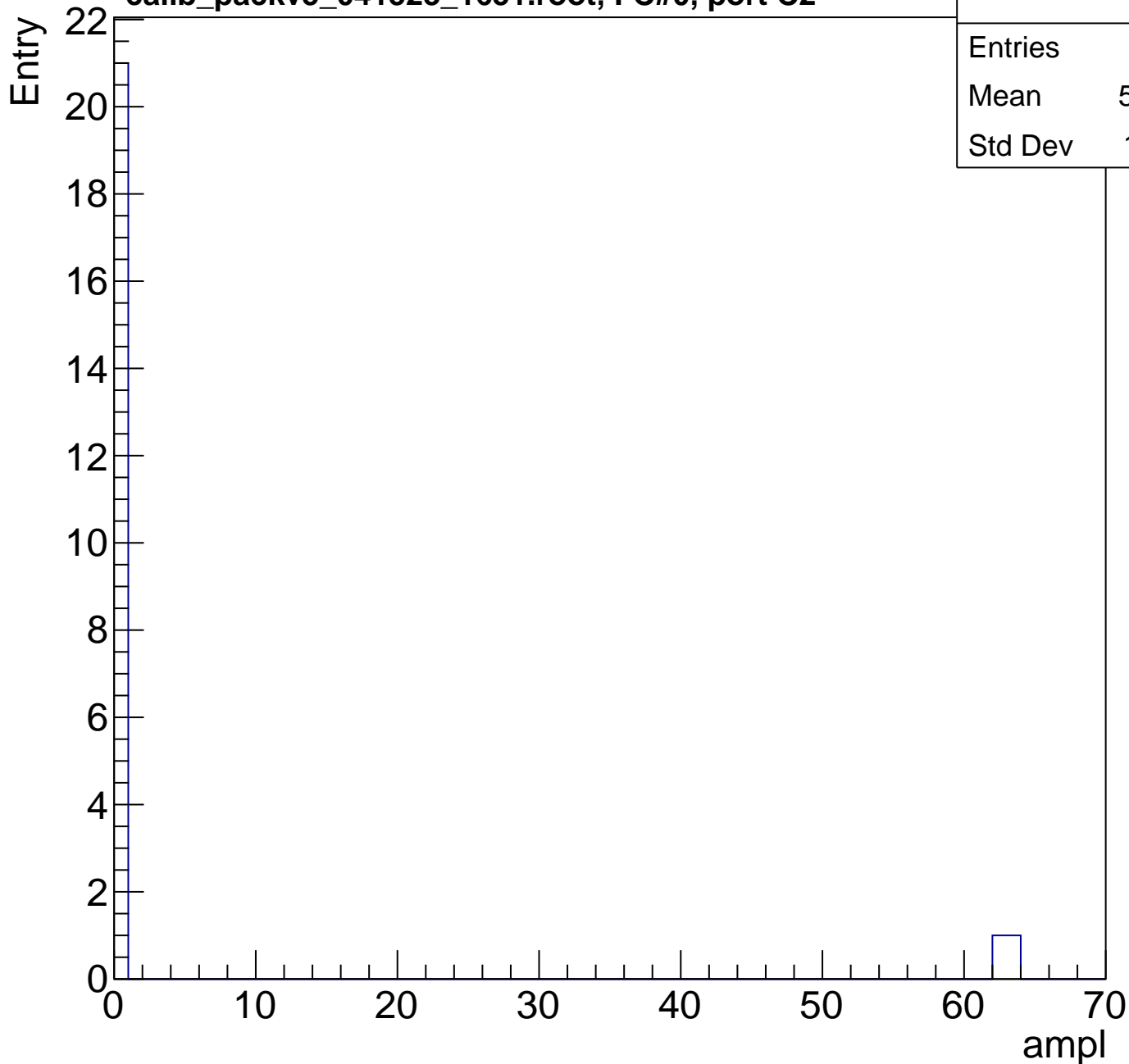




# B1L103S, U25-ch127, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	23
Mean	5.435
Std Dev	17.61



# B1L103S, U25-ch127, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	23
Mean	5.435
Std Dev	17.61

