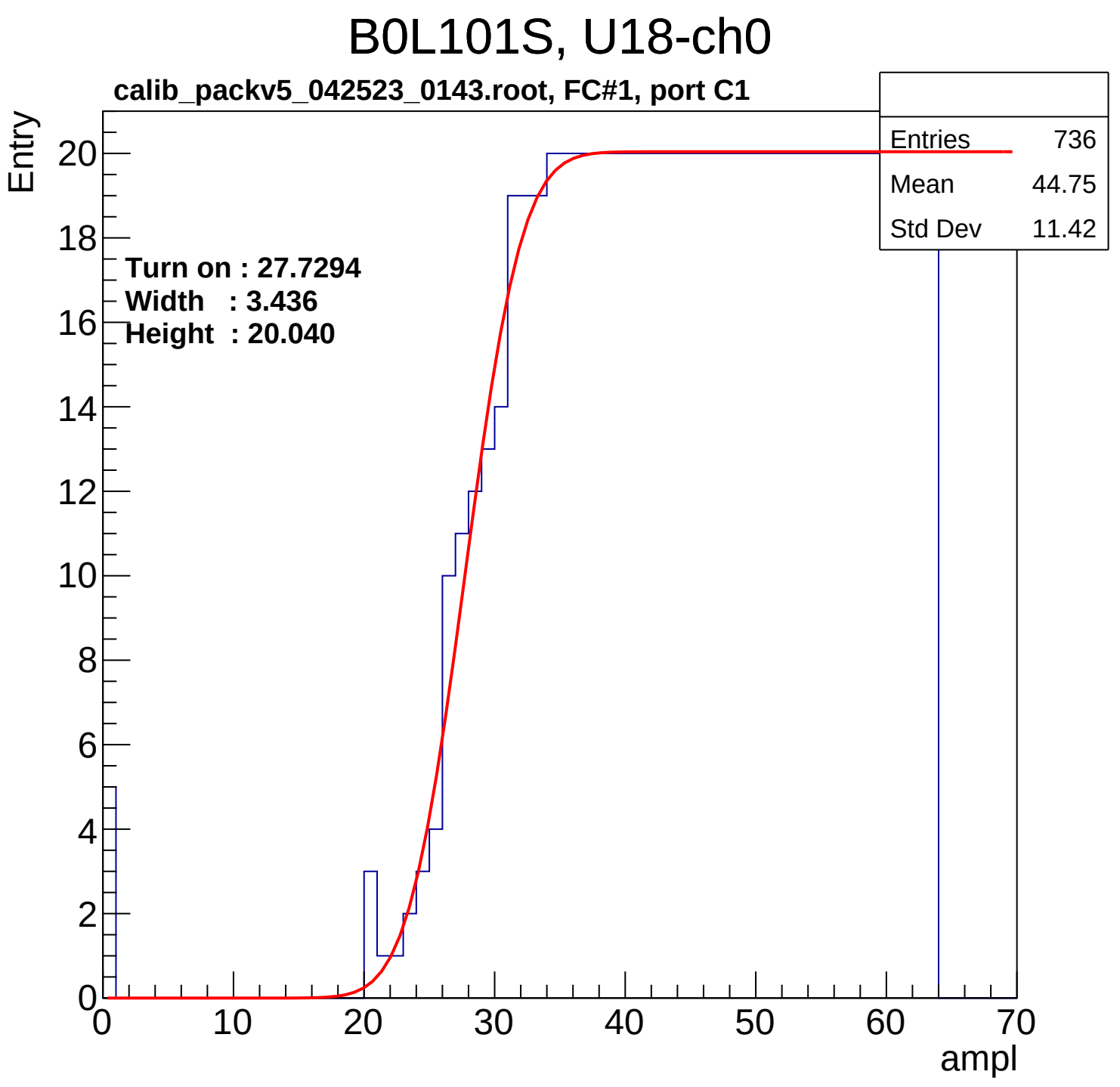
B0L101S, U18-ch0
calib_packv5_042523_0143.root, FC#1, port C1
Entries 736
Mean 44.75
Std Dev 11.42
Turn on : 27.7294
Width : 3.436
Height : 20.040
Entry
ampl
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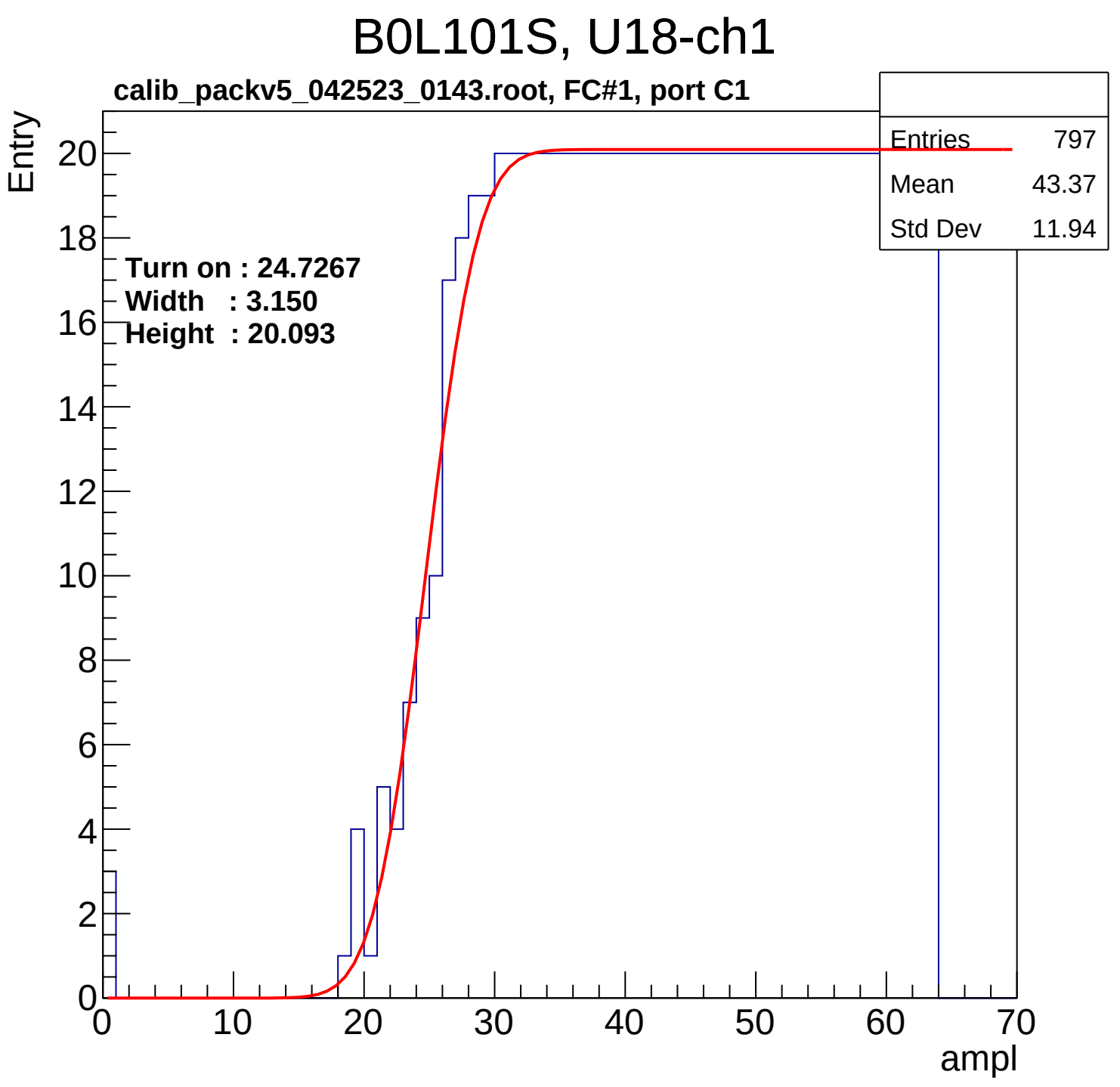
B0L101S, U18-ch1
calib_packv5_042523_0143.root, FC#1, port C1
Entries 797
Mean 43.37
Std Dev 11.94
Turn on : 24.7267
Width : 3.150
Height : 20.093
Entry
ampl
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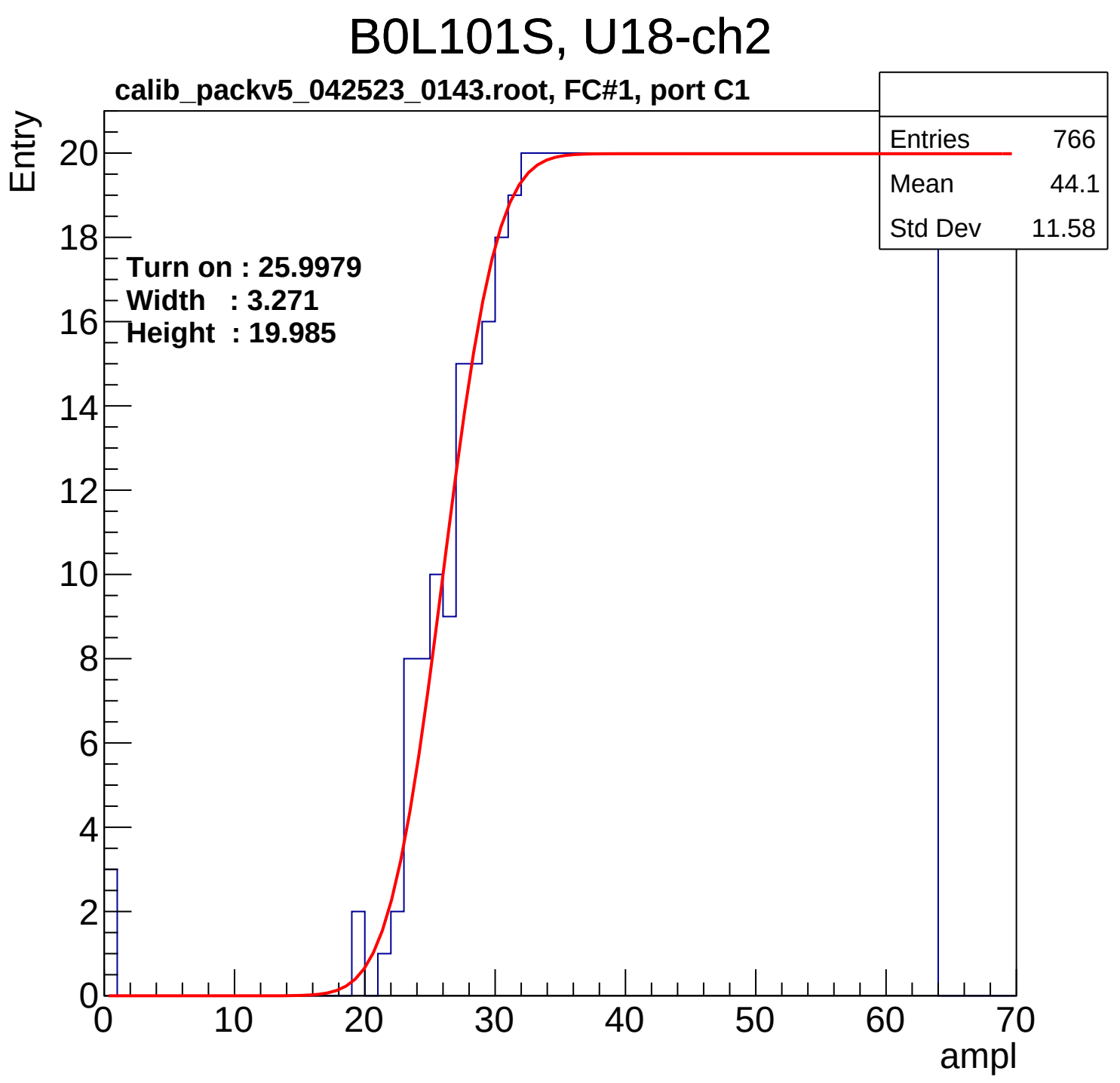
B0L101S, U18-ch2
calib_packv5_042523_0143.root, FC#1, port C1
Entries 766
Mean 44.1
Std Dev 11.58
Turn on : 25.9979
Width : 3.271
Height : 19.985
Entry
ampl
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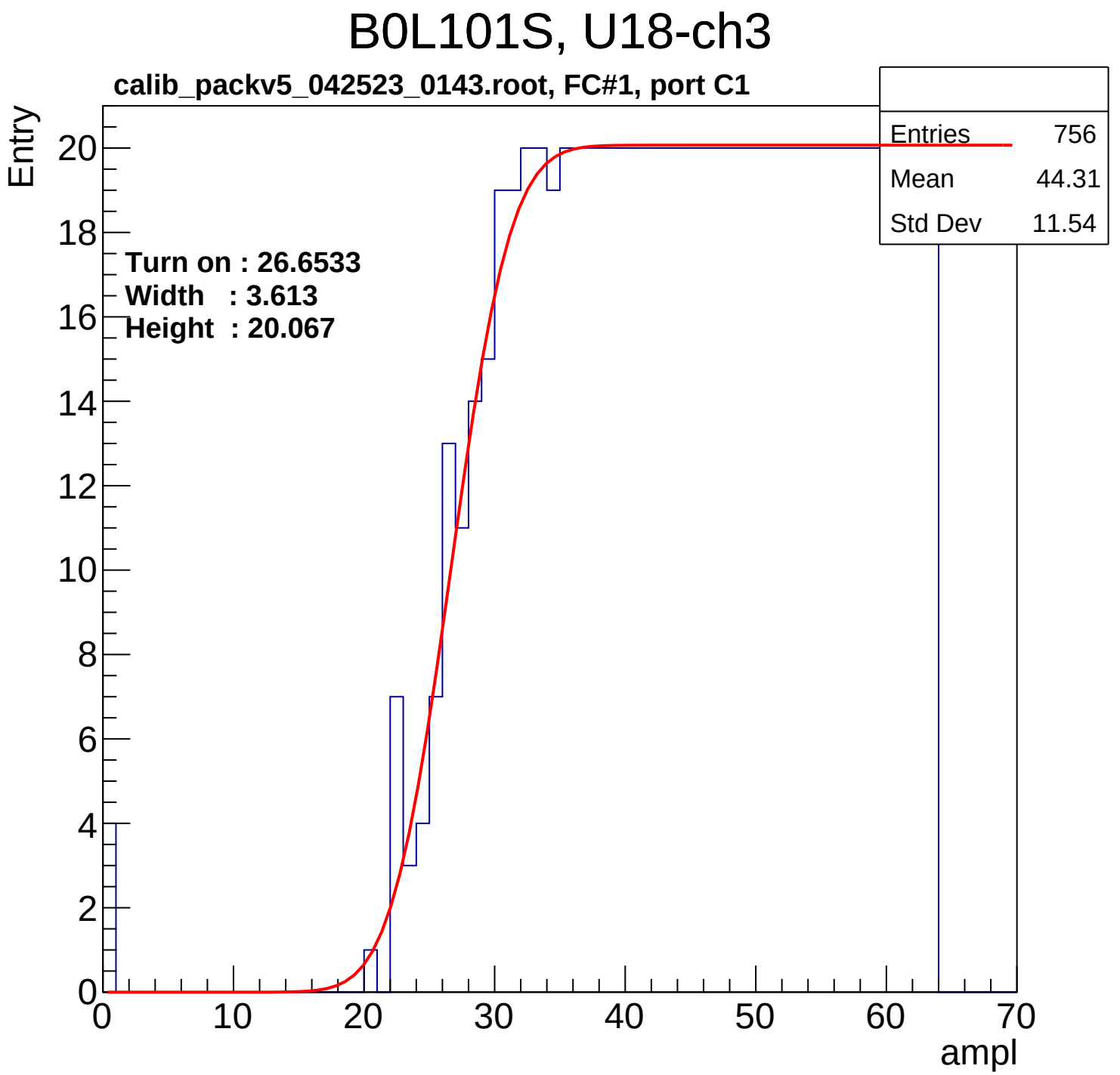
B0L101S, U18-ch3
calib_packv5_042523_0143.root, FC#1, port C1
Entries 756
Mean 44.31
Std Dev 11.54
Turn on : 26.6533
Width : 3.613
Height : 20.067
Entry
ampl
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6
8
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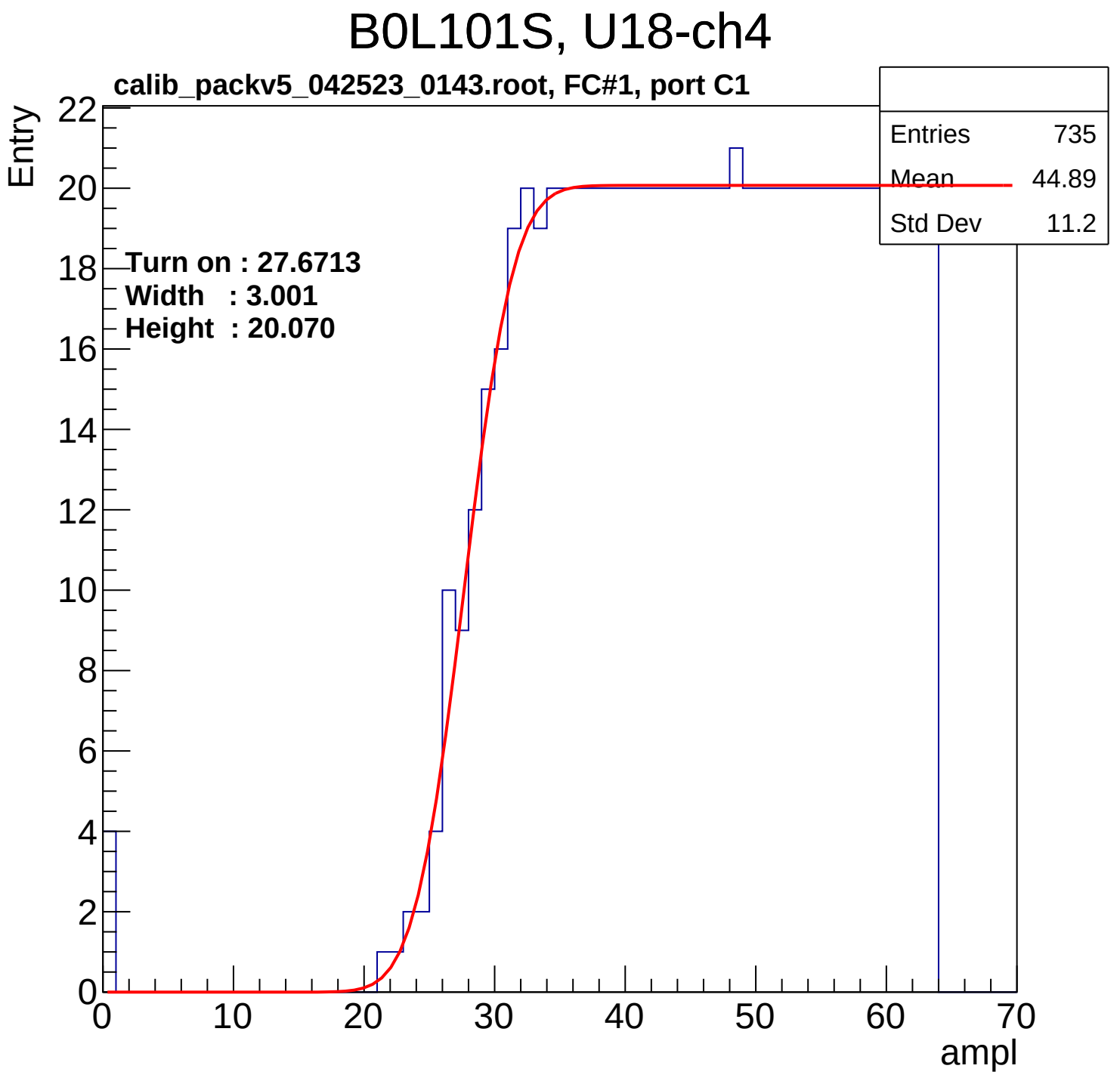
B0L101S, U18-ch4
calib_packv5_042523_0143.root, FC#1, port C1
Entries 735
Mean 44.89
Std Dev 11.2
Turn on : 27.6713
Width : 3.001
Height : 20.070
Entry
ampl
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8
10
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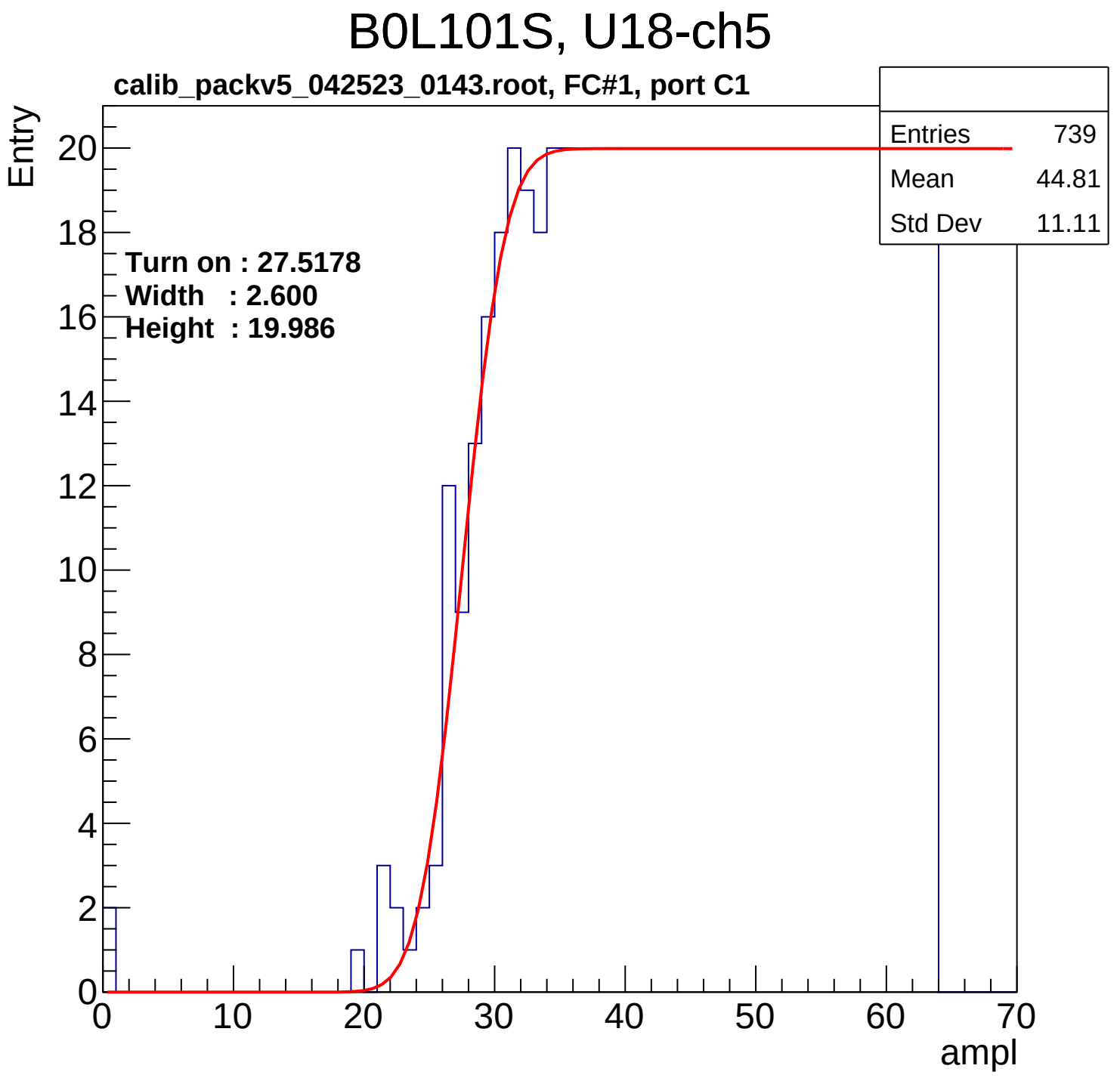
B0L101S, U18-ch5
calib_packv5_042523_0143.root, FC#1, port C1
Entries 739
Mean 44.81
Std Dev 11.11
Turn on : 27.5178
Width : 2.600
Height : 19.986
Entry
ampl
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6
8
10
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16
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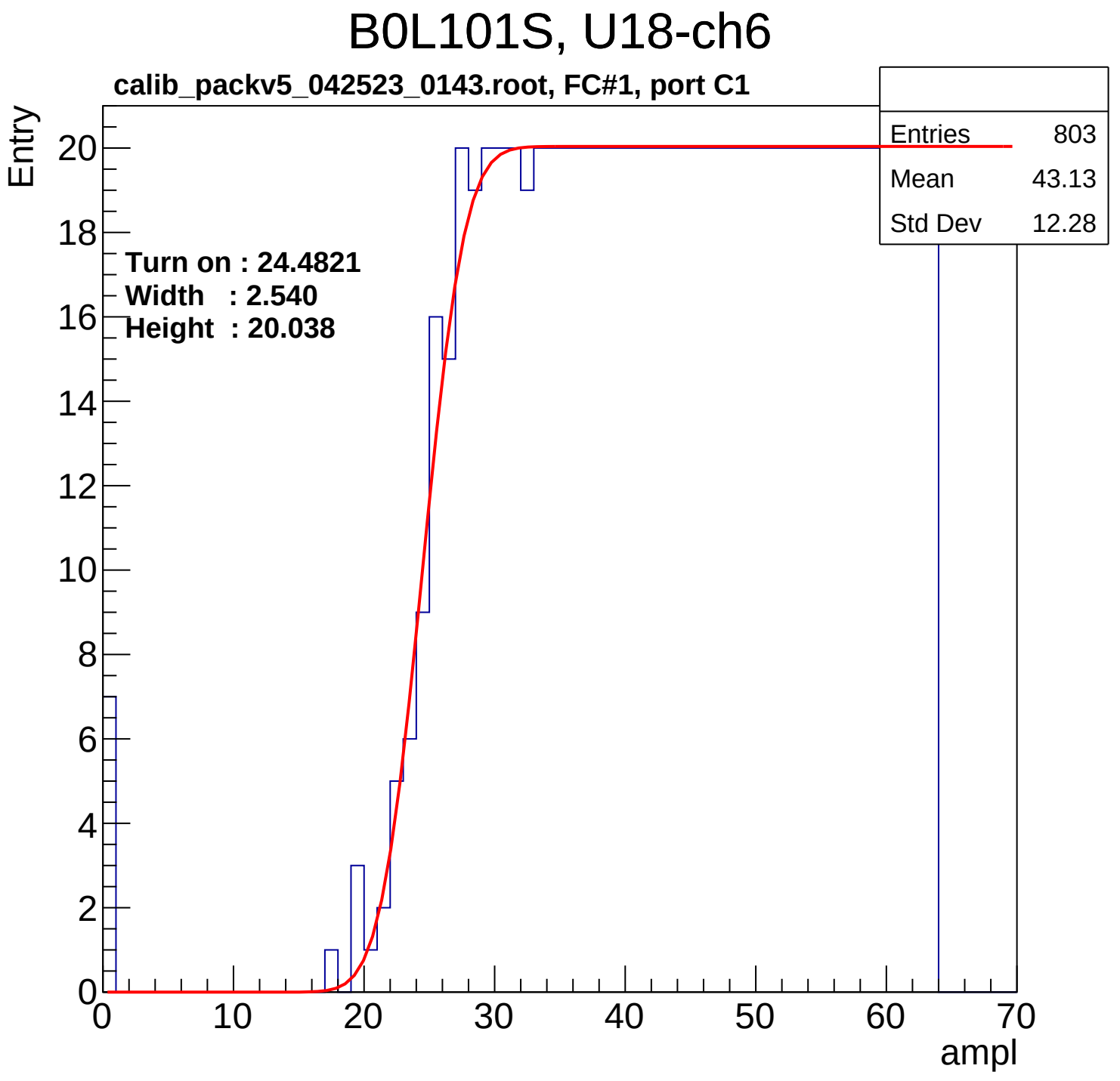
B0L101S, U18-ch6
calib_packv5_042523_0143.root, FC#1, port C1
Entries 803
Mean 43.13
Std Dev 12.28
Turn on : 24.4821
Width : 2.540
Height : 20.038
Entry
ampl
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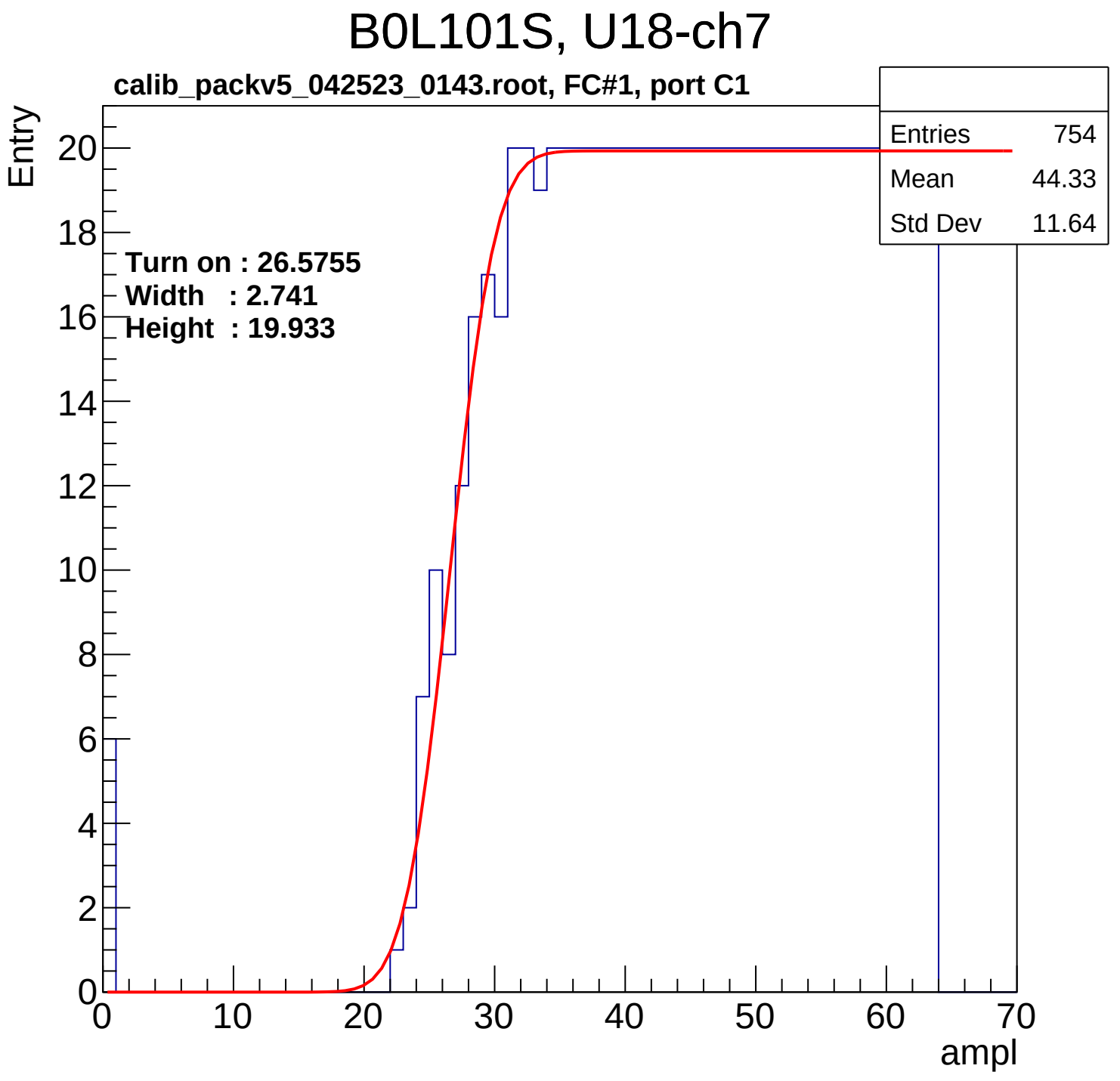
B0L101S, U18-ch7
calib_packv5_042523_0143.root, FC#1, port C1
Entries 754
Mean 44.33
Std Dev 11.64
Turn on : 26.5755
Width : 2.741
Height : 19.933
Entry
ampl
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6
8
10
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14
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0
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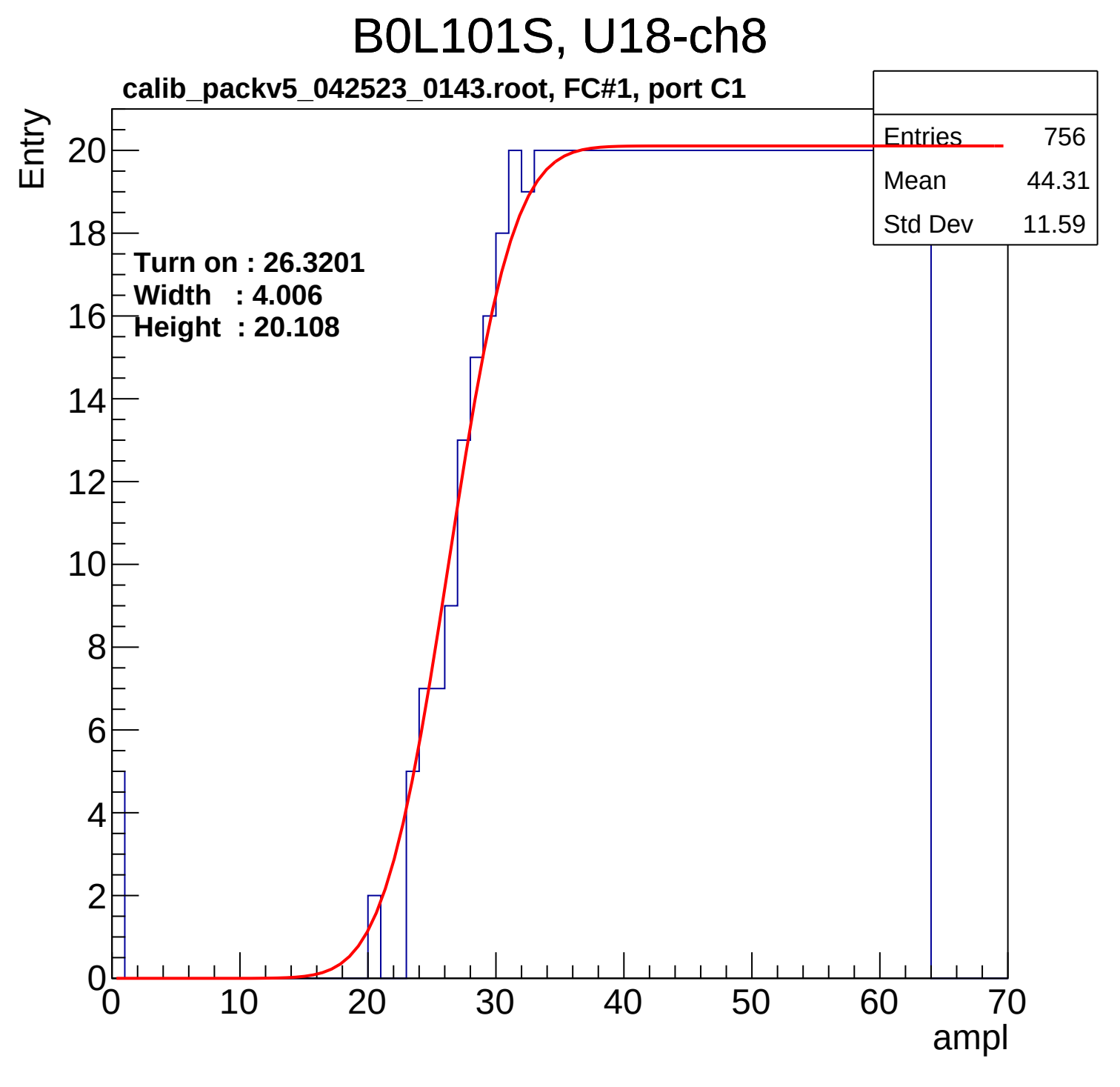
B0L101S, U18-ch8
calib_packv5_042523_0143.root, FC#1, port C1
Entries 756
Mean 44.31
Std Dev 11.59
Turn on : 26.3201
Width : 4.006
Height : 20.108
Entry
ampl
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6
8
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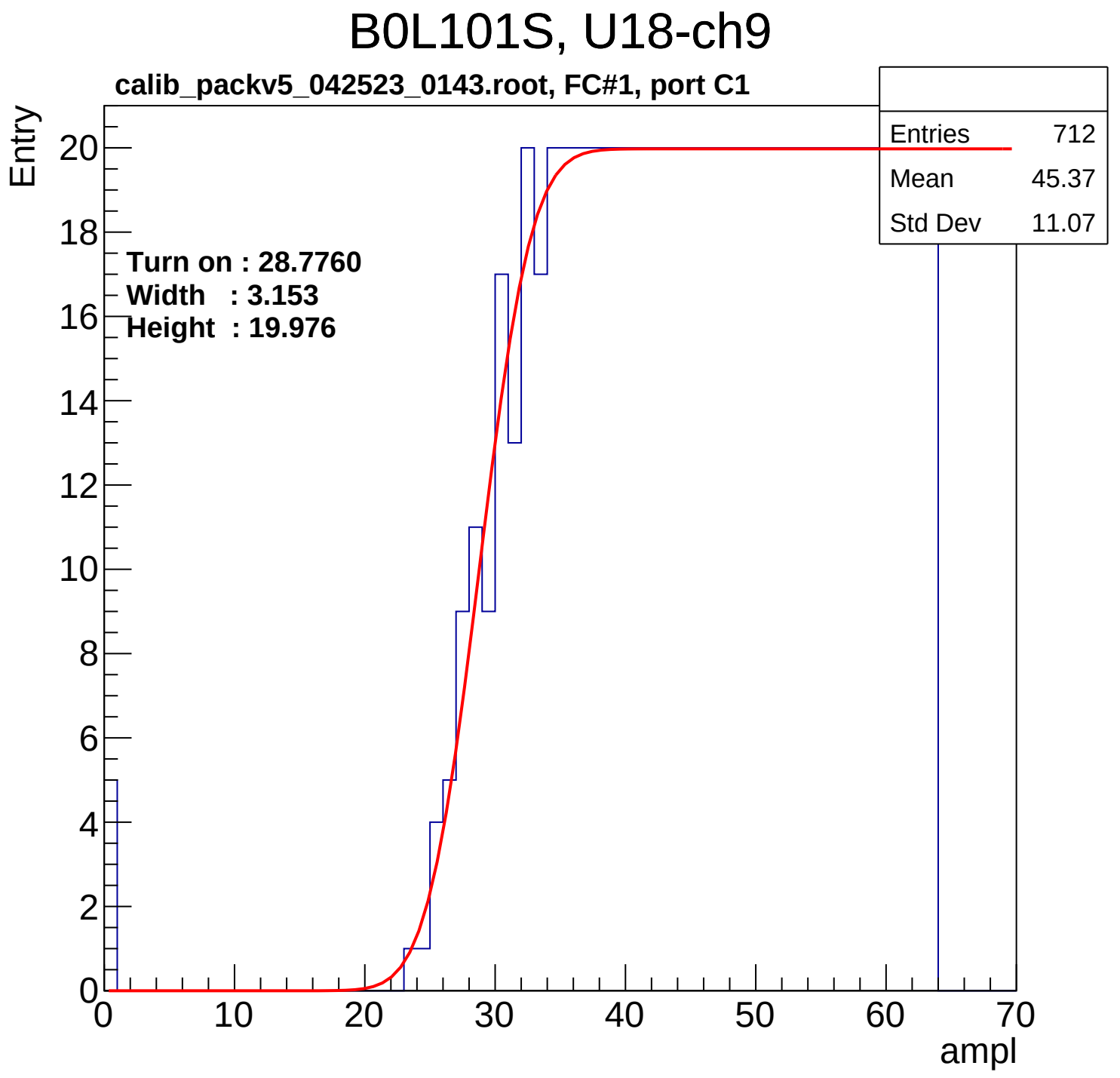
B0L101S, U18-ch9
calib_packv5_042523_0143.root, FC#1, port C1
Entries 712
Mean 45.37
Std Dev 11.07
Turn on : 28.7760
Width : 3.153
Height : 19.976
Entry
ampl
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6
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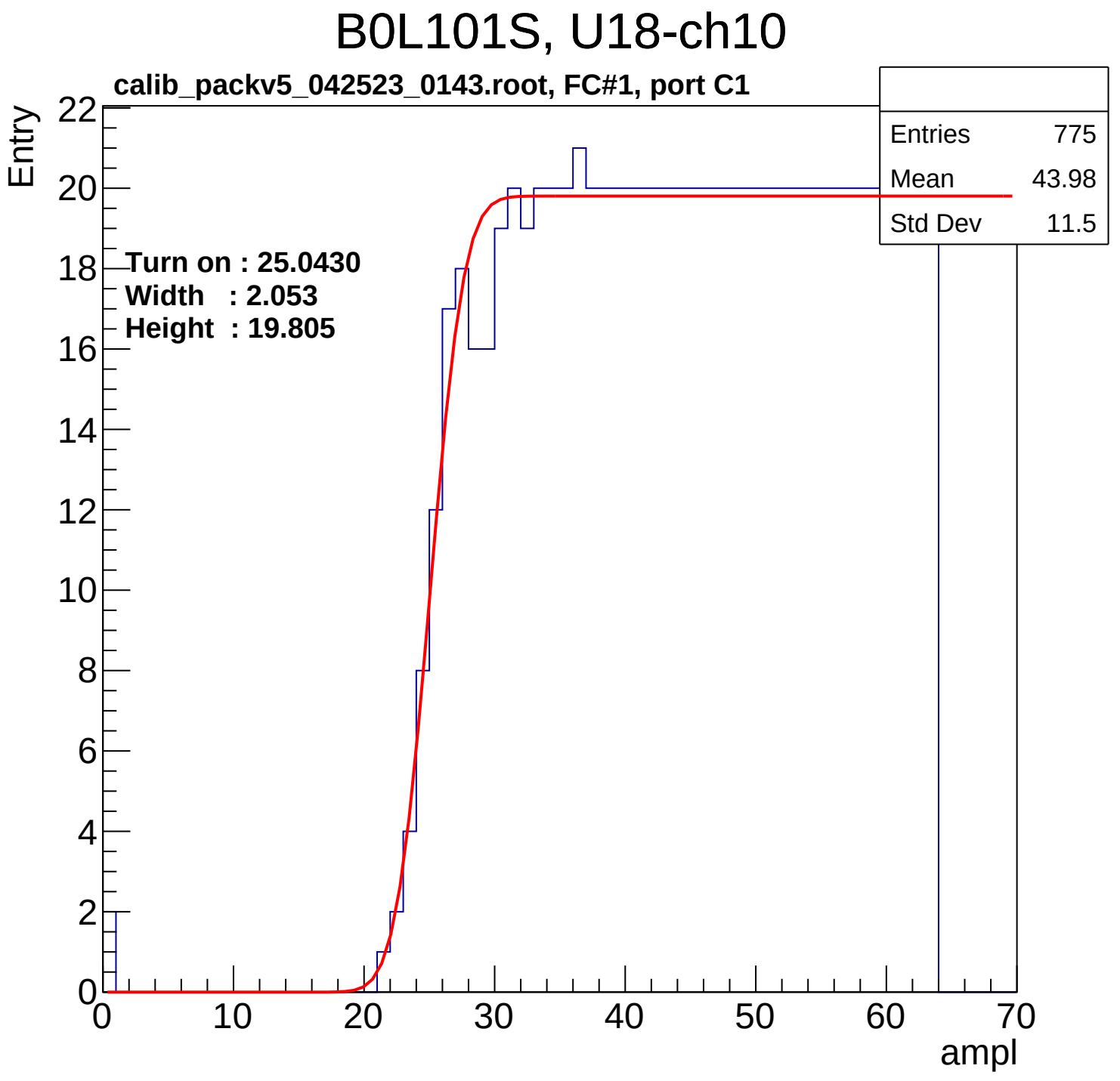
B0L101S, U18-ch10
calib_packv5_042523_0143.root, FC#1, port C1
Entries 775
Mean 43.98
Std Dev 11.5
Turn on : 25.0430
Width : 2.053
Height : 19.805
Entry
ampl
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8
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16
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20
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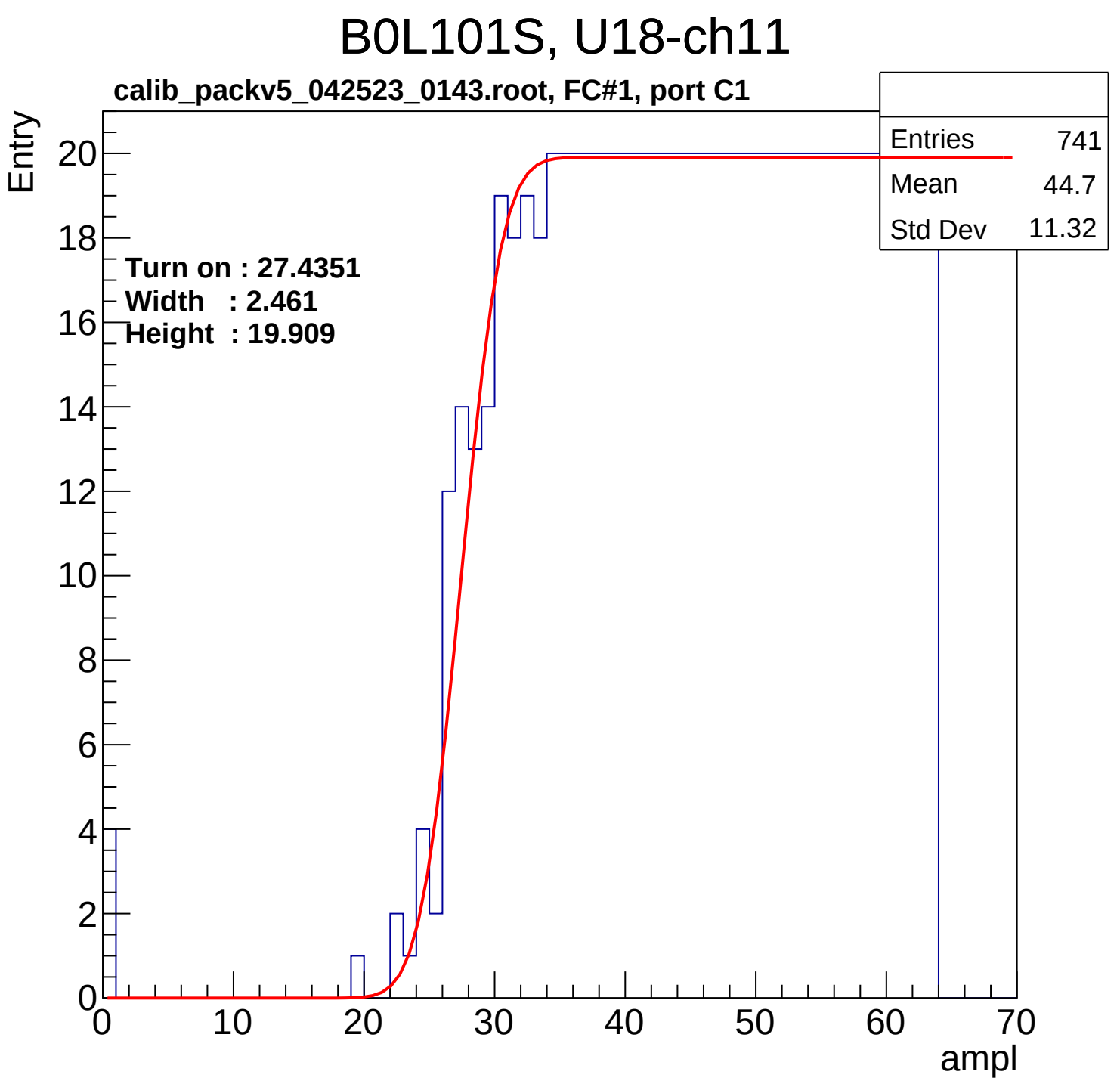
B0L101S, U18-ch11
calib_packv5_042523_0143.root, FC#1, port C1
Entries 741
Mean 44.7
Std Dev 11.32
Turn on : 27.4351
Width : 2.461
Height : 19.909
Entry
ampl
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6
8
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12
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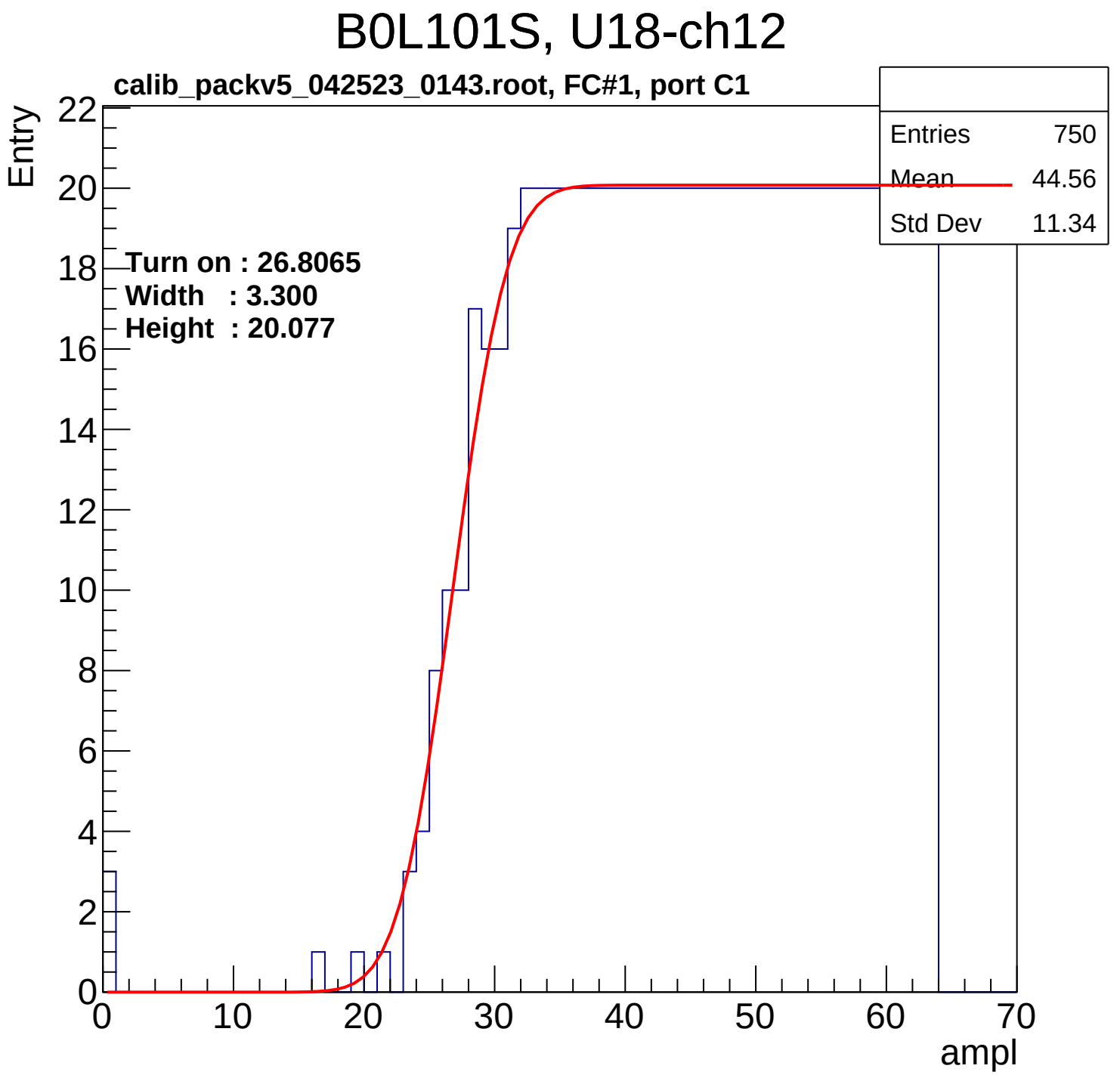
B0L101S, U18-ch12
calib_packv5_042523_0143.root, FC#1, port C1
Entries 750
Mean 44.56
Std Dev 11.34
Turn on : 26.8065
Width : 3.300
Height : 20.077
Entry
ampl
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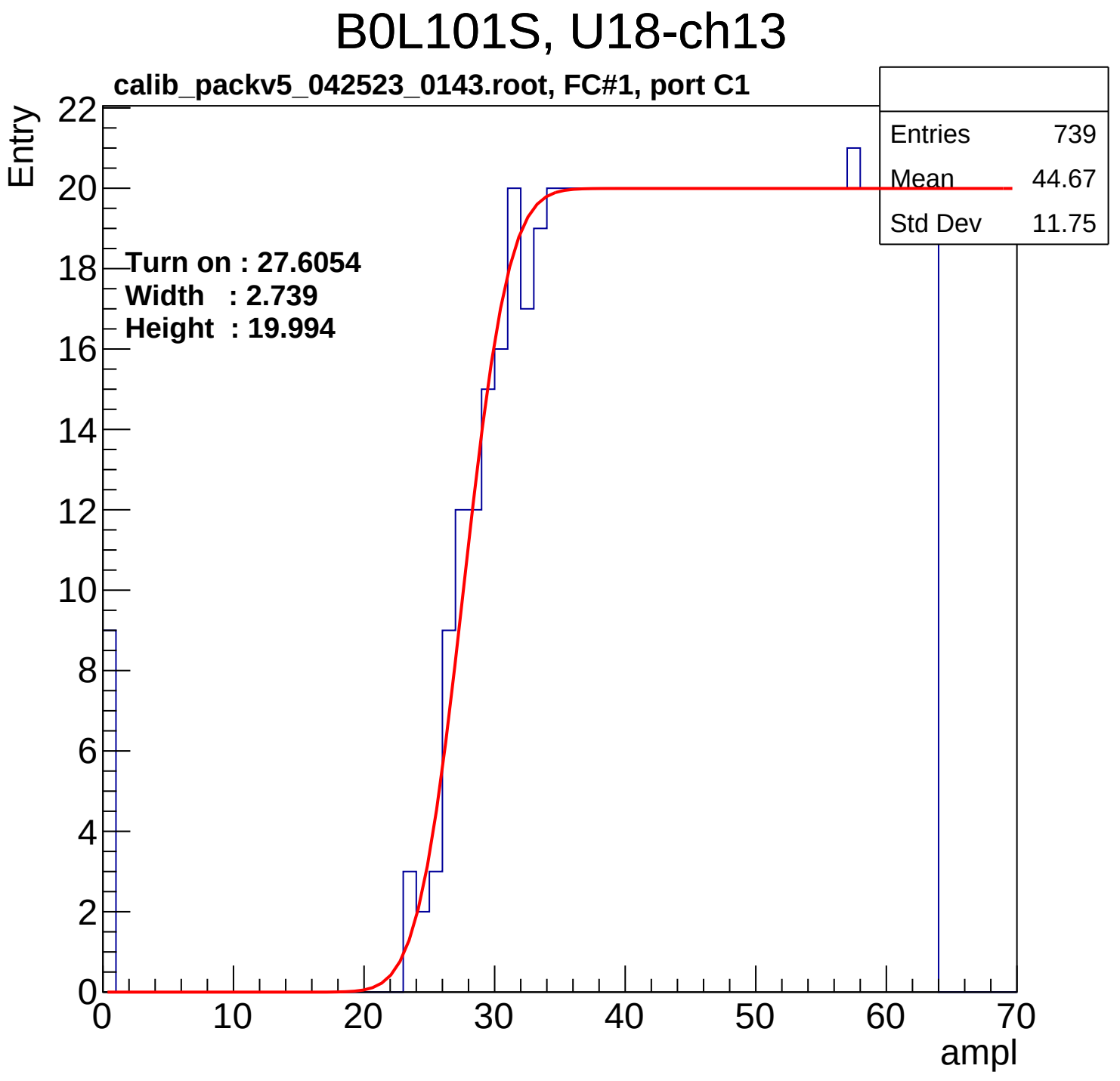
B0L101S, U18-ch13
calib_packv5_042523_0143.root, FC#1, port C1
Entries 739
Mean 44.67
Std Dev 11.75
Turn on : 27.6054
Width : 2.739
Height : 19.994
Entry
ampl
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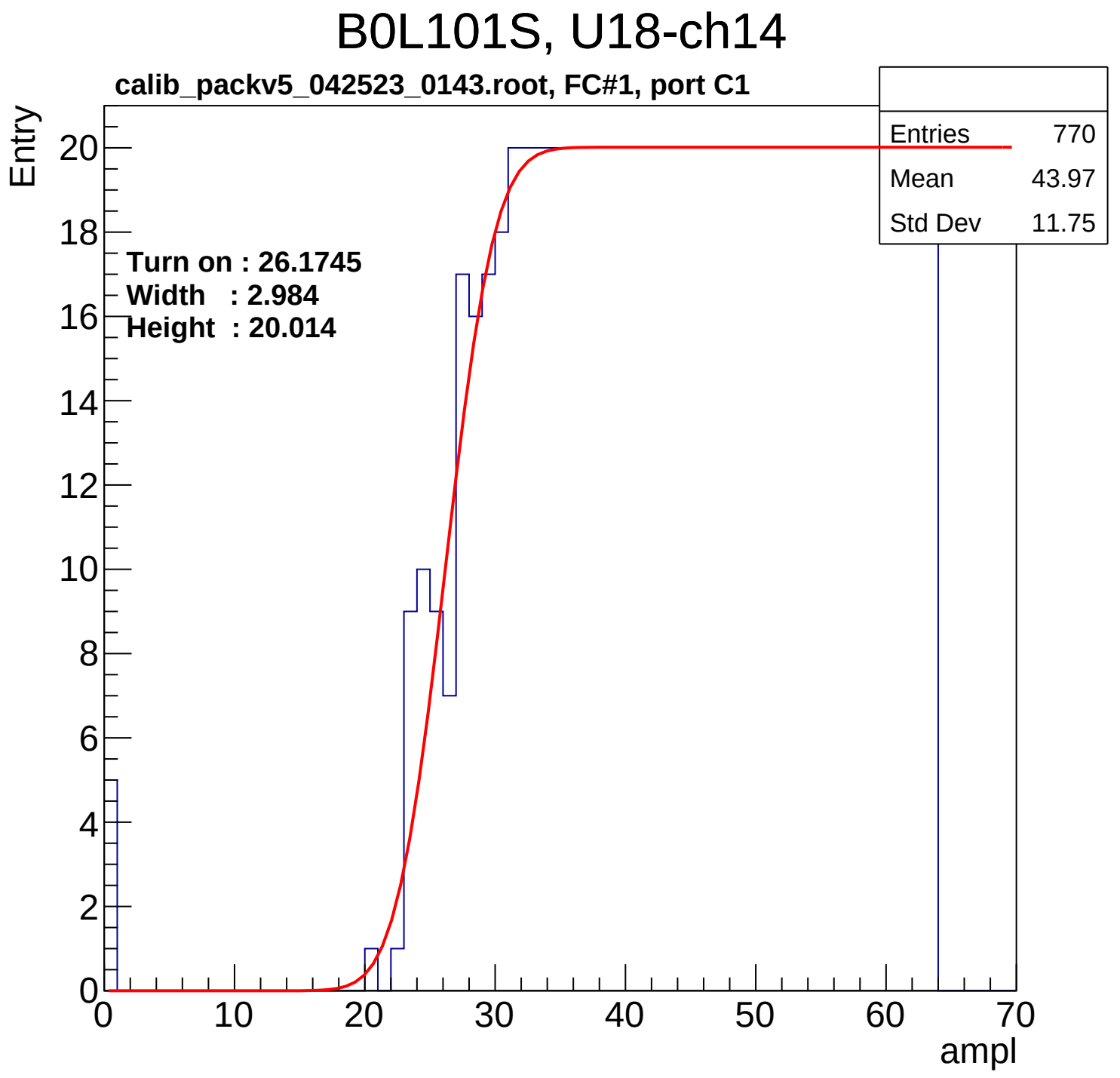
B0L101S, U18-ch14
calib_packv5_042523_0143.root, FC#1, port C1
Entries 770
Mean 43.97
Std Dev 11.75
Turn on : 26.1745
Width : 2.984
Height : 20.014
Entry
ampl
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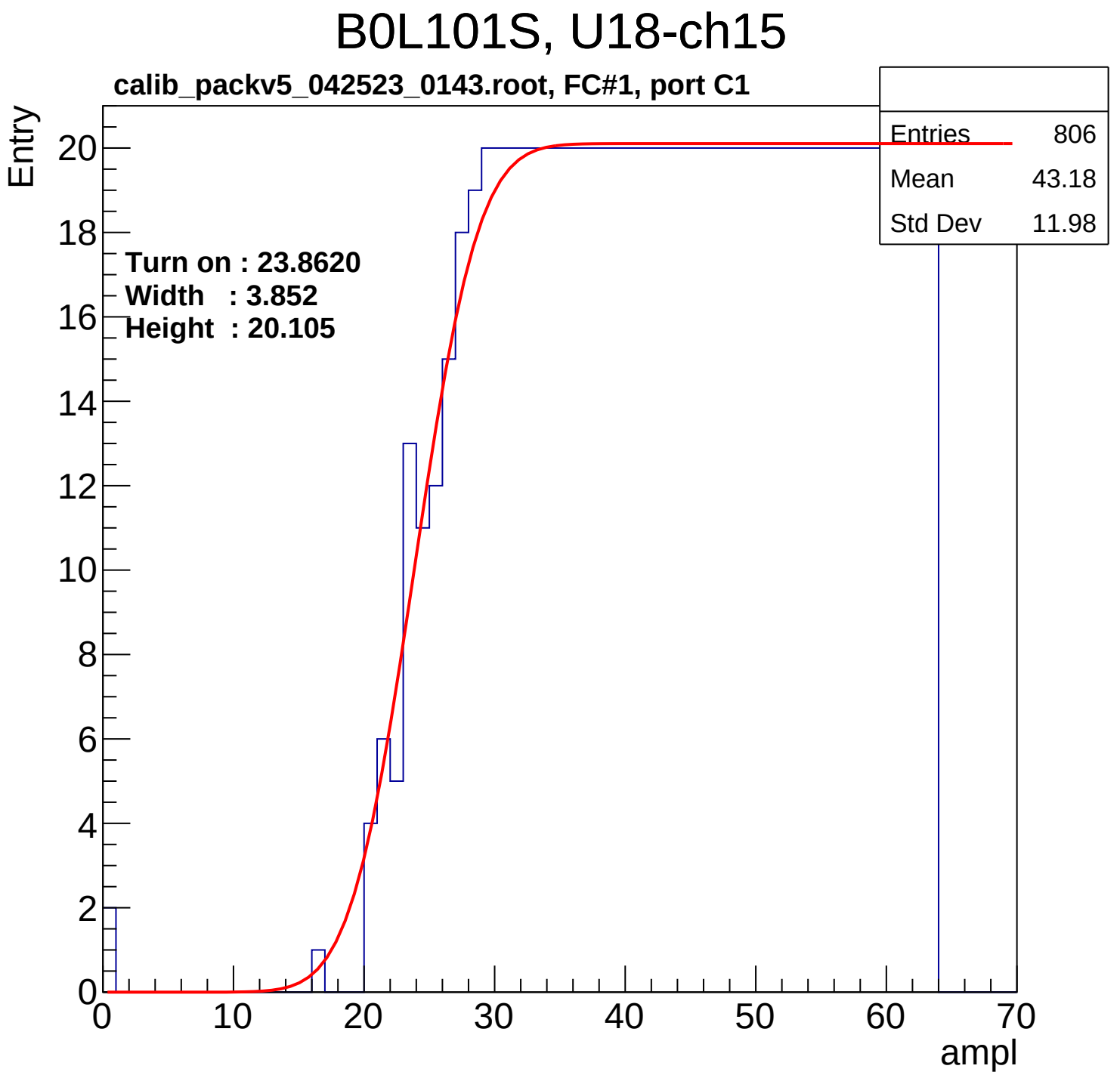
B0L101S, U18-ch15
calib_packv5_042523_0143.root, FC#1, port C1
Entries 806
Mean 43.18
Std Dev 11.98
Turn on : 23.8620
Width : 3.852
Height : 20.105
Entry
ampl
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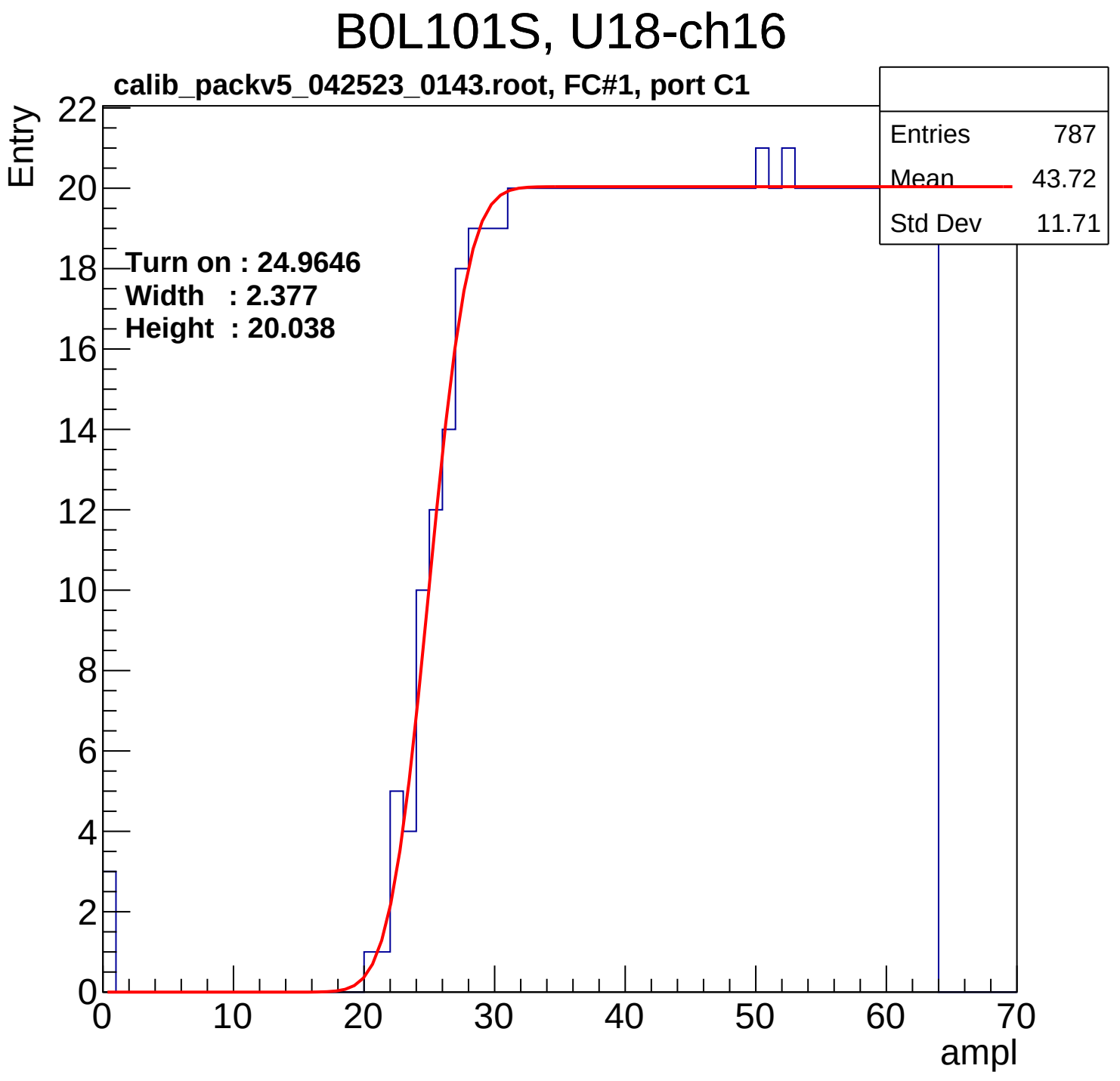
B0L101S, U18-ch16
calib_packv5_042523_0143.root, FC#1, port C1
Entries 787
Mean 43.72
Std Dev 11.71
Turn on : 24.9646
Width : 2.377
Height : 20.038
Entry
ampl
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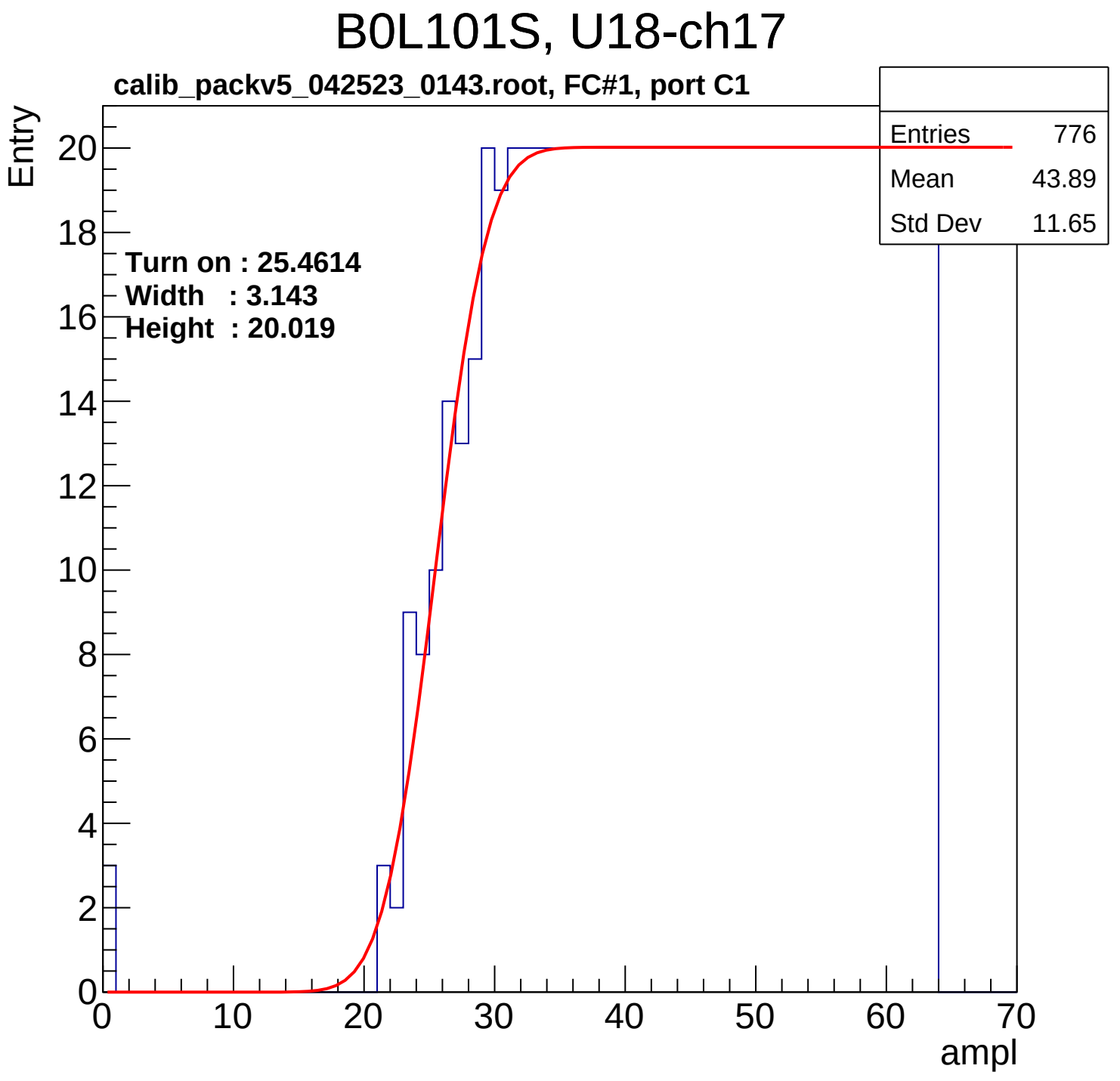
B0L101S, U18-ch17
calib_packv5_042523_0143.root, FC#1, port C1
Entries 776
Mean 43.89
Std Dev 11.65
Turn on : 25.4614
Width : 3.143
Height : 20.019
Entry
ampl
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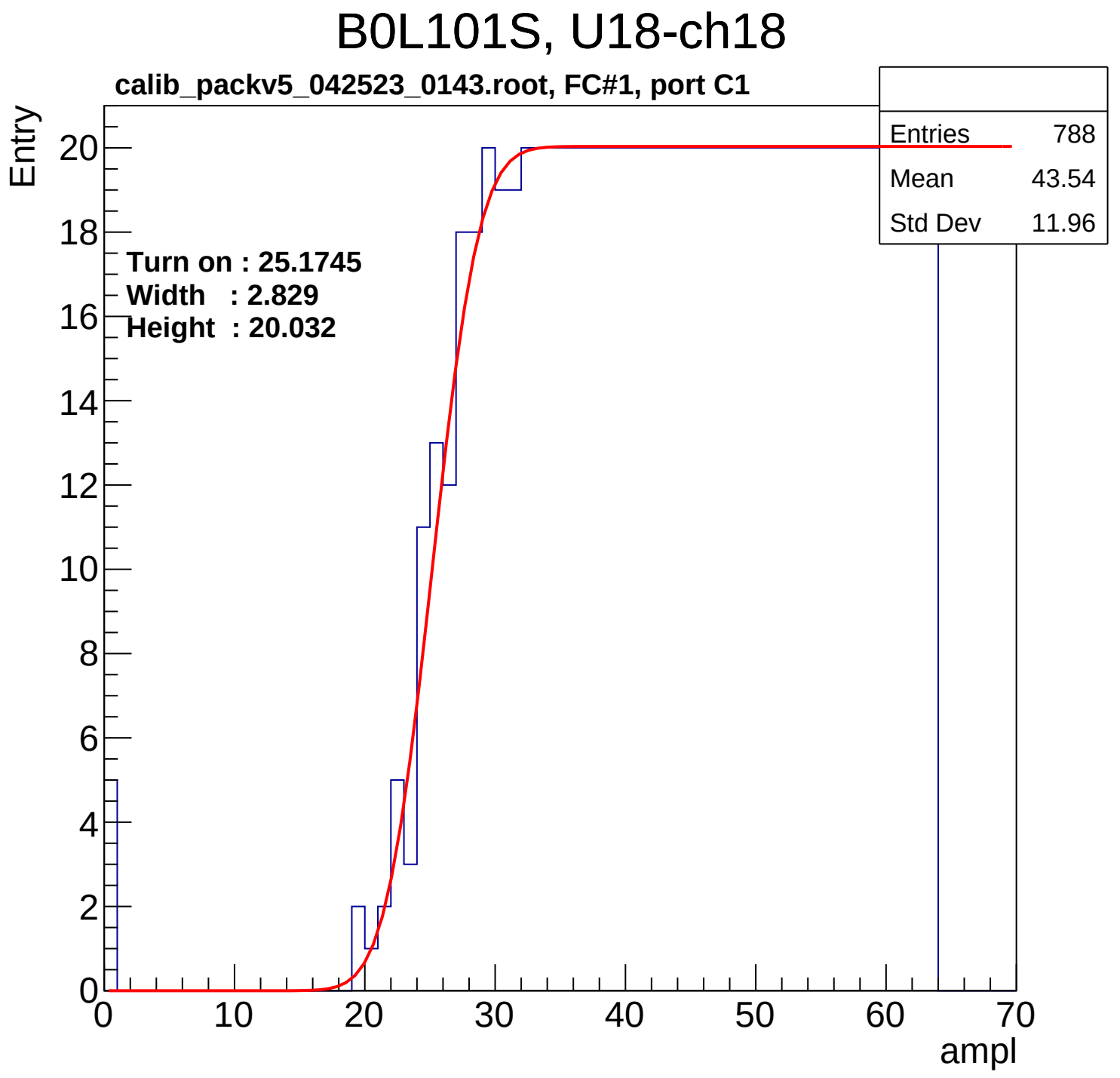
B0L101S, U18-ch18
calib_packv5_042523_0143.root, FC#1, port C1
Entries 788
Mean 43.54
Std Dev 11.96
Turn on : 25.1745
Width : 2.829
Height : 20.032
Entry
ampl
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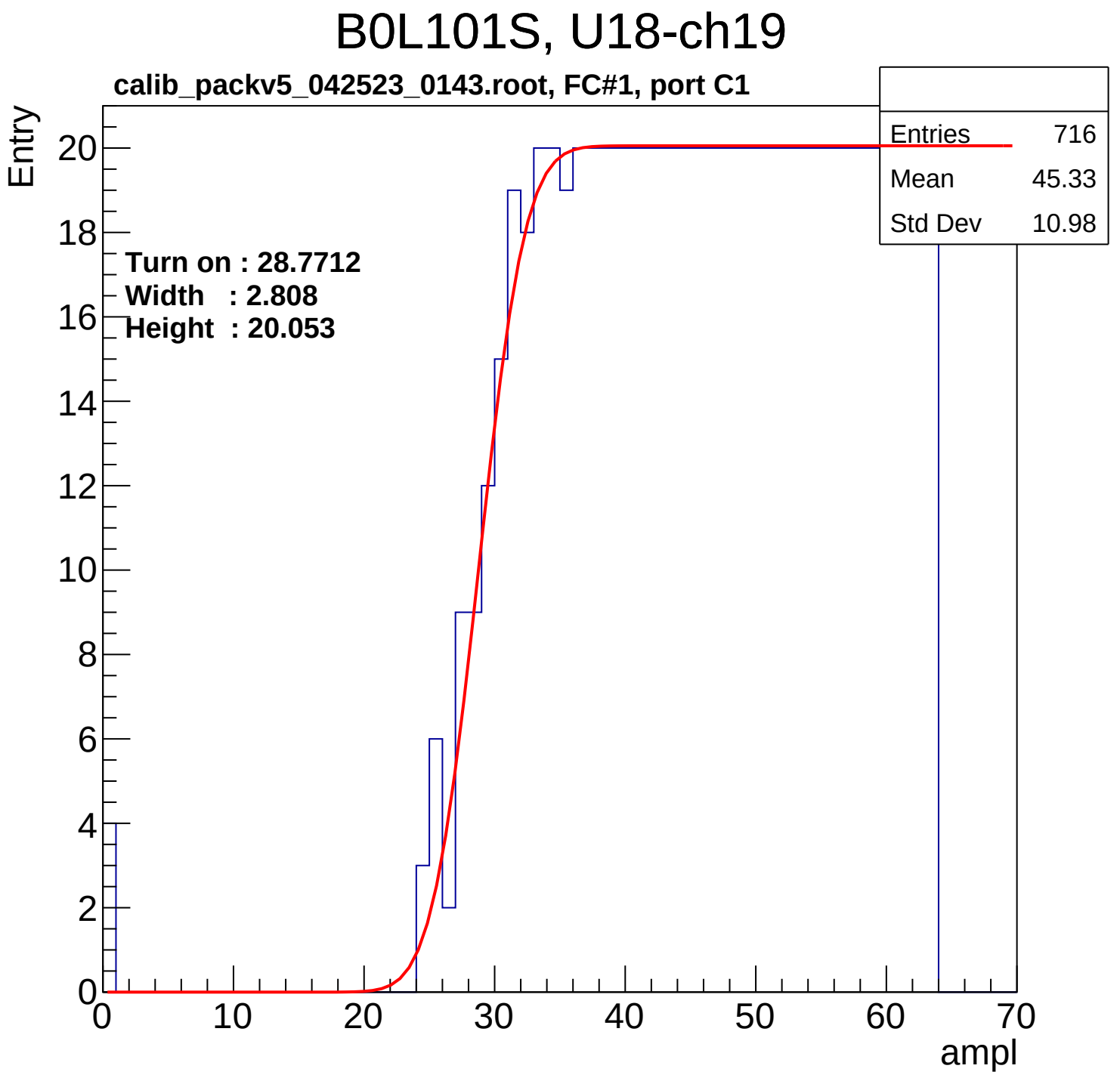
B0L101S, U18-ch19
calib_packv5_042523_0143.root, FC#1, port C1
Entries 716
Mean 45.33
Std Dev 10.98
Turn on : 28.7712
Width : 2.808
Height : 20.053
Entry
ampl
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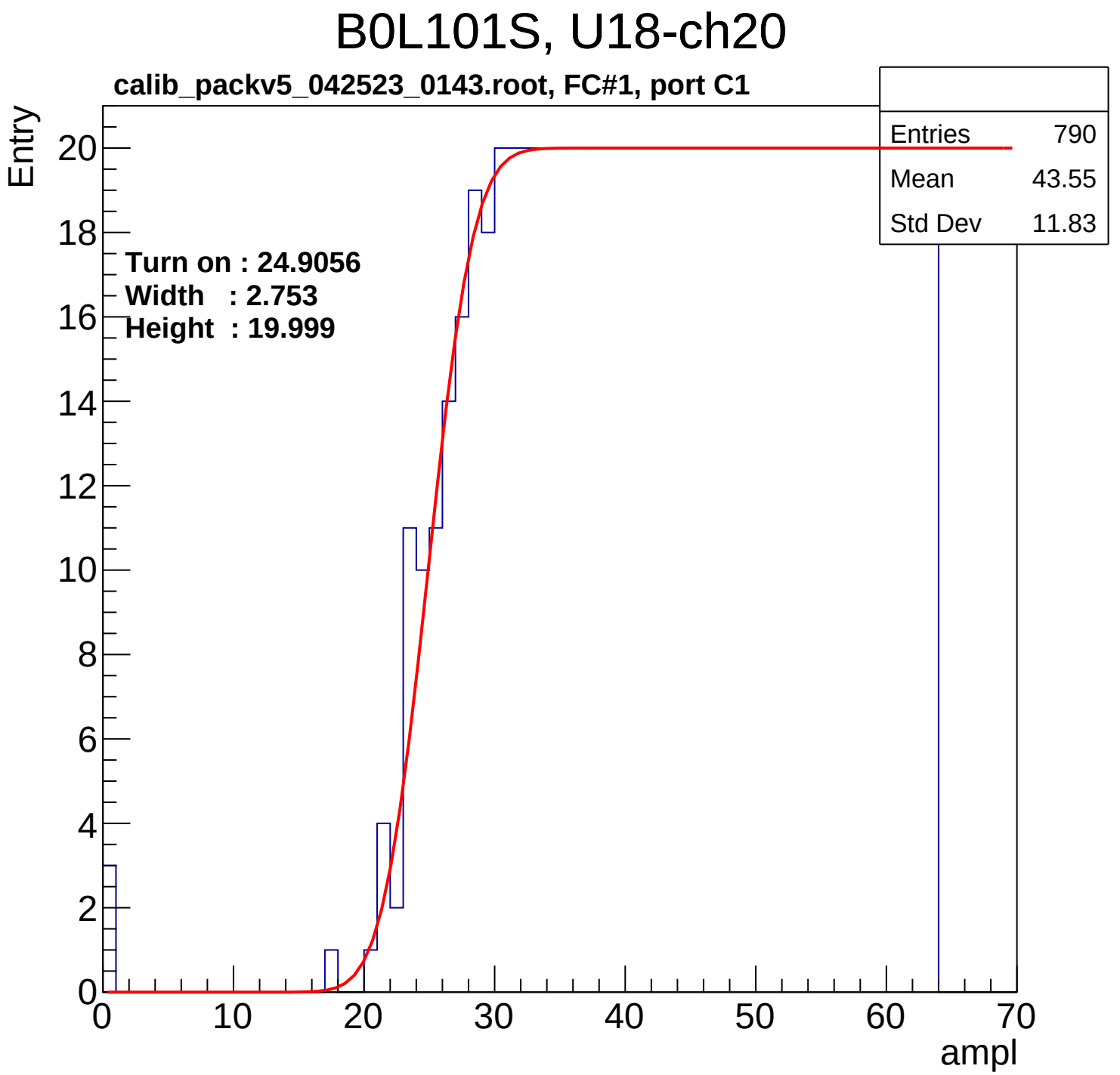
B0L101S, U18-ch20
calib_packv5_042523_0143.root, FC#1, port C1
Entries 790
Mean 43.55
Std Dev 11.83
Turn on : 24.9056
Width : 2.753
Height : 19.999
Entry
ampl
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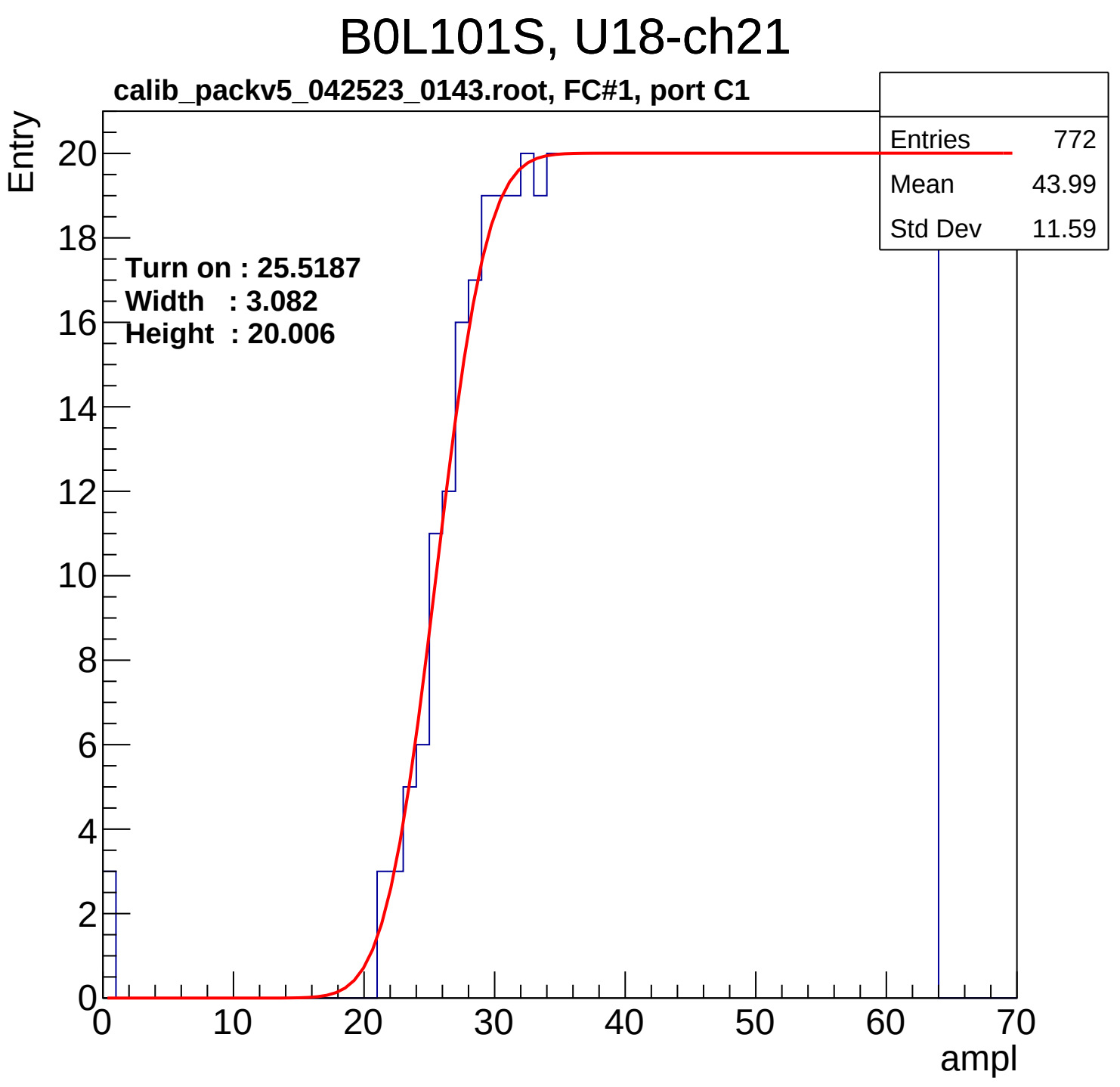
B0L101S, U18-ch21
calib_packv5_042523_0143.root, FC#1, port C1
Entries 772
Mean 43.99
Std Dev 11.59
Turn on : 25.5187
Width : 3.082
Height : 20.006
Entry
ampl
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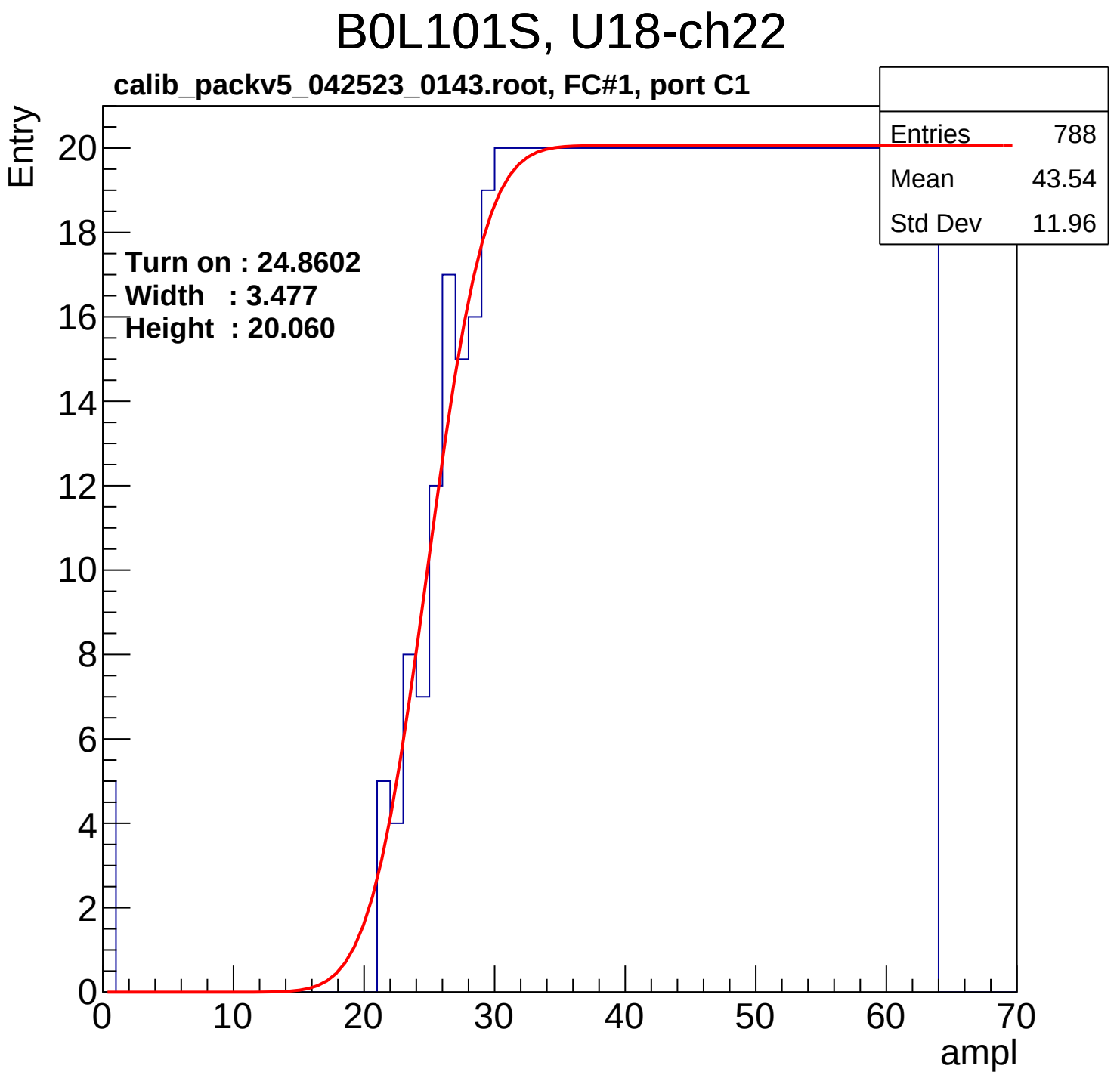
B0L101S, U18-ch22
calib_packv5_042523_0143.root, FC#1, port C1
Entries 788
Mean 43.54
Std Dev 11.96
Turn on : 24.8602
Width : 3.477
Height : 20.060
Entry
ampl
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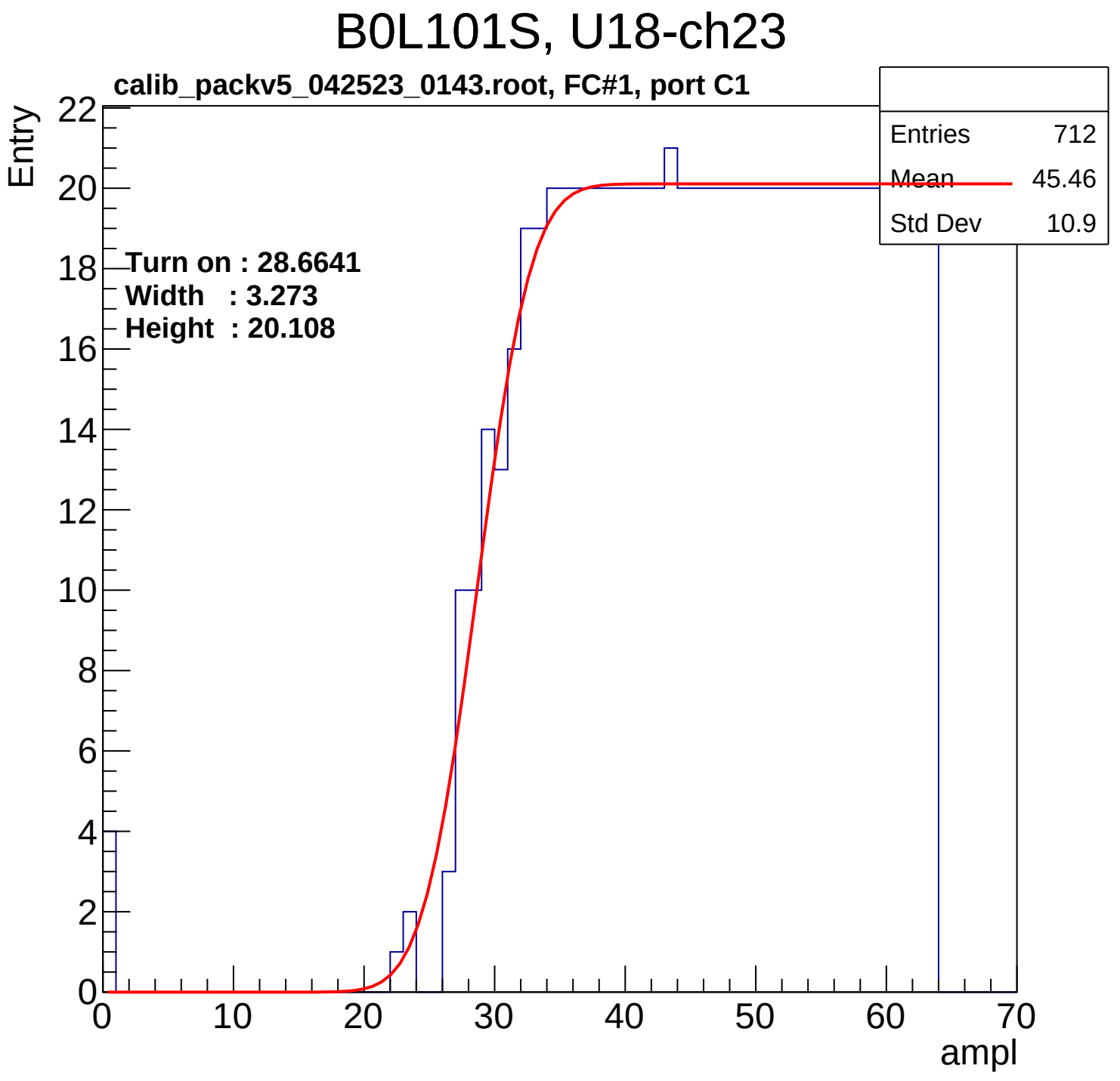
B0L101S, U18-ch23
calib_packv5_042523_0143.root, FC#1, port C1
Entries 712
Mean 45.46
Std Dev 10.9
Turn on : 28.6641
Width : 3.273
Height : 20.108
Entry
ampl
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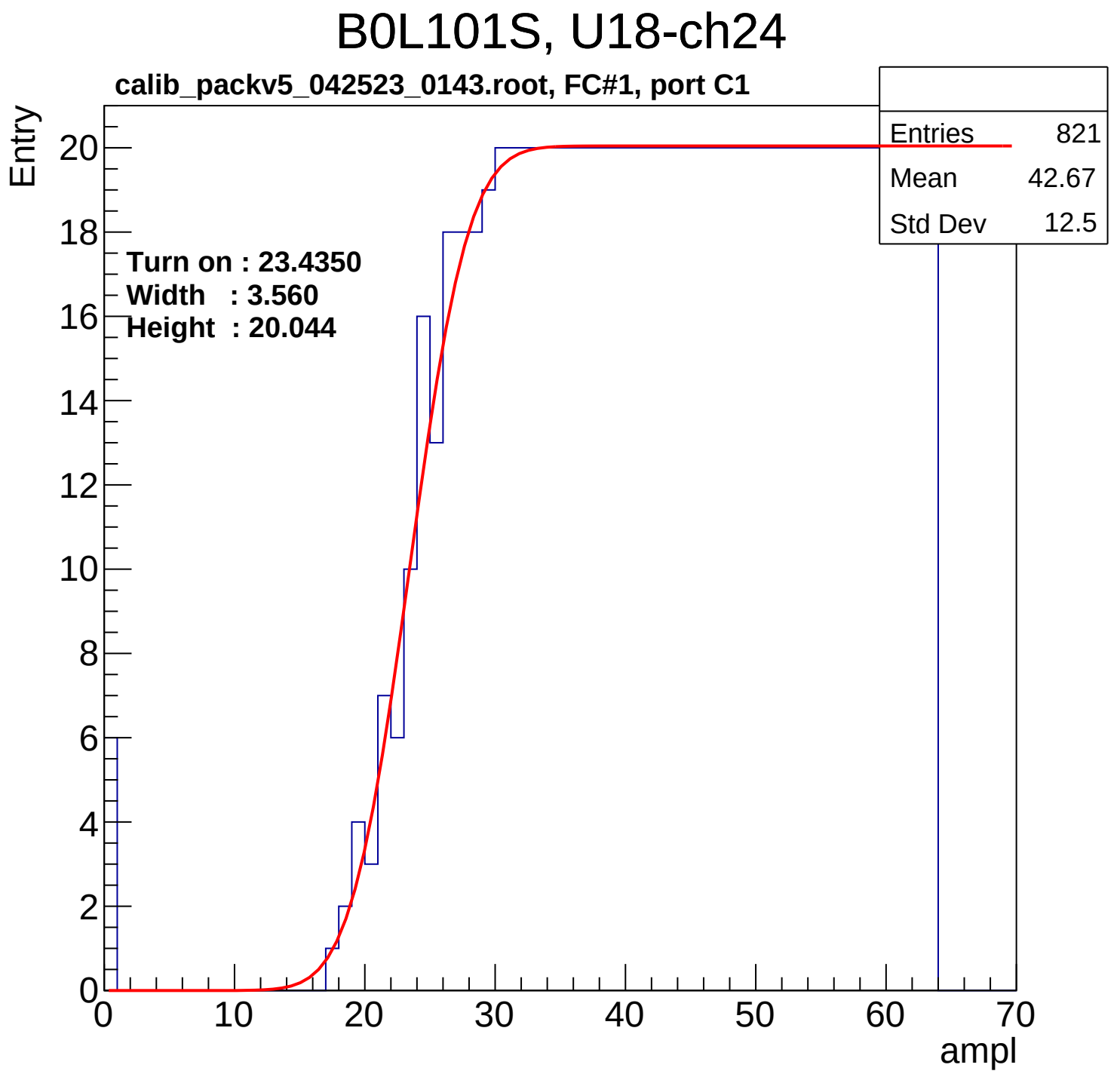
B0L101S, U18-ch24
calib_packv5_042523_0143.root, FC#1, port C1
Entries 821
Mean 42.67
Std Dev 12.5
Turn on : 23.4350
Width : 3.560
Height : 20.044
Entry
ampl
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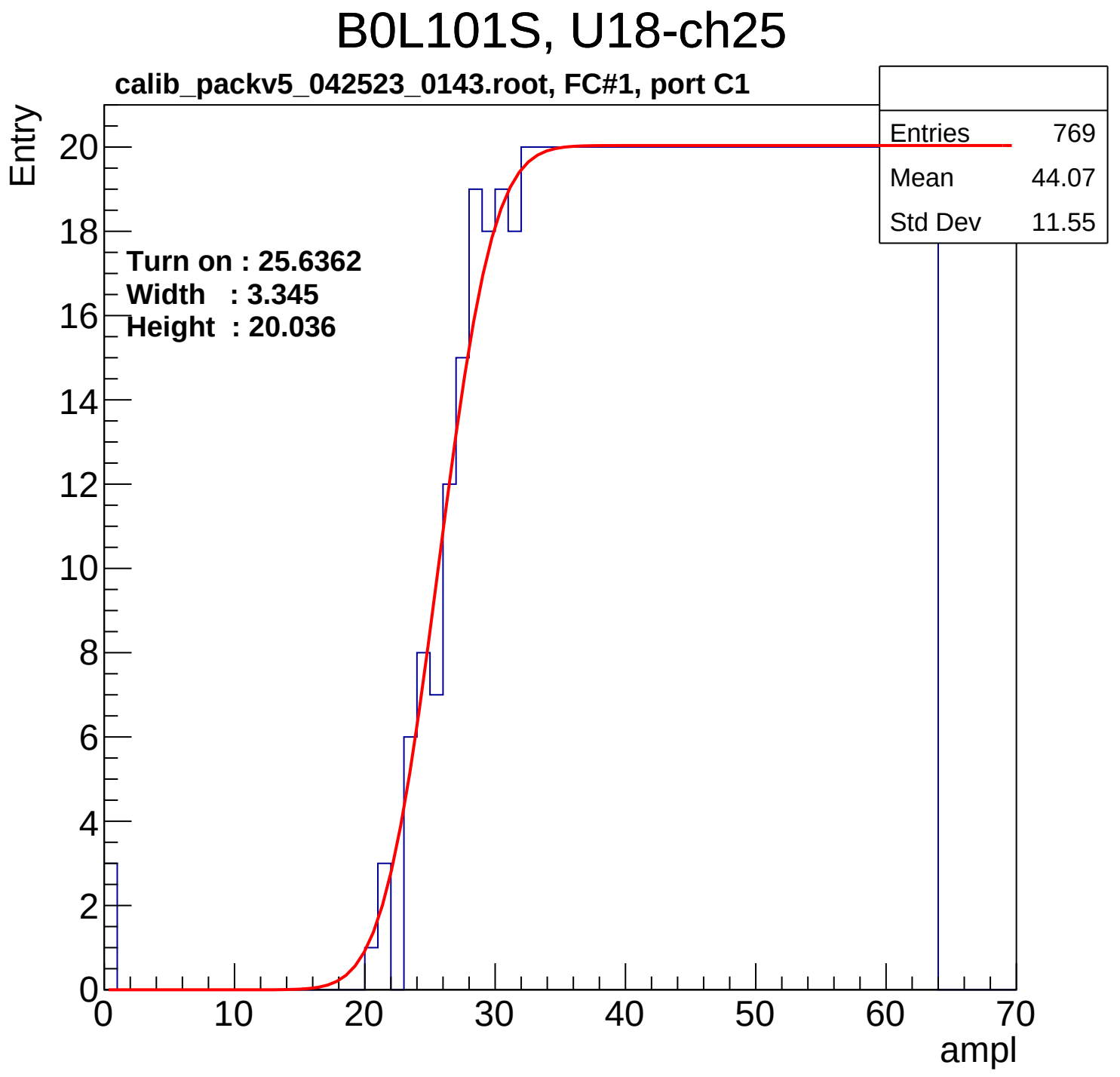
B0L101S, U18-ch25
calib_packv5_042523_0143.root, FC#1, port C1
Entries 769
Mean 44.07
Std Dev 11.55
Turn on : 25.6362
Width : 3.345
Height : 20.036
Entry
ampl
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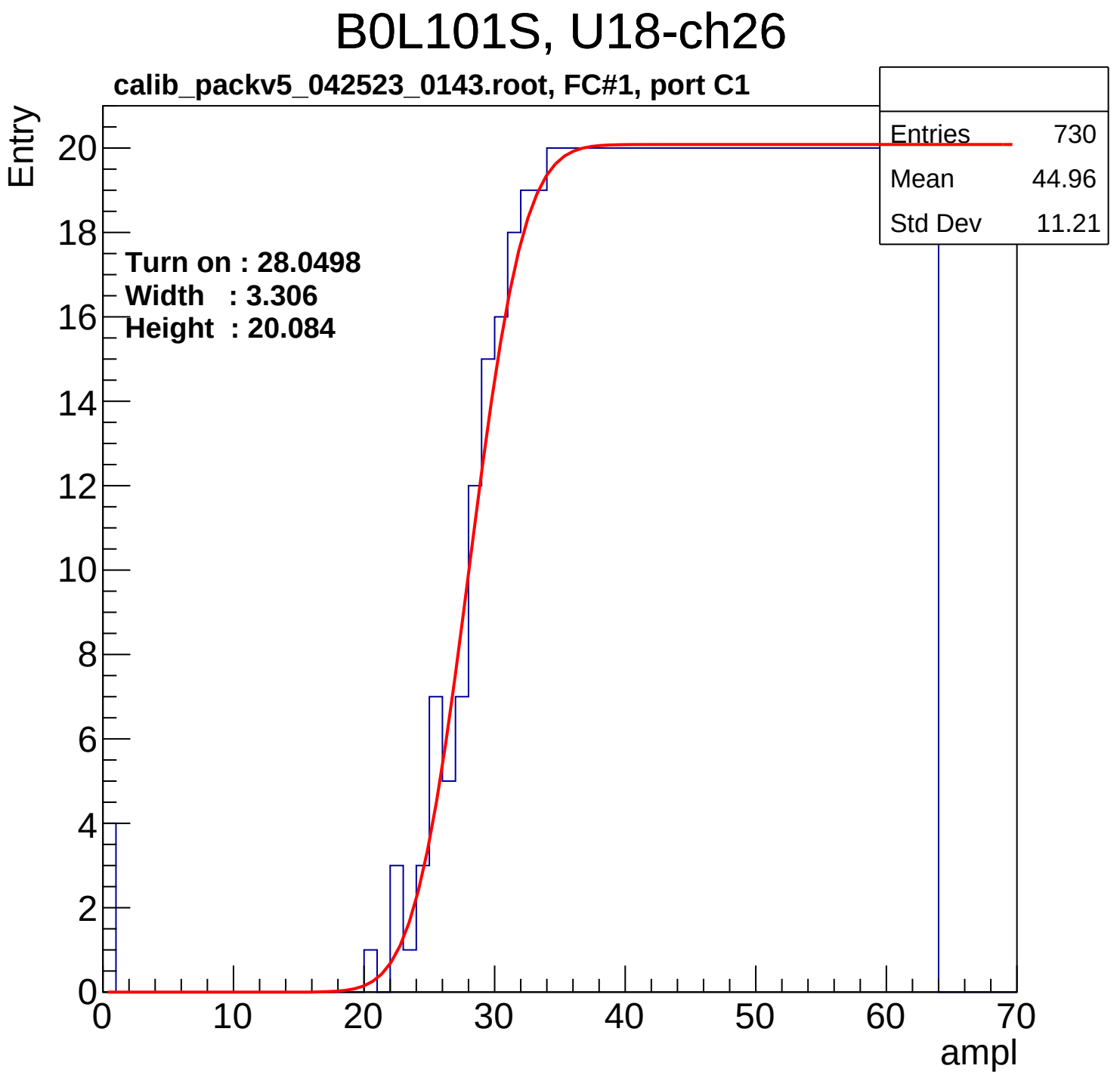
B0L101S, U18-ch26
calib_packv5_042523_0143.root, FC#1, port C1
Entries 730
Mean 44.96
Std Dev 11.21
Turn on : 28.0498
Width : 3.306
Height : 20.084
Entry
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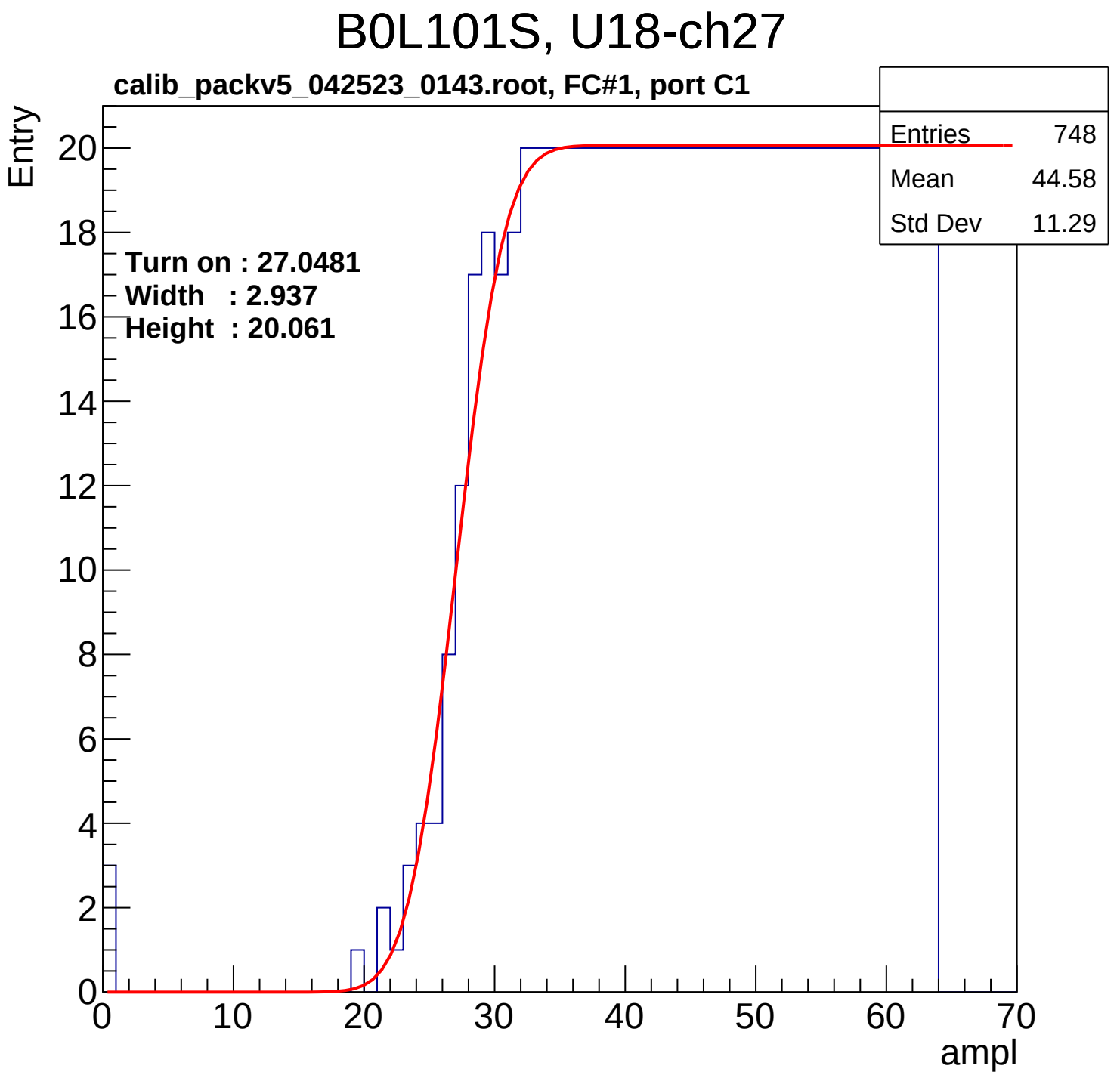
B0L101S, U18-ch27
calib_packv5_042523_0143.root, FC#1, port C1
Entries 748
Mean 44.58
Std Dev 11.29
Turn on : 27.0481
Width : 2.937
Height : 20.061
Entry
ampl
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2
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12
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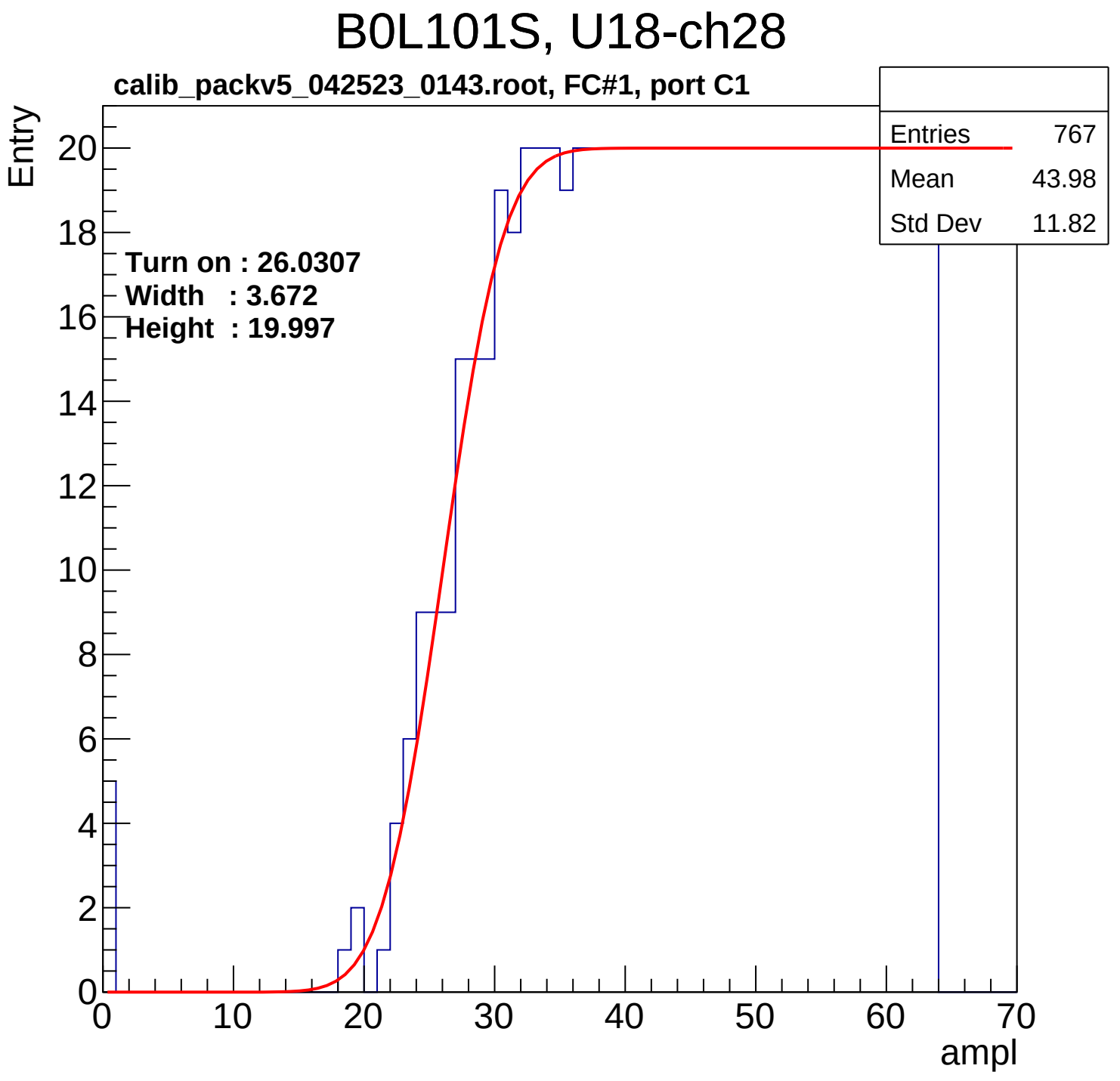
B0L101S, U18-ch28
calib_packv5_042523_0143.root, FC#1, port C1
Entries 767
Mean 43.98
Std Dev 11.82
Turn on : 26.0307
Width : 3.672
Height : 19.997
Entry
ampl
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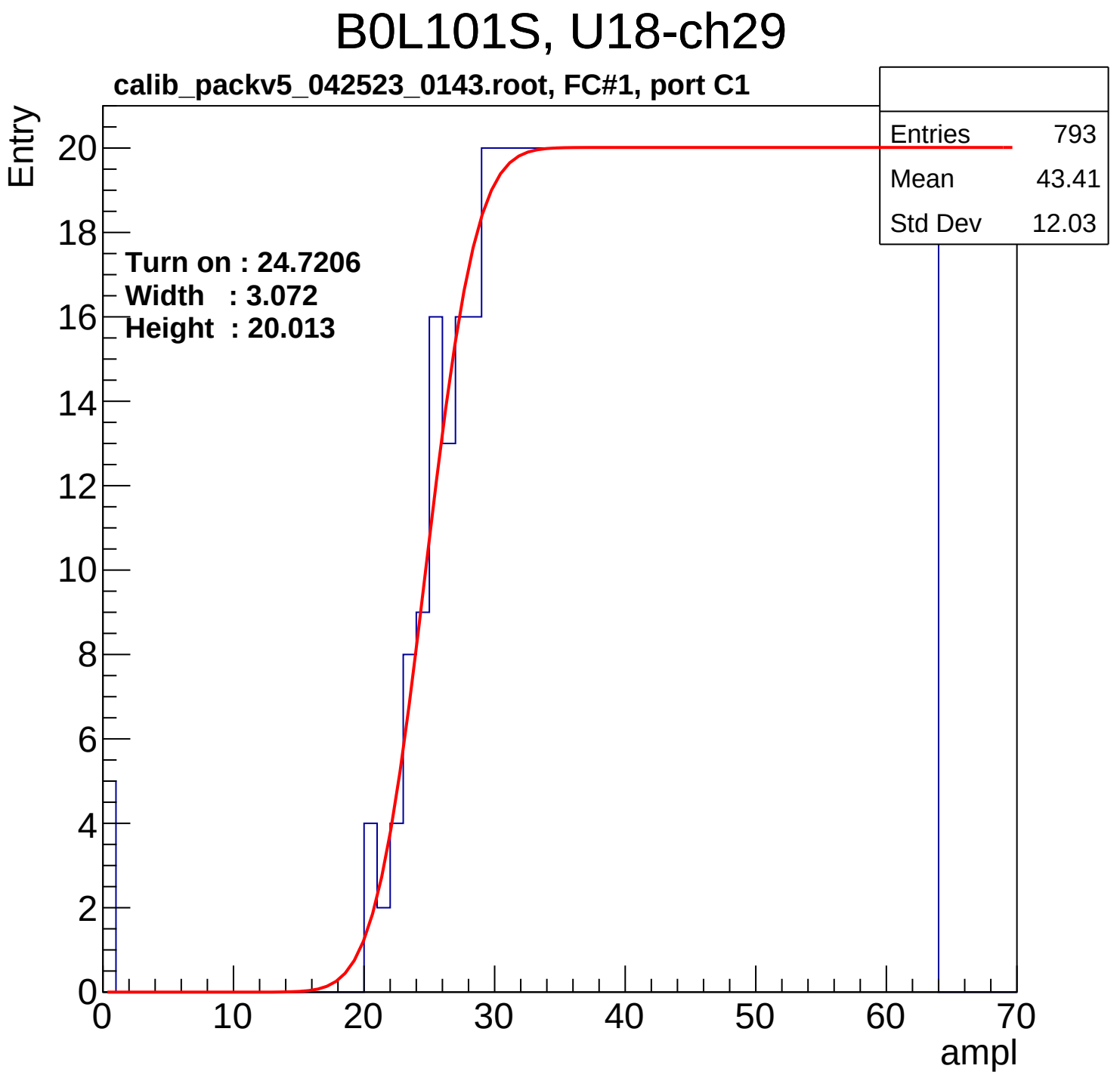
B0L101S, U18-ch29
calib_packv5_042523_0143.root, FC#1, port C1
Entries 793
Mean 43.41
Std Dev 12.03
Turn on : 24.7206
Width : 3.072
Height : 20.013
Entry
ampl
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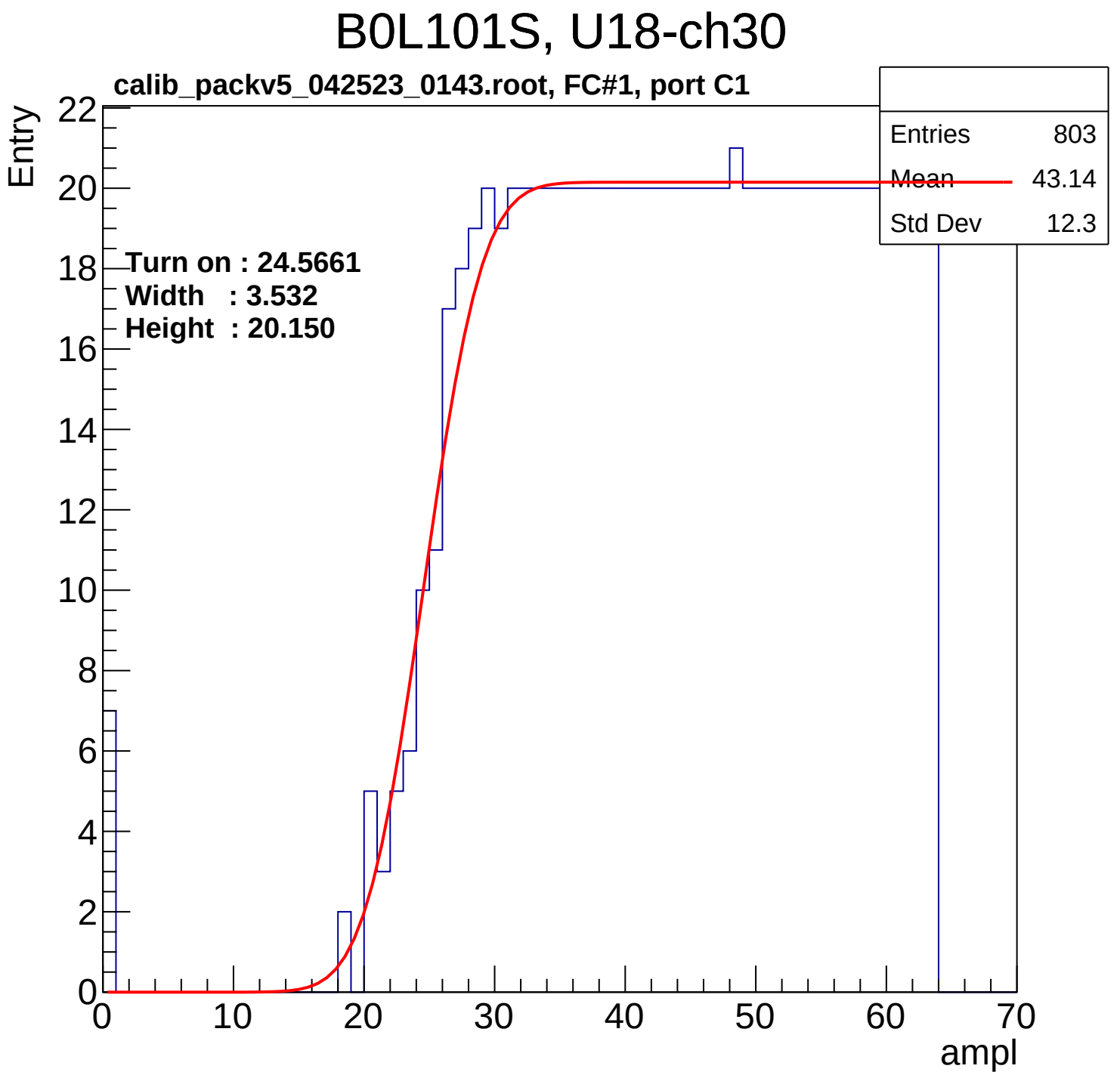
B0L101S, U18-ch30
calib_packv5_042523_0143.root, FC#1, port C1
Entries 803
Mean 43.14
Std Dev 12.3
Turn on : 24.5661
Width : 3.532
Height : 20.150
Entry
ampl
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8
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16
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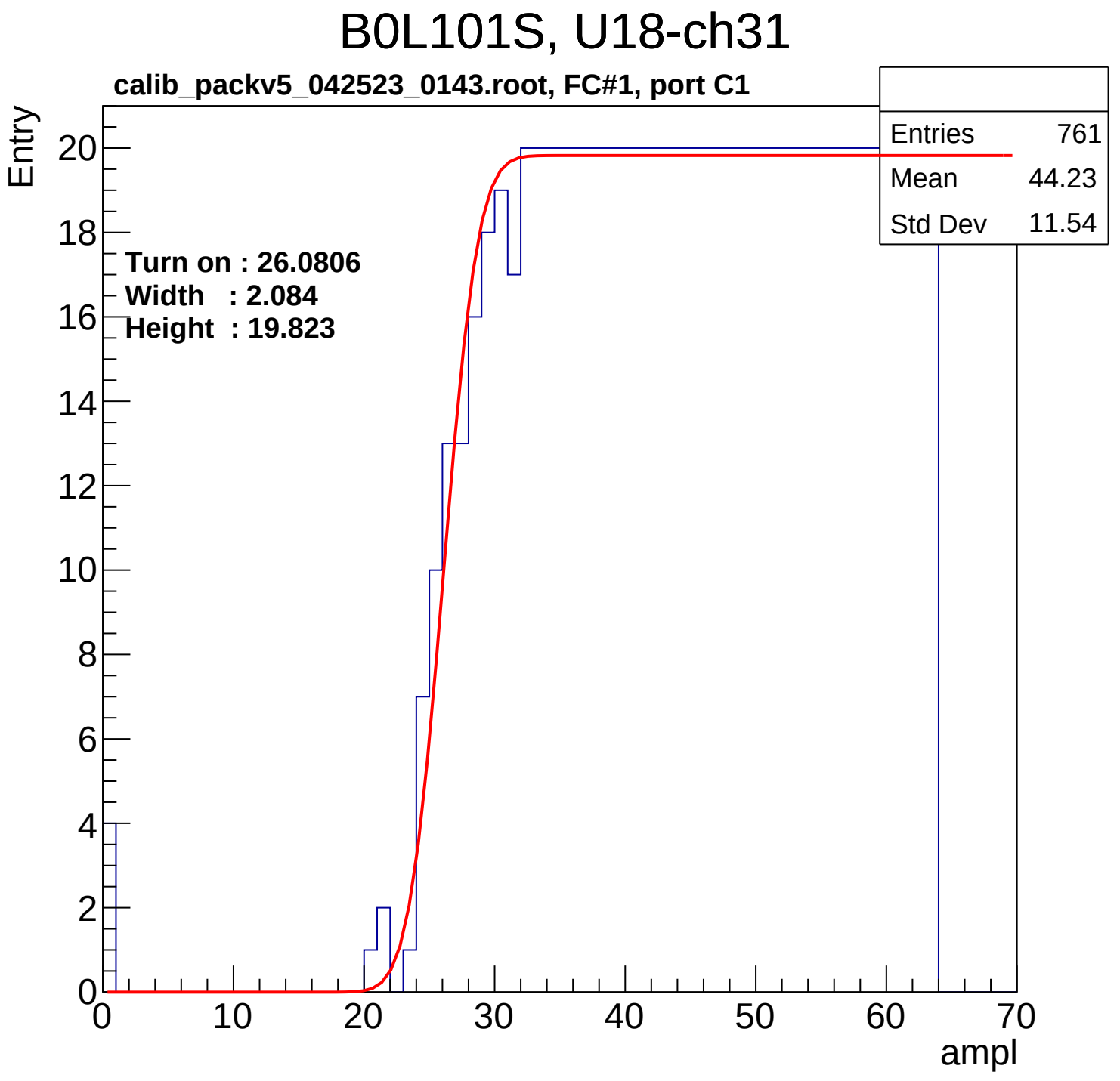
B0L101S, U18-ch31
calib_packv5_042523_0143.root, FC#1, port C1
Entries 761
Mean 44.23
Std Dev 11.54
Turn on : 26.0806
Width : 2.084
Height : 19.823
Entry
ampl
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6
8
10
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16
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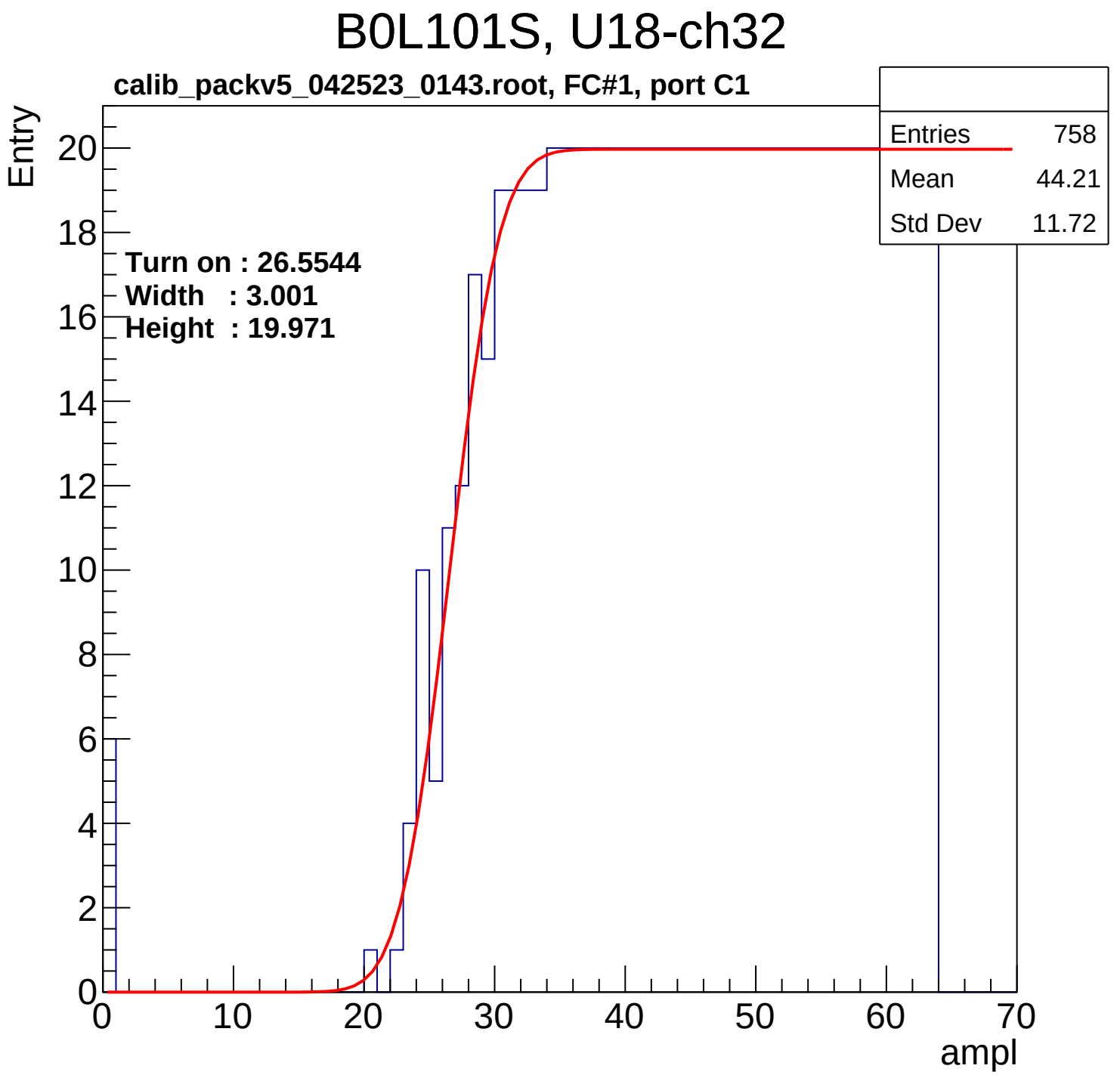
B0L101S, U18-ch32
calib_packv5_042523_0143.root, FC#1, port C1
Entries 758
Mean 44.21
Std Dev 11.72
Turn on : 26.5544
Width : 3.001
Height : 19.971
Entry
ampl
0
2
4
6
8
10
12
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16
18
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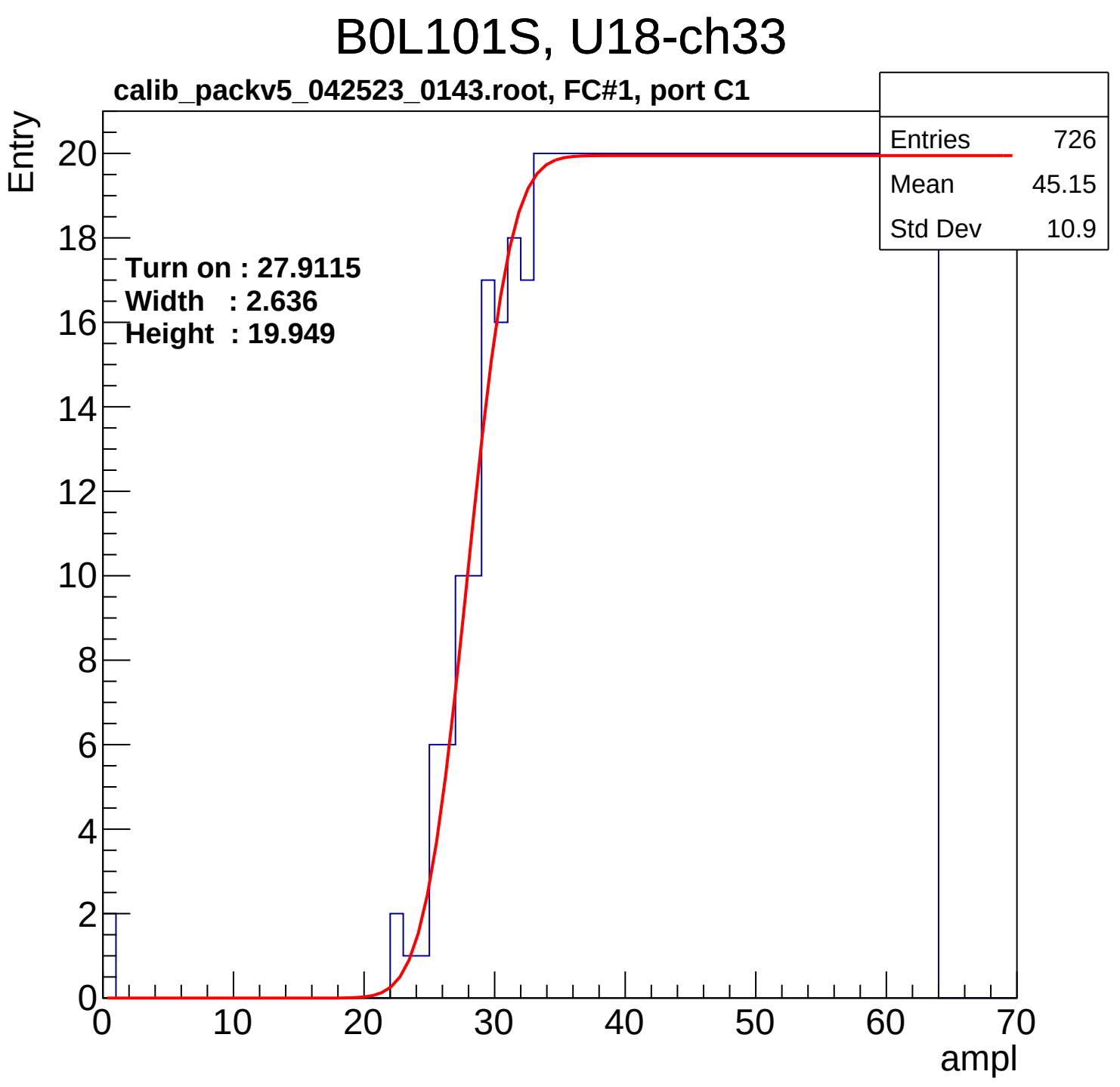
B0L101S, U18-ch33
calib_packv5_042523_0143.root, FC#1, port C1
Entries 726
Mean 45.15
Std Dev 10.9
Turn on : 27.9115
Width : 2.636
Height : 19.949
Entry
ampl
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6
8
10
12
14
16
18
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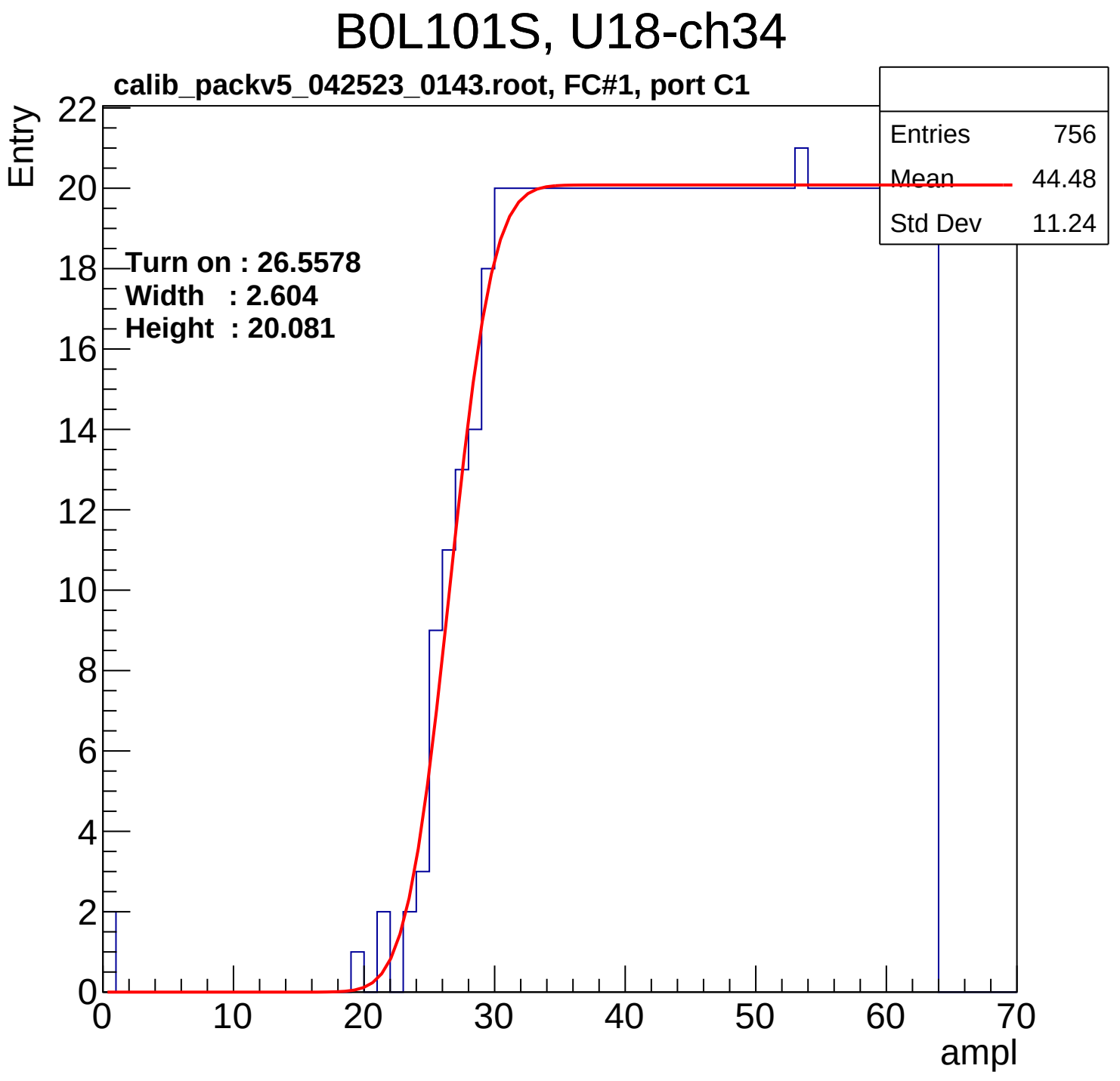
B0L101S, U18-ch34
calib_packv5_042523_0143.root, FC#1, port C1
Entries 756
Mean 44.48
Std Dev 11.24
Turn on : 26.5578
Width : 2.604
Height : 20.081
Entry
ampl
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8
10
12
14
16
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20
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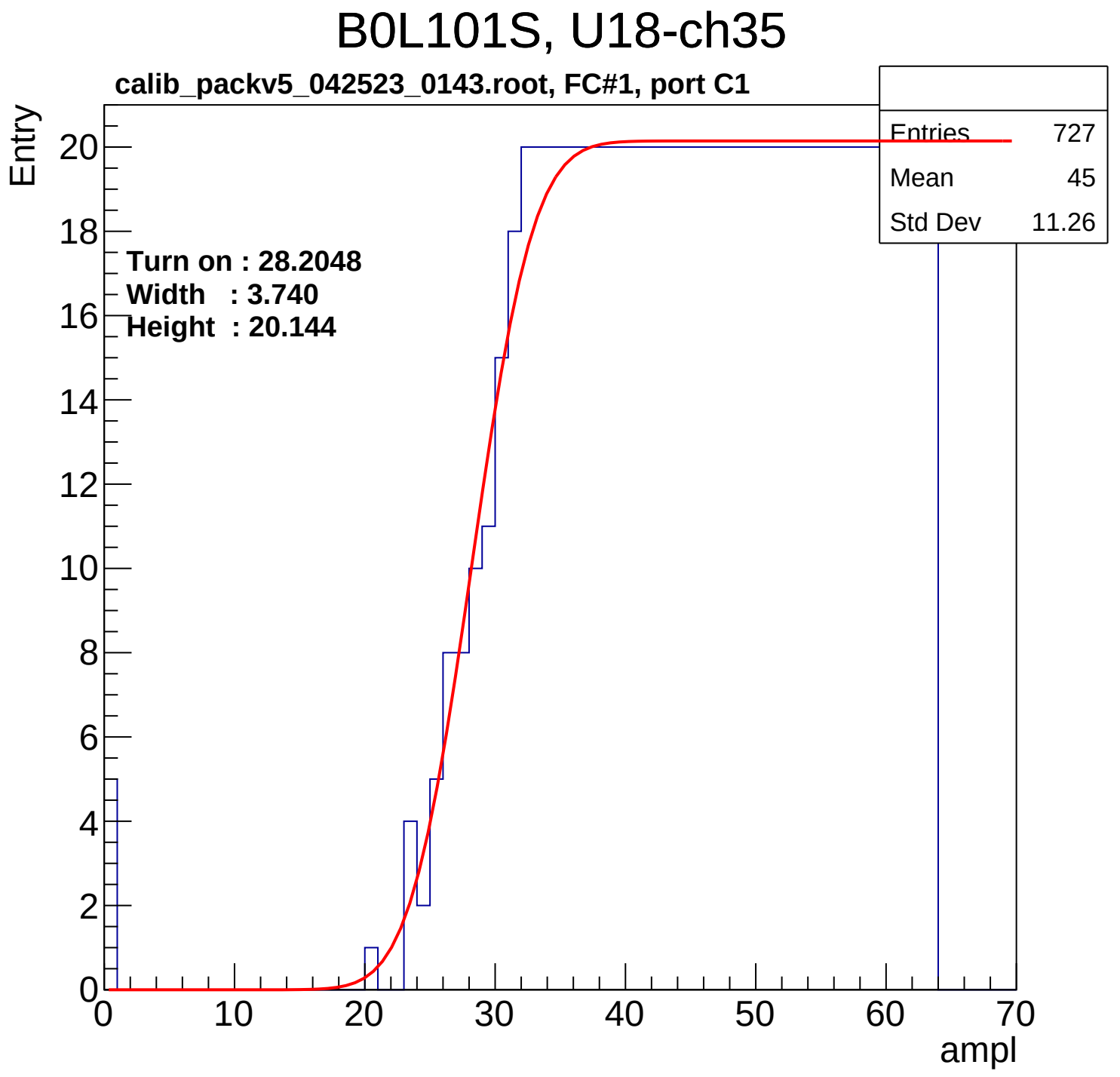
B0L101S, U18-ch35
calib_packv5_042523_0143.root, FC#1, port C1
Entries 727
Mean 45
Std Dev 11.26
Turn on : 28.2048
Width : 3.740
Height : 20.144
Entry
ampl
0
2
4
6
8
10
12
14
16
18
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0
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20
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60
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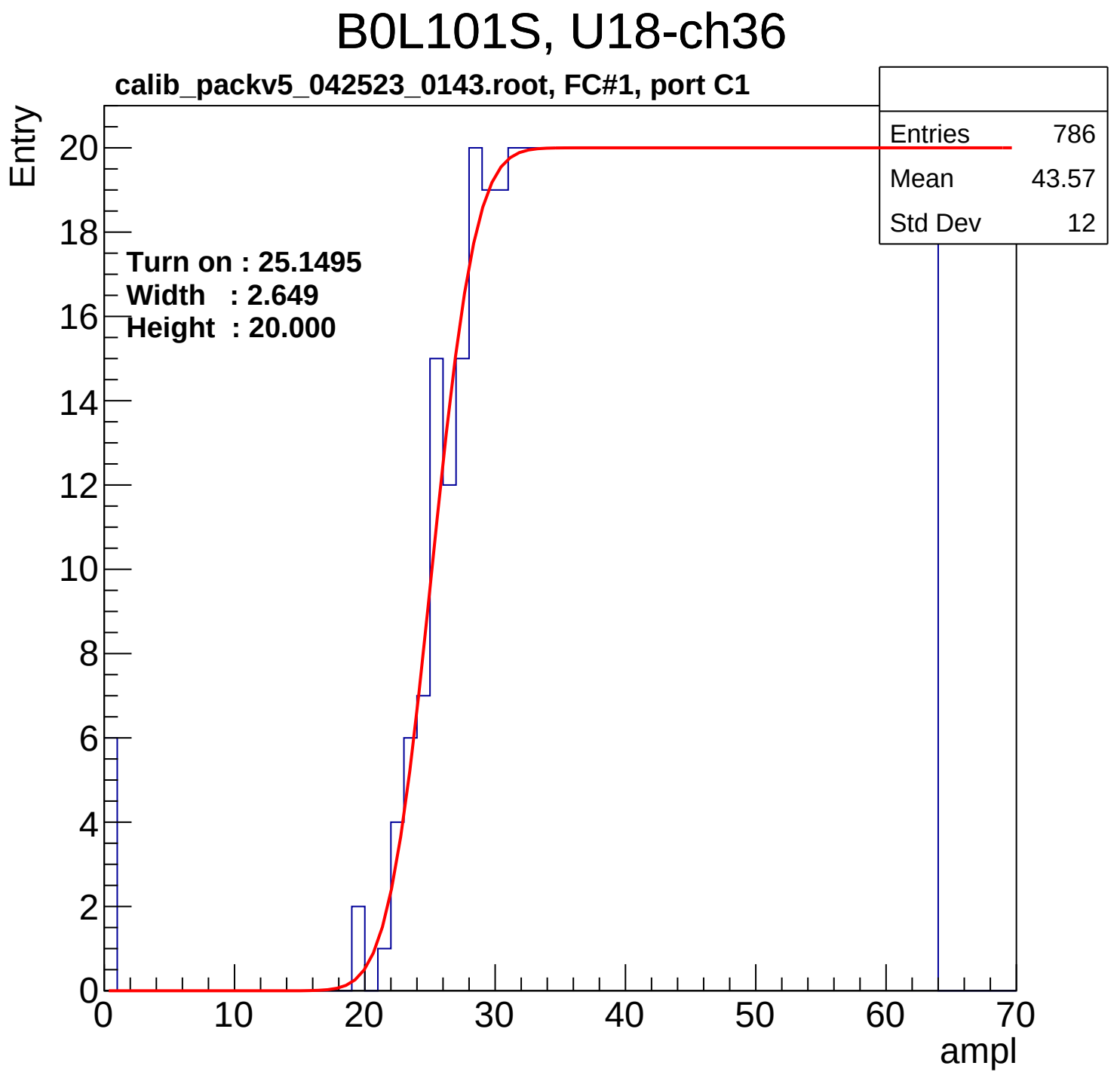
B0L101S, U18-ch36
calib_packv5_042523_0143.root, FC#1, port C1
Entries 786
Mean 43.57
Std Dev 12
Turn on : 25.1495
Width : 2.649
Height : 20.000
Entry
ampl
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6
8
10
12
14
16
18
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60
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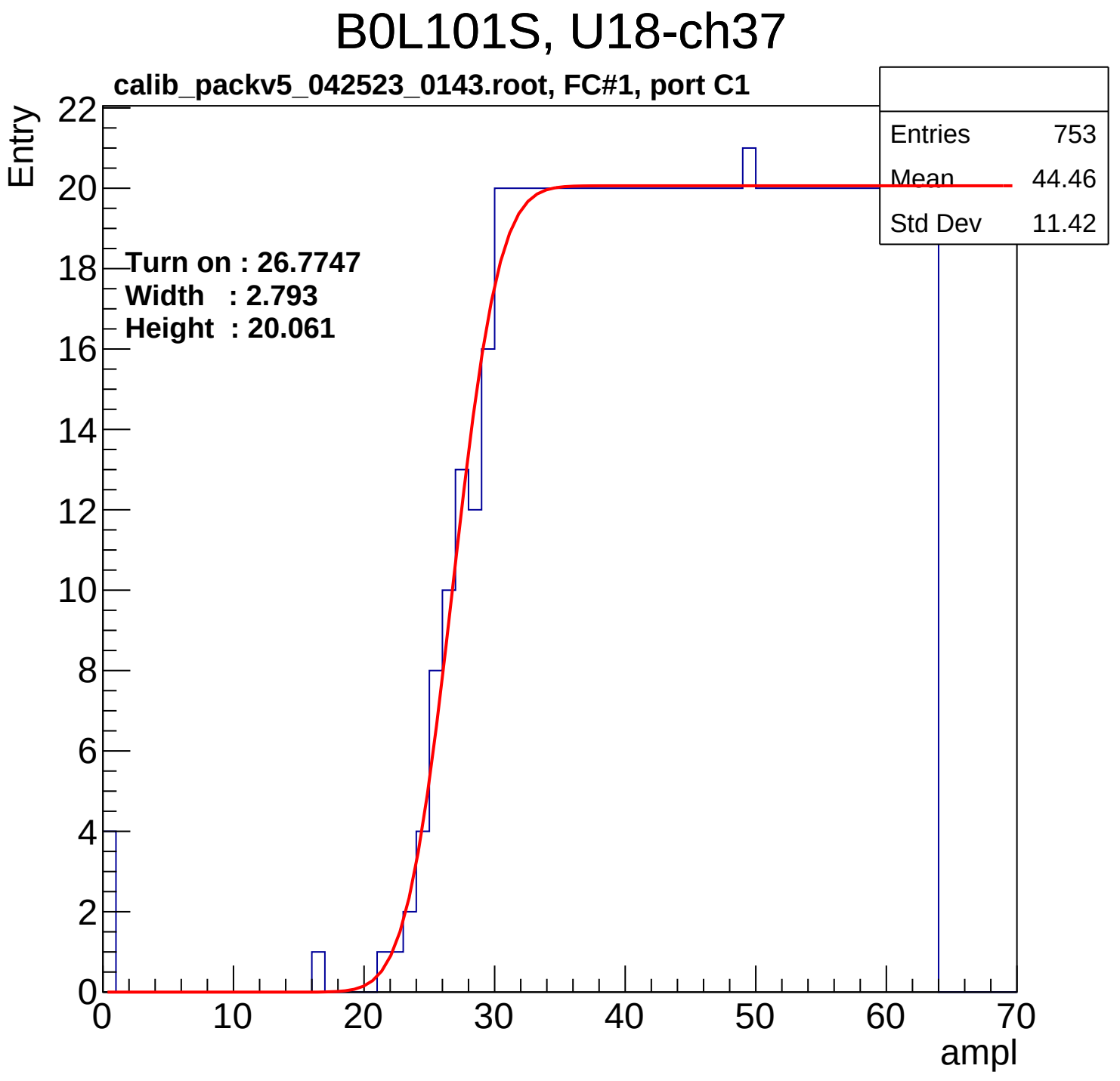
B0L101S, U18-ch37
calib_packv5_042523_0143.root, FC#1, port C1
Entries 753
Mean 44.46
Std Dev 11.42
Turn on : 26.7747
Width : 2.793
Height : 20.061
Entry
ampl
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2
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6
8
10
12
14
16
18
20
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0
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20
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40
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60
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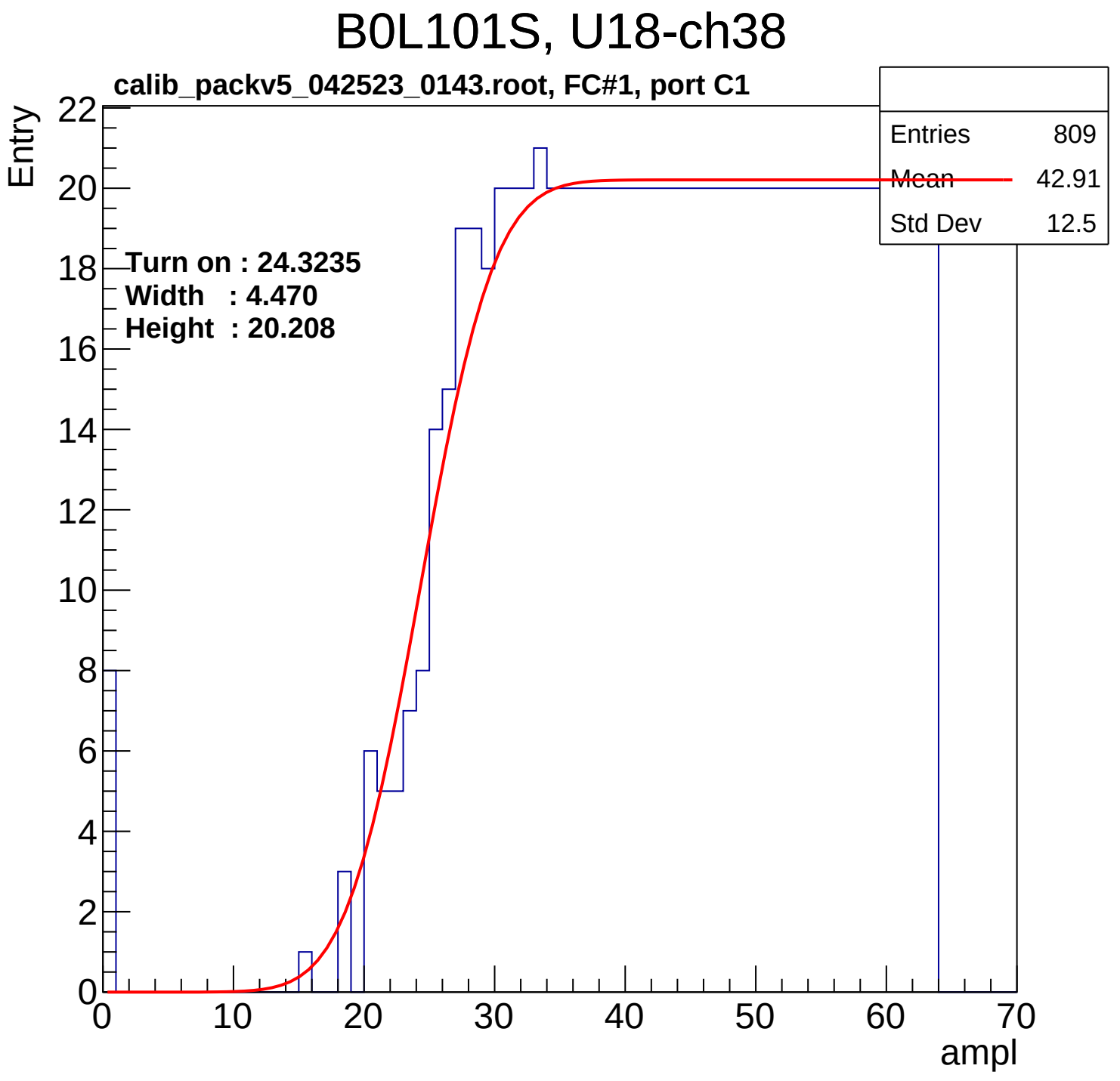
B0L101S, U18-ch38
calib_packv5_042523_0143.root, FC#1, port C1
Entries 809
Mean 42.91
Std Dev 12.5
Turn on : 24.3235
Width : 4.470
Height : 20.208
Entry
ampl
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8
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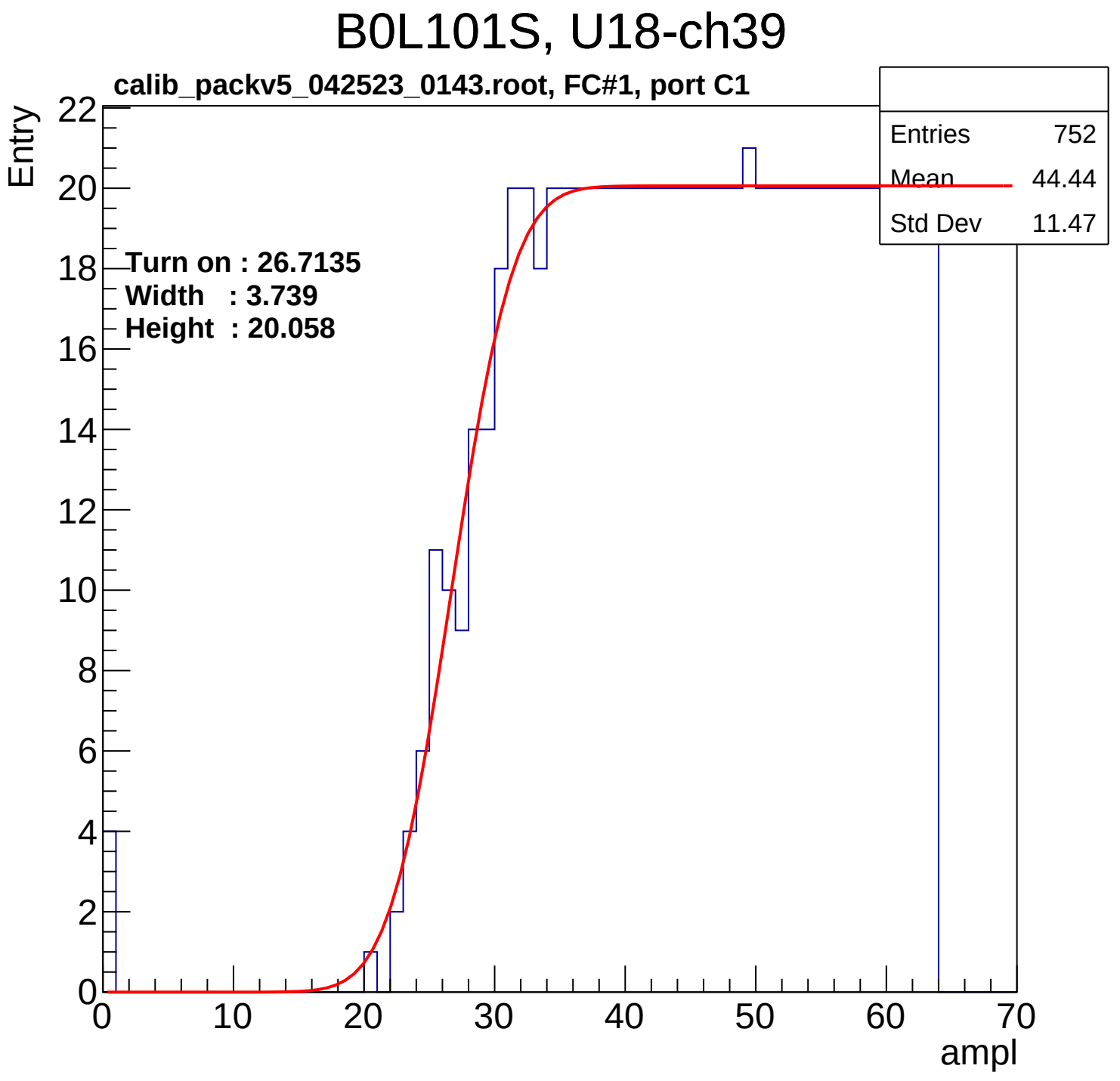
B0L101S, U18-ch39
calib_packv5_042523_0143.root, FC#1, port C1
Entries 752
Mean 44.44
Std Dev 11.47
Turn on : 26.7135
Width : 3.739
Height : 20.058
Entry
ampl
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6
8
10
12
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16
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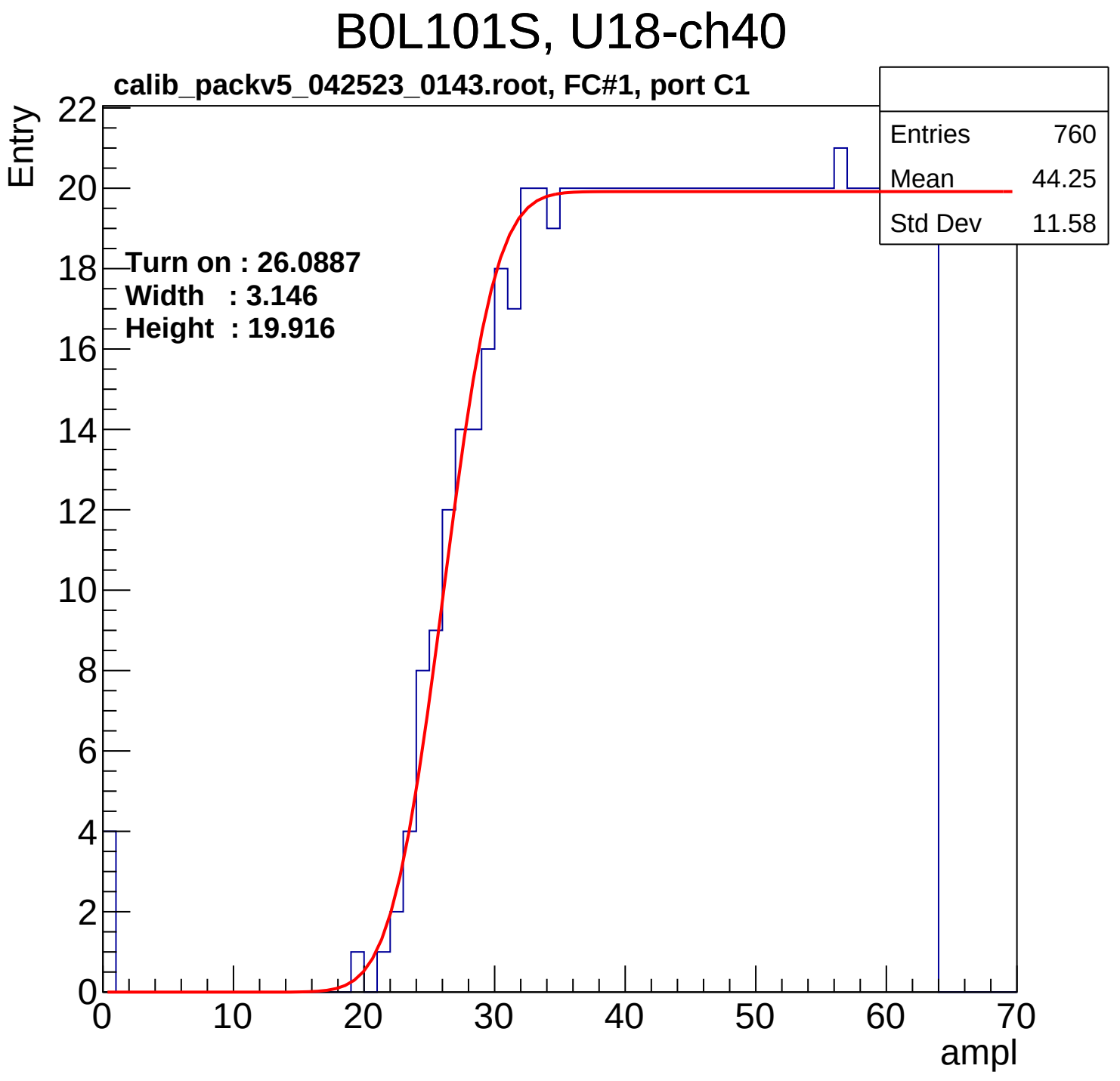
B0L101S, U18-ch40
calib_packv5_042523_0143.root, FC#1, port C1
Entries 760
Mean 44.25
Std Dev 11.58
Turn on : 26.0887
Width : 3.146
Height : 19.916
Entry
ampl
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8
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16
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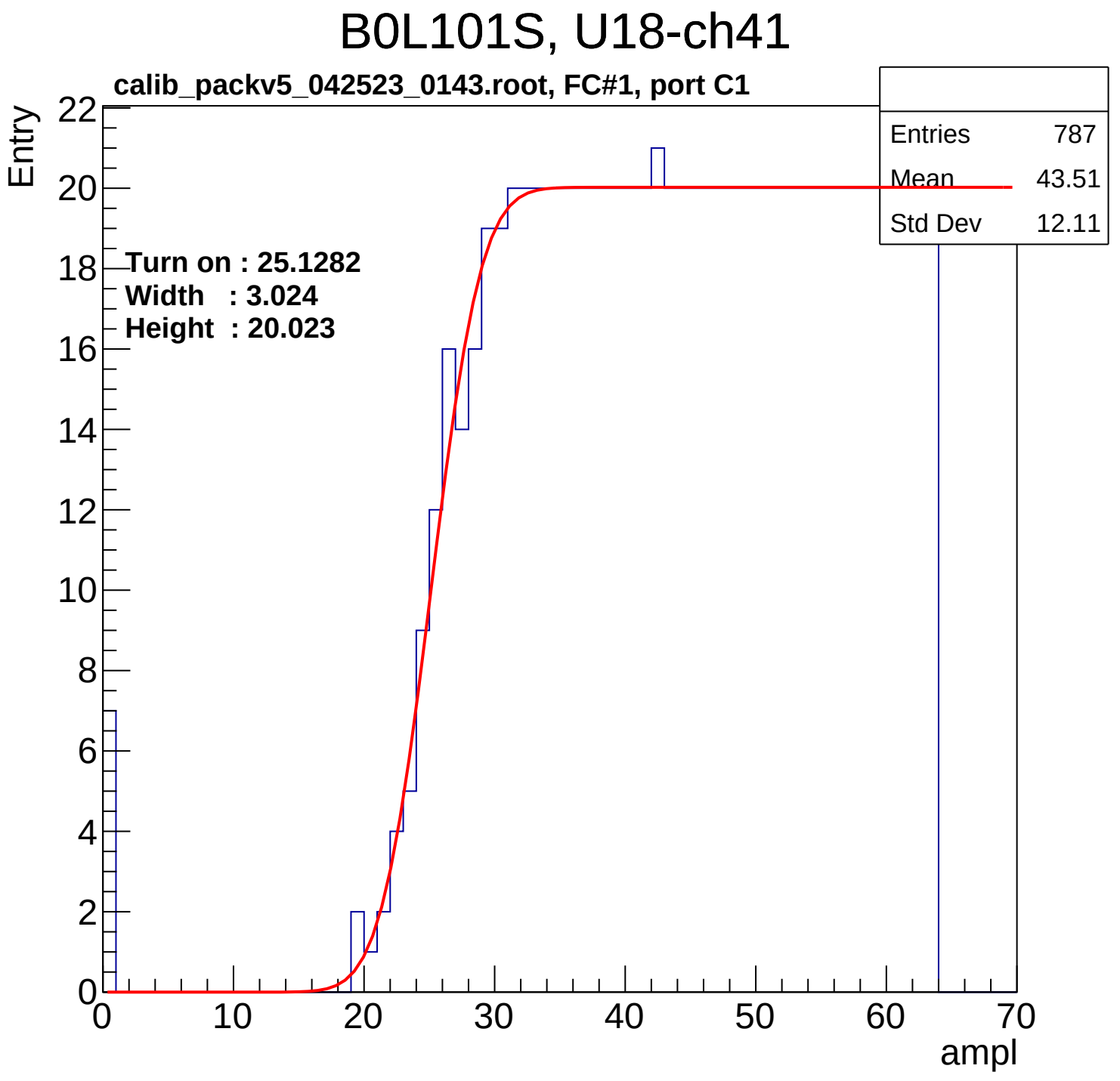
B0L101S, U18-ch41
calib_packv5_042523_0143.root, FC#1, port C1
Entries 787
Mean 43.51
Std Dev 12.11
Turn on : 25.1282
Width : 3.024
Height : 20.023
Entry
ampl
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12
14
16
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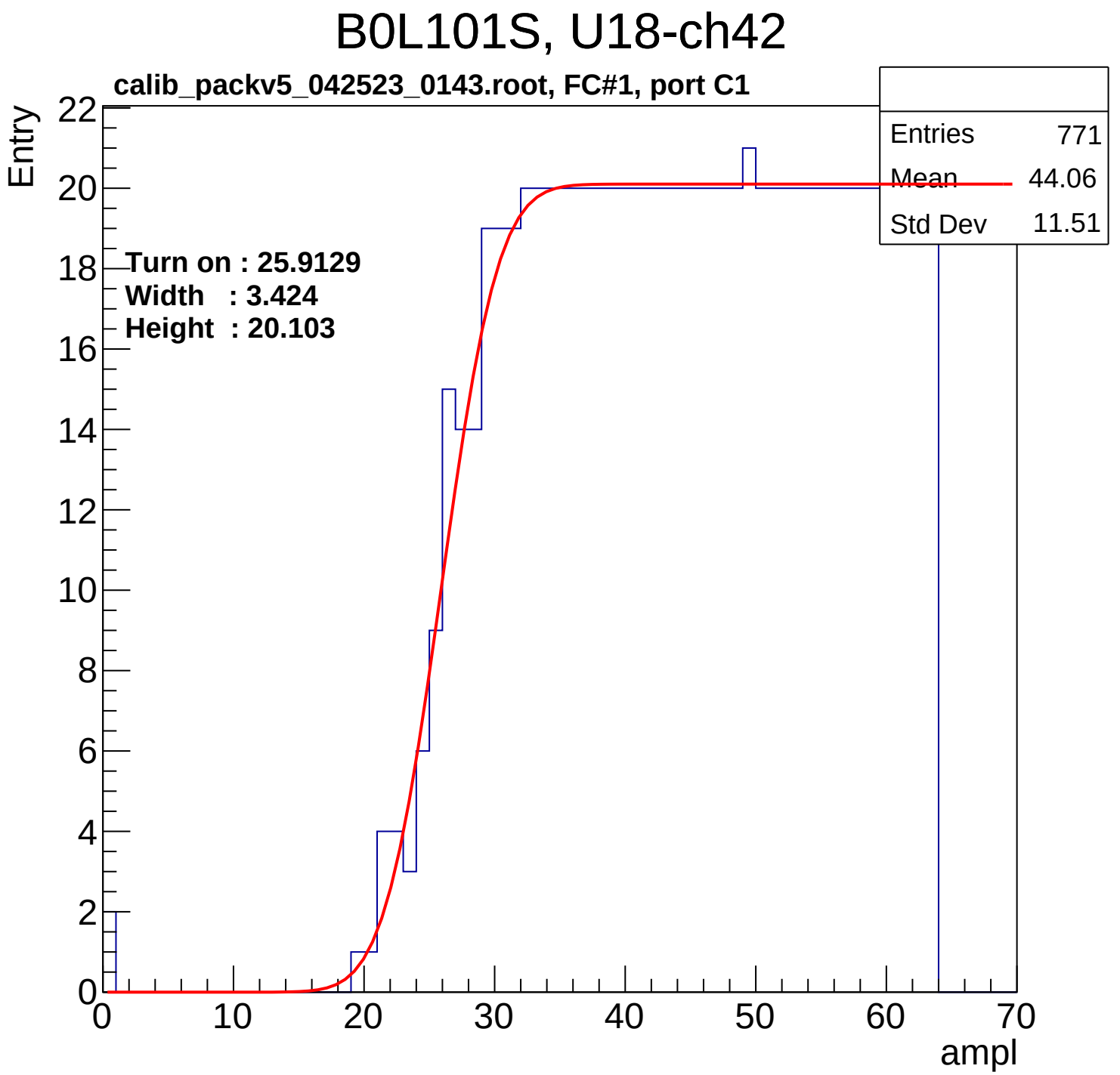
B0L101S, U18-ch42
calib_packv5_042523_0143.root, FC#1, port C1
Entries 771
Mean 44.06
Std Dev 11.51
Turn on : 25.9129
Width : 3.424
Height : 20.103
Entry
ampl
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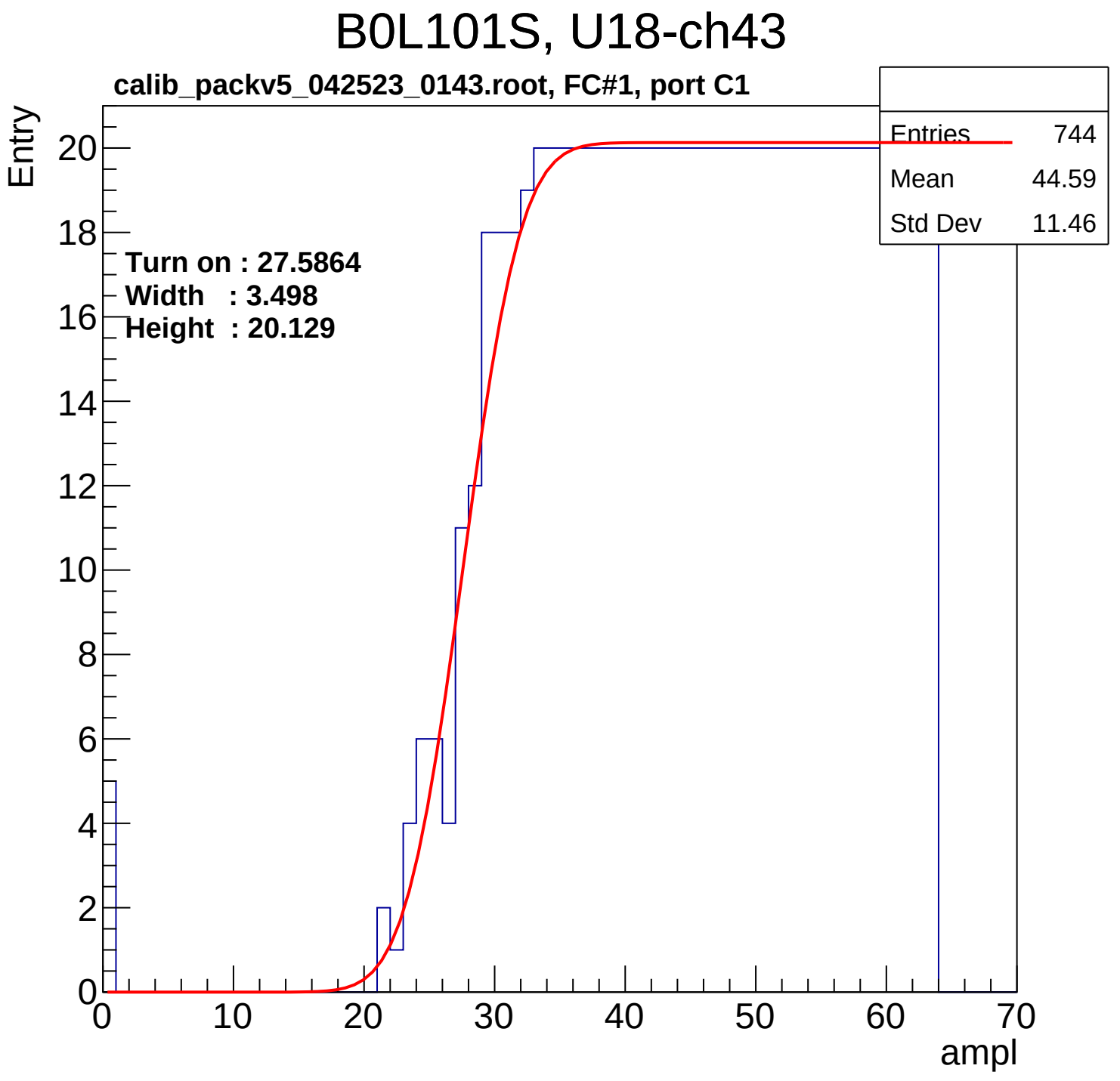
B0L101S, U18-ch43
calib_packv5_042523_0143.root, FC#1, port C1
Entries 744
Mean 44.59
Std Dev 11.46
Turn on : 27.5864
Width : 3.498
Height : 20.129
Entry
ampl
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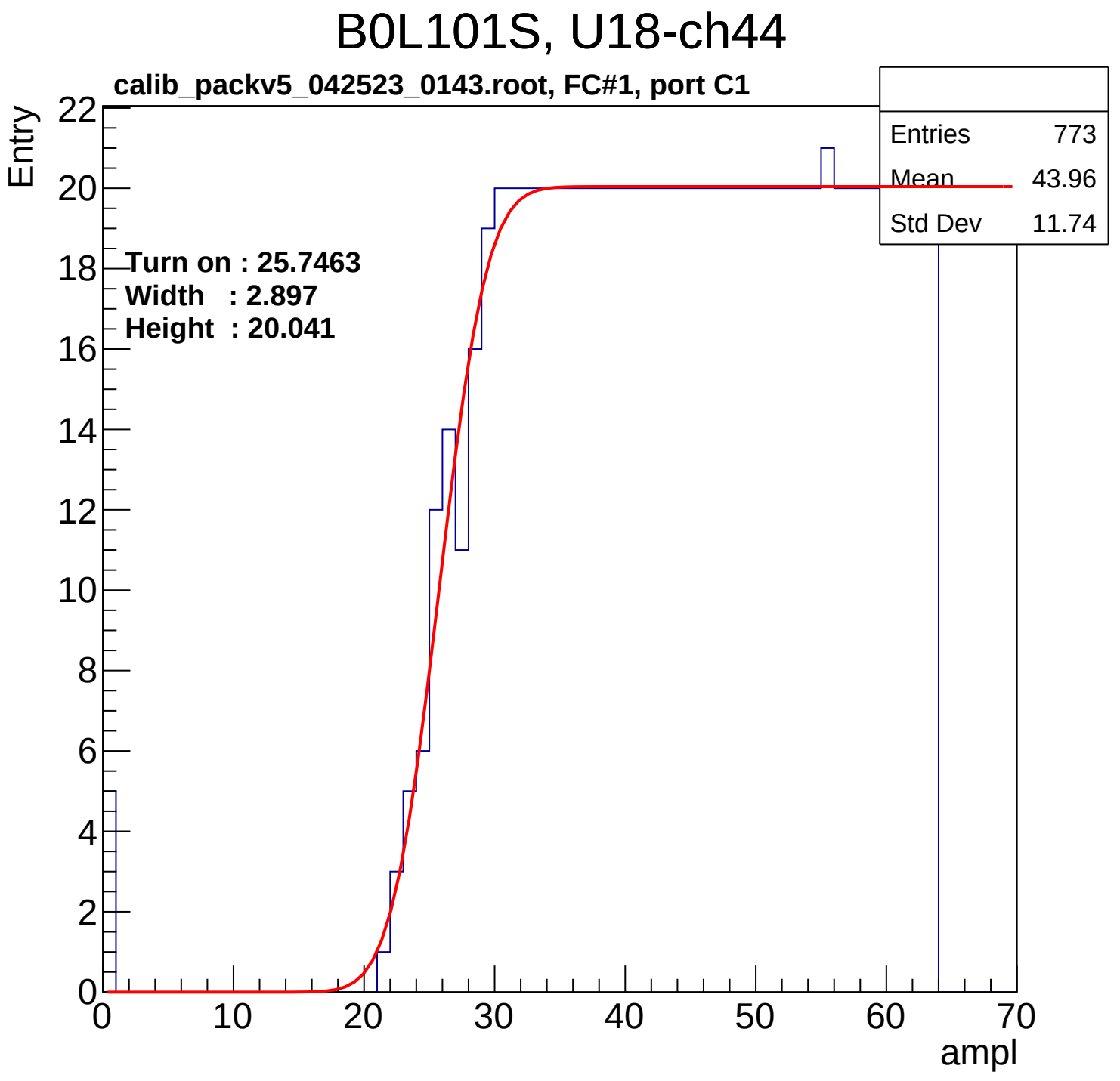
B0L101S, U18-ch44
calib_packv5_042523_0143.root, FC#1, port C1
Entries 773
Mean 43.96
Std Dev 11.74
Turn on : 25.7463
Width : 2.897
Height : 20.041
Entry
ampl
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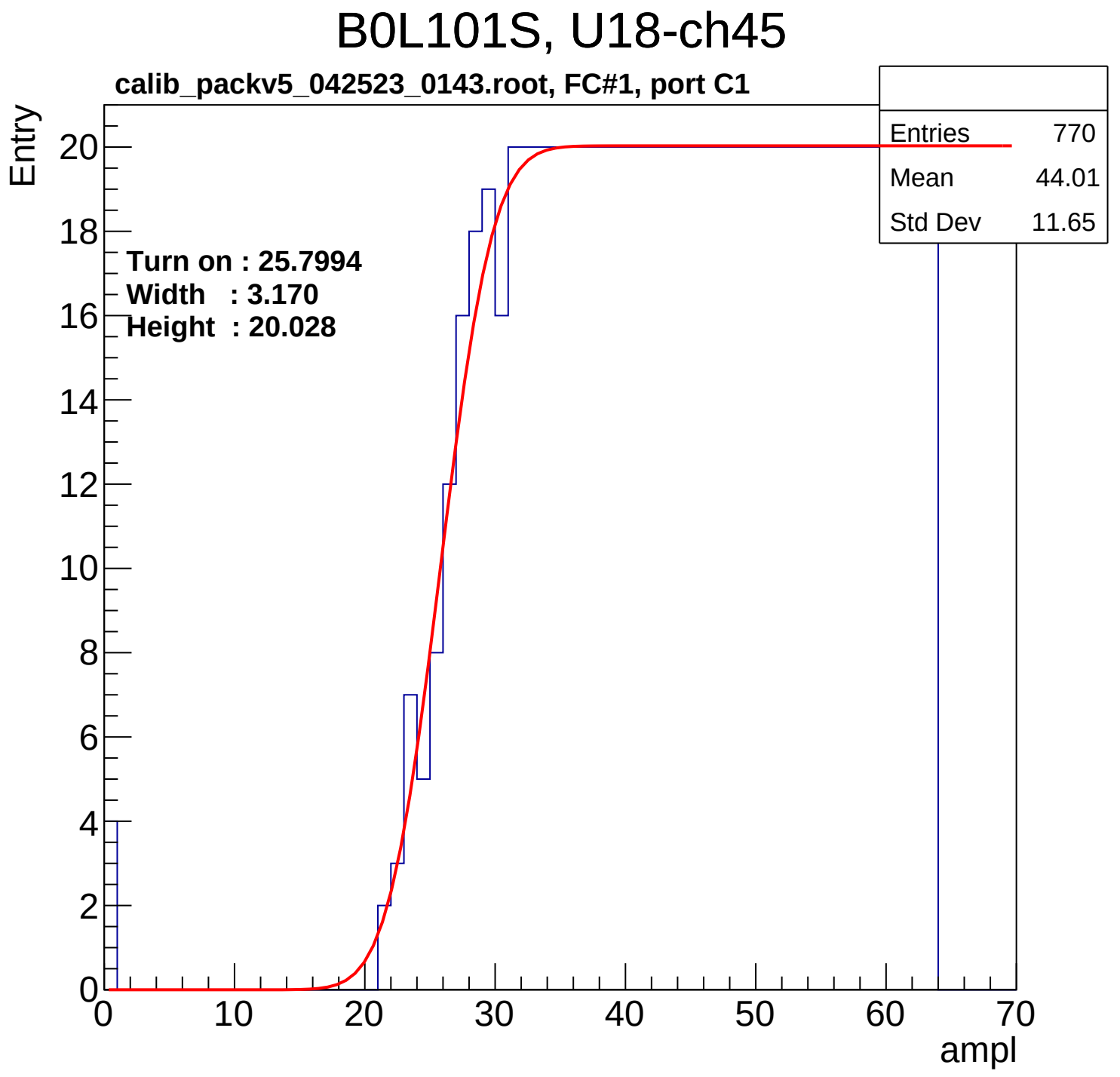
B0L101S, U18-ch45
calib_packv5_042523_0143.root, FC#1, port C1
Entries 770
Mean 44.01
Std Dev 11.65
Turn on : 25.7994
Width : 3.170
Height : 20.028
Entry
ampl
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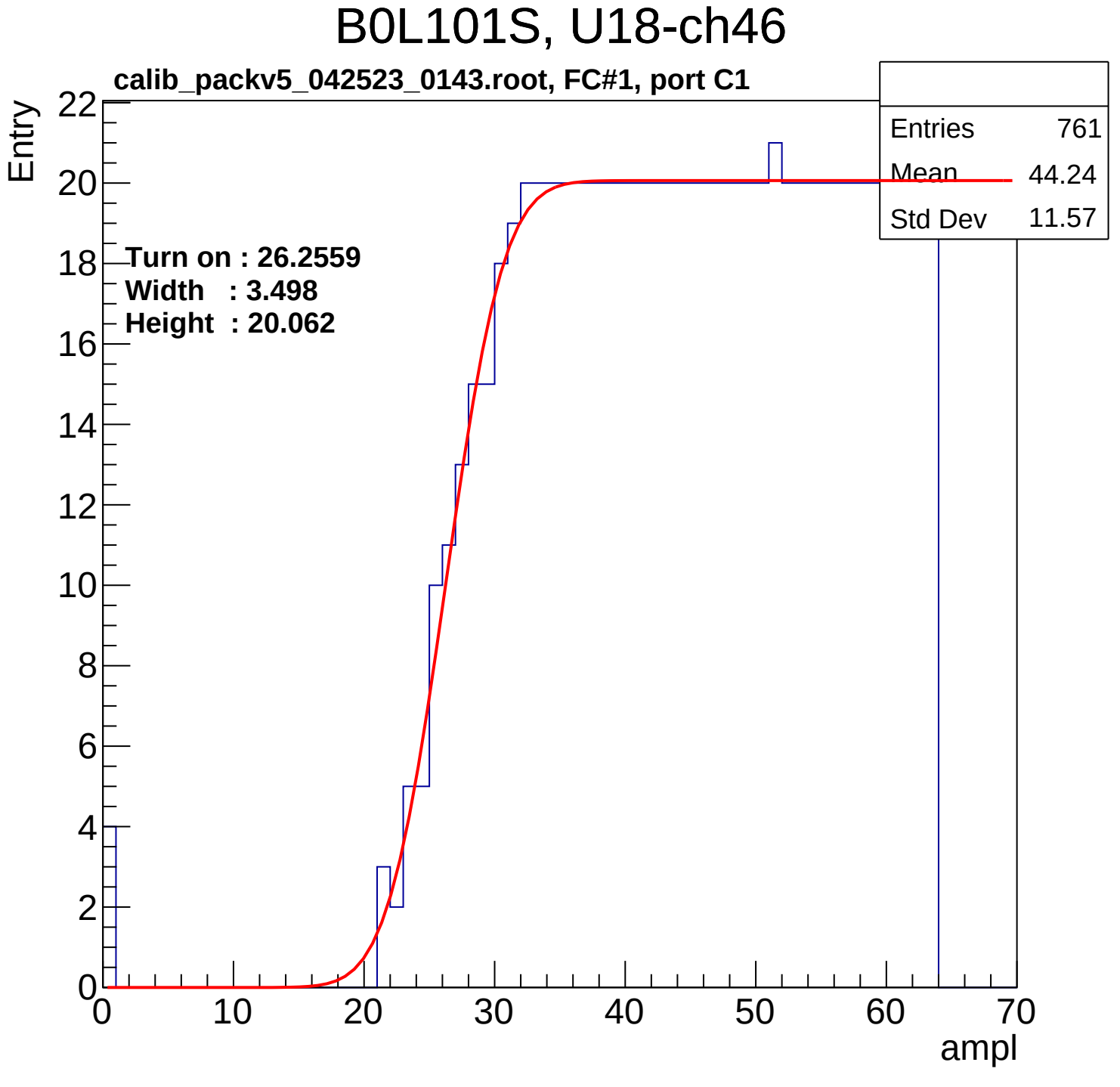
B0L101S, U18-ch46
calib_packv5_042523_0143.root, FC#1, port C1
Entries 761
Mean 44.24
Std Dev 11.57
Turn on : 26.2559
Width : 3.498
Height : 20.062
Entry
ampl
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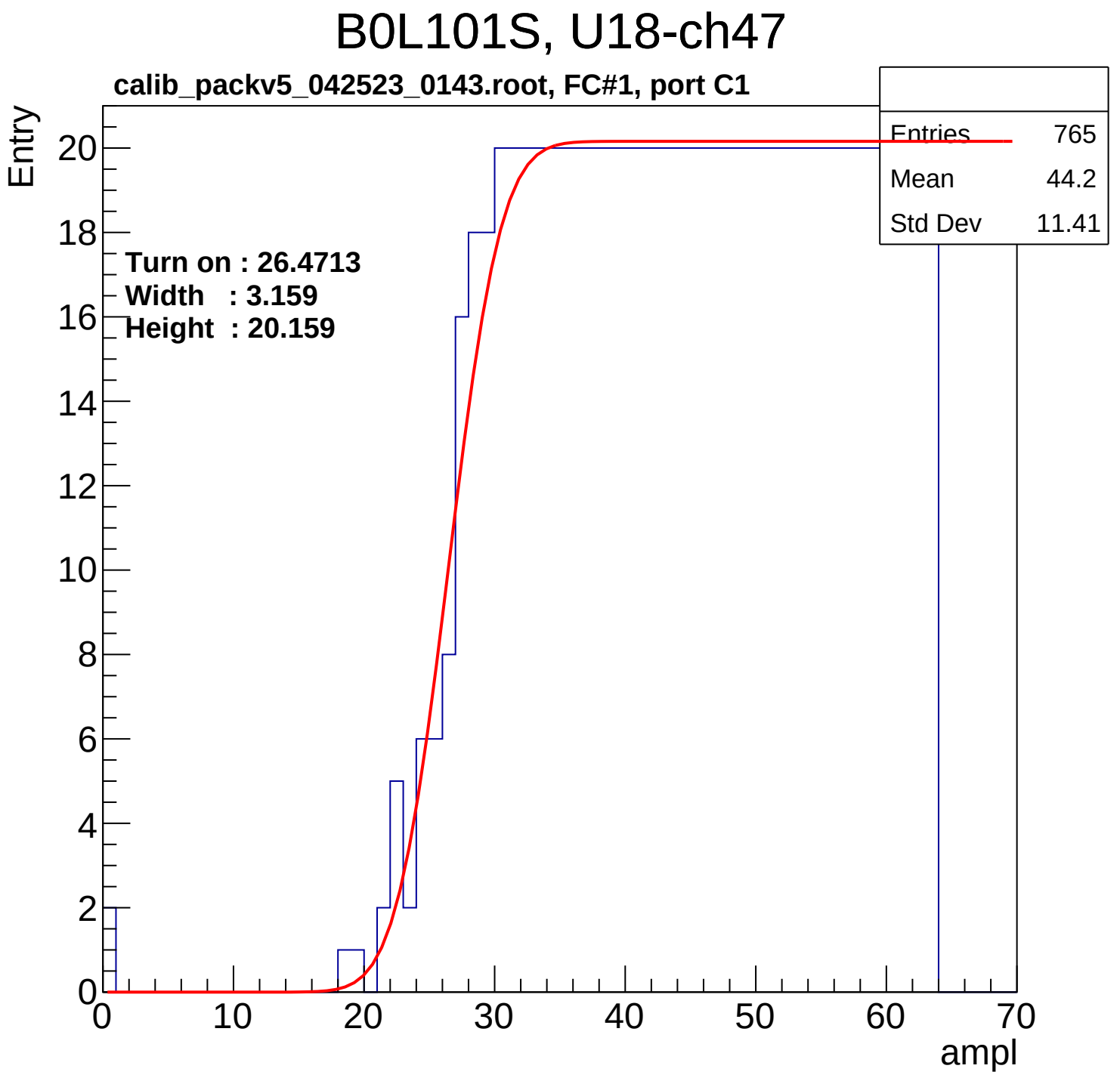
B0L101S, U18-ch47
calib_packv5_042523_0143.root, FC#1, port C1
Entries 765
Mean 44.2
Std Dev 11.41
Turn on : 26.4713
Width : 3.159
Height : 20.159
Entry
ampl
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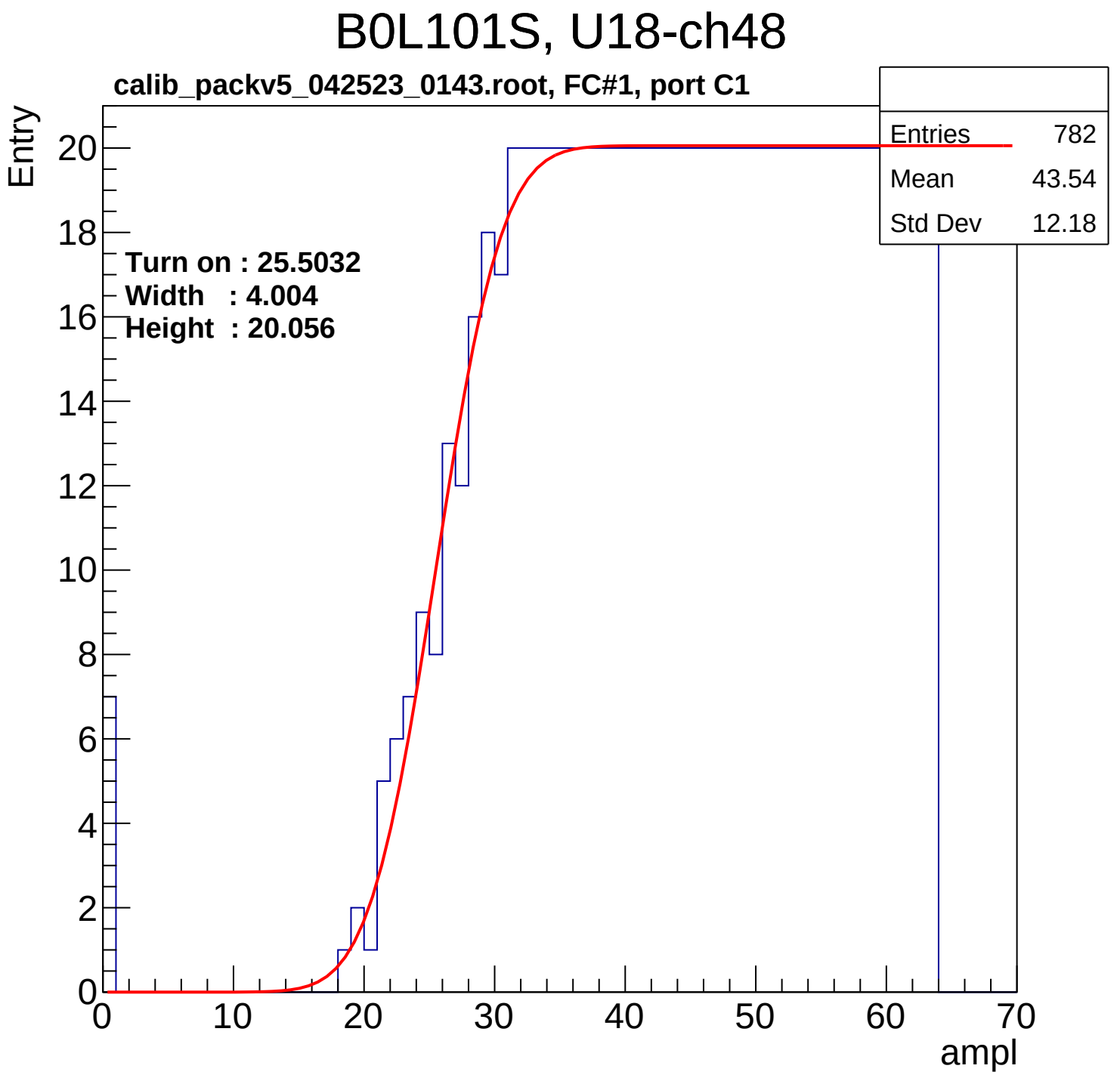
B0L101S, U18-ch48
calib_packv5_042523_0143.root, FC#1, port C1
Entries 782
Mean 43.54
Std Dev 12.18
Turn on : 25.5032
Width : 4.004
Height : 20.056
Entry
ampl
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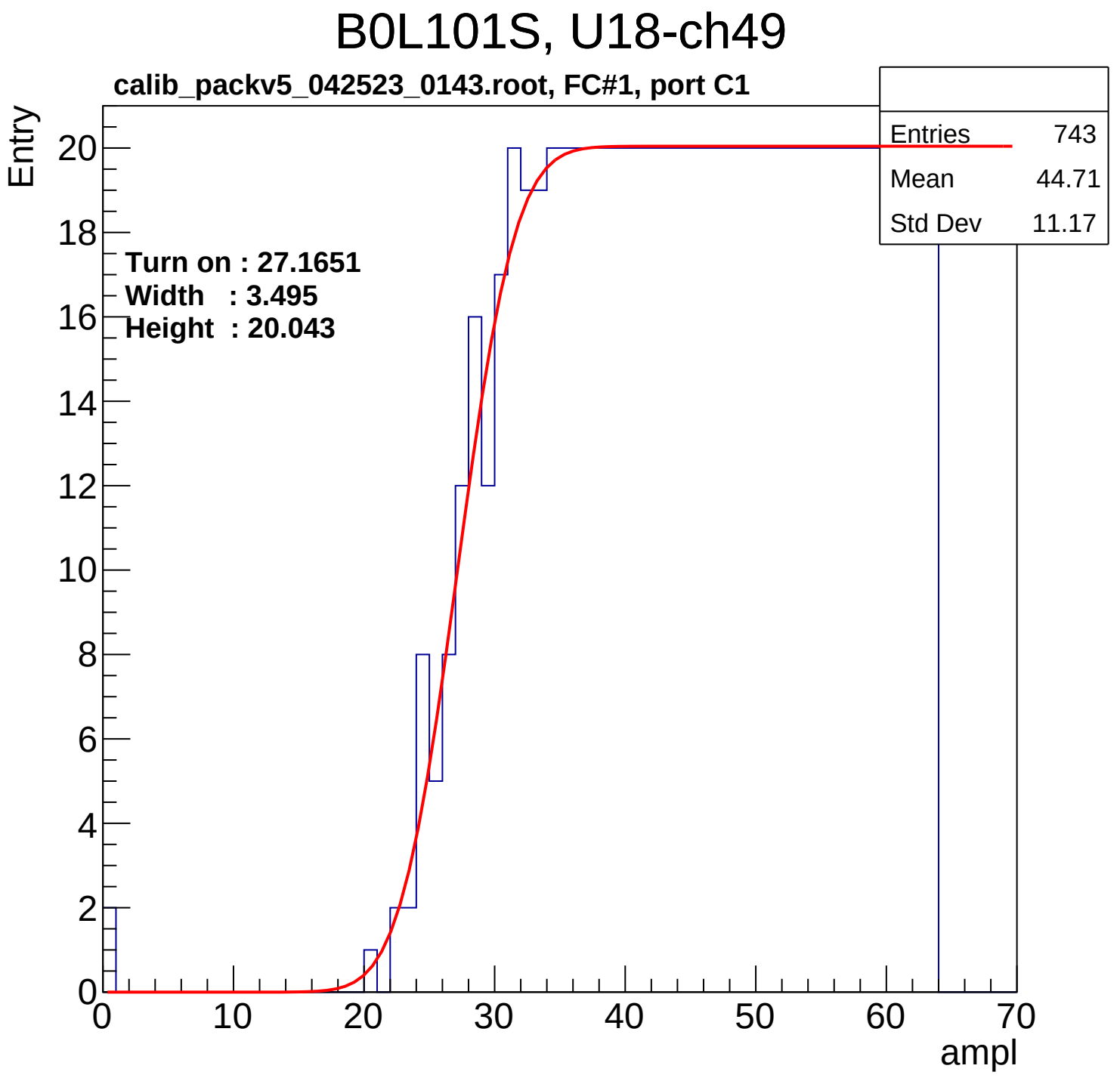
B0L101S, U18-ch49
calib_packv5_042523_0143.root, FC#1, port C1
Entries 743
Mean 44.71
Std Dev 11.17
Turn on : 27.1651
Width : 3.495
Height : 20.043
Entry
ampl
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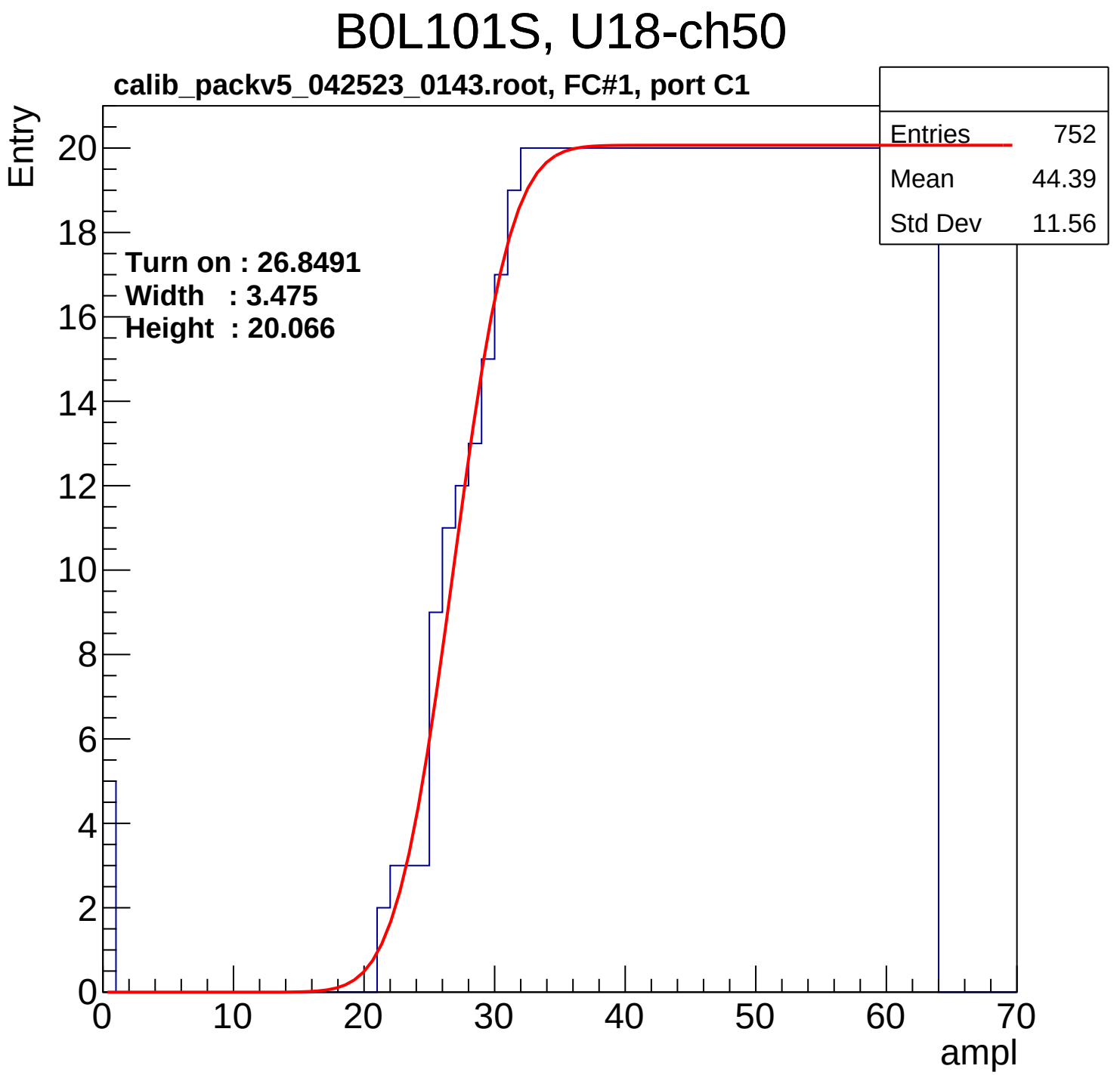
B0L101S, U18-ch50
calib_packv5_042523_0143.root, FC#1, port C1
Entries 752
Mean 44.39
Std Dev 11.56
Turn on : 26.8491
Width : 3.475
Height : 20.066
Entry
ampl
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8
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60
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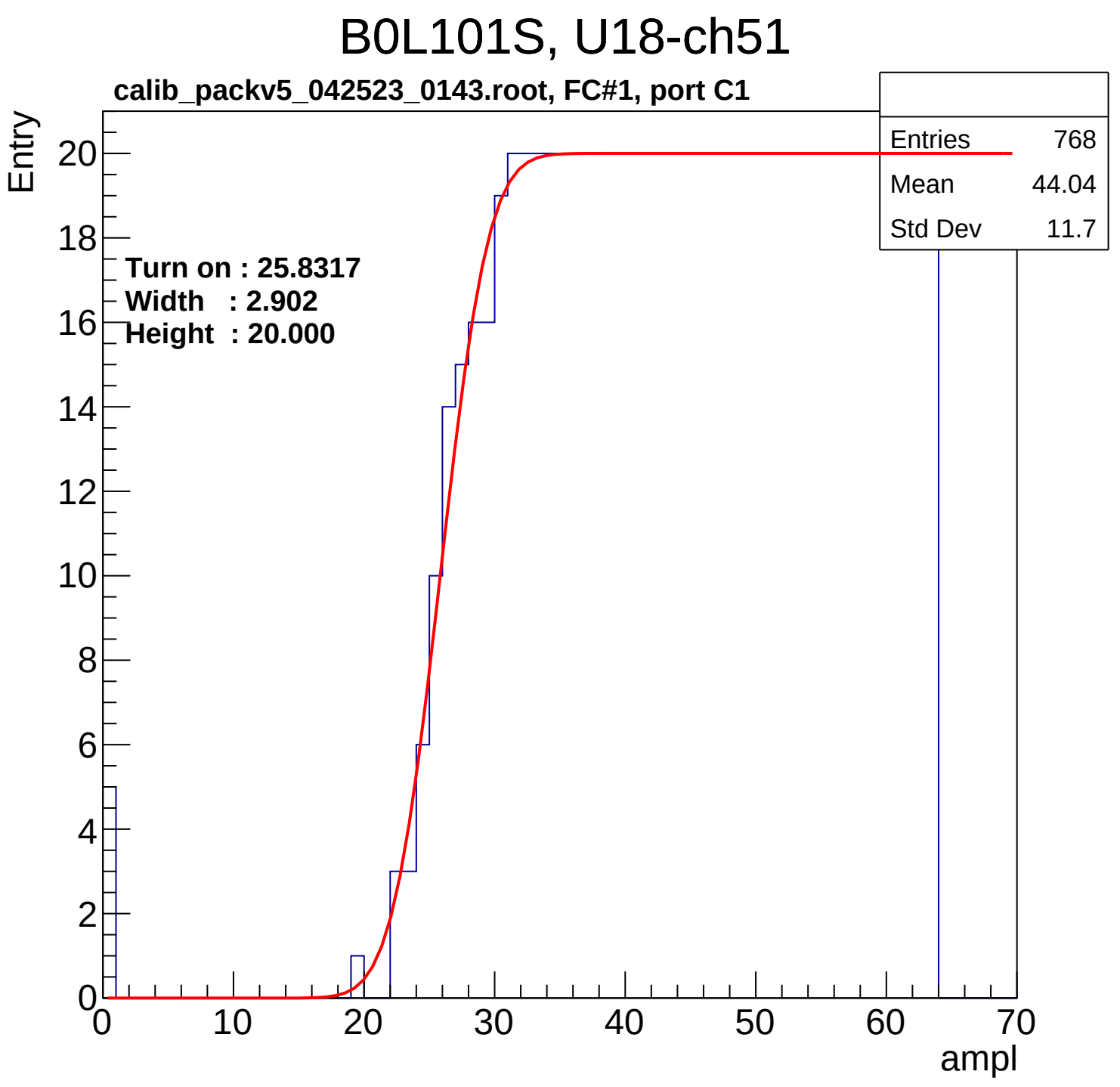
B0L101S, U18-ch51
calib_packv5_042523_0143.root, FC#1, port C1
Entries 768
Mean 44.04
Std Dev 11.7
Turn on : 25.8317
Width : 2.902
Height : 20.000
Entry
ampl
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8
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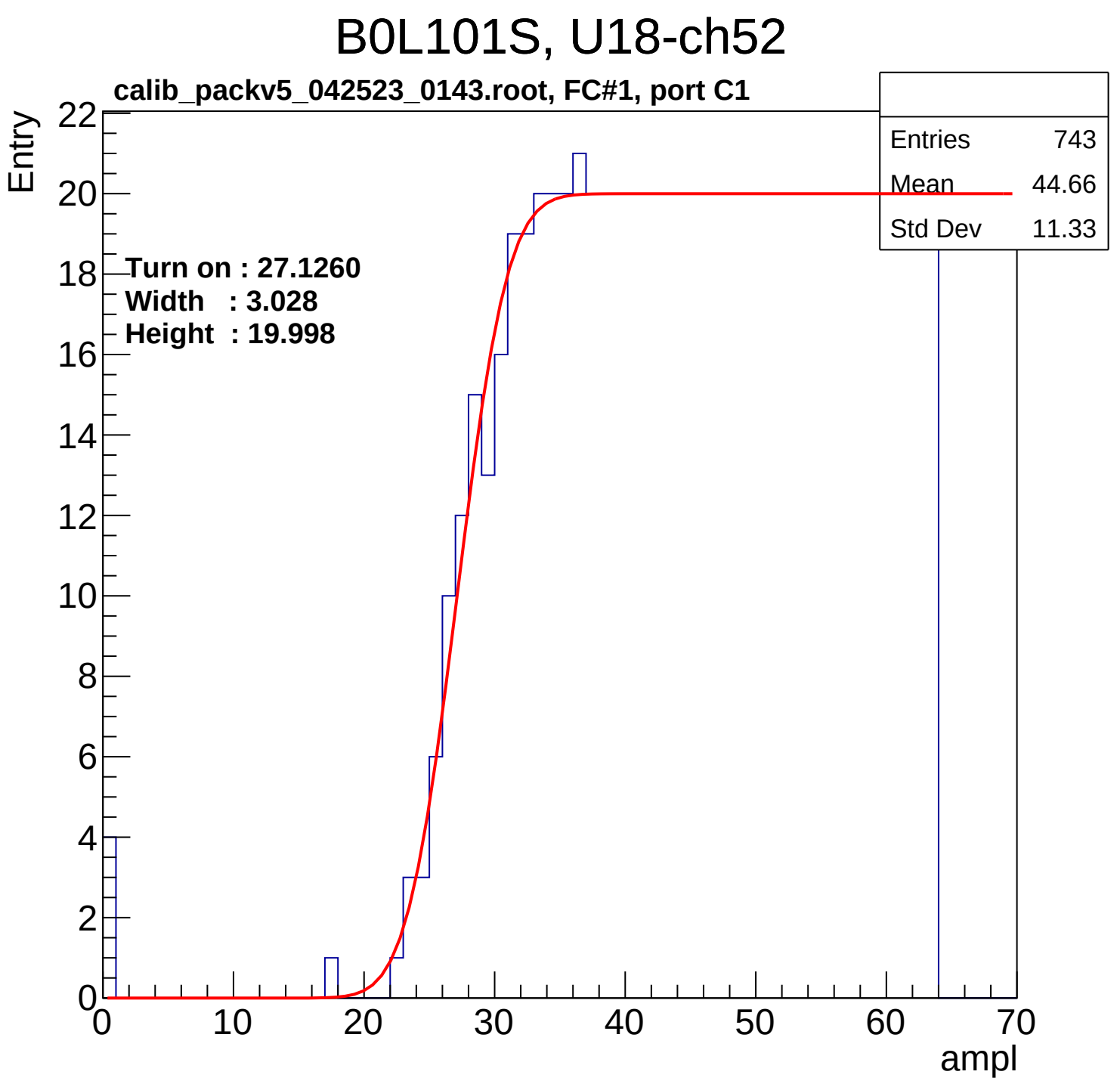
B0L101S, U18-ch52
calib_packv5_042523_0143.root, FC#1, port C1
Entries 743
Mean 44.66
Std Dev 11.33
Turn on : 27.1260
Width : 3.028
Height : 19.998
Entry
ampl
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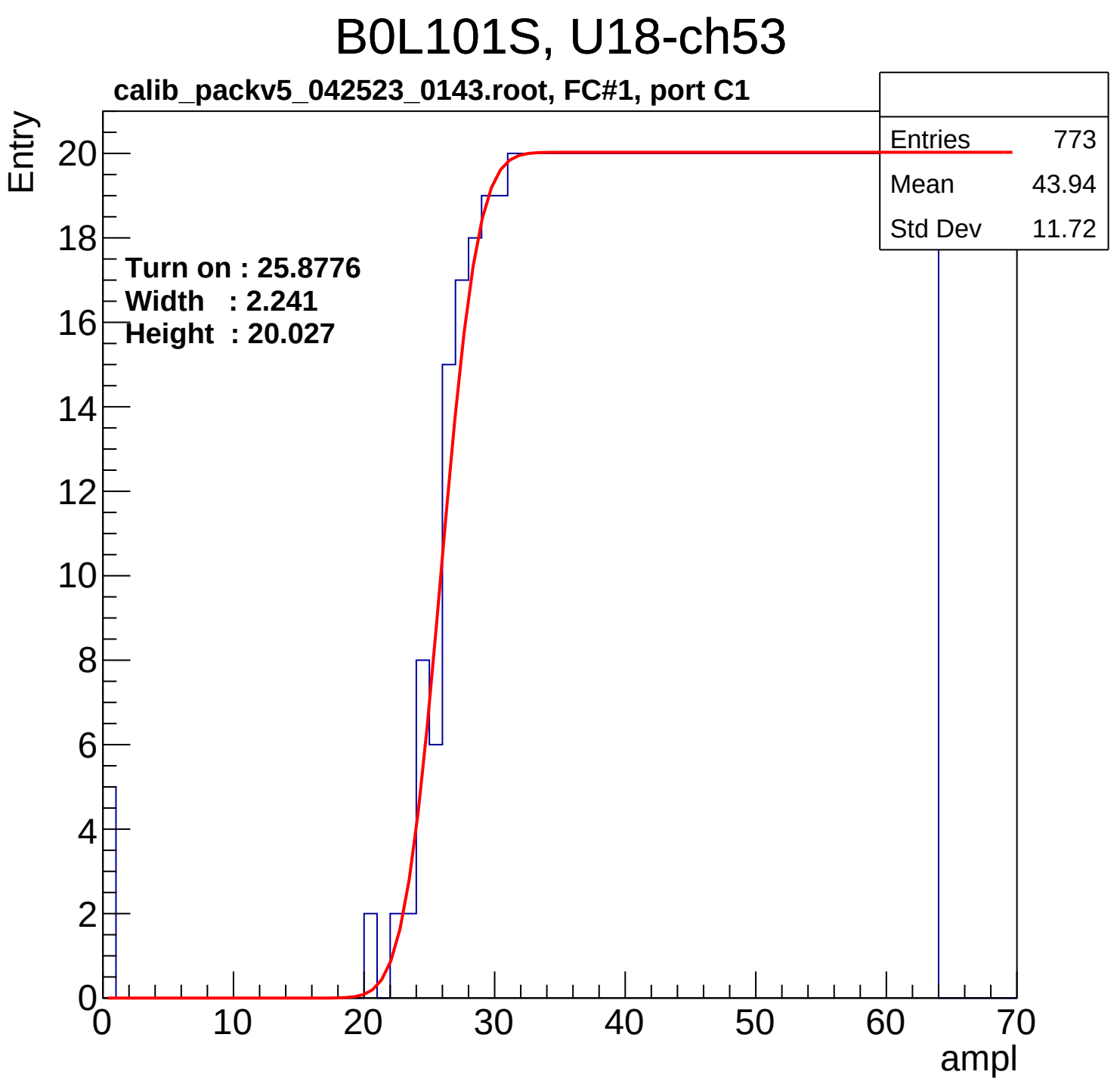
B0L101S, U18-ch53
calib_packv5_042523_0143.root, FC#1, port C1
Entries 773
Mean 43.94
Std Dev 11.72
Turn on : 25.8776
Width : 2.241
Height : 20.027
Entry
ampl
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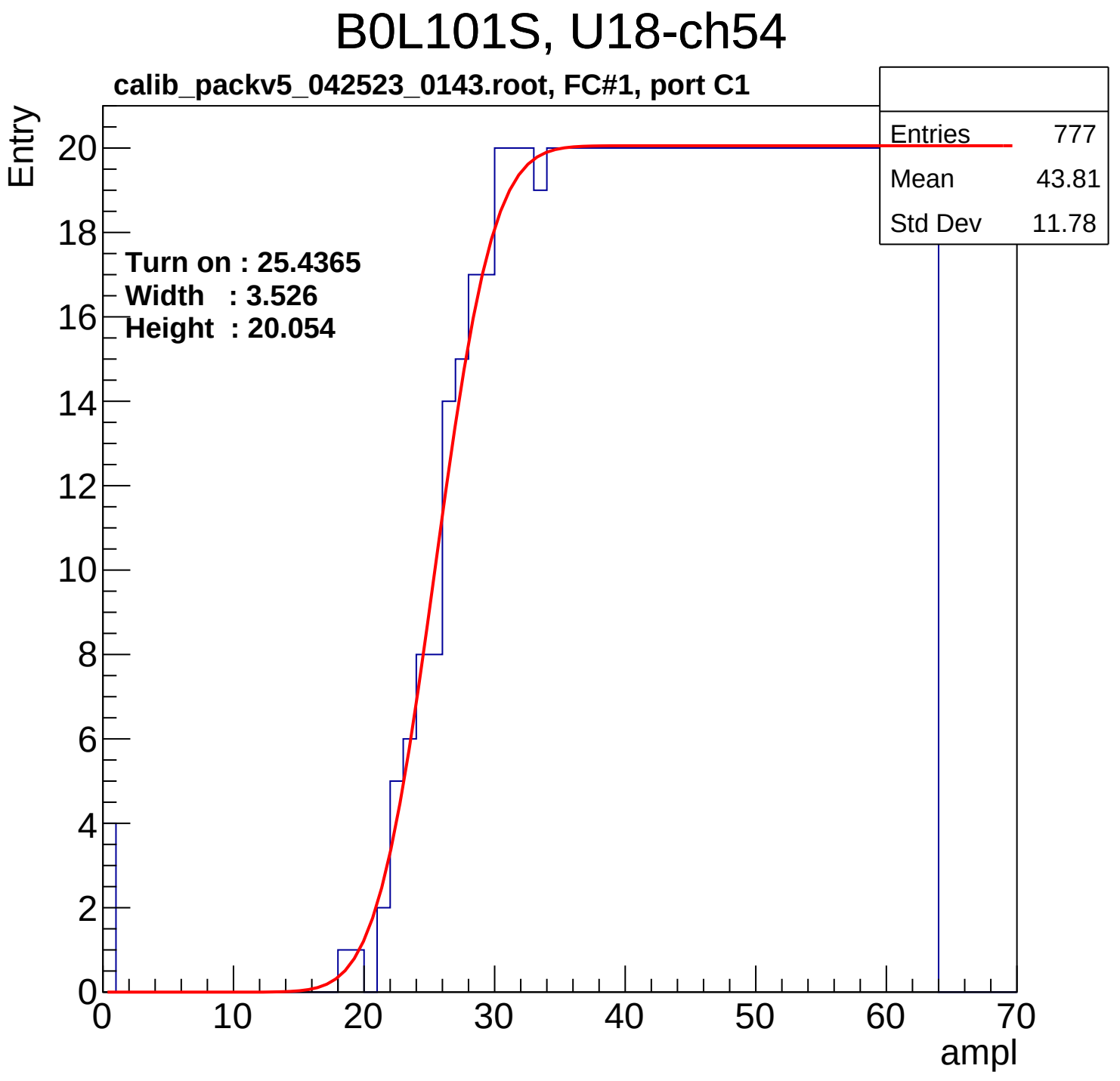
B0L101S, U18-ch54
calib_packv5_042523_0143.root, FC#1, port C1
Entries 777
Mean 43.81
Std Dev 11.78
Turn on : 25.4365
Width : 3.526
Height : 20.054
Entry
ampl
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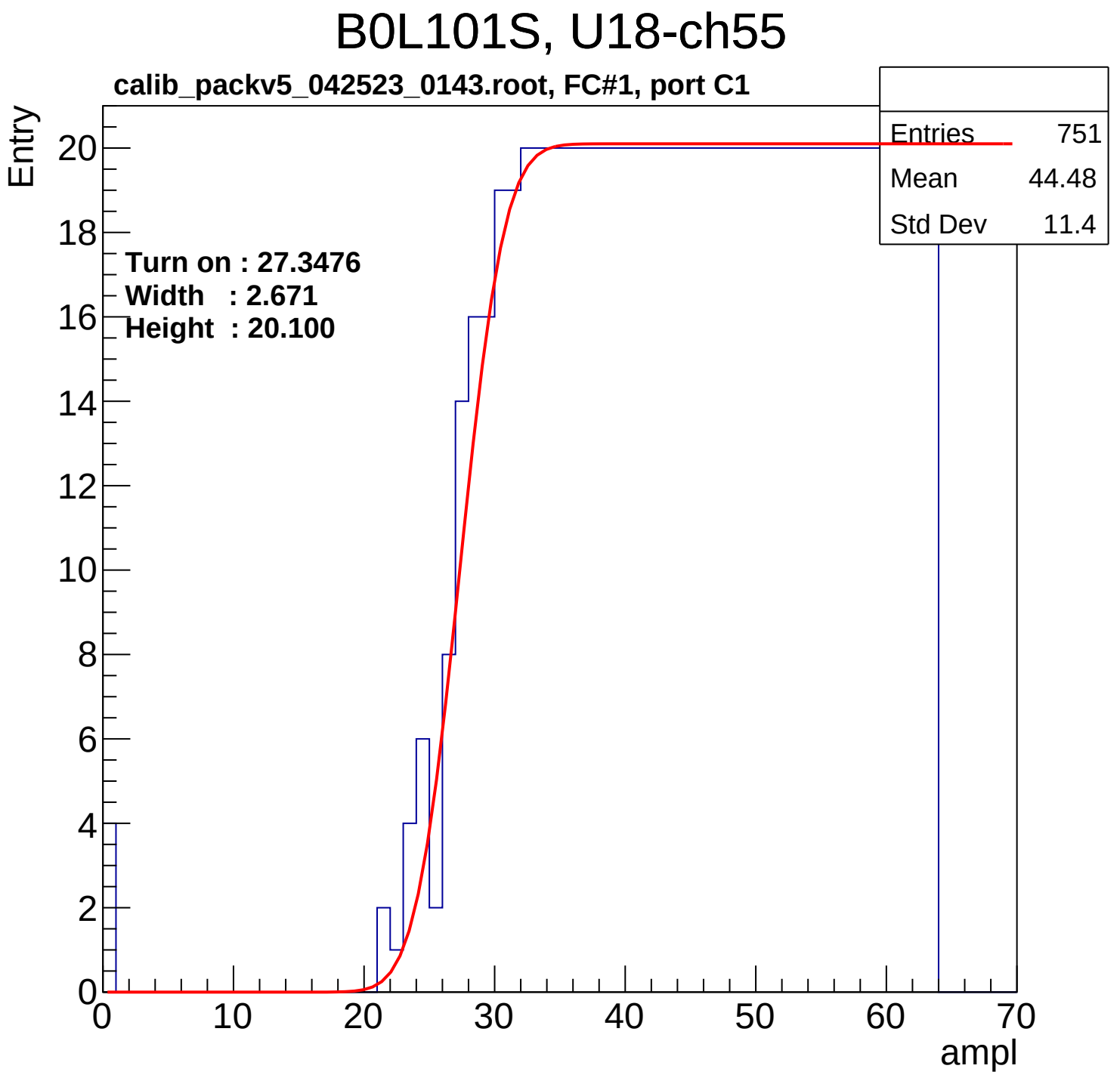
B0L101S, U18-ch55
calib_packv5_042523_0143.root, FC#1, port C1
Entries 751
Mean 44.48
Std Dev 11.4
Turn on : 27.3476
Width : 2.671
Height : 20.100
Entry
ampl
0
2
4
6
8
10
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14
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18
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40
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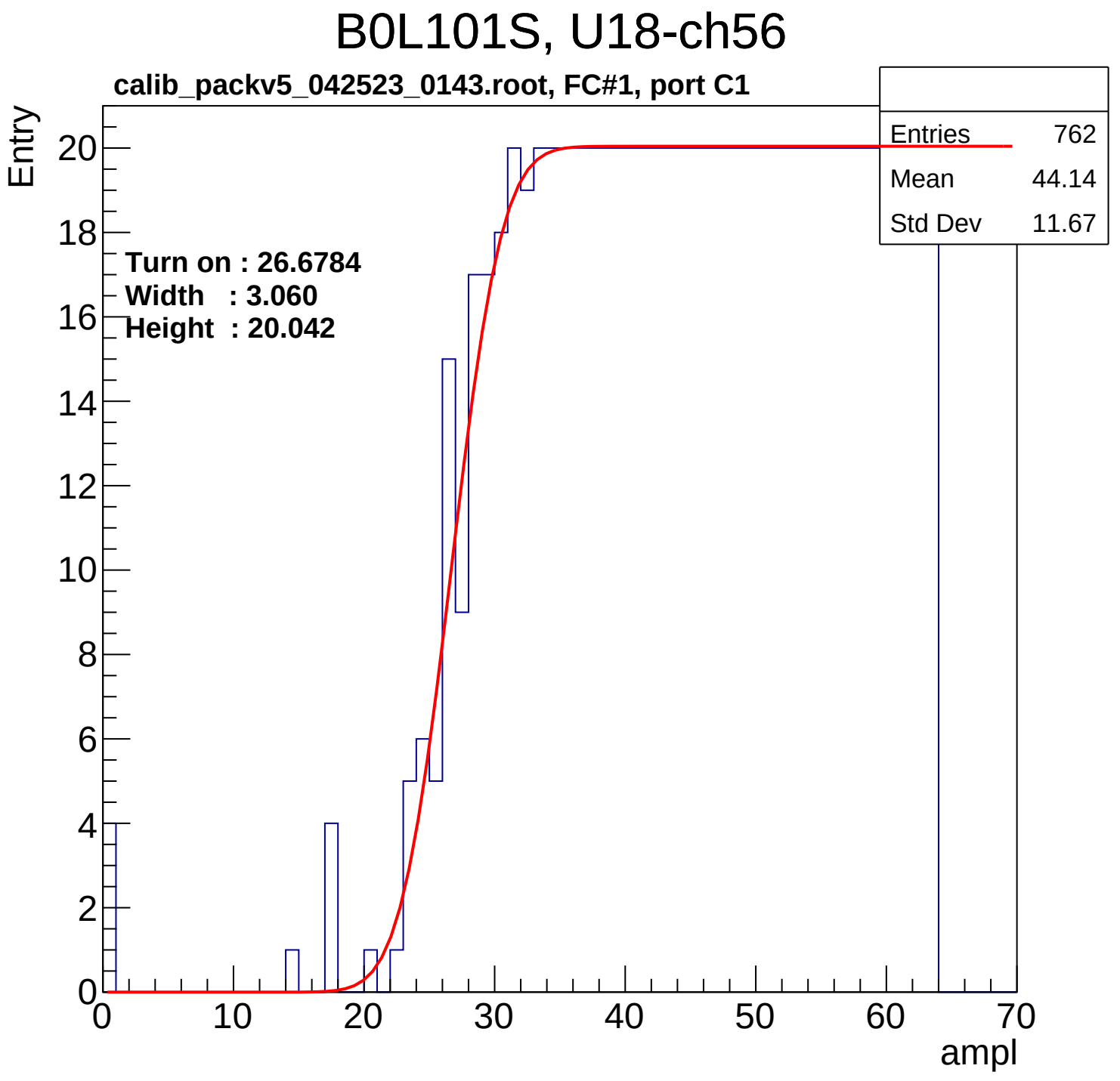
B0L101S, U18-ch56
calib_packv5_042523_0143.root, FC#1, port C1
Entries 762
Mean 44.14
Std Dev 11.67
Turn on : 26.6784
Width : 3.060
Height : 20.042
Entry
ampl
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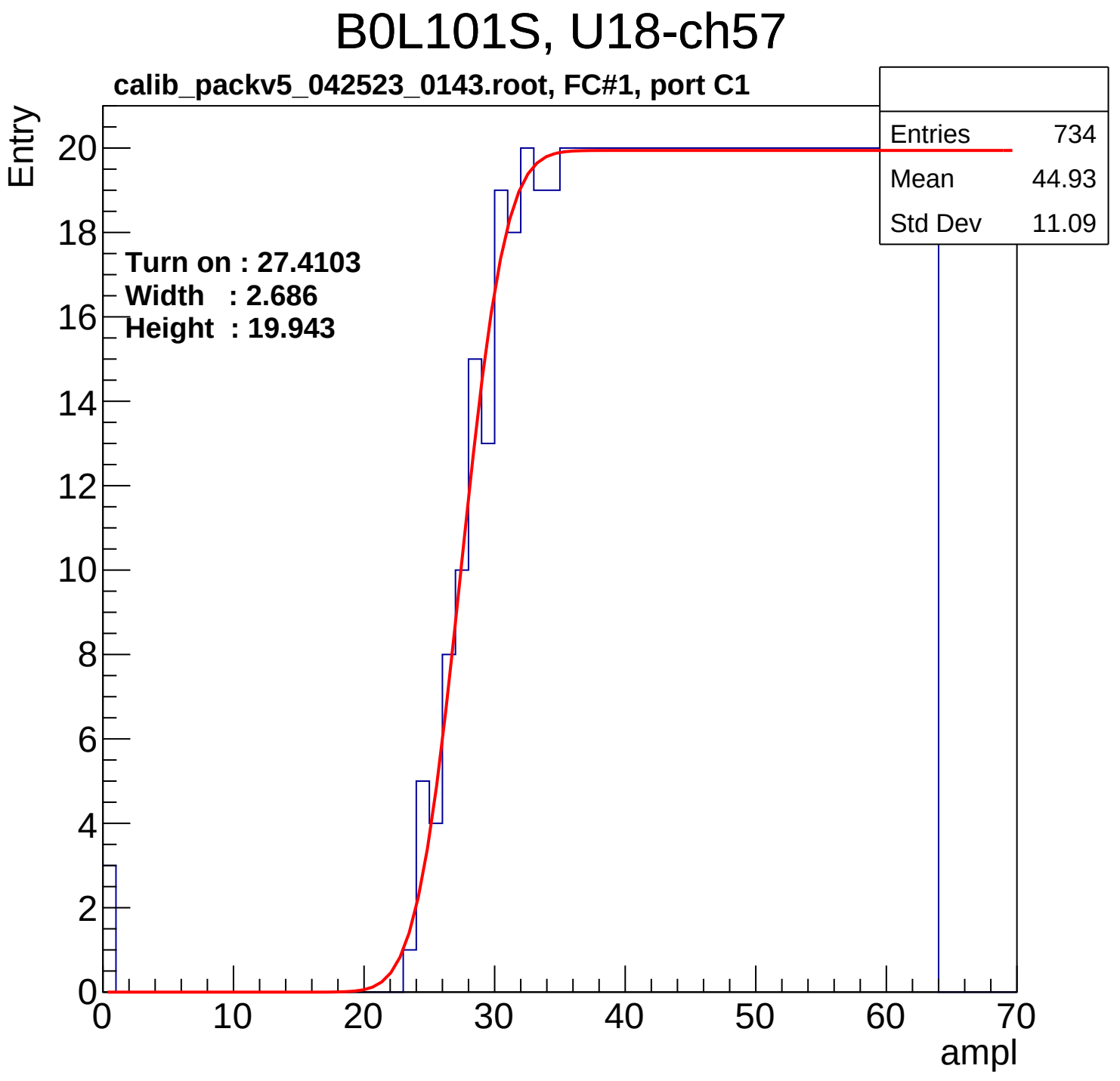
B0L101S, U18-ch57
calib_packv5_042523_0143.root, FC#1, port C1
Entries 734
Mean 44.93
Std Dev 11.09
Turn on : 27.4103
Width : 2.686
Height : 19.943
Entry
ampl
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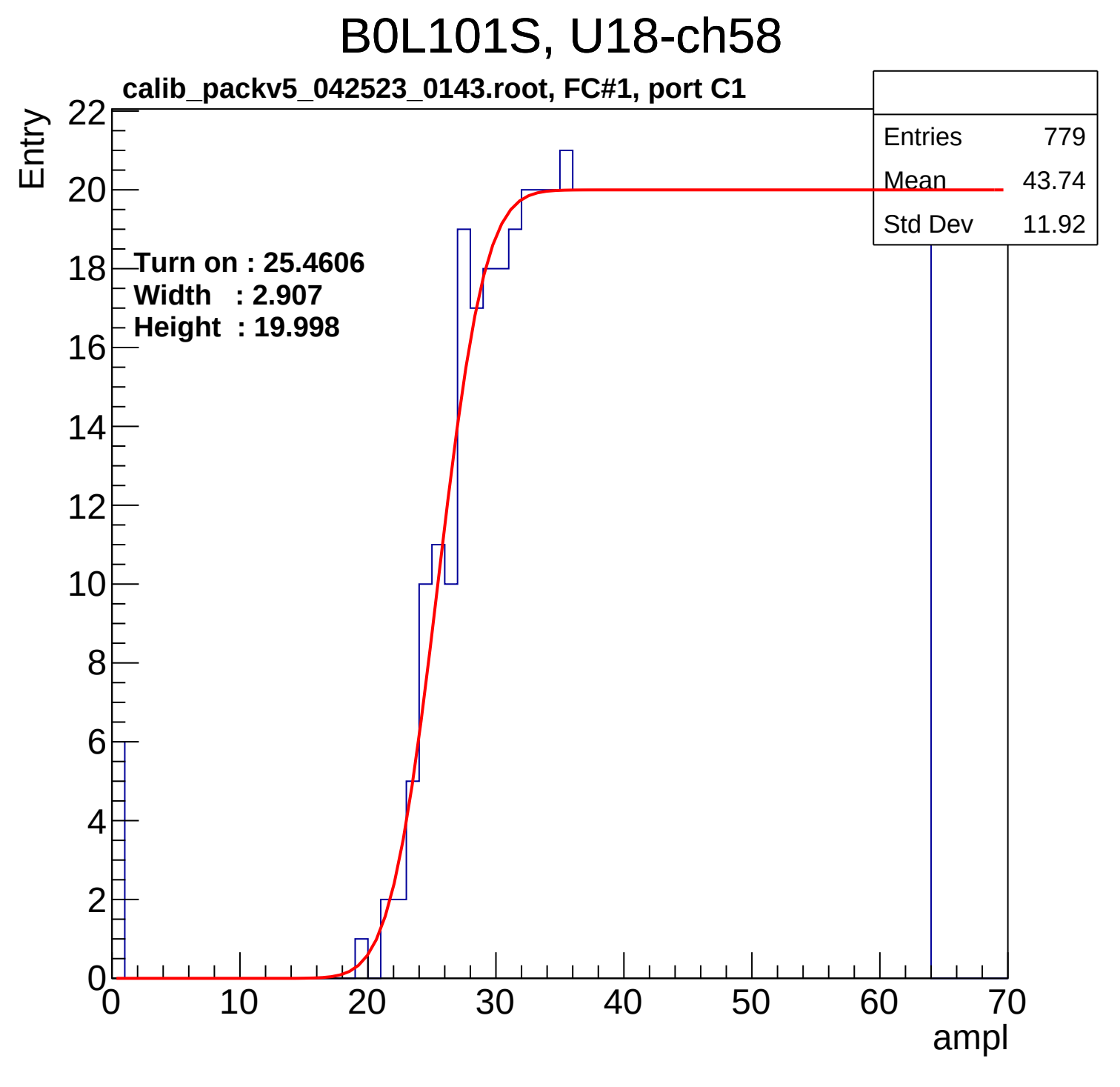
B0L101S, U18-ch58
calib_packv5_042523_0143.root, FC#1, port C1
Entries 779
Mean 43.74
Std Dev 11.92
Turn on : 25.4606
Width : 2.907
Height : 19.998
Entry
ampl
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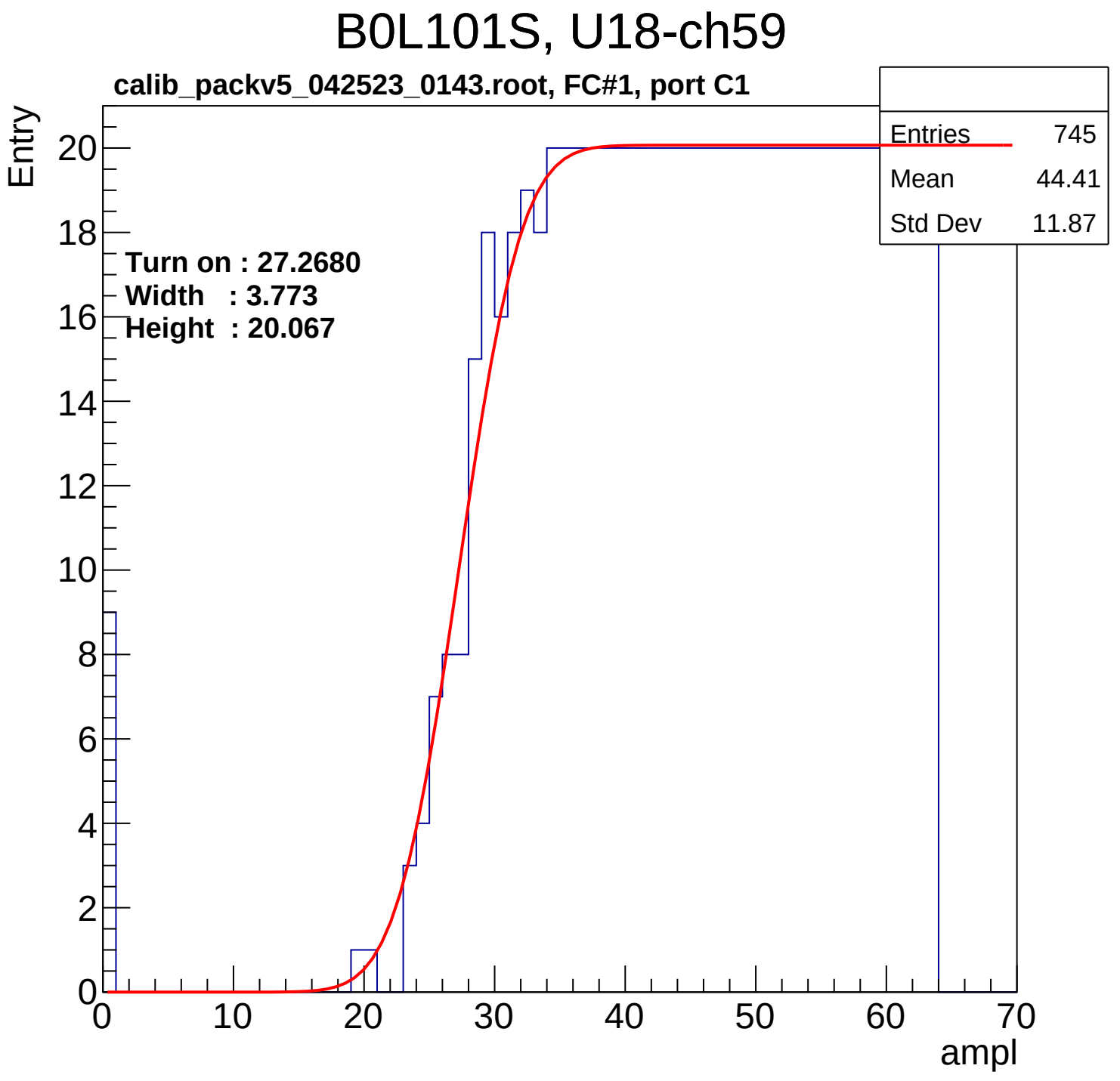
B0L101S, U18-ch59
calib_packv5_042523_0143.root, FC#1, port C1
Entries 745
Mean 44.41
Std Dev 11.87
Turn on : 27.2680
Width : 3.773
Height : 20.067
Entry
ampl
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6
8
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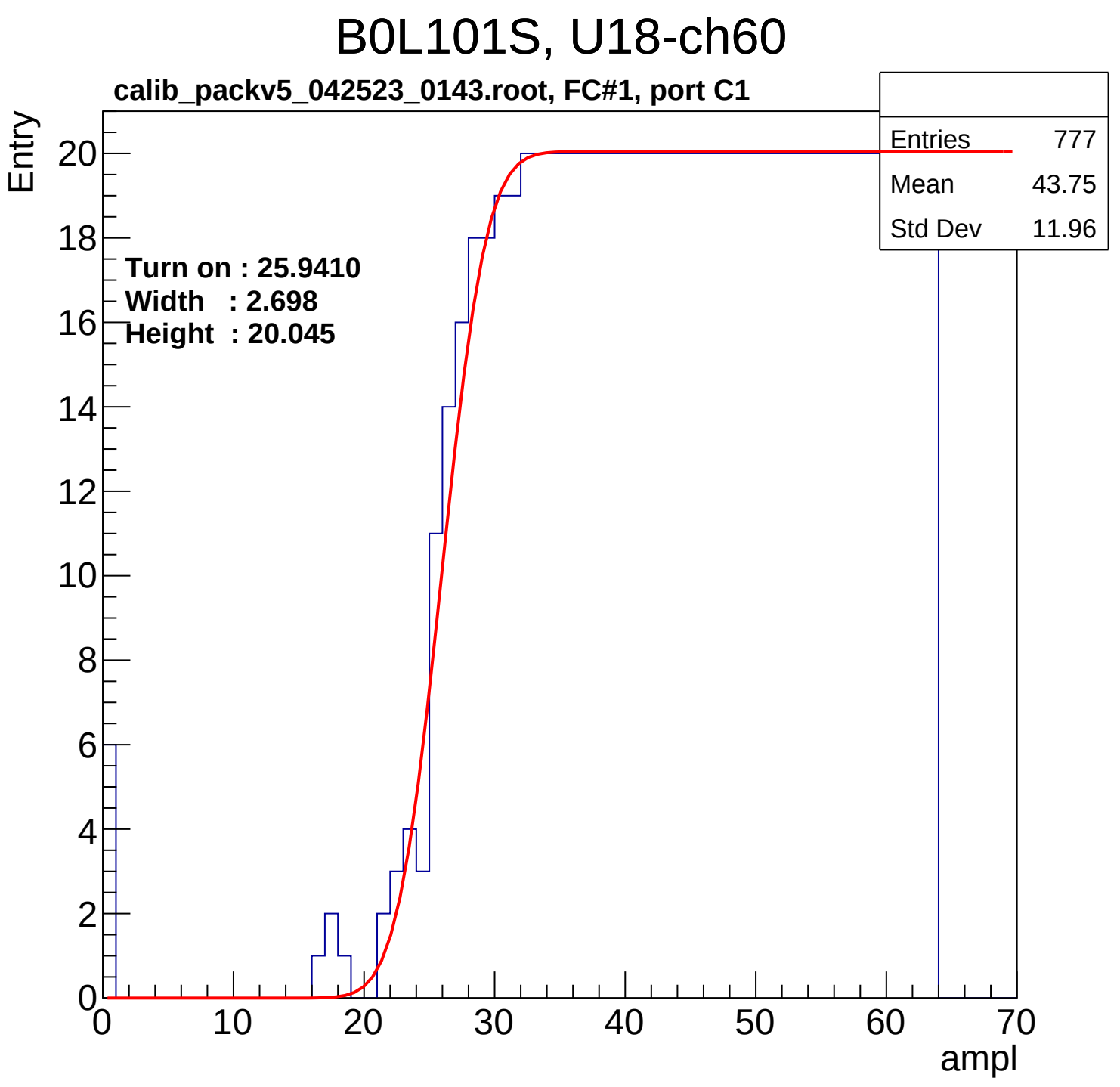
B0L101S, U18-ch60
calib_packv5_042523_0143.root, FC#1, port C1
Entries 777
Mean 43.75
Std Dev 11.96
Turn on : 25.9410
Width : 2.698
Height : 20.045
Entry
ampl
0
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6
8
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12
14
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18
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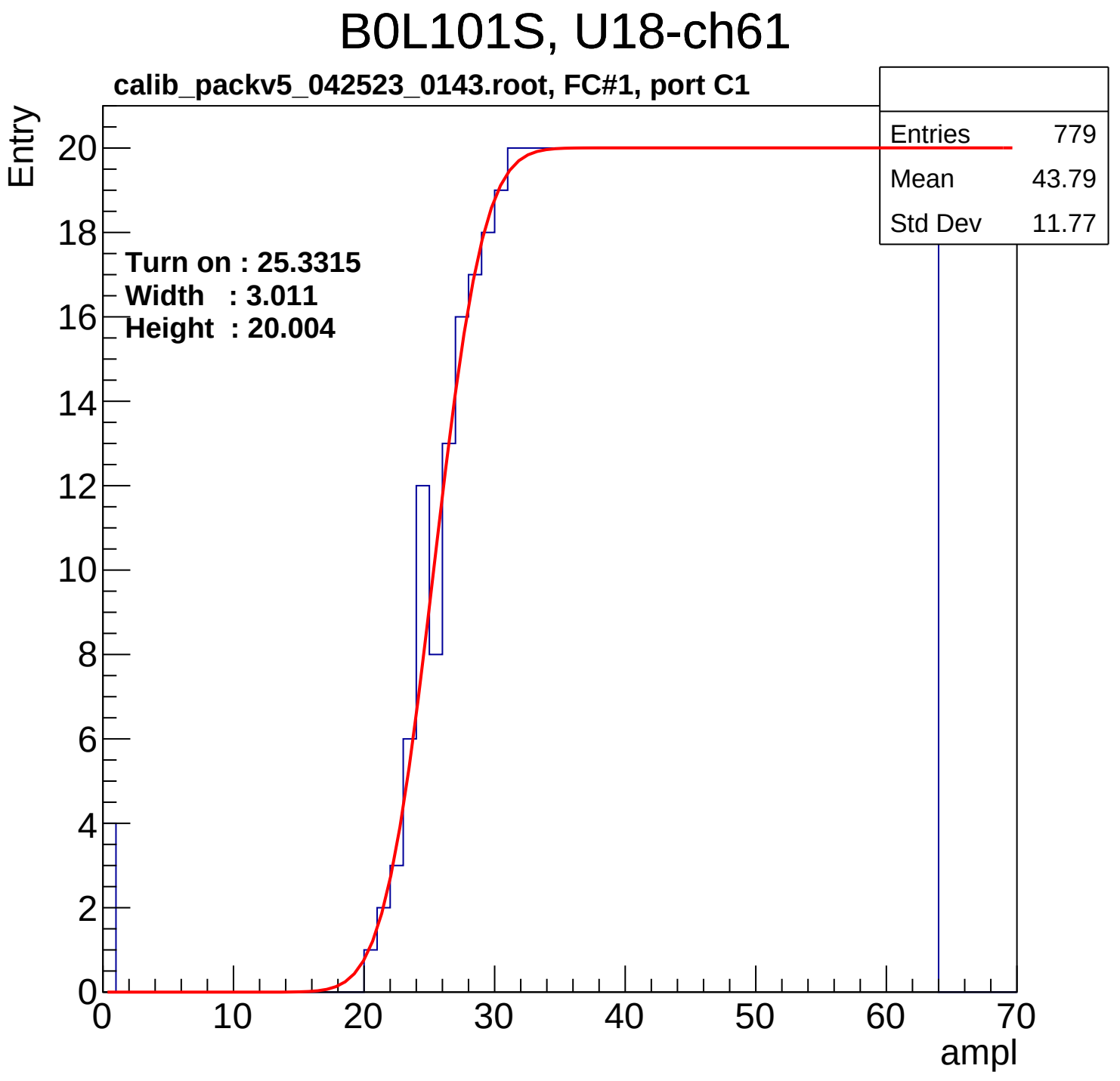
B0L101S, U18-ch61
calib_packv5_042523_0143.root, FC#1, port C1
Entries 779
Mean 43.79
Std Dev 11.77
Turn on : 25.3315
Width : 3.011
Height : 20.004
Entry
ampl
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2
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6
8
10
12
14
16
18
20
0
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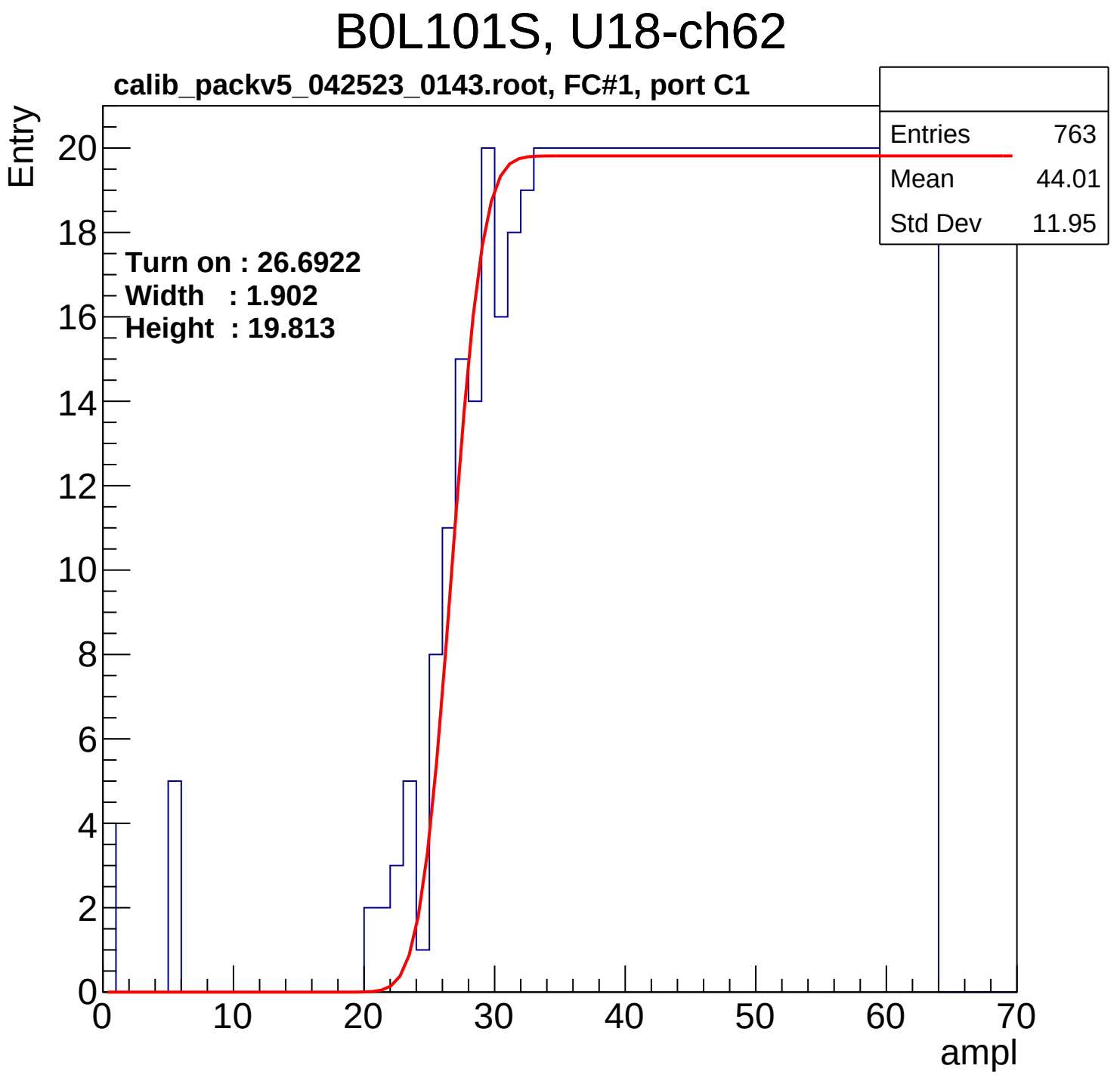
B0L101S, U18-ch62
calib_packv5_042523_0143.root, FC#1, port C1
Entries 763
Mean 44.01
Std Dev 11.95
Turn on : 26.6922
Width : 1.902
Height : 19.813
Entry
ampl
0
2
4
6
8
10
12
14
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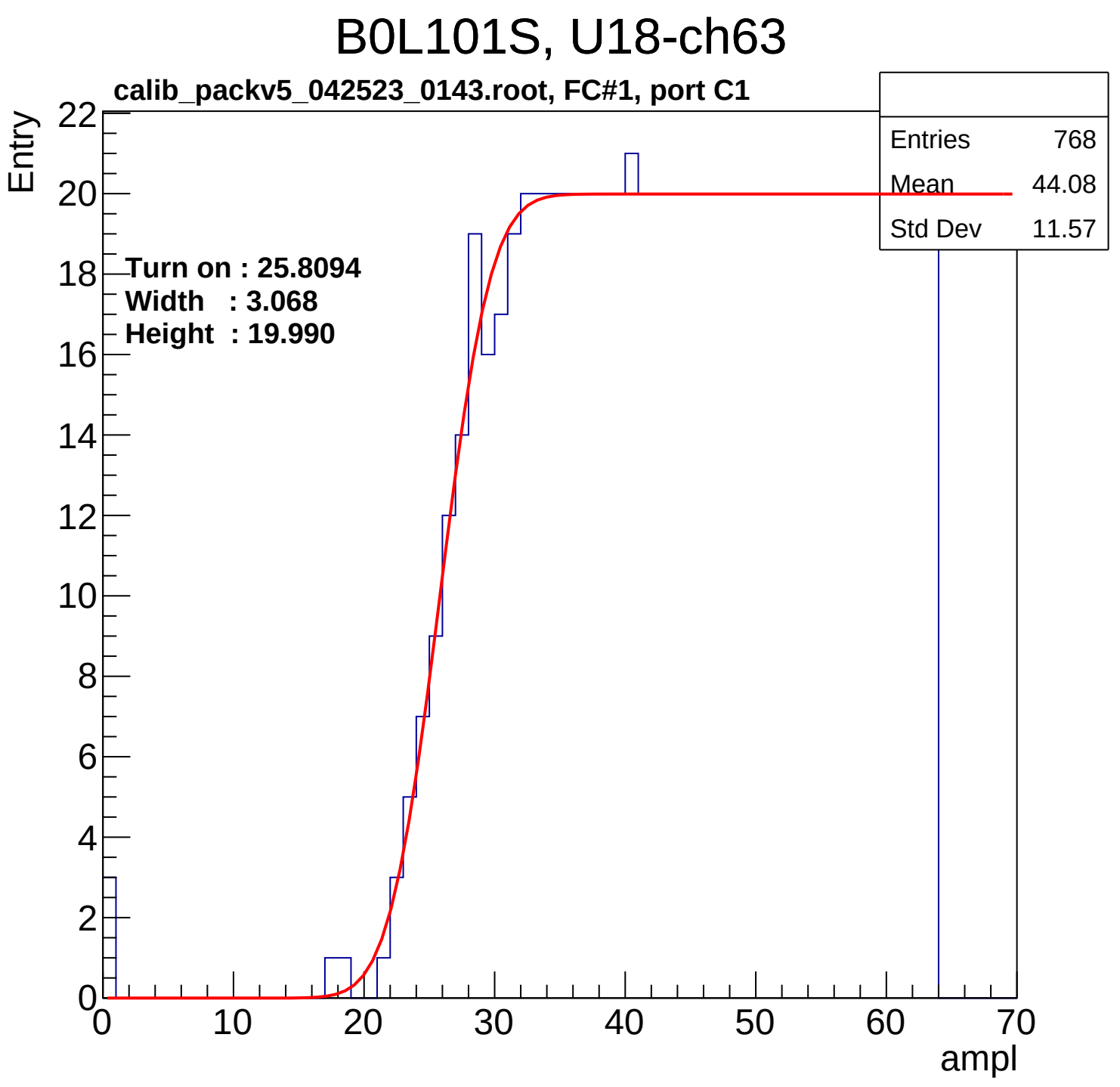
B0L101S, U18-ch63
calib_packv5_042523_0143.root, FC#1, port C1
Entries 768
Mean 44.08
Std Dev 11.57
Turn on : 25.8094
Width : 3.068
Height : 19.990
Entry
ampl
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6
8
10
12
14
16
18
20
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0
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40
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60
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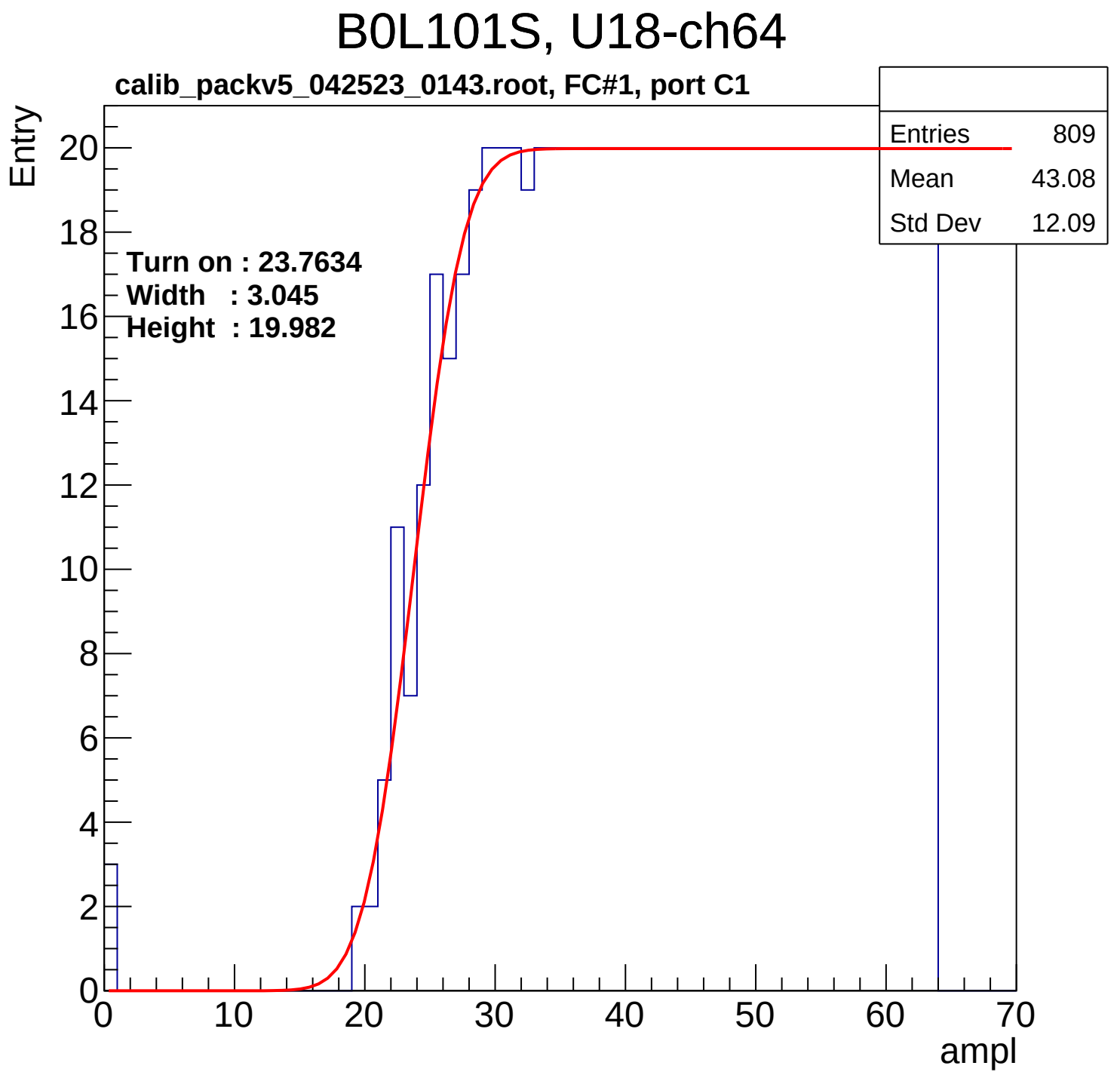
B0L101S, U18-ch64
calib_packv5_042523_0143.root, FC#1, port C1
Entries 809
Mean 43.08
Std Dev 12.09
Turn on : 23.7634
Width : 3.045
Height : 19.982
Entry
ampl
0
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6
8
10
12
14
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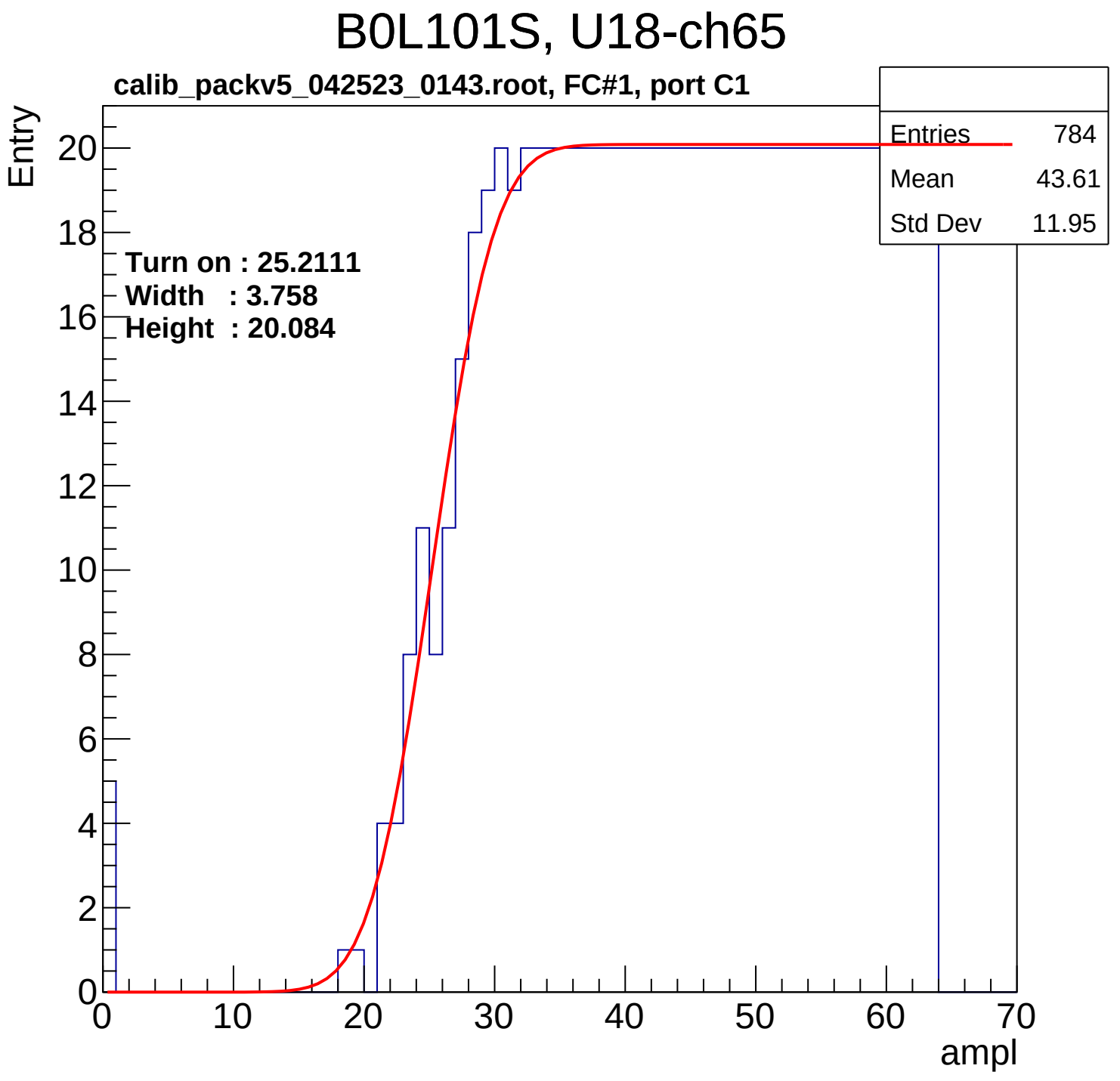
B0L101S, U18-ch65
calib_packv5_042523_0143.root, FC#1, port C1
Entries 784
Mean 43.61
Std Dev 11.95
Turn on : 25.2111
Width : 3.758
Height : 20.084
Entry
ampl
0
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6
8
10
12
14
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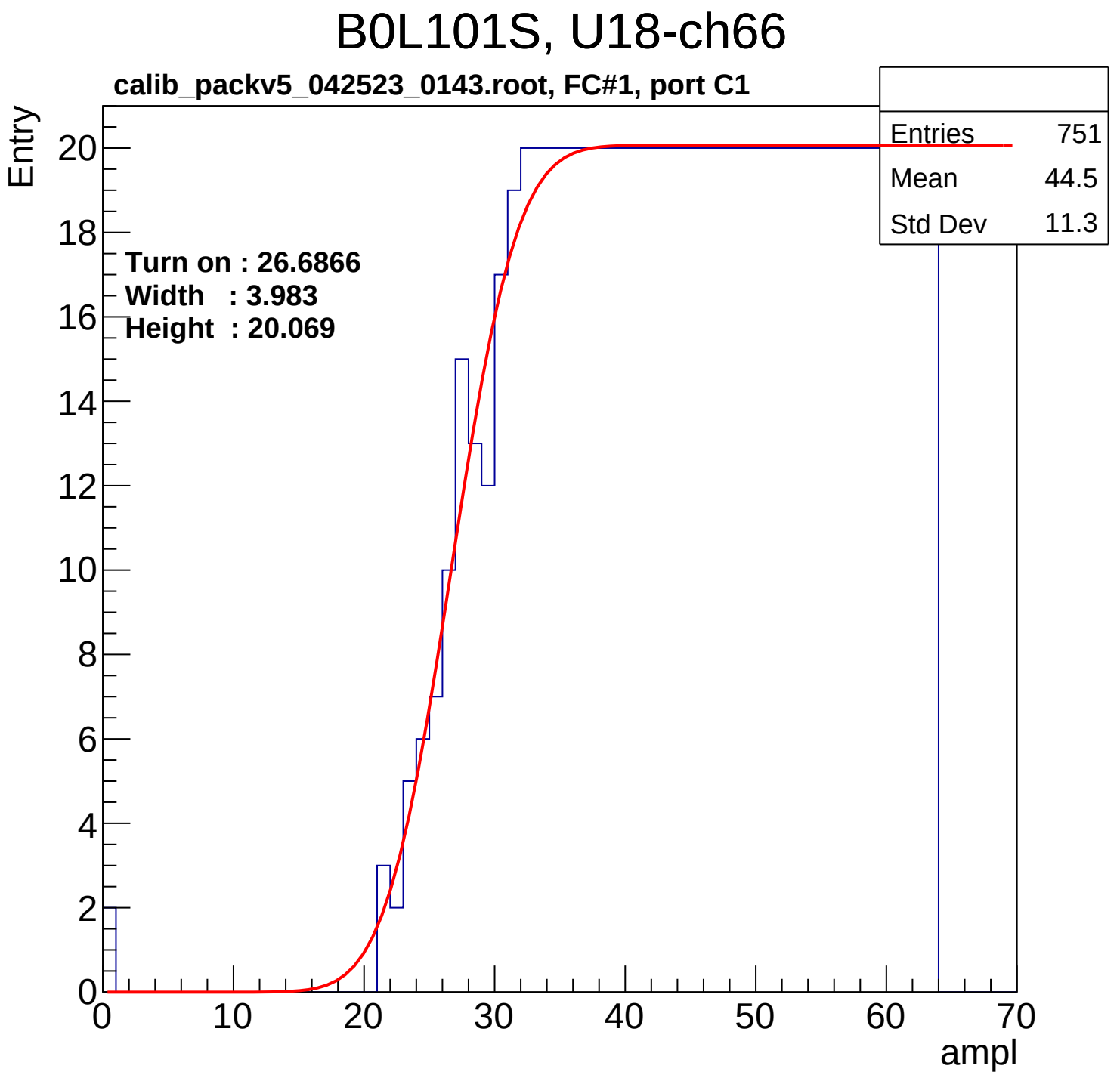
B0L101S, U18-ch66
calib_packv5_042523_0143.root, FC#1, port C1
Entries 751
Mean 44.5
Std Dev 11.3
Turn on : 26.6866
Width : 3.983
Height : 20.069
Entry
ampl
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4
6
8
10
12
14
16
18
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0
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20
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60
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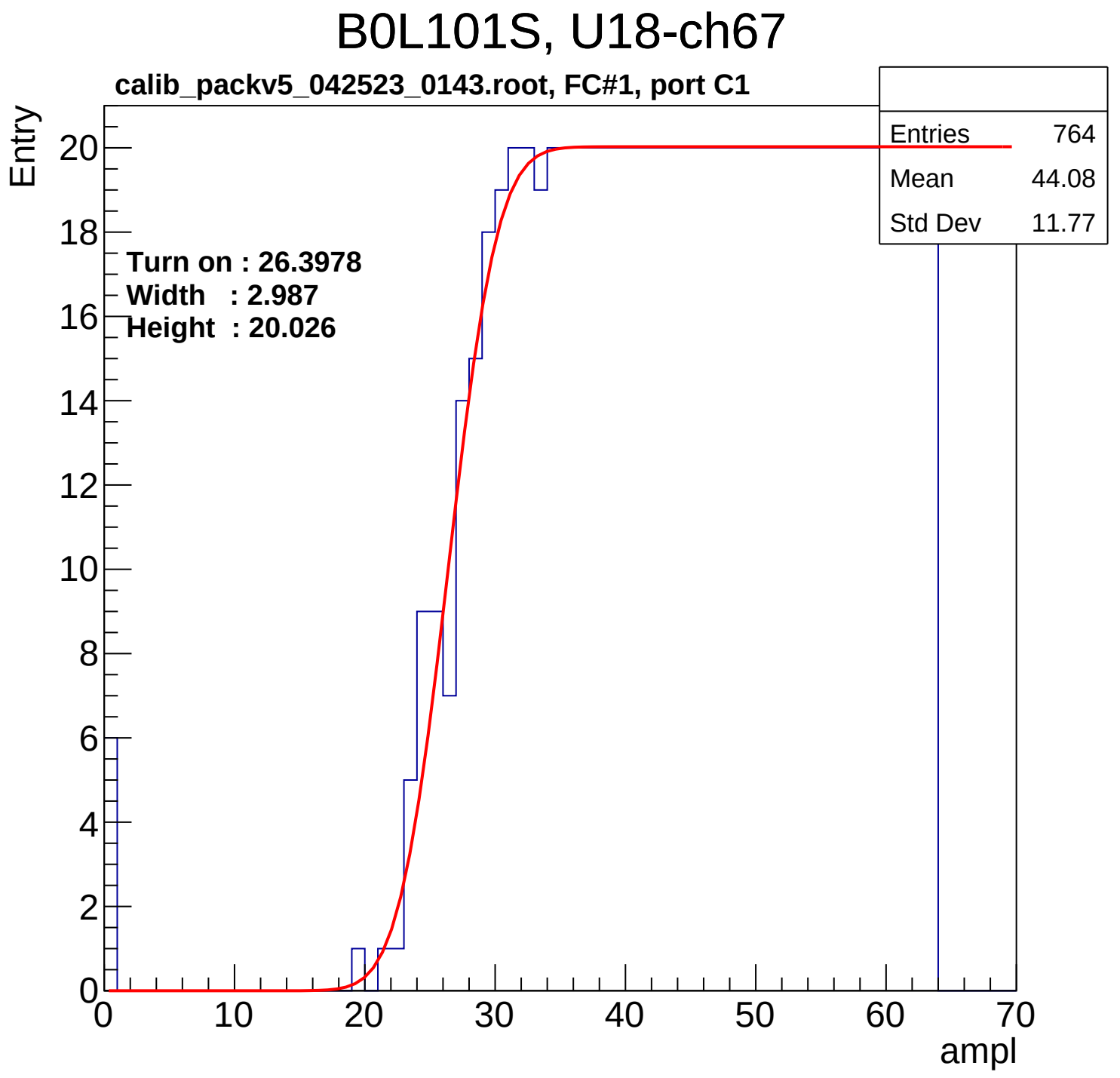
B0L101S, U18-ch67
calib_packv5_042523_0143.root, FC#1, port C1
Entries 764
Mean 44.08
Std Dev 11.77
Turn on : 26.3978
Width : 2.987
Height : 20.026
Entry
ampl
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6
8
10
12
14
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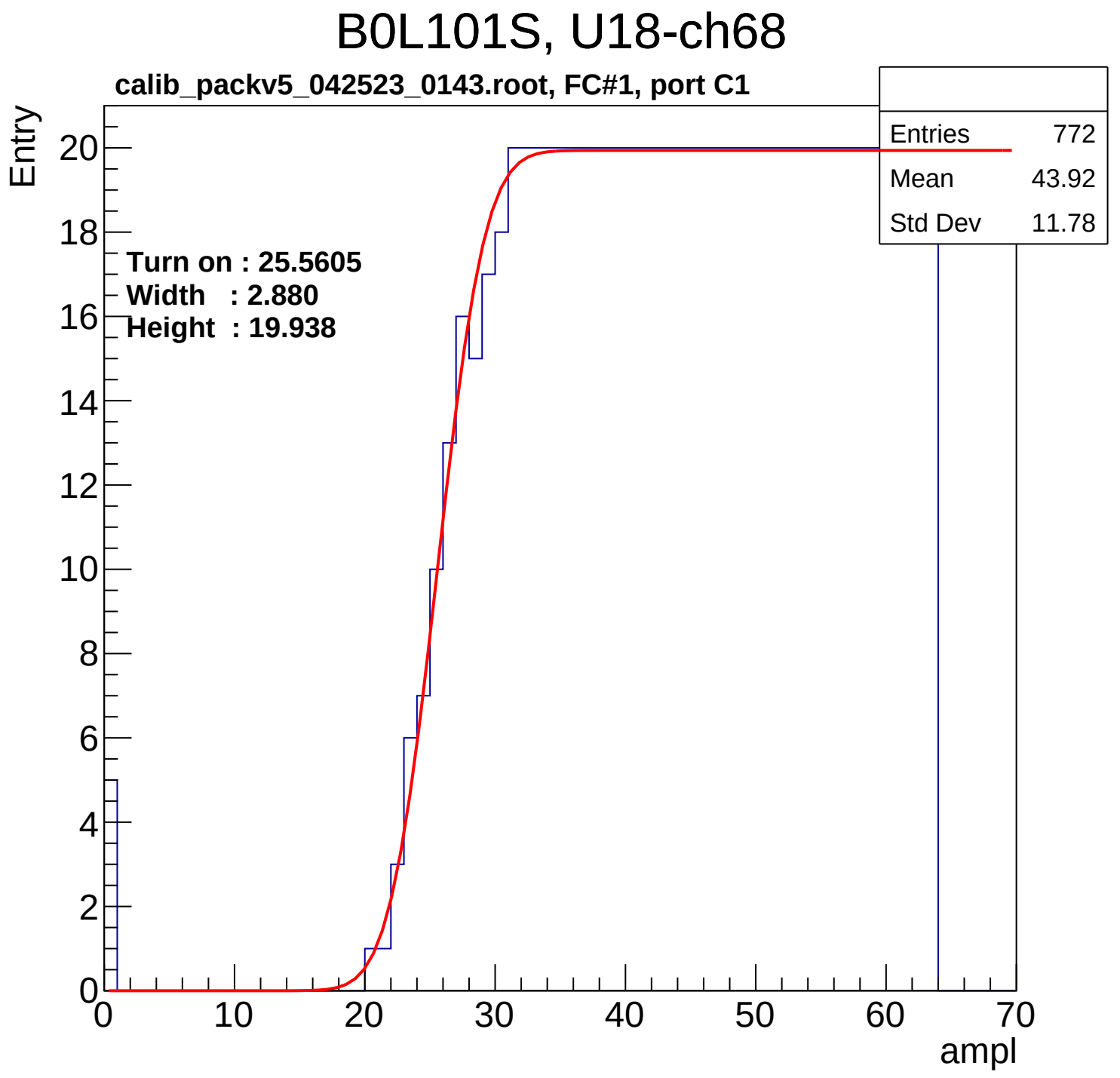
B0L101S, U18-ch68
calib_packv5_042523_0143.root, FC#1, port C1
Entries 772
Mean 43.92
Std Dev 11.78
Turn on : 25.5605
Width : 2.880
Height : 19.938
Entry
ampl
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6
8
10
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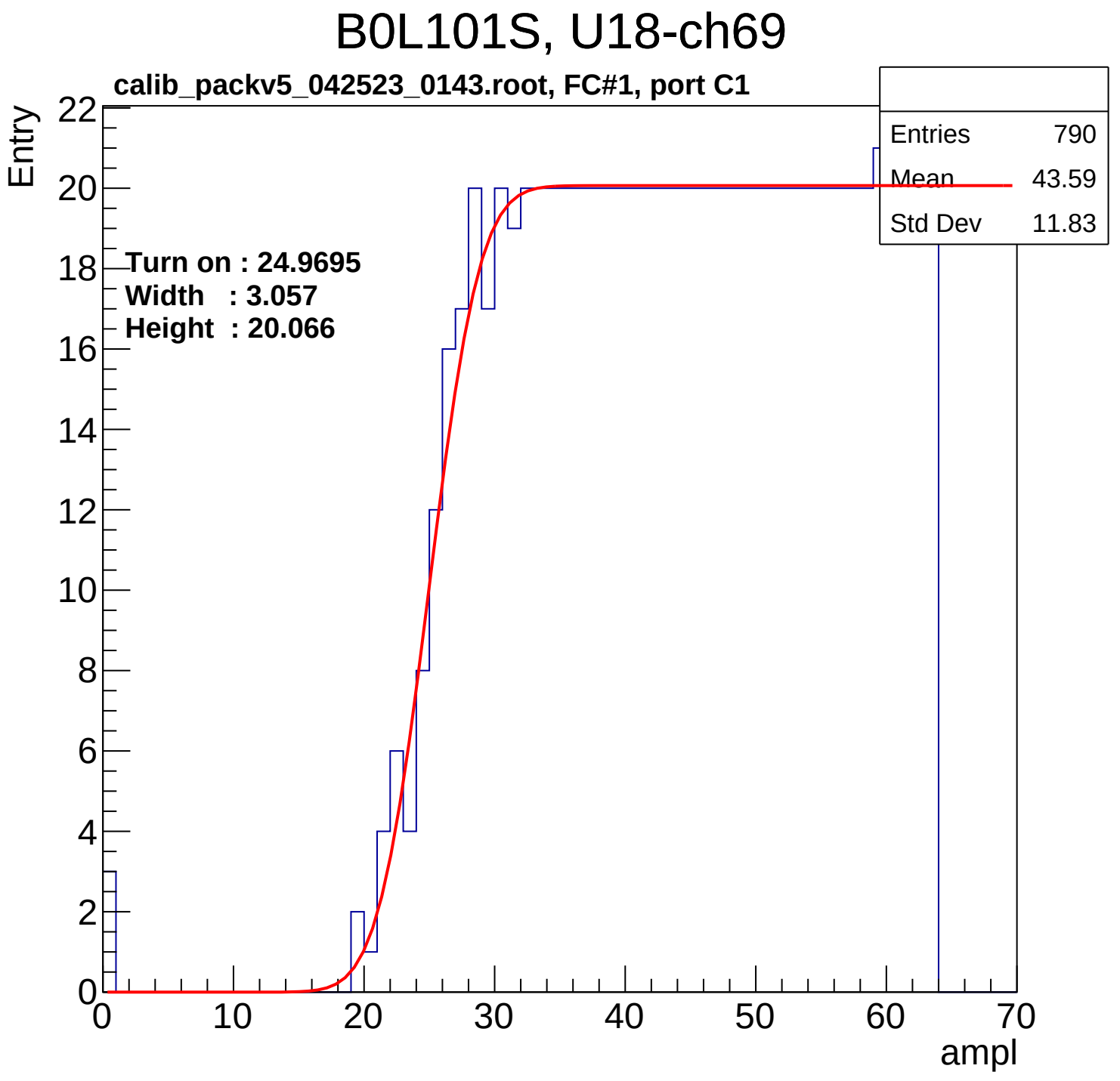
B0L101S, U18-ch69
calib_packv5_042523_0143.root, FC#1, port C1
Entries 790
Mean 43.59
Std Dev 11.83
Turn on : 24.9695
Width : 3.057
Height : 20.066
Entry
ampl
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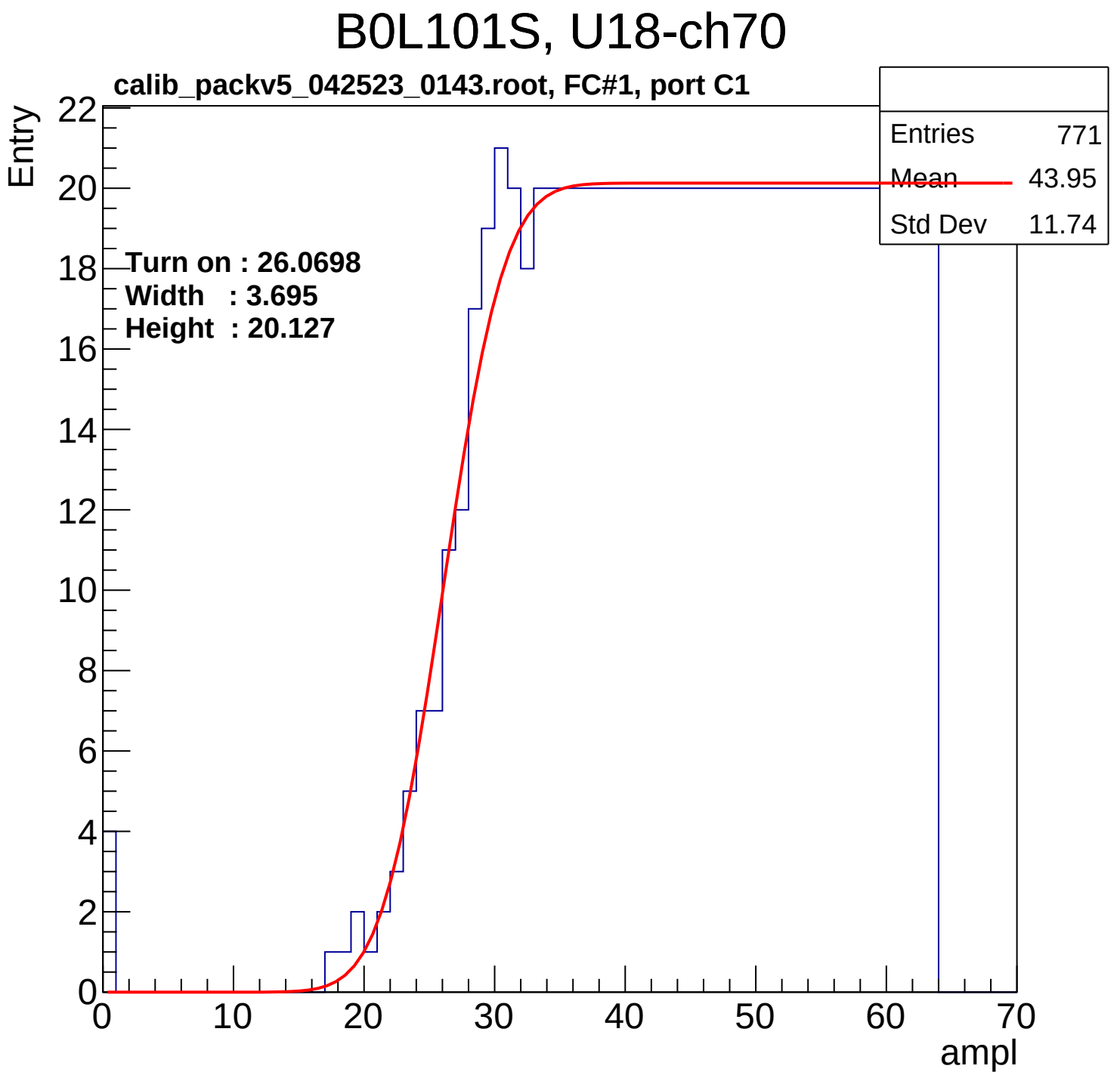
B0L101S, U18-ch70
calib_packv5_042523_0143.root, FC#1, port C1
Entries 771
Mean 43.95
Std Dev 11.74
Turn on : 26.0698
Width : 3.695
Height : 20.127
Entry
ampl
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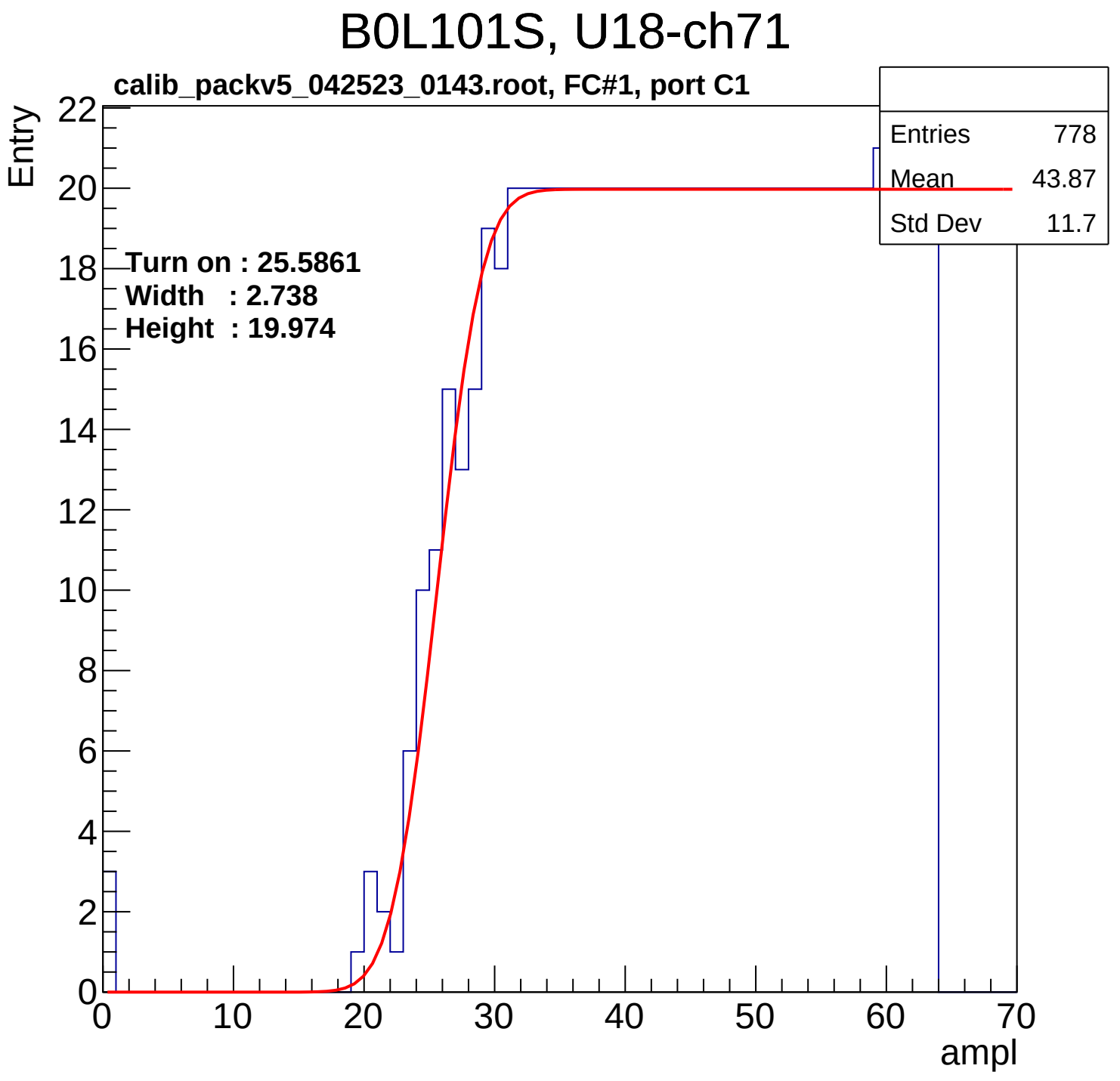
B0L101S, U18-ch71
calib_packv5_042523_0143.root, FC#1, port C1
Entries 778
Mean 43.87
Std Dev 11.7
Turn on : 25.5861
Width : 2.738
Height : 19.974
Entry
ampl
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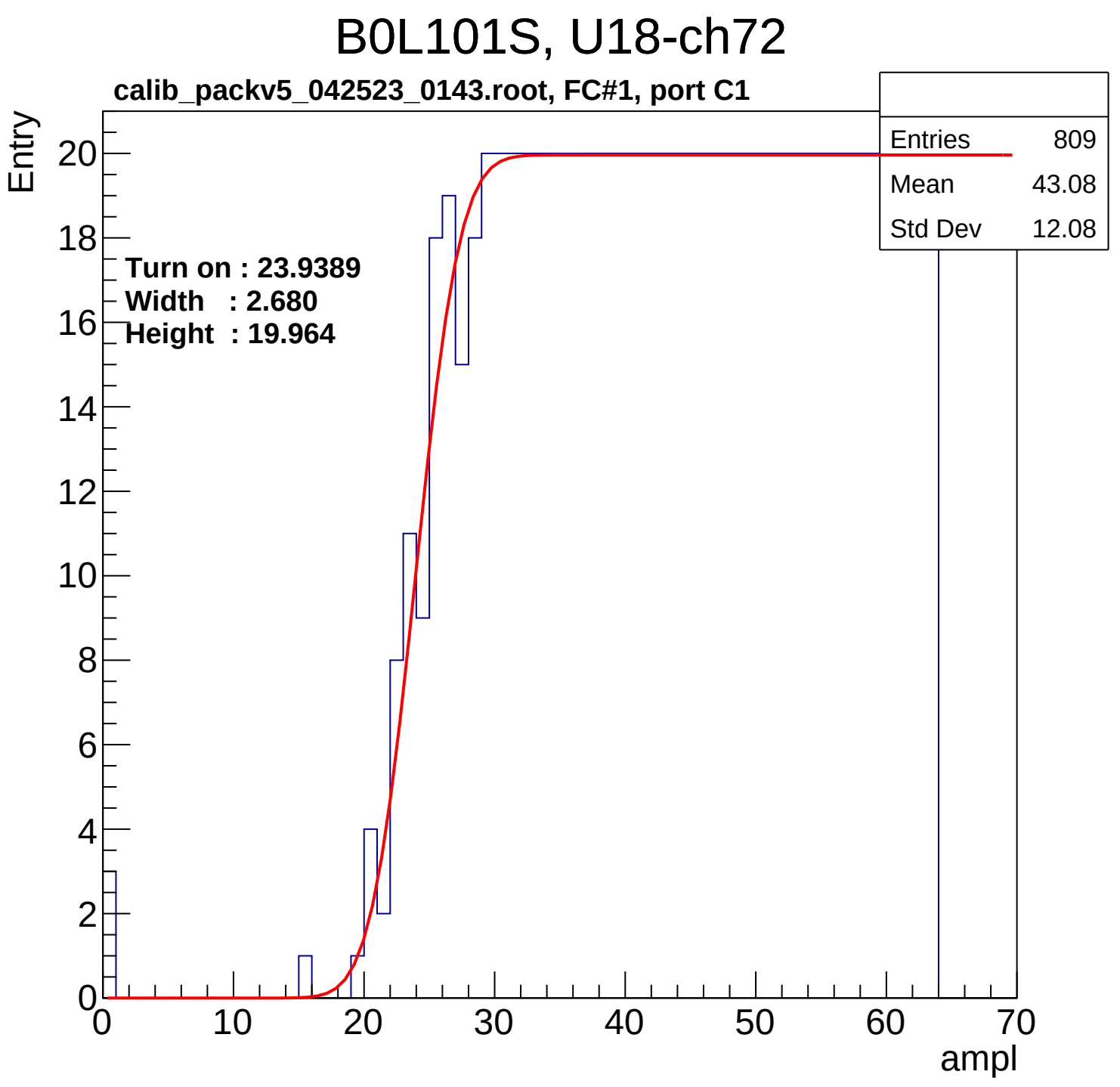
B0L101S, U18-ch72
calib_packv5_042523_0143.root, FC#1, port C1
Entries 809
Mean 43.08
Std Dev 12.08
Turn on : 23.9389
Width : 2.680
Height : 19.964
Entry
ampl
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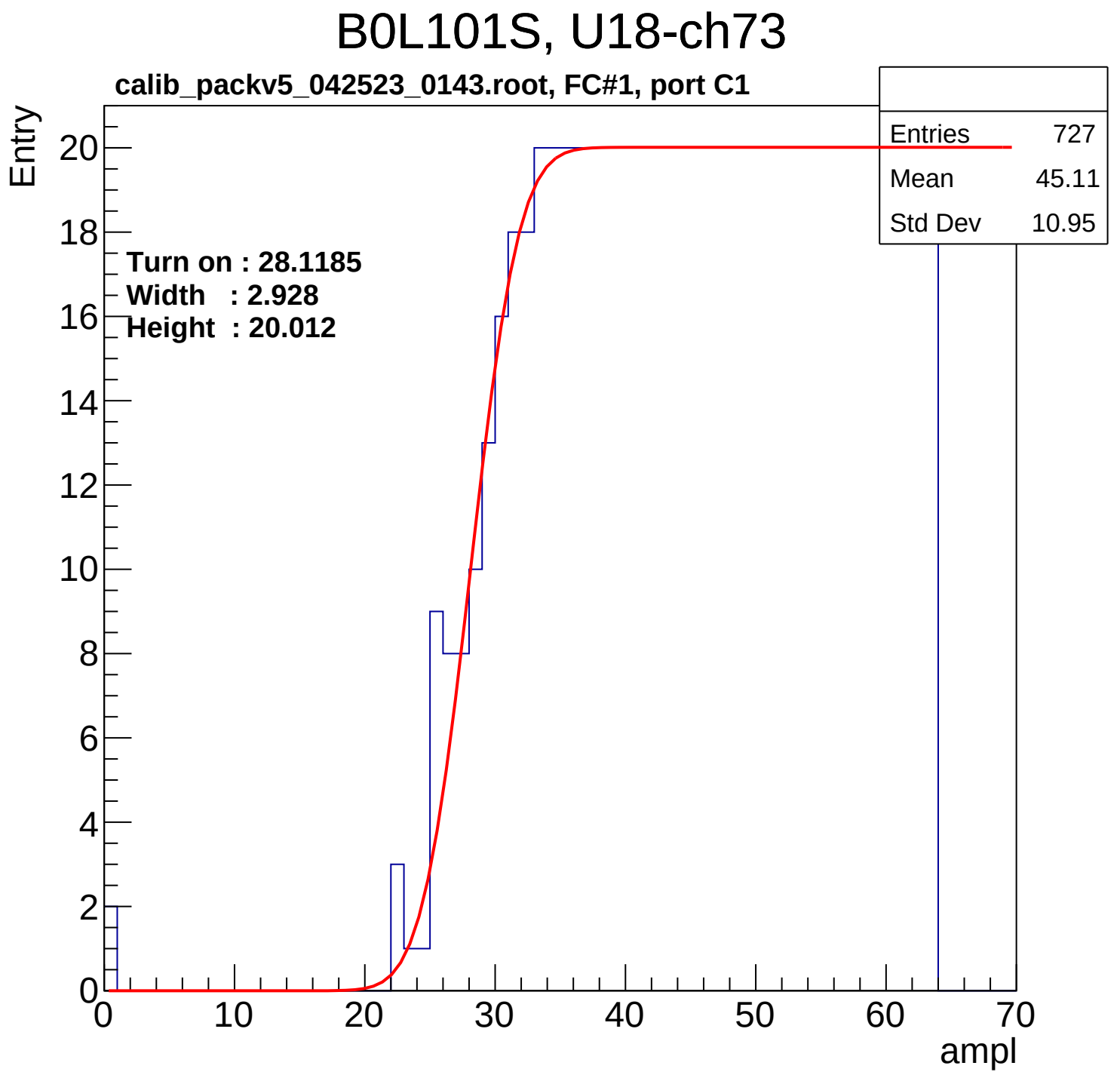
B0L101S, U18-ch73
calib_packv5_042523_0143.root, FC#1, port C1
Entries 727
Mean 45.11
Std Dev 10.95
Turn on : 28.1185
Width : 2.928
Height : 20.012
Entry
ampl
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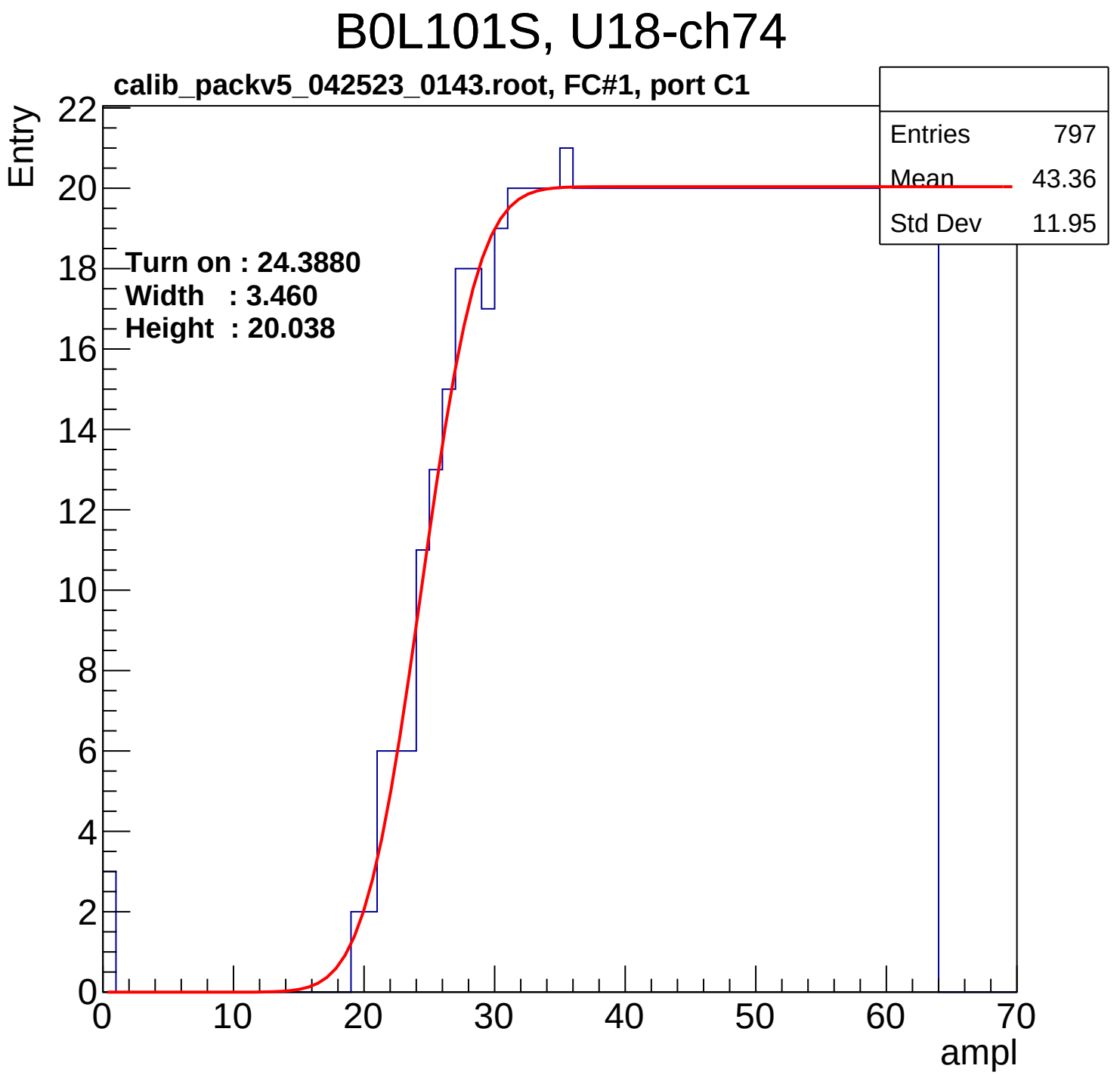
B0L101S, U18-ch74
calib_packv5_042523_0143.root, FC#1, port C1
Entries 797
Mean 43.36
Std Dev 11.95
Turn on : 24.3880
Width : 3.460
Height : 20.038
Entry
ampl
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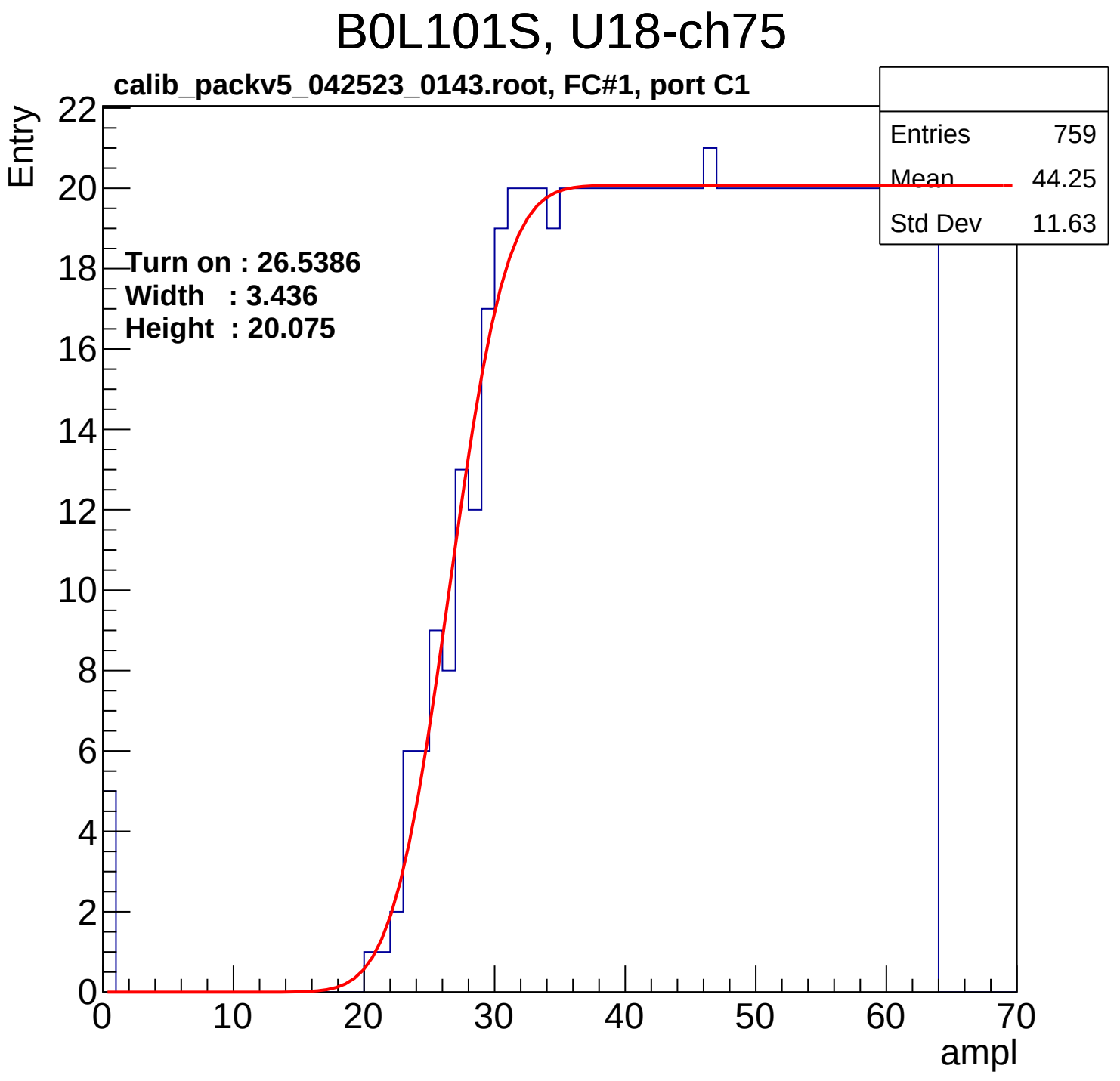
B0L101S, U18-ch75
calib_packv5_042523_0143.root, FC#1, port C1
Entries 759
Mean 44.25
Std Dev 11.63
Turn on : 26.5386
Width : 3.436
Height : 20.075
Entry
ampl
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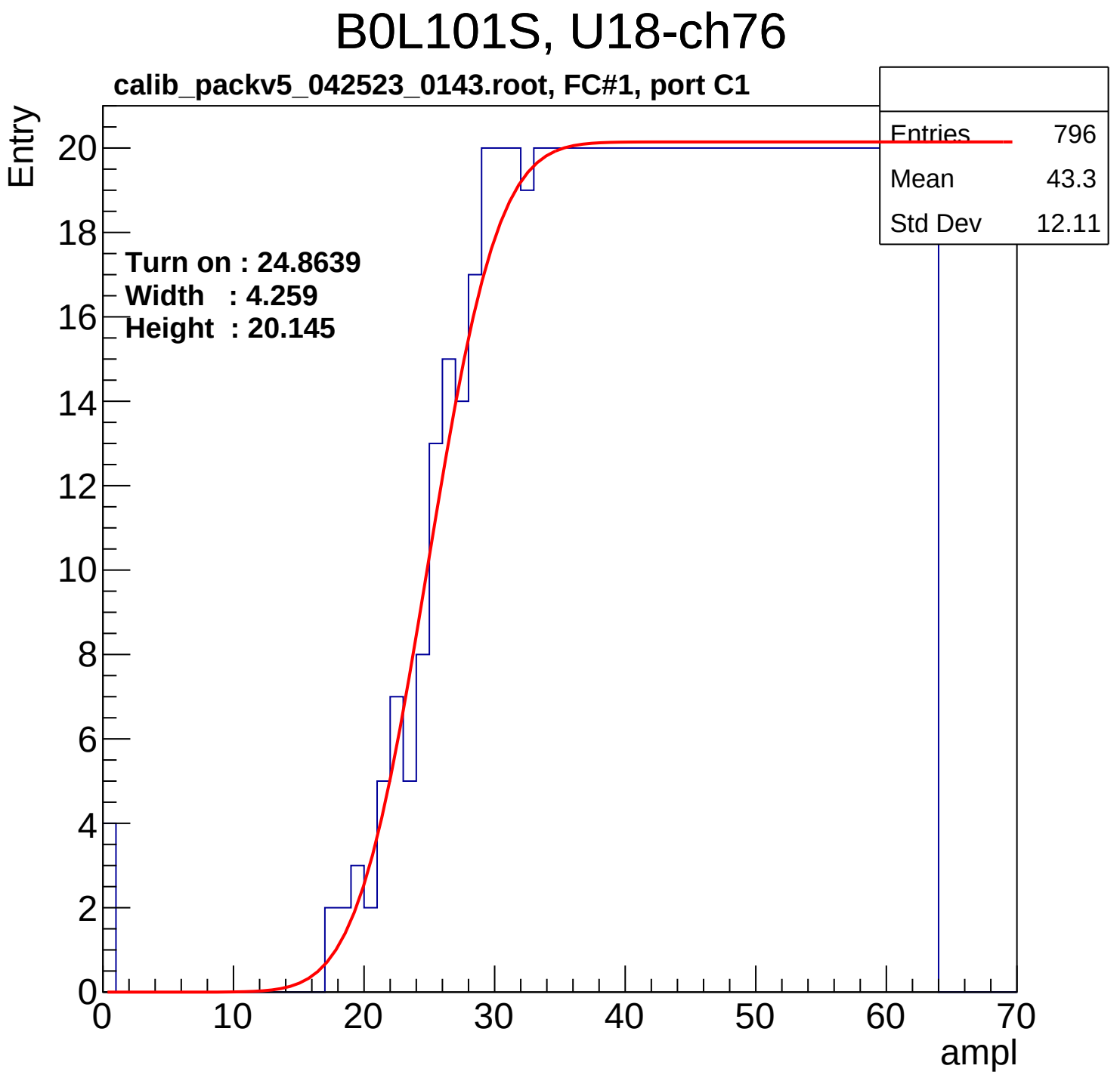
B0L101S, U18-ch76
calib_packv5_042523_0143.root, FC#1, port C1
Entries 796
Mean 43.3
Std Dev 12.11
Turn on : 24.8639
Width : 4.259
Height : 20.145
Entry
ampl
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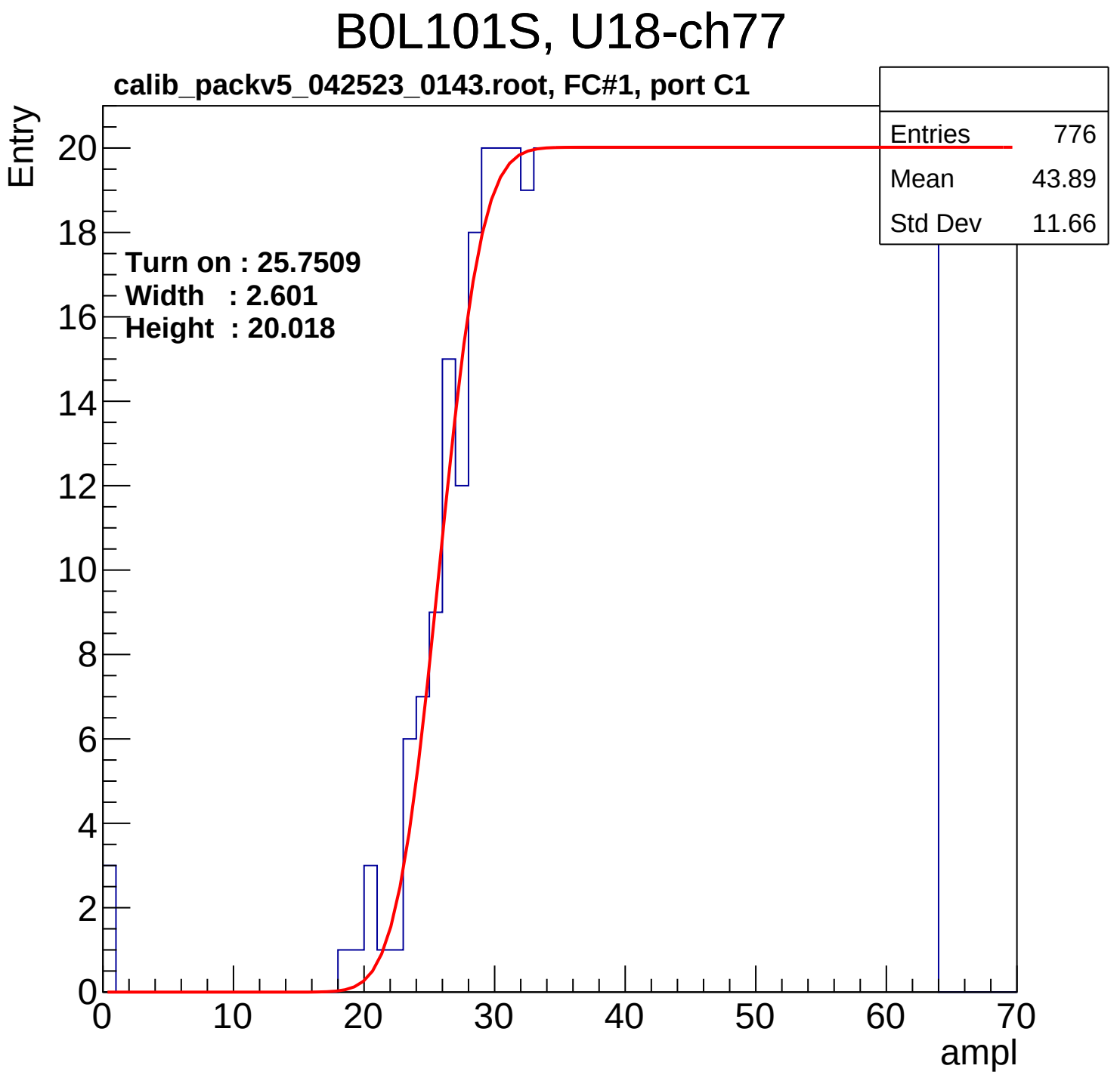
B0L101S, U18-ch77
calib_packv5_042523_0143.root, FC#1, port C1
Entries 776
Mean 43.89
Std Dev 11.66
Turn on : 25.7509
Width : 2.601
Height : 20.018
Entry
ampl
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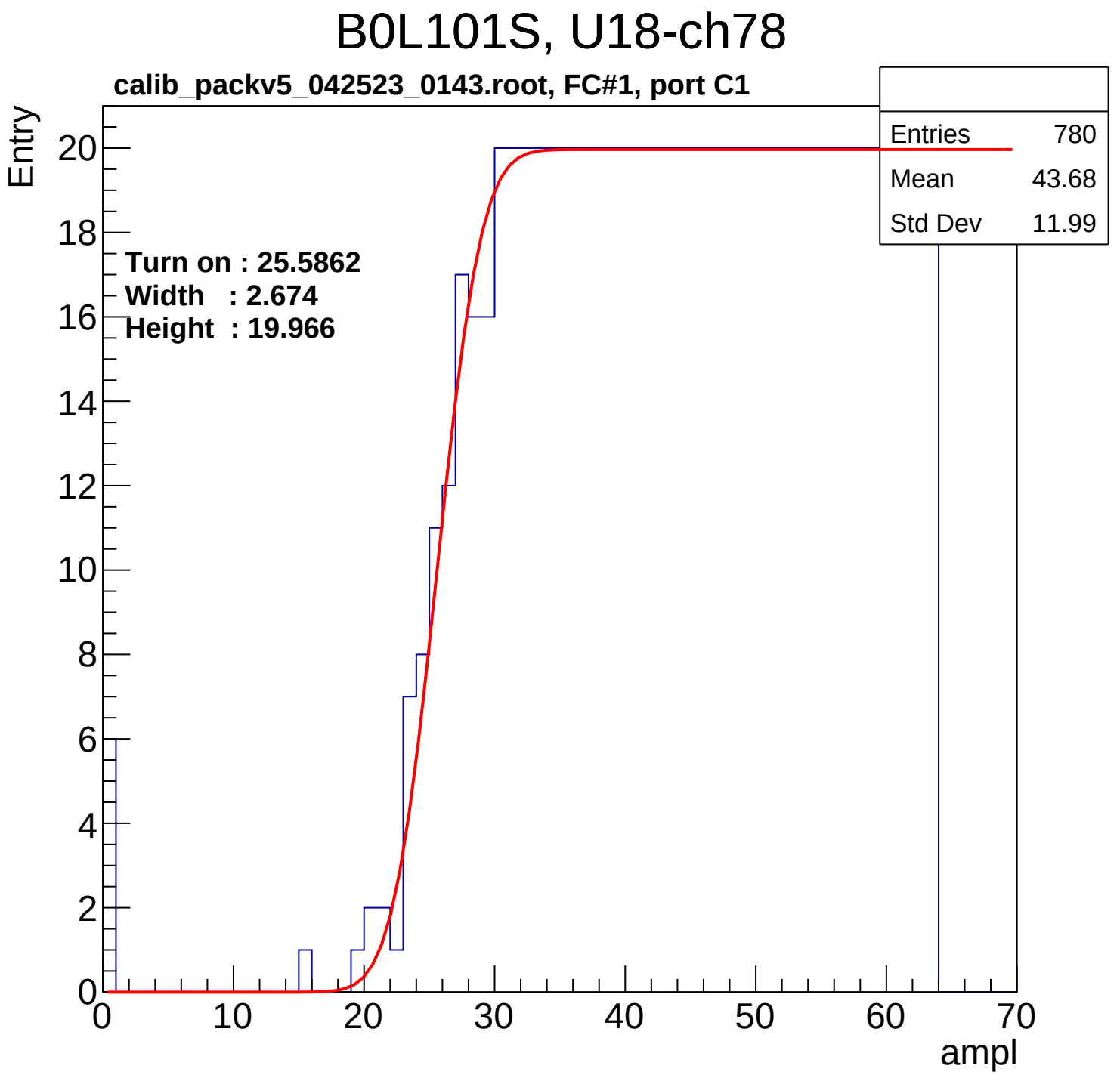
B0L101S, U18-ch78
calib_packv5_042523_0143.root, FC#1, port C1
Entries 780
Mean 43.68
Std Dev 11.99
Turn on : 25.5862
Width : 2.674
Height : 19.966
Entry
ampl
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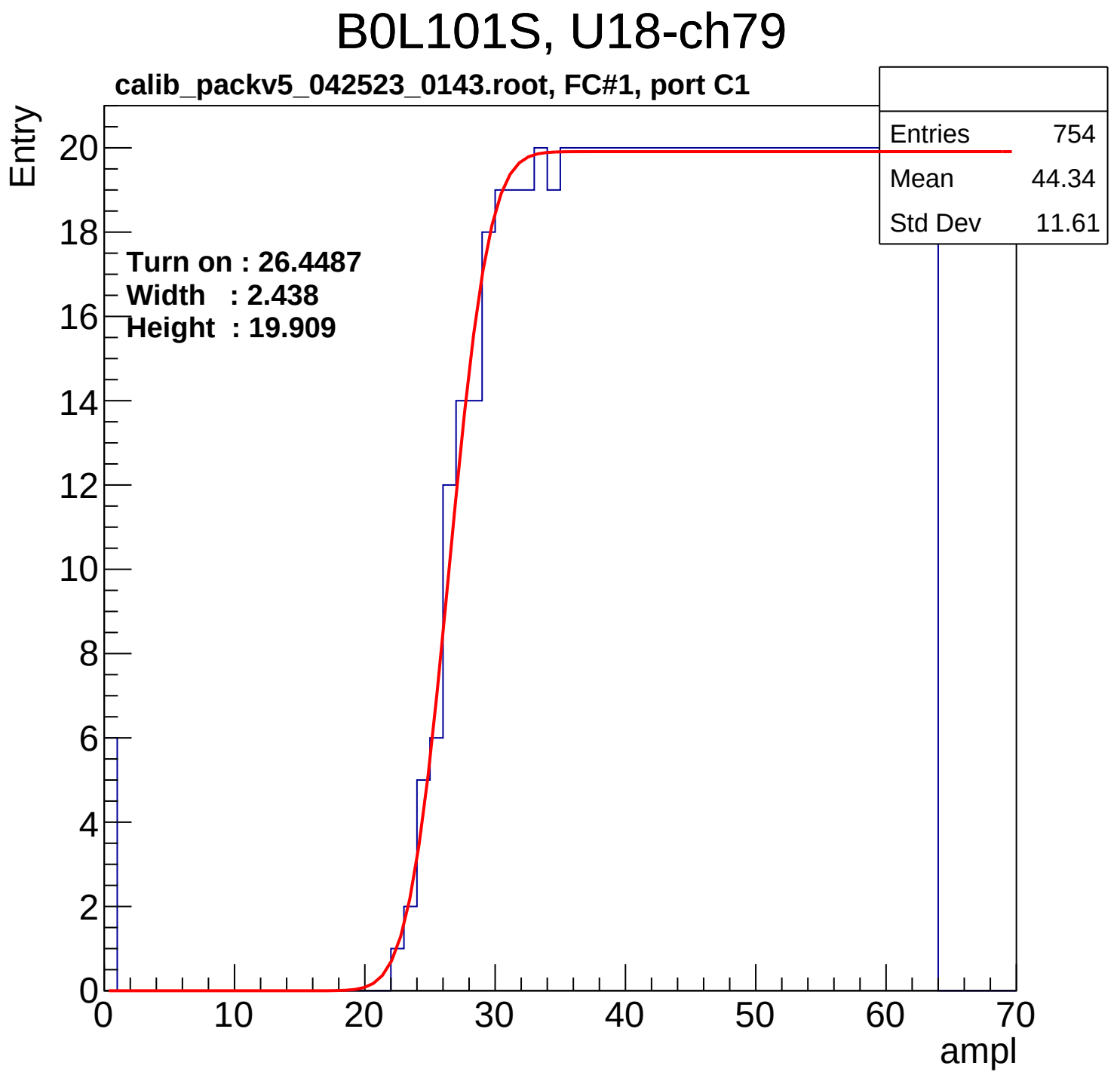
B0L101S, U18-ch79
calib_packv5_042523_0143.root, FC#1, port C1
Entries 754
Mean 44.34
Std Dev 11.61
Turn on : 26.4487
Width : 2.438
Height : 19.909
Entry
ampl
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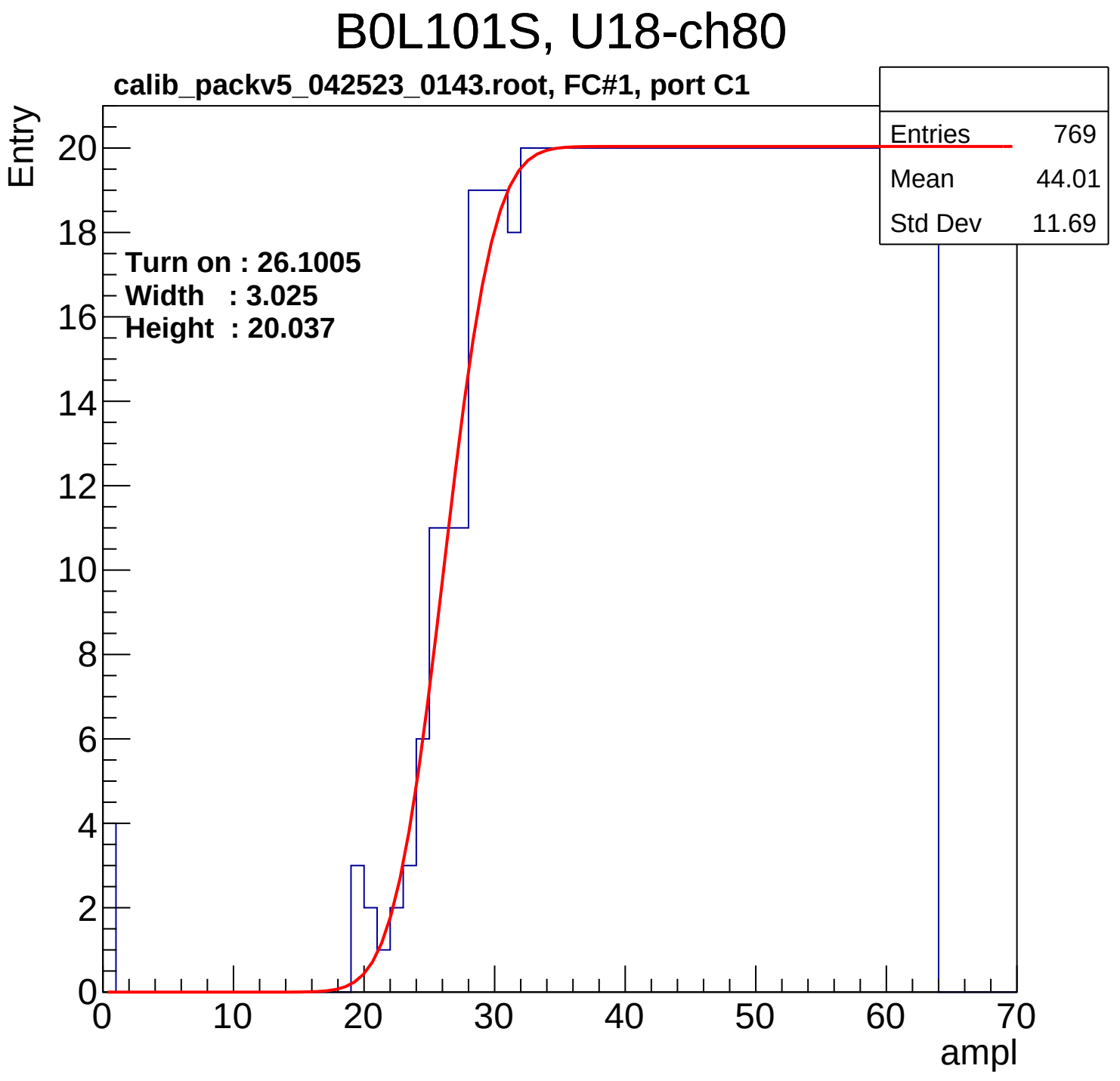
B0L101S, U18-ch80
calib_packv5_042523_0143.root, FC#1, port C1
Entries 769
Mean 44.01
Std Dev 11.69
Turn on : 26.1005
Width : 3.025
Height : 20.037
Entry
ampl
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6
8
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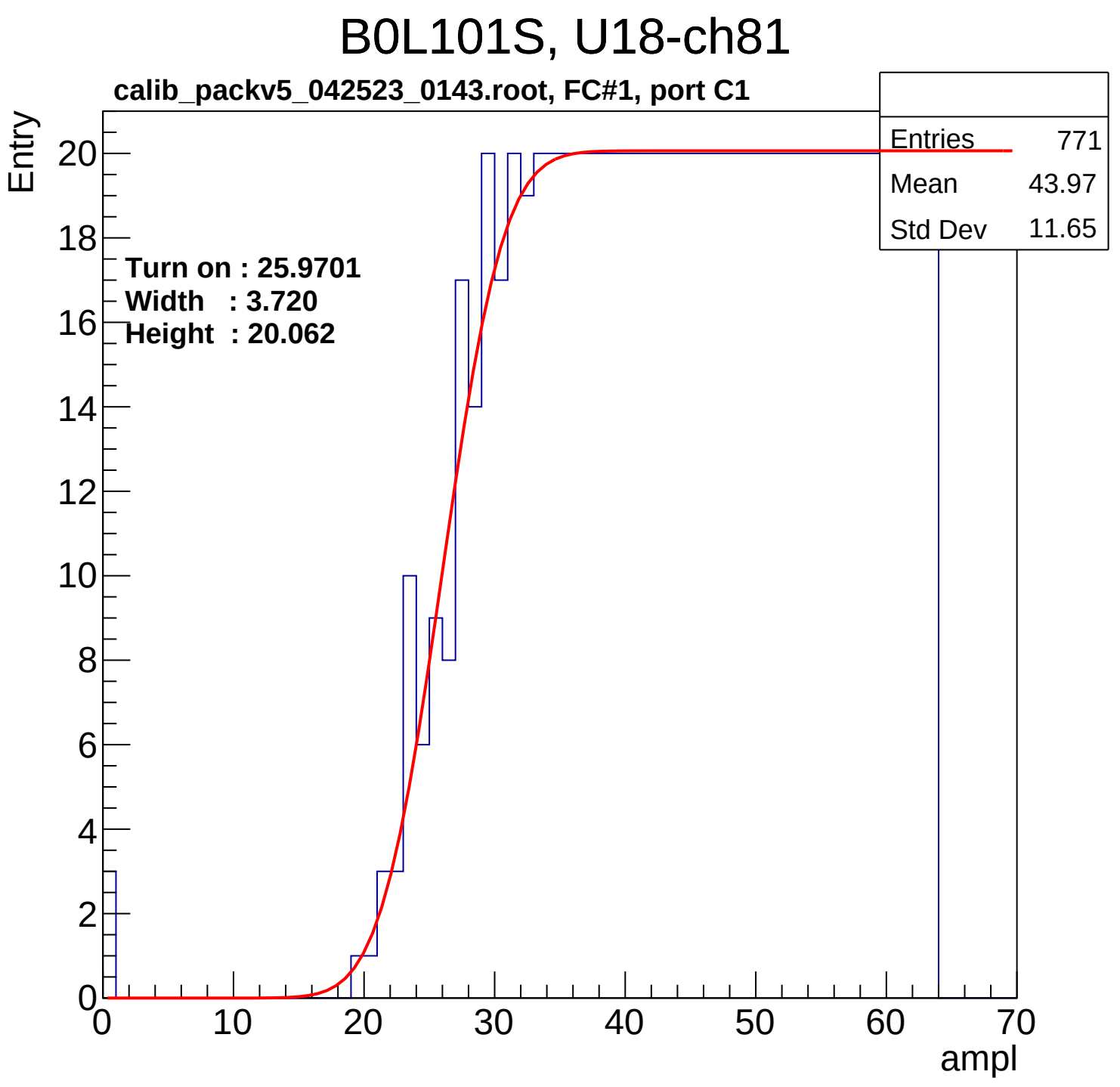
B0L101S, U18-ch81
calib_packv5_042523_0143.root, FC#1, port C1
Entries 771
Mean 43.97
Std Dev 11.65
Turn on : 25.9701
Width : 3.720
Height : 20.062
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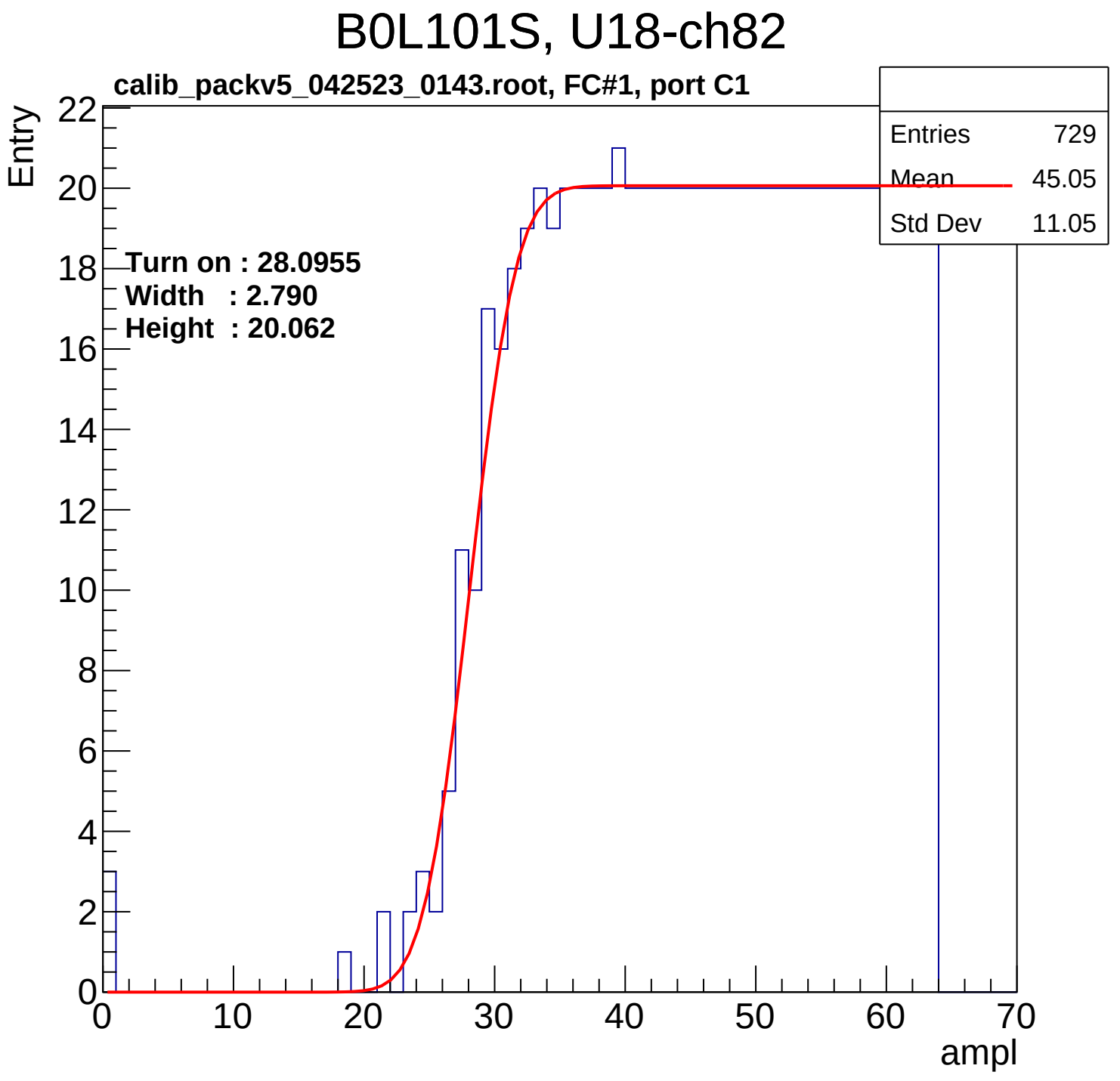
B0L101S, U18-ch82
calib_packv5_042523_0143.root, FC#1, port C1
Entries 729
Mean 45.05
Std Dev 11.05
Turn on : 28.0955
Width : 2.790
Height : 20.062
Entry
ampl
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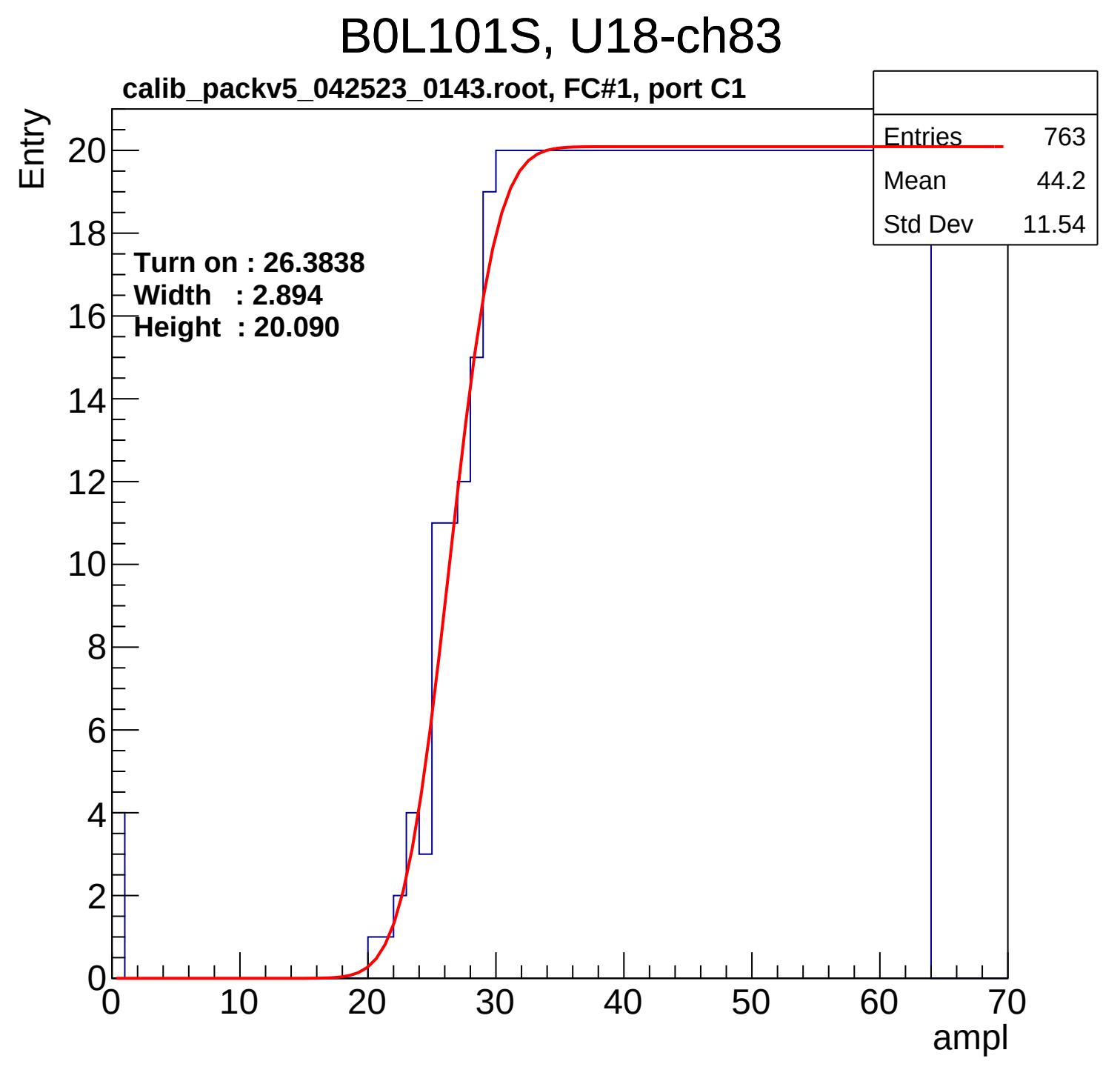
B0L101S, U18-ch83
calib_packv5_042523_0143.root, FC#1, port C1
Entries 763
Mean 44.2
Std Dev 11.54
Turn on : 26.3838
Width : 2.894
Height : 20.090
Entry
ampl
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2
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6
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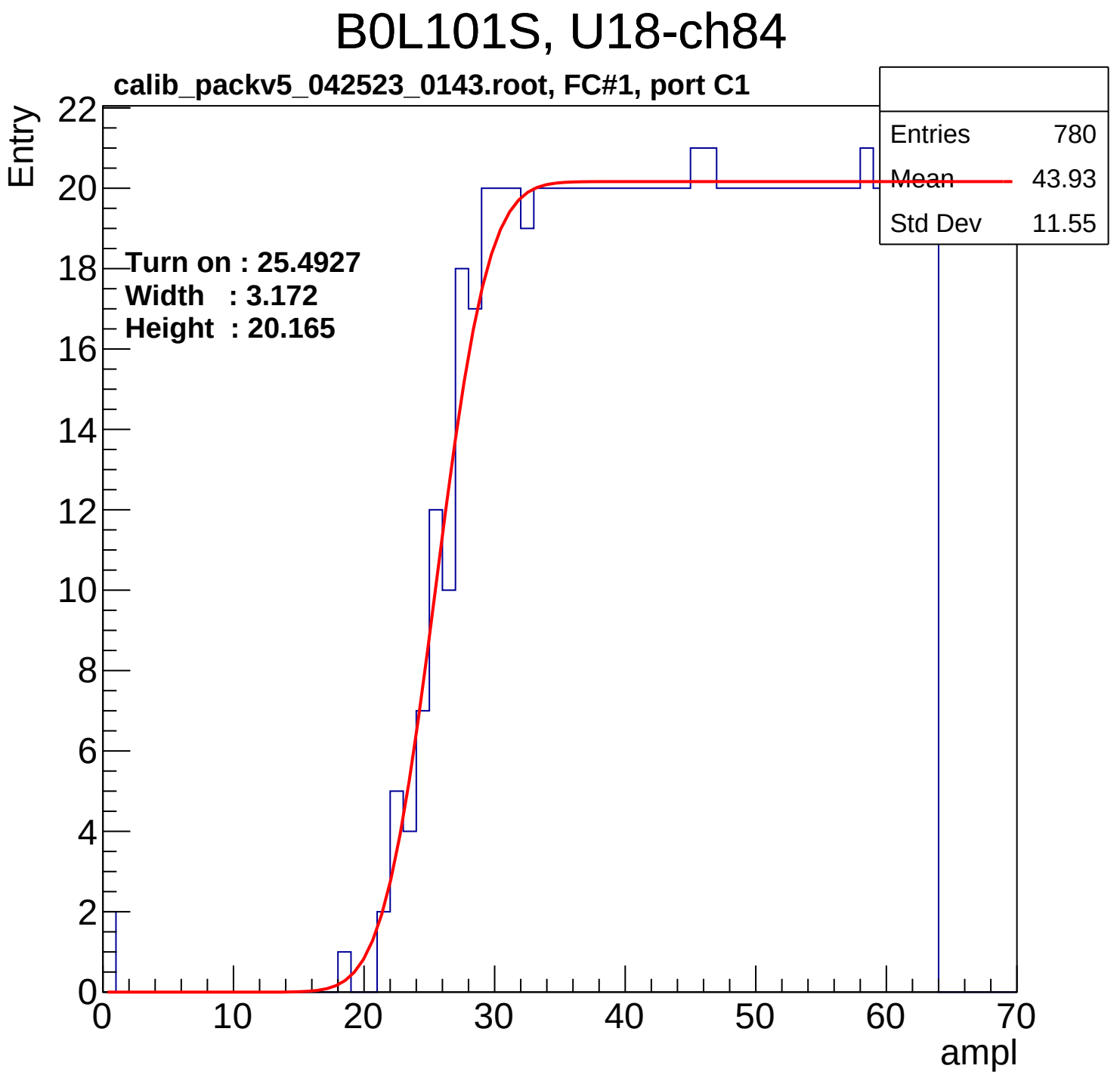
B0L101S, U18-ch84
calib_packv5_042523_0143.root, FC#1, port C1
Entries 780
Mean 43.93
Std Dev 11.55
Turn on : 25.4927
Width : 3.172
Height : 20.165
Entry
ampl
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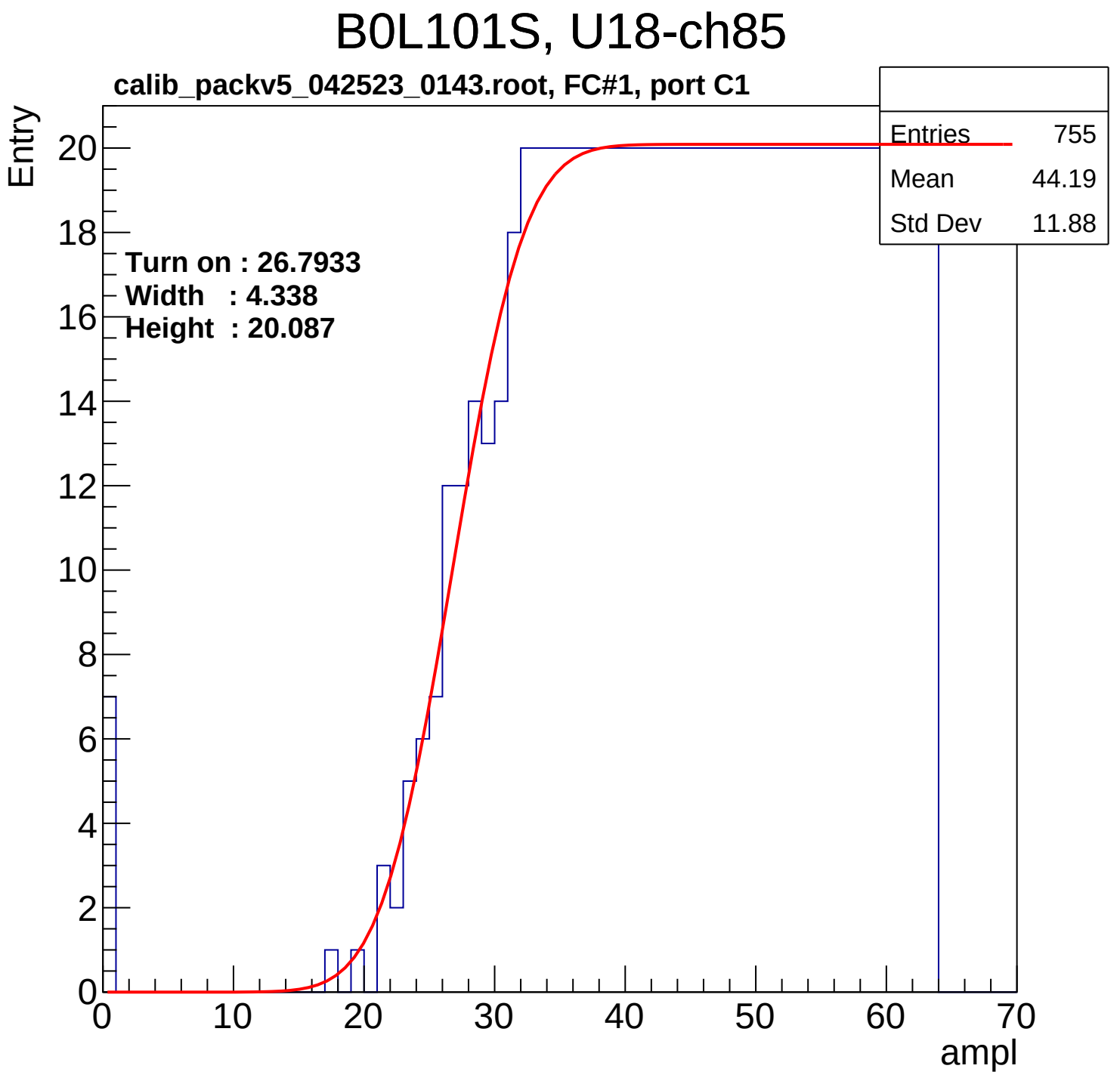
B0L101S, U18-ch85
calib_packv5_042523_0143.root, FC#1, port C1
Entries 755
Mean 44.19
Std Dev 11.88
Turn on : 26.7933
Width : 4.338
Height : 20.087
Entry
ampl
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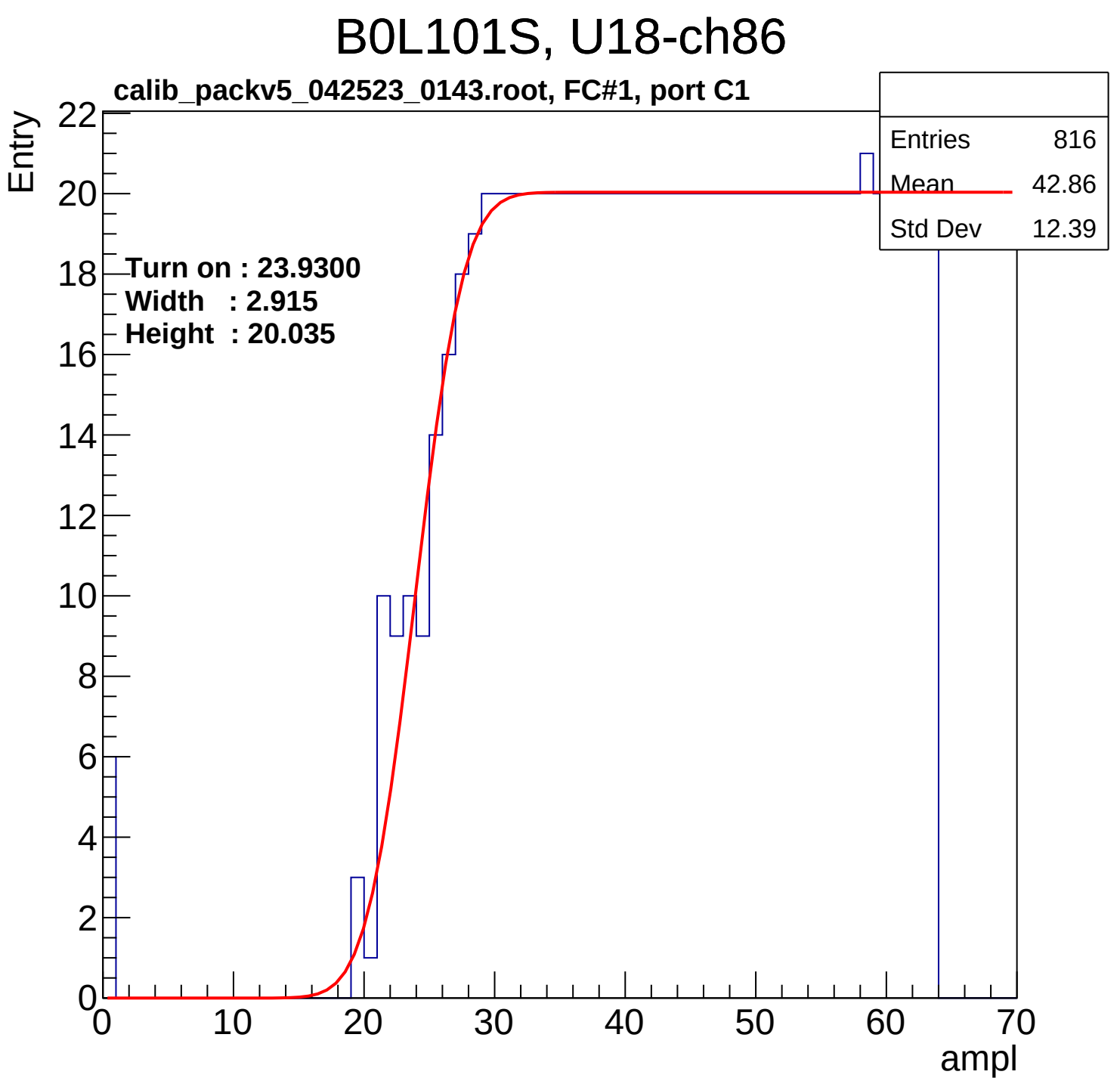
B0L101S, U18-ch86
calib_packv5_042523_0143.root, FC#1, port C1
Entries 816
Mean 42.86
Std Dev 12.39
Turn on : 23.9300
Width : 2.915
Height : 20.035
Entry
ampl
0
2
4
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8
10
12
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16
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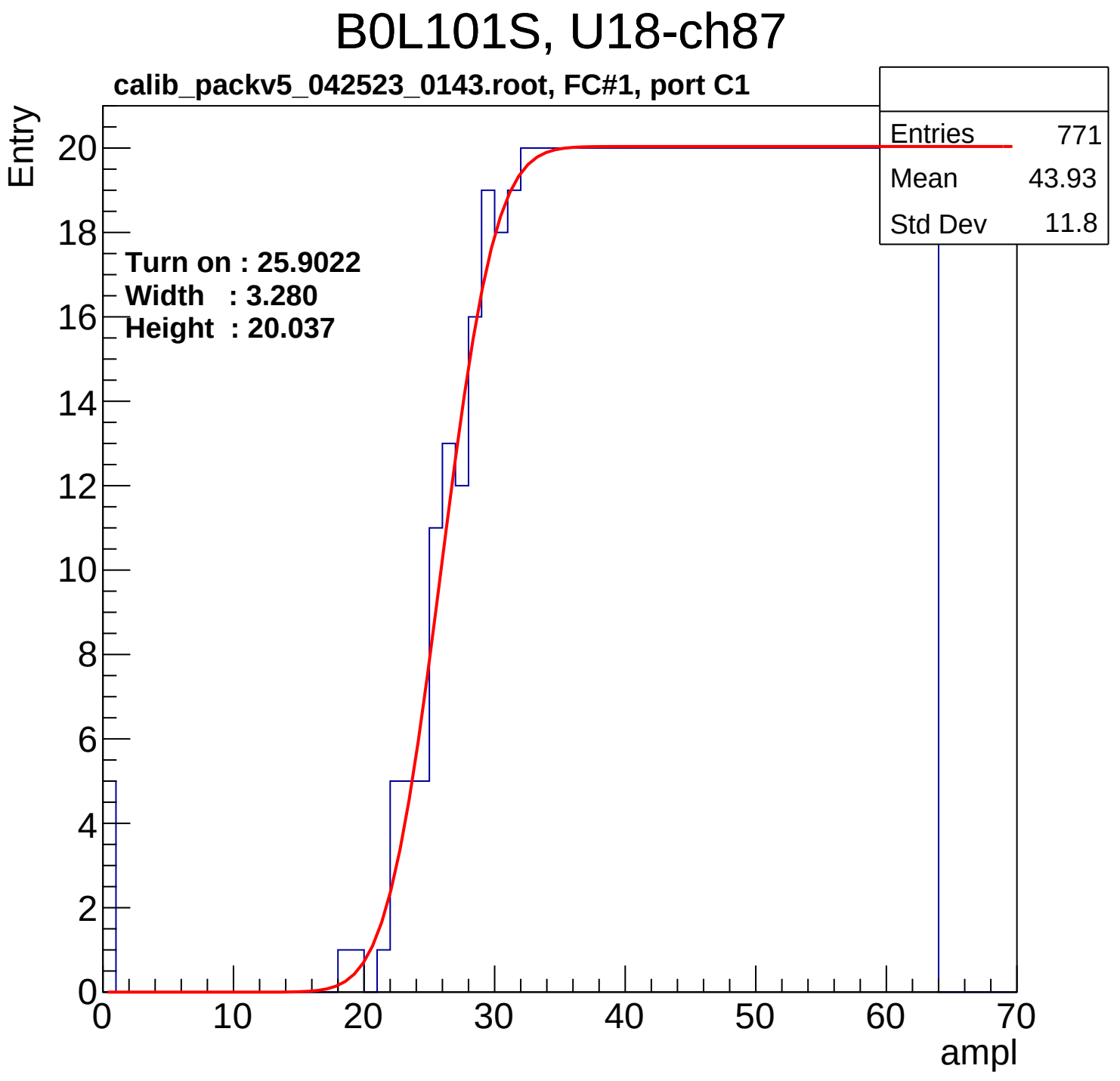
B0L101S, U18-ch87
calib_packv5_042523_0143.root, FC#1, port C1
Entries 771
Mean 43.93
Std Dev 11.8
Turn on : 25.9022
Width : 3.280
Height : 20.037
Entry
ampl
0
2
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6
8
10
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14
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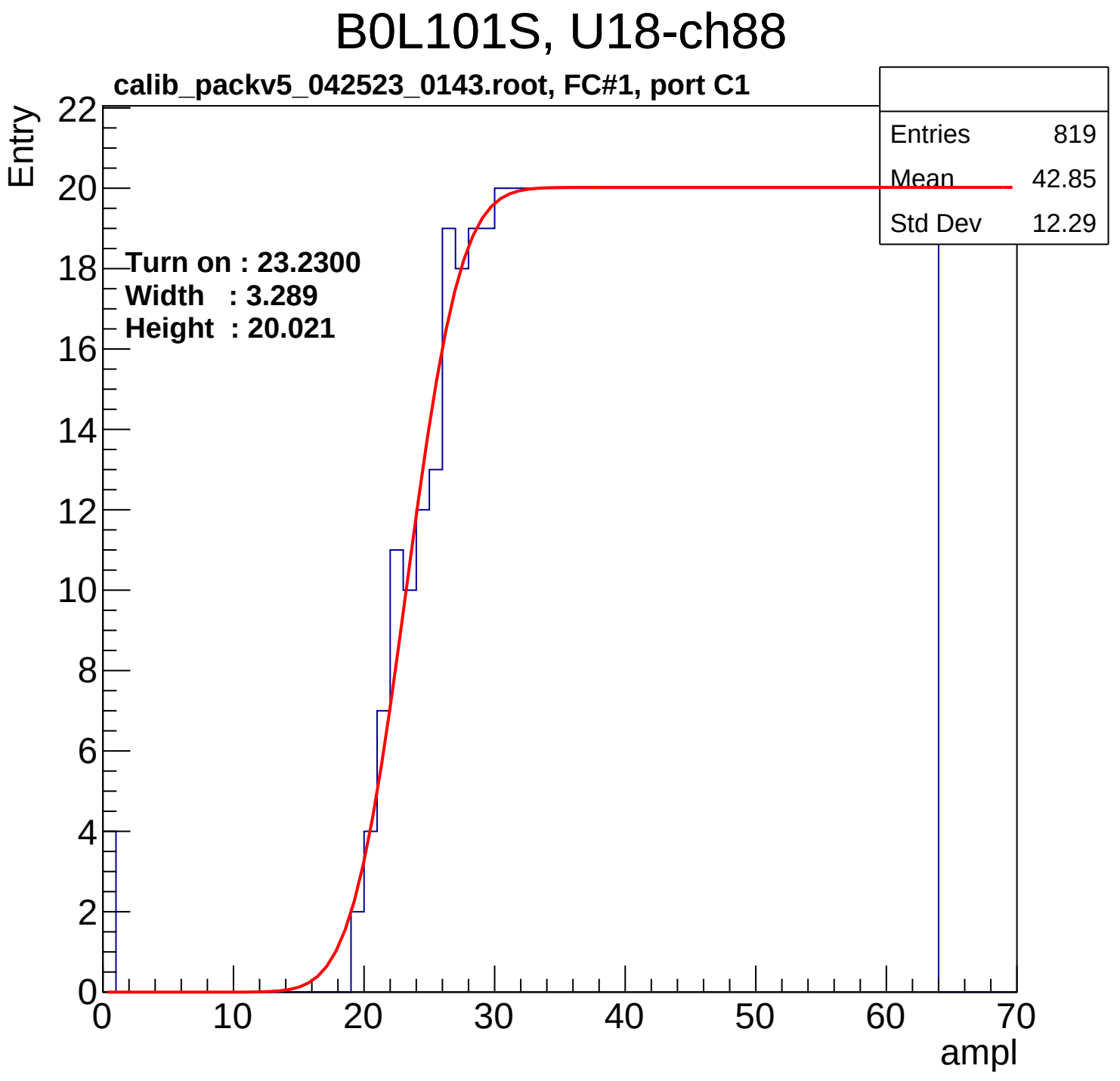
B0L101S, U18-ch88
calib_packv5_042523_0143.root, FC#1, port C1
Entries 819
Mean 42.85
Std Dev 12.29
Turn on : 23.2300
Width : 3.289
Height : 20.021
Entry
ampl
0
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8
10
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16
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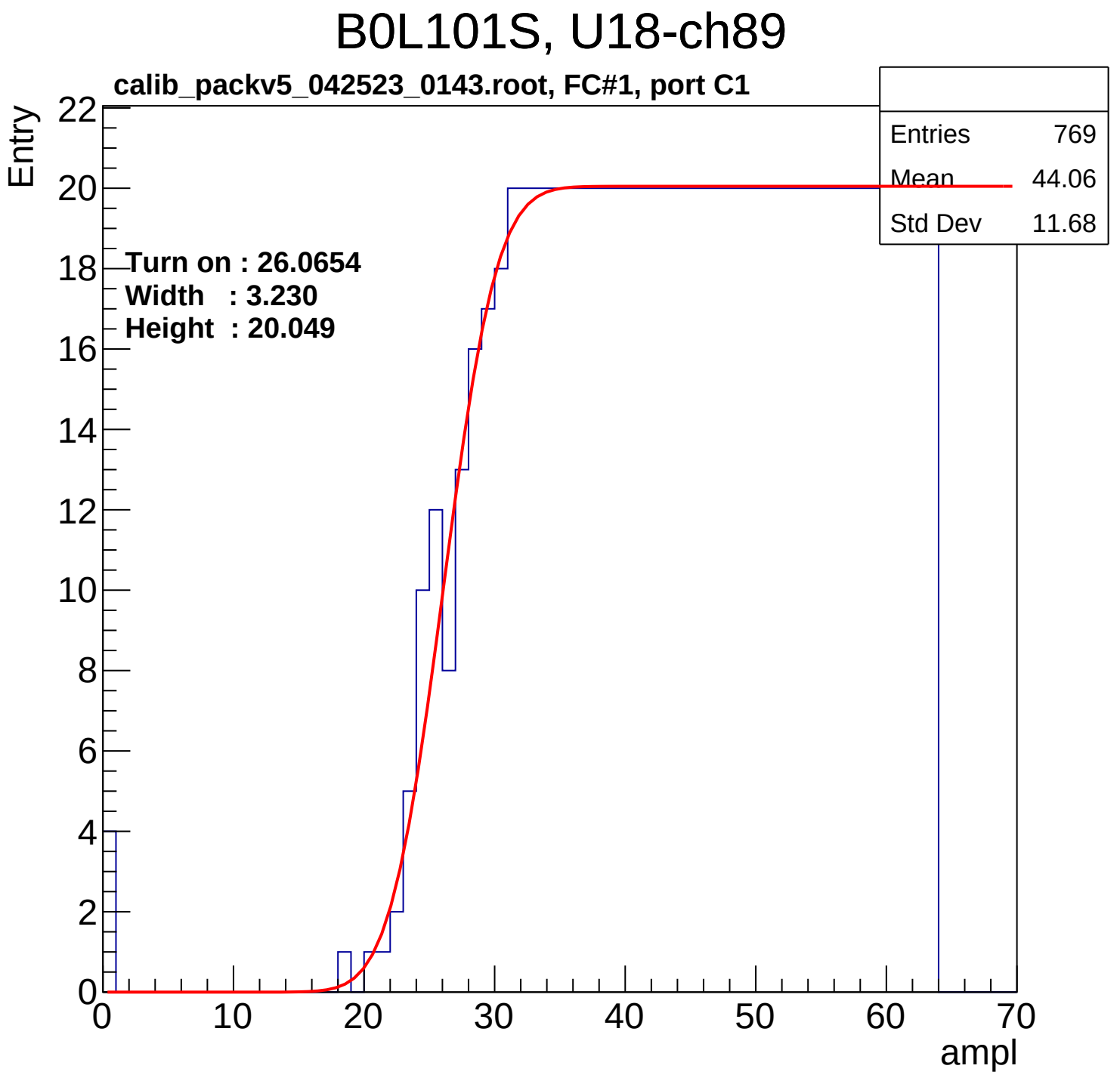
B0L101S, U18-ch89
calib_packv5_042523_0143.root, FC#1, port C1
Entries 769
Mean 44.06
Std Dev 11.68
Turn on : 26.0654
Width : 3.230
Height : 20.049
Entry
ampl
0
2
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6
8
10
12
14
16
18
20
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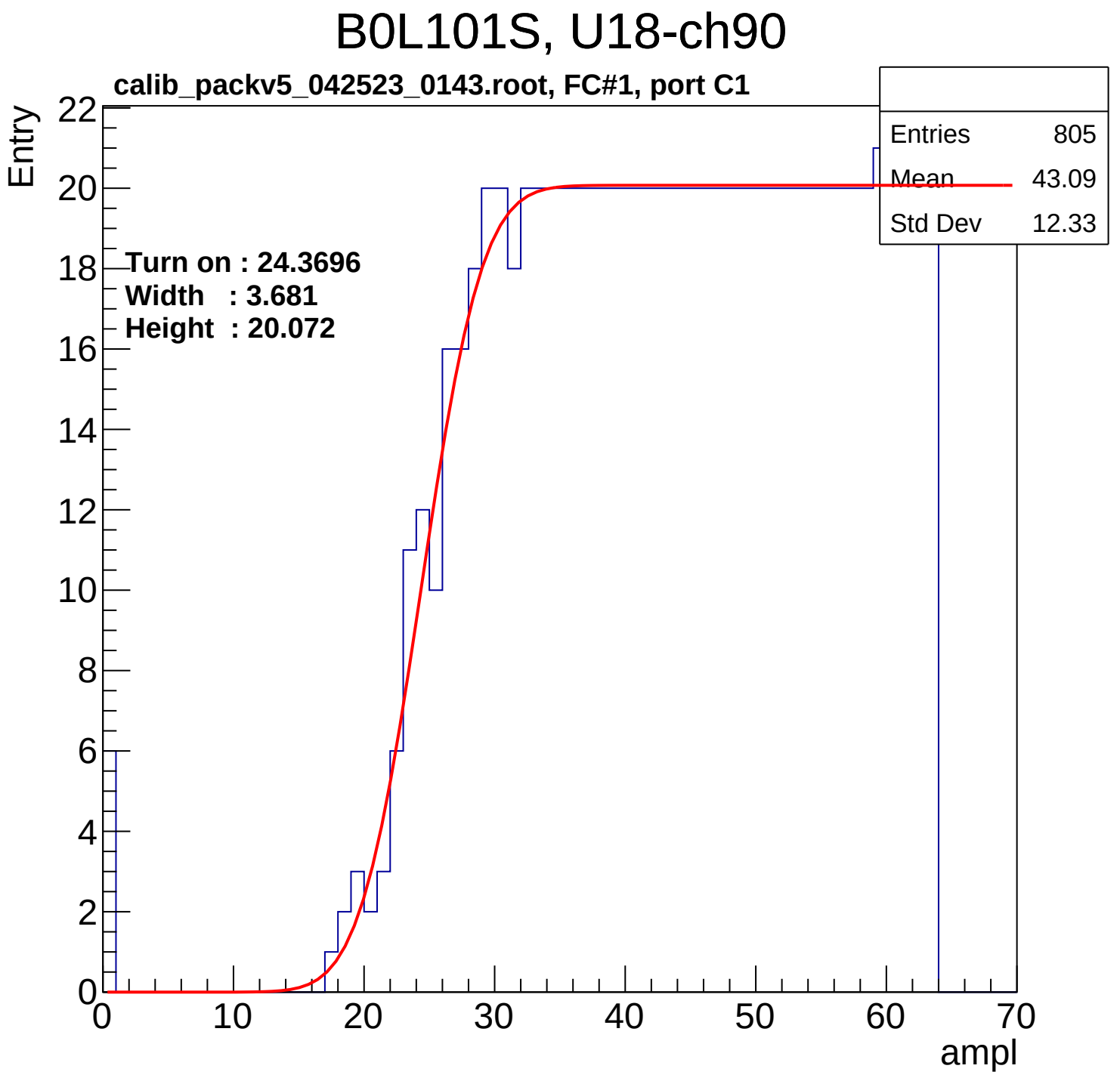
B0L101S, U18-ch90
calib_packv5_042523_0143.root, FC#1, port C1
Entries 805
Mean 43.09
Std Dev 12.33
Turn on : 24.3696
Width : 3.681
Height : 20.072
Entry
ampl
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8
10
12
14
16
18
20
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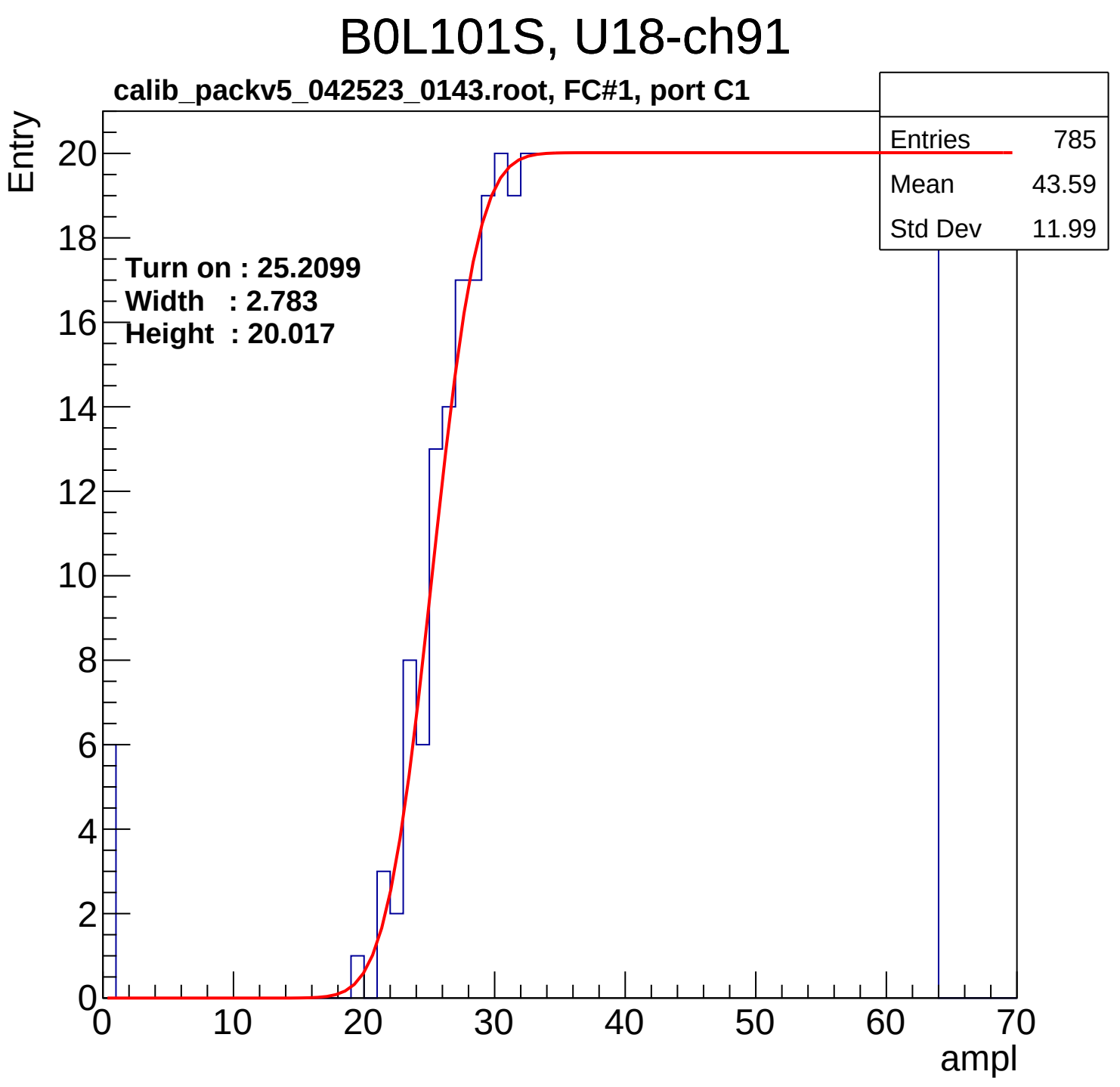
B0L101S, U18-ch91
calib_packv5_042523_0143.root, FC#1, port C1
Entries 785
Mean 43.59
Std Dev 11.99
Turn on : 25.2099
Width : 2.783
Height : 20.017
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
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20
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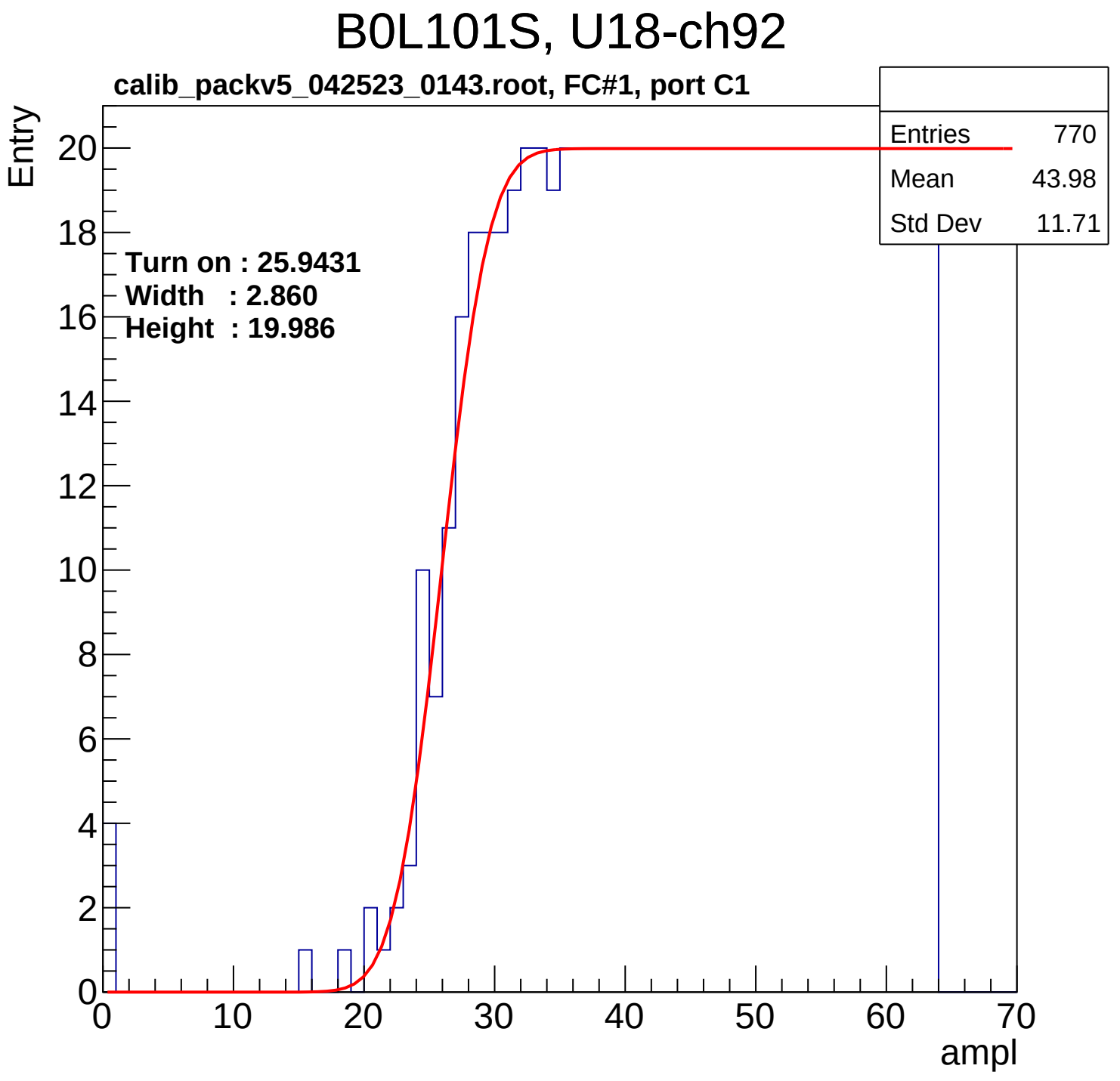
B0L101S, U18-ch92
calib_packv5_042523_0143.root, FC#1, port C1
Entries 770
Mean 43.98
Std Dev 11.71
Turn on : 25.9431
Width : 2.860
Height : 19.986
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
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20
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40
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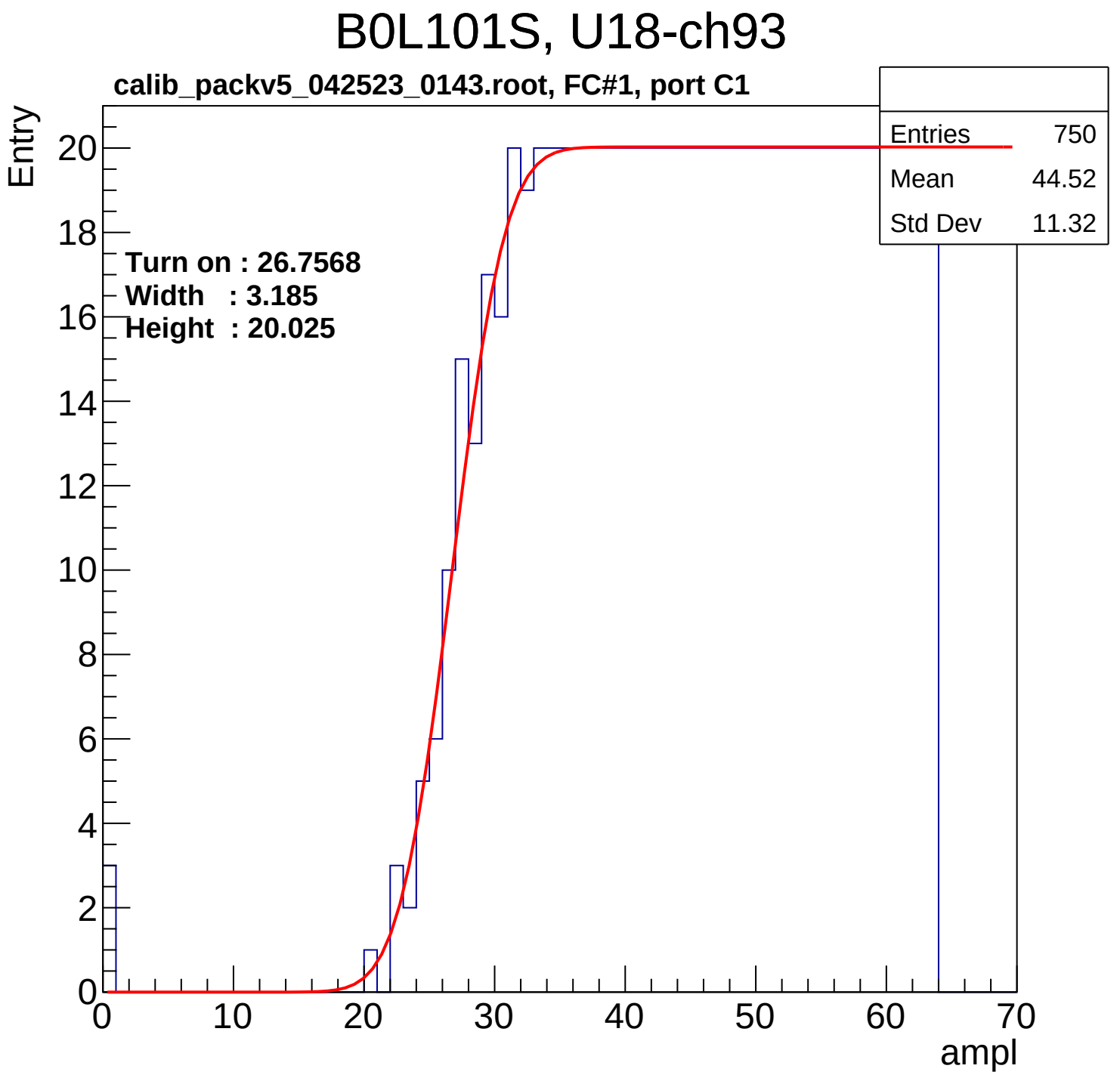
B0L101S, U18-ch93
calib_packv5_042523_0143.root, FC#1, port C1
Entries 750
Mean 44.52
Std Dev 11.32
Turn on : 26.7568
Width : 3.185
Height : 20.025
Entry
ampl
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6
8
10
12
14
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0
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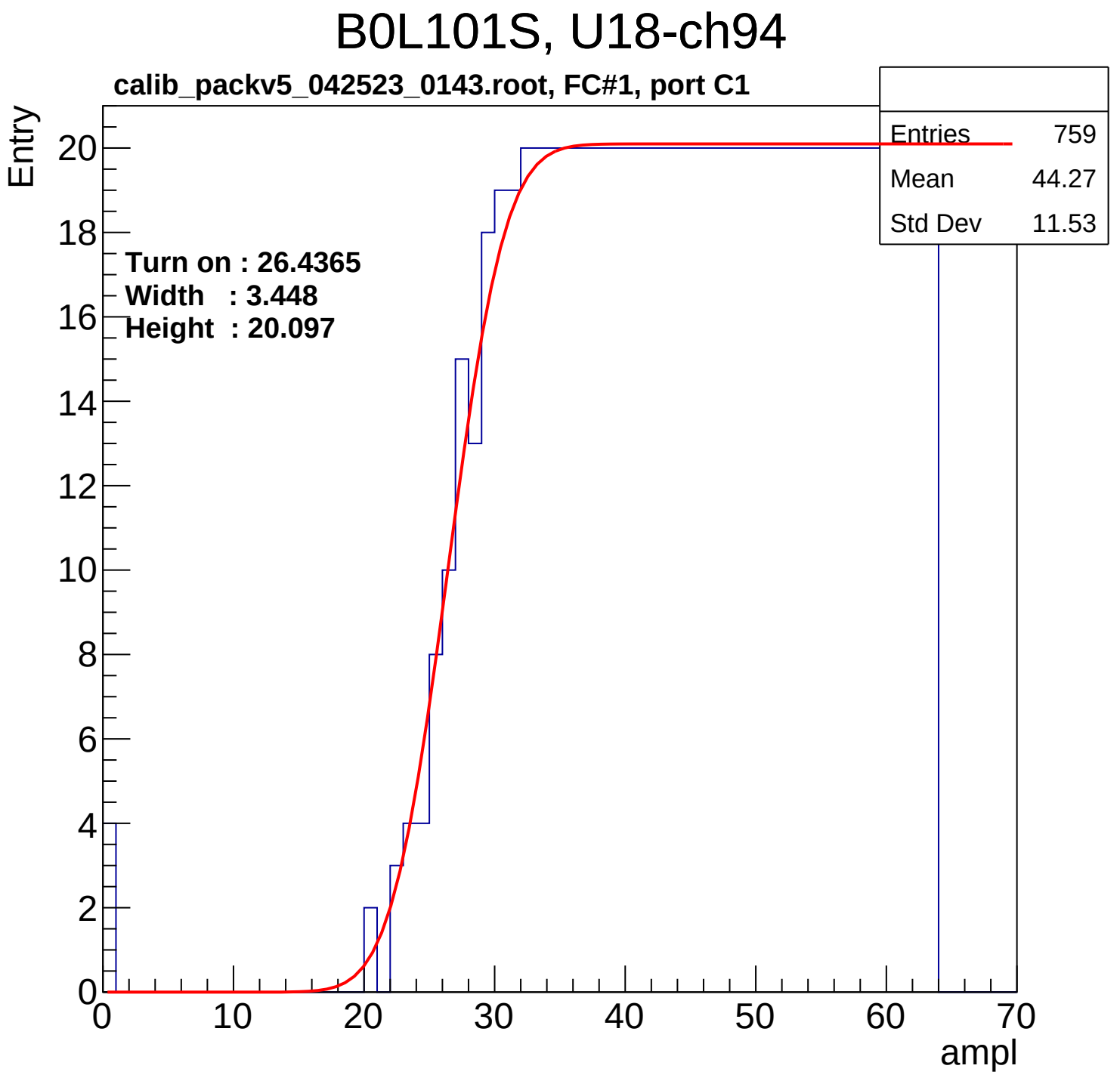
B0L101S, U18-ch94
calib_packv5_042523_0143.root, FC#1, port C1
Entries 759
Mean 44.27
Std Dev 11.53
Turn on : 26.4365
Width : 3.448
Height : 20.097
Entry
ampl
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6
8
10
12
14
16
18
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0
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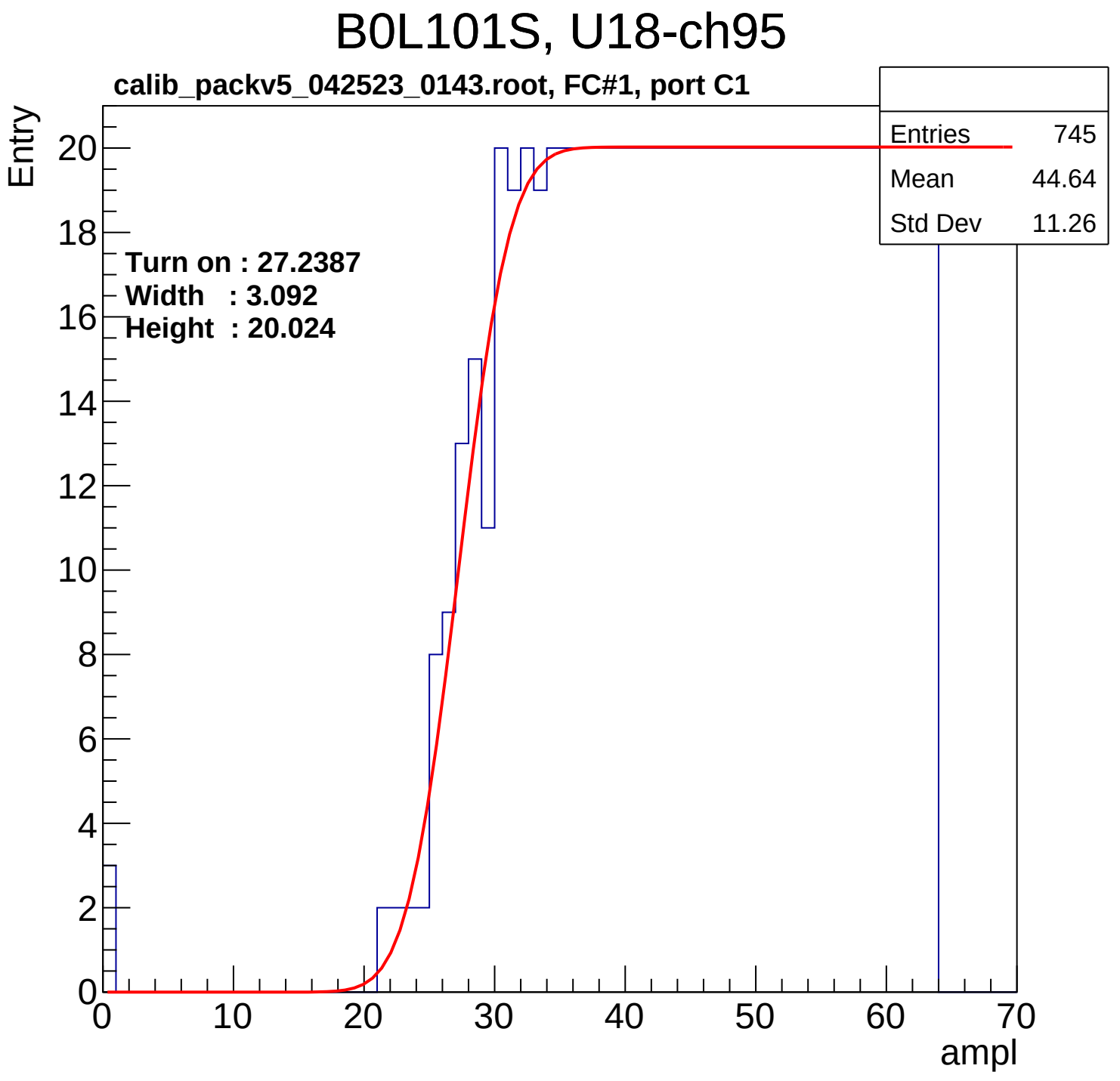
B0L101S, U18-ch95
calib_packv5_042523_0143.root, FC#1, port C1
Entries 745
Mean 44.64
Std Dev 11.26
Turn on : 27.2387
Width : 3.092
Height : 20.024
Entry
ampl
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6
8
10
12
14
16
18
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0
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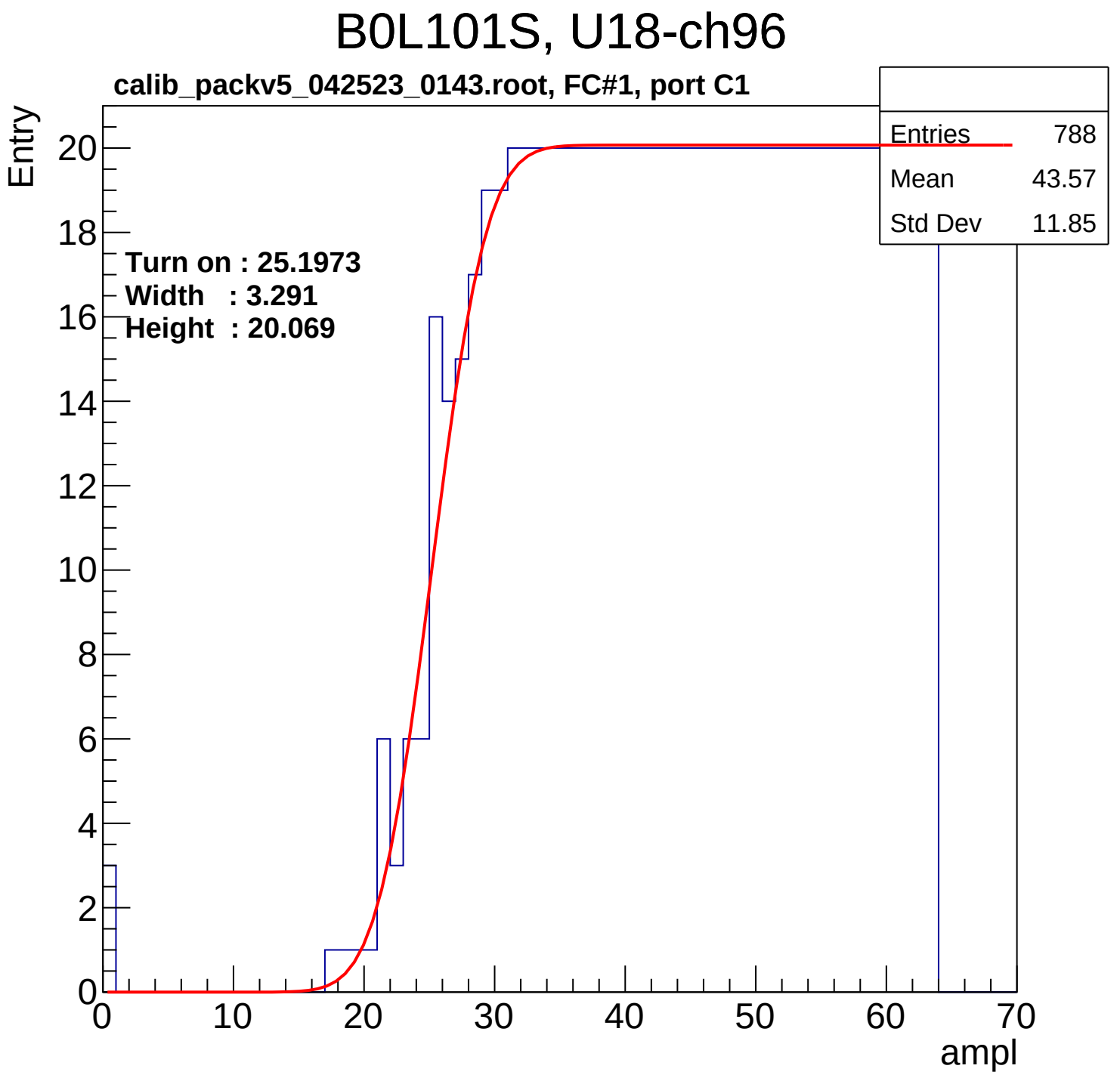
B0L101S, U18-ch96
calib_packv5_042523_0143.root, FC#1, port C1
Entries 788
Mean 43.57
Std Dev 11.85
Turn on : 25.1973
Width : 3.291
Height : 20.069
Entry
ampl
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6
8
10
12
14
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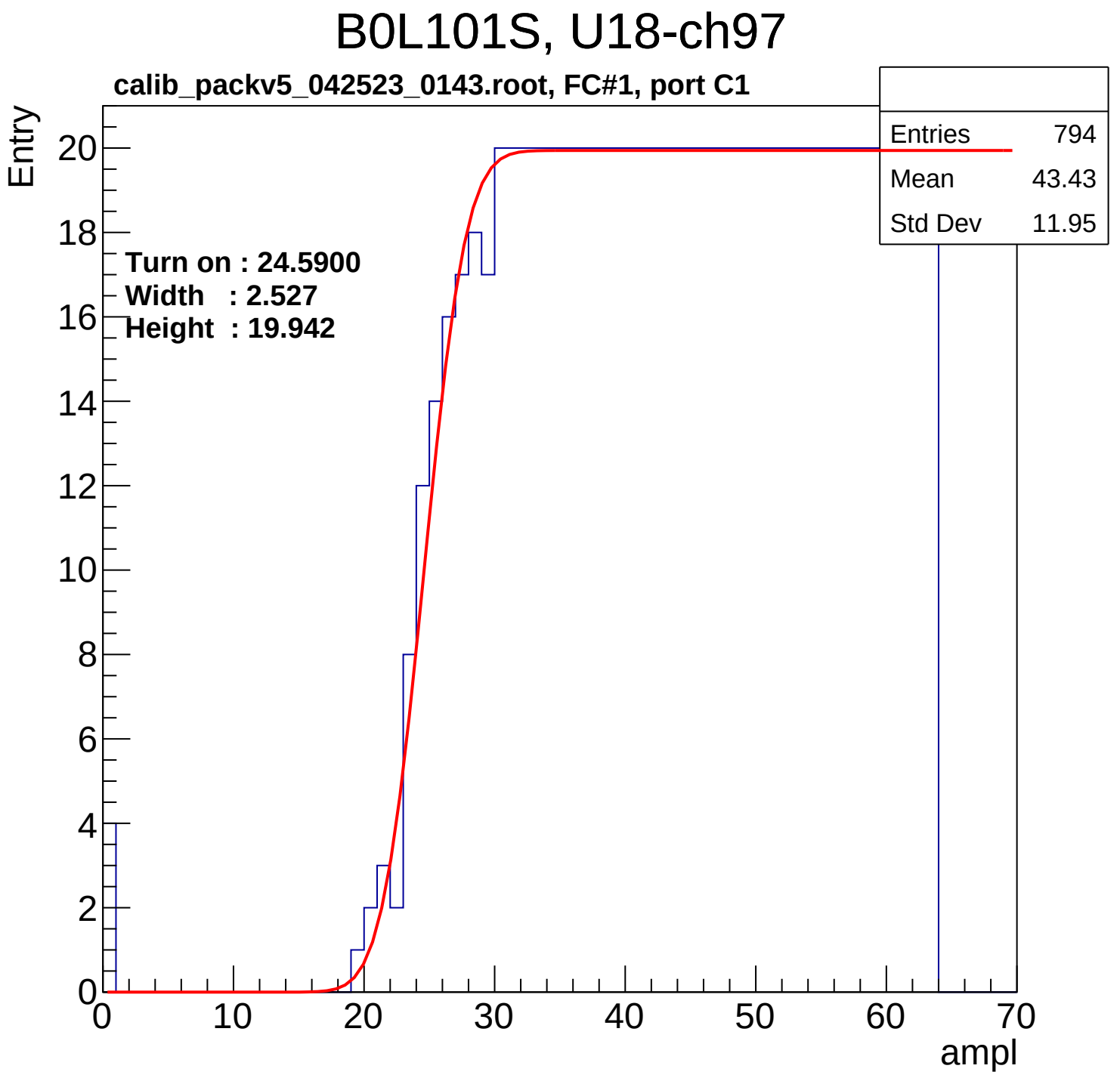
B0L101S, U18-ch97
calib_packv5_042523_0143.root, FC#1, port C1
Entries 794
Mean 43.43
Std Dev 11.95
Turn on : 24.5900
Width : 2.527
Height : 19.942
Entry
ampl
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10
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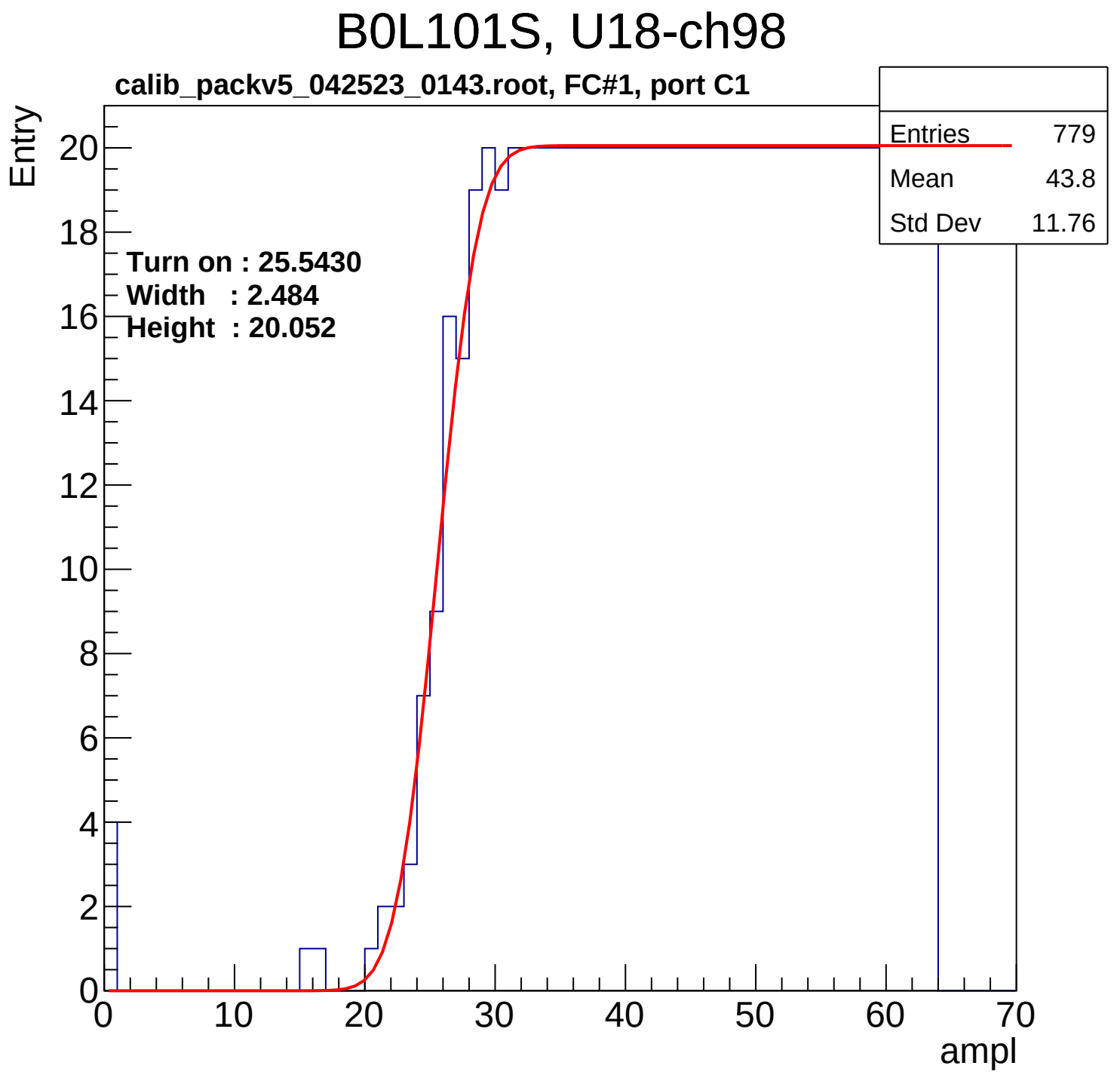
B0L101S, U18-ch98
calib_packv5_042523_0143.root, FC#1, port C1
Entries 779
Mean 43.8
Std Dev 11.76
Turn on : 25.5430
Width : 2.484
Height : 20.052
Entry
ampl
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6
8
10
12
14
16
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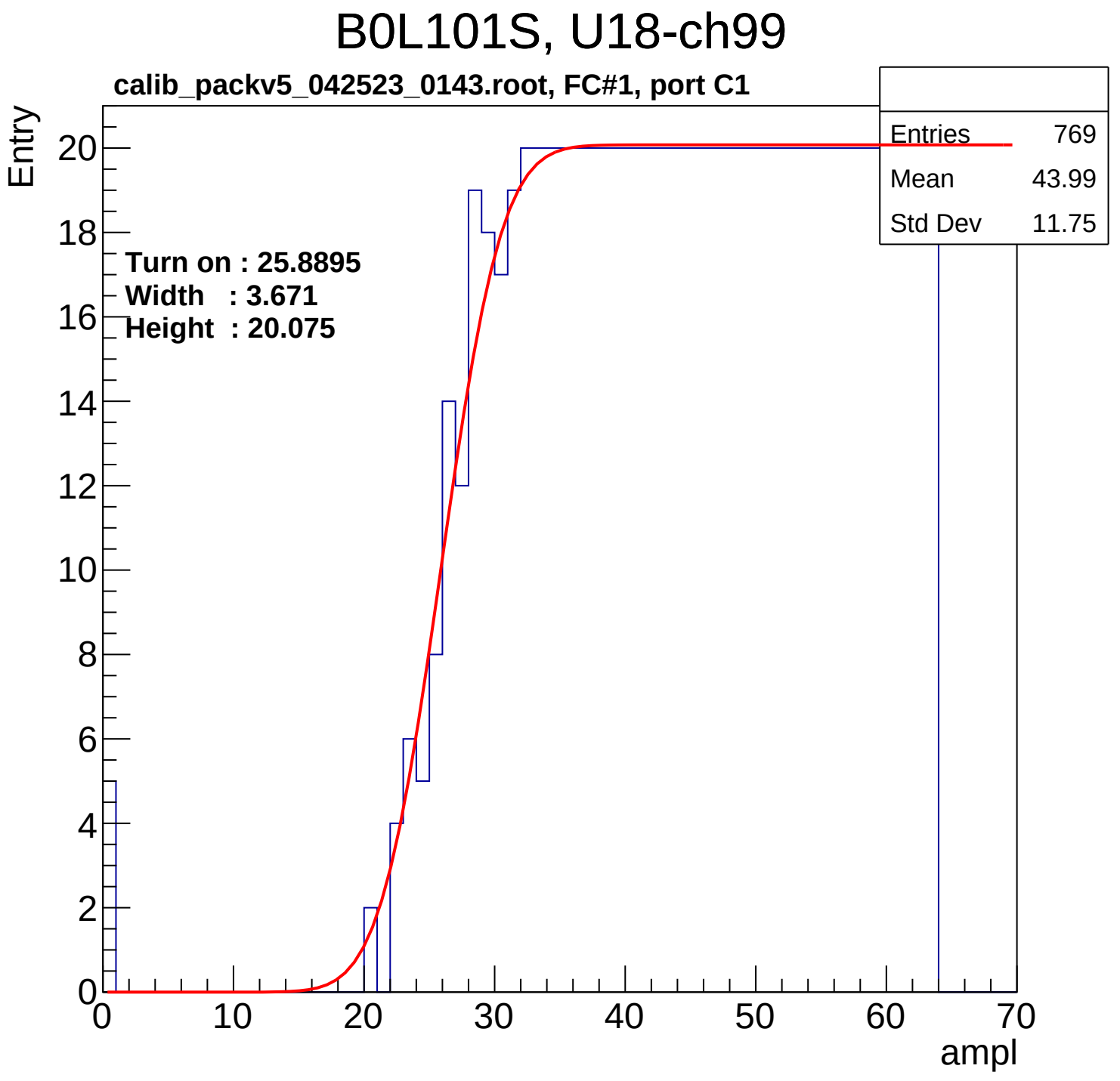
B0L101S, U18-ch99
calib_packv5_042523_0143.root, FC#1, port C1
Entries 769
Mean 43.99
Std Dev 11.75
Turn on : 25.8895
Width : 3.671
Height : 20.075
Entry
ampl
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8
10
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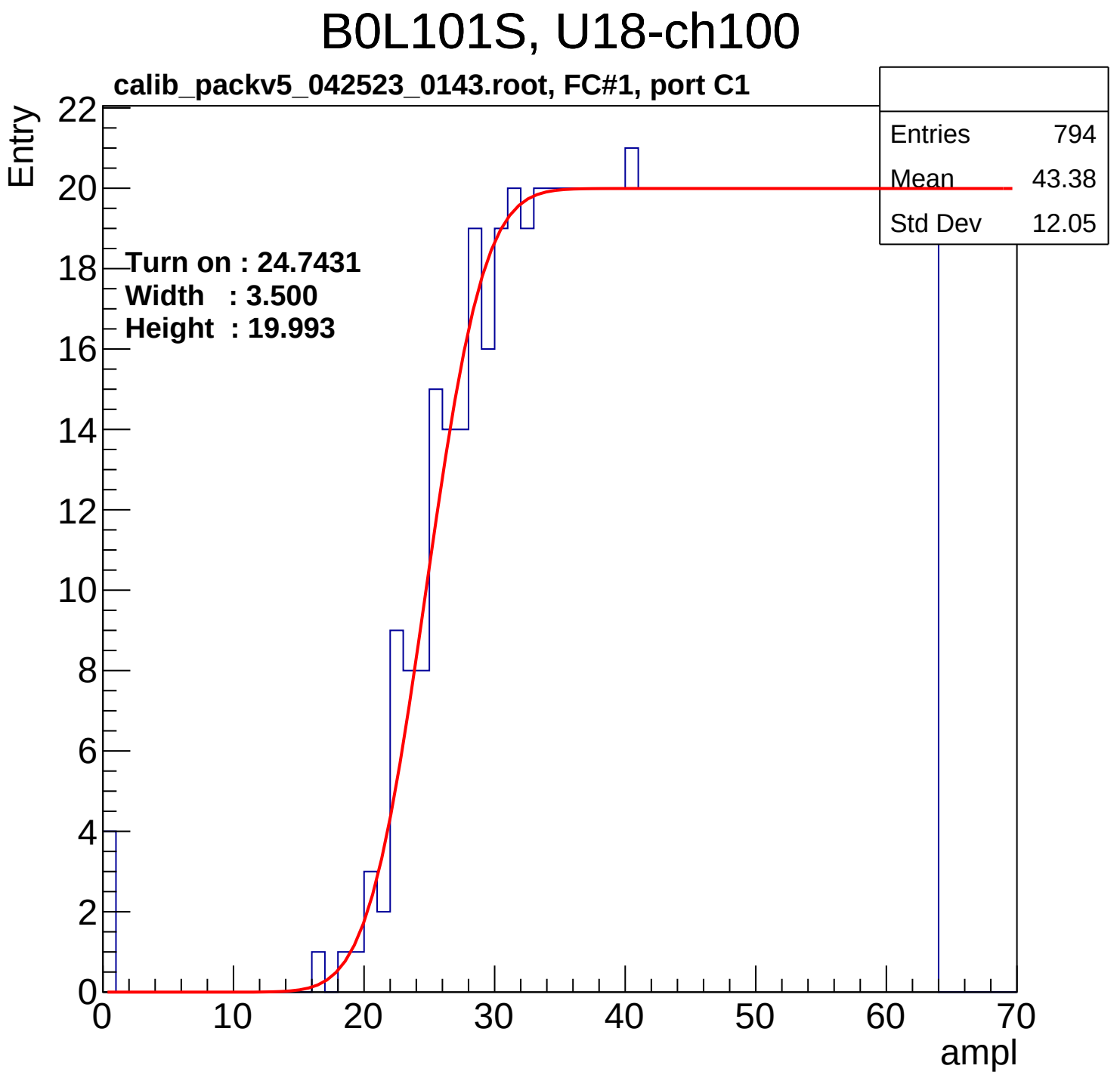
B0L101S, U18-ch100
calib_packv5_042523_0143.root, FC#1, port C1
Entries 794
Mean 43.38
Std Dev 12.05
Turn on : 24.7431
Width : 3.500
Height : 19.993
Entry
ampl
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8
10
12
14
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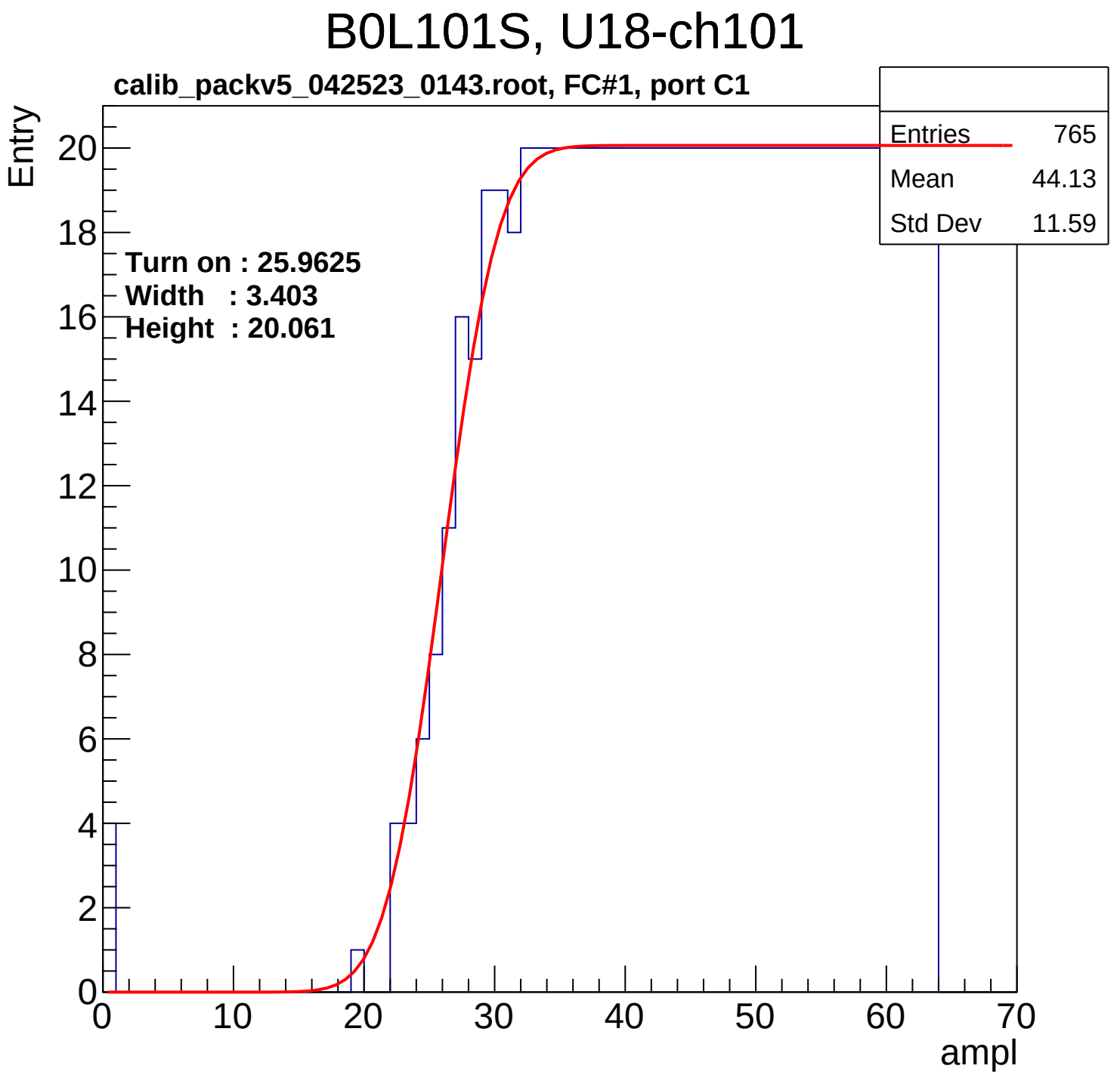
B0L101S, U18-ch101
calib_packv5_042523_0143.root, FC#1, port C1
Entries 765
Mean 44.13
Std Dev 11.59
Turn on : 25.9625
Width : 3.403
Height : 20.061
Entry
ampl
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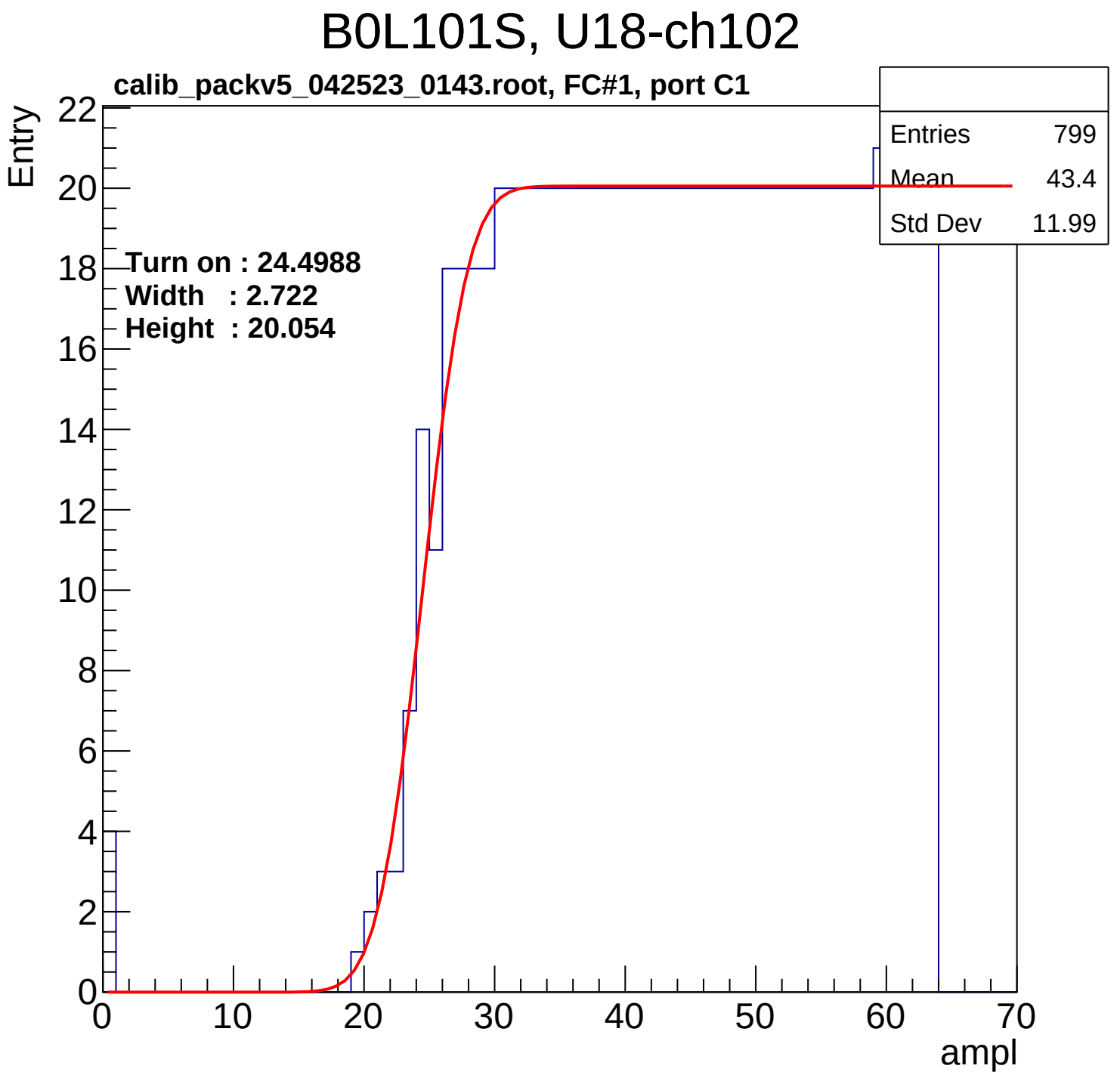
B0L101S, U18-ch102
calib_packv5_042523_0143.root, FC#1, port C1
Entries 799
Mean 43.4
Std Dev 11.99
Turn on : 24.4988
Width : 2.722
Height : 20.054
Entry
ampl
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8
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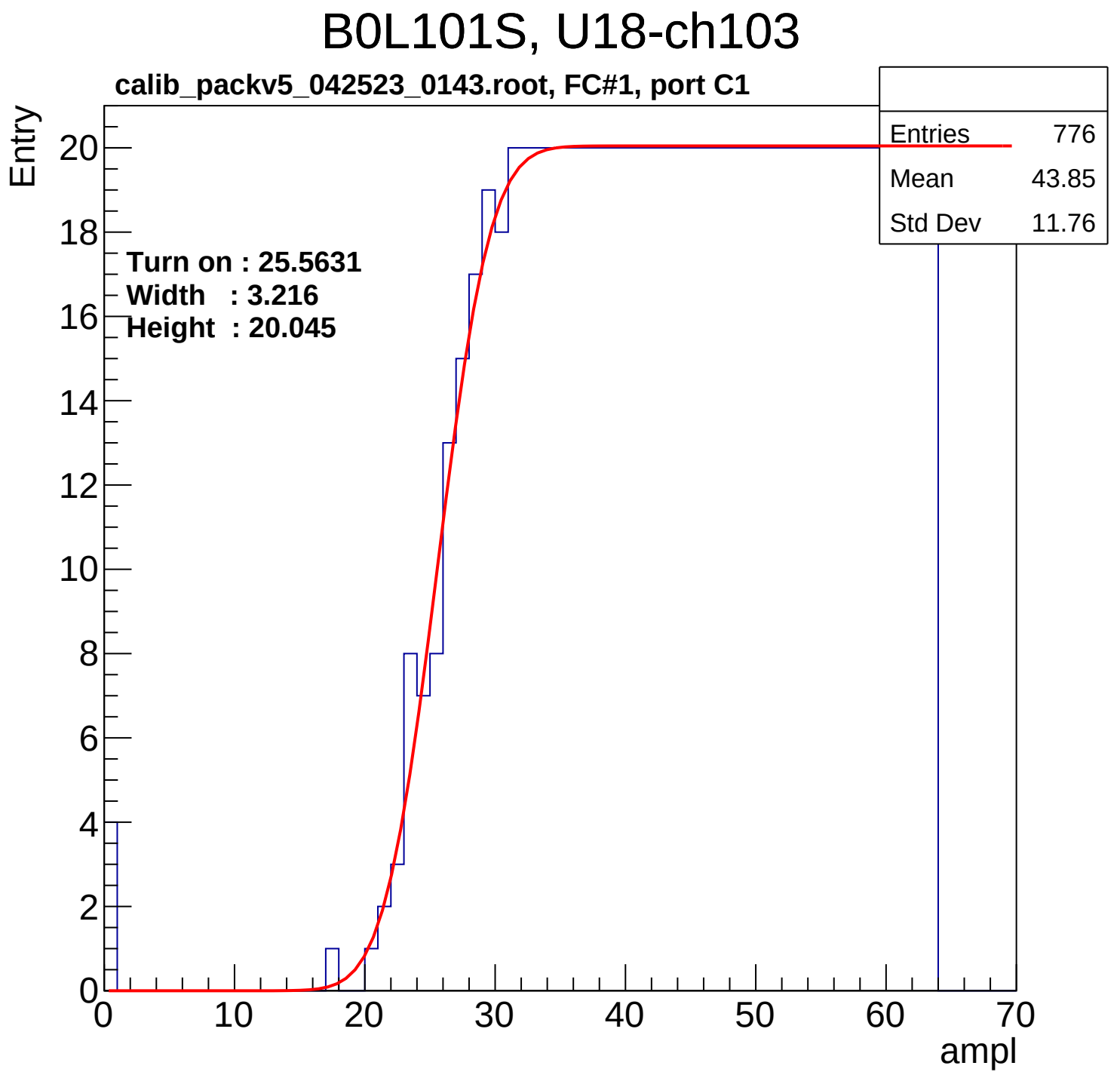
B0L101S, U18-ch103
calib_packv5_042523_0143.root, FC#1, port C1
Entries 776
Mean 43.85
Std Dev 11.76
Turn on : 25.5631
Width : 3.216
Height : 20.045
Entry
ampl
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6
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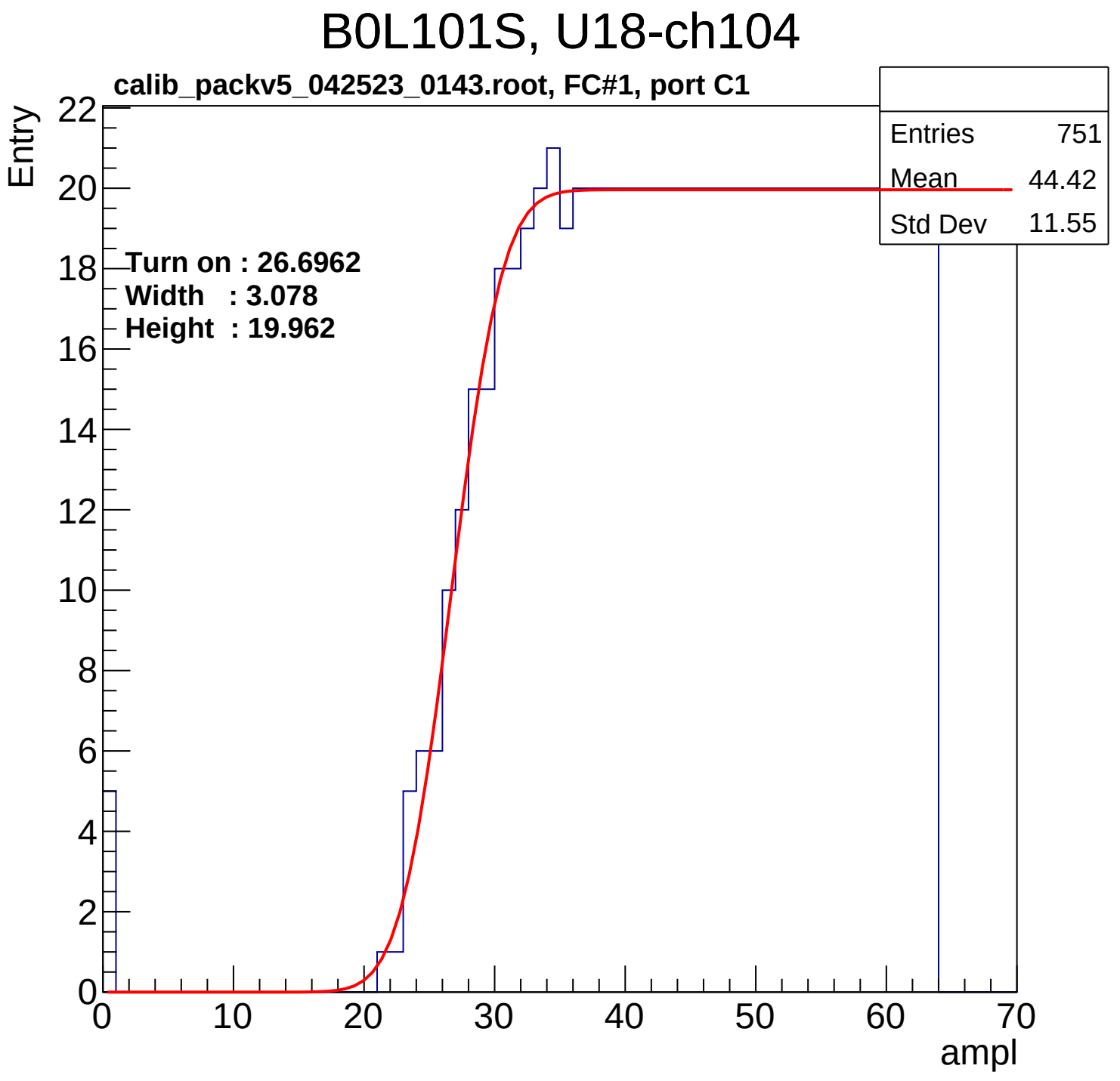
B0L101S, U18-ch104
calib_packv5_042523_0143.root, FC#1, port C1
Entries 751
Mean 44.42
Std Dev 11.55
Turn on : 26.6962
Width : 3.078
Height : 19.962
Entry
ampl
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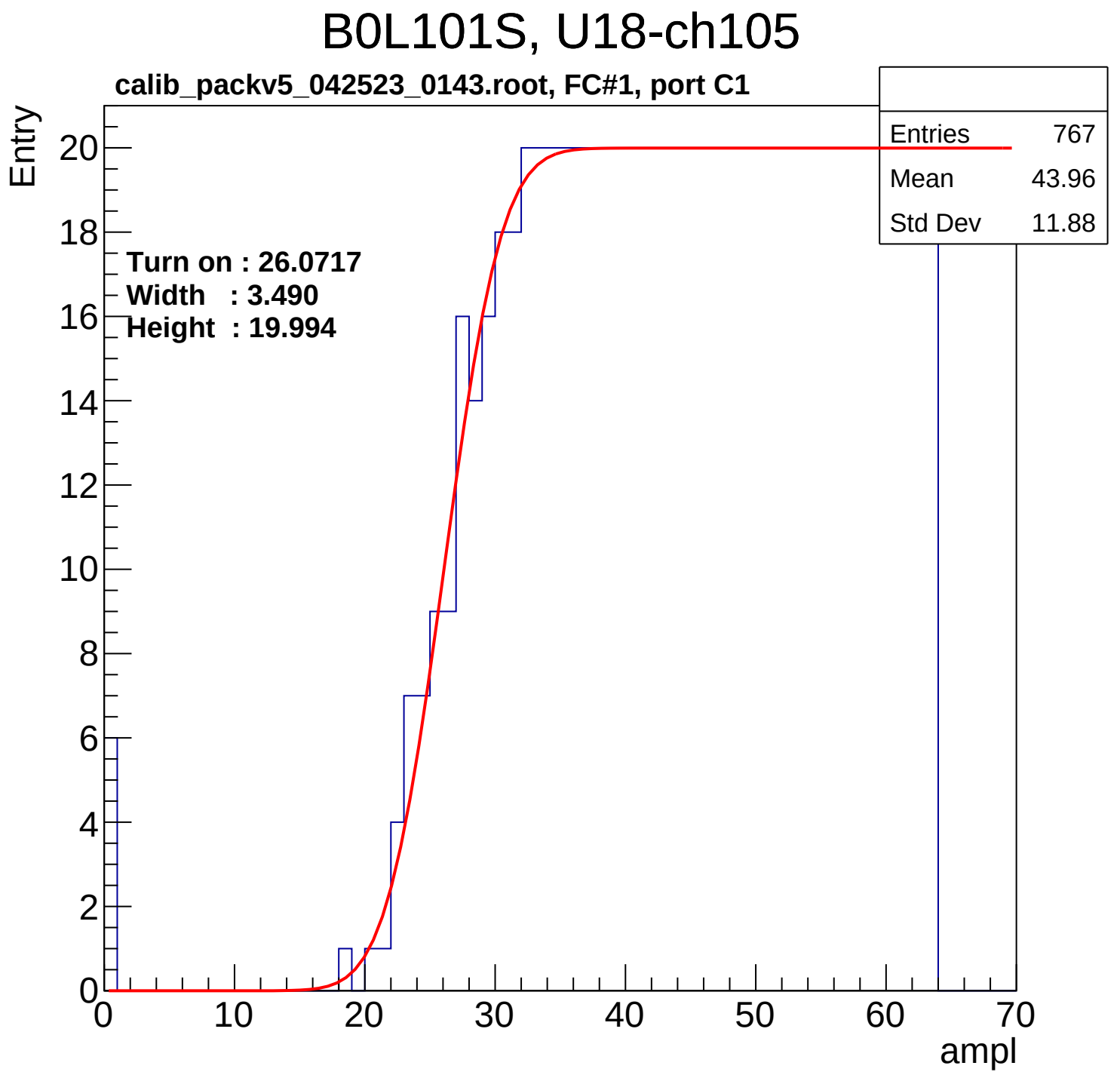
B0L101S, U18-ch105
calib_packv5_042523_0143.root, FC#1, port C1
Entries 767
Mean 43.96
Std Dev 11.88
Turn on : 26.0717
Width : 3.490
Height : 19.994
Entry
ampl
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6
8
10
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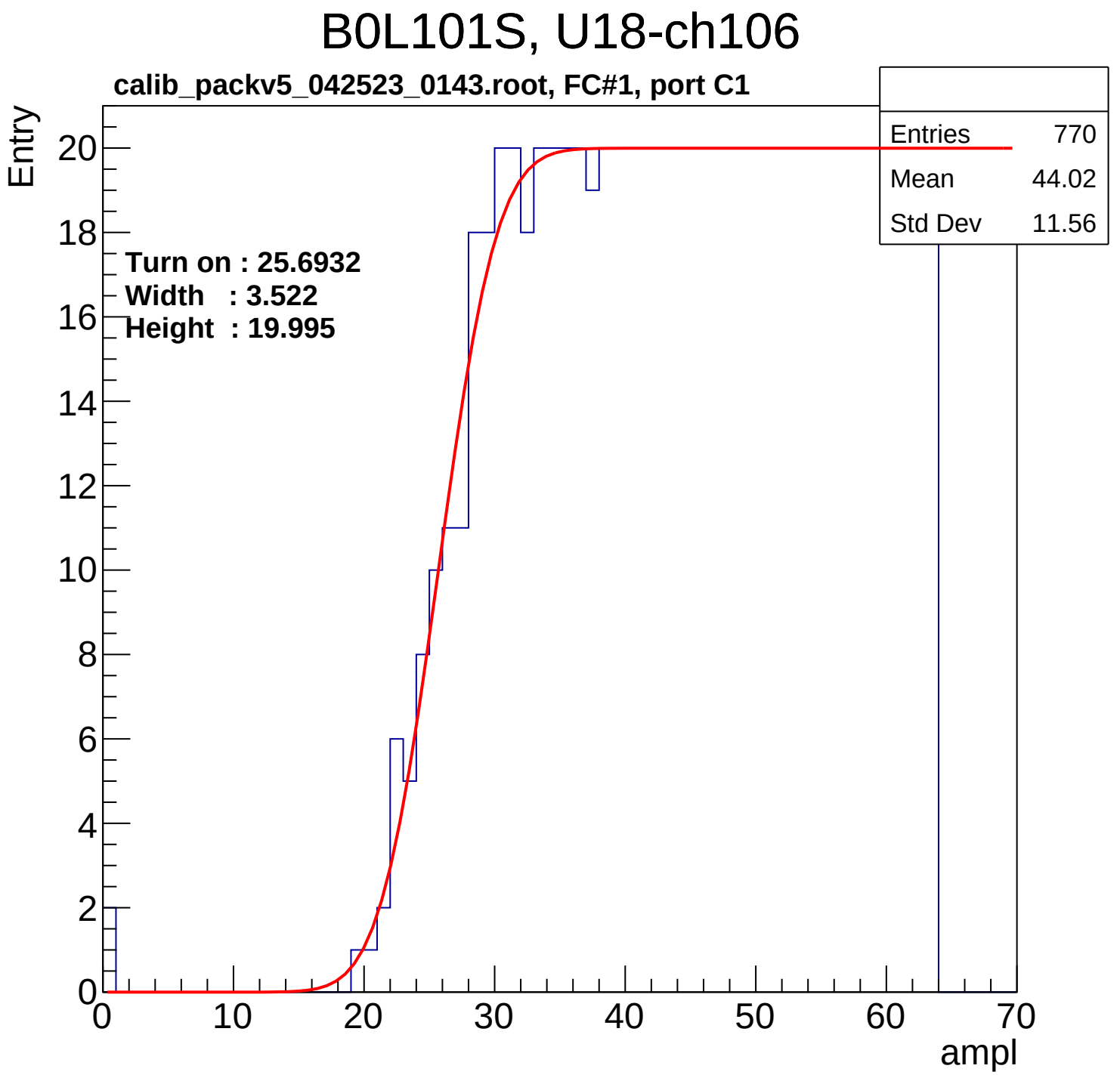
B0L101S, U18-ch106
calib_packv5_042523_0143.root, FC#1, port C1
Entries 770
Mean 44.02
Std Dev 11.56
Turn on : 25.6932
Width : 3.522
Height : 19.995
Entry
ampl
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6
8
10
12
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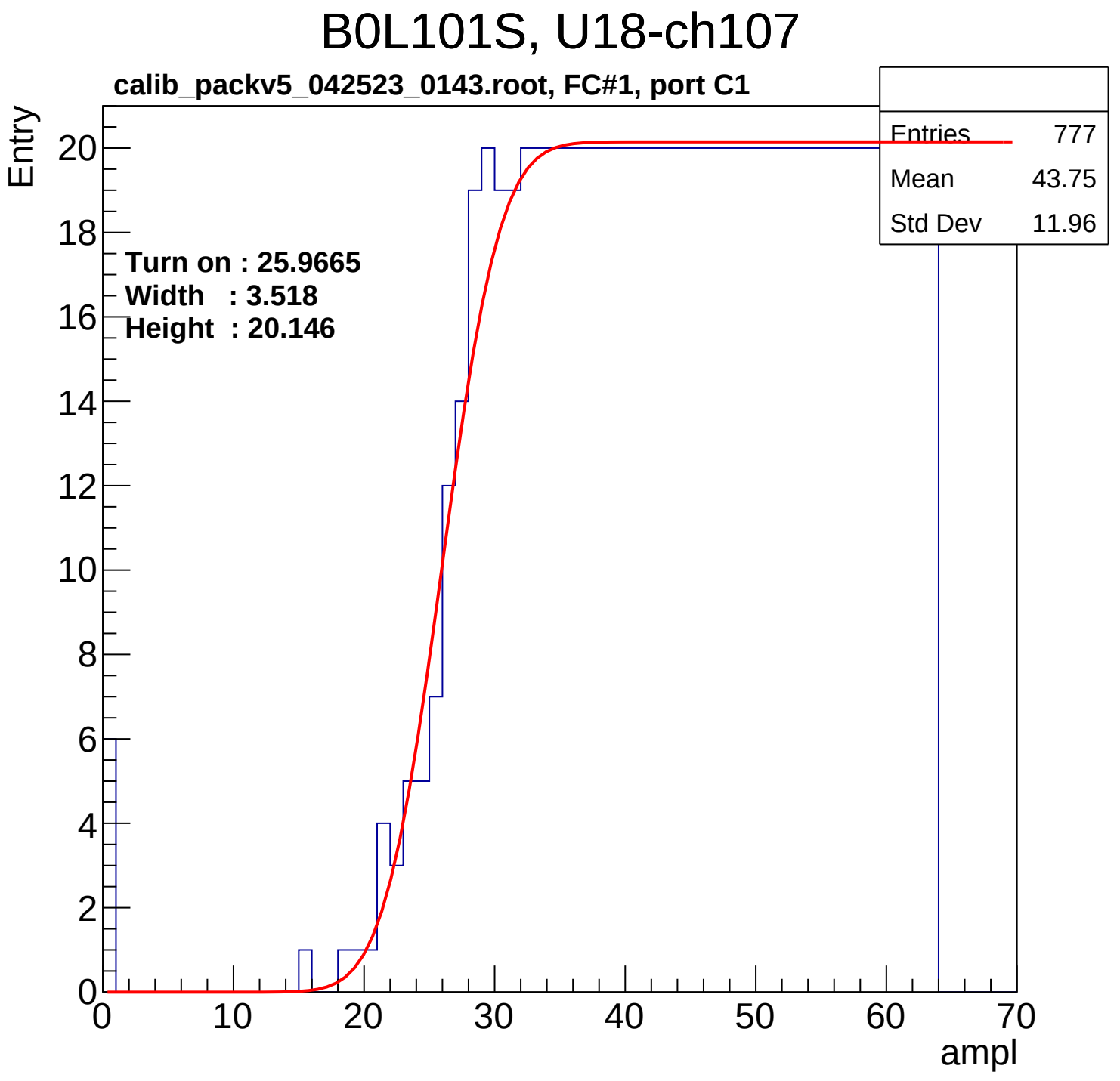
B0L101S, U18-ch107
calib_packv5_042523_0143.root, FC#1, port C1
Entries 777
Mean 43.75
Std Dev 11.96
Turn on : 25.9665
Width : 3.518
Height : 20.146
Entry
ampl
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6
8
10
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14
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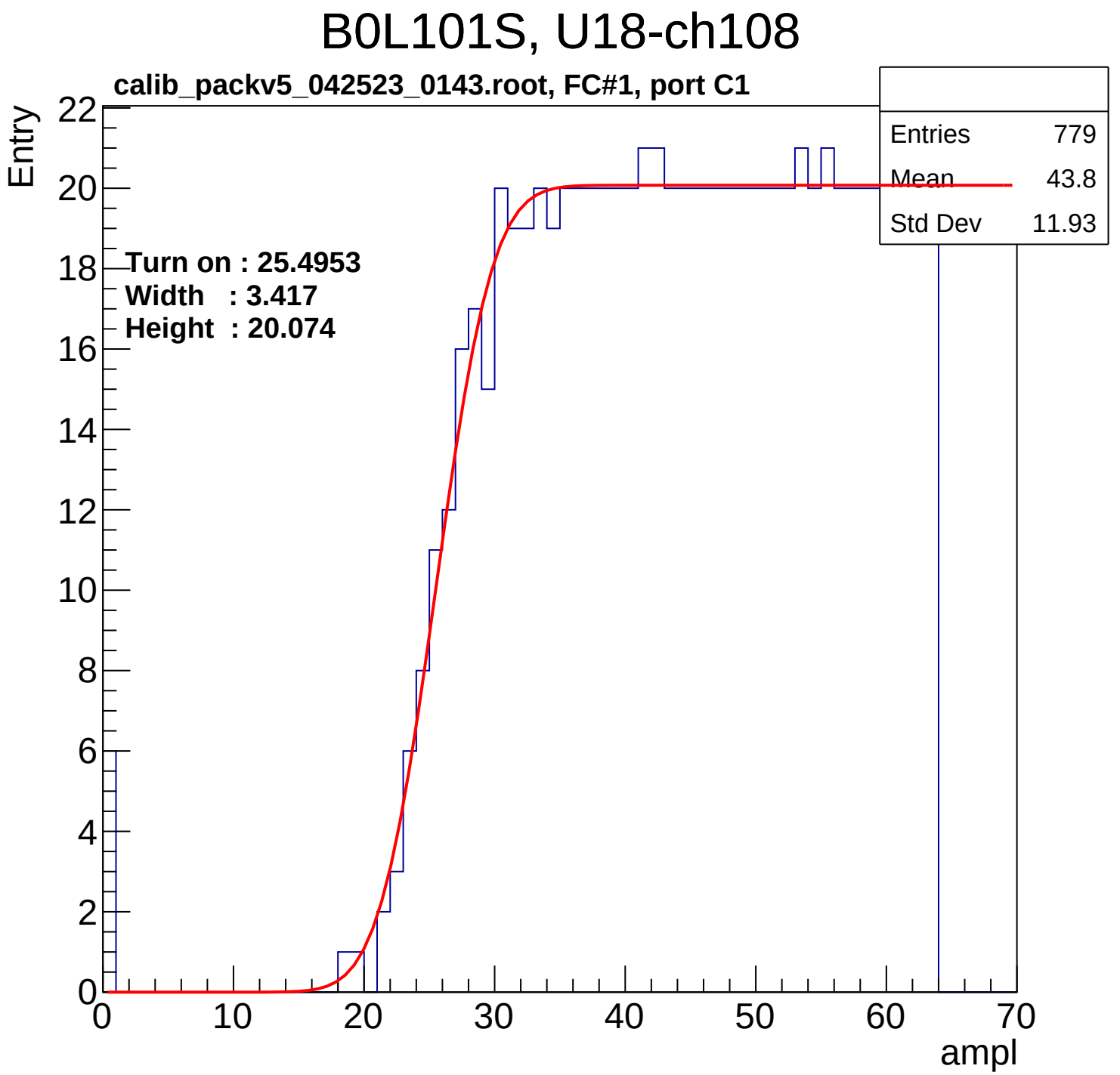
B0L101S, U18-ch108
calib_packv5_042523_0143.root, FC#1, port C1
Entries 779
Mean 43.8
Std Dev 11.93
Turn on : 25.4953
Width : 3.417
Height : 20.074
Entry
ampl
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8
10
12
14
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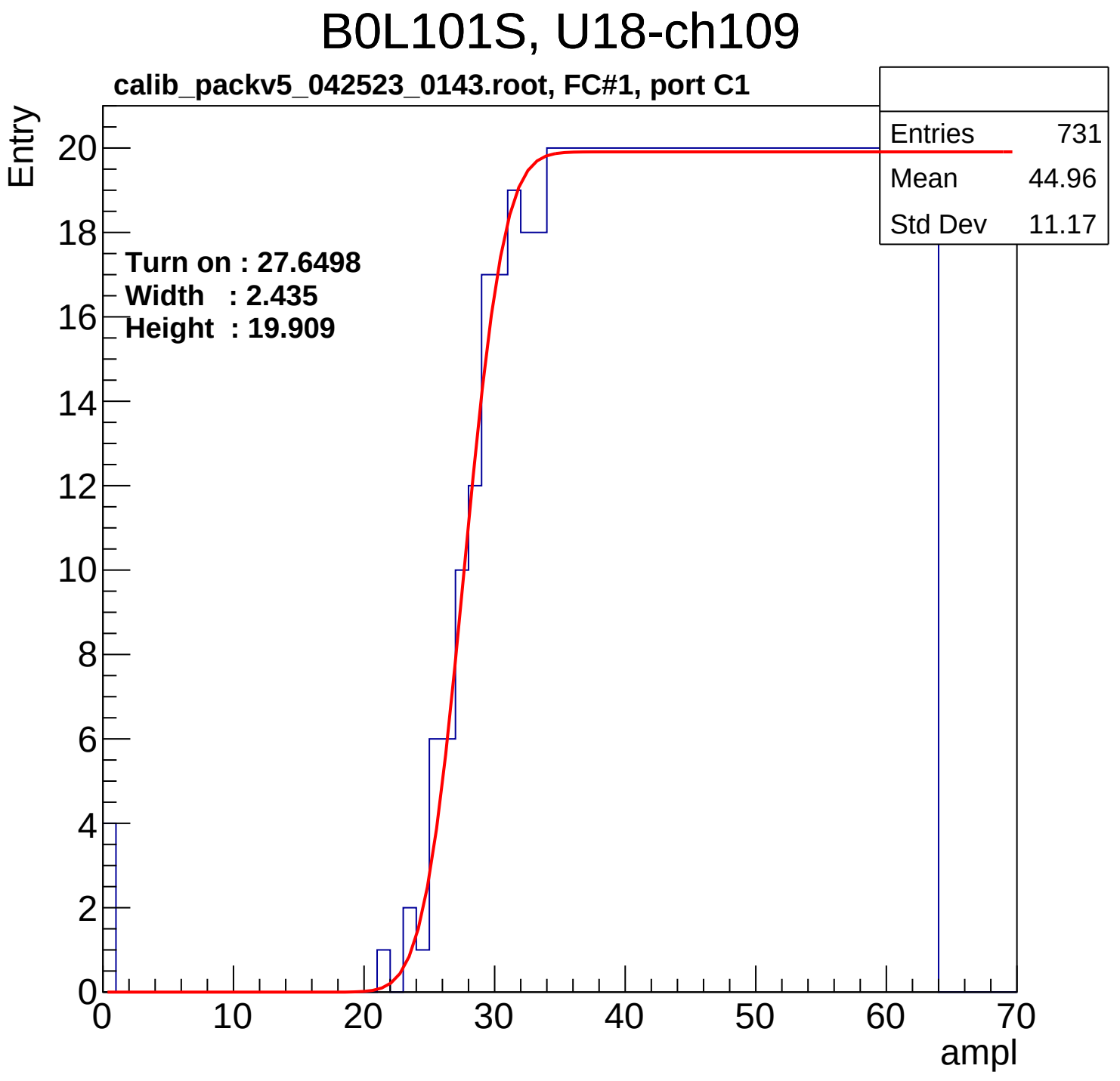
B0L101S, U18-ch109
calib_packv5_042523_0143.root, FC#1, port C1
Entries 731
Mean 44.96
Std Dev 11.17
Turn on : 27.6498
Width : 2.435
Height : 19.909
Entry
ampl
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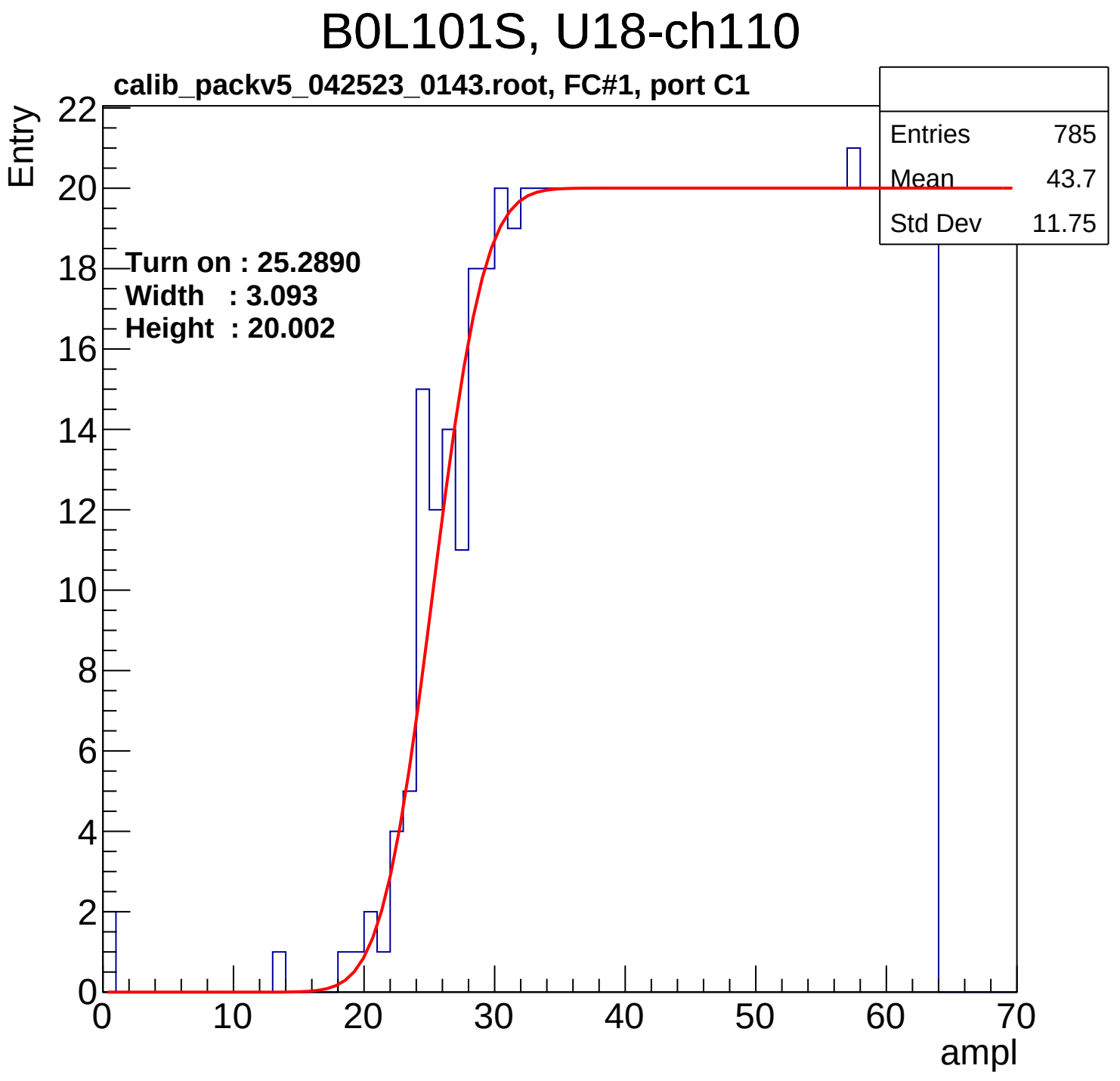
B0L101S, U18-ch110
calib_packv5_042523_0143.root, FC#1, port C1
Entries 785
Mean 43.7
Std Dev 11.75
Turn on : 25.2890
Width : 3.093
Height : 20.002
Entry
ampl
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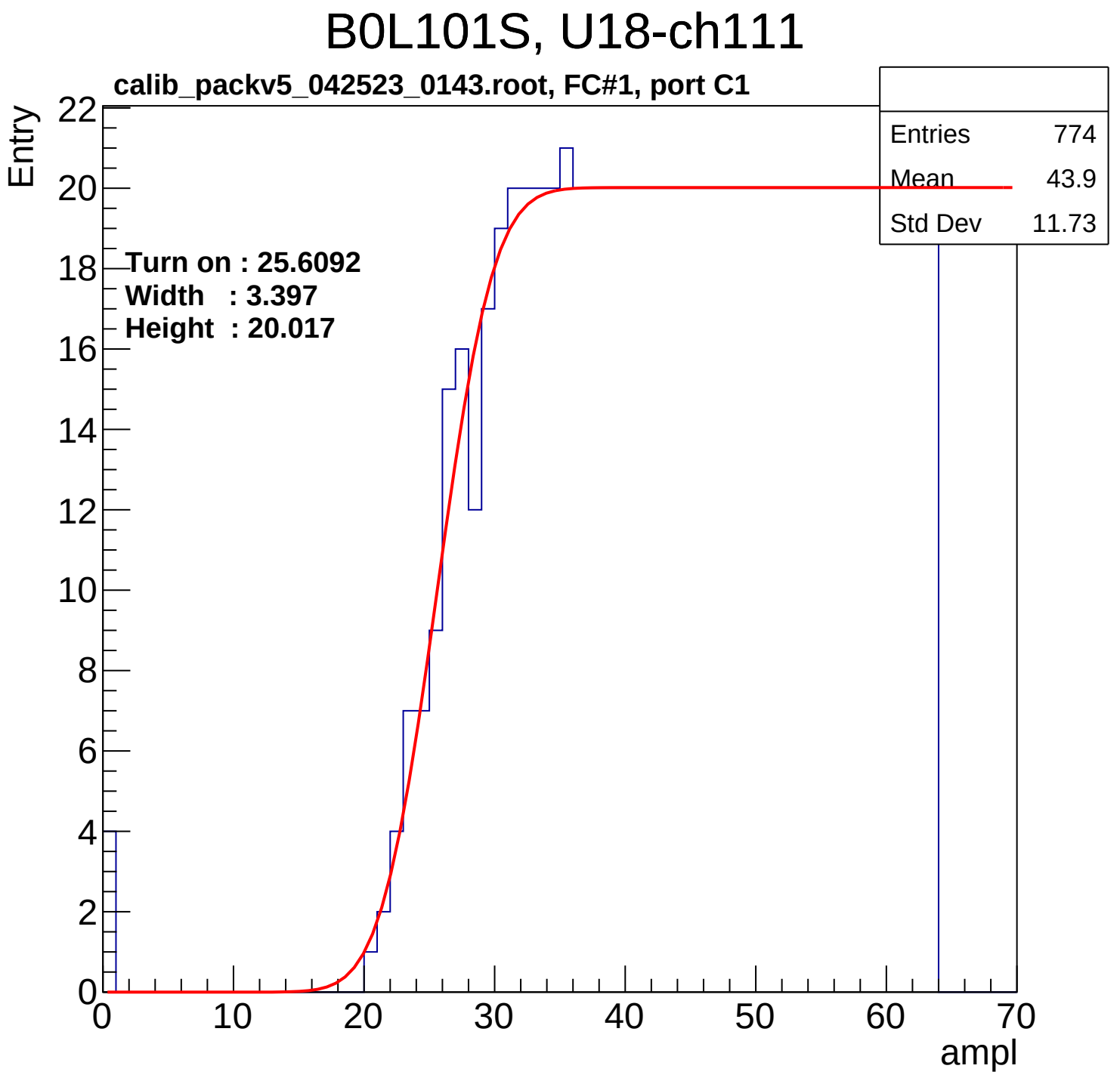
B0L101S, U18-ch111
calib_packv5_042523_0143.root, FC#1, port C1
Entries 774
Mean 43.9
Std Dev 11.73
Turn on : 25.6092
Width : 3.397
Height : 20.017
Entry
ampl
0
2
4
6
8
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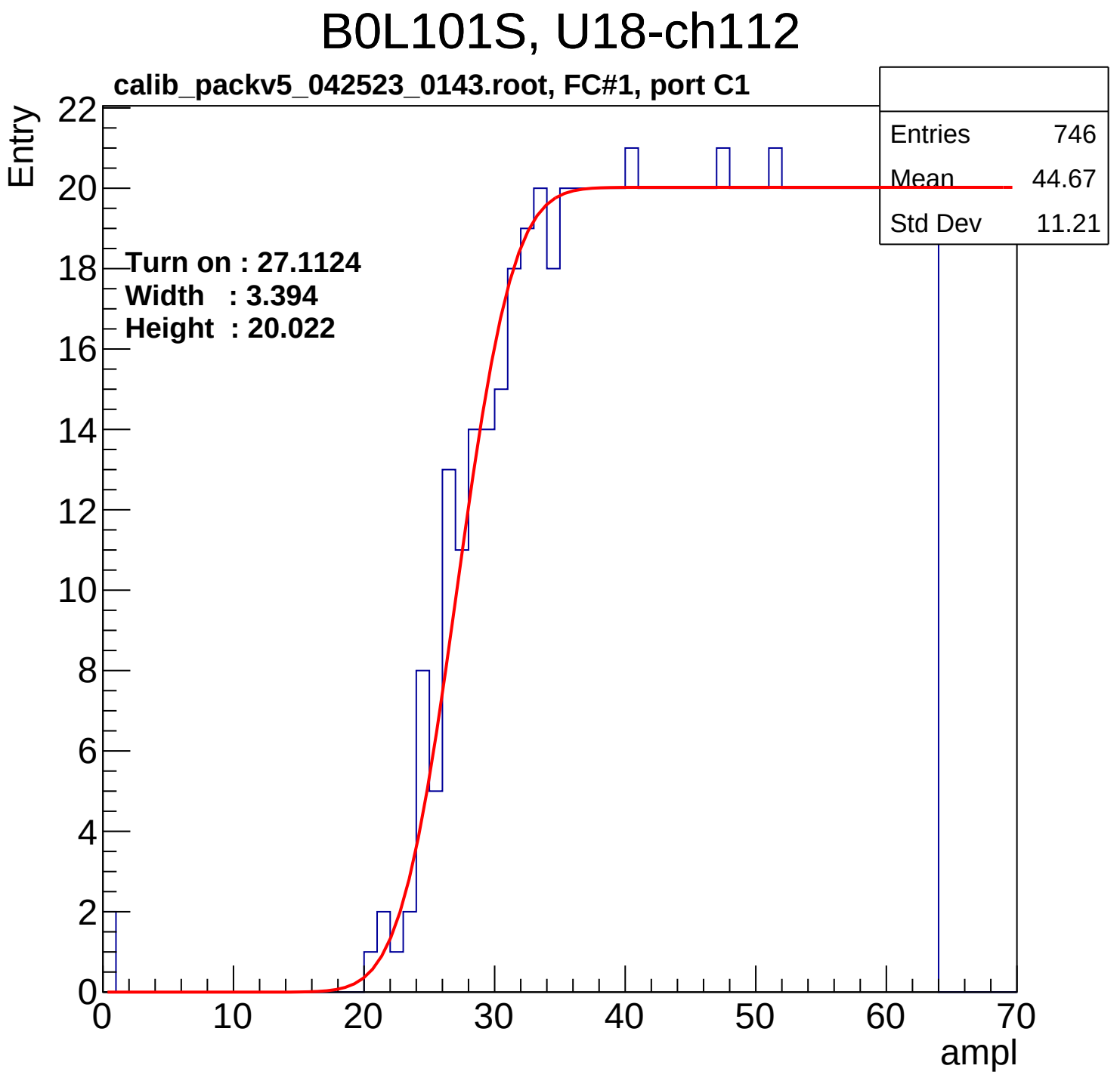
B0L101S, U18-ch112
calib_packv5_042523_0143.root, FC#1, port C1
Entries 746
Mean 44.67
Std Dev 11.21
Turn on : 27.1124
Width : 3.394
Height : 20.022
Entry
ampl
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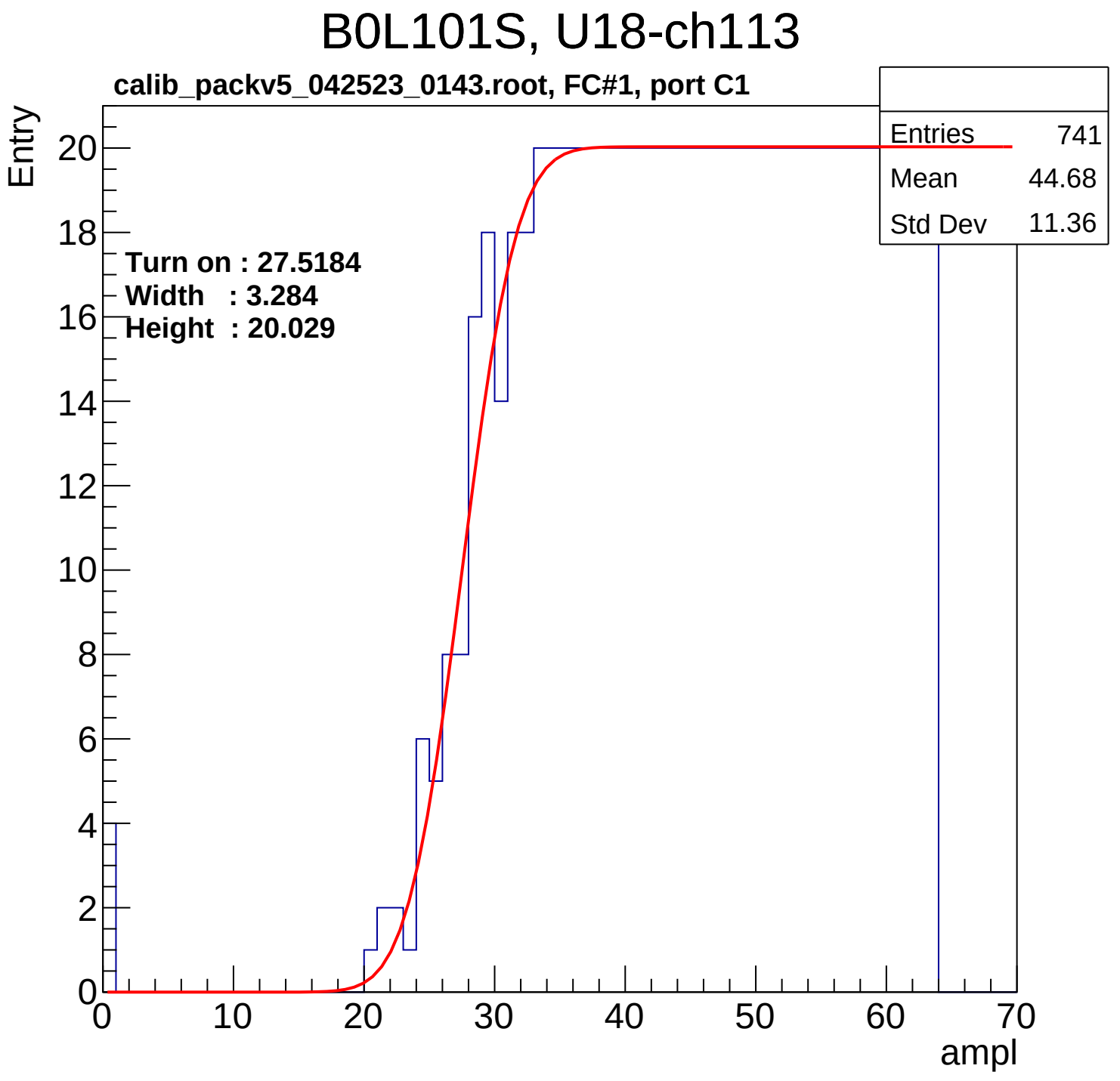
B0L101S, U18-ch113
calib_packv5_042523_0143.root, FC#1, port C1
Entries 741
Mean 44.68
Std Dev 11.36
Turn on : 27.5184
Width : 3.284
Height : 20.029
Entry
ampl
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6
8
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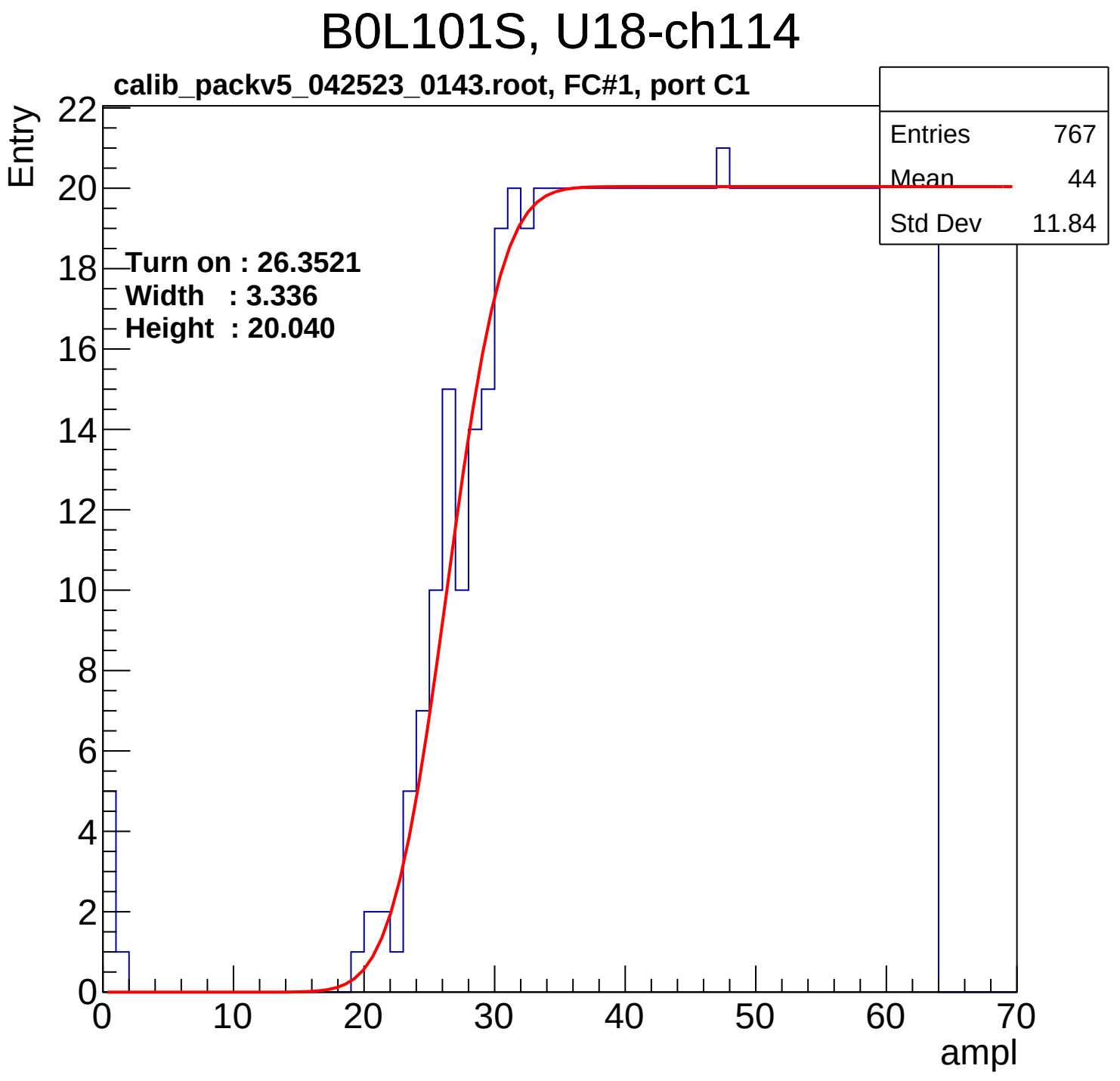
B0L101S, U18-ch114
calib_packv5_042523_0143.root, FC#1, port C1
Entries 767
Mean 44
Std Dev 11.84
Turn on : 26.3521
Width : 3.336
Height : 20.040
Entry
ampl
0
2
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6
8
10
12
14
16
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20
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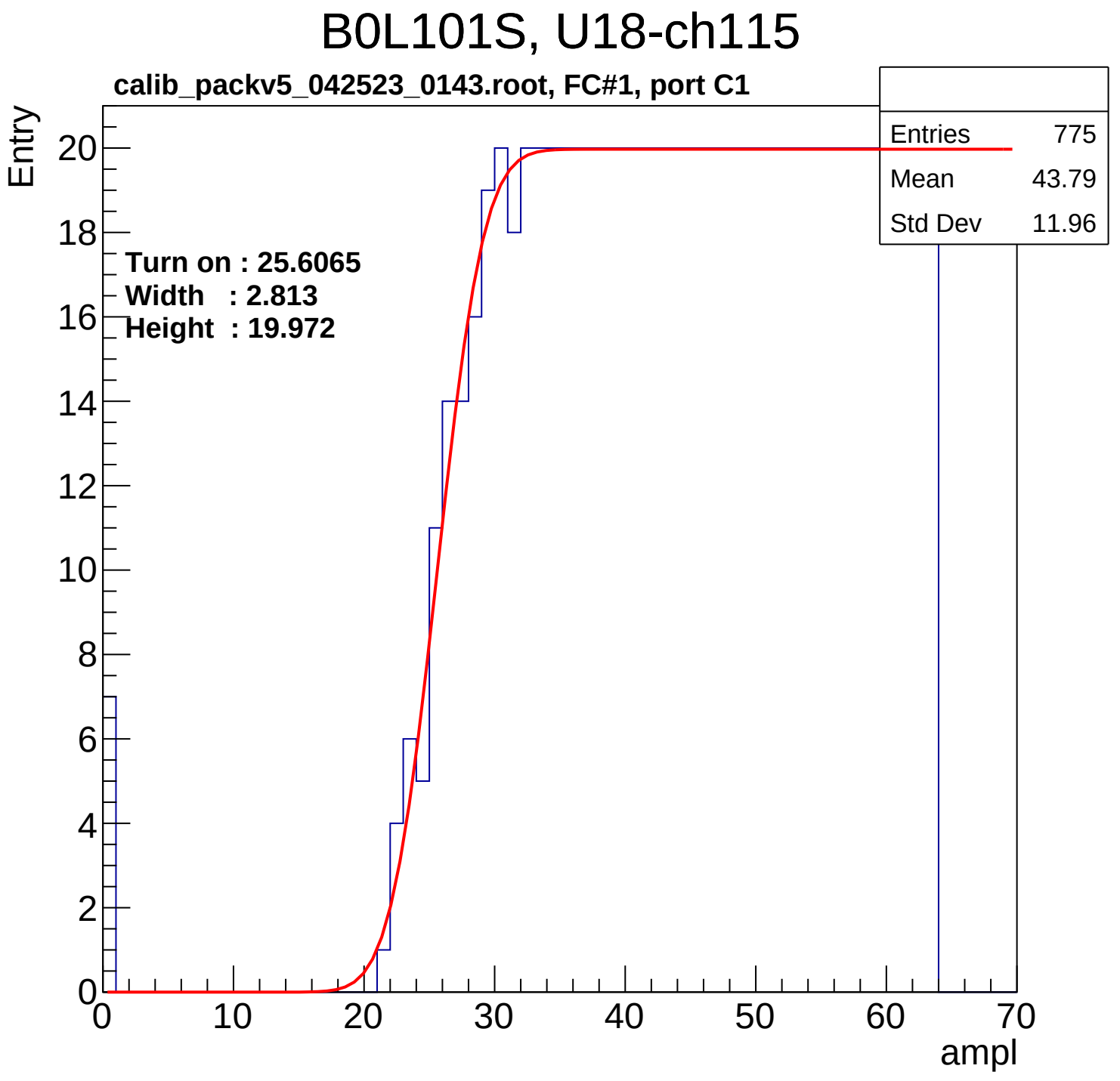
B0L101S, U18-ch115
calib_packv5_042523_0143.root, FC#1, port C1
Entries 775
Mean 43.79
Std Dev 11.96
Turn on : 25.6065
Width : 2.813
Height : 19.972
Entry
ampl
0
2
4
6
8
10
12
14
16
18
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0
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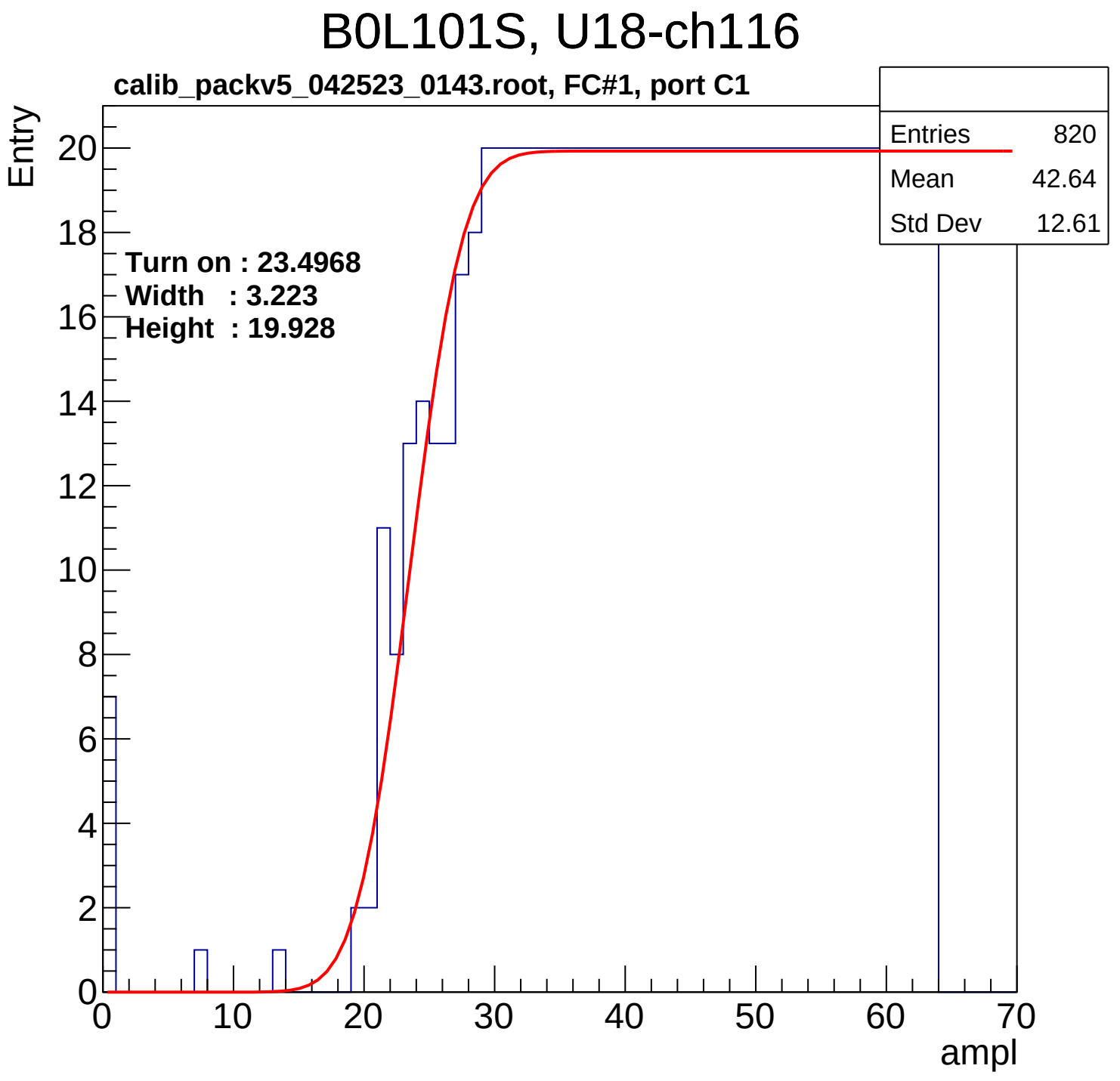
B0L101S, U18-ch116
calib_packv5_042523_0143.root, FC#1, port C1
Entries 820
Mean 42.64
Std Dev 12.61
Turn on : 23.4968
Width : 3.223
Height : 19.928
Entry
ampl
0
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6
8
10
12
14
16
18
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0
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20
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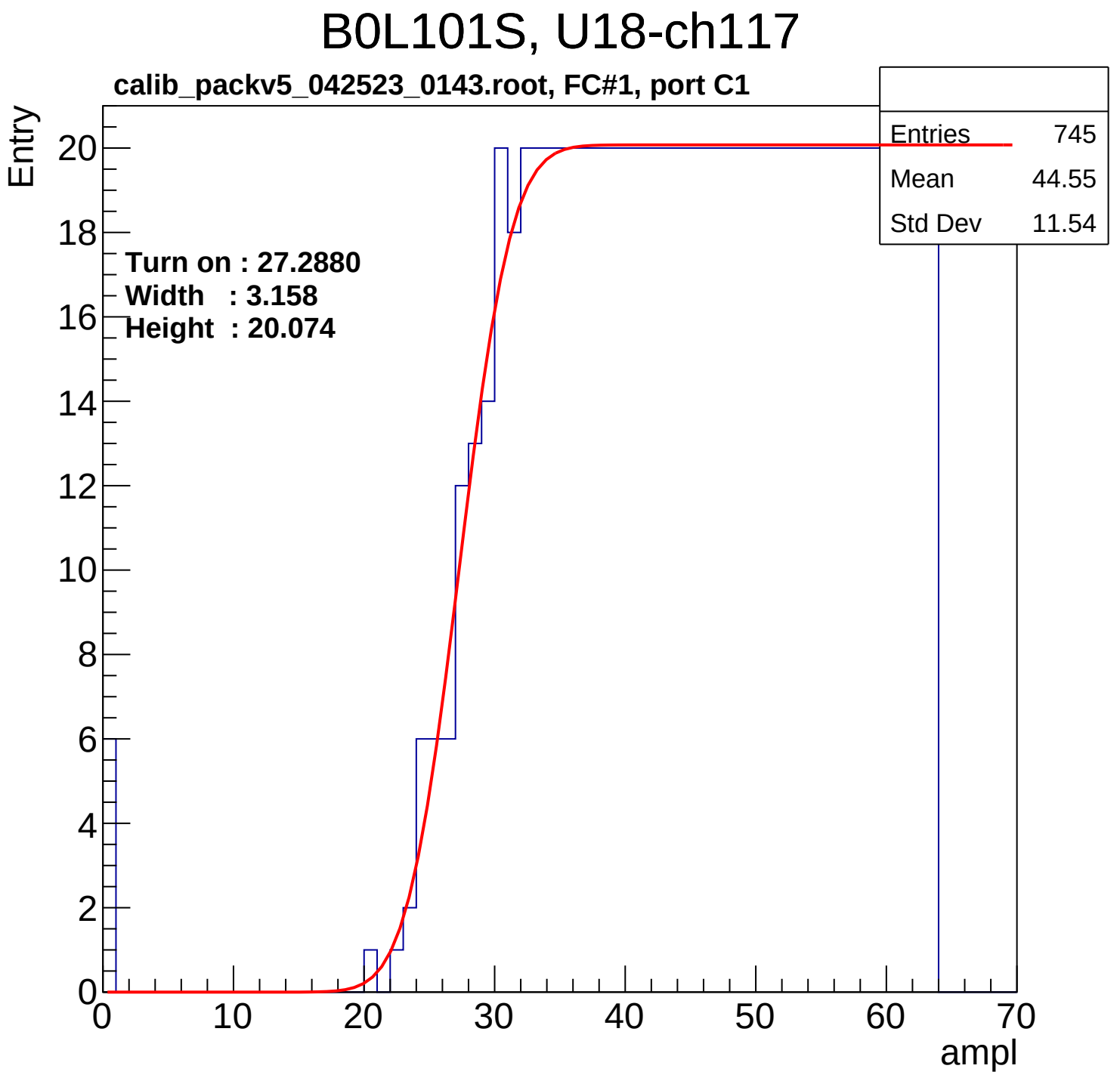
B0L101S, U18-ch117
calib_packv5_042523_0143.root, FC#1, port C1
Entries 745
Mean 44.55
Std Dev 11.54
Turn on : 27.2880
Width : 3.158
Height : 20.074
Entry
ampl
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6
8
10
12
14
16
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0
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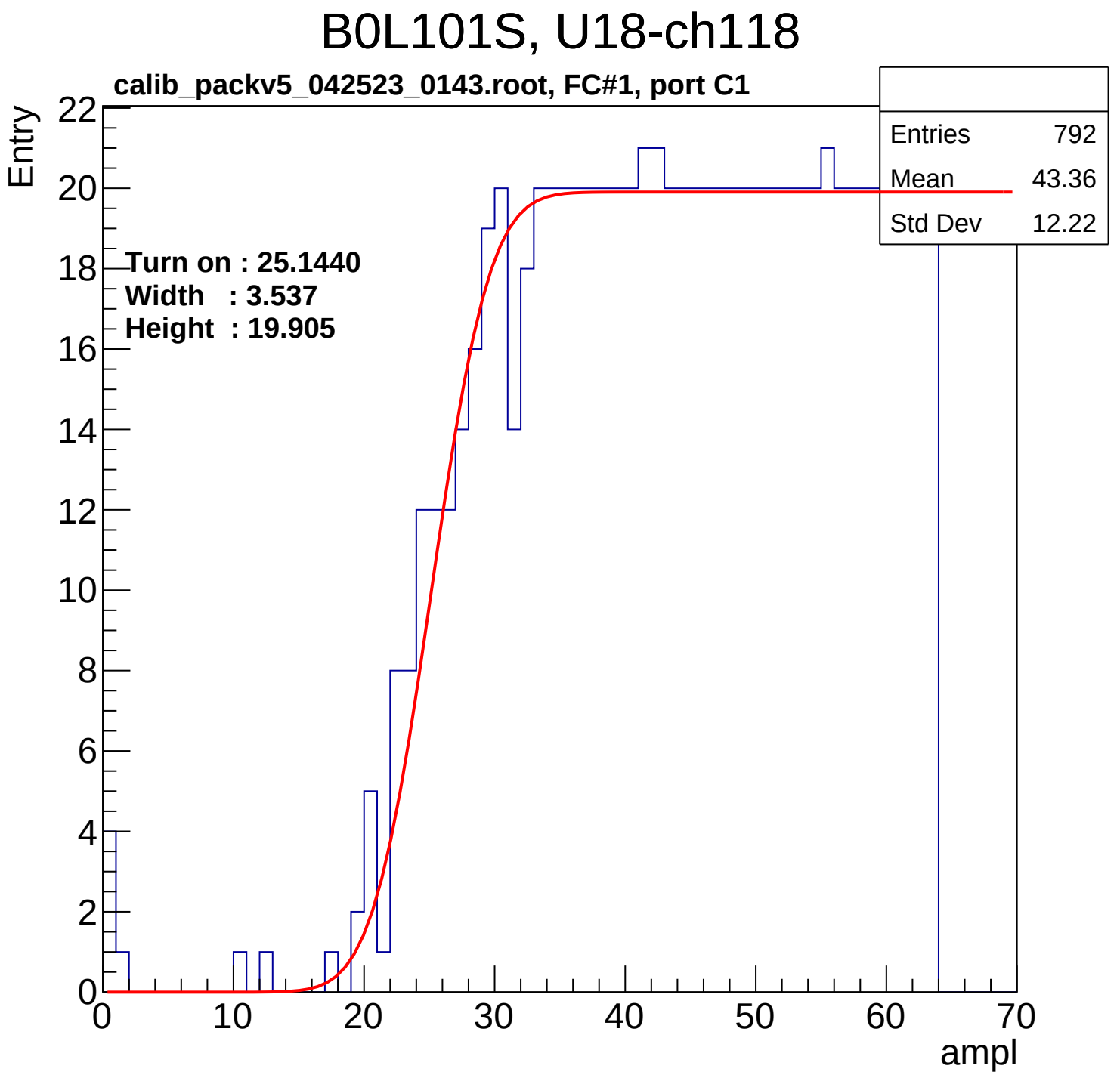
B0L101S, U18-ch118
calib_packv5_042523_0143.root, FC#1, port C1
Entries 792
Mean 43.36
Std Dev 12.22
Turn on : 25.1440
Width : 3.537
Height : 19.905
Entry
ampl
0
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8
10
12
14
16
18
20
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20
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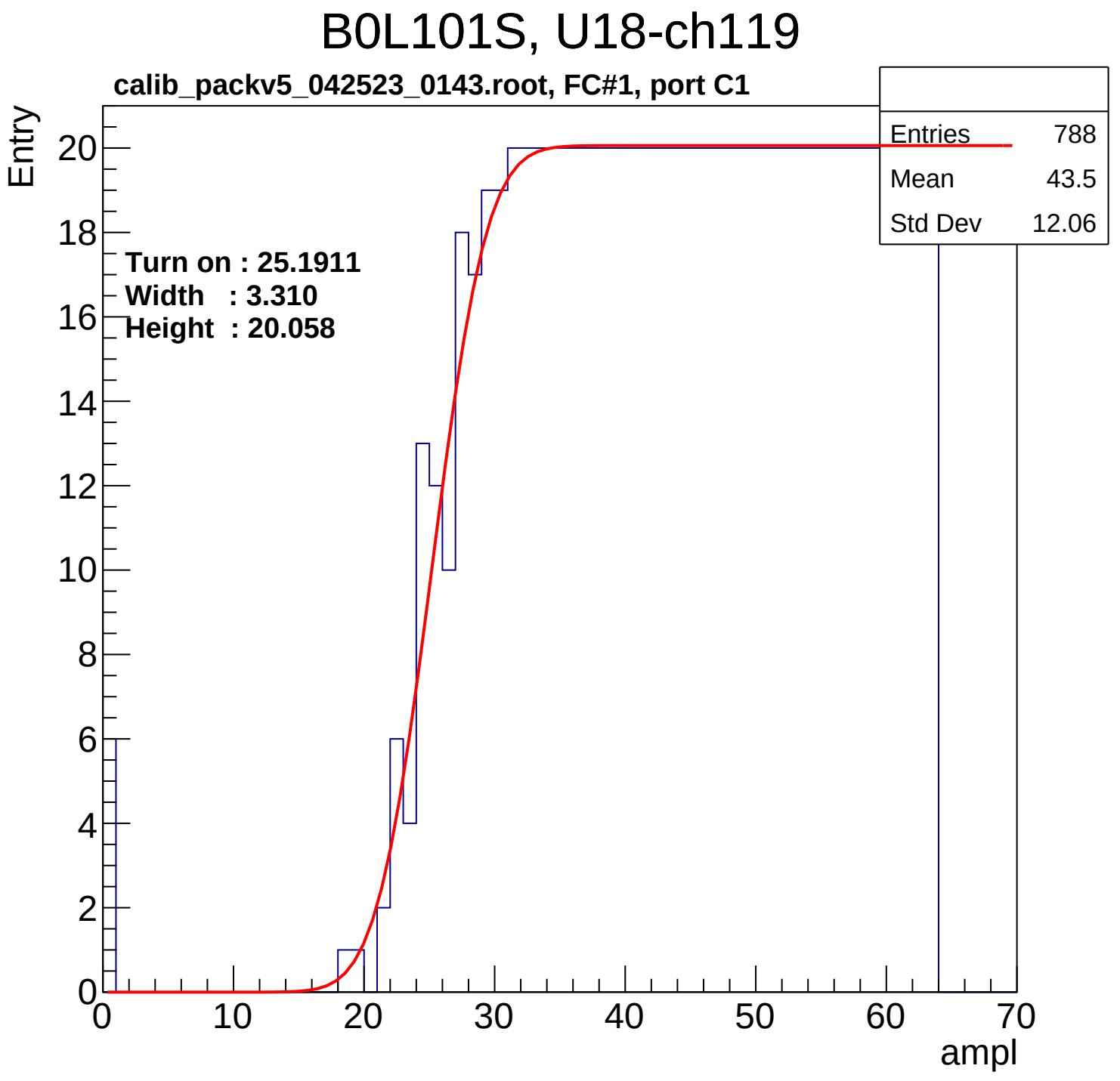
B0L101S, U18-ch119
calib_packv5_042523_0143.root, FC#1, port C1
Entries 788
Mean 43.5
Std Dev 12.06
Turn on : 25.1911
Width : 3.310
Height : 20.058
Entry
ampl
0
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6
8
10
12
14
16
18
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0
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20
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60
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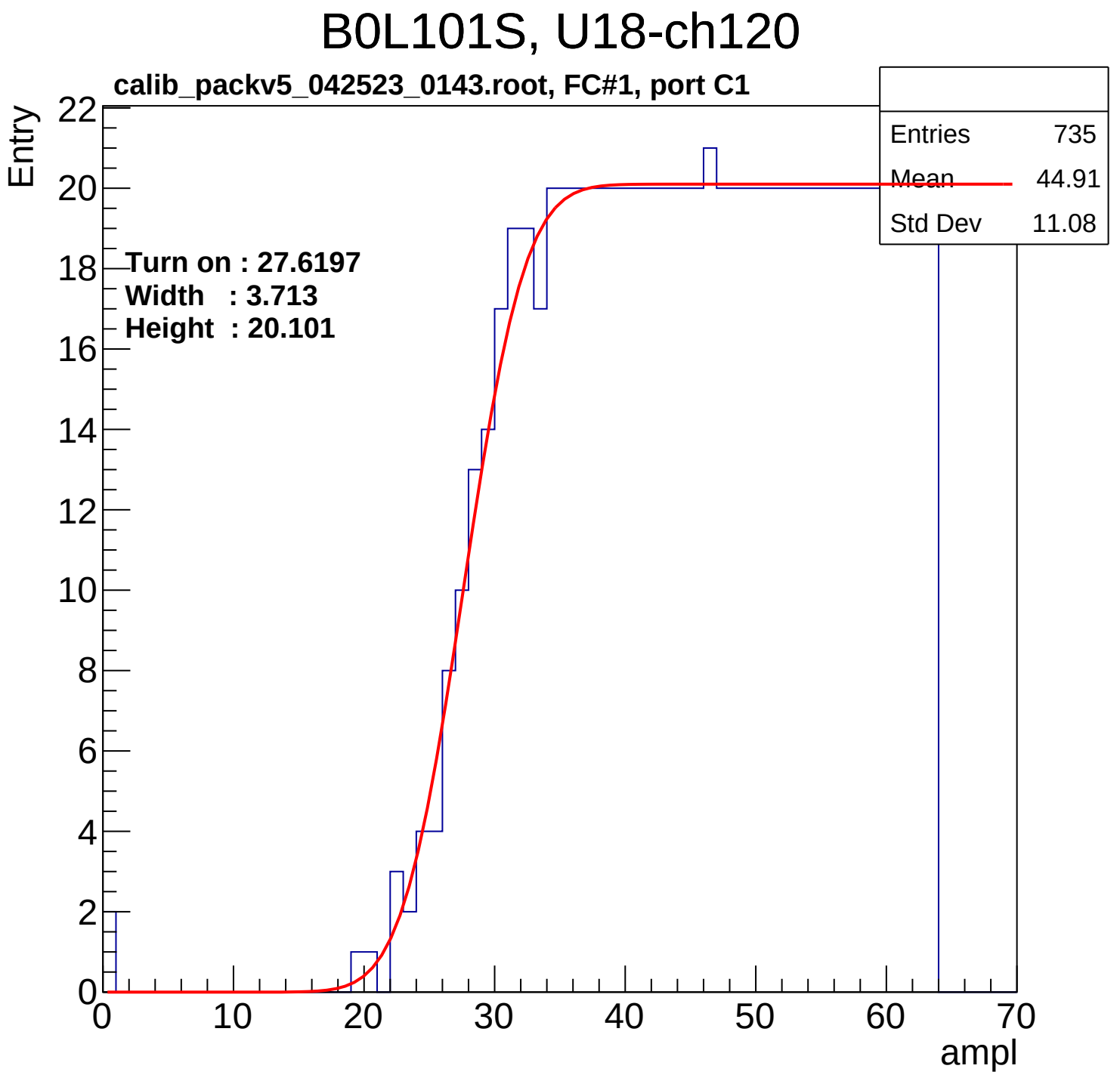
B0L101S, U18-ch120
calib_packv5_042523_0143.root, FC#1, port C1
Entries 735
Mean 44.91
Std Dev 11.08
Turn on : 27.6197
Width : 3.713
Height : 20.101
Entry
ampl
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8
10
12
14
16
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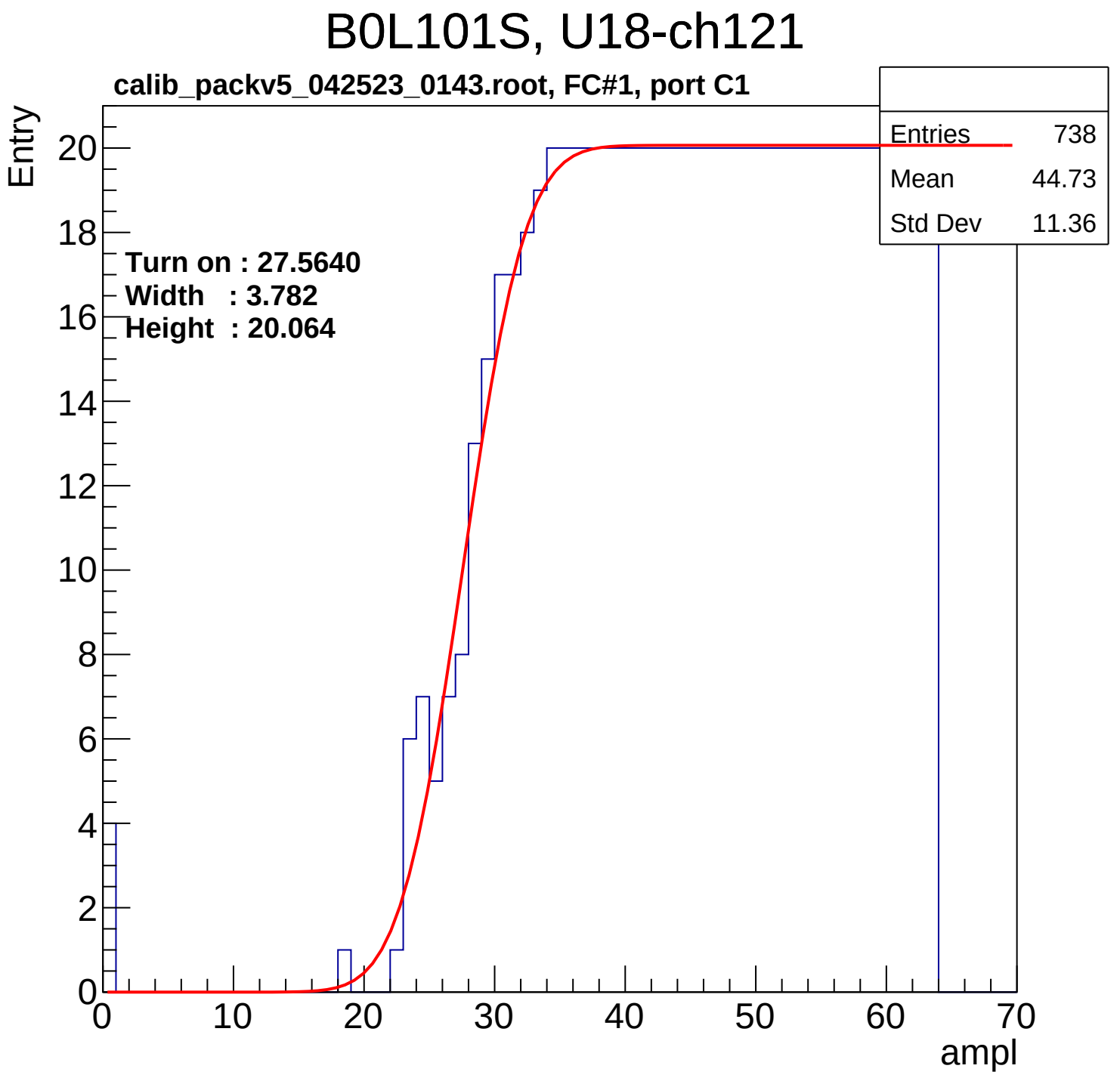
B0L101S, U18-ch121
calib_packv5_042523_0143.root, FC#1, port C1
Entries 738
Mean 44.73
Std Dev 11.36
Turn on : 27.5640
Width : 3.782
Height : 20.064
Entry
ampl
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6
8
10
12
14
16
18
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0
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20
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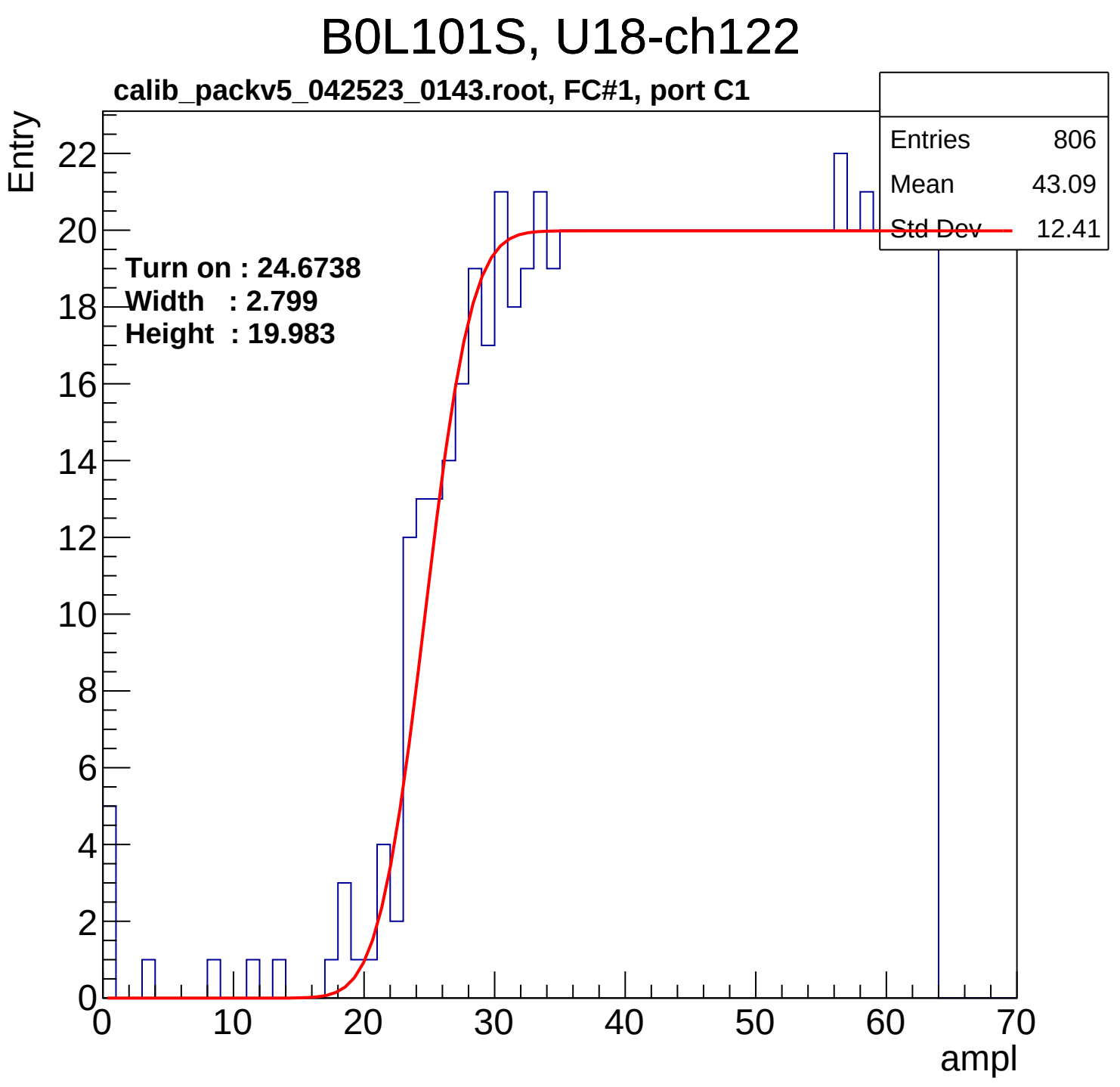
B0L101S, U18-ch122
calib_packv5_042523_0143.root, FC#1, port C1
Entries 806
Mean 43.09
Std Dev 12.41
Turn on : 24.6738
Width : 2.799
Height : 19.983
Entry
ampl
0
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6
8
10
12
14
16
18
20
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0
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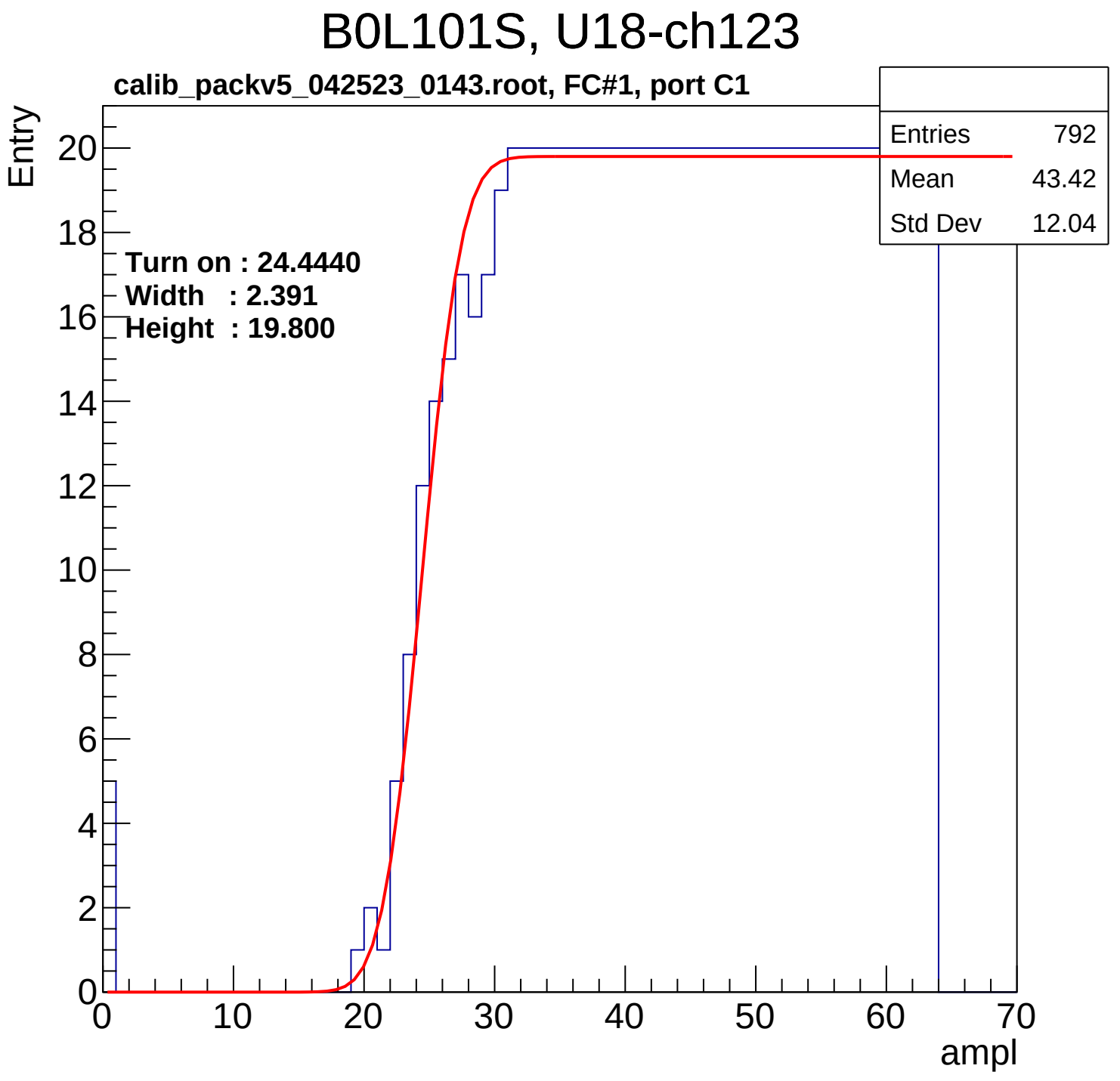
B0L101S, U18-ch123
calib_packv5_042523_0143.root, FC#1, port C1
Entries 792
Mean 43.42
Std Dev 12.04
Turn on : 24.4440
Width : 2.391
Height : 19.800
Entry
ampl
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6
8
10
12
14
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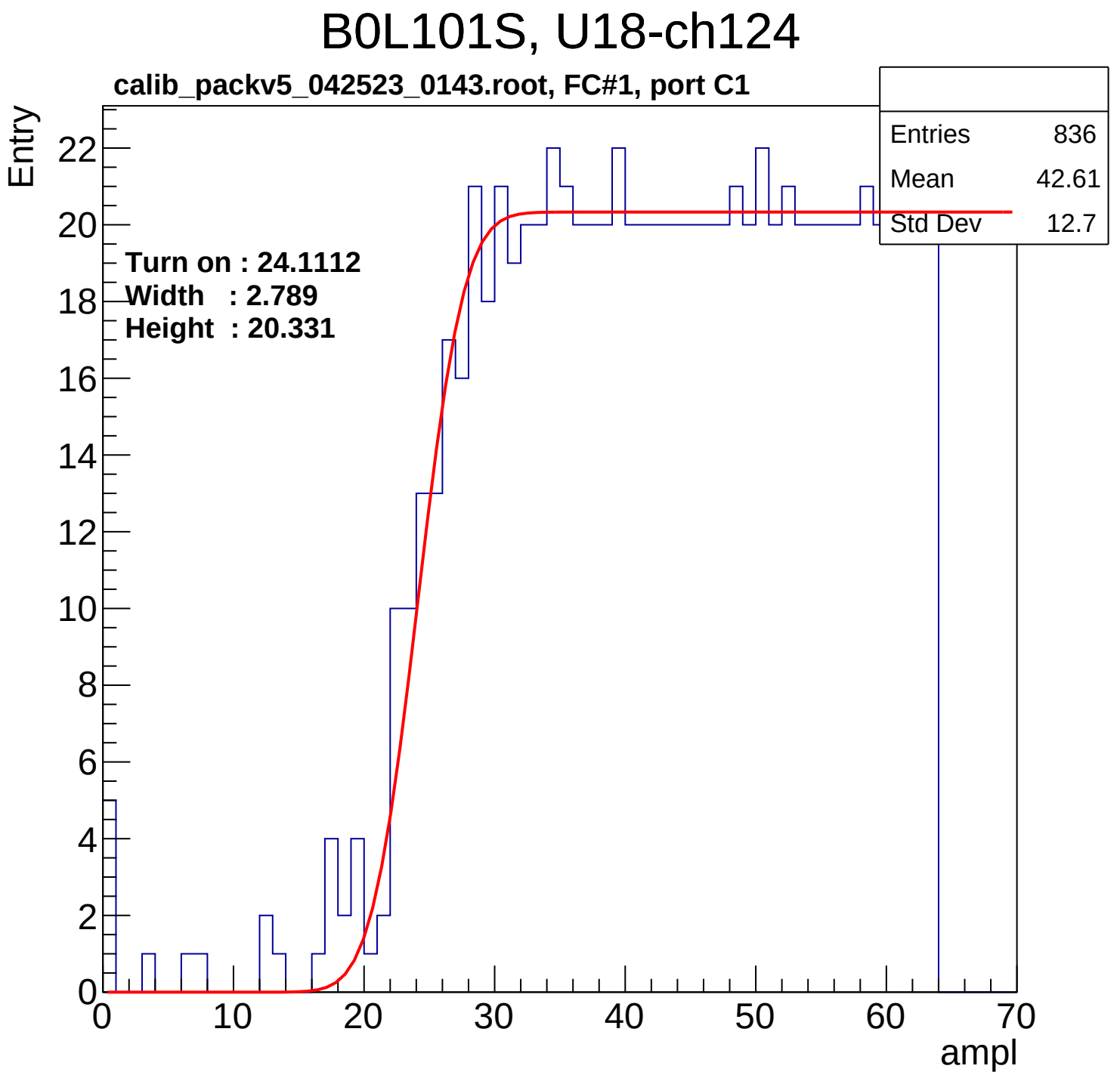
B0L101S, U18-ch124
calib_packv5_042523_0143.root, FC#1, port C1
Entries 836
Mean 42.61
Std Dev 12.7
Turn on : 24.1112
Width : 2.789
Height : 20.331
Entry
ampl
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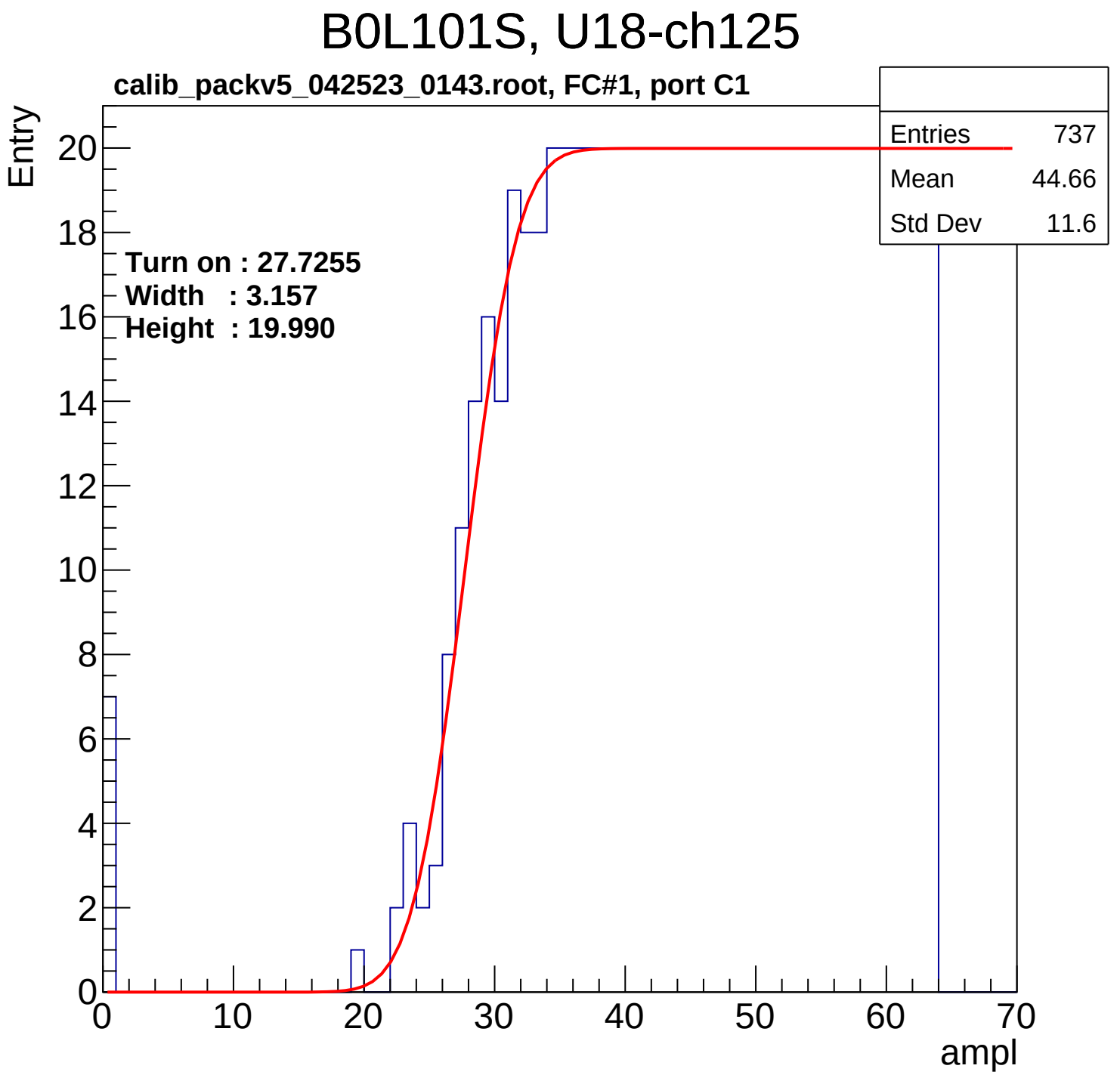
B0L101S, U18-ch125
calib_packv5_042523_0143.root, FC#1, port C1
Entries 737
Mean 44.66
Std Dev 11.6
Turn on : 27.7255
Width : 3.157
Height : 19.990
Entry
ampl
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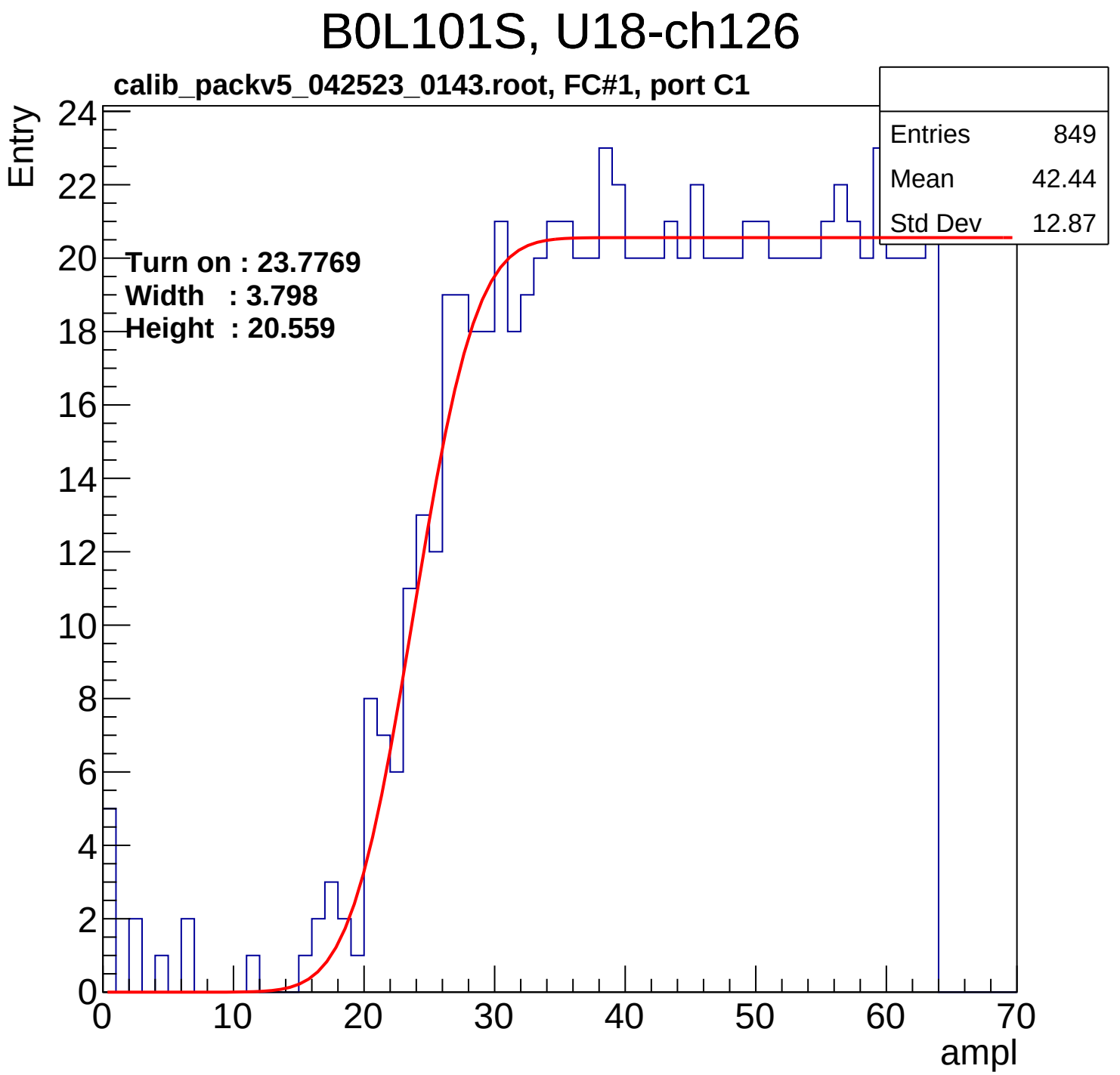
B0L101S, U18-ch126
calib_packv5_042523_0143.root, FC#1, port C1
Entries 849
Mean 42.44
Std Dev 12.87
Turn on : 23.7769
Width : 3.798
Height : 20.559
Entry
ampl
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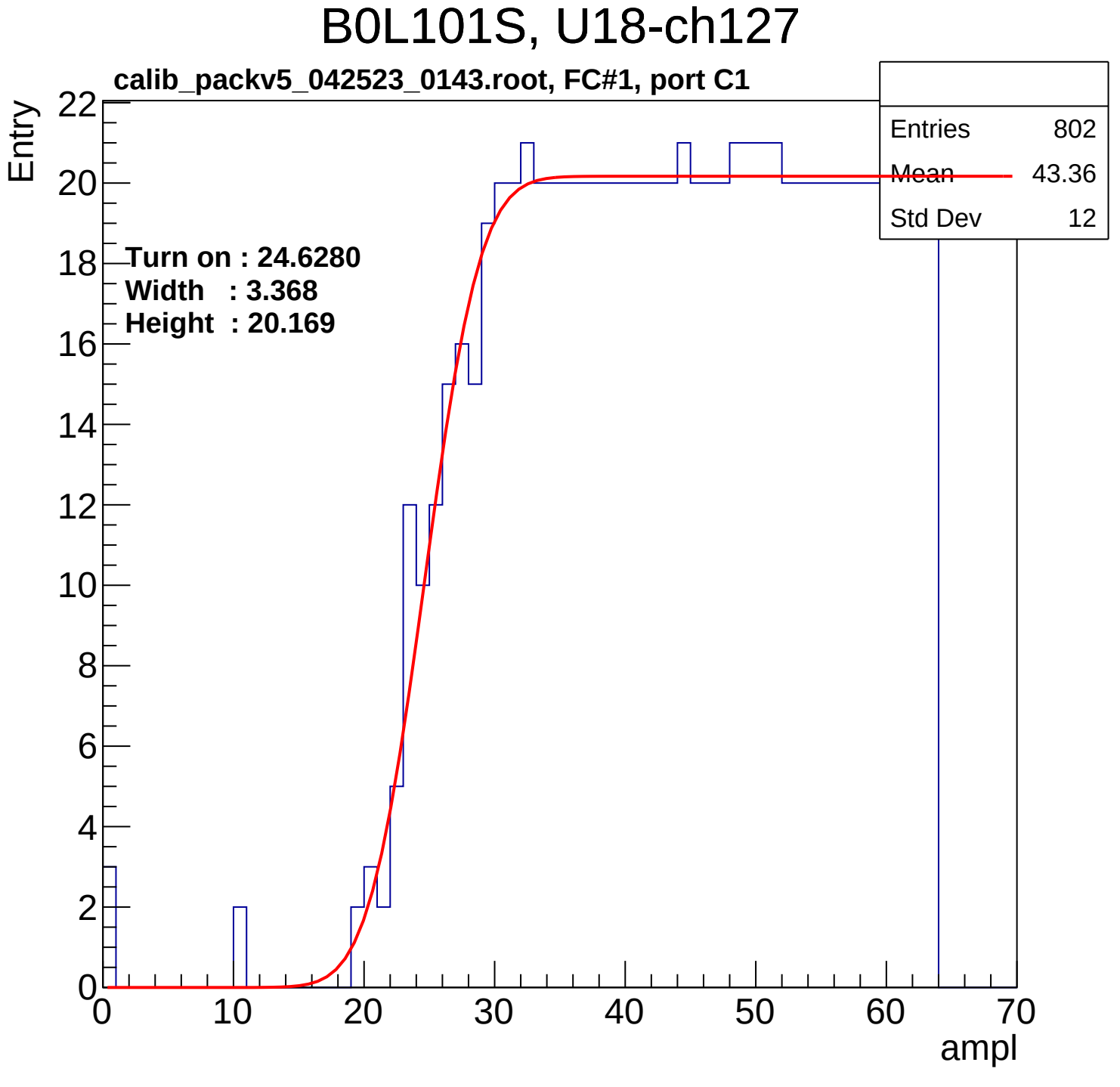
B0L101S, U18-ch127
calib_packv5_042523_0143.root, FC#1, port C1
Entries 802
Mean 43.36
Std Dev 12
Turn on : 24.6280
Width : 3.368
Height : 20.169
Entry
ampl
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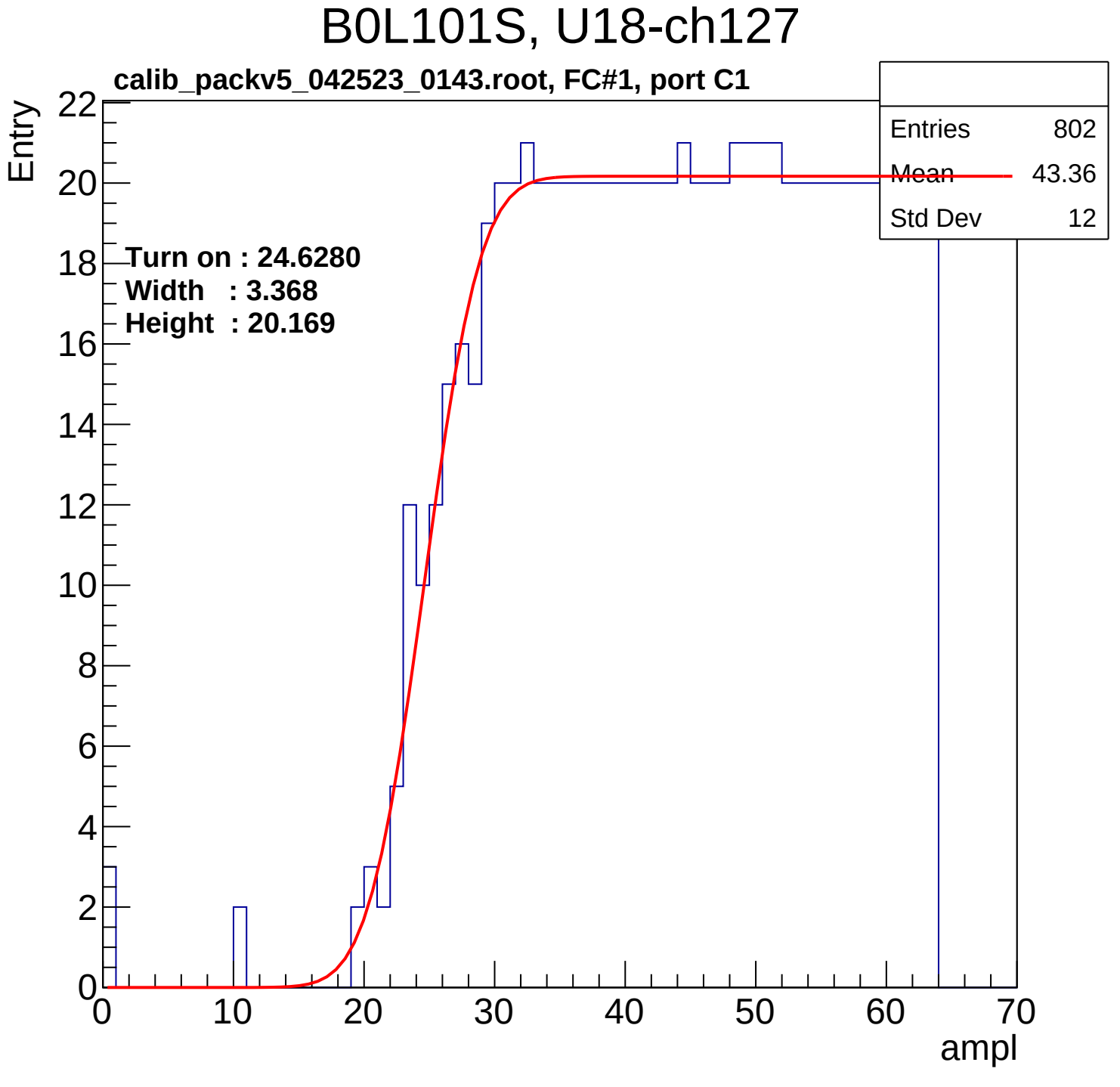
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calib_packv5_042523_0143.root, FC#1, port C1
Entries 802
Mean 43.36
Std Dev 12
Turn on : 24.6280
Width : 3.368
Height : 20.169
Entry
ampl
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