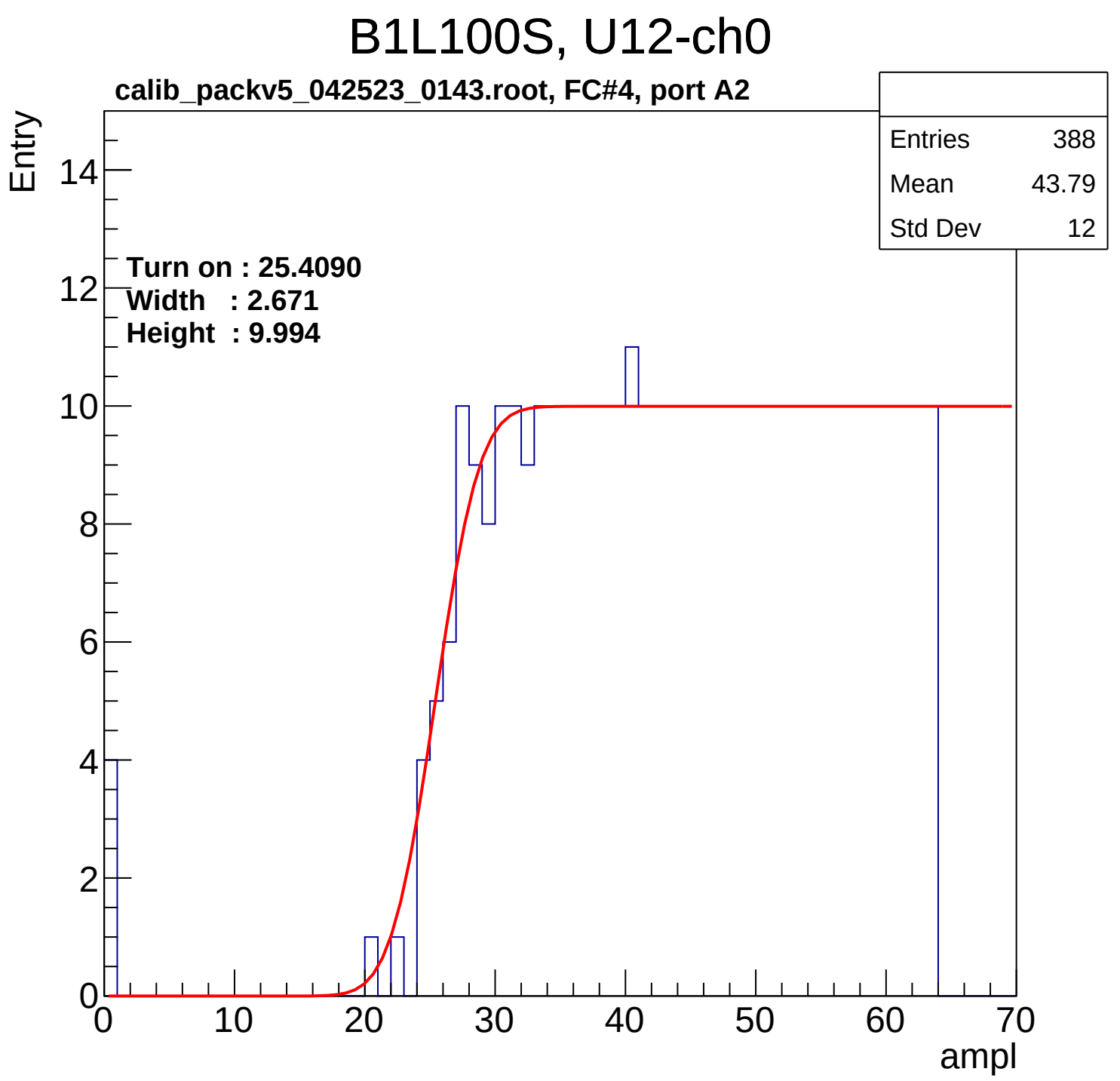
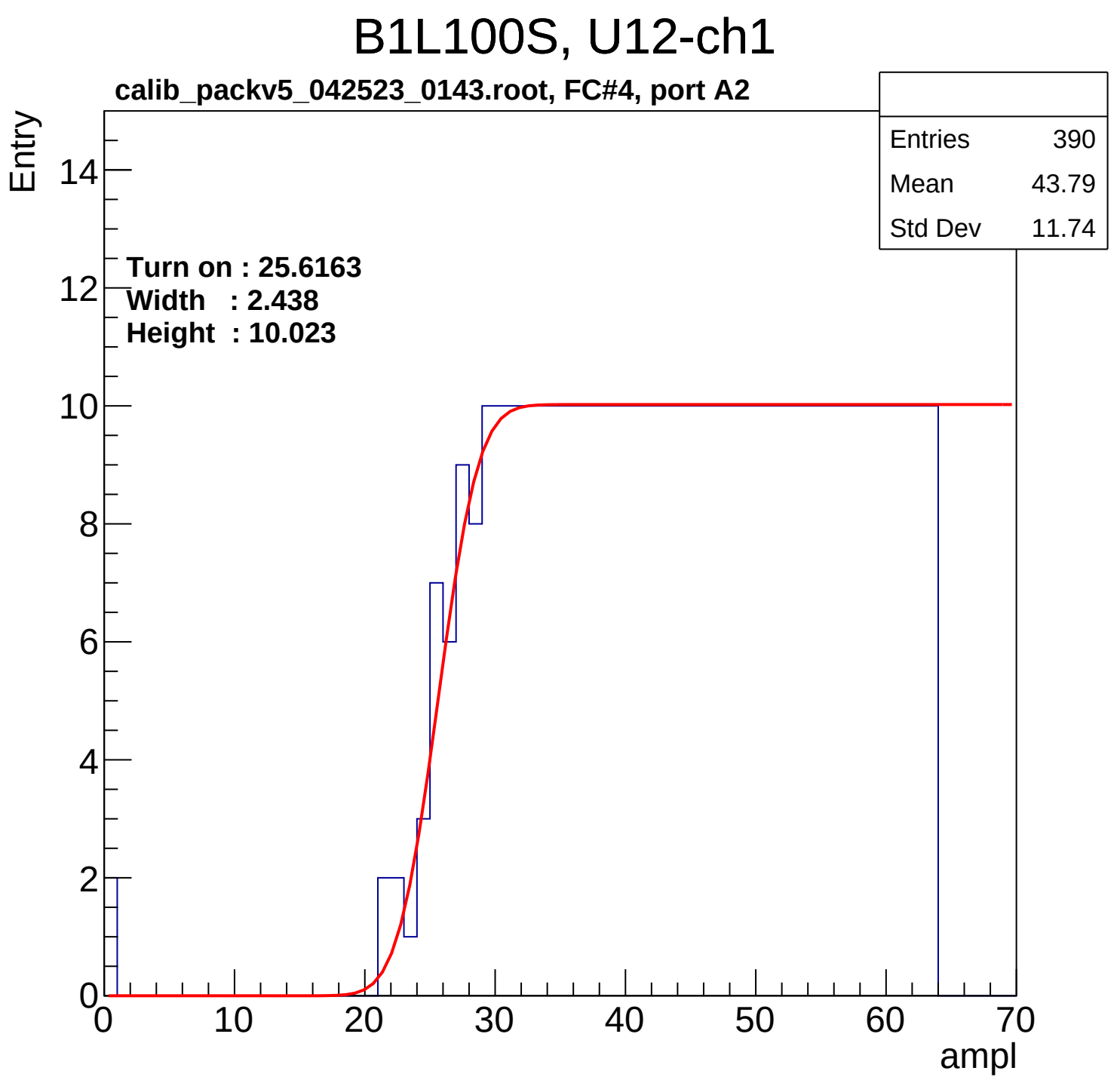
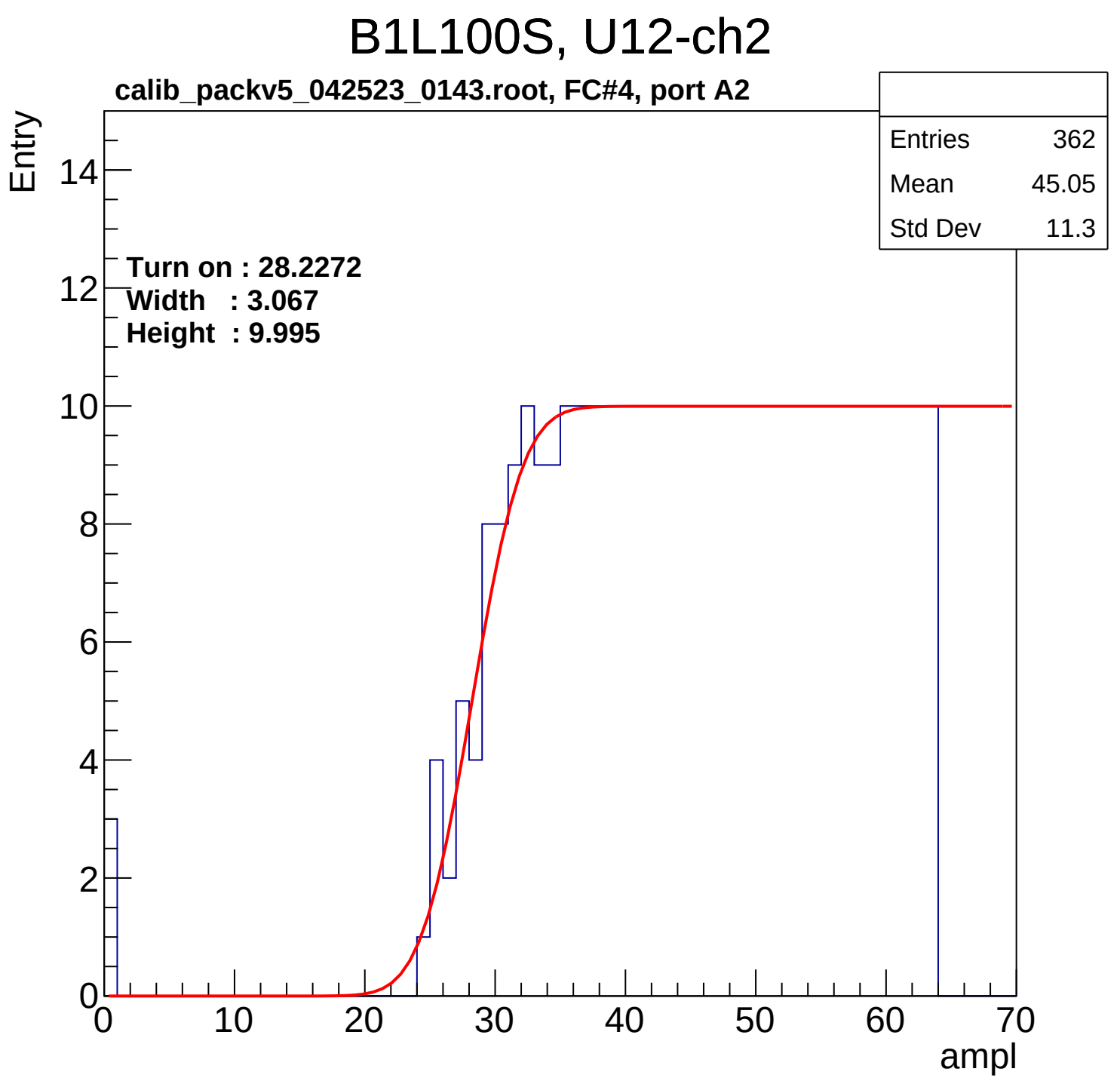
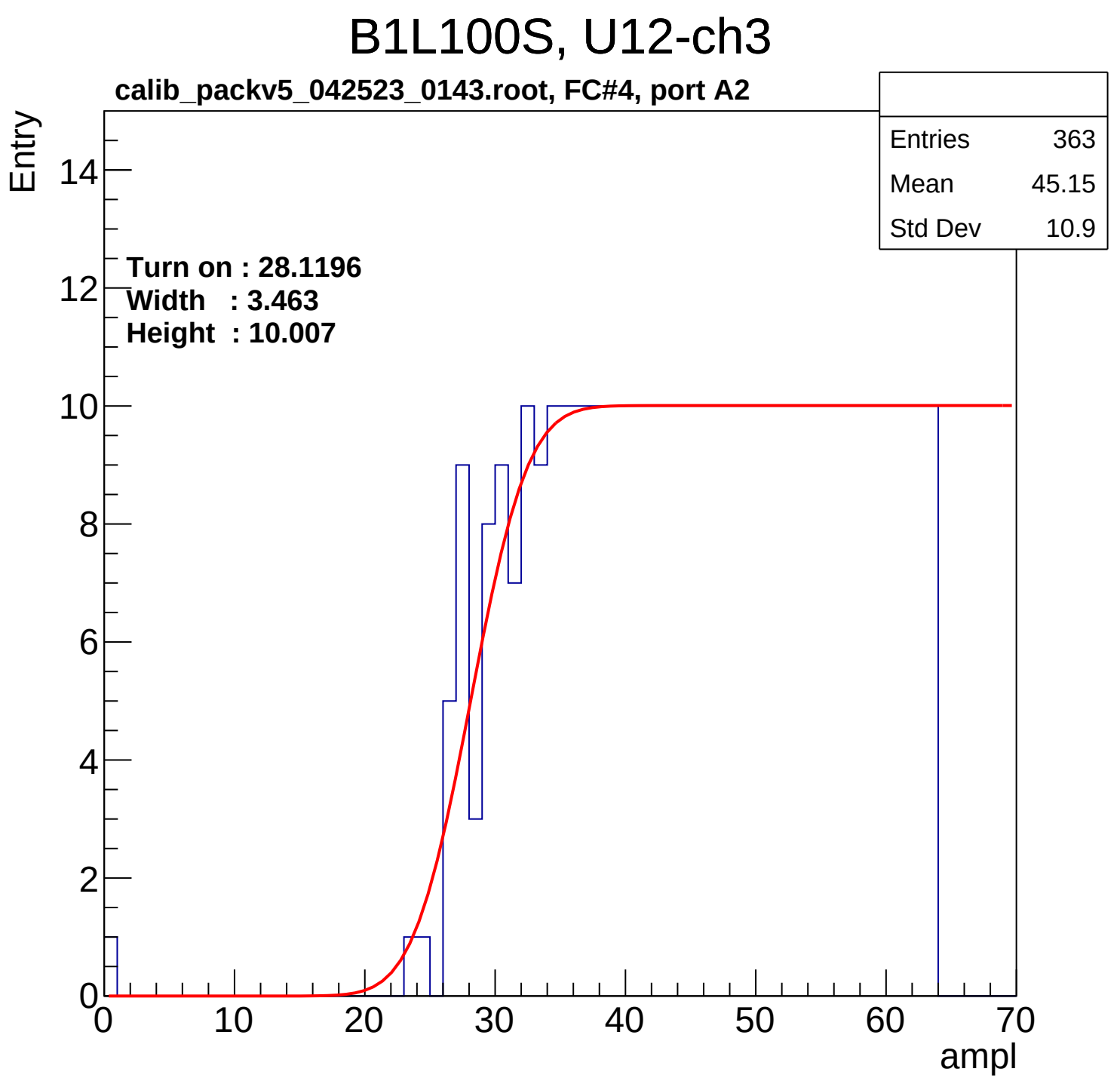
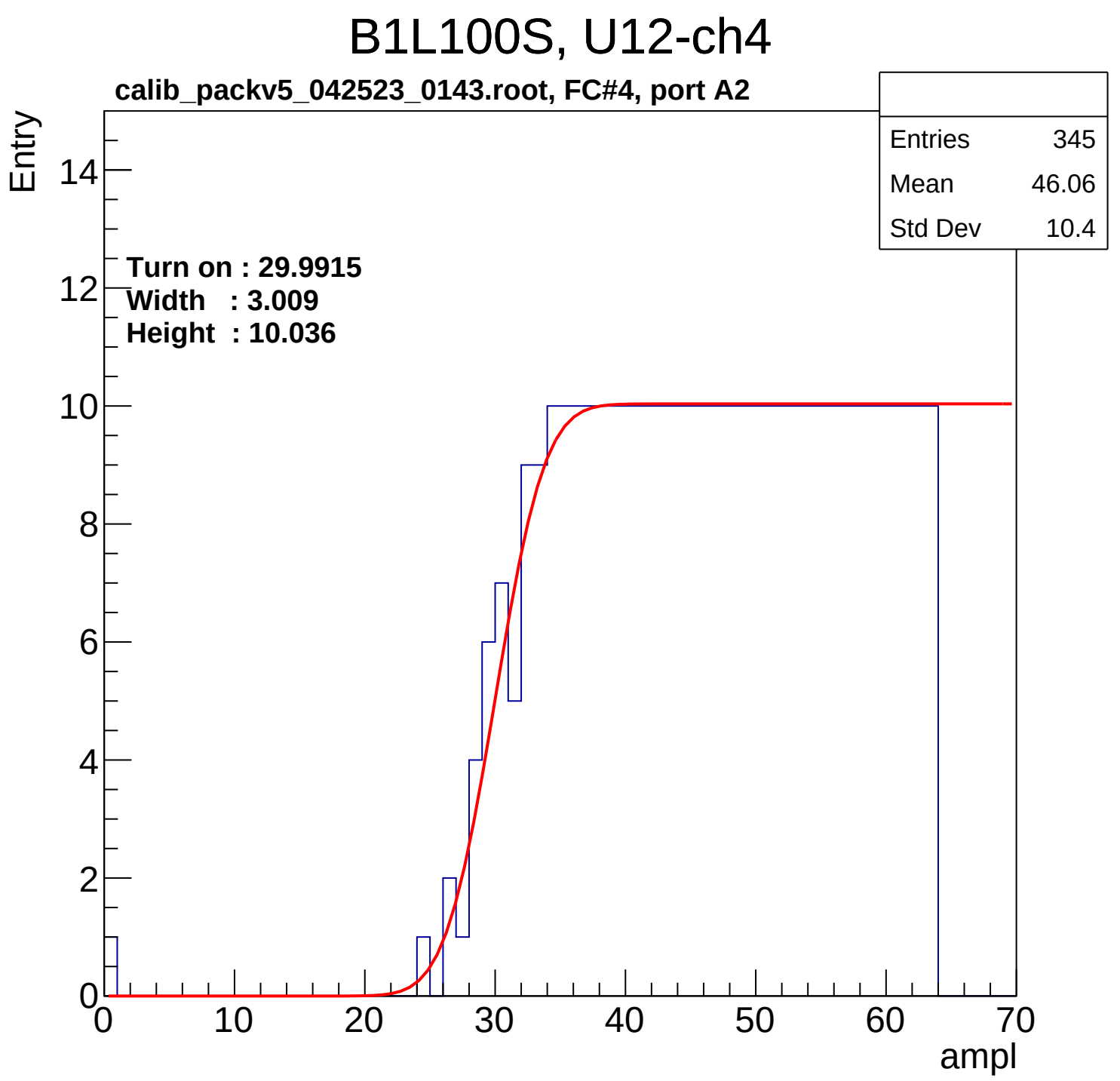
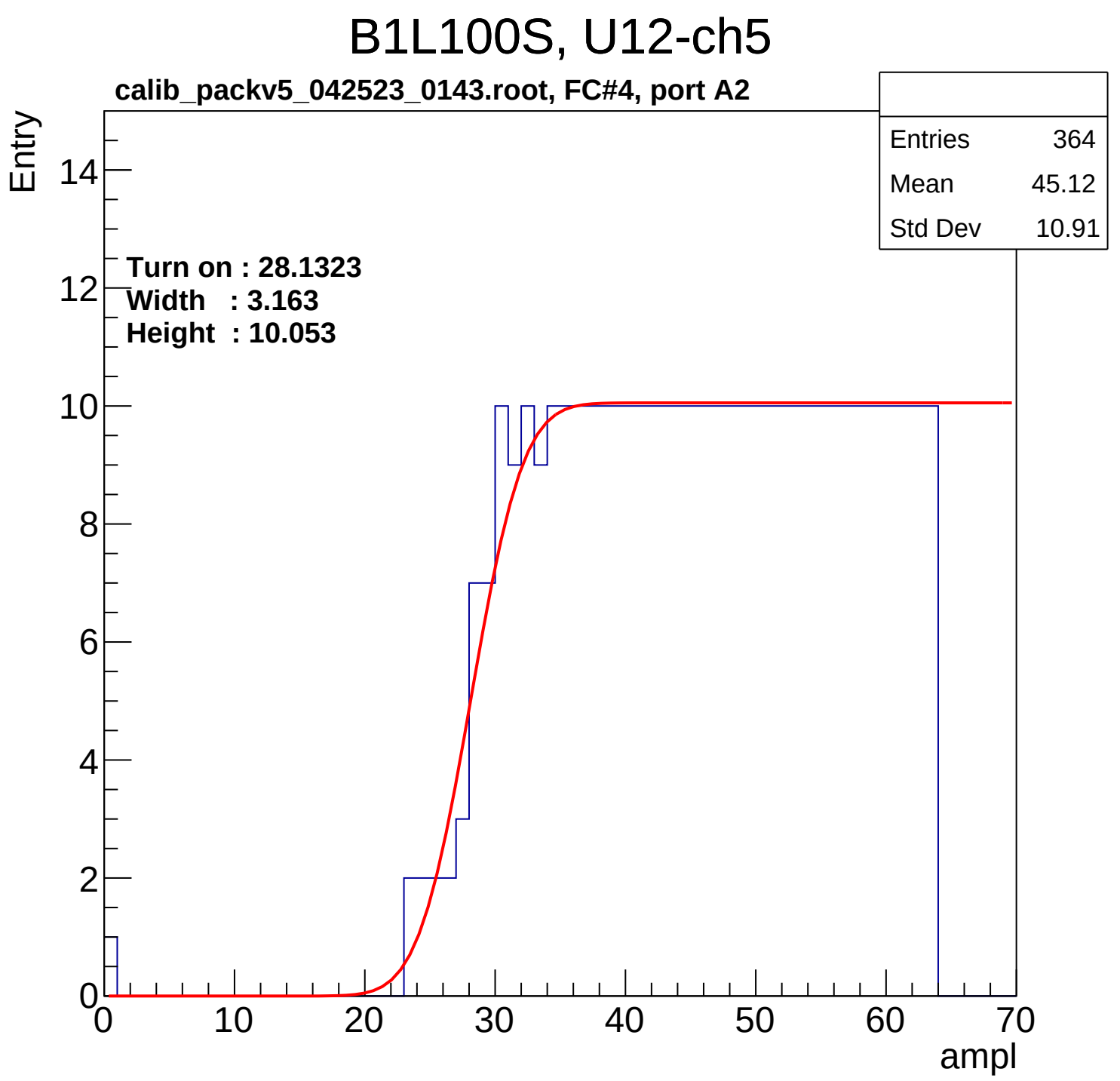

B1L100S, U12-ch0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 388
Mean 43.79
Std Dev 12
Turn on : 25.4090
Width : 2.671
Height : 9.994
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

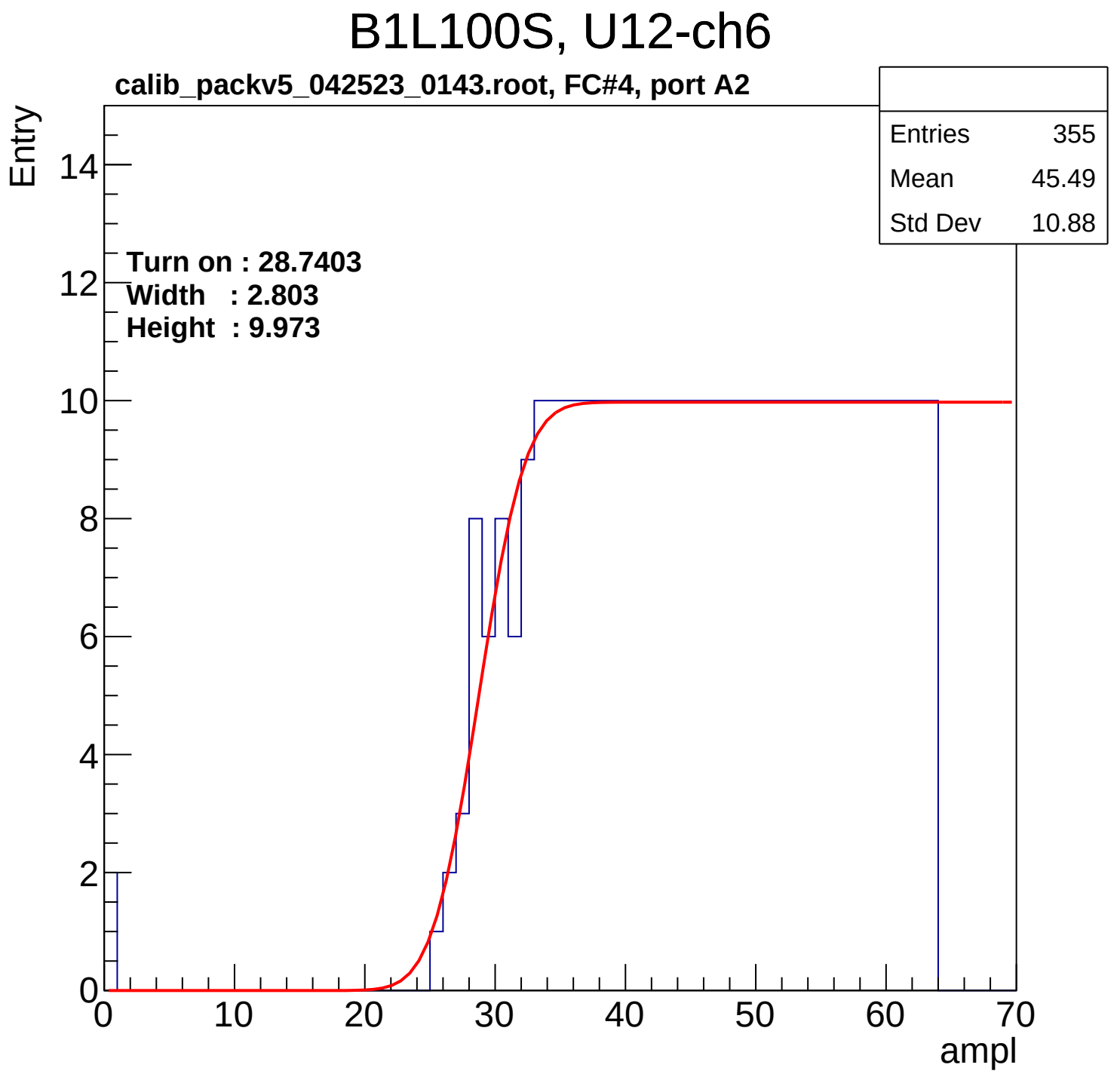

B1L100S, U12-ch1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 390
Mean 43.79
Std Dev 11.74
Turn on : 25.6163
Width : 2.438
Height : 10.023
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

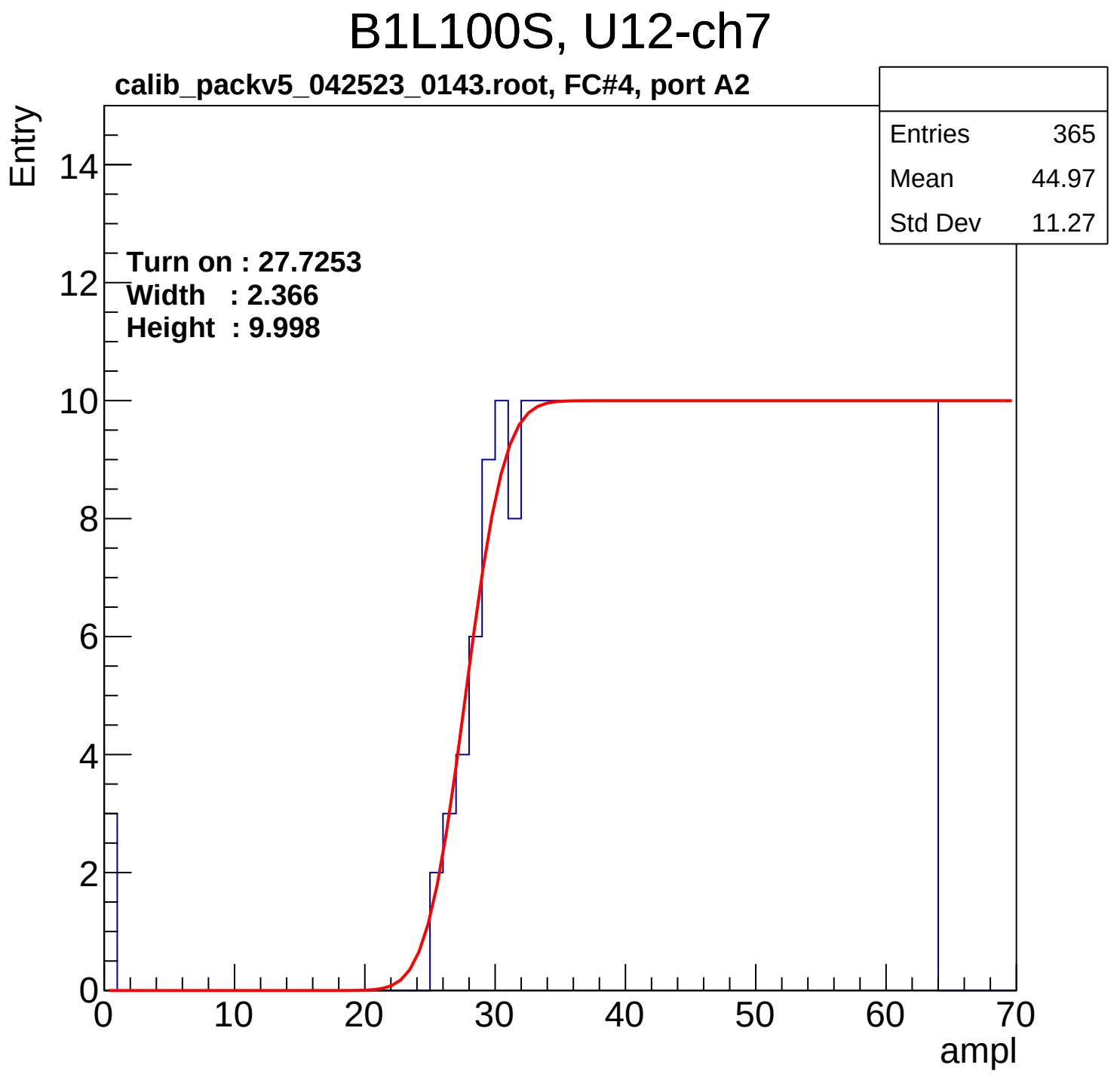

B1L100S, U12-ch2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 362
Mean 45.05
Std Dev 11.3
Turn on : 28.2272
Width : 3.067
Height : 9.995
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

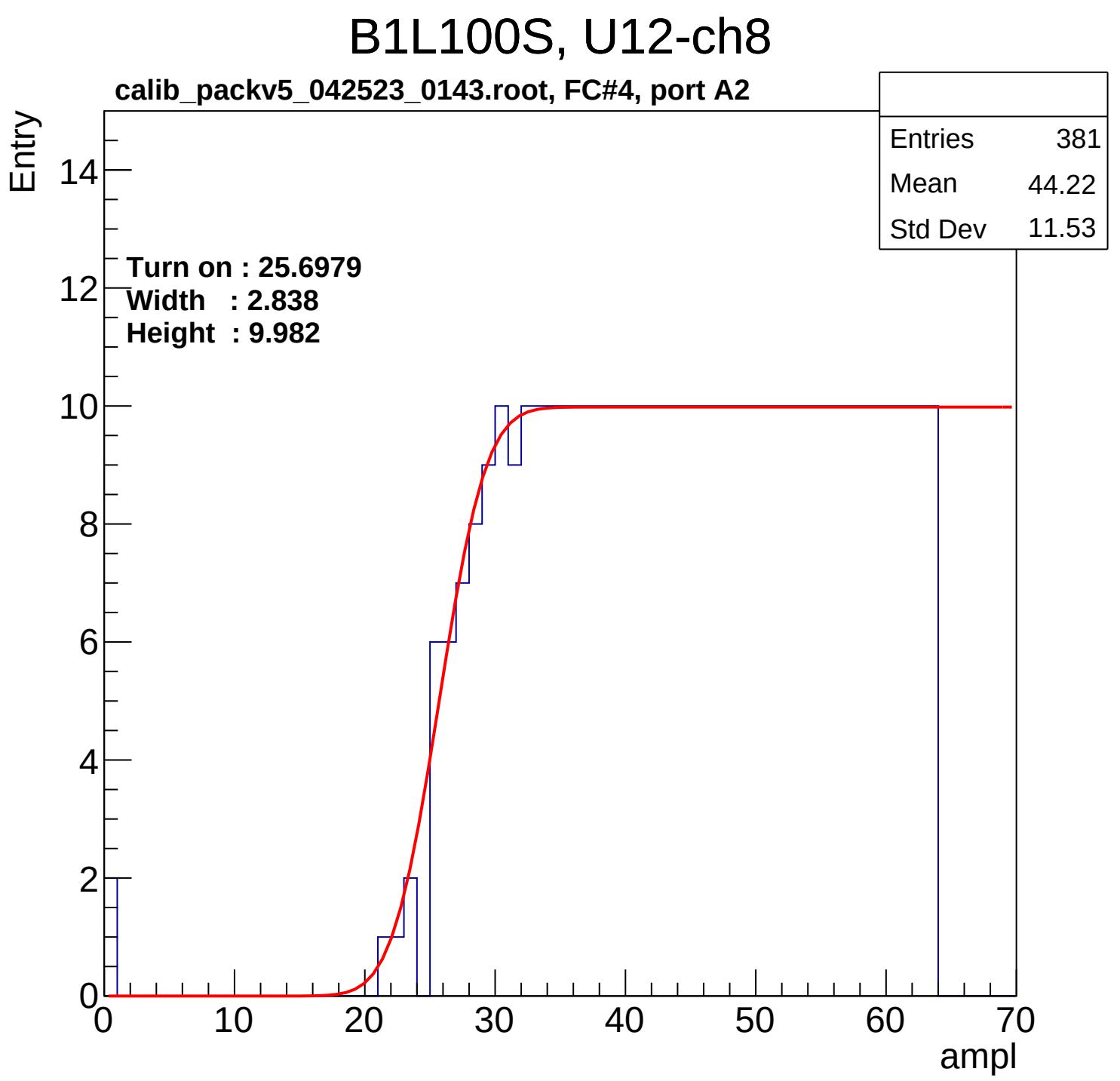

B1L100S, U12-ch3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 363
Mean 45.15
Std Dev 10.9
Turn on : 28.1196
Width : 3.463
Height : 10.007
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

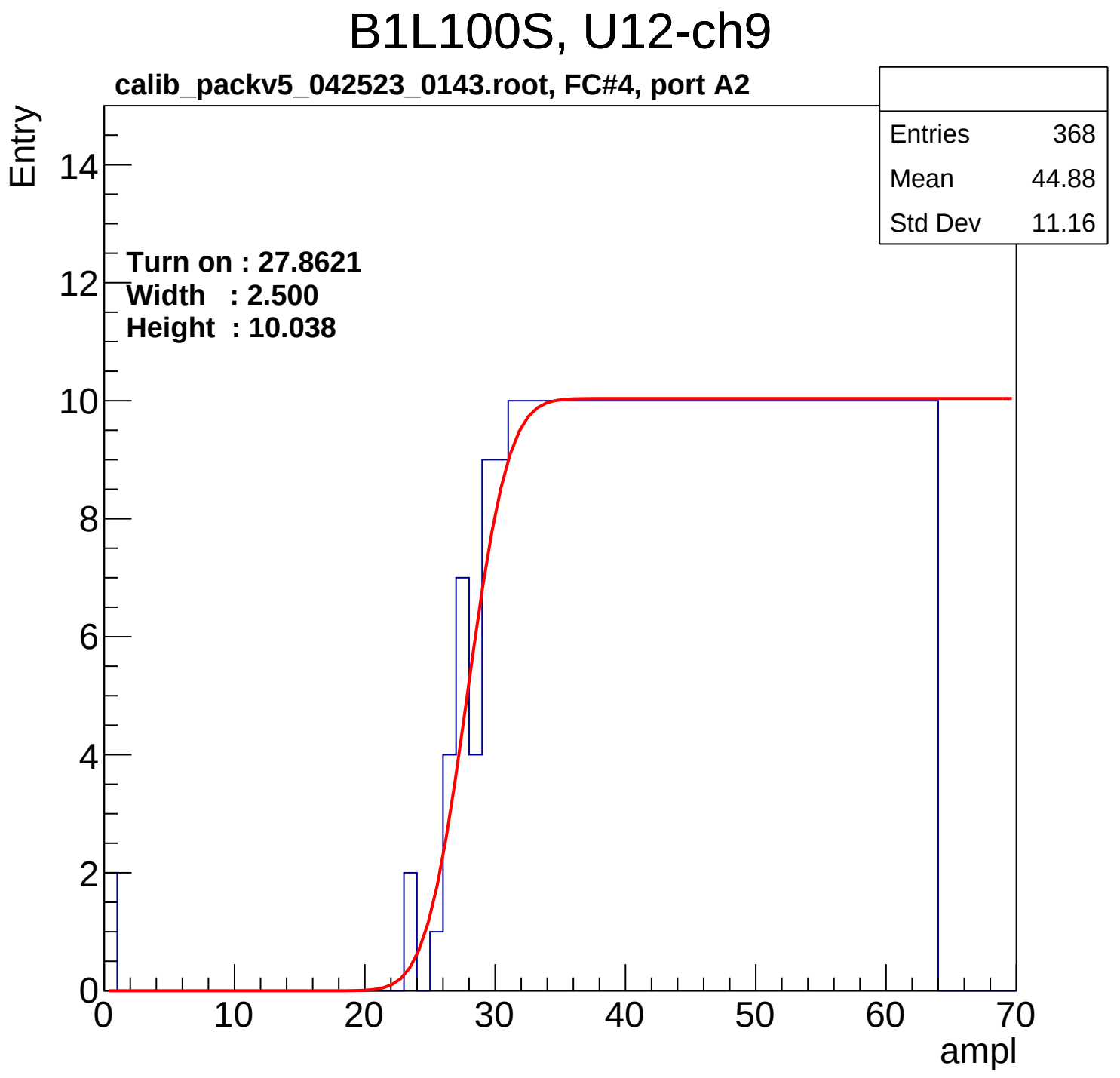

B1L100S, U12-ch4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 345
Mean 46.06
Std Dev 10.4
Turn on : 29.9915
Width : 3.009
Height : 10.036
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

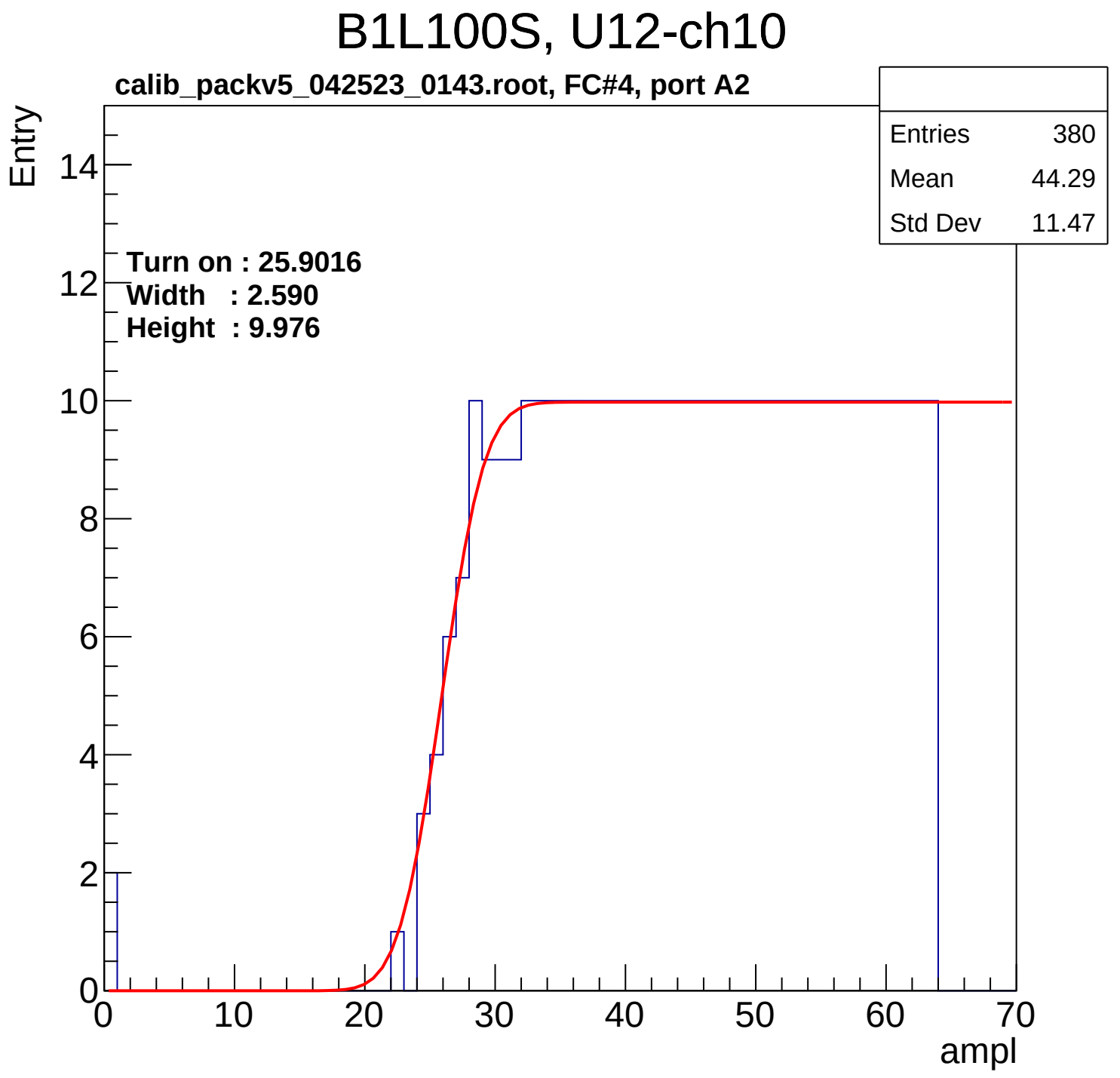

B1L100S, U12-ch5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 364
Mean 45.12
Std Dev 10.91
Turn on : 28.1323
Width : 3.163
Height : 10.053
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

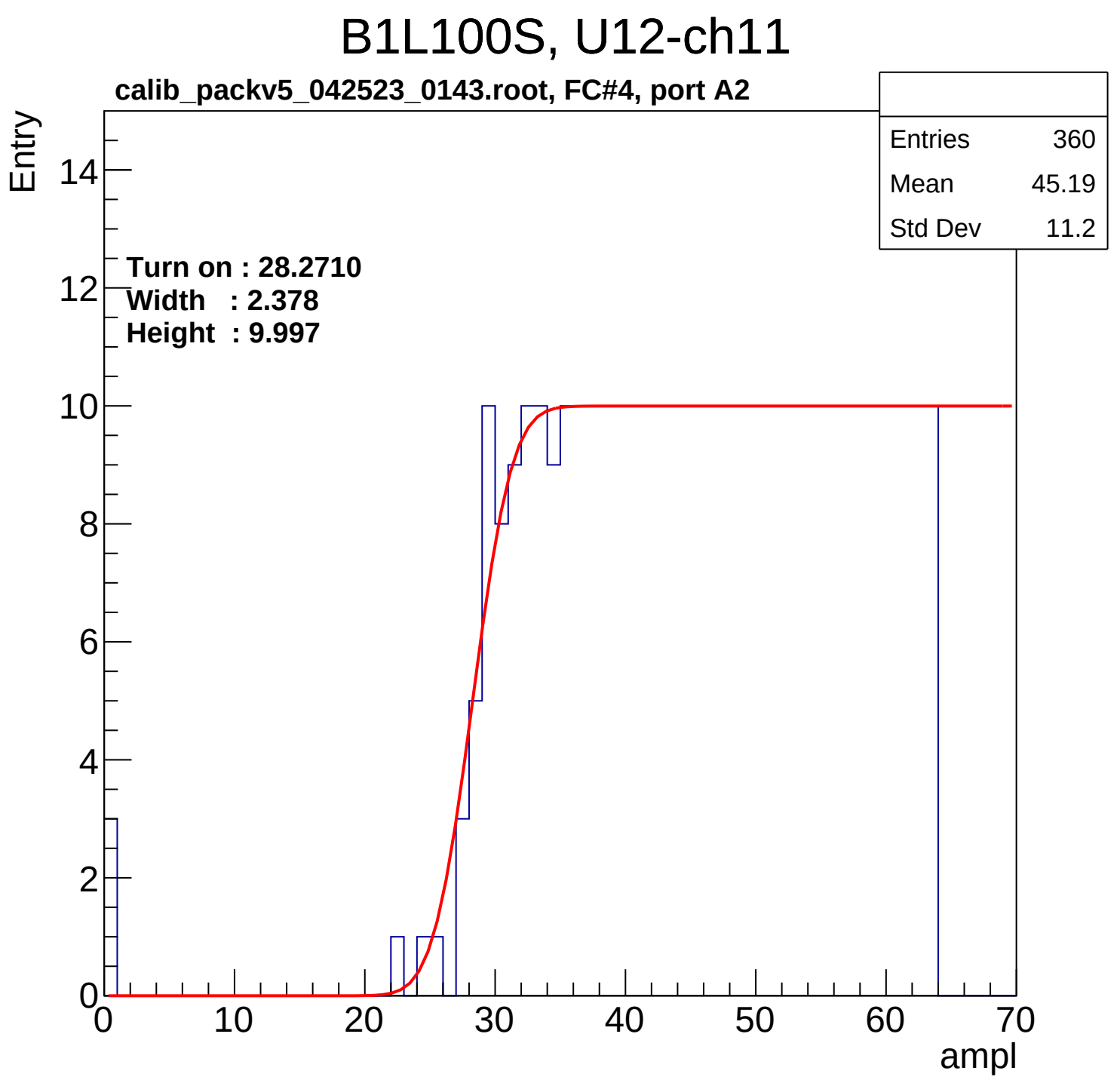

B1L100S, U12-ch6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 355
Mean 45.49
Std Dev 10.88
Turn on : 28.7403
Width : 2.803
Height : 9.973
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

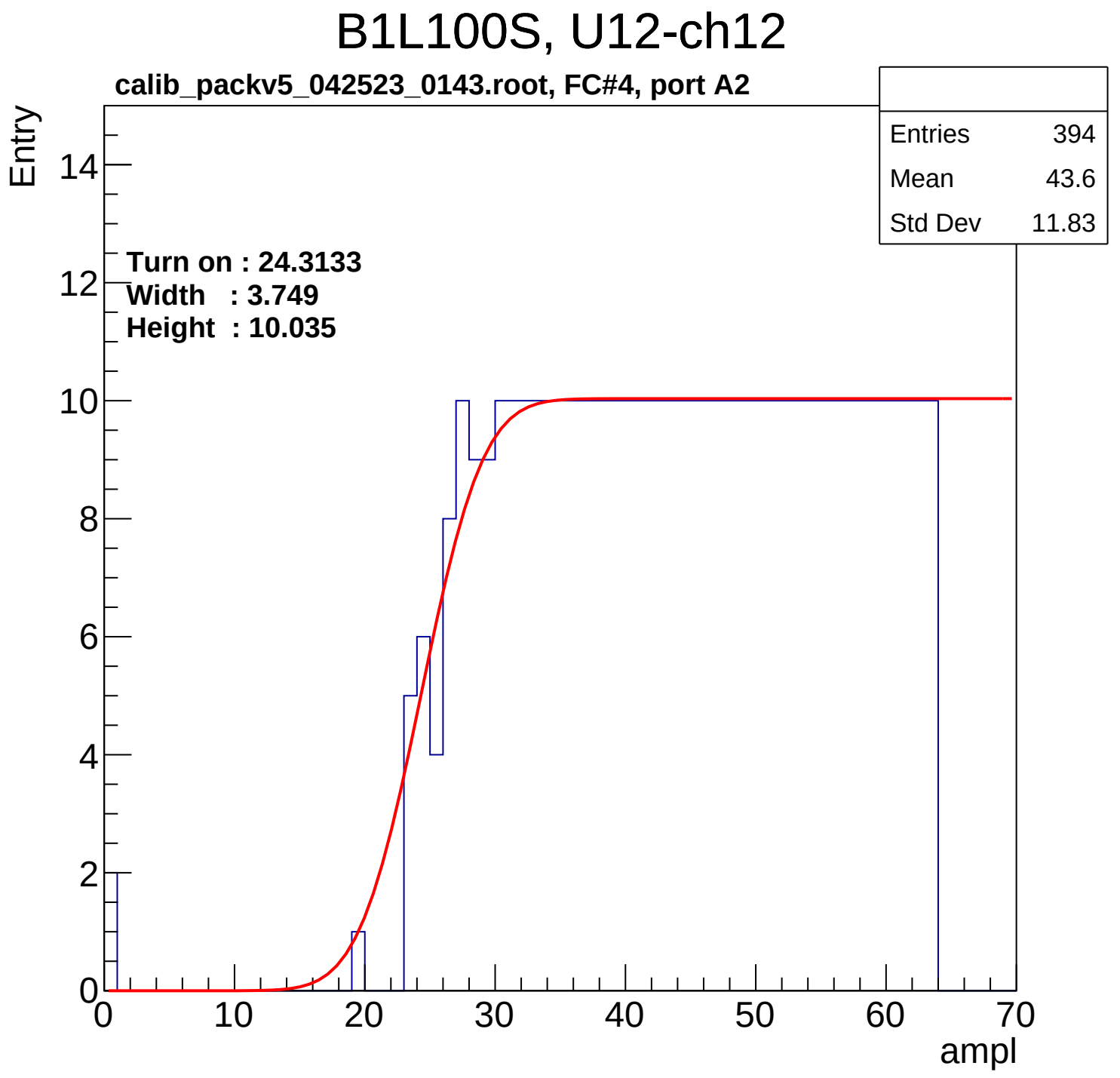

B1L100S, U12-ch7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 365
Mean 44.97
Std Dev 11.27
Turn on : 27.7253
Width : 2.366
Height : 9.998
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

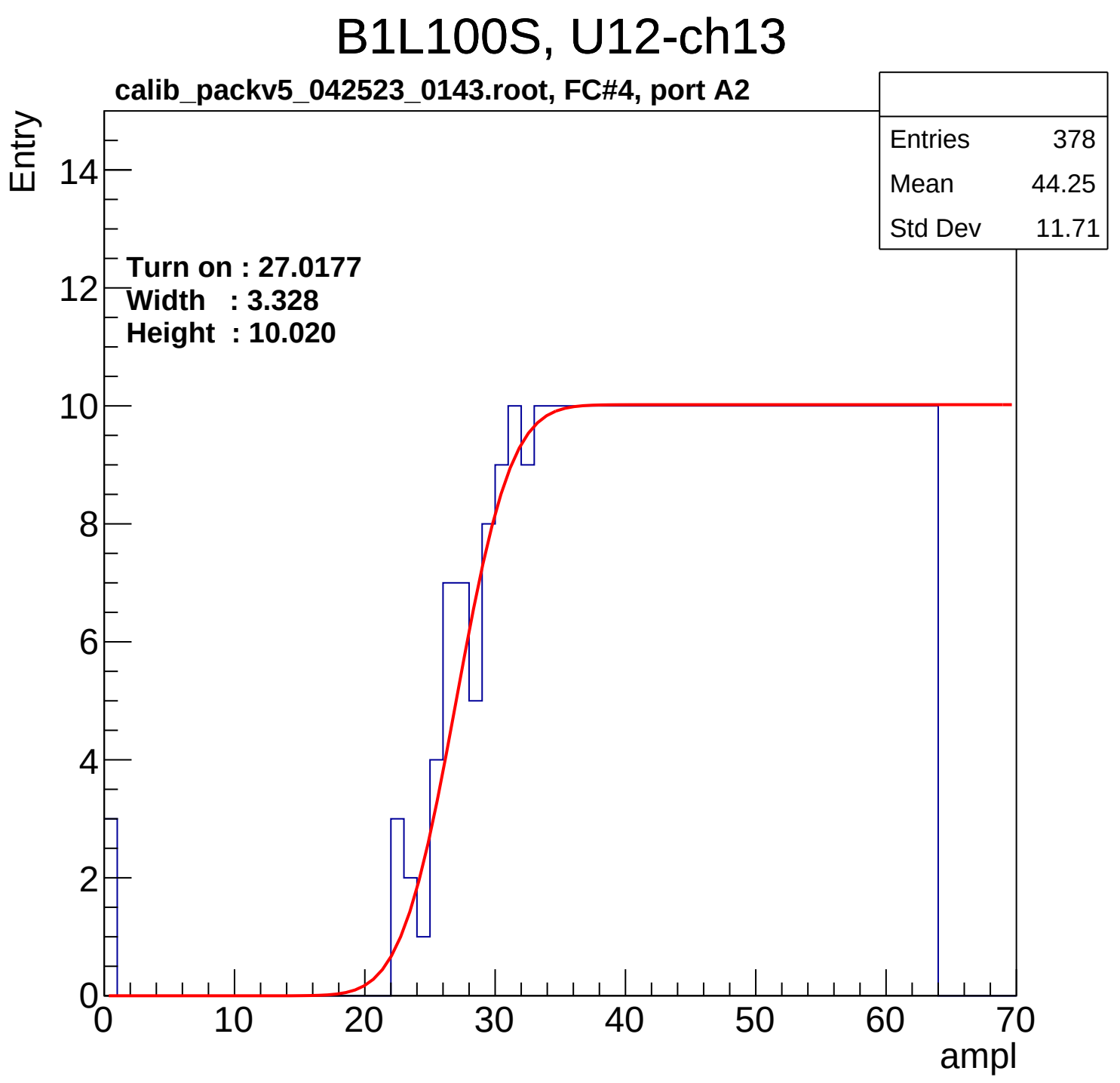

B1L100S, U12-ch8
calib_packv5_042523_0143.root, FC#4, port A2
Entries 381
Mean 44.22
Std Dev 11.53
Turn on : 25.6979
Width : 2.838
Height : 9.982
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

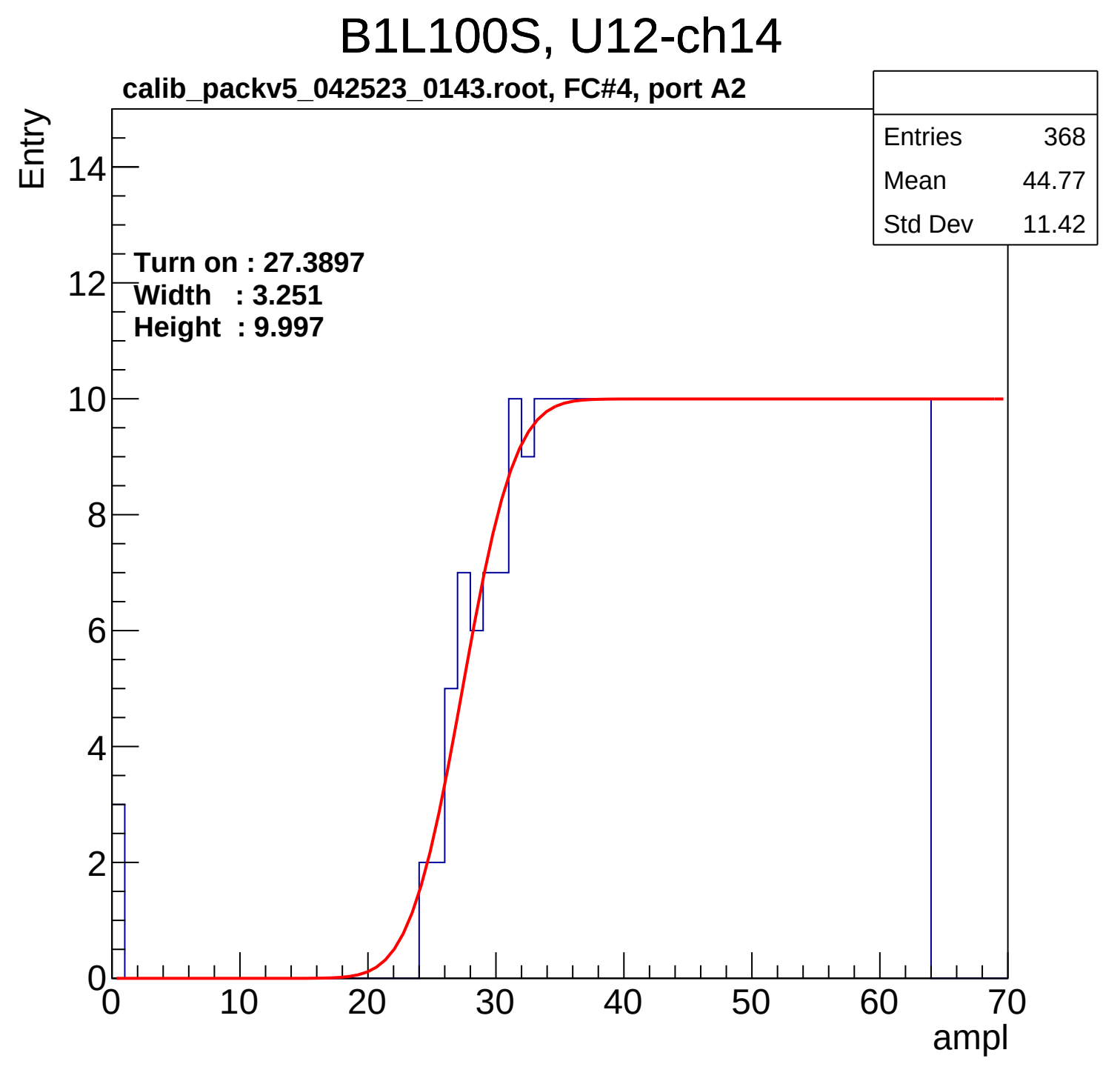

B1L100S, U12-ch9
calib_packv5_042523_0143.root, FC#4, port A2
Entries 368
Mean 44.88
Std Dev 11.16
Turn on : 27.8621
Width : 2.500
Height : 10.038
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

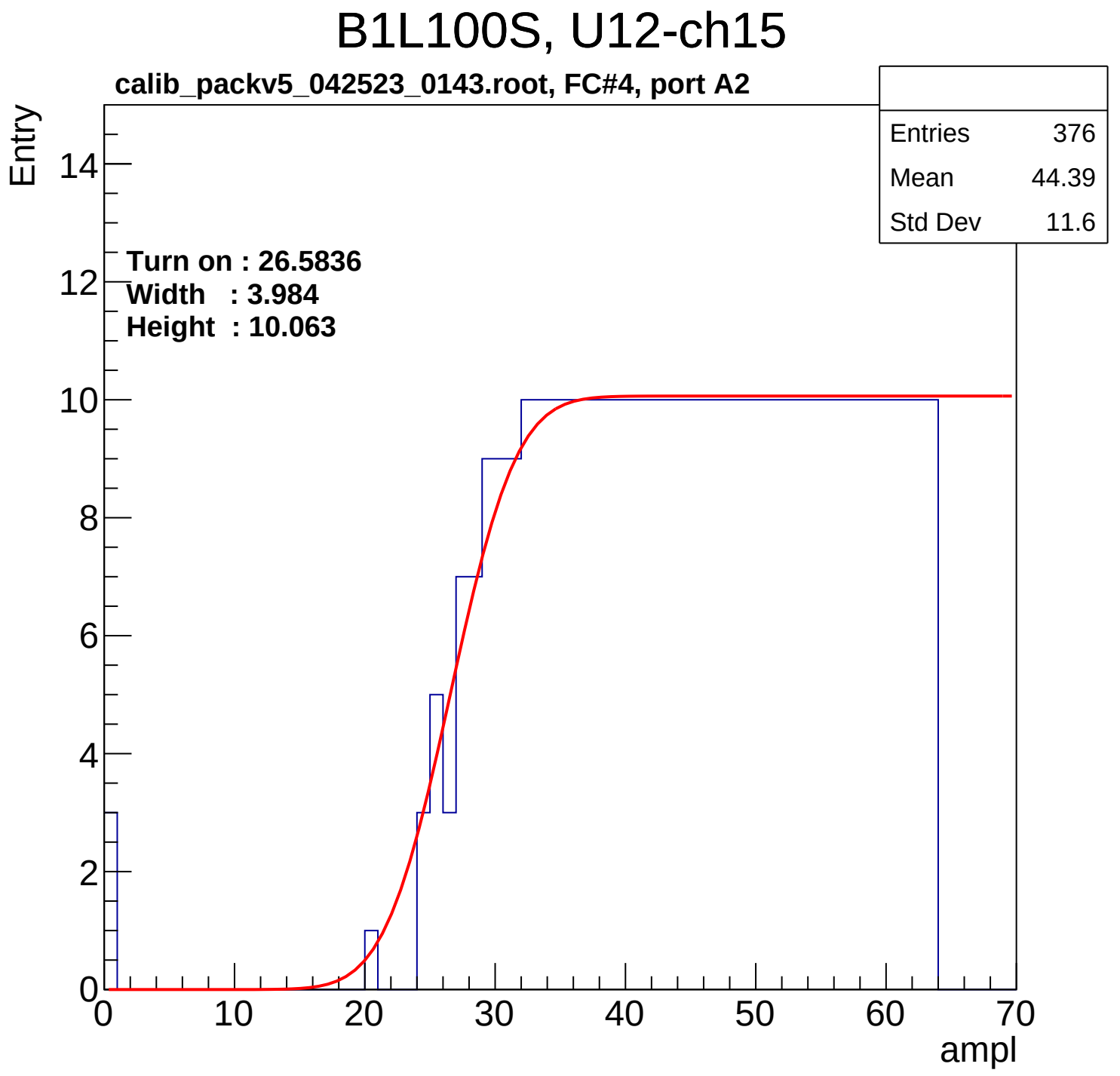

B1L100S, U12-ch10
calib_packv5_042523_0143.root, FC#4, port A2
Entries 380
Mean 44.29
Std Dev 11.47
Turn on : 25.9016
Width : 2.590
Height : 9.976
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

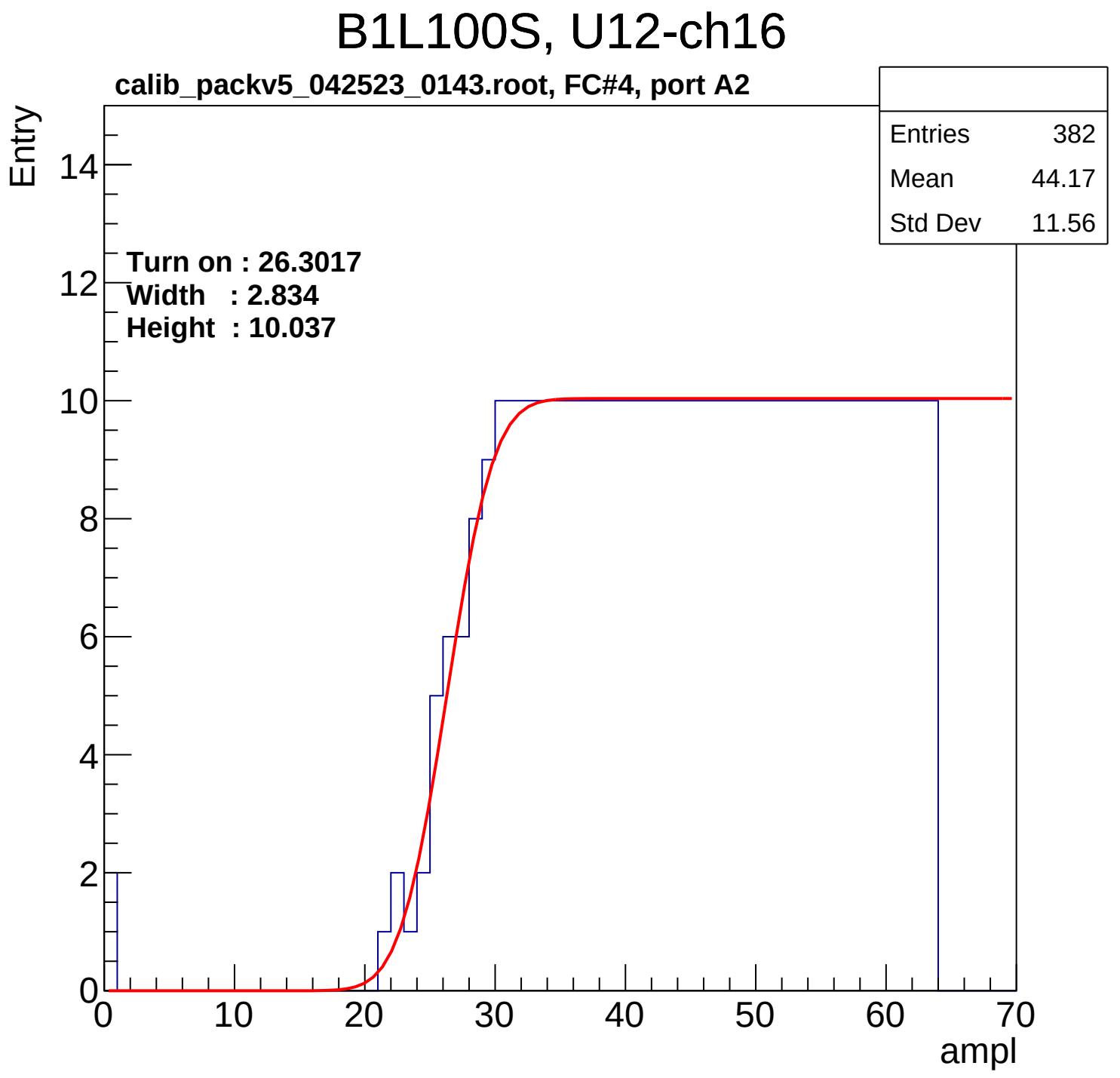

B1L100S, U12-ch11
calib_packv5_042523_0143.root, FC#4, port A2
Entries 360
Mean 45.19
Std Dev 11.2
Turn on : 28.2710
Width : 2.378
Height : 9.997
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

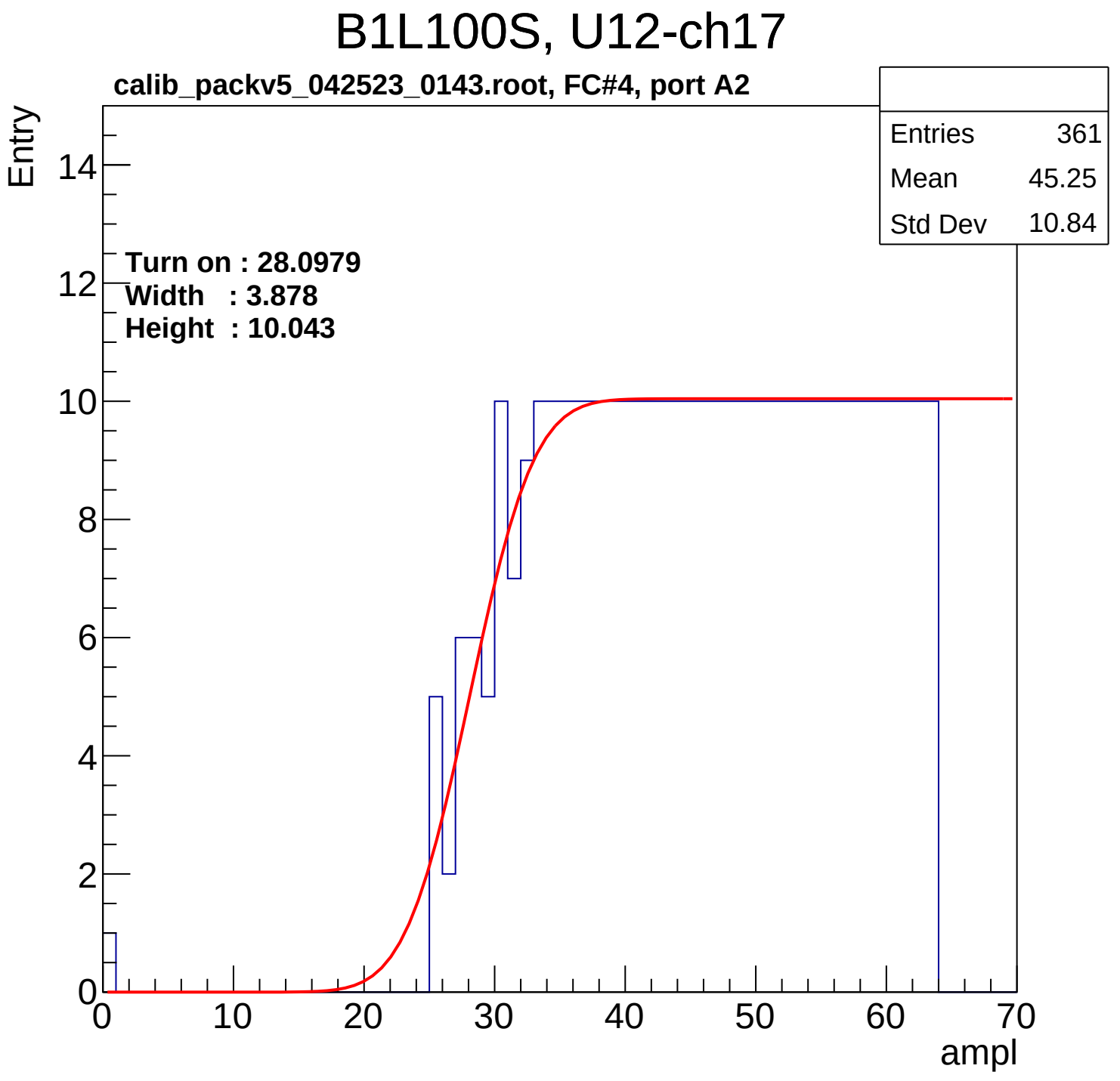

B1L100S, U12-ch12
calib_packv5_042523_0143.root, FC#4, port A2
Entries 394
Mean 43.6
Std Dev 11.83
Turn on : 24.3133
Width : 3.749
Height : 10.035
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

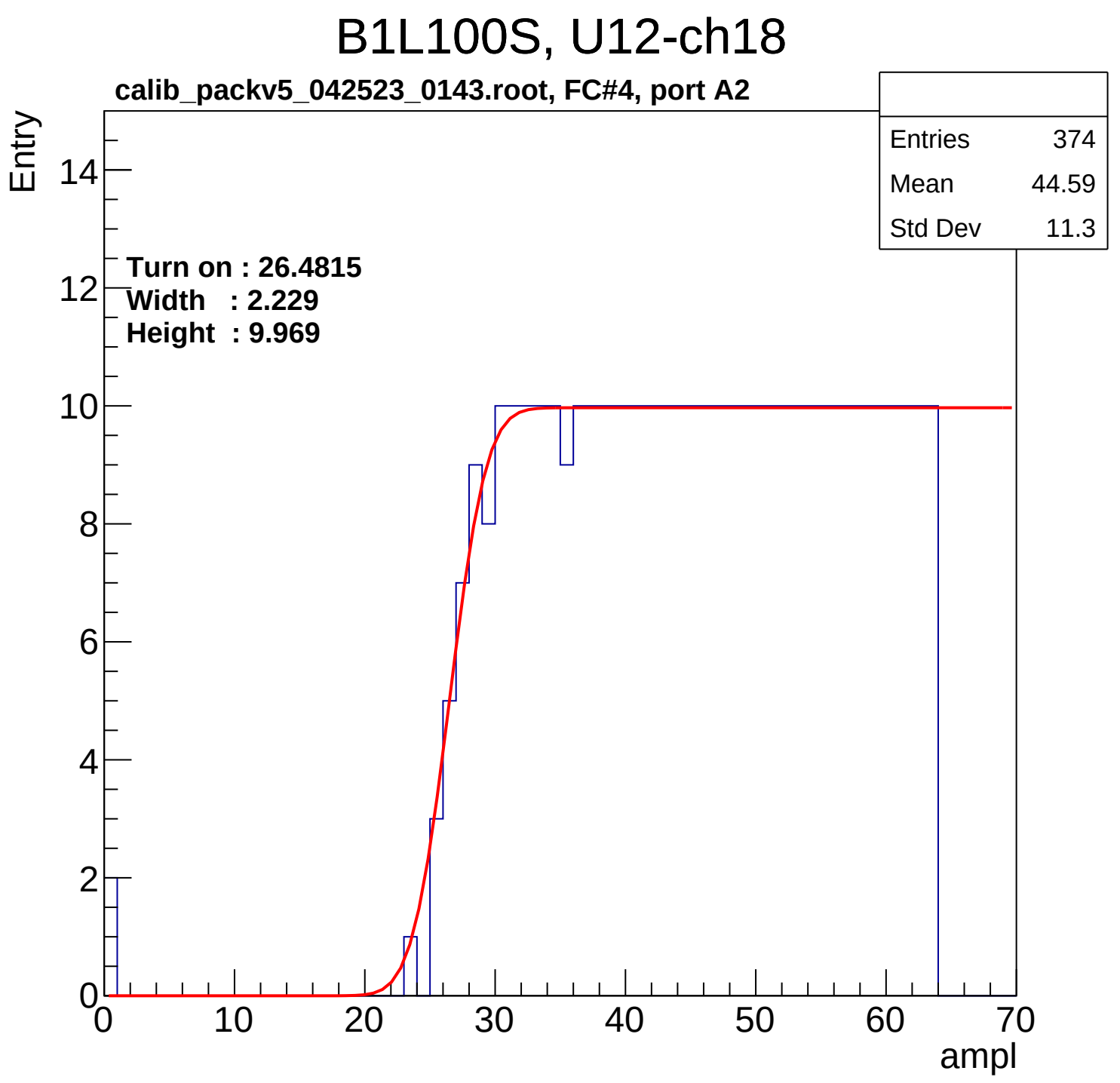

B1L100S, U12-ch13
calib_packv5_042523_0143.root, FC#4, port A2
Entries 378
Mean 44.25
Std Dev 11.71
Turn on : 27.0177
Width : 3.328
Height : 10.020
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

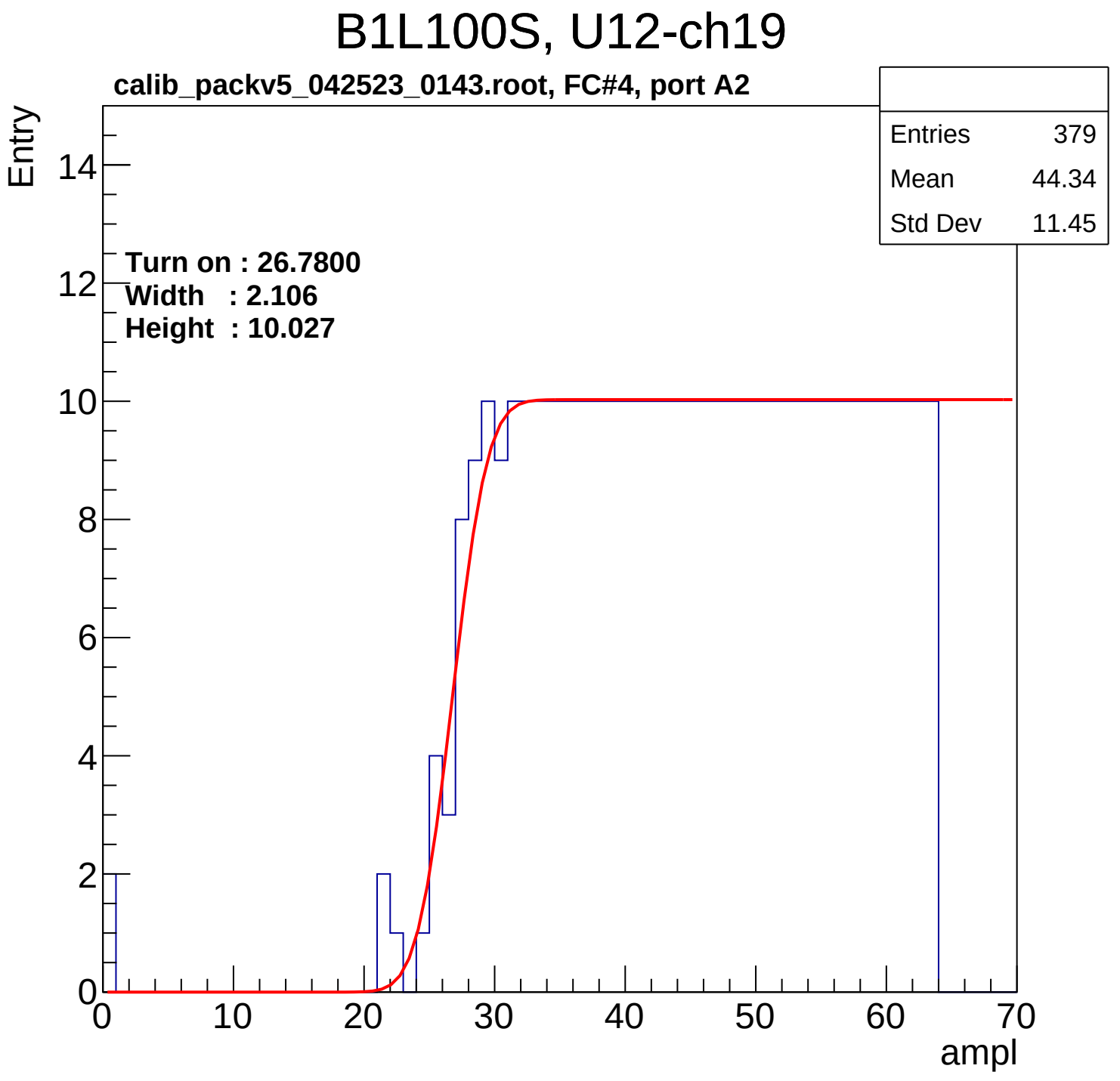

B1L100S, U12-ch14
calib_packv5_042523_0143.root, FC#4, port A2
Entries 368
Mean 44.77
Std Dev 11.42
Turn on : 27.3897
Width : 3.251
Height : 9.997
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

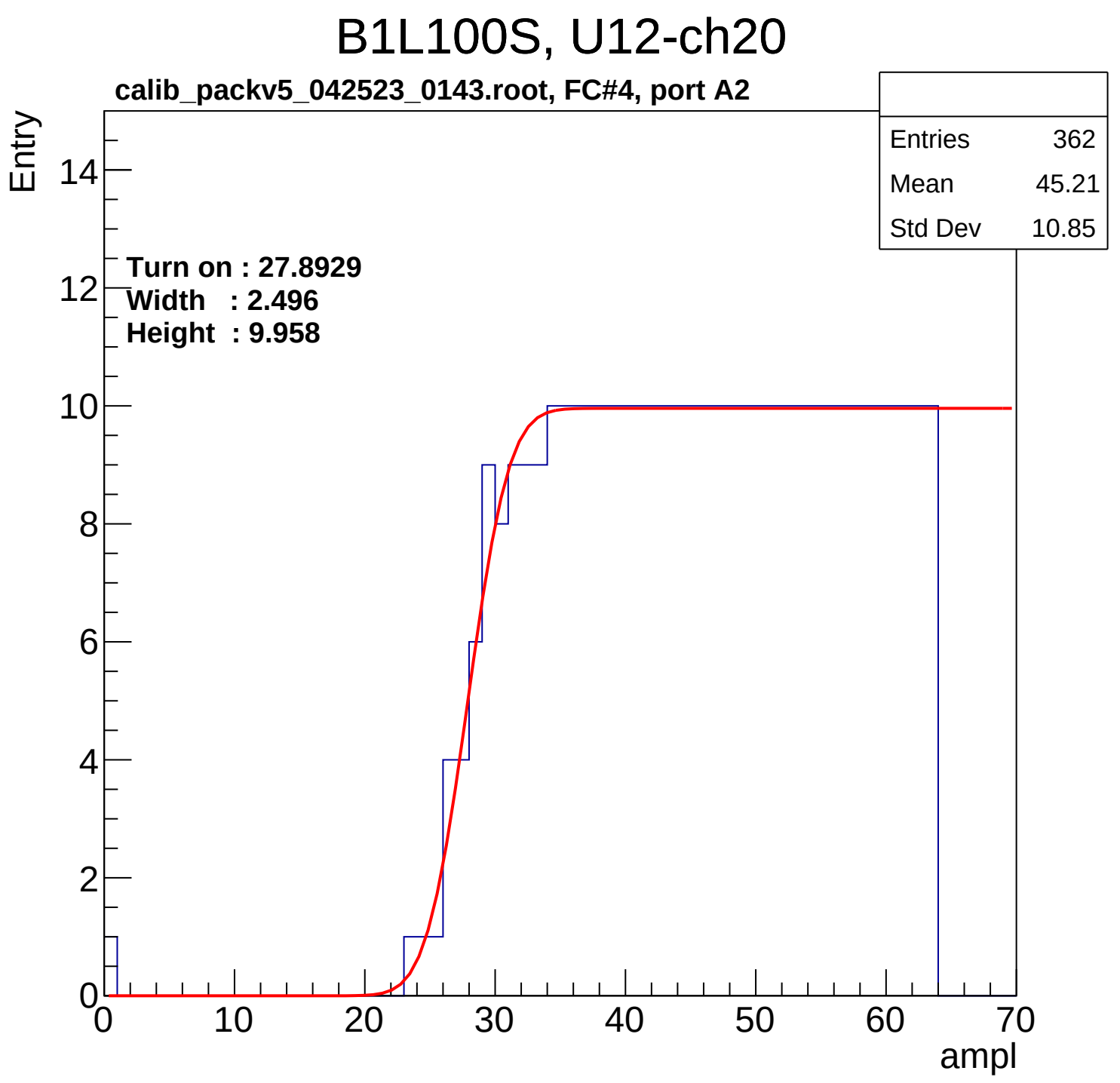

B1L100S, U12-ch15
calib_packv5_042523_0143.root, FC#4, port A2
Entries 376
Mean 44.39
Std Dev 11.6
Turn on : 26.5836
Width : 3.984
Height : 10.063
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

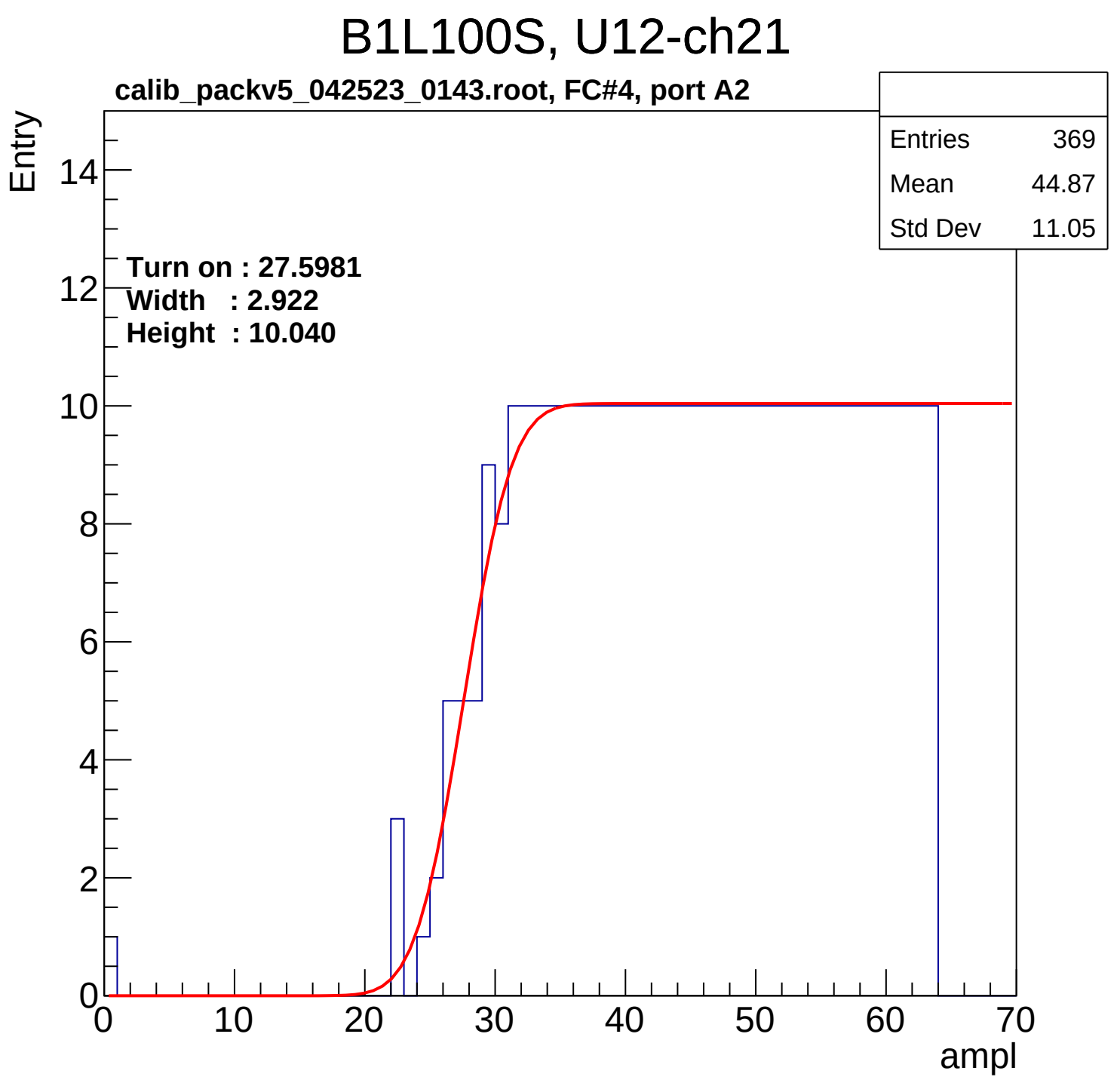

B1L100S, U12-ch16
calib_packv5_042523_0143.root, FC#4, port A2
Entries 382
Mean 44.17
Std Dev 11.56
Turn on : 26.3017
Width : 2.834
Height : 10.037
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

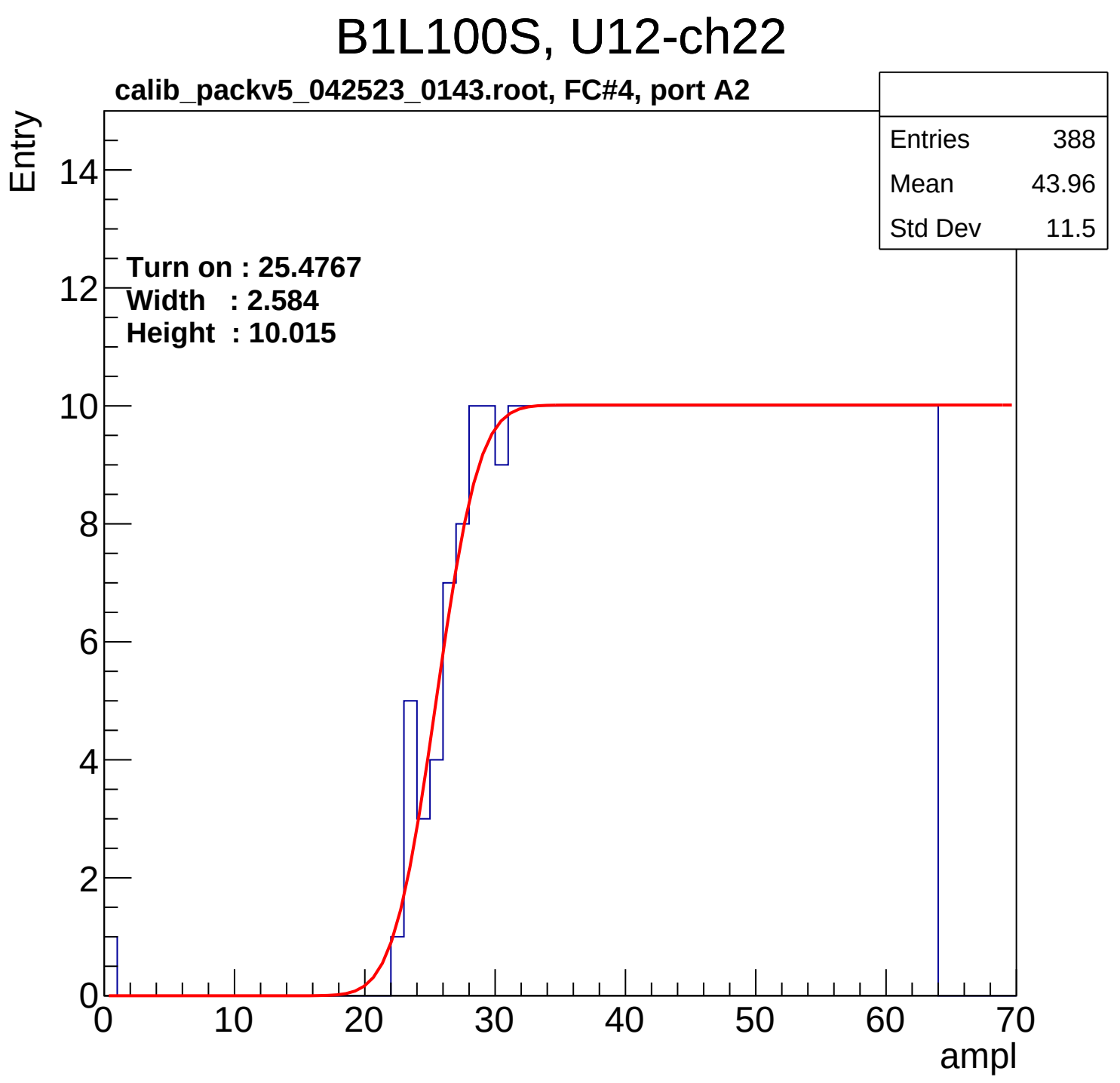

B1L100S, U12-ch17
calib_packv5_042523_0143.root, FC#4, port A2
Entries 361
Mean 45.25
Std Dev 10.84
Turn on : 28.0979
Width : 3.878
Height : 10.043
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

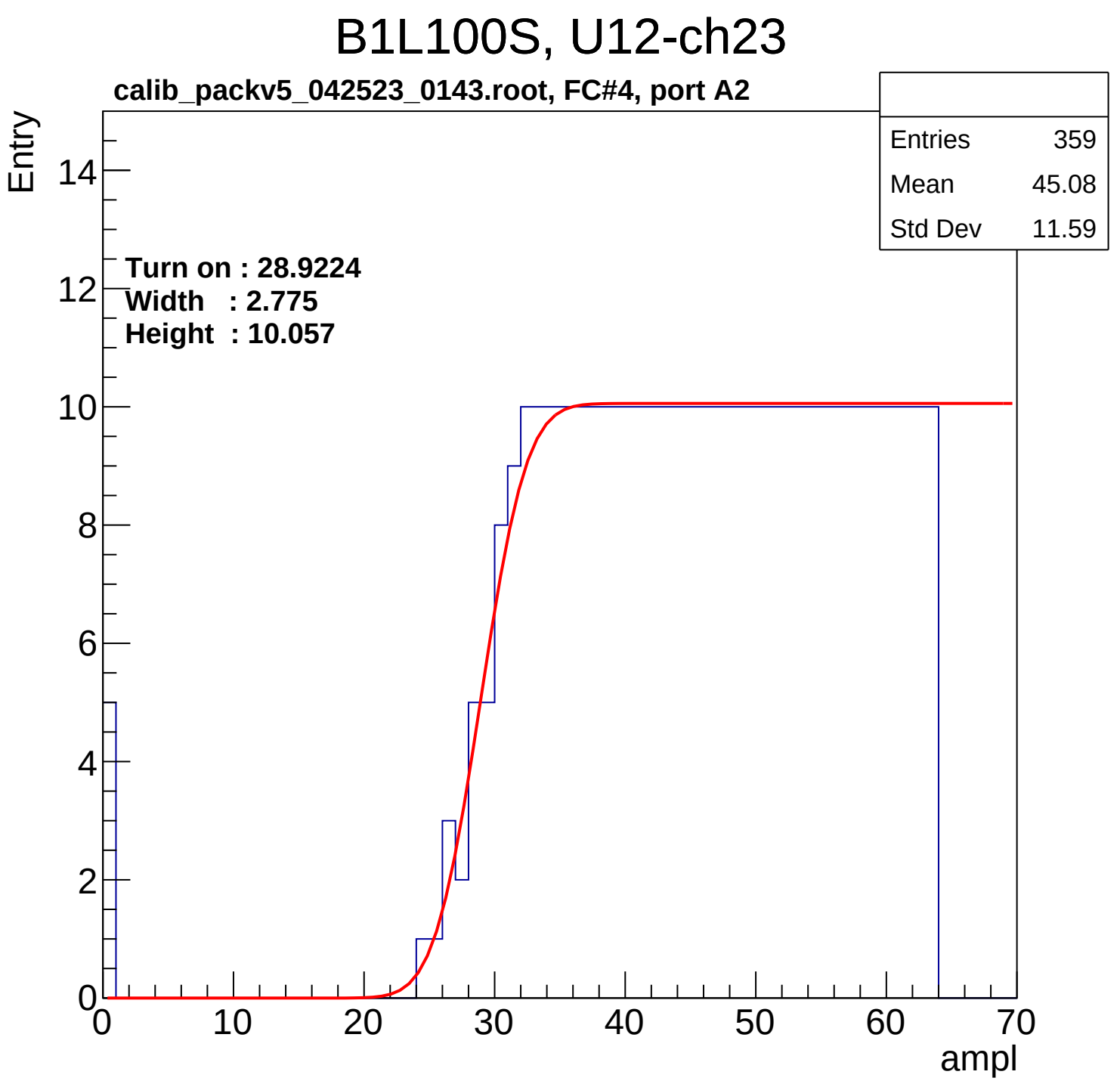

B1L100S, U12-ch18
calib_packv5_042523_0143.root, FC#4, port A2
Entries 374
Mean 44.59
Std Dev 11.3
Turn on : 26.4815
Width : 2.229
Height : 9.969
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

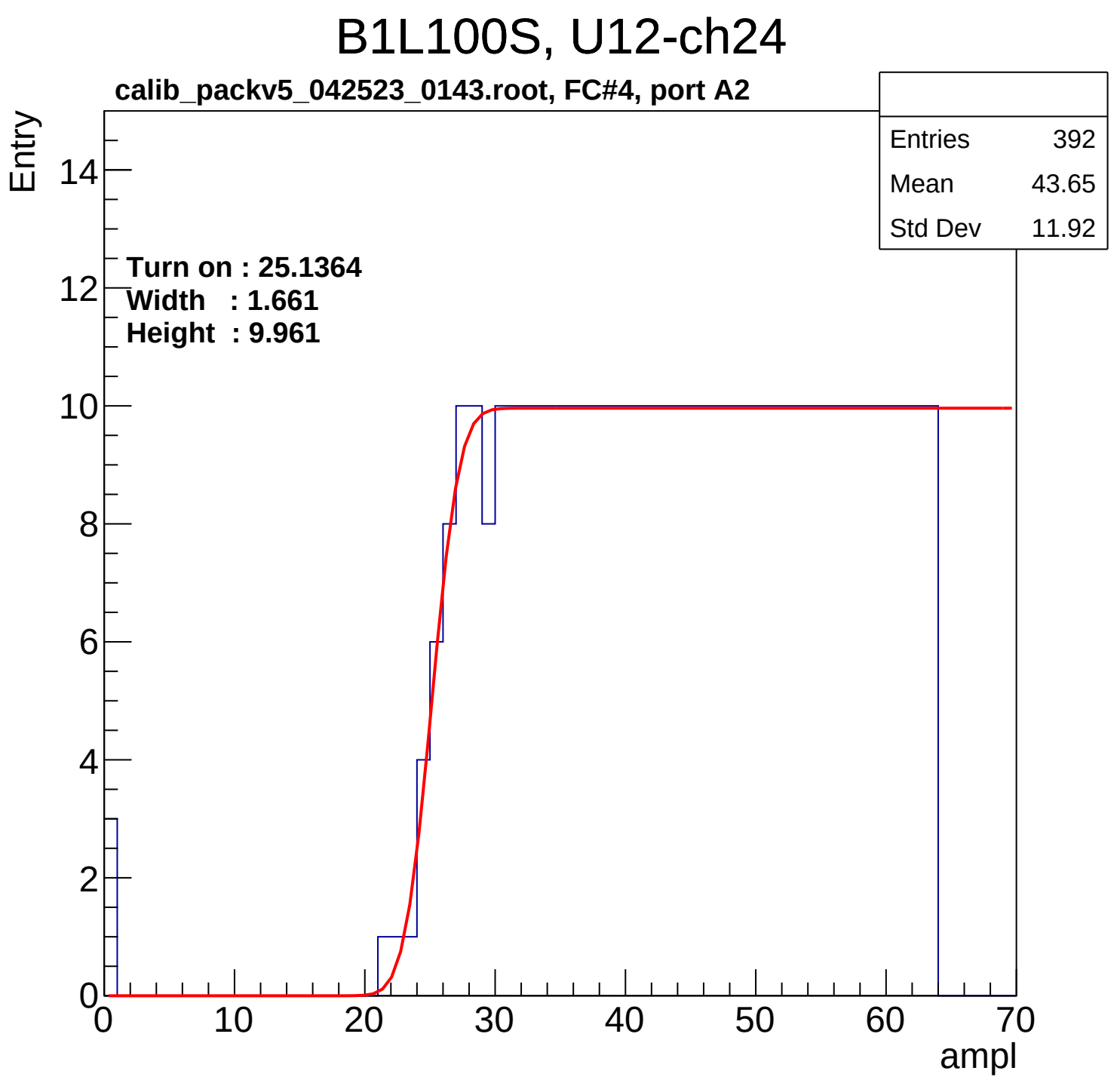

B1L100S, U12-ch19
calib_packv5_042523_0143.root, FC#4, port A2
Entries 379
Mean 44.34
Std Dev 11.45
Turn on : 26.7800
Width : 2.106
Height : 10.027
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

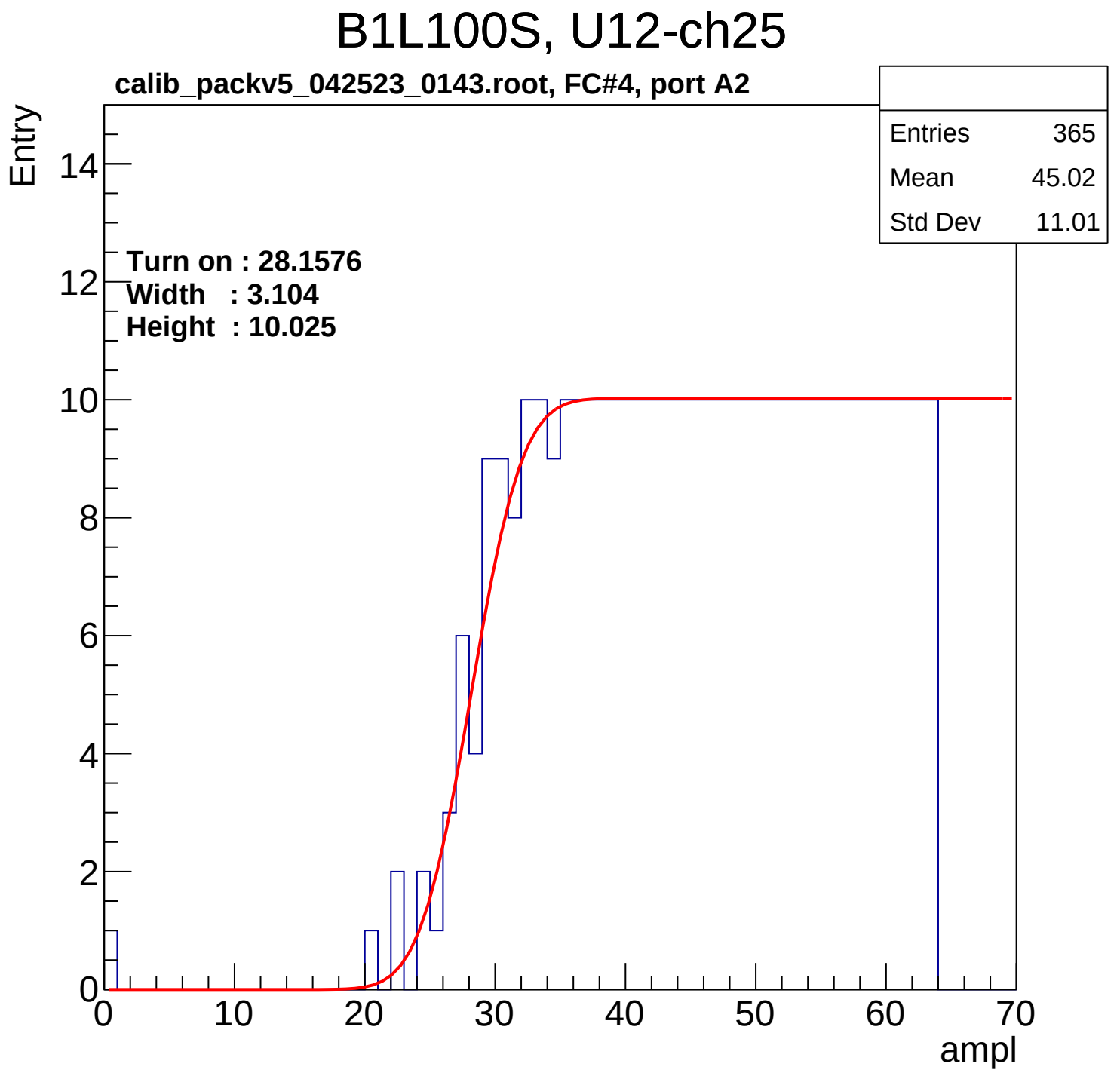

B1L100S, U12-ch20
calib_packv5_042523_0143.root, FC#4, port A2
Entries 362
Mean 45.21
Std Dev 10.85
Turn on : 27.8929
Width : 2.496
Height : 9.958
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

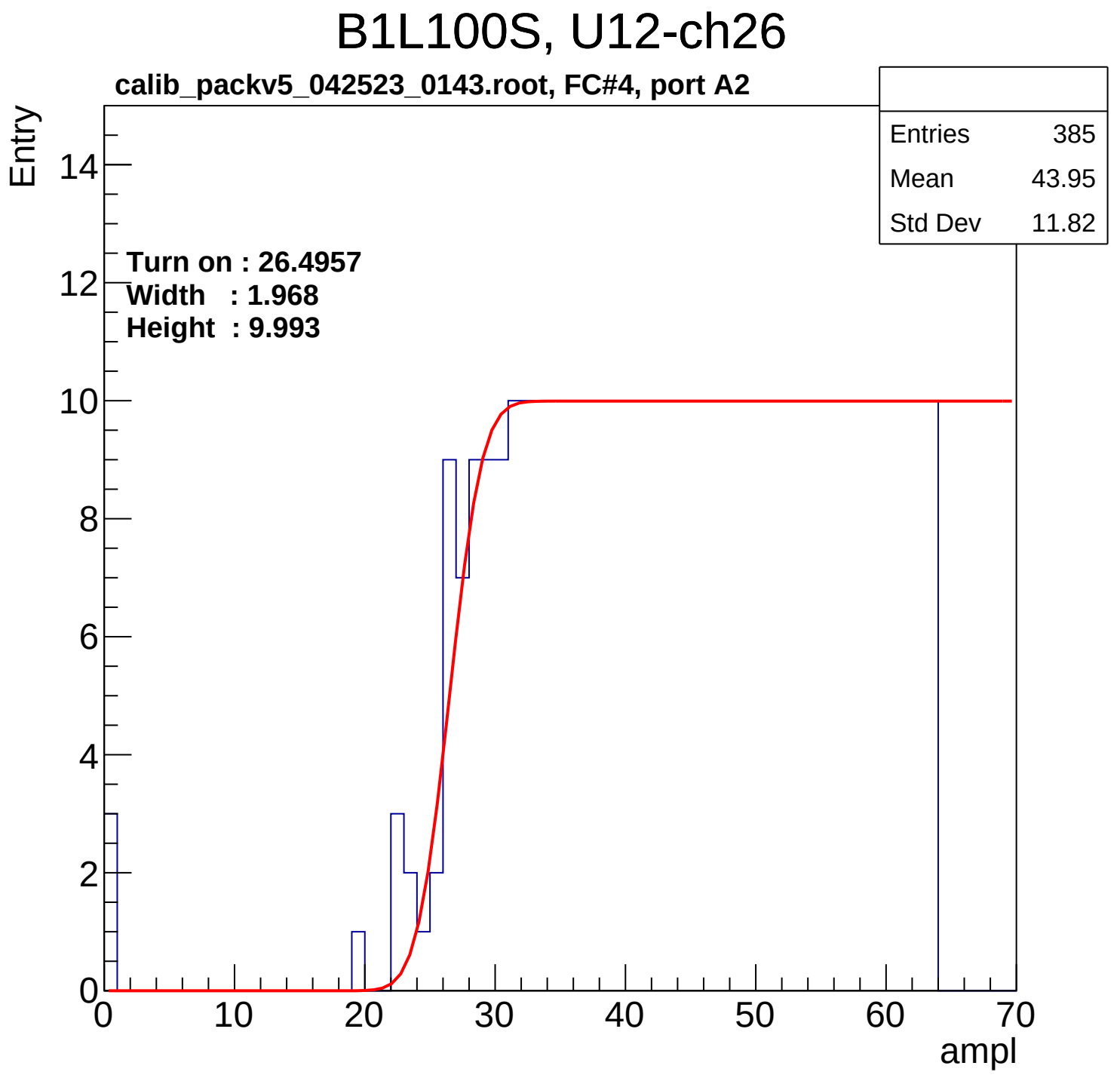

B1L100S, U12-ch21
calib_packv5_042523_0143.root, FC#4, port A2
Entries 369
Mean 44.87
Std Dev 11.05
Turn on : 27.5981
Width : 2.922
Height : 10.040
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

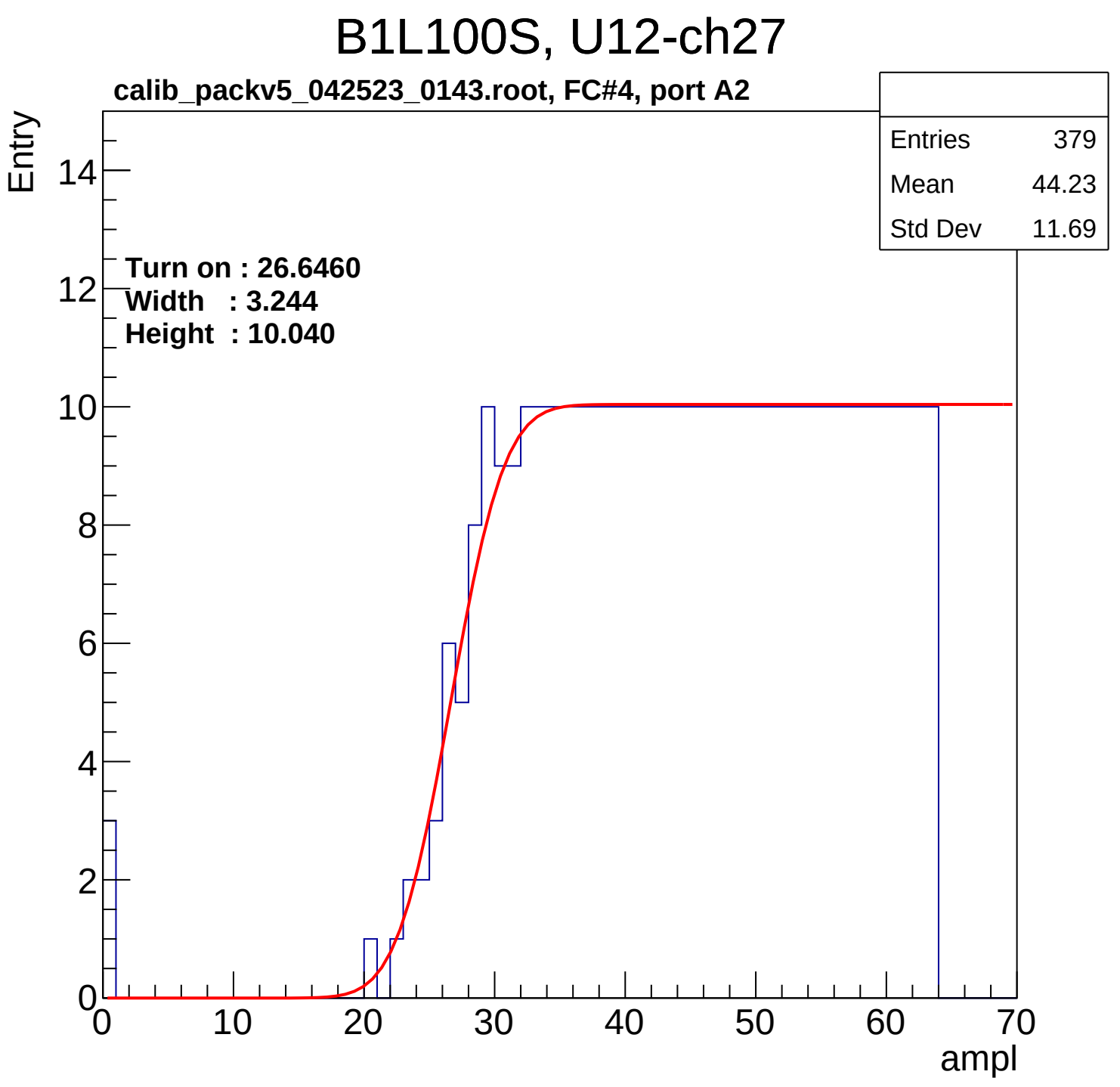

B1L100S, U12-ch22
calib_packv5_042523_0143.root, FC#4, port A2
Entries 388
Mean 43.96
Std Dev 11.5
Turn on : 25.4767
Width : 2.584
Height : 10.015
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

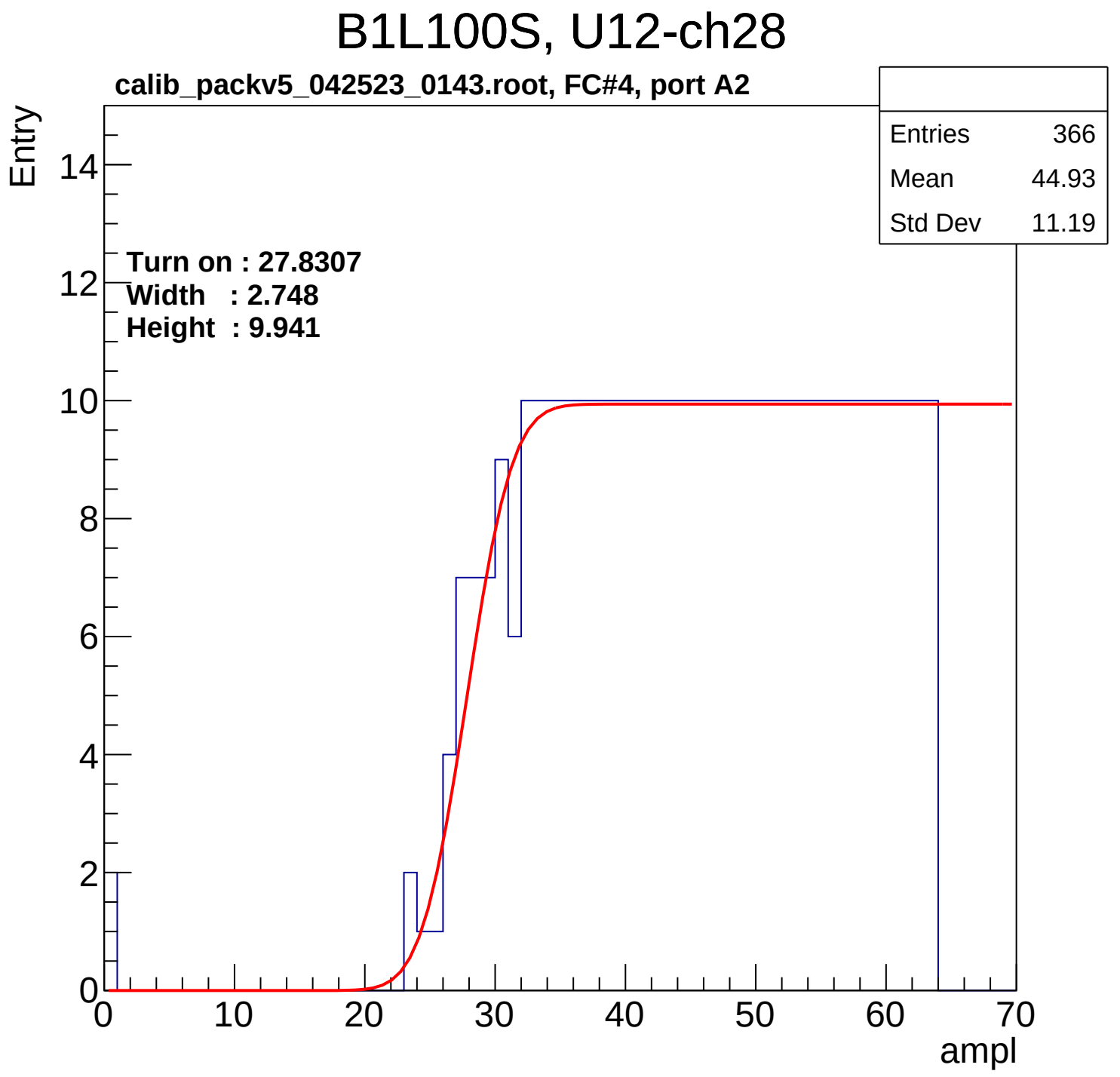

B1L100S, U12-ch23
calib_packv5_042523_0143.root, FC#4, port A2
Entries 359
Mean 45.08
Std Dev 11.59
Turn on : 28.9224
Width : 2.775
Height : 10.057
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

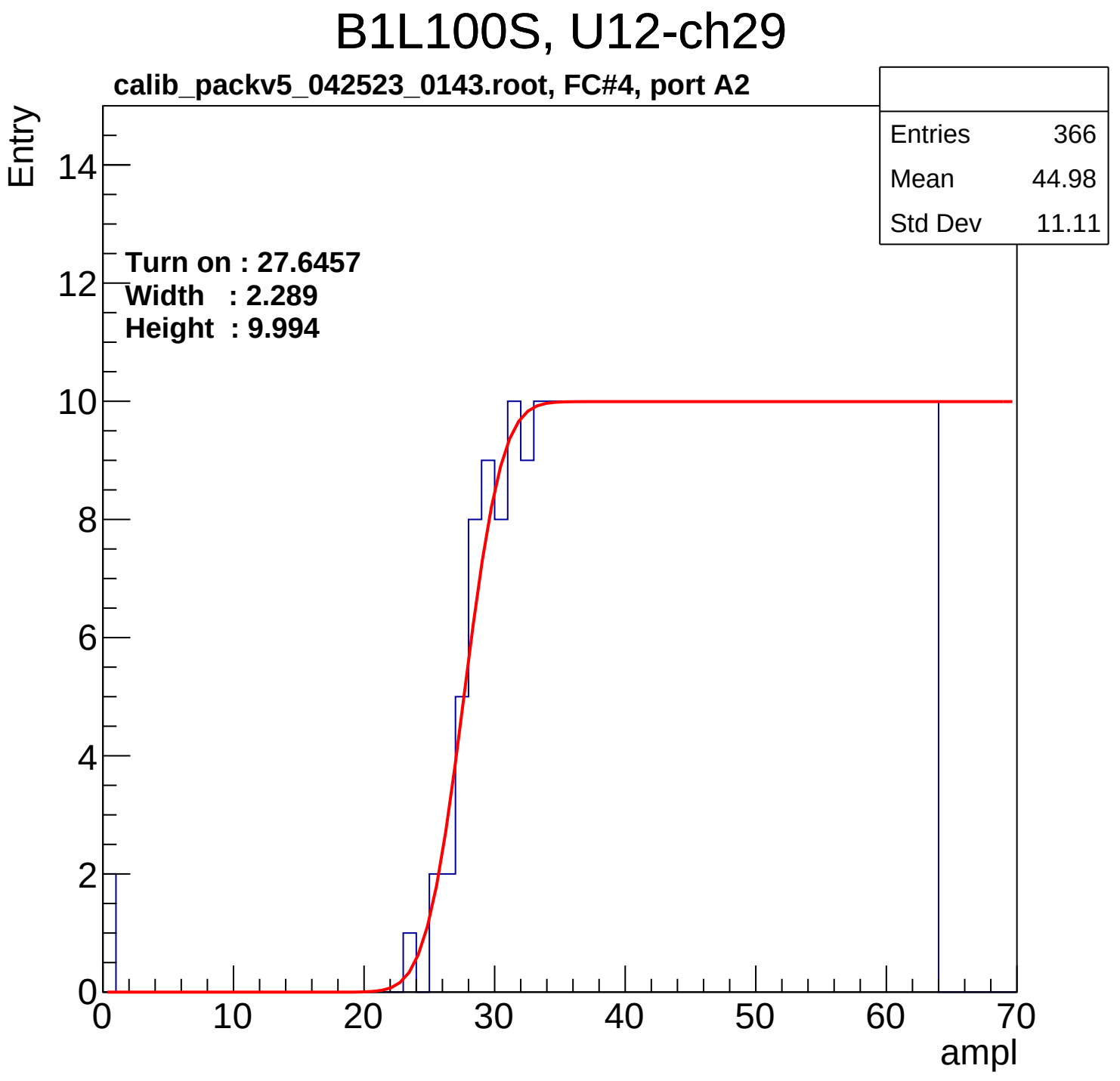

B1L100S, U12-ch24
calib_packv5_042523_0143.root, FC#4, port A2
Entries 392
Mean 43.65
Std Dev 11.92
Turn on : 25.1364
Width : 1.661
Height : 9.961
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

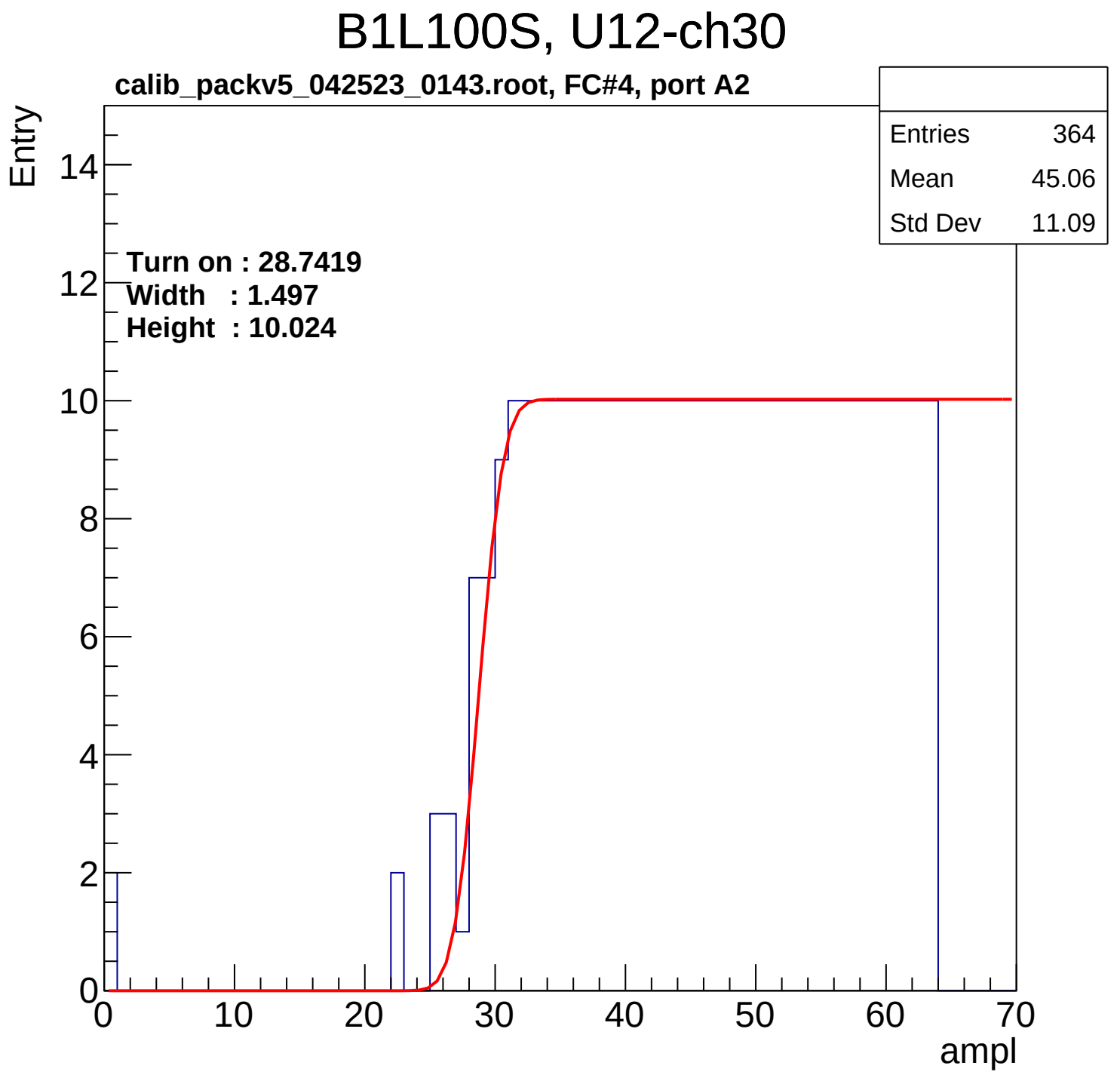

B1L100S, U12-ch25
calib_packv5_042523_0143.root, FC#4, port A2
Entries 365
Mean 45.02
Std Dev 11.01
Turn on : 28.1576
Width : 3.104
Height : 10.025
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

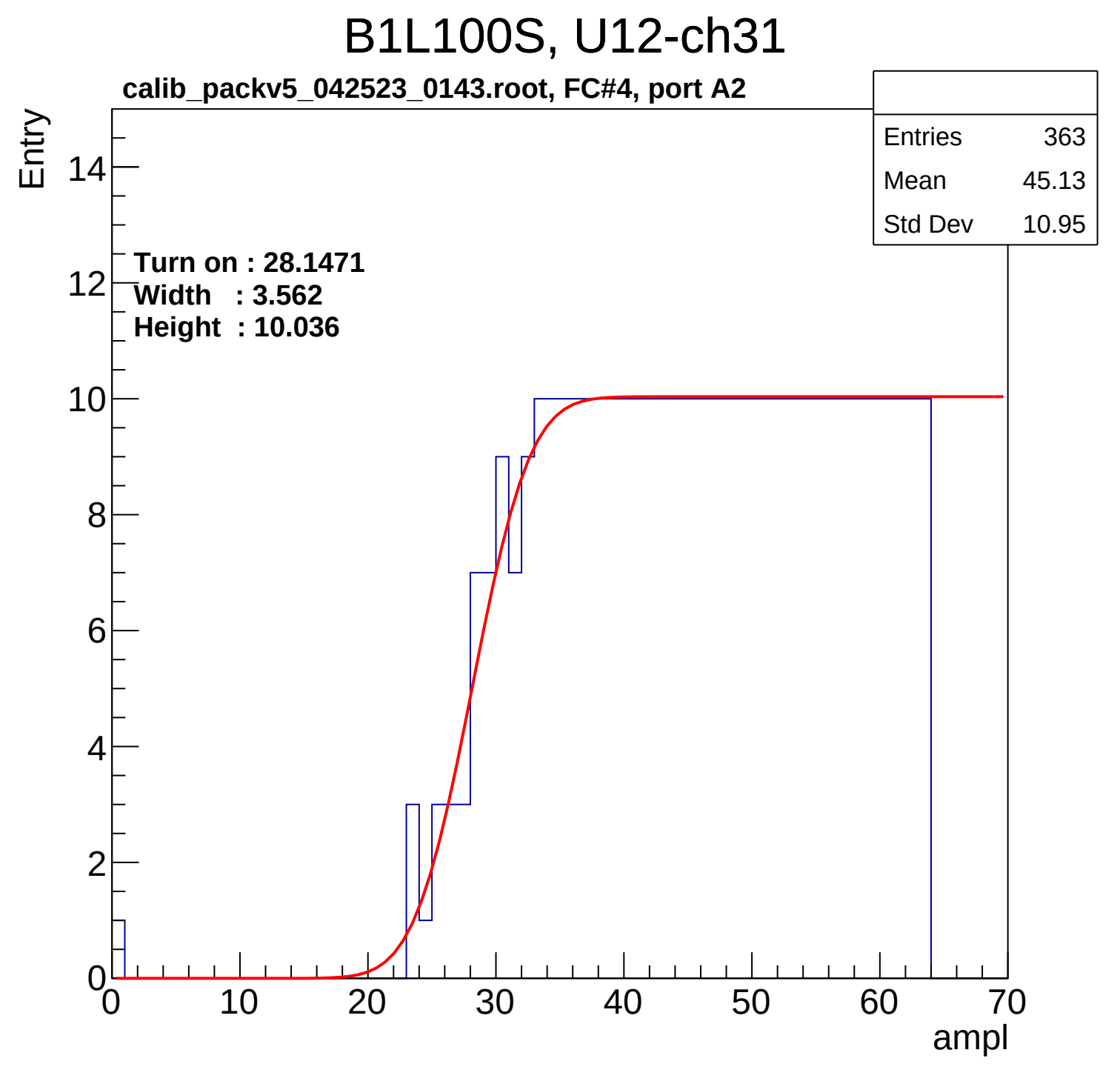

B1L100S, U12-ch26
calib_packv5_042523_0143.root, FC#4, port A2
Entries 385
Mean 43.95
Std Dev 11.82
Turn on : 26.4957
Width : 1.968
Height : 9.993
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

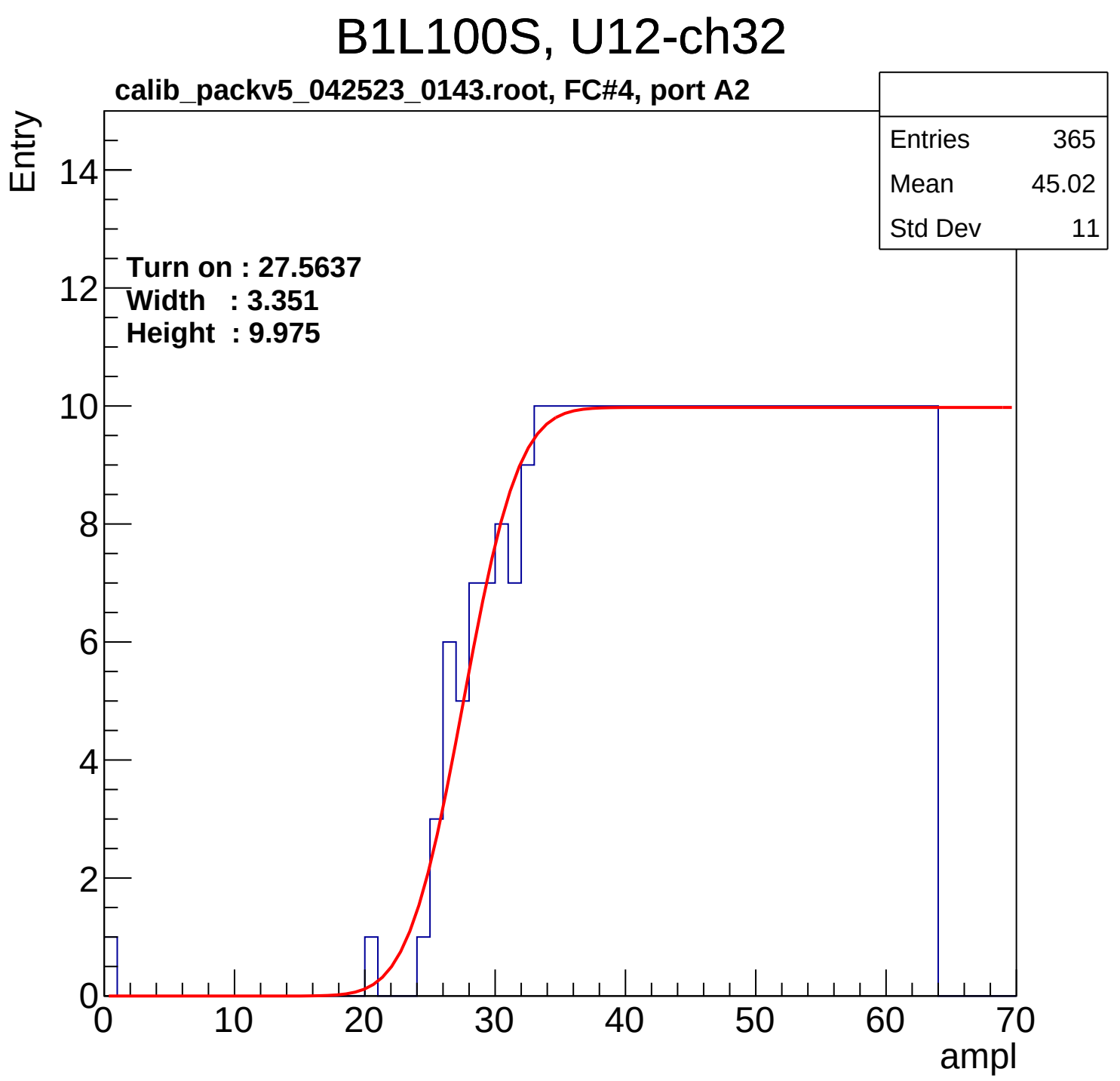

B1L100S, U12-ch27
calib_packv5_042523_0143.root, FC#4, port A2
Entries 379
Mean 44.23
Std Dev 11.69
Turn on : 26.6460
Width : 3.244
Height : 10.040
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

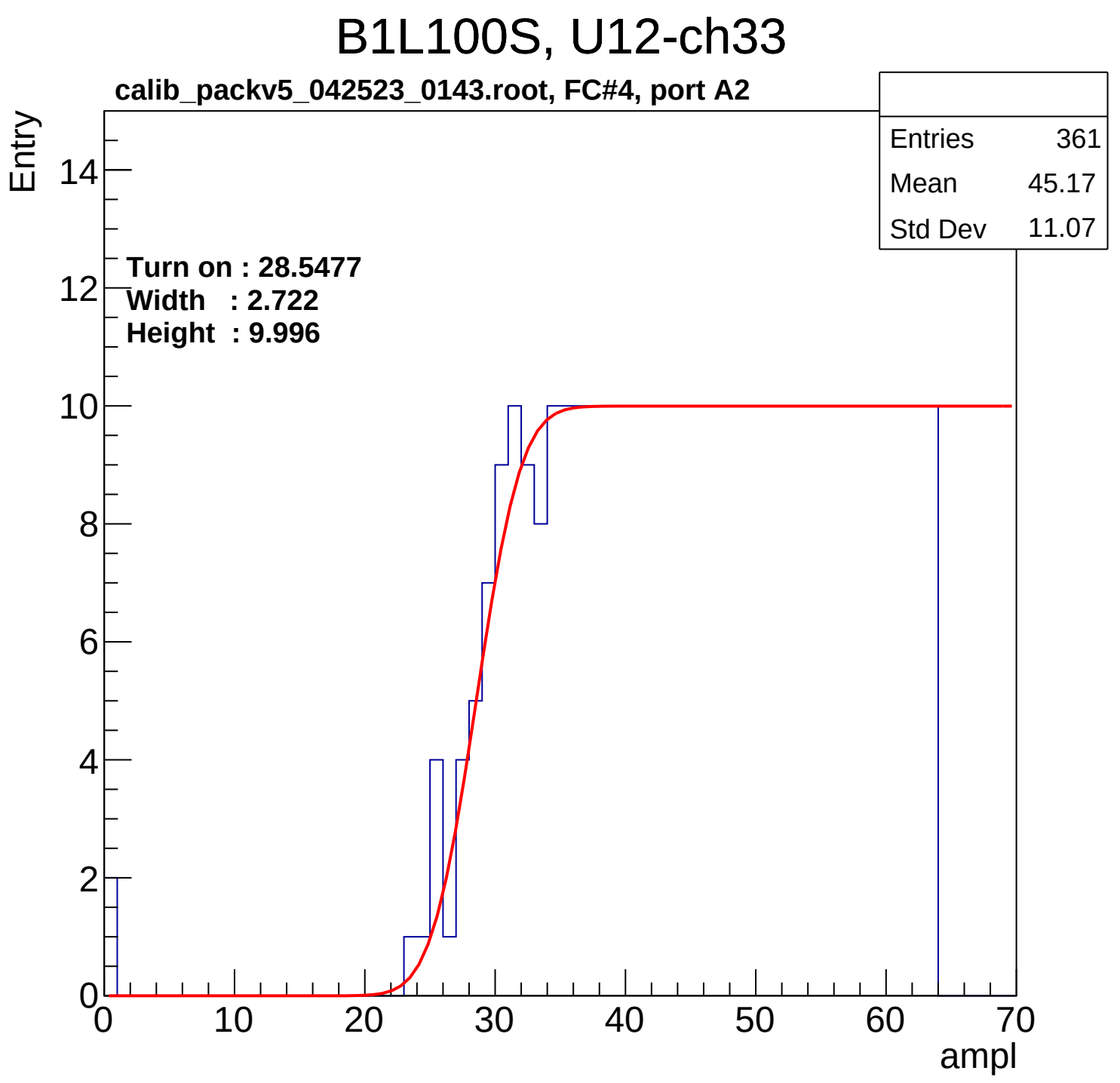

B1L100S, U12-ch28
calib_packv5_042523_0143.root, FC#4, port A2
Entries 366
Mean 44.93
Std Dev 11.19
Turn on : 27.8307
Width : 2.748
Height : 9.941
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

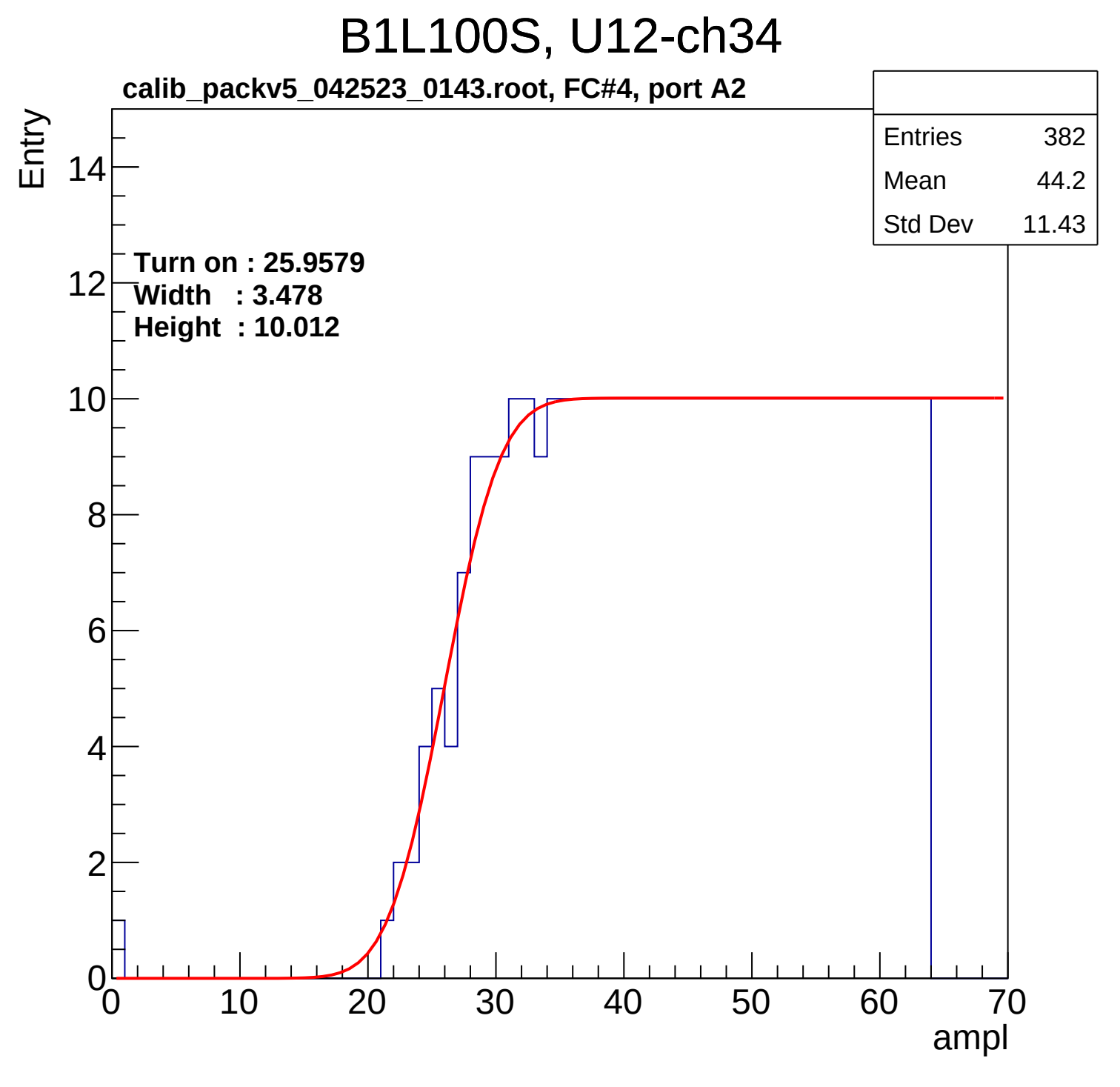

B1L100S, U12-ch29
calib_packv5_042523_0143.root, FC#4, port A2
Entries 366
Mean 44.98
Std Dev 11.11
Turn on : 27.6457
Width : 2.289
Height : 9.994
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

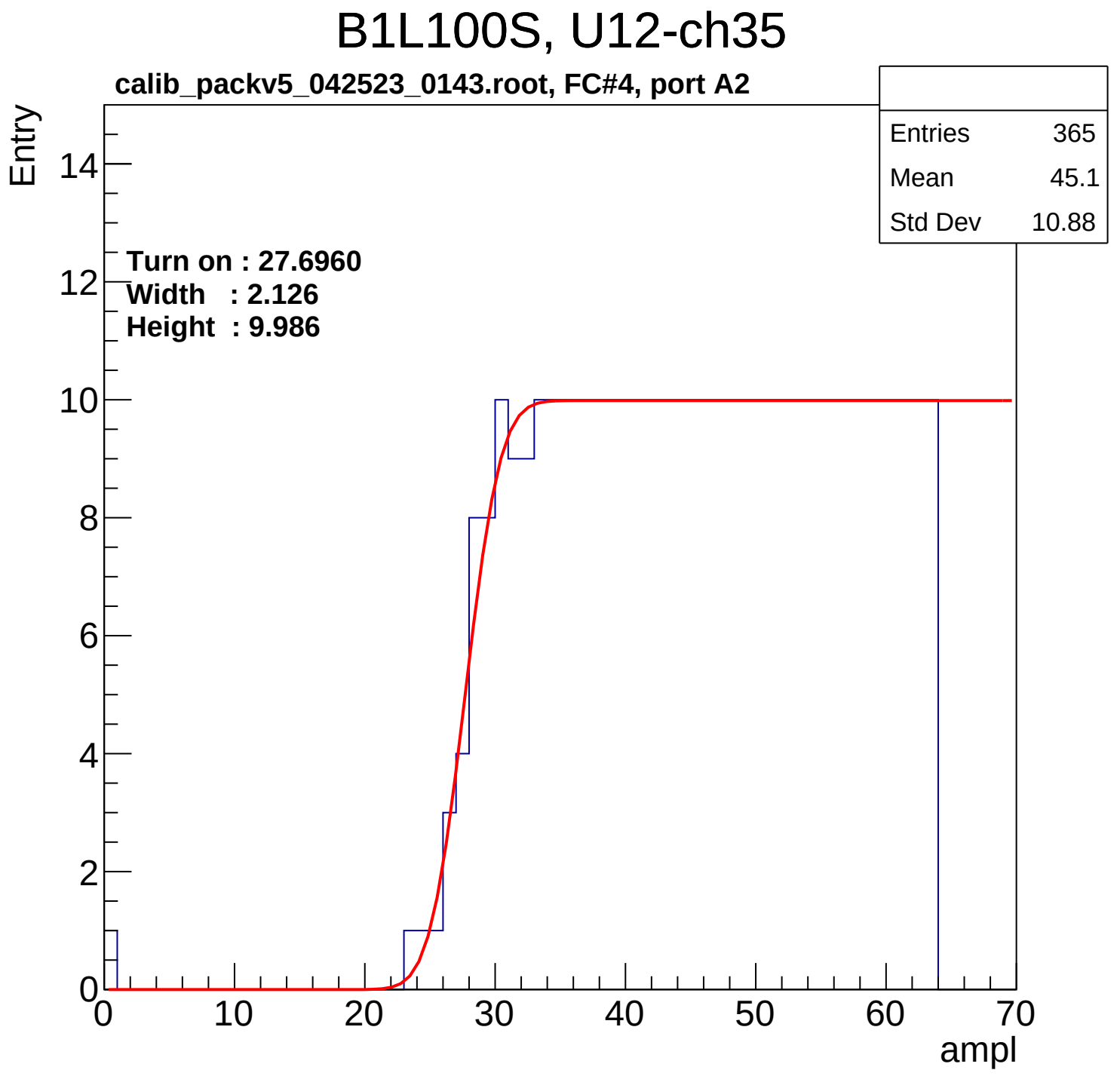

B1L100S, U12-ch30
calib_packv5_042523_0143.root, FC#4, port A2
Entries 364
Mean 45.06
Std Dev 11.09
Turn on : 28.7419
Width : 1.497
Height : 10.024
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

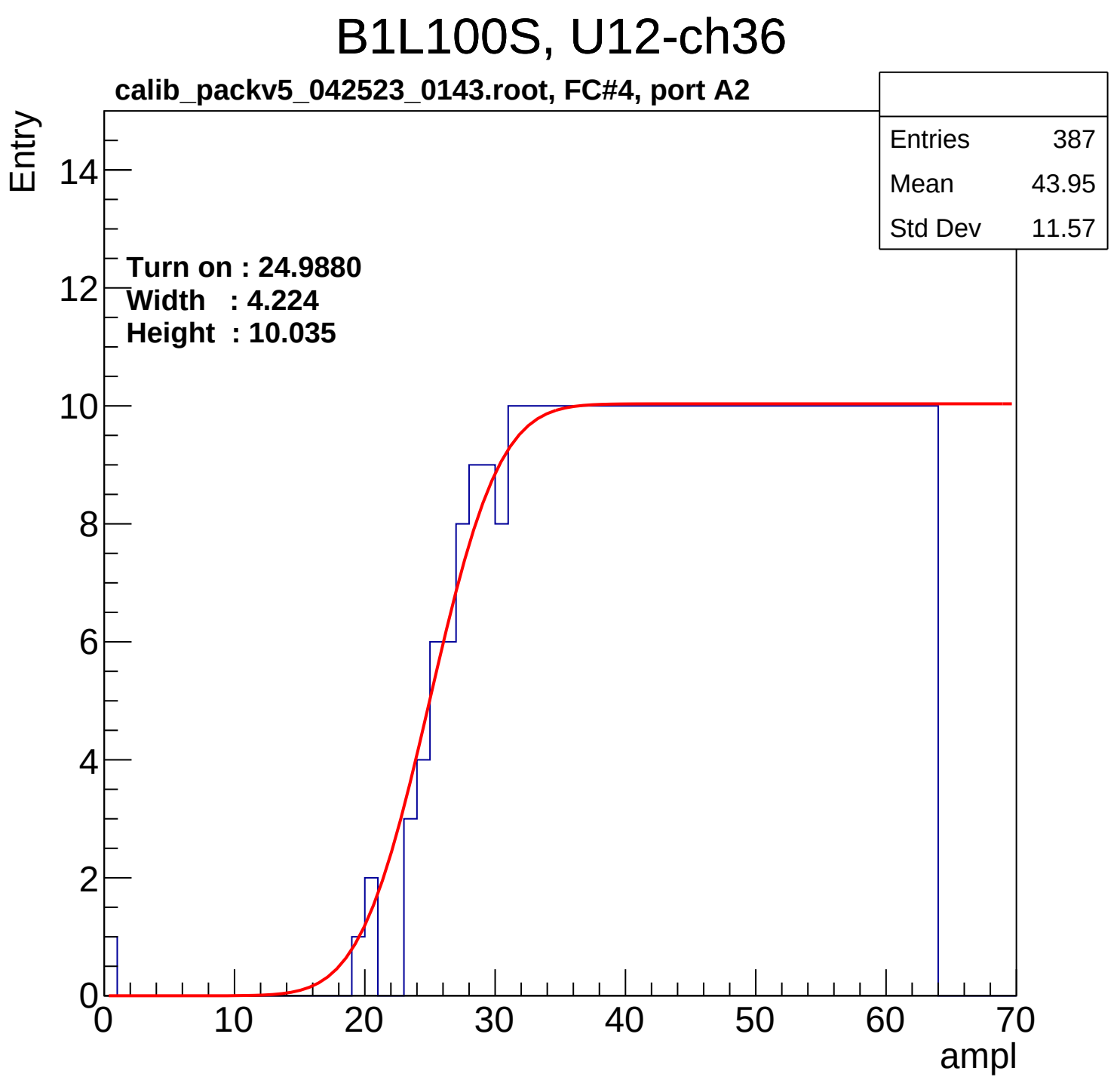

B1L100S, U12-ch31
calib_packv5_042523_0143.root, FC#4, port A2
Entries 363
Mean 45.13
Std Dev 10.95
Turn on : 28.1471
Width : 3.562
Height : 10.036
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

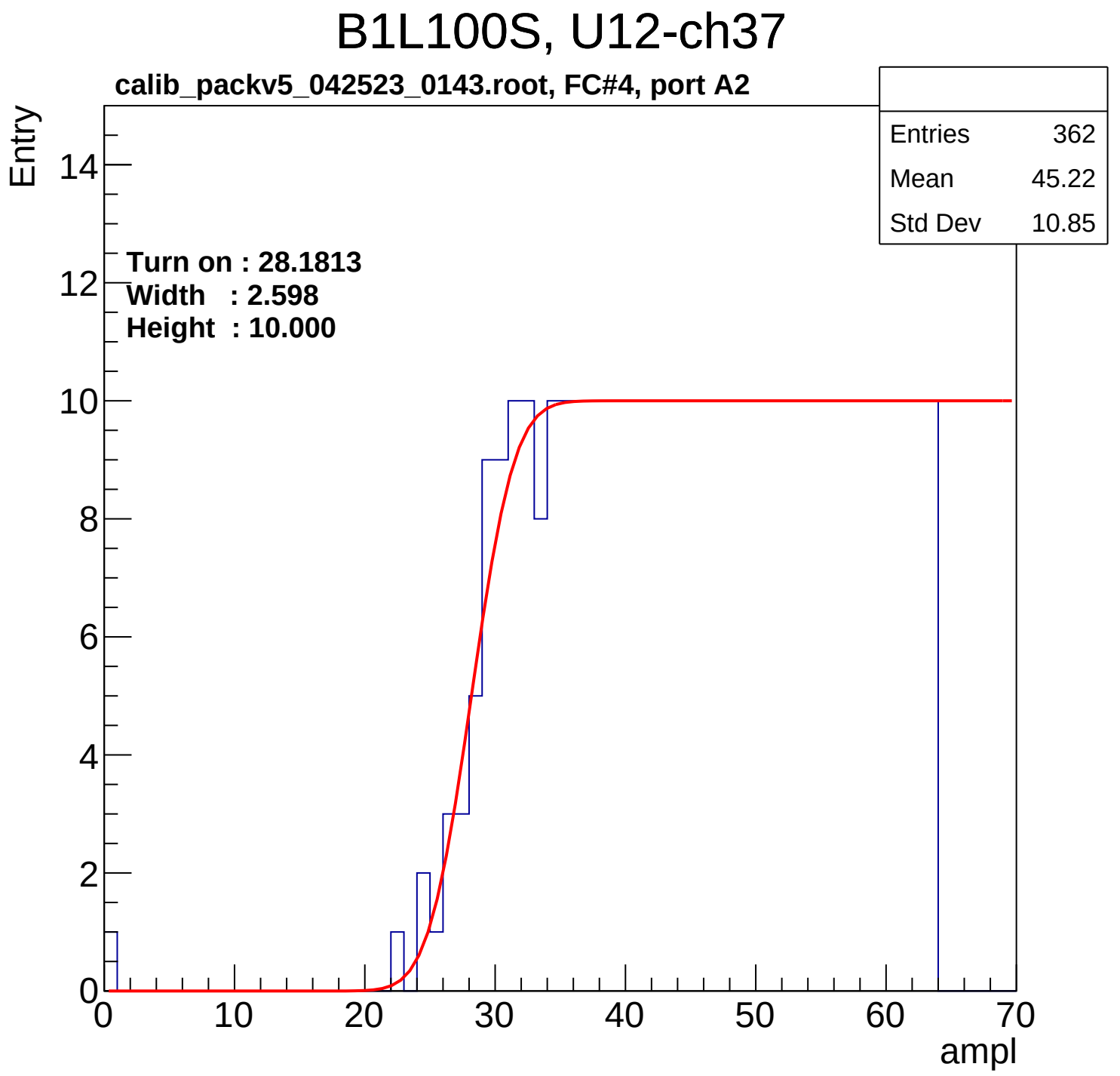

B1L100S, U12-ch32
calib_packv5_042523_0143.root, FC#4, port A2
Entries 365
Mean 45.02
Std Dev 11
Turn on : 27.5637
Width : 3.351
Height : 9.975
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

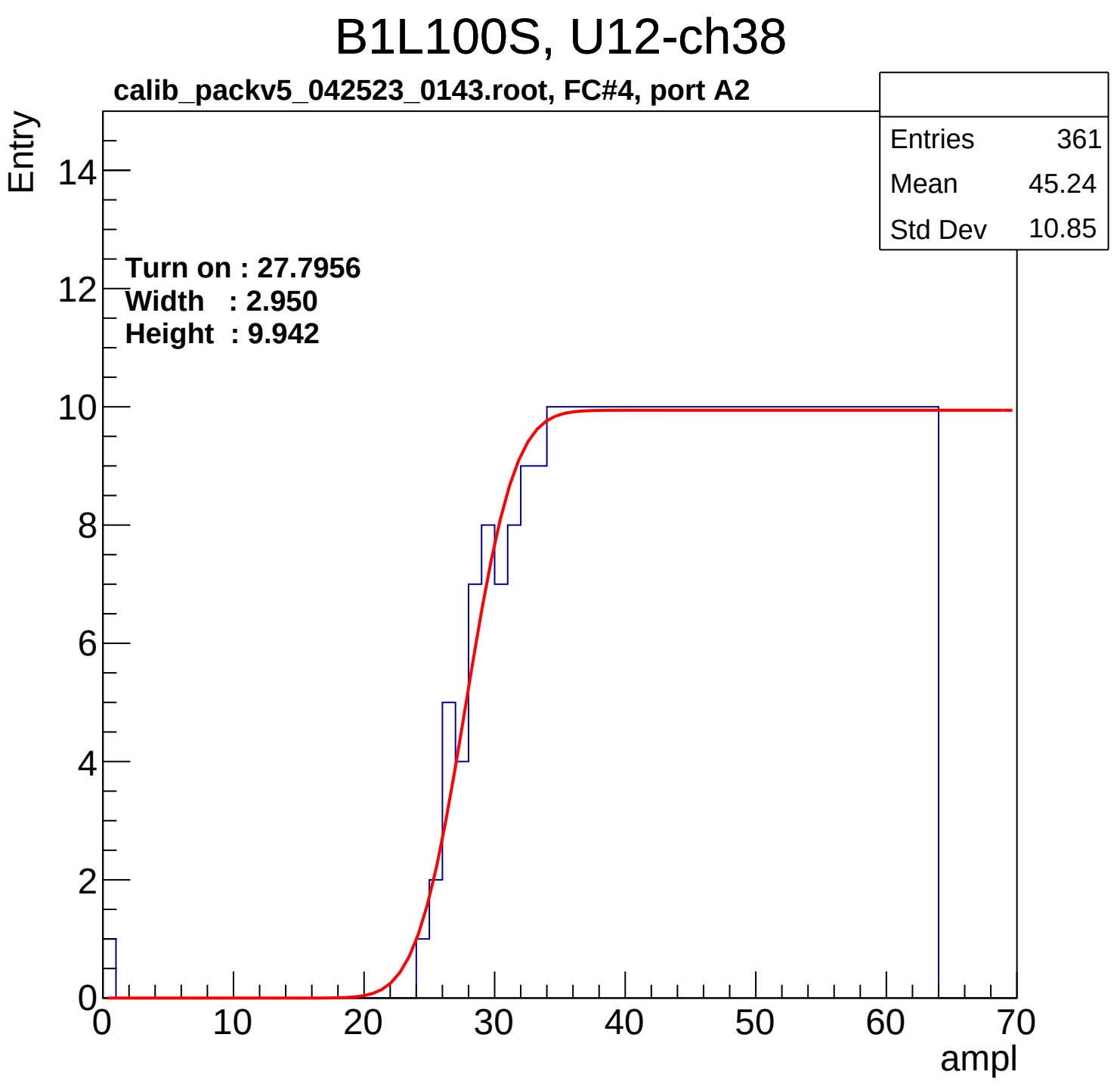

B1L100S, U12-ch33
calib_packv5_042523_0143.root, FC#4, port A2
Entries 361
Mean 45.17
Std Dev 11.07
Turn on : 28.5477
Width : 2.722
Height : 9.996
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

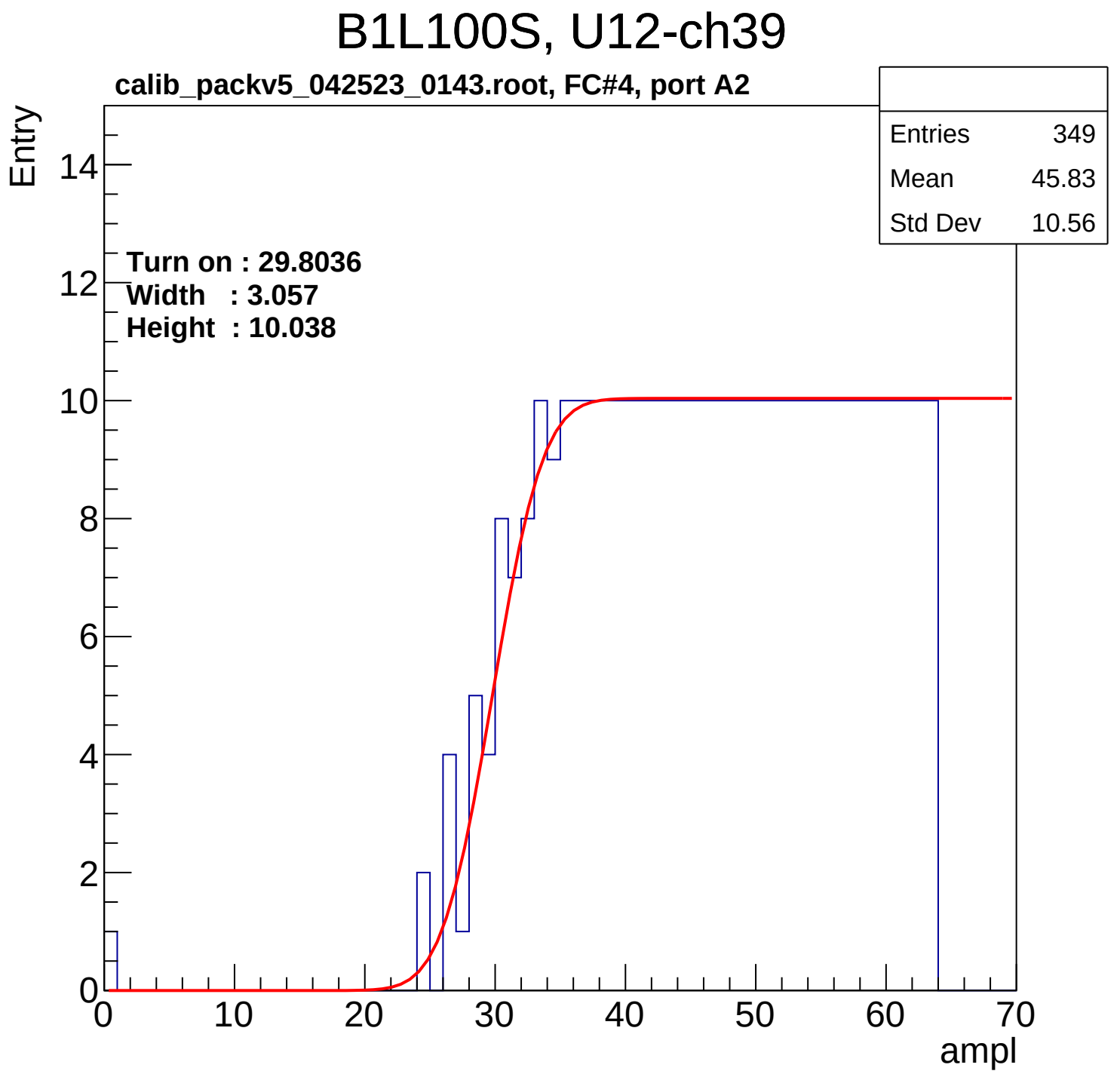

B1L100S, U12-ch34
calib_packv5_042523_0143.root, FC#4, port A2
Entries 382
Mean 44.2
Std Dev 11.43
Turn on : 25.9579
Width : 3.478
Height : 10.012
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

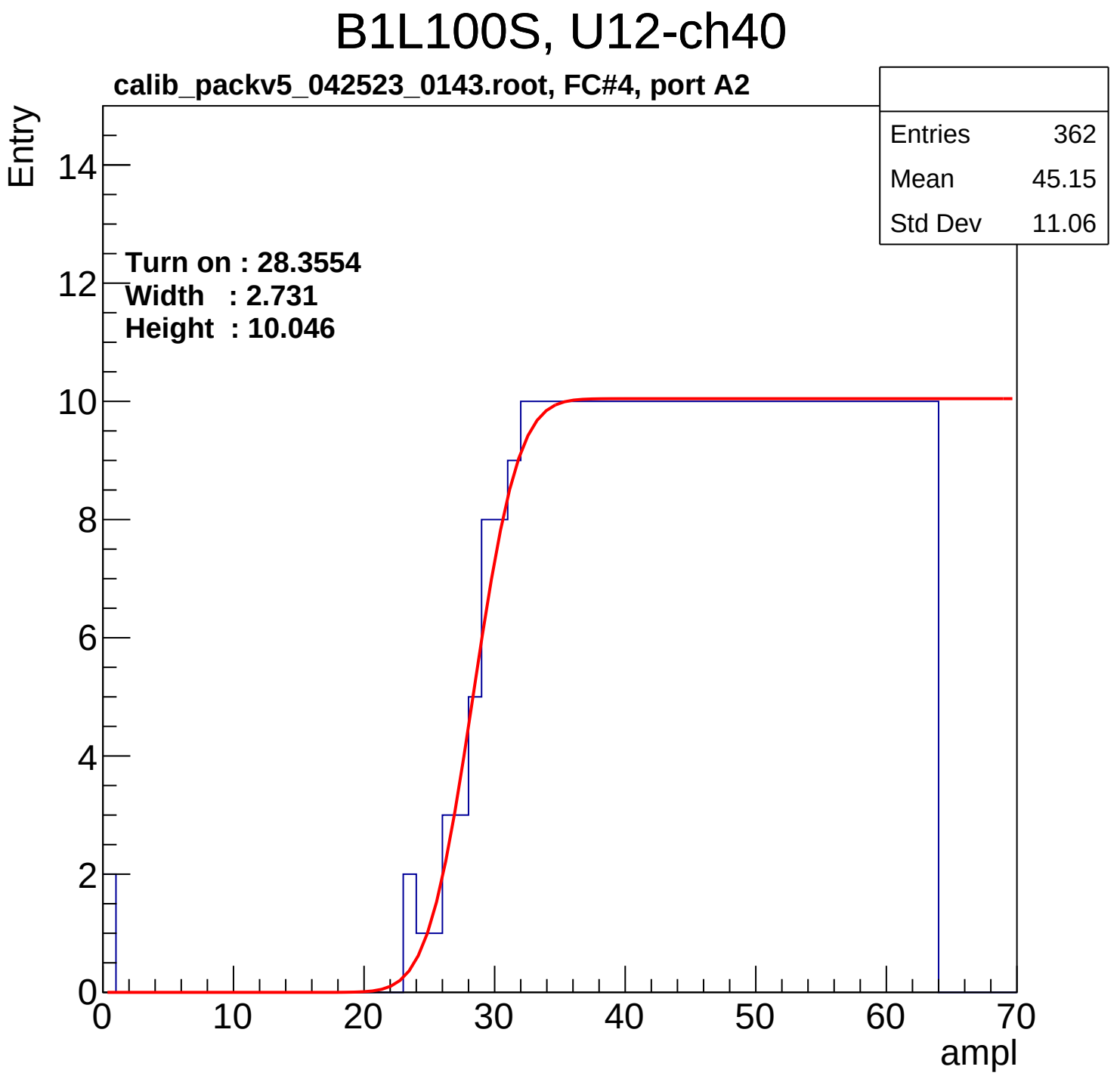

B1L100S, U12-ch35
calib_packv5_042523_0143.root, FC#4, port A2
Entries 365
Mean 45.1
Std Dev 10.88
Turn on : 27.6960
Width : 2.126
Height : 9.986
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

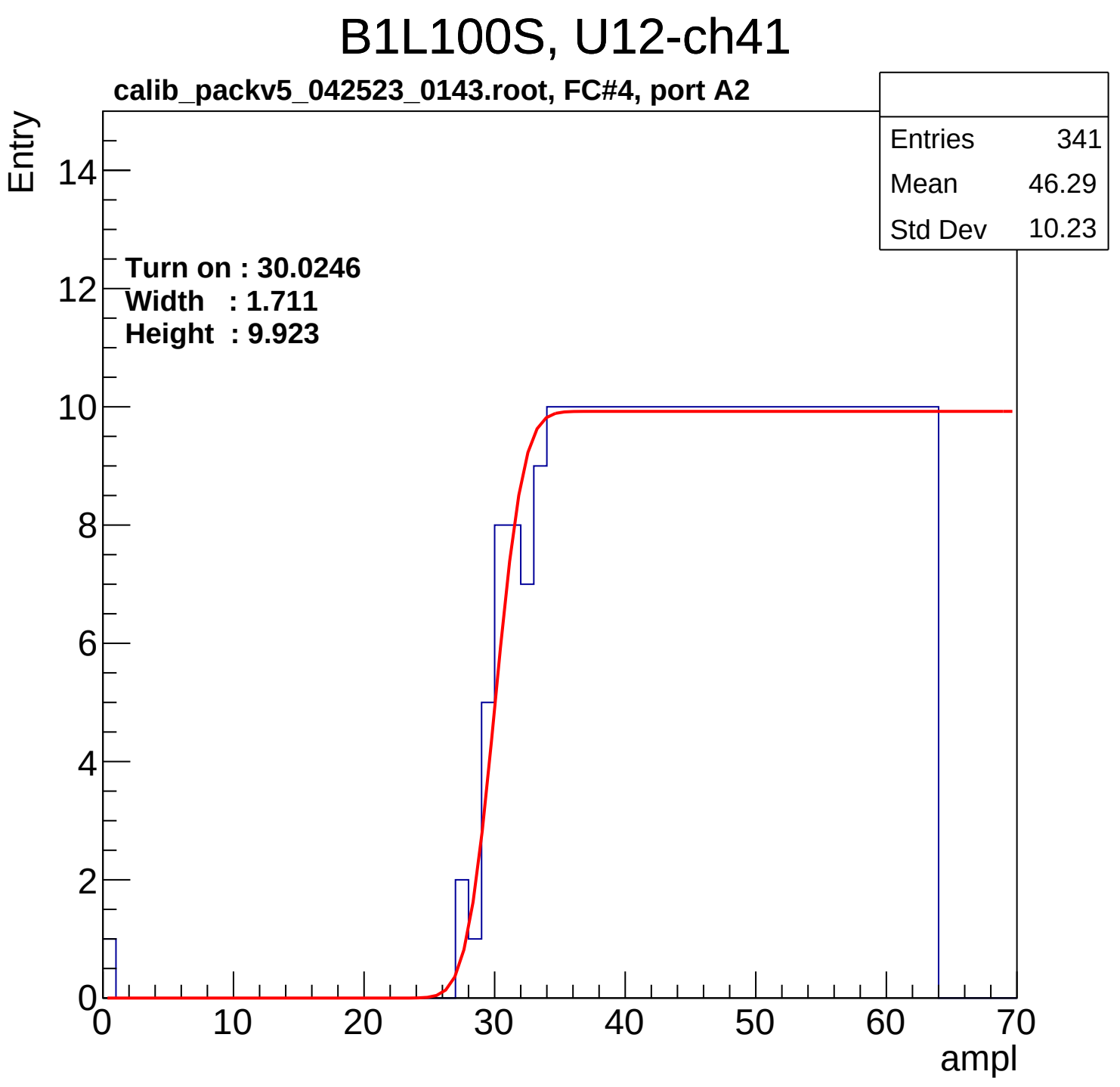

B1L100S, U12-ch36
calib_packv5_042523_0143.root, FC#4, port A2
Entries 387
Mean 43.95
Std Dev 11.57
Turn on : 24.9880
Width : 4.224
Height : 10.035
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

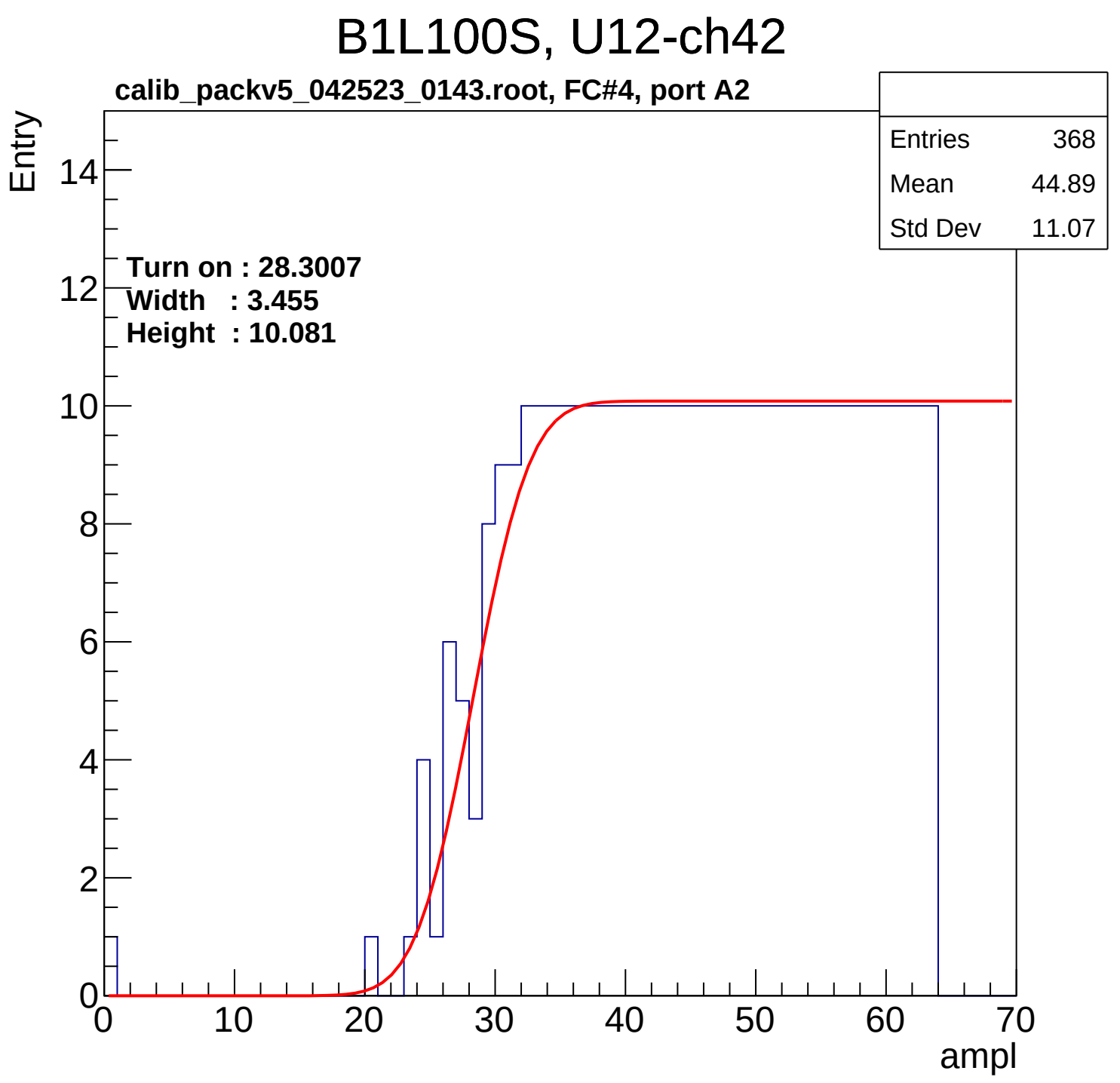

B1L100S, U12-ch37
calib_packv5_042523_0143.root, FC#4, port A2
Entries 362
Mean 45.22
Std Dev 10.85
Turn on : 28.1813
Width : 2.598
Height : 10.000
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

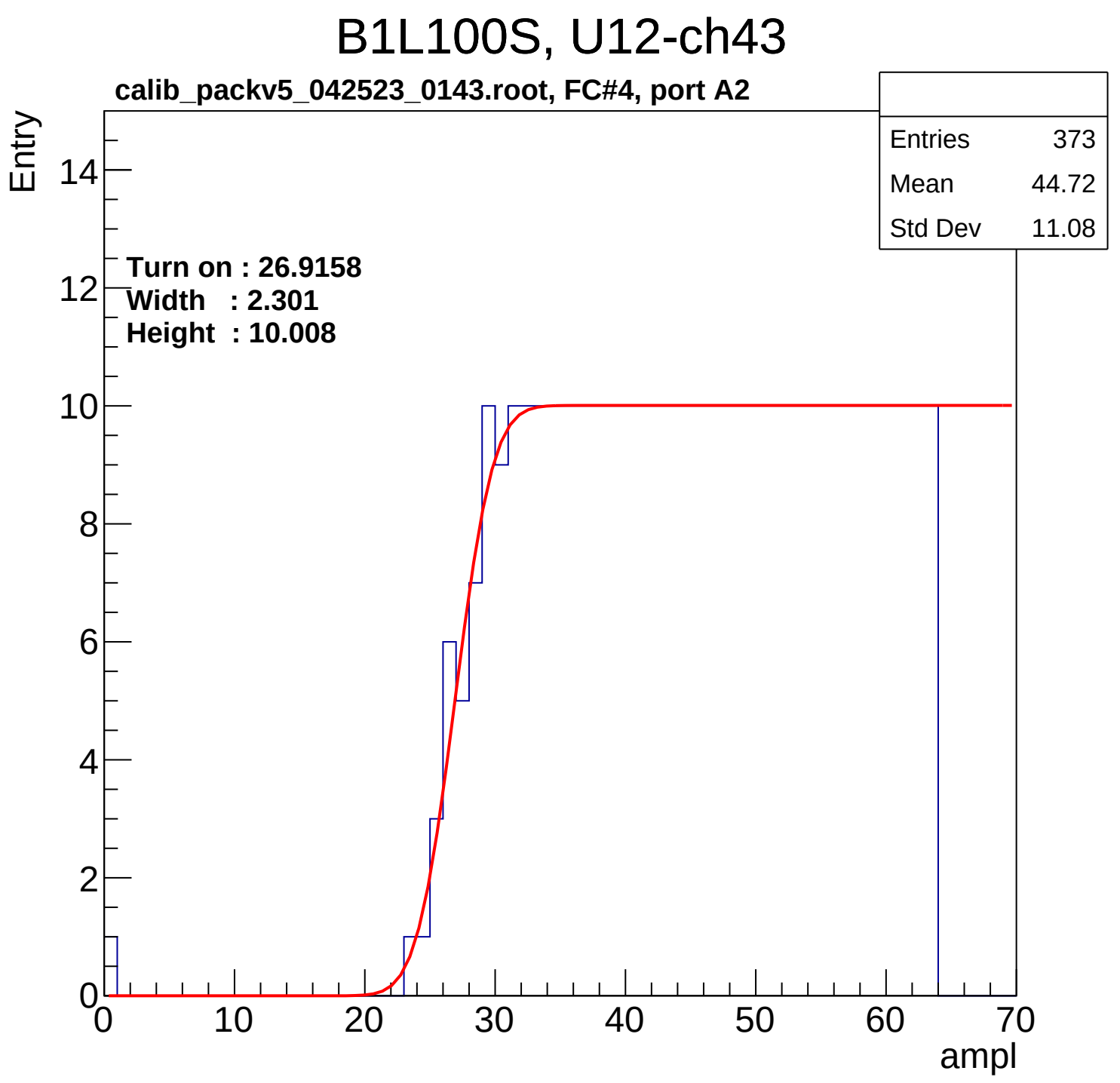

B1L100S, U12-ch38
calib_packv5_042523_0143.root, FC#4, port A2
Entries 361
Mean 45.24
Std Dev 10.85
Turn on : 27.7956
Width : 2.950
Height : 9.942
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

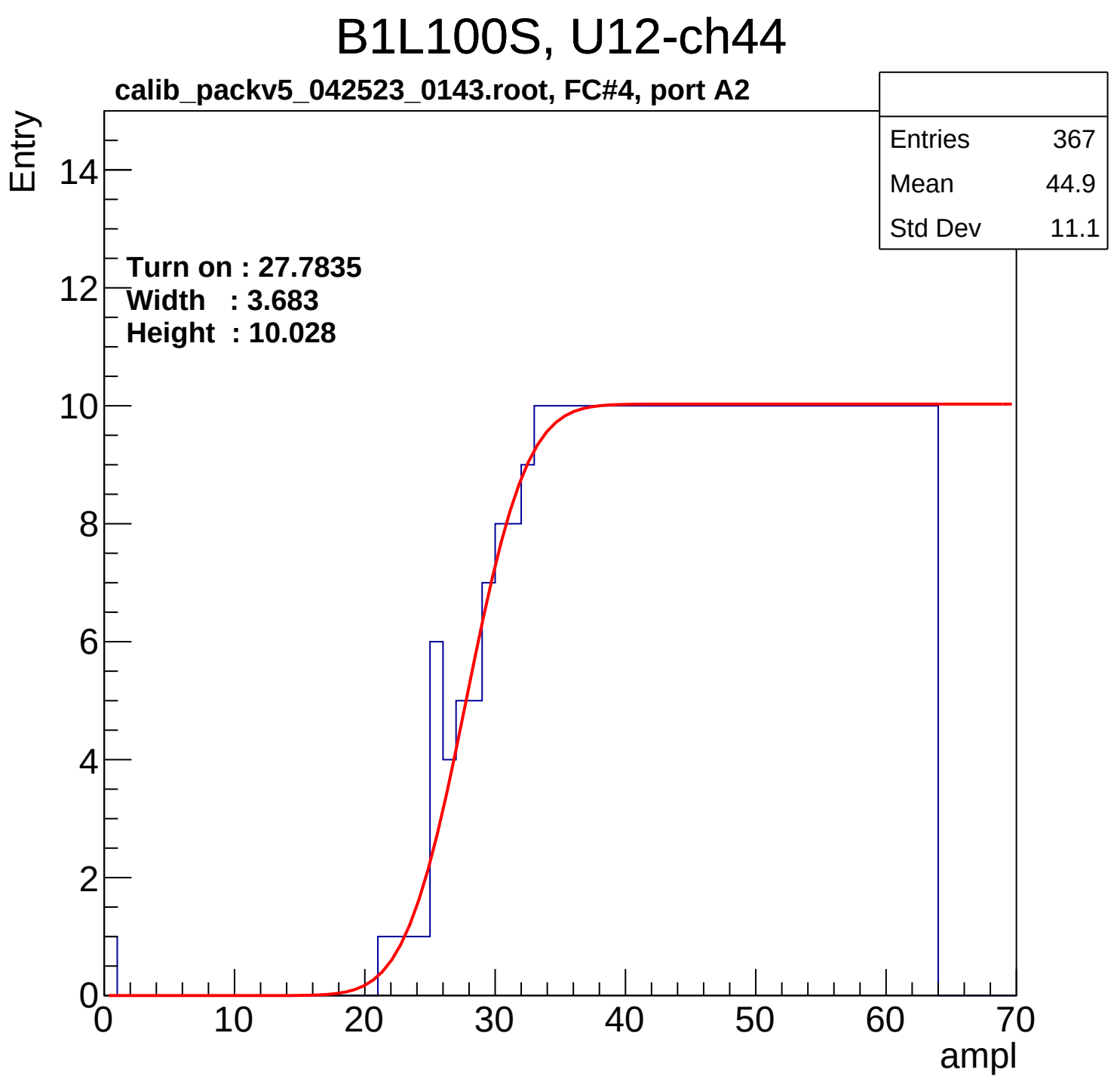

B1L100S, U12-ch39
calib_packv5_042523_0143.root, FC#4, port A2
Entries 349
Mean 45.83
Std Dev 10.56
Turn on : 29.8036
Width : 3.057
Height : 10.038
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

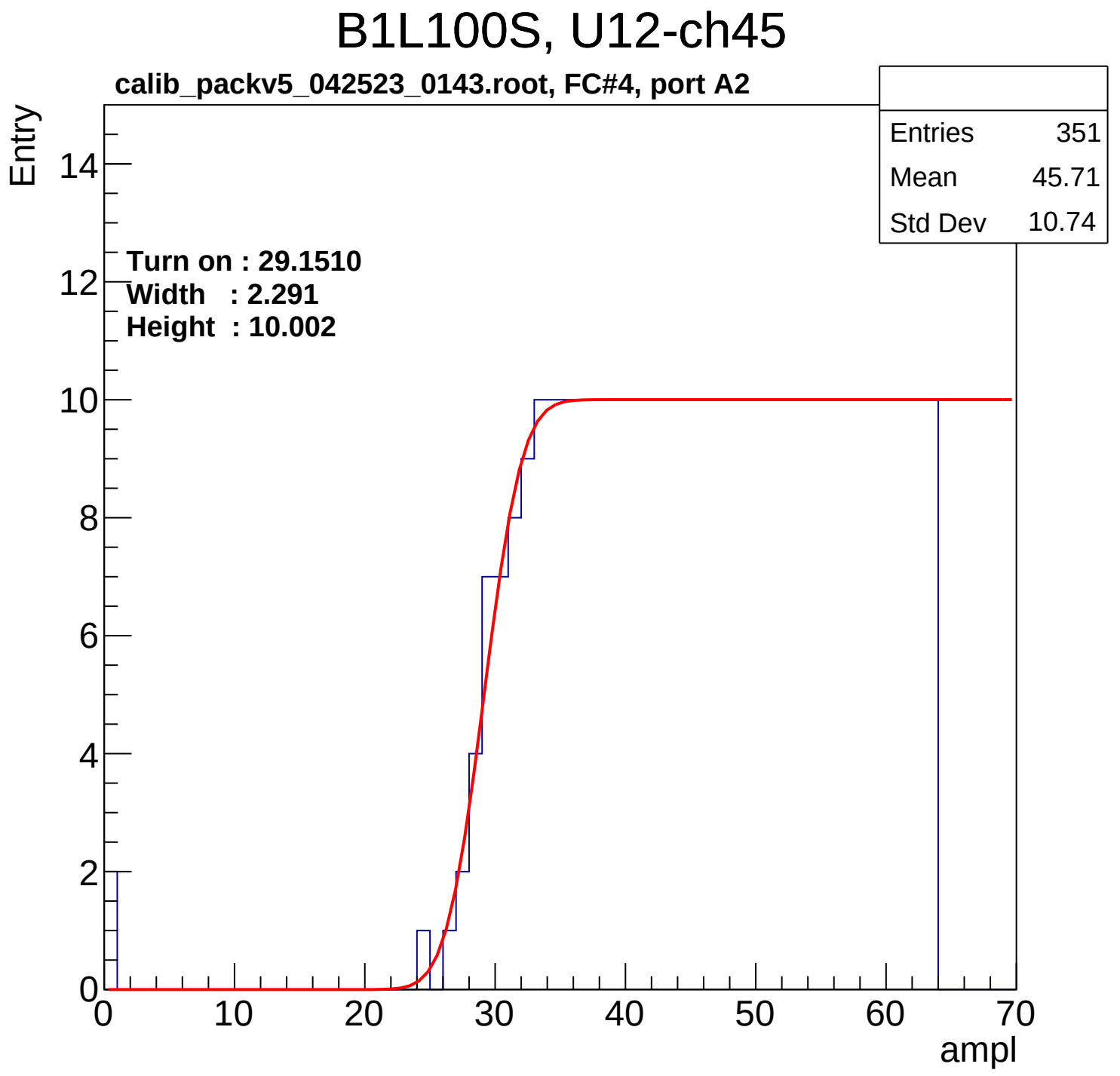

B1L100S, U12-ch40
calib_packv5_042523_0143.root, FC#4, port A2
Entries 362
Mean 45.15
Std Dev 11.06
Turn on : 28.3554
Width : 2.731
Height : 10.046
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

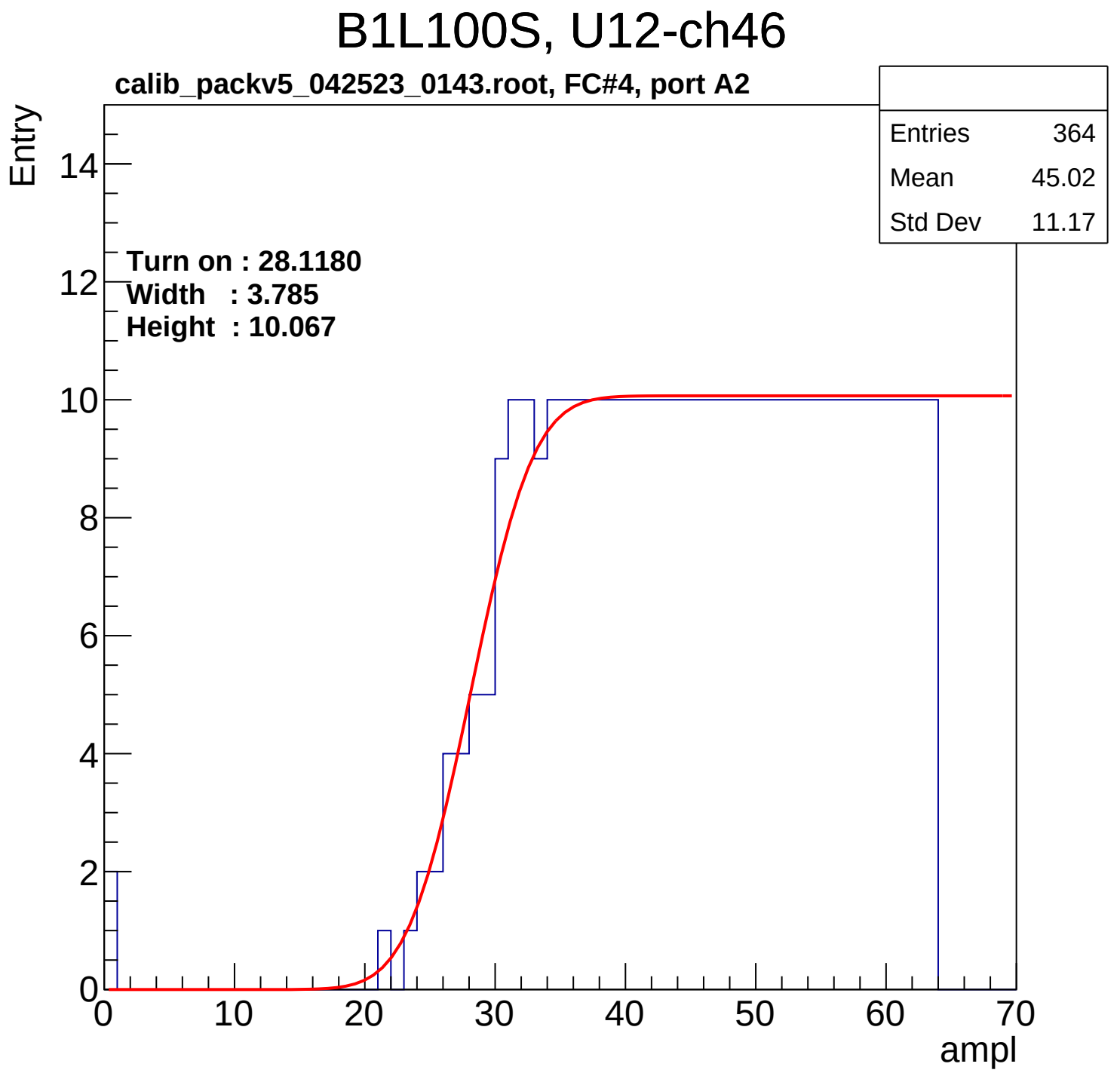

B1L100S, U12-ch41
calib_packv5_042523_0143.root, FC#4, port A2
Entries 341
Mean 46.29
Std Dev 10.23
Turn on : 30.0246
Width : 1.711
Height : 9.923
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

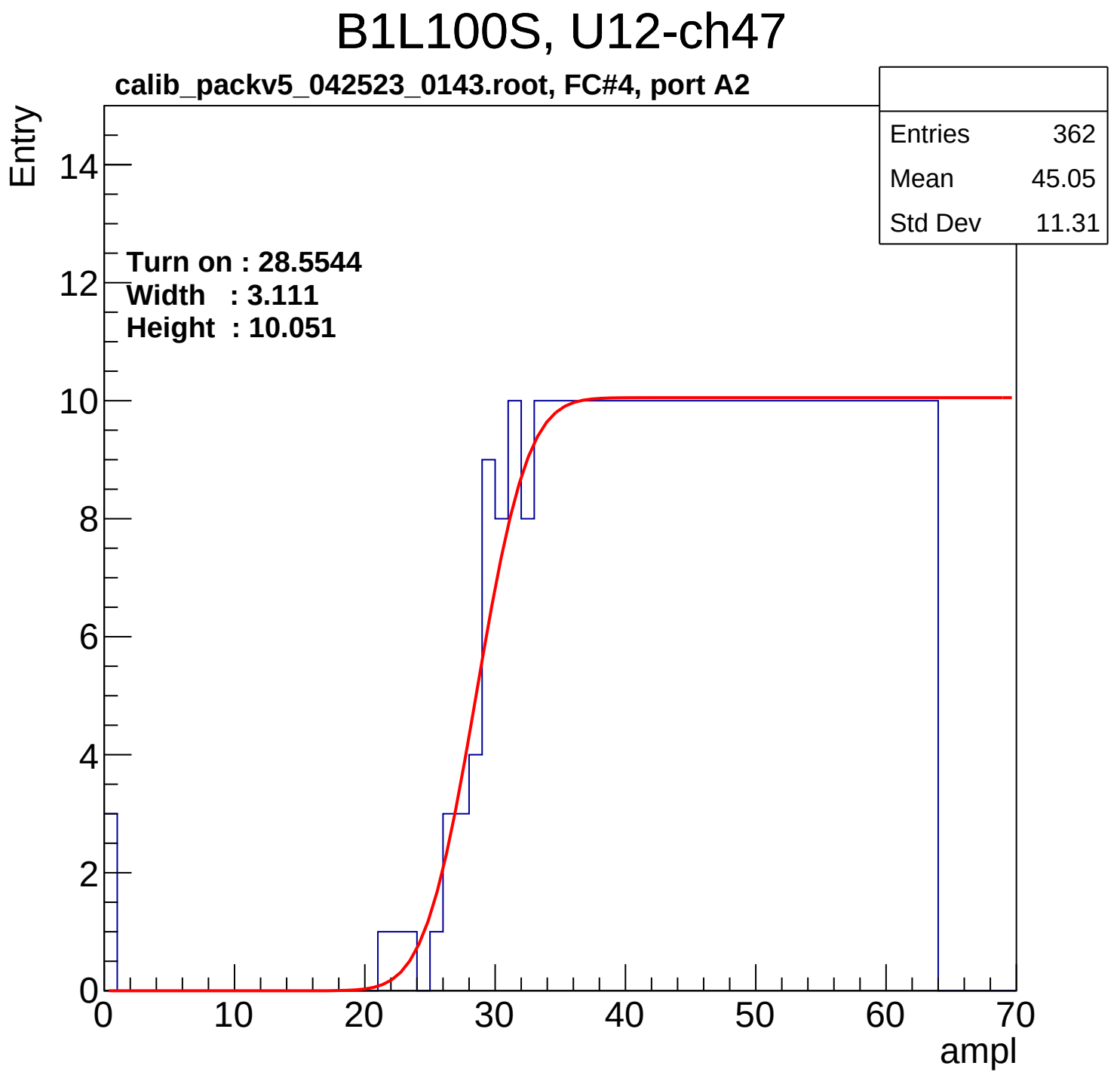

B1L100S, U12-ch42
calib_packv5_042523_0143.root, FC#4, port A2
Entries 368
Mean 44.89
Std Dev 11.07
Turn on : 28.3007
Width : 3.455
Height : 10.081
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

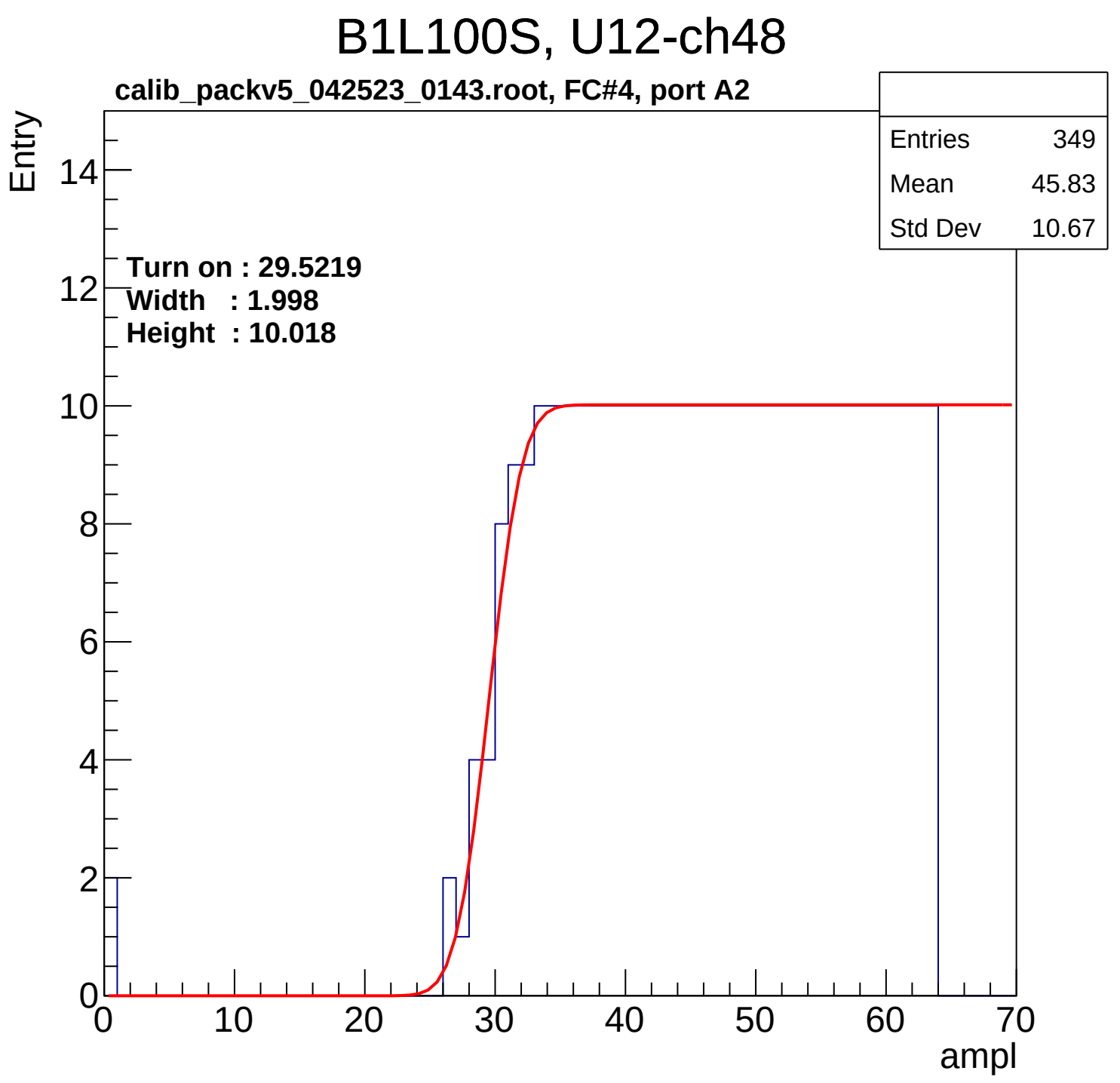

B1L100S, U12-ch43
calib_packv5_042523_0143.root, FC#4, port A2
Entries 373
Mean 44.72
Std Dev 11.08
Turn on : 26.9158
Width : 2.301
Height : 10.008
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

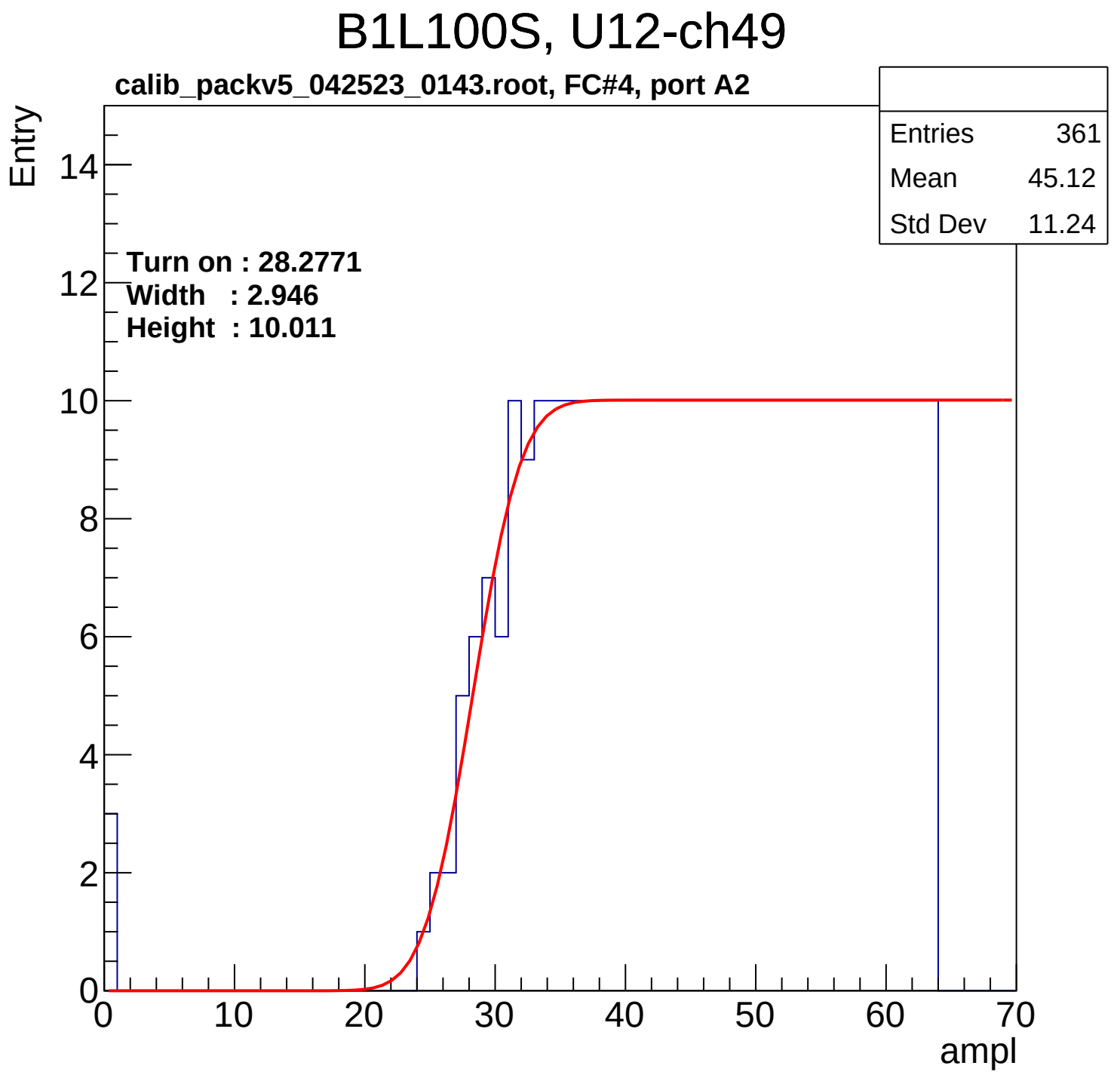

B1L100S, U12-ch44
calib_packv5_042523_0143.root, FC#4, port A2
Entries 367
Mean 44.9
Std Dev 11.1
Turn on : 27.7835
Width : 3.683
Height : 10.028
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

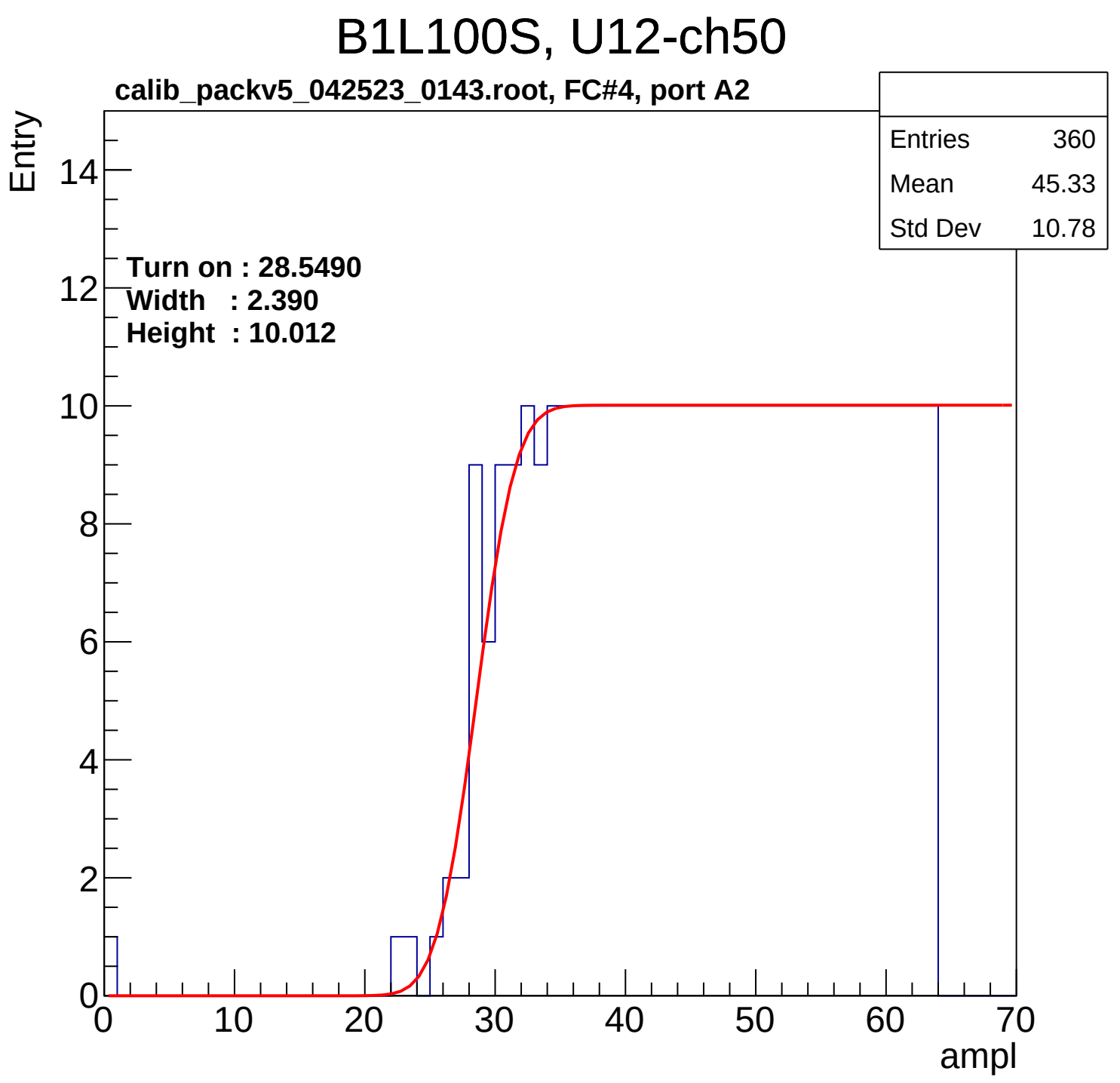

B1L100S, U12-ch45
calib_packv5_042523_0143.root, FC#4, port A2
Entries 351
Mean 45.71
Std Dev 10.74
Turn on : 29.1510
Width : 2.291
Height : 10.002
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

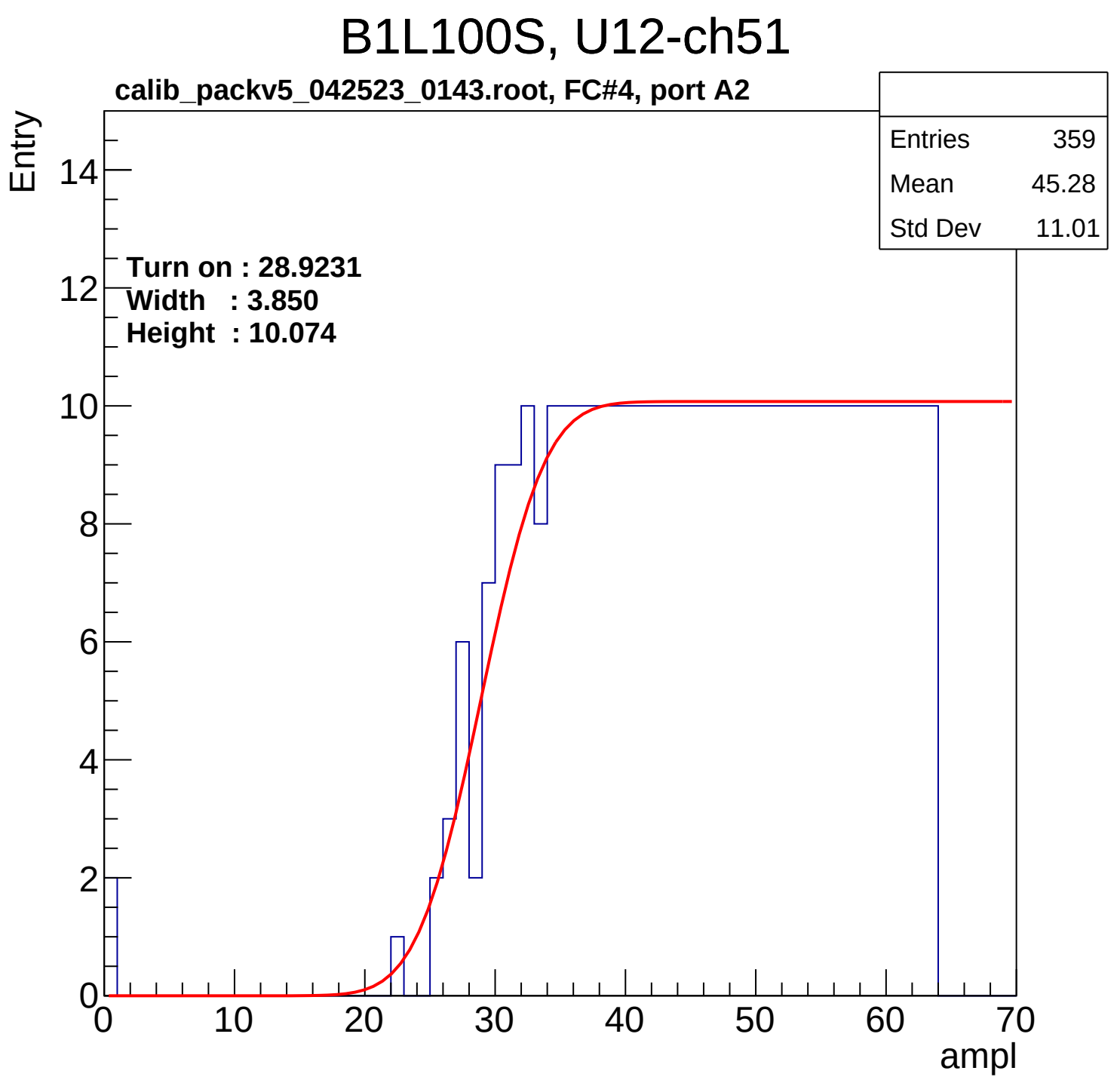

B1L100S, U12-ch46
calib_packv5_042523_0143.root, FC#4, port A2
Entries 364
Mean 45.02
Std Dev 11.17
Turn on : 28.1180
Width : 3.785
Height : 10.067
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

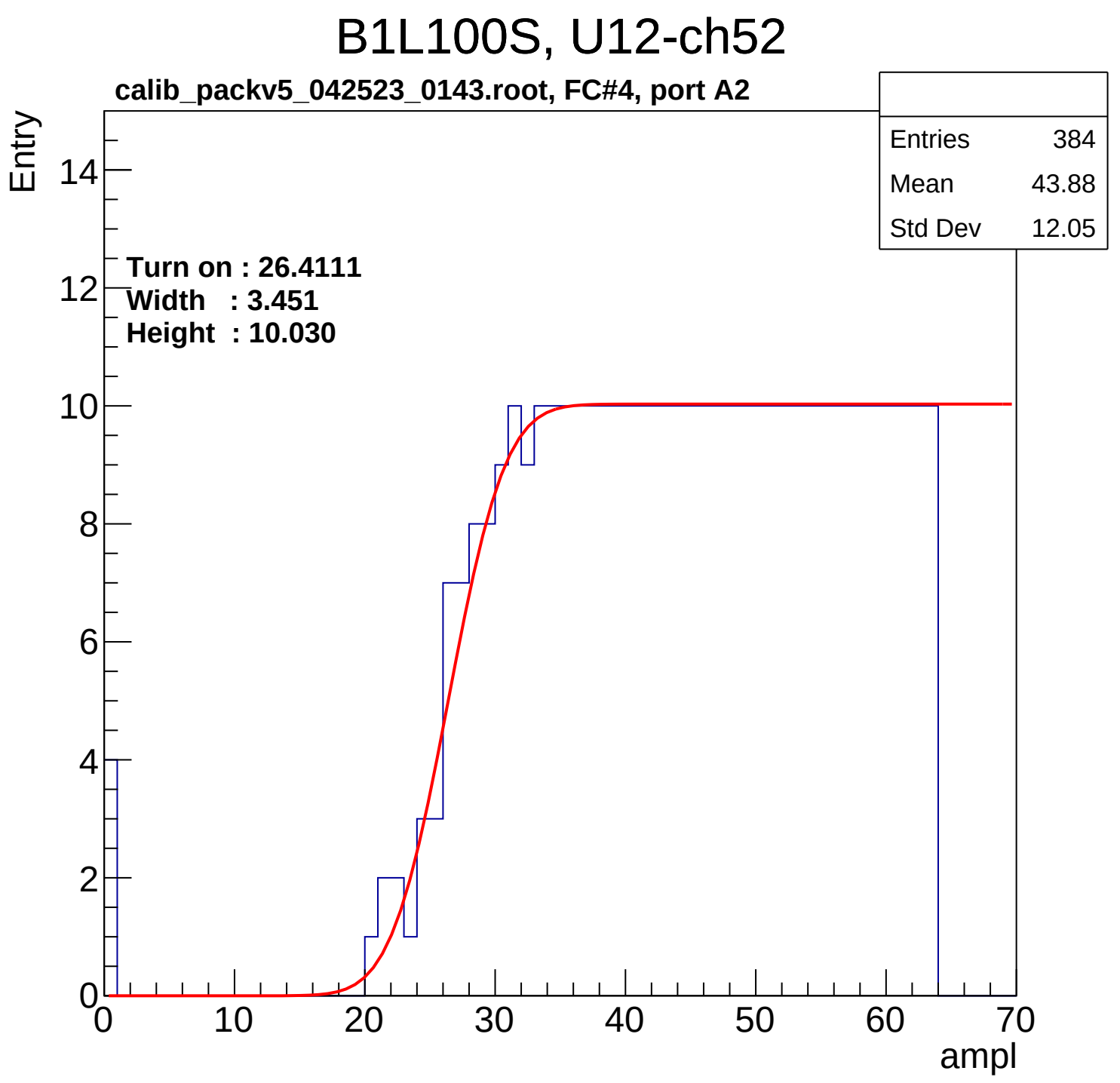

B1L100S, U12-ch47
calib_packv5_042523_0143.root, FC#4, port A2
Entries 362
Mean 45.05
Std Dev 11.31
Turn on : 28.5544
Width : 3.111
Height : 10.051
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

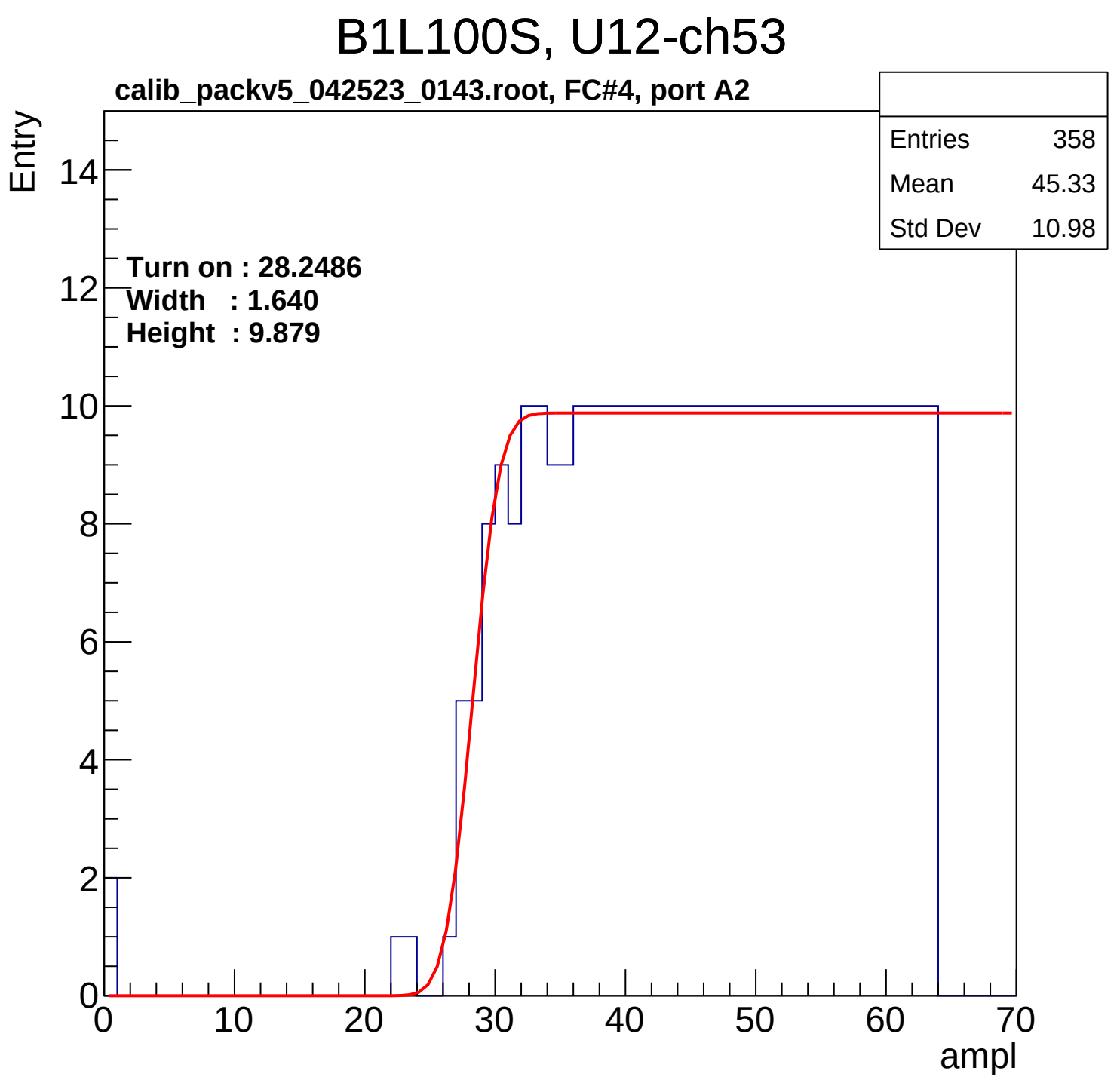

B1L100S, U12-ch48
calib_packv5_042523_0143.root, FC#4, port A2
Entries 349
Mean 45.83
Std Dev 10.67
Turn on : 29.5219
Width : 1.998
Height : 10.018
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

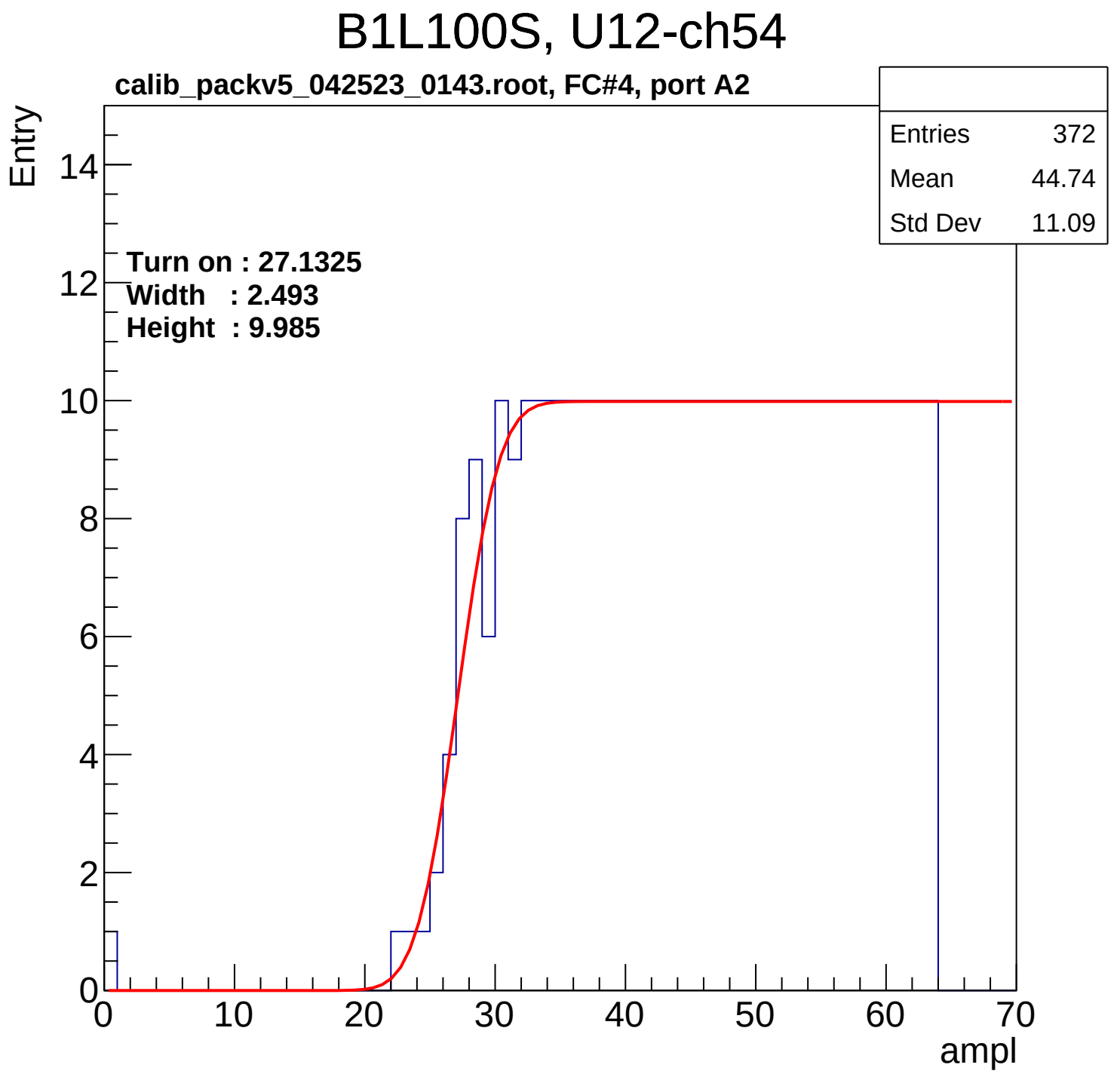

B1L100S, U12-ch49
calib_packv5_042523_0143.root, FC#4, port A2
Entries 361
Mean 45.12
Std Dev 11.24
Turn on : 28.2771
Width : 2.946
Height : 10.011
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

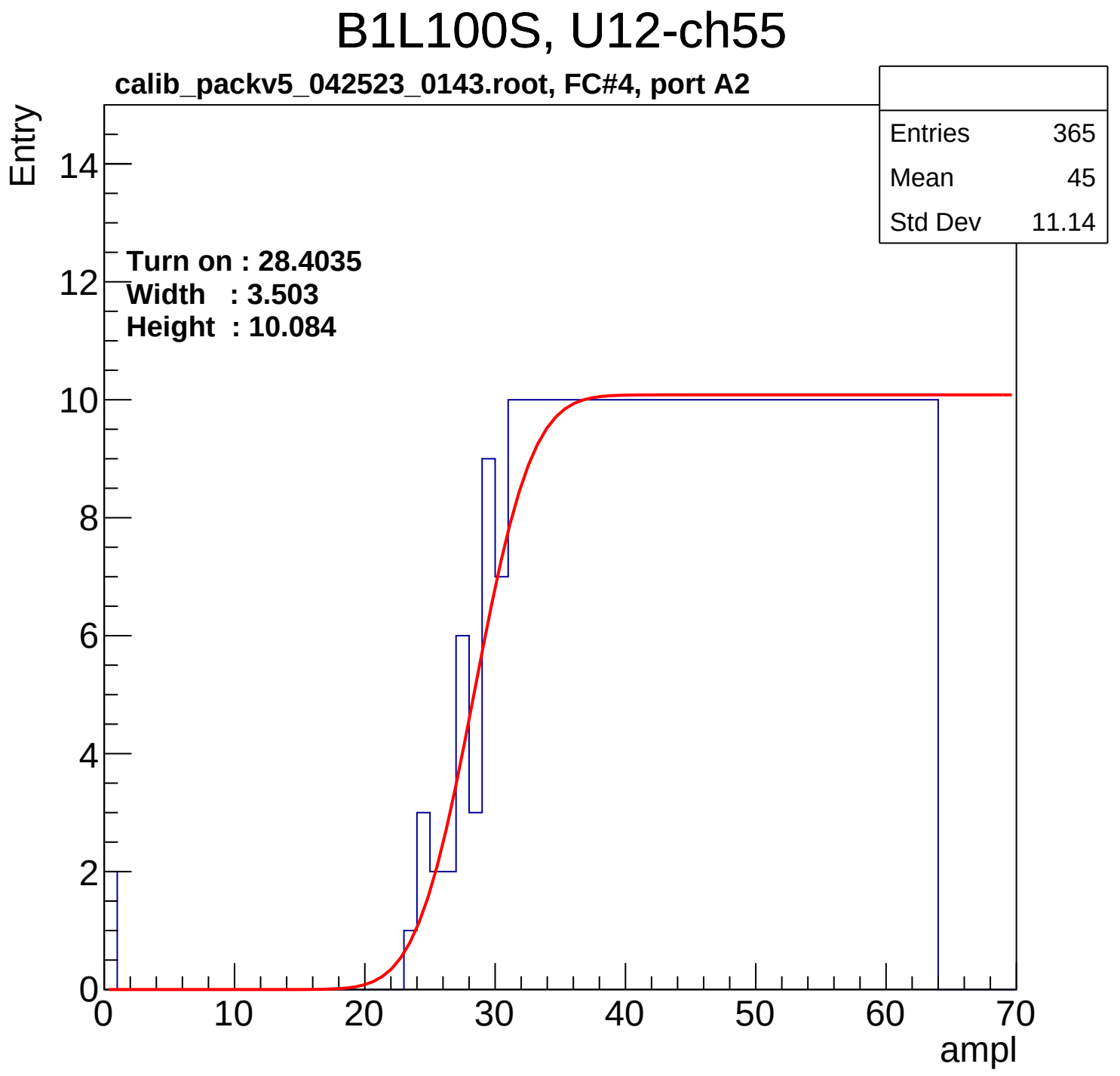

B1L100S, U12-ch50
calib_packv5_042523_0143.root, FC#4, port A2
Entries 360
Mean 45.33
Std Dev 10.78
Turn on : 28.5490
Width : 2.390
Height : 10.012
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

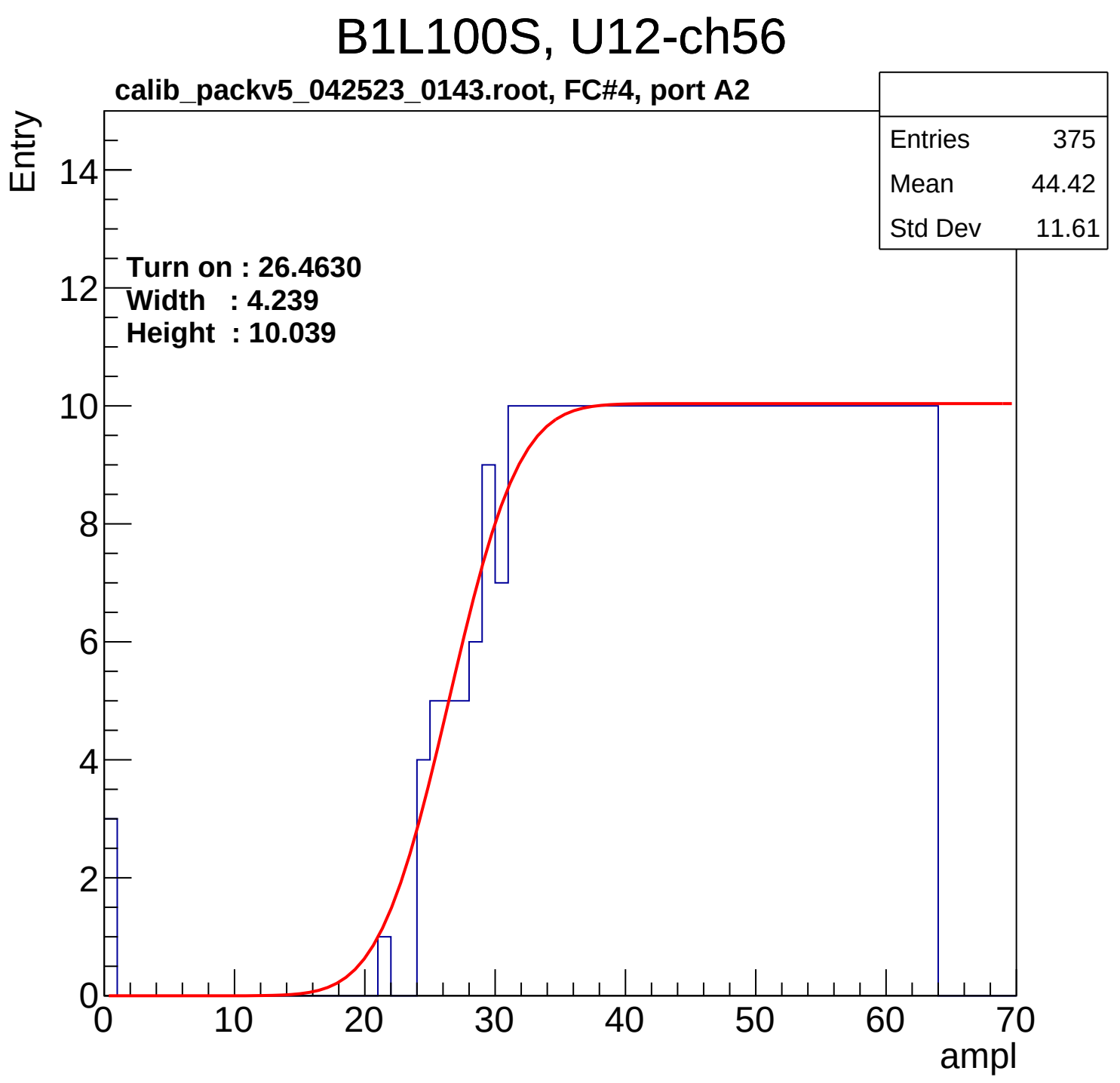

B1L100S, U12-ch51
calib_packv5_042523_0143.root, FC#4, port A2
Entries 359
Mean 45.28
Std Dev 11.01
Turn on : 28.9231
Width : 3.850
Height : 10.074
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

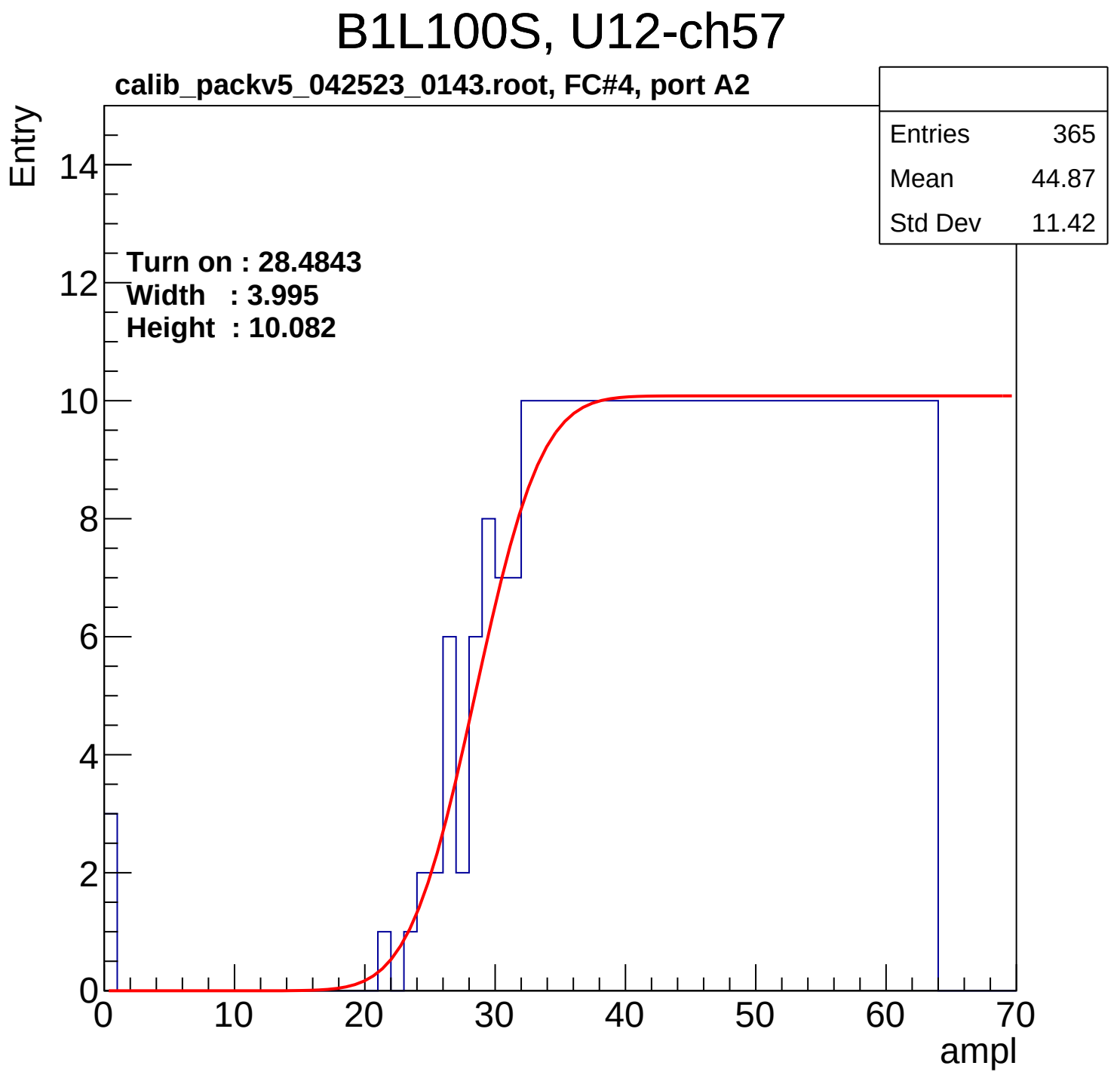

B1L100S, U12-ch52
calib_packv5_042523_0143.root, FC#4, port A2
Entries 384
Mean 43.88
Std Dev 12.05
Turn on : 26.4111
Width : 3.451
Height : 10.030
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

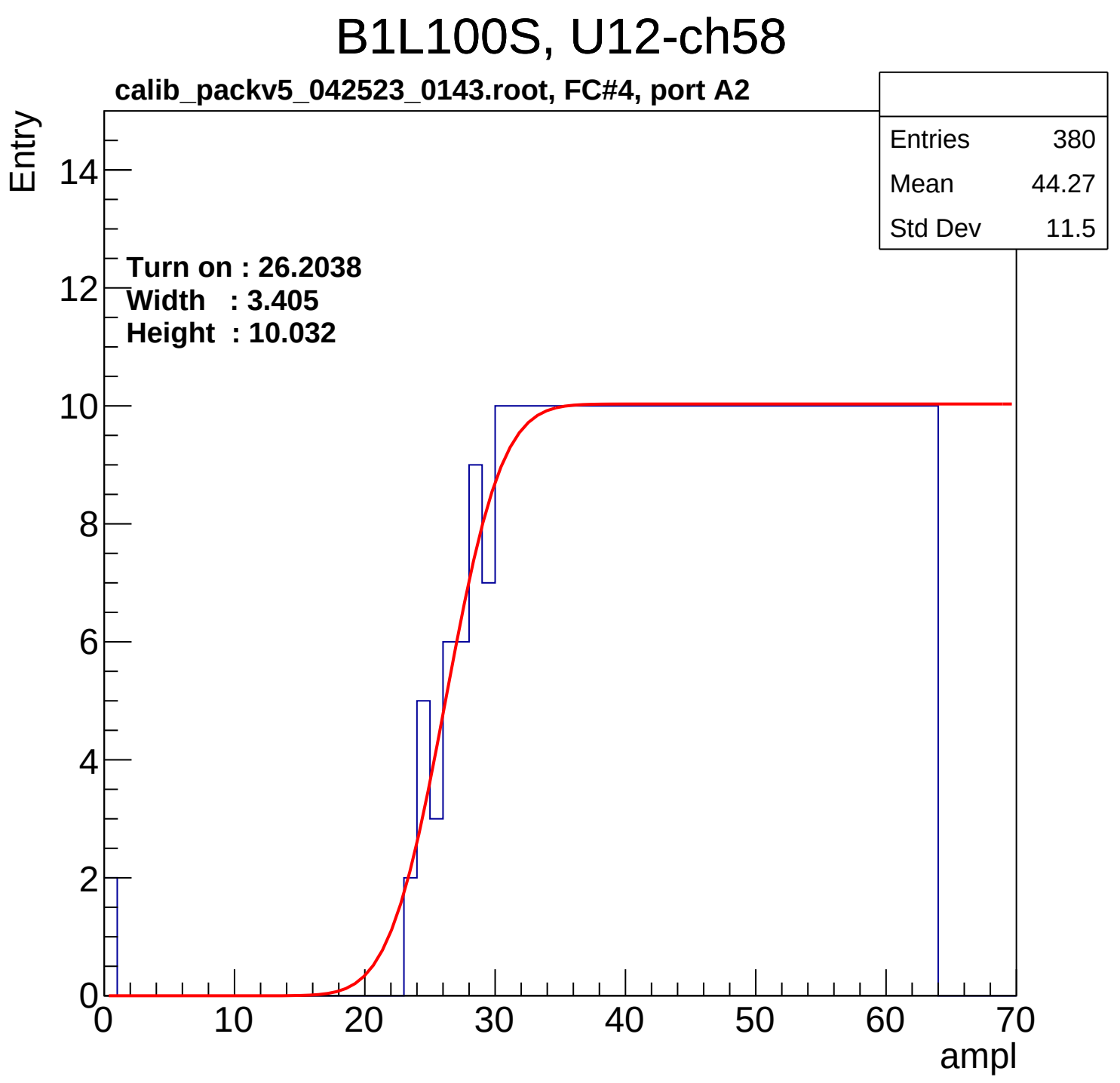

B1L100S, U12-ch53
calib_packv5_042523_0143.root, FC#4, port A2
Entries 358
Mean 45.33
Std Dev 10.98
Turn on : 28.2486
Width : 1.640
Height : 9.879
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

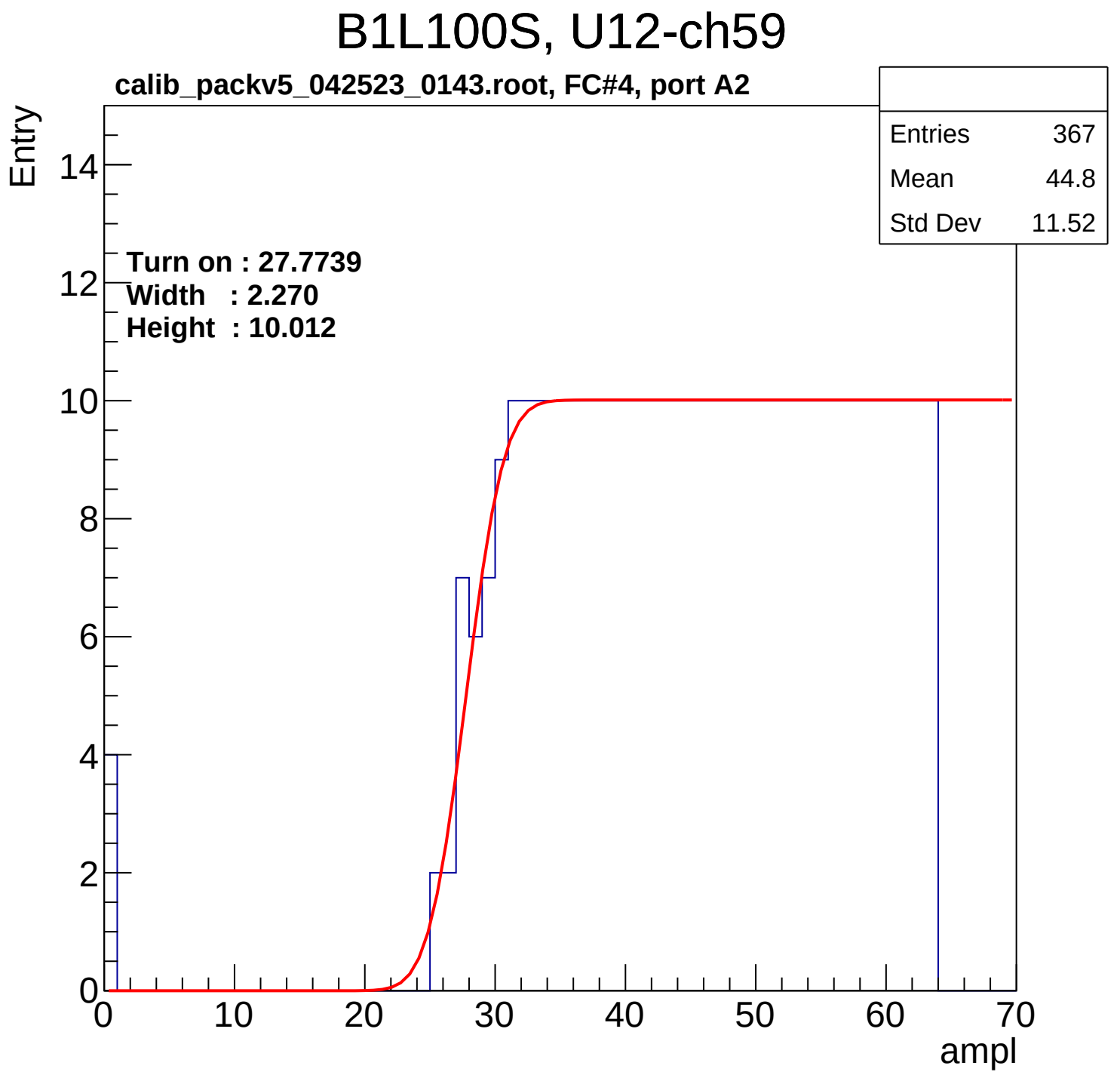

B1L100S, U12-ch54
calib_packv5_042523_0143.root, FC#4, port A2
Entries 372
Mean 44.74
Std Dev 11.09
Turn on : 27.1325
Width : 2.493
Height : 9.985
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

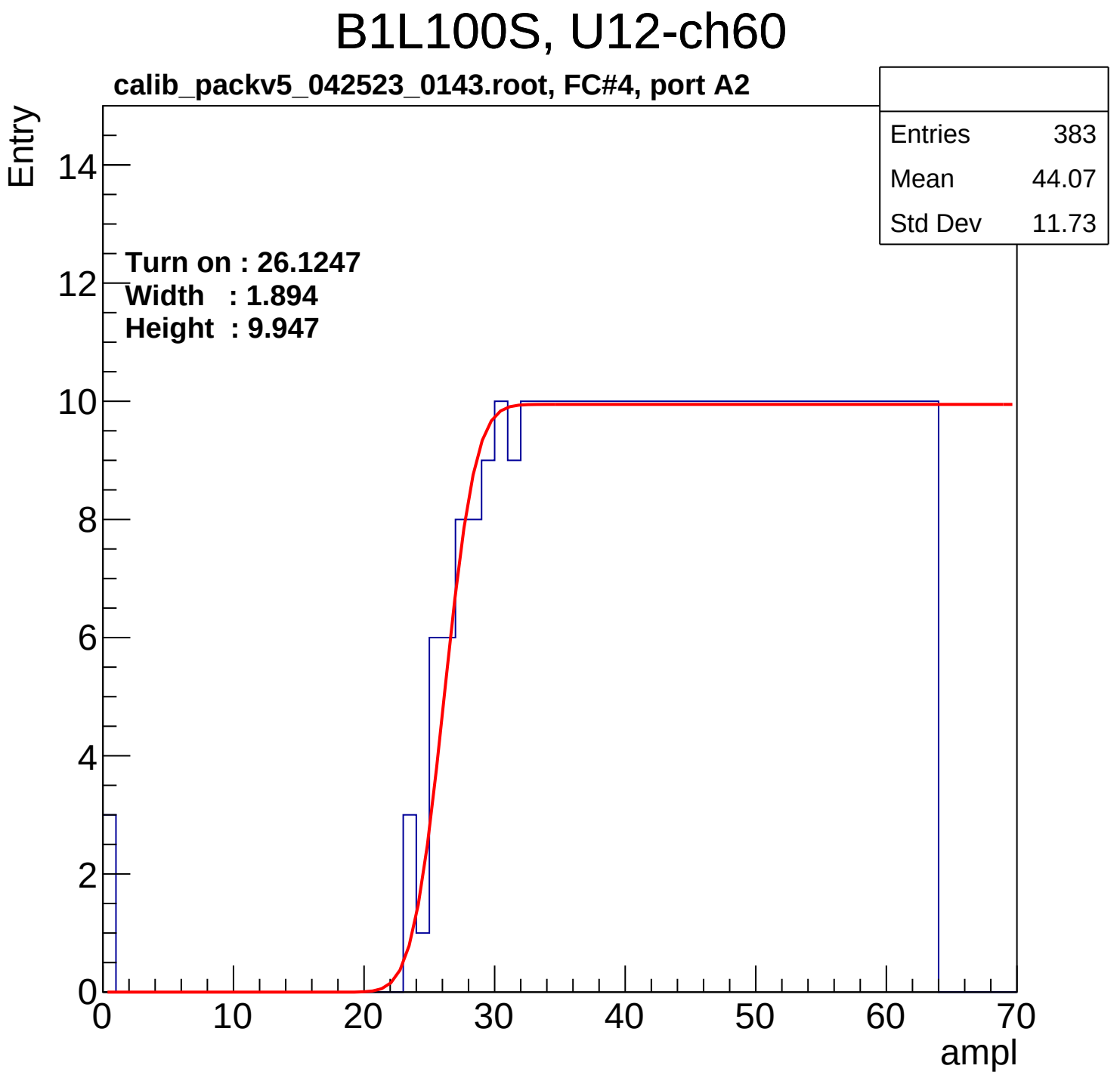

B1L100S, U12-ch55
calib_packv5_042523_0143.root, FC#4, port A2
Entries 365
Mean 45
Std Dev 11.14
Turn on : 28.4035
Width : 3.503
Height : 10.084
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

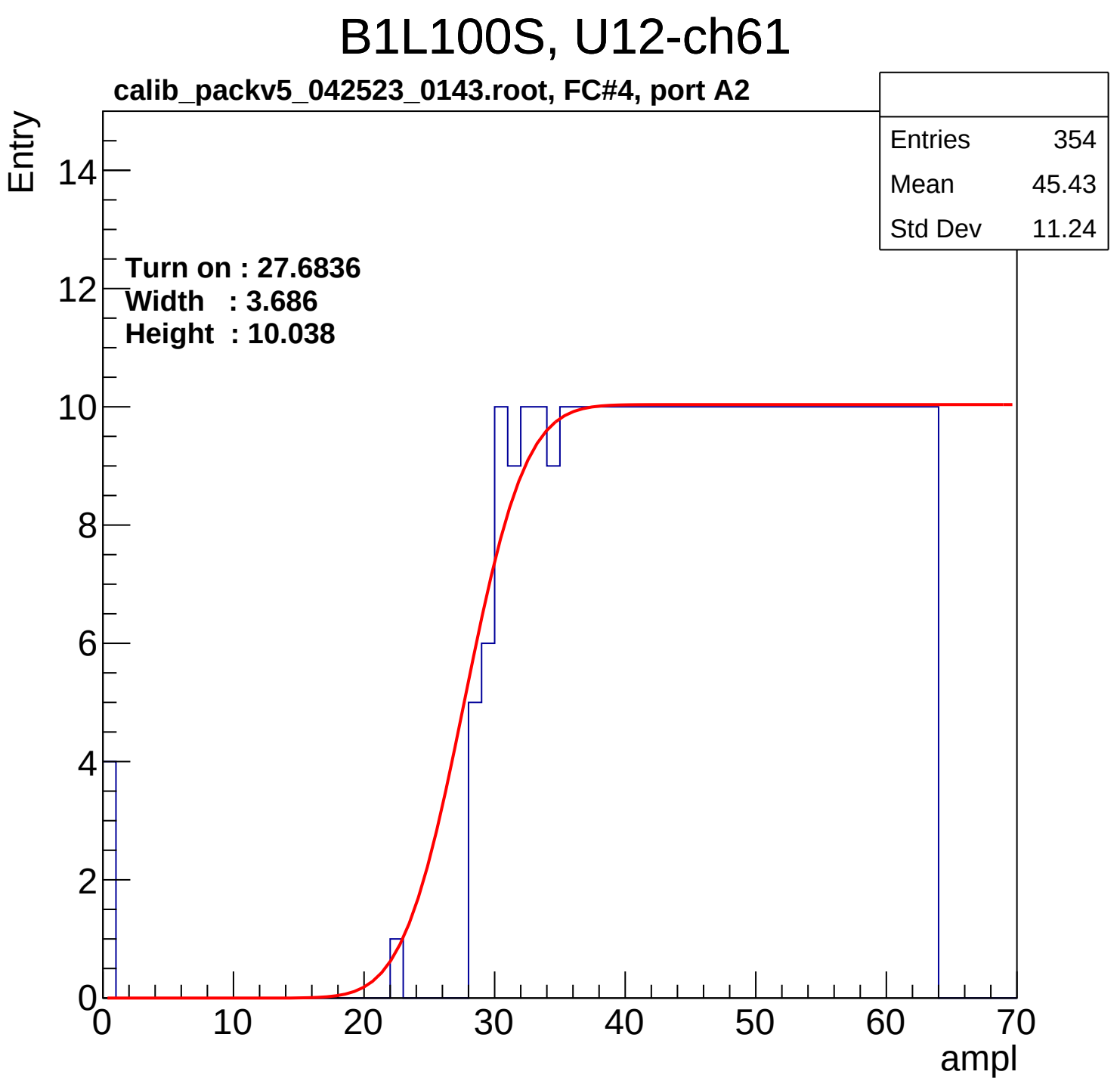

B1L100S, U12-ch56
calib_packv5_042523_0143.root, FC#4, port A2
Entries 375
Mean 44.42
Std Dev 11.61
Turn on : 26.4630
Width : 4.239
Height : 10.039
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

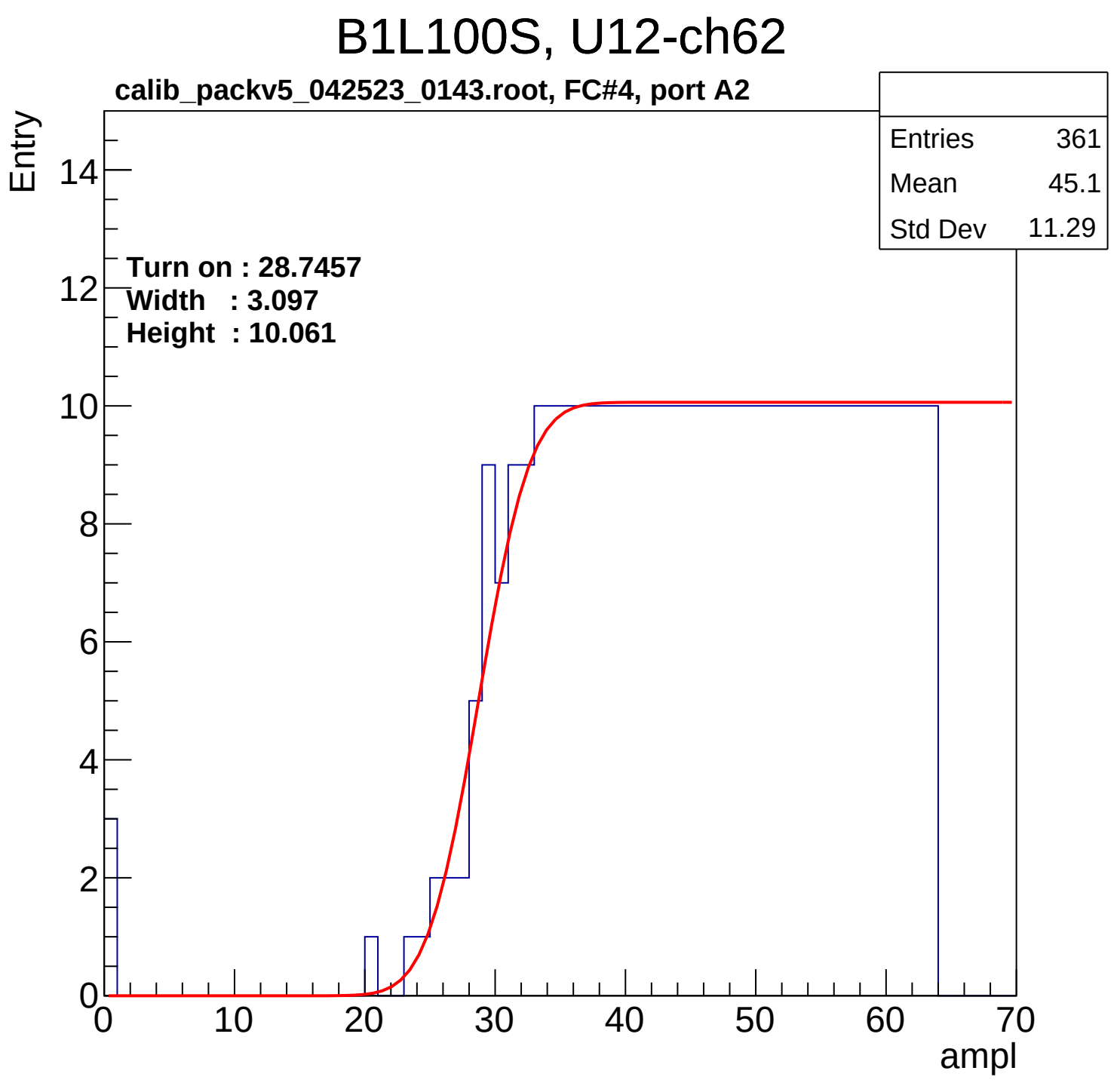

B1L100S, U12-ch57
calib_packv5_042523_0143.root, FC#4, port A2
Entries 365
Mean 44.87
Std Dev 11.42
Turn on : 28.4843
Width : 3.995
Height : 10.082
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

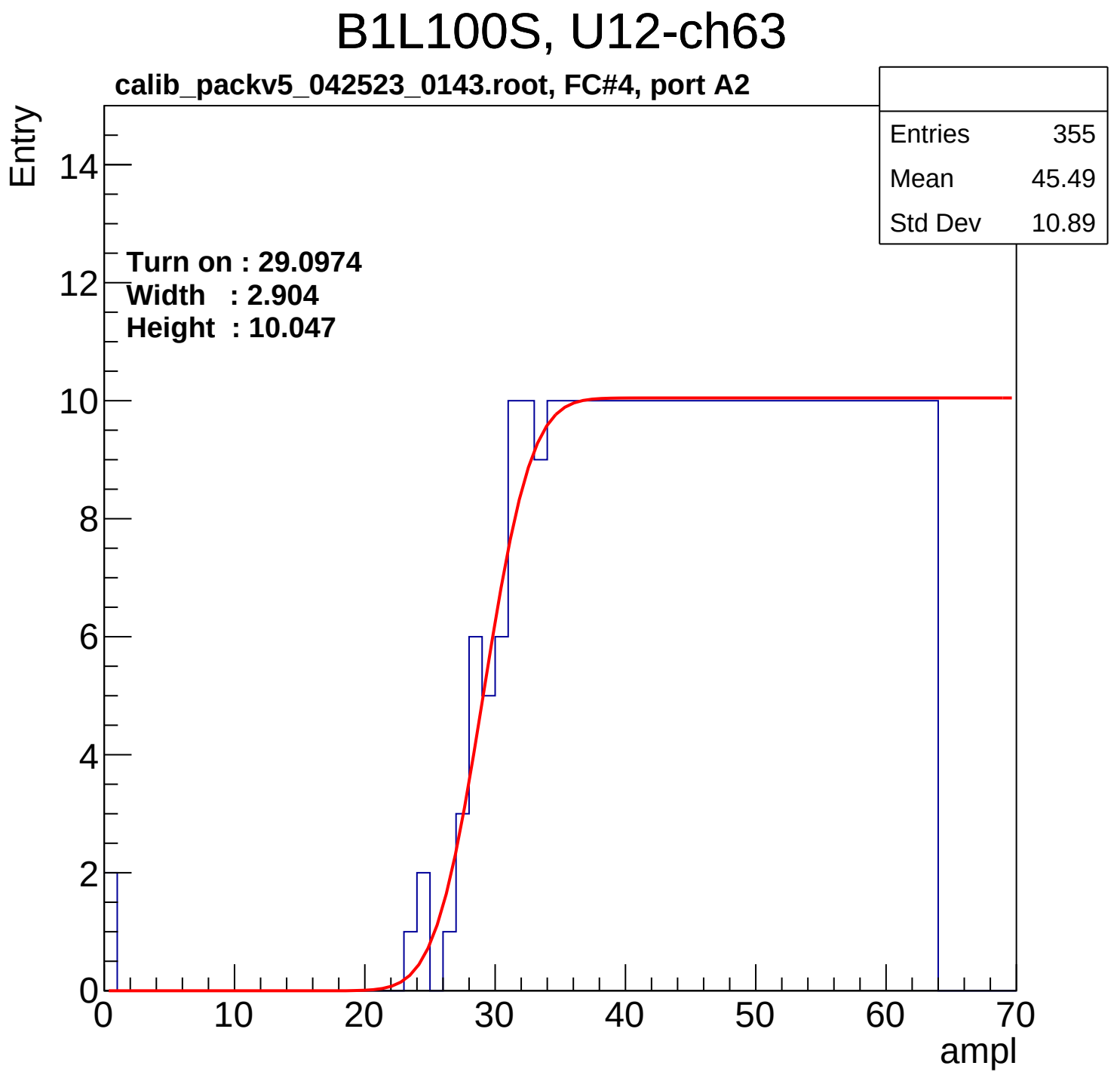

B1L100S, U12-ch58
calib_packv5_042523_0143.root, FC#4, port A2
Entries 380
Mean 44.27
Std Dev 11.5
Turn on : 26.2038
Width : 3.405
Height : 10.032
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

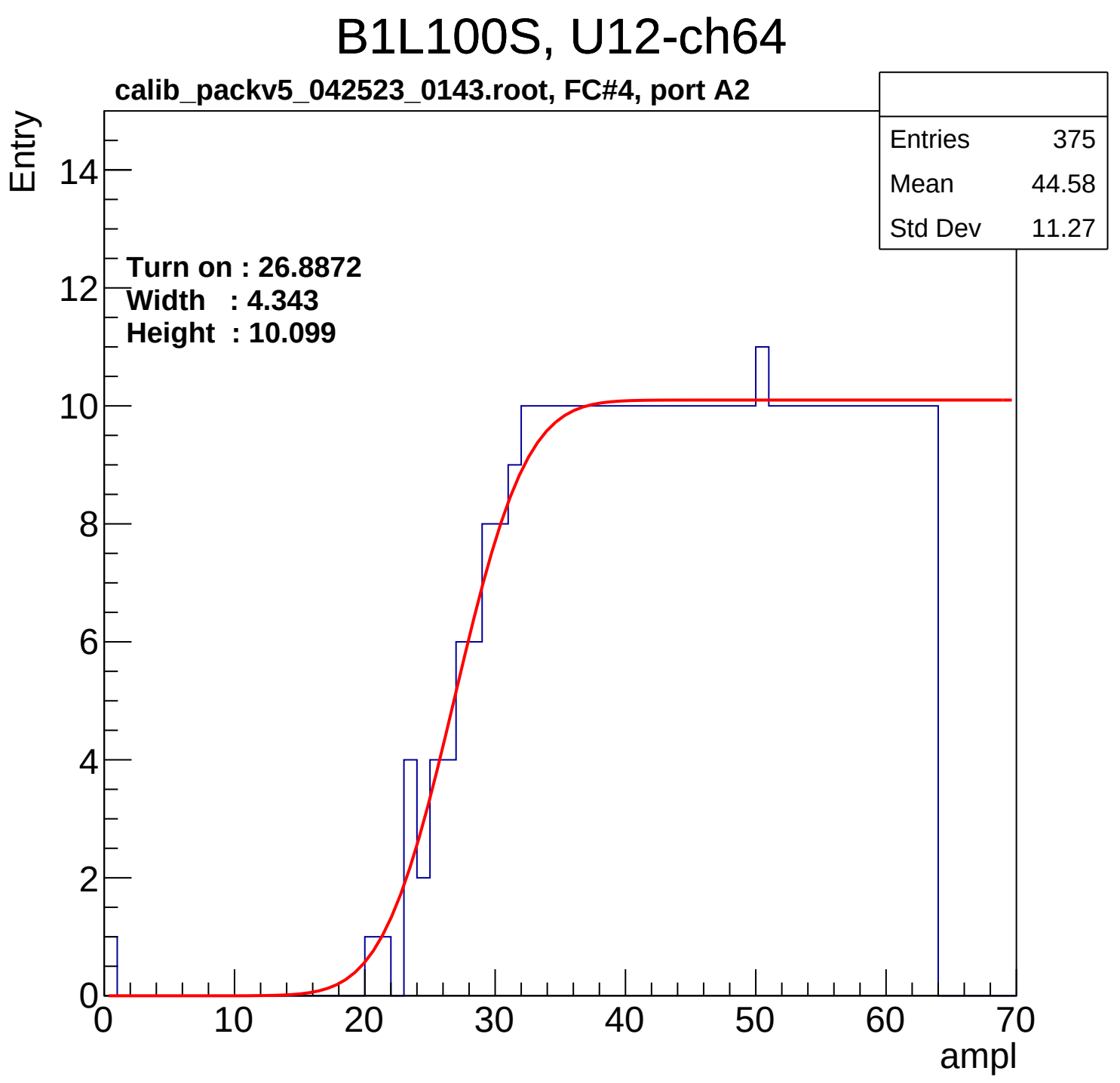

B1L100S, U12-ch59
calib_packv5_042523_0143.root, FC#4, port A2
Entries 367
Mean 44.8
Std Dev 11.52
Turn on : 27.7739
Width : 2.270
Height : 10.012
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

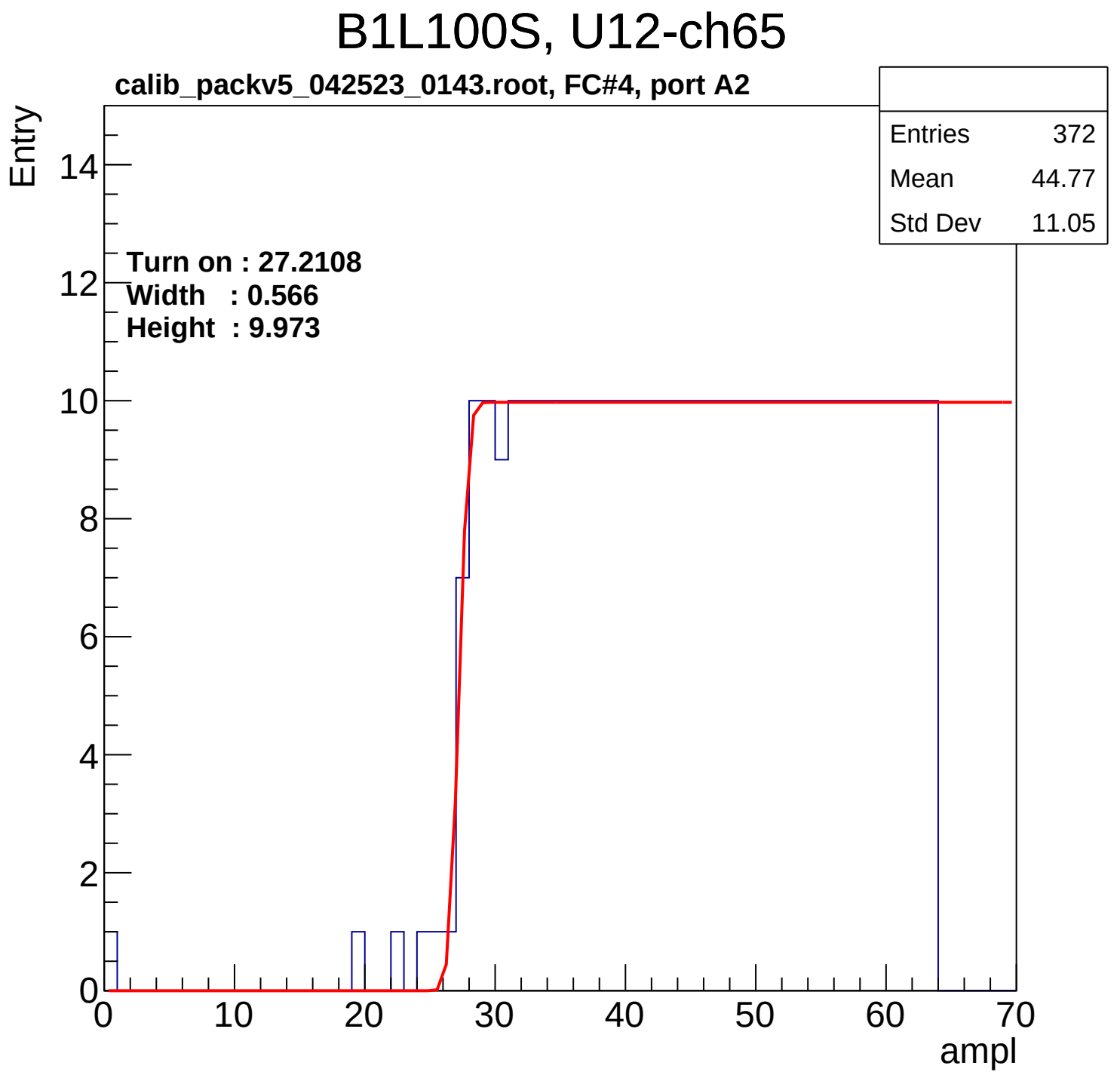

B1L100S, U12-ch60
calib_packv5_042523_0143.root, FC#4, port A2
Entries 383
Mean 44.07
Std Dev 11.73
Turn on : 26.1247
Width : 1.894
Height : 9.947
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

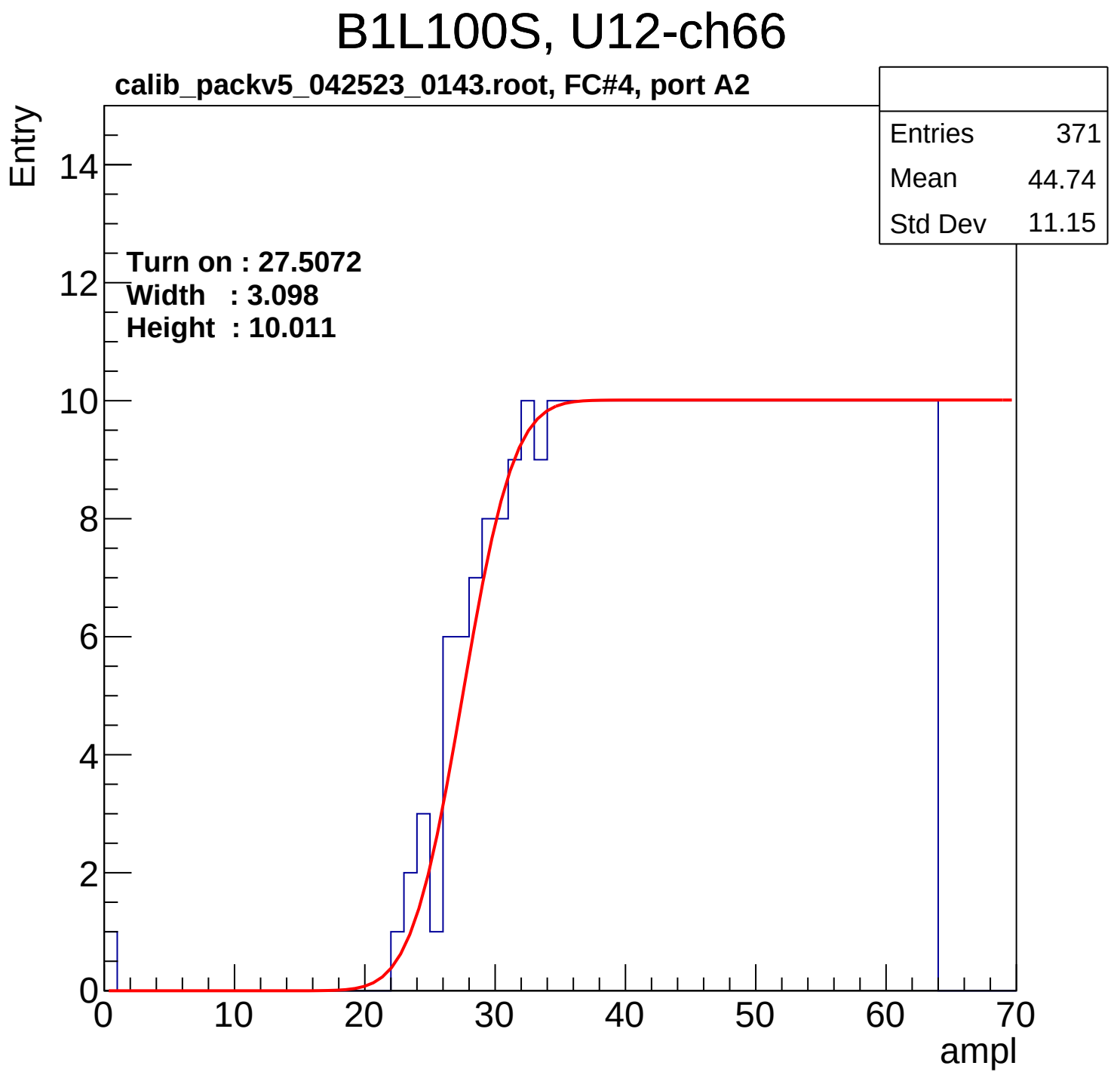

B1L100S, U12-ch61
calib_packv5_042523_0143.root, FC#4, port A2
Entries 354
Mean 45.43
Std Dev 11.24
Turn on : 27.6836
Width : 3.686
Height : 10.038
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

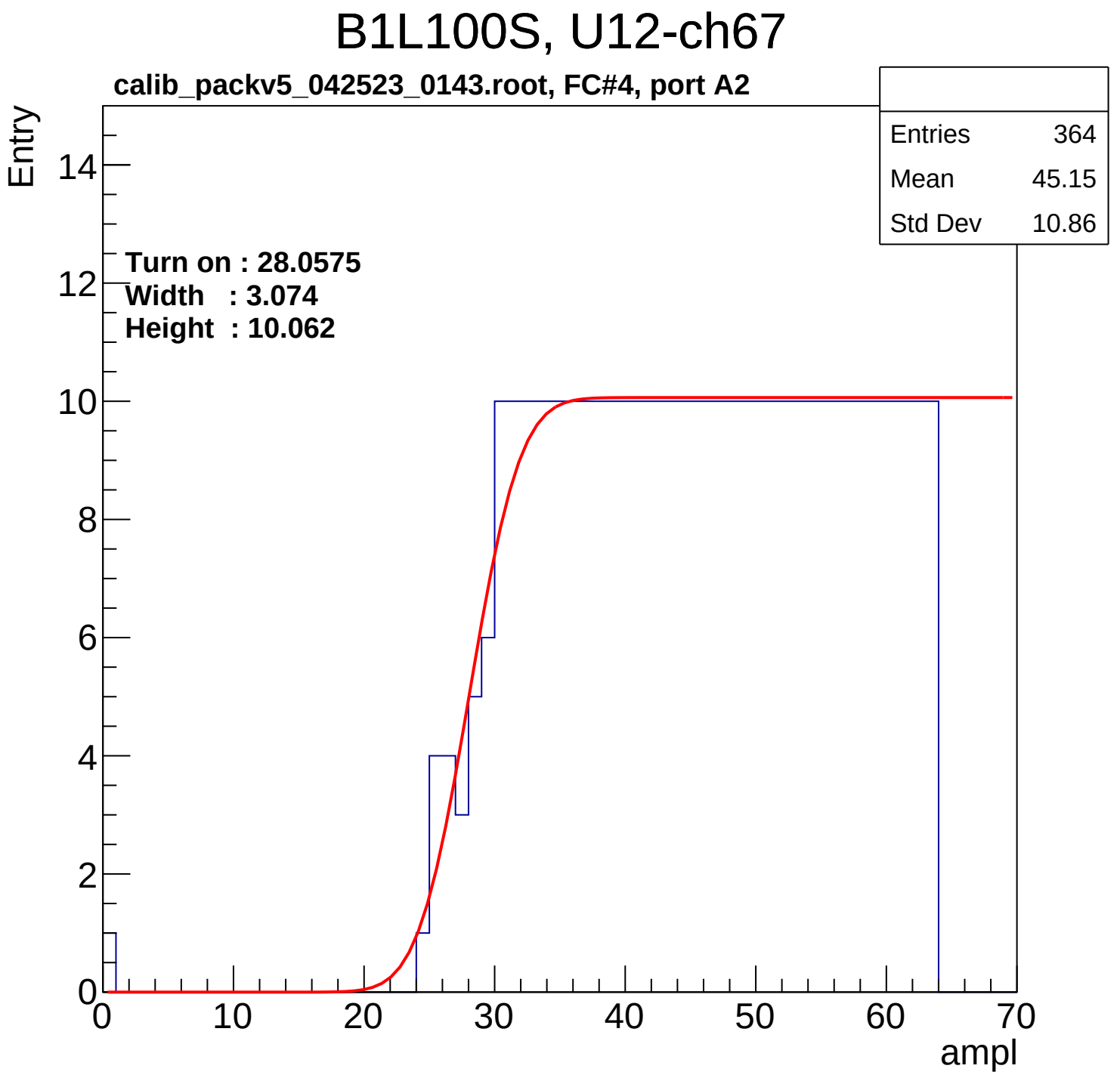

B1L100S, U12-ch62
calib_packv5_042523_0143.root, FC#4, port A2
Entries 361
Mean 45.1
Std Dev 11.29
Turn on : 28.7457
Width : 3.097
Height : 10.061
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

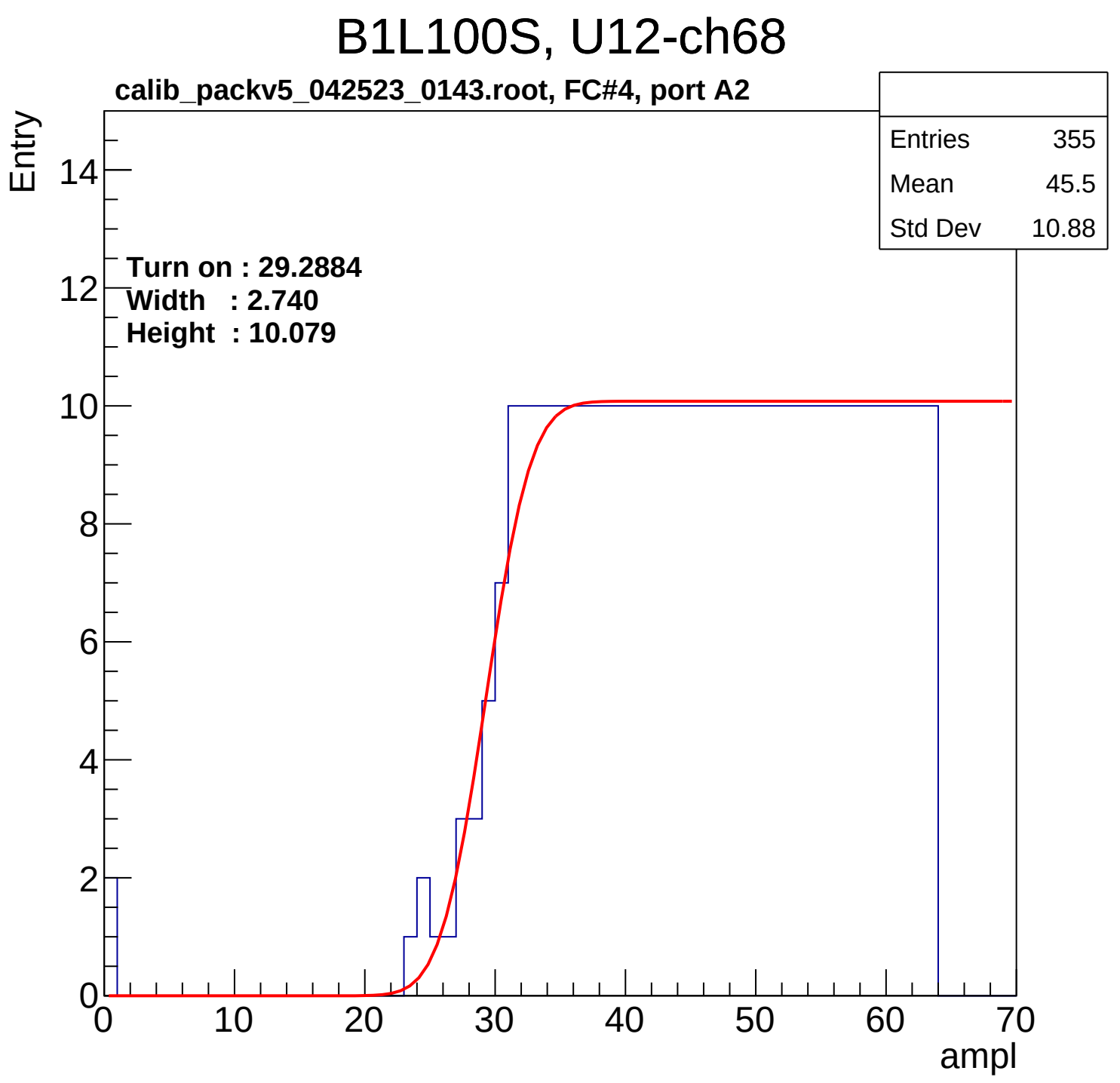

B1L100S, U12-ch63
calib_packv5_042523_0143.root, FC#4, port A2
Entries 355
Mean 45.49
Std Dev 10.89
Turn on : 29.0974
Width : 2.904
Height : 10.047
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

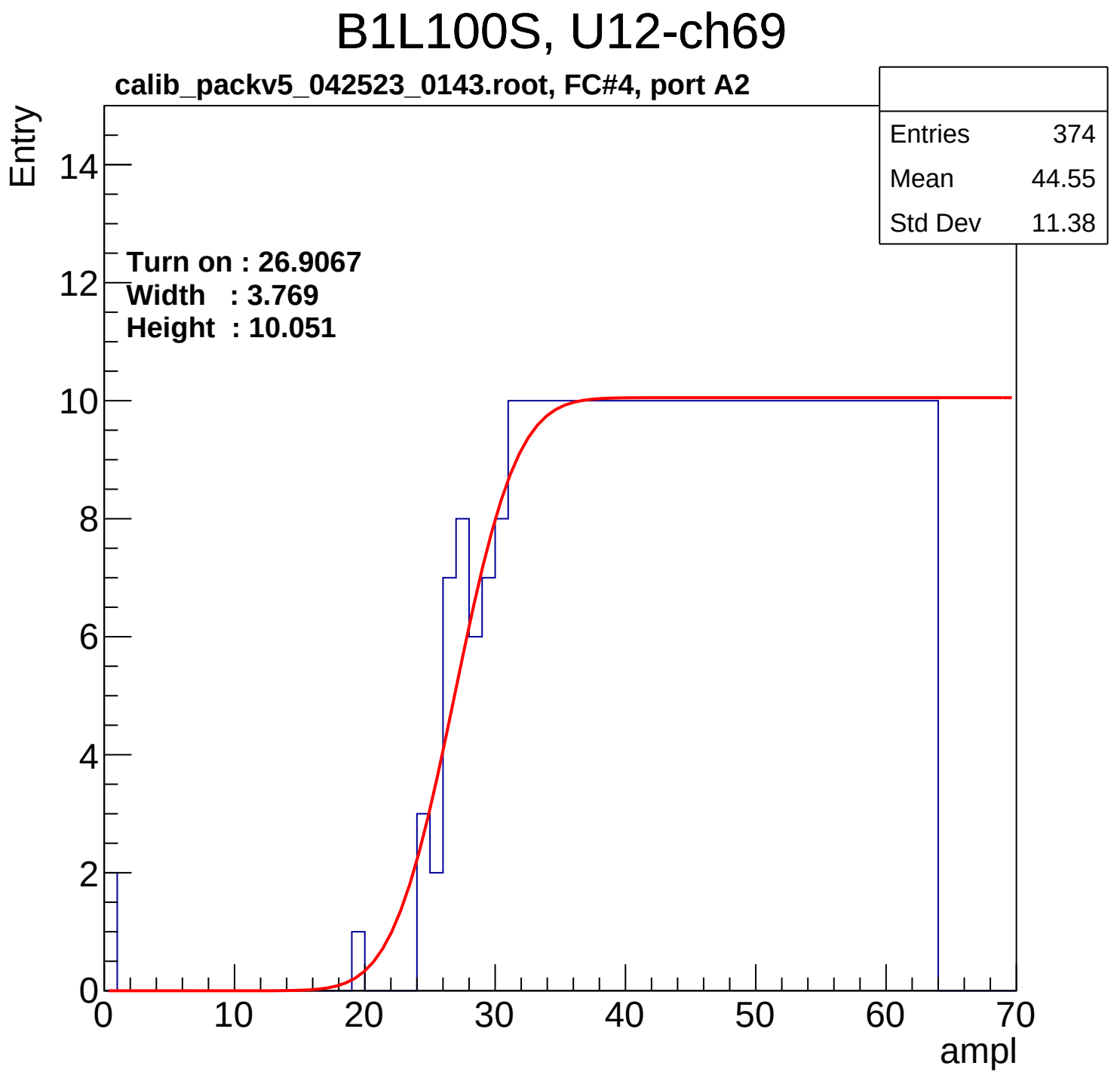

B1L100S, U12-ch64
calib_packv5_042523_0143.root, FC#4, port A2
Entries 375
Mean 44.58
Std Dev 11.27
Turn on : 26.8872
Width : 4.343
Height : 10.099
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

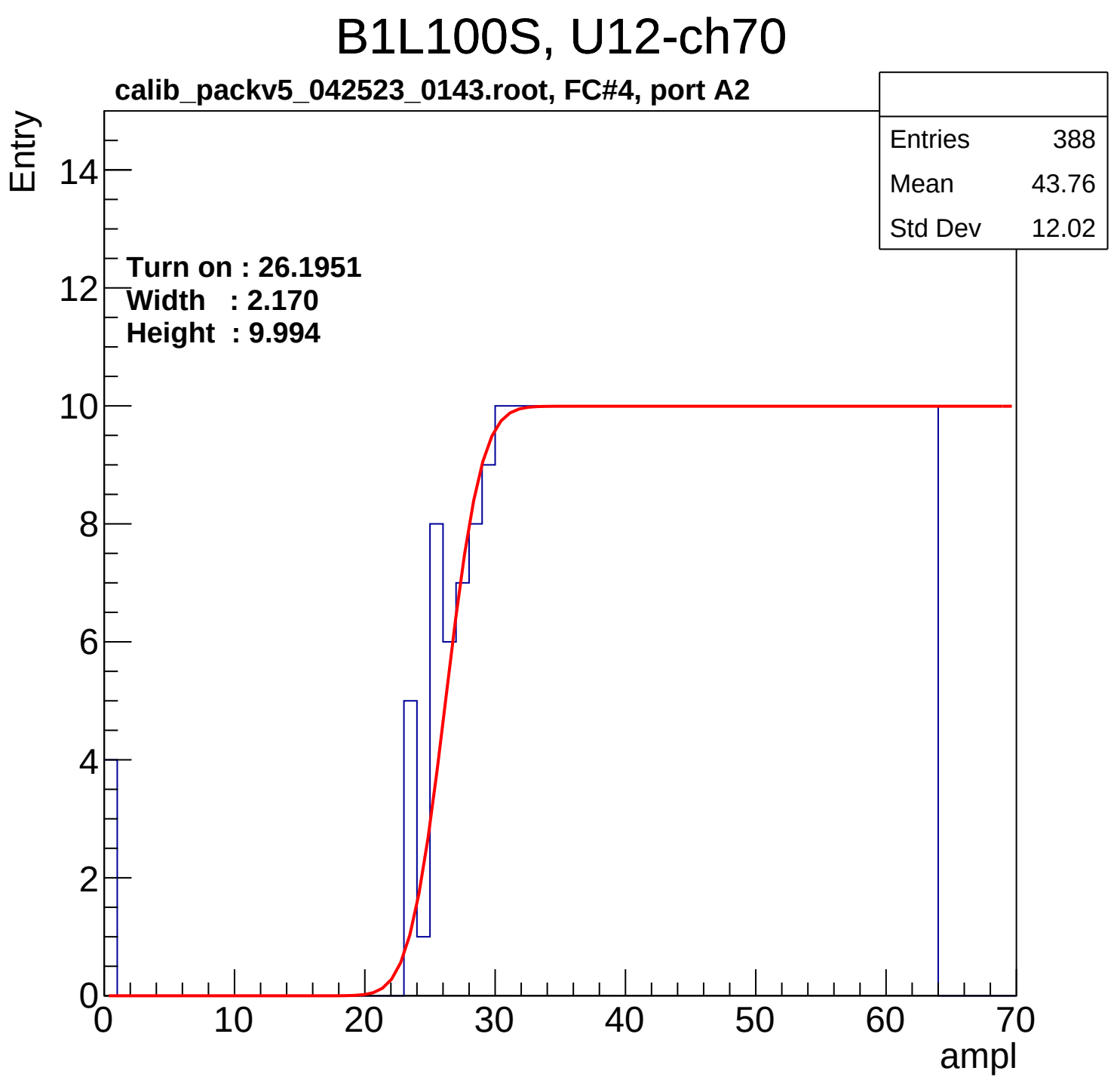

B1L100S, U12-ch65
calib_packv5_042523_0143.root, FC#4, port A2
Entries 372
Mean 44.77
Std Dev 11.05
Turn on : 27.2108
Width : 0.566
Height : 9.973
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

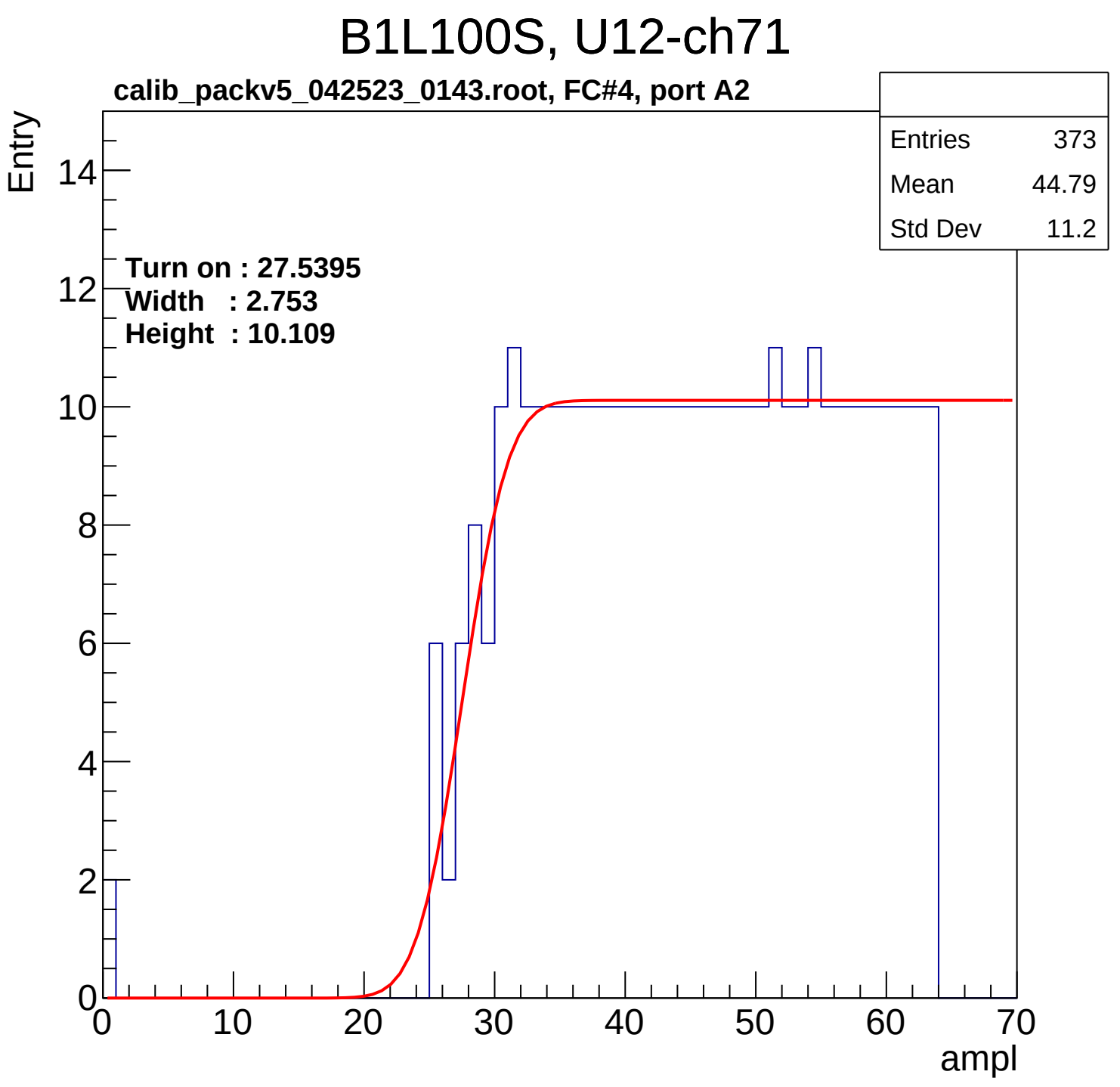

B1L100S, U12-ch66
calib_packv5_042523_0143.root, FC#4, port A2
Entries 371
Mean 44.74
Std Dev 11.15
Turn on : 27.5072
Width : 3.098
Height : 10.011
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

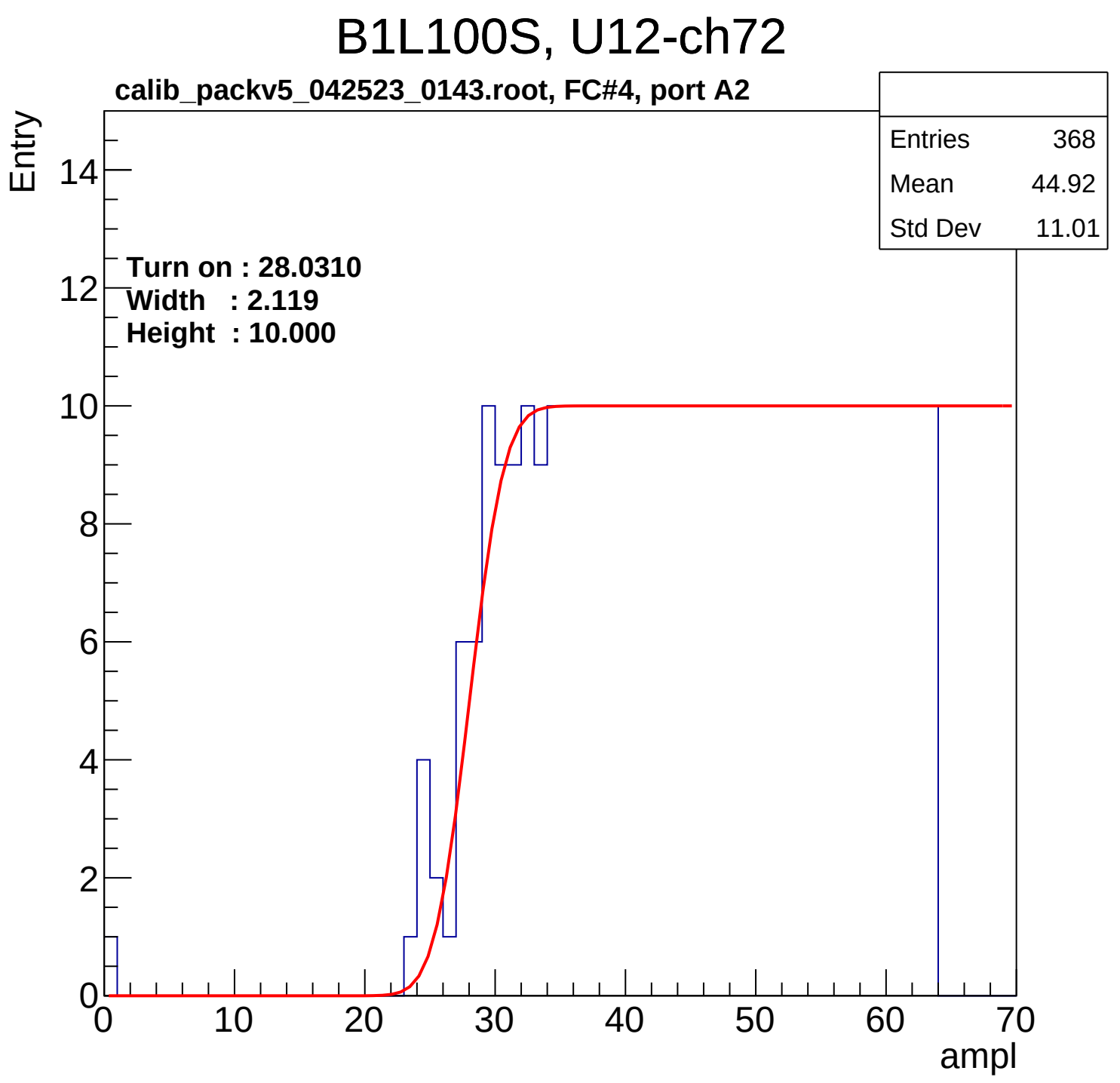

B1L100S, U12-ch67
calib_packv5_042523_0143.root, FC#4, port A2
Entries 364
Mean 45.15
Std Dev 10.86
Turn on : 28.0575
Width : 3.074
Height : 10.062
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

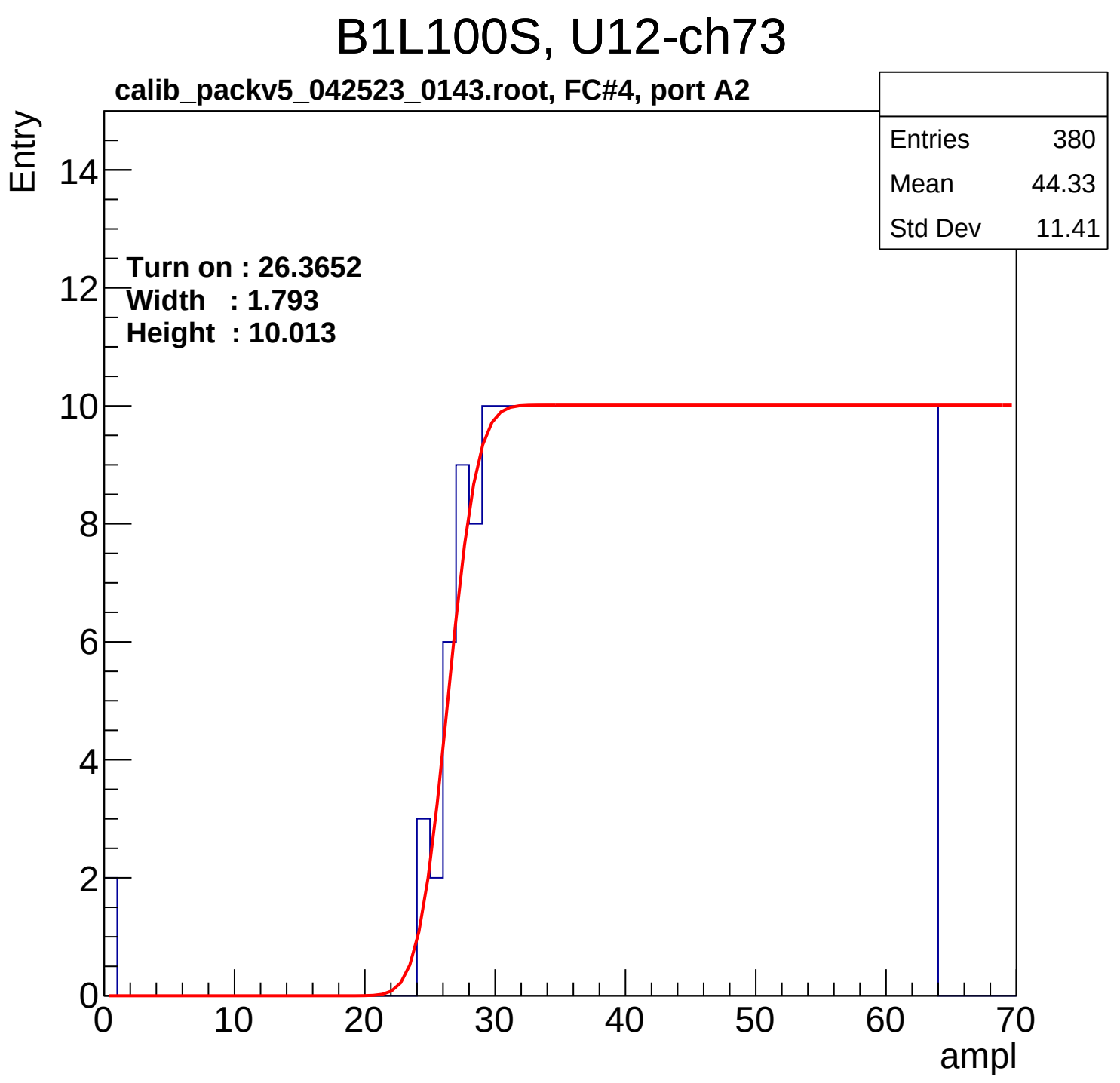

B1L100S, U12-ch68
calib_packv5_042523_0143.root, FC#4, port A2
Entries 355
Mean 45.5
Std Dev 10.88
Turn on : 29.2884
Width : 2.740
Height : 10.079
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

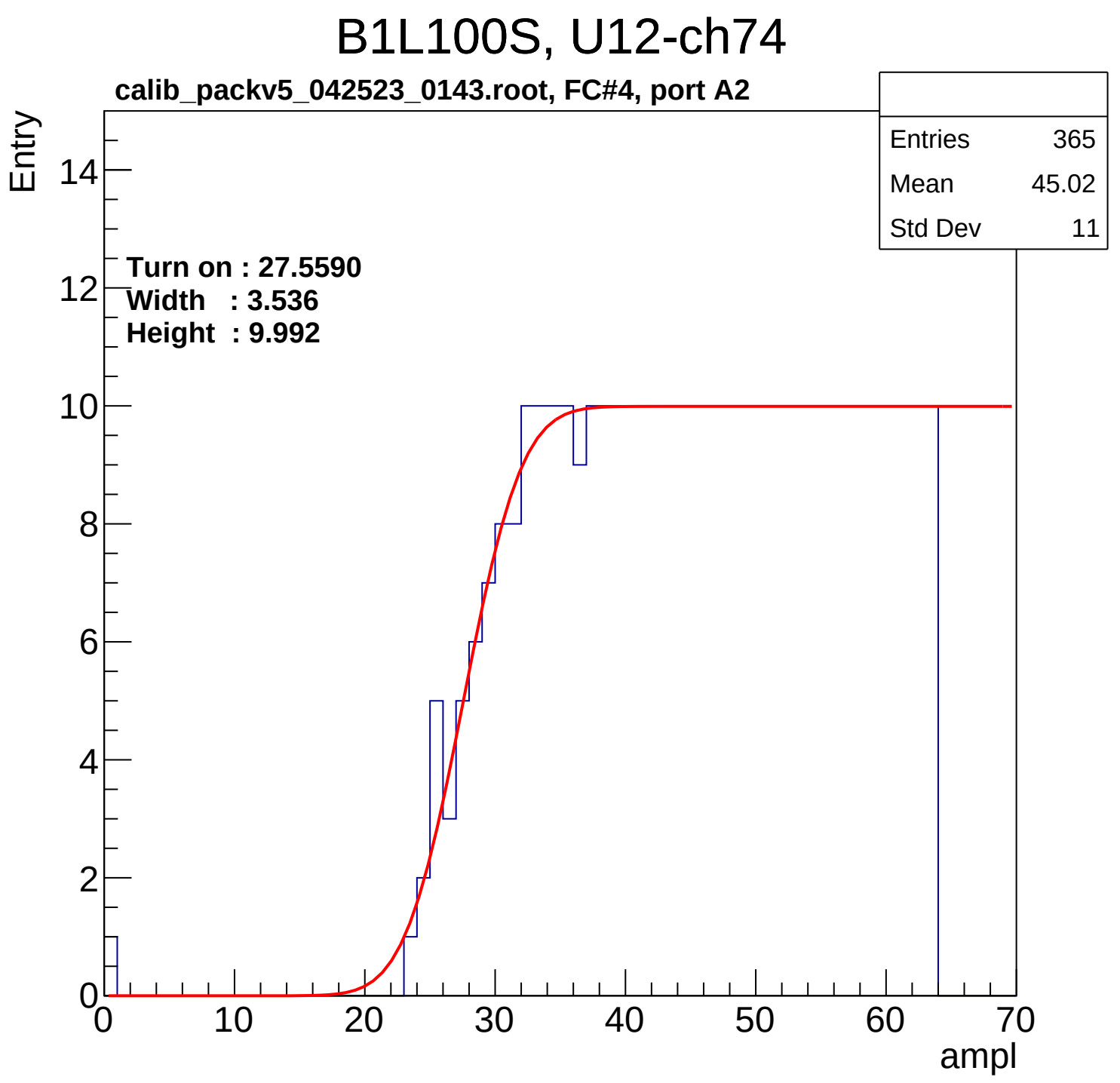

B1L100S, U12-ch69
calib_packv5_042523_0143.root, FC#4, port A2
Entries 374
Mean 44.55
Std Dev 11.38
Turn on : 26.9067
Width : 3.769
Height : 10.051
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

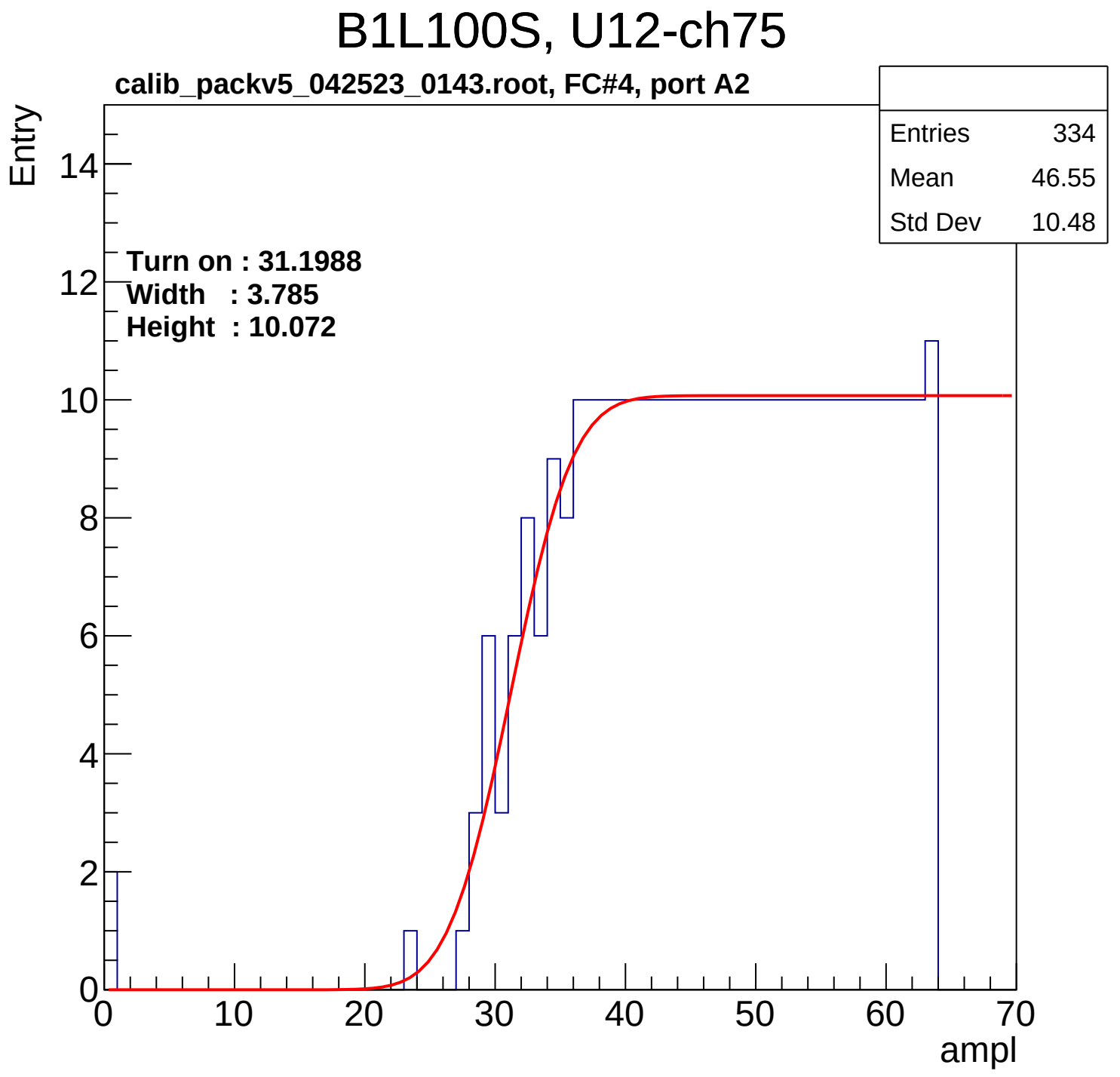

B1L100S, U12-ch70
calib_packv5_042523_0143.root, FC#4, port A2
Entries 388
Mean 43.76
Std Dev 12.02
Turn on : 26.1951
Width : 2.170
Height : 9.994
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

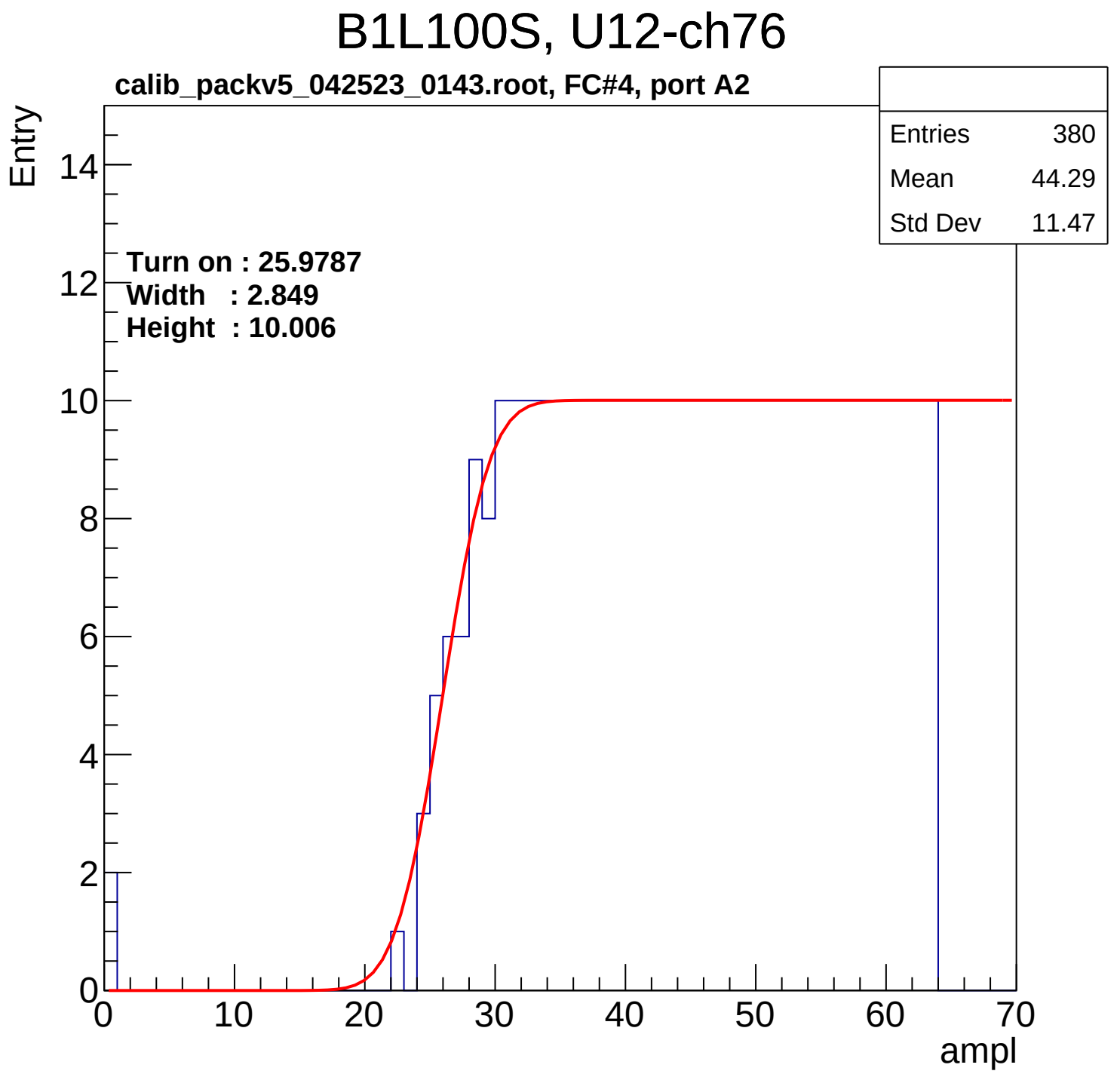

B1L100S, U12-ch71
calib_packv5_042523_0143.root, FC#4, port A2
Entries 373
Mean 44.79
Std Dev 11.2
Turn on : 27.5395
Width : 2.753
Height : 10.109
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

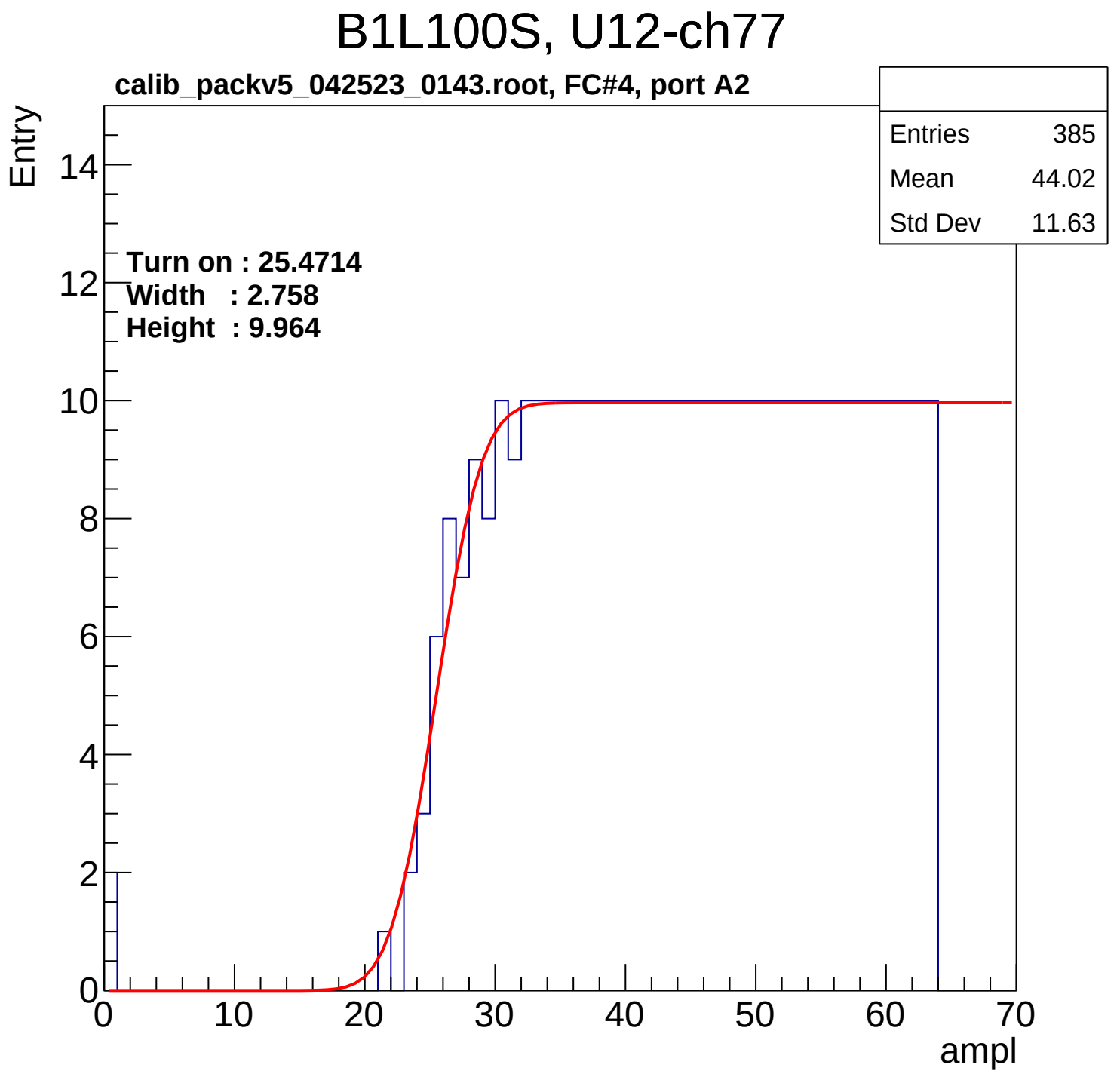

B1L100S, U12-ch72
calib_packv5_042523_0143.root, FC#4, port A2
Entries 368
Mean 44.92
Std Dev 11.01
Turn on : 28.0310
Width : 2.119
Height : 10.000
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

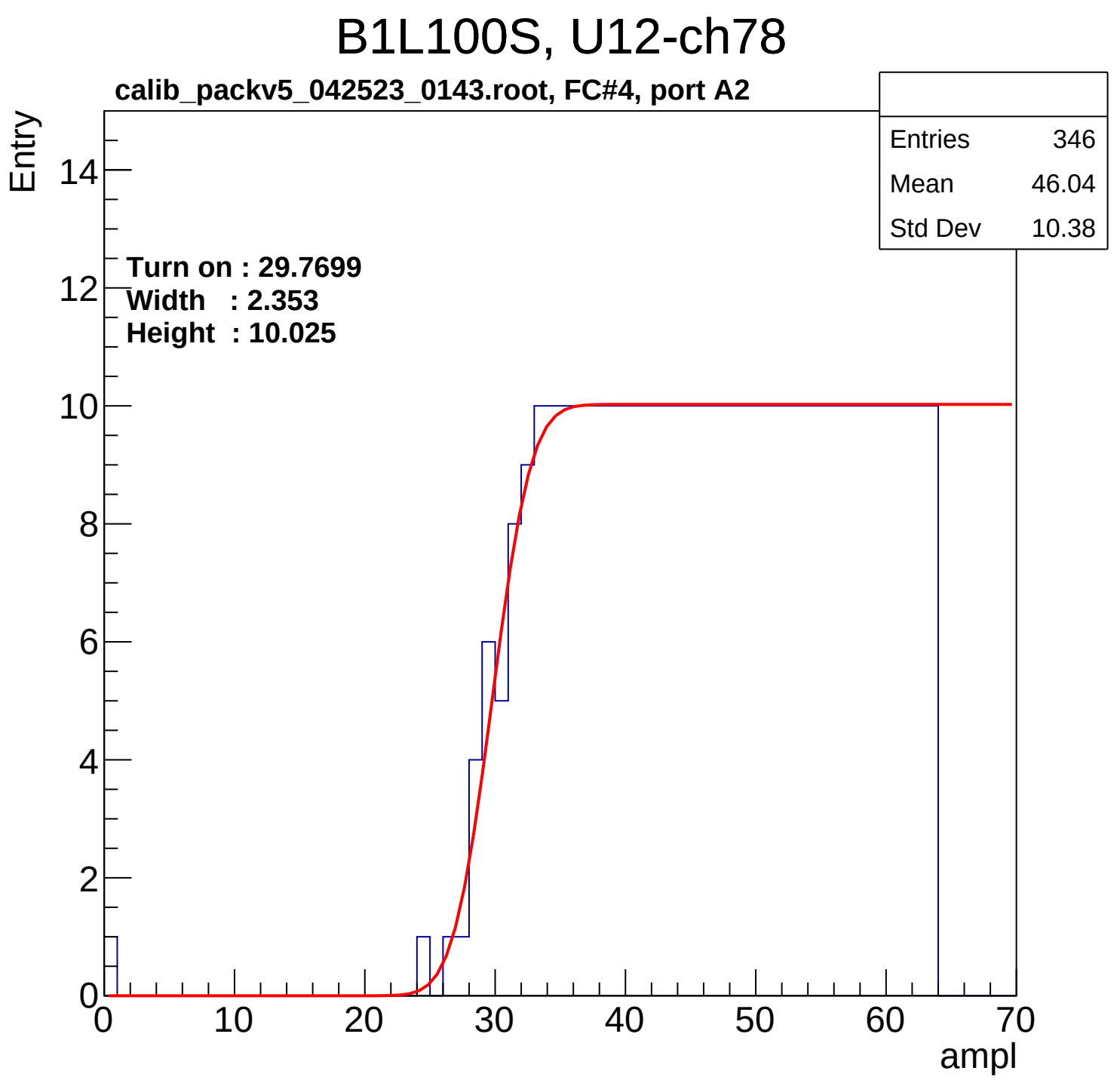

B1L100S, U12-ch73
calib_packv5_042523_0143.root, FC#4, port A2
Entries 380
Mean 44.33
Std Dev 11.41
Turn on : 26.3652
Width : 1.793
Height : 10.013
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

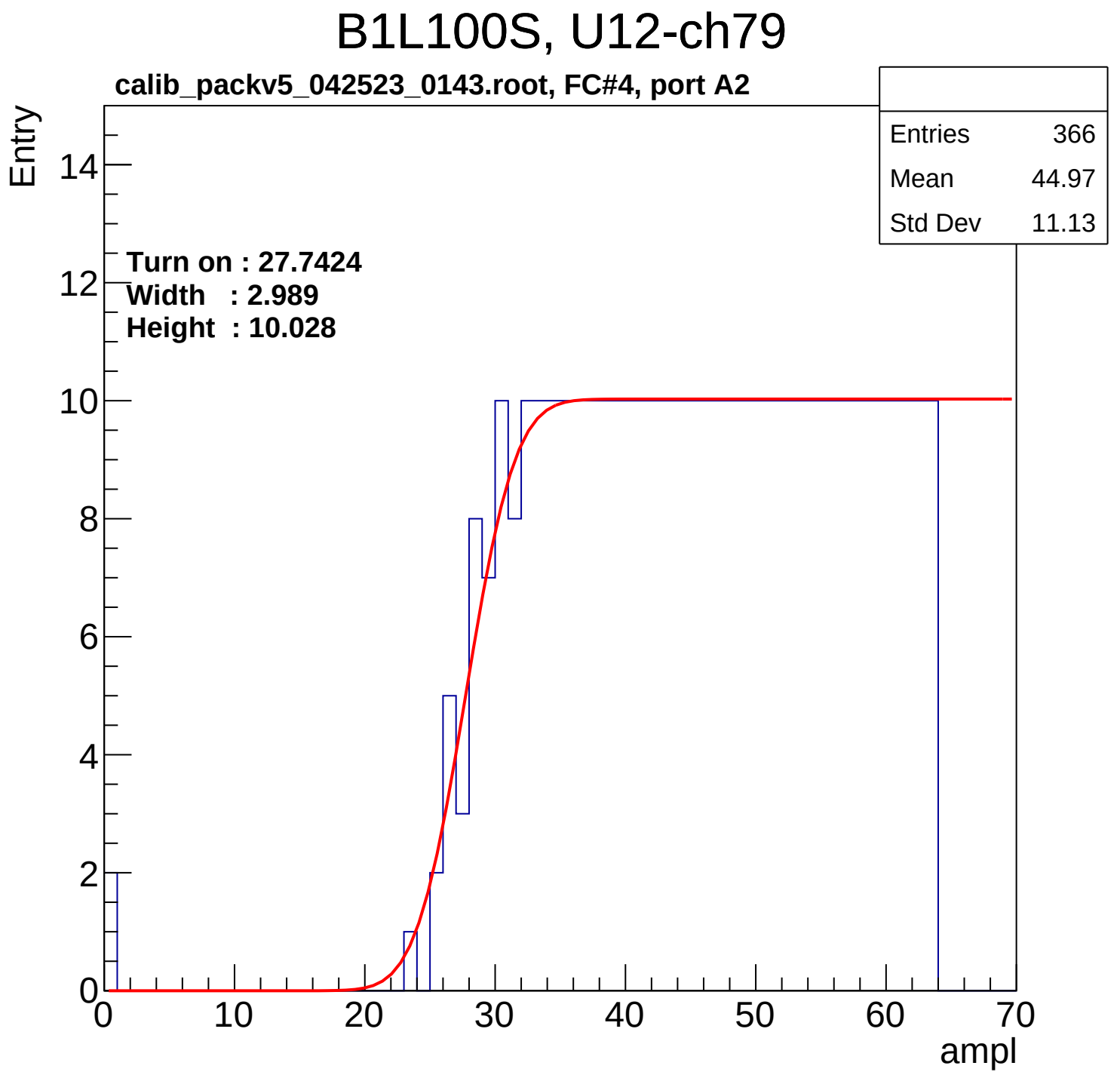

B1L100S, U12-ch74
calib_packv5_042523_0143.root, FC#4, port A2
Entries 365
Mean 45.02
Std Dev 11
Turn on : 27.5590
Width : 3.536
Height : 9.992
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

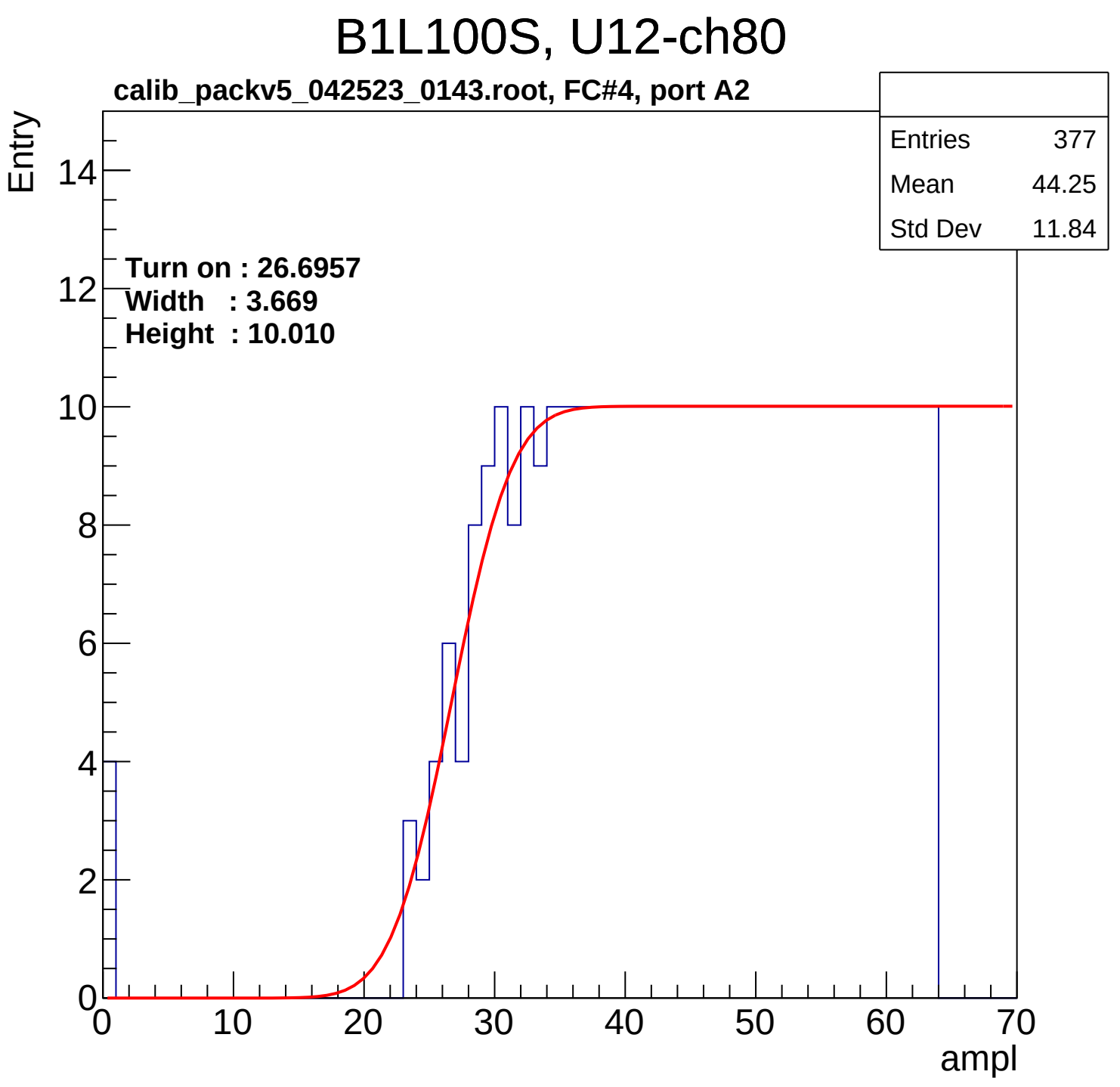

B1L100S, U12-ch75
calib_packv5_042523_0143.root, FC#4, port A2
Entries 334
Mean 46.55
Std Dev 10.48
Turn on : 31.1988
Width : 3.785
Height : 10.072
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

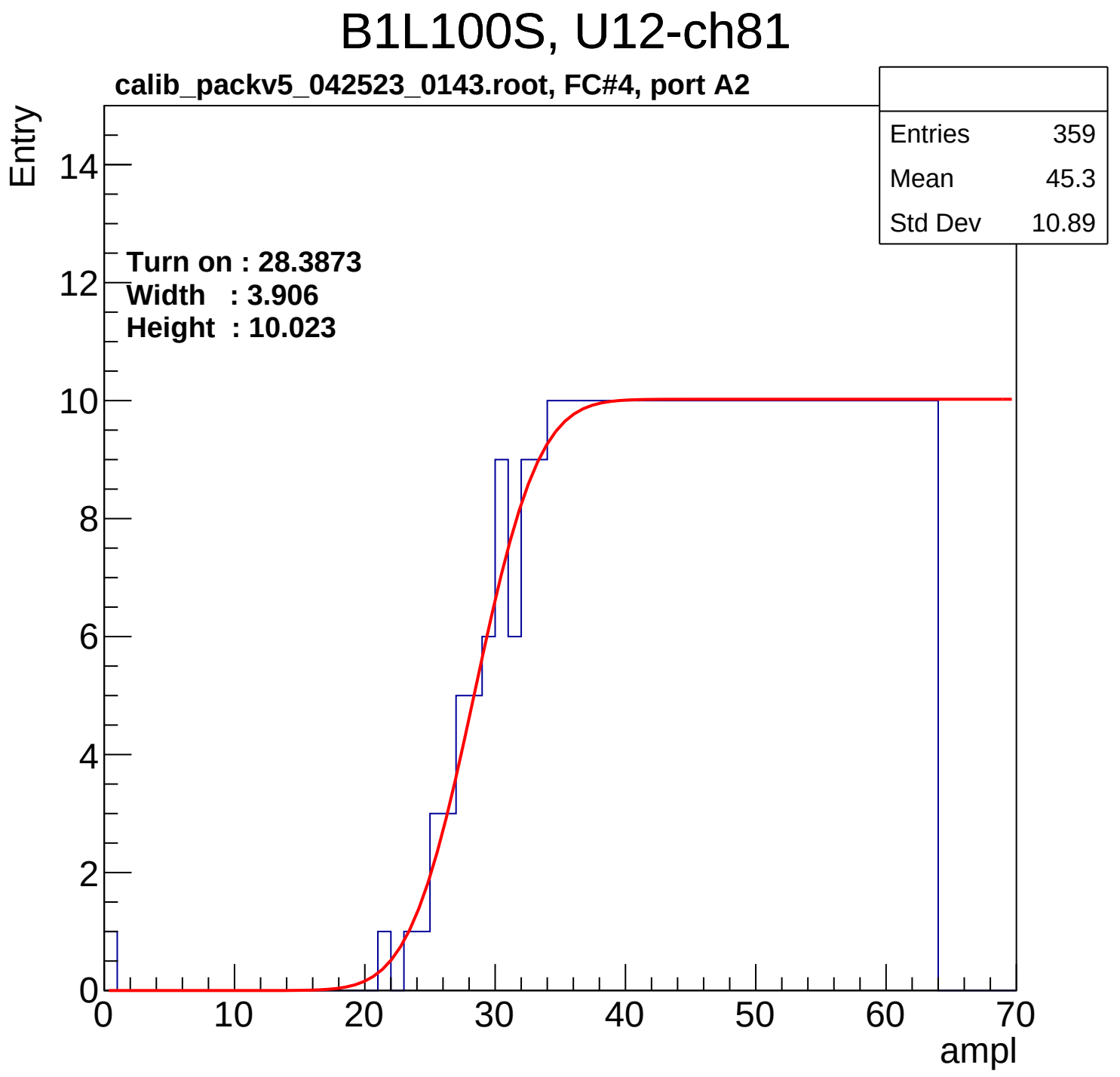

B1L100S, U12-ch76
calib_packv5_042523_0143.root, FC#4, port A2
Entries 380
Mean 44.29
Std Dev 11.47
Turn on : 25.9787
Width : 2.849
Height : 10.006
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

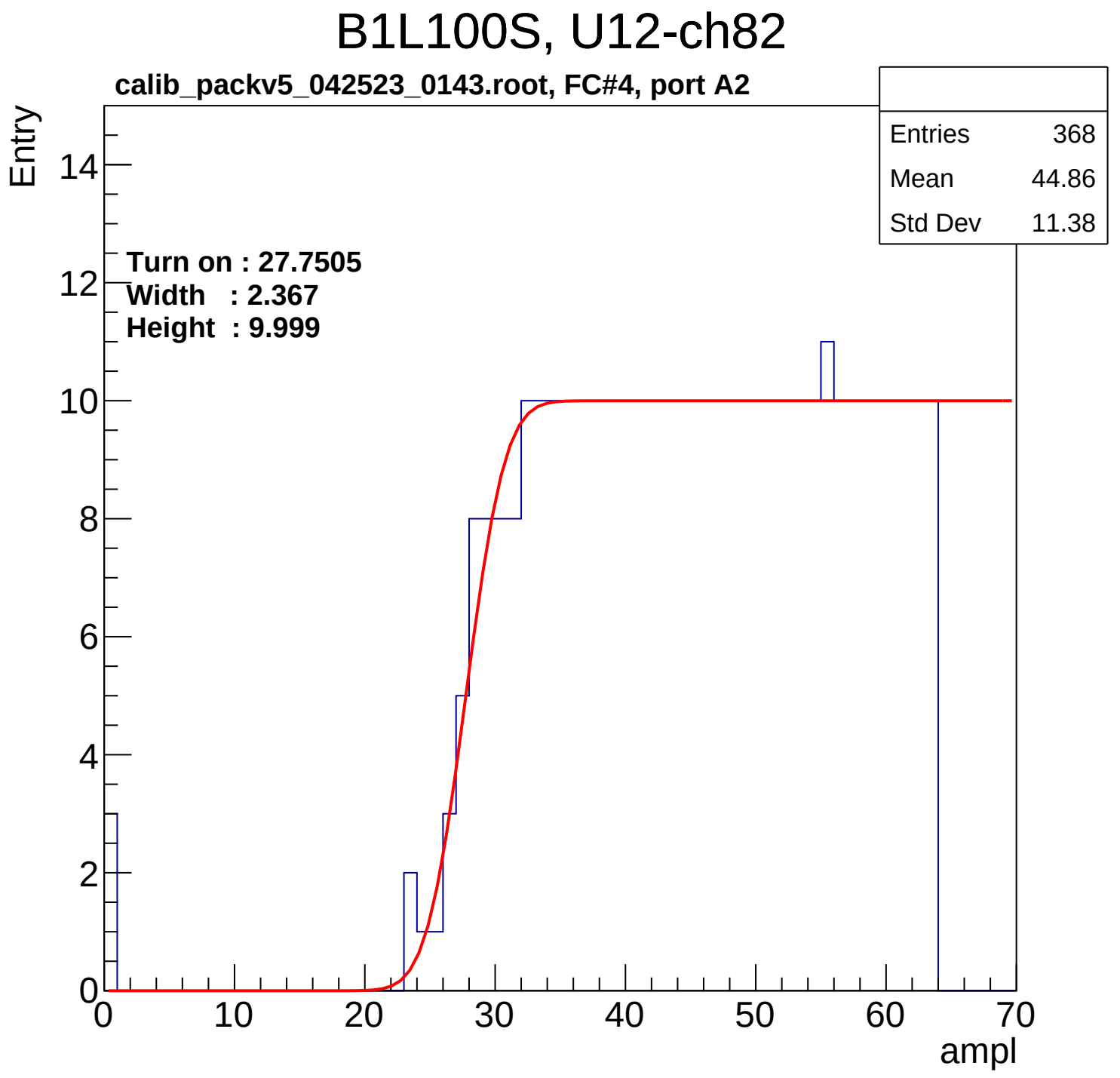

B1L100S, U12-ch77
calib_packv5_042523_0143.root, FC#4, port A2
Entries 385
Mean 44.02
Std Dev 11.63
Turn on : 25.4714
Width : 2.758
Height : 9.964
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

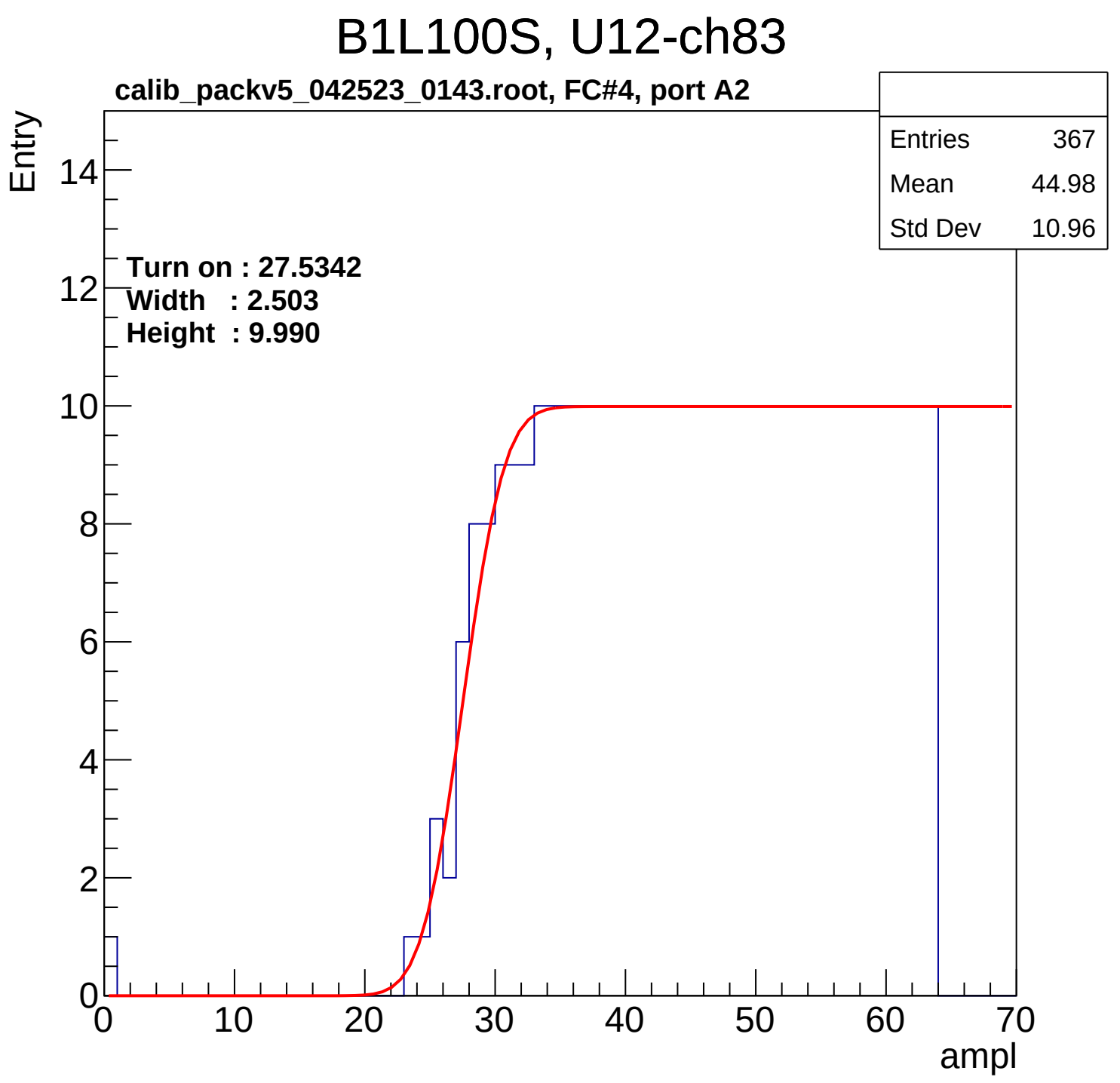

B1L100S, U12-ch78
calib_packv5_042523_0143.root, FC#4, port A2
Entries 346
Mean 46.04
Std Dev 10.38
Turn on : 29.7699
Width : 2.353
Height : 10.025
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

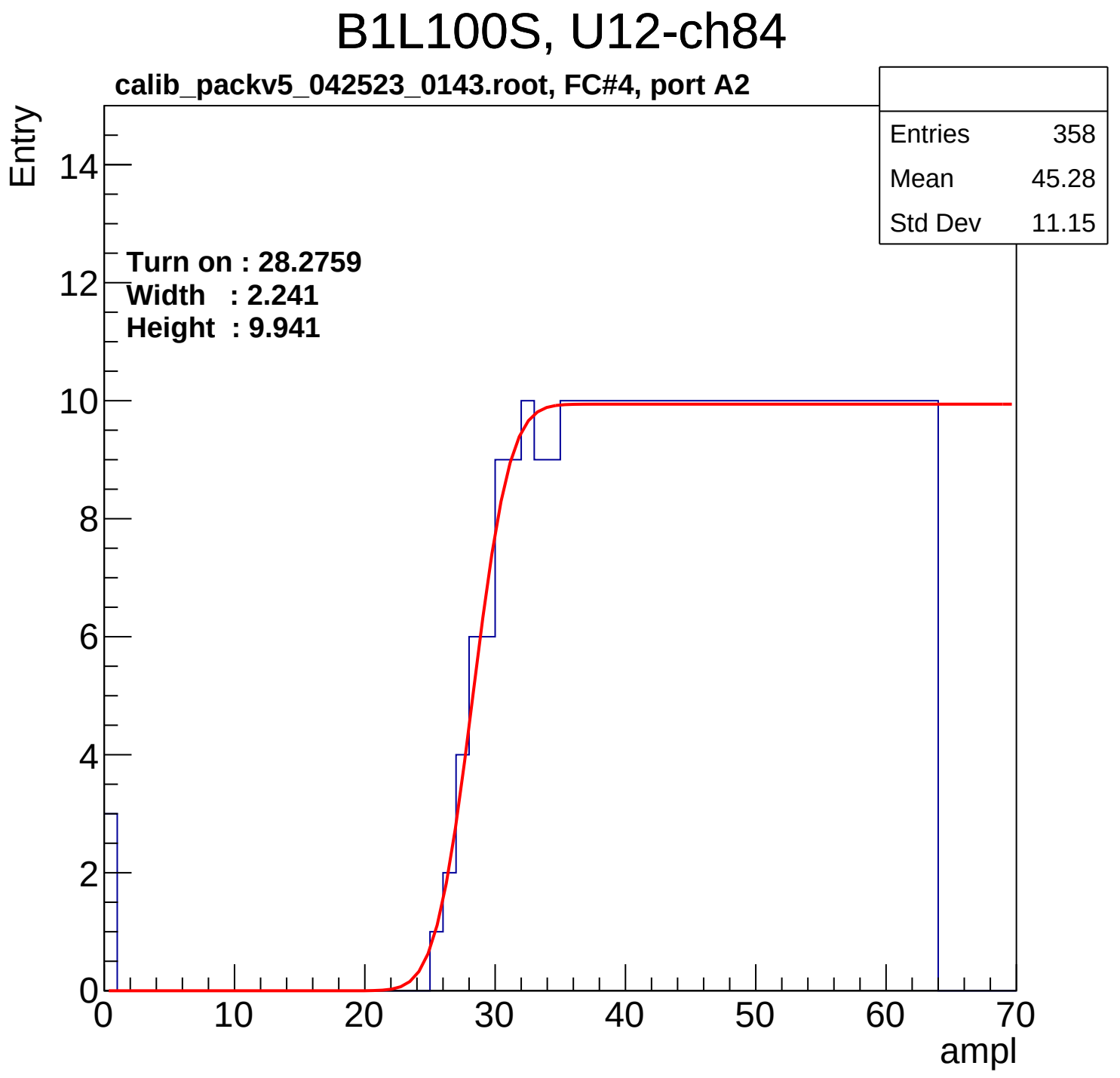

B1L100S, U12-ch79
calib_packv5_042523_0143.root, FC#4, port A2
Entries 366
Mean 44.97
Std Dev 11.13
Turn on : 27.7424
Width : 2.989
Height : 10.028
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

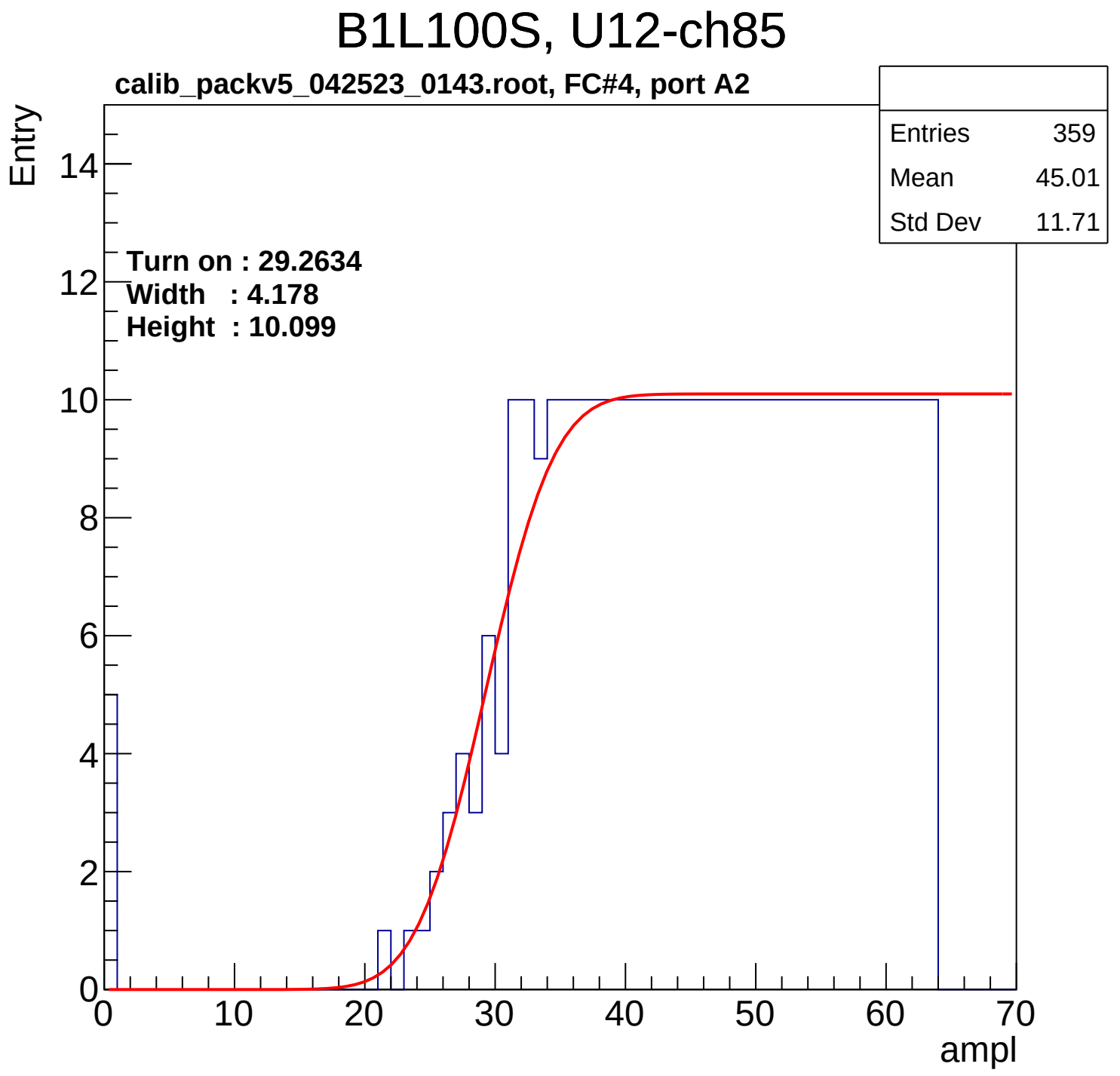

B1L100S, U12-ch80
calib_packv5_042523_0143.root, FC#4, port A2
Entries 377
Mean 44.25
Std Dev 11.84
Turn on : 26.6957
Width : 3.669
Height : 10.010
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

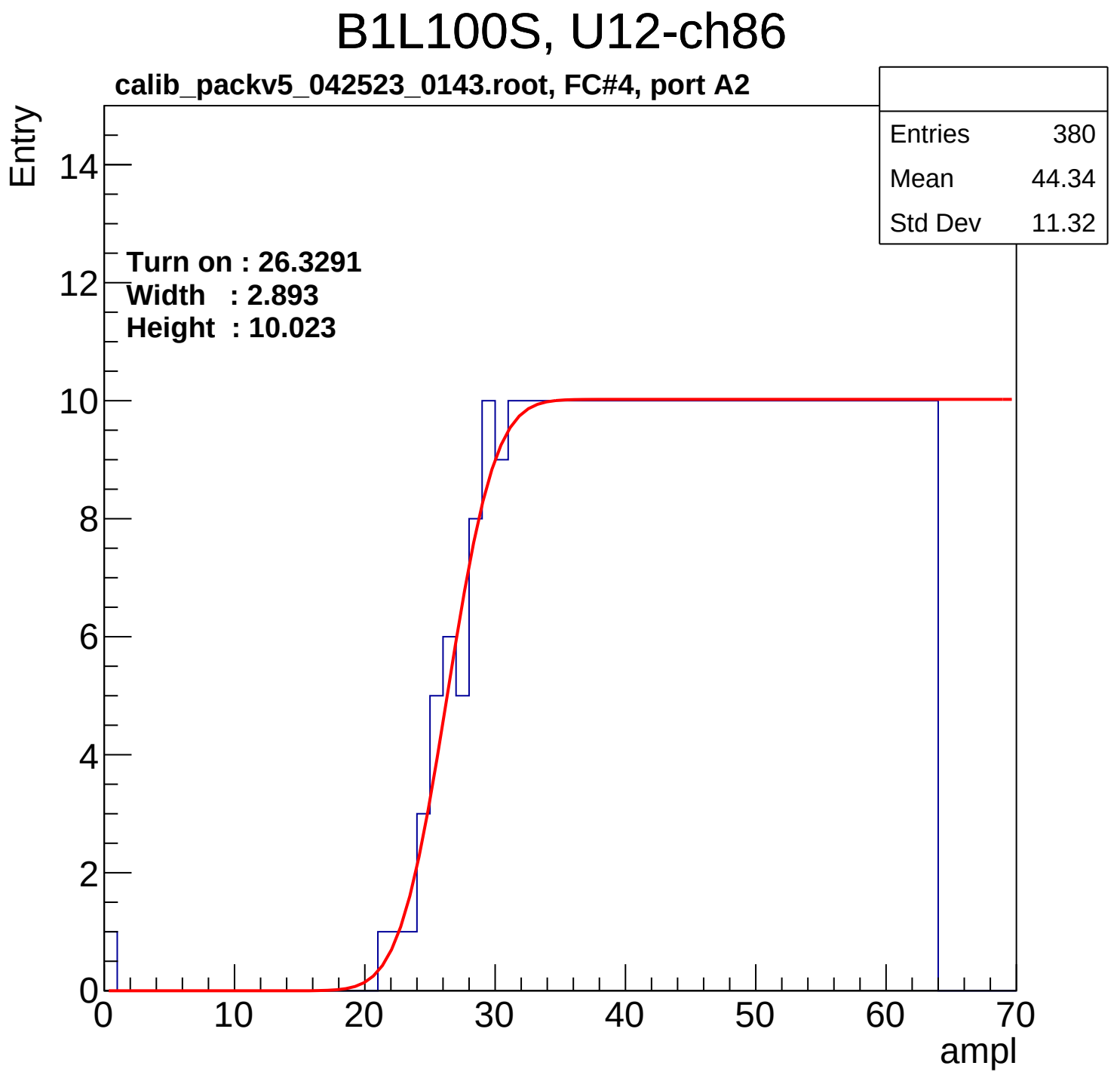

B1L100S, U12-ch81
calib_packv5_042523_0143.root, FC#4, port A2
Entries 359
Mean 45.3
Std Dev 10.89
Turn on : 28.3873
Width : 3.906
Height : 10.023
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

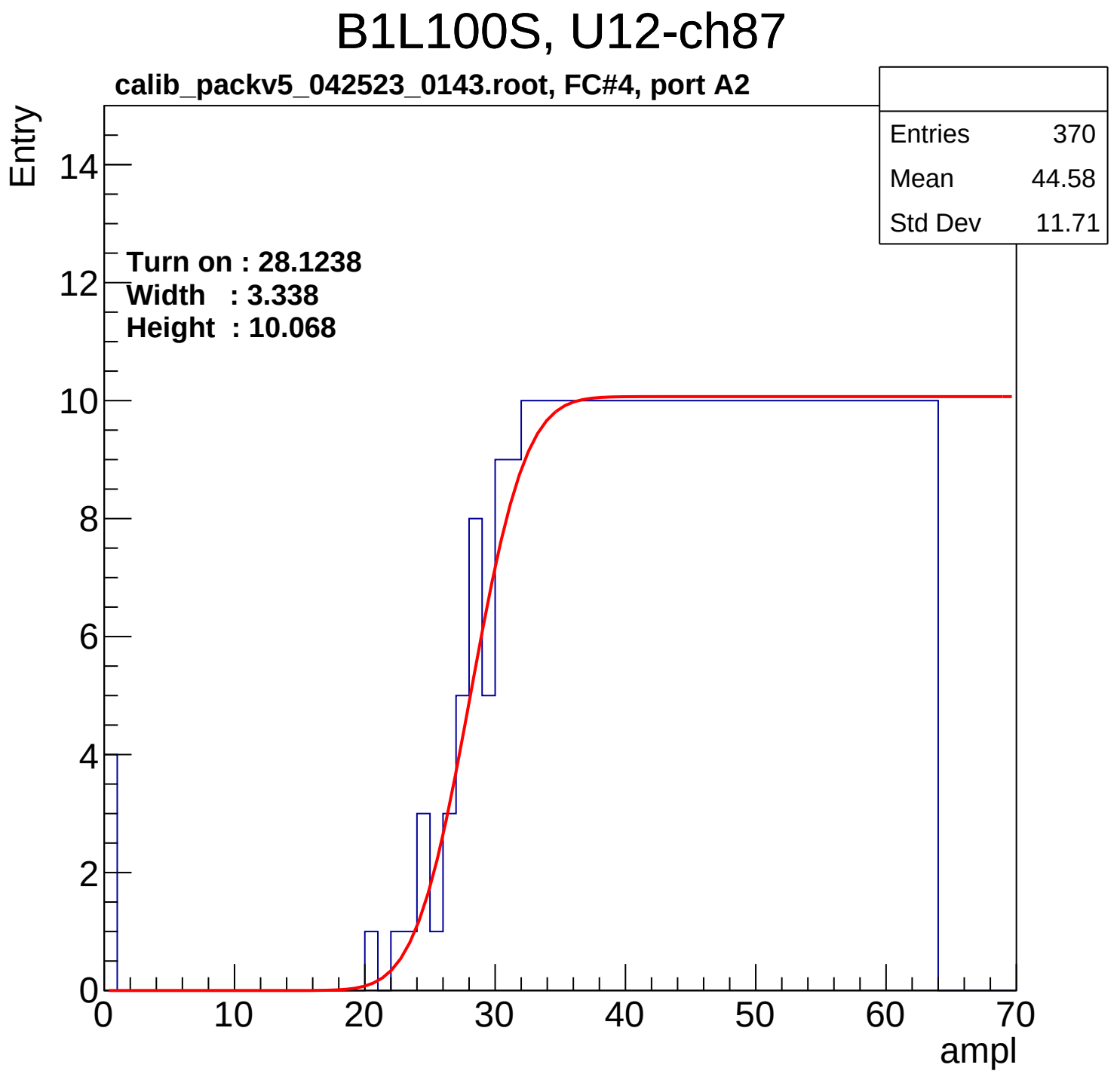

B1L100S, U12-ch82
calib_packv5_042523_0143.root, FC#4, port A2
Entries 368
Mean 44.86
Std Dev 11.38
Turn on : 27.7505
Width : 2.367
Height : 9.999
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

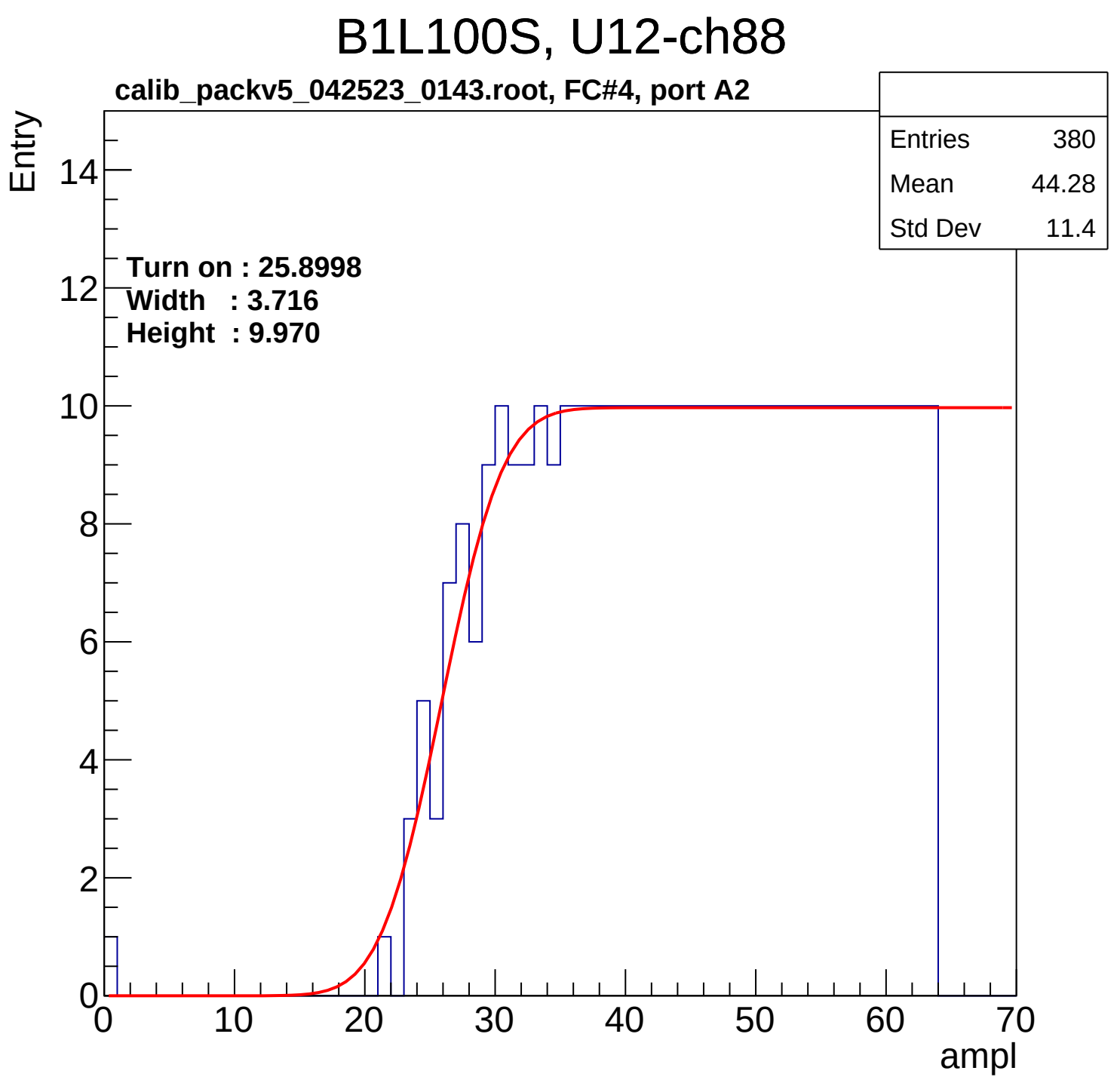

B1L100S, U12-ch83
calib_packv5_042523_0143.root, FC#4, port A2
Entries 367
Mean 44.98
Std Dev 10.96
Turn on : 27.5342
Width : 2.503
Height : 9.990
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

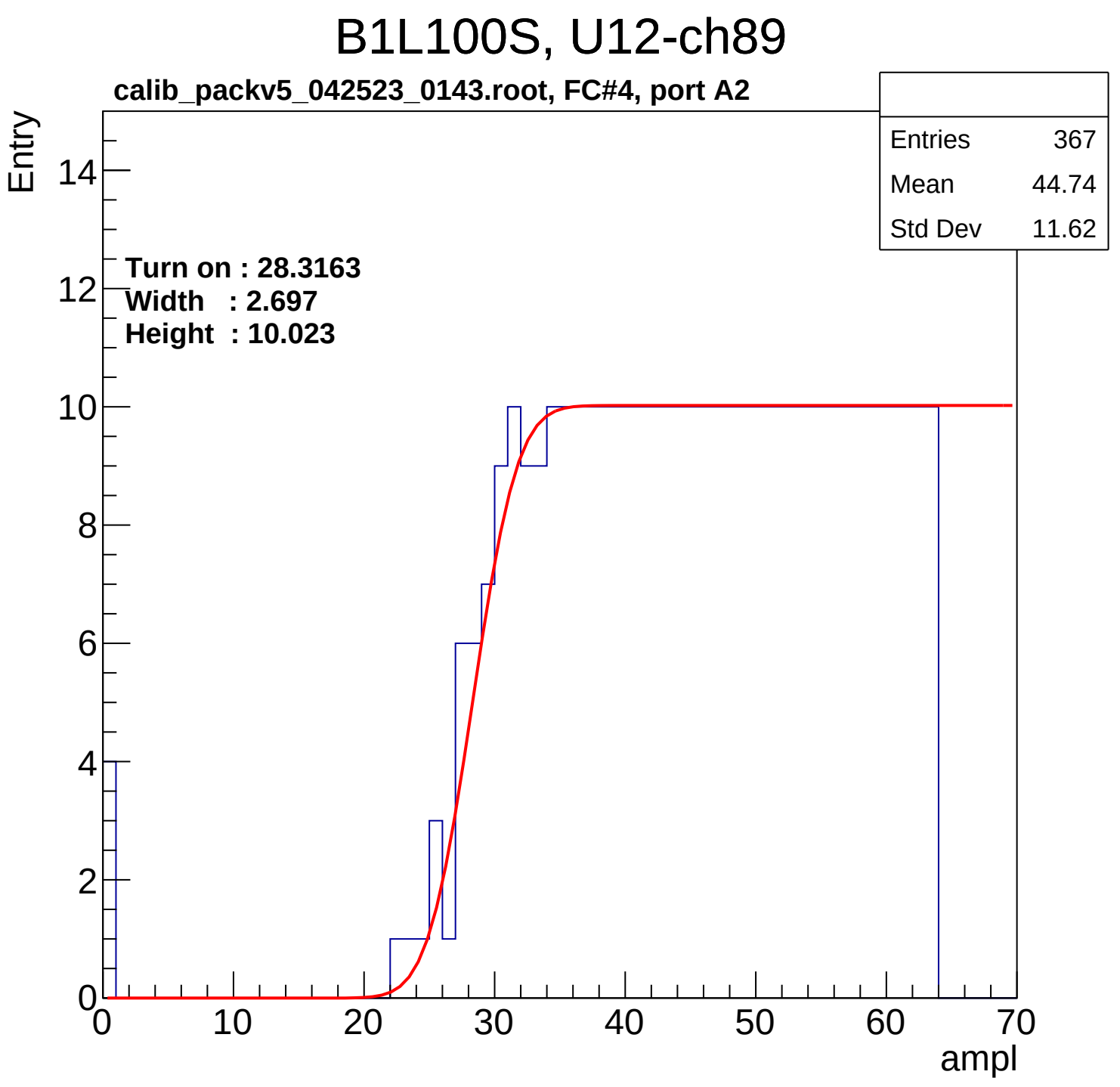

B1L100S, U12-ch84
calib_packv5_042523_0143.root, FC#4, port A2
Entries 358
Mean 45.28
Std Dev 11.15
Turn on : 28.2759
Width : 2.241
Height : 9.941
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

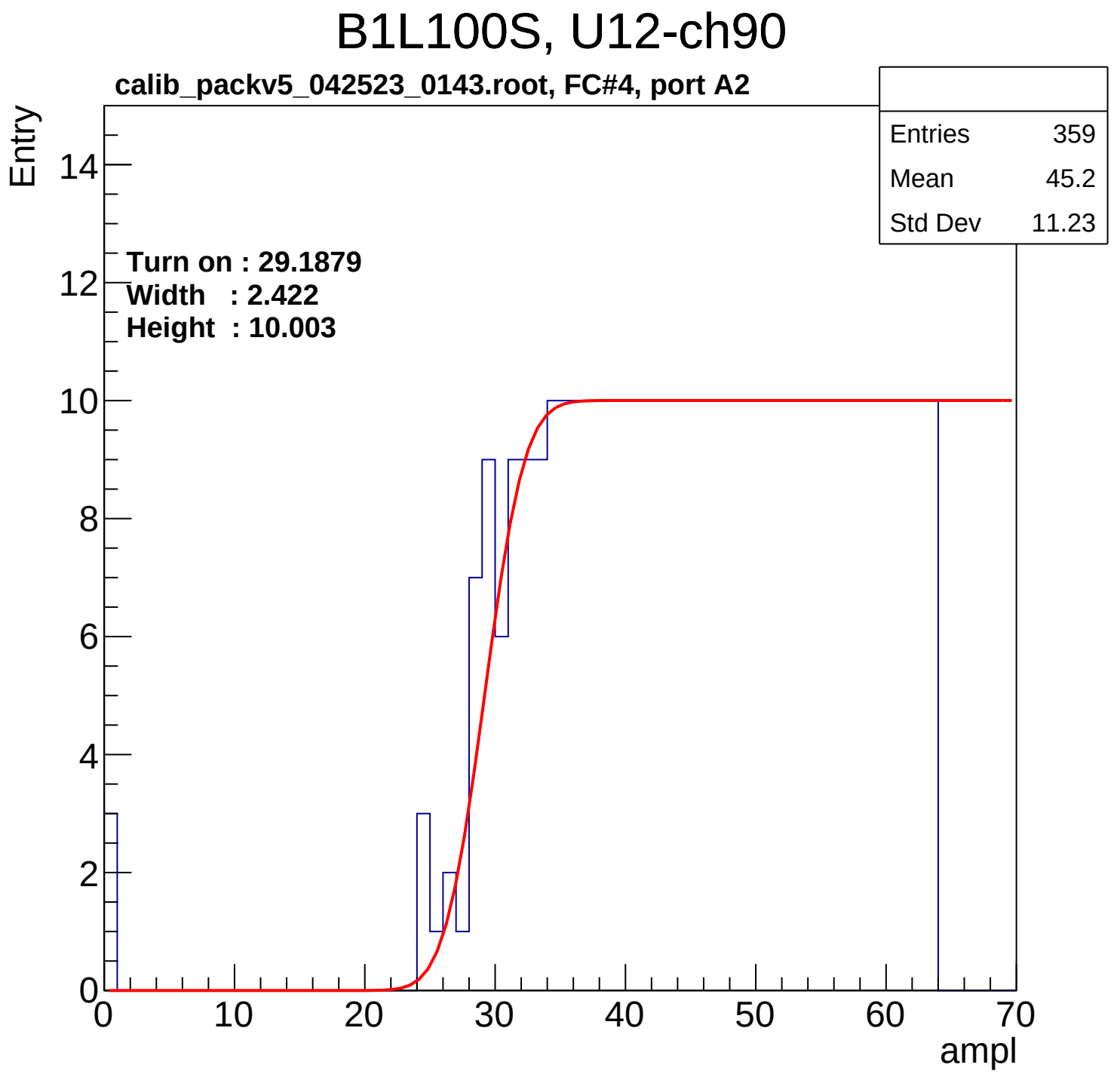

B1L100S, U12-ch85
calib_packv5_042523_0143.root, FC#4, port A2
Entries 359
Mean 45.01
Std Dev 11.71
Turn on : 29.2634
Width : 4.178
Height : 10.099
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

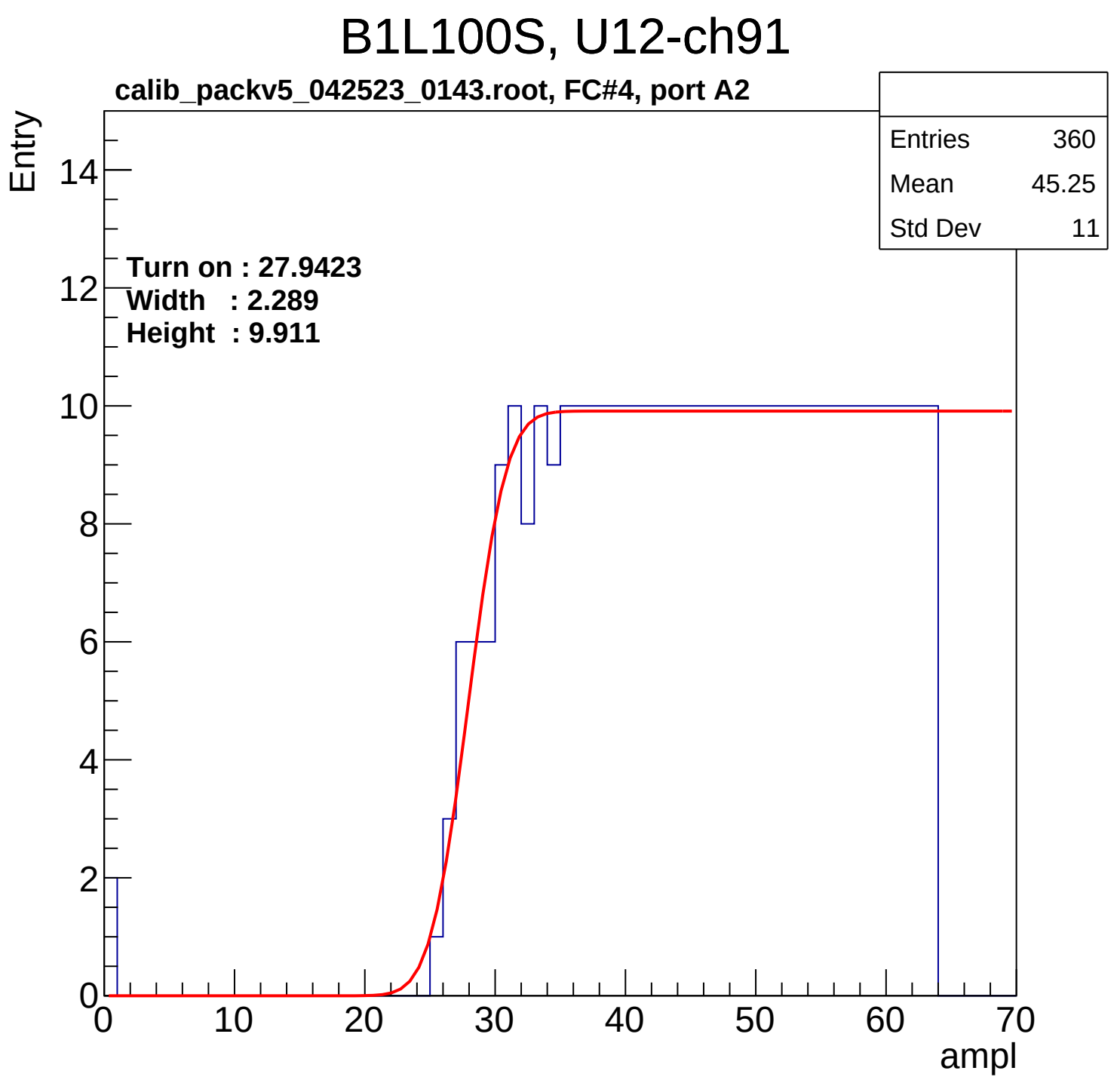

B1L100S, U12-ch86
calib_packv5_042523_0143.root, FC#4, port A2
Entries 380
Mean 44.34
Std Dev 11.32
Turn on : 26.3291
Width : 2.893
Height : 10.023
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

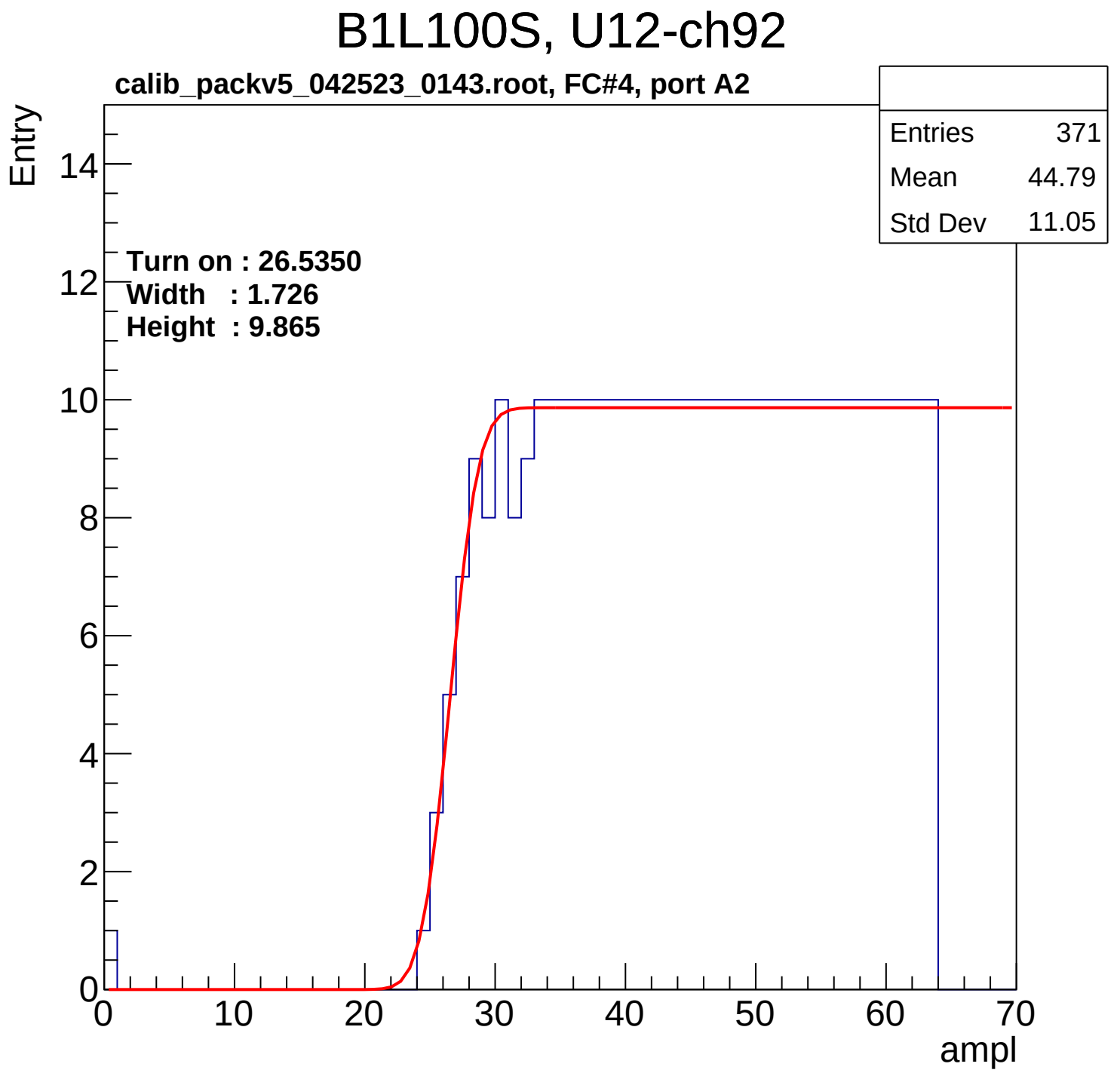

B1L100S, U12-ch87
calib_packv5_042523_0143.root, FC#4, port A2
Entries 370
Mean 44.58
Std Dev 11.71
Turn on : 28.1238
Width : 3.338
Height : 10.068
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

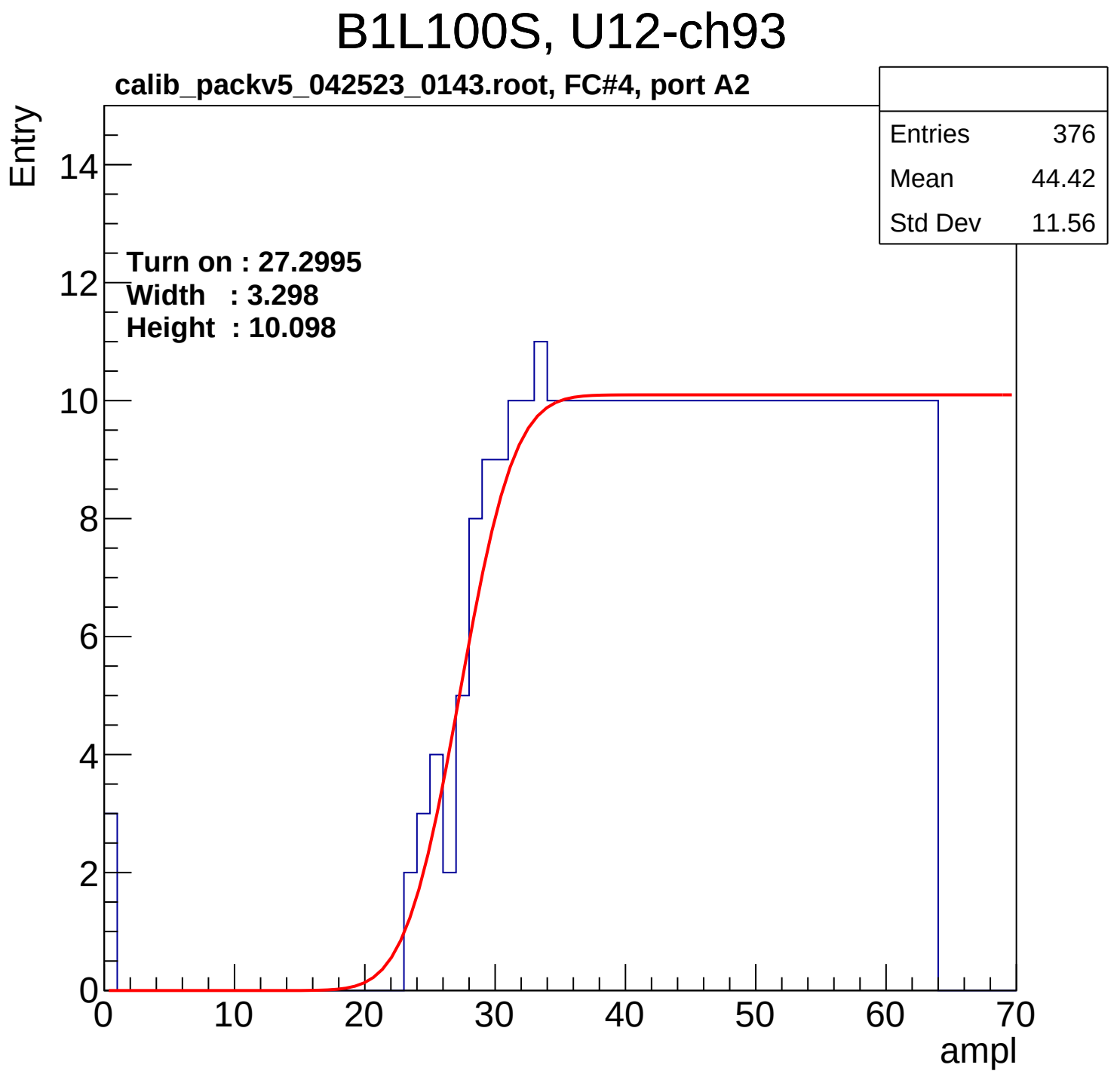

B1L100S, U12-ch88
calib_packv5_042523_0143.root, FC#4, port A2
Entries 380
Mean 44.28
Std Dev 11.4
Turn on : 25.8998
Width : 3.716
Height : 9.970
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

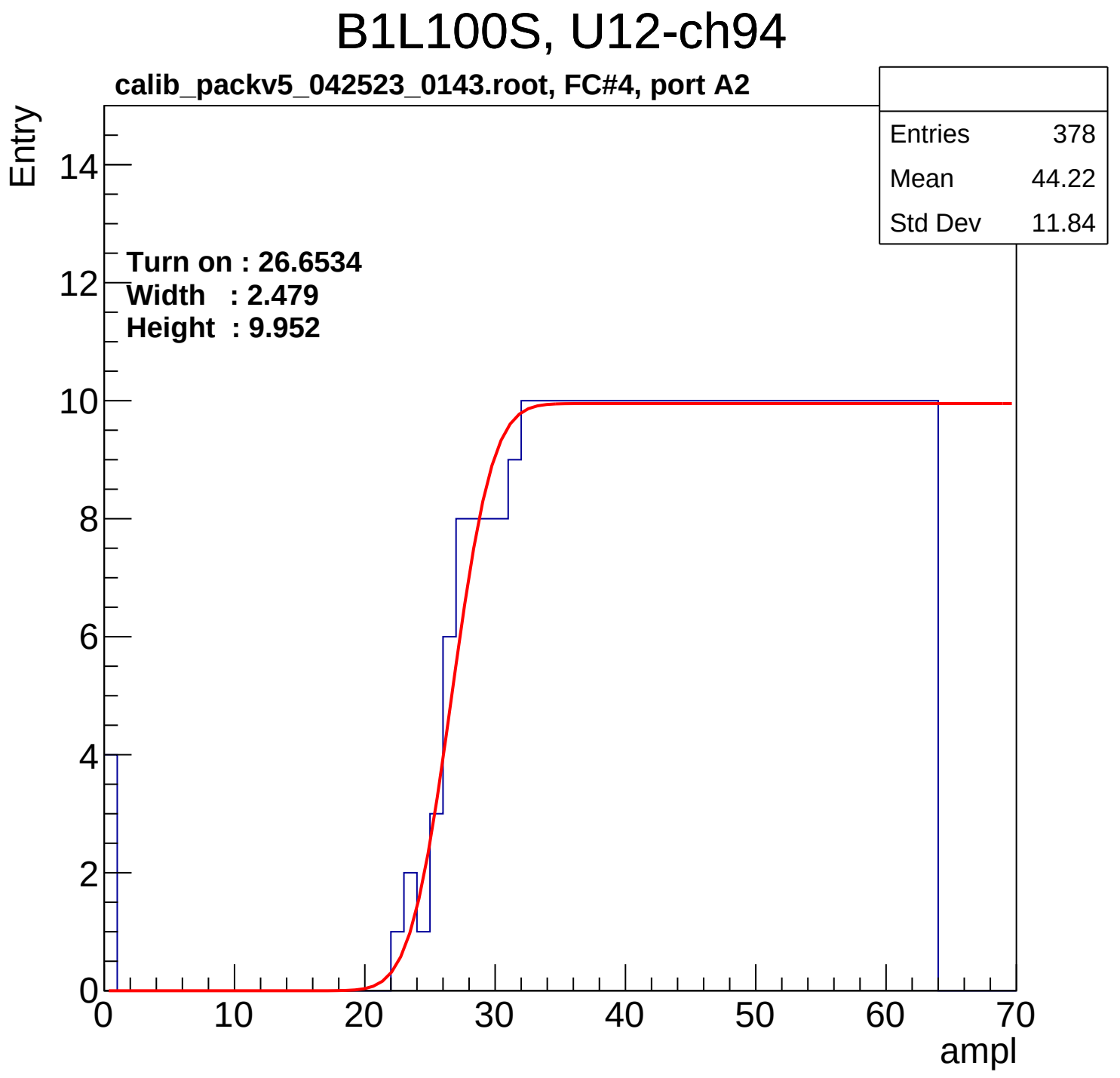

B1L100S, U12-ch89
calib_packv5_042523_0143.root, FC#4, port A2
Entries 367
Mean 44.74
Std Dev 11.62
Turn on : 28.3163
Width : 2.697
Height : 10.023
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

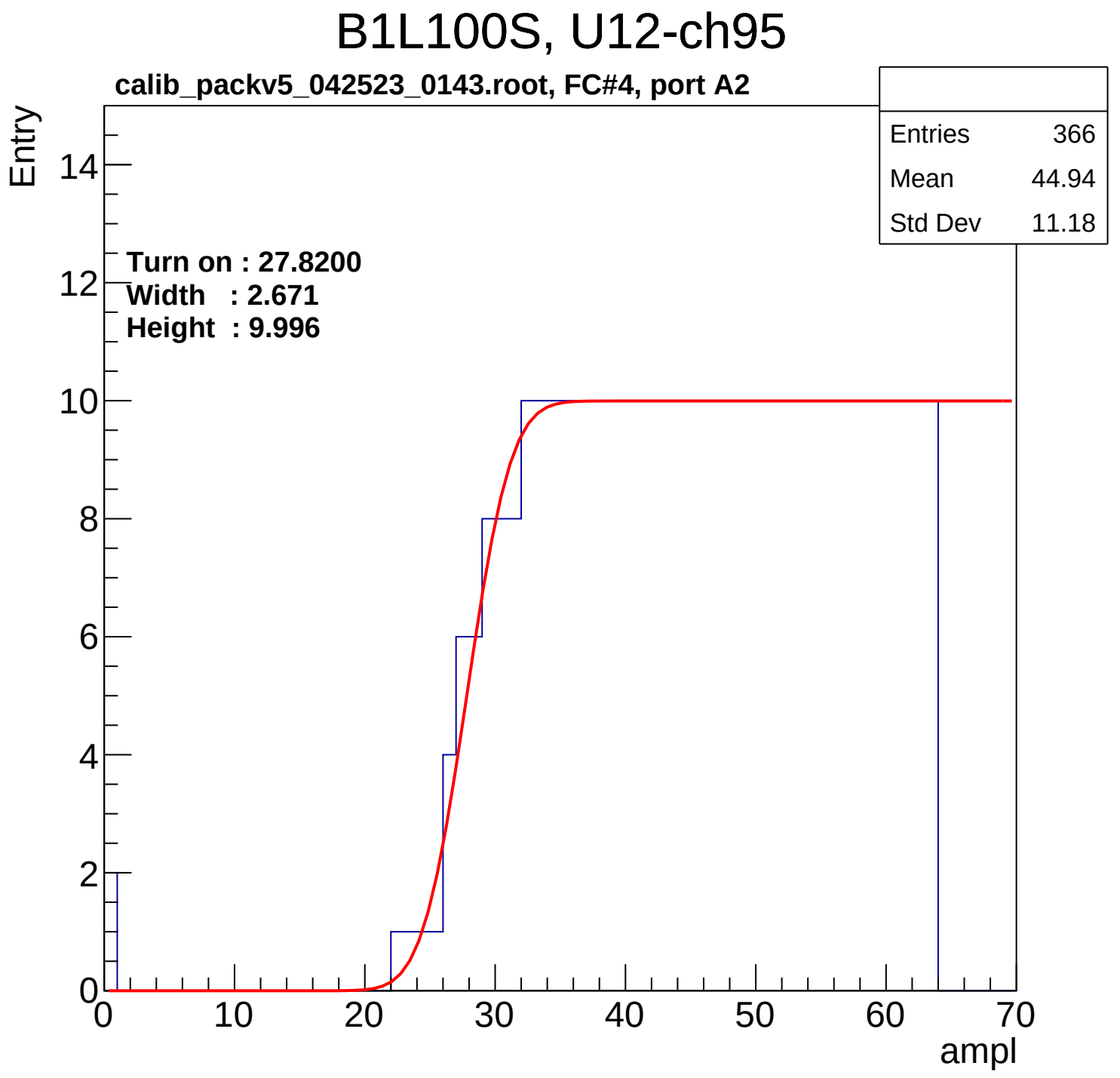

B1L100S, U12-ch90
calib_packv5_042523_0143.root, FC#4, port A2
Entries 359
Mean 45.2
Std Dev 11.23
Turn on : 29.1879
Width : 2.422
Height : 10.003
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

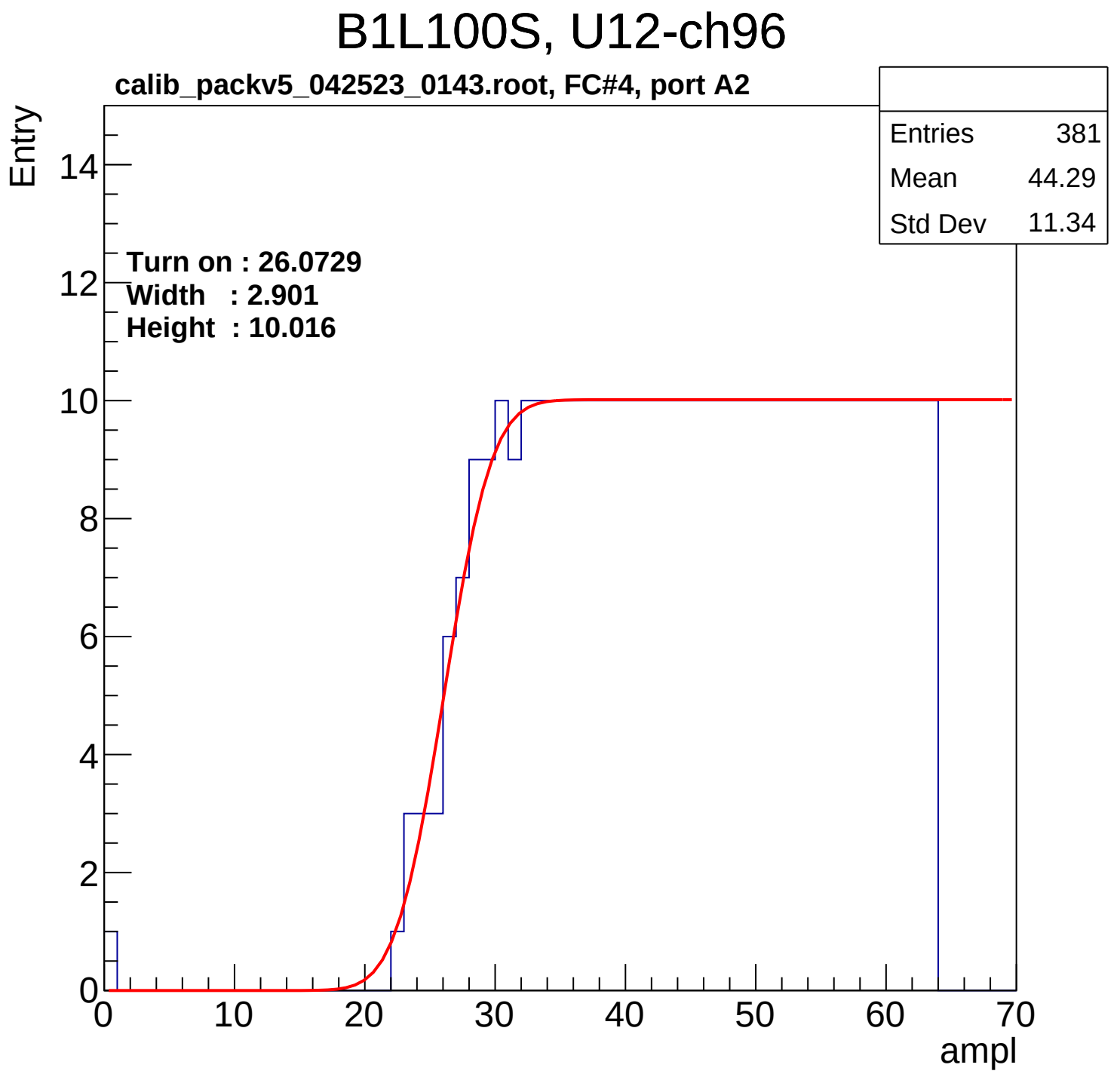

B1L100S, U12-ch91
calib_packv5_042523_0143.root, FC#4, port A2
Entries 360
Mean 45.25
Std Dev 11
Turn on : 27.9423
Width : 2.289
Height : 9.911
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

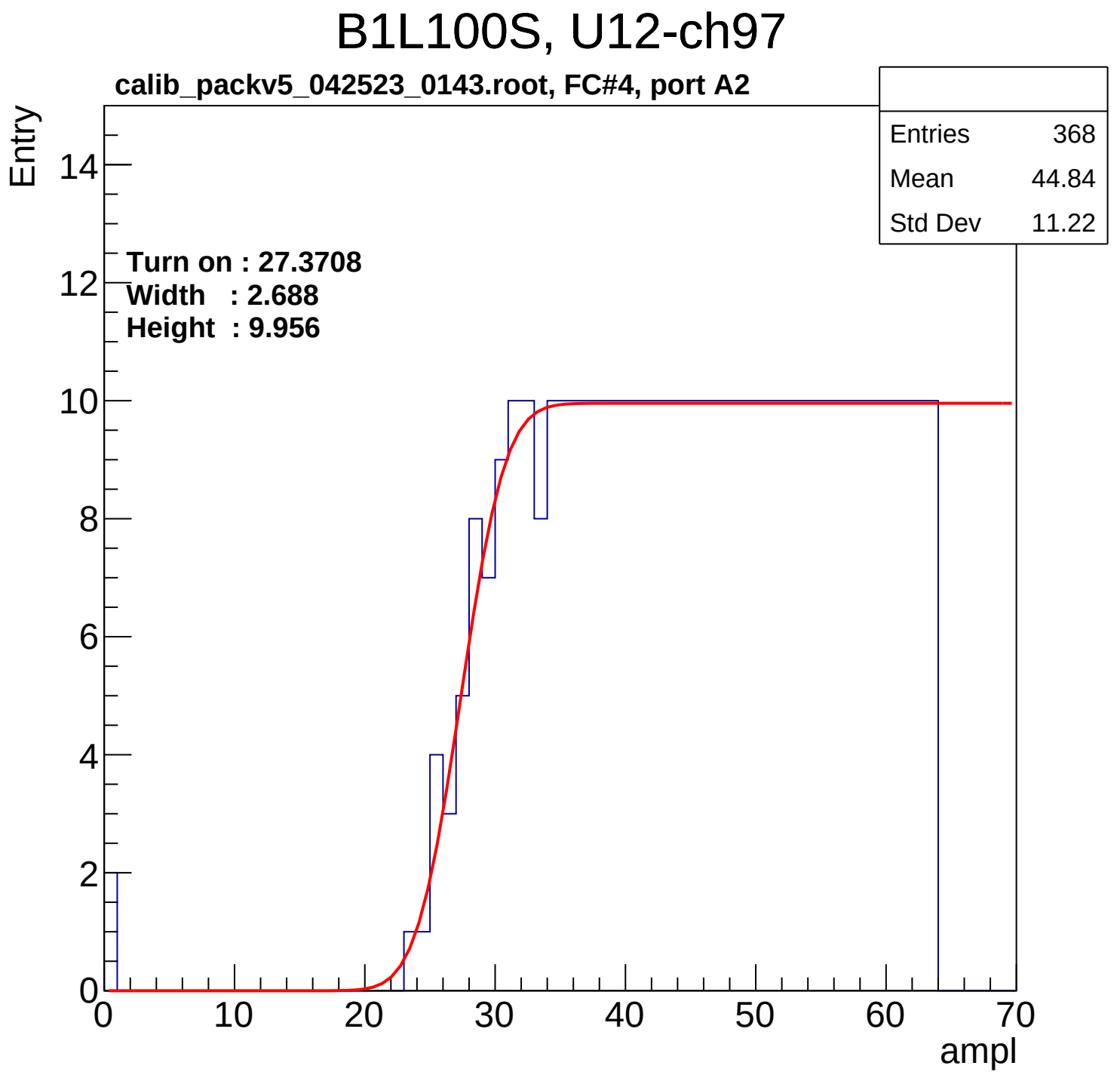

B1L100S, U12-ch92
calib_packv5_042523_0143.root, FC#4, port A2
Entries 371
Mean 44.79
Std Dev 11.05
Turn on : 26.5350
Width : 1.726
Height : 9.865
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

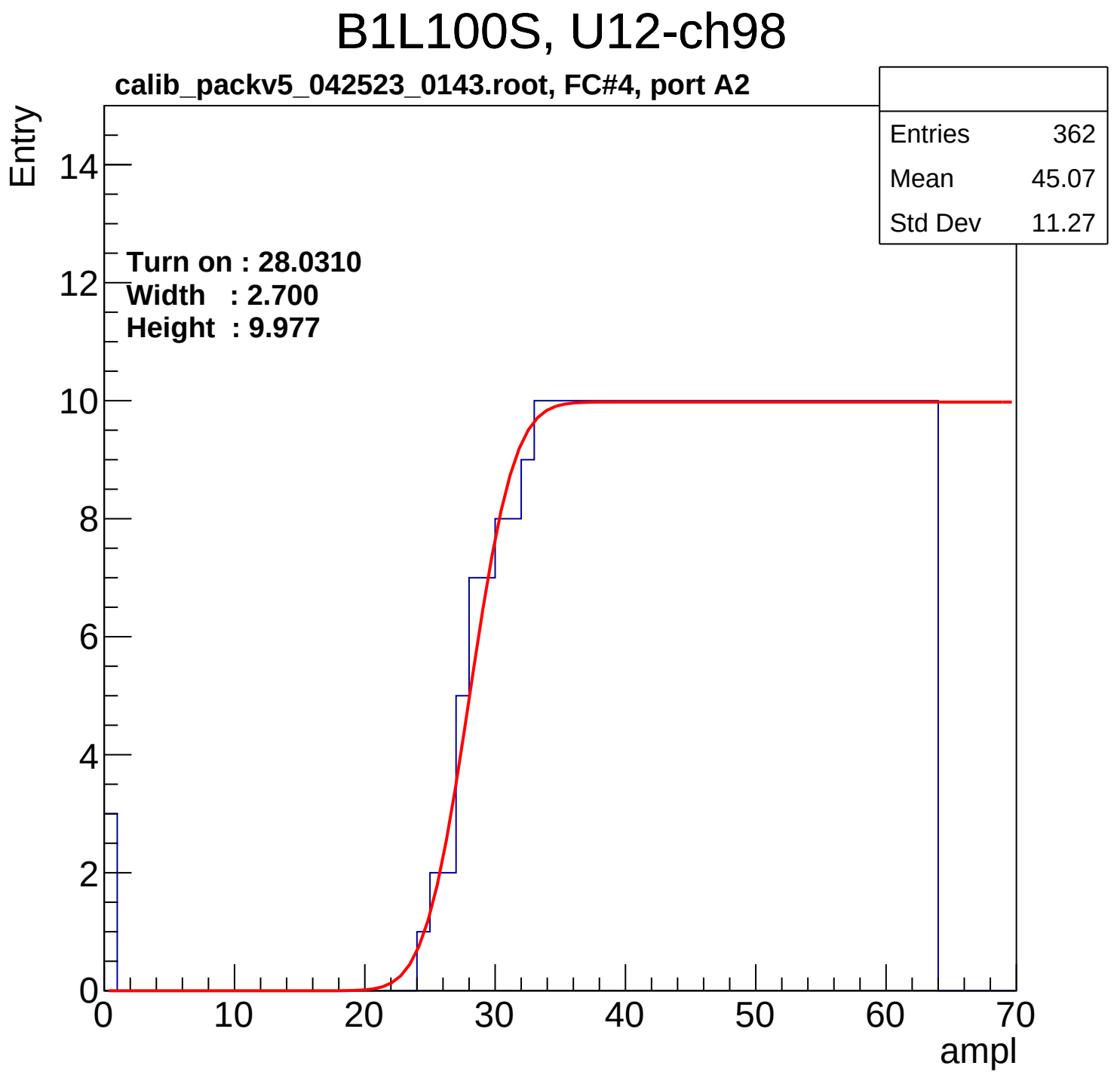

B1L100S, U12-ch93
calib_packv5_042523_0143.root, FC#4, port A2
Entries 376
Mean 44.42
Std Dev 11.56
Turn on : 27.2995
Width : 3.298
Height : 10.098
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

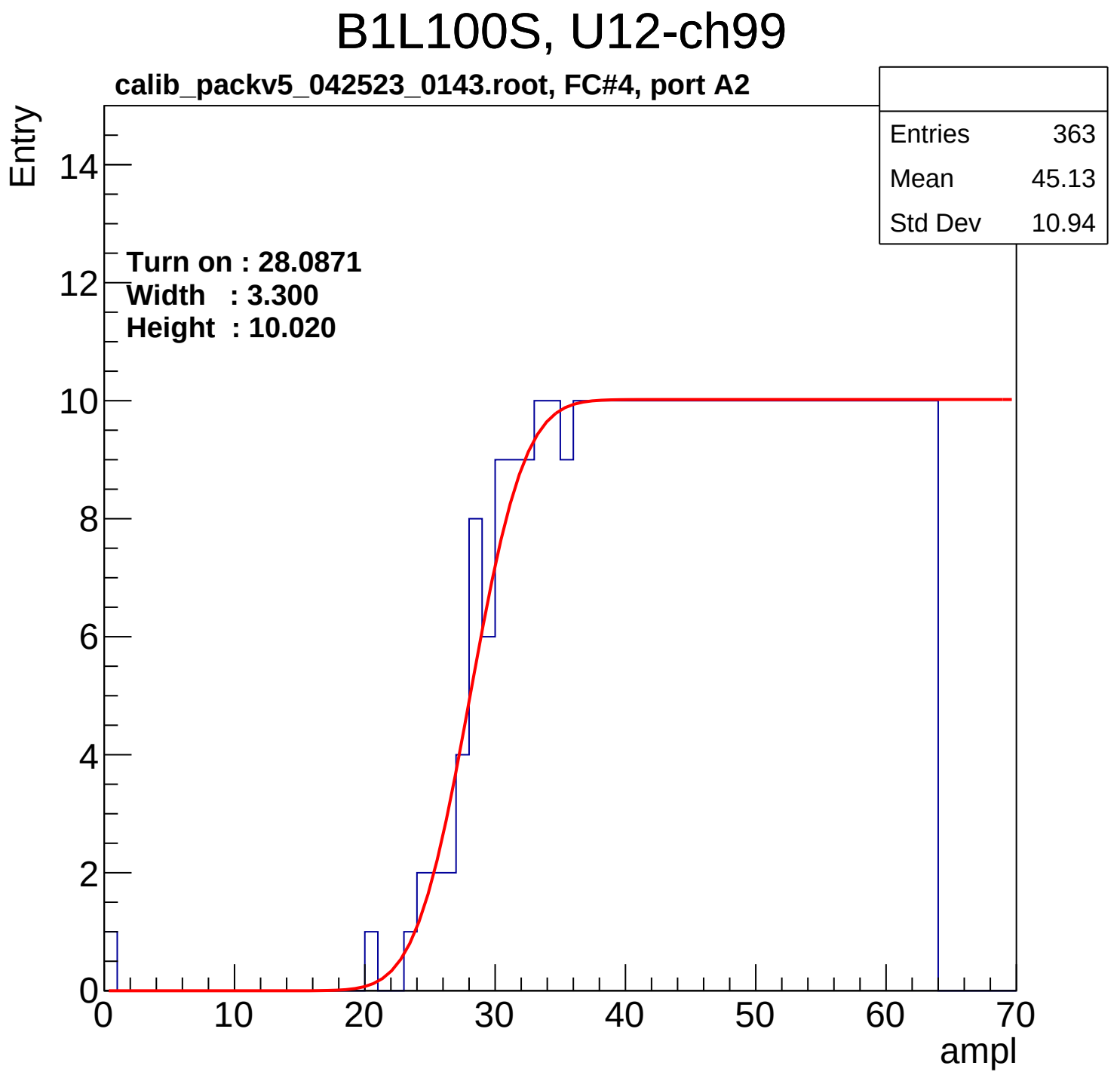

B1L100S, U12-ch94
calib_packv5_042523_0143.root, FC#4, port A2
Entries 378
Mean 44.22
Std Dev 11.84
Turn on : 26.6534
Width : 2.479
Height : 9.952
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

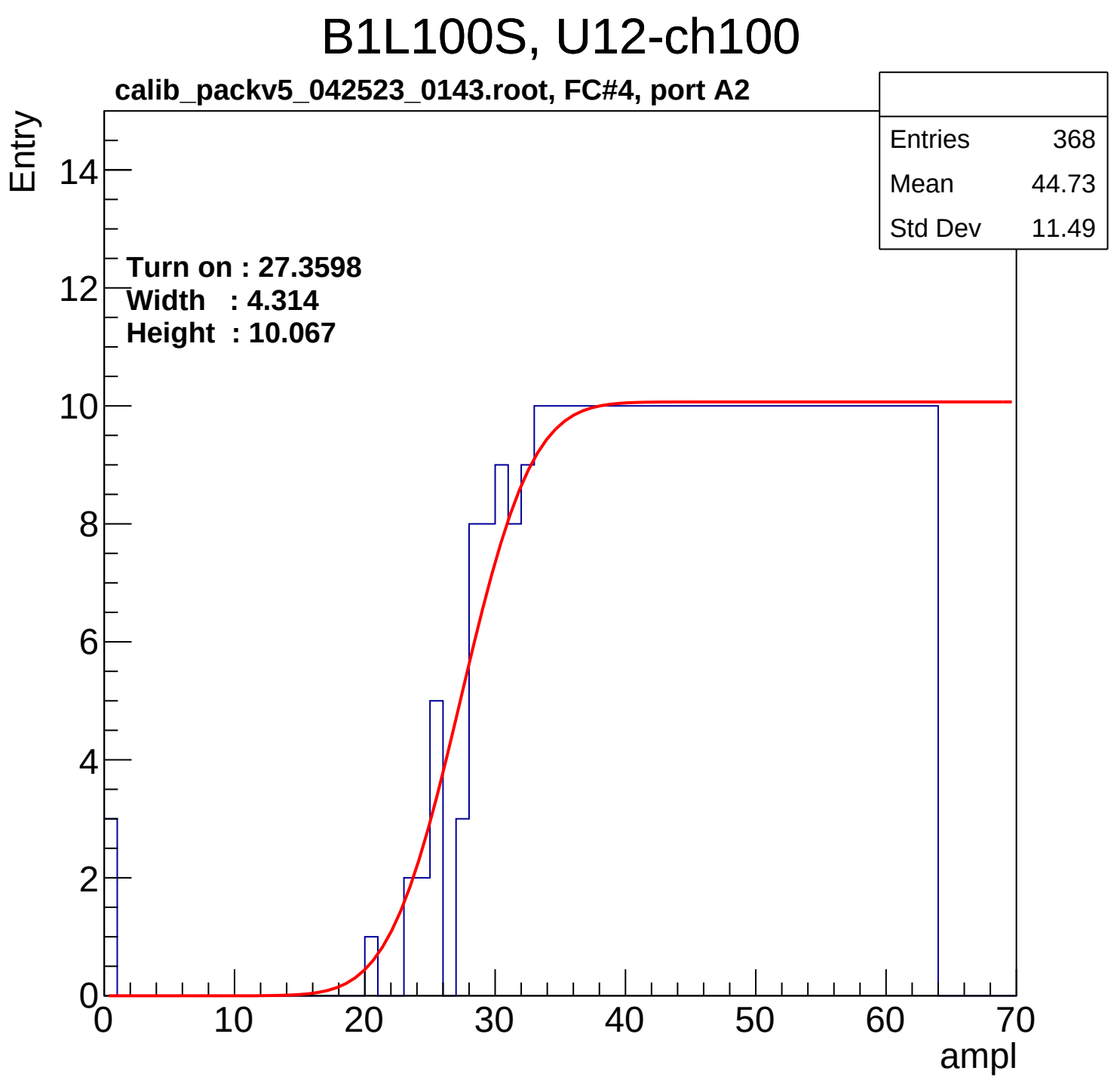

B1L100S, U12-ch95
calib_packv5_042523_0143.root, FC#4, port A2
Entries 366
Mean 44.94
Std Dev 11.18
Turn on : 27.8200
Width : 2.671
Height : 9.996
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

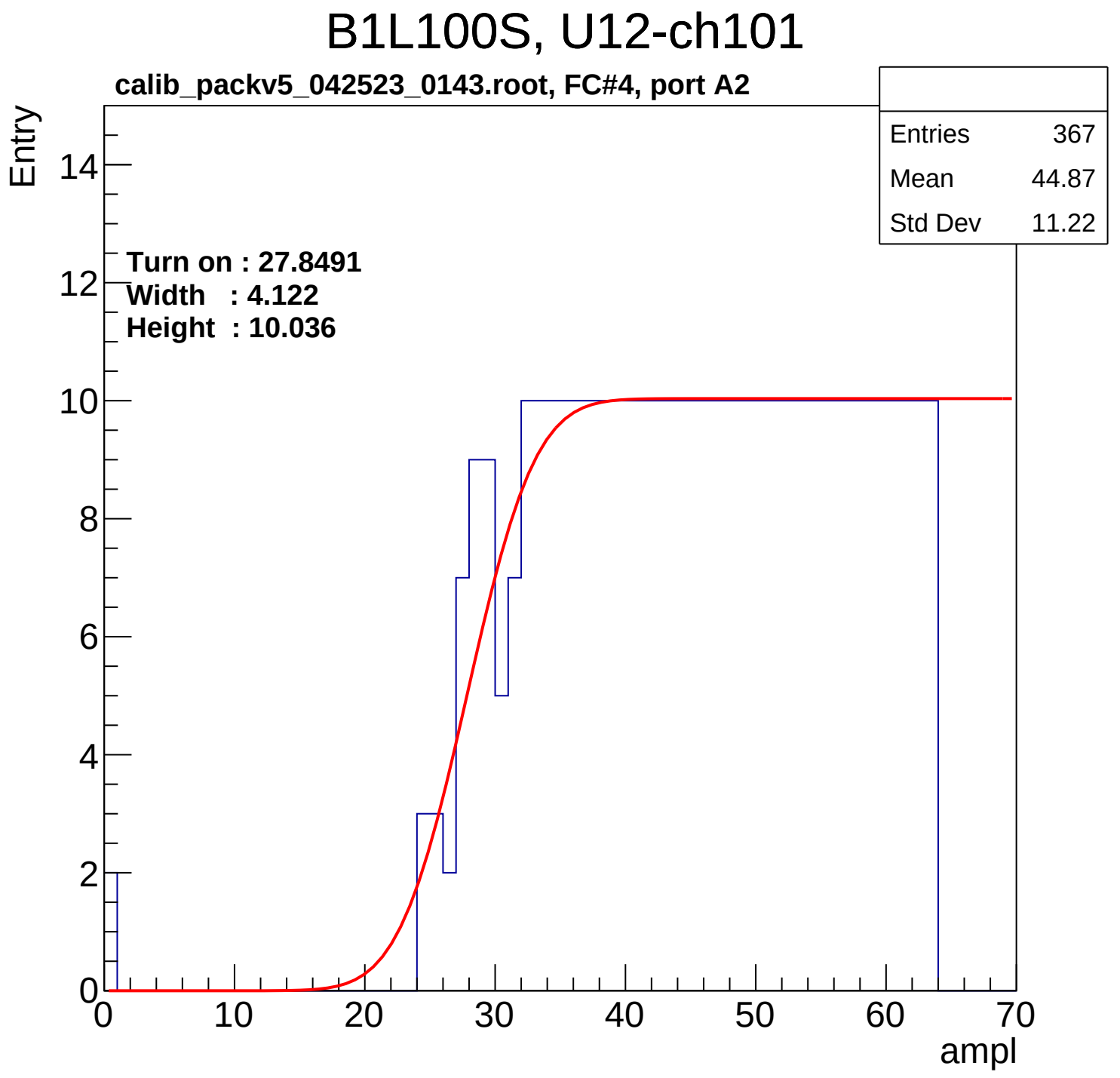

B1L100S, U12-ch96
calib_packv5_042523_0143.root, FC#4, port A2
Entries 381
Mean 44.29
Std Dev 11.34
Turn on : 26.0729
Width : 2.901
Height : 10.016
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

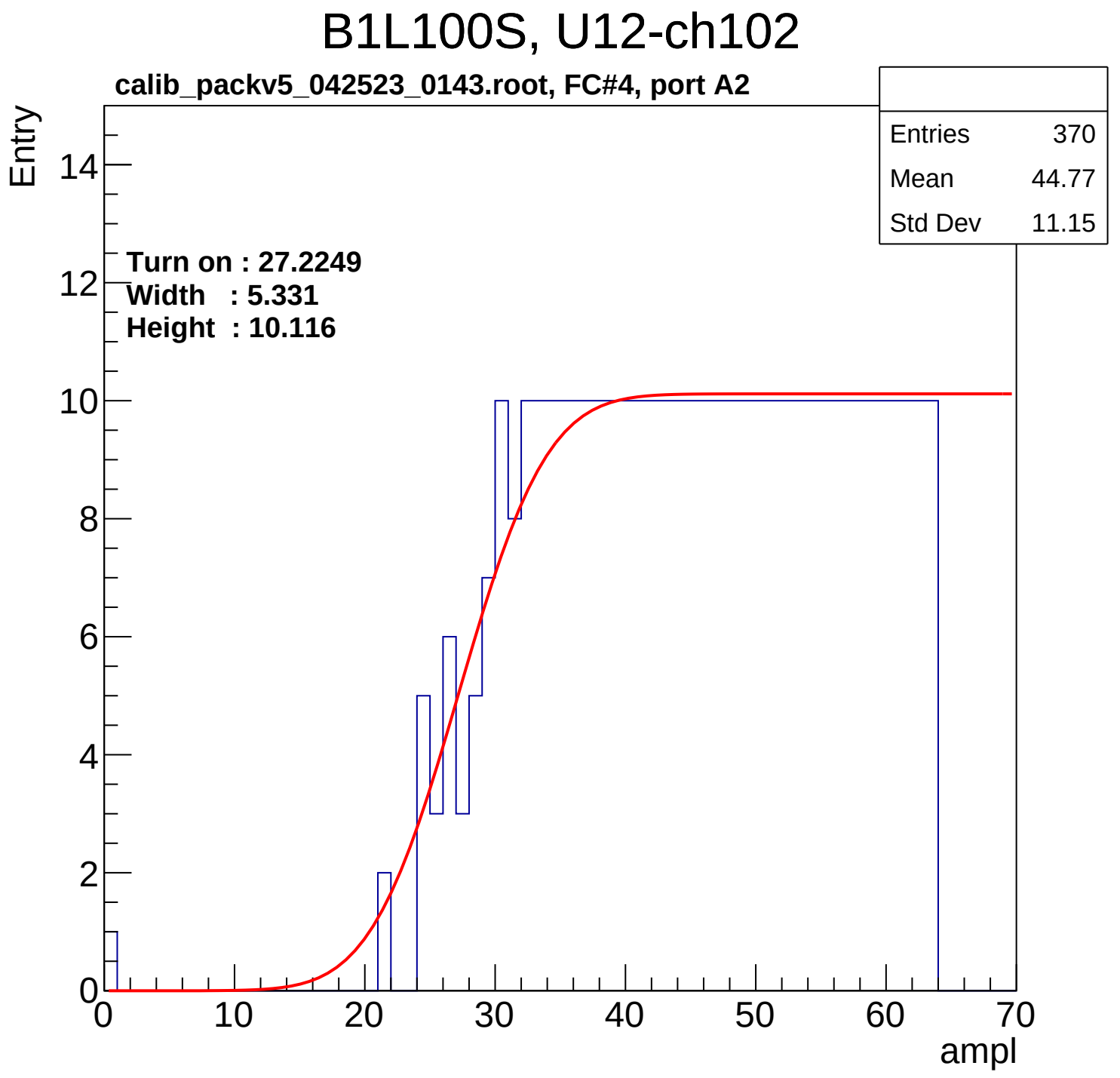

B1L100S, U12-ch97
calib_packv5_042523_0143.root, FC#4, port A2
Entries 368
Mean 44.84
Std Dev 11.22
Turn on : 27.3708
Width : 2.688
Height : 9.956
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

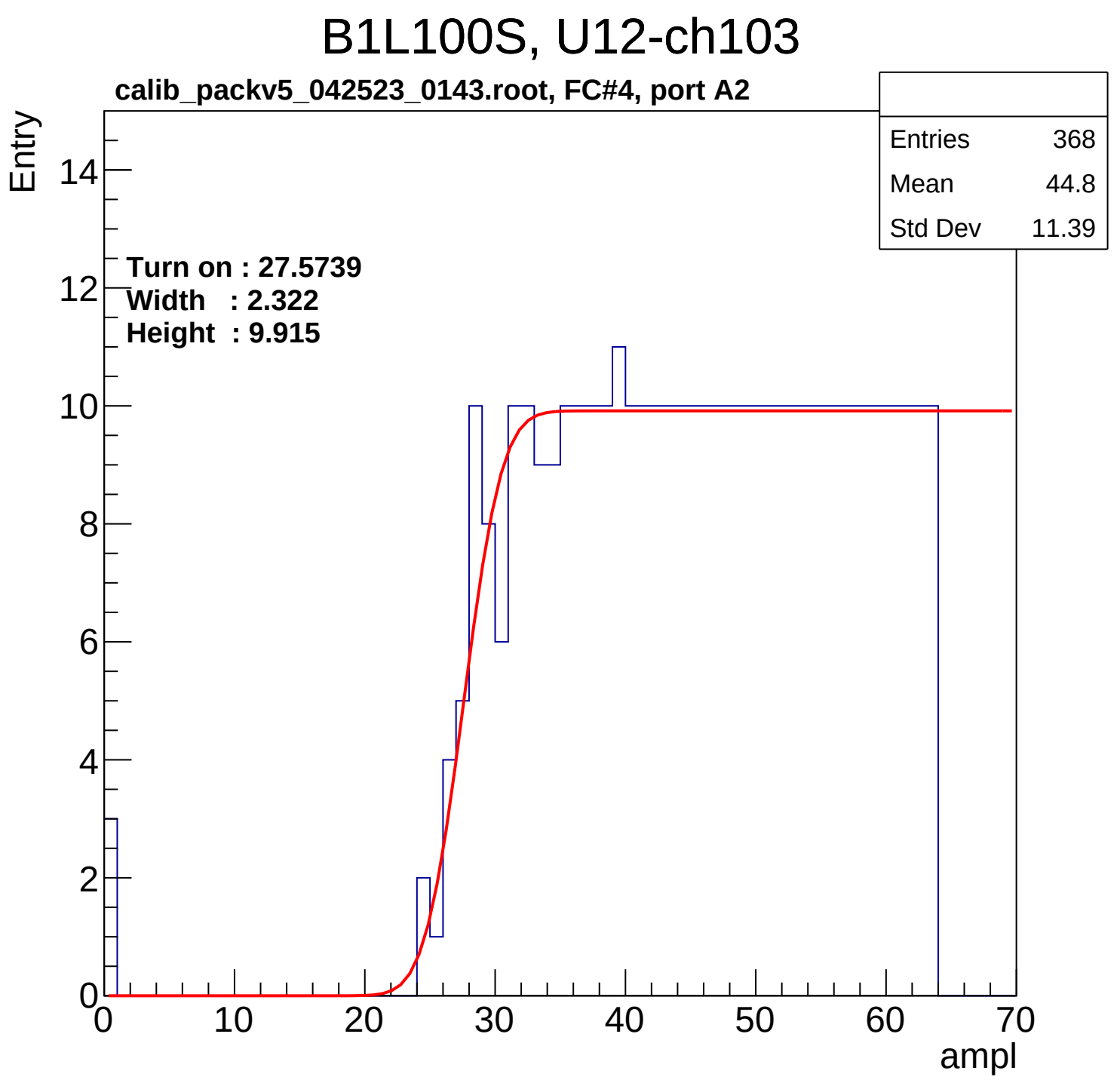

B1L100S, U12-ch98
calib_packv5_042523_0143.root, FC#4, port A2
Entries 362
Mean 45.07
Std Dev 11.27
Turn on : 28.0310
Width : 2.700
Height : 9.977
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

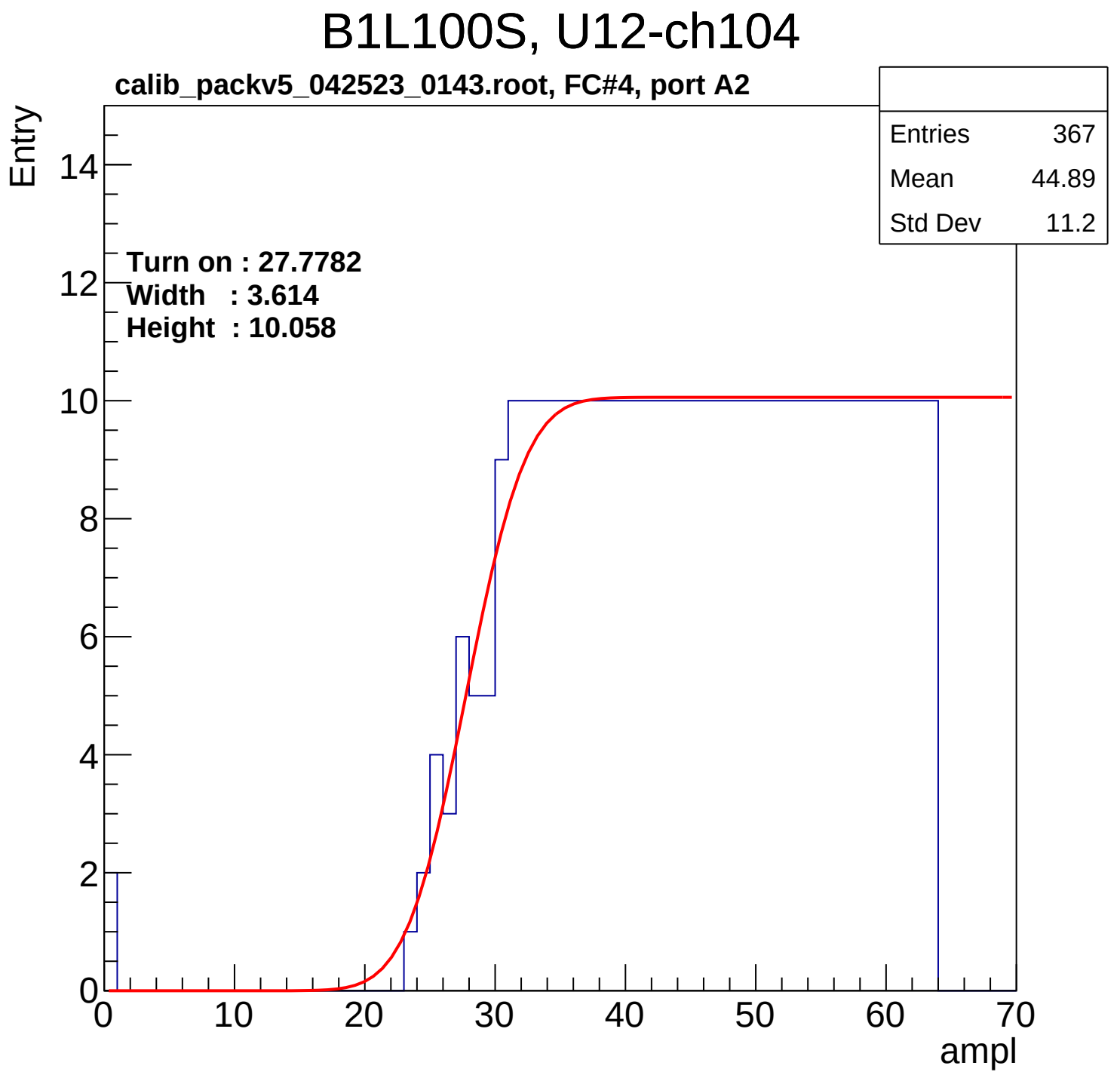

B1L100S, U12-ch99
calib_packv5_042523_0143.root, FC#4, port A2
Entries 363
Mean 45.13
Std Dev 10.94
Turn on : 28.0871
Width : 3.300
Height : 10.020
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

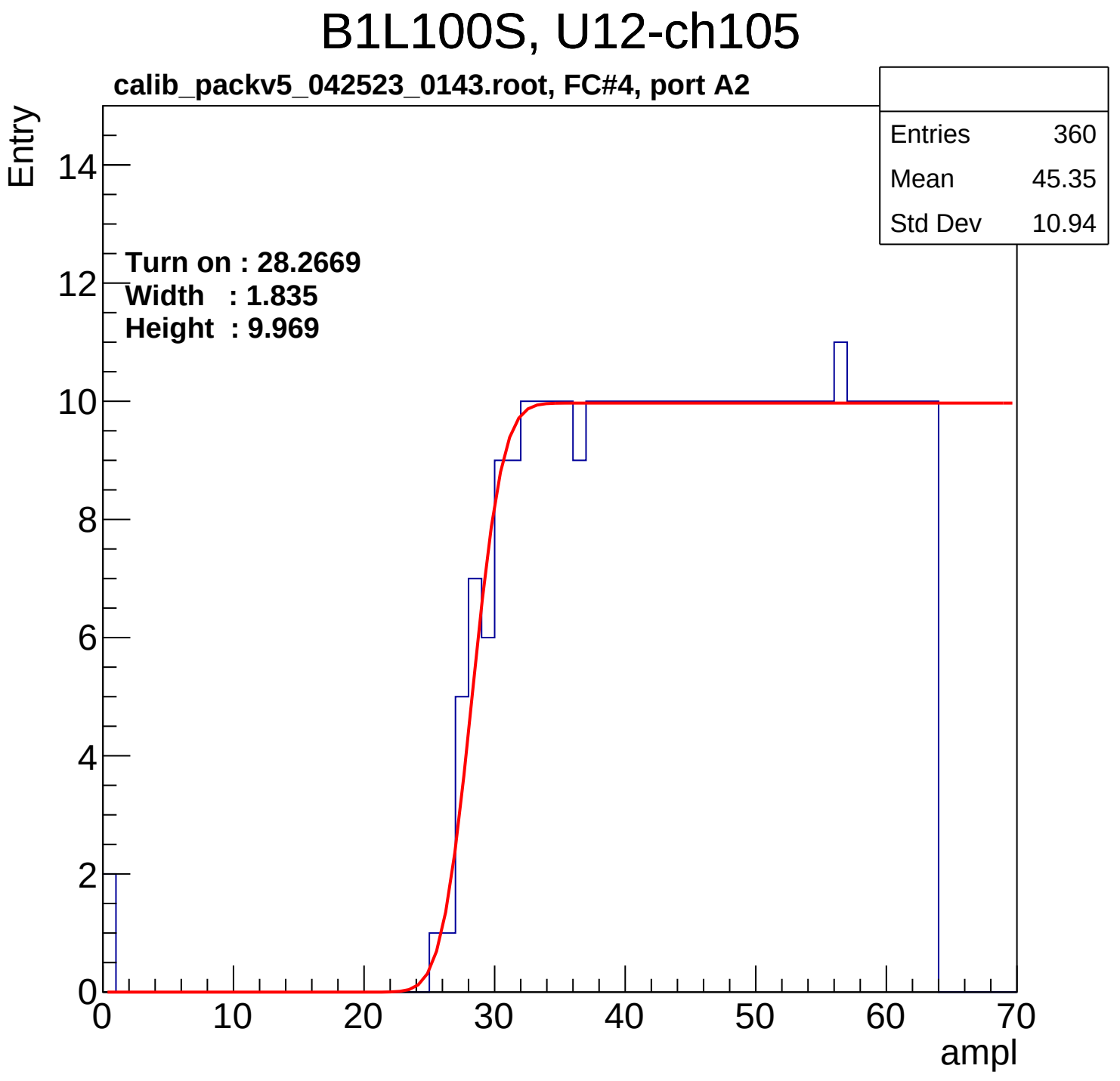

B1L100S, U12-ch100
calib_packv5_042523_0143.root, FC#4, port A2
Entries 368
Mean 44.73
Std Dev 11.49
Turn on : 27.3598
Width : 4.314
Height : 10.067
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

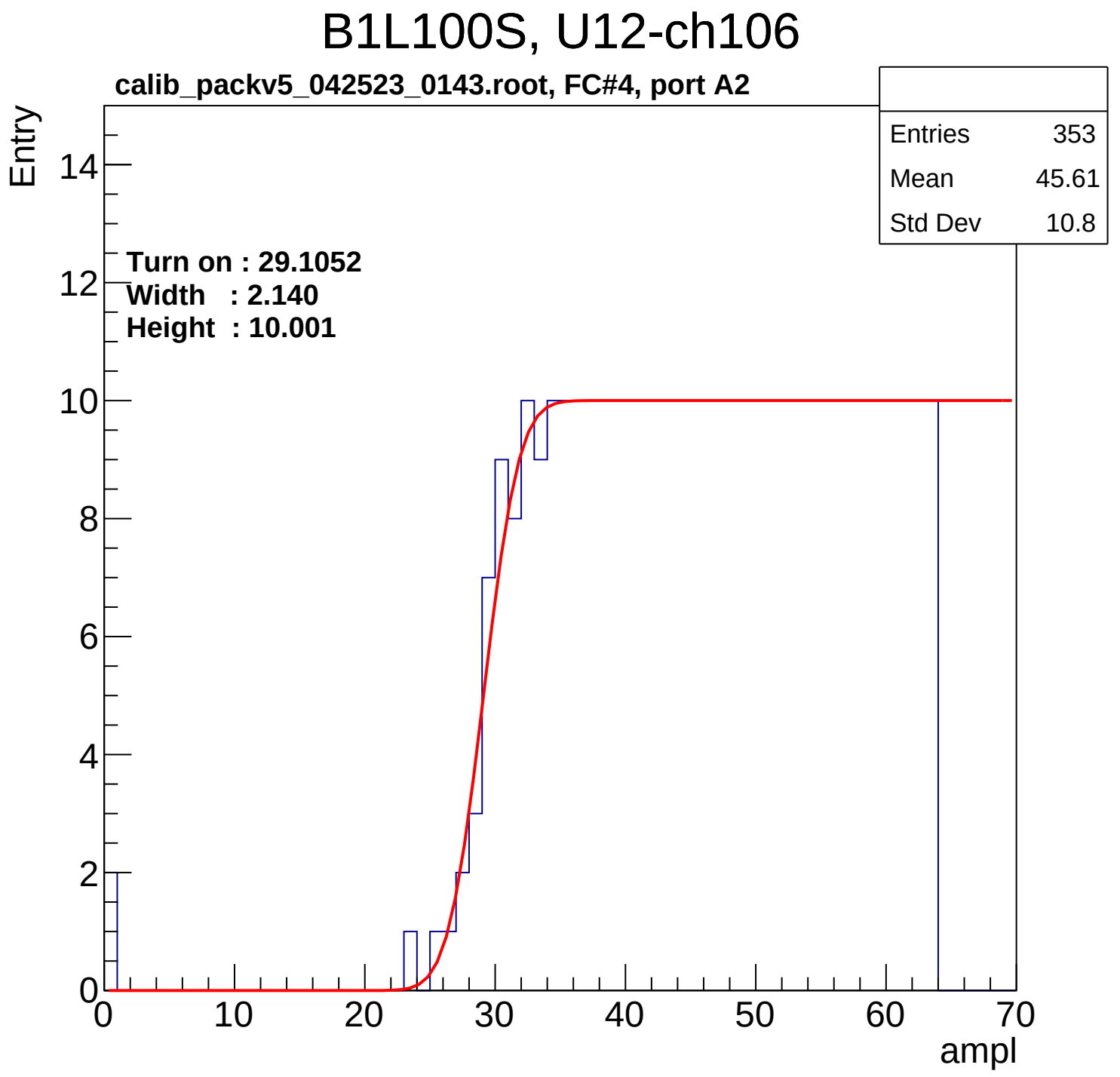

B1L100S, U12-ch101
calib_packv5_042523_0143.root, FC#4, port A2
Entries 367
Mean 44.87
Std Dev 11.22
Turn on : 27.8491
Width : 4.122
Height : 10.036
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

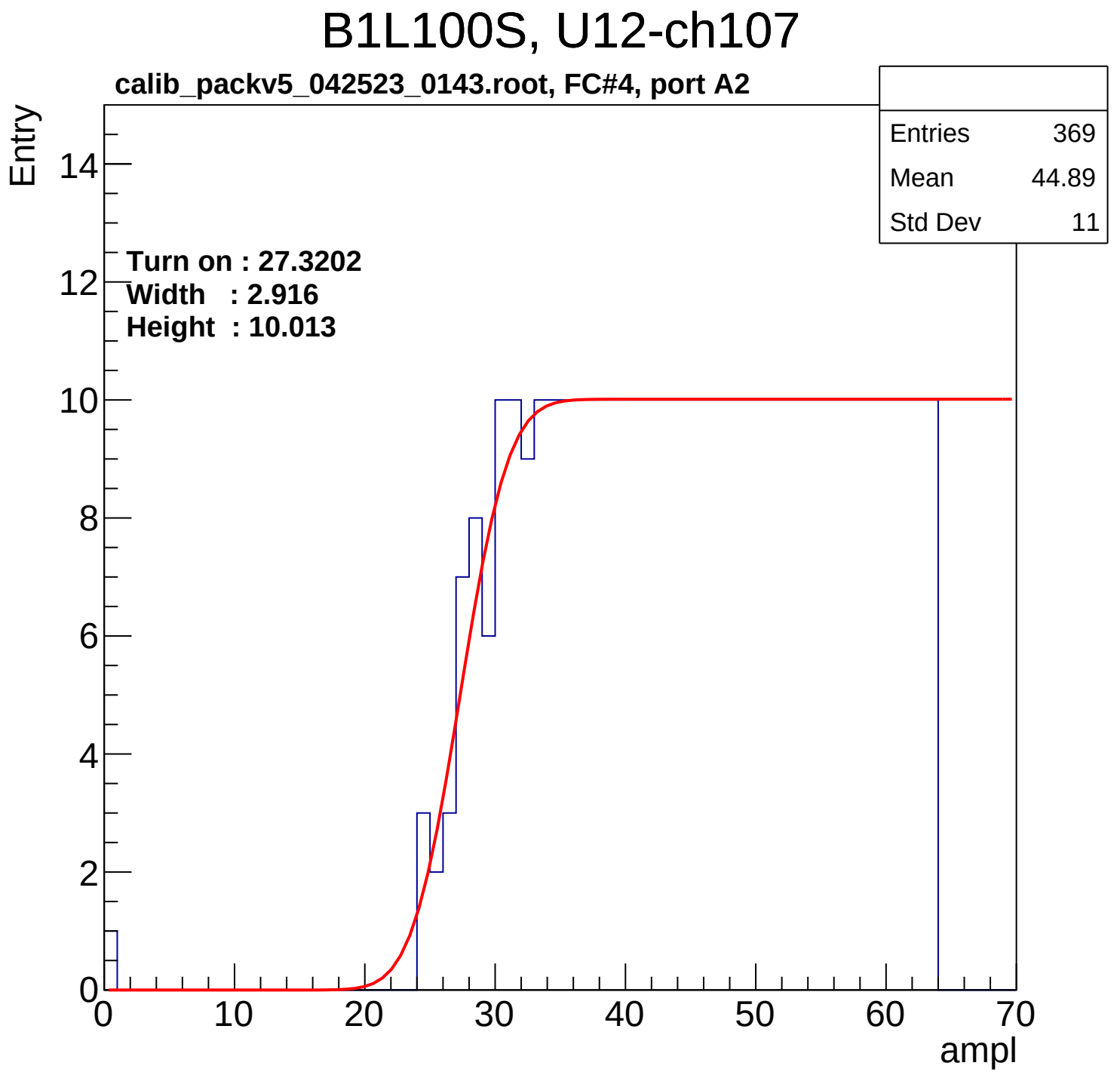

B1L100S, U12-ch102
calib_packv5_042523_0143.root, FC#4, port A2
Entries 370
Mean 44.77
Std Dev 11.15
Turn on : 27.2249
Width : 5.331
Height : 10.116
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

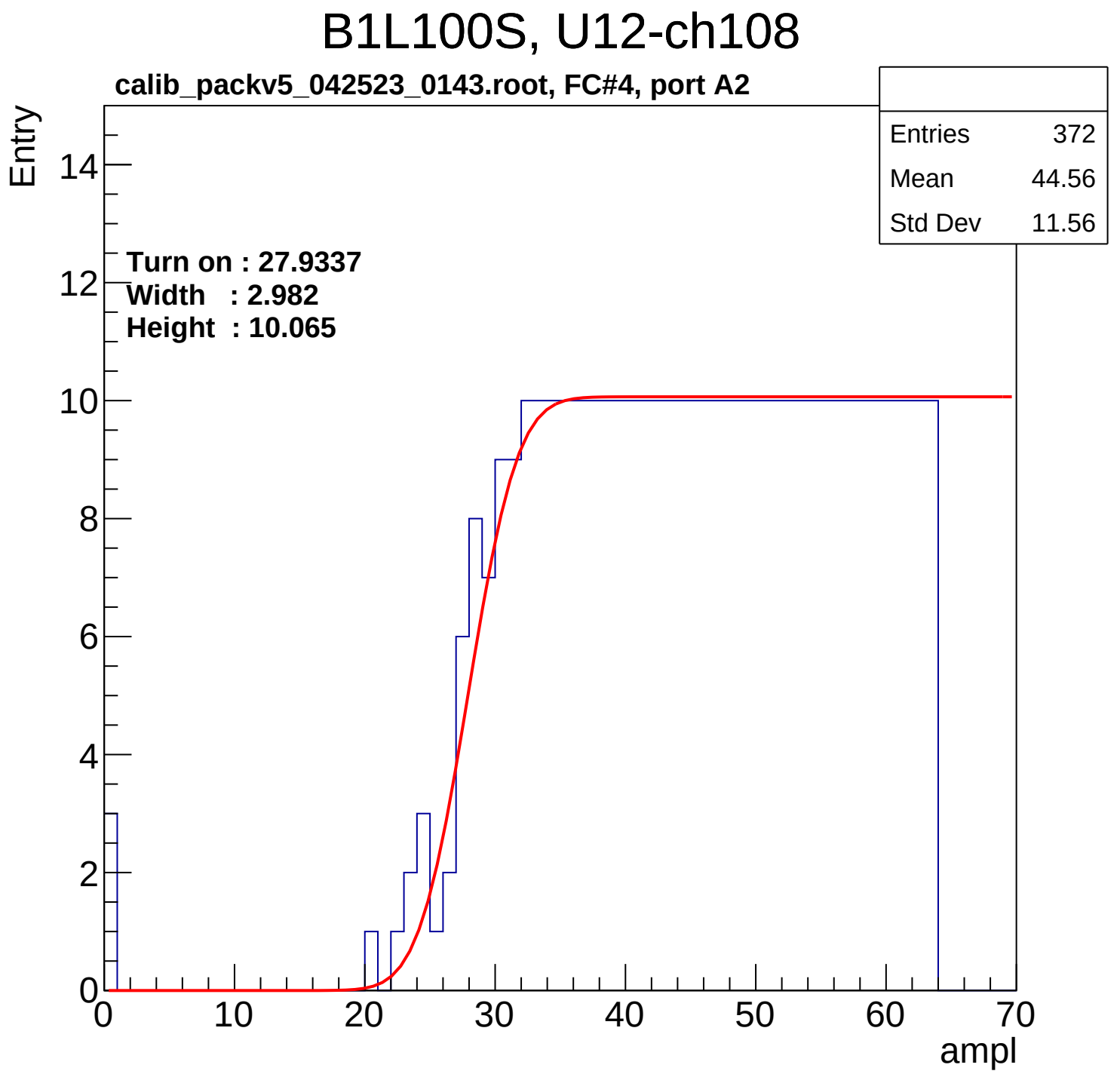

B1L100S, U12-ch103
calib_packv5_042523_0143.root, FC#4, port A2
Entries 368
Mean 44.8
Std Dev 11.39
Turn on : 27.5739
Width : 2.322
Height : 9.915
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

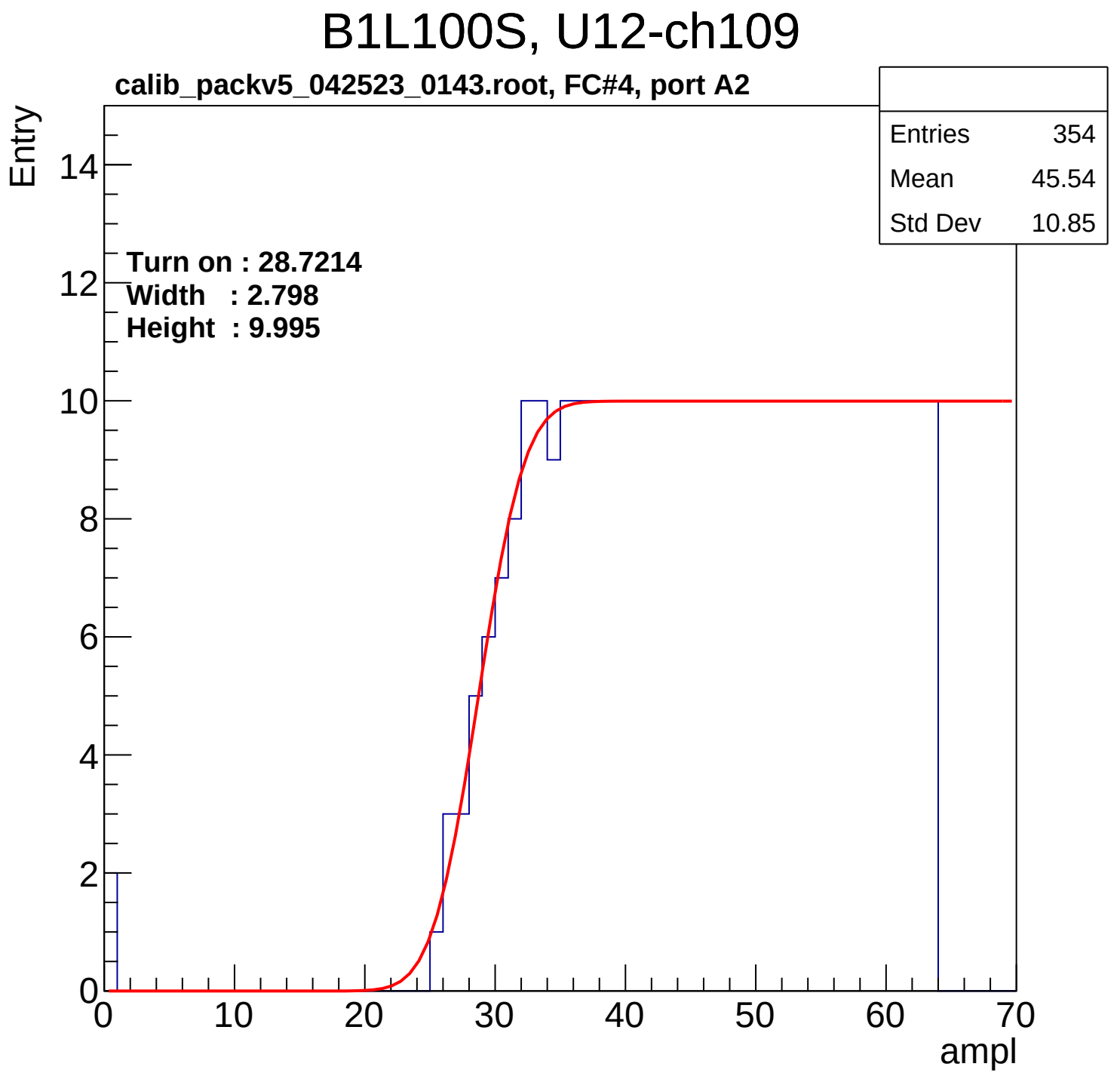

B1L100S, U12-ch104
calib_packv5_042523_0143.root, FC#4, port A2
Entries 367
Mean 44.89
Std Dev 11.2
Turn on : 27.7782
Width : 3.614
Height : 10.058
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

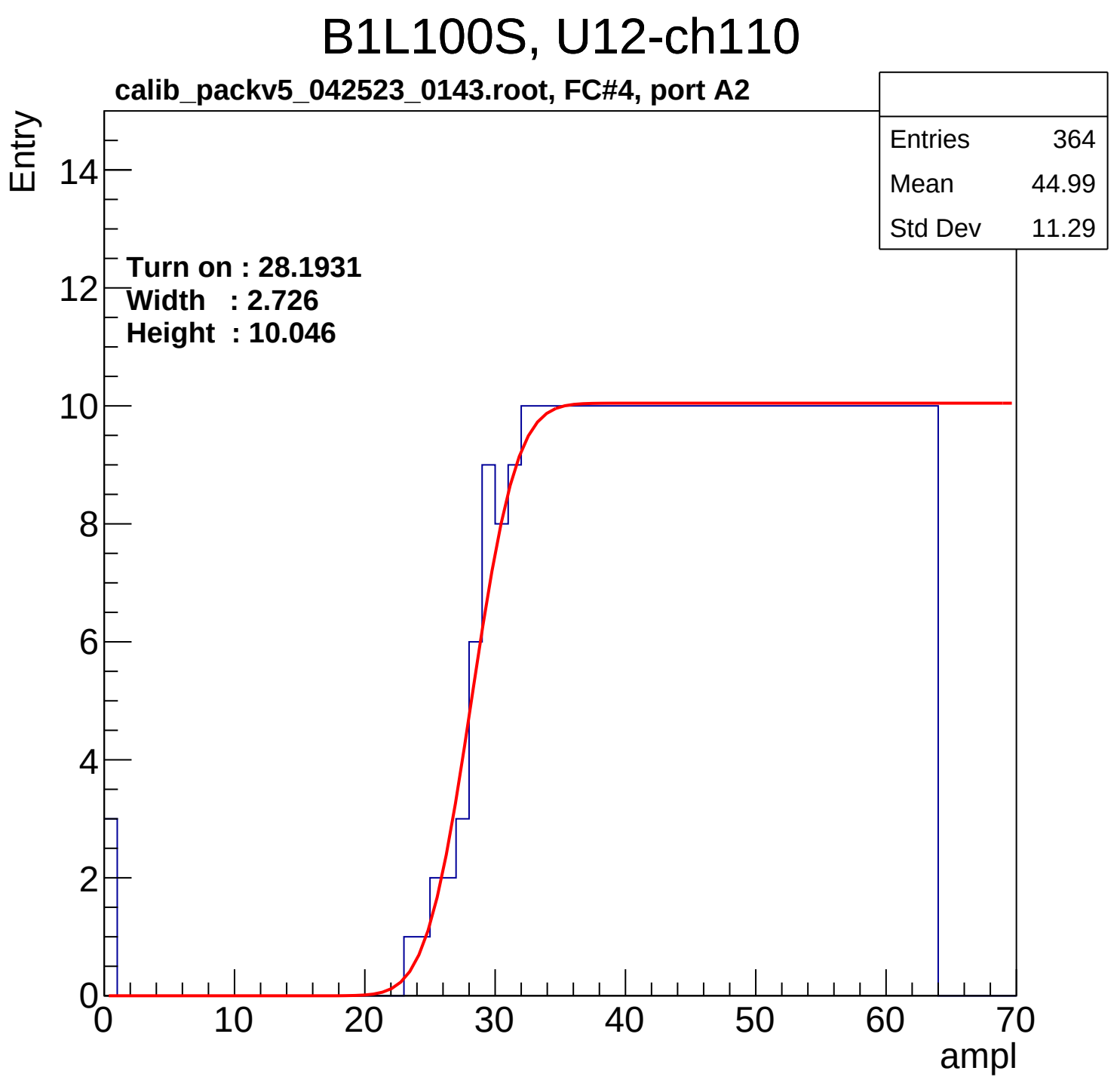

B1L100S, U12-ch105
calib_packv5_042523_0143.root, FC#4, port A2
Entries 360
Mean 45.35
Std Dev 10.94
Turn on : 28.2669
Width : 1.835
Height : 9.969
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

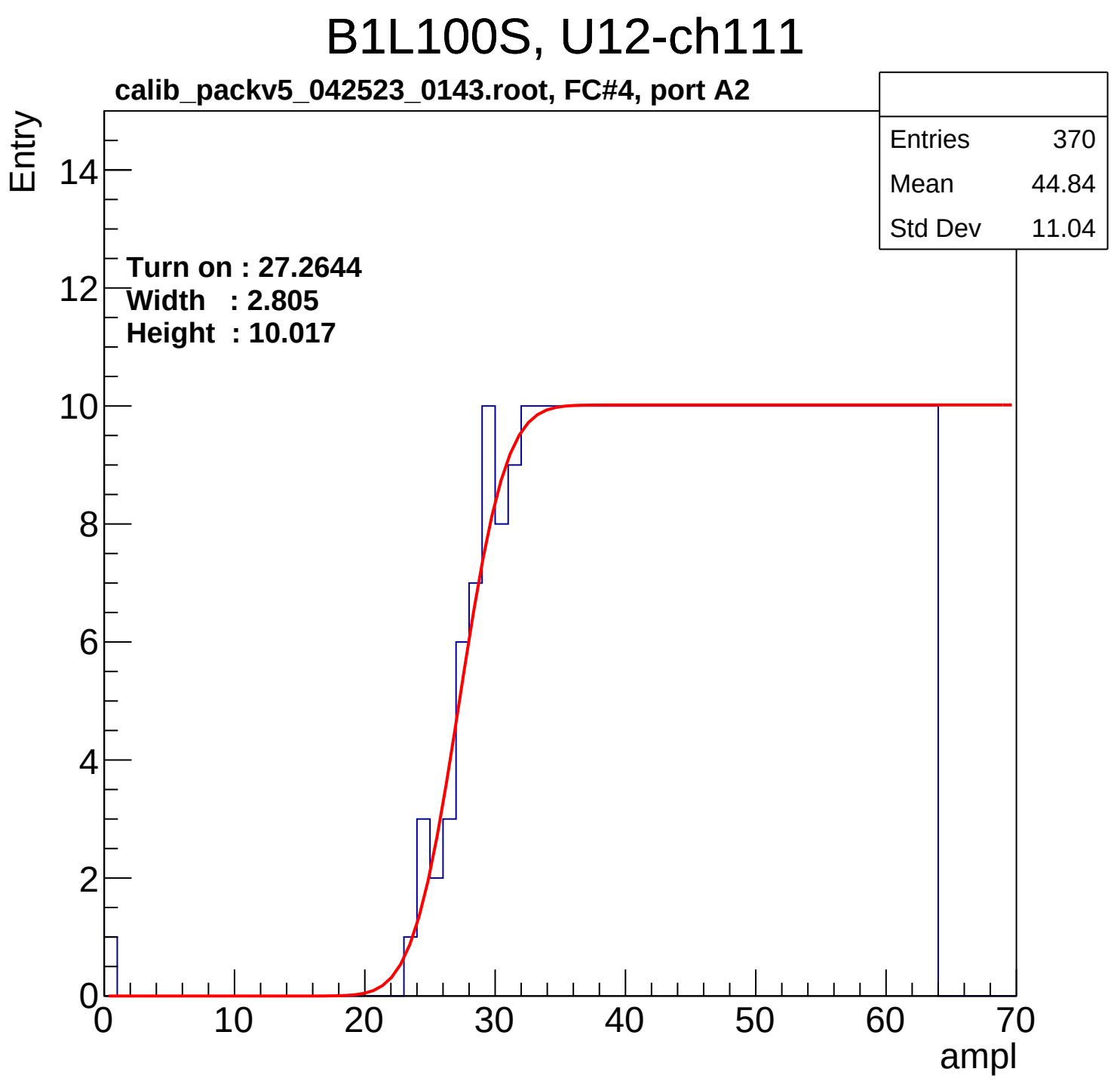

B1L100S, U12-ch106
calib_packv5_042523_0143.root, FC#4, port A2
Entries 353
Mean 45.61
Std Dev 10.8
Turn on : 29.1052
Width : 2.140
Height : 10.001
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

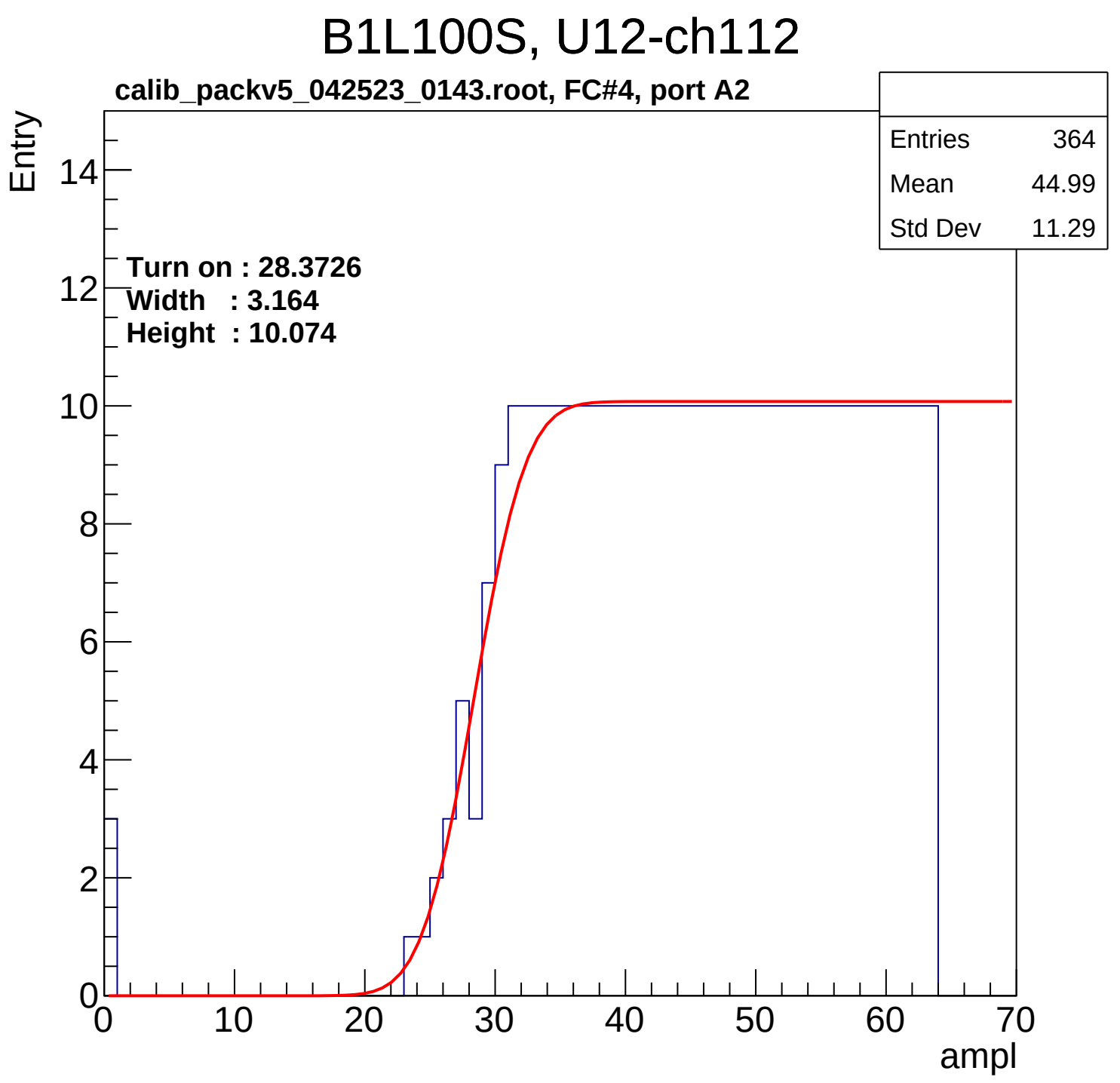

B1L100S, U12-ch107
calib_packv5_042523_0143.root, FC#4, port A2
Entries 369
Mean 44.89
Std Dev 11
Turn on : 27.3202
Width : 2.916
Height : 10.013
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

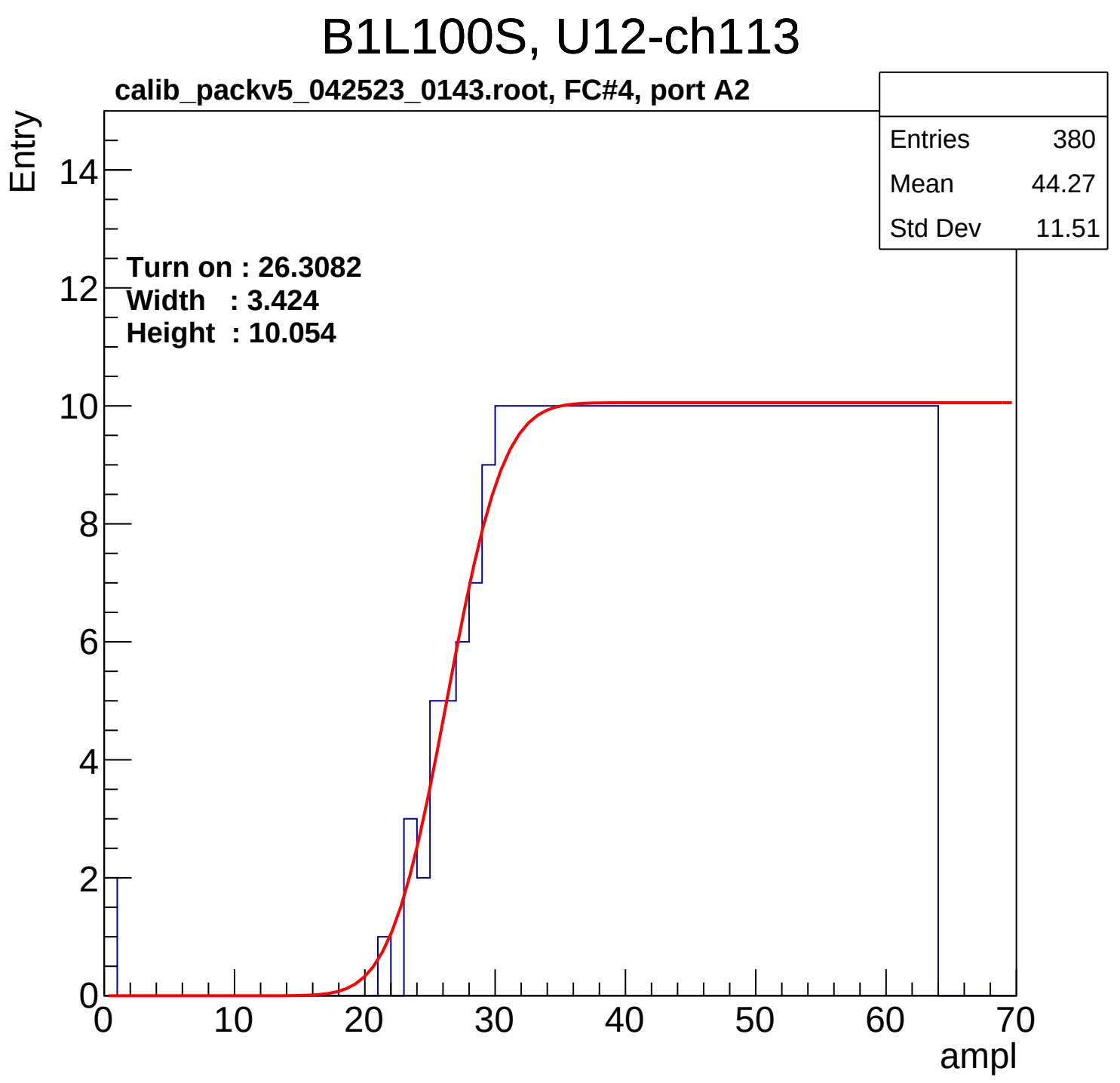

B1L100S, U12-ch108
calib_packv5_042523_0143.root, FC#4, port A2
Entries 372
Mean 44.56
Std Dev 11.56
Turn on : 27.9337
Width : 2.982
Height : 10.065
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

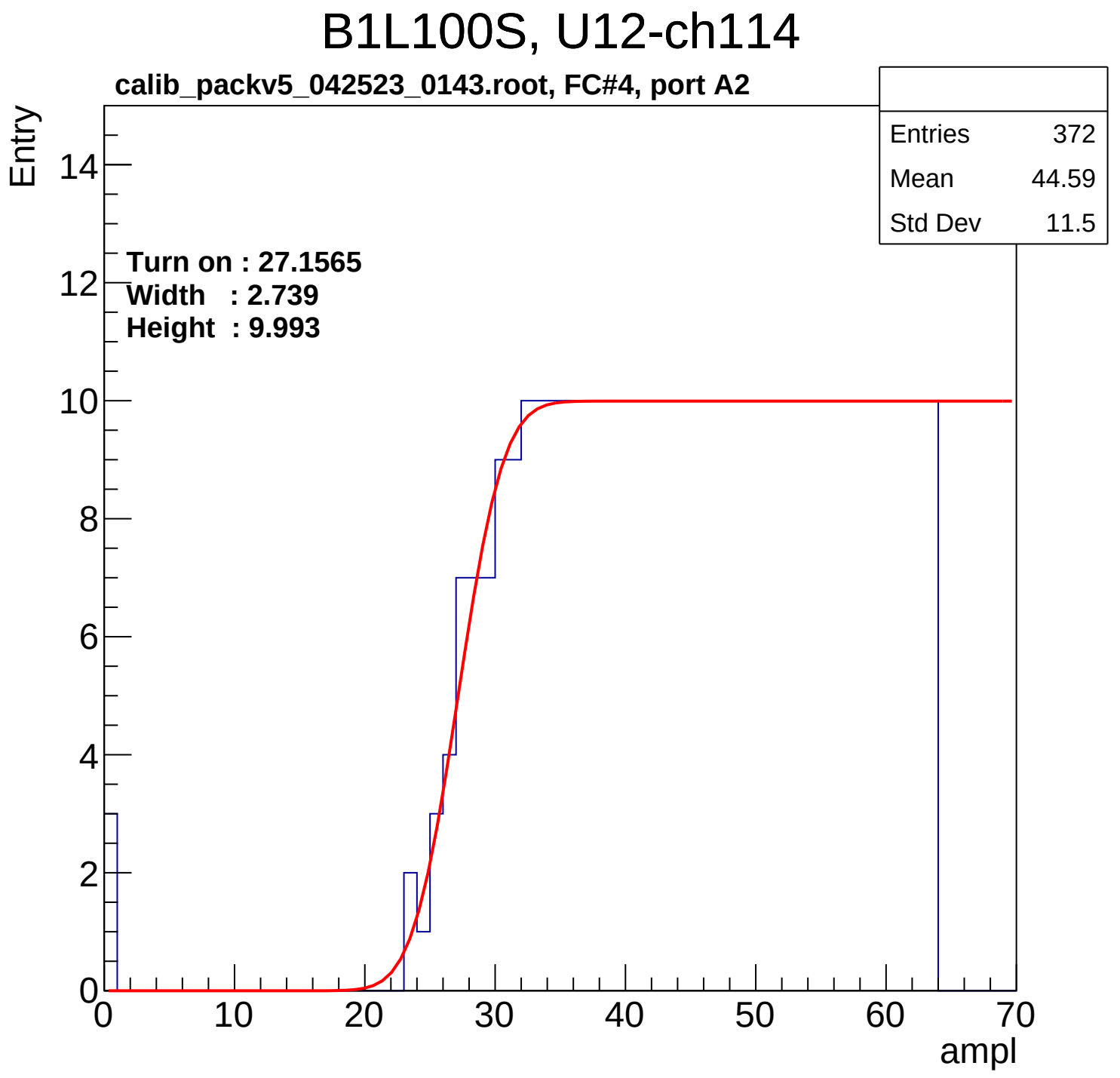

B1L100S, U12-ch109
calib_packv5_042523_0143.root, FC#4, port A2
Entries 354
Mean 45.54
Std Dev 10.85
Turn on : 28.7214
Width : 2.798
Height : 9.995
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

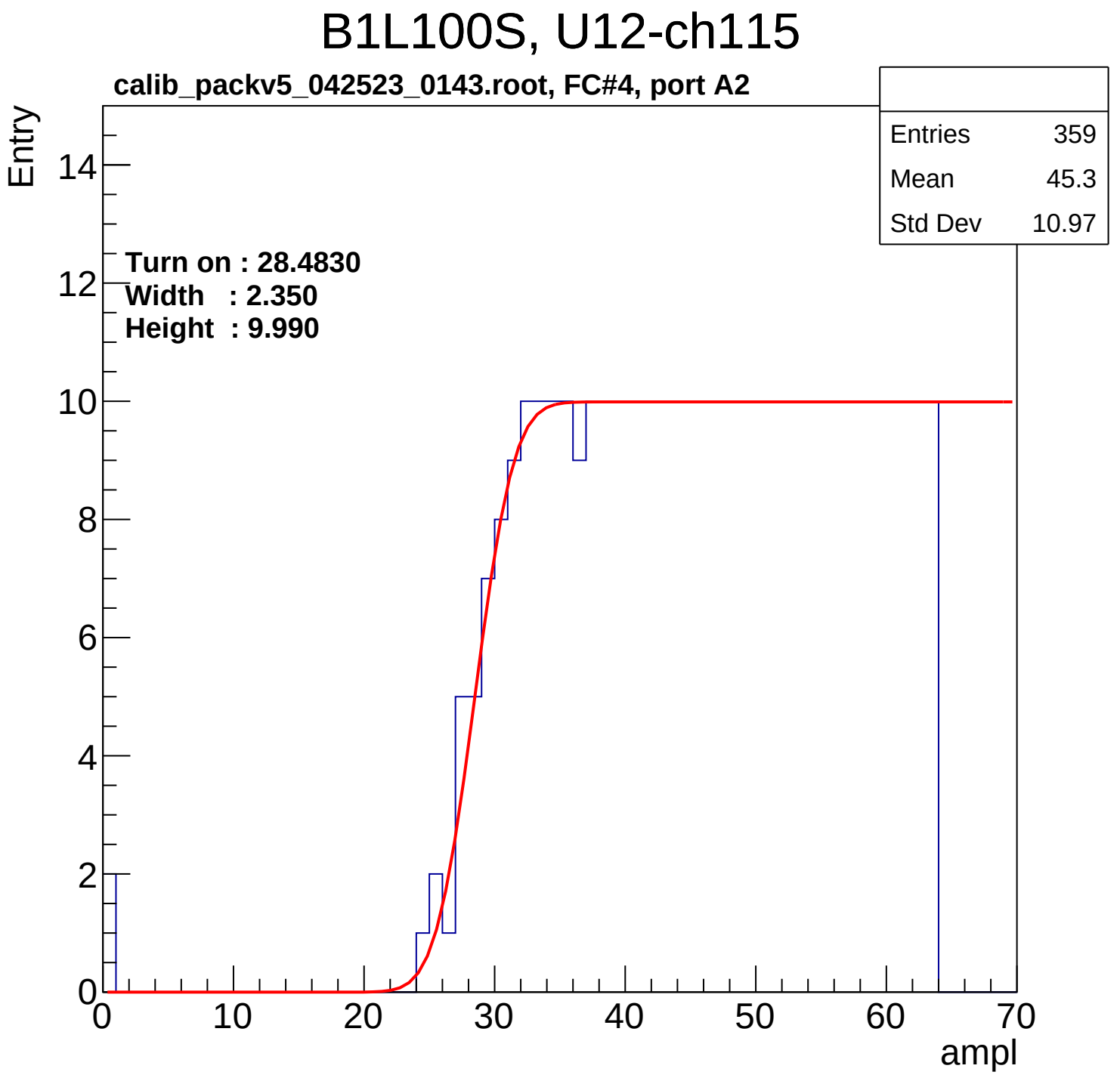

B1L100S, U12-ch110
calib_packv5_042523_0143.root, FC#4, port A2
Entries 364
Mean 44.99
Std Dev 11.29
Turn on : 28.1931
Width : 2.726
Height : 10.046
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

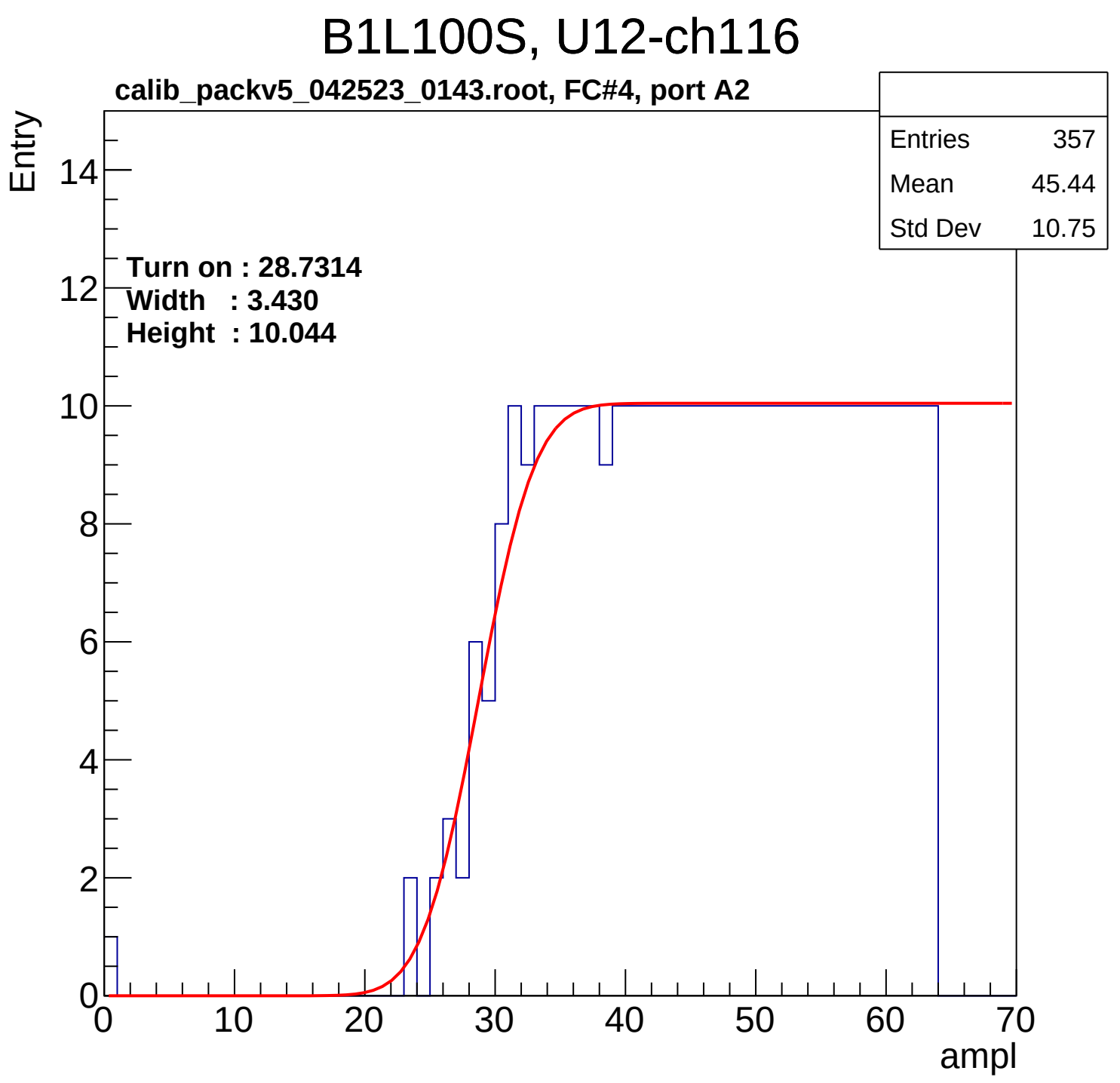

B1L100S, U12-ch111
calib_packv5_042523_0143.root, FC#4, port A2
Entries 370
Mean 44.84
Std Dev 11.04
Turn on : 27.2644
Width : 2.805
Height : 10.017
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

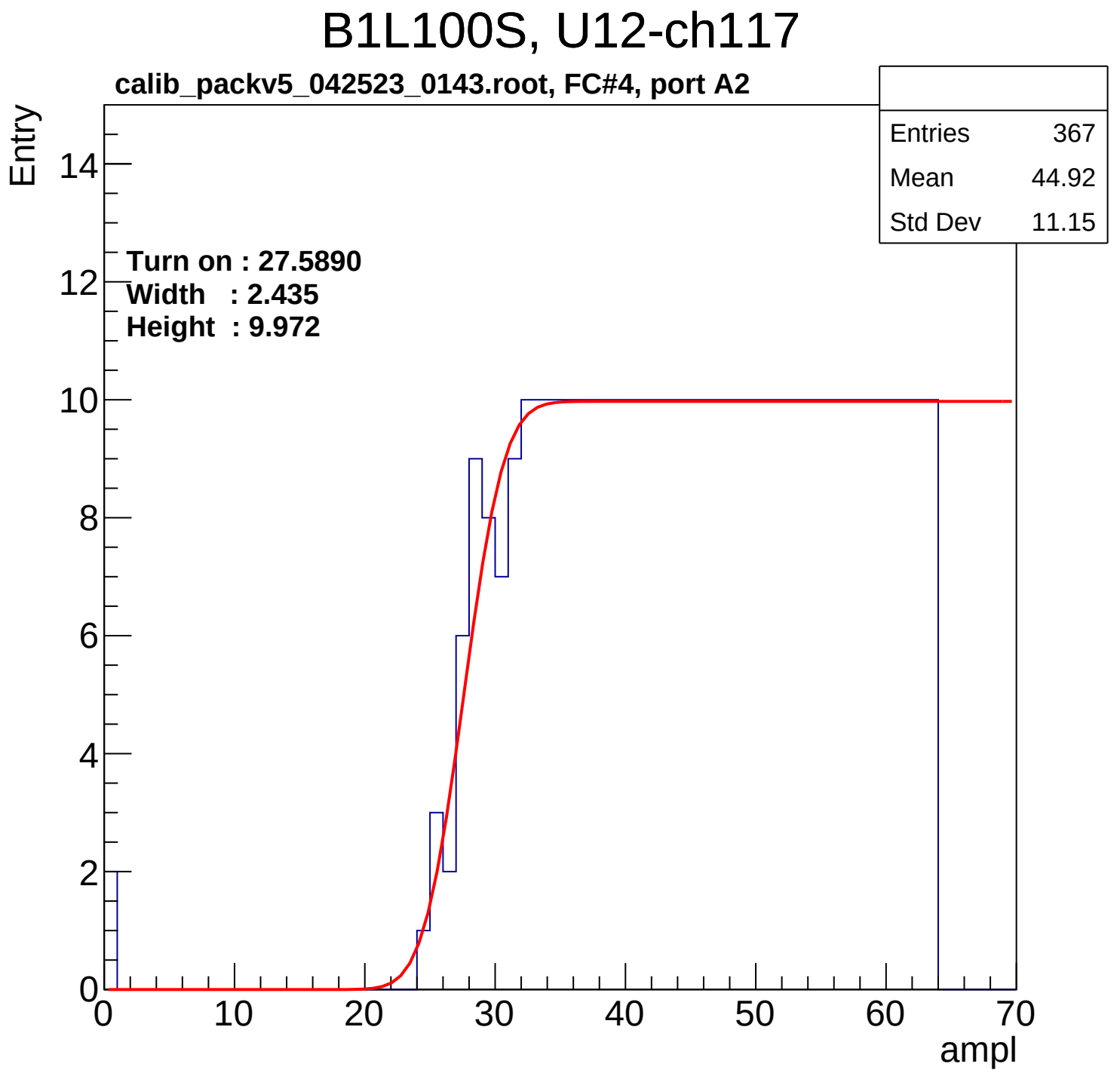

B1L100S, U12-ch112
calib_packv5_042523_0143.root, FC#4, port A2
Entries 364
Mean 44.99
Std Dev 11.29
Turn on : 28.3726
Width : 3.164
Height : 10.074
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

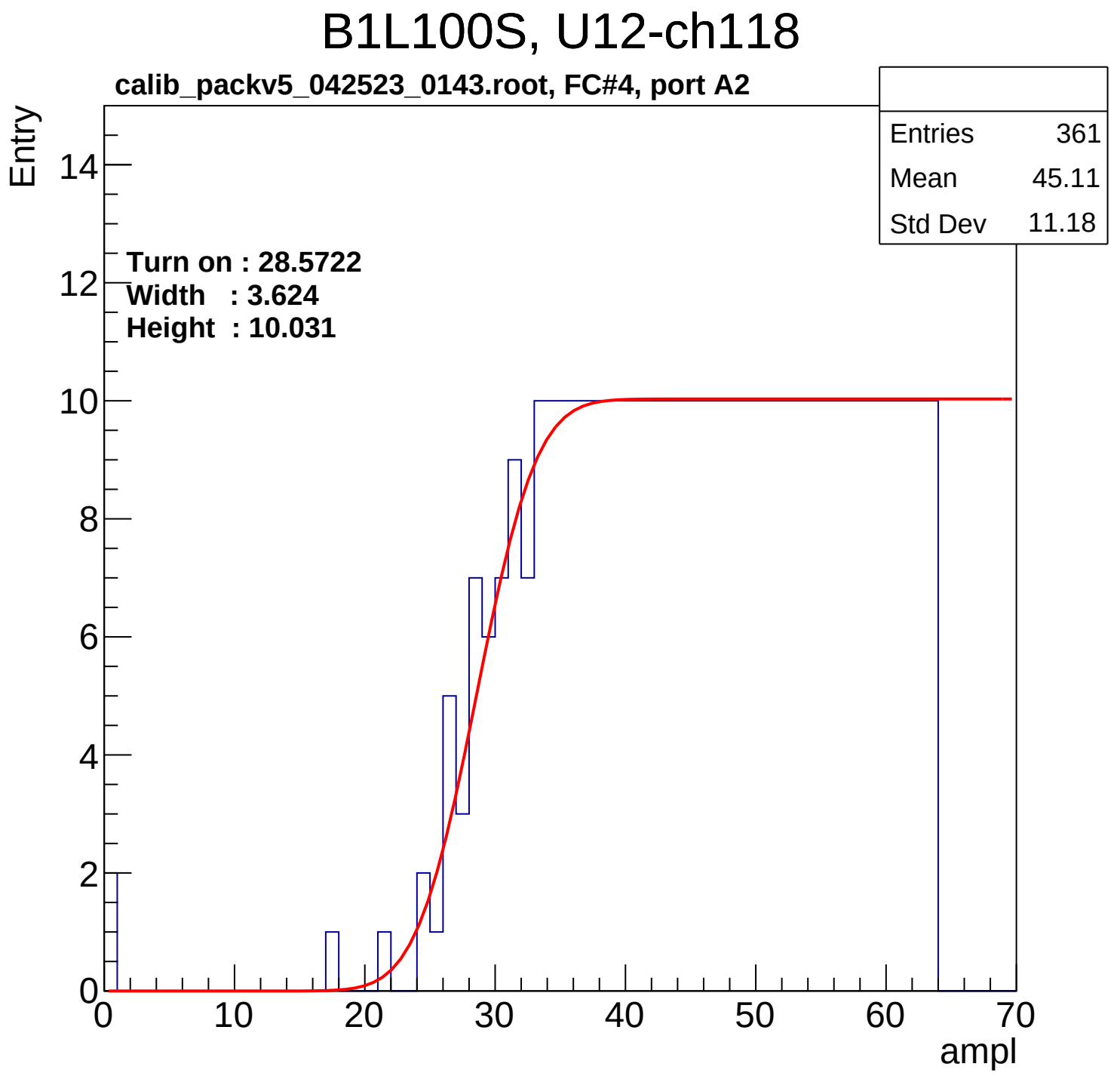

B1L100S, U12-ch113
calib_packv5_042523_0143.root, FC#4, port A2
Entries 380
Mean 44.27
Std Dev 11.51
Turn on : 26.3082
Width : 3.424
Height : 10.054
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

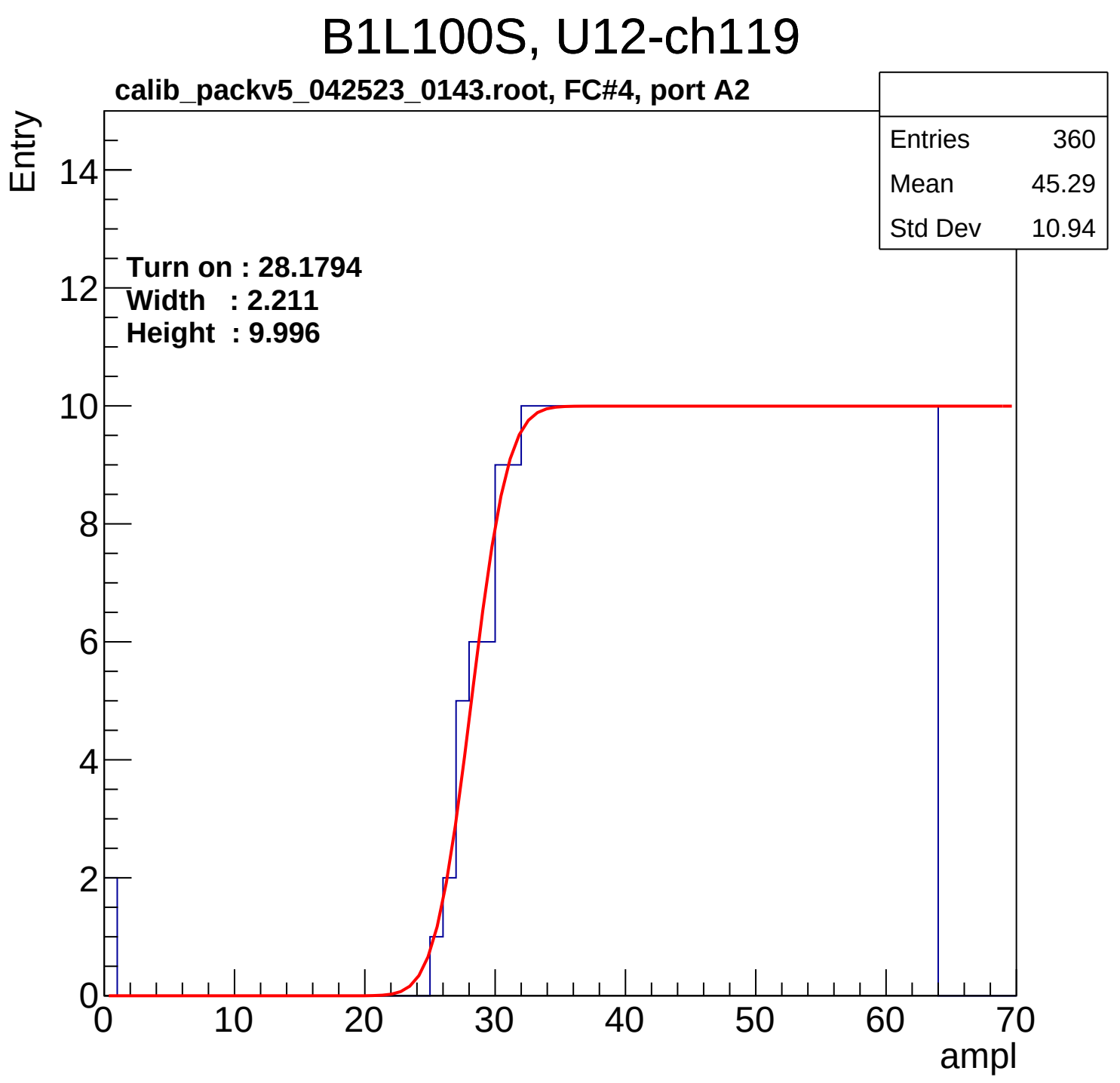

B1L100S, U12-ch114
calib_packv5_042523_0143.root, FC#4, port A2
Entries 372
Mean 44.59
Std Dev 11.5
Turn on : 27.1565
Width : 2.739
Height : 9.993
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

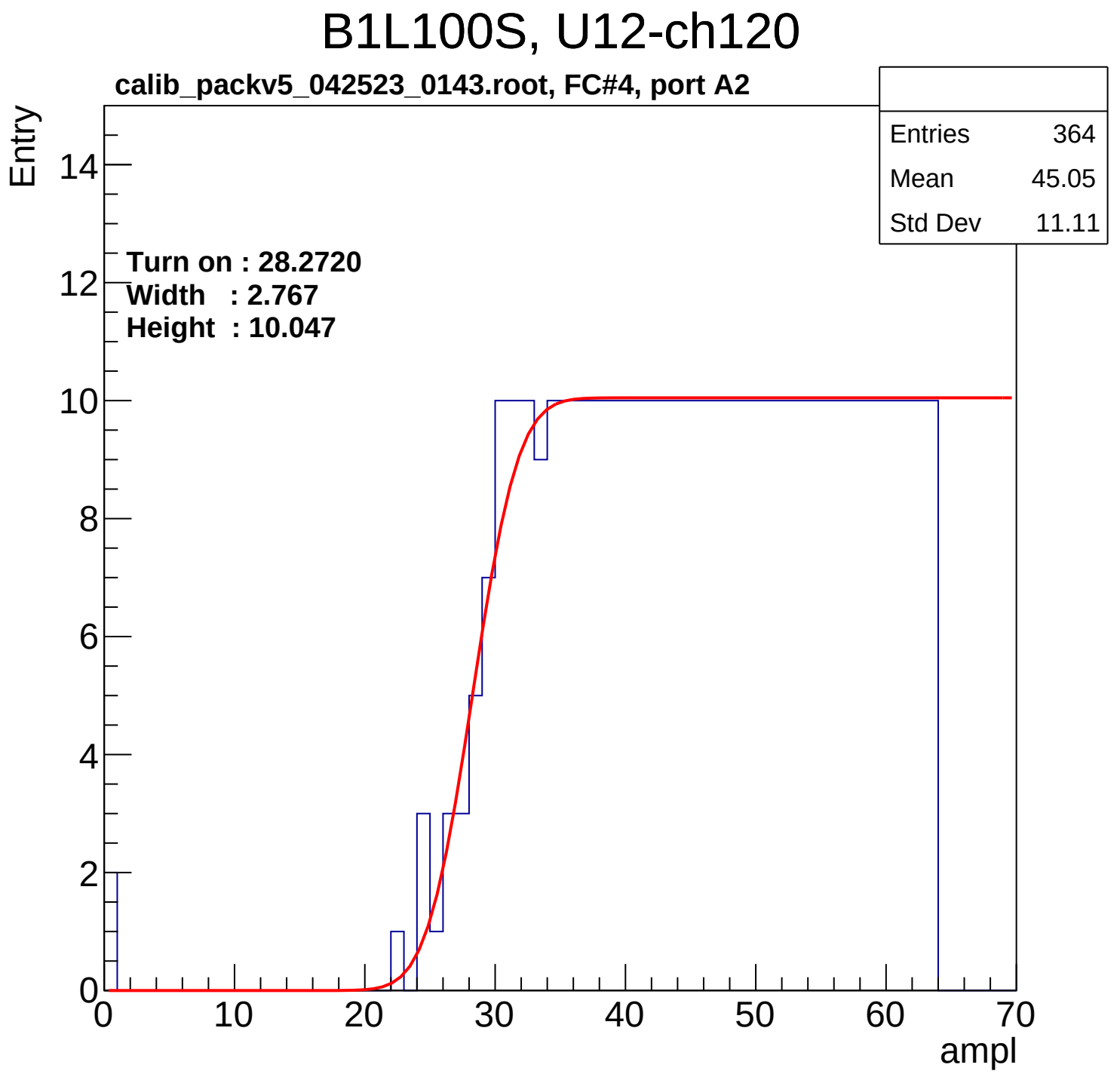

B1L100S, U12-ch115
calib_packv5_042523_0143.root, FC#4, port A2
Entries 359
Mean 45.3
Std Dev 10.97
Turn on : 28.4830
Width : 2.350
Height : 9.990
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

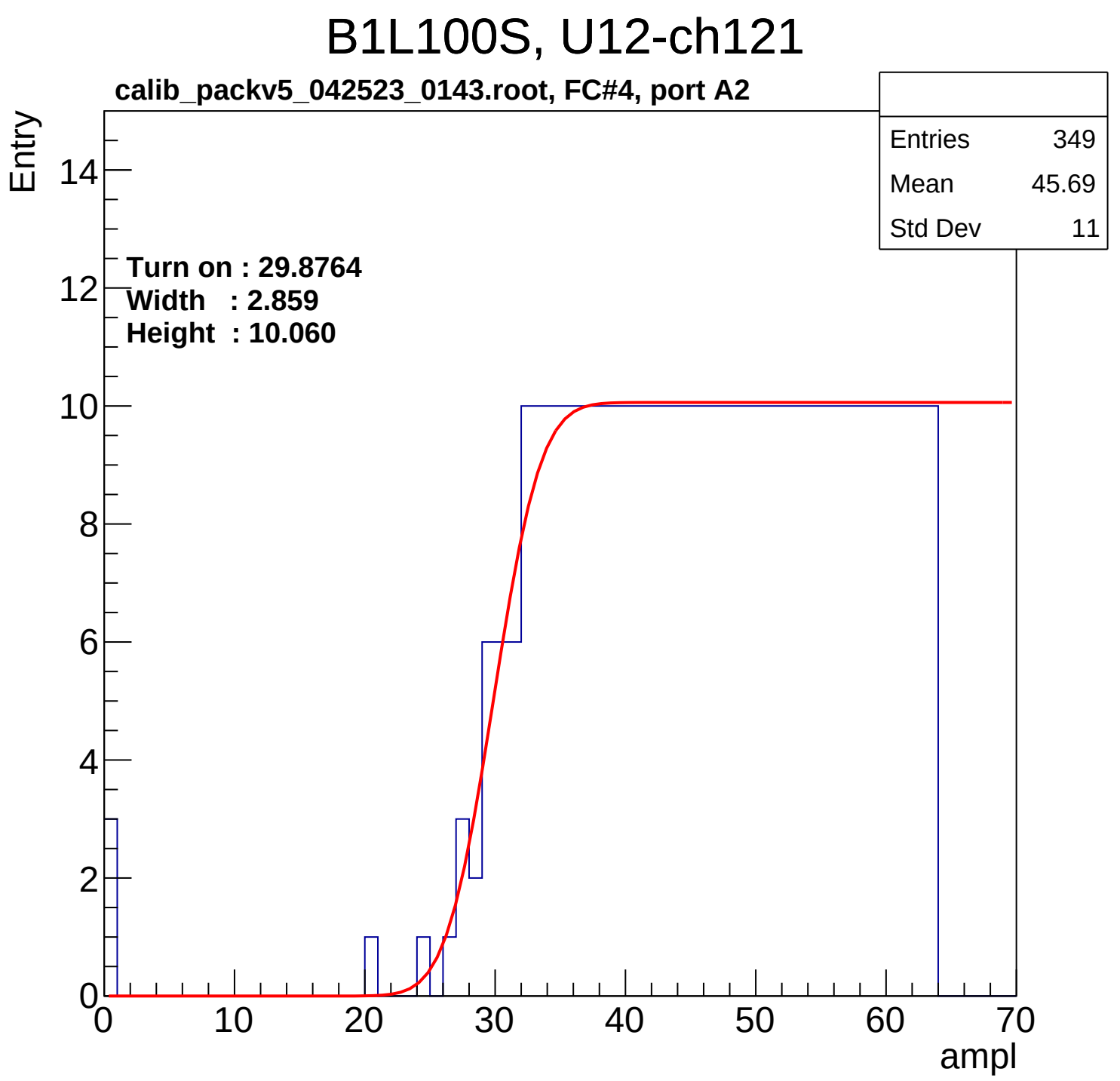

B1L100S, U12-ch116
calib_packv5_042523_0143.root, FC#4, port A2
Entries 357
Mean 45.44
Std Dev 10.75
Turn on : 28.7314
Width : 3.430
Height : 10.044
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

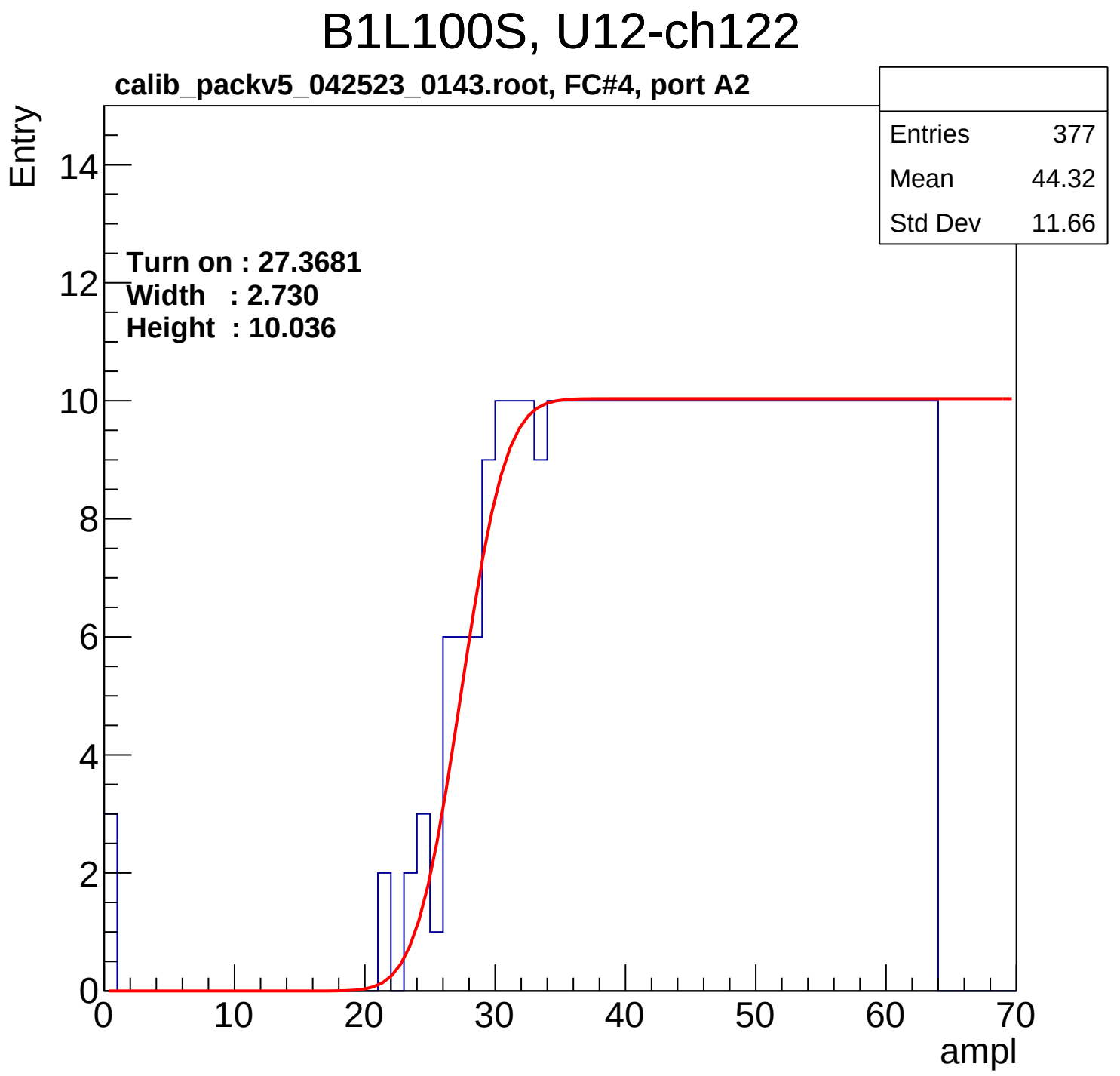

B1L100S, U12-ch117
calib_packv5_042523_0143.root, FC#4, port A2
Entries 367
Mean 44.92
Std Dev 11.15
Turn on : 27.5890
Width : 2.435
Height : 9.972
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

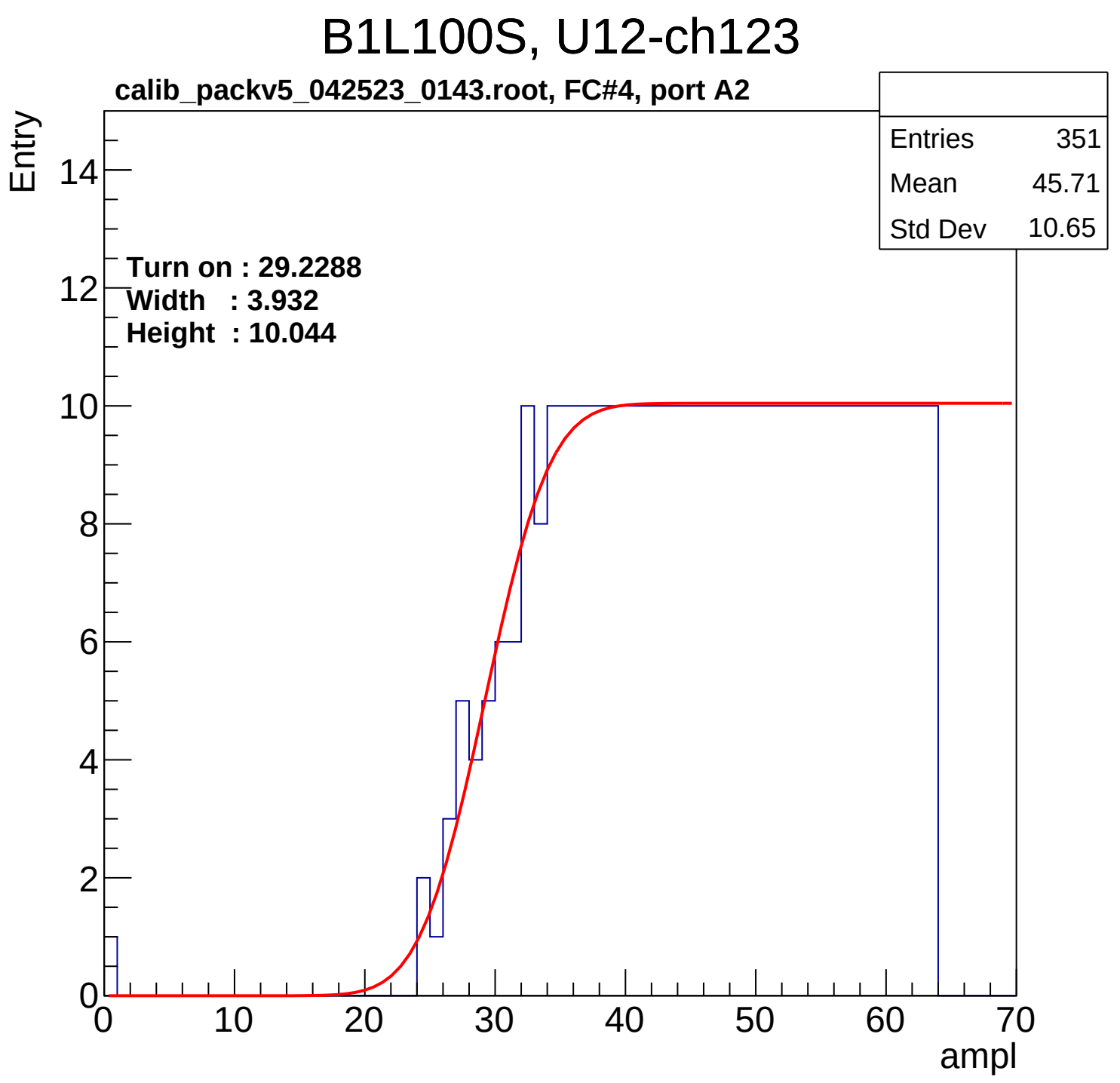

B1L100S, U12-ch118
calib_packv5_042523_0143.root, FC#4, port A2
Entries 361
Mean 45.11
Std Dev 11.18
Turn on : 28.5722
Width : 3.624
Height : 10.031
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

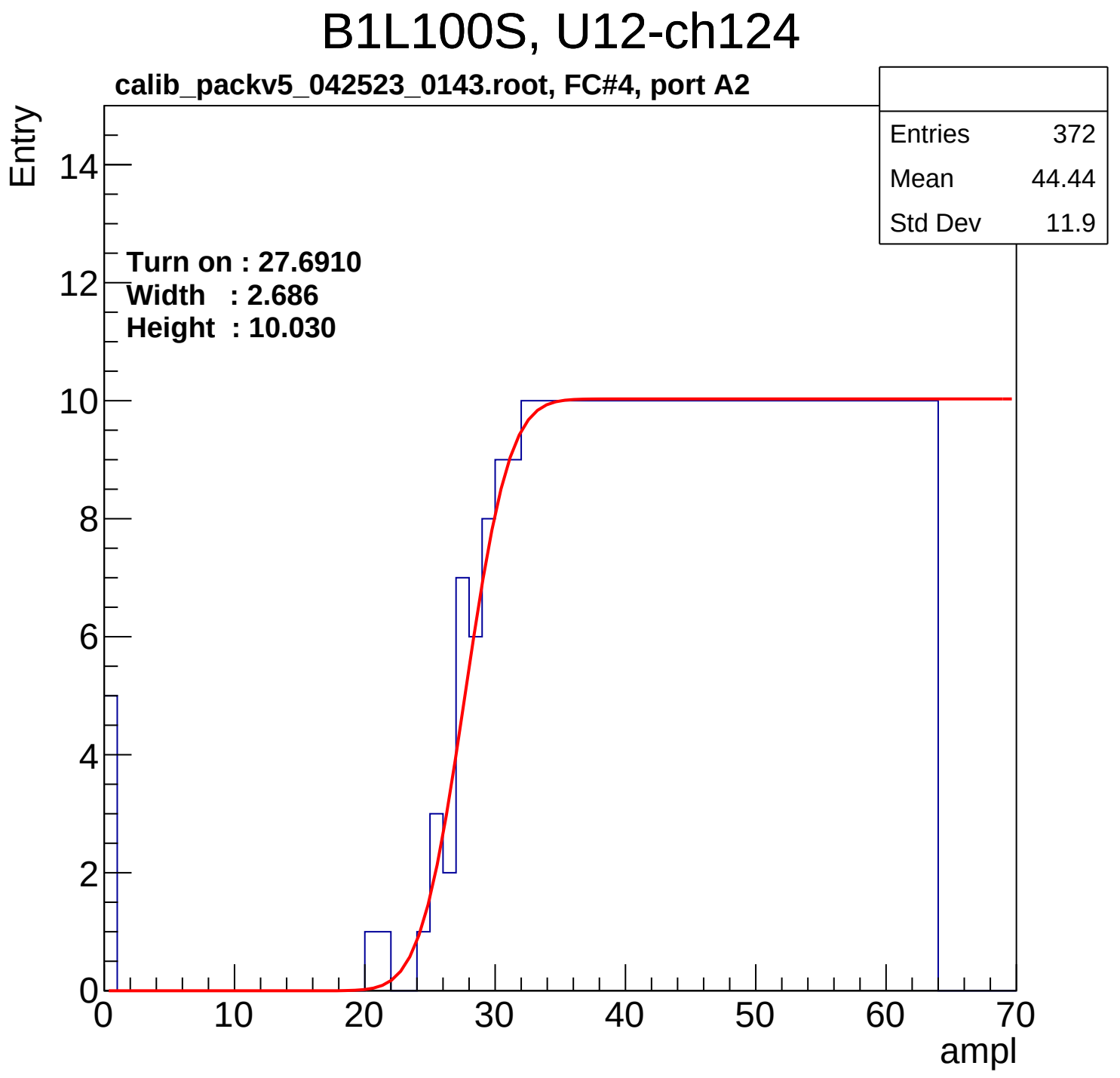

B1L100S, U12-ch119
calib_packv5_042523_0143.root, FC#4, port A2
Entries 360
Mean 45.29
Std Dev 10.94
Turn on : 28.1794
Width : 2.211
Height : 9.996
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

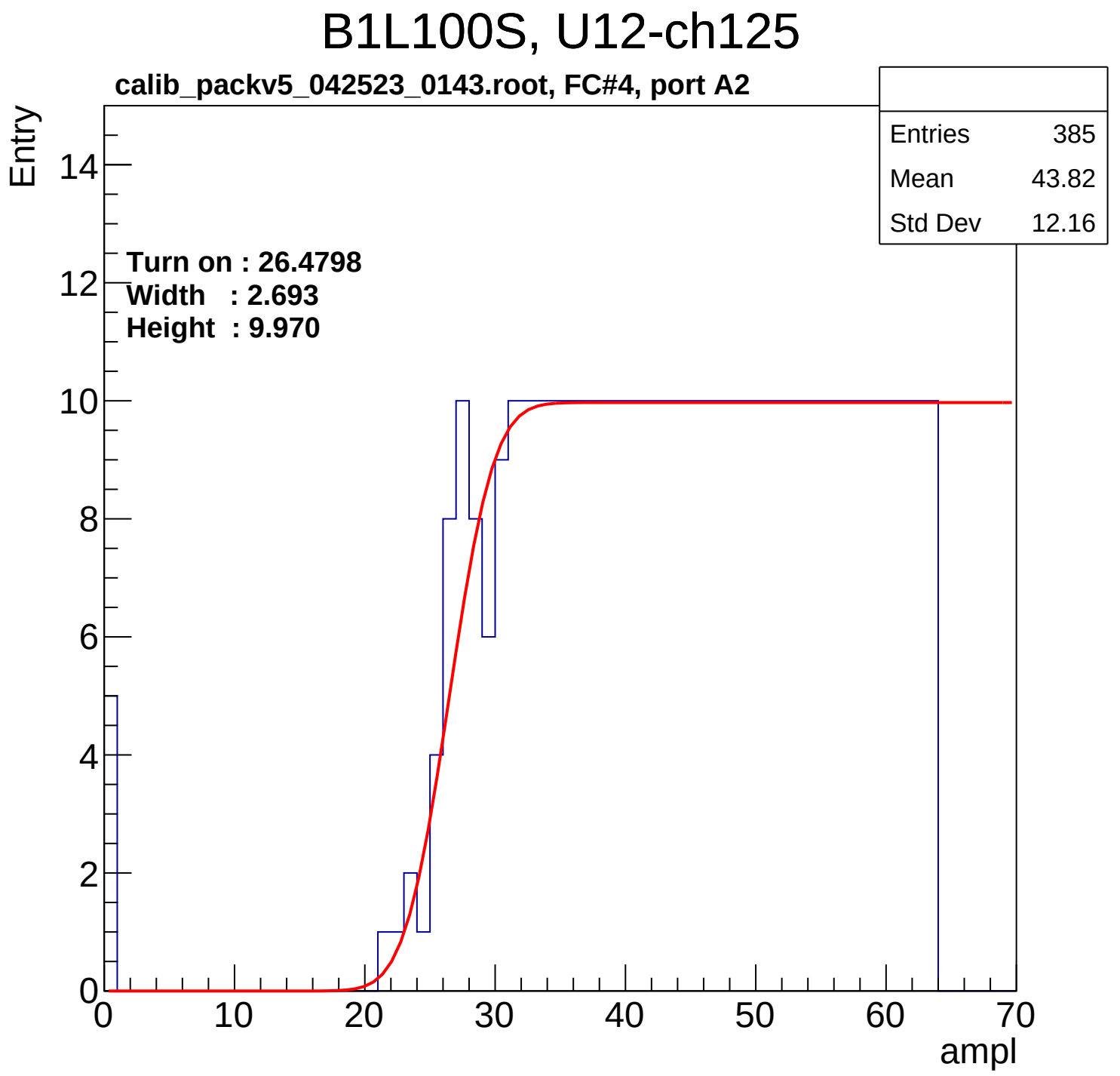

B1L100S, U12-ch120
calib_packv5_042523_0143.root, FC#4, port A2
Entries 364
Mean 45.05
Std Dev 11.11
Turn on : 28.2720
Width : 2.767
Height : 10.047
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

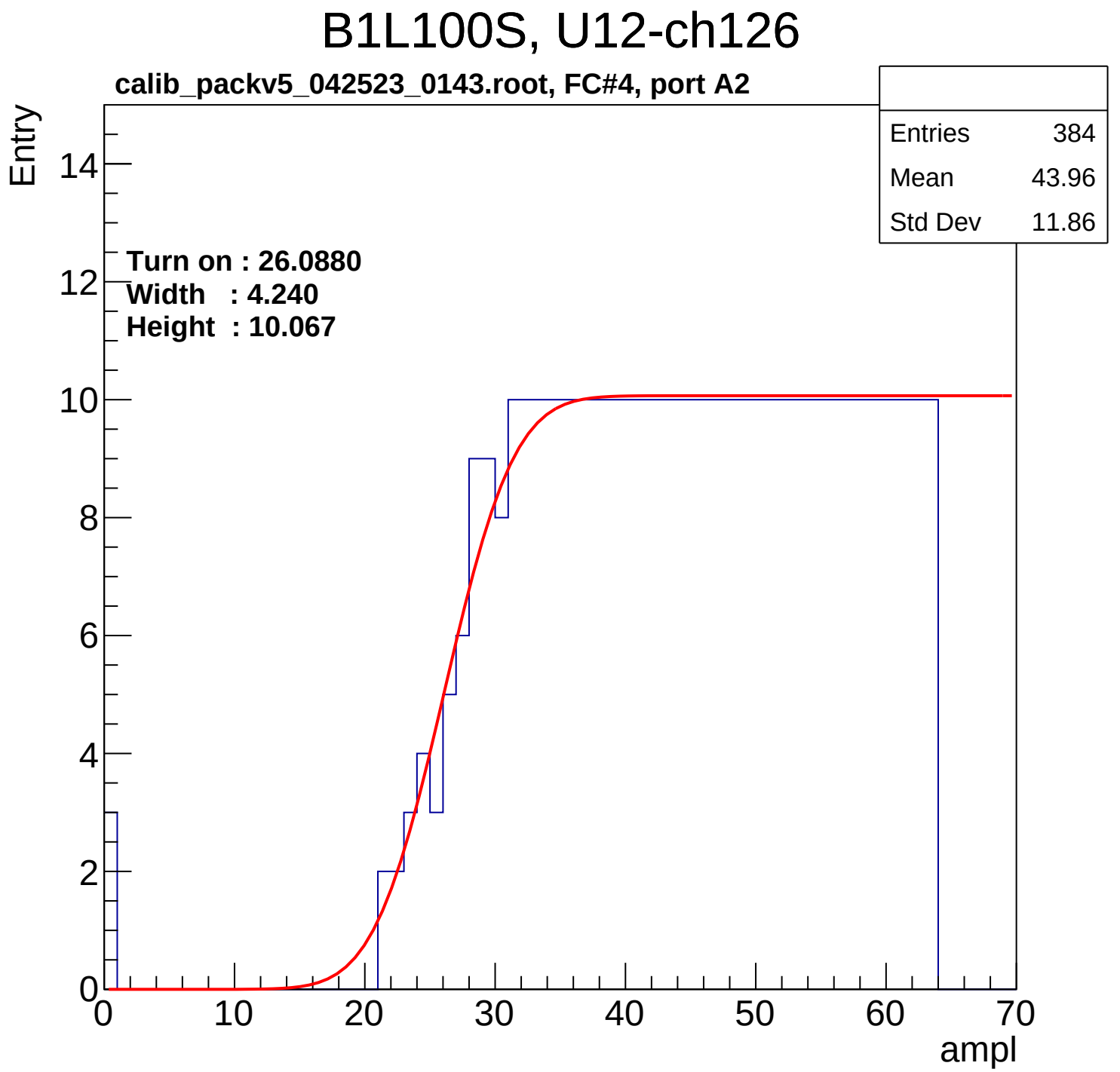

B1L100S, U12-ch121
calib_packv5_042523_0143.root, FC#4, port A2
Entries 349
Mean 45.69
Std Dev 11
Turn on : 29.8764
Width : 2.859
Height : 10.060
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

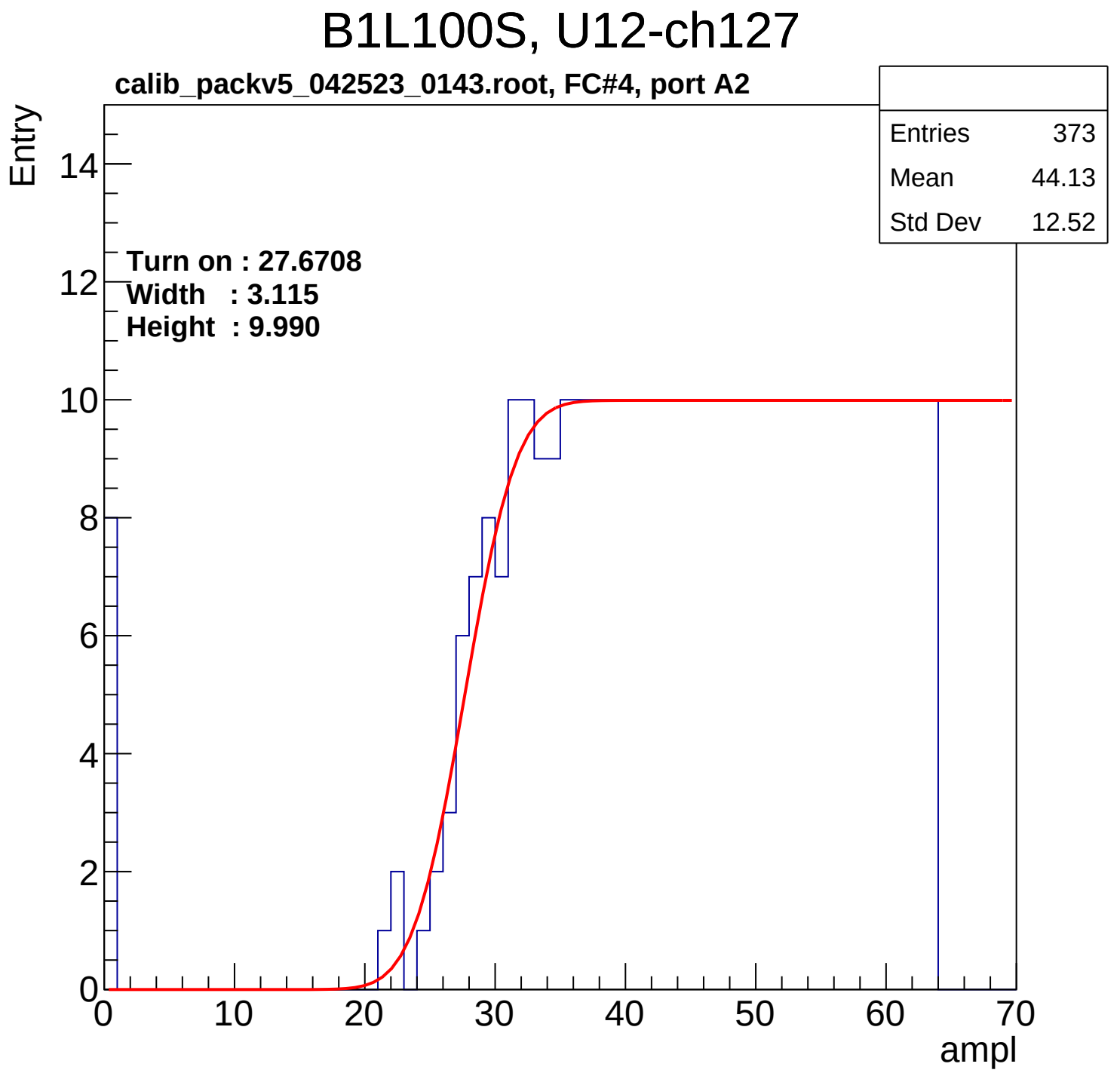

B1L100S, U12-ch122
calib_packv5_042523_0143.root, FC#4, port A2
Entries 377
Mean 44.32
Std Dev 11.66
Turn on : 27.3681
Width : 2.730
Height : 10.036
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

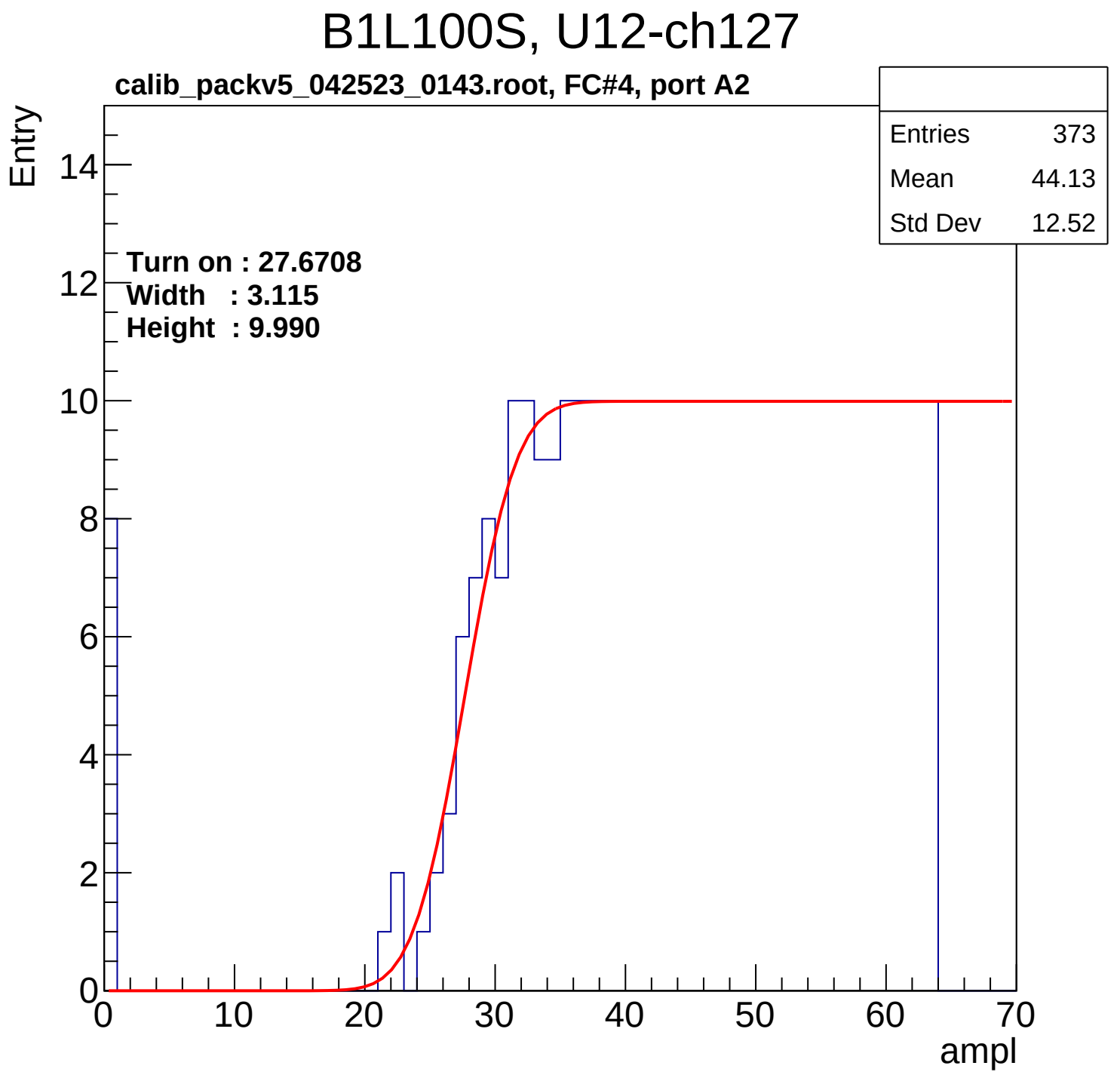

B1L100S, U12-ch123
calib_packv5_042523_0143.root, FC#4, port A2
Entries 351
Mean 45.71
Std Dev 10.65
Turn on : 29.2288
Width : 3.932
Height : 10.044
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L100S, U12-ch124
calib_packv5_042523_0143.root, FC#4, port A2
Entries 372
Mean 44.44
Std Dev 11.9
Turn on : 27.6910
Width : 2.686
Height : 10.030
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L100S, U12-ch125
calib_packv5_042523_0143.root, FC#4, port A2
Entries 385
Mean 43.82
Std Dev 12.16
Turn on : 26.4798
Width : 2.693
Height : 9.970
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L100S, U12-ch126
calib_packv5_042523_0143.root, FC#4, port A2
Entries 384
Mean 43.96
Std Dev 11.86
Turn on : 26.0880
Width : 4.240
Height : 10.067
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L100S, U12-ch127
calib_packv5_042523_0143.root, FC#4, port A2
Entries 373
Mean 44.13
Std Dev 12.52
Turn on : 27.6708
Width : 3.115
Height : 9.990
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L100S, U12-ch127
calib_packv5_042523_0143.root, FC#4, port A2
Entries 373
Mean 44.13
Std Dev 12.52
Turn on : 27.6708
Width : 3.115
Height : 9.990
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70