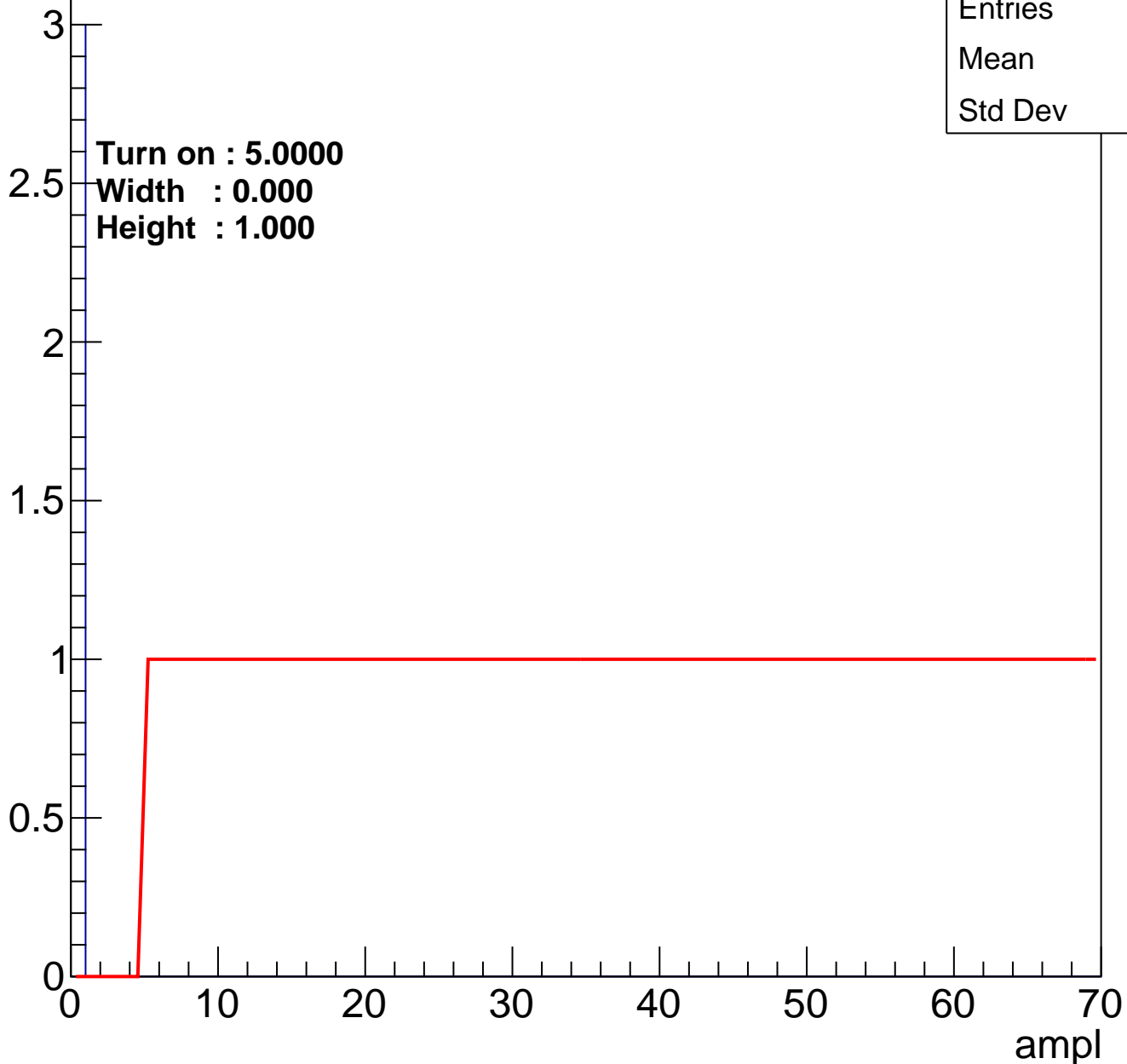


B1L001S, U12-ch0

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	3
Mean	0
Std Dev	0

B1L001S, U12-ch1

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	0
Mean	0
Std Dev	0

B1L001S, U12-ch2

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	2
Mean	0
Std Dev	0

B1L001S, U12-ch3

calib_packv5_042523_0143.root, FC#2, port C2

Entry



B1L001S, U12-ch4

calib_packv5_042523_0143.root, FC#2, port C2

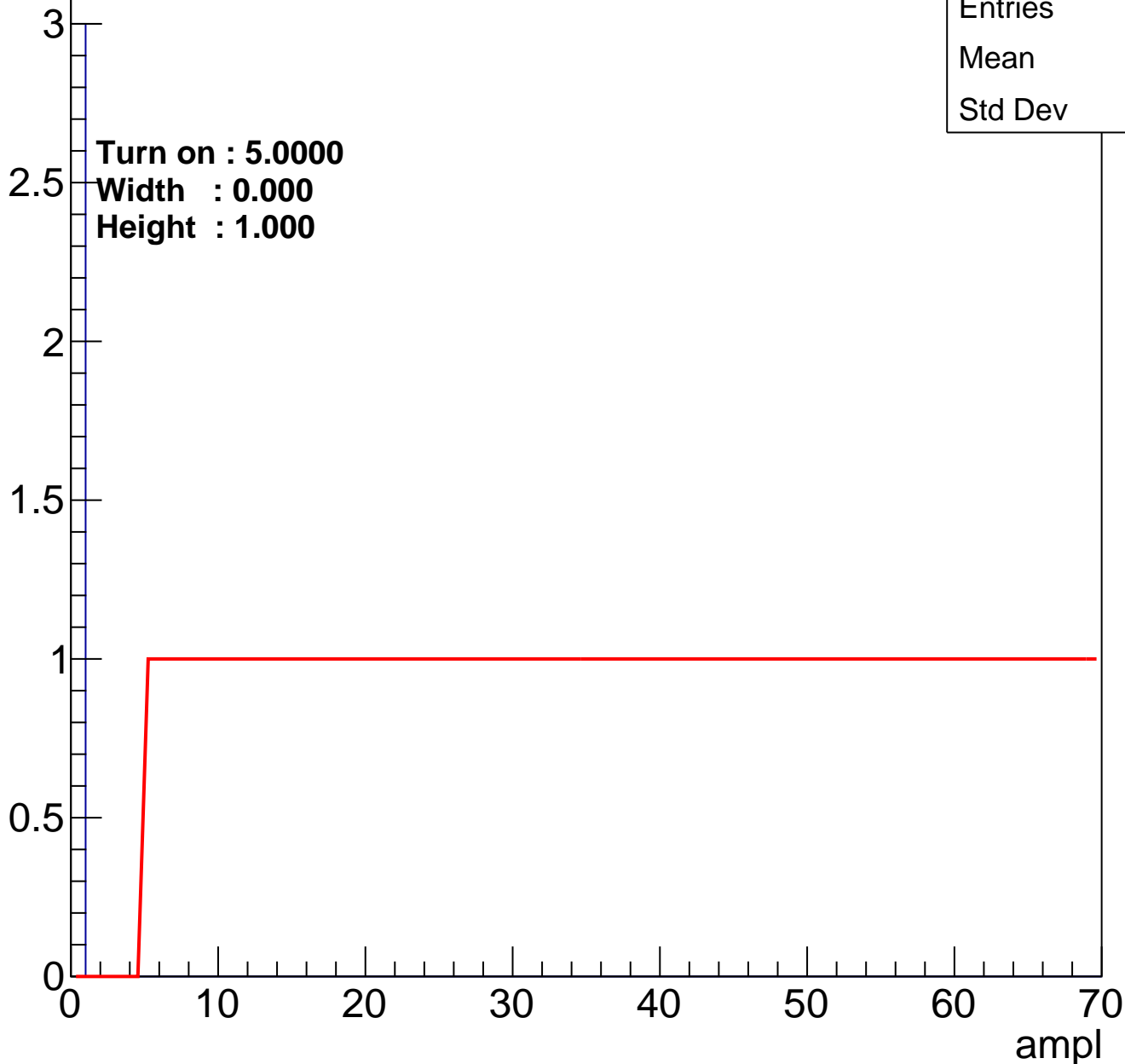
Entry



B1L001S, U12-ch5

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	3
Mean	0
Std Dev	0

B1L001S, U12-ch6

calib_packv5_042523_0143.root, FC#2, port C2

Entry



B1L001S, U12-ch7

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	0
Mean	0
Std Dev	0

B1L001S, U12-ch8

calib_packv5_042523_0143.root, FC#2, port C2

Entry

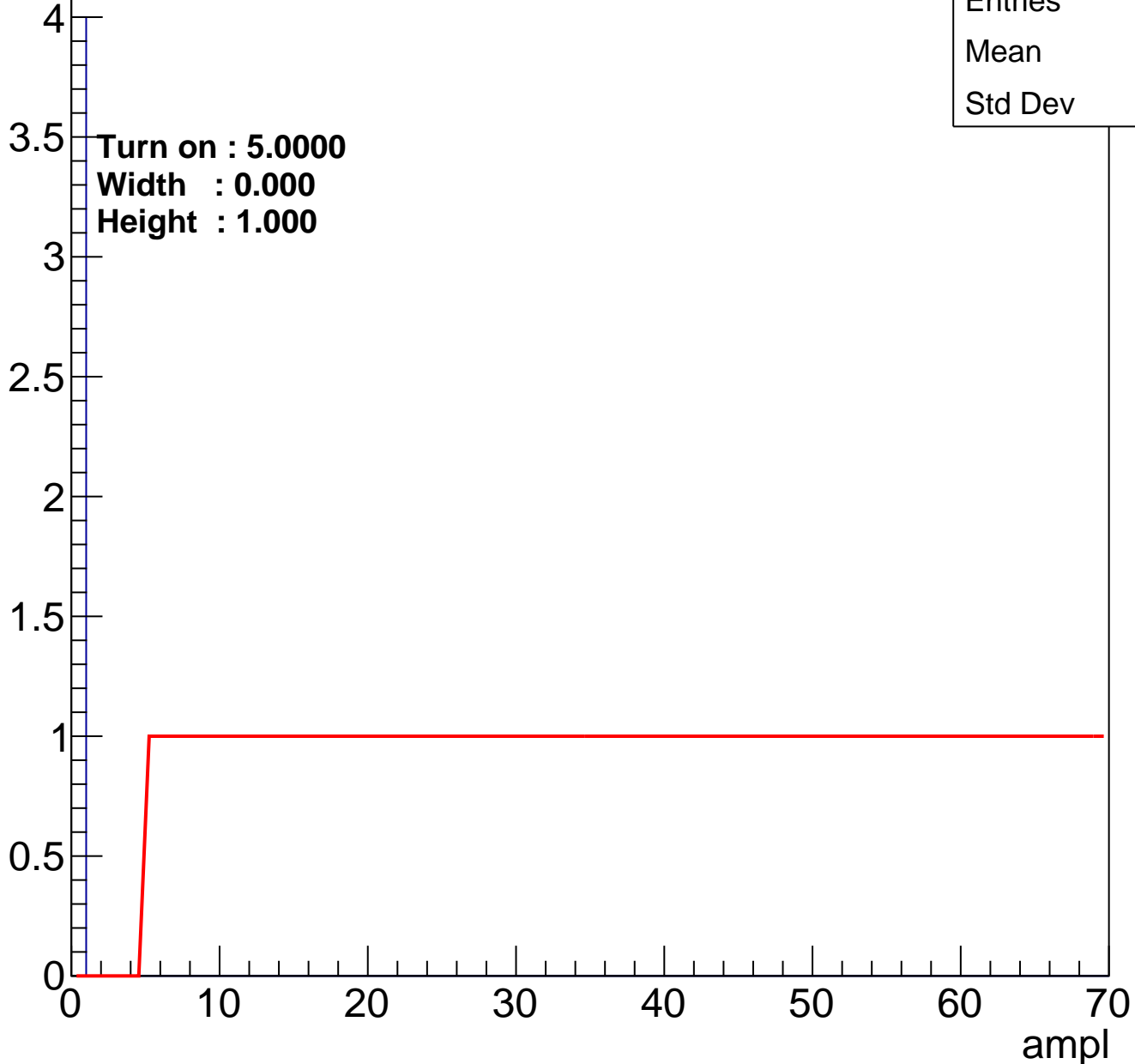


Entries	2
Mean	0
Std Dev	0

B1L001S, U12-ch9

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	4
Mean	0
Std Dev	0

B1L001S, U12-ch10

calib_packv5_042523_0143.root, FC#2, port C2

Entry

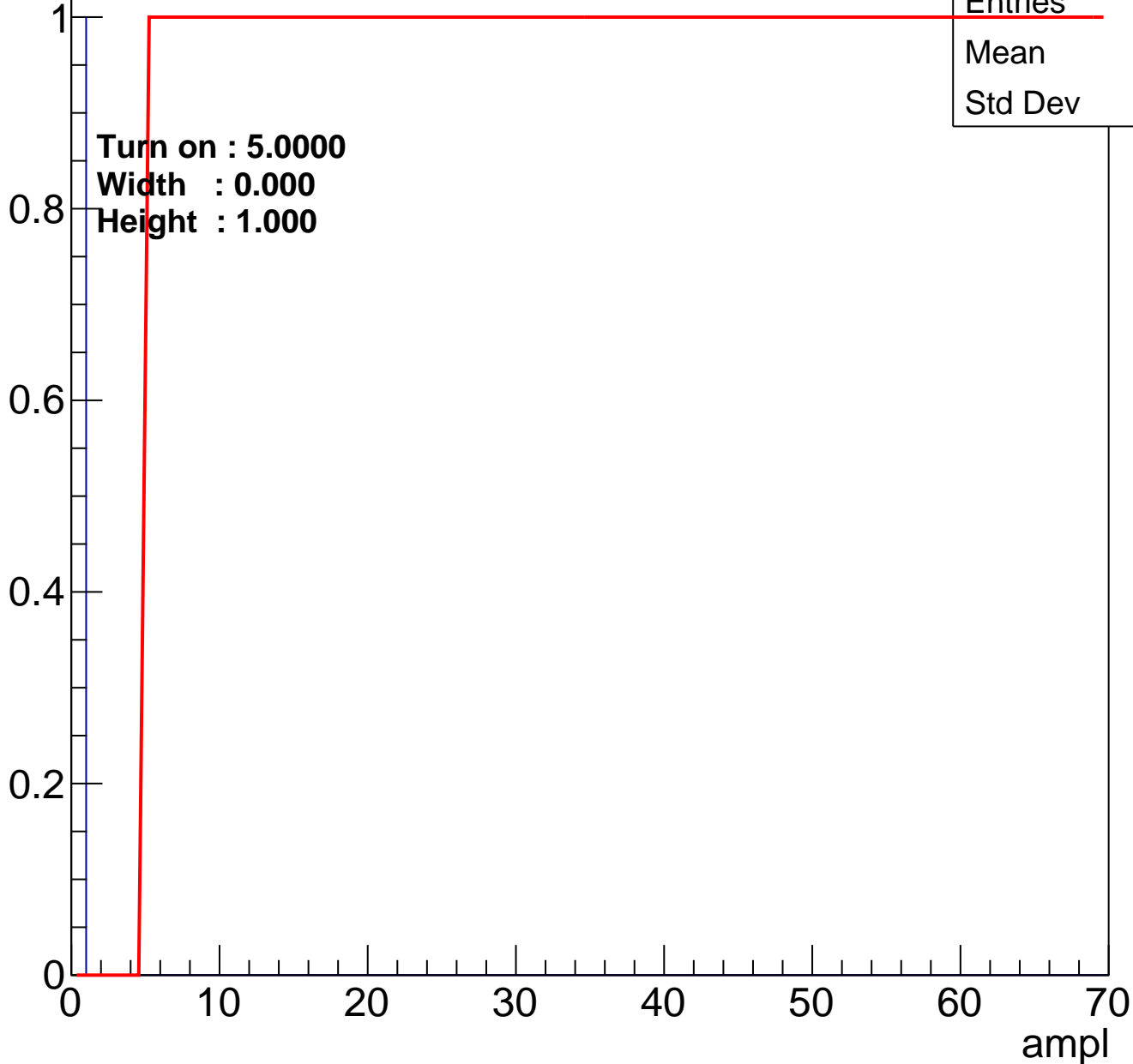


Entries	0
Mean	0
Std Dev	0

B1L001S, U12-ch11

calib_packv5_042523_0143.root, FC#2, port C2

Entry



B1L001S, U12-ch12

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	0
Mean	0
Std Dev	0

B1L001S, U12-ch13

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	1
Mean	0
Std Dev	0

B1L001S, U12-ch14

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	2
Mean	0
Std Dev	0

B1L001S, U12-ch15

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	0
Mean	0
Std Dev	0

B1L001S, U12-ch16

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	2
Mean	0
Std Dev	0

B1L001S, U12-ch17

calib_packv5_042523_0143.root, FC#2, port C2

Entry

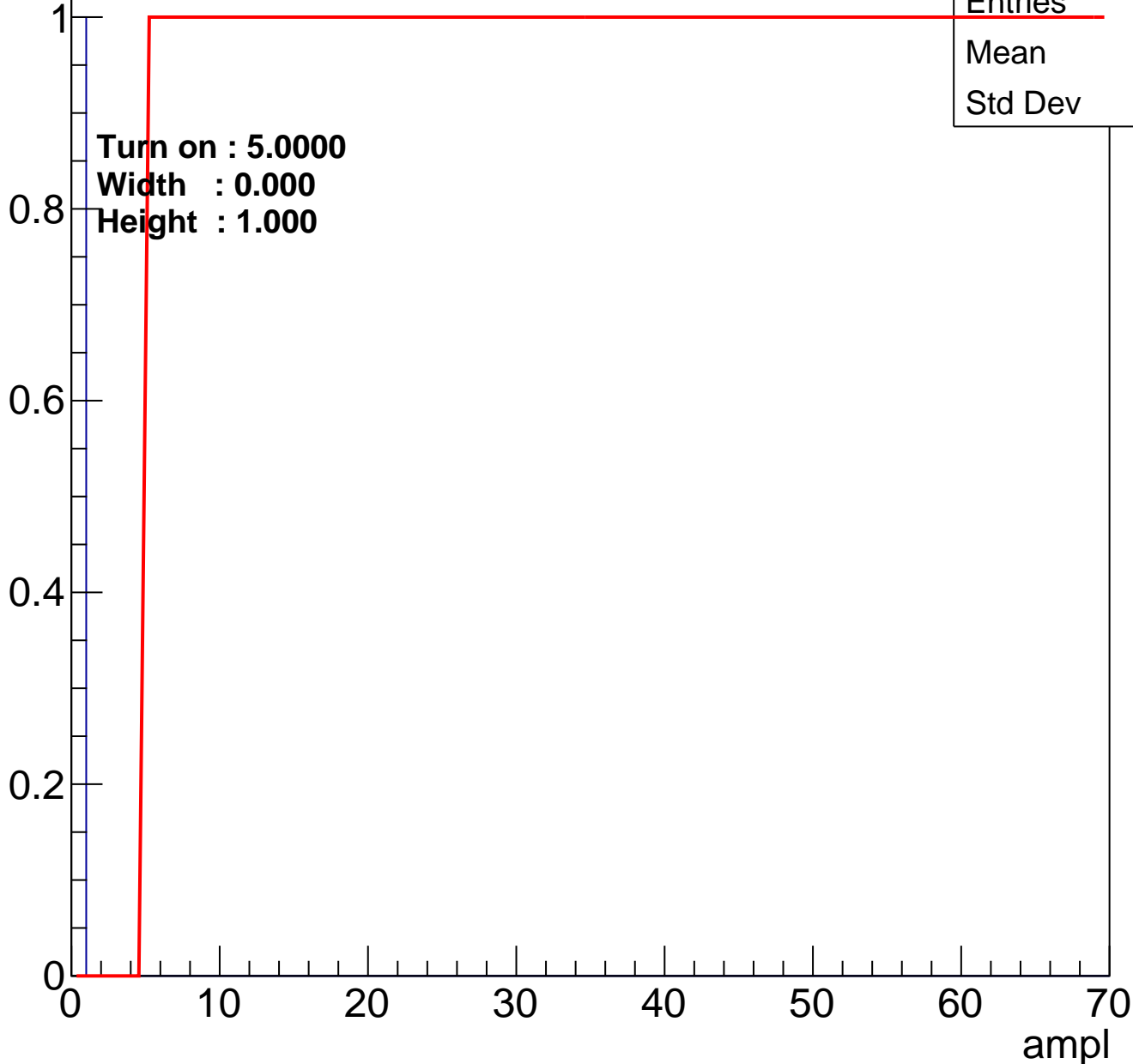


Entries	0
Mean	0
Std Dev	0

B1L001S, U12-ch18

calib_packv5_042523_0143.root, FC#2, port C2

Entry



B1L001S, U12-ch19

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	0
Mean	0
Std Dev	0

B1L001S, U12-ch20

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	2
Mean	0
Std Dev	0

B1L001S, U12-ch21

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	0
Mean	0
Std Dev	0

B1L001S, U12-ch22

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	2
Mean	0
Std Dev	0

B1L001S, U12-ch23

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	2
Mean	0
Std Dev	0

B1L001S, U12-ch24

calib_packv5_042523_0143.root, FC#2, port C2

Entry



B1L001S, U12-ch25

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	0
Mean	0
Std Dev	0

B1L001S, U12-ch26

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	0
Mean	0
Std Dev	0

B1L001S, U12-ch27

calib_packv5_042523_0143.root, FC#2, port C2

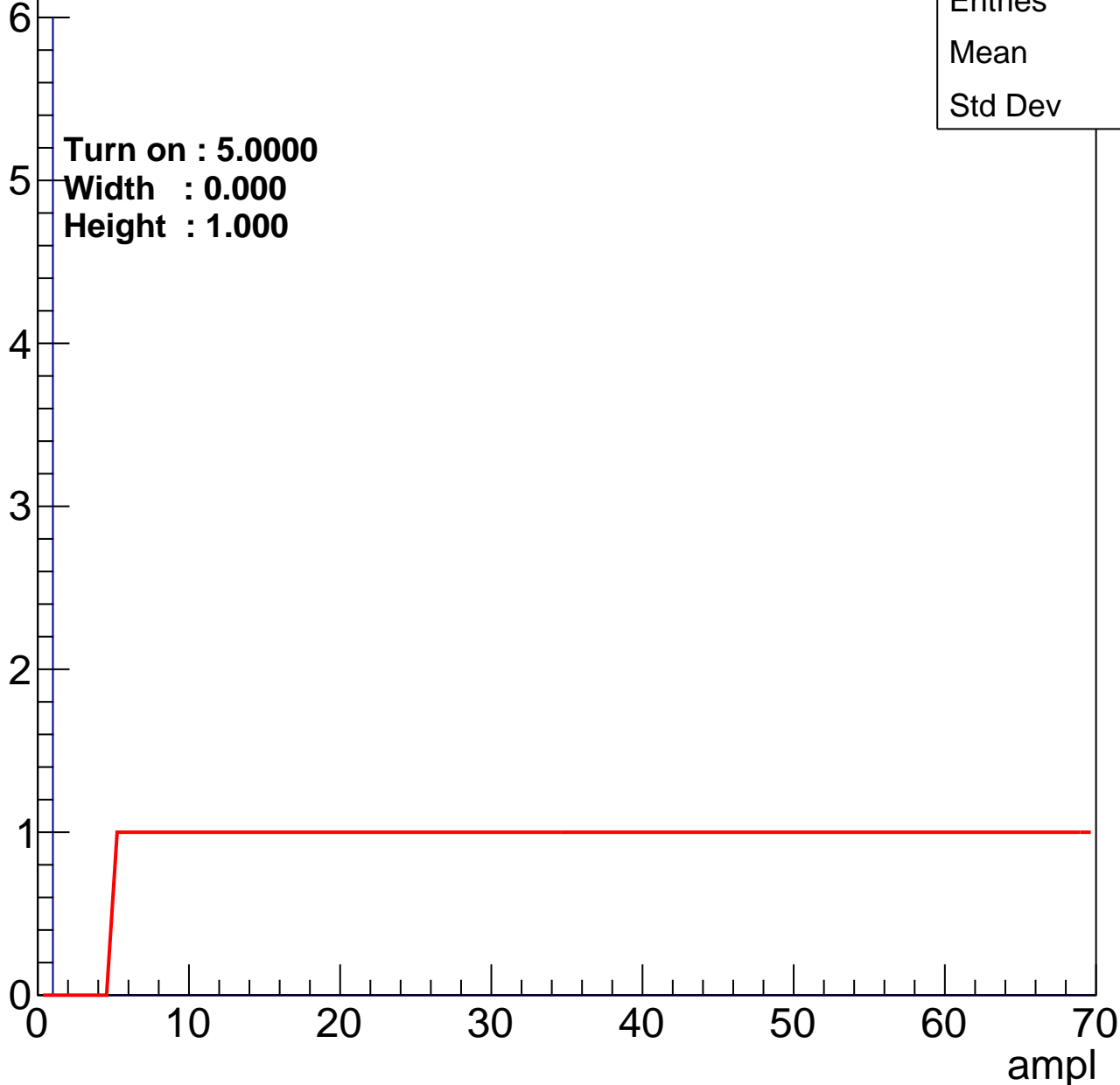
Entry

Entries	6
Mean	0
Std Dev	0

Turn on : 5.0000

Width : 0.000

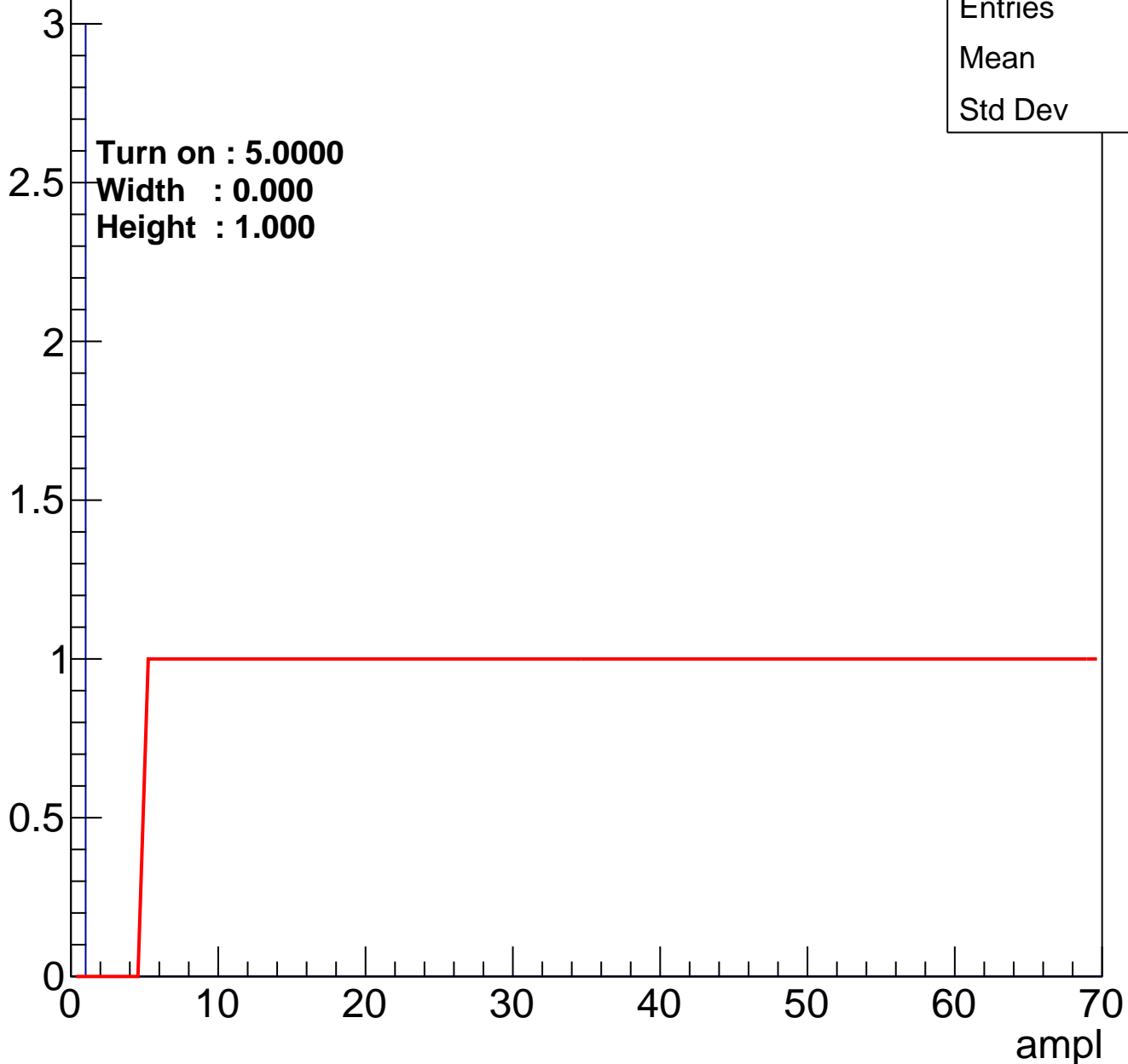
Height : 1.000



B1L001S, U12-ch28

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	3
Mean	0
Std Dev	0

B1L001S, U12-ch29

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	0
Mean	0
Std Dev	0

B1L001S, U12-ch30

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	1
Mean	0
Std Dev	0

B1L001S, U12-ch31

calib_packv5_042523_0143.root, FC#2, port C2

Entry

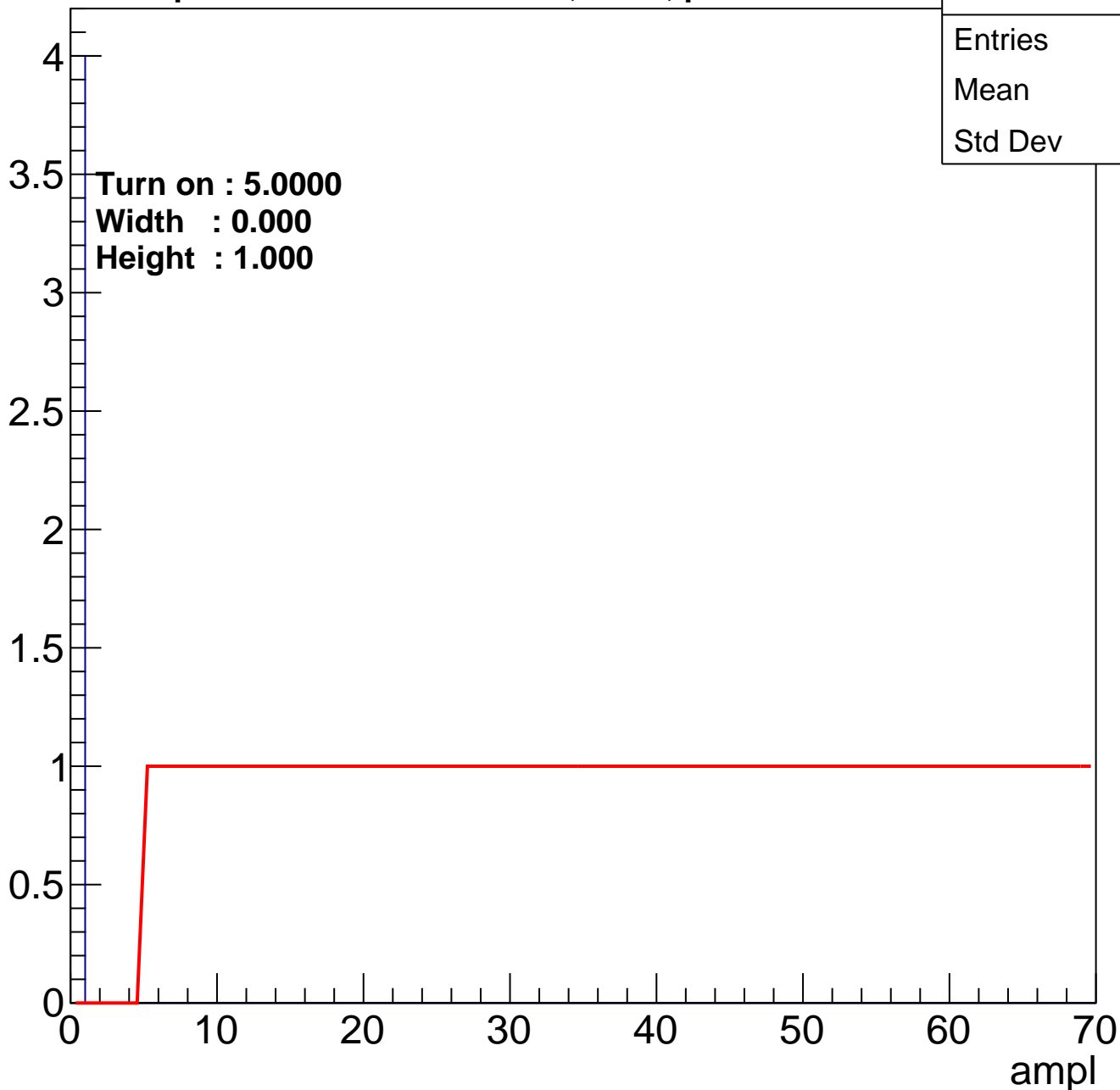


Entries	2
Mean	0
Std Dev	0

B1L001S, U12-ch32

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	4
Mean	0
Std Dev	0

B1L001S, U12-ch33

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	0
Mean	0
Std Dev	0

B1L001S, U12-ch34

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	2
Mean	0
Std Dev	0

B1L001S, U12-ch35

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	3
Mean	0
Std Dev	0

B1L001S, U12-ch36

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	3
Mean	0
Std Dev	0

B1L001S, U12-ch37

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	0
Mean	0
Std Dev	0

B1L001S, U12-ch38

calib_packv5_042523_0143.root, FC#2, port C2

Entry

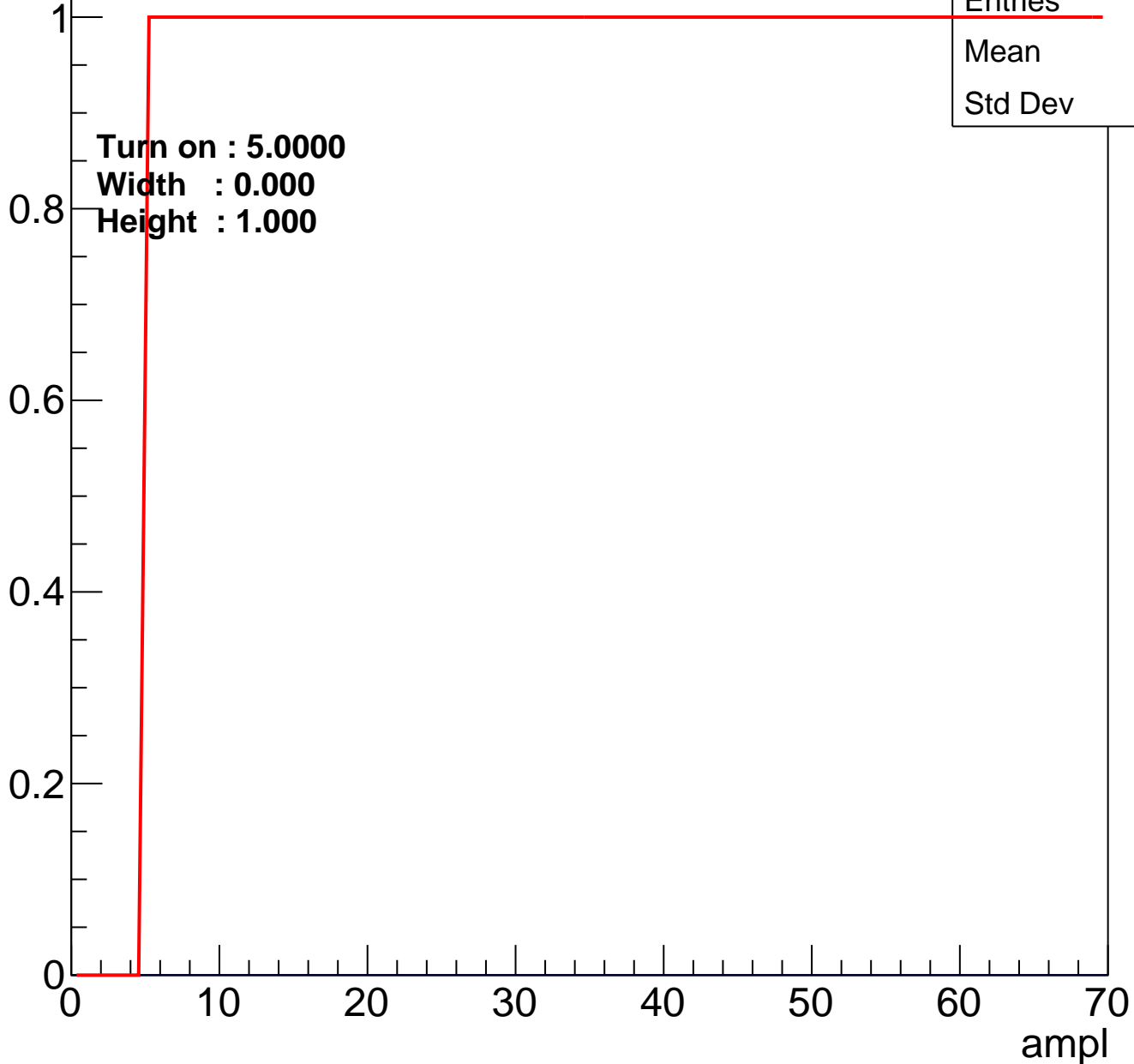


Entries	1
Mean	0
Std Dev	0

B1L001S, U12-ch39

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	0
Mean	0
Std Dev	0

B1L001S, U12-ch40

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	0
Mean	0
Std Dev	0

B1L001S, U12-ch41

calib_packv5_042523_0143.root, FC#2, port C2

Entry



B1L001S, U12-ch42

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	3
Mean	0
Std Dev	0

B1L001S, U12-ch43

calib_packv5_042523_0143.root, FC#2, port C2

Entry



B1L001S, U12-ch44

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	0
Mean	0
Std Dev	0

B1L001S, U12-ch45

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	2
Mean	0
Std Dev	0

B1L001S, U12-ch46

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	0
Mean	0
Std Dev	0

B1L001S, U12-ch47

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	0
Mean	0
Std Dev	0

B1L001S, U12-ch48

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	2
Mean	0
Std Dev	0

B1L001S, U12-ch49

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	2
Mean	0
Std Dev	0

B1L001S, U12-ch50

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	3
Mean	0
Std Dev	0

B1L001S, U12-ch51

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	1
Mean	0
Std Dev	0

B1L001S, U12-ch52

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	1
Mean	0
Std Dev	0

B1L001S, U12-ch53

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	0
Mean	0
Std Dev	0

B1L001S, U12-ch54

calib_packv5_042523_0143.root, FC#2, port C2

Entry

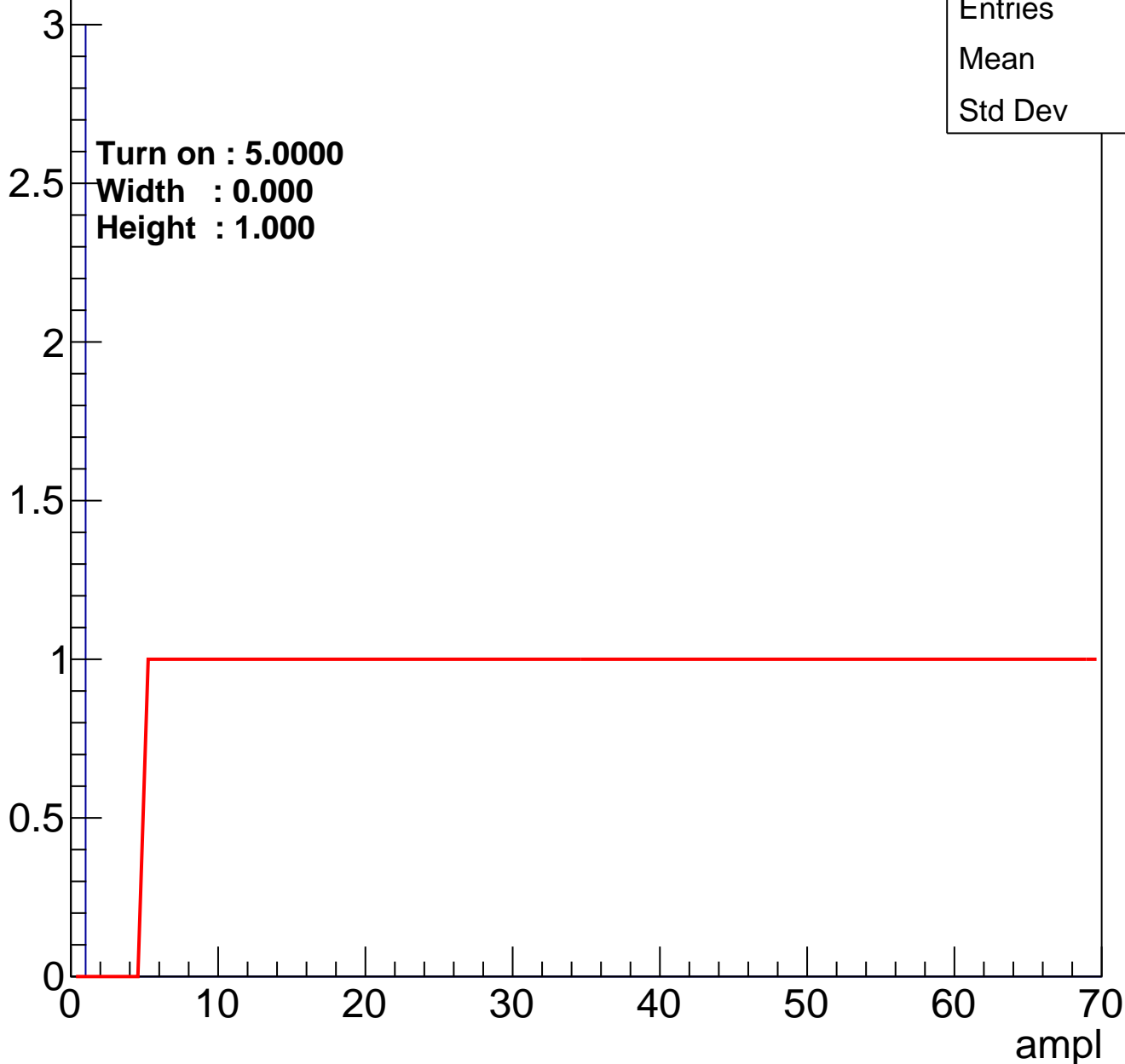


Entries	0
Mean	0
Std Dev	0

B1L001S, U12-ch55

calib_packv5_042523_0143.root, FC#2, port C2

Entry



B1L001S, U12-ch56

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	2
Mean	0
Std Dev	0

B1L001S, U12-ch57

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	2
Mean	0
Std Dev	0

B1L001S, U12-ch58

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	1
Mean	0
Std Dev	0

B1L001S, U12-ch59

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	0
Mean	0
Std Dev	0

B1L001S, U12-ch60

calib_packv5_042523_0143.root, FC#2, port C2

Entry

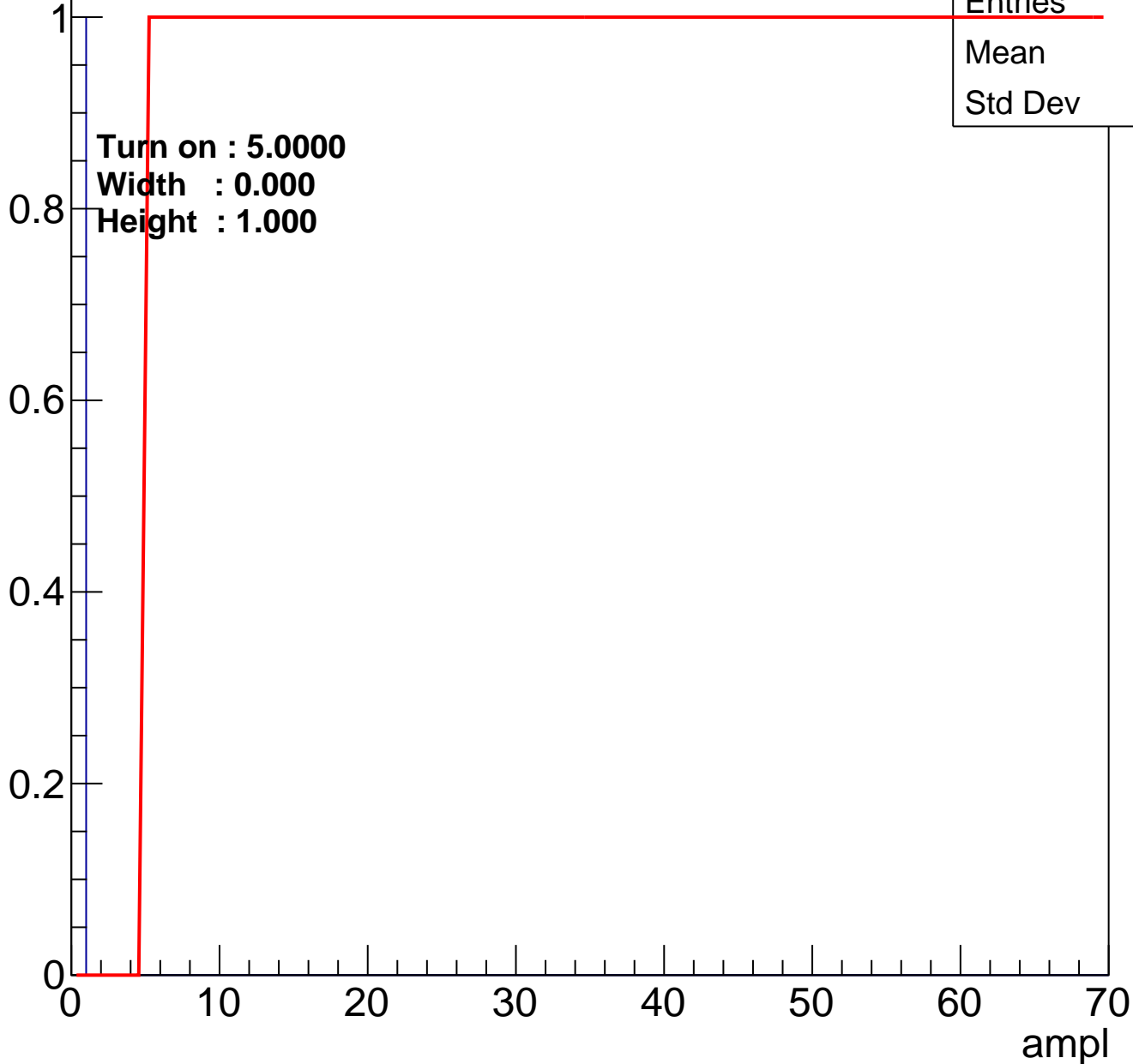


Entries	2
Mean	0
Std Dev	0

B1L001S, U12-ch61

calib_packv5_042523_0143.root, FC#2, port C2

Entry

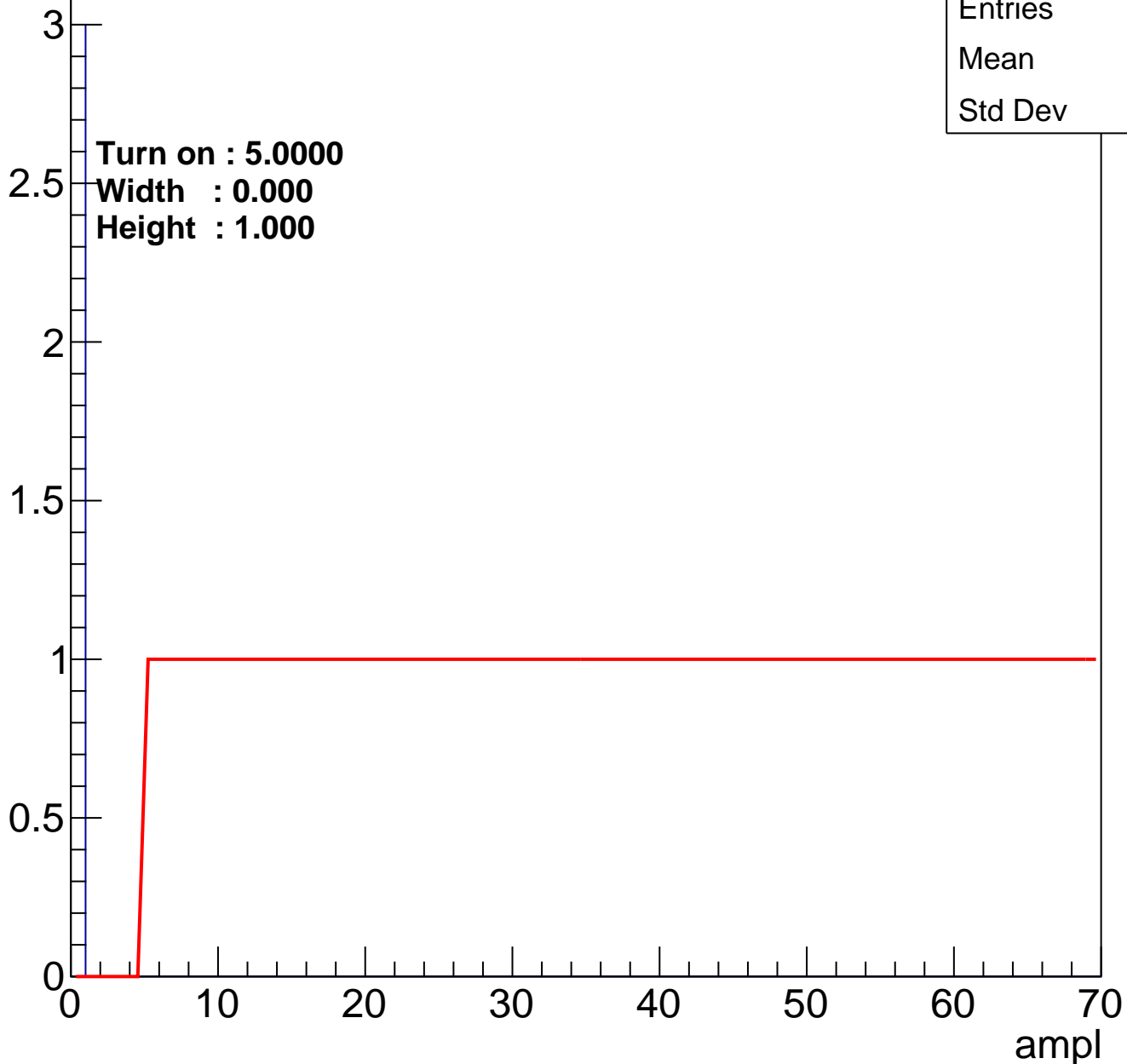


Entries	1
Mean	0
Std Dev	0

B1L001S, U12-ch62

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	3
Mean	0
Std Dev	0

B1L001S, U12-ch63

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	2
Mean	0
Std Dev	0

B1L001S, U12-ch64

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	1
Mean	0
Std Dev	0

B1L001S, U12-ch65

calib_packv5_042523_0143.root, FC#2, port C2

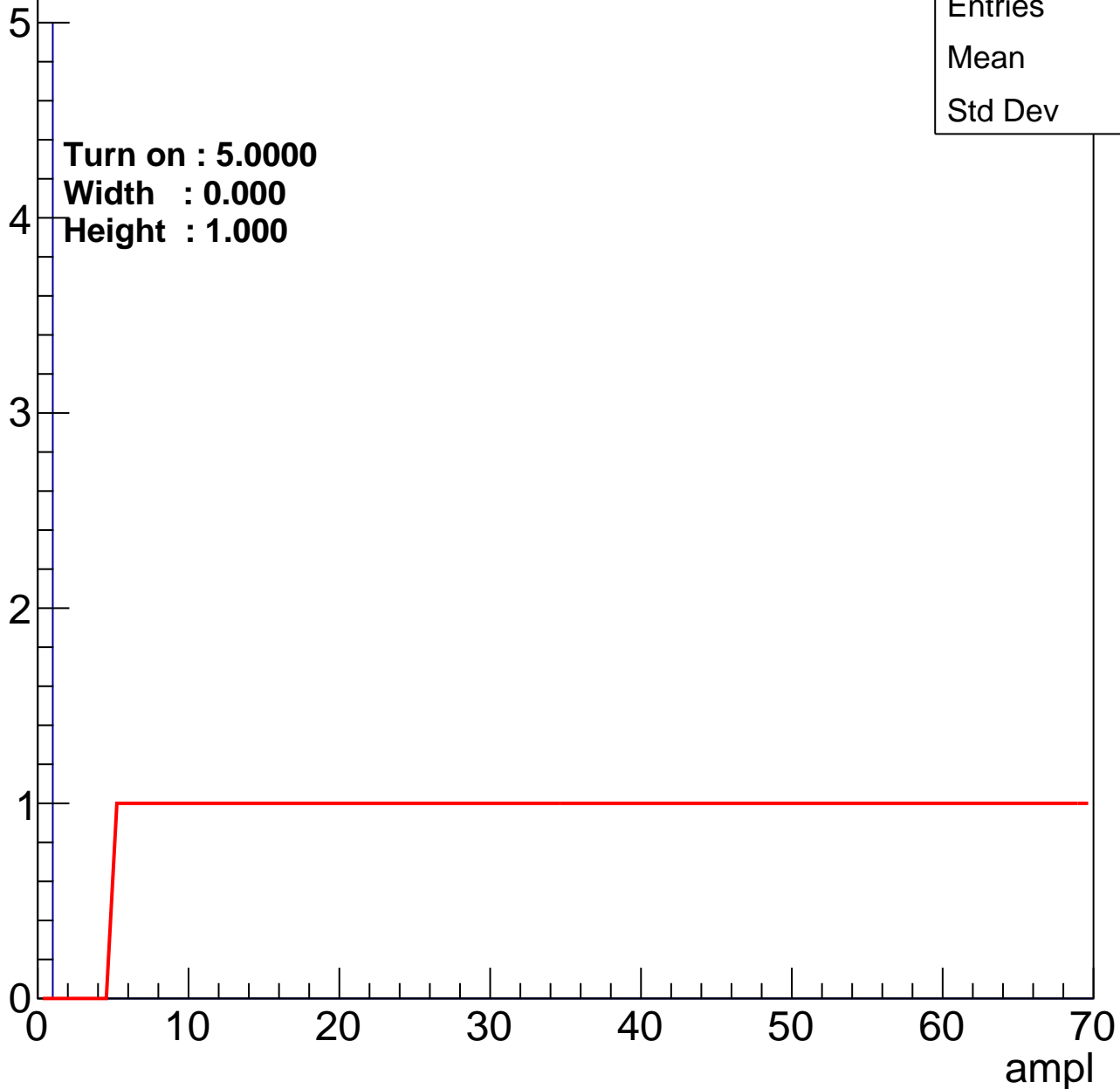
Entry

Entries	5
Mean	0
Std Dev	0

Turn on : 5.0000

Width : 0.000

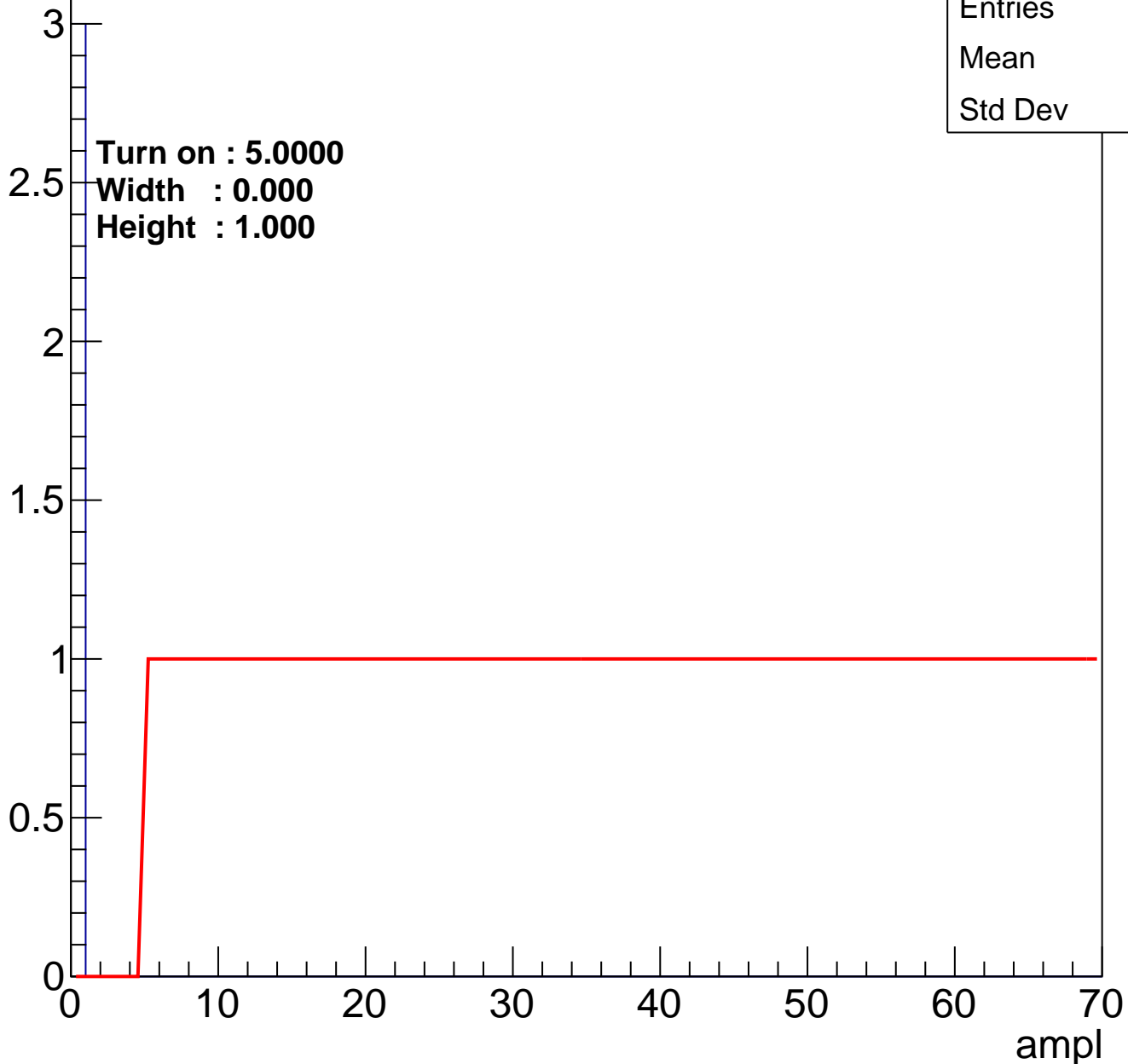
Height : 1.000



B1L001S, U12-ch66

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	3
Mean	0
Std Dev	0

B1L001S, U12-ch67

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	2
Mean	0
Std Dev	0

B1L001S, U12-ch68

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	0
Mean	0
Std Dev	0

B1L001S, U12-ch69

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	0
Mean	0
Std Dev	0

B1L001S, U12-ch70

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	0
Mean	0
Std Dev	0

B1L001S, U12-ch71

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	0
Mean	0
Std Dev	0

B1L001S, U12-ch72

calib_packv5_042523_0143.root, FC#2, port C2

Entry



B1L001S, U12-ch73

calib_packv5_042523_0143.root, FC#2, port C2

Entry

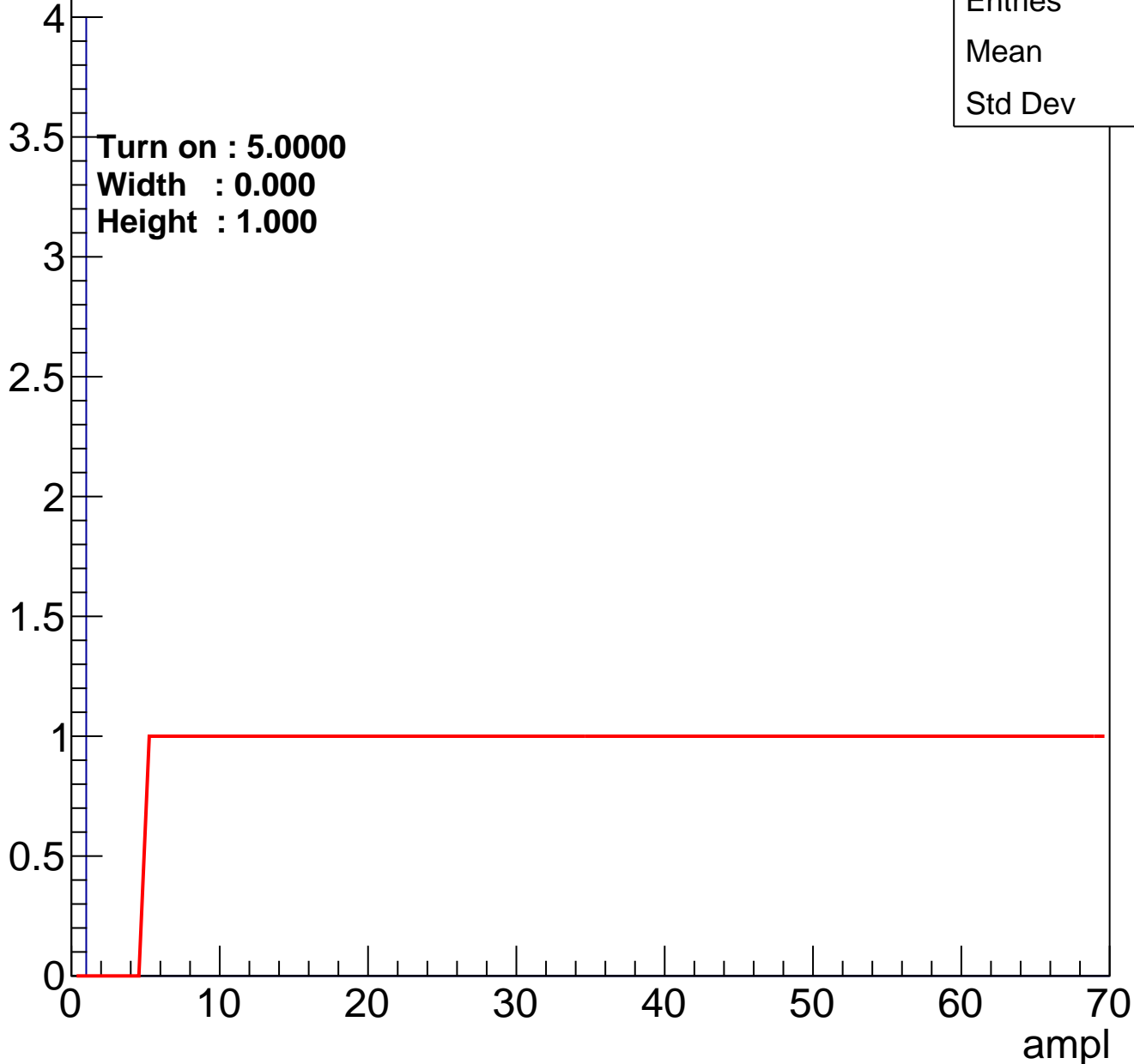


Entries	2
Mean	0
Std Dev	0

B1L001S, U12-ch74

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	4
Mean	0
Std Dev	0

B1L001S, U12-ch75

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	1
Mean	0
Std Dev	0

B1L001S, U12-ch76

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	0
Mean	0
Std Dev	0

B1L001S, U12-ch77

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	1
Mean	0
Std Dev	0

B1L001S, U12-ch78

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	2
Mean	0
Std Dev	0

B1L001S, U12-ch79

calib_packv5_042523_0143.root, FC#2, port C2

Entry

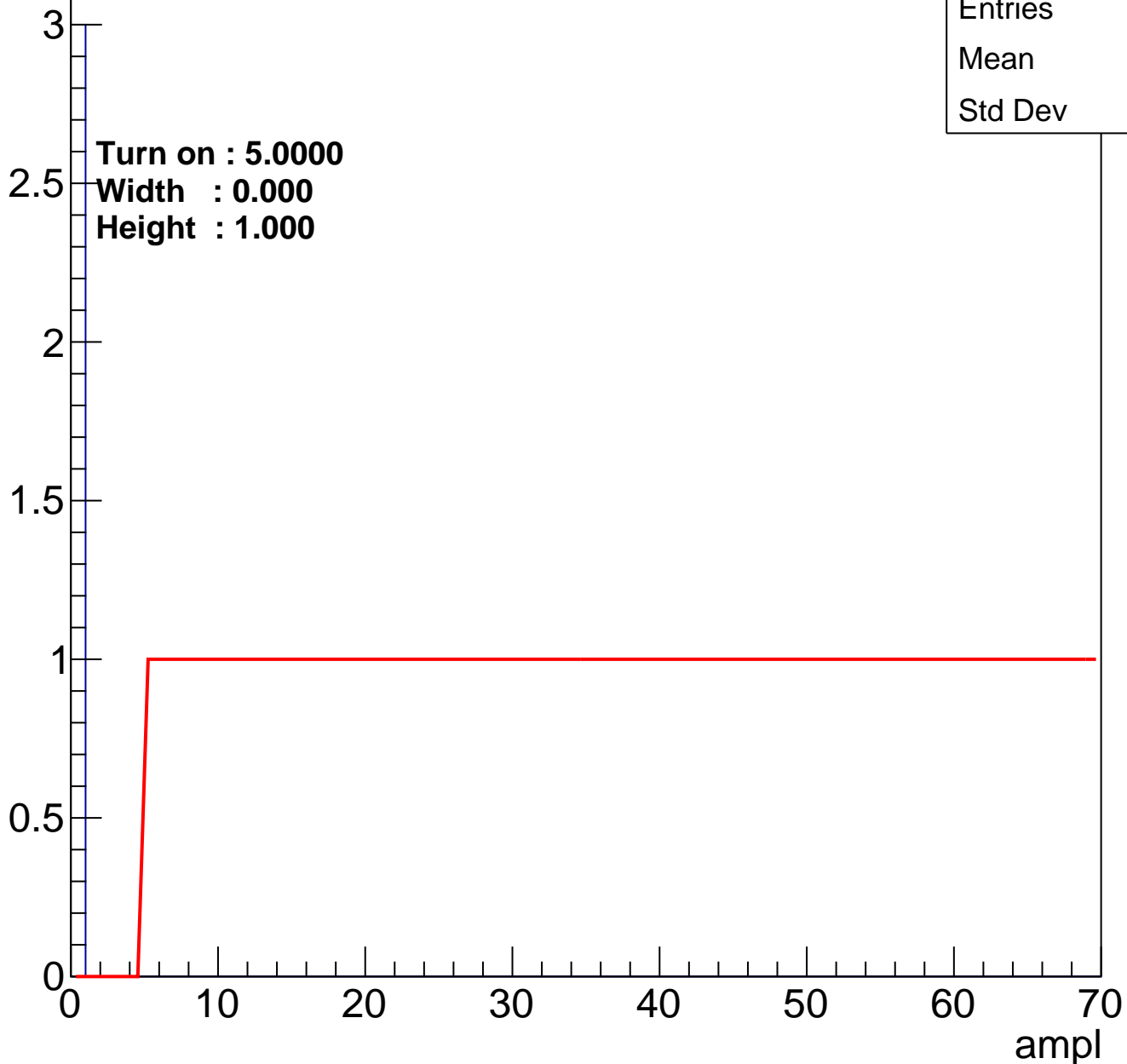


Entries	2
Mean	0
Std Dev	0

B1L001S, U12-ch80

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	3
Mean	0
Std Dev	0

B1L001S, U12-ch81

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	2
Mean	0
Std Dev	0

B1L001S, U12-ch82

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	3
Mean	0
Std Dev	0

B1L001S, U12-ch83

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	0
Mean	0
Std Dev	0

B1L001S, U12-ch84

calib_packv5_042523_0143.root, FC#2, port C2

Entry



B1L001S, U12-ch85

calib_packv5_042523_0143.root, FC#2, port C2

Entry



B1L001S, U12-ch86

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	0
Mean	0
Std Dev	0

B1L001S, U12-ch87

calib_packv5_042523_0143.root, FC#2, port C2

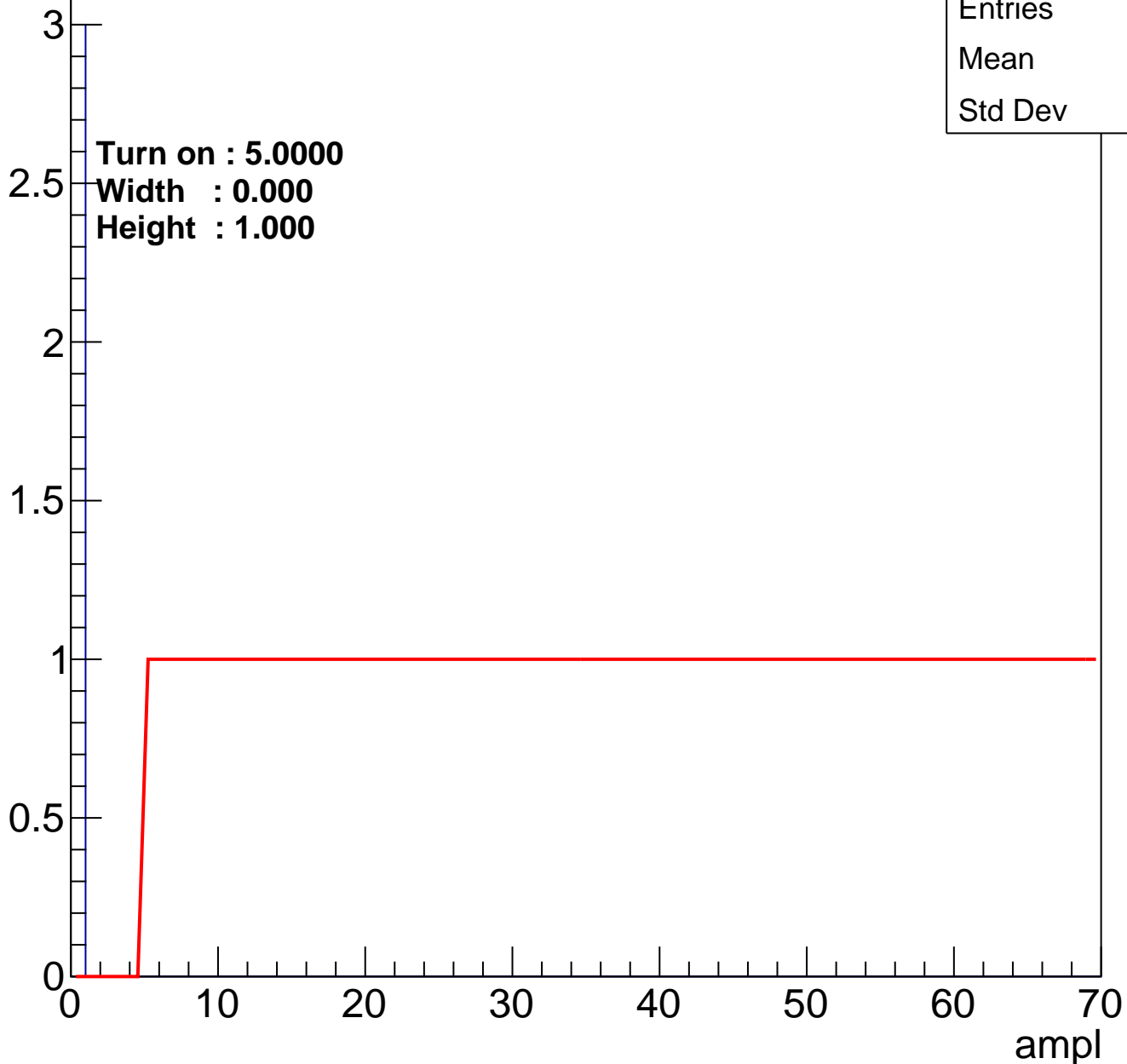
Entry



B1L001S, U12-ch88

calib_packv5_042523_0143.root, FC#2, port C2

Entry

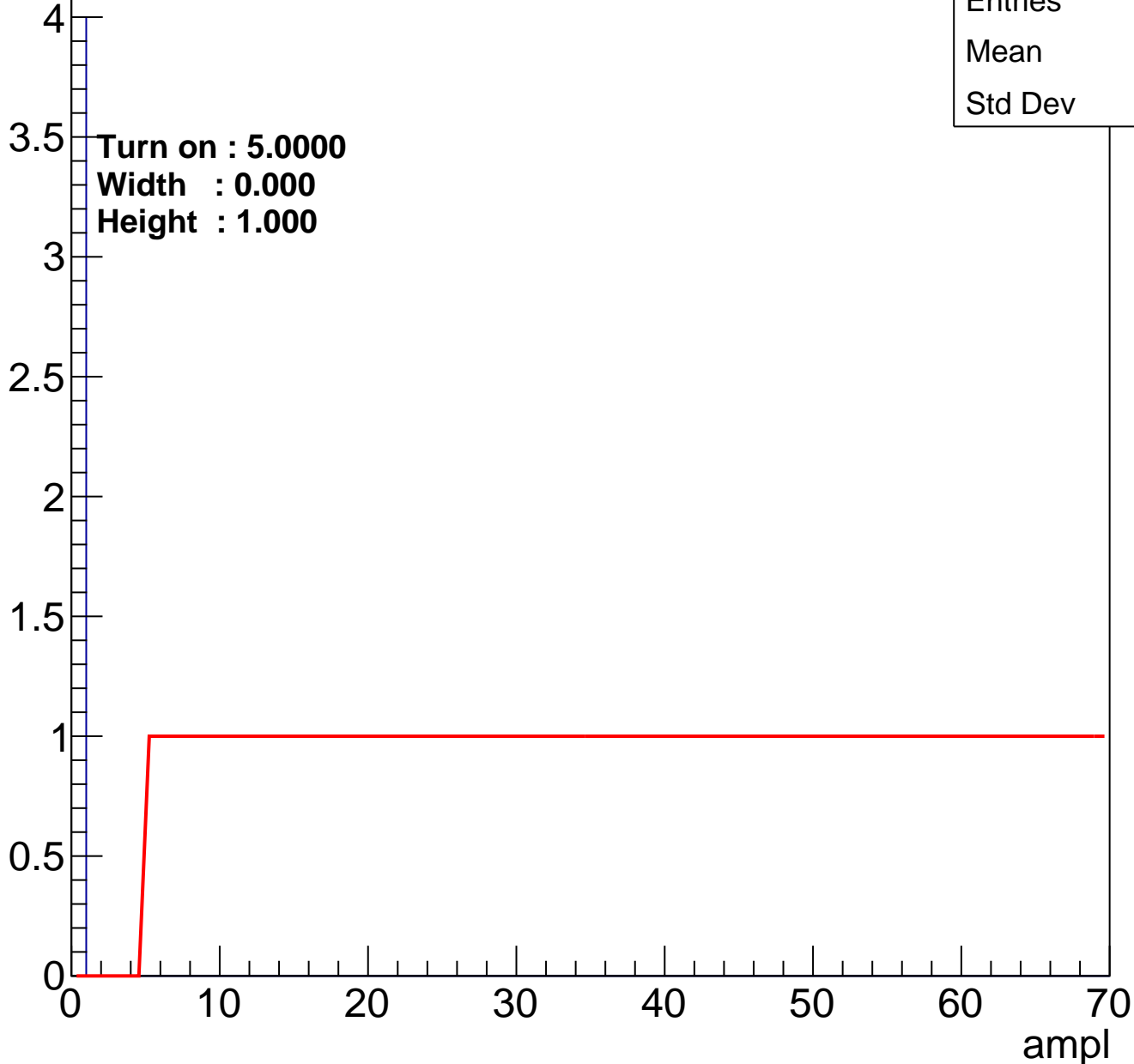


Entries	3
Mean	0
Std Dev	0

B1L001S, U12-ch89

calib_packv5_042523_0143.root, FC#2, port C2

Entry

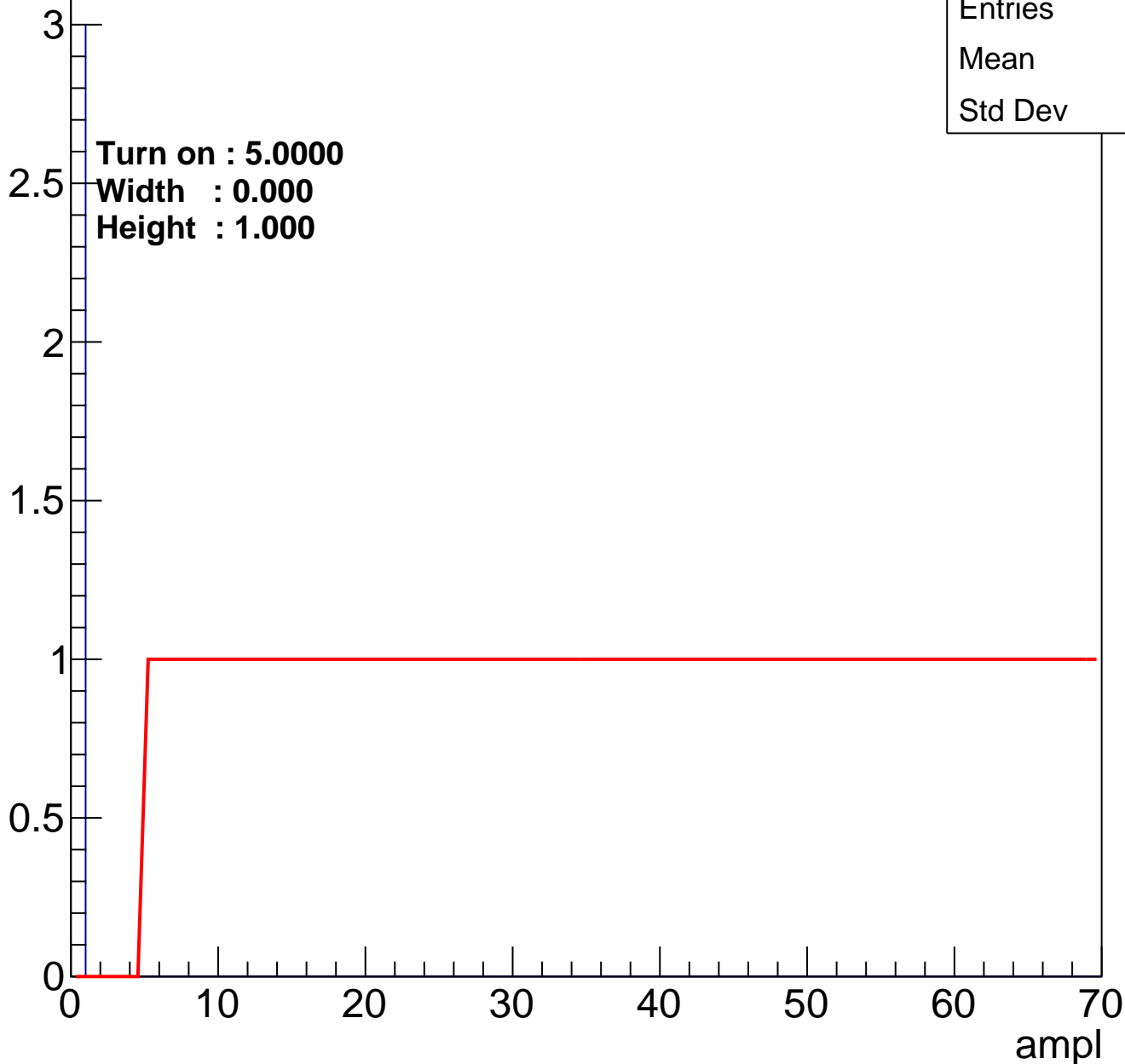


Entries	4
Mean	0
Std Dev	0

B1L001S, U12-ch90

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	3
Mean	0
Std Dev	0

B1L001S, U12-ch91

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	3
Mean	0
Std Dev	0

B1L001S, U12-ch92

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	2
Mean	0
Std Dev	0

B1L001S, U12-ch93

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	2
Mean	0
Std Dev	0

B1L001S, U12-ch94

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	1
Mean	0
Std Dev	0

B1L001S, U12-ch95

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	0
Mean	0
Std Dev	0

B1L001S, U12-ch96

calib_packv5_042523_0143.root, FC#2, port C2

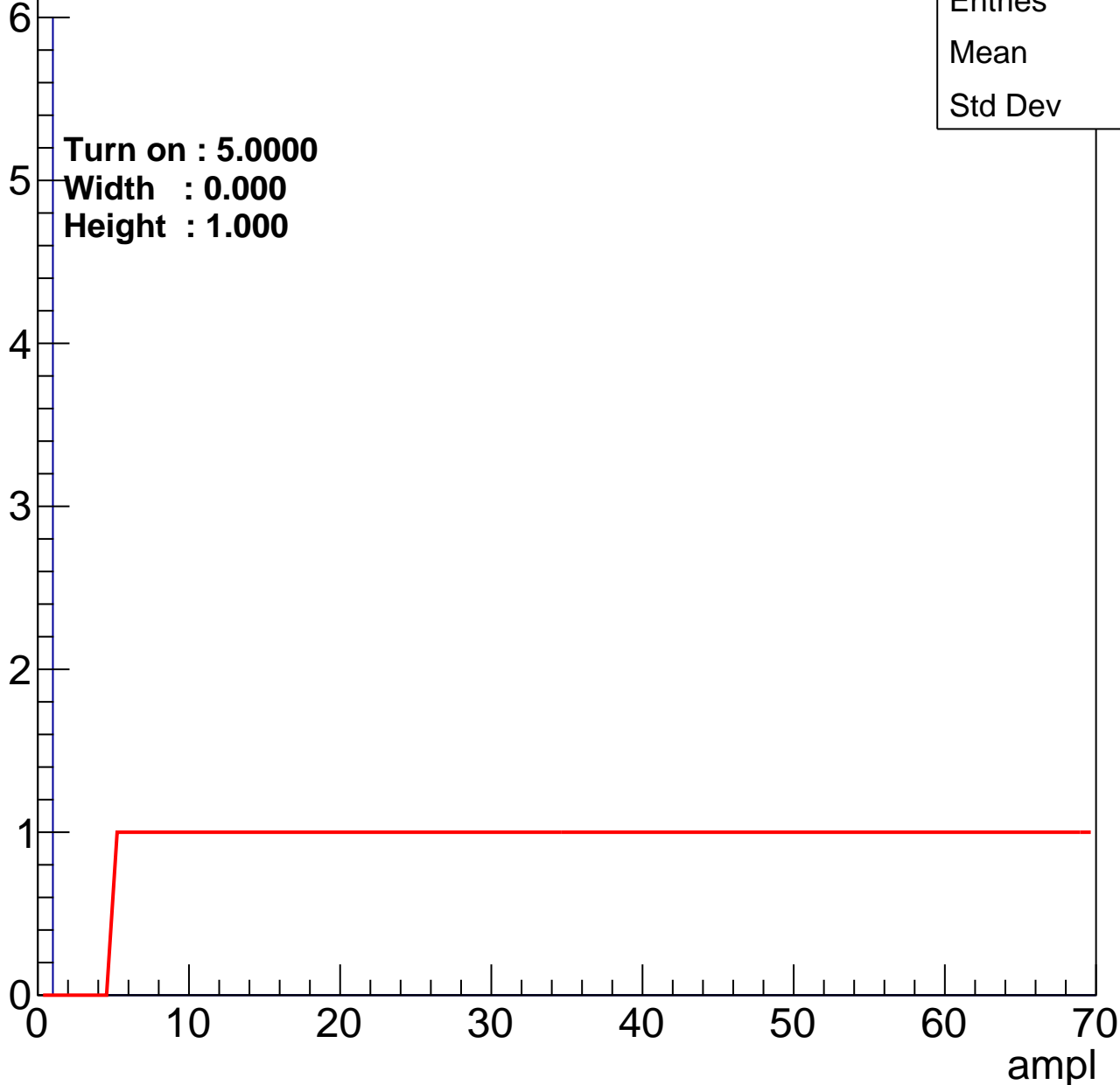
Entry

Entries	6
Mean	0
Std Dev	0

Turn on : 5.0000

Width : 0.000

Height : 1.000



B1L001S, U12-ch97

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	0
Mean	0
Std Dev	0

B1L001S, U12-ch98

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	2
Mean	0
Std Dev	0

B1L001S, U12-ch99

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	2
Mean	0
Std Dev	0

B1L001S, U12-ch100

calib_packv5_042523_0143.root, FC#2, port C2

Entry



B1L001S, U12-ch101

calib_packv5_042523_0143.root, FC#2, port C2

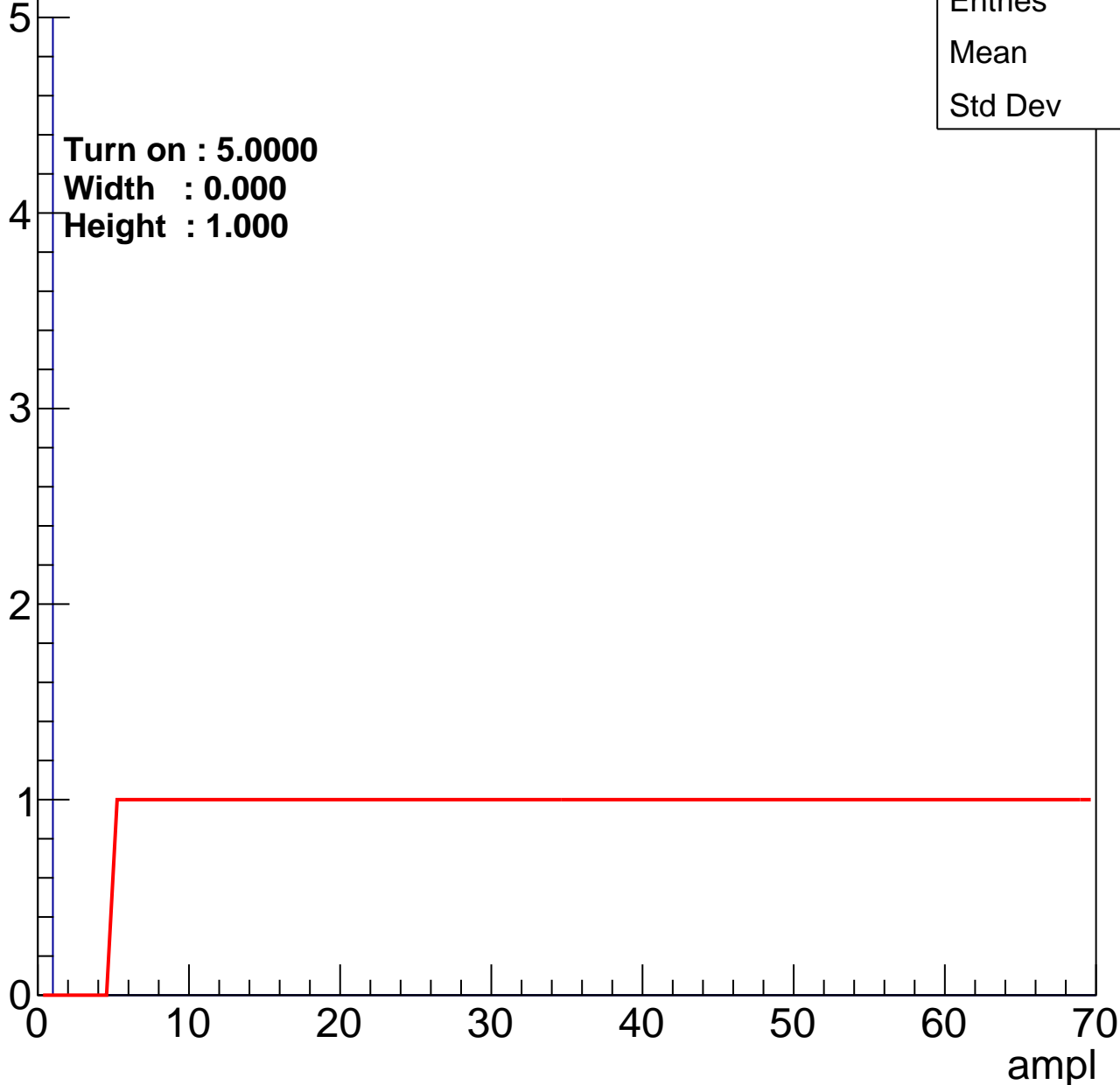
Entry

Entries	5
Mean	0
Std Dev	0

Turn on : 5.0000

Width : 0.000

Height : 1.000



B1L001S, U12-ch102

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	0
Mean	0
Std Dev	0

B1L001S, U12-ch103

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	2
Mean	0
Std Dev	0

B1L001S, U12-ch104

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	2
Mean	0
Std Dev	0

B1L001S, U12-ch105

calib_packv5_042523_0143.root, FC#2, port C2

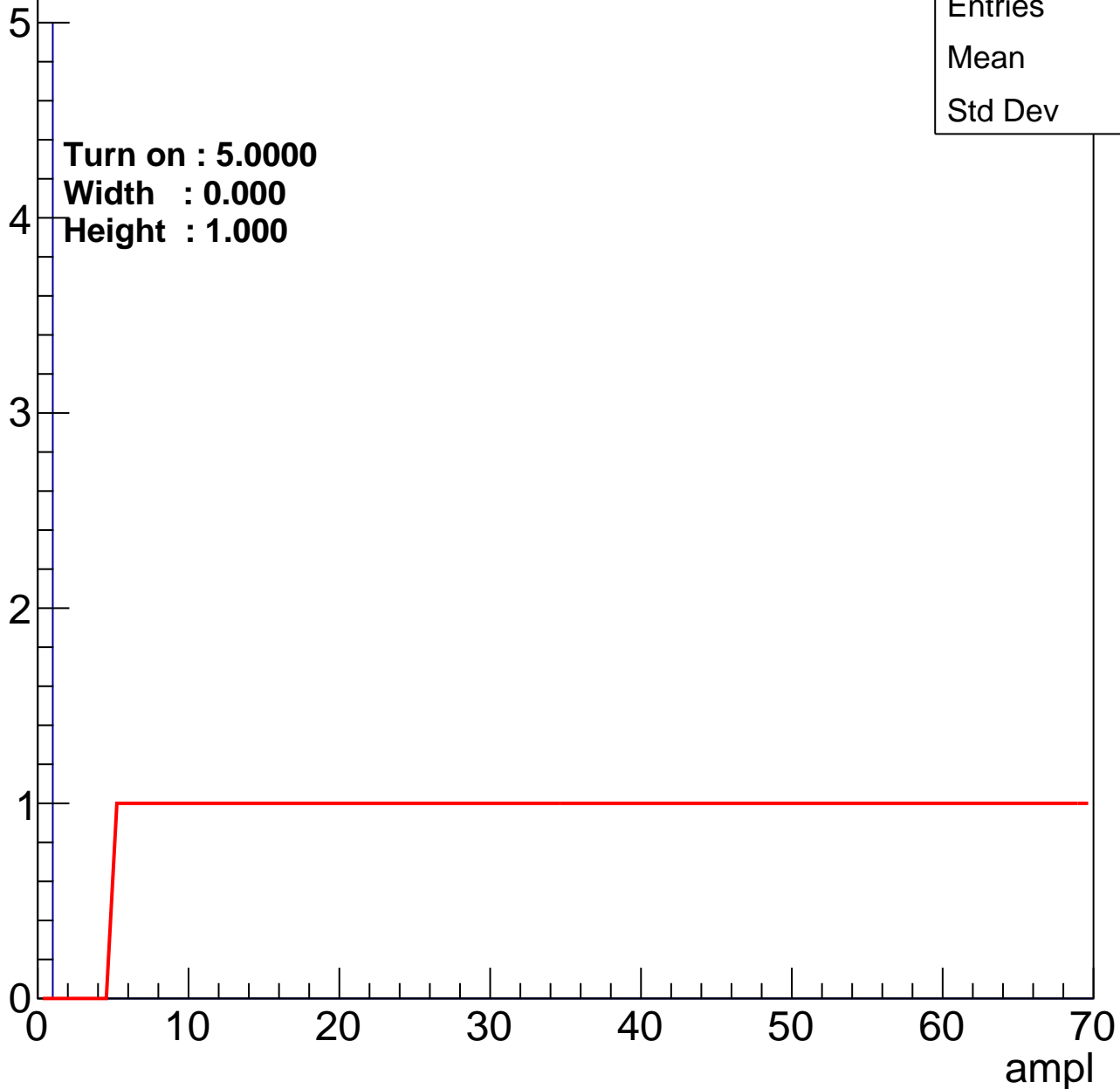
Entry

Entries	5
Mean	0
Std Dev	0

Turn on : 5.0000

Width : 0.000

Height : 1.000



B1L001S, U12-ch106

calib_packv5_042523_0143.root, FC#2, port C2

Entry



B1L001S, U12-ch107

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	2
Mean	0
Std Dev	0

B1L001S, U12-ch108

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	2
Mean	0
Std Dev	0

B1L001S, U12-ch109

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	1
Mean	0
Std Dev	0

B1L001S, U12-ch110

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	1
Mean	0
Std Dev	0

B1L001S, U12-ch111

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	2
Mean	0
Std Dev	0

B1L001S, U12-ch112

calib_packv5_042523_0143.root, FC#2, port C2

Entry

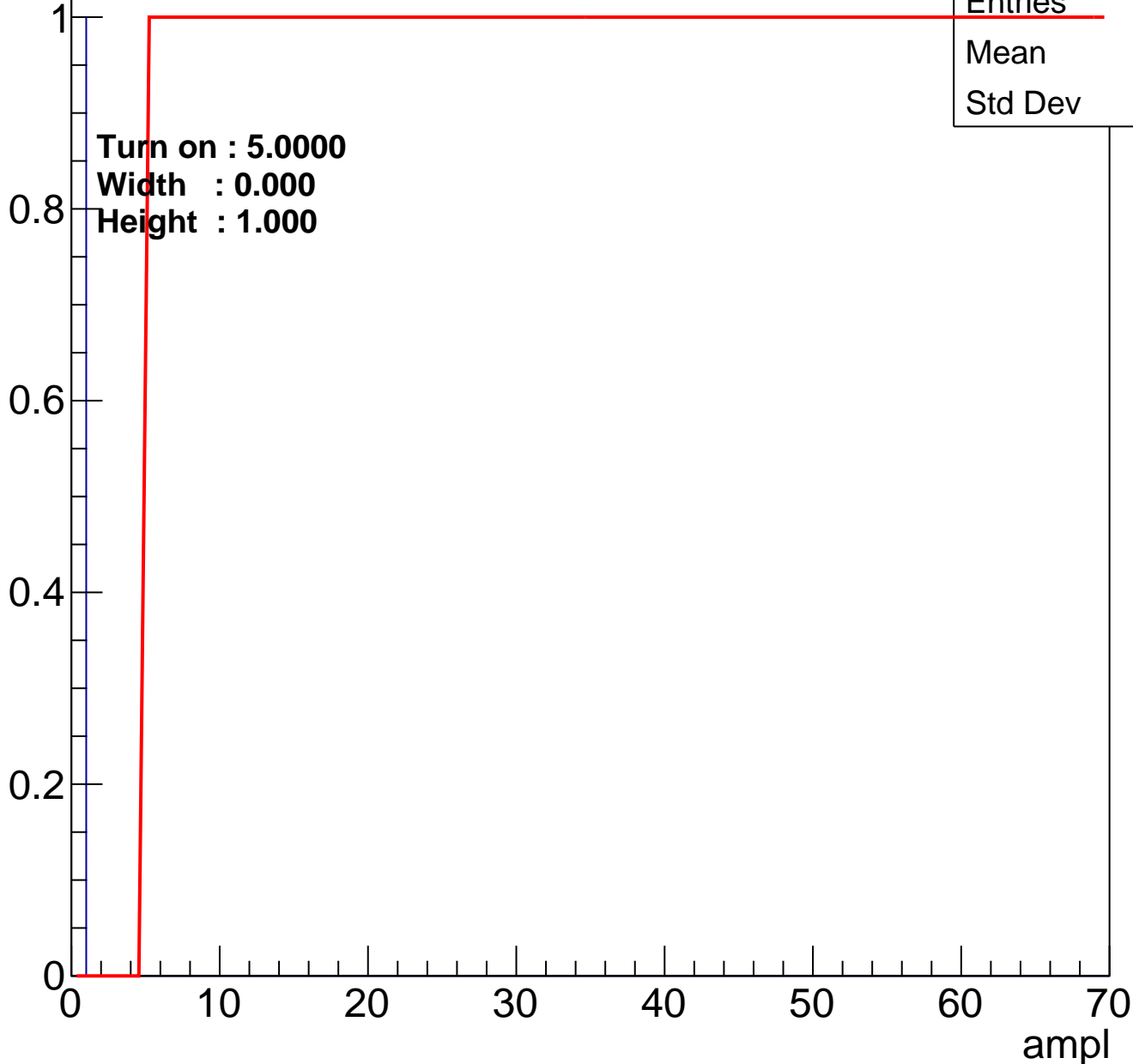


Entries	0
Mean	0
Std Dev	0

B1L001S, U12-ch113

calib_packv5_042523_0143.root, FC#2, port C2

Entry



B1L001S, U12-ch114

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	0
Mean	0
Std Dev	0

B1L001S, U12-ch115

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	3
Mean	0
Std Dev	0

B1L001S, U12-ch116

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	1
Mean	0
Std Dev	0

B1L001S, U12-ch117

calib_packv5_042523_0143.root, FC#2, port C2

Entry

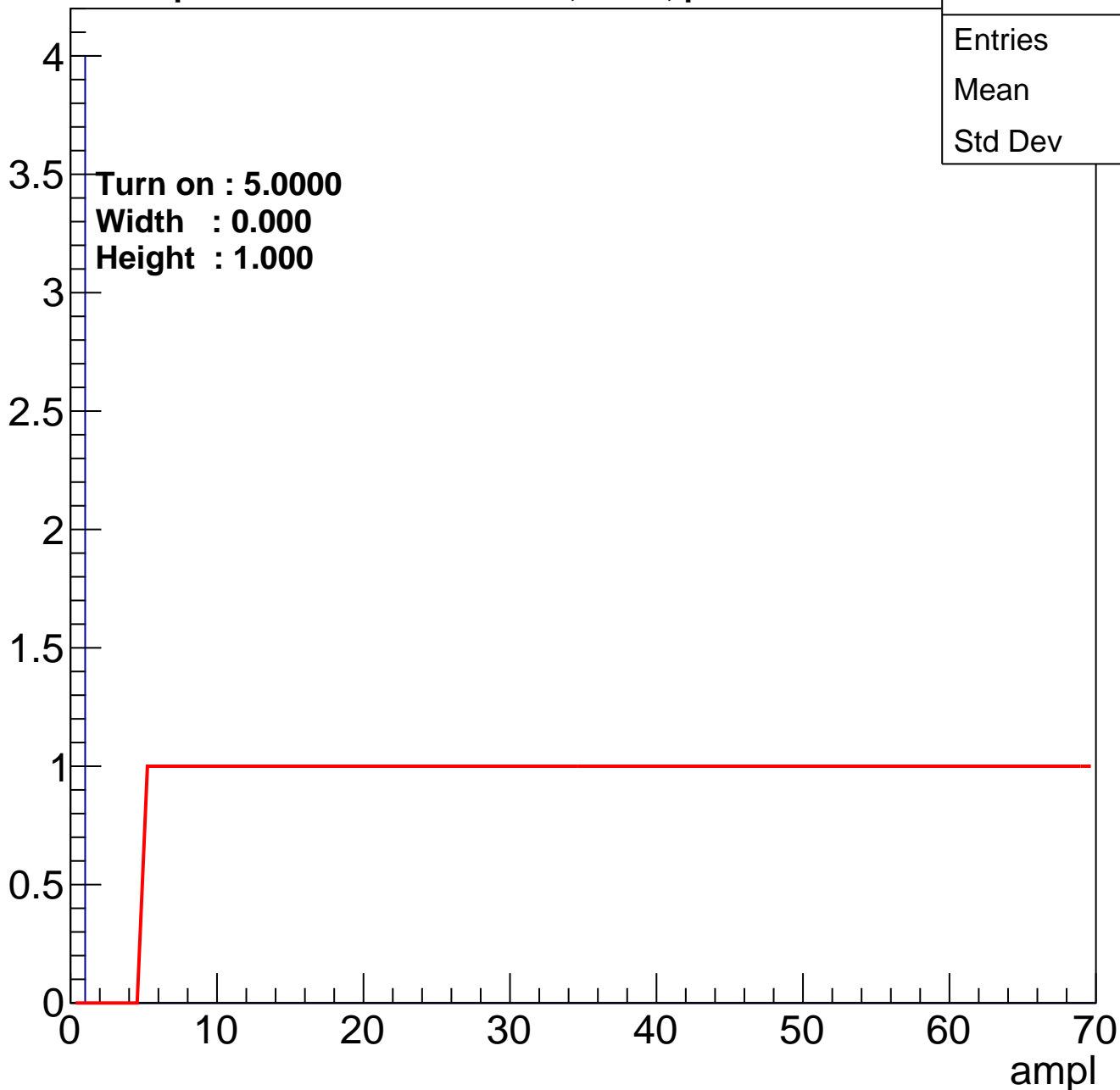


Entries	2
Mean	0
Std Dev	0

B1L001S, U12-ch118

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	4
Mean	0
Std Dev	0

B1L001S, U12-ch119

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	1
Mean	0
Std Dev	0

B1L001S, U12-ch120

calib_packv5_042523_0143.root, FC#2, port C2

Entry

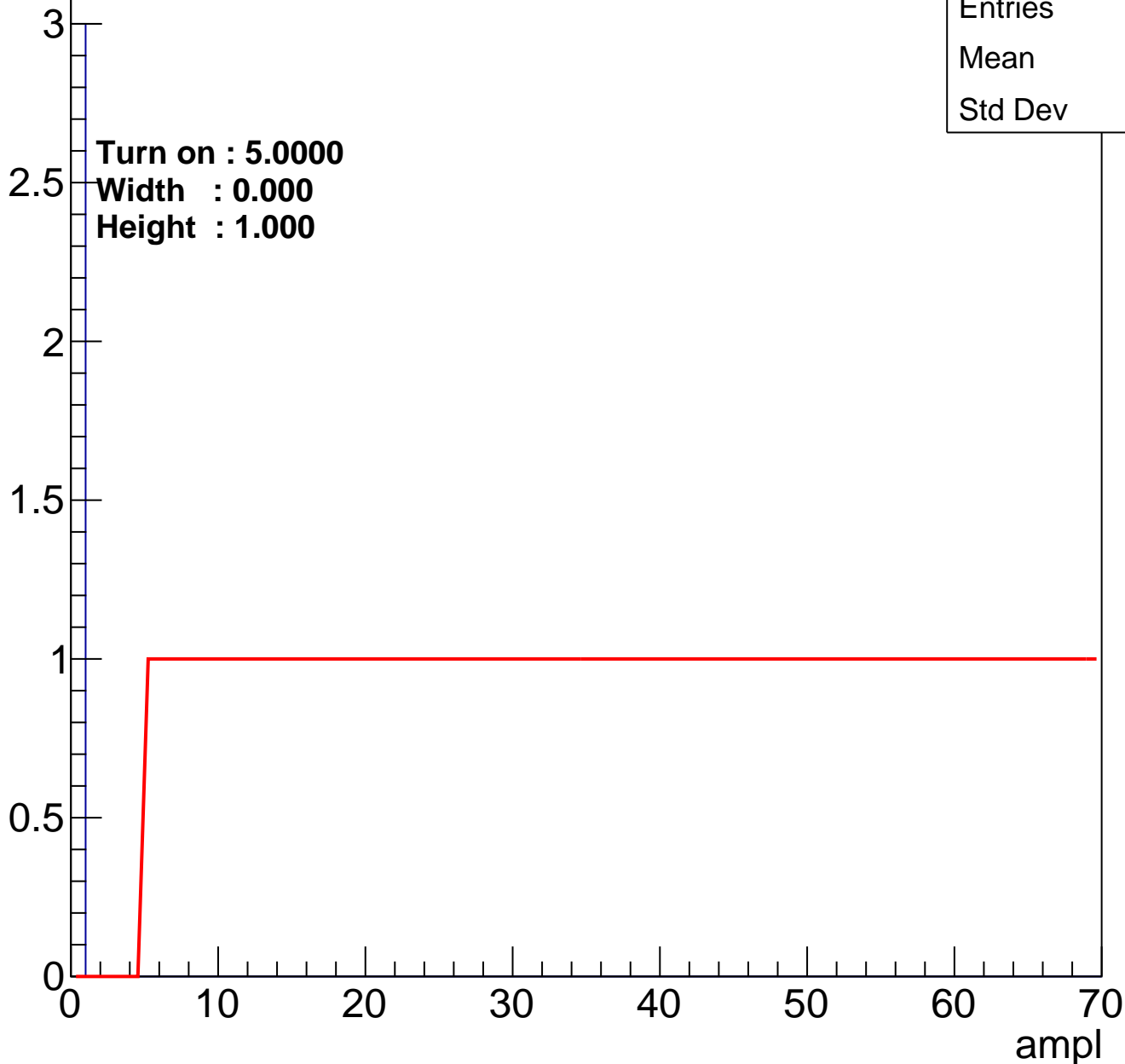


Entries	1
Mean	0
Std Dev	0

B1L001S, U12-ch121

calib_packv5_042523_0143.root, FC#2, port C2

Entry

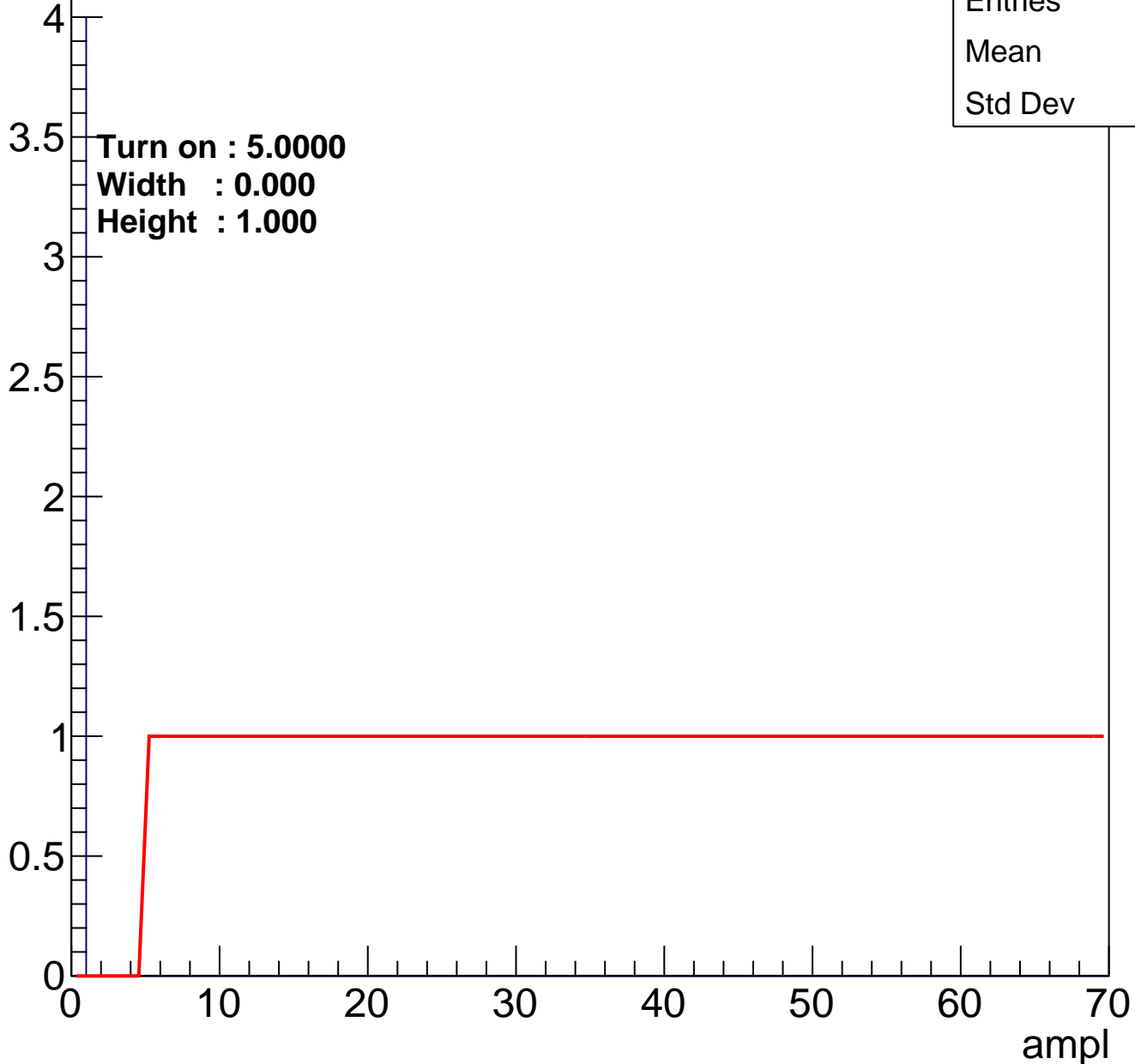


Entries	3
Mean	0
Std Dev	0

B1L001S, U12-ch122

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	4
Mean	0
Std Dev	0

B1L001S, U12-ch123

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	1
Mean	0
Std Dev	0

B1L001S, U12-ch124

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	0
Mean	0
Std Dev	0

B1L001S, U12-ch125

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	1
Mean	0
Std Dev	0

B1L001S, U12-ch126

calib_packv5_042523_0143.root, FC#2, port C2

Entry



Entries	1
Mean	0
Std Dev	0

B1L001S, U12-ch127

calib_packv5_042523_0143.root, FC#2, port C2

Entry



B1L001S, U12-ch127

calib_packv5_042523_0143.root, FC#2, port C2

Entry

