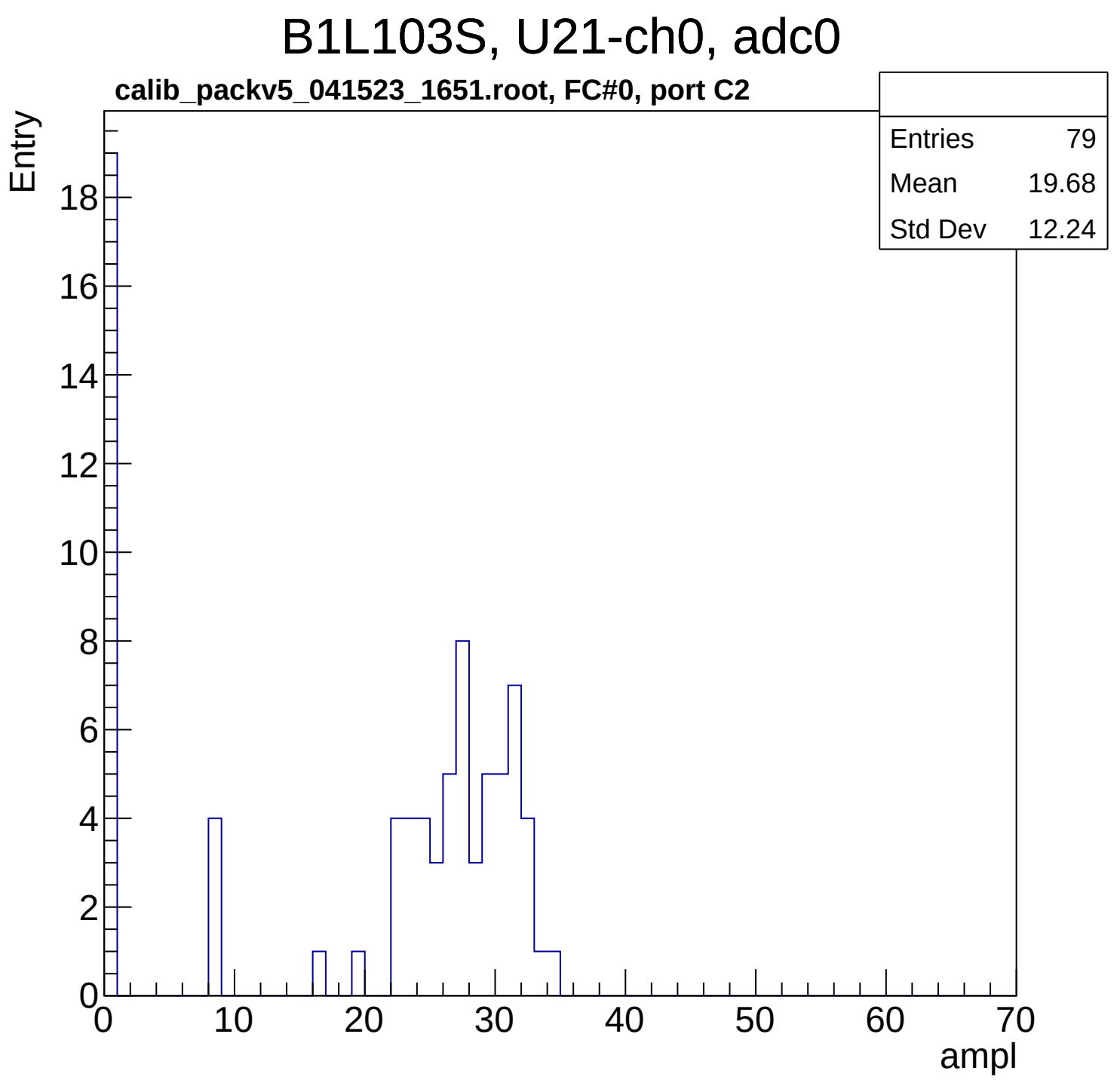
B1L103S, U21-ch0, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 19.68
Std Dev 12.24
Entry
0
2
4
6
8
10
12
14
16
18
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10
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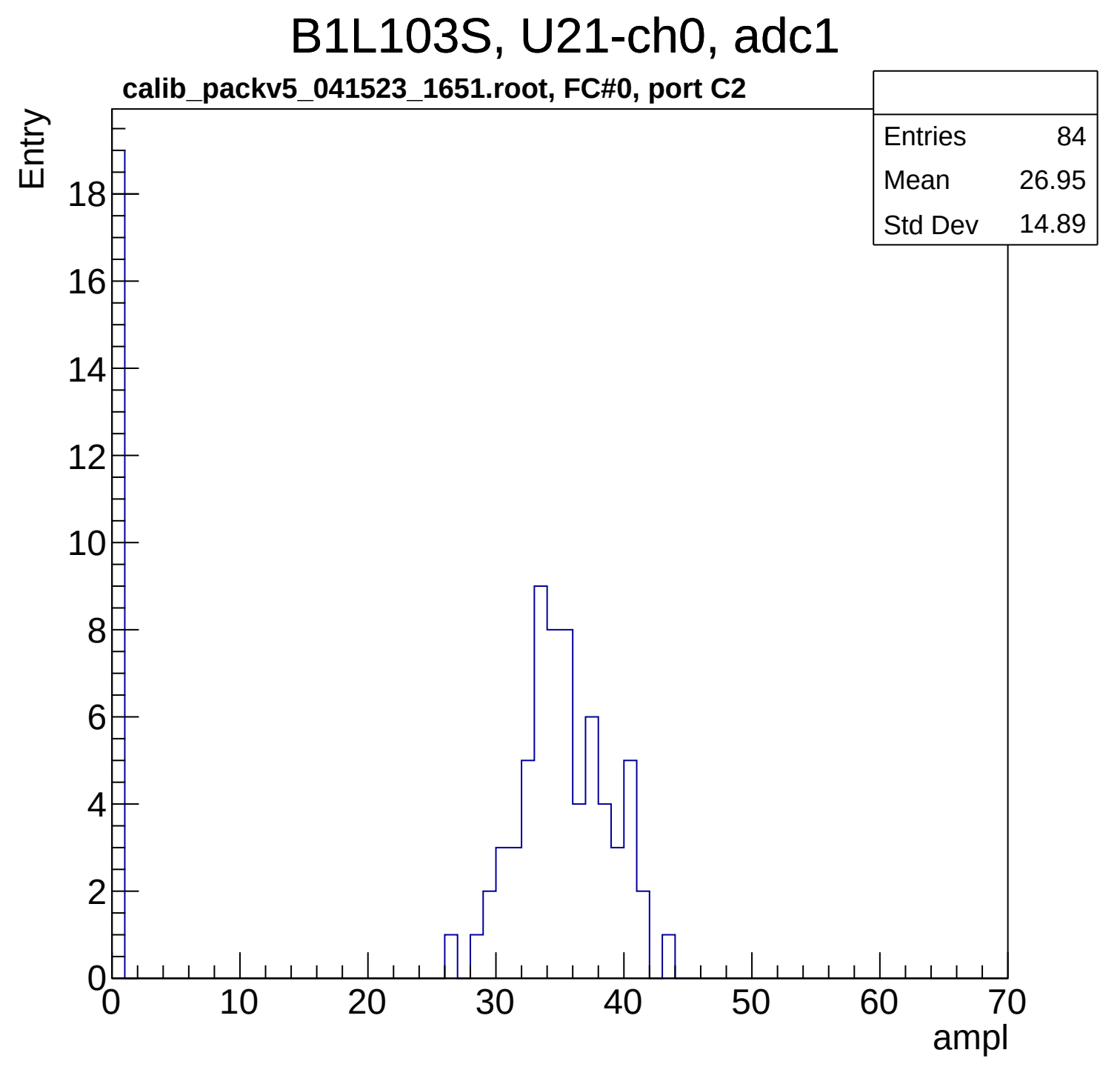
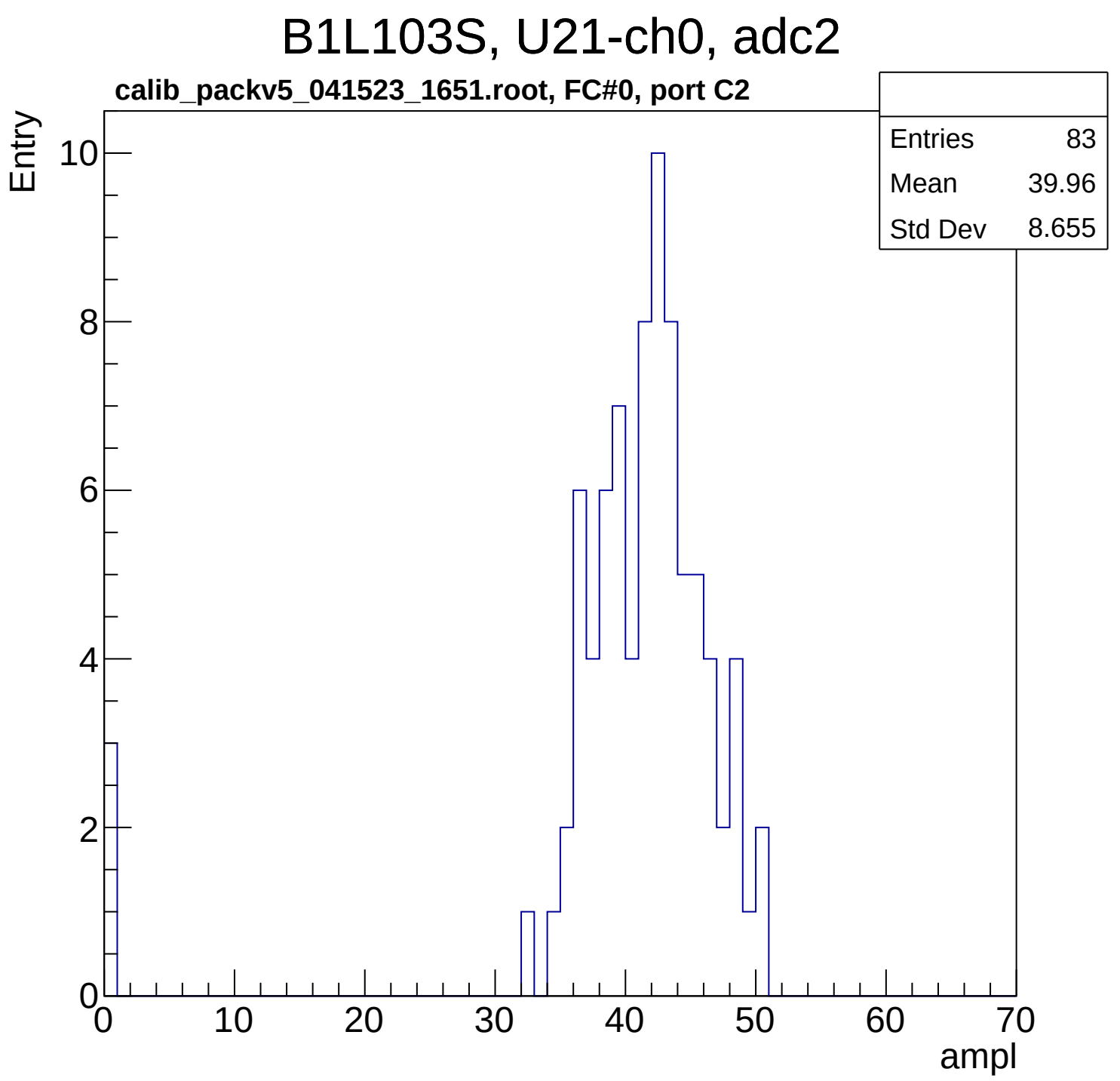
70
ampl


B1L103S, U21-ch0, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 26.95
Std Dev 14.89
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch0, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 39.96
Std Dev 8.655
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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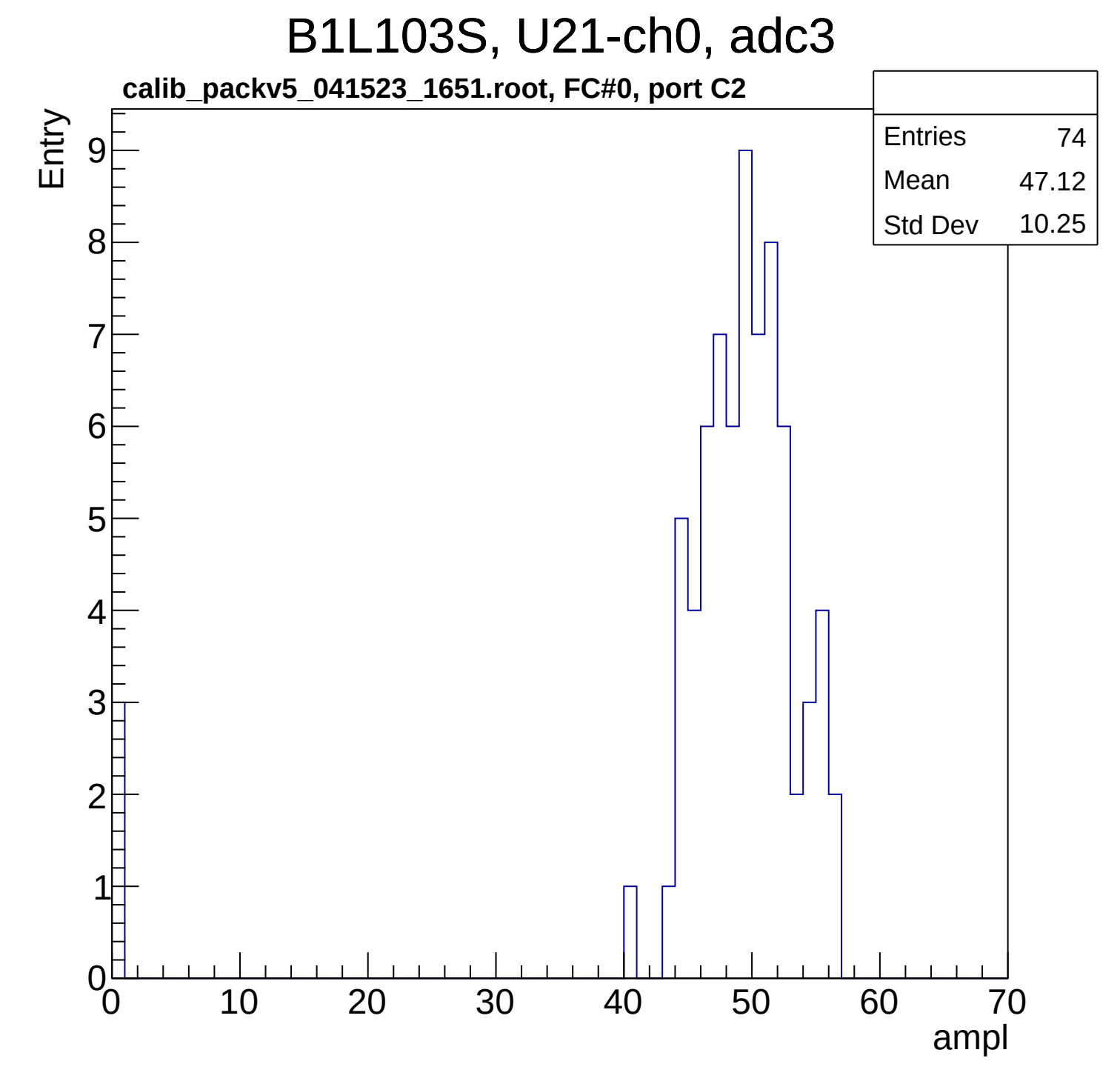
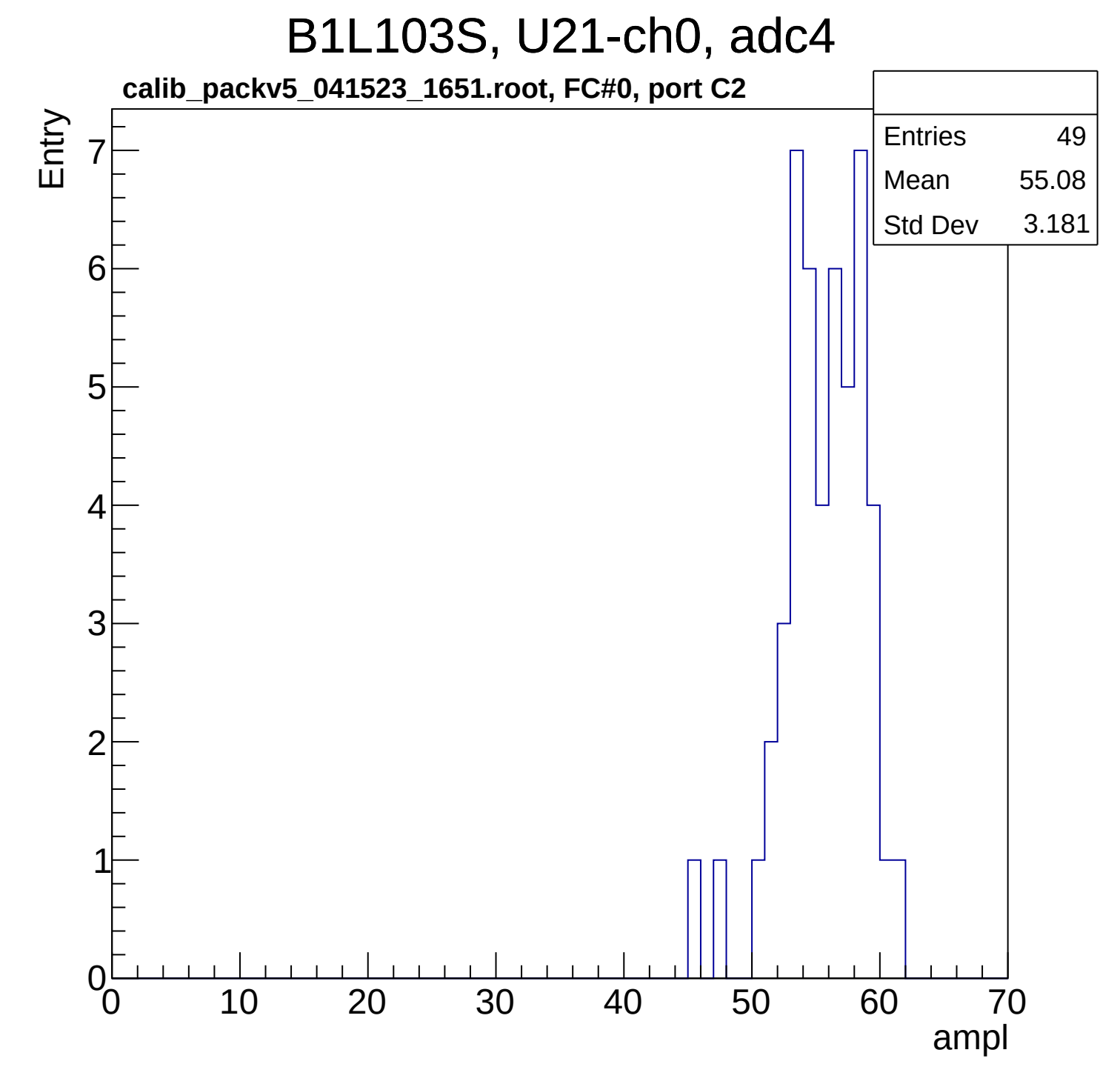

B1L103S, U21-ch0, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 47.12
Std Dev 10.25
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L103S, U21-ch0, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 55.08
Std Dev 3.181
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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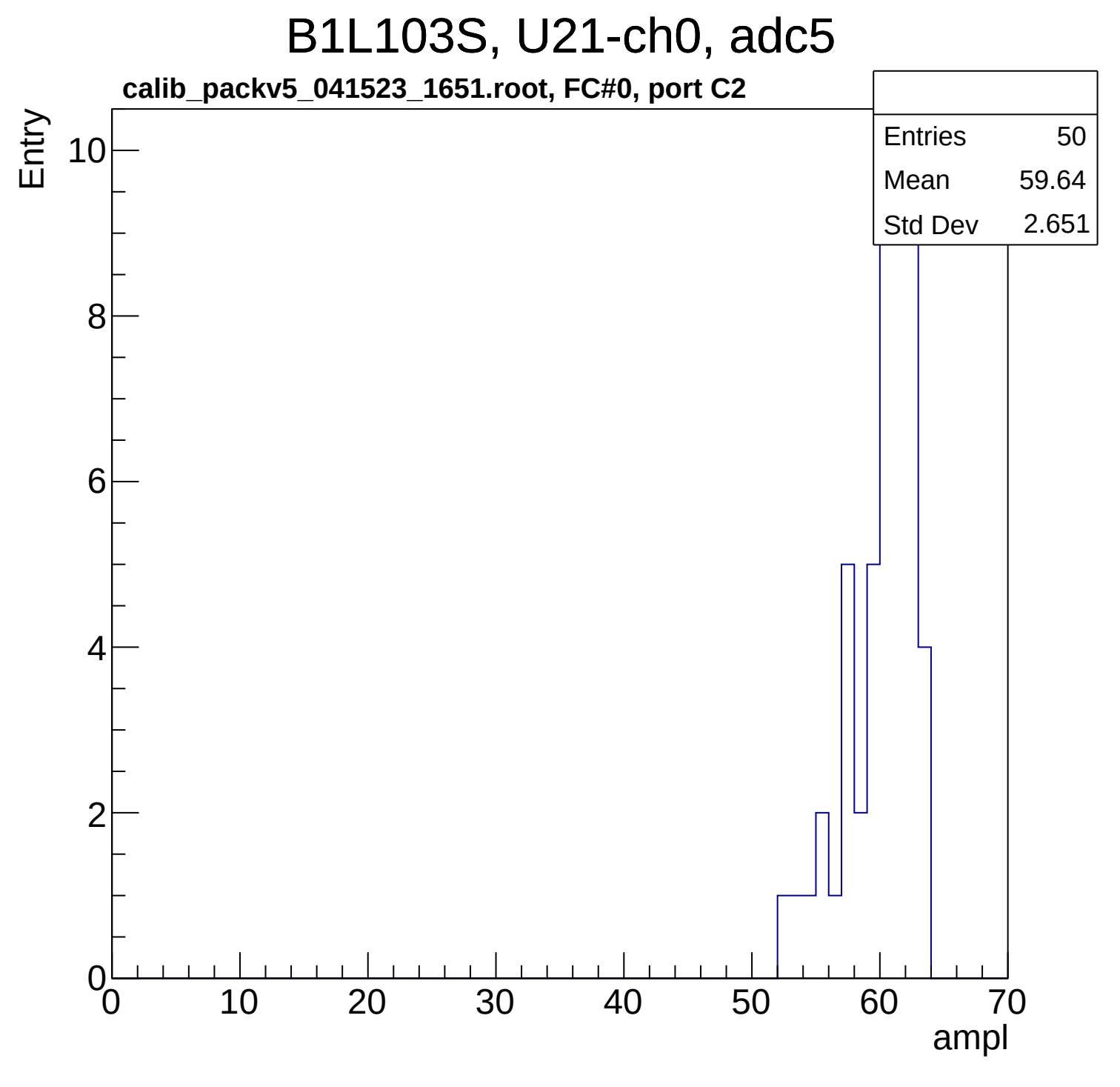
B1L103S, U21-ch0, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 59.64
Std Dev 2.651
Entry
ampl
0
2
4
6
8
10
0
10
20
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40
50
60
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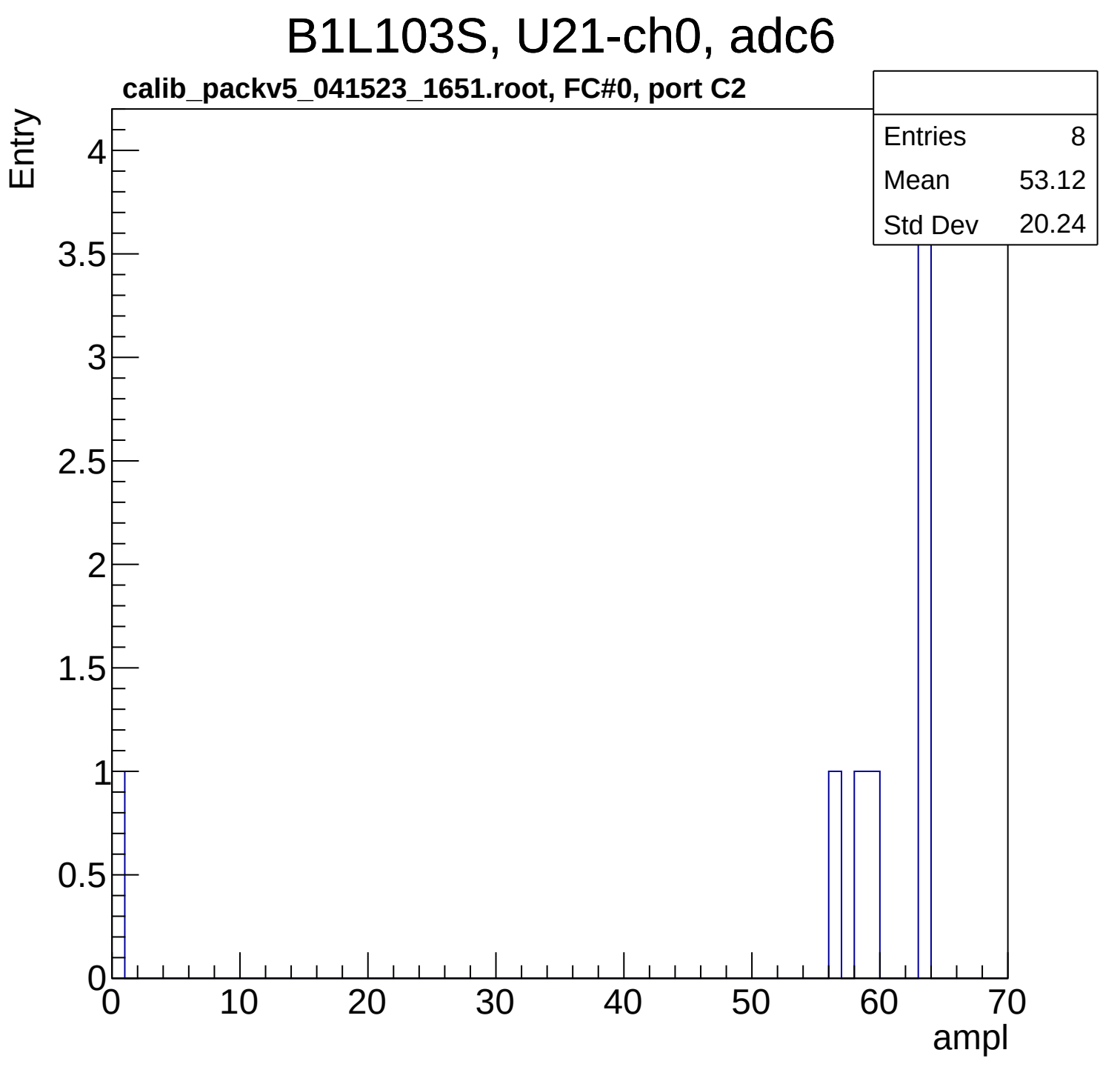
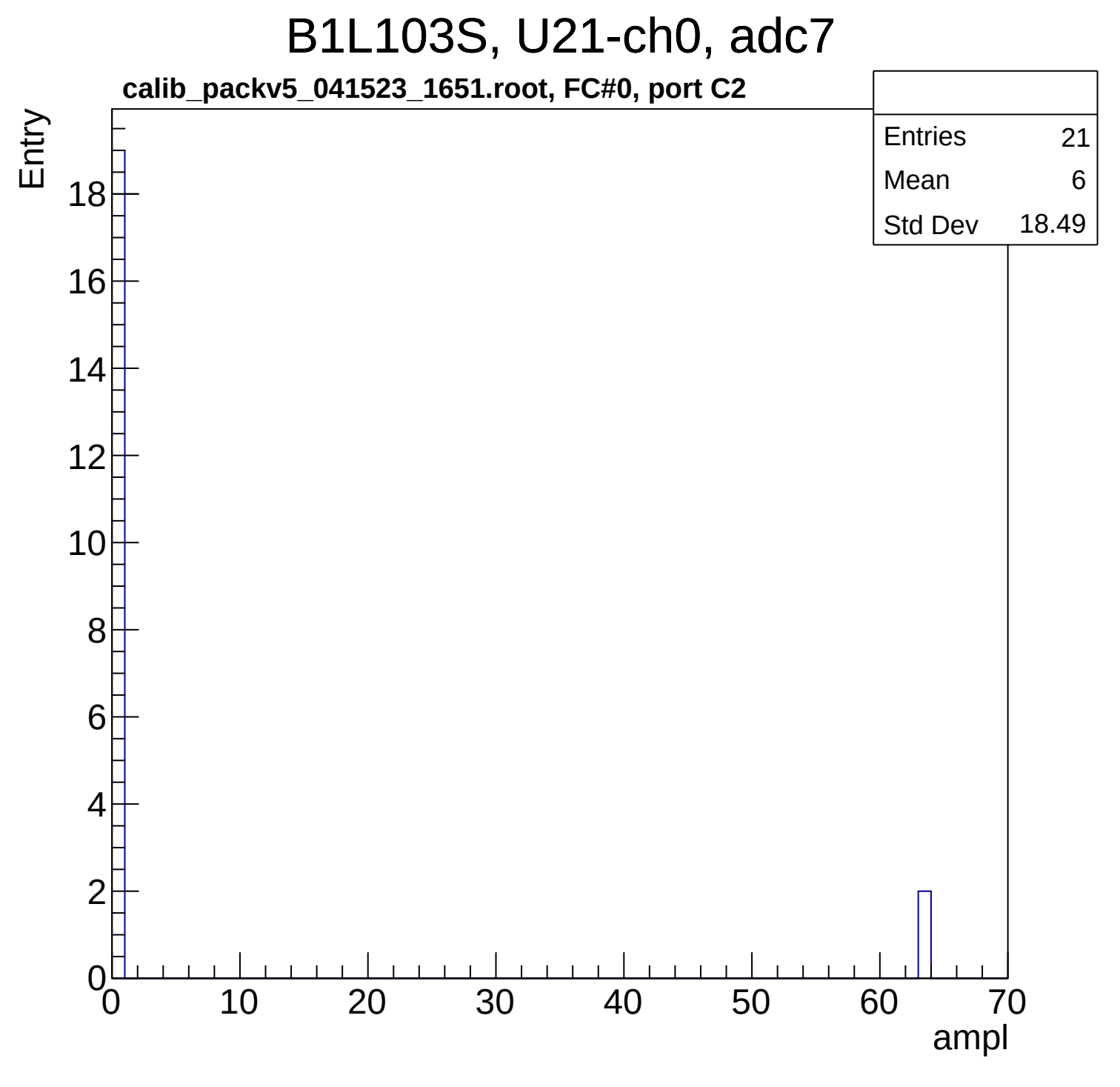

B1L103S, U21-ch0, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 53.12
Std Dev 20.24
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U21-ch0, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 6
Std Dev 18.49
Entry
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6
8
10
12
14
16
18
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10
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30
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50
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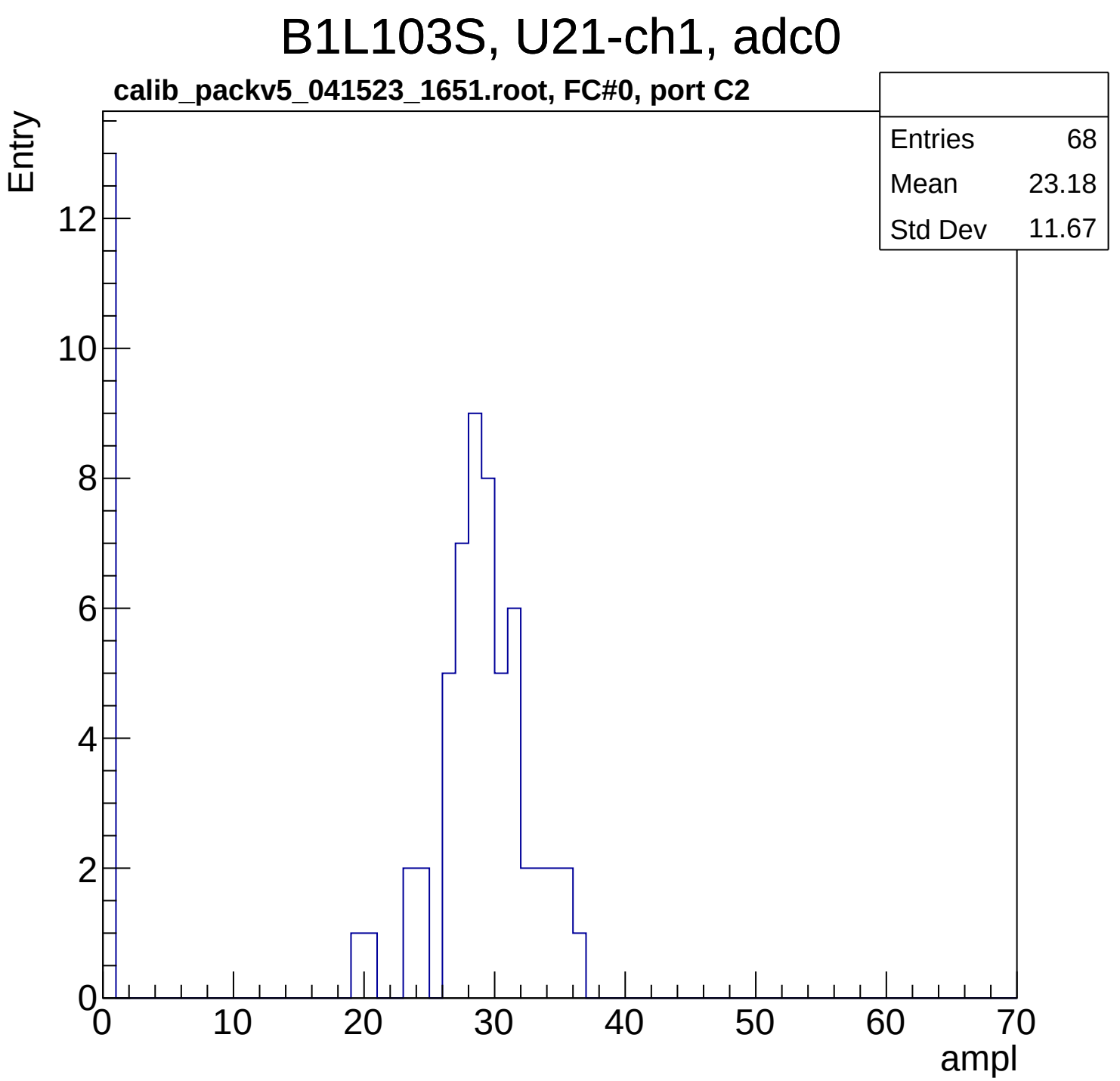
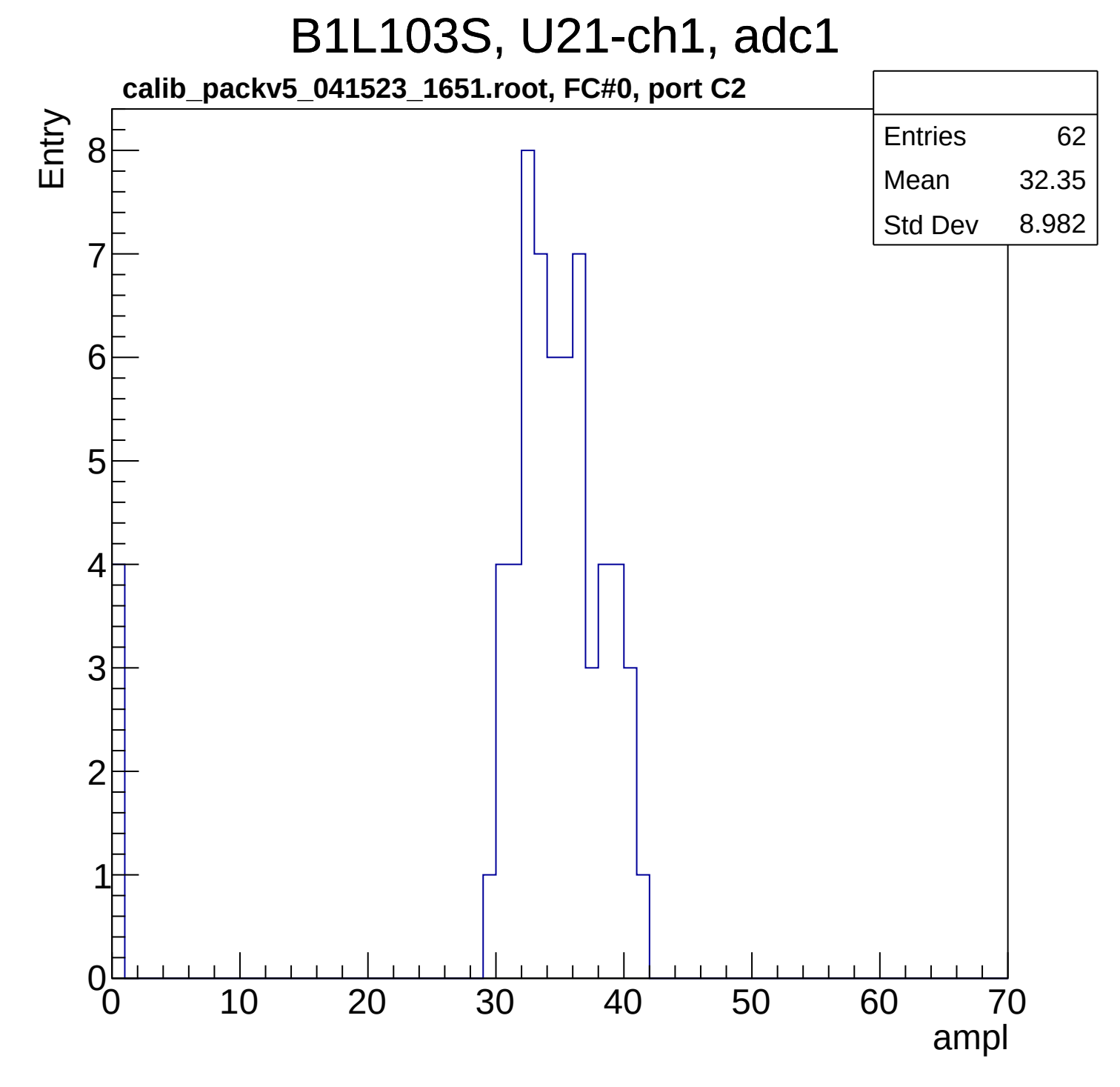
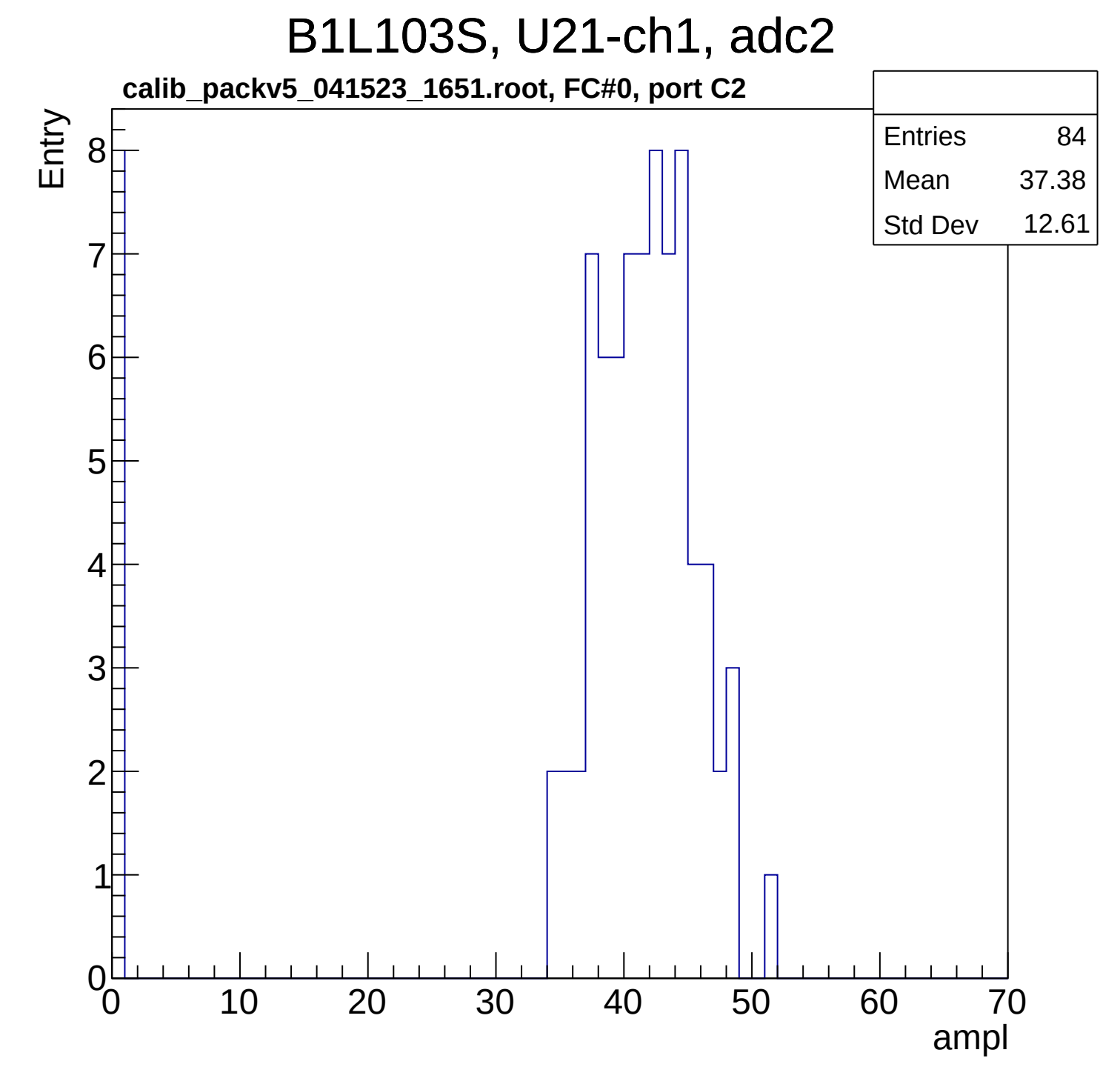
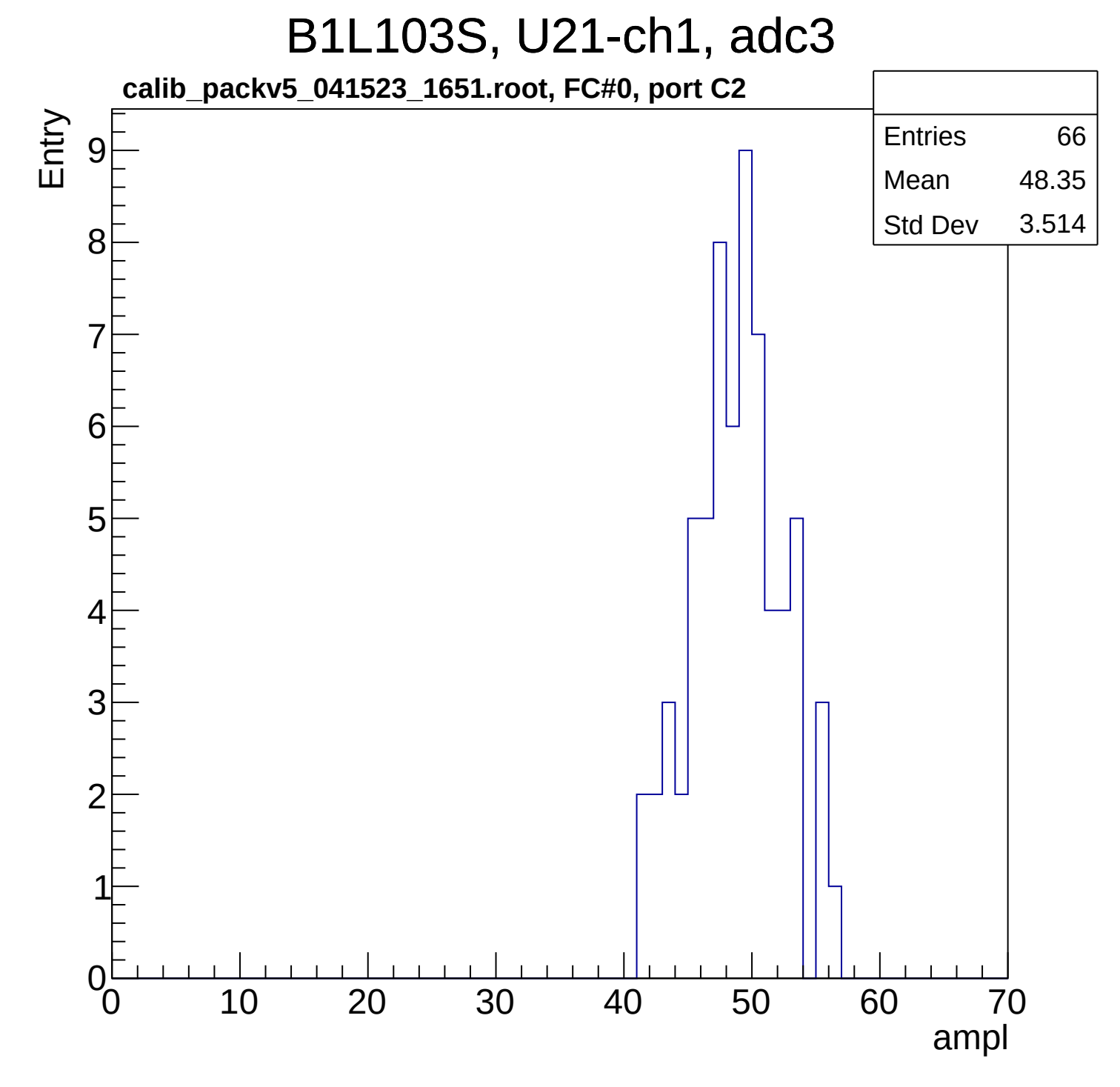
70
ampl


B1L103S, U21-ch1, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 23.18
Std Dev 11.67
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch1, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 32.35
Std Dev 8.982
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch1, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 37.38
Std Dev 12.61
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch1, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 48.35
Std Dev 3.514
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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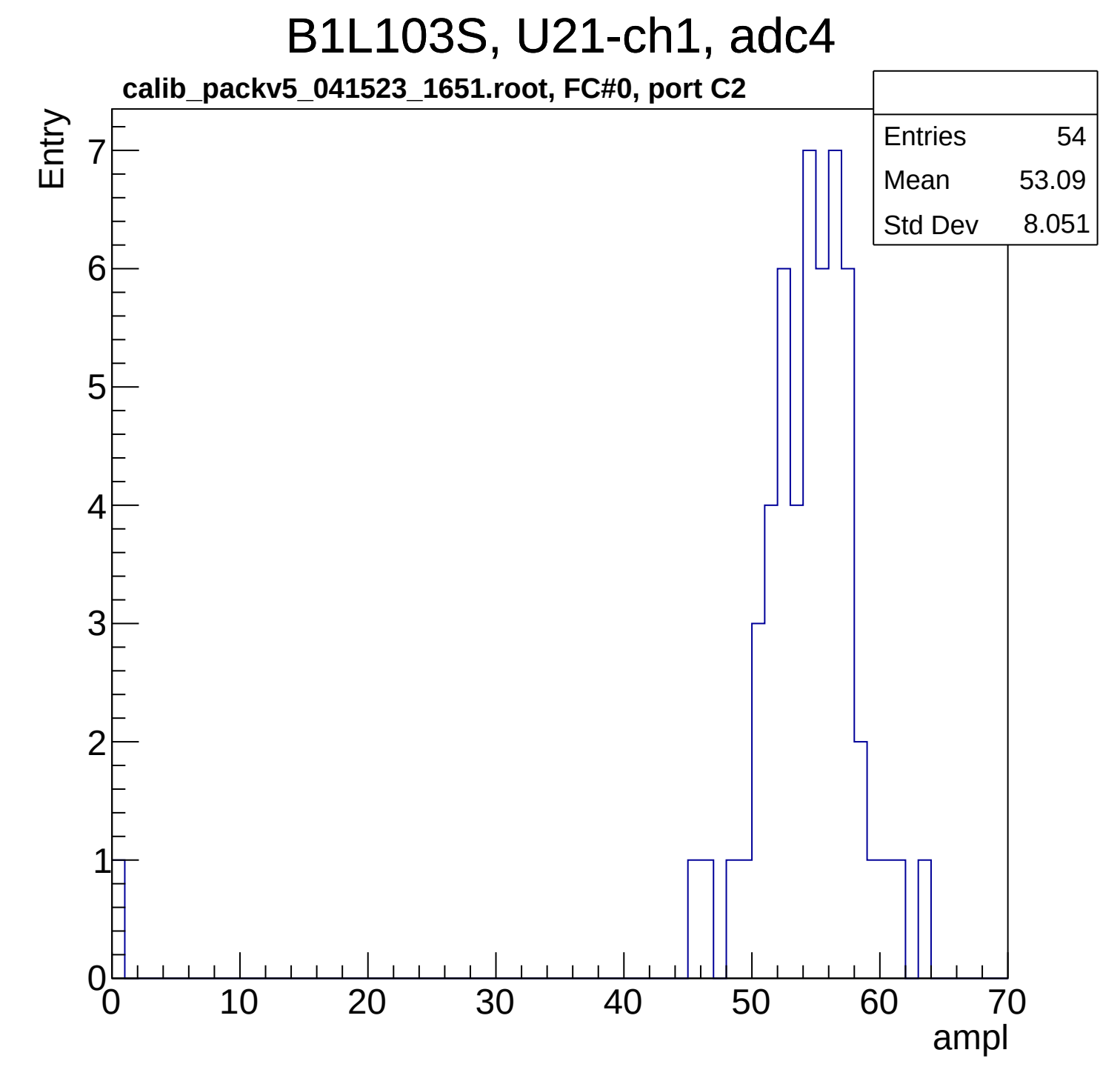
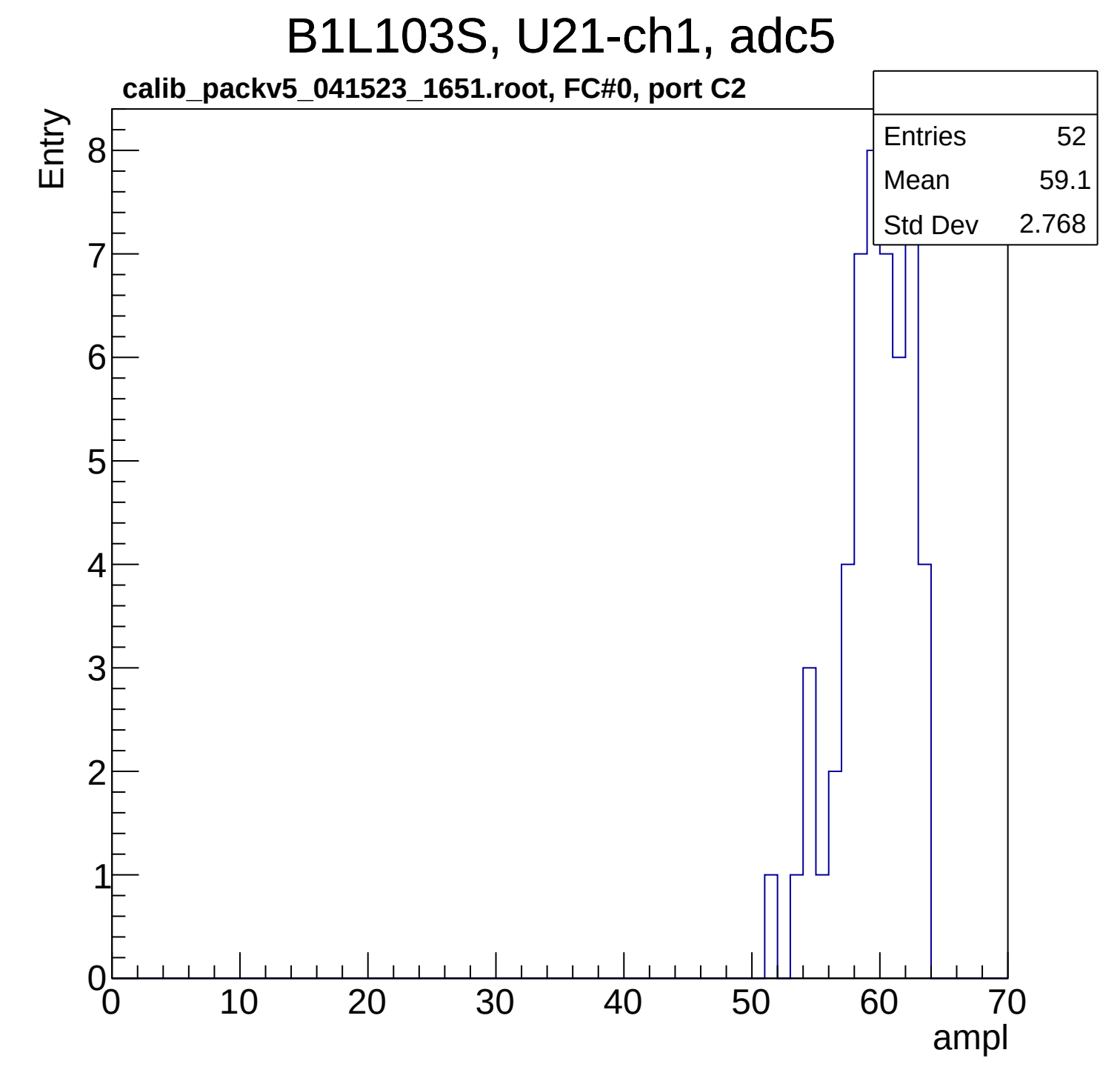
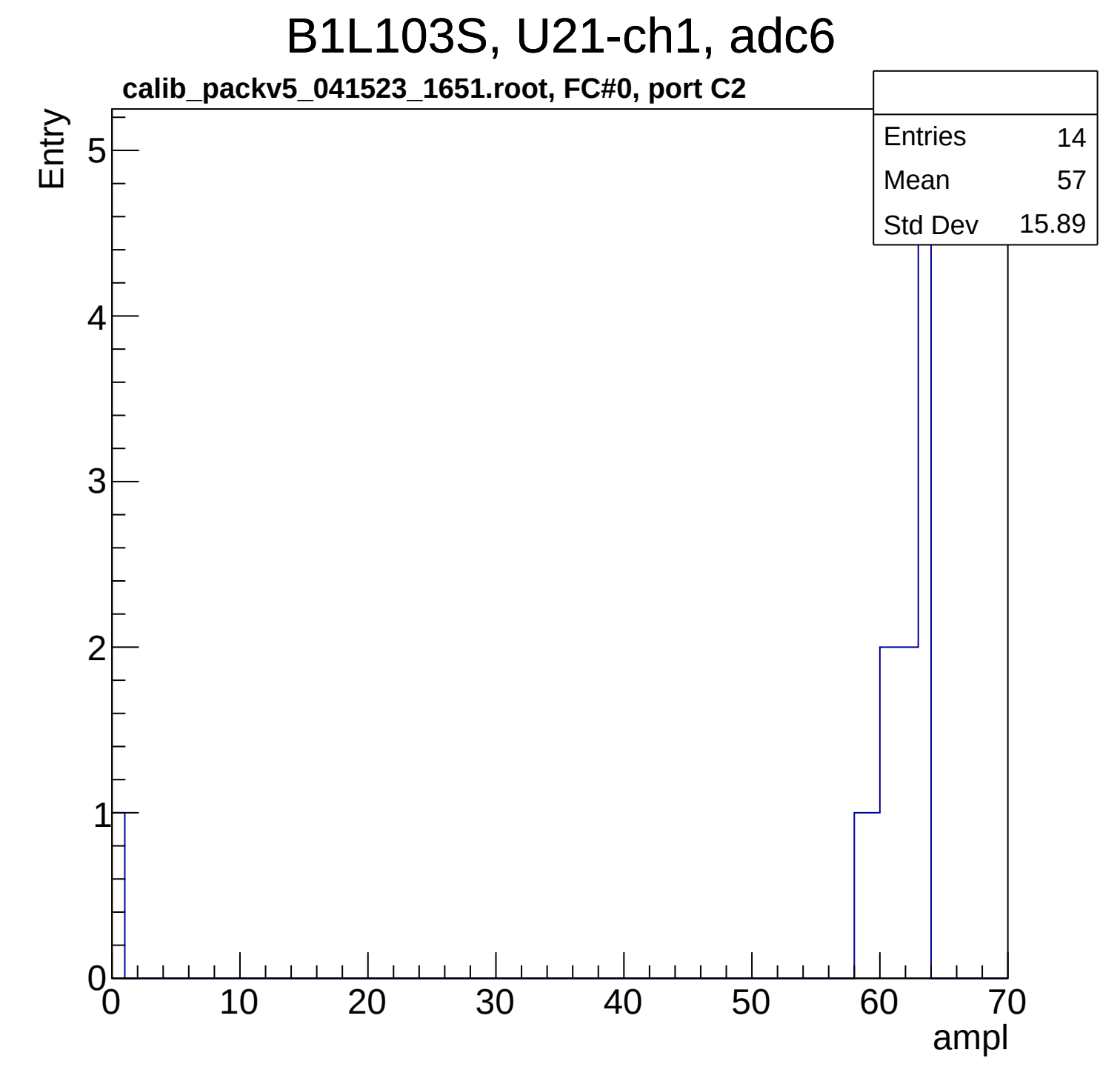
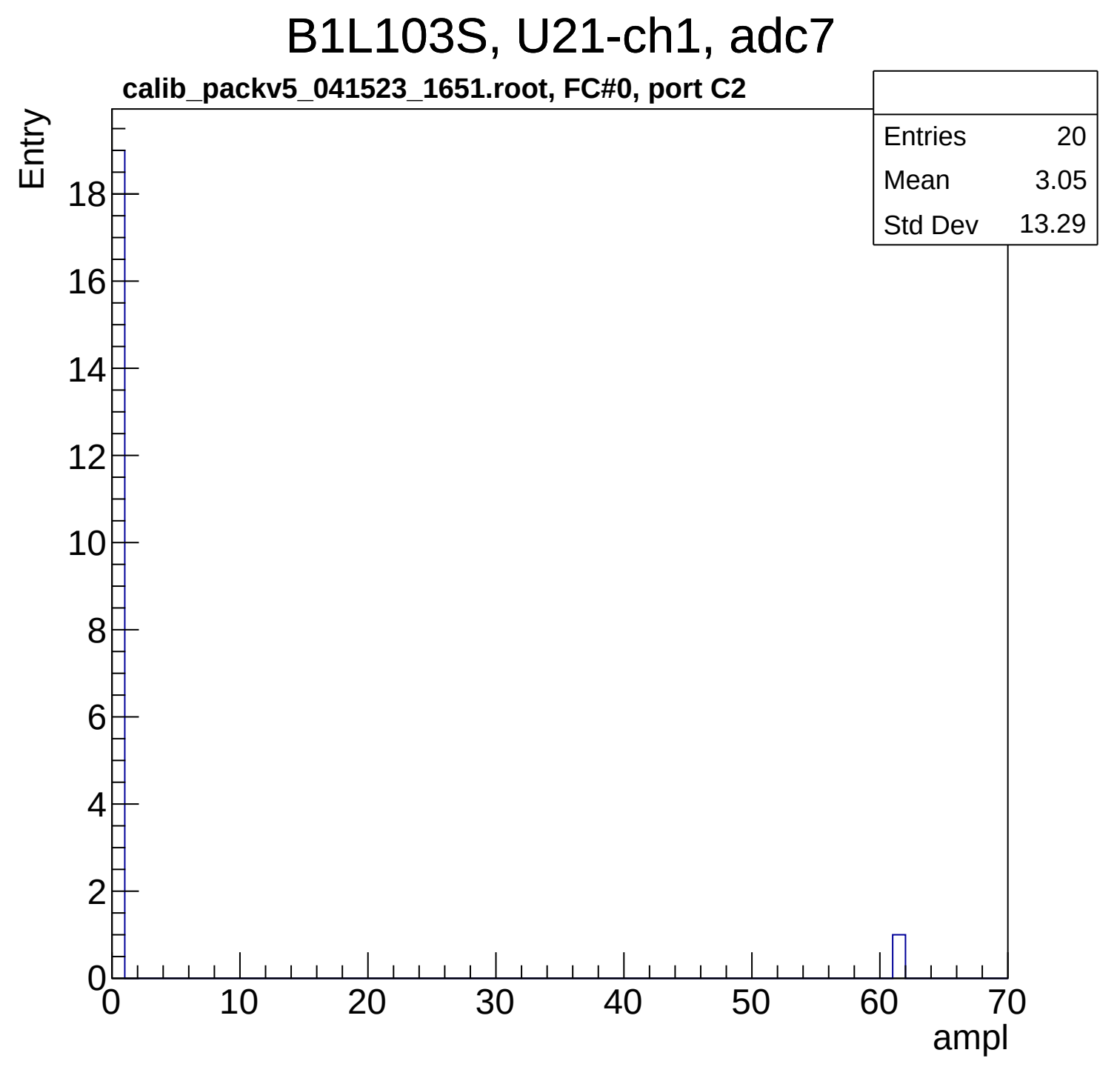
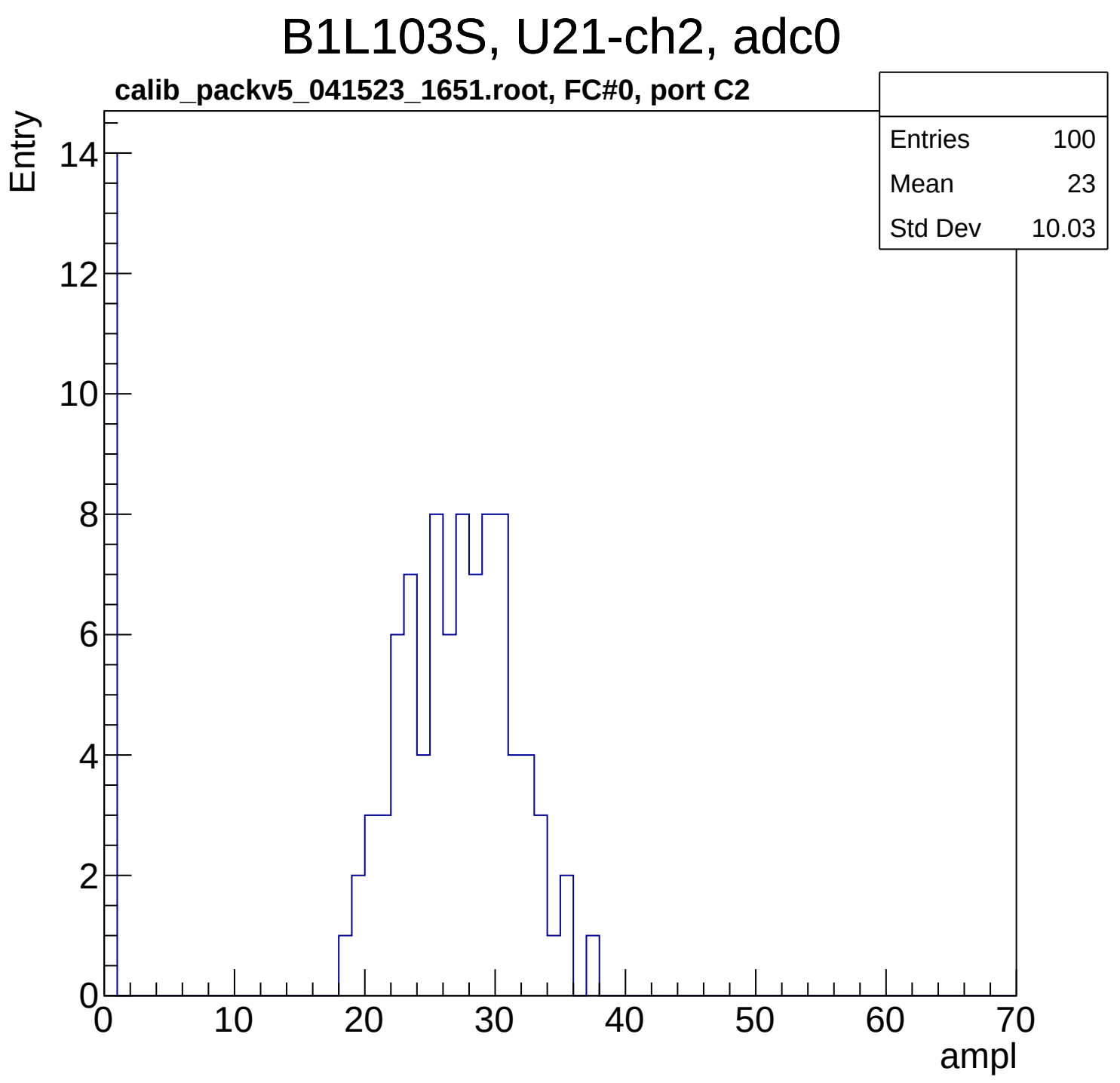

B1L103S, U21-ch1, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 53.09
Std Dev 8.051
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U21-ch1, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 59.1
Std Dev 2.768
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch1, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 57
Std Dev 15.89
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch1, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.05
Std Dev 13.29
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch2, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 100
Mean 23
Std Dev 10.03
Entry
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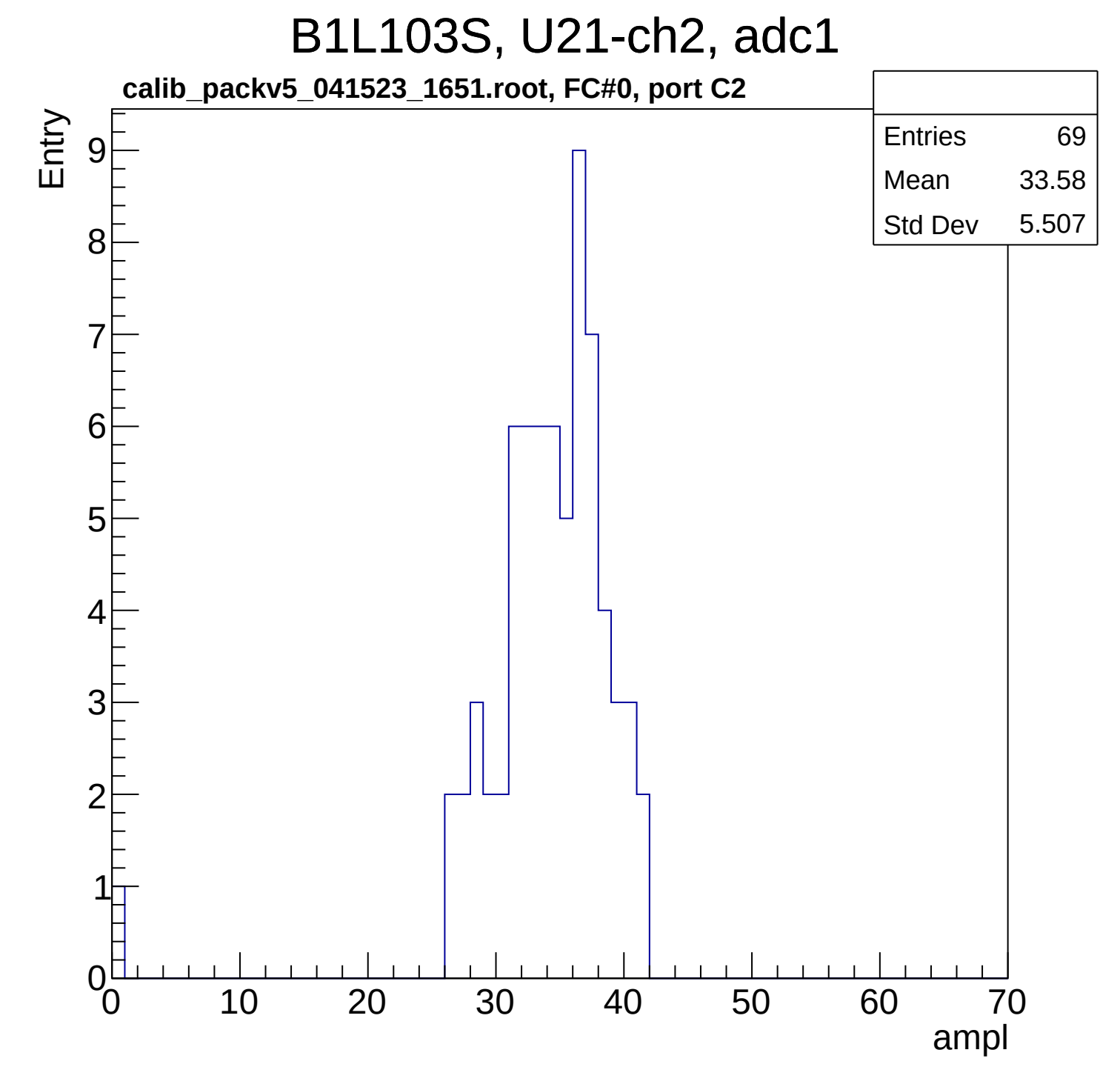
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch2, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 33.58
Std Dev 5.507
Entry
ampl
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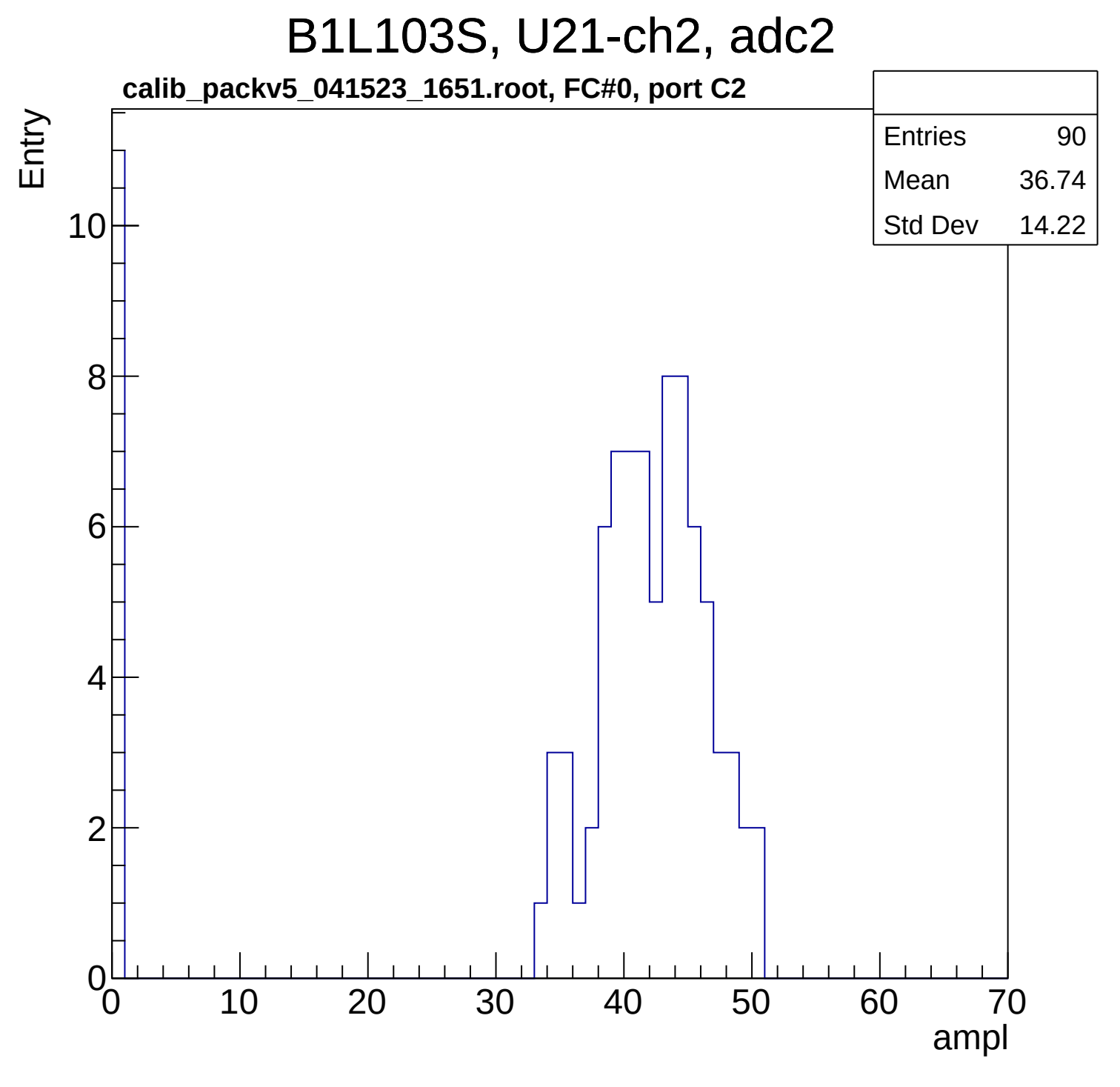
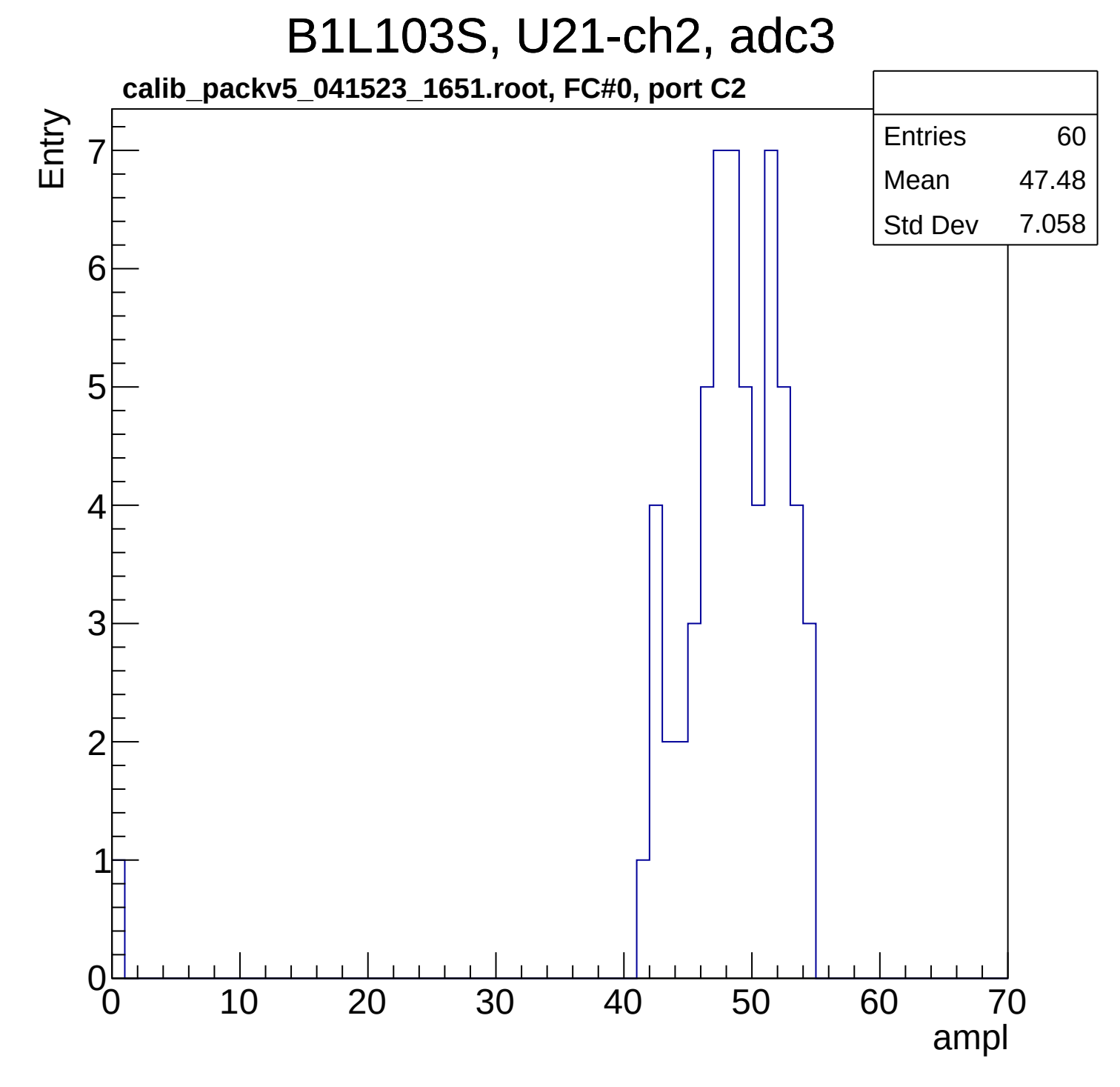
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch2, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 36.74
Std Dev 14.22
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch2, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 47.48
Std Dev 7.058
Entry
ampl
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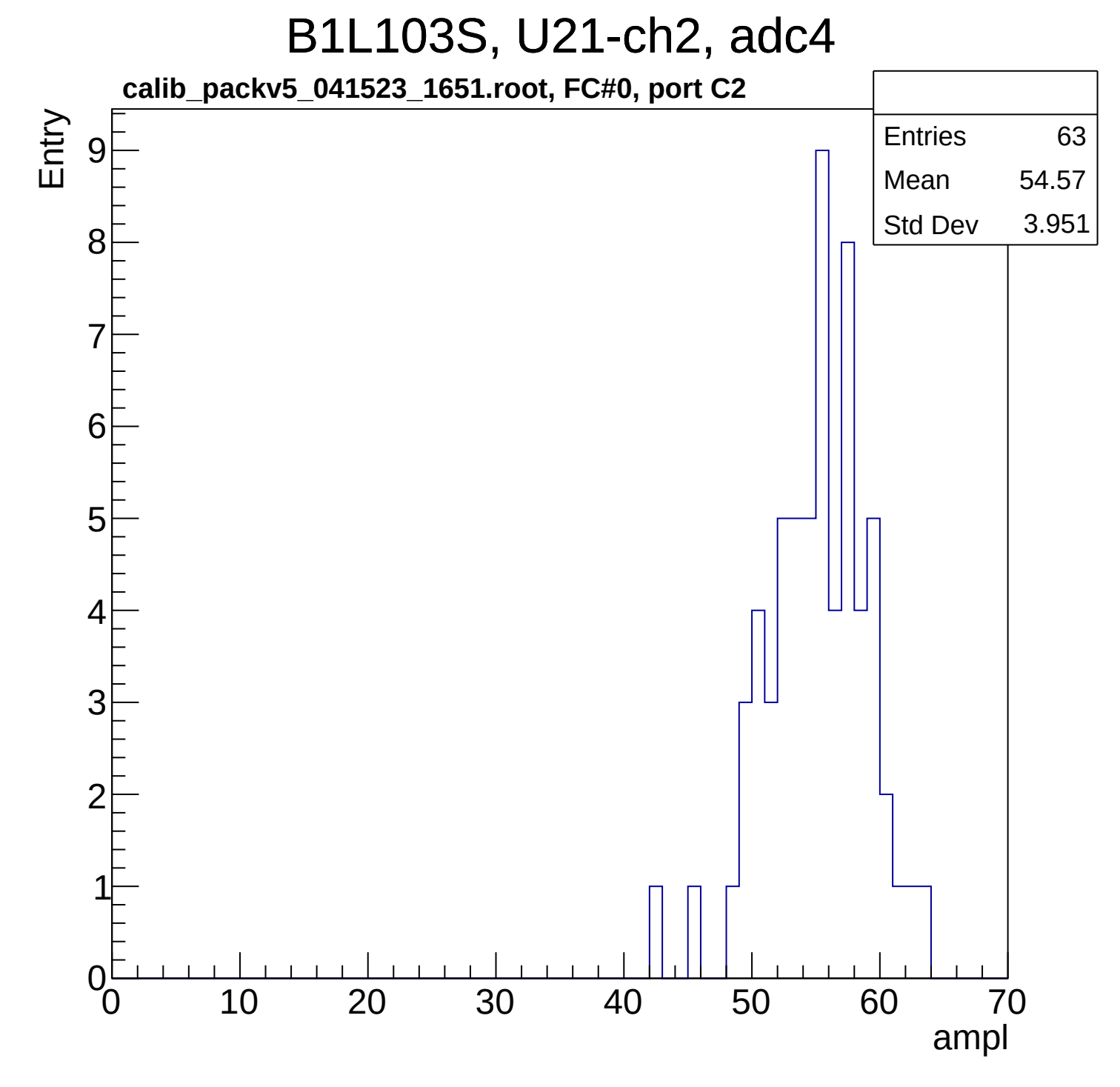
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U21-ch2, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 54.57
Std Dev 3.951
Entry
ampl
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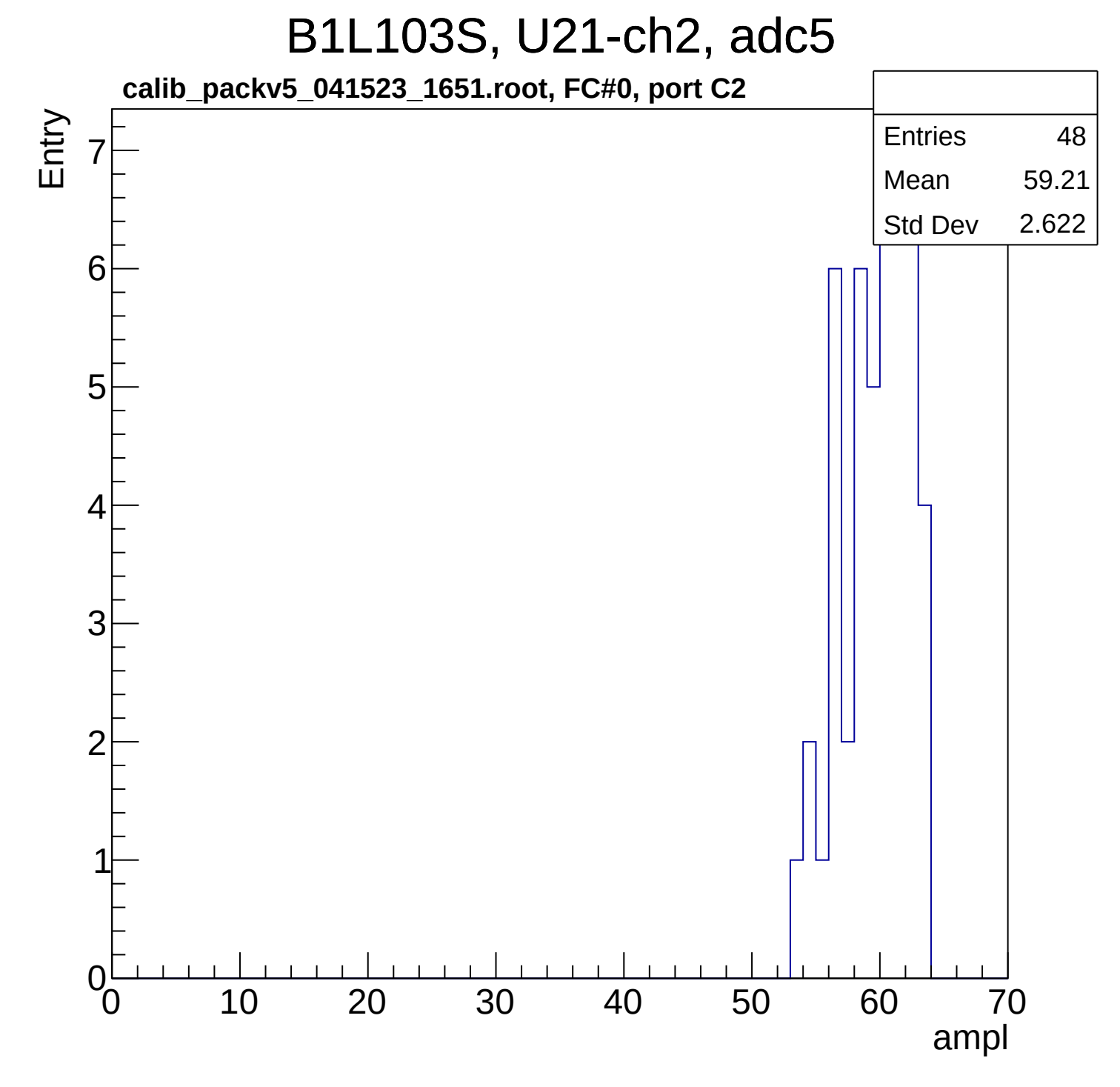
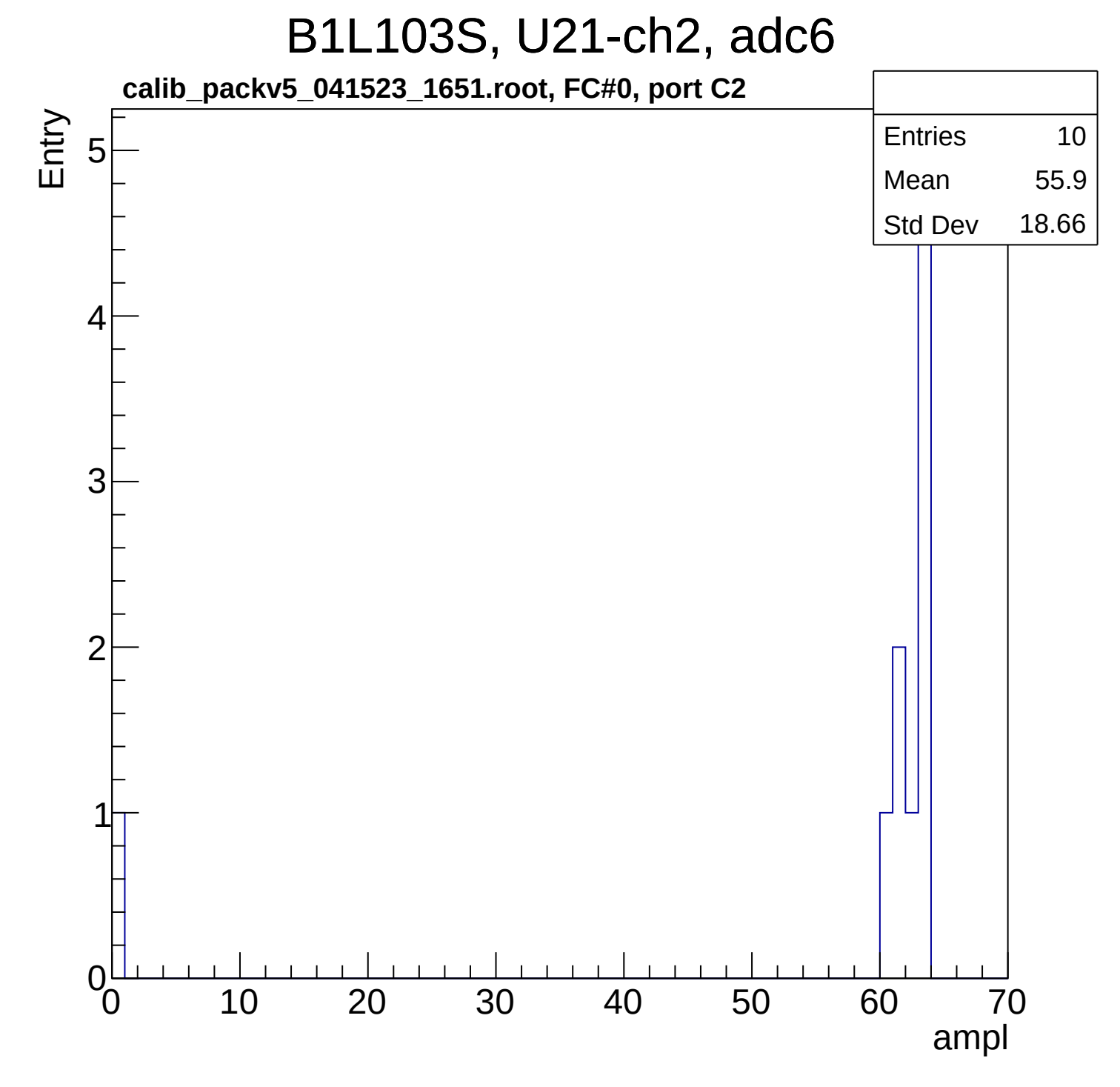
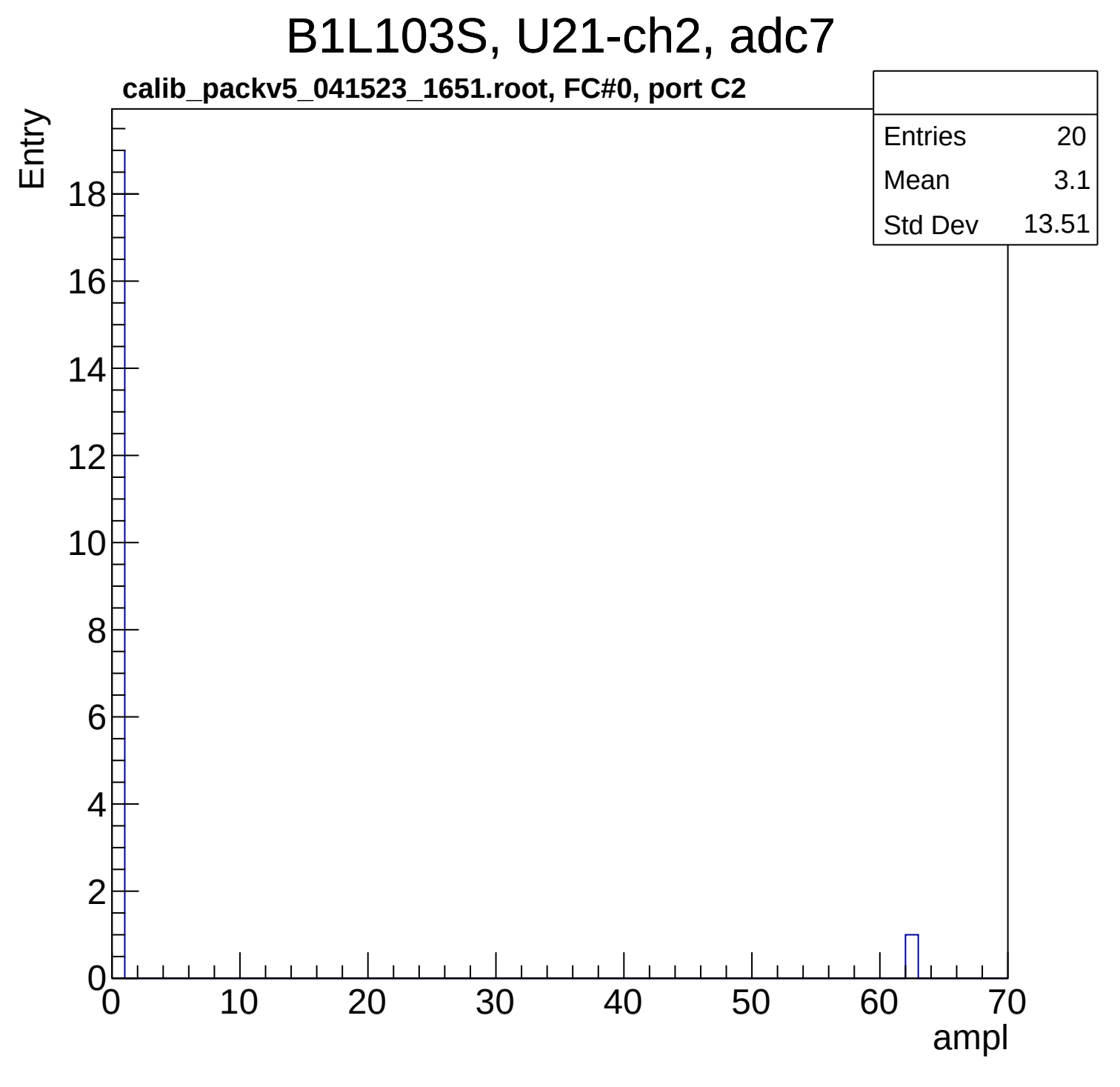
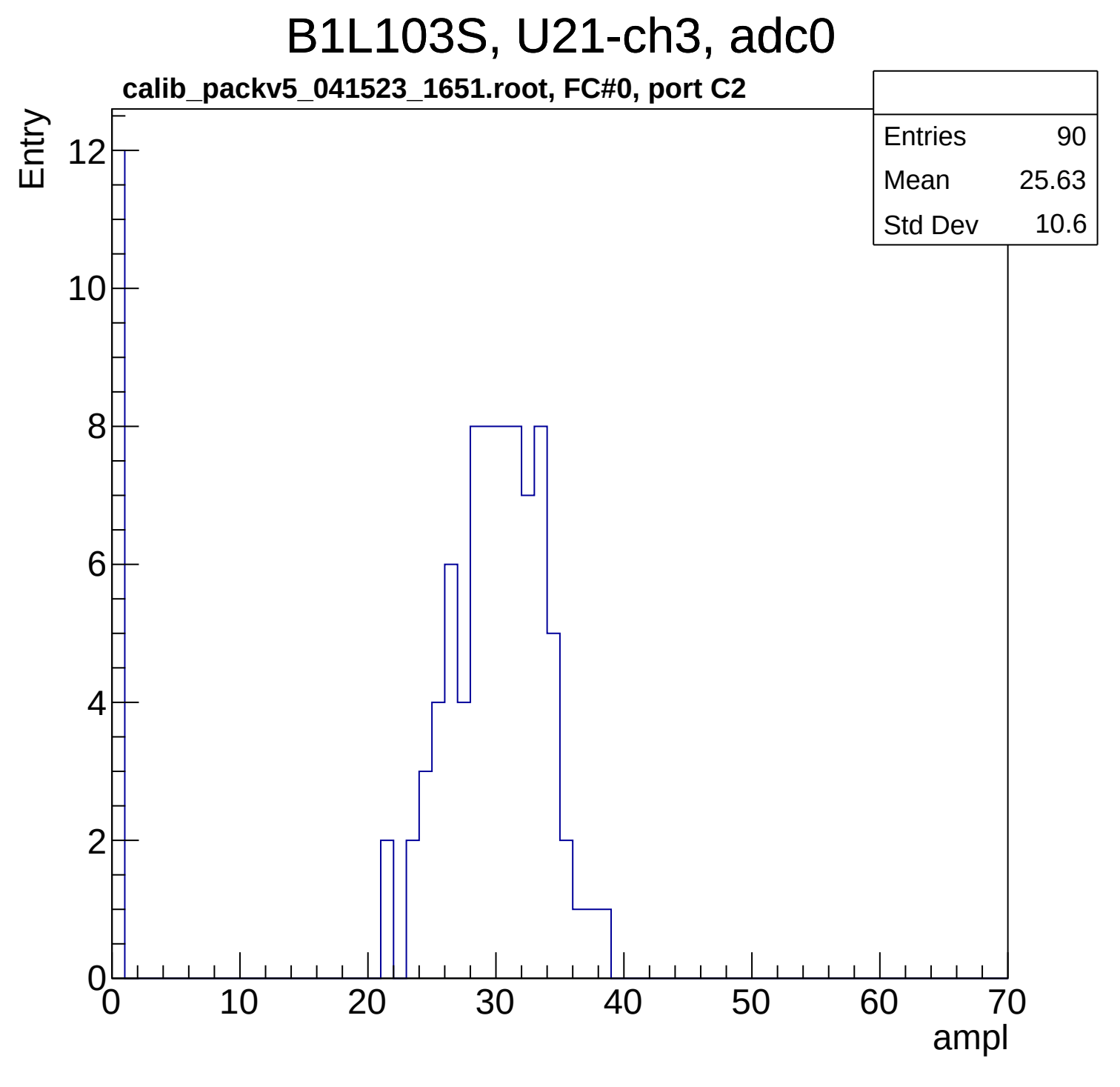
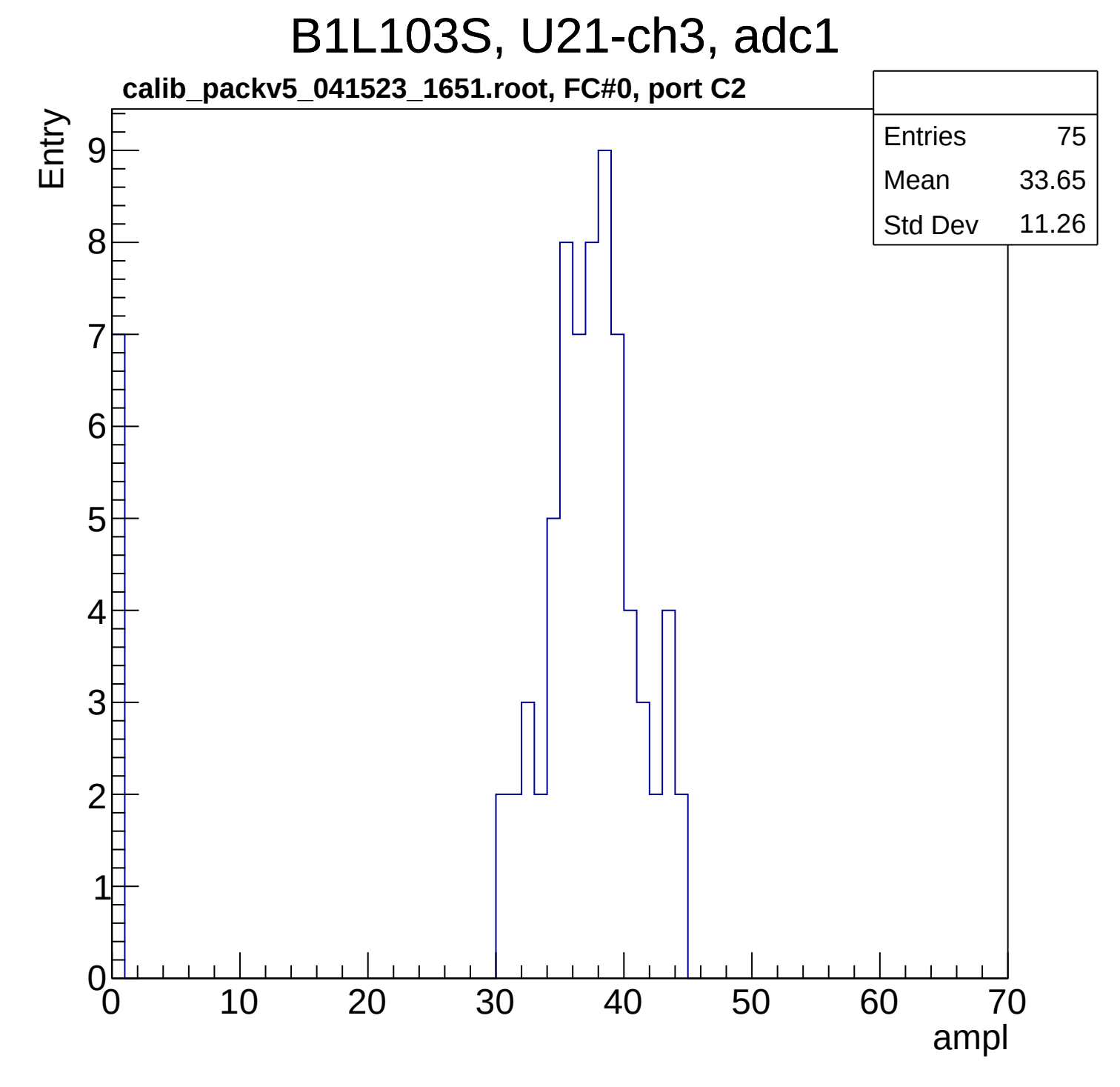
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch2, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 59.21
Std Dev 2.622
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U21-ch2, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 55.9
Std Dev 18.66
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U21-ch2, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch3, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 25.63
Std Dev 10.6
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch3, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 33.65
Std Dev 11.26
Entry
ampl
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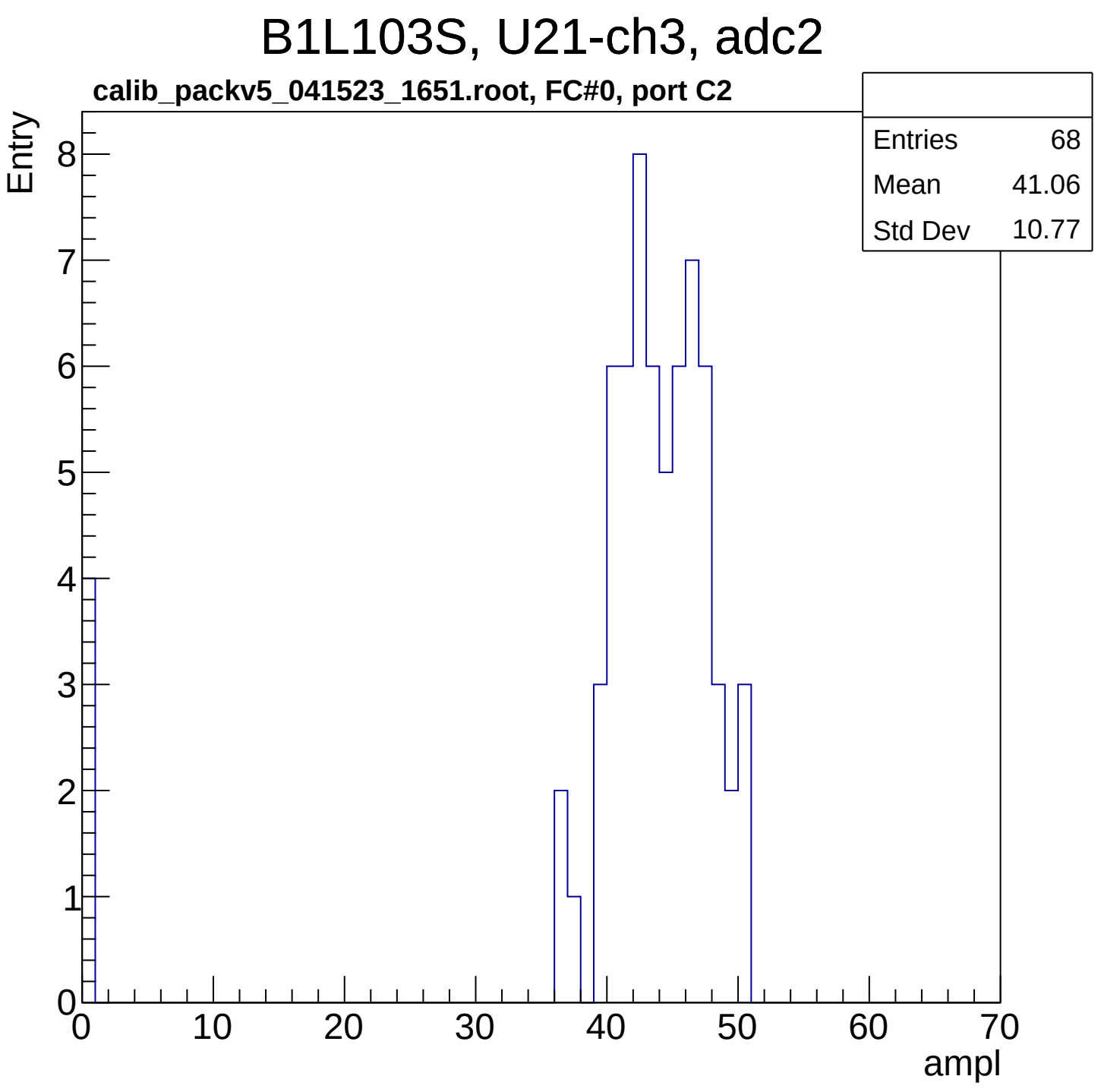
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch3, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 41.06
Std Dev 10.77
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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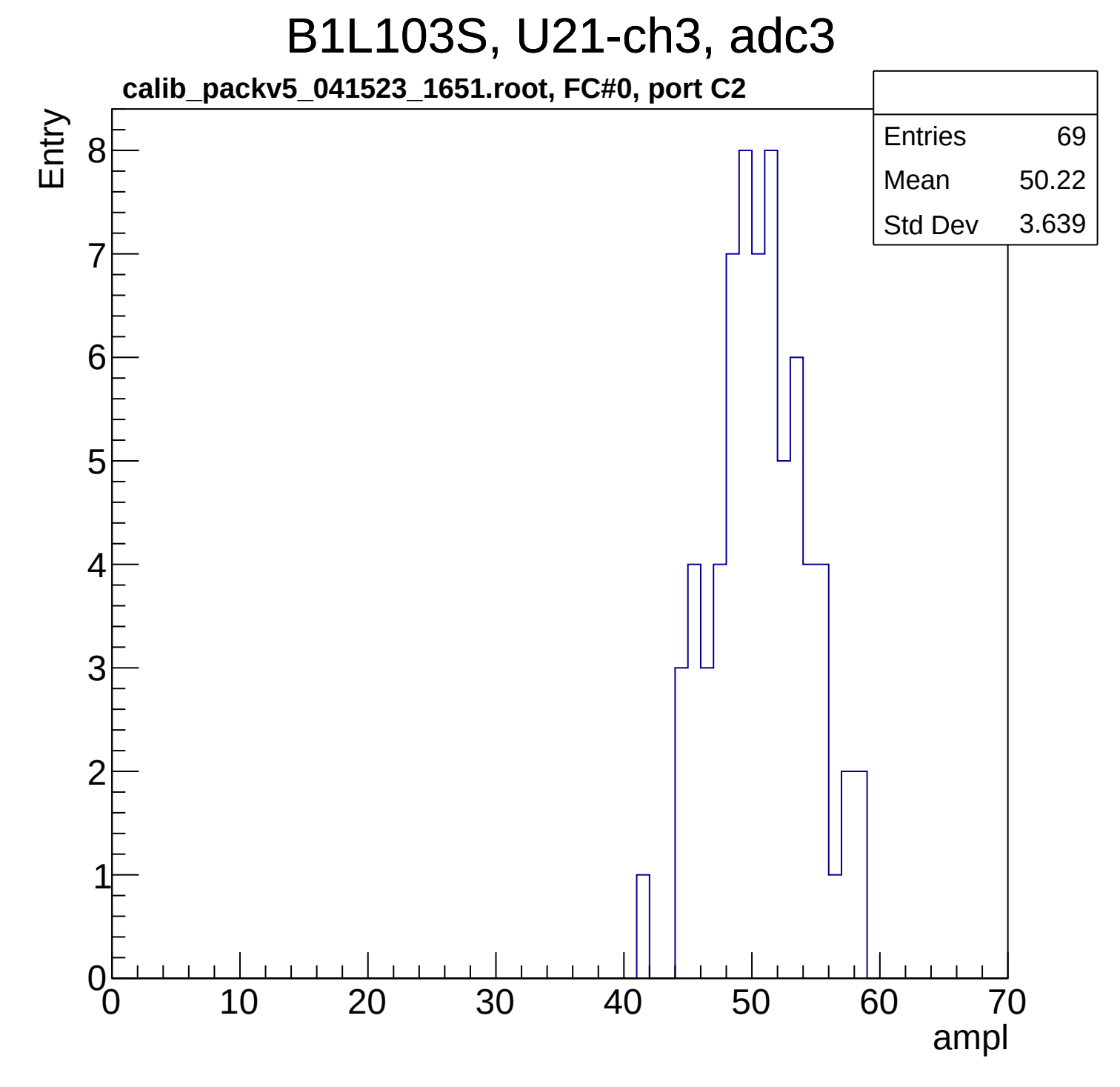
40
50
60
70


B1L103S, U21-ch3, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 50.22
Std Dev 3.639
Entry
ampl
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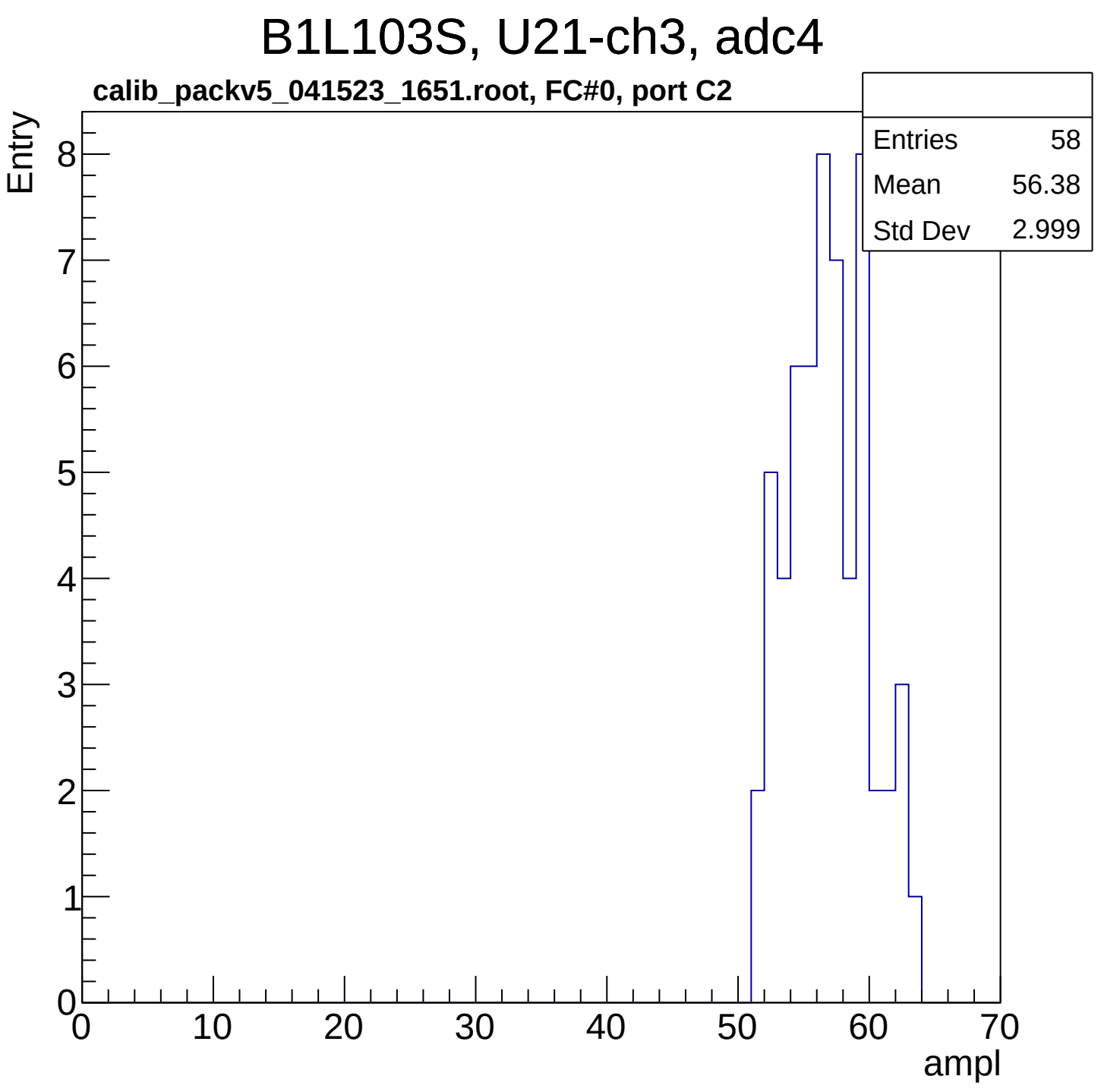
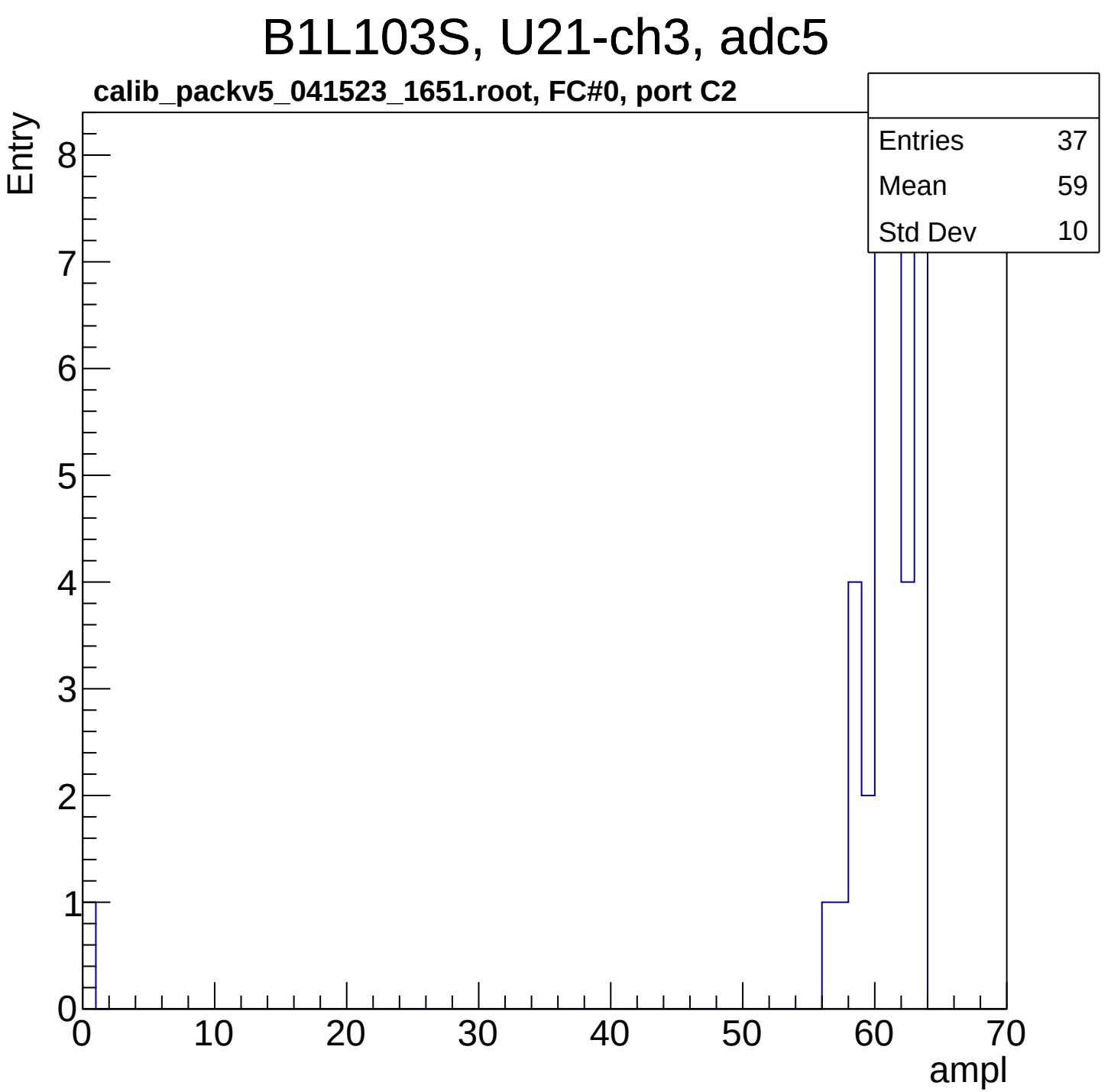
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch3, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 56.38
Std Dev 2.999
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch3, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 59
Std Dev 10
Entry
ampl
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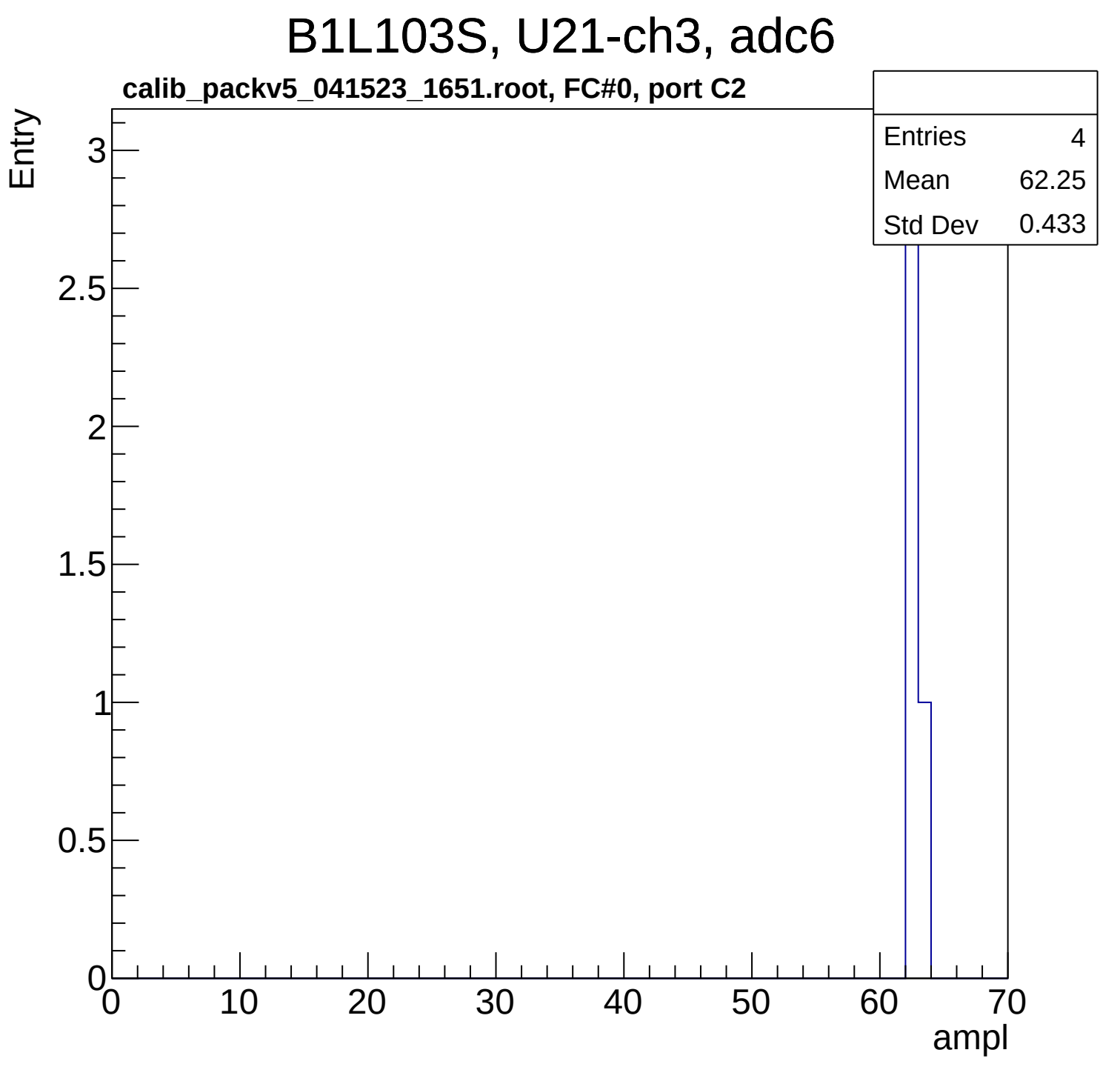
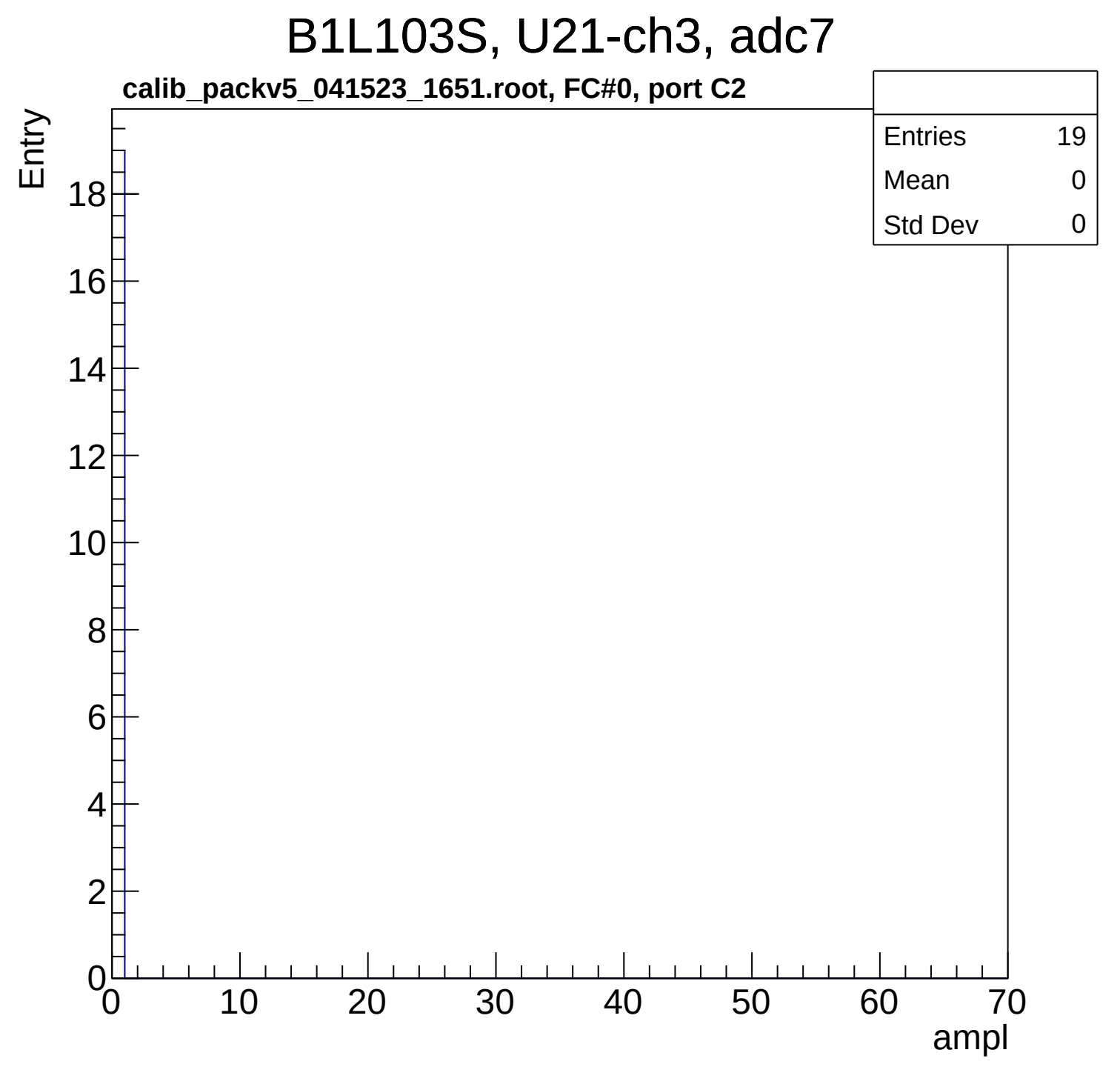
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch3, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 62.25
Std Dev 0.433
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U21-ch3, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
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10
20
30
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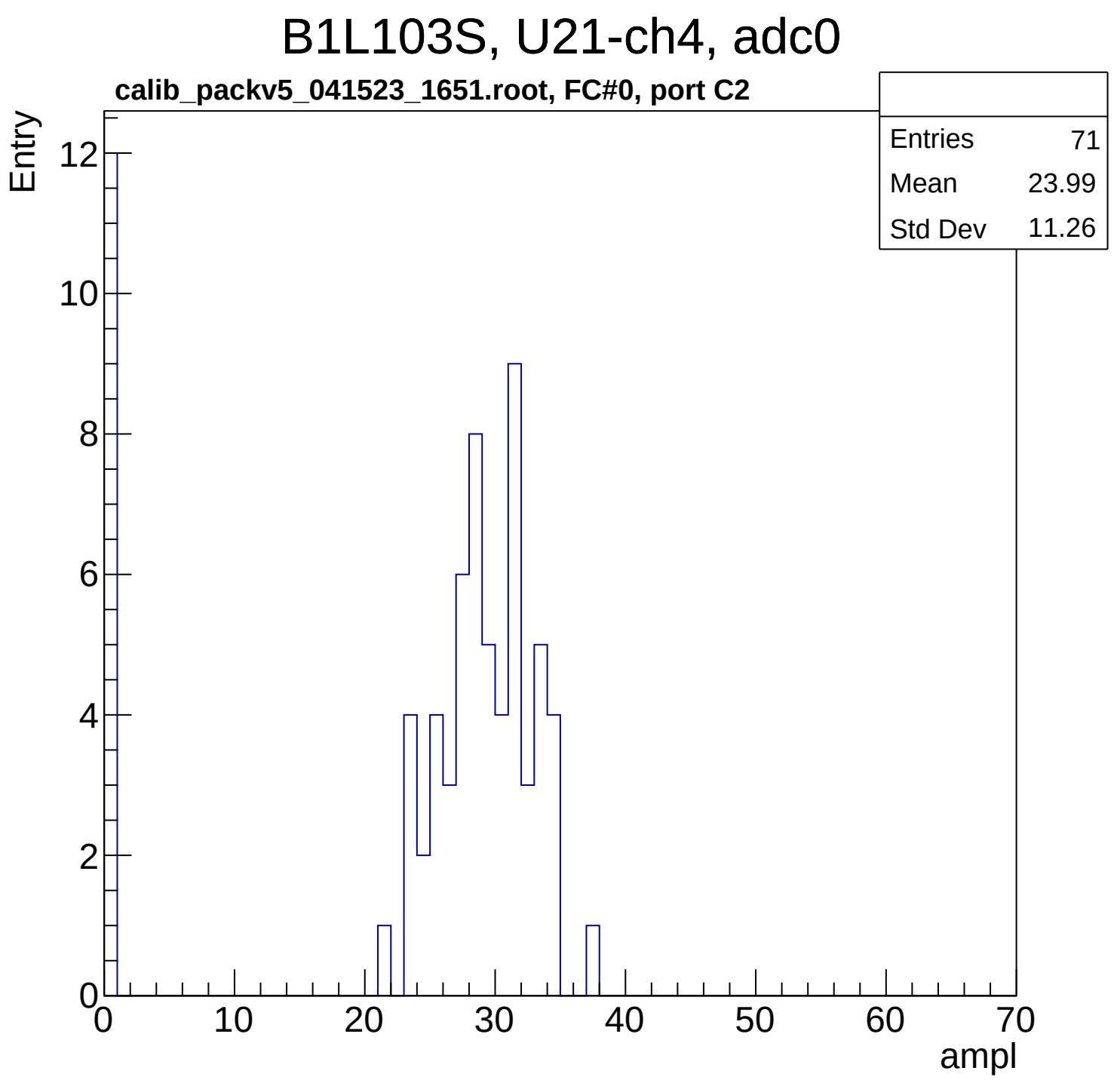
50
60
70
ampl


B1L103S, U21-ch4, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 23.99
Std Dev 11.26
Entry
0
2
4
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8
10
12
0
10
20
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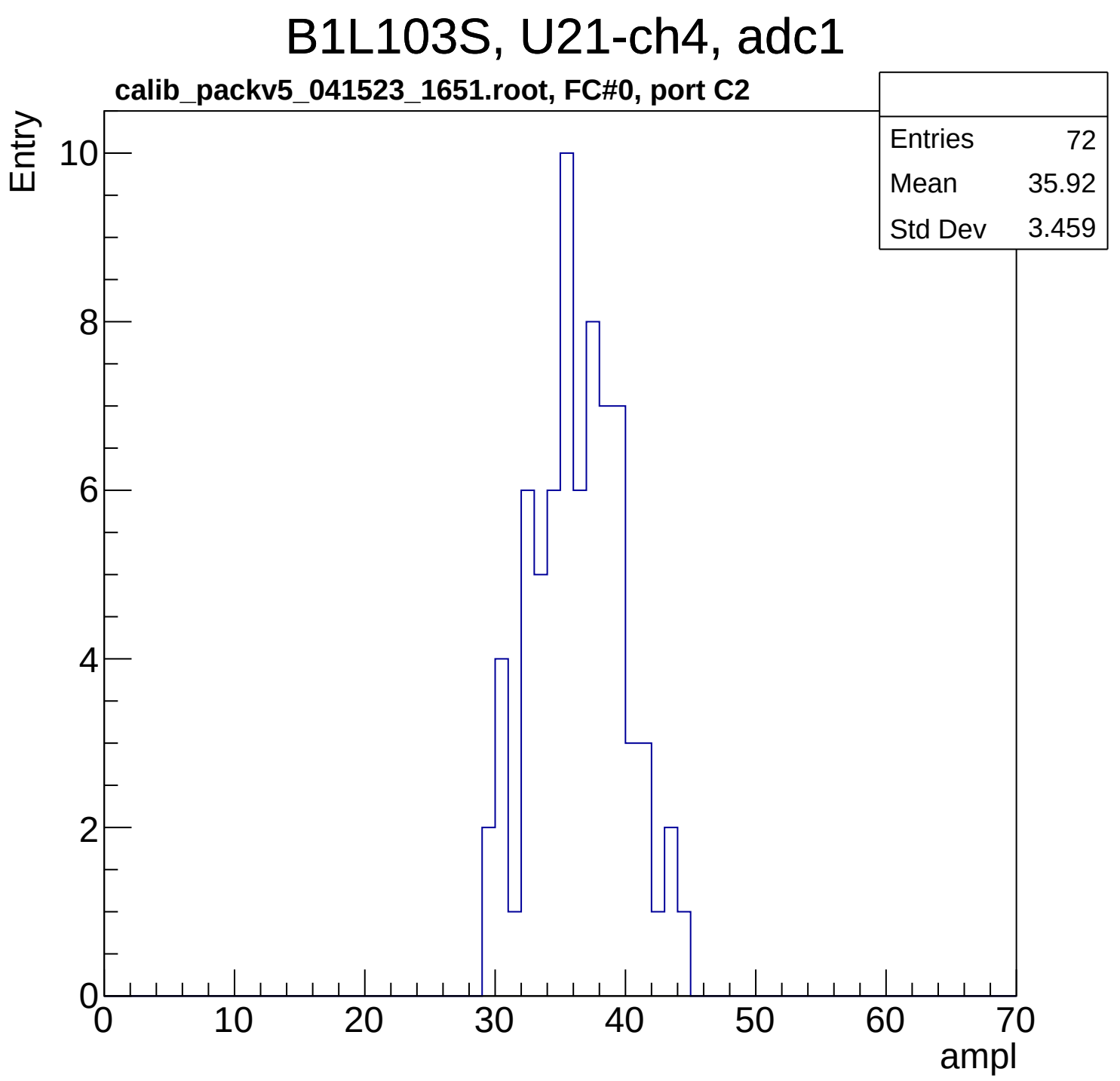
40
50
60
70
ampl


B1L103S, U21-ch4, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 35.92
Std Dev 3.459
Entry
ampl
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2
4
6
8
10
0
10
20
30
40
50
60
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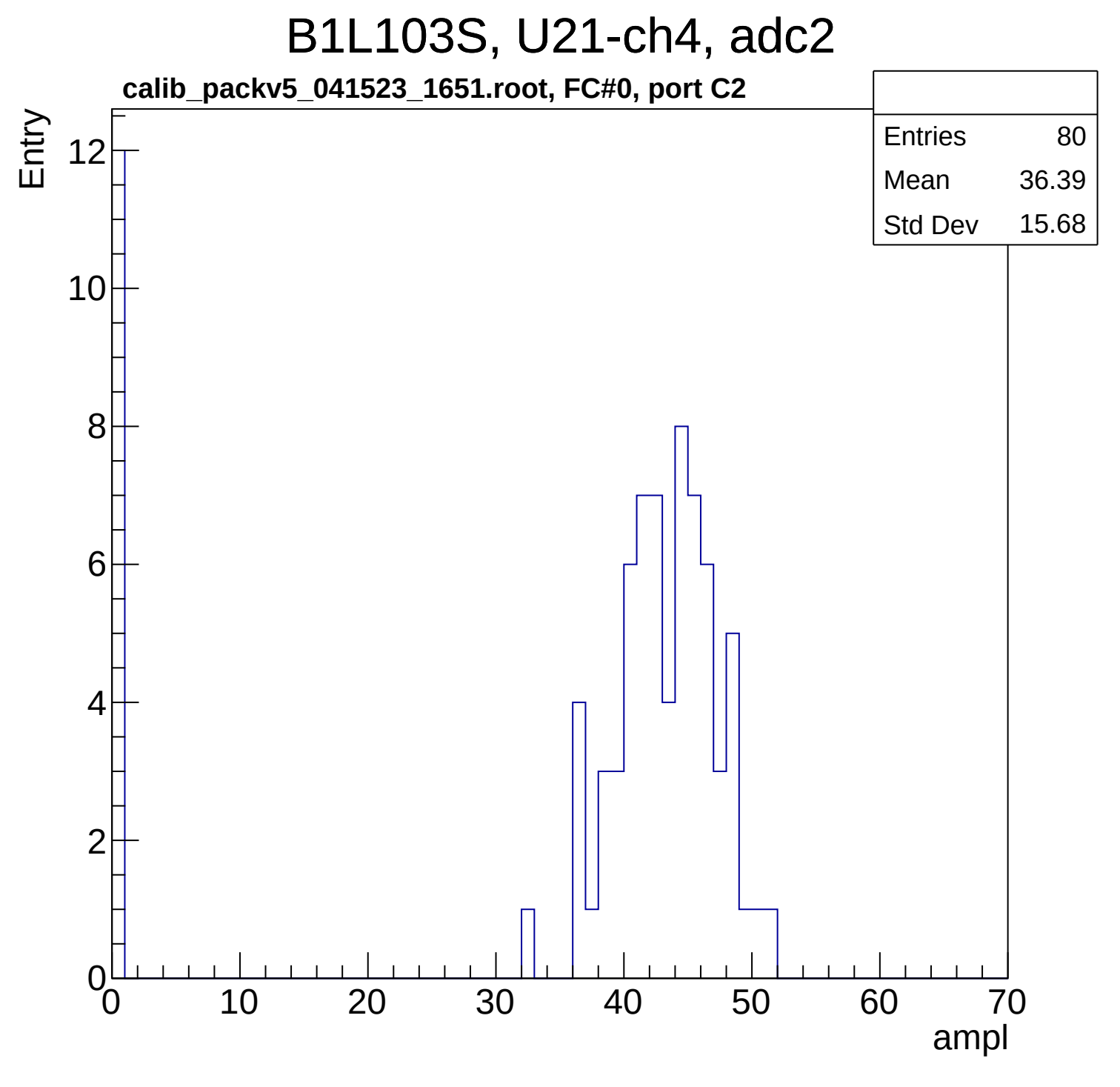
B1L103S, U21-ch4, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 36.39
Std Dev 15.68
Entry
0
2
4
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8
10
12
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10
20
30
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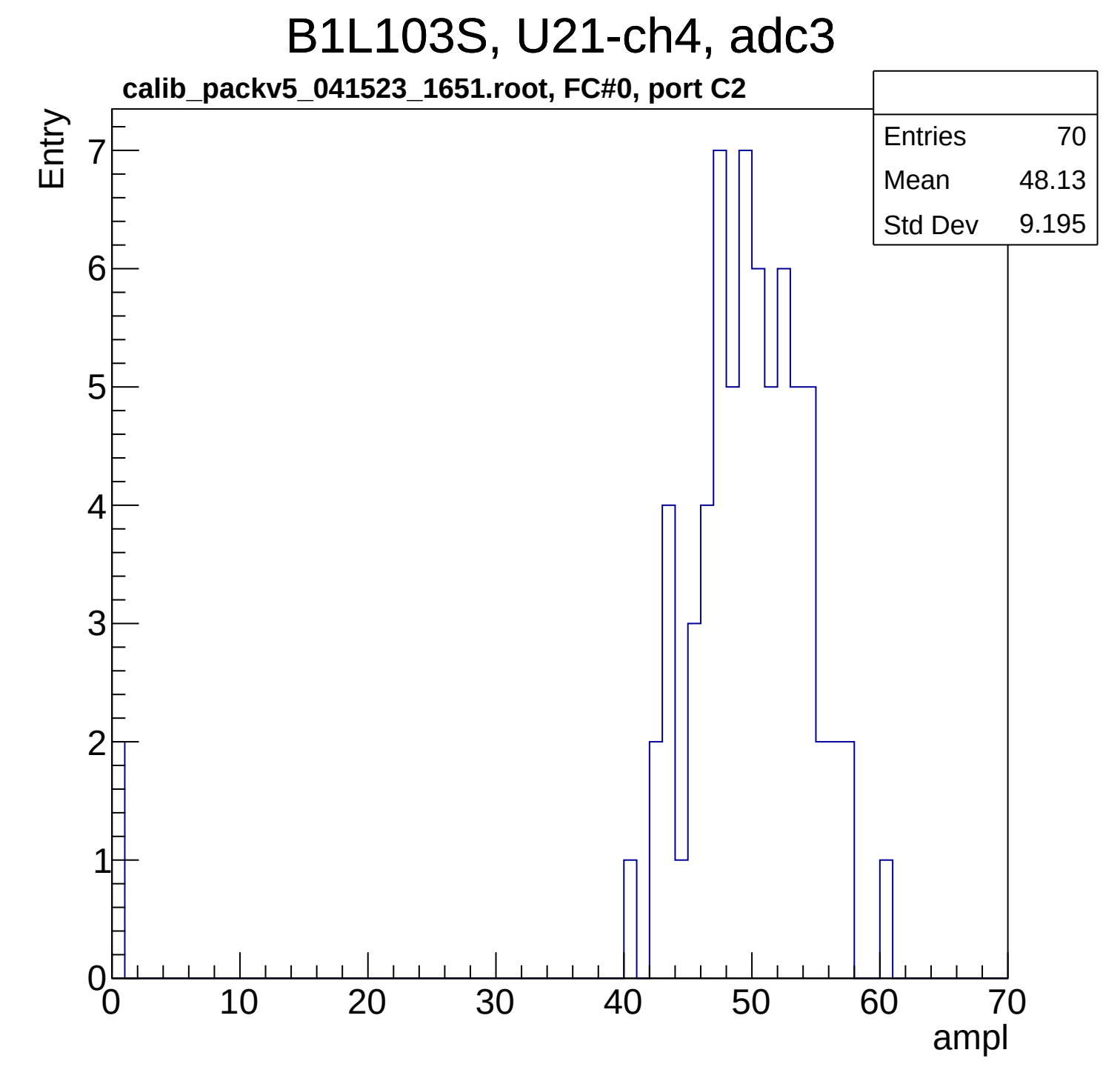
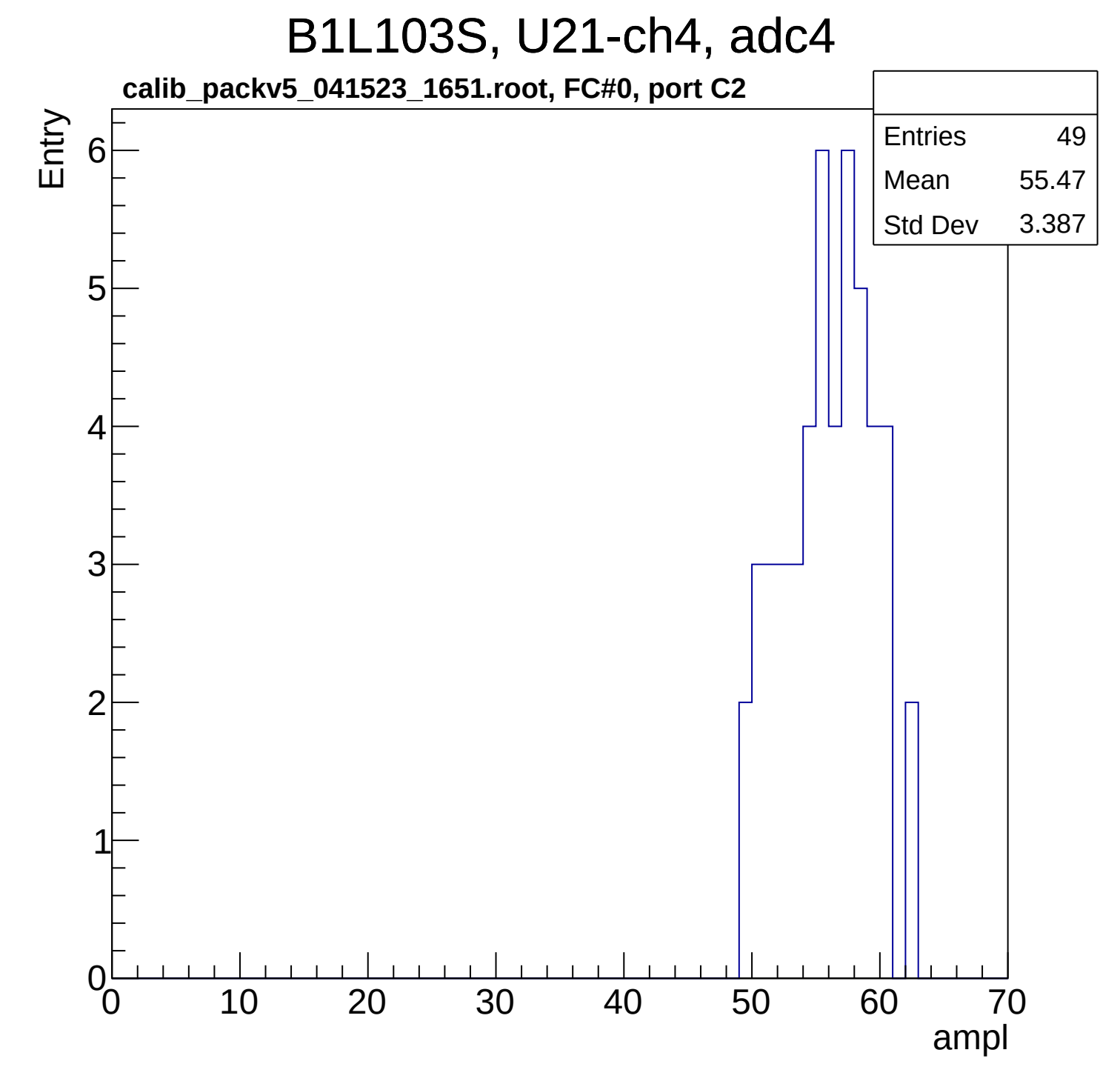
50
60
70
ampl


B1L103S, U21-ch4, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 48.13
Std Dev 9.195
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U21-ch4, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 55.47
Std Dev 3.387
Entry
ampl
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2
3
4
5
6
0
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30
40
50
60
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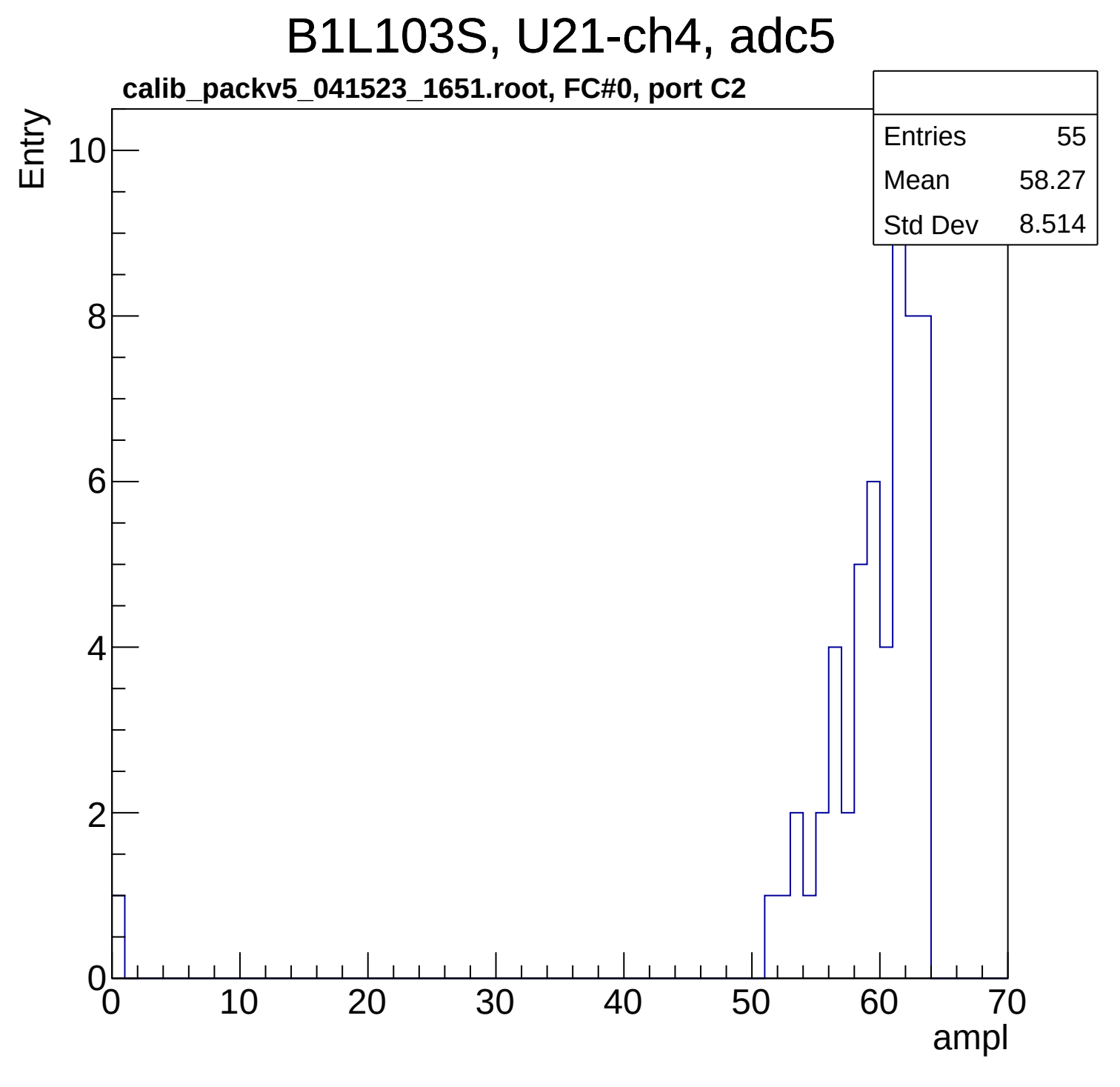
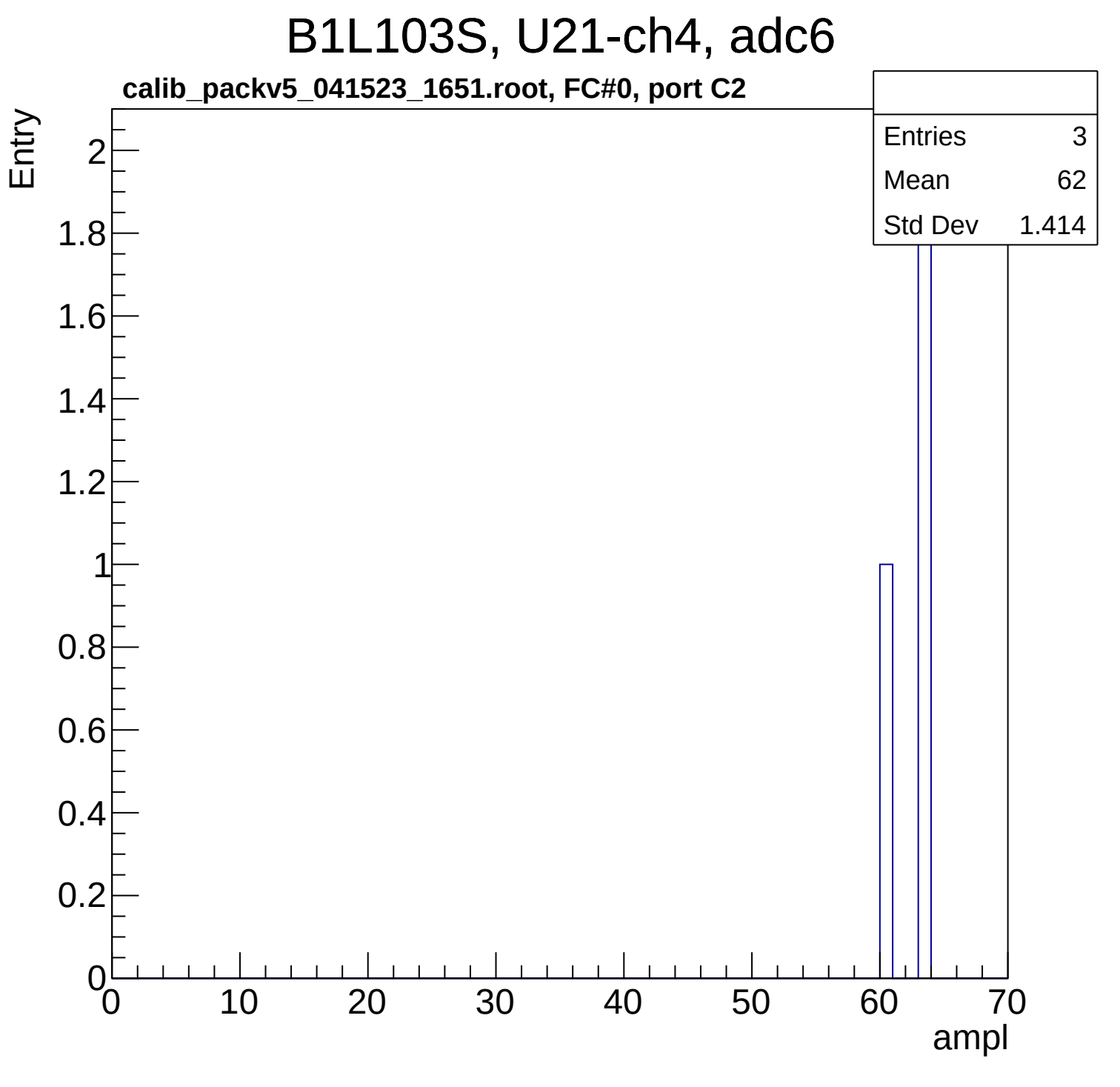
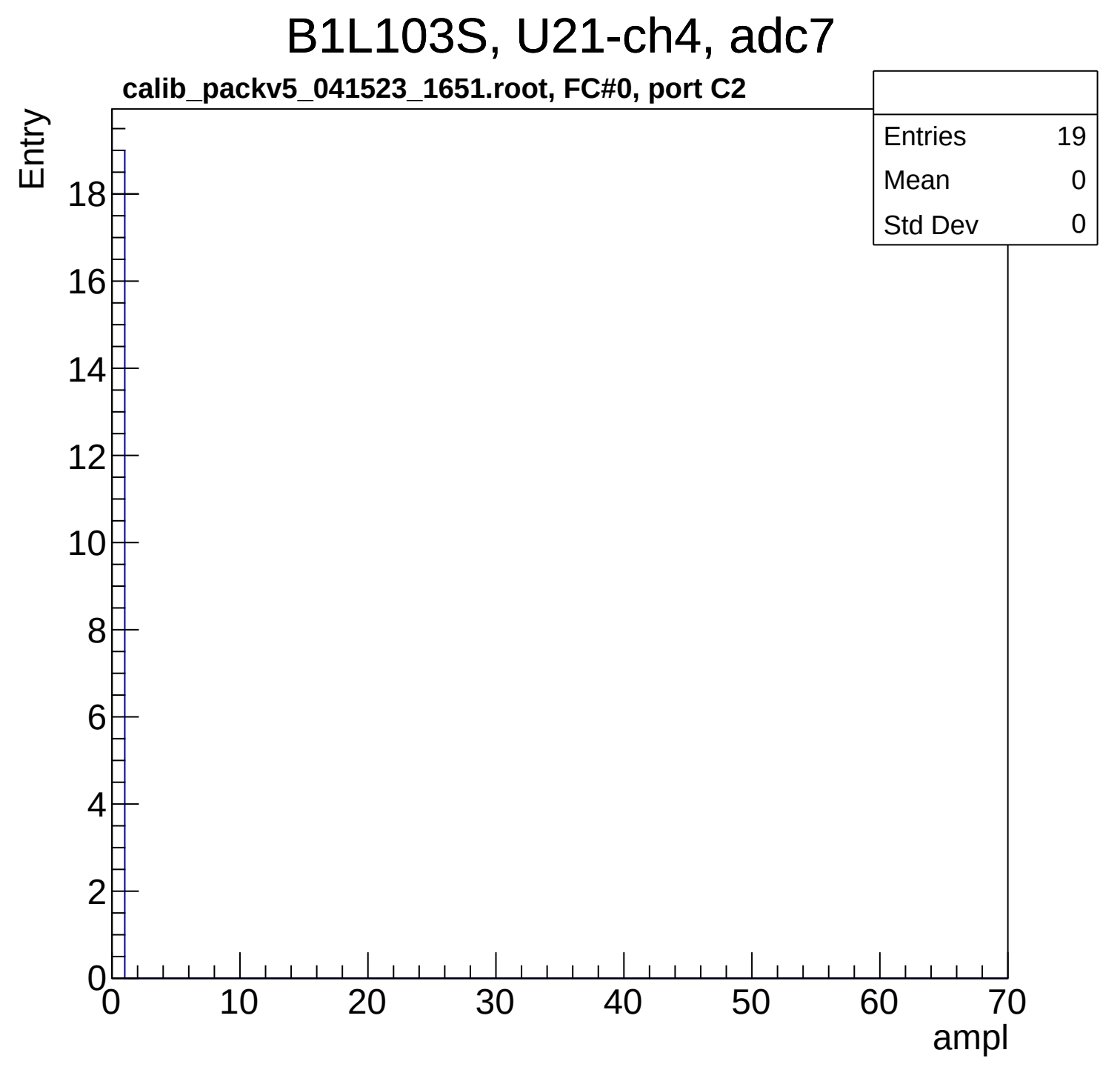
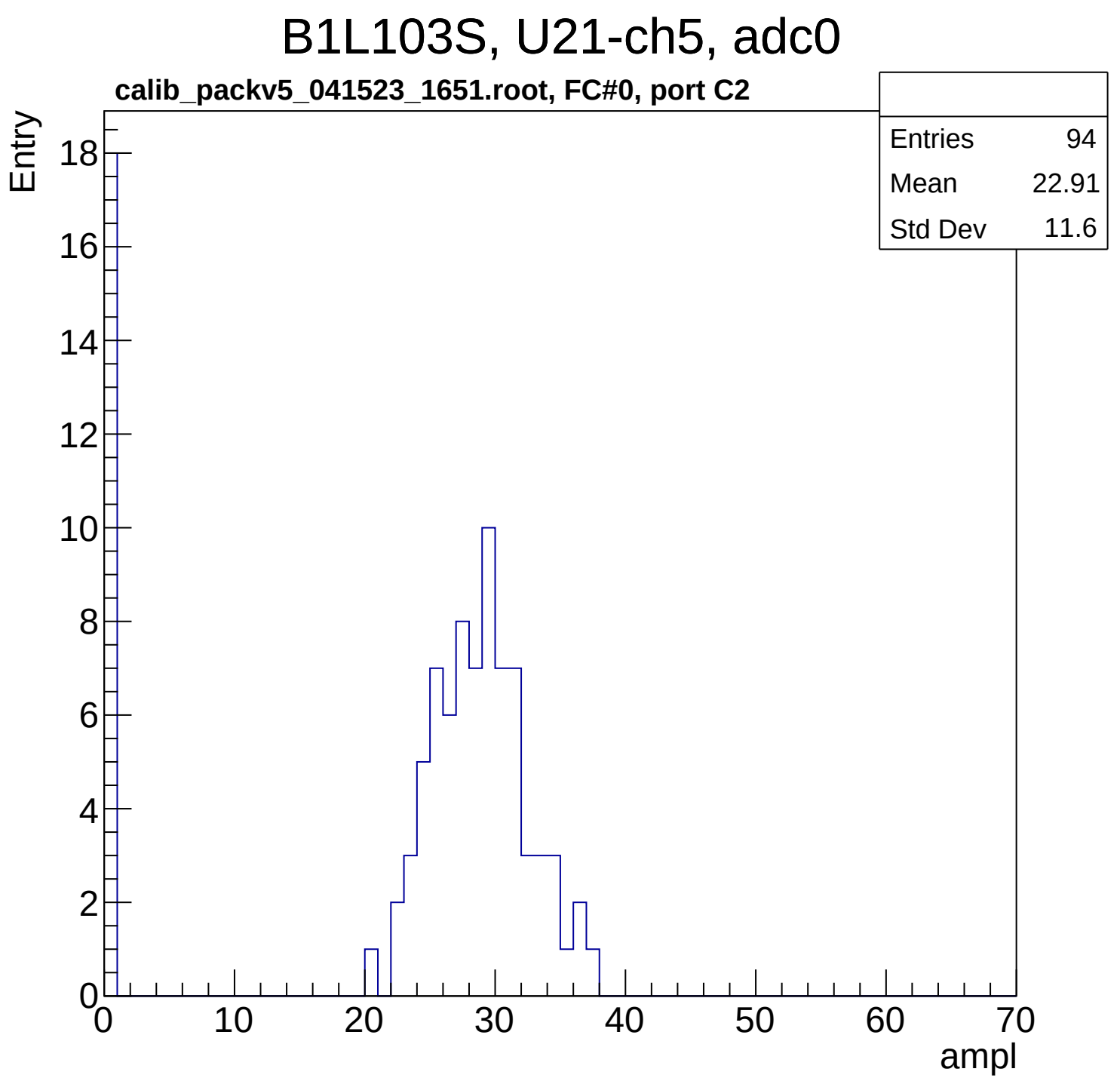
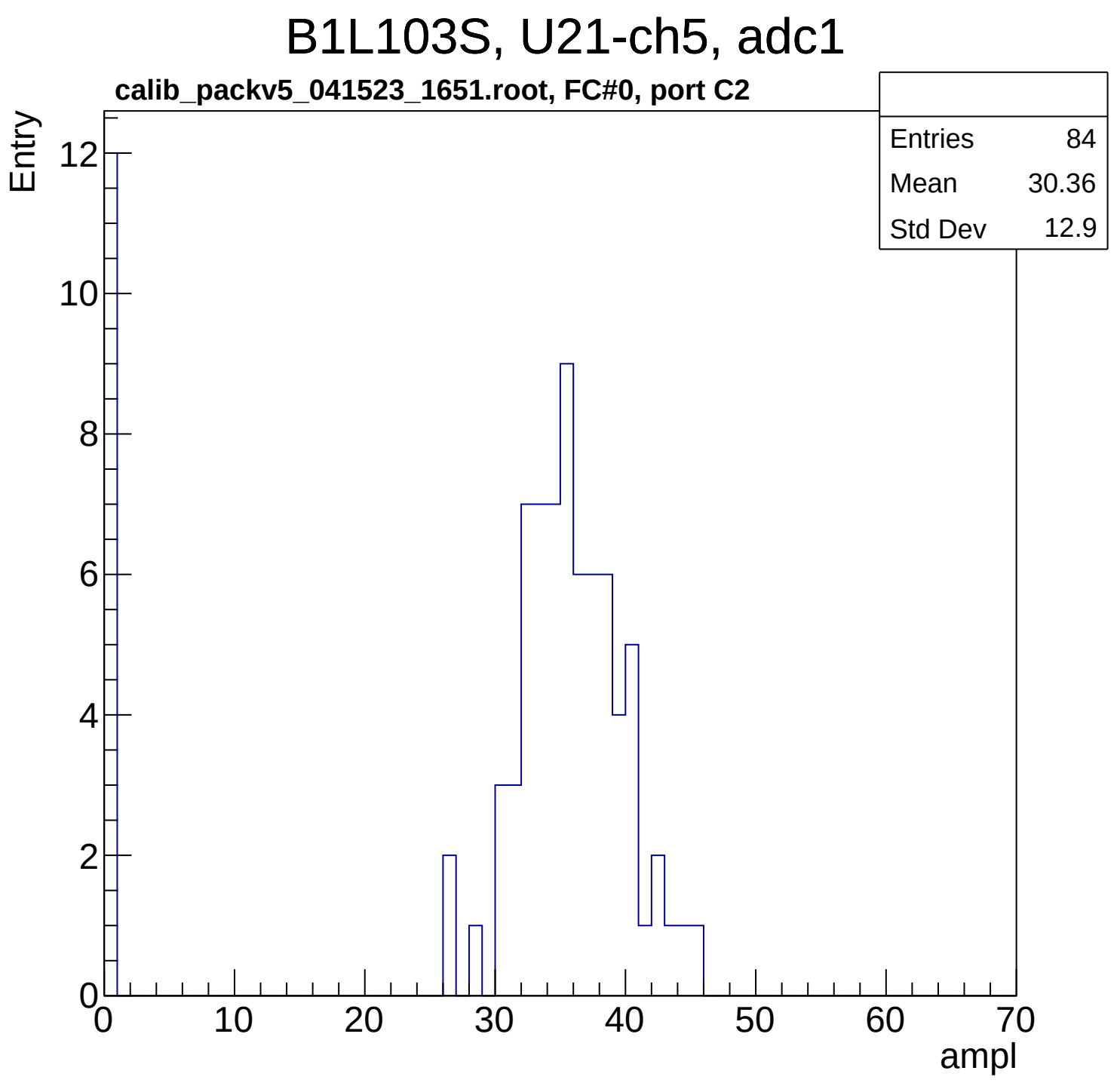
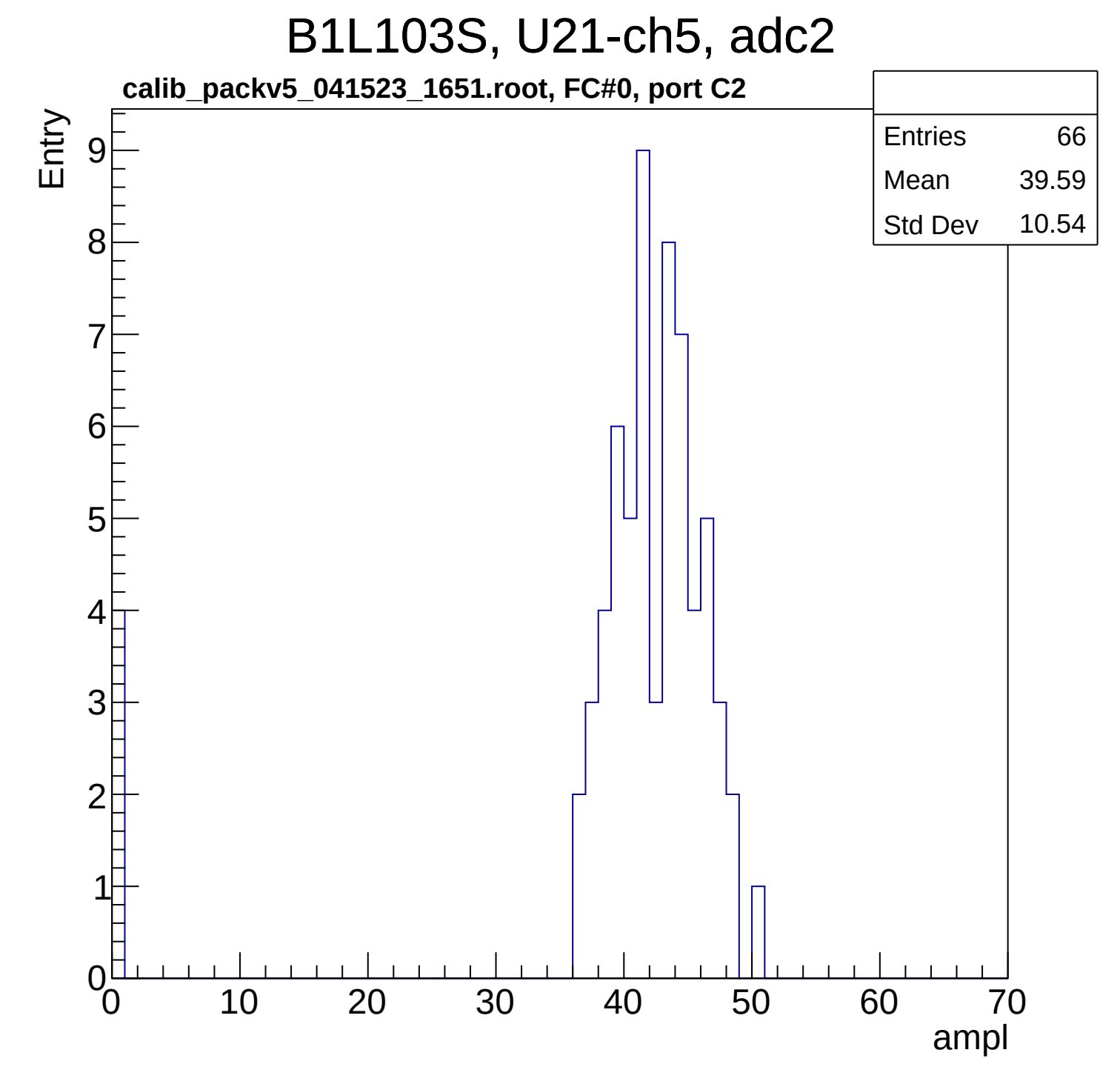

B1L103S, U21-ch4, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 58.27
Std Dev 8.514
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

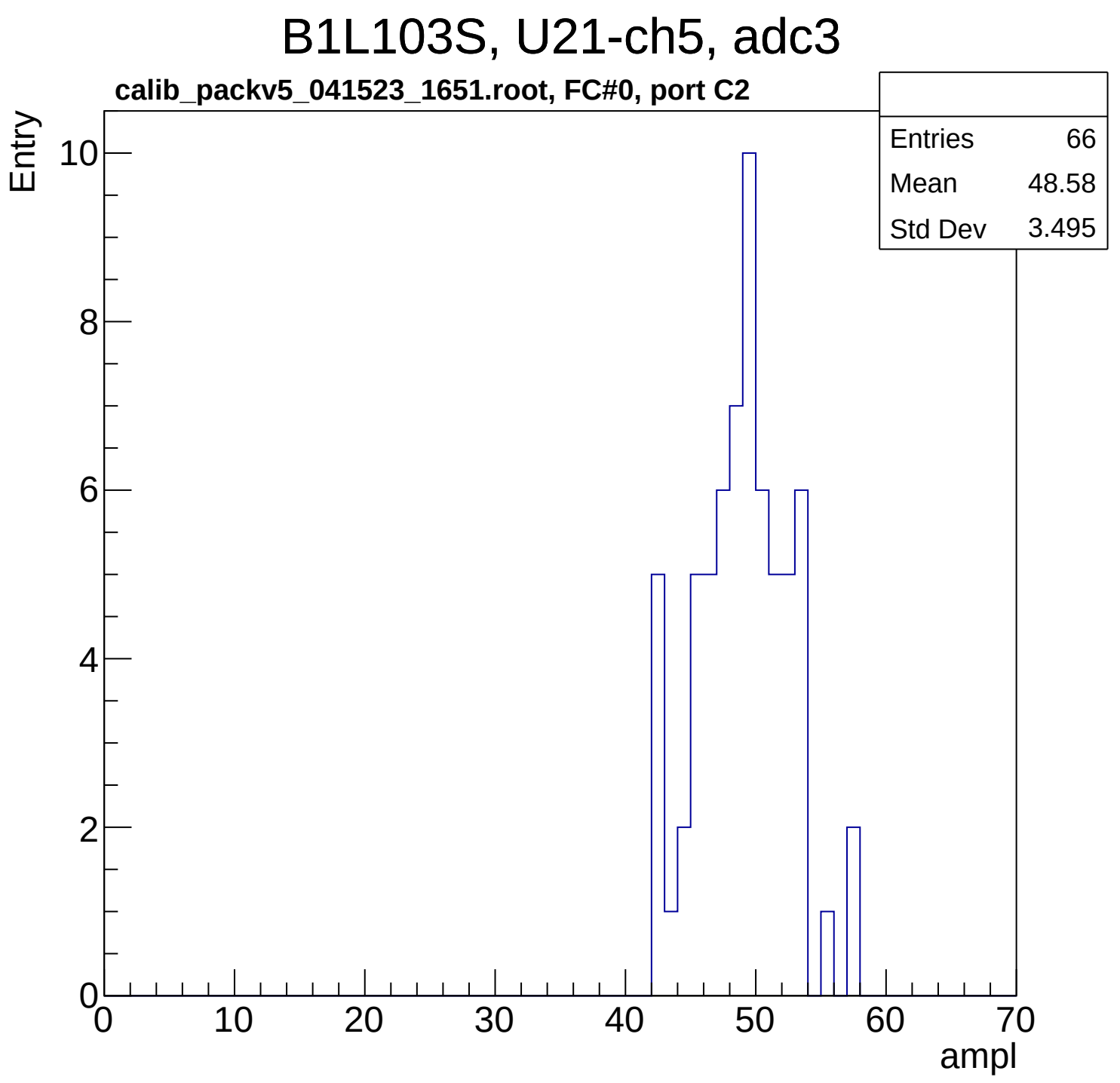

B1L103S, U21-ch4, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 62
Std Dev 1.414
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

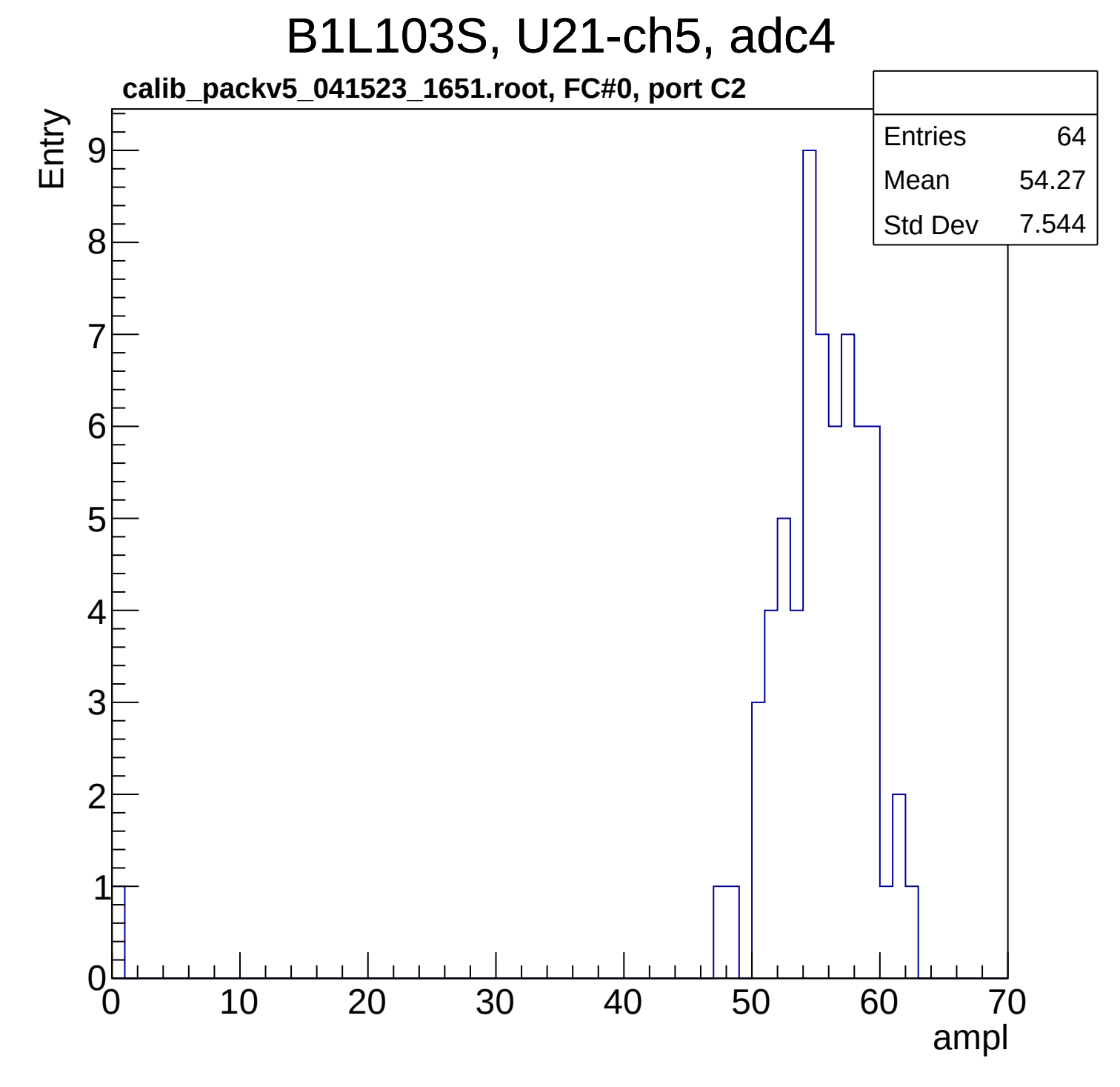

B1L103S, U21-ch4, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch5, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 22.91
Std Dev 11.6
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch5, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 30.36
Std Dev 12.9
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch5, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 39.59
Std Dev 10.54
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch5, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 48.58
Std Dev 3.495
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U21-ch5, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 54.27
Std Dev 7.544
Entry
ampl
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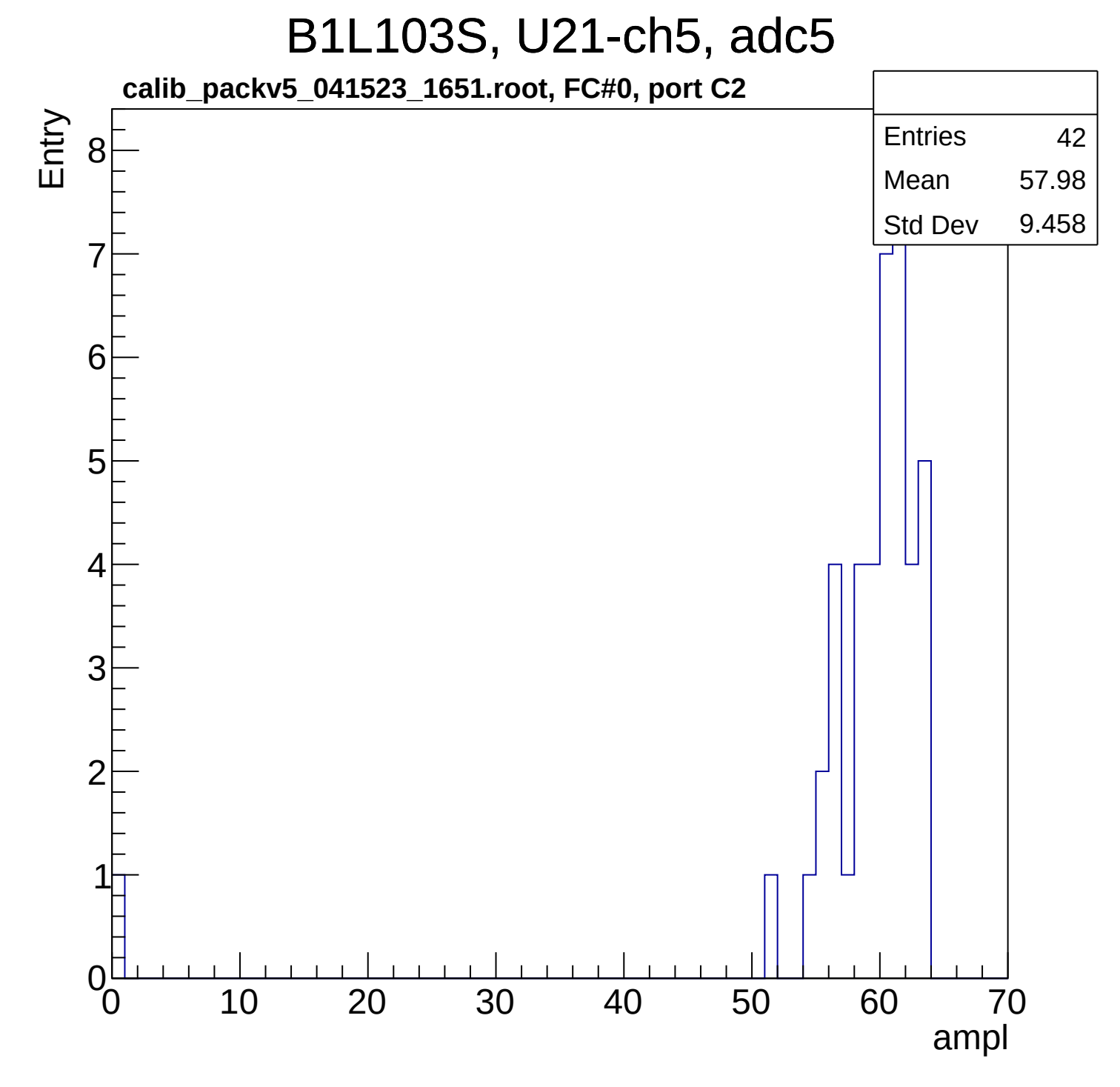
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch5, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 57.98
Std Dev 9.458
Entry
ampl
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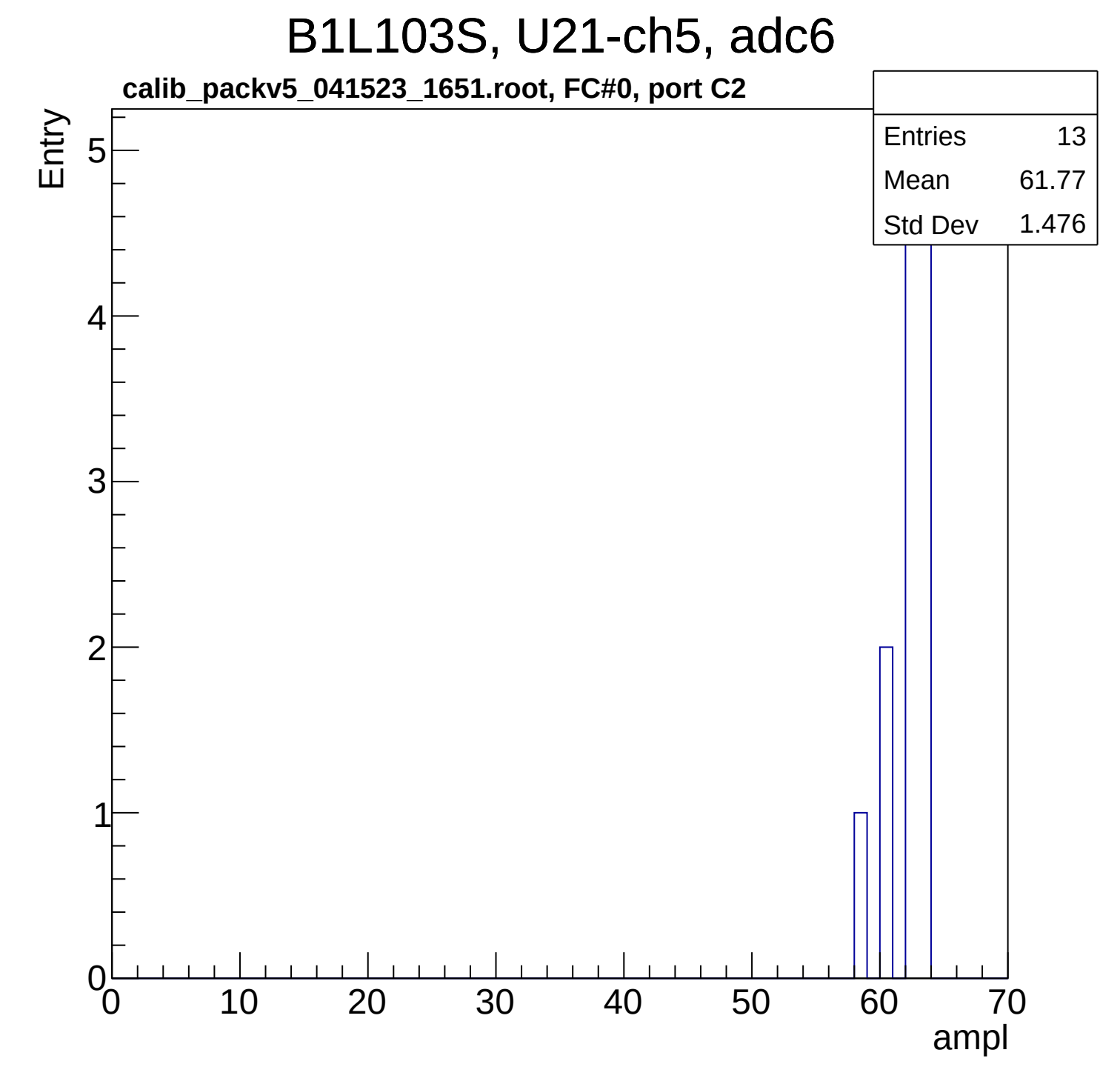
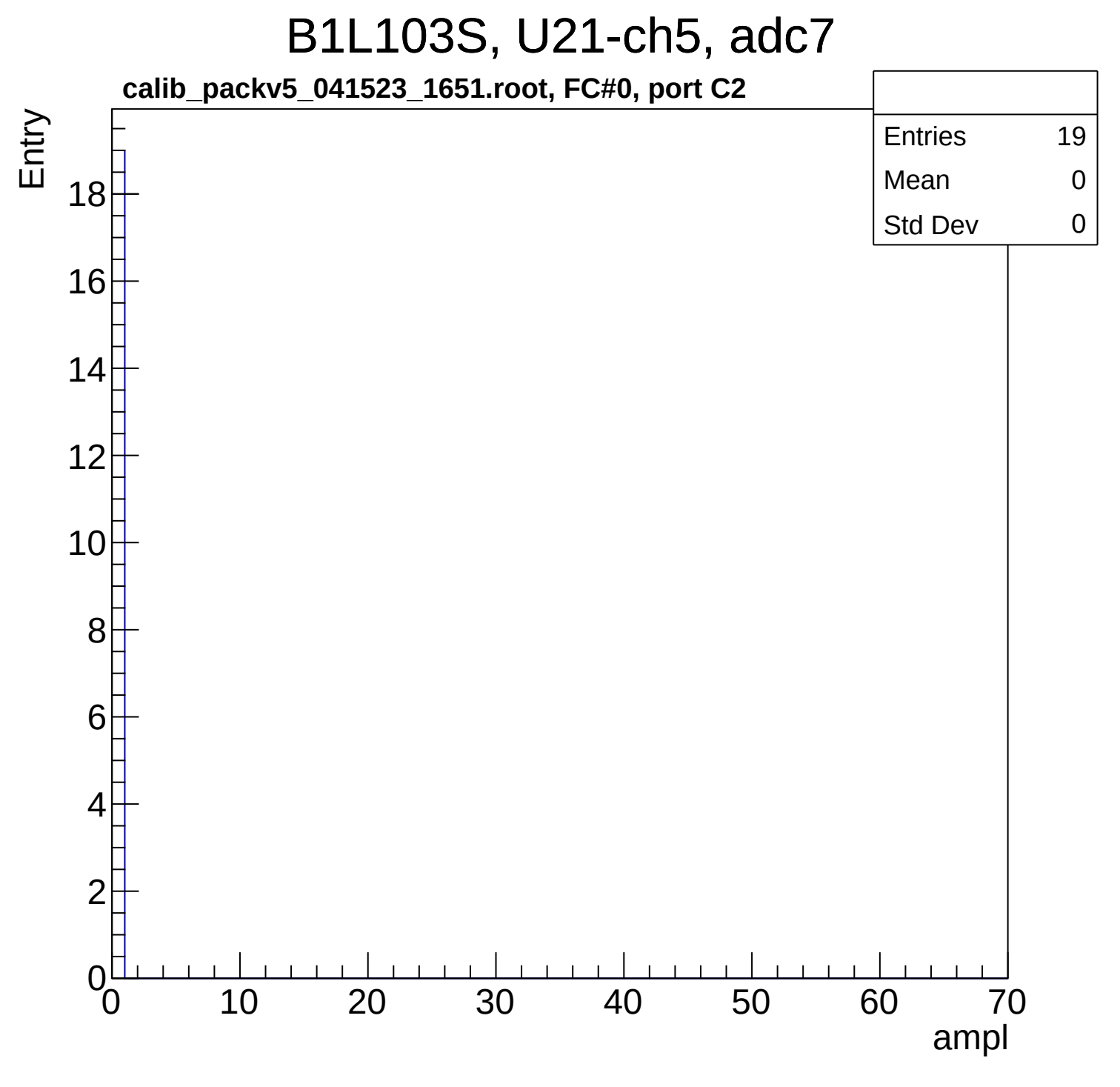
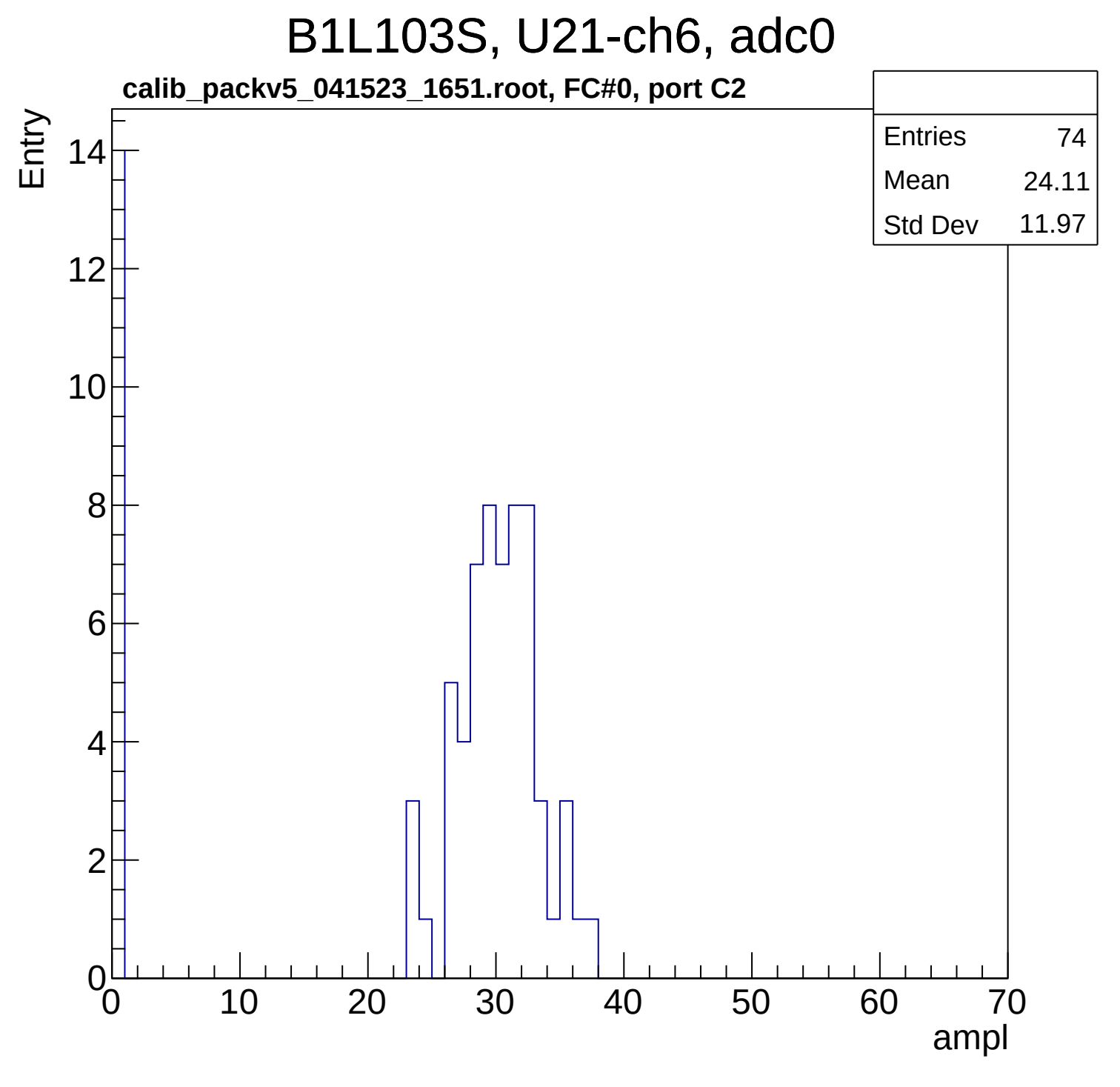
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch5, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 61.77
Std Dev 1.476
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U21-ch5, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch6, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 24.11
Std Dev 11.97
Entry
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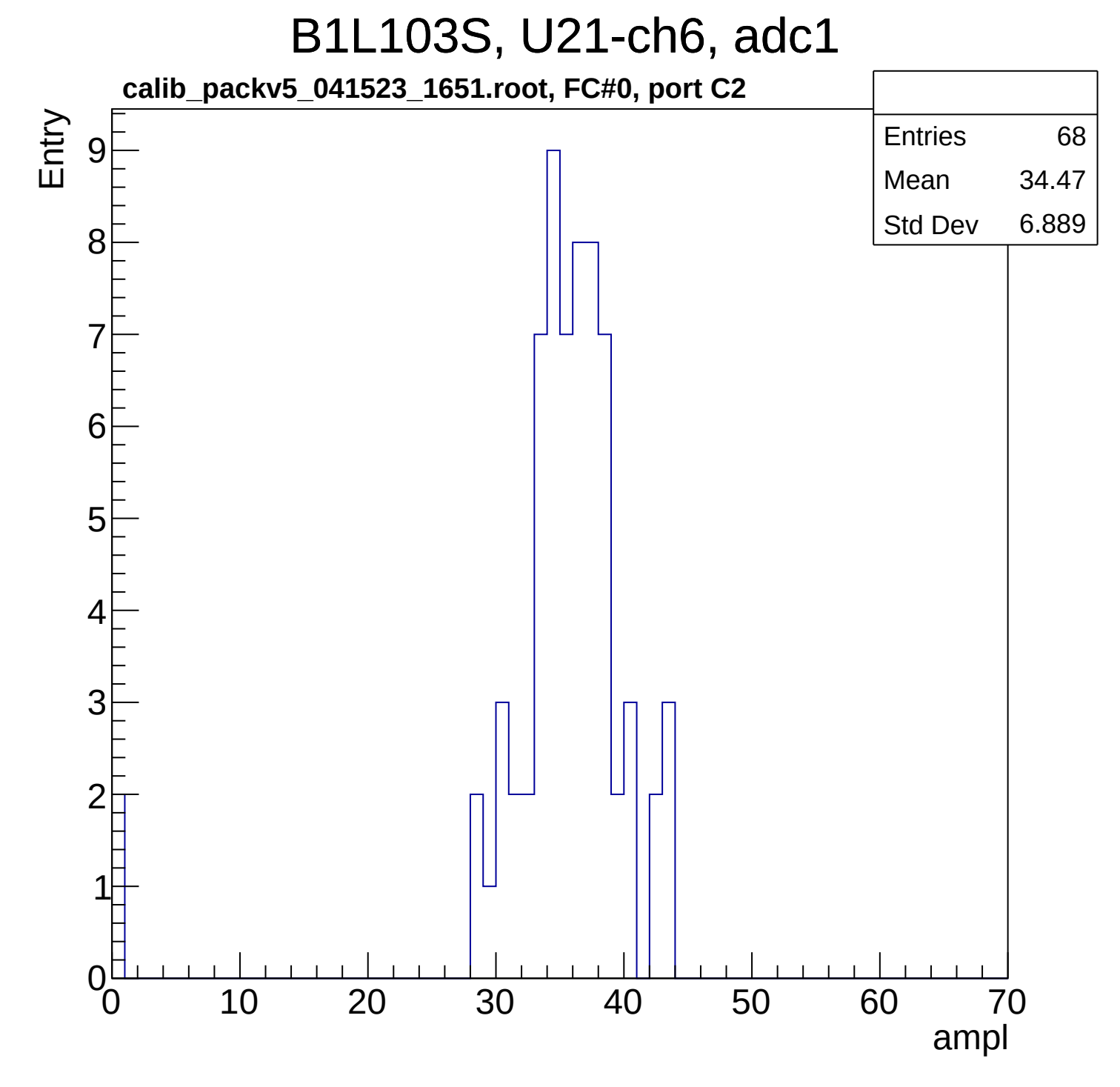
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch6, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 34.47
Std Dev 6.889
Entry
ampl
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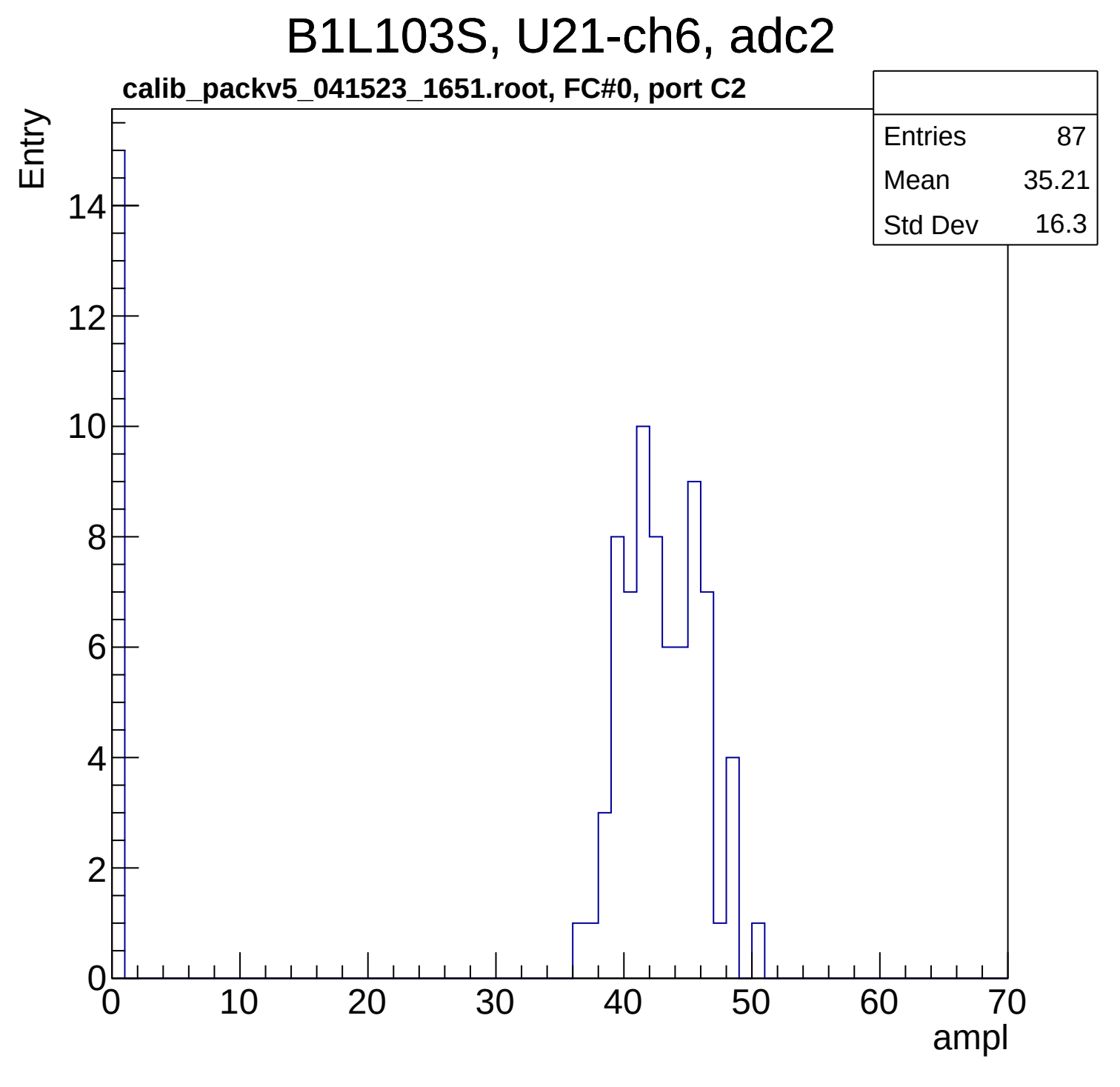
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch6, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 35.21
Std Dev 16.3
Entry
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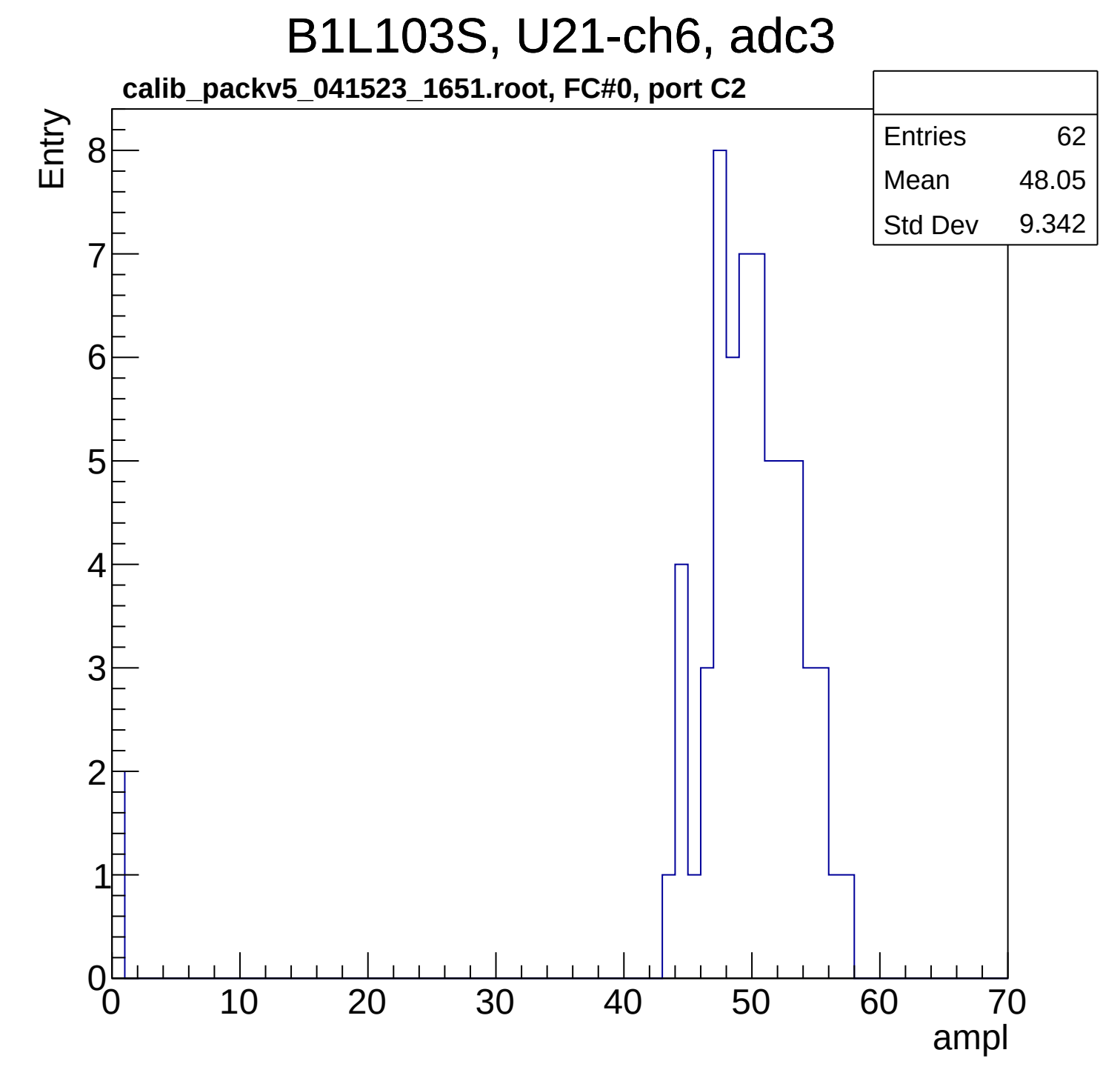
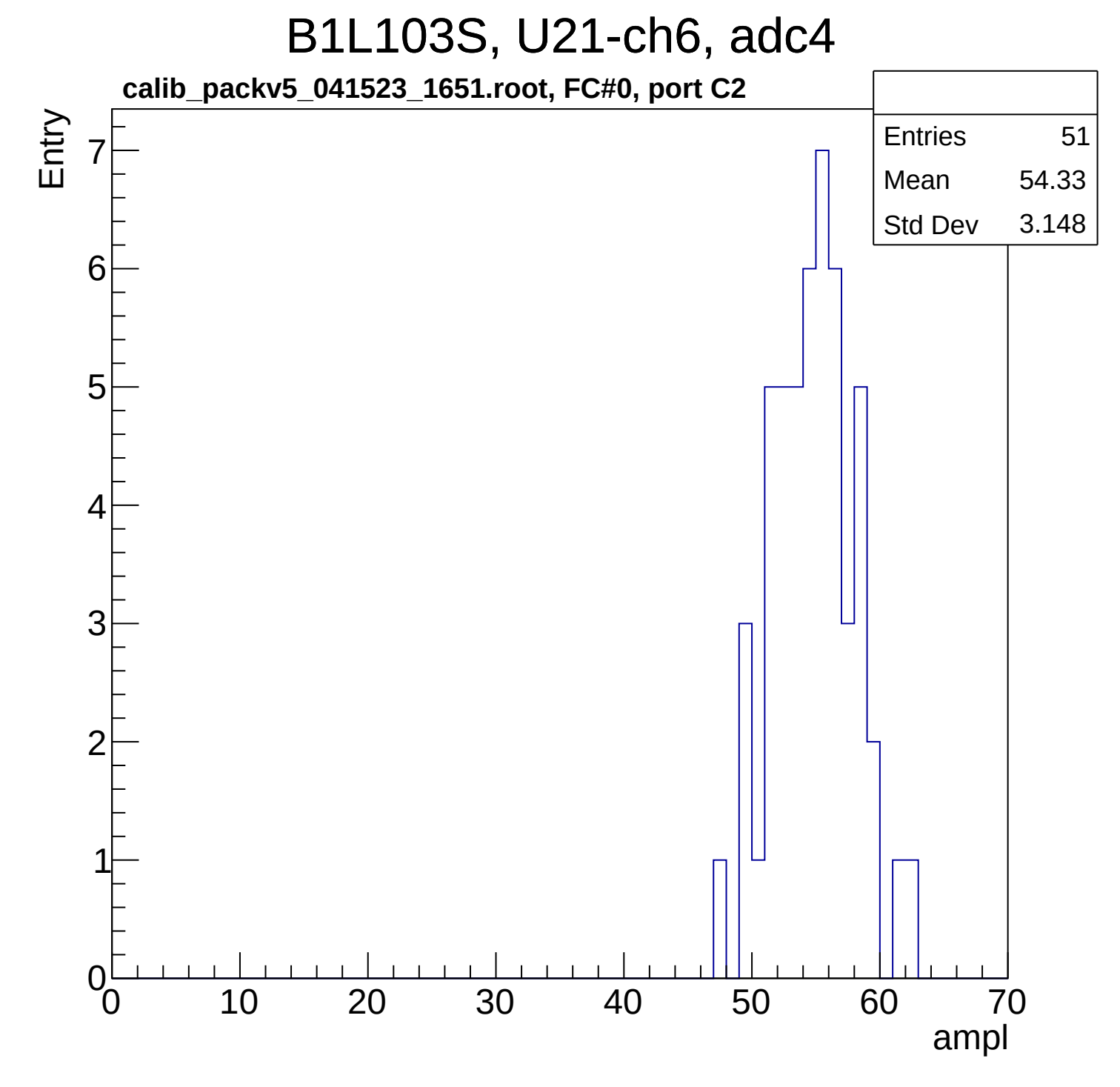
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch6, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 48.05
Std Dev 9.342
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch6, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 54.33
Std Dev 3.148
Entry
ampl
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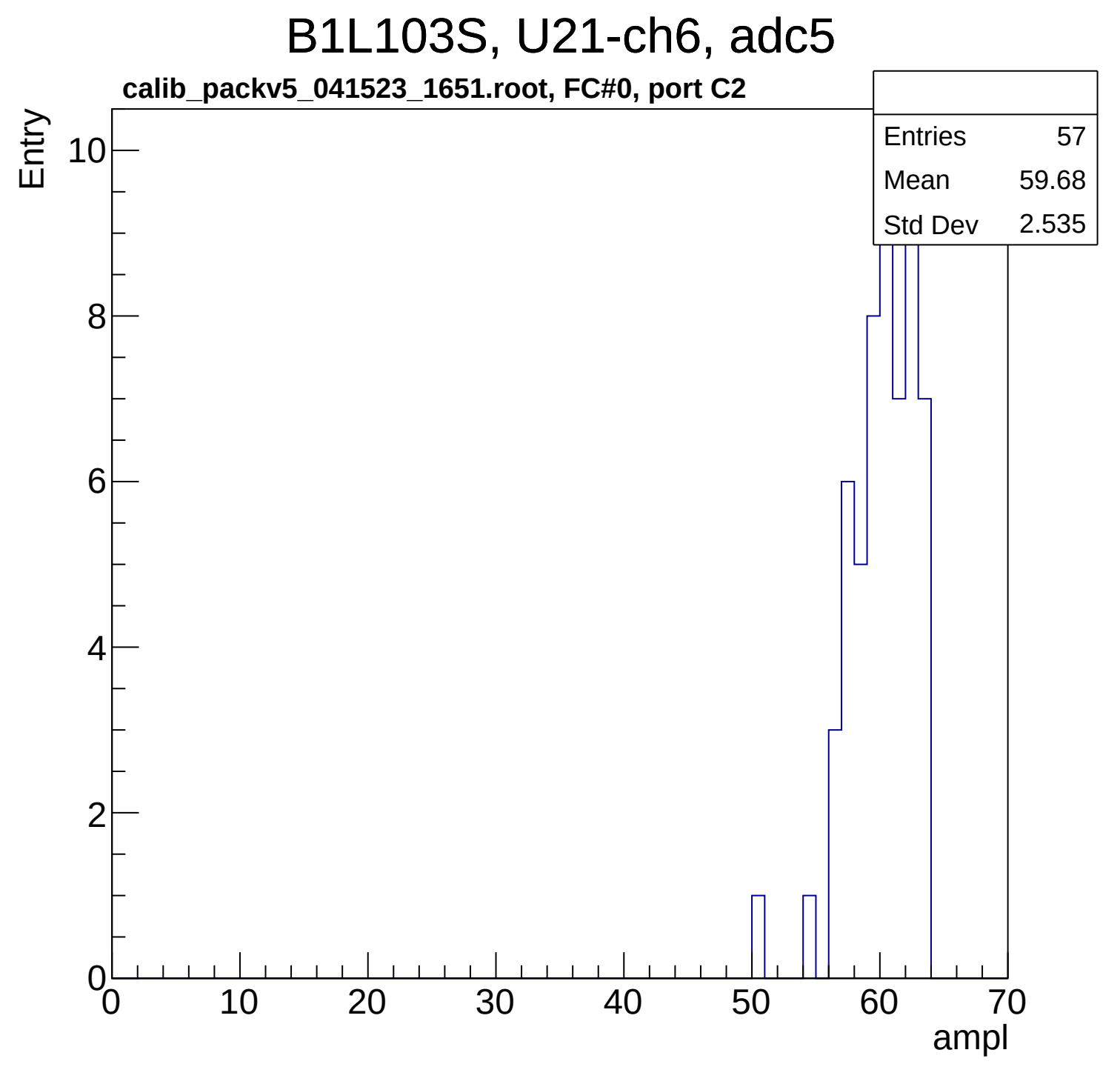
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U21-ch6, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 59.68
Std Dev 2.535
Entry
ampl
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2
4
6
8
10
0
10
20
30
40
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60
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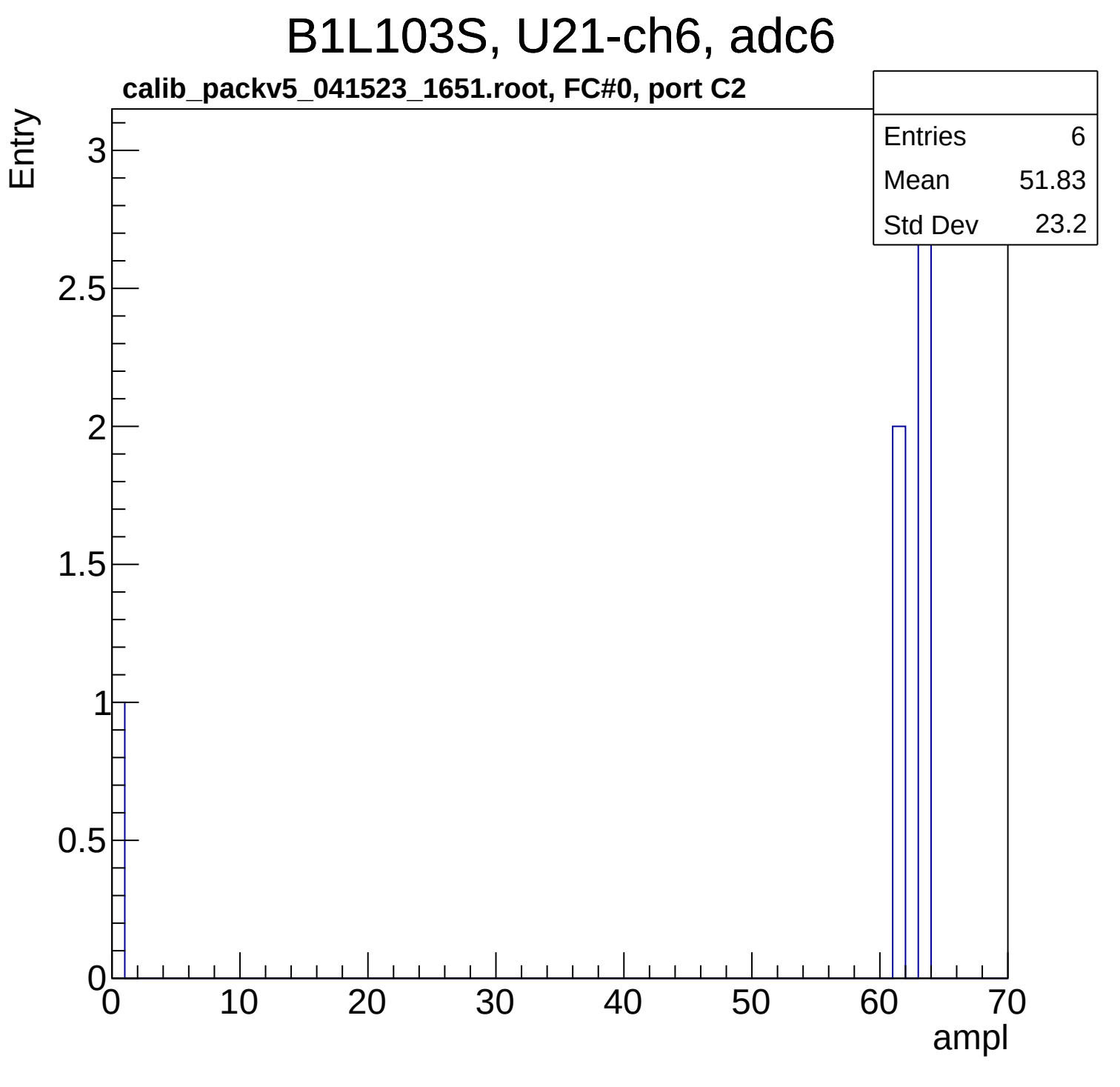
B1L103S, U21-ch6, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 51.83
Std Dev 23.2
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
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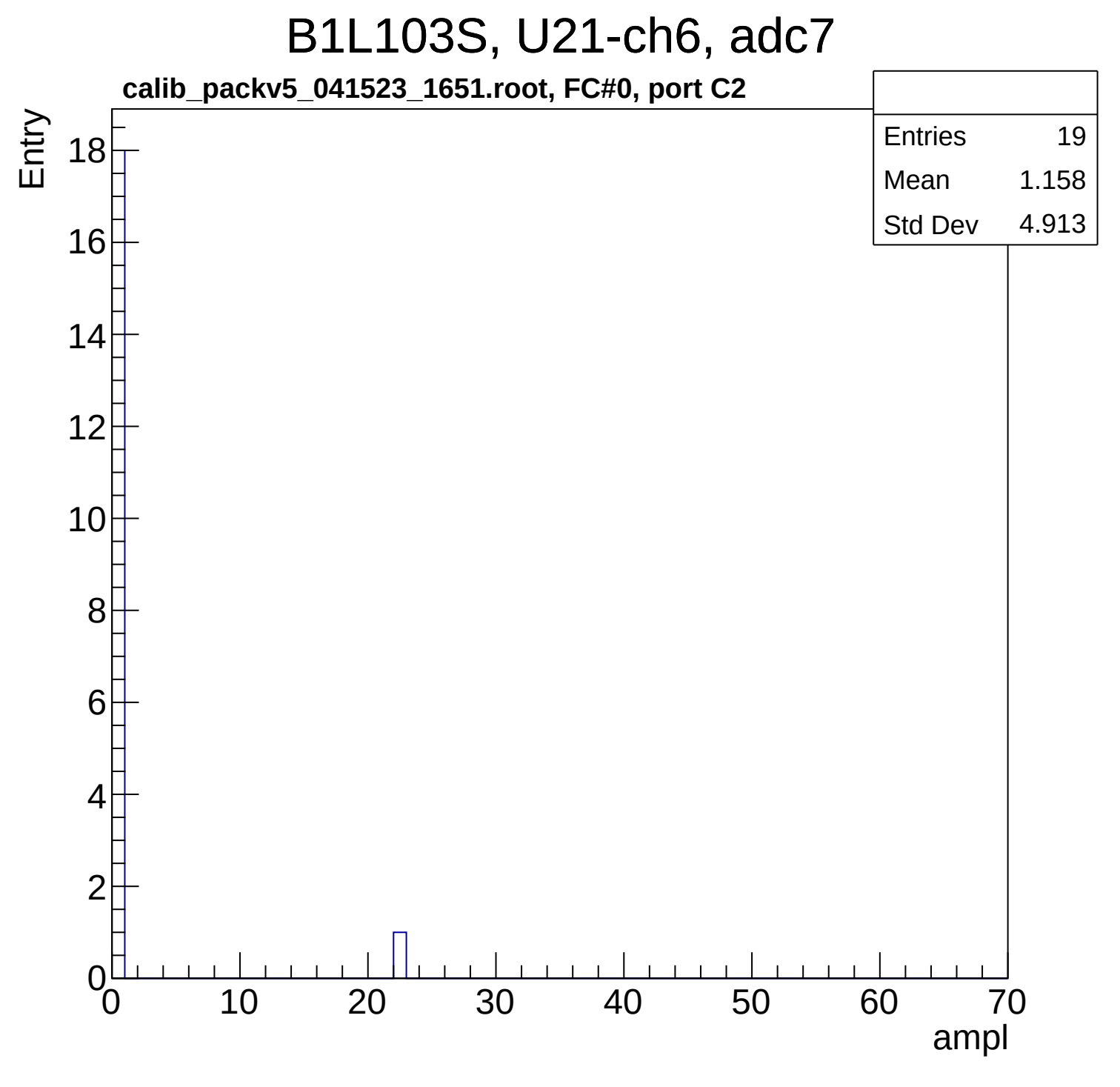
40
50
60
70


B1L103S, U21-ch6, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.158
Std Dev 4.913
Entry
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6
8
10
12
14
16
18
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10
20
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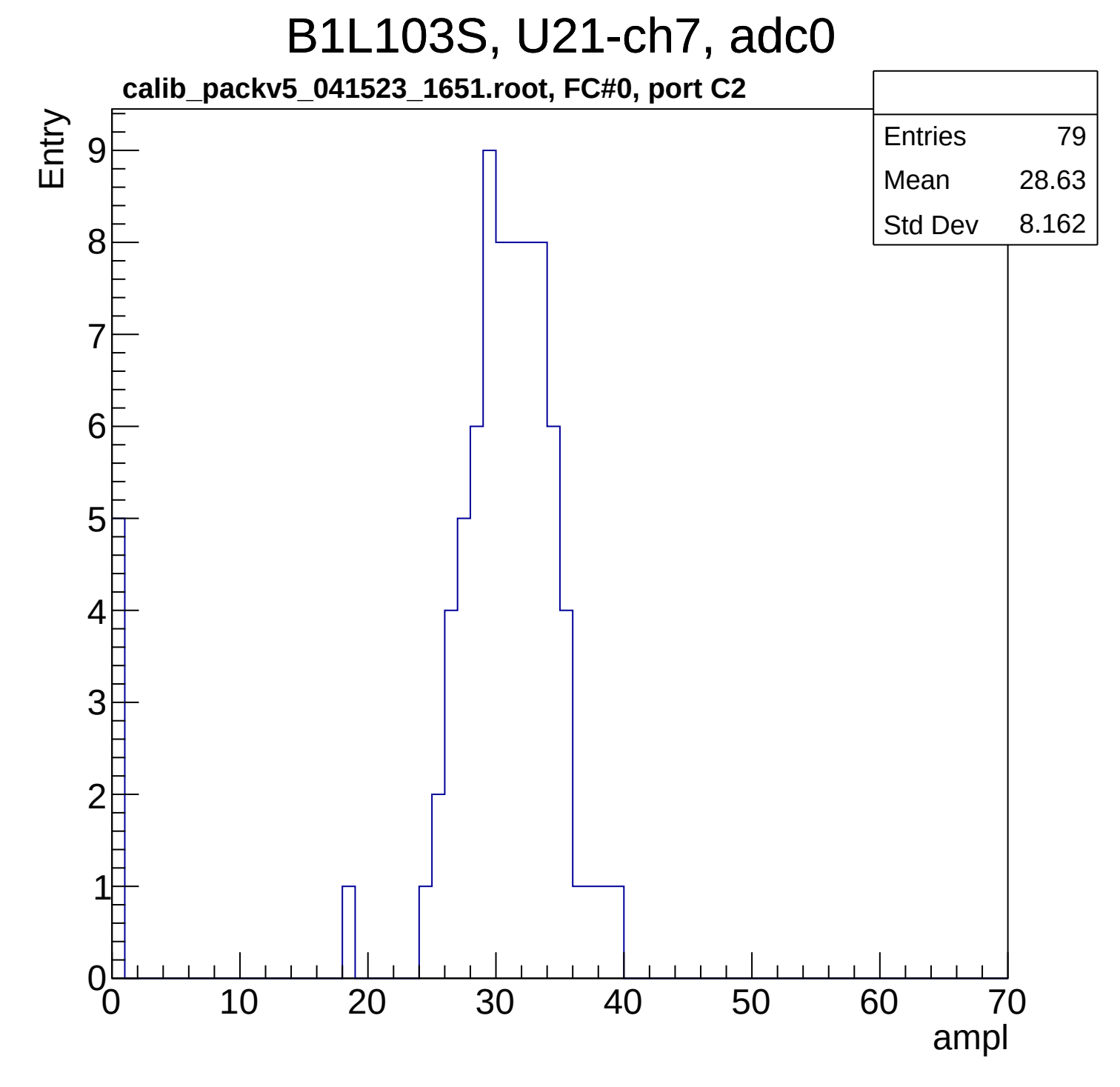
50
60
70
ampl


B1L103S, U21-ch7, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 28.63
Std Dev 8.162
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
50
60
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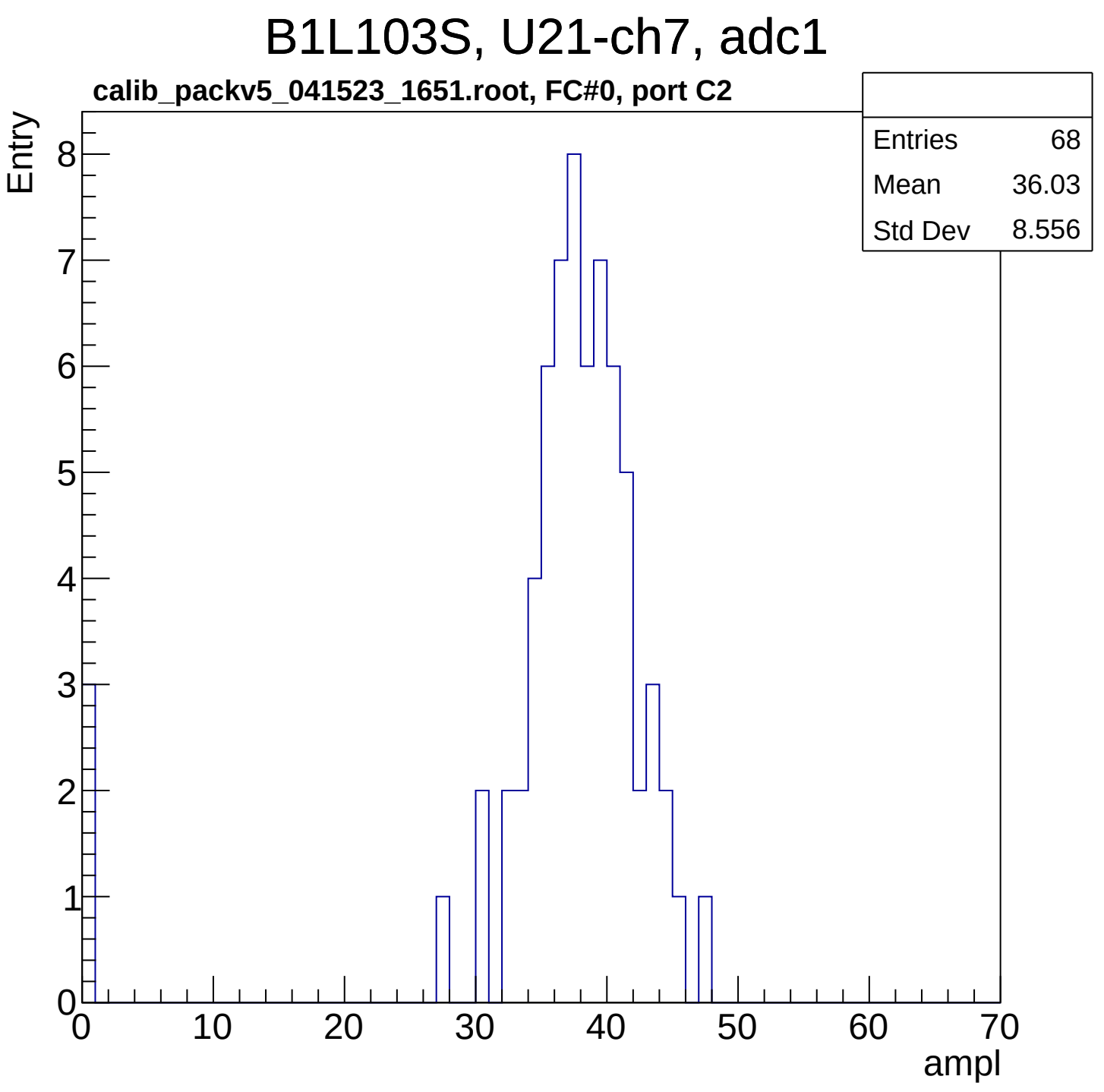
B1L103S, U21-ch7, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 36.03
Std Dev 8.556
Entry
ampl
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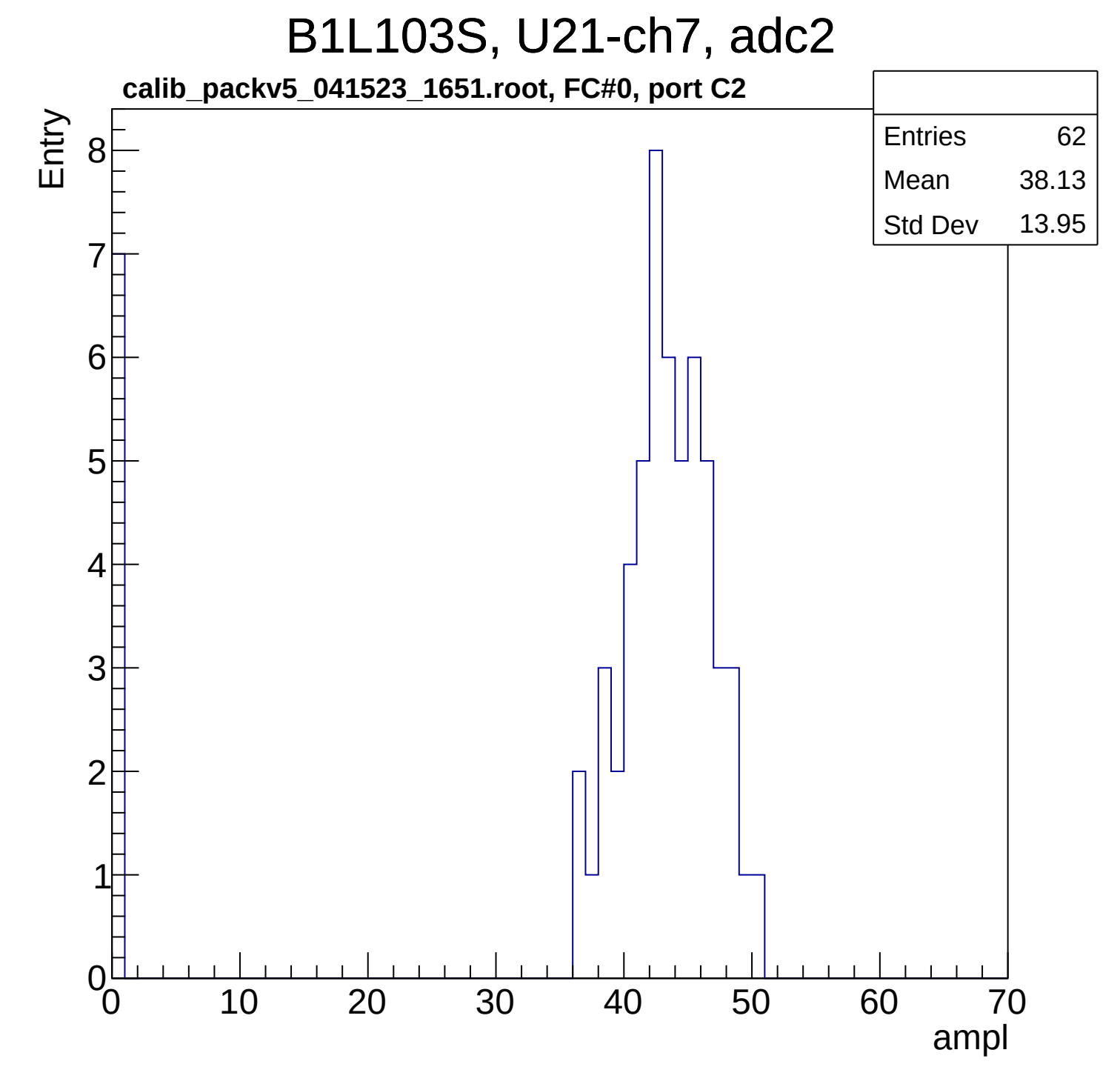
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch7, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 38.13
Std Dev 13.95
Entry
ampl
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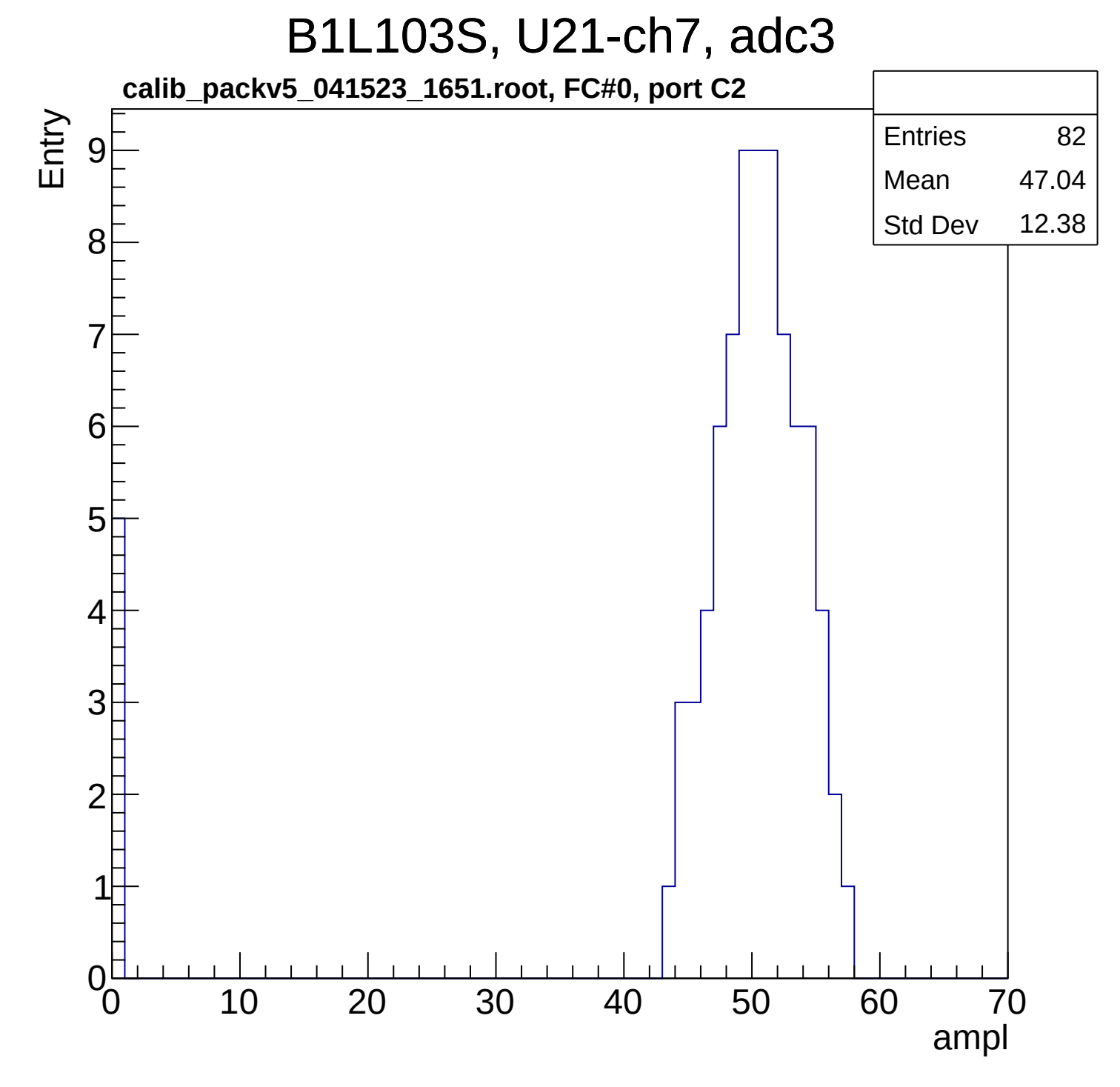
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch7, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 47.04
Std Dev 12.38
Entry
ampl
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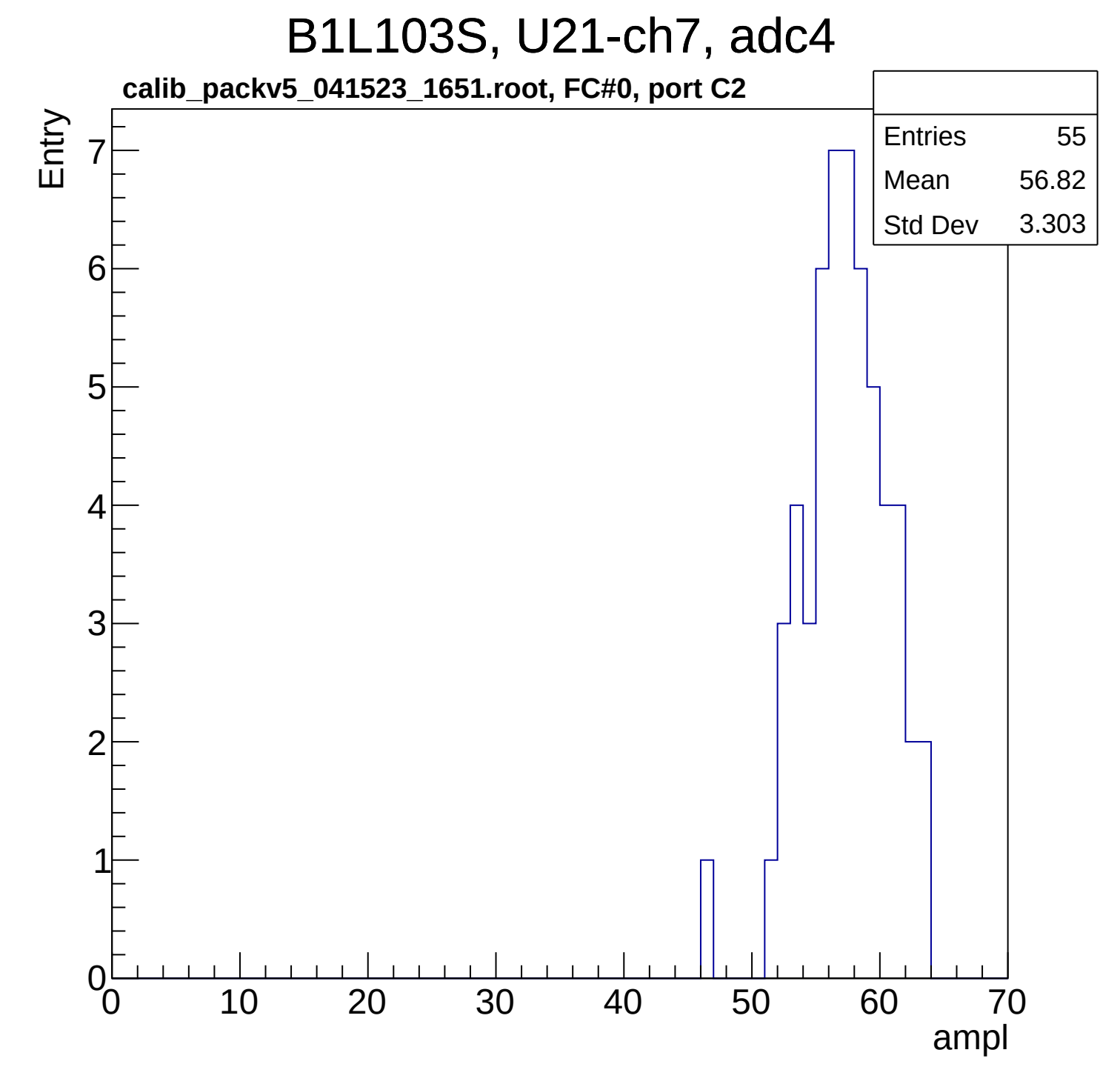
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch7, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 56.82
Std Dev 3.303
Entry
ampl
0
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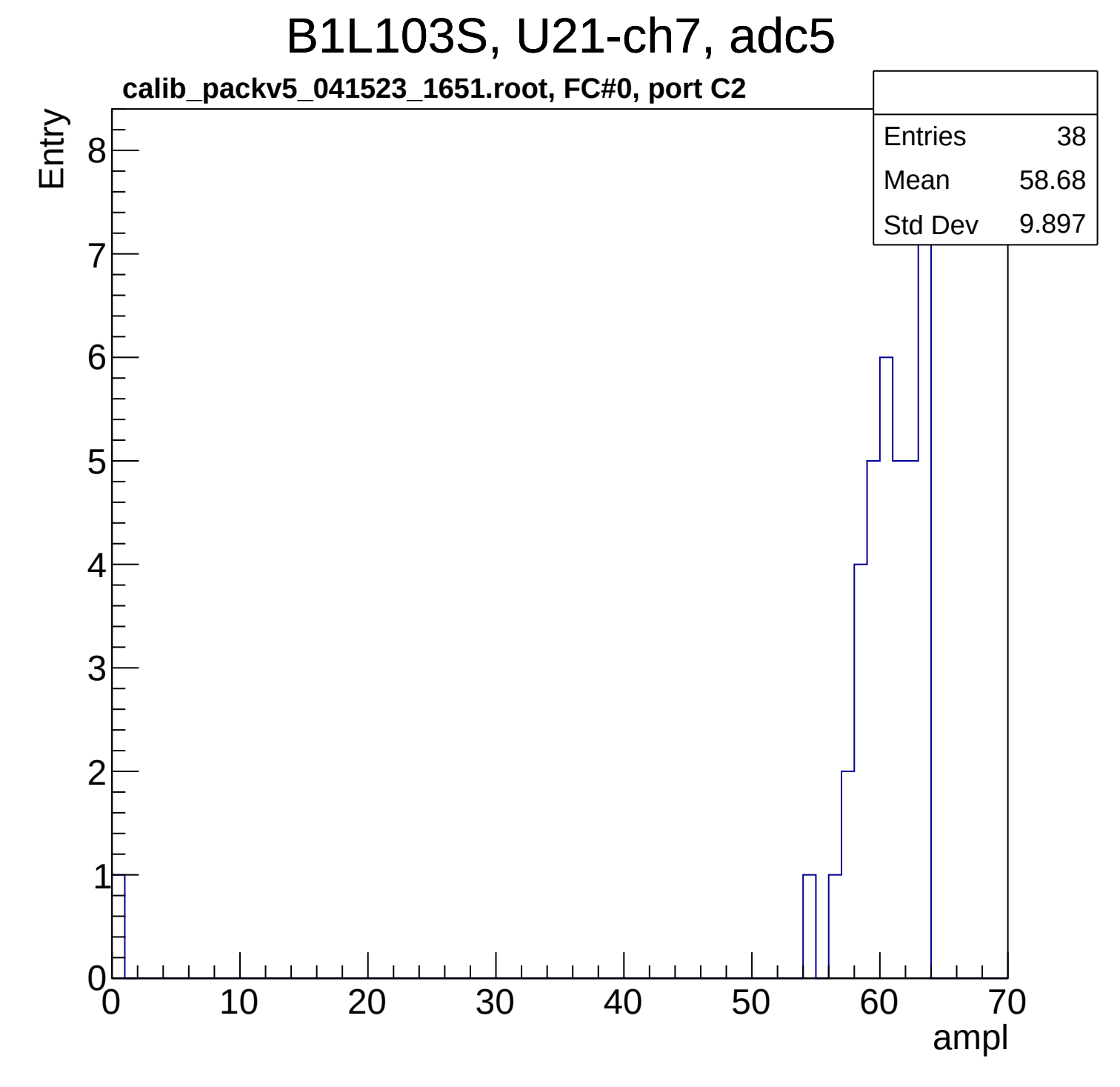
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U21-ch7, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 58.68
Std Dev 9.897
Entry
ampl
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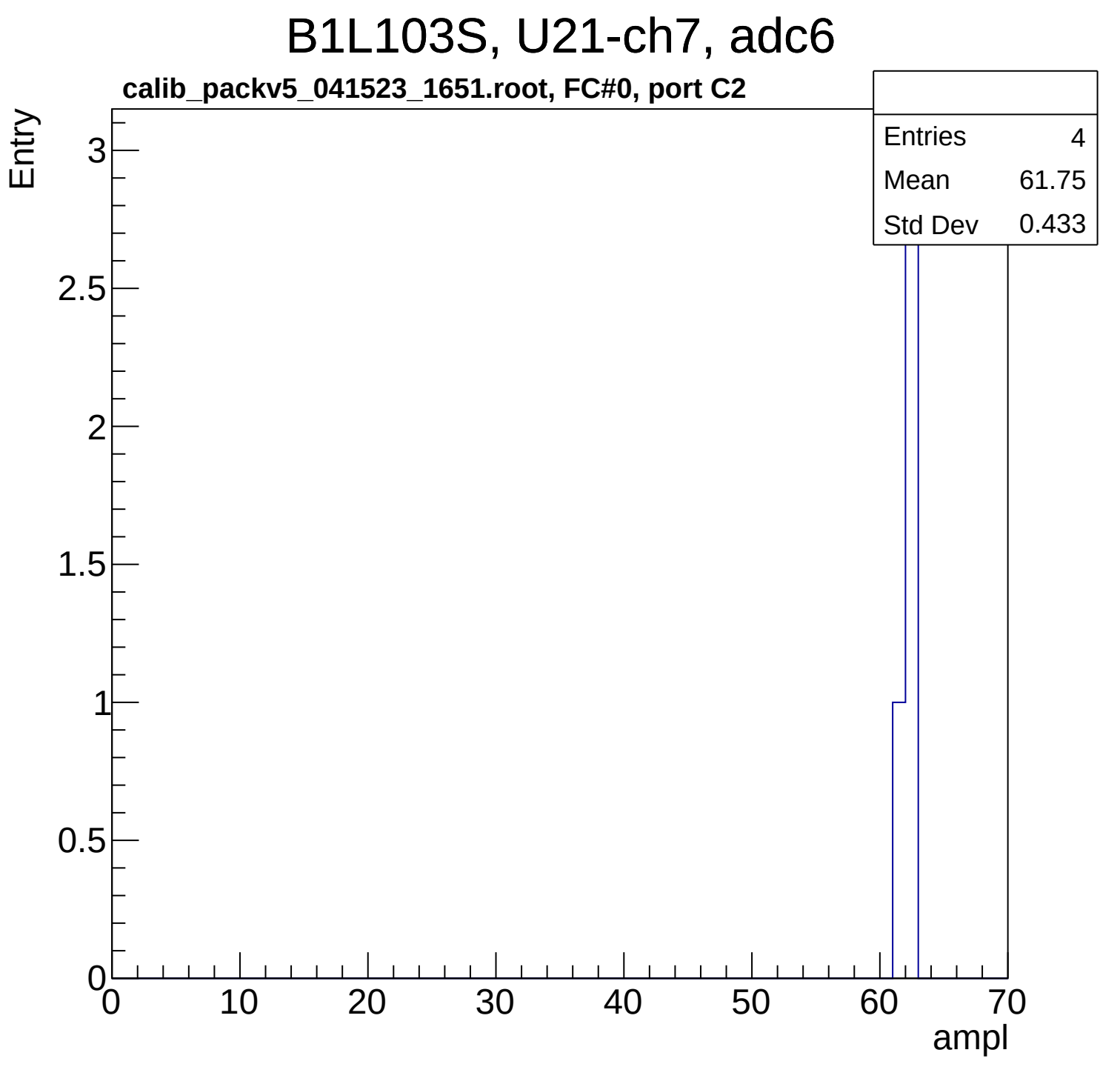
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch7, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 61.75
Std Dev 0.433
Entry
ampl
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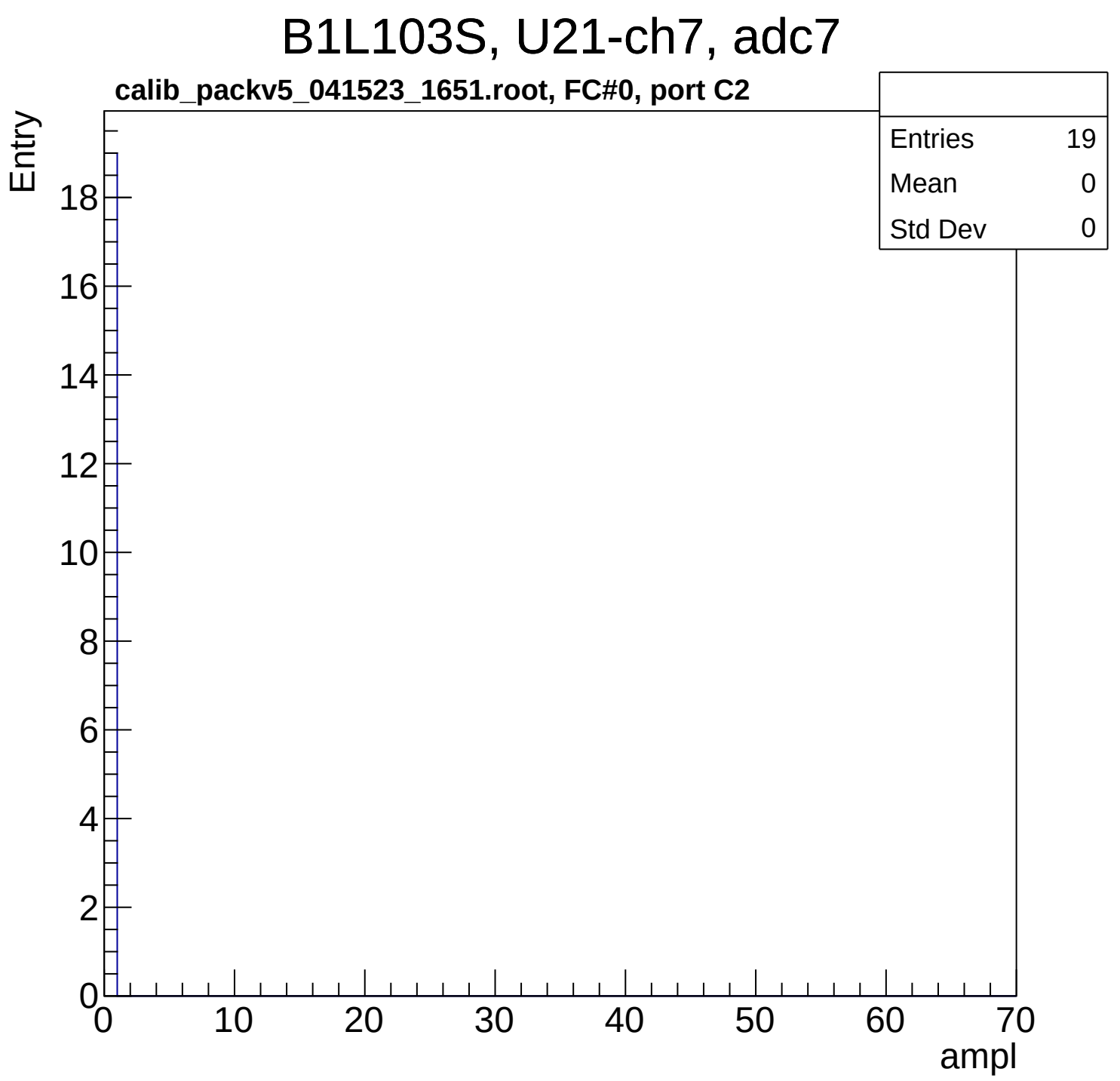
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U21-ch7, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
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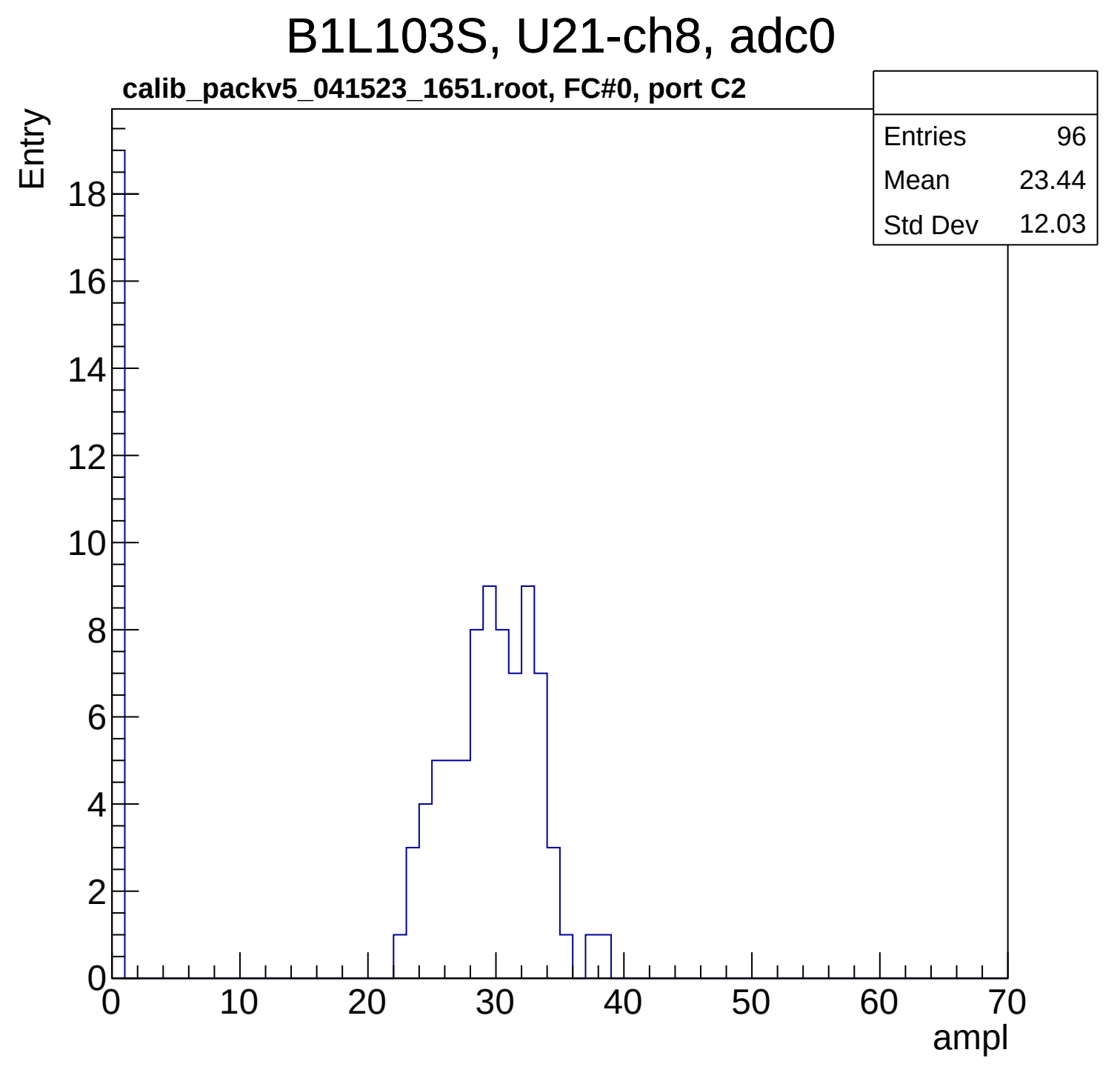
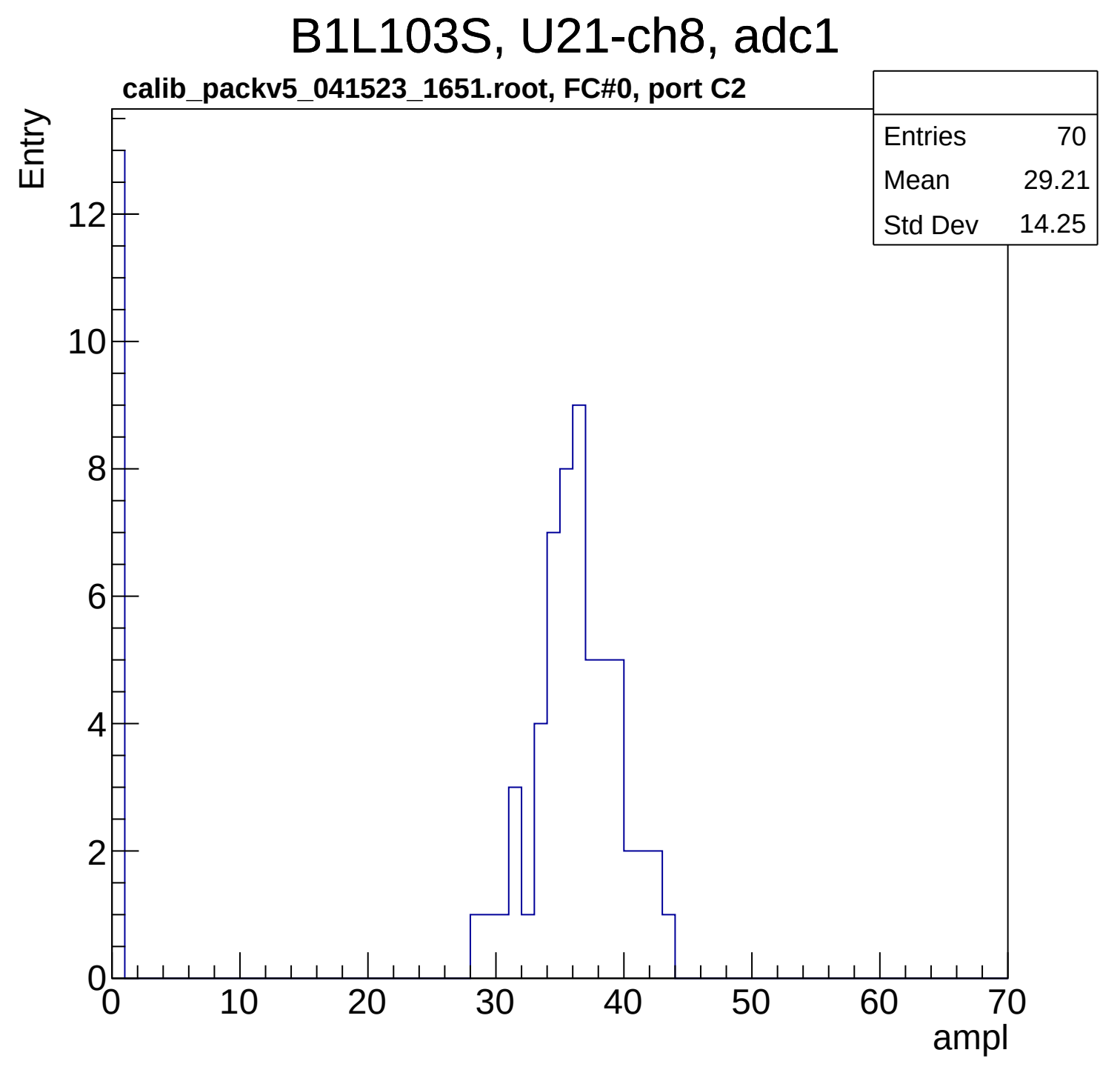
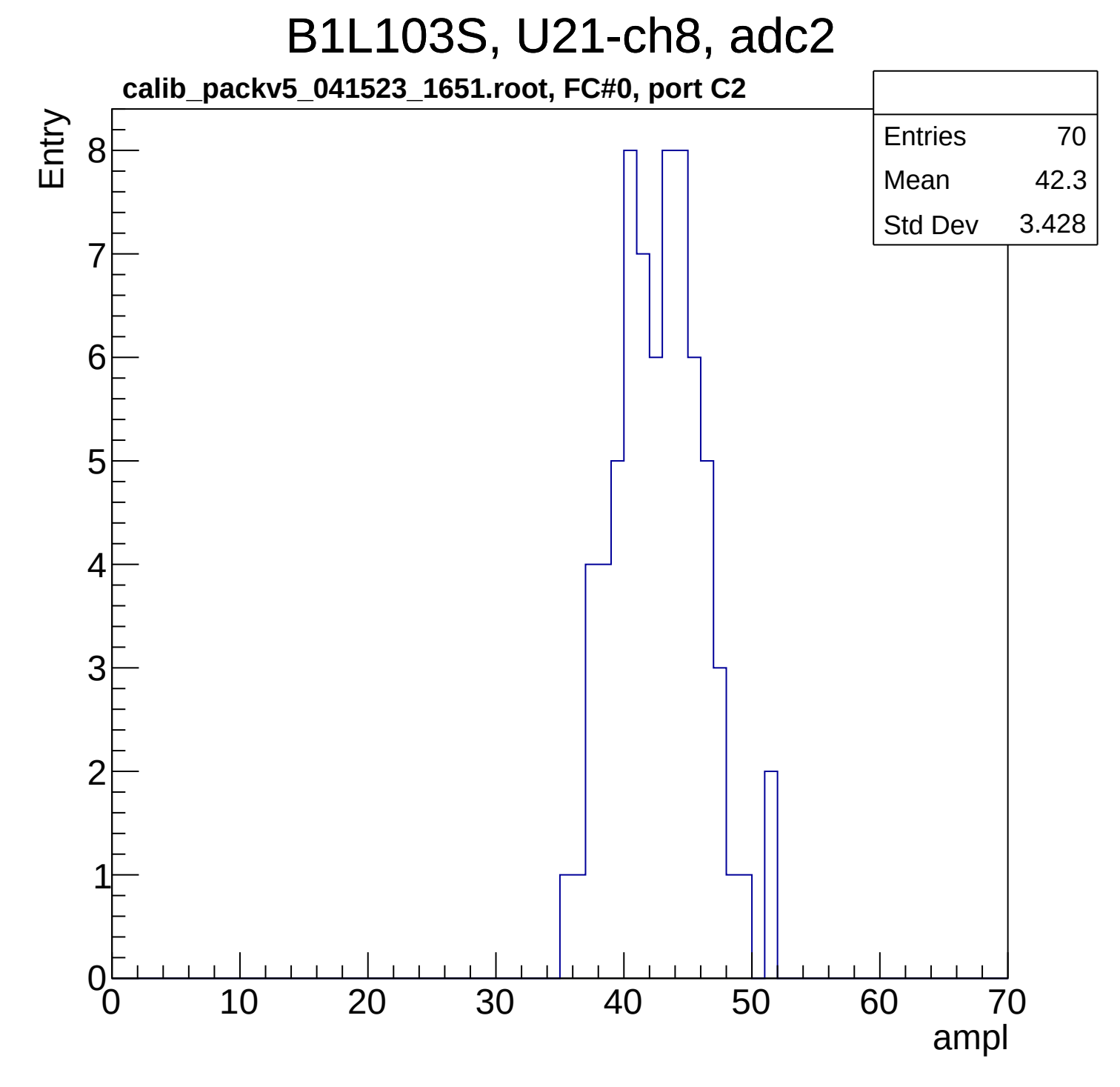
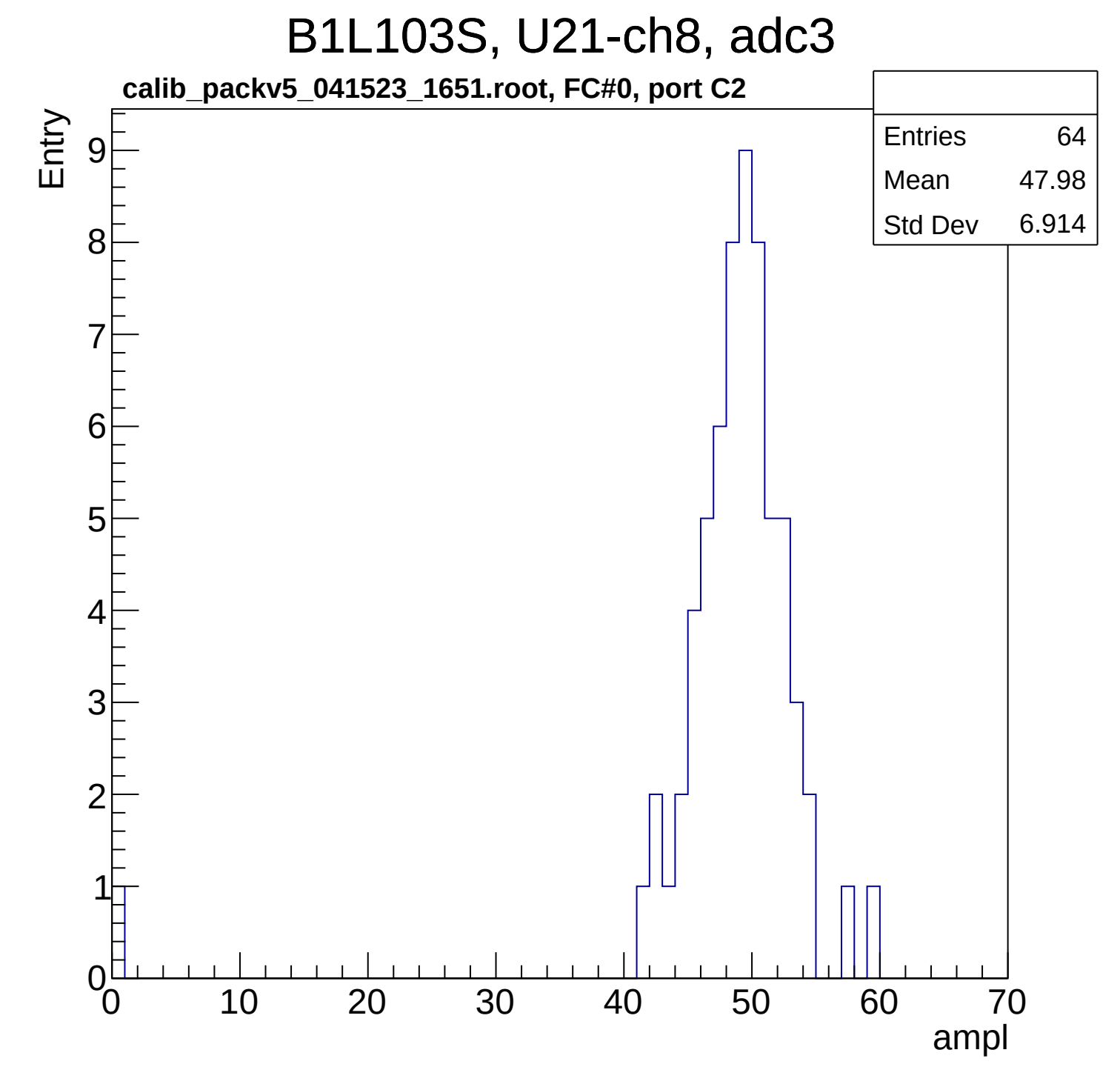
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch8, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 96
Mean 23.44
Std Dev 12.03
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch8, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 29.21
Std Dev 14.25
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch8, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 42.3
Std Dev 3.428
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch8, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 47.98
Std Dev 6.914
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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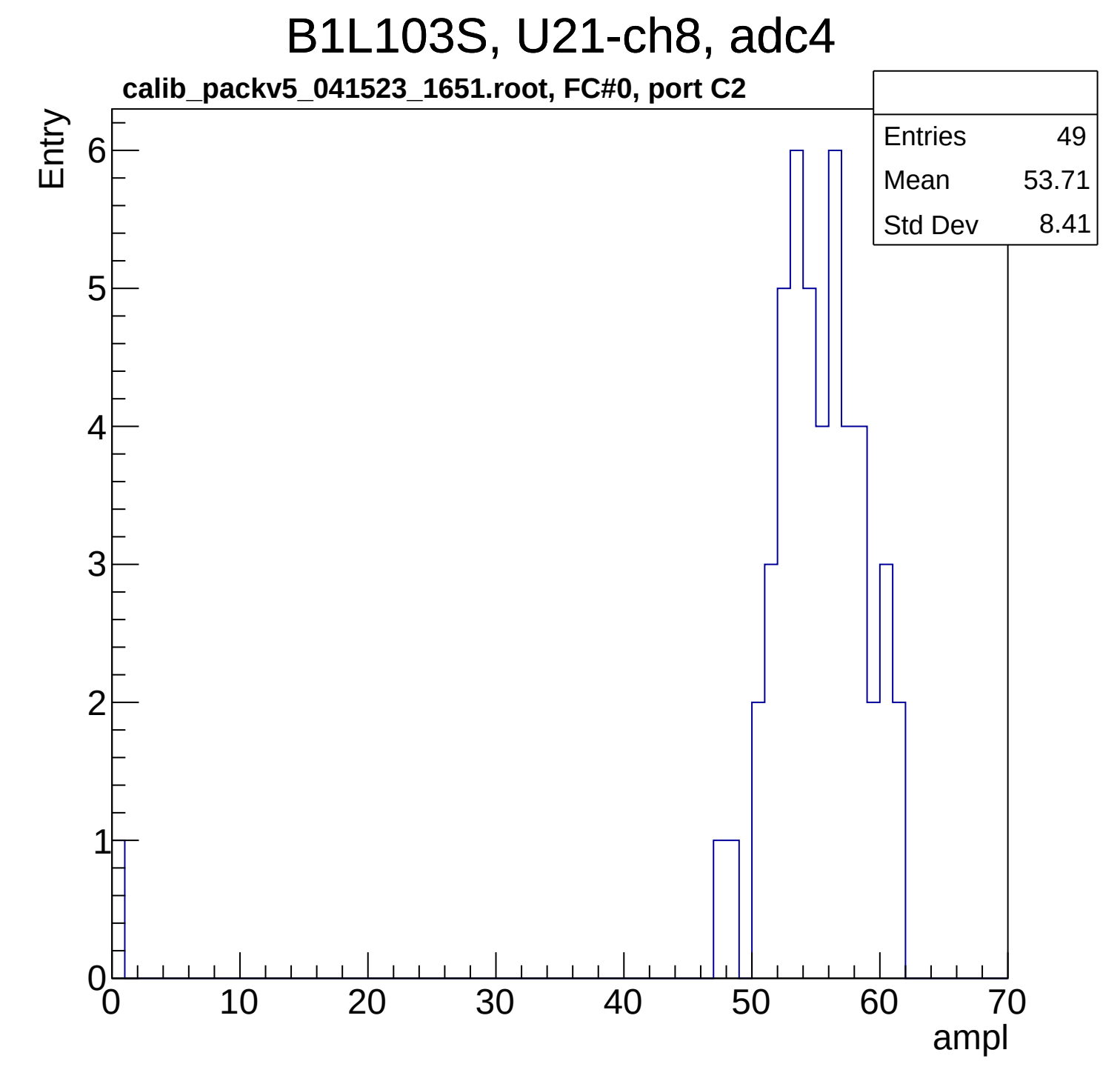
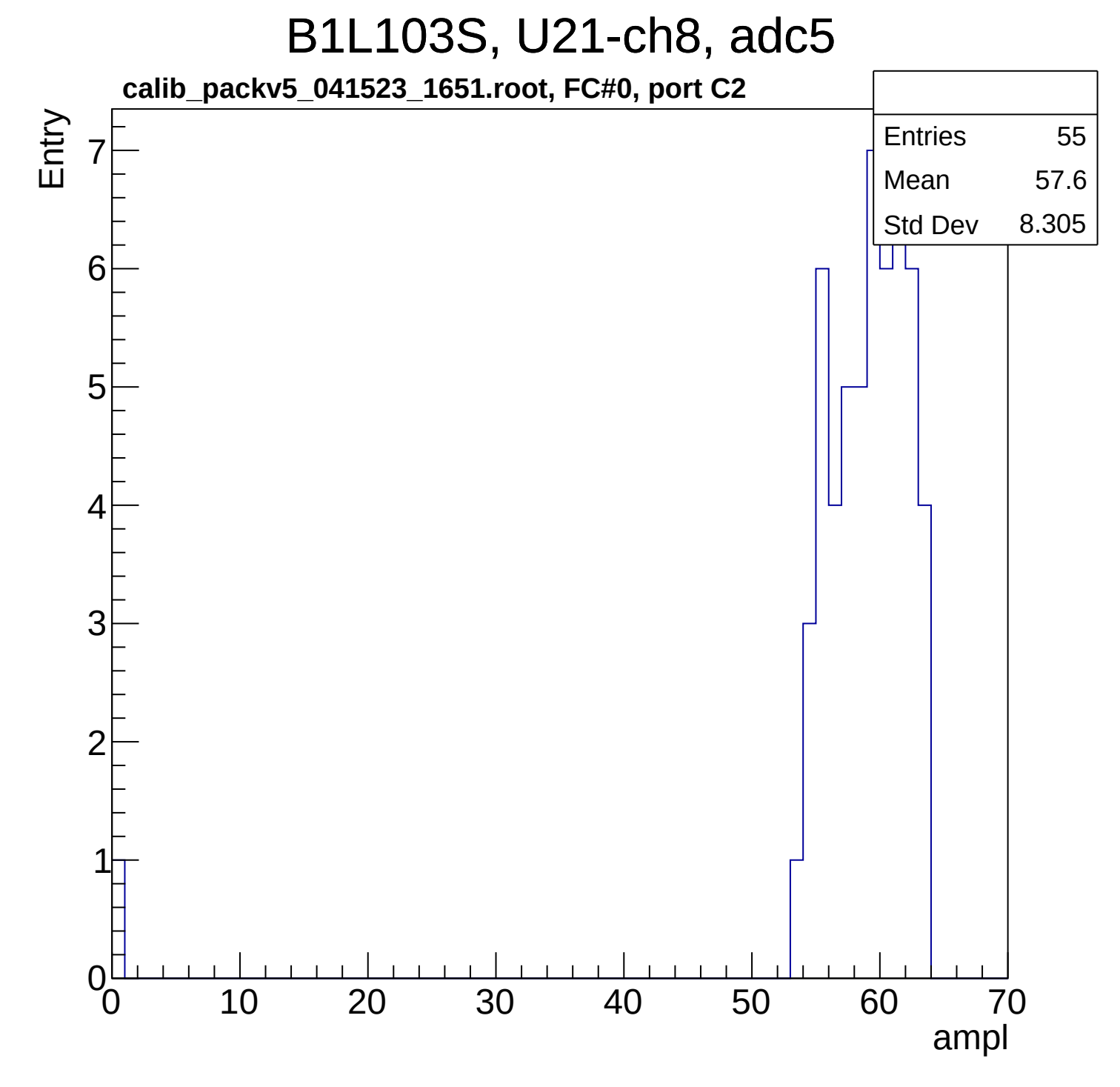
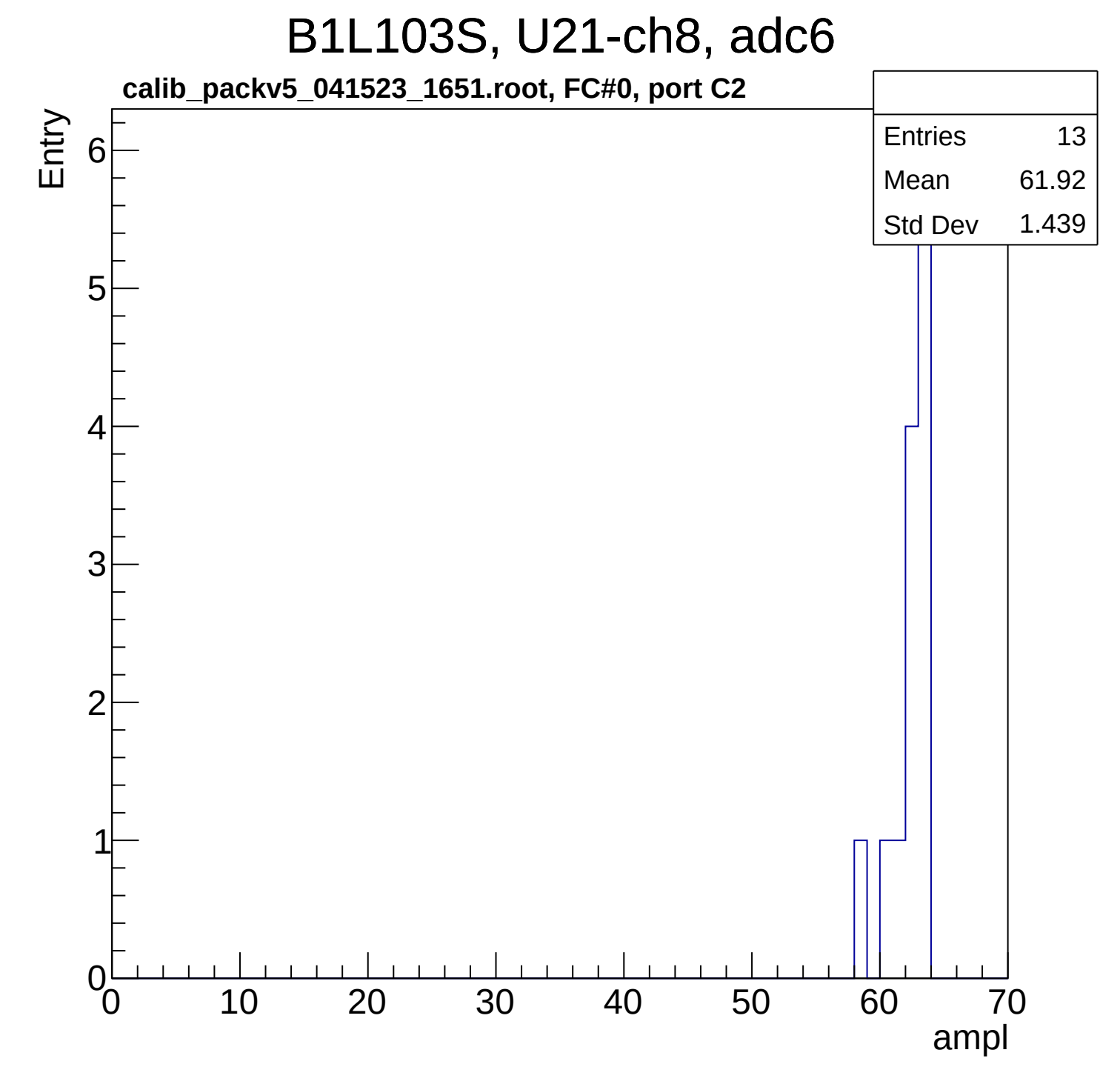
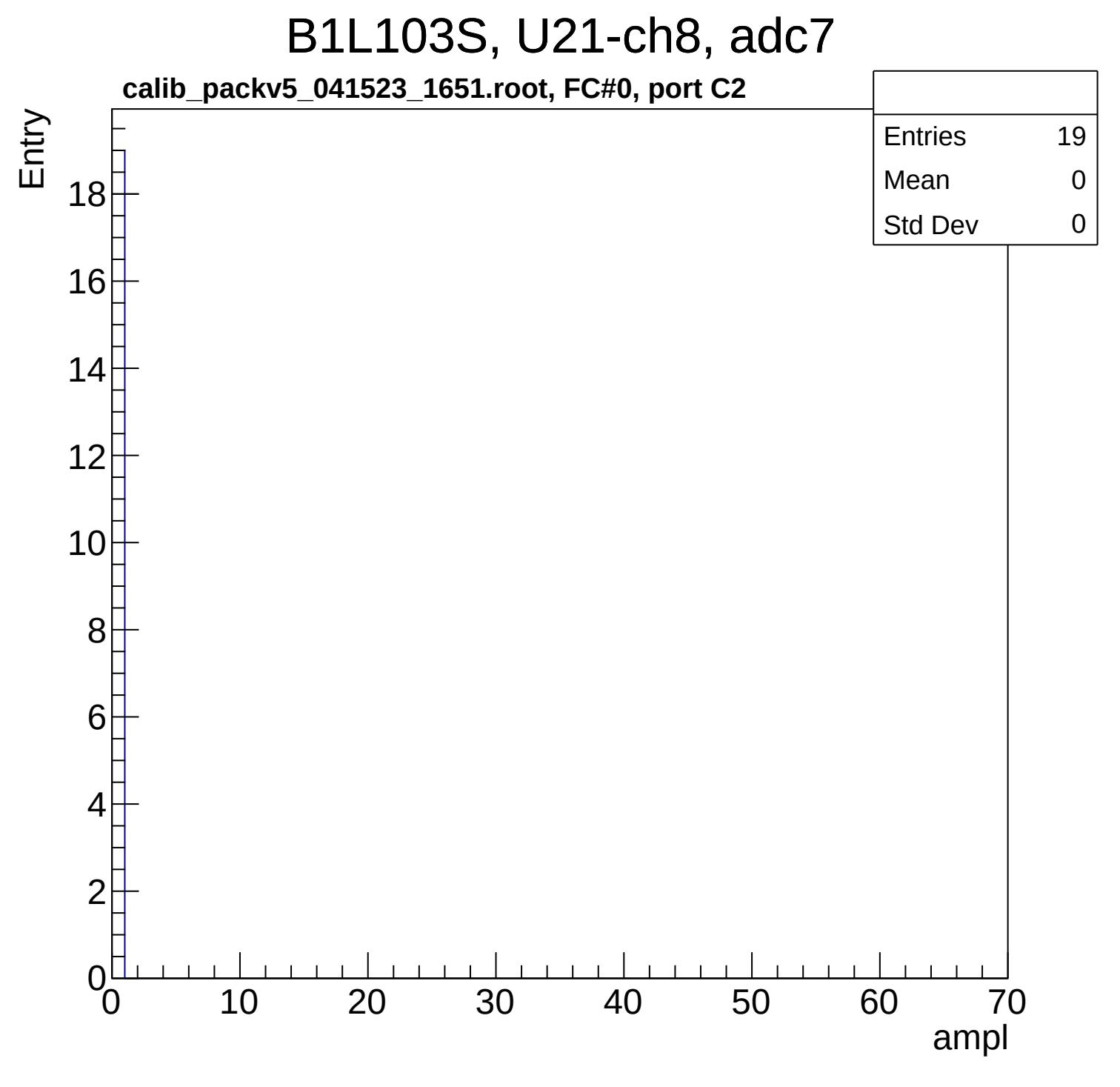
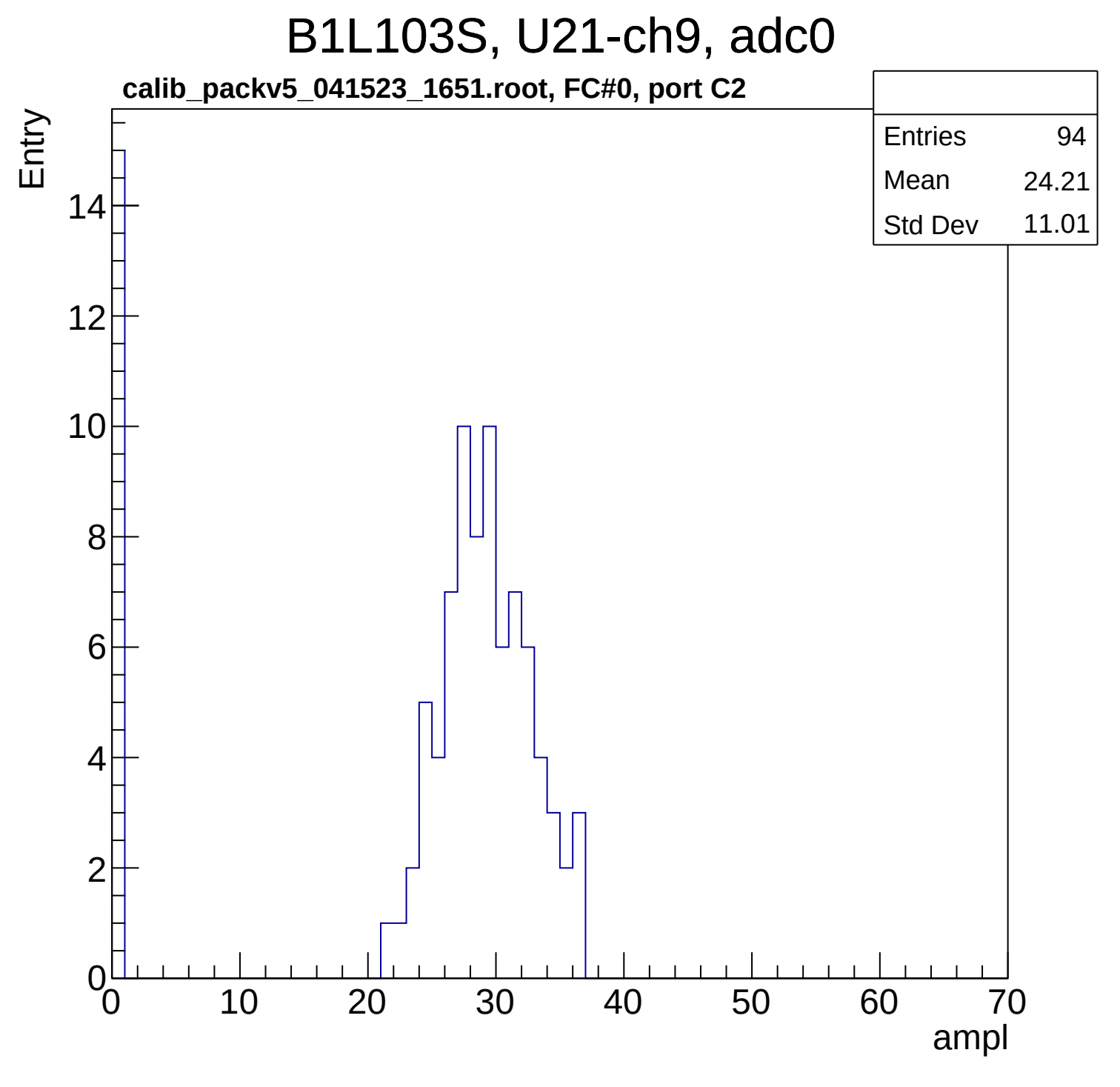
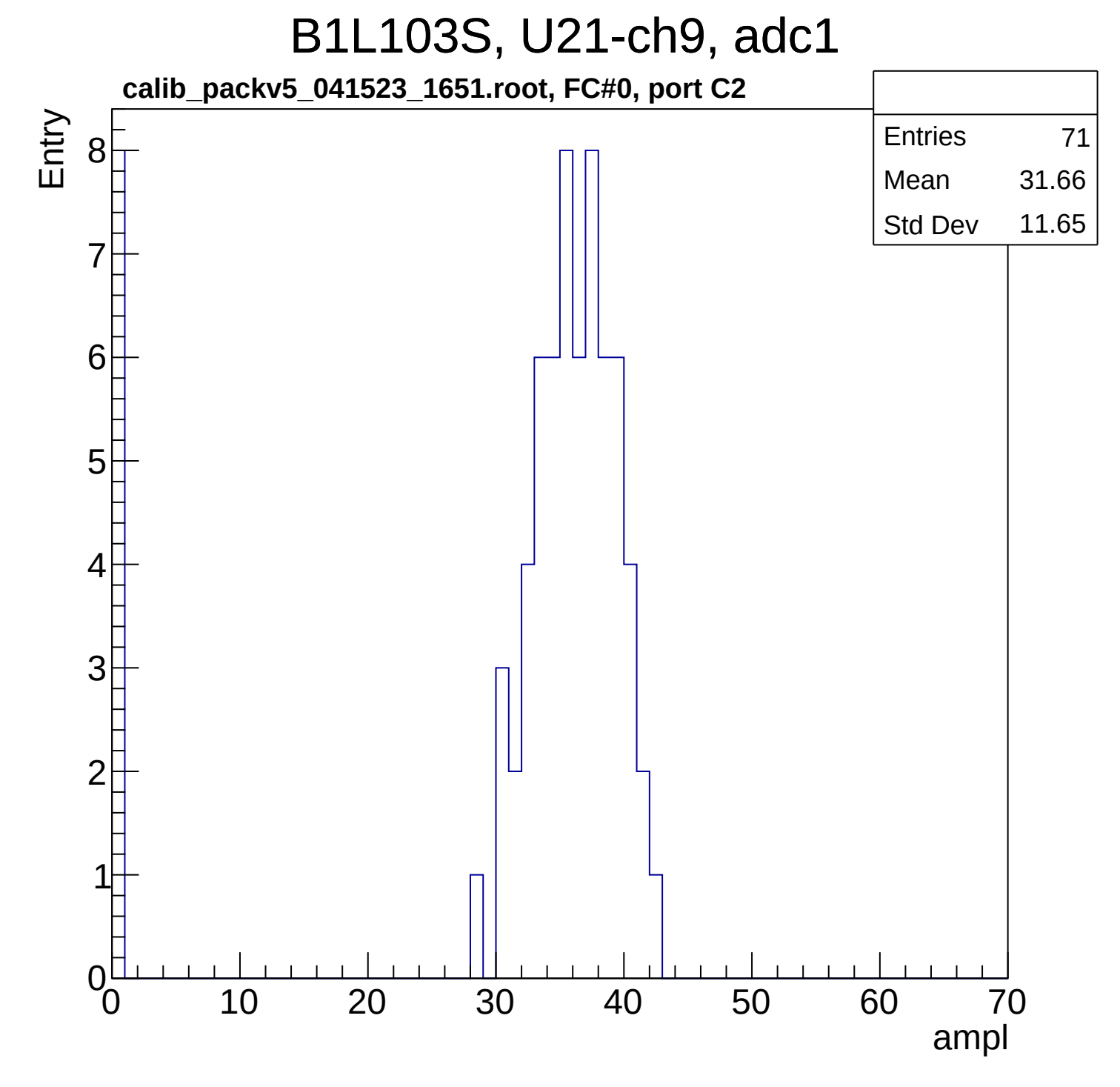

B1L103S, U21-ch8, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 53.71
Std Dev 8.41
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

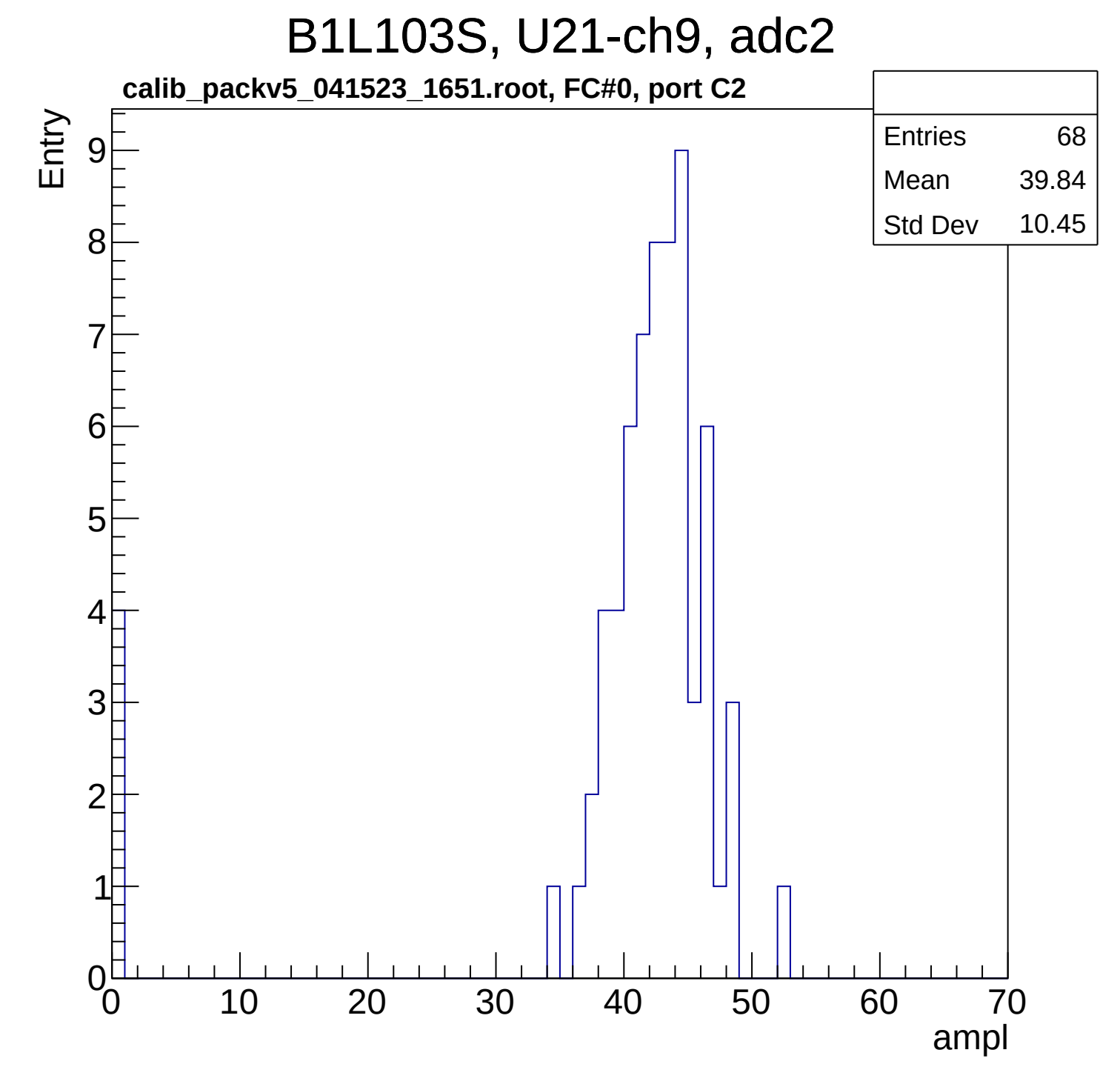

B1L103S, U21-ch8, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 57.6
Std Dev 8.305
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

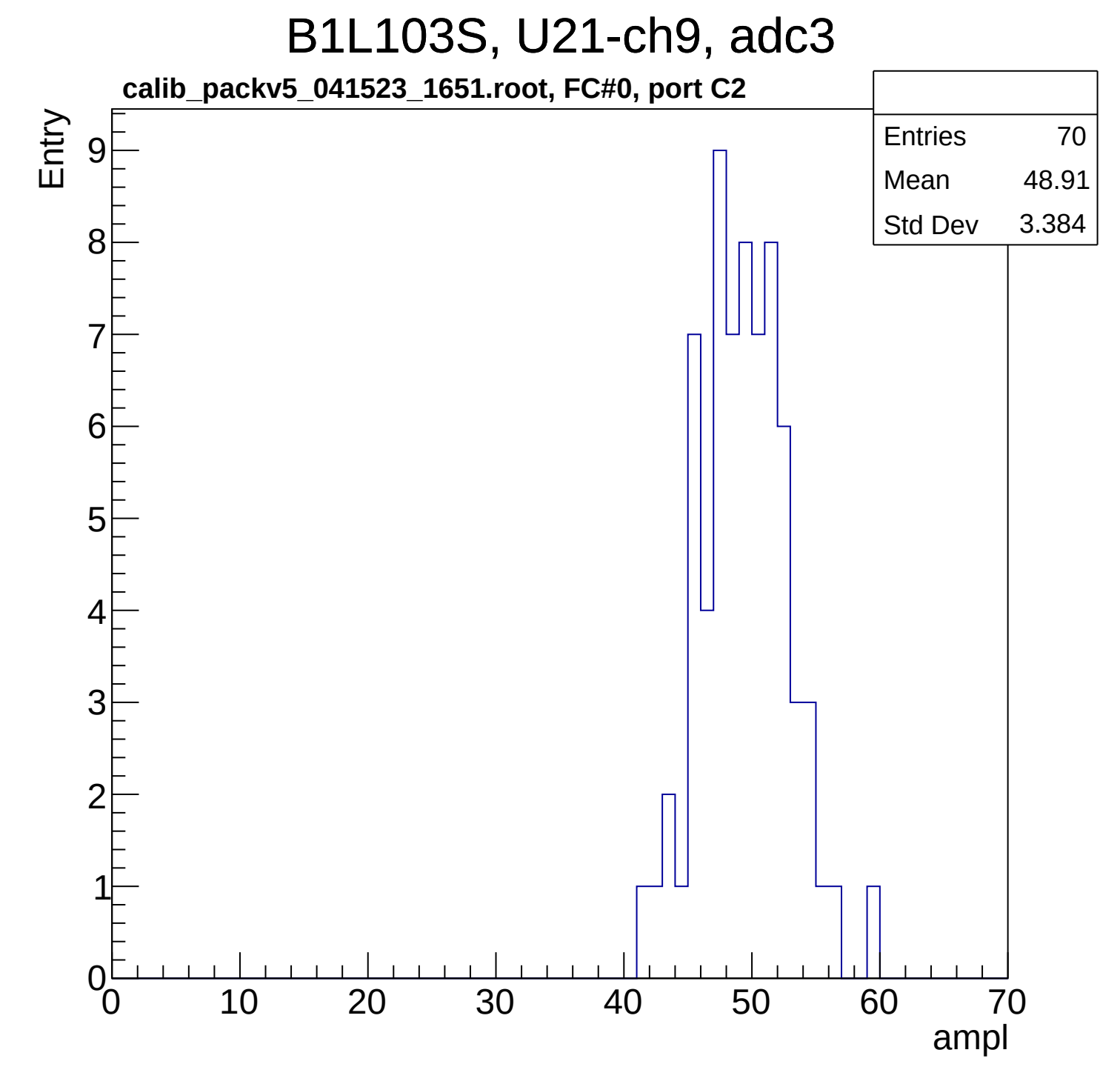

B1L103S, U21-ch8, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 61.92
Std Dev 1.439
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

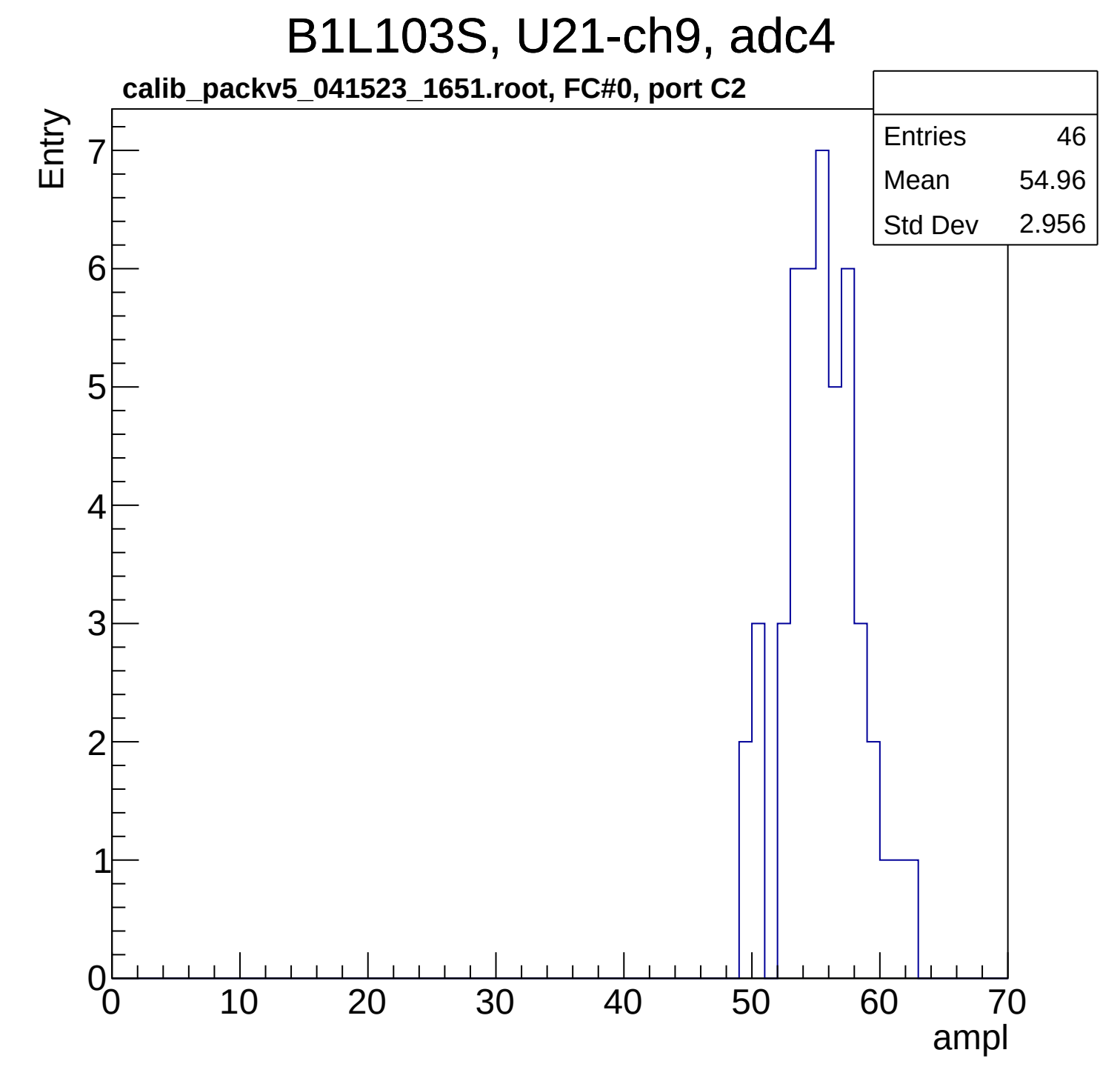

B1L103S, U21-ch8, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

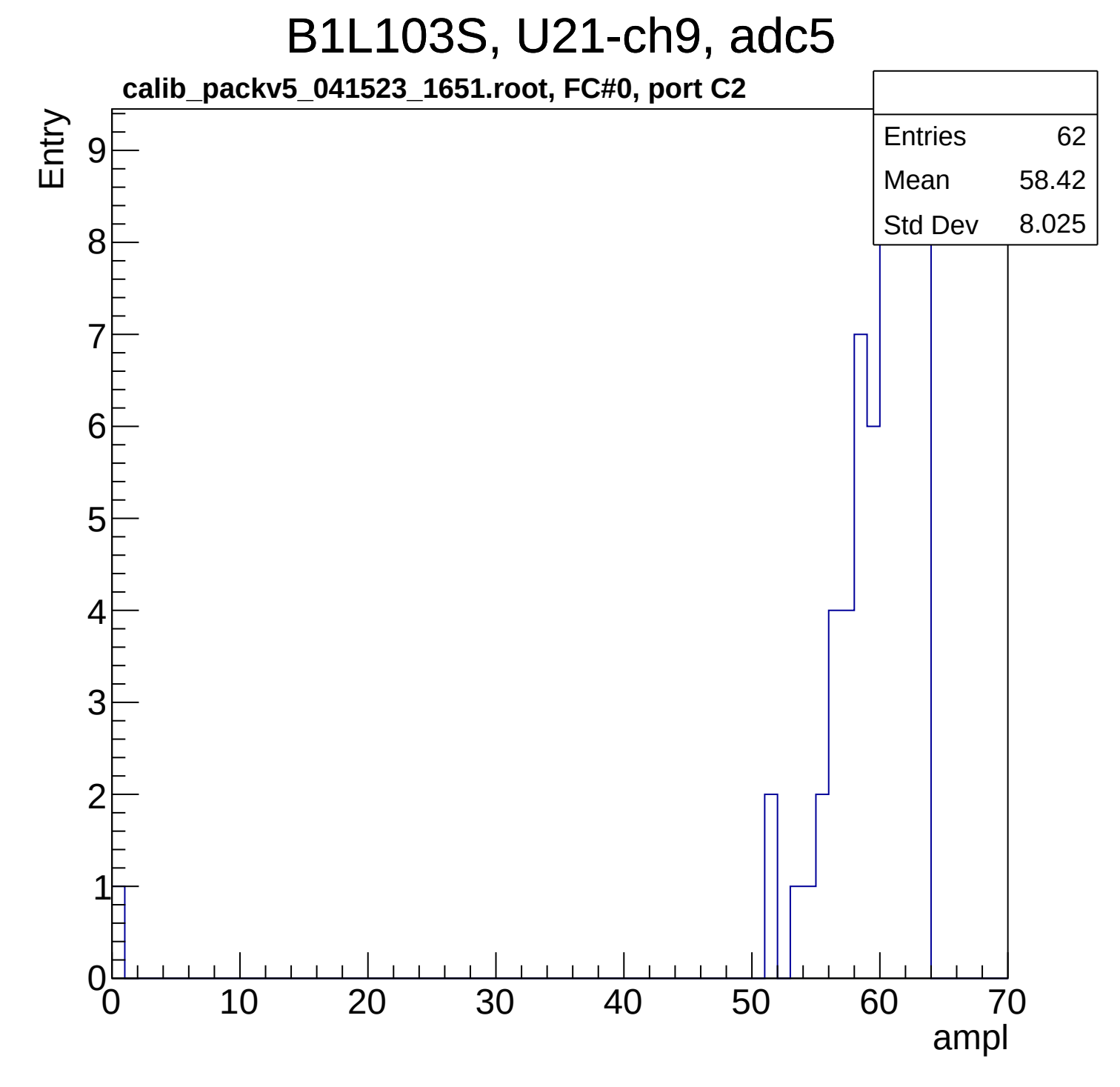

B1L103S, U21-ch9, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 24.21
Std Dev 11.01
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch9, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 31.66
Std Dev 11.65
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch9, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 39.84
Std Dev 10.45
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch9, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 48.91
Std Dev 3.384
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch9, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 54.96
Std Dev 2.956
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U21-ch9, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 58.42
Std Dev 8.025
Entry
ampl
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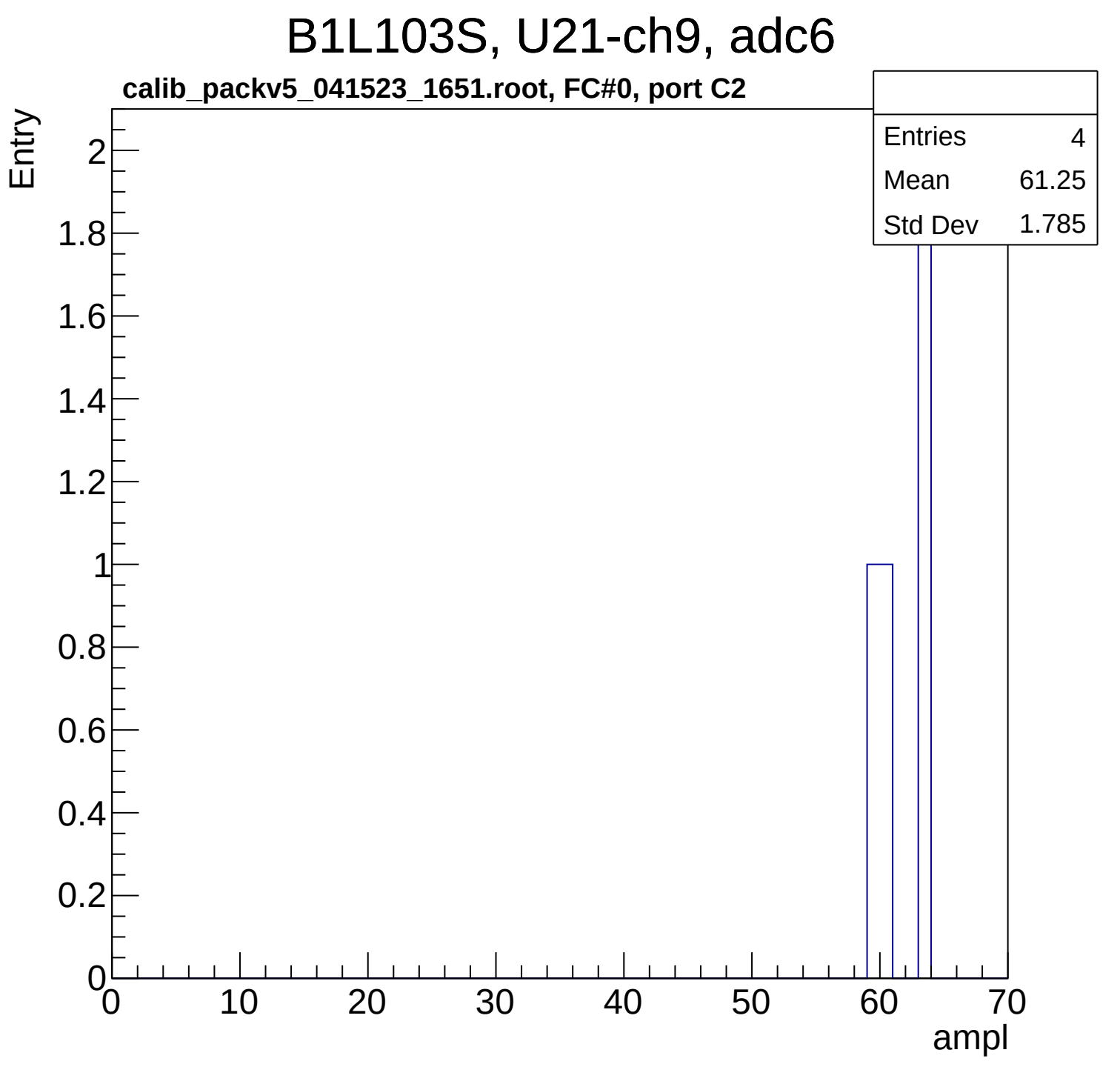
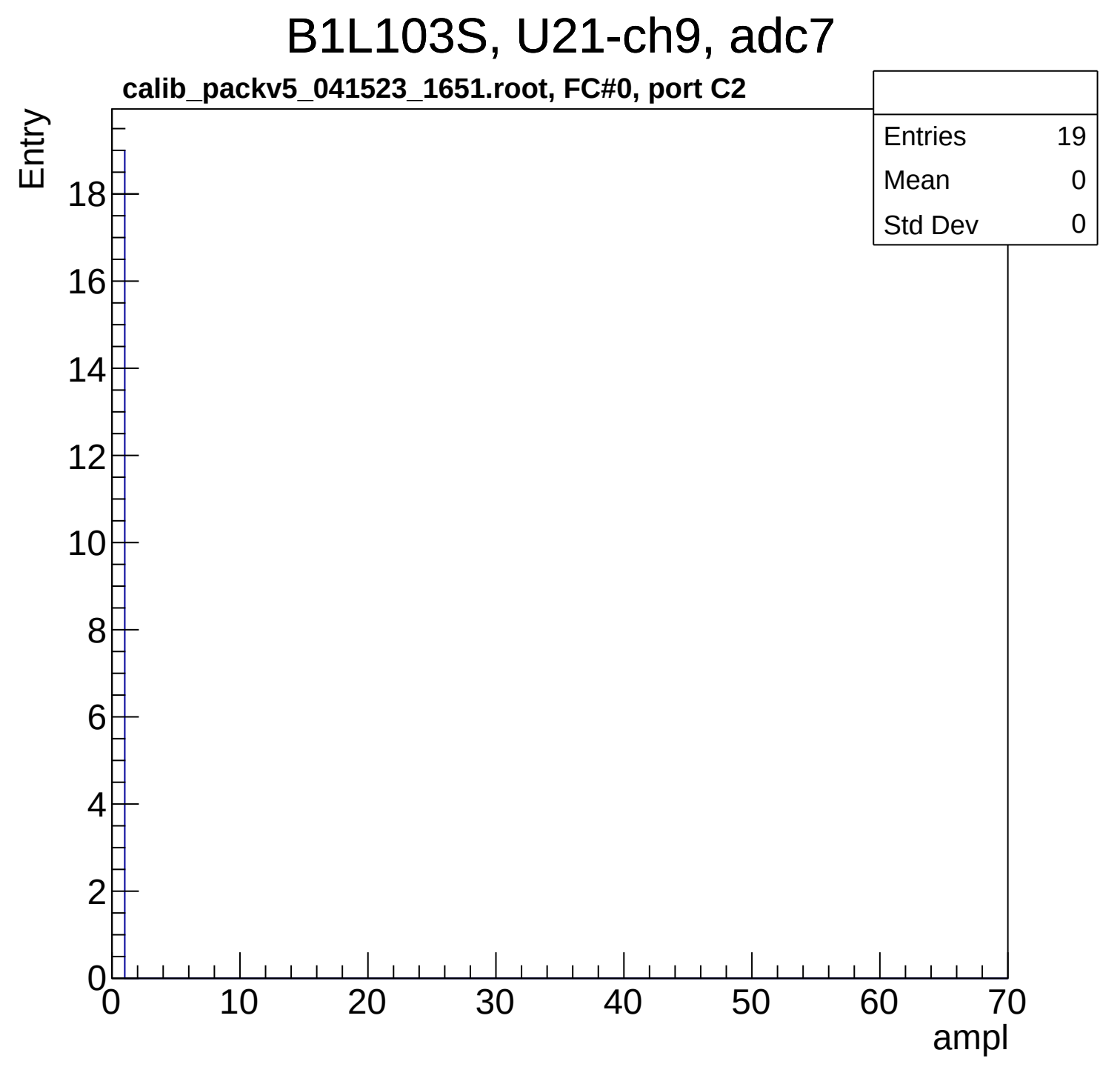
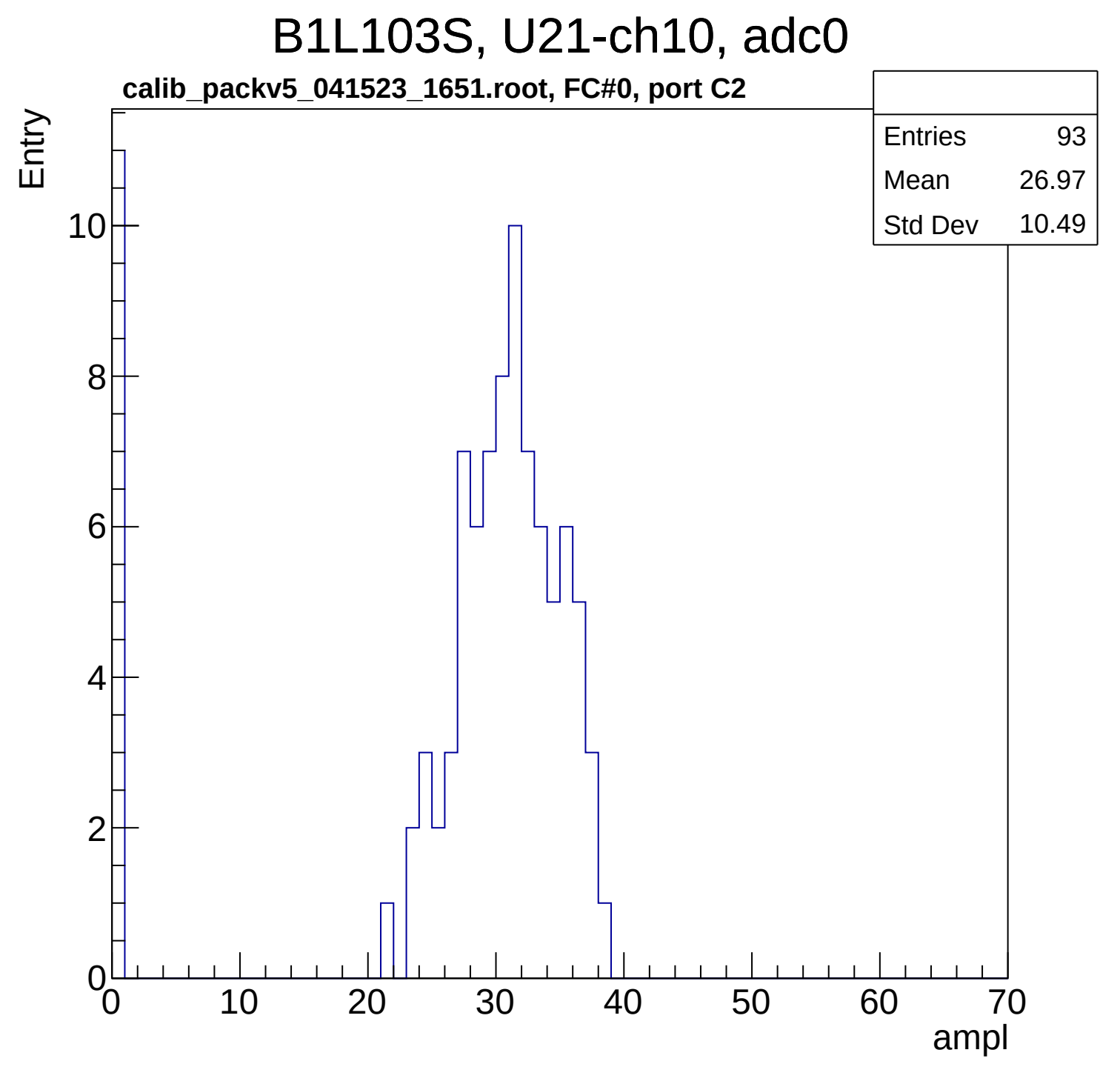
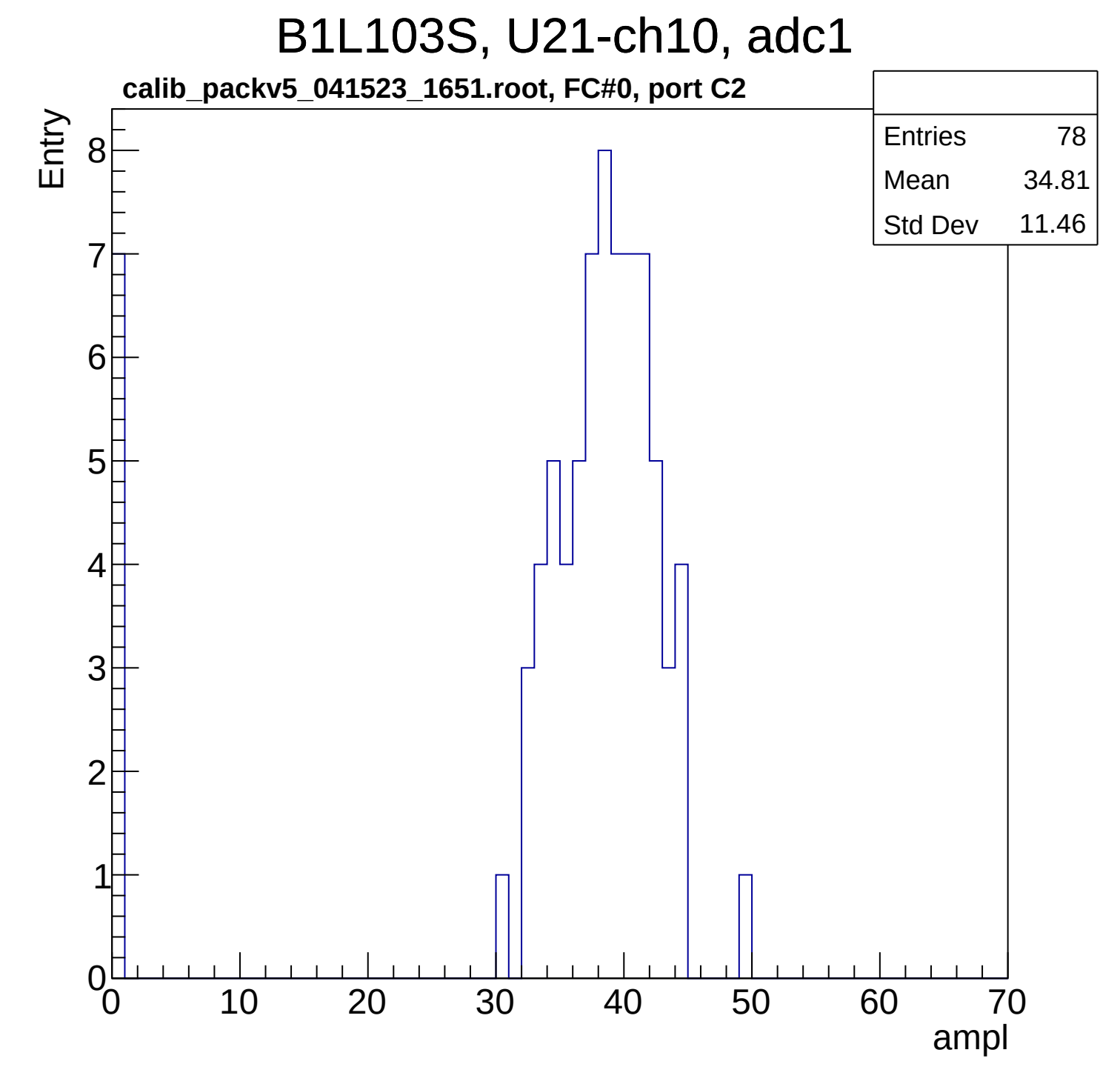
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch9, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 61.25
Std Dev 1.785
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U21-ch9, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch10, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 26.97
Std Dev 10.49
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch10, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 34.81
Std Dev 11.46
Entry
ampl
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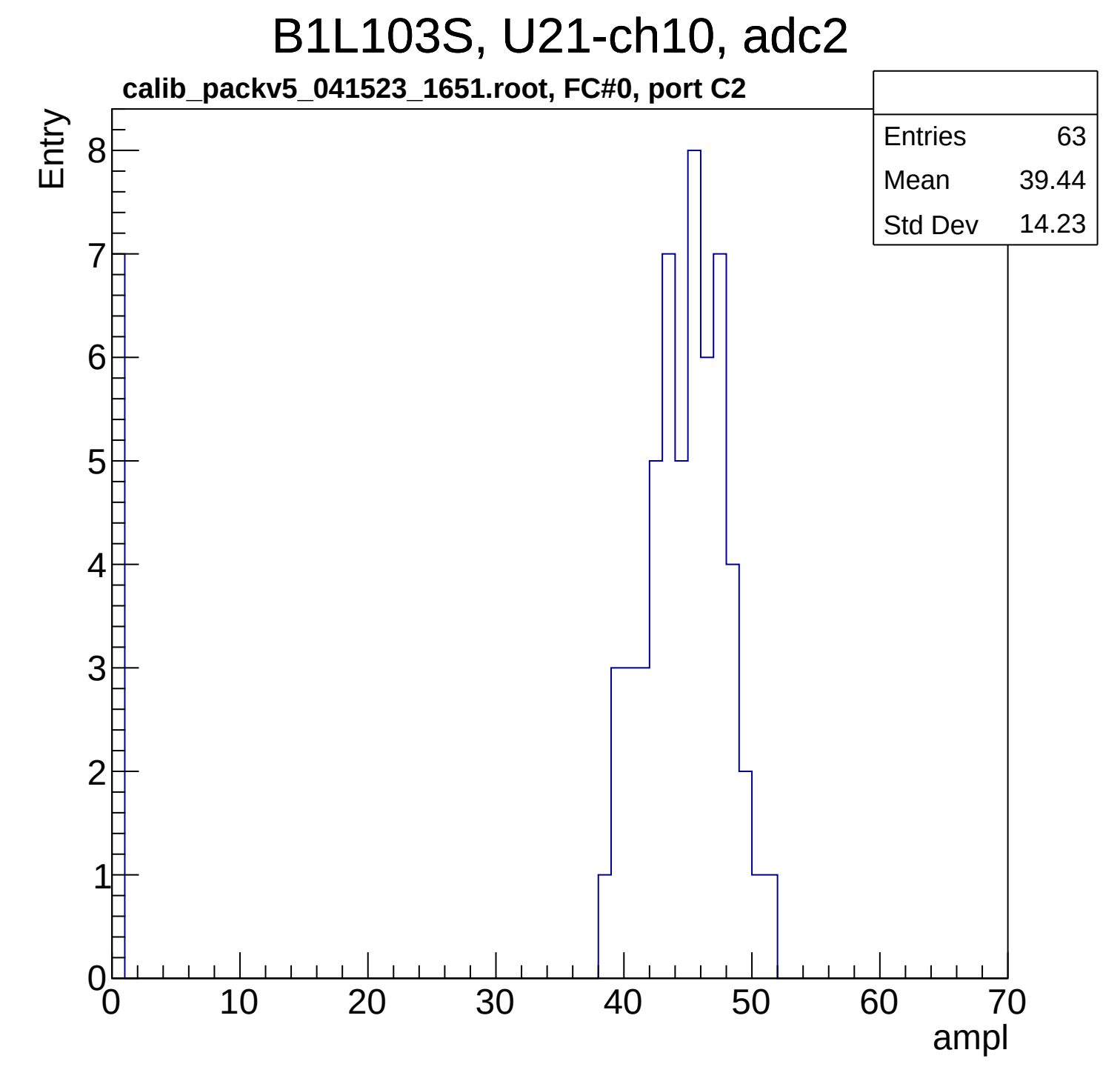
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch10, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 39.44
Std Dev 14.23
Entry
ampl
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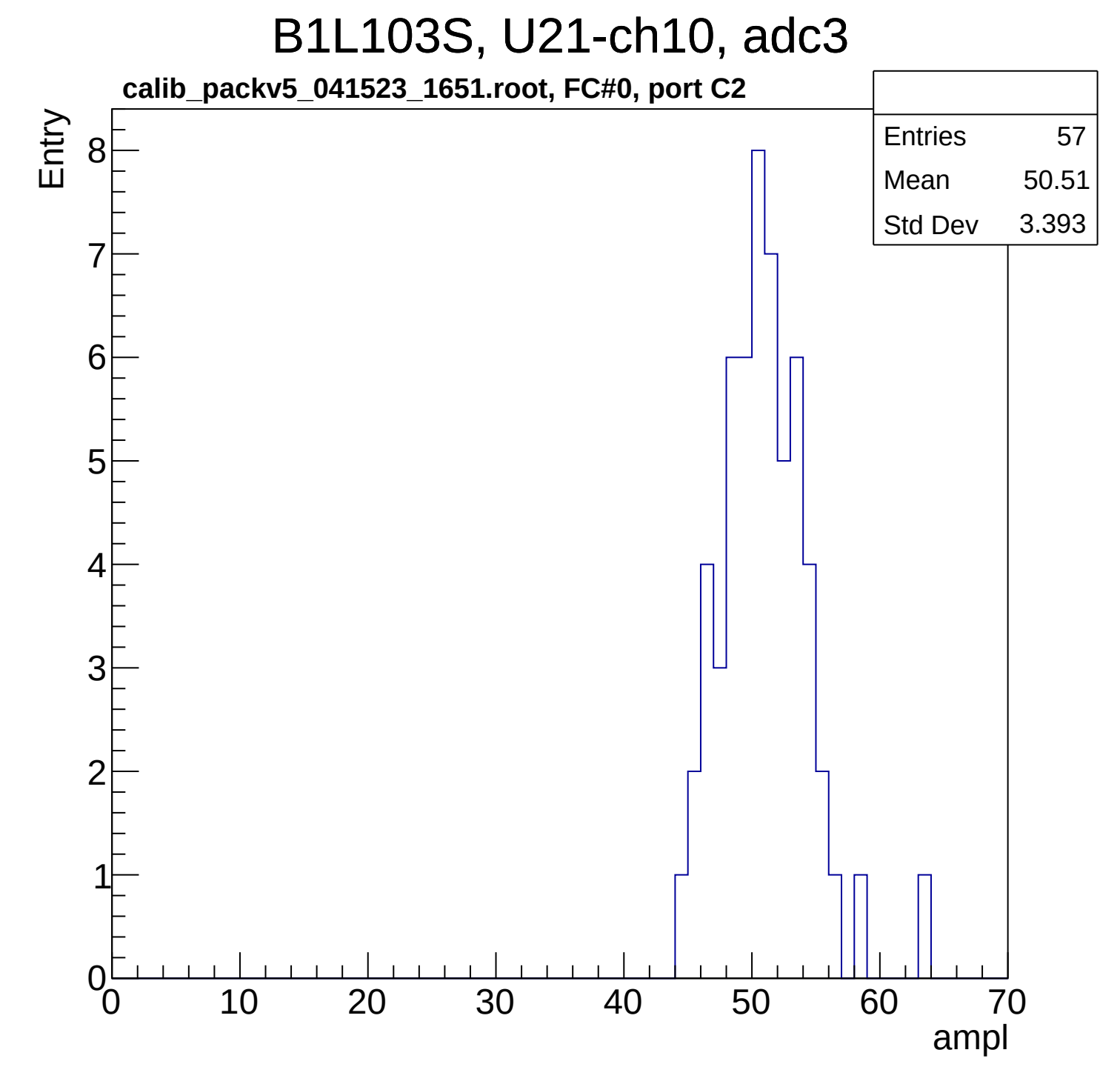
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch10, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 50.51
Std Dev 3.393
Entry
ampl
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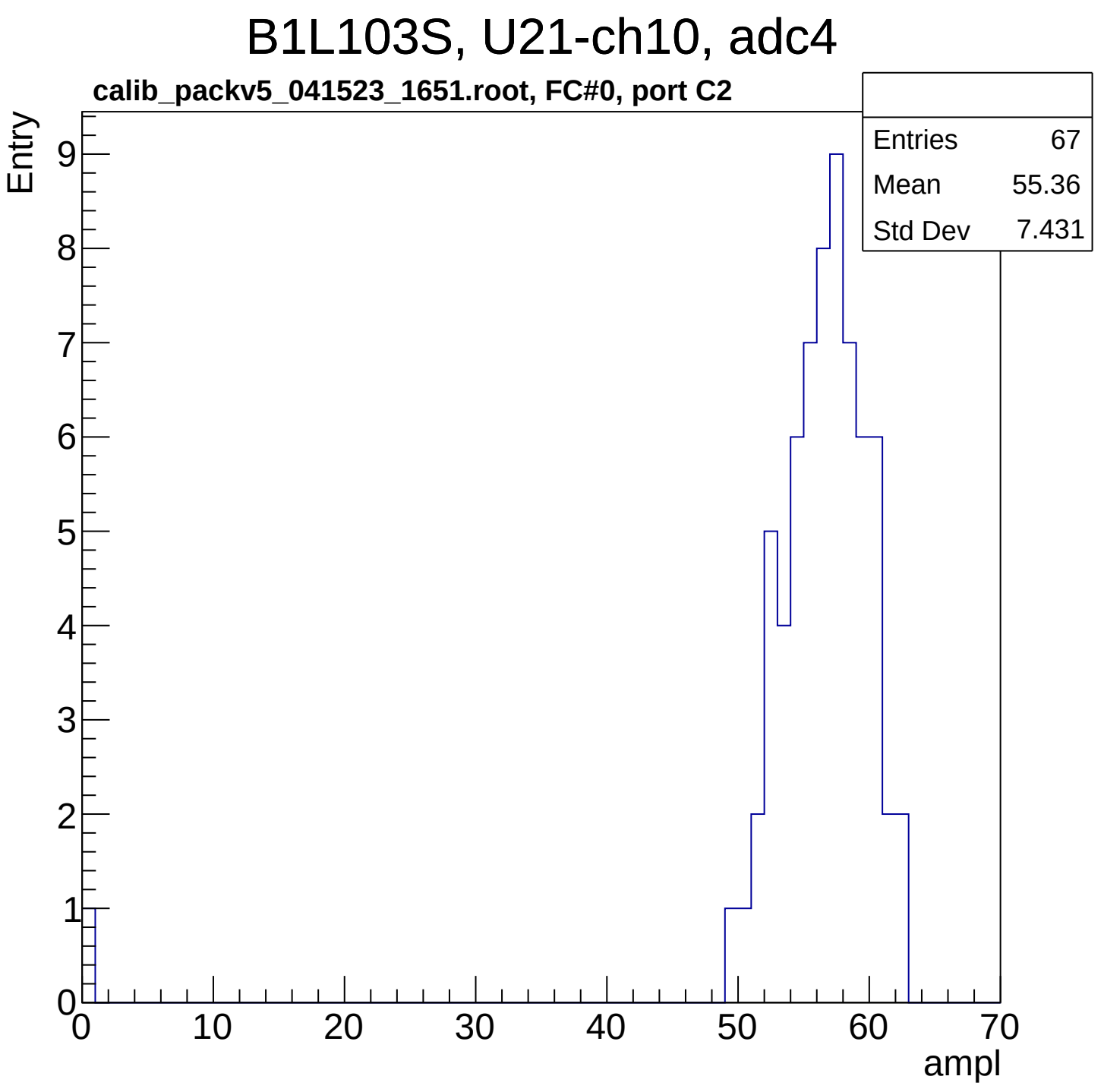
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch10, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 55.36
Std Dev 7.431
Entry
ampl
0
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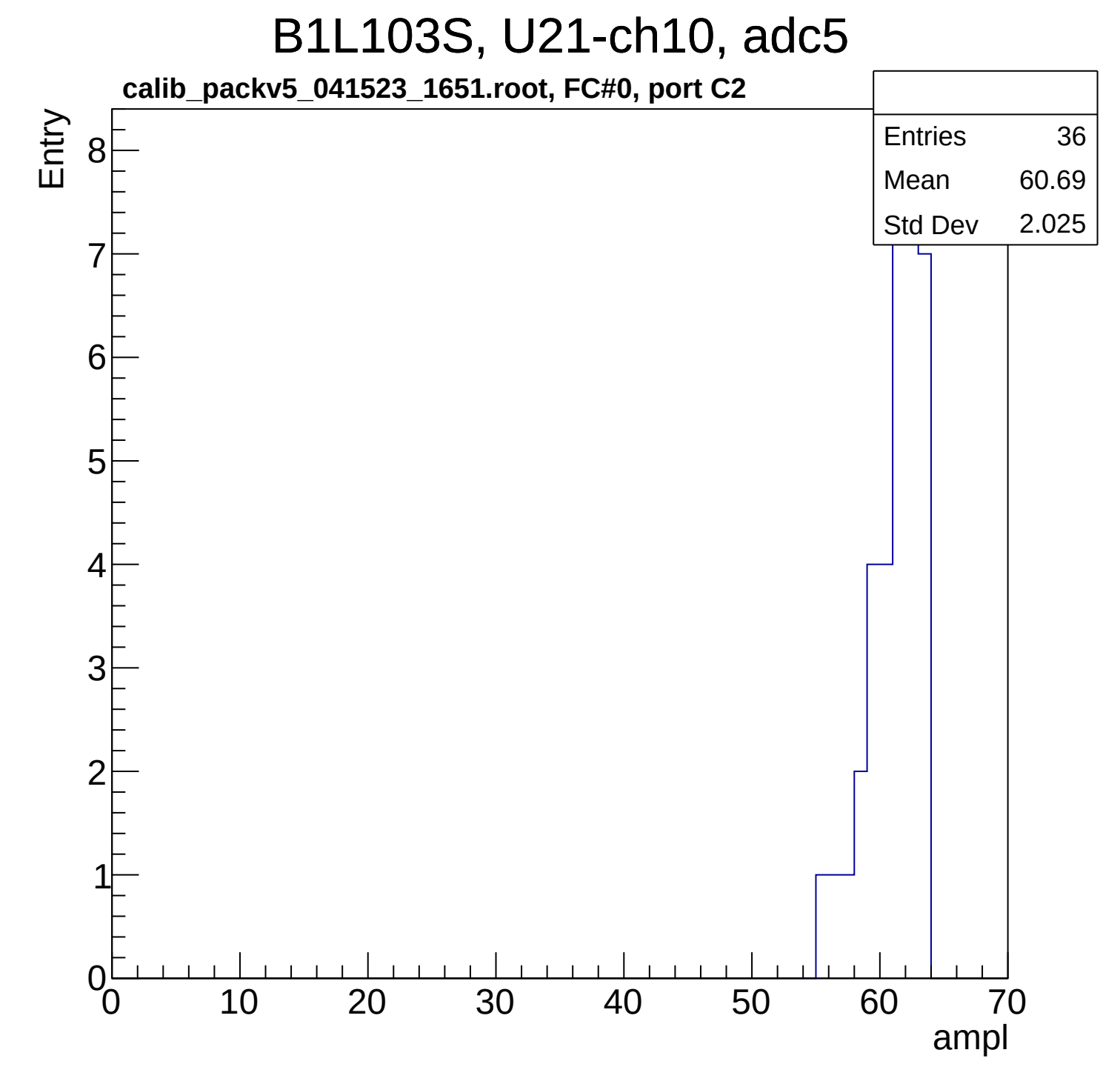
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch10, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 60.69
Std Dev 2.025
Entry
ampl
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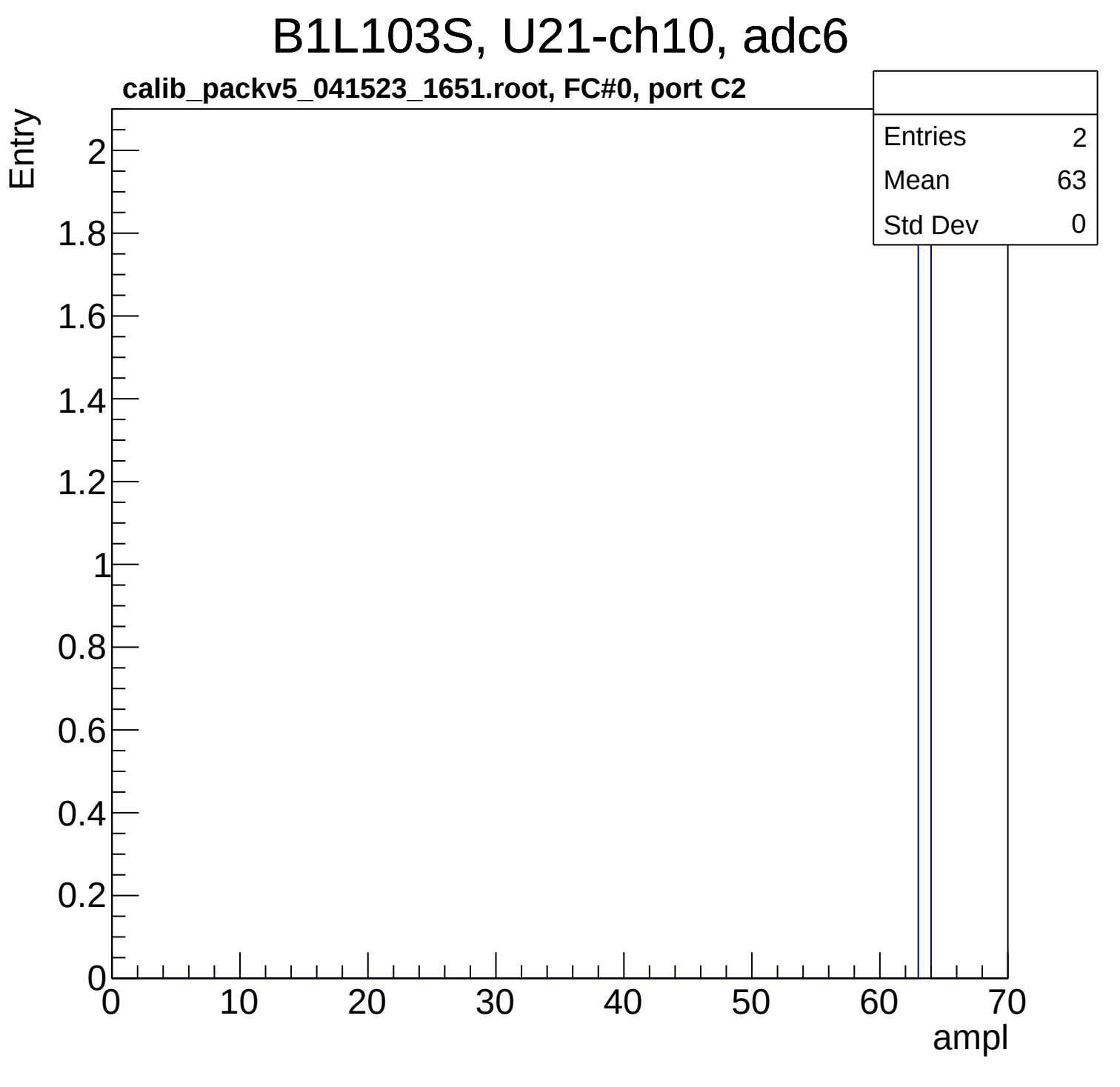
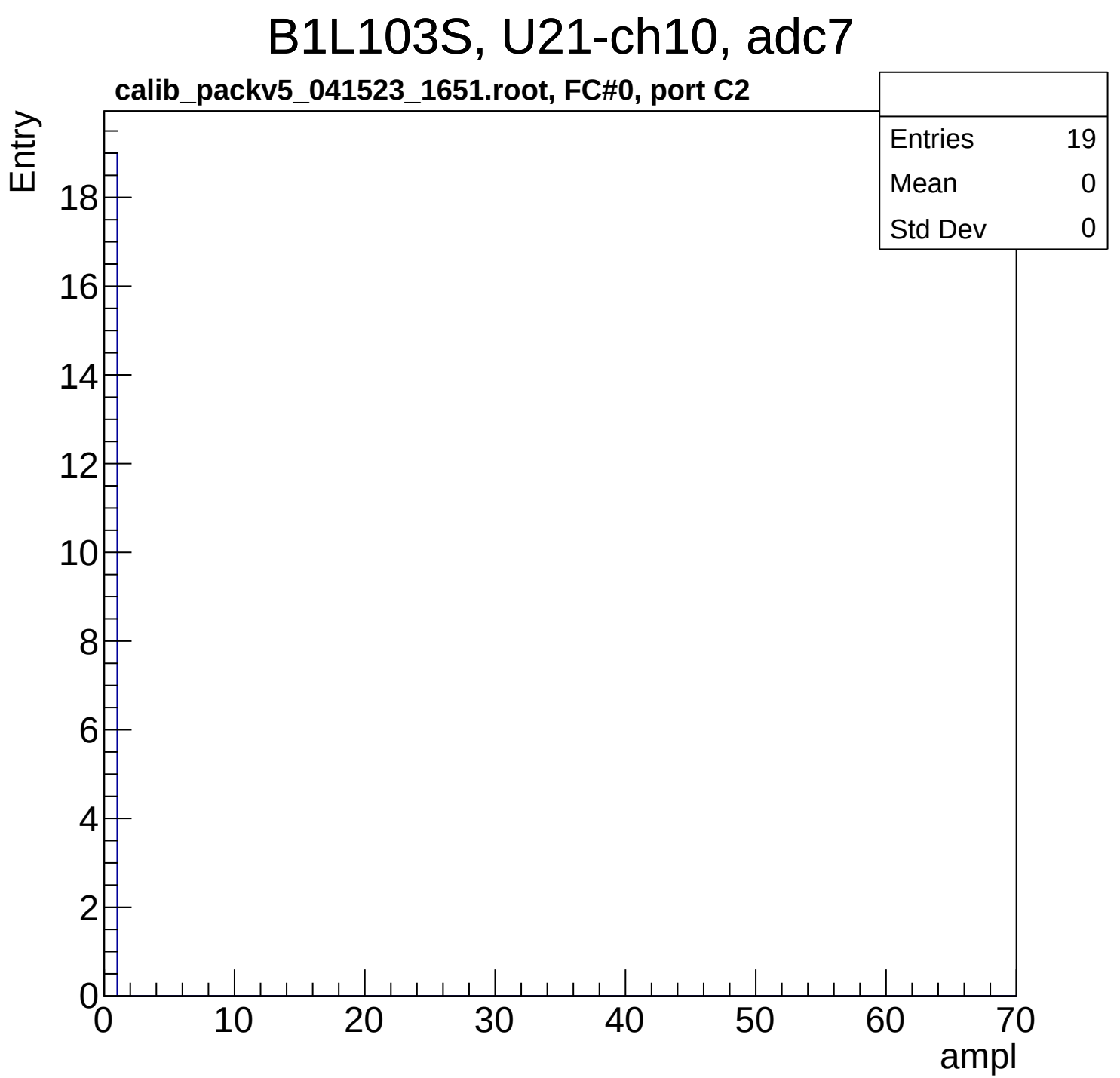
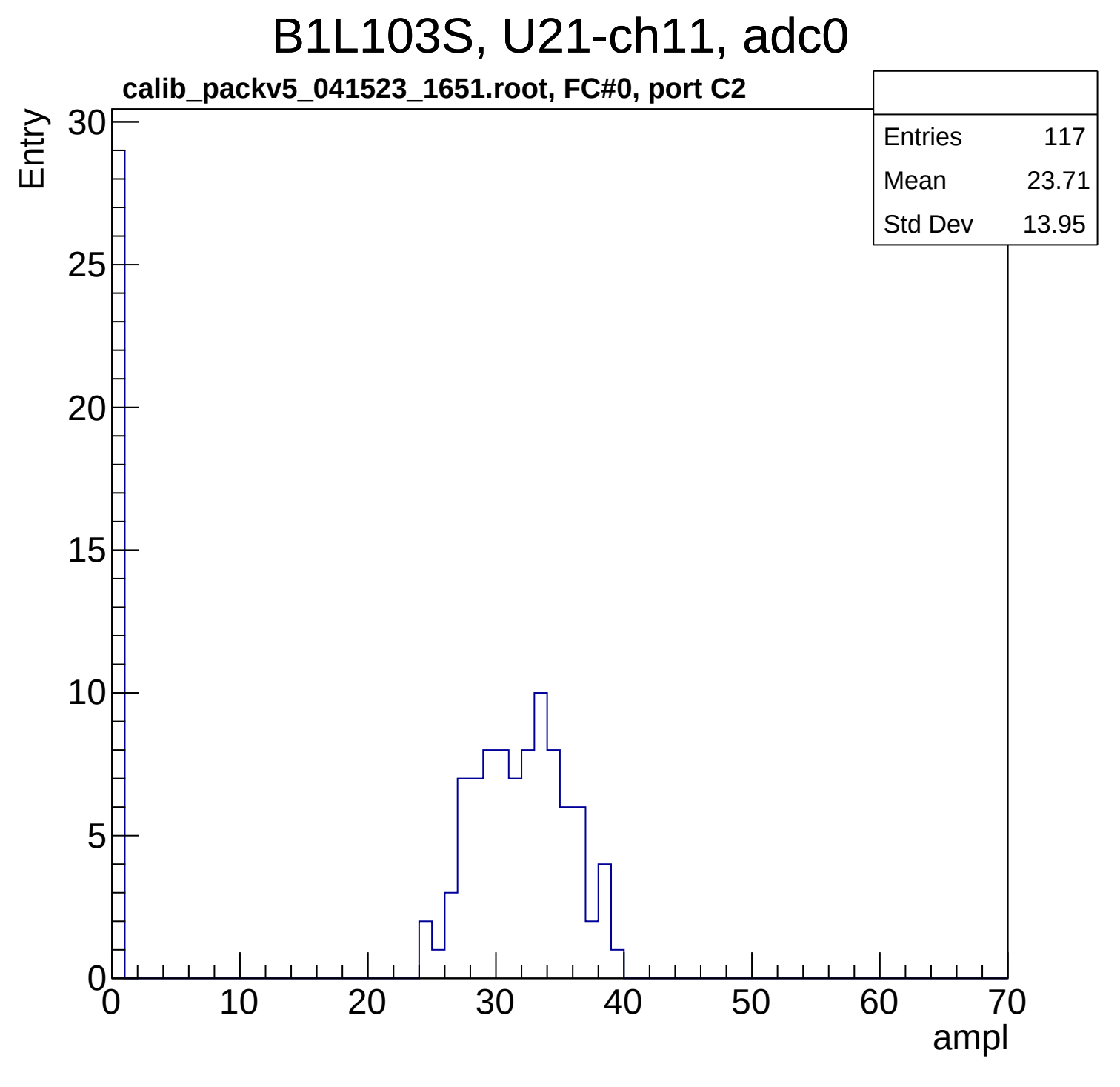
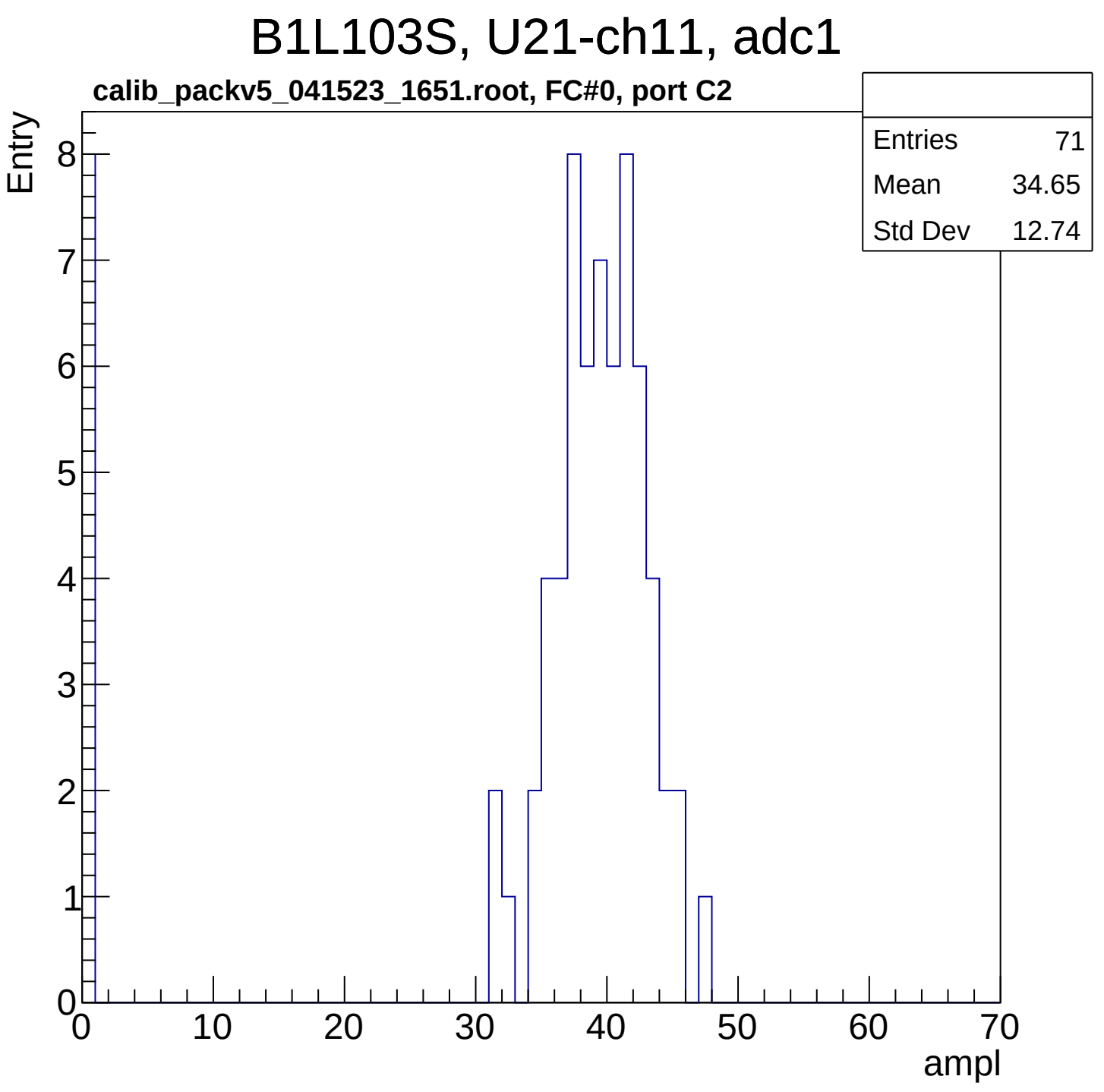
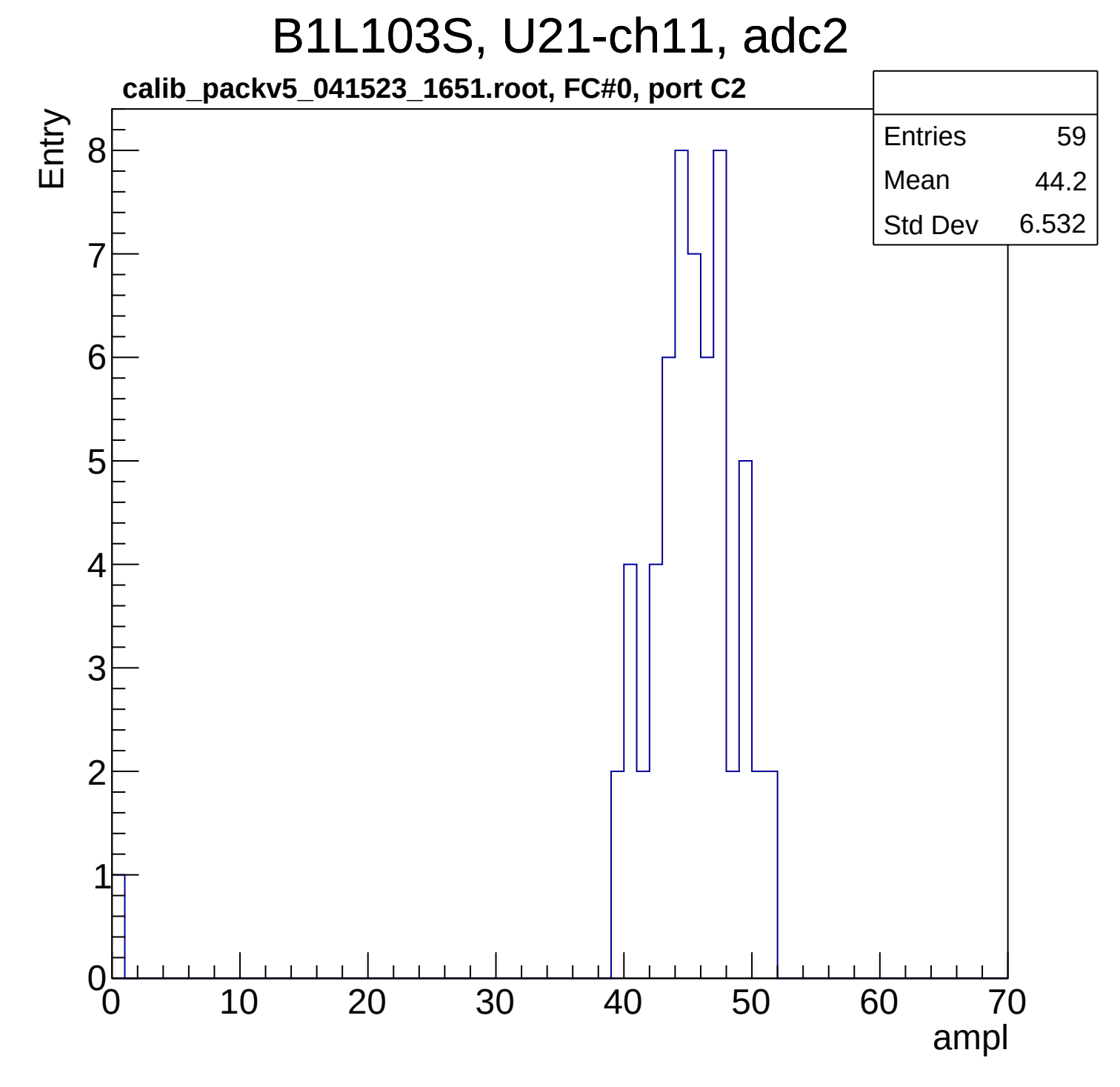
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

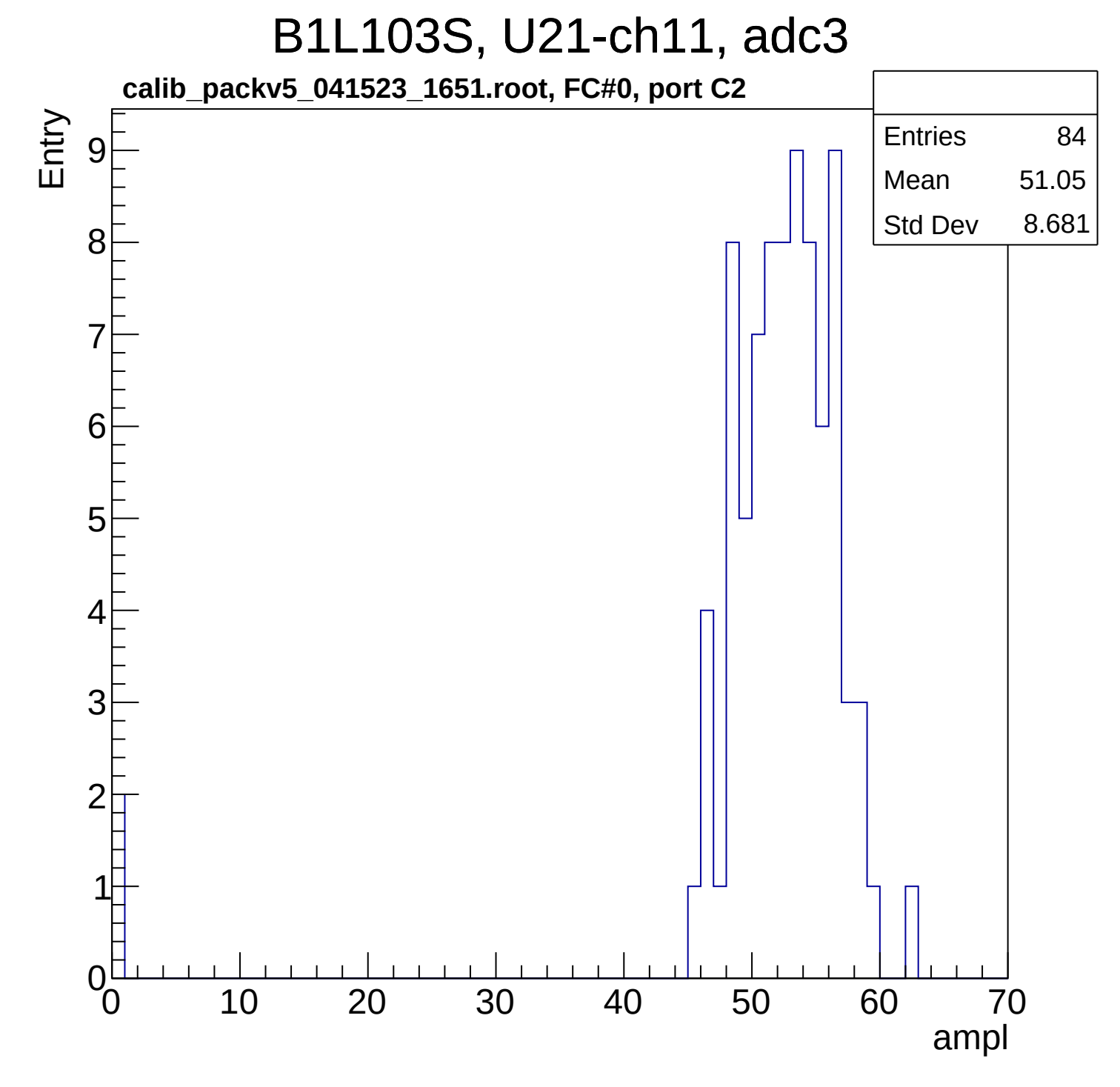

B1L103S, U21-ch10, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 63
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U21-ch10, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch11, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 117
Mean 23.71
Std Dev 13.95
Entry
ampl
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70


B1L103S, U21-ch11, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 34.65
Std Dev 12.74
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch11, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 44.2
Std Dev 6.532
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch11, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 51.05
Std Dev 8.681
Entry
ampl
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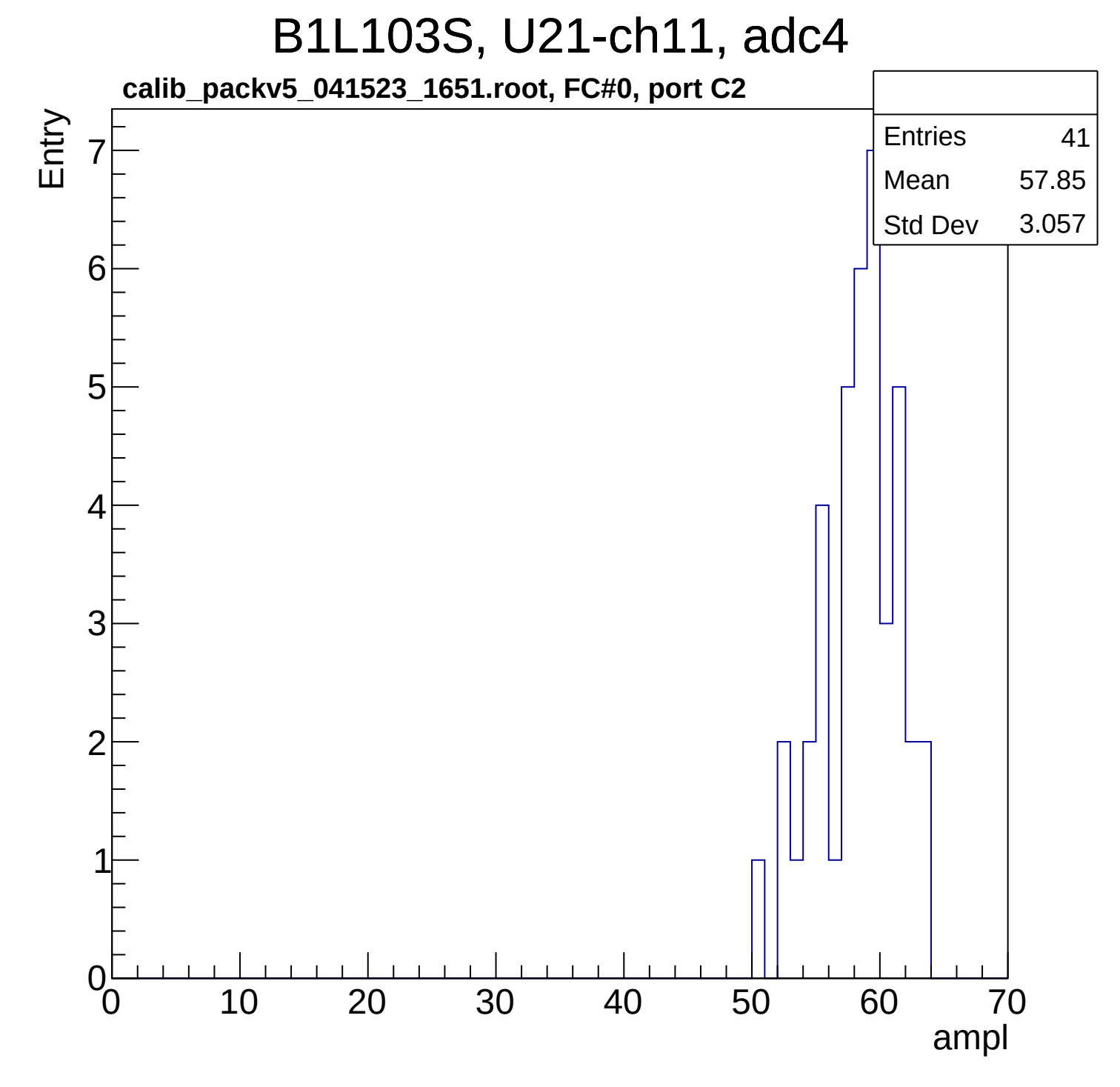
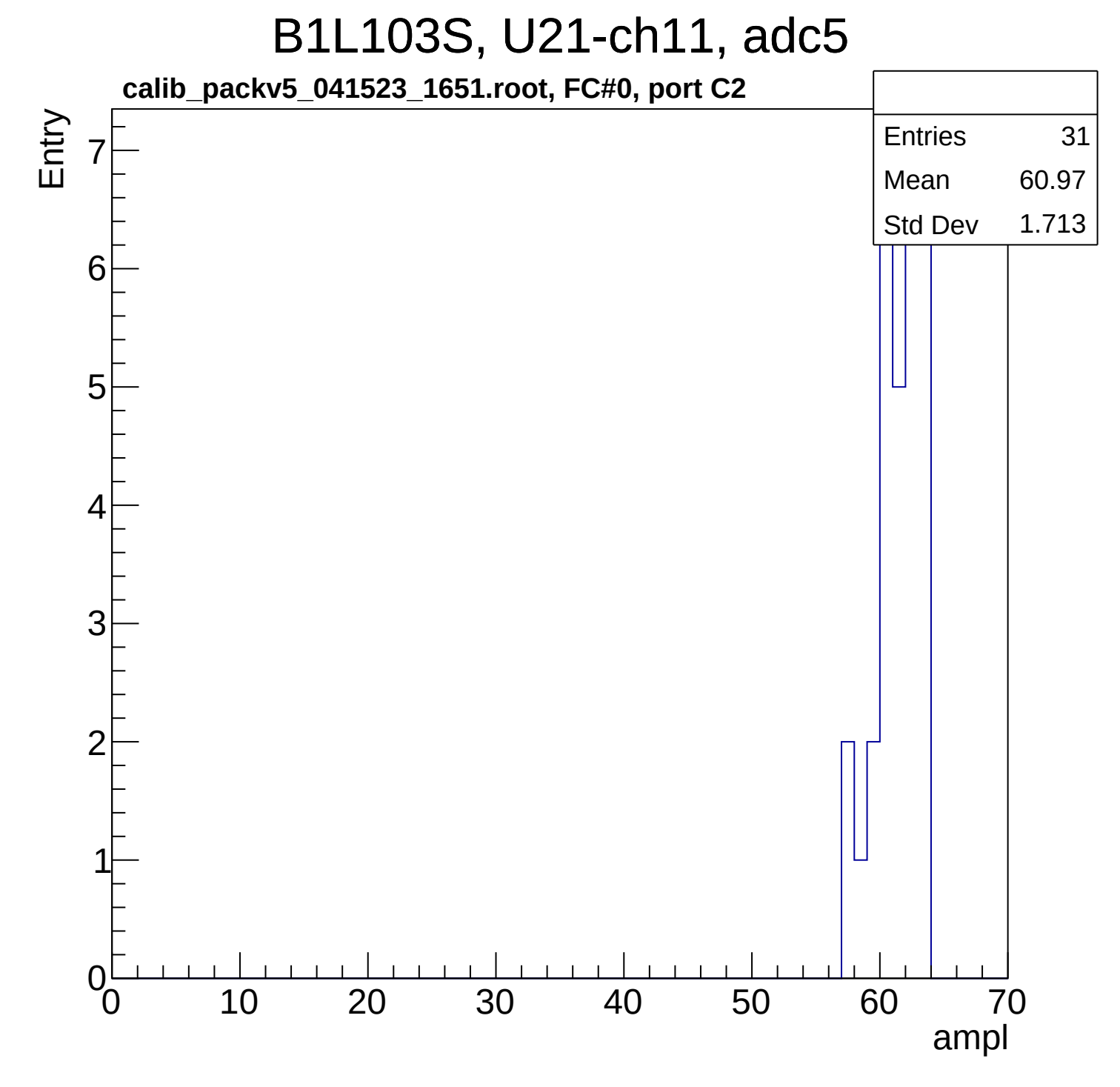
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch11, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 57.85
Std Dev 3.057
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U21-ch11, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 60.97
Std Dev 1.713
Entry
ampl
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2
3
4
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0
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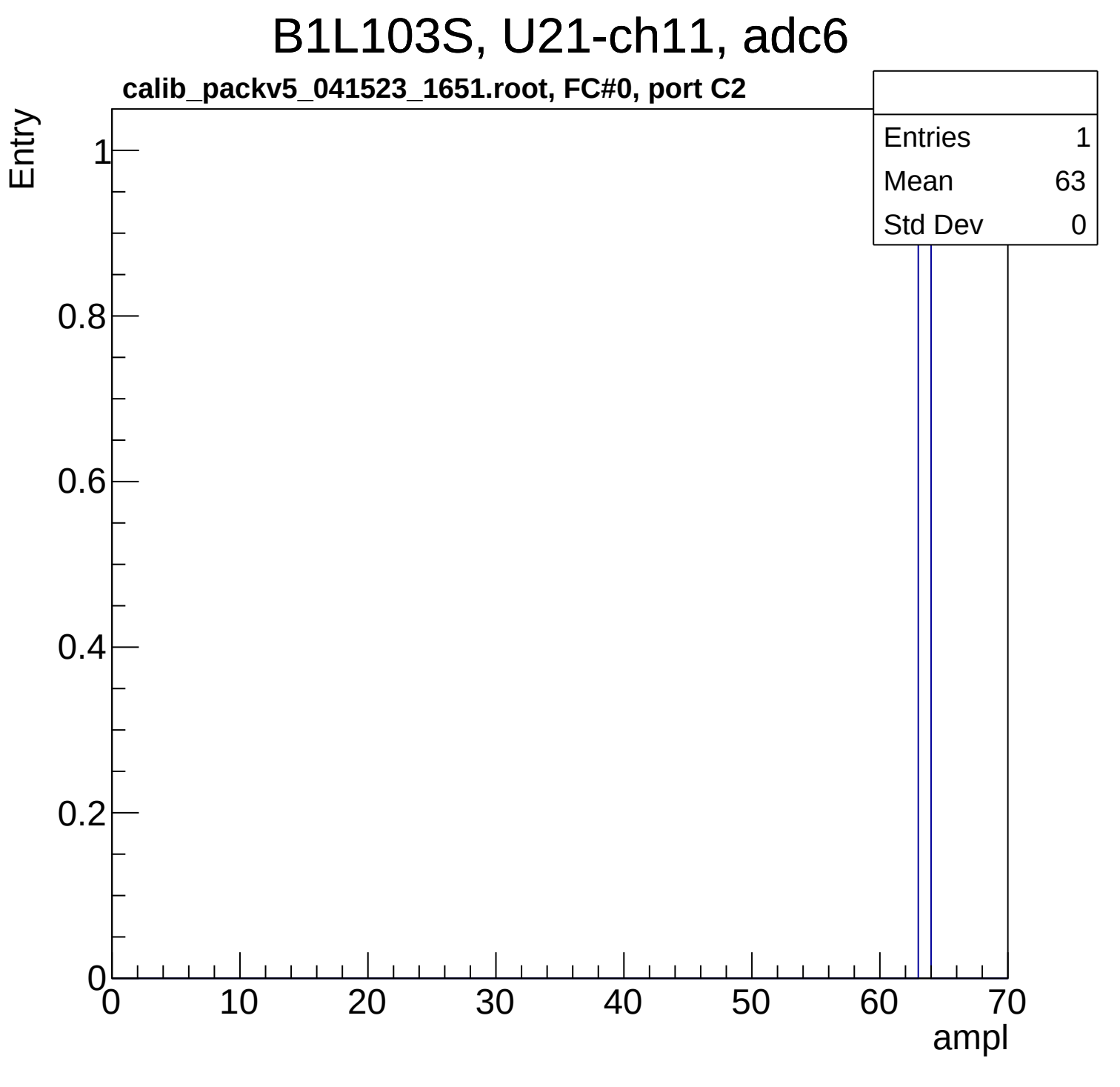
B1L103S, U21-ch11, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 1
Mean 63
Std Dev 0
Entry
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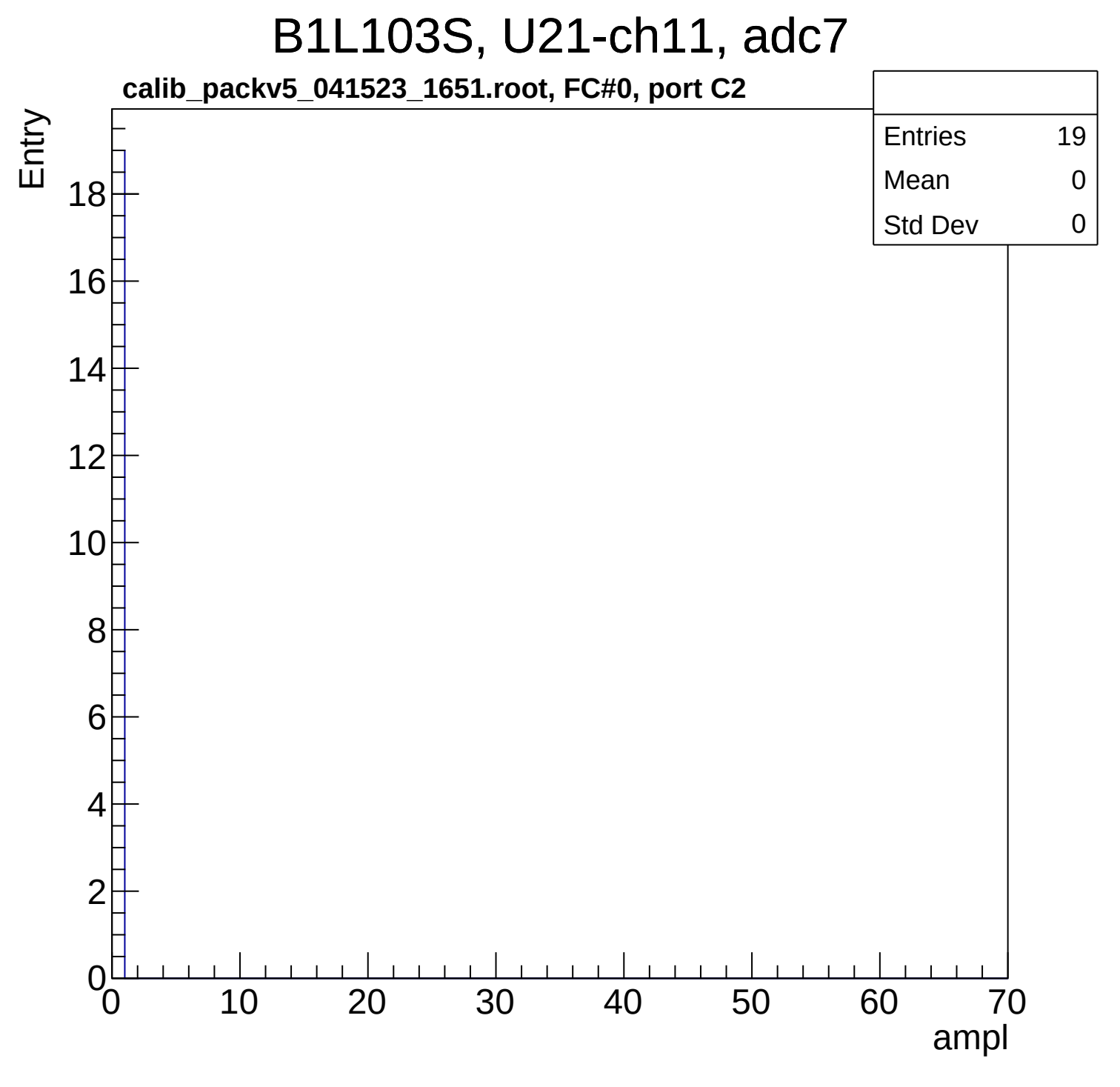
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch11, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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2
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6
8
10
12
14
16
18
0
10
20
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50
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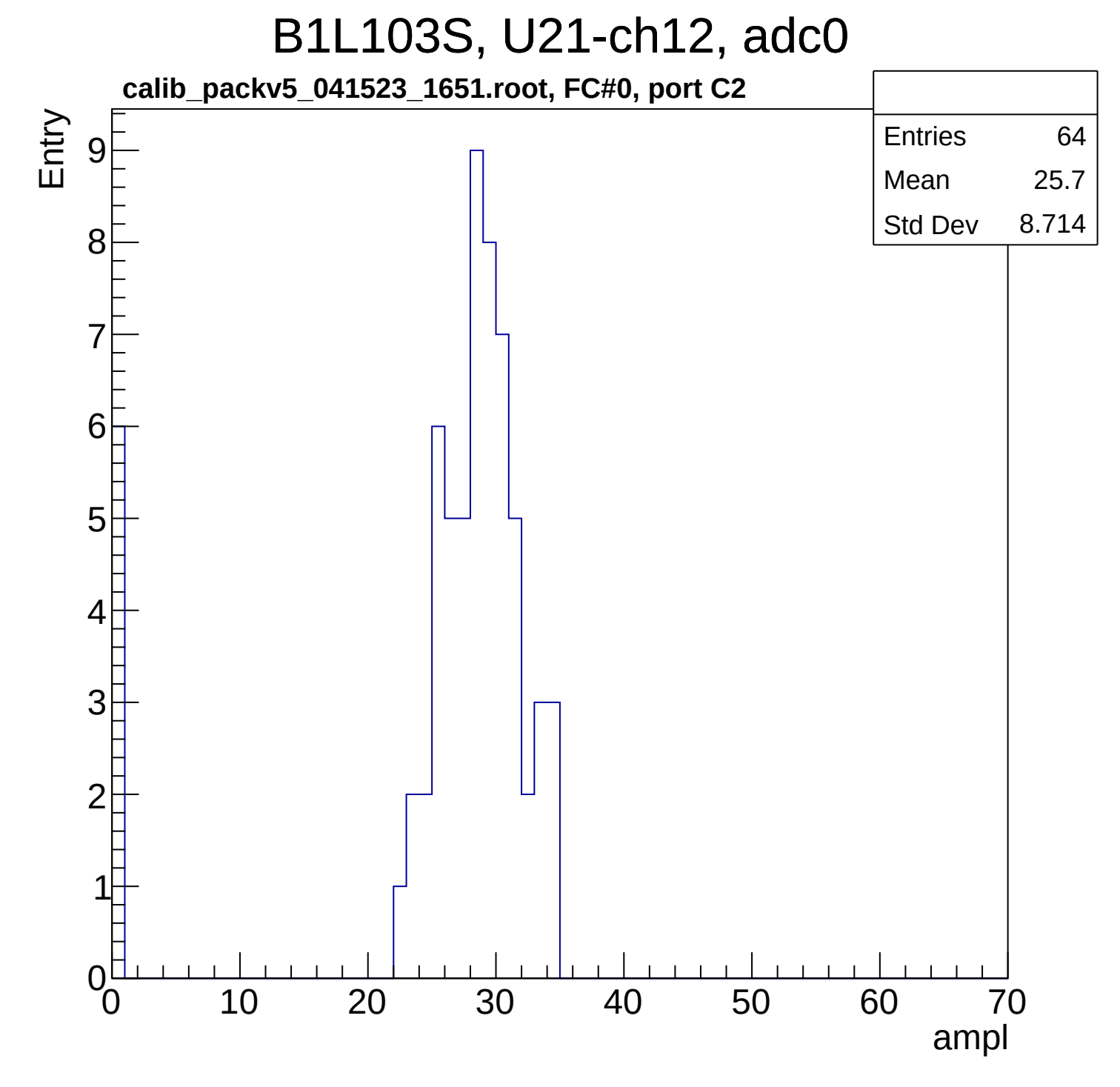
70
ampl


B1L103S, U21-ch12, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 25.7
Std Dev 8.714
Entry
ampl
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2
3
4
5
6
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8
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0
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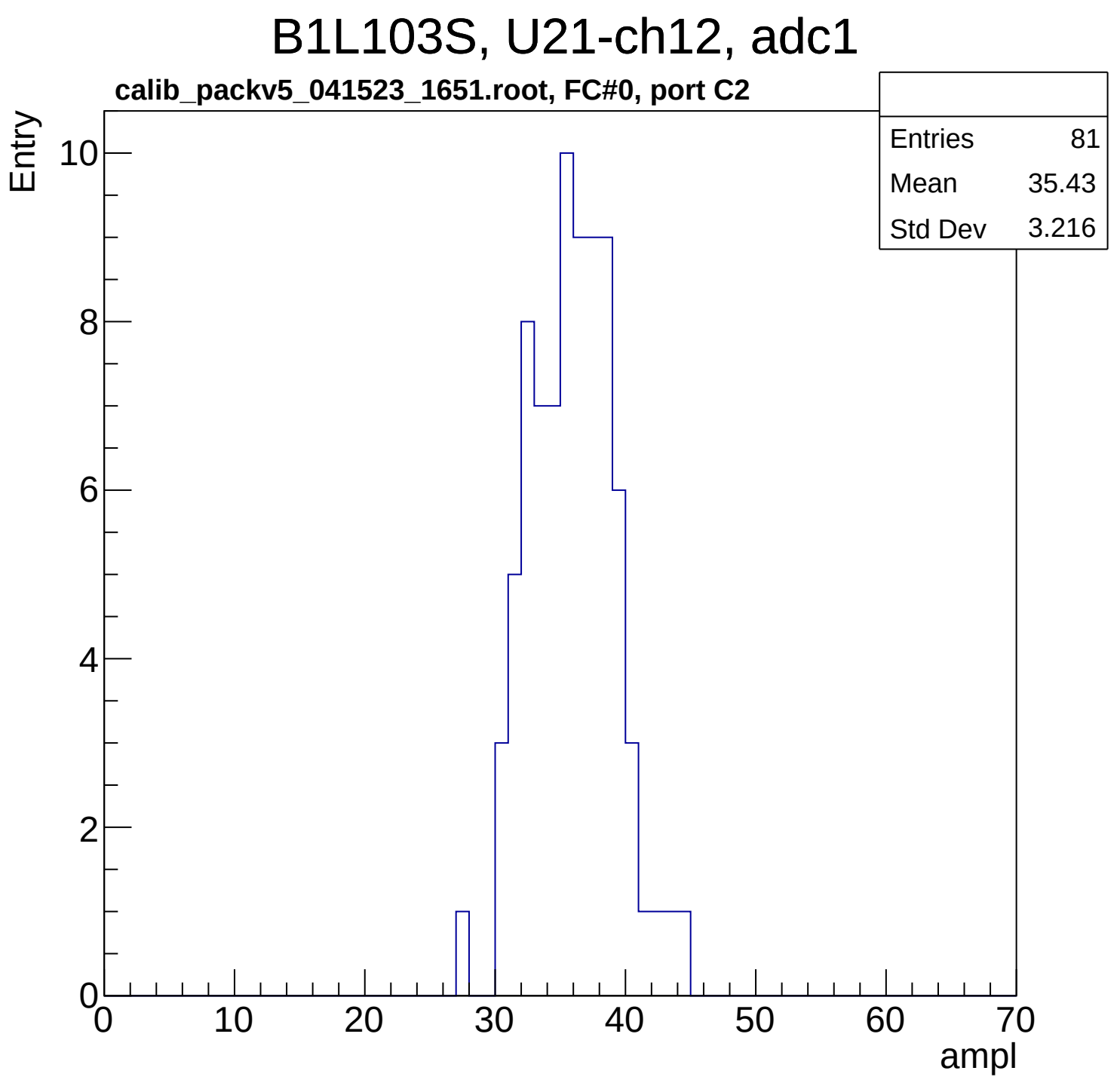
B1L103S, U21-ch12, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 35.43
Std Dev 3.216
Entry
ampl
0
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4
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8
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0
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40
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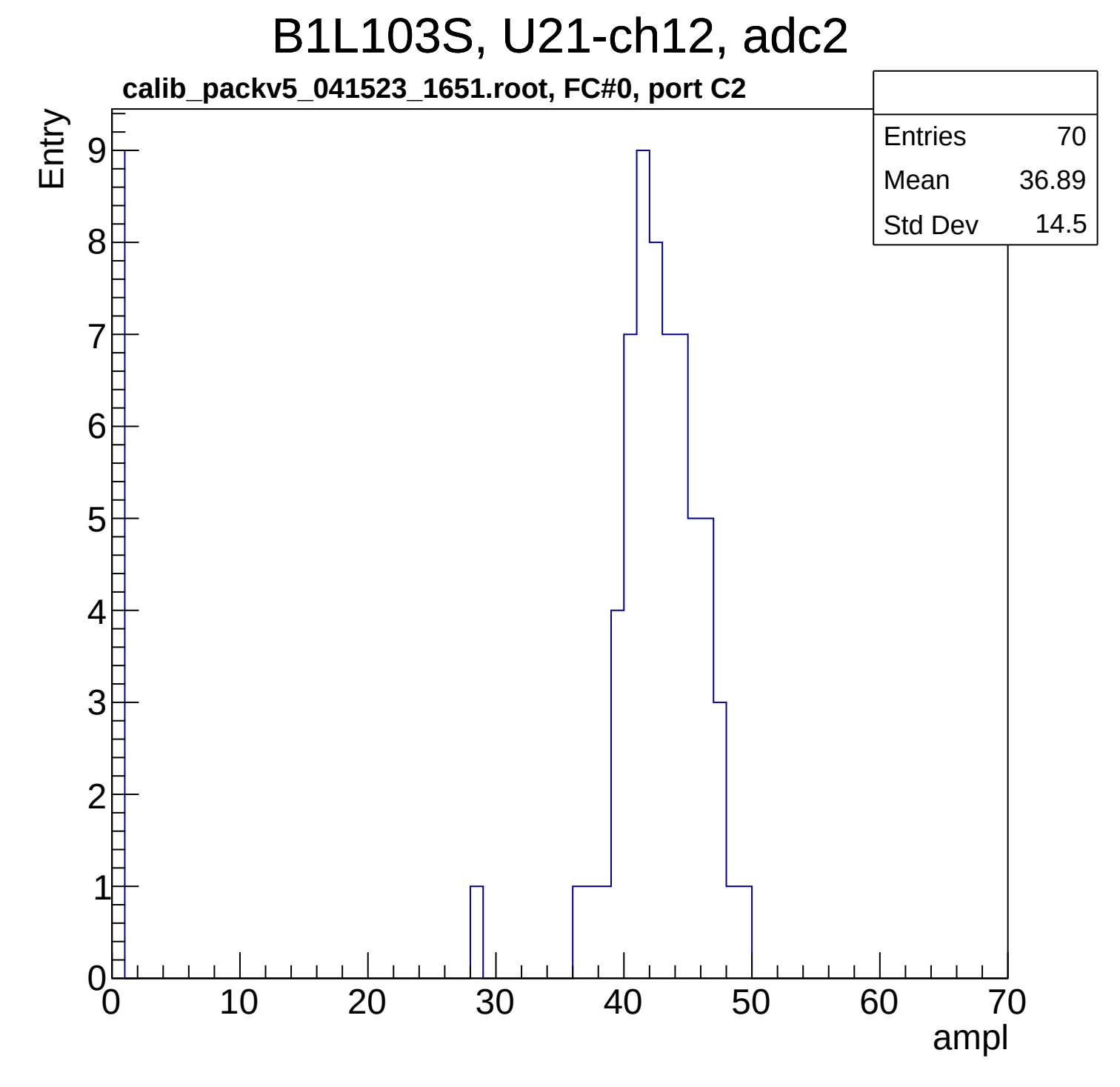
B1L103S, U21-ch12, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 36.89
Std Dev 14.5
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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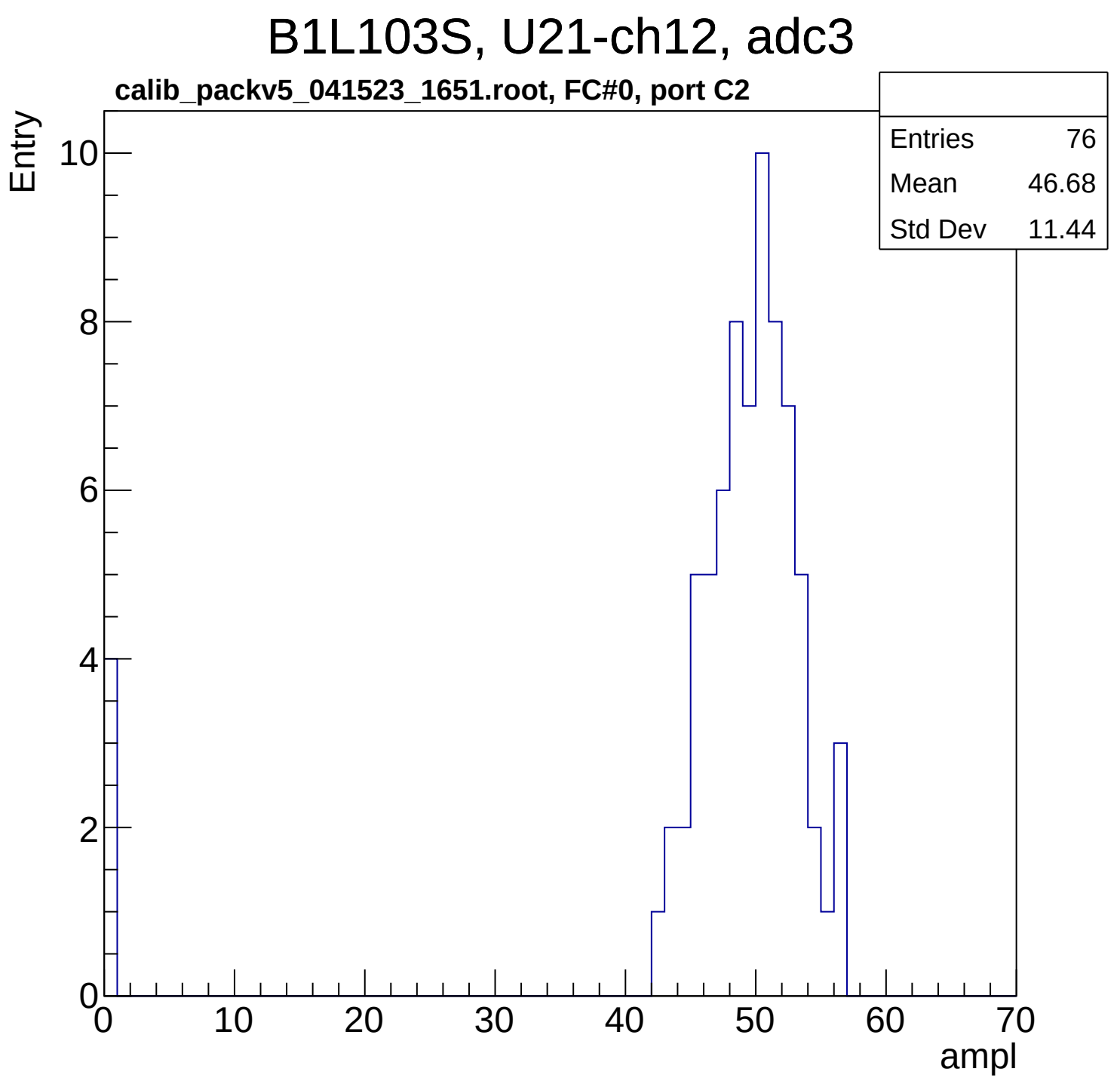
B1L103S, U21-ch12, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 46.68
Std Dev 11.44
Entry
ampl
0
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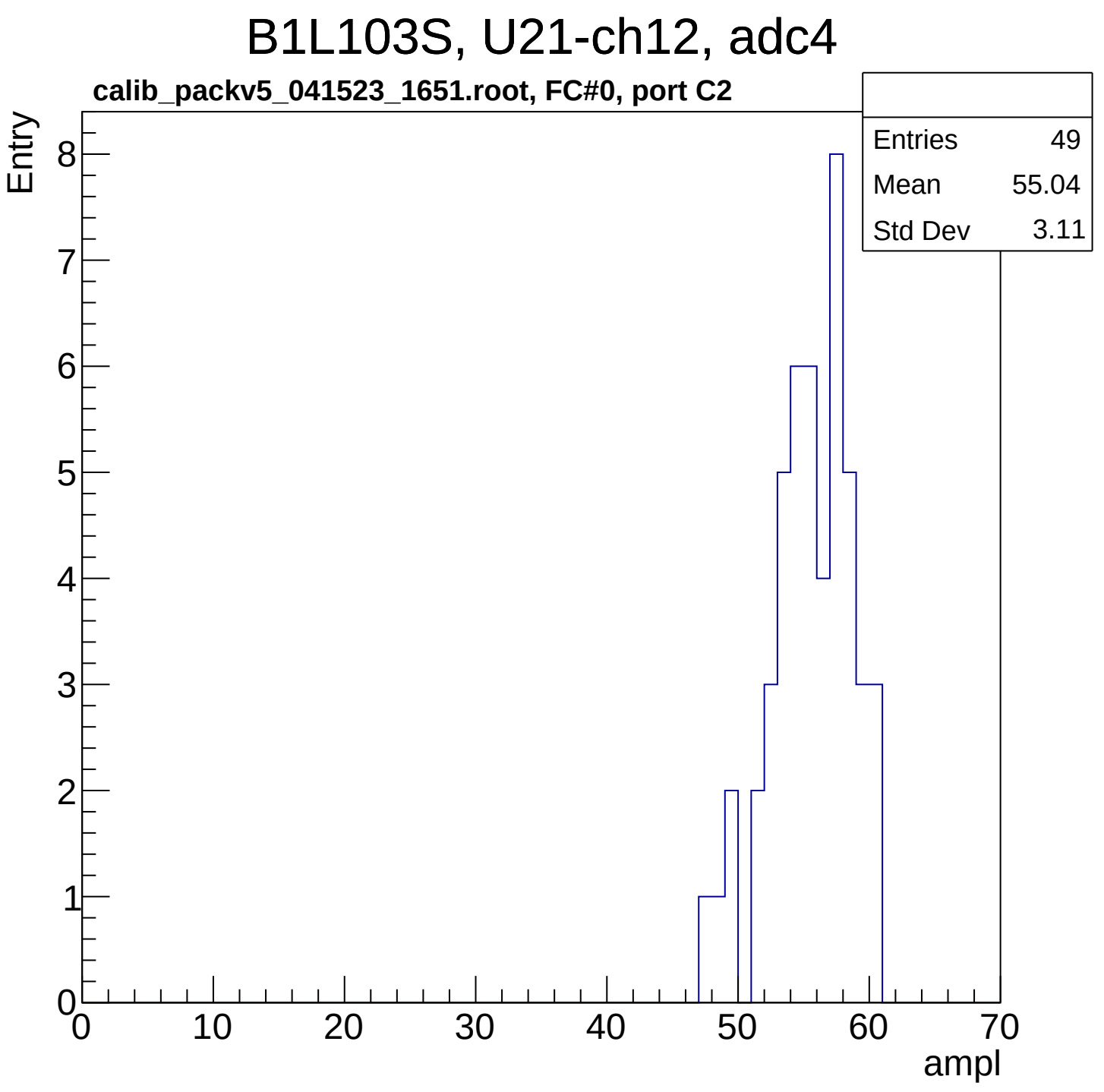
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U21-ch12, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 55.04
Std Dev 3.11
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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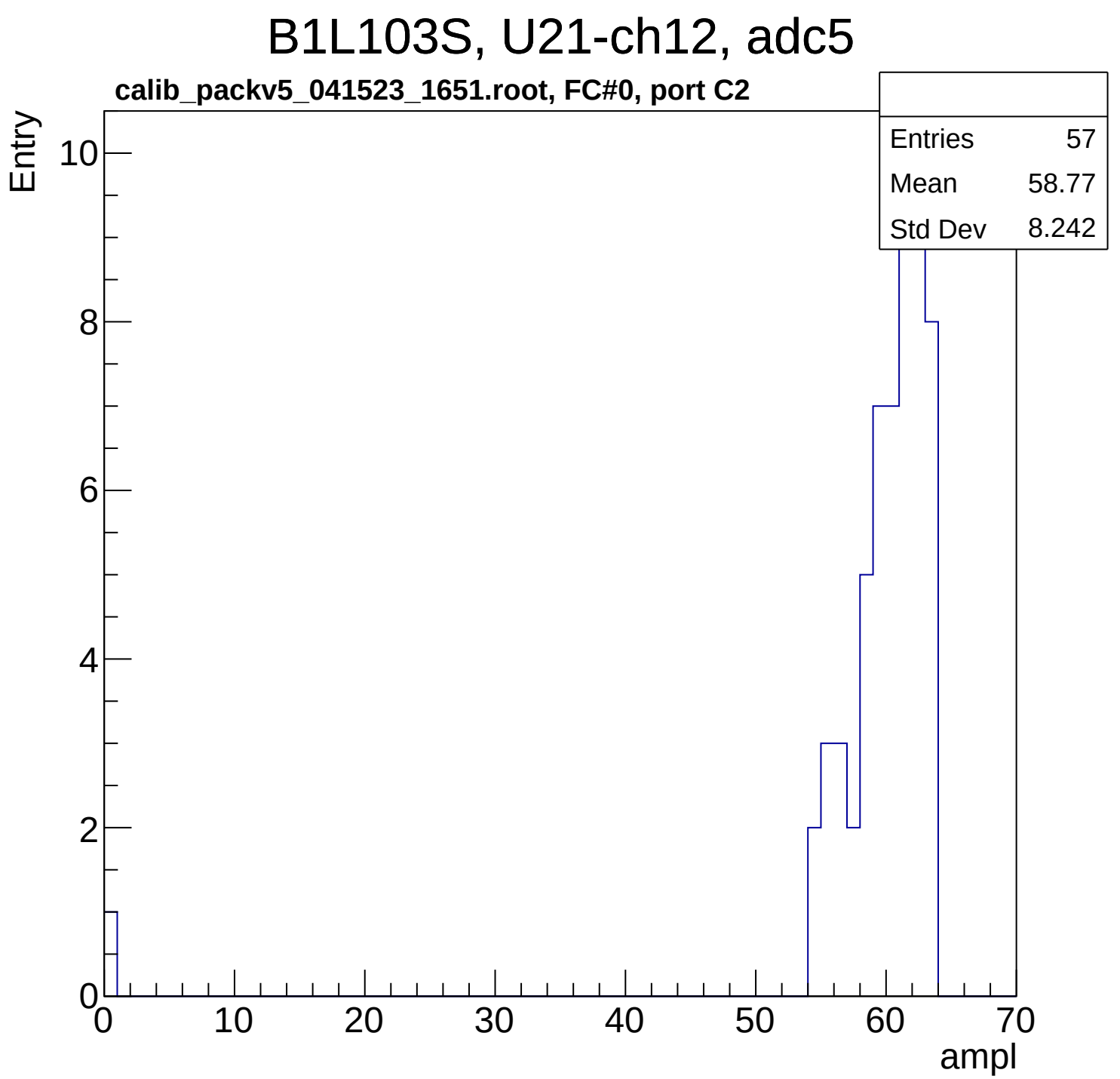
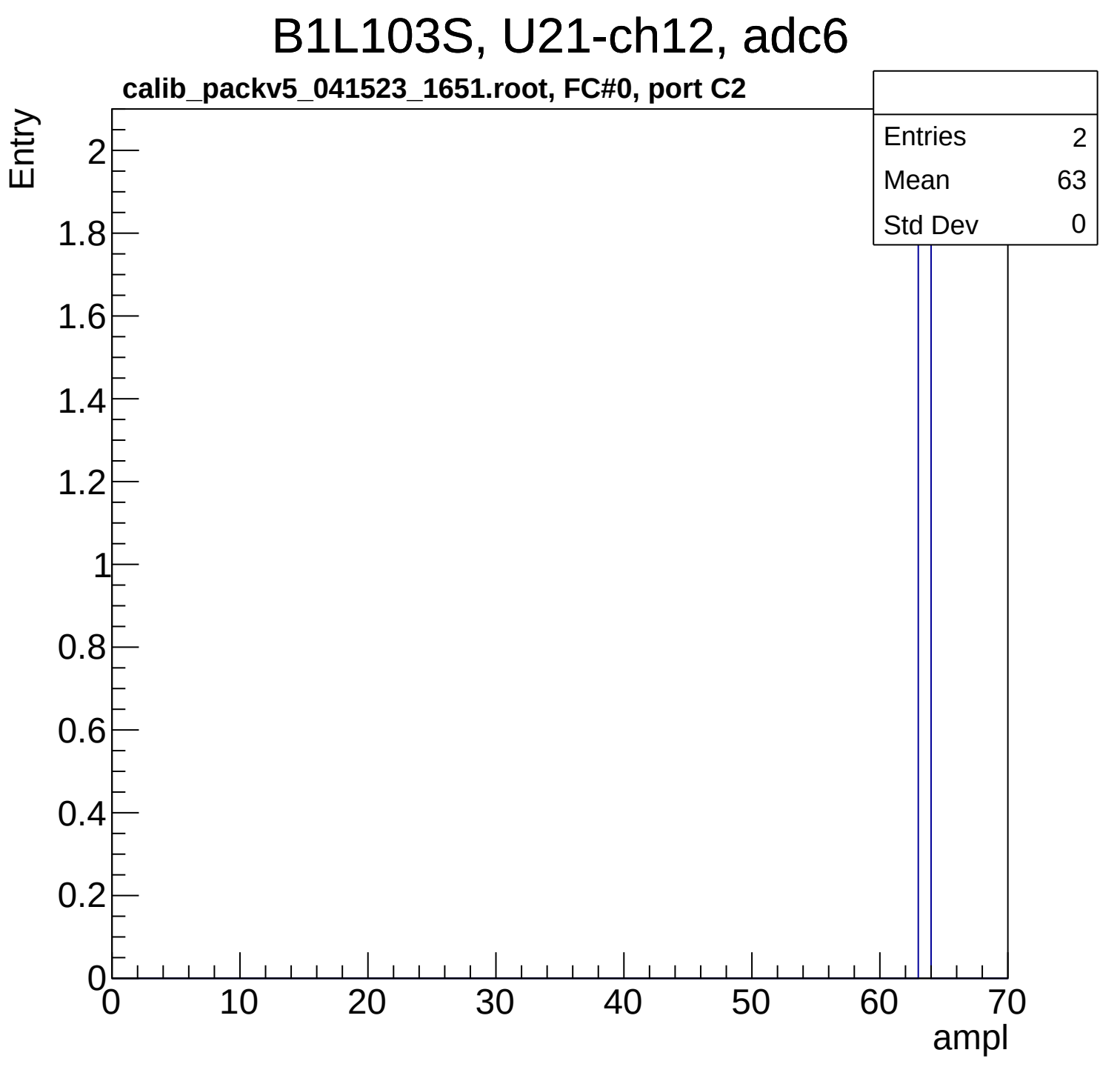
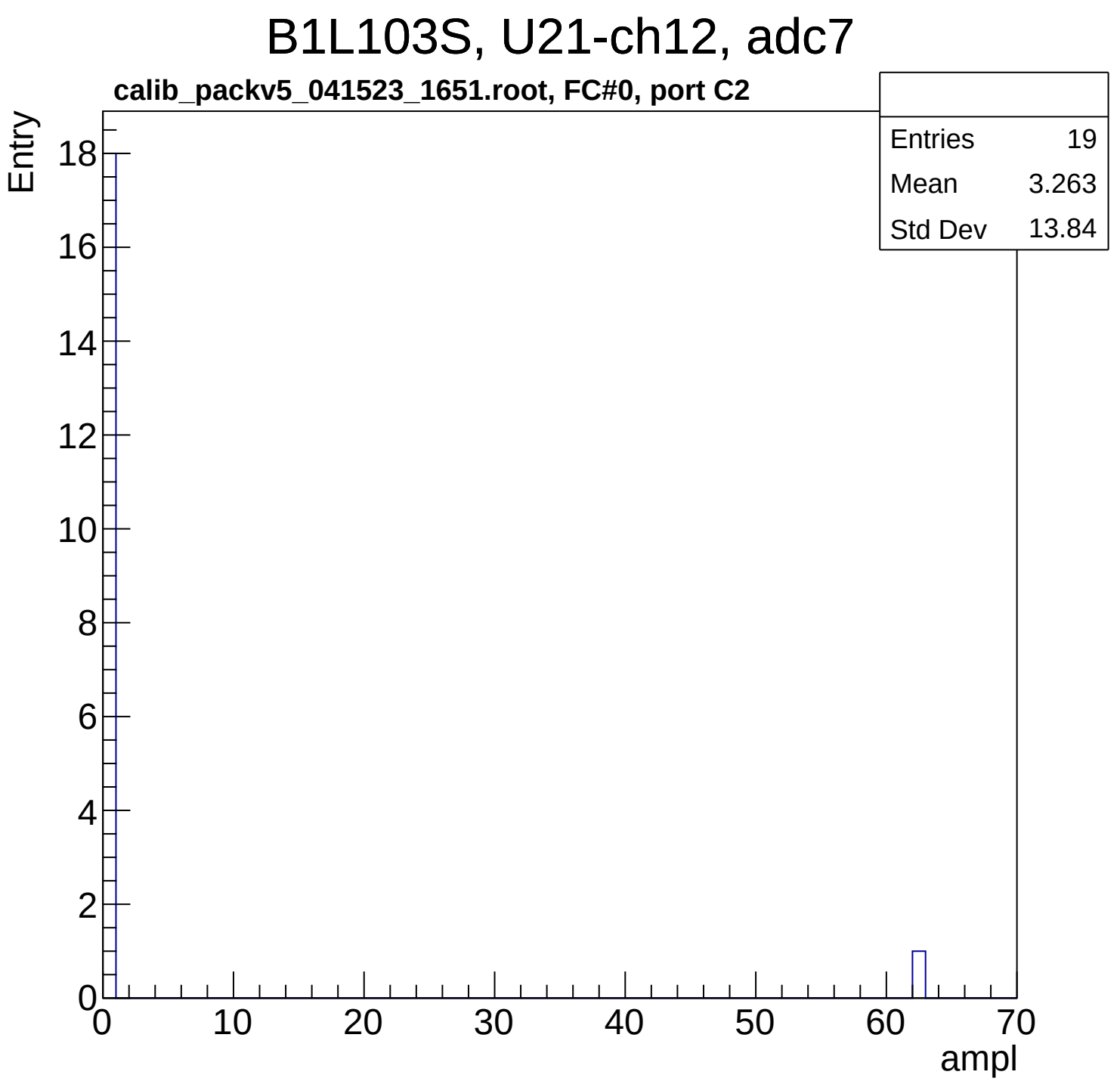
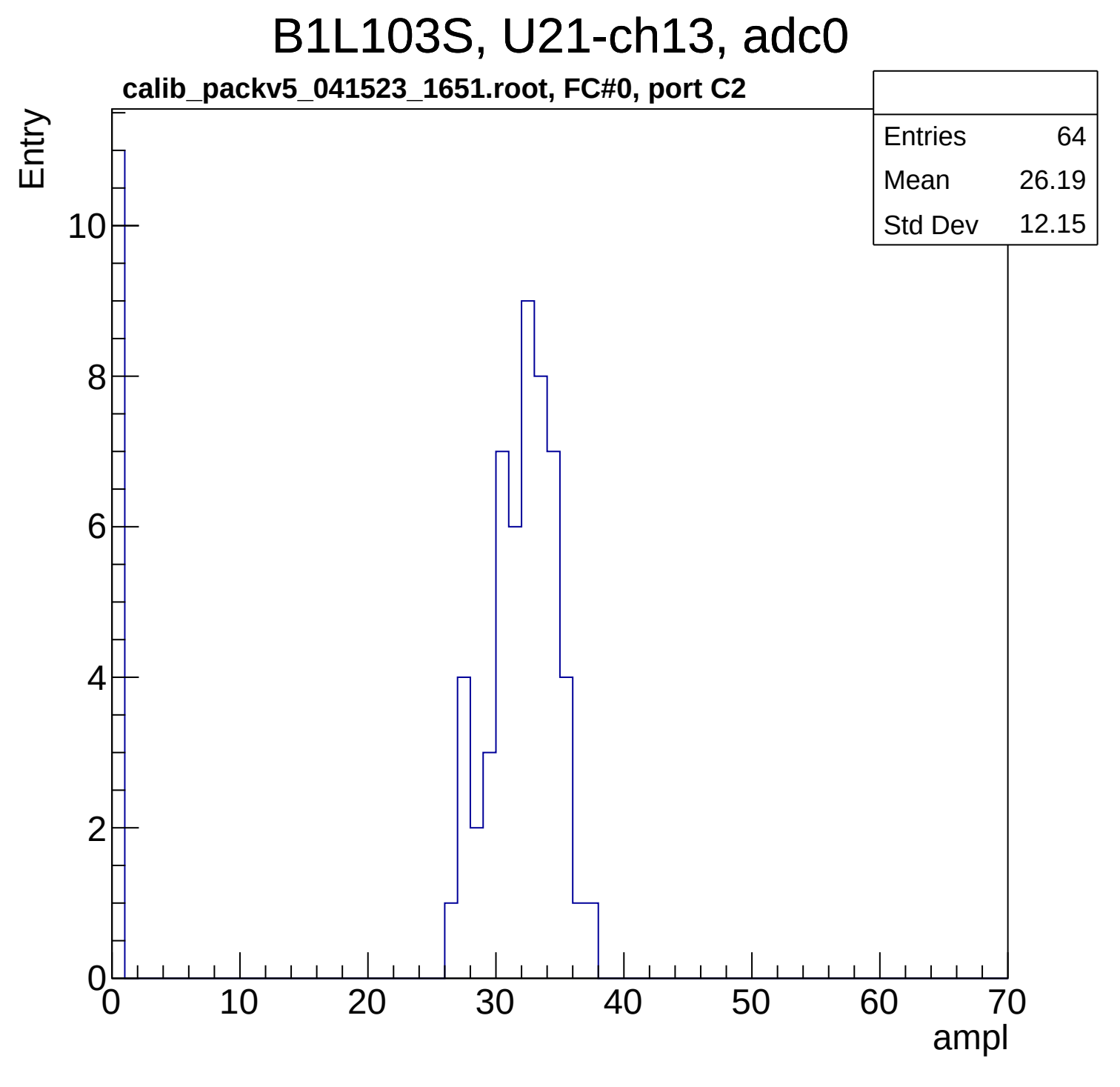
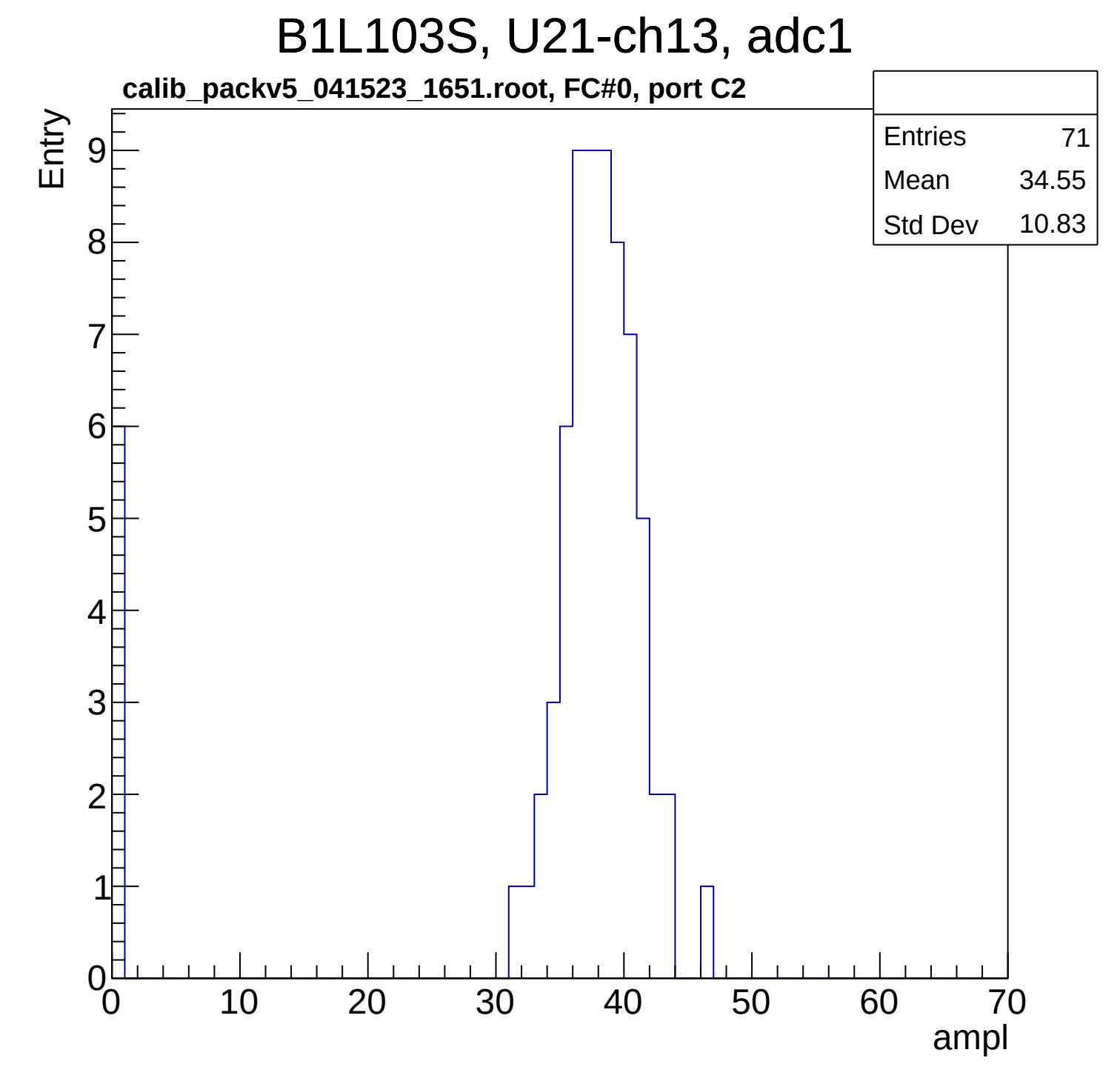
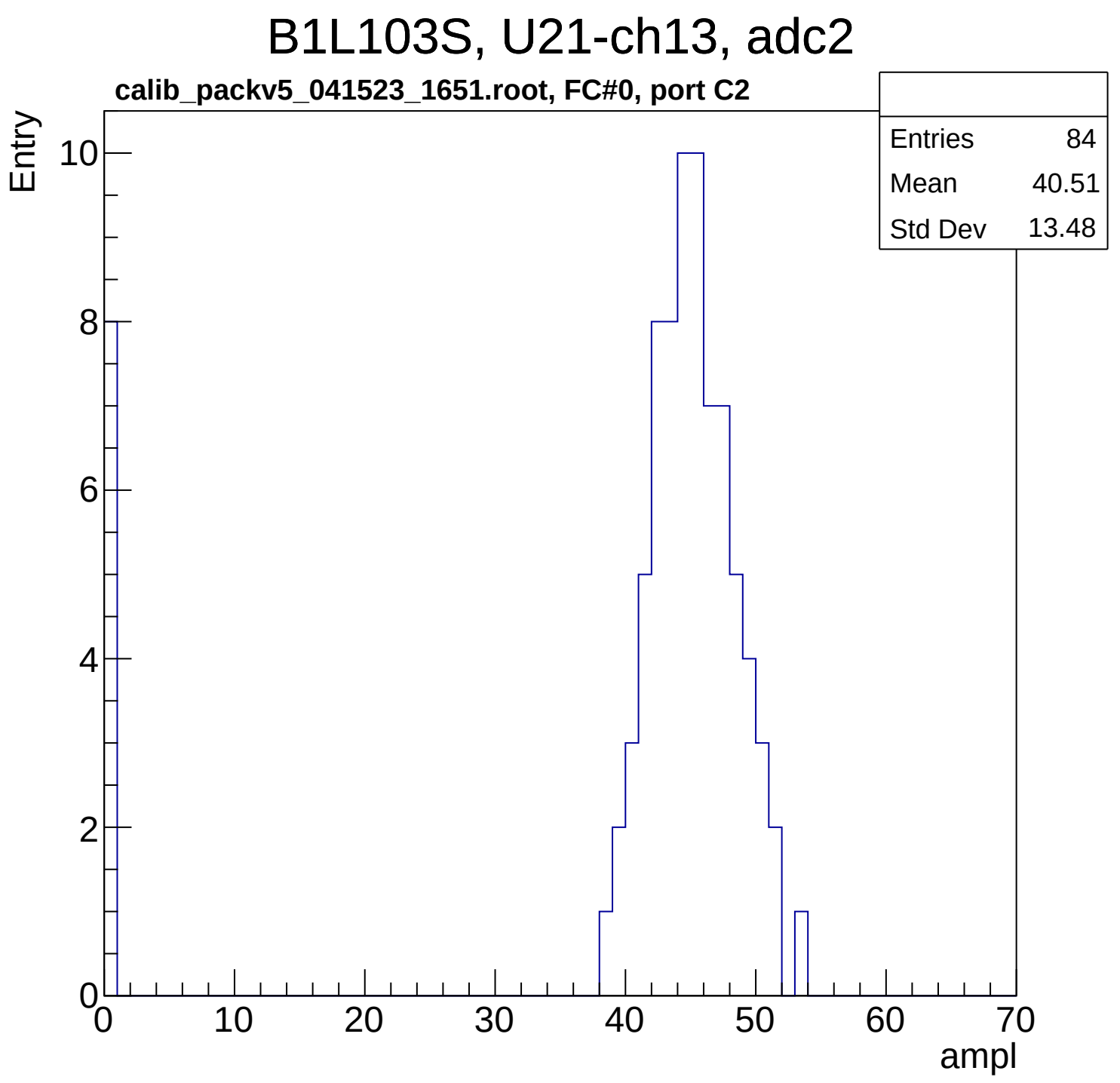

B1L103S, U21-ch12, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 58.77
Std Dev 8.242
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

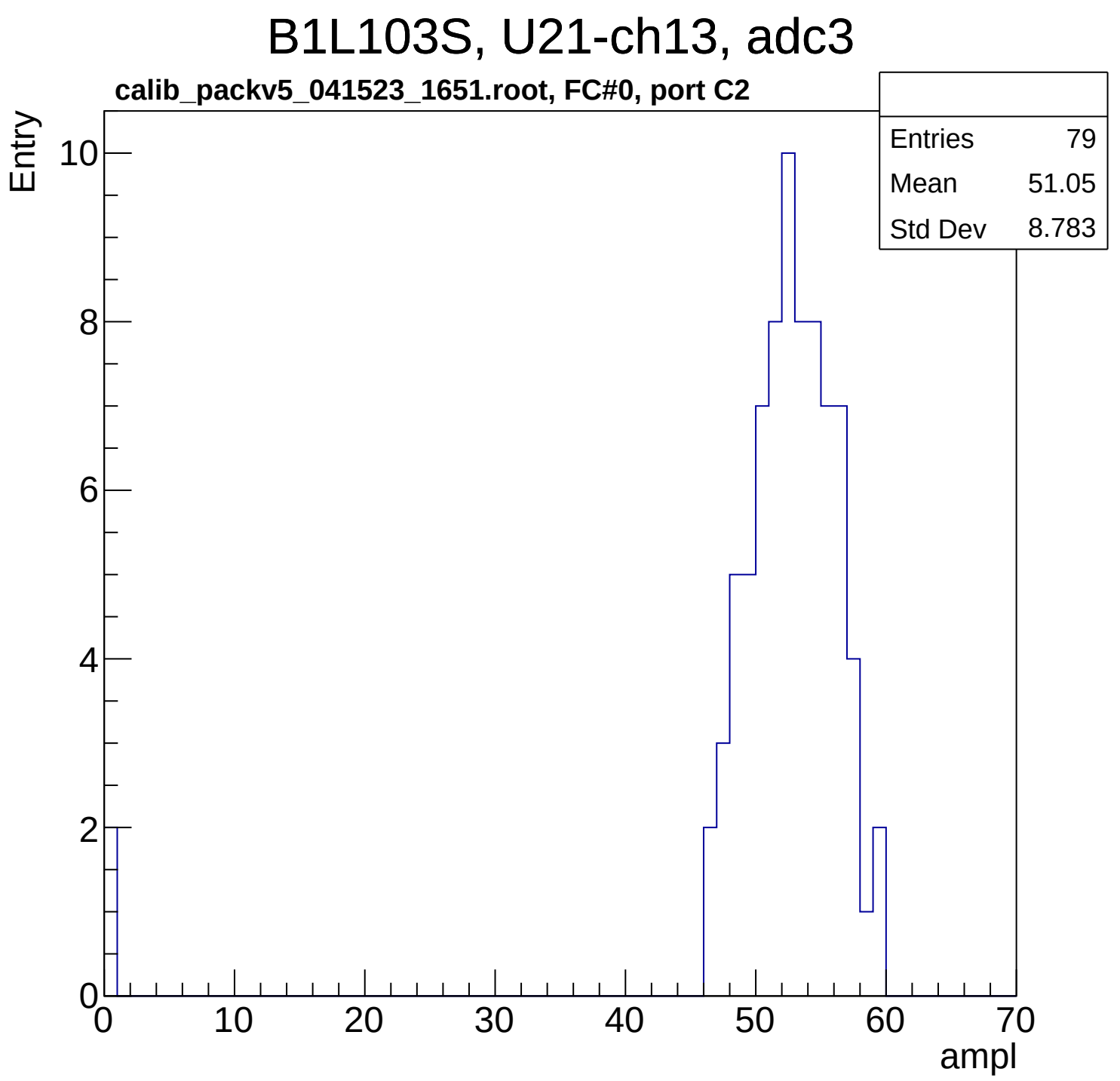

B1L103S, U21-ch12, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 63
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

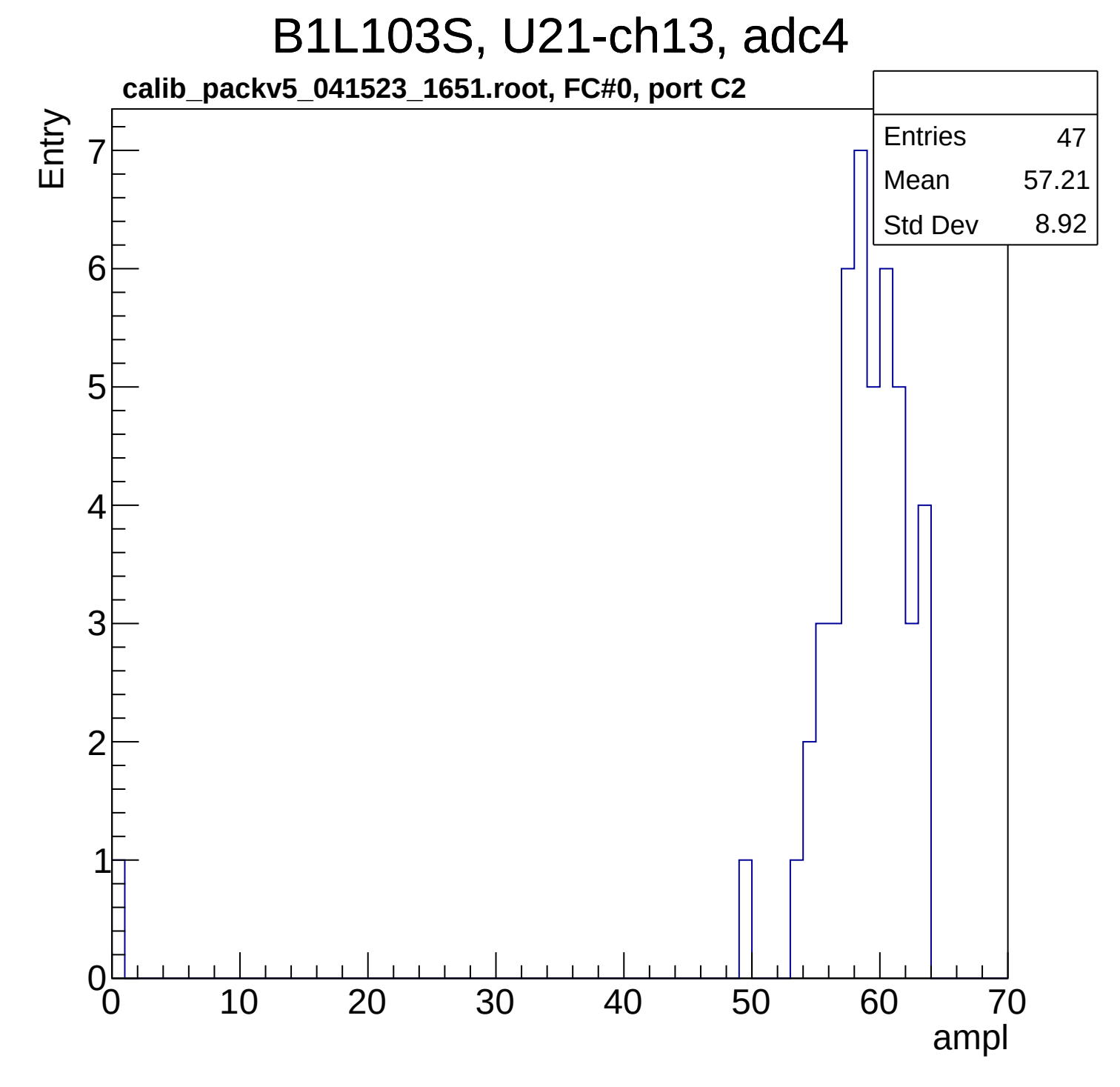

B1L103S, U21-ch12, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.263
Std Dev 13.84
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

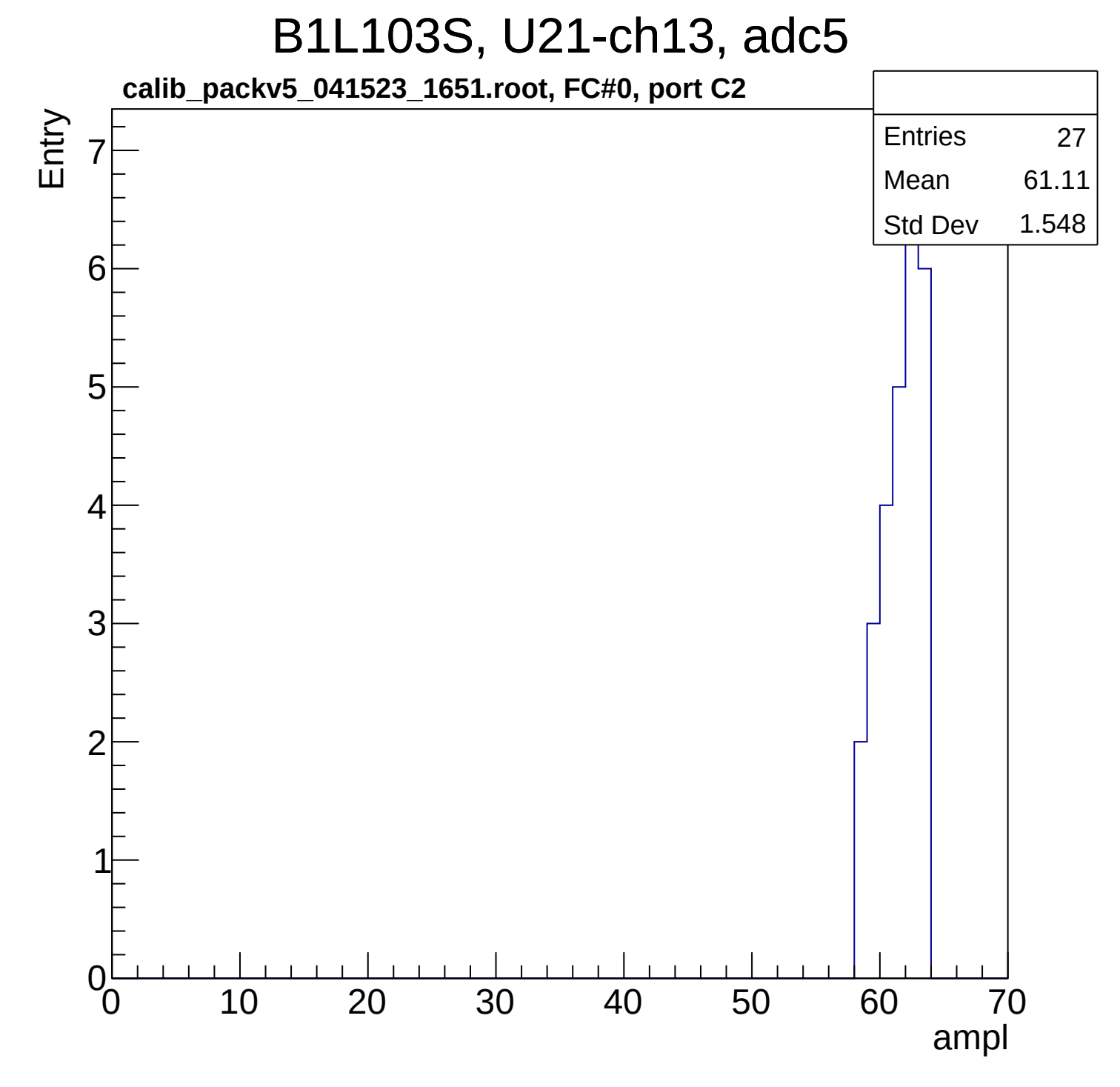

B1L103S, U21-ch13, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 26.19
Std Dev 12.15
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

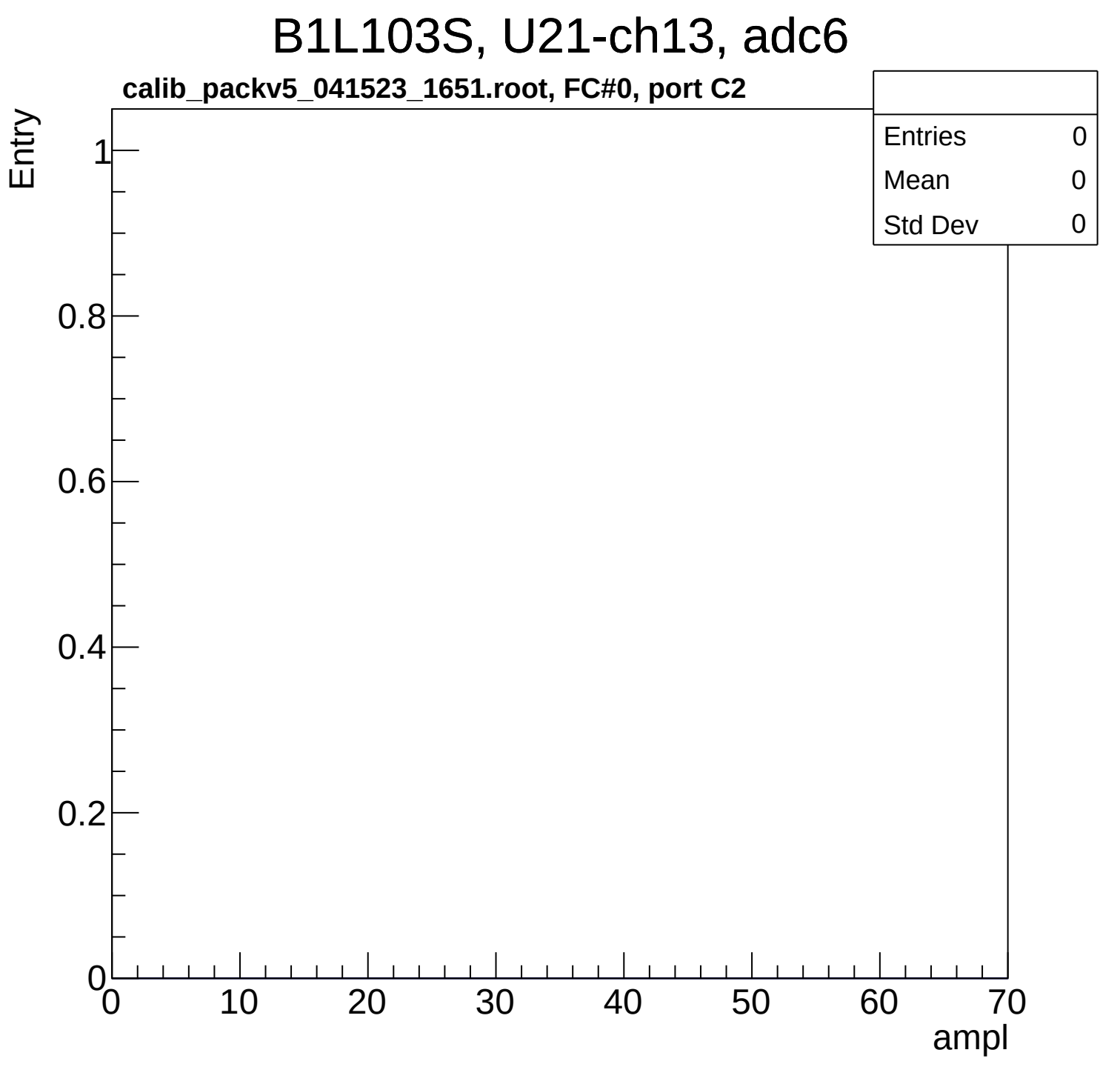

B1L103S, U21-ch13, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 34.55
Std Dev 10.83
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch13, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 40.51
Std Dev 13.48
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch13, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 51.05
Std Dev 8.783
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U21-ch13, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 57.21
Std Dev 8.92
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U21-ch13, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 61.11
Std Dev 1.548
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U21-ch13, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 0
Mean 0
Std Dev 0
Entry
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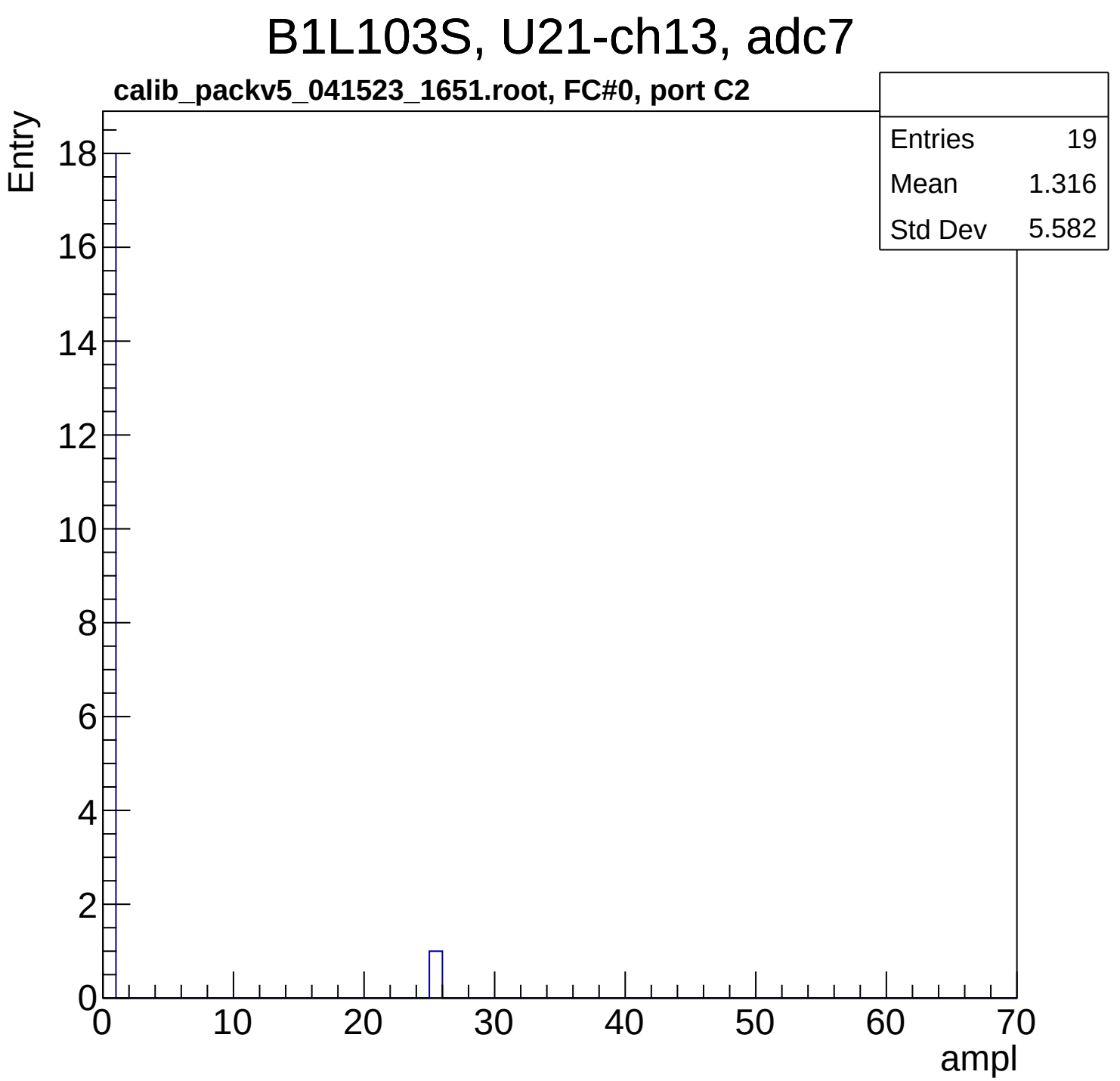
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch13, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.316
Std Dev 5.582
Entry
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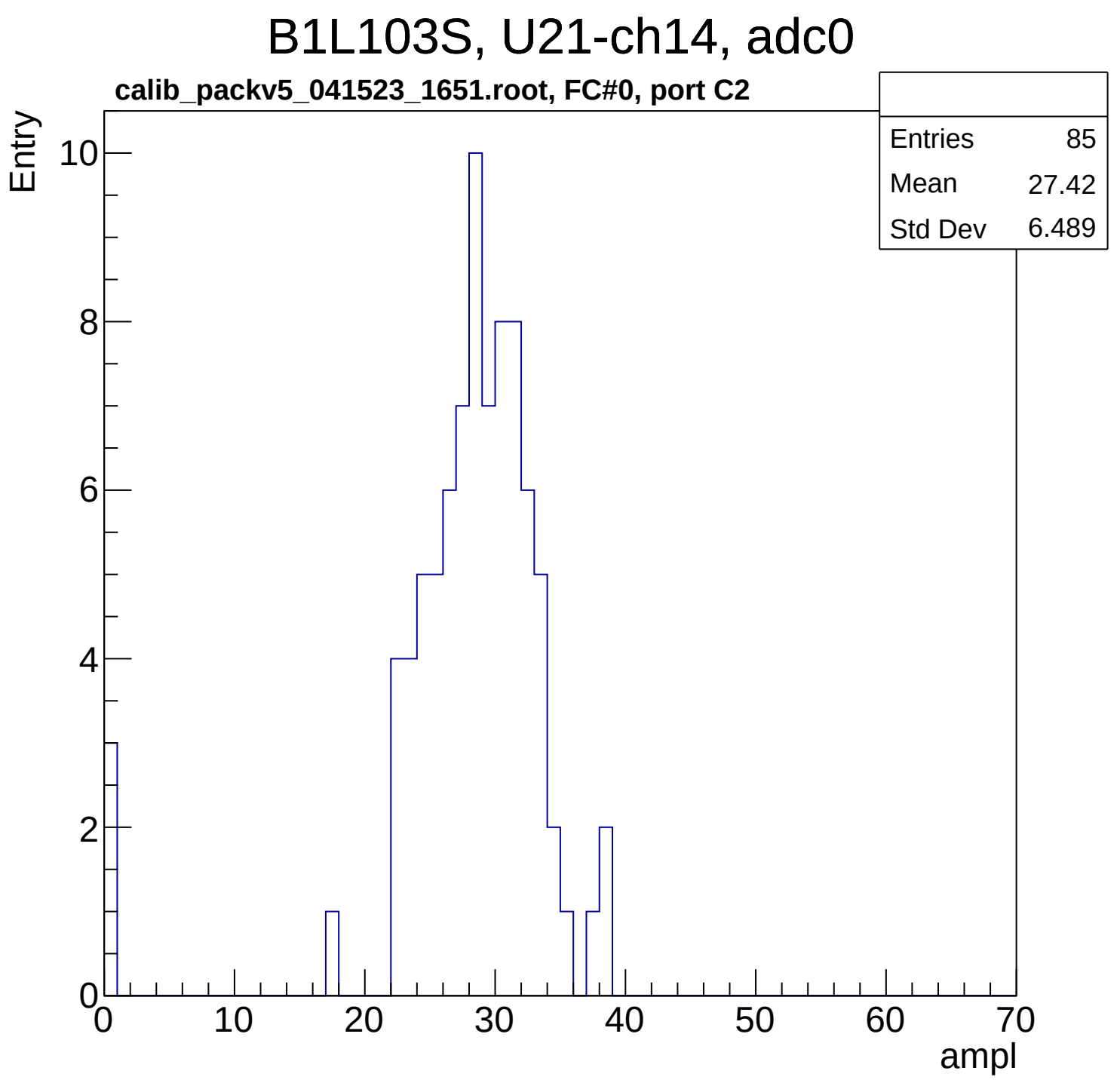
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch14, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 27.42
Std Dev 6.489
Entry
ampl
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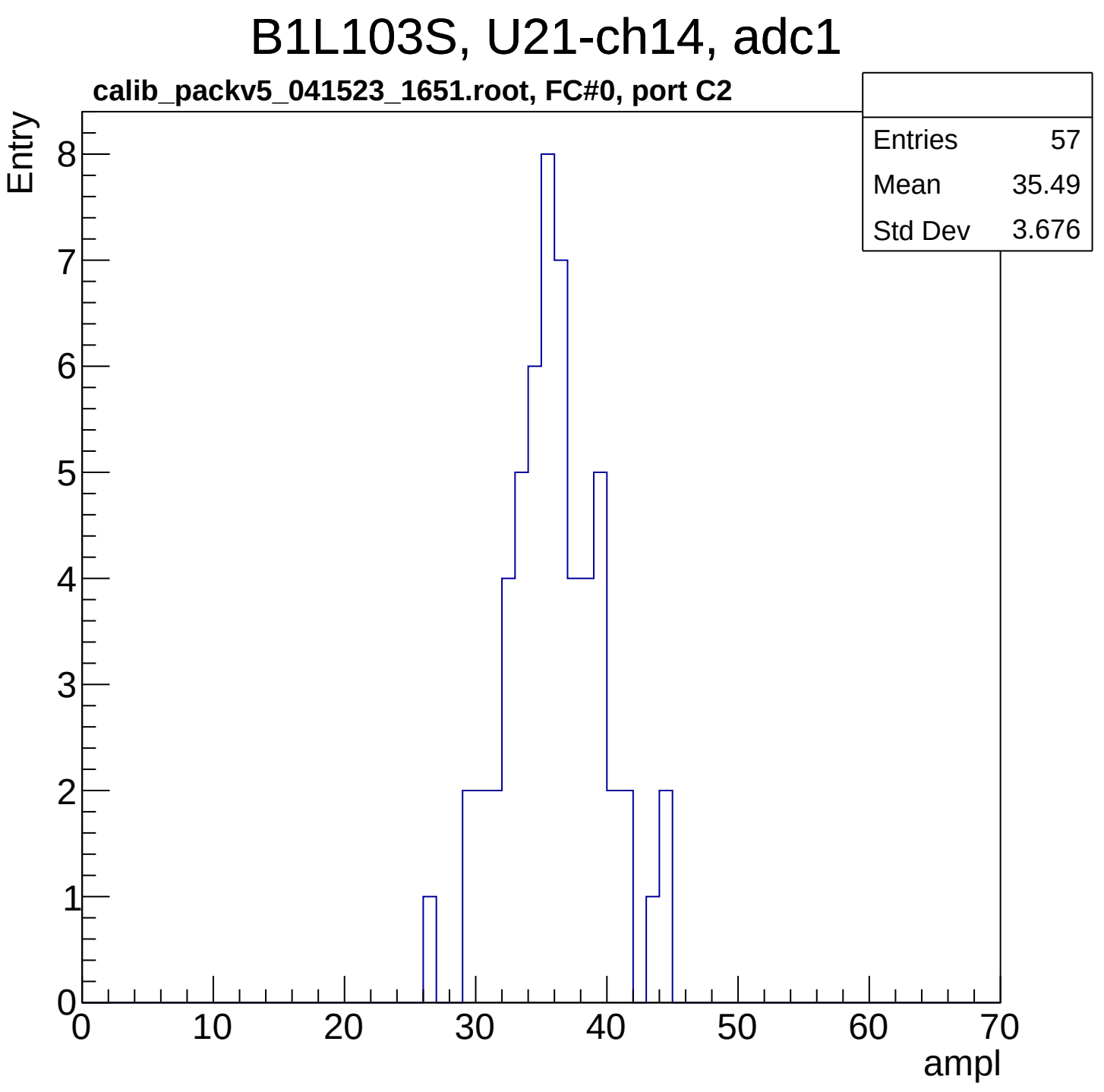
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U21-ch14, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 35.49
Std Dev 3.676
Entry
ampl
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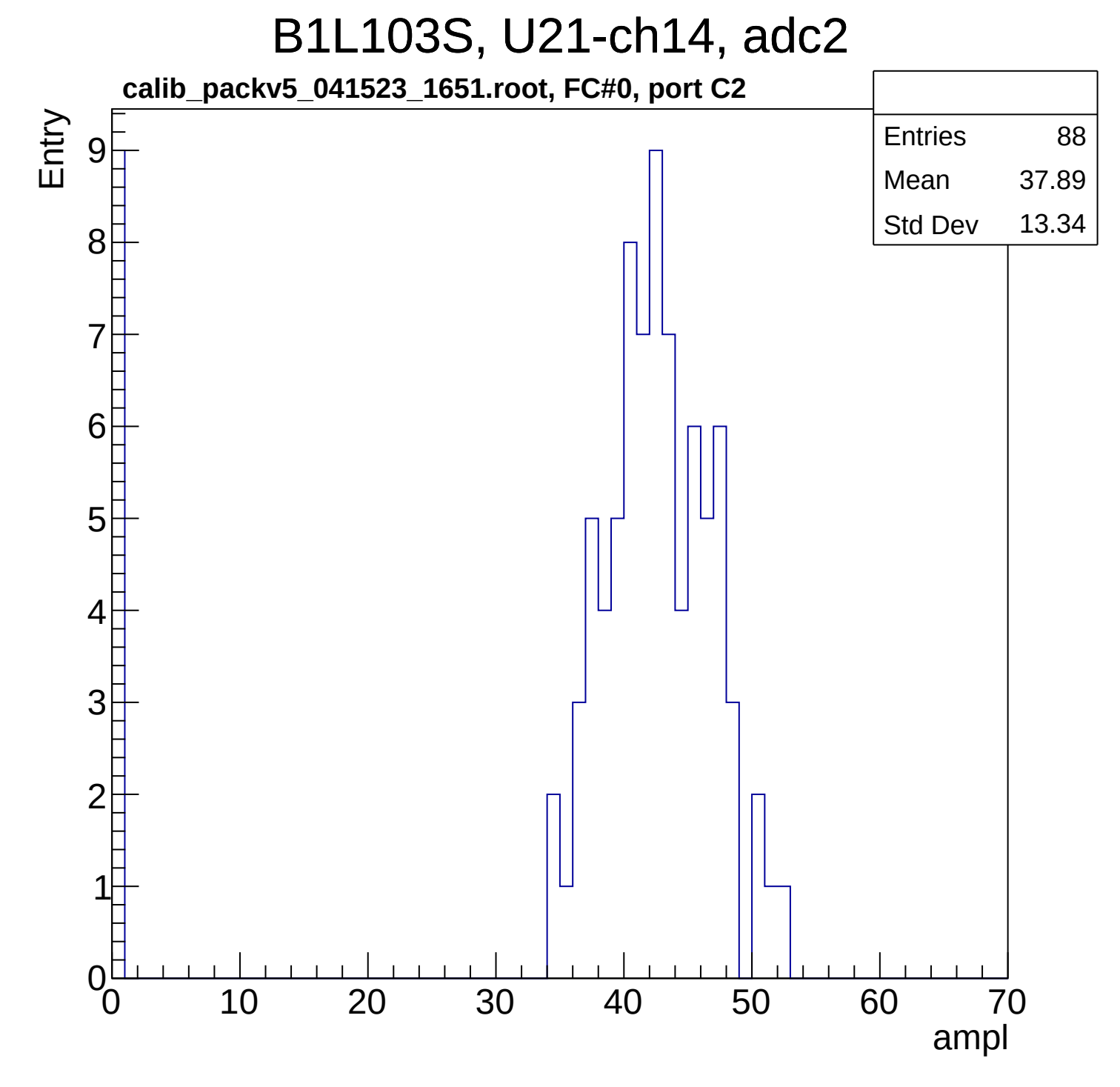
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch14, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 37.89
Std Dev 13.34
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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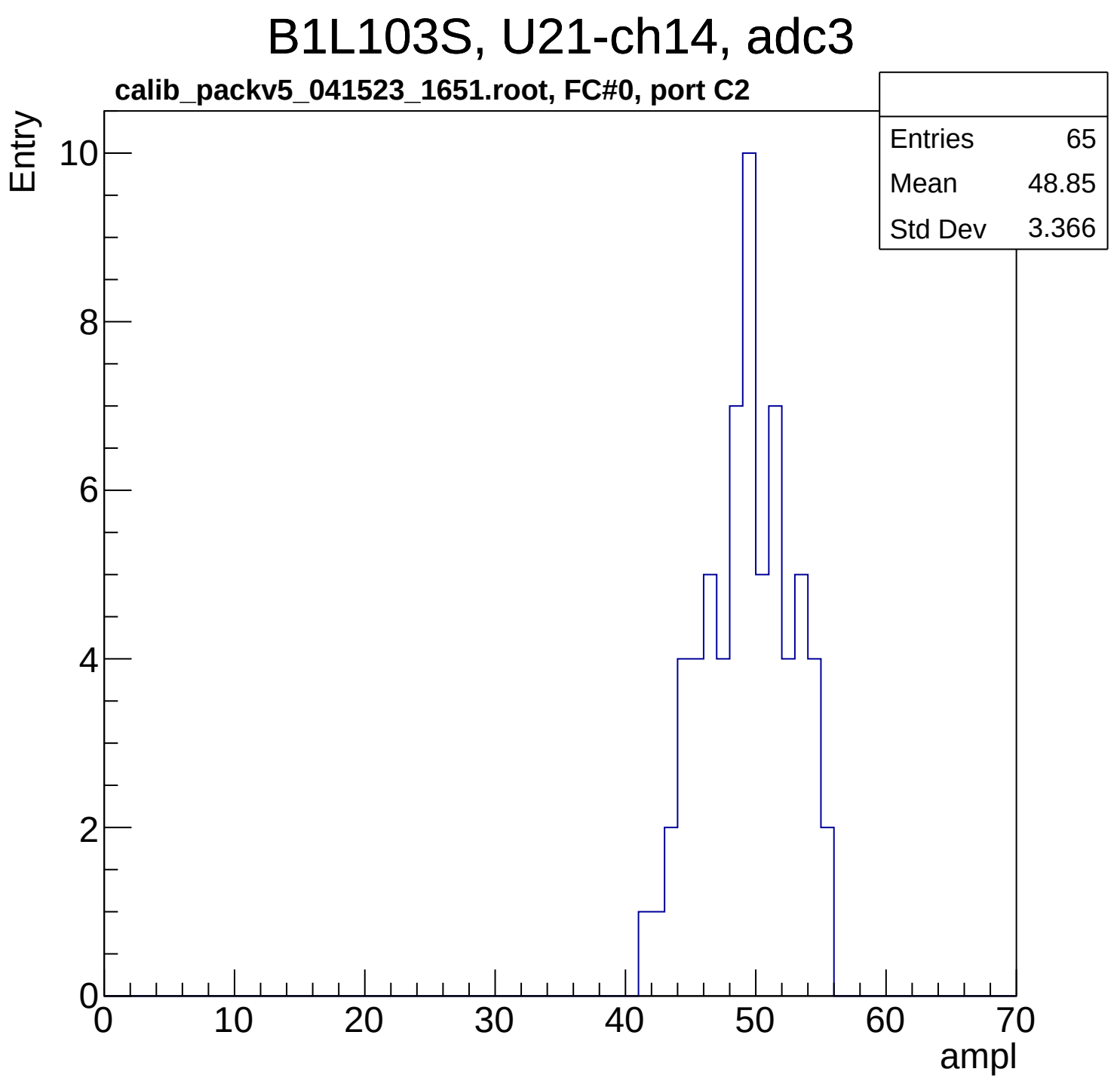
60
70


B1L103S, U21-ch14, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 48.85
Std Dev 3.366
Entry
ampl
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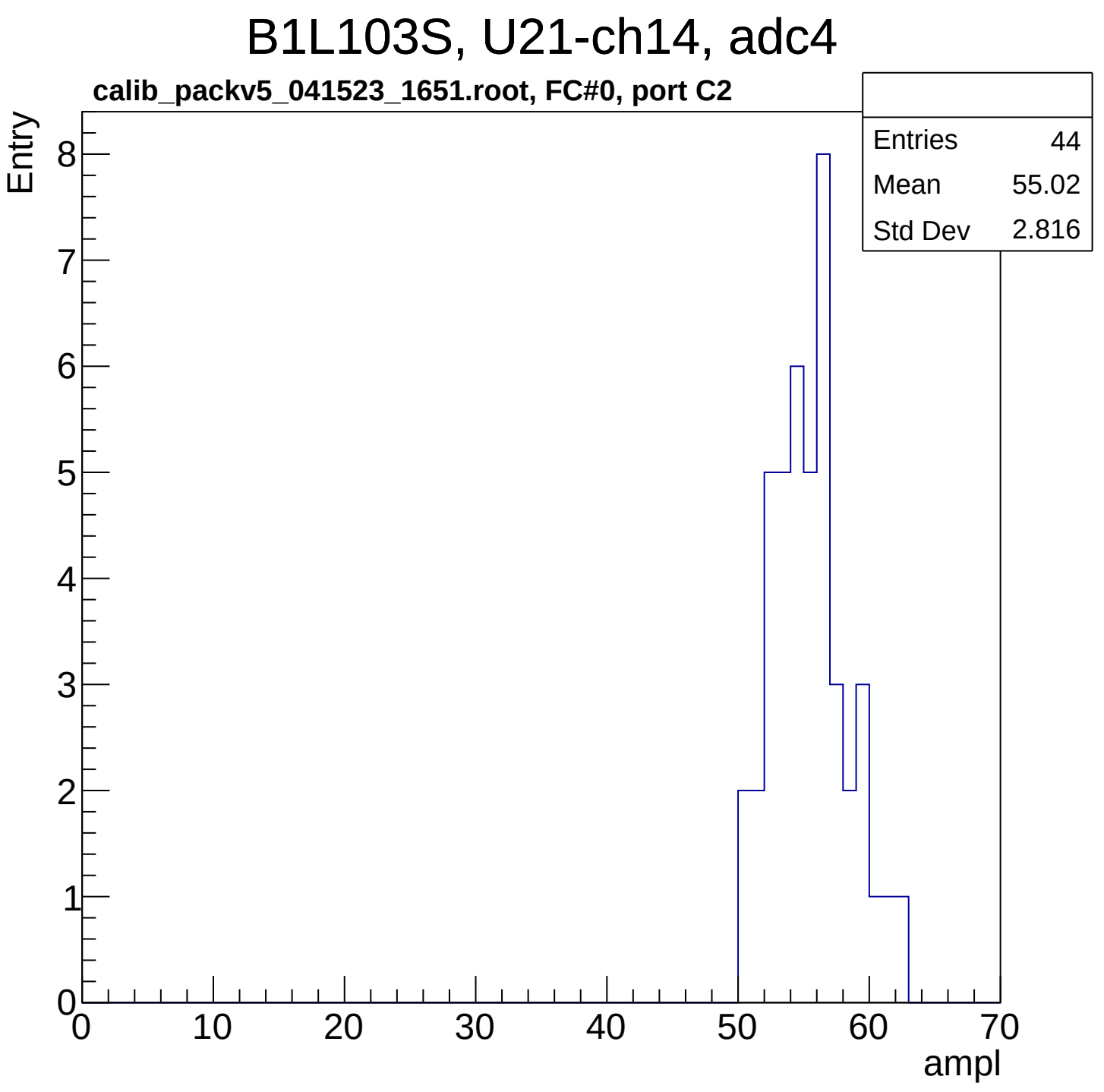
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U21-ch14, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 55.02
Std Dev 2.816
Entry
ampl
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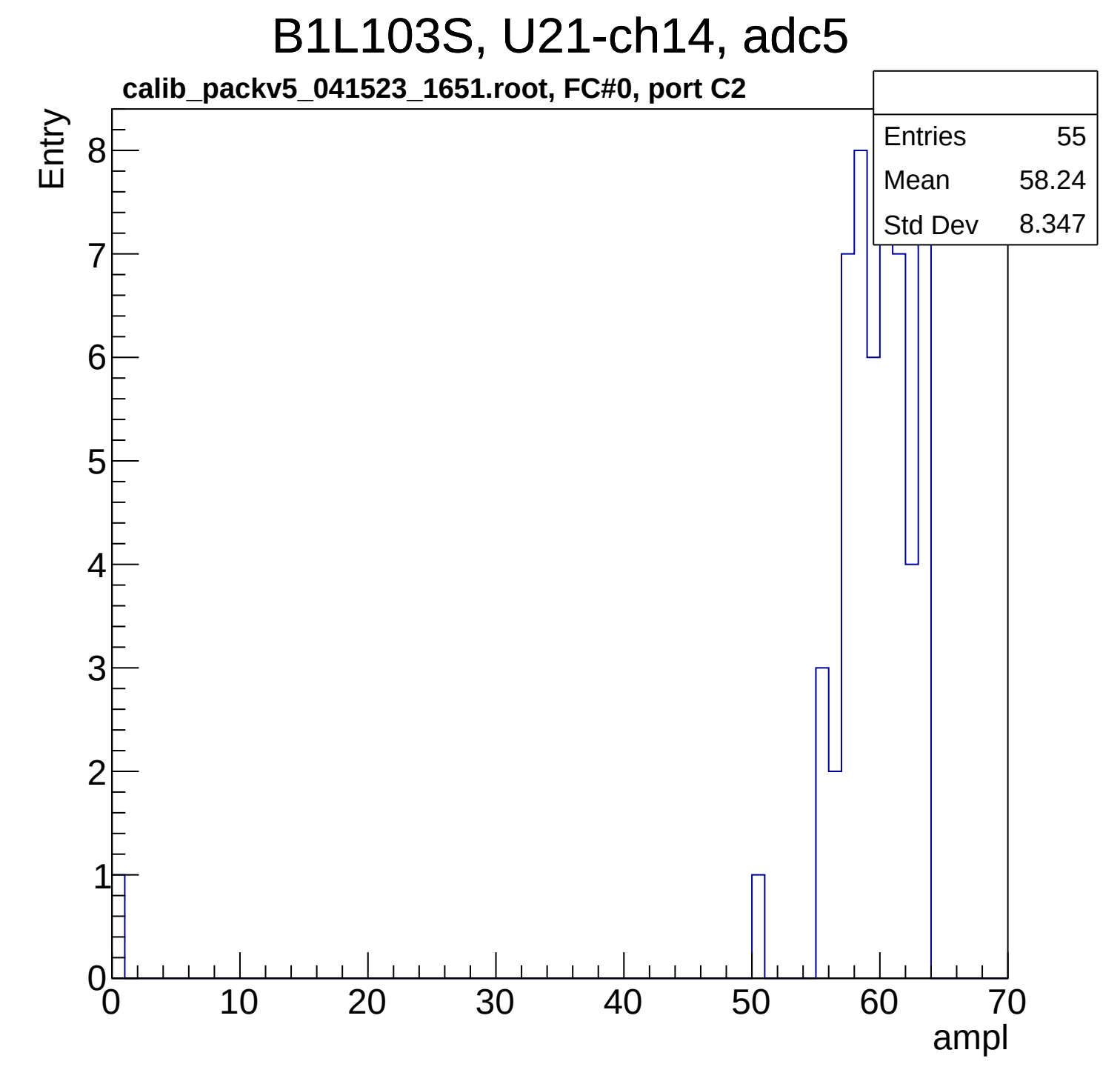
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch14, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 58.24
Std Dev 8.347
Entry
ampl
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2
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4
5
6
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0
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40
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60
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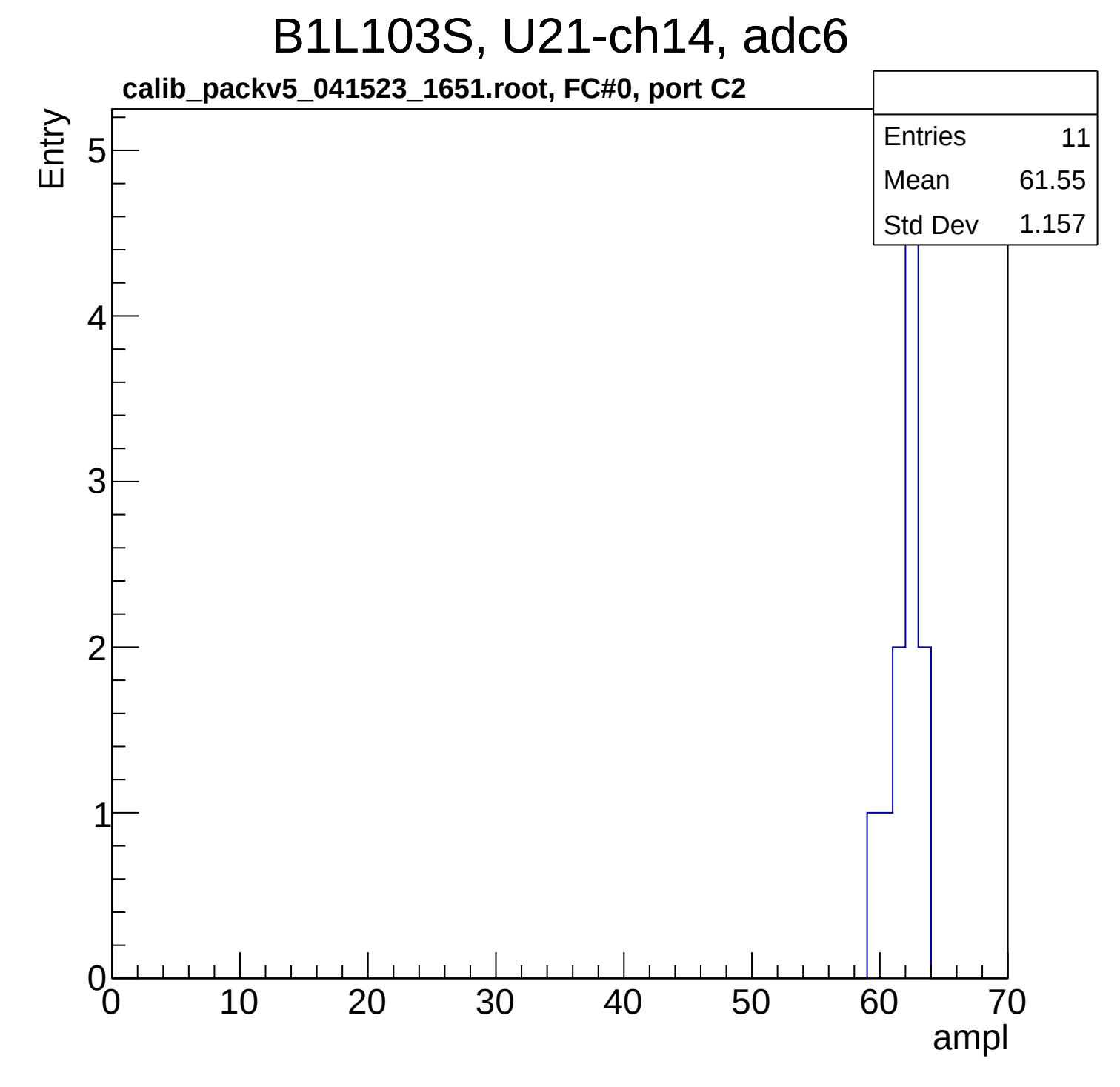
B1L103S, U21-ch14, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 61.55
Std Dev 1.157
Entry
ampl
0
1
2
3
4
5
0
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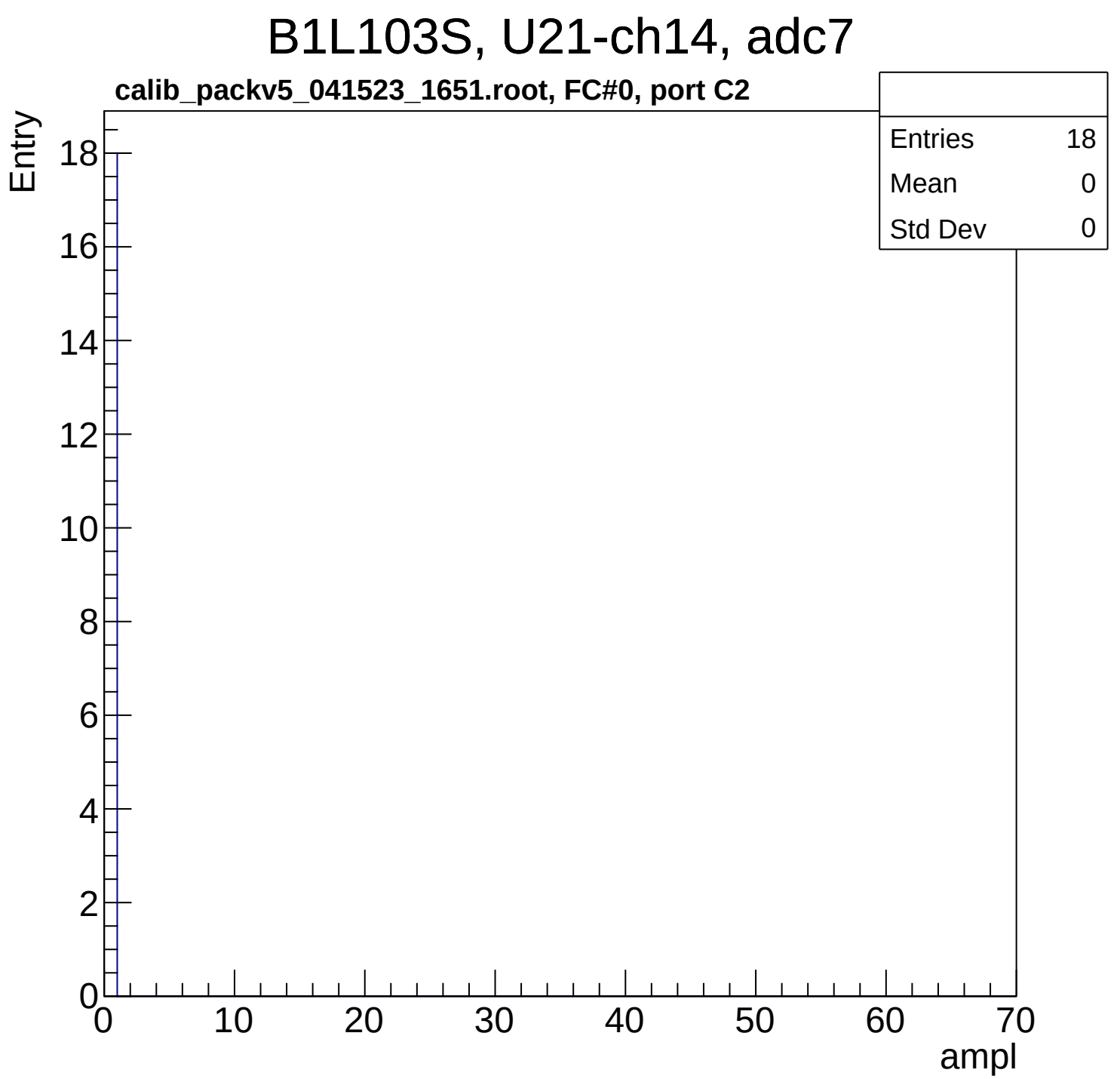
40
50
60
70


B1L103S, U21-ch14, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
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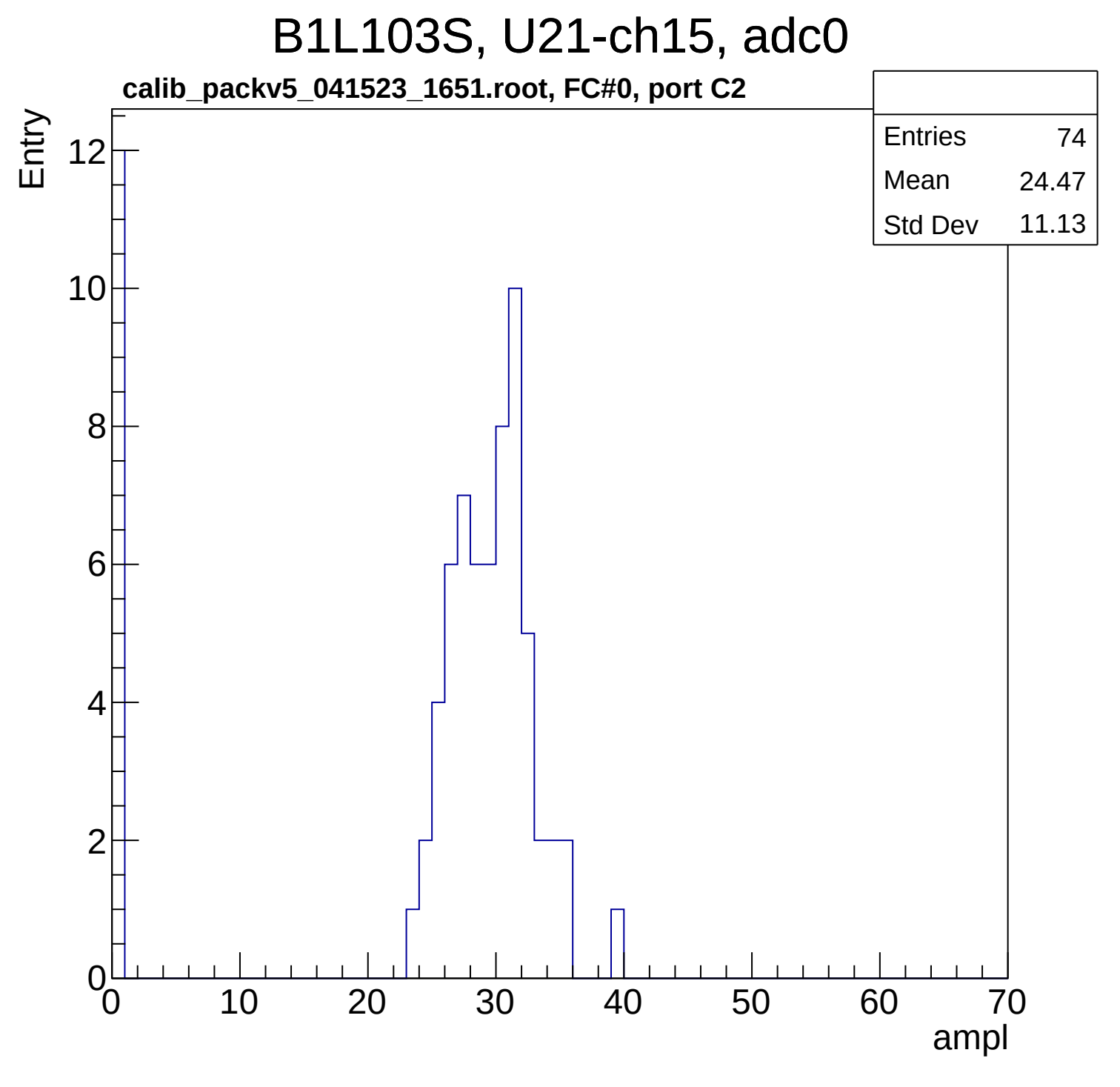
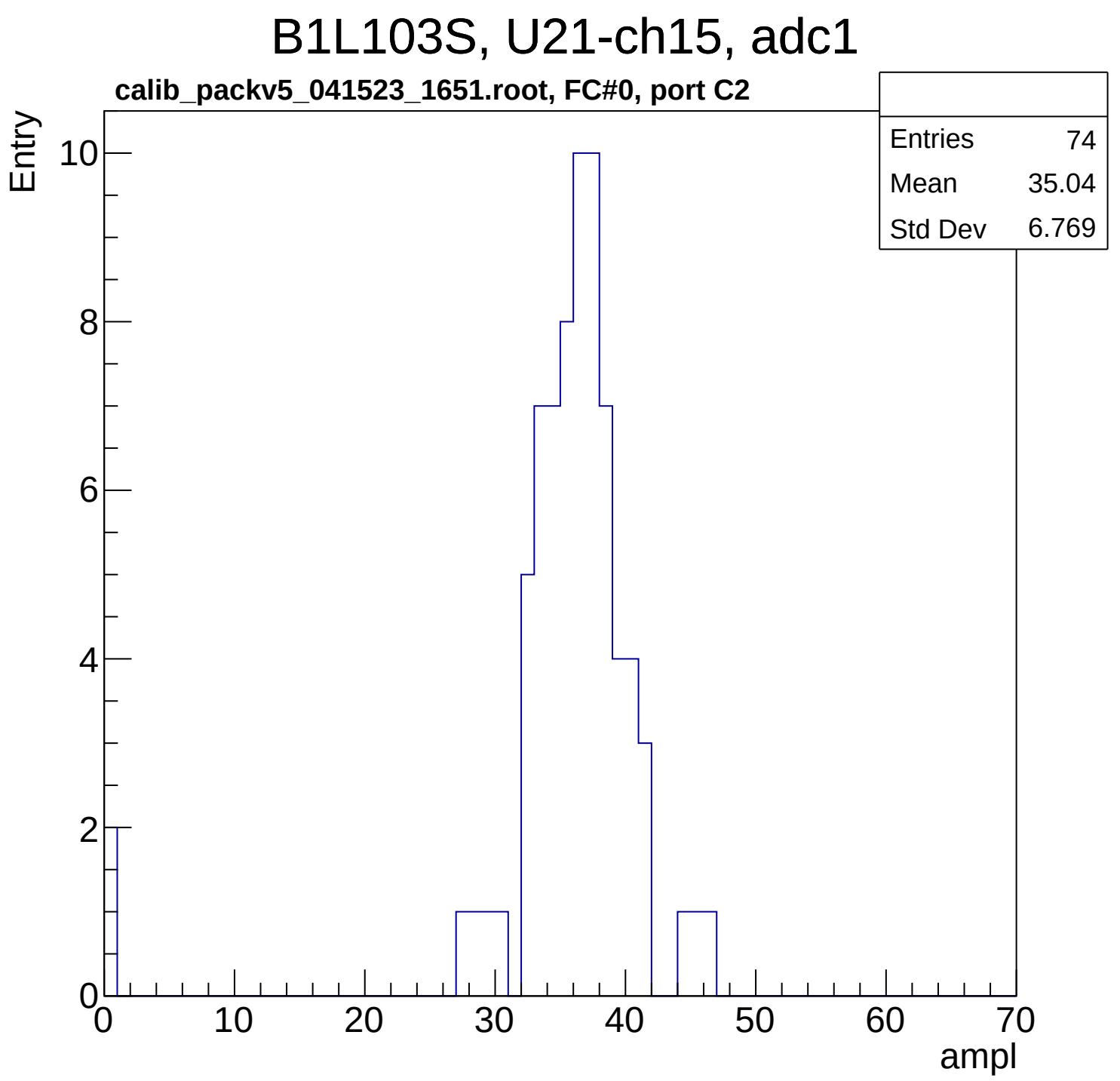
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch15, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 24.47
Std Dev 11.13
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch15, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 35.04
Std Dev 6.769
Entry
ampl
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2
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10
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40
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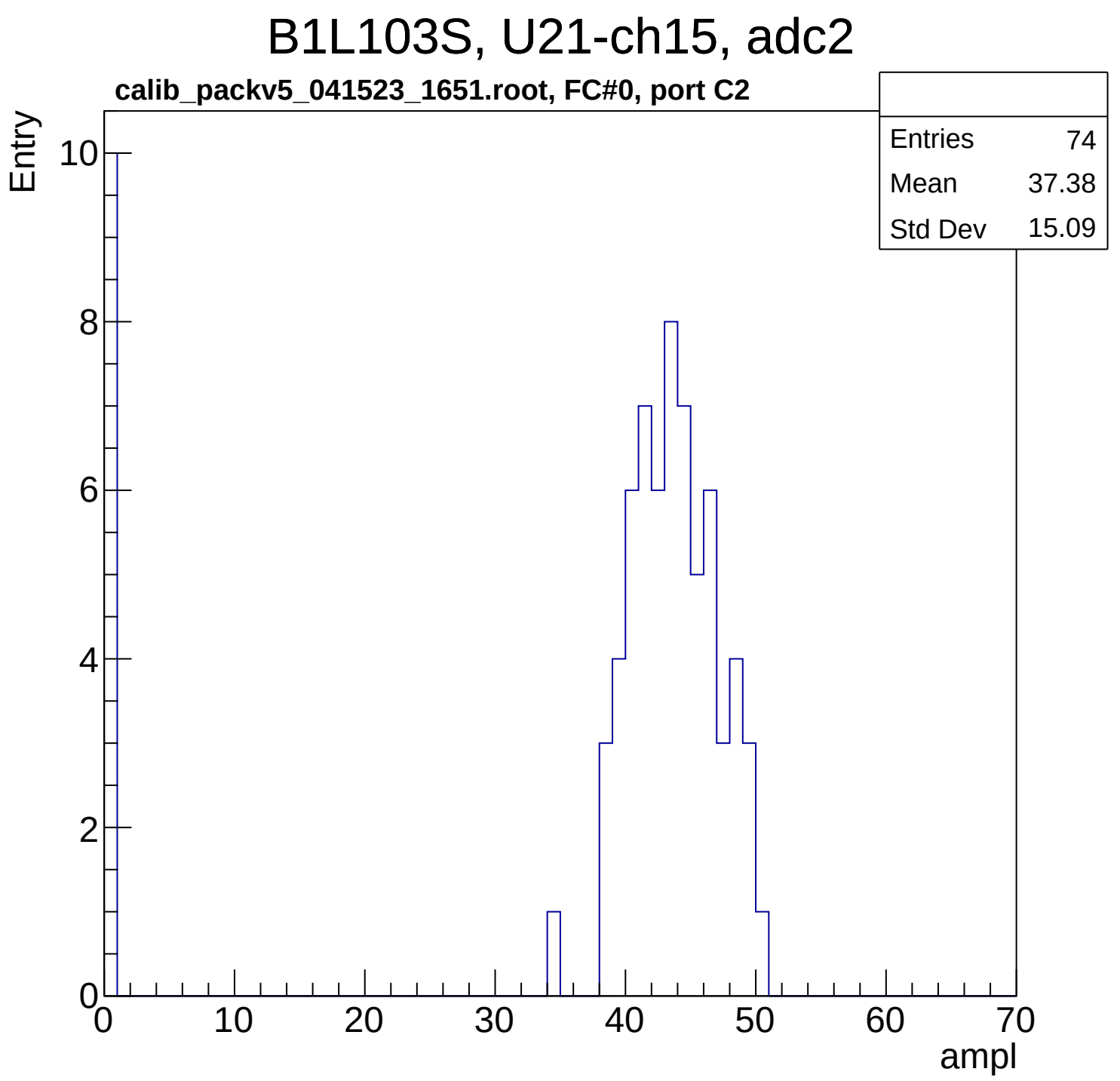
60
70


B1L103S, U21-ch15, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 37.38
Std Dev 15.09
Entry
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10
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10
20
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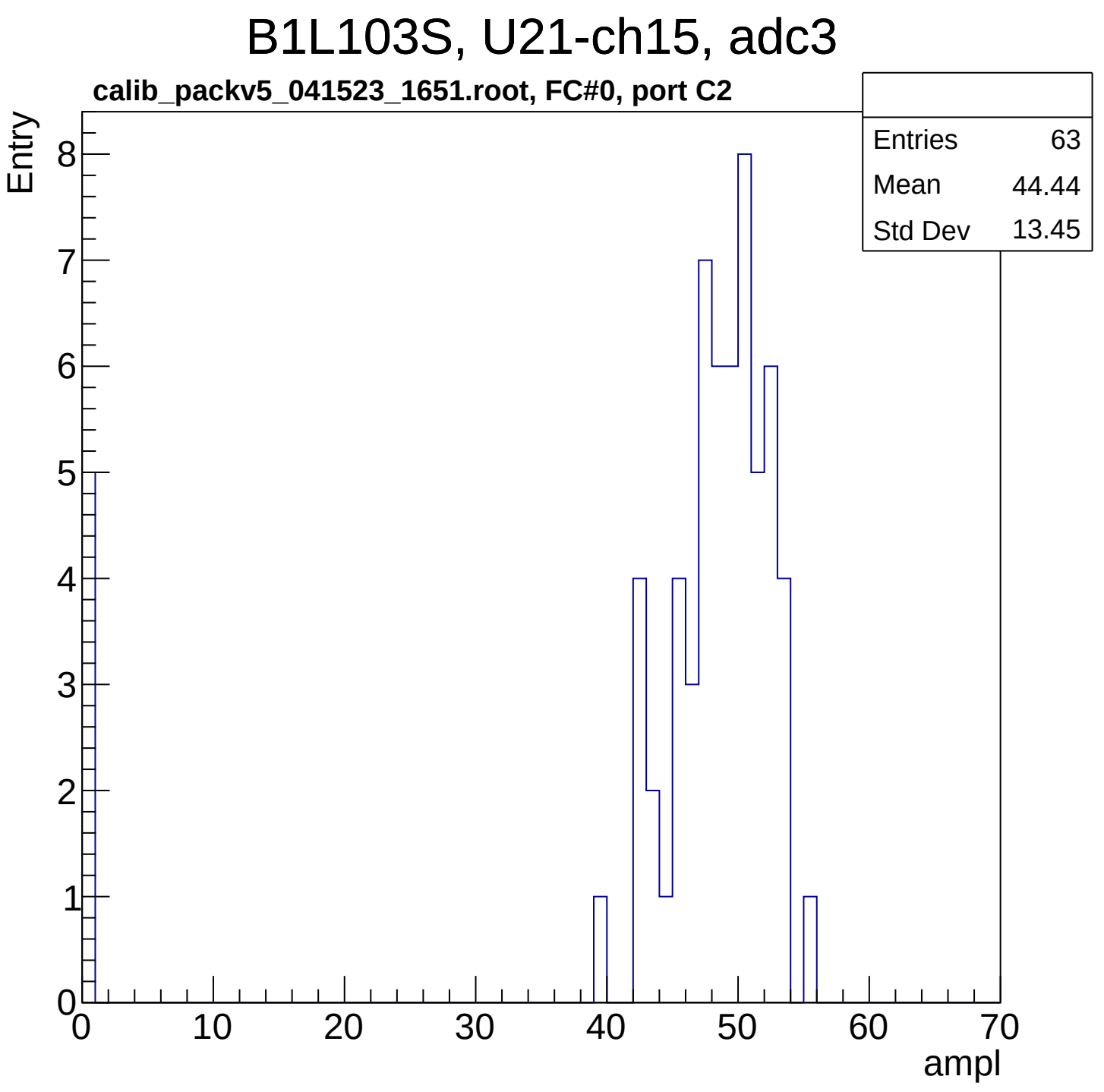
50
60
70
ampl


B1L103S, U21-ch15, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 44.44
Std Dev 13.45
Entry
ampl
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1
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3
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0
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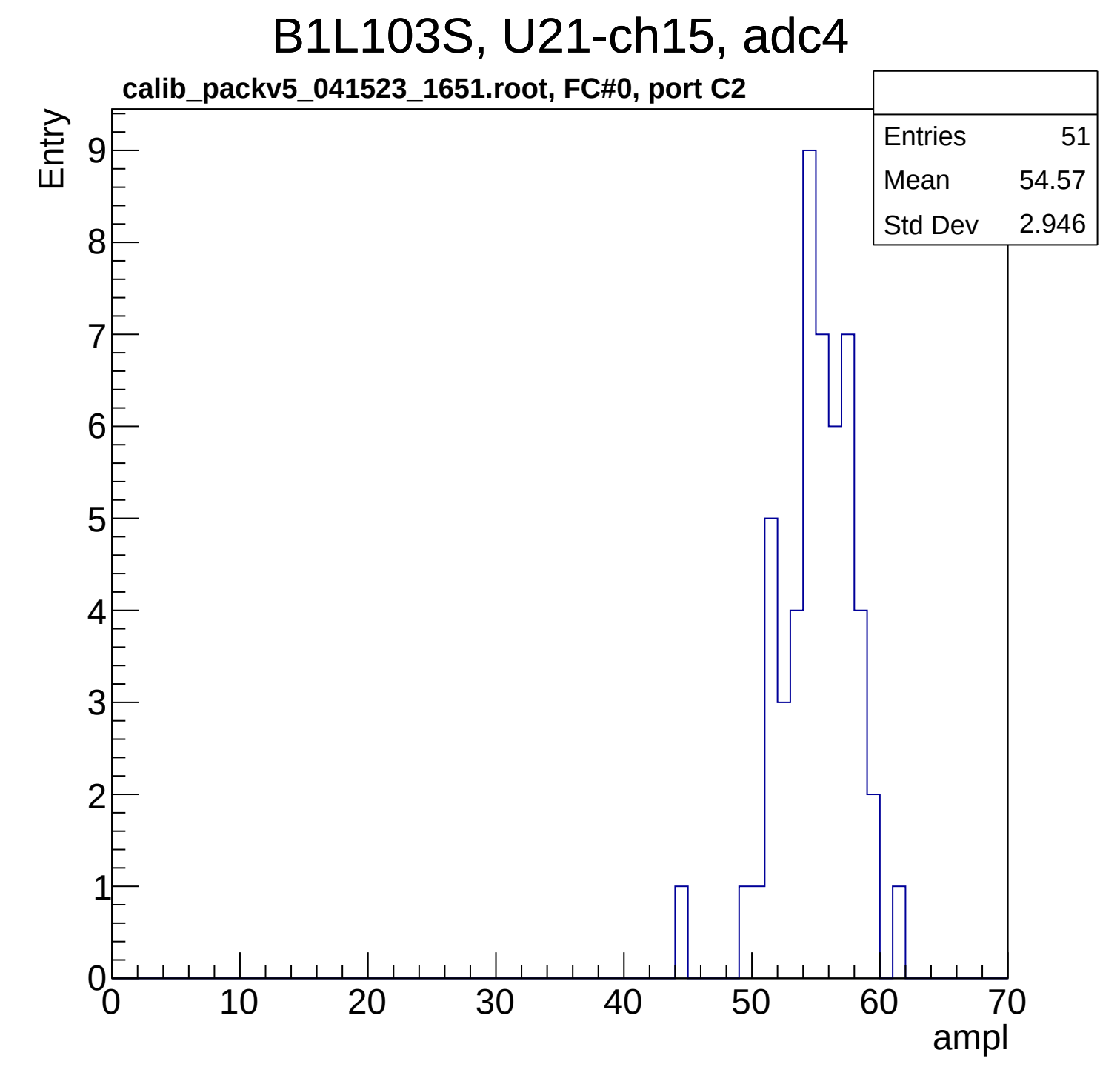
60
70


B1L103S, U21-ch15, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 54.57
Std Dev 2.946
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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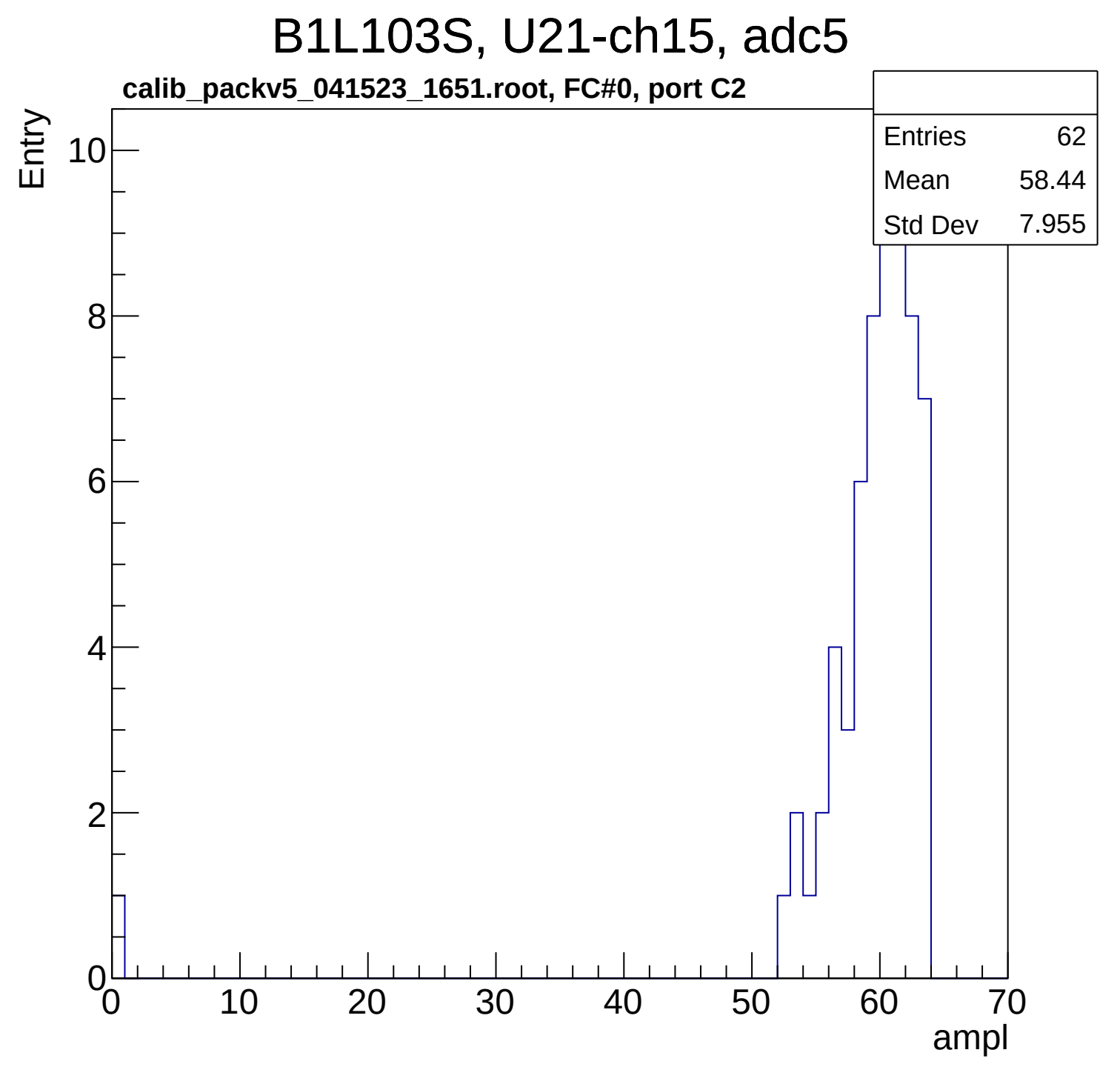
40
50
60
70


B1L103S, U21-ch15, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 58.44
Std Dev 7.955
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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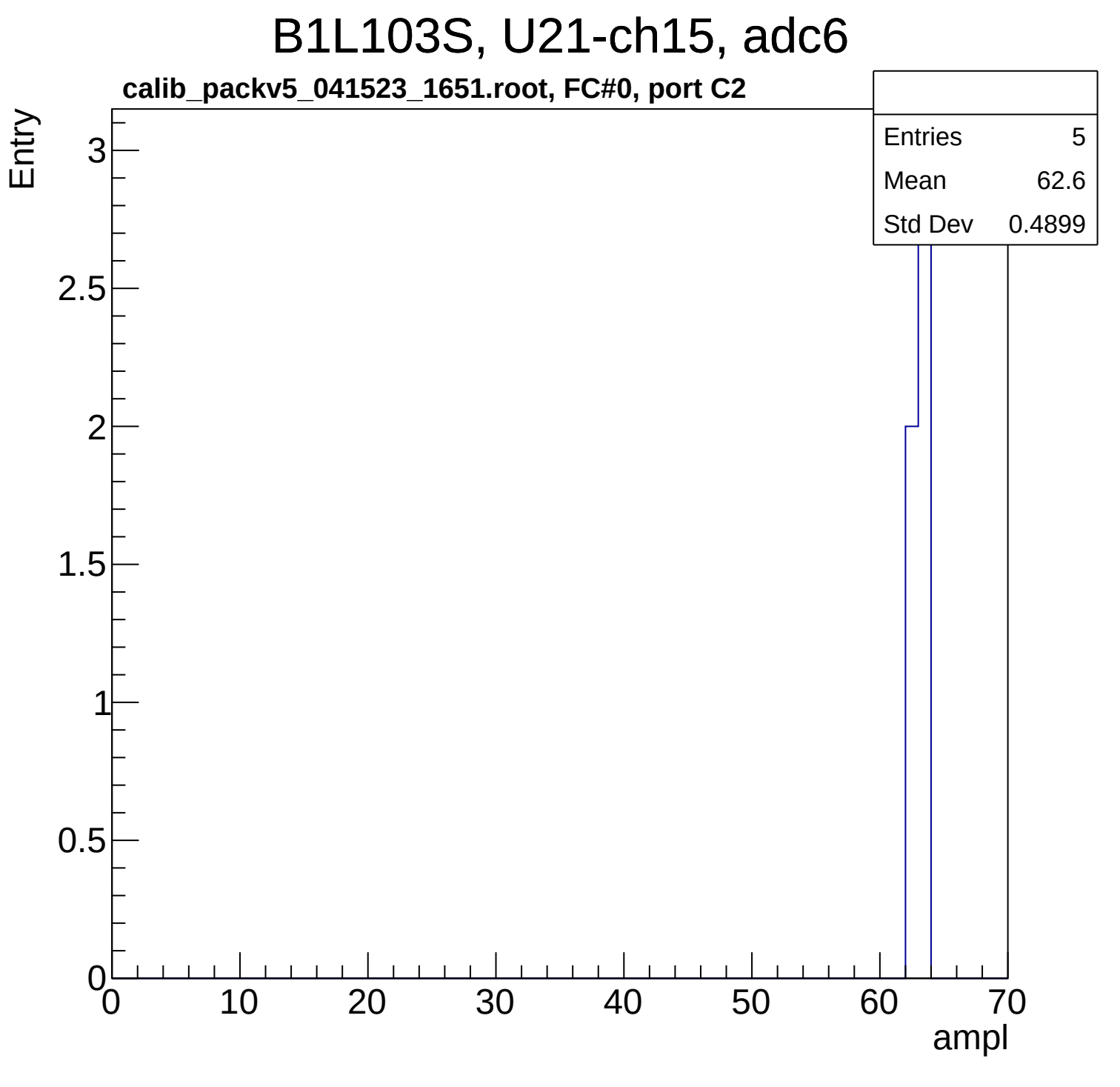
B1L103S, U21-ch15, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 62.6
Std Dev 0.4899
Entry
ampl
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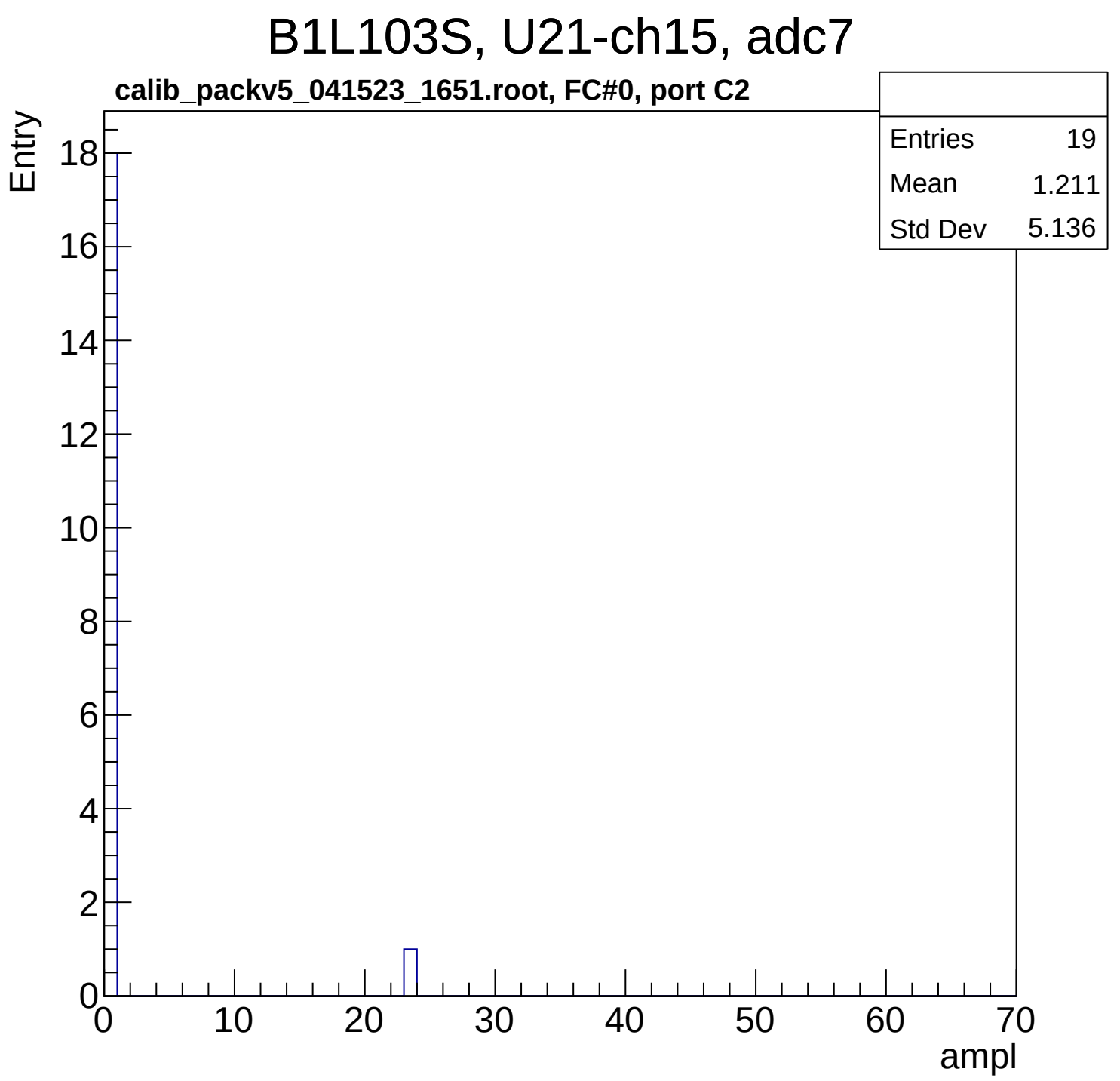
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U21-ch15, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.211
Std Dev 5.136
Entry
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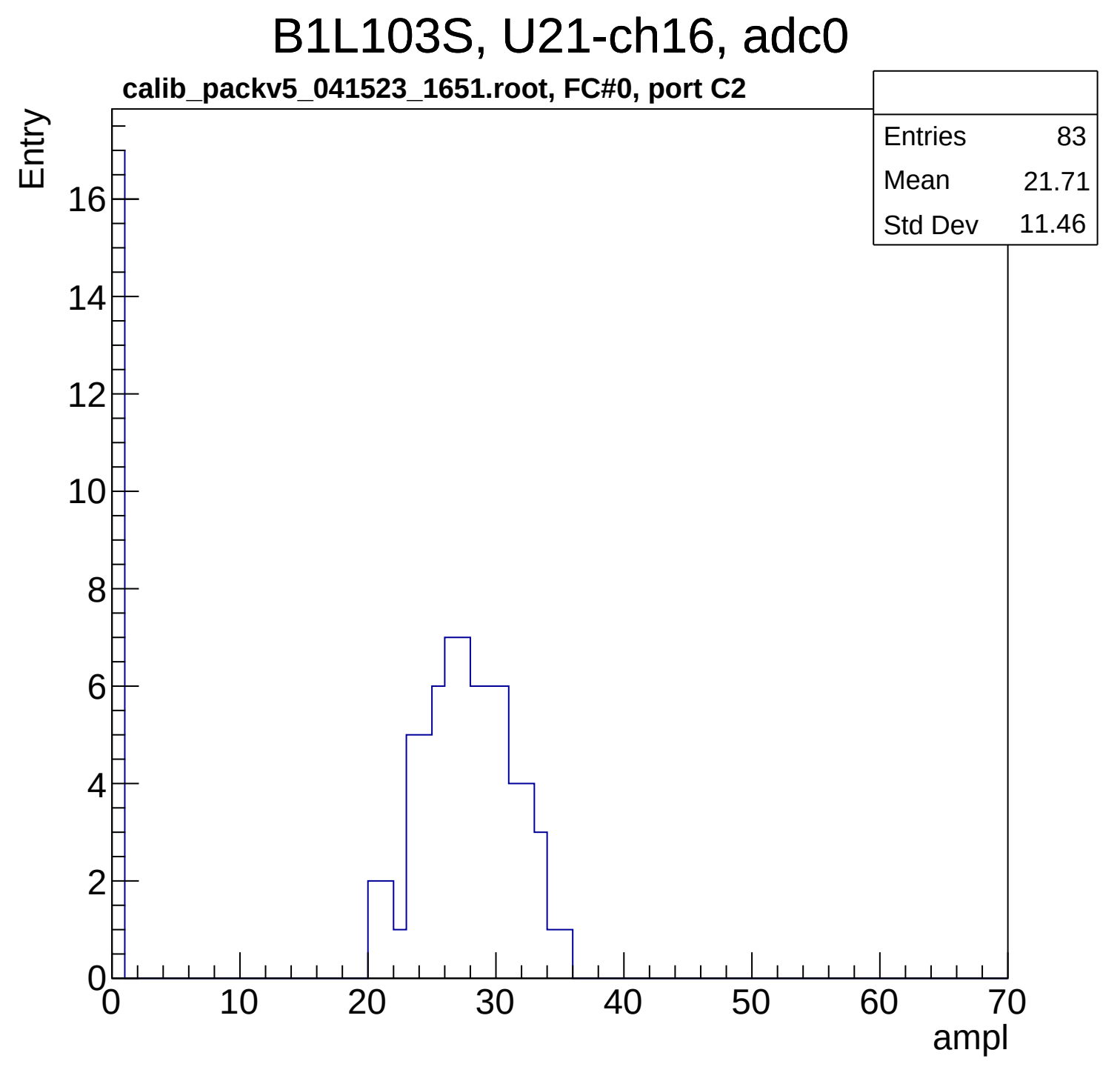
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch16, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 21.71
Std Dev 11.46
Entry
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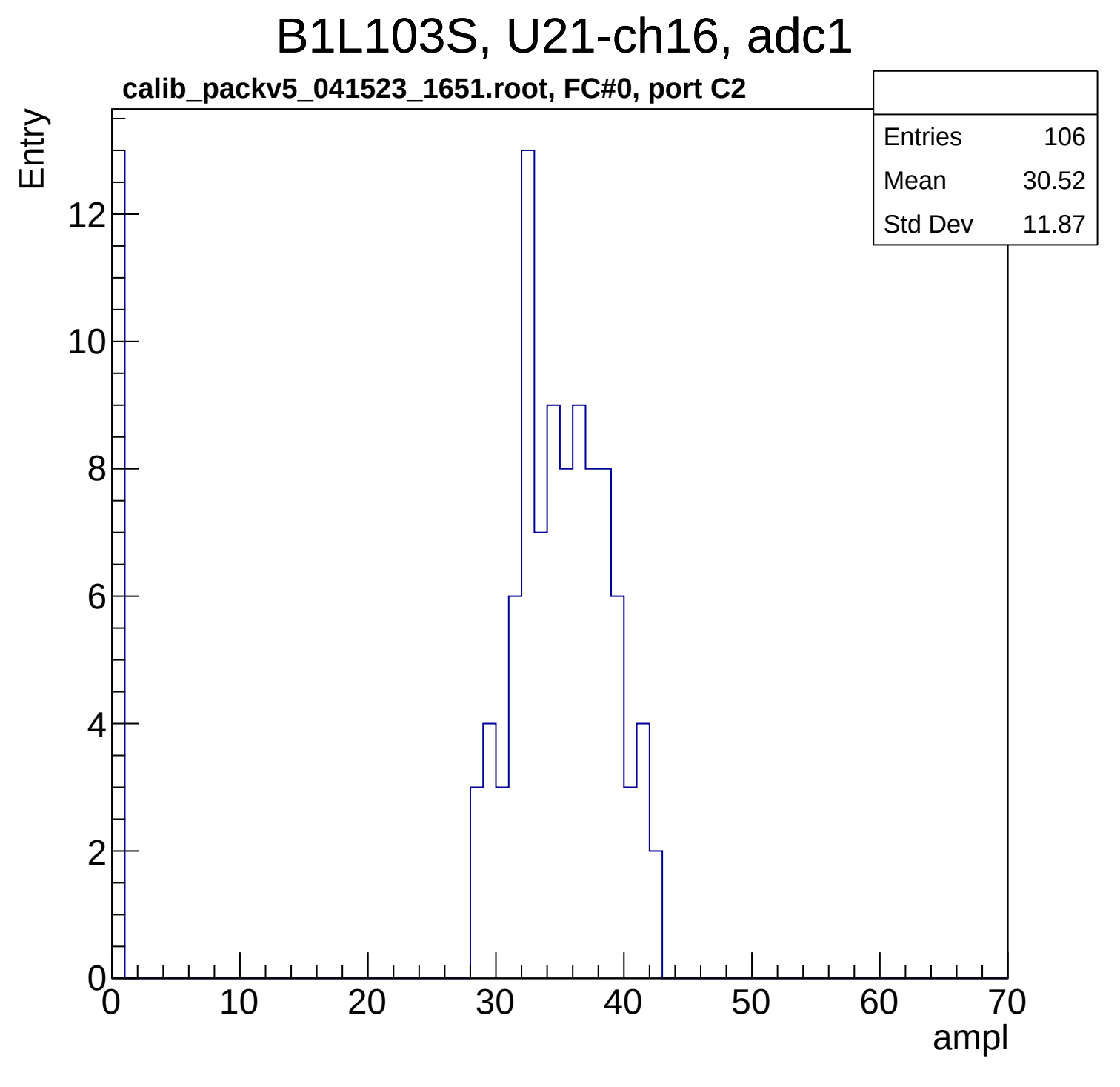
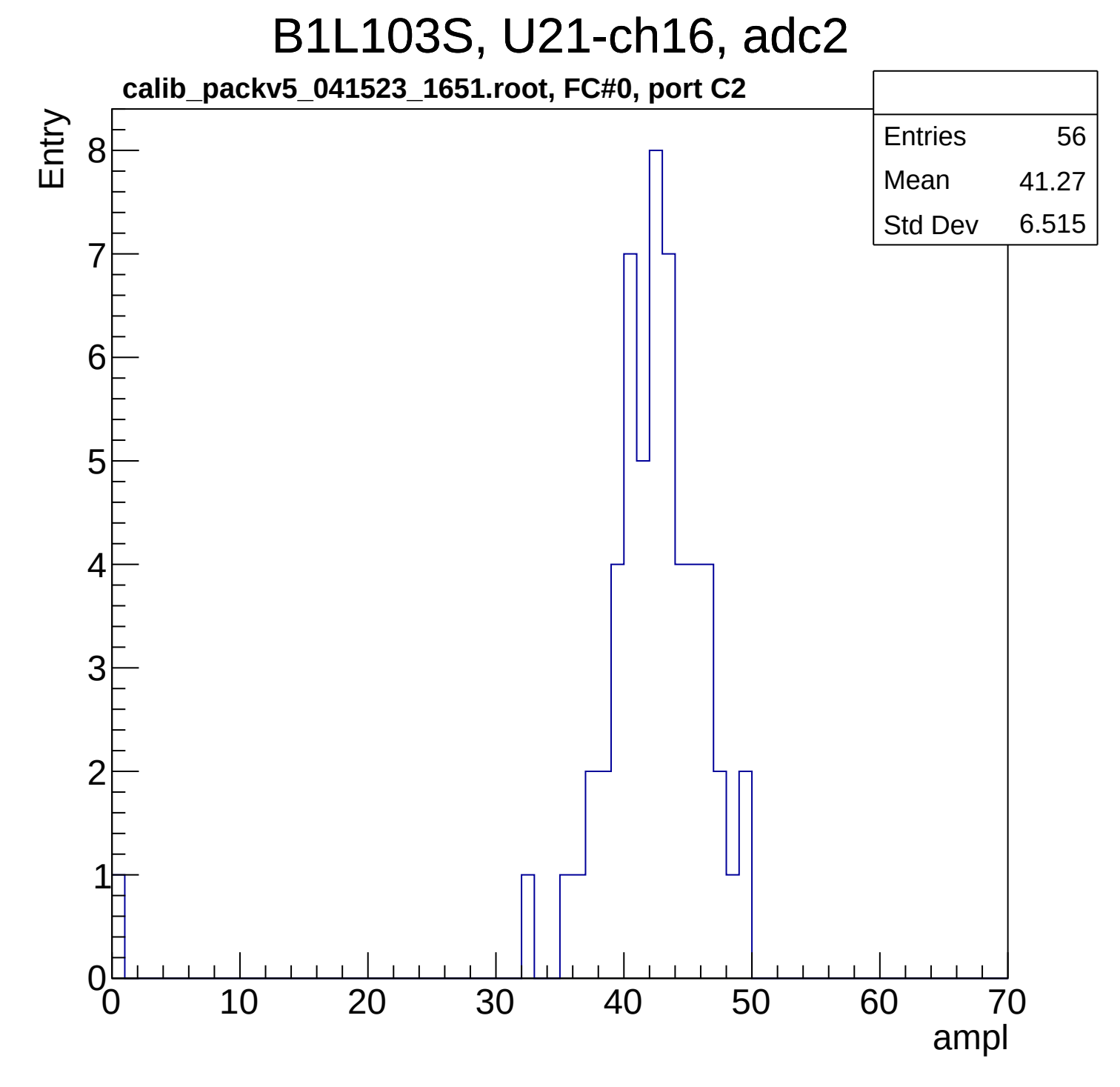
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch16, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 106
Mean 30.52
Std Dev 11.87
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch16, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 41.27
Std Dev 6.515
Entry
ampl
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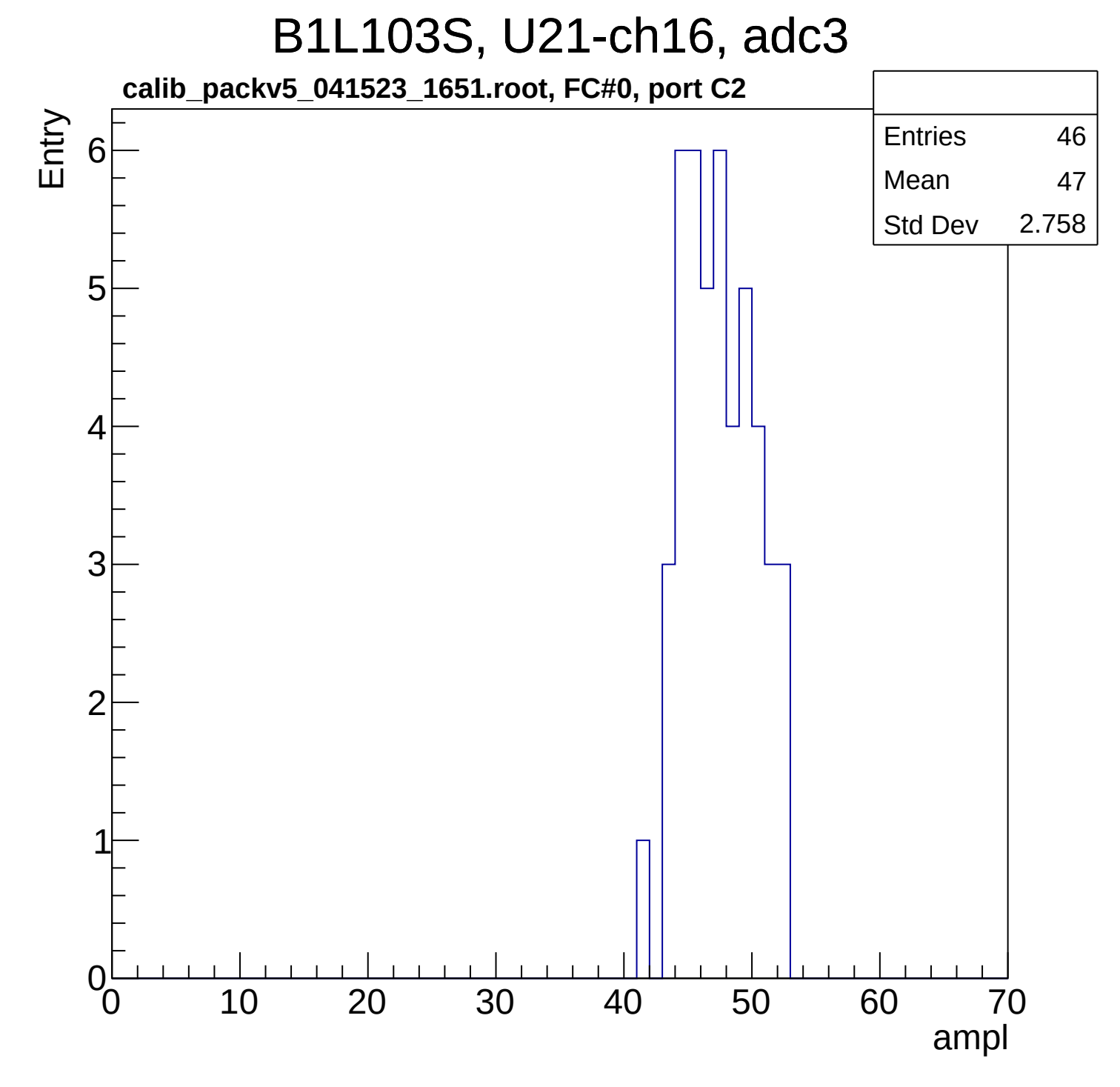
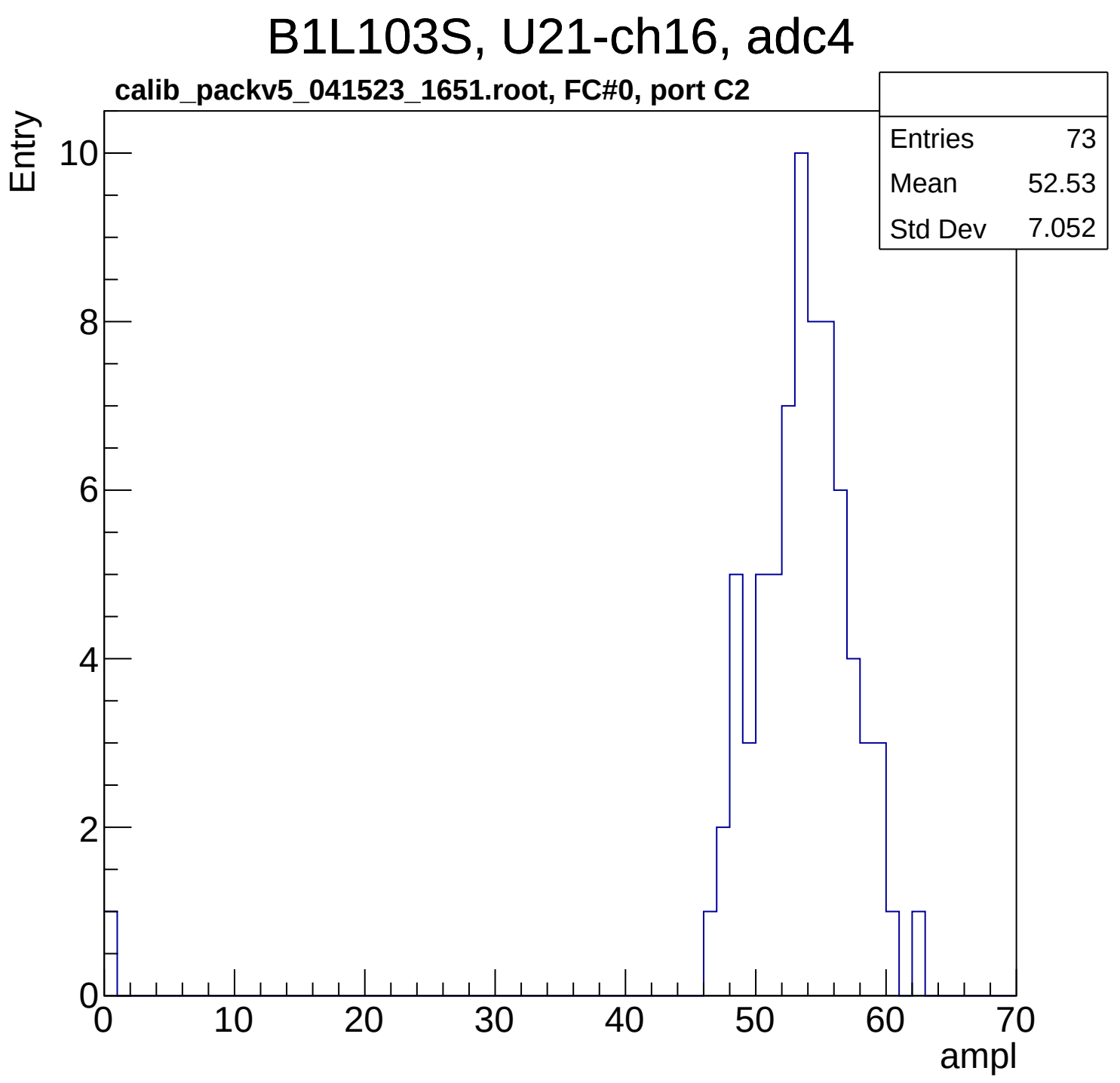
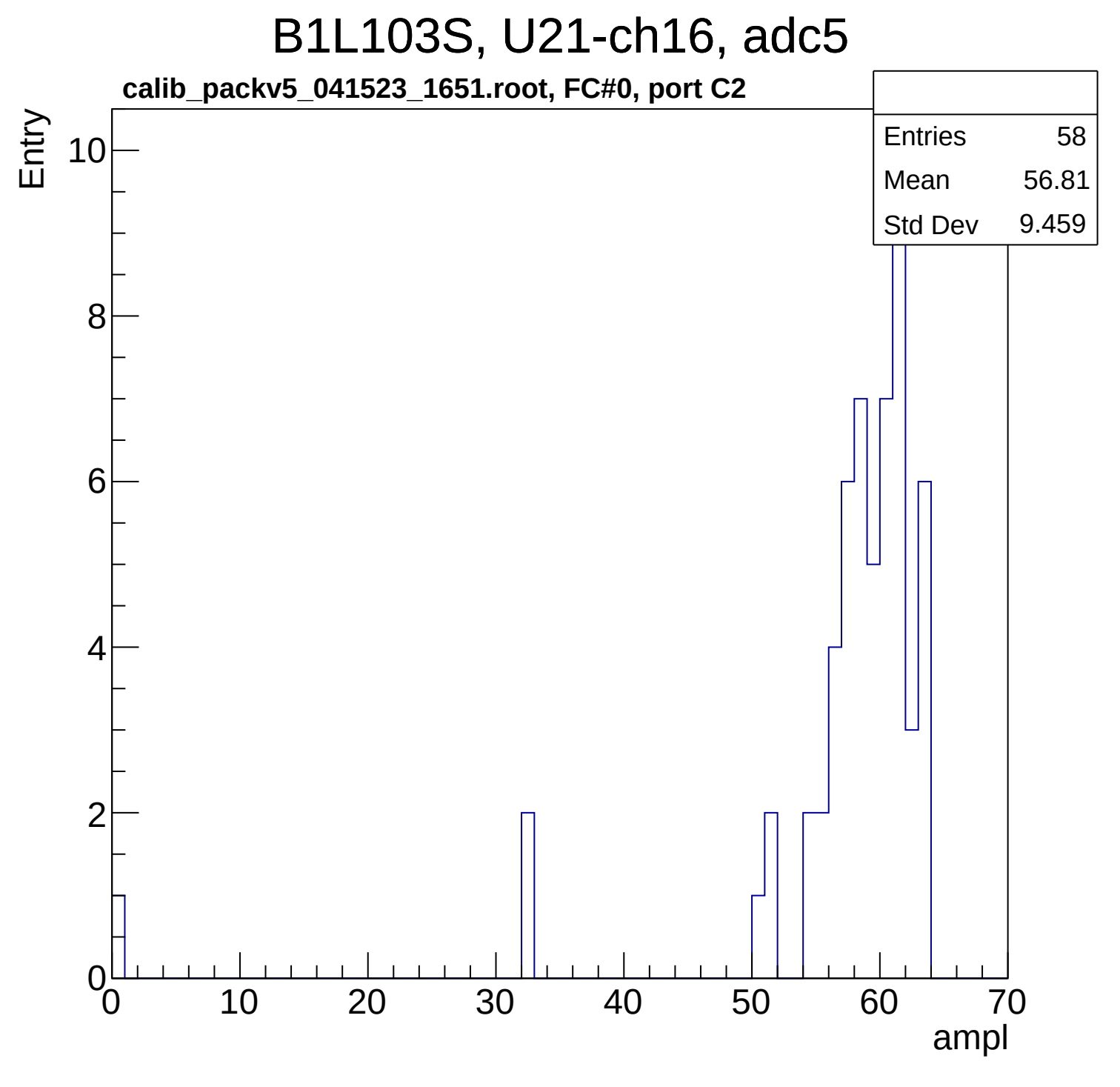
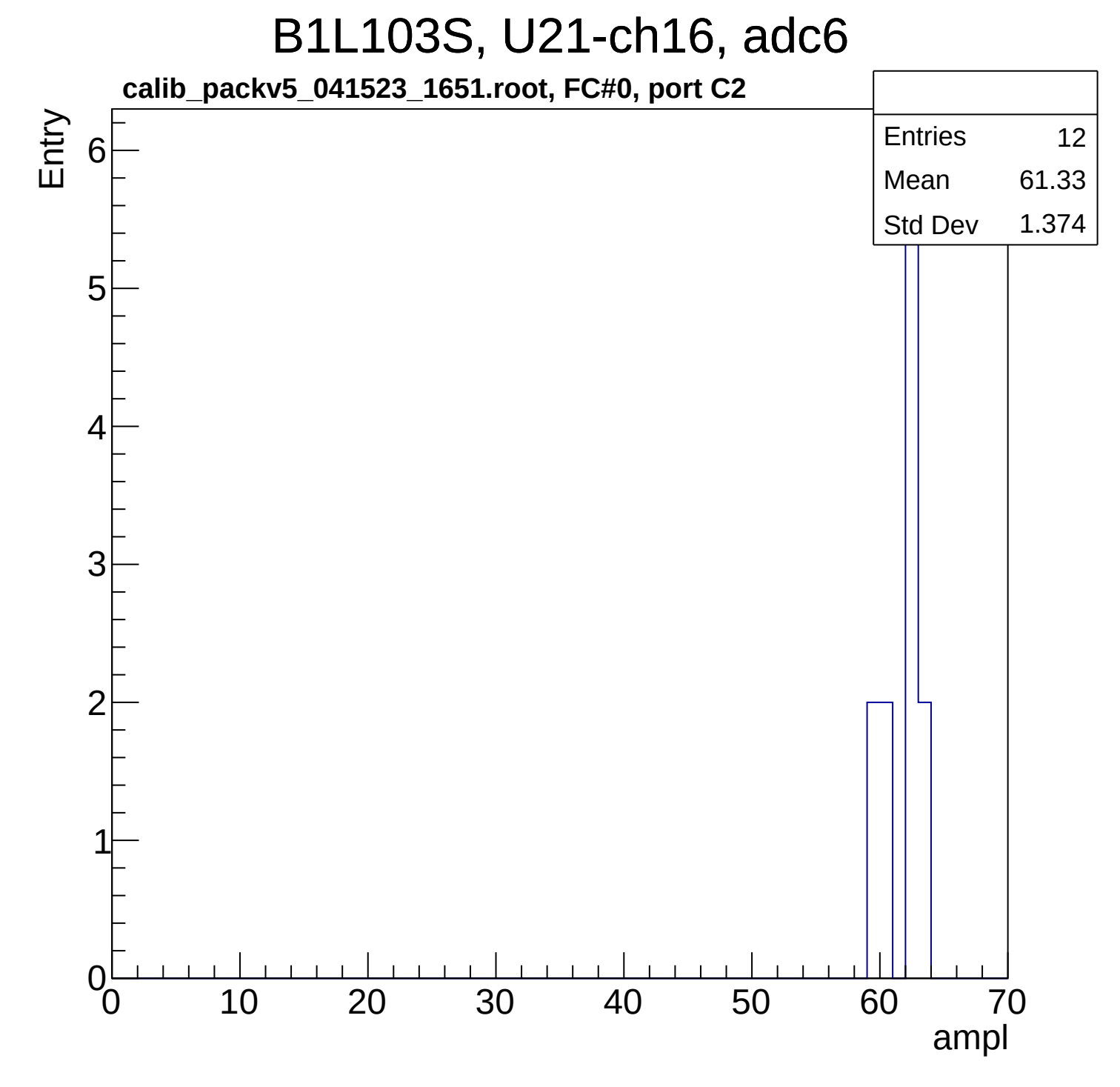
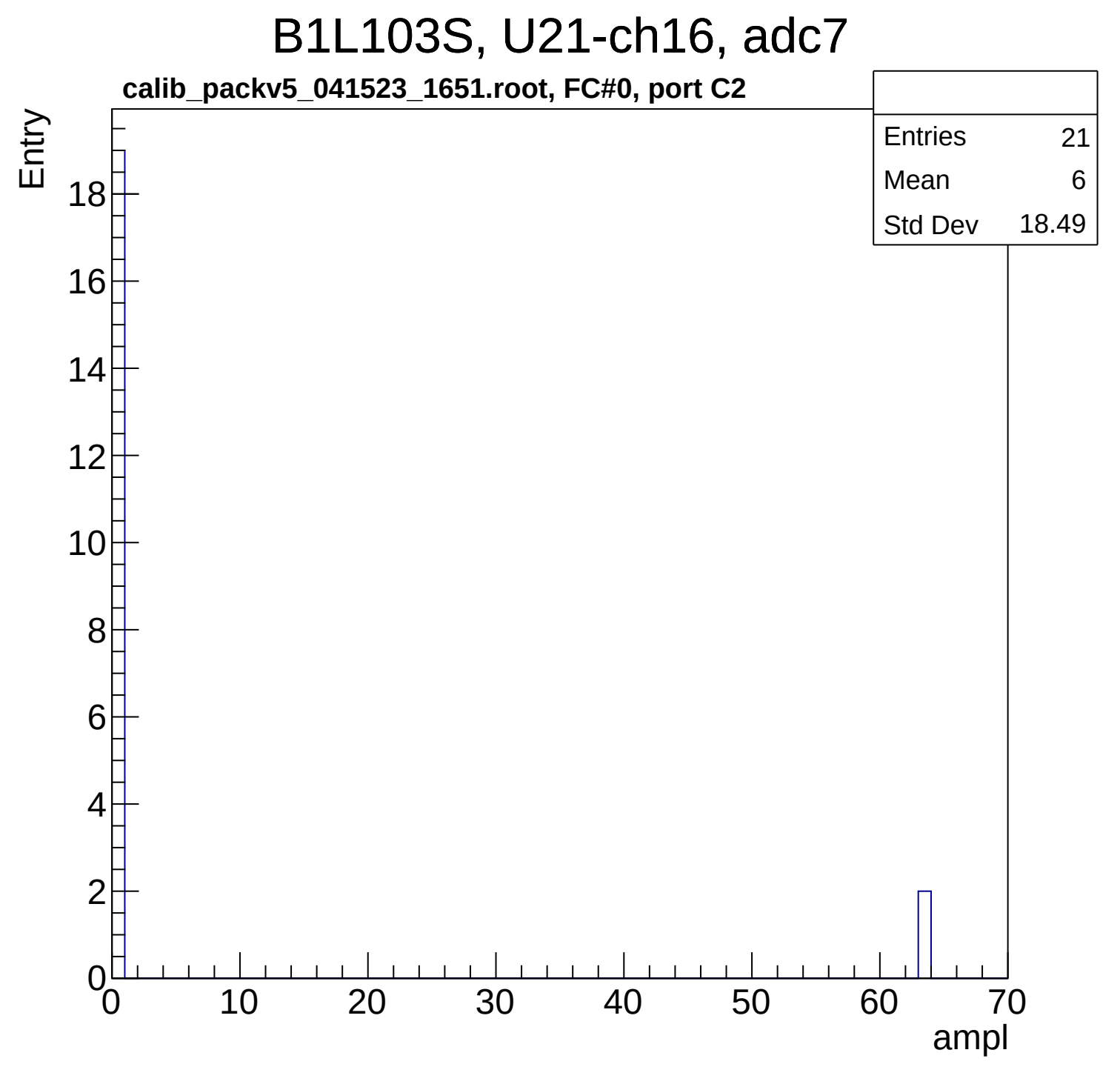
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

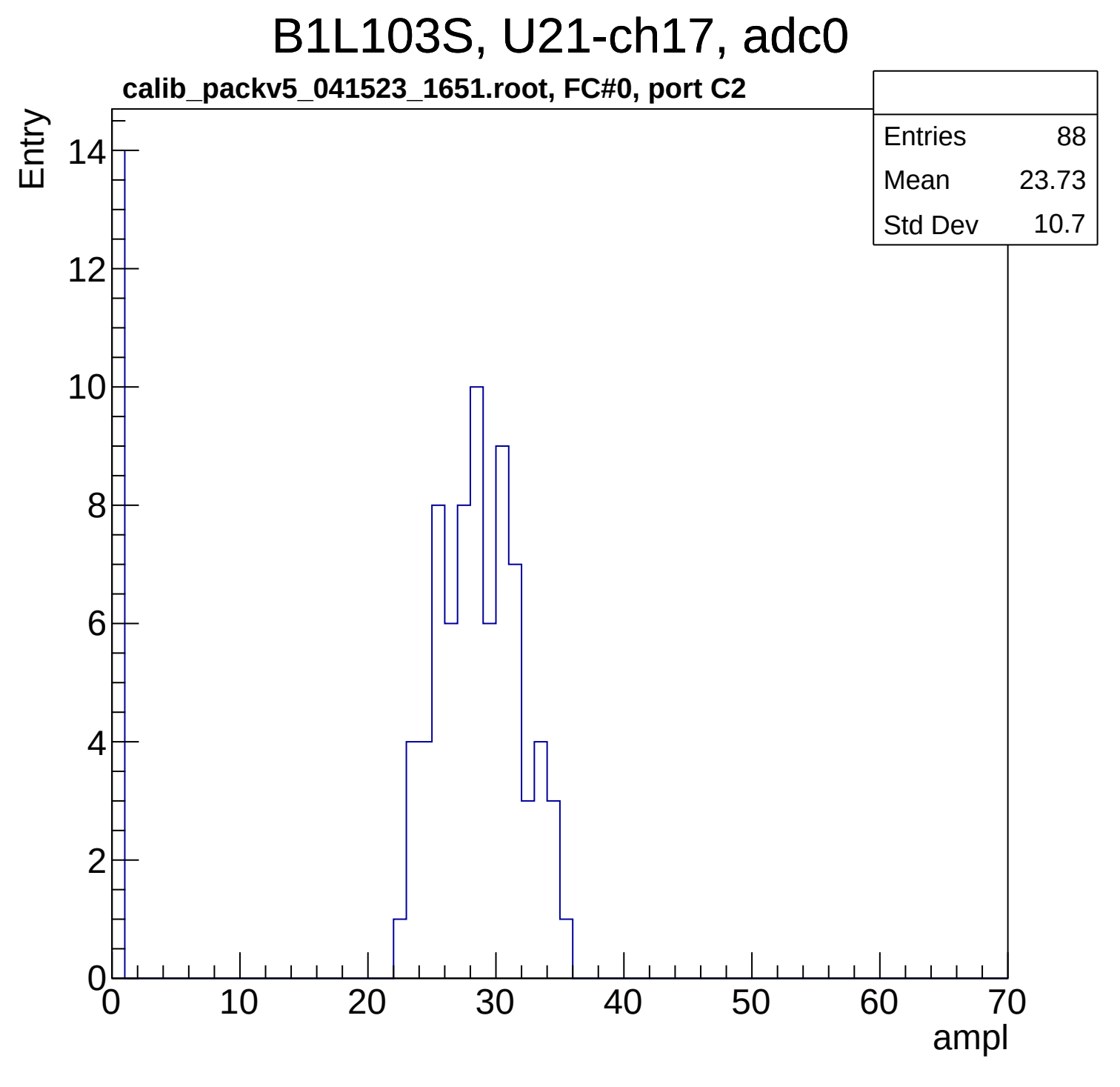

B1L103S, U21-ch16, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 47
Std Dev 2.758
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

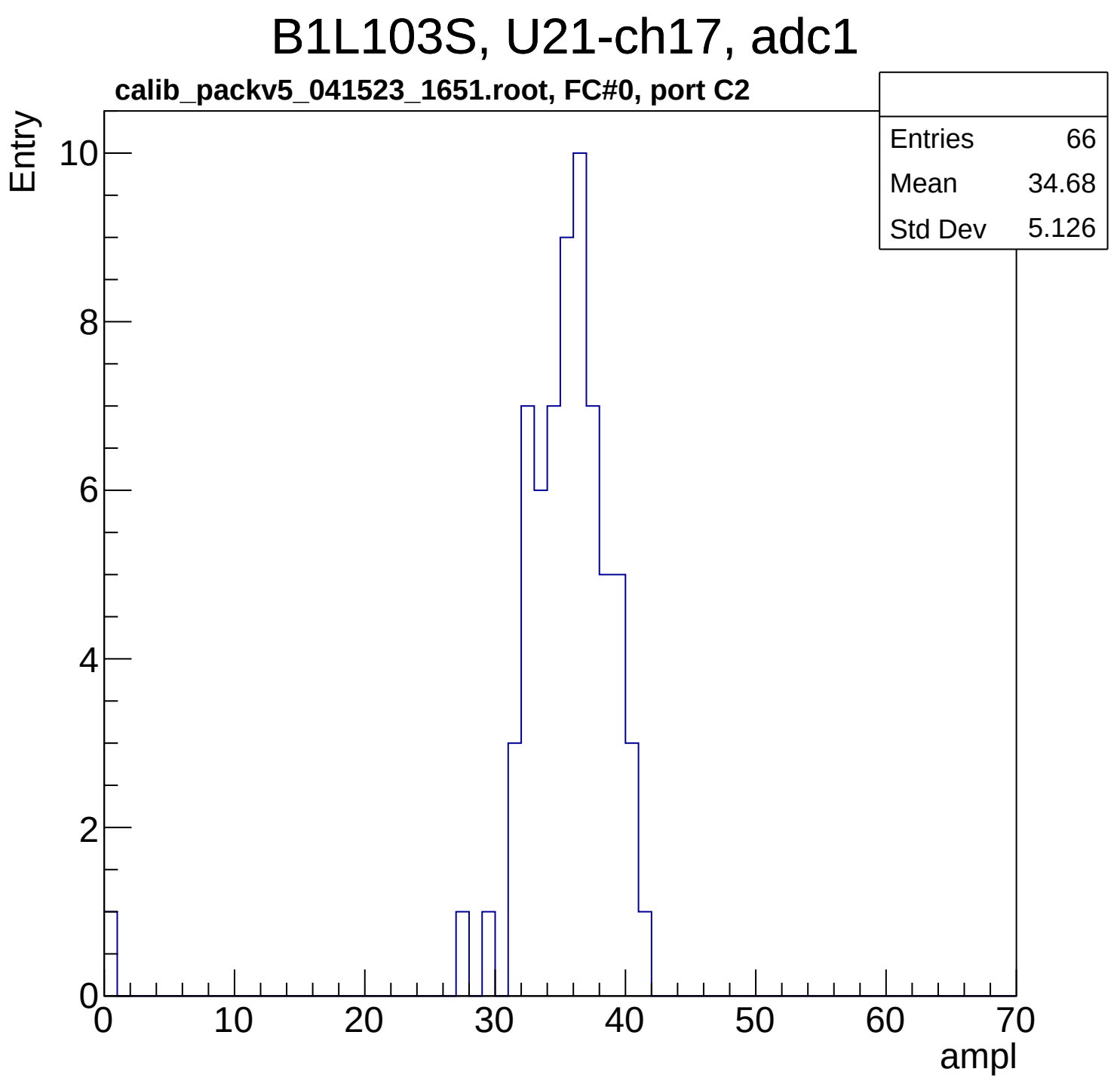

B1L103S, U21-ch16, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 52.53
Std Dev 7.052
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

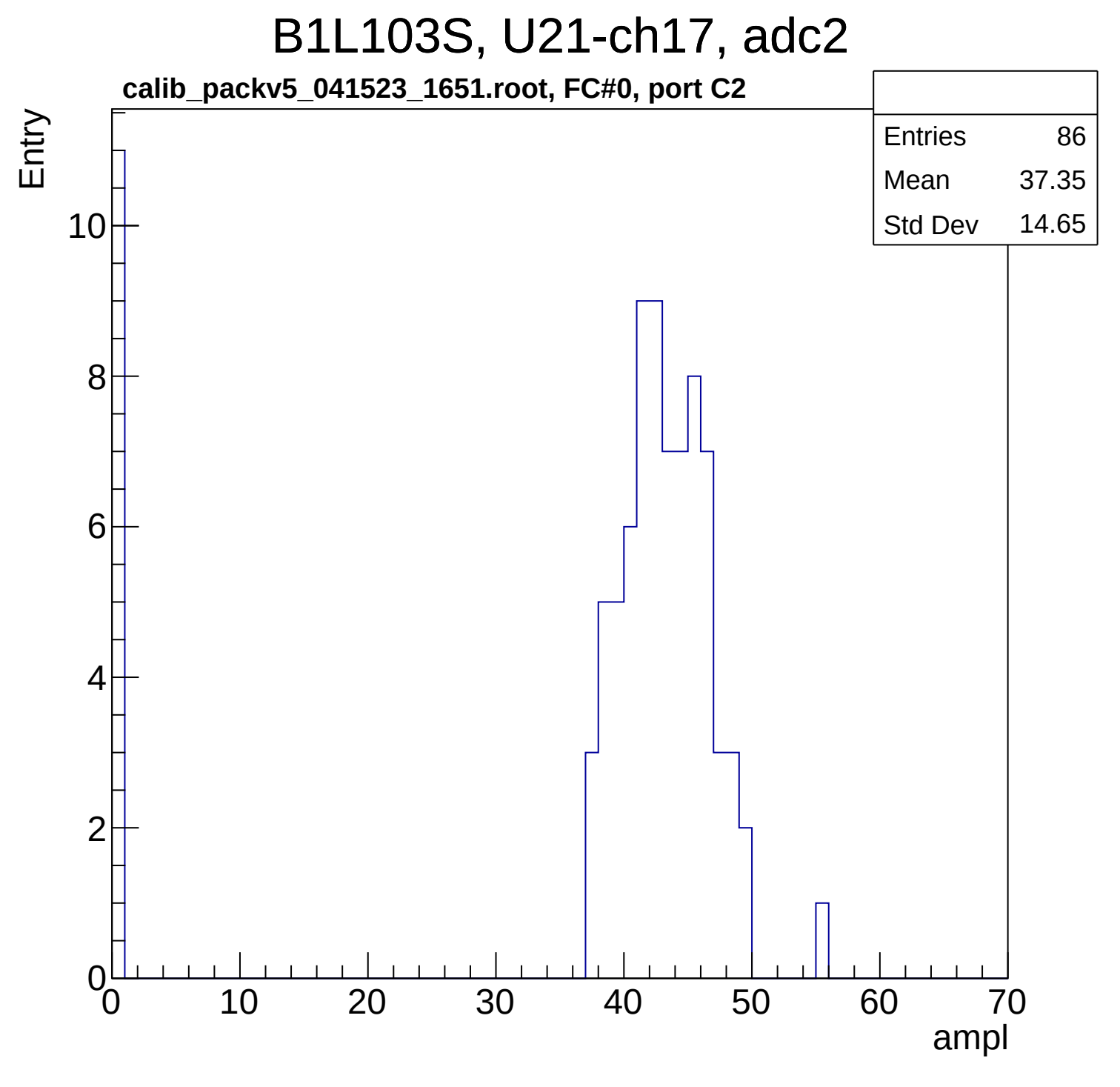

B1L103S, U21-ch16, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 56.81
Std Dev 9.459
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

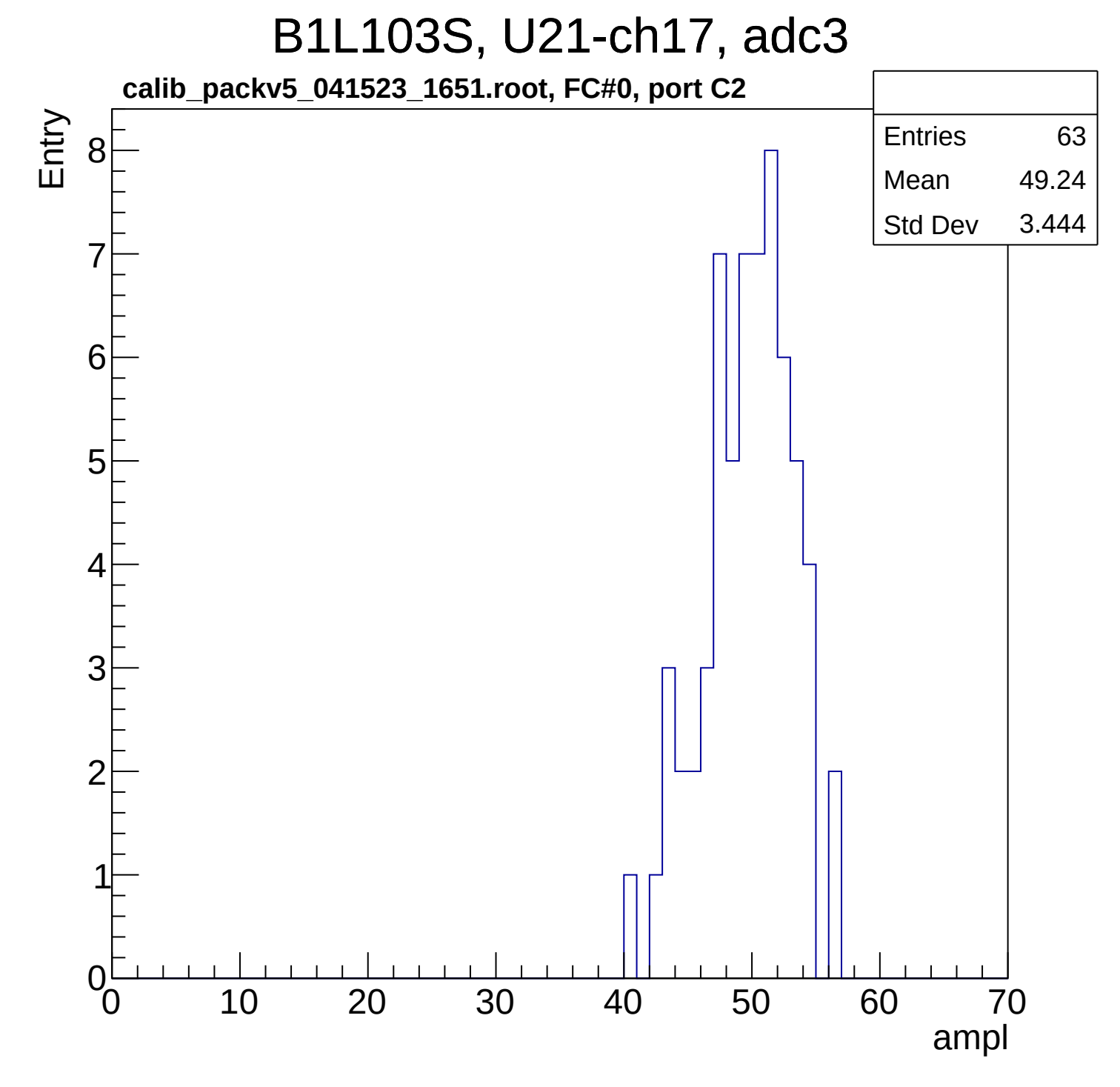

B1L103S, U21-ch16, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.33
Std Dev 1.374
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch16, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 6
Std Dev 18.49
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch17, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 23.73
Std Dev 10.7
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch17, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 34.68
Std Dev 5.126
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch17, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 37.35
Std Dev 14.65
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch17, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 49.24
Std Dev 3.444
Entry
ampl
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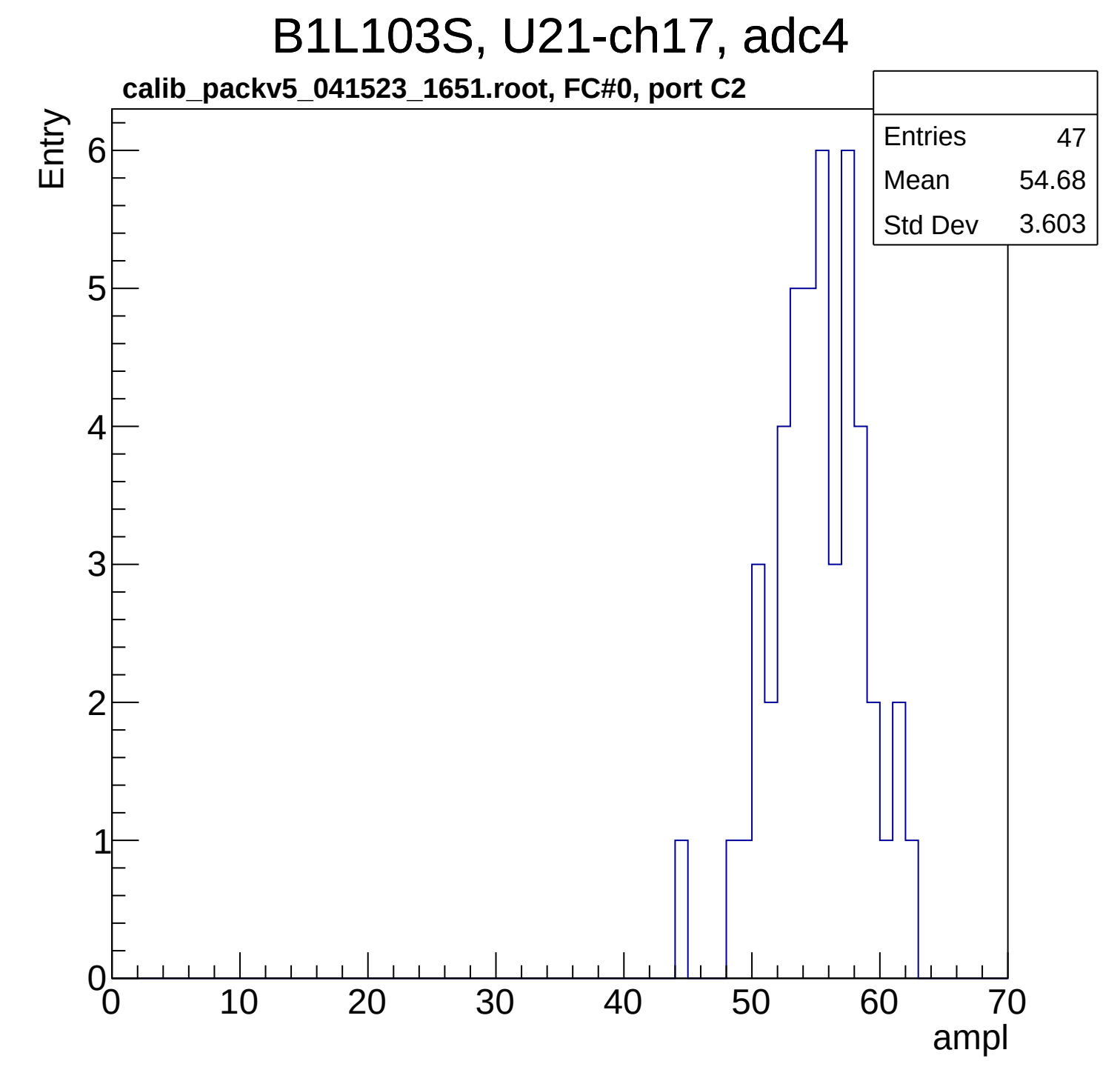
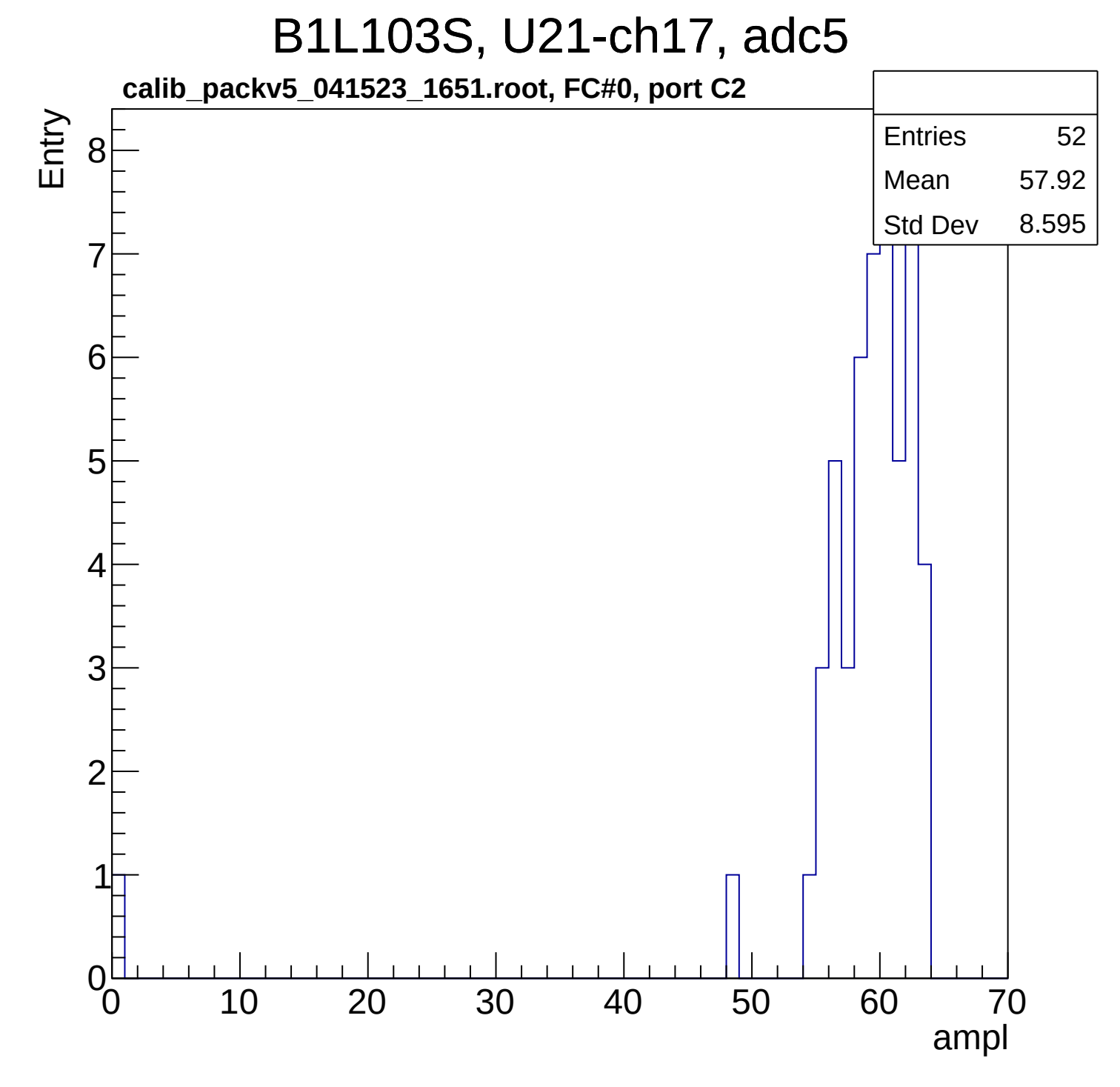
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch17, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 54.68
Std Dev 3.603
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U21-ch17, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 57.92
Std Dev 8.595
Entry
ampl
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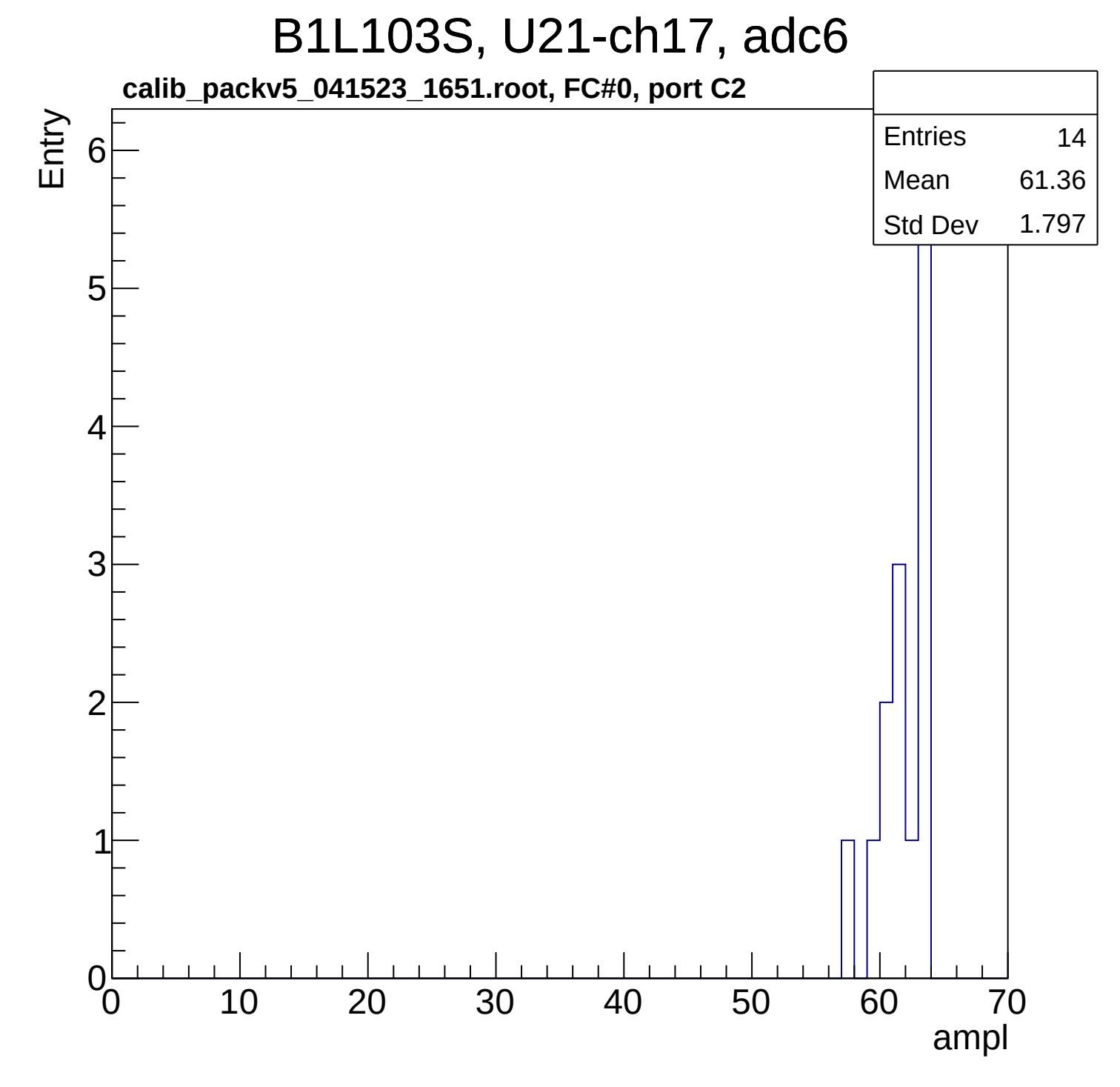
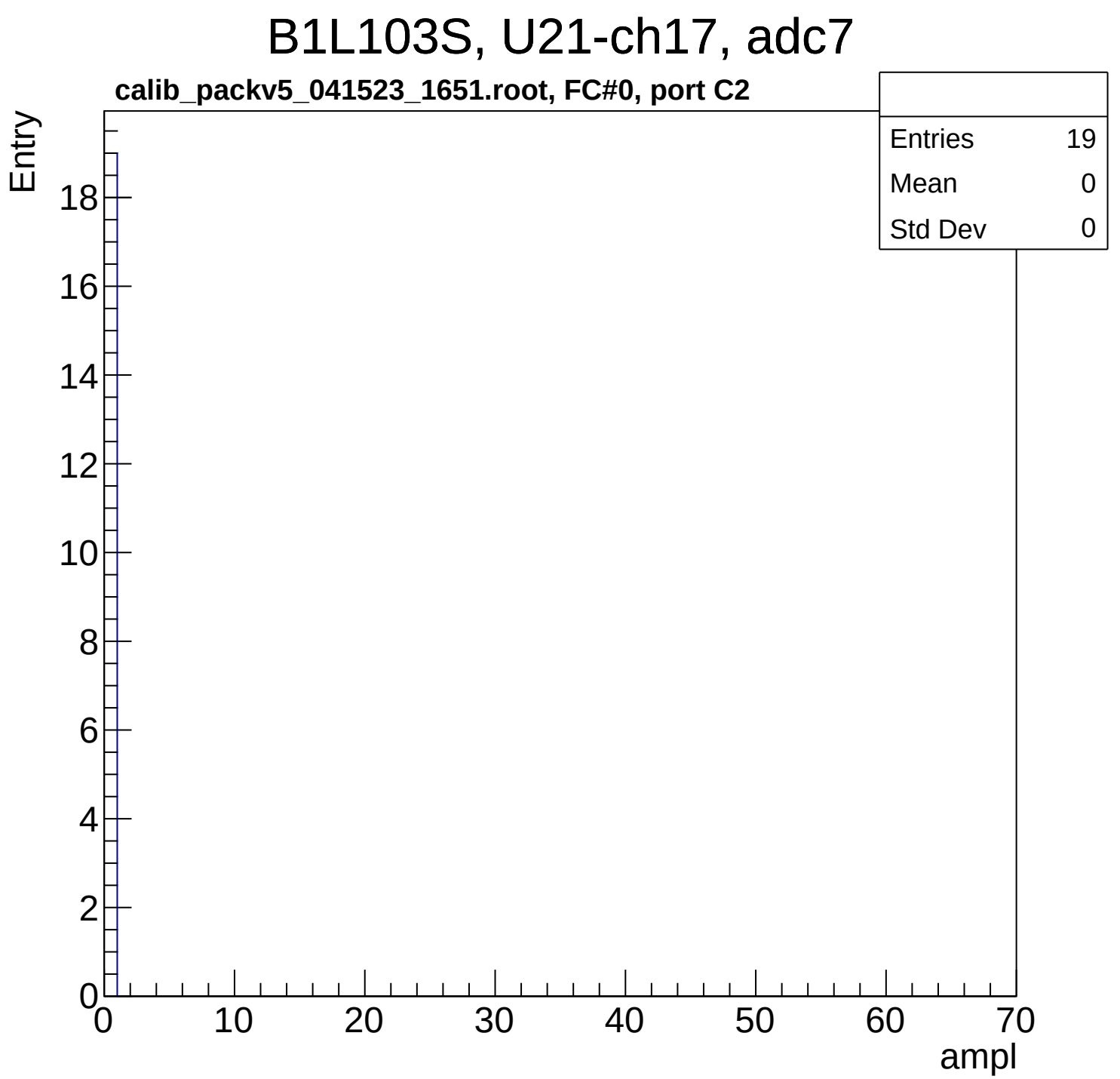
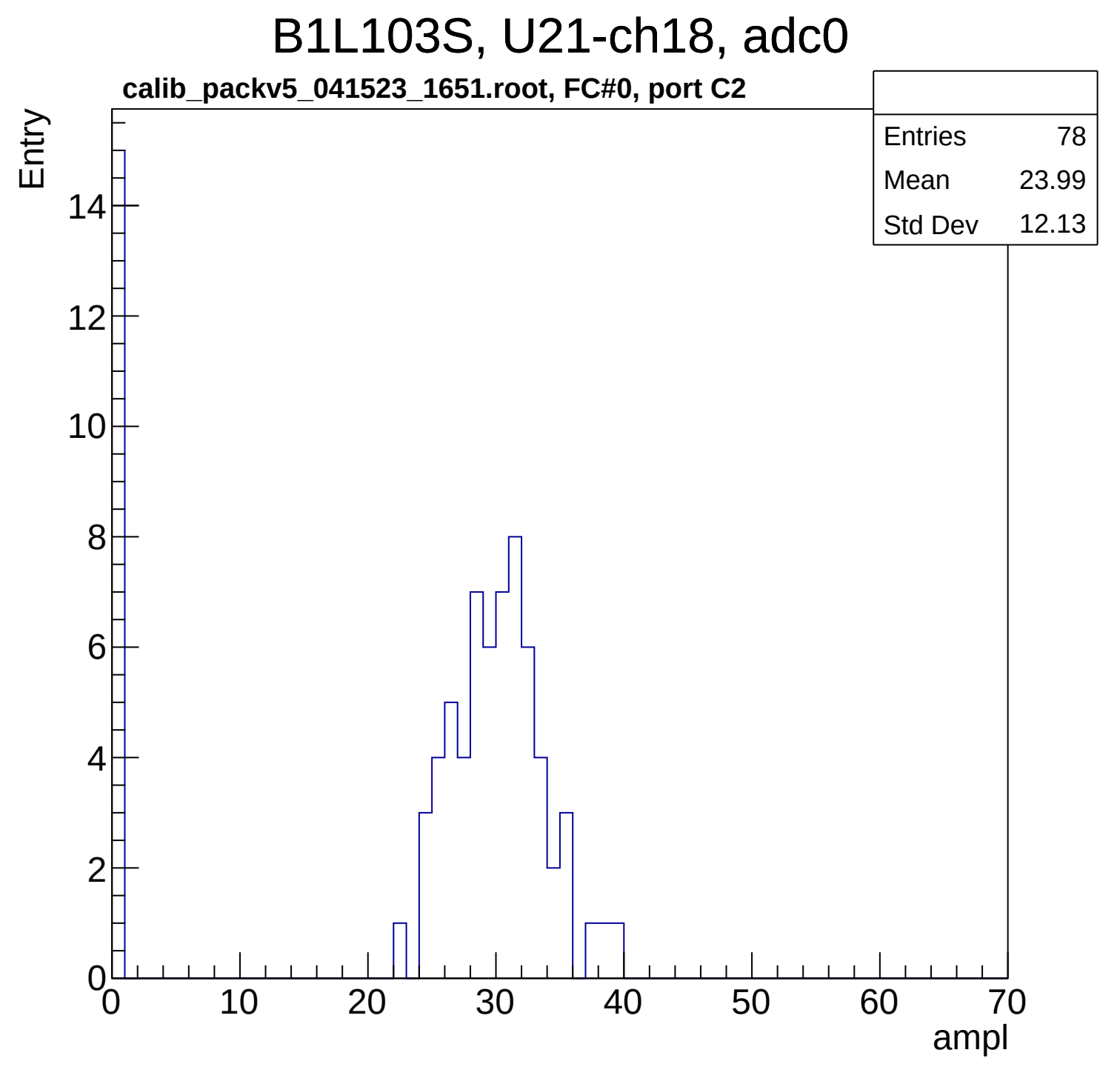
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch17, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 61.36
Std Dev 1.797
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U21-ch17, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch18, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 23.99
Std Dev 12.13
Entry
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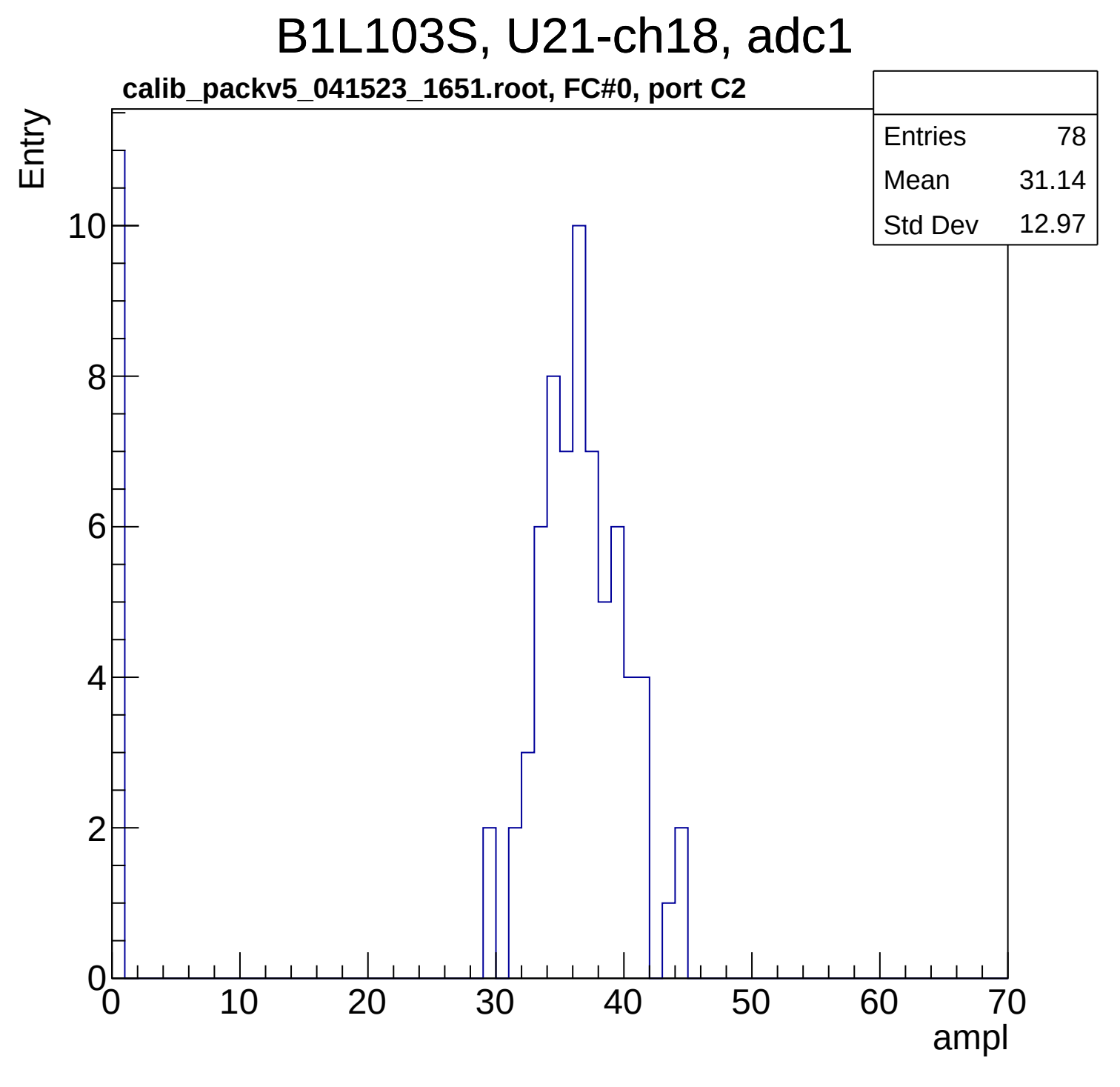
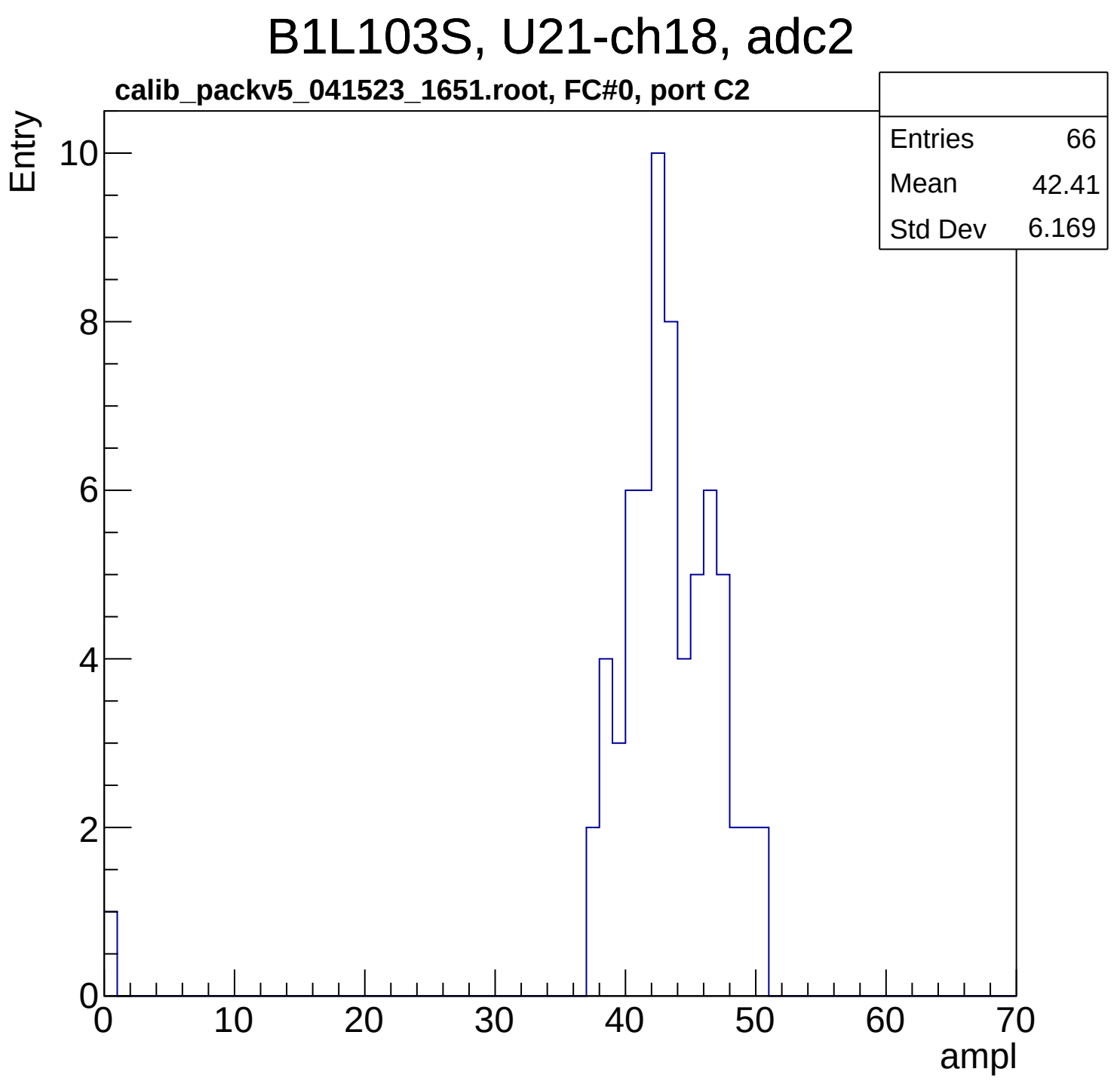
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch18, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 31.14
Std Dev 12.97
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch18, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 42.41
Std Dev 6.169
Entry
ampl
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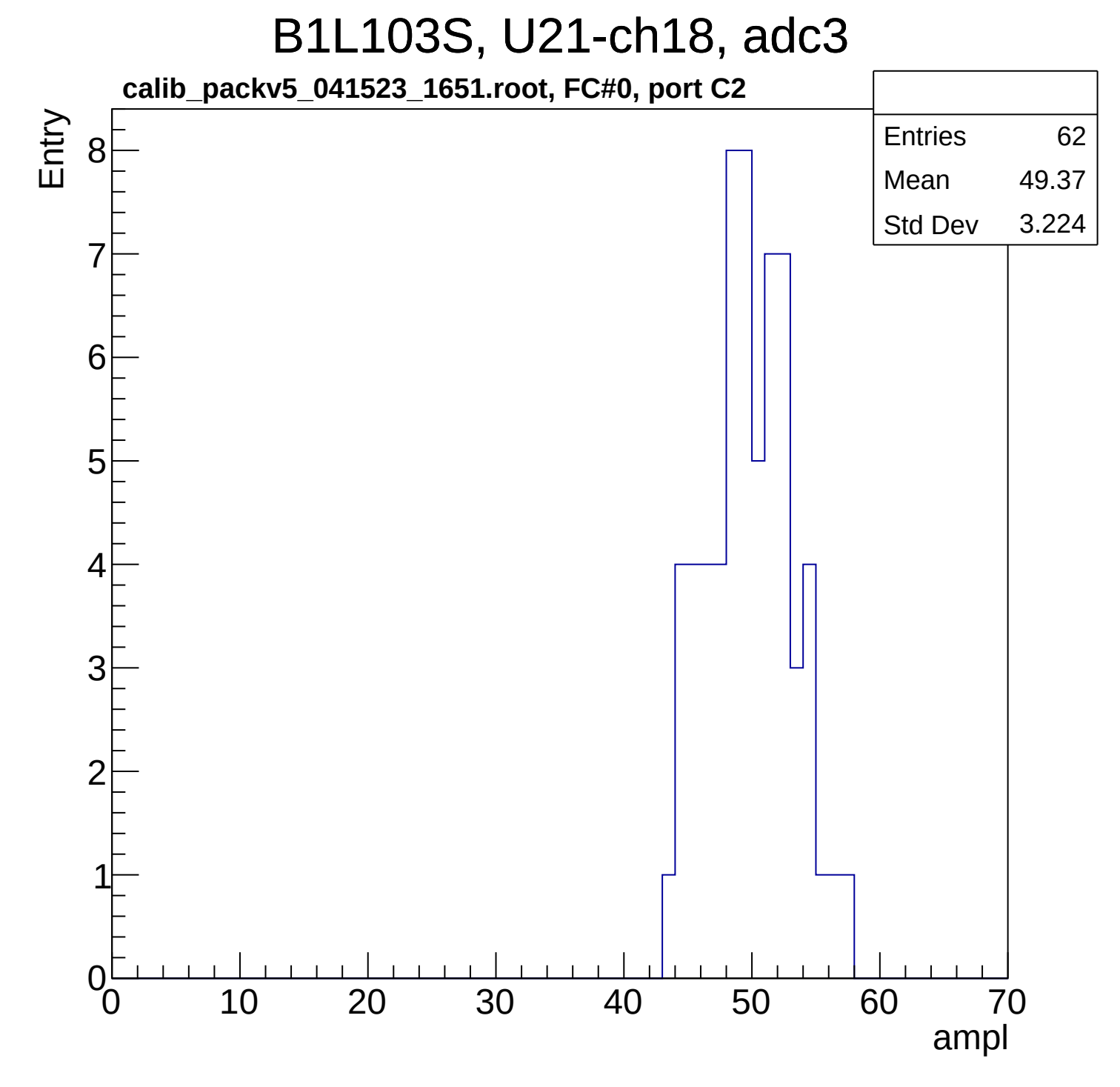
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U21-ch18, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 49.37
Std Dev 3.224
Entry
ampl
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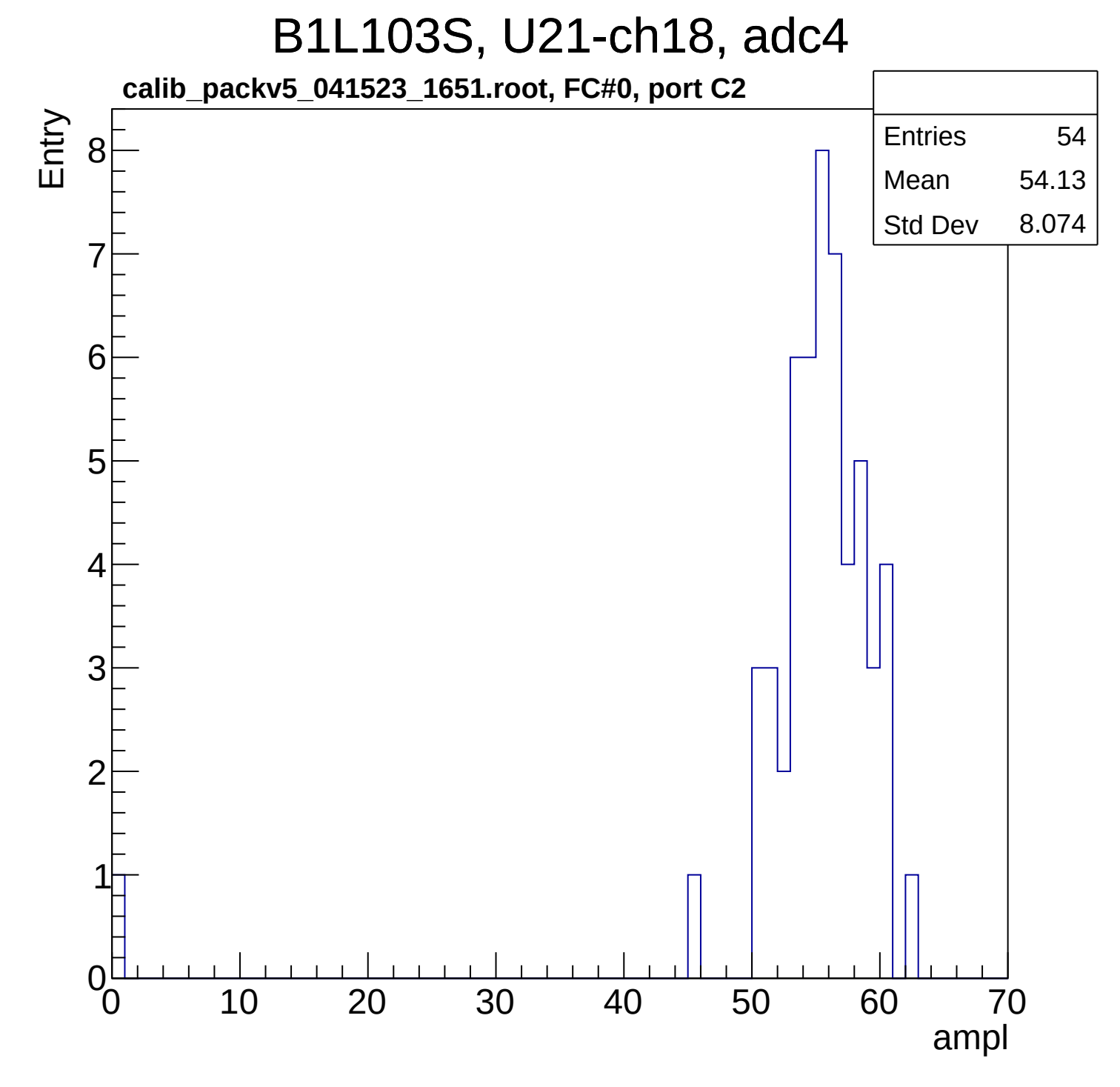
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch18, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 54.13
Std Dev 8.074
Entry
ampl
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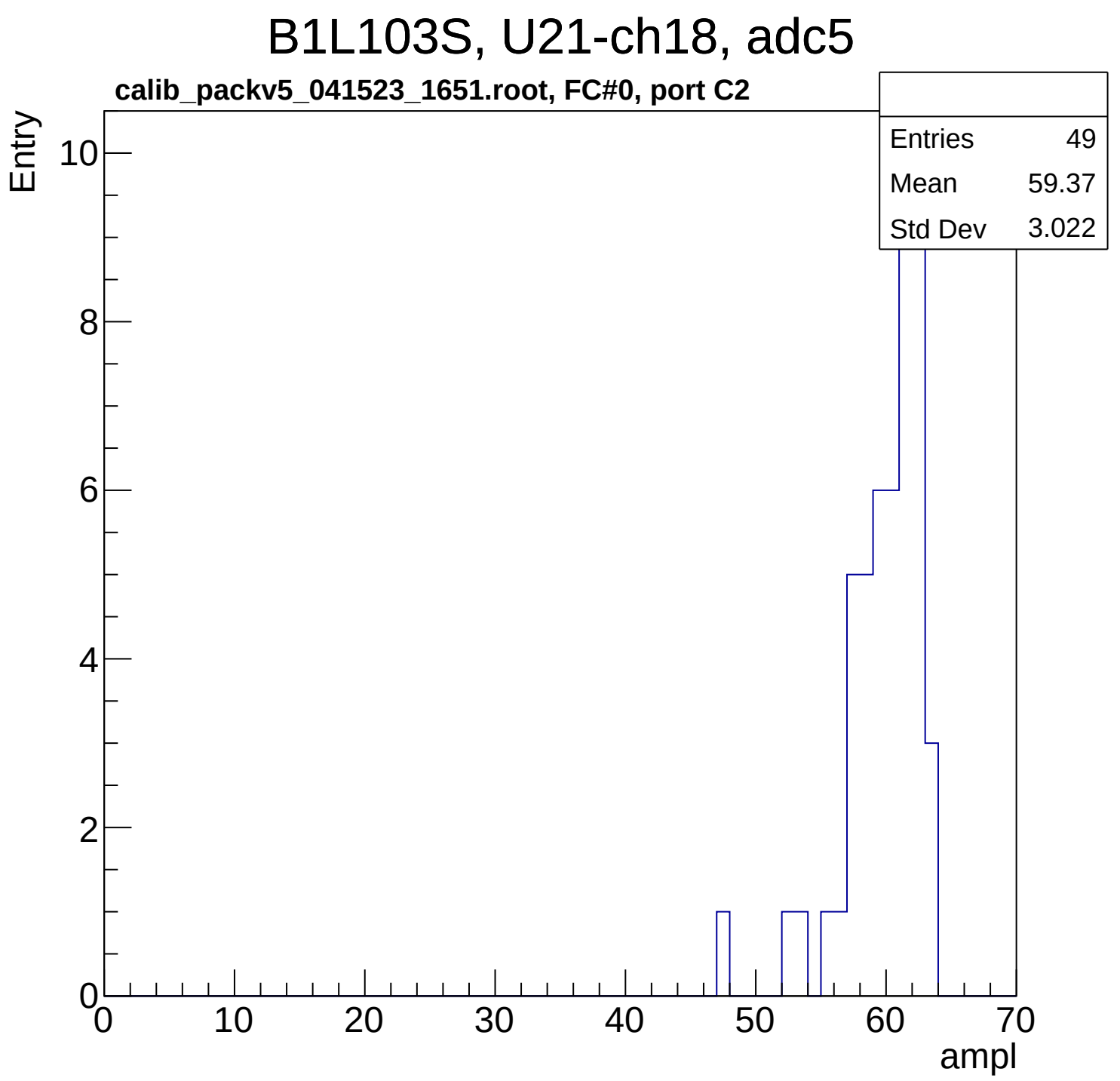
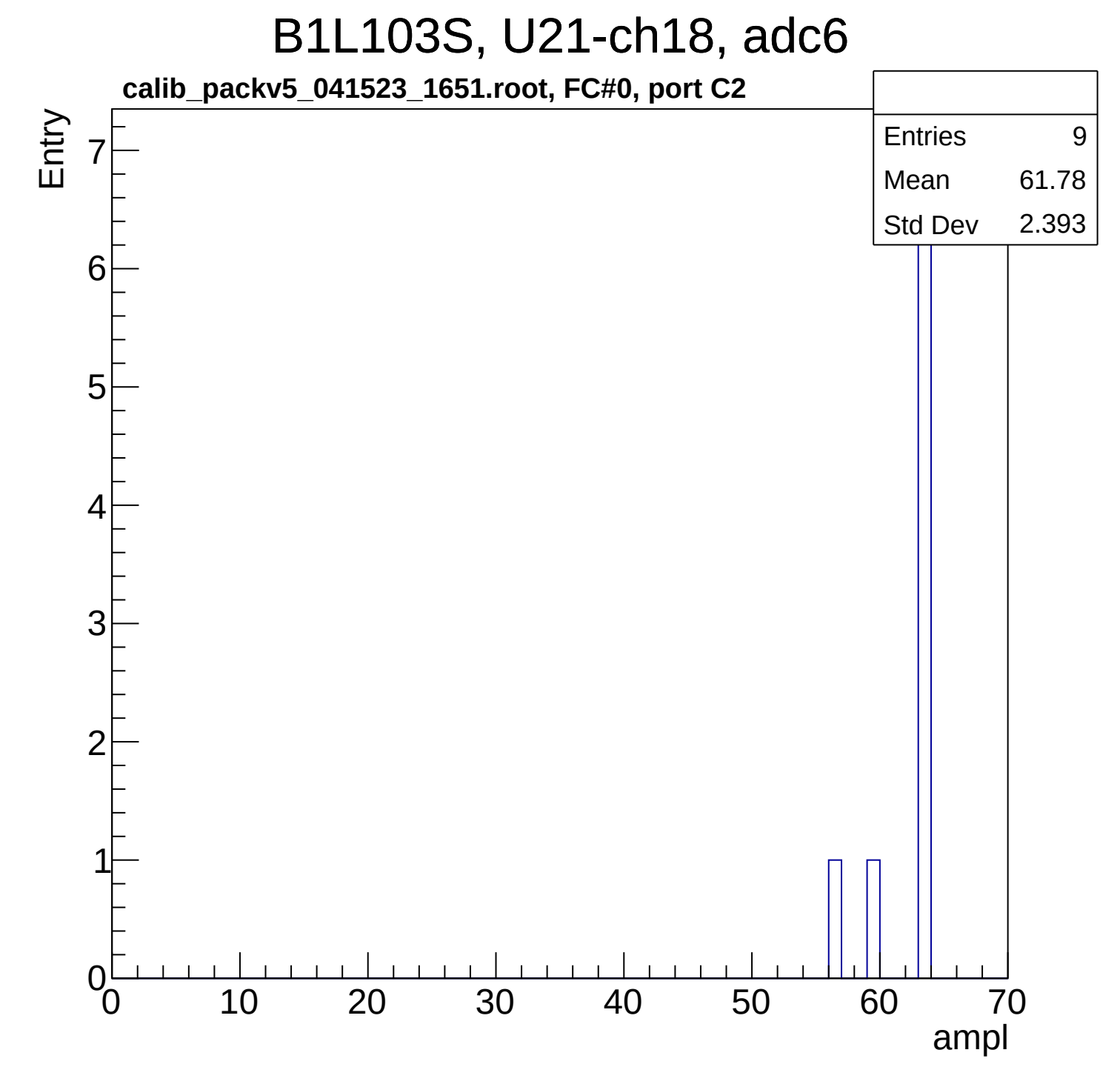
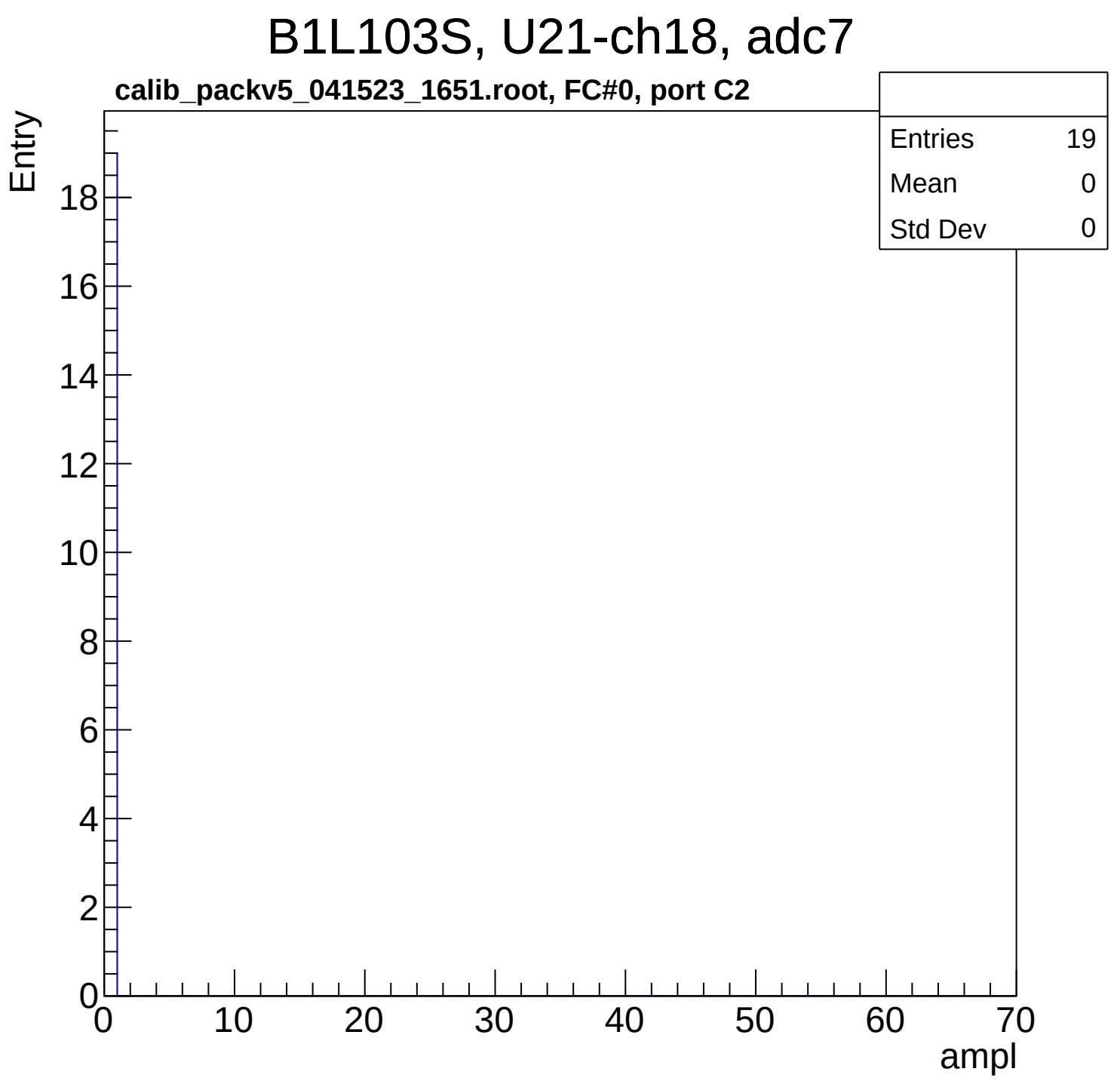
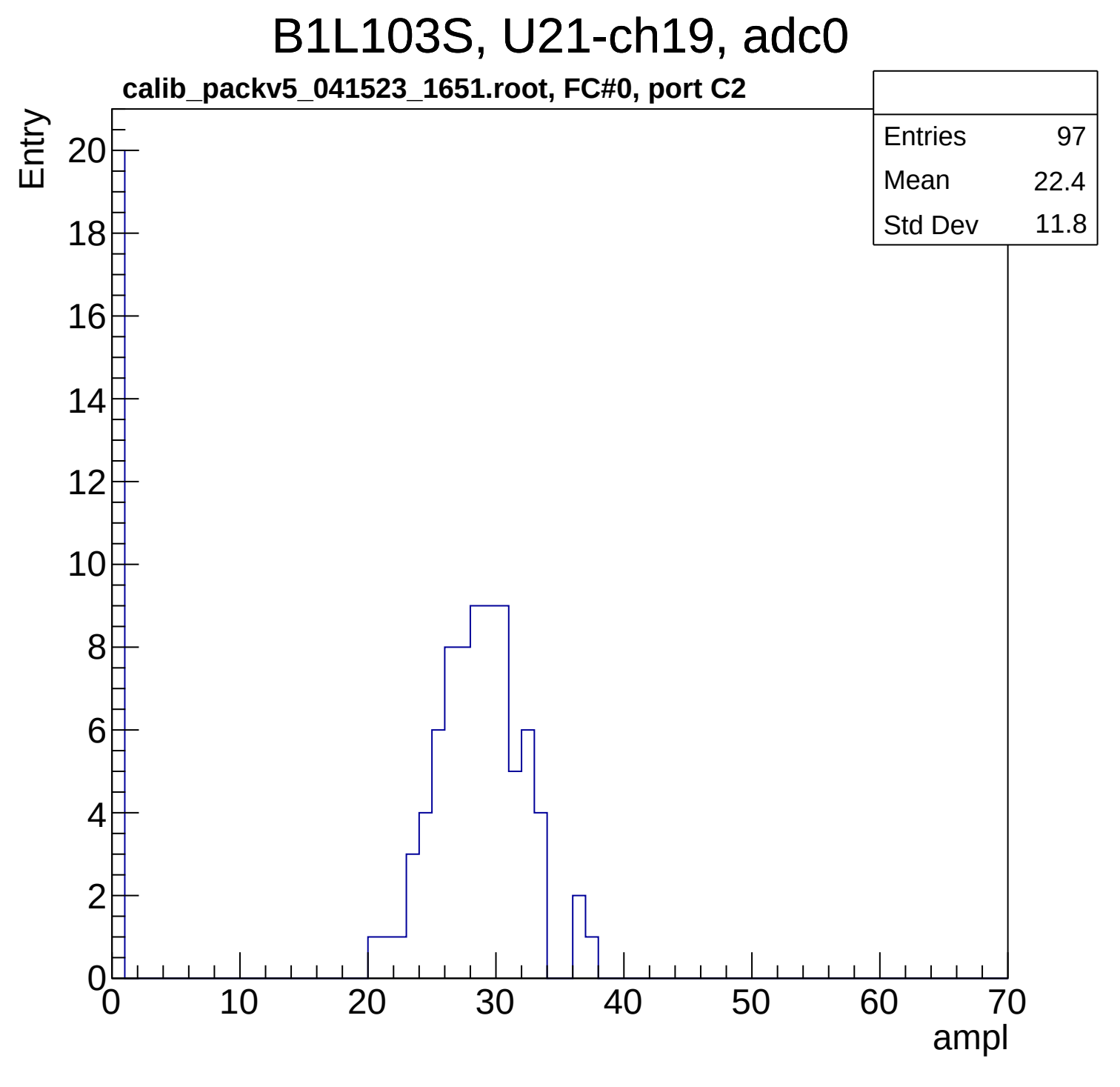
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch18, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 59.37
Std Dev 3.022
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch18, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 61.78
Std Dev 2.393
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U21-ch18, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch19, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 22.4
Std Dev 11.8
Entry
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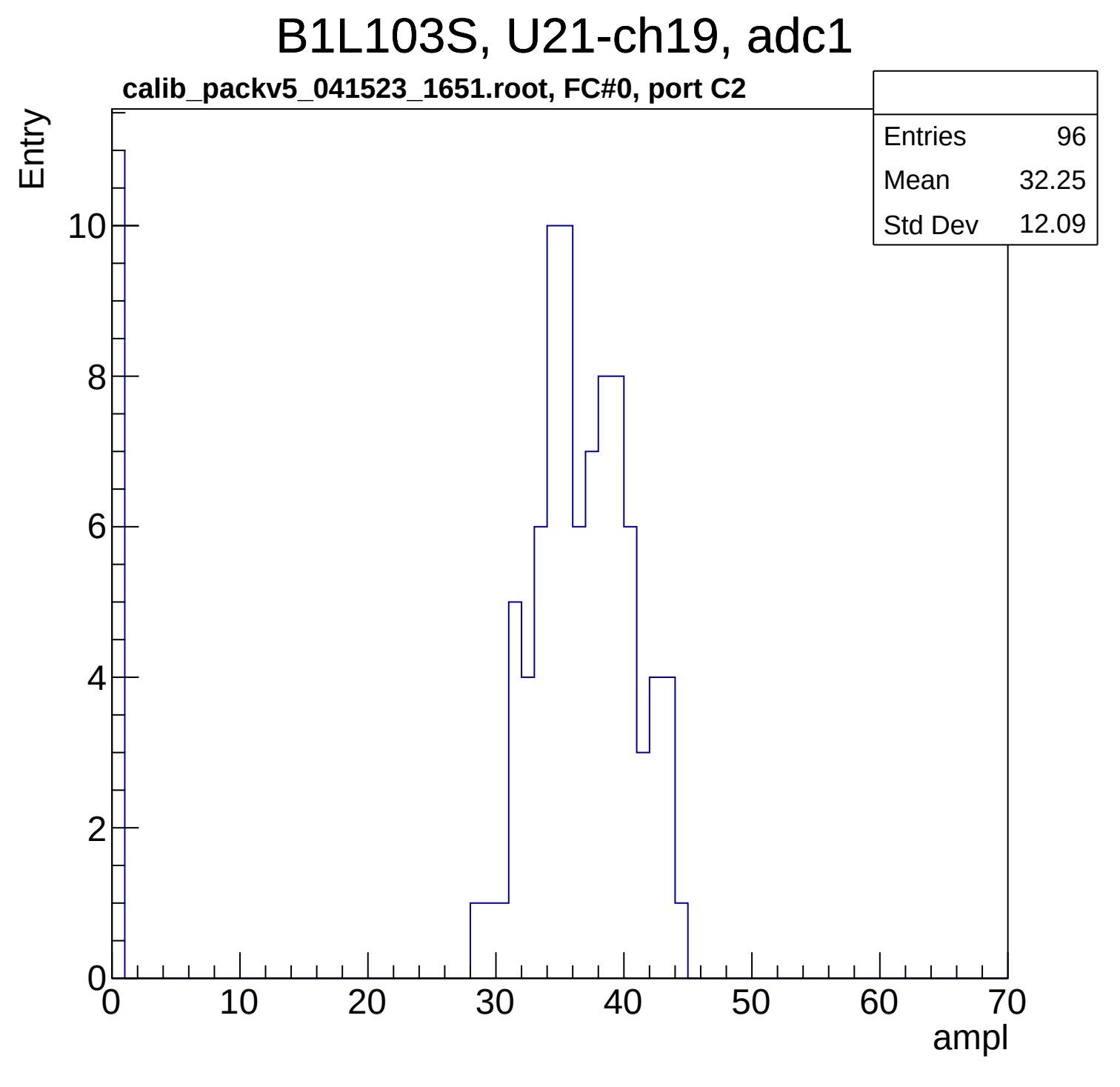
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch19, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 96
Mean 32.25
Std Dev 12.09
Entry
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6
8
10
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10
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30
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50
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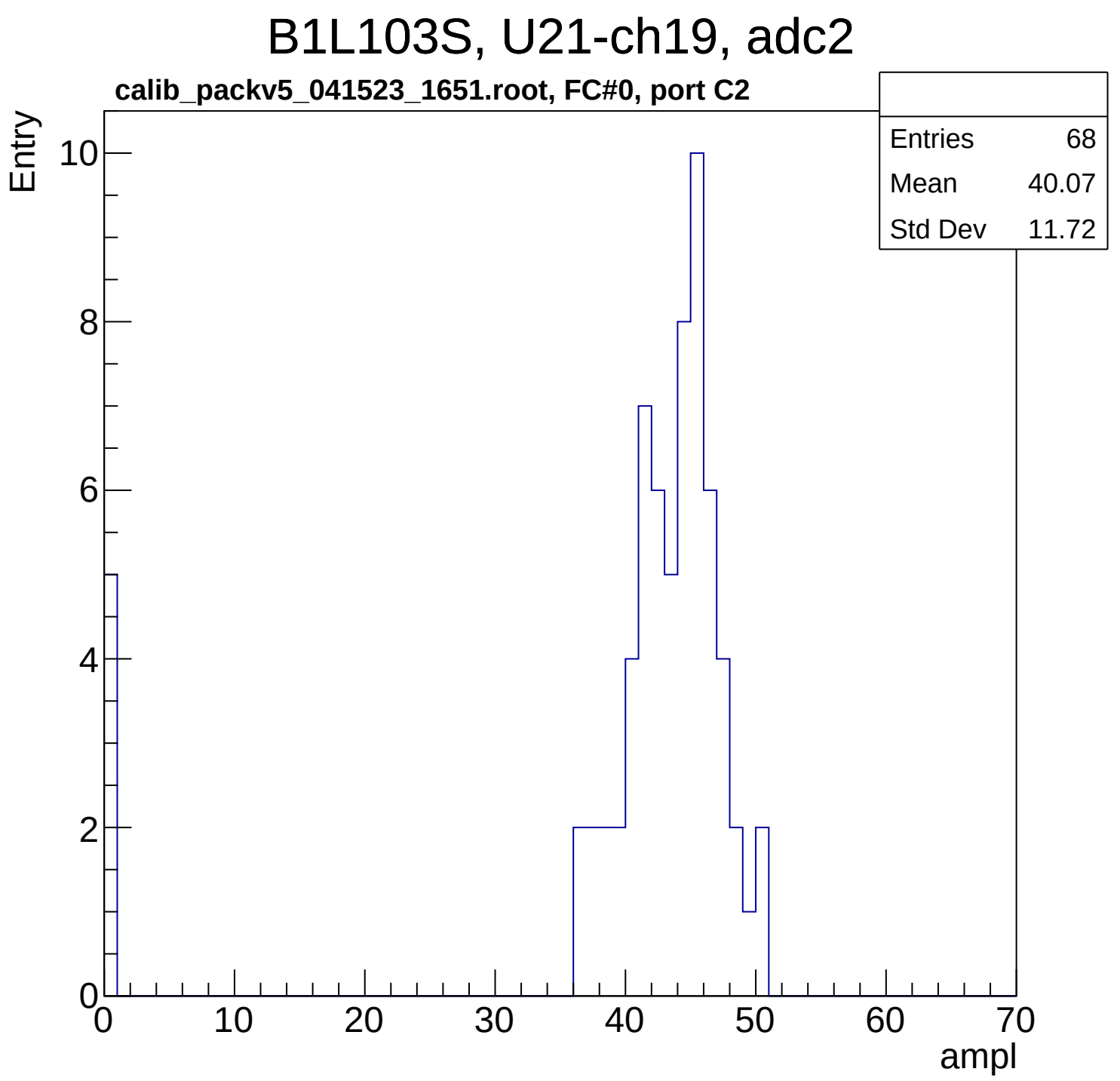
70
ampl


B1L103S, U21-ch19, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 40.07
Std Dev 11.72
Entry
ampl
0
2
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6
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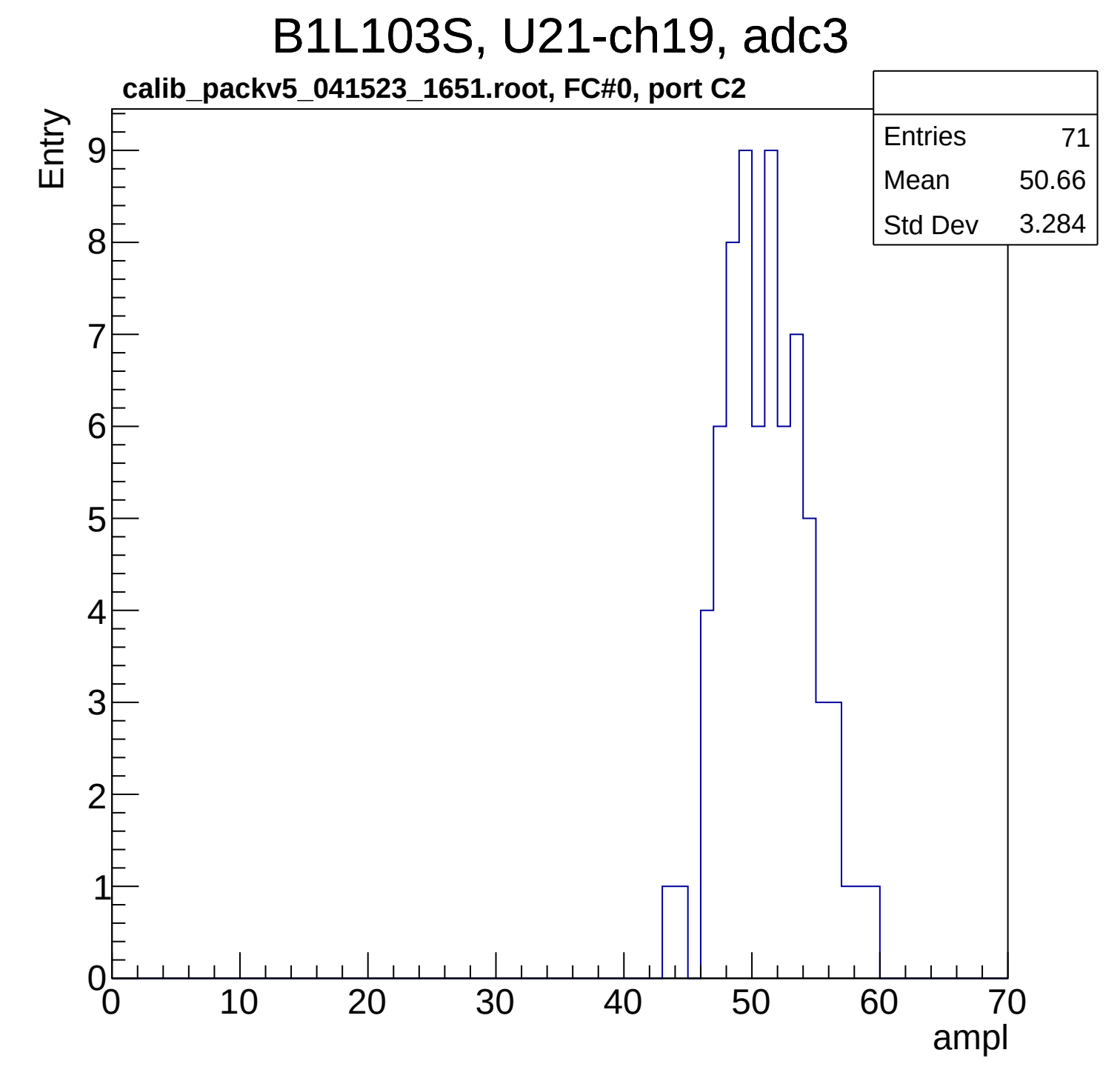
10
0
10
20
30
40
50
60
70


B1L103S, U21-ch19, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 50.66
Std Dev 3.284
Entry
ampl
0
1
2
3
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6
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8
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0
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40
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60
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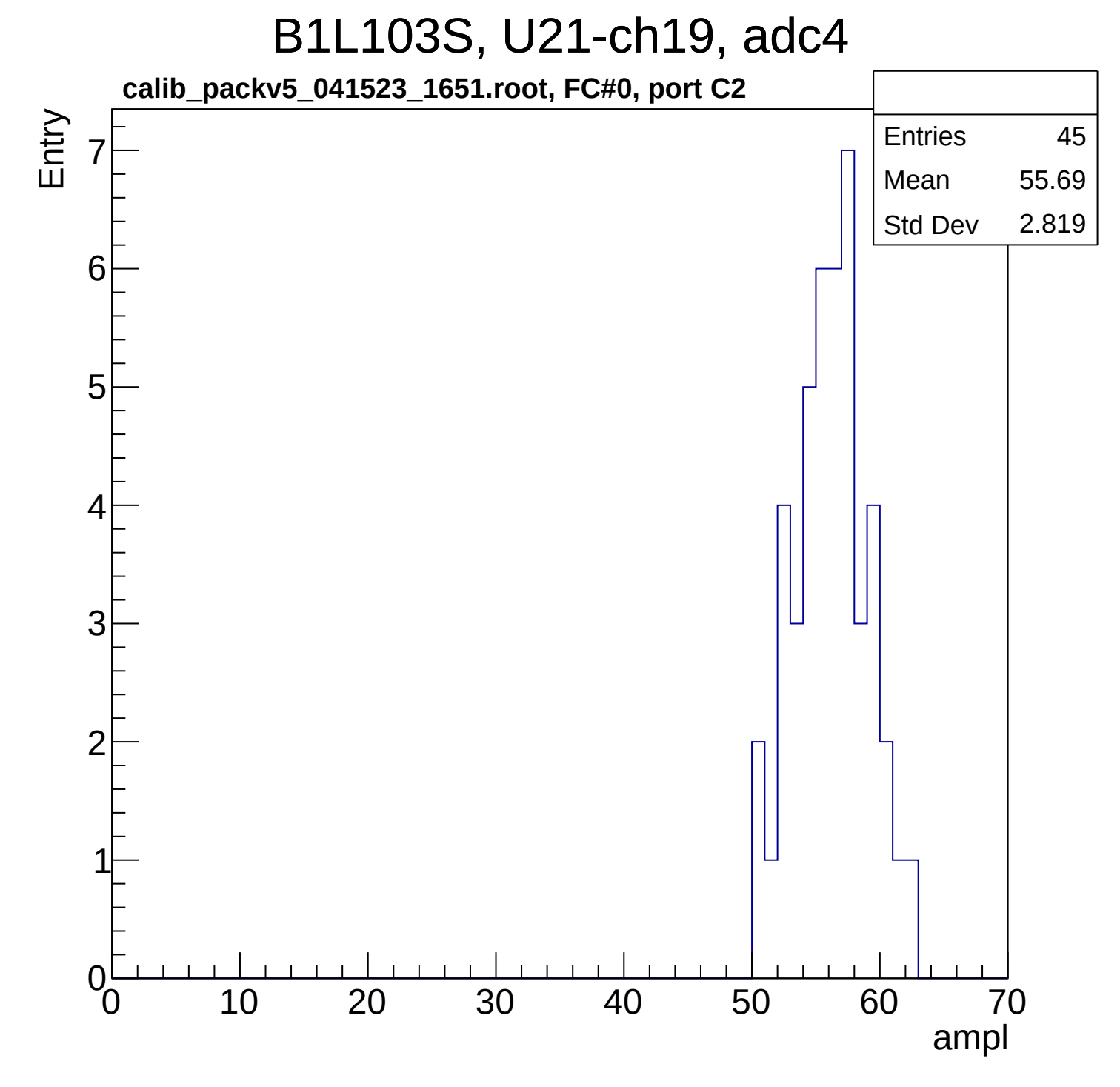
B1L103S, U21-ch19, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 55.69
Std Dev 2.819
Entry
ampl
0
1
2
3
4
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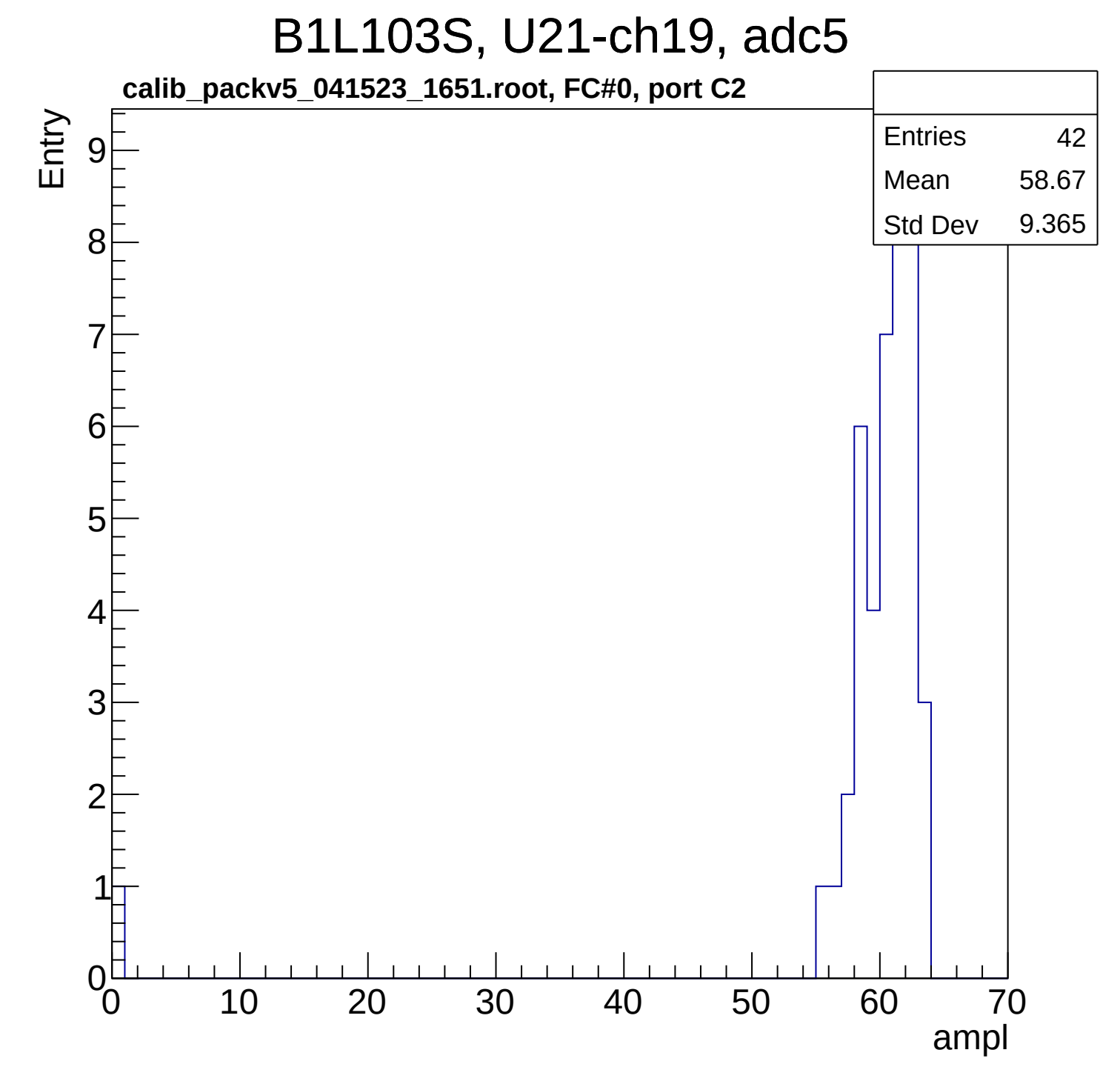
B1L103S, U21-ch19, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 58.67
Std Dev 9.365
Entry
ampl
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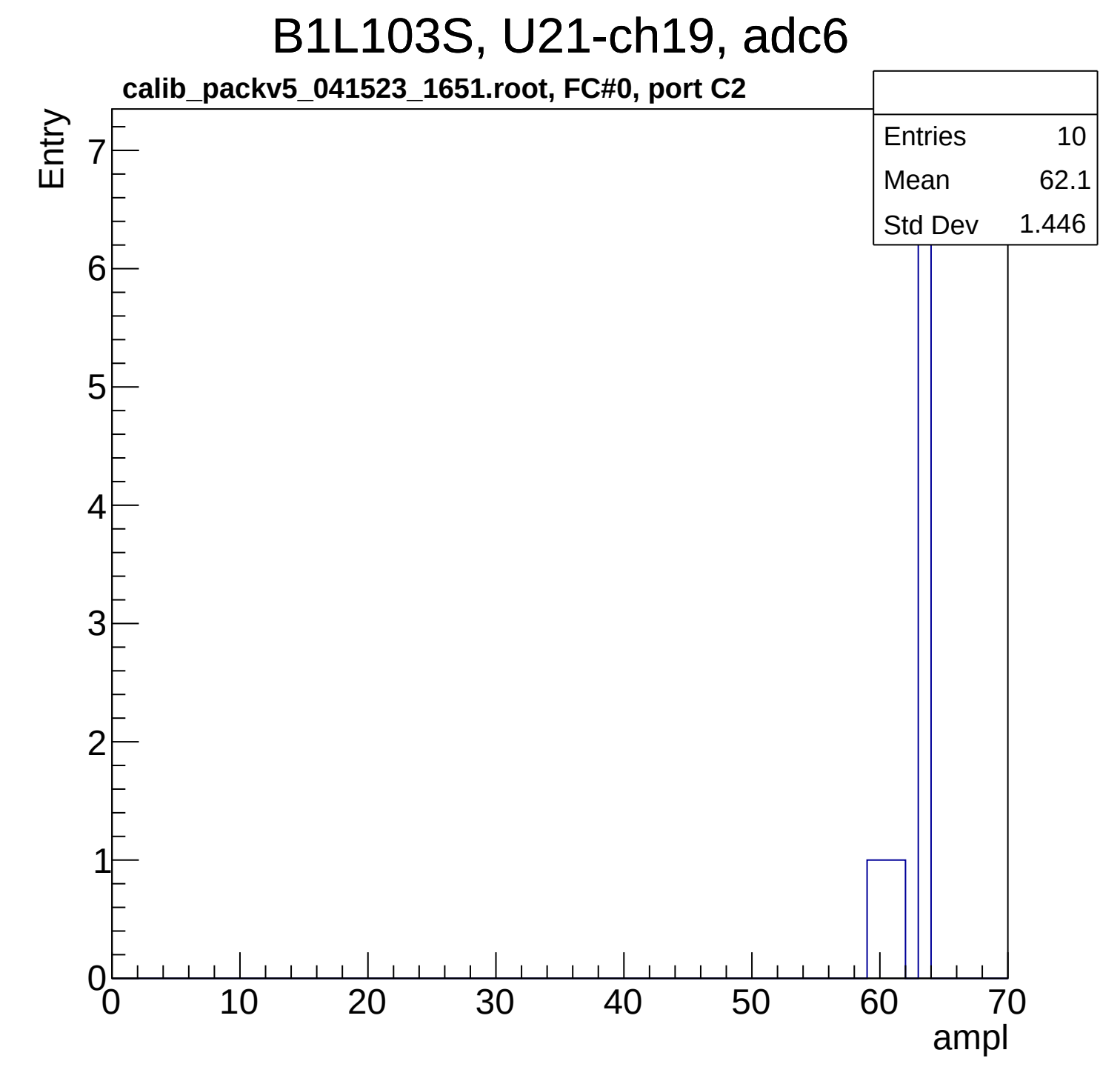
B1L103S, U21-ch19, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 62.1
Std Dev 1.446
Entry
ampl
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1
2
3
4
5
6
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0
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40
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60
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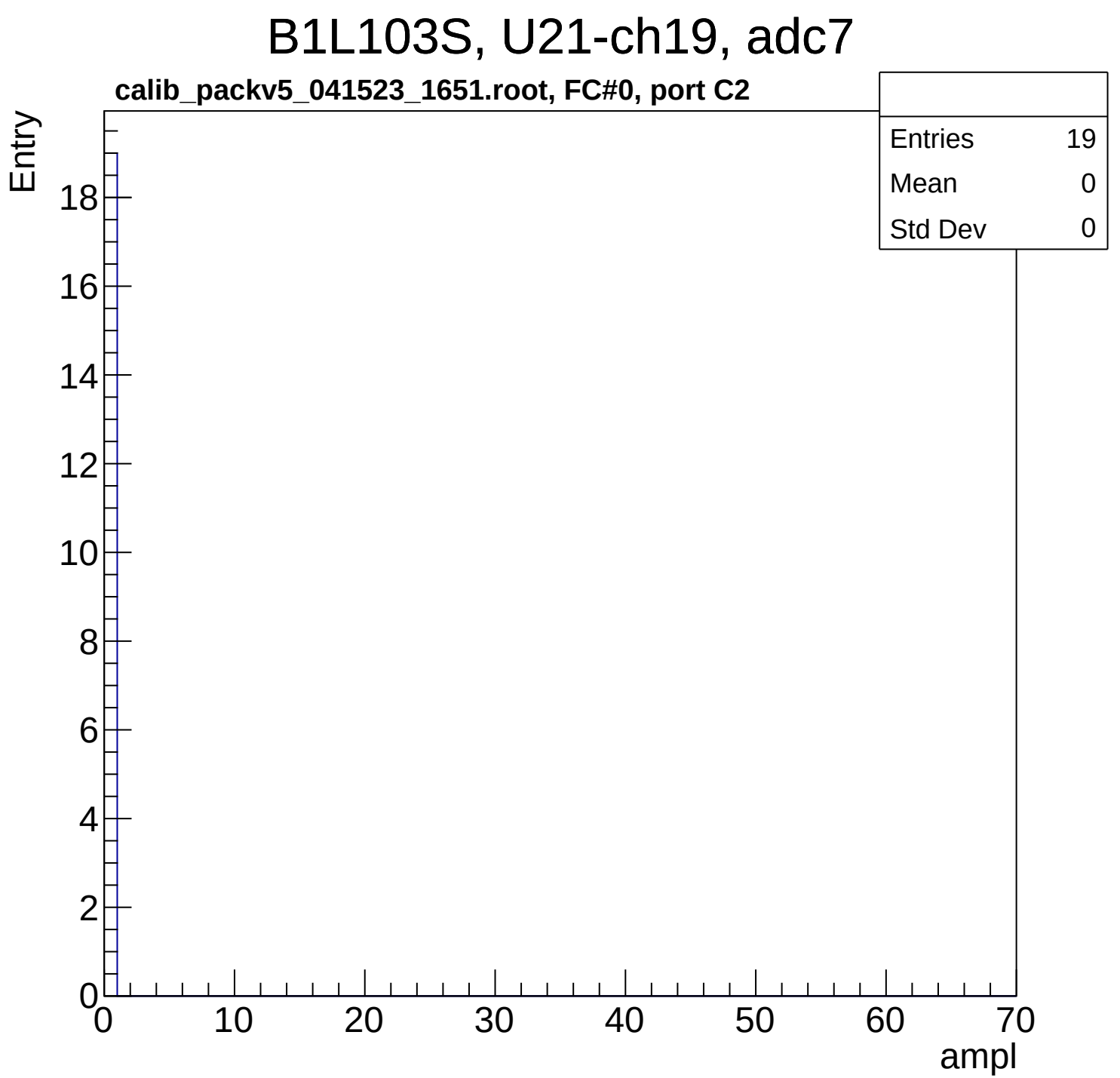
B1L103S, U21-ch19, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
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10
20
30
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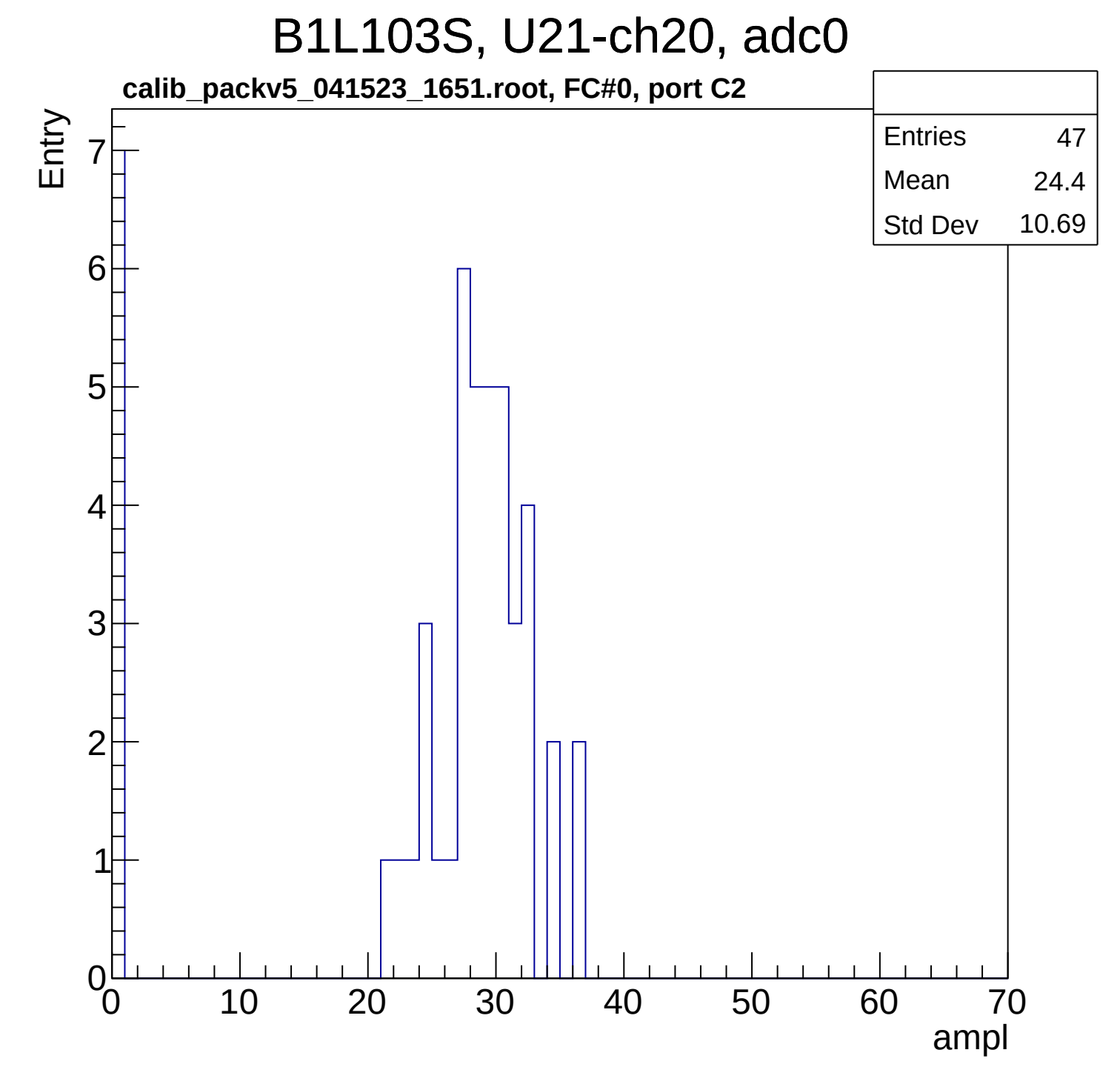
50
60
70
ampl


B1L103S, U21-ch20, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 24.4
Std Dev 10.69
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
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40
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60
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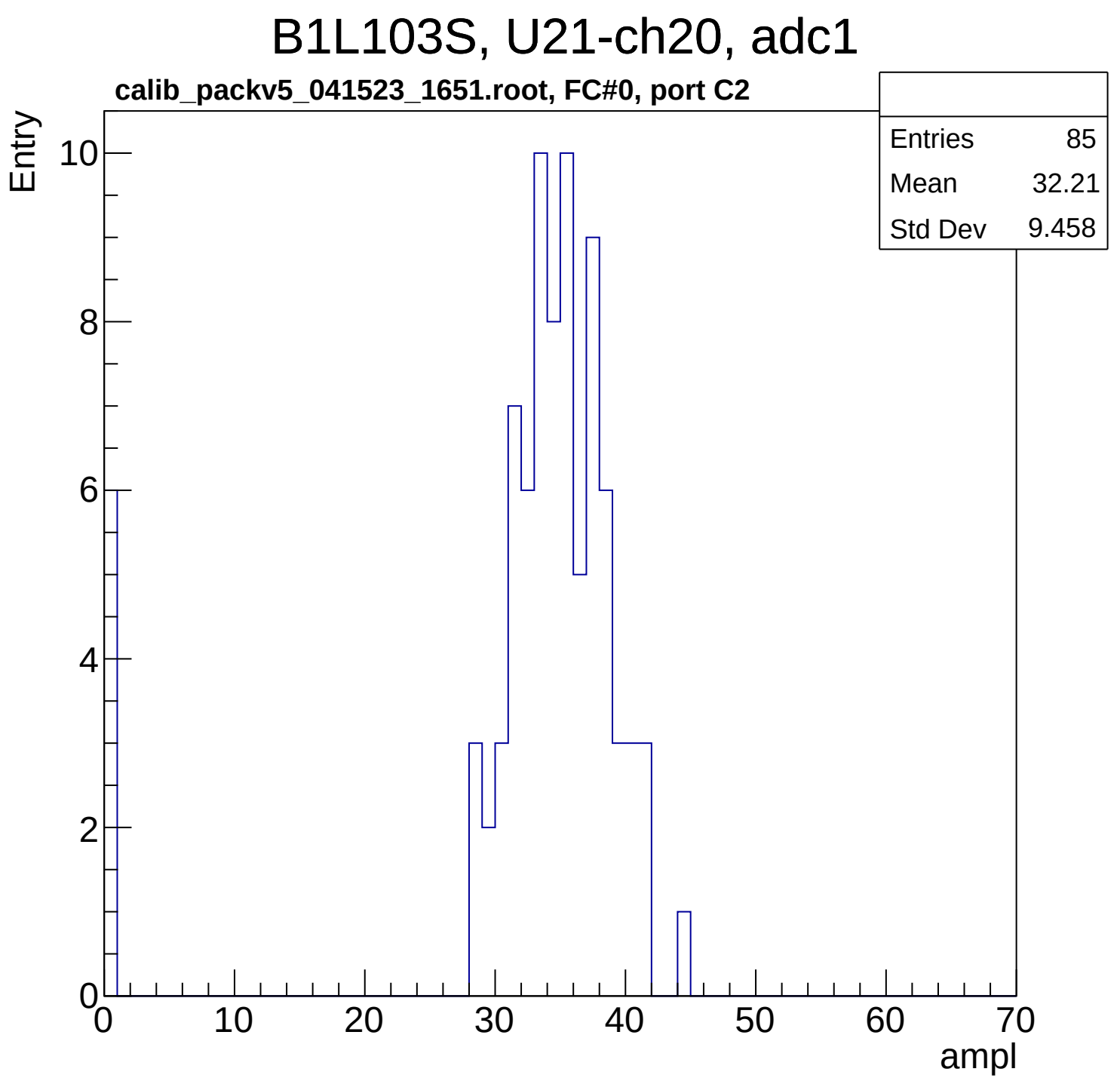
B1L103S, U21-ch20, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 32.21
Std Dev 9.458
Entry
ampl
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4
6
8
10
0
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40
50
60
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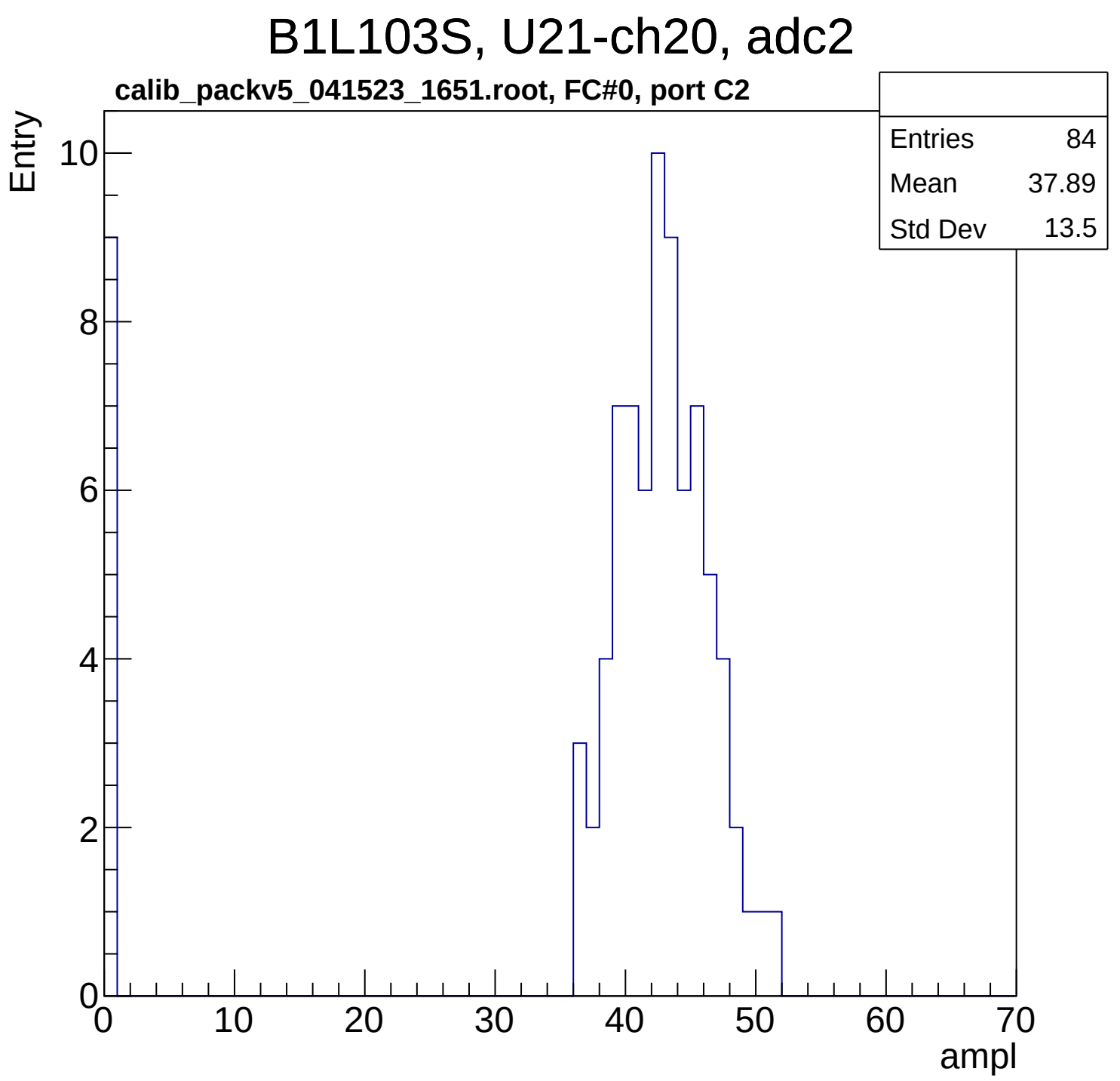
B1L103S, U21-ch20, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 37.89
Std Dev 13.5
Entry
ampl
0
2
4
6
8
10
0
10
20
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40
50
60
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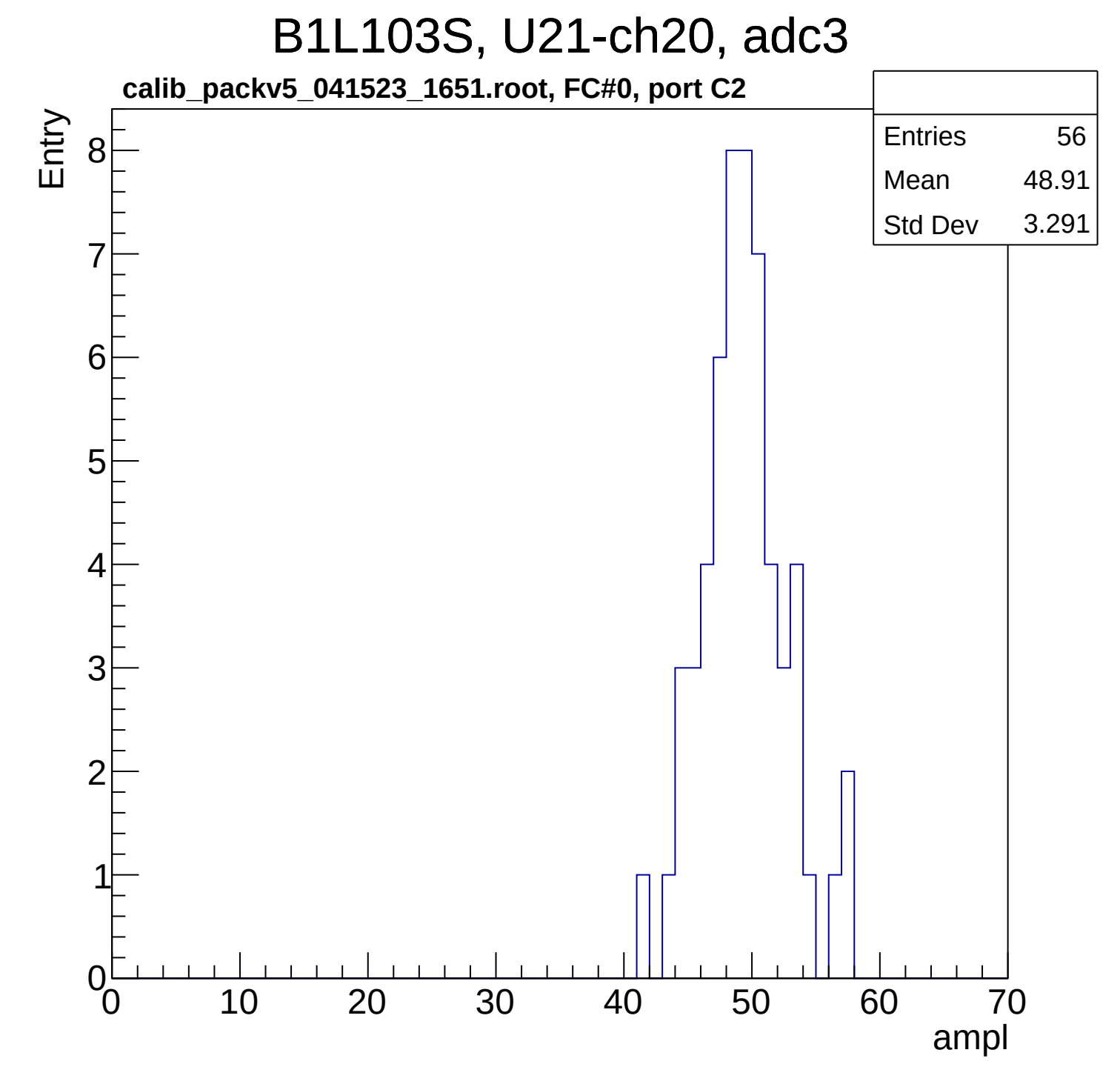
B1L103S, U21-ch20, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 48.91
Std Dev 3.291
Entry
ampl
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1
2
3
4
5
6
7
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0
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40
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60
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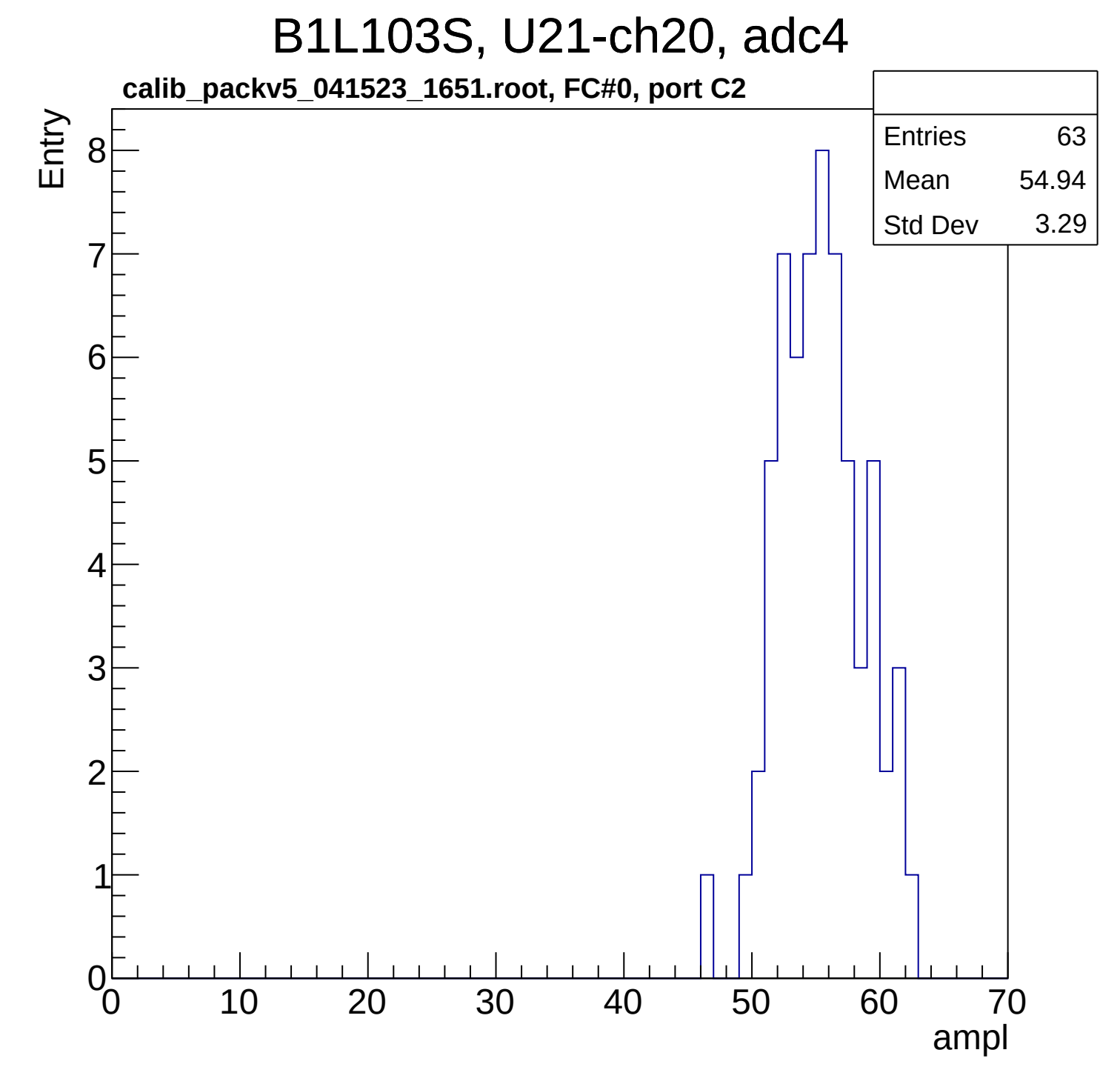
B1L103S, U21-ch20, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 54.94
Std Dev 3.29
Entry
ampl
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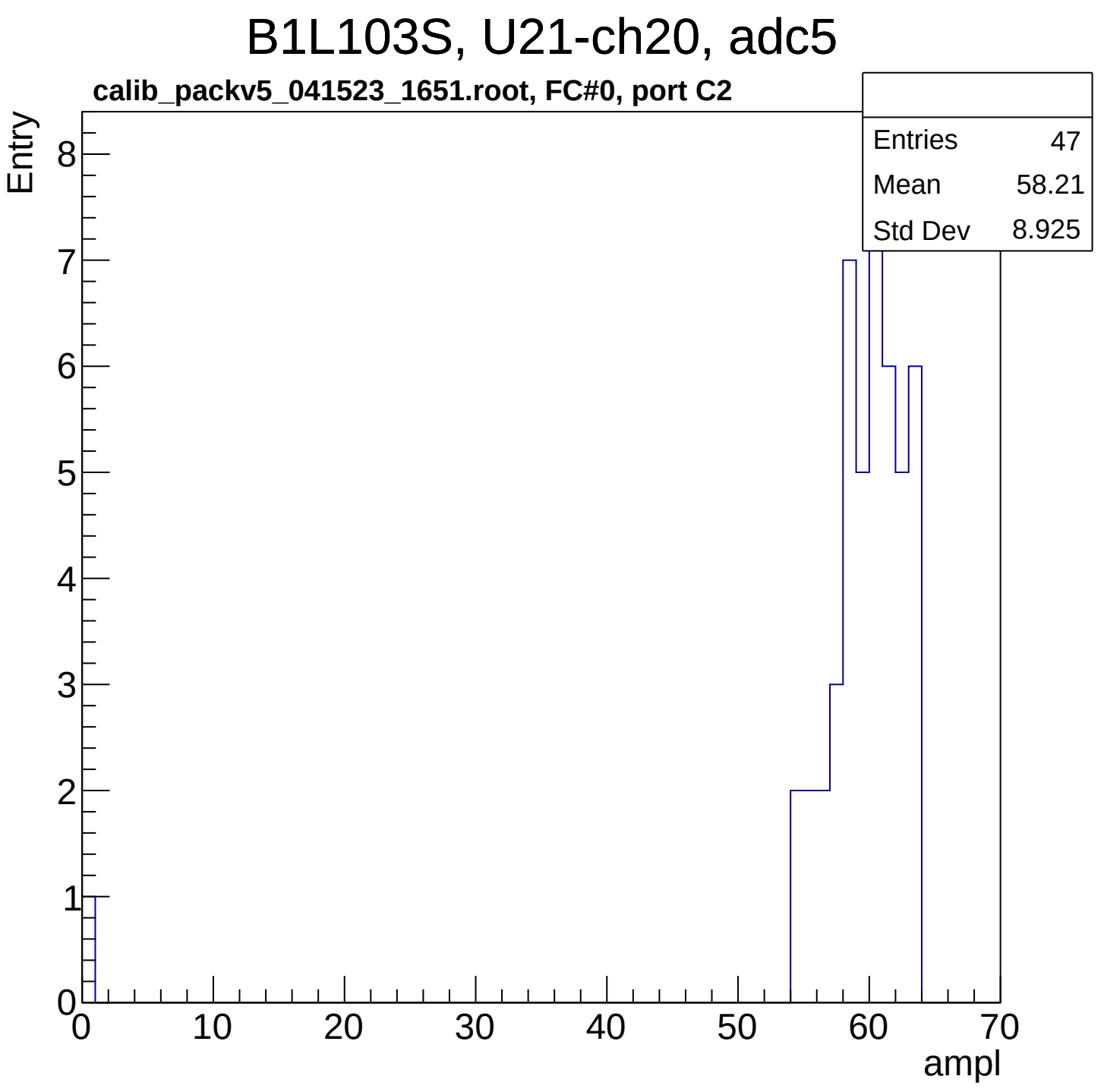
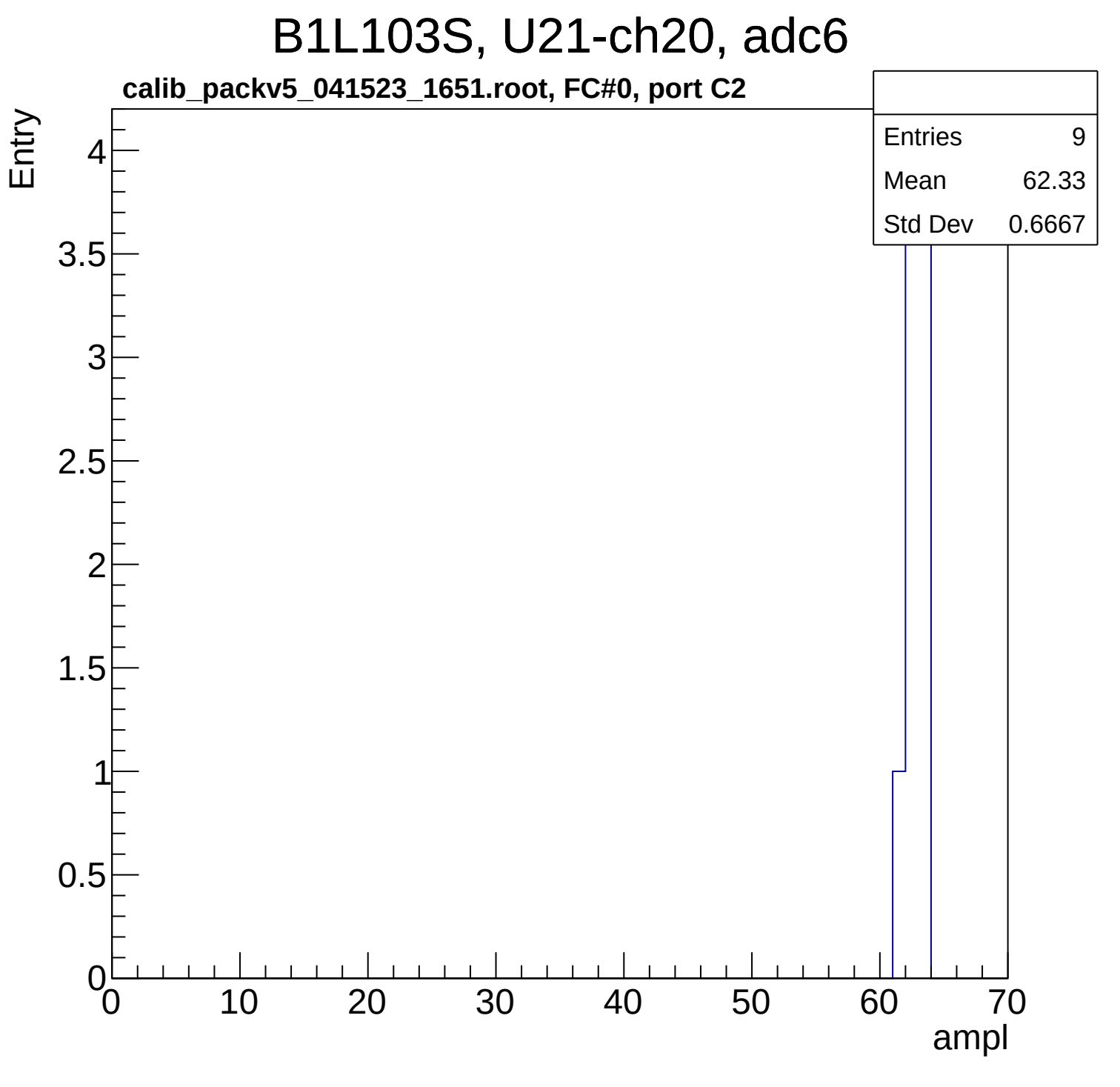
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch20, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 58.21
Std Dev 8.925
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch20, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 62.33
Std Dev 0.6667
Entry
ampl
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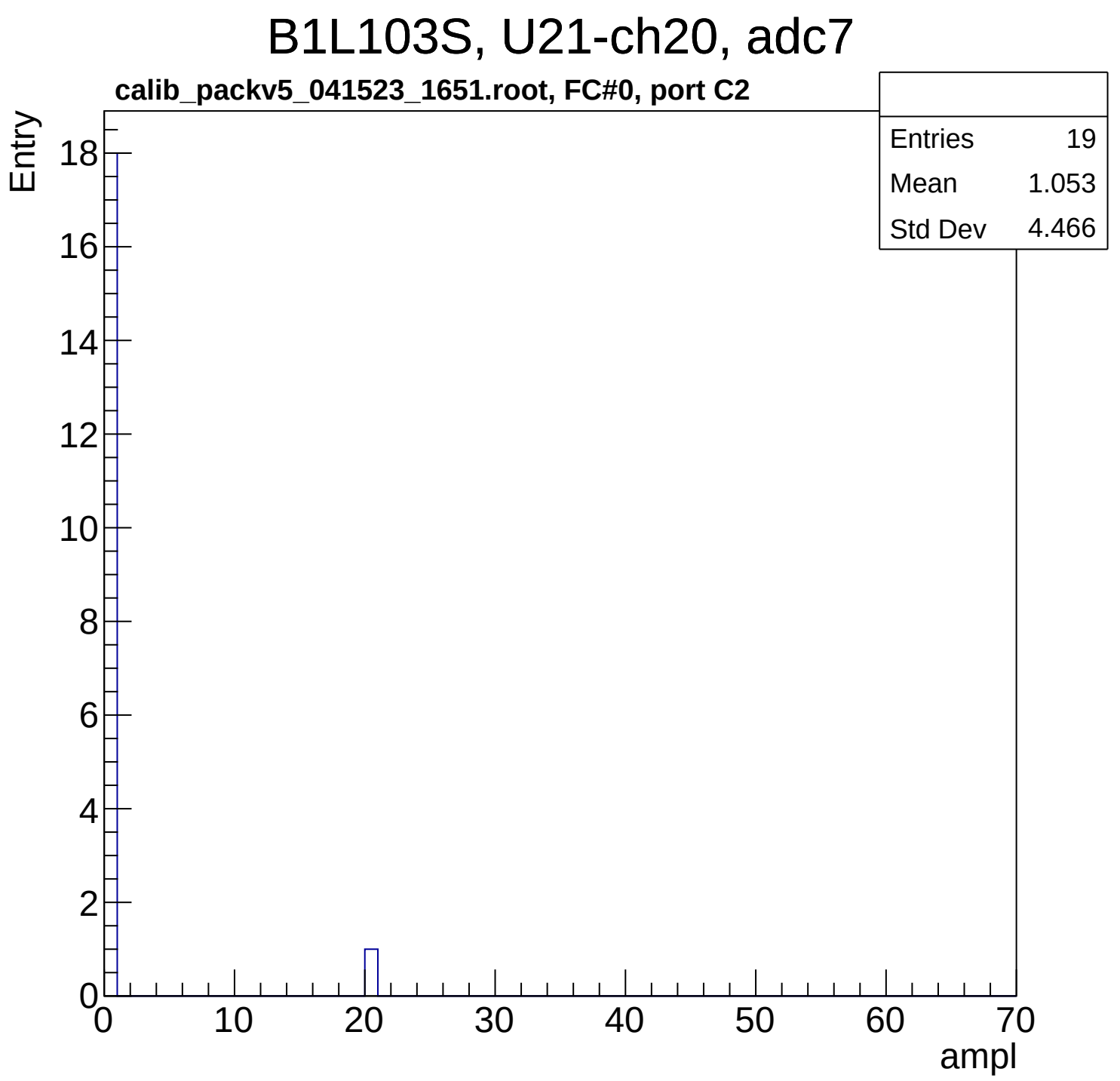
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U21-ch20, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.053
Std Dev 4.466
Entry
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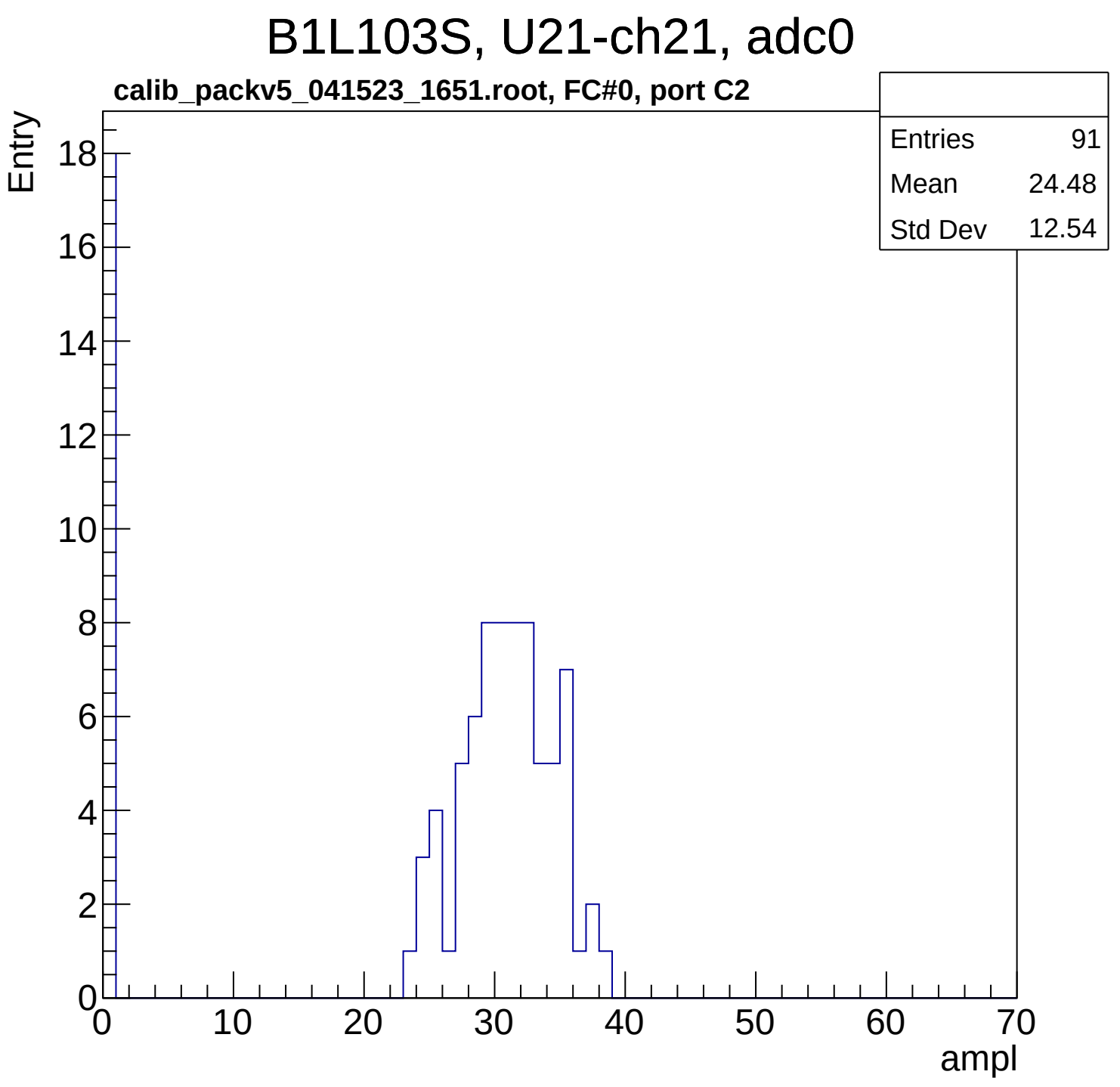
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch21, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 24.48
Std Dev 12.54
Entry
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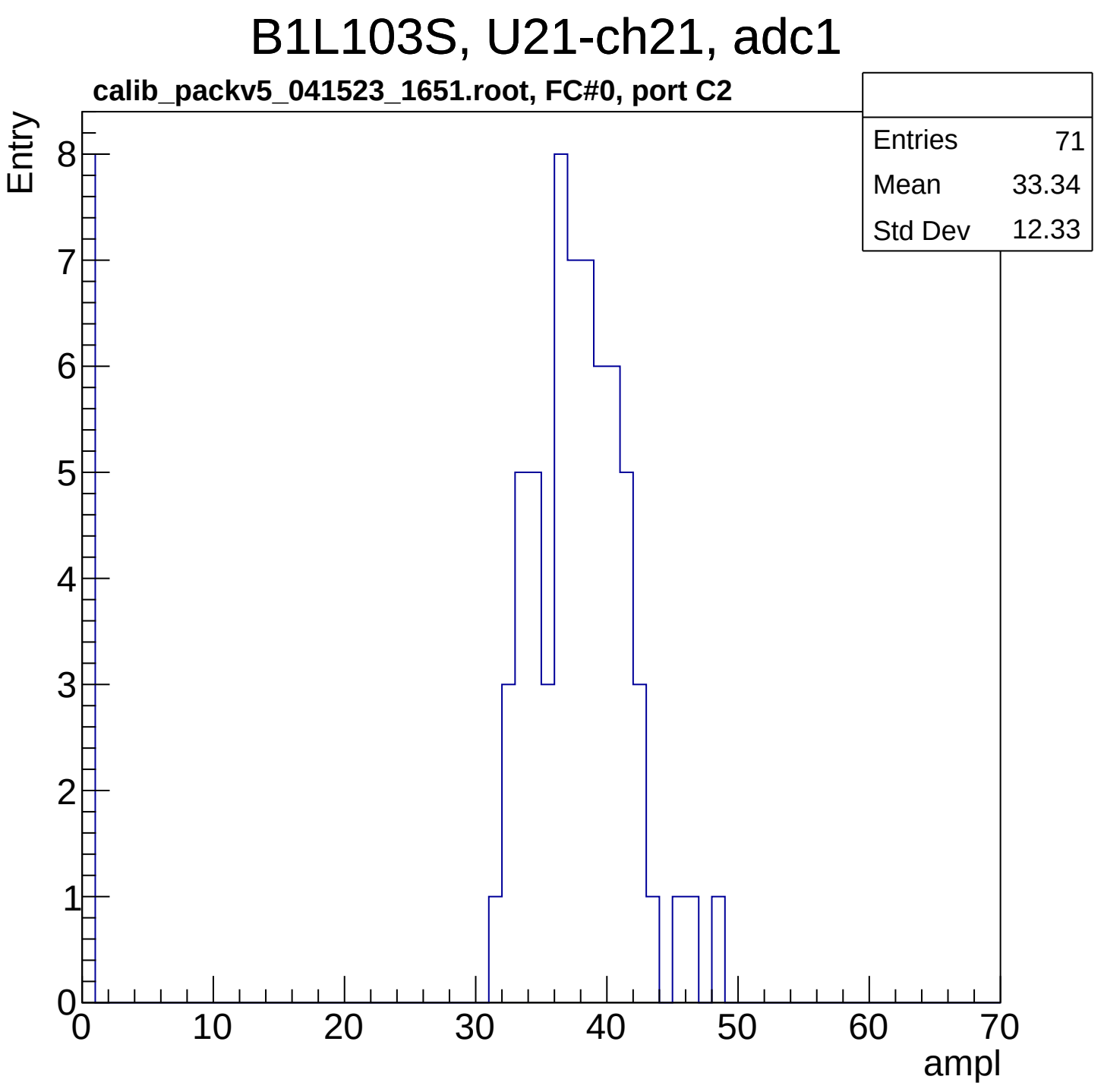
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch21, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 33.34
Std Dev 12.33
Entry
ampl
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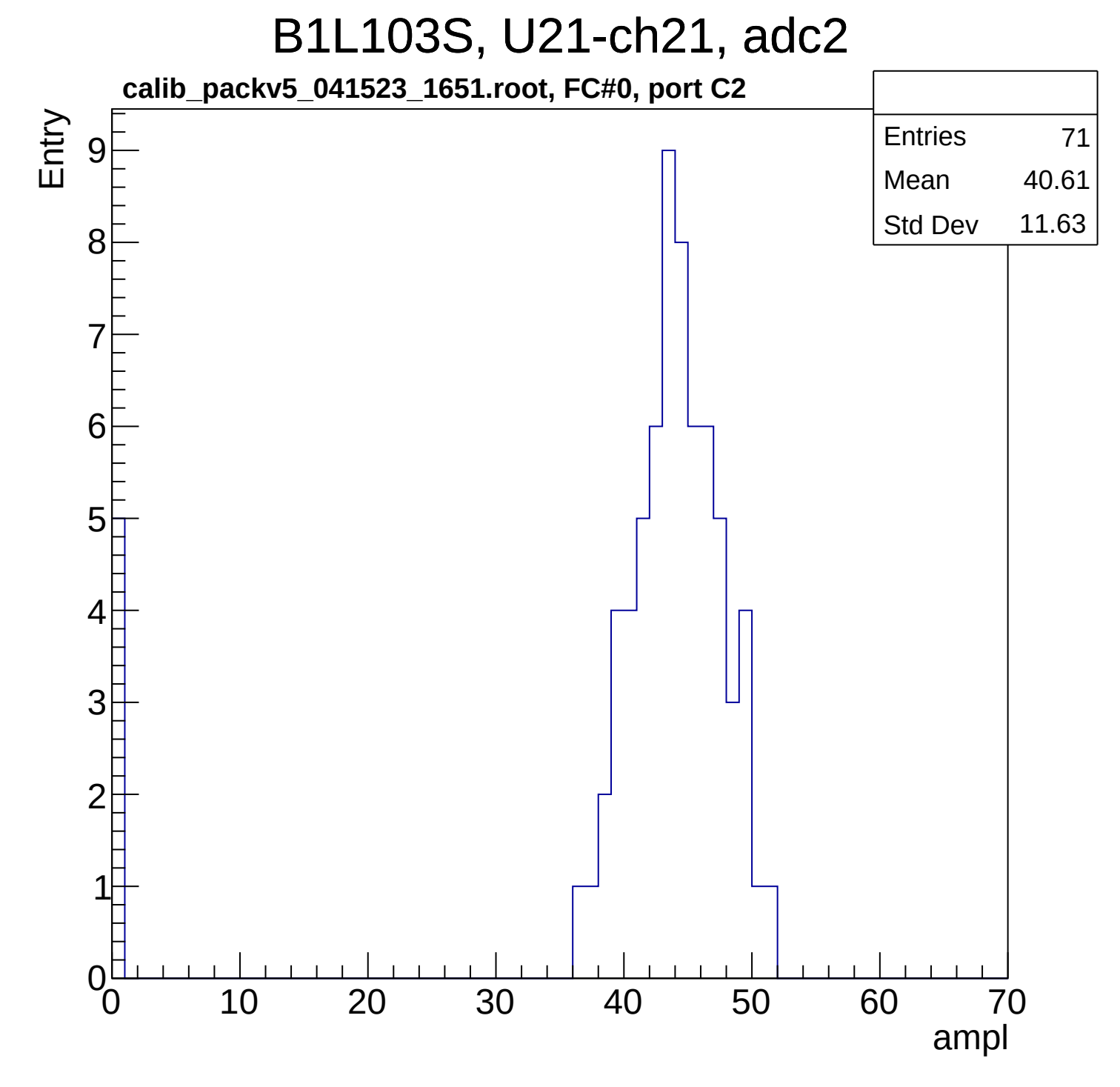
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch21, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 40.61
Std Dev 11.63
Entry
ampl
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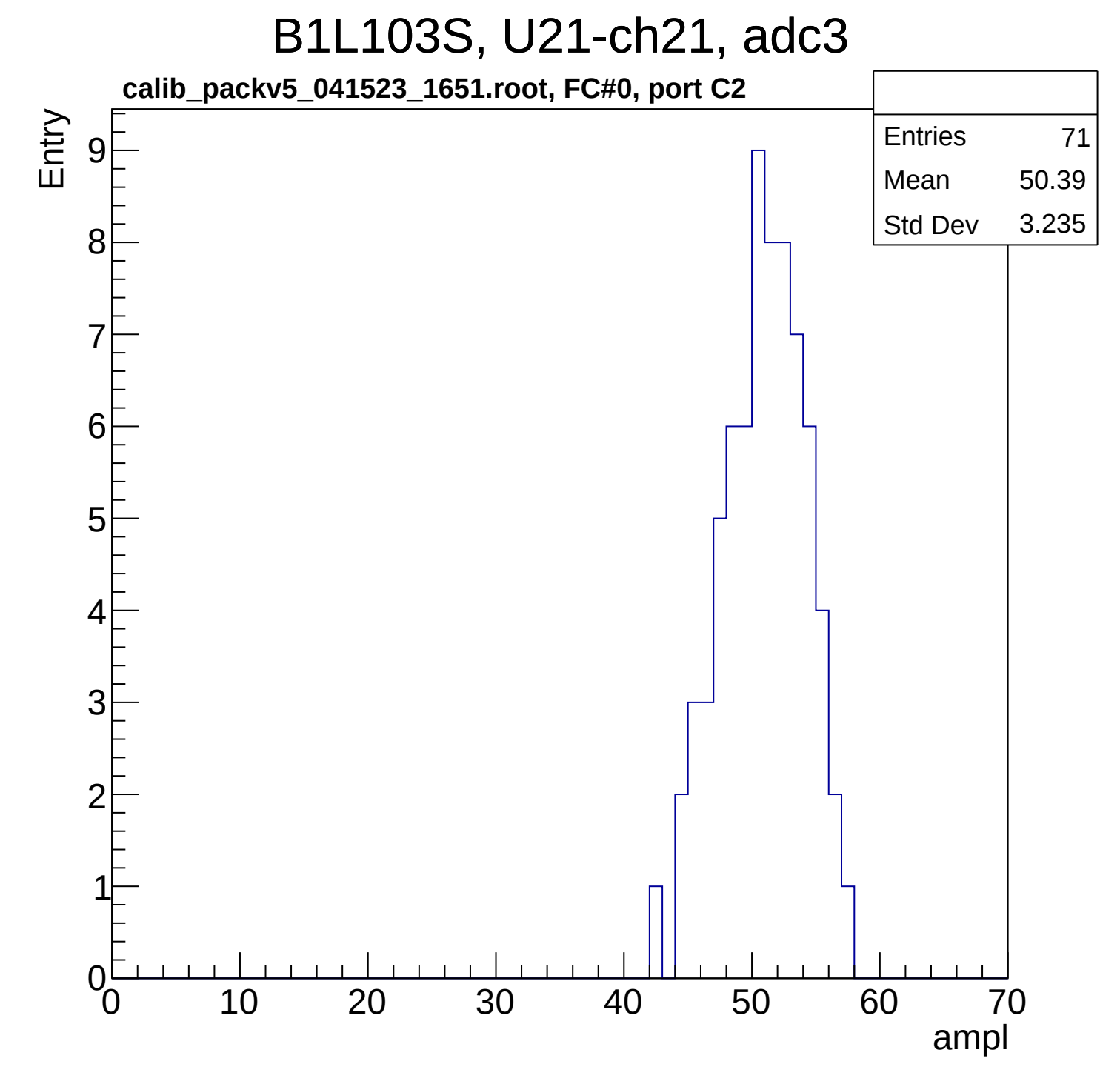
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch21, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 50.39
Std Dev 3.235
Entry
ampl
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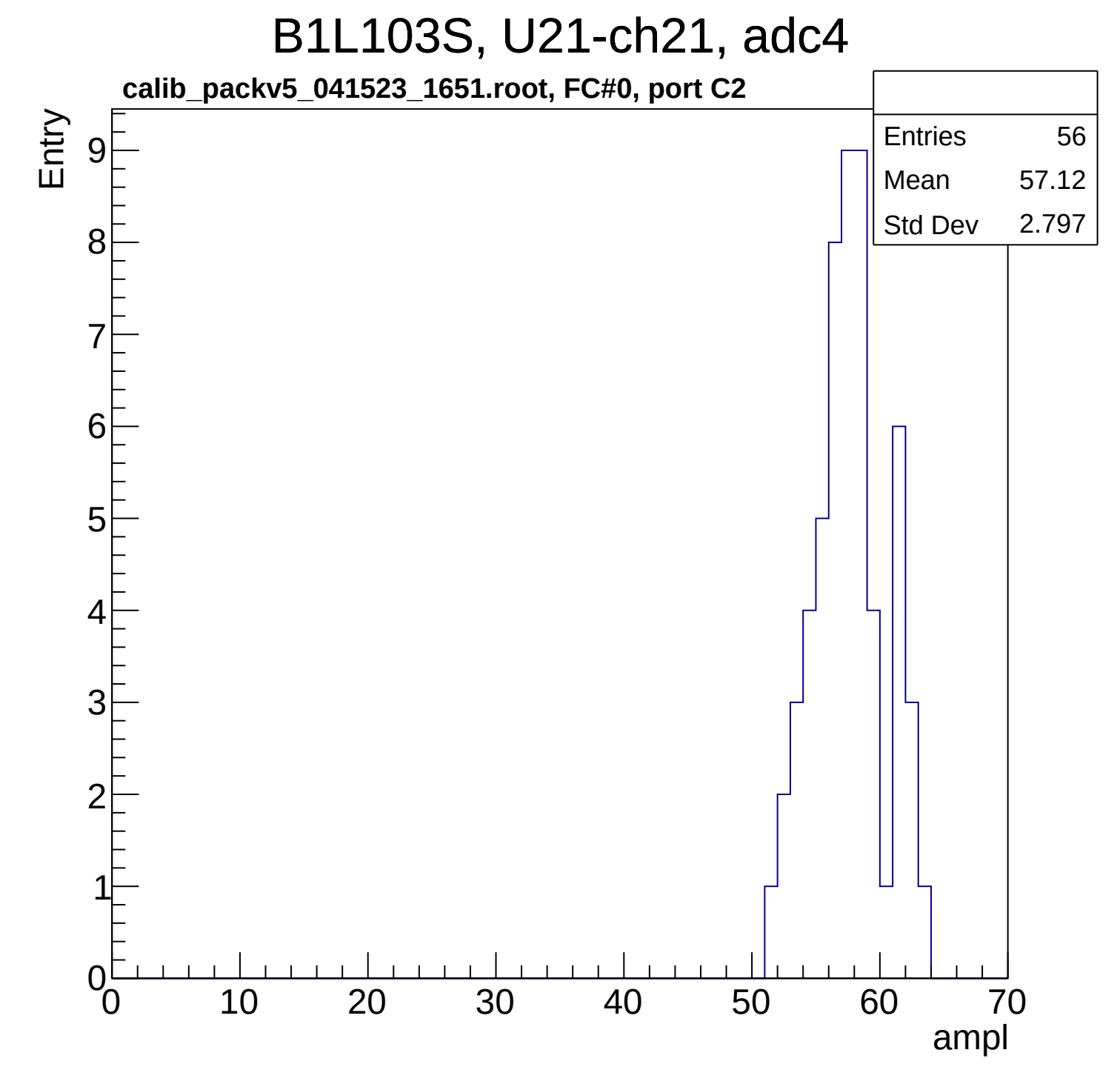
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch21, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 57.12
Std Dev 2.797
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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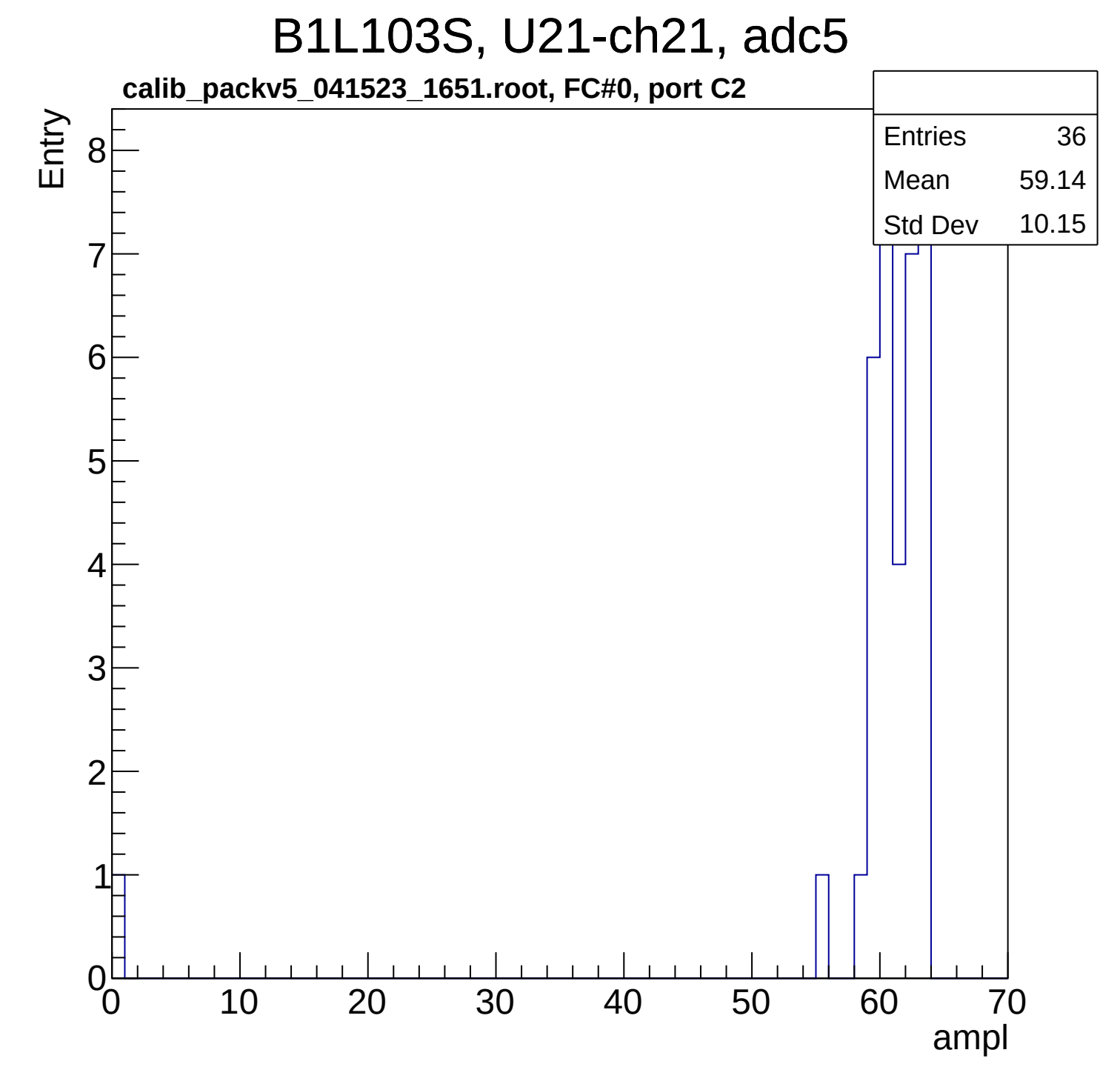
B1L103S, U21-ch21, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 59.14
Std Dev 10.15
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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40
50
60
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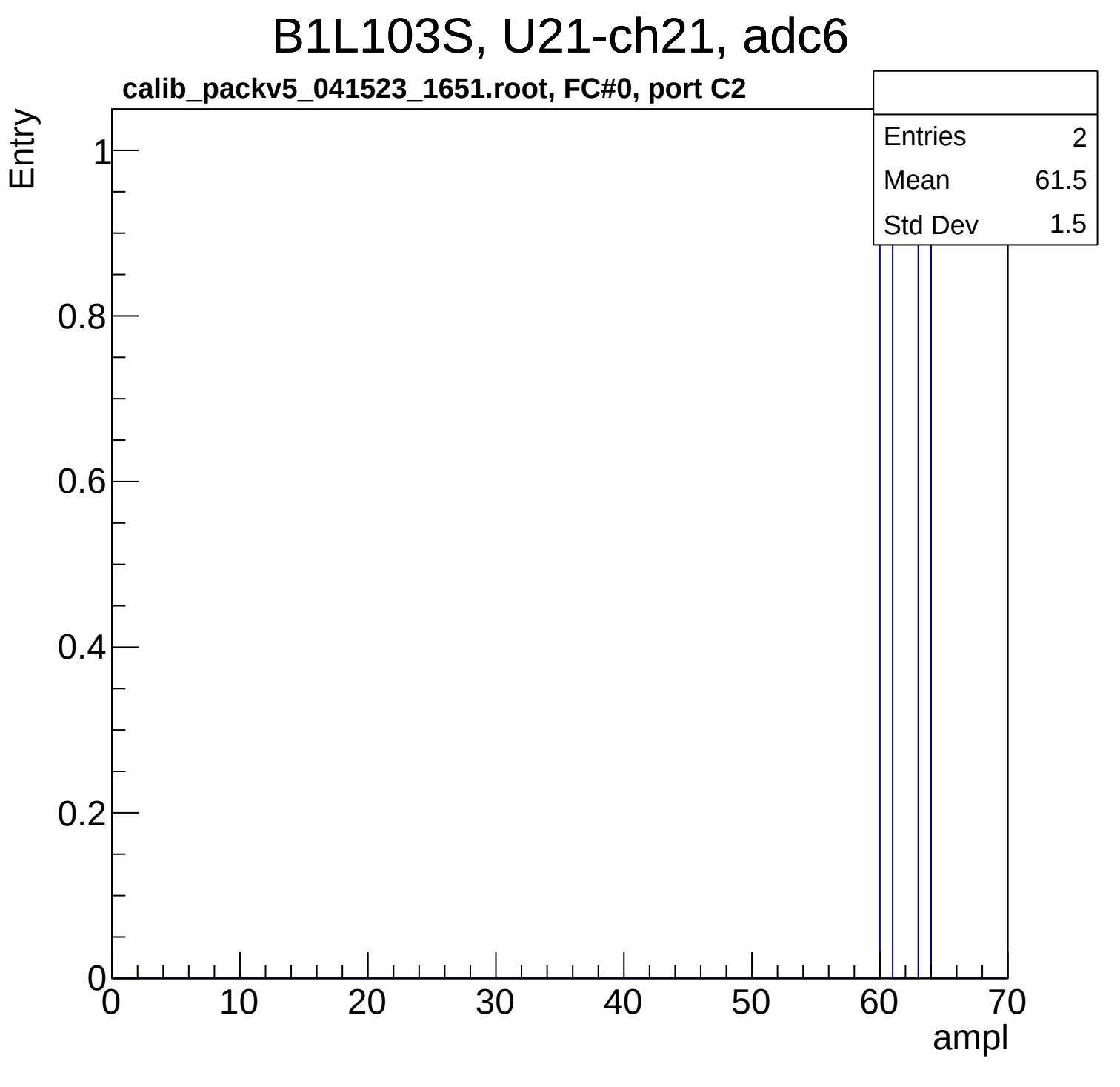
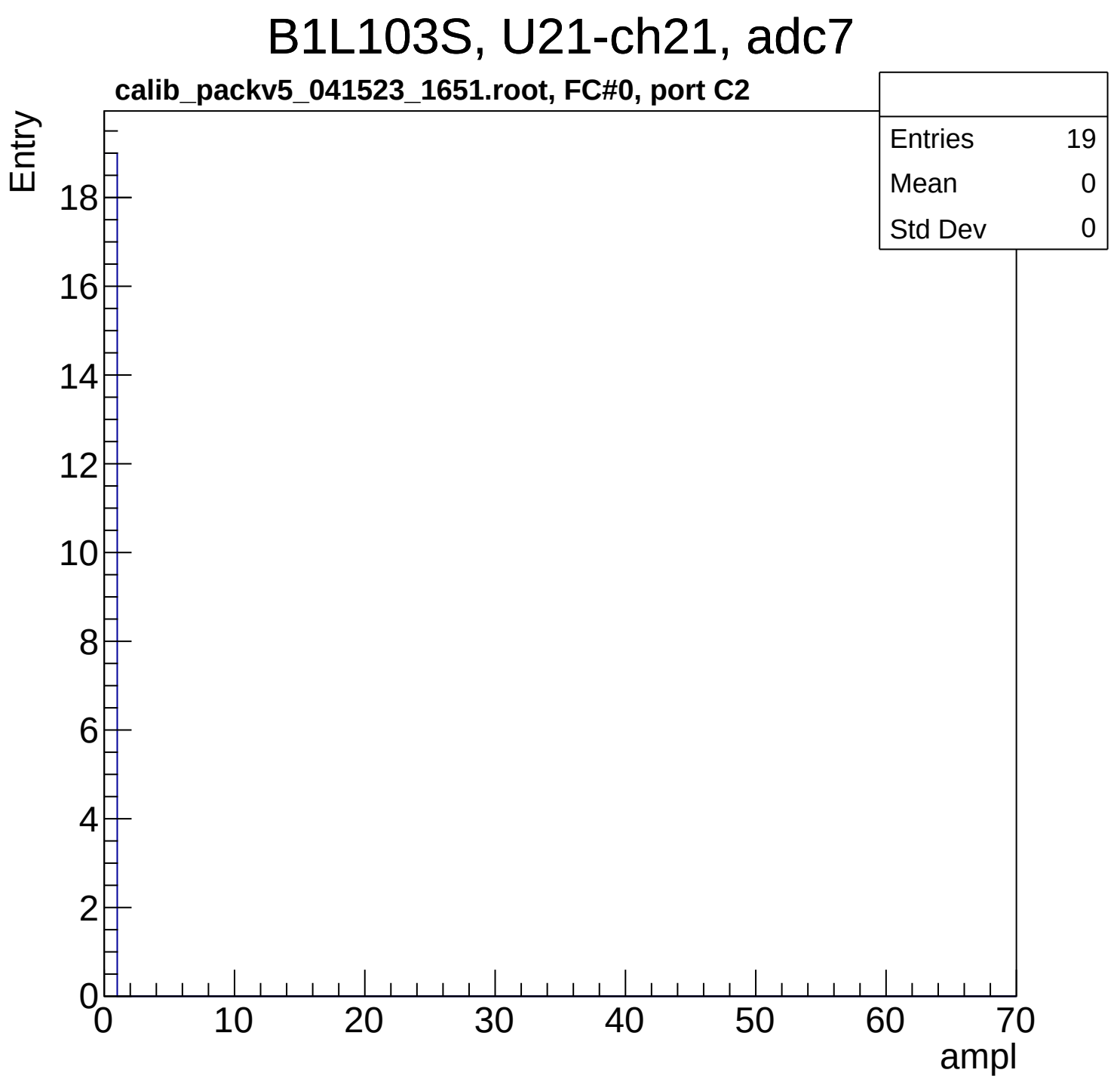
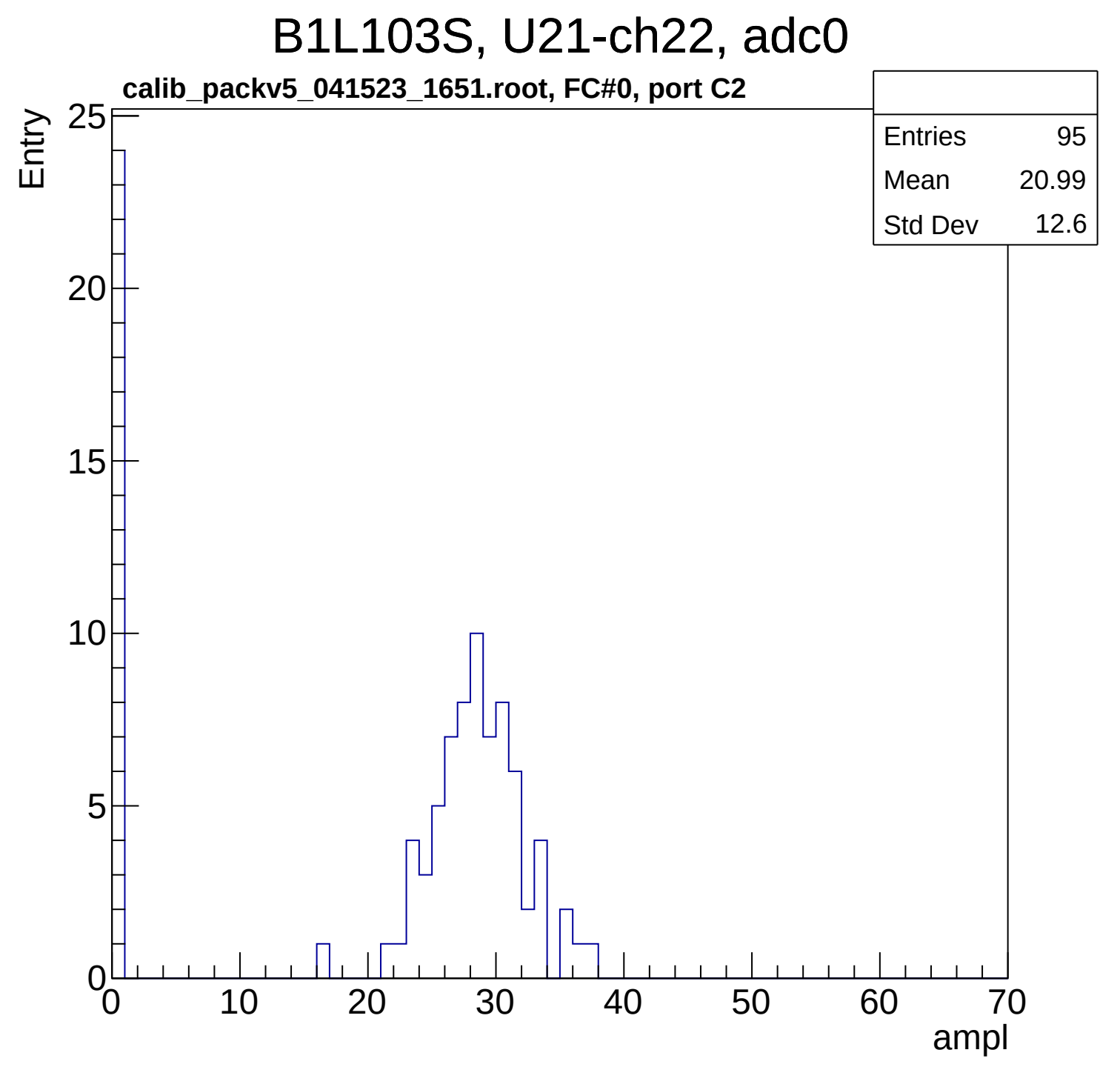
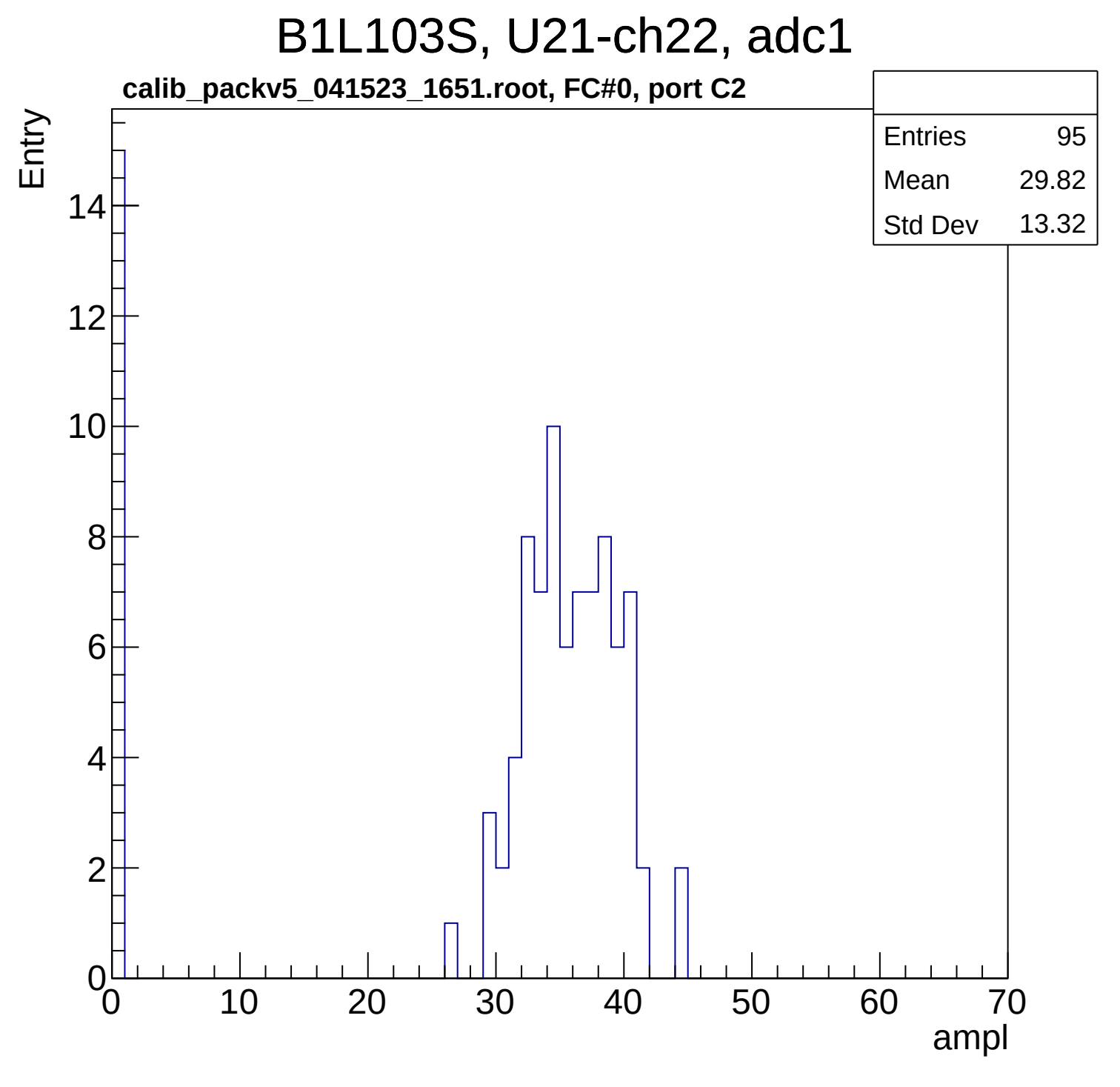

B1L103S, U21-ch21, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 61.5
Std Dev 1.5
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B1L103S, U21-ch21, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch22, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 20.99
Std Dev 12.6
Entry
ampl
0
5
10
15
20
25
0
10
20
30
40
50
60
70


B1L103S, U21-ch22, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 29.82
Std Dev 13.32
Entry
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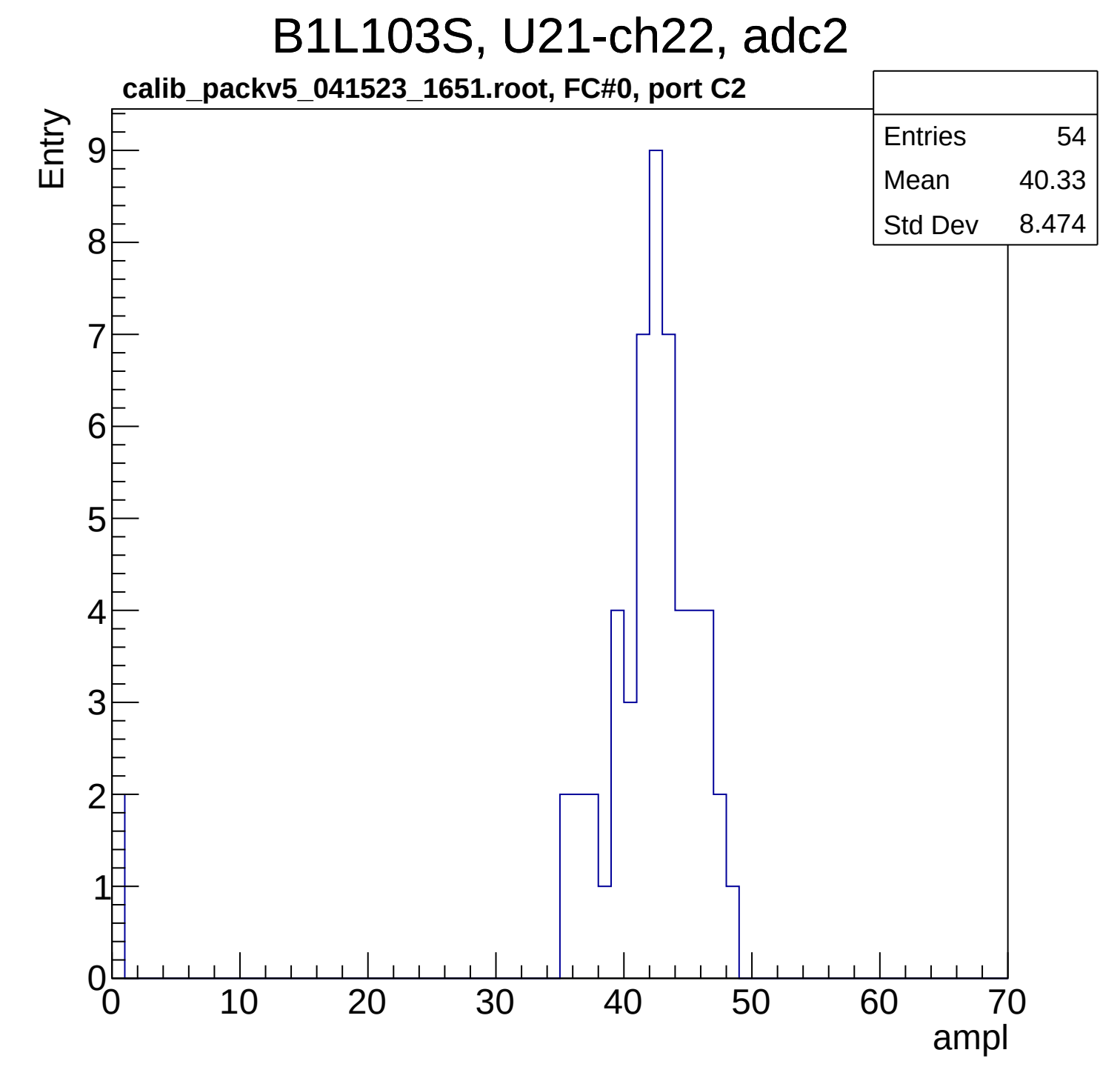
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch22, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 40.33
Std Dev 8.474
Entry
ampl
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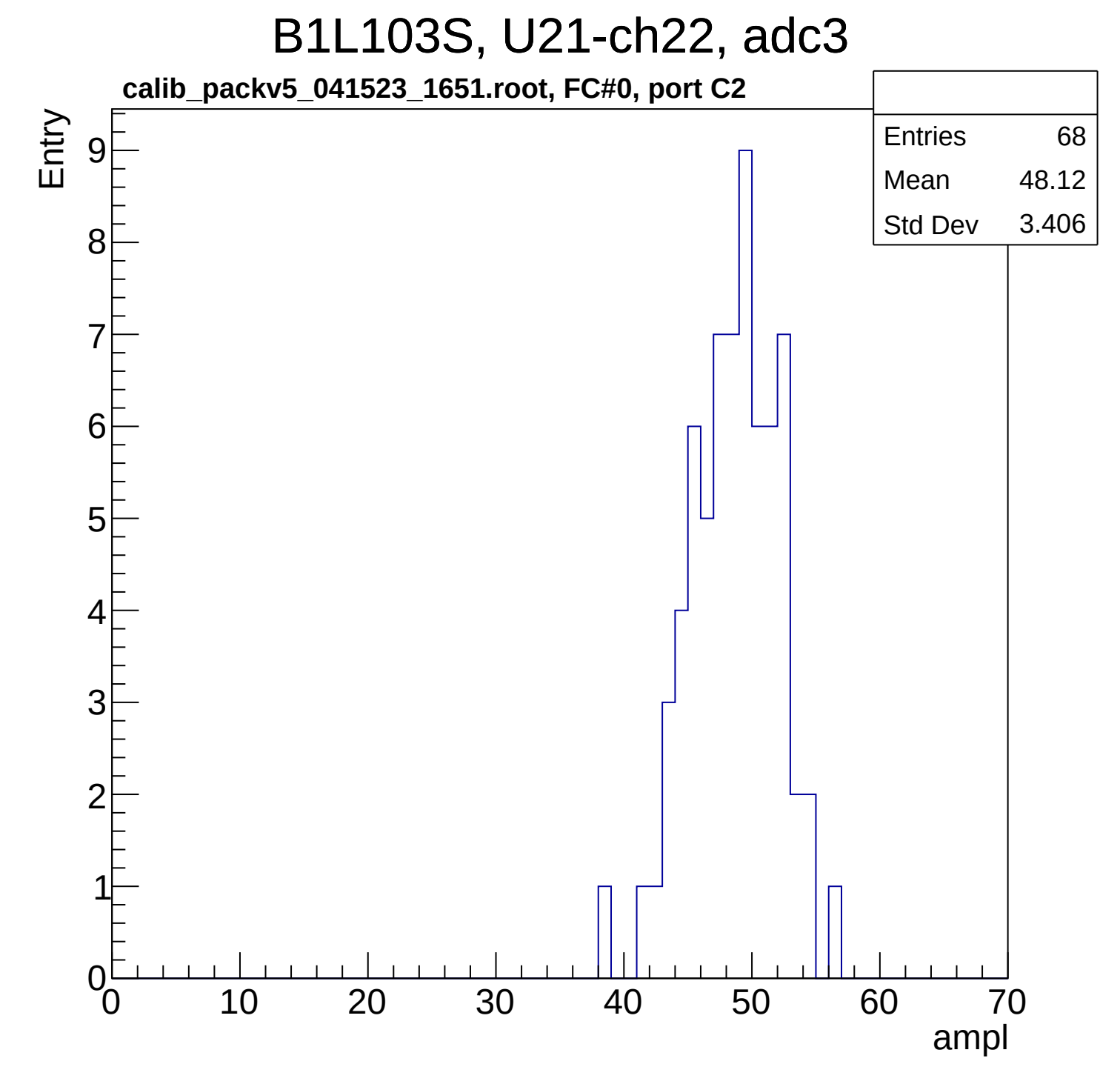
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch22, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 48.12
Std Dev 3.406
Entry
ampl
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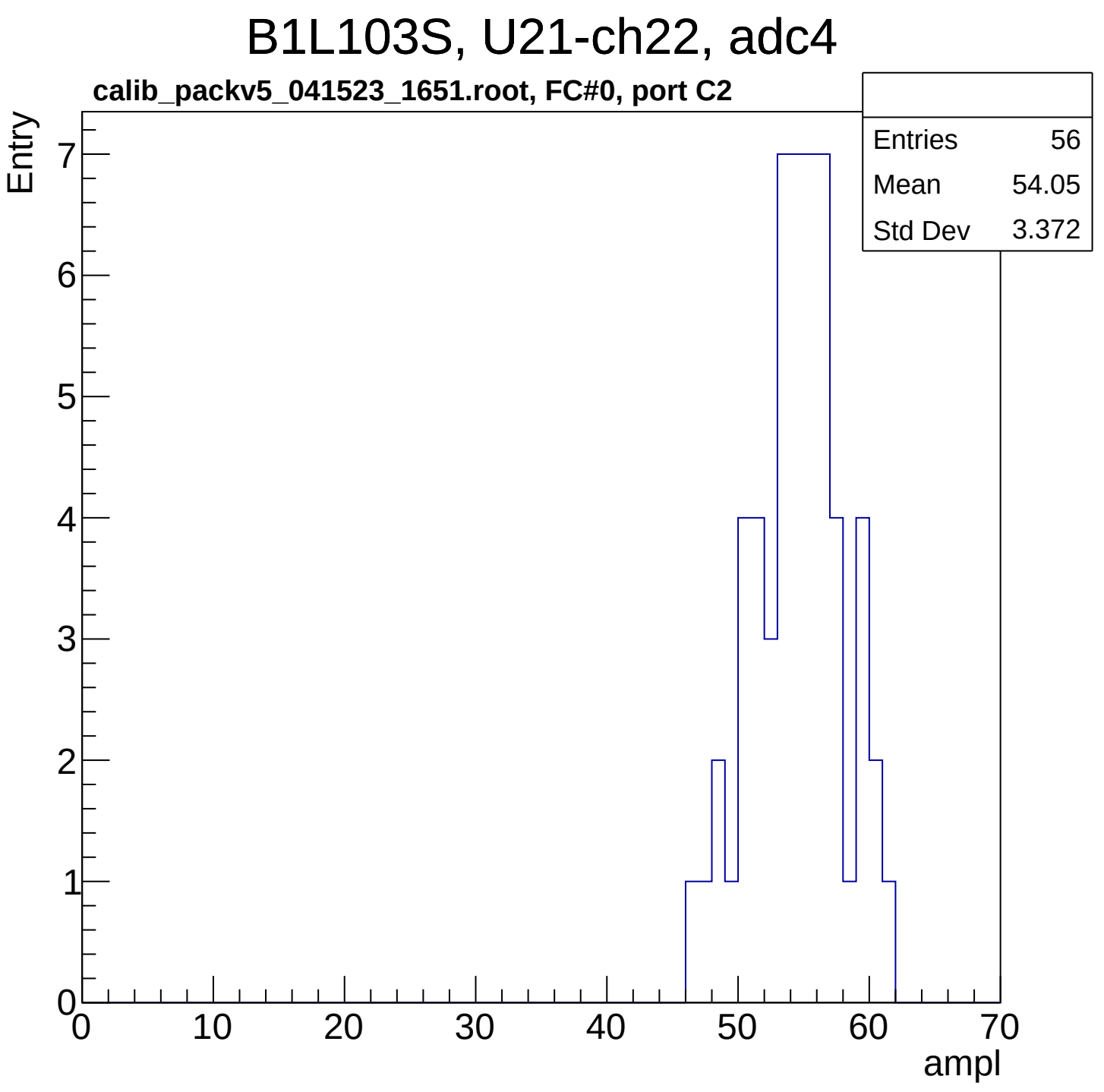
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch22, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 54.05
Std Dev 3.372
Entry
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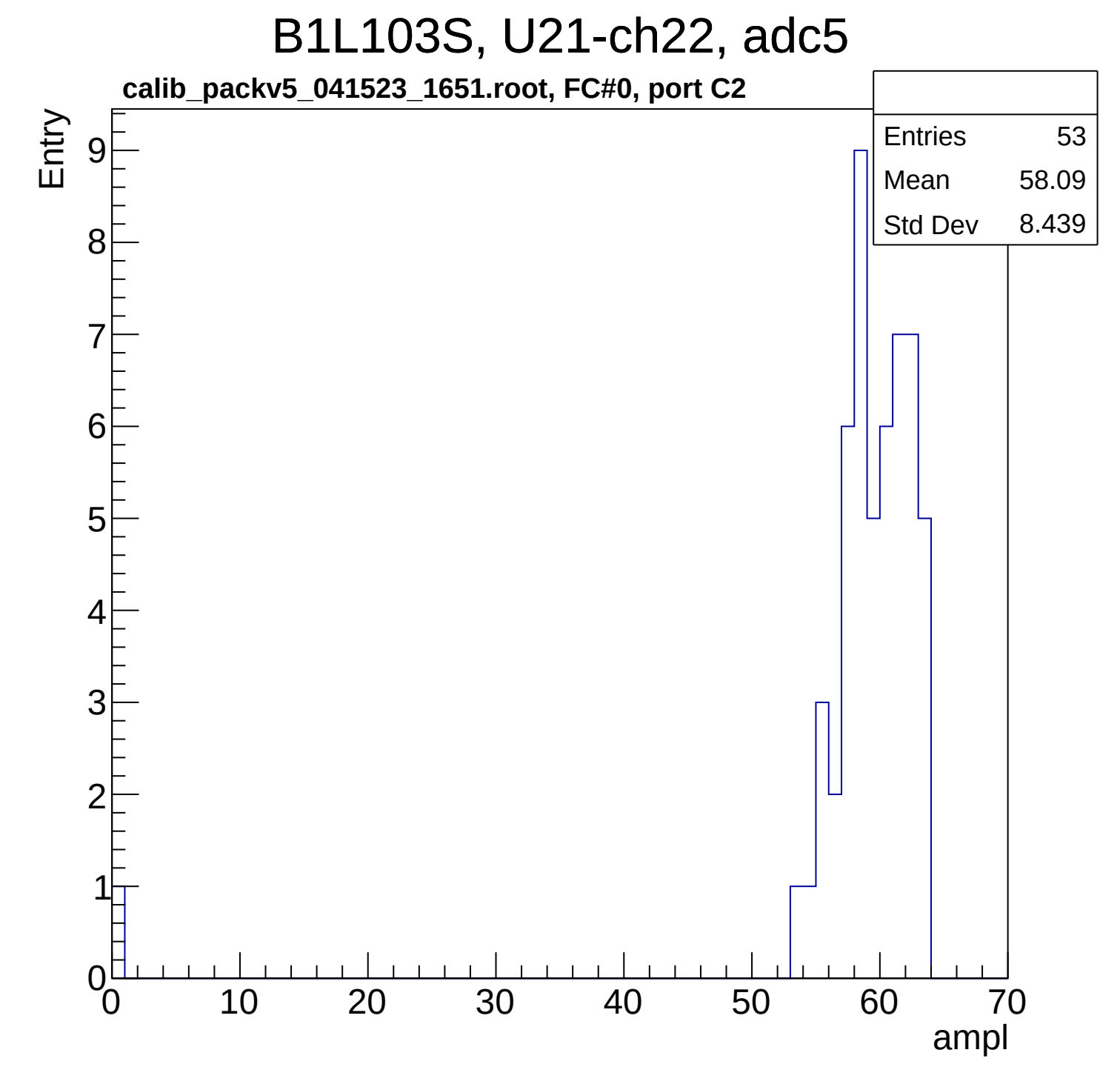
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch22, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 58.09
Std Dev 8.439
Entry
ampl
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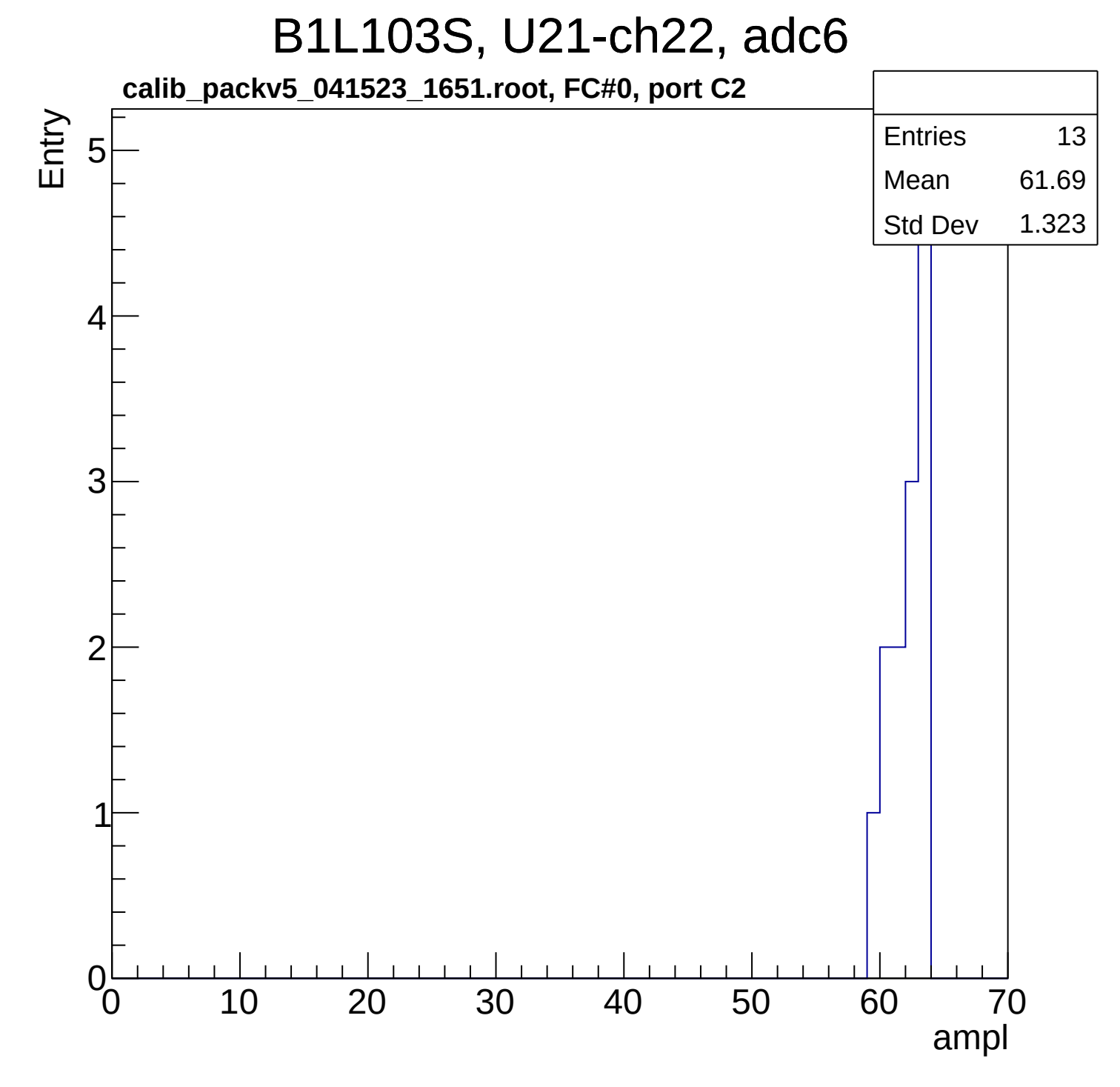
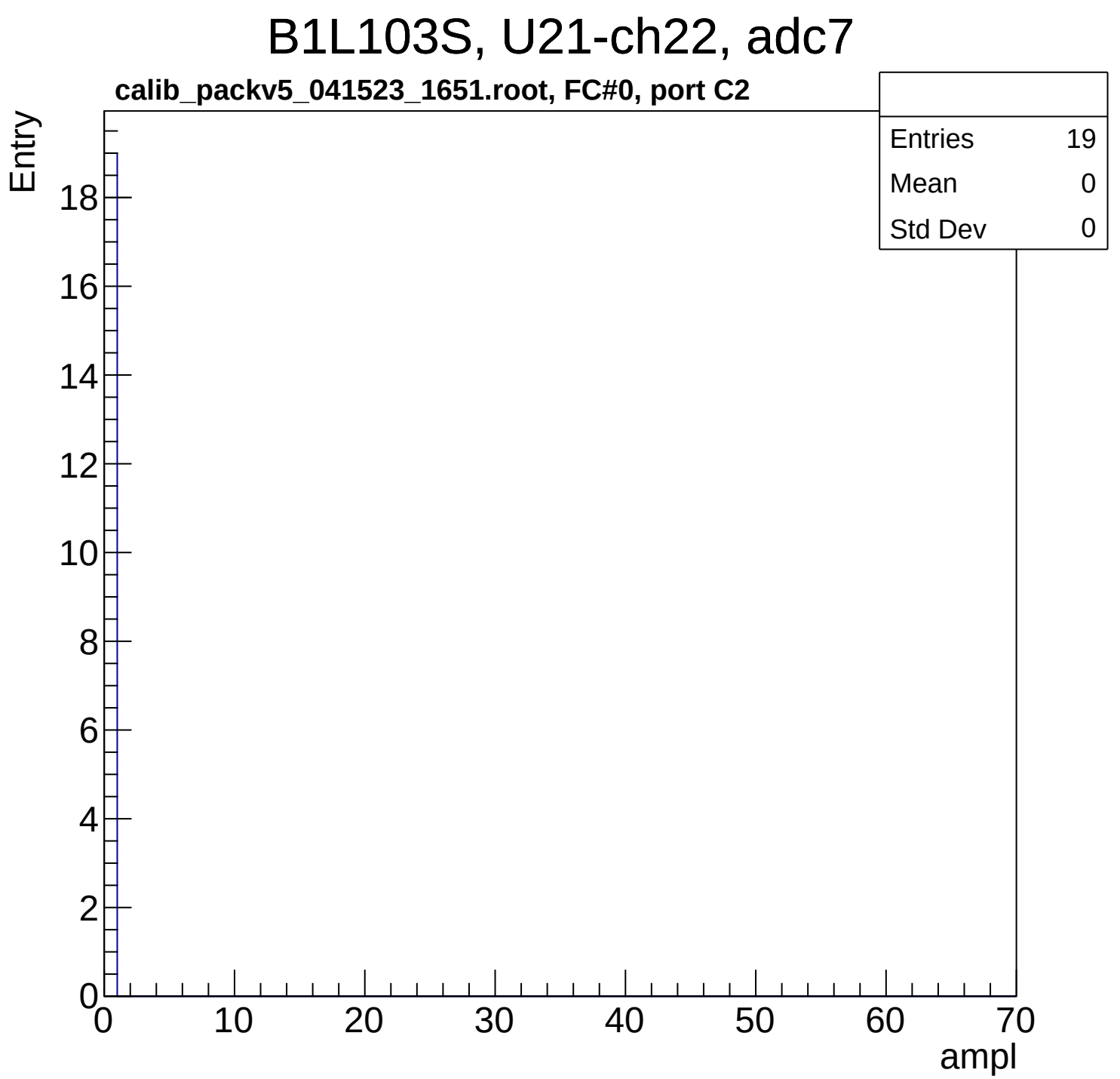
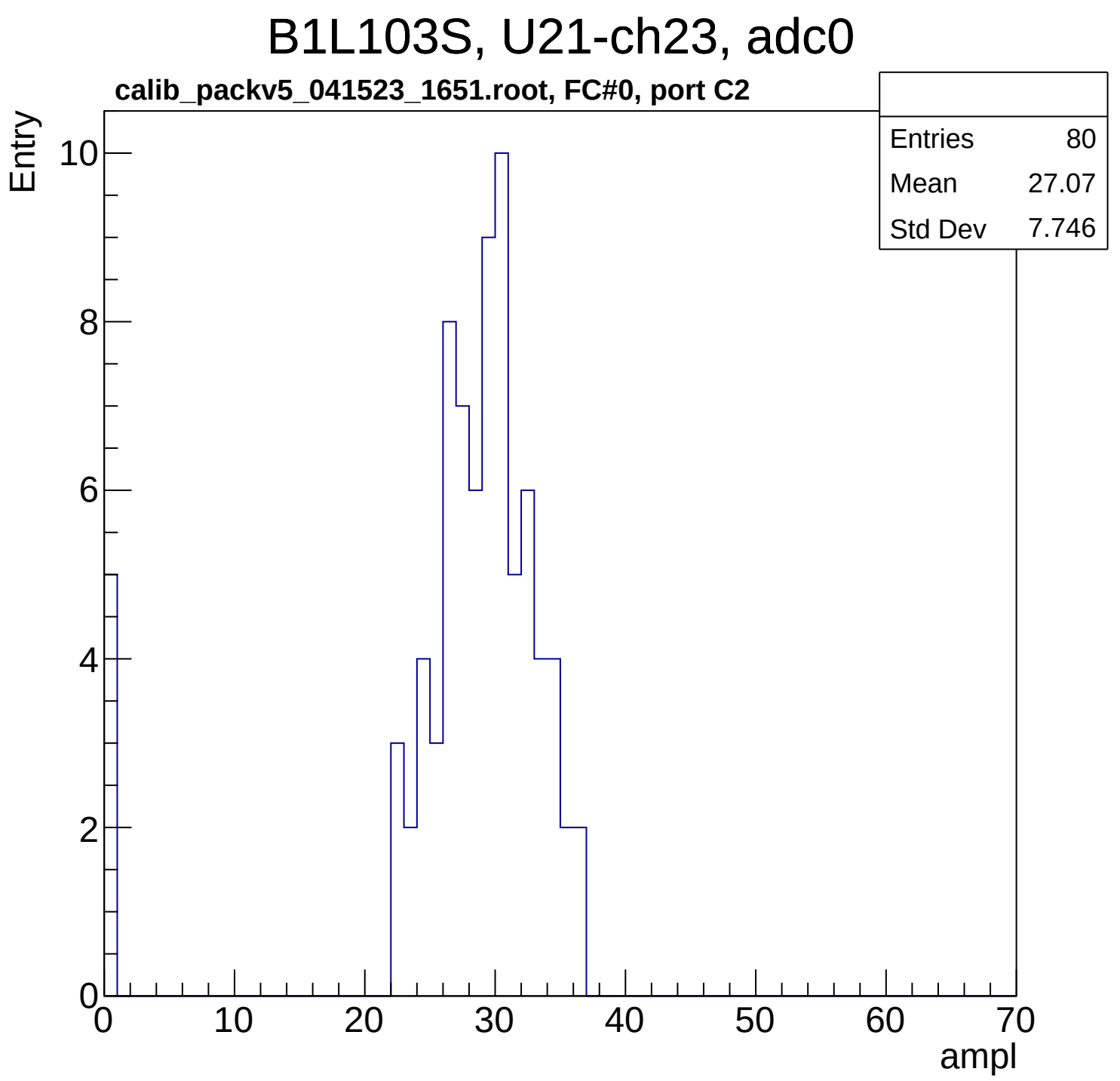
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch22, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 61.69
Std Dev 1.323
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U21-ch22, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch23, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 27.07
Std Dev 7.746
Entry
ampl
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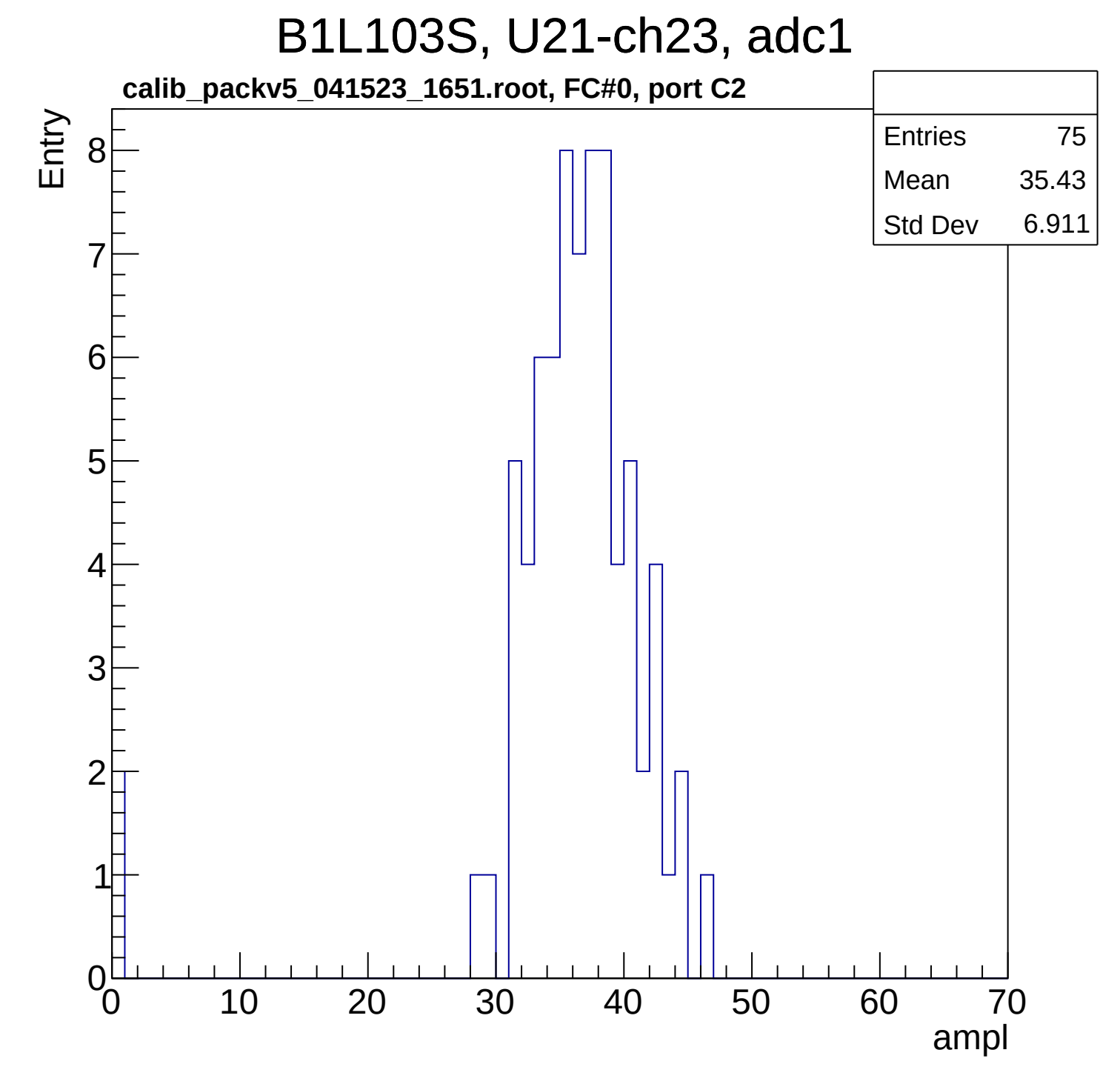
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U21-ch23, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 35.43
Std Dev 6.911
Entry
ampl
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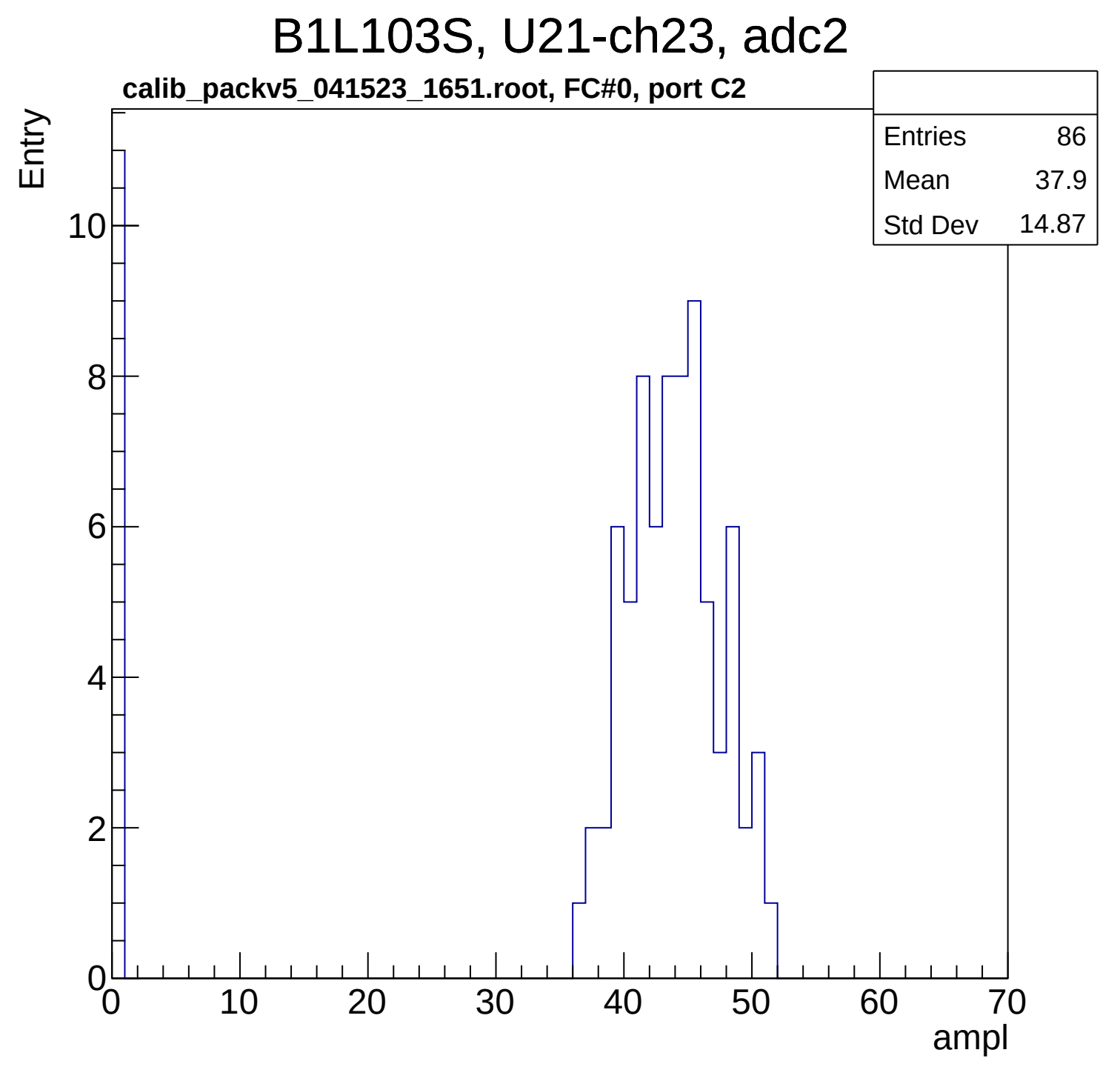
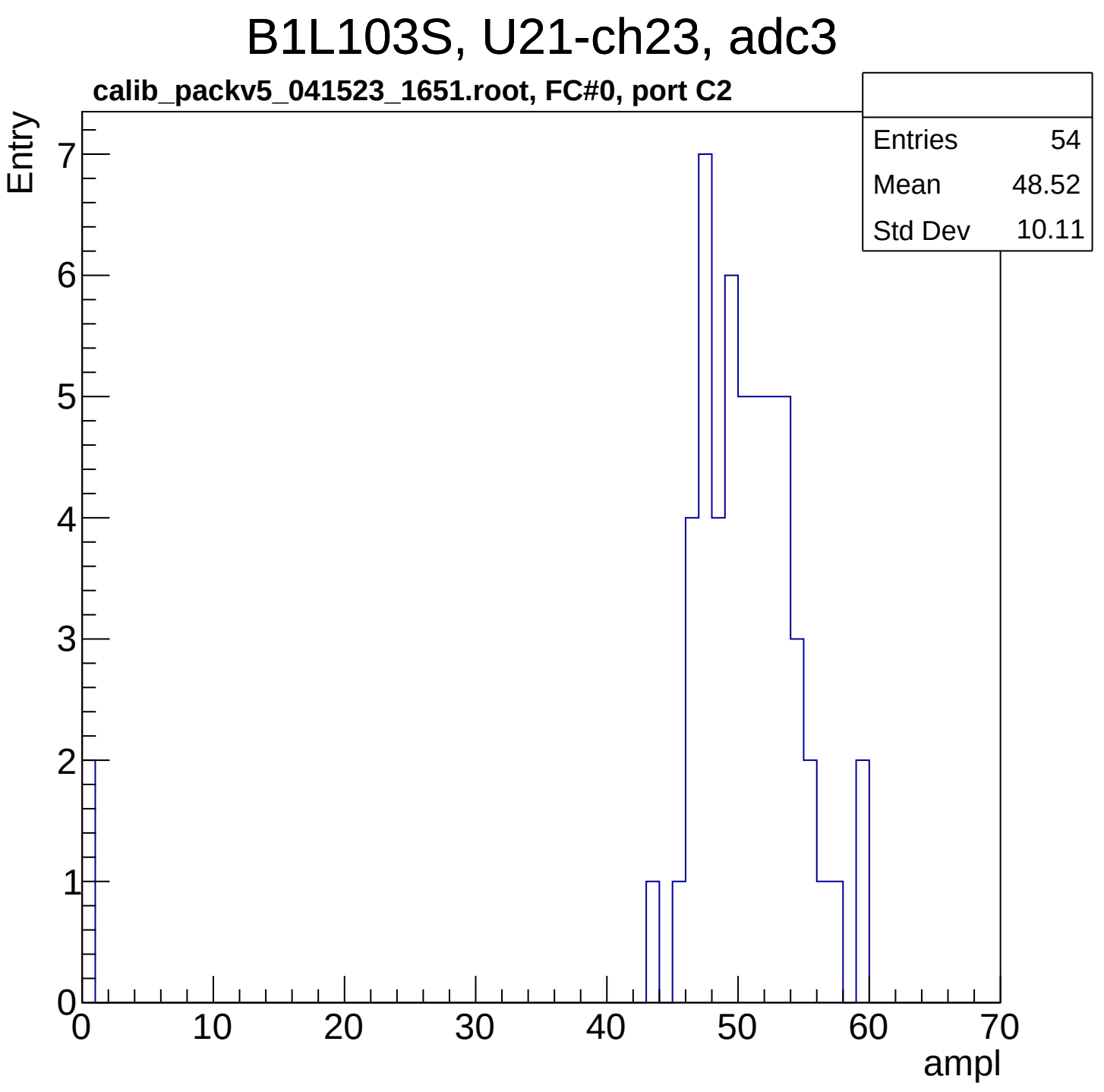
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch23, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 37.9
Std Dev 14.87
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch23, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 48.52
Std Dev 10.11
Entry
ampl
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2
3
4
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6
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0
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40
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60
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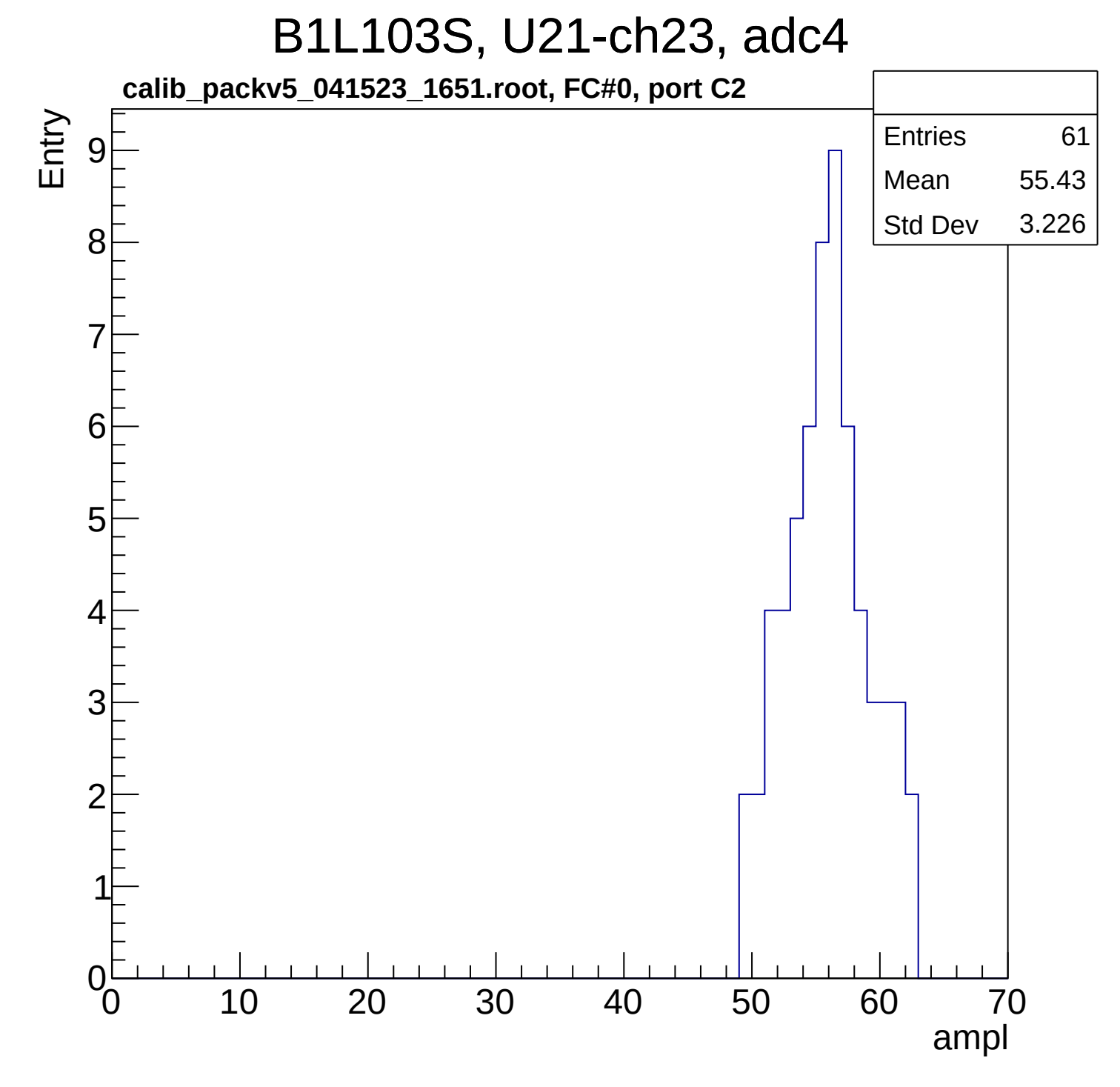
B1L103S, U21-ch23, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 55.43
Std Dev 3.226
Entry
ampl
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2
3
4
5
6
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8
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0
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40
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60
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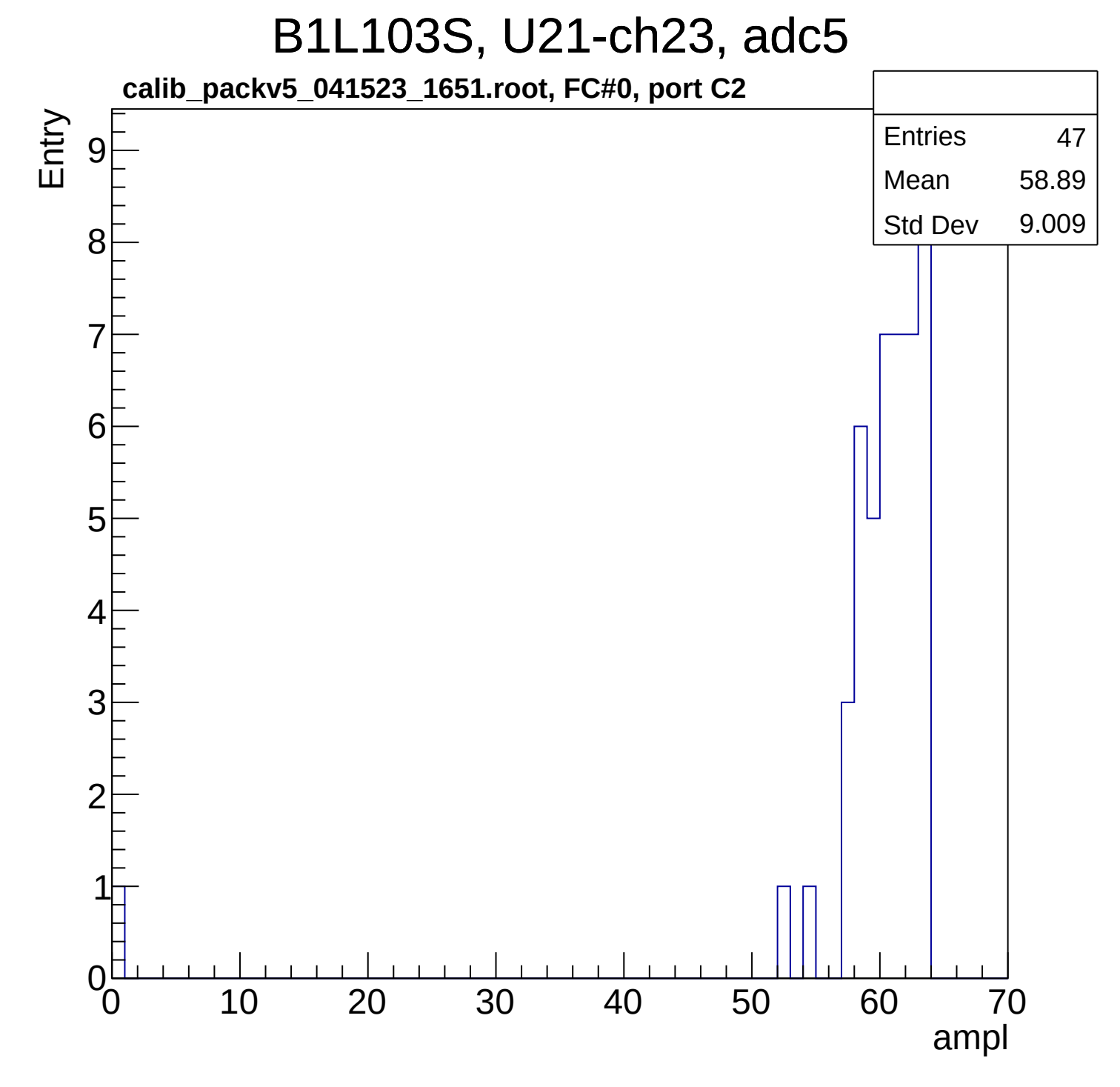
B1L103S, U21-ch23, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 58.89
Std Dev 9.009
Entry
ampl
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2
3
4
5
6
7
8
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0
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40
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60
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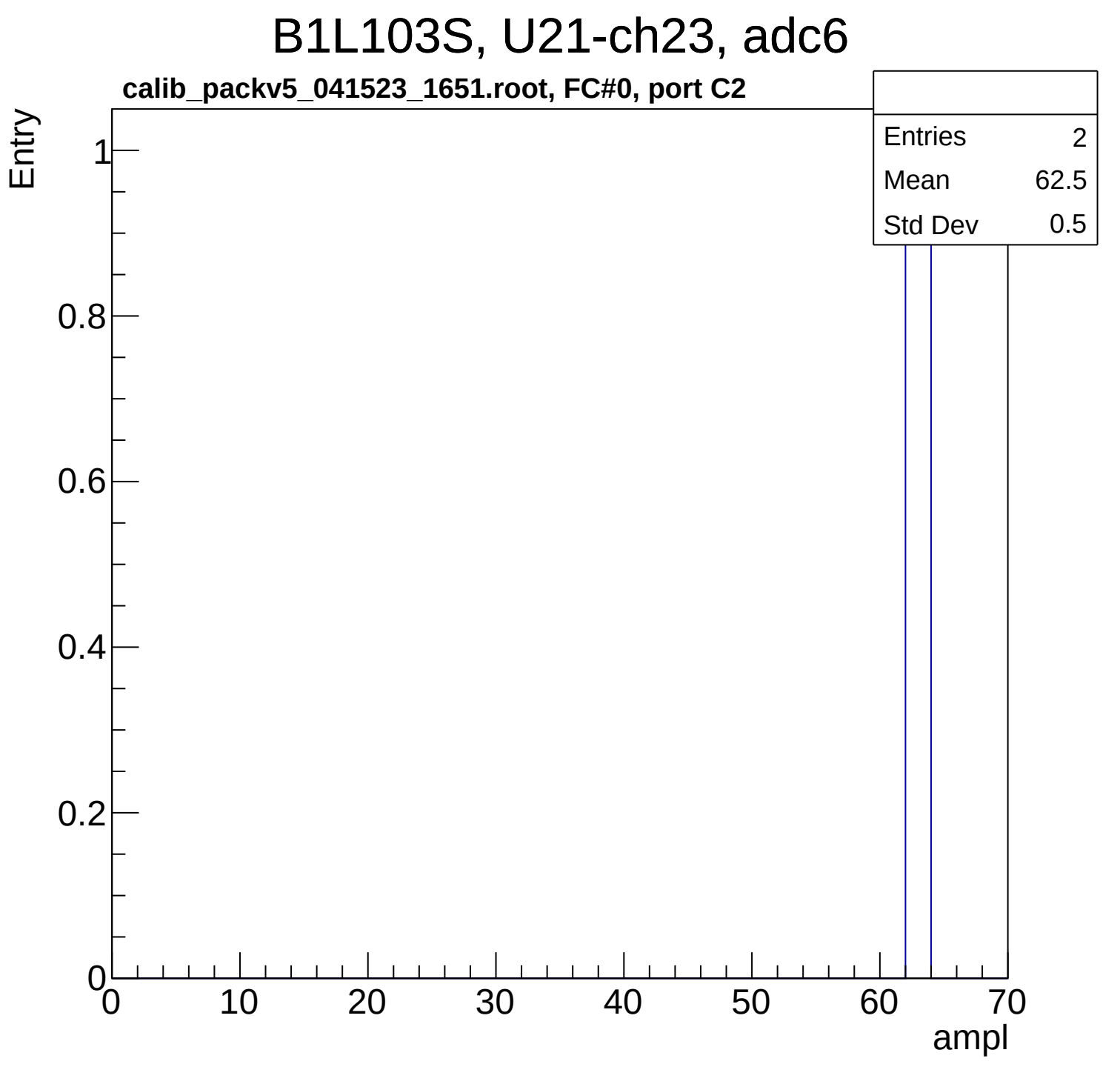
B1L103S, U21-ch23, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
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0.8
0.6
0.4
0.2
0
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10
20
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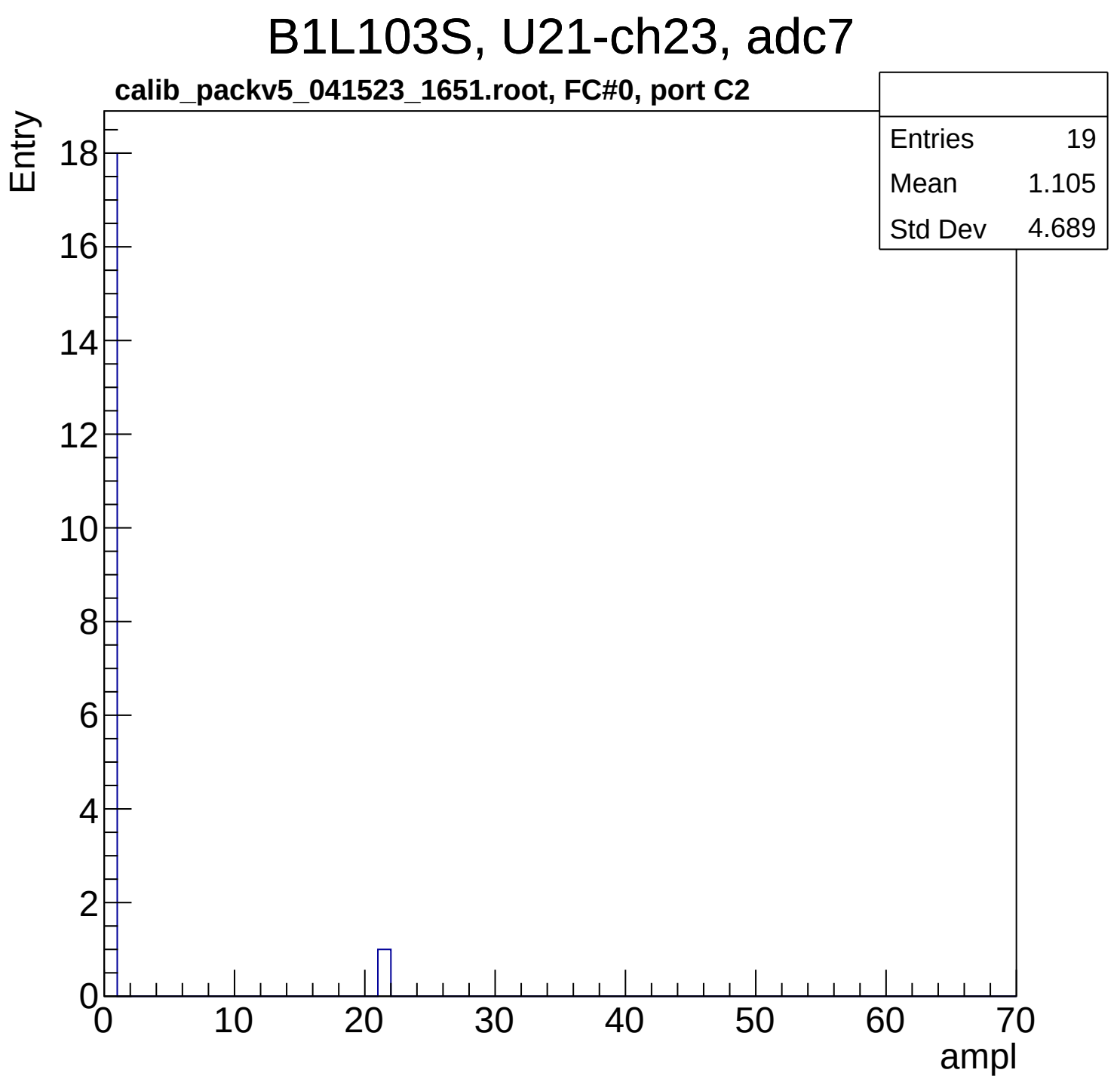
40
50
60
70
ampl


B1L103S, U21-ch23, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.105
Std Dev 4.689
Entry
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6
8
10
12
14
16
18
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10
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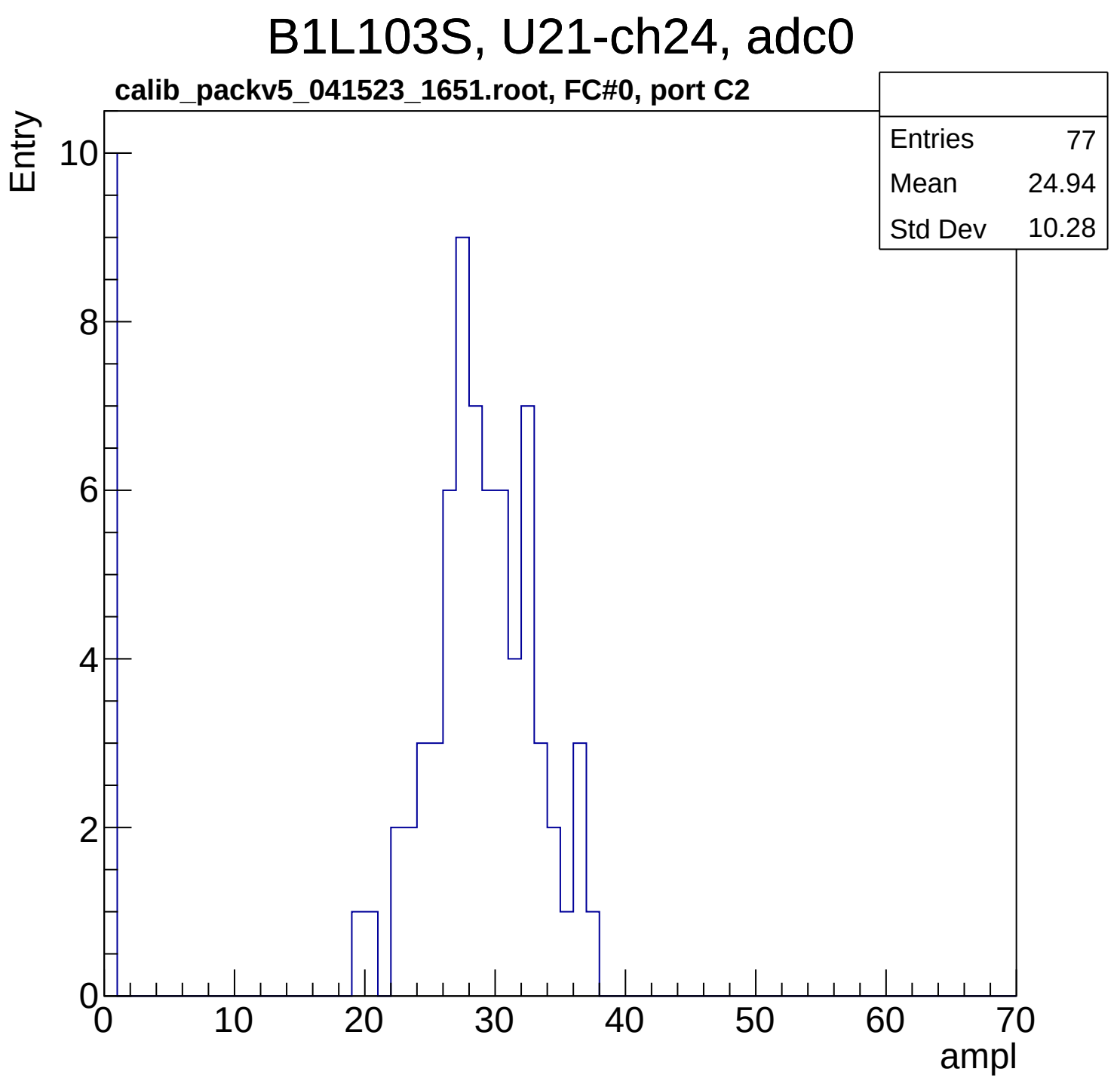
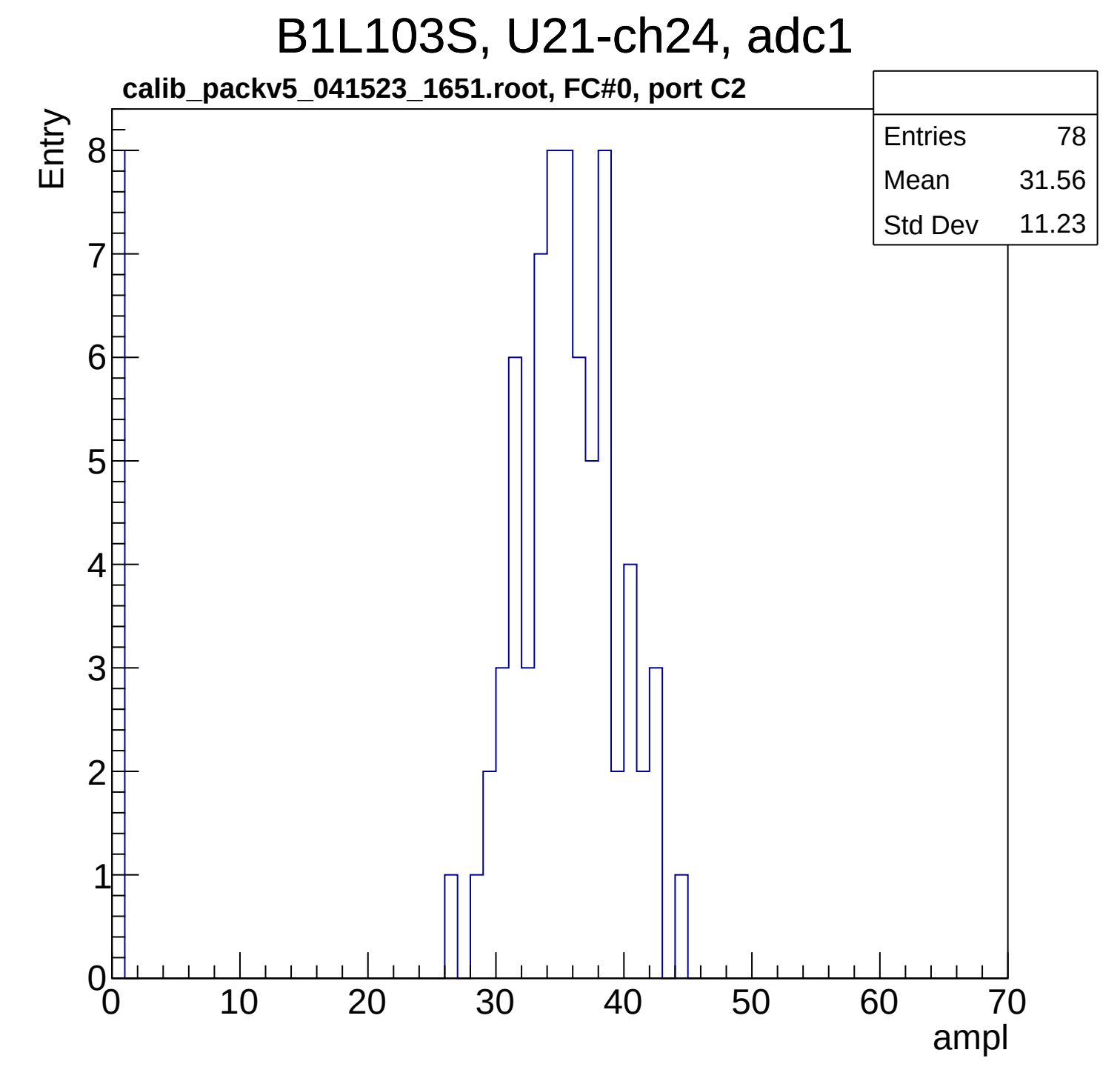
50
60
70
ampl


B1L103S, U21-ch24, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 24.94
Std Dev 10.28
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch24, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 31.56
Std Dev 11.23
Entry
ampl
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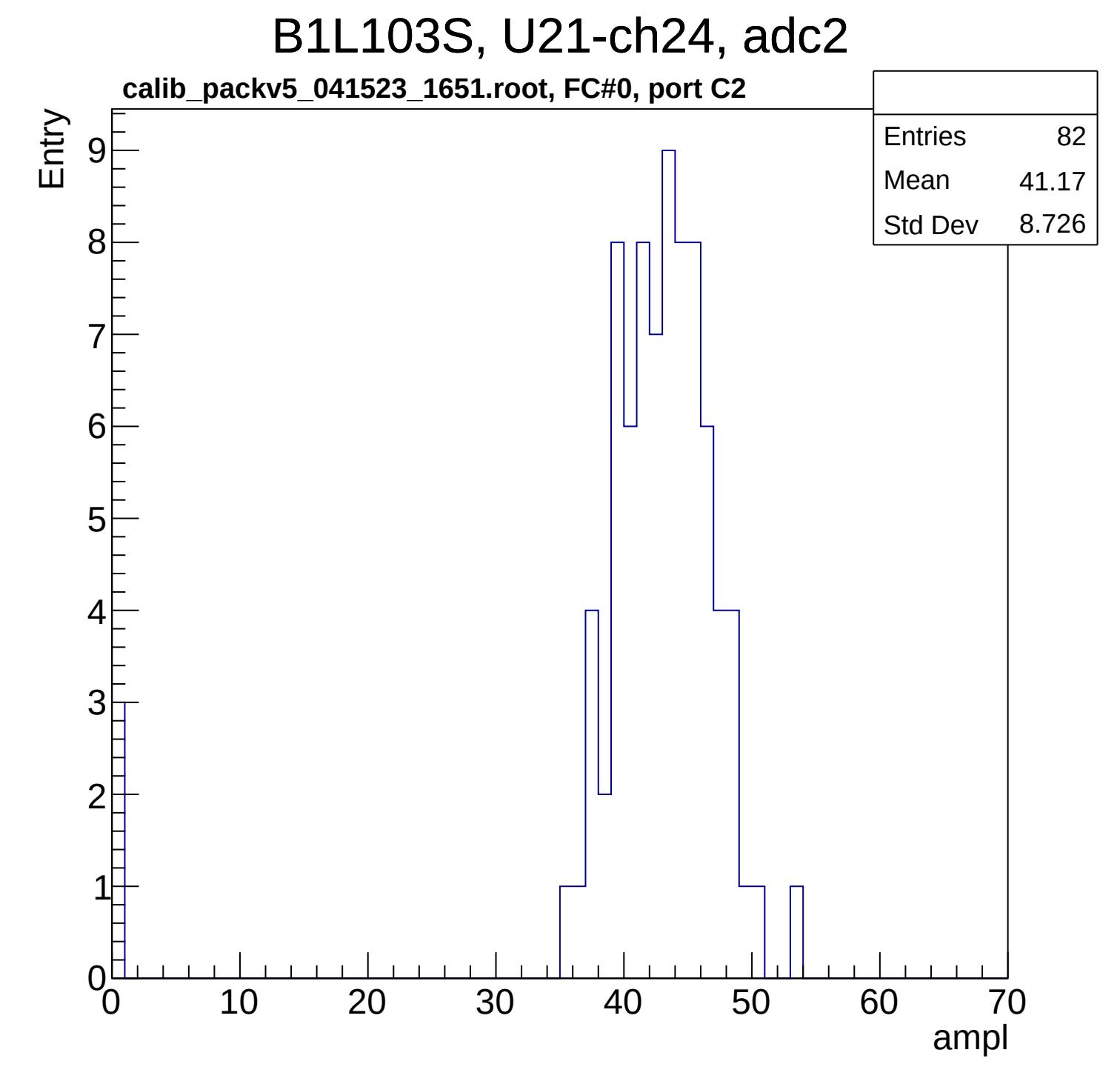
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch24, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 41.17
Std Dev 8.726
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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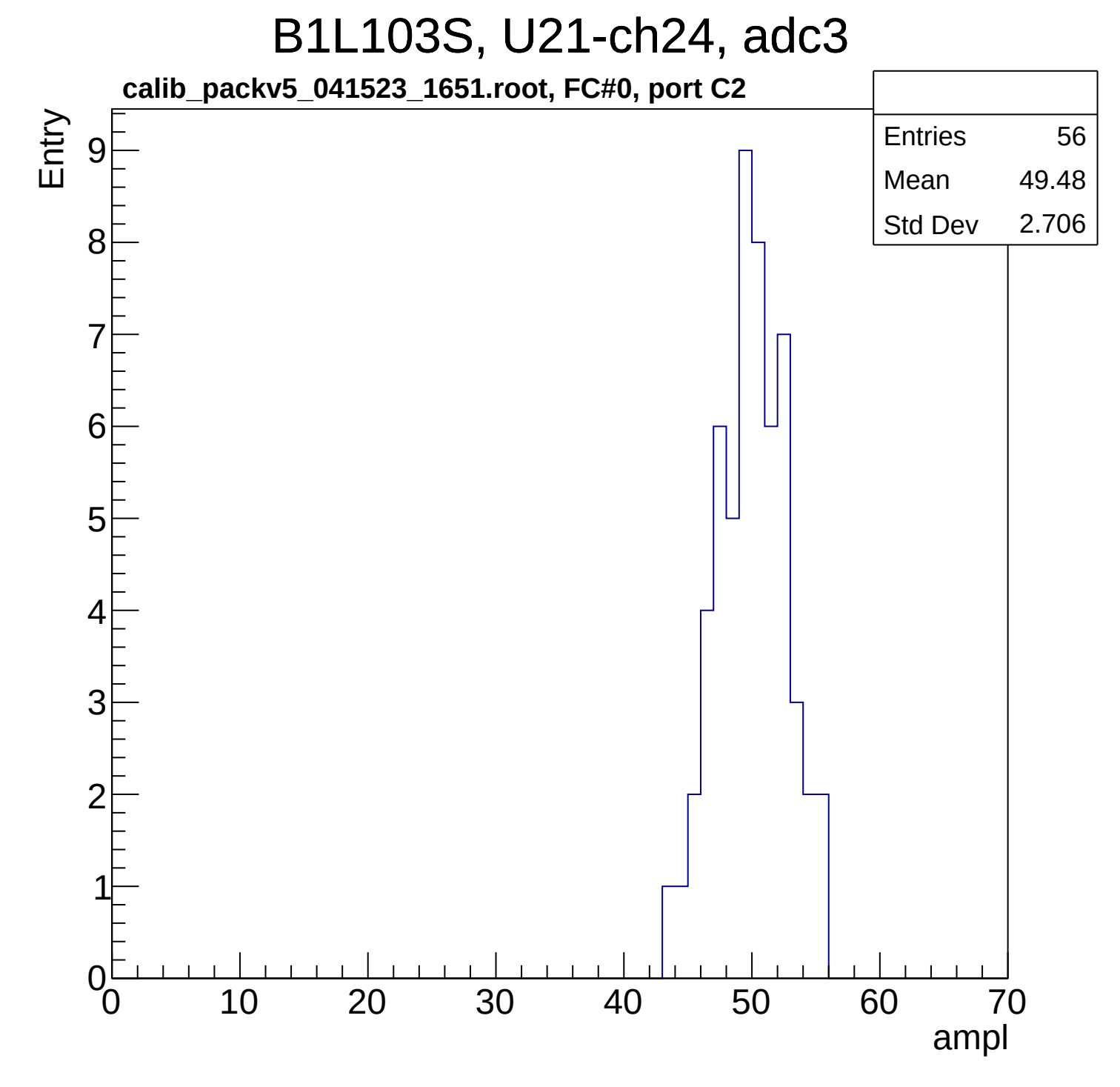
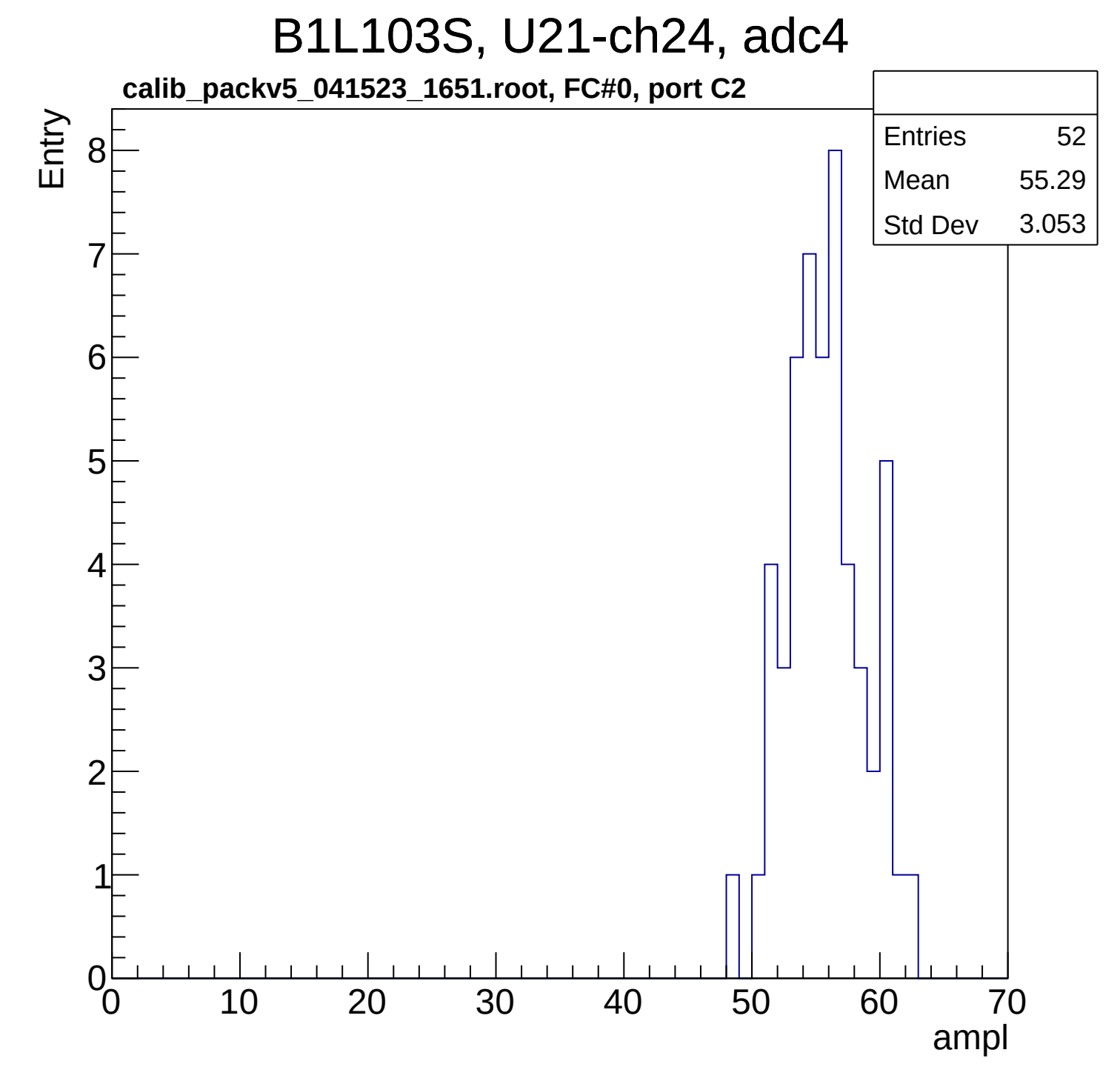
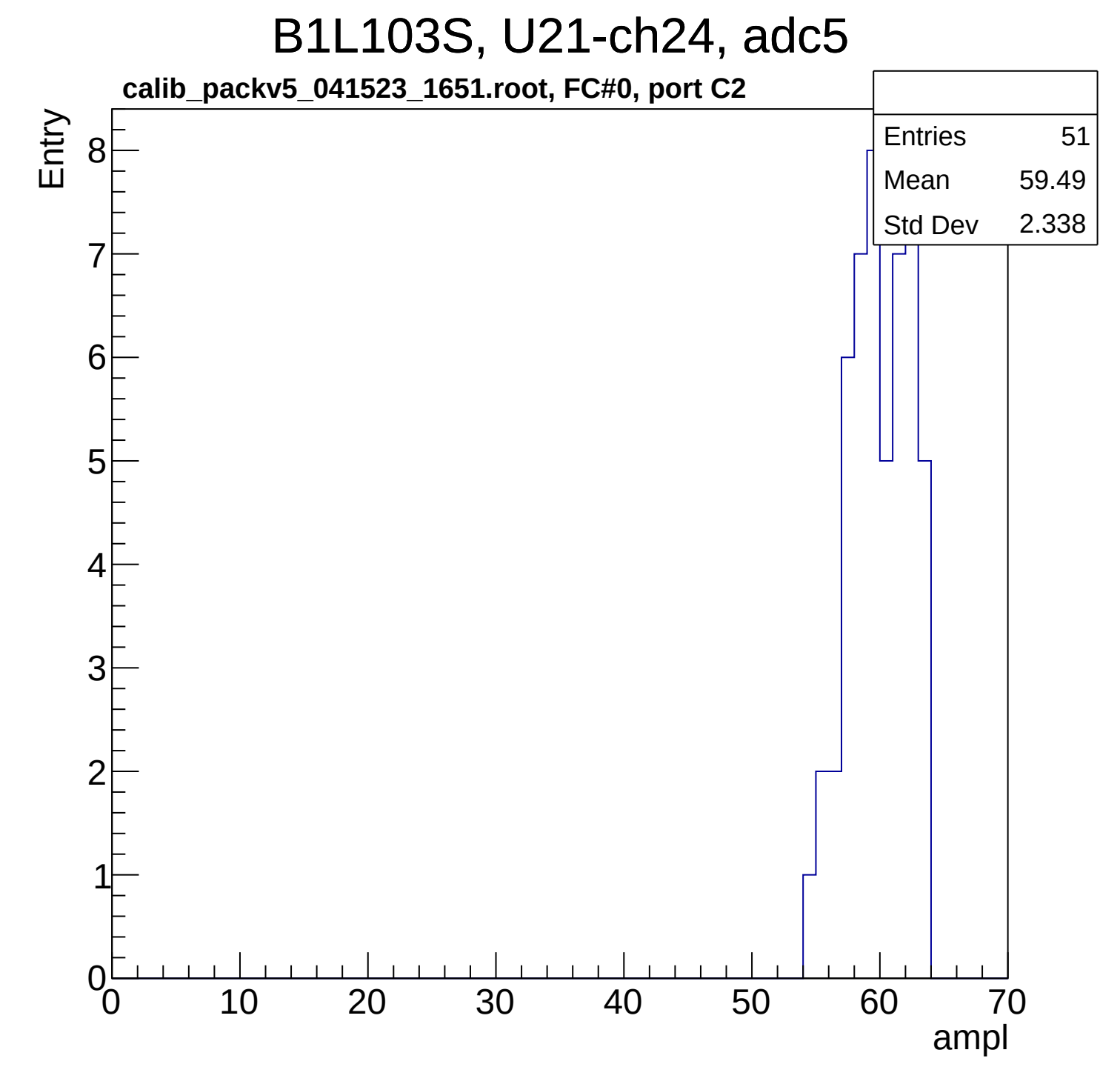
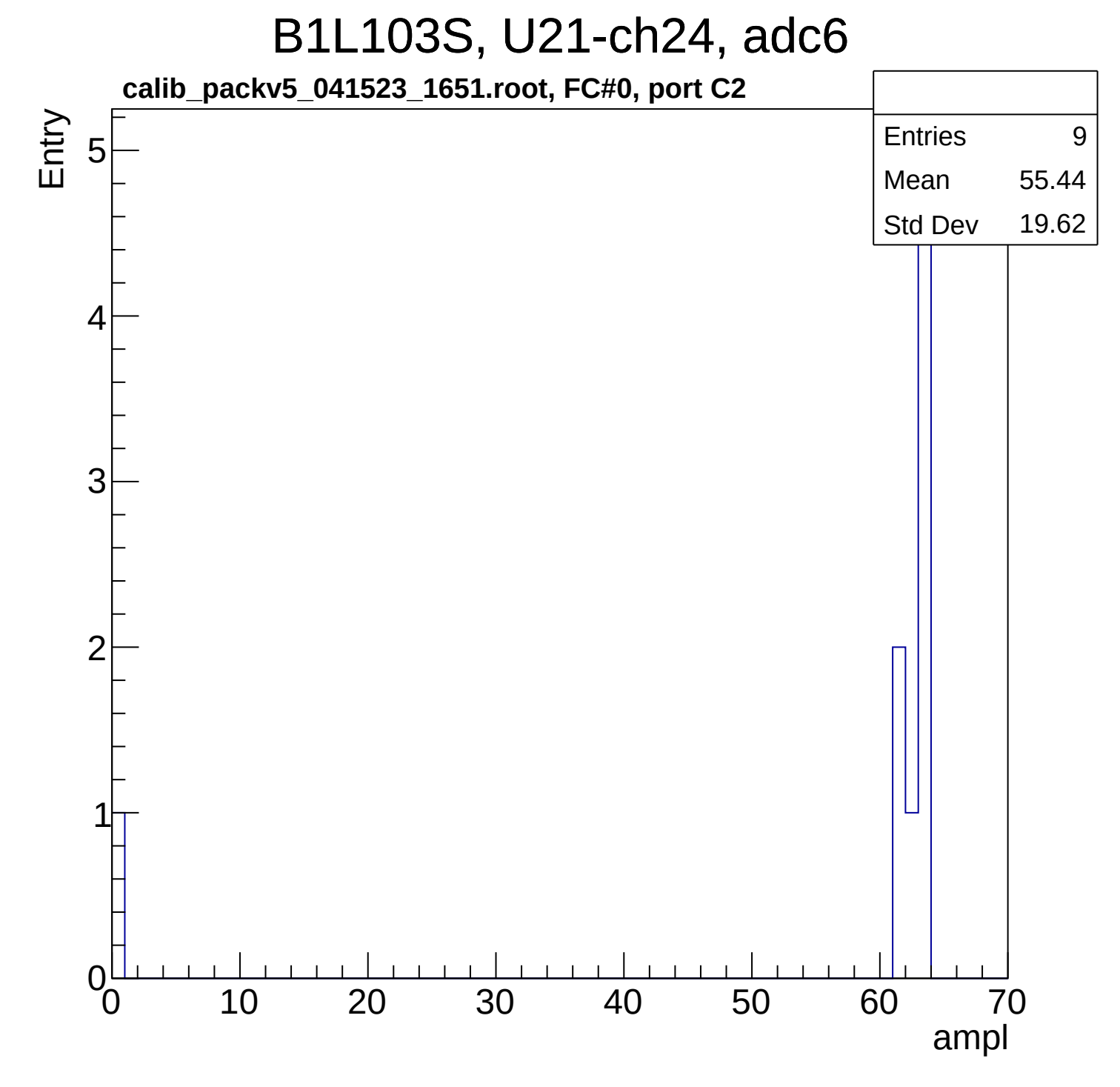
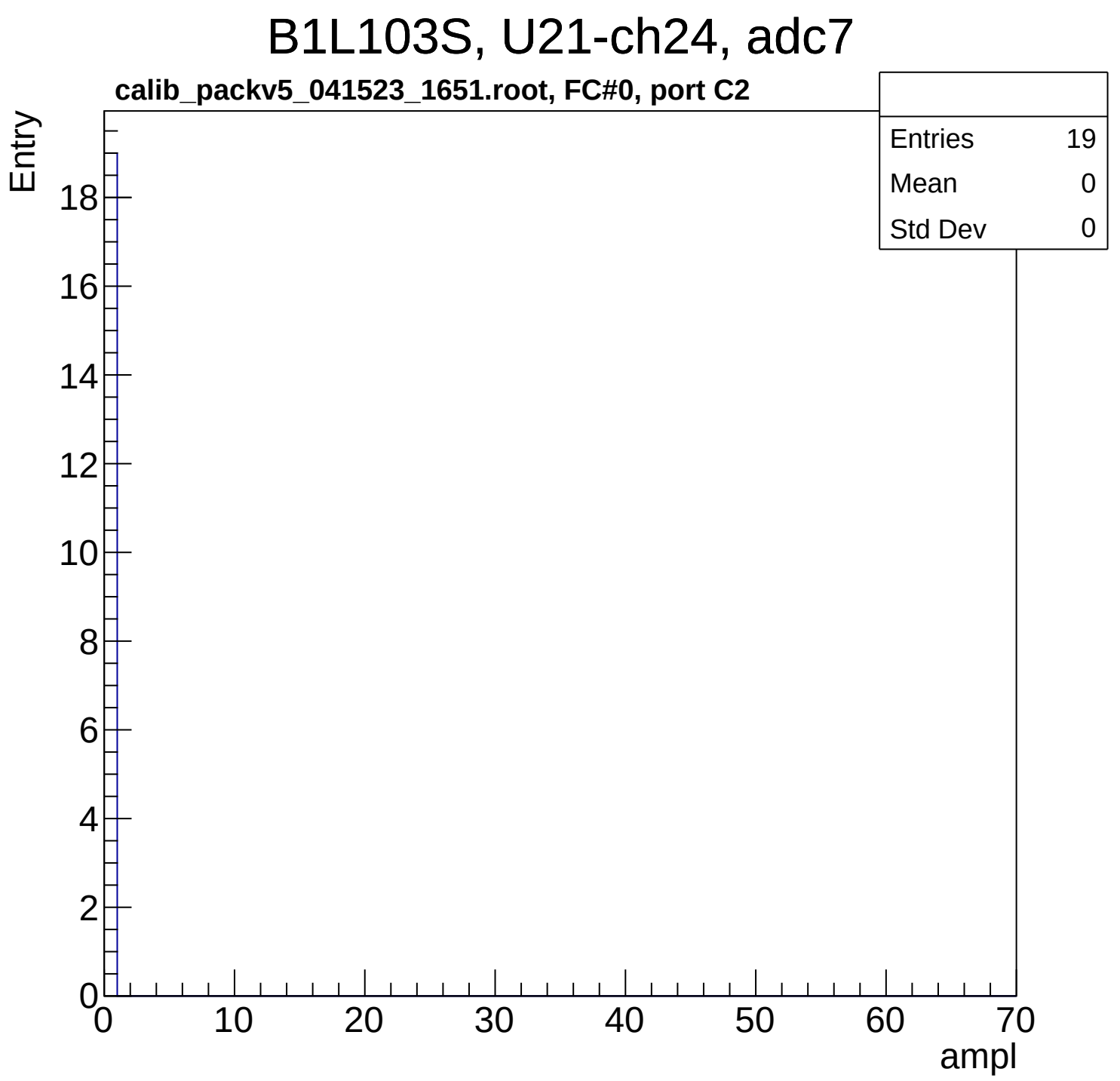
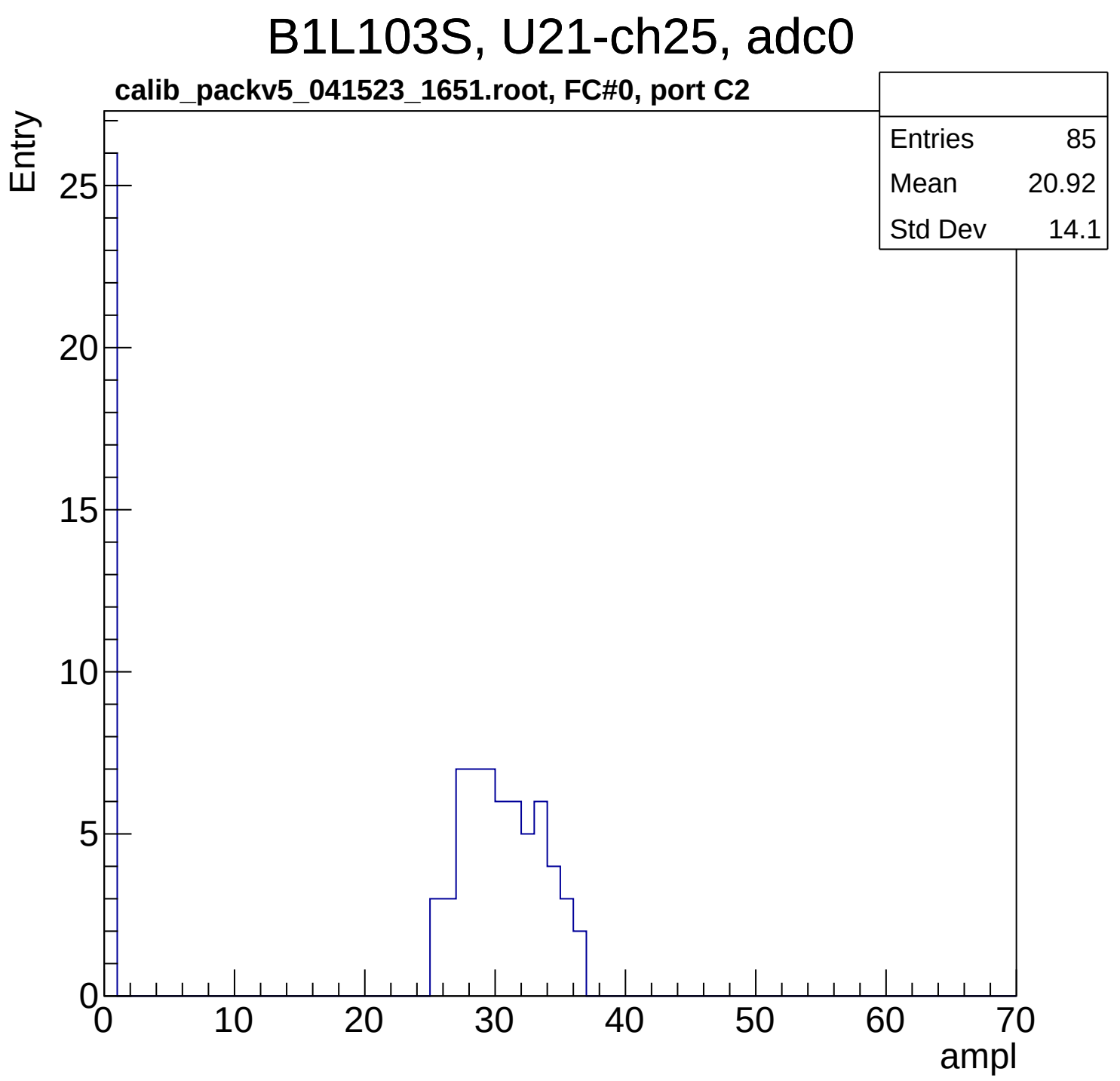

B1L103S, U21-ch24, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 49.48
Std Dev 2.706
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

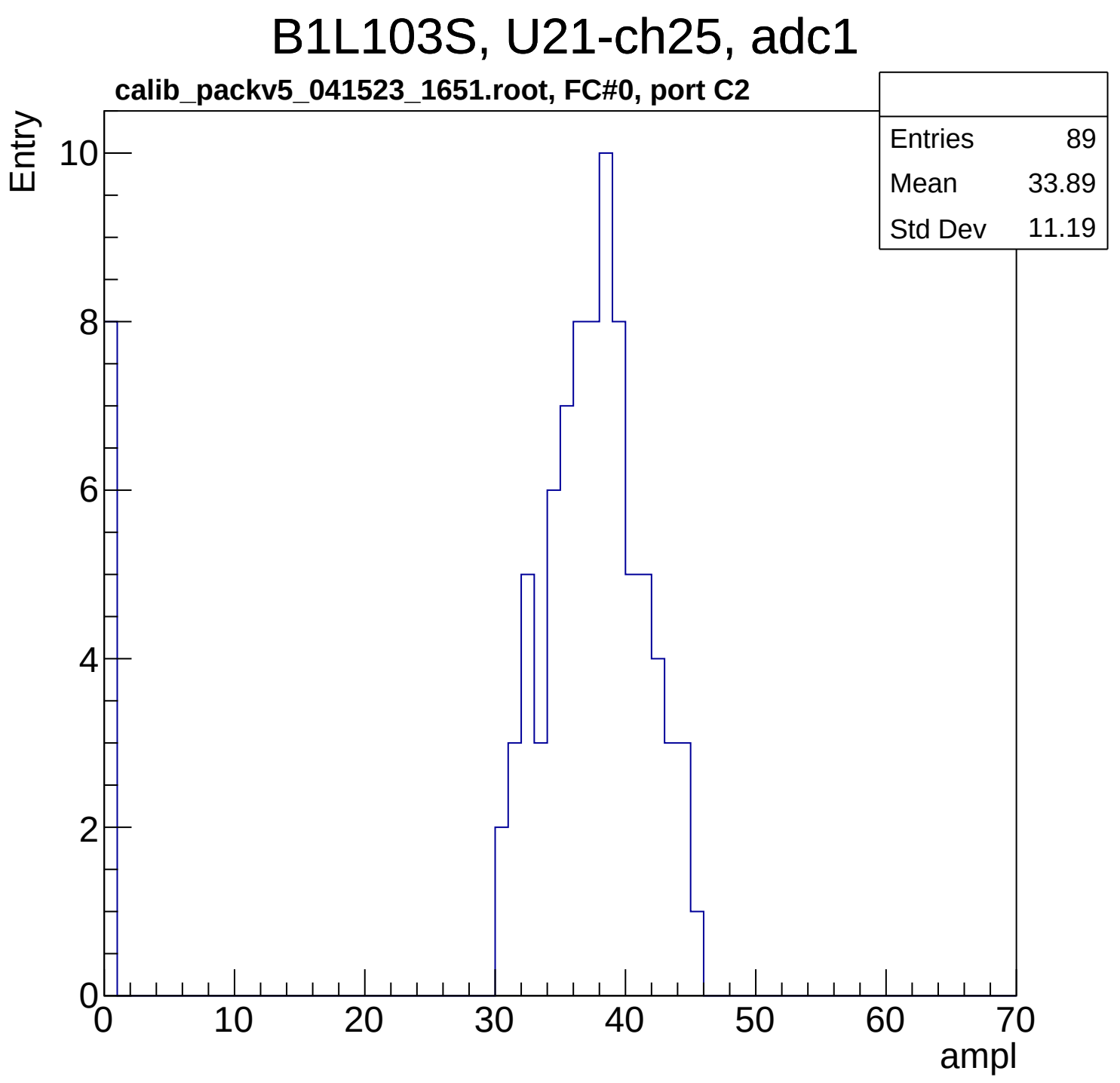

B1L103S, U21-ch24, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 55.29
Std Dev 3.053
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

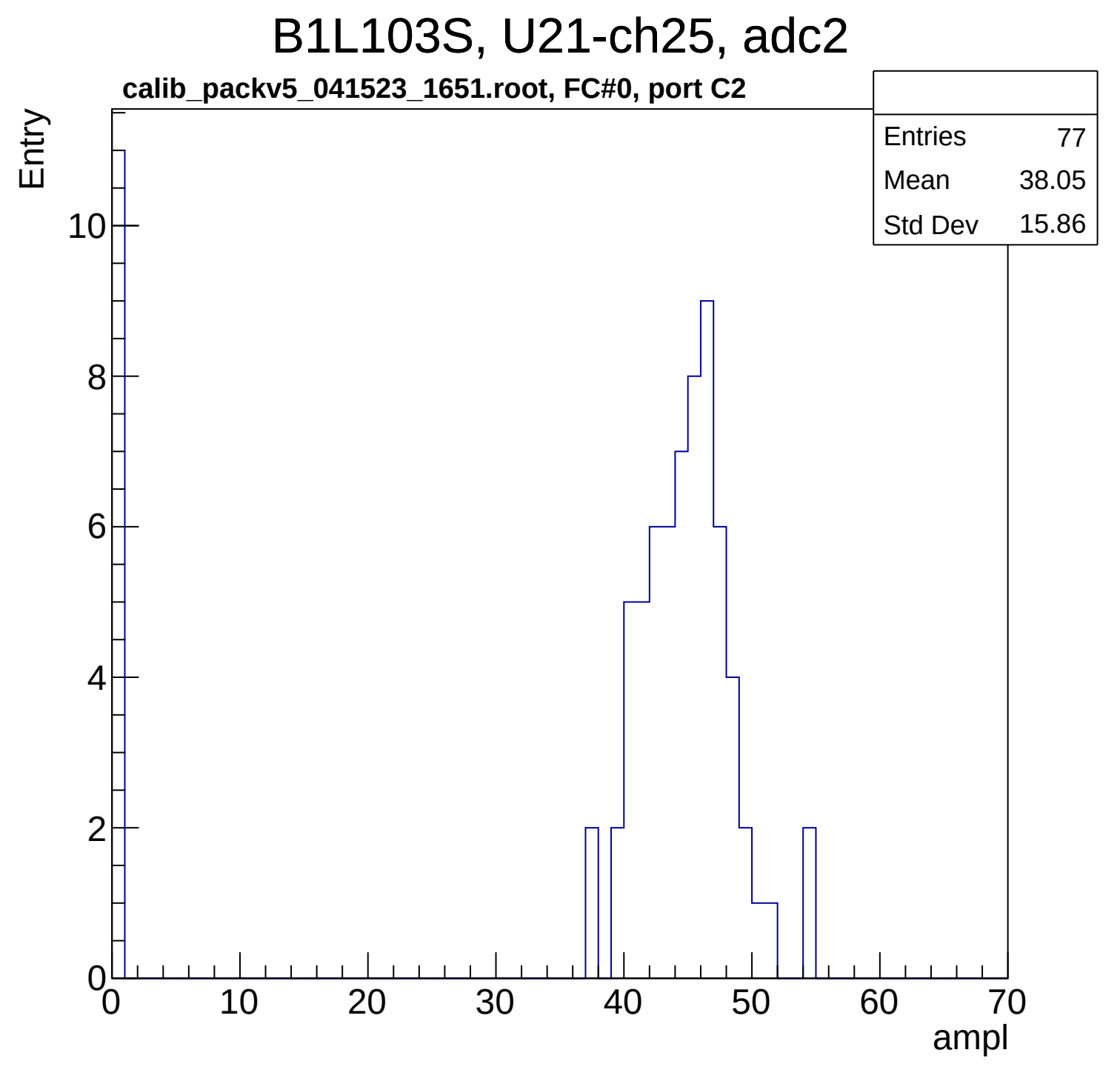

B1L103S, U21-ch24, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 59.49
Std Dev 2.338
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

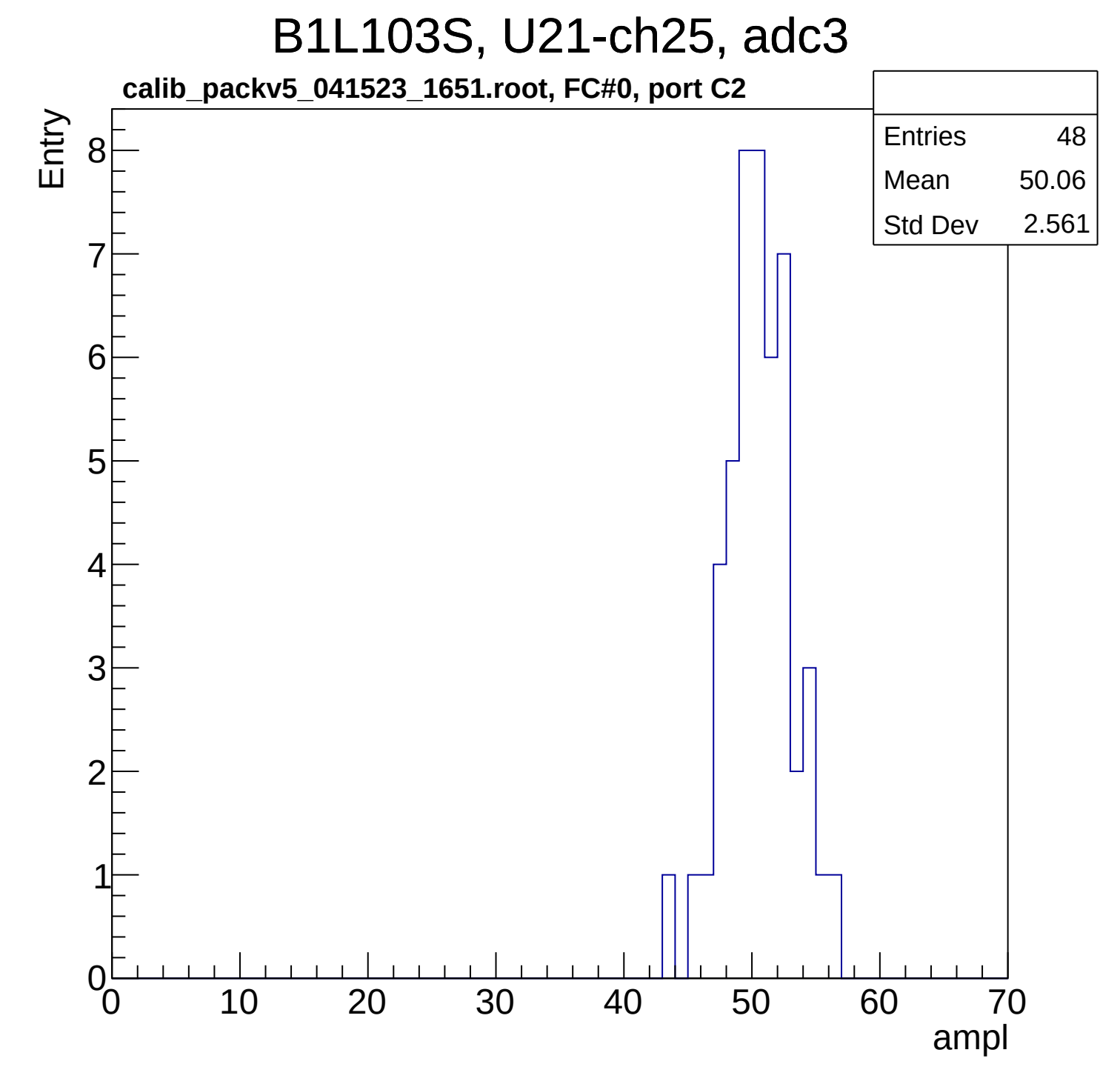

B1L103S, U21-ch24, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 55.44
Std Dev 19.62
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch24, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch25, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 20.92
Std Dev 14.1
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch25, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 33.89
Std Dev 11.19
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U21-ch25, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 38.05
Std Dev 15.86
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch25, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 50.06
Std Dev 2.561
Entry
ampl
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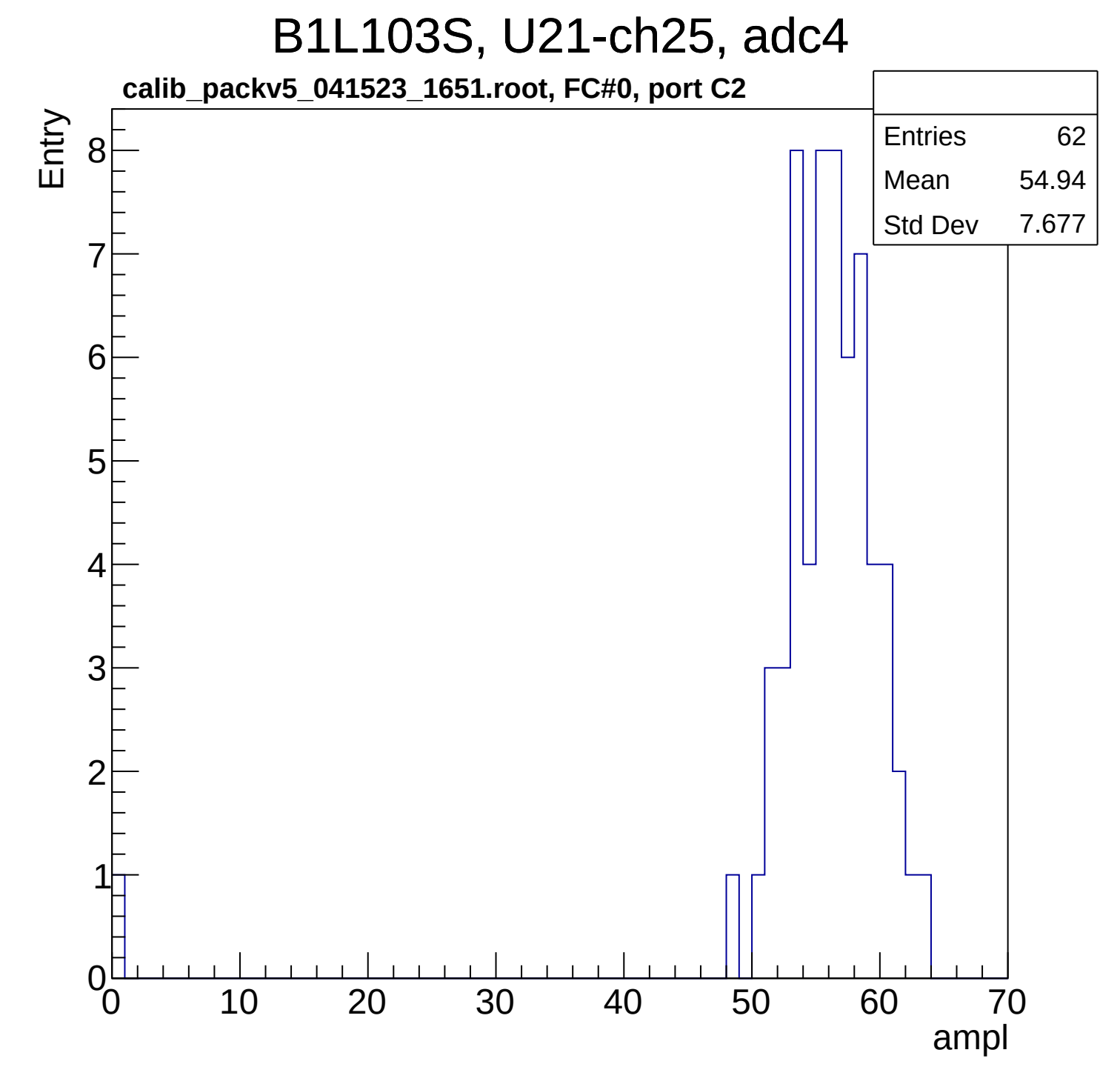
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch25, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 54.94
Std Dev 7.677
Entry
ampl
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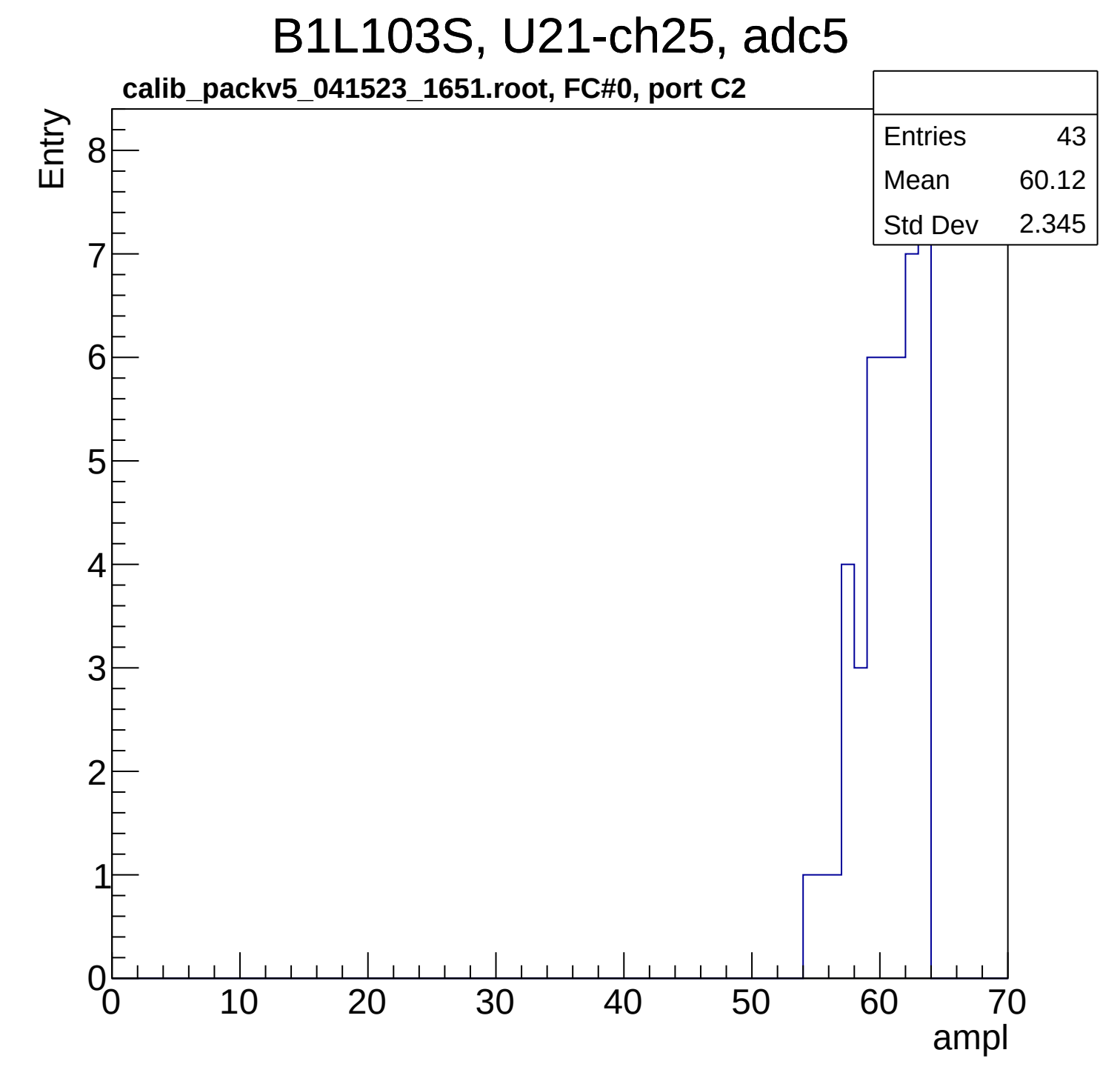
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch25, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 60.12
Std Dev 2.345
Entry
ampl
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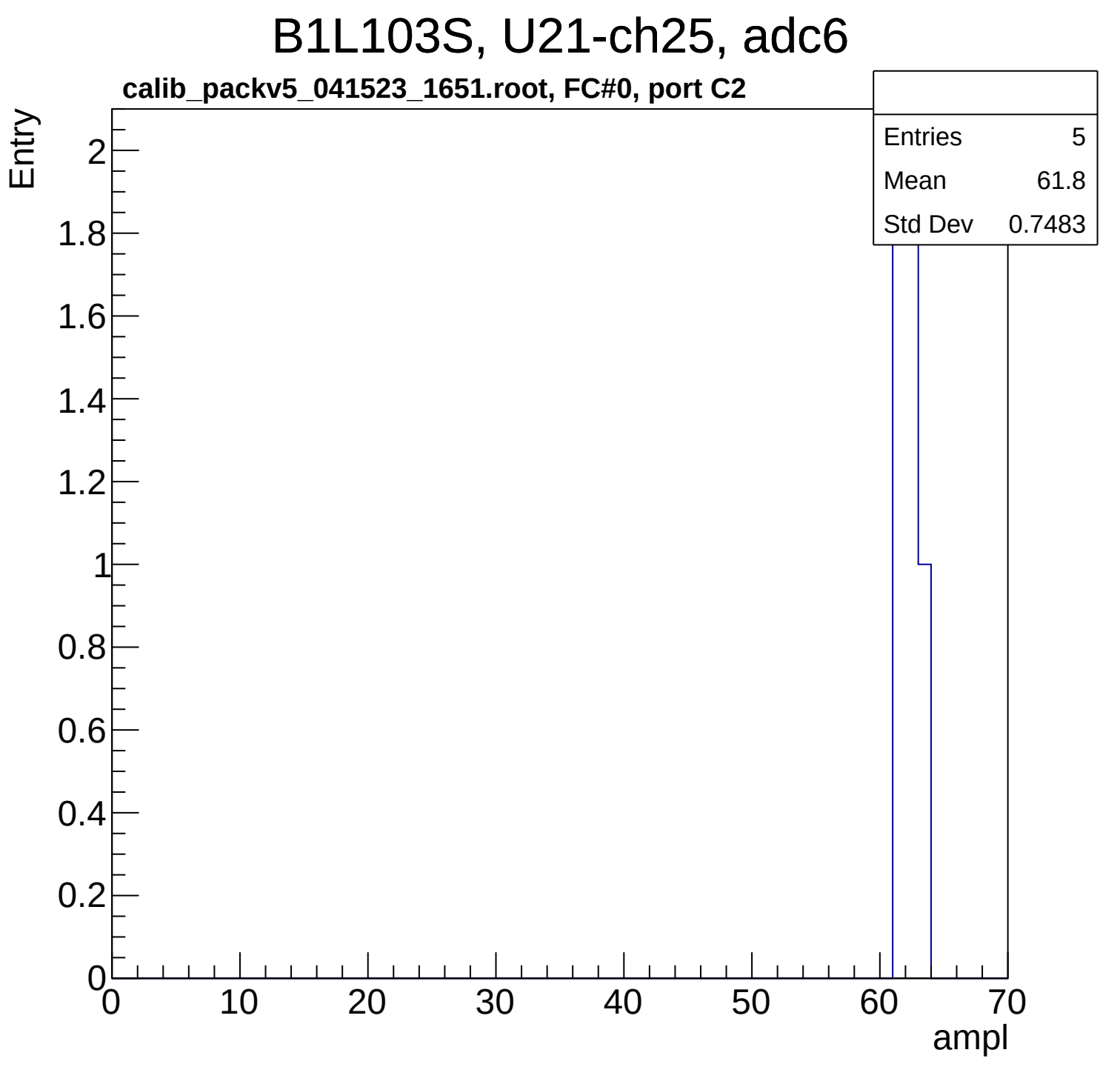
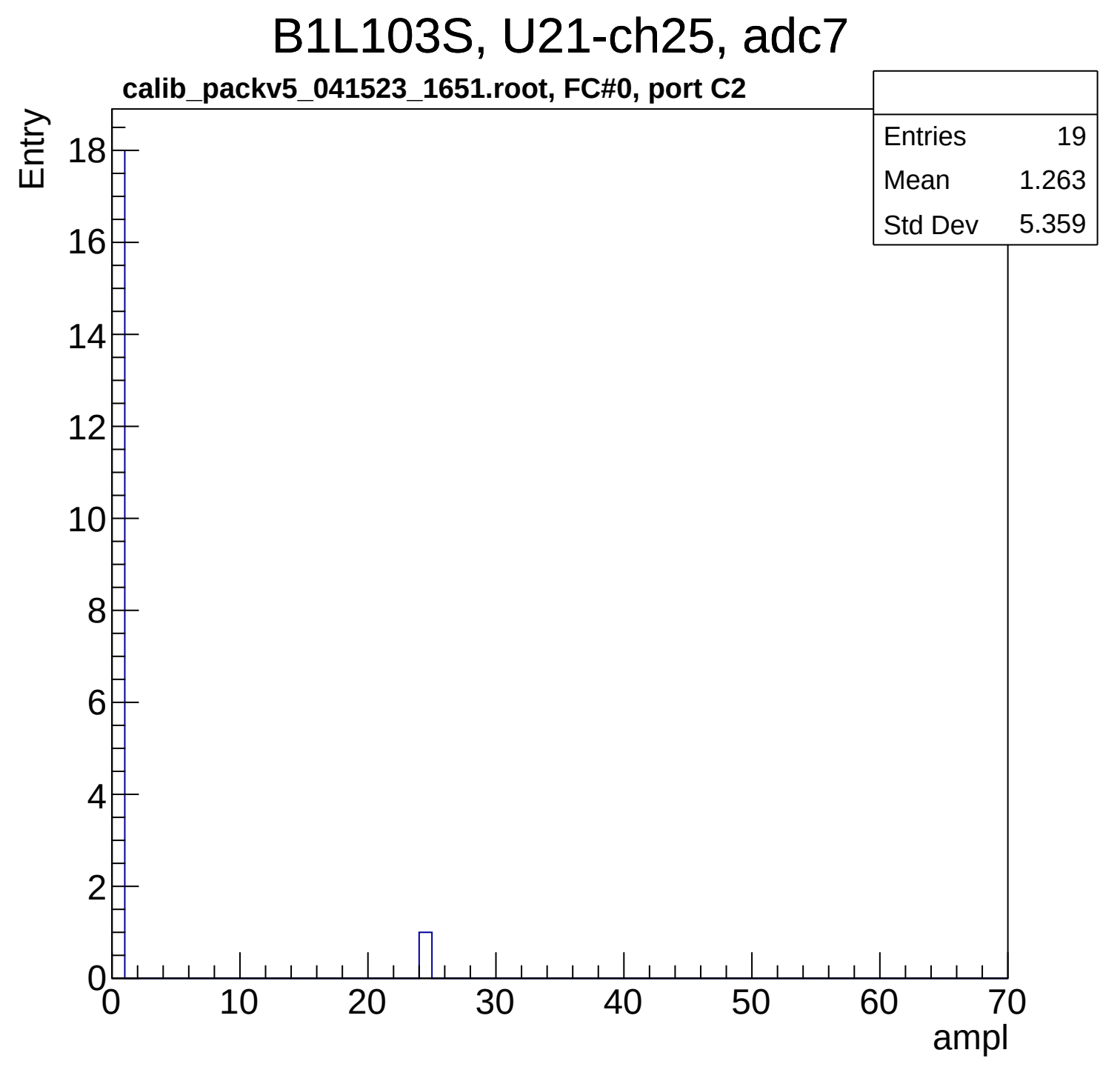
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch25, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 61.8
Std Dev 0.7483
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U21-ch25, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.263
Std Dev 5.359
Entry
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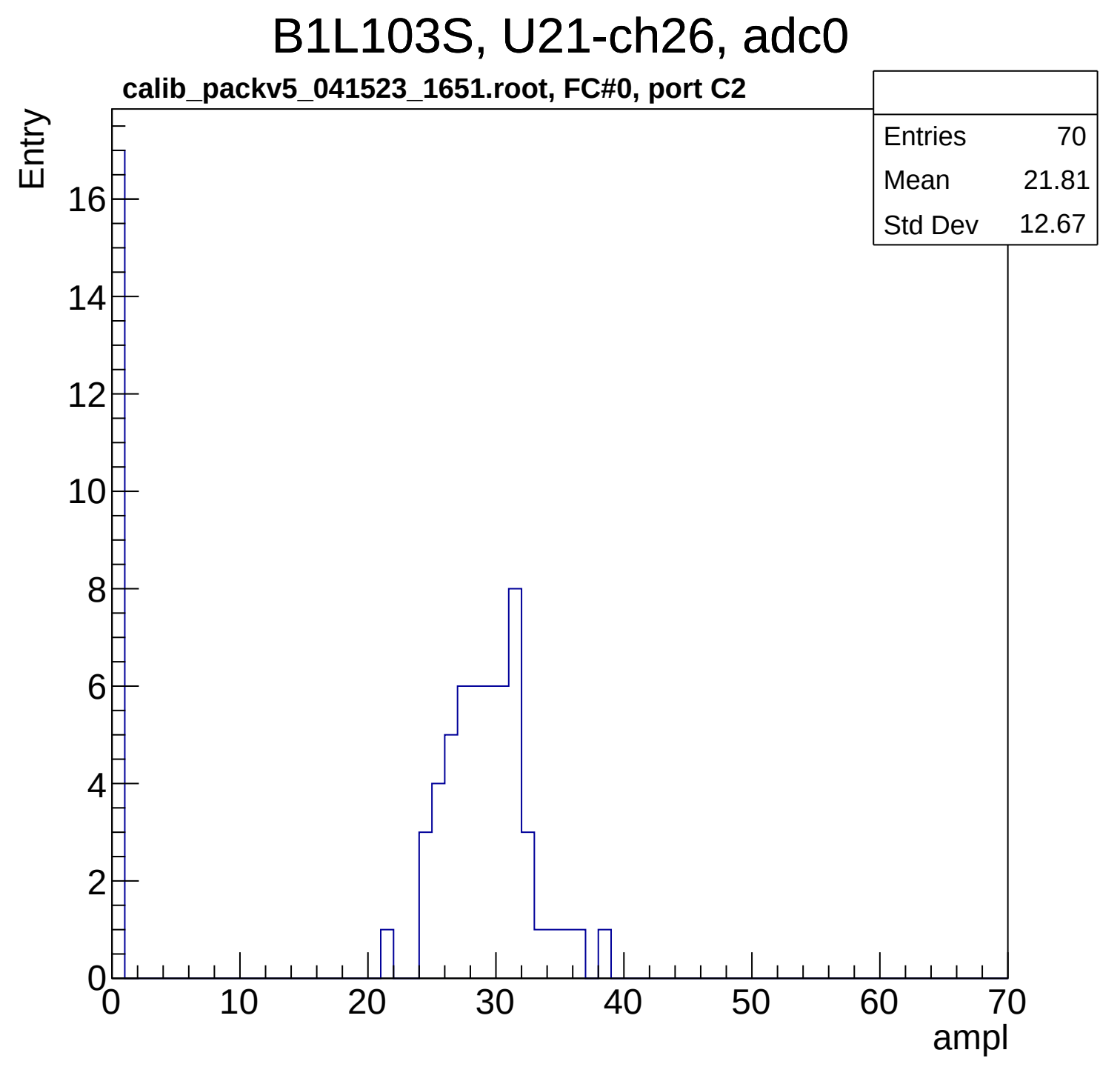
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch26, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 21.81
Std Dev 12.67
Entry
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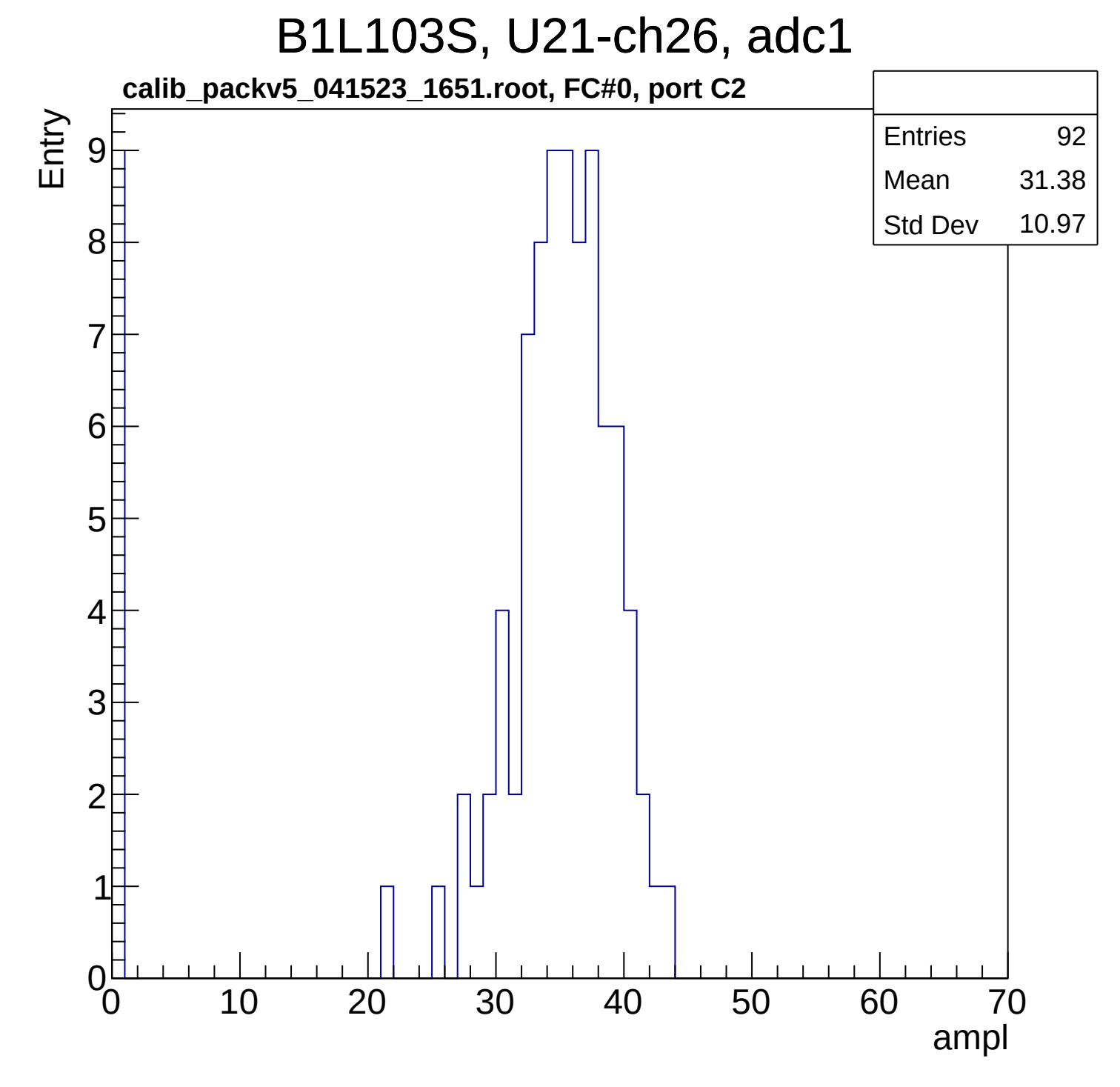
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch26, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 31.38
Std Dev 10.97
Entry
ampl
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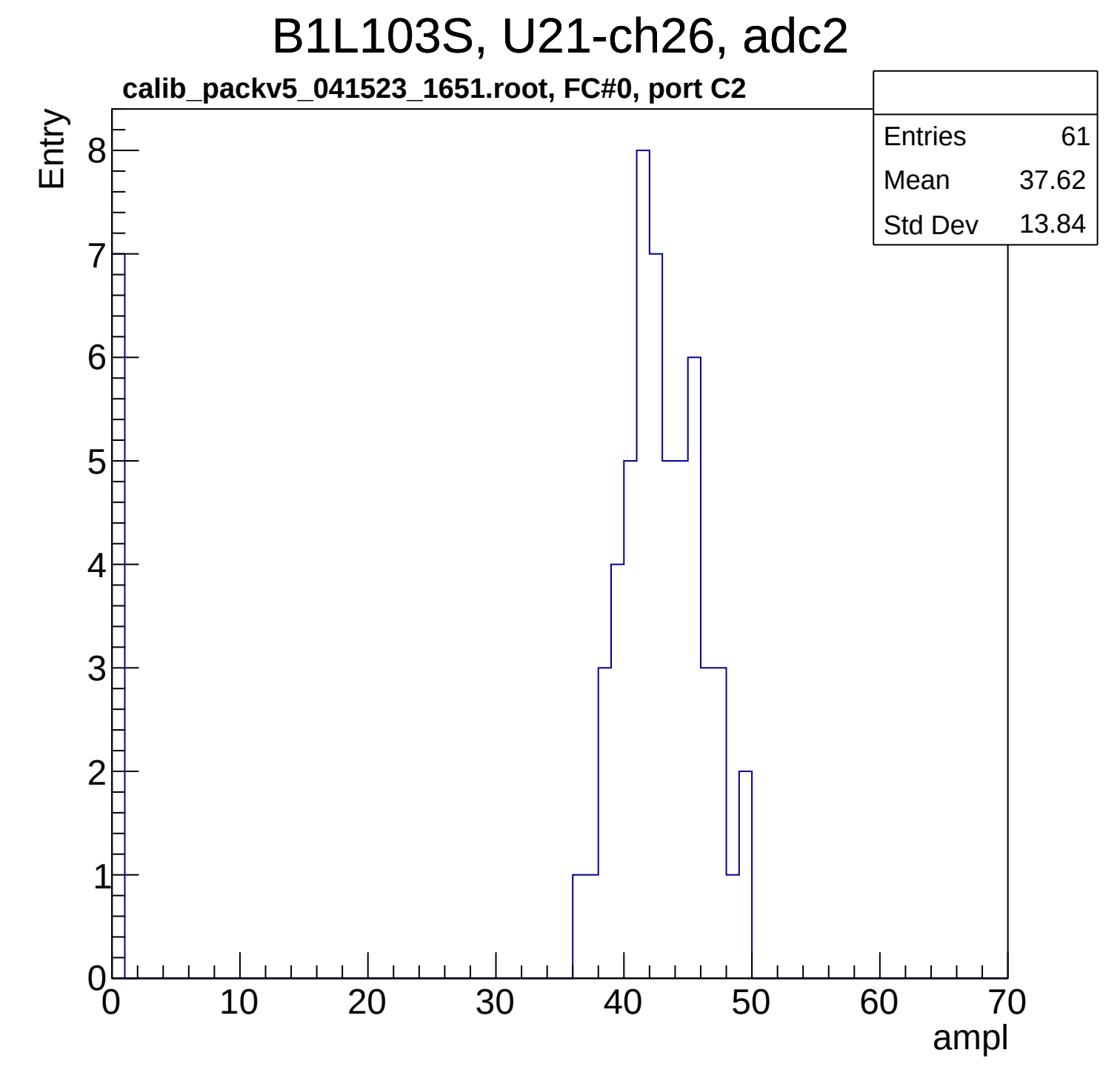
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch26, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 37.62
Std Dev 13.84
Entry
ampl
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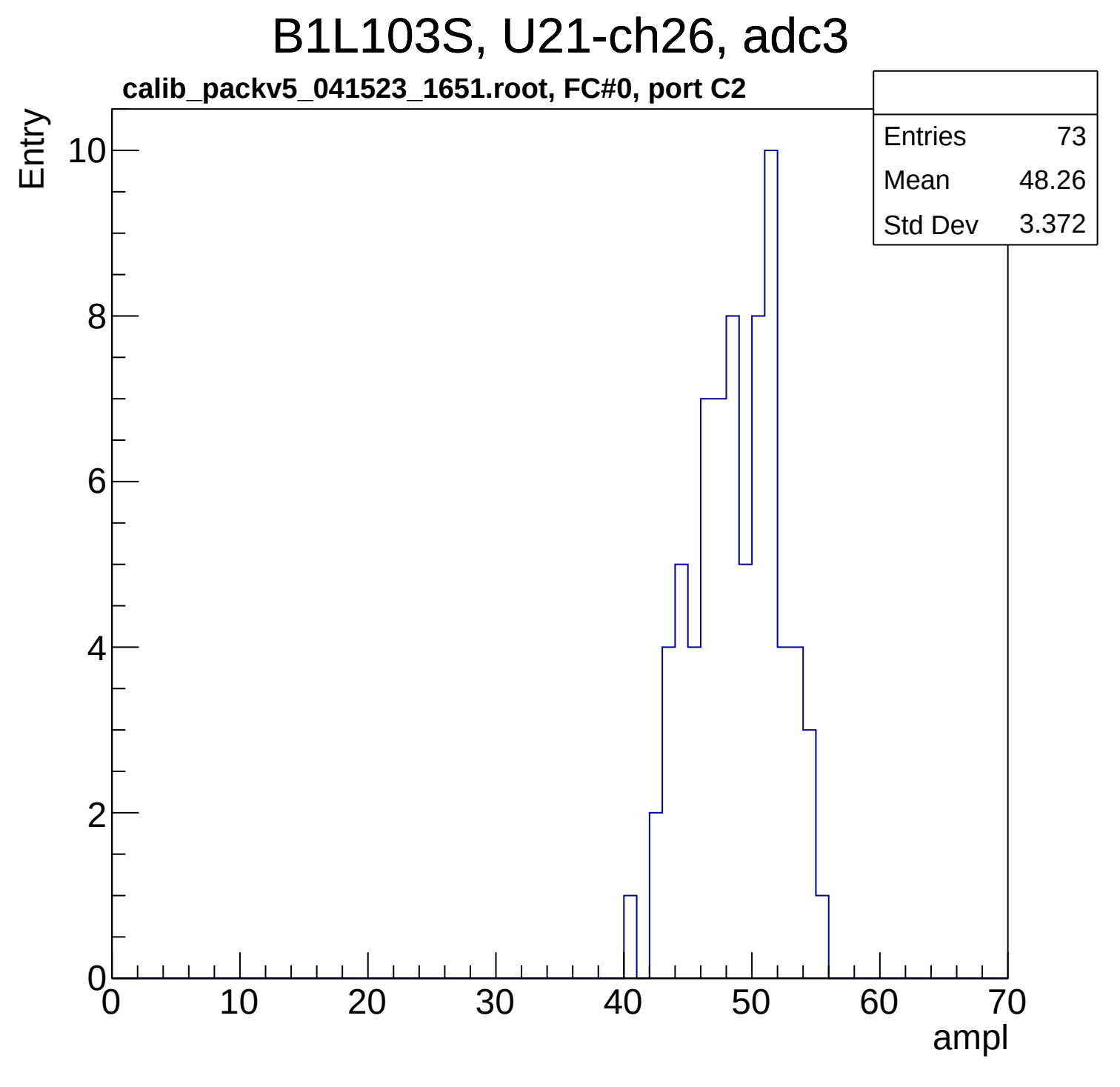
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch26, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 48.26
Std Dev 3.372
Entry
ampl
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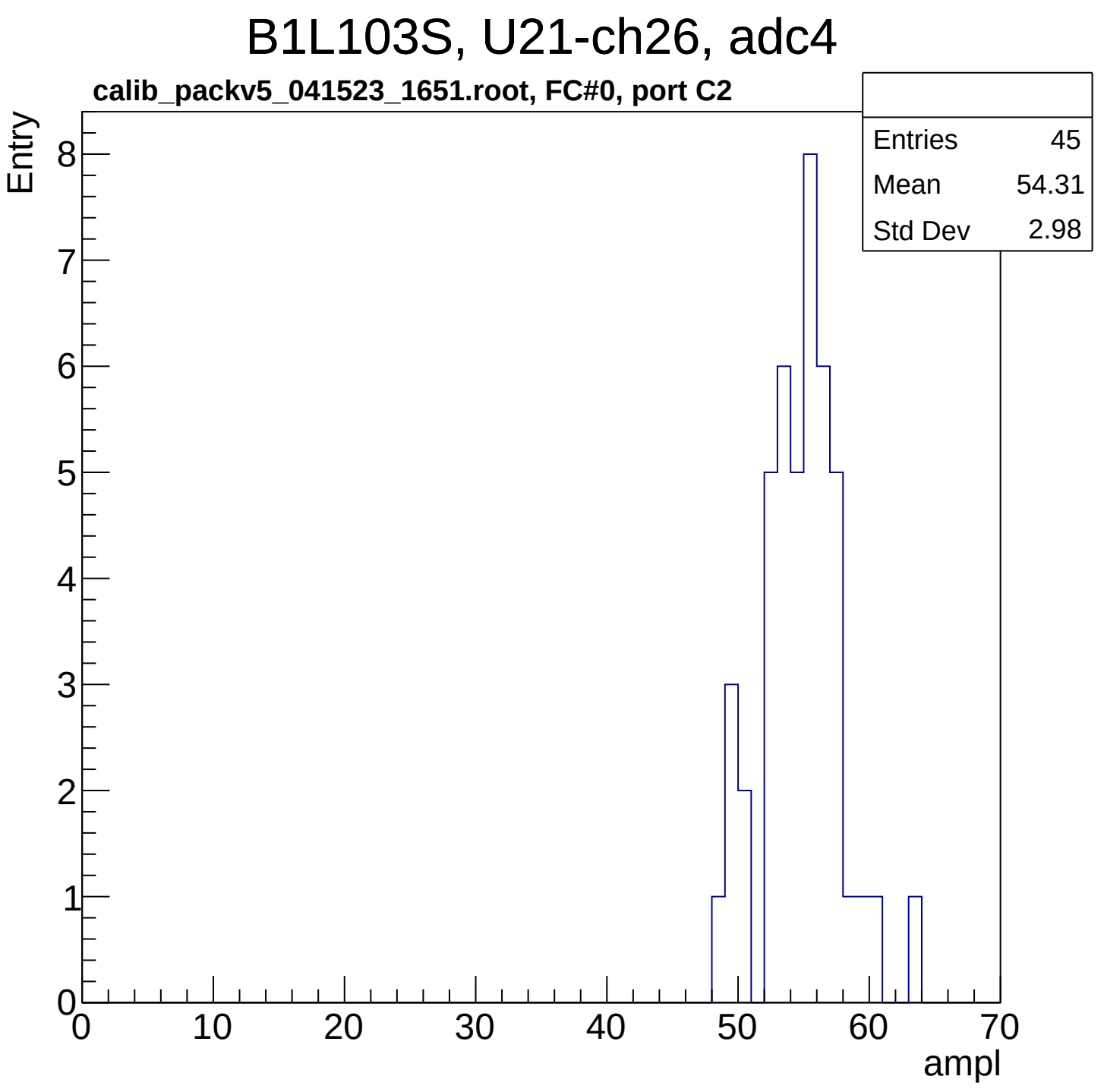
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U21-ch26, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 54.31
Std Dev 2.98
Entry
ampl
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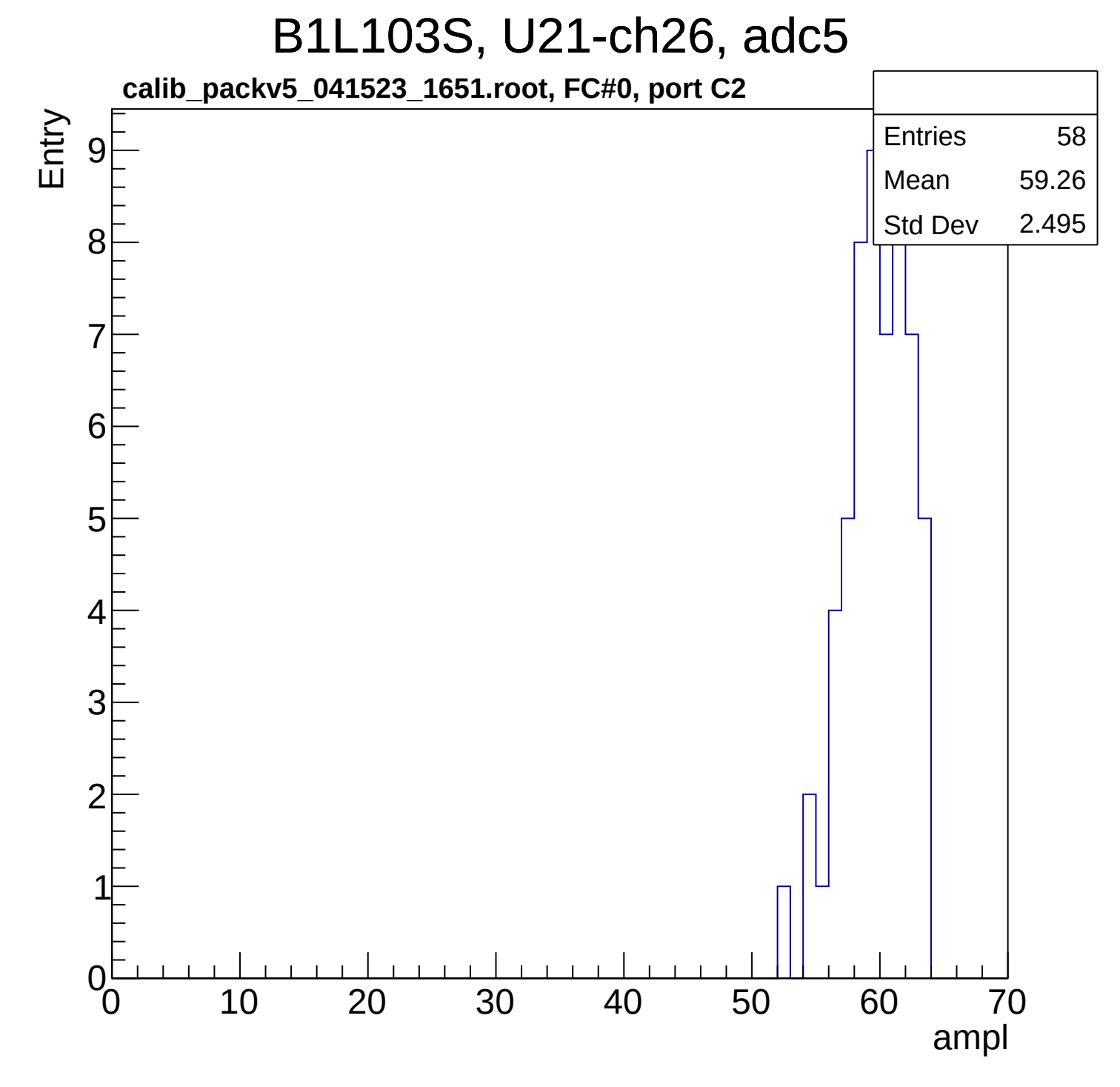
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch26, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 59.26
Std Dev 2.495
Entry
ampl
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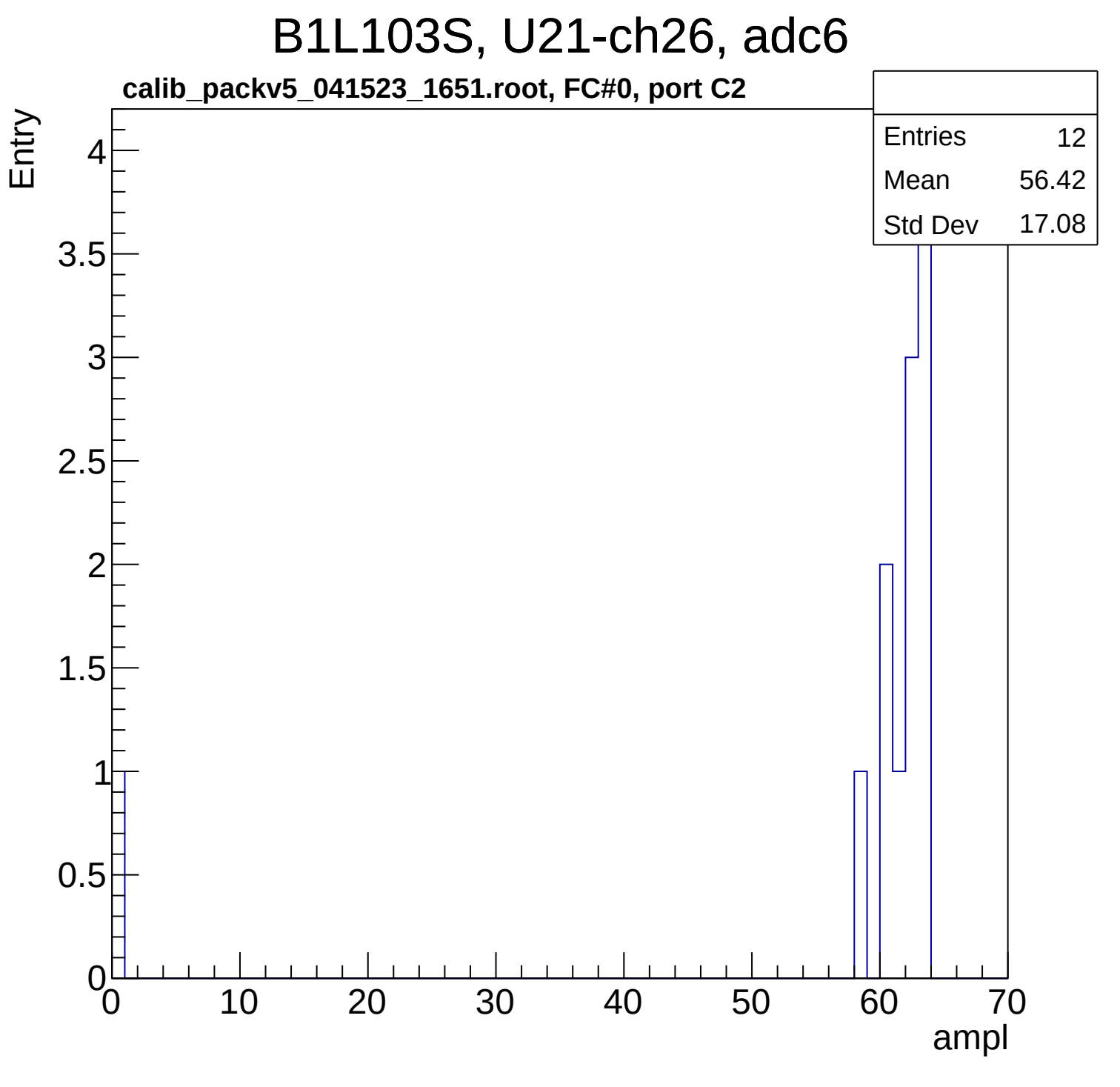
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch26, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 56.42
Std Dev 17.08
Entry
ampl
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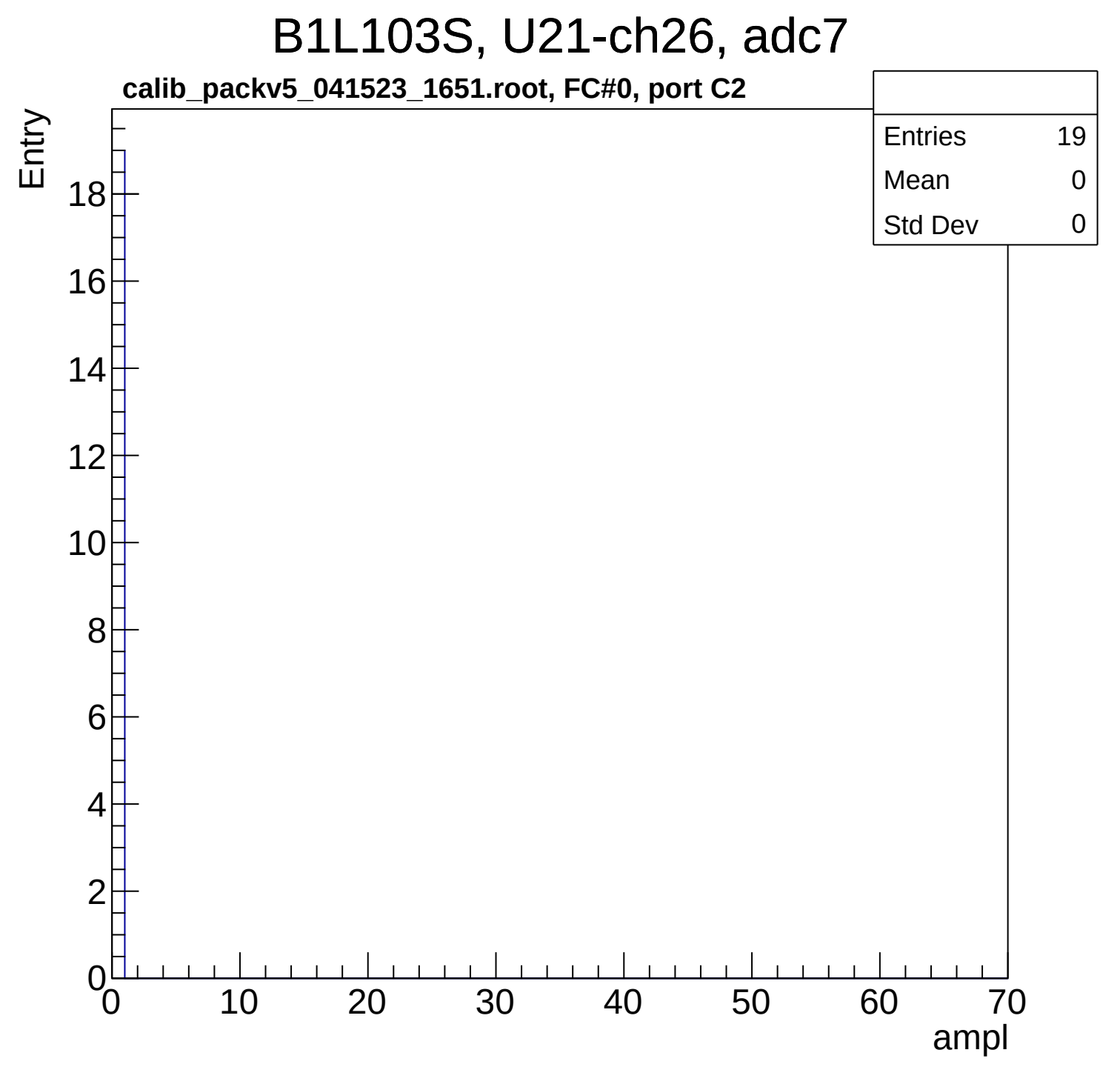
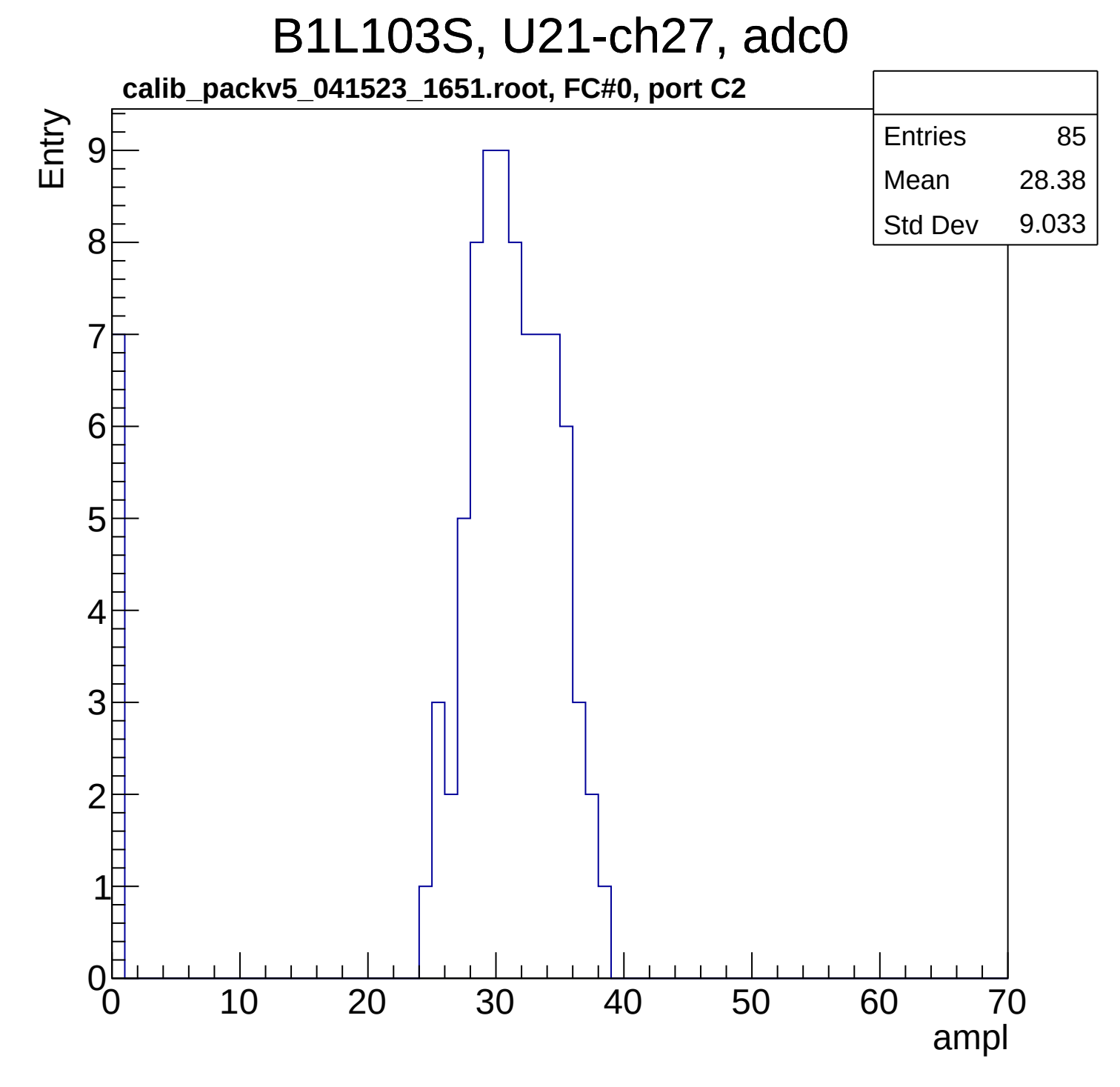
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U21-ch26, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch27, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 28.38
Std Dev 9.033
Entry
ampl
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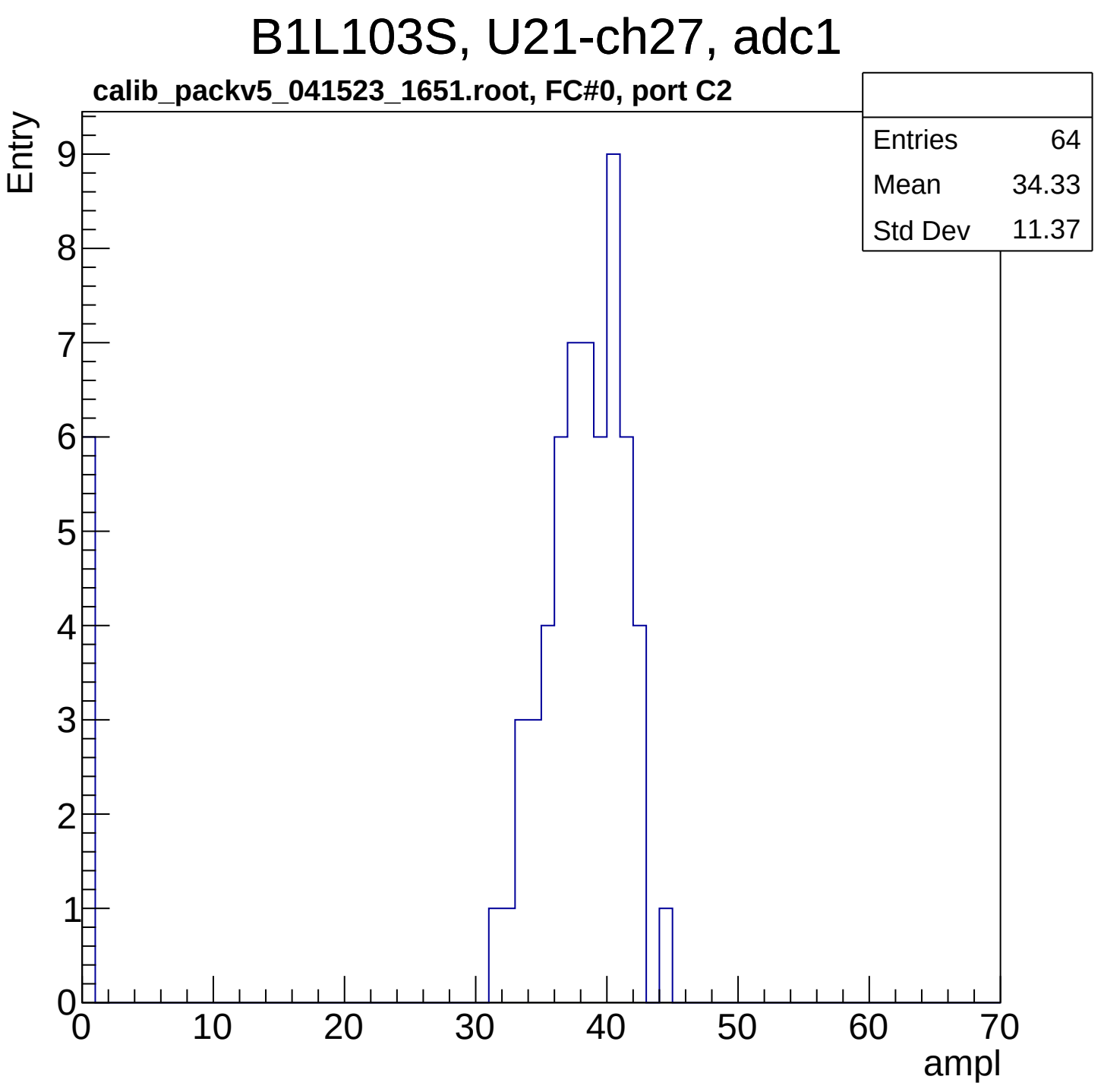
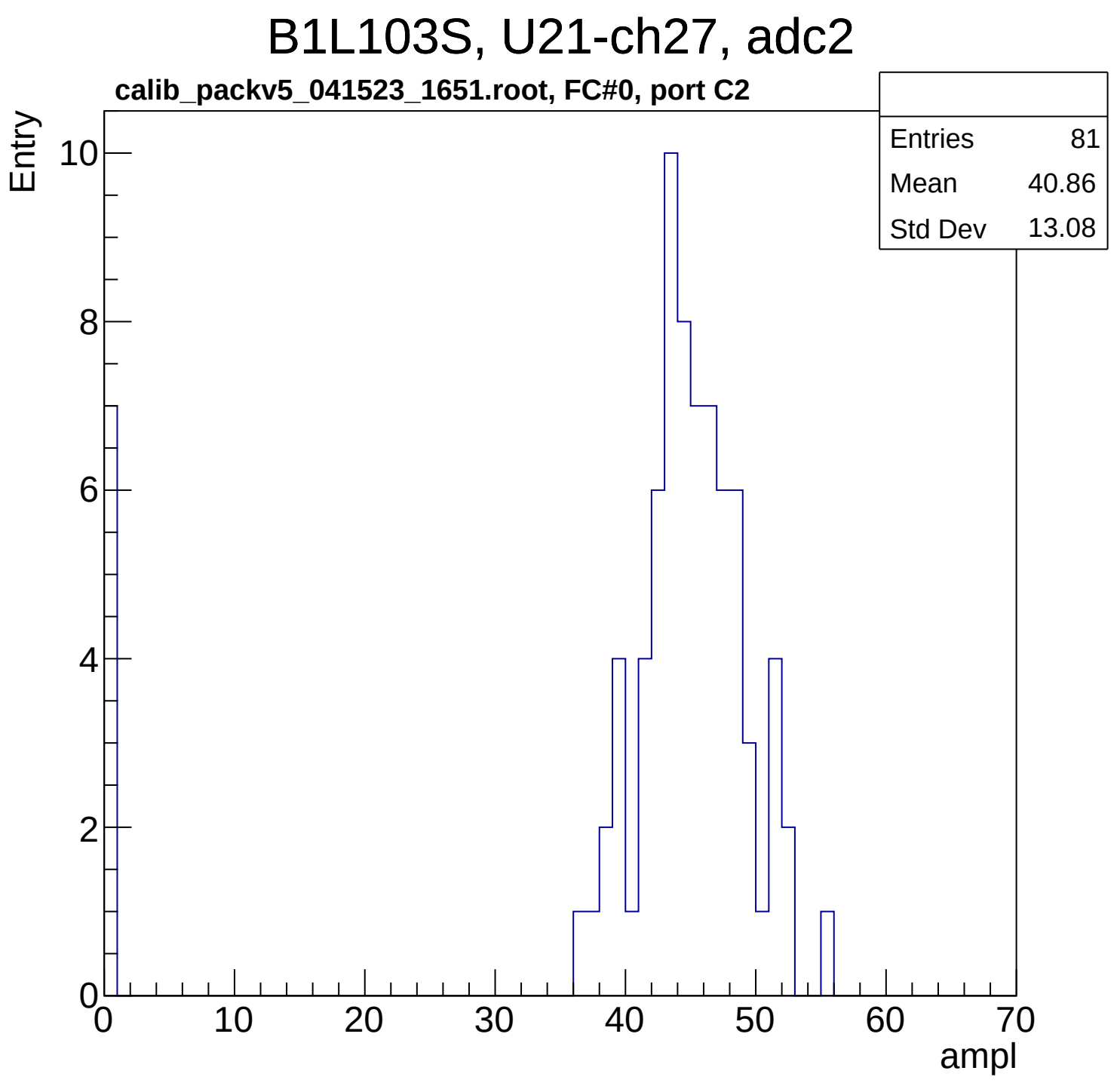
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch27, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 34.33
Std Dev 11.37
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch27, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 40.86
Std Dev 13.08
Entry
0
2
4
6
8
10
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50
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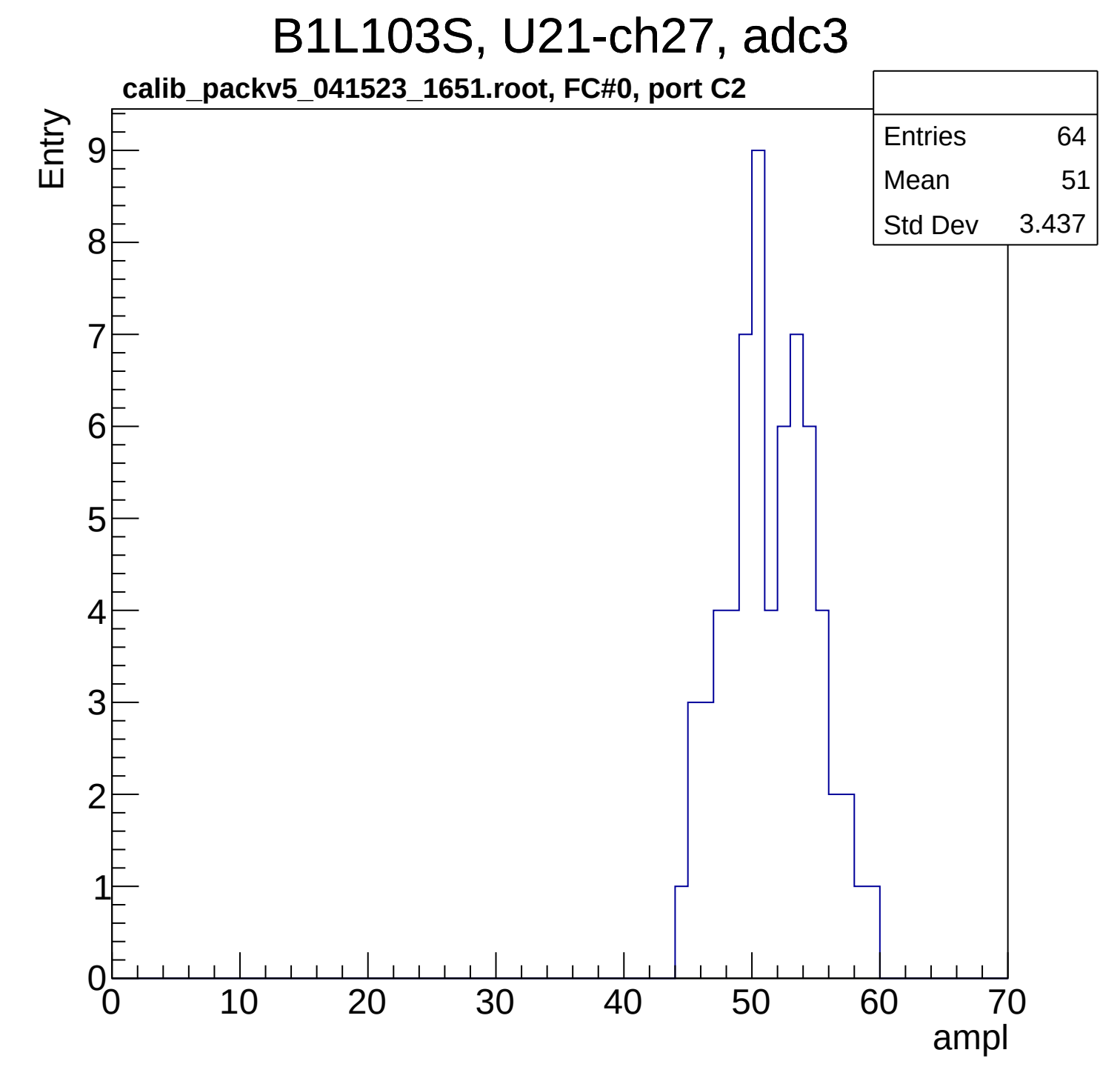
70
ampl


B1L103S, U21-ch27, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 51
Std Dev 3.437
Entry
ampl
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4
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0
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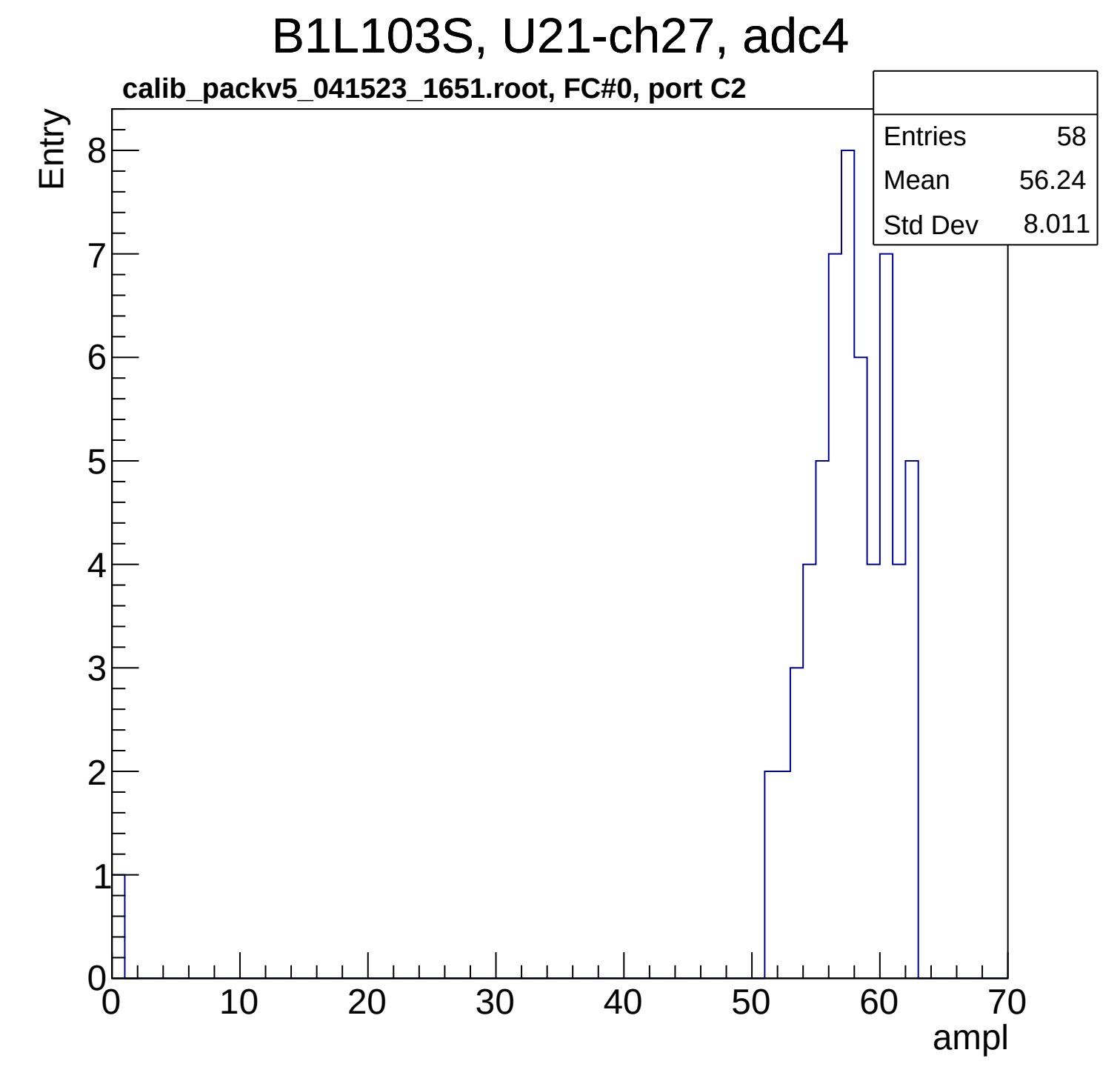
B1L103S, U21-ch27, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 56.24
Std Dev 8.011
Entry
ampl
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2
3
4
5
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7
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0
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40
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60
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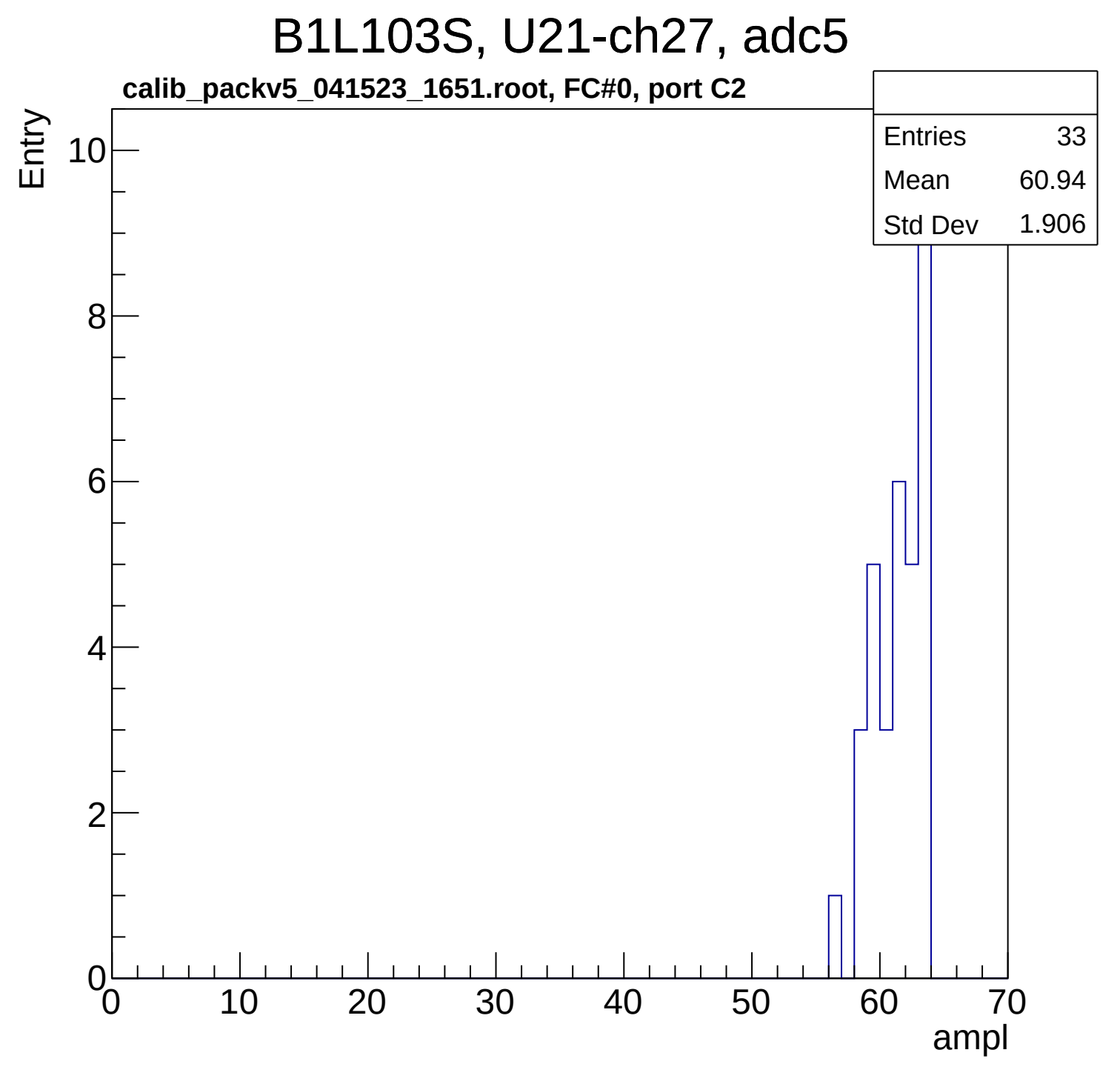
B1L103S, U21-ch27, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 60.94
Std Dev 1.906
Entry
ampl
0
2
4
6
8
10
0
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20
30
40
50
60
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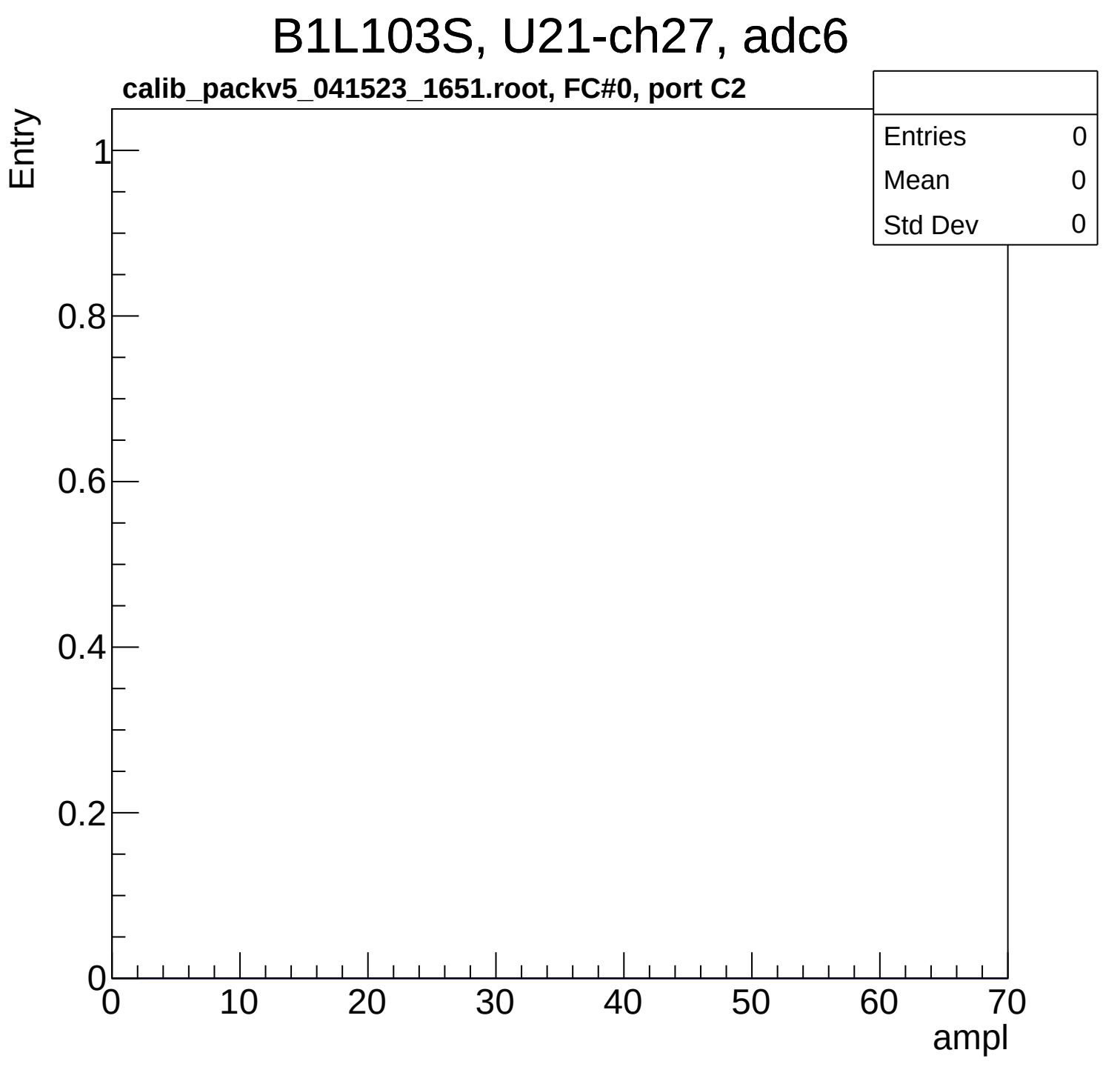
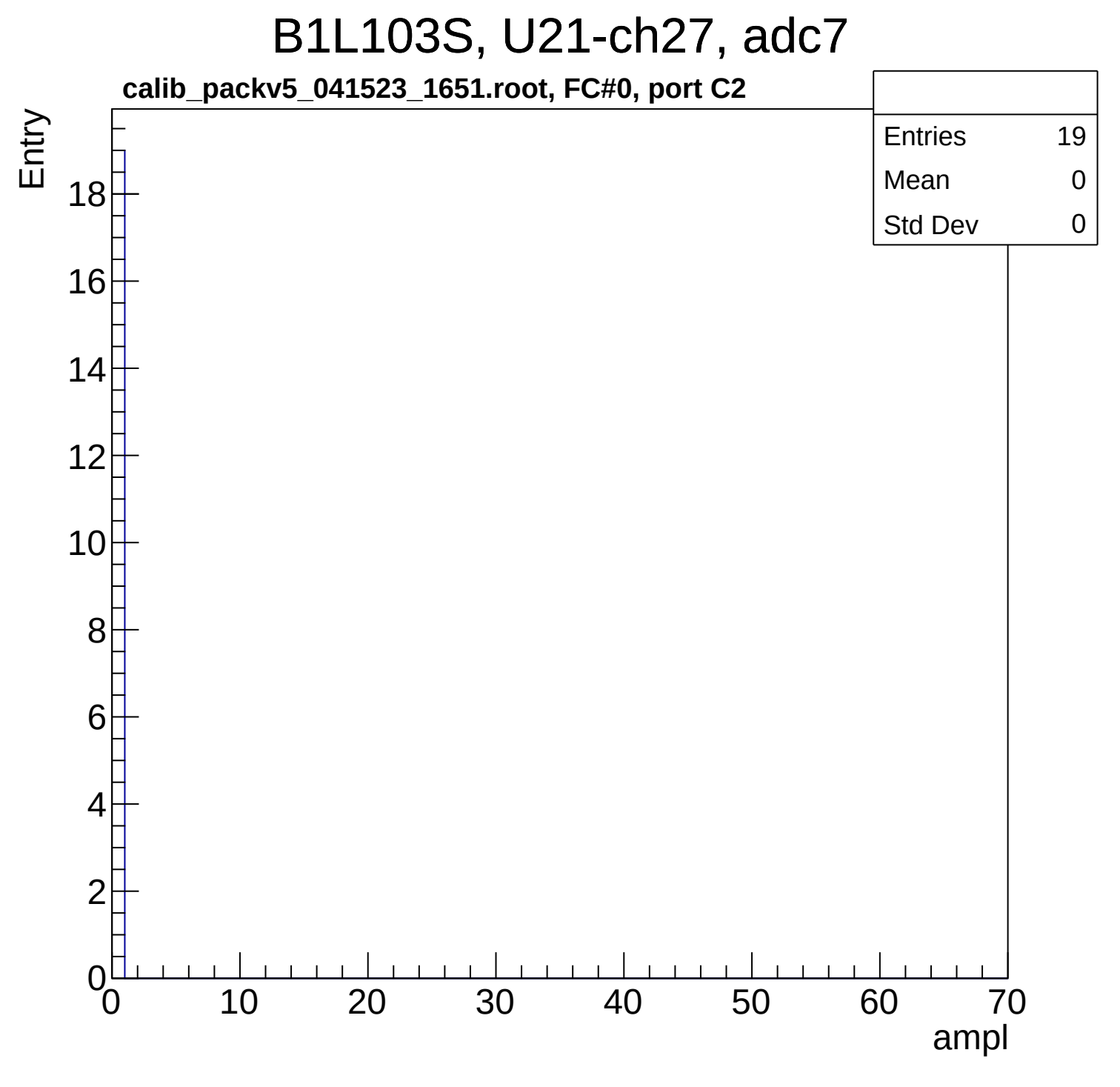
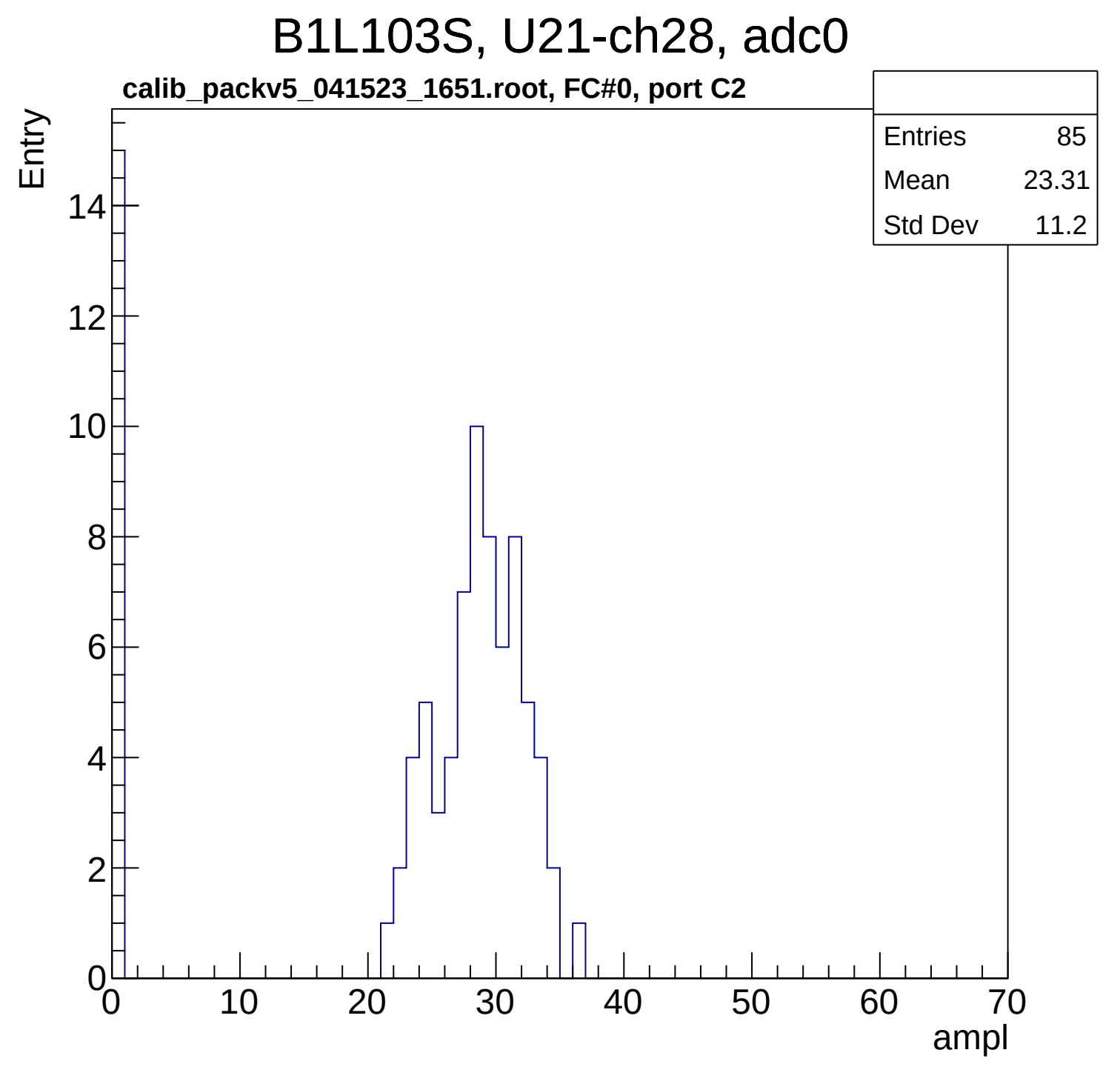

B1L103S, U21-ch27, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch27, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch28, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 23.31
Std Dev 11.2
Entry
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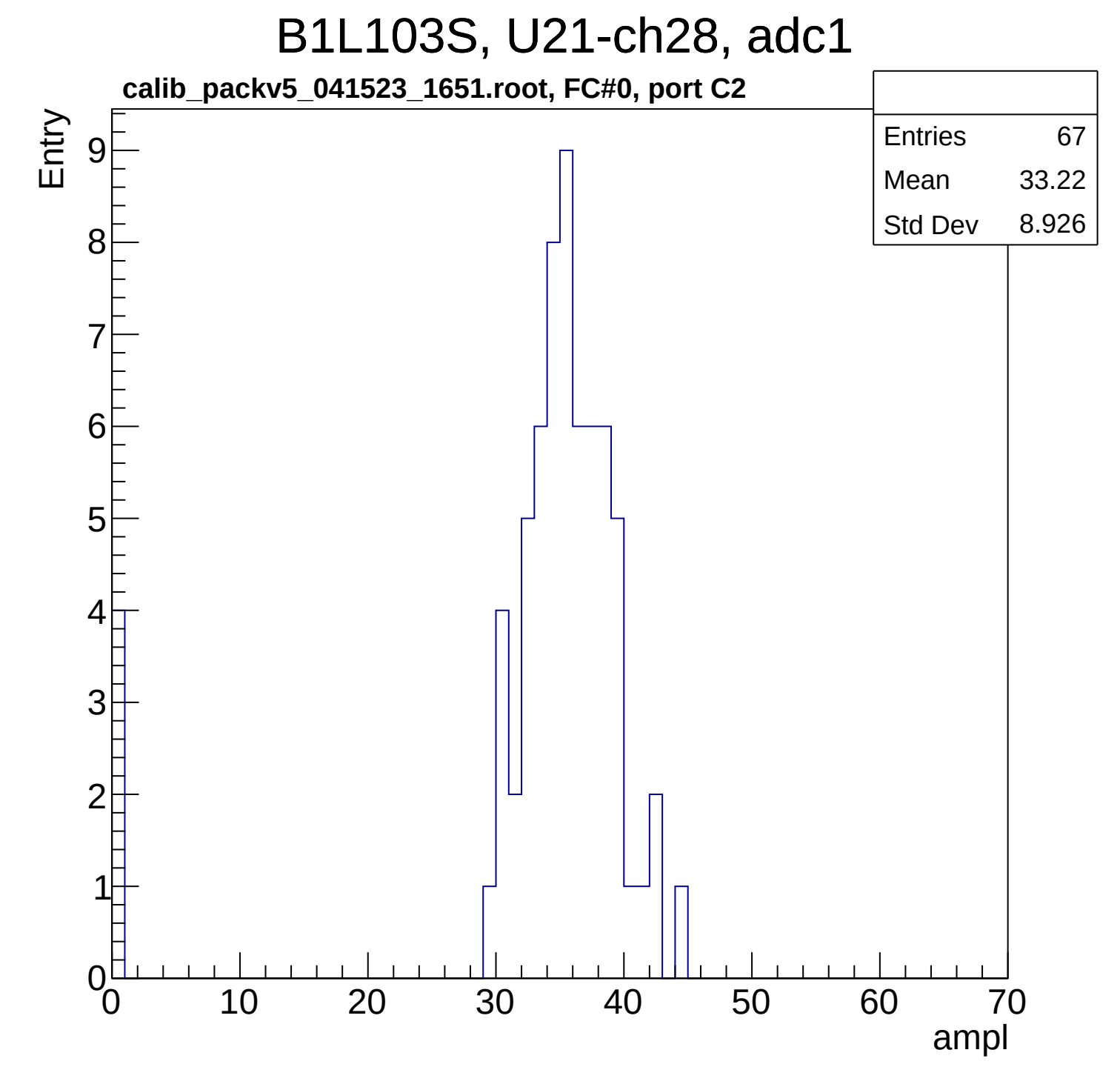
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch28, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 33.22
Std Dev 8.926
Entry
ampl
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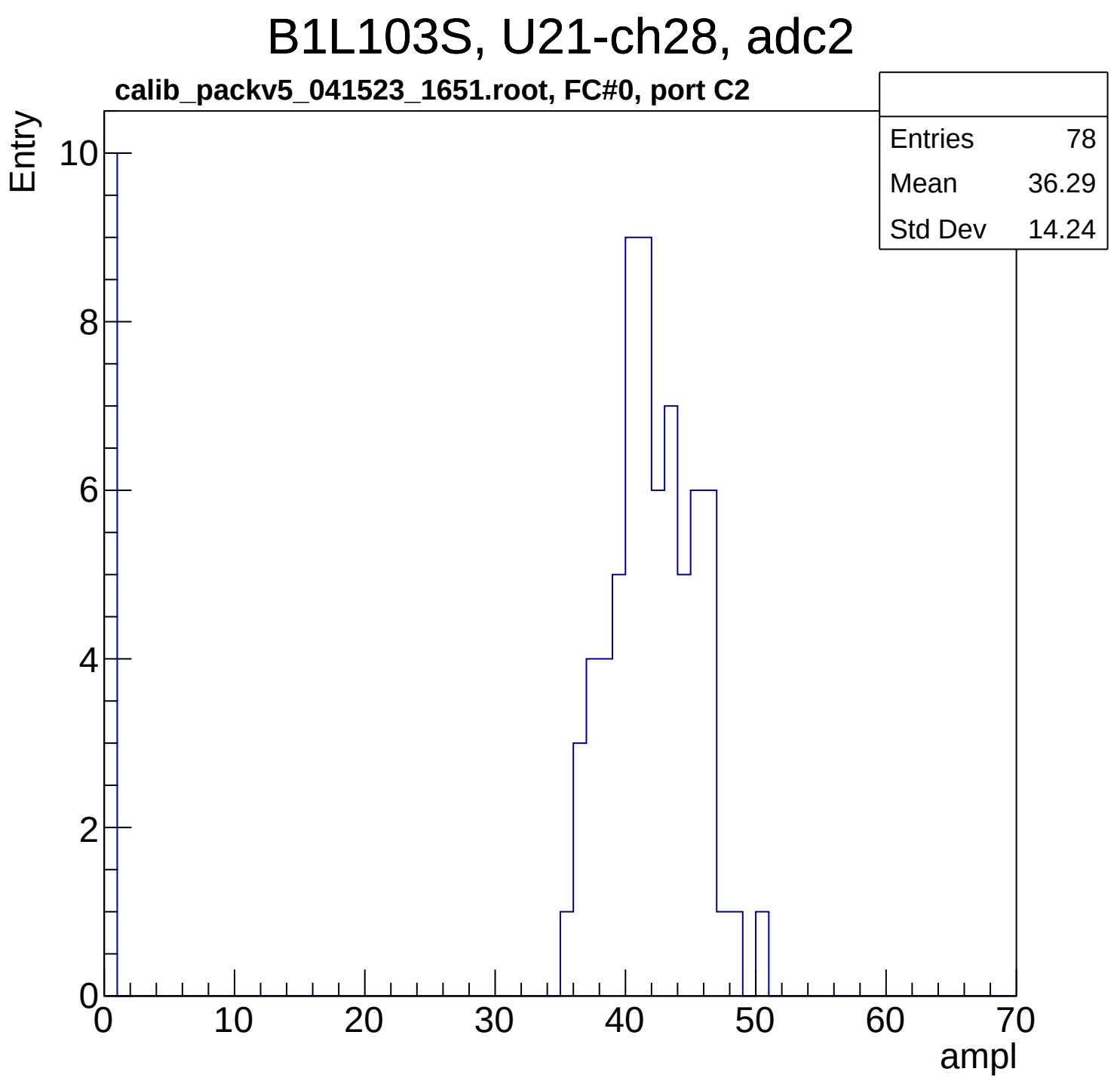
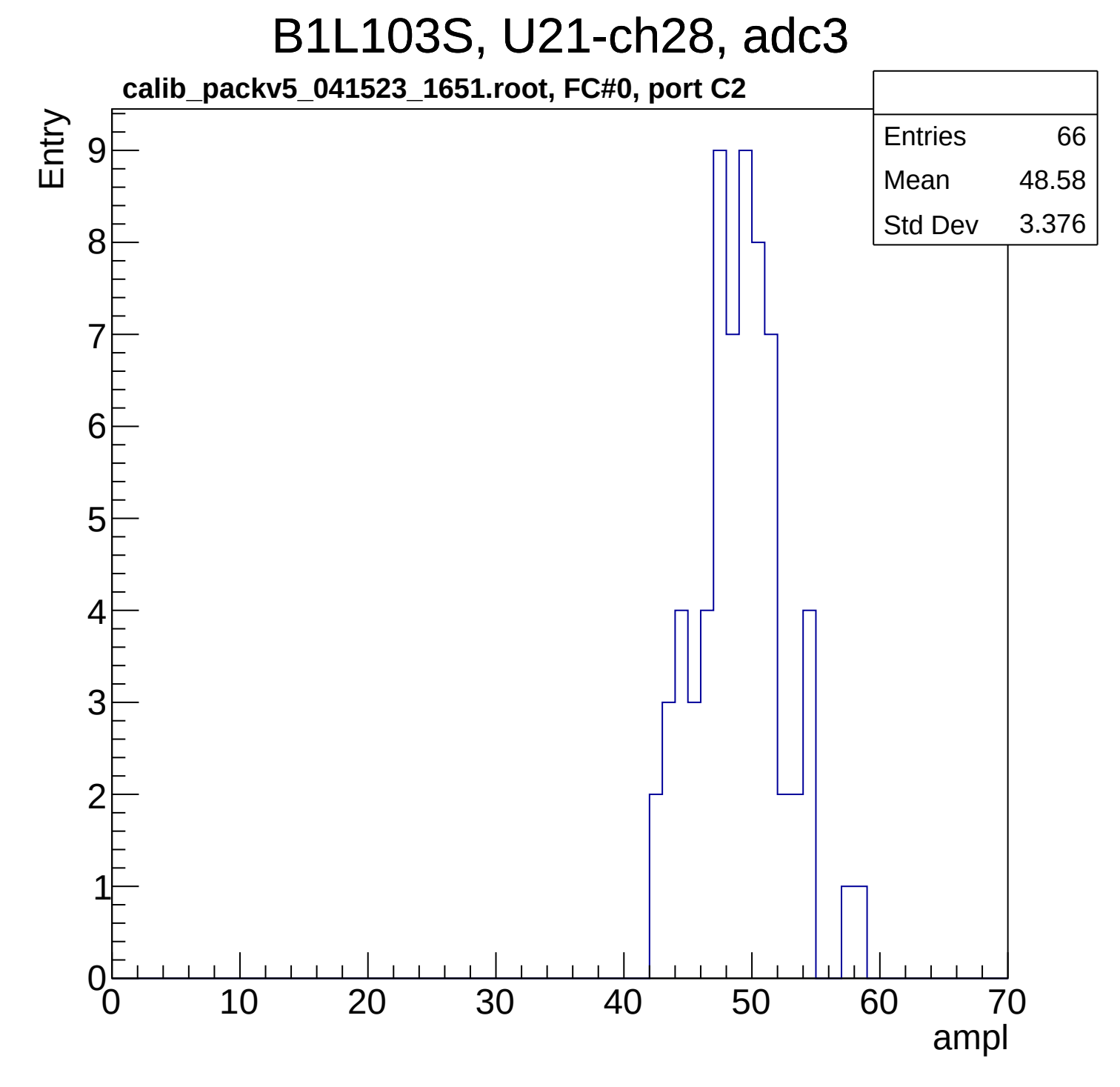
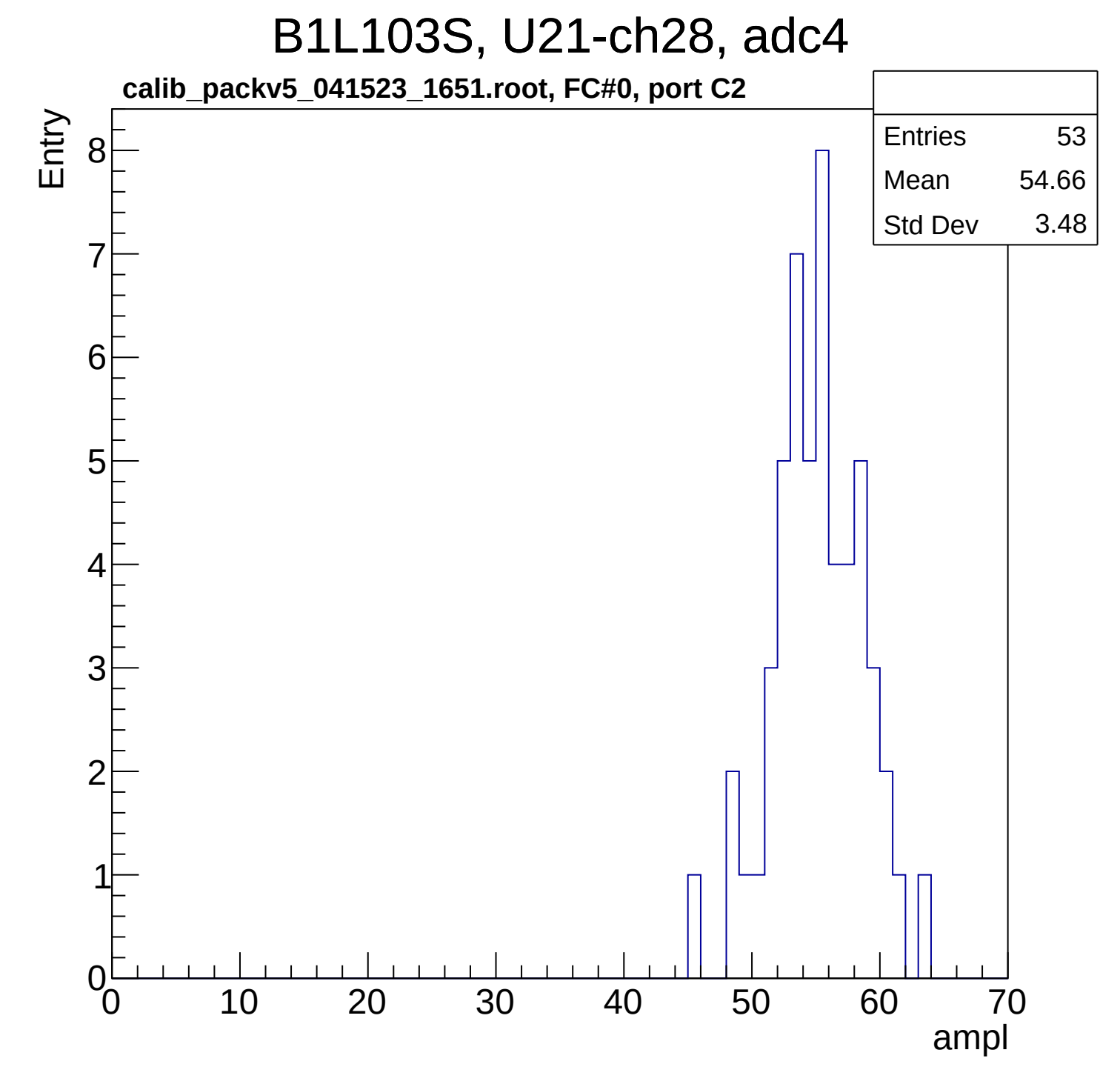
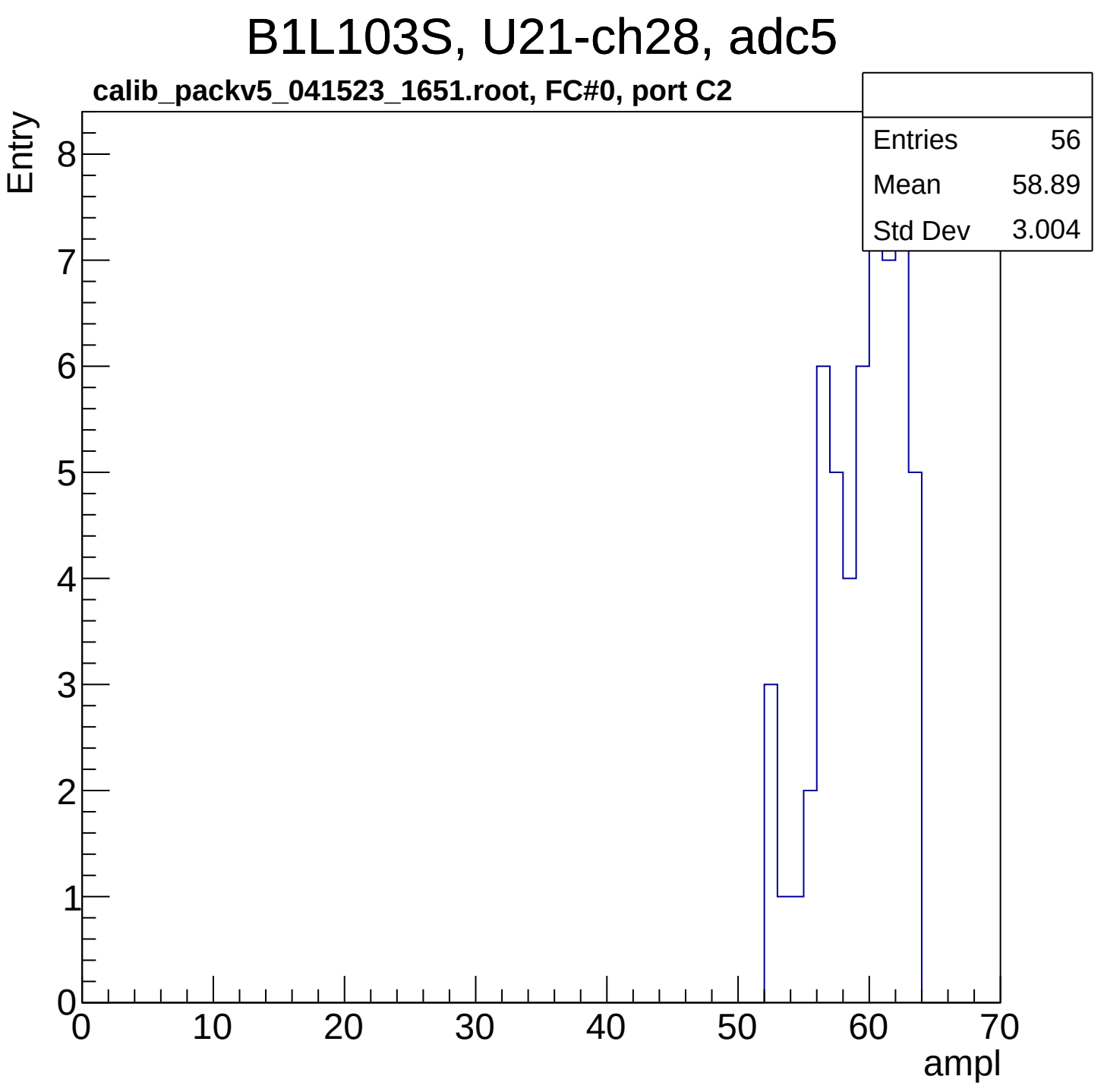
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch28, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 36.29
Std Dev 14.24
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch28, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 48.58
Std Dev 3.376
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch28, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 54.66
Std Dev 3.48
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch28, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 58.89
Std Dev 3.004
Entry
ampl
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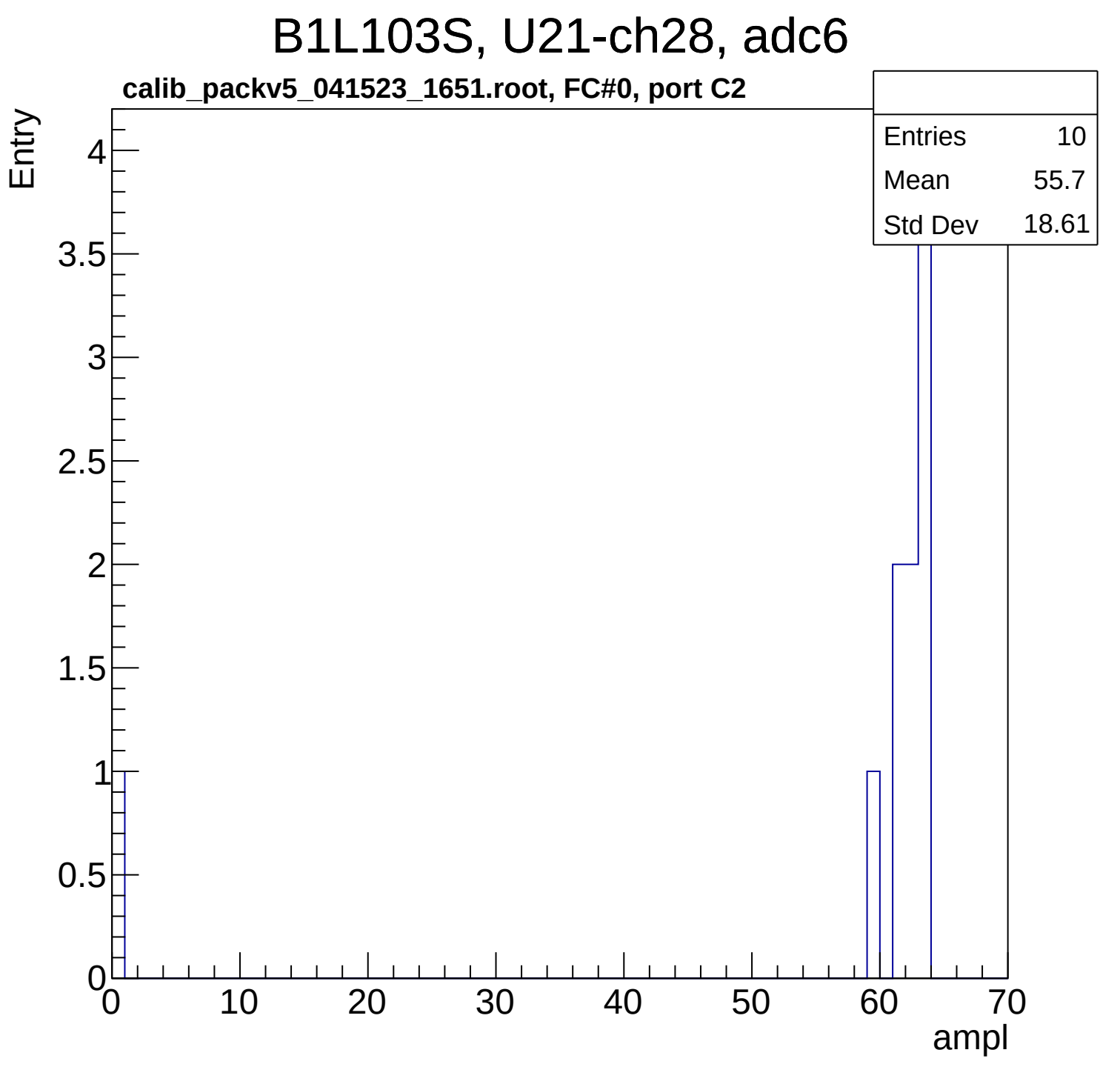
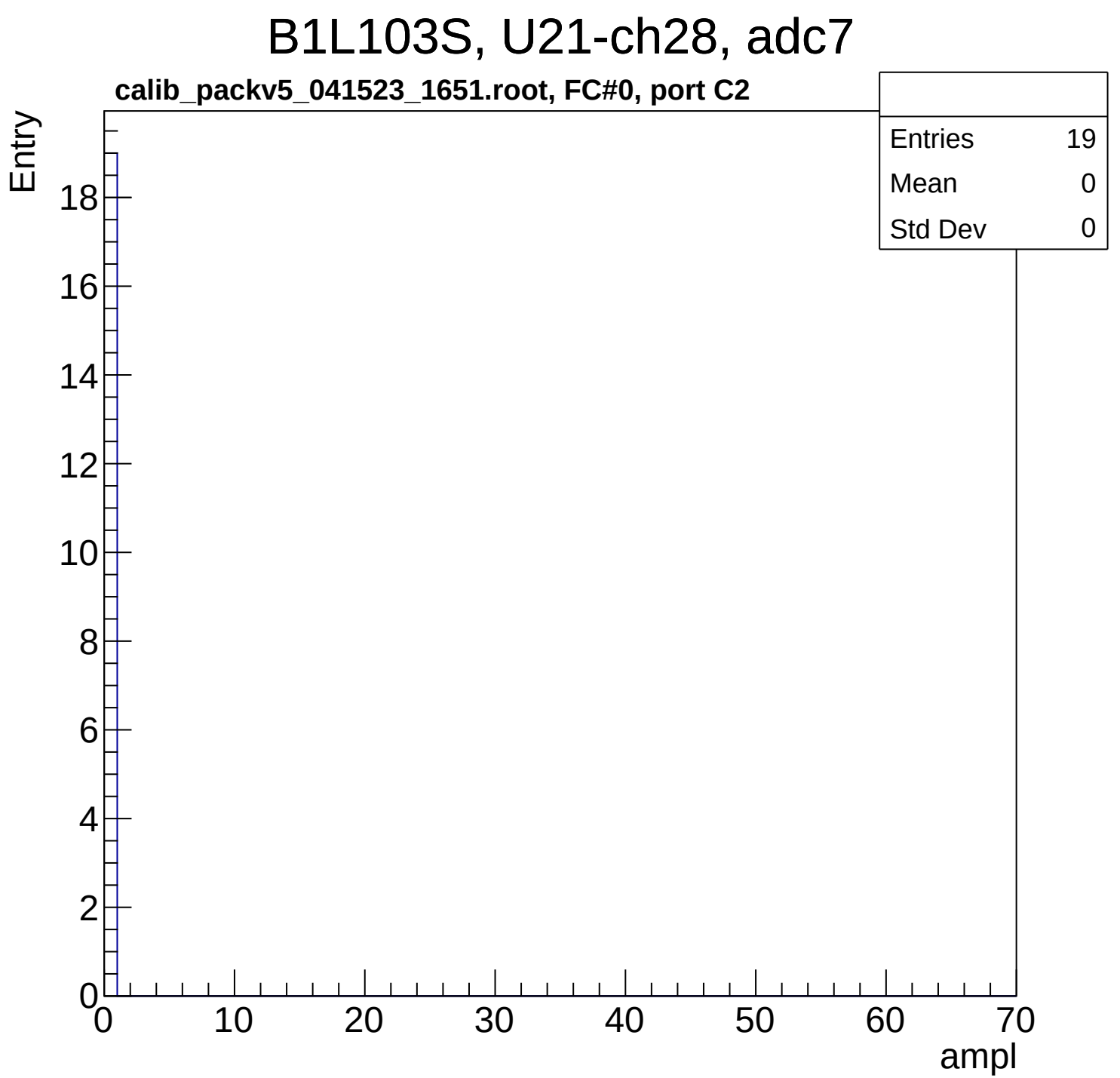
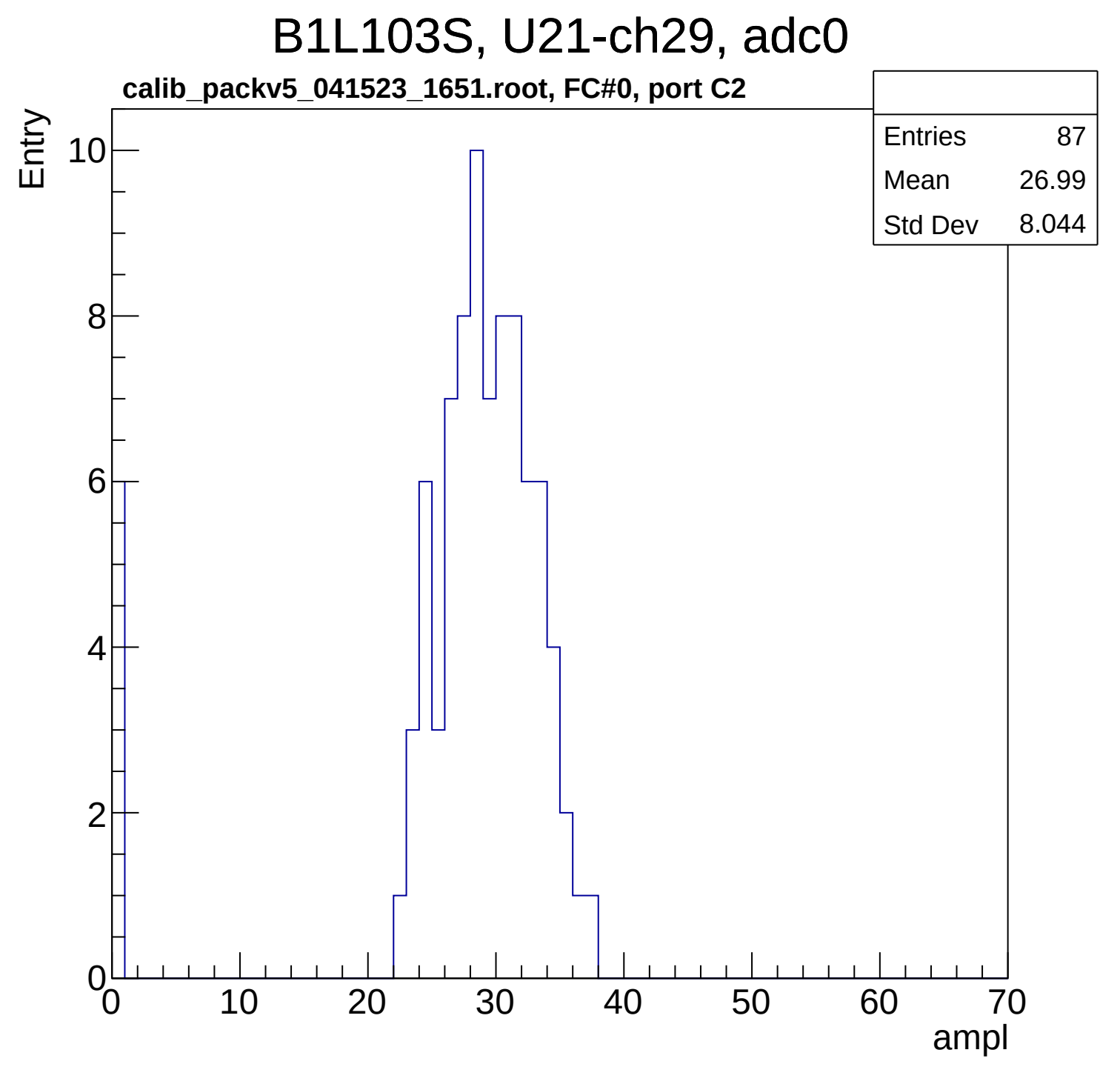
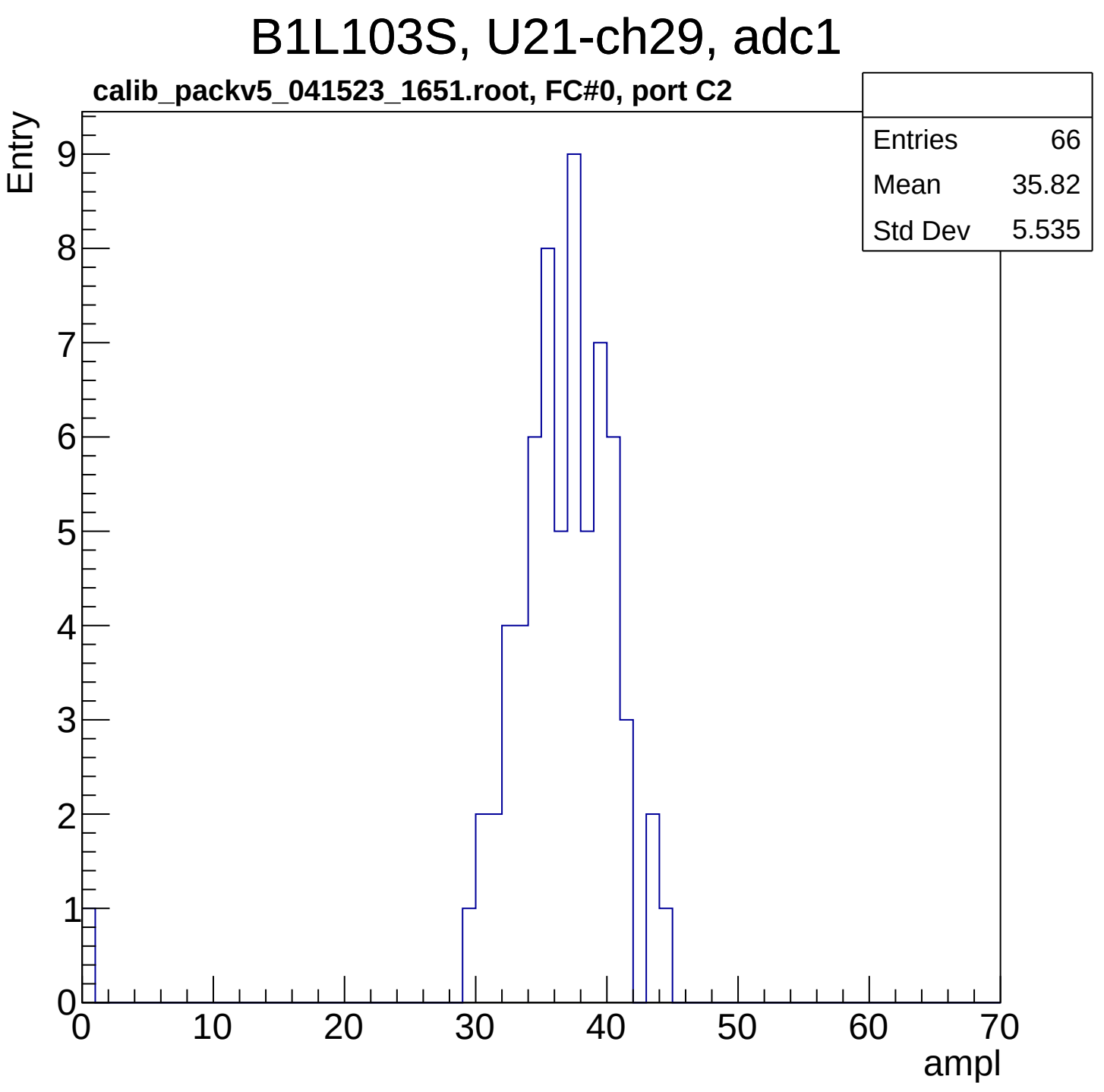
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch28, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 55.7
Std Dev 18.61
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U21-ch28, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch29, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 26.99
Std Dev 8.044
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U21-ch29, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 35.82
Std Dev 5.535
Entry
ampl
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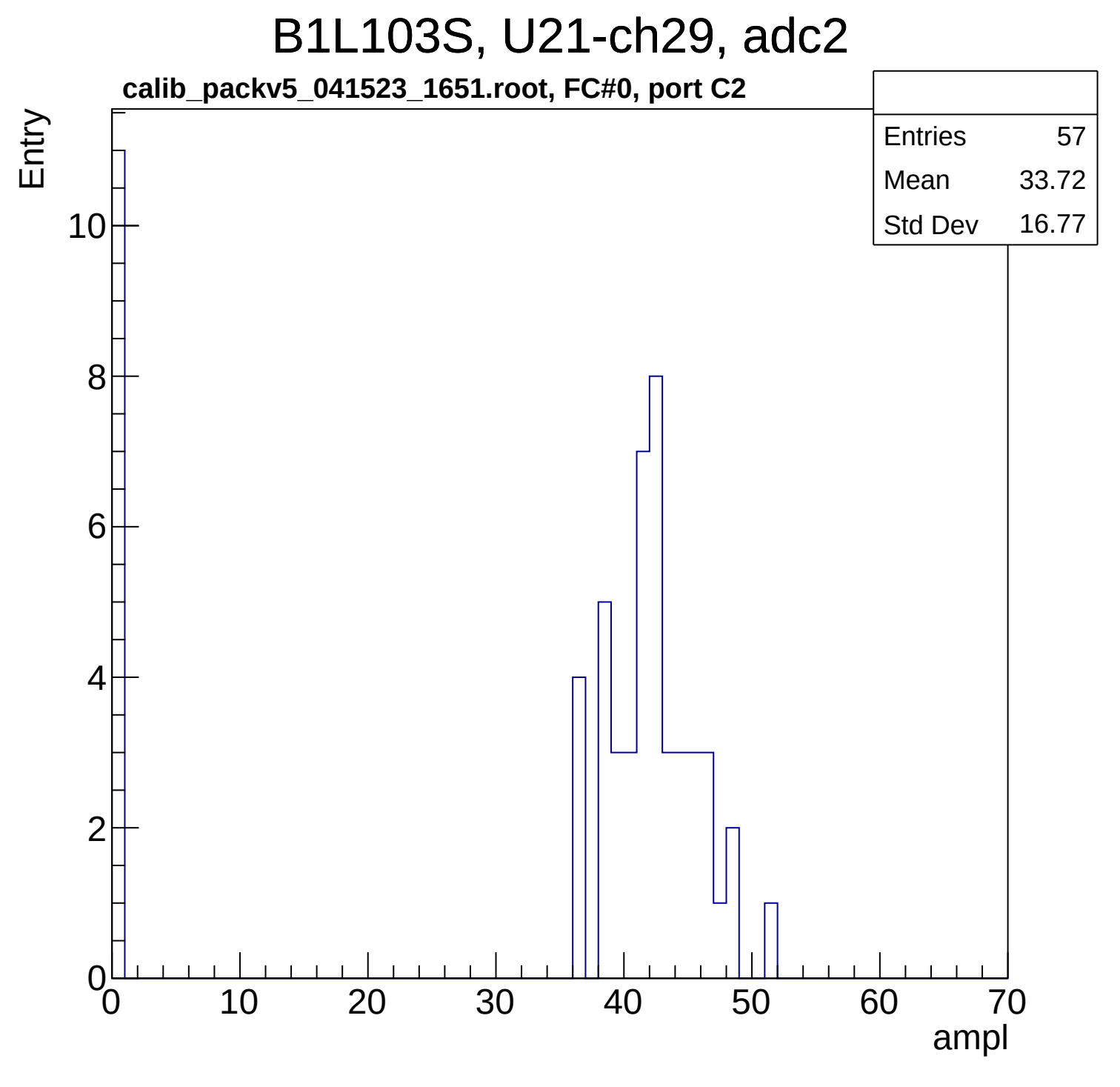
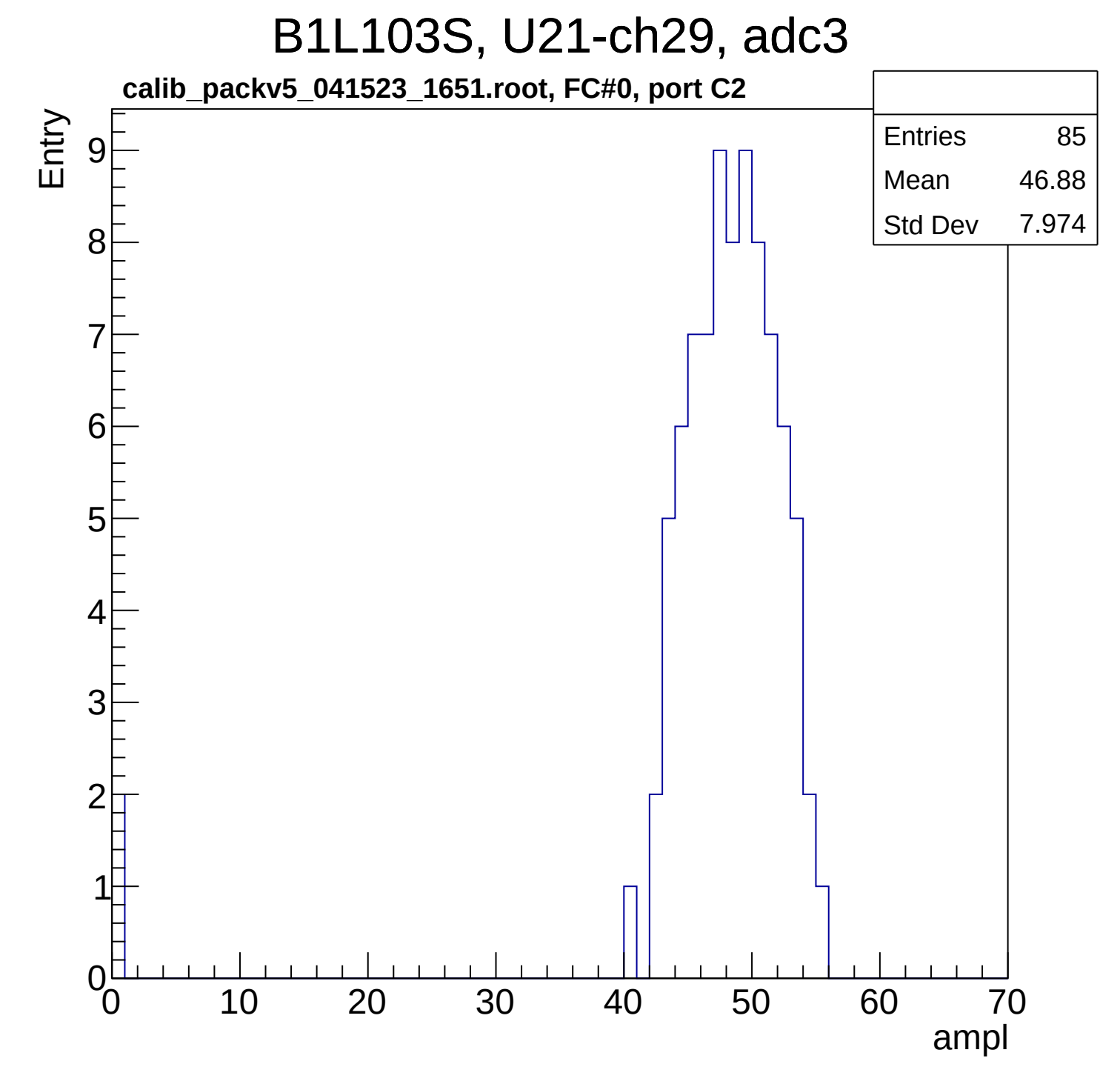
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch29, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 33.72
Std Dev 16.77
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch29, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 46.88
Std Dev 7.974
Entry
ampl
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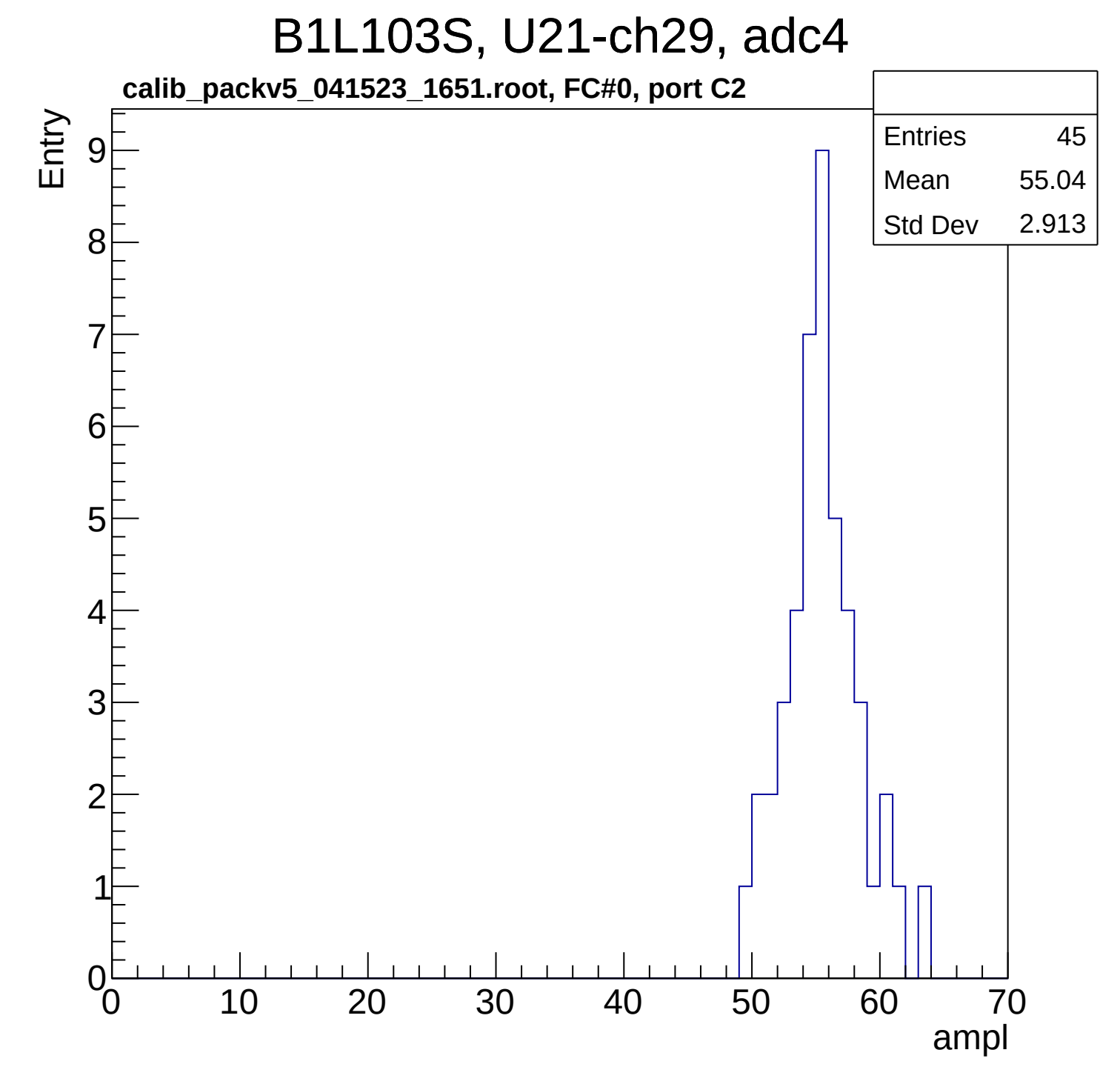
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch29, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 55.04
Std Dev 2.913
Entry
ampl
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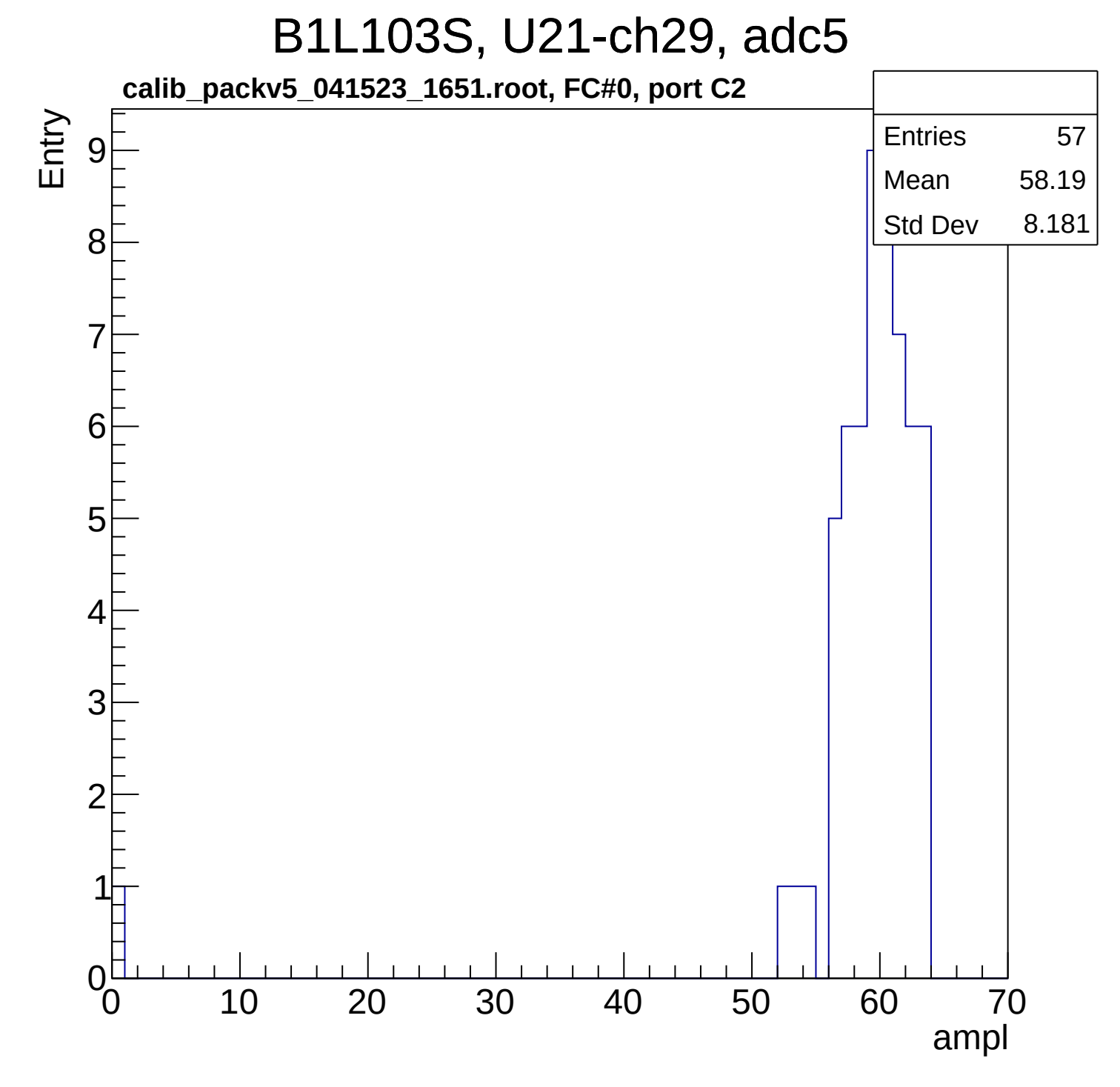
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch29, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 58.19
Std Dev 8.181
Entry
ampl
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2
3
4
5
6
7
8
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0
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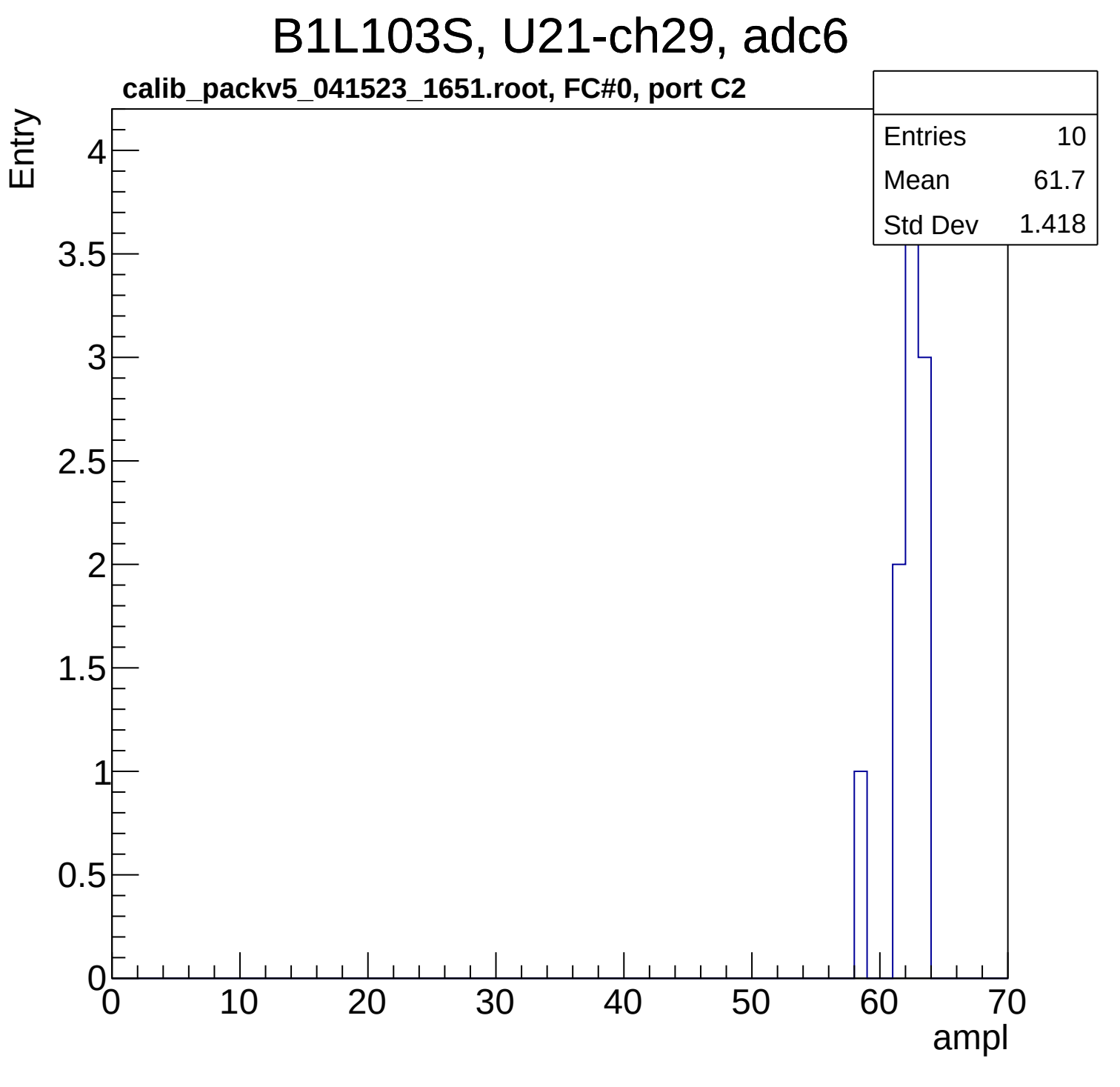
60
70


B1L103S, U21-ch29, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61.7
Std Dev 1.418
Entry
ampl
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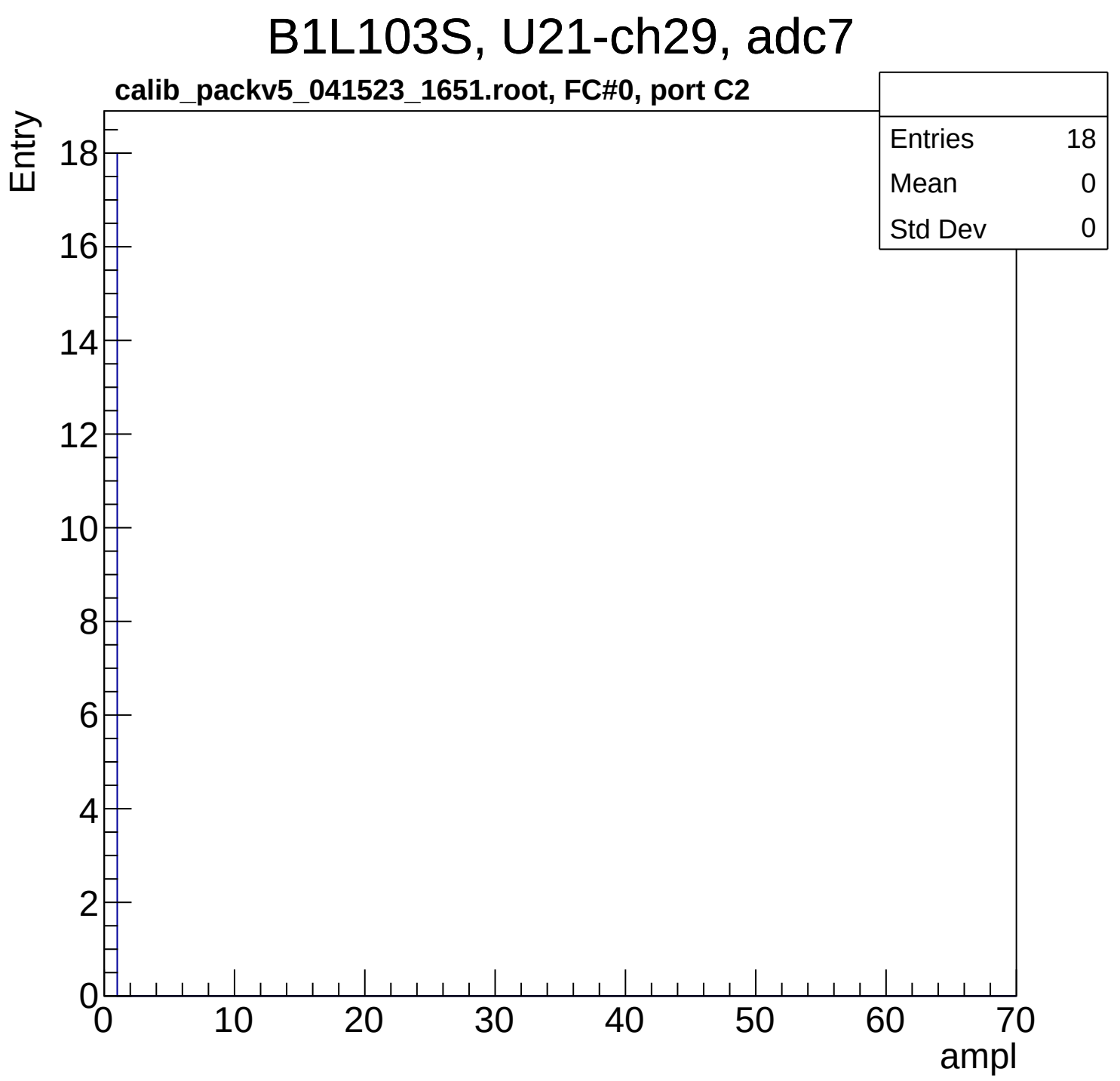
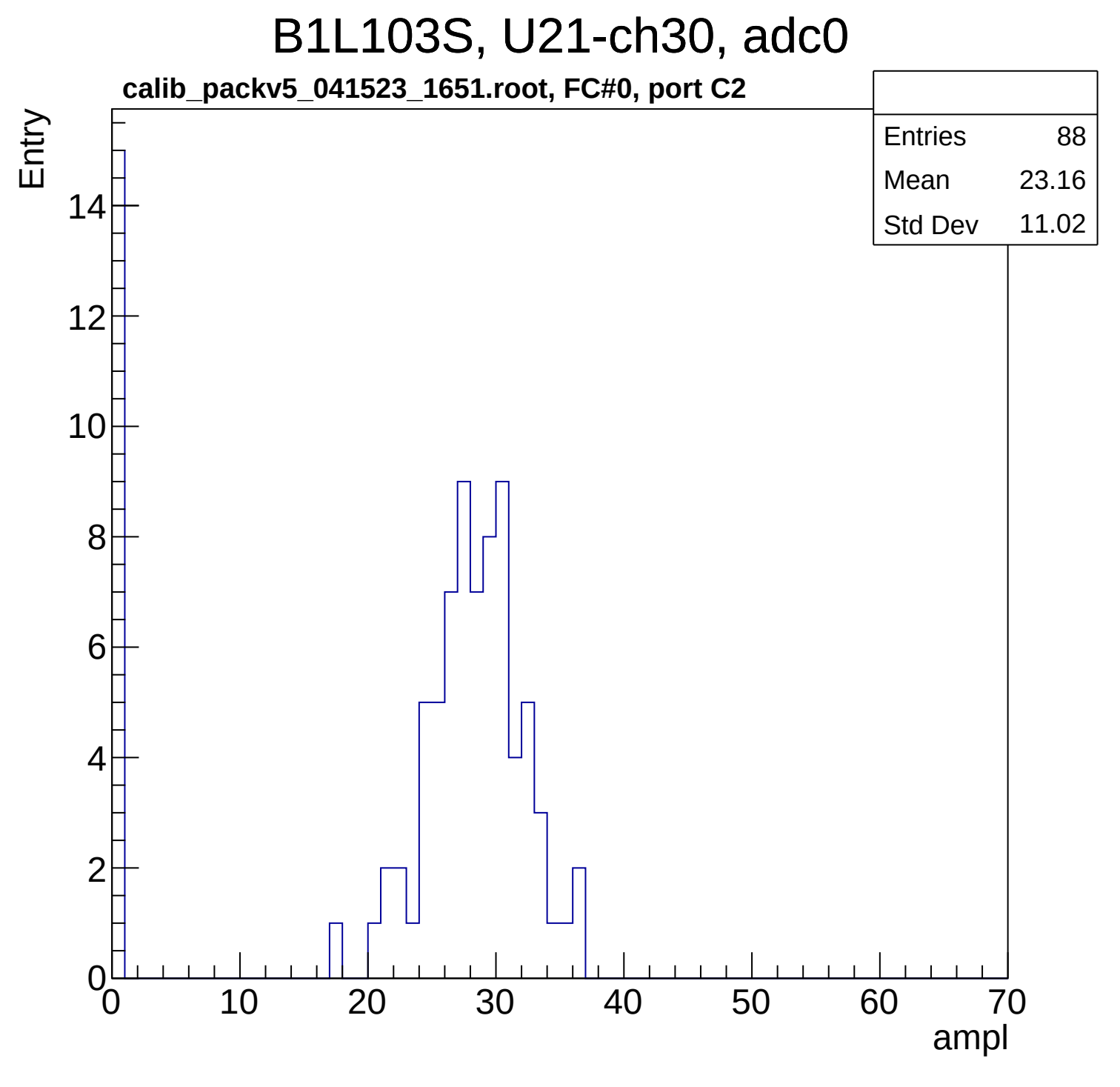
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U21-ch29, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch30, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 23.16
Std Dev 11.02
Entry
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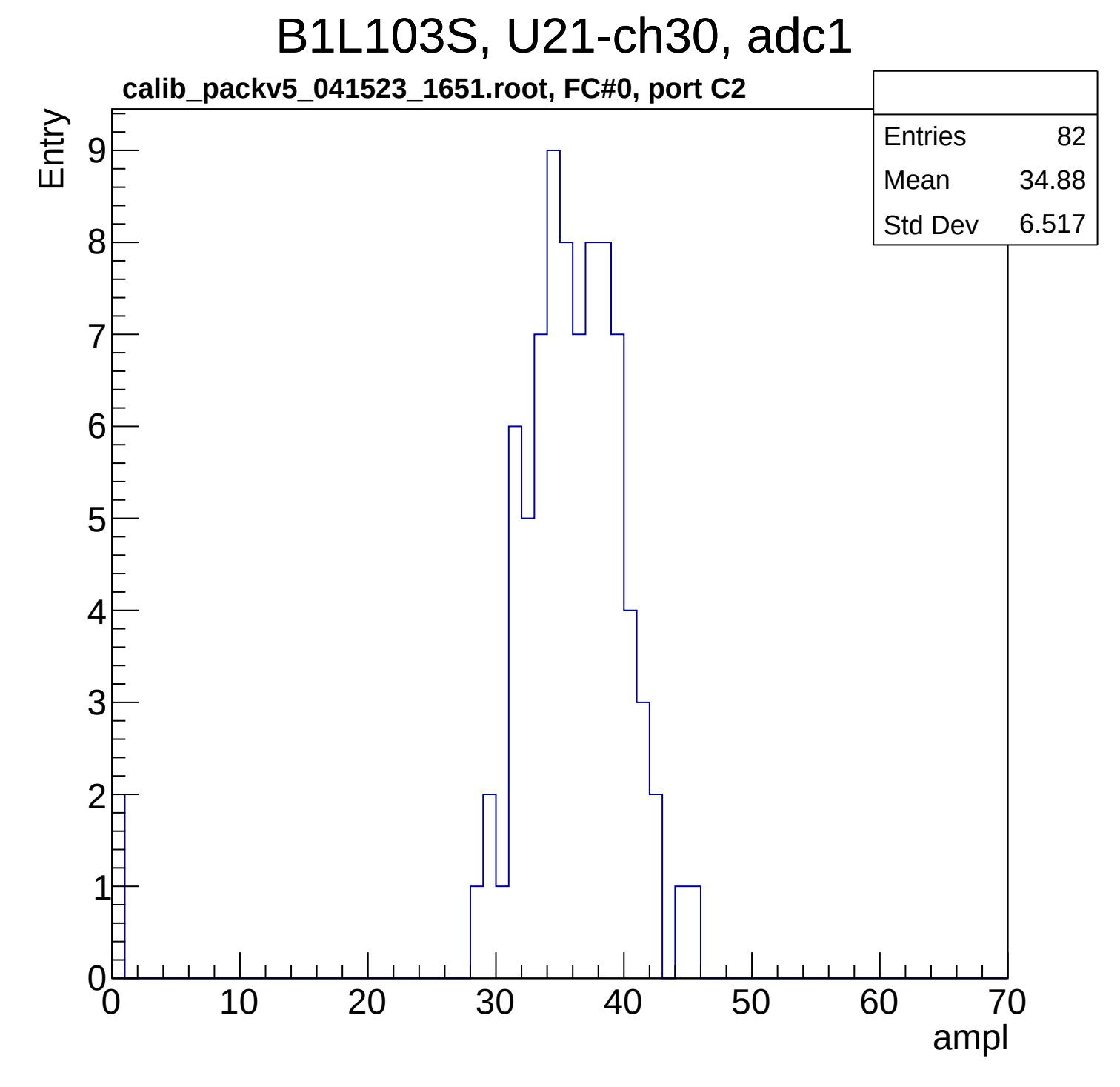
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch30, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 34.88
Std Dev 6.517
Entry
ampl
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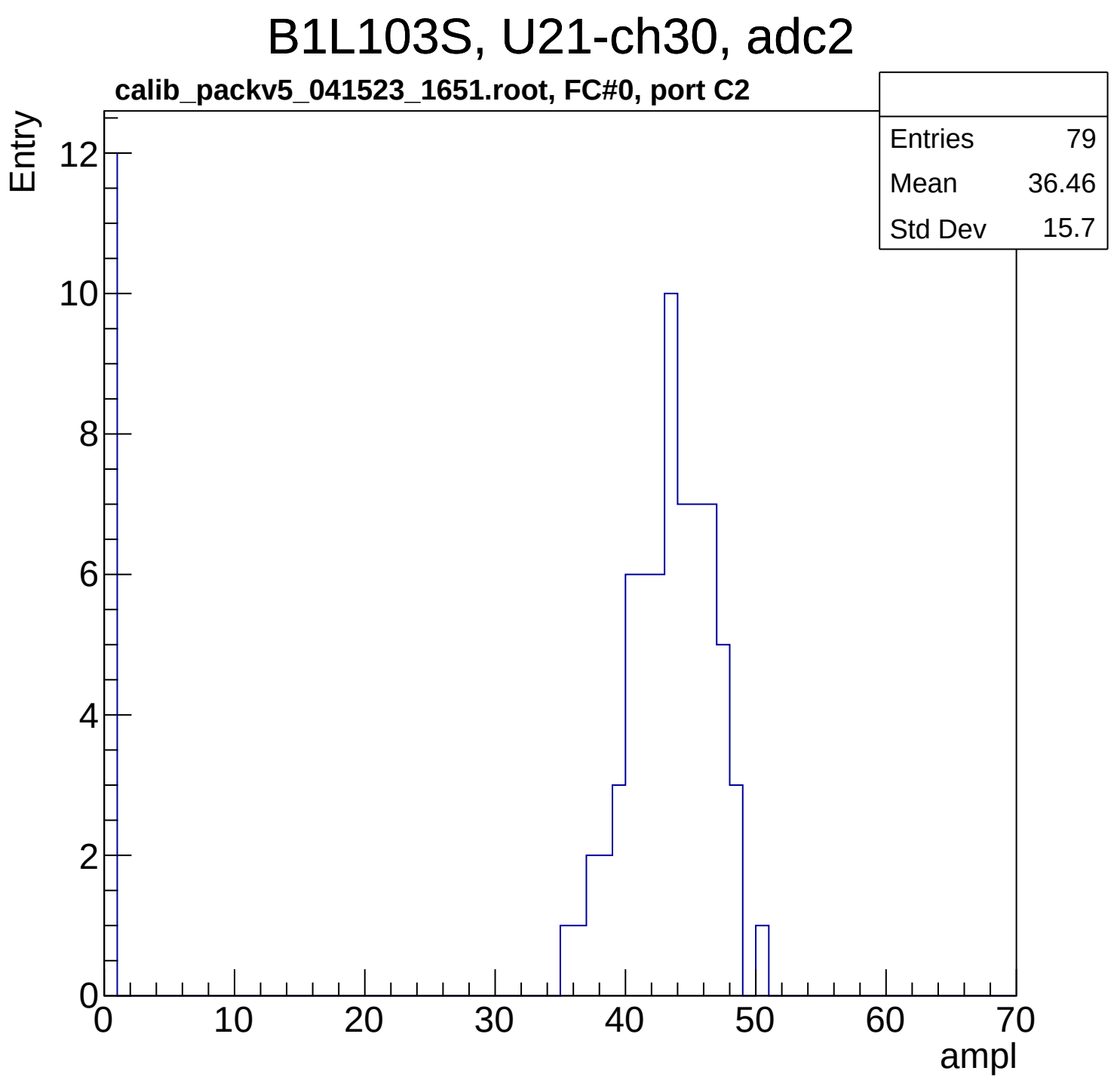
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch30, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 36.46
Std Dev 15.7
Entry
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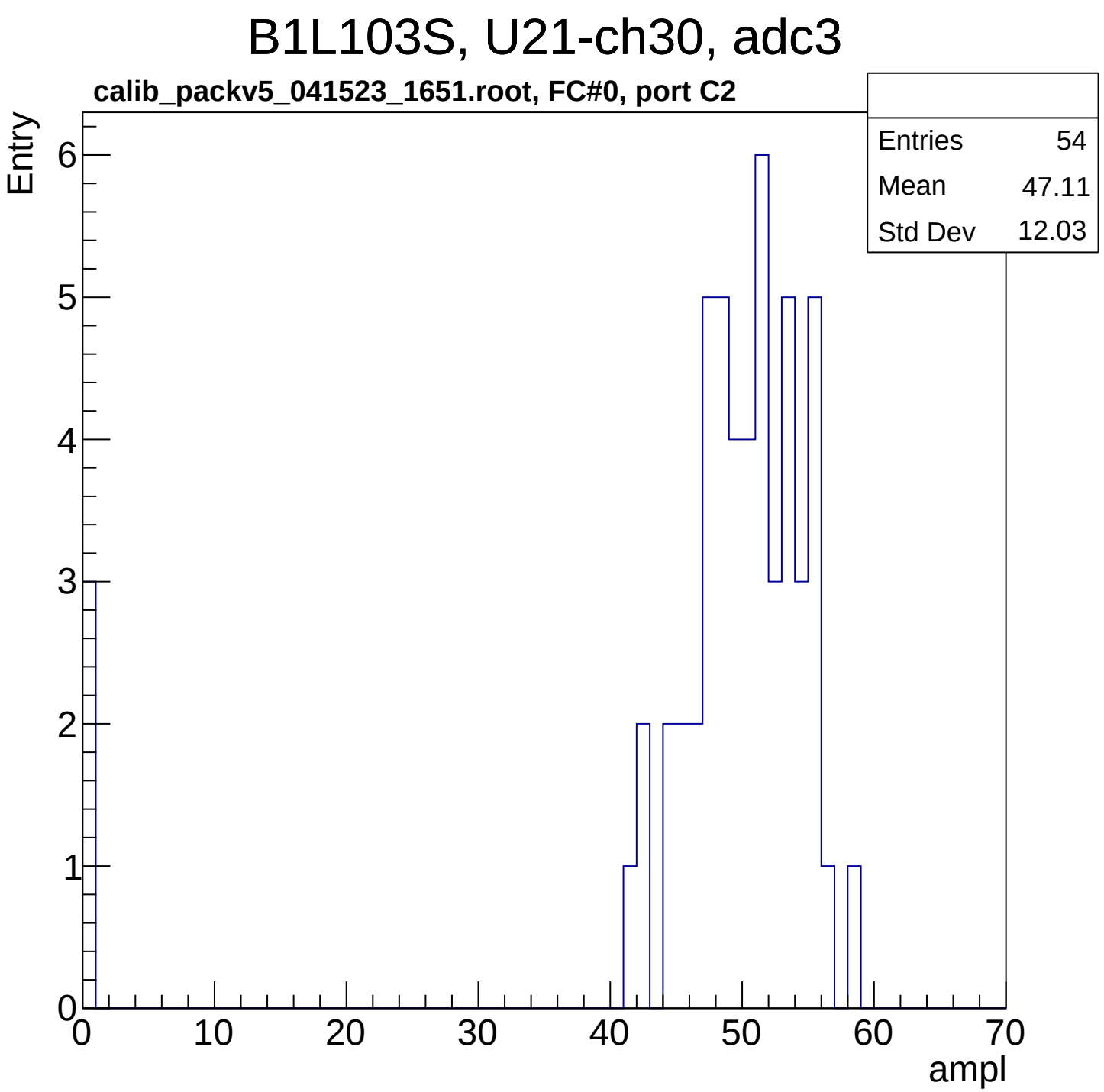
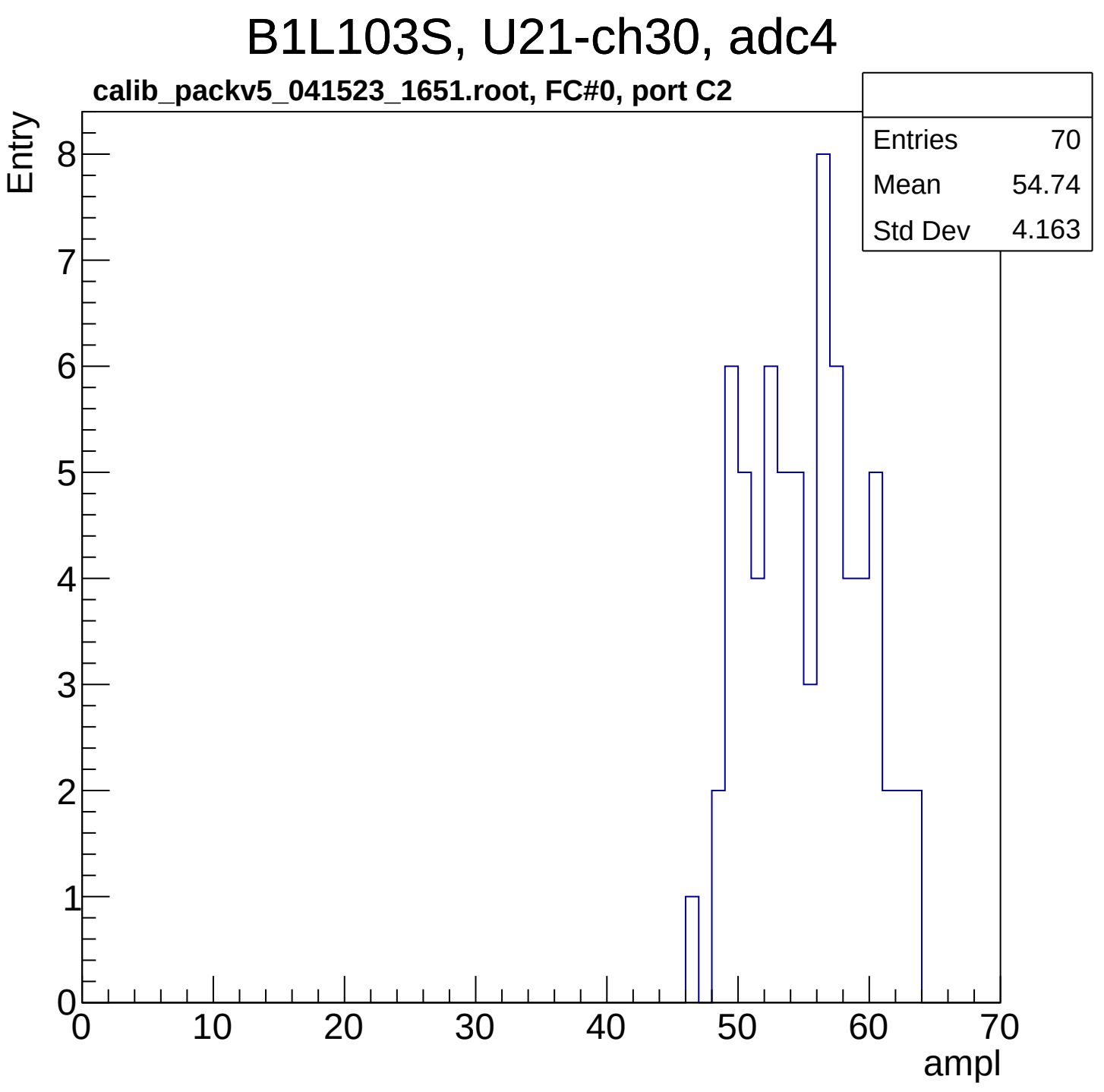
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch30, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 47.11
Std Dev 12.03
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U21-ch30, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 54.74
Std Dev 4.163
Entry
ampl
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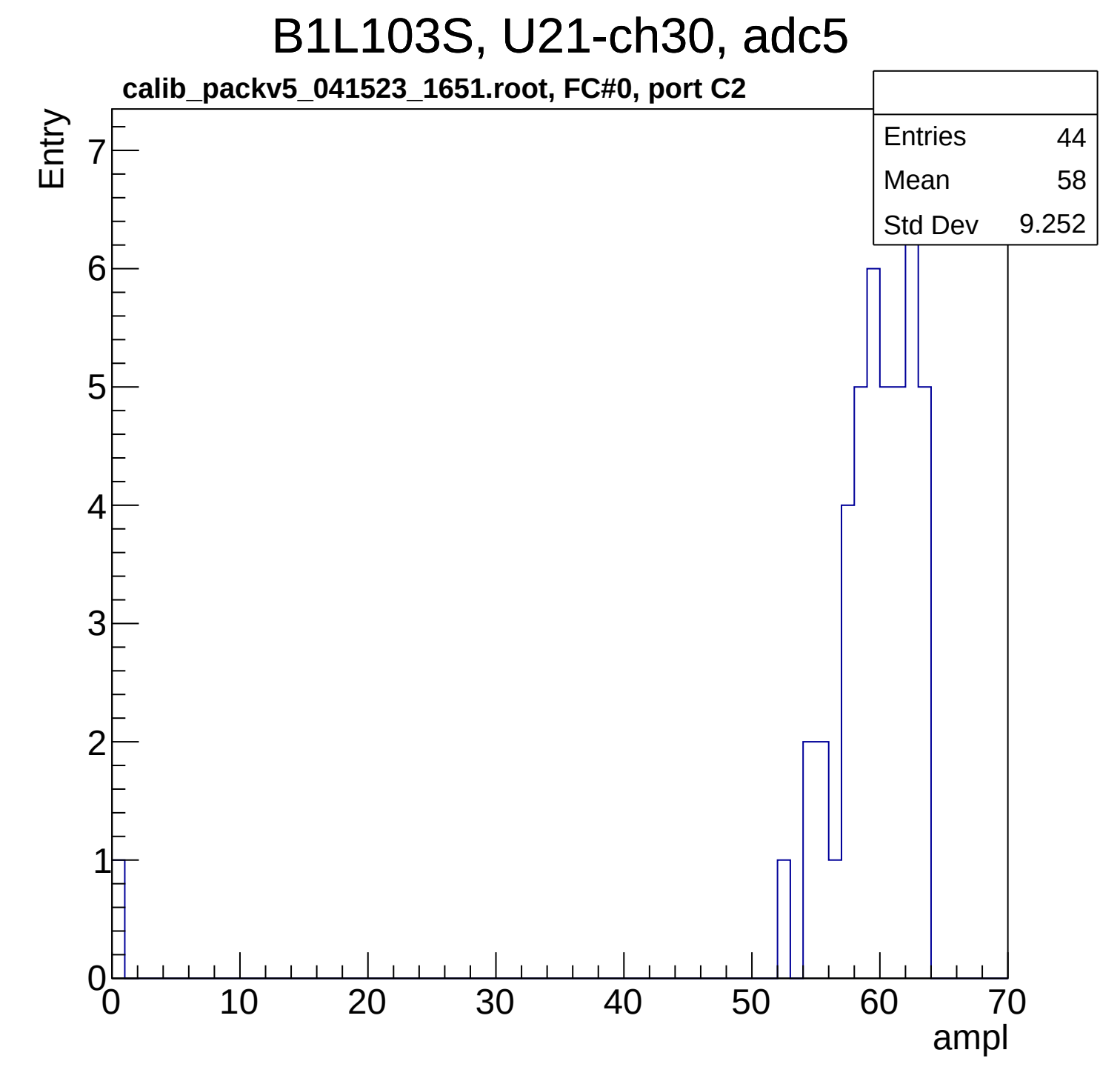
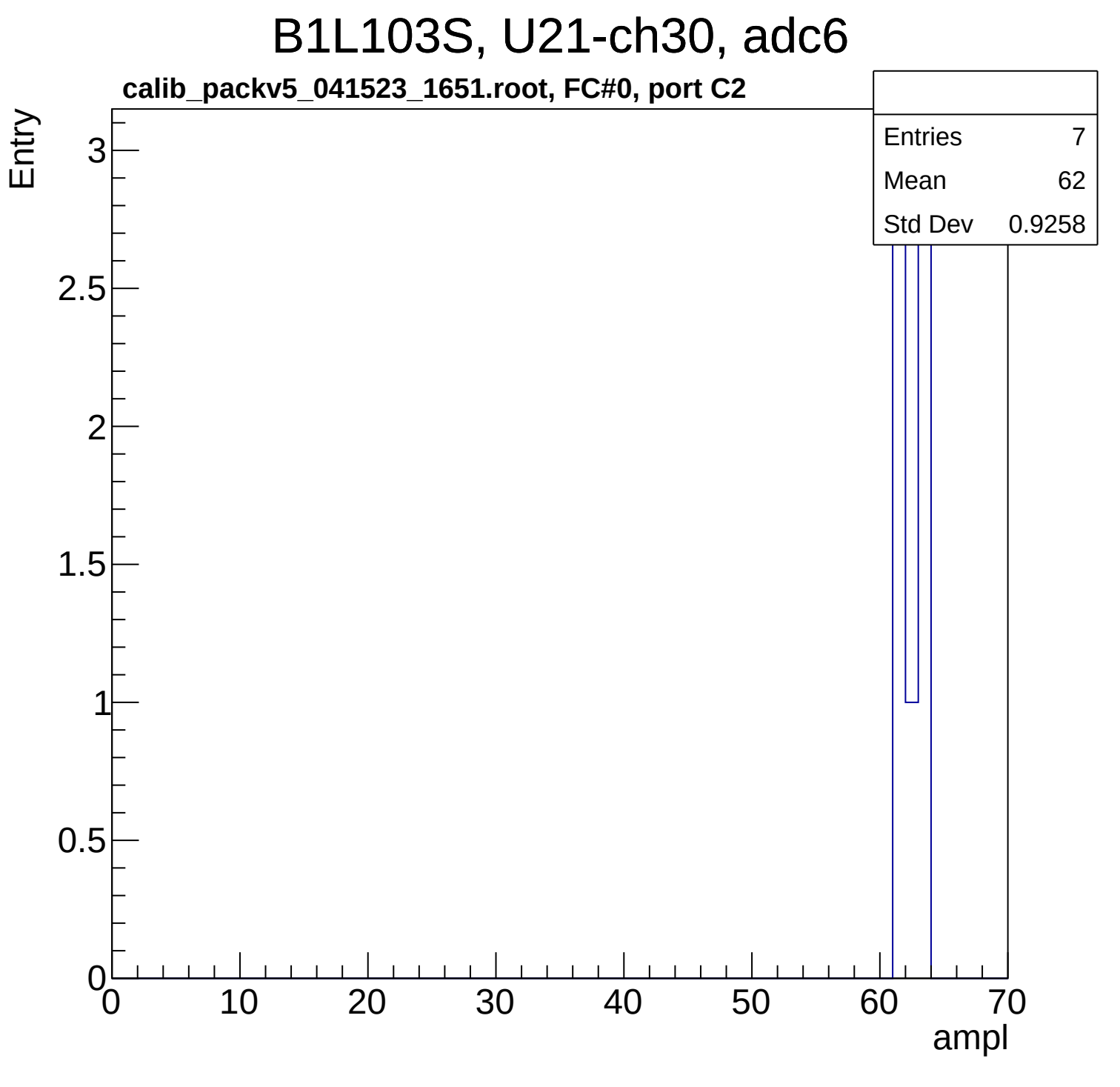
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch30, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 58
Std Dev 9.252
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U21-ch30, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 62
Std Dev 0.9258
Entry
ampl
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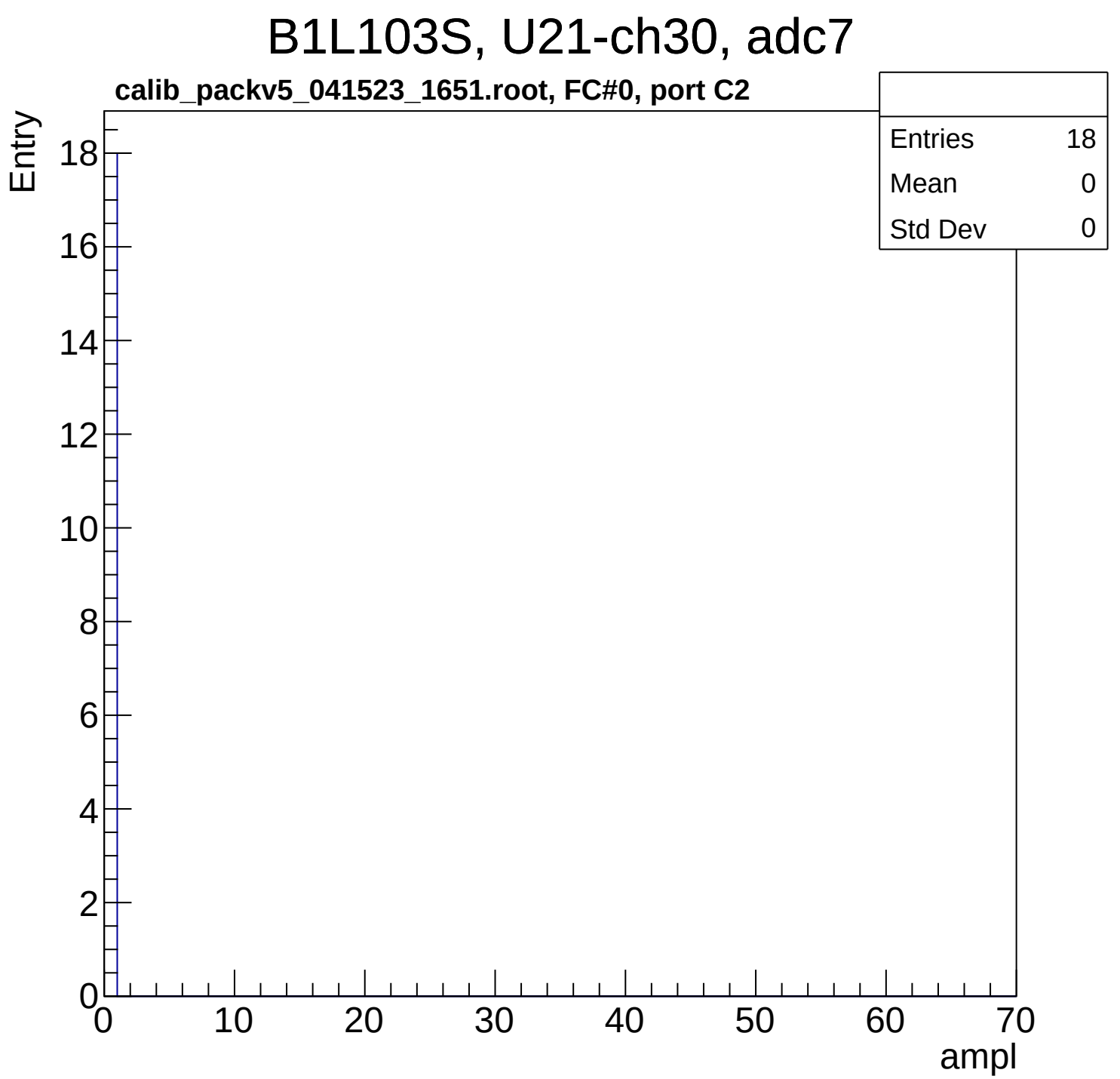
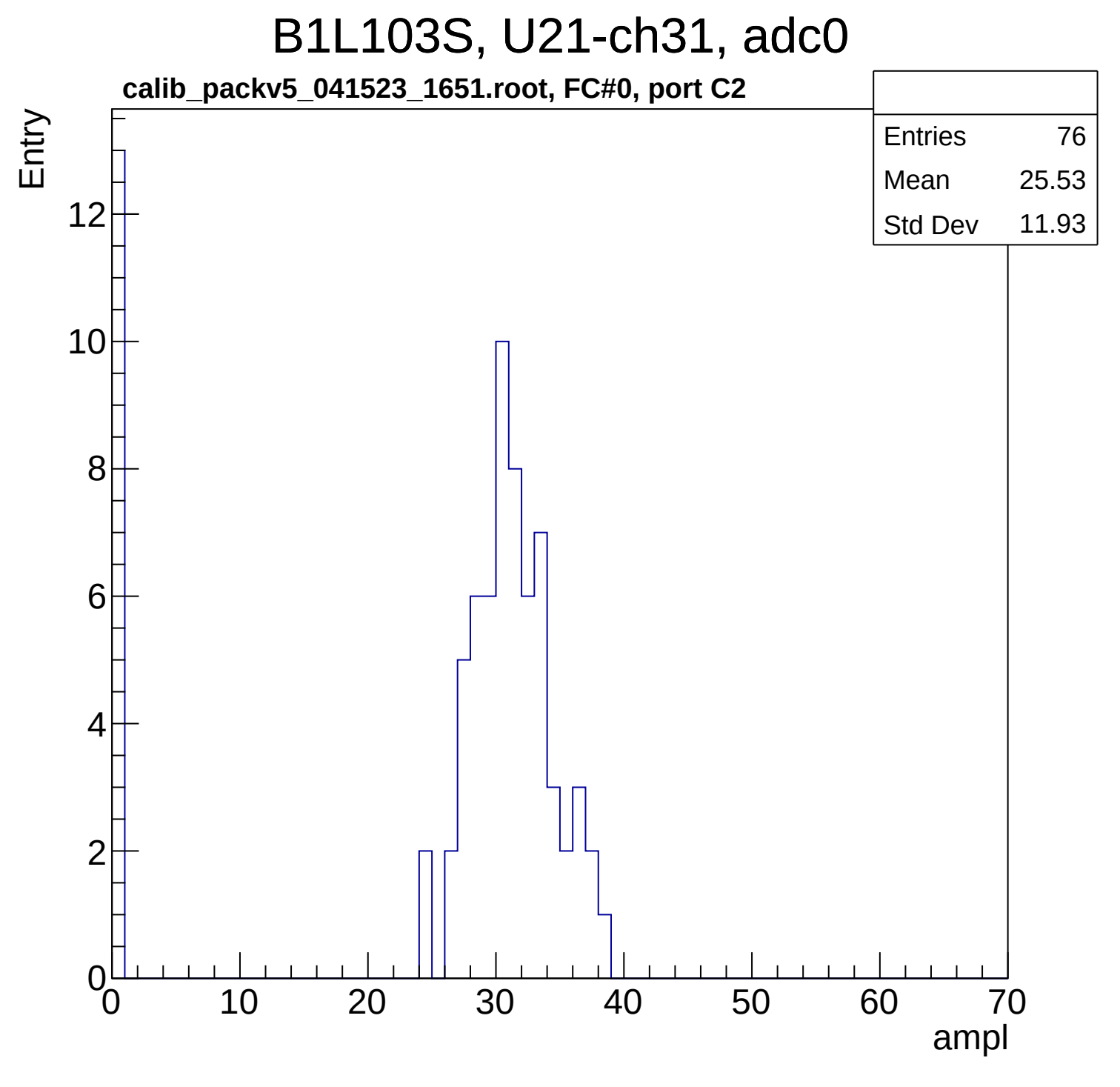
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U21-ch30, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch31, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 25.53
Std Dev 11.93
Entry
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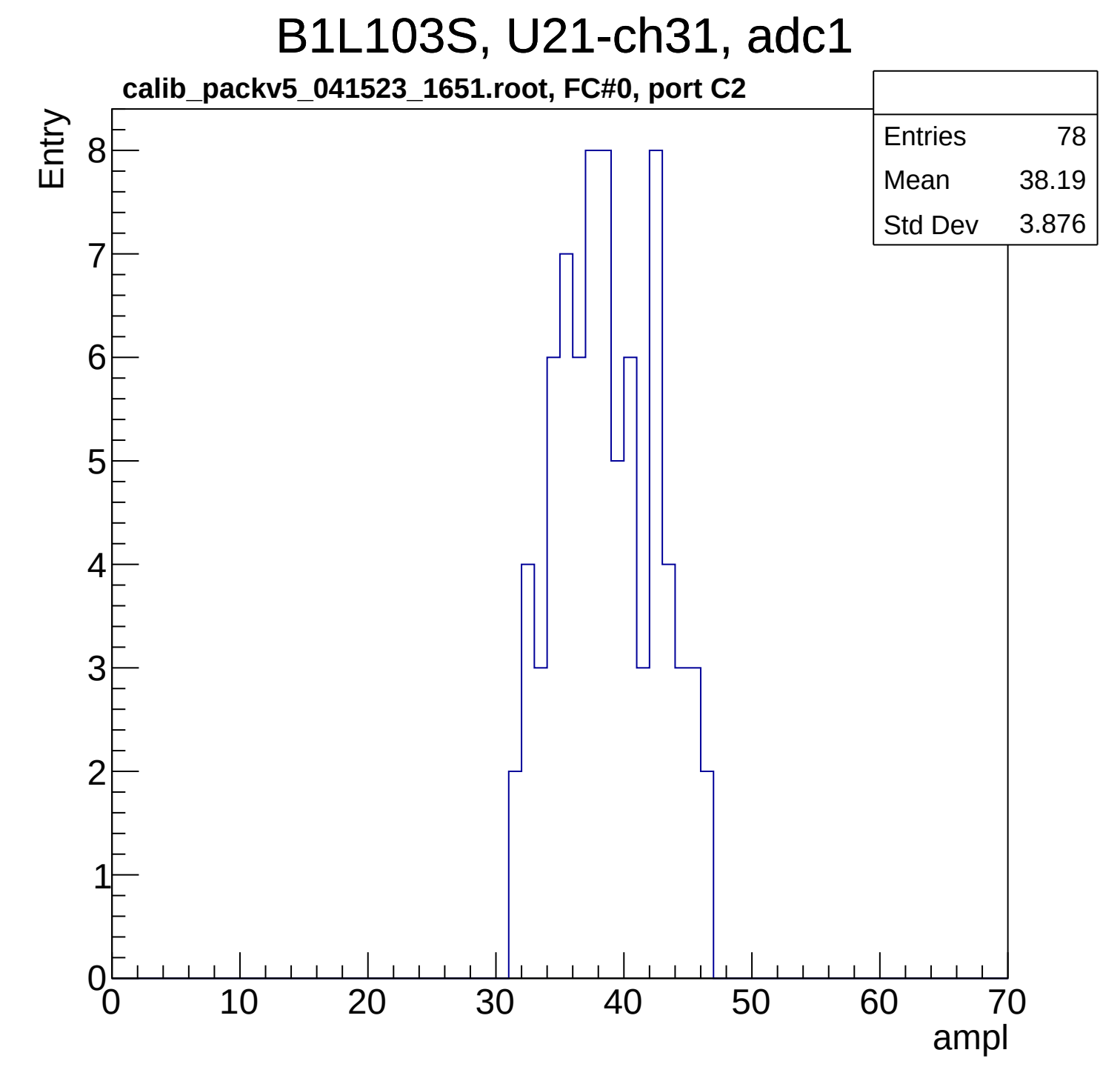
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch31, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 38.19
Std Dev 3.876
Entry
ampl
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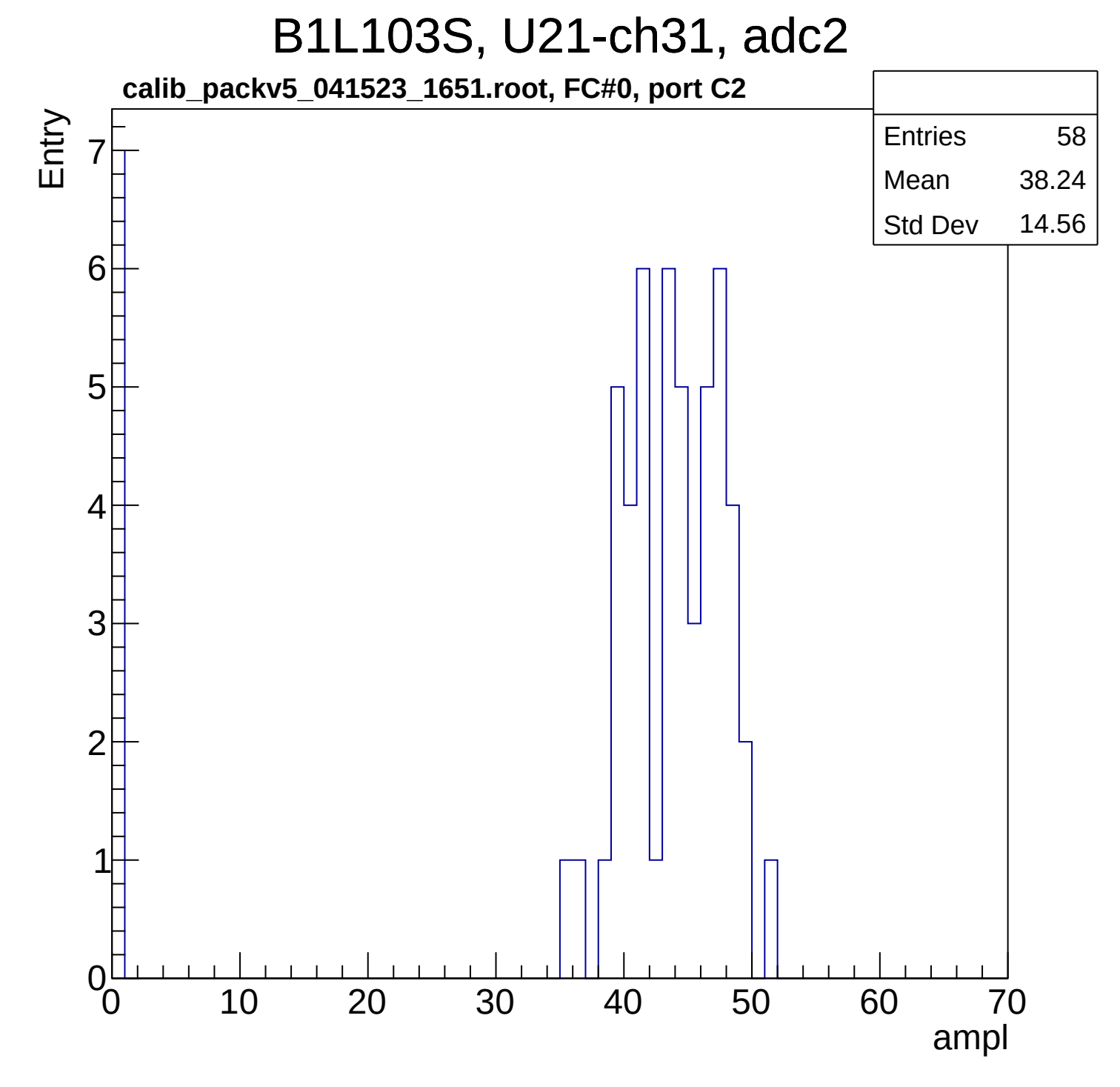
B1L103S, U21-ch31, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 38.24
Std Dev 14.56
Entry
ampl
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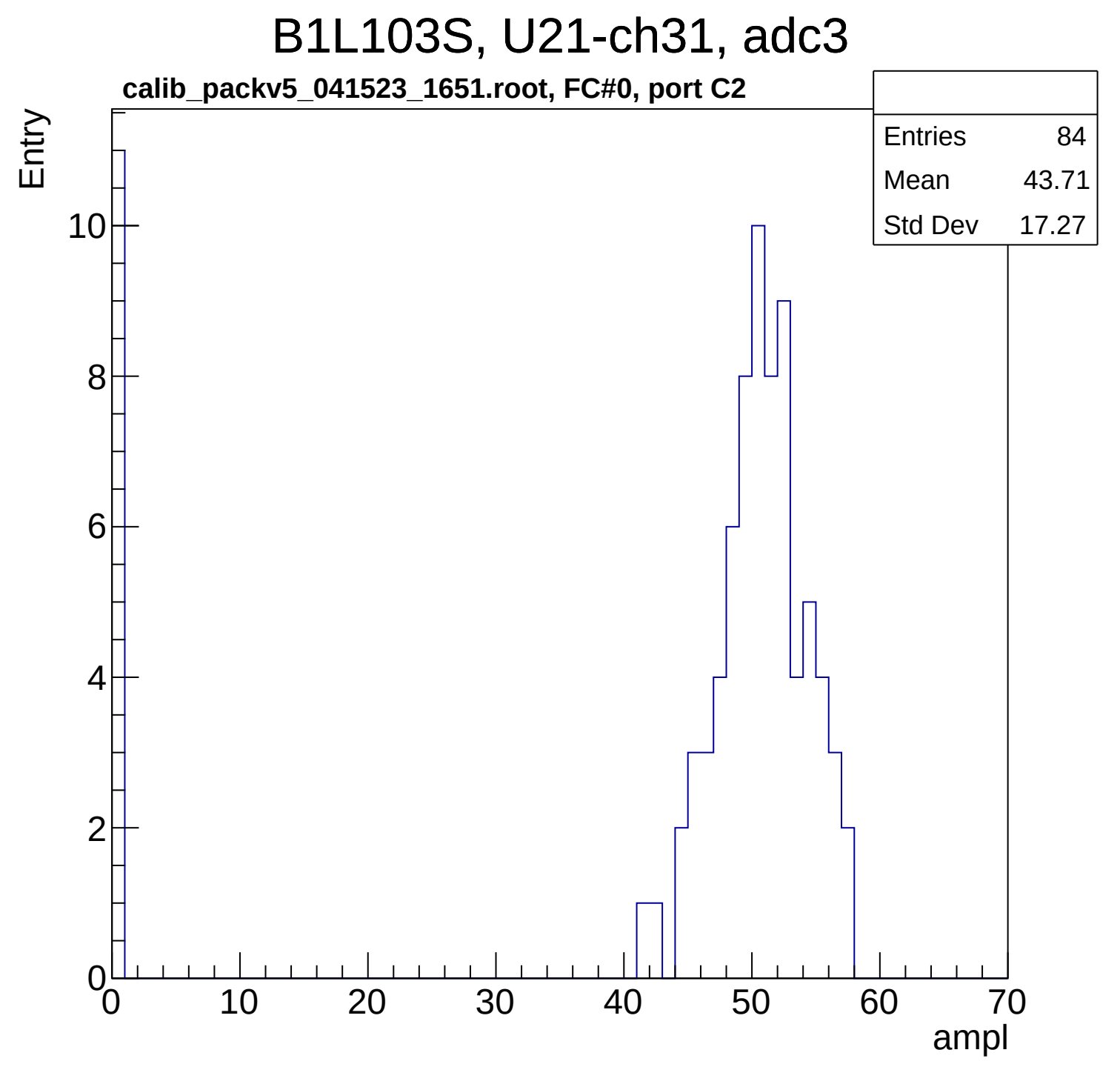
B1L103S, U21-ch31, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 43.71
Std Dev 17.27
Entry
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10
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20
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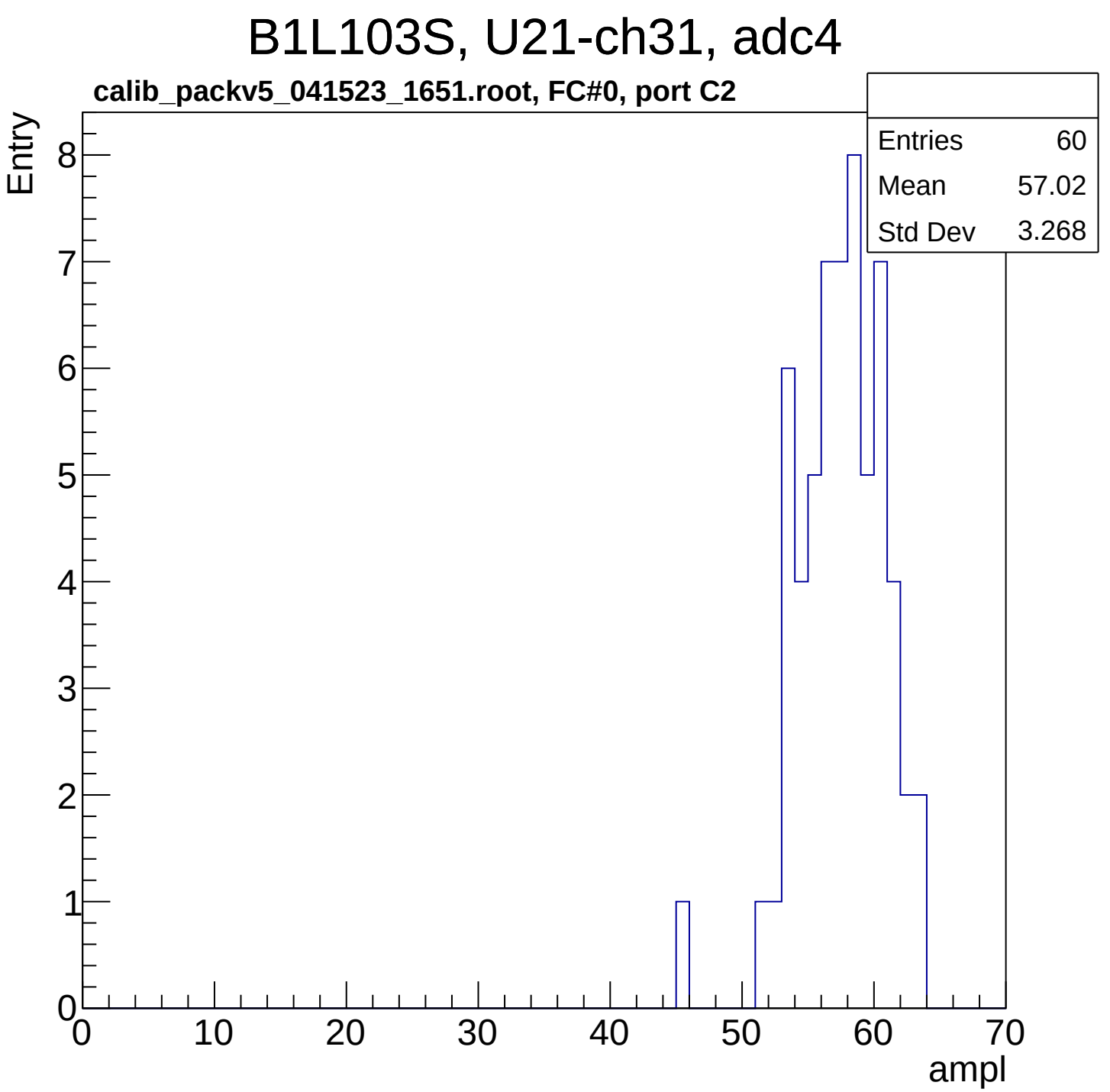
50
60
70
ampl


B1L103S, U21-ch31, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 57.02
Std Dev 3.268
Entry
ampl
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0
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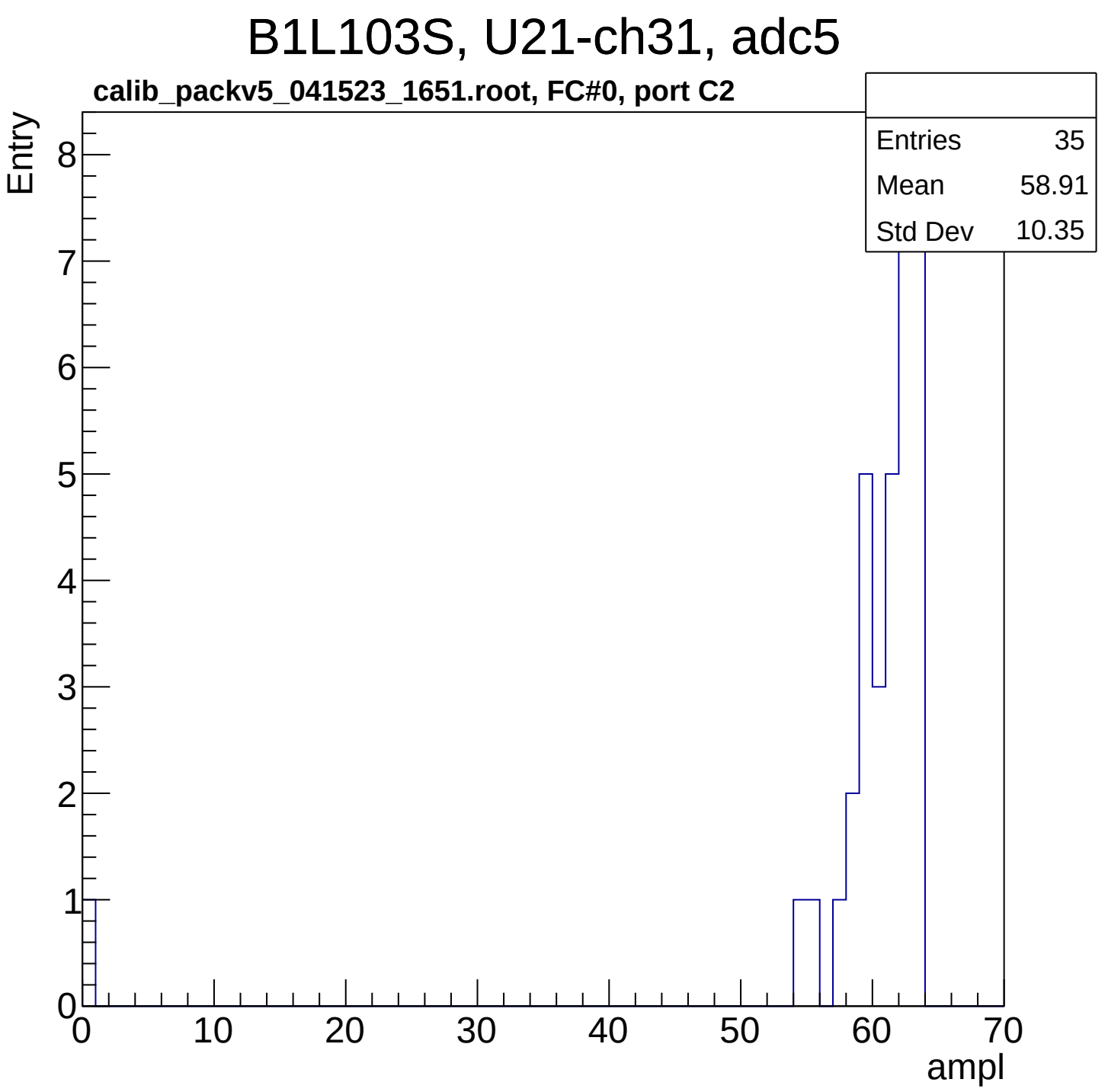
B1L103S, U21-ch31, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 58.91
Std Dev 10.35
Entry
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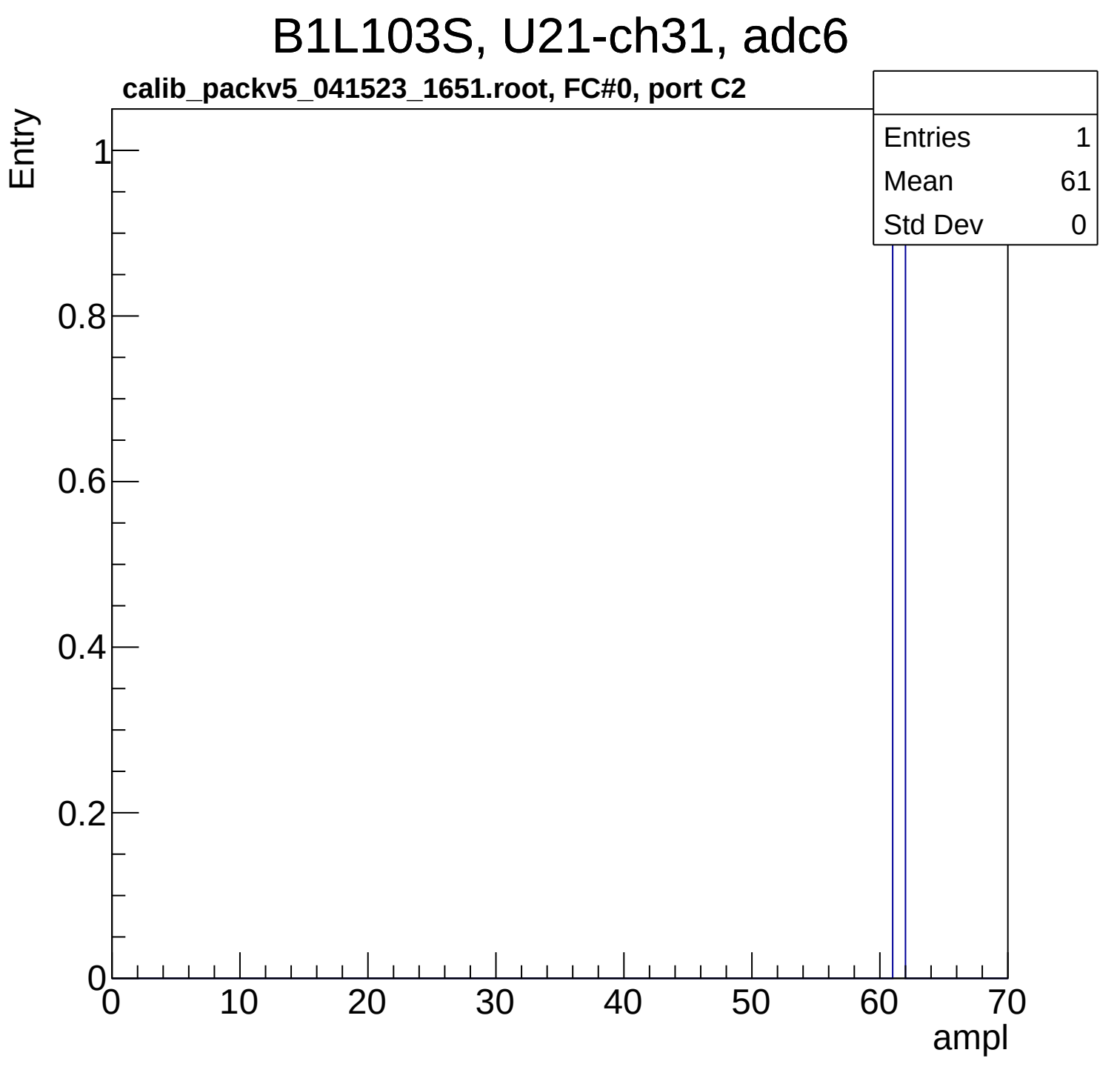
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch31, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 1
Mean 61
Std Dev 0
Entry
ampl
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0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
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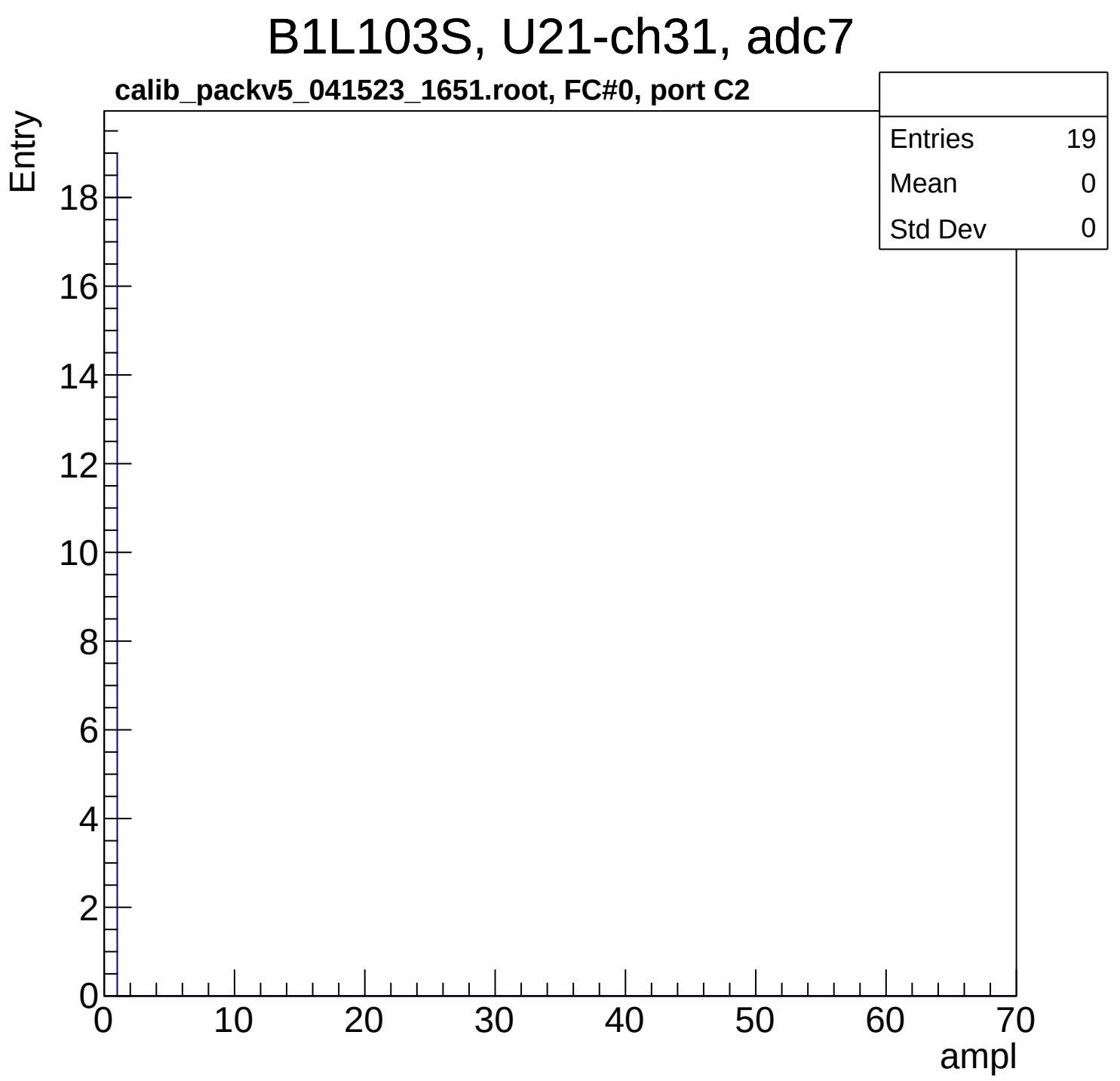
B1L103S, U21-ch31, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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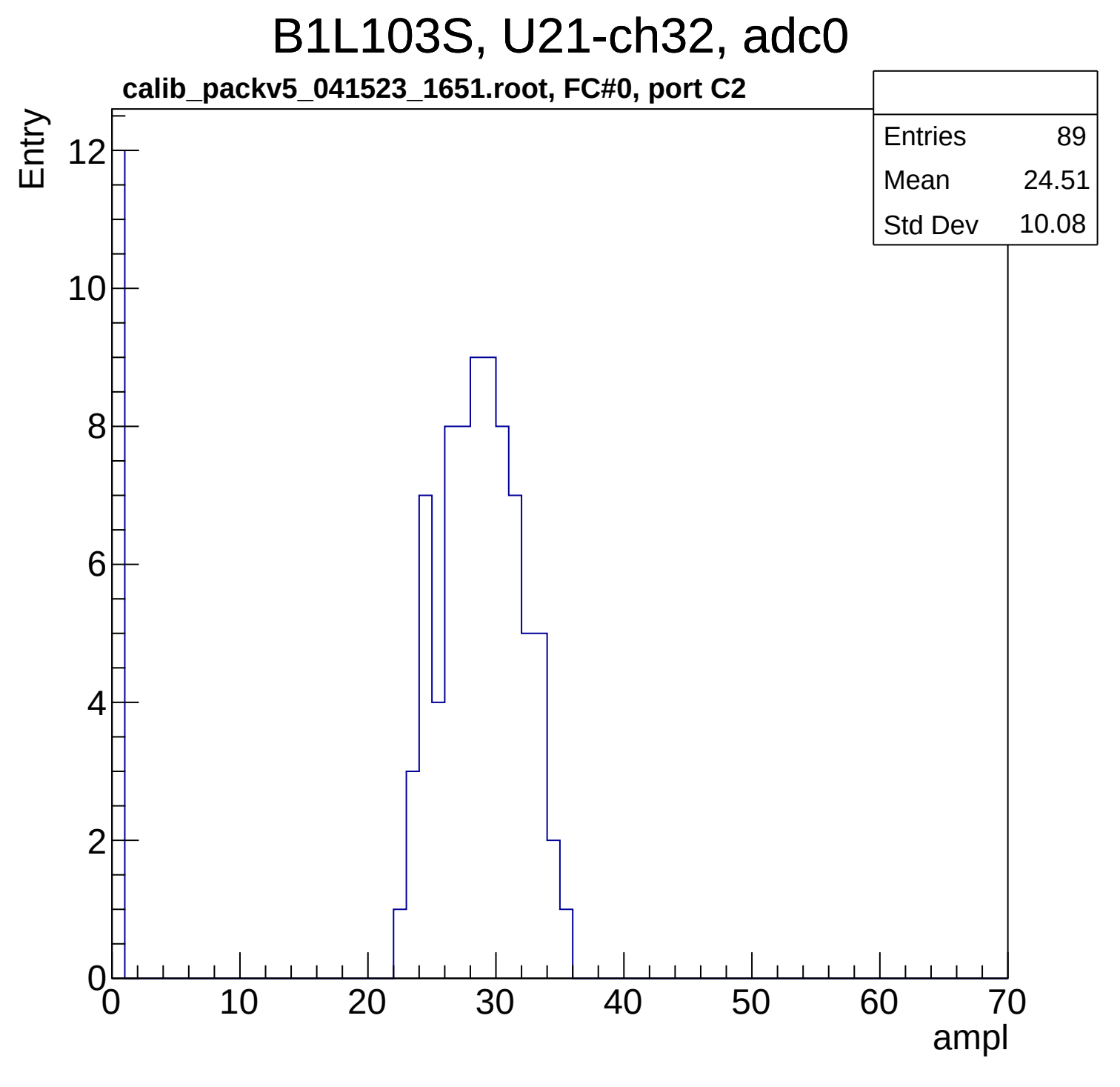
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch32, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 24.51
Std Dev 10.08
Entry
ampl
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6
8
10
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0
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40
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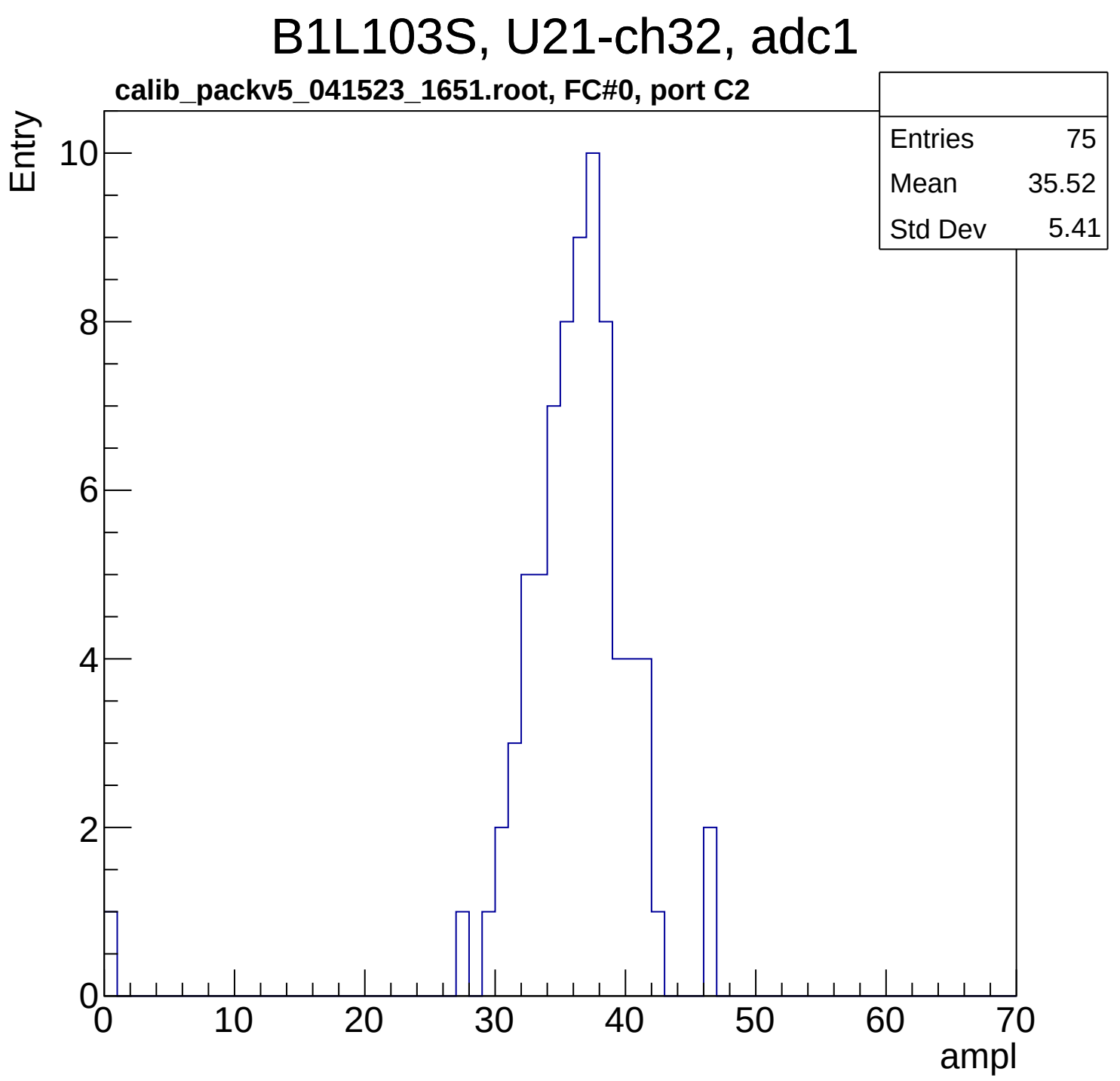
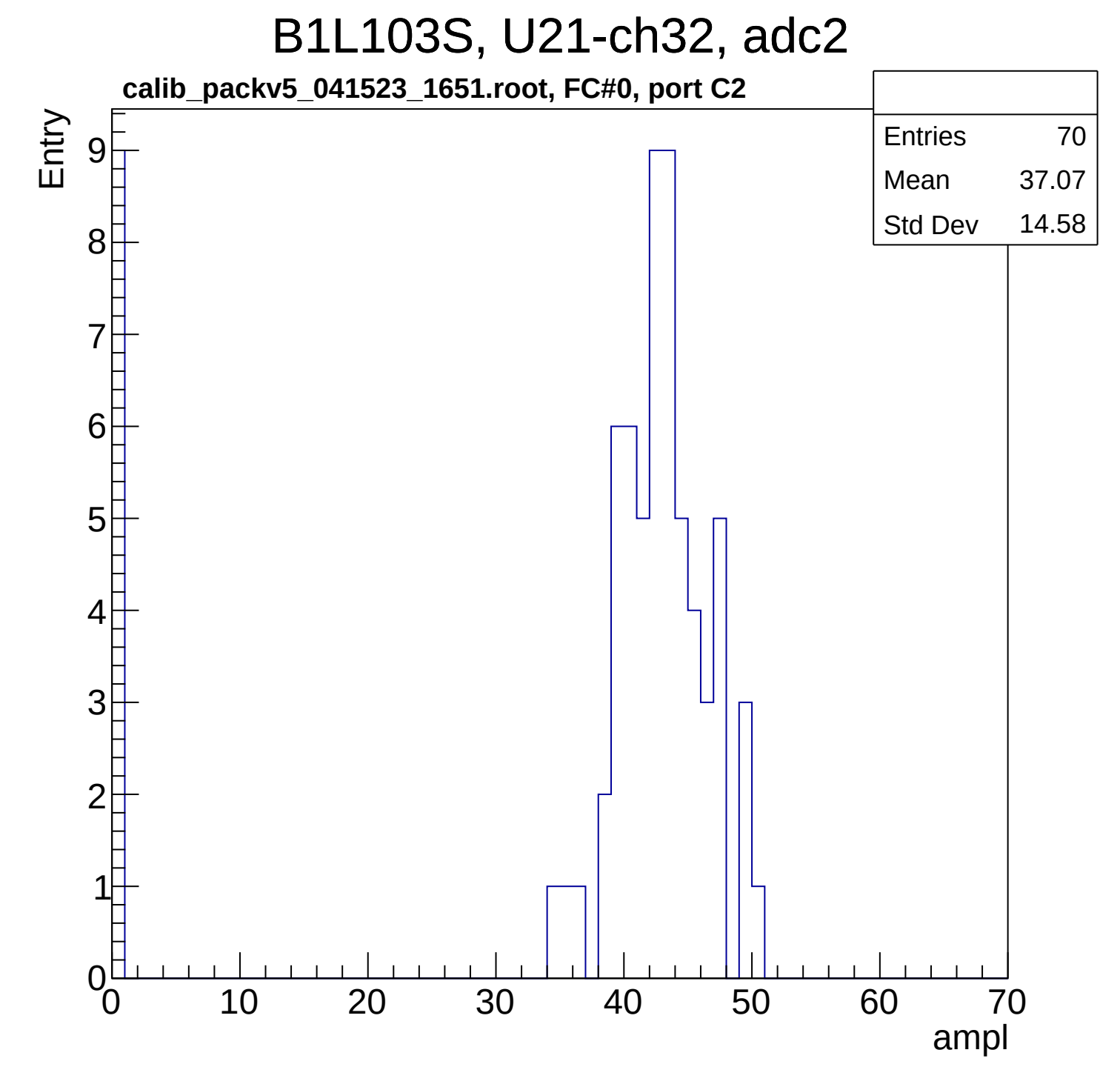

B1L103S, U21-ch32, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 35.52
Std Dev 5.41
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch32, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 37.07
Std Dev 14.58
Entry
ampl
0
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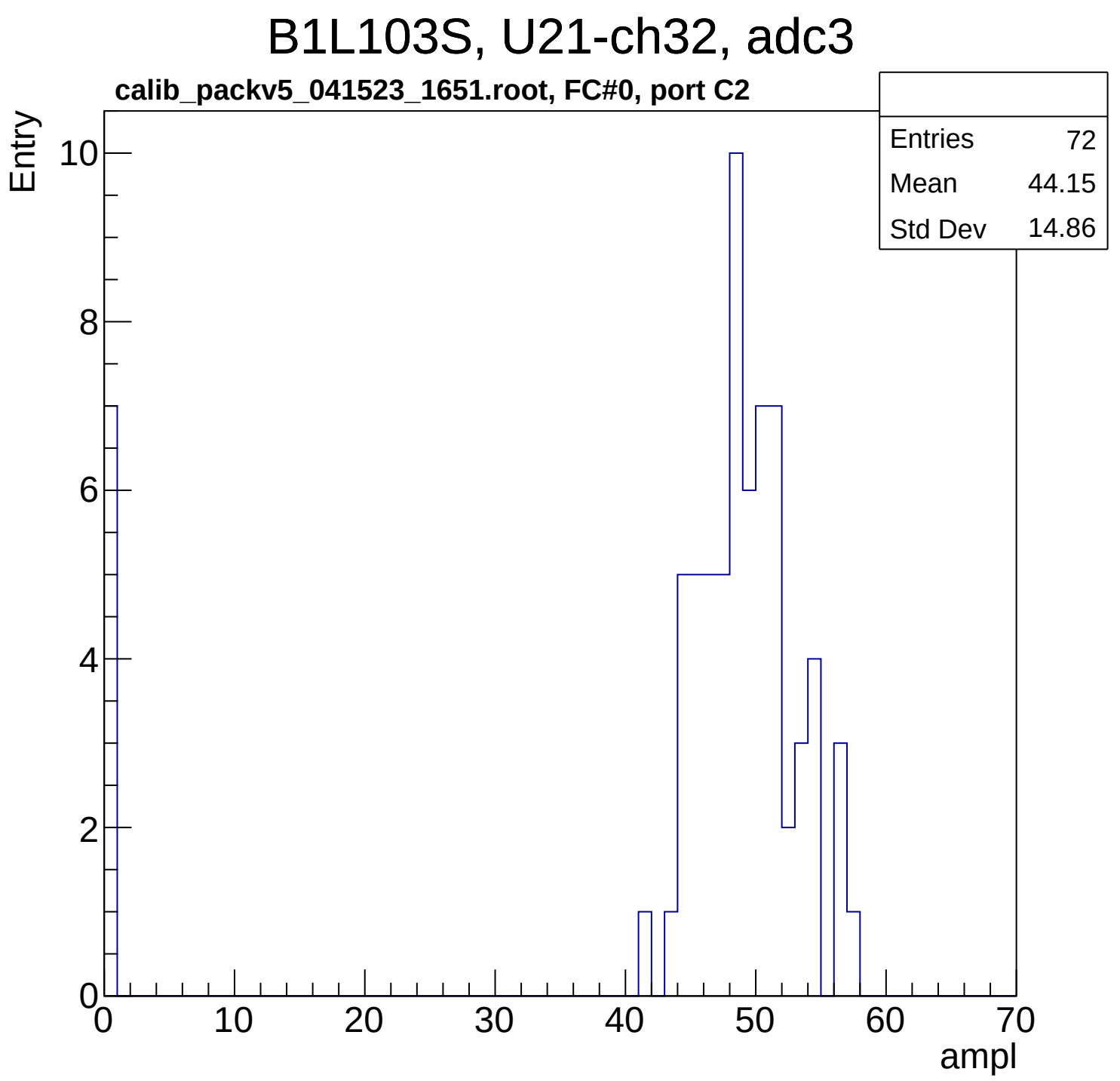
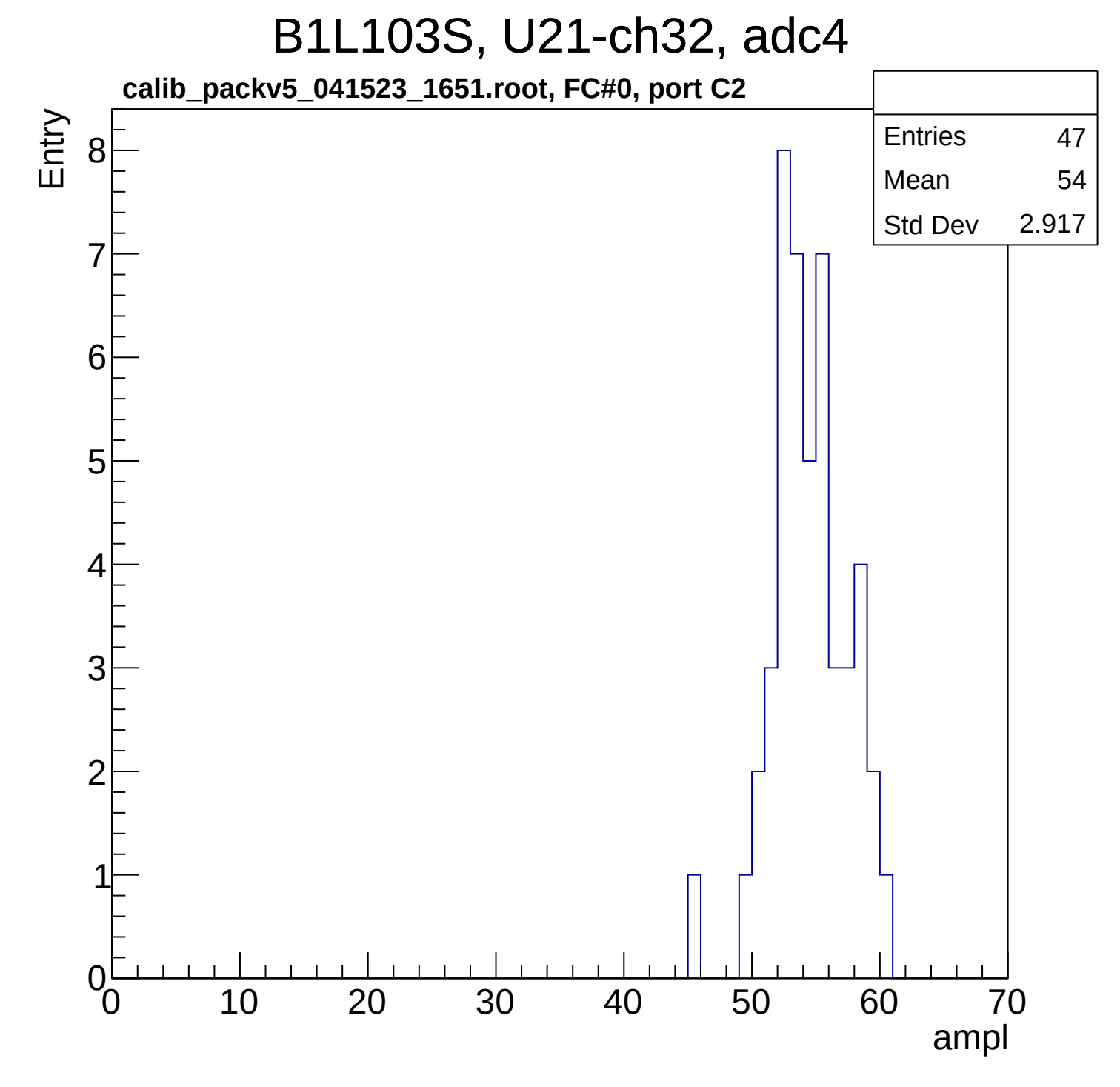
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch32, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 44.15
Std Dev 14.86
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch32, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 54
Std Dev 2.917
Entry
ampl
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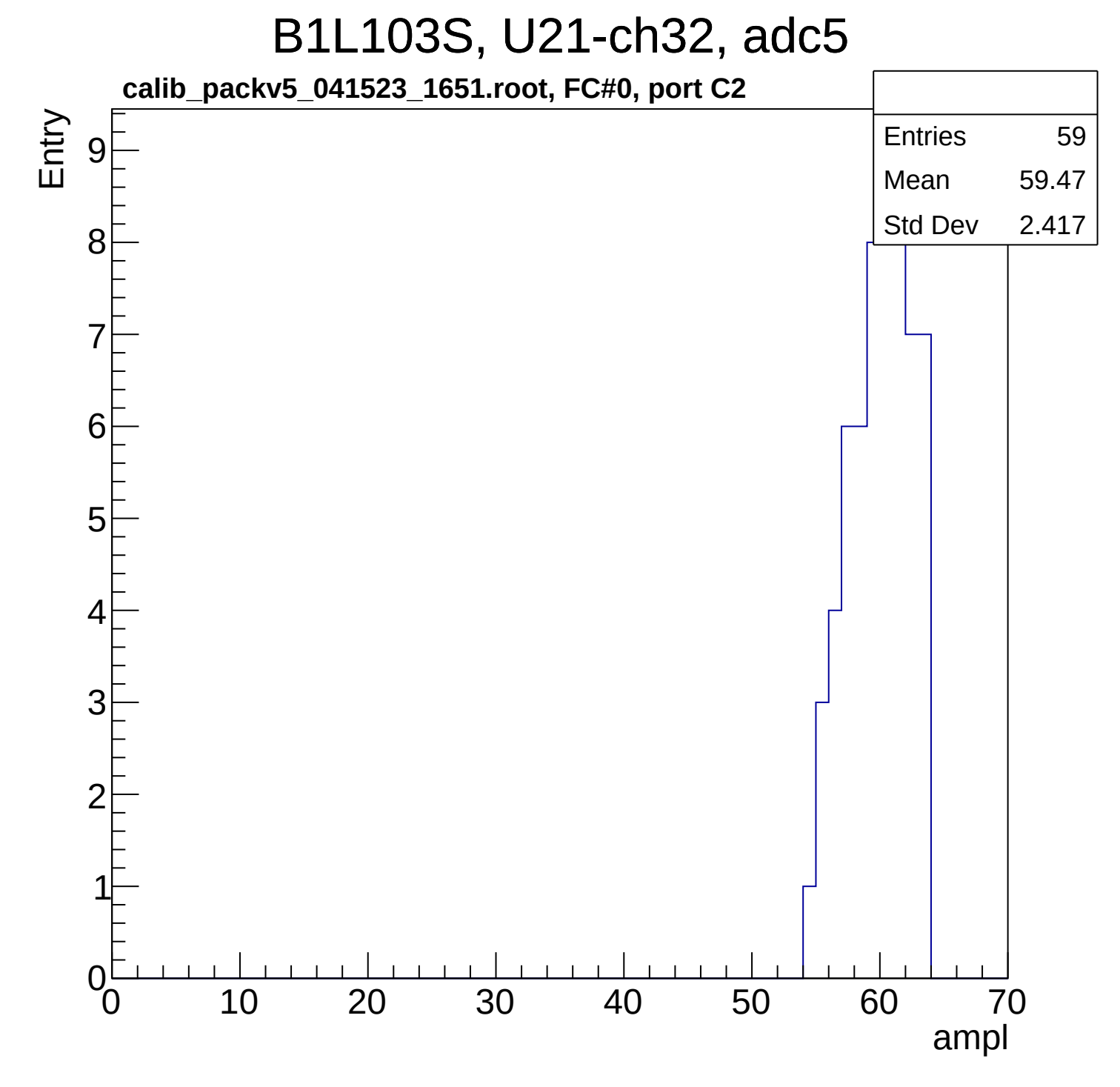
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch32, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 59.47
Std Dev 2.417
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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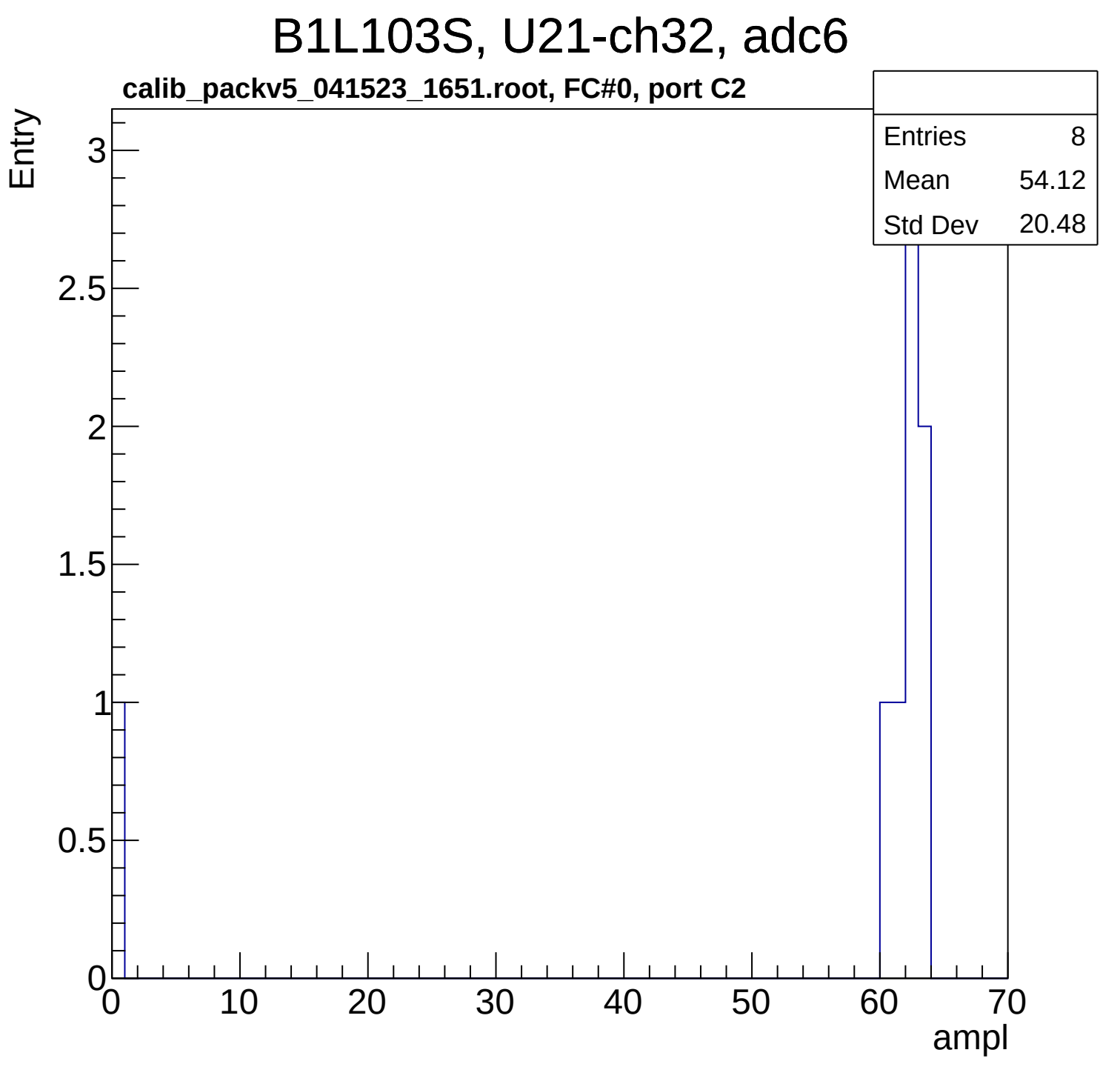
B1L103S, U21-ch32, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 54.12
Std Dev 20.48
Entry
ampl
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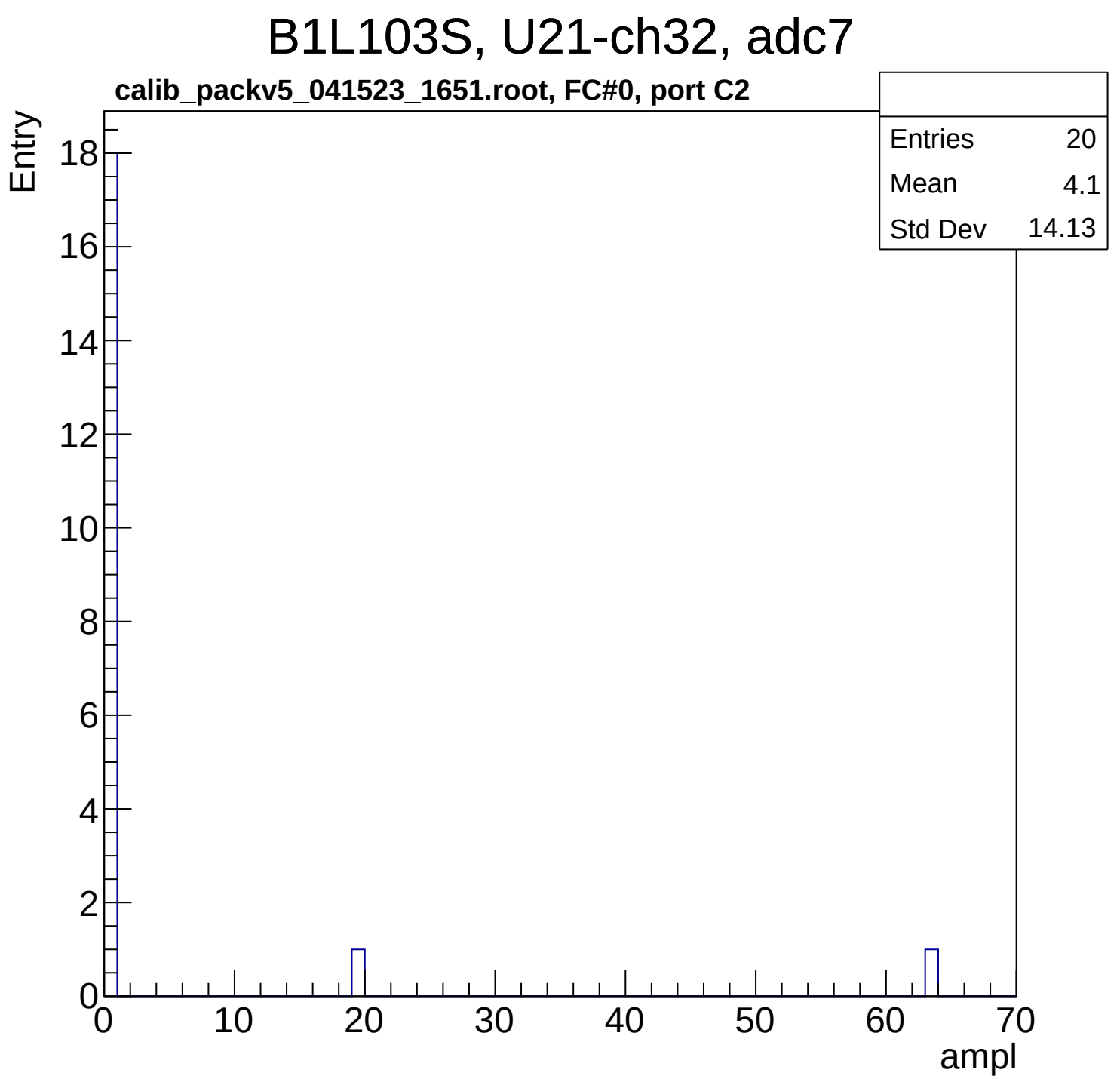
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U21-ch32, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4.1
Std Dev 14.13
Entry
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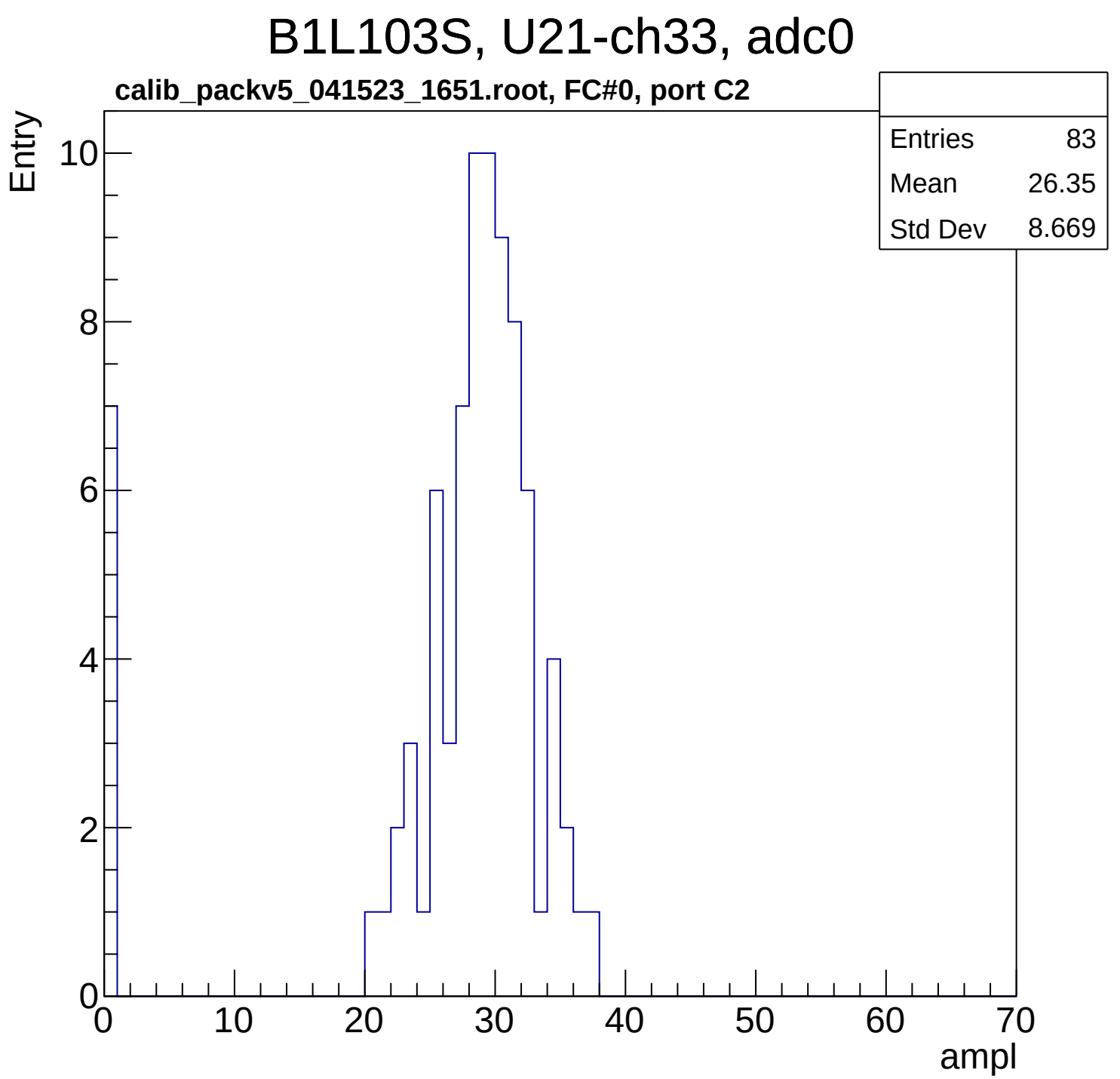
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch33, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 26.35
Std Dev 8.669
Entry
ampl
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4
6
8
10
0
10
20
30
40
50
60
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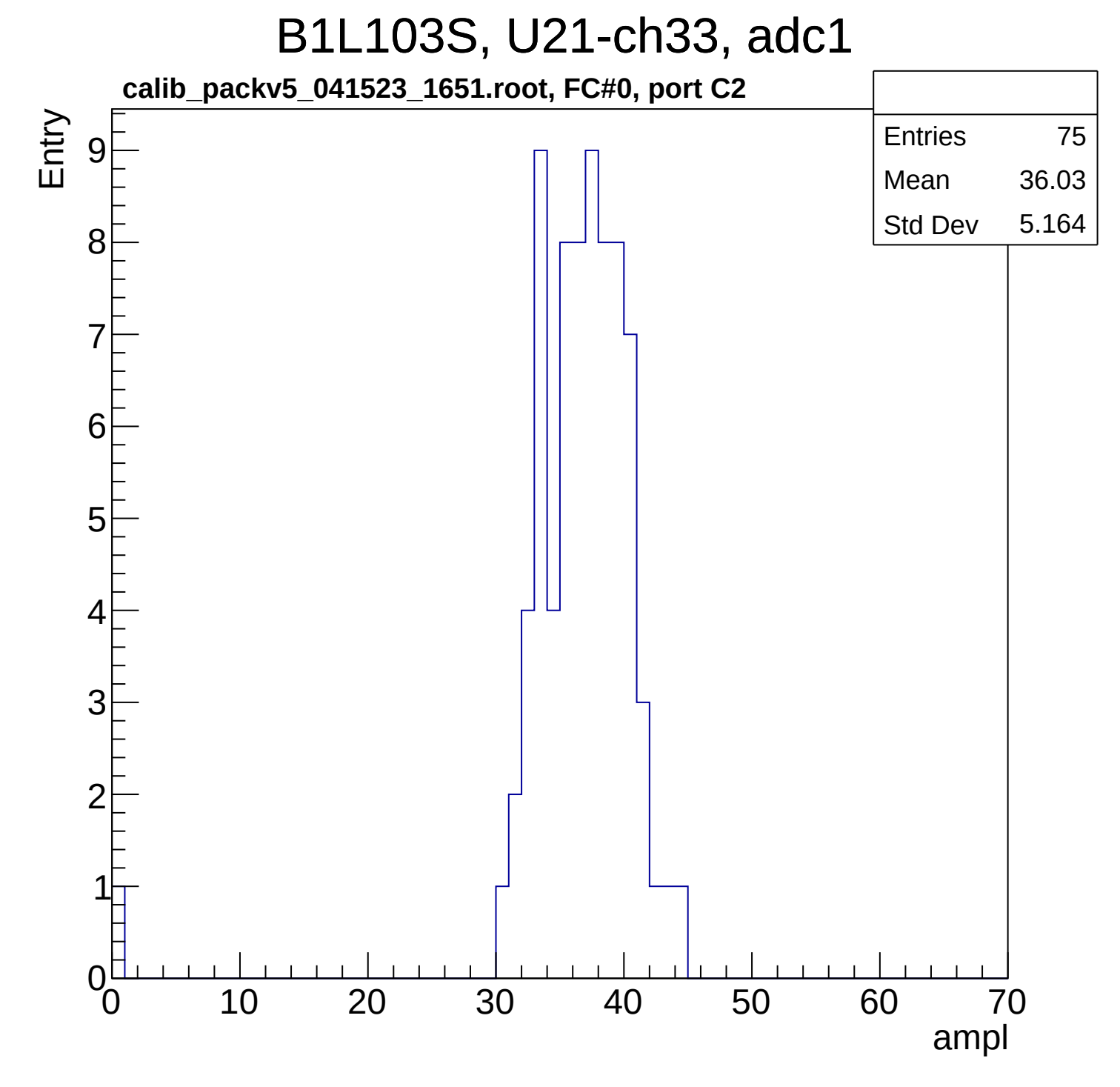
B1L103S, U21-ch33, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 36.03
Std Dev 5.164
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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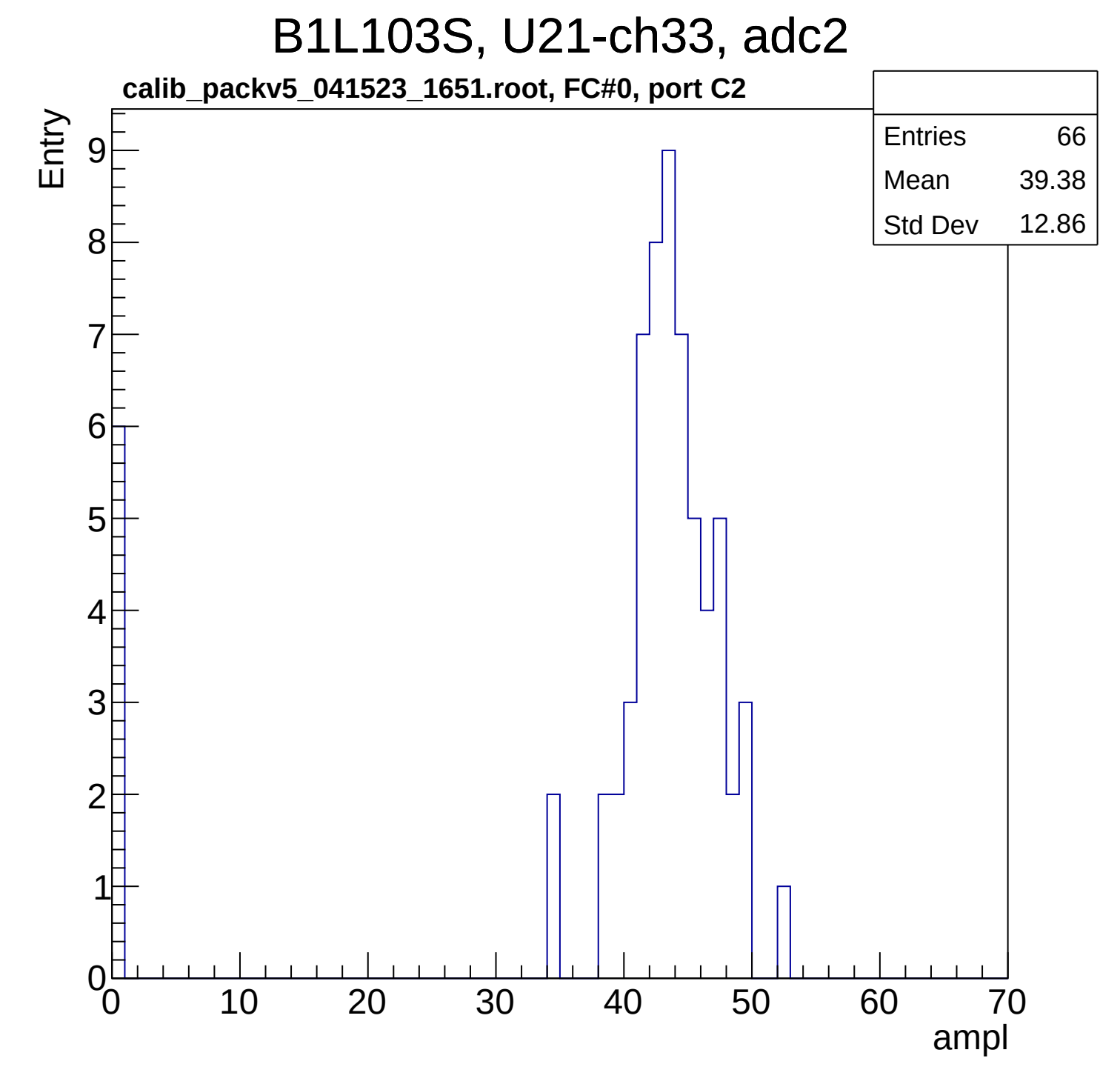
B1L103S, U21-ch33, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 39.38
Std Dev 12.86
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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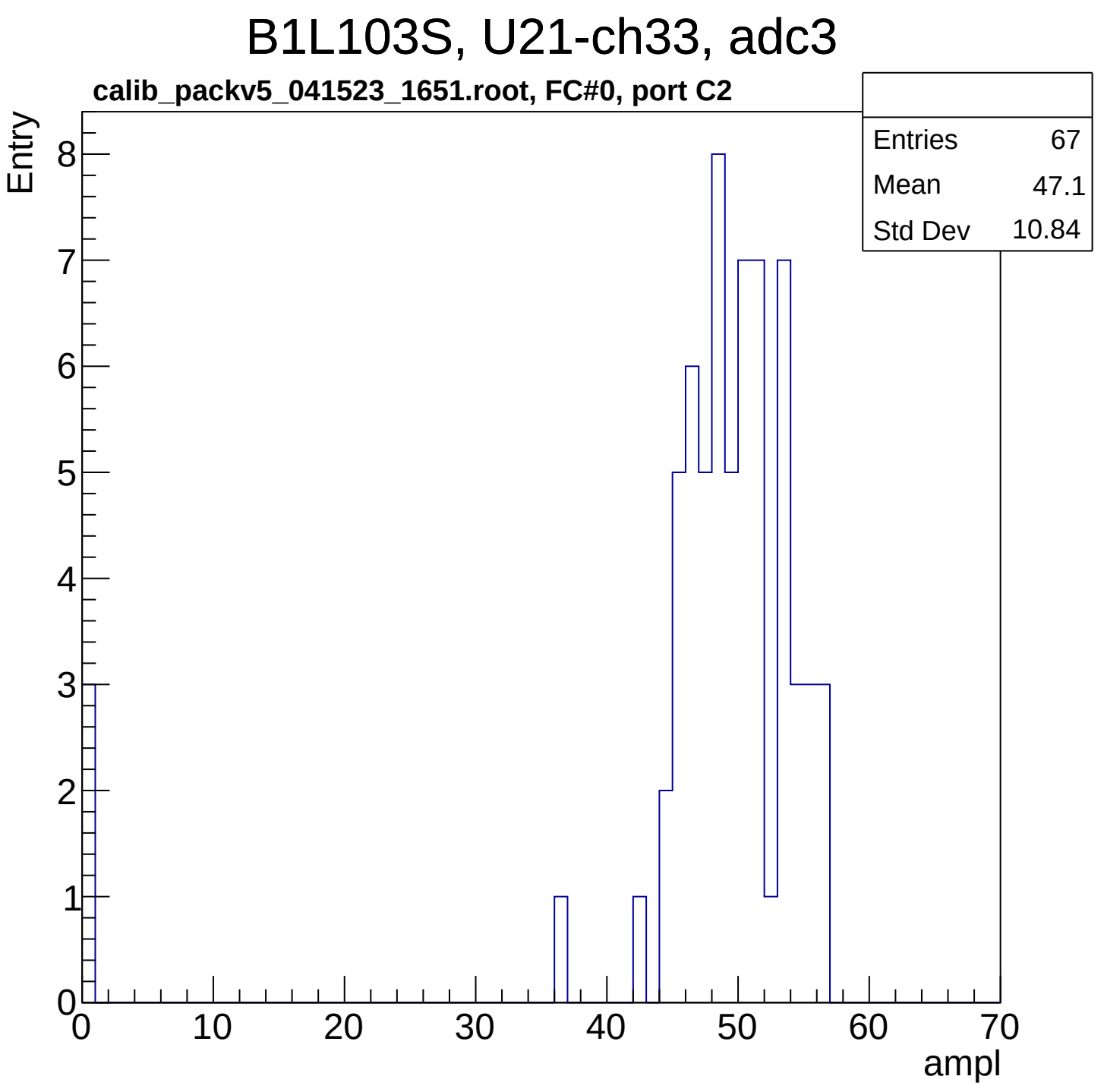
40
50
60
70


B1L103S, U21-ch33, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 47.1
Std Dev 10.84
Entry
ampl
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4
5
6
7
8
0
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20
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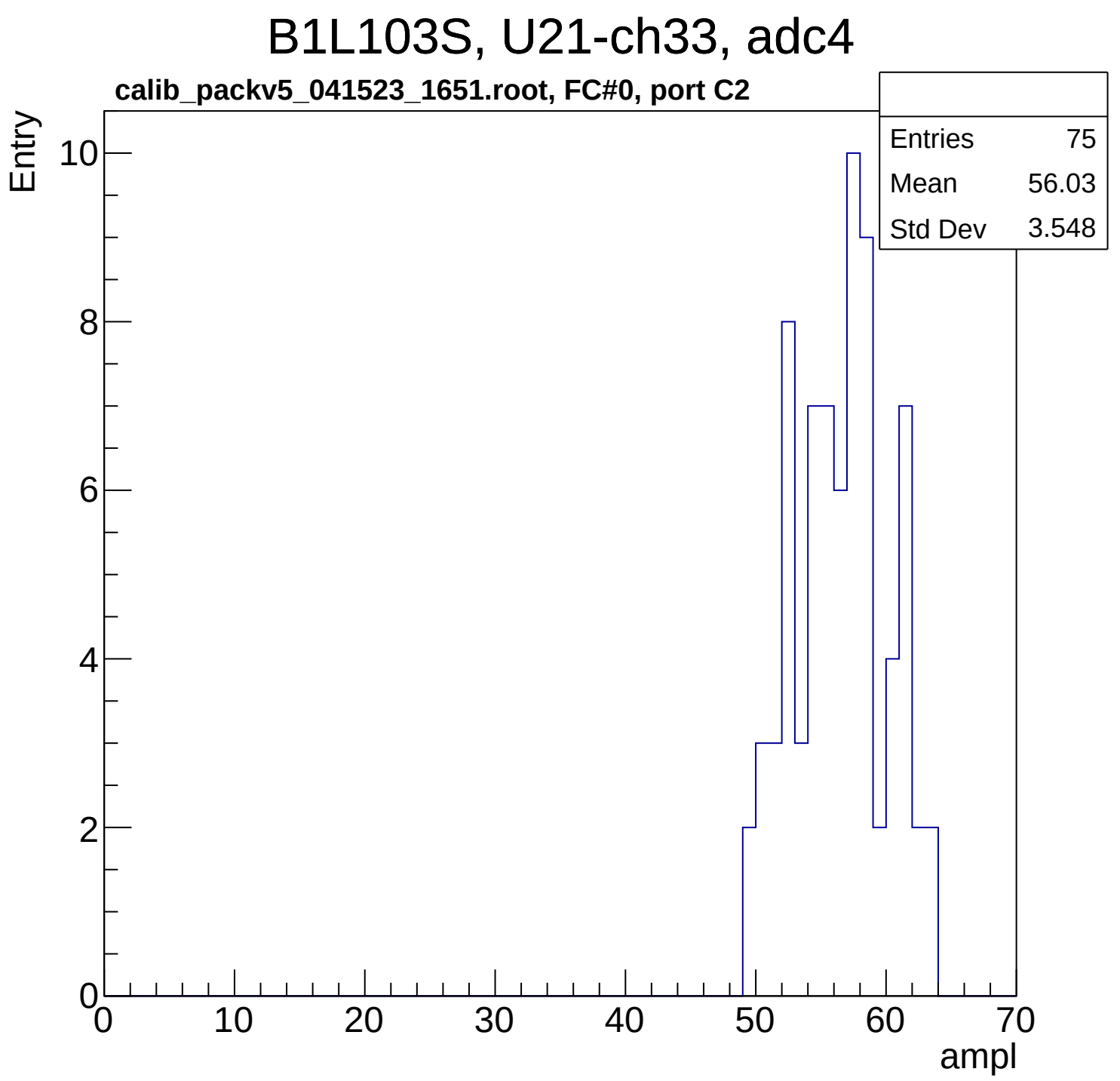
B1L103S, U21-ch33, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 56.03
Std Dev 3.548
Entry
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20
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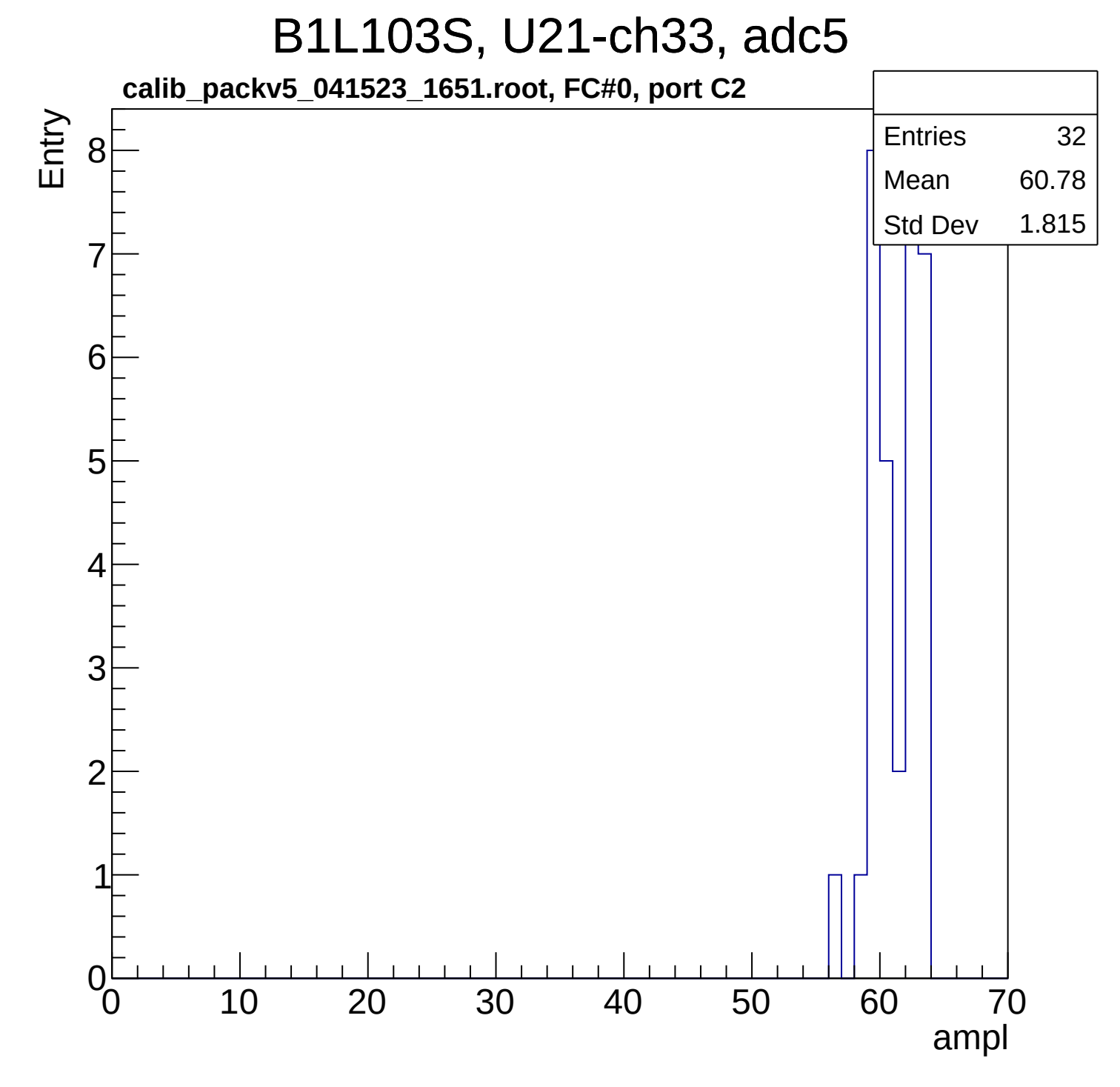
70
ampl


B1L103S, U21-ch33, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 60.78
Std Dev 1.815
Entry
ampl
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5
6
7
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0
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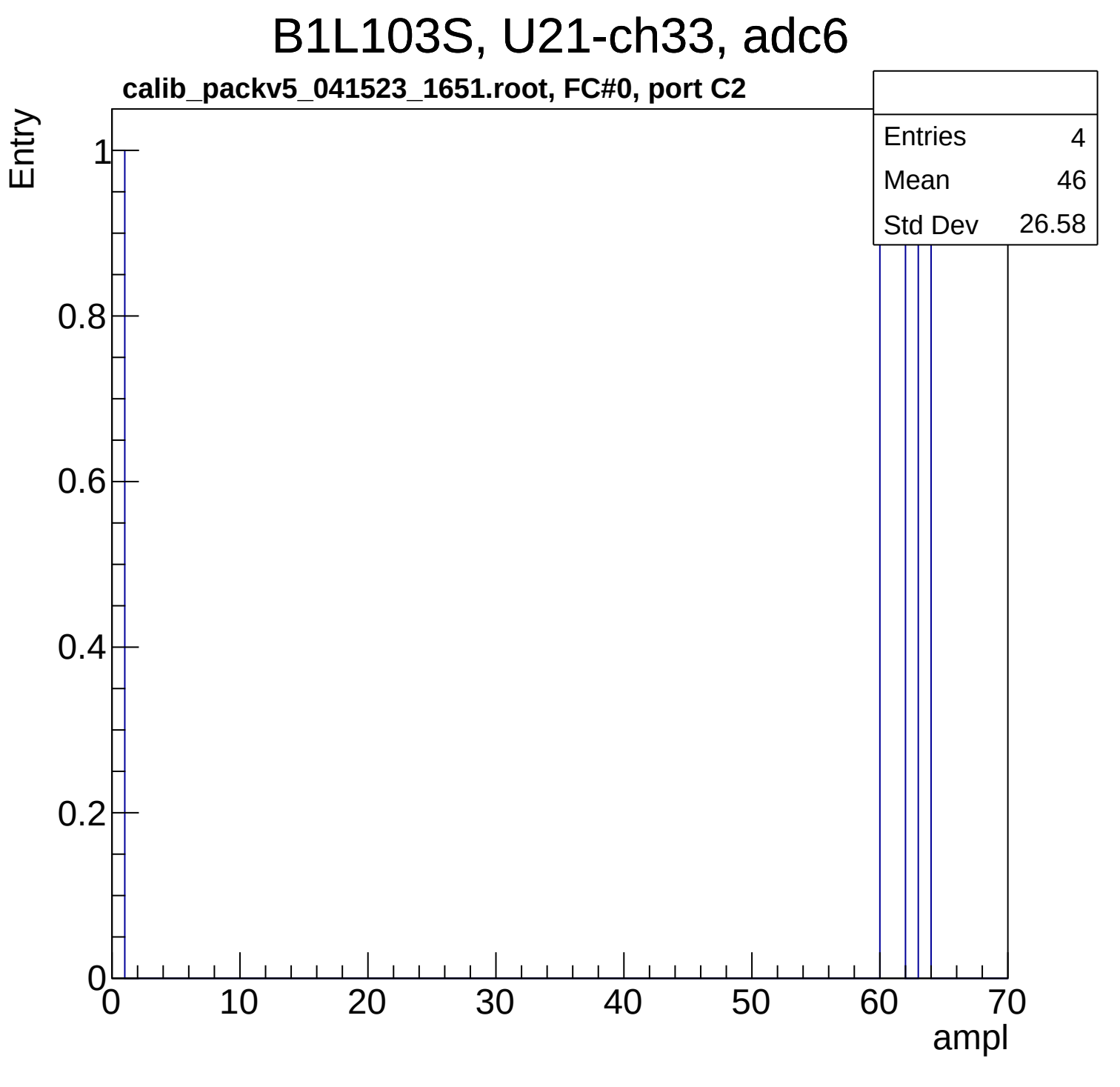
B1L103S, U21-ch33, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 46
Std Dev 26.58
Entry
ampl
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0.8
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0
10
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40
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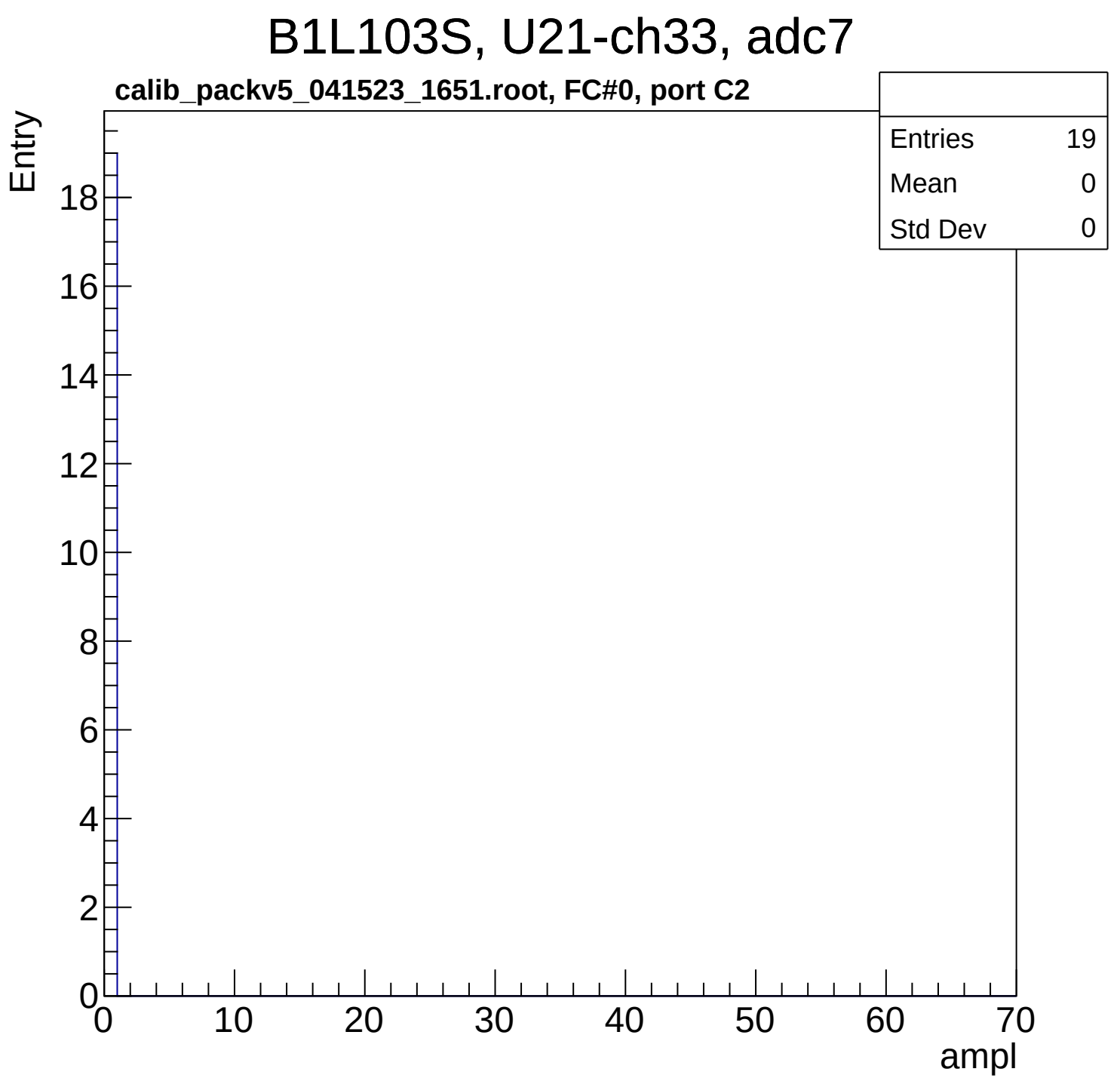
B1L103S, U21-ch33, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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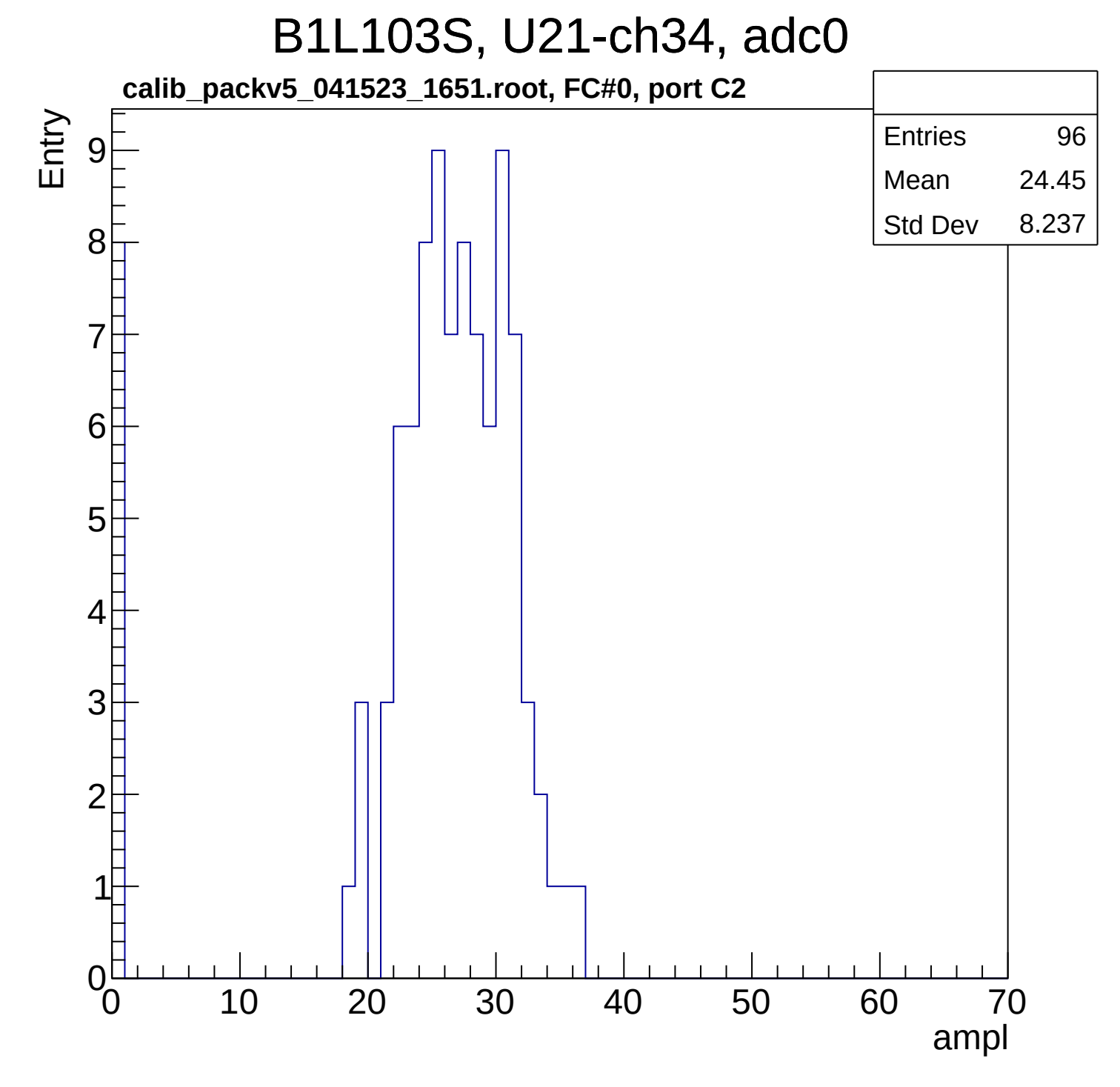
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch34, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 96
Mean 24.45
Std Dev 8.237
Entry
ampl
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6
7
8
9
0
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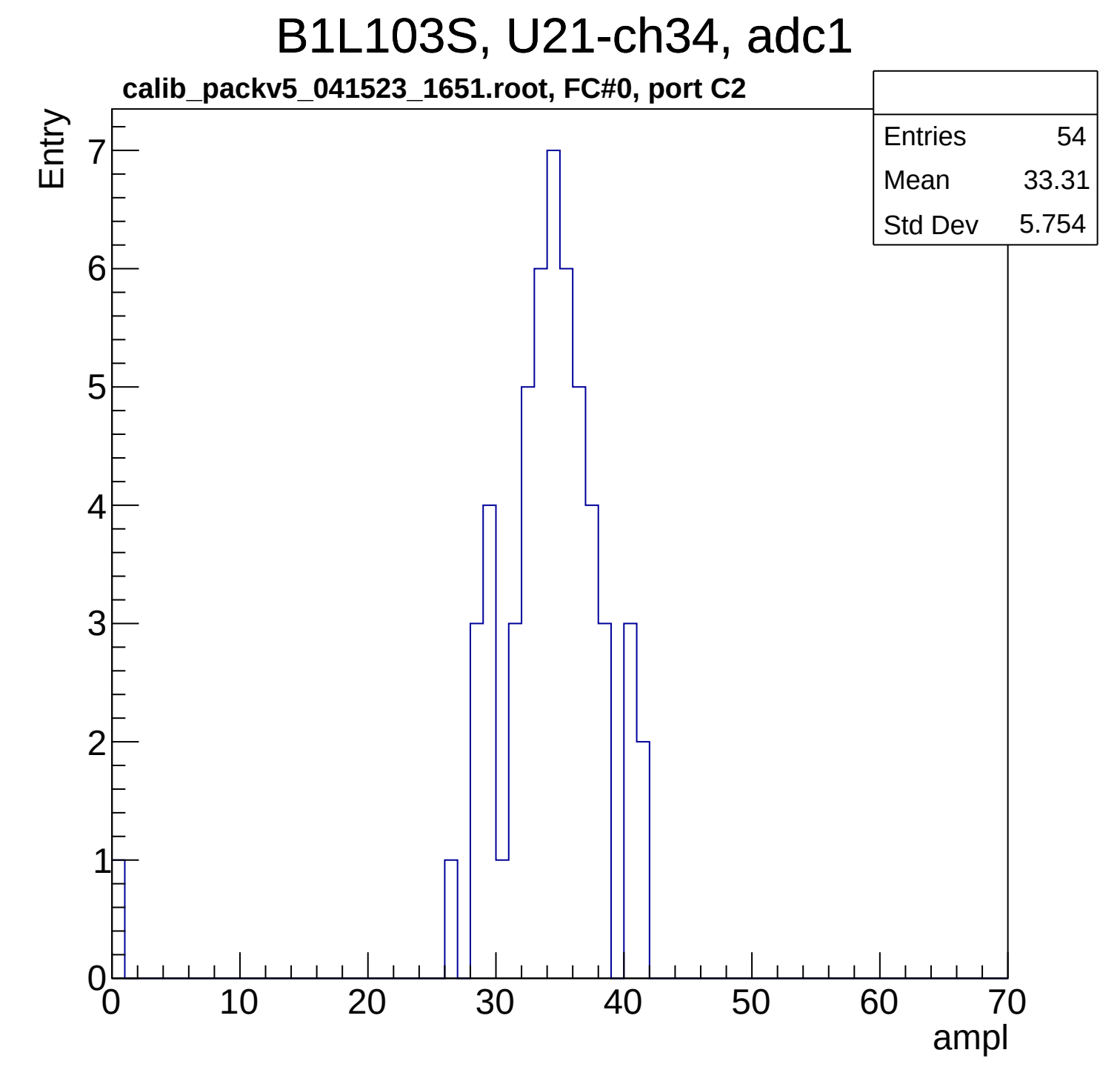
B1L103S, U21-ch34, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 33.31
Std Dev 5.754
Entry
ampl
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1
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4
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6
7
0
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20
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60
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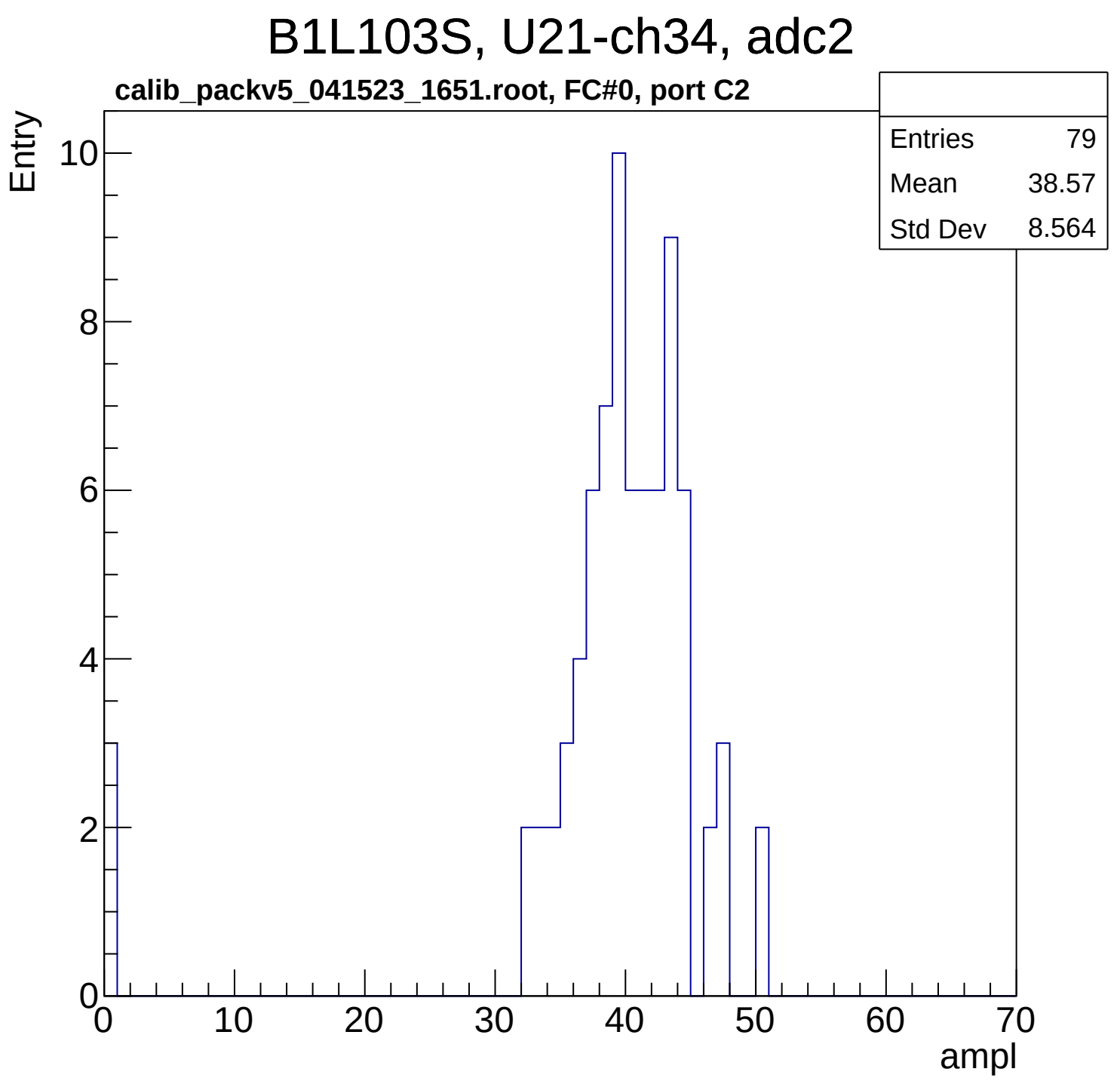
B1L103S, U21-ch34, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 38.57
Std Dev 8.564
Entry
ampl
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0
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60
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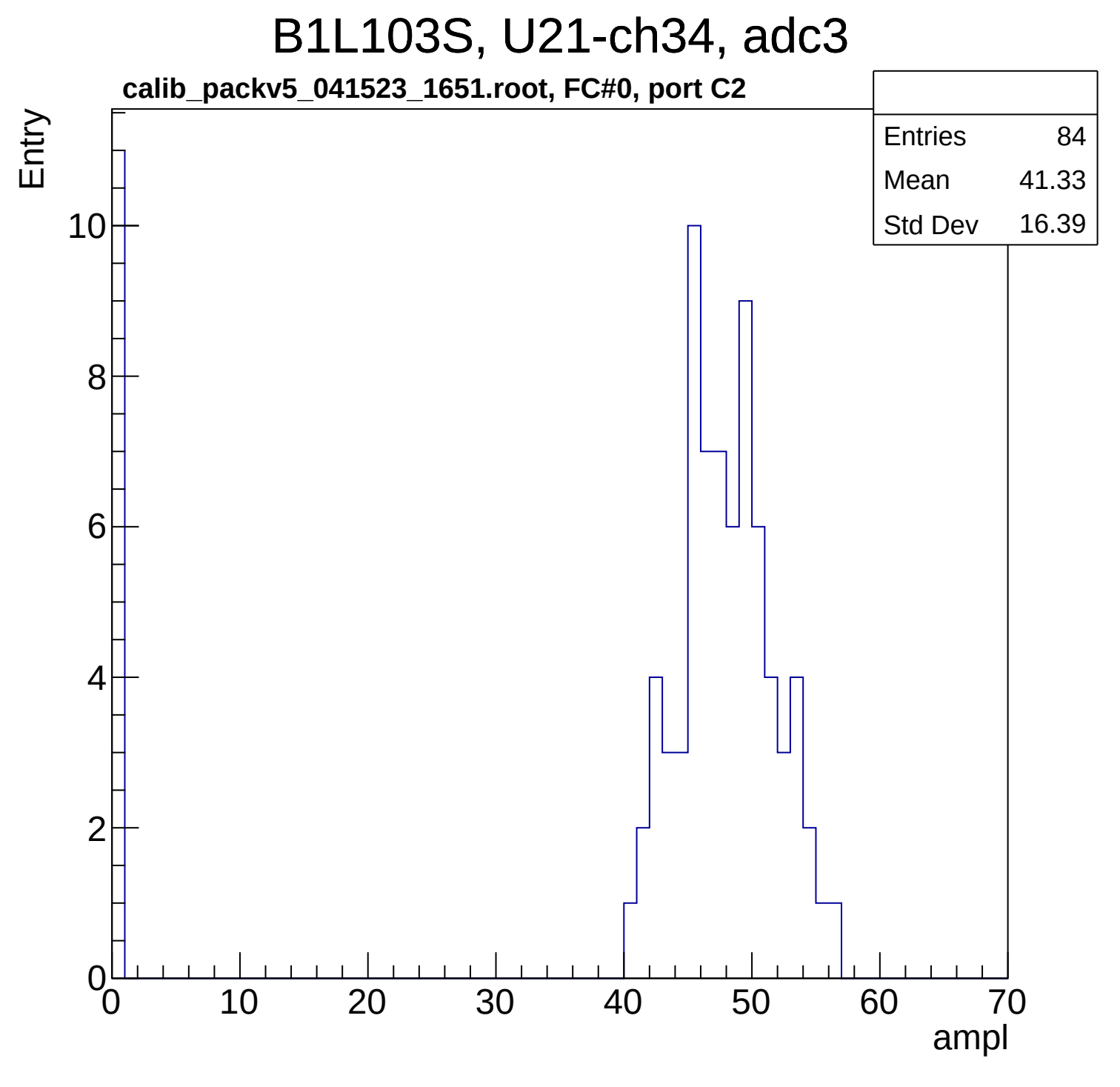
B1L103S, U21-ch34, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 41.33
Std Dev 16.39
Entry
ampl
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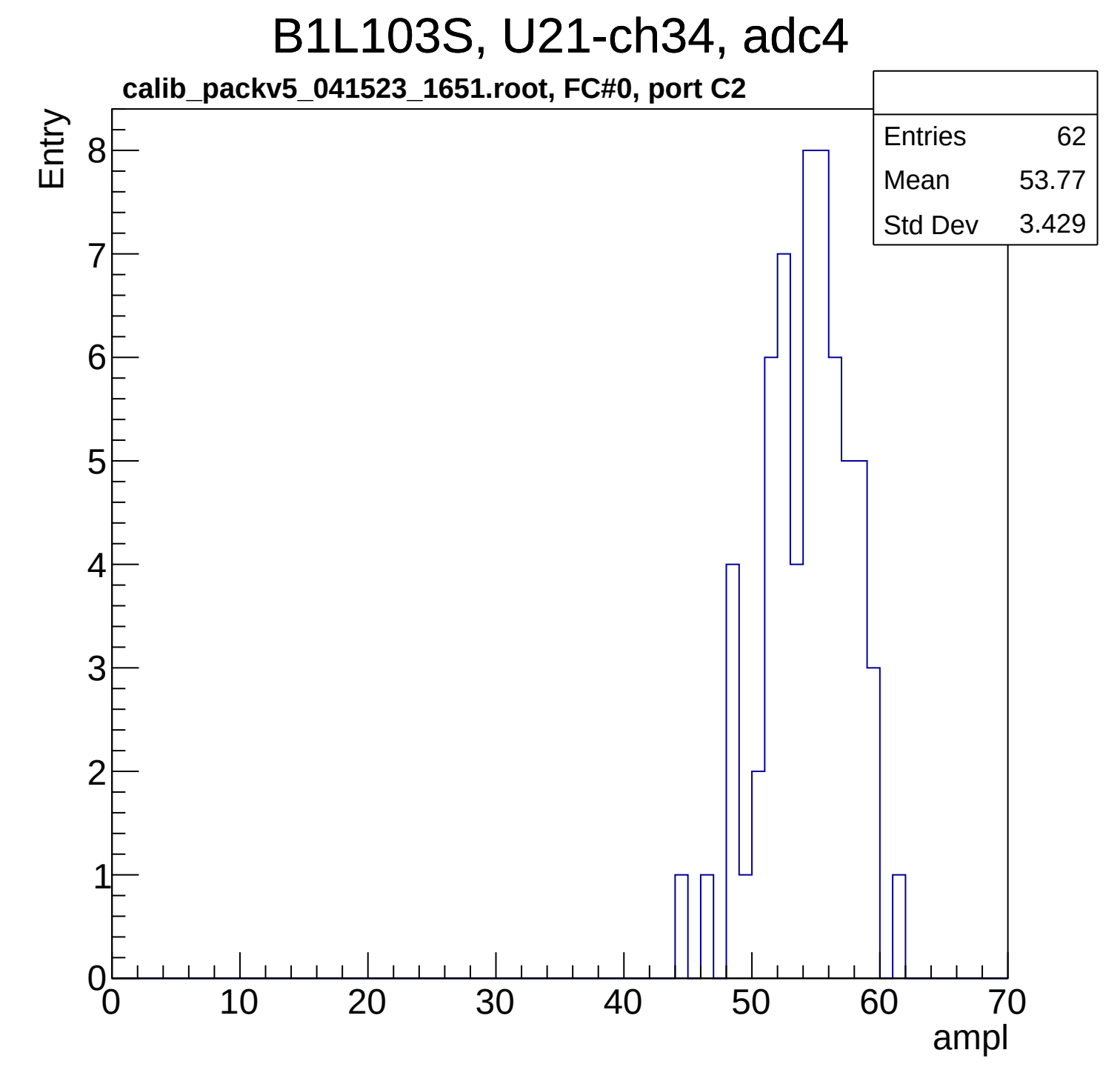
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U21-ch34, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 53.77
Std Dev 3.429
Entry
ampl
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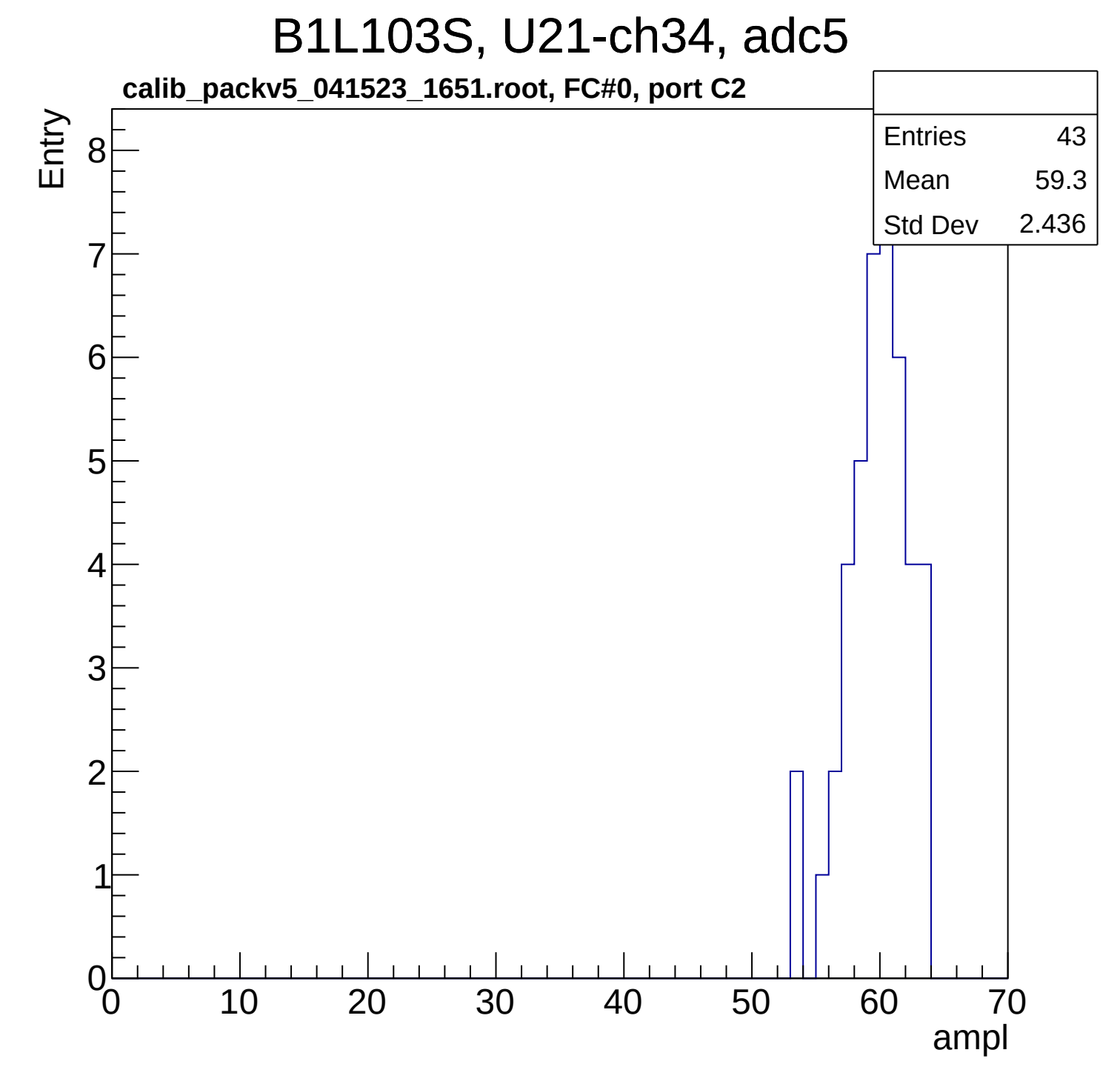
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch34, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 59.3
Std Dev 2.436
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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40
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60
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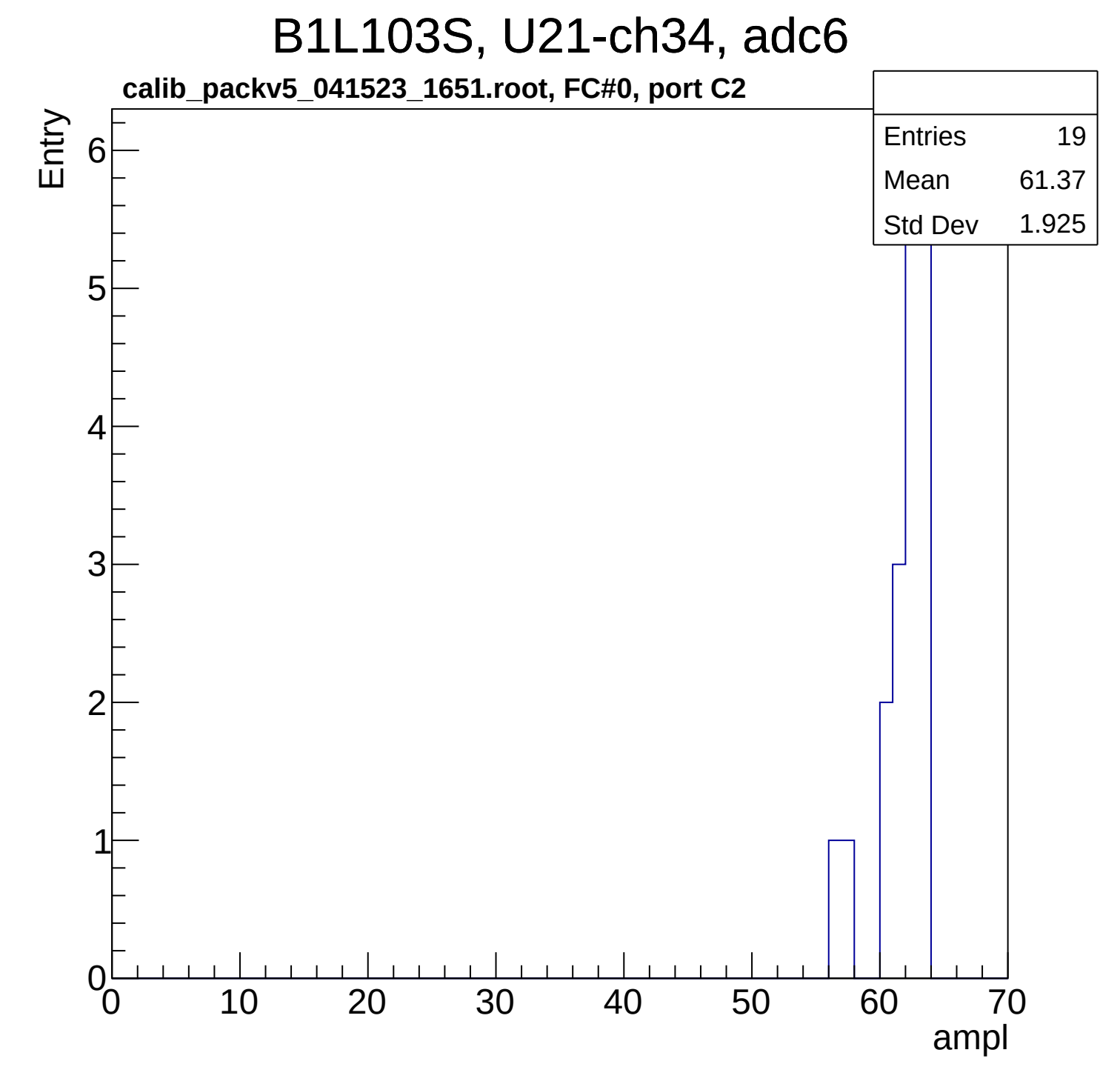
B1L103S, U21-ch34, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 61.37
Std Dev 1.925
Entry
ampl
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2
3
4
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6
0
10
20
30
40
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60
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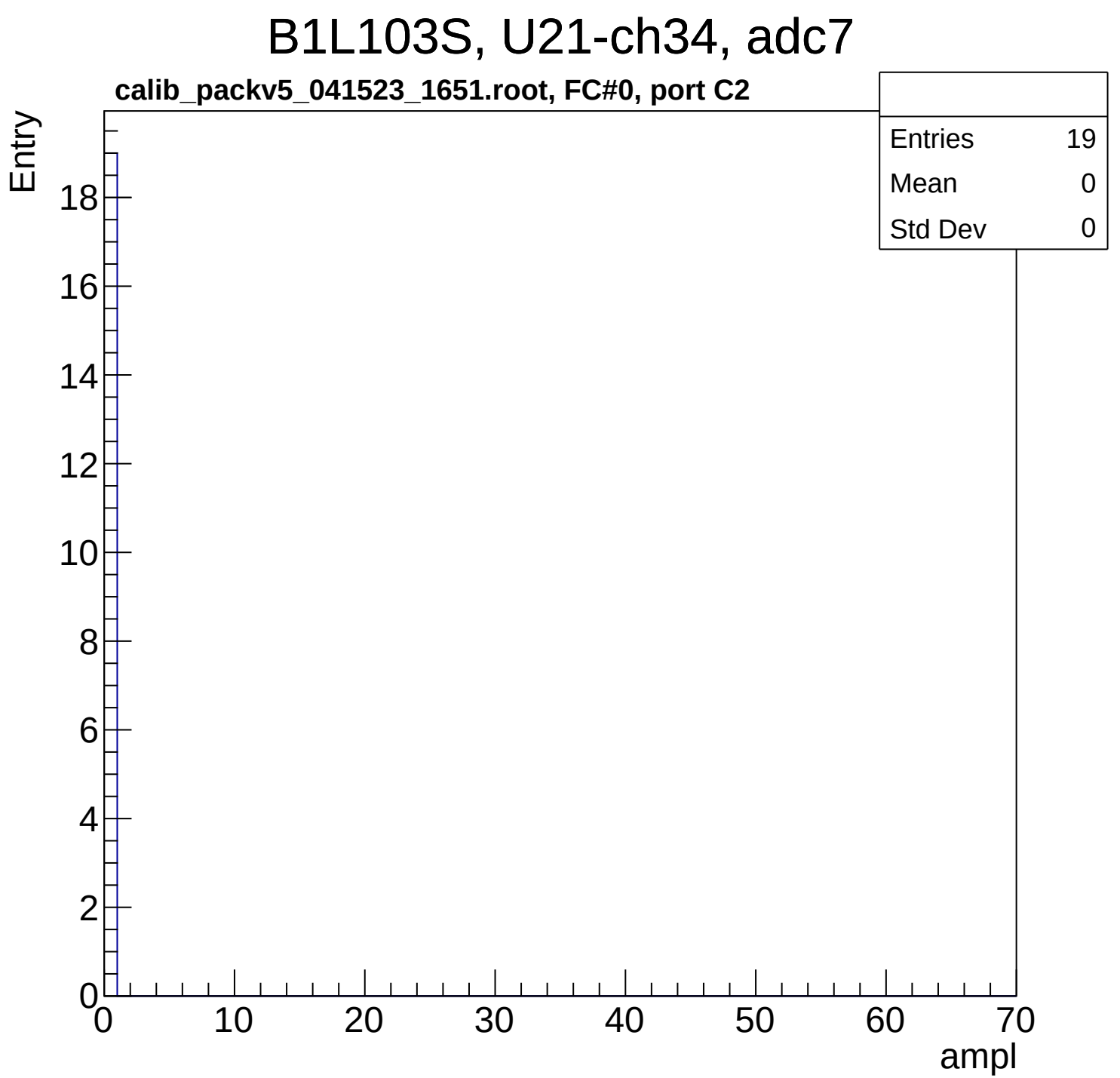
B1L103S, U21-ch34, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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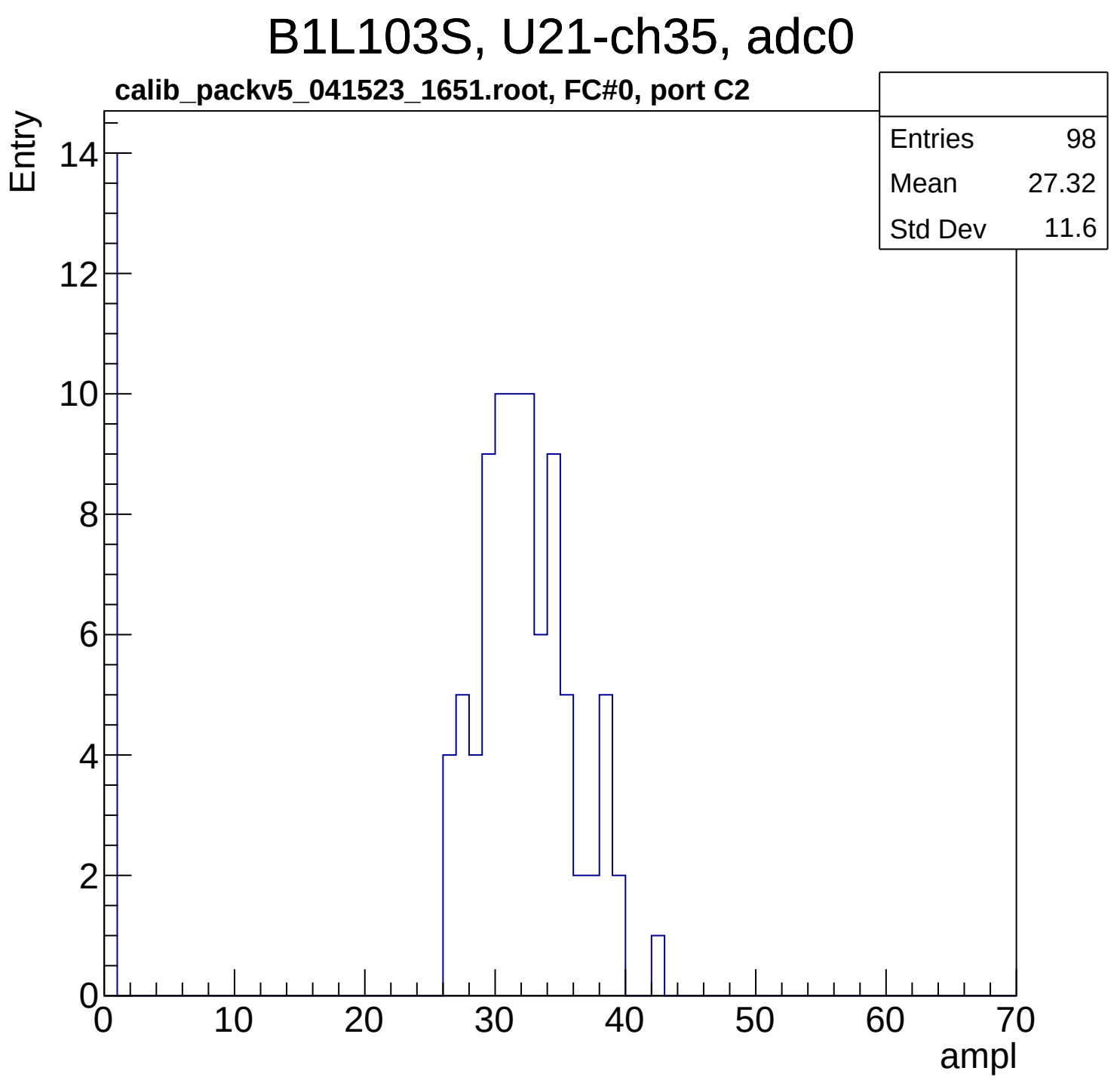
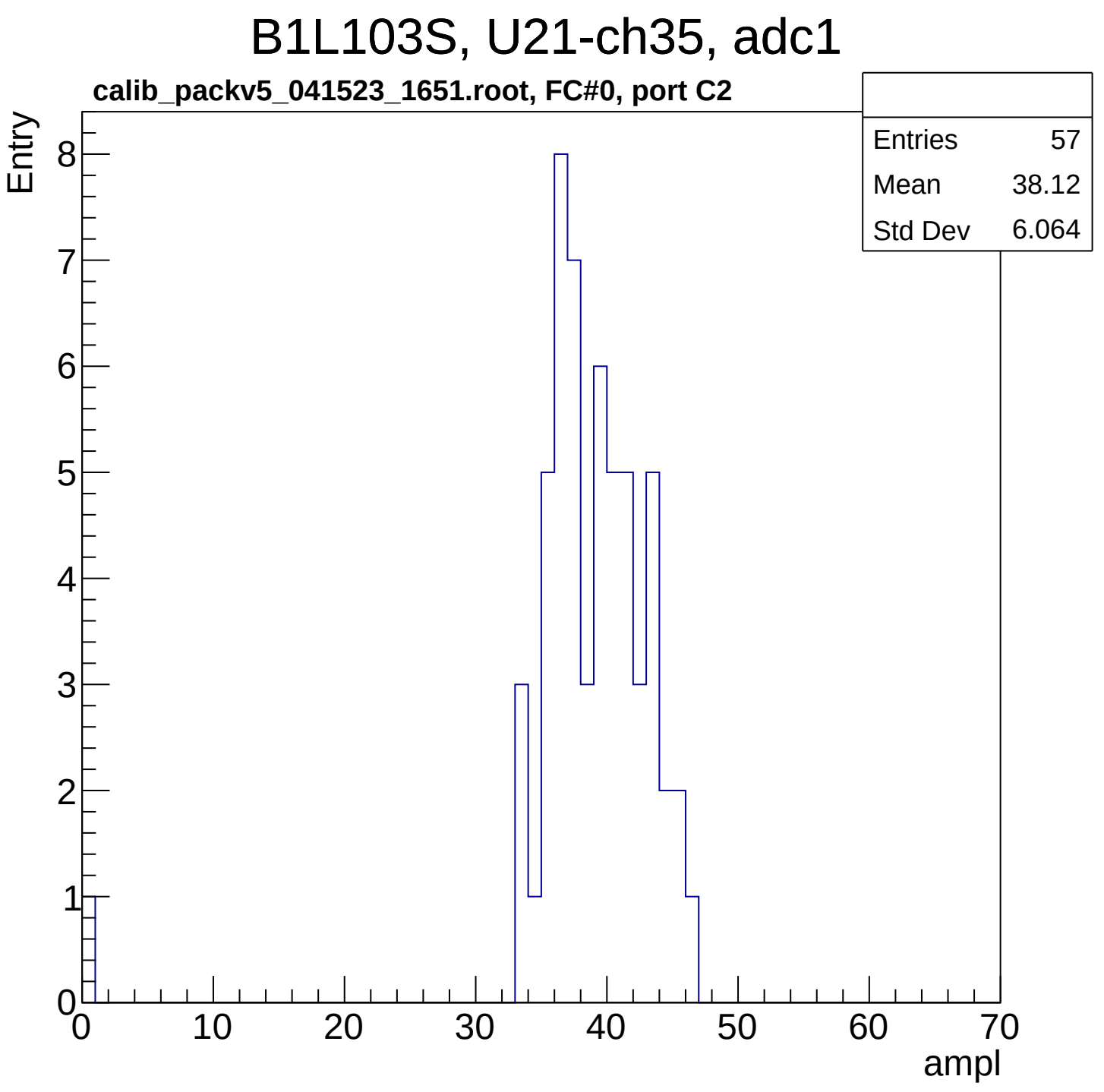
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch35, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 98
Mean 27.32
Std Dev 11.6
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U21-ch35, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 38.12
Std Dev 6.064
Entry
ampl
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1
2
3
4
5
6
7
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0
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40
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60
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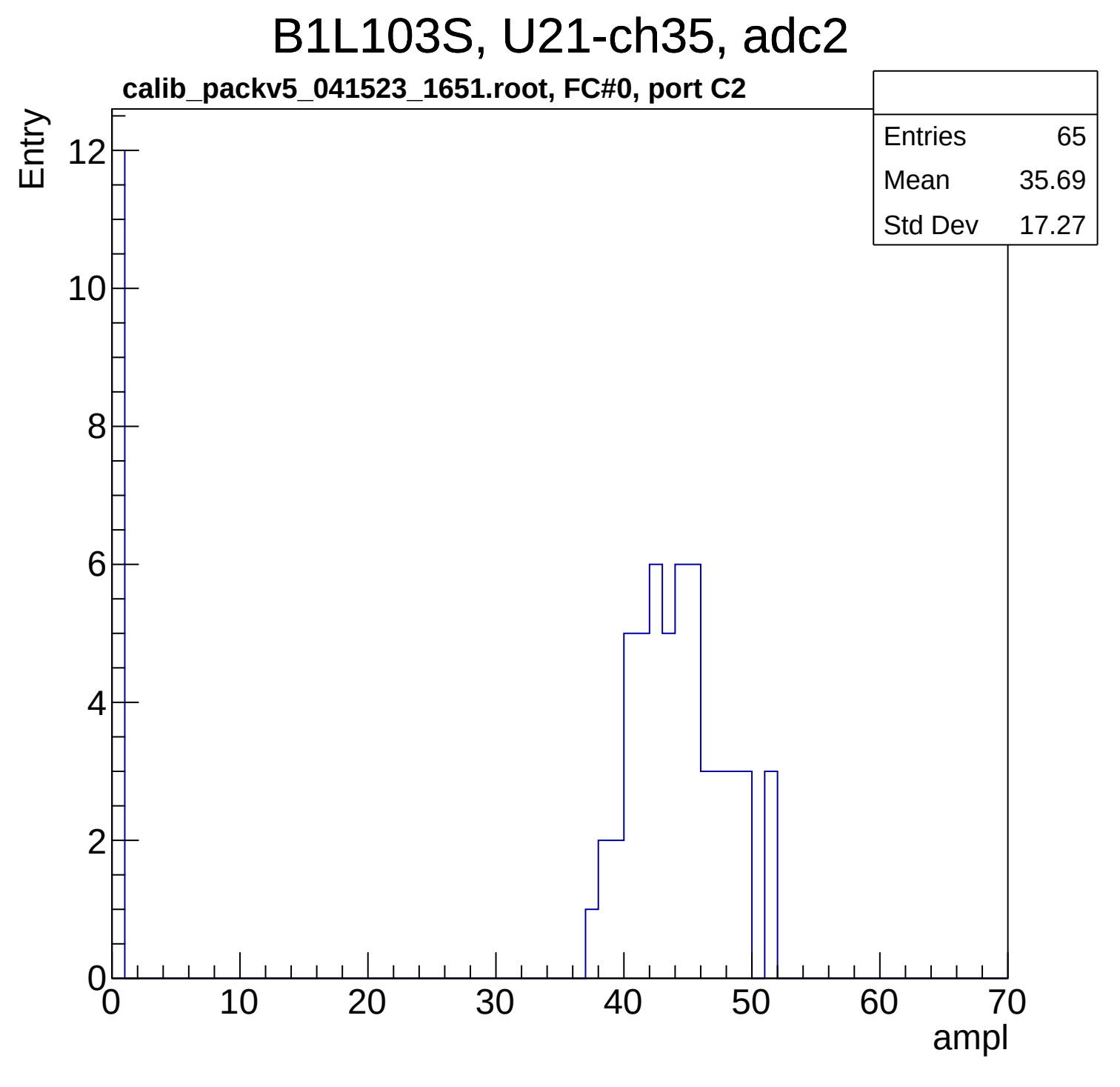
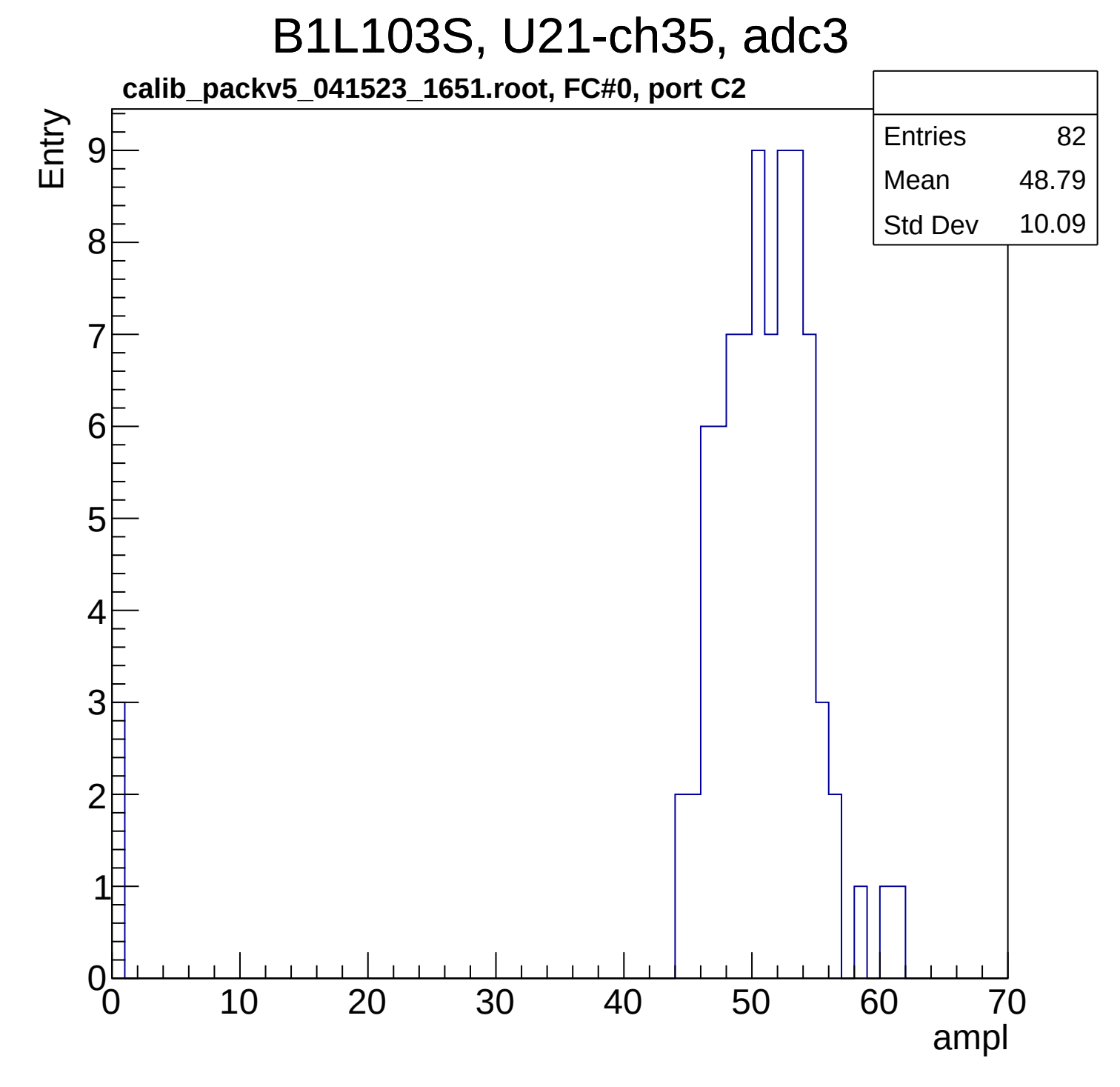

B1L103S, U21-ch35, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 35.69
Std Dev 17.27
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch35, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 48.79
Std Dev 10.09
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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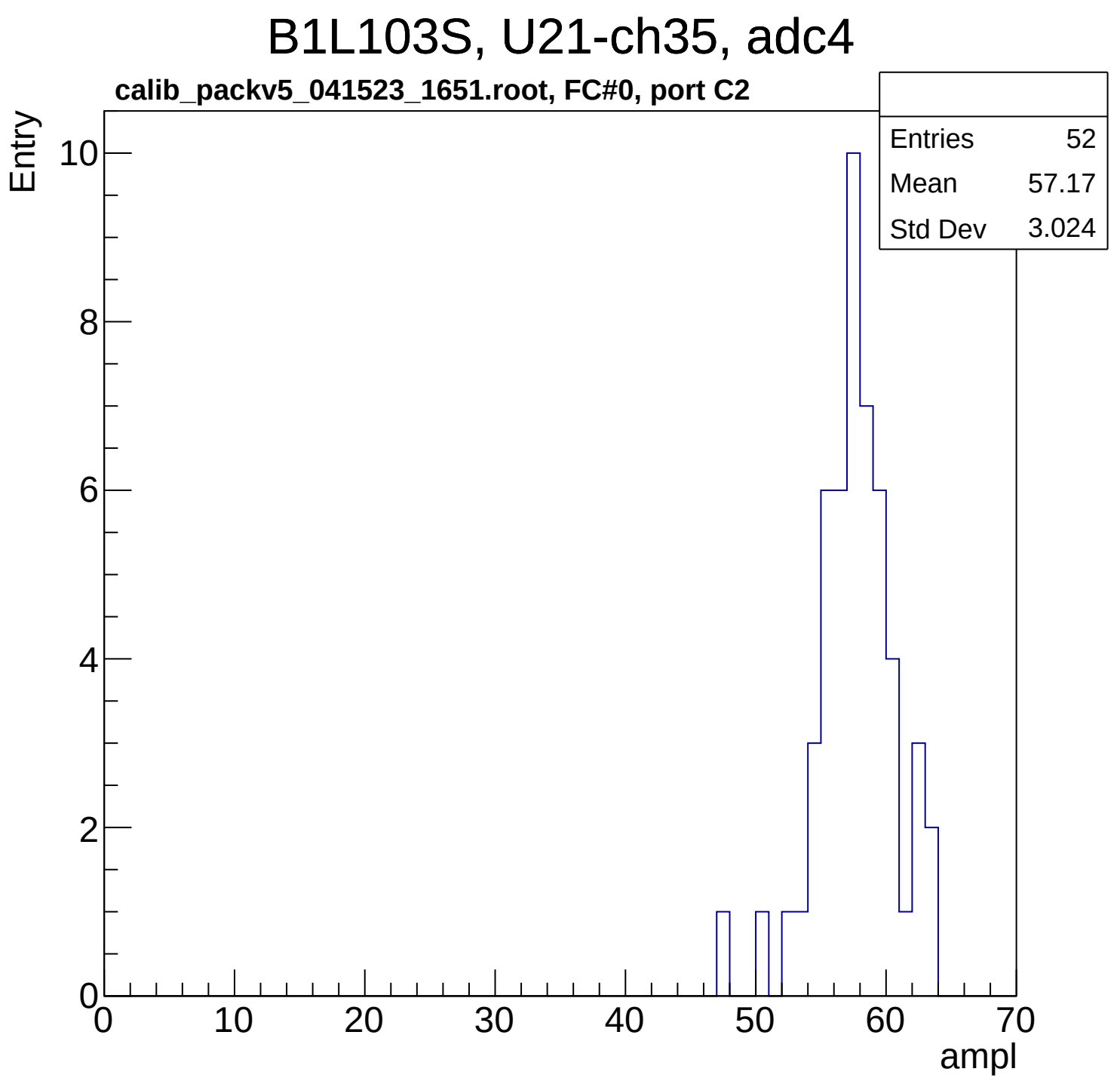
B1L103S, U21-ch35, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 57.17
Std Dev 3.024
Entry
0
2
4
6
8
10
0
10
20
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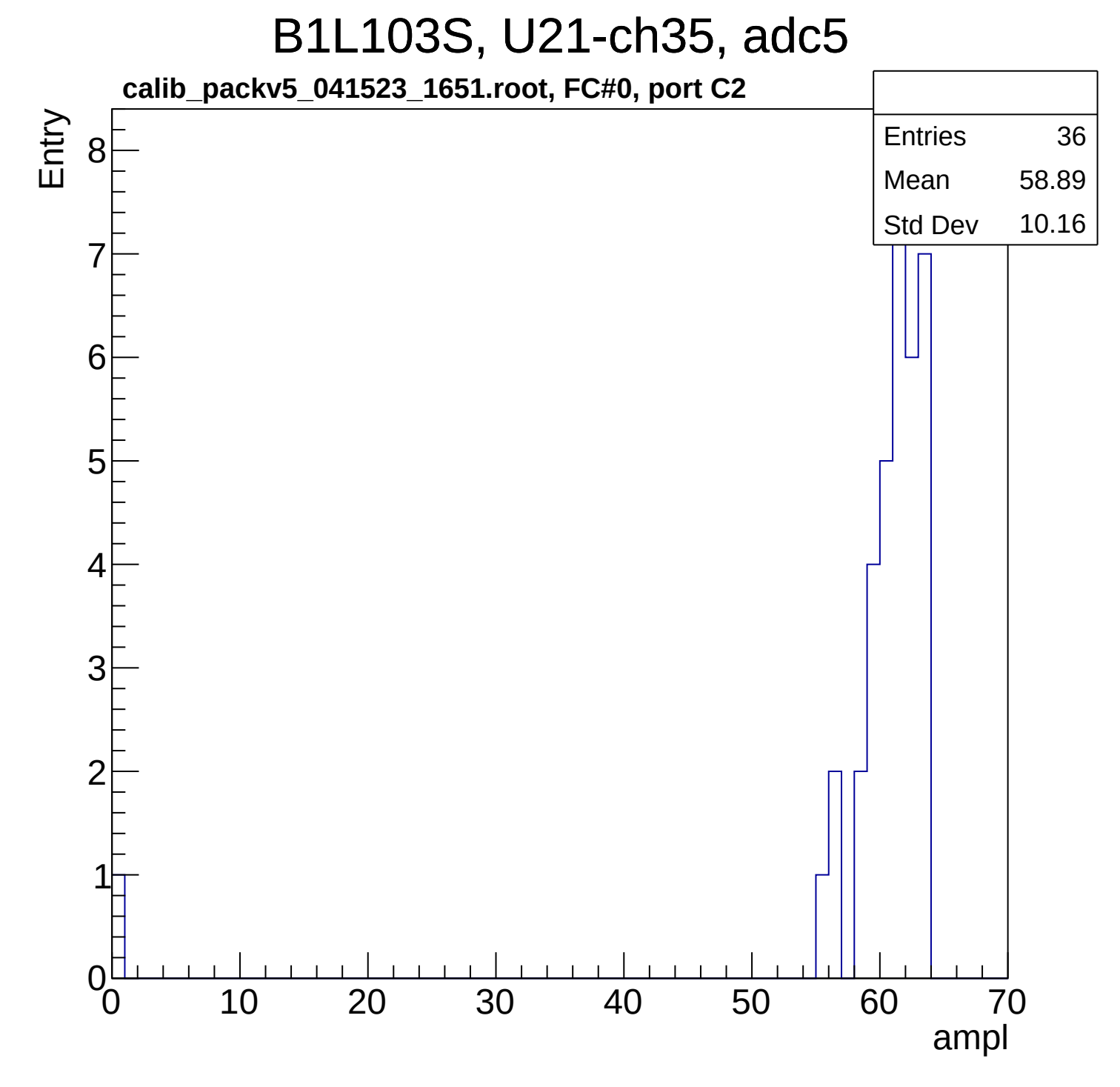
50
60
70
ampl


B1L103S, U21-ch35, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 58.89
Std Dev 10.16
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
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40
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60
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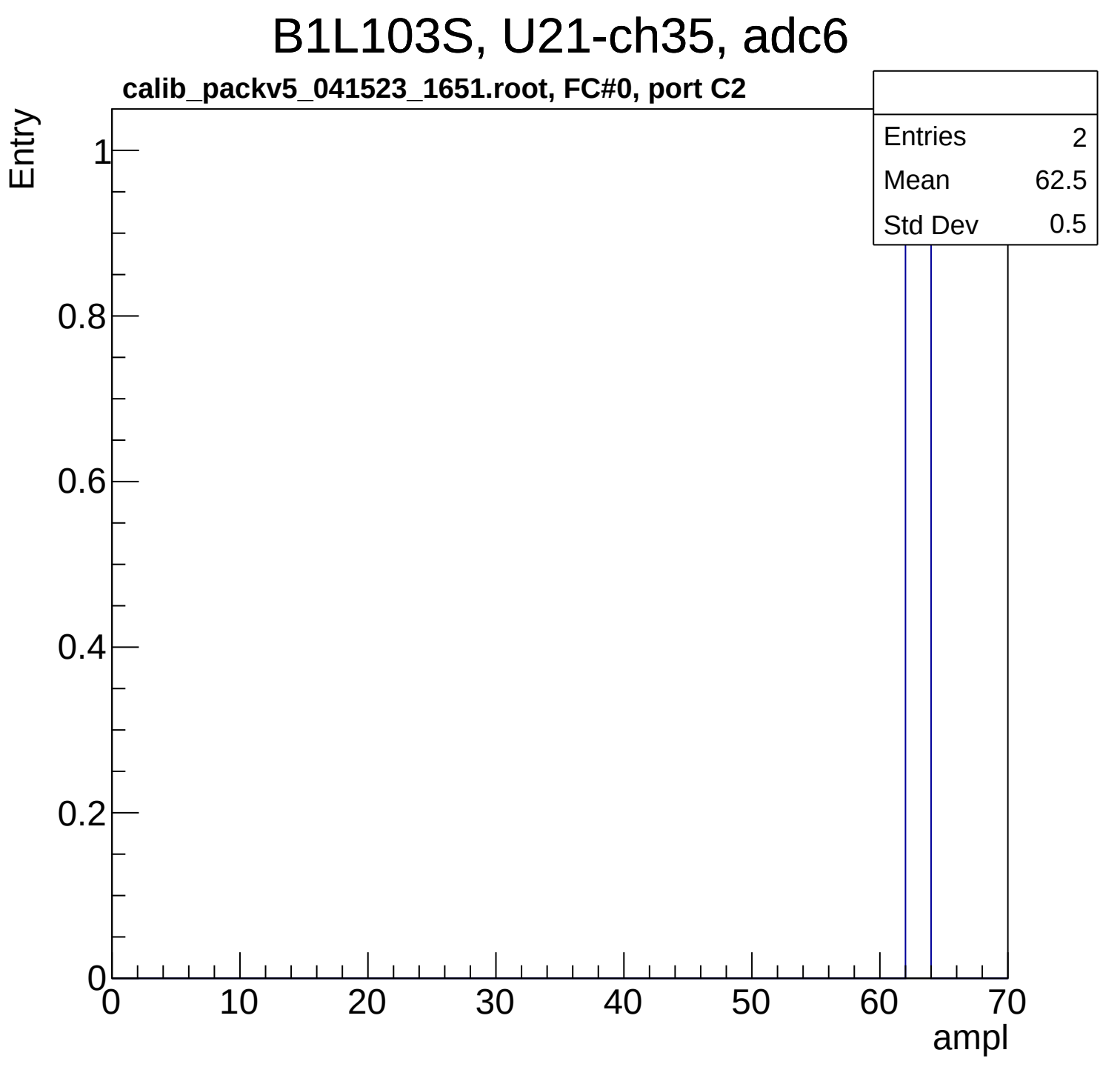
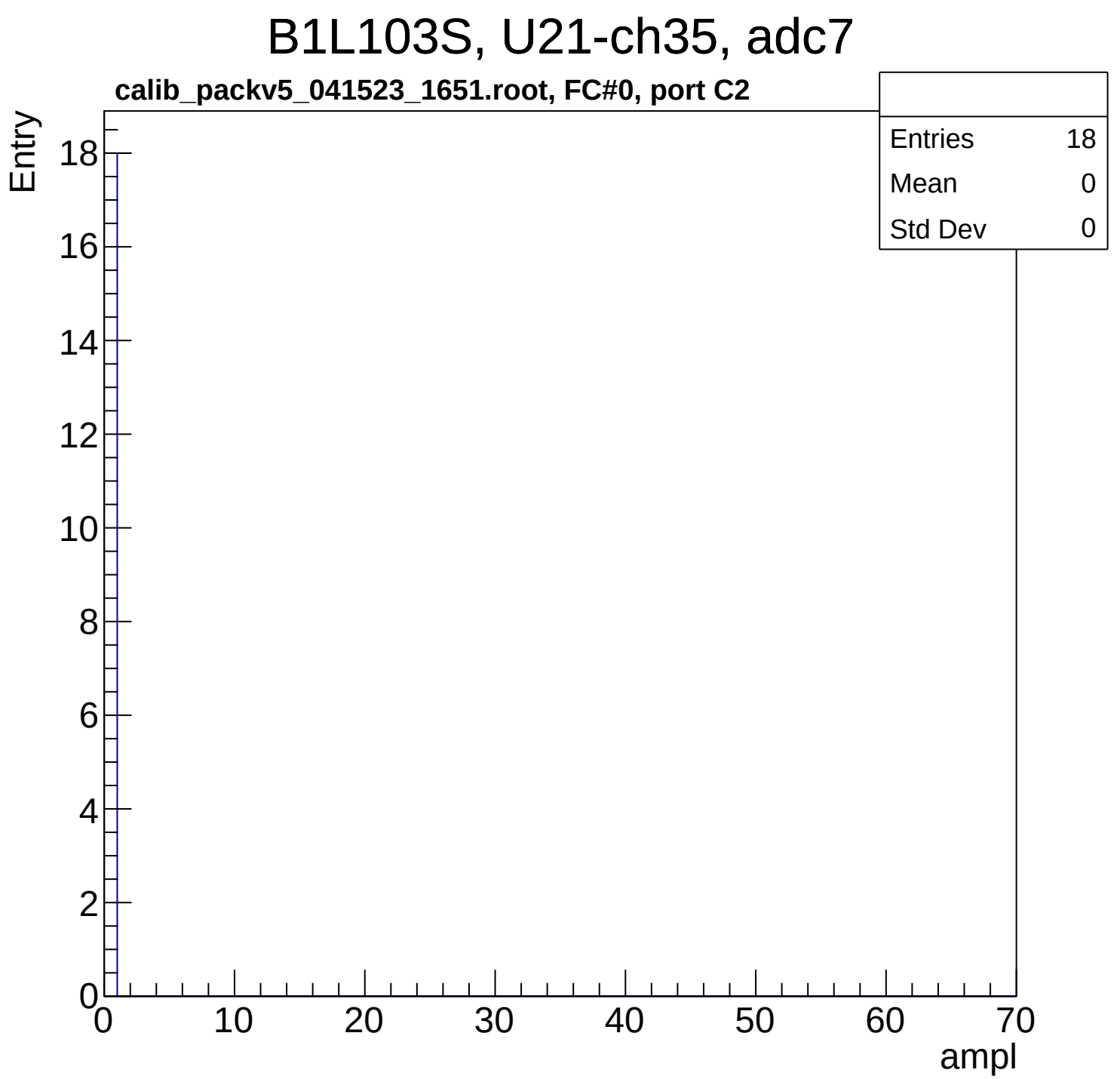
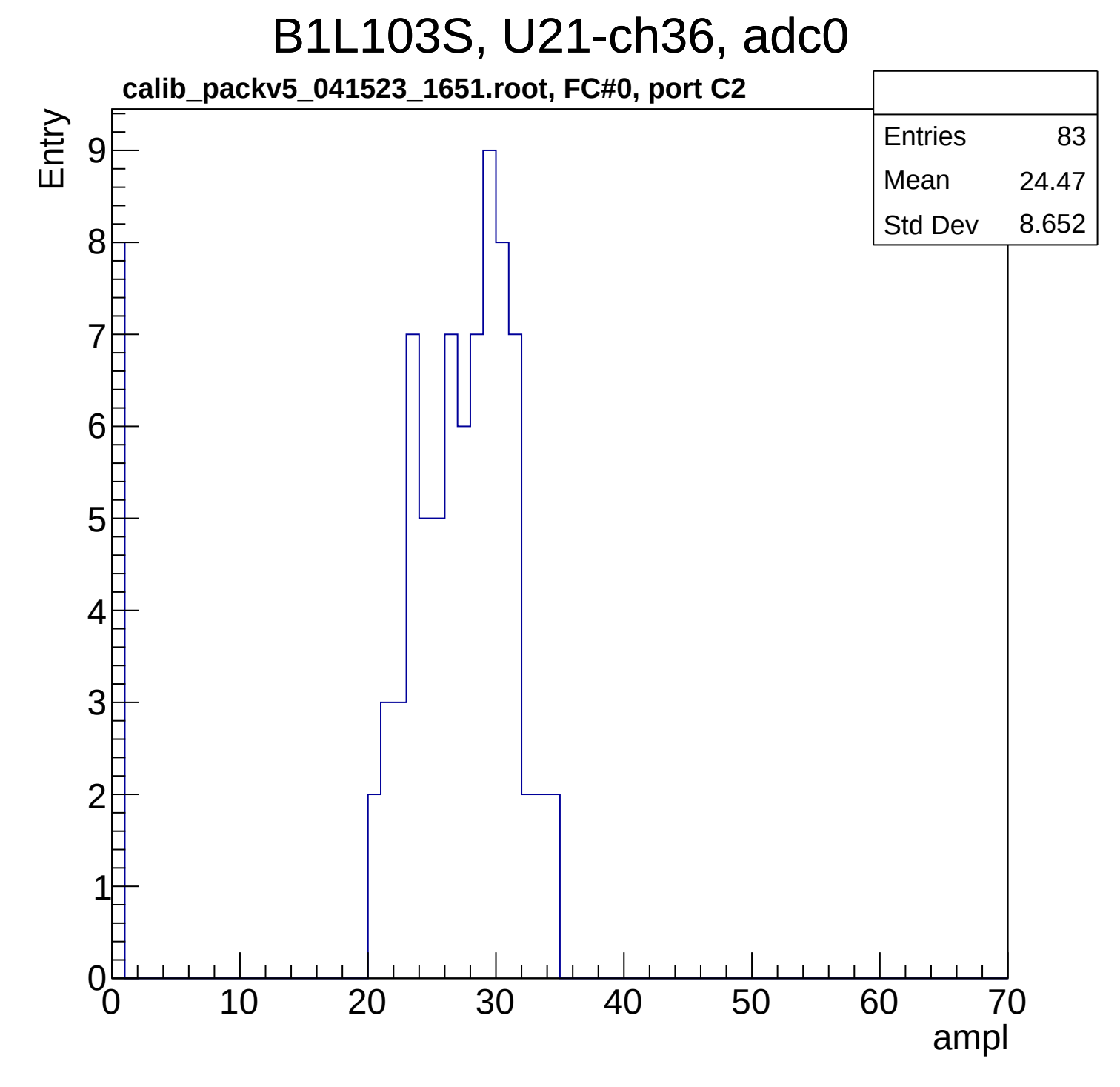

B1L103S, U21-ch35, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch35, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch36, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 24.47
Std Dev 8.652
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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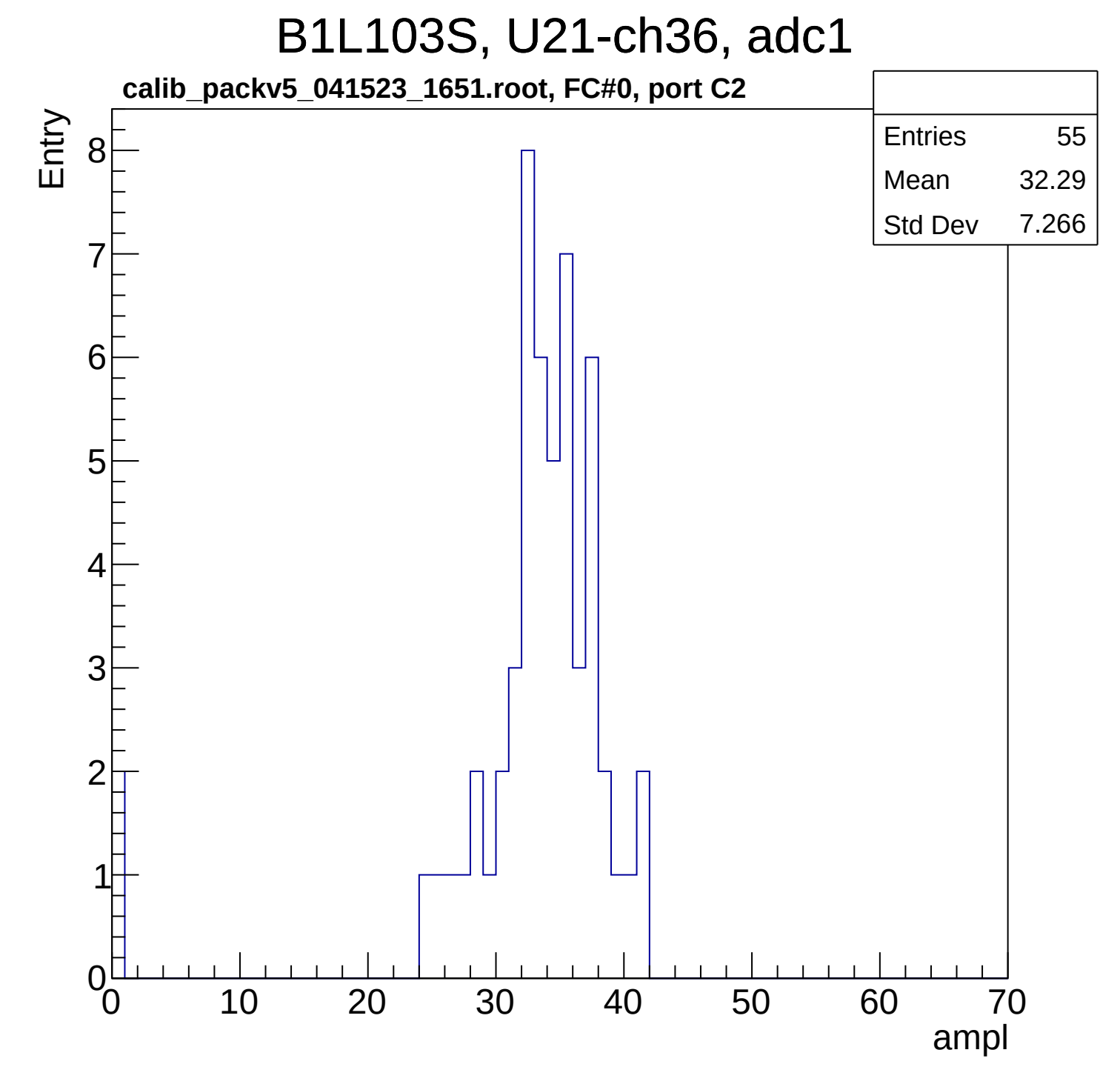
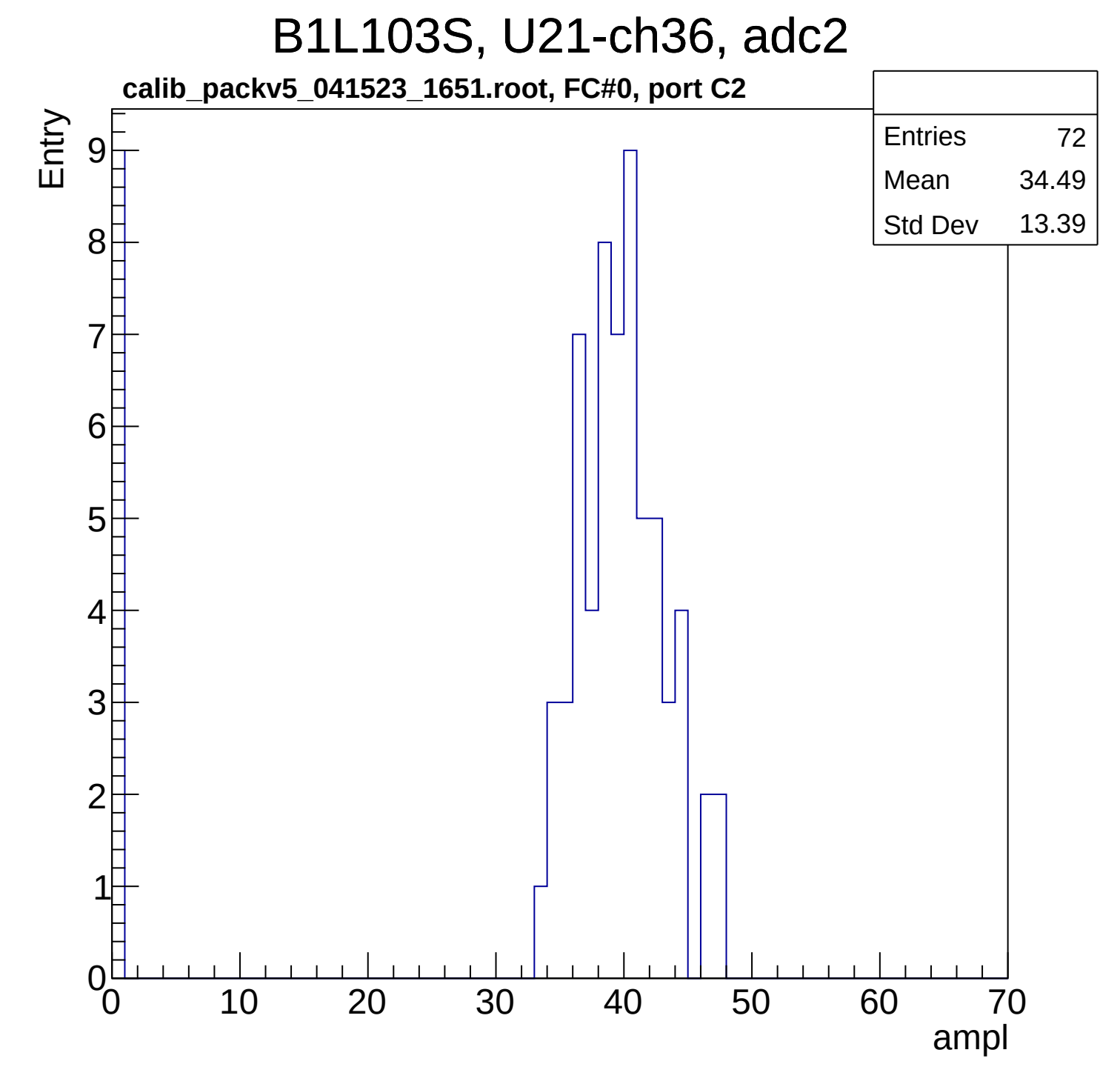
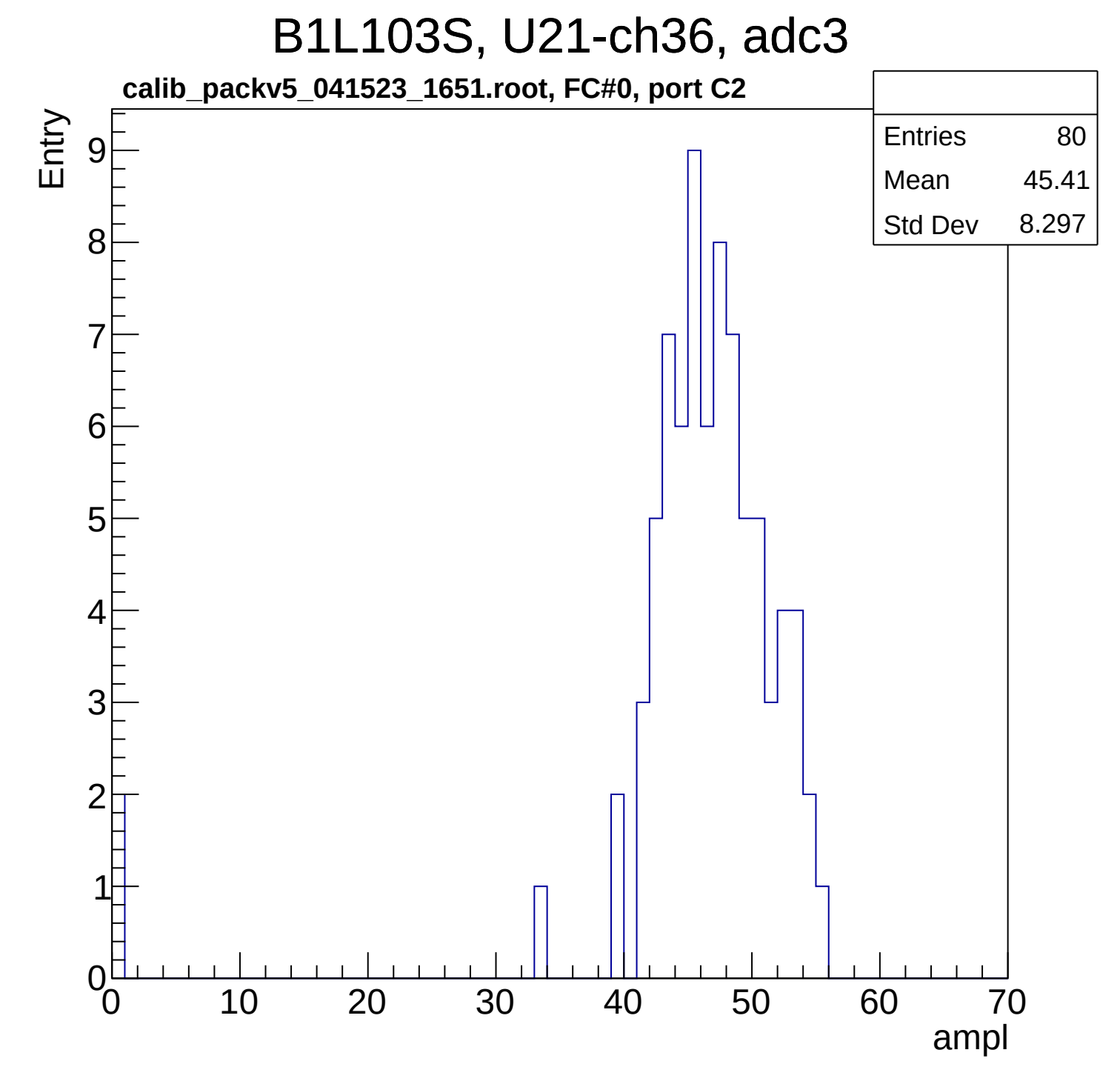
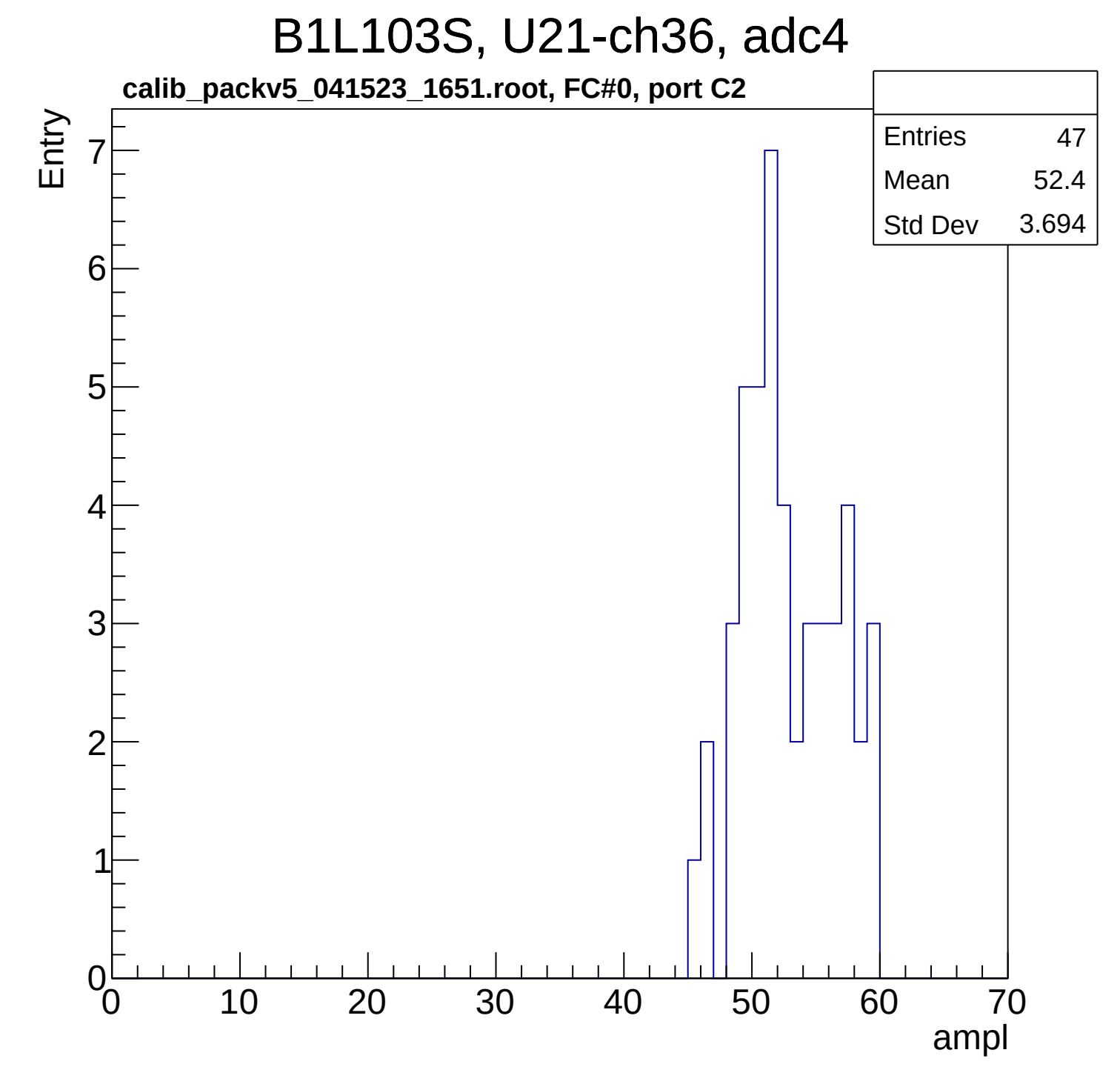
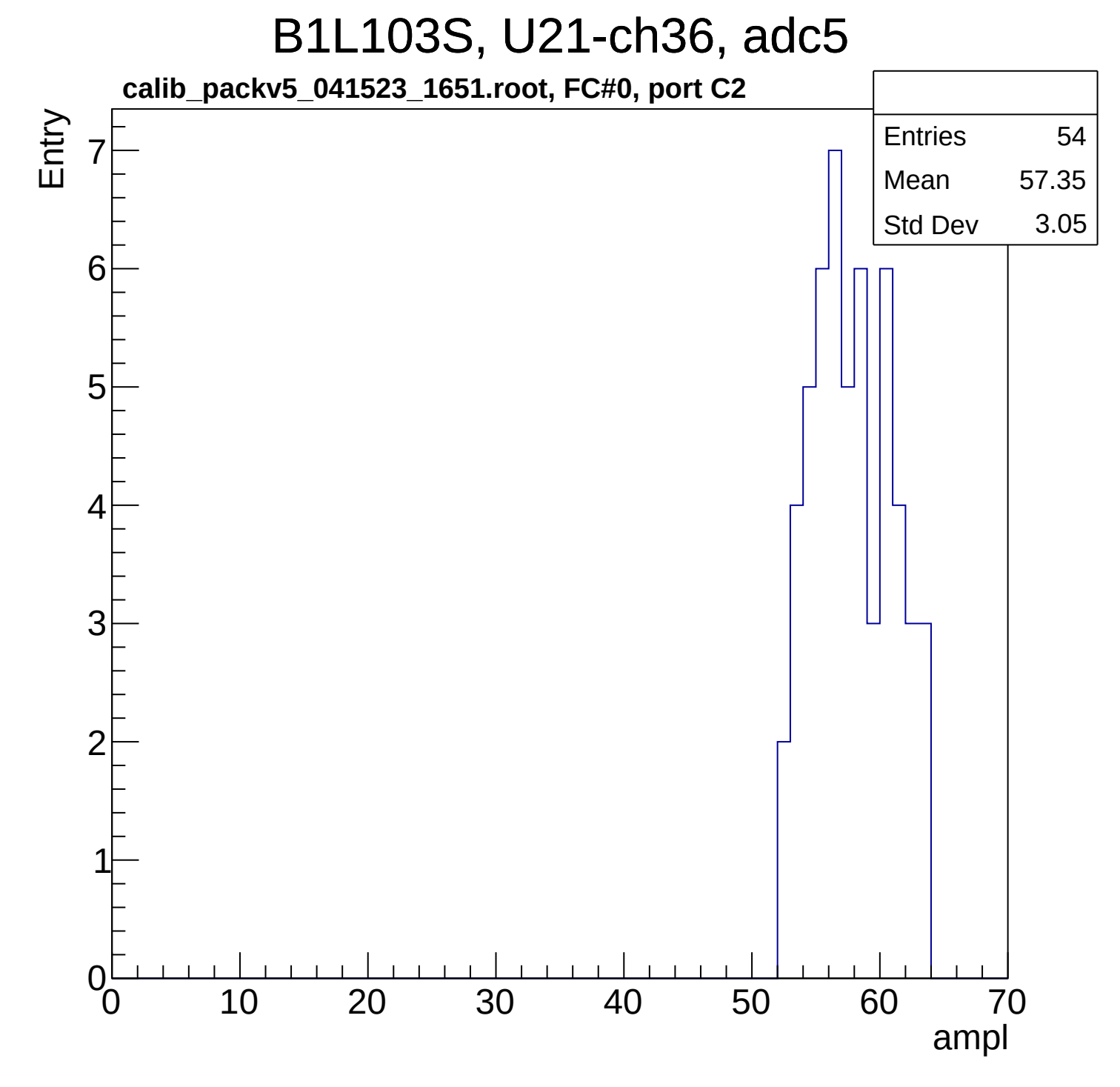
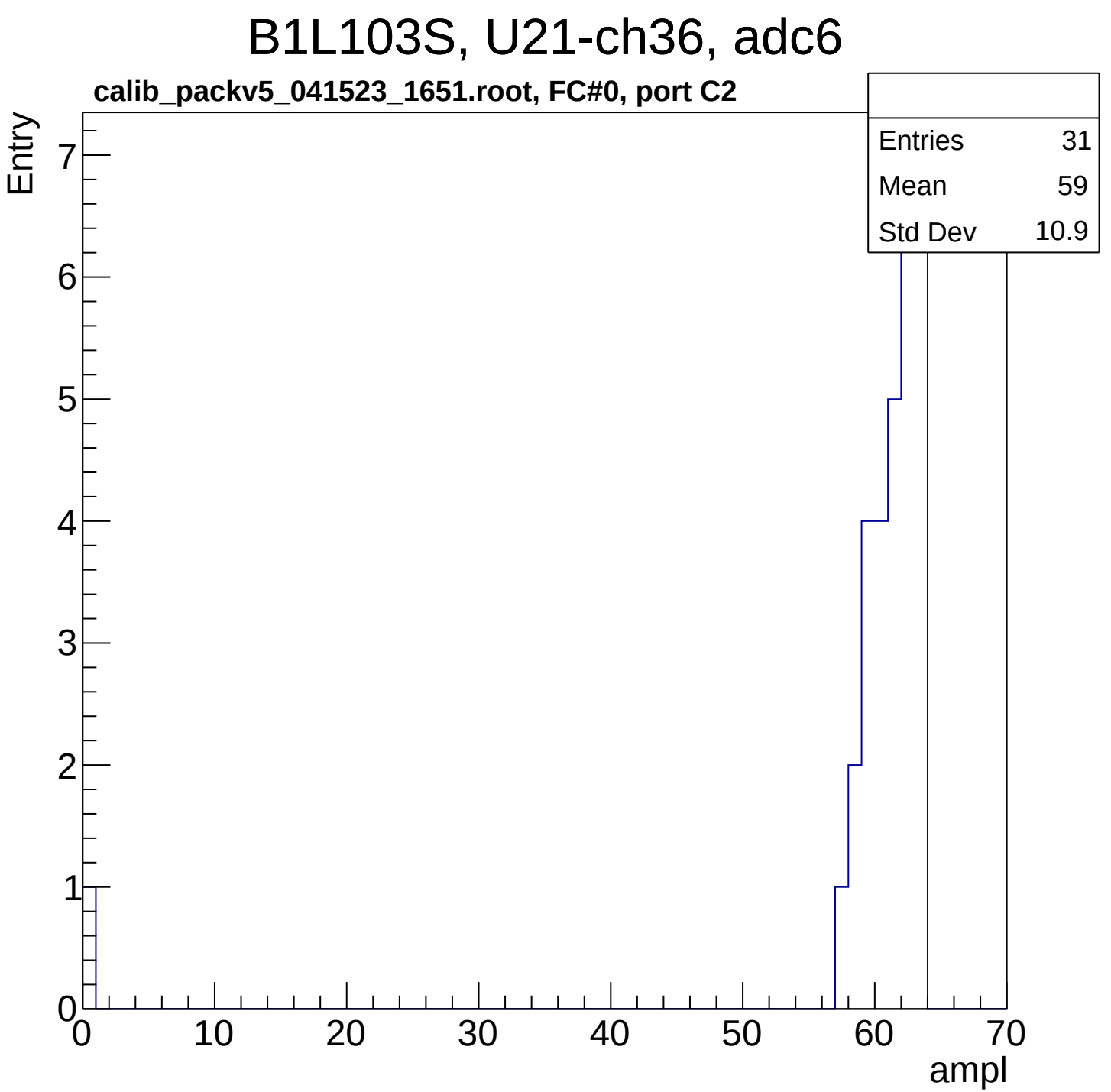

B1L103S, U21-ch36, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 32.29
Std Dev 7.266
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

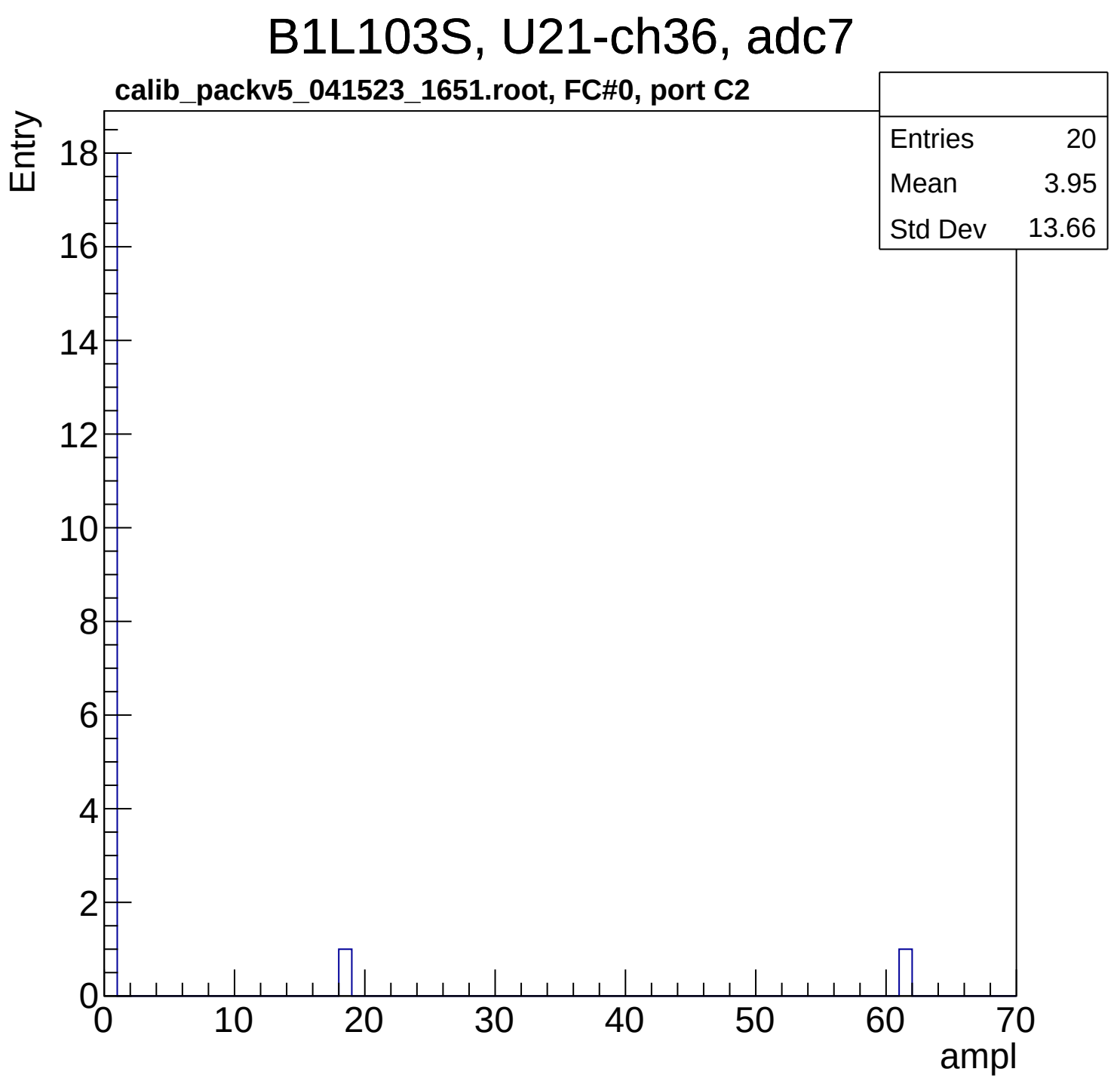

B1L103S, U21-ch36, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 34.49
Std Dev 13.39
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

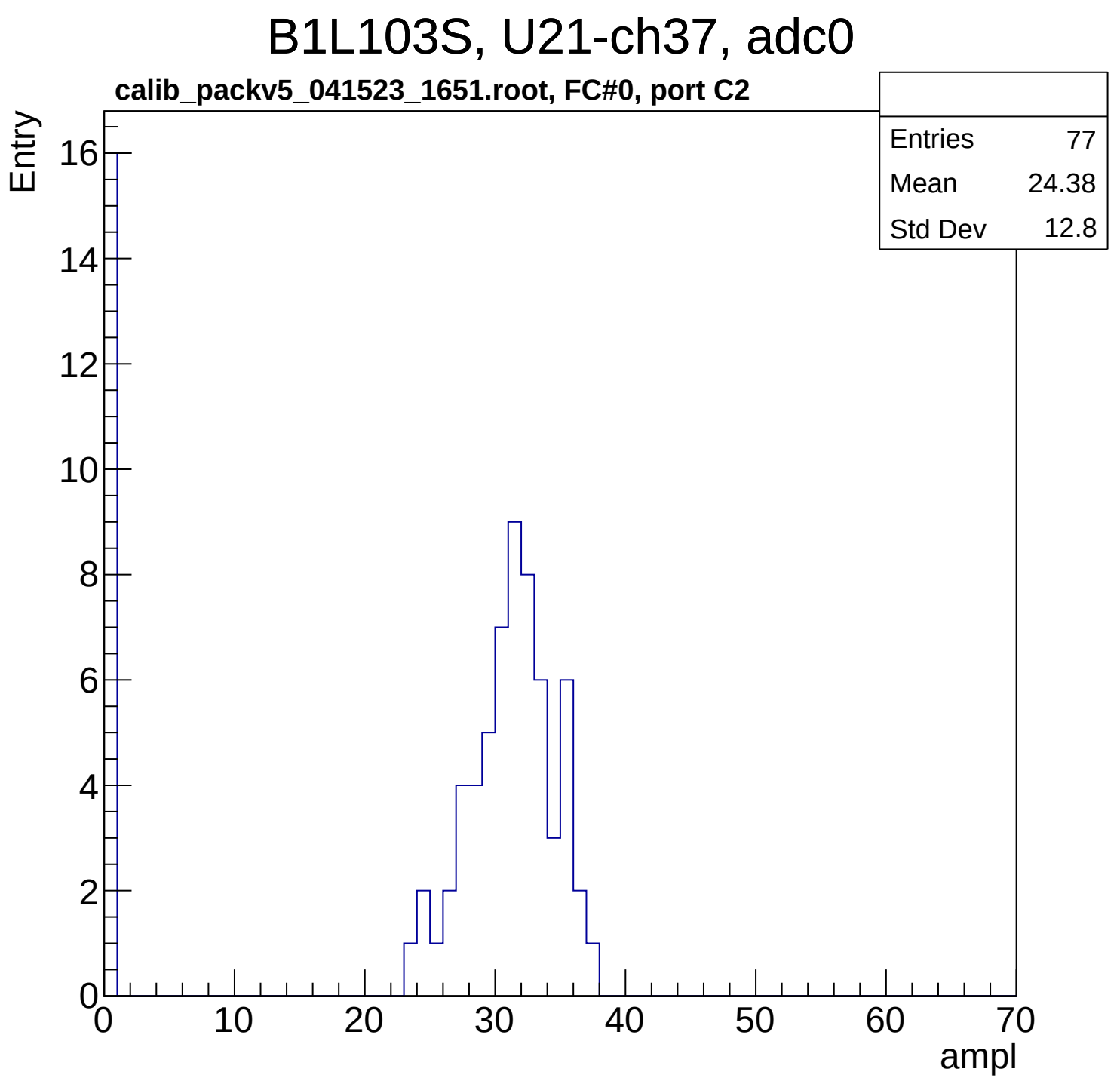

B1L103S, U21-ch36, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 45.41
Std Dev 8.297
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch36, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 52.4
Std Dev 3.694
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U21-ch36, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 57.35
Std Dev 3.05
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U21-ch36, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 59
Std Dev 10.9
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch36, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.95
Std Dev 13.66
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch37, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 24.38
Std Dev 12.8
Entry
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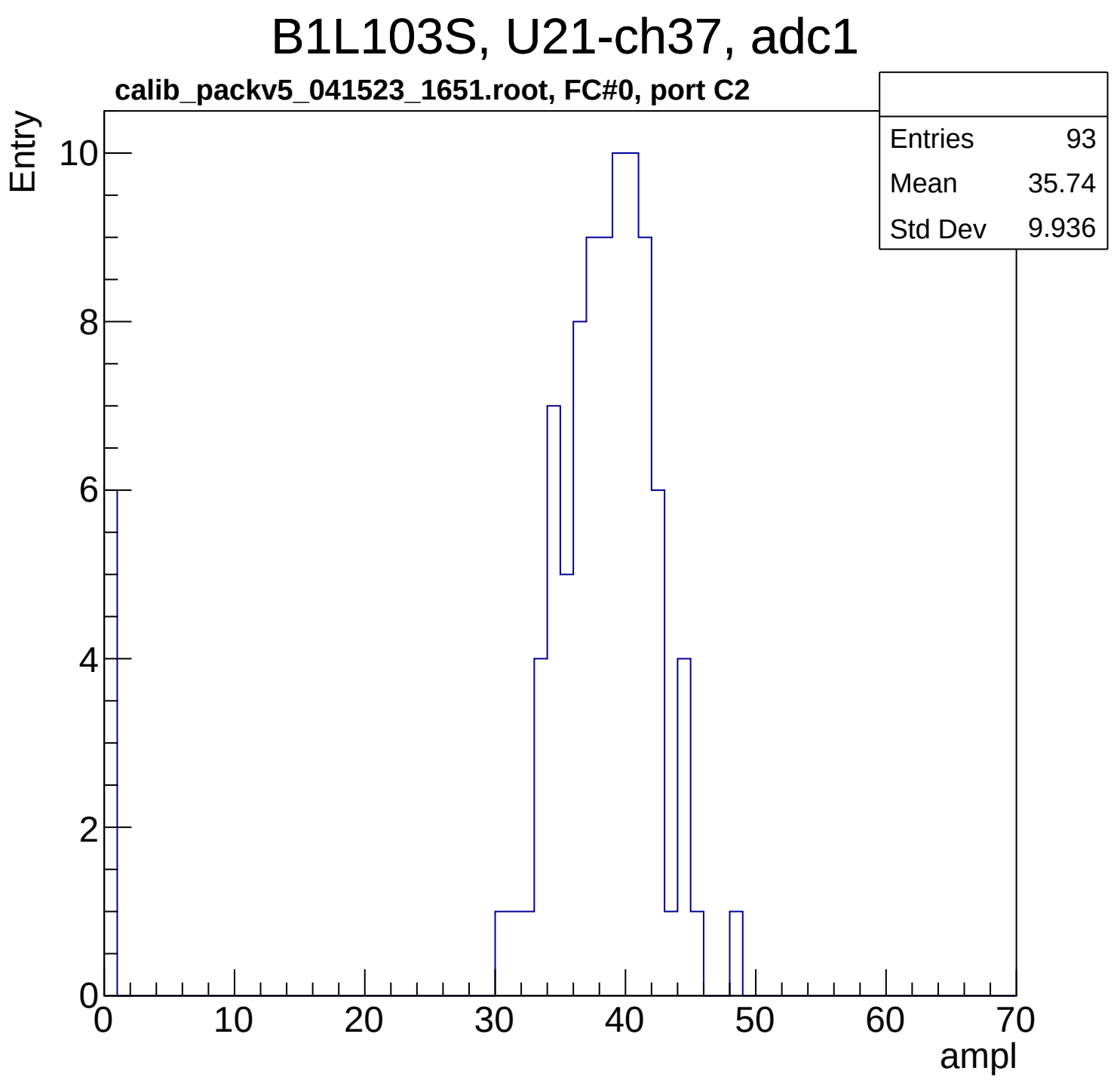
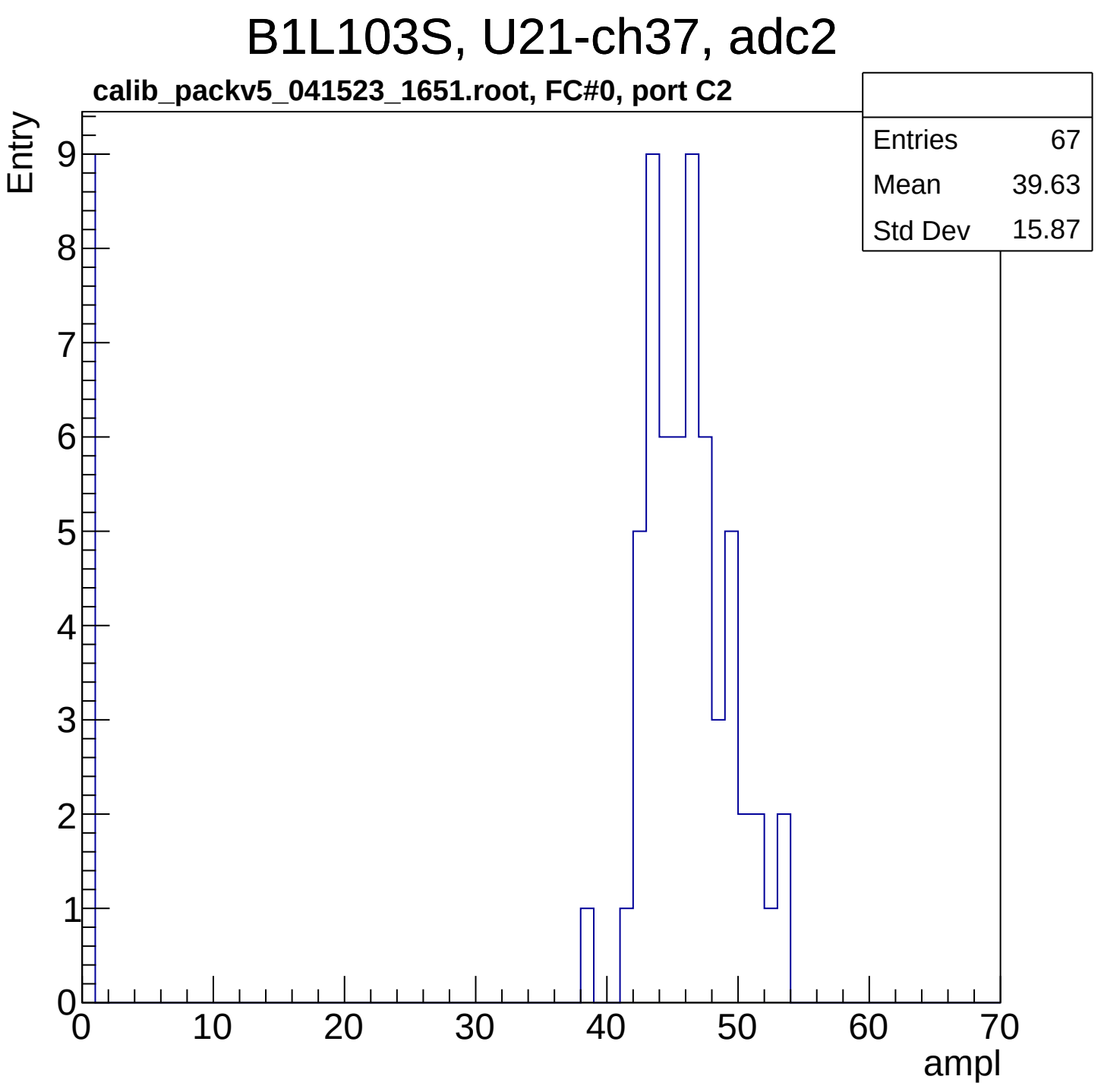
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch37, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 35.74
Std Dev 9.936
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U21-ch37, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 39.63
Std Dev 15.87
Entry
ampl
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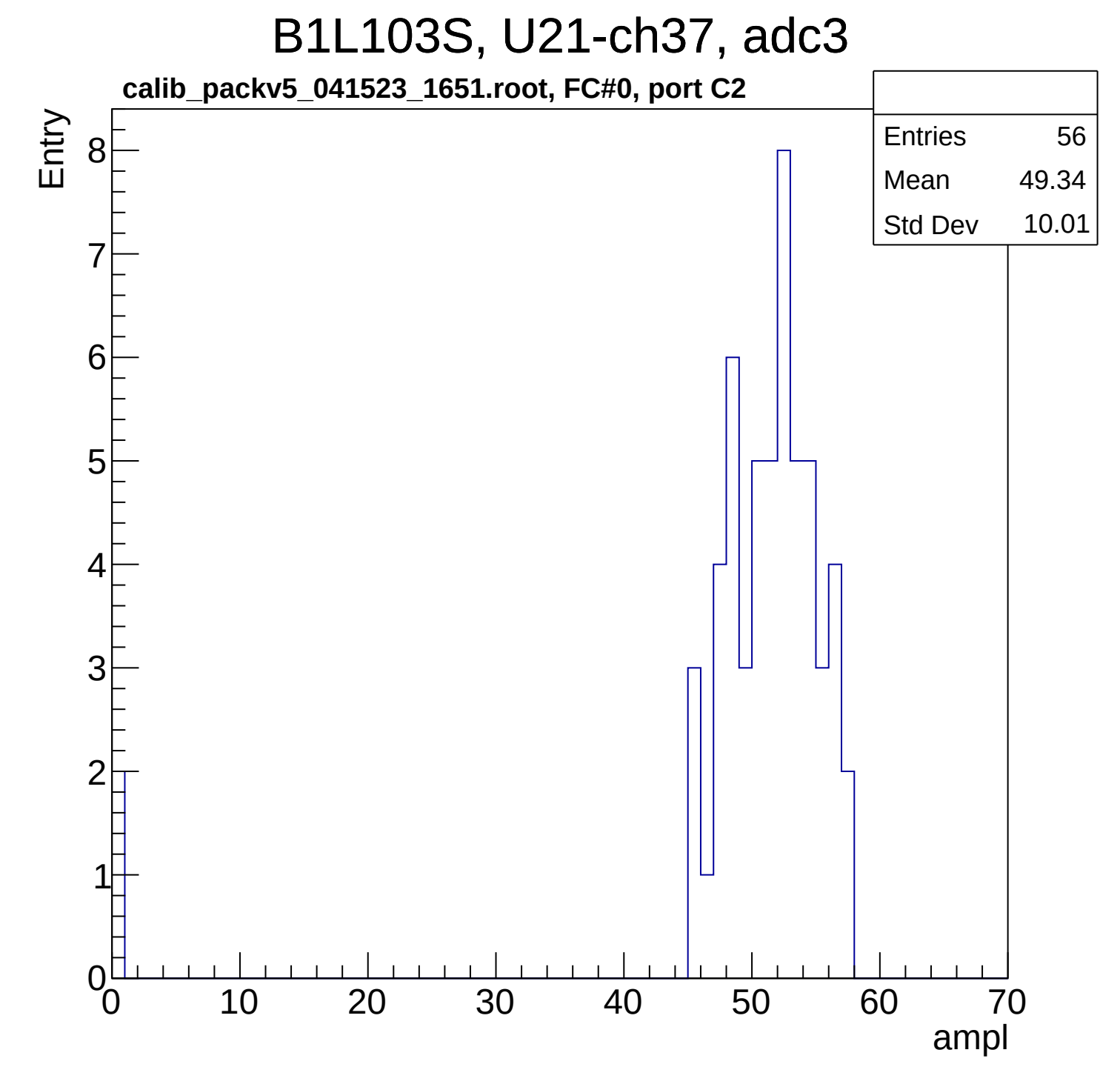
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch37, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 49.34
Std Dev 10.01
Entry
ampl
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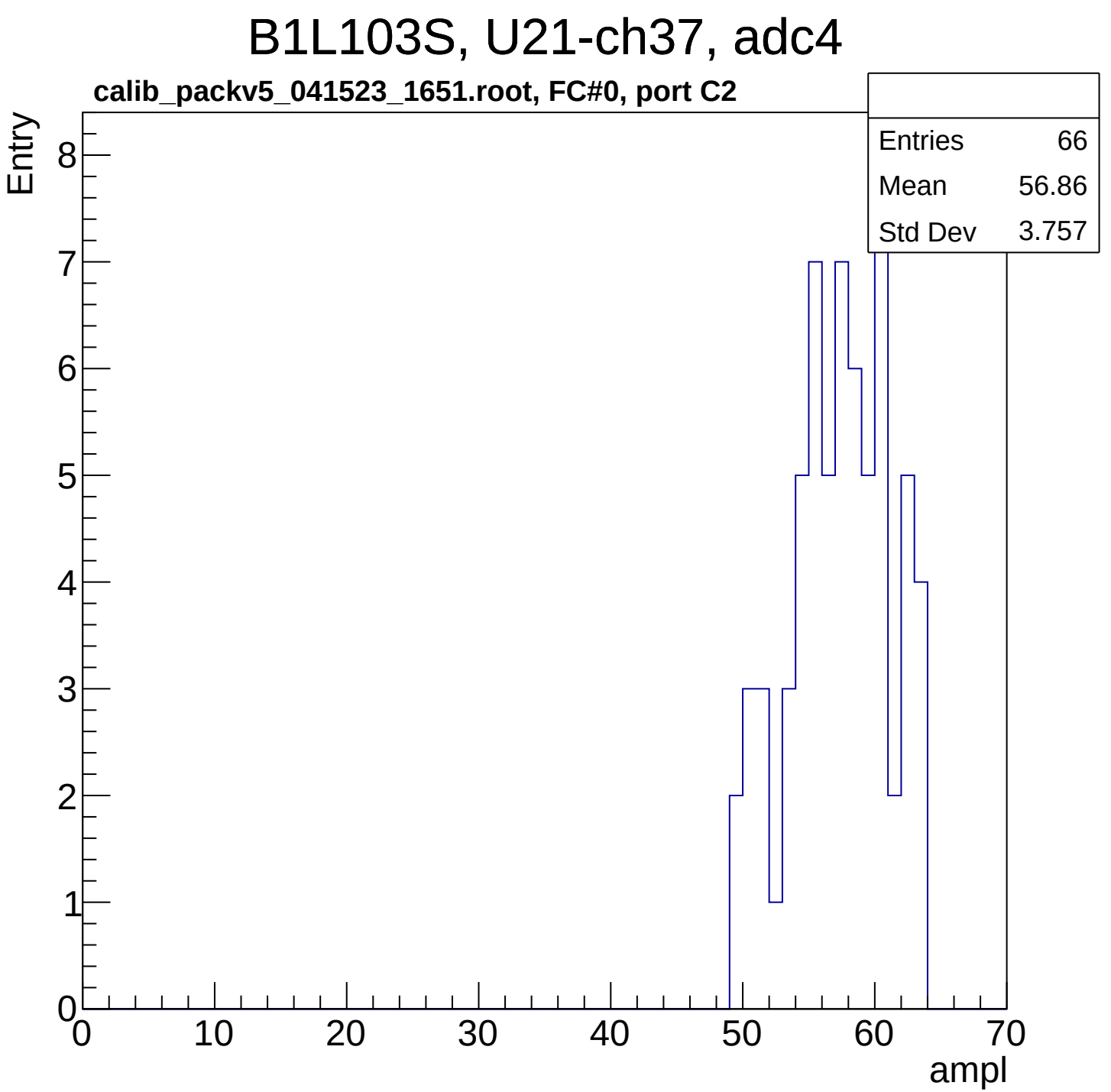
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch37, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 56.86
Std Dev 3.757
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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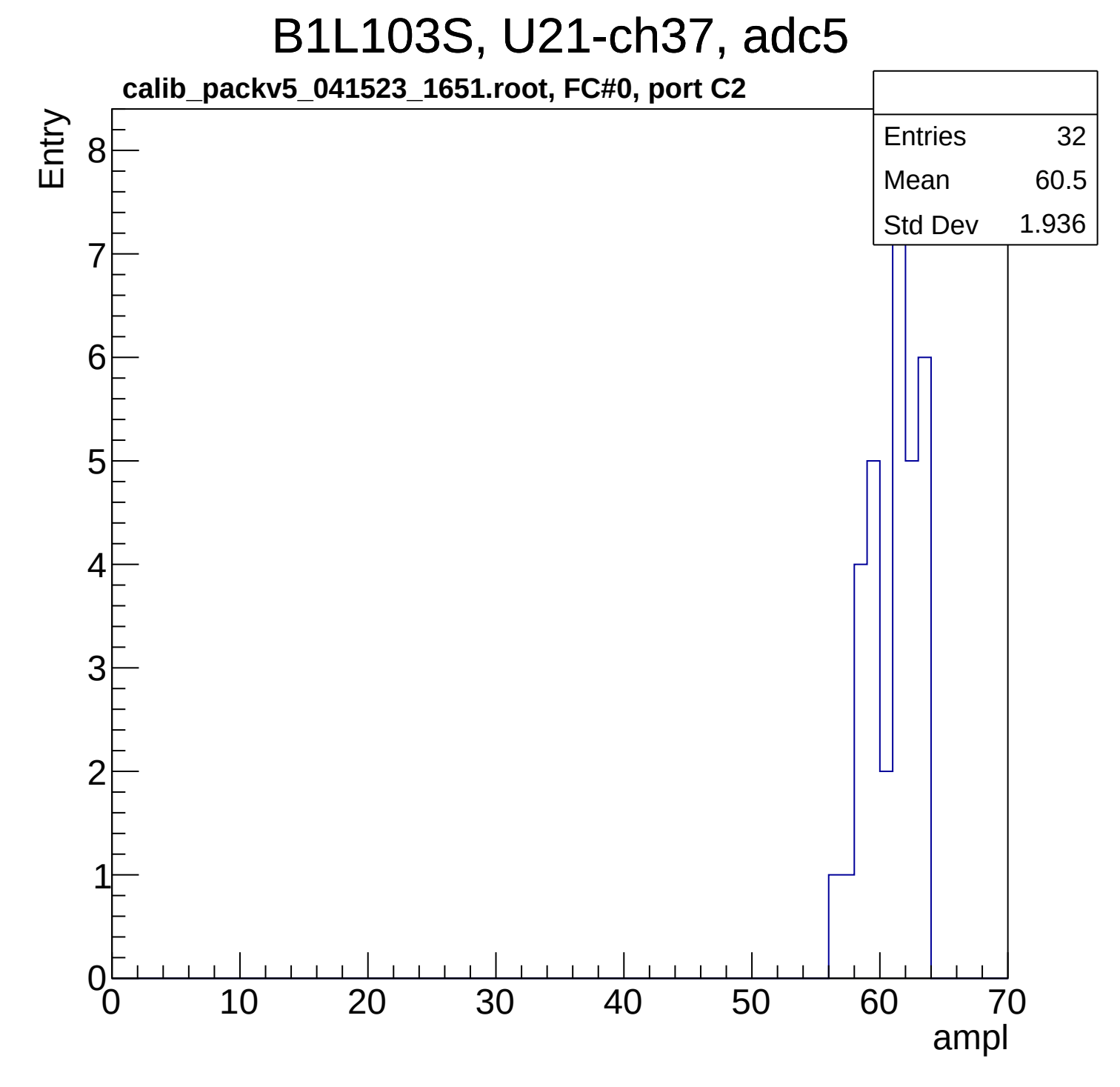
40
50
60
70


B1L103S, U21-ch37, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 60.5
Std Dev 1.936
Entry
ampl
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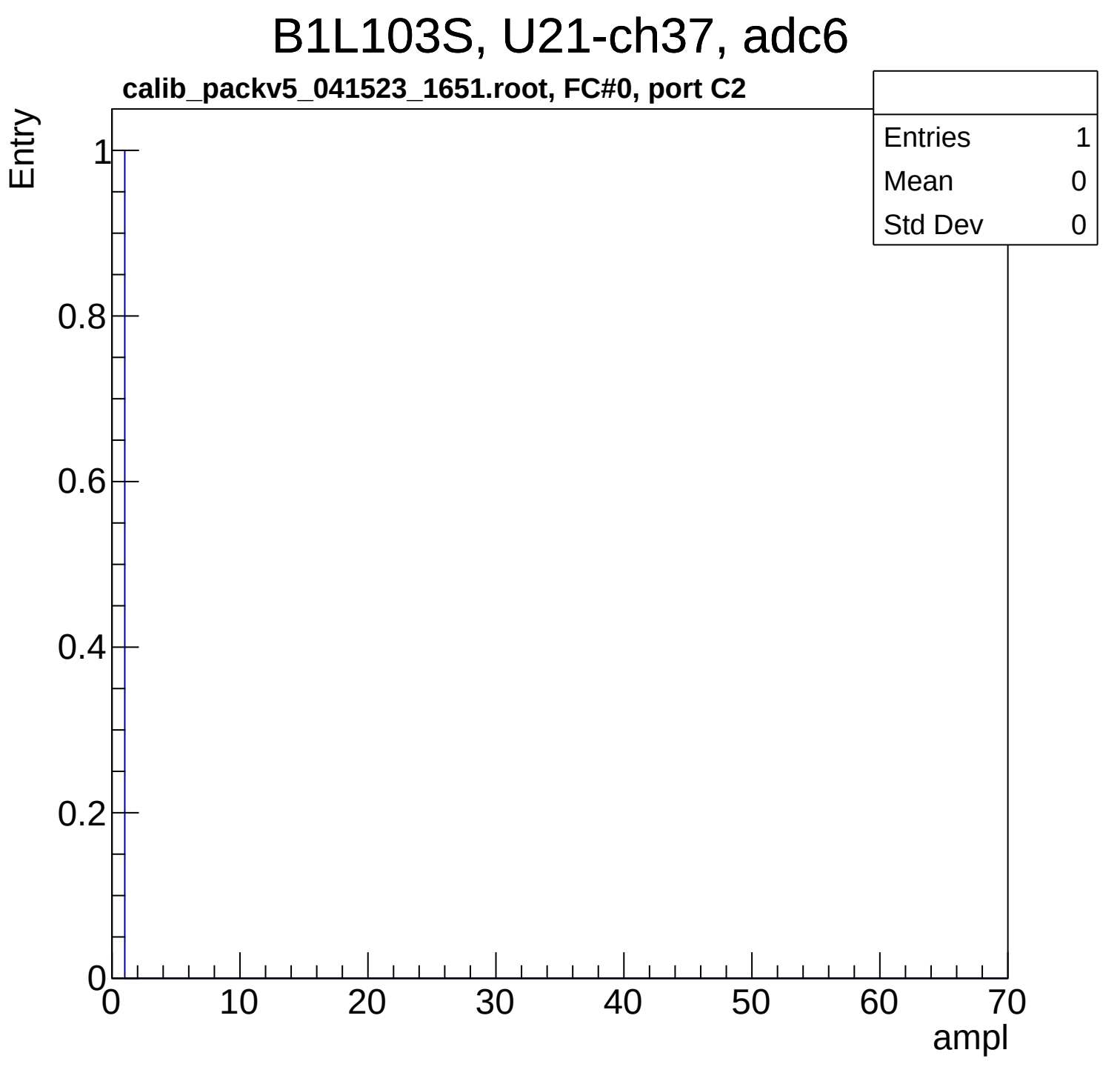
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch37, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 1
Mean 0
Std Dev 0
Entry
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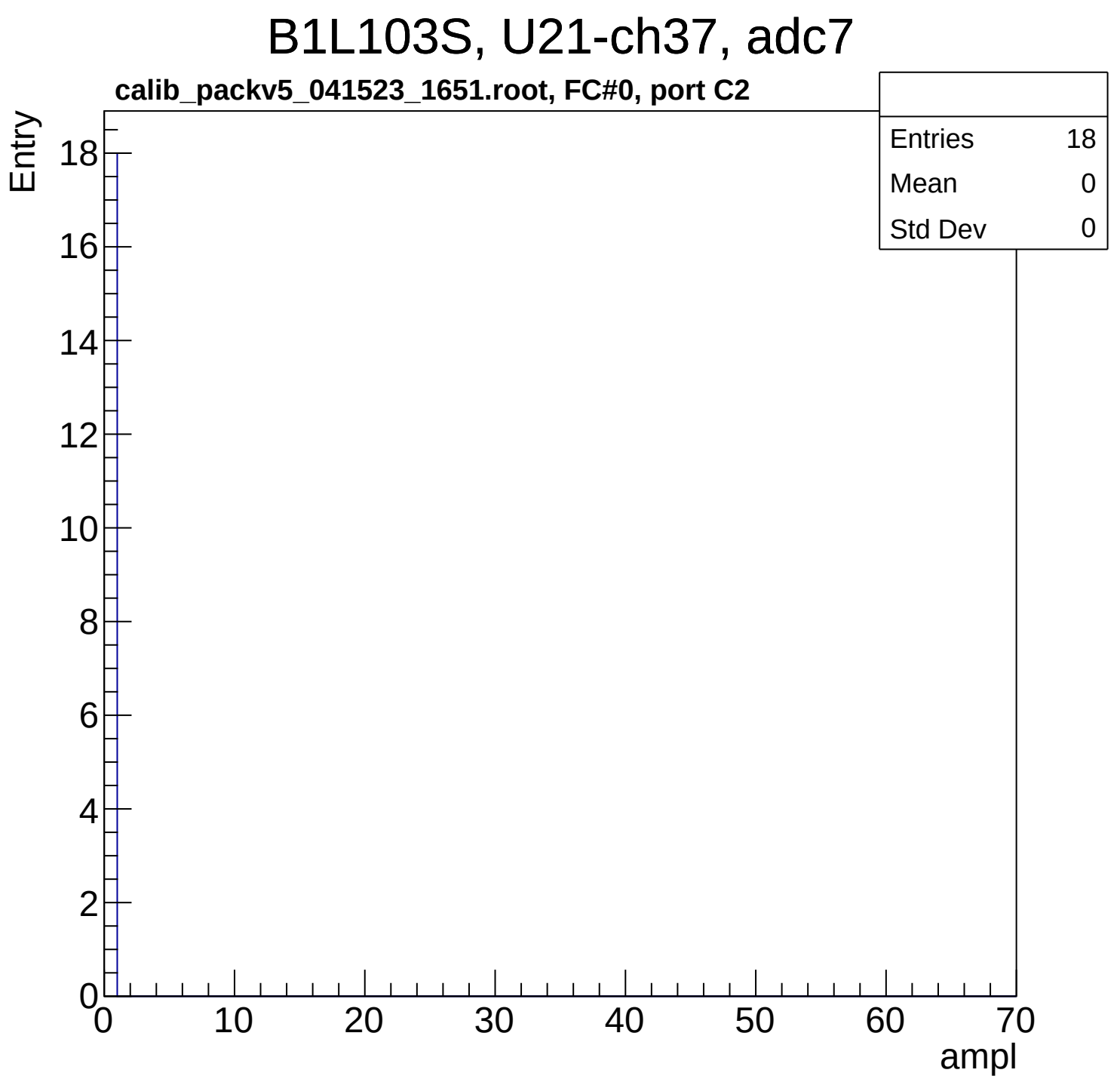
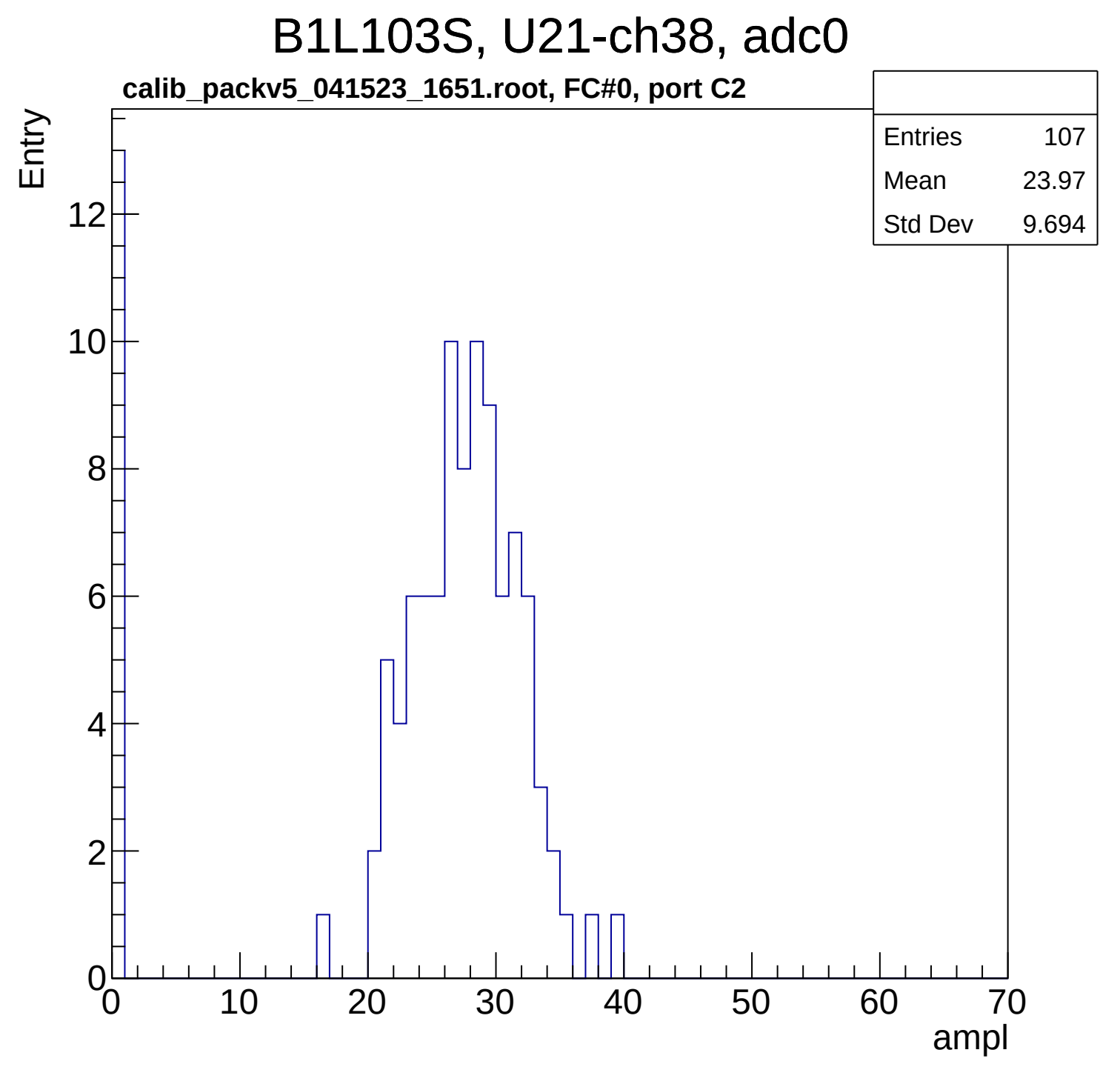
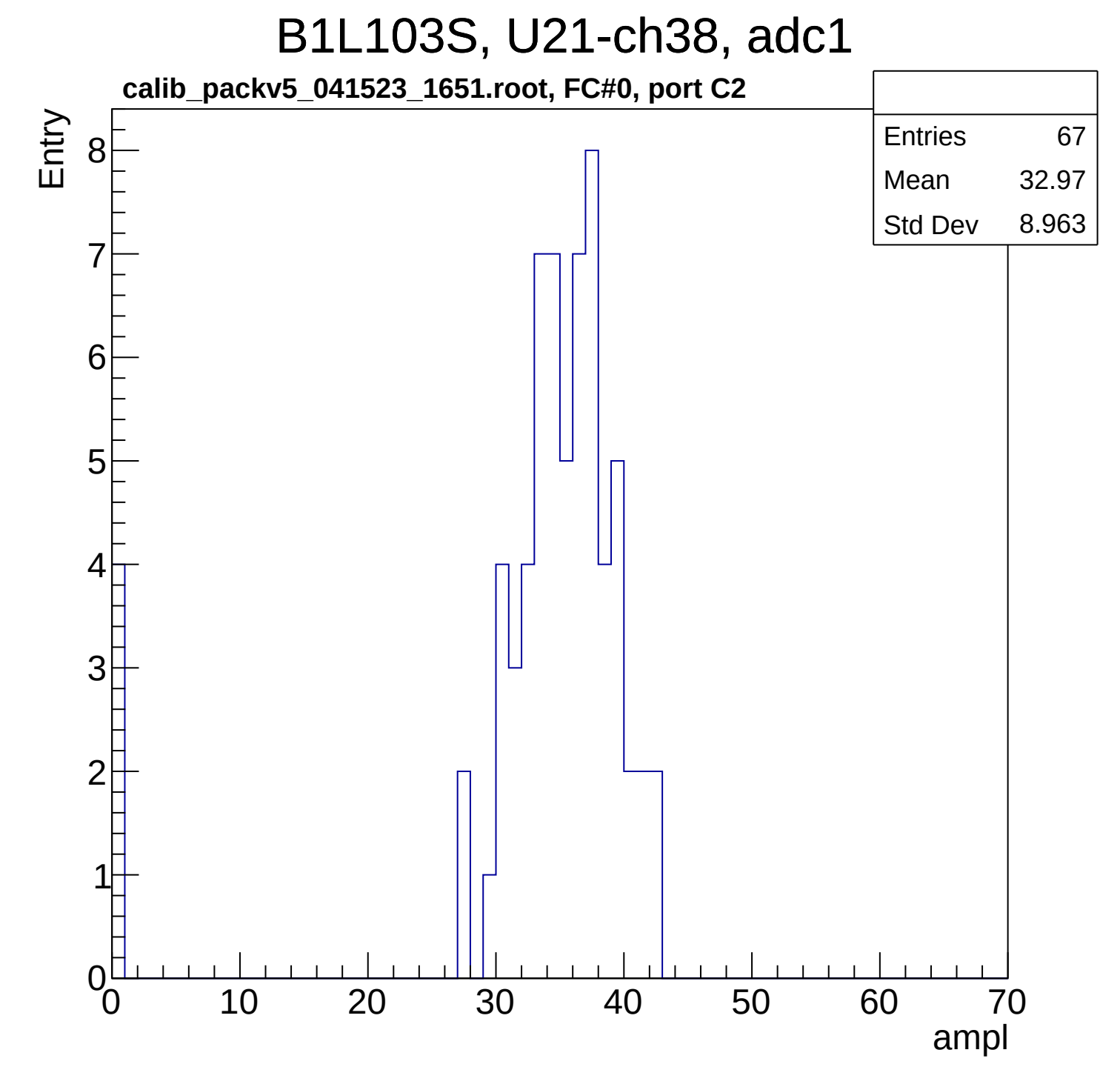
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch37, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch38, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 107
Mean 23.97
Std Dev 9.694
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch38, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 32.97
Std Dev 8.963
Entry
ampl
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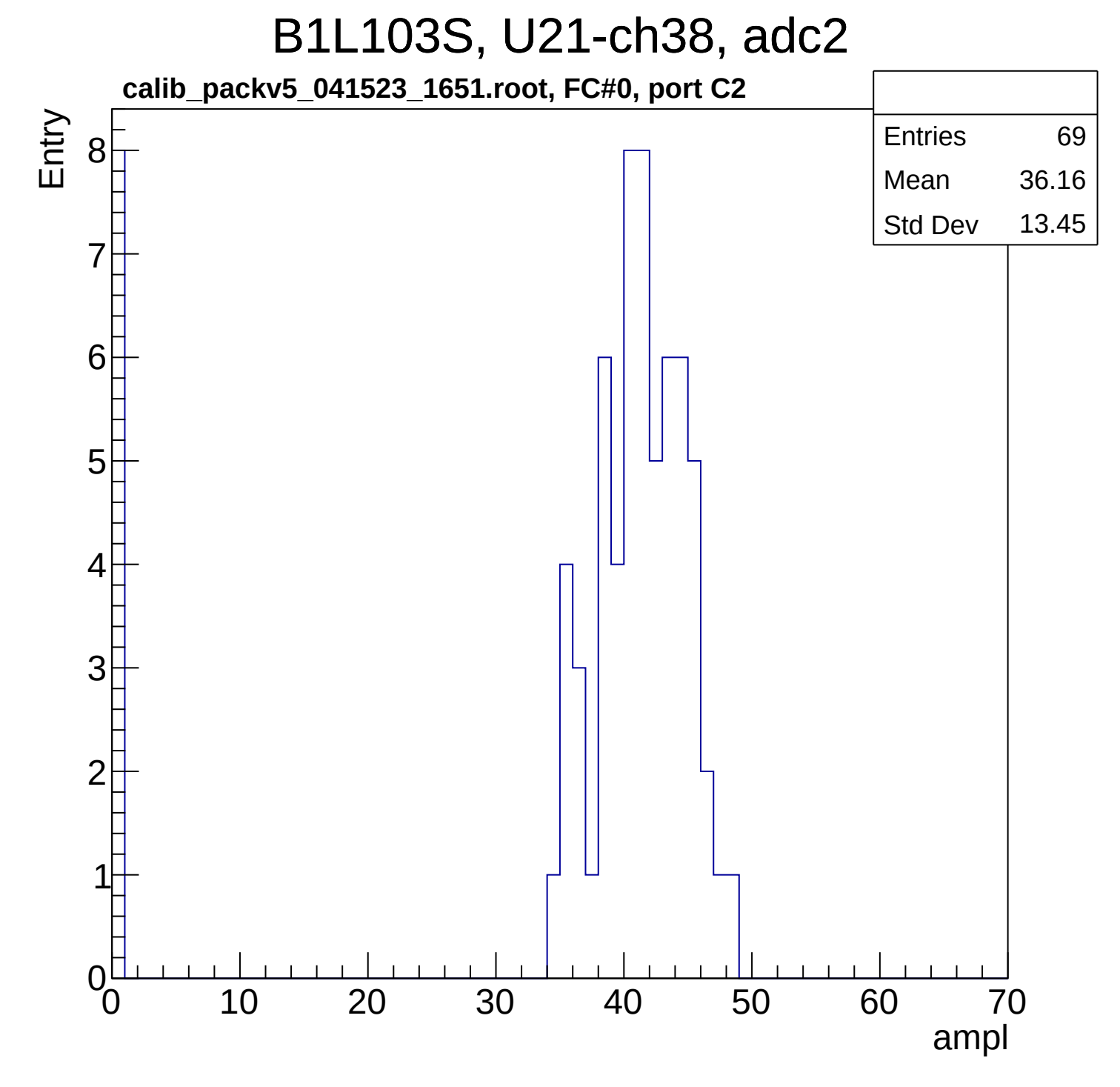
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch38, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 36.16
Std Dev 13.45
Entry
ampl
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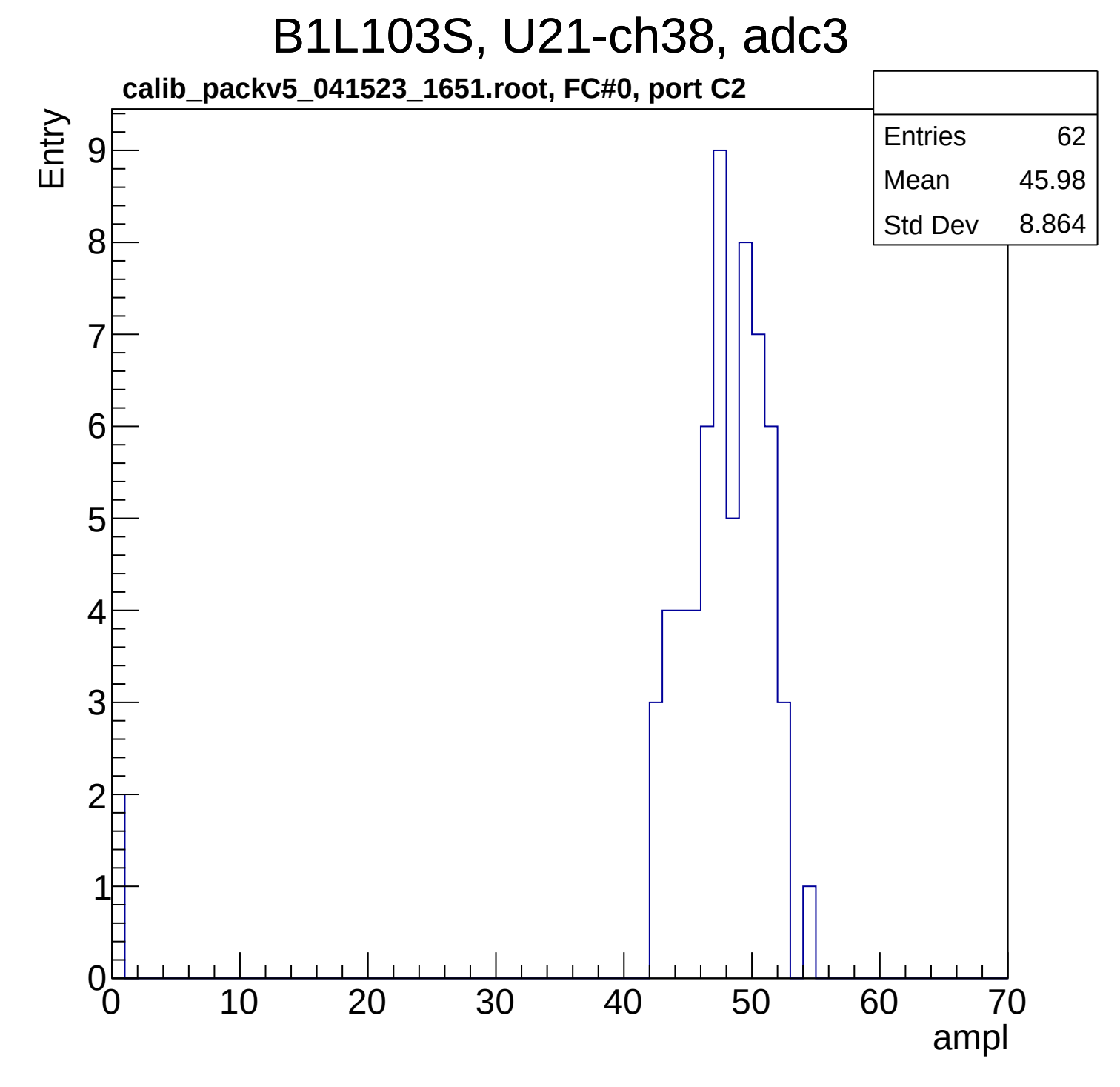
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch38, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 45.98
Std Dev 8.864
Entry
ampl
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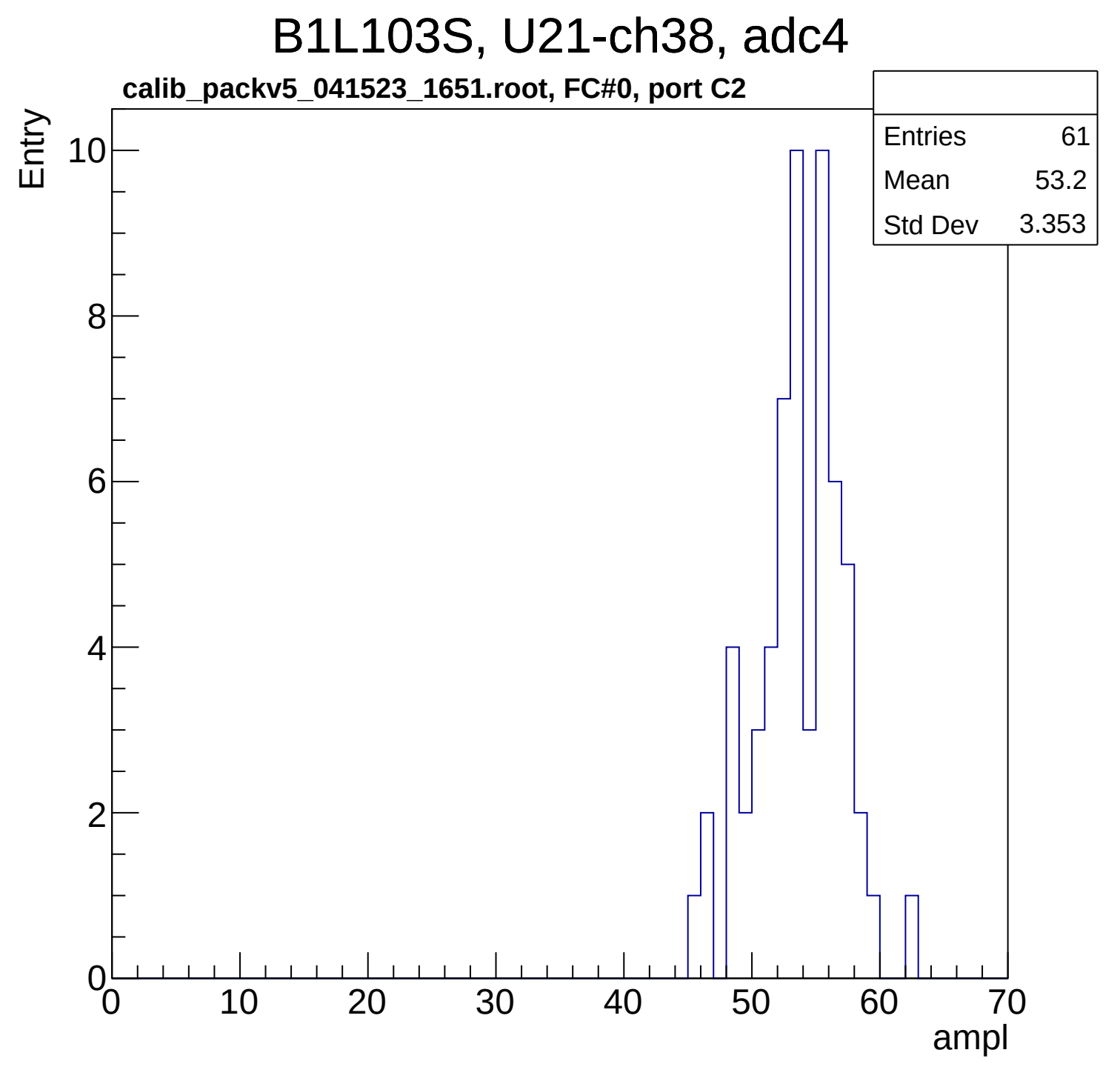
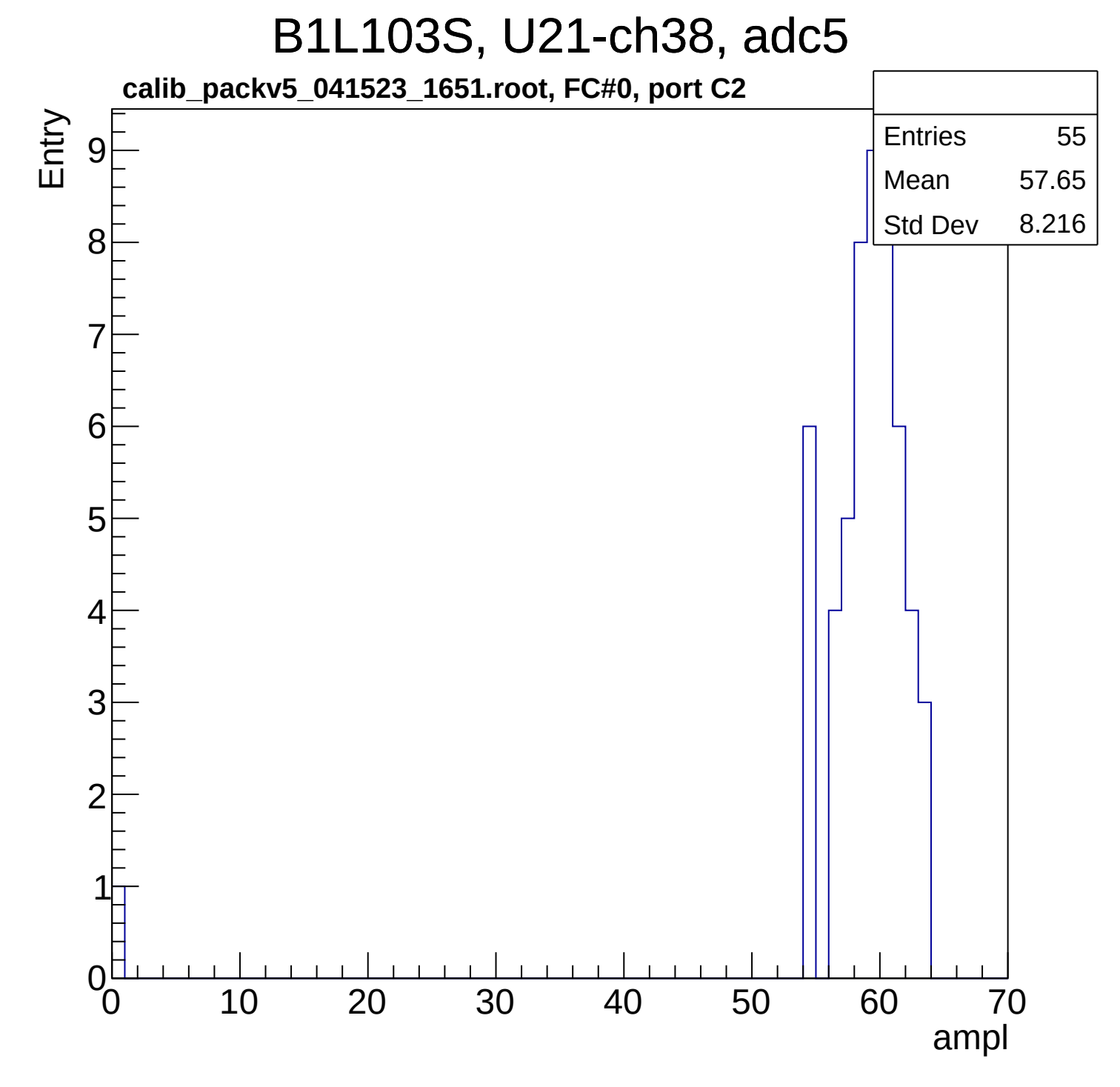
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch38, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 53.2
Std Dev 3.353
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U21-ch38, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 57.65
Std Dev 8.216
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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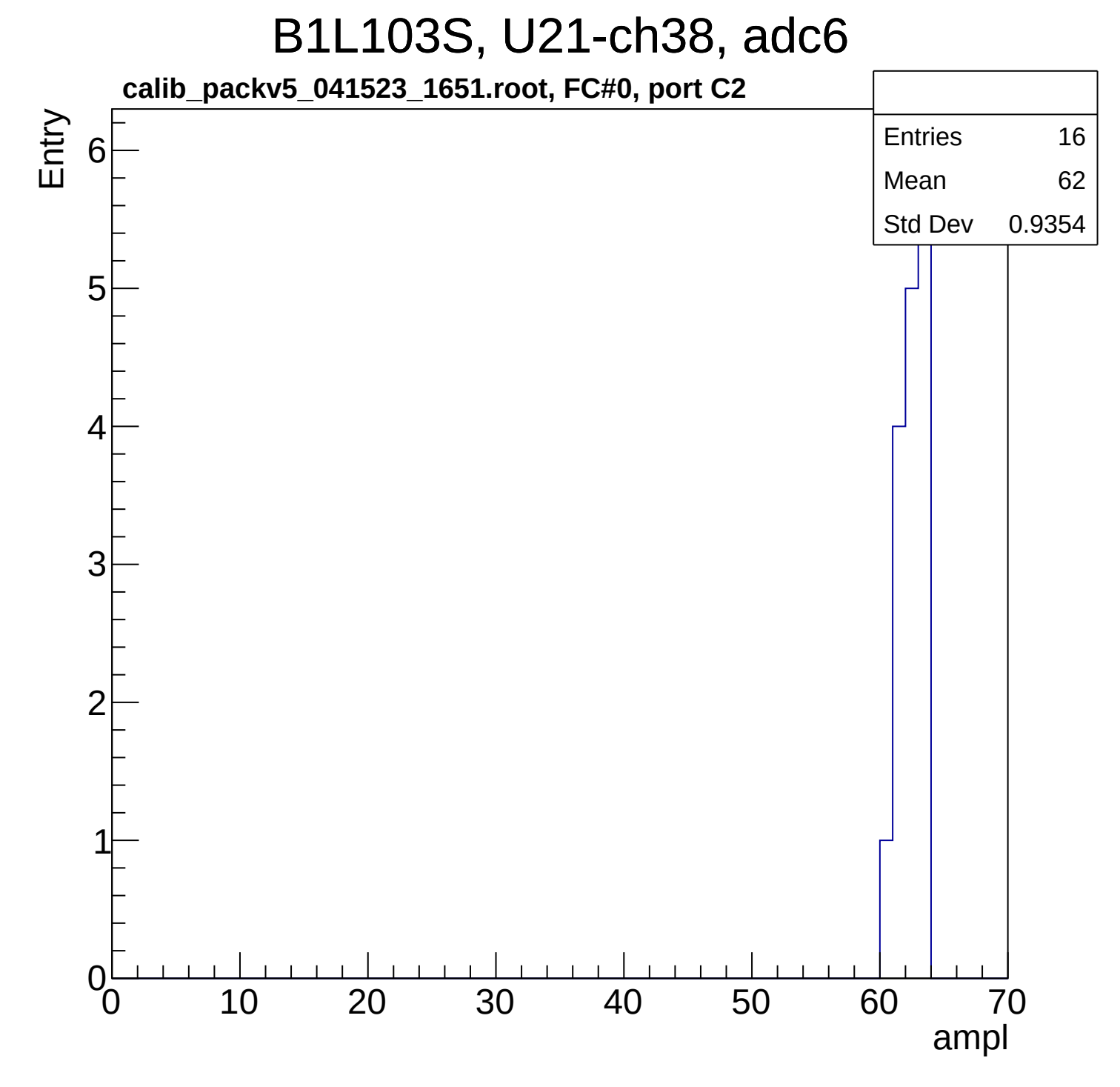
B1L103S, U21-ch38, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 62
Std Dev 0.9354
Entry
0
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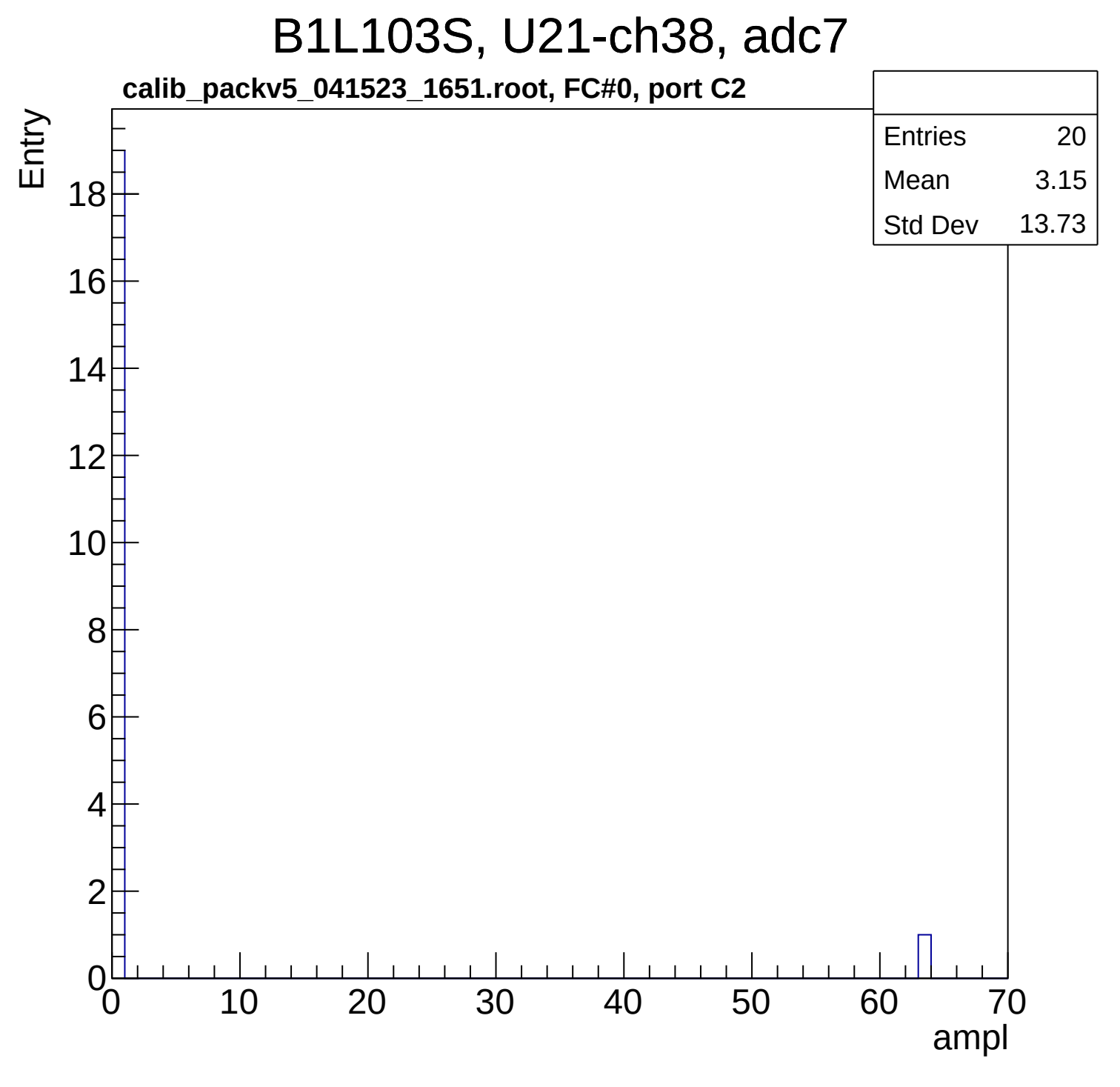
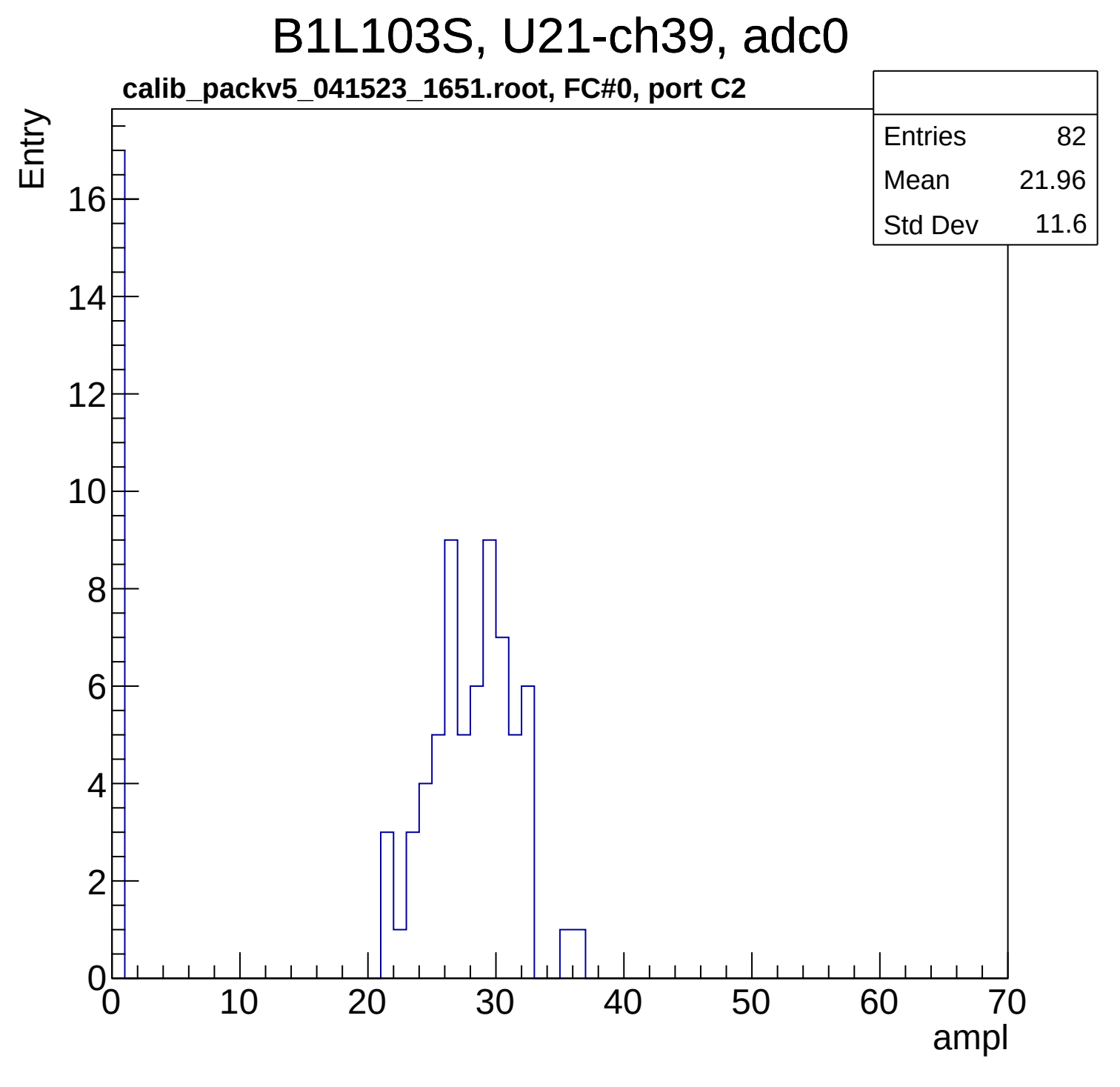
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch38, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch39, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 21.96
Std Dev 11.6
Entry
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4
6
8
10
12
14
16
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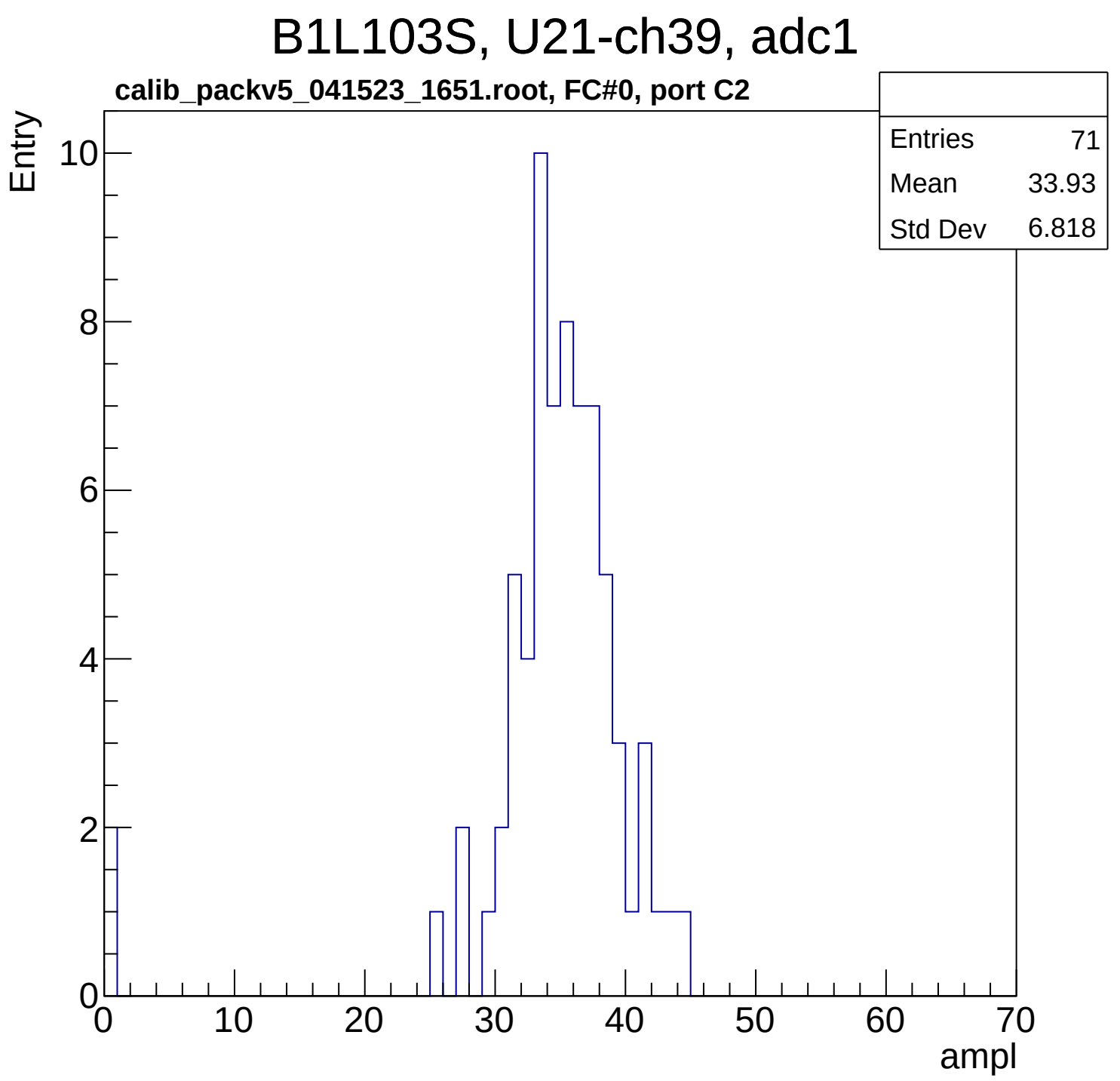
70
ampl


B1L103S, U21-ch39, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 33.93
Std Dev 6.818
Entry
ampl
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8
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40
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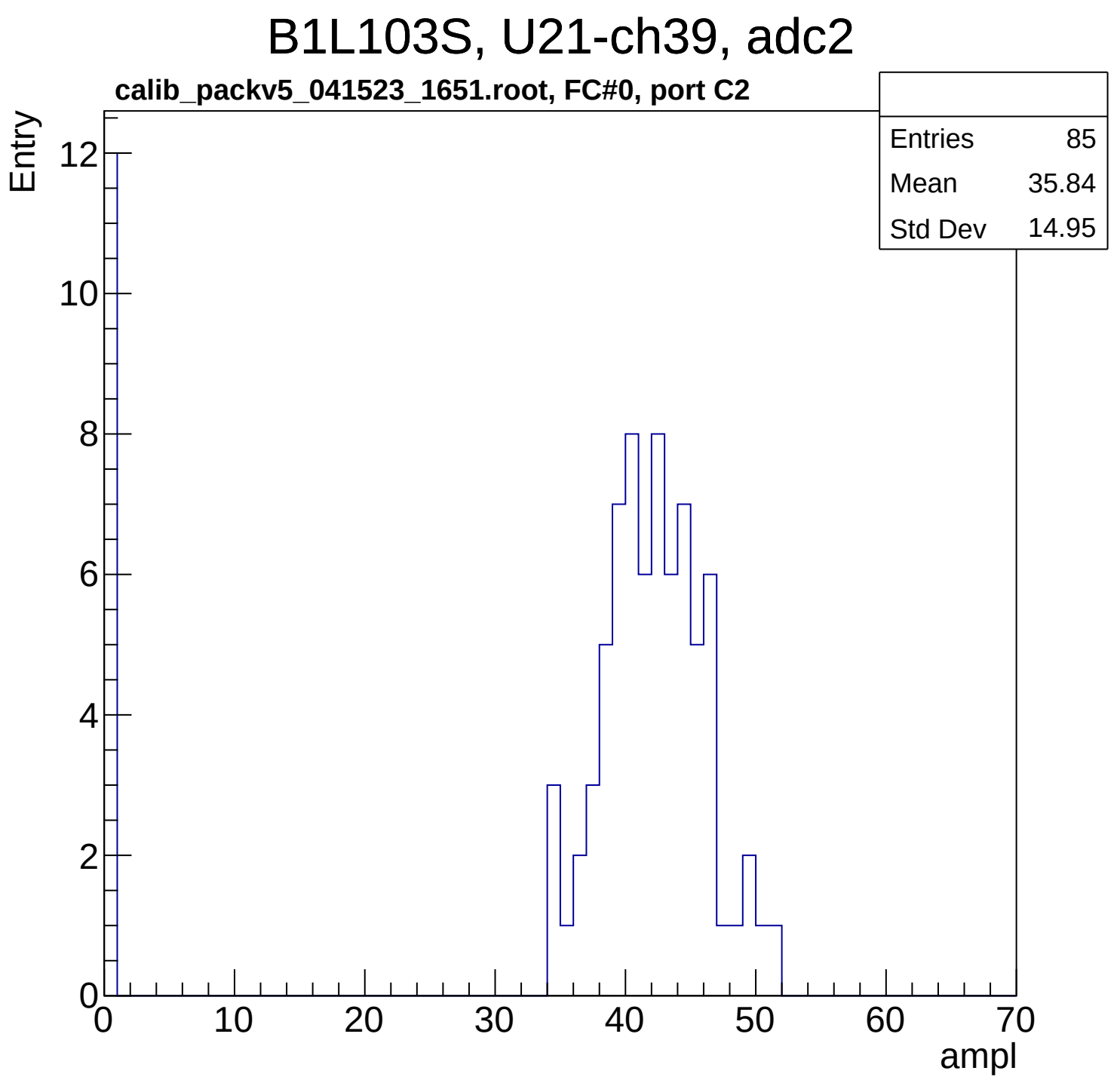
B1L103S, U21-ch39, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 35.84
Std Dev 14.95
Entry
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4
6
8
10
12
0
10
20
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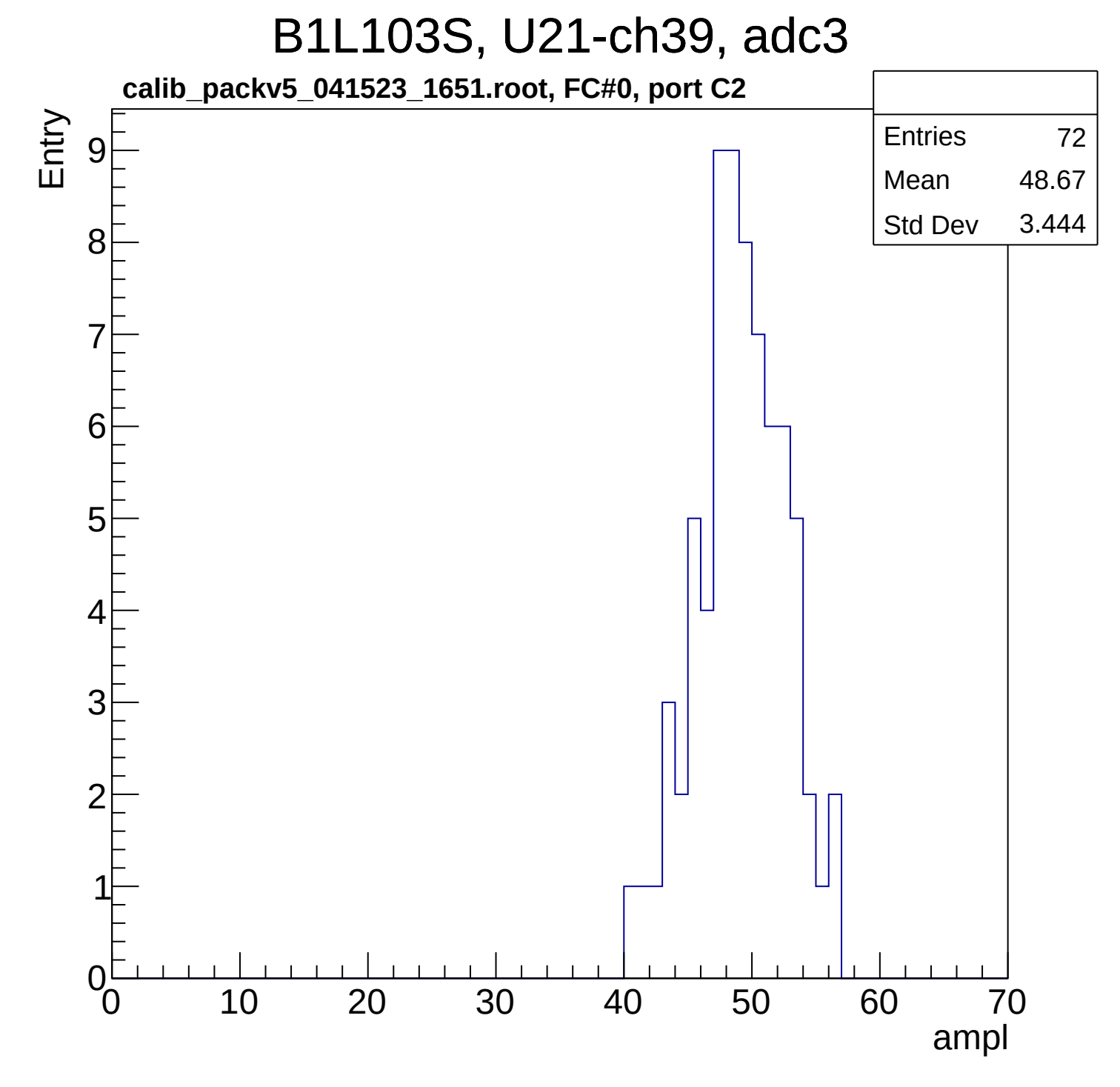
40
50
60
70
ampl


B1L103S, U21-ch39, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 48.67
Std Dev 3.444
Entry
ampl
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5
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0
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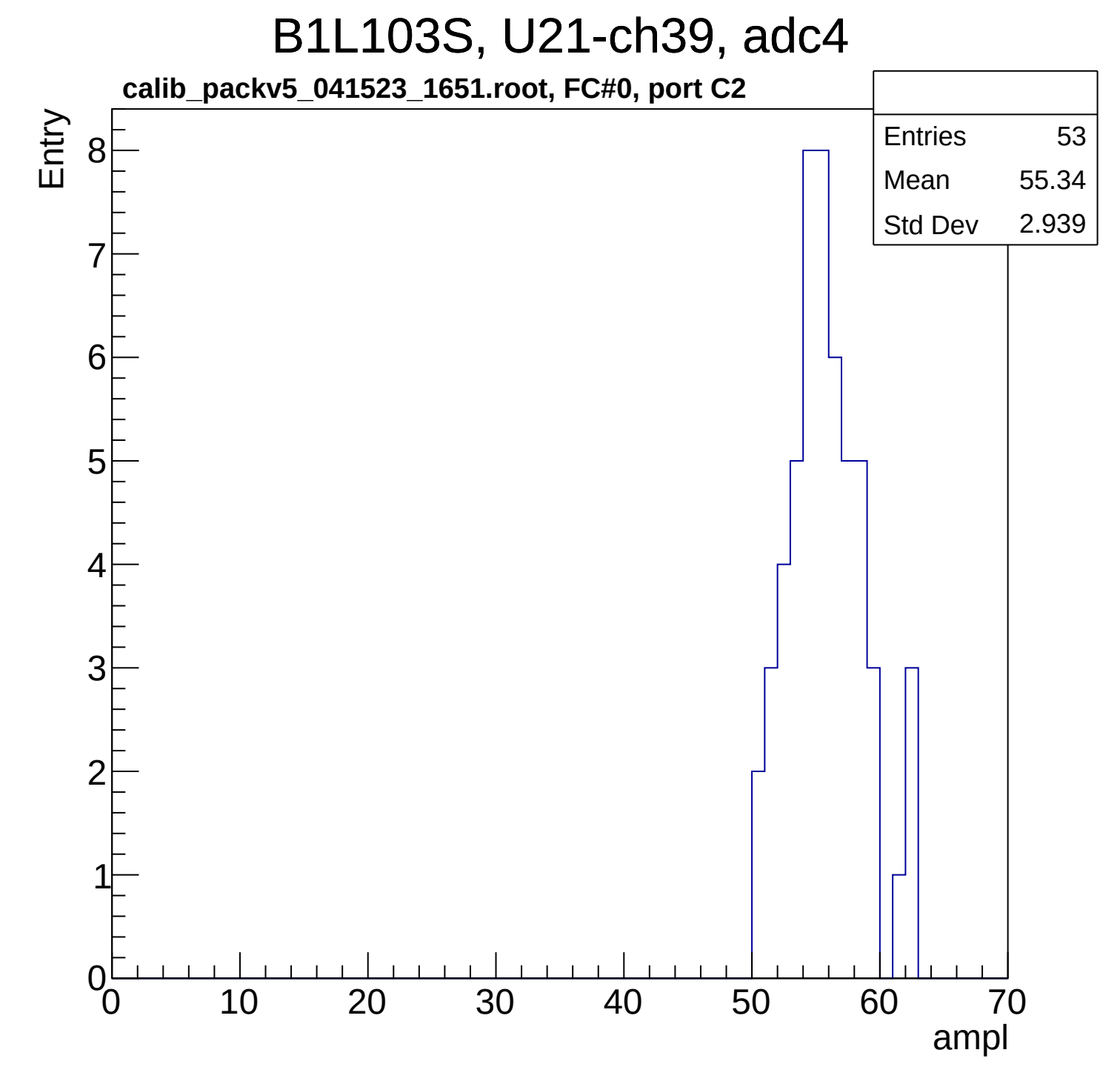
B1L103S, U21-ch39, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 55.34
Std Dev 2.939
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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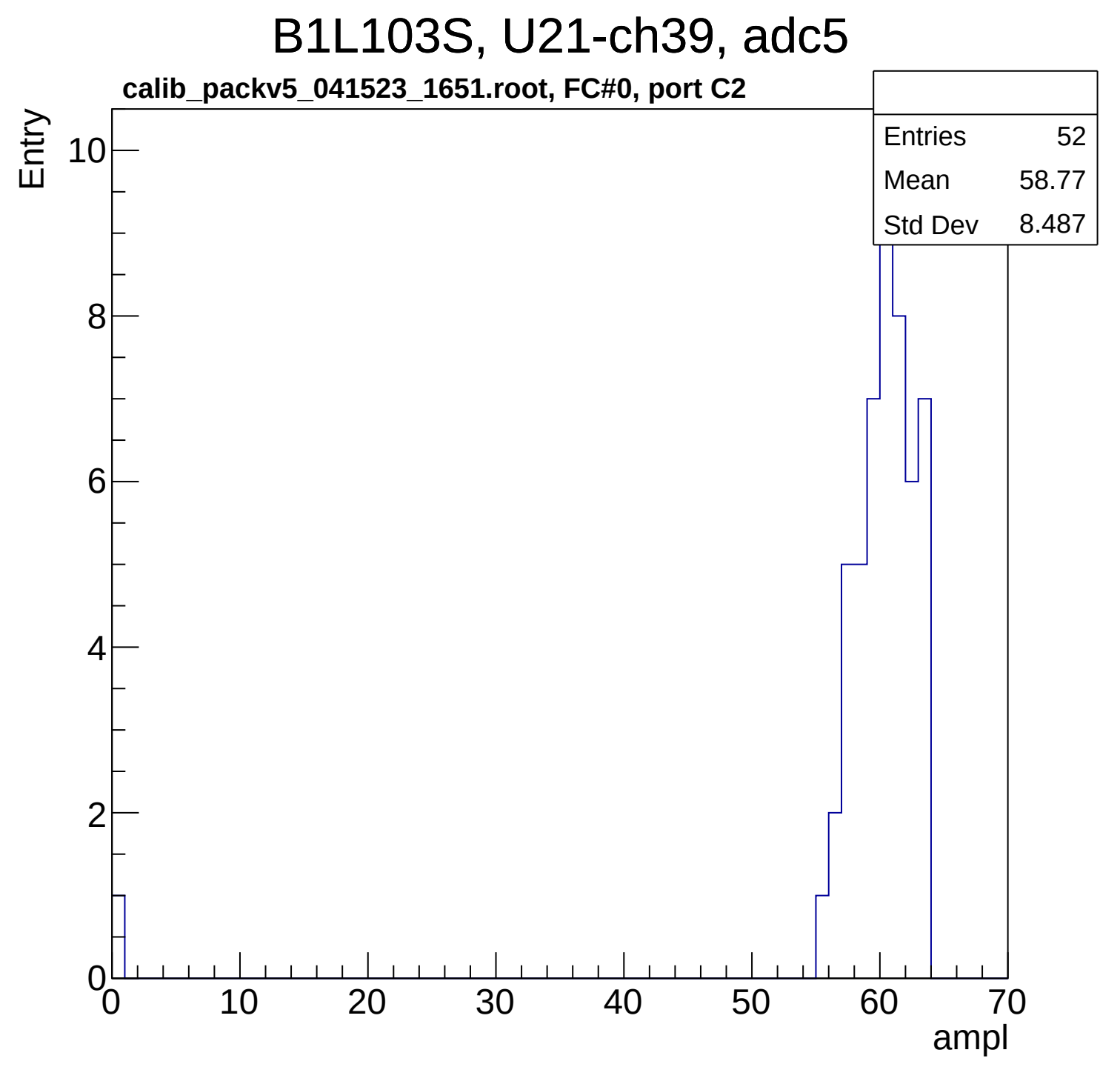
B1L103S, U21-ch39, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 58.77
Std Dev 8.487
Entry
ampl
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2
4
6
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0
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20
30
40
50
60
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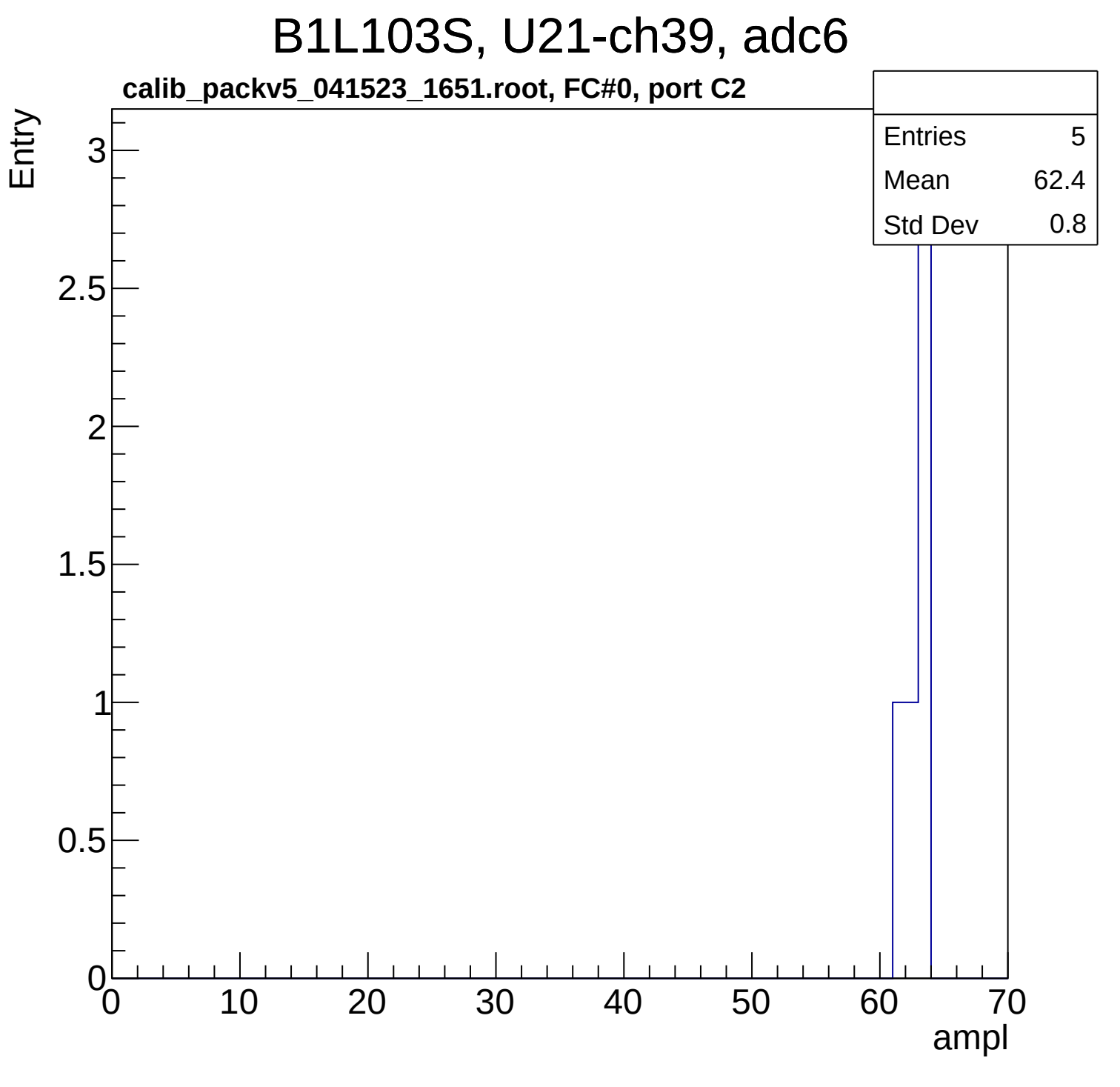
B1L103S, U21-ch39, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 62.4
Std Dev 0.8
Entry
ampl
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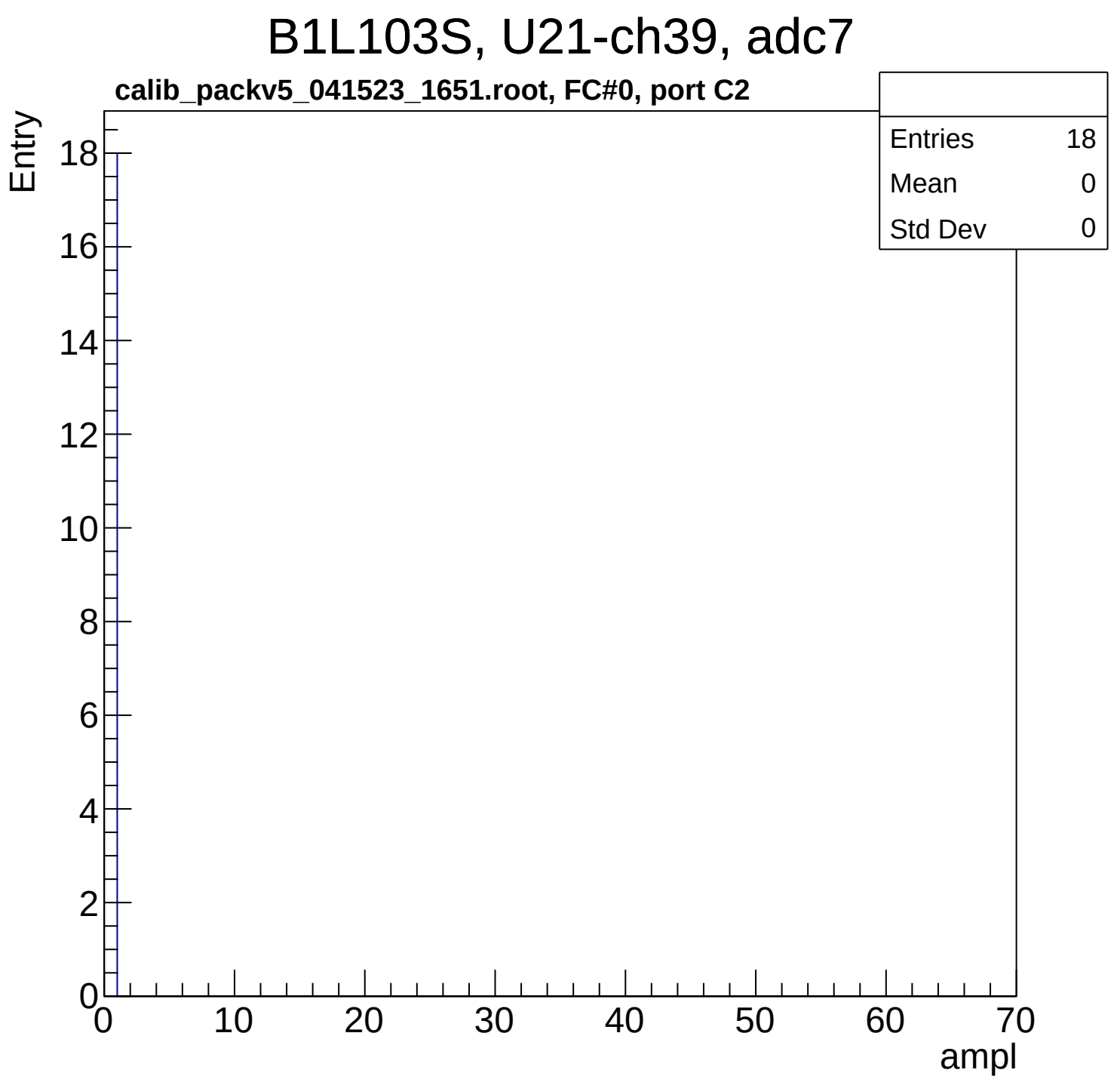
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U21-ch39, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
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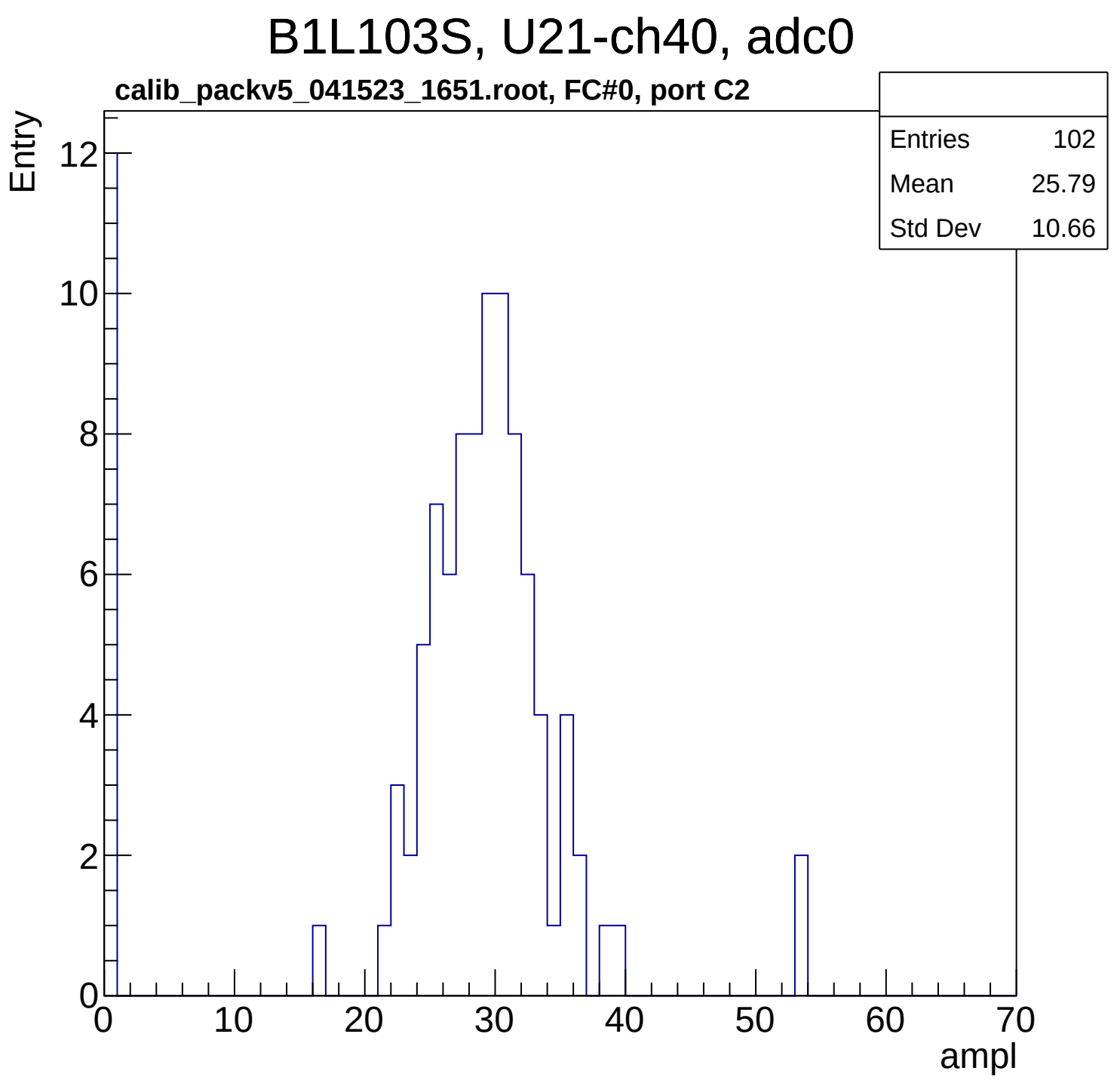
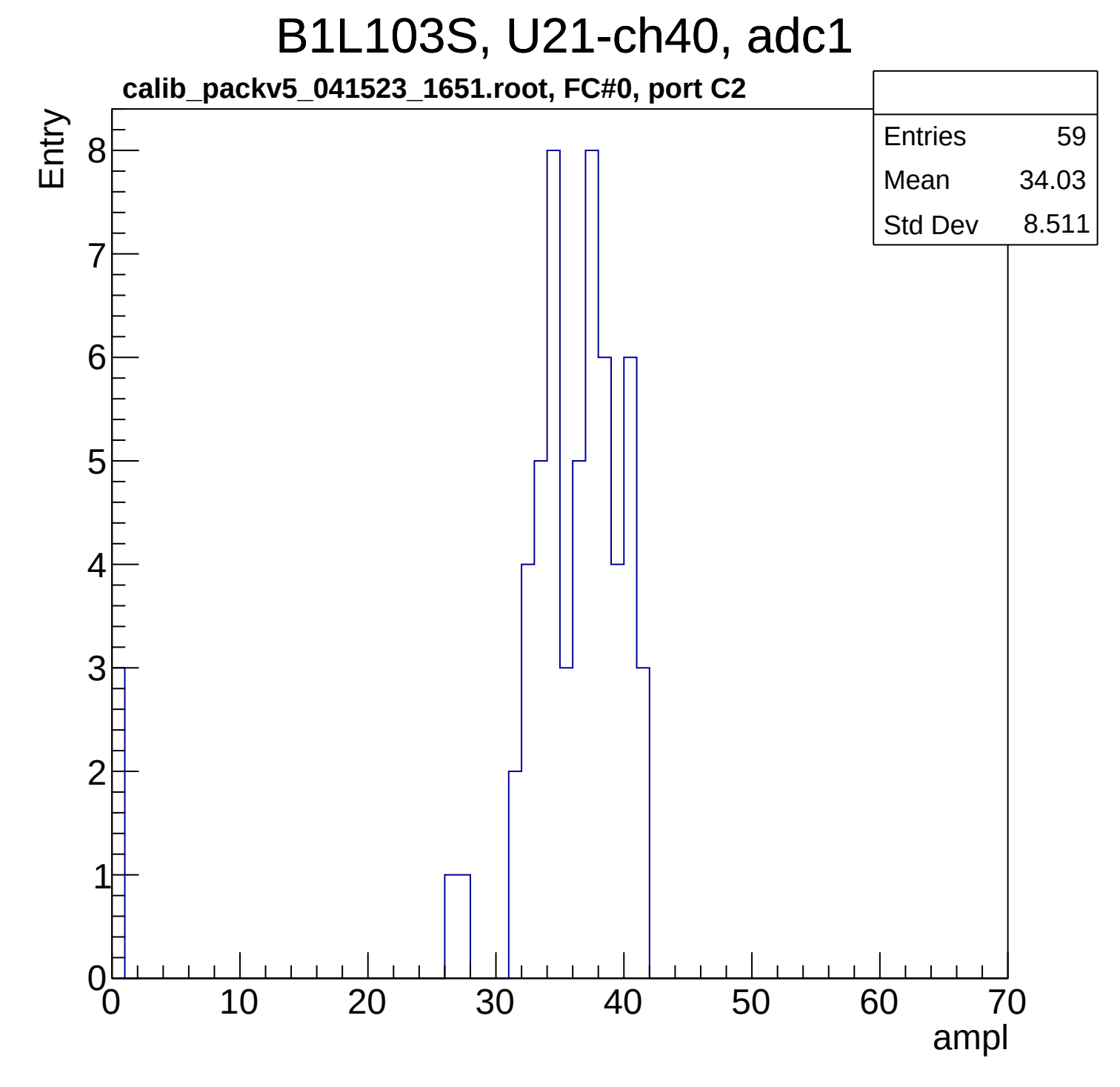
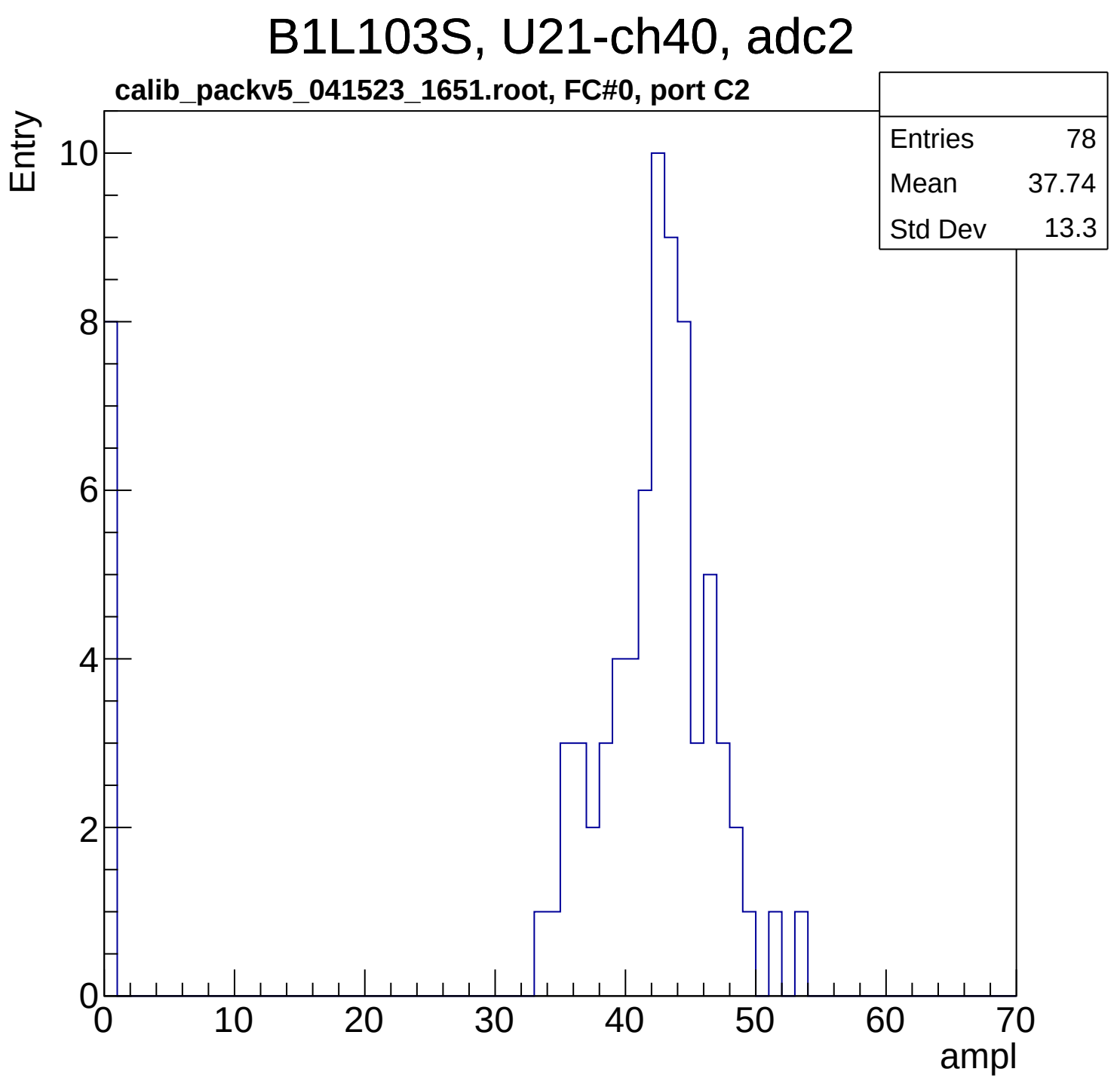
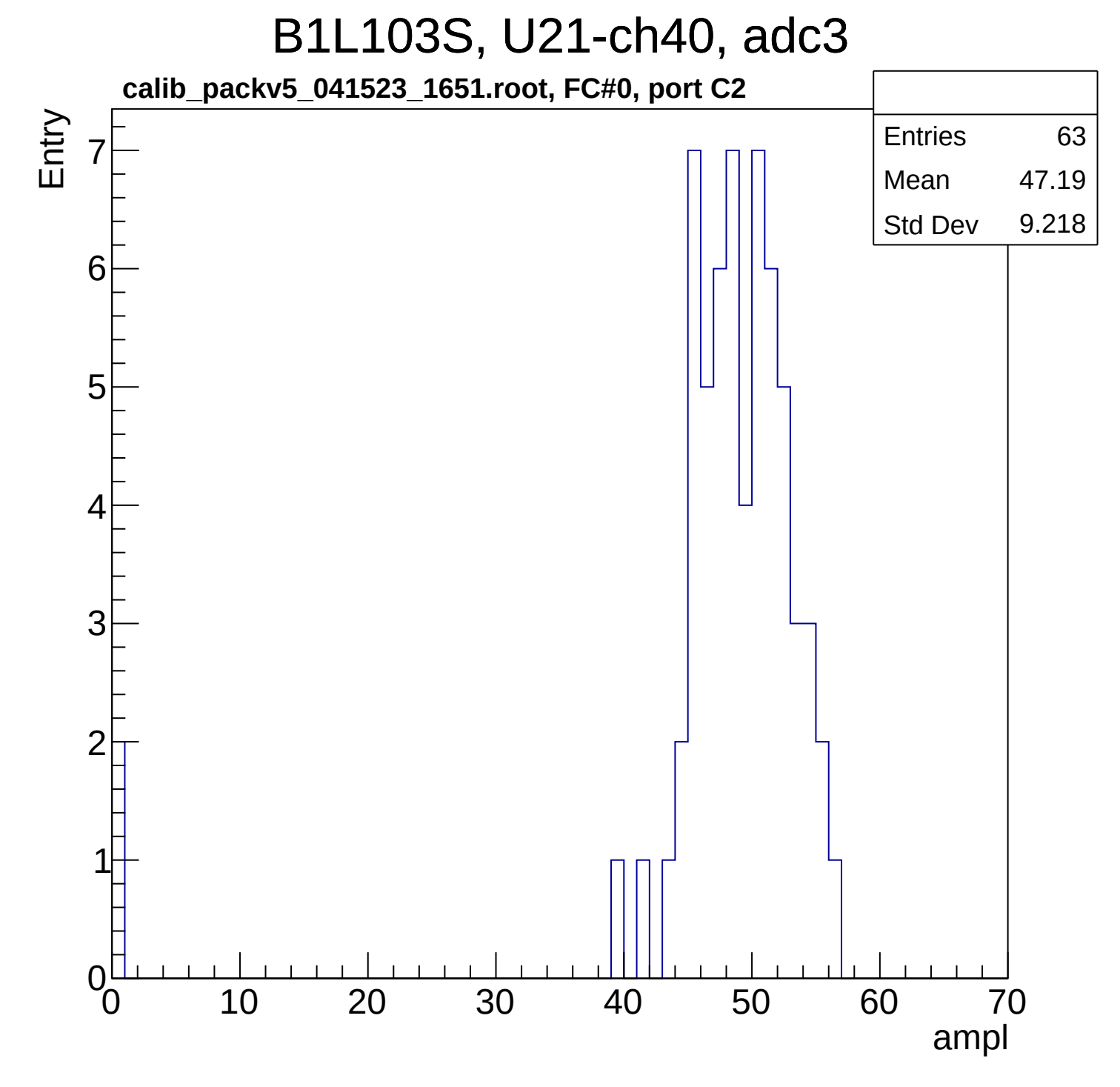
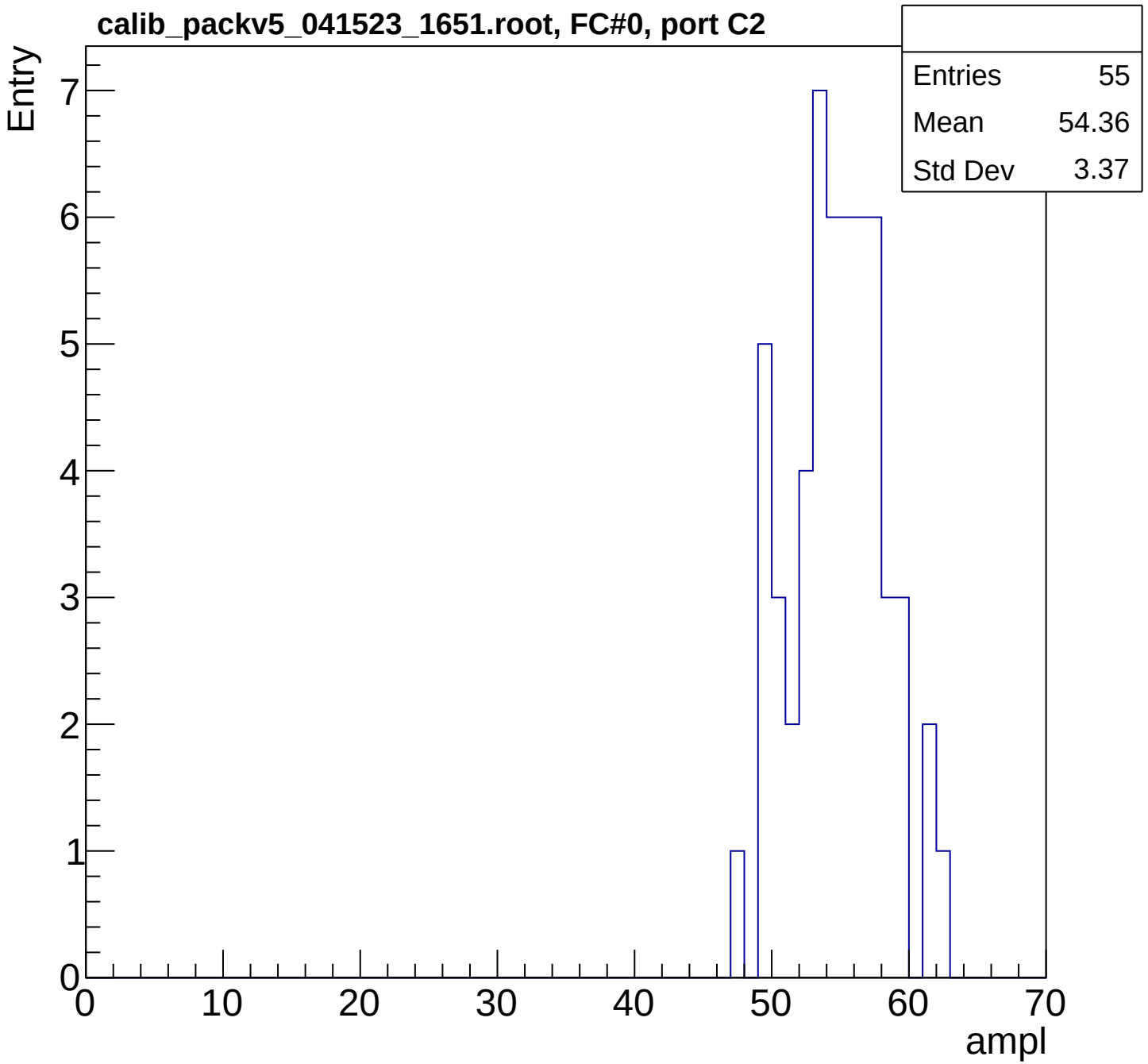
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

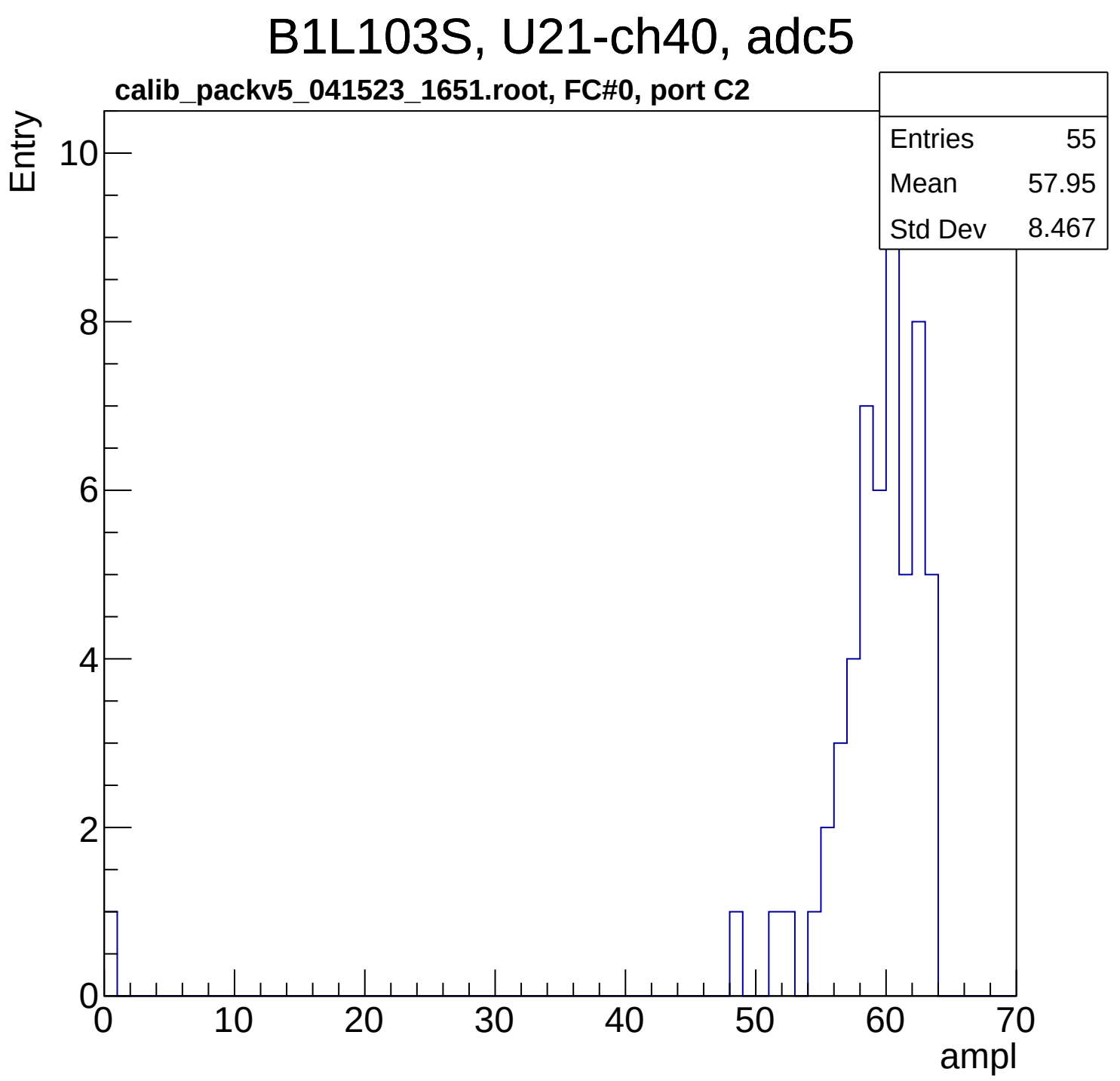

B1L103S, U21-ch40, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 102
Mean 25.79
Std Dev 10.66
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

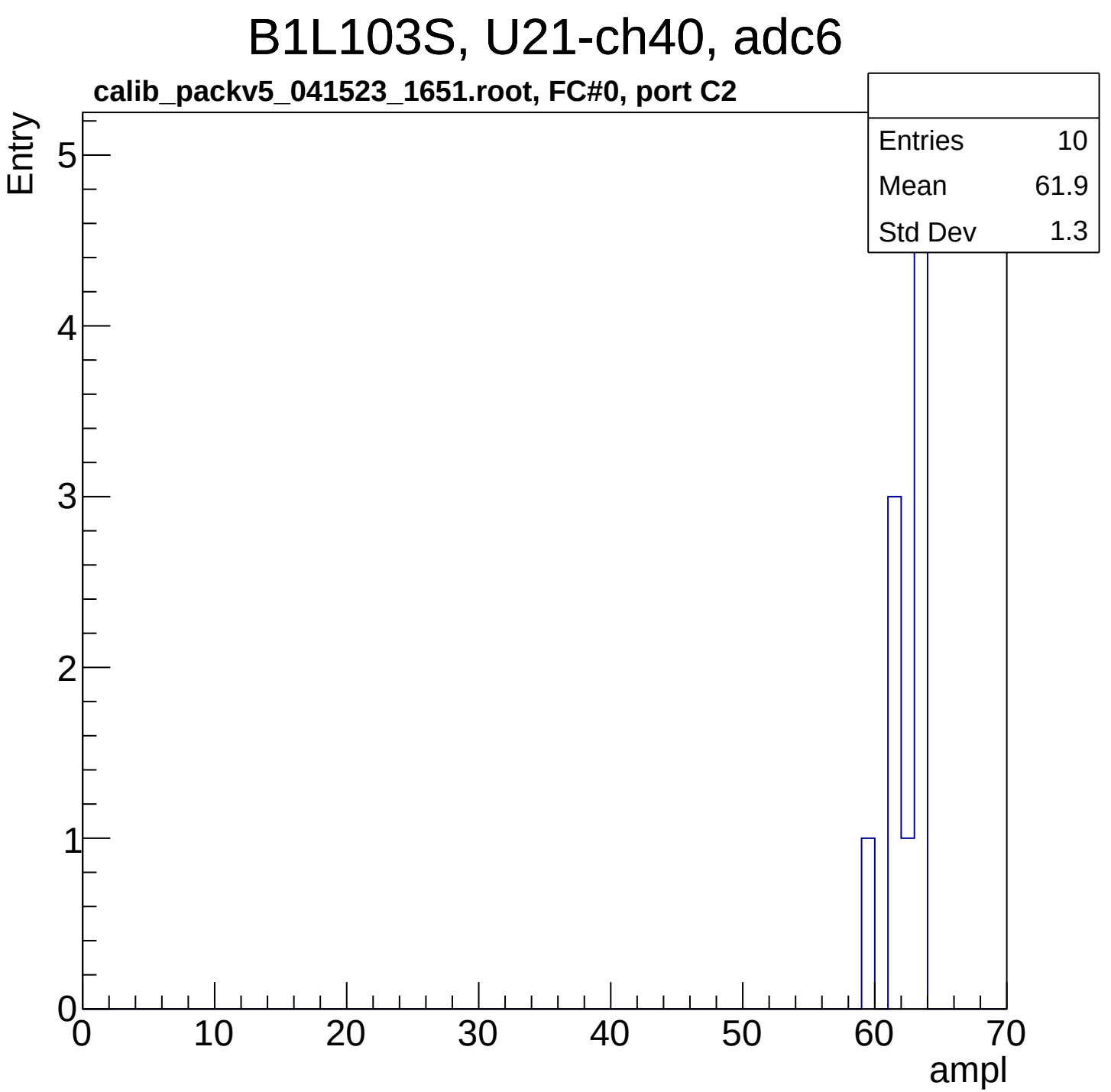

B1L103S, U21-ch40, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 34.03
Std Dev 8.511
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

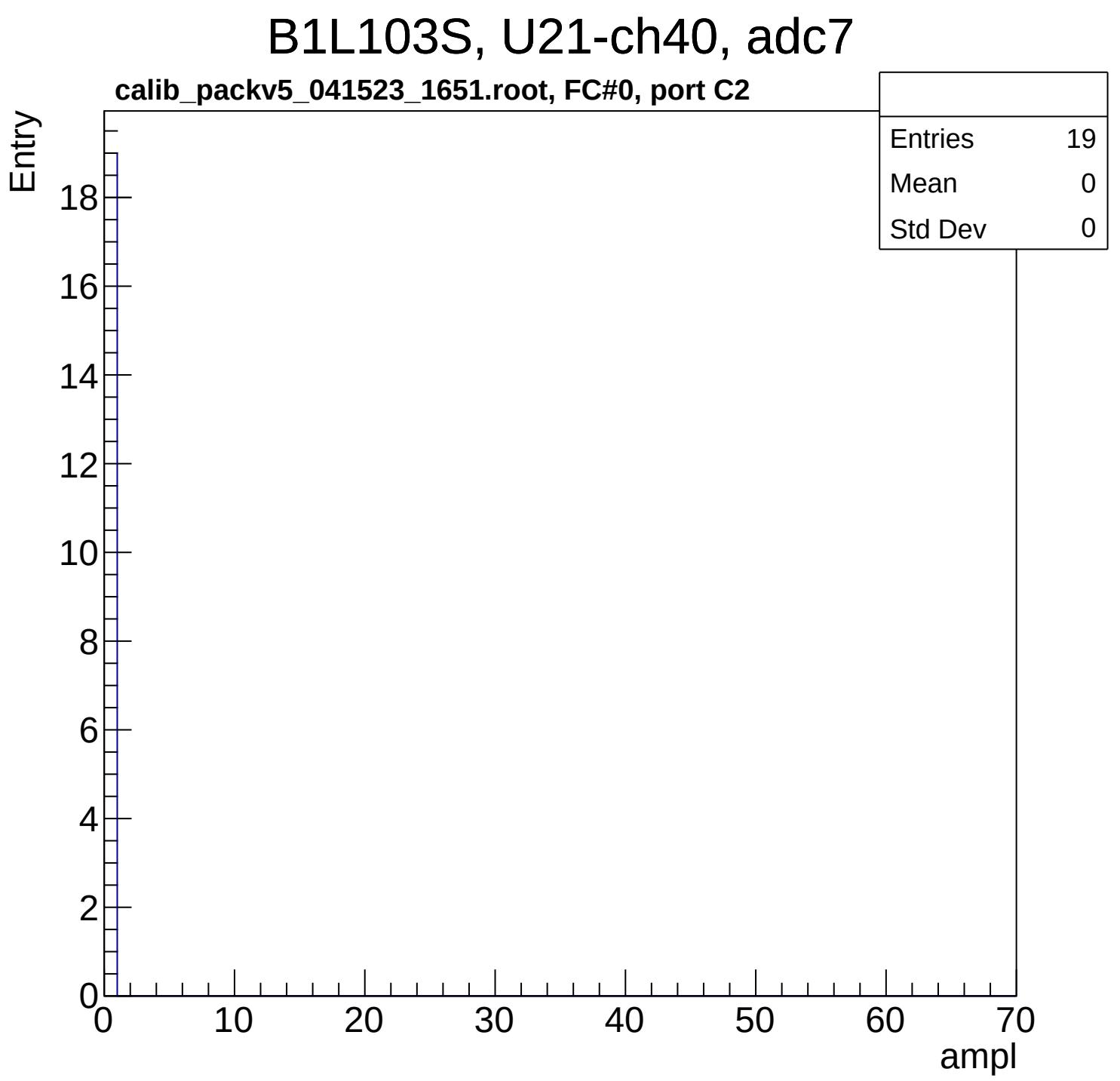

B1L103S, U21-ch40, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 37.74
Std Dev 13.3
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

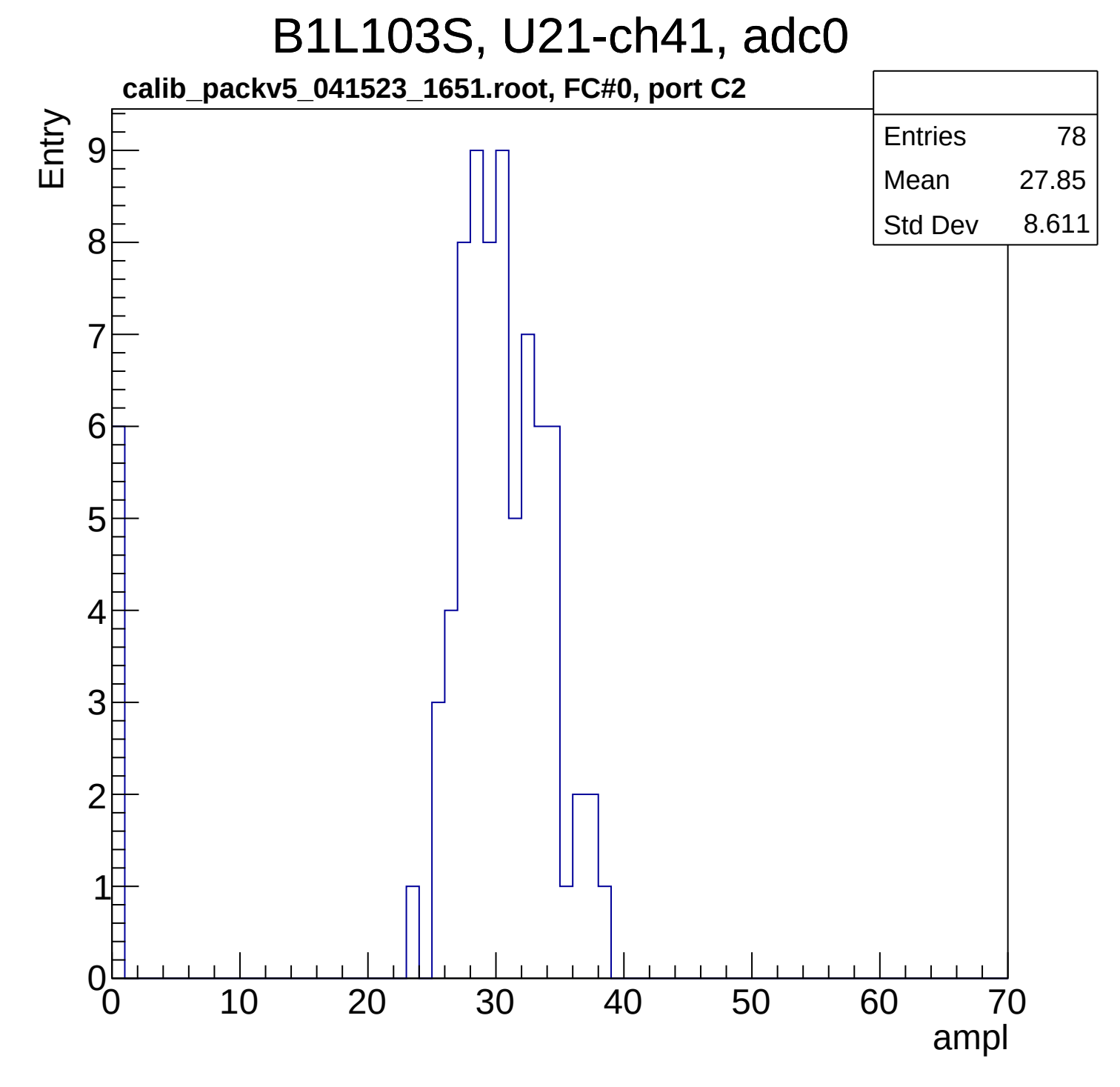

B1L103S, U21-ch40, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 47.19
Std Dev 9.218
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U21-ch40, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 54.36
Std Dev 3.37
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U21-ch40, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 57.95
Std Dev 8.467
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch40, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61.9
Std Dev 1.3
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch40, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch41, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 27.85
Std Dev 8.611
Entry
ampl
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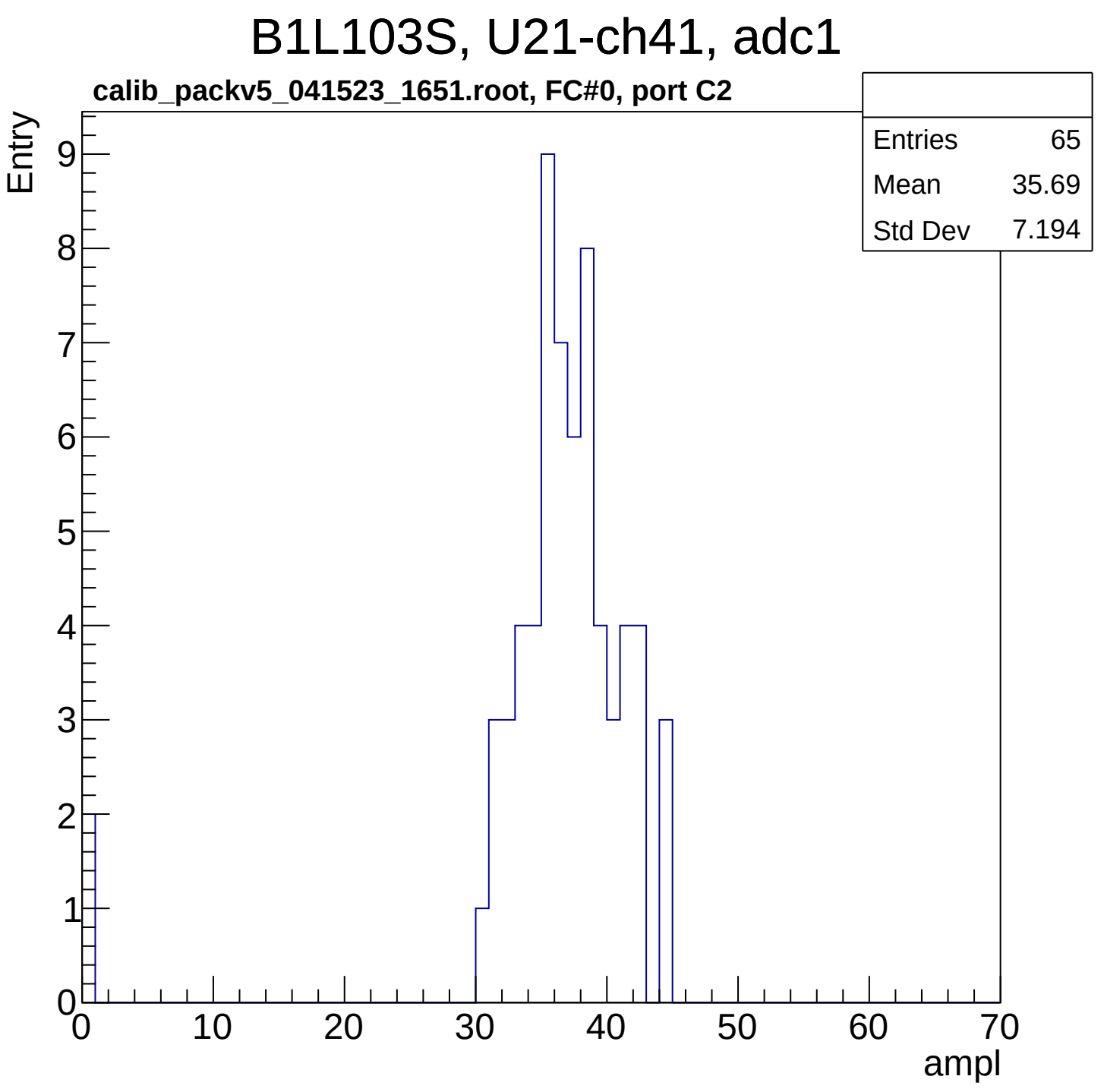
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch41, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 35.69
Std Dev 7.194
Entry
ampl
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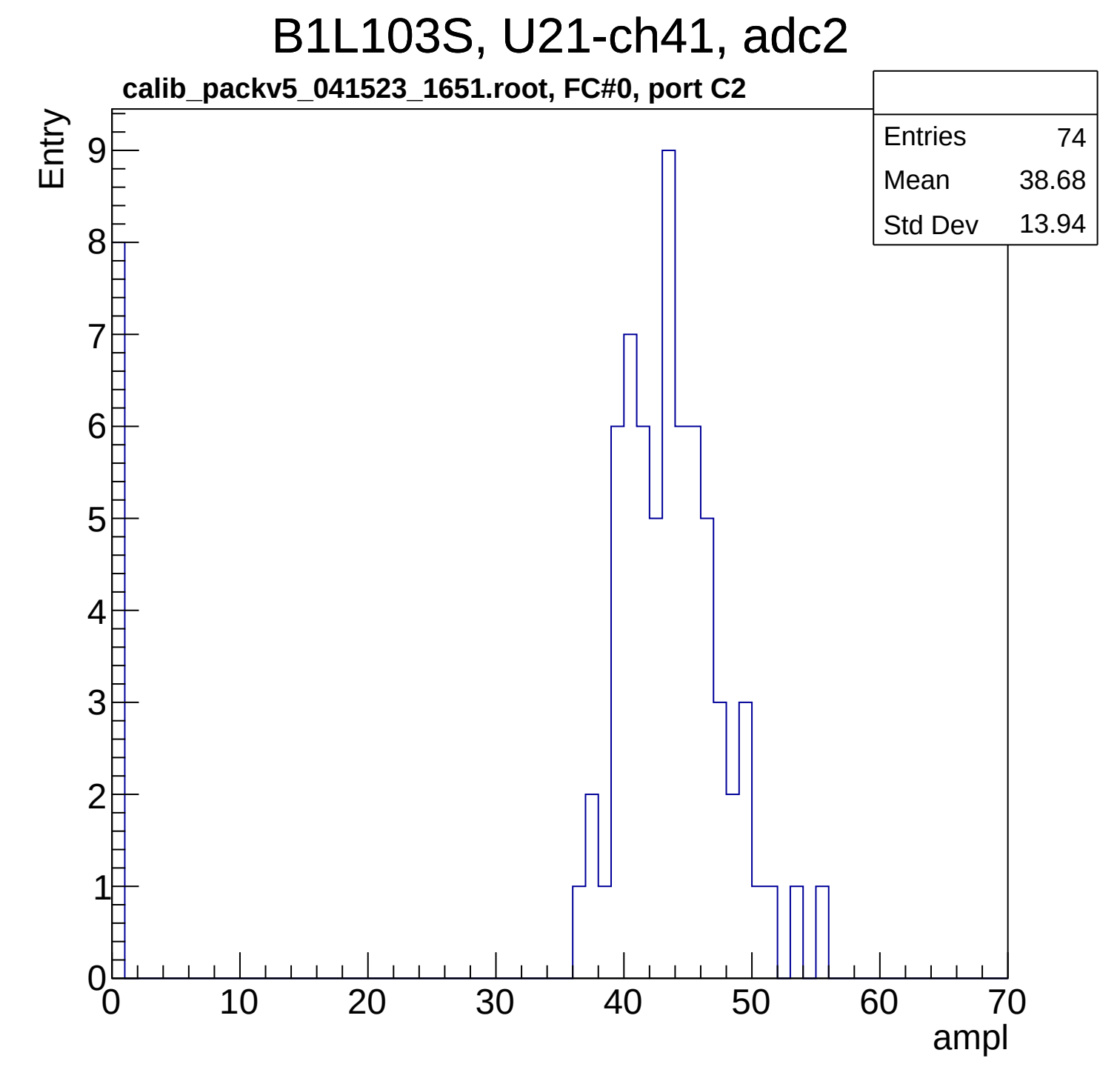
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch41, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 38.68
Std Dev 13.94
Entry
ampl
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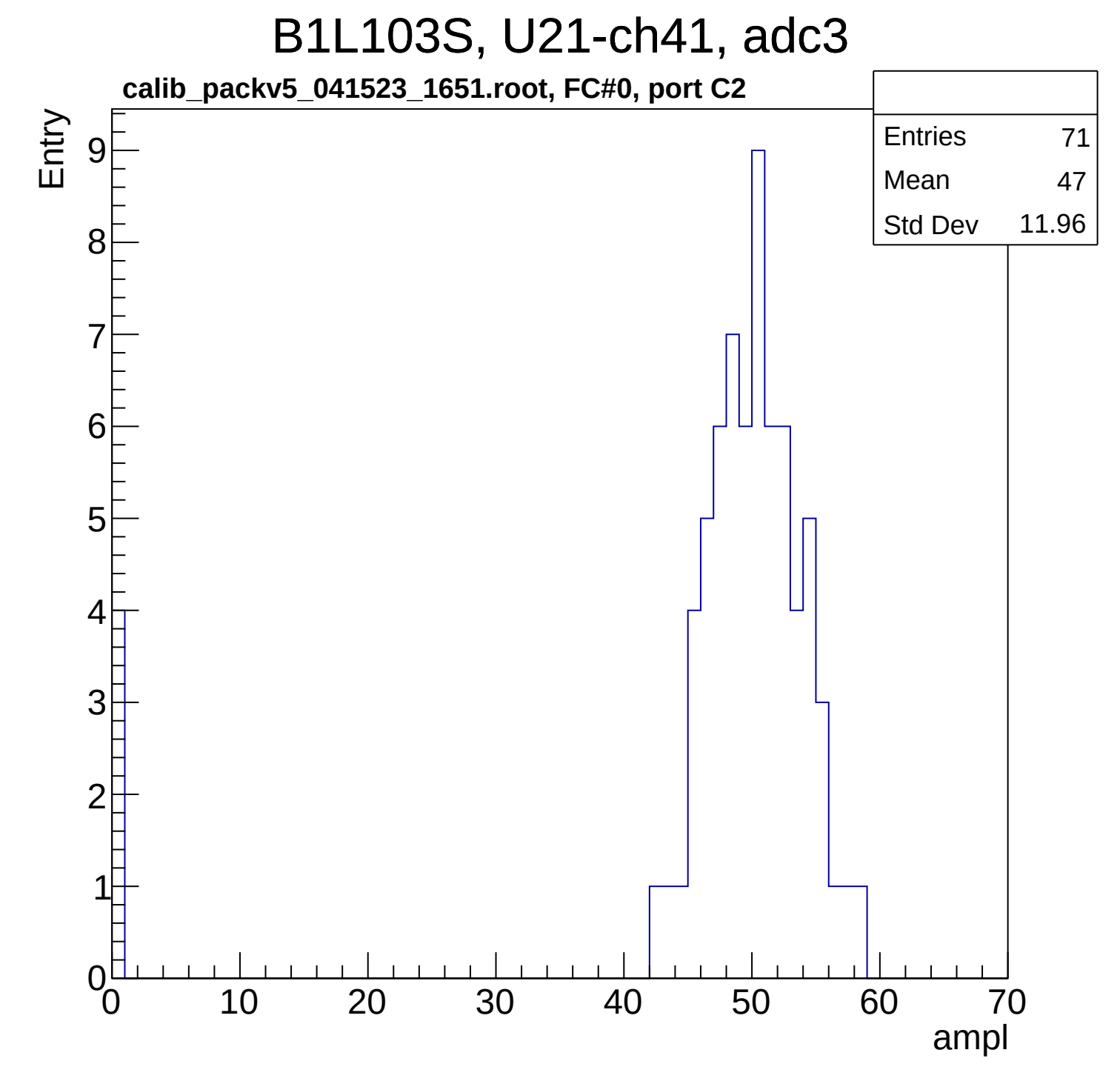
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch41, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 47
Std Dev 11.96
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
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30
40
50
60
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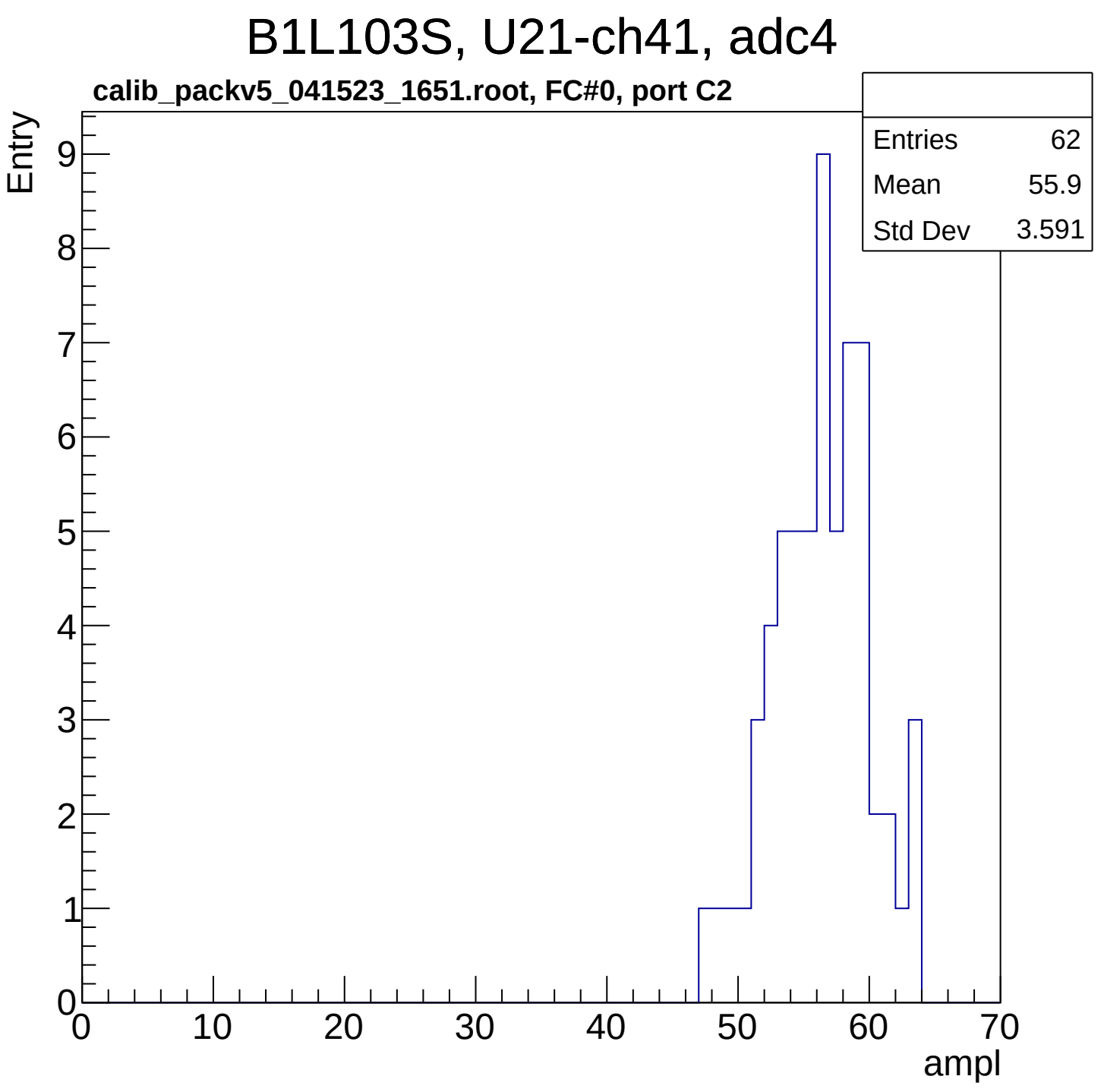
B1L103S, U21-ch41, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 55.9
Std Dev 3.591
Entry
ampl
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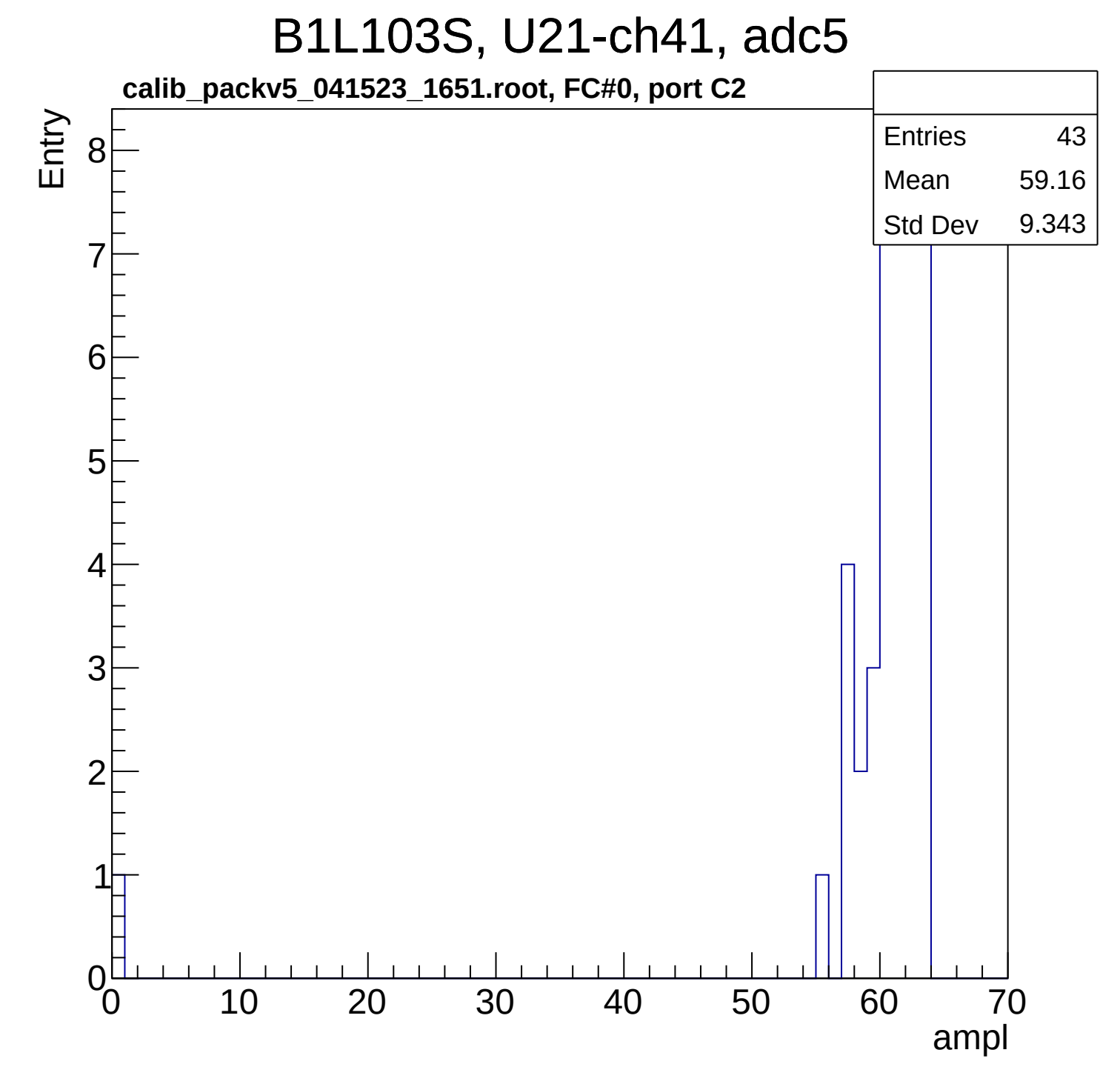
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch41, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 59.16
Std Dev 9.343
Entry
ampl
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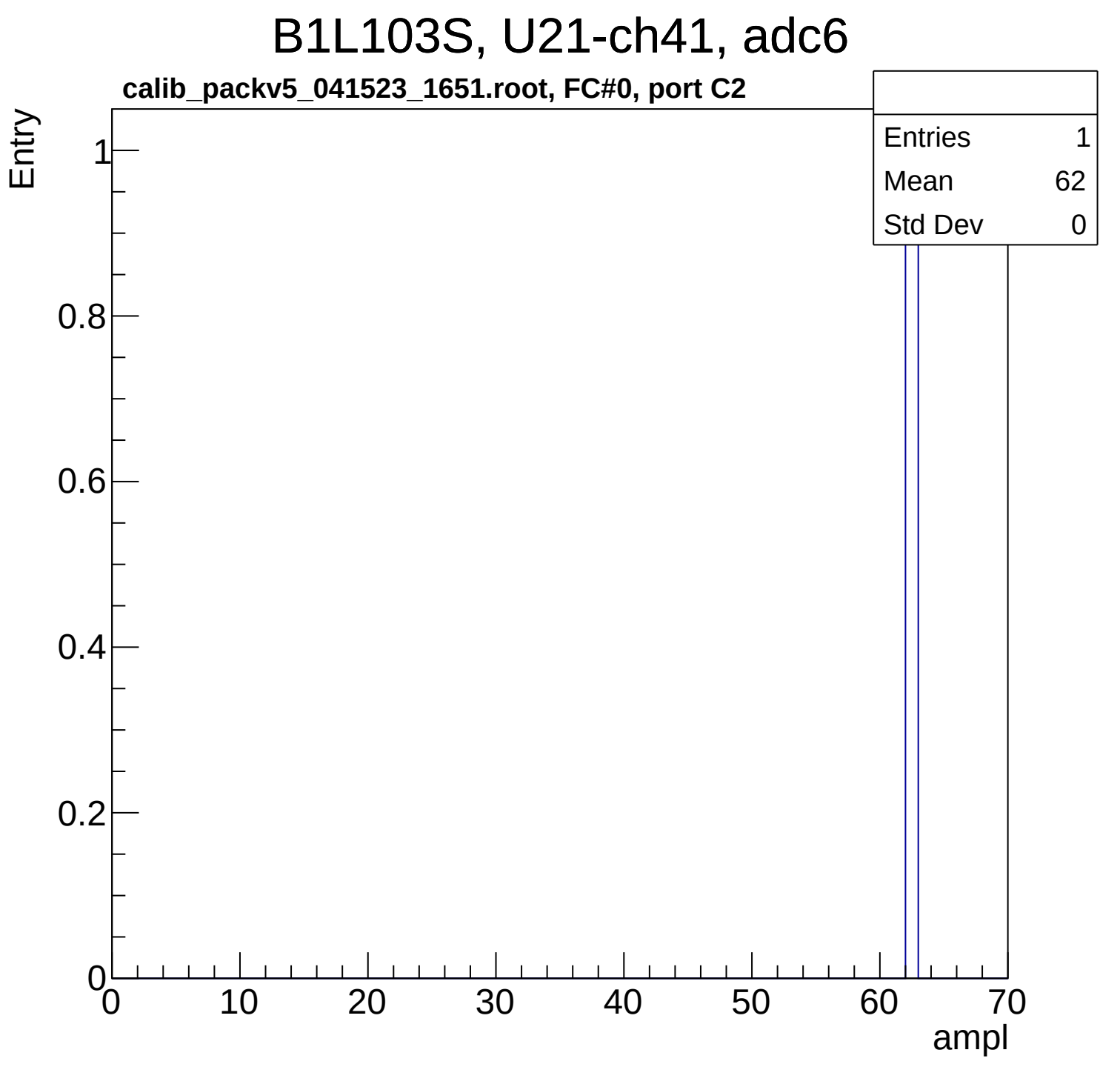
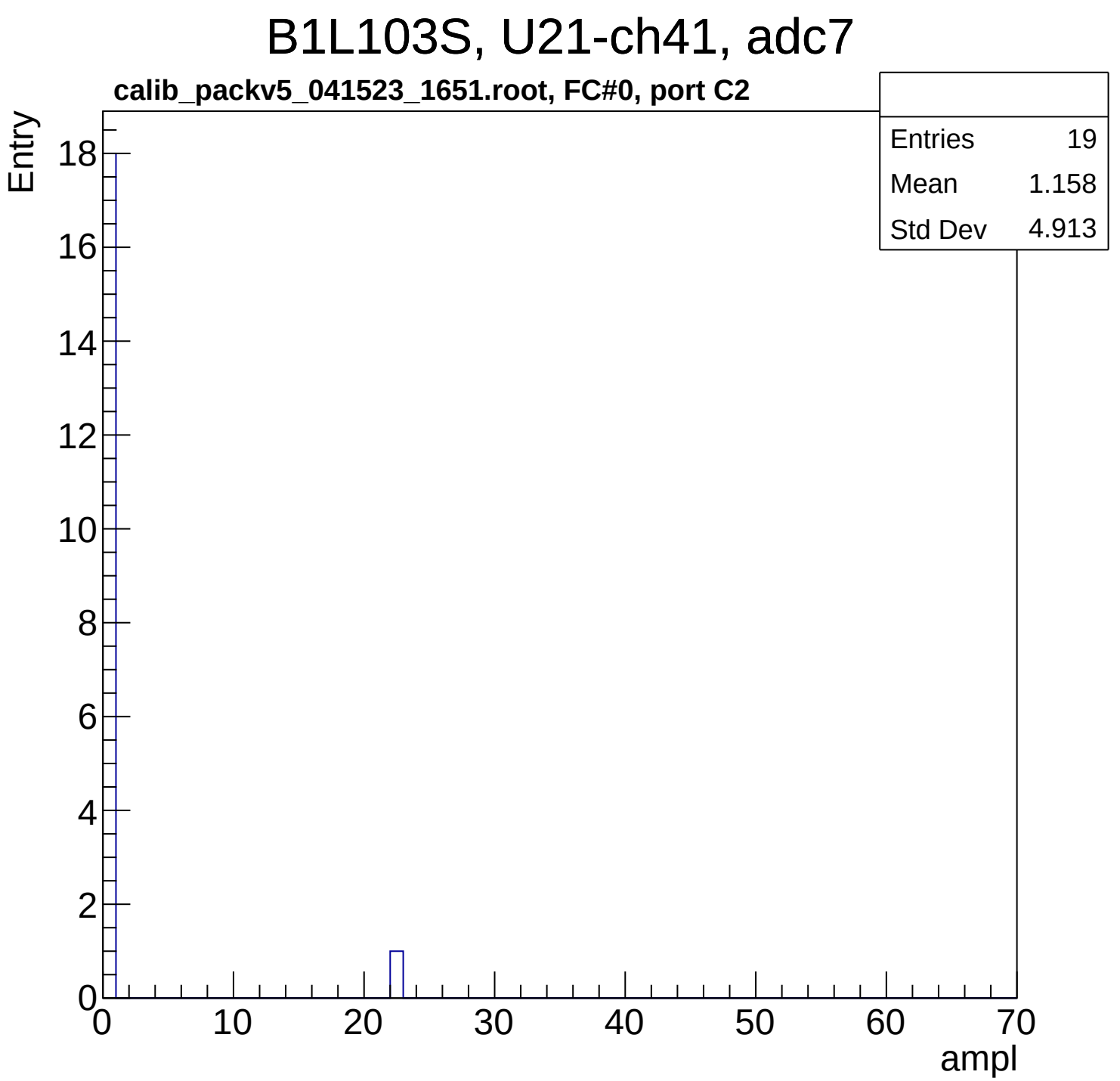
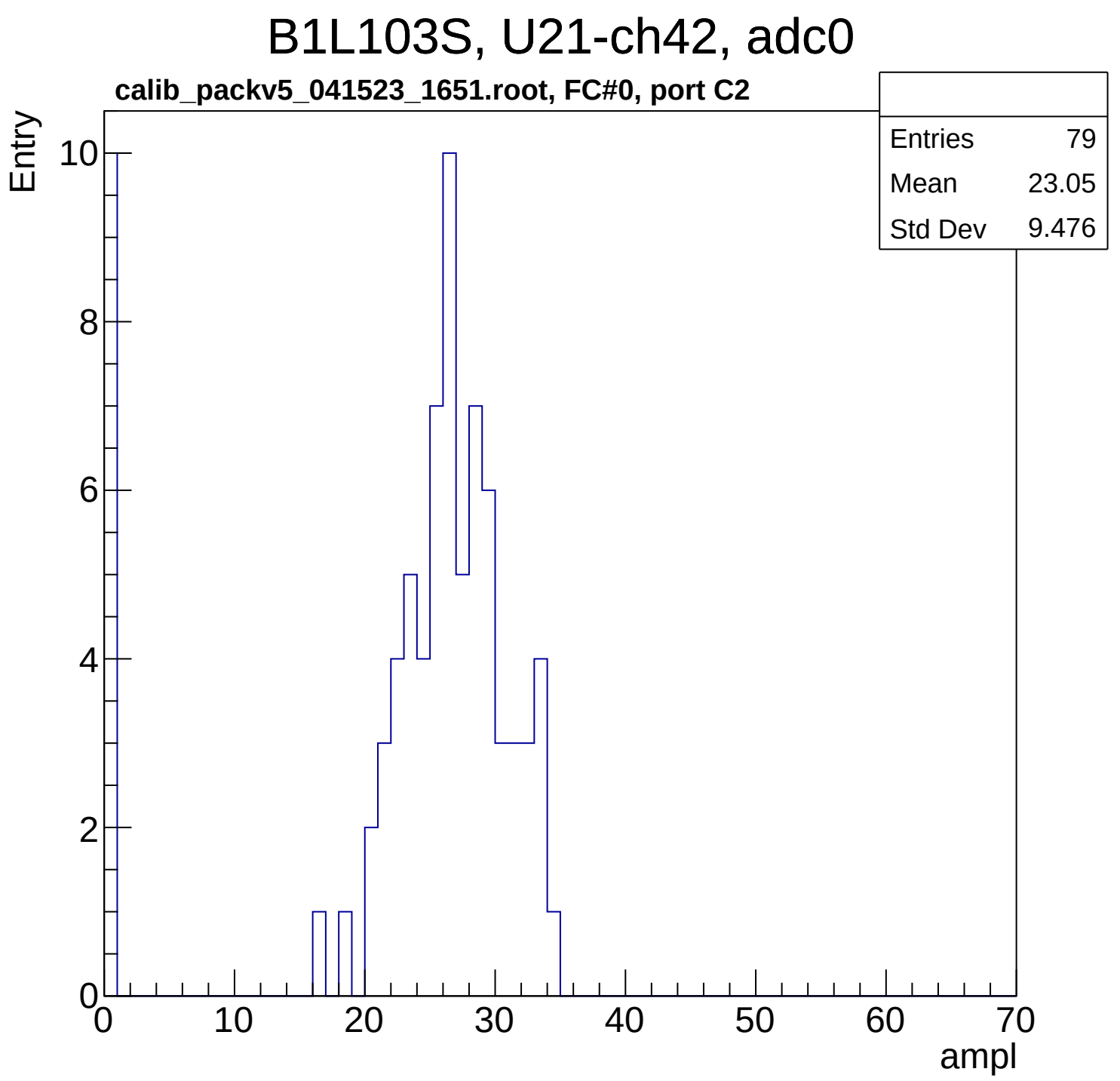
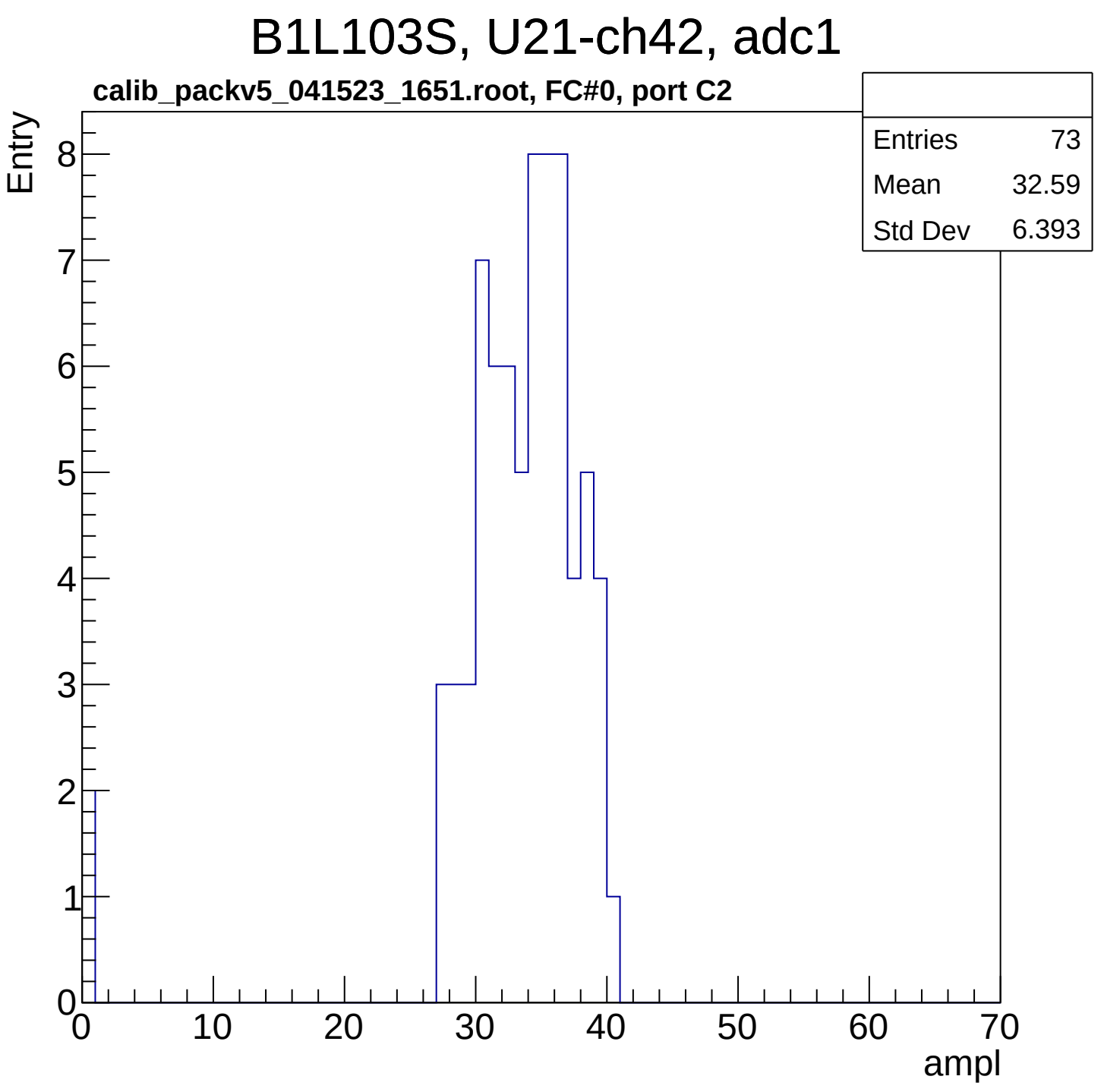
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch41, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 1
Mean 62
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch41, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.158
Std Dev 4.913
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch42, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 23.05
Std Dev 9.476
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch42, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 32.59
Std Dev 6.393
Entry
ampl
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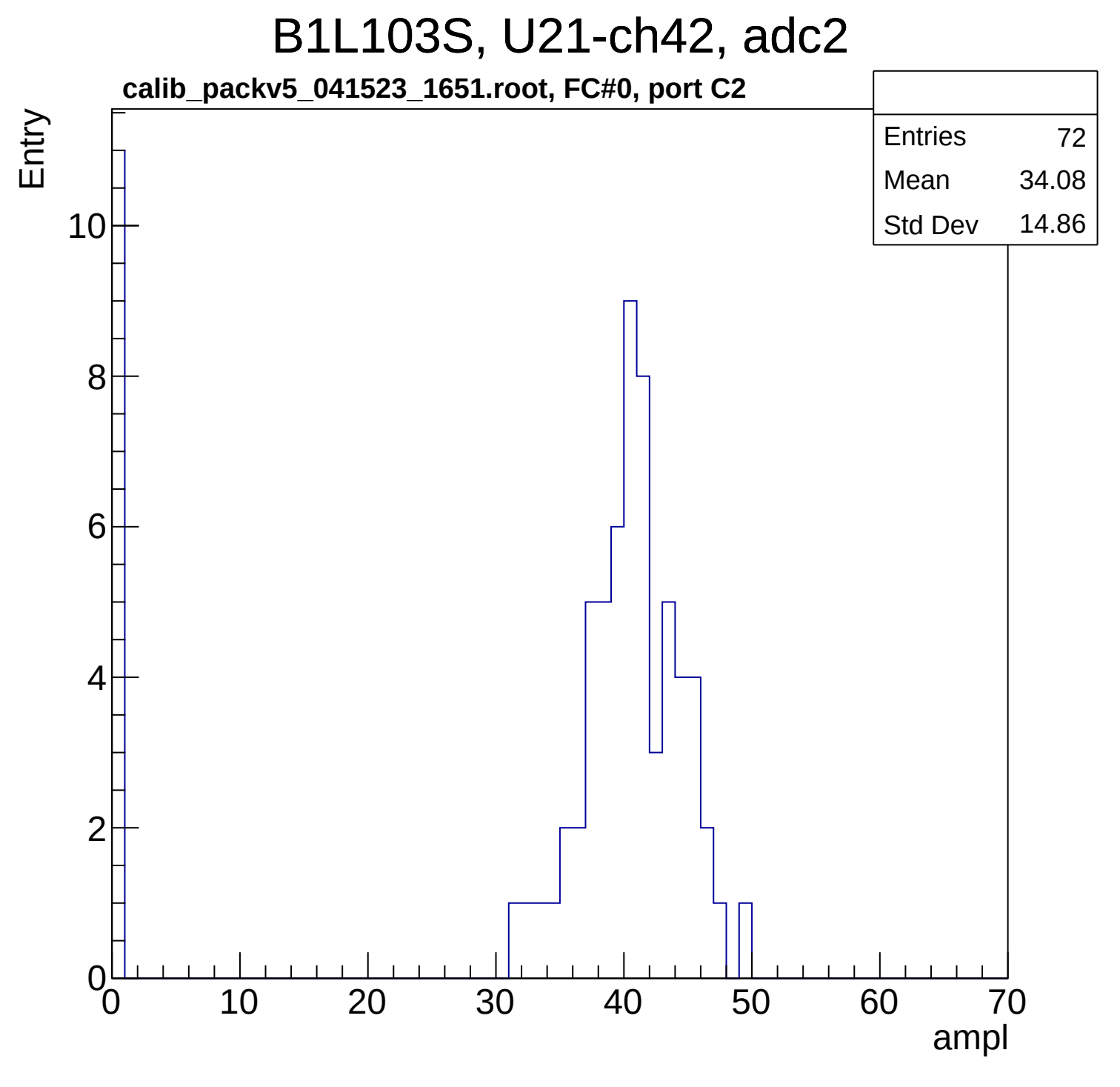
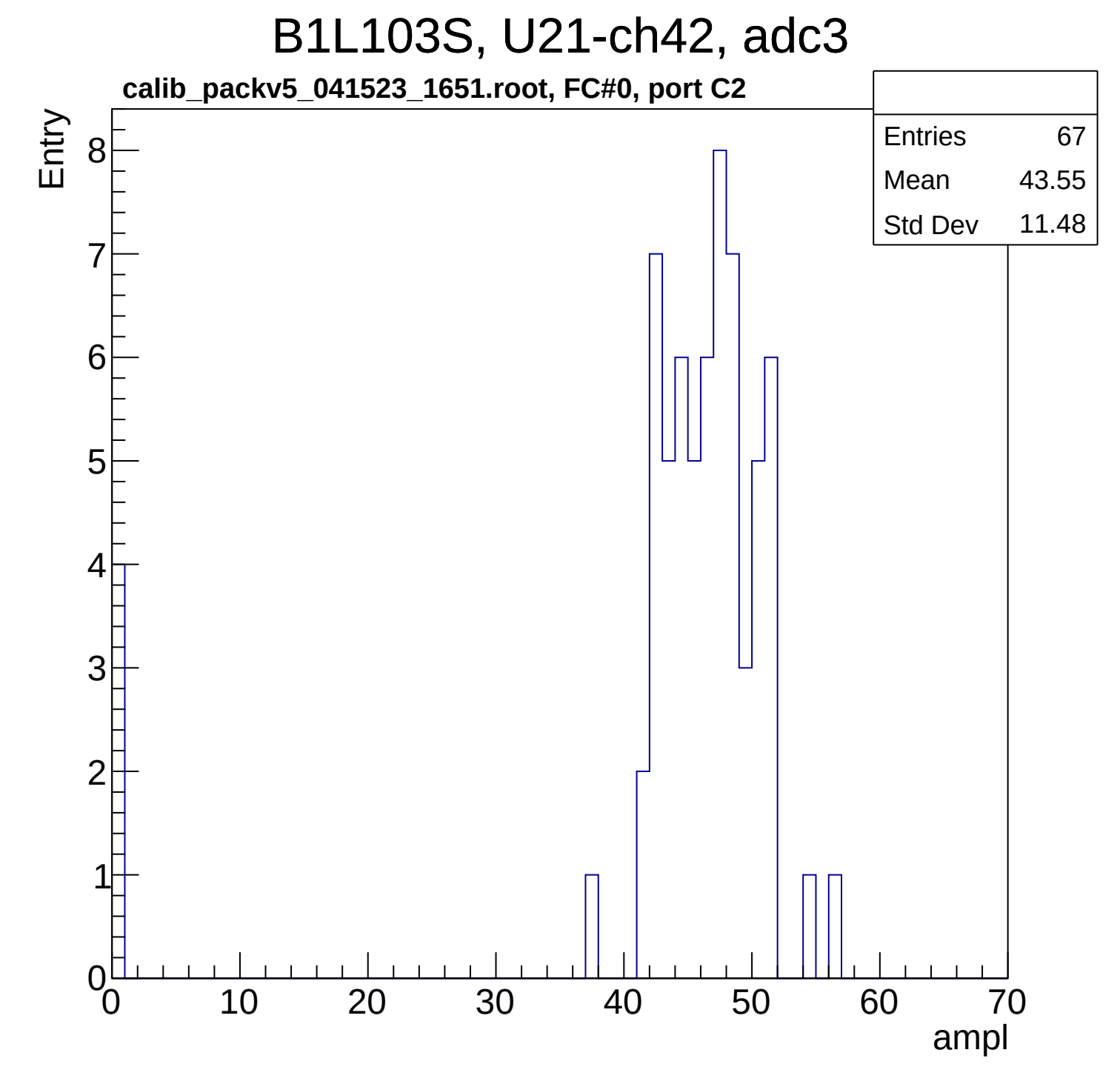
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch42, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 34.08
Std Dev 14.86
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch42, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 43.55
Std Dev 11.48
Entry
ampl
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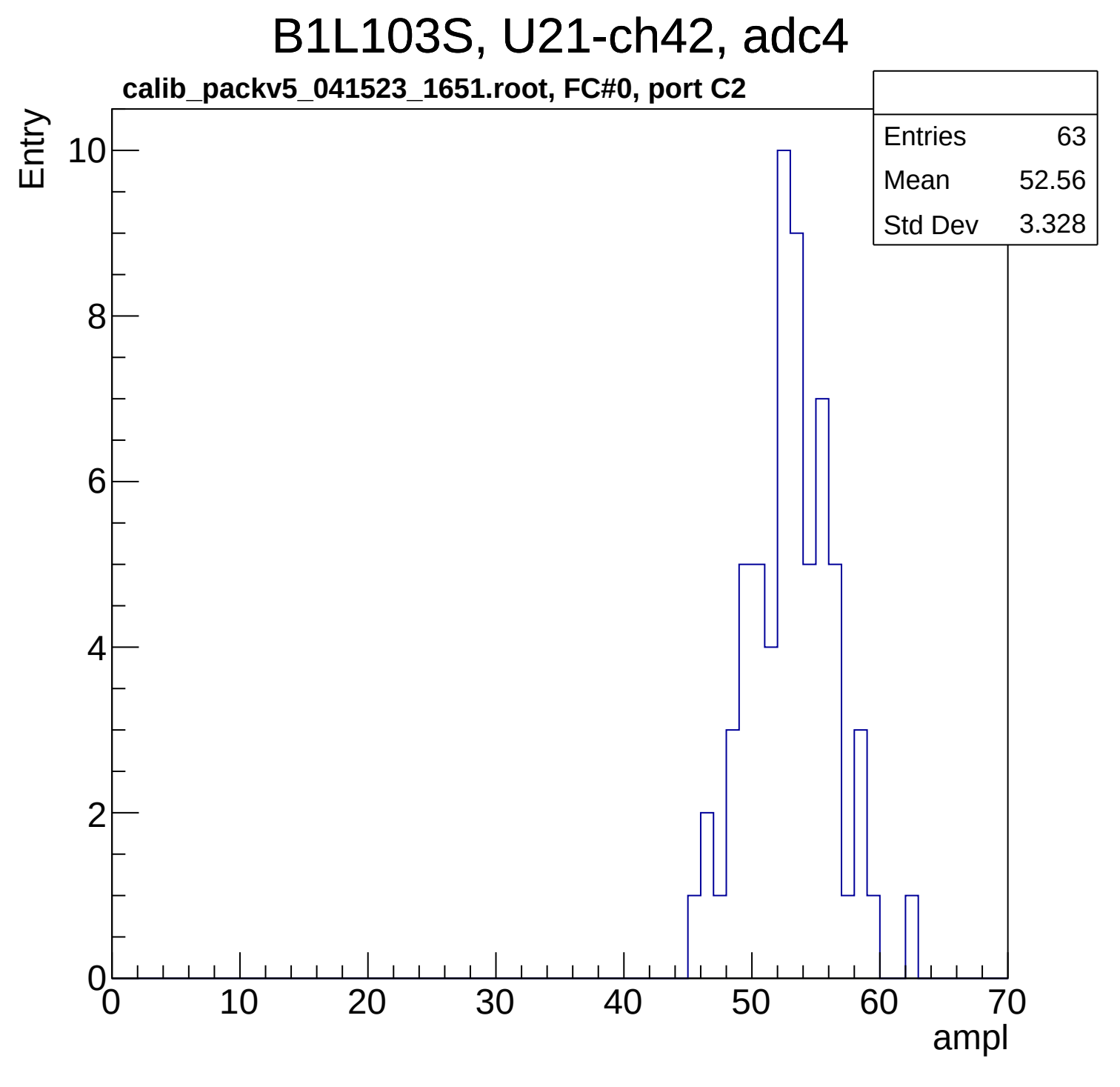
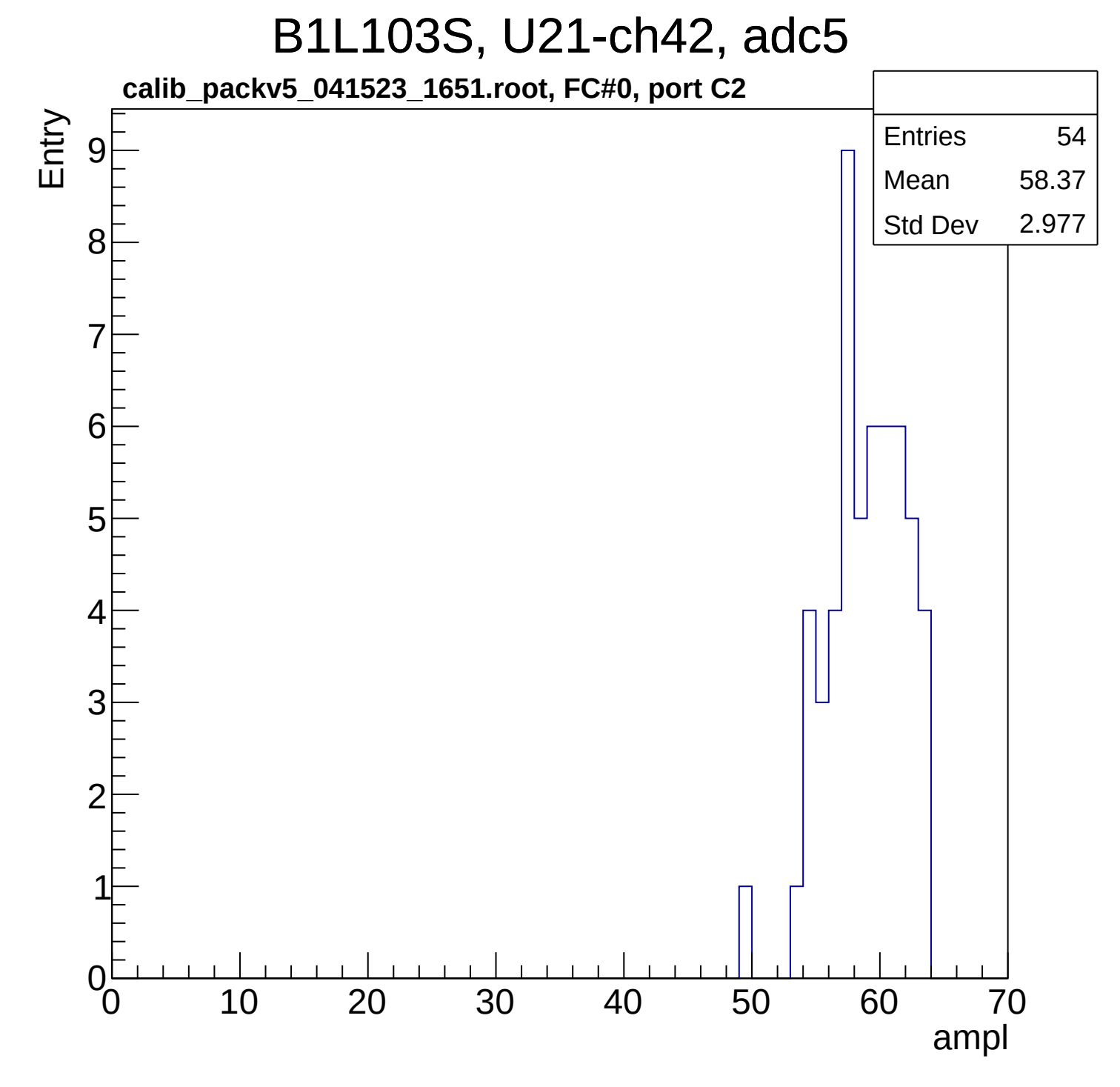
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch42, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 52.56
Std Dev 3.328
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U21-ch42, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 58.37
Std Dev 2.977
Entry
ampl
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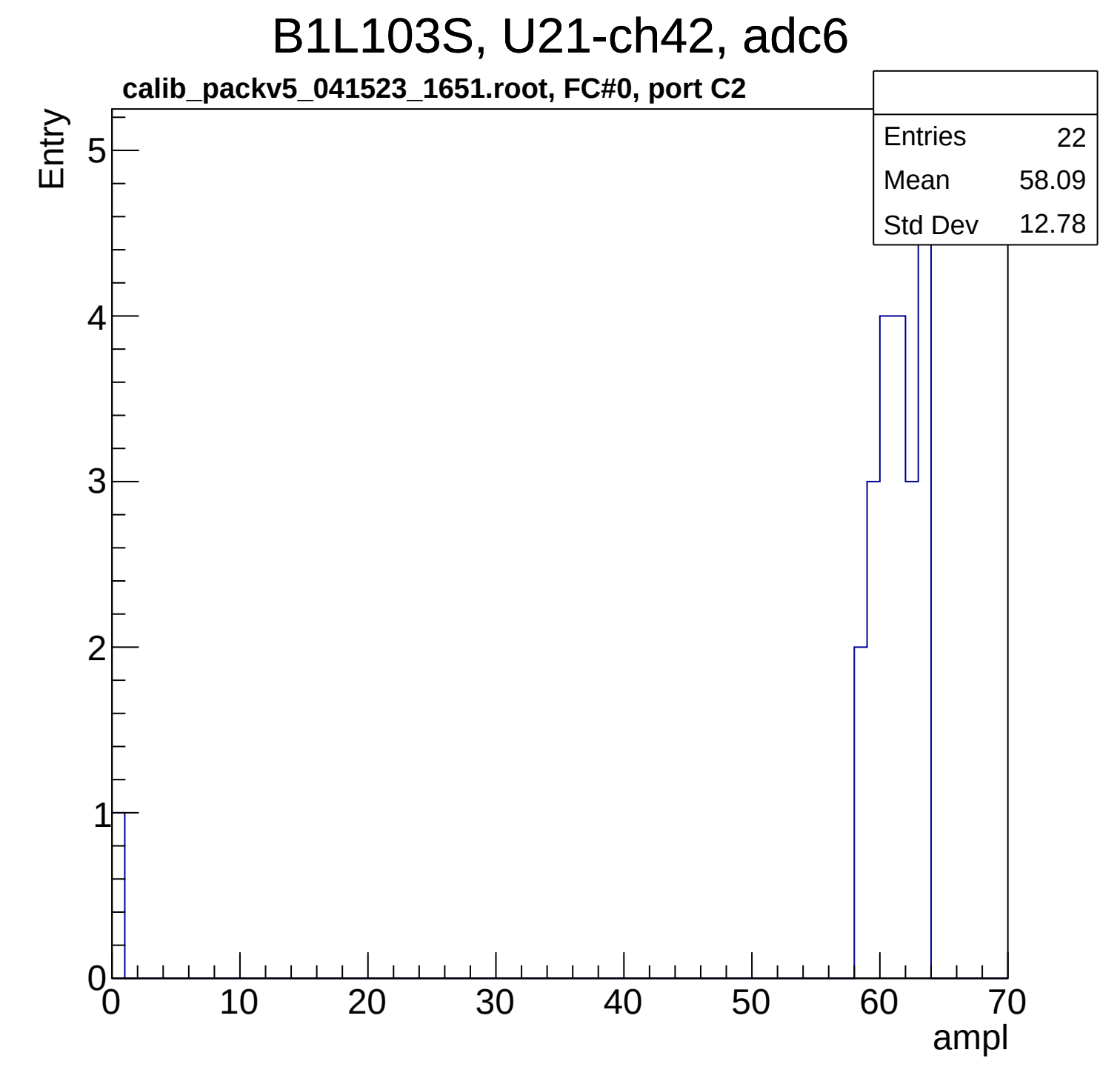
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch42, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 58.09
Std Dev 12.78
Entry
ampl
0
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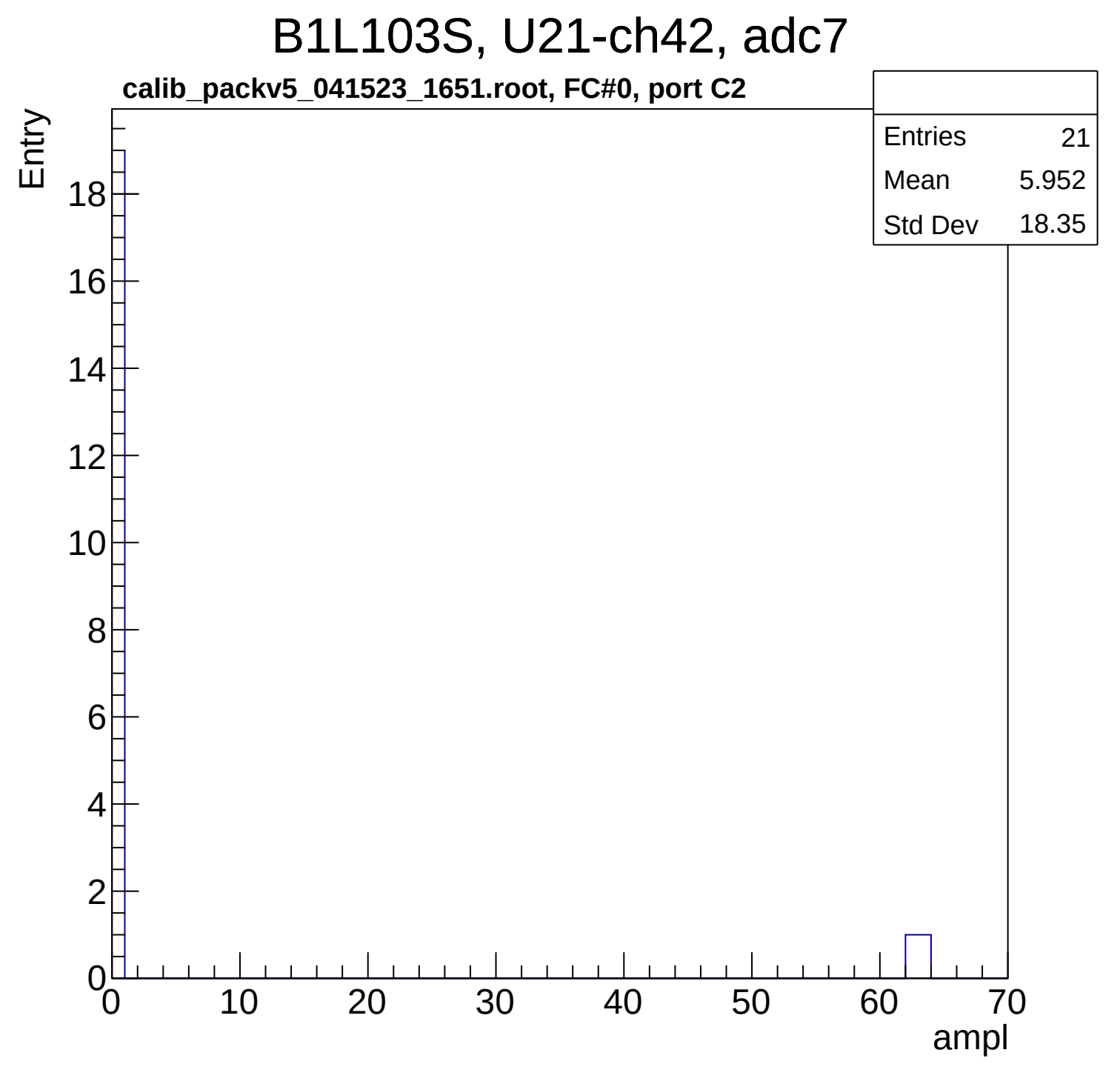
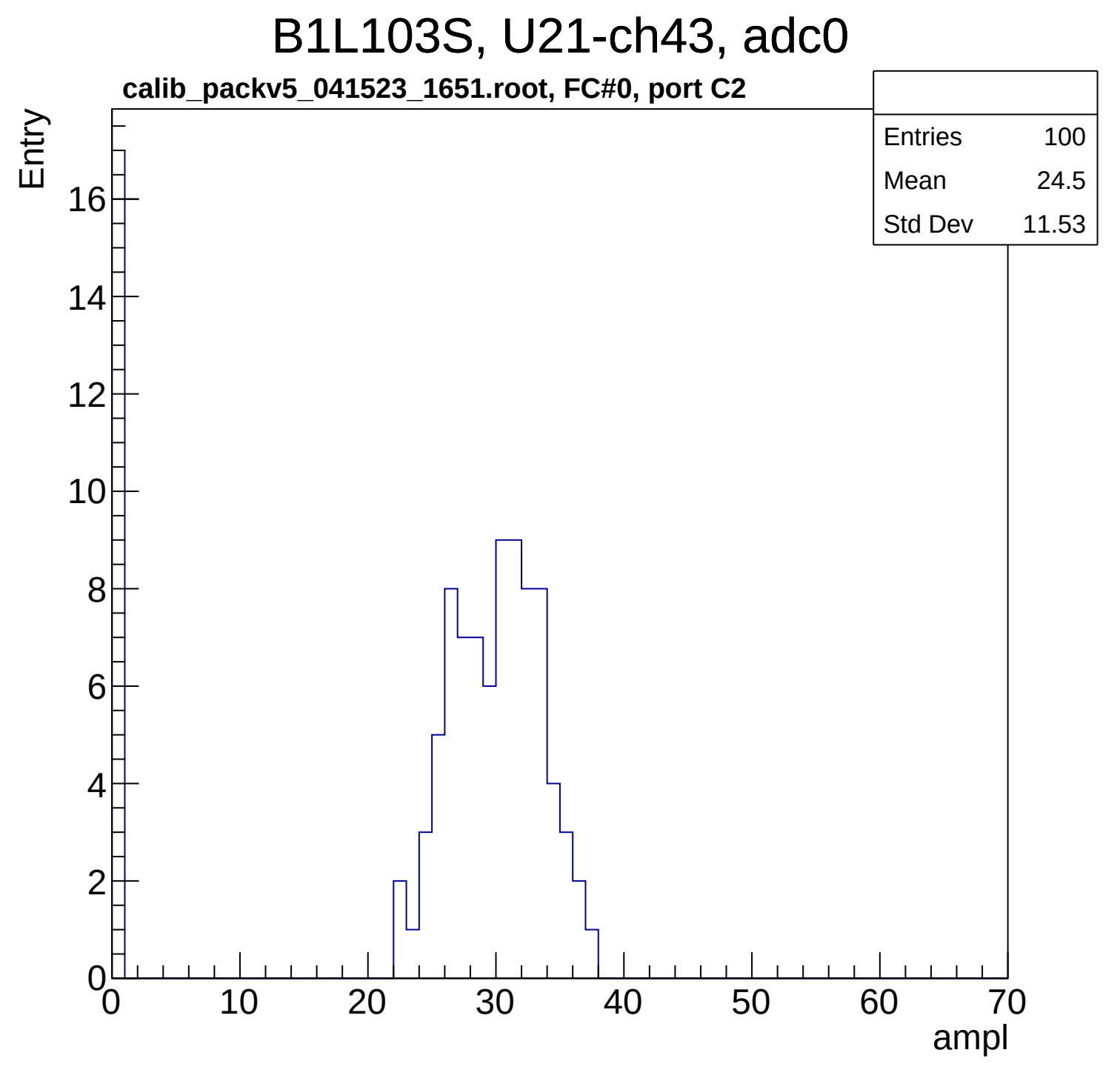
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U21-ch42, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.952
Std Dev 18.35
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch43, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 100
Mean 24.5
Std Dev 11.53
Entry
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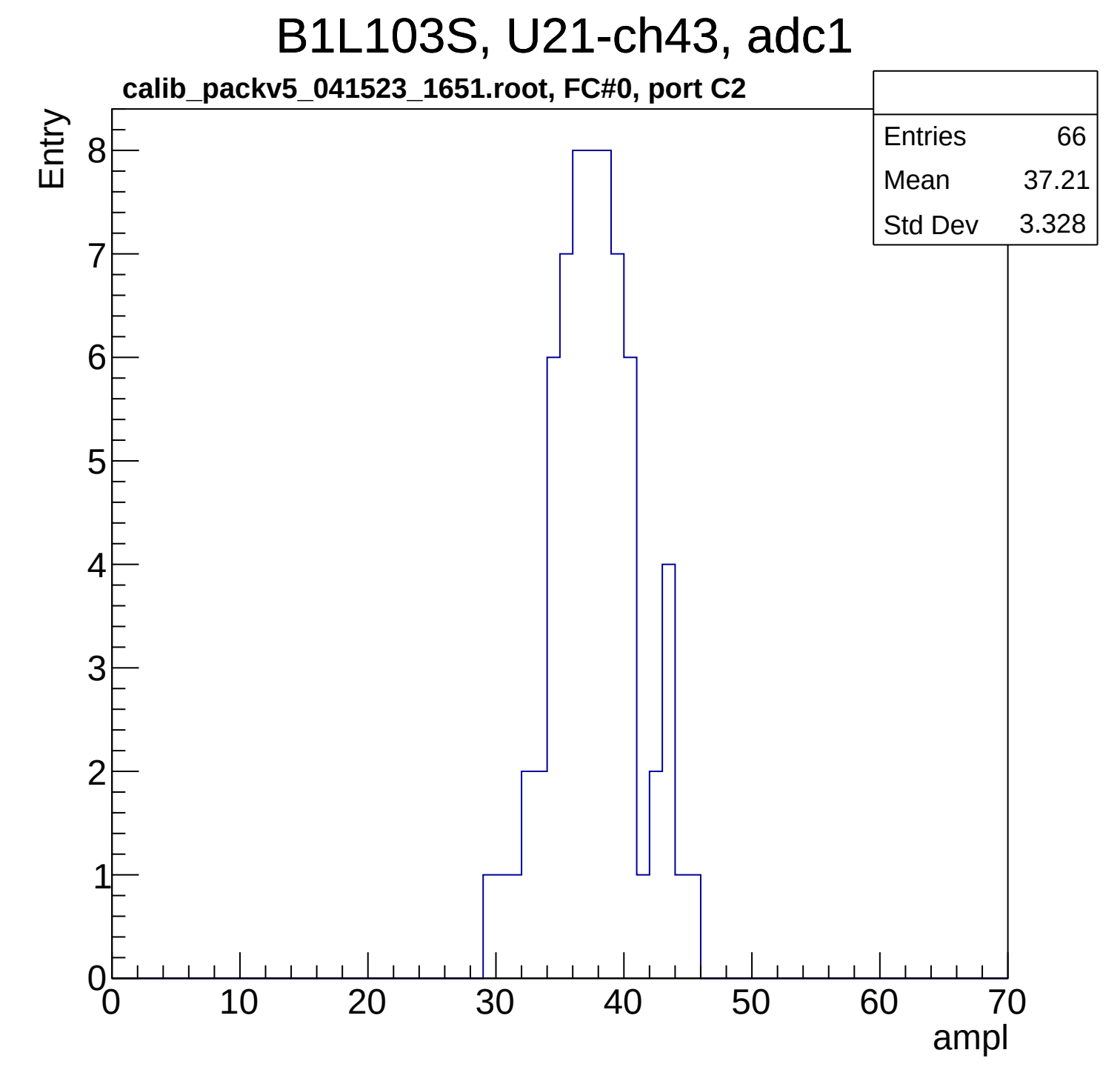
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch43, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 37.21
Std Dev 3.328
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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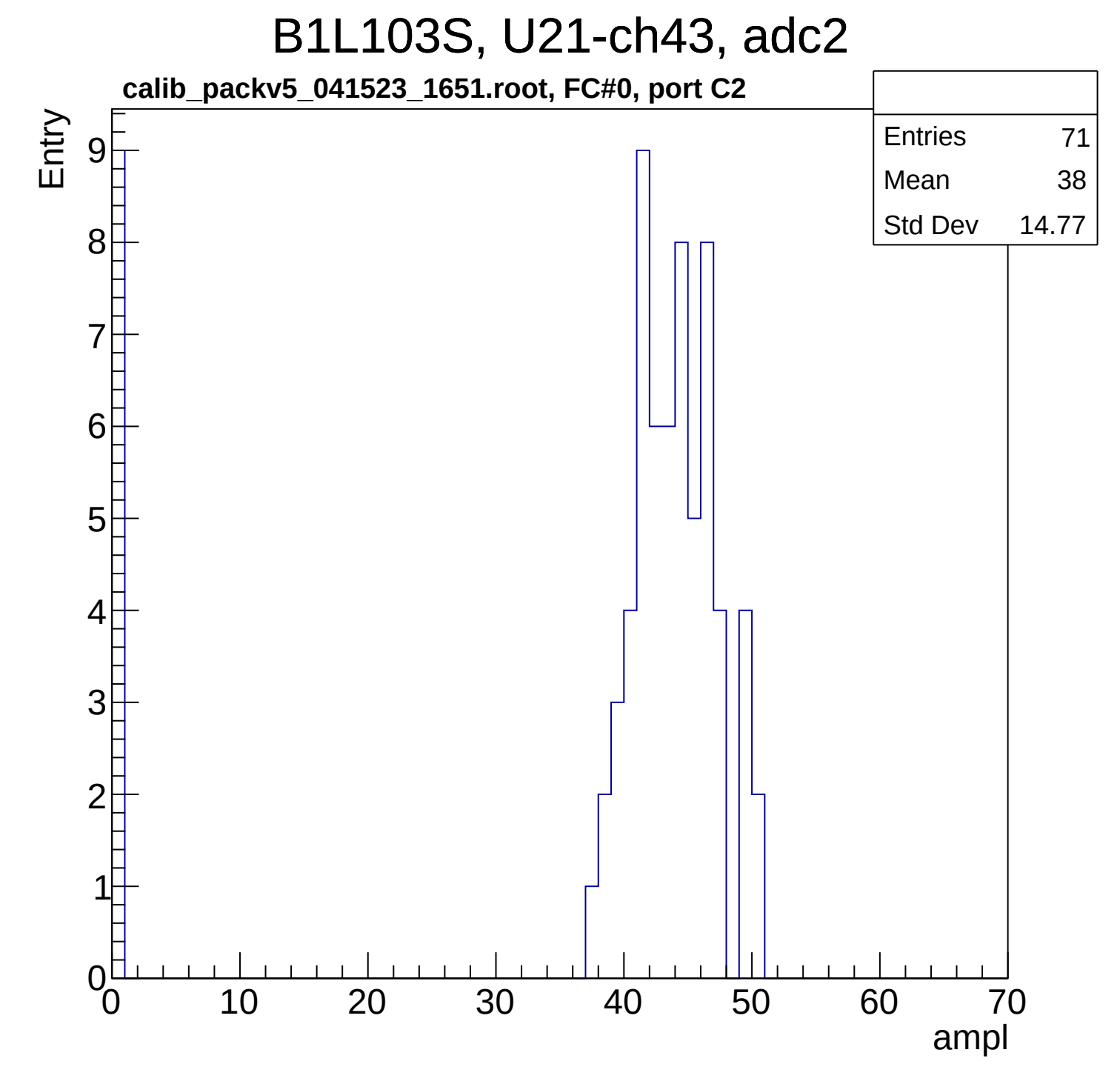
B1L103S, U21-ch43, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 38
Std Dev 14.77
Entry
ampl
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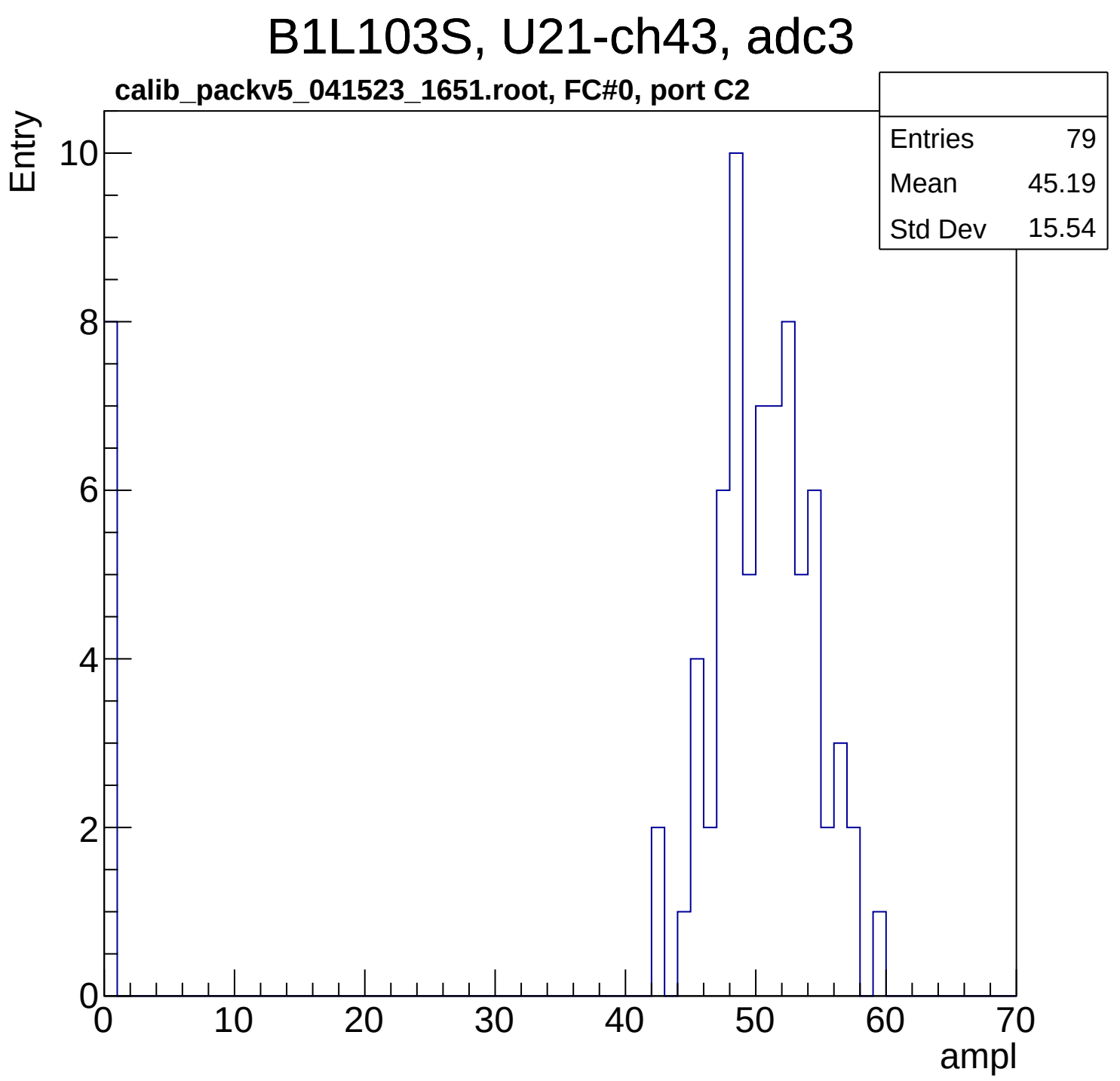
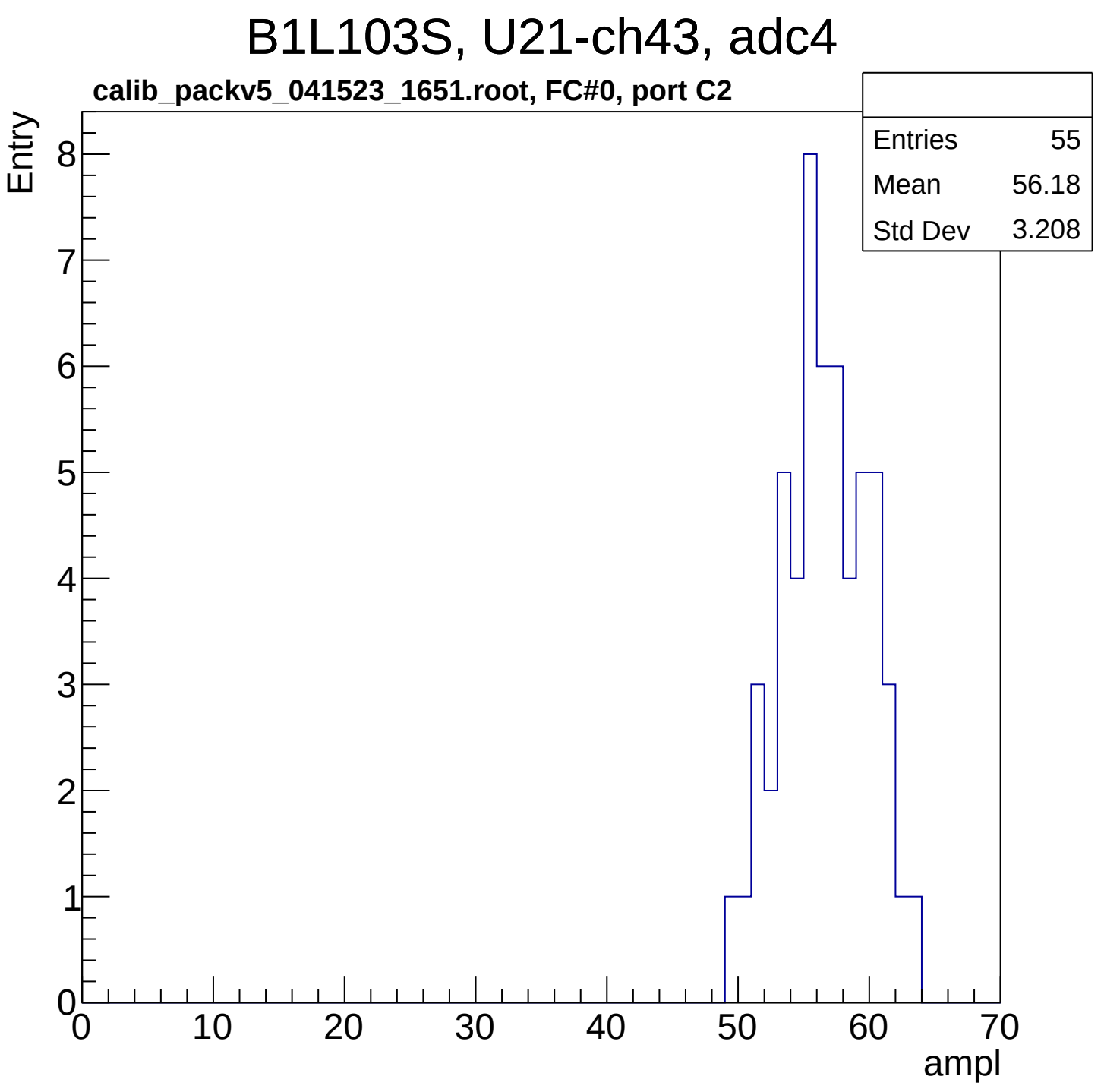
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch43, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 45.19
Std Dev 15.54
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U21-ch43, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 56.18
Std Dev 3.208
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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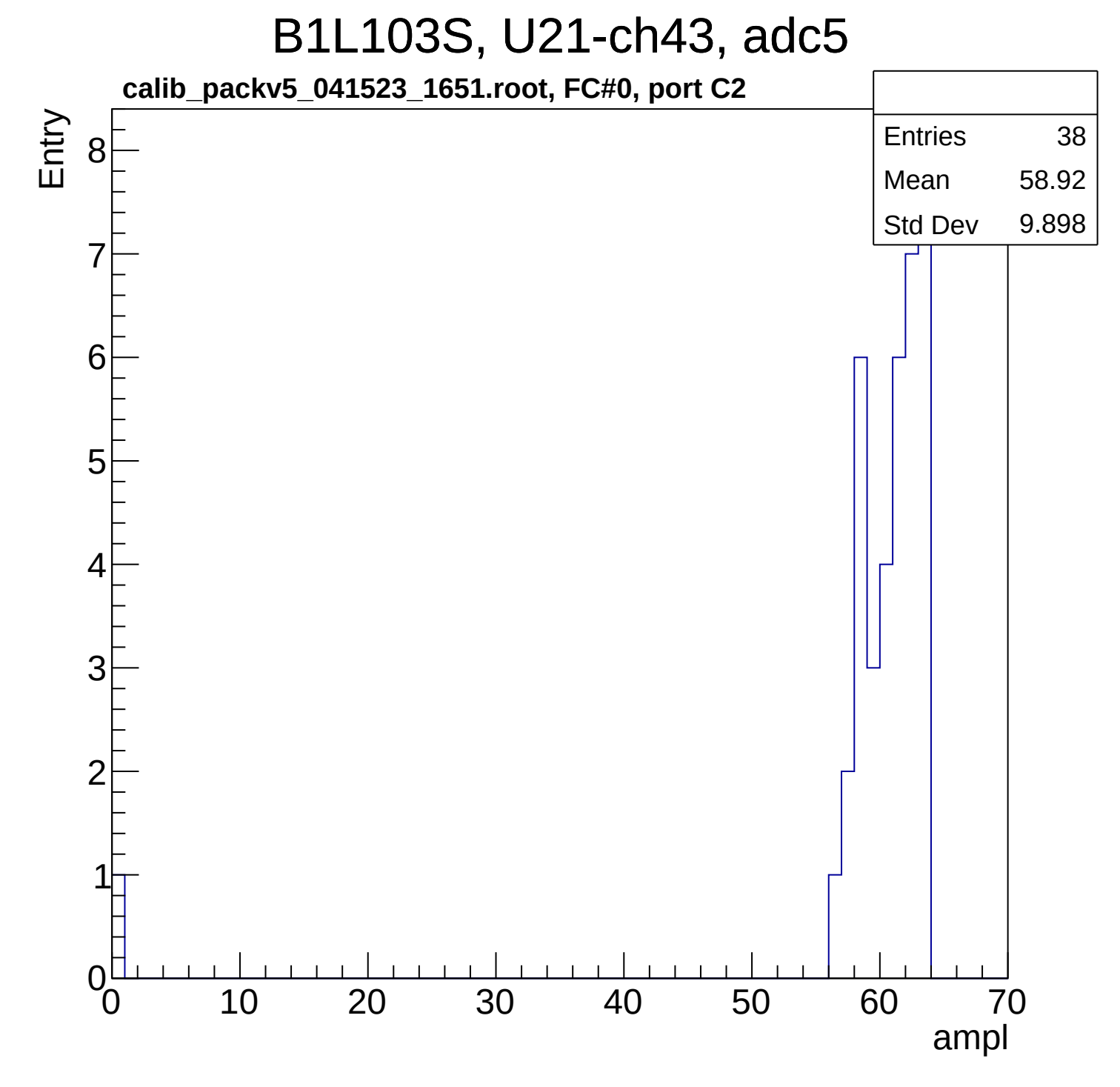
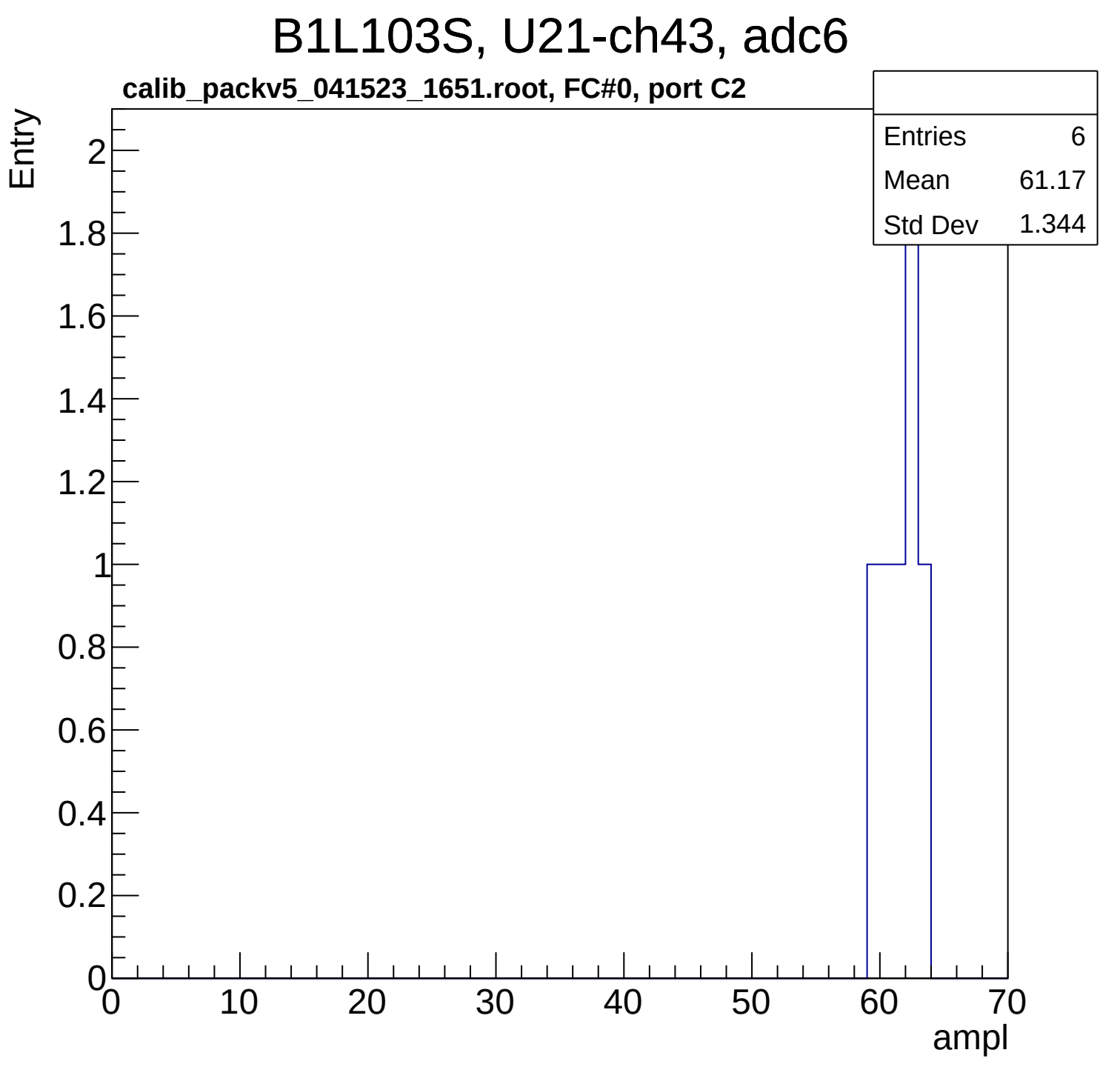
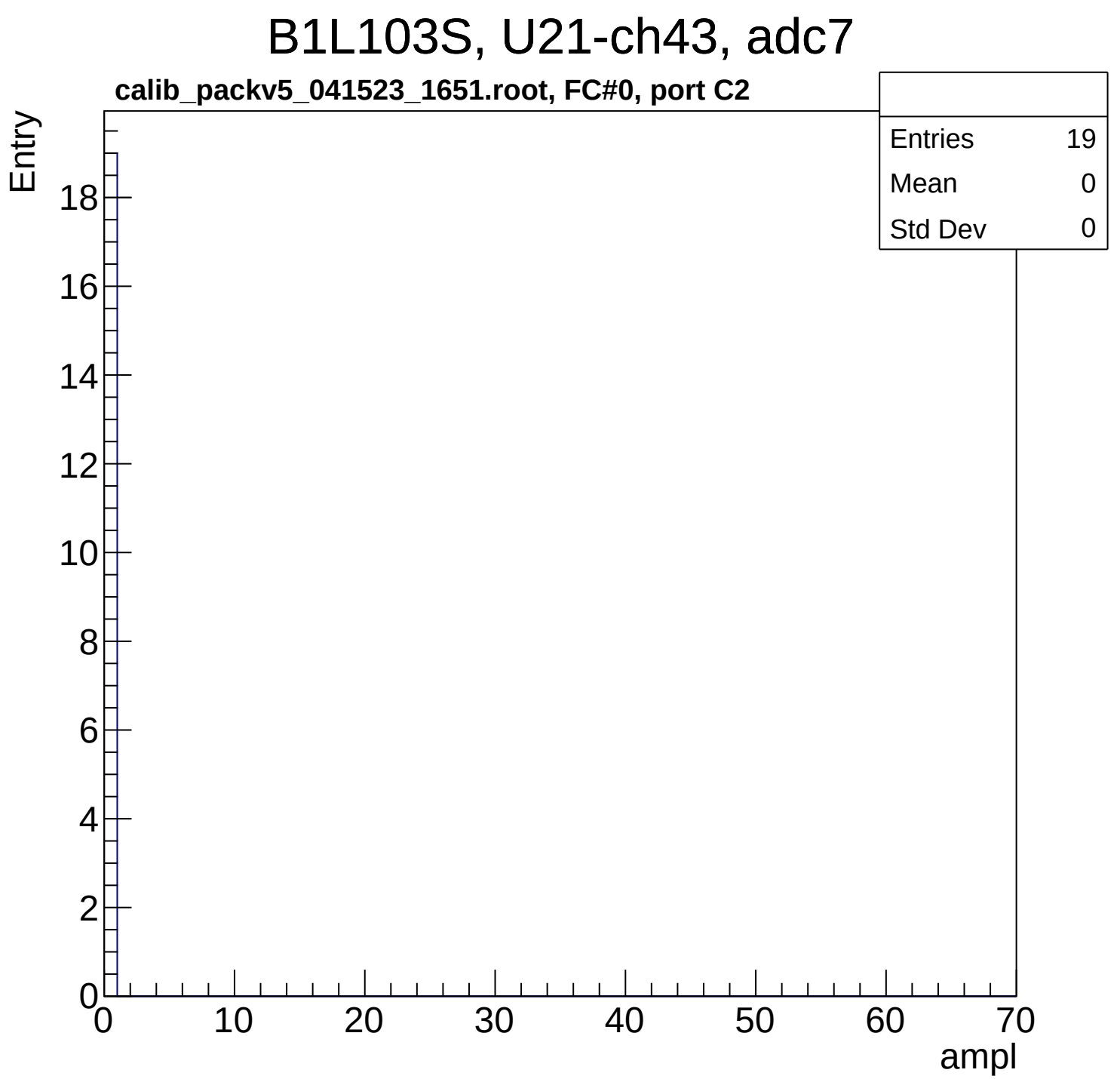
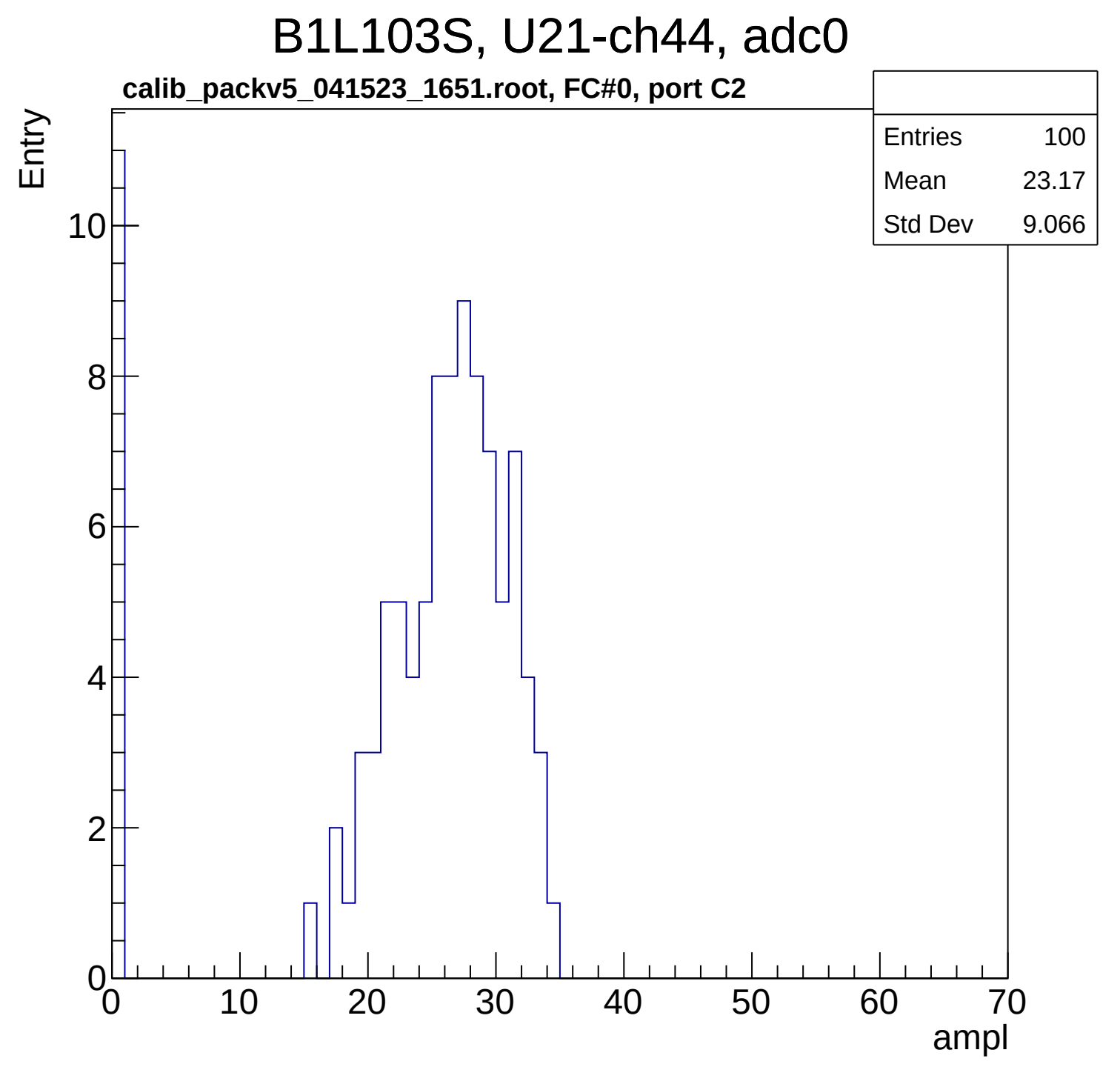
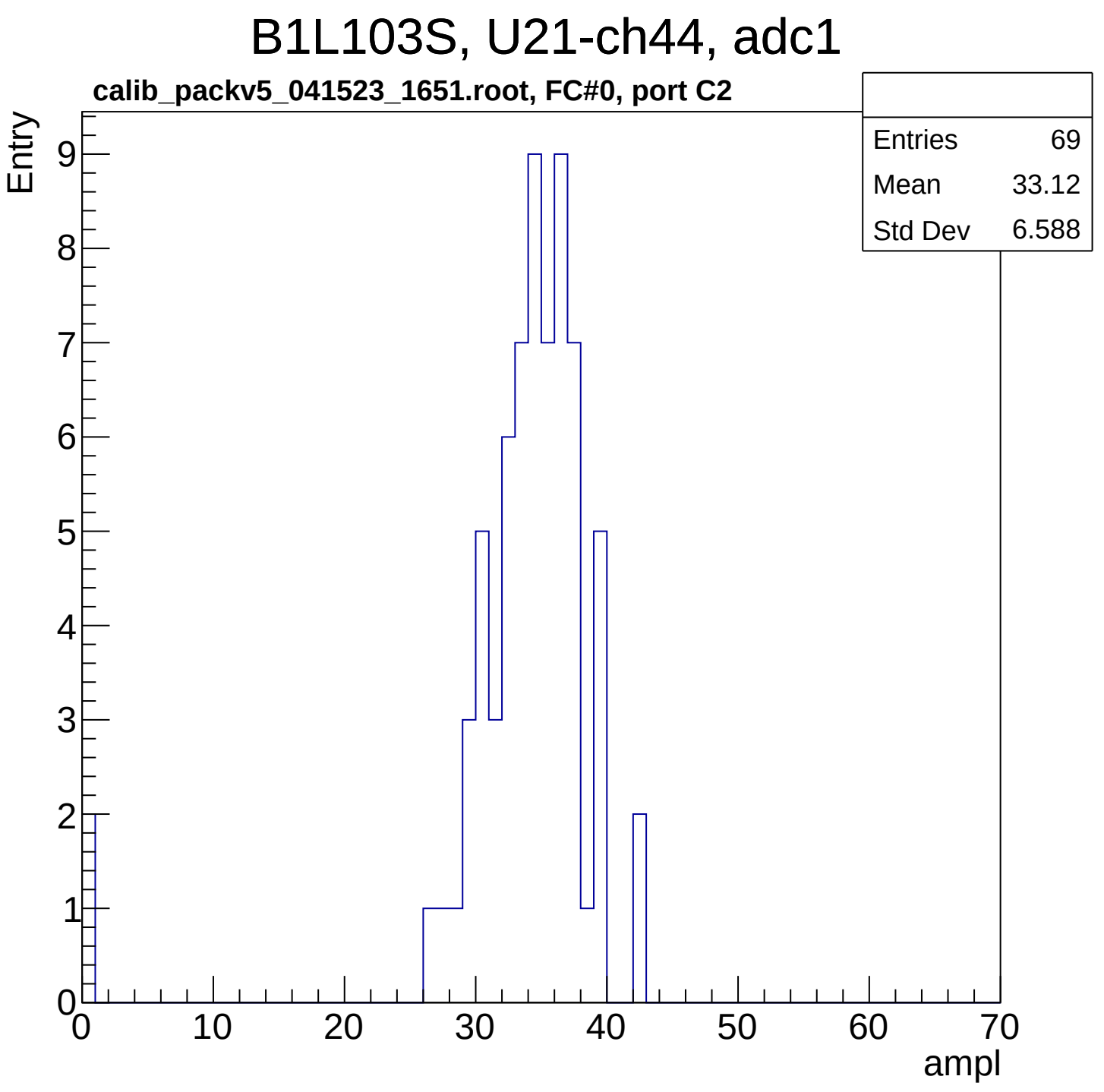
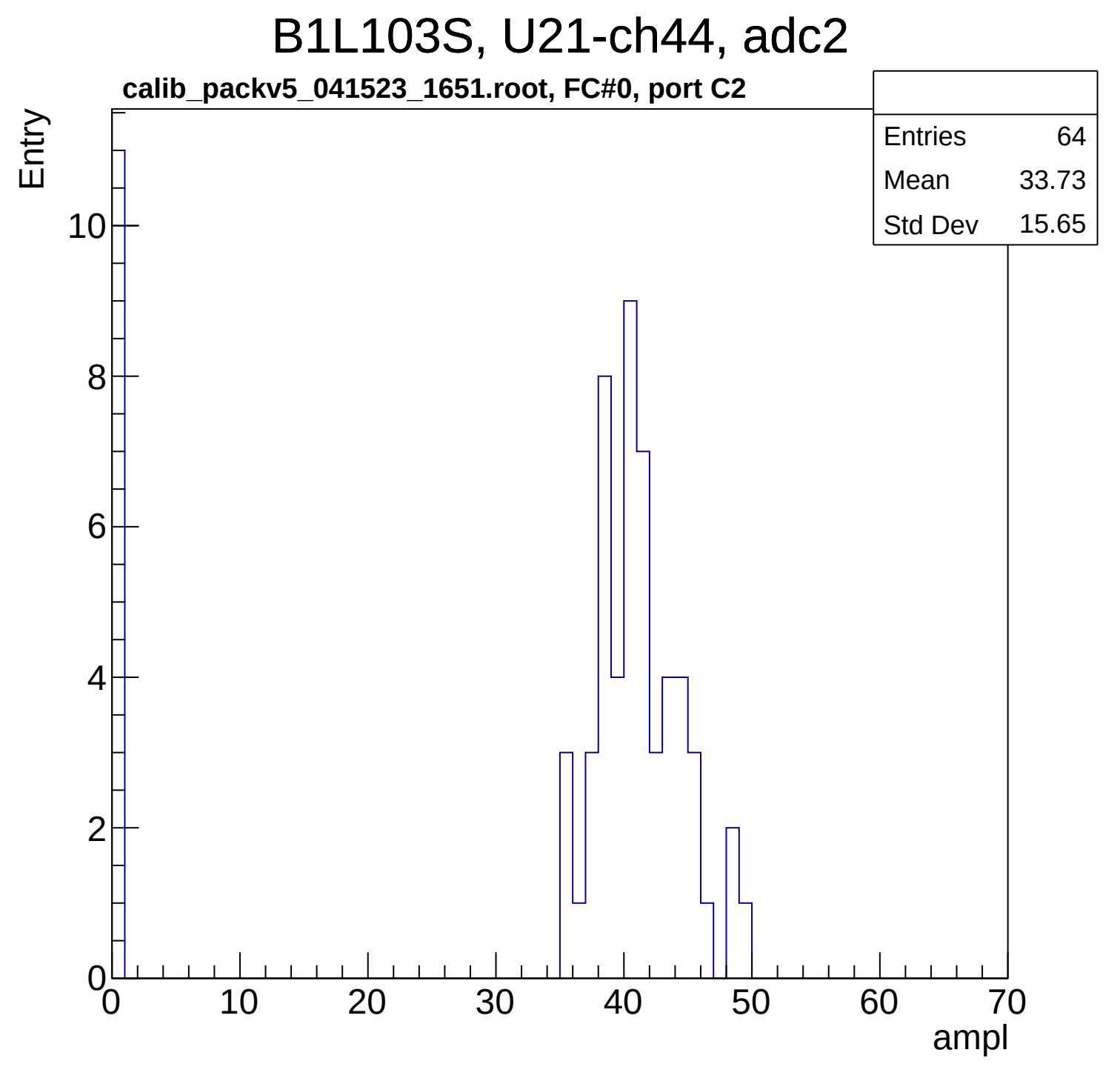

B1L103S, U21-ch43, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 58.92
Std Dev 9.898
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

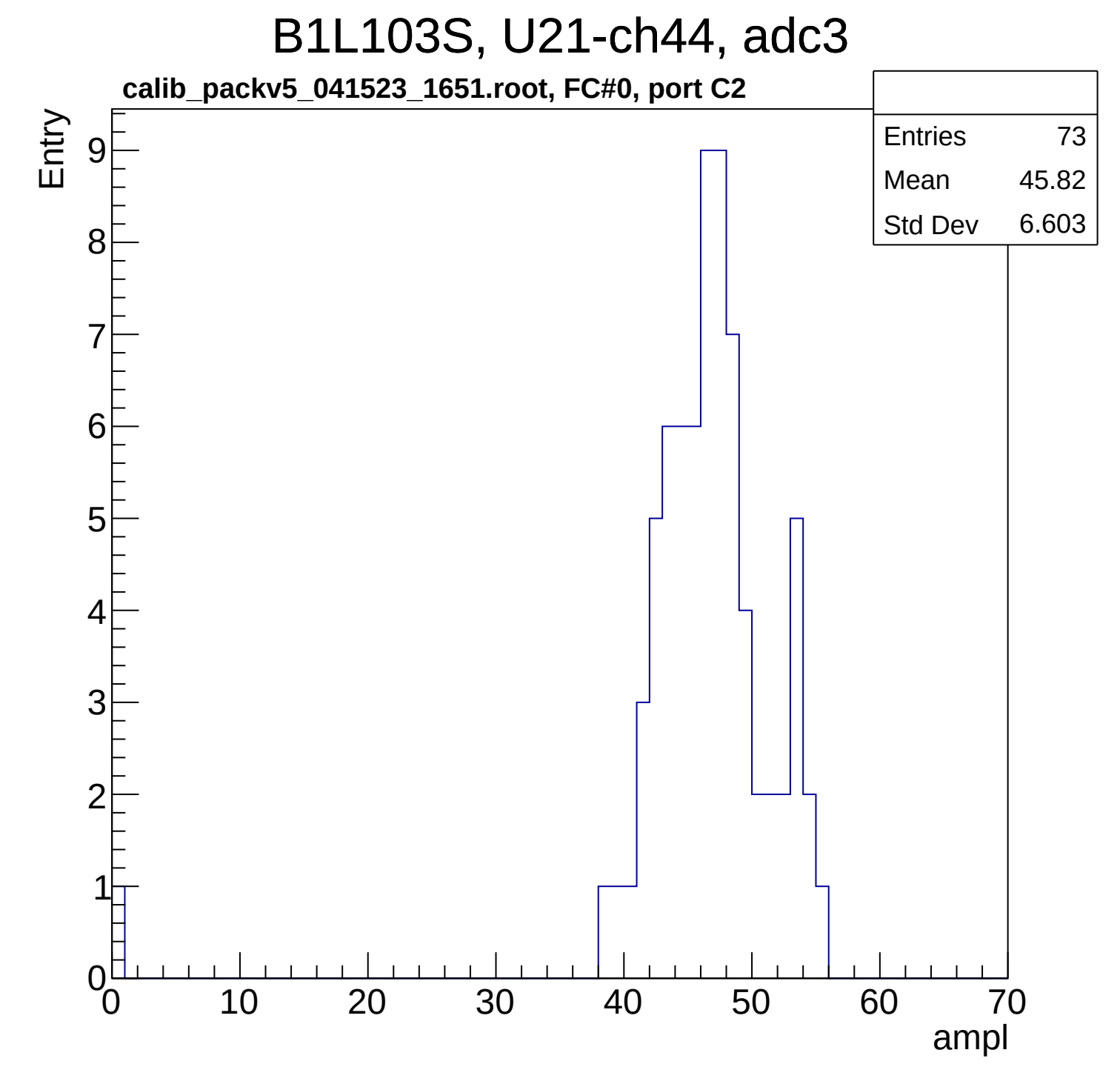

B1L103S, U21-ch43, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 61.17
Std Dev 1.344
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

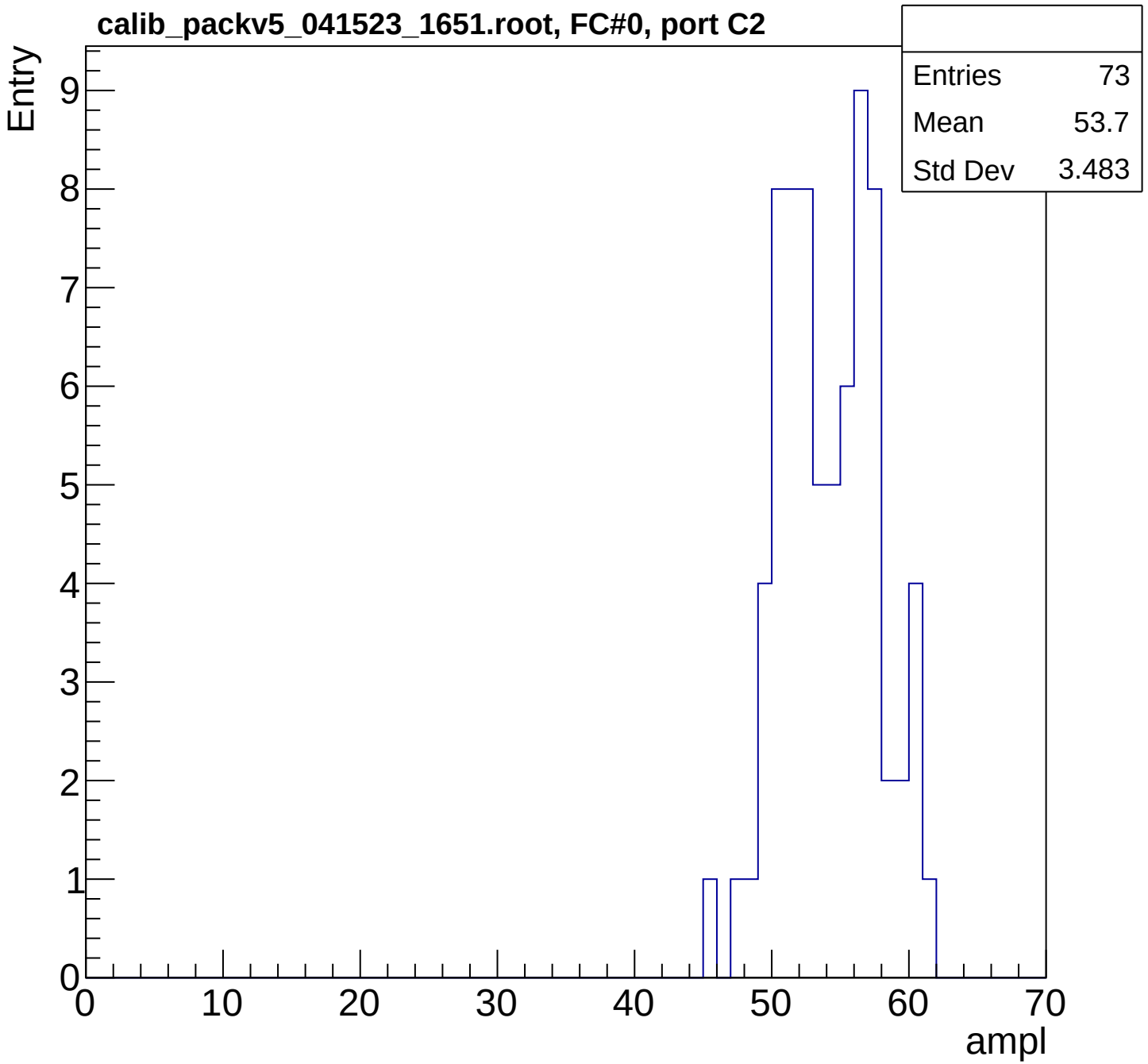

B1L103S, U21-ch43, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

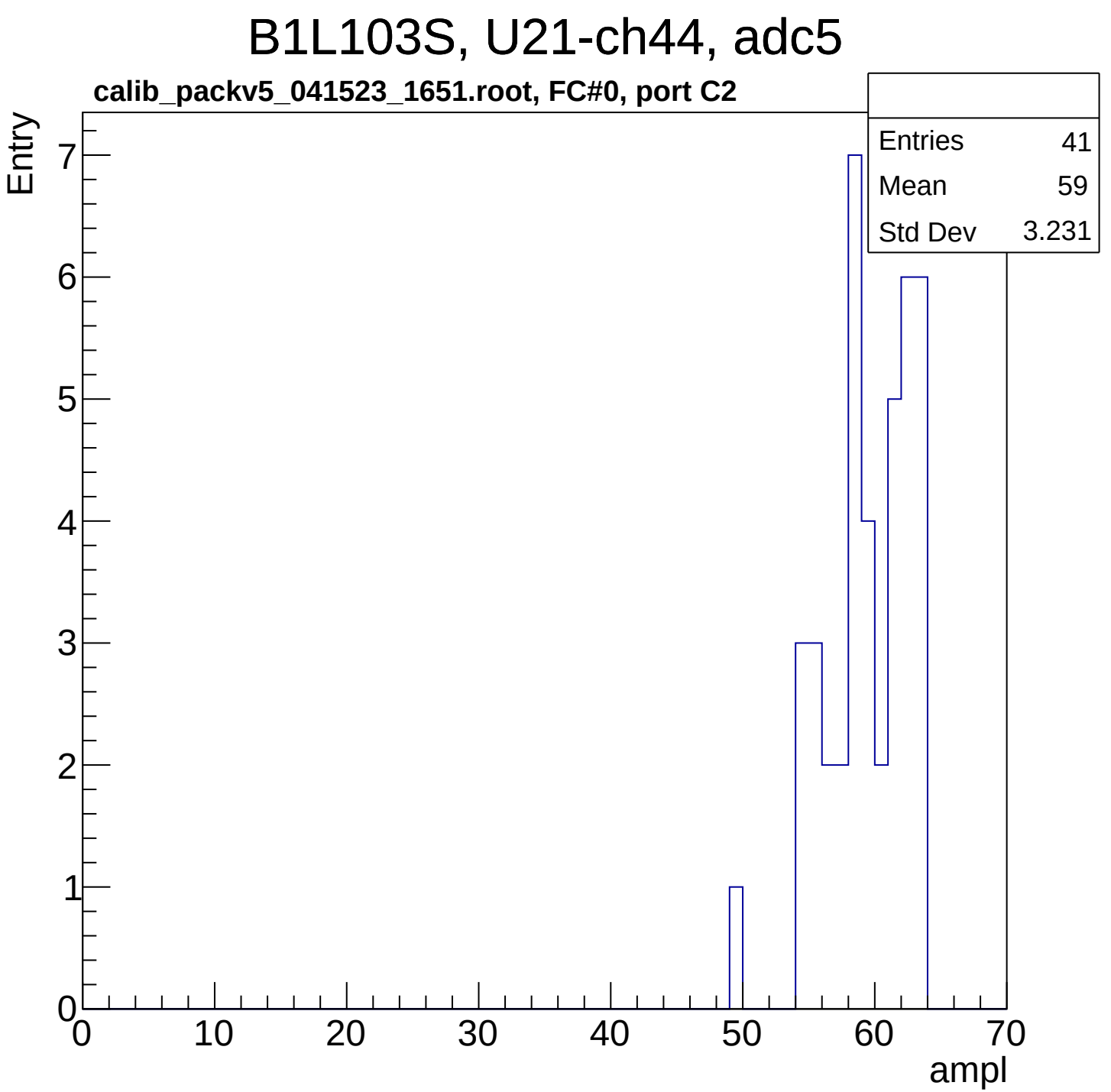

B1L103S, U21-ch44, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 100
Mean 23.17
Std Dev 9.066
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

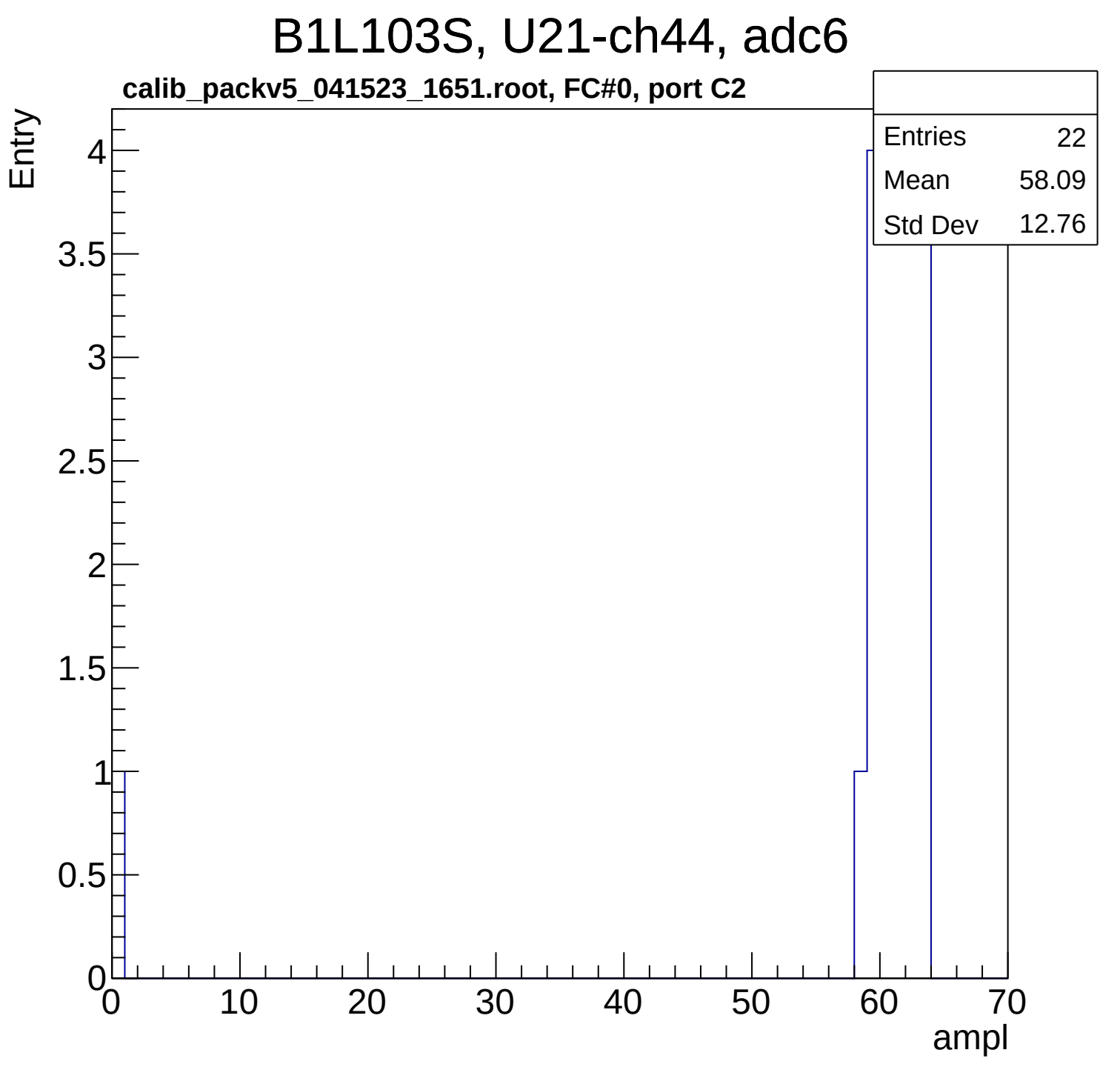

B1L103S, U21-ch44, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 33.12
Std Dev 6.588
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

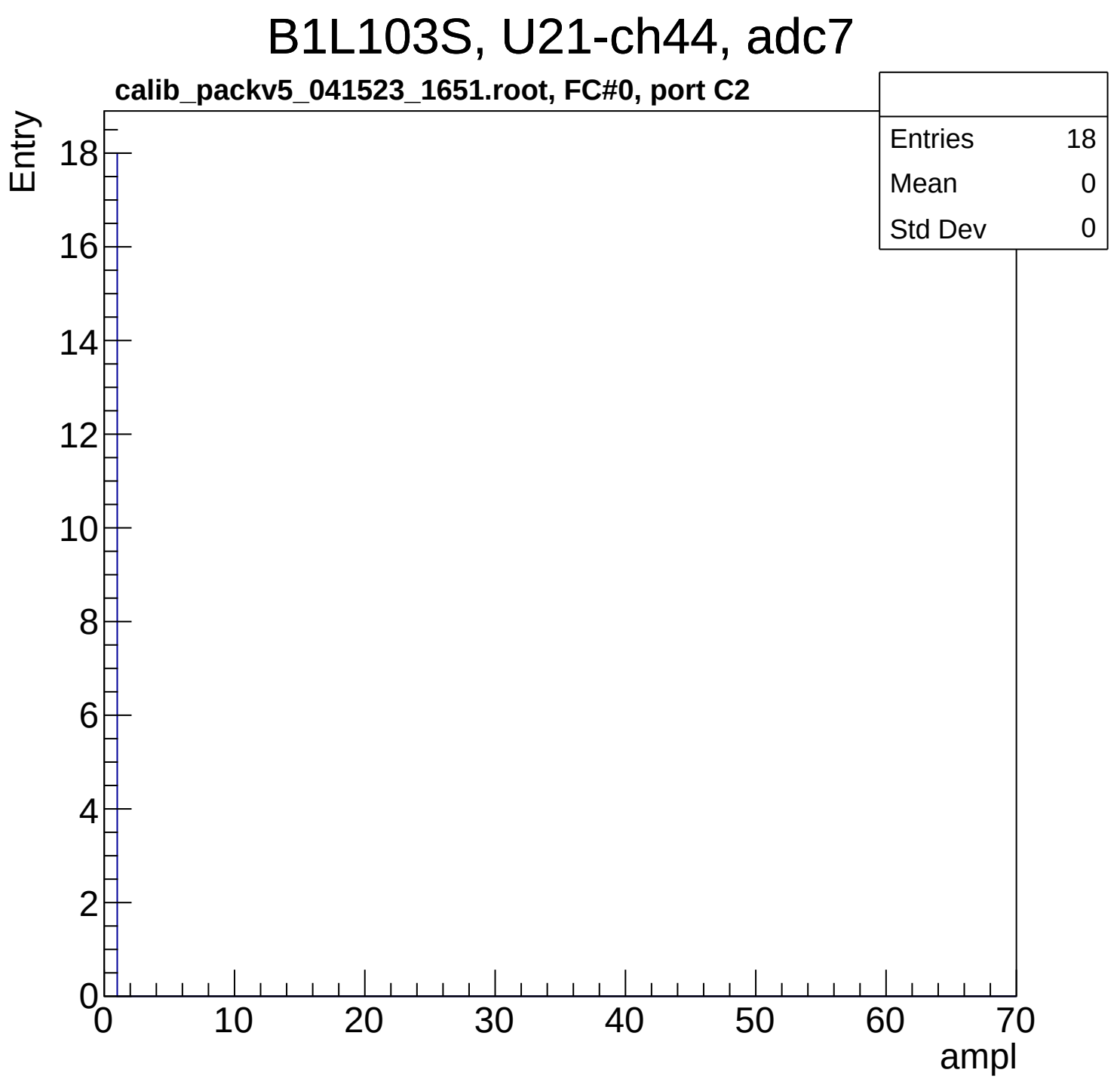

B1L103S, U21-ch44, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 33.73
Std Dev 15.65
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

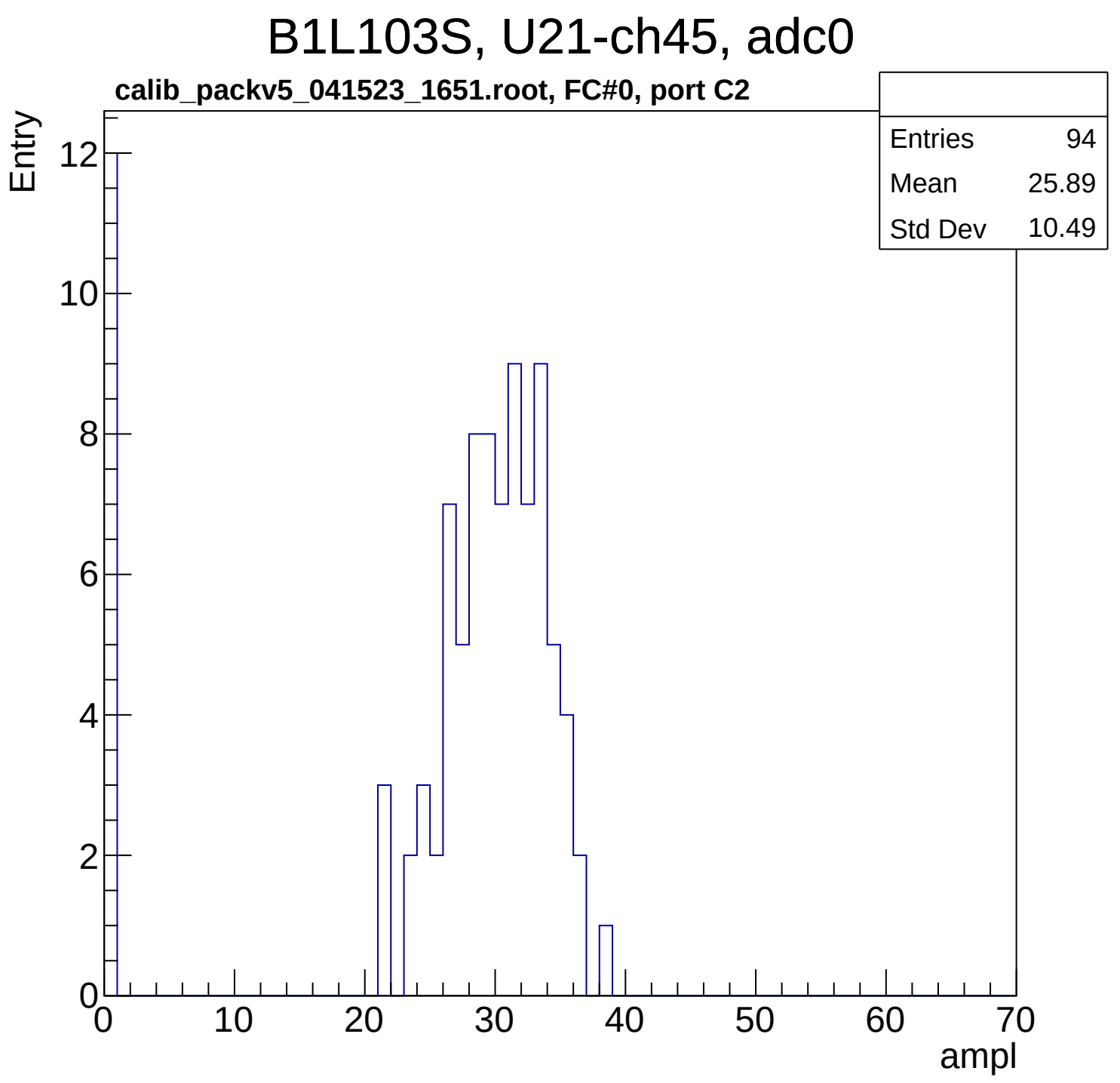

B1L103S, U21-ch44, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 45.82
Std Dev 6.603
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

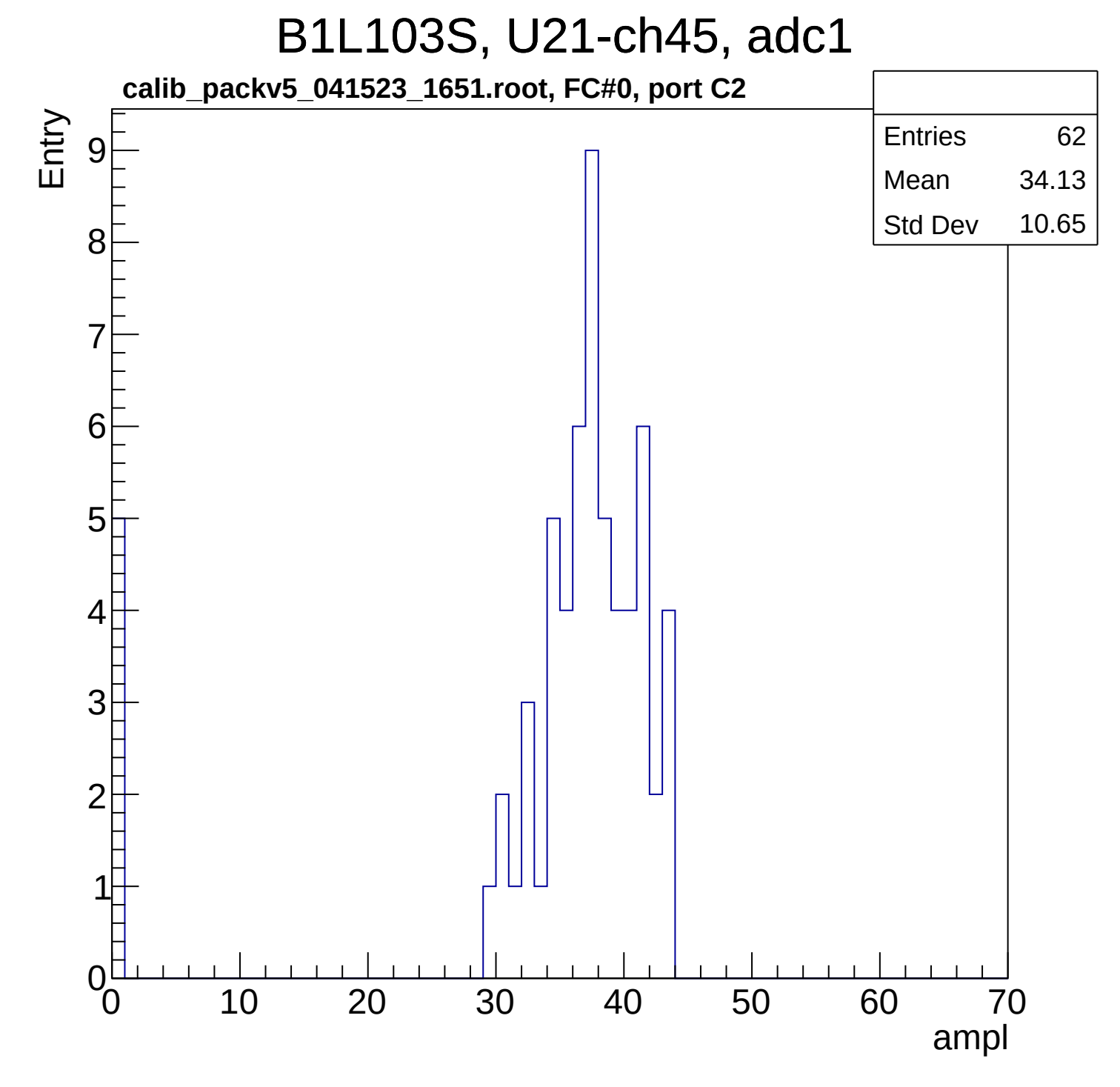

B1L103S, U21-ch44, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 53.7
Std Dev 3.483
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

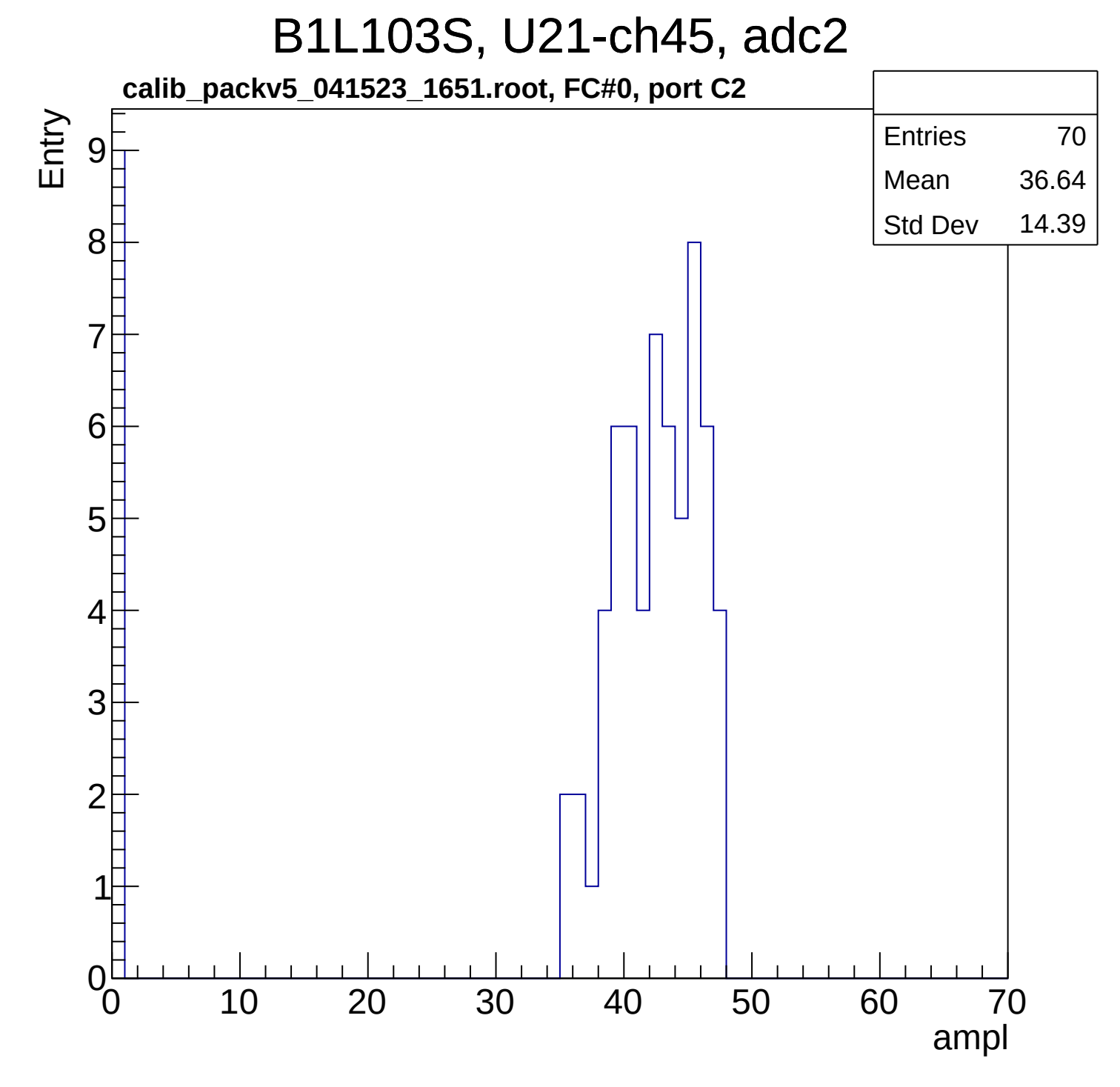

B1L103S, U21-ch44, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 59
Std Dev 3.231
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U21-ch44, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 58.09
Std Dev 12.76
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U21-ch44, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch45, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 25.89
Std Dev 10.49
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch45, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 34.13
Std Dev 10.65
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch45, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 36.64
Std Dev 14.39
Entry
ampl
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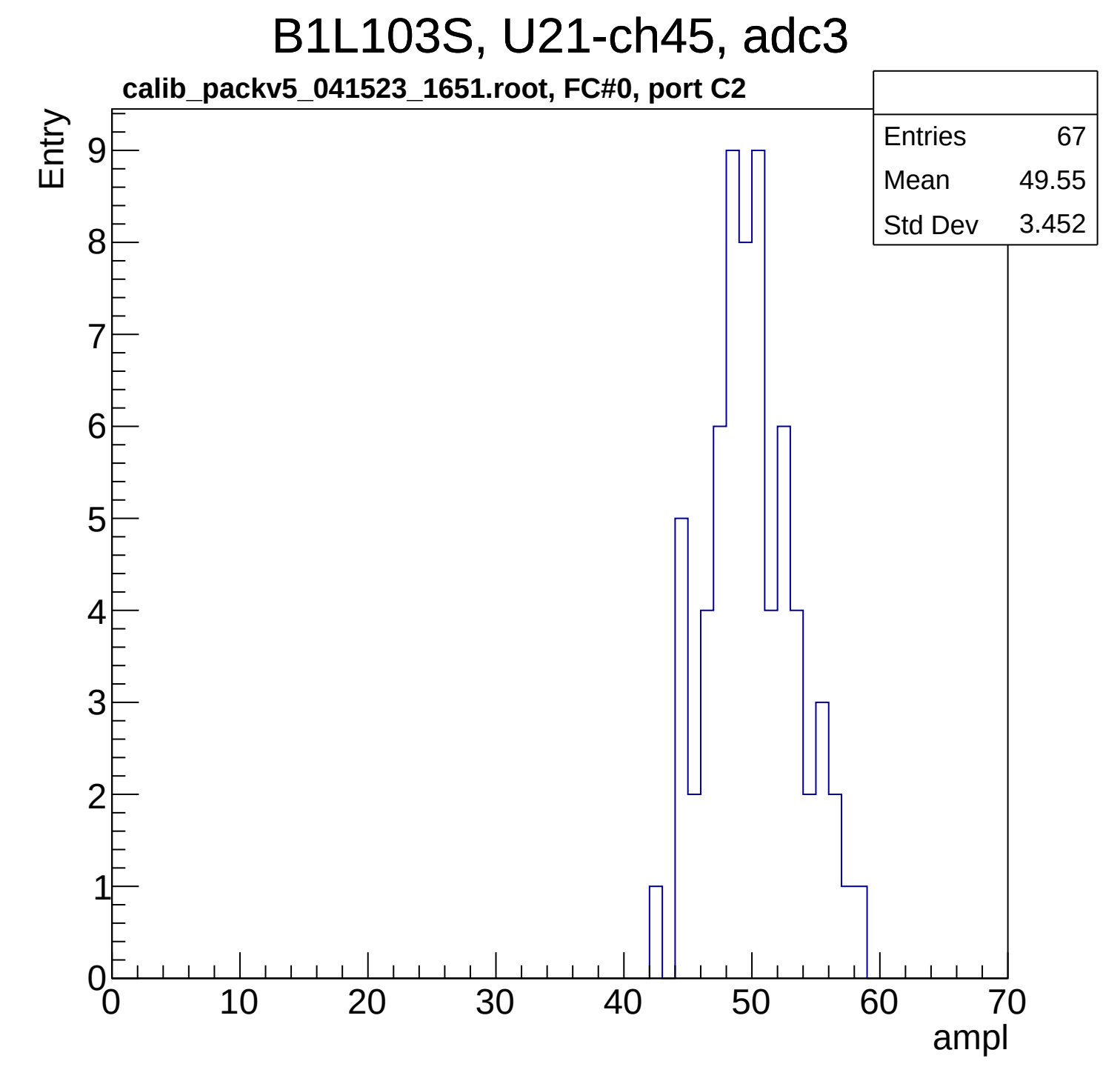
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch45, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 49.55
Std Dev 3.452
Entry
ampl
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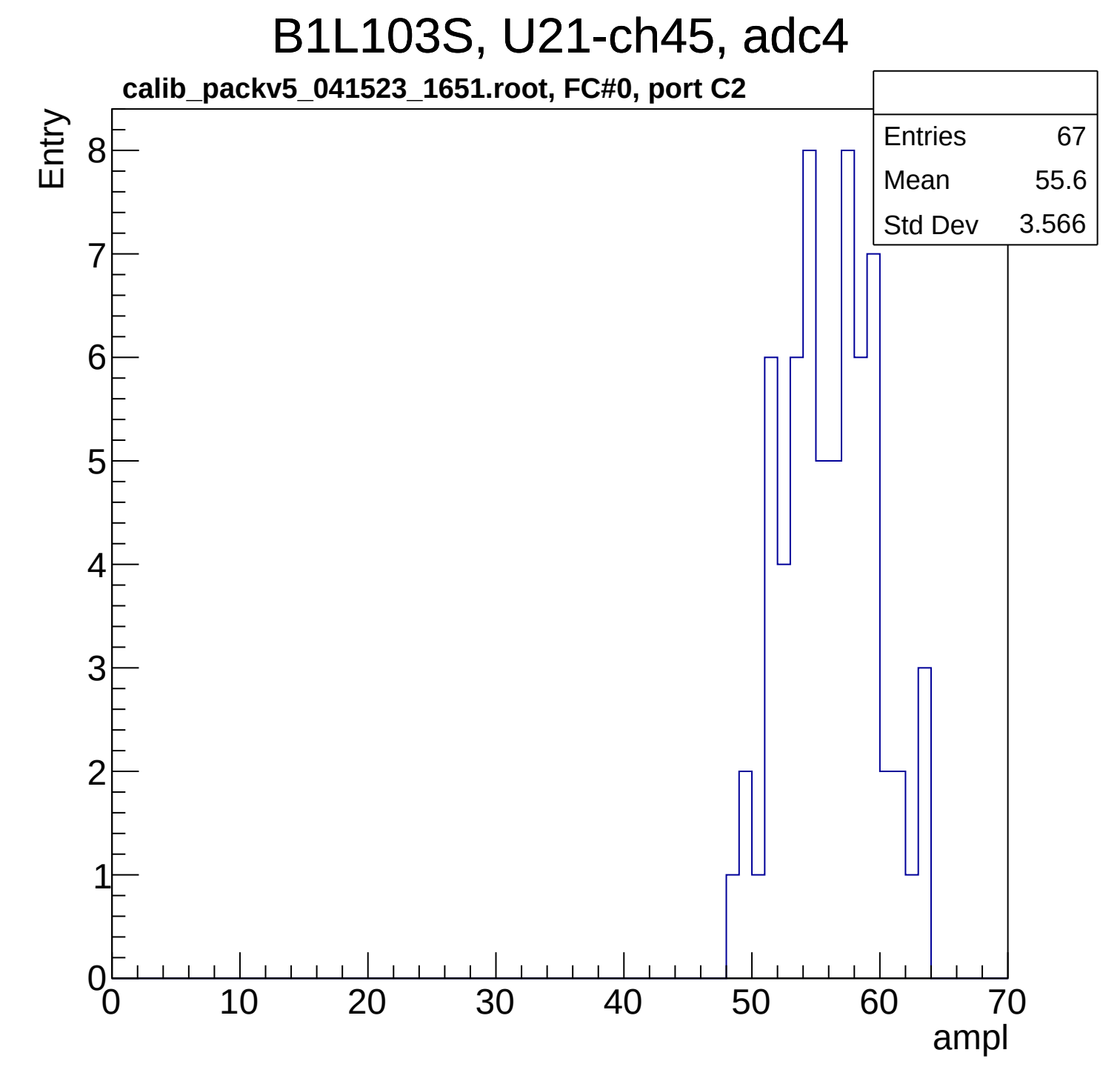
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch45, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 55.6
Std Dev 3.566
Entry
ampl
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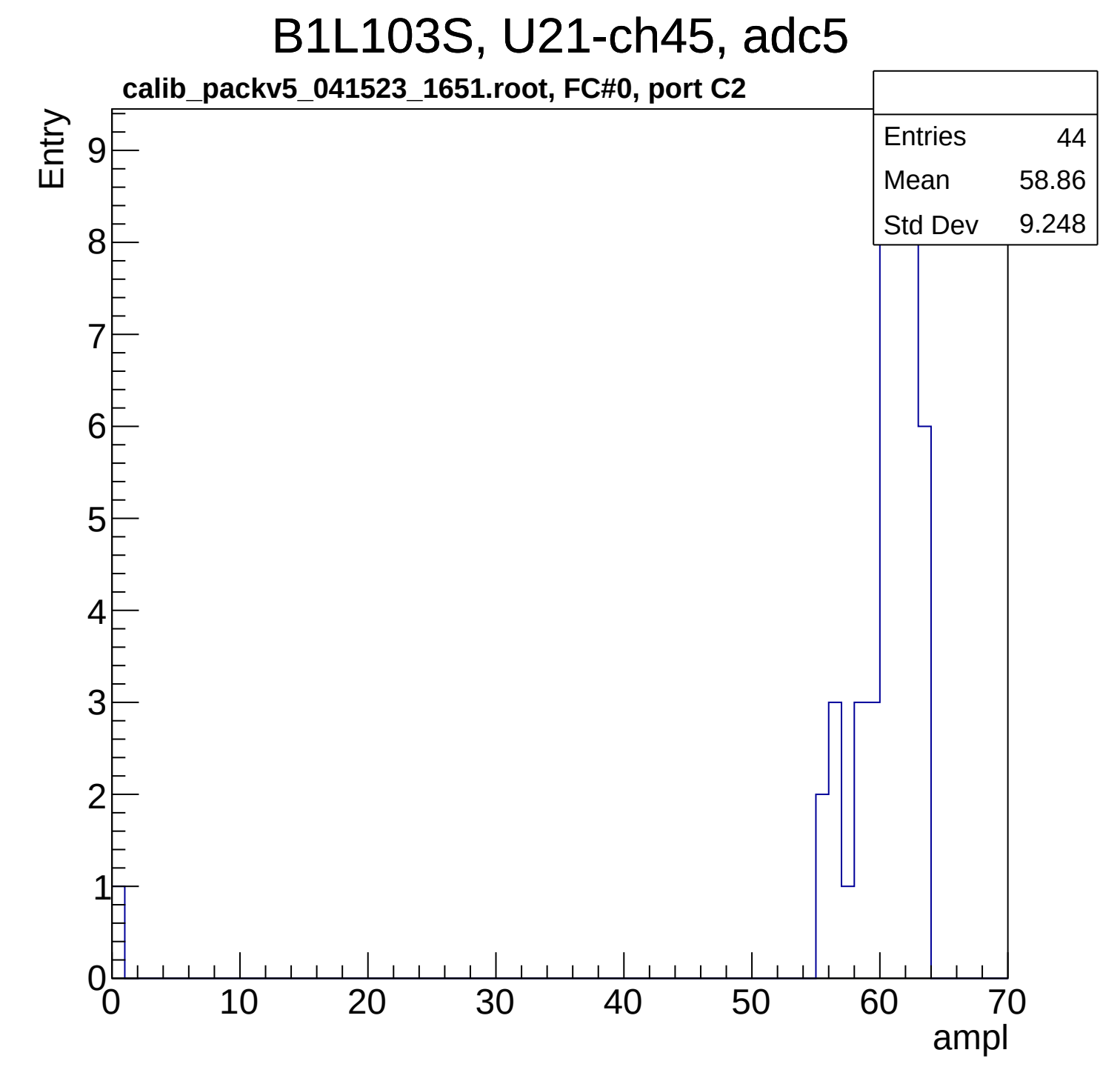
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch45, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 58.86
Std Dev 9.248
Entry
ampl
0
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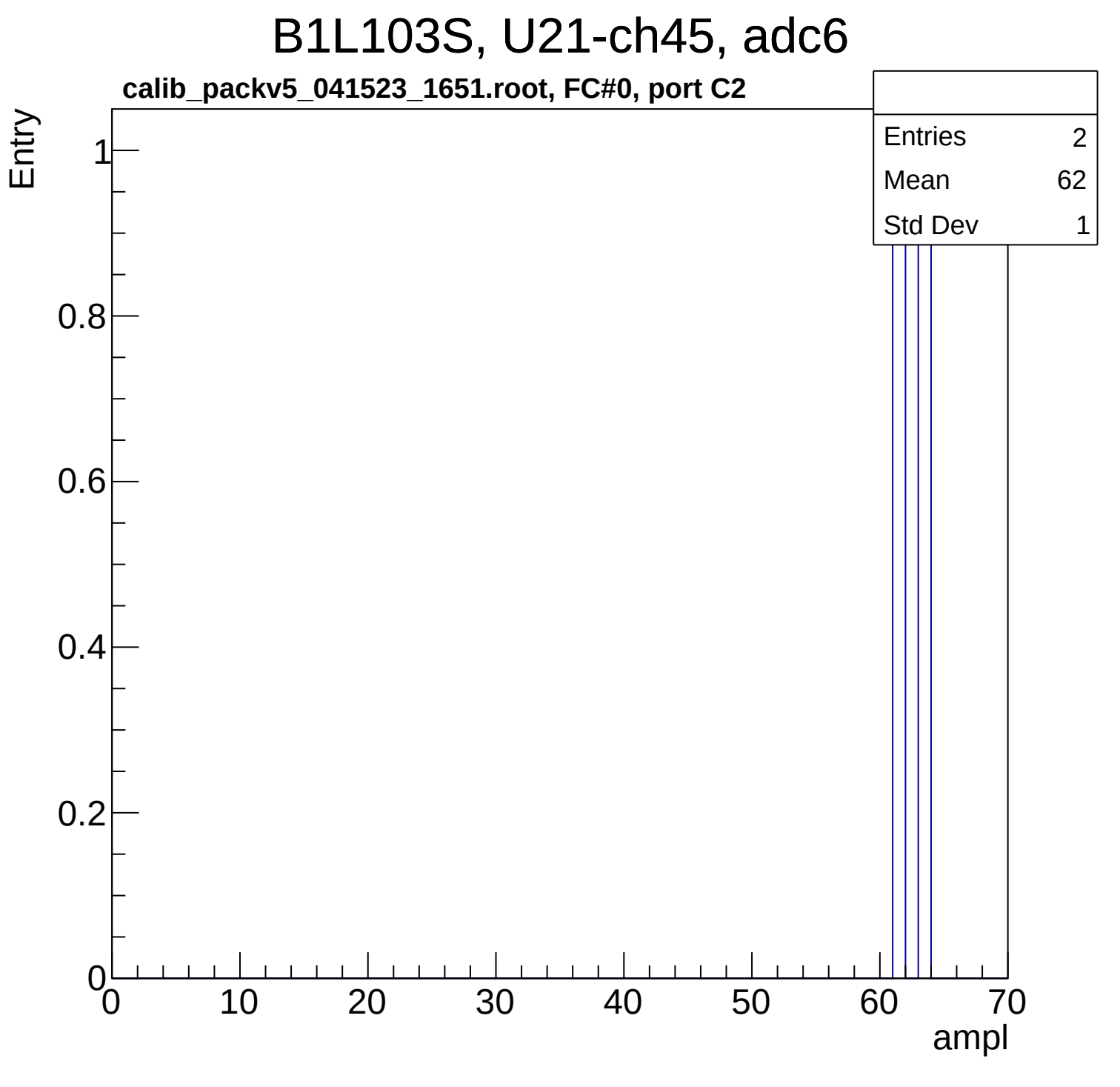
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch45, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 62
Std Dev 1
Entry
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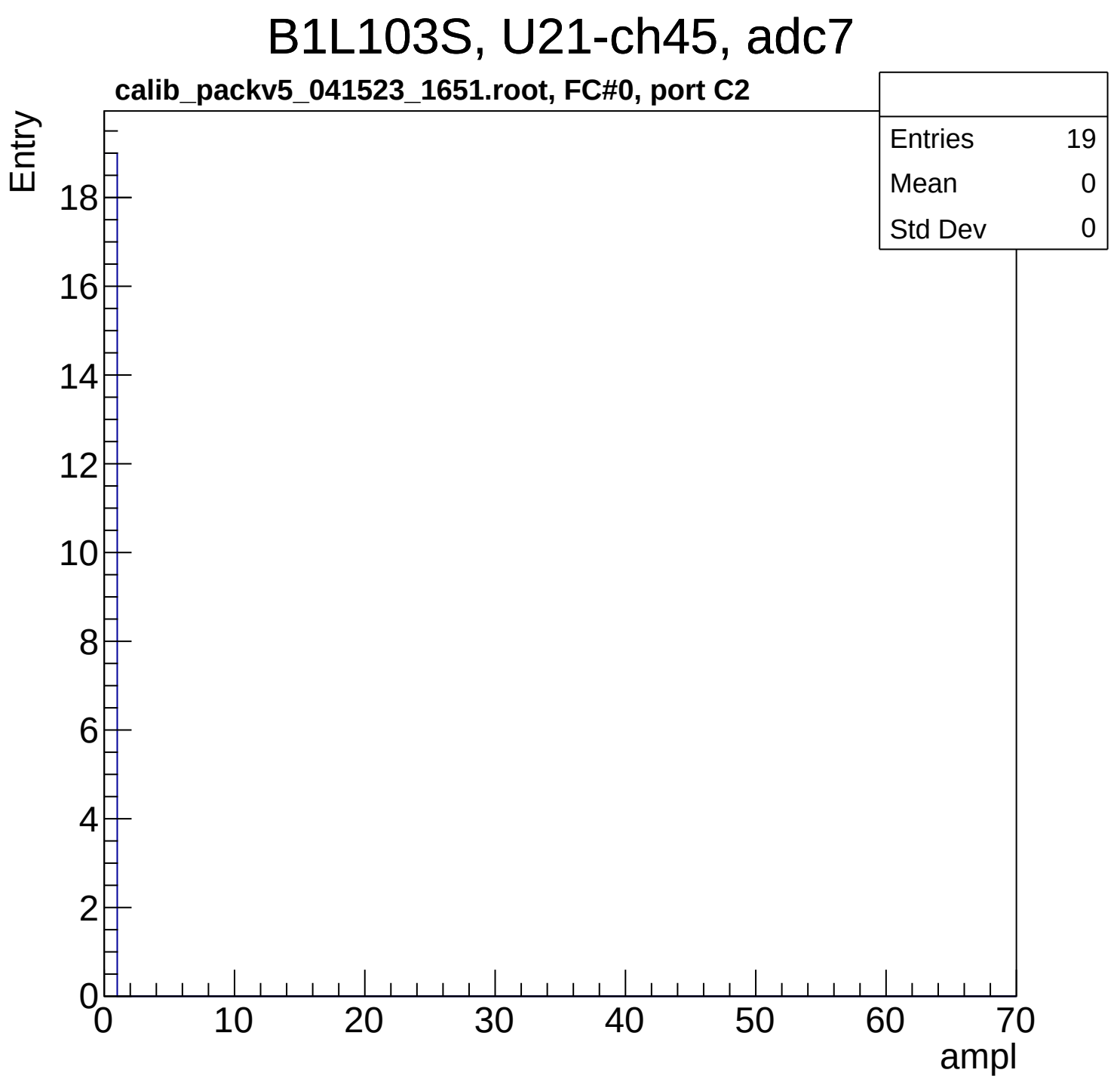
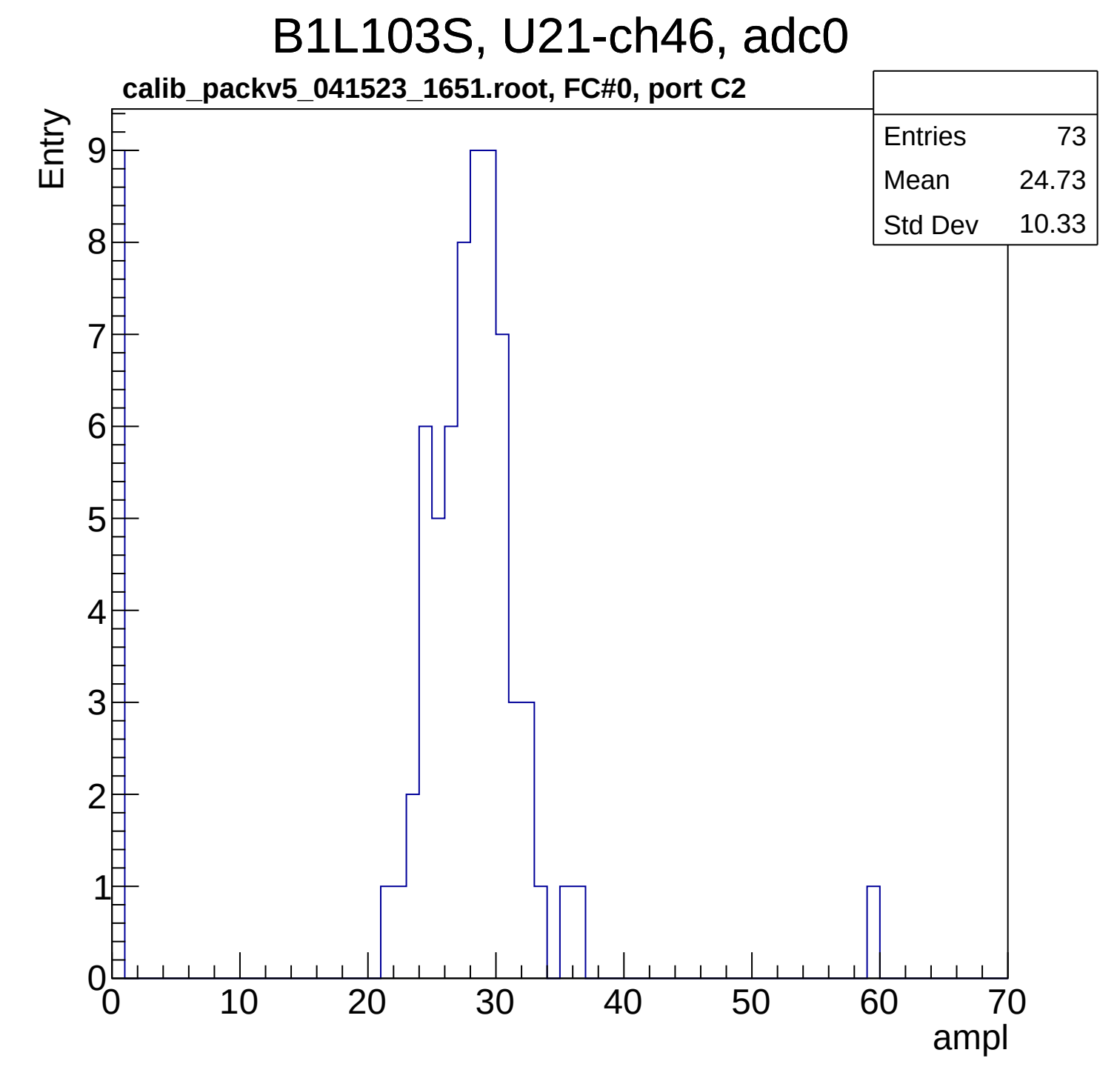
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch45, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch46, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 24.73
Std Dev 10.33
Entry
ampl
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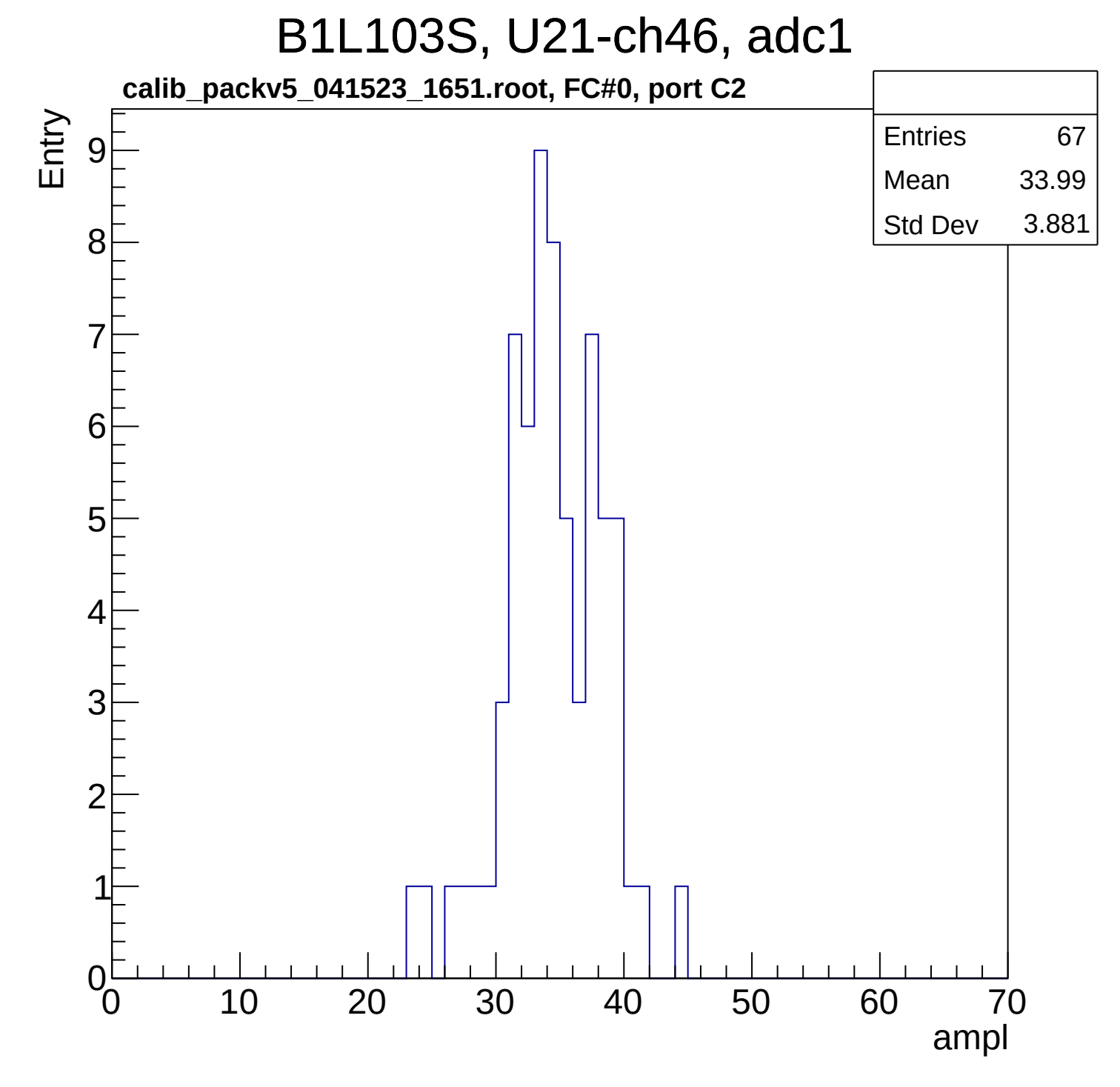
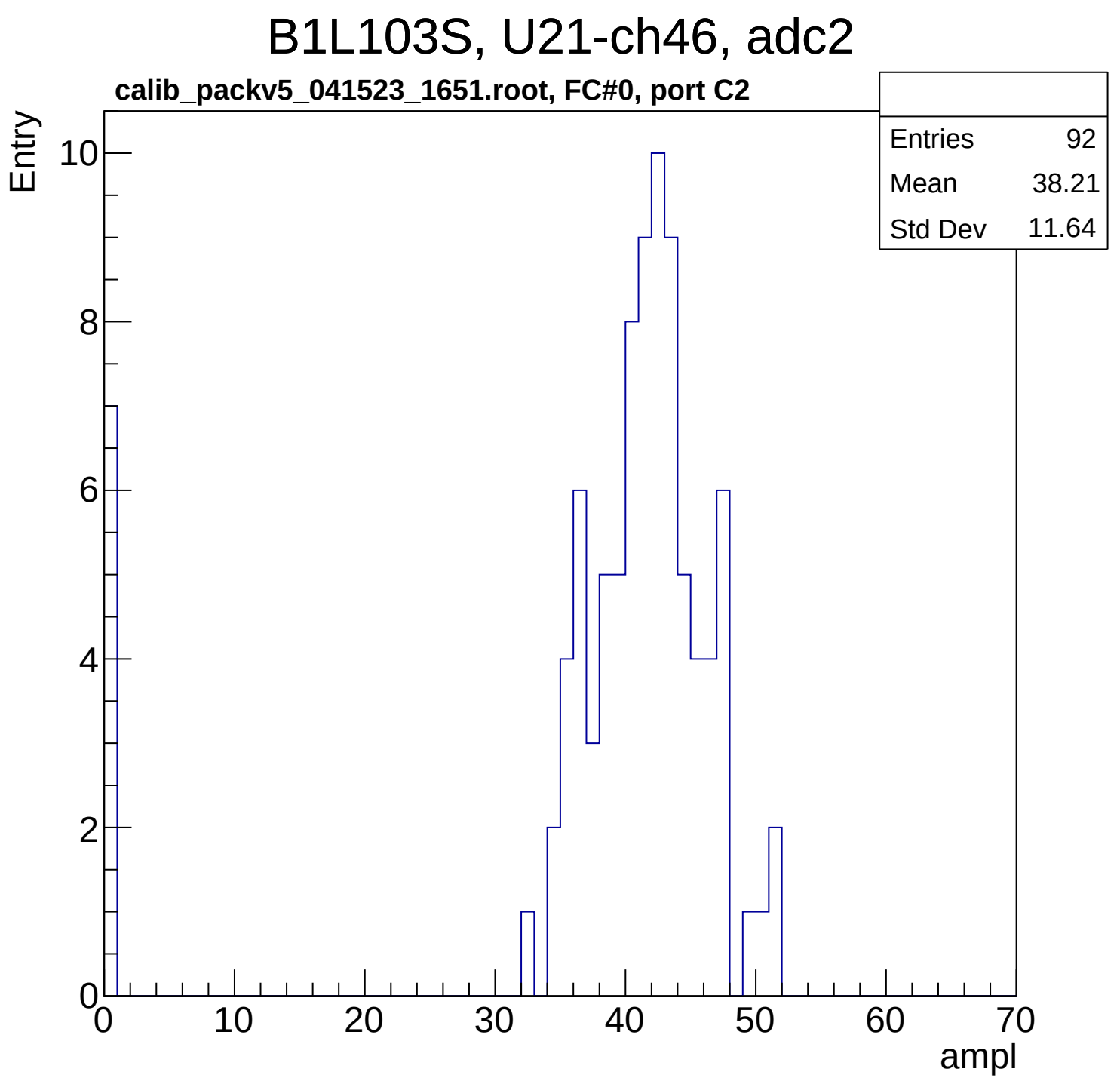
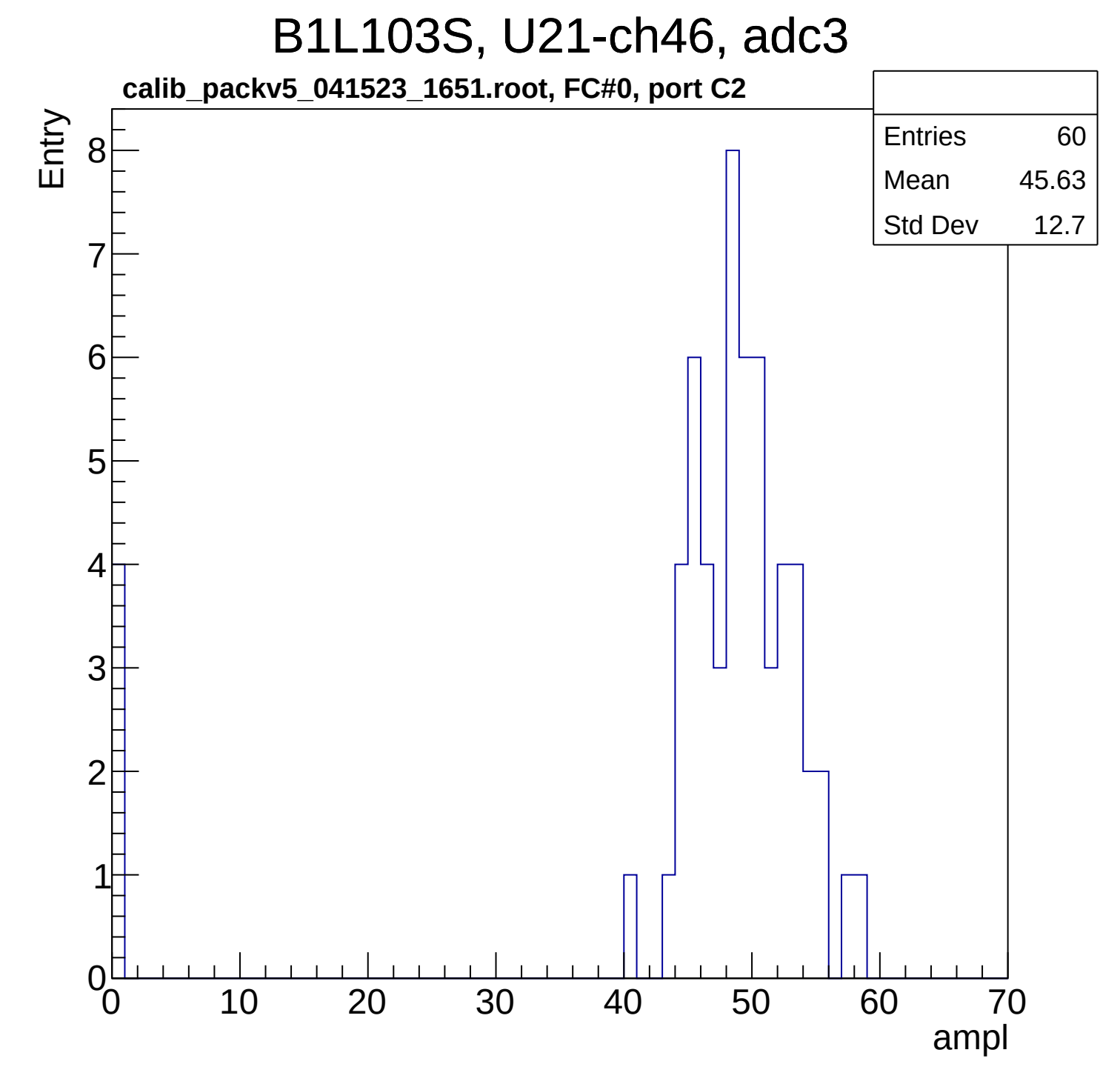
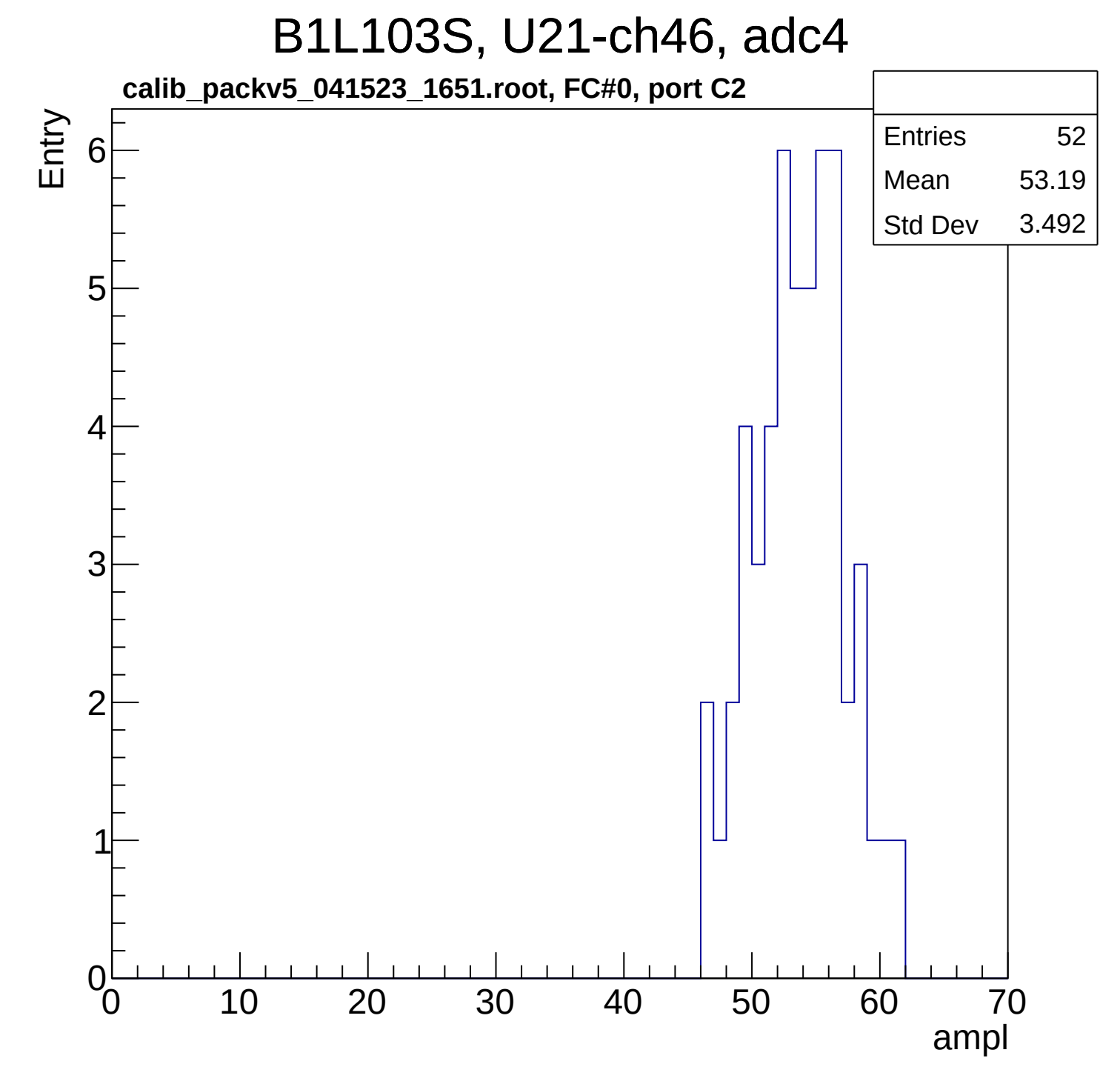
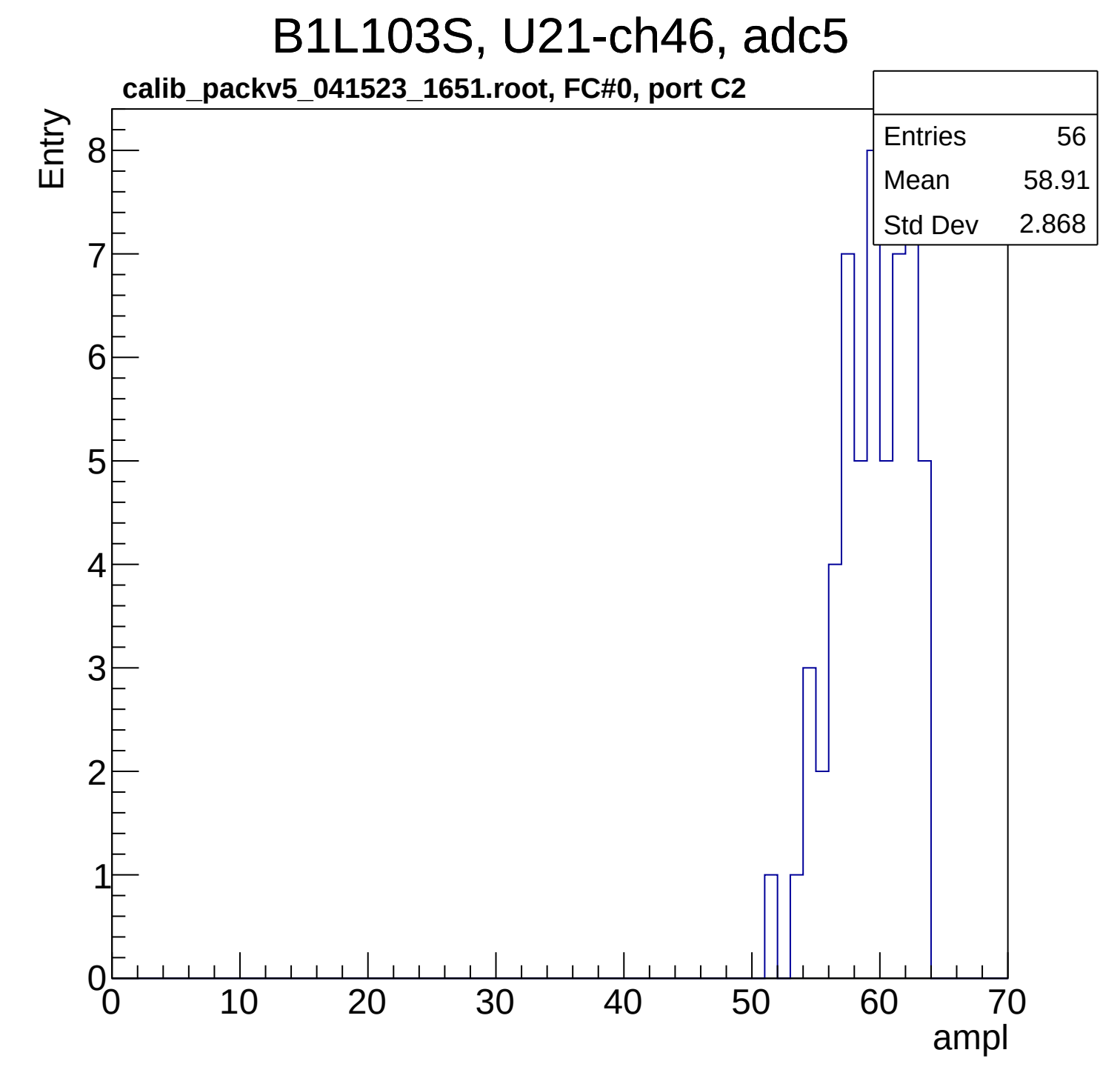
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

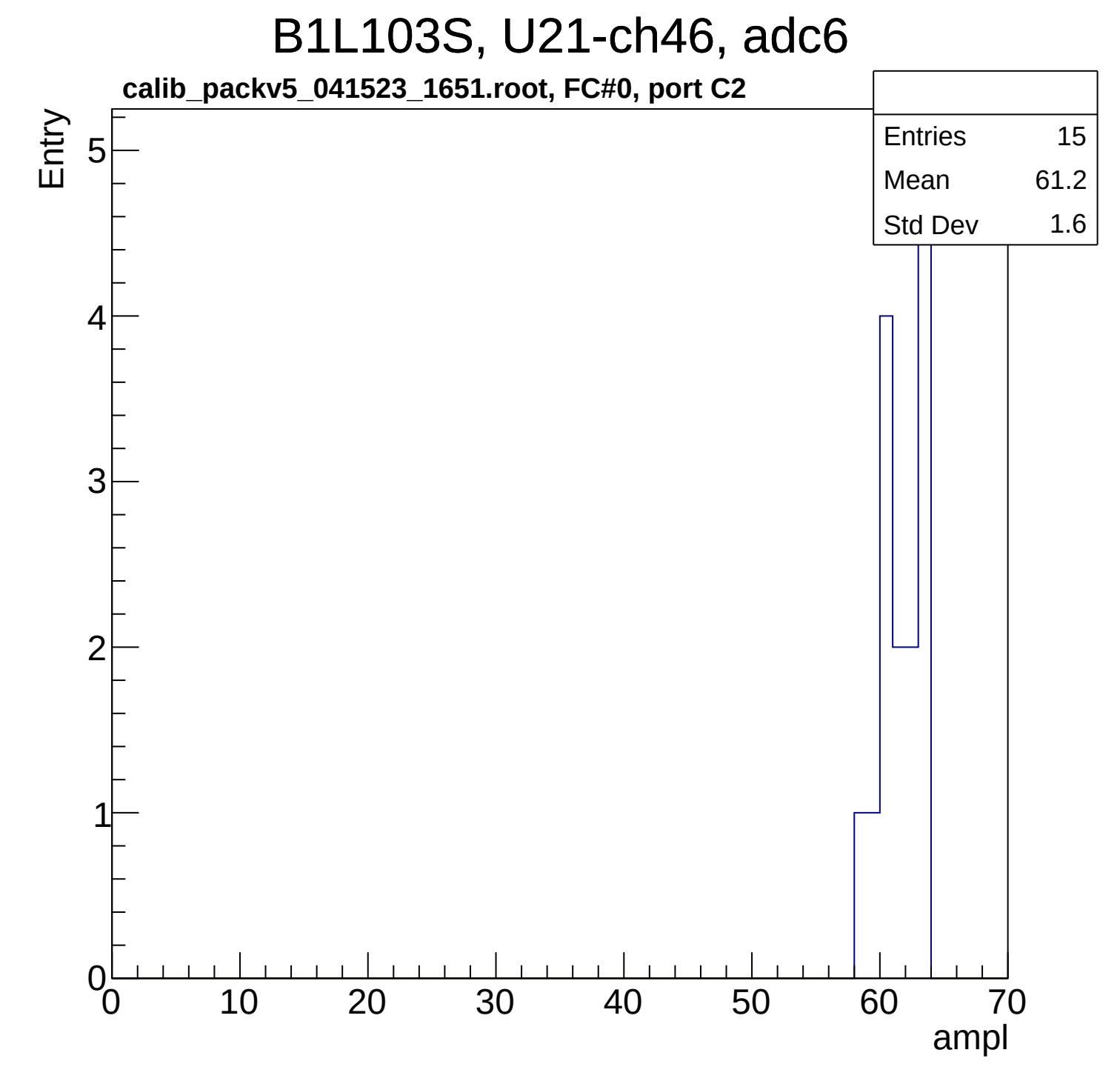

B1L103S, U21-ch46, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 33.99
Std Dev 3.881
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch46, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 38.21
Std Dev 11.64
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch46, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 45.63
Std Dev 12.7
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch46, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 53.19
Std Dev 3.492
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U21-ch46, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 58.91
Std Dev 2.868
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch46, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 61.2
Std Dev 1.6
Entry
0
1
2
3
4
5
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10
20
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50
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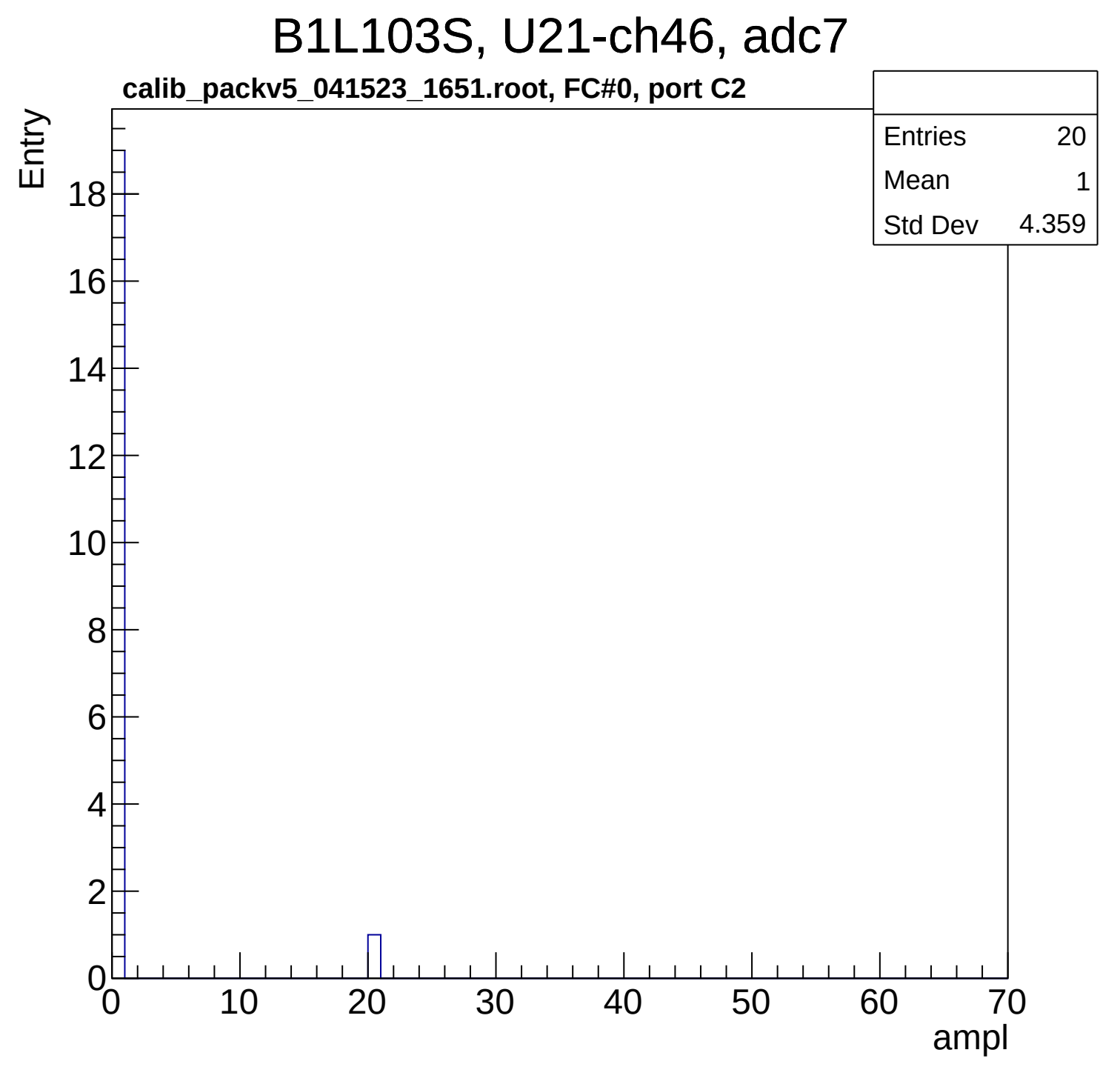
70
ampl


B1L103S, U21-ch46, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 1
Std Dev 4.359
Entry
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10
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14
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18
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10
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50
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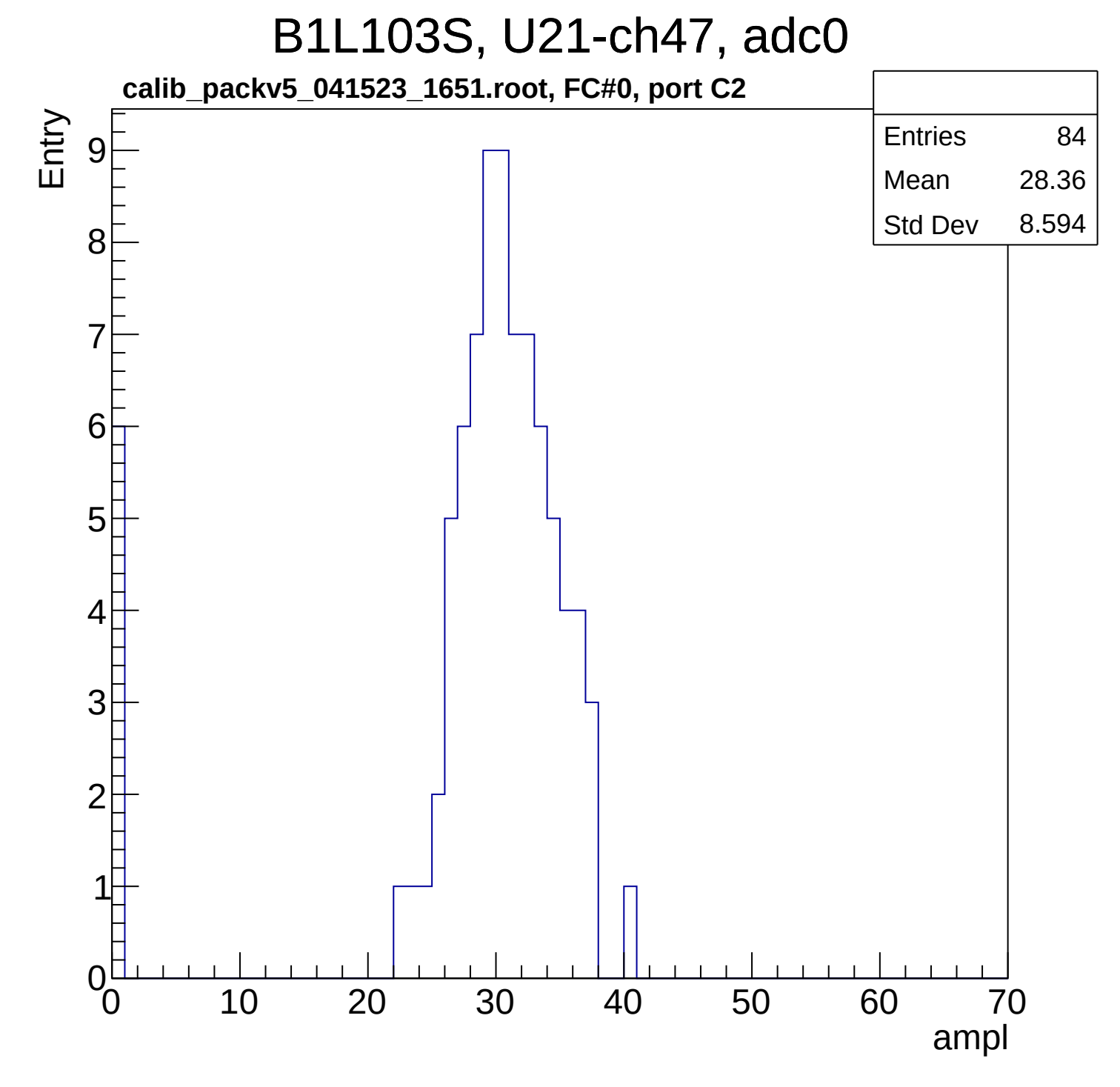
ampl


B1L103S, U21-ch47, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 28.36
Std Dev 8.594
Entry
ampl
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3
4
5
6
7
8
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0
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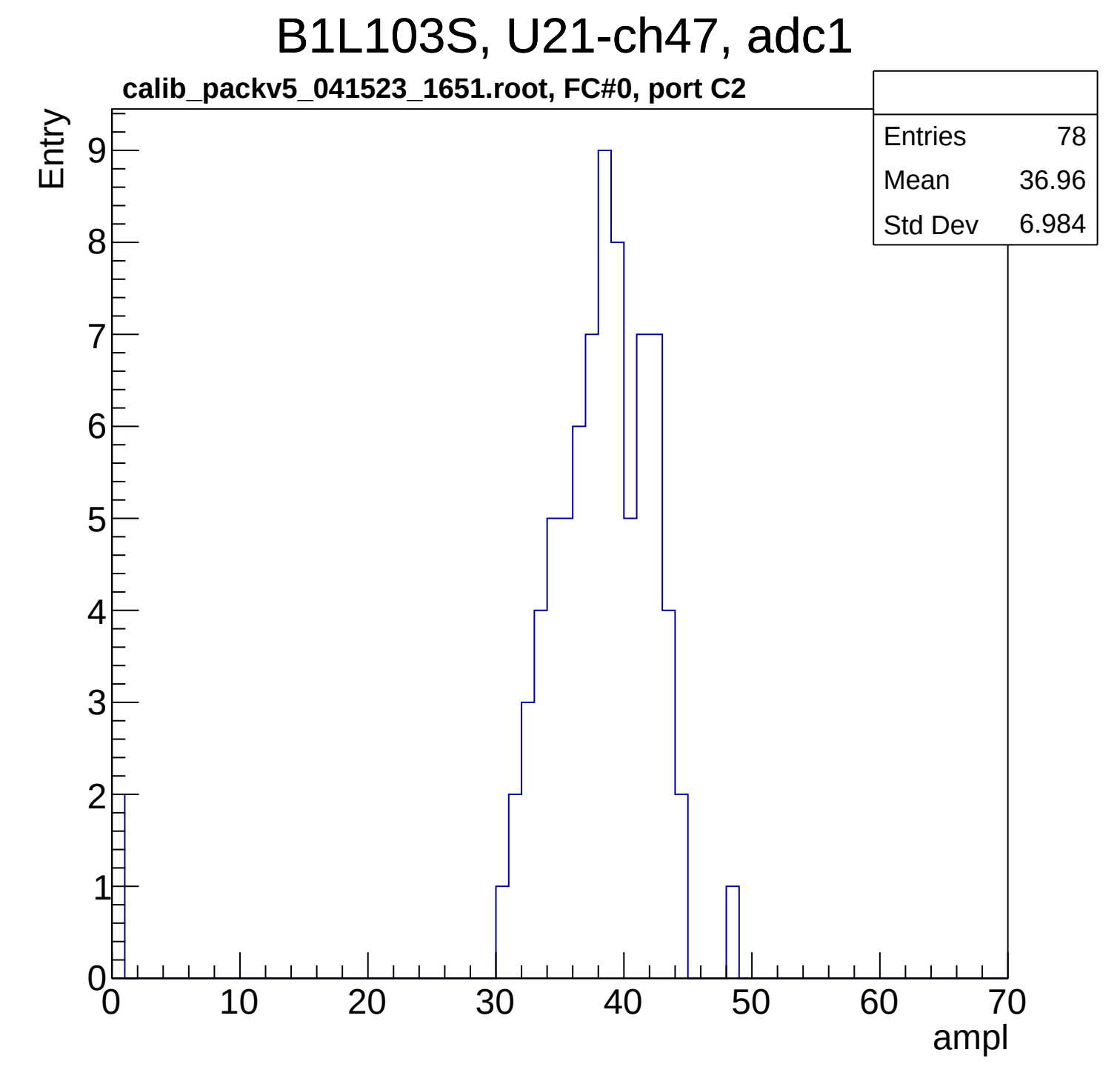
B1L103S, U21-ch47, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 36.96
Std Dev 6.984
Entry
ampl
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3
4
5
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7
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0
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60
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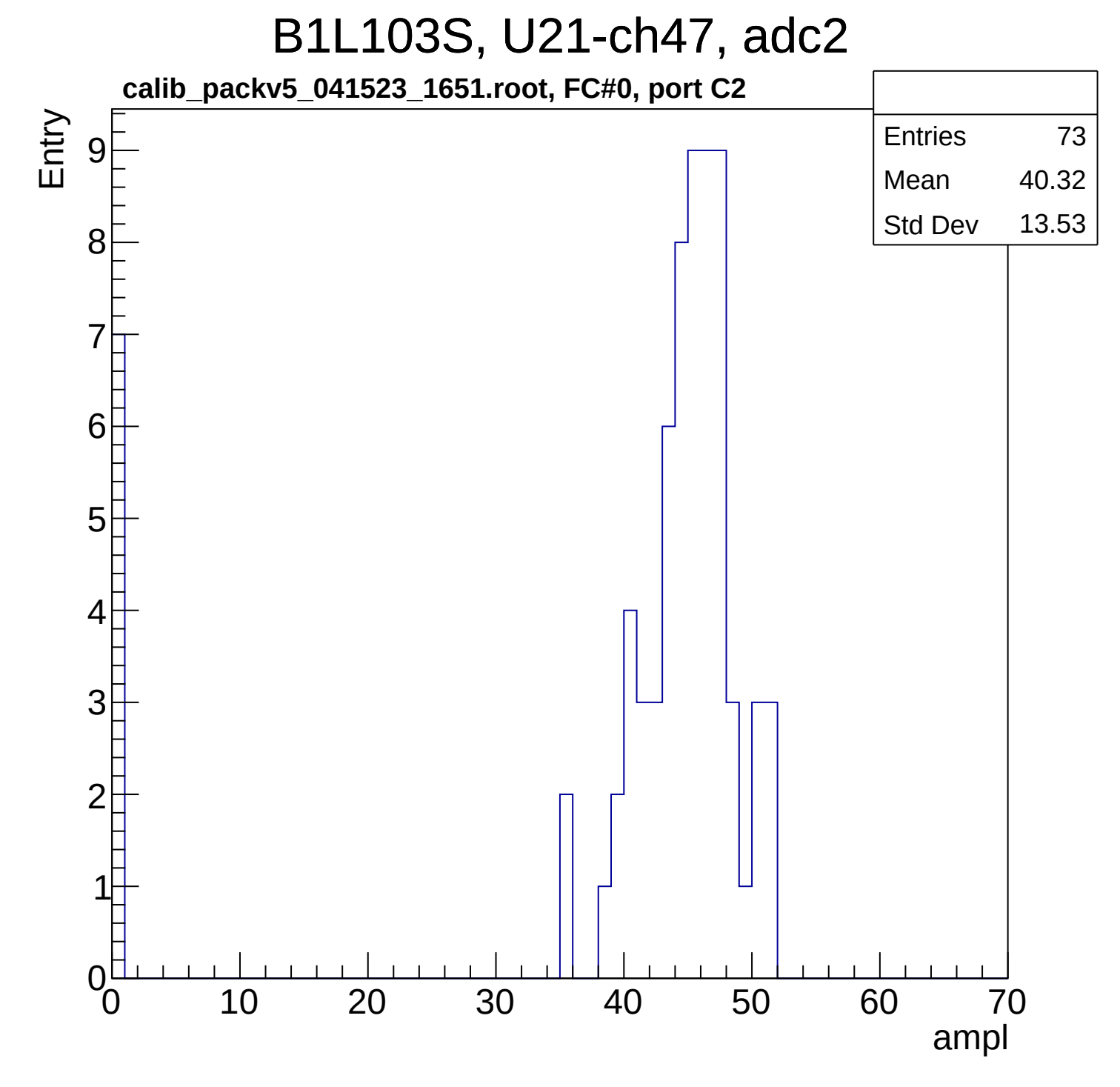
B1L103S, U21-ch47, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 40.32
Std Dev 13.53
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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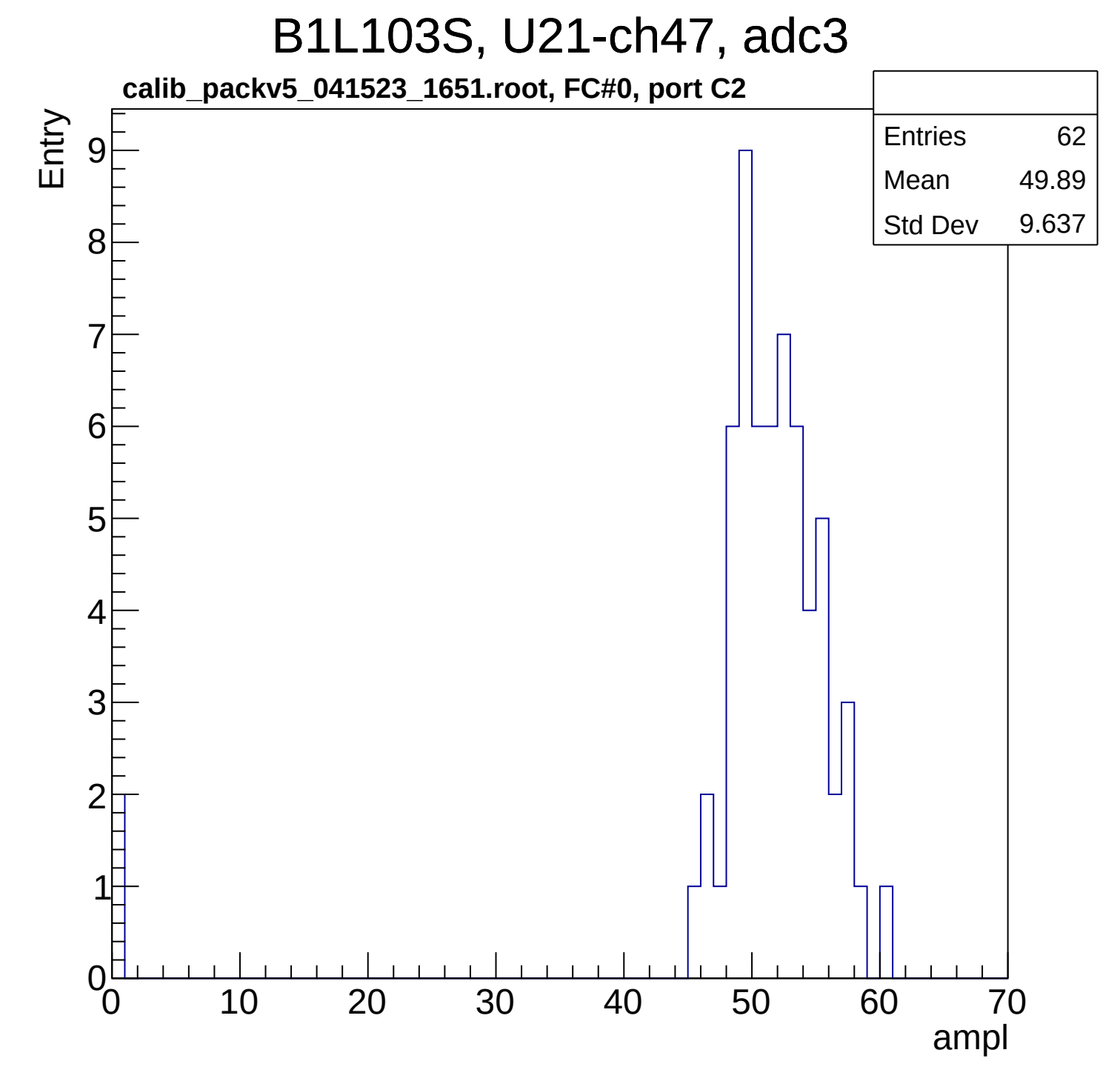
B1L103S, U21-ch47, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 49.89
Std Dev 9.637
Entry
ampl
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4
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8
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0
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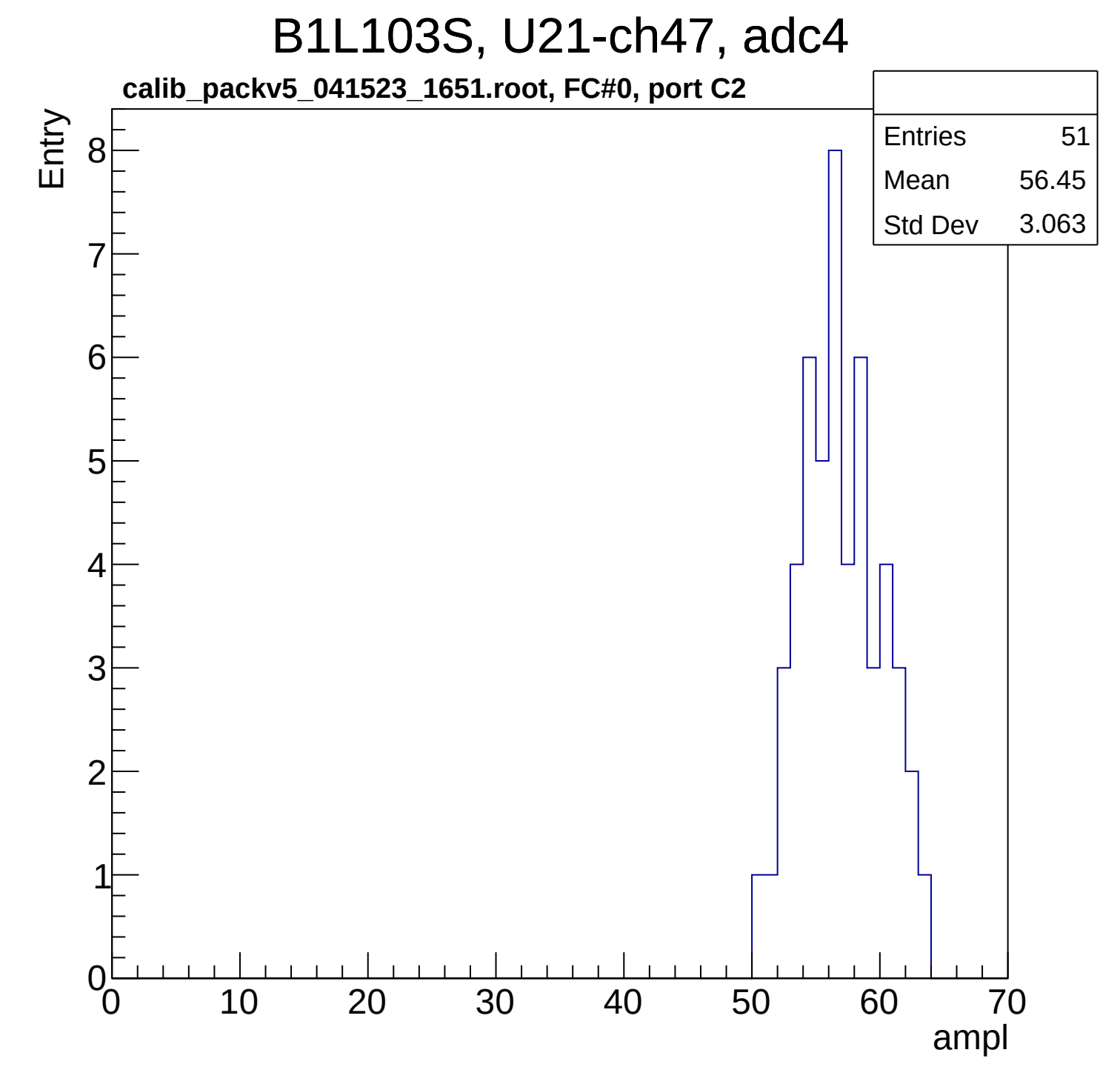
B1L103S, U21-ch47, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 56.45
Std Dev 3.063
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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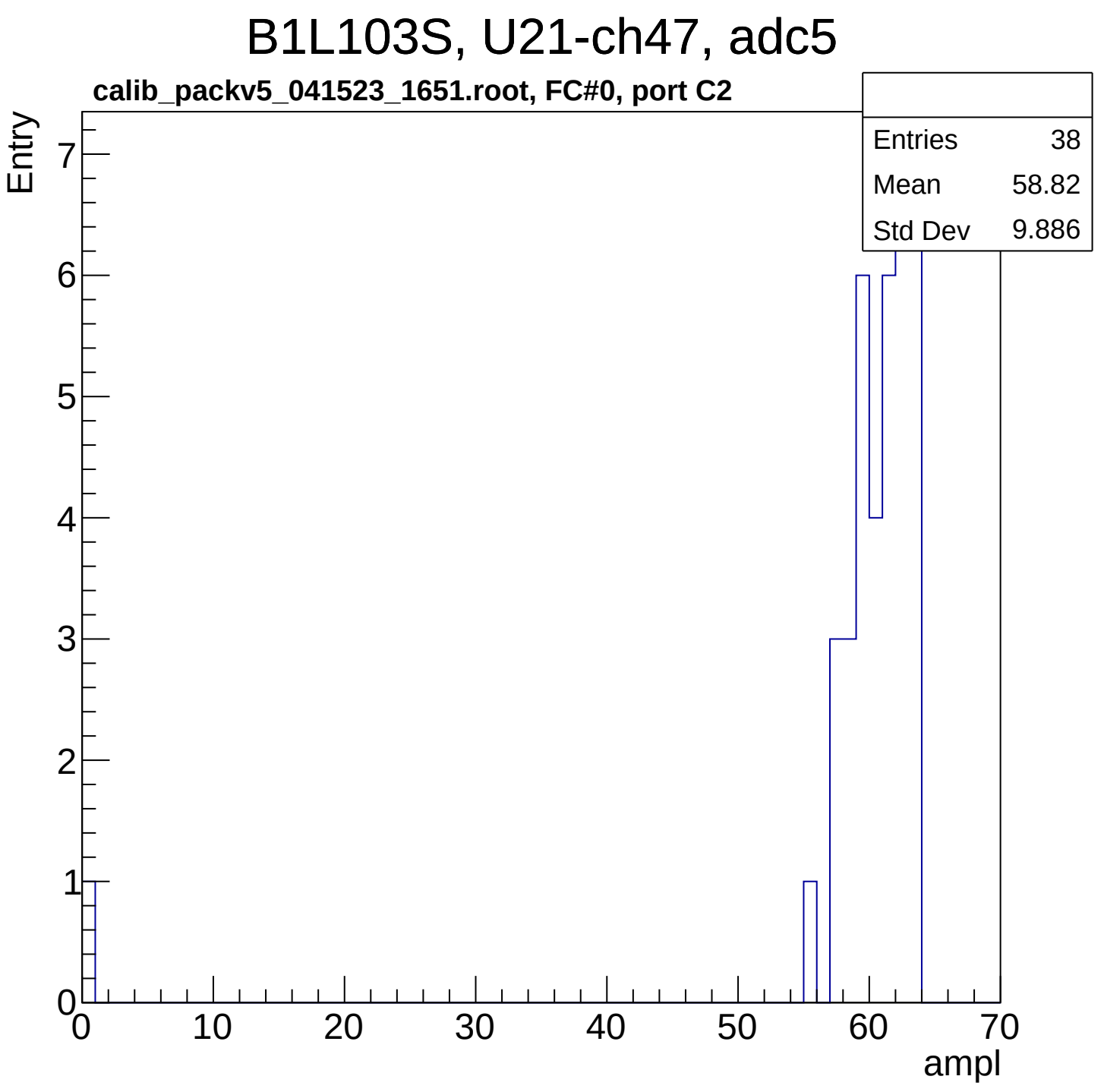
B1L103S, U21-ch47, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 58.82
Std Dev 9.886
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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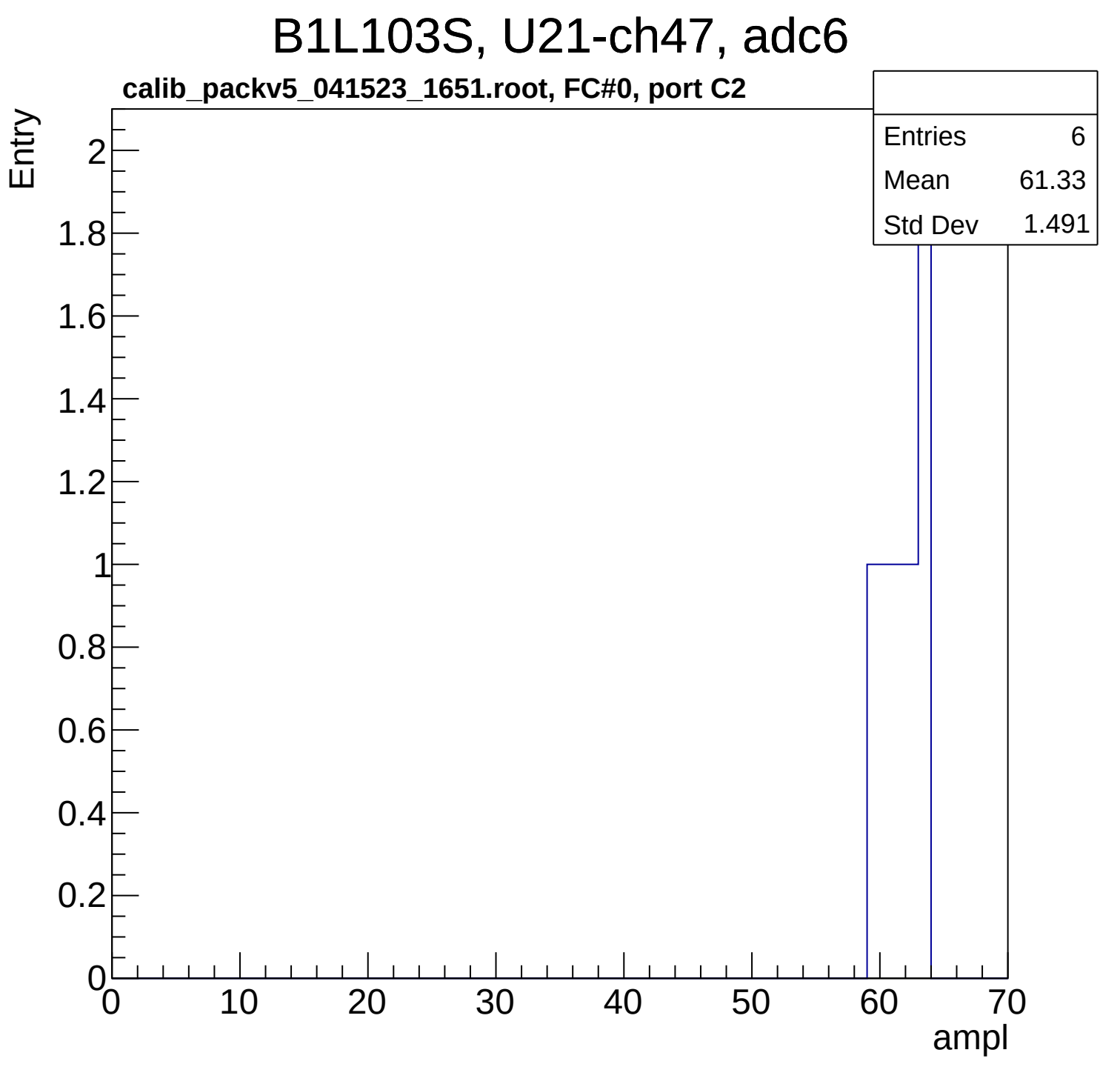
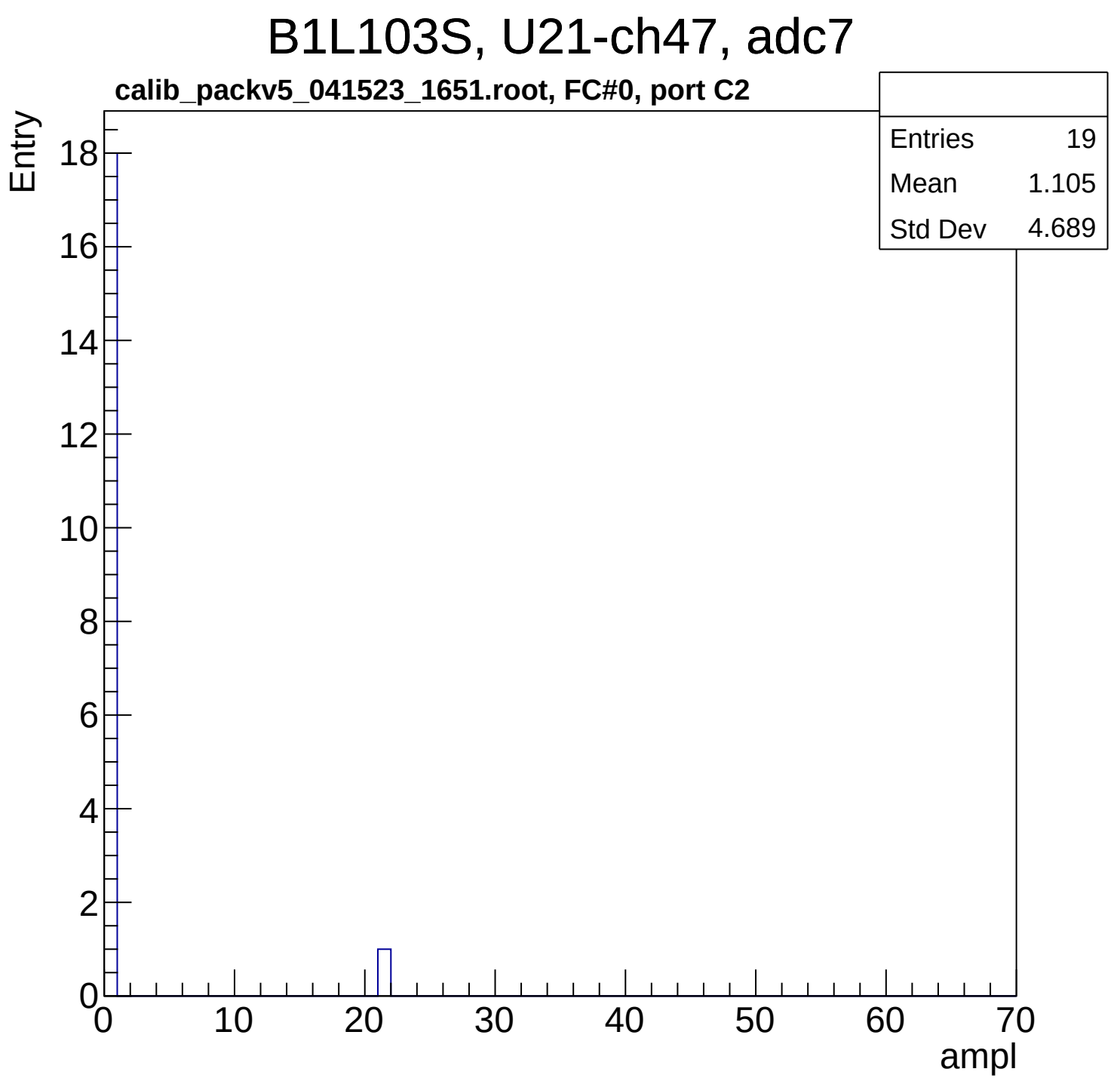
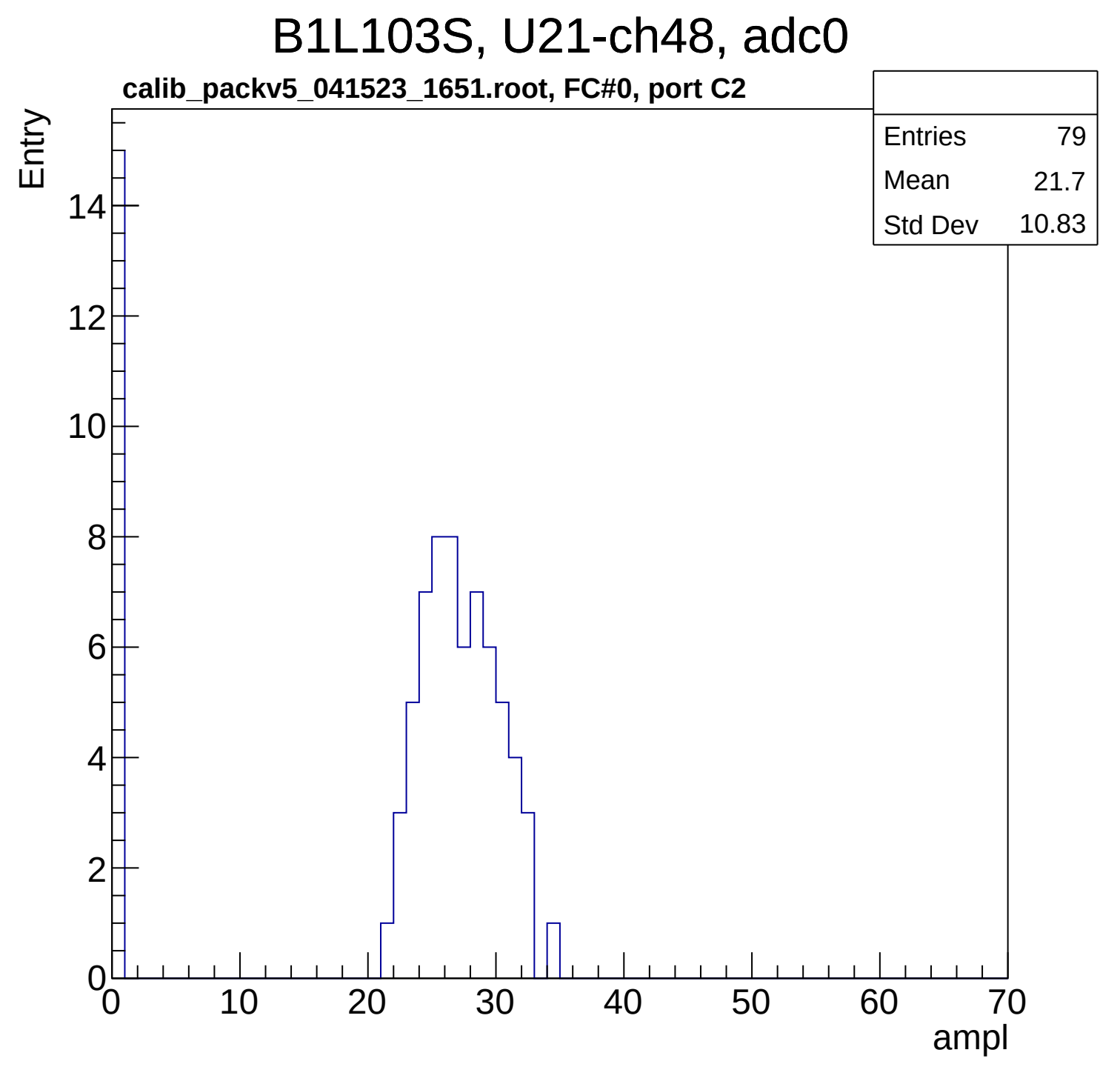

B1L103S, U21-ch47, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 61.33
Std Dev 1.491
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U21-ch47, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.105
Std Dev 4.689
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch48, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 21.7
Std Dev 10.83
Entry
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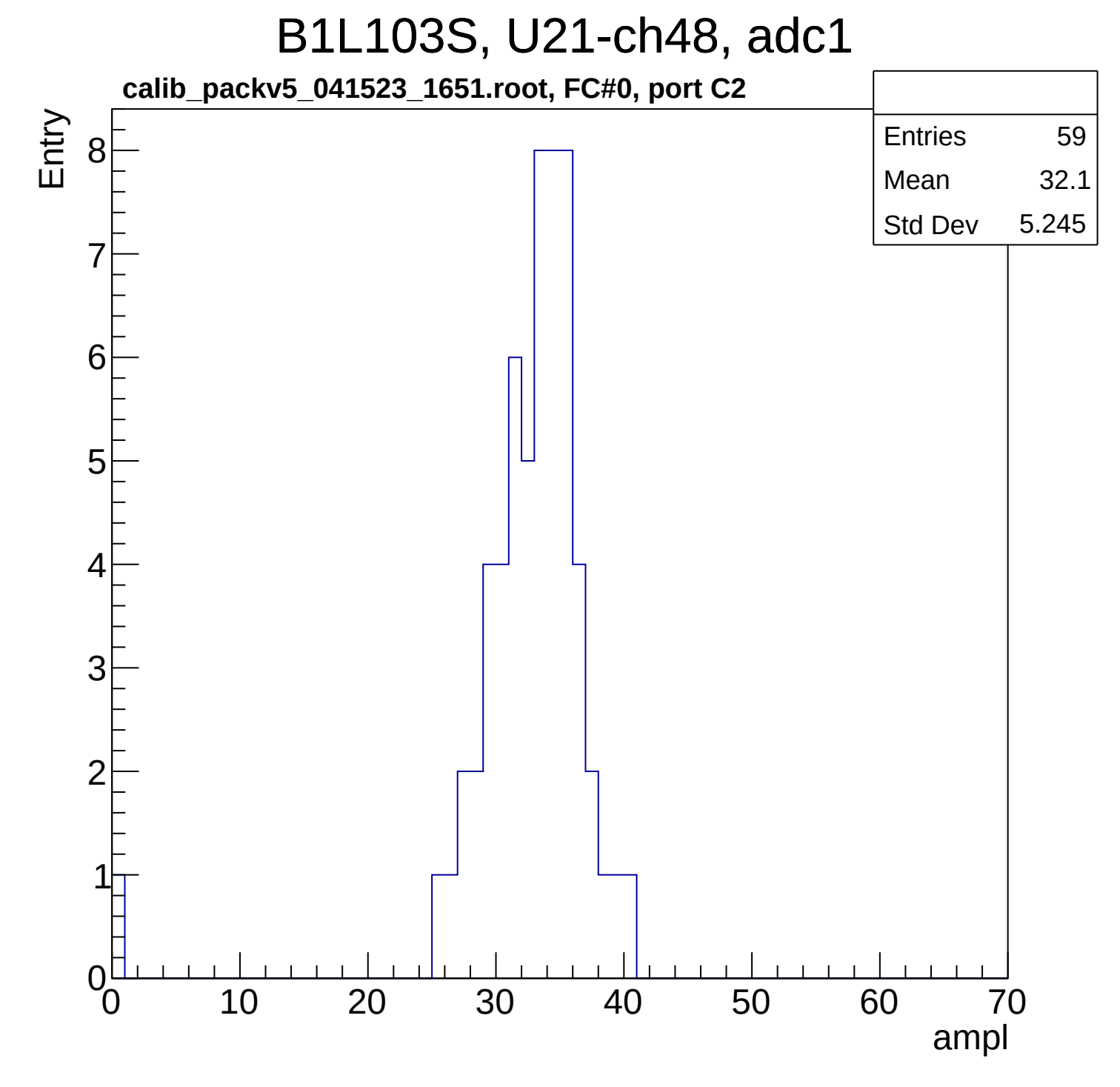
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch48, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 32.1
Std Dev 5.245
Entry
ampl
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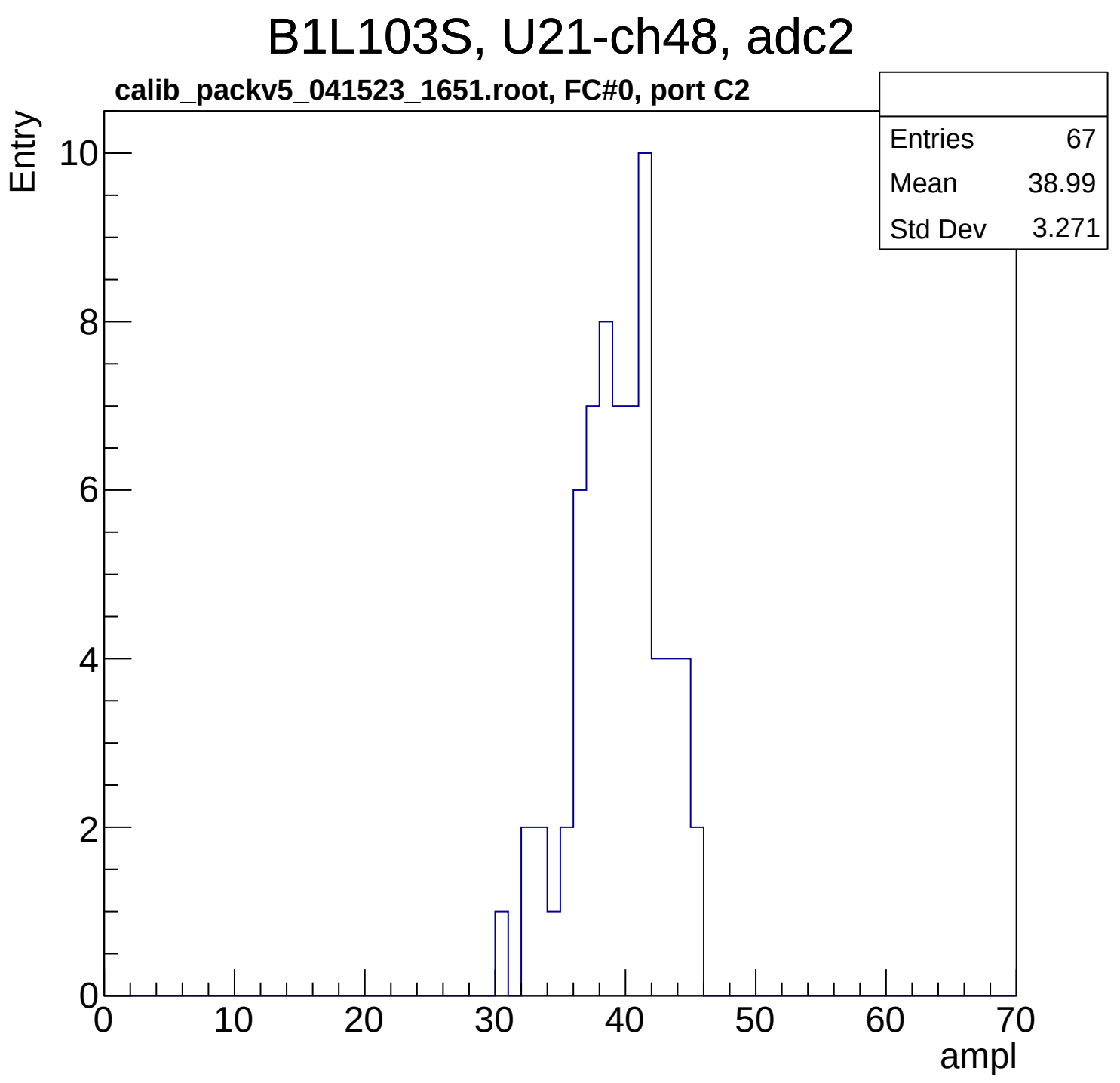
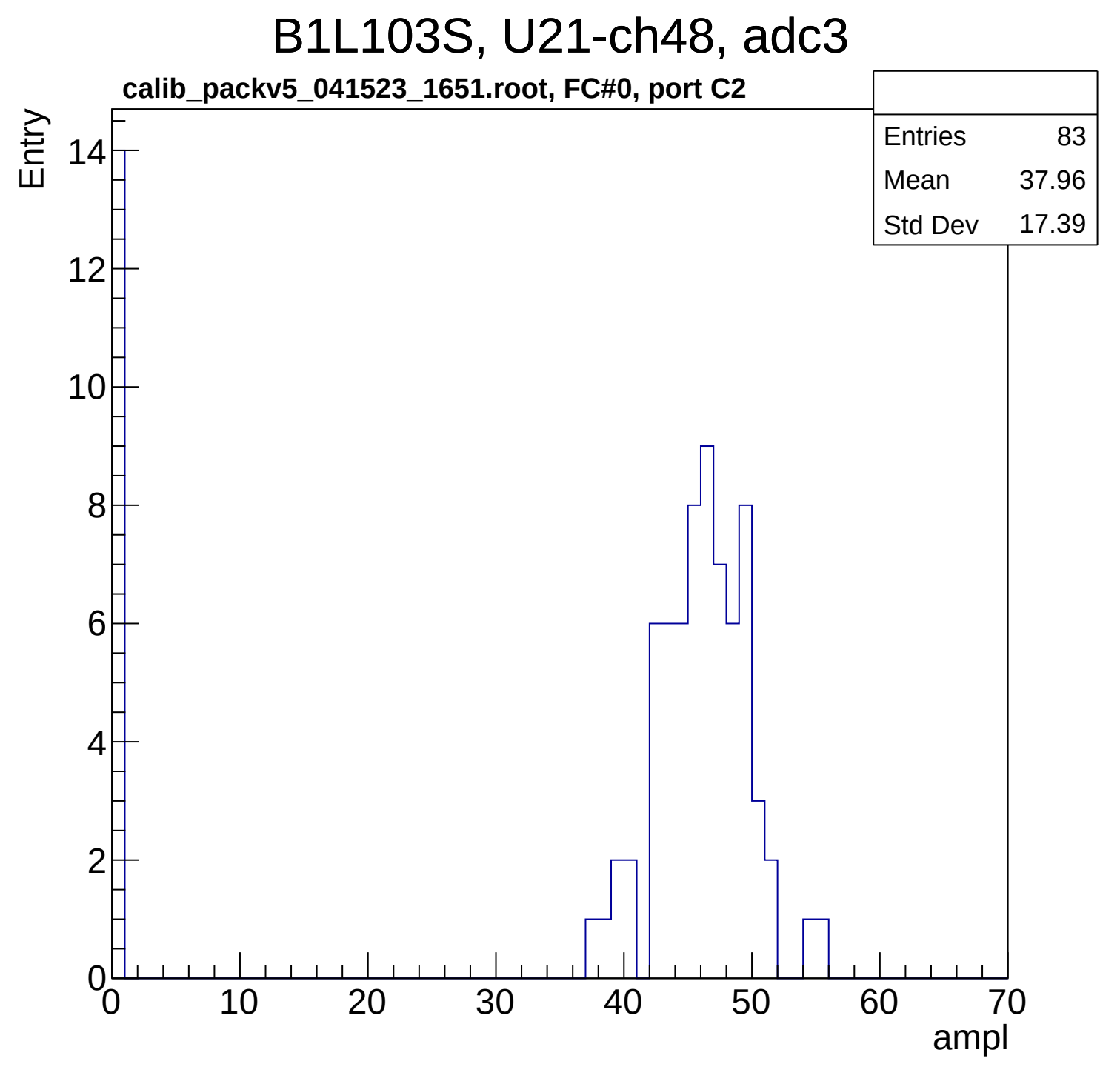
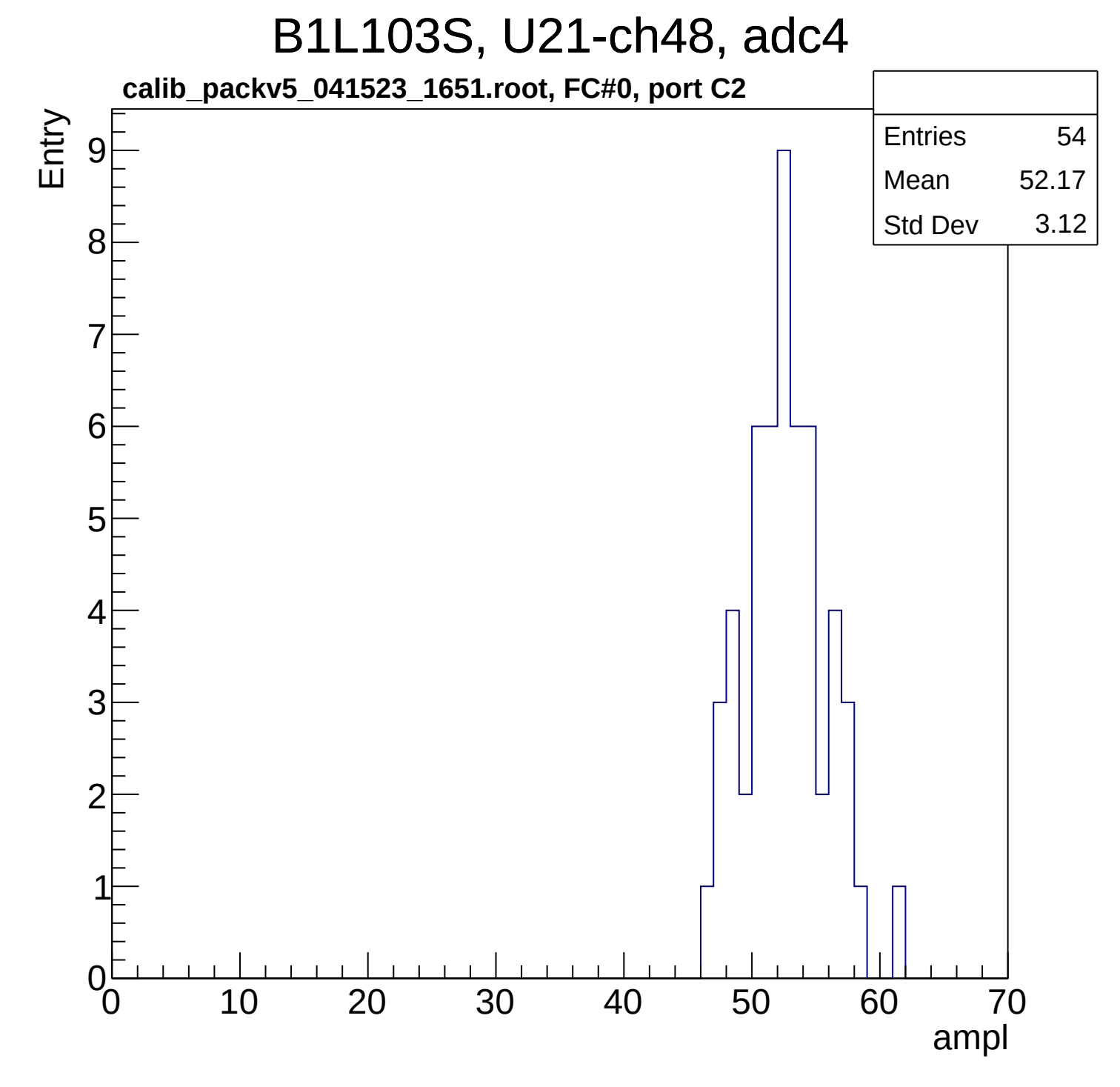
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch48, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 38.99
Std Dev 3.271
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U21-ch48, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 37.96
Std Dev 17.39
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U21-ch48, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 52.17
Std Dev 3.12
Entry
ampl
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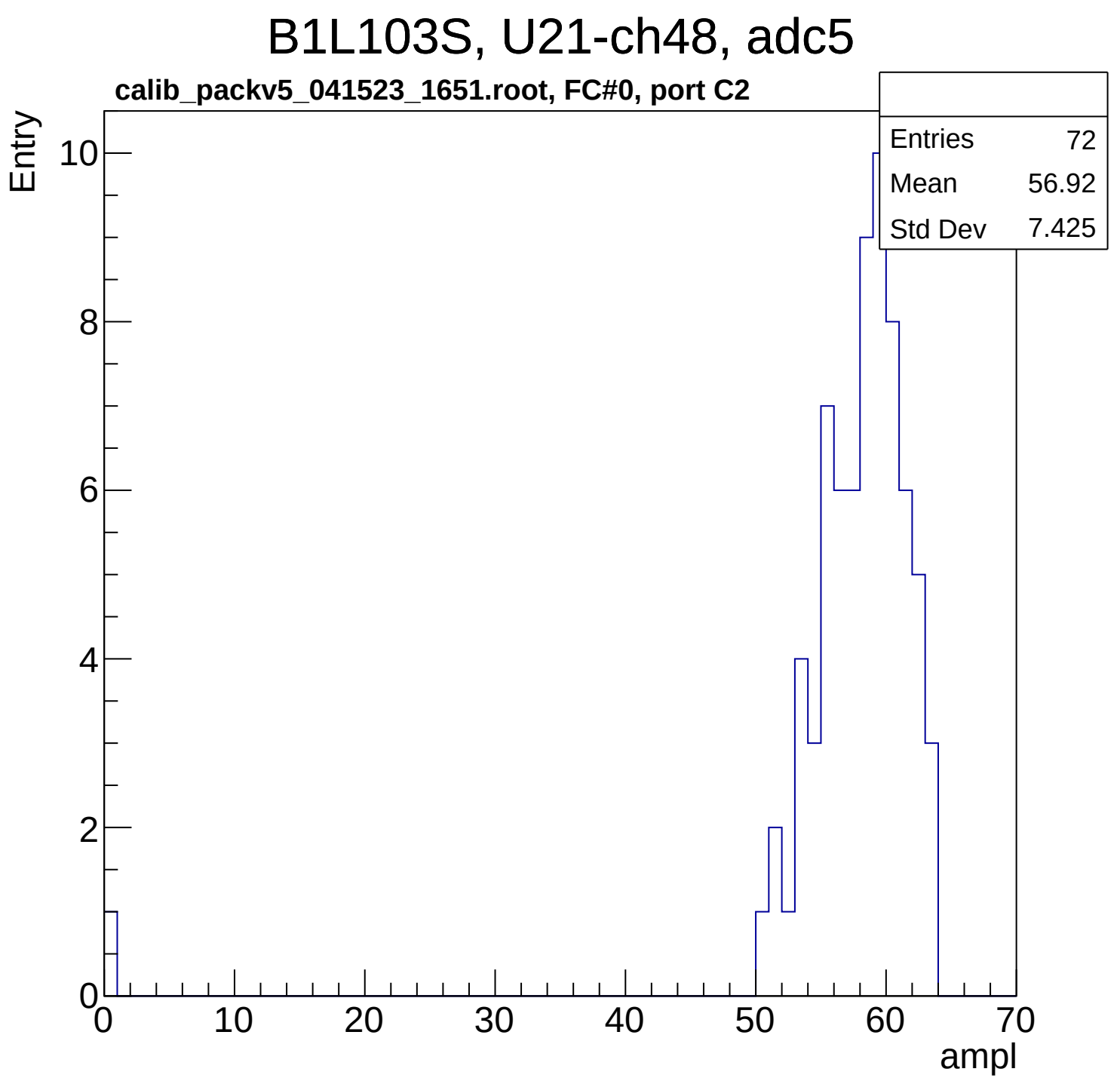
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch48, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 56.92
Std Dev 7.425
Entry
ampl
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4
6
8
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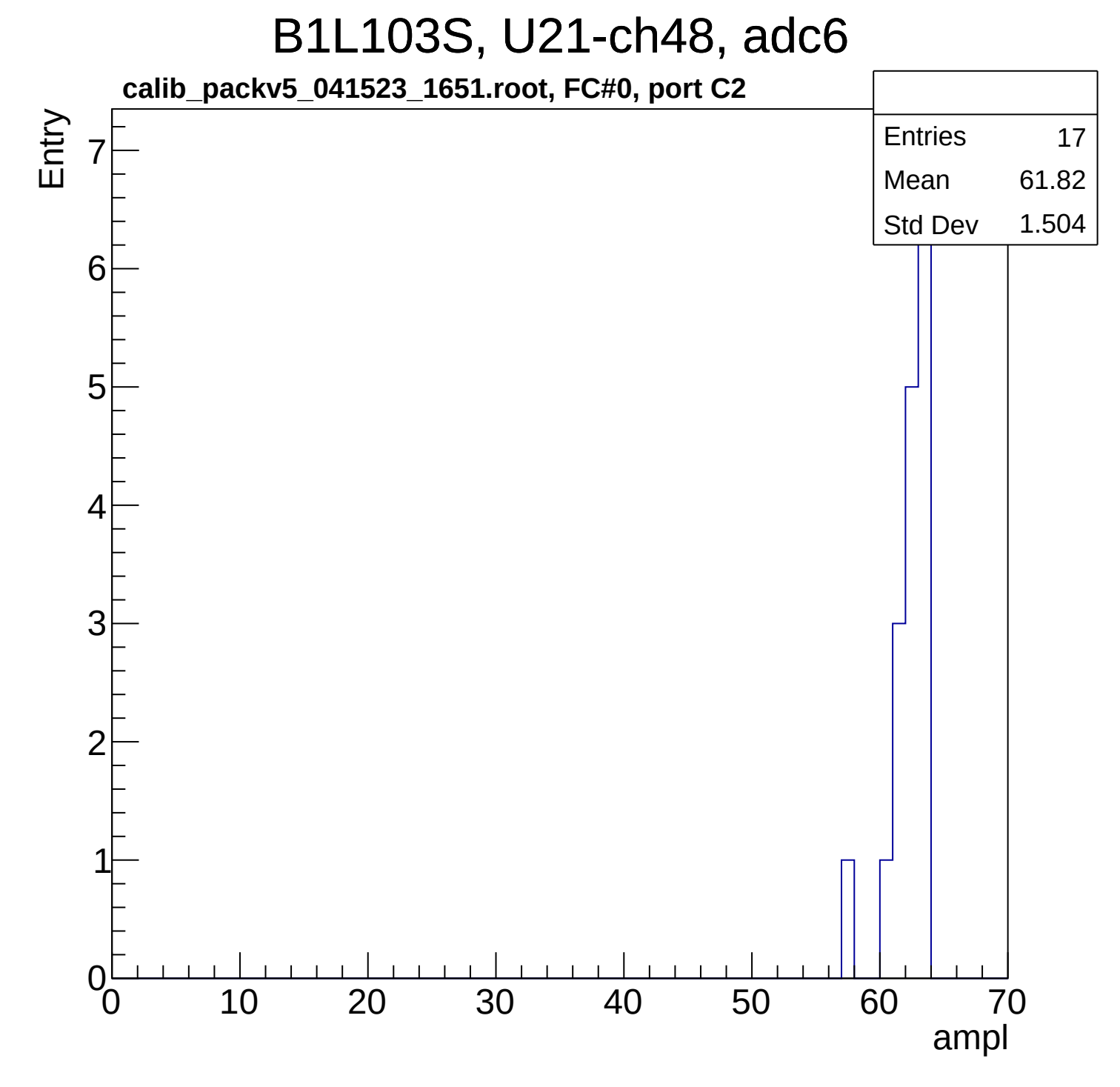
0
10
20
30
40
50
60
70


B1L103S, U21-ch48, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 61.82
Std Dev 1.504
Entry
ampl
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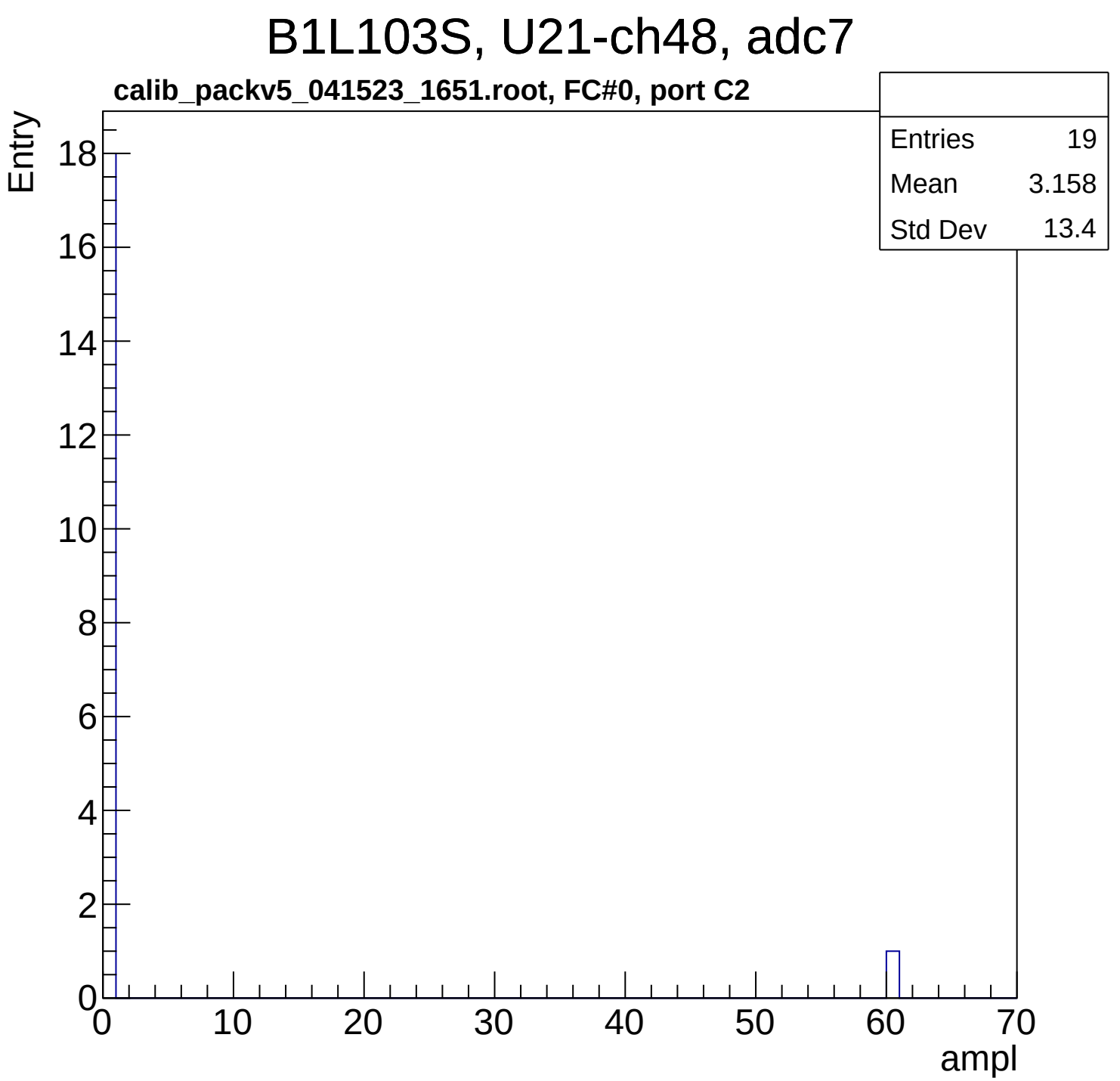
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U21-ch48, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.158
Std Dev 13.4
Entry
0
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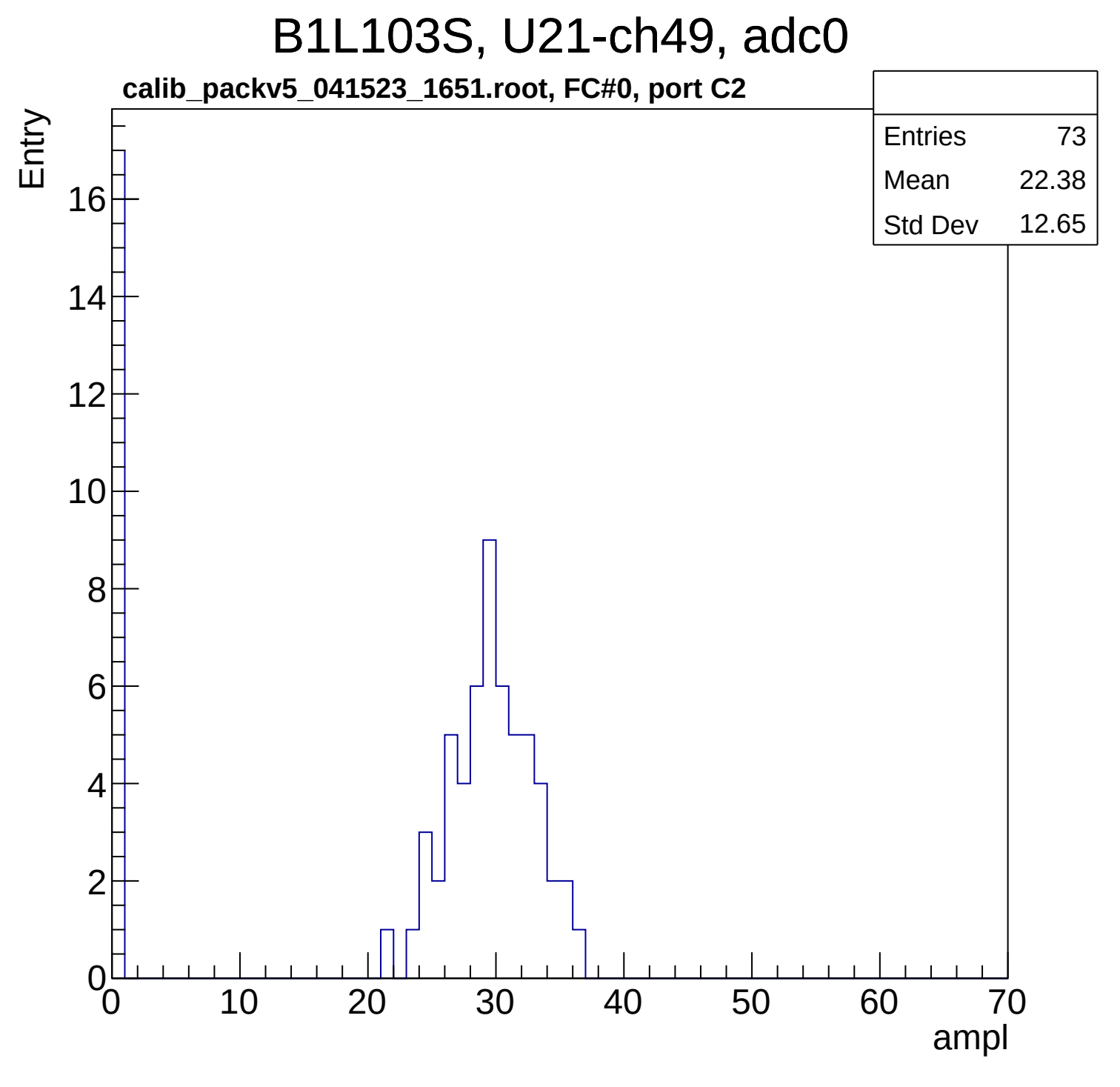
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch49, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 22.38
Std Dev 12.65
Entry
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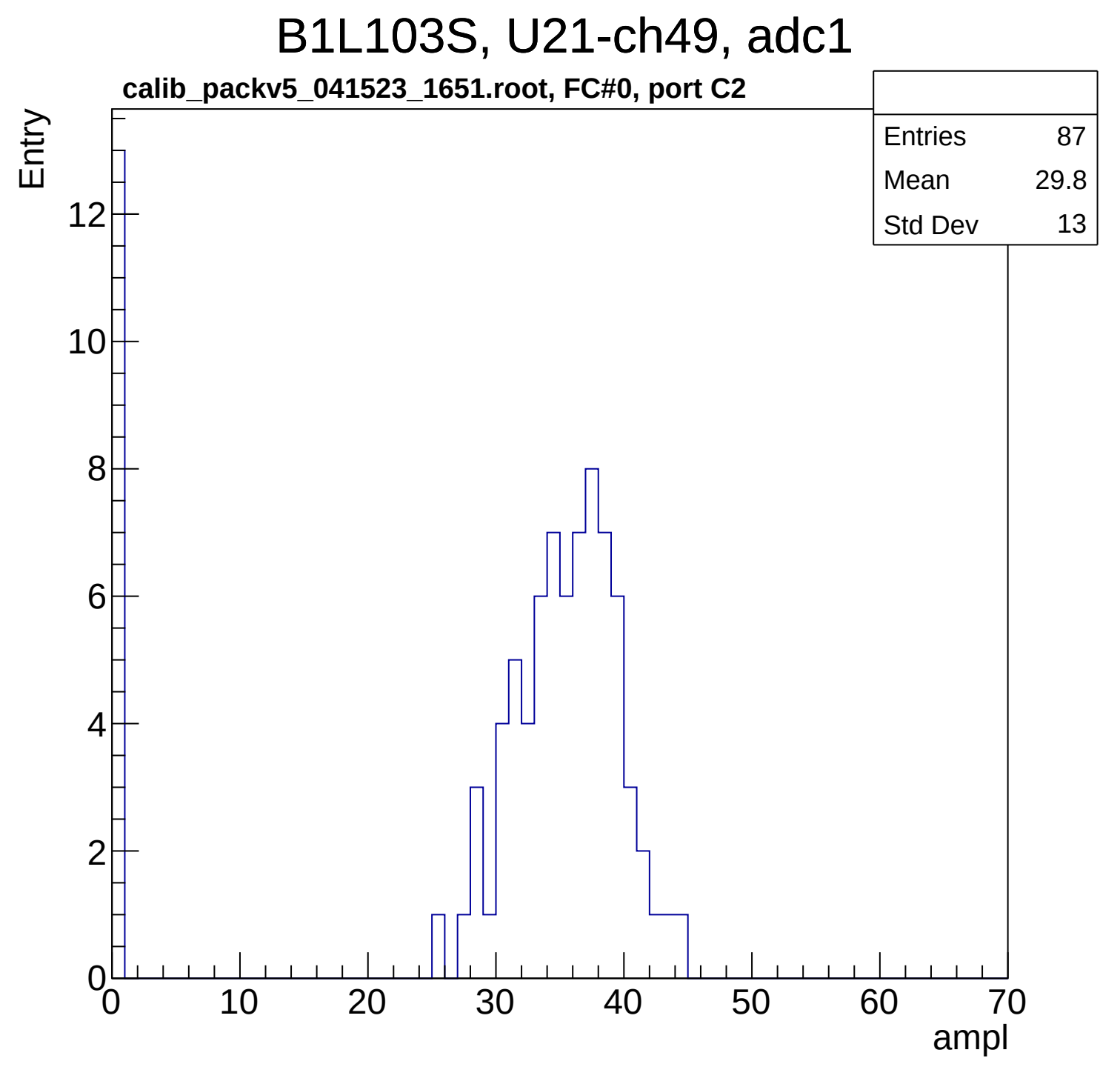
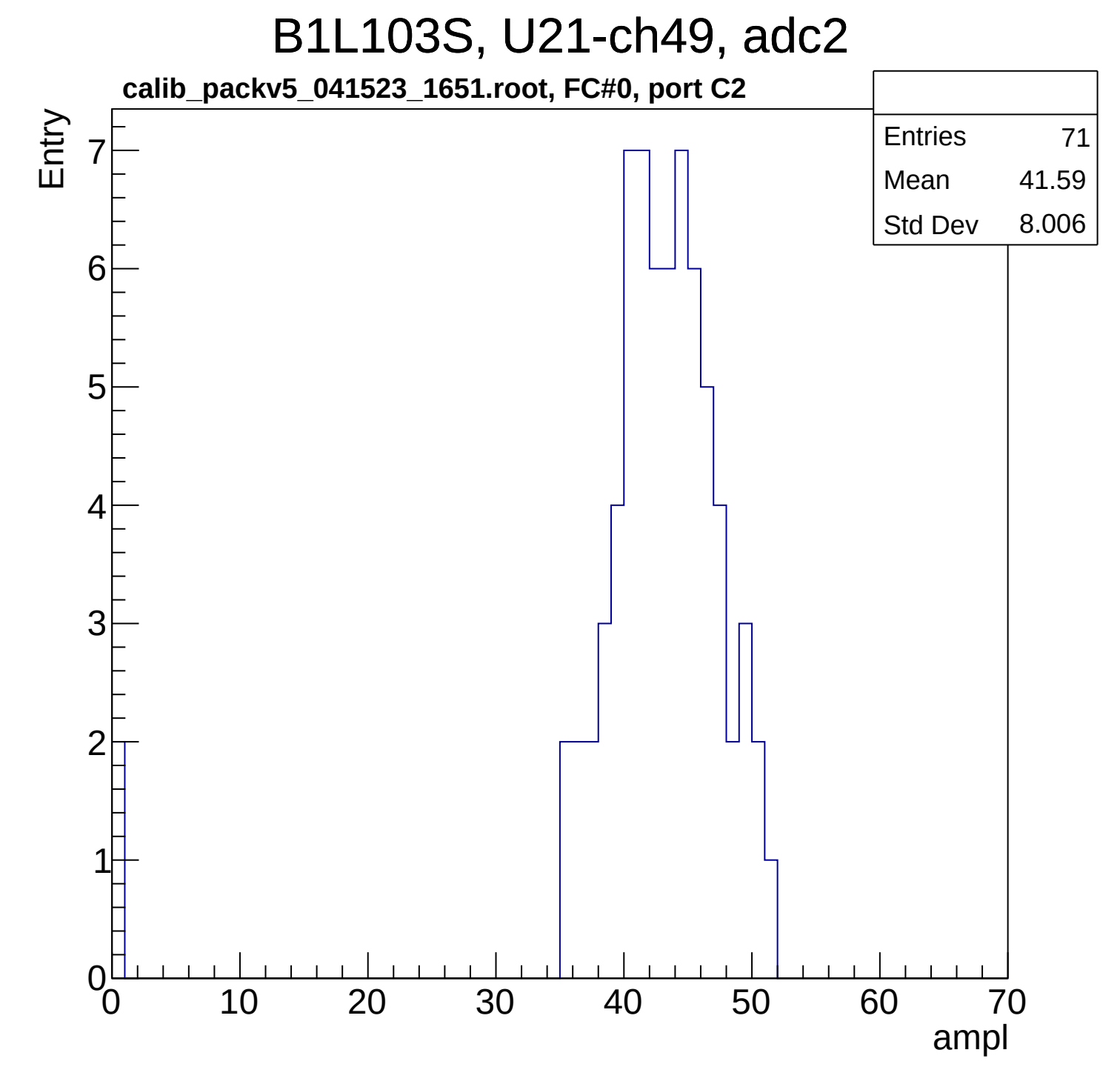
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch49, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 29.8
Std Dev 13
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch49, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 41.59
Std Dev 8.006
Entry
ampl
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2
3
4
5
6
7
0
10
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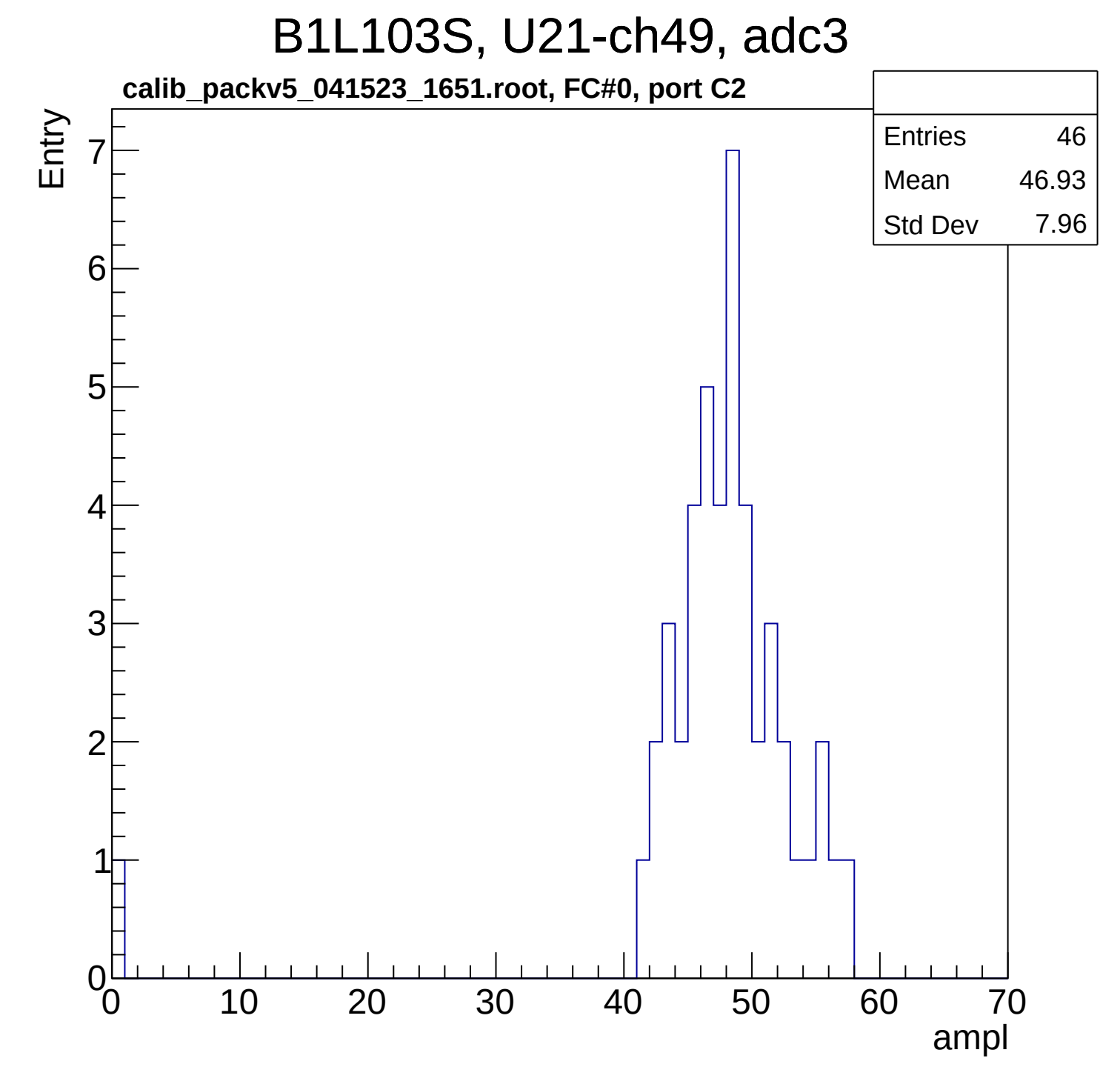
30
40
50
60
70


B1L103S, U21-ch49, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 46.93
Std Dev 7.96
Entry
ampl
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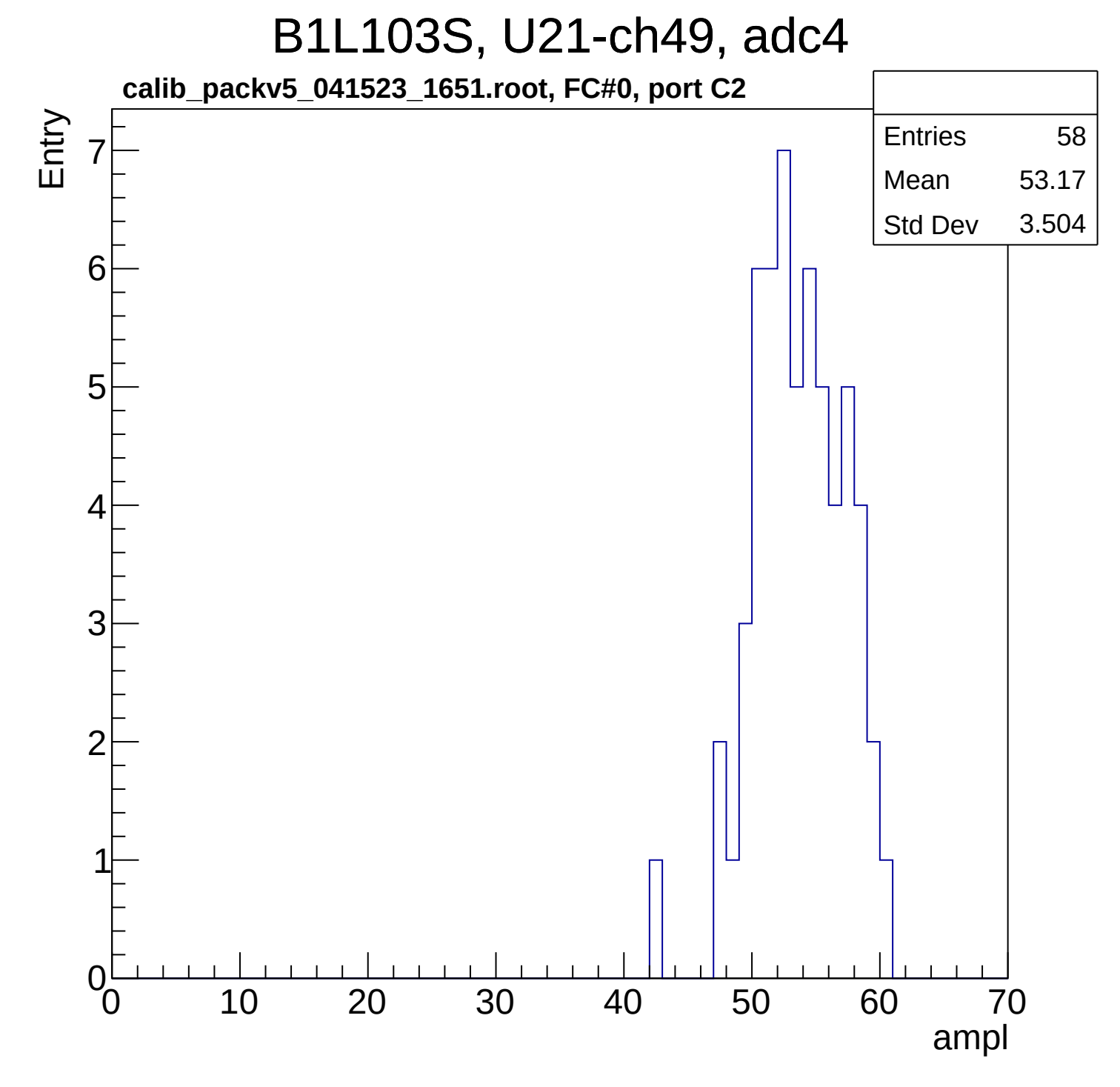
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U21-ch49, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 53.17
Std Dev 3.504
Entry
ampl
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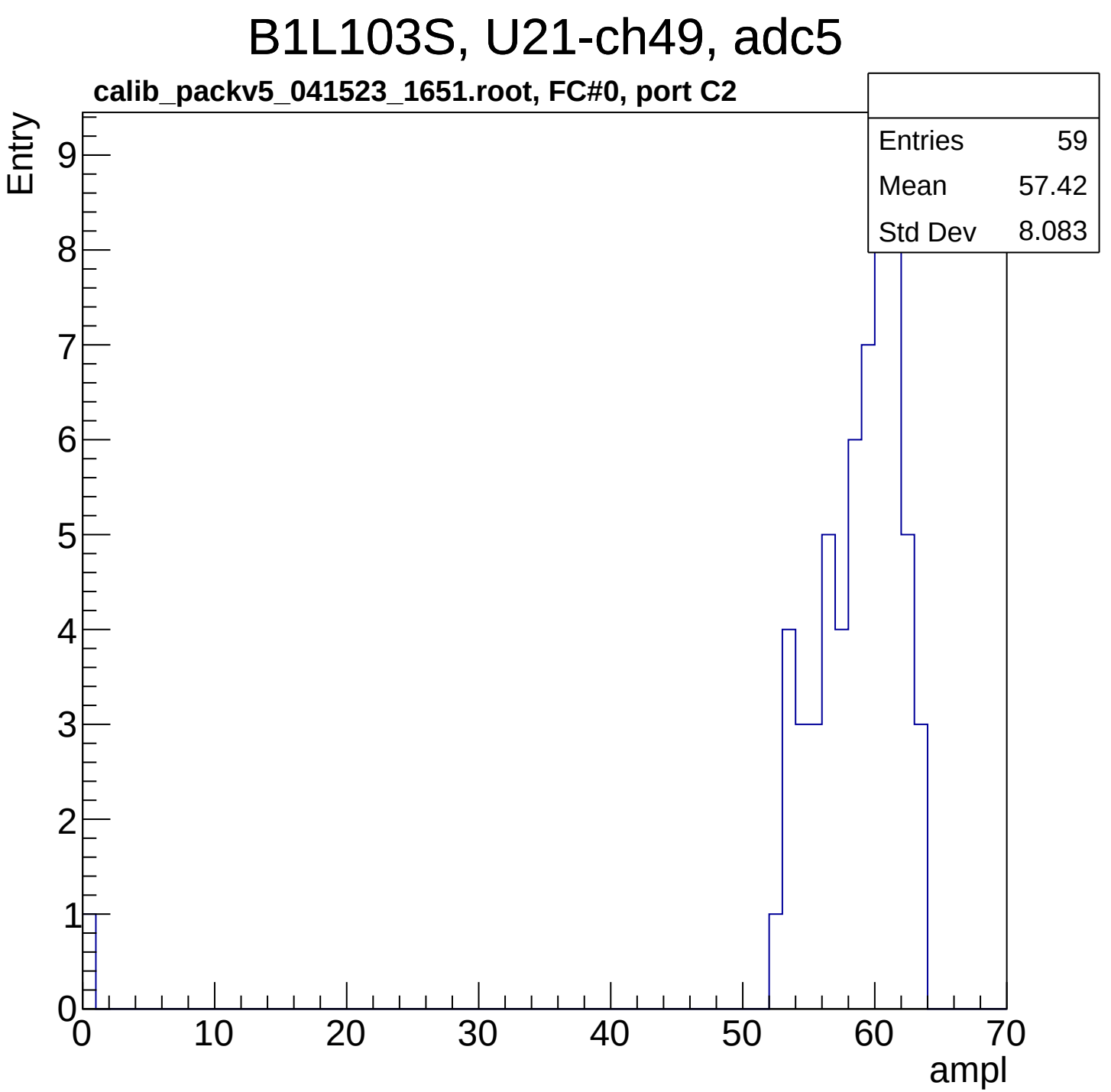
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U21-ch49, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 57.42
Std Dev 8.083
Entry
ampl
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2
3
4
5
6
7
8
9
0
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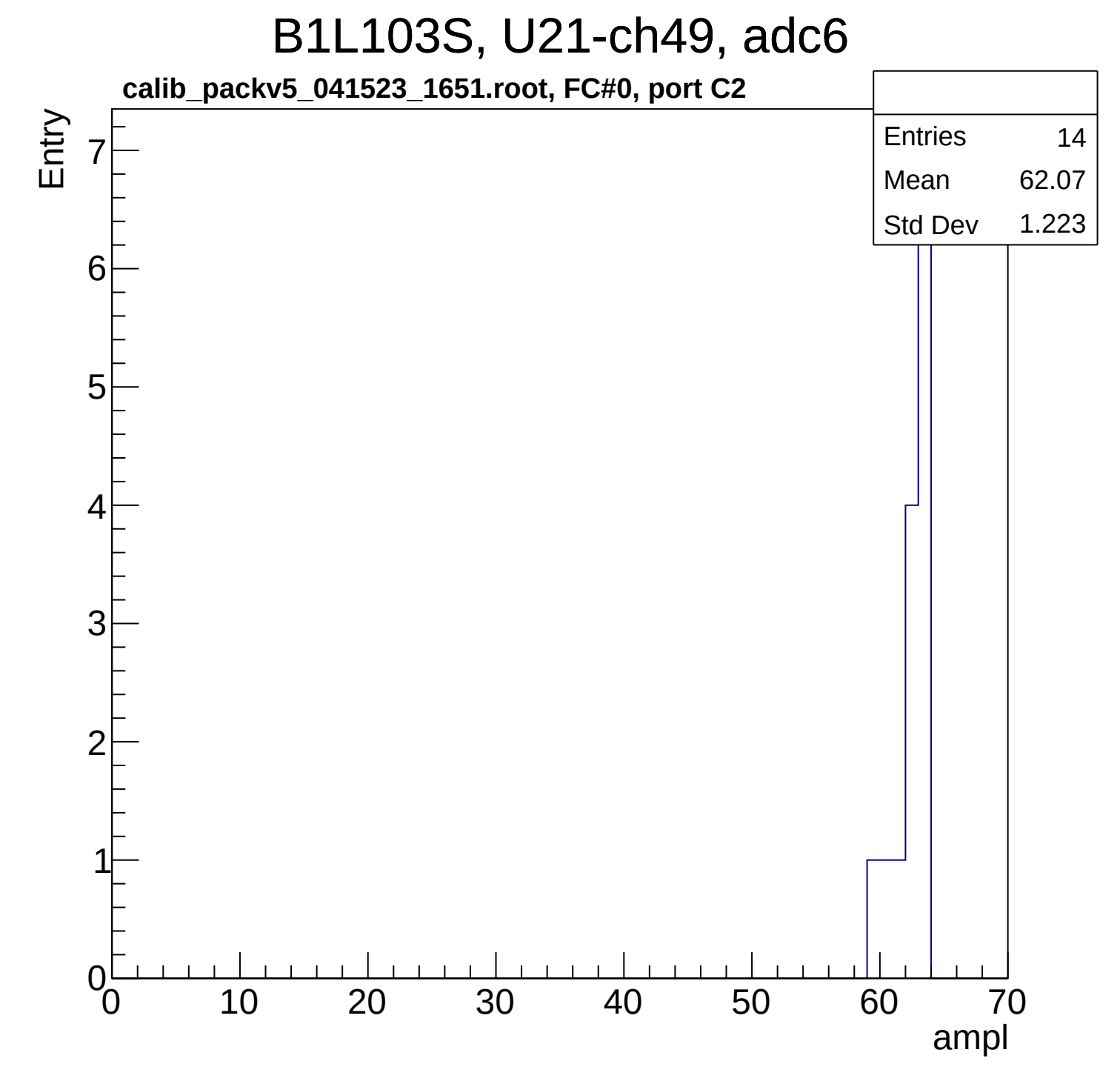
40
50
60
70


B1L103S, U21-ch49, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 62.07
Std Dev 1.223
Entry
ampl
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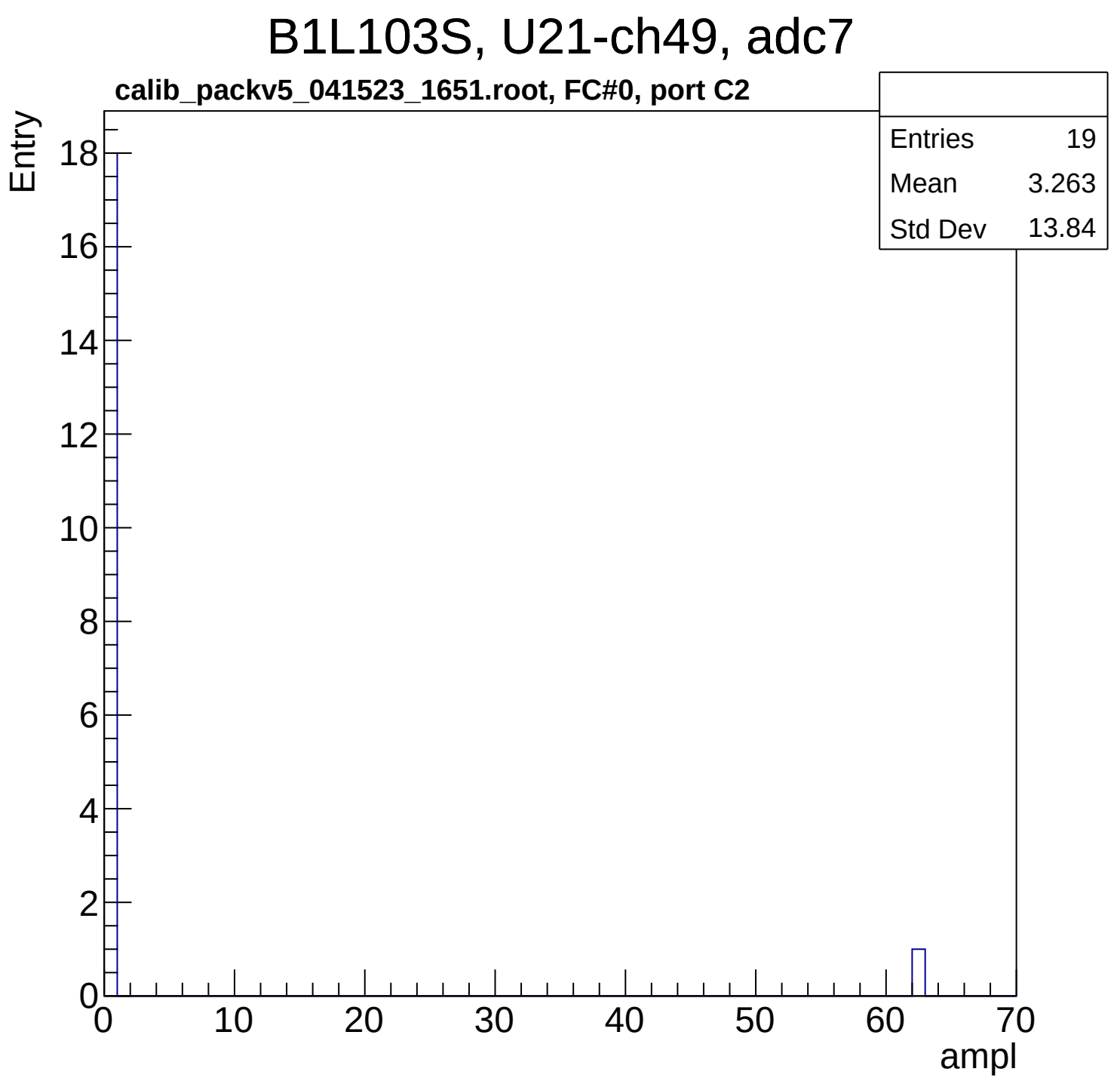
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U21-ch49, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.263
Std Dev 13.84
Entry
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6
8
10
12
14
16
18
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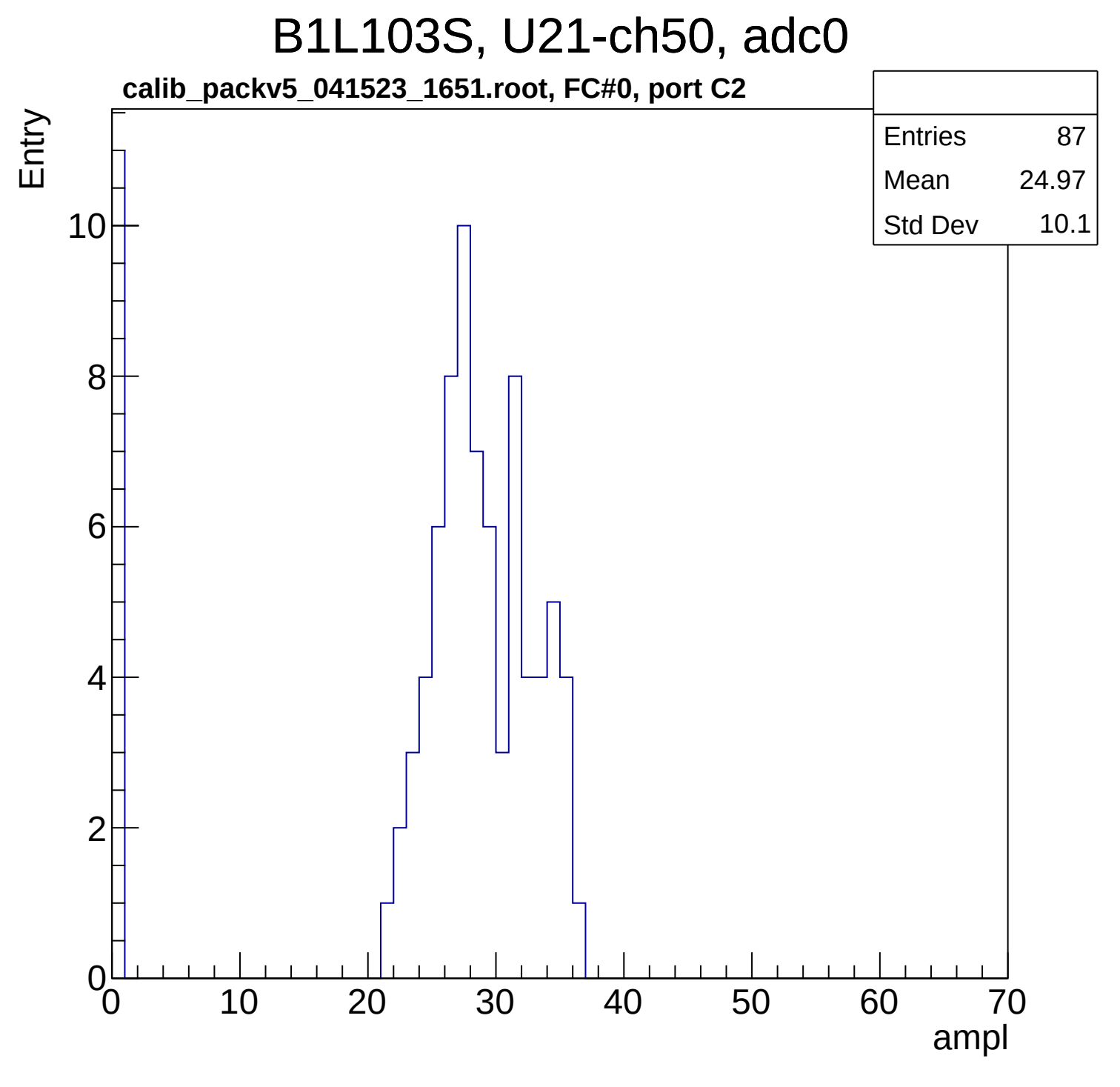
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch50, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 24.97
Std Dev 10.1
Entry
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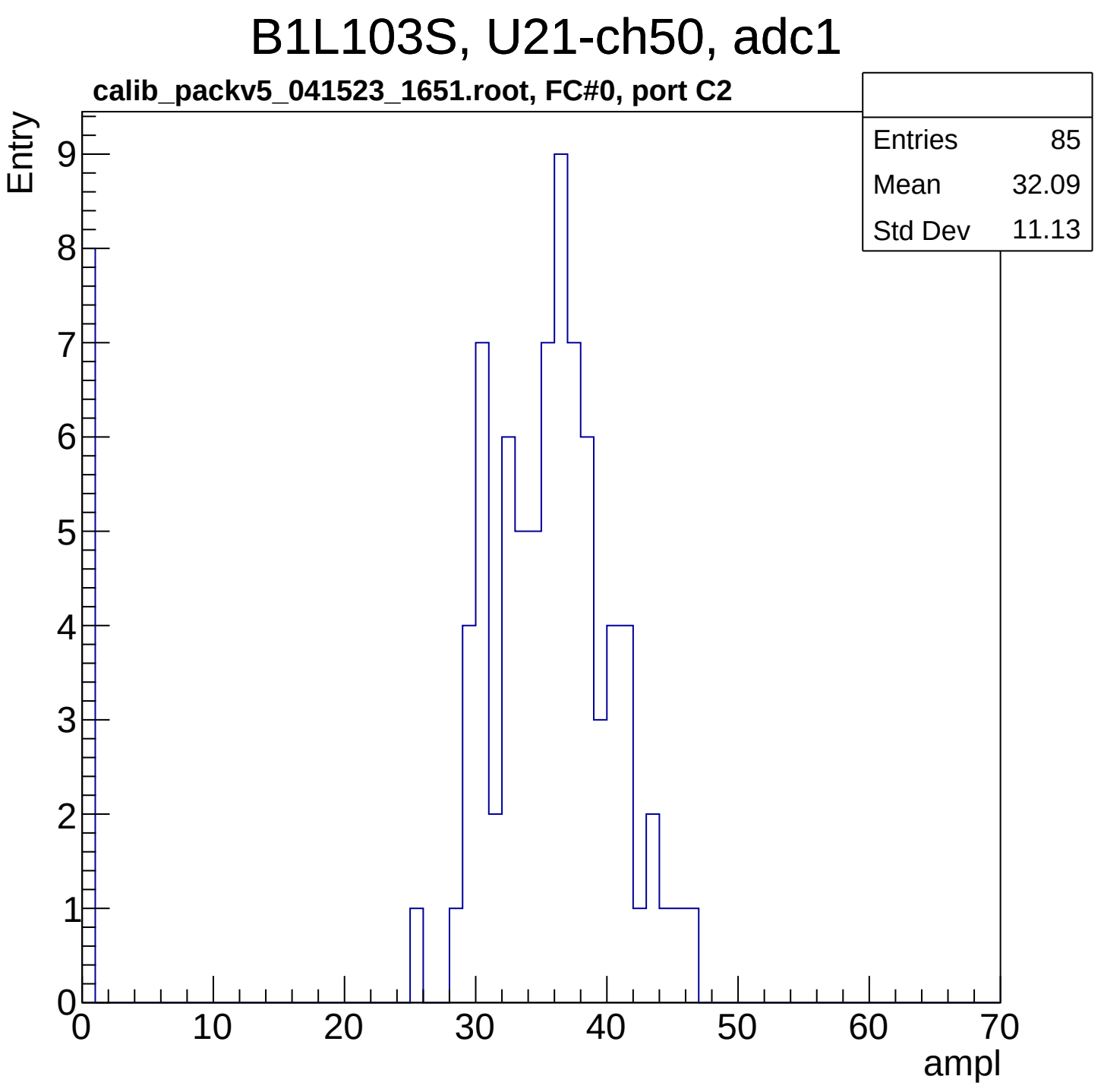
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch50, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 32.09
Std Dev 11.13
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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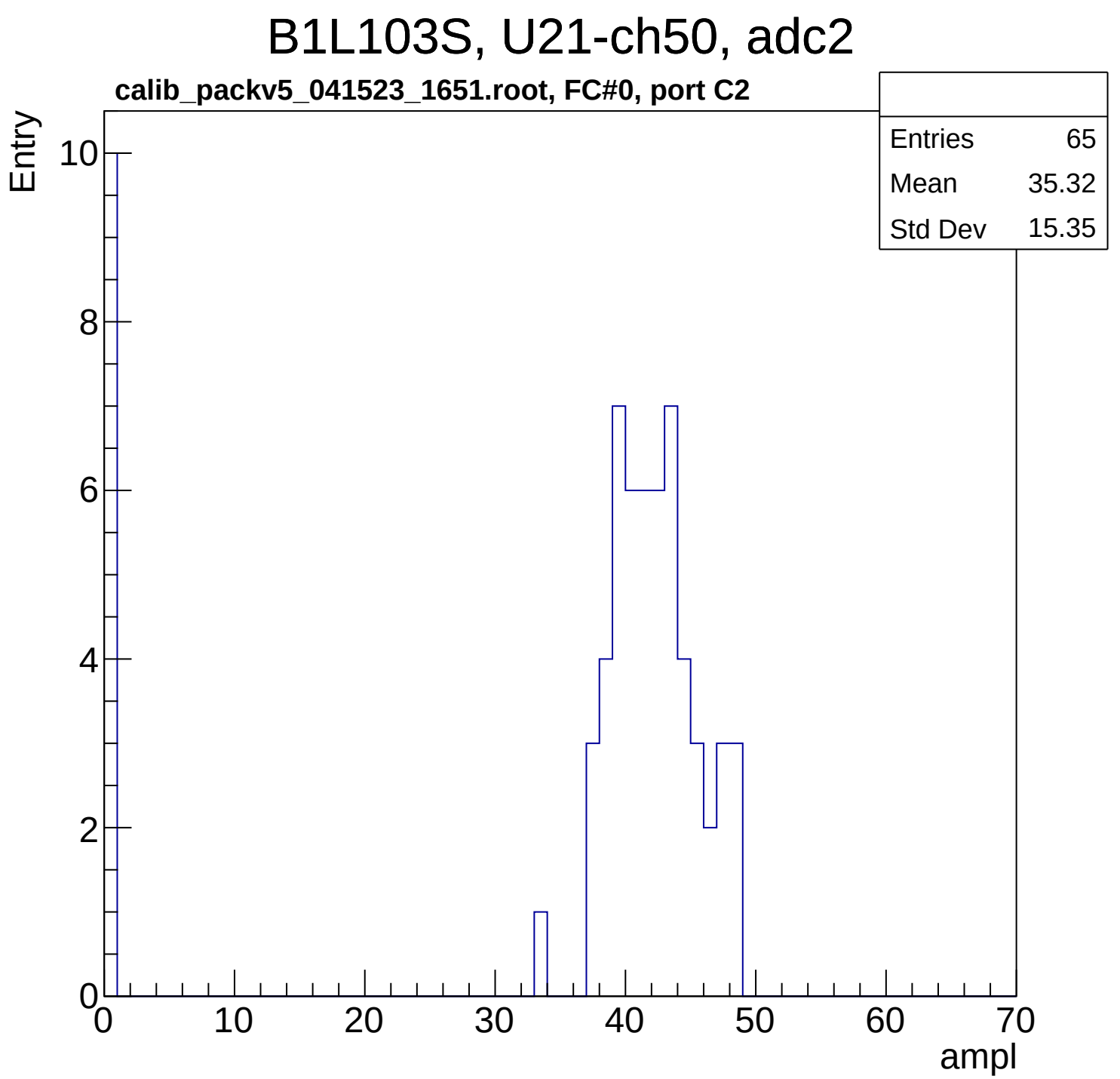
40
50
60
70


B1L103S, U21-ch50, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 35.32
Std Dev 15.35
Entry
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4
6
8
10
0
10
20
30
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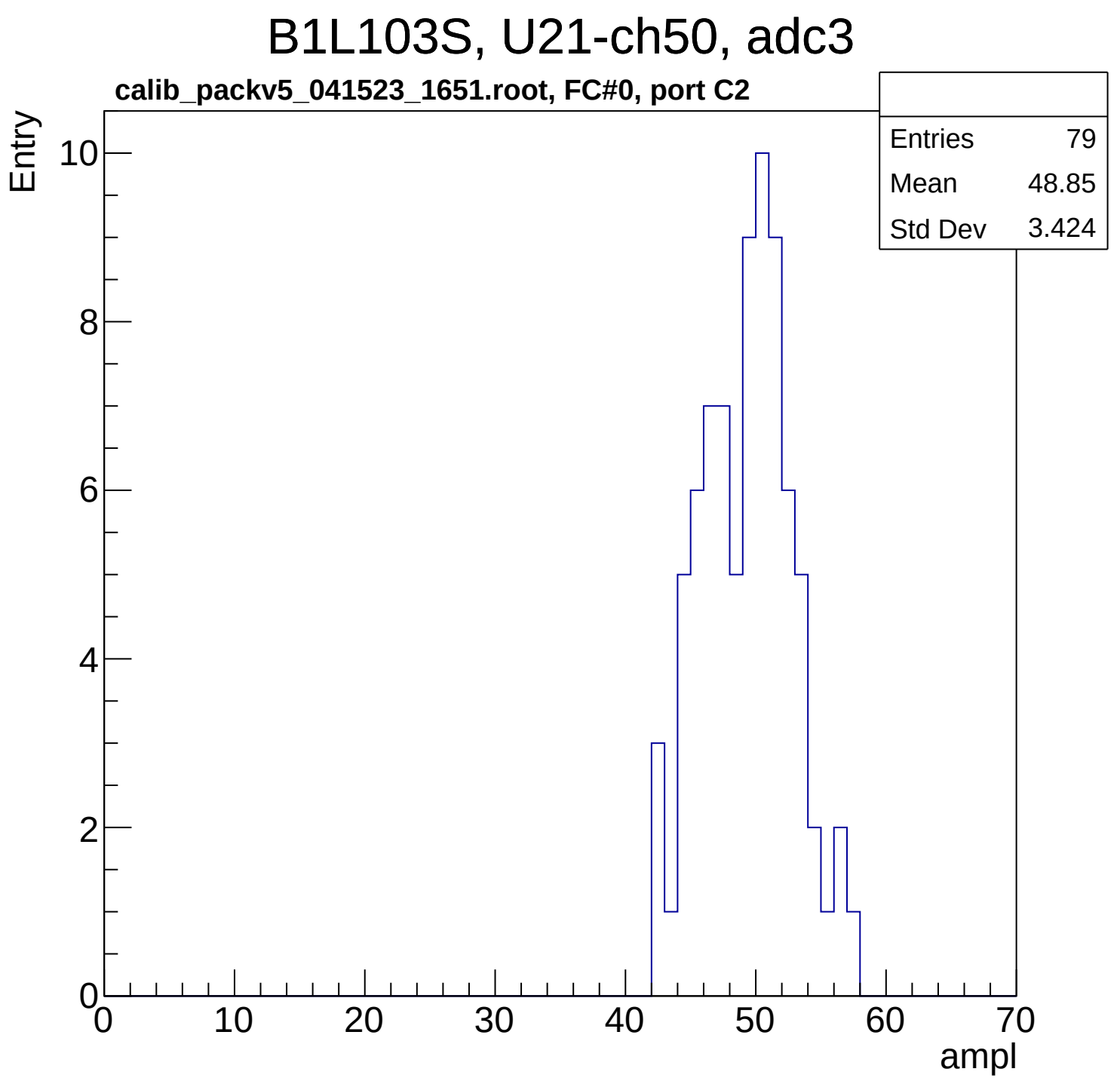
50
60
70
ampl


B1L103S, U21-ch50, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 48.85
Std Dev 3.424
Entry
ampl
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4
6
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0
10
20
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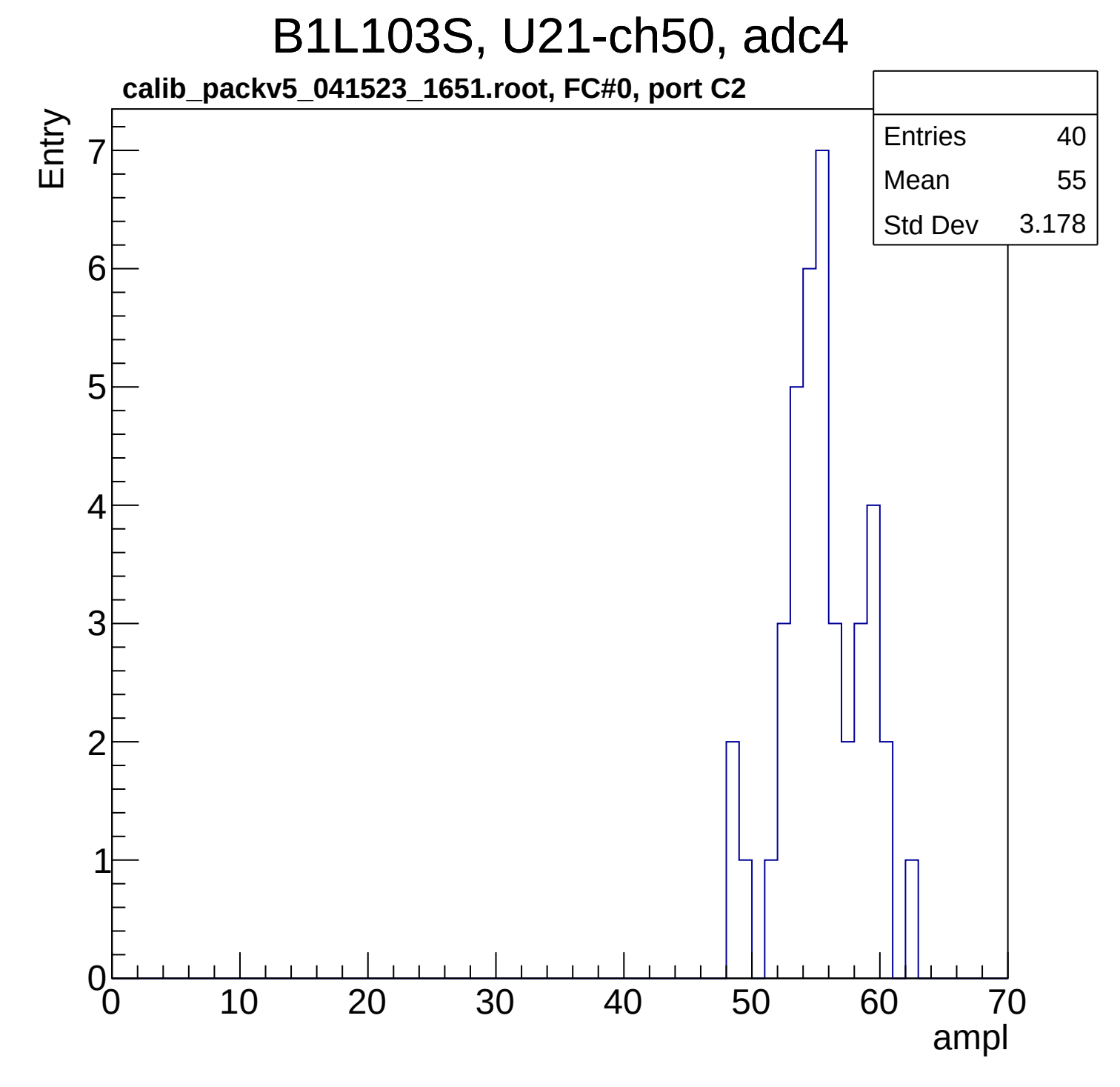
40
50
60
70


B1L103S, U21-ch50, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 55
Std Dev 3.178
Entry
ampl
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0
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40
50
60
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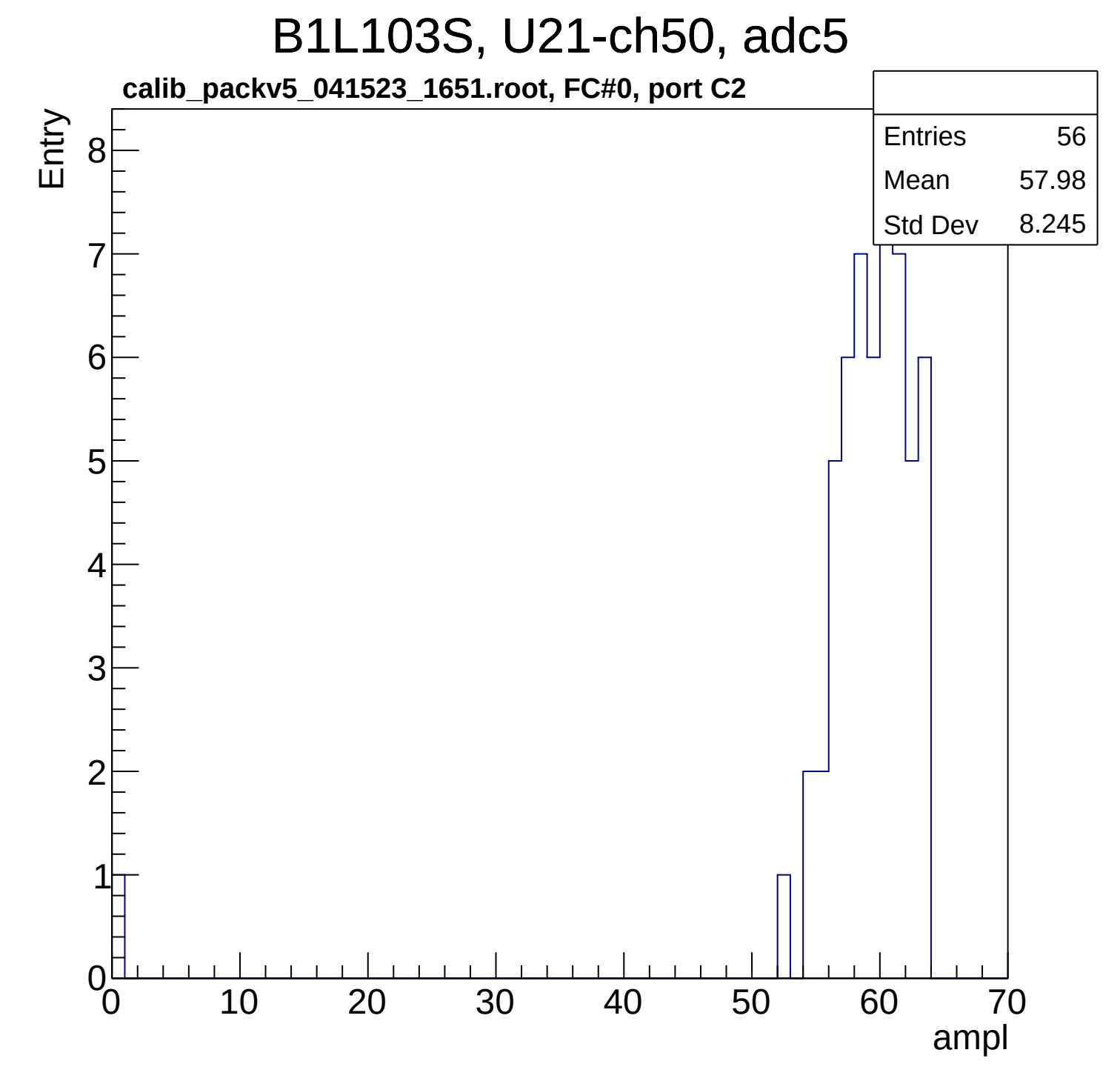
B1L103S, U21-ch50, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 57.98
Std Dev 8.245
Entry
ampl
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5
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7
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60
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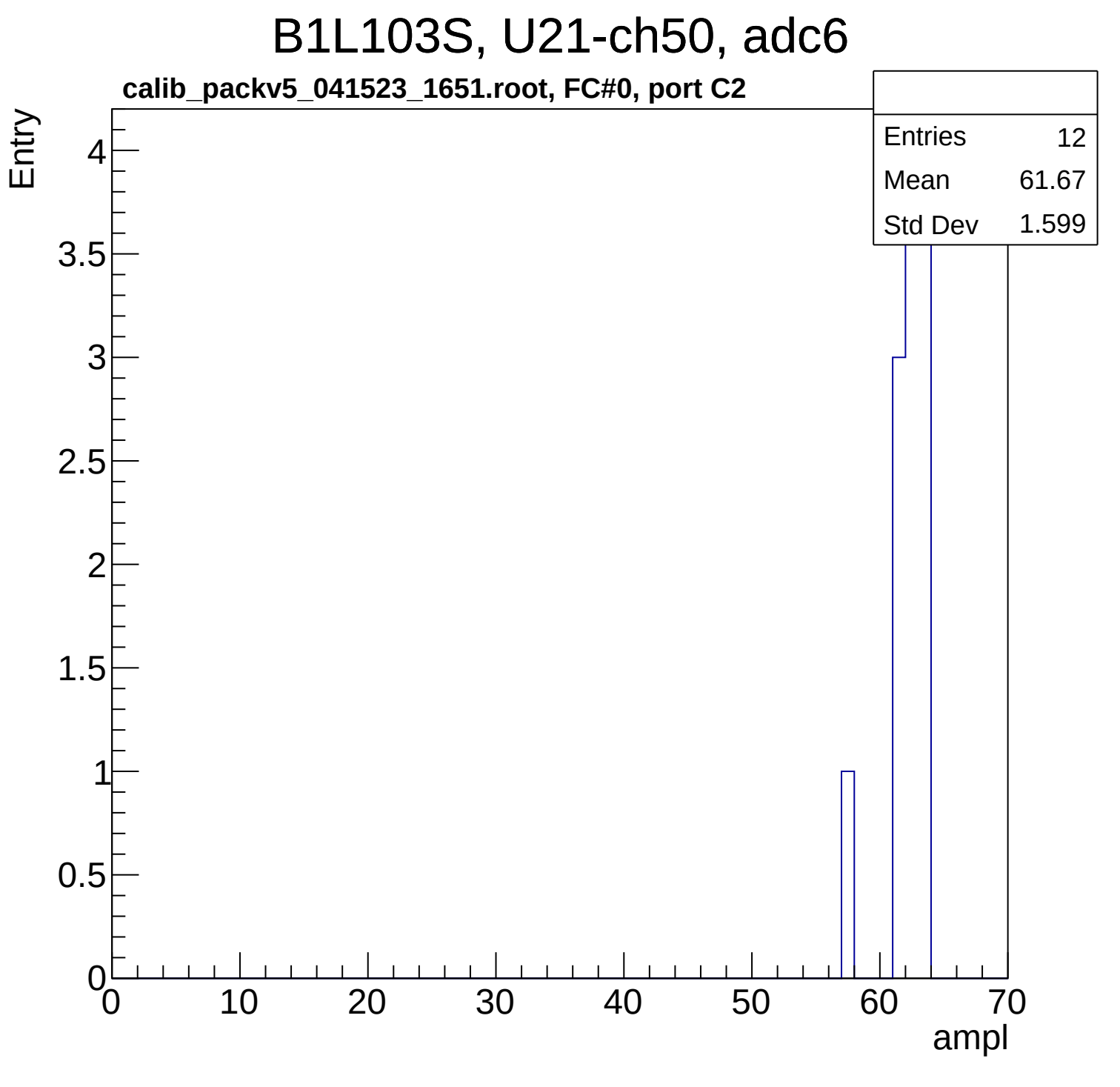
B1L103S, U21-ch50, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.67
Std Dev 1.599
Entry
ampl
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1.5
2
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3
3.5
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0
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60
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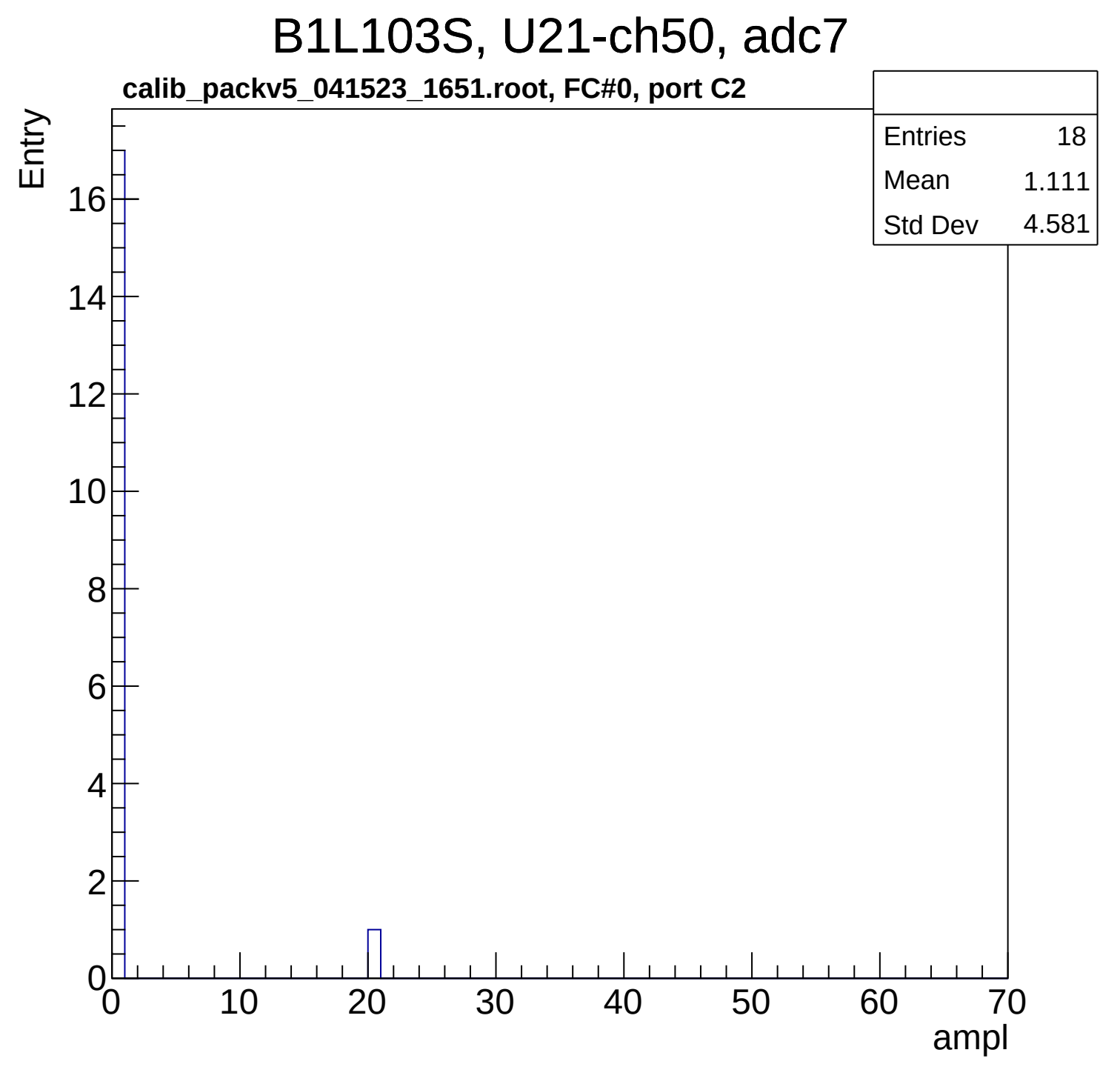
B1L103S, U21-ch50, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.111
Std Dev 4.581
Entry
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6
8
10
12
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16
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10
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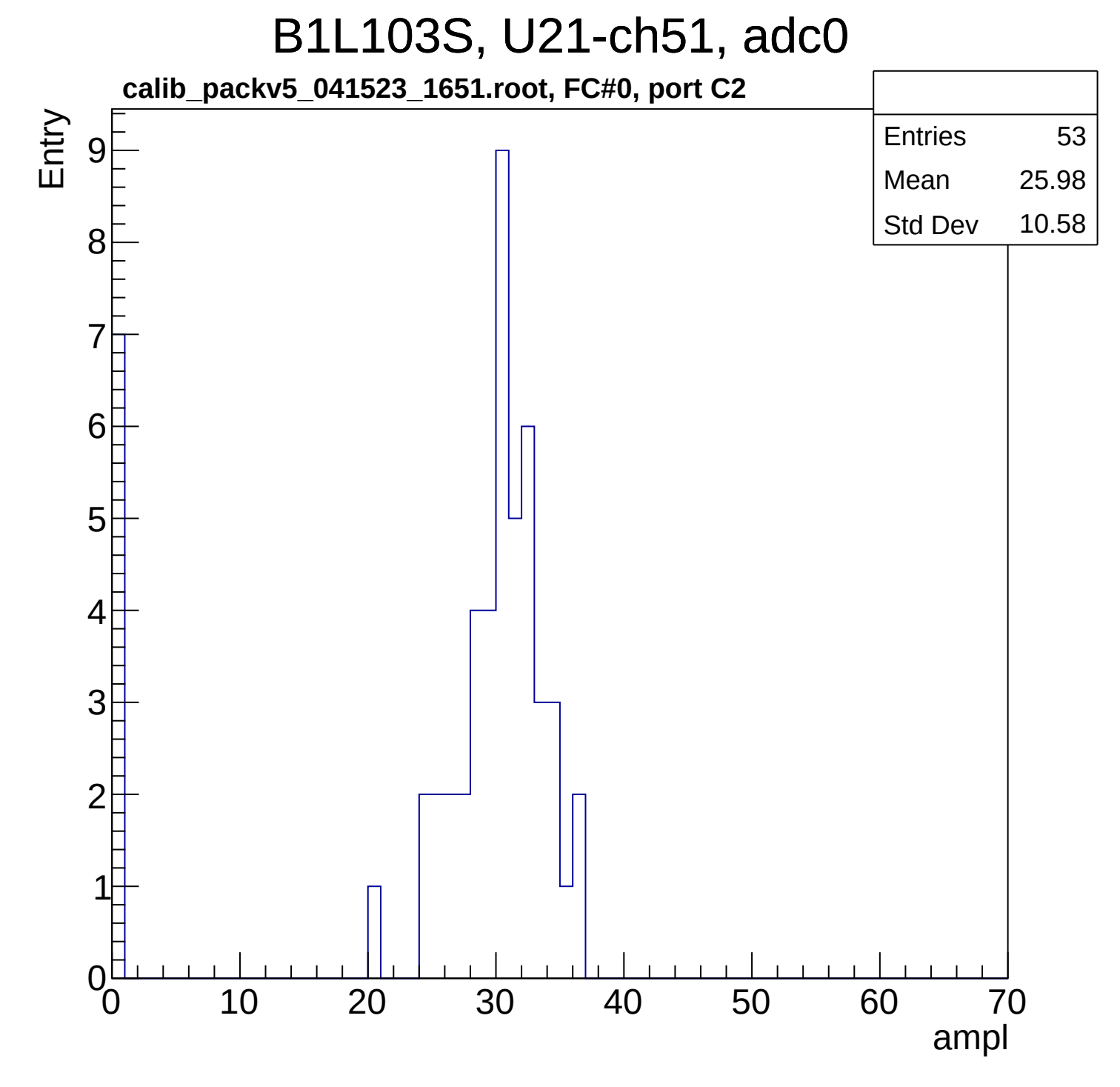
40
50
60
70
ampl


B1L103S, U21-ch51, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 25.98
Std Dev 10.58
Entry
ampl
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2
3
4
5
6
7
8
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0
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60
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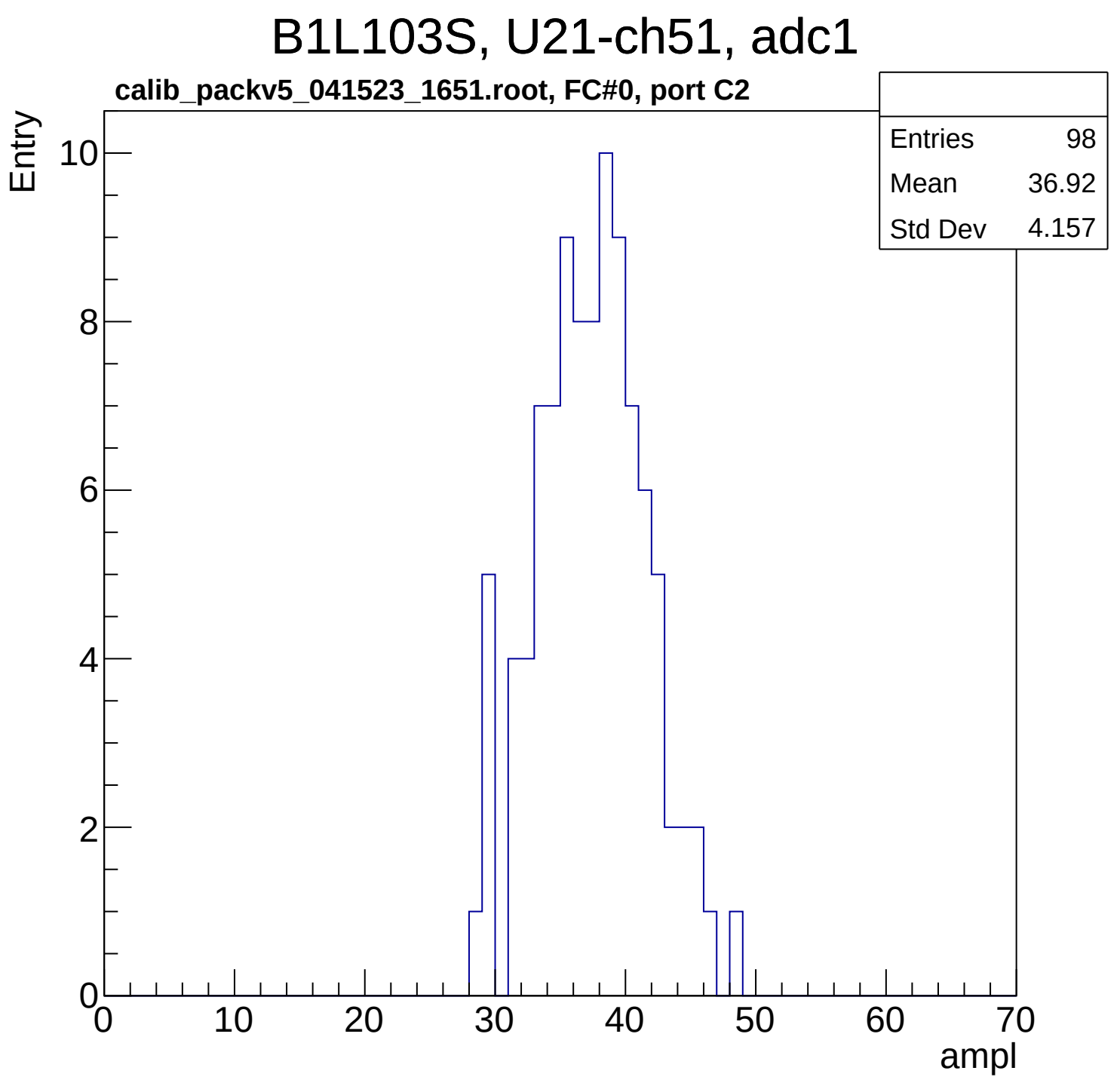
B1L103S, U21-ch51, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 98
Mean 36.92
Std Dev 4.157
Entry
0
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10
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10
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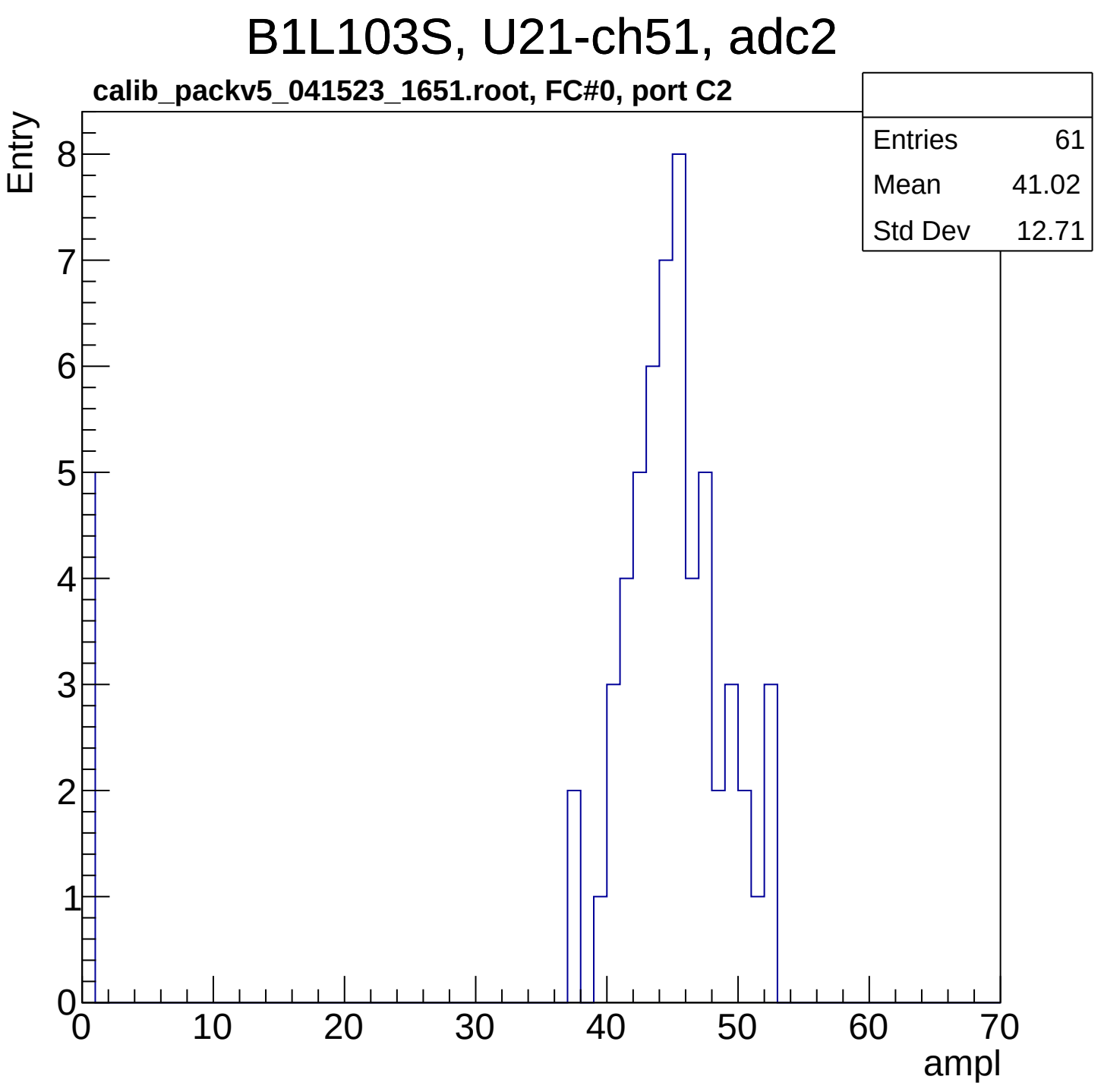
50
60
70
ampl


B1L103S, U21-ch51, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 41.02
Std Dev 12.71
Entry
ampl
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2
3
4
5
6
7
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0
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20
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40
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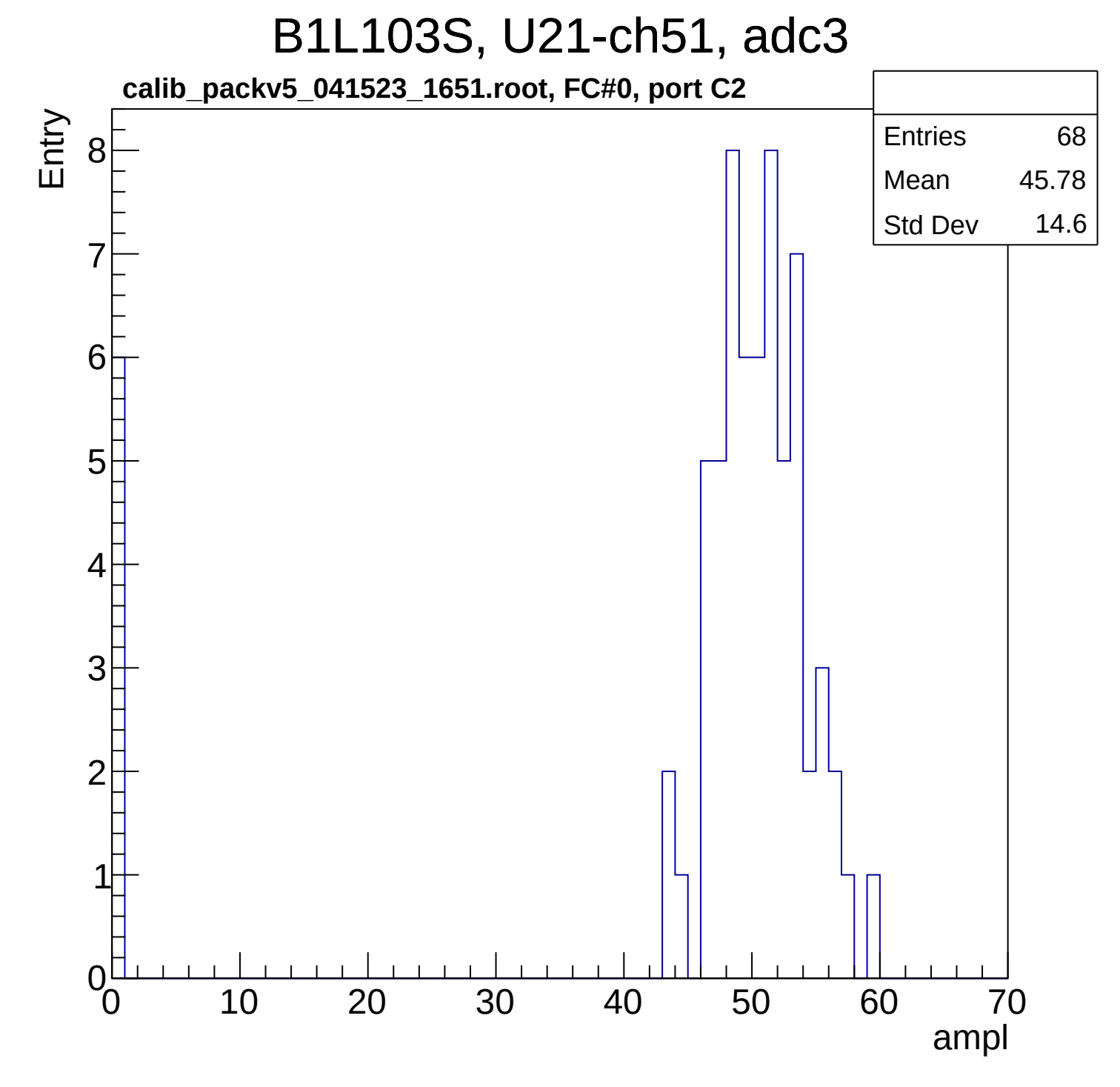
B1L103S, U21-ch51, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 45.78
Std Dev 14.6
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
50
60
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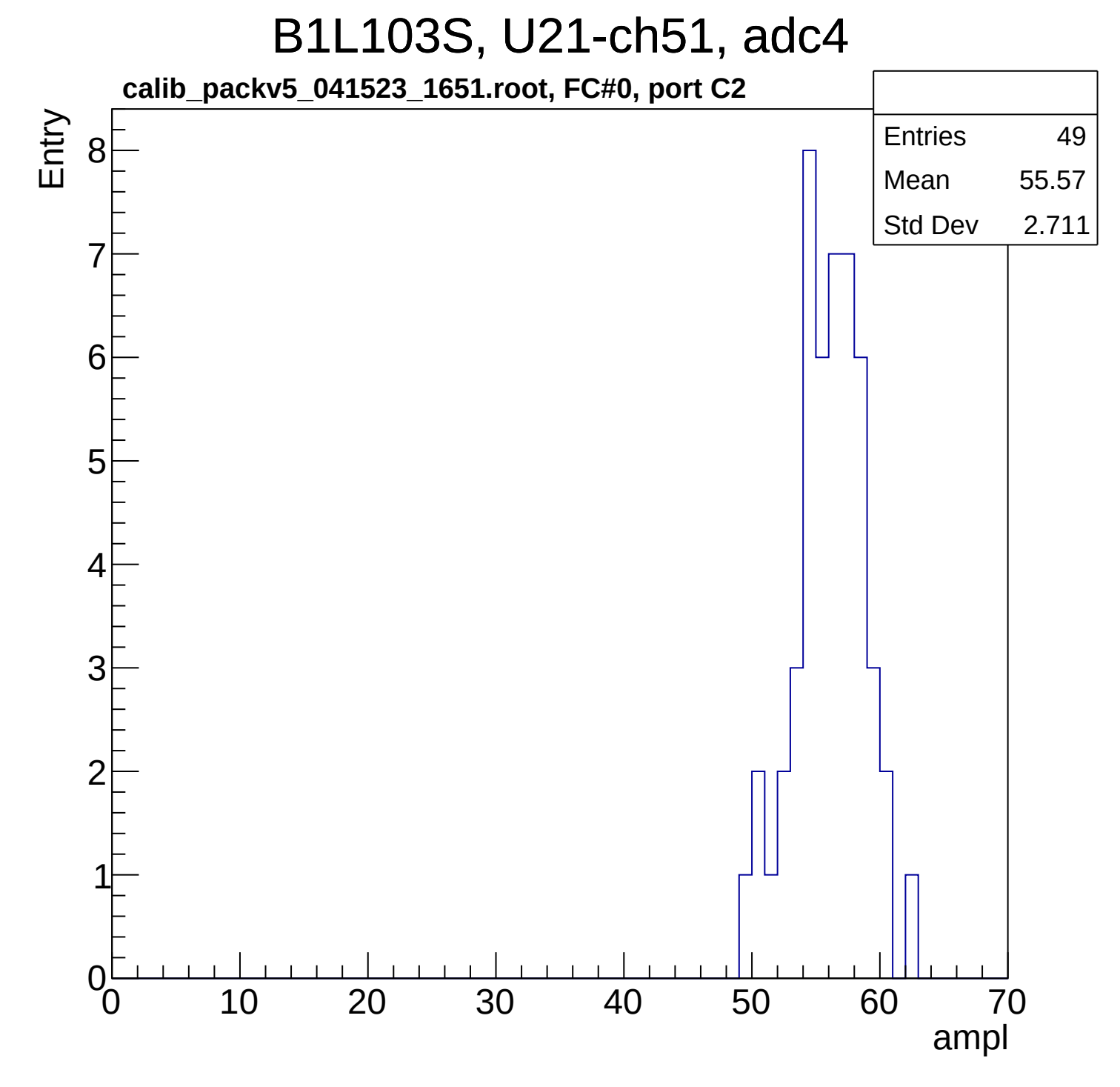
B1L103S, U21-ch51, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 55.57
Std Dev 2.711
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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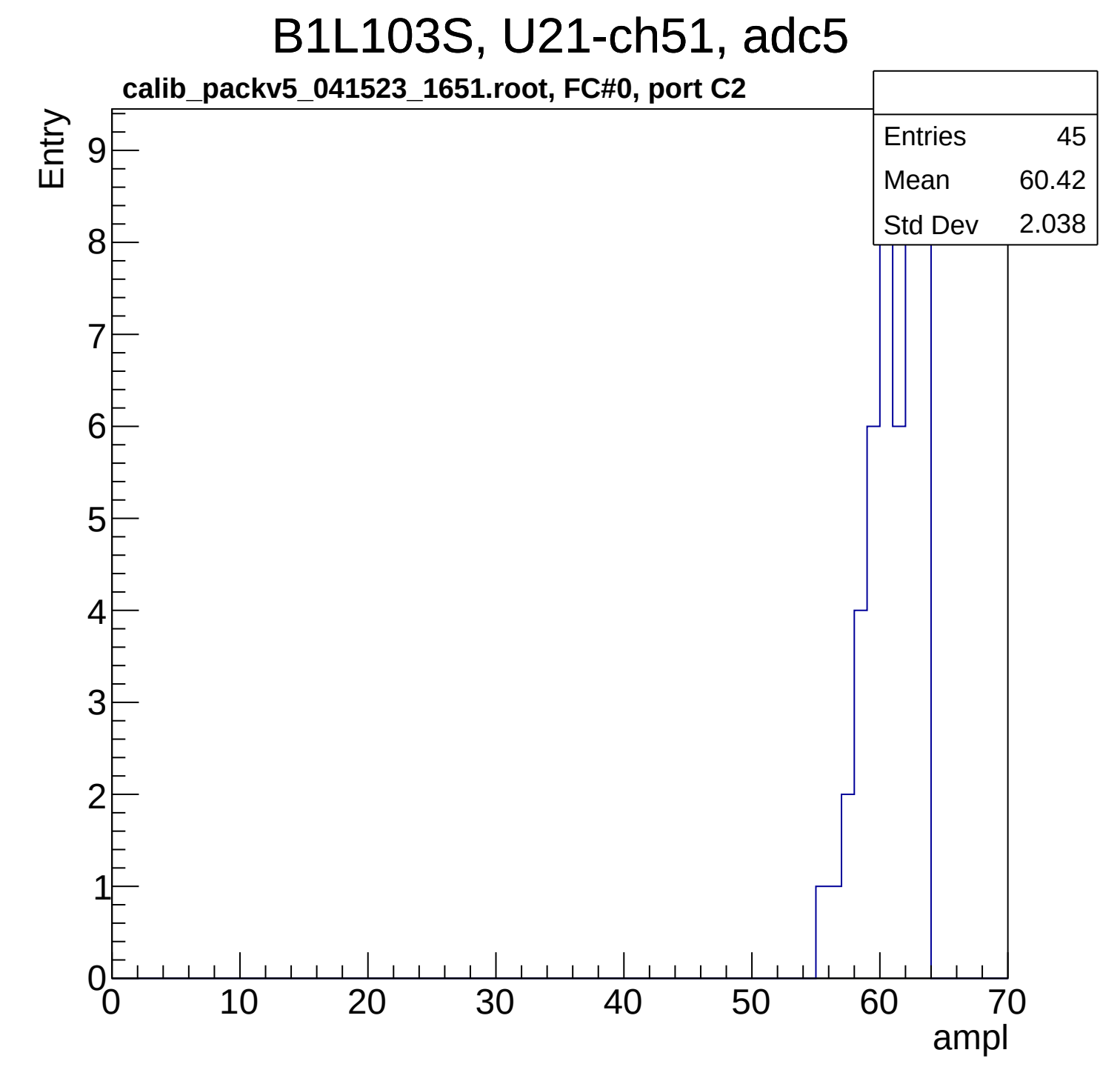
B1L103S, U21-ch51, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 60.42
Std Dev 2.038
Entry
ampl
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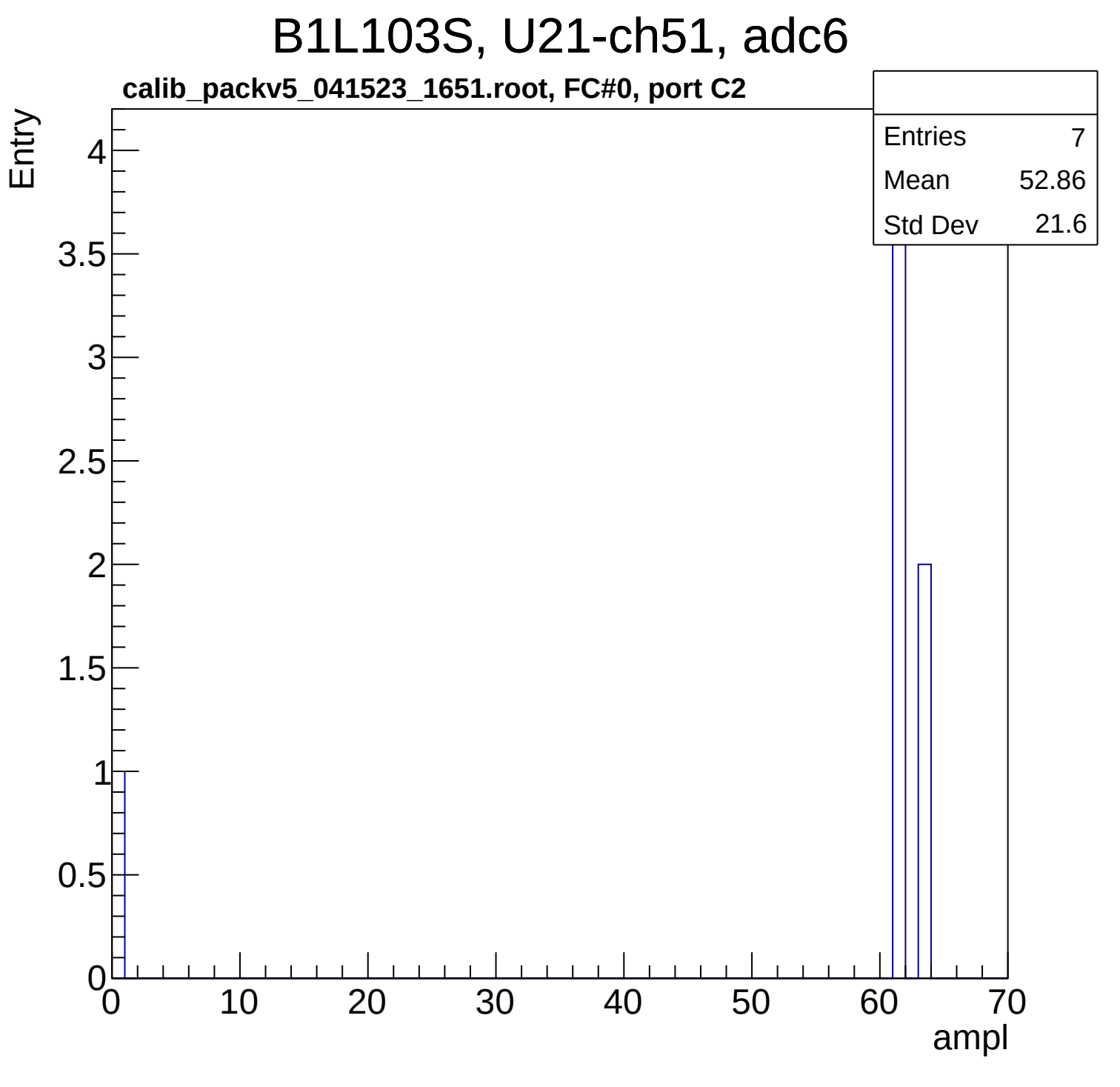
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch51, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 52.86
Std Dev 21.6
Entry
ampl
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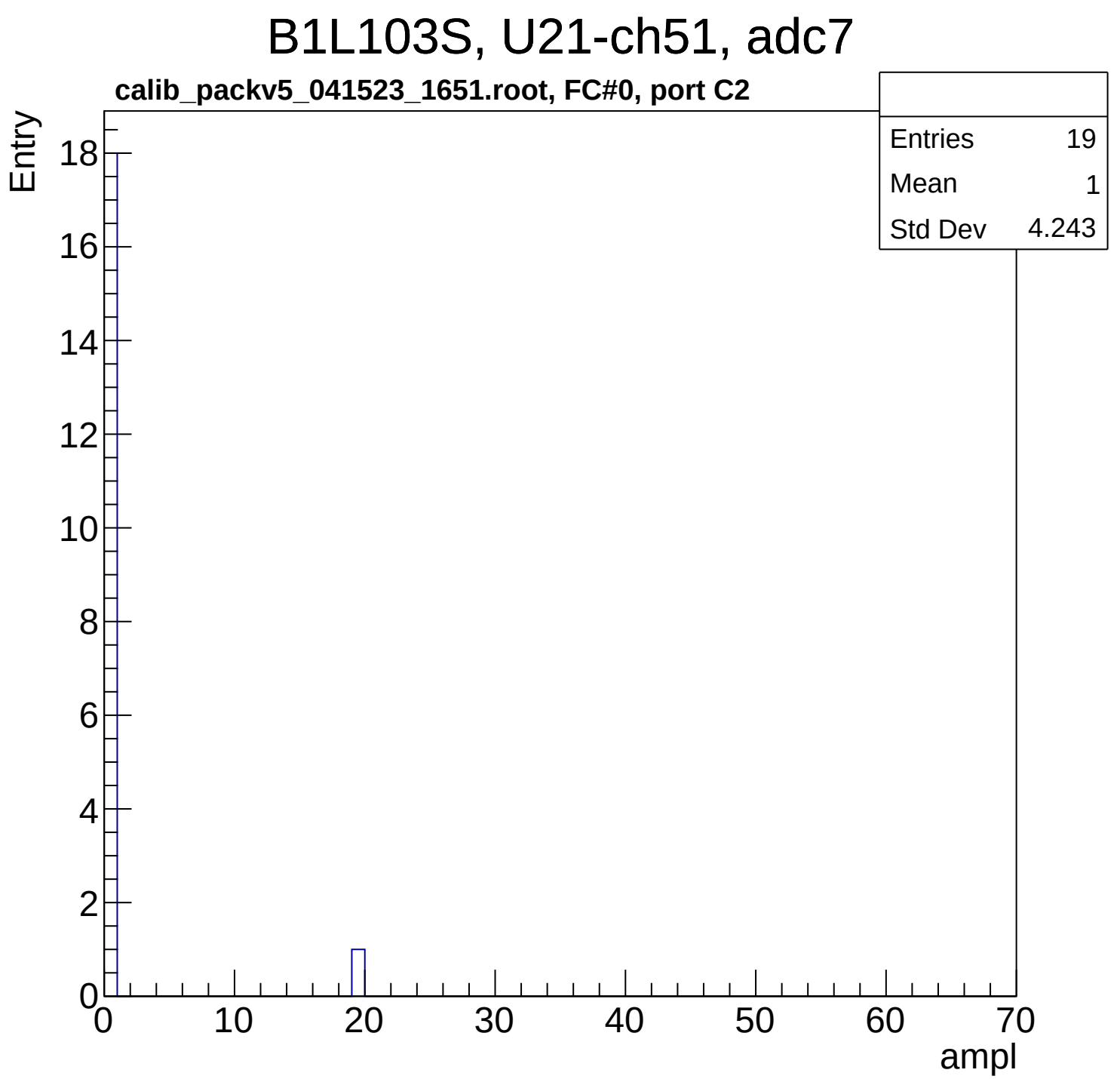
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U21-ch51, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1
Std Dev 4.243
Entry
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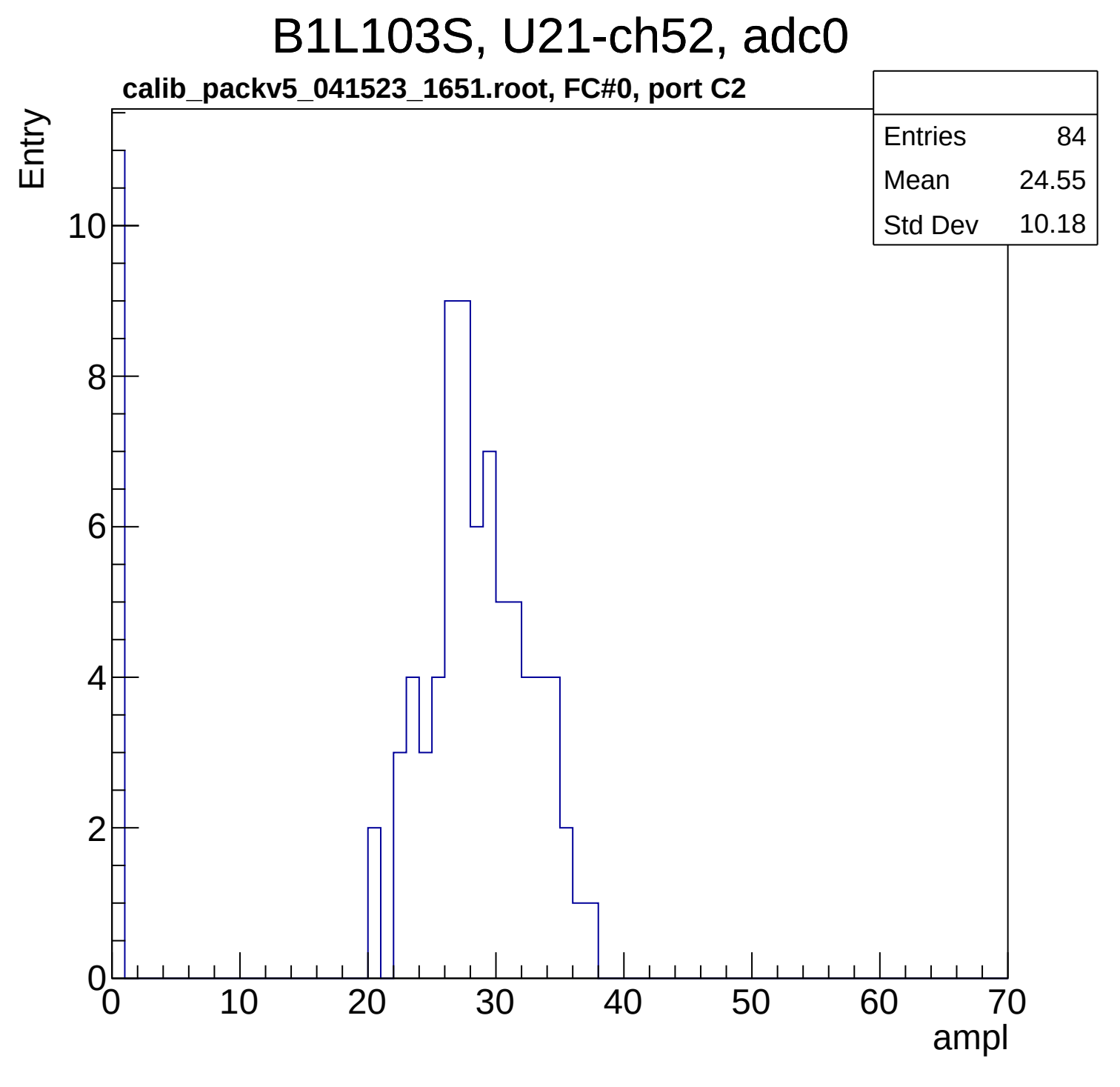
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch52, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 24.55
Std Dev 10.18
Entry
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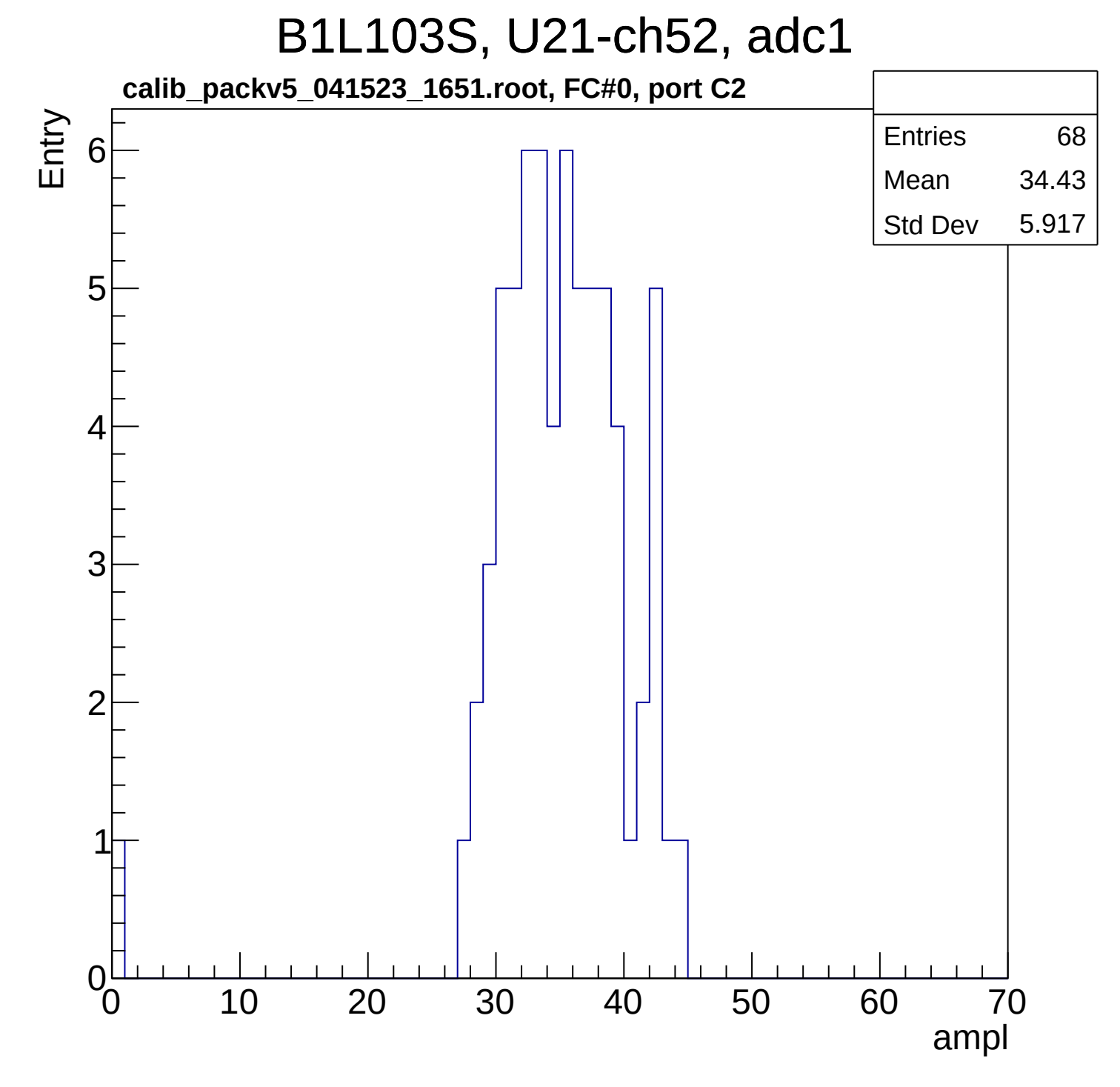
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch52, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 34.43
Std Dev 5.917
Entry
ampl
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1
2
3
4
5
6
0
10
20
30
40
50
60
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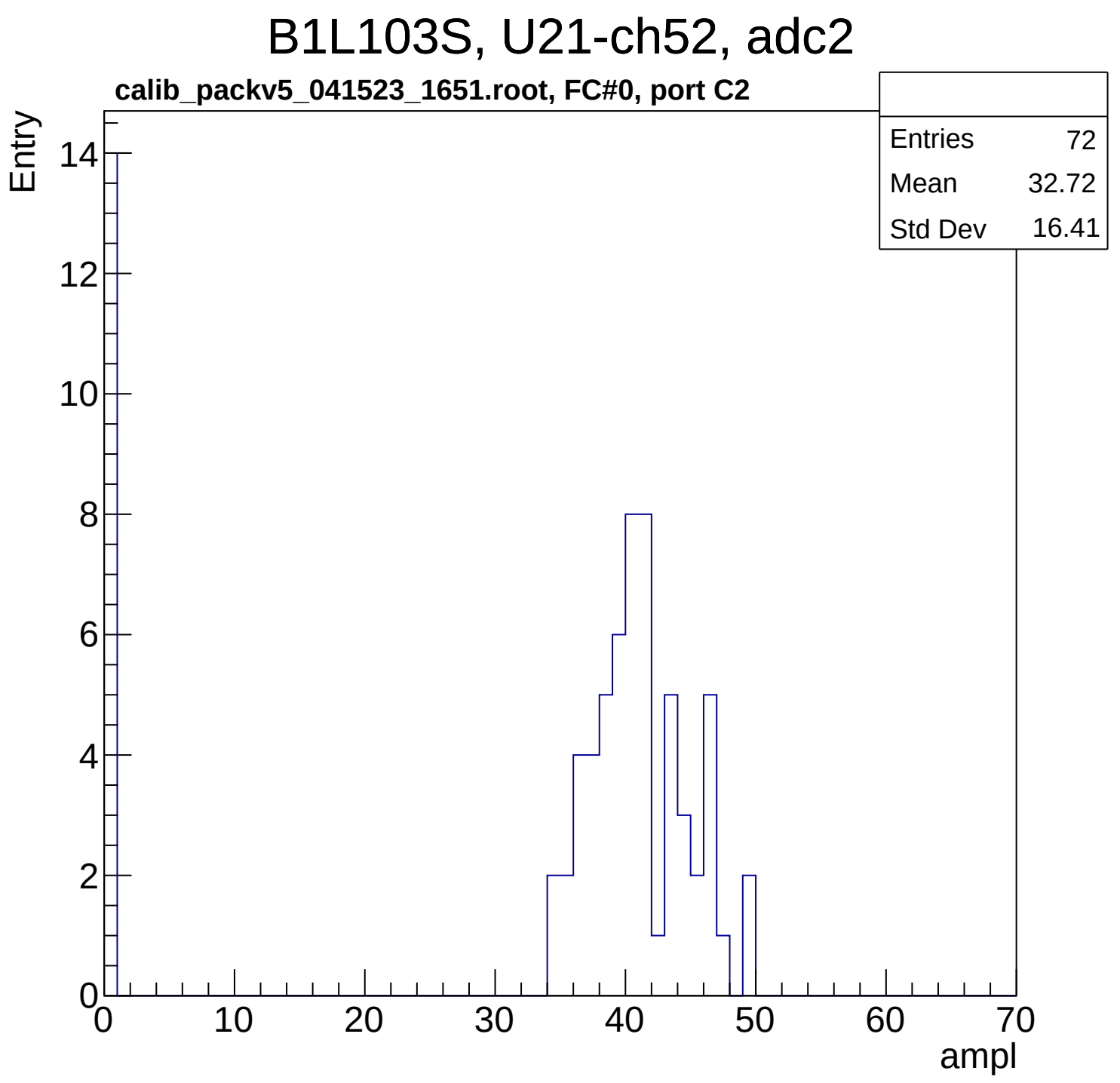
B1L103S, U21-ch52, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 32.72
Std Dev 16.41
Entry
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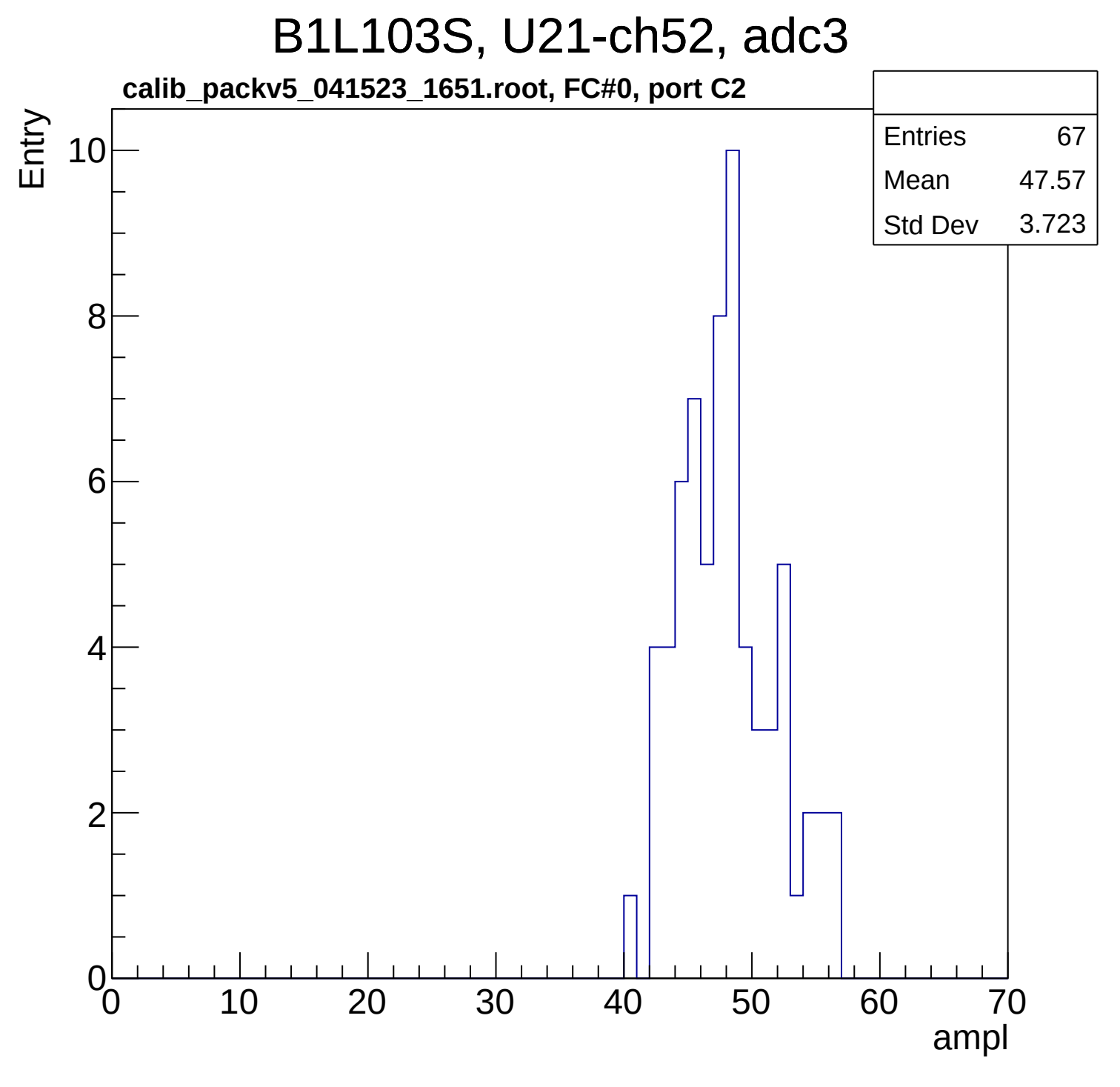
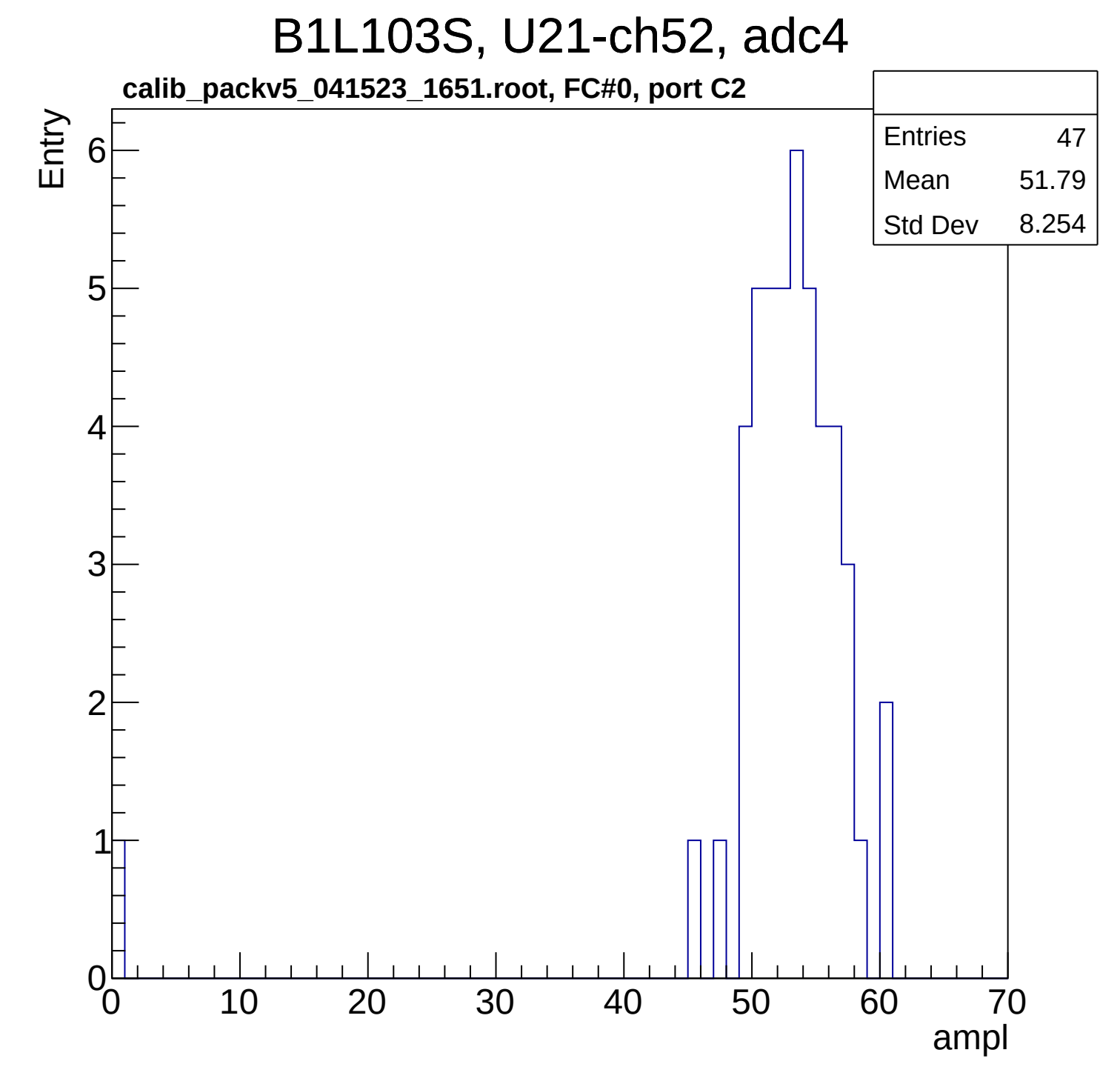
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch52, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 47.57
Std Dev 3.723
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U21-ch52, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 51.79
Std Dev 8.254
Entry
ampl
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1
2
3
4
5
6
0
10
20
30
40
50
60
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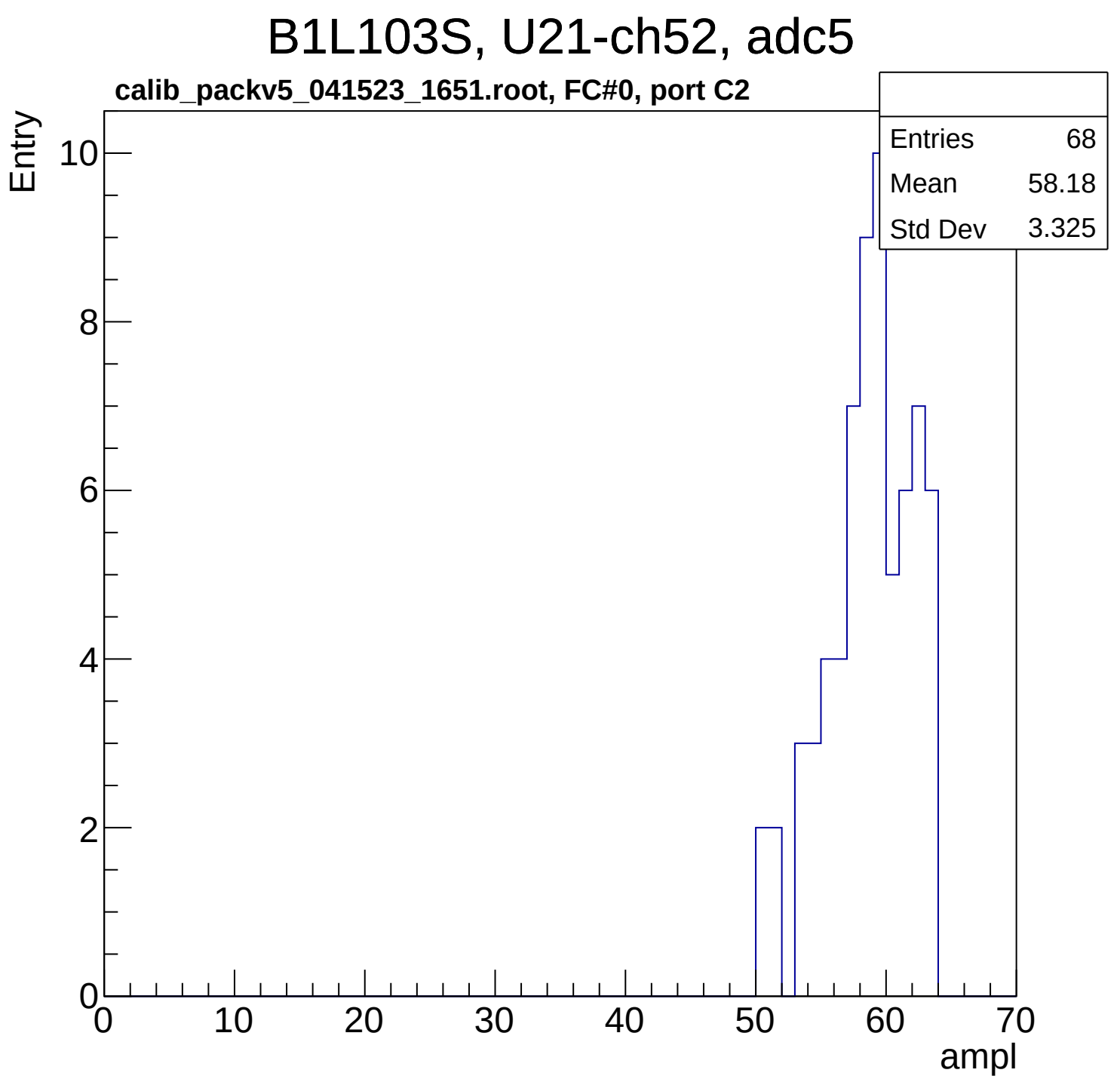
B1L103S, U21-ch52, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 58.18
Std Dev 3.325
Entry
ampl
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8
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0
10
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40
50
60
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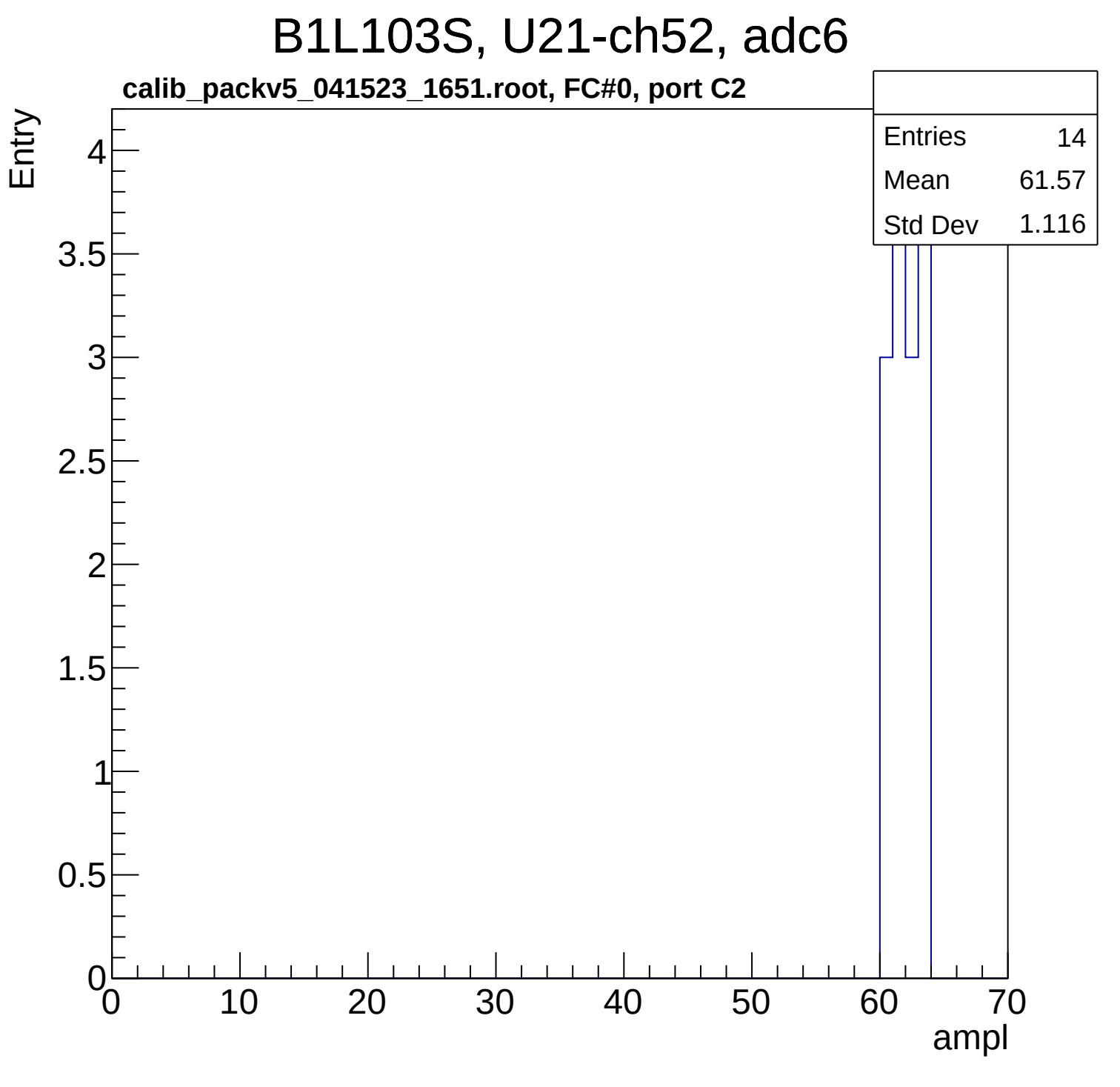
B1L103S, U21-ch52, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 61.57
Std Dev 1.116
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
10
20
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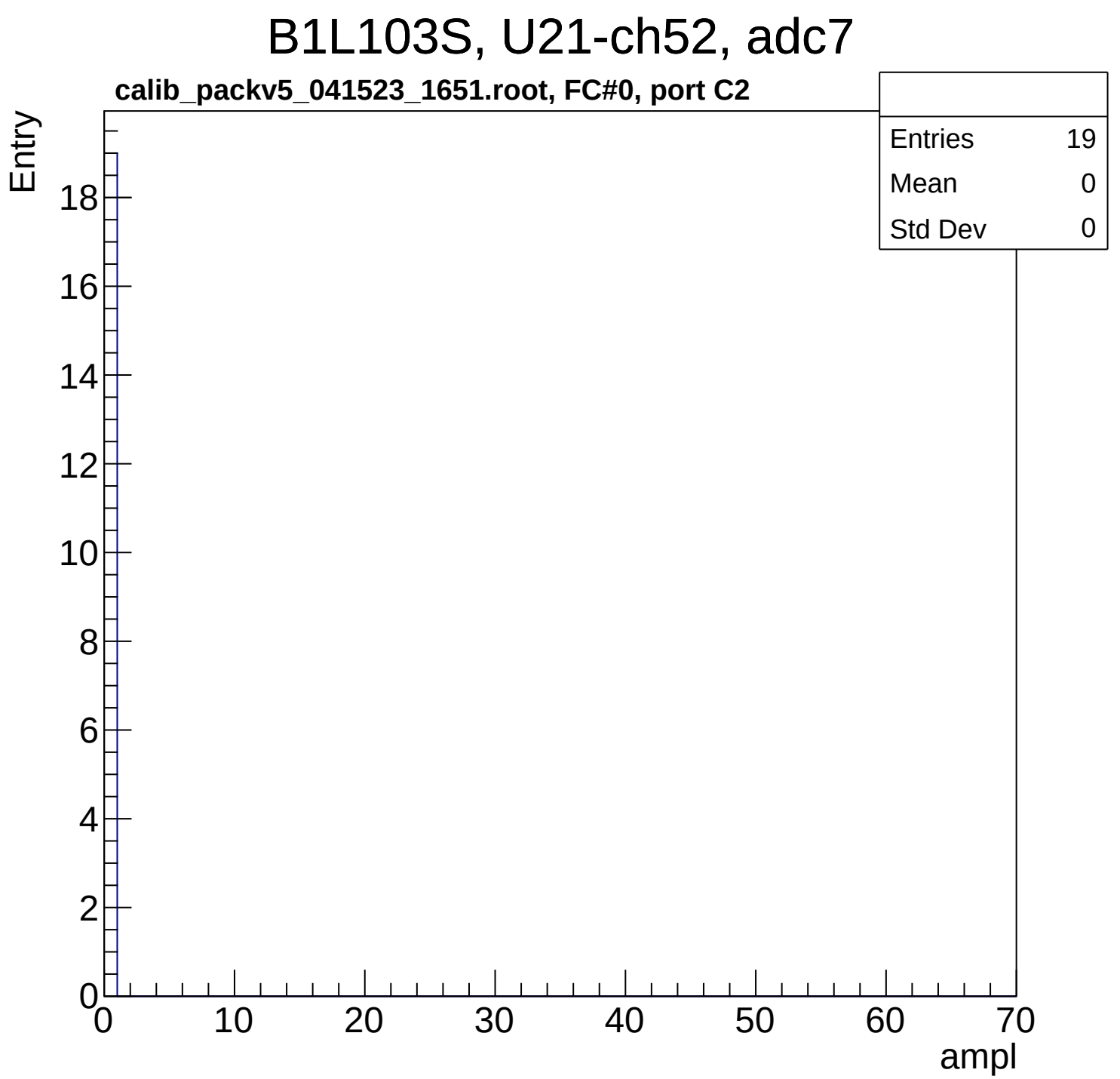
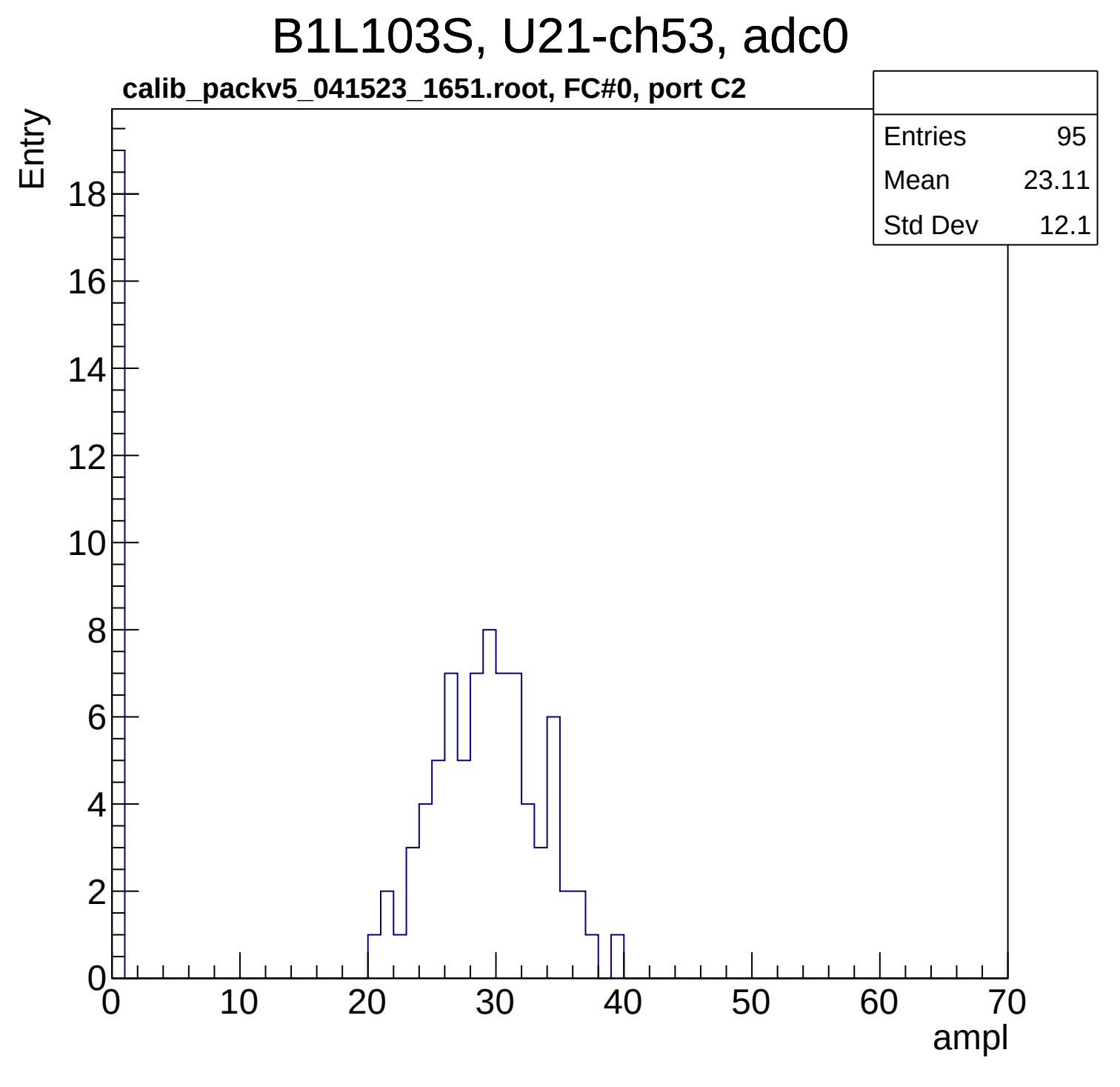
40
50
60
70


B1L103S, U21-ch52, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch53, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 23.11
Std Dev 12.1
Entry
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8
10
12
14
16
18
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10
20
30
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50
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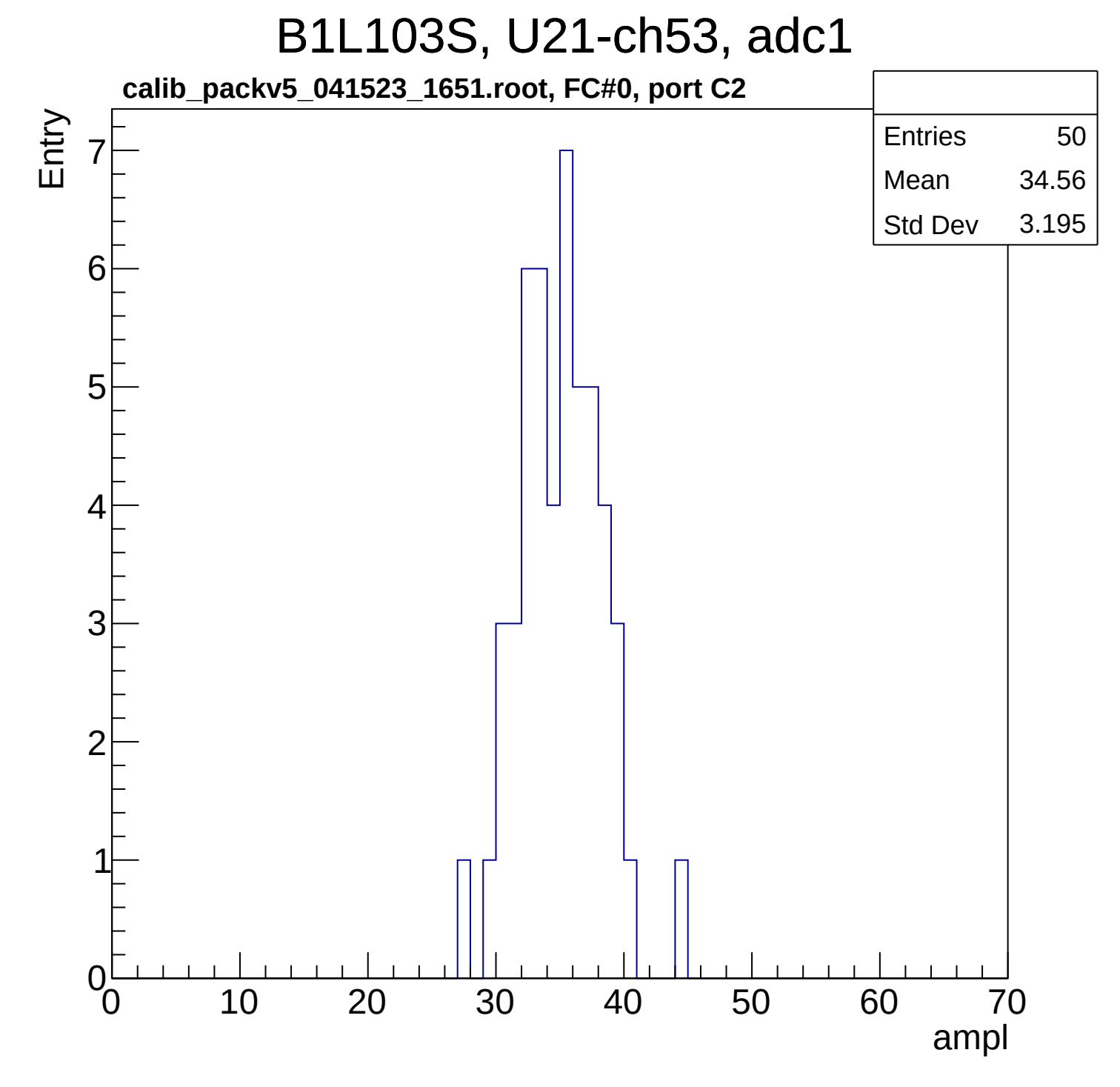
70
ampl


B1L103S, U21-ch53, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 34.56
Std Dev 3.195
Entry
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3
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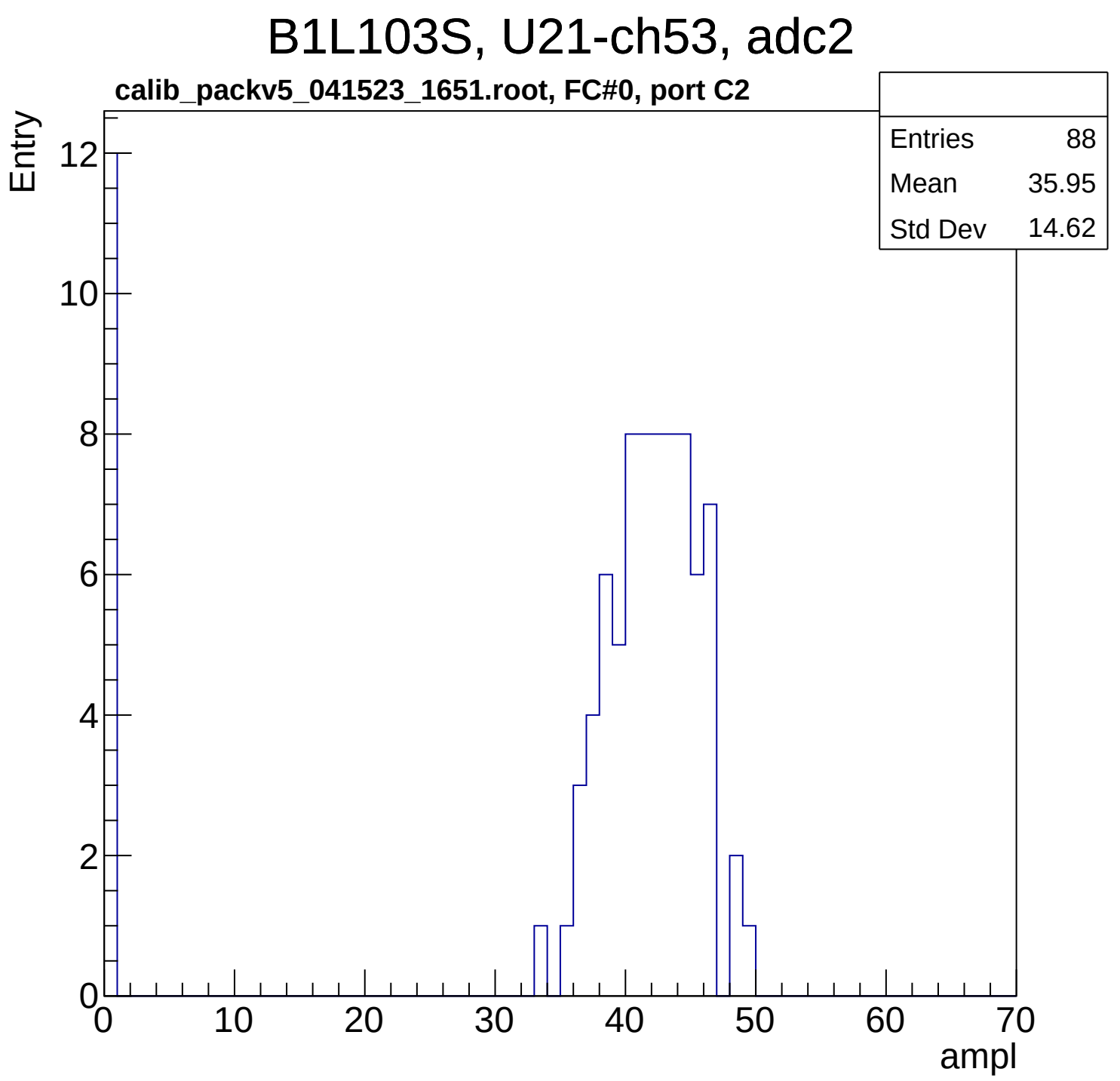
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch53, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 35.95
Std Dev 14.62
Entry
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6
8
10
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10
20
30
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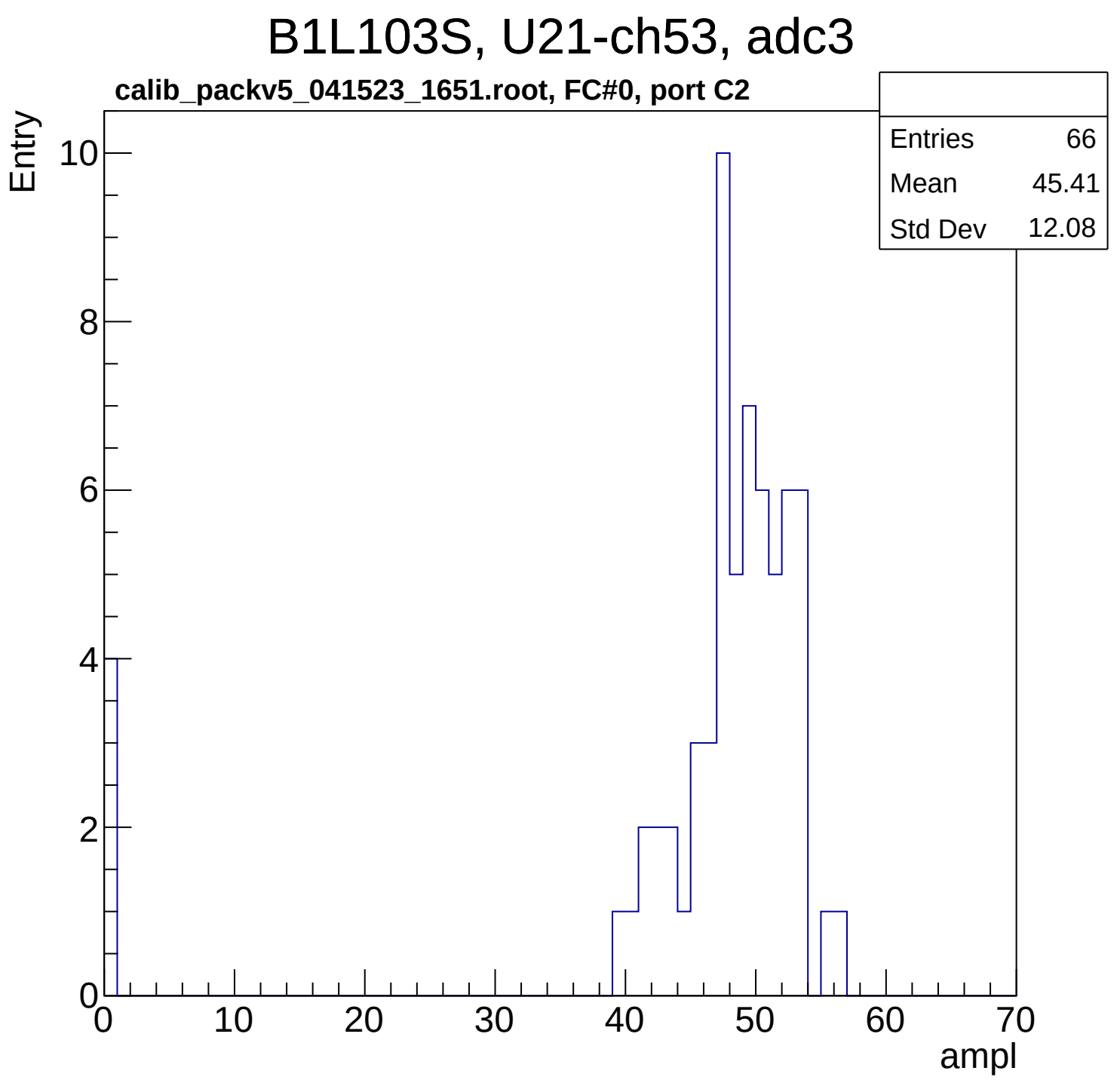
50
60
70
ampl


B1L103S, U21-ch53, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 45.41
Std Dev 12.08
Entry
ampl
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4
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8
10
0
10
20
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40
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60
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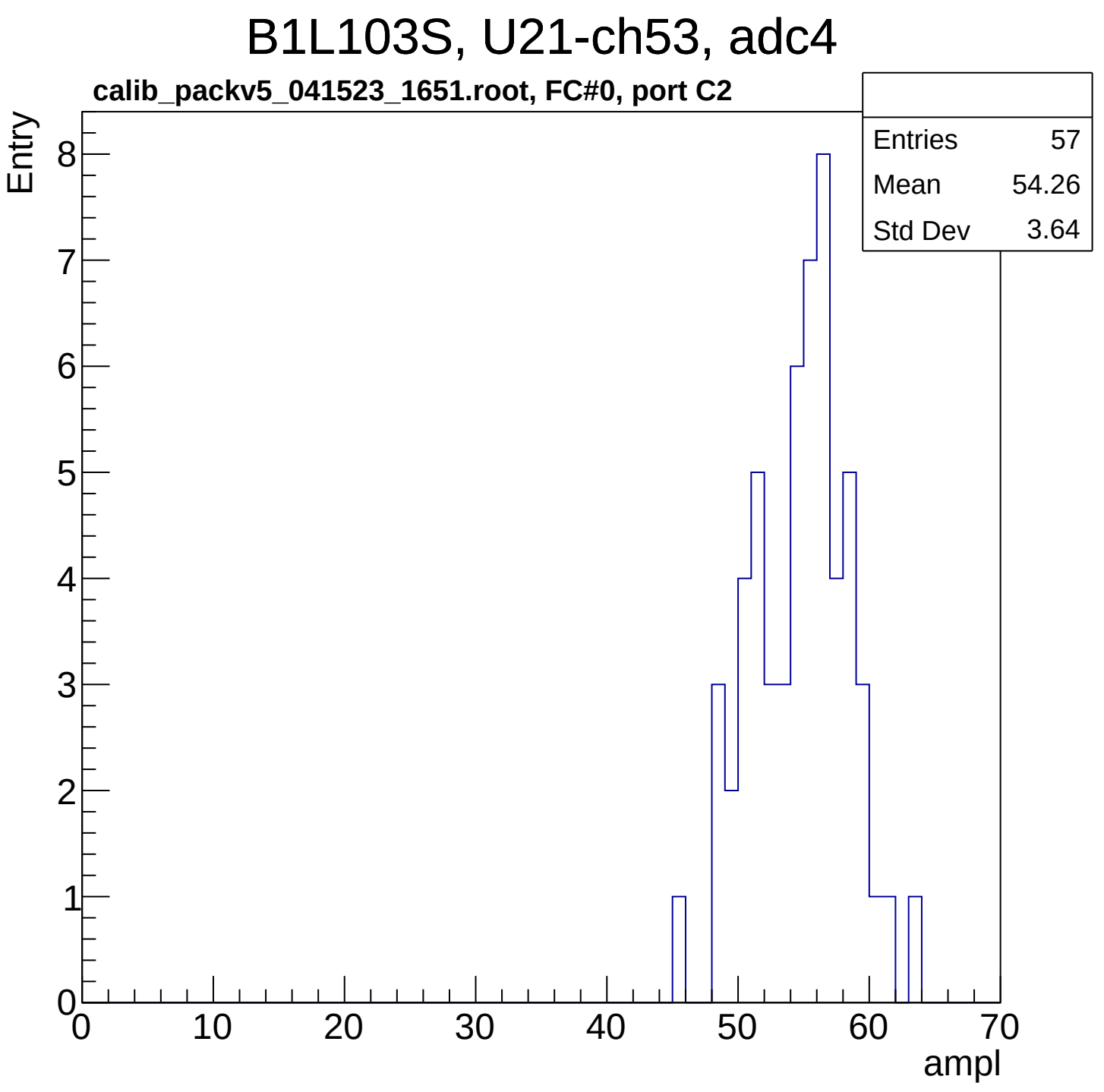
B1L103S, U21-ch53, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 54.26
Std Dev 3.64
Entry
ampl
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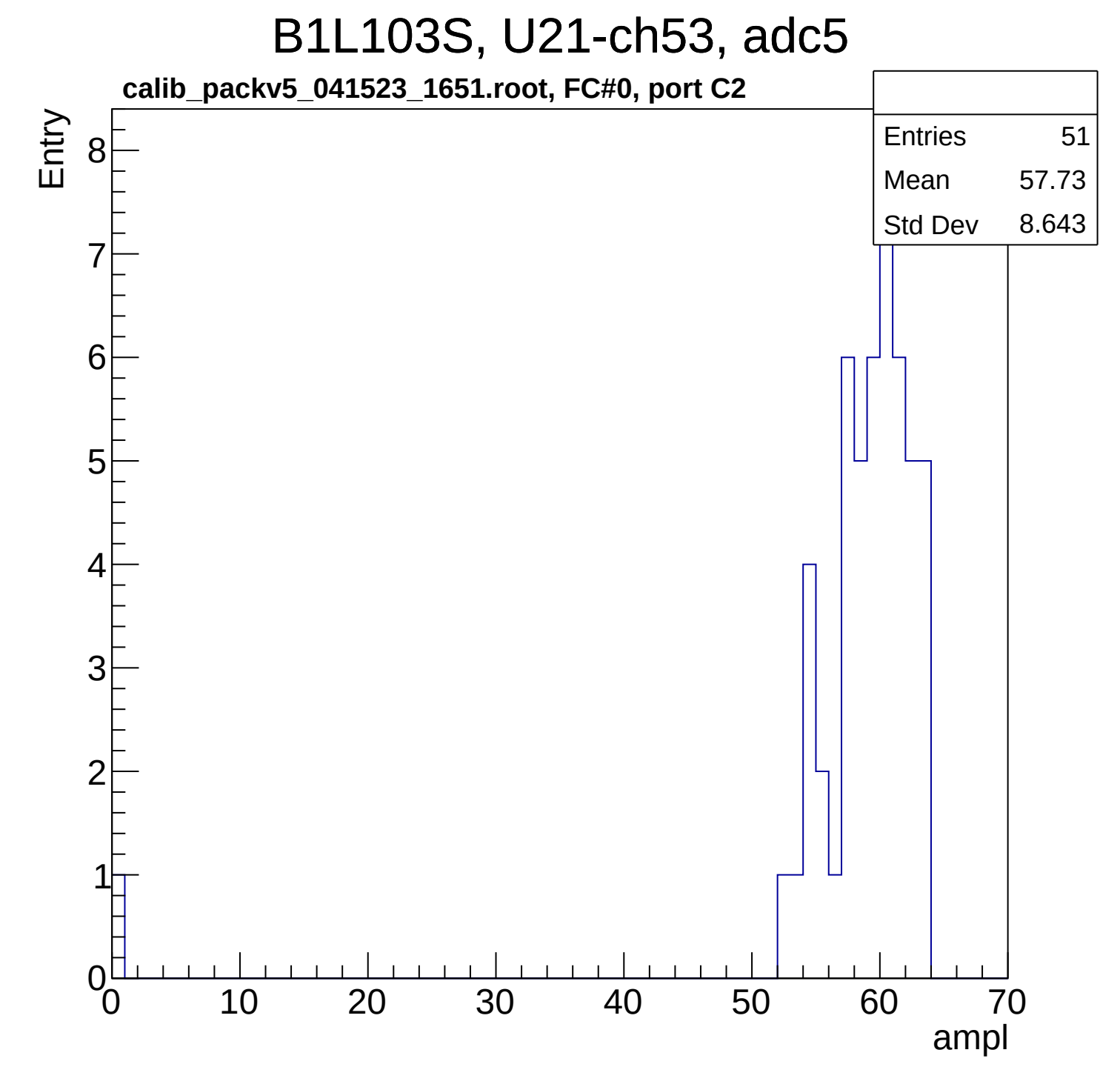
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch53, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 57.73
Std Dev 8.643
Entry
ampl
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2
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4
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6
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0
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60
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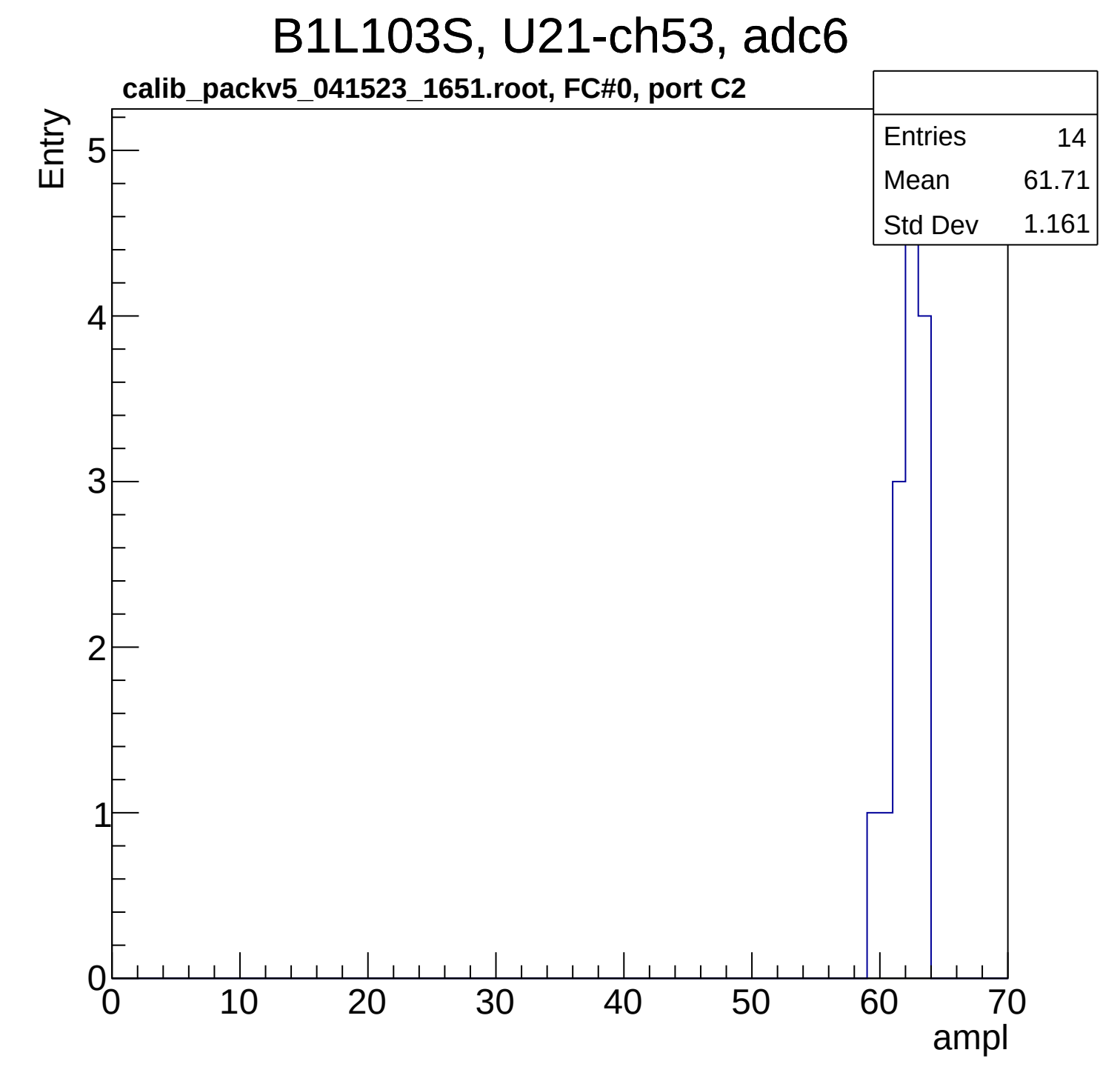
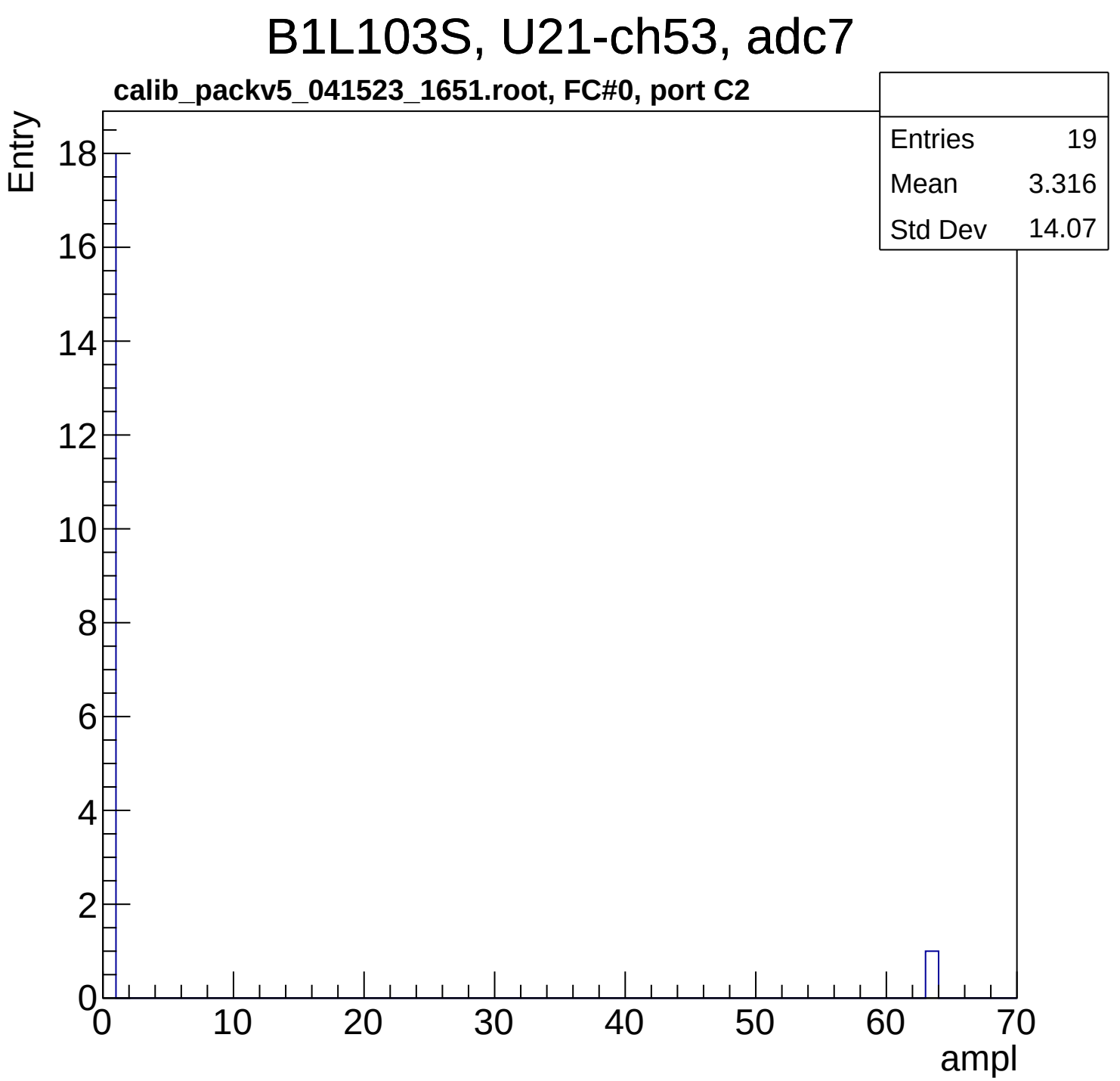

B1L103S, U21-ch53, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 61.71
Std Dev 1.161
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U21-ch53, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.316
Std Dev 14.07
Entry
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6
8
10
12
14
16
18
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10
20
30
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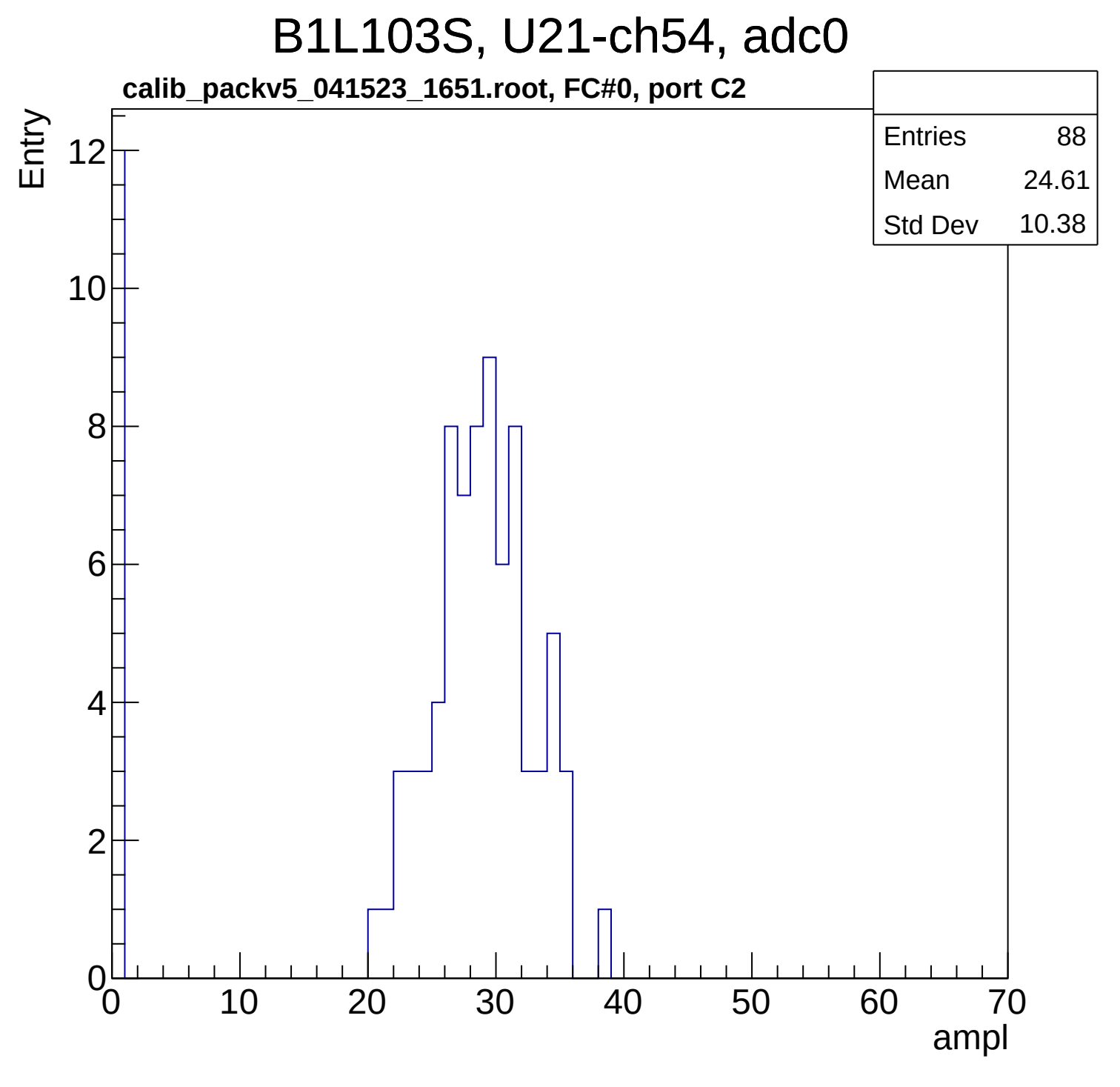
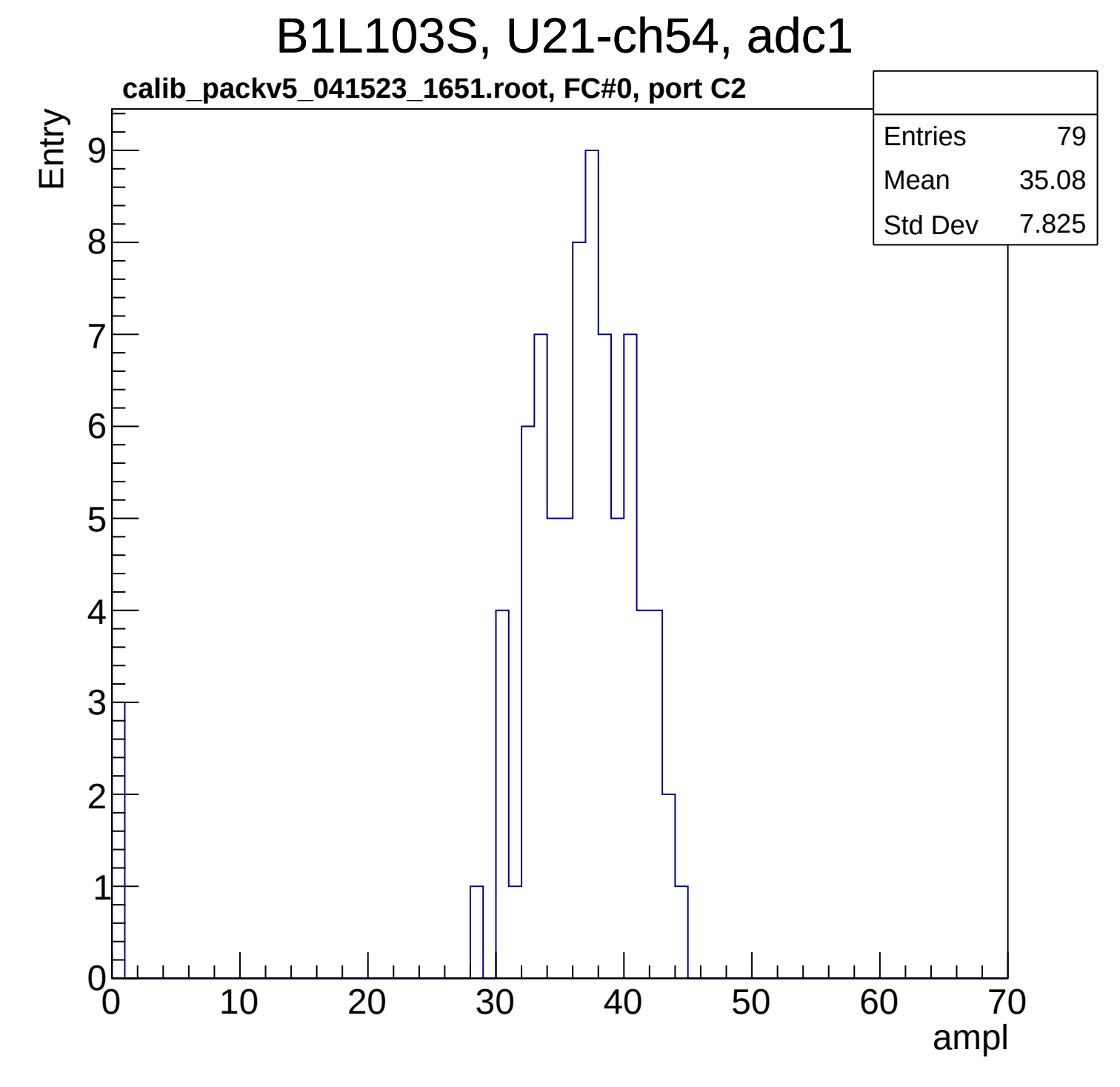
50
60
70
ampl


B1L103S, U21-ch54, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 24.61
Std Dev 10.38
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U21-ch54, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 35.08
Std Dev 7.825
Entry
ampl
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2
3
4
5
6
7
8
9
0
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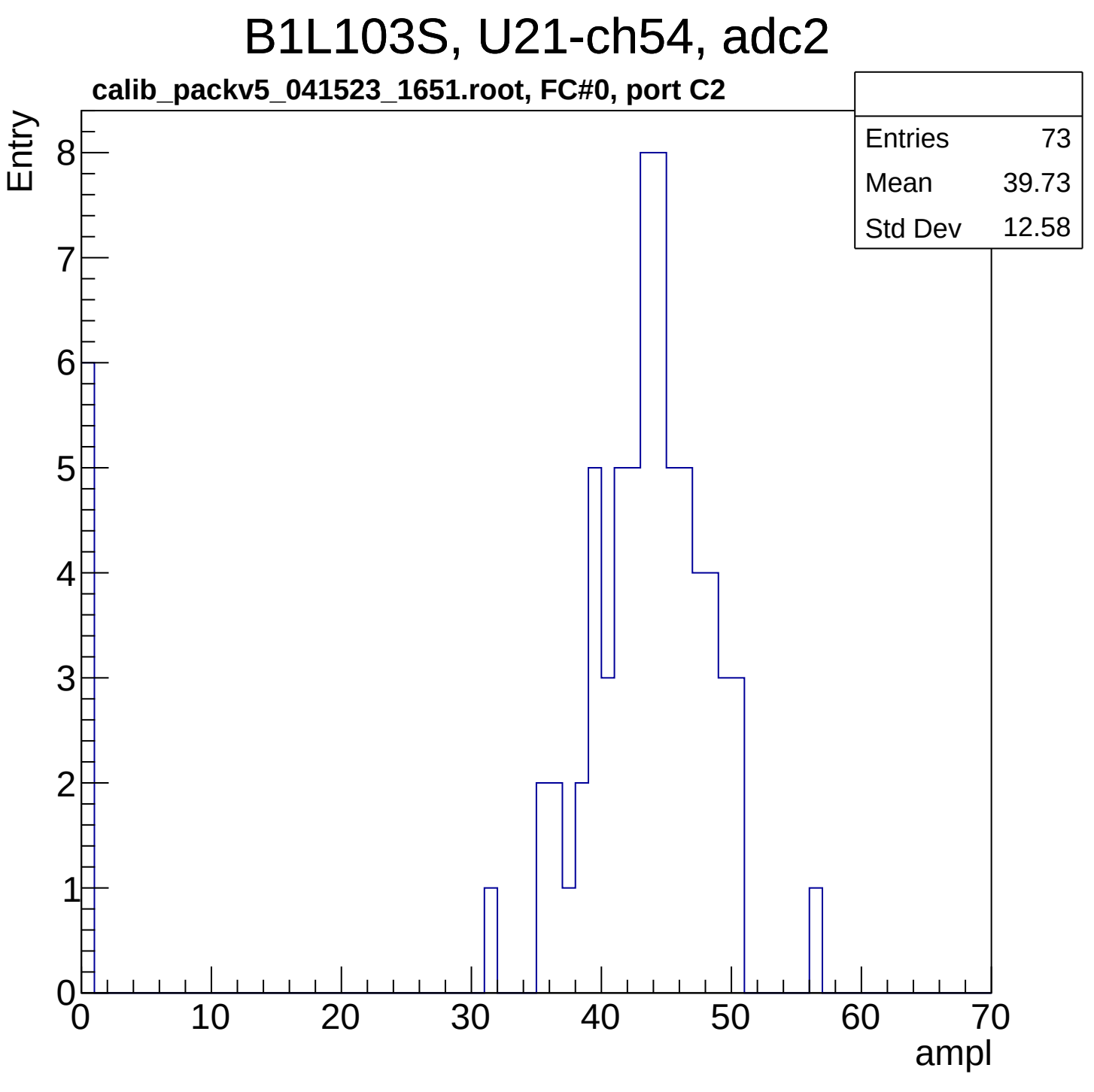
B1L103S, U21-ch54, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 39.73
Std Dev 12.58
Entry
ampl
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3
4
5
6
7
8
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10
20
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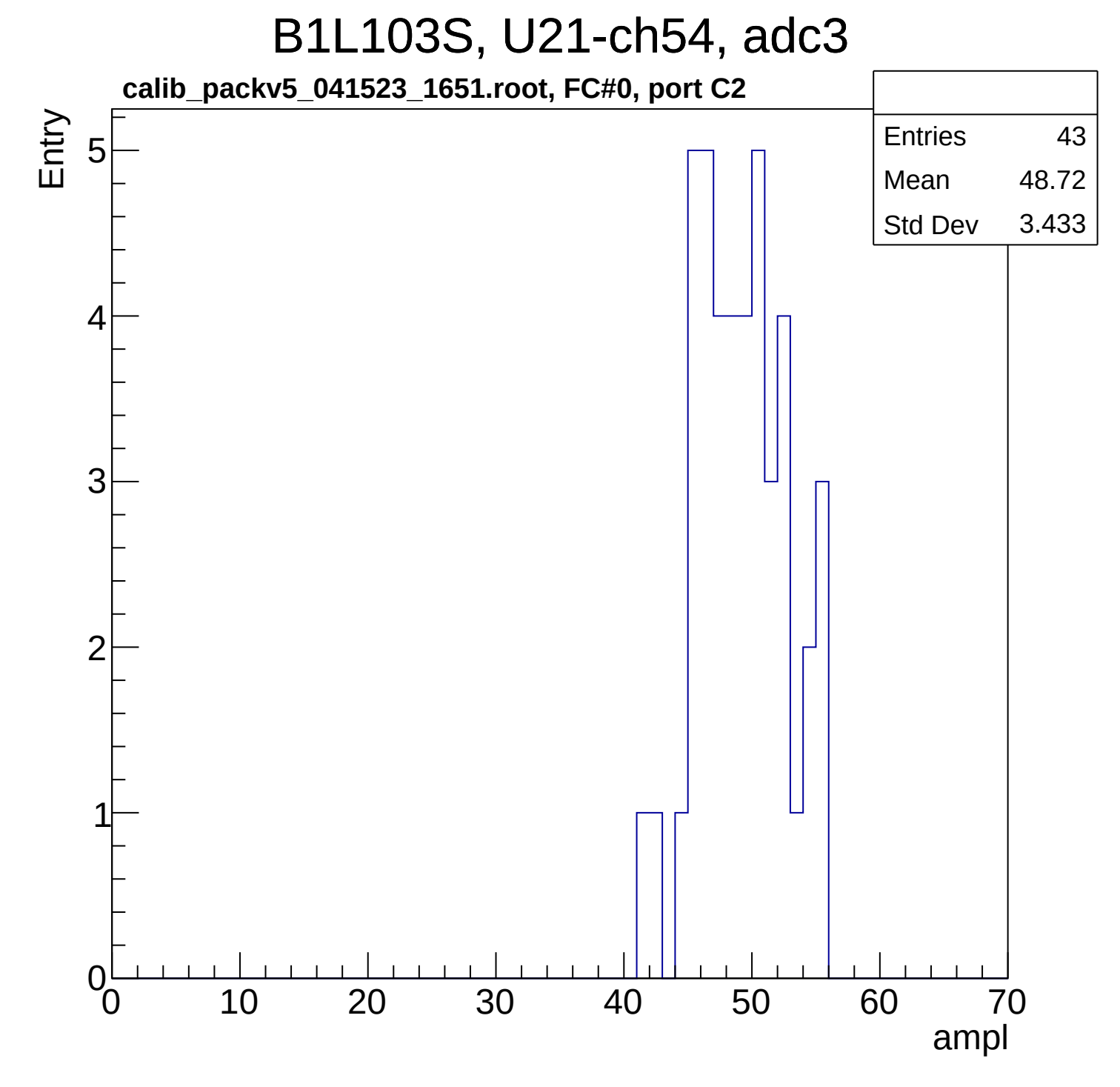
40
50
60
70


B1L103S, U21-ch54, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 48.72
Std Dev 3.433
Entry
ampl
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0
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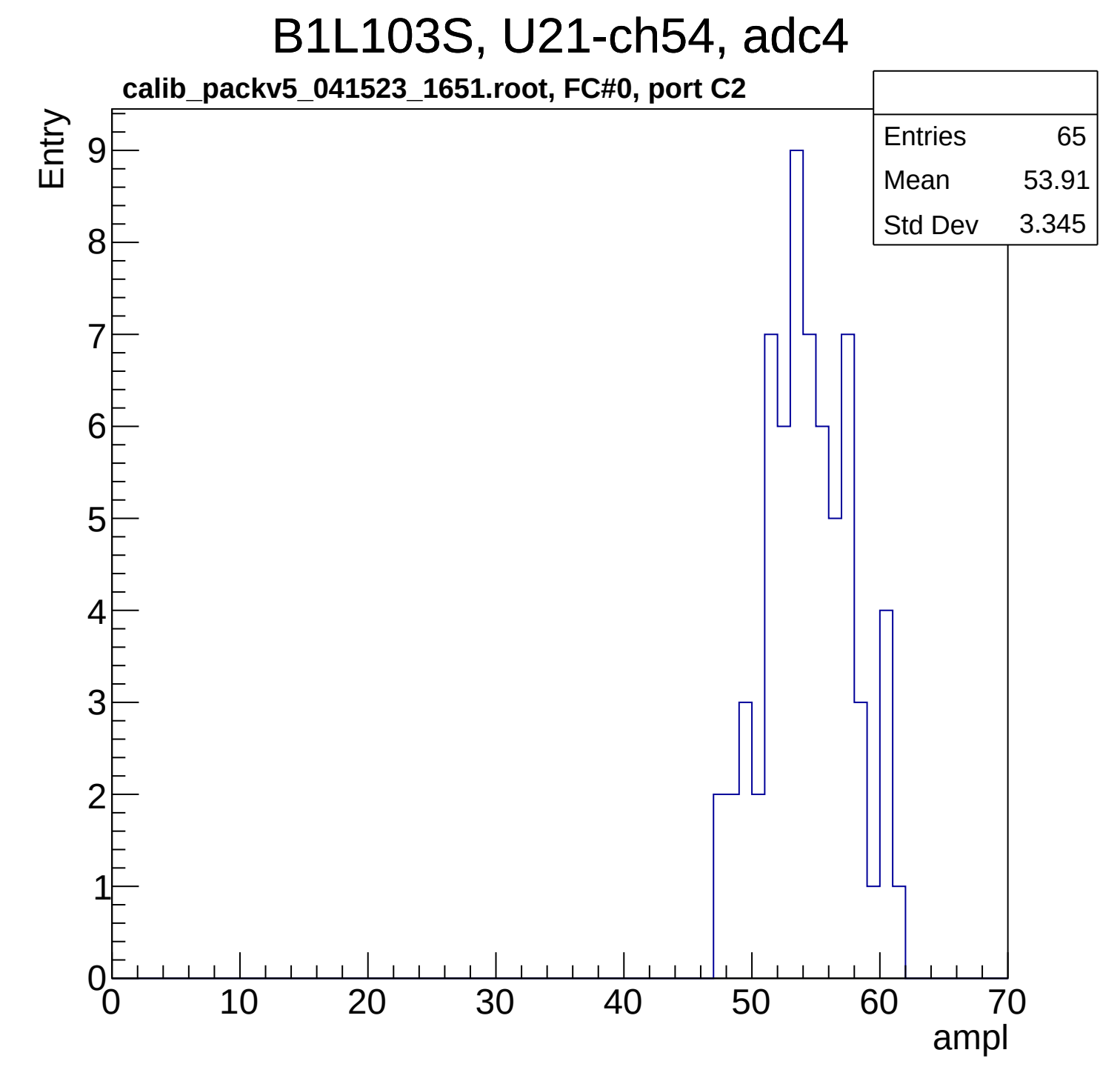
60
70


B1L103S, U21-ch54, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 53.91
Std Dev 3.345
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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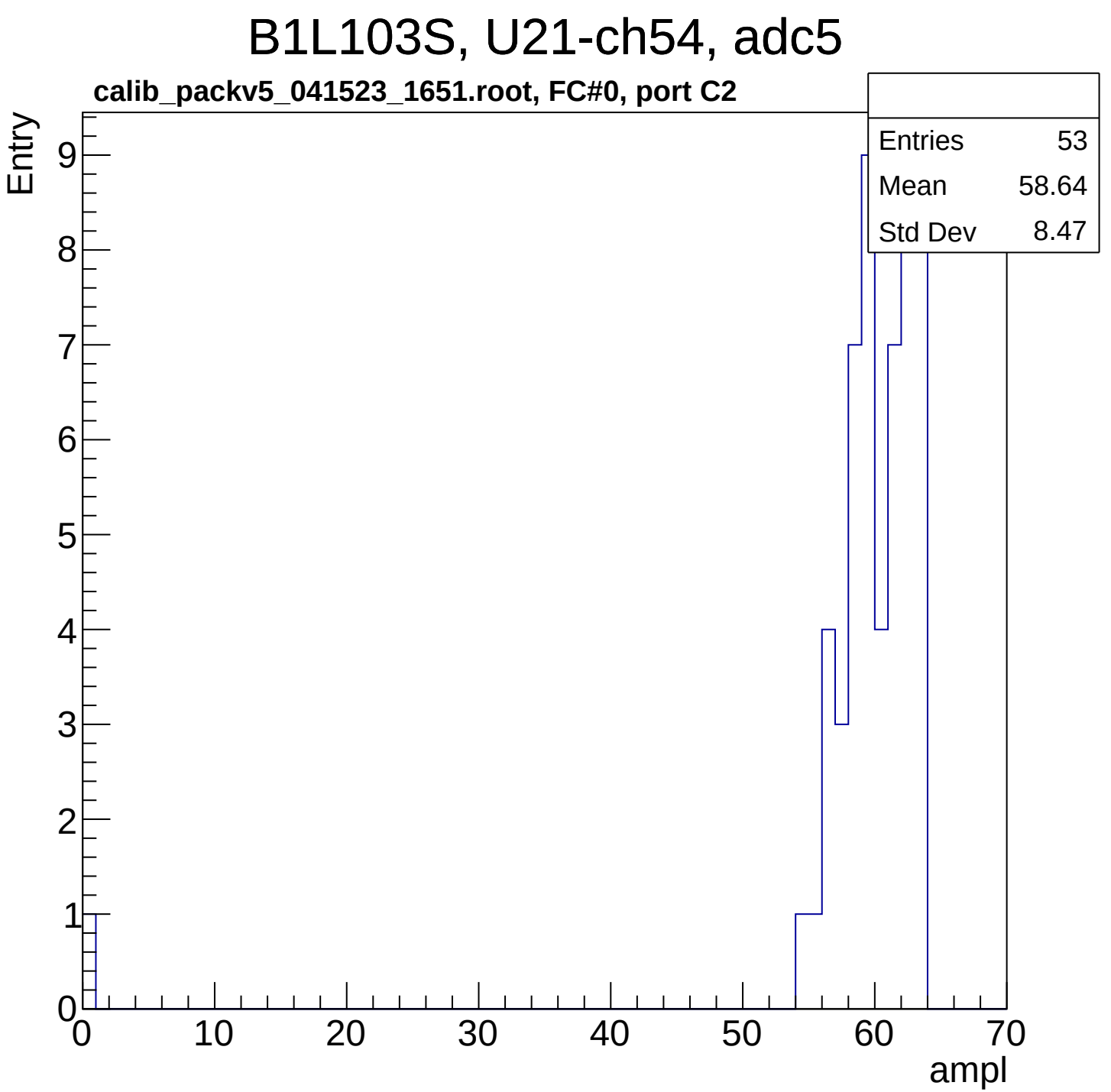
B1L103S, U21-ch54, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 58.64
Std Dev 8.47
Entry
ampl
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2
3
4
5
6
7
8
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0
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60
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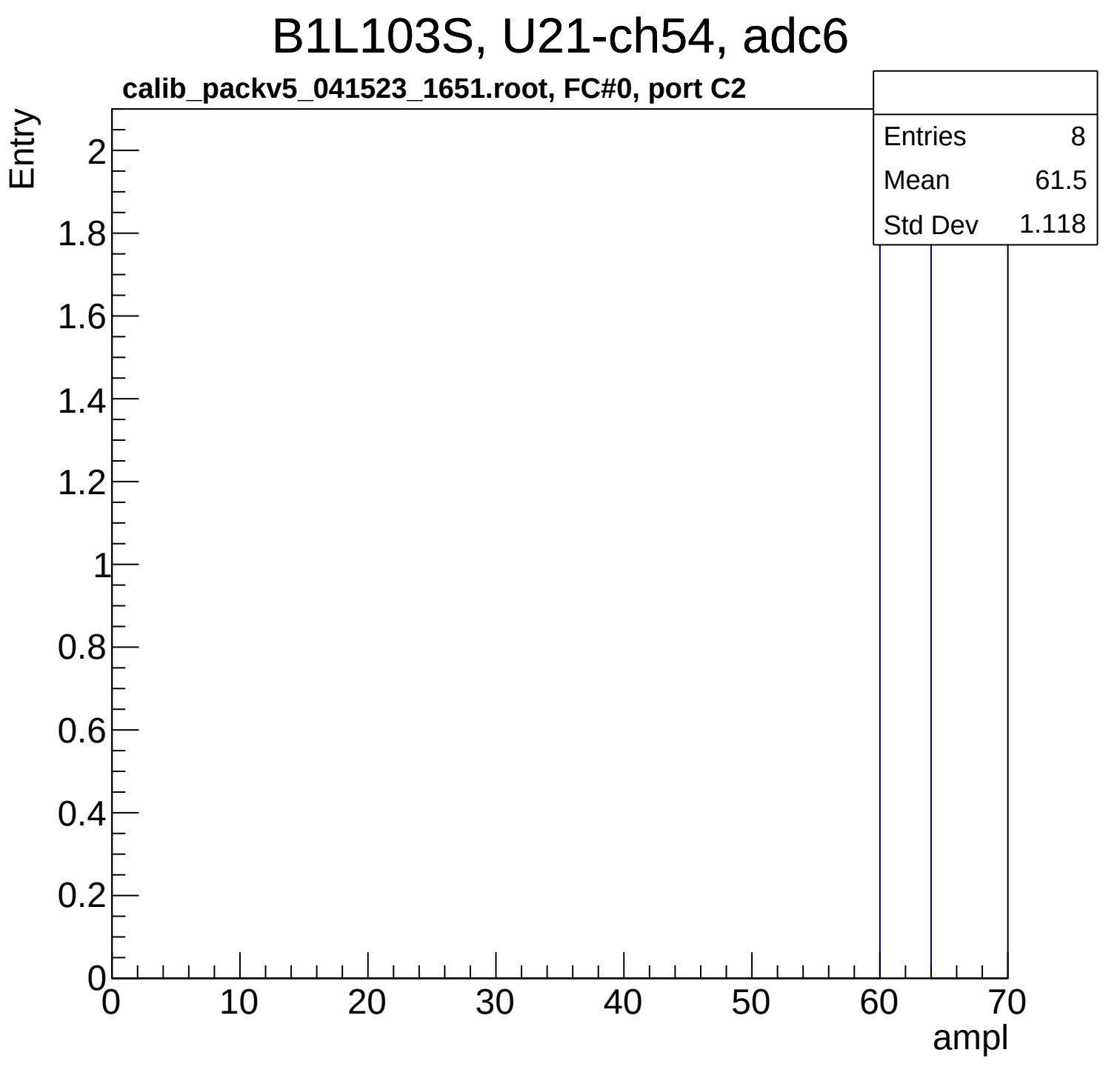
B1L103S, U21-ch54, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 61.5
Std Dev 1.118
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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40
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60
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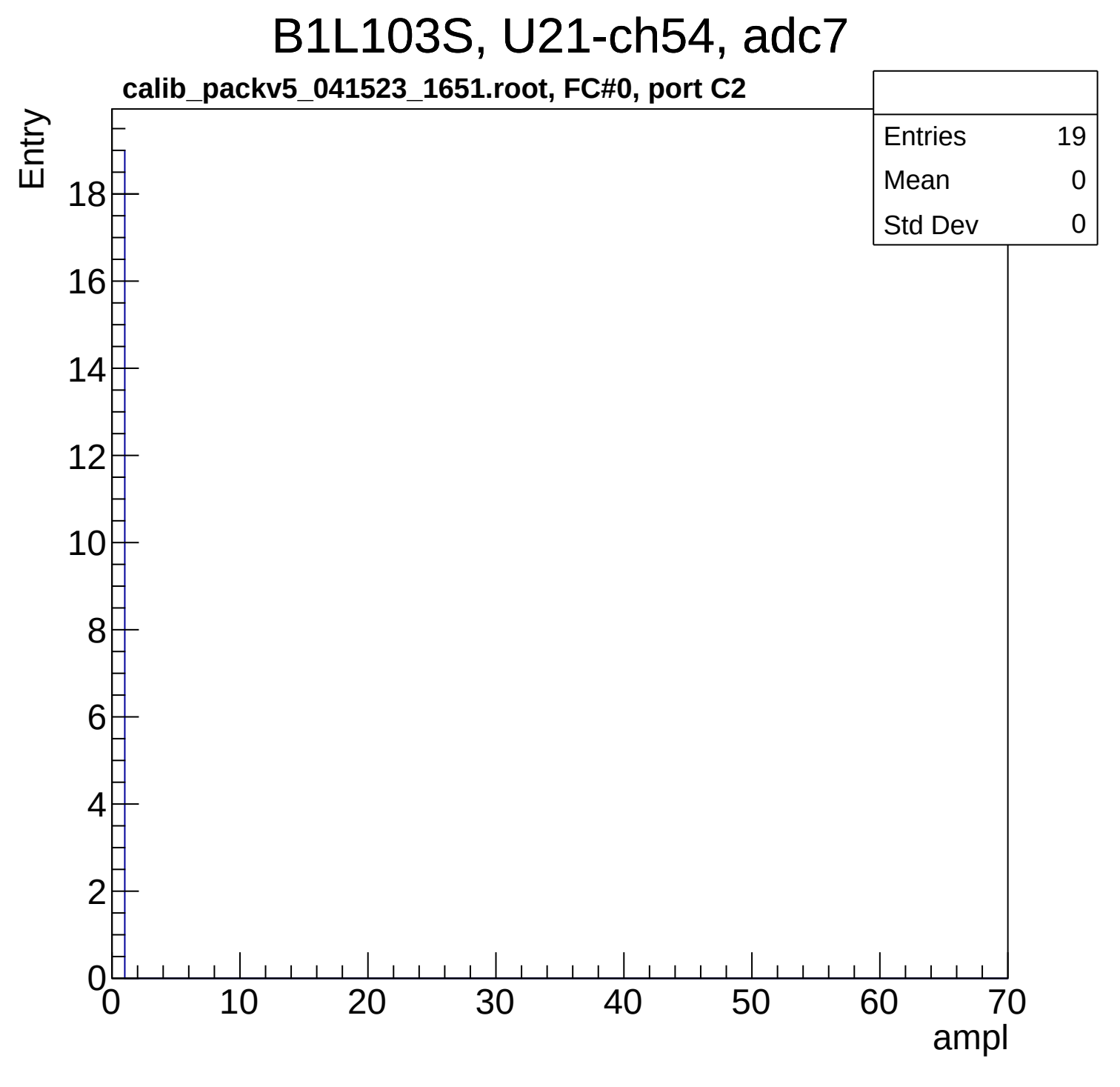
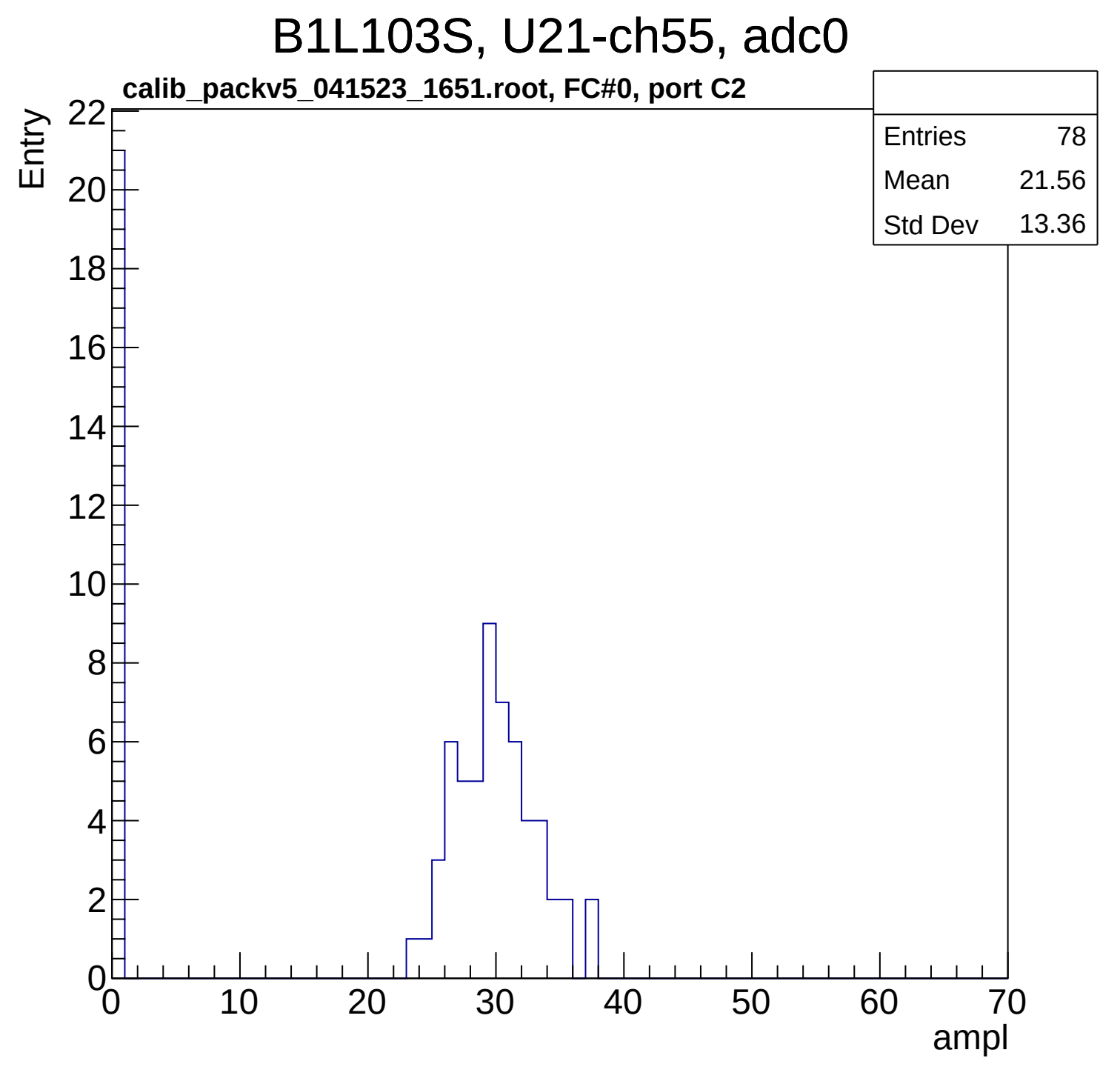

B1L103S, U21-ch54, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch55, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 21.56
Std Dev 13.36
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
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40
50
60
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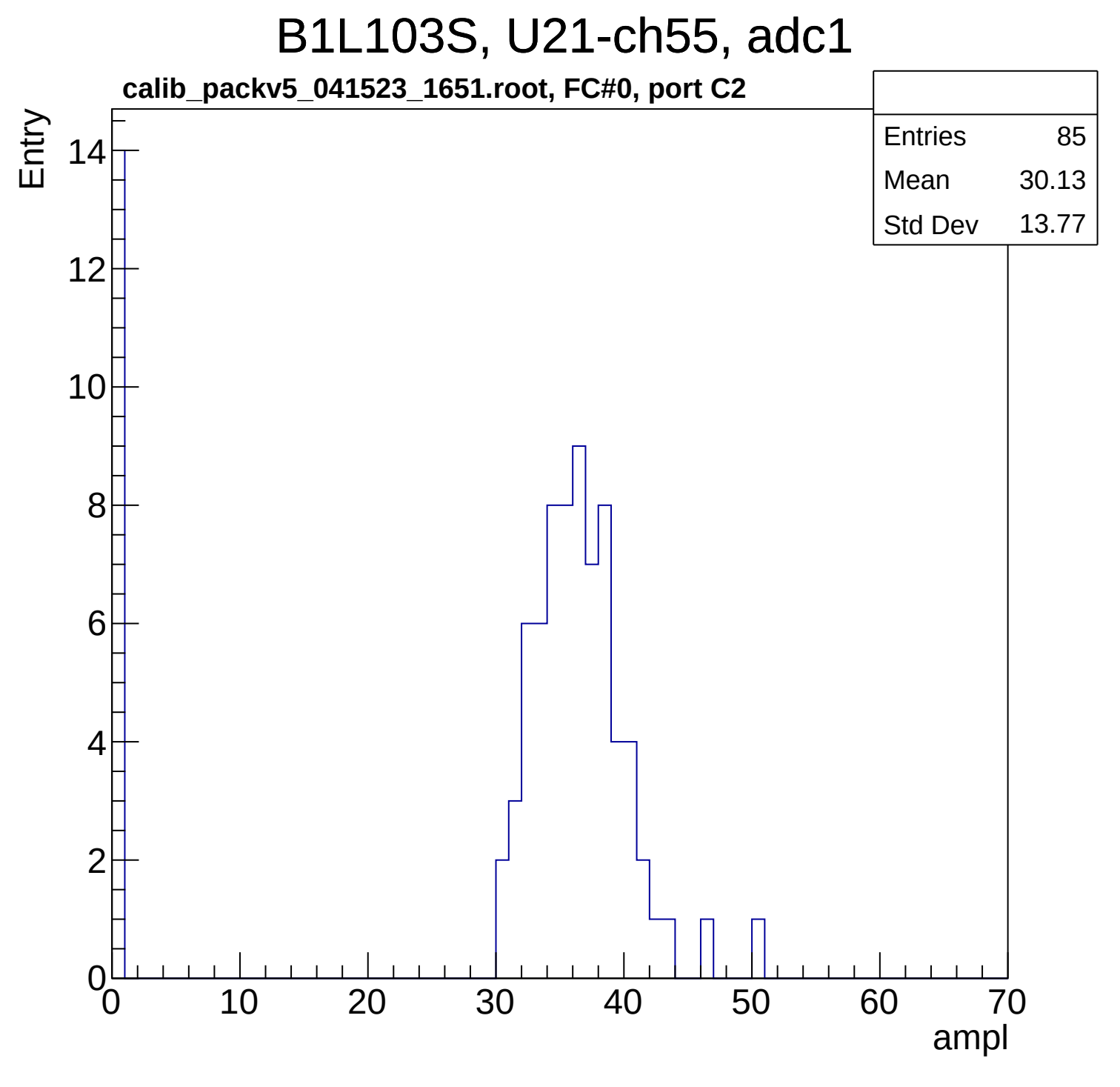
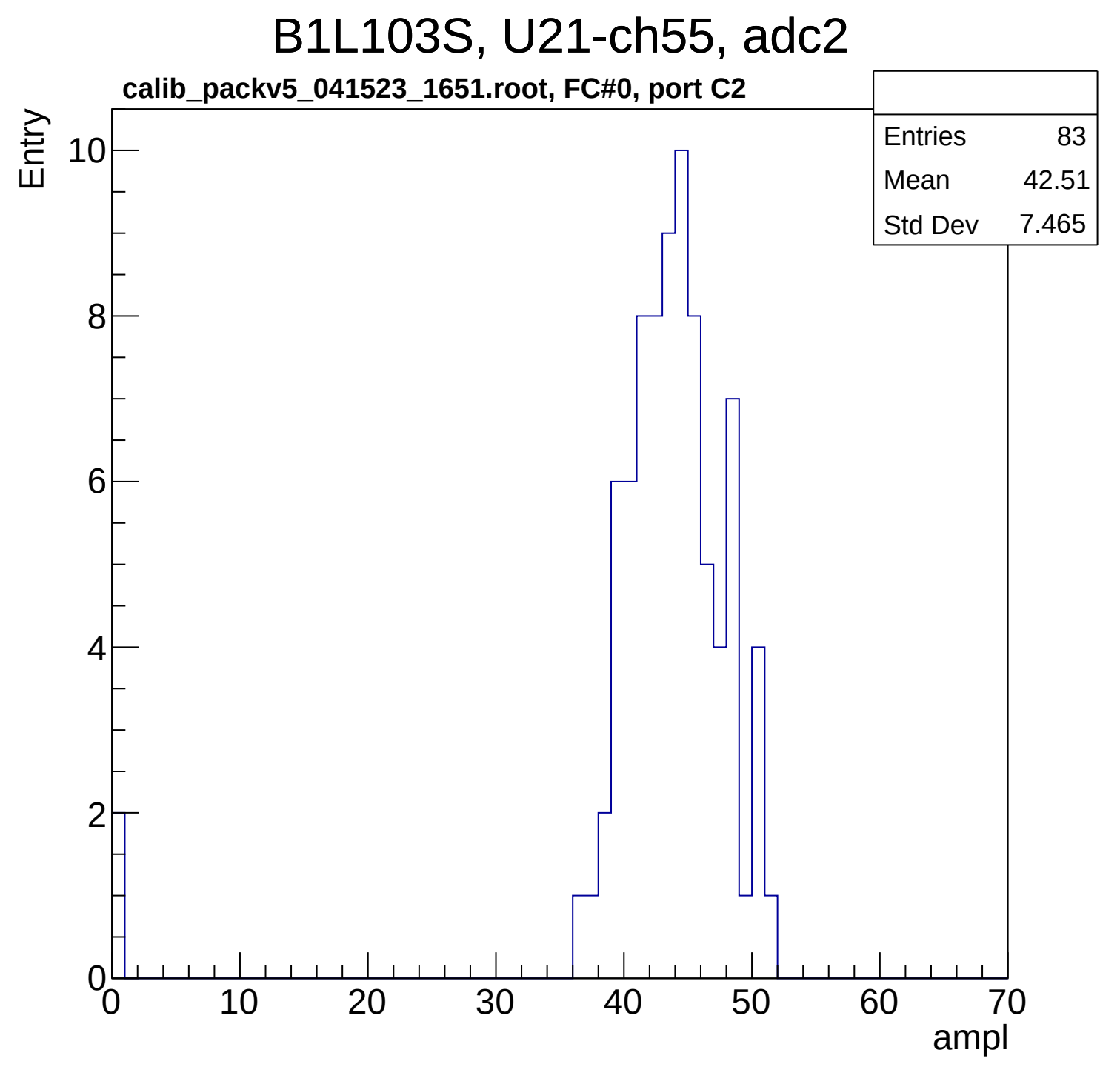
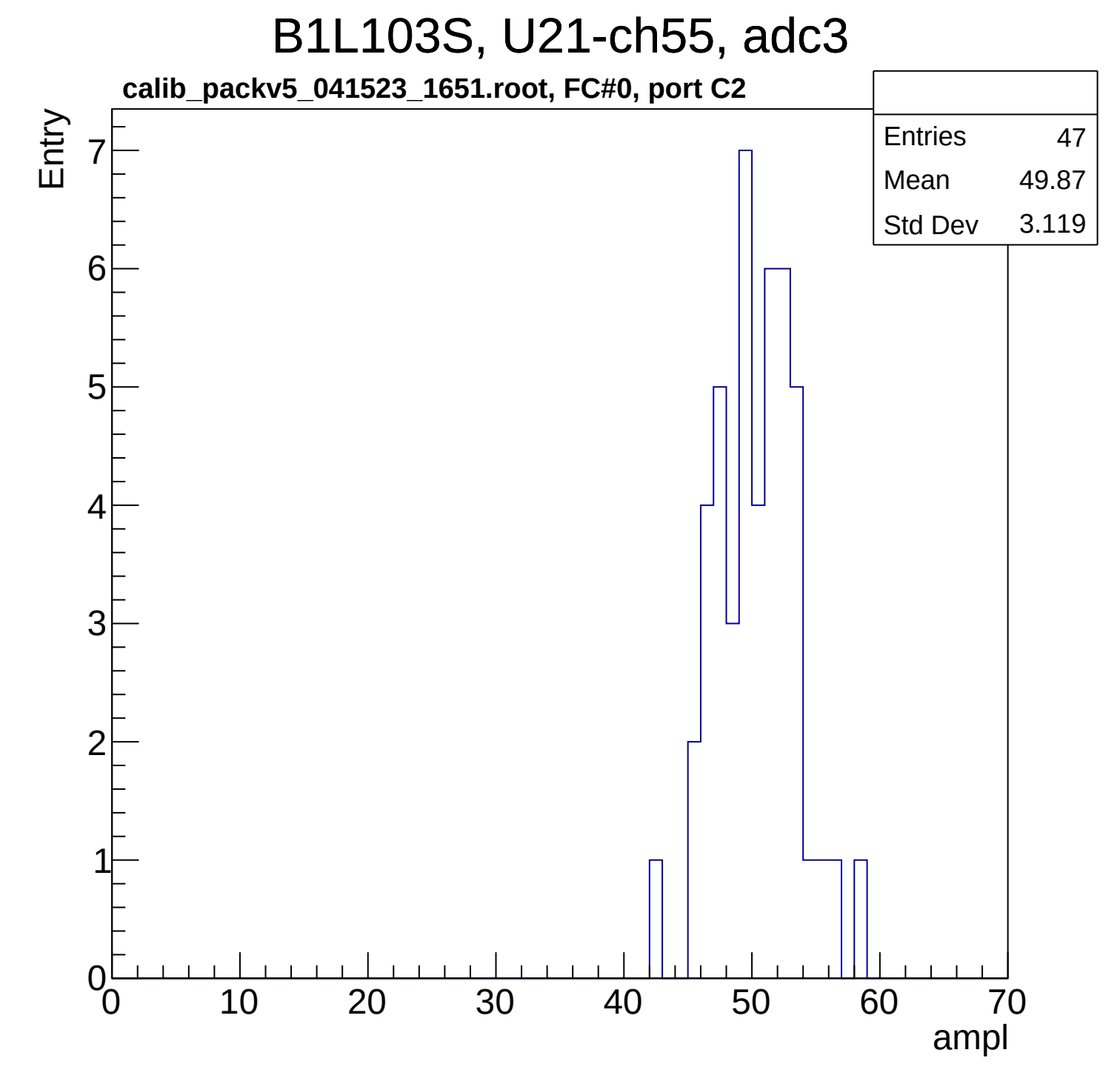

B1L103S, U21-ch55, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 30.13
Std Dev 13.77
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch55, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 42.51
Std Dev 7.465
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U21-ch55, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 49.87
Std Dev 3.119
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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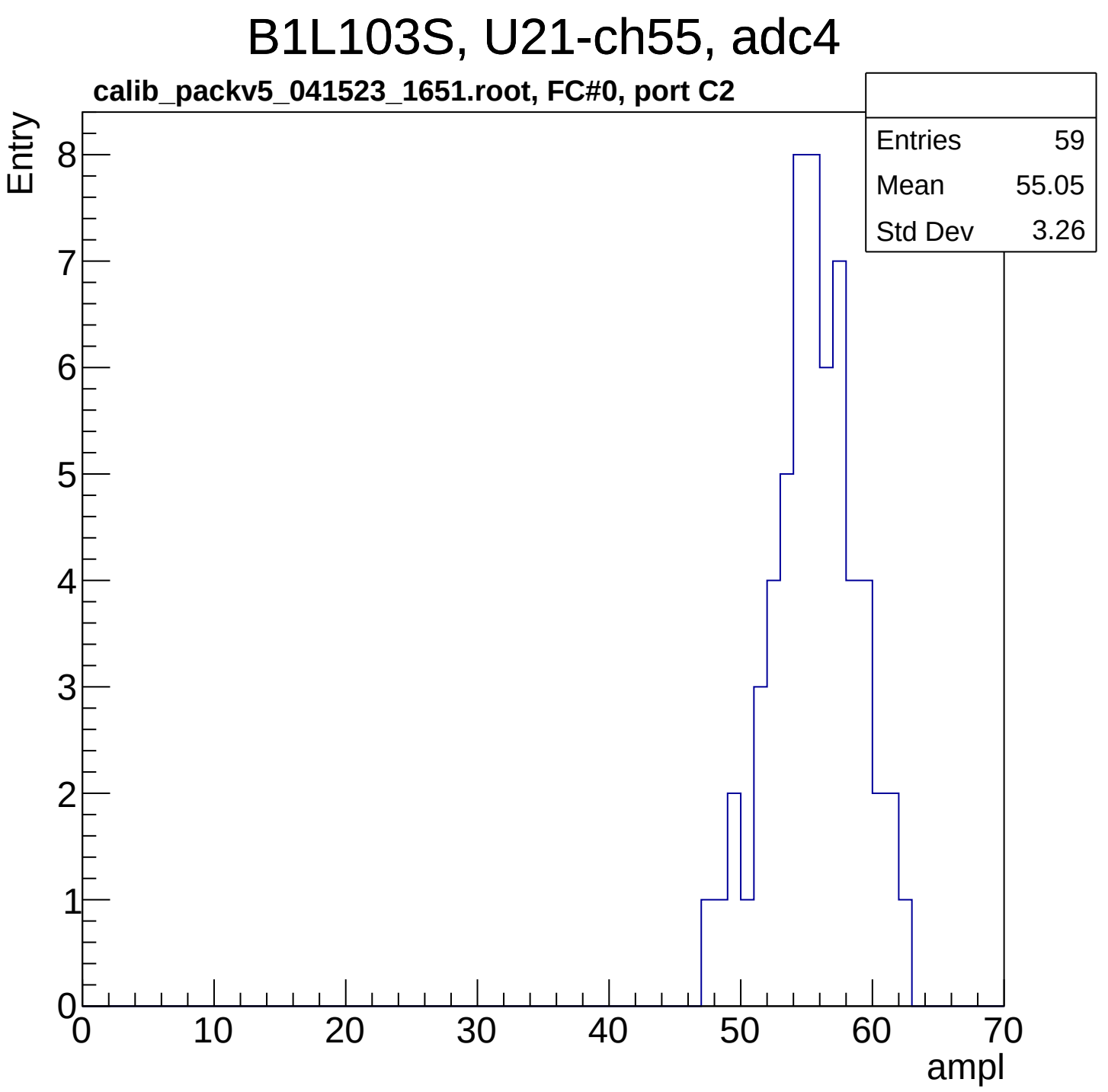
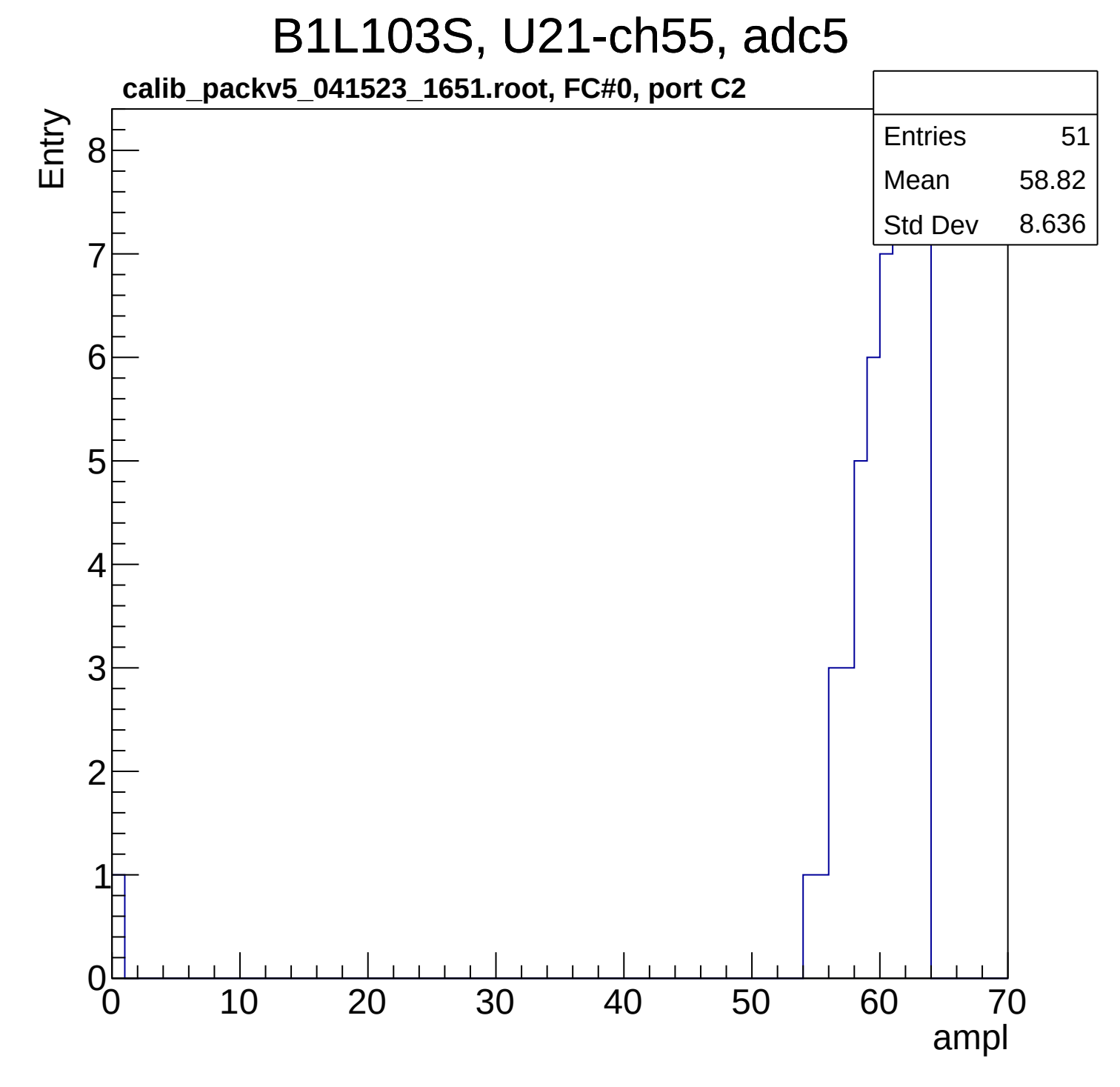

B1L103S, U21-ch55, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 55.05
Std Dev 3.26
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch55, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 58.82
Std Dev 8.636
Entry
ampl
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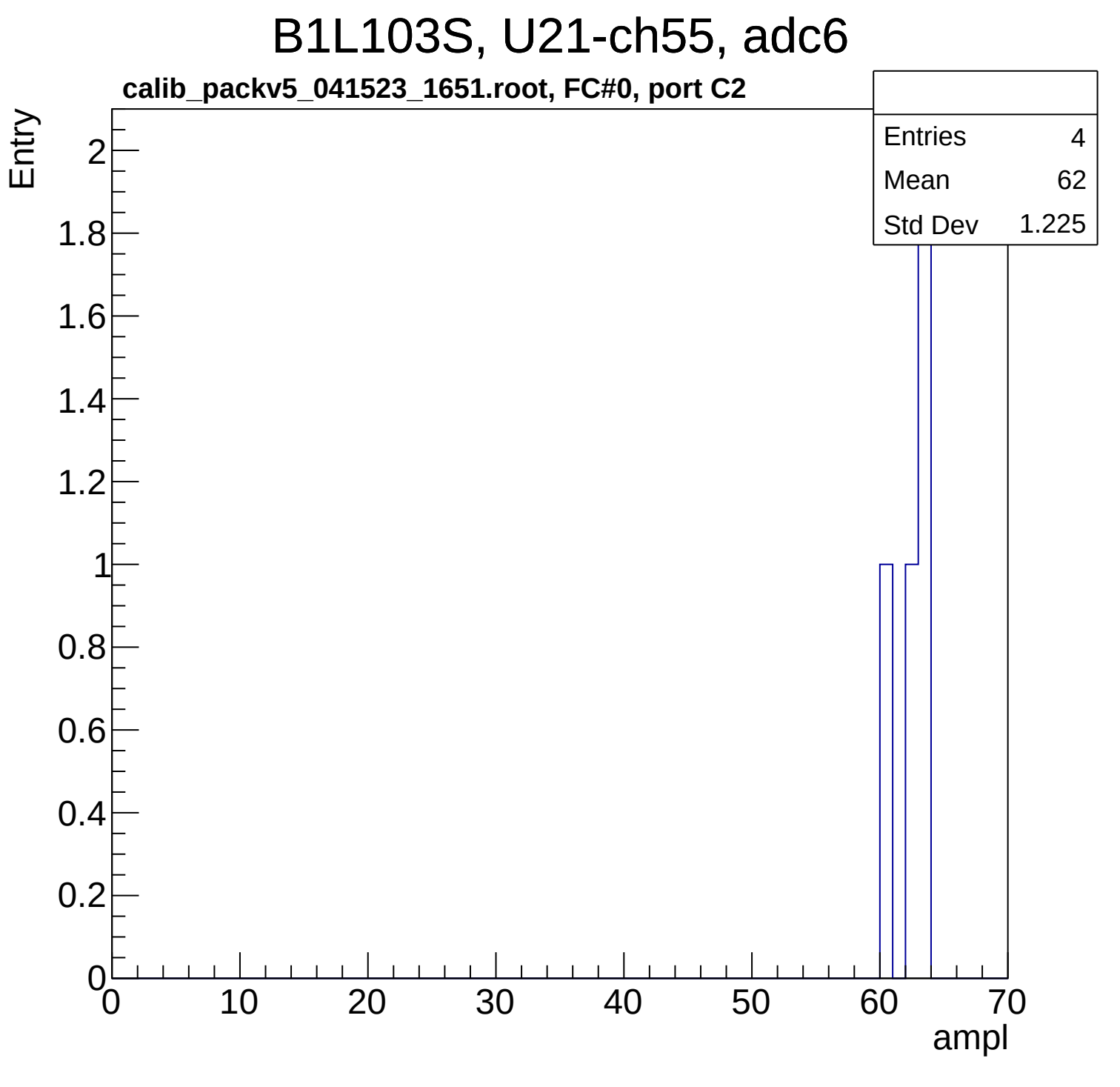
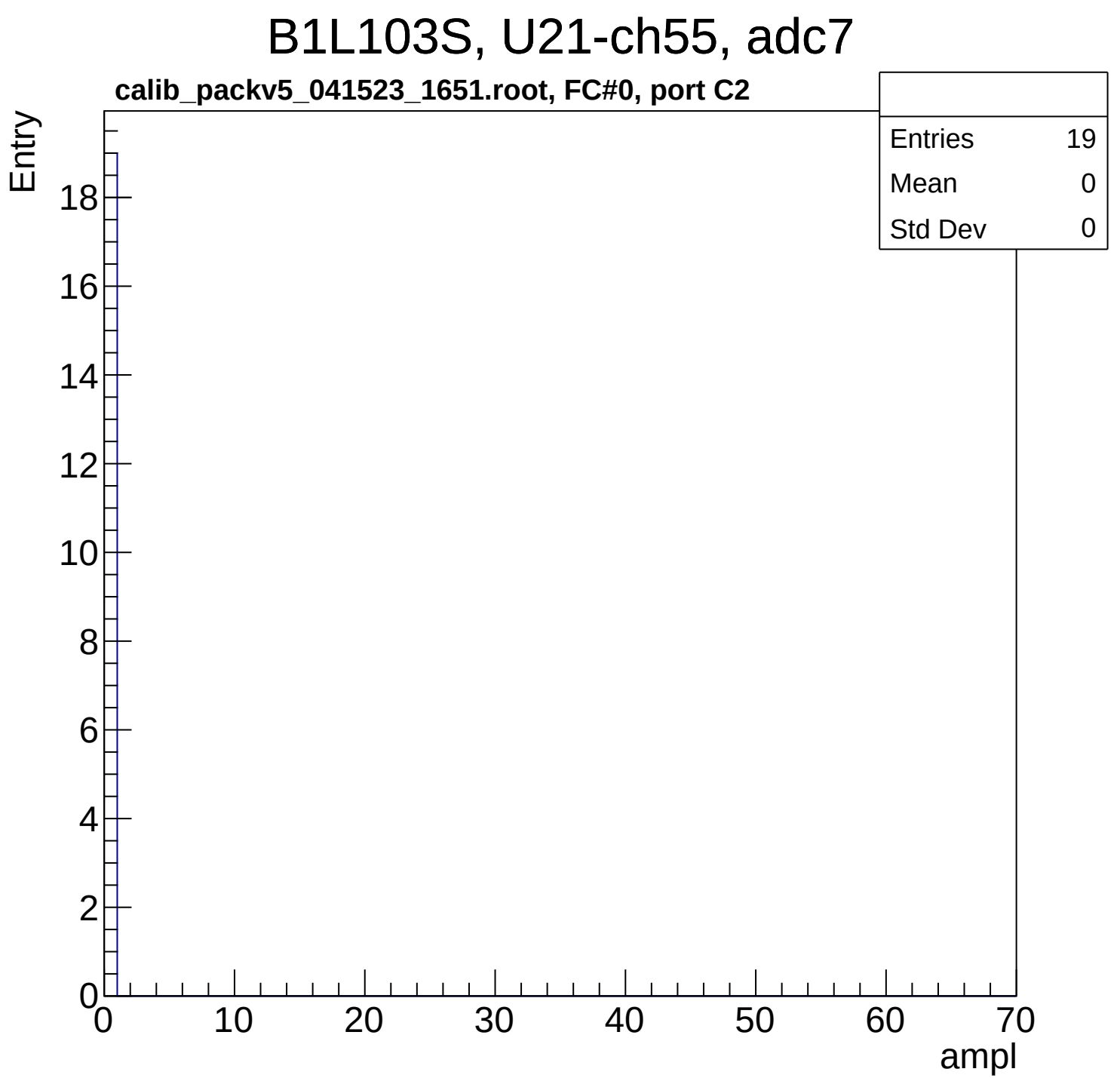
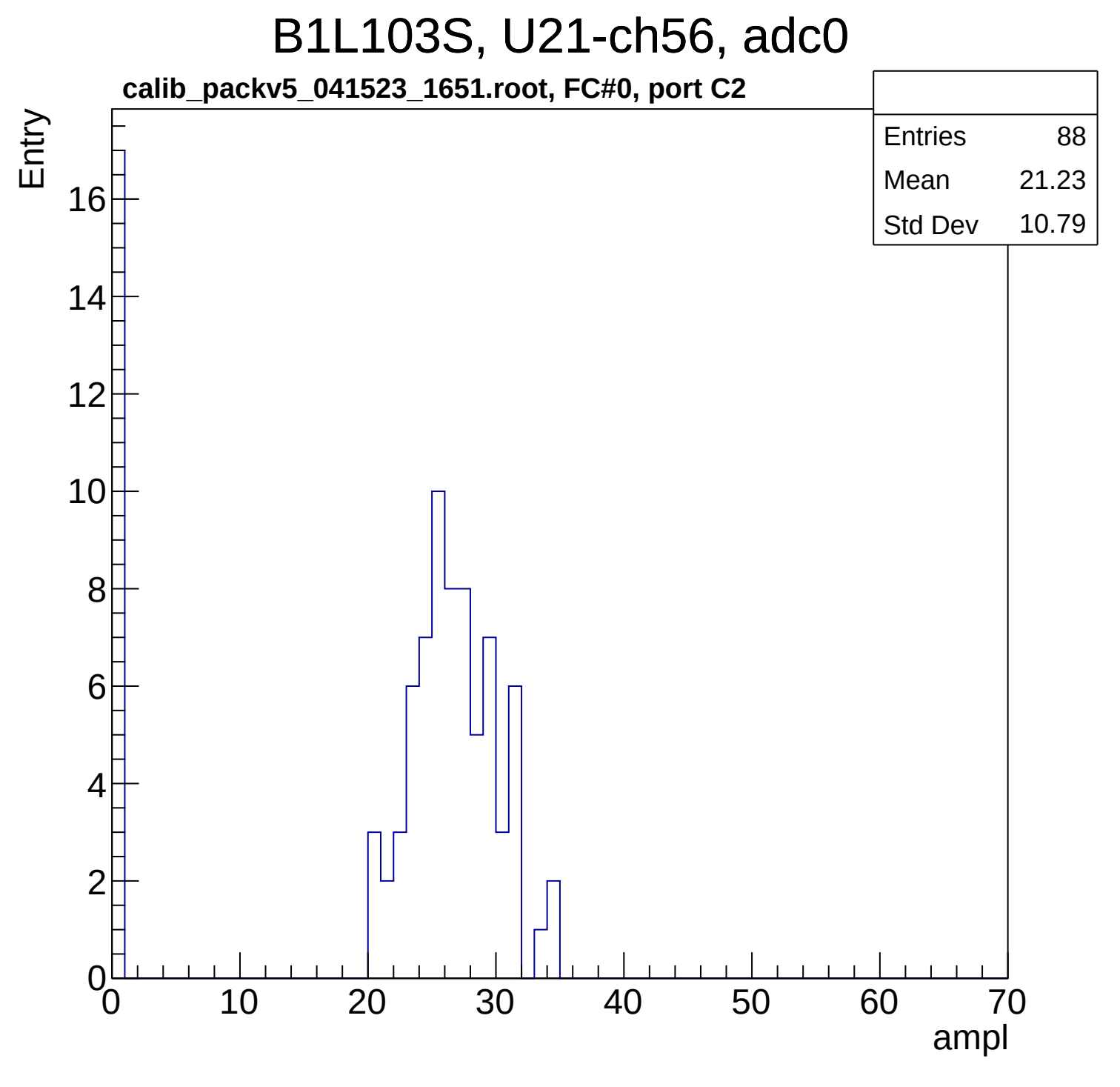
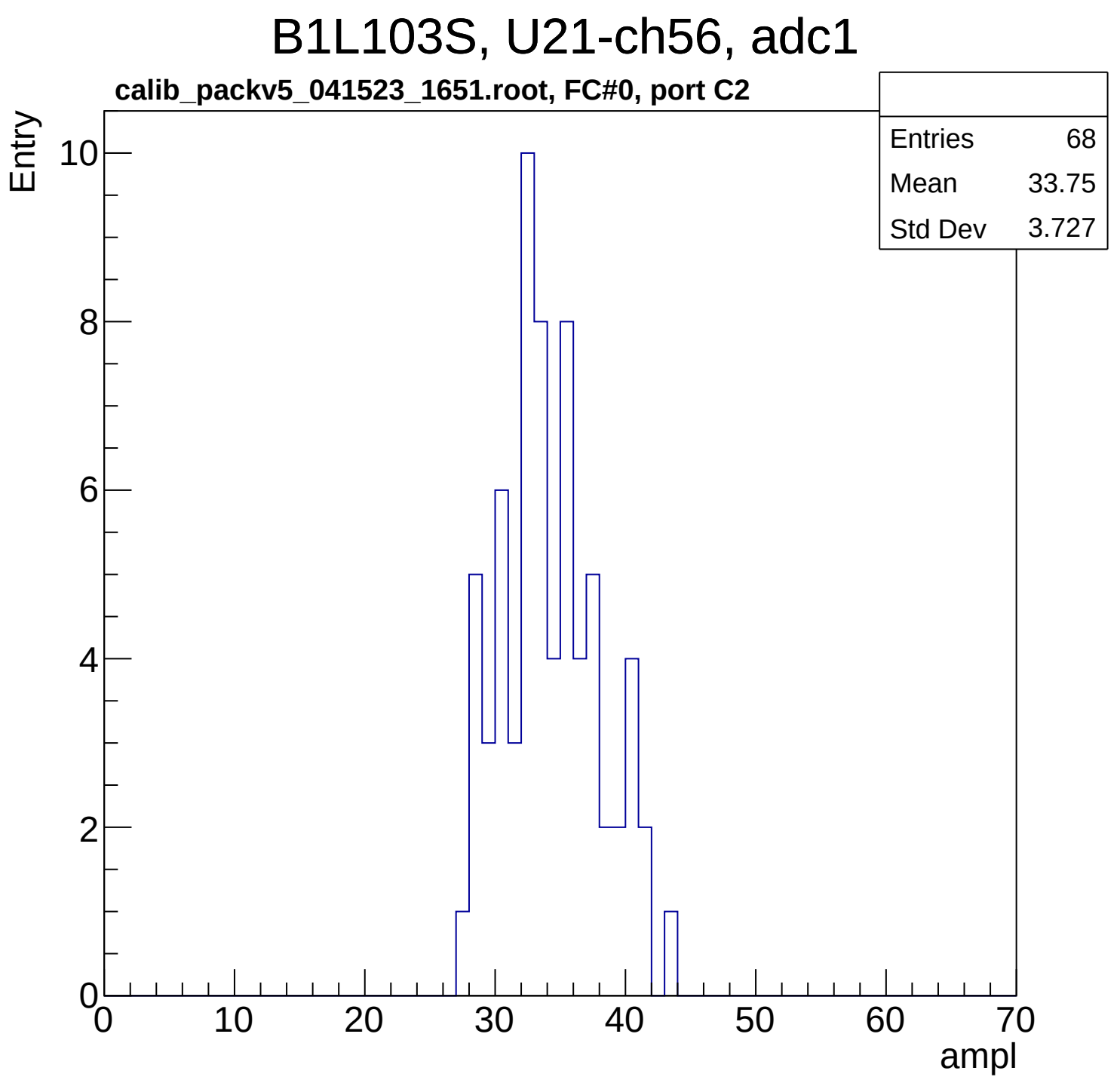
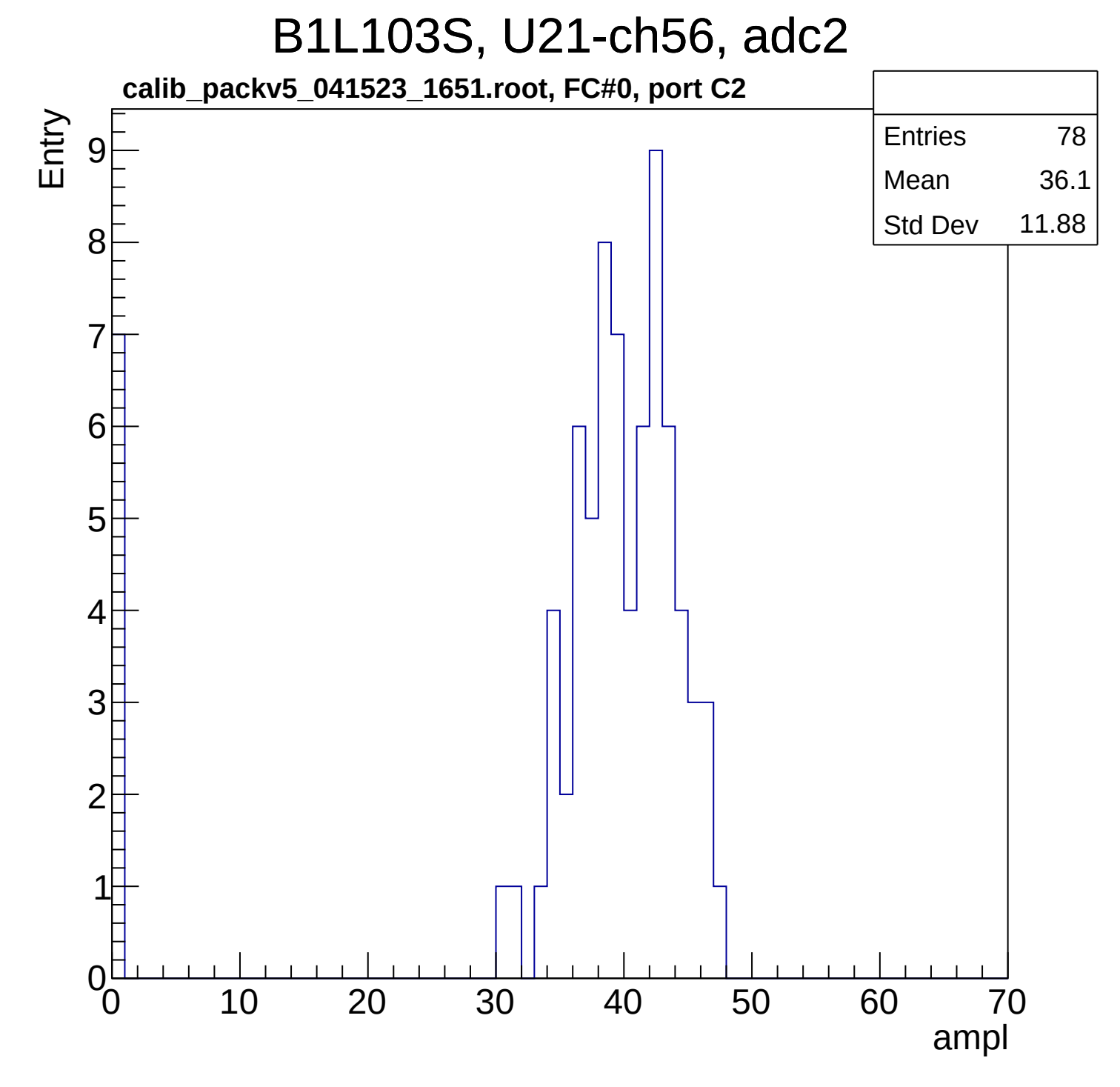
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

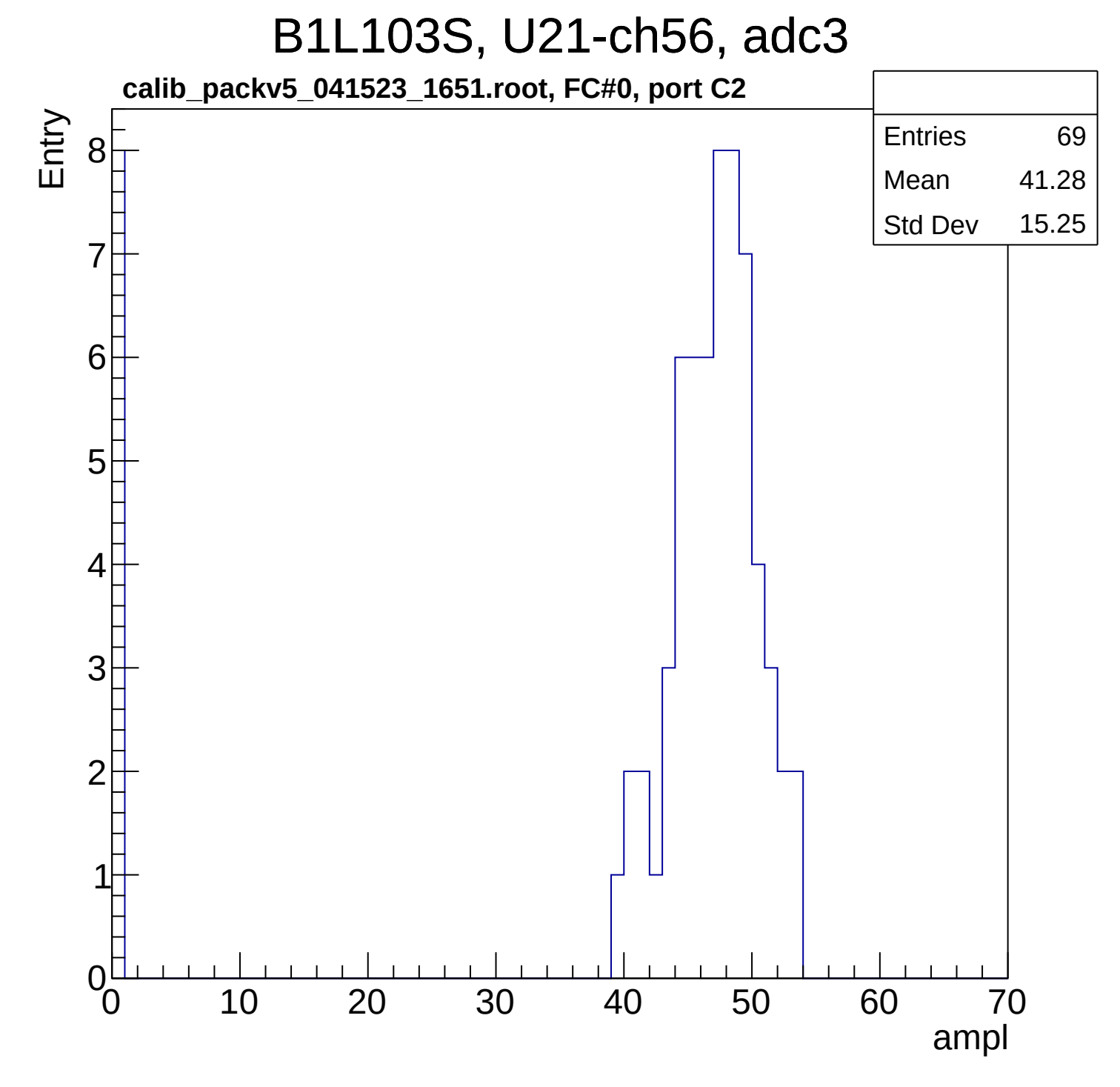

B1L103S, U21-ch55, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 62
Std Dev 1.225
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

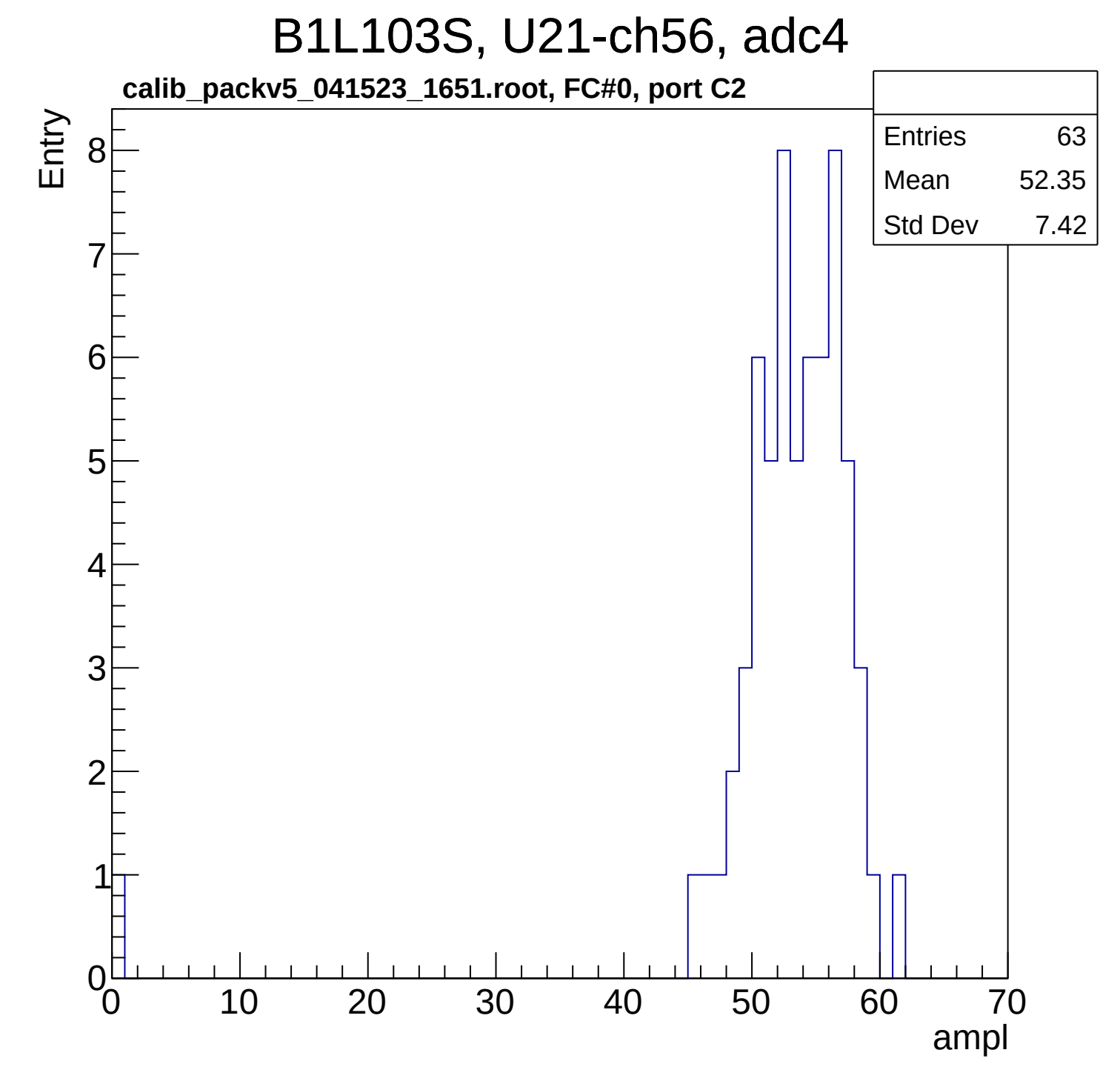

B1L103S, U21-ch55, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

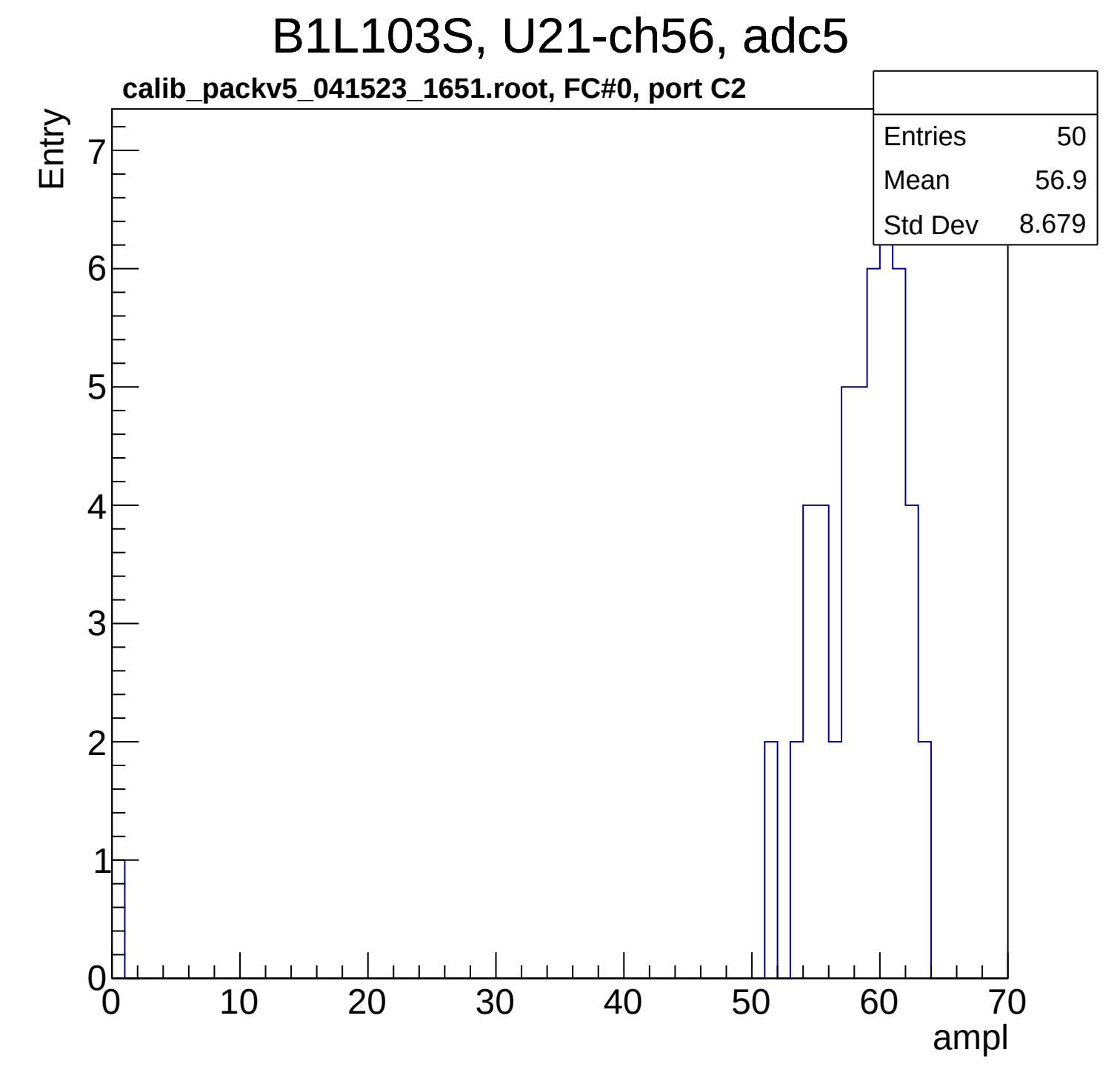

B1L103S, U21-ch56, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 21.23
Std Dev 10.79
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

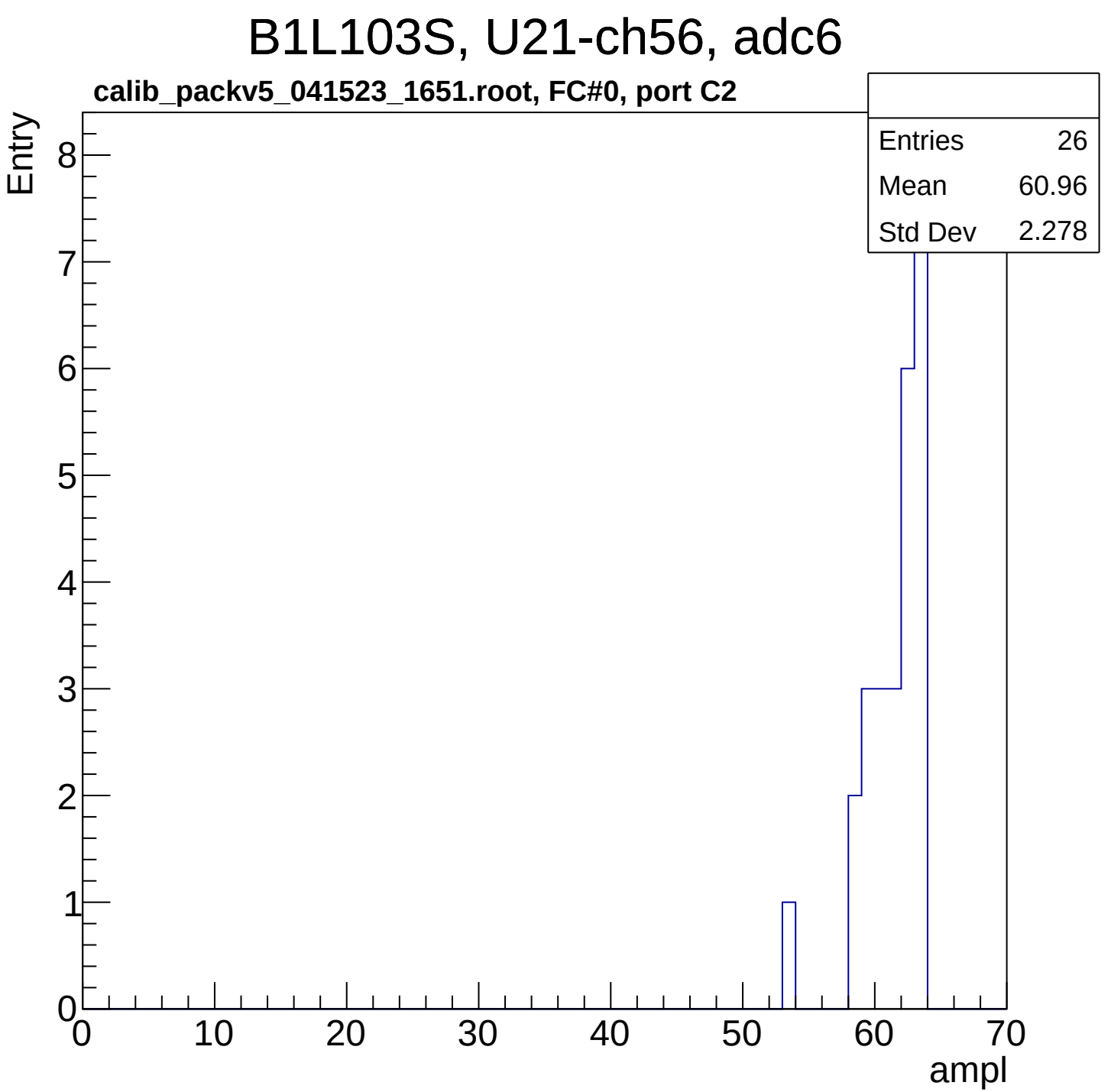

B1L103S, U21-ch56, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 33.75
Std Dev 3.727
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U21-ch56, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 36.1
Std Dev 11.88
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch56, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 41.28
Std Dev 15.25
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch56, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 52.35
Std Dev 7.42
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch56, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 56.9
Std Dev 8.679
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U21-ch56, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 60.96
Std Dev 2.278
Entry
ampl
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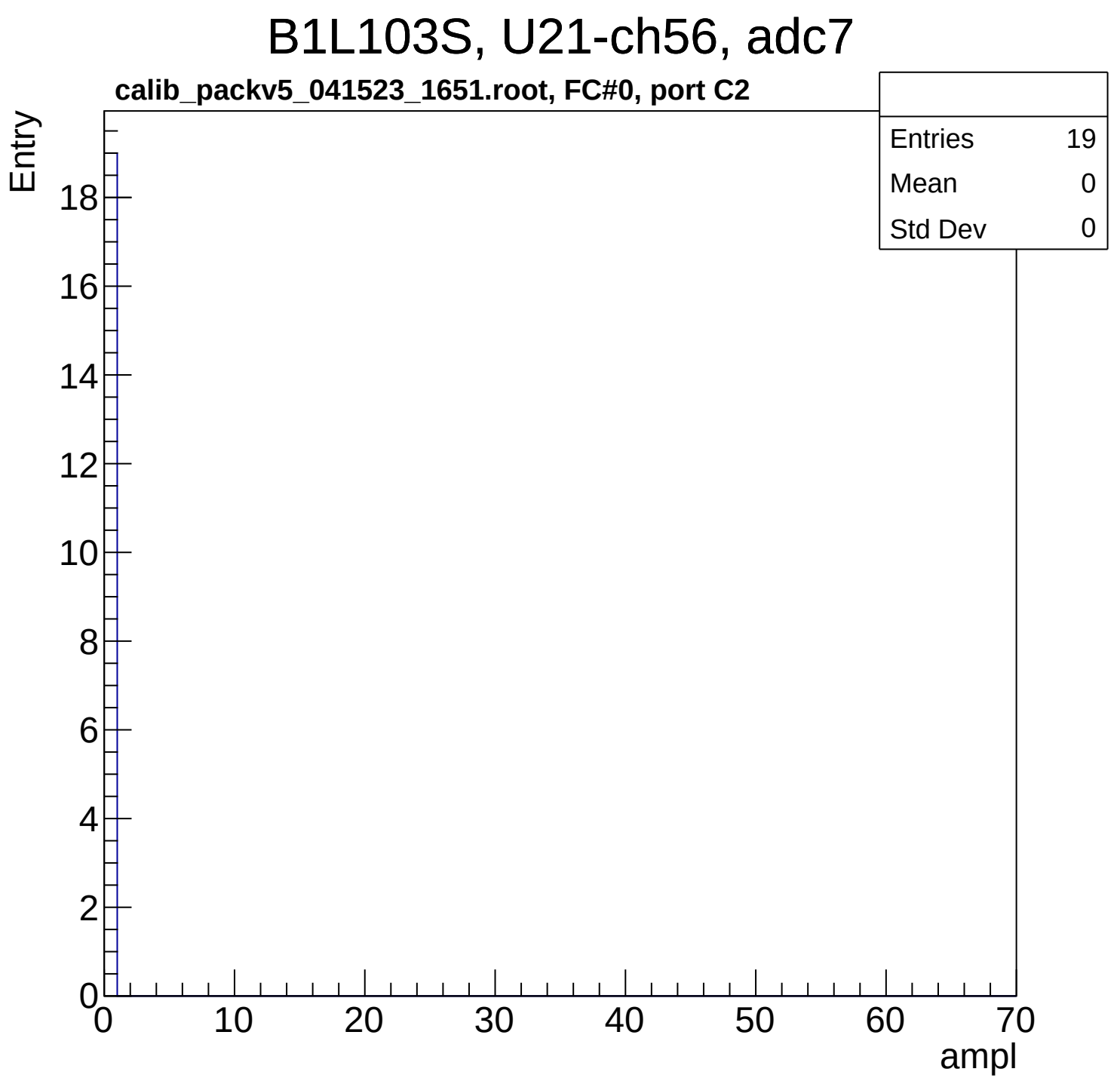
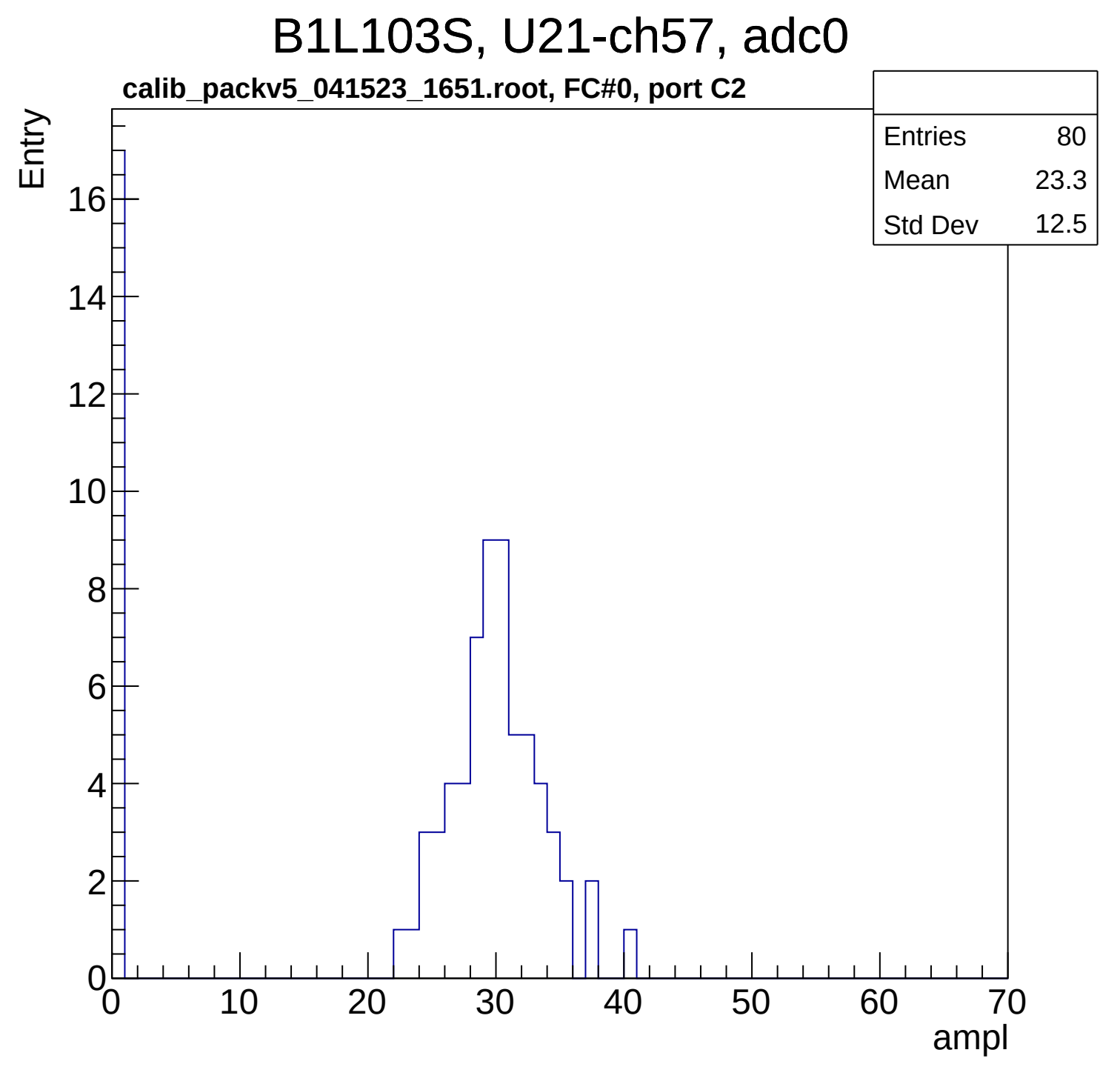
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch56, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch57, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 23.3
Std Dev 12.5
Entry
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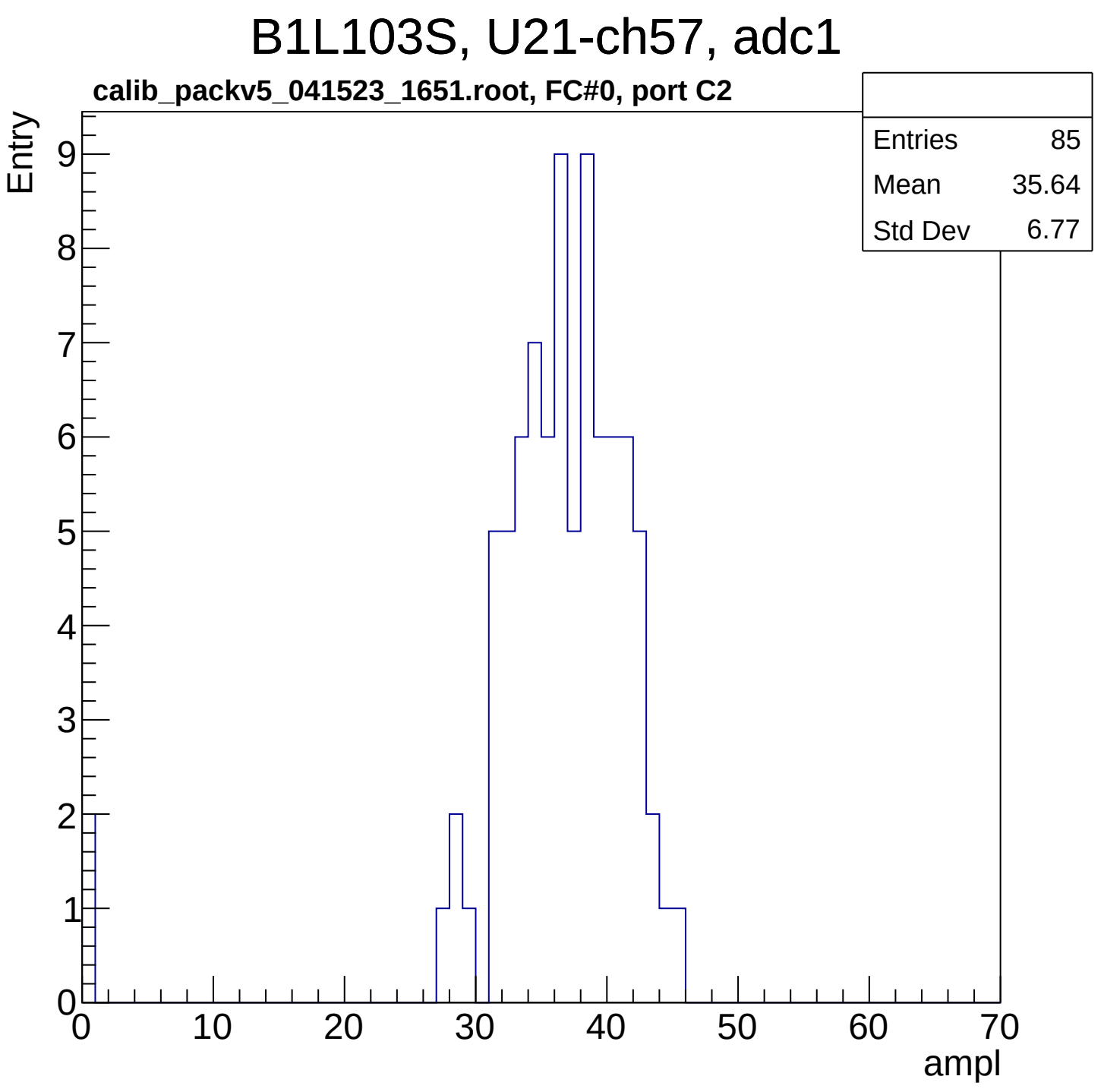
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch57, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 35.64
Std Dev 6.77
Entry
ampl
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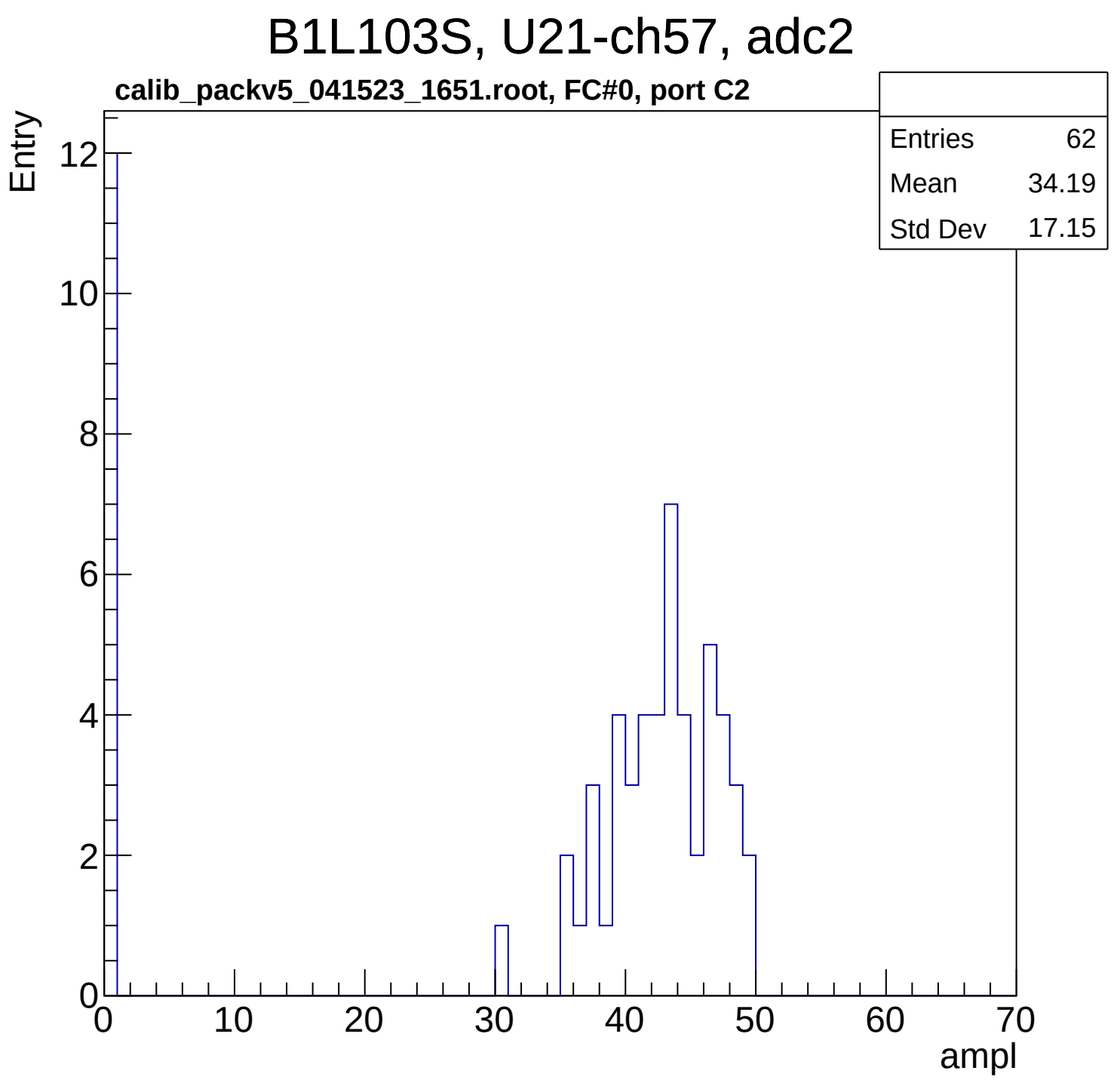
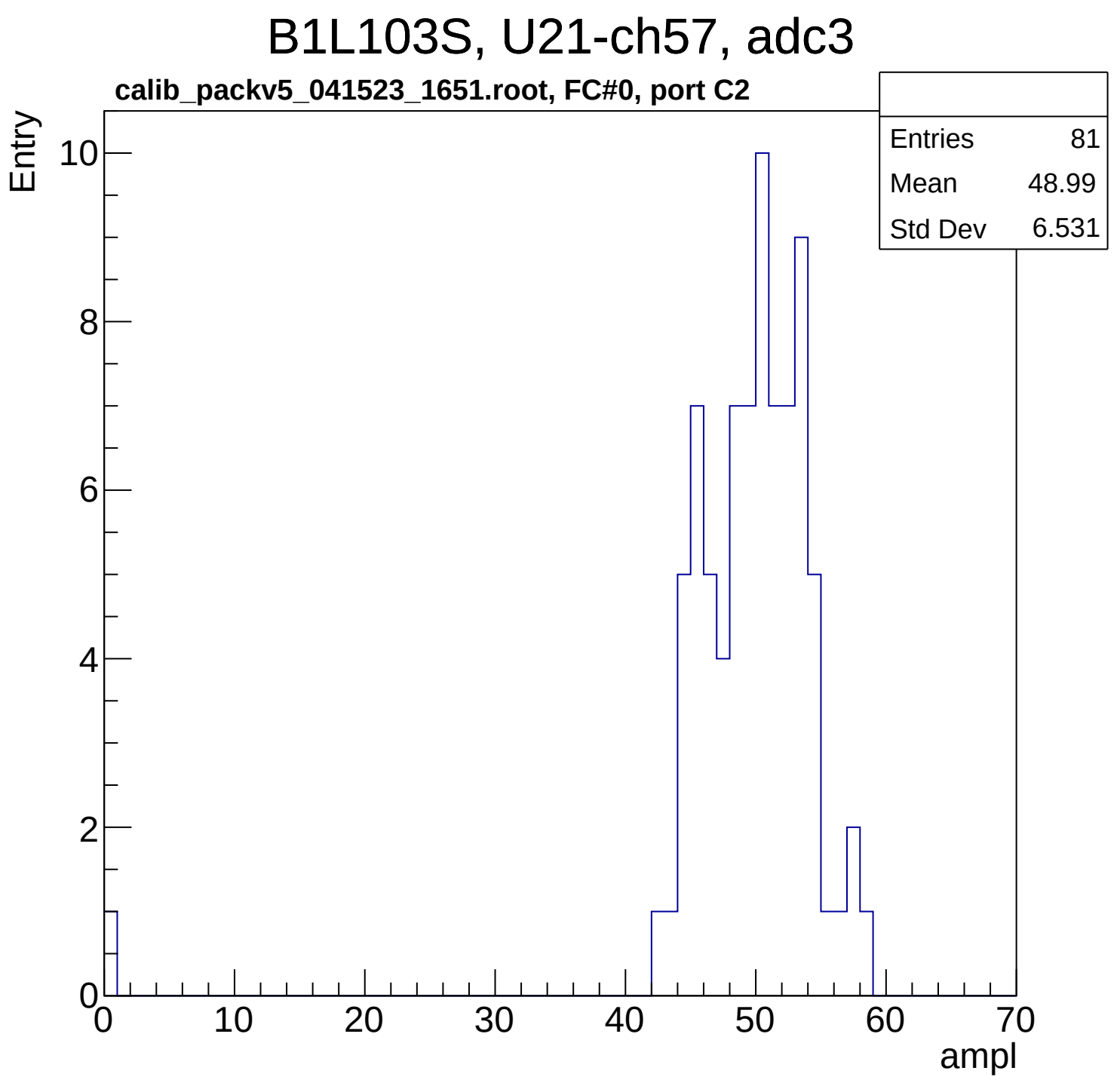
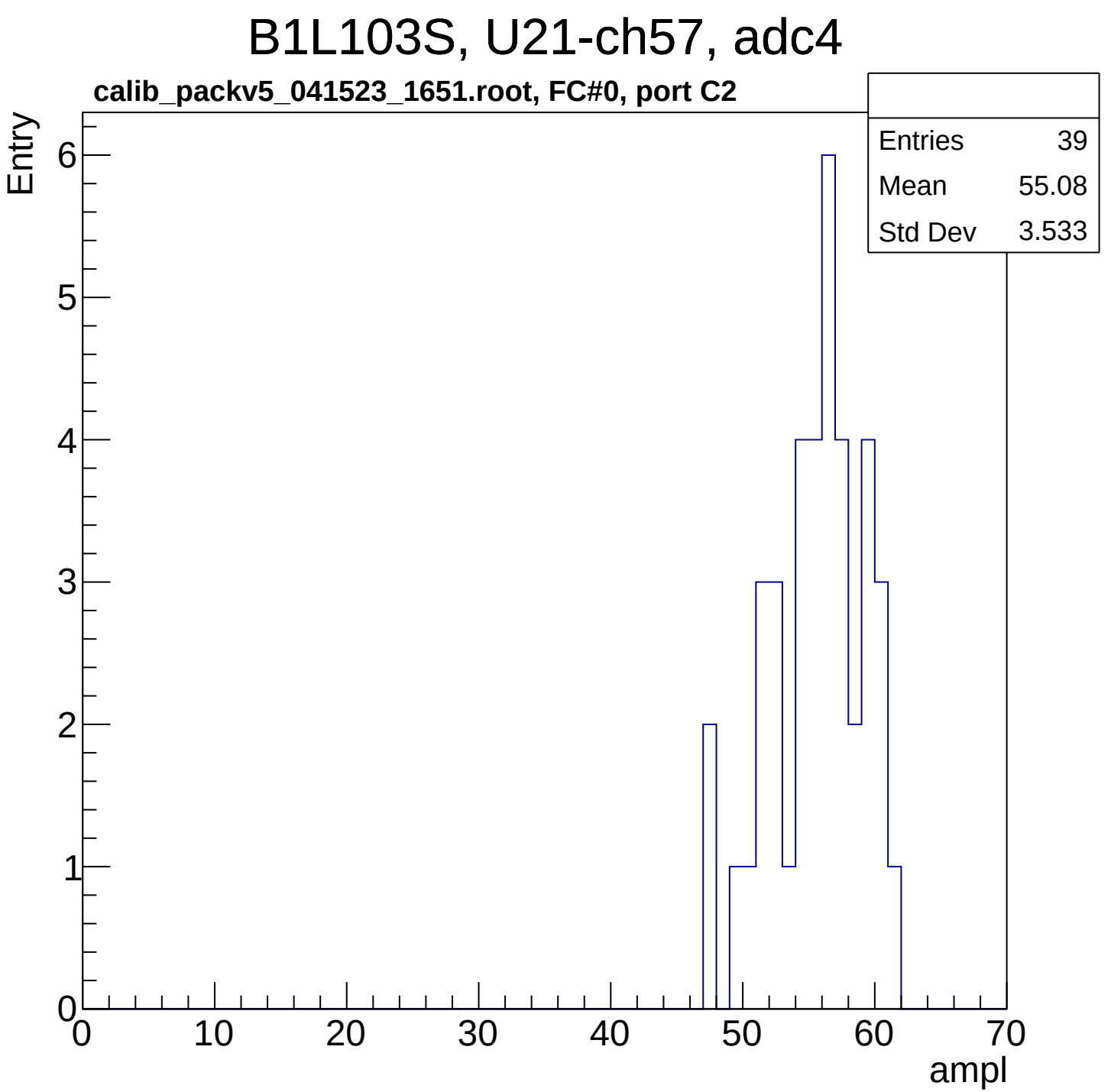
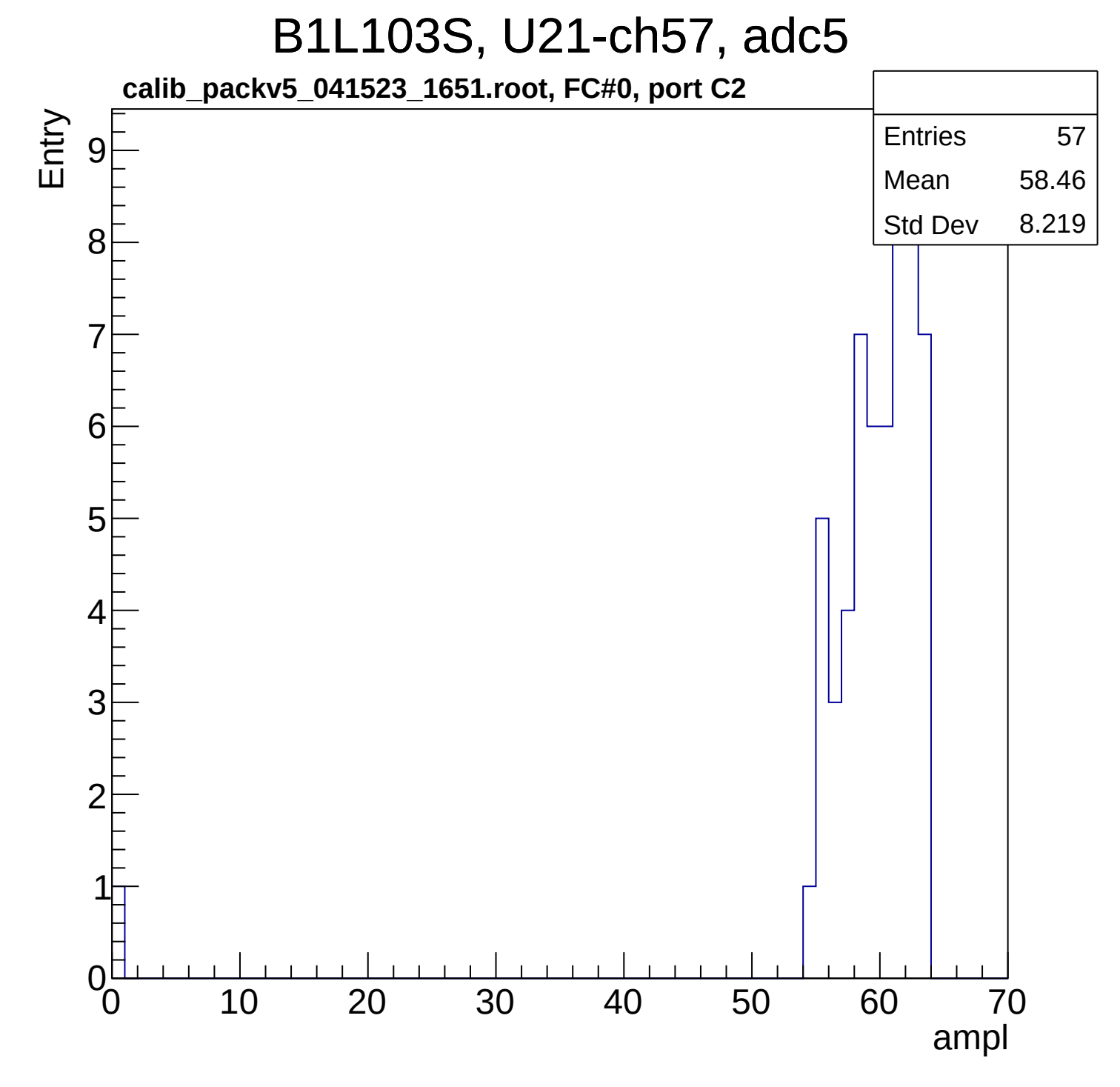
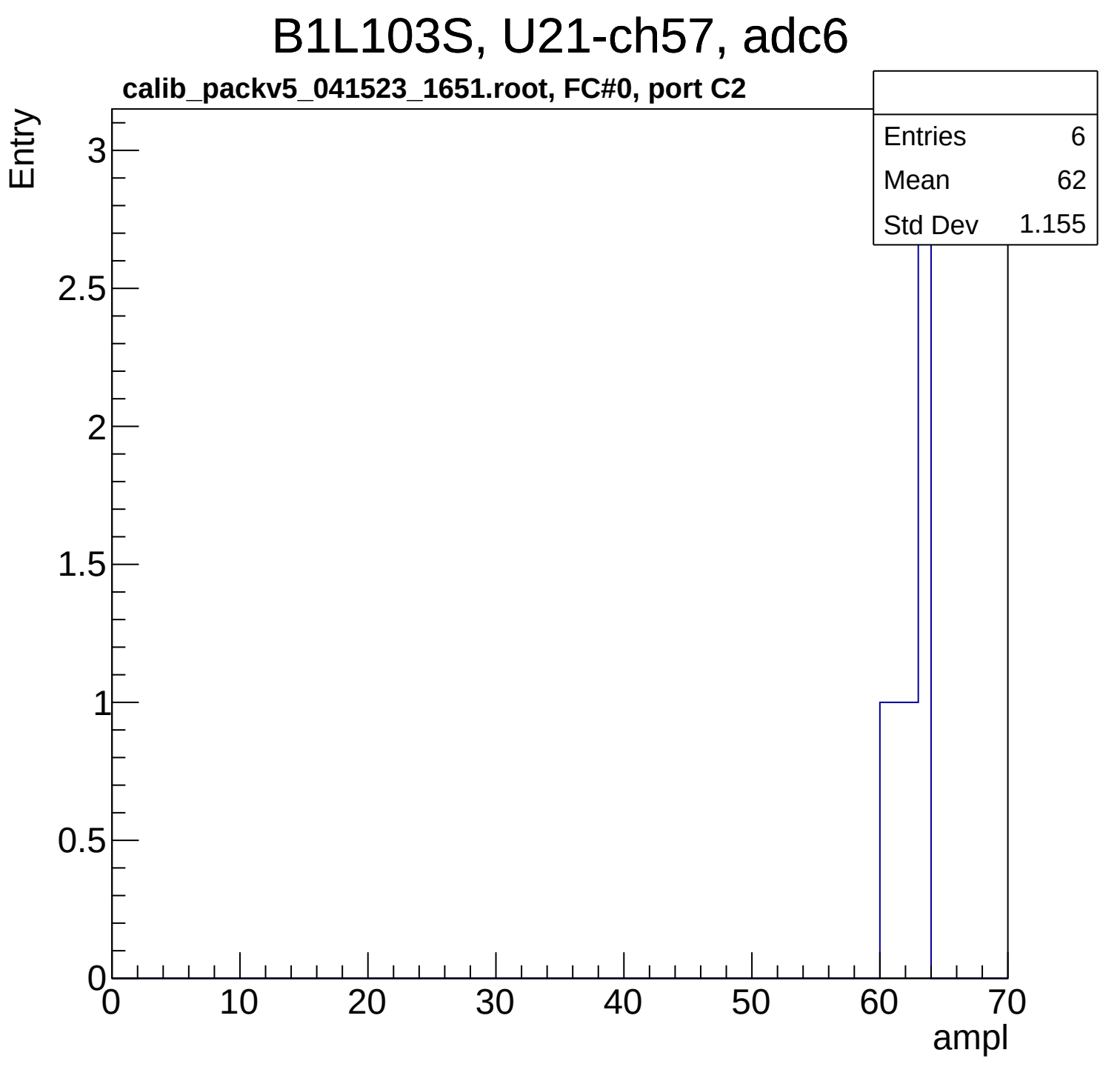
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

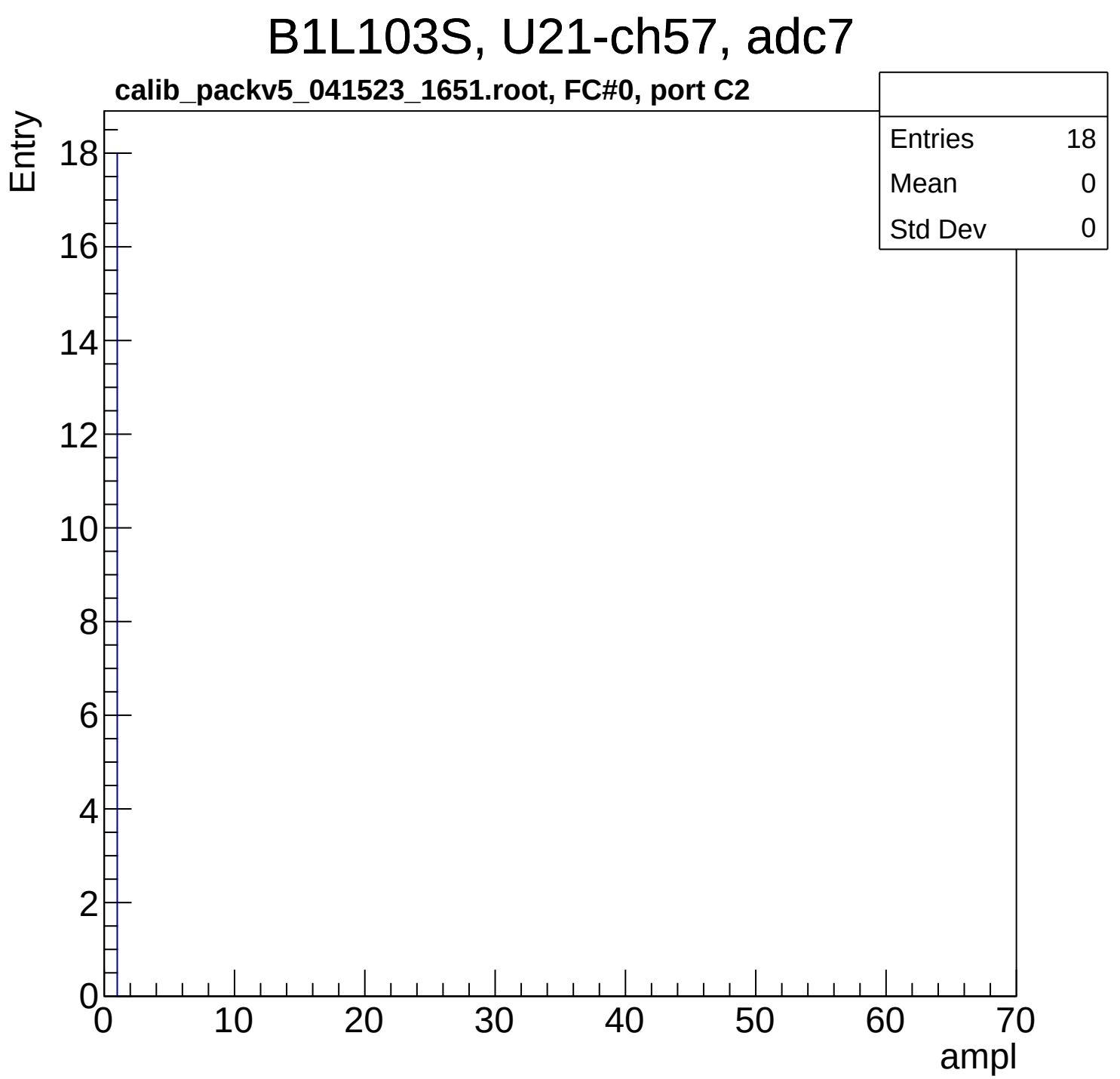

B1L103S, U21-ch57, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 34.19
Std Dev 17.15
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

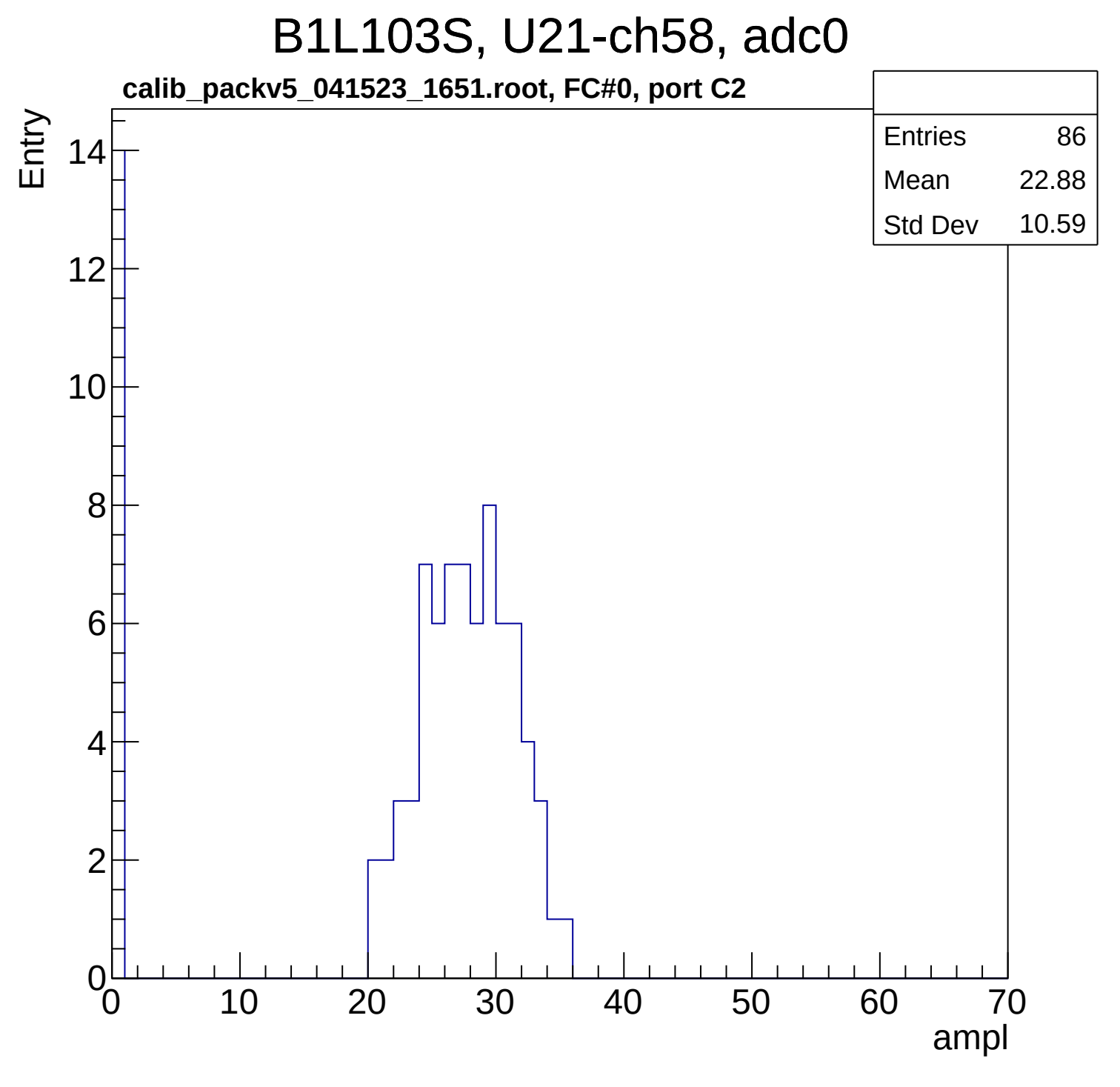

B1L103S, U21-ch57, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 48.99
Std Dev 6.531
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U21-ch57, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 55.08
Std Dev 3.533
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U21-ch57, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 58.46
Std Dev 8.219
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch57, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 62
Std Dev 1.155
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U21-ch57, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch58, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 22.88
Std Dev 10.59
Entry
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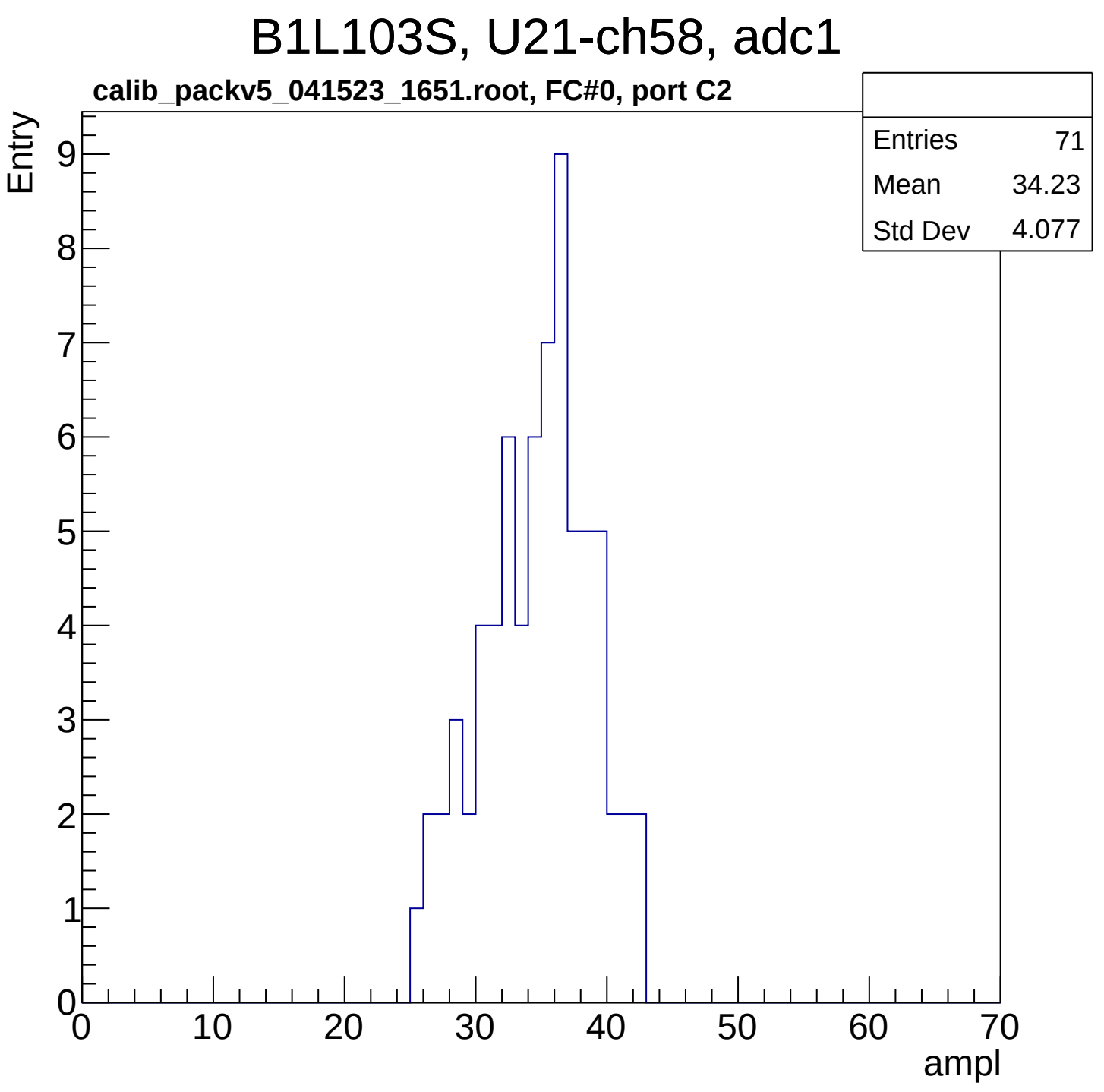
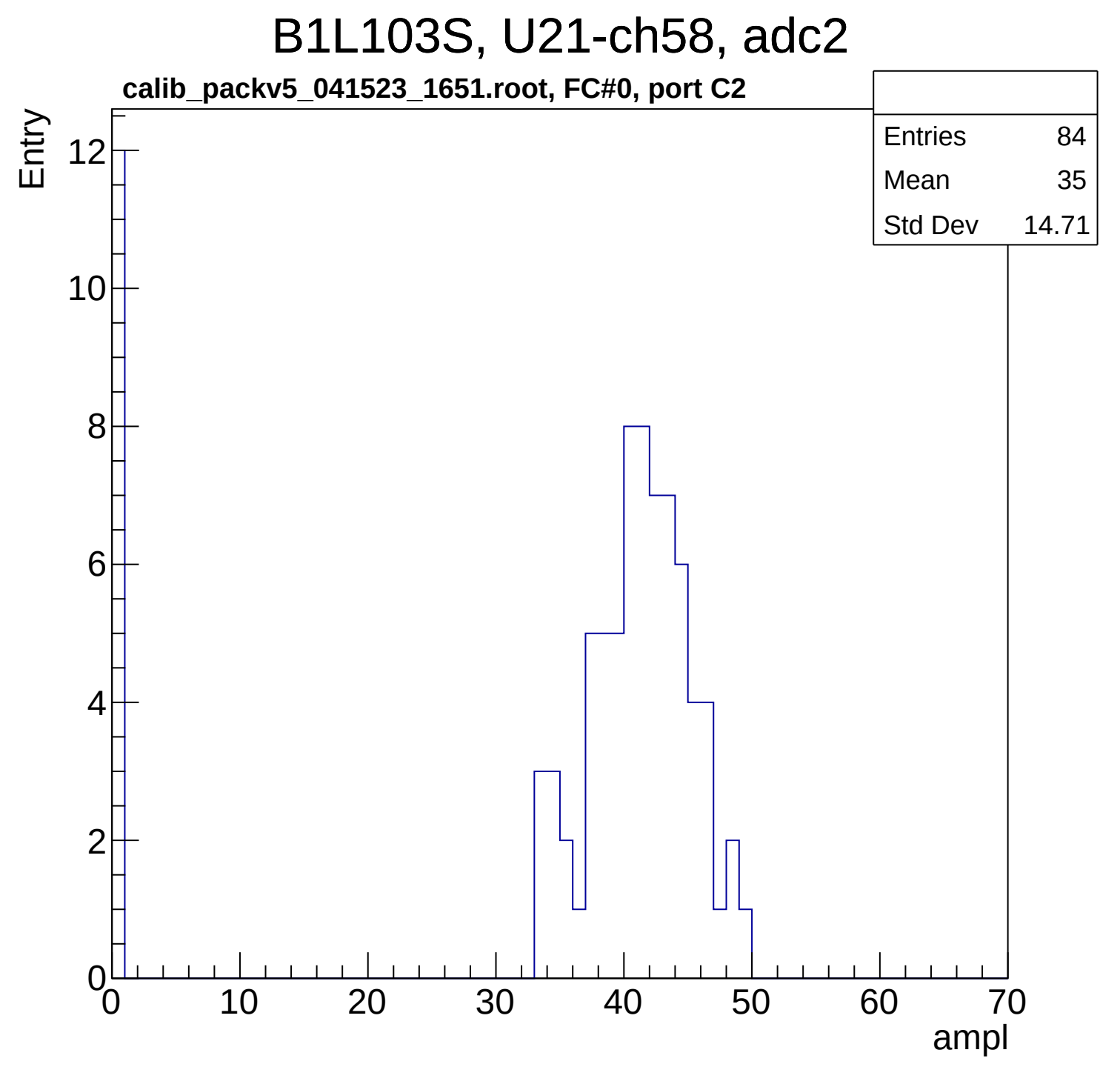
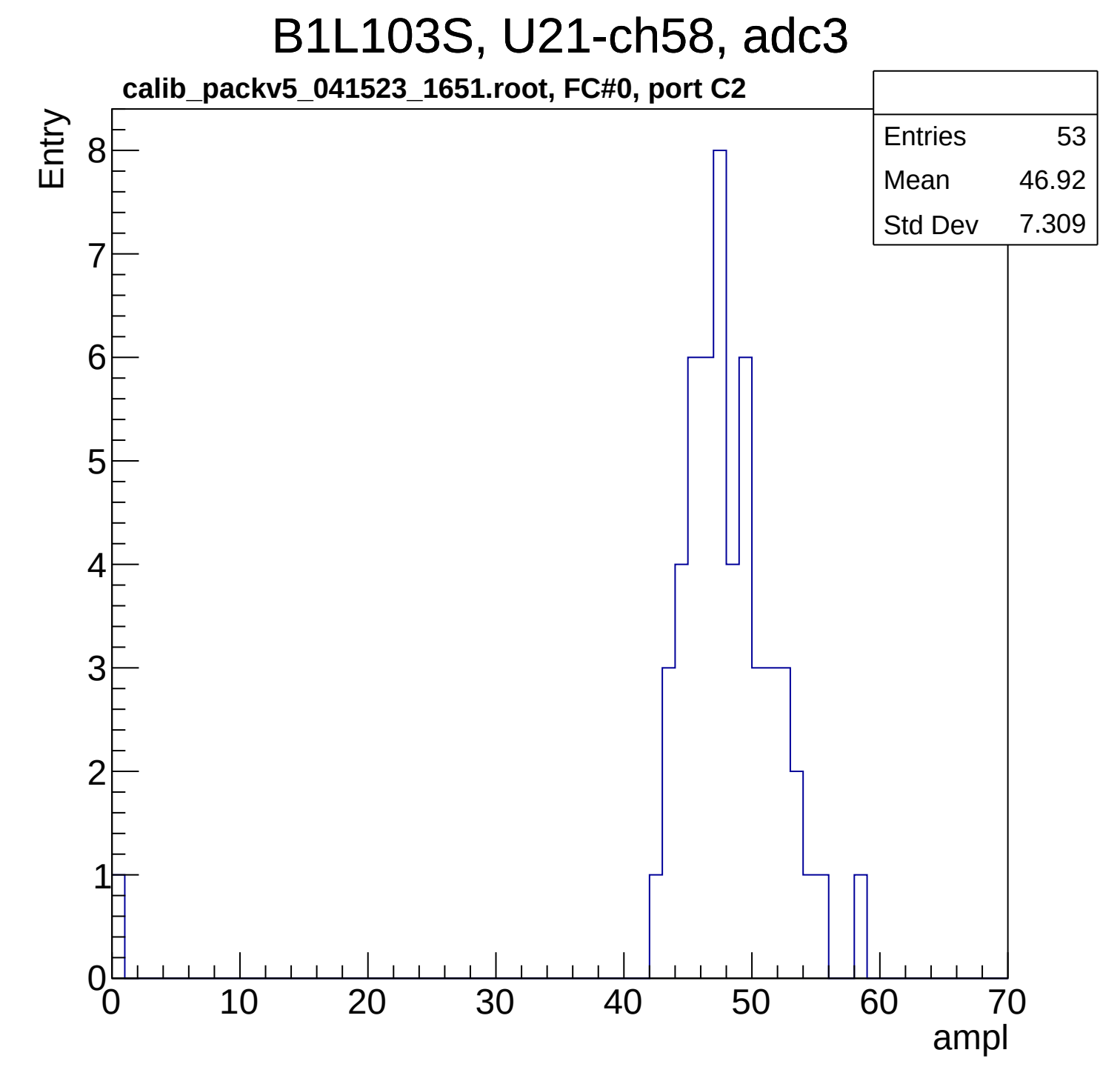
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch58, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 34.23
Std Dev 4.077
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch58, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 35
Std Dev 14.71
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch58, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 46.92
Std Dev 7.309
Entry
ampl
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2
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4
5
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7
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0
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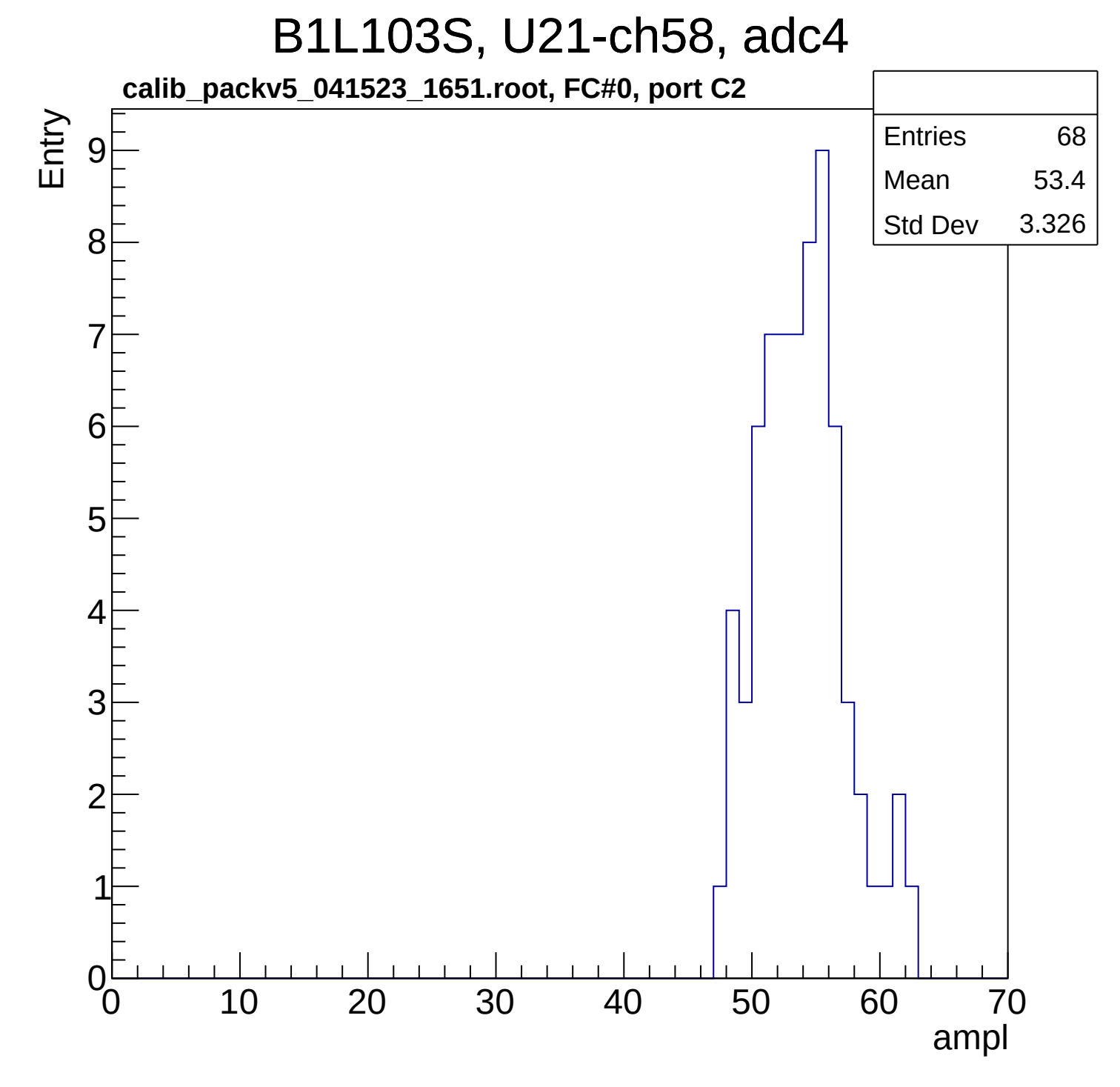
B1L103S, U21-ch58, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 53.4
Std Dev 3.326
Entry
ampl
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6
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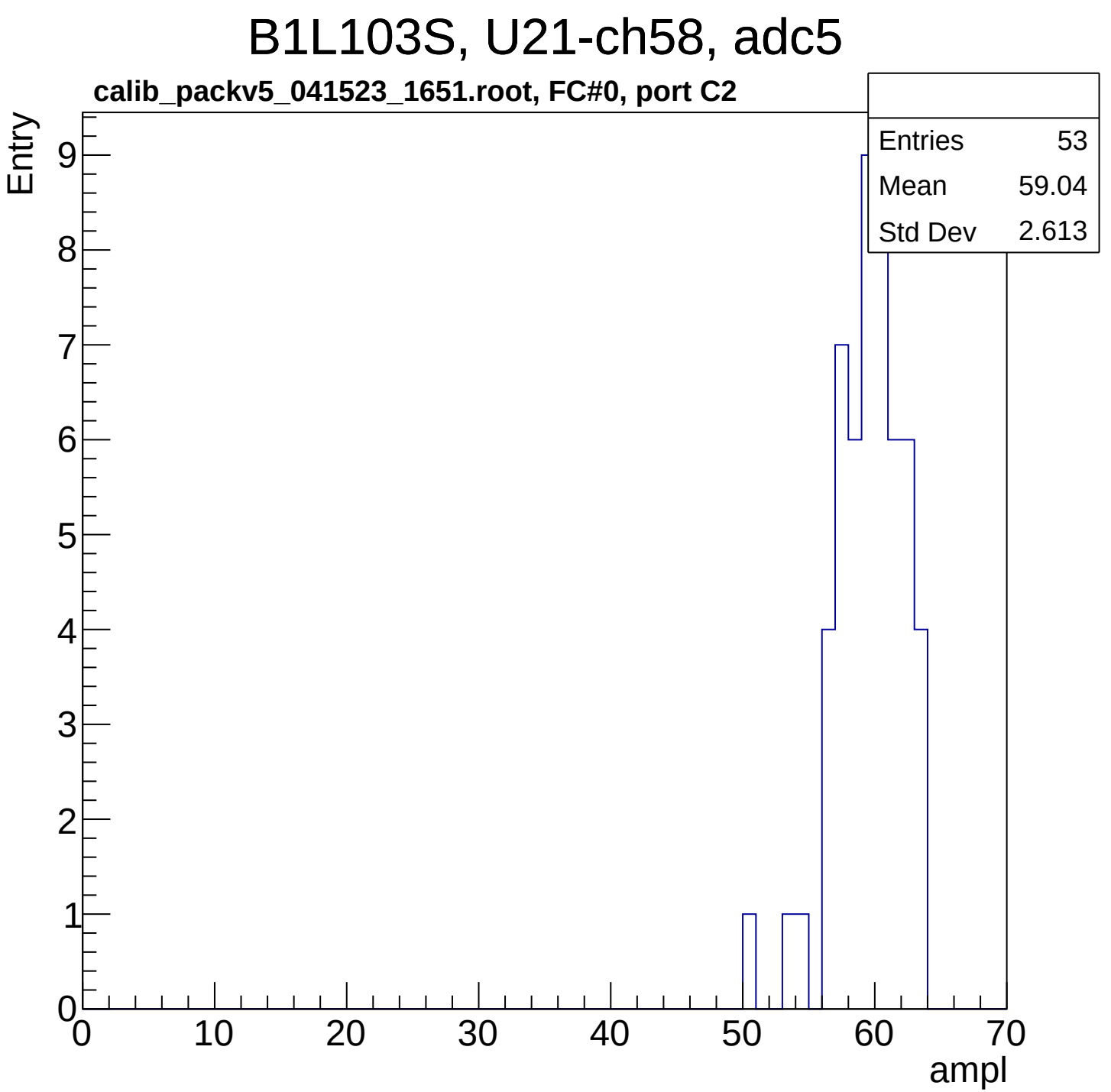
B1L103S, U21-ch58, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 59.04
Std Dev 2.613
Entry
ampl
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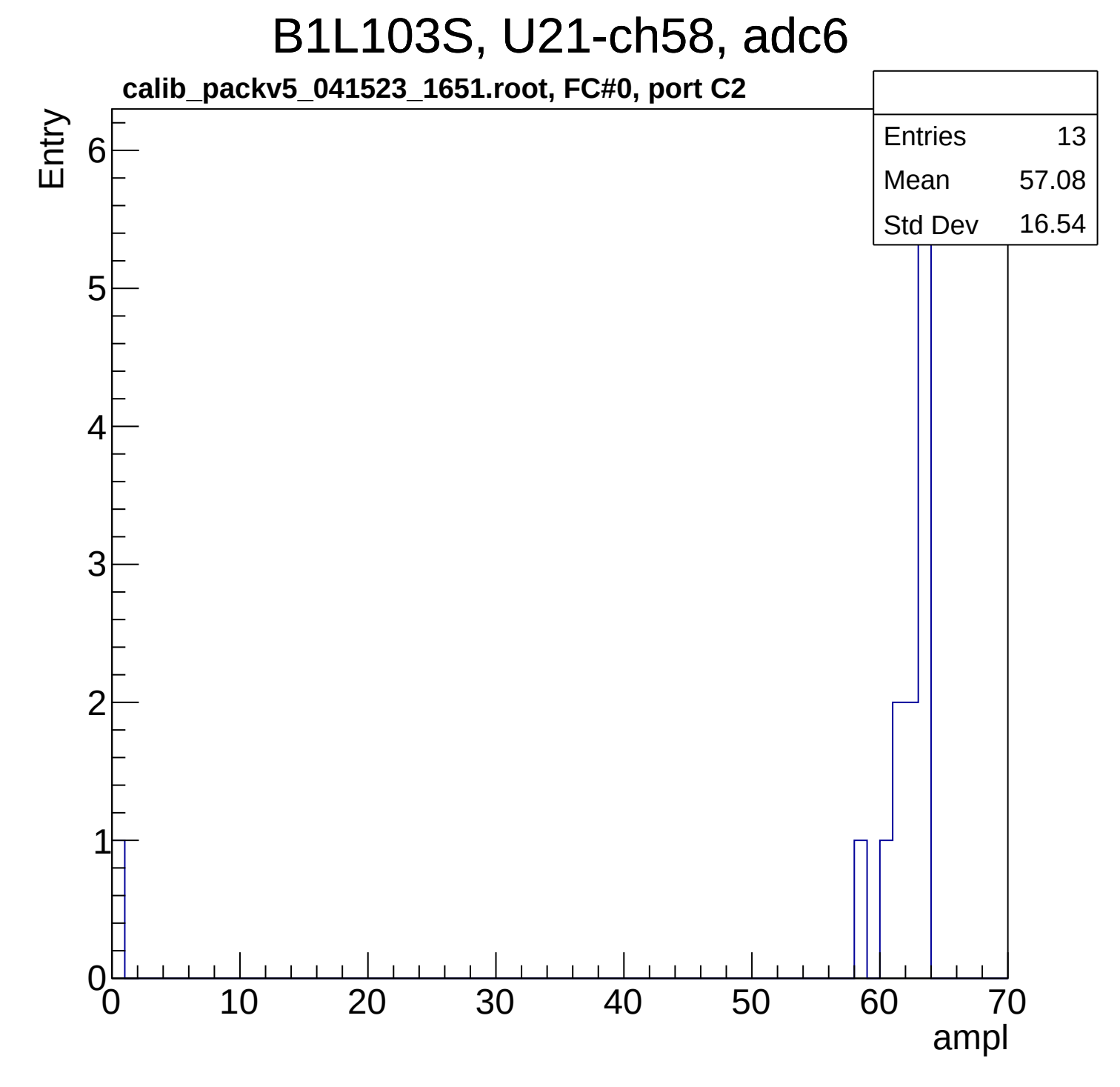
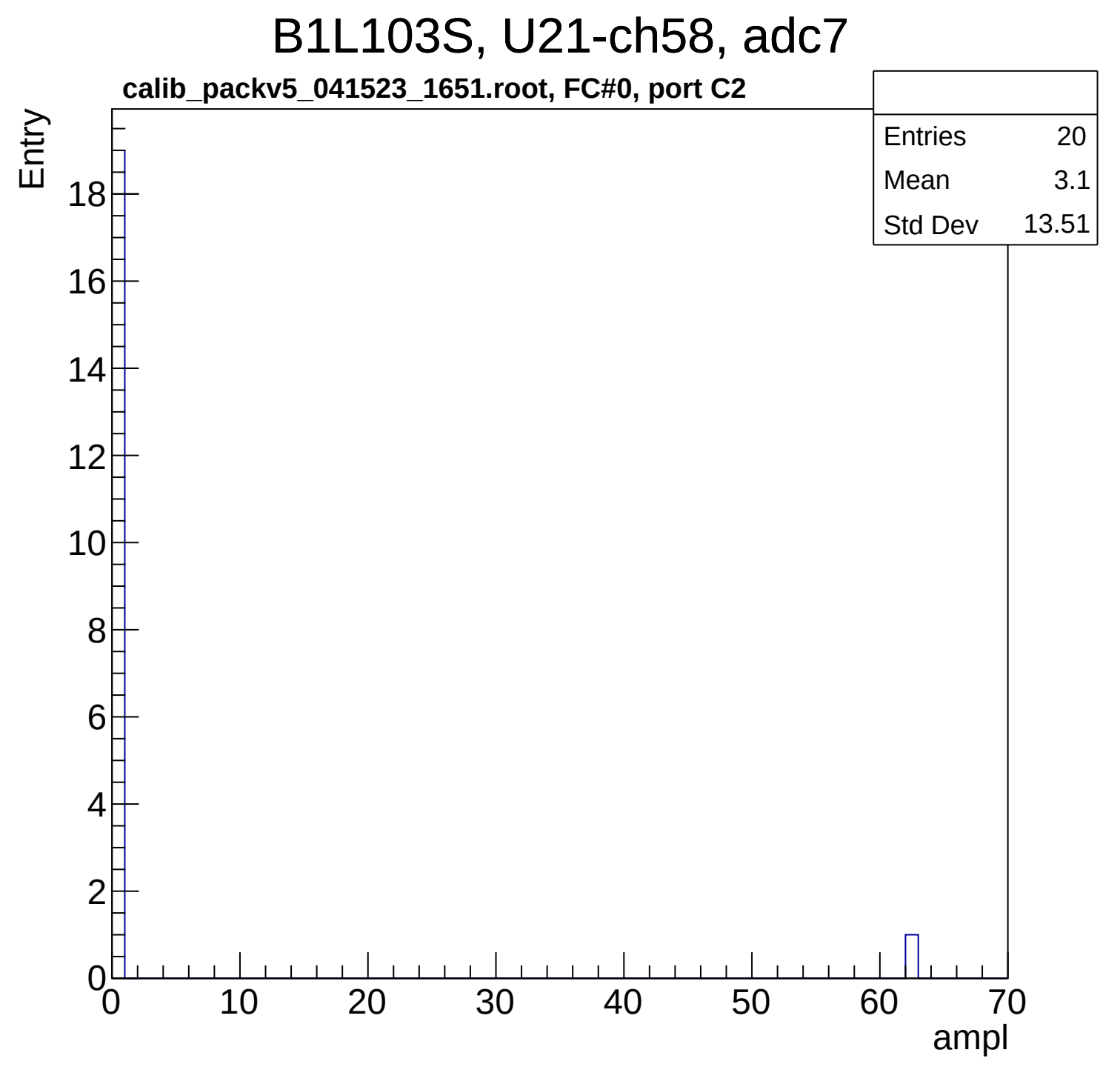

B1L103S, U21-ch58, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 57.08
Std Dev 16.54
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch58, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
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6
8
10
12
14
16
18
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10
20
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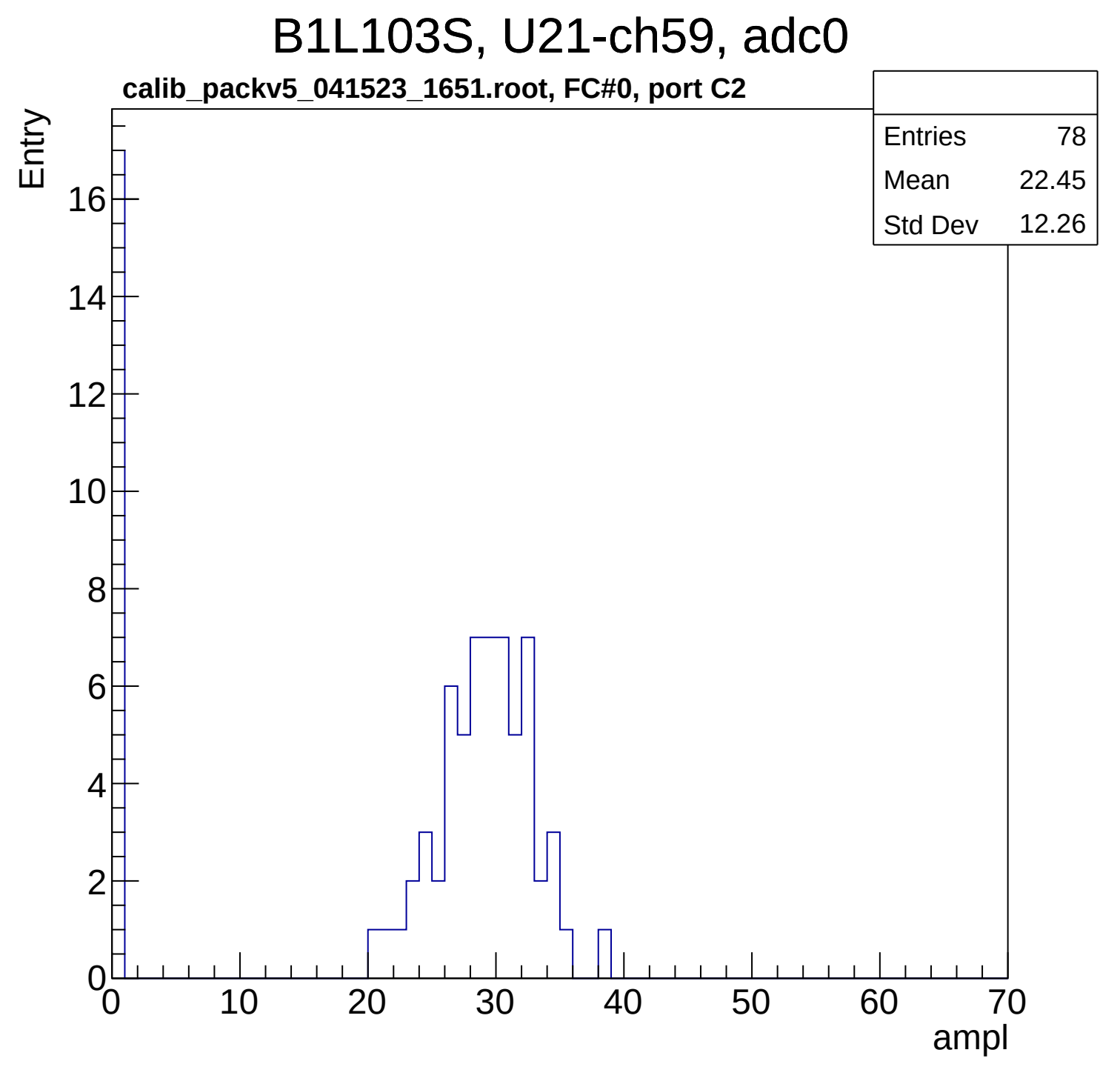
50
60
70
ampl


B1L103S, U21-ch59, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 22.45
Std Dev 12.26
Entry
0
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4
6
8
10
12
14
16
0
10
20
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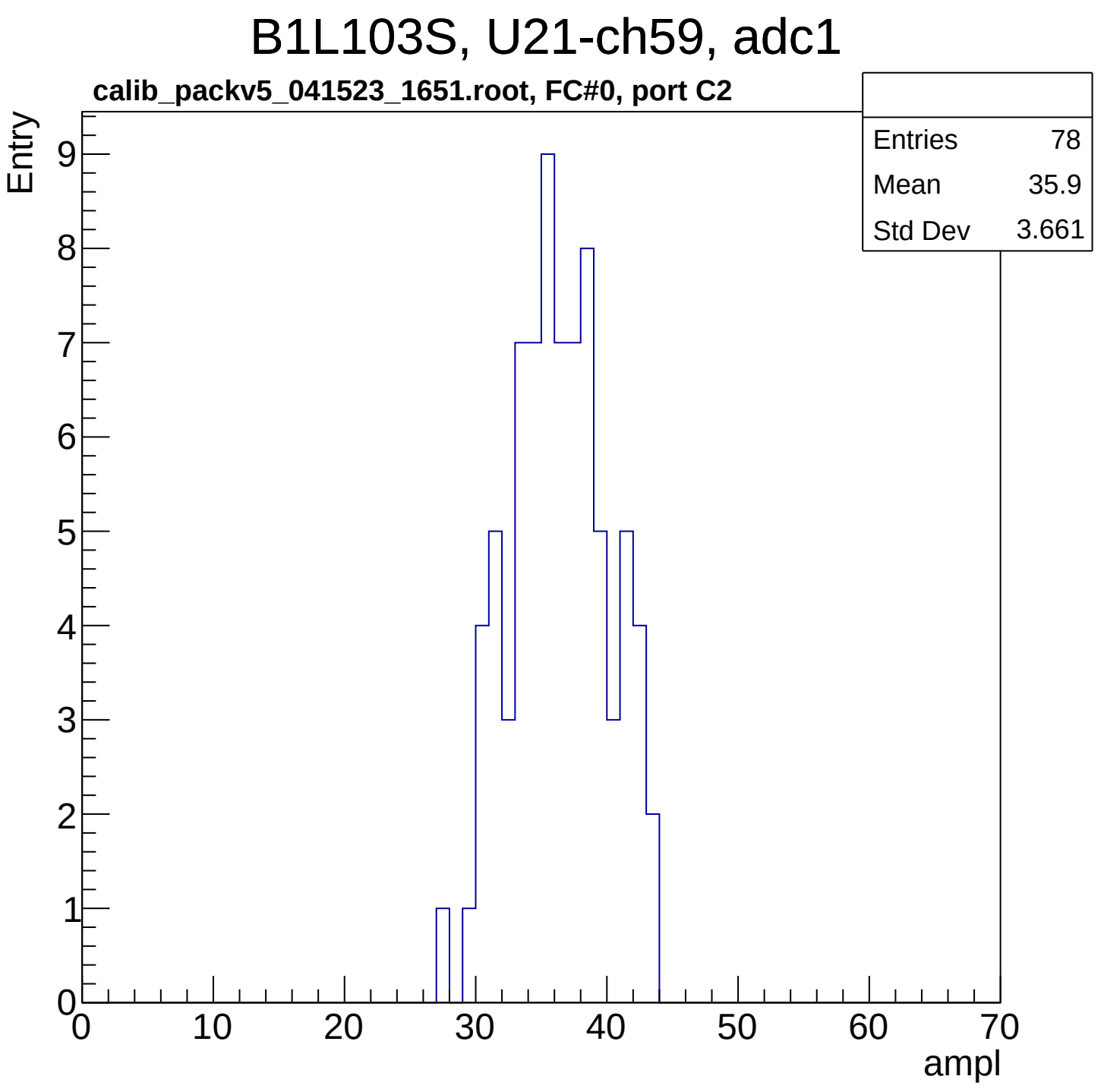
40
50
60
70
ampl


B1L103S, U21-ch59, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 35.9
Std Dev 3.661
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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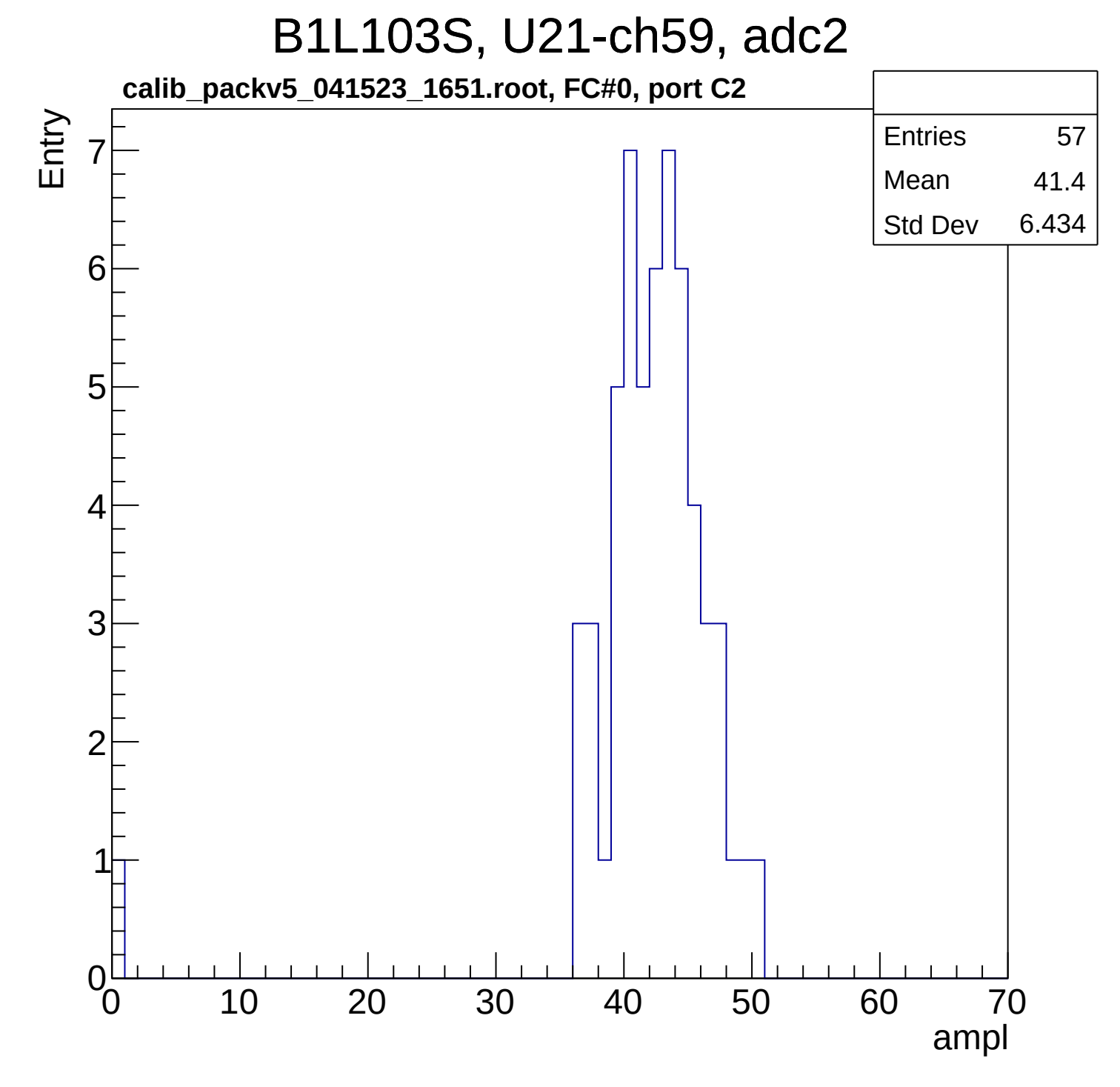
B1L103S, U21-ch59, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 41.4
Std Dev 6.434
Entry
ampl
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1
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3
4
5
6
7
0
10
20
30
40
50
60
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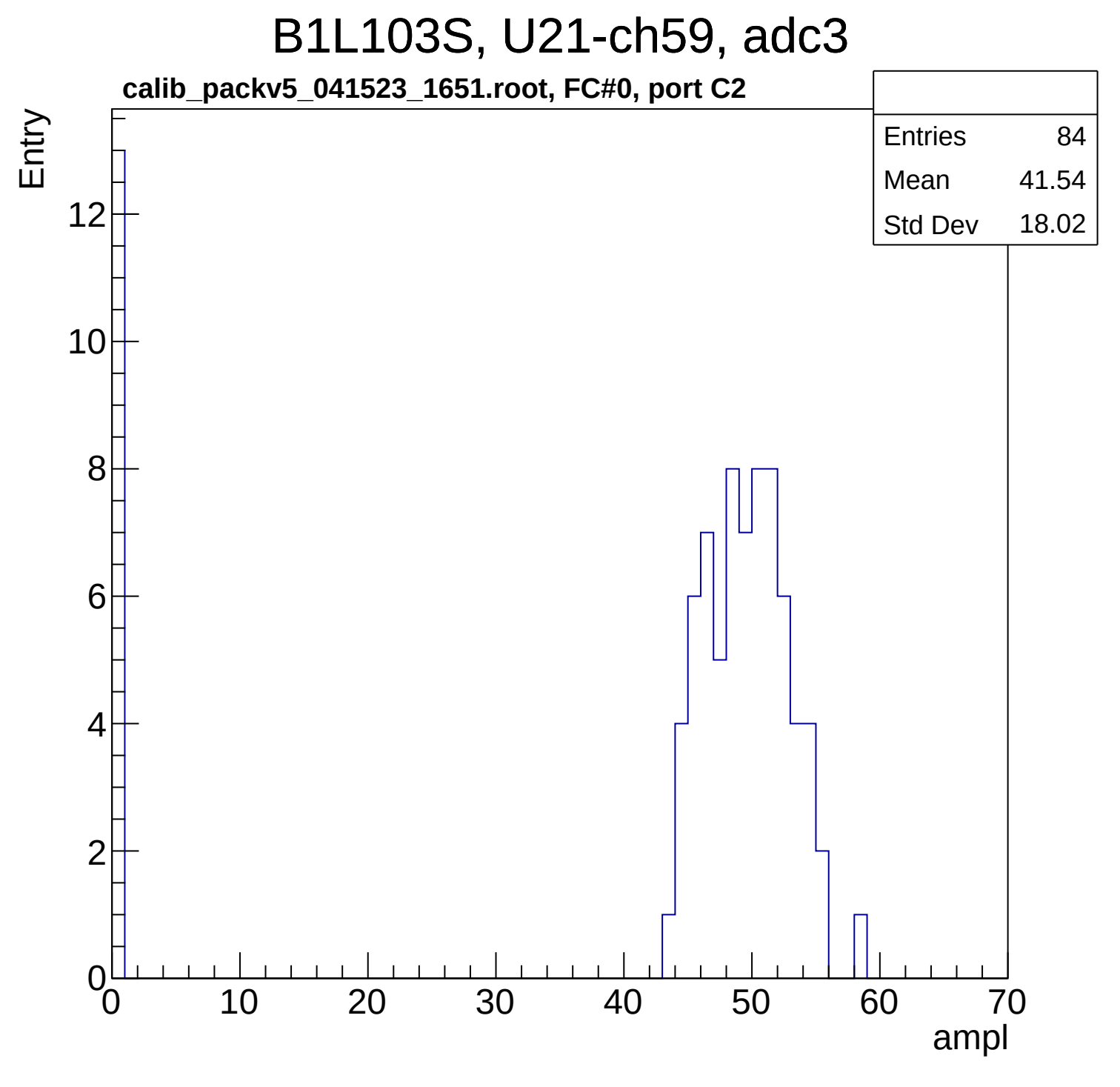
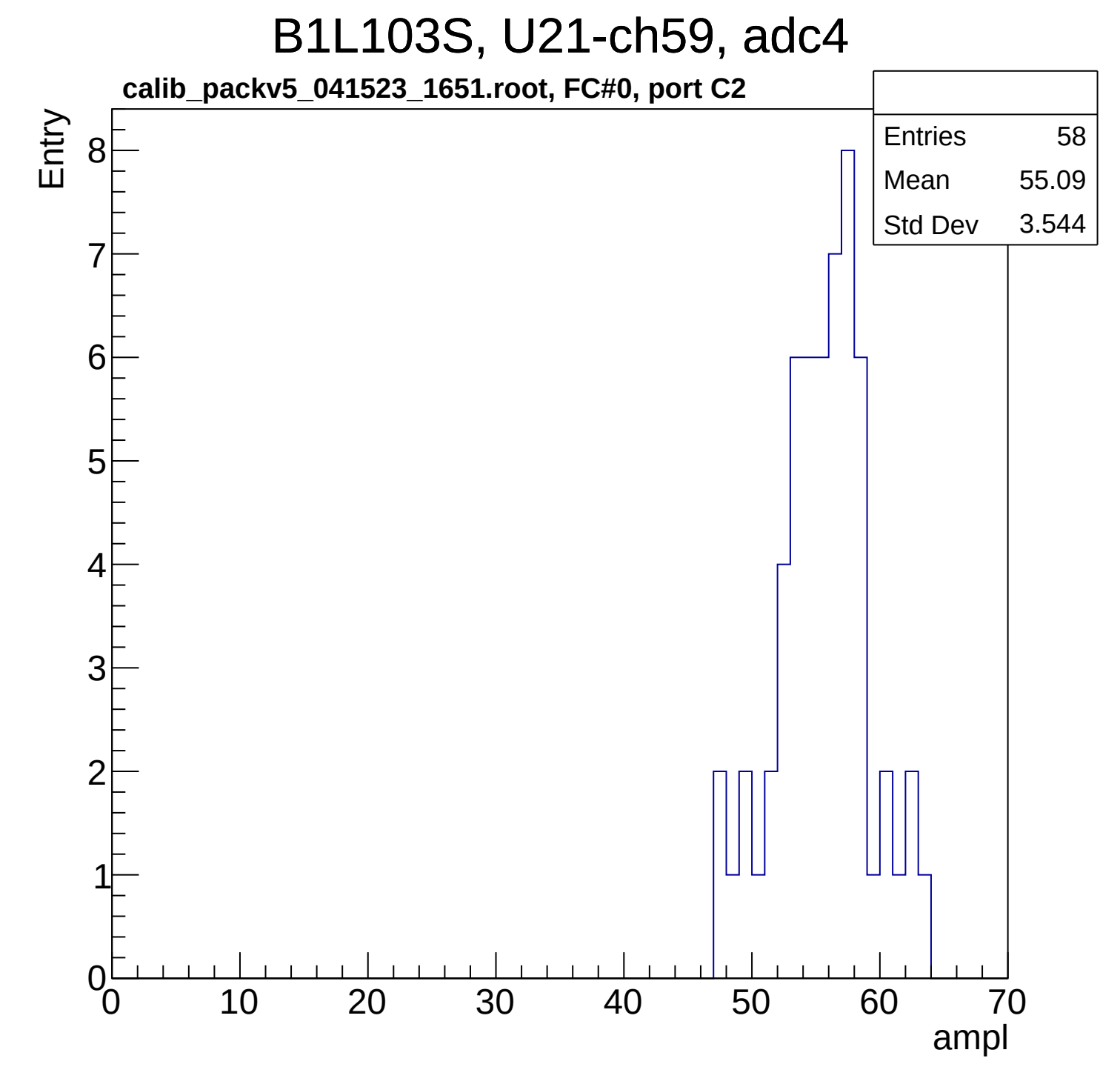

B1L103S, U21-ch59, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 41.54
Std Dev 18.02
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch59, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 55.09
Std Dev 3.544
Entry
ampl
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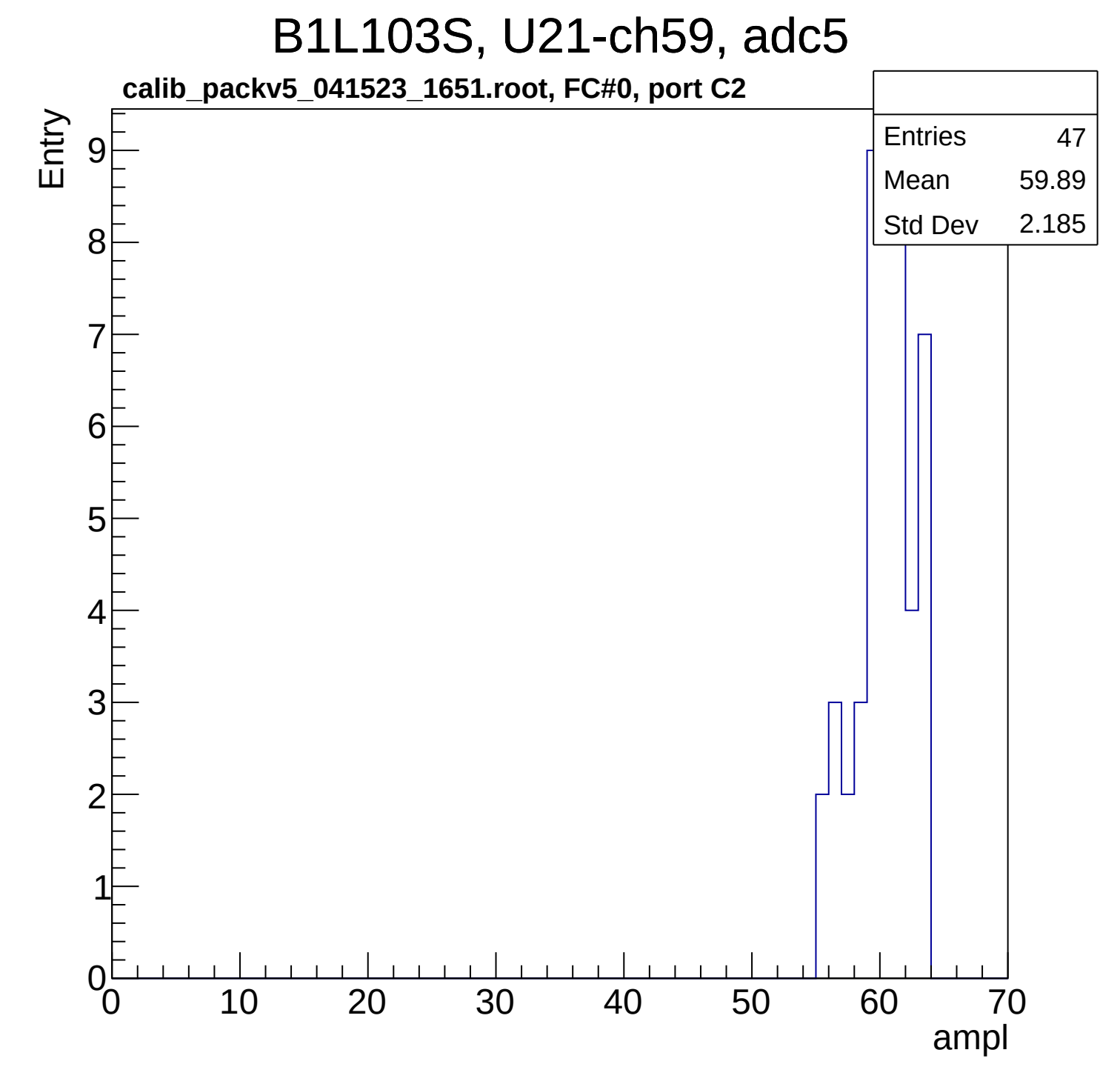
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch59, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 59.89
Std Dev 2.185
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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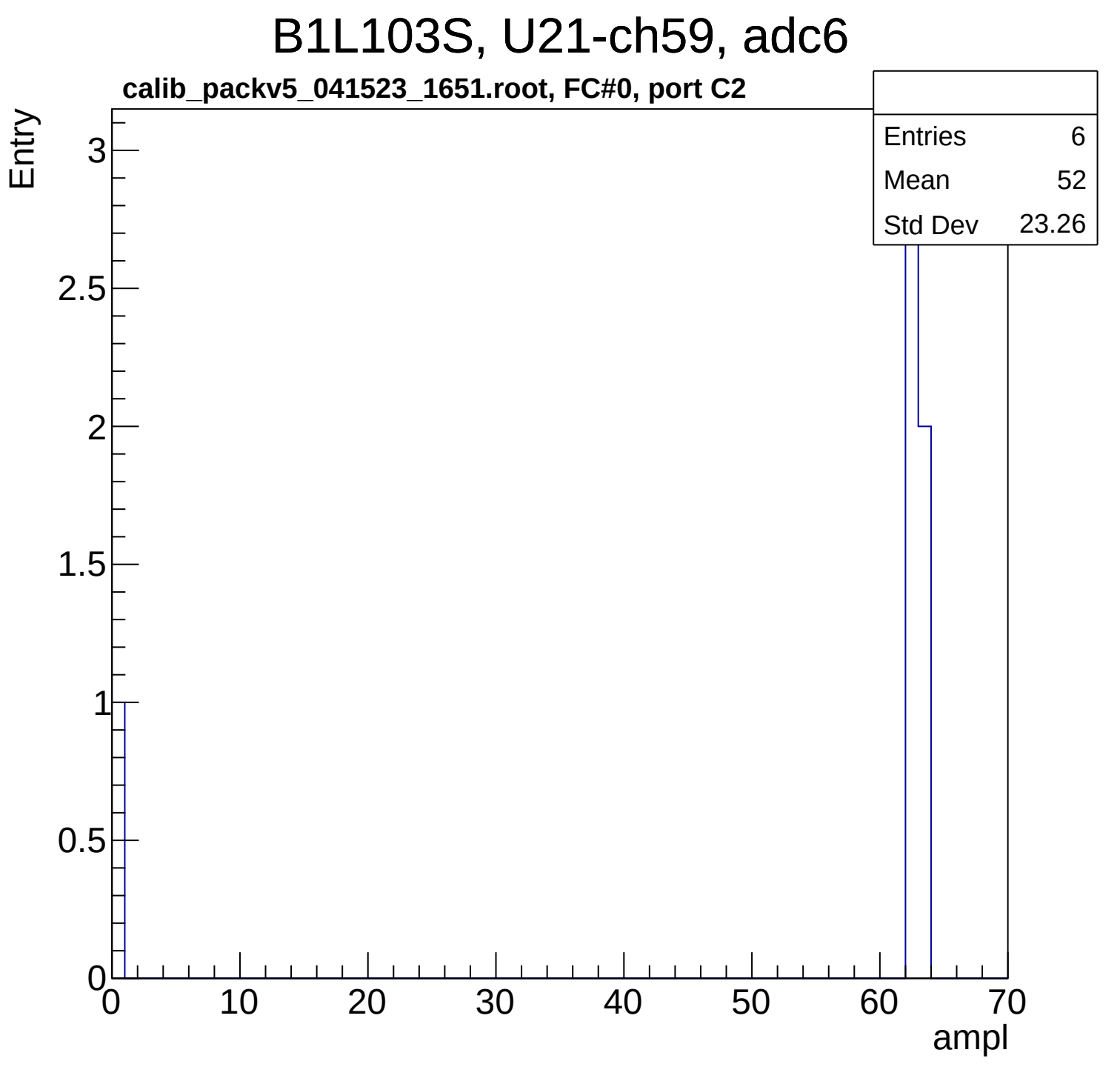
B1L103S, U21-ch59, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 52
Std Dev 23.26
Entry
ampl
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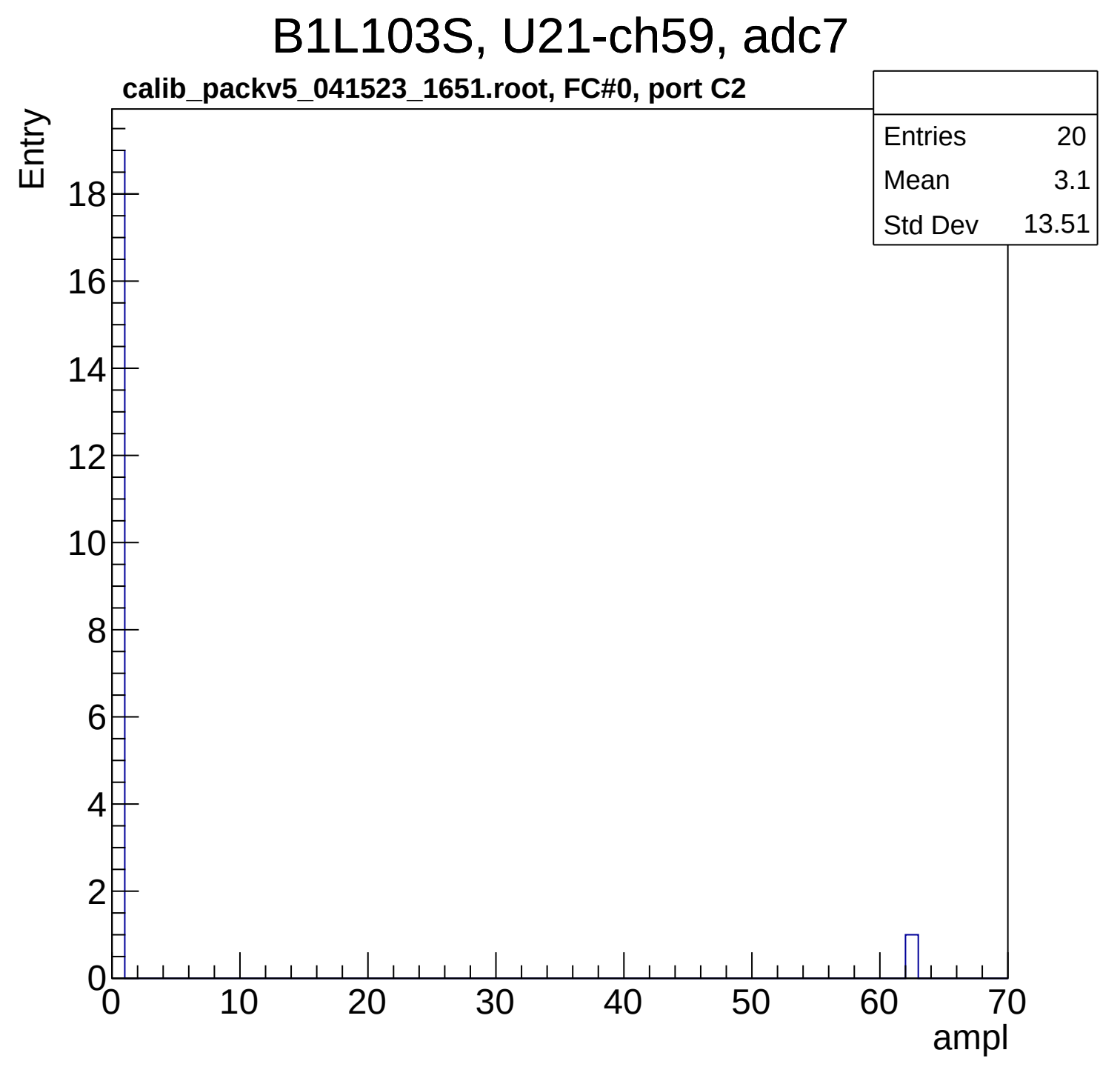
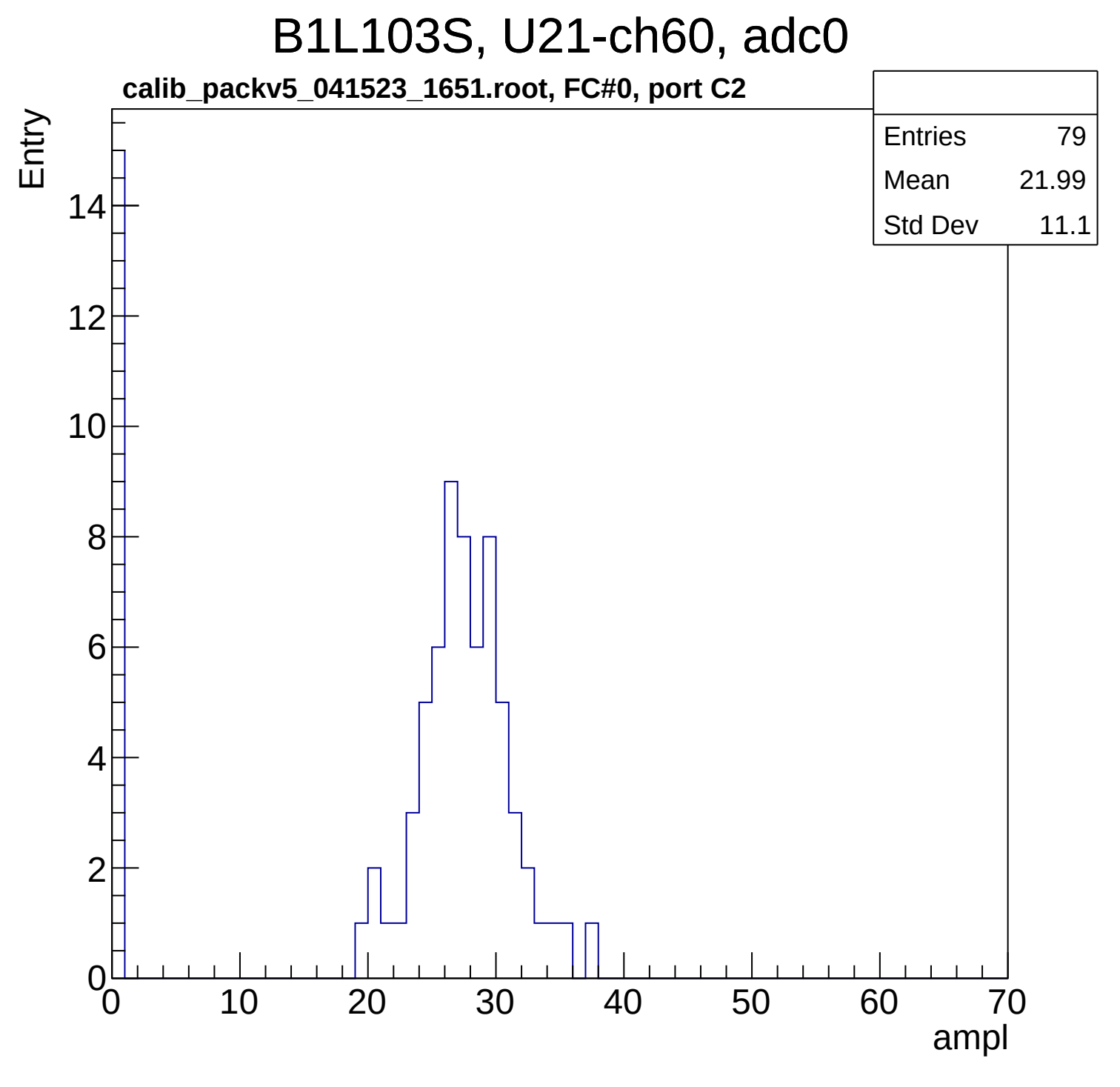
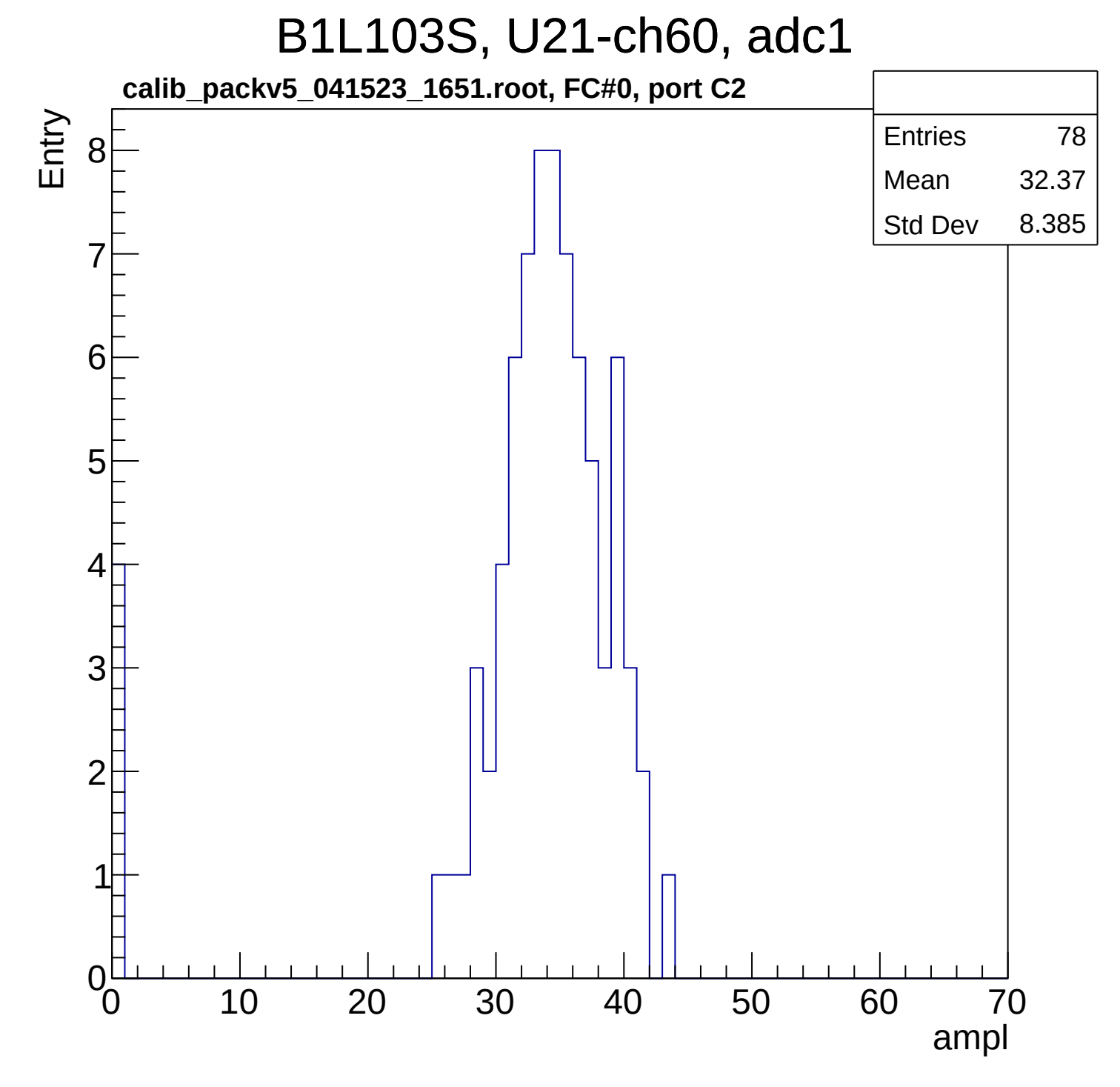
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U21-ch59, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch60, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 21.99
Std Dev 11.1
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch60, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 32.37
Std Dev 8.385
Entry
ampl
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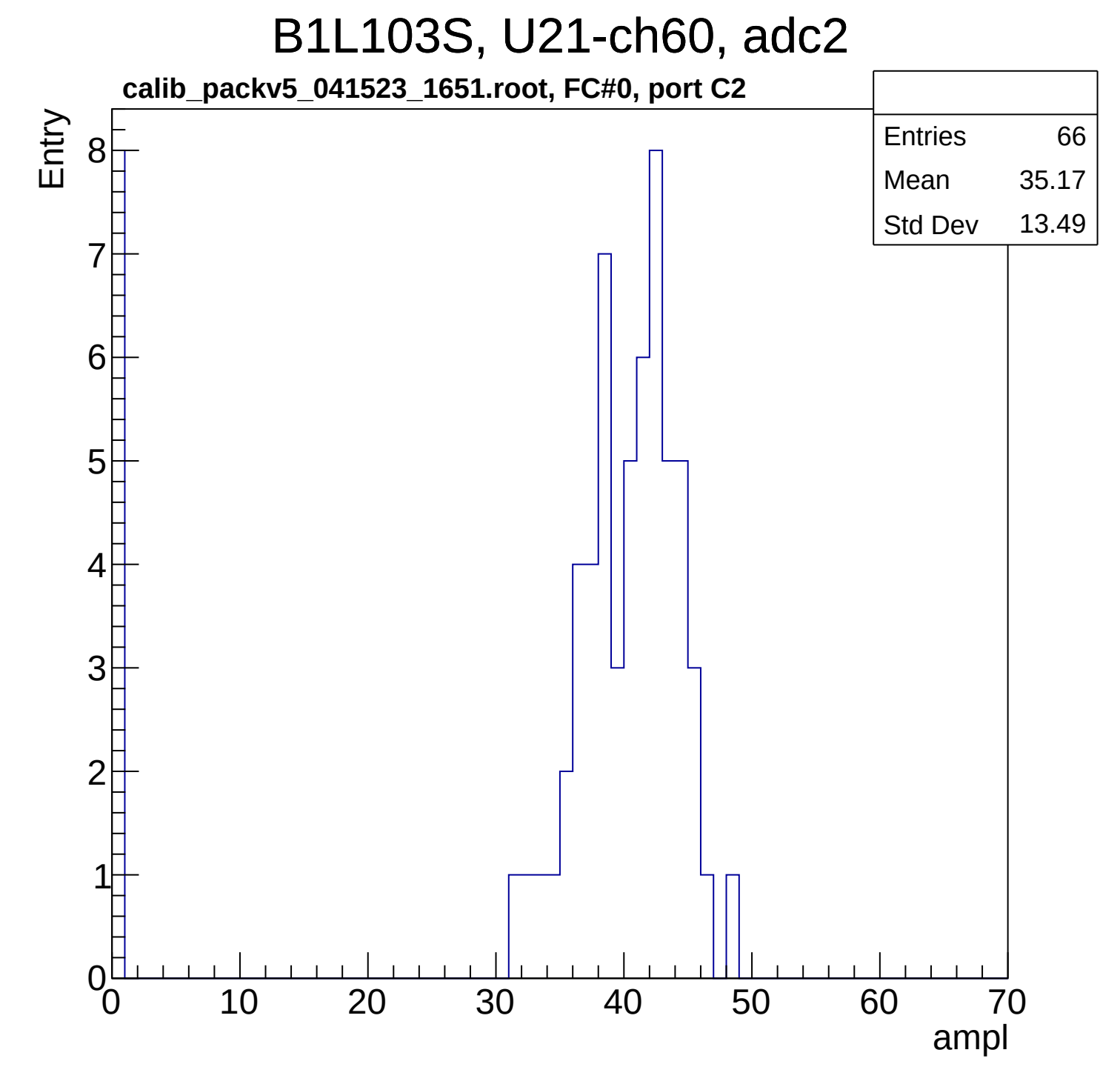
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch60, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 35.17
Std Dev 13.49
Entry
ampl
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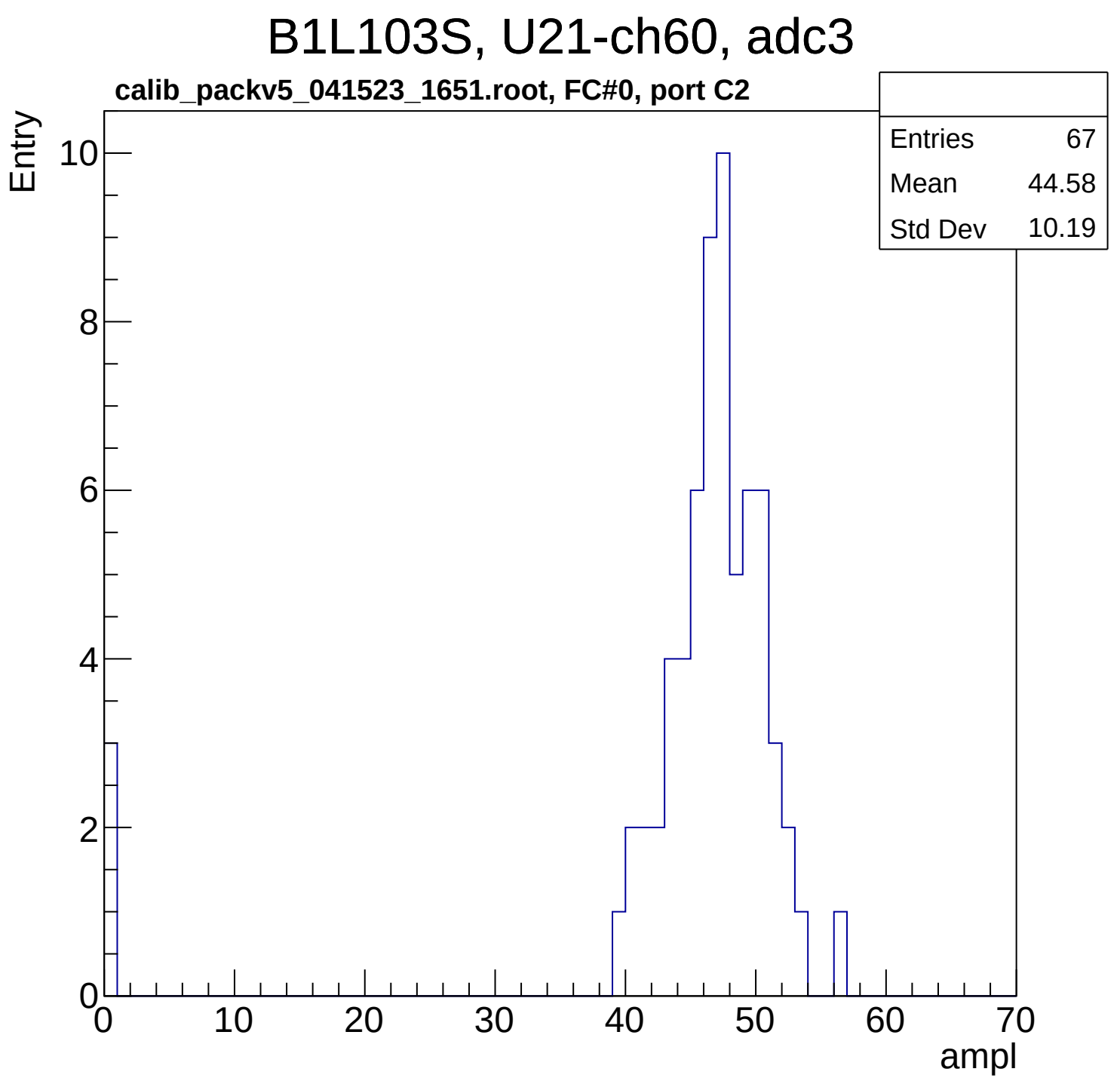
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch60, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 44.58
Std Dev 10.19
Entry
ampl
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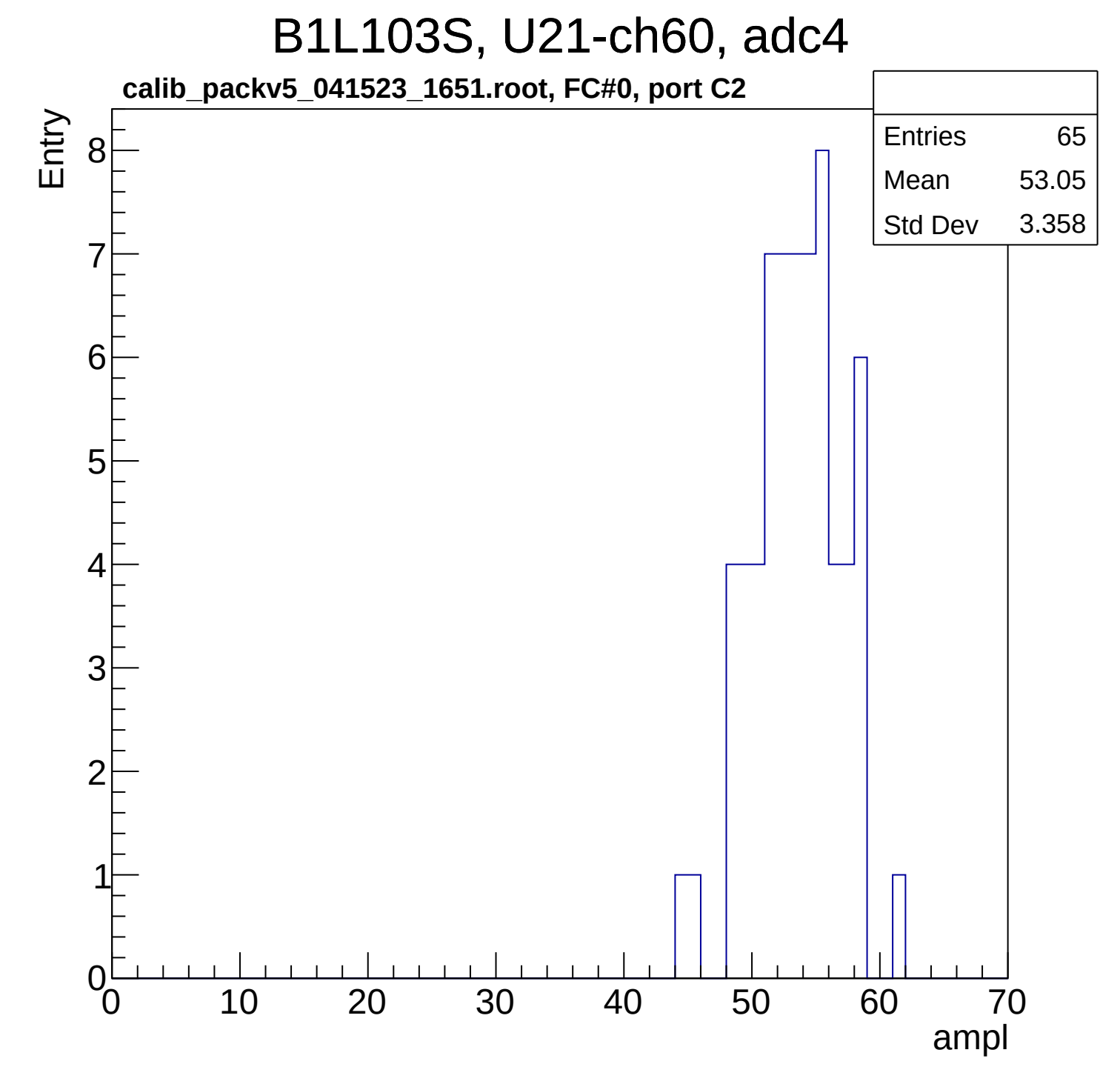
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U21-ch60, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 53.05
Std Dev 3.358
Entry
ampl
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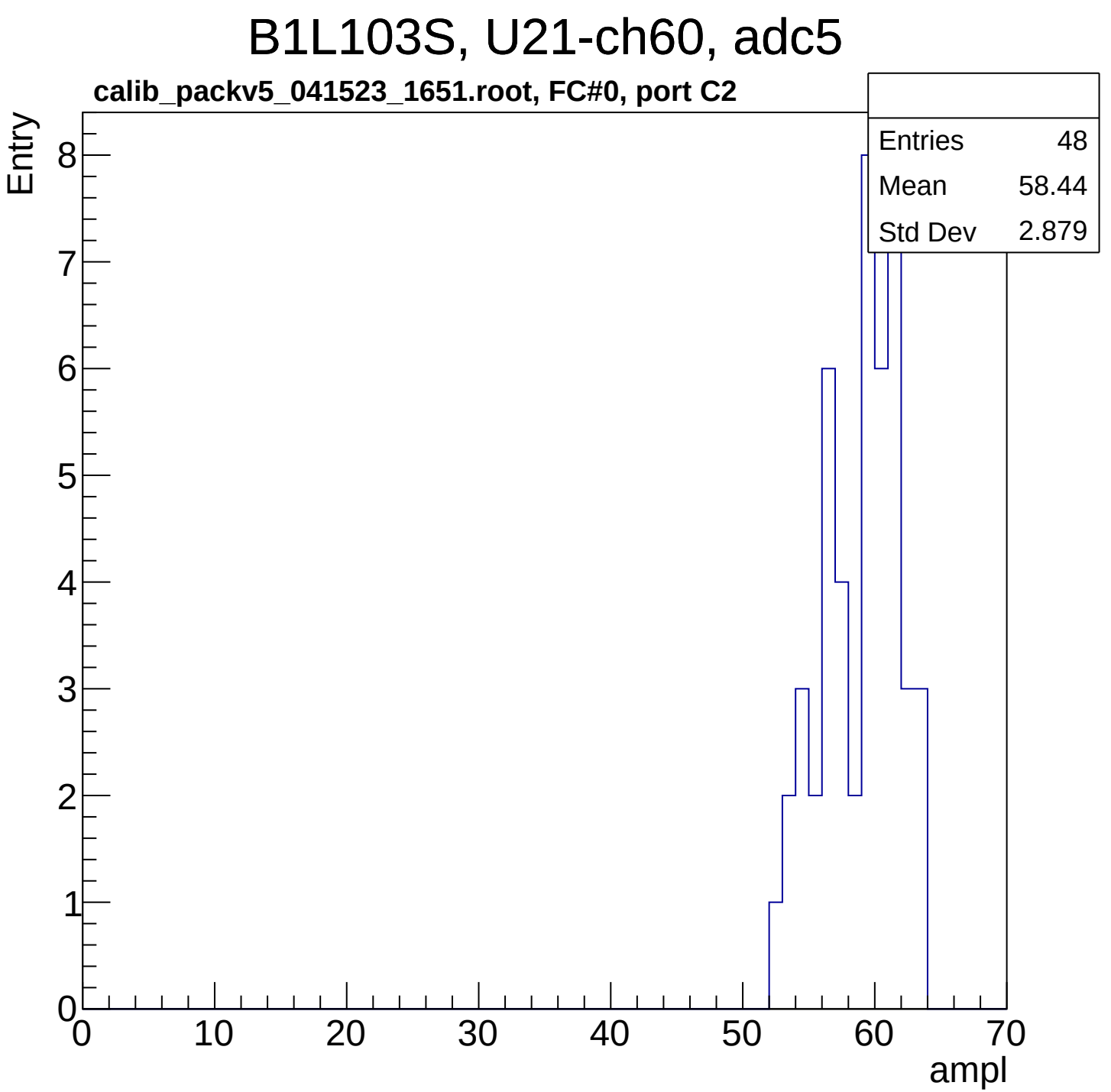
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch60, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 58.44
Std Dev 2.879
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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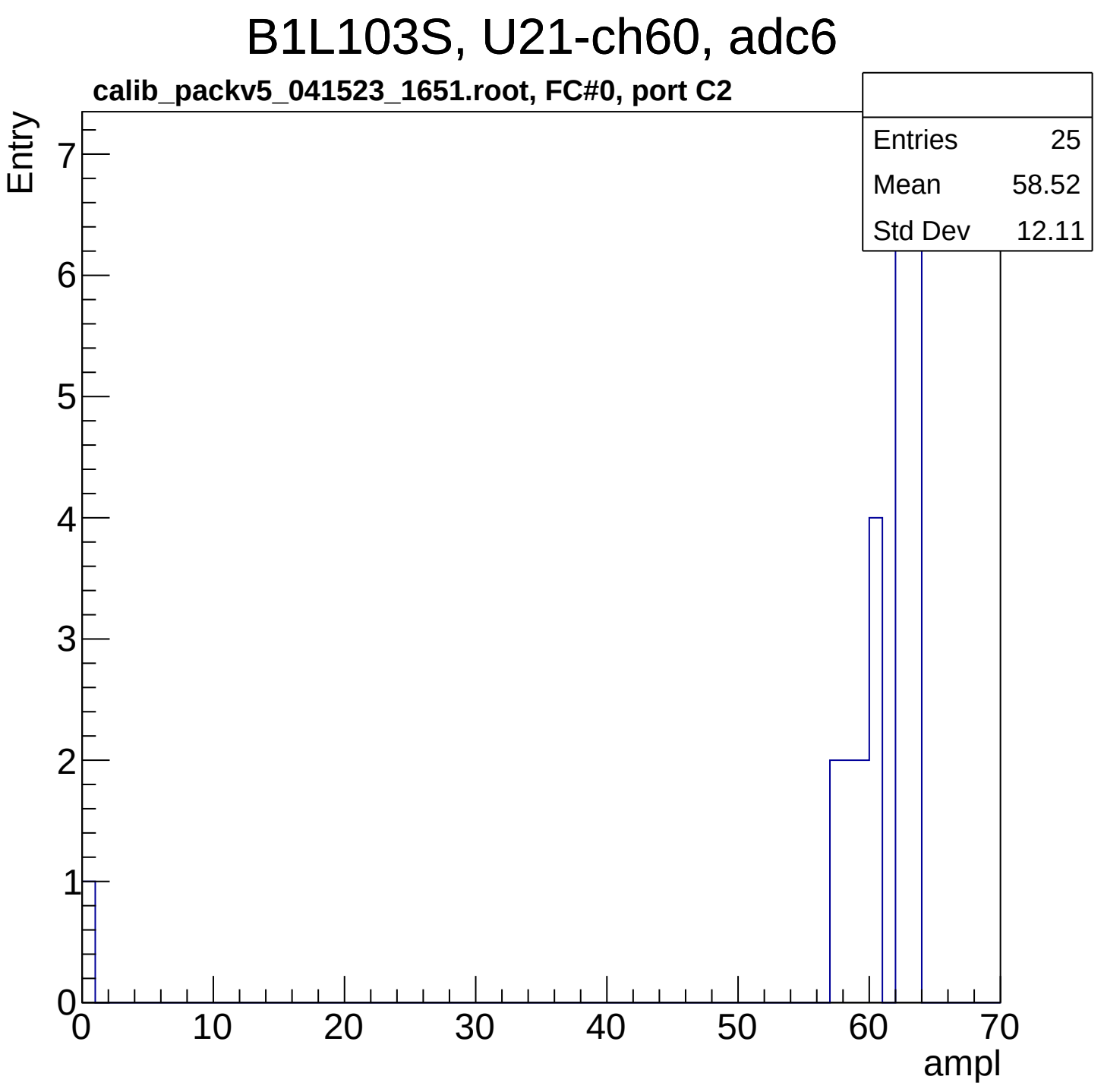
40
50
60
70


B1L103S, U21-ch60, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 58.52
Std Dev 12.11
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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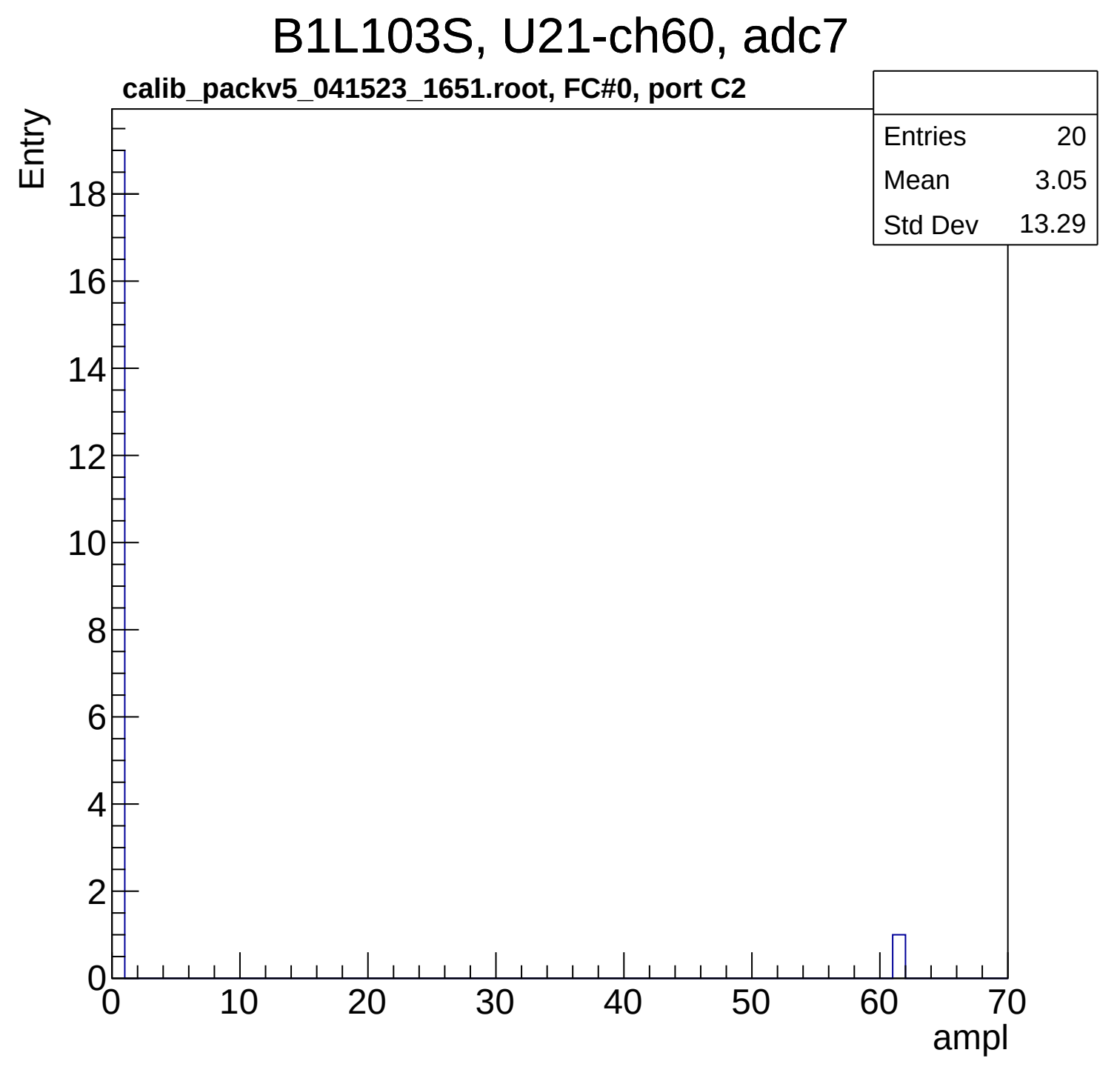
40
50
60
70


B1L103S, U21-ch60, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.05
Std Dev 13.29
Entry
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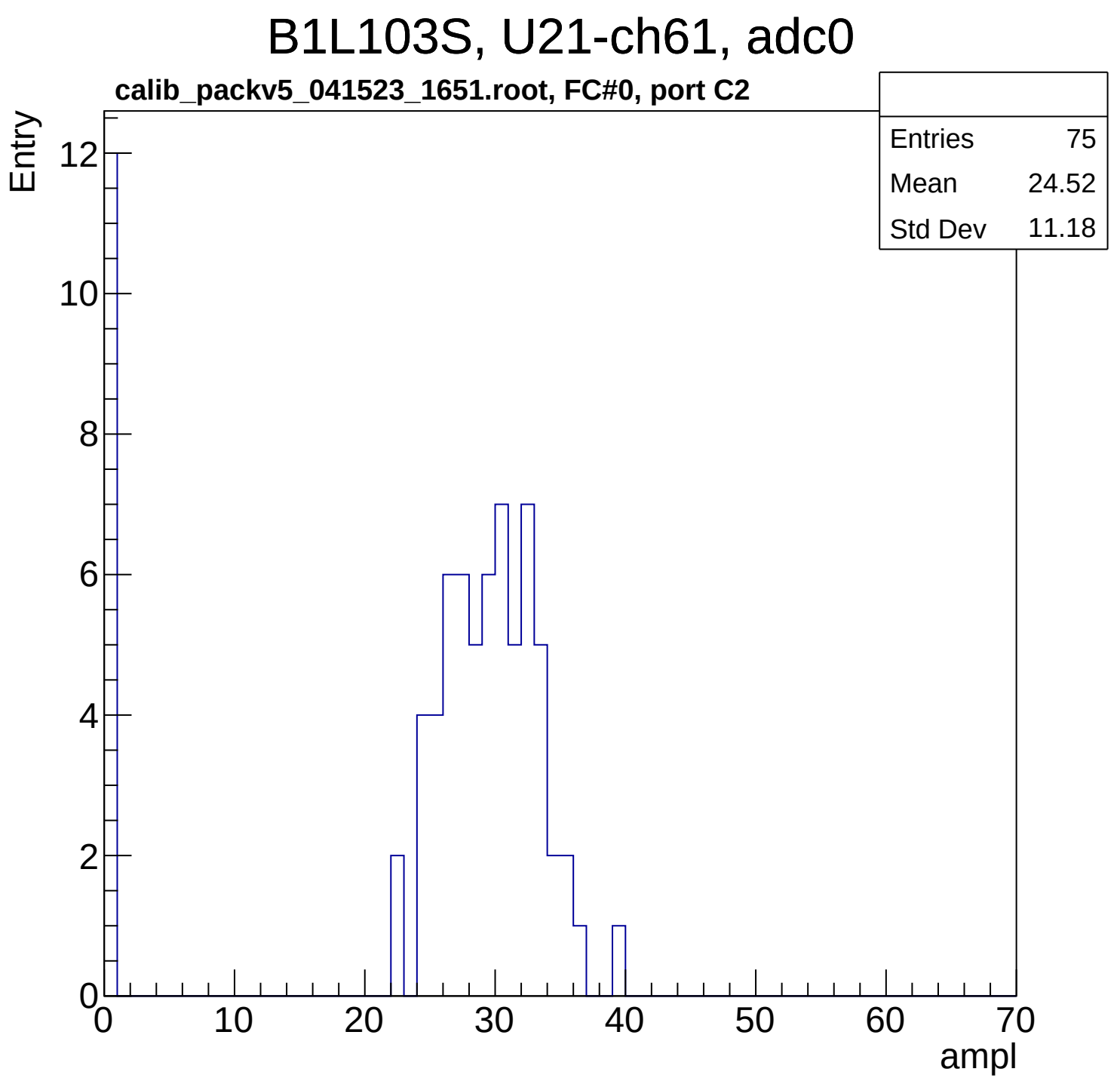
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch61, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 24.52
Std Dev 11.18
Entry
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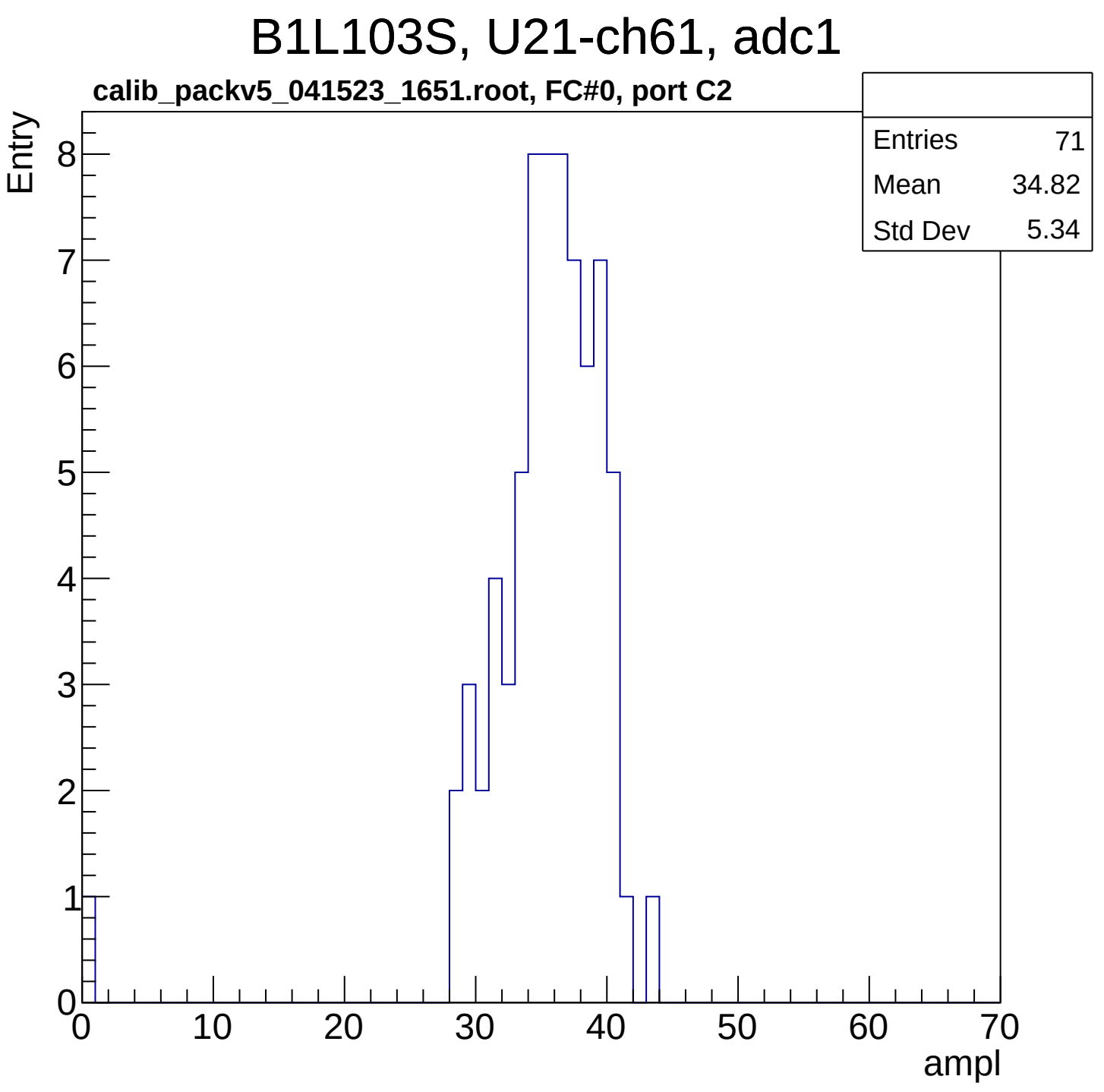
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch61, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 34.82
Std Dev 5.34
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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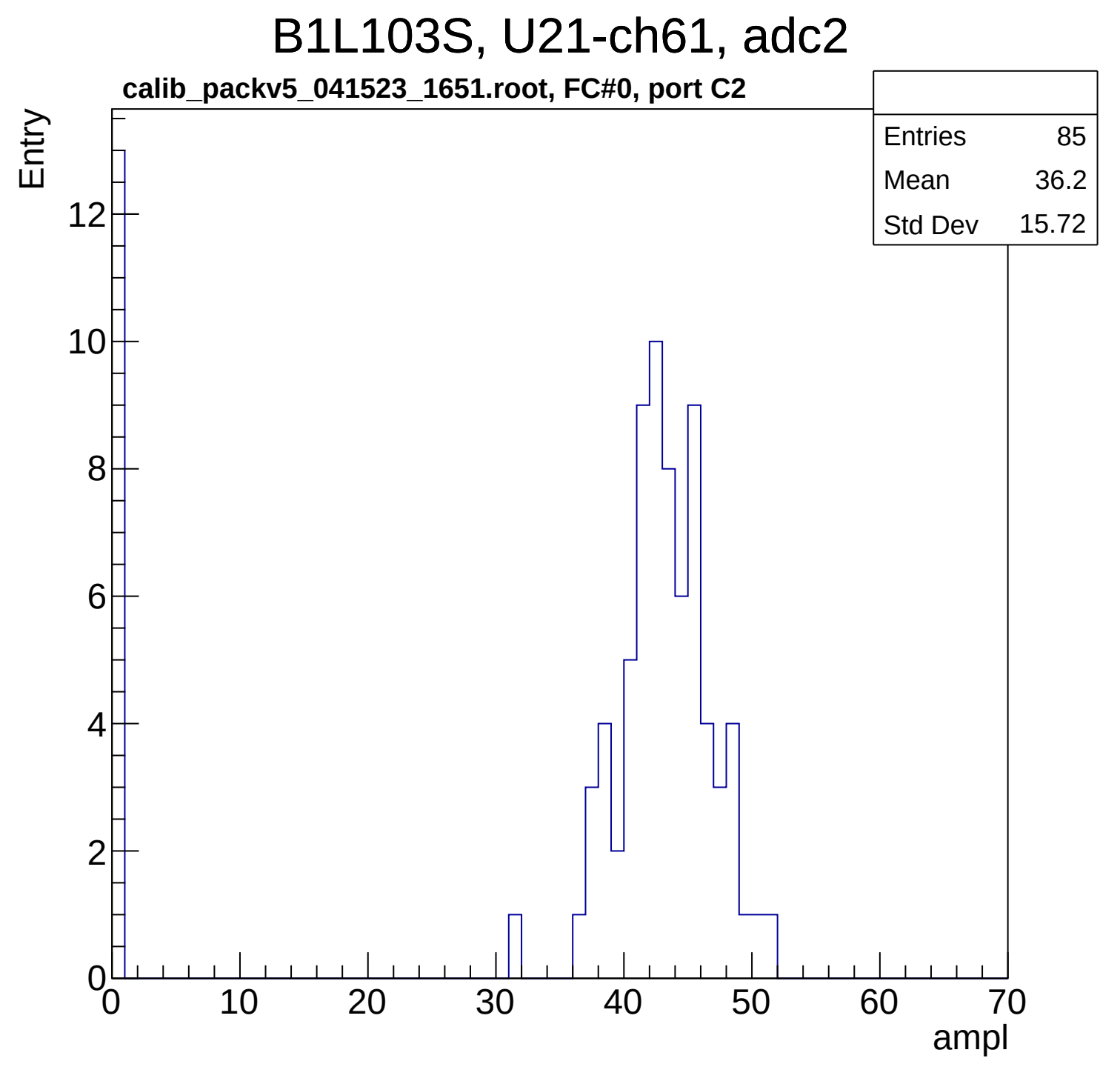
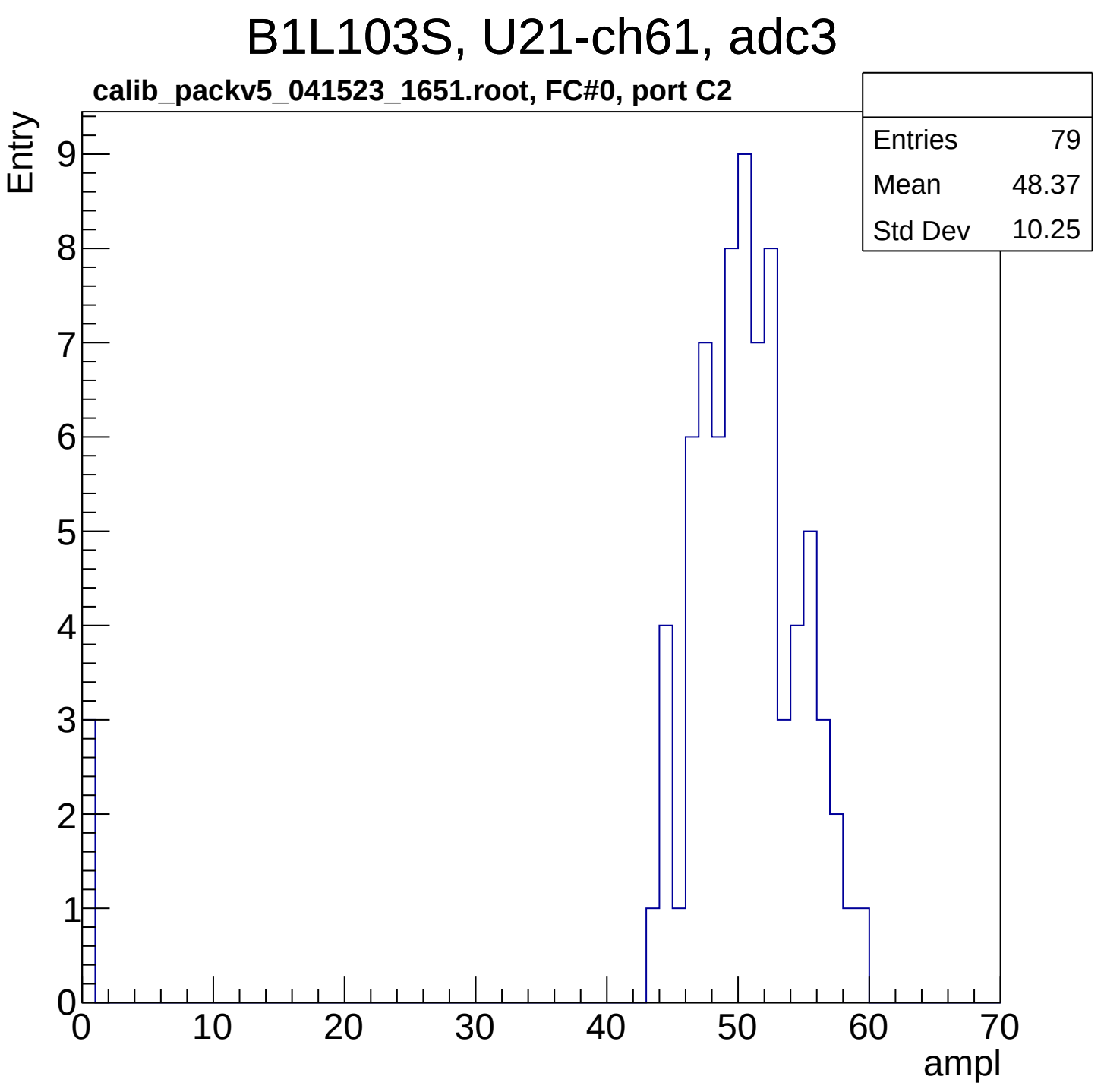

B1L103S, U21-ch61, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 36.2
Std Dev 15.72
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch61, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 48.37
Std Dev 10.25
Entry
ampl
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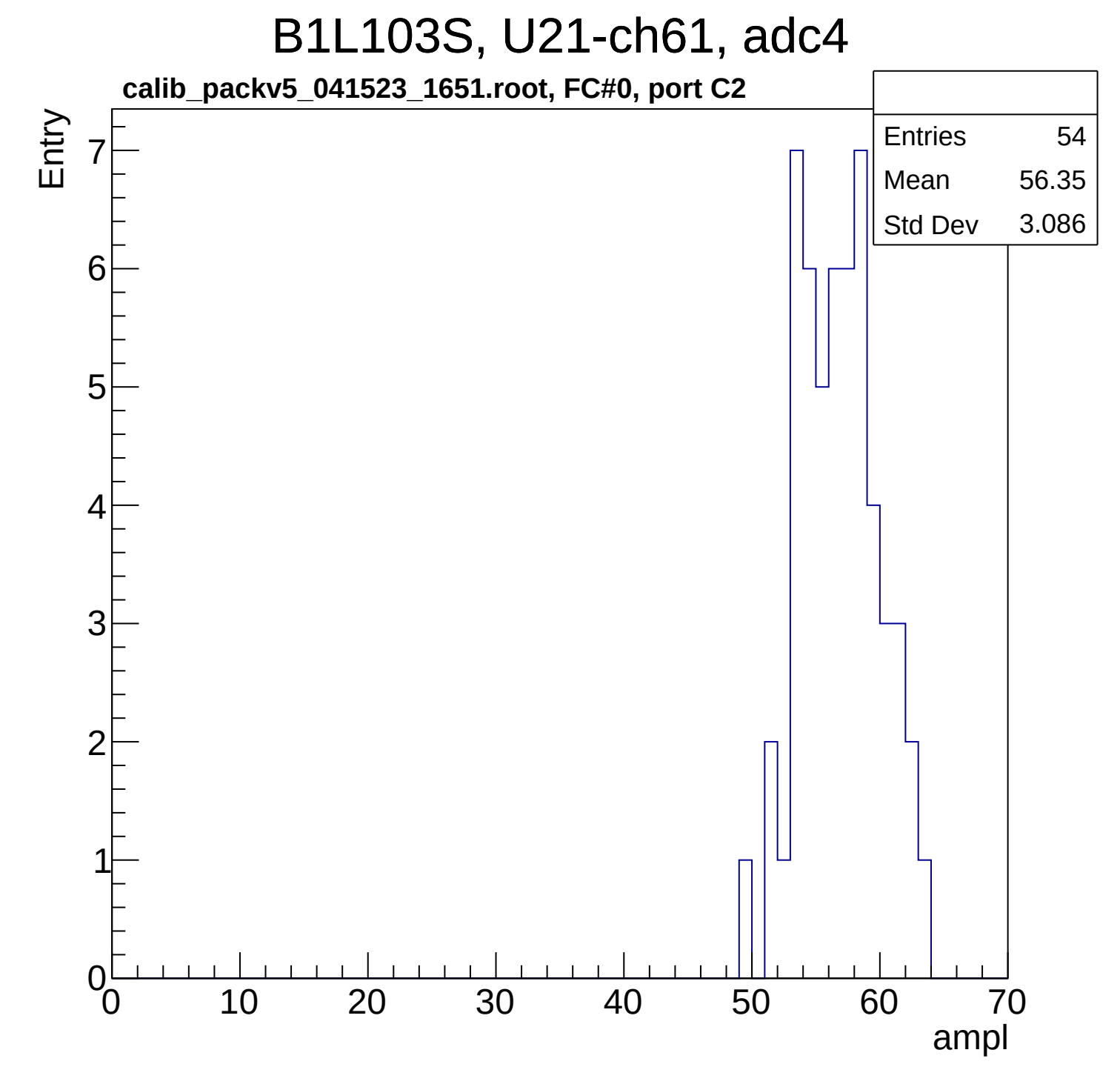
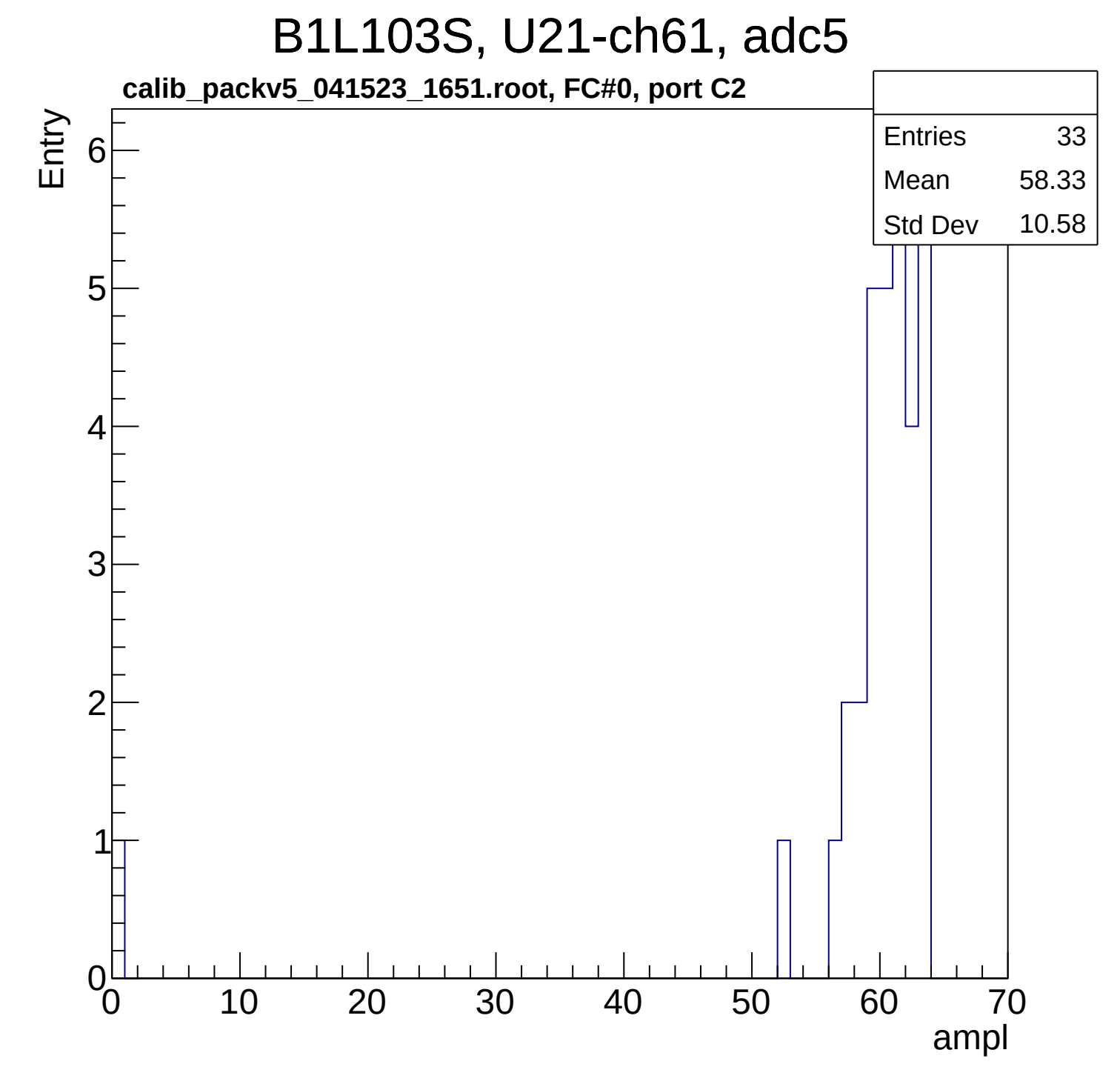
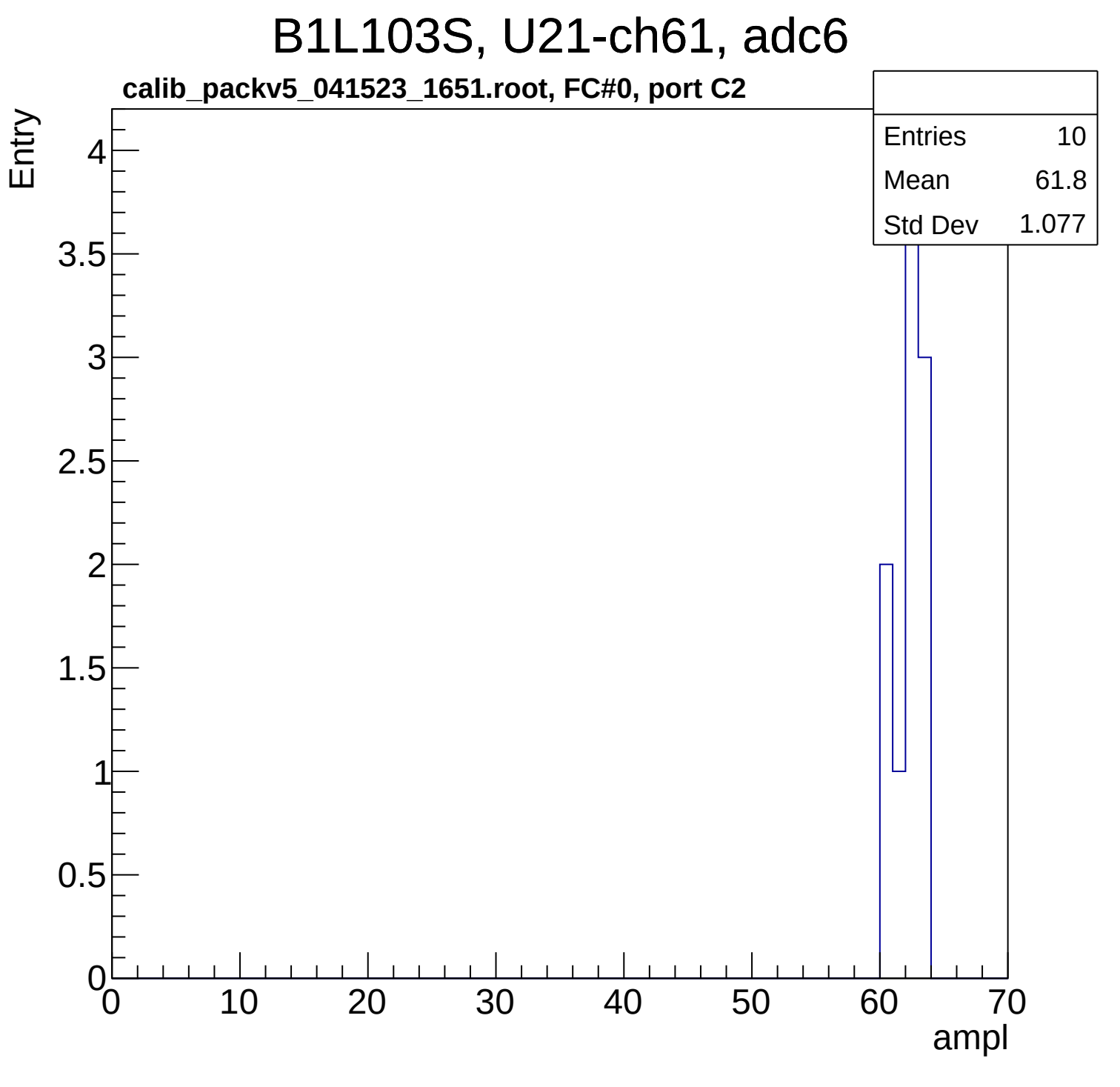
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch61, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 56.35
Std Dev 3.086
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U21-ch61, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 58.33
Std Dev 10.58
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U21-ch61, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61.8
Std Dev 1.077
Entry
ampl
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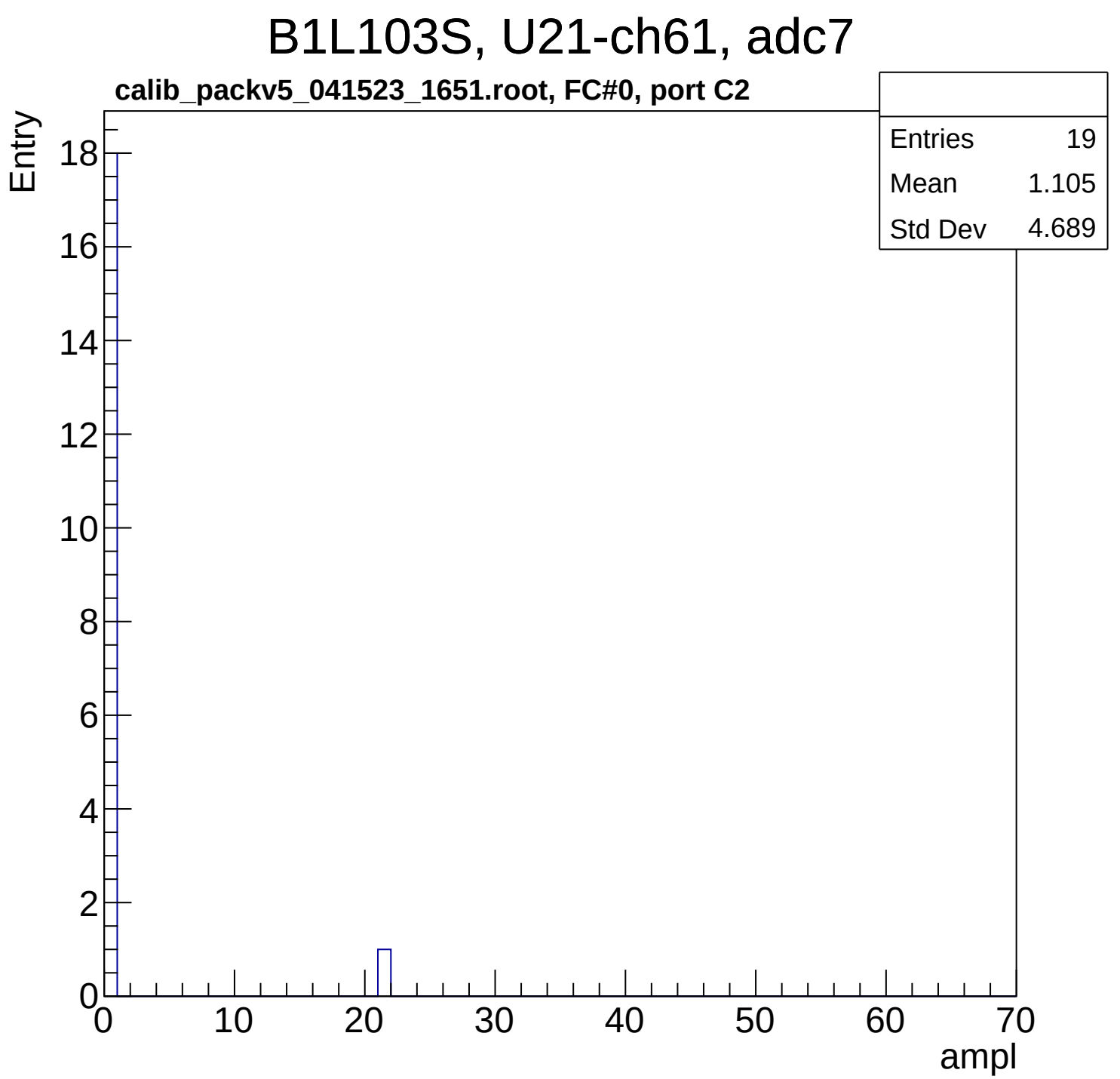
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U21-ch61, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.105
Std Dev 4.689
Entry
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4
6
8
10
12
14
16
18
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10
20
30
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50
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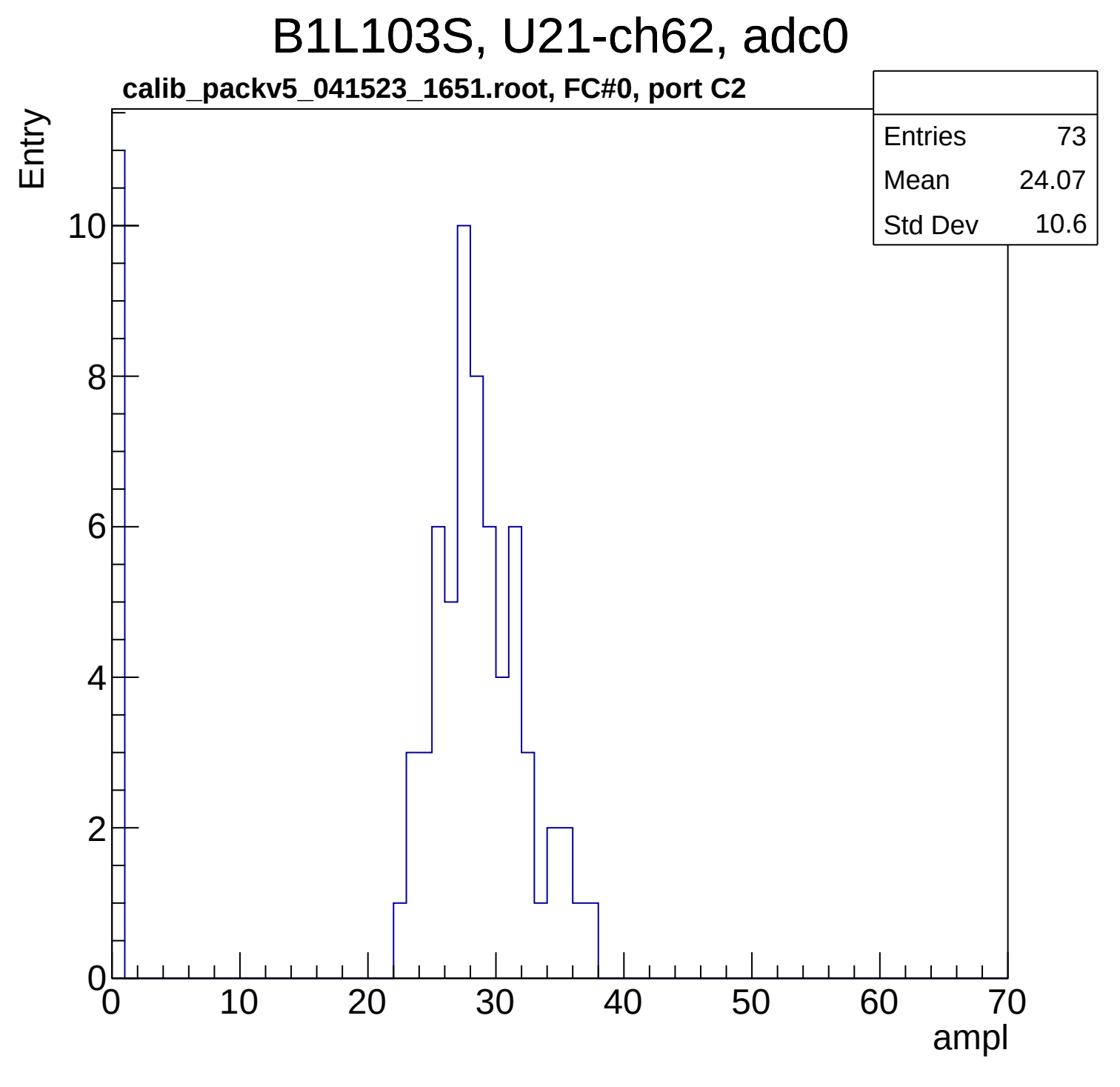
70
ampl


B1L103S, U21-ch62, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 24.07
Std Dev 10.6
Entry
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4
6
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10
0
10
20
30
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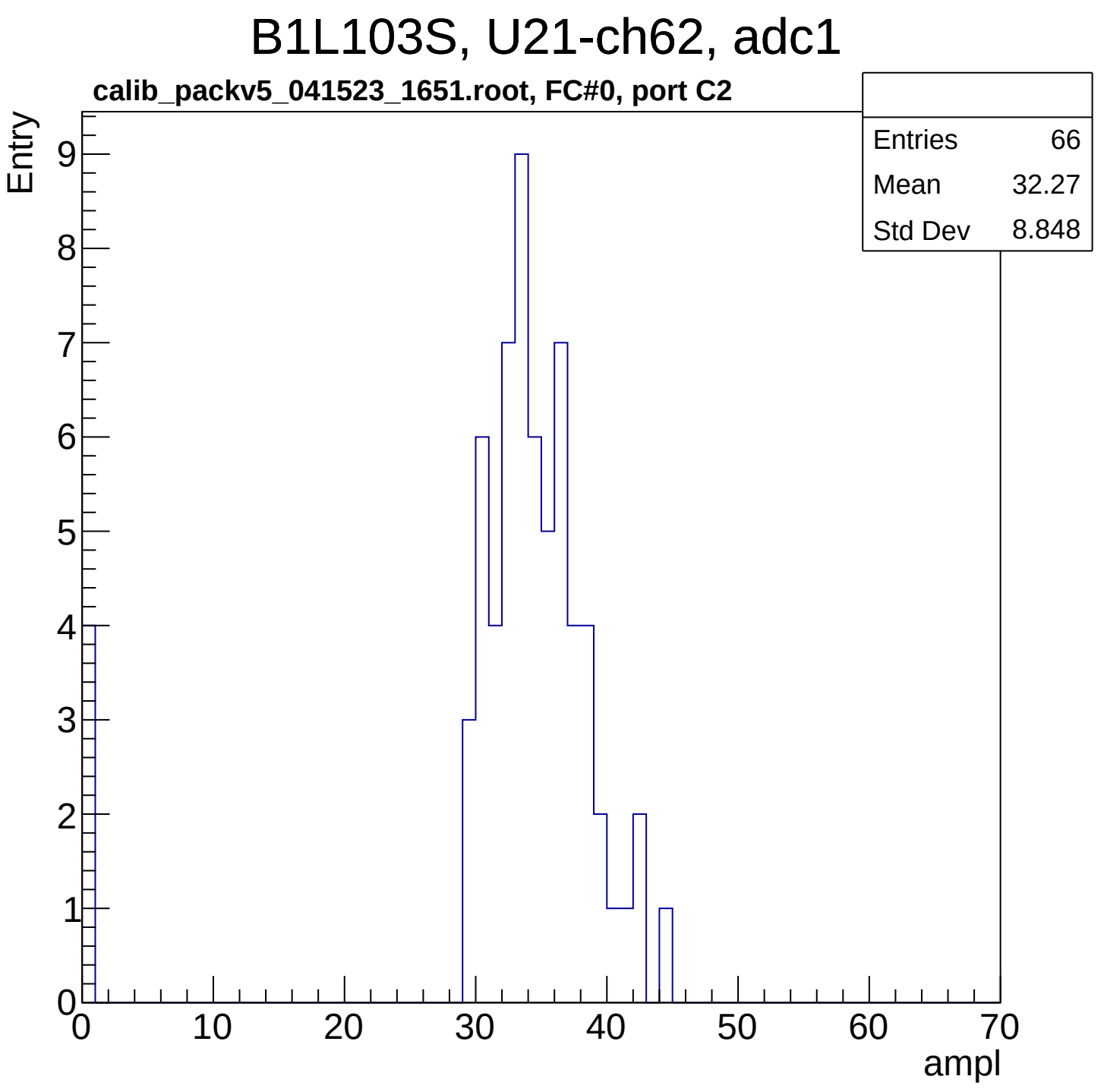
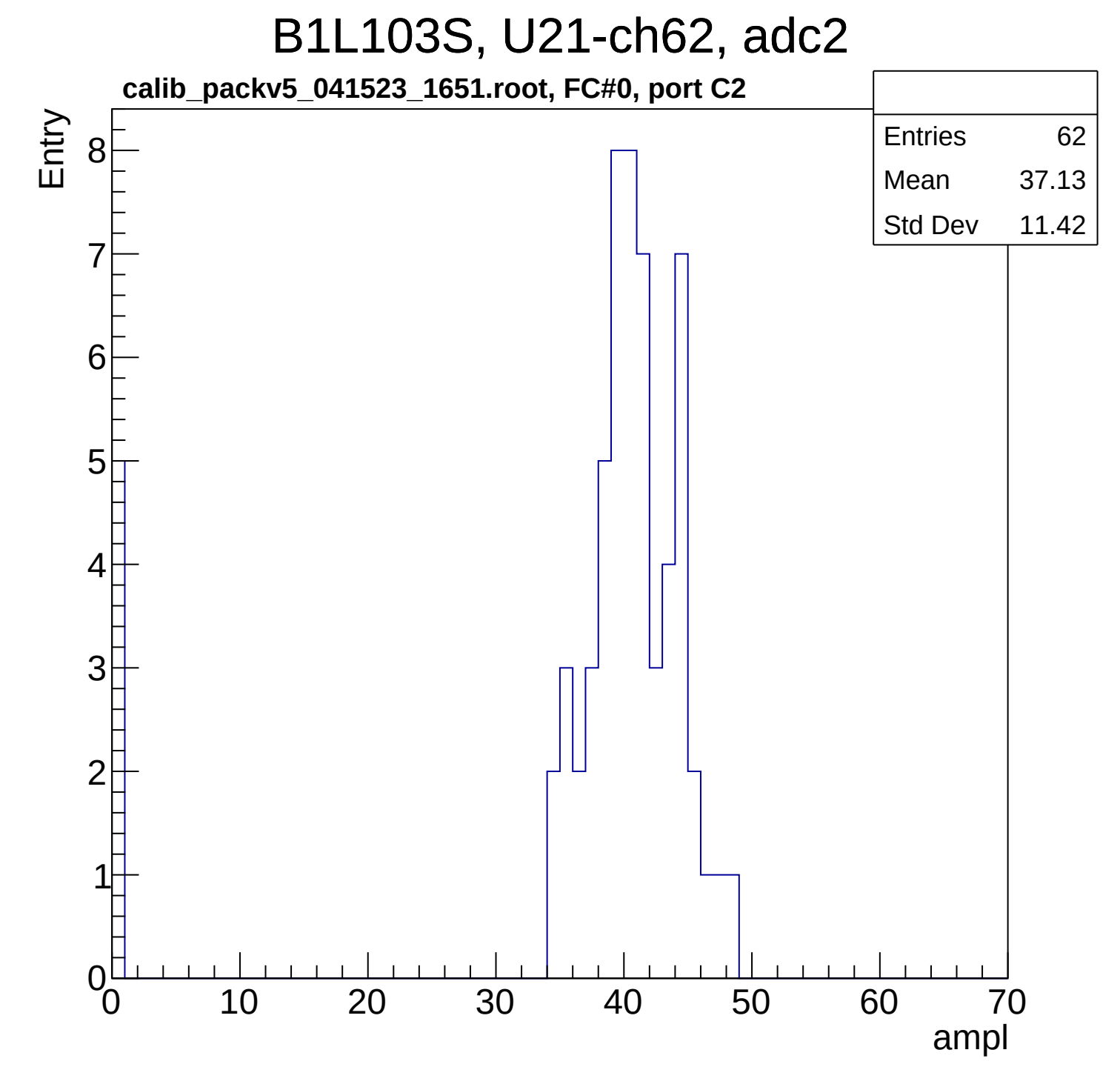
50
60
70
ampl


B1L103S, U21-ch62, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 32.27
Std Dev 8.848
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch62, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 37.13
Std Dev 11.42
Entry
ampl
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3
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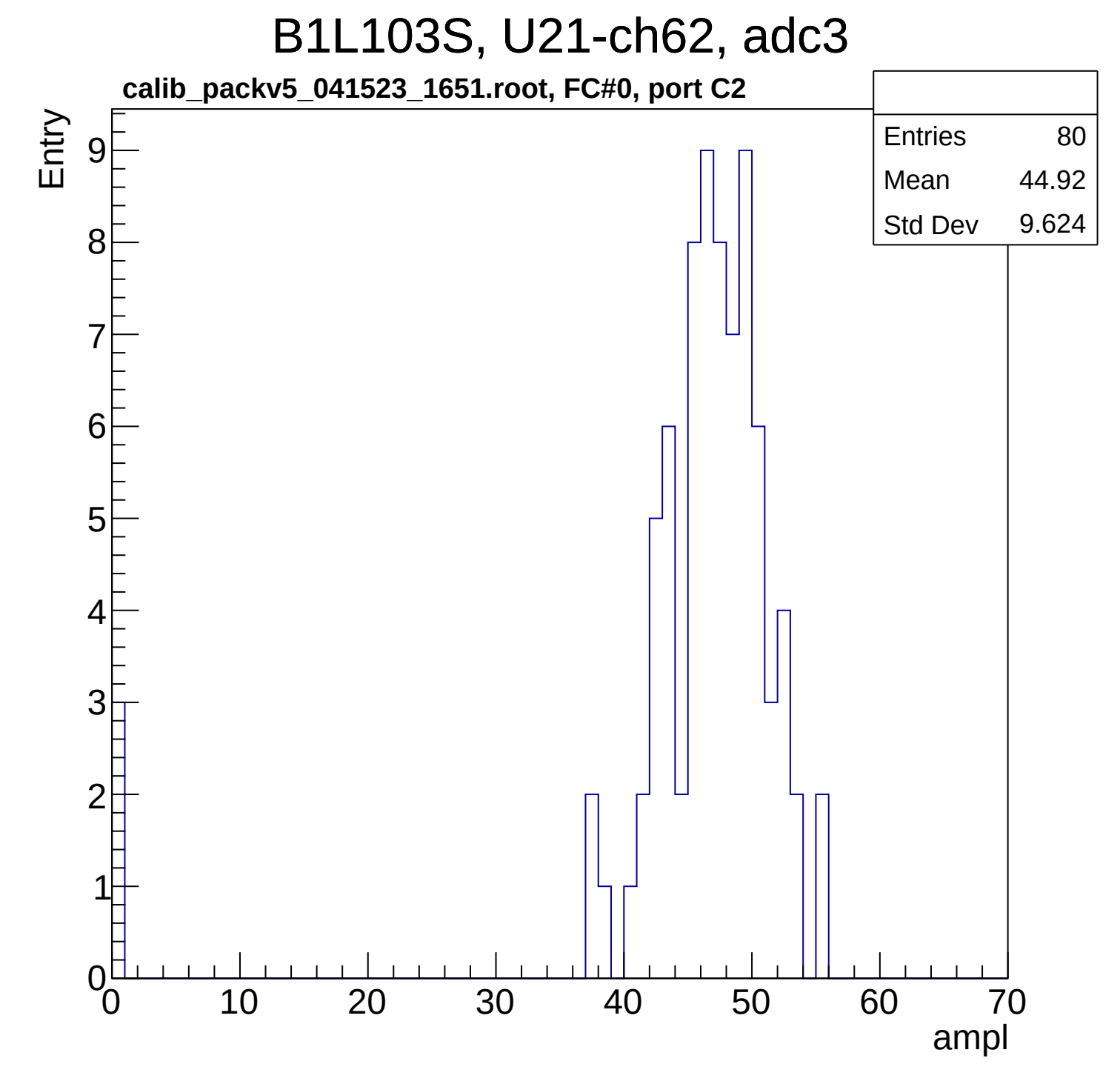
B1L103S, U21-ch62, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 44.92
Std Dev 9.624
Entry
ampl
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0
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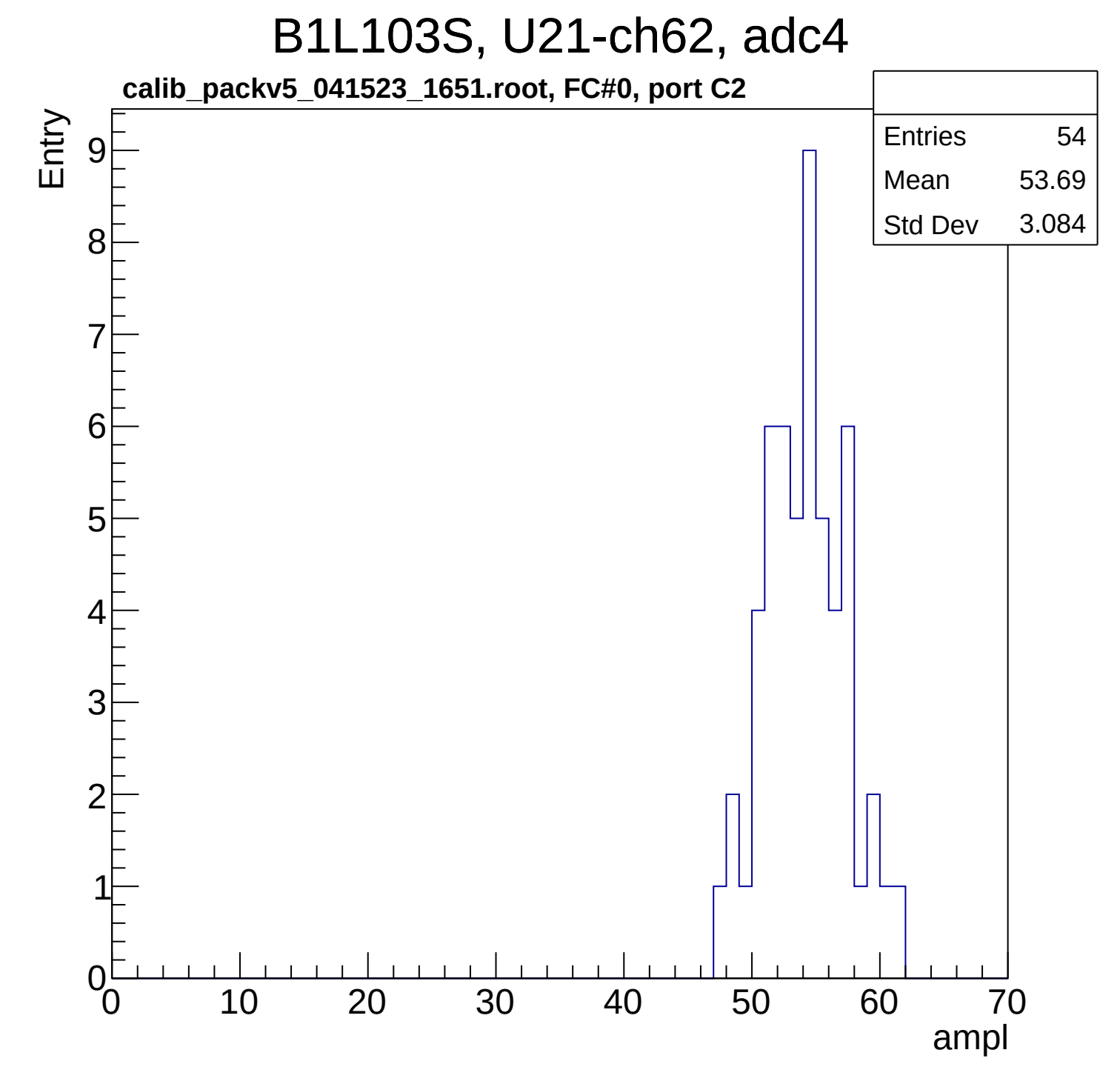
B1L103S, U21-ch62, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 53.69
Std Dev 3.084
Entry
ampl
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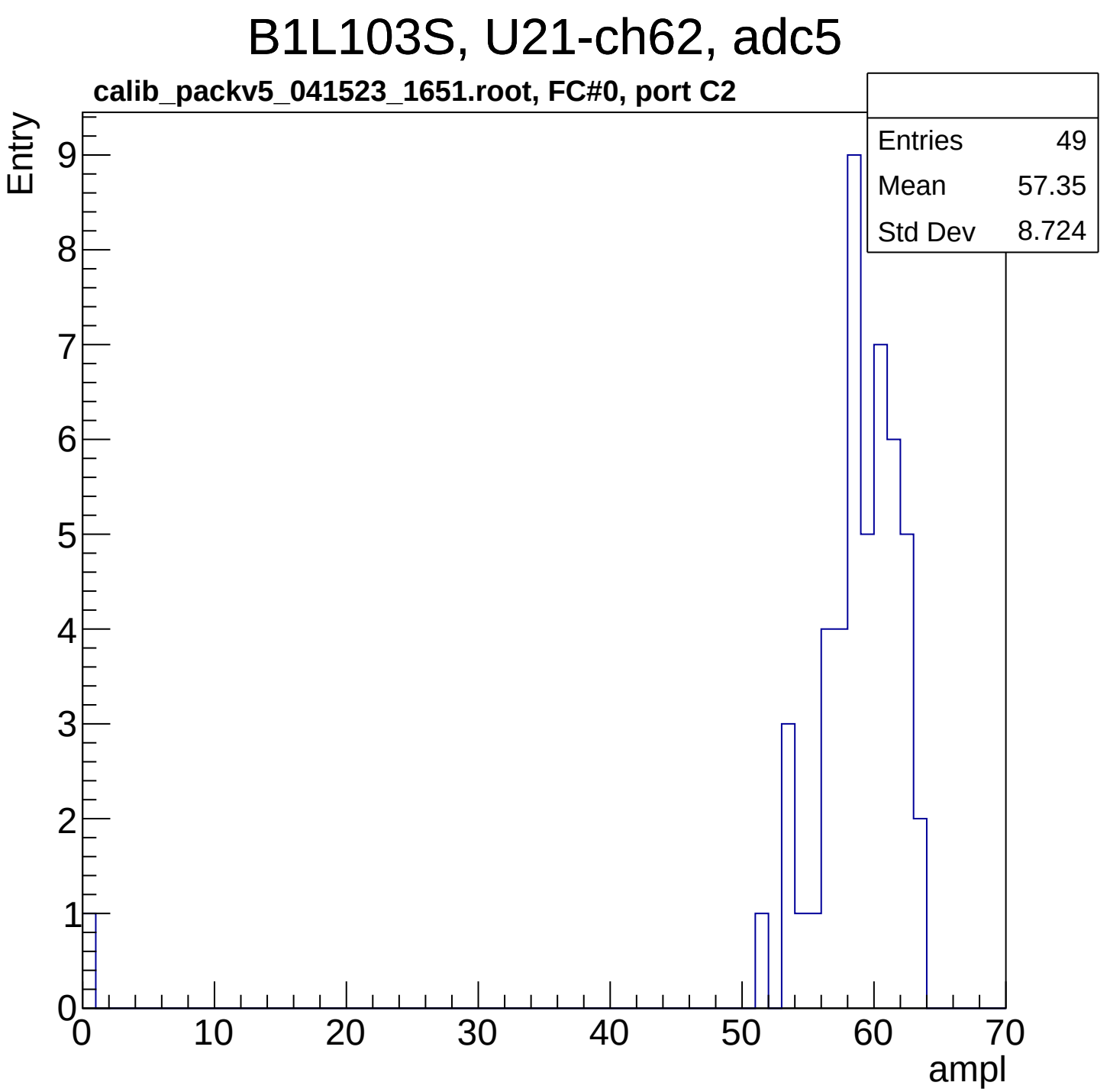
B1L103S, U21-ch62, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 57.35
Std Dev 8.724
Entry
ampl
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3
4
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6
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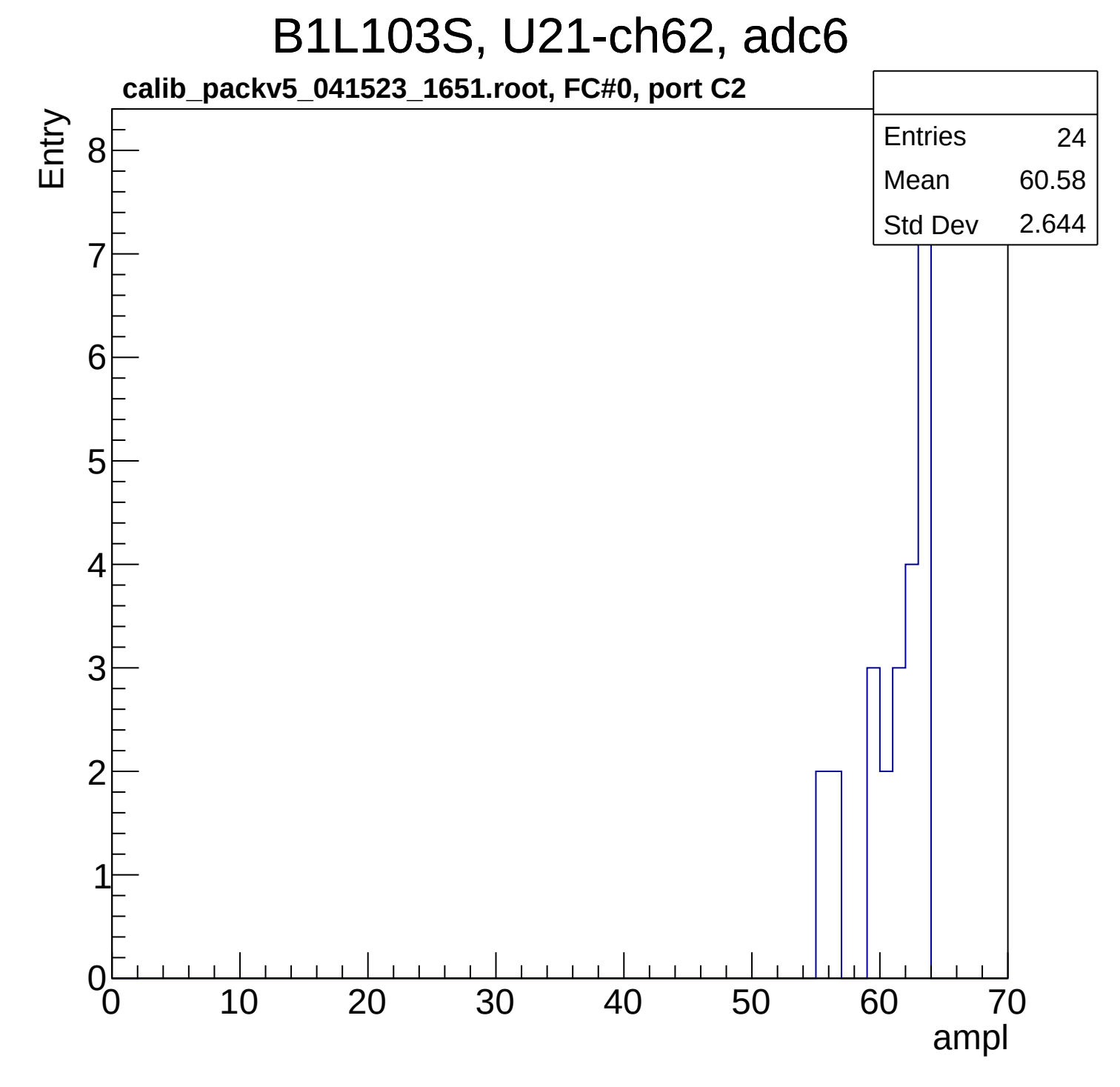
B1L103S, U21-ch62, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 60.58
Std Dev 2.644
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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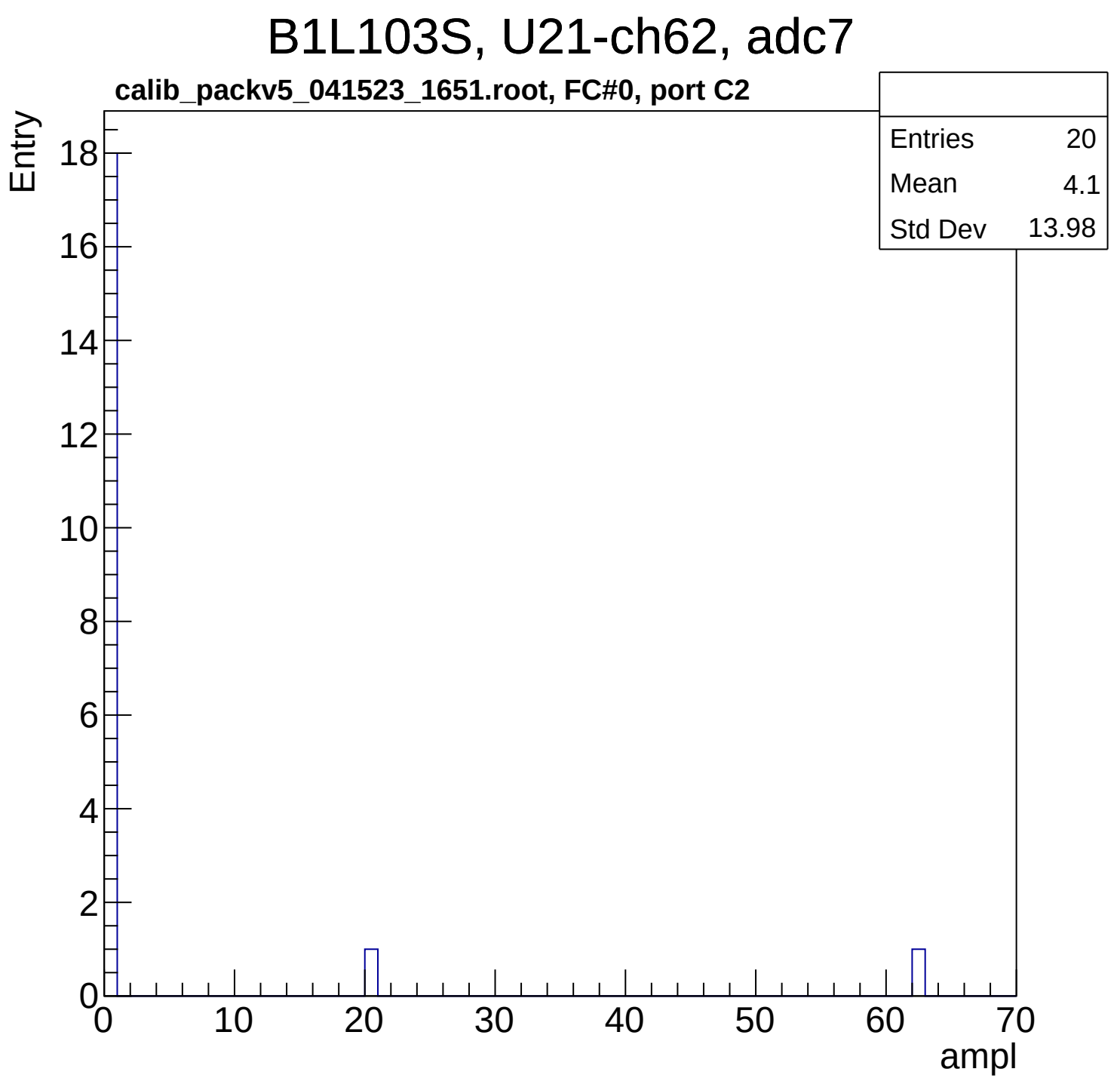
B1L103S, U21-ch62, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4.1
Std Dev 13.98
Entry
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6
8
10
12
14
16
18
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10
20
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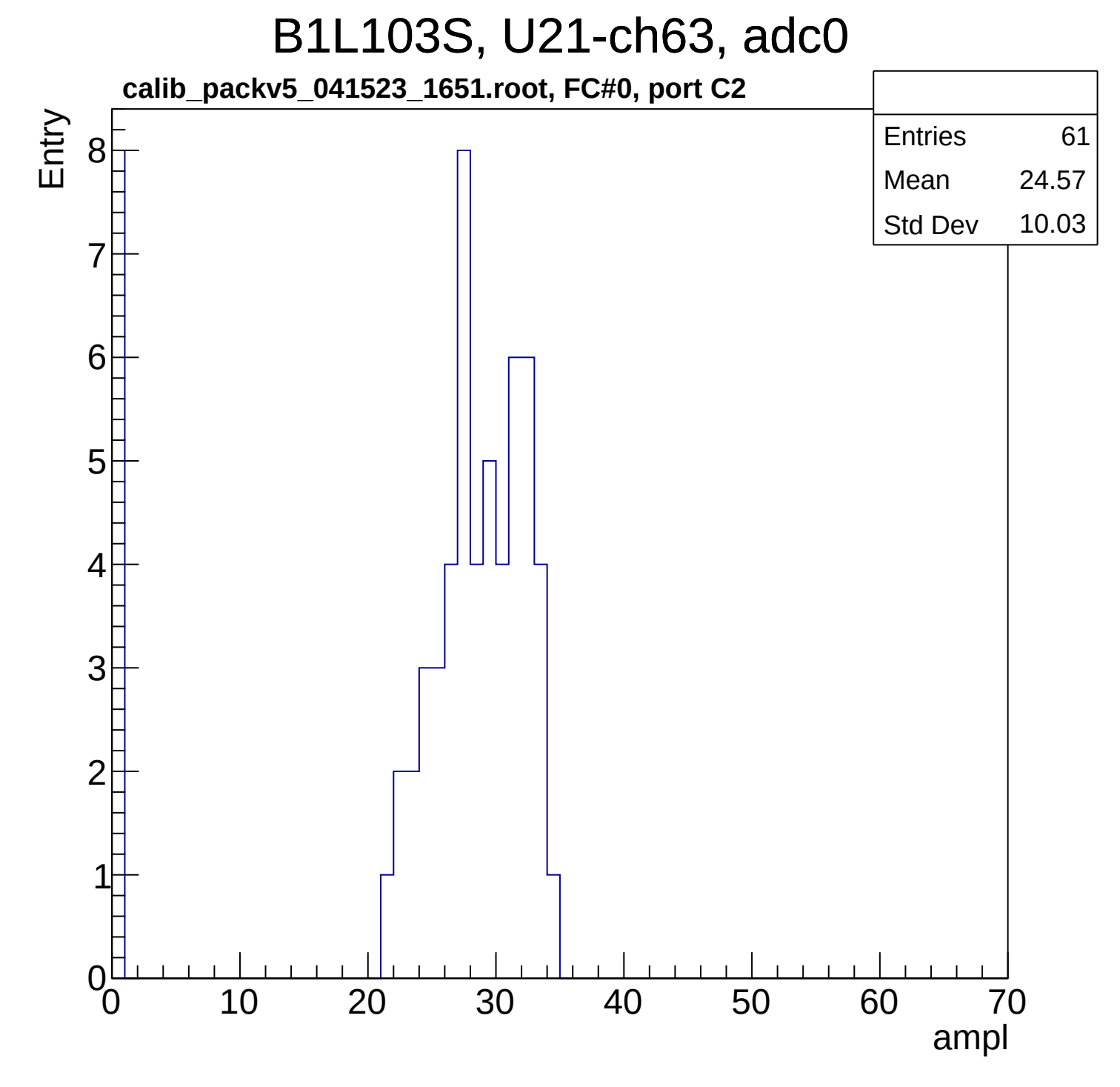
50
60
70
ampl


B1L103S, U21-ch63, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 24.57
Std Dev 10.03
Entry
ampl
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4
5
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7
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0
10
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40
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60
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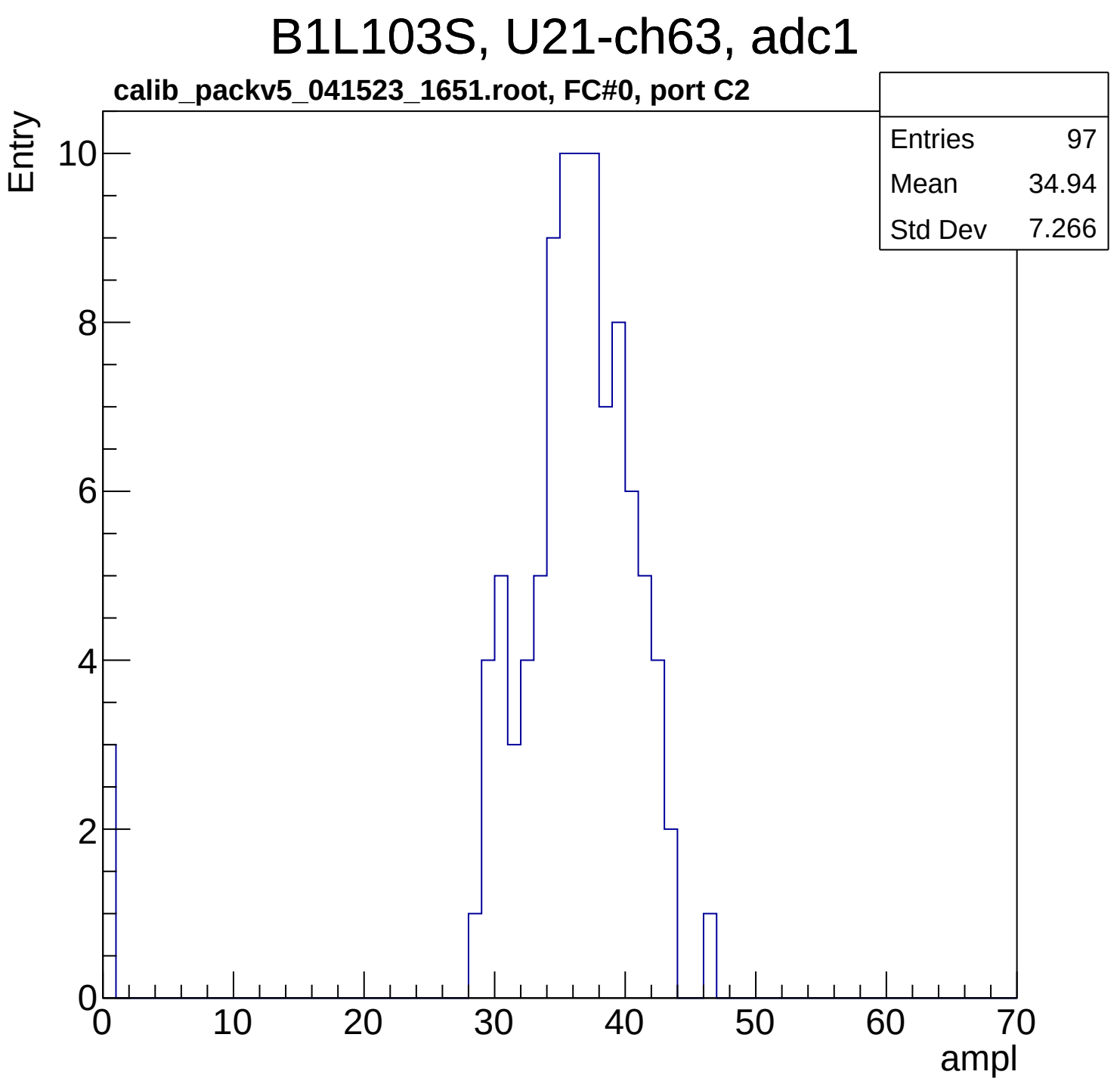
B1L103S, U21-ch63, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 34.94
Std Dev 7.266
Entry
ampl
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4
6
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10
0
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40
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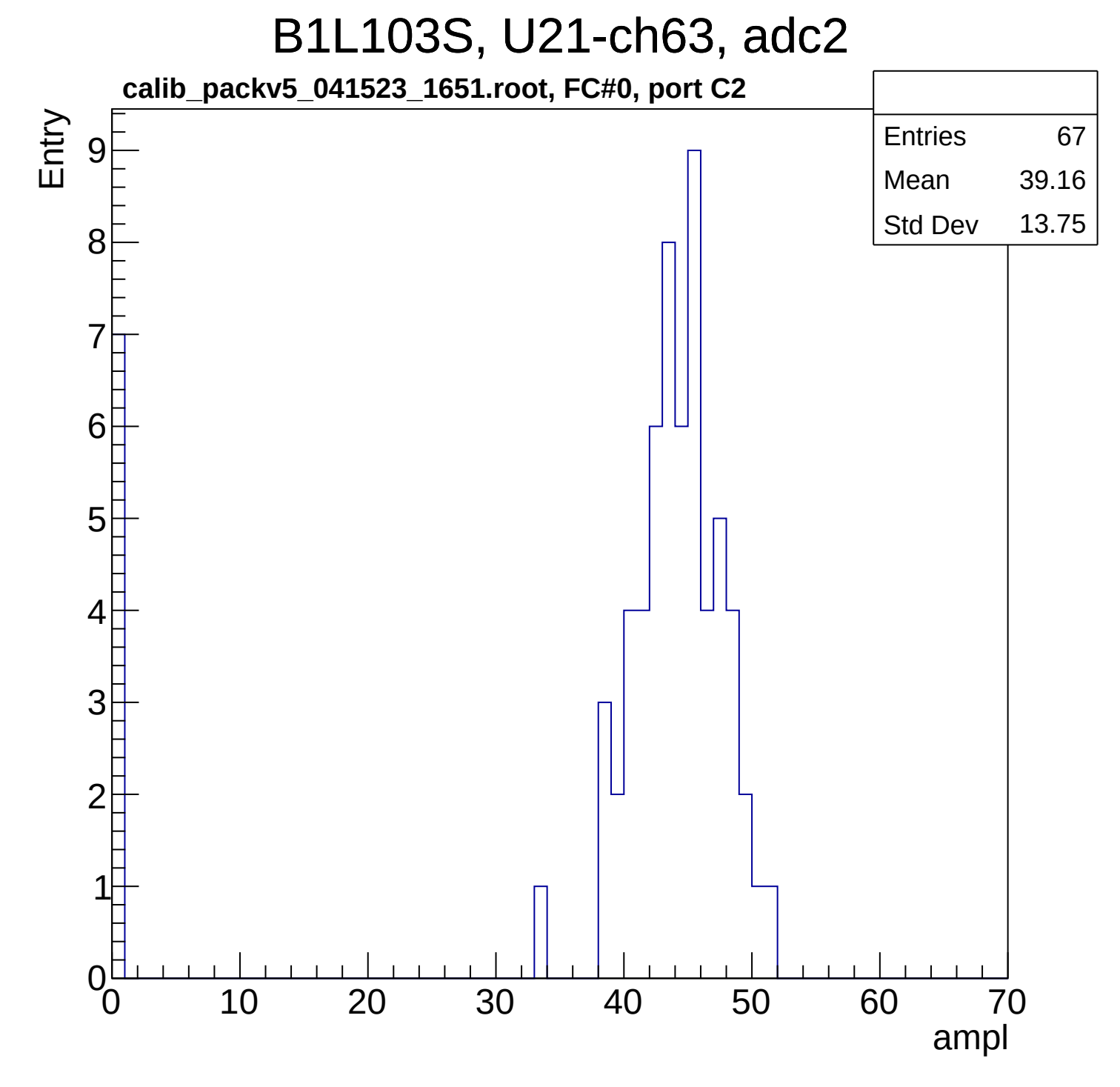
B1L103S, U21-ch63, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 39.16
Std Dev 13.75
Entry
ampl
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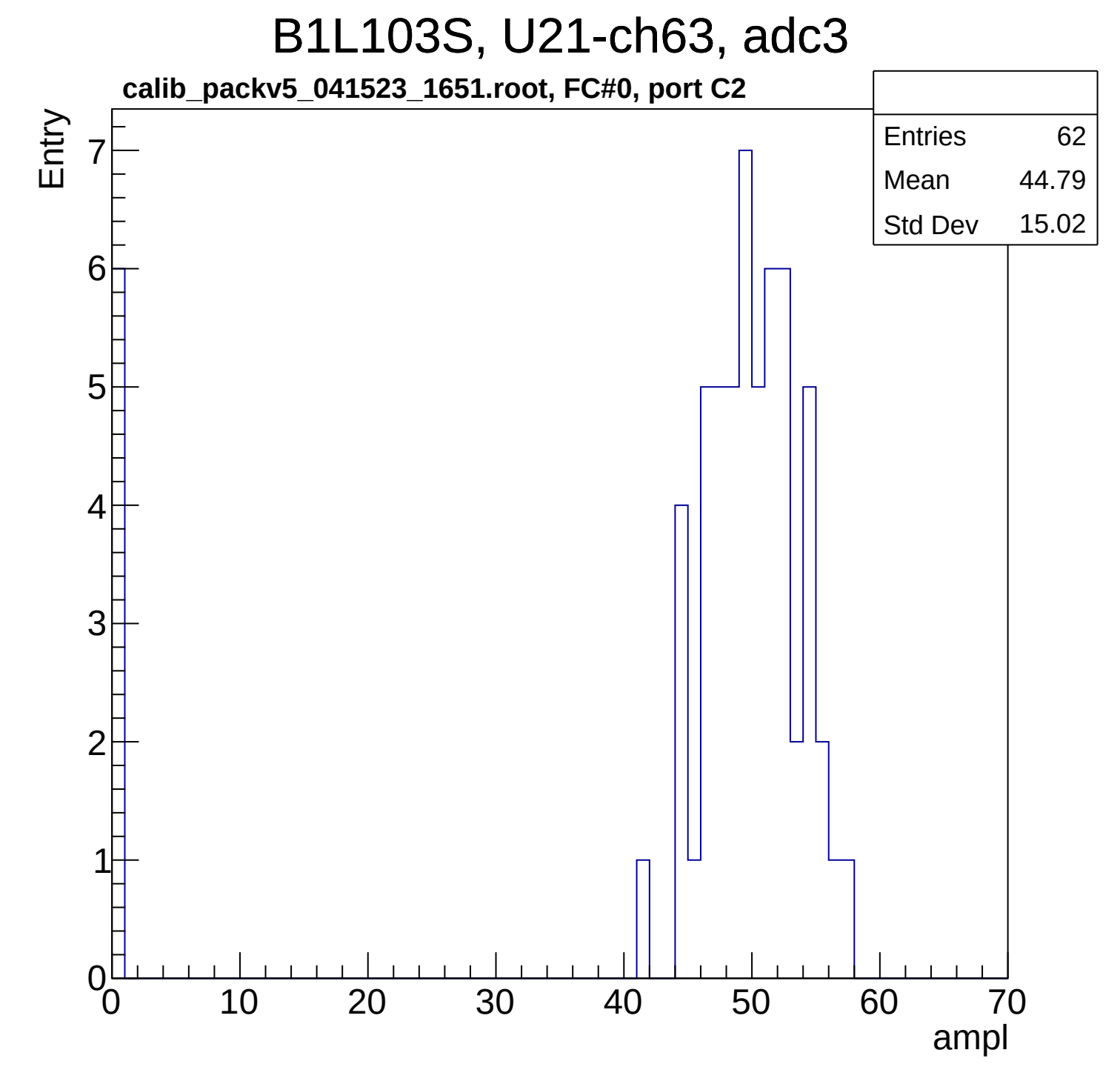
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch63, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 44.79
Std Dev 15.02
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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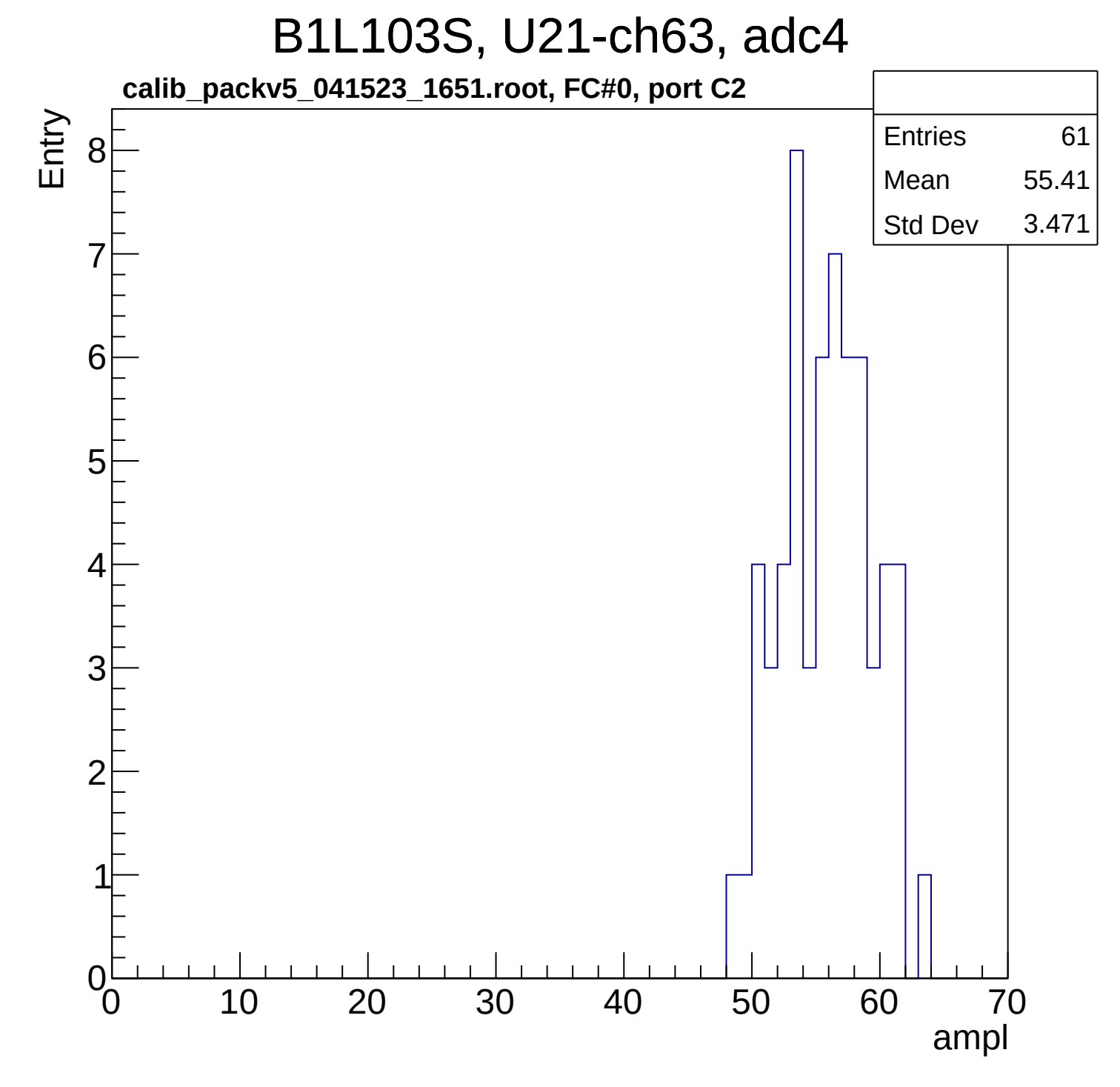
B1L103S, U21-ch63, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 55.41
Std Dev 3.471
Entry
ampl
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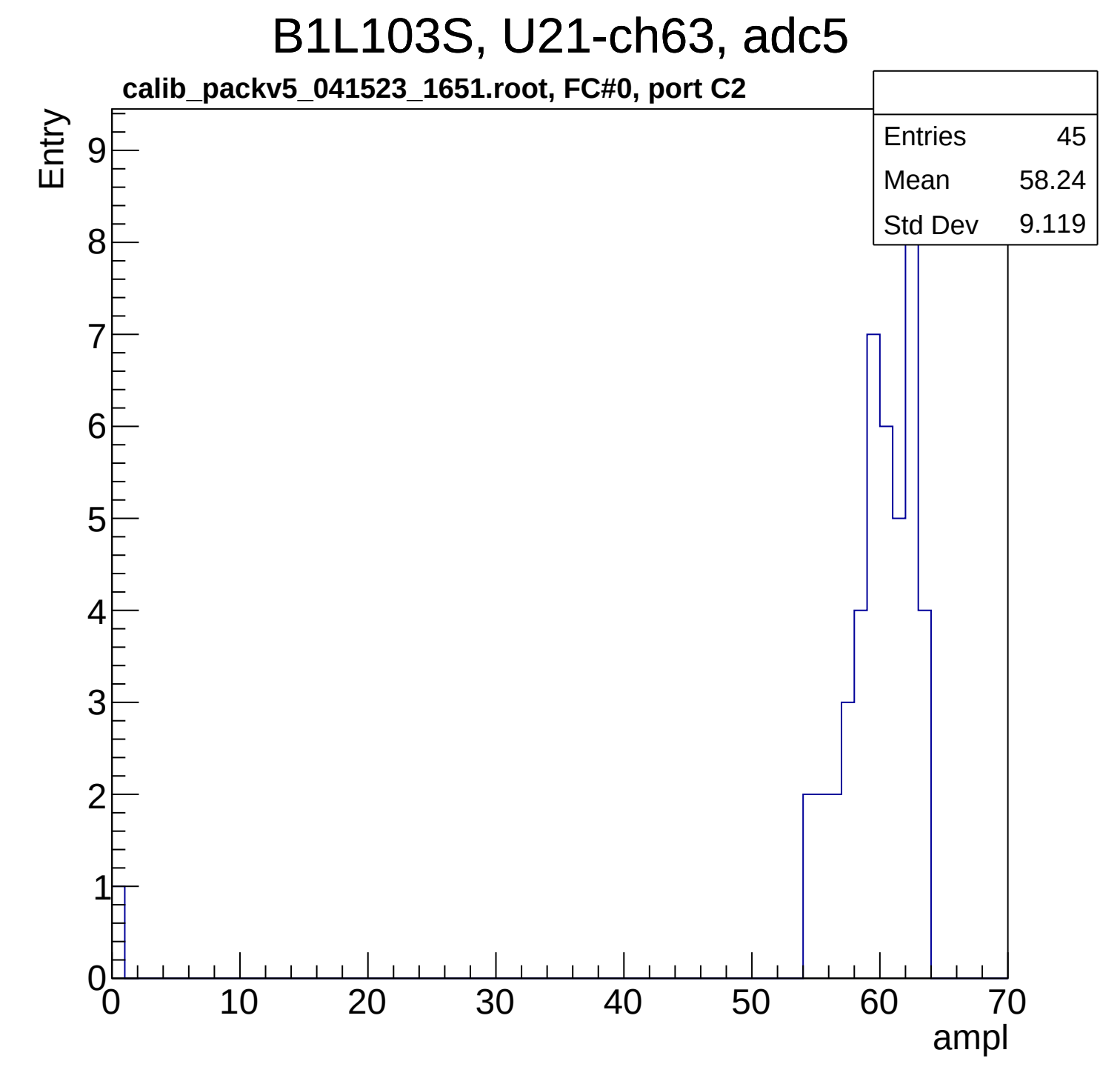
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch63, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 58.24
Std Dev 9.119
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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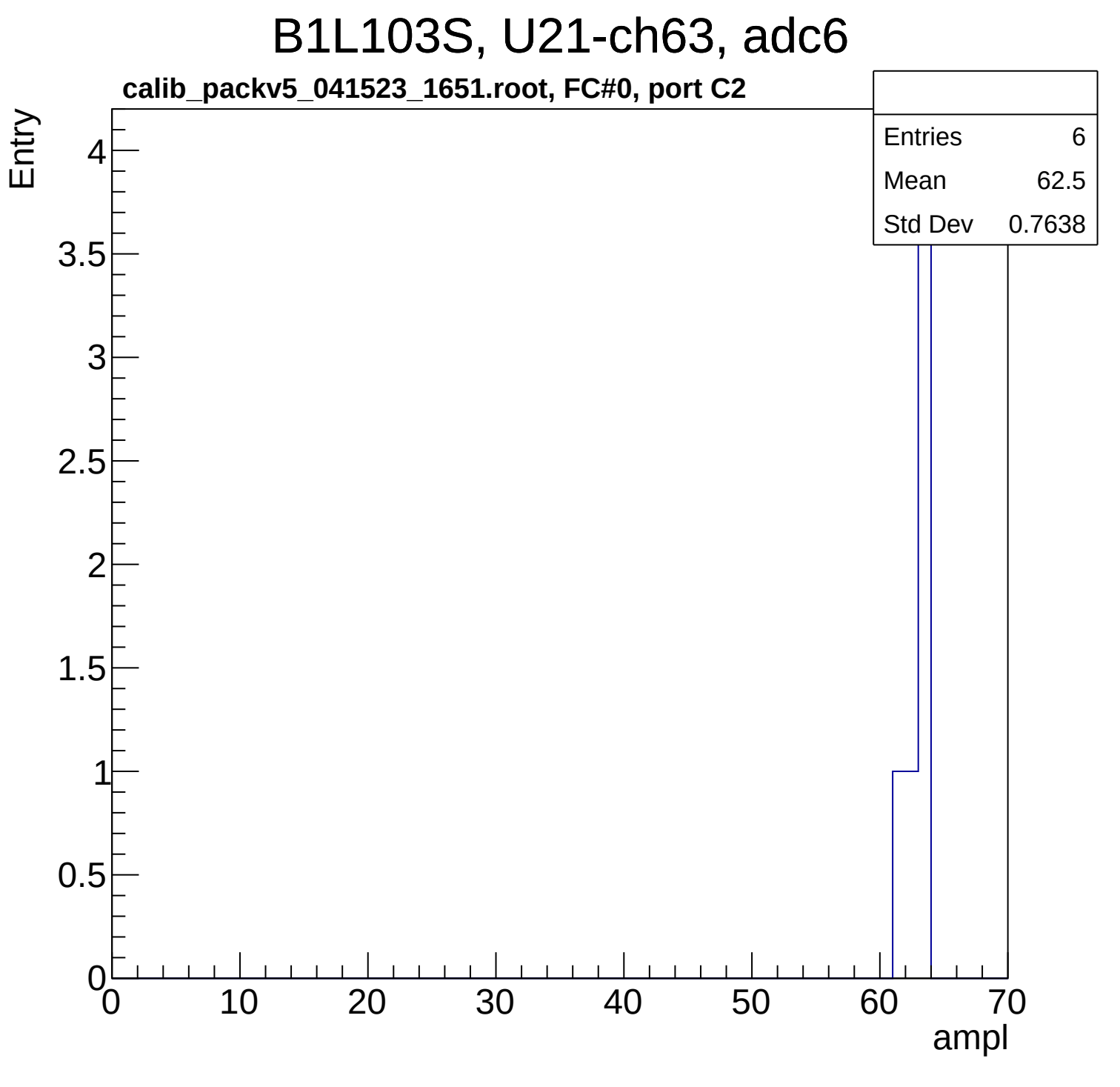
B1L103S, U21-ch63, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 62.5
Std Dev 0.7638
Entry
ampl
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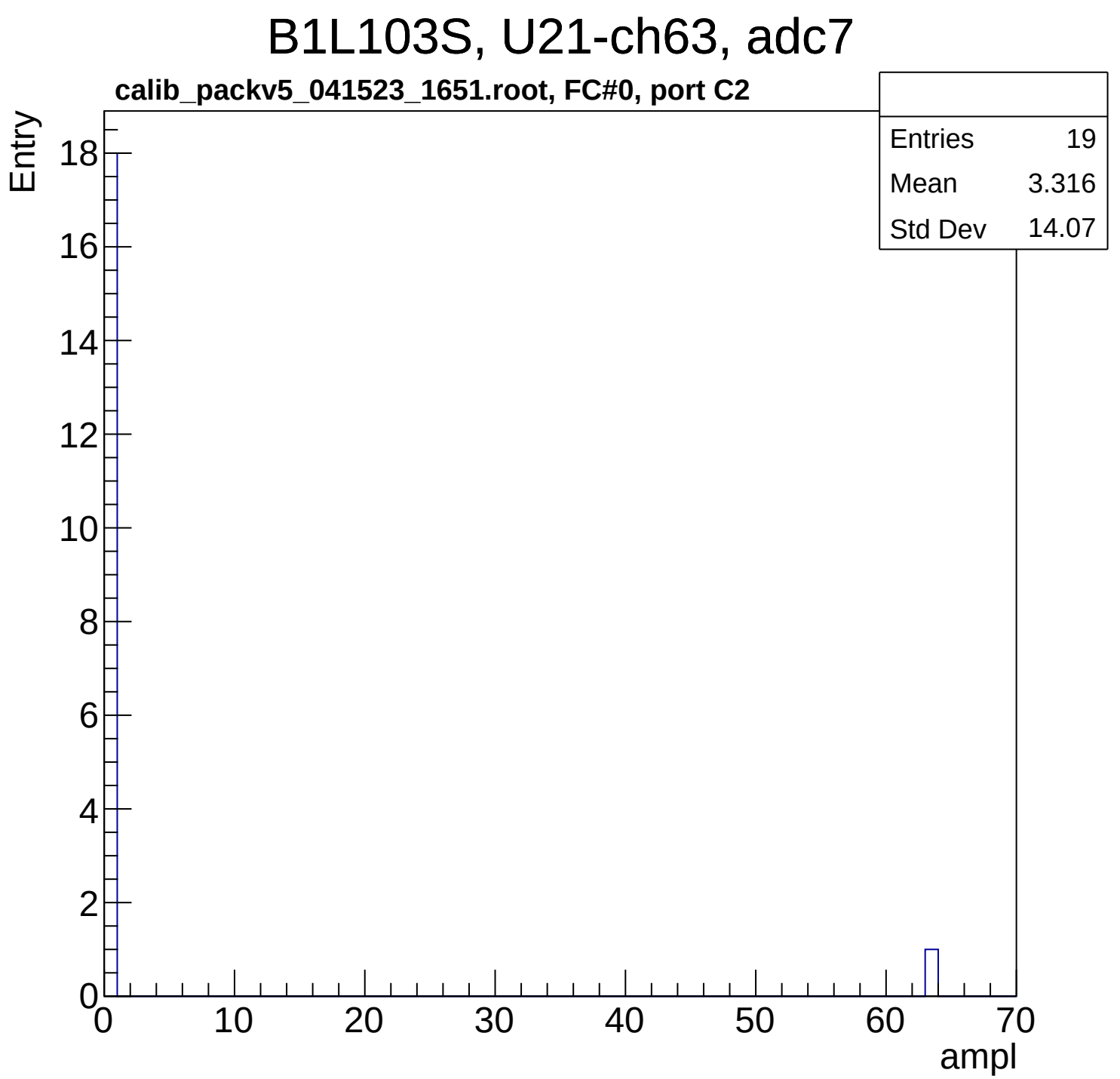
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U21-ch63, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.316
Std Dev 14.07
Entry
0
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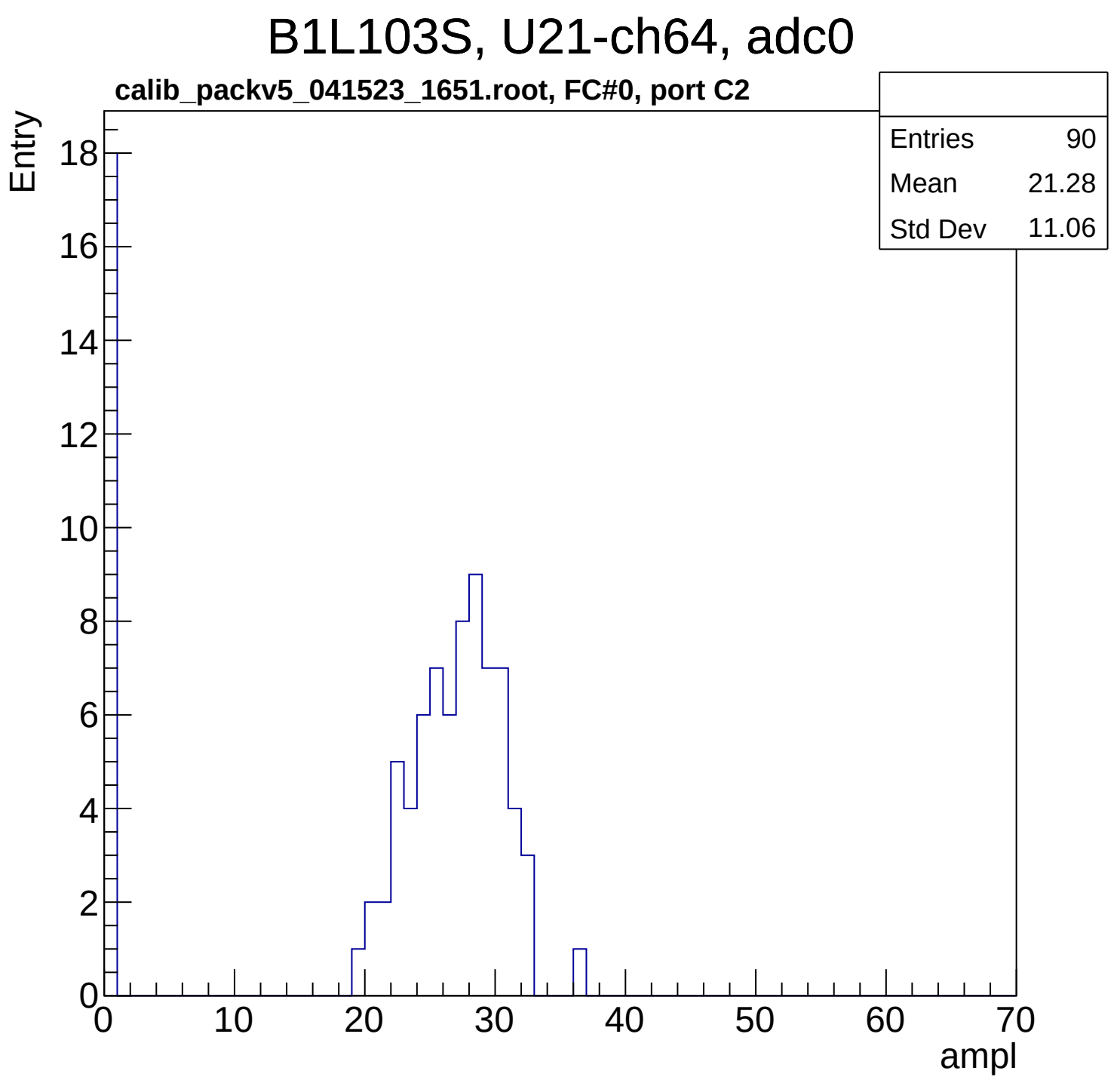
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch64, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 21.28
Std Dev 11.06
Entry
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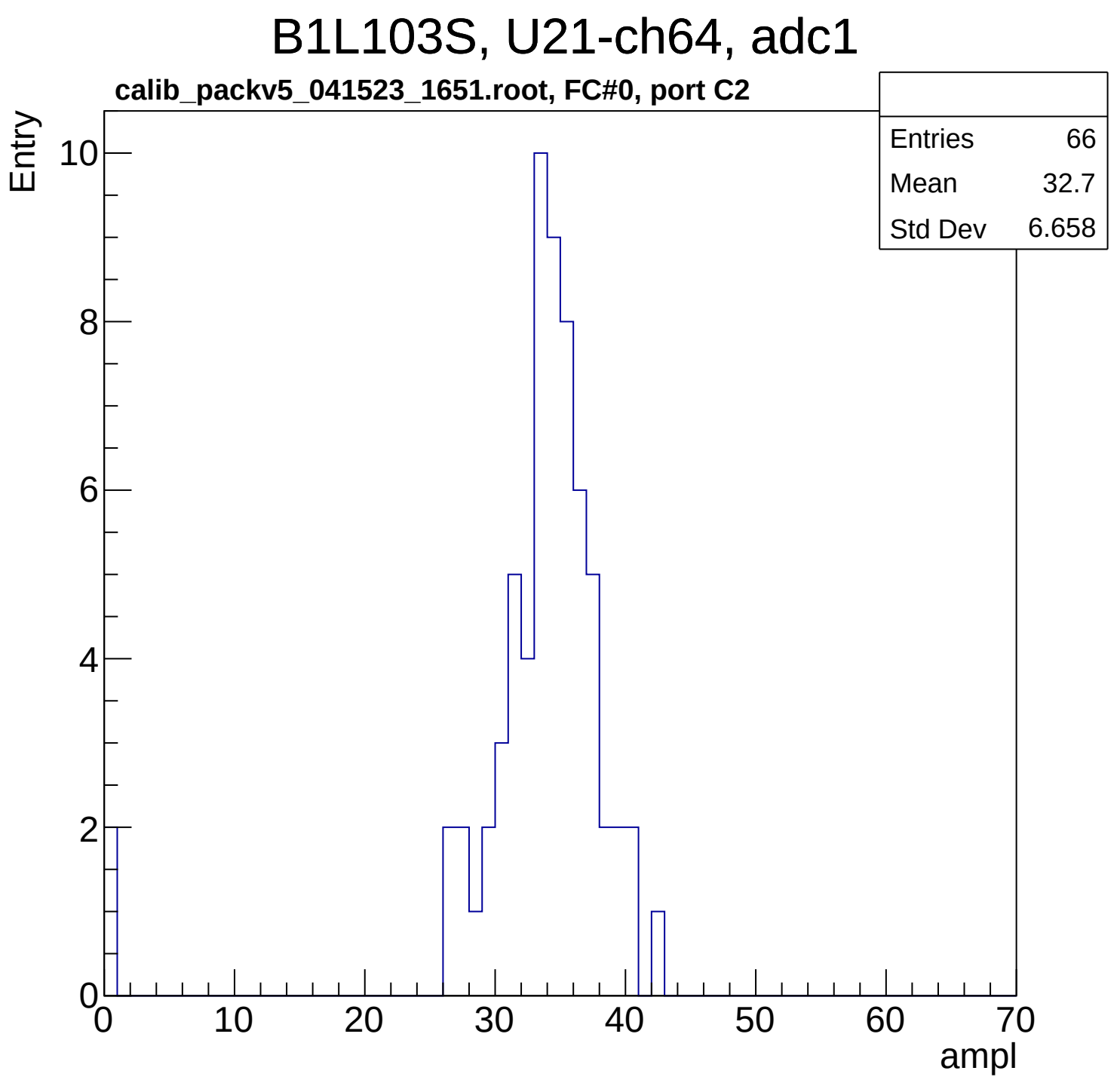
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch64, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 32.7
Std Dev 6.658
Entry
ampl
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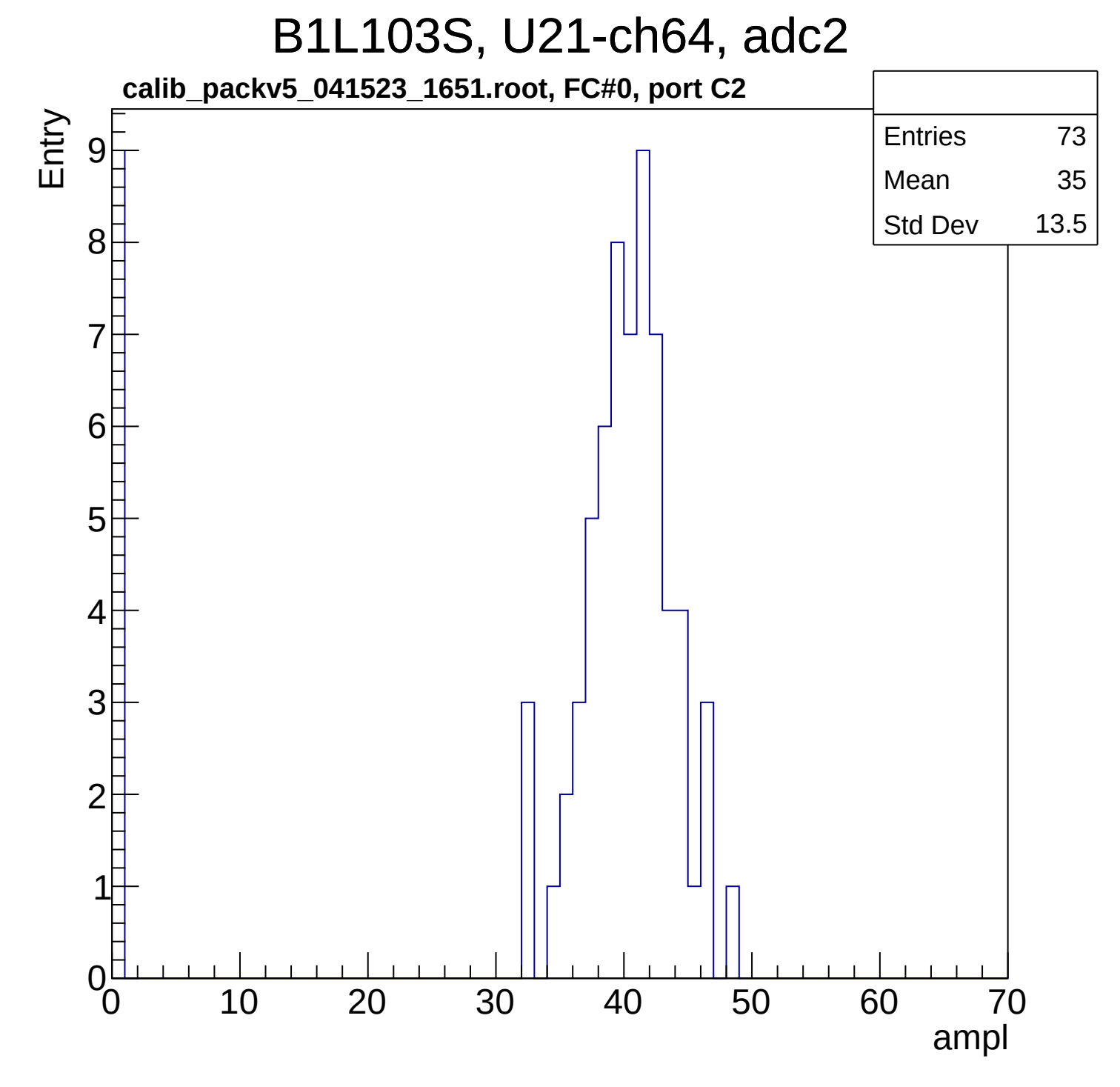
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U21-ch64, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 35
Std Dev 13.5
Entry
ampl
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3
4
5
6
7
8
9
0
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40
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60
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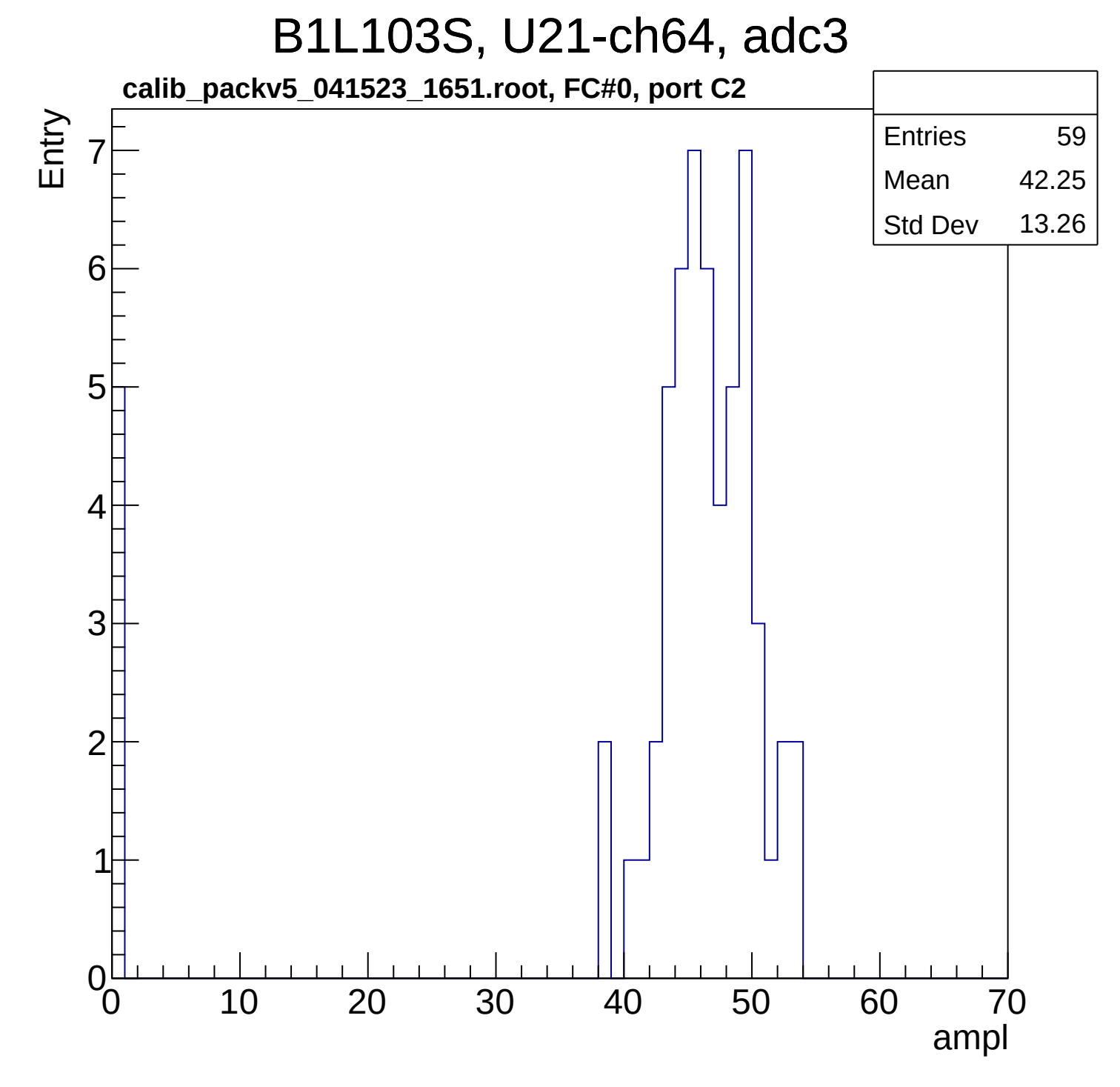
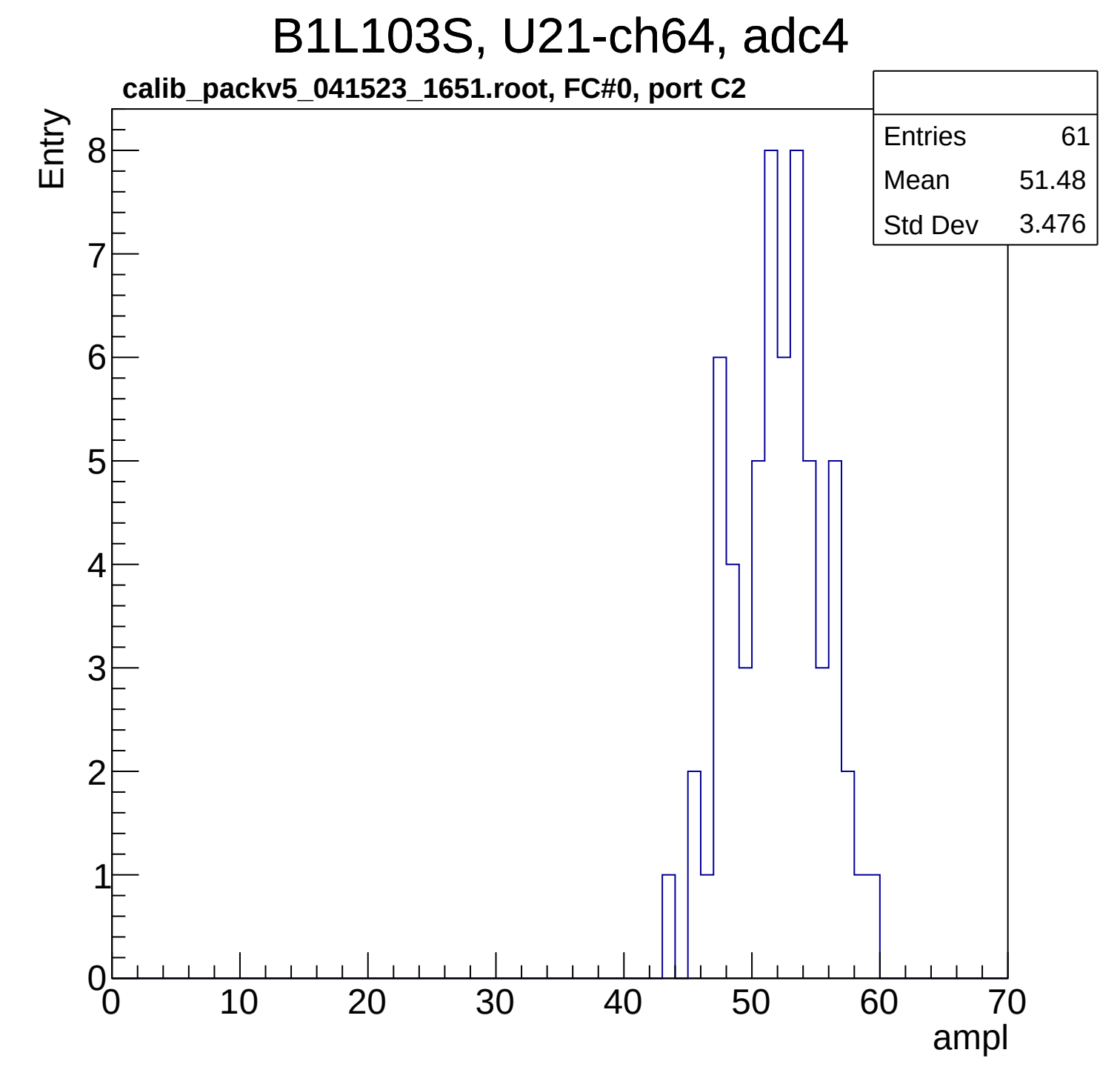

B1L103S, U21-ch64, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 42.25
Std Dev 13.26
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U21-ch64, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 51.48
Std Dev 3.476
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
50
60
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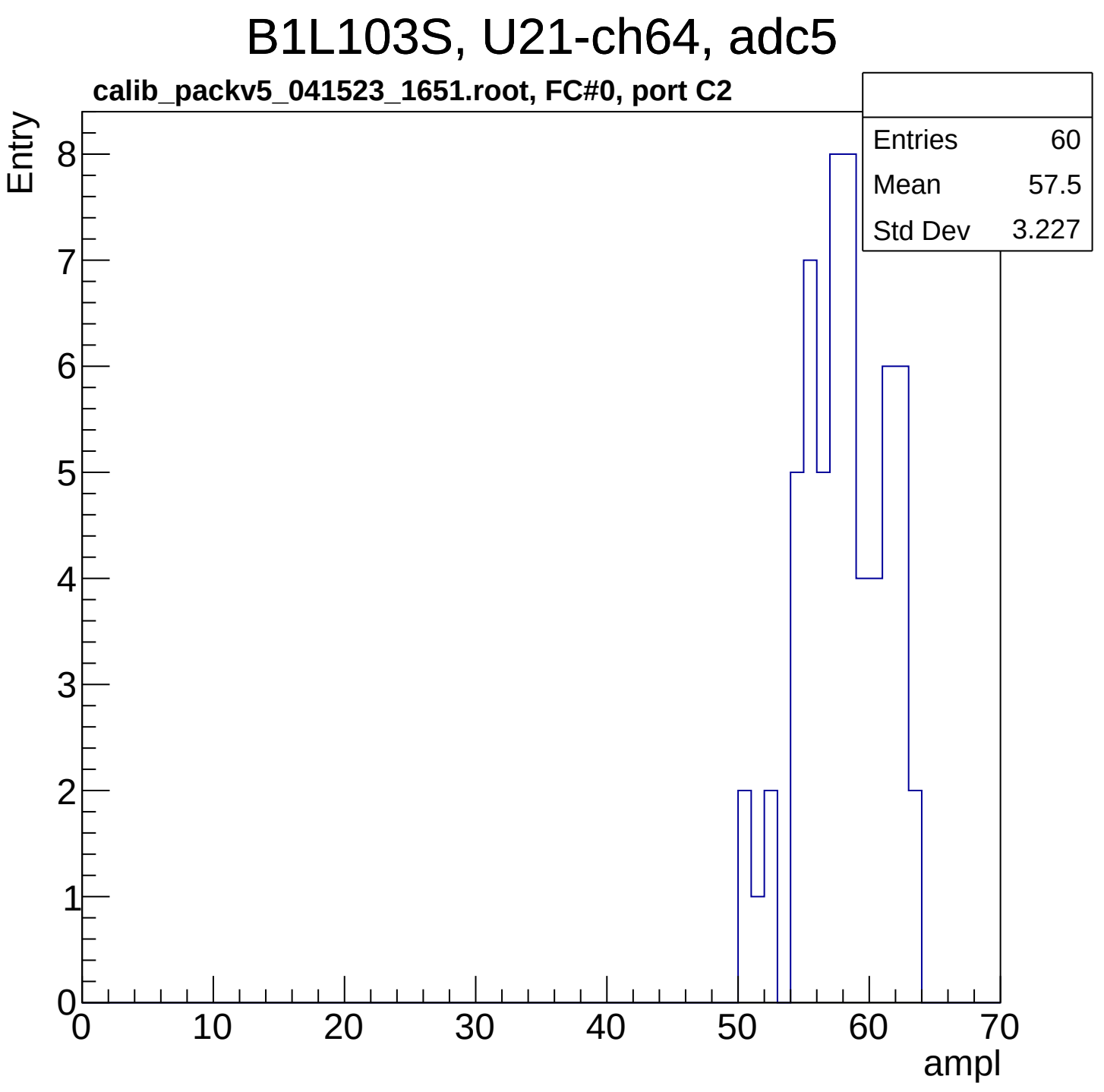
B1L103S, U21-ch64, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 57.5
Std Dev 3.227
Entry
ampl
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2
3
4
5
6
7
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0
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60
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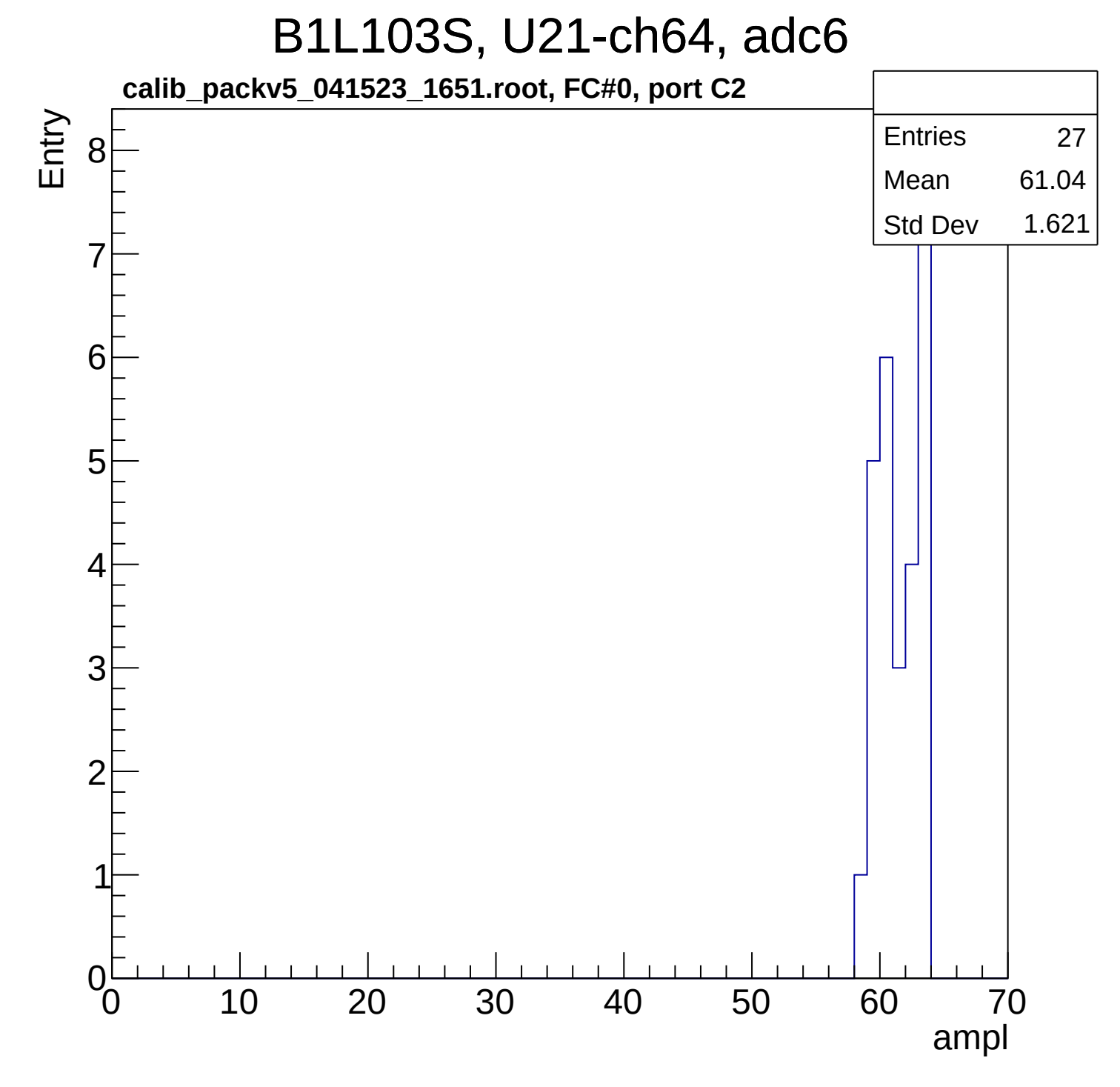
B1L103S, U21-ch64, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 61.04
Std Dev 1.621
Entry
ampl
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2
3
4
5
6
7
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0
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20
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40
50
60
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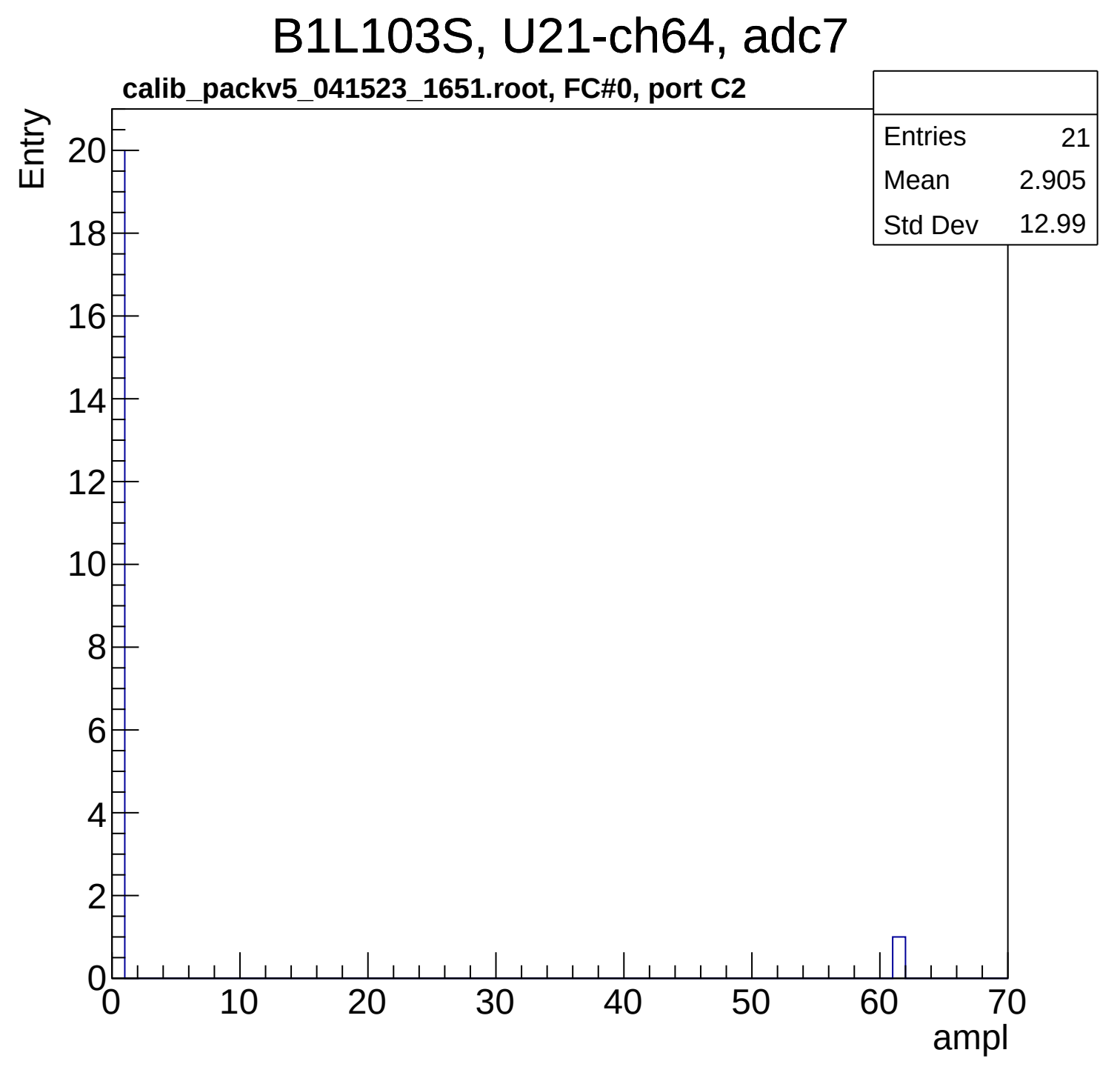
B1L103S, U21-ch64, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 2.905
Std Dev 12.99
Entry
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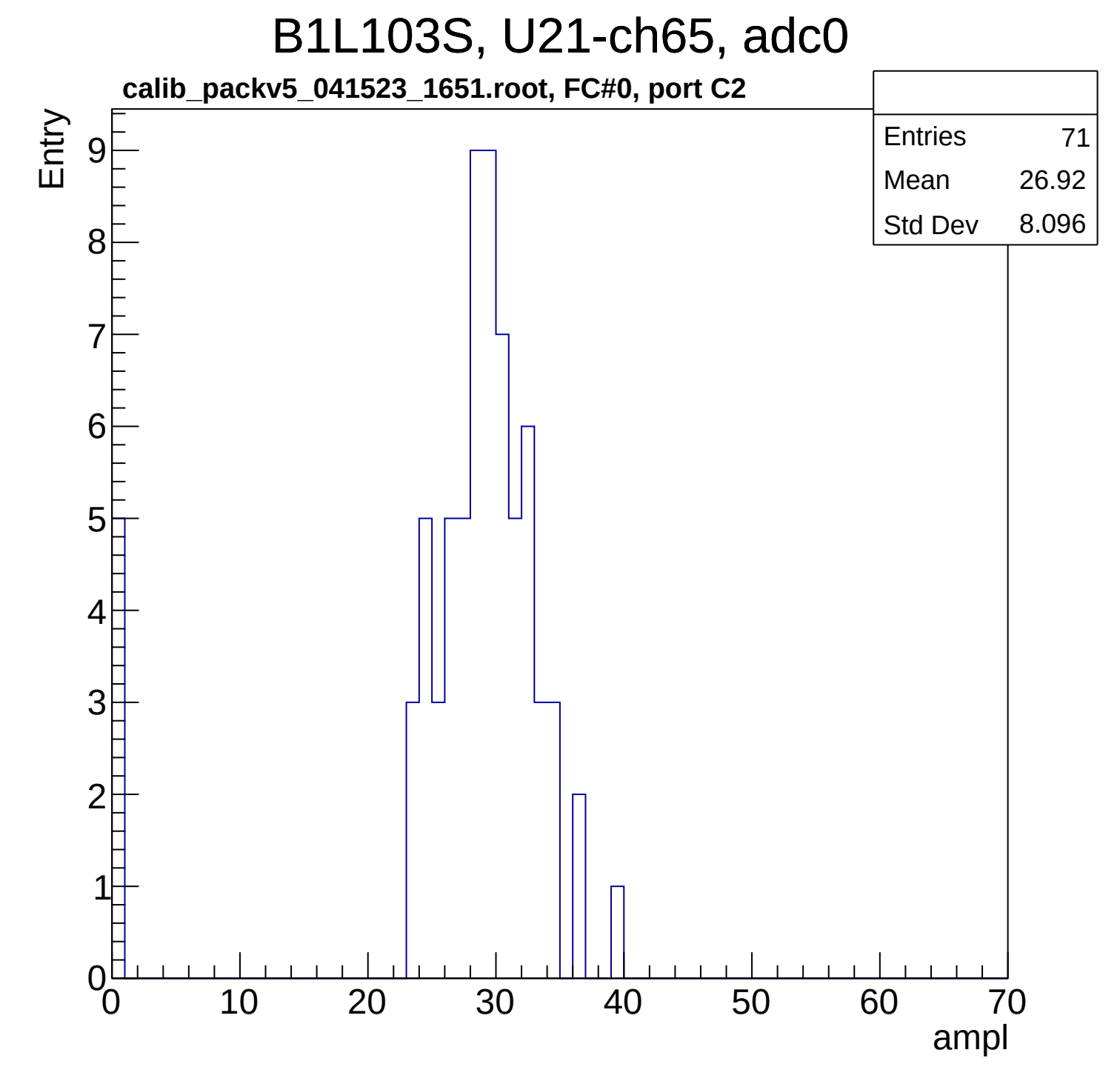
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch65, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 26.92
Std Dev 8.096
Entry
ampl
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3
4
5
6
7
8
9
0
10
20
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40
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60
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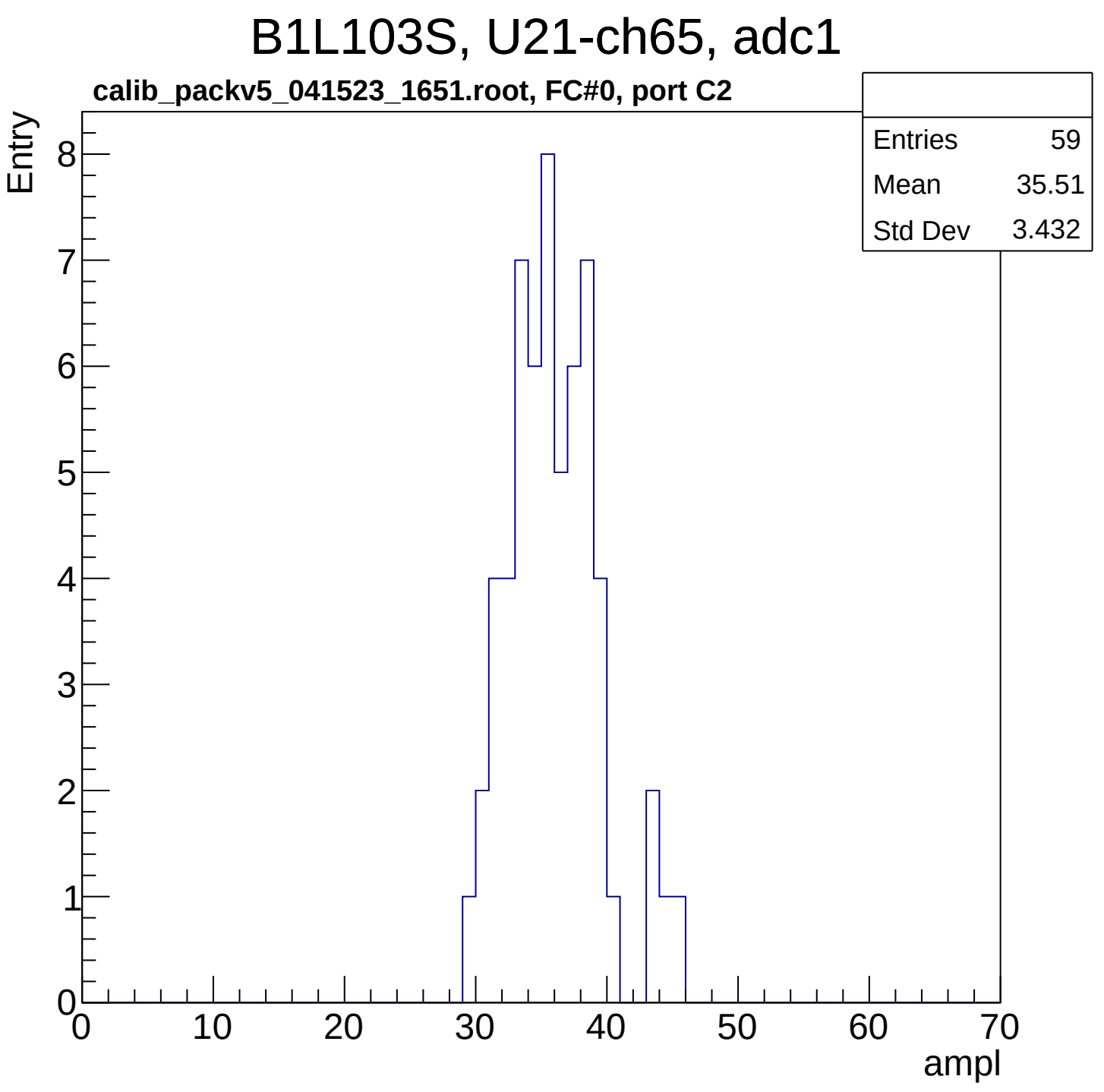
B1L103S, U21-ch65, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 35.51
Std Dev 3.432
Entry
ampl
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2
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4
5
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7
8
0
10
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40
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60
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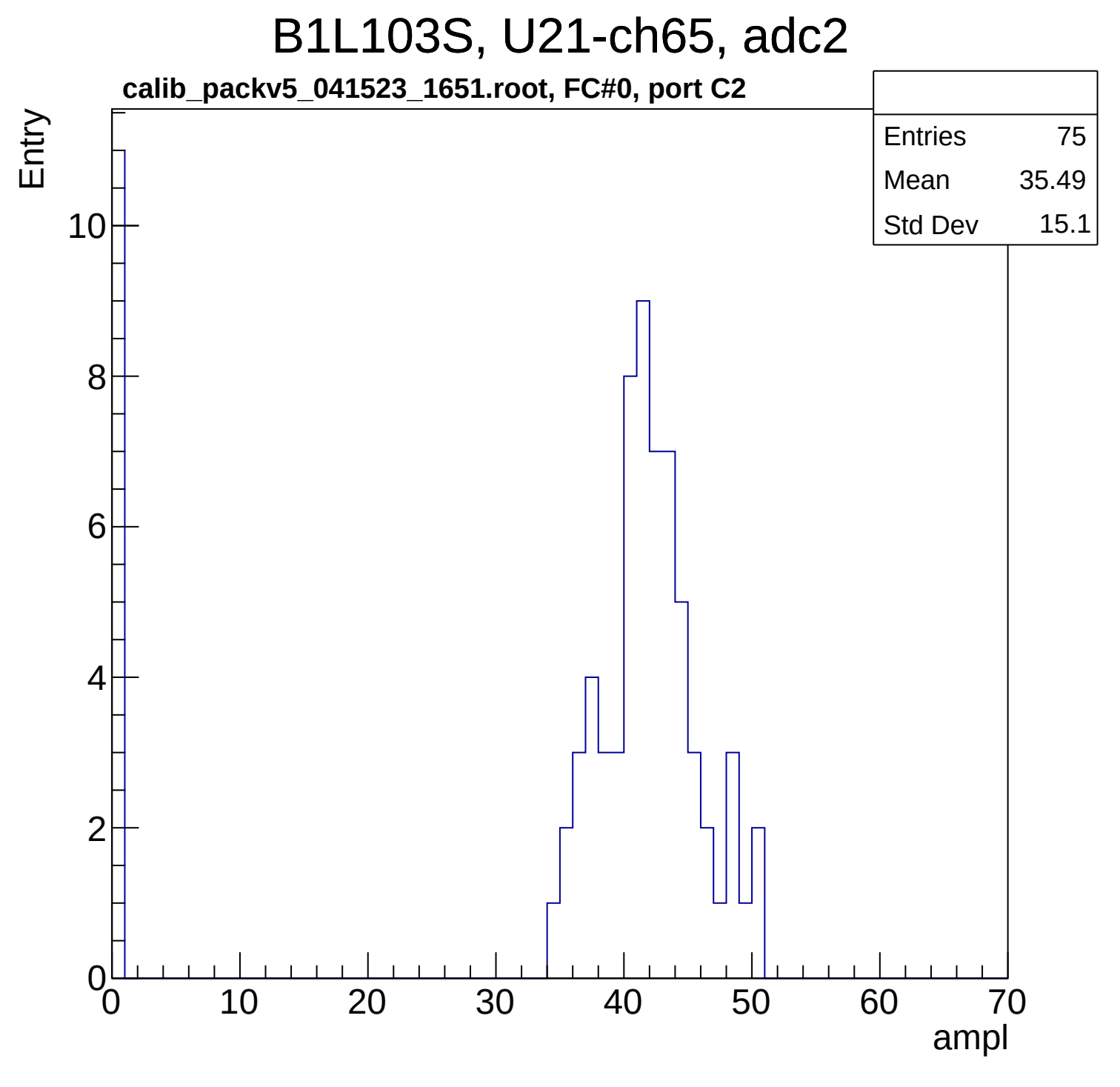
B1L103S, U21-ch65, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 35.49
Std Dev 15.1
Entry
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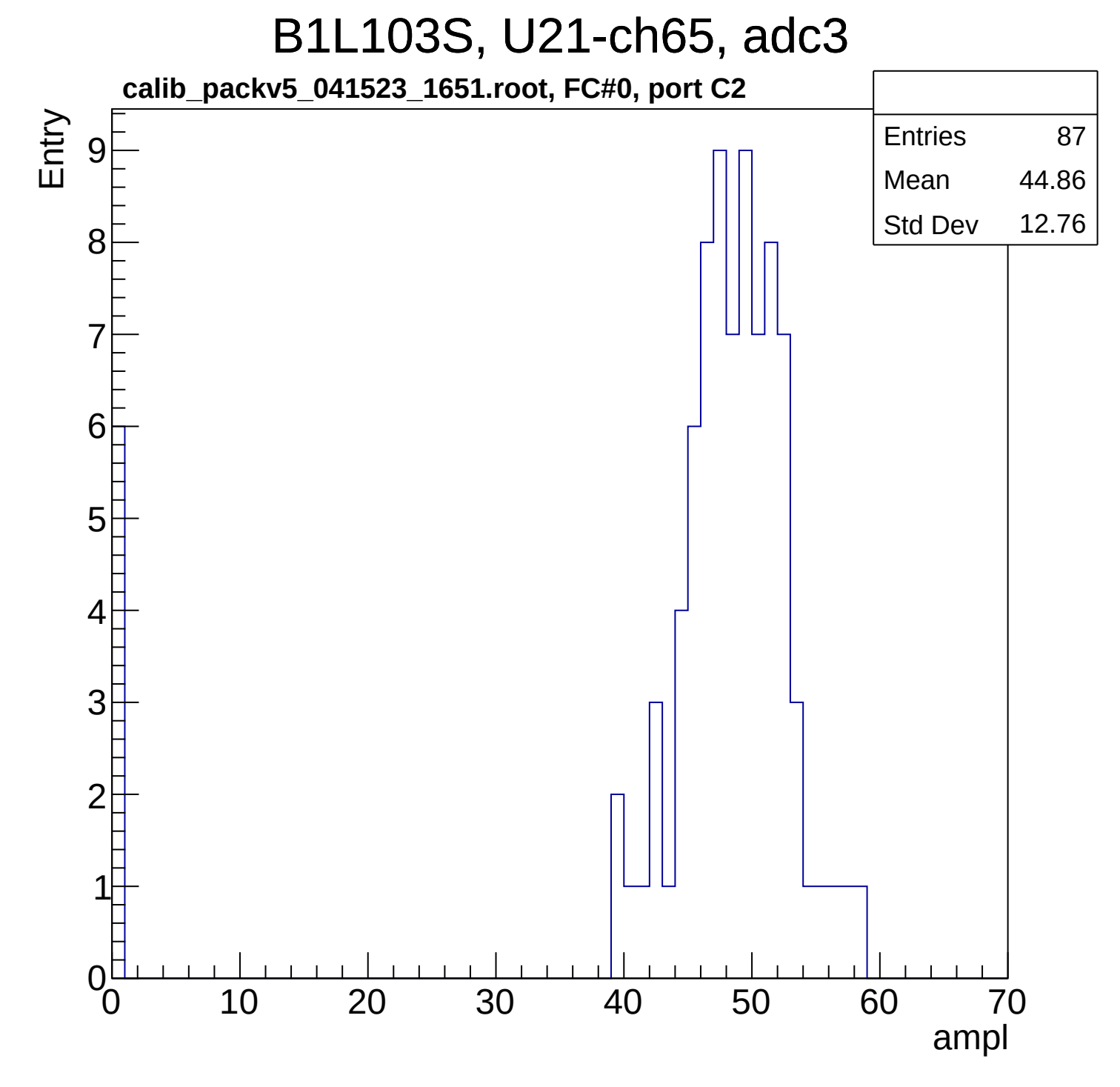
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch65, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 44.86
Std Dev 12.76
Entry
ampl
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3
4
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6
7
8
9
0
10
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60
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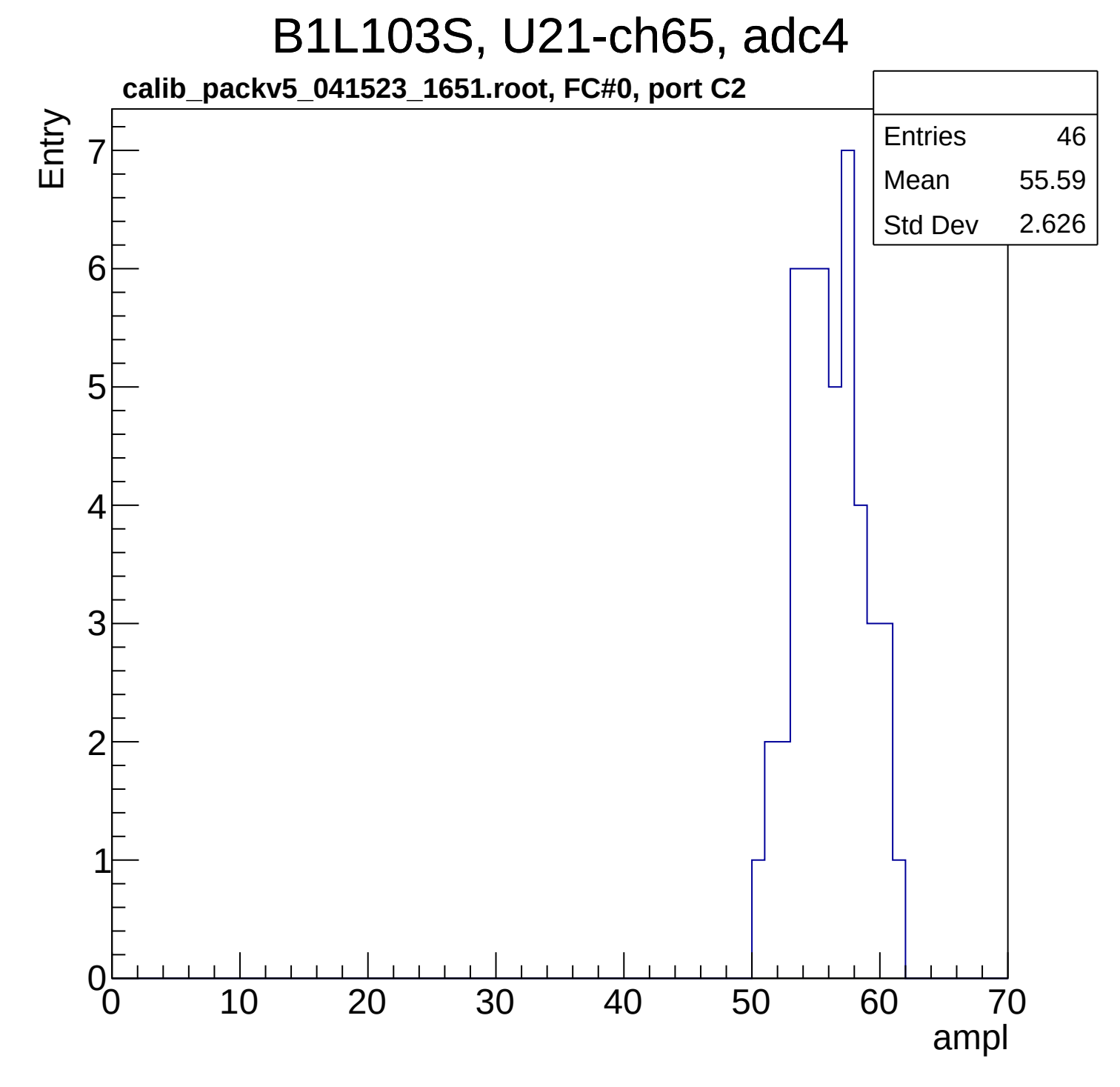
B1L103S, U21-ch65, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 55.59
Std Dev 2.626
Entry
ampl
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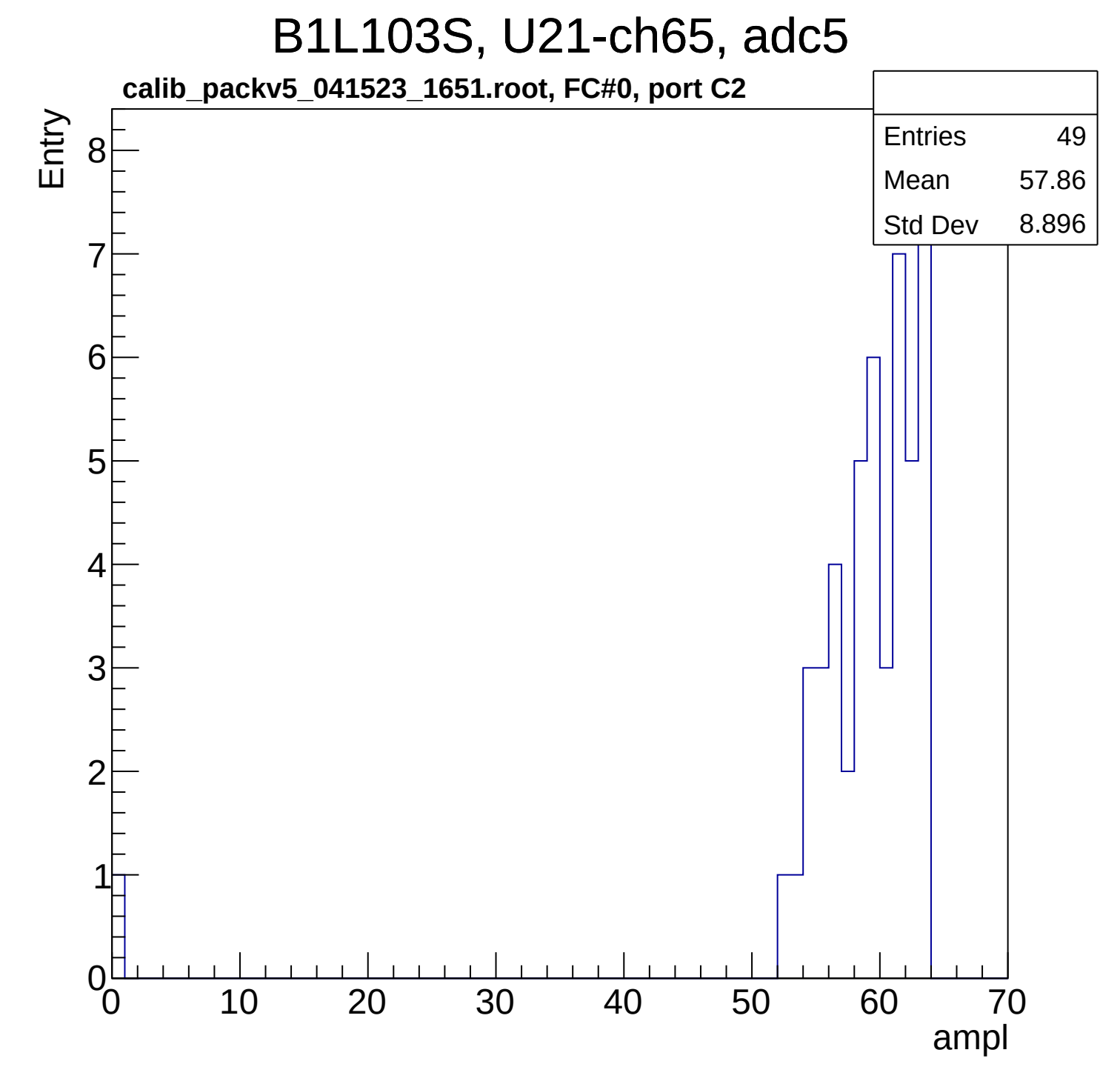
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U21-ch65, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 57.86
Std Dev 8.896
Entry
ampl
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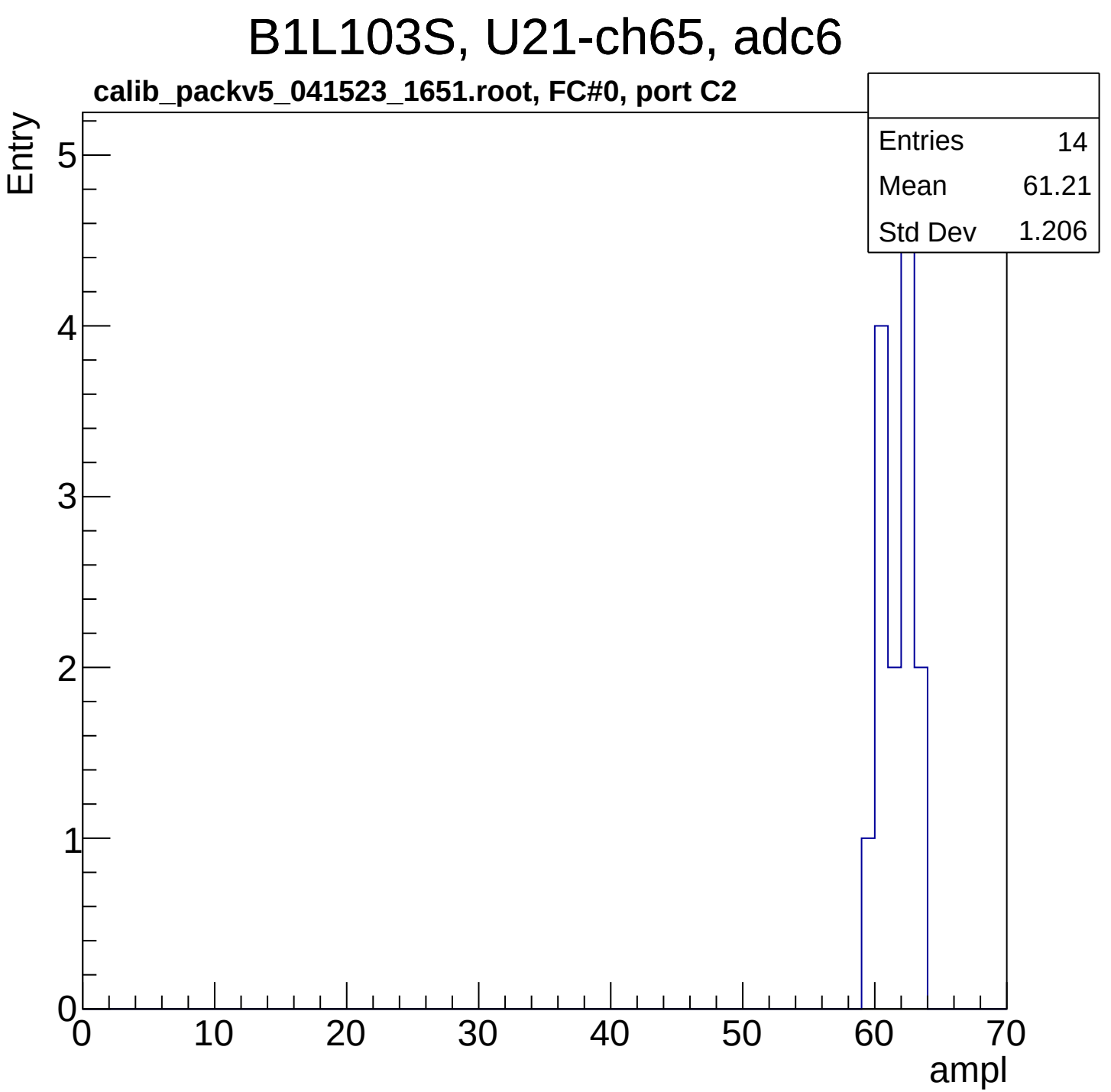
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch65, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 61.21
Std Dev 1.206
Entry
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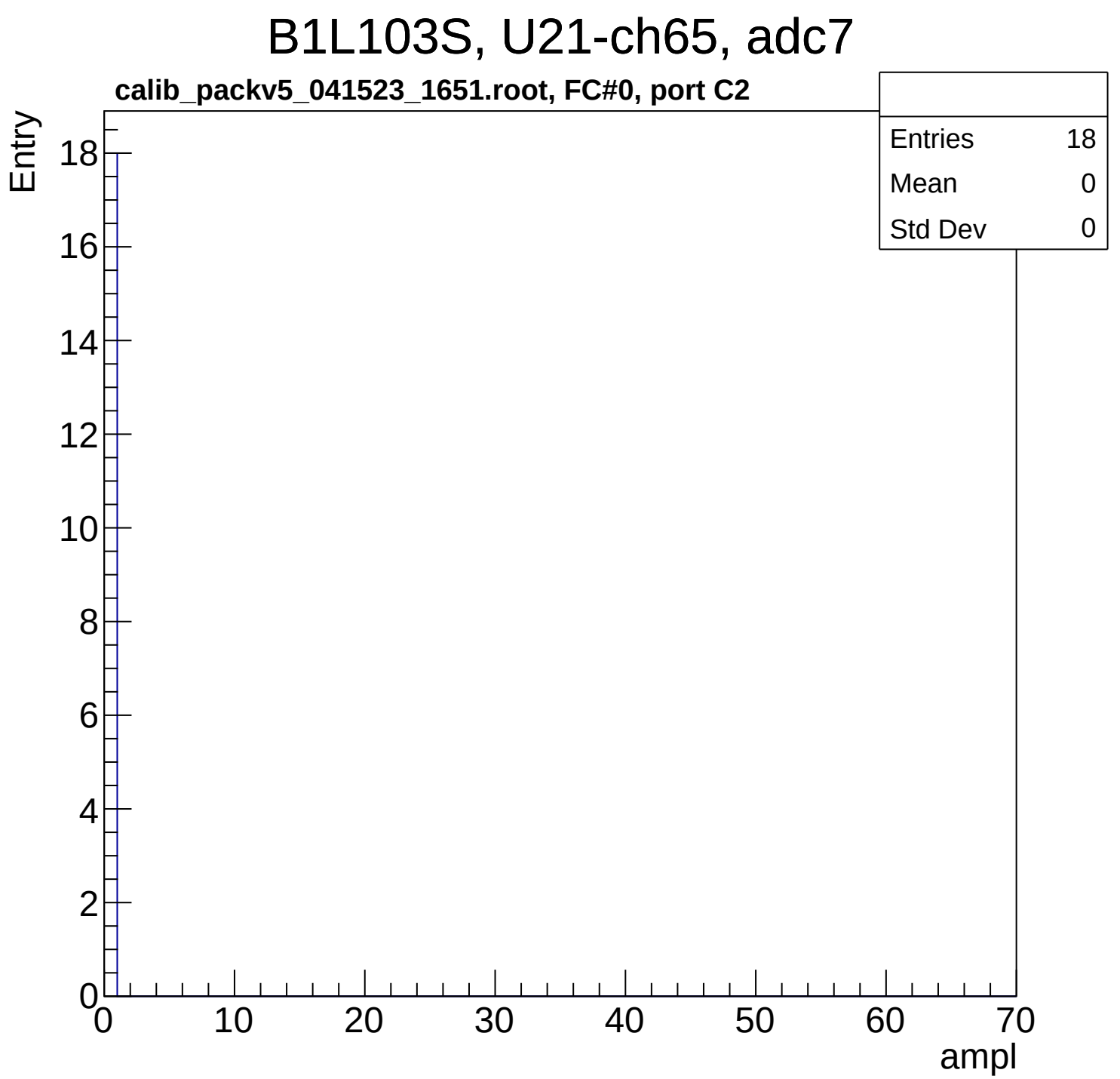
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch65, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
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6
8
10
12
14
16
18
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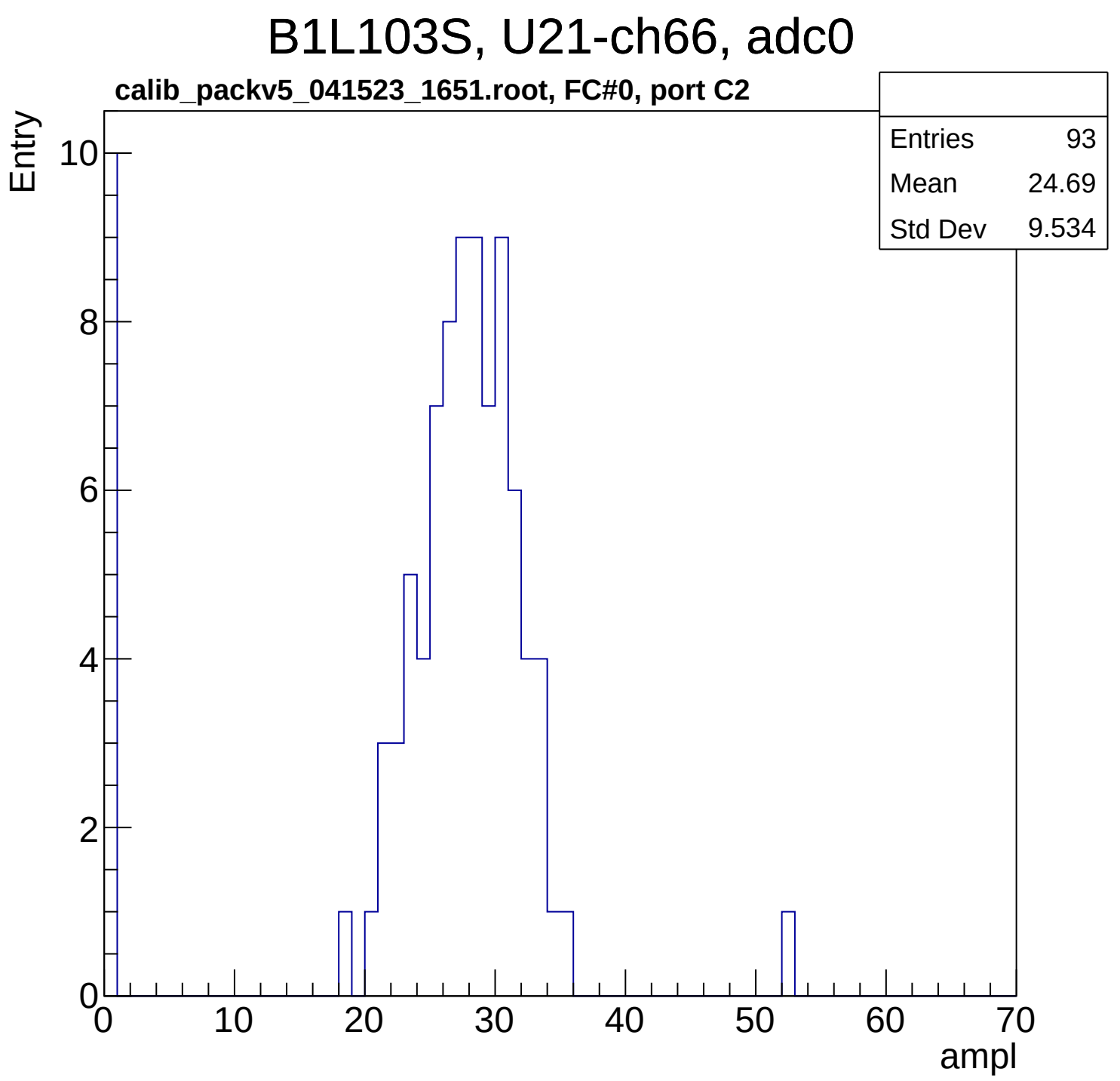
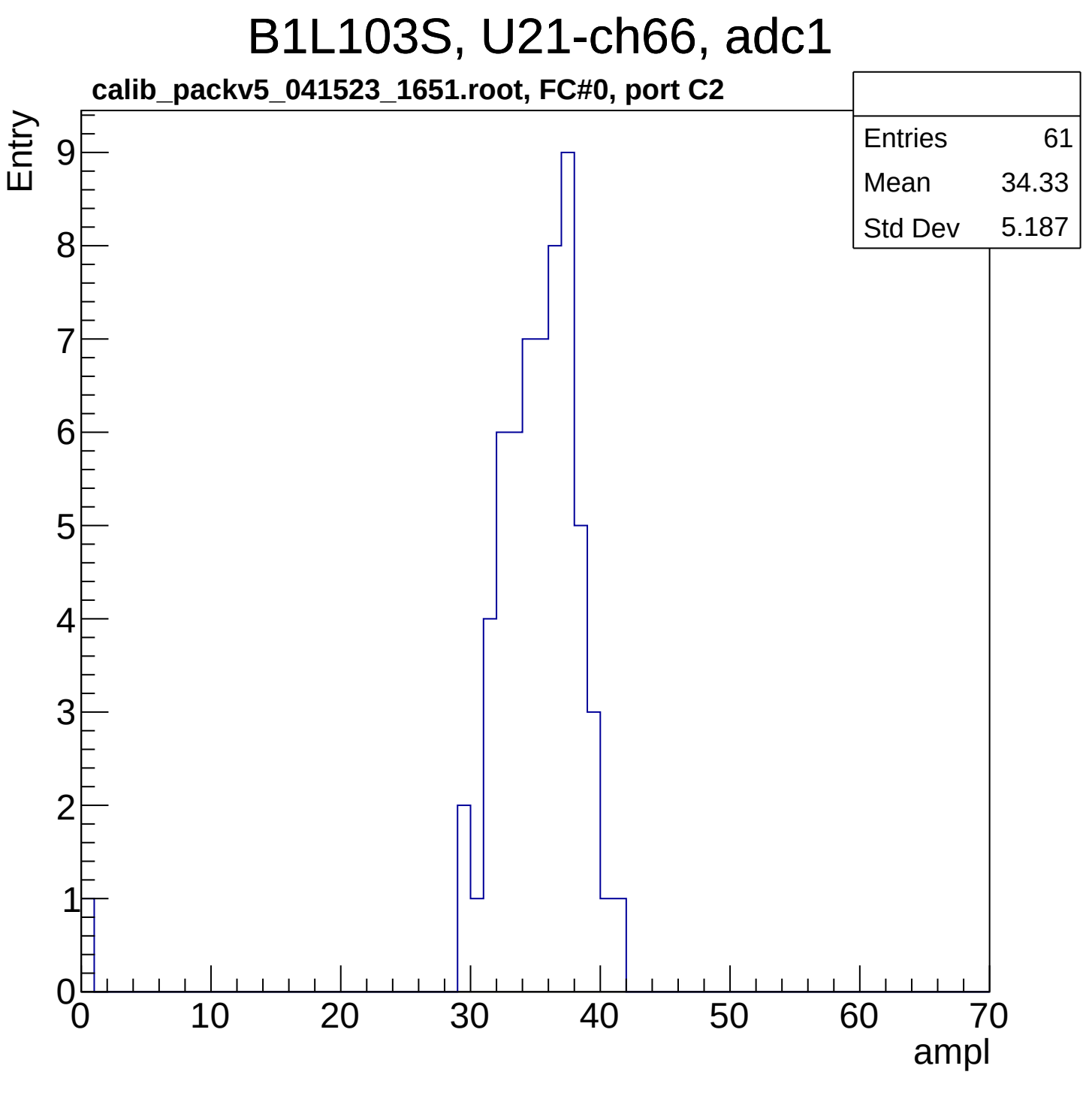
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch66, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 24.69
Std Dev 9.534
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch66, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 34.33
Std Dev 5.187
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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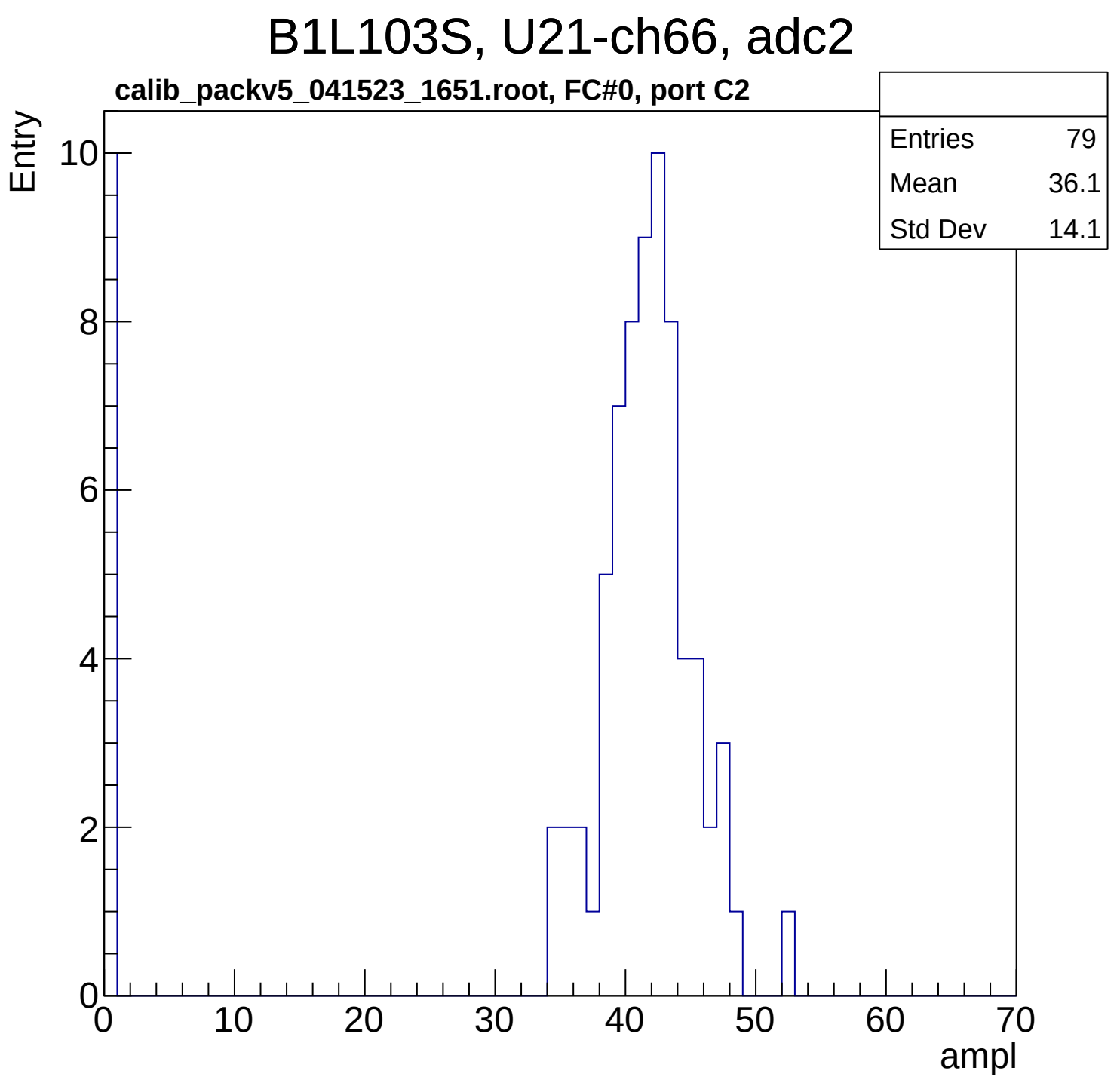
B1L103S, U21-ch66, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 36.1
Std Dev 14.1
Entry
0
2
4
6
8
10
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10
20
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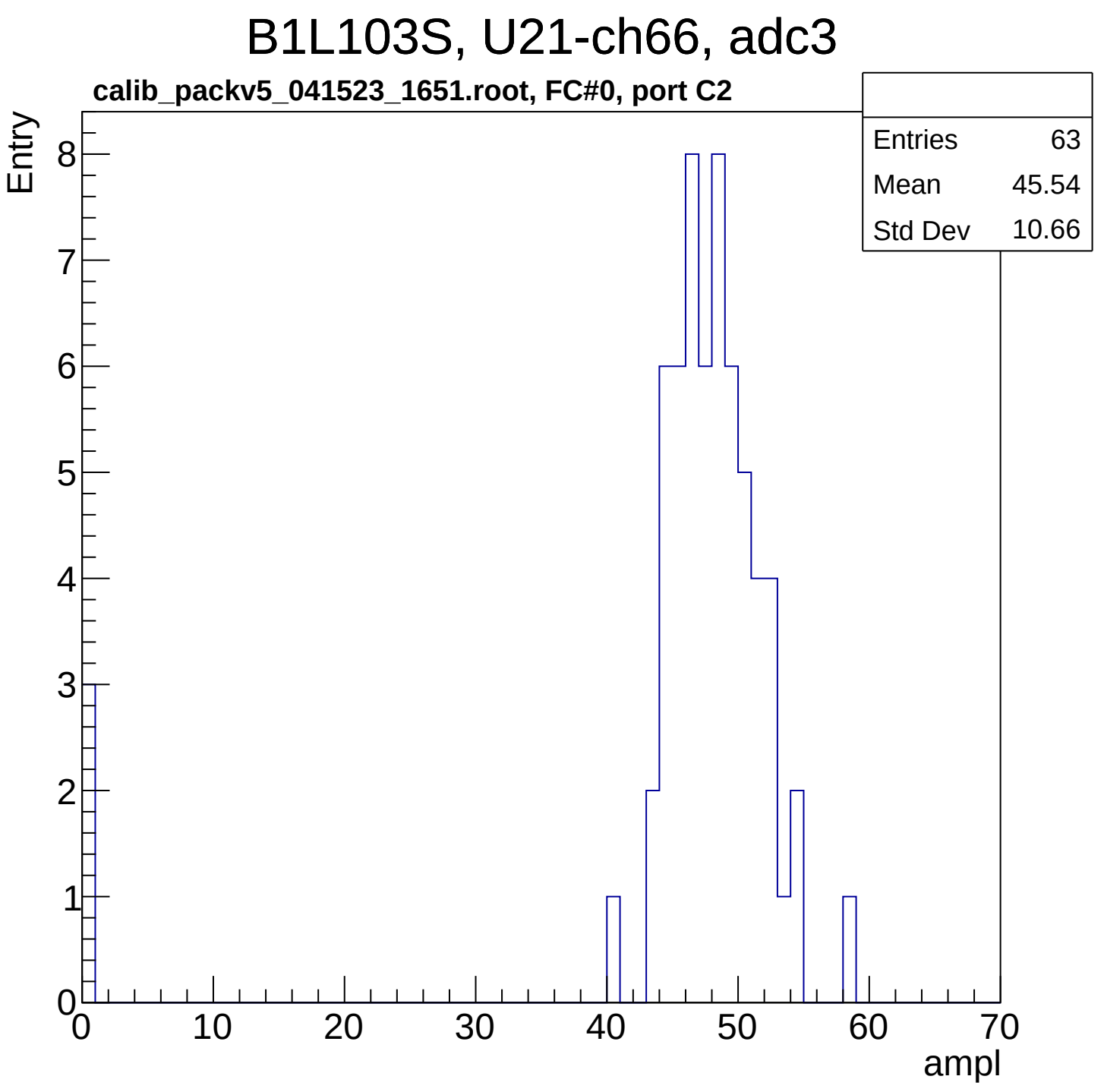
40
50
60
70
ampl


B1L103S, U21-ch66, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 45.54
Std Dev 10.66
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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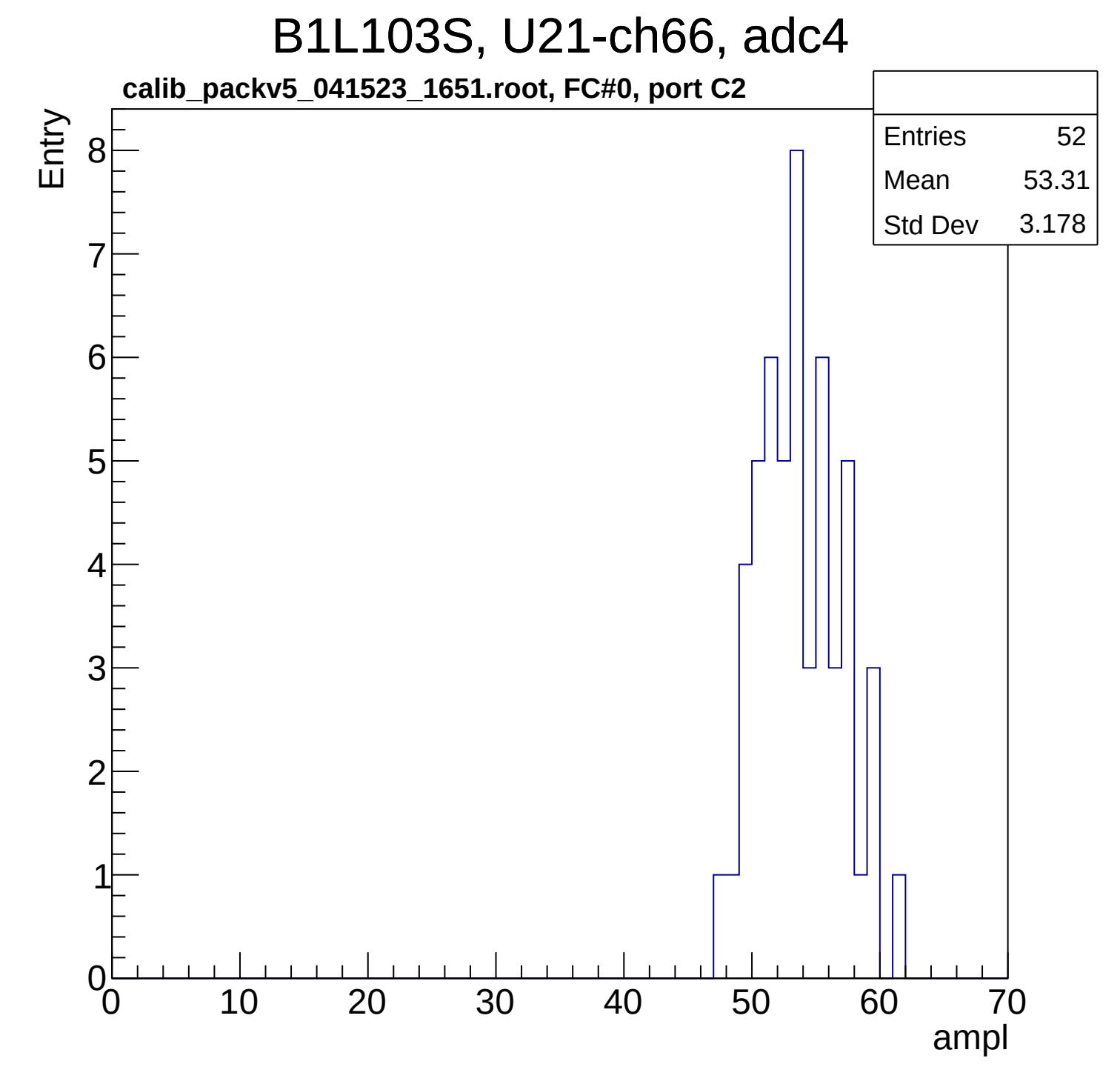
B1L103S, U21-ch66, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 53.31
Std Dev 3.178
Entry
ampl
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2
3
4
5
6
7
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0
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40
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60
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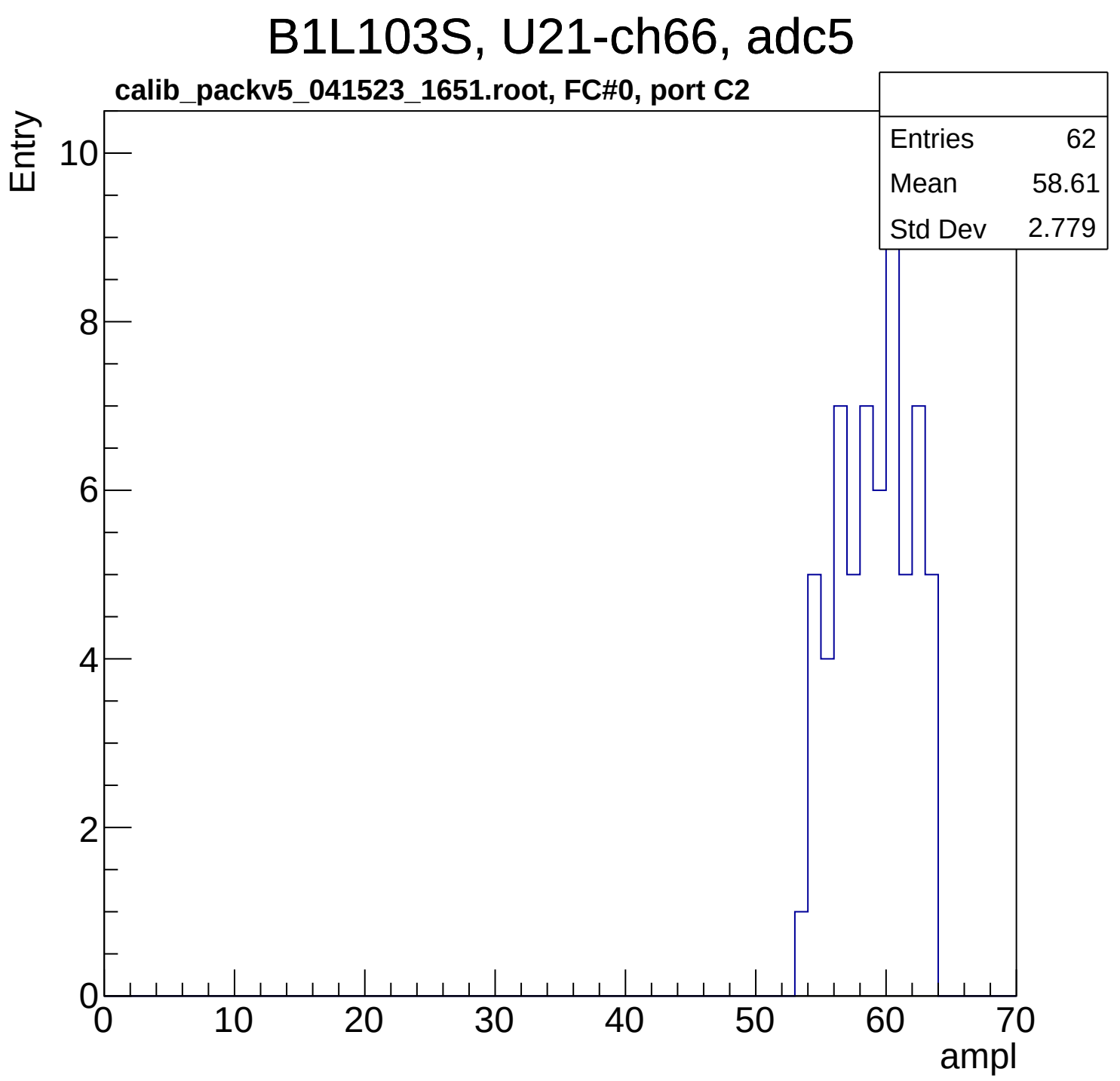
B1L103S, U21-ch66, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 58.61
Std Dev 2.779
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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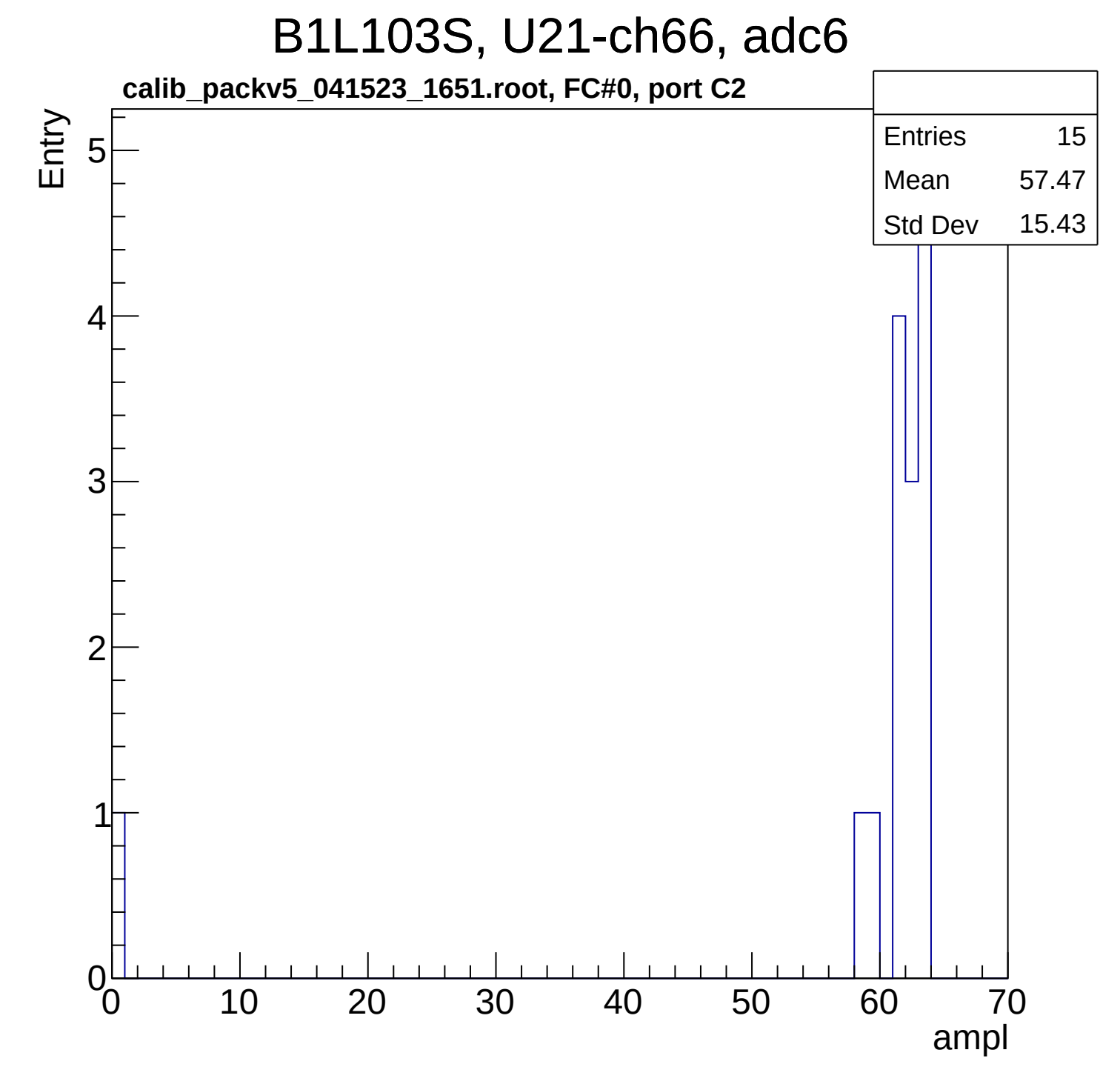
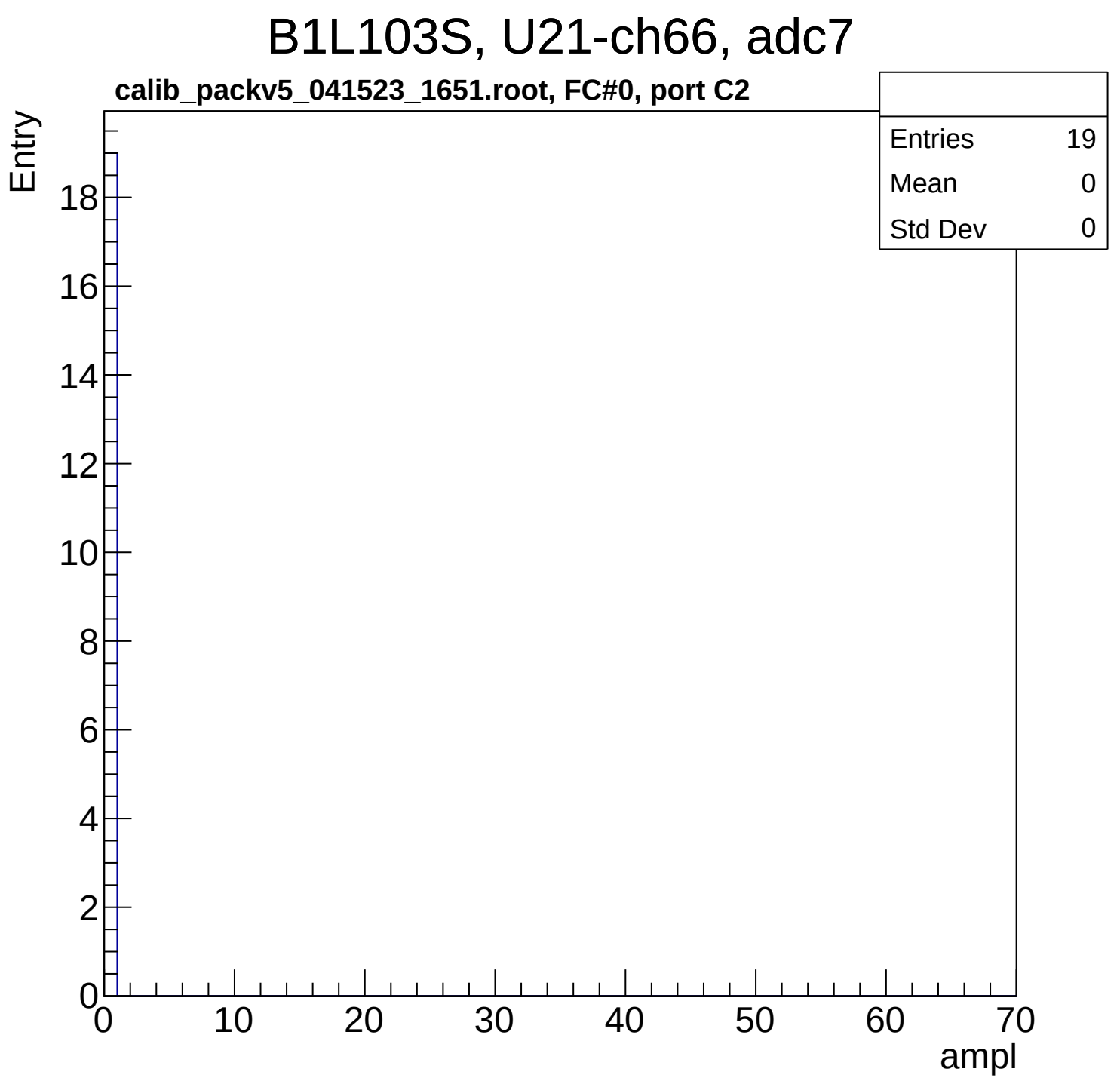
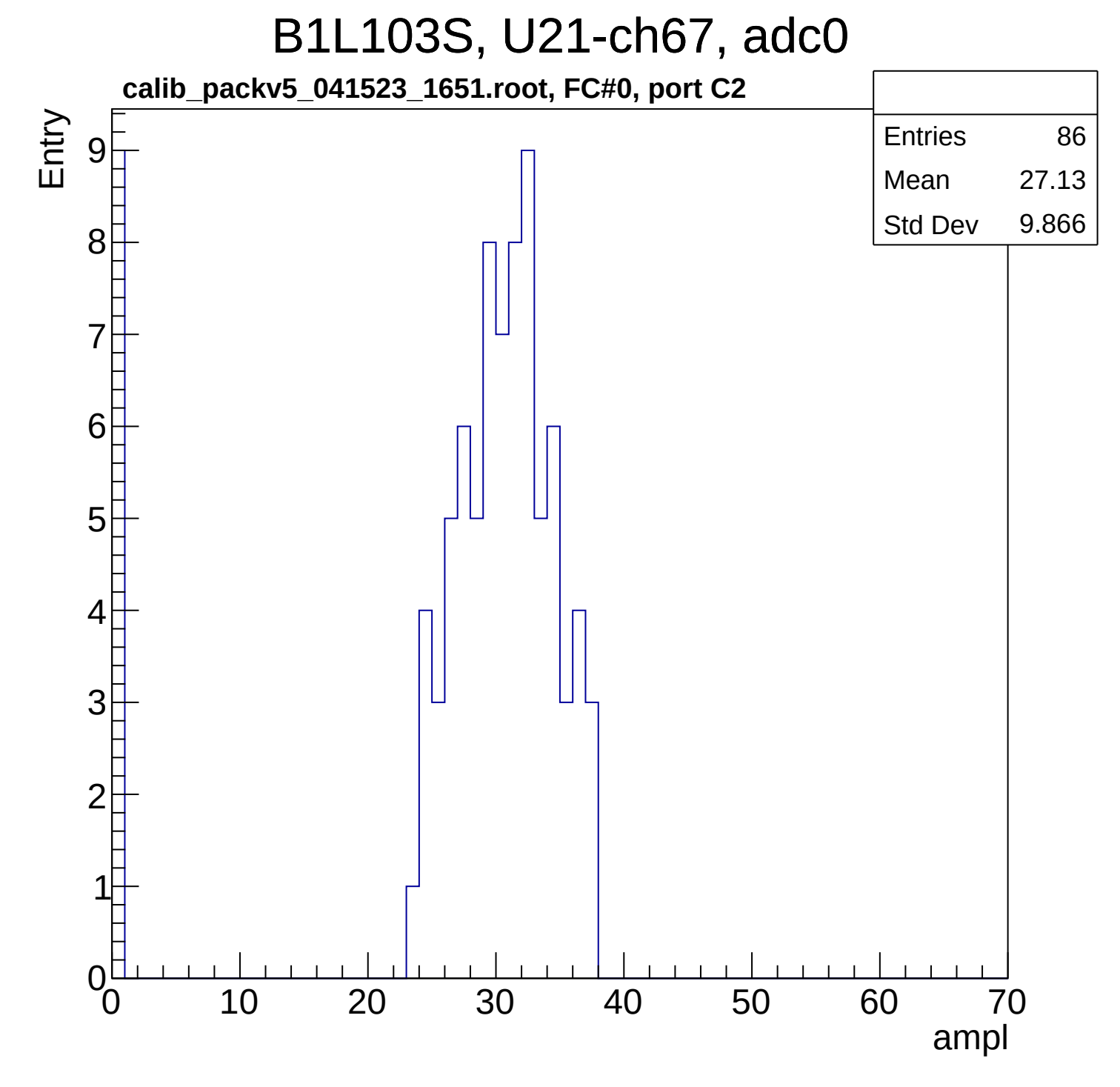

B1L103S, U21-ch66, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 57.47
Std Dev 15.43
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U21-ch66, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch67, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 27.13
Std Dev 9.866
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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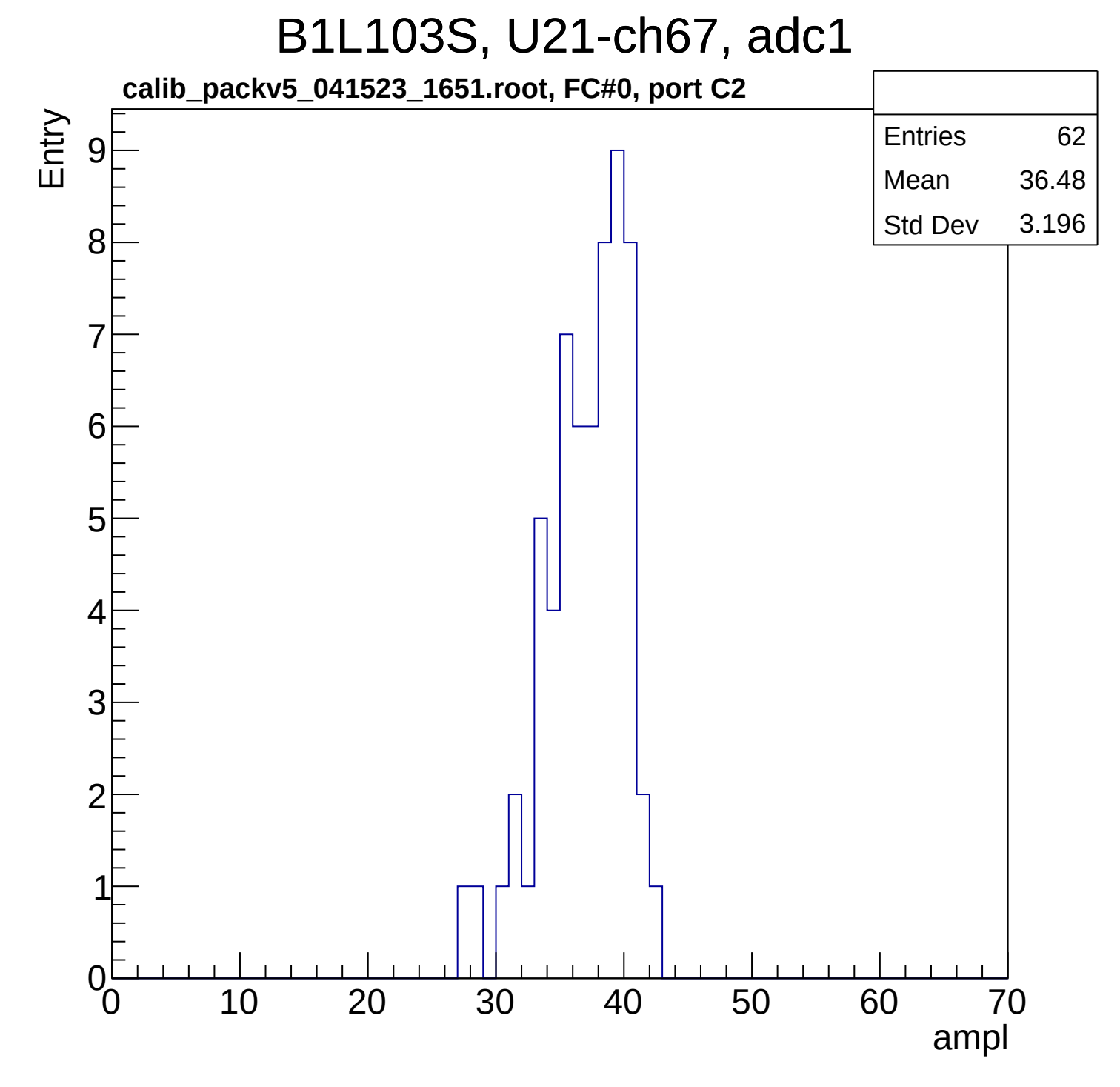
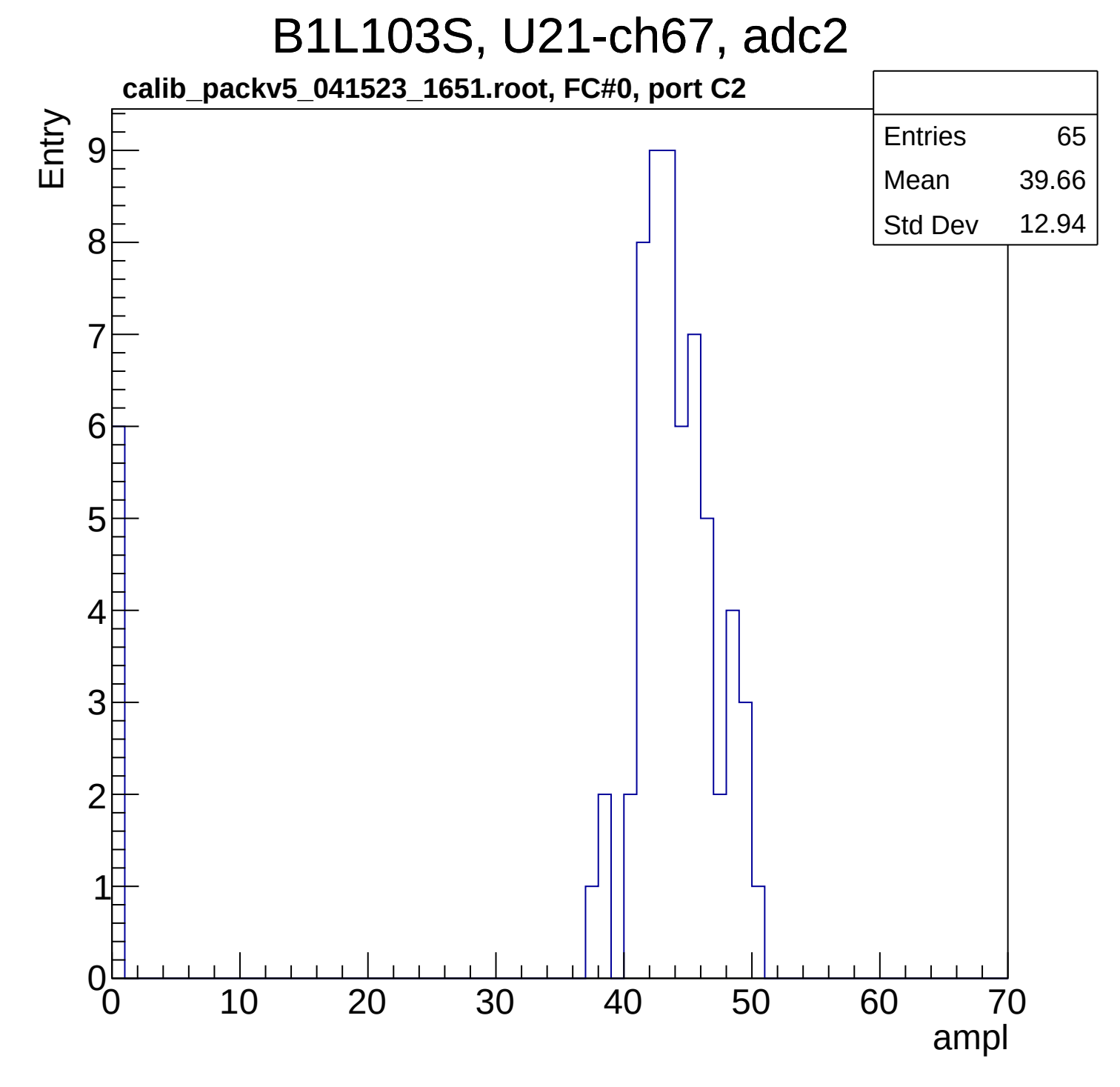
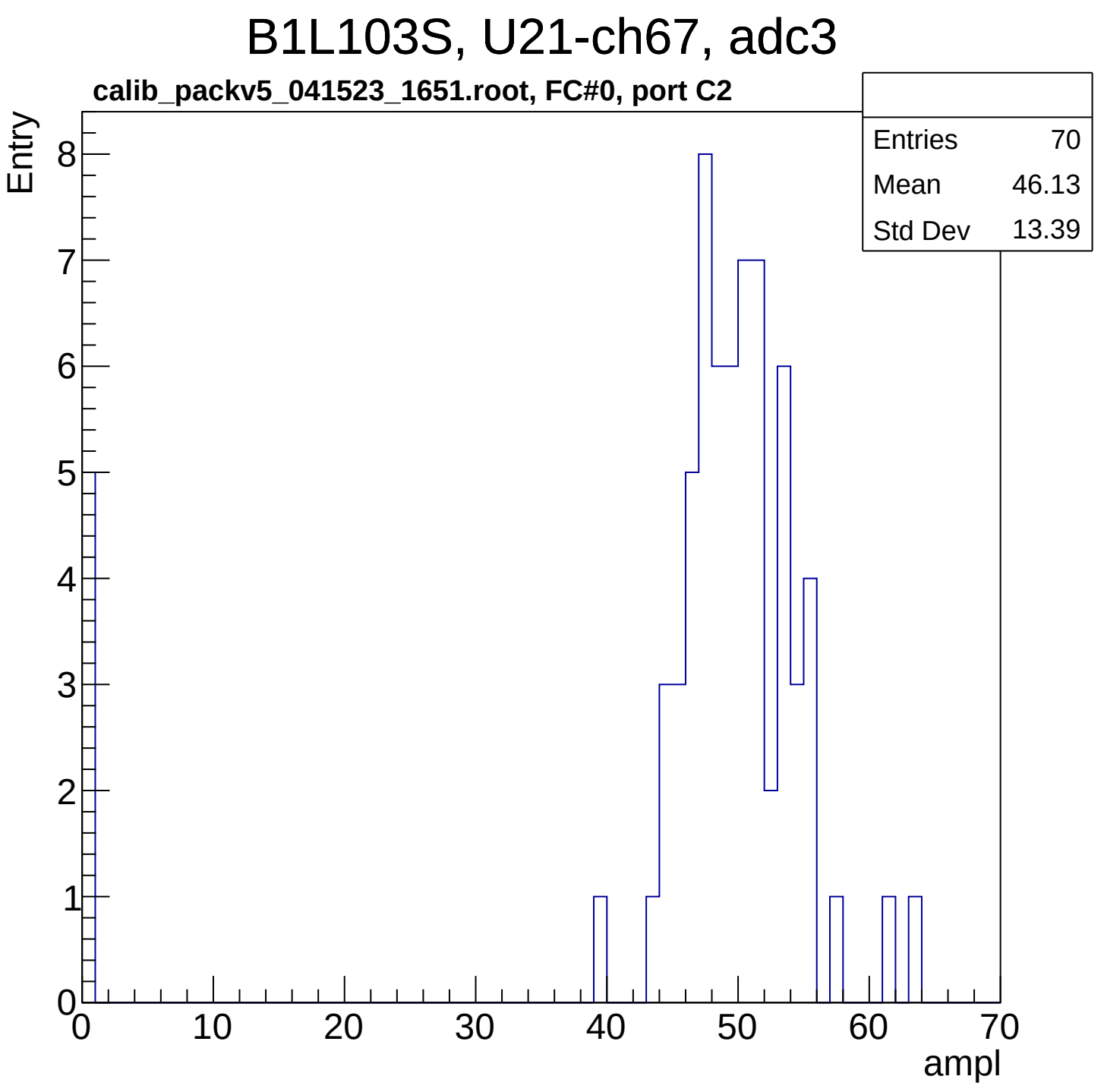
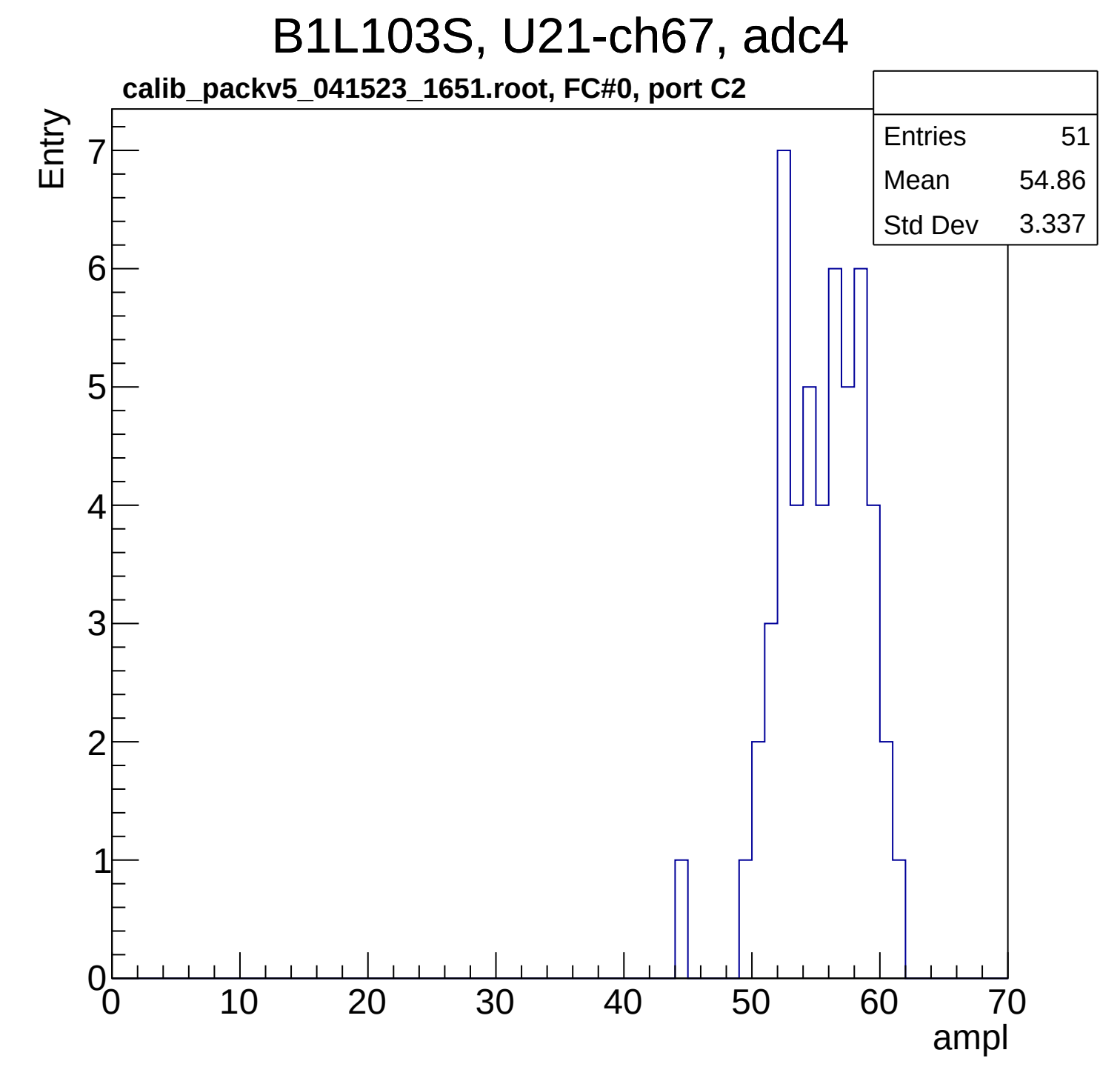
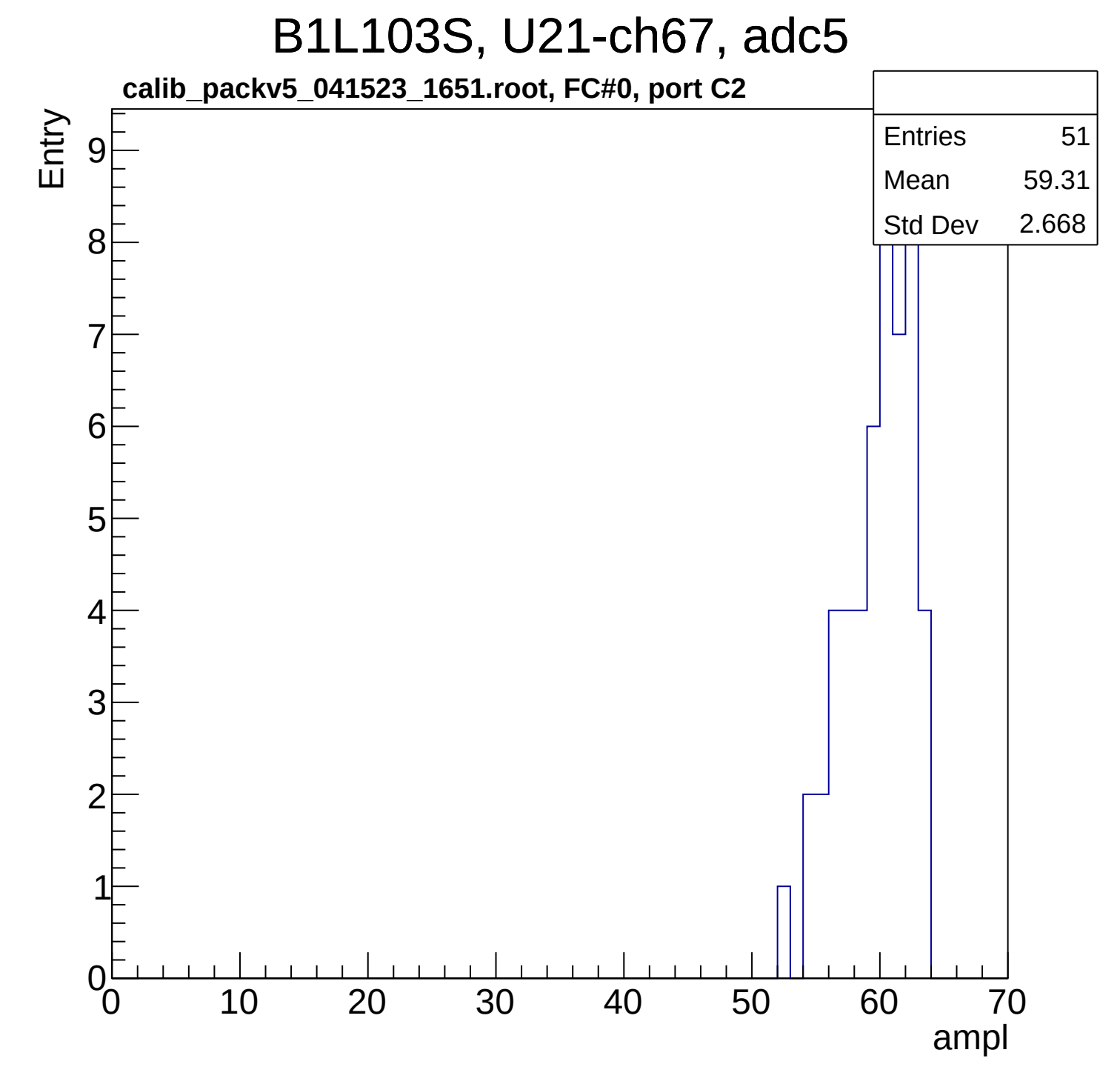
40
50
60
70

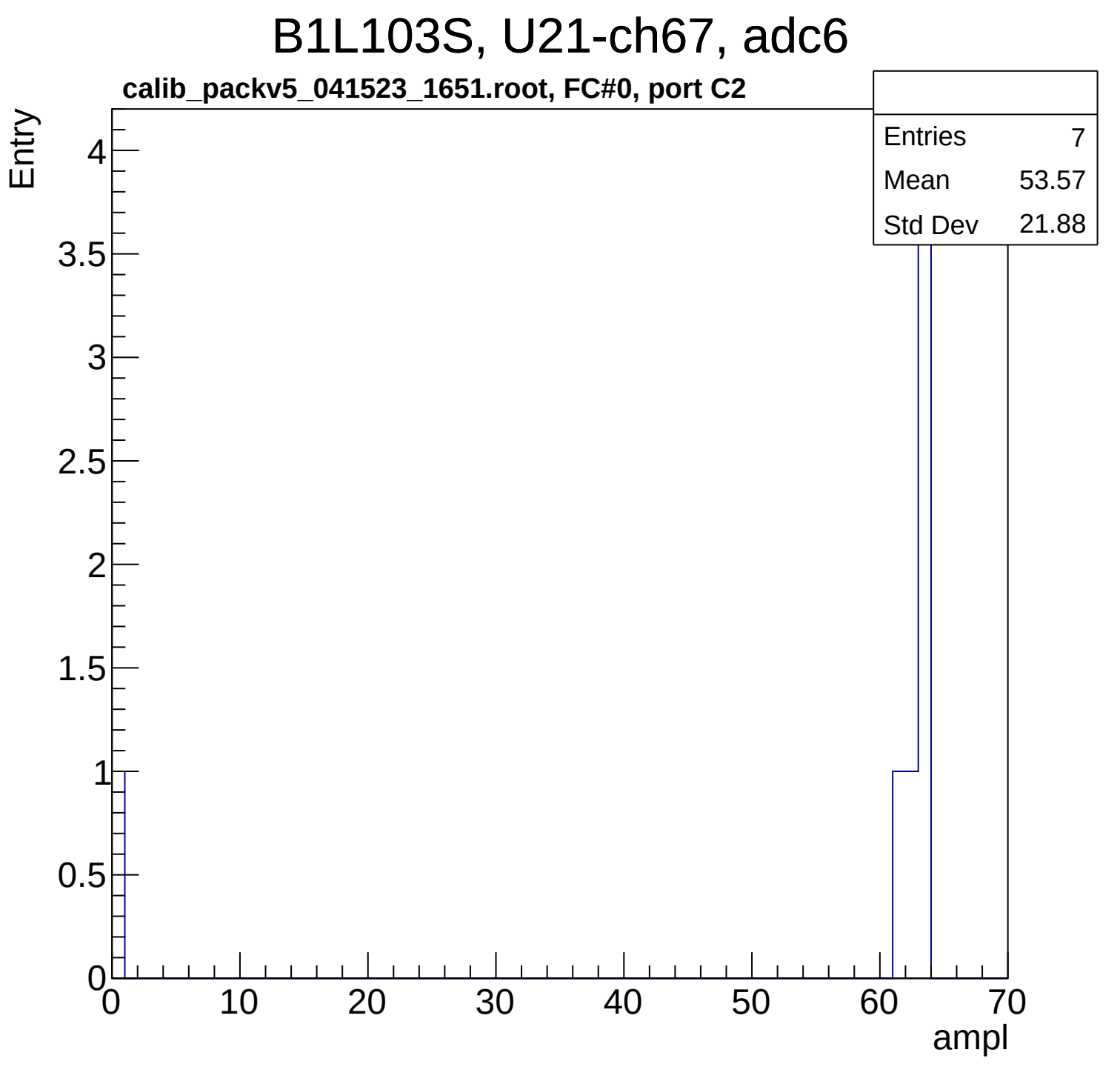

B1L103S, U21-ch67, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 36.48
Std Dev 3.196
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch67, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 39.66
Std Dev 12.94
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch67, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 46.13
Std Dev 13.39
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch67, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 54.86
Std Dev 3.337
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U21-ch67, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 59.31
Std Dev 2.668
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch67, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 53.57
Std Dev 21.88
Entry
ampl
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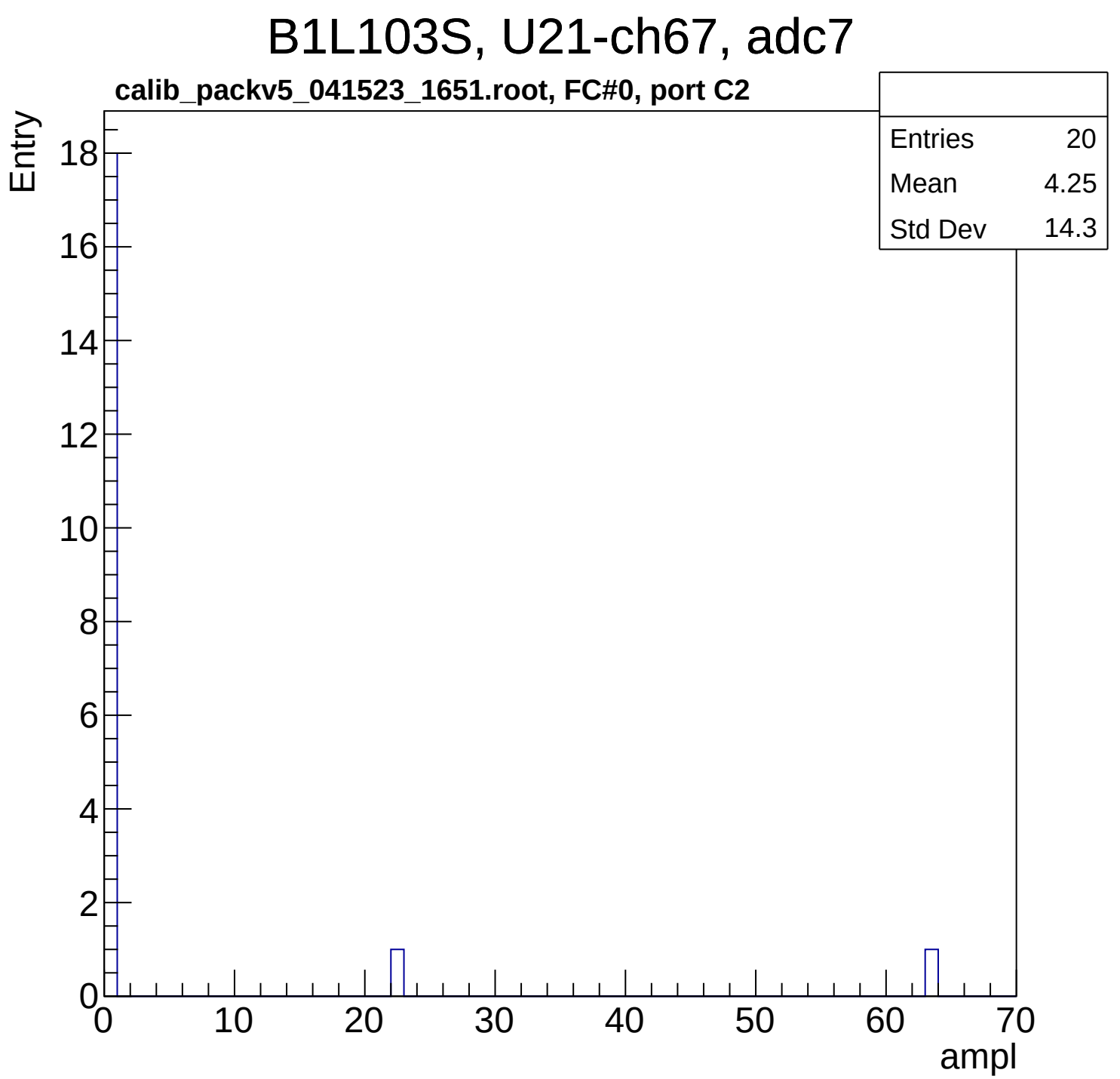
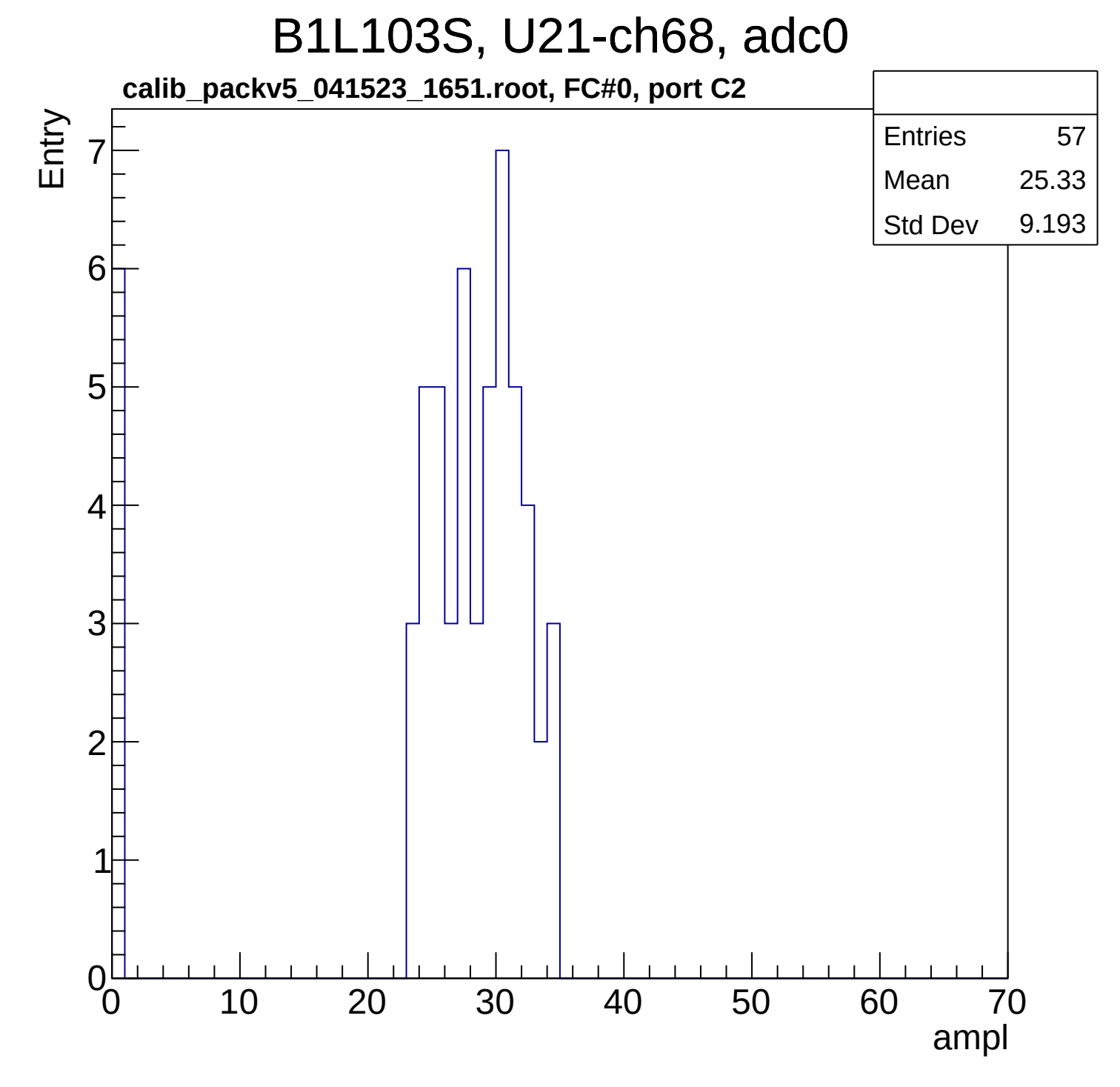
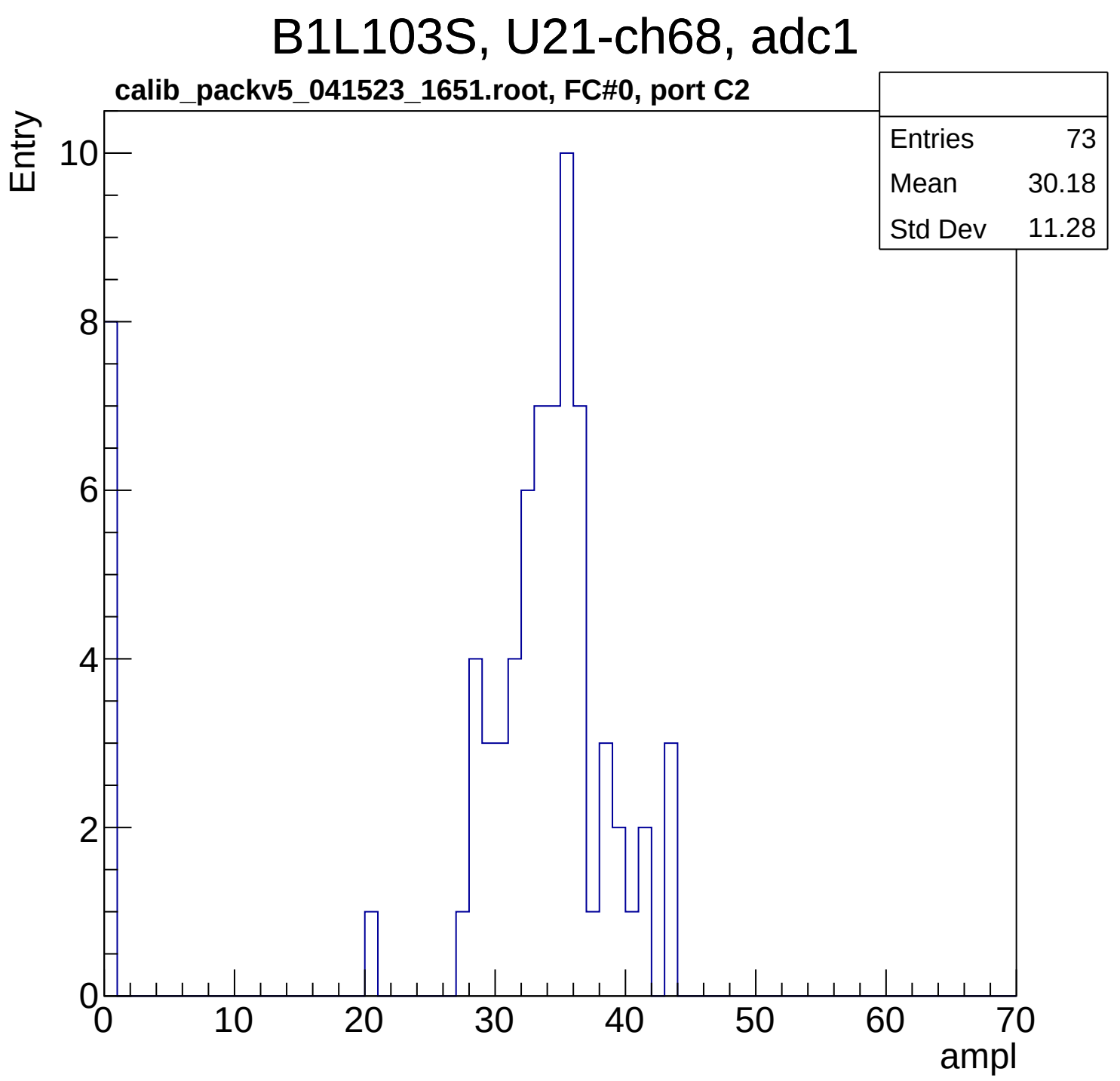
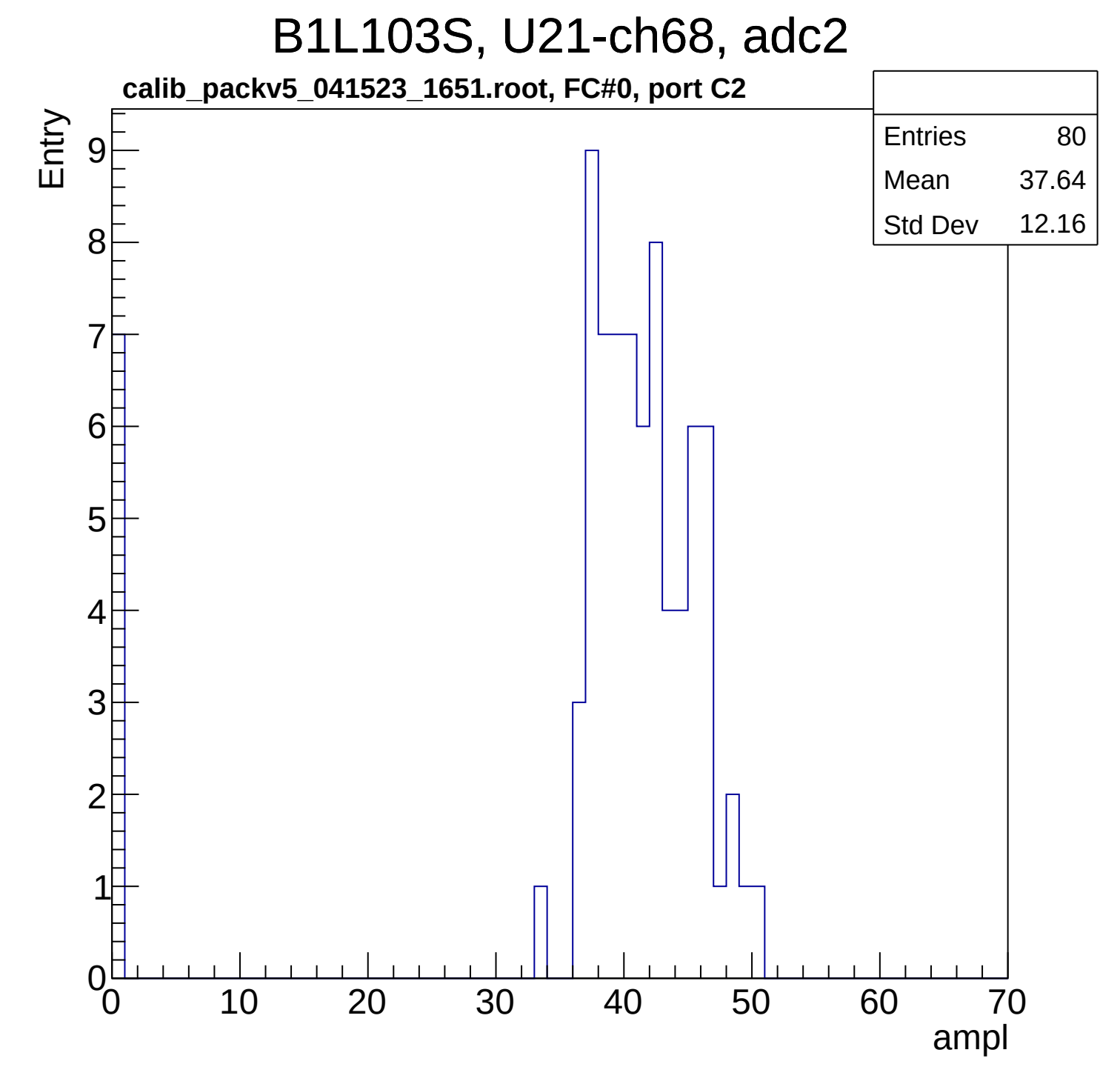
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U21-ch67, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4.25
Std Dev 14.3
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch68, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 25.33
Std Dev 9.193
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U21-ch68, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 30.18
Std Dev 11.28
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U21-ch68, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 37.64
Std Dev 12.16
Entry
ampl
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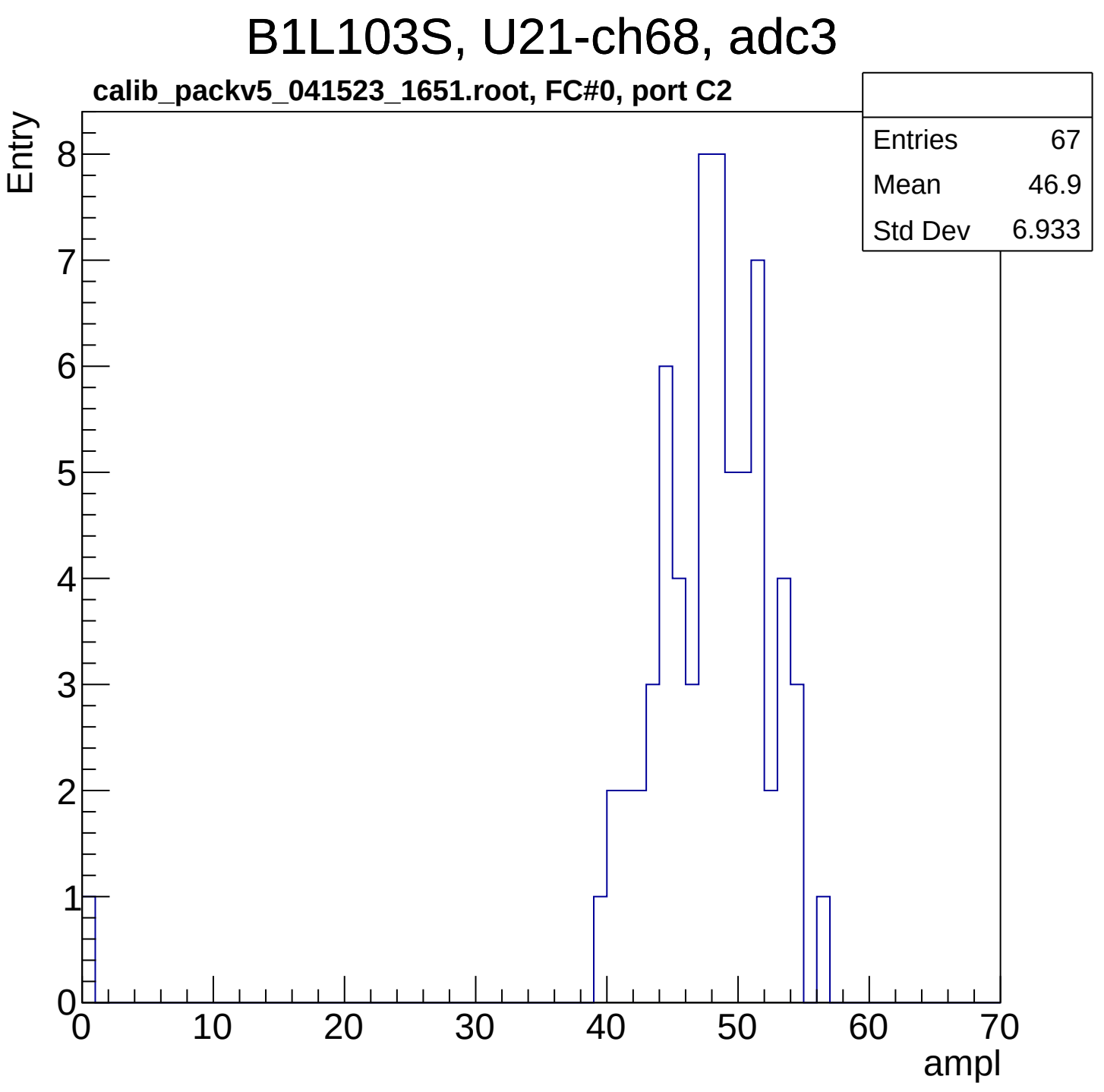
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch68, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 46.9
Std Dev 6.933
Entry
ampl
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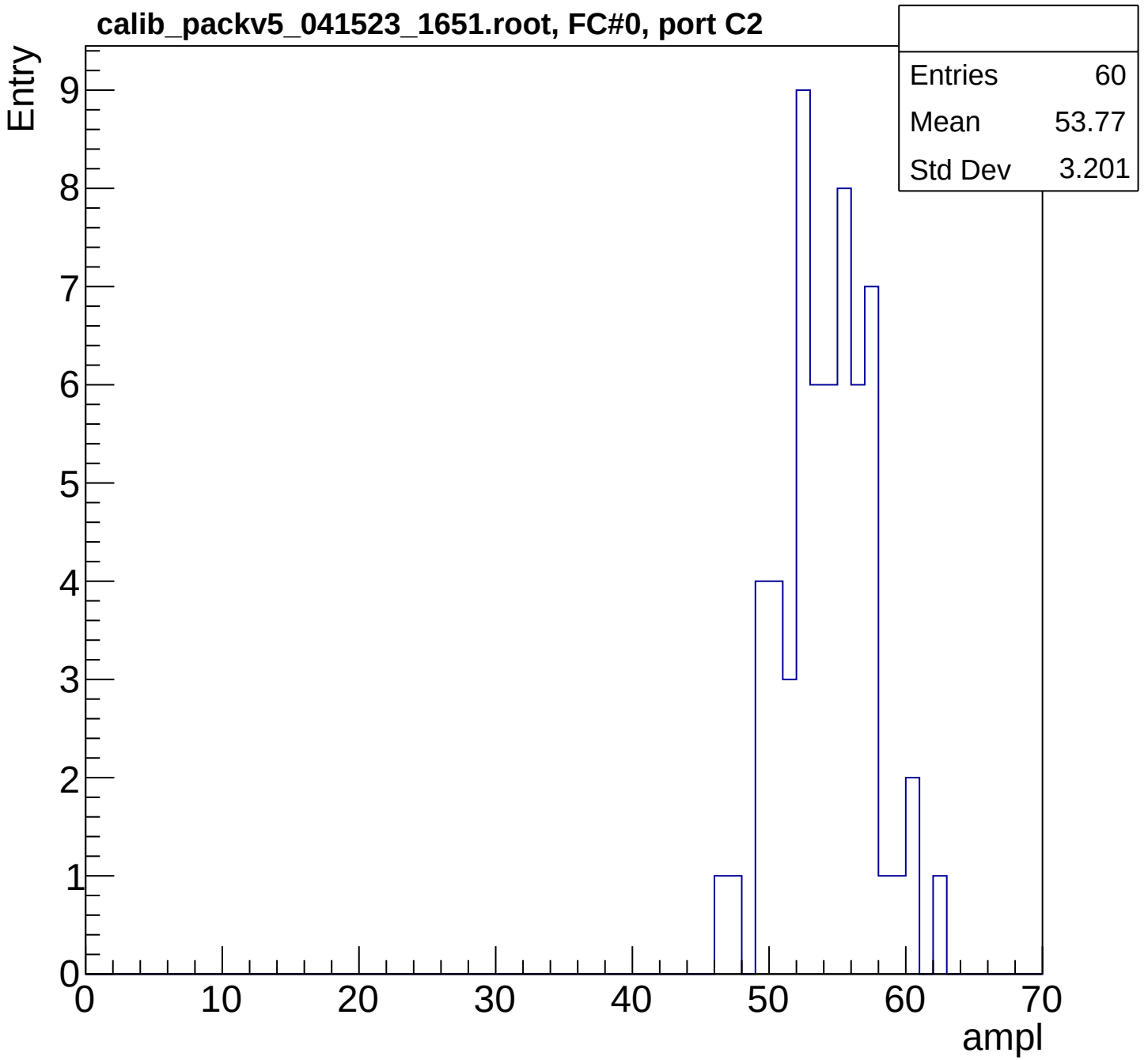
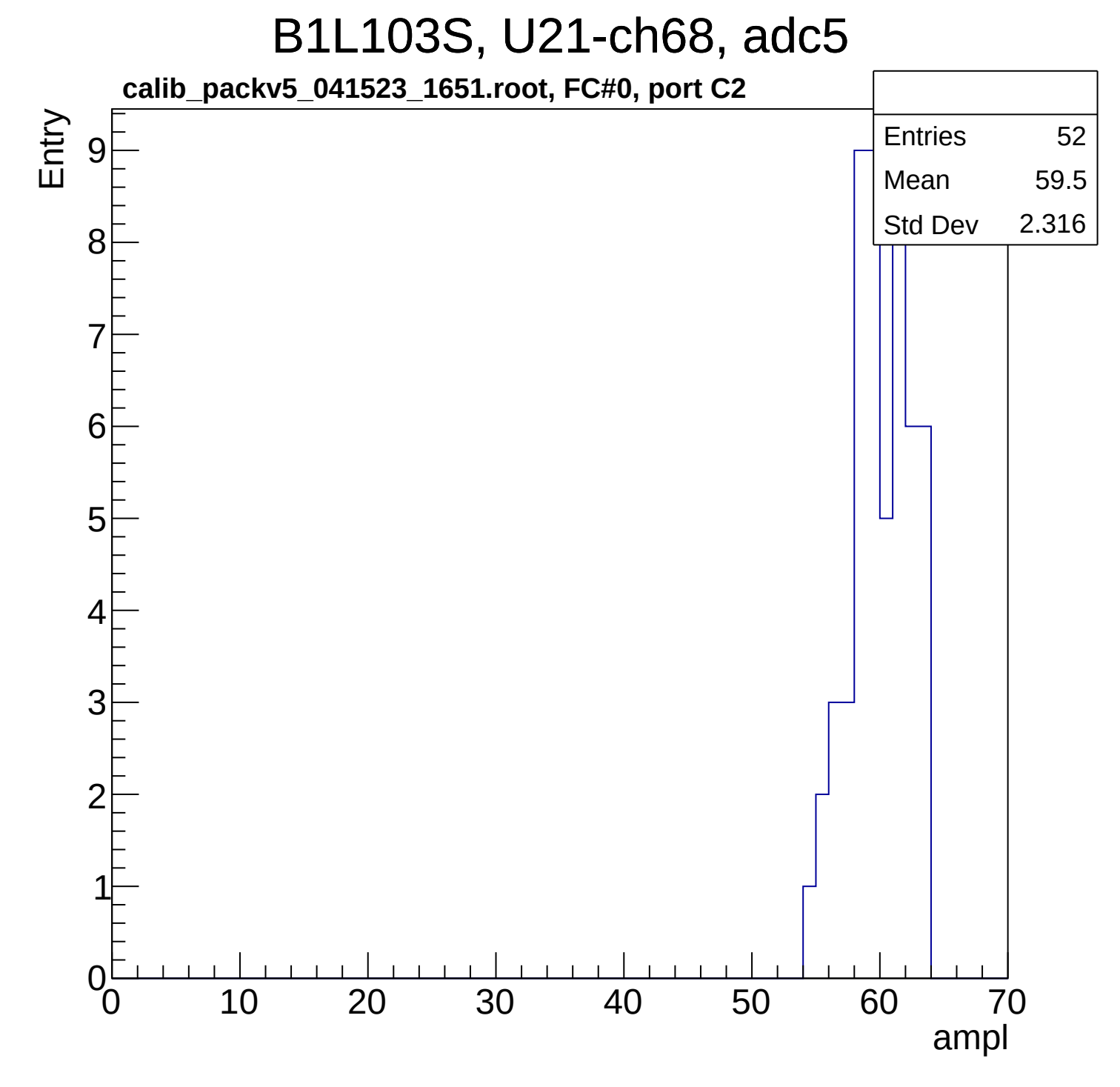
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch68, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 53.77
Std Dev 3.201
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch68, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 59.5
Std Dev 2.316
Entry
ampl
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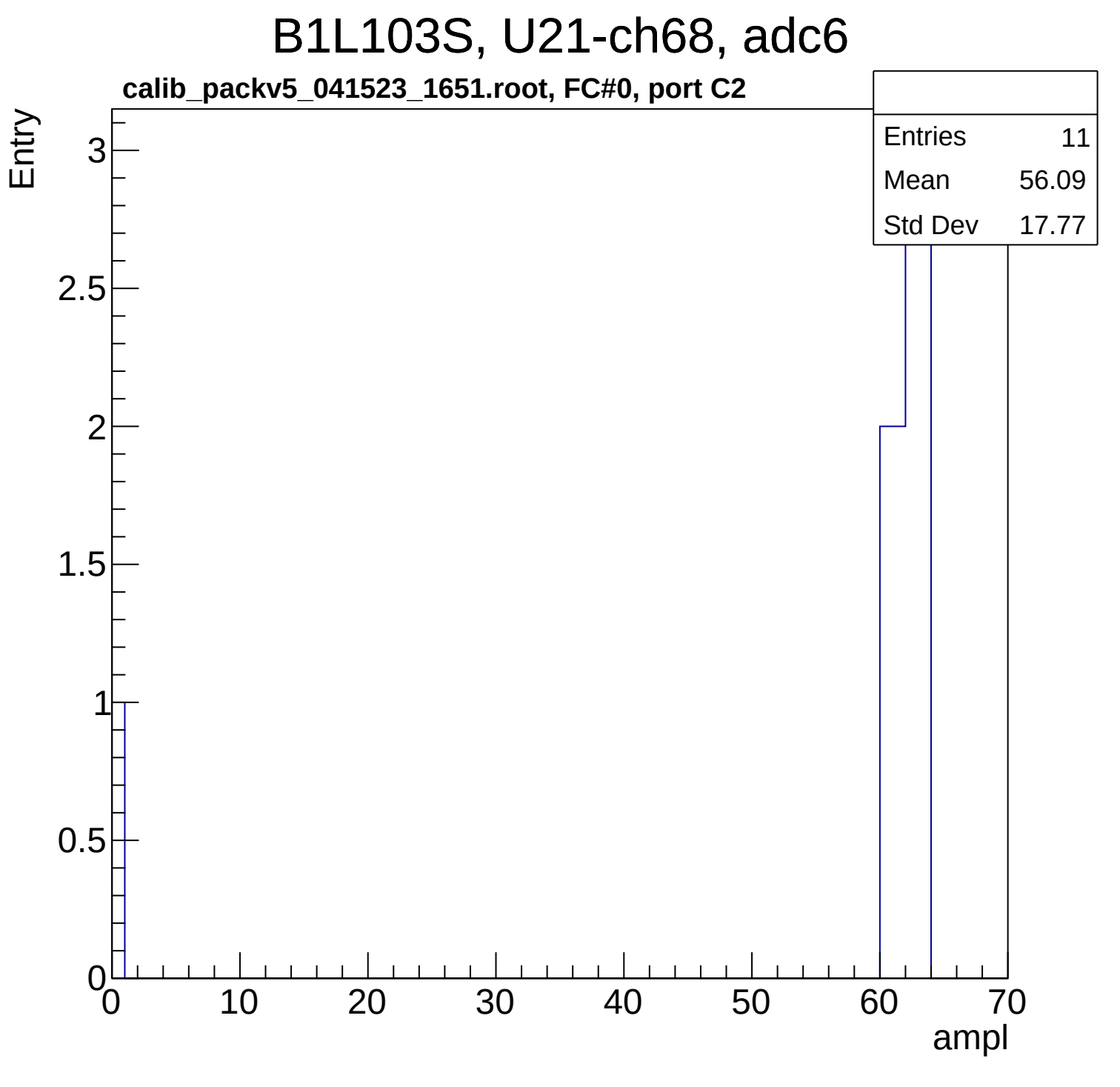
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch68, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 56.09
Std Dev 17.77
Entry
ampl
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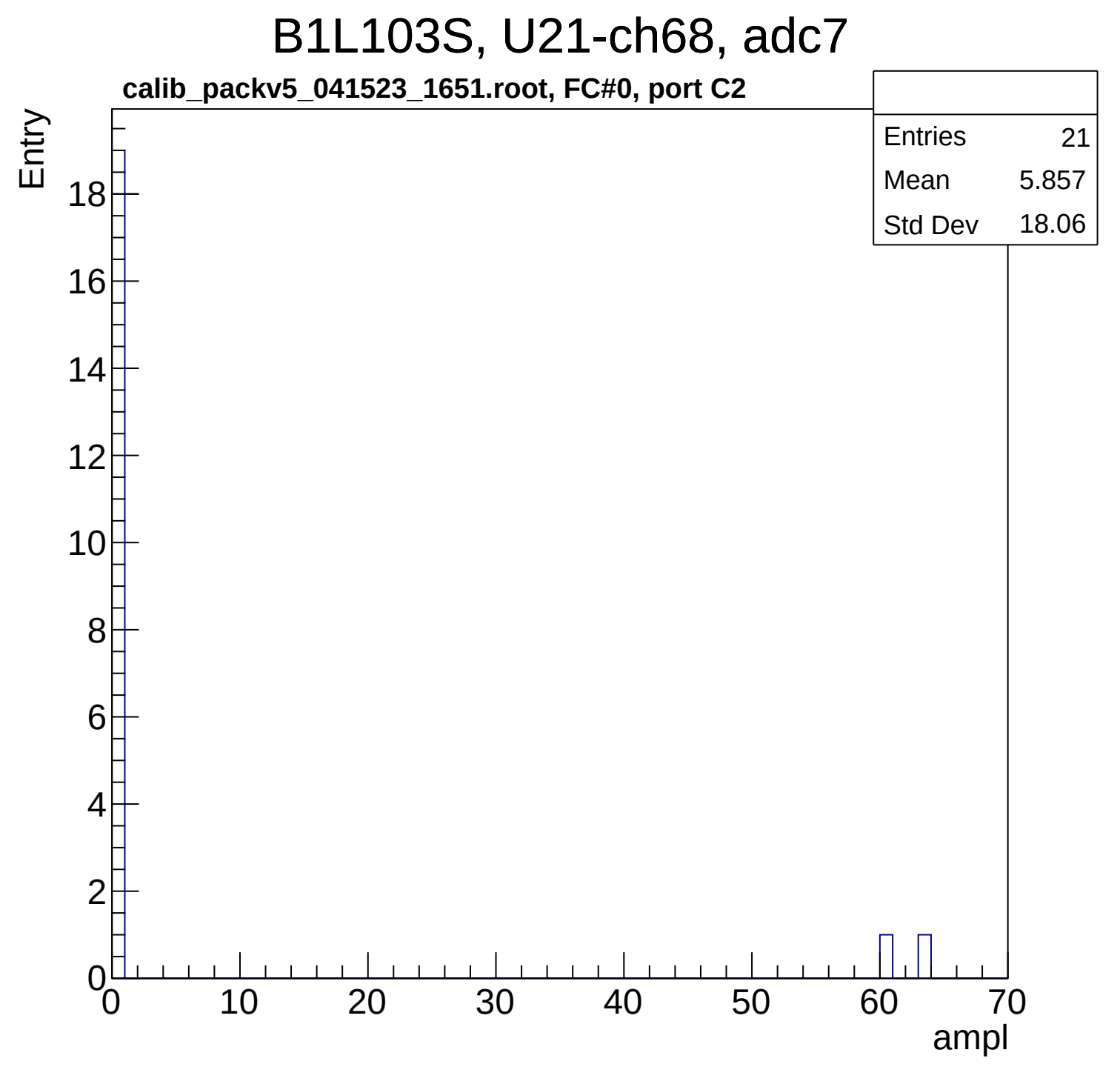
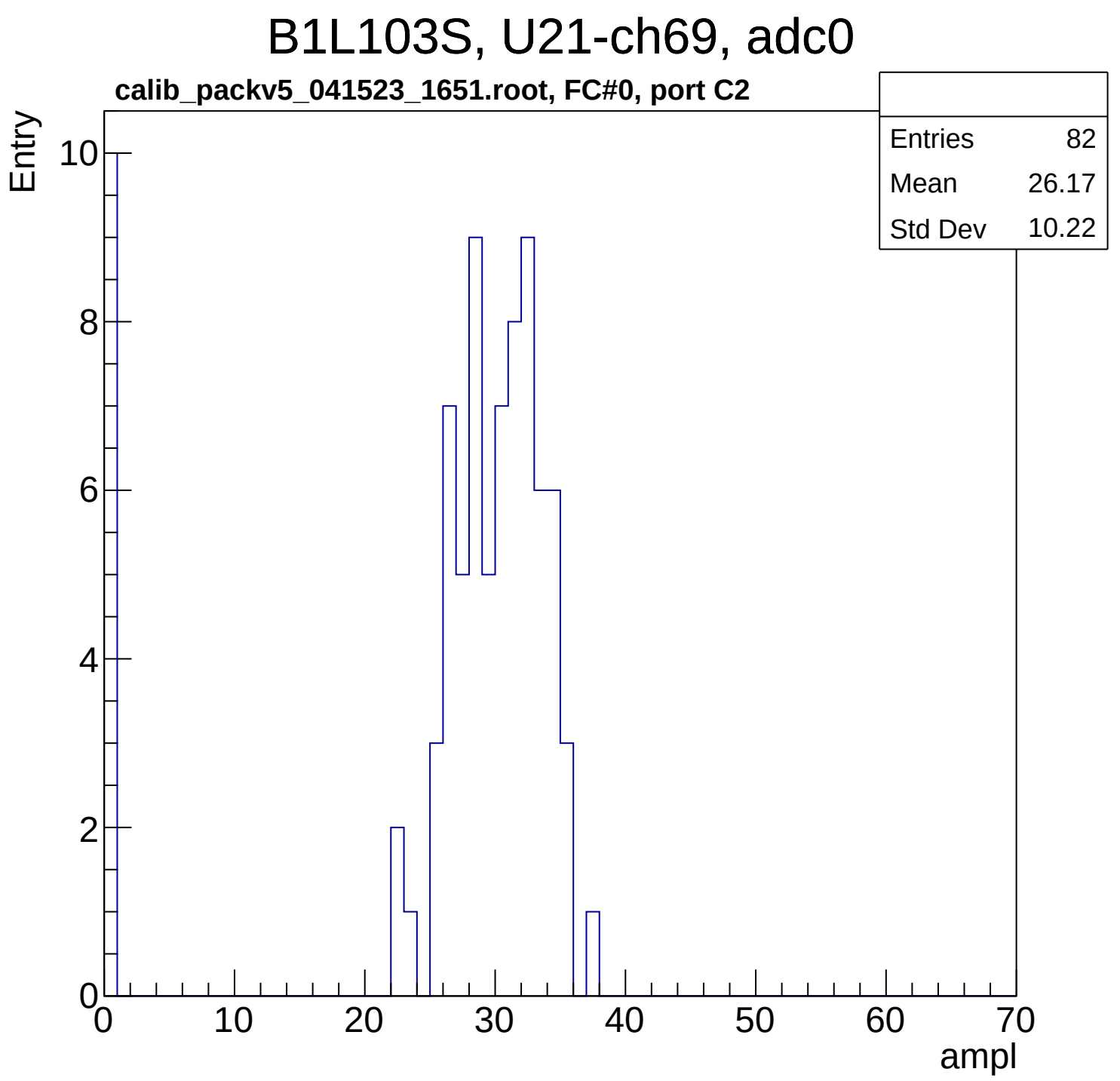
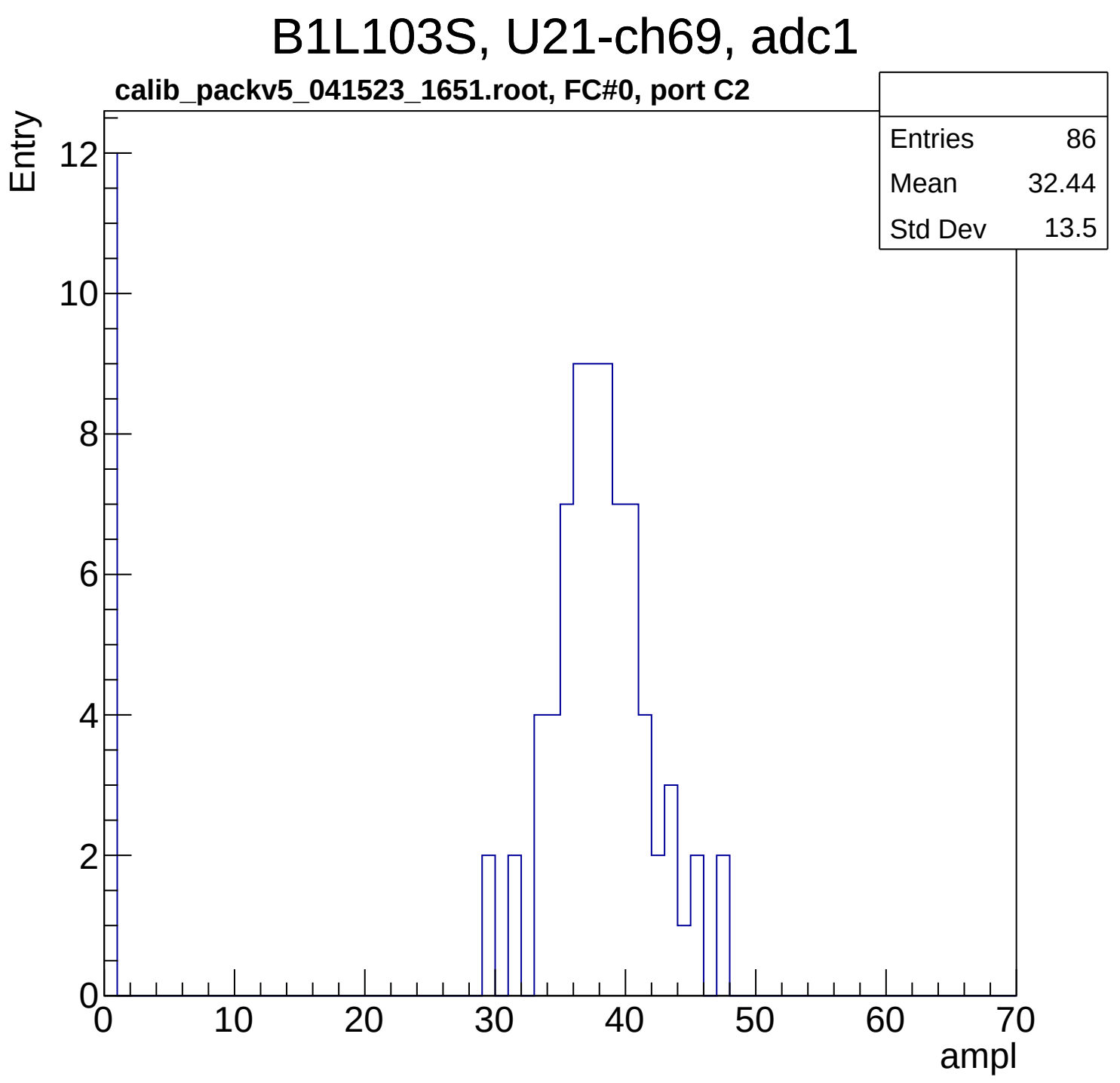
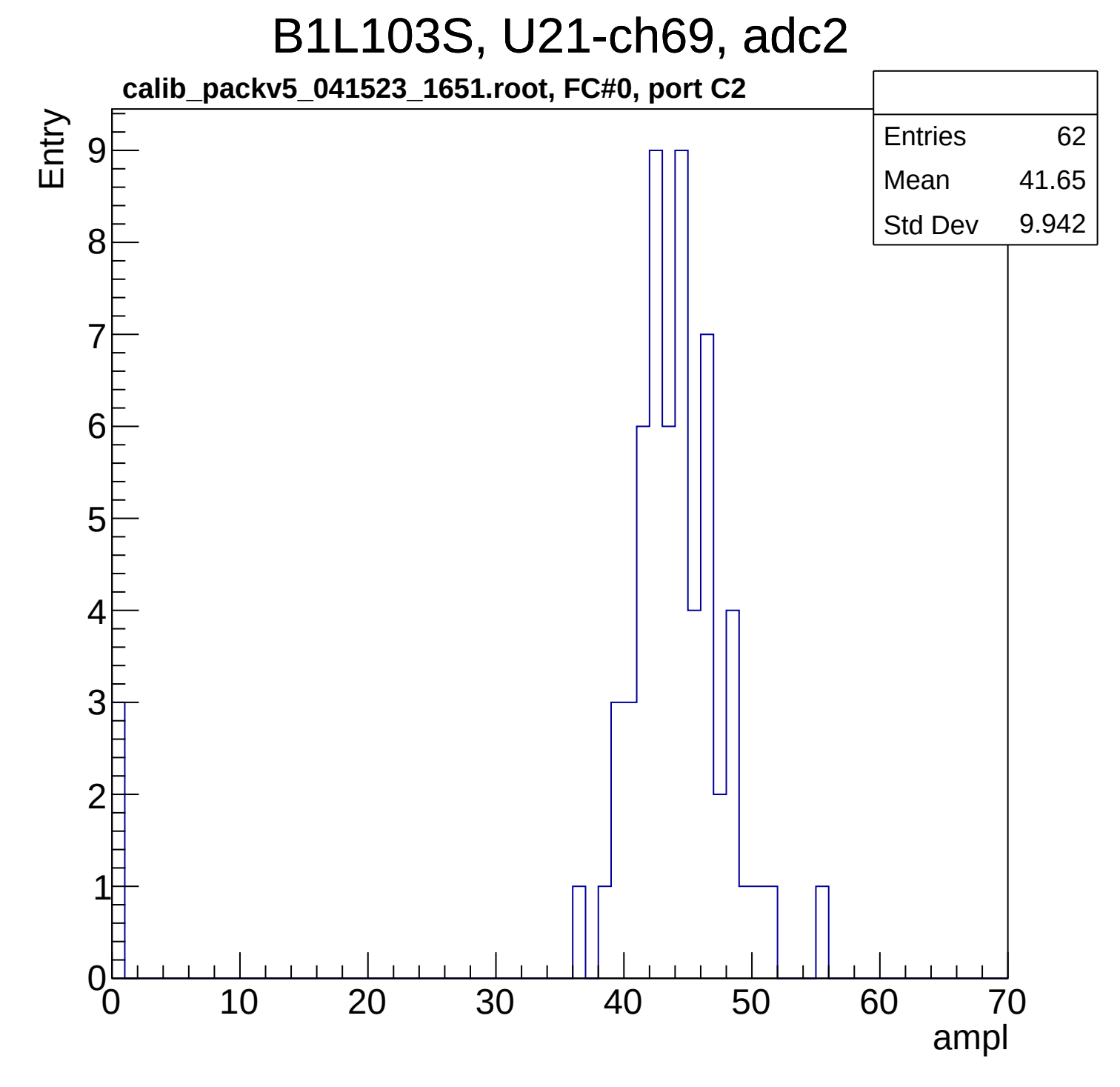
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U21-ch68, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.857
Std Dev 18.06
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch69, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 26.17
Std Dev 10.22
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch69, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 32.44
Std Dev 13.5
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch69, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 41.65
Std Dev 9.942
Entry
ampl
0
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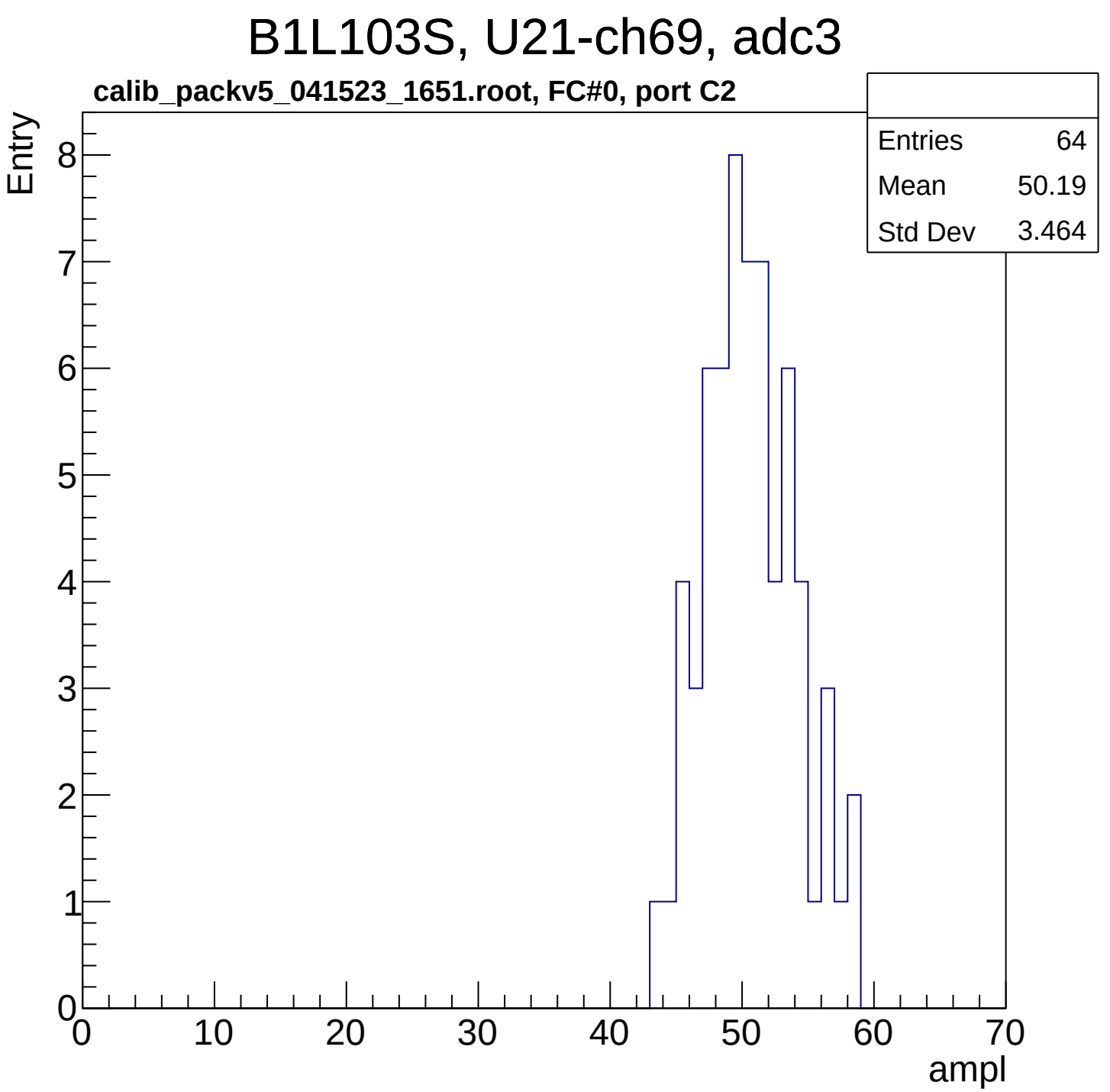
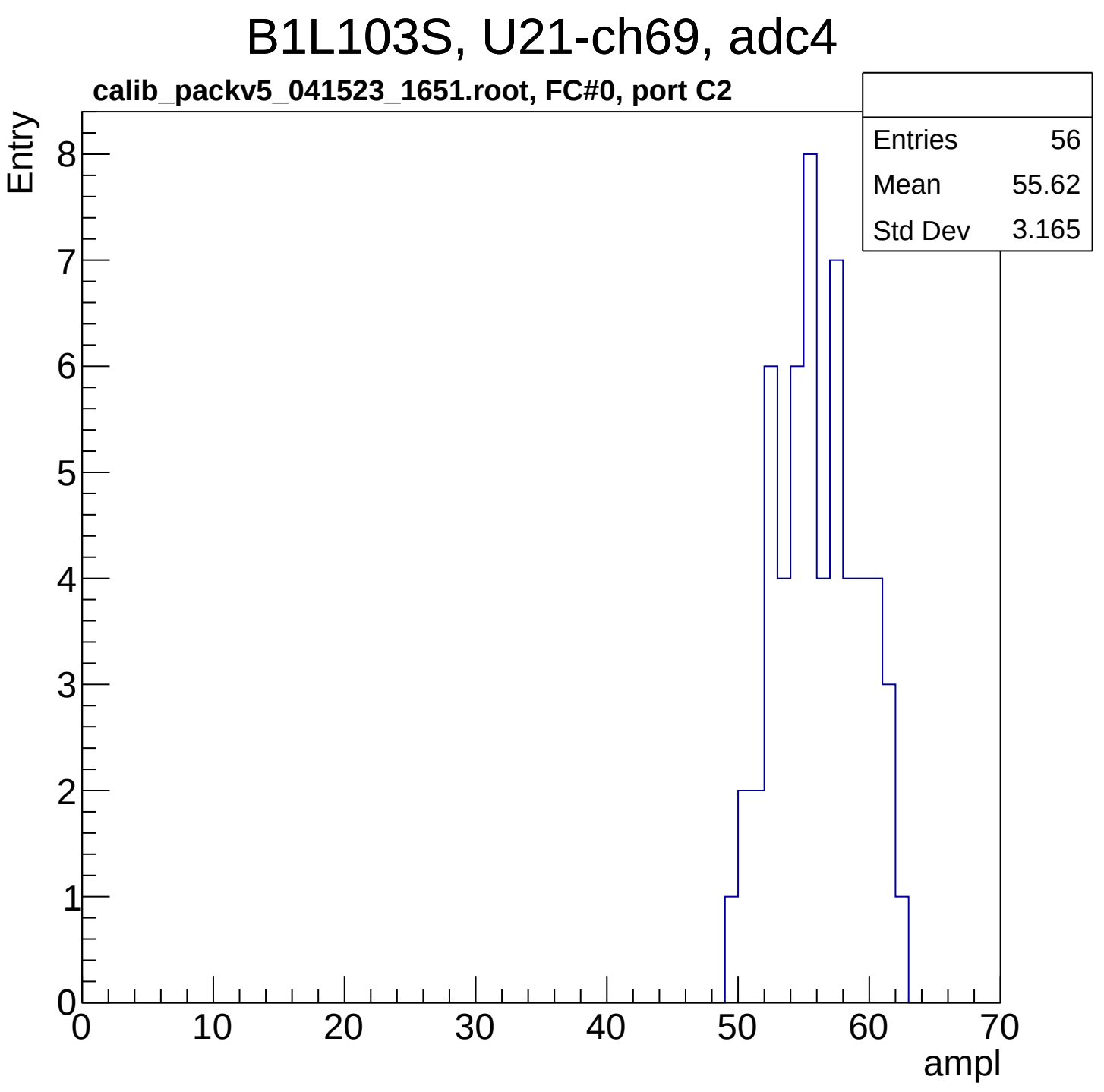
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch69, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 50.19
Std Dev 3.464
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch69, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 55.62
Std Dev 3.165
Entry
0
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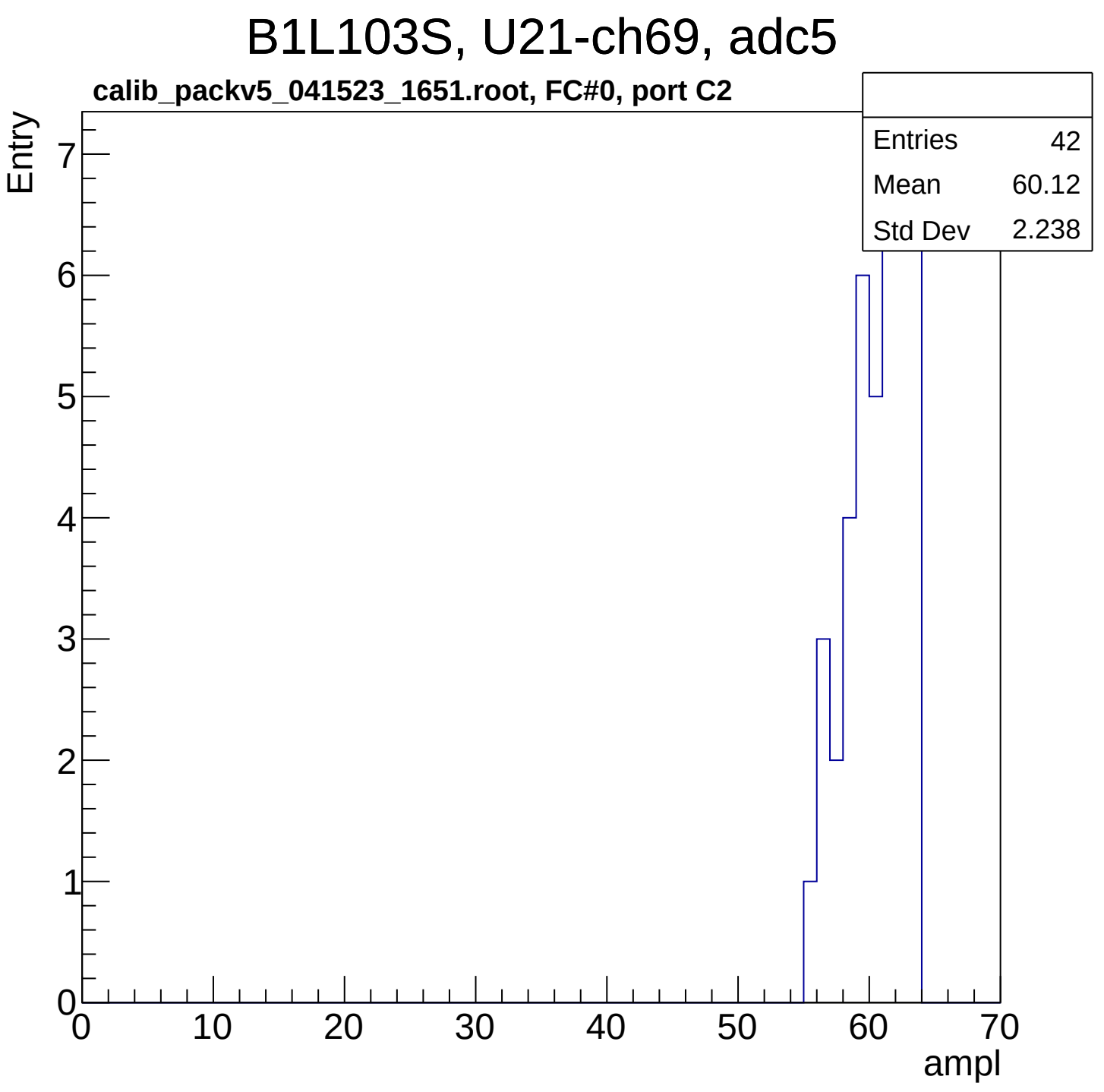
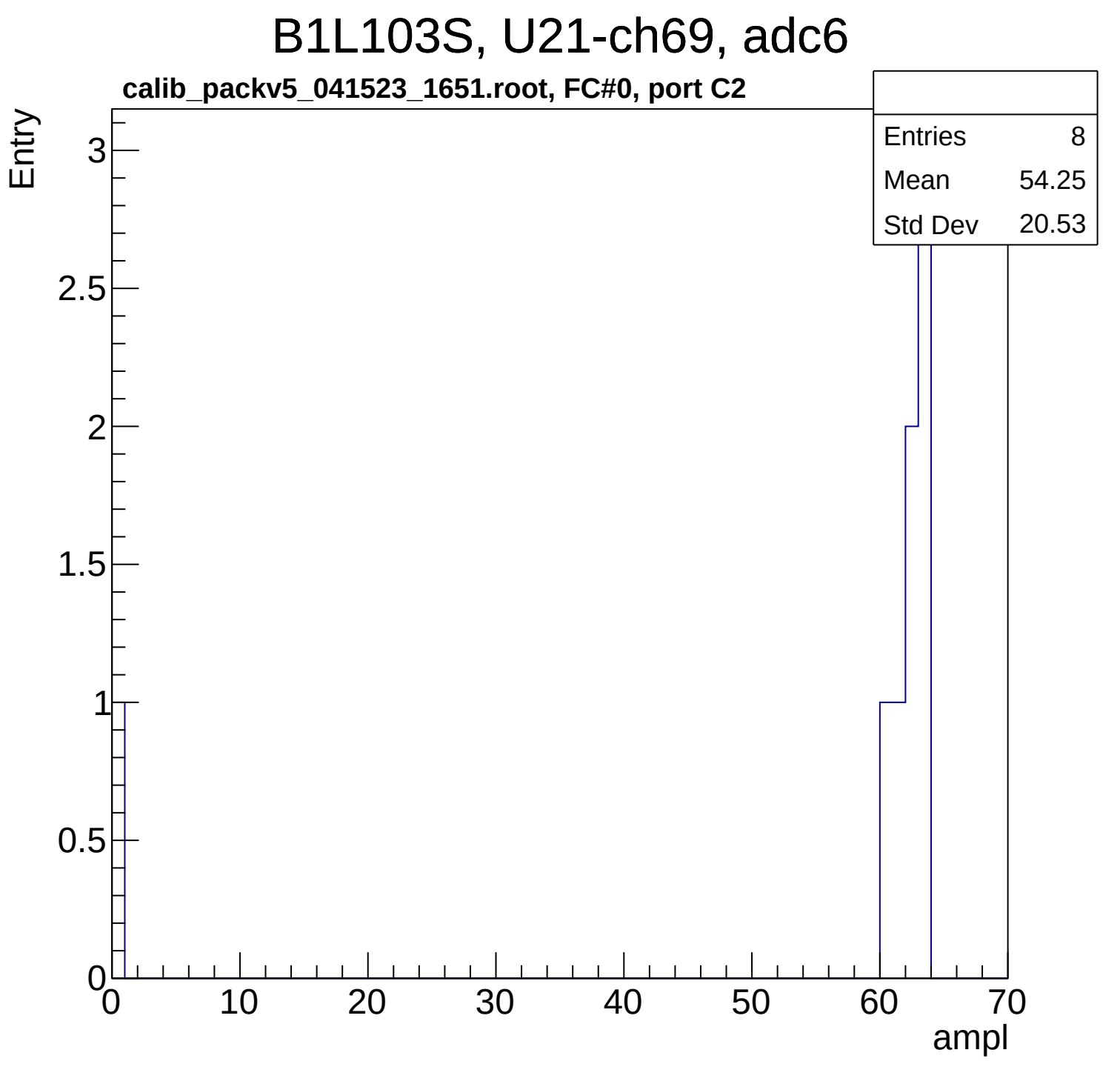
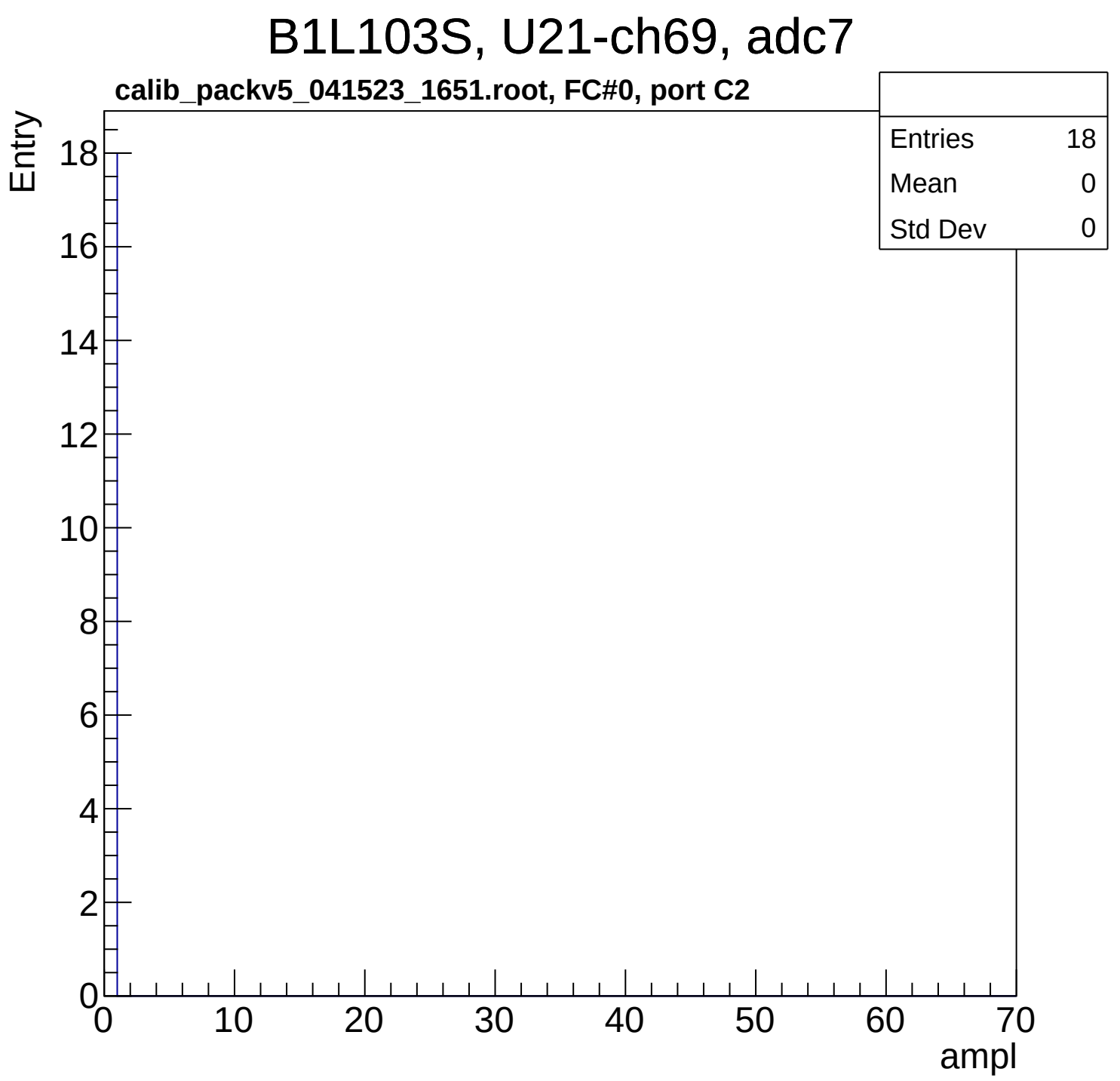
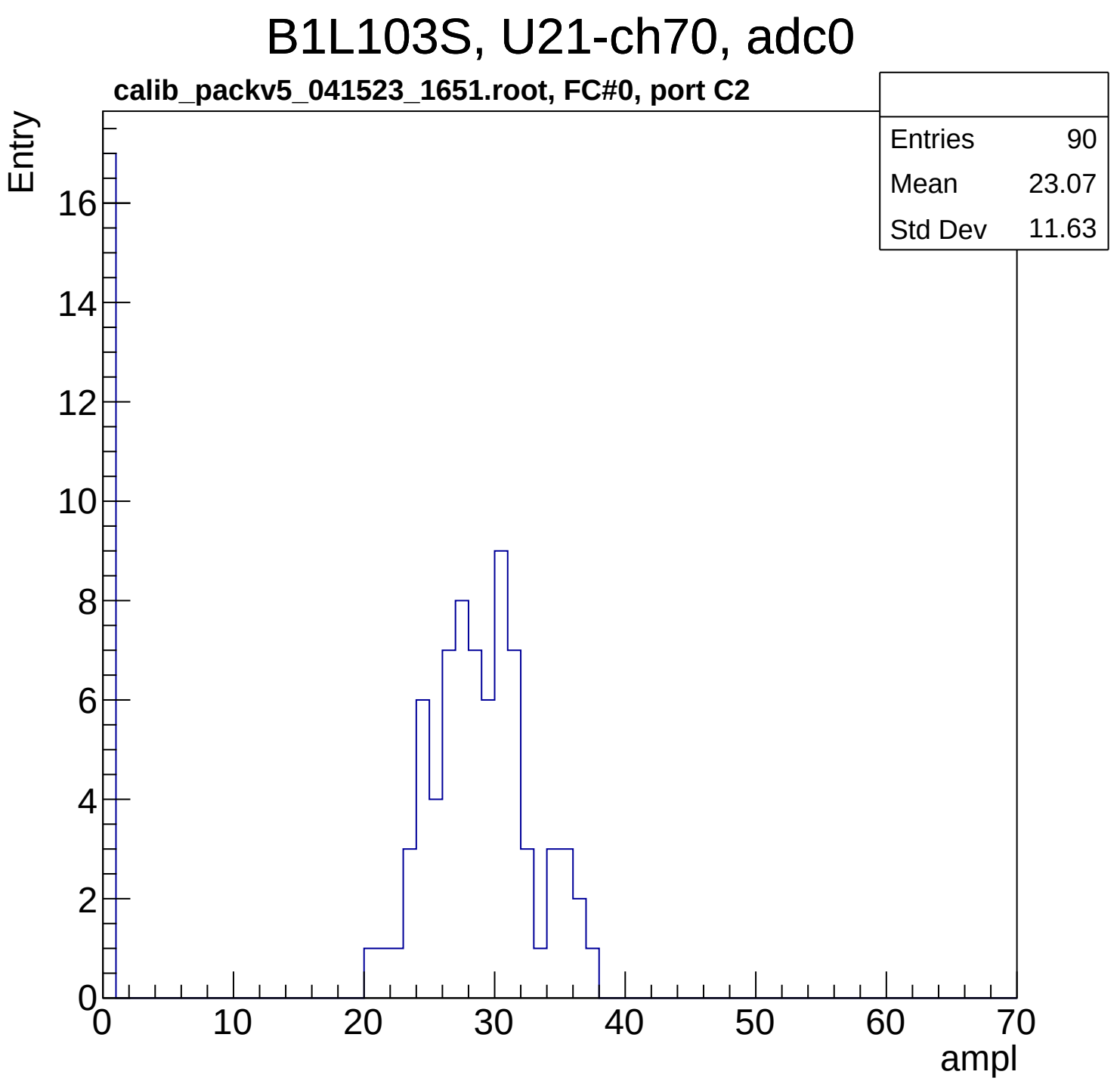
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch69, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 60.12
Std Dev 2.238
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch69, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 54.25
Std Dev 20.53
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U21-ch69, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch70, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 23.07
Std Dev 11.63
Entry
0
2
4
6
8
10
12
14
16
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10
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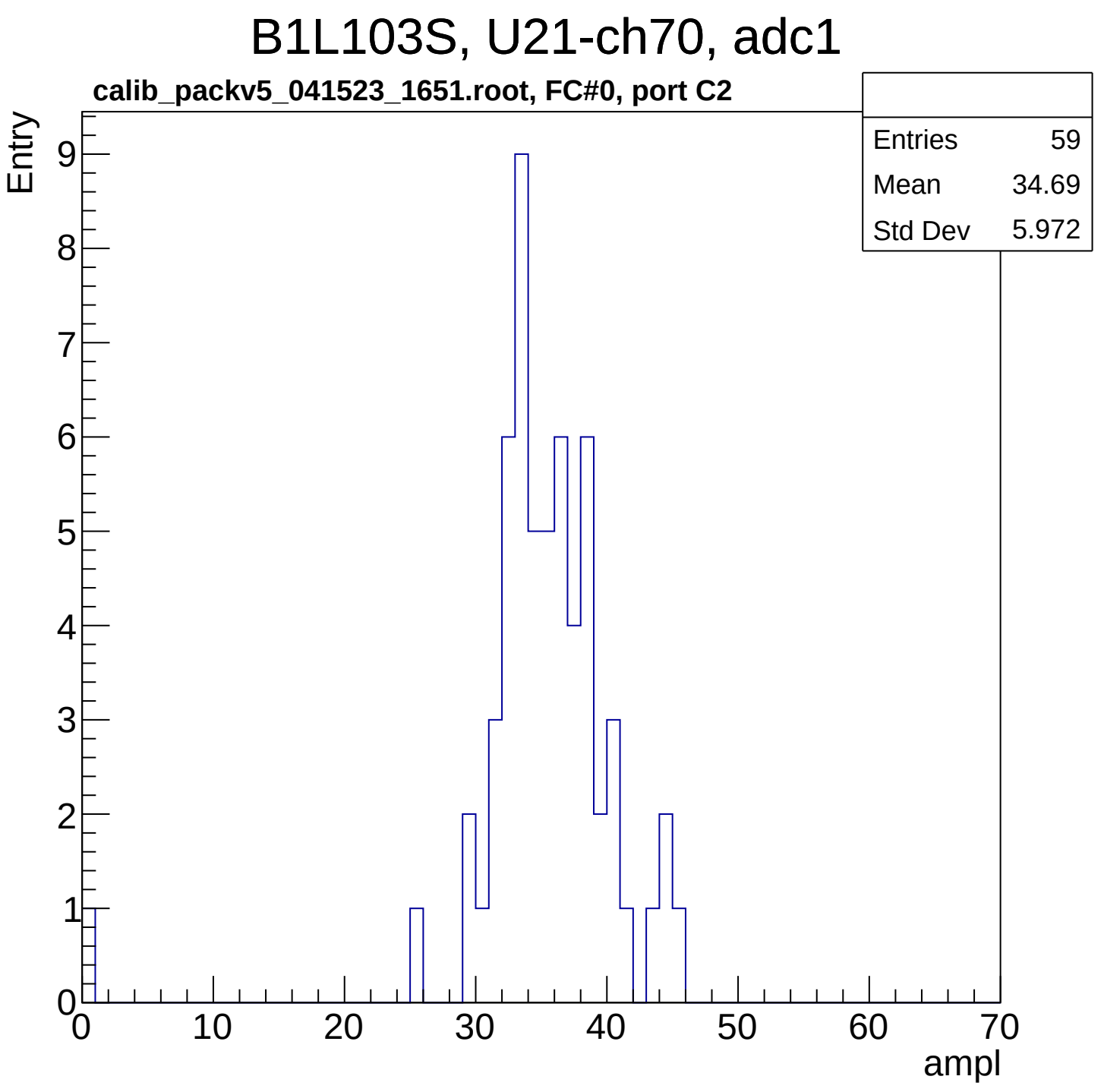
70
ampl


B1L103S, U21-ch70, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 34.69
Std Dev 5.972
Entry
ampl
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2
3
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5
6
7
8
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0
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60
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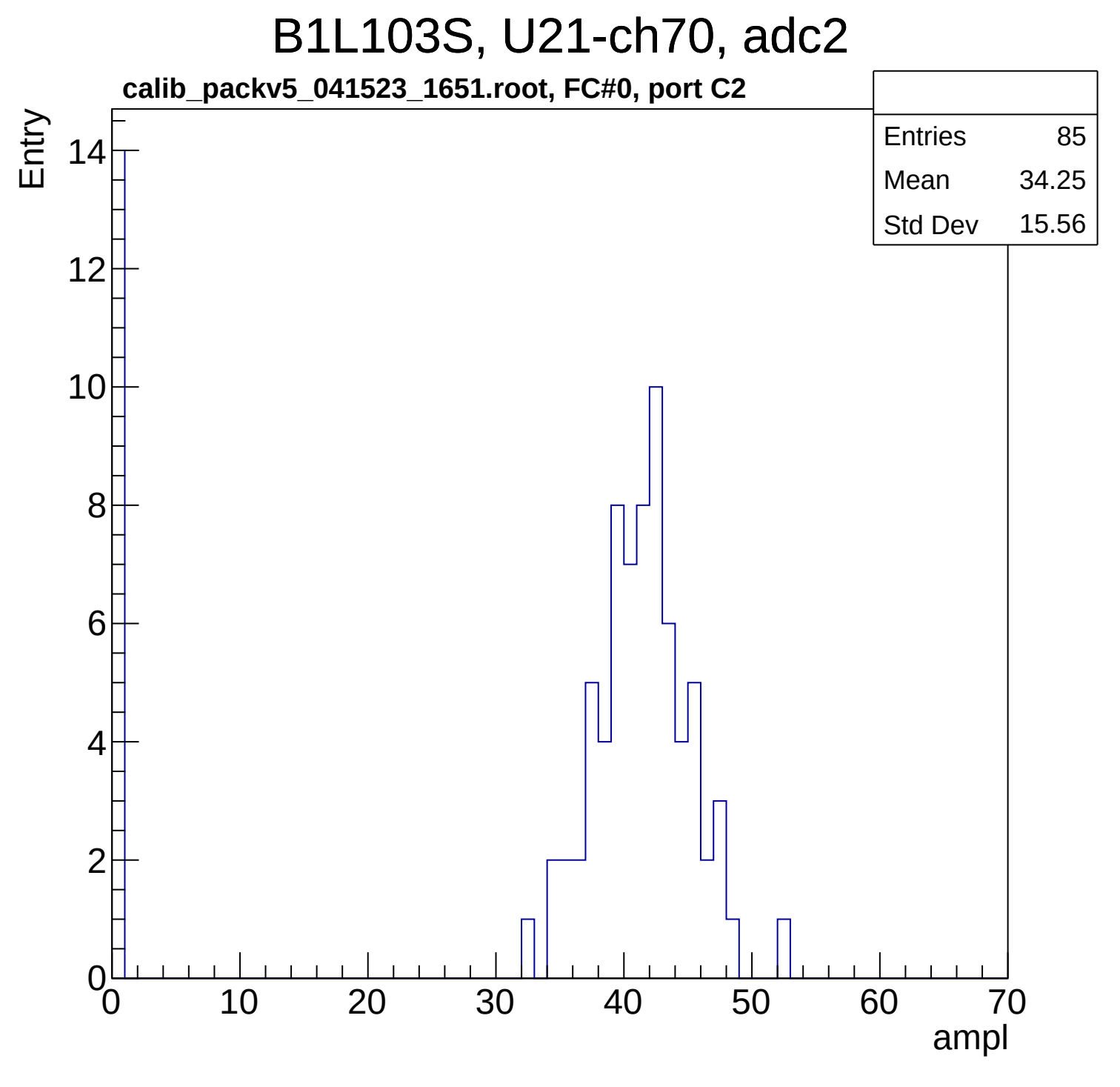
B1L103S, U21-ch70, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 34.25
Std Dev 15.56
Entry
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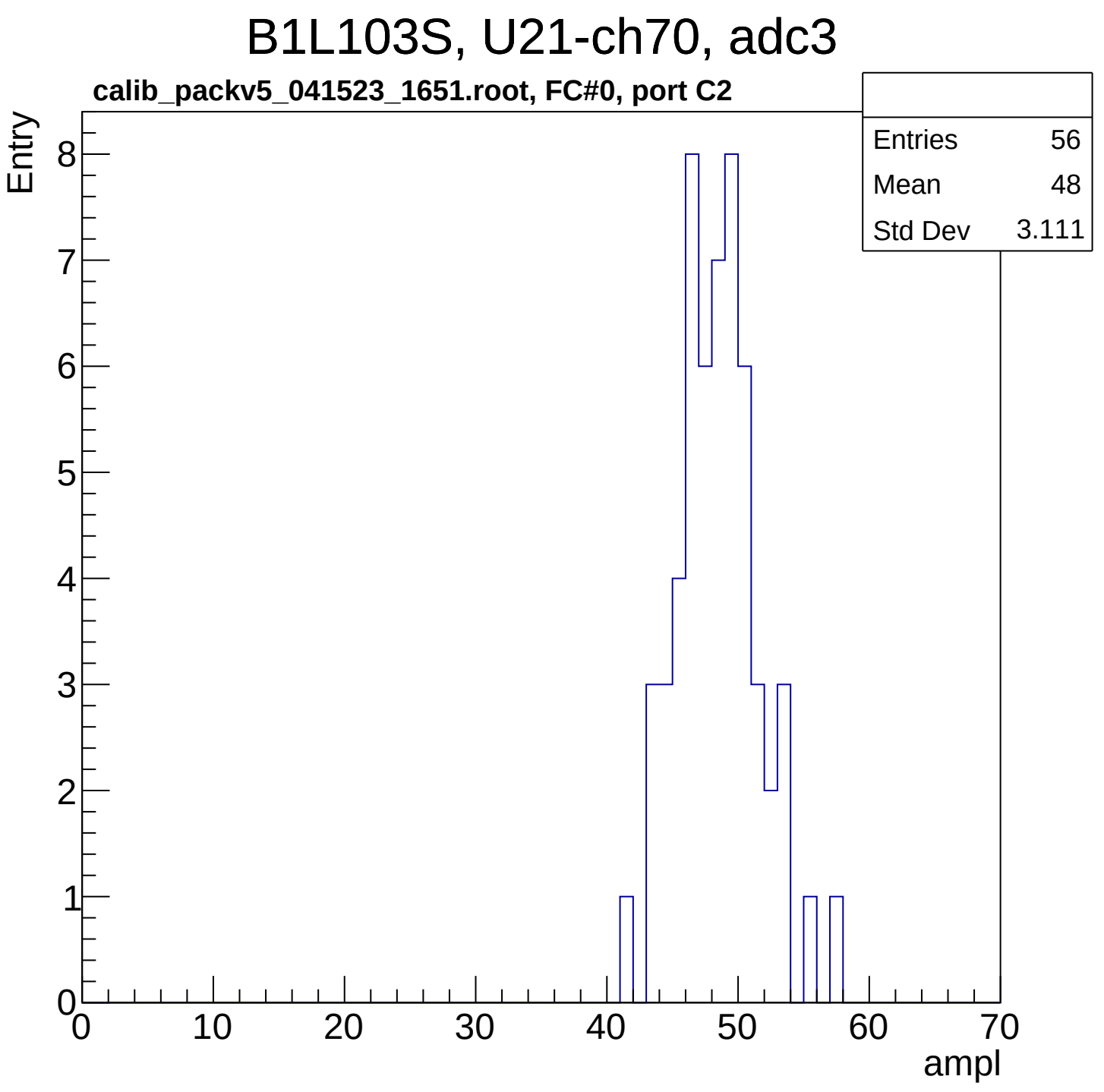
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch70, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 48
Std Dev 3.111
Entry
ampl
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2
3
4
5
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7
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0
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40
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60
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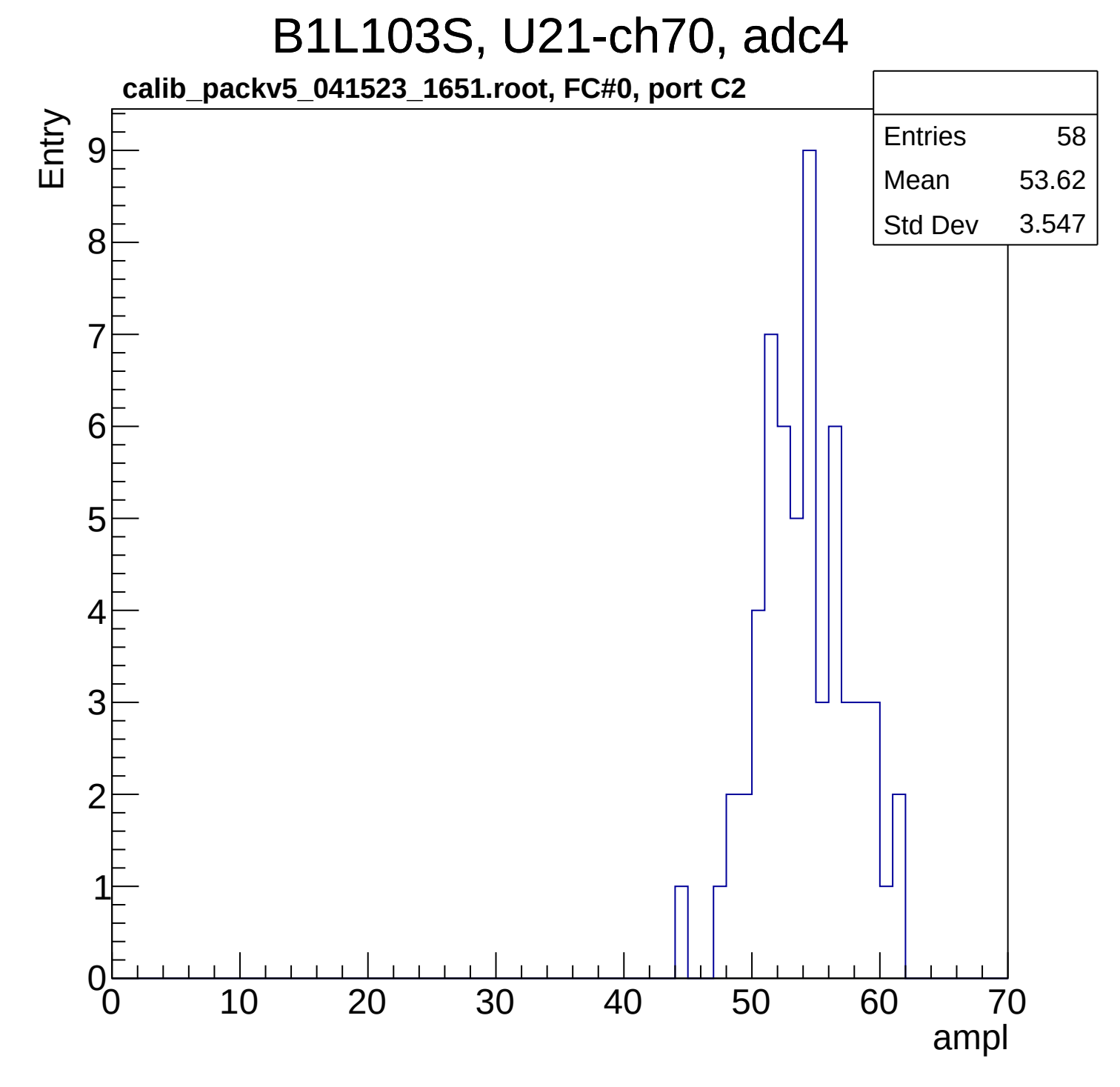
B1L103S, U21-ch70, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 53.62
Std Dev 3.547
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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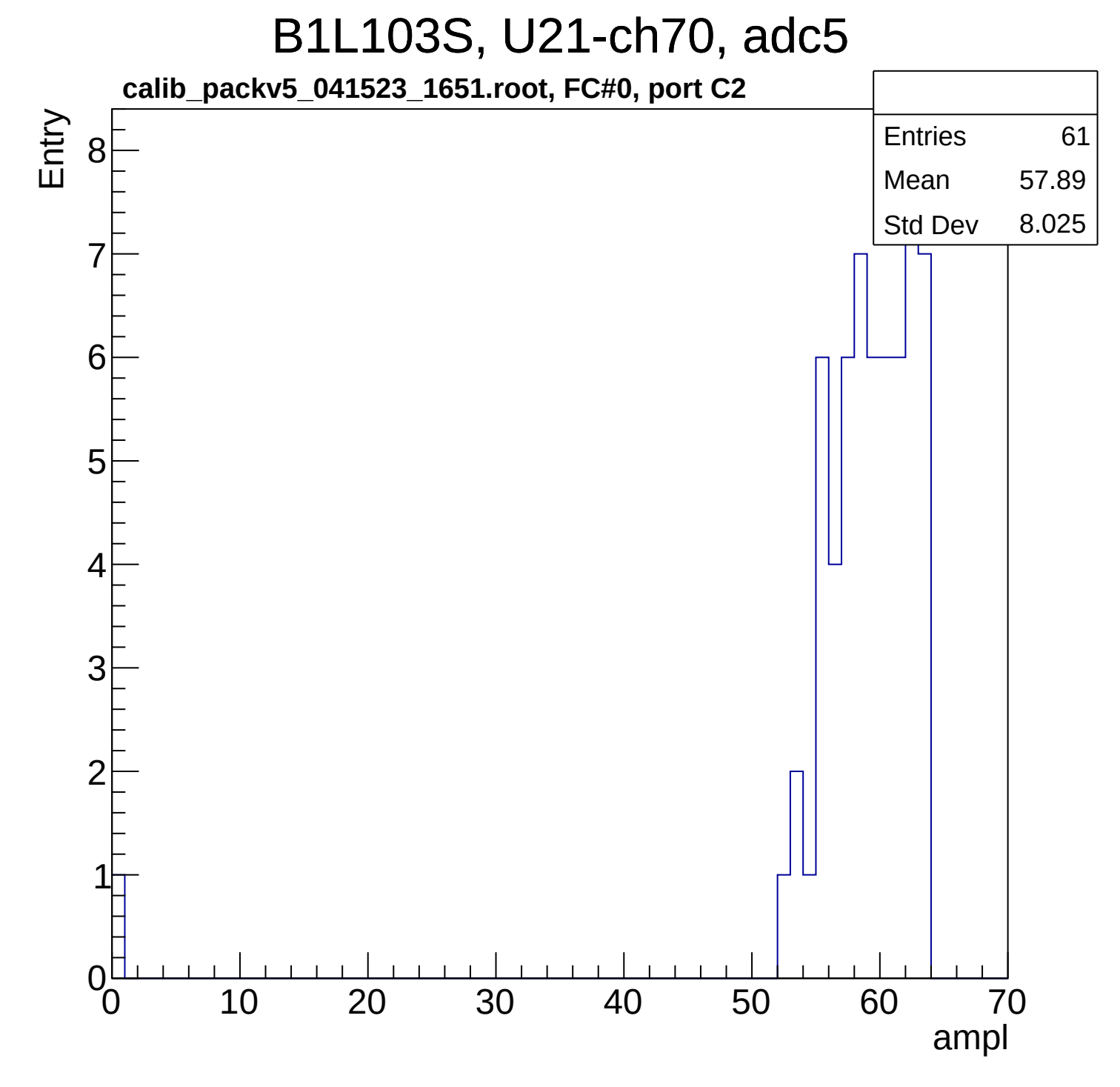
B1L103S, U21-ch70, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 57.89
Std Dev 8.025
Entry
ampl
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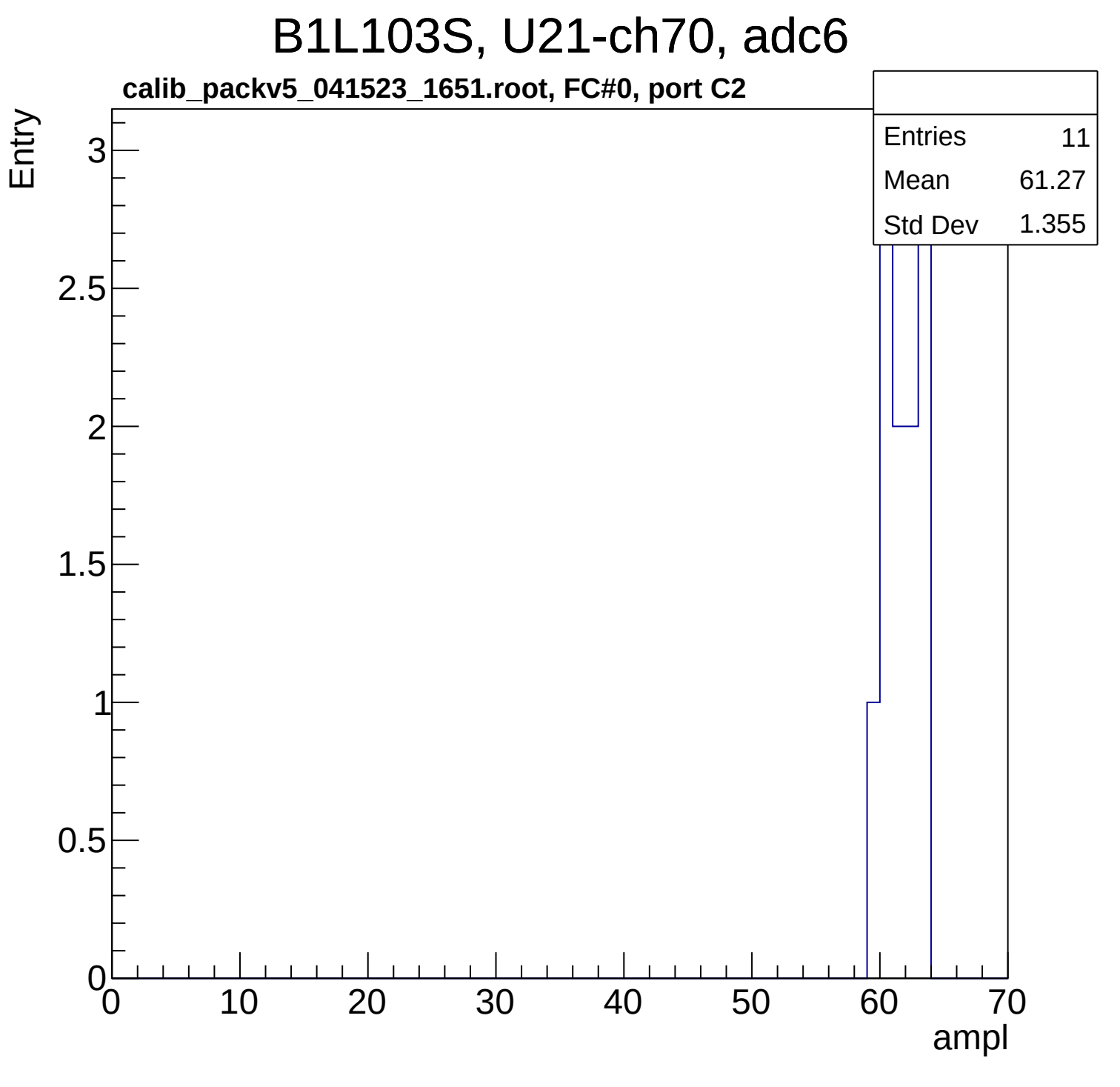
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch70, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 61.27
Std Dev 1.355
Entry
ampl
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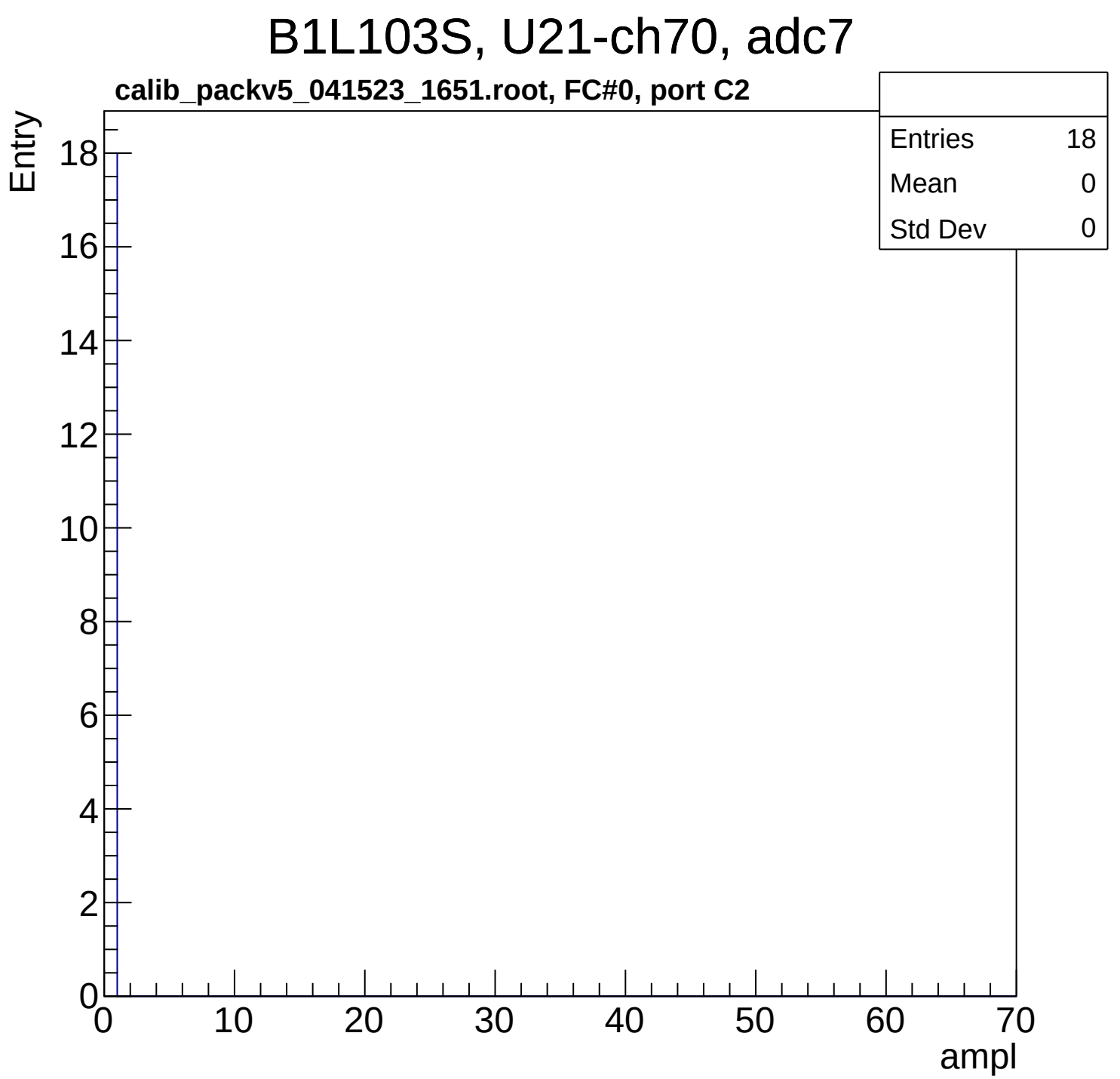
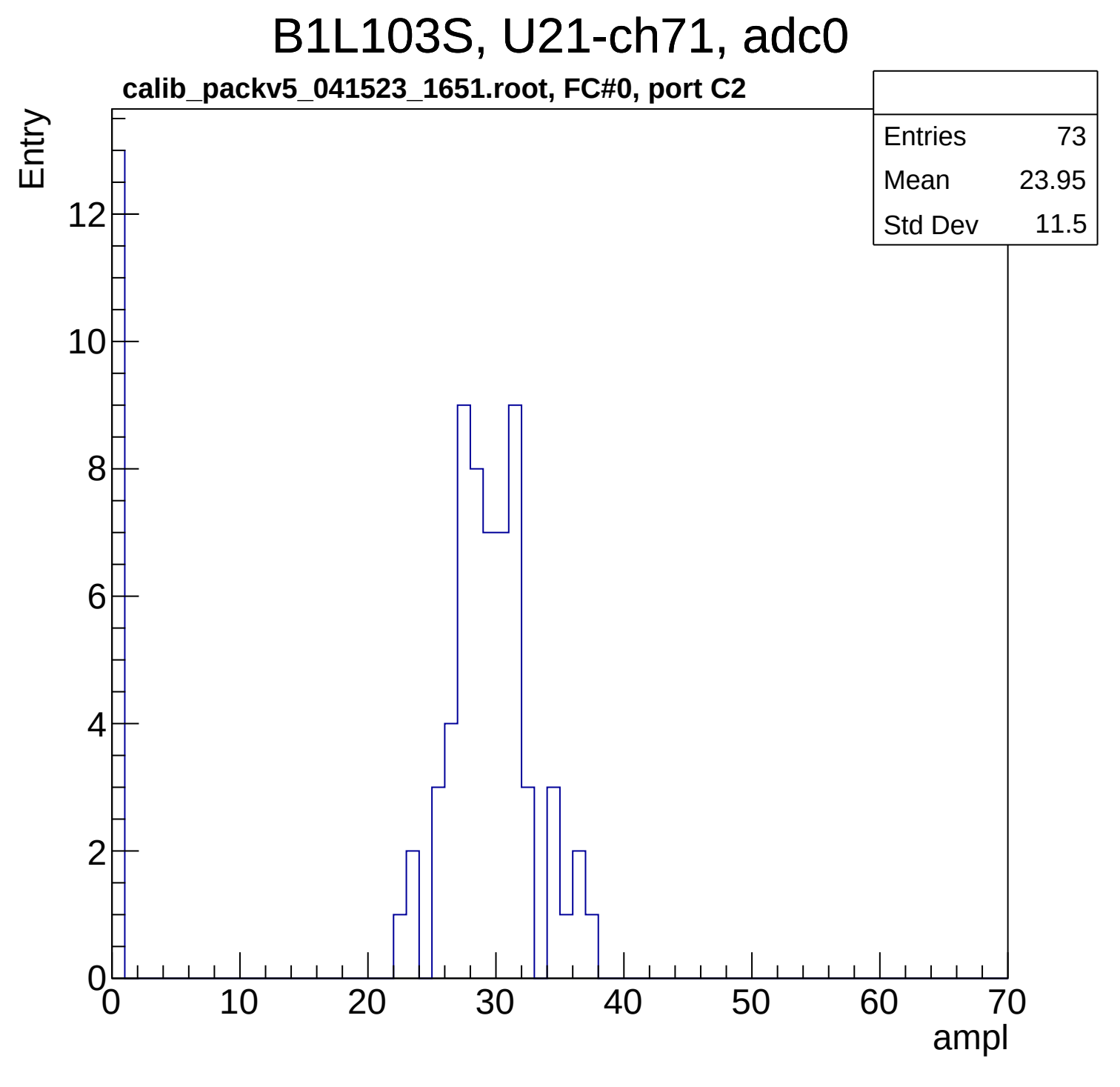
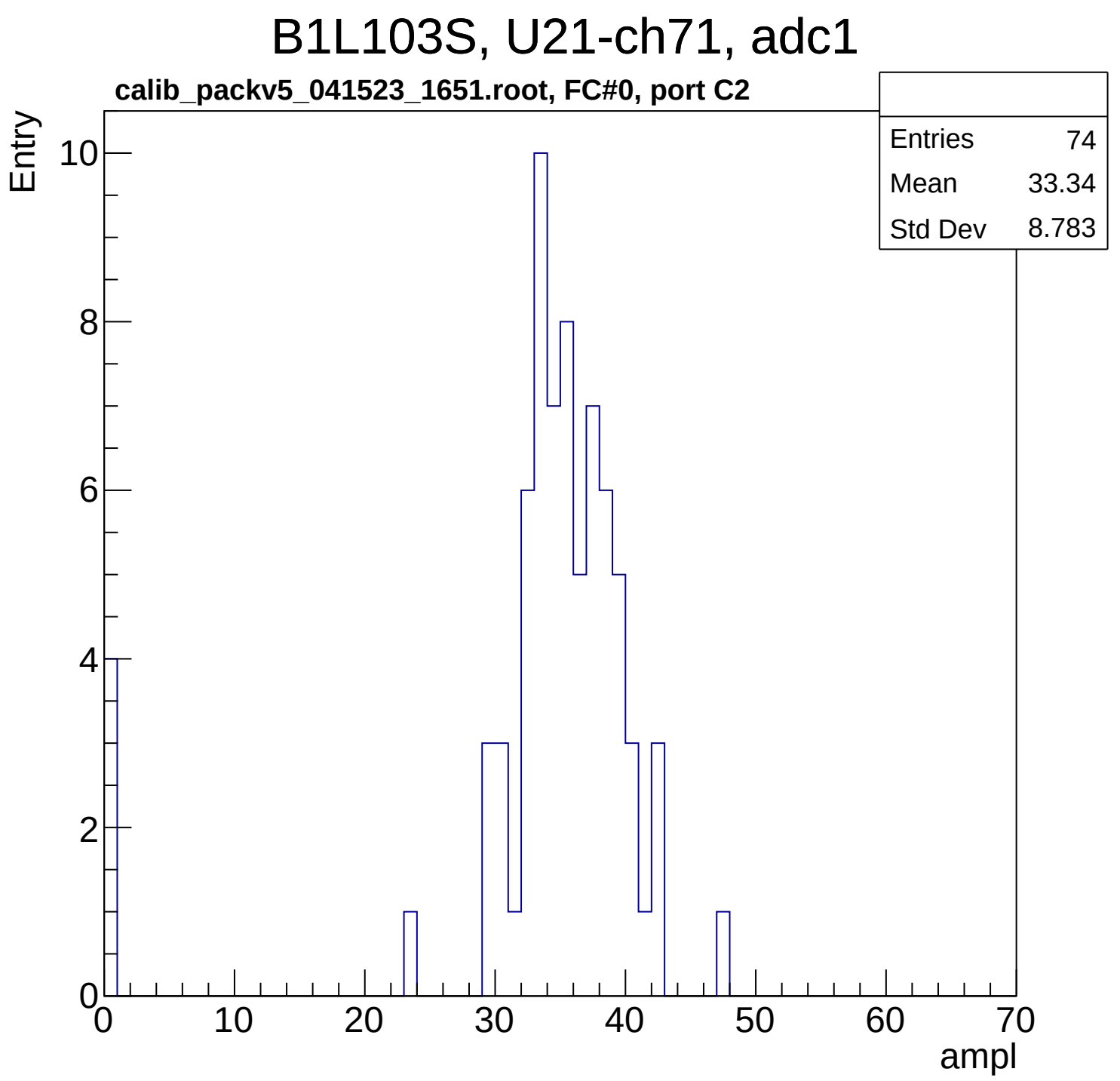
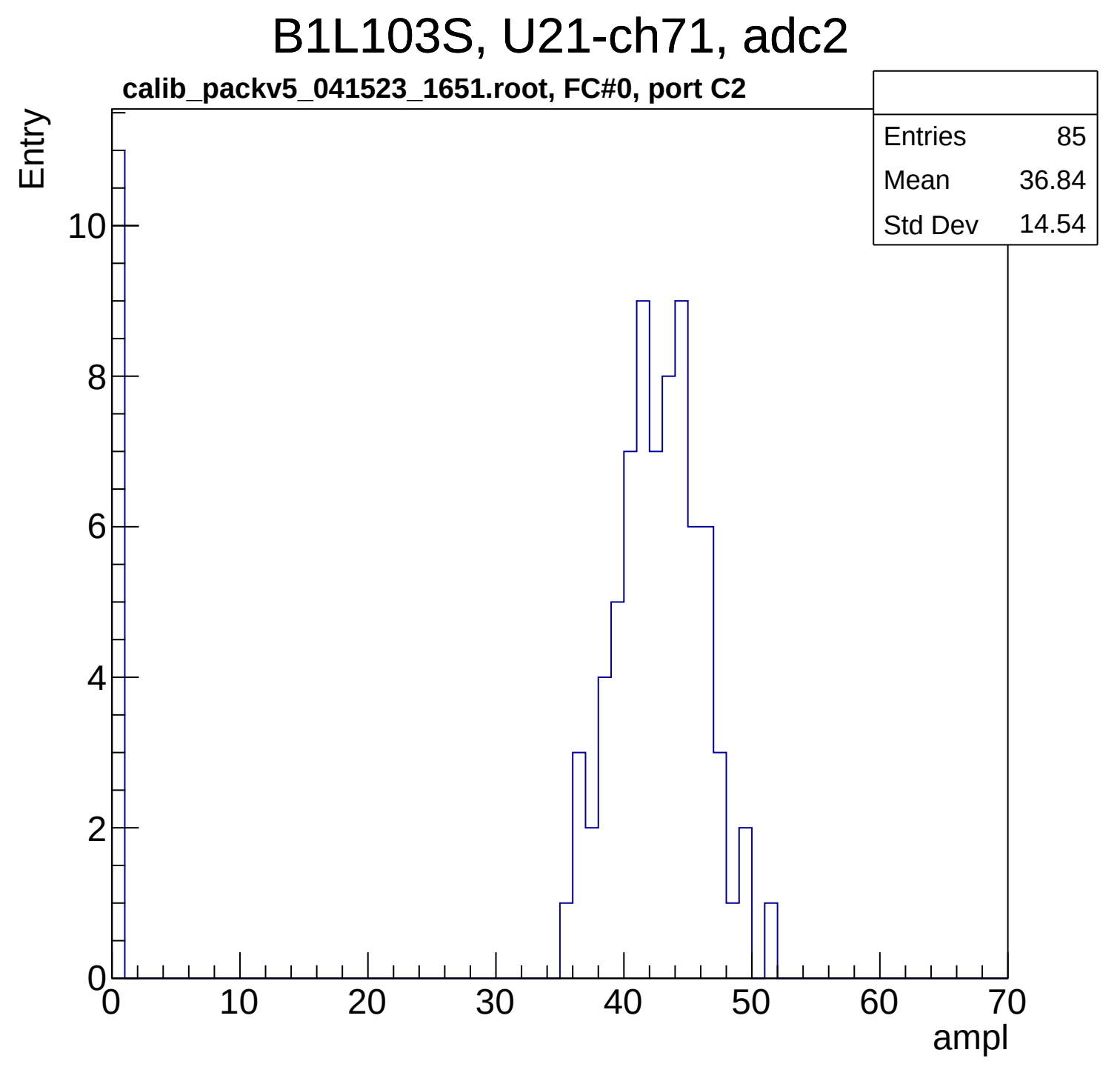
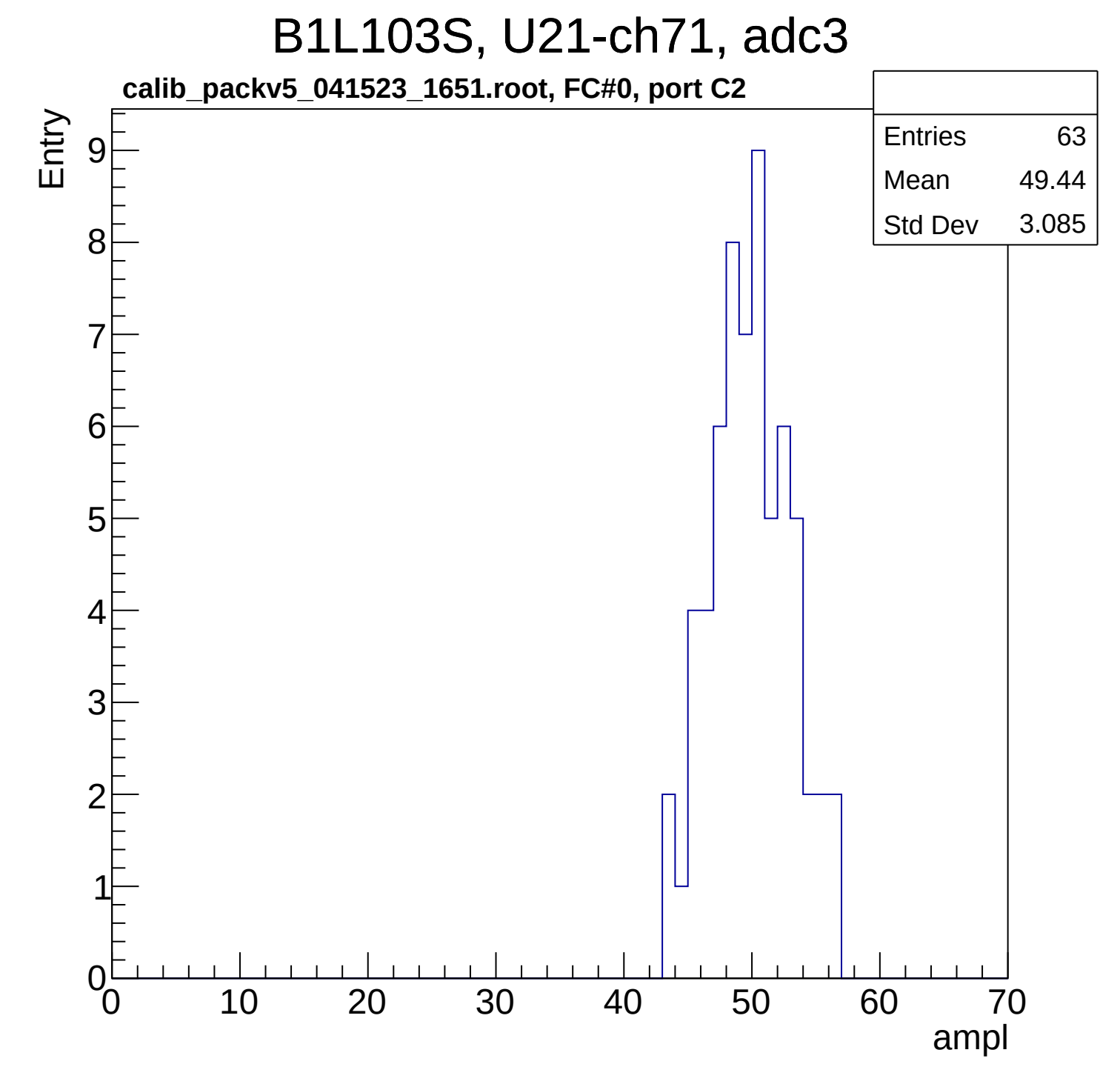
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

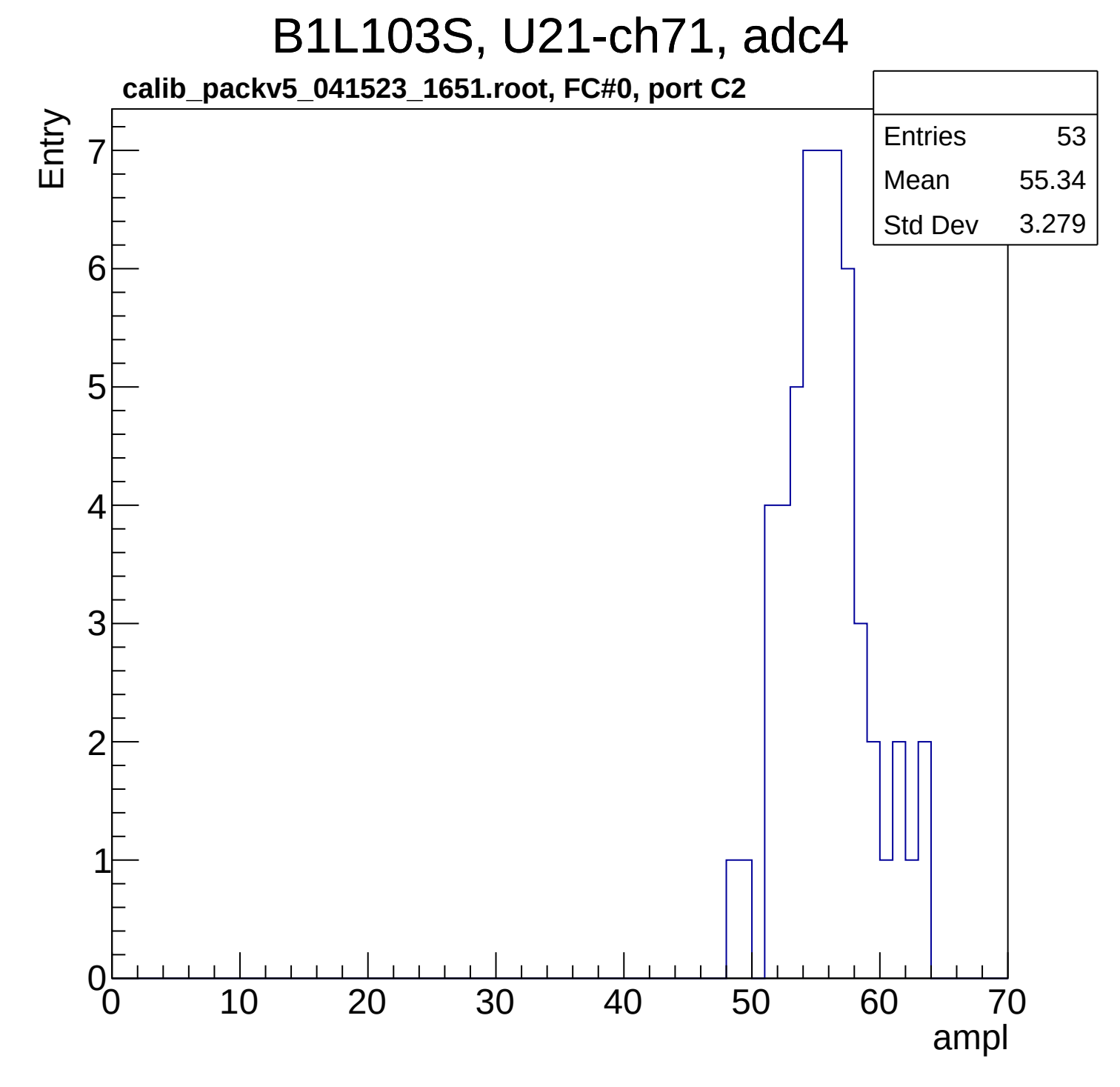

B1L103S, U21-ch70, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

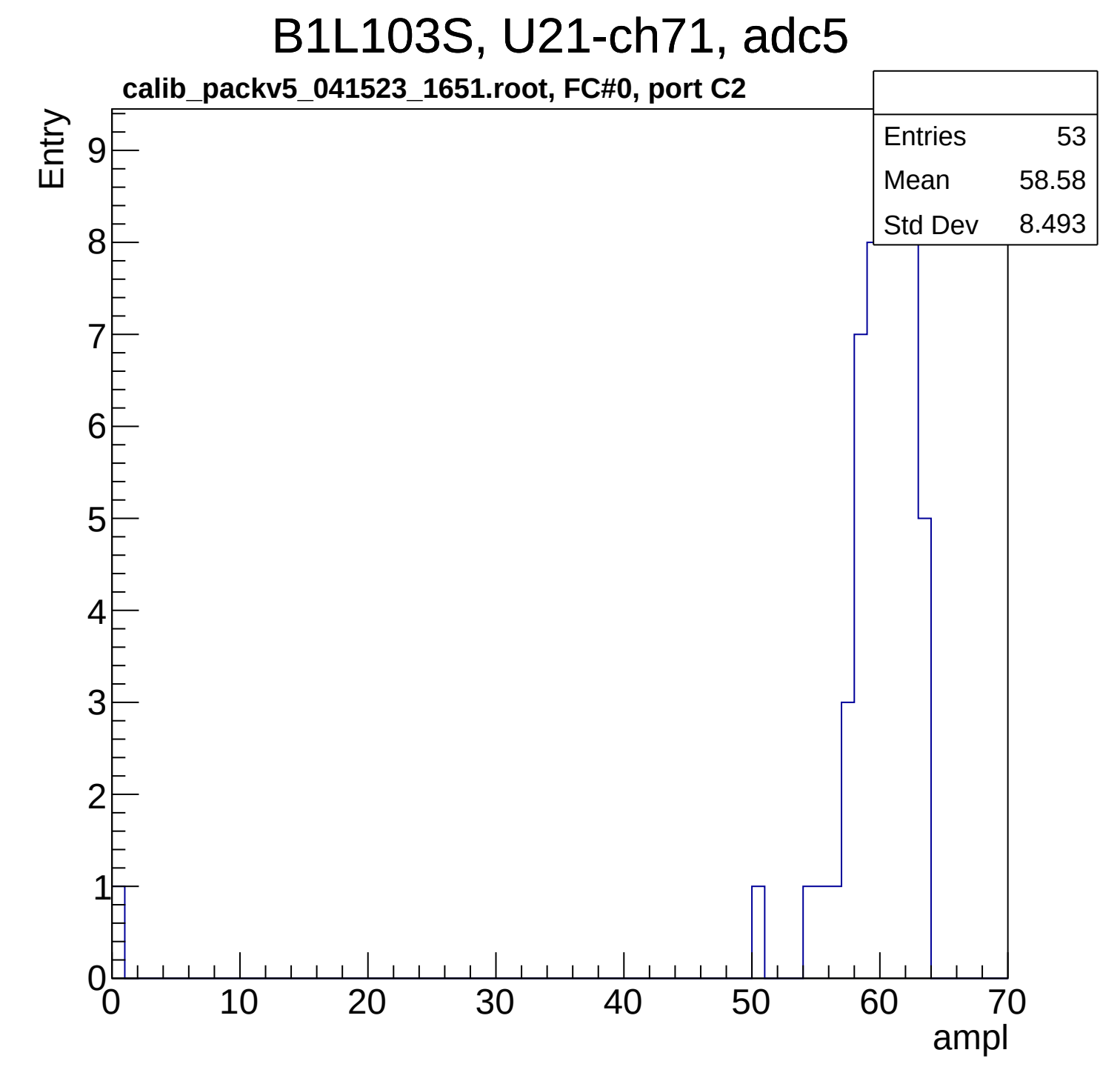

B1L103S, U21-ch71, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 23.95
Std Dev 11.5
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch71, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 33.34
Std Dev 8.783
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U21-ch71, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 36.84
Std Dev 14.54
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch71, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 49.44
Std Dev 3.085
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch71, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 55.34
Std Dev 3.279
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U21-ch71, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 58.58
Std Dev 8.493
Entry
ampl
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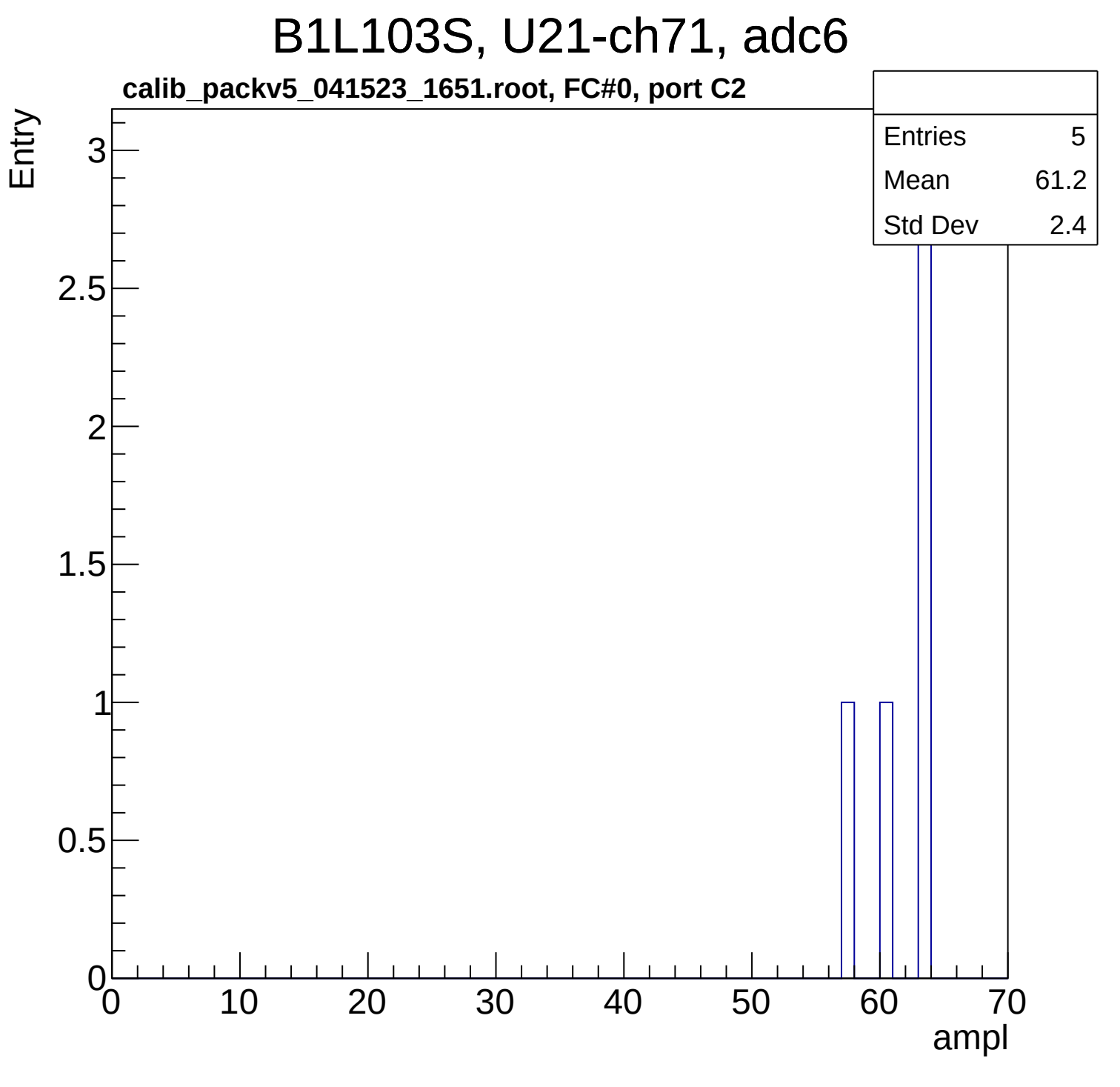
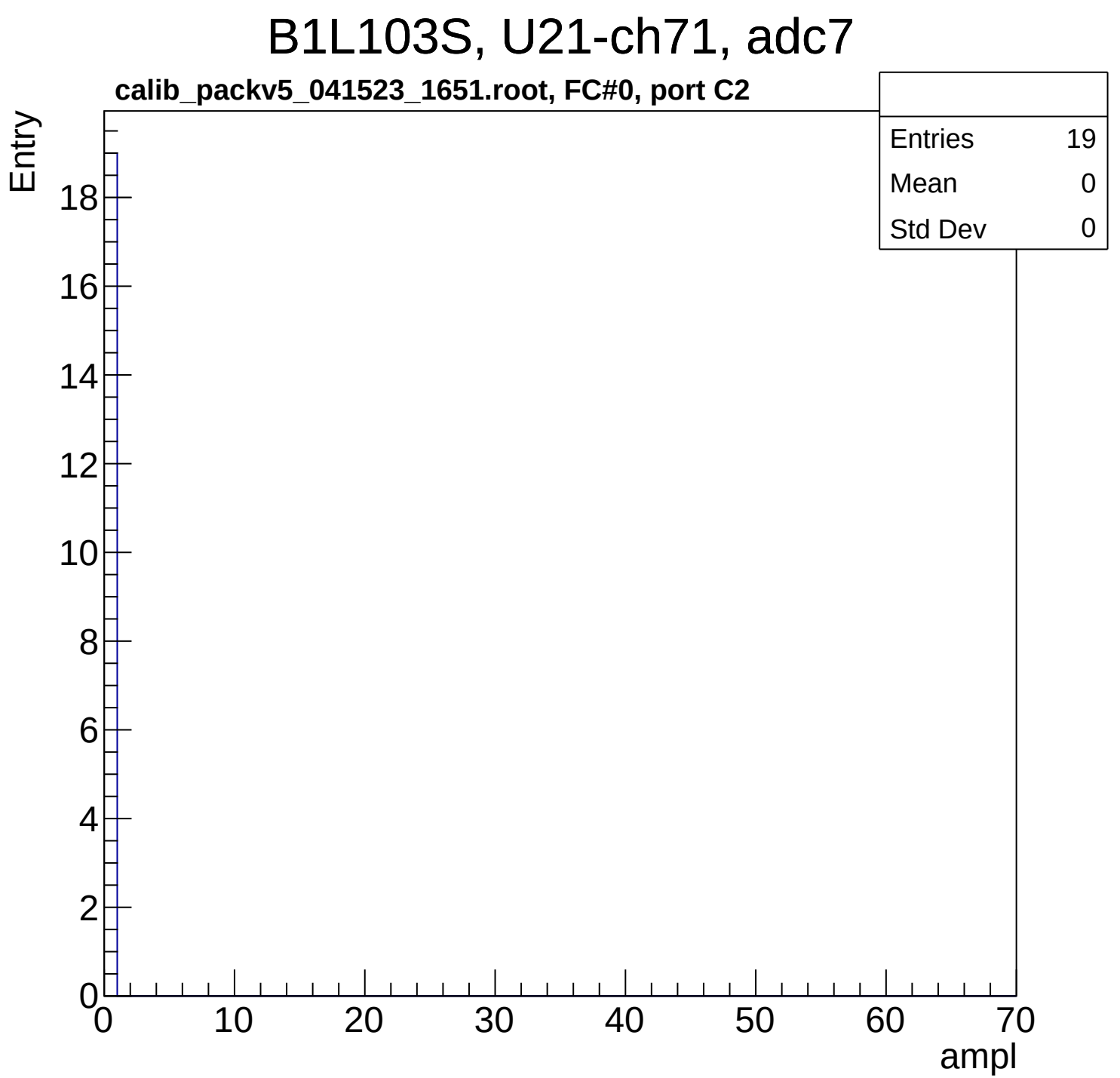
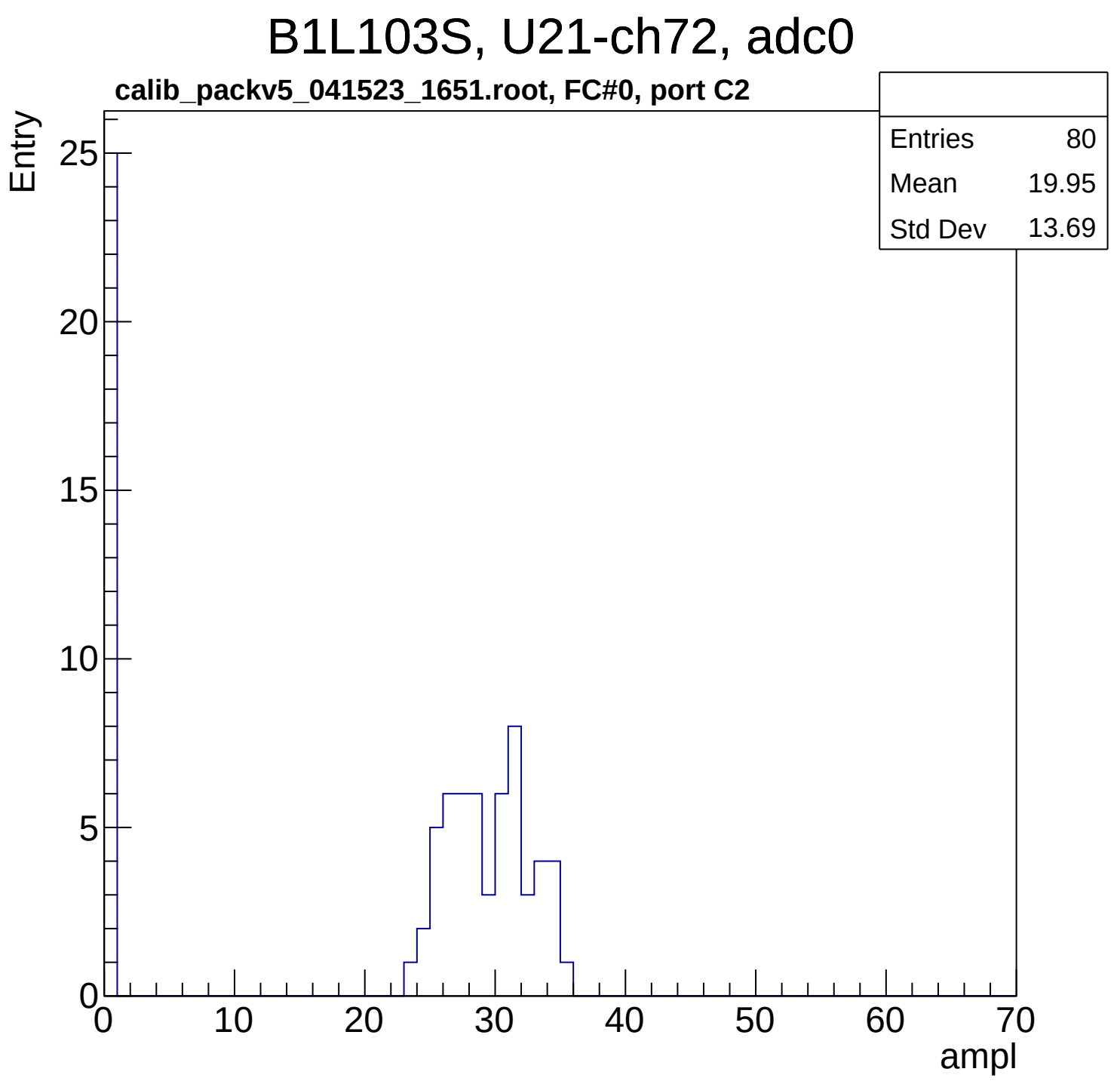
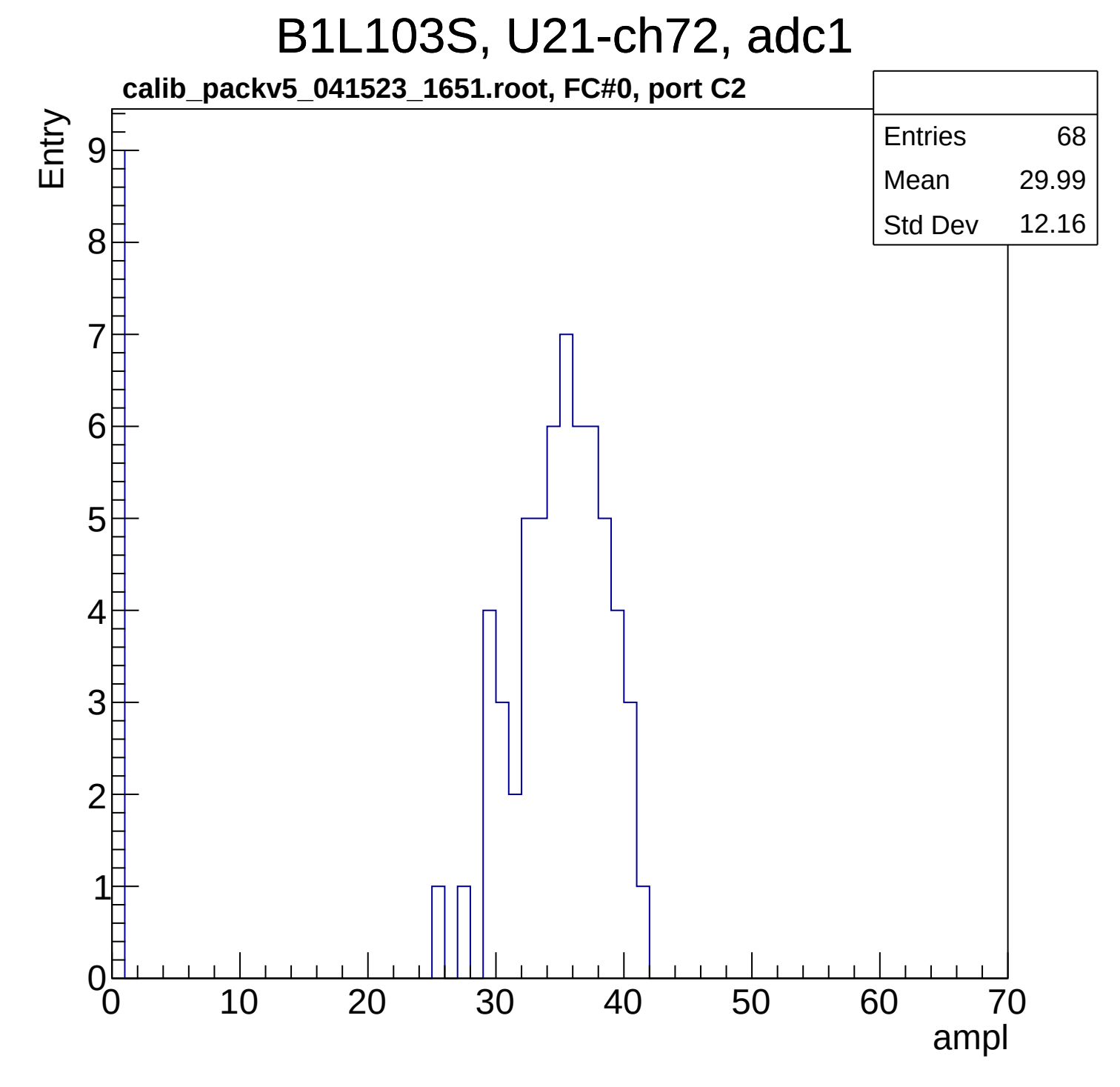
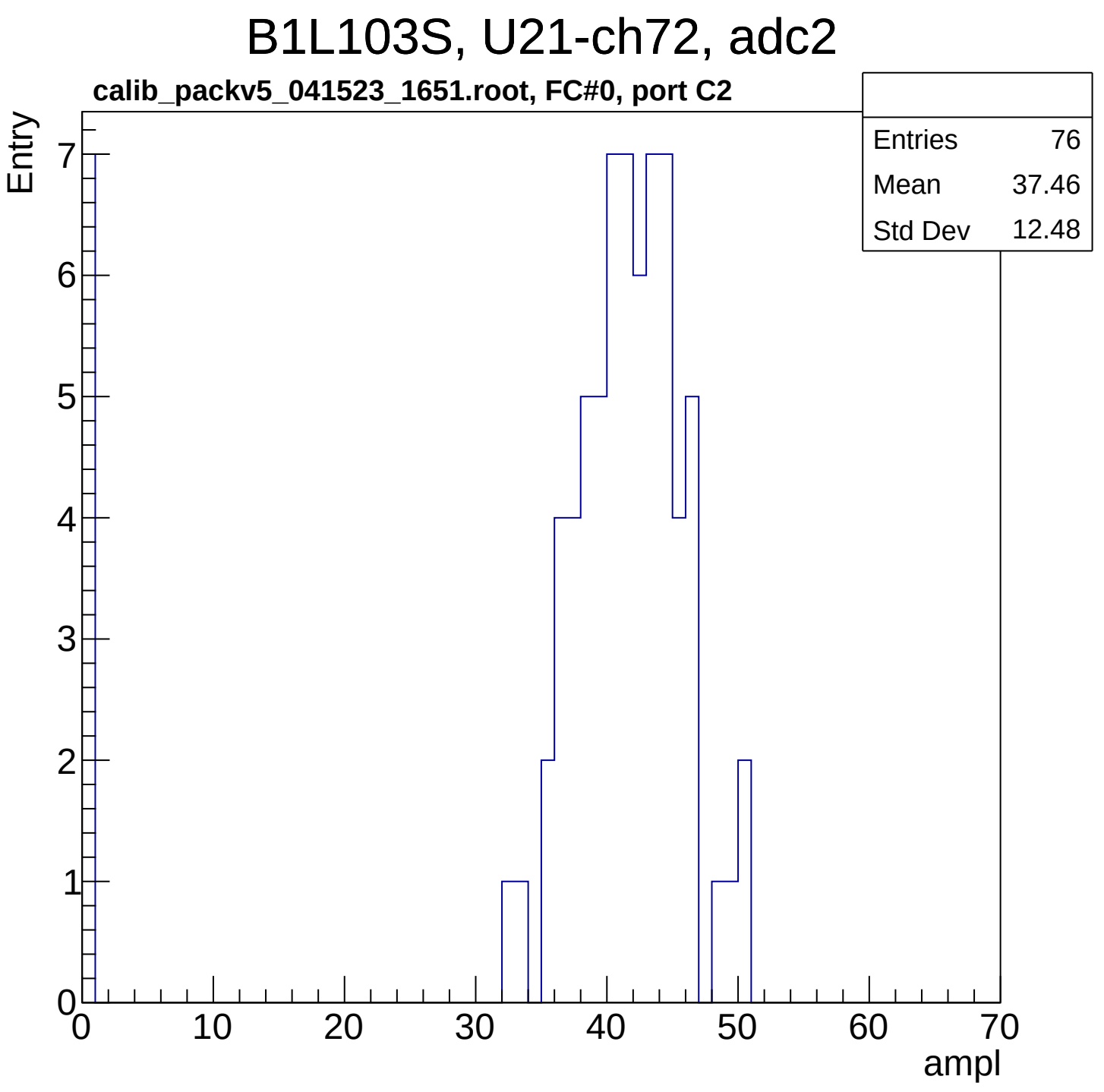
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

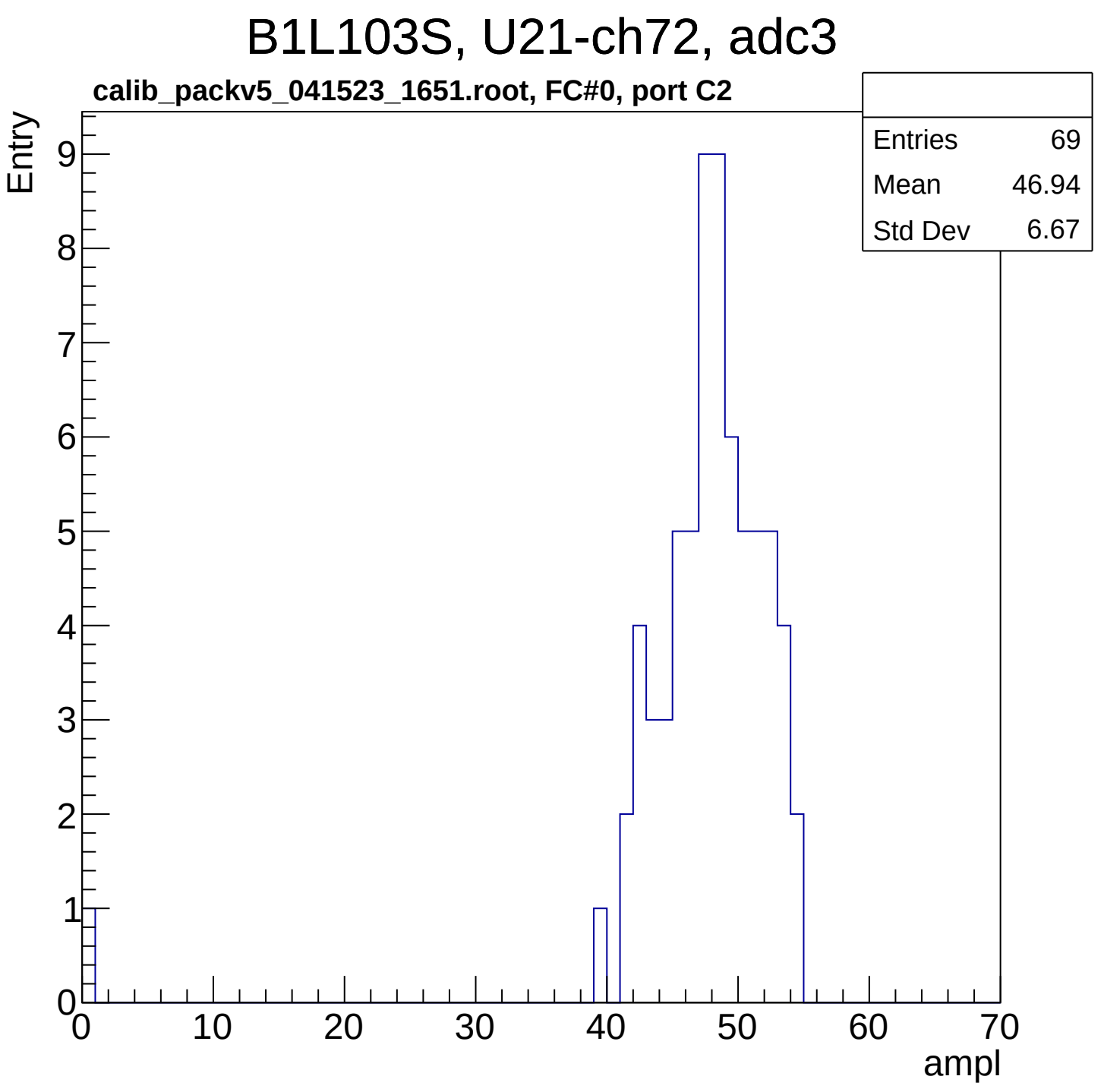

B1L103S, U21-ch71, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 61.2
Std Dev 2.4
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U21-ch71, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch72, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 19.95
Std Dev 13.69
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch72, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 29.99
Std Dev 12.16
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch72, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 37.46
Std Dev 12.48
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U21-ch72, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 46.94
Std Dev 6.67
Entry
ampl
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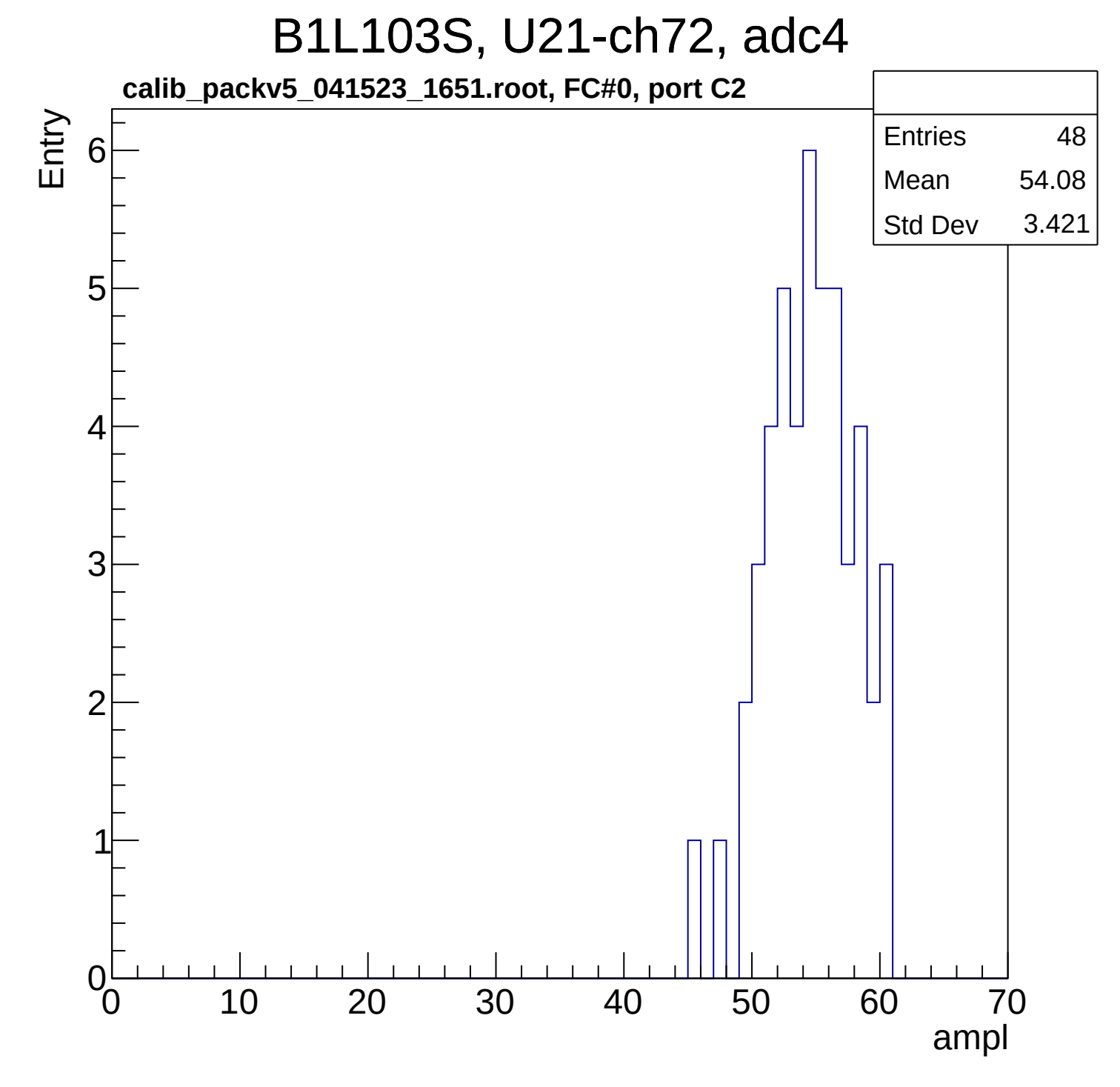
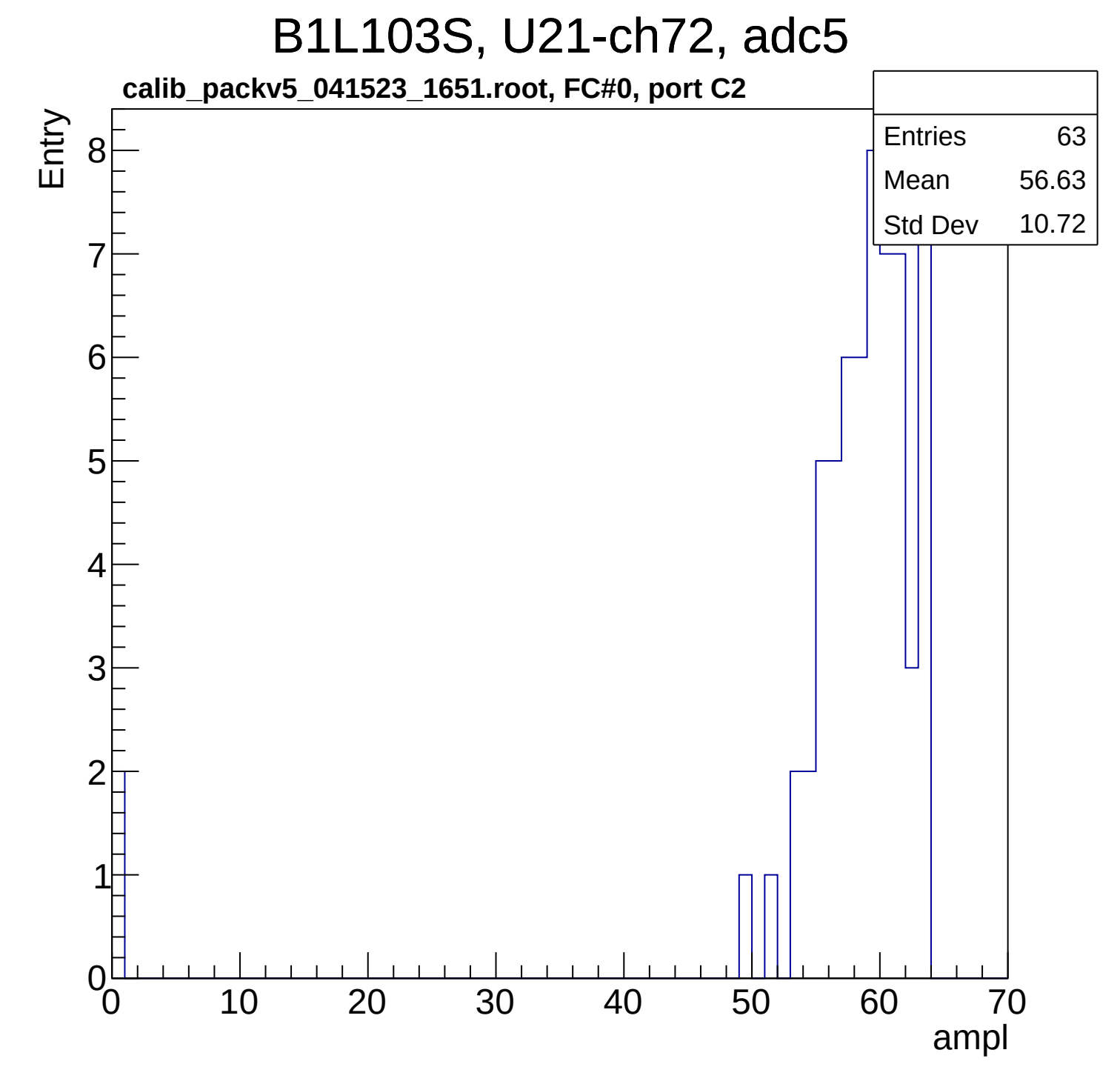
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch72, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 54.08
Std Dev 3.421
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U21-ch72, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 56.63
Std Dev 10.72
Entry
ampl
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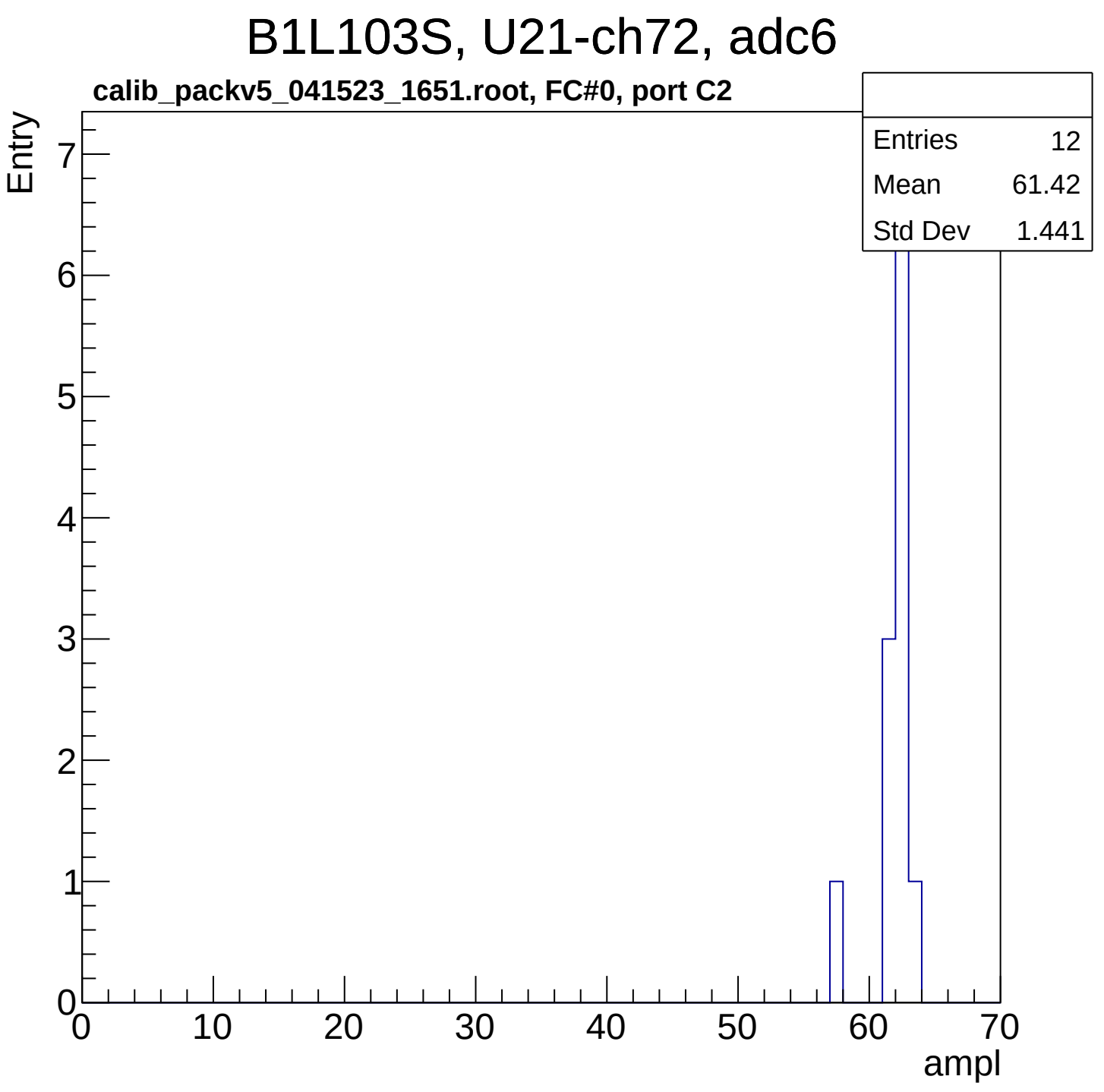
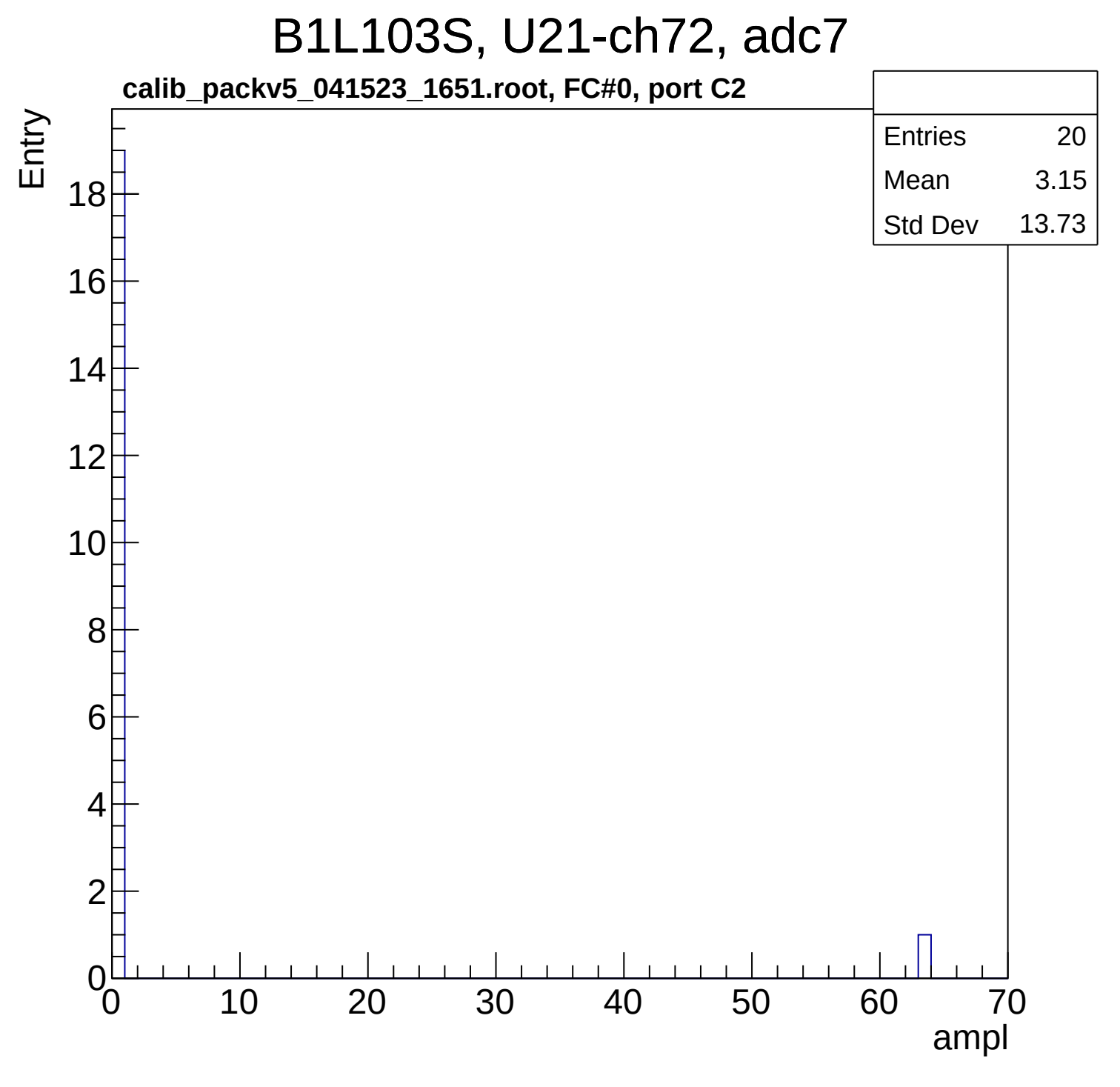
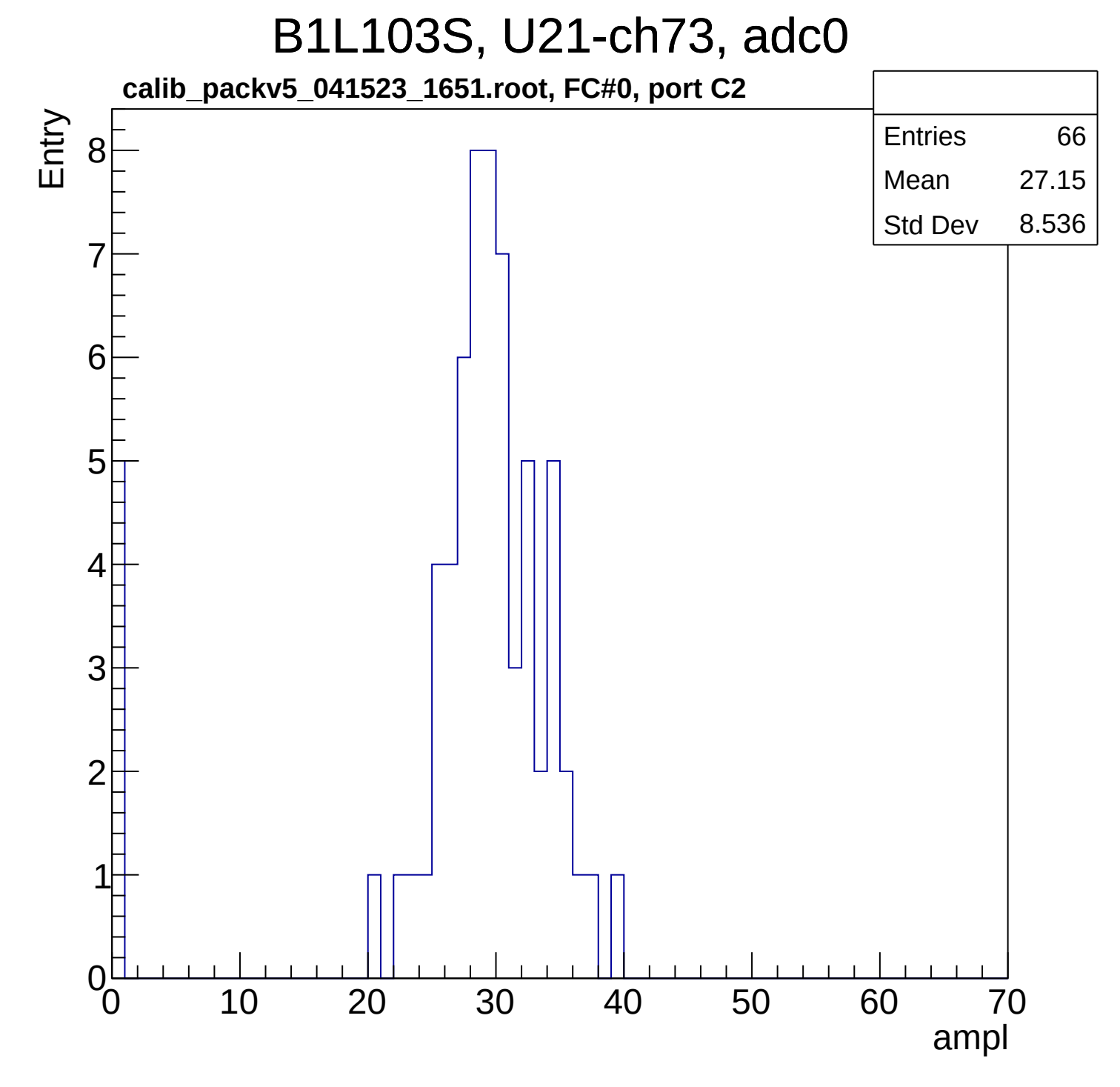
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch72, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.42
Std Dev 1.441
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U21-ch72, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch73, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 27.15
Std Dev 8.536
Entry
ampl
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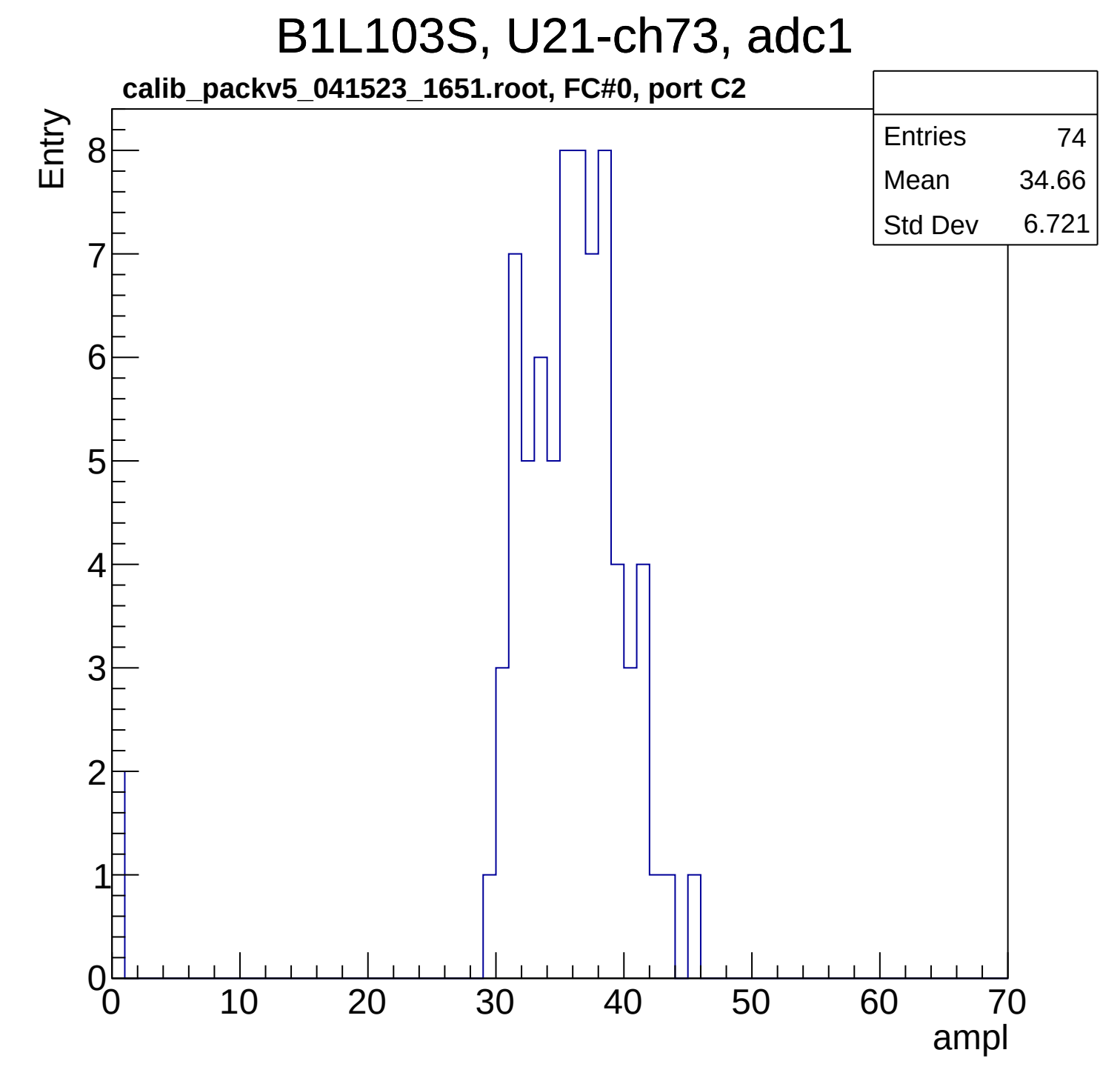
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch73, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 34.66
Std Dev 6.721
Entry
ampl
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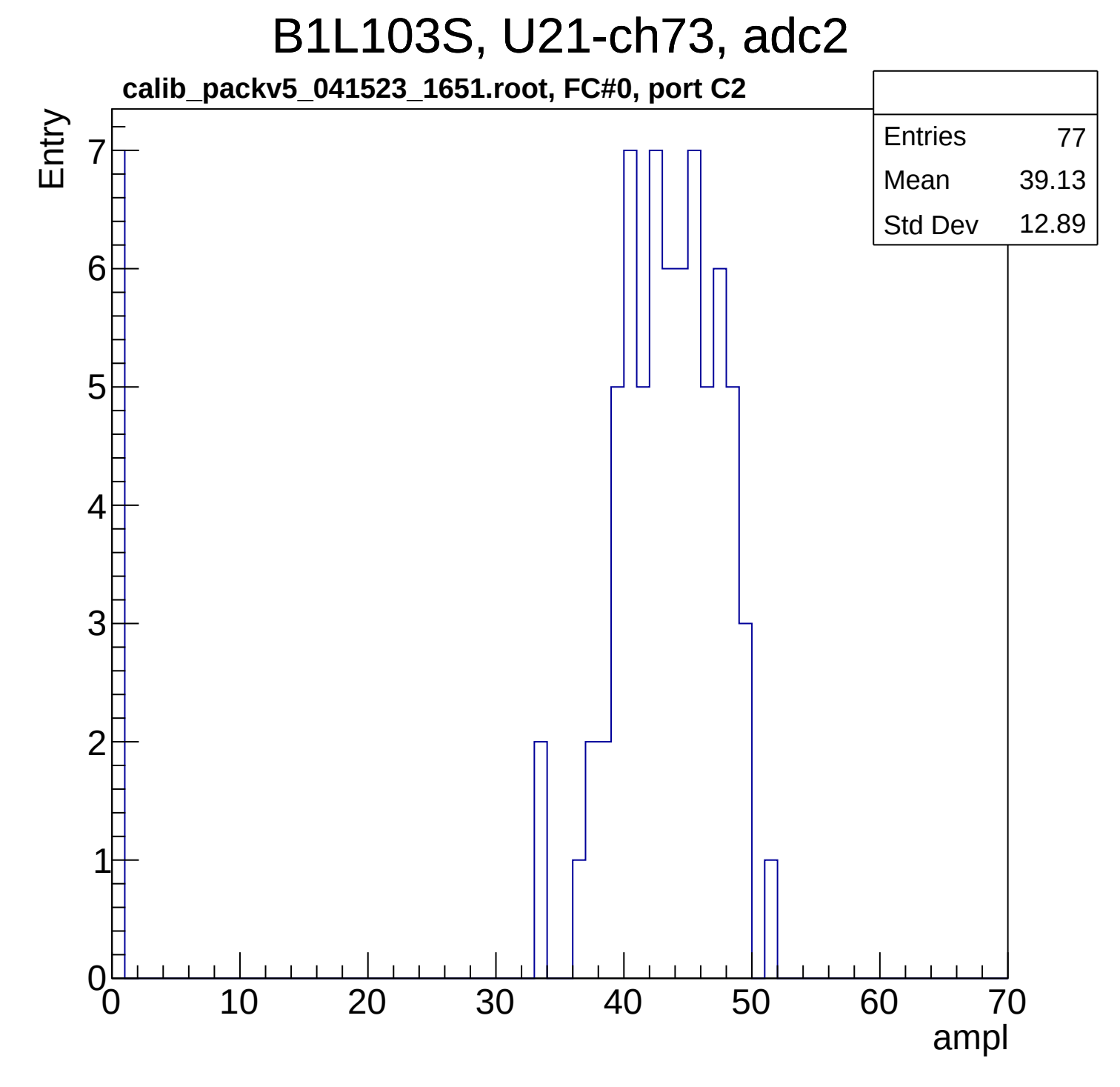
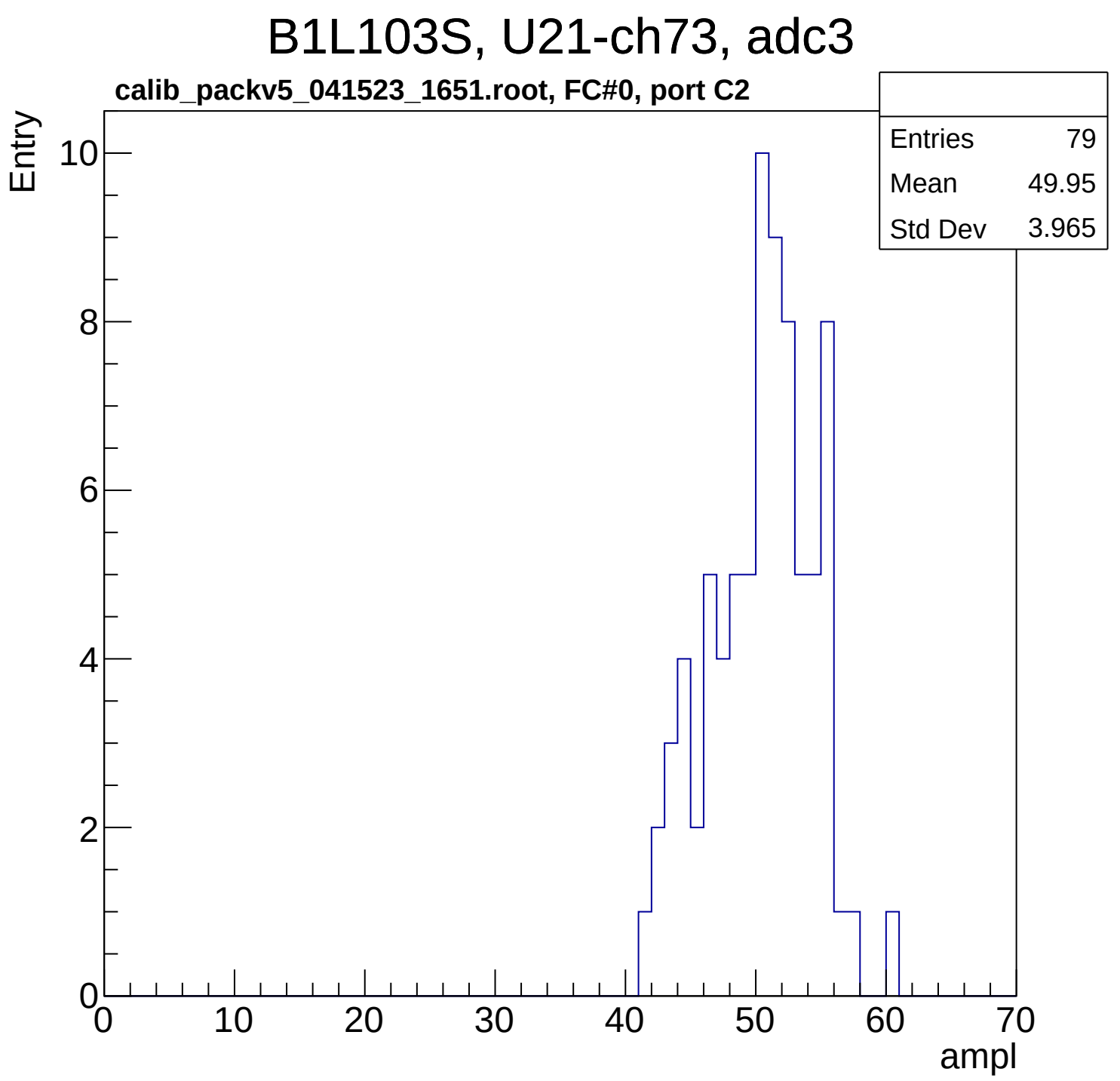
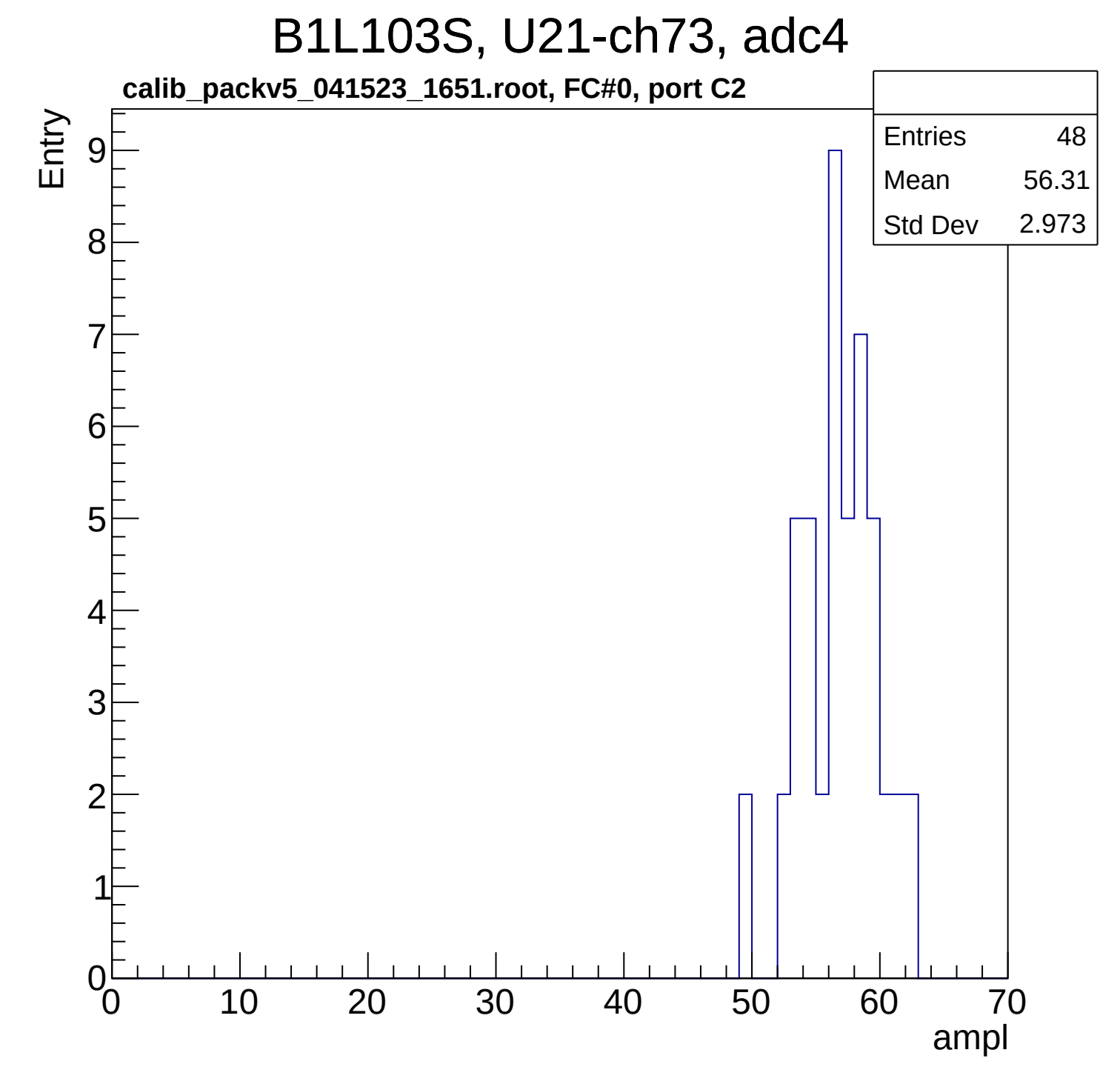
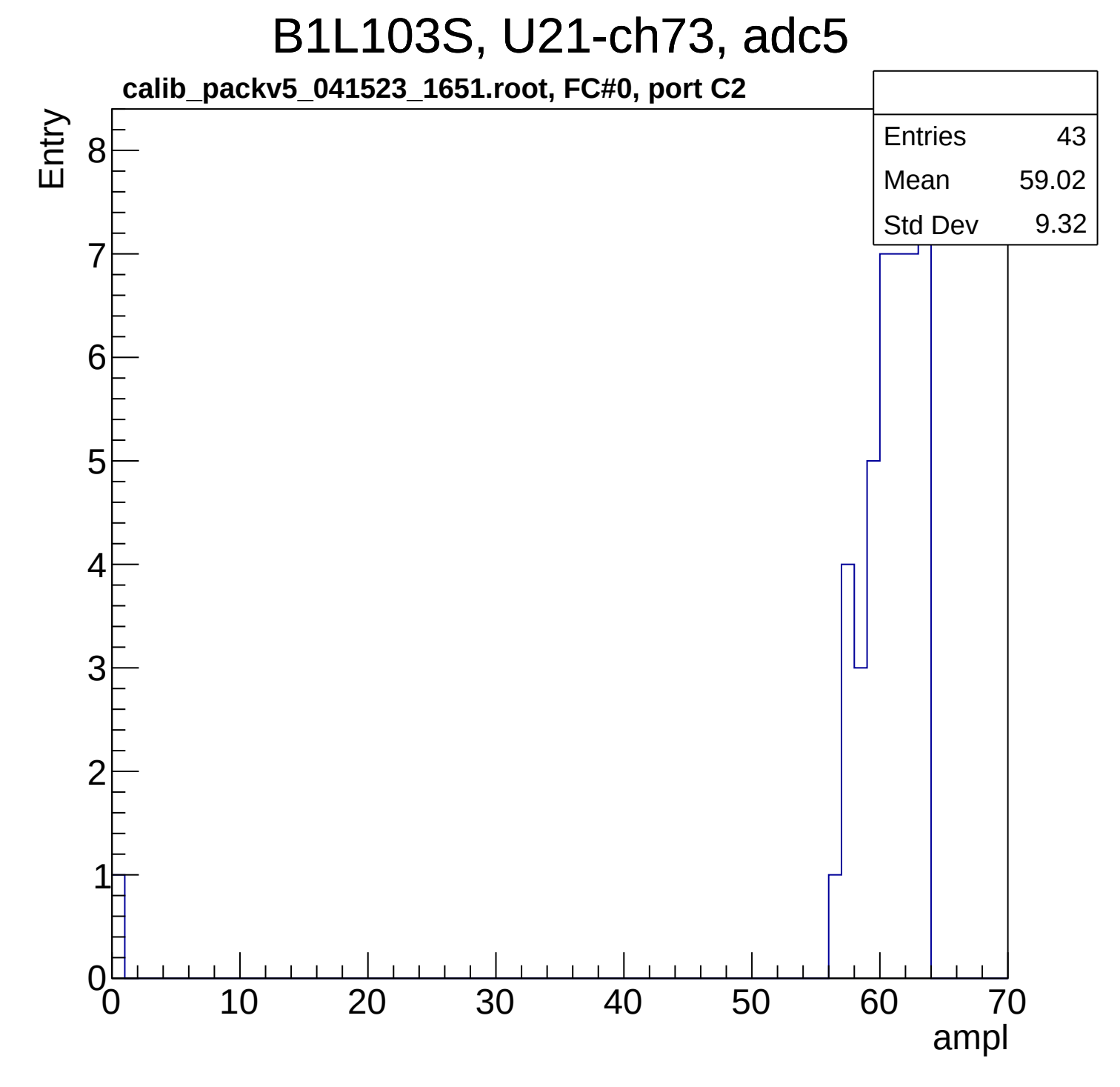
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch73, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 39.13
Std Dev 12.89
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U21-ch73, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 49.95
Std Dev 3.965
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U21-ch73, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 56.31
Std Dev 2.973
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch73, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 59.02
Std Dev 9.32
Entry
ampl
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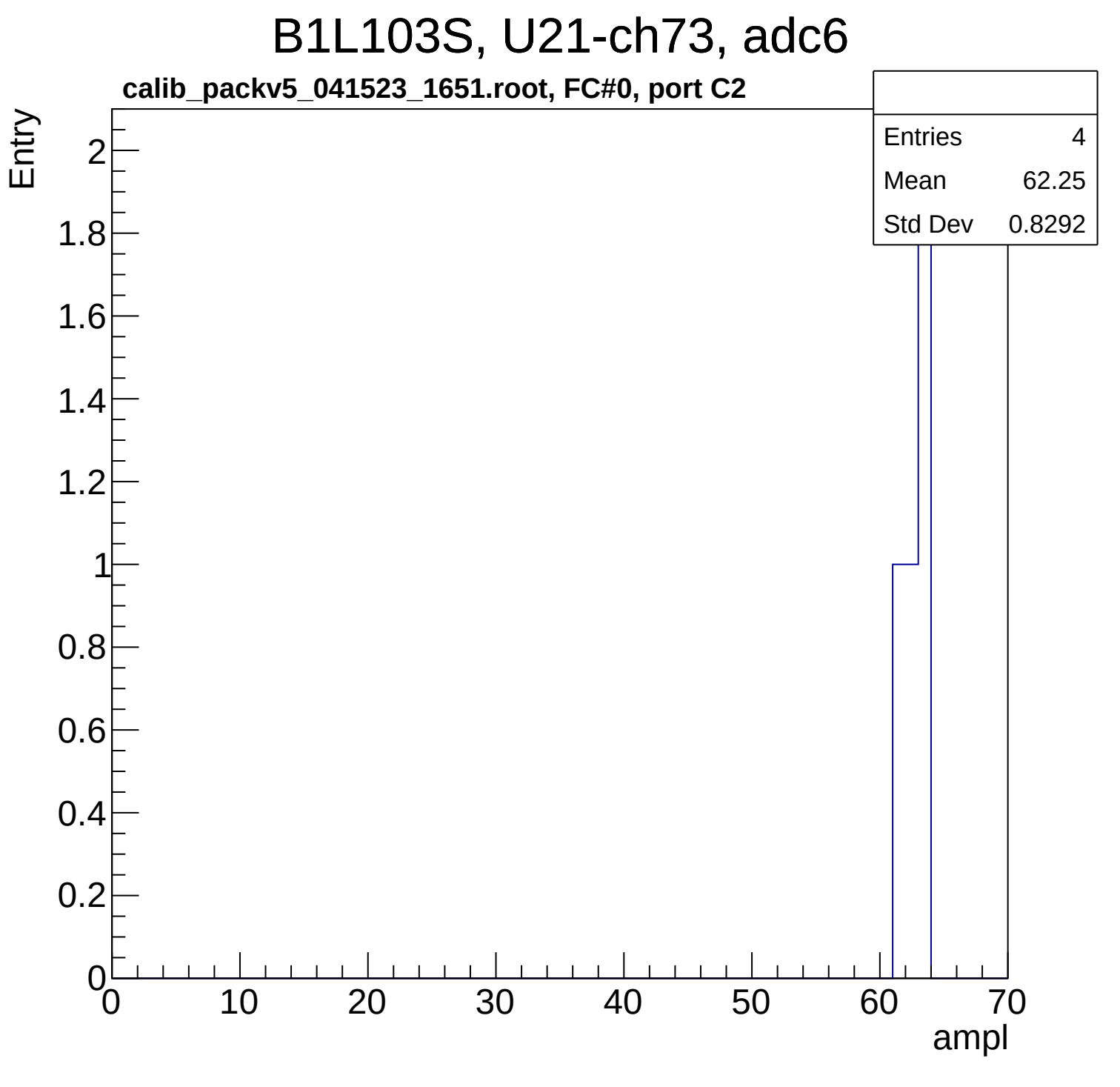
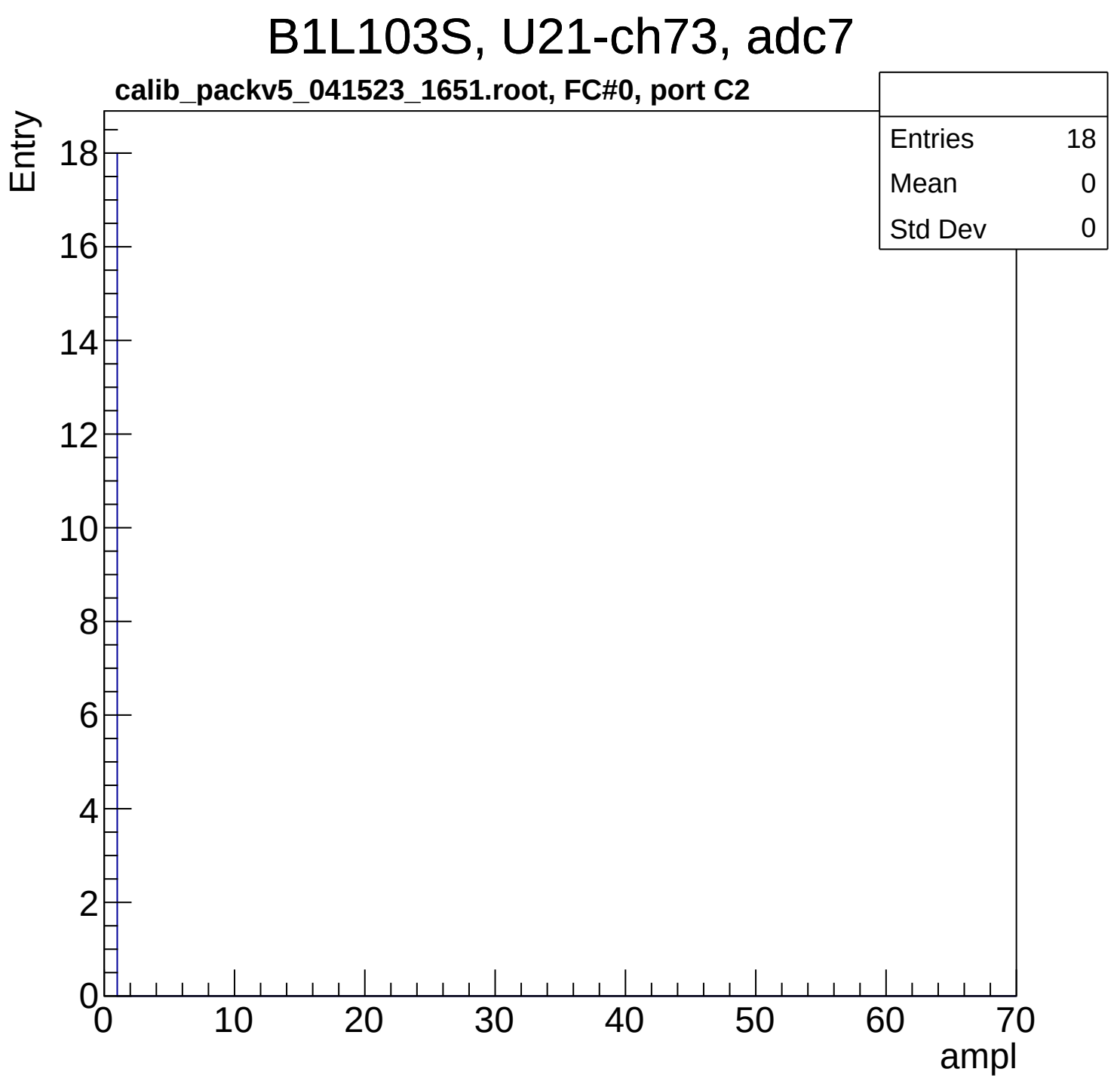
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch73, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 62.25
Std Dev 0.8292
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U21-ch73, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
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2
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6
8
10
12
14
16
18
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10
20
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50
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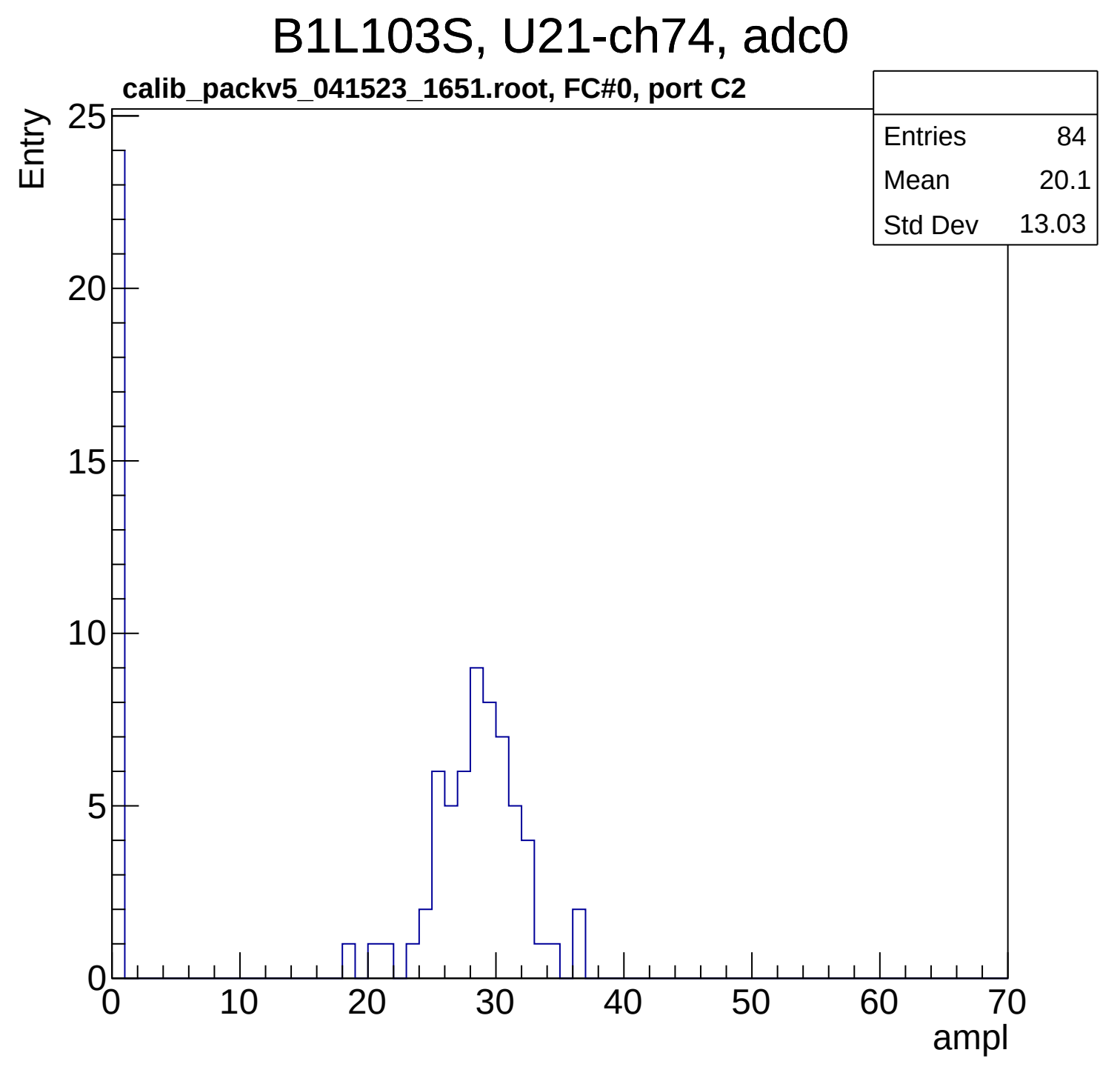
70
ampl


B1L103S, U21-ch74, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 20.1
Std Dev 13.03
Entry
ampl
0
5
10
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0
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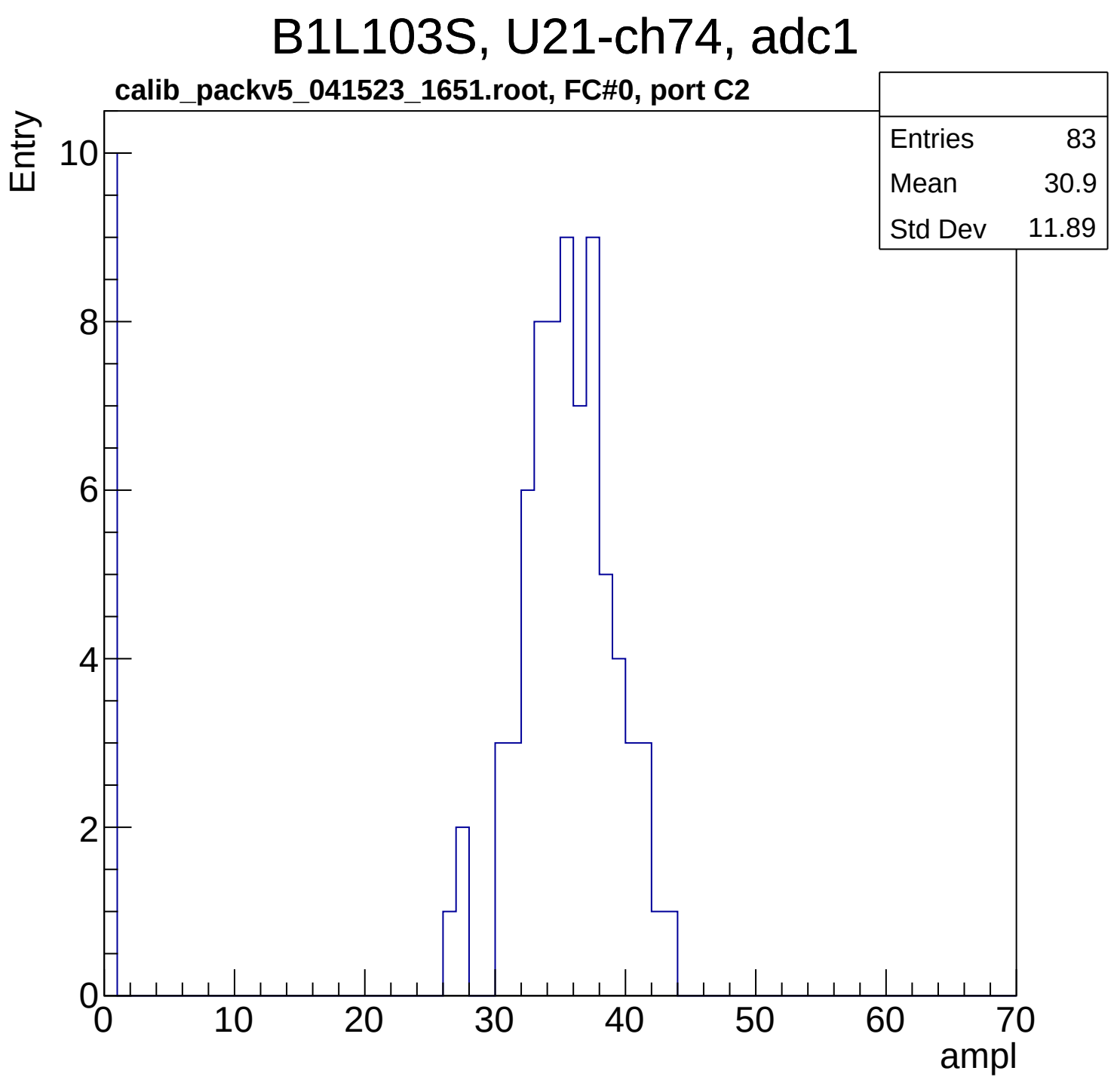
B1L103S, U21-ch74, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 30.9
Std Dev 11.89
Entry
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2
4
6
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10
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10
20
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50
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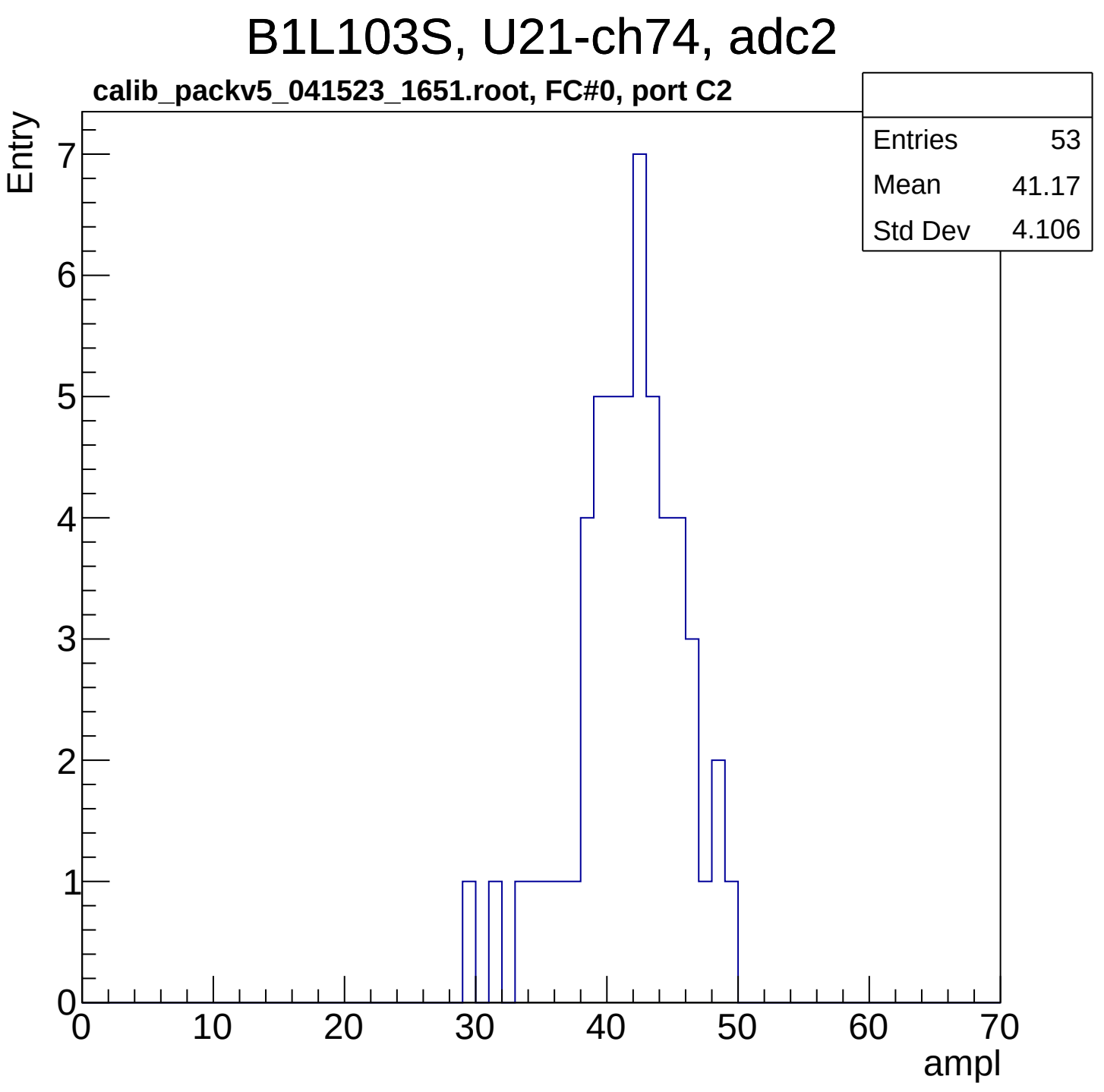
70
ampl


B1L103S, U21-ch74, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 41.17
Std Dev 4.106
Entry
ampl
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0
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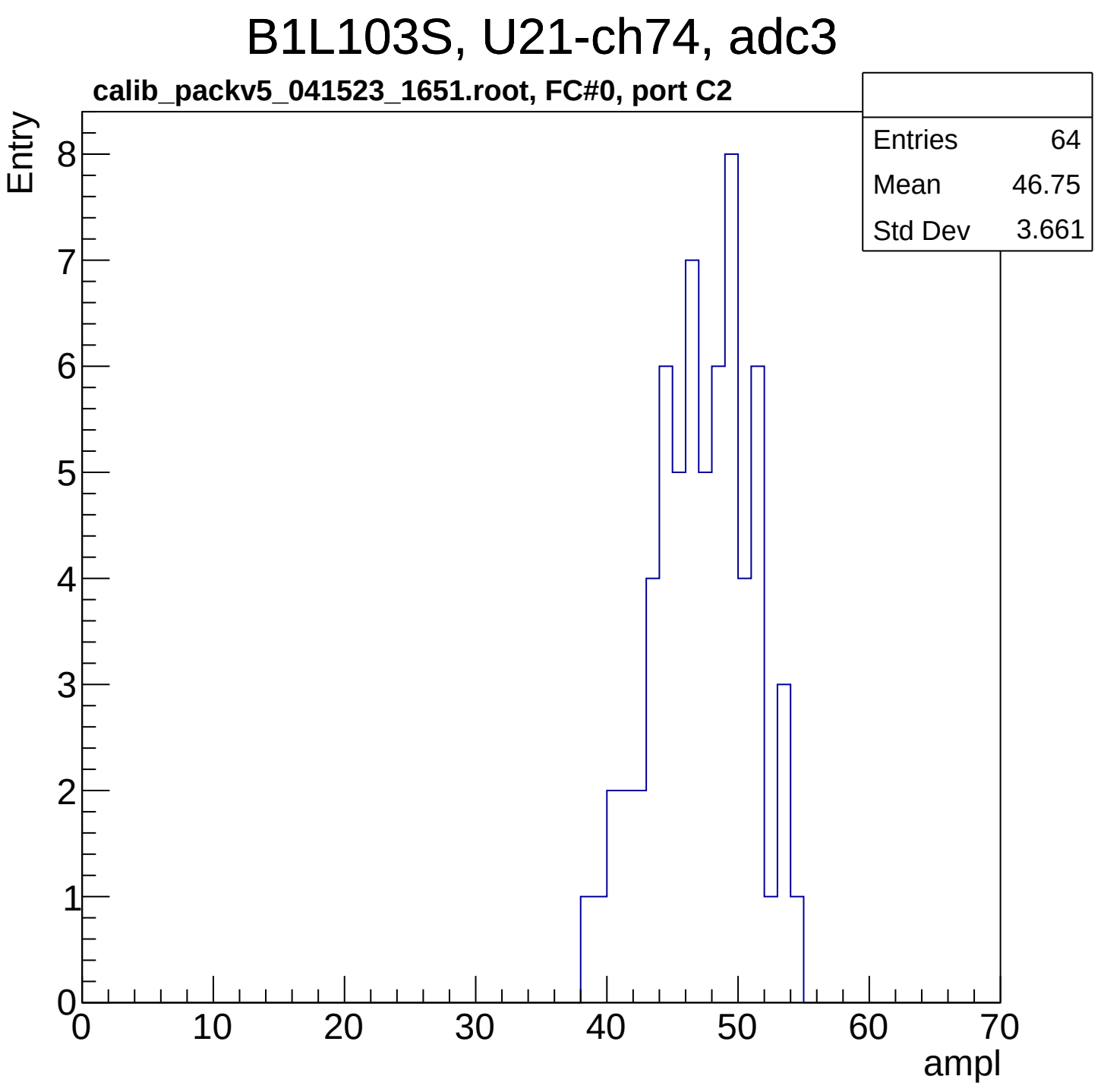
B1L103S, U21-ch74, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 46.75
Std Dev 3.661
Entry
ampl
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7
8
0
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40
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60
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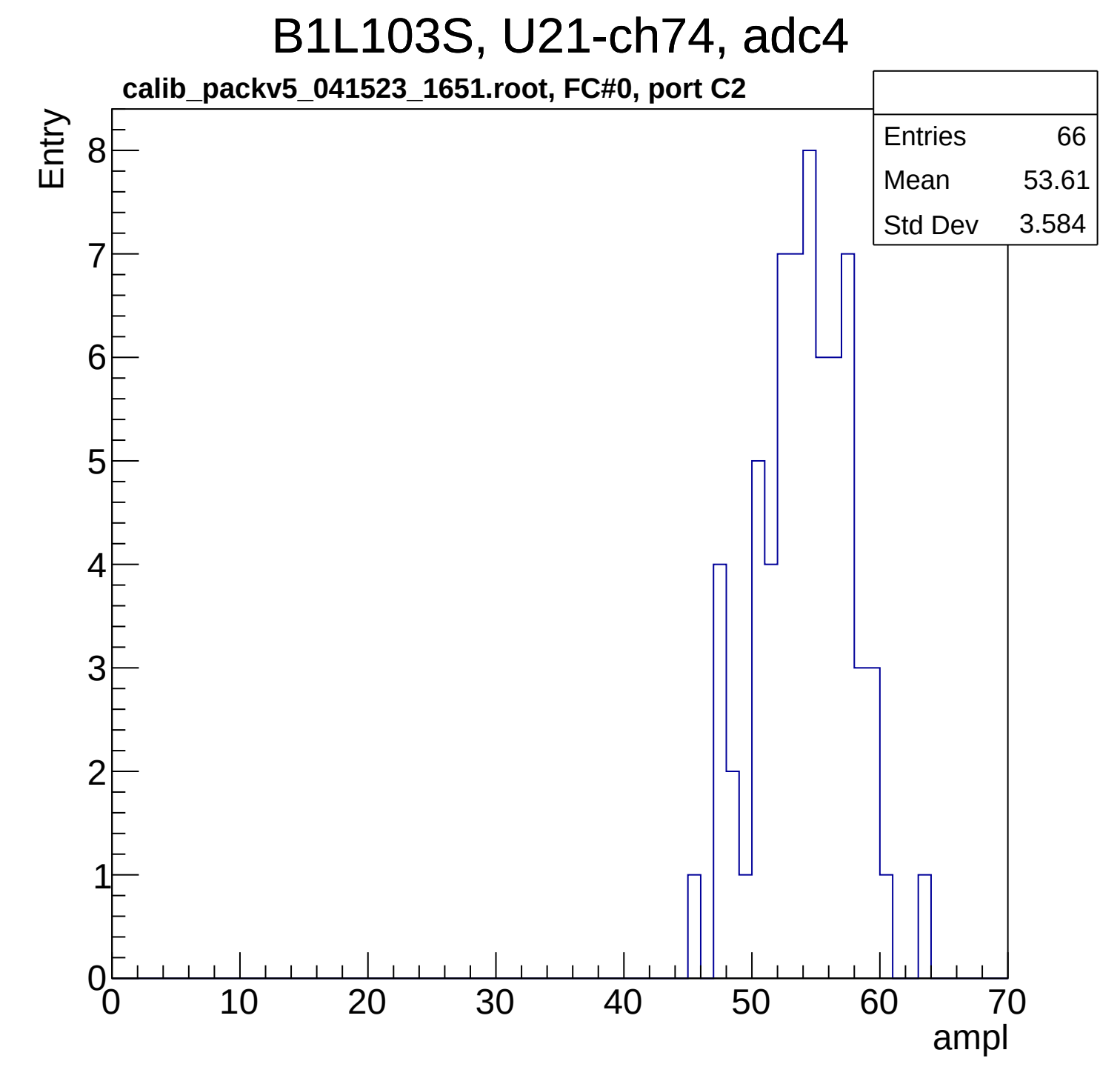
B1L103S, U21-ch74, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 53.61
Std Dev 3.584
Entry
ampl
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4
5
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7
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0
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40
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60
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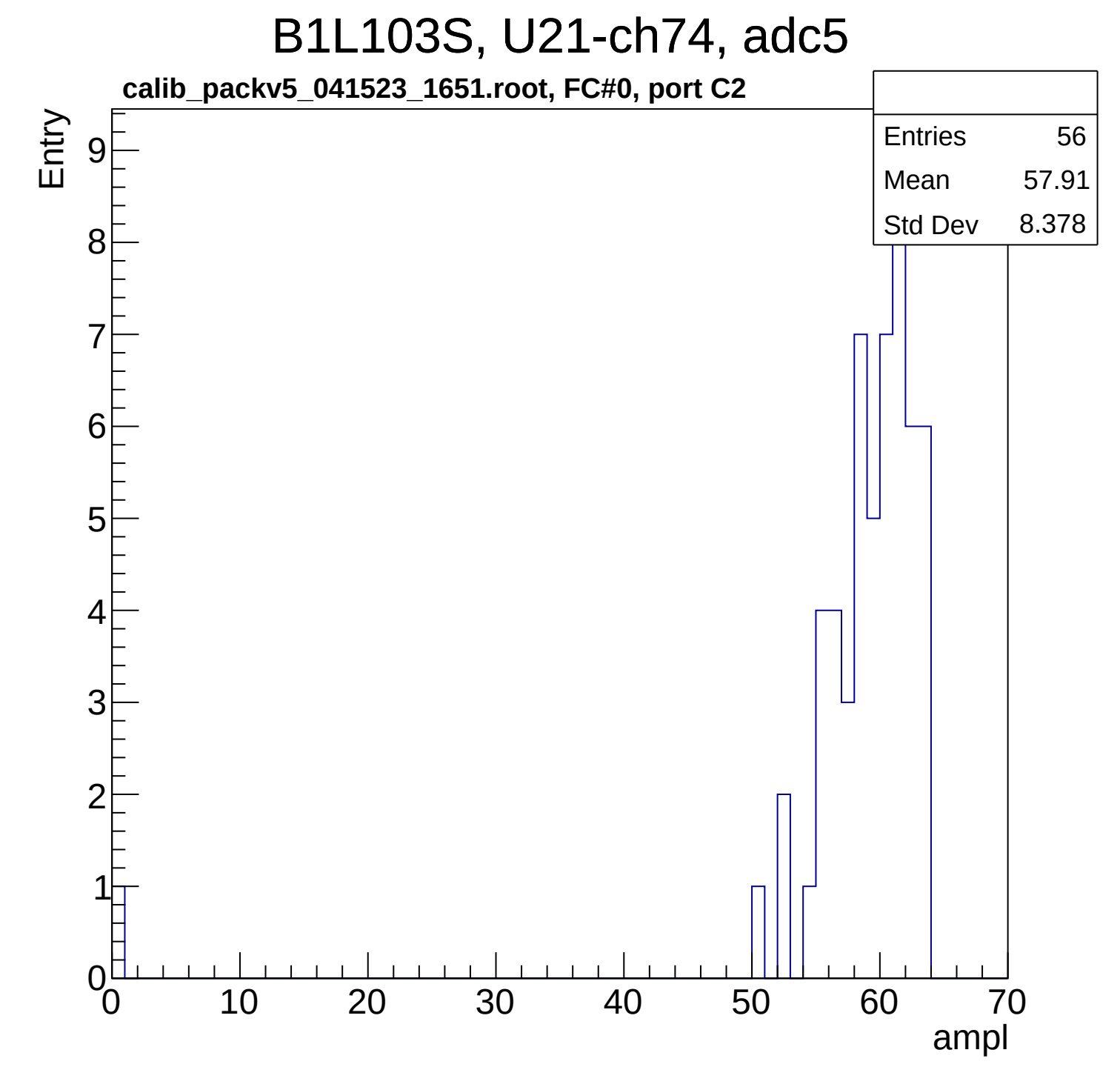
B1L103S, U21-ch74, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 57.91
Std Dev 8.378
Entry
ampl
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6
7
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0
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60
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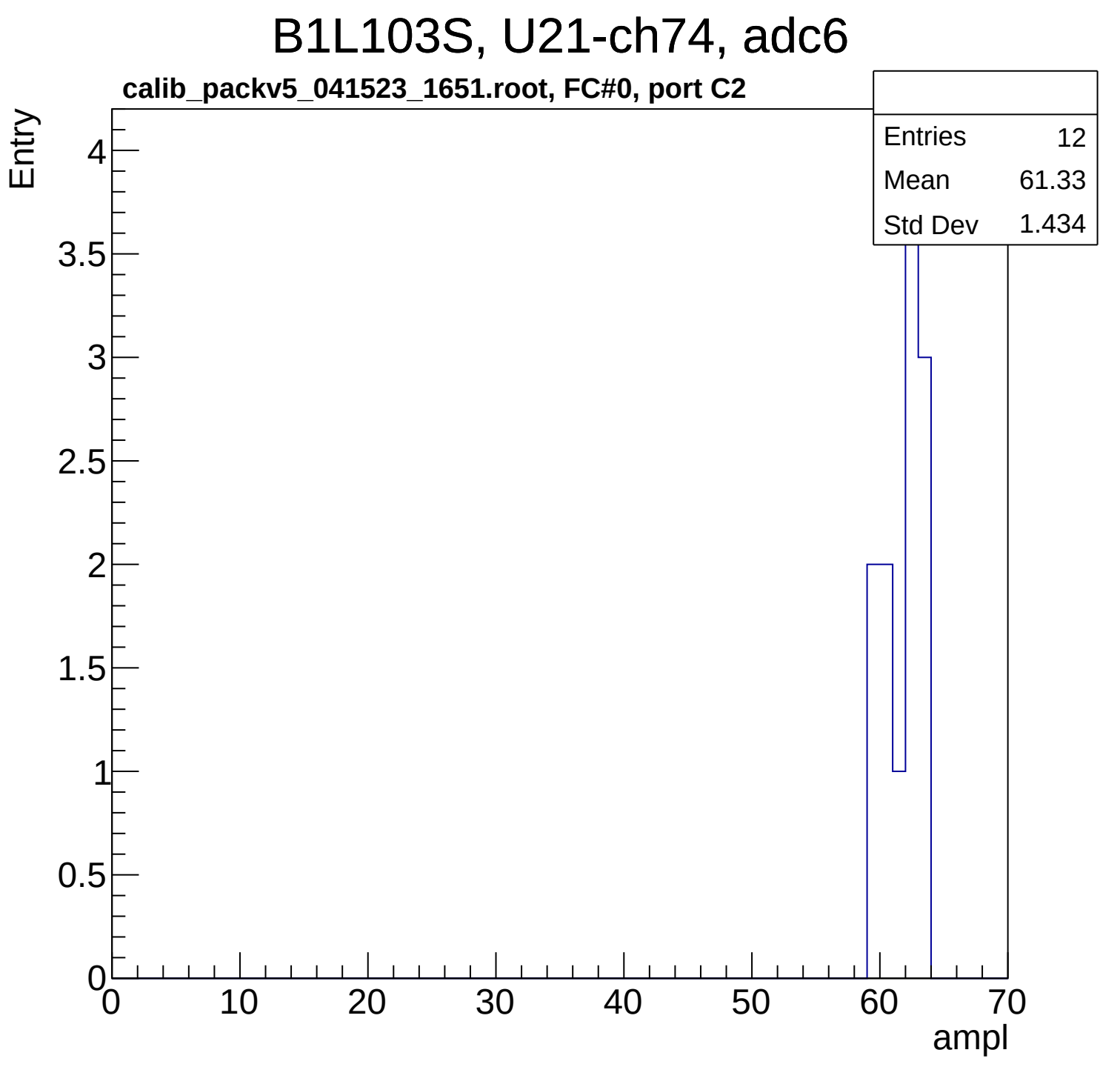
B1L103S, U21-ch74, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.33
Std Dev 1.434
Entry
ampl
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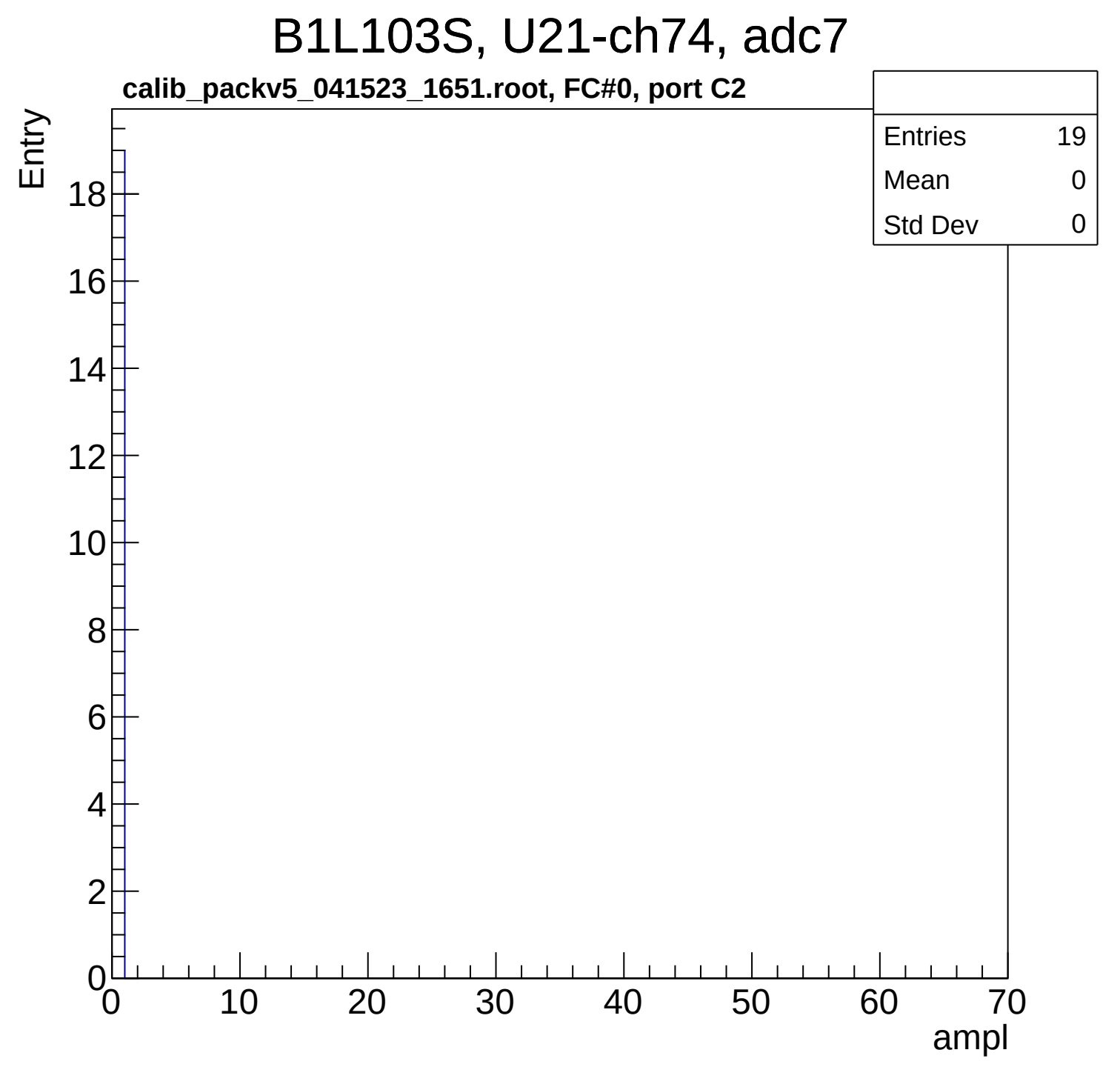
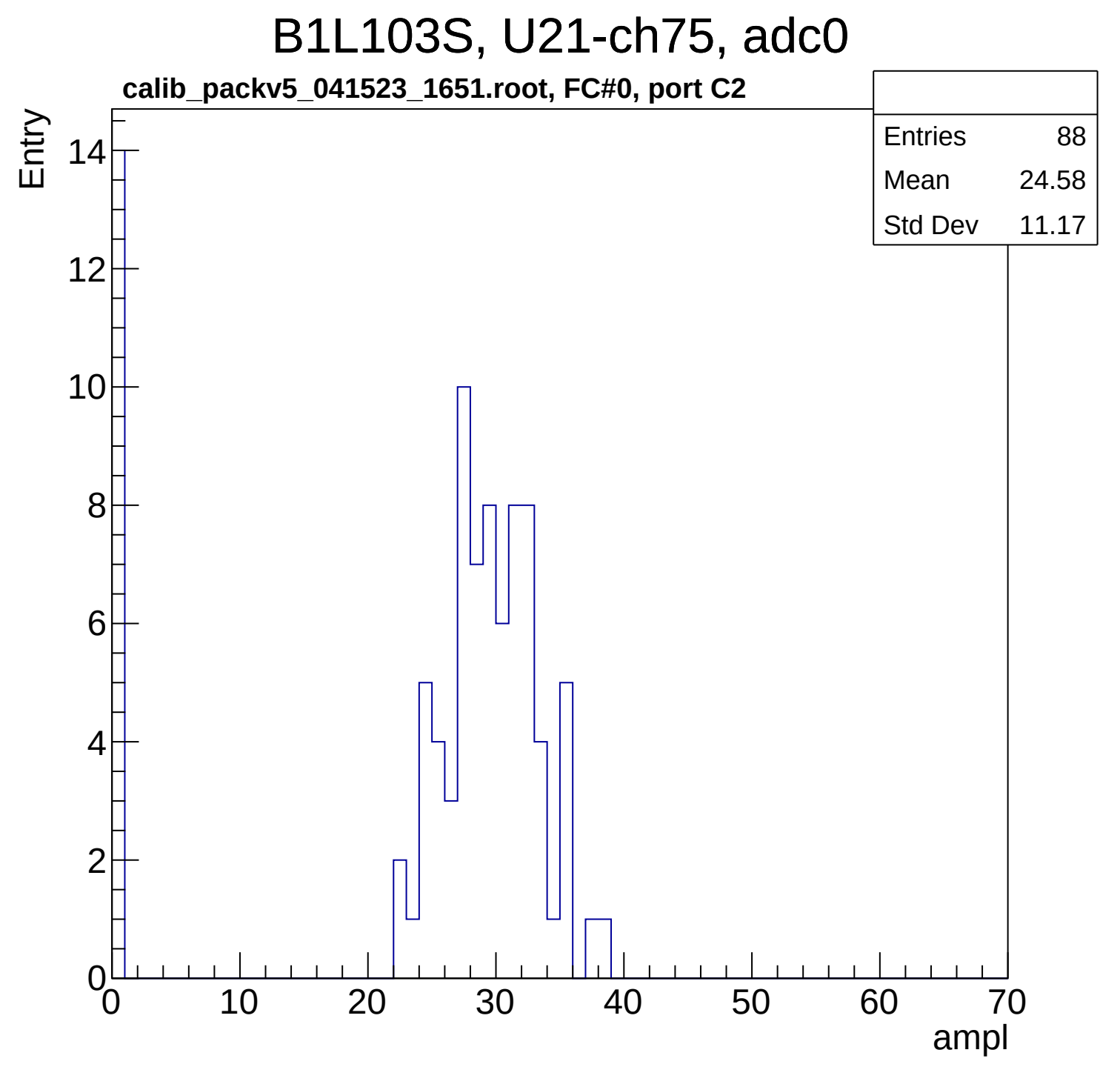
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U21-ch74, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch75, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 24.58
Std Dev 11.17
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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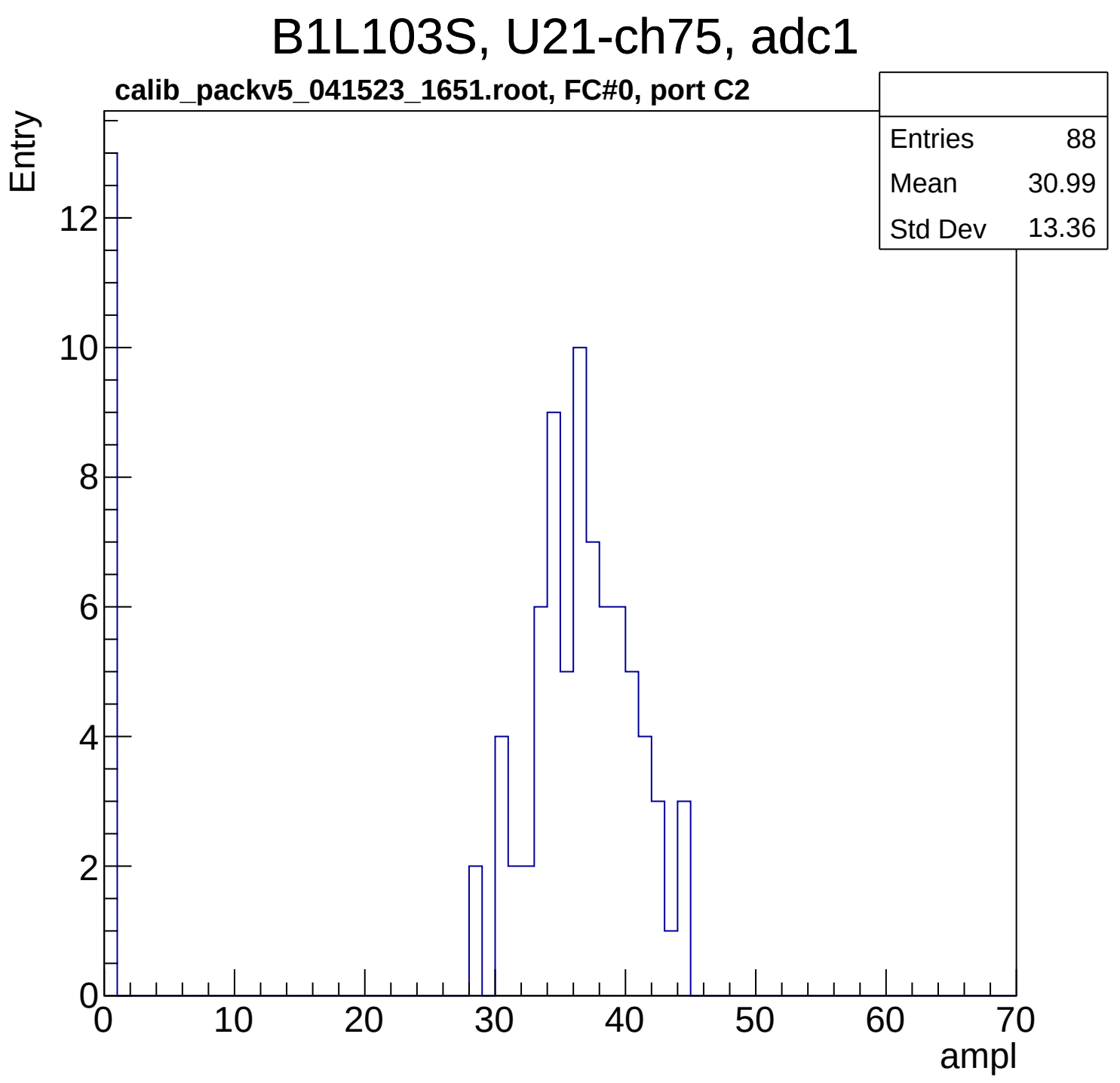
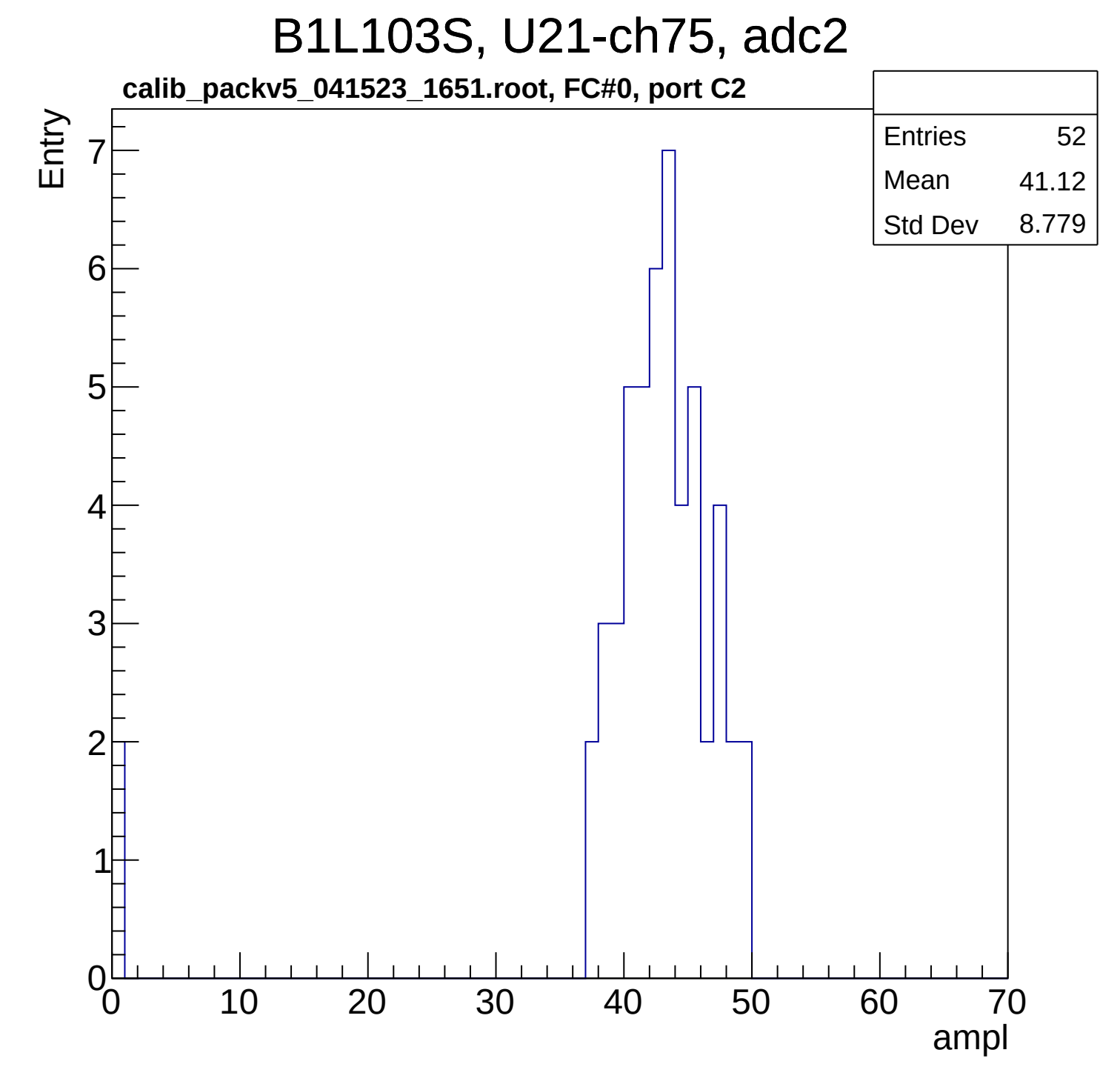

B1L103S, U21-ch75, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 30.99
Std Dev 13.36
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch75, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 41.12
Std Dev 8.779
Entry
ampl
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1
2
3
4
5
6
7
0
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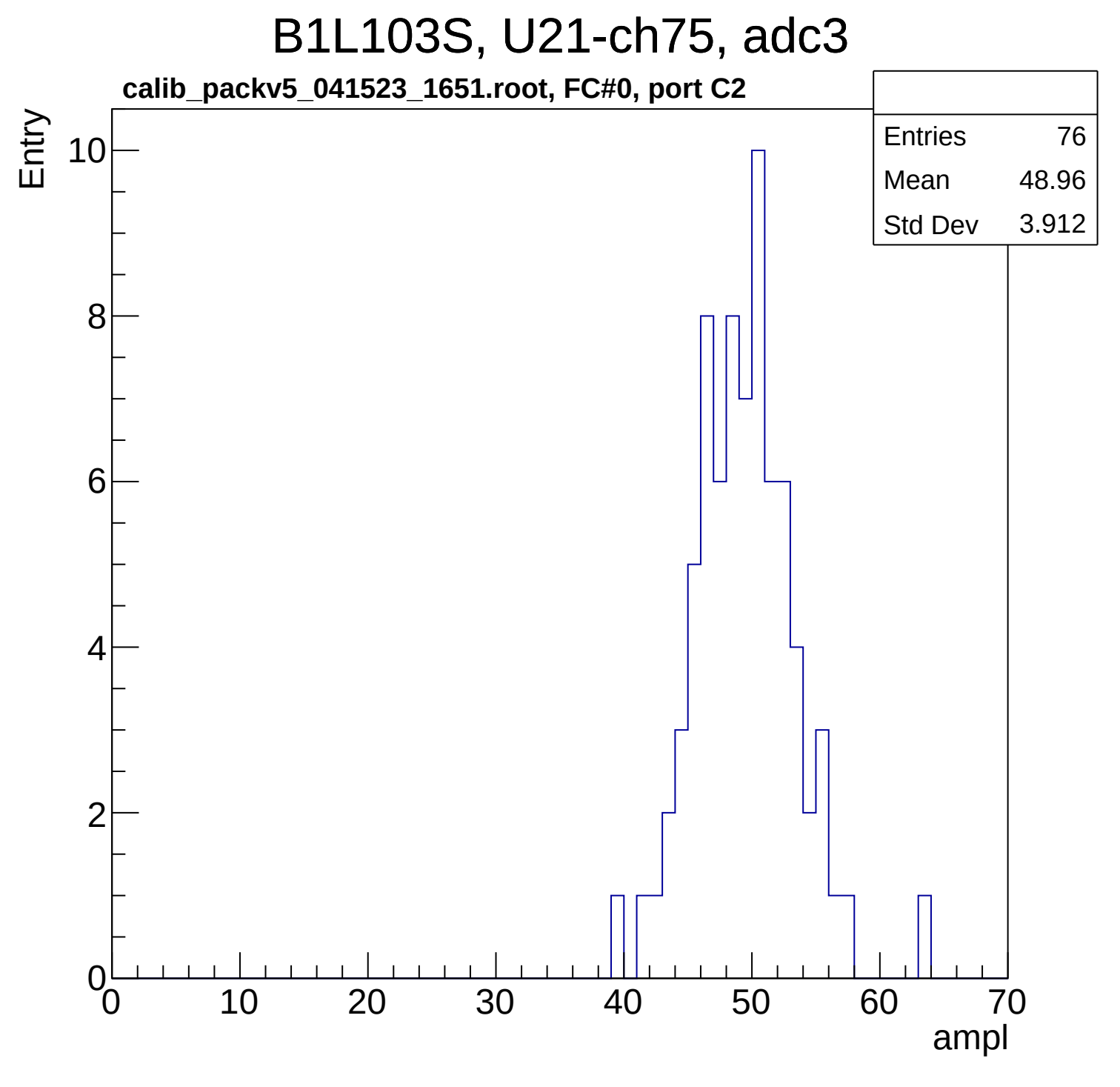
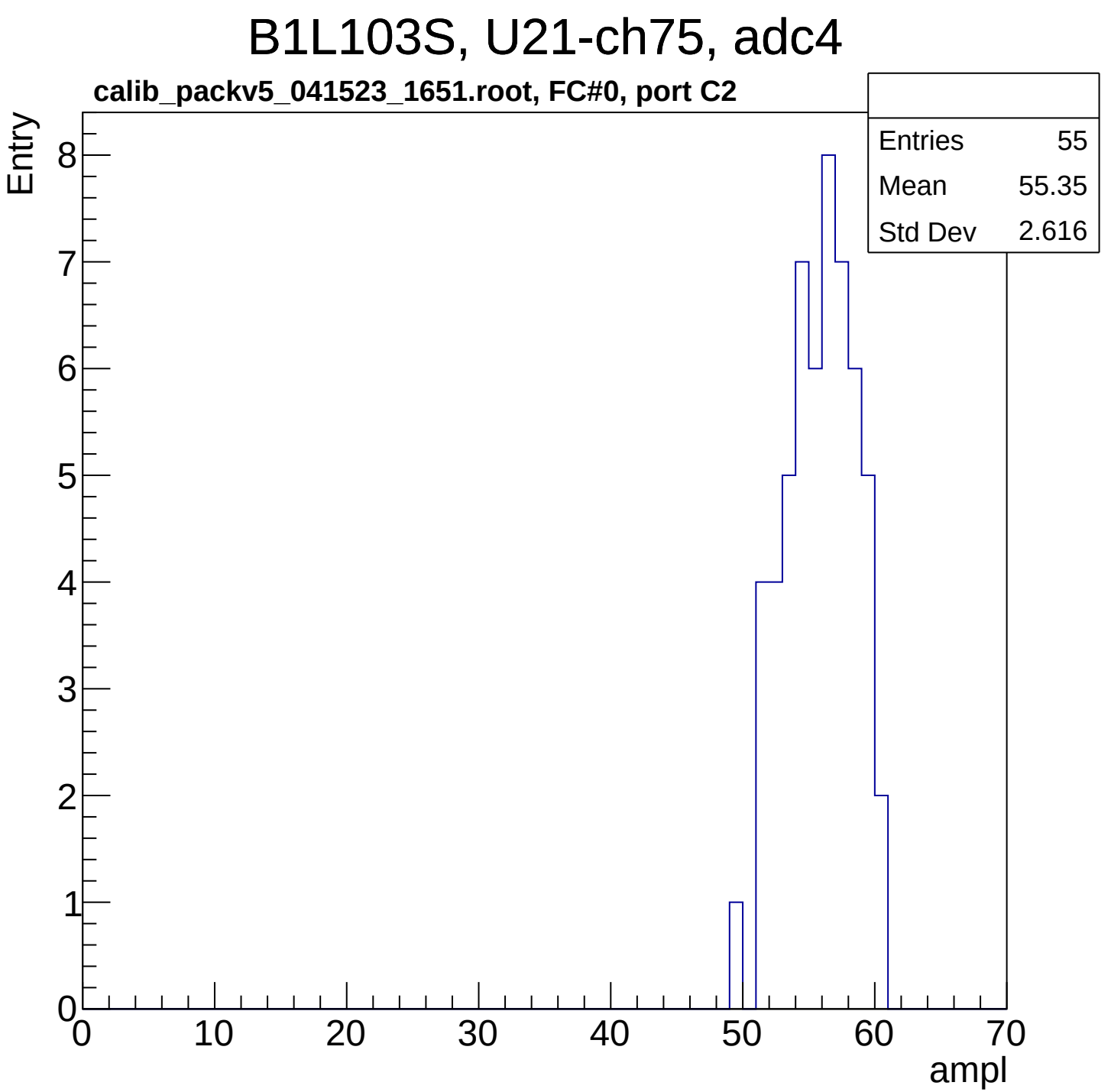
20
30
40
50
60
70


B1L103S, U21-ch75, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 48.96
Std Dev 3.912
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch75, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 55.35
Std Dev 2.616
Entry
ampl
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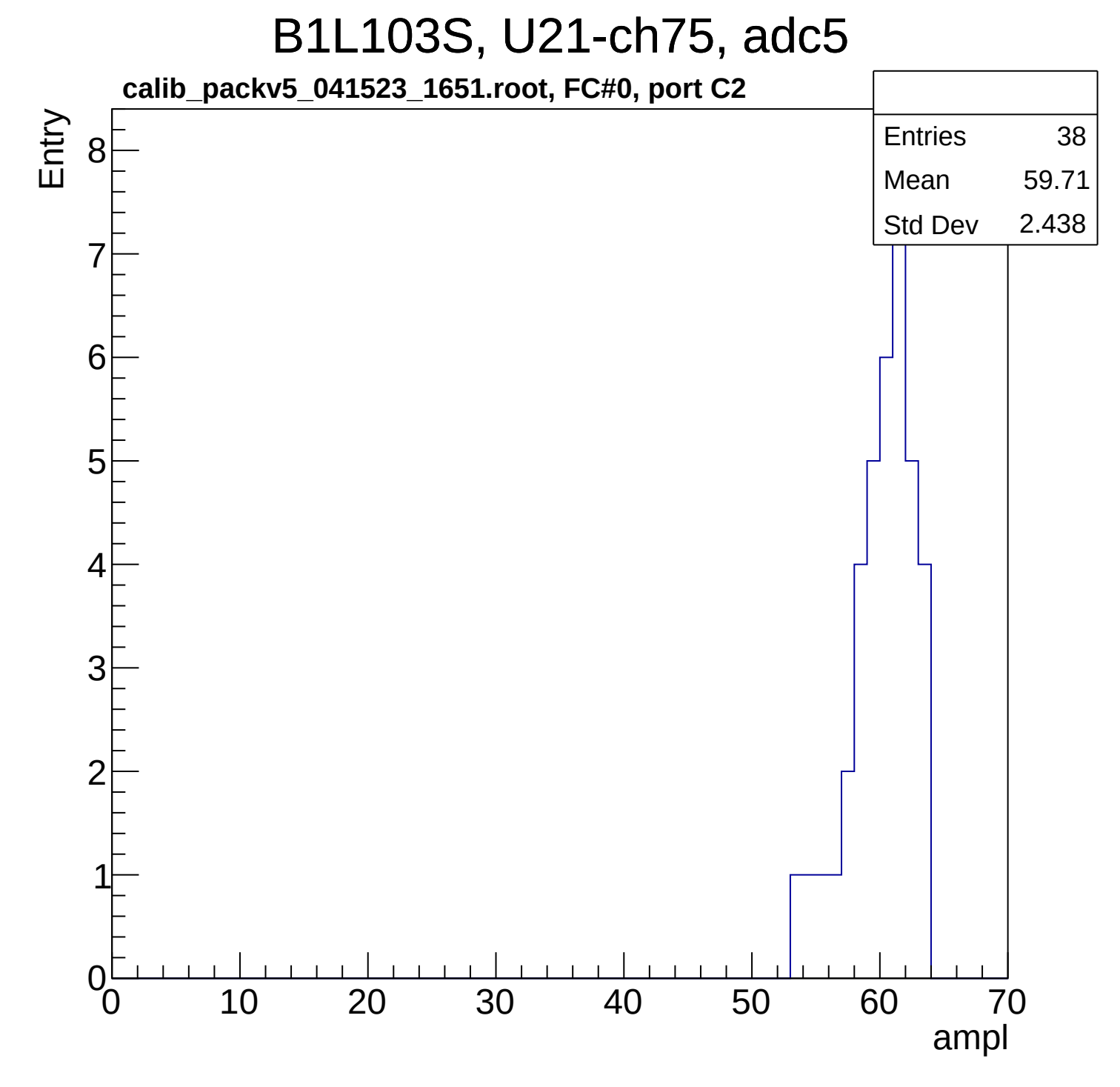
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch75, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 59.71
Std Dev 2.438
Entry
ampl
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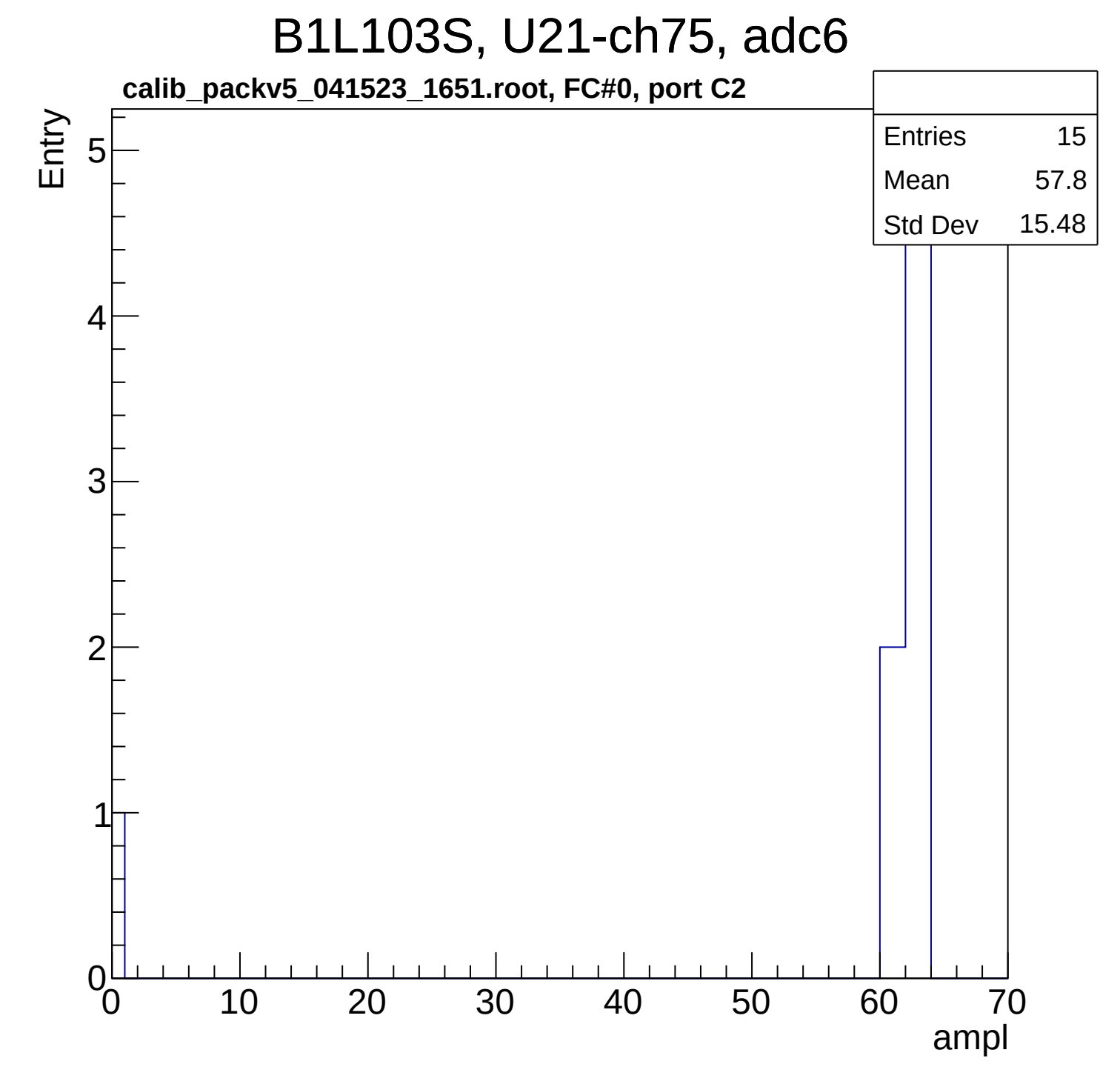
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch75, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 57.8
Std Dev 15.48
Entry
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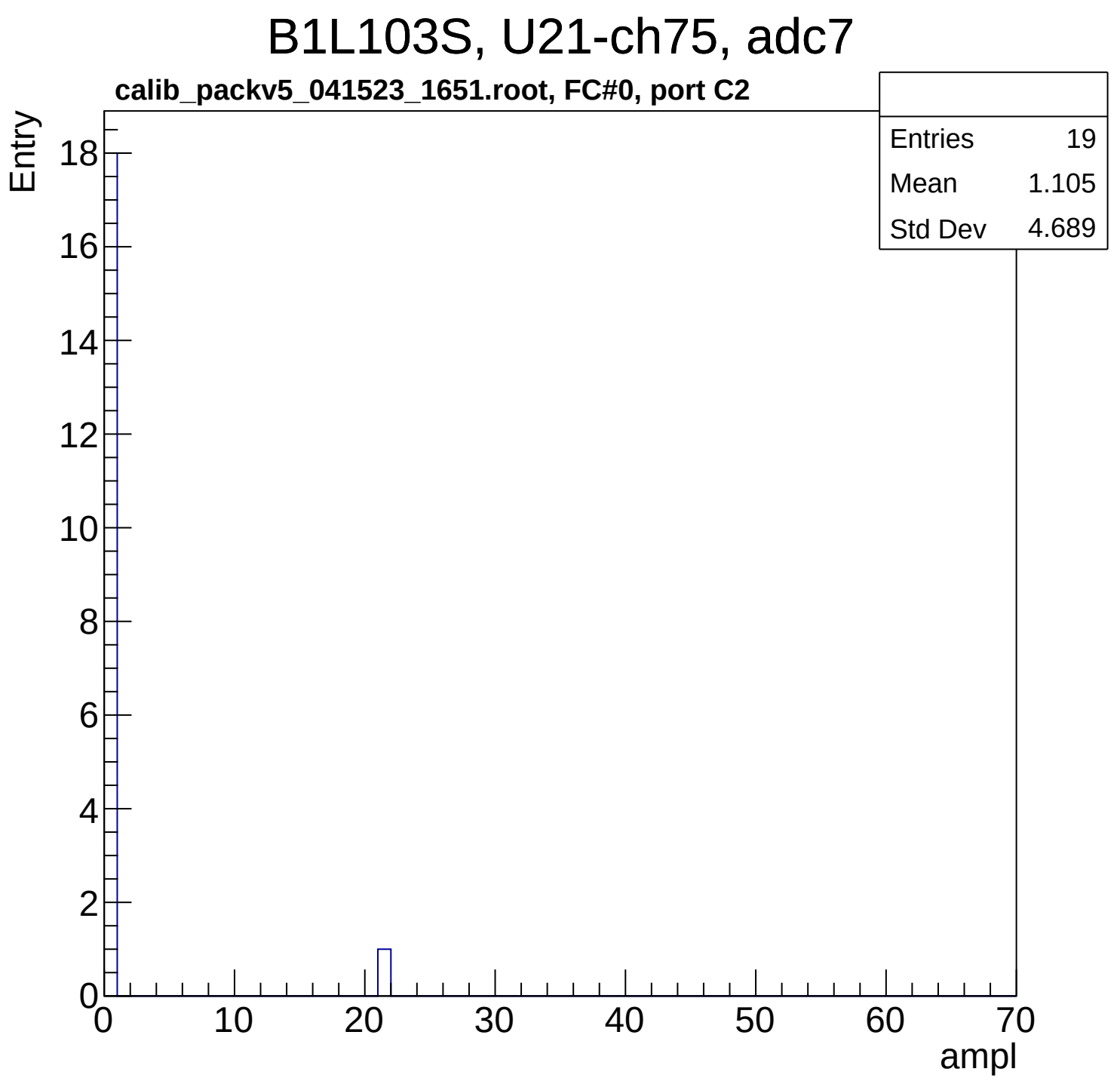
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch75, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.105
Std Dev 4.689
Entry
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6
8
10
12
14
16
18
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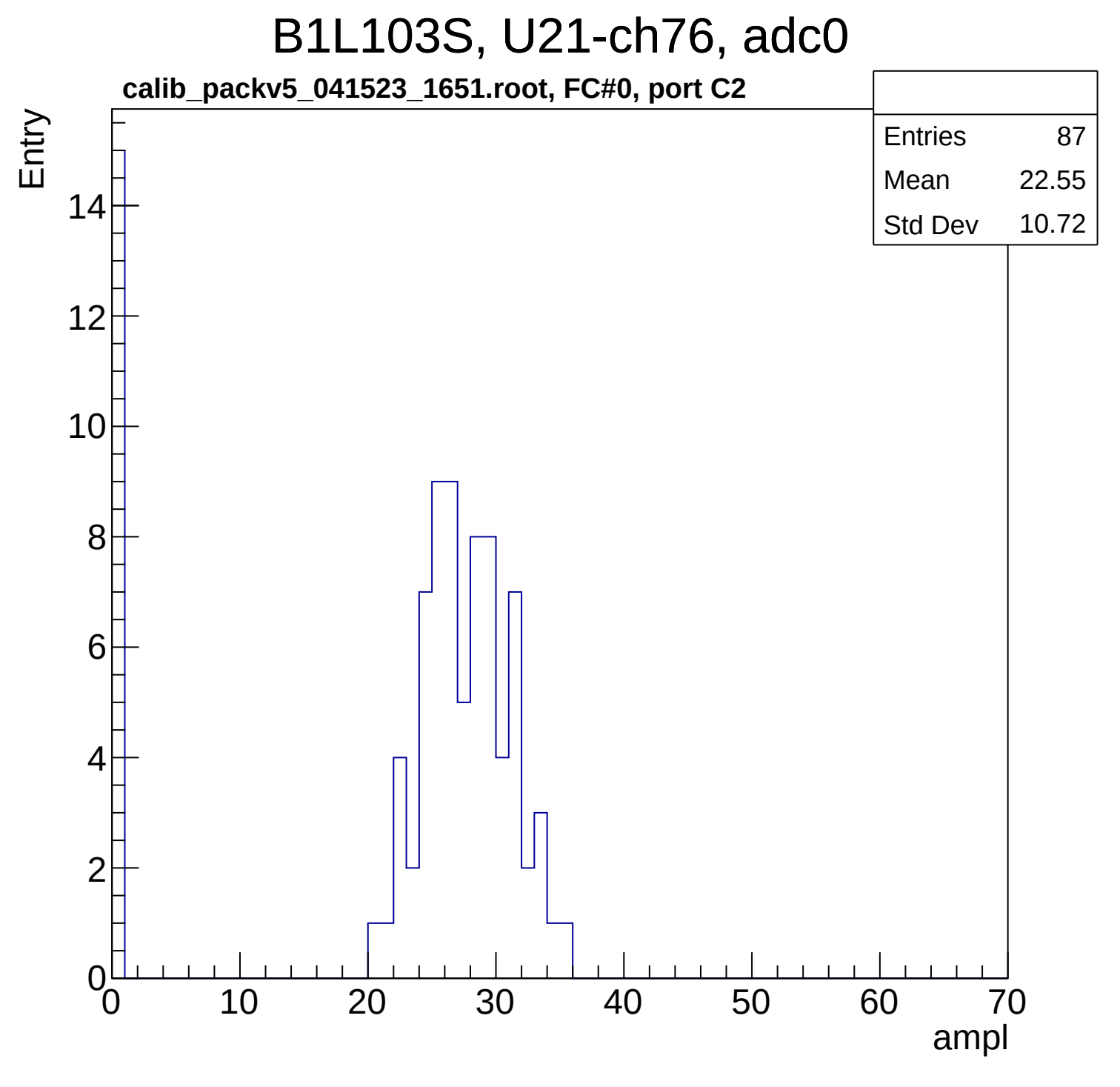
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch76, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 22.55
Std Dev 10.72
Entry
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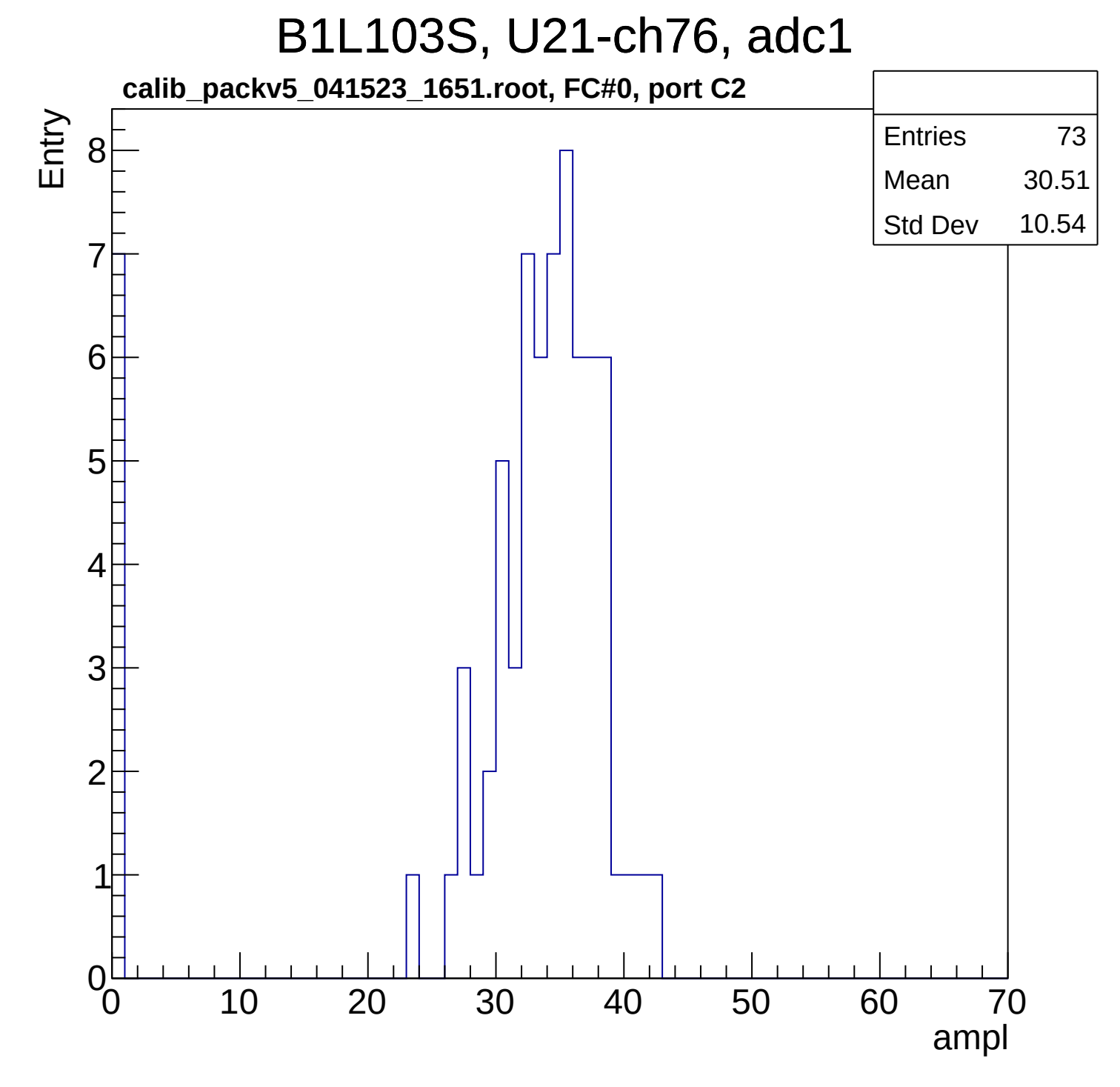
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch76, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 30.51
Std Dev 10.54
Entry
ampl
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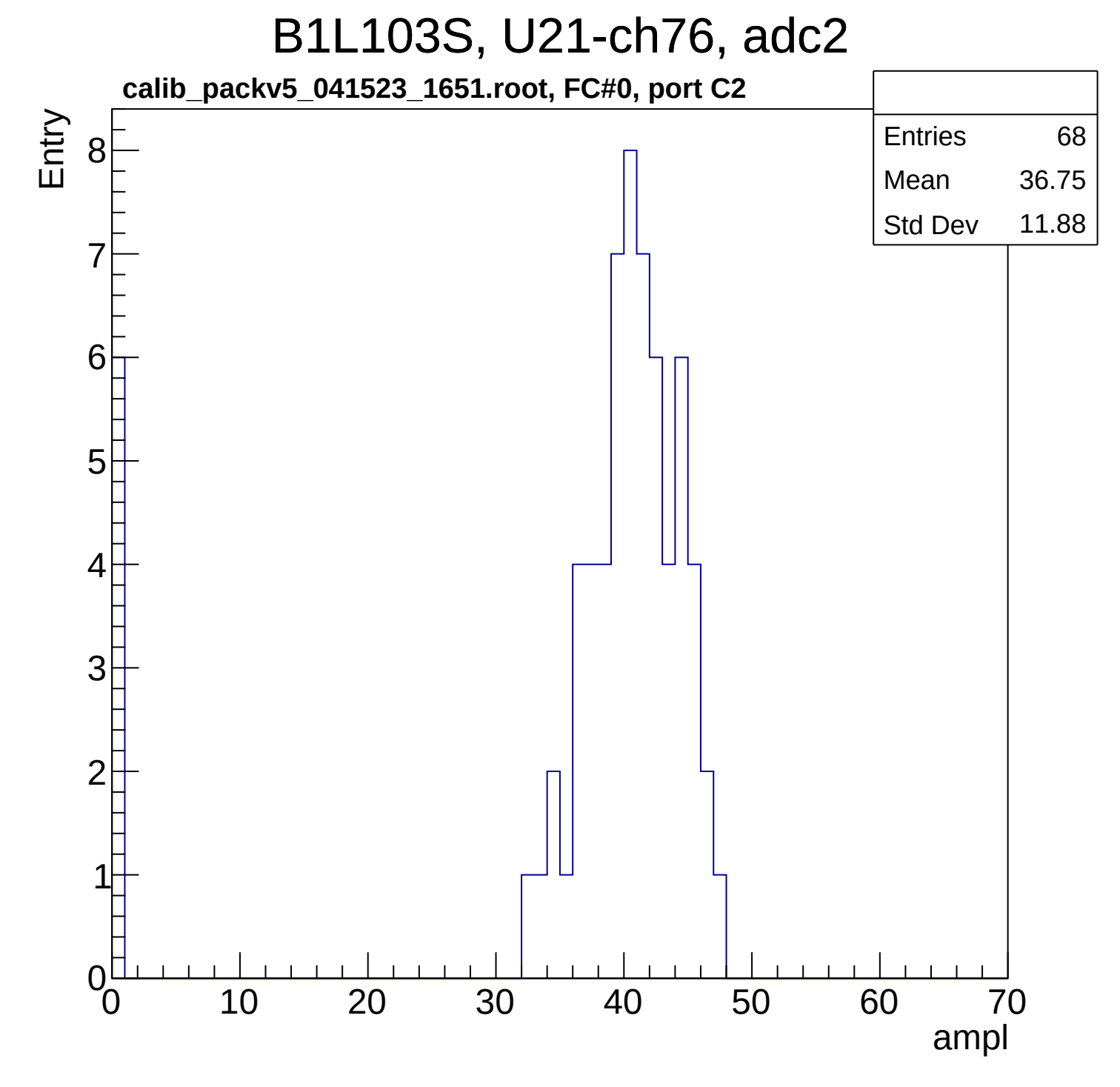
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch76, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 36.75
Std Dev 11.88
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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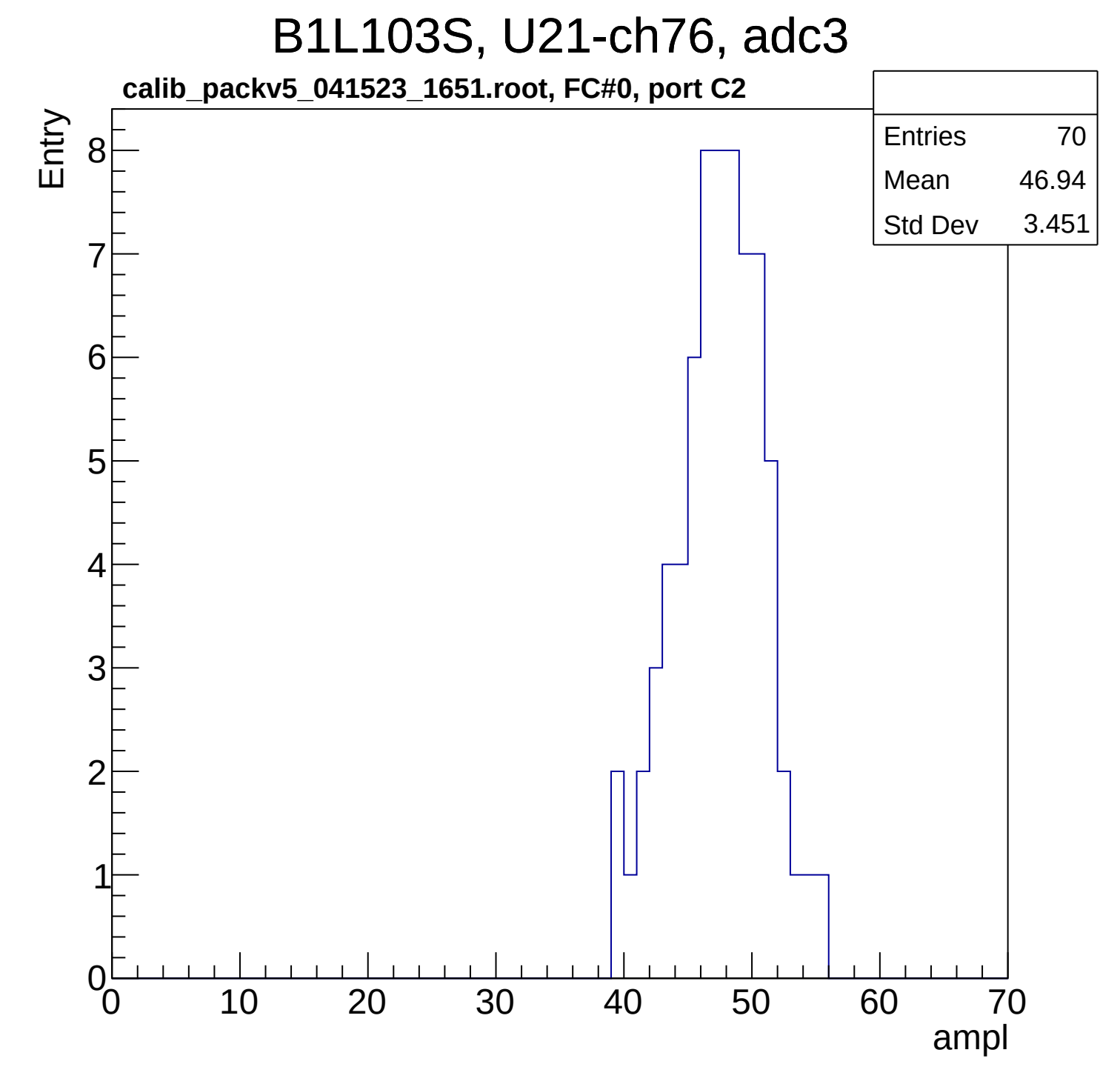
40
50
60
70


B1L103S, U21-ch76, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 46.94
Std Dev 3.451
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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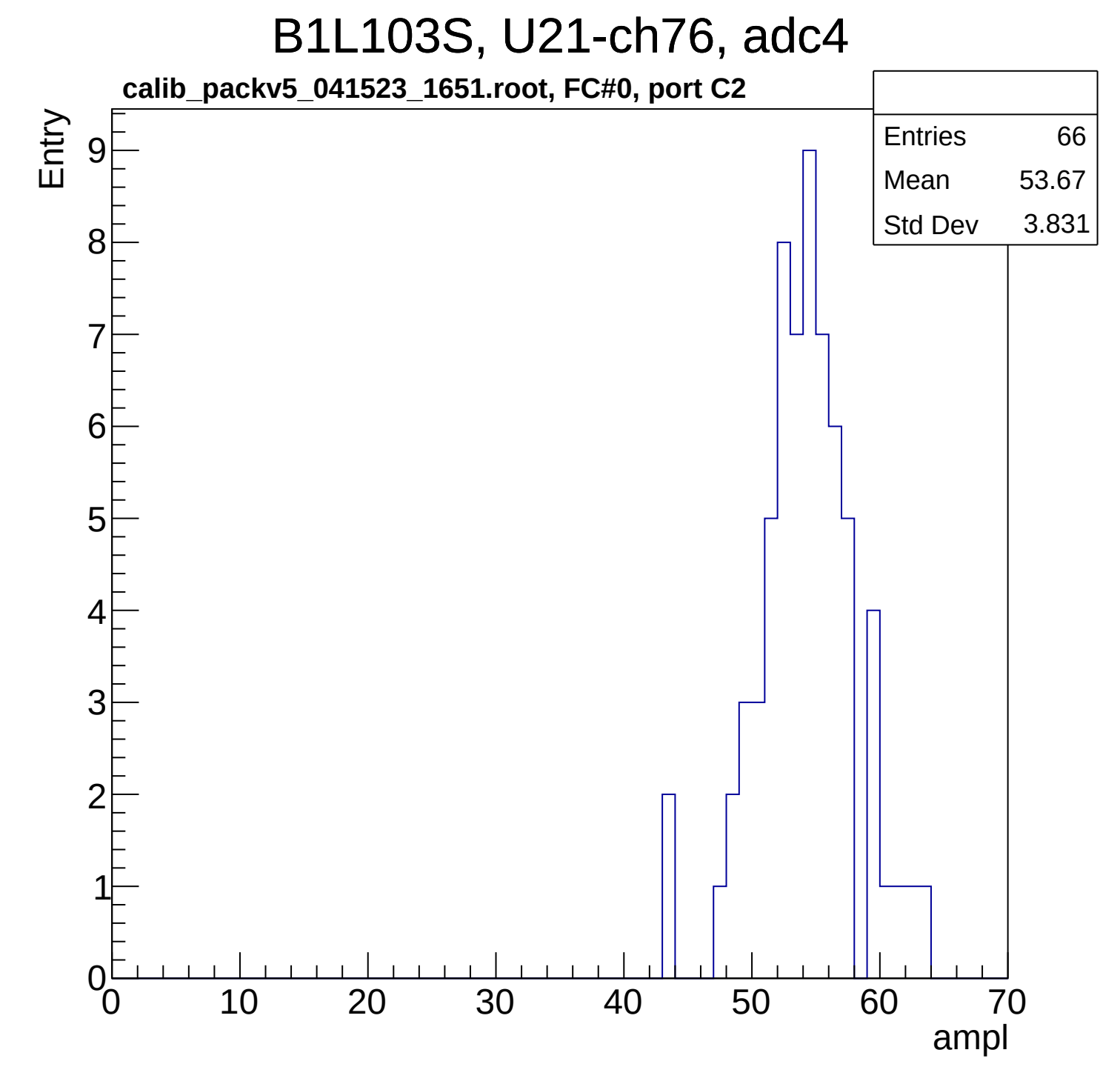
40
50
60
70


B1L103S, U21-ch76, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 53.67
Std Dev 3.831
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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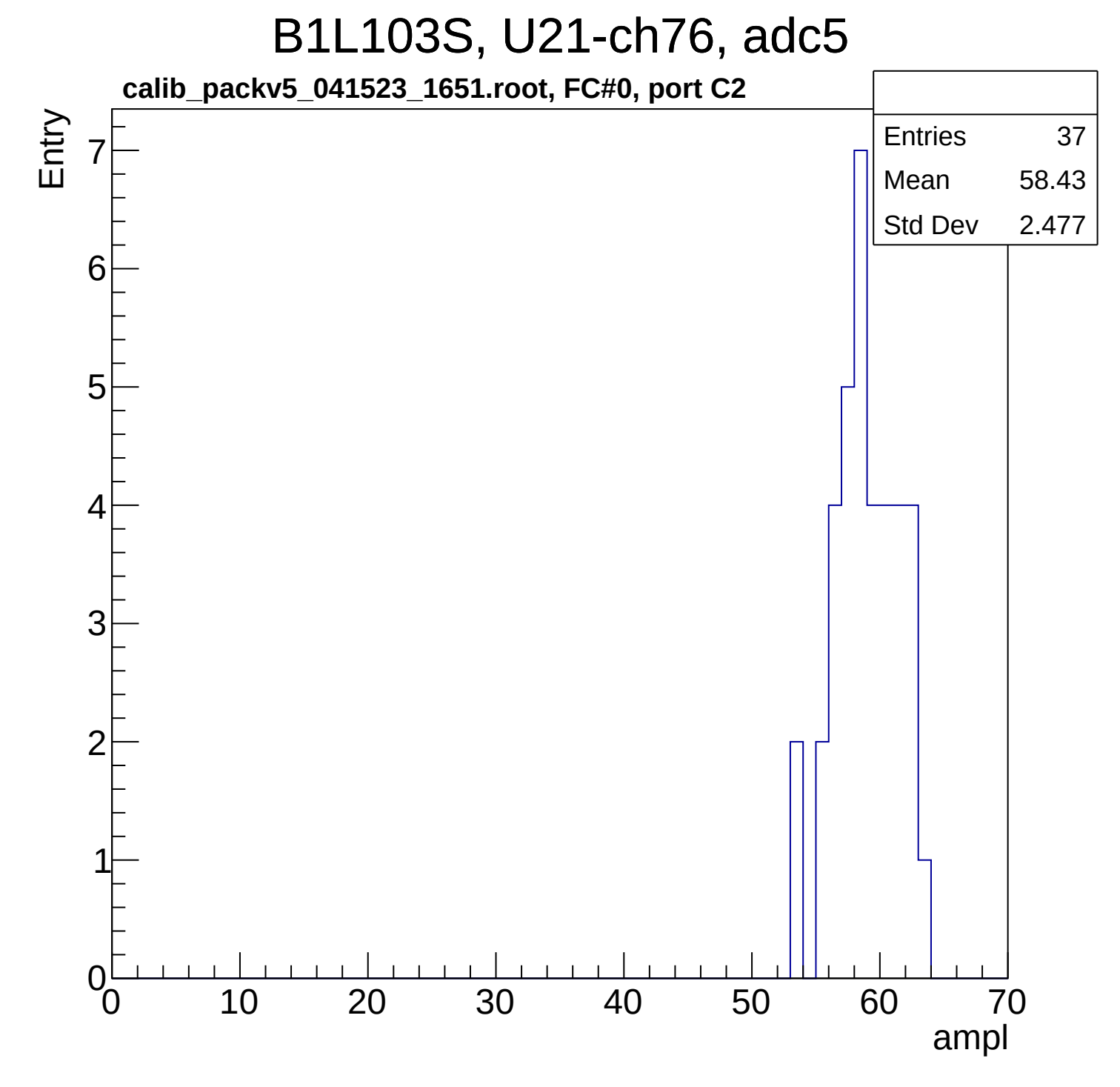
40
50
60
70


B1L103S, U21-ch76, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 58.43
Std Dev 2.477
Entry
ampl
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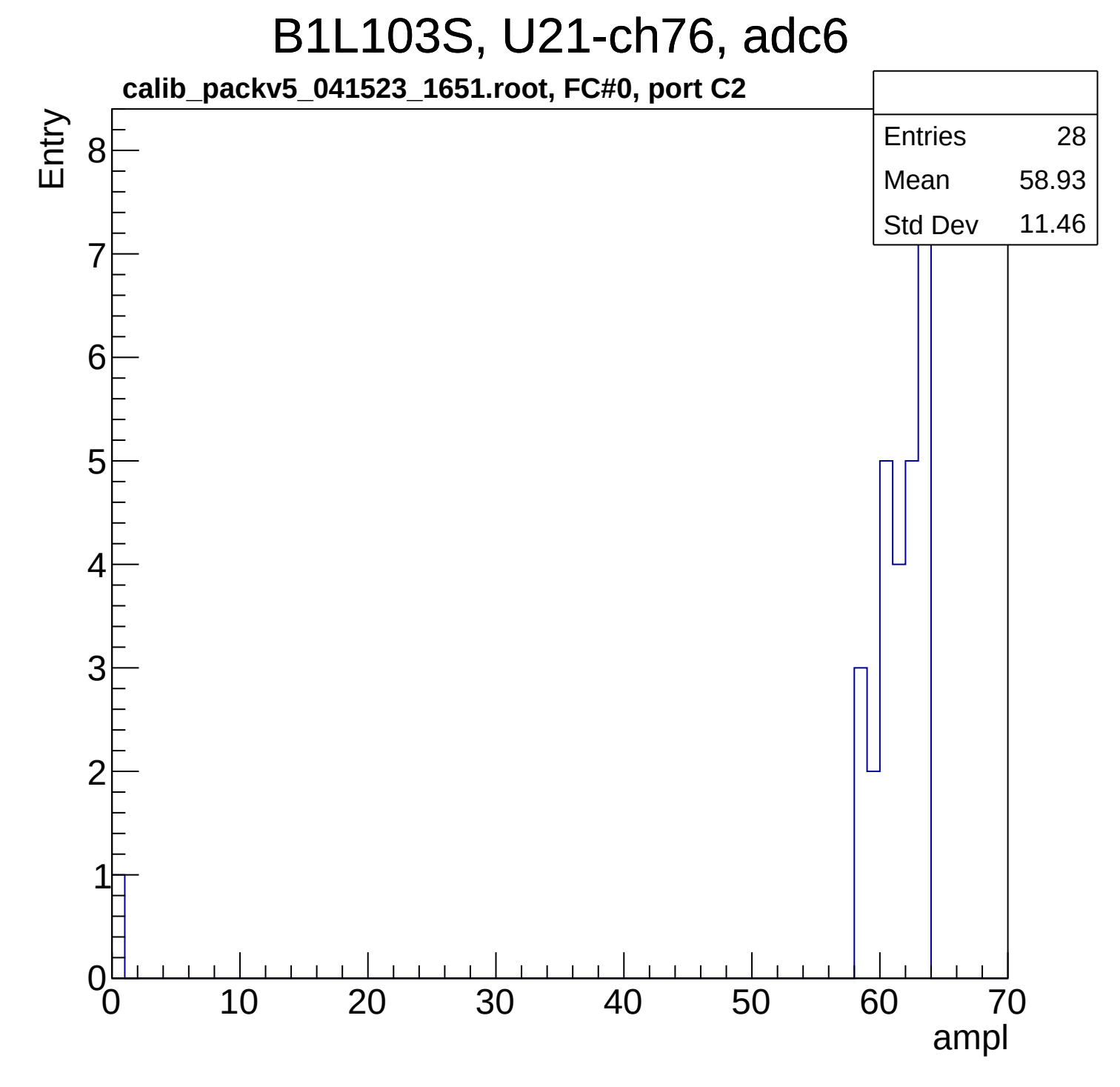
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U21-ch76, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 58.93
Std Dev 11.46
Entry
ampl
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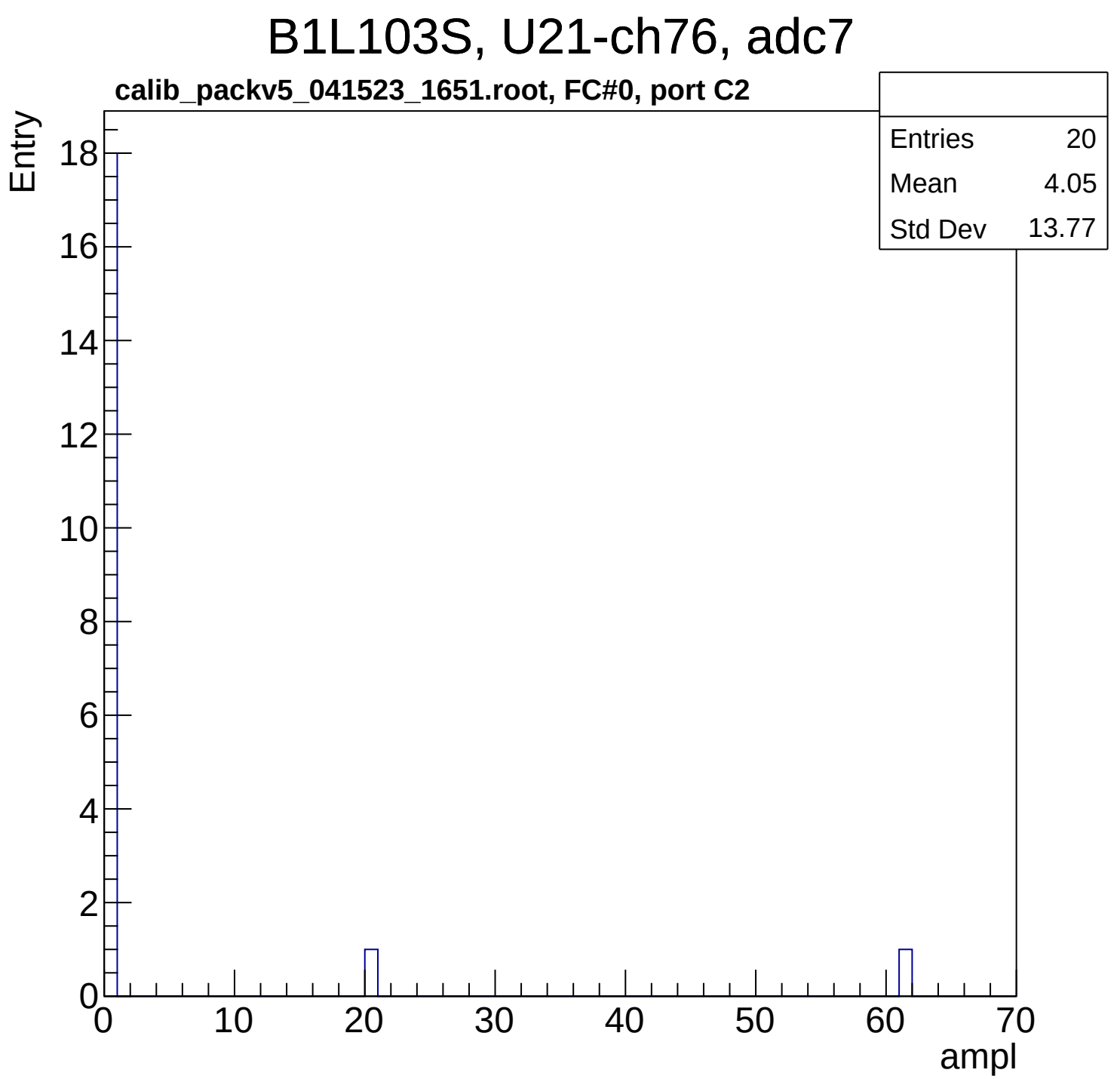
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch76, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4.05
Std Dev 13.77
Entry
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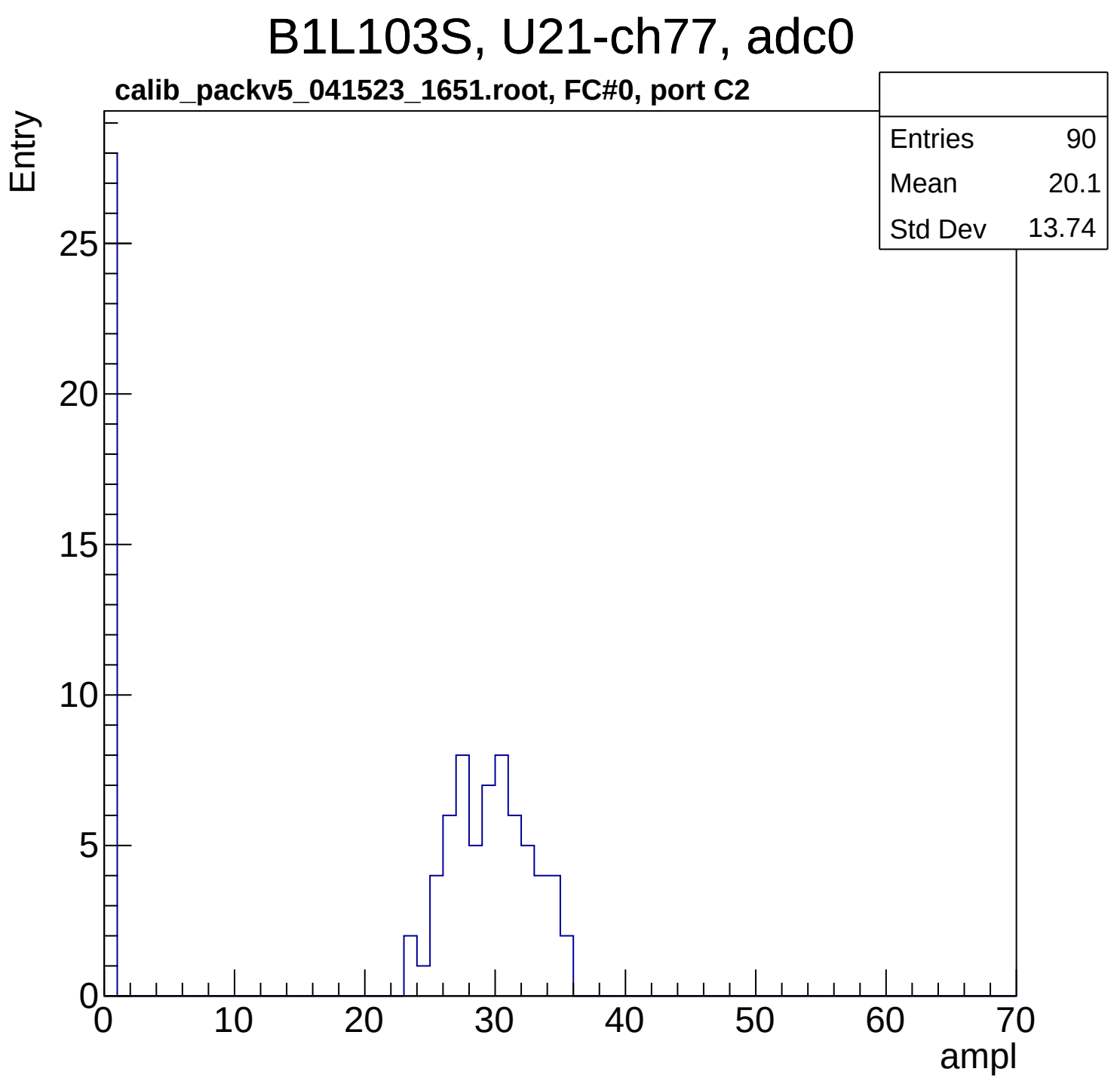
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch77, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 20.1
Std Dev 13.74
Entry
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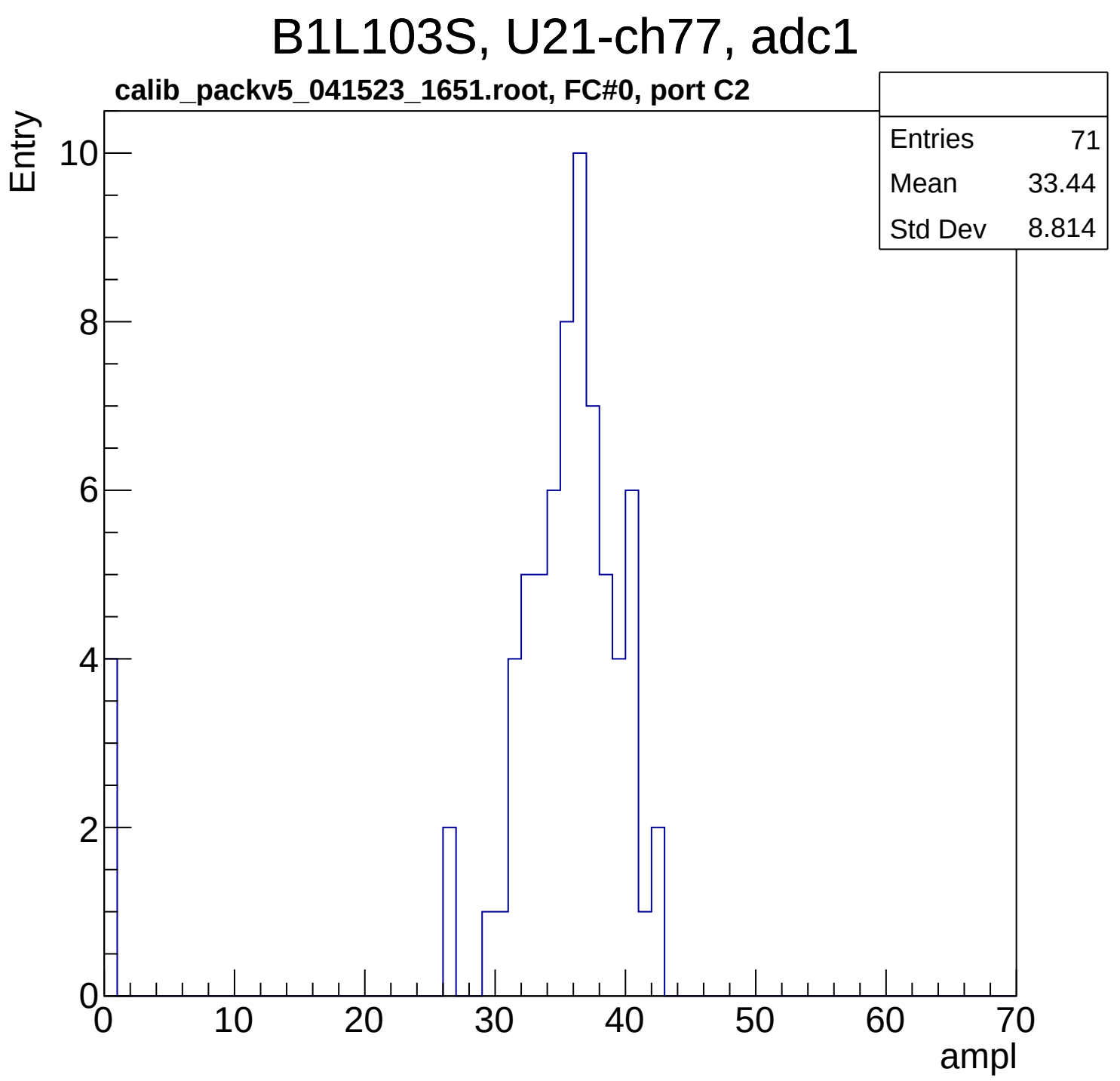
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch77, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 33.44
Std Dev 8.814
Entry
ampl
0
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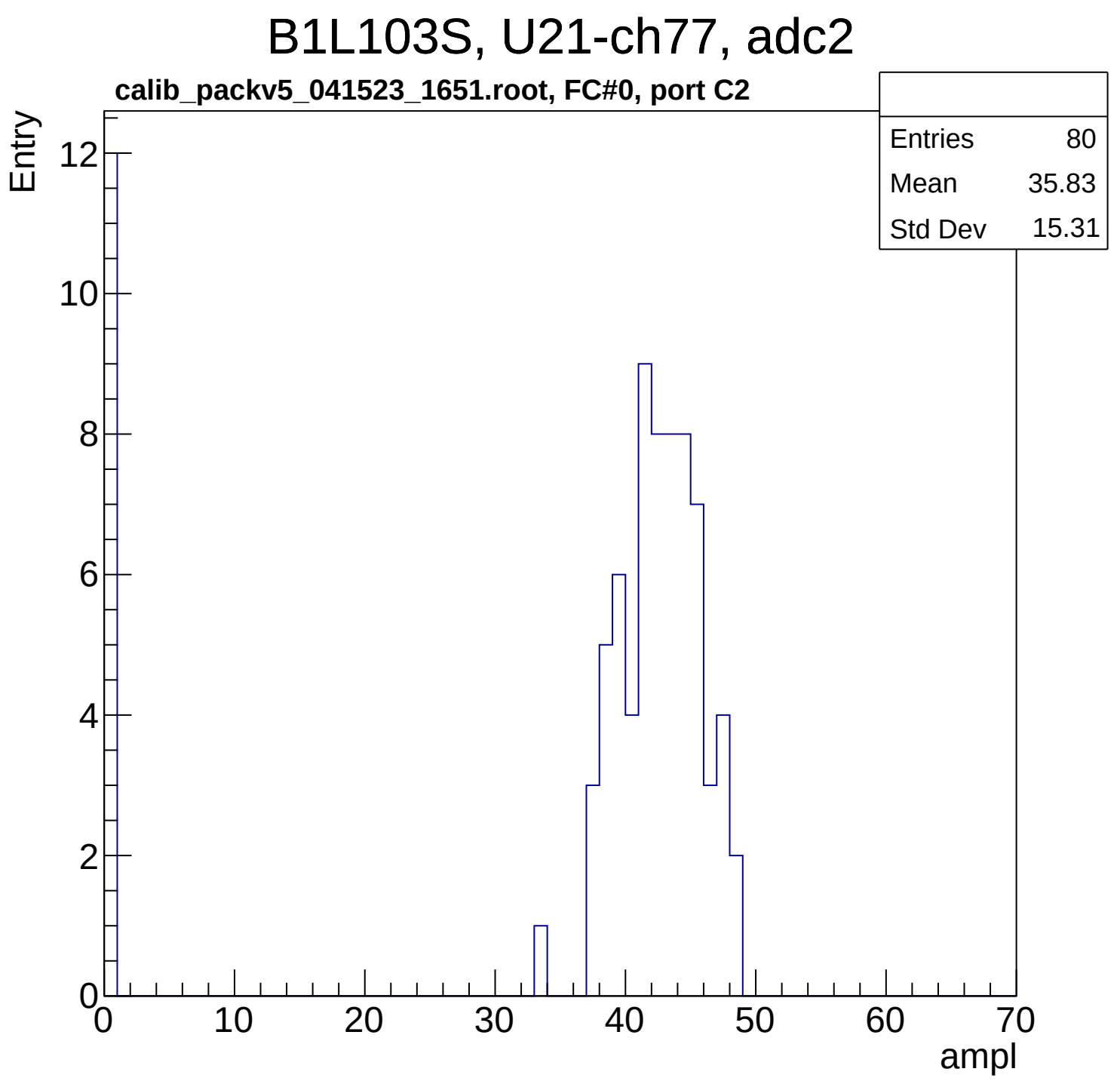
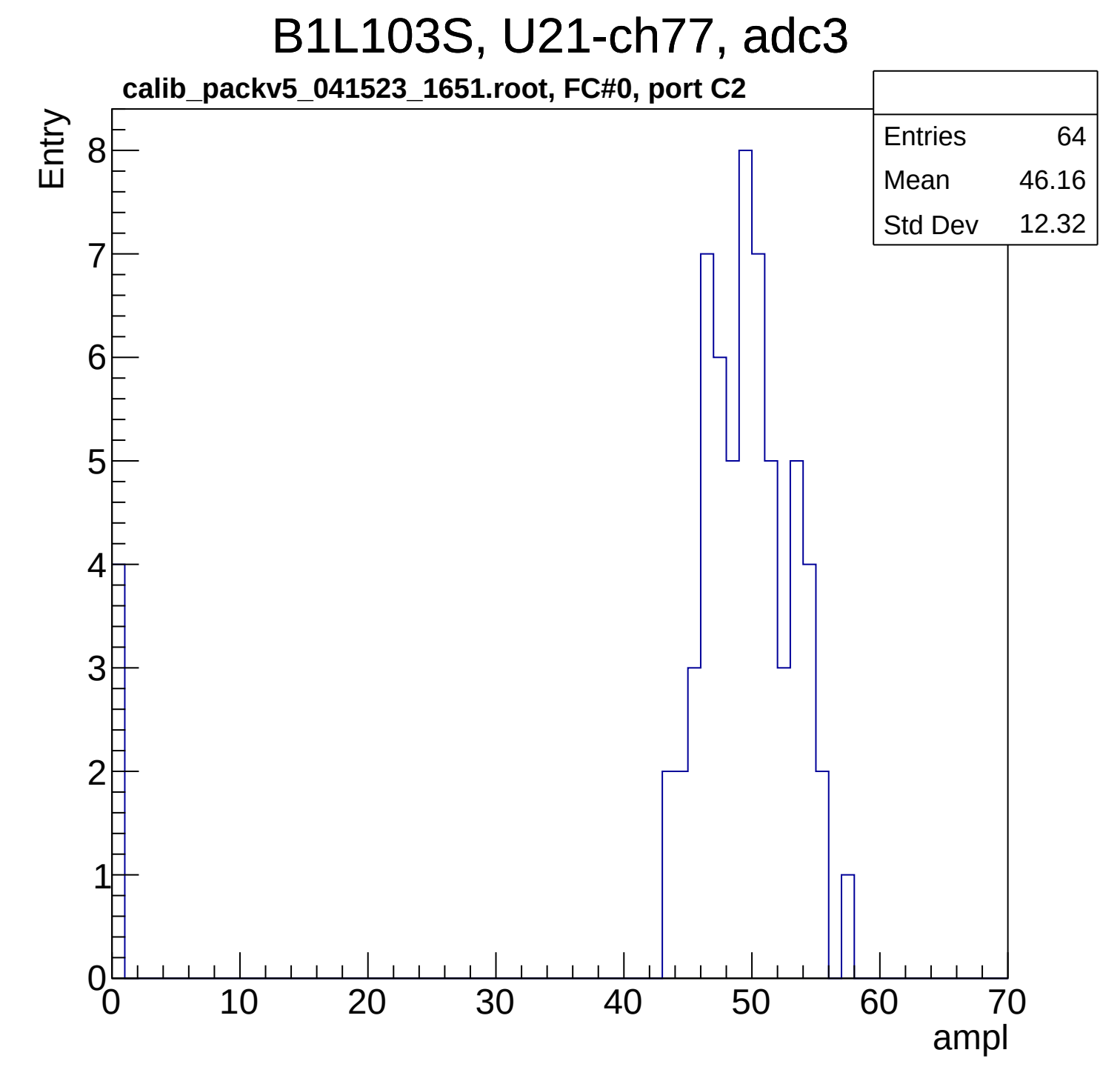
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U21-ch77, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 35.83
Std Dev 15.31
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch77, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 46.16
Std Dev 12.32
Entry
ampl
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1
2
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4
5
6
7
8
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20
30
40
50
60
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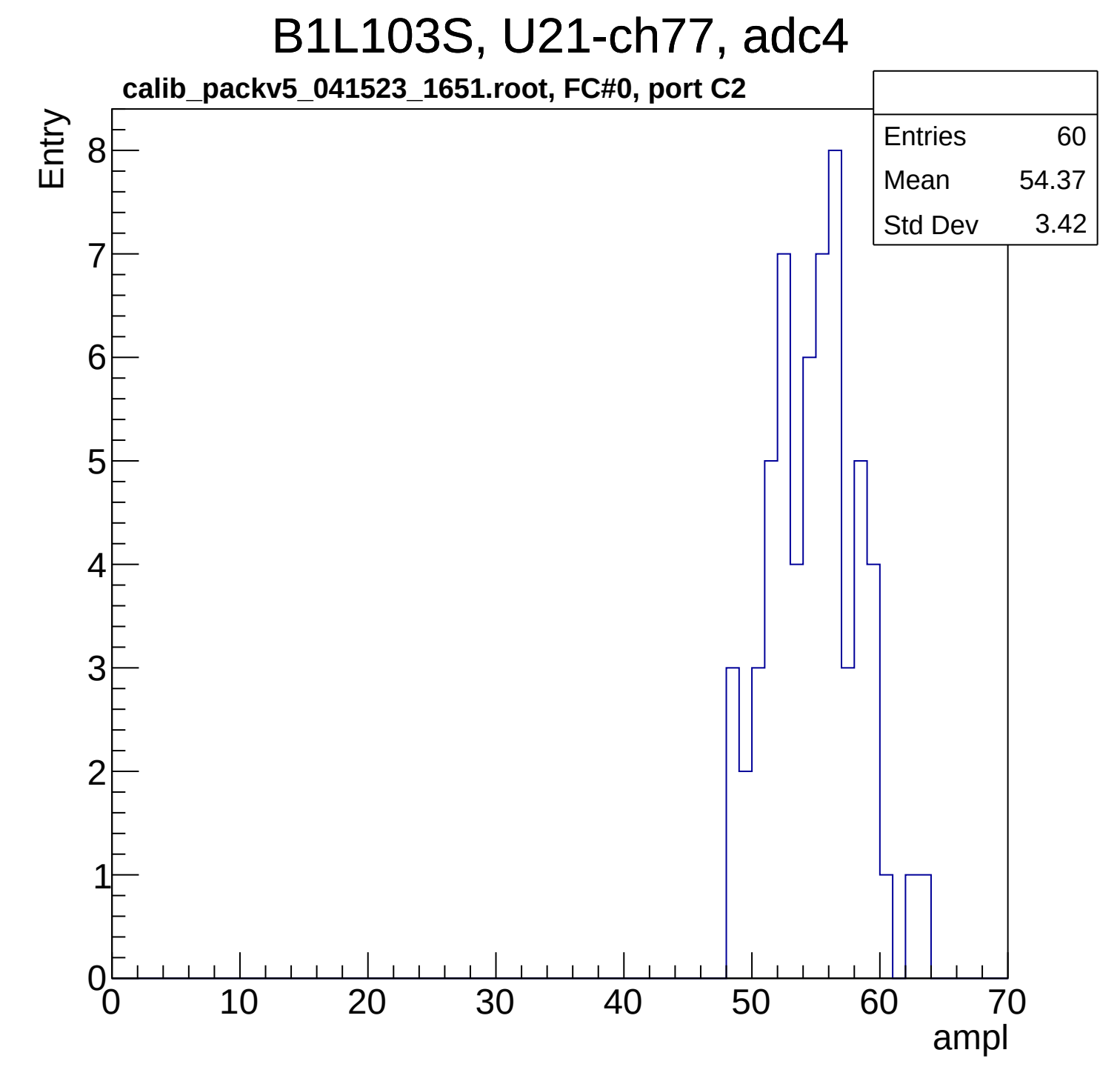
B1L103S, U21-ch77, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 54.37
Std Dev 3.42
Entry
ampl
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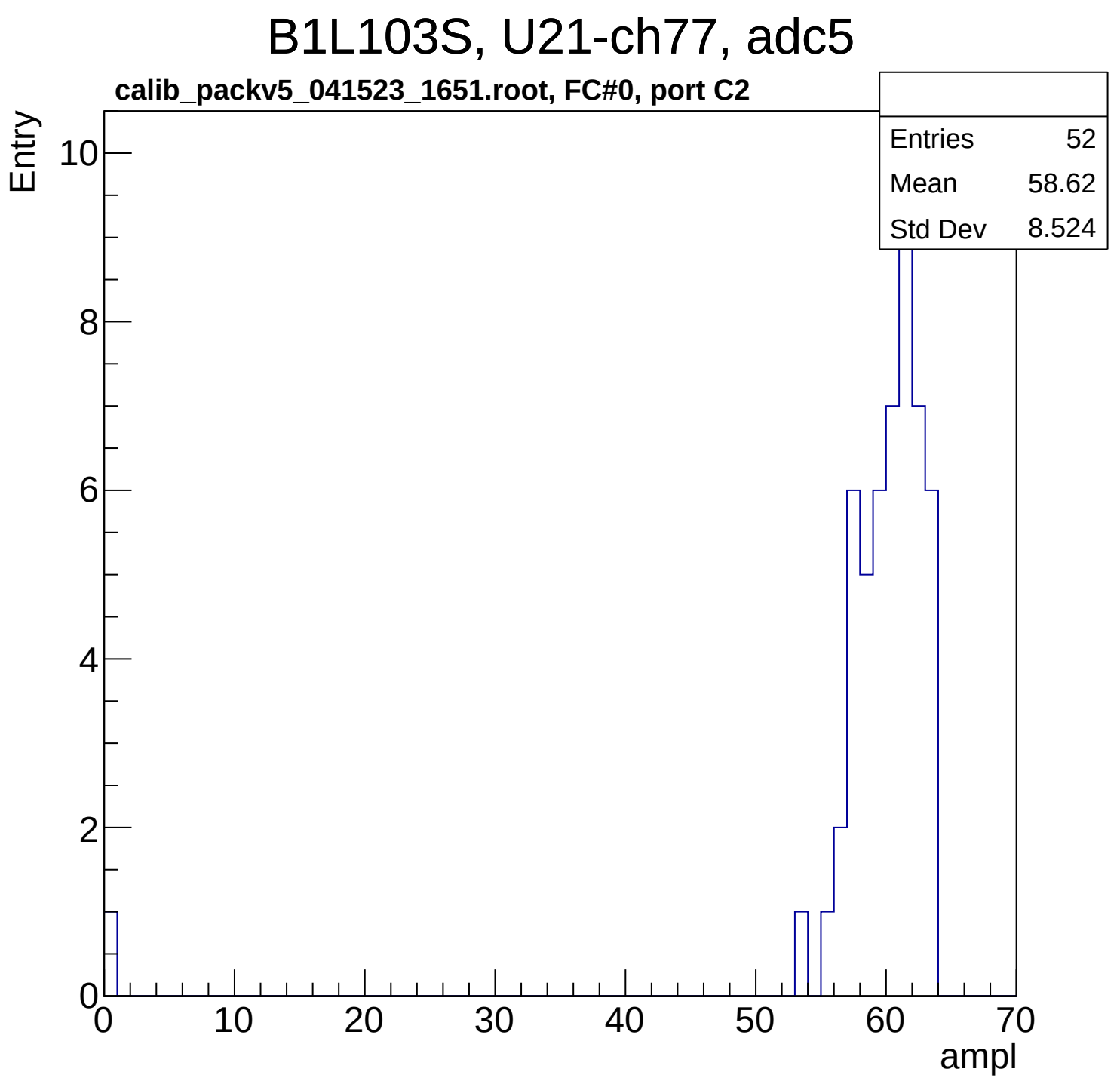
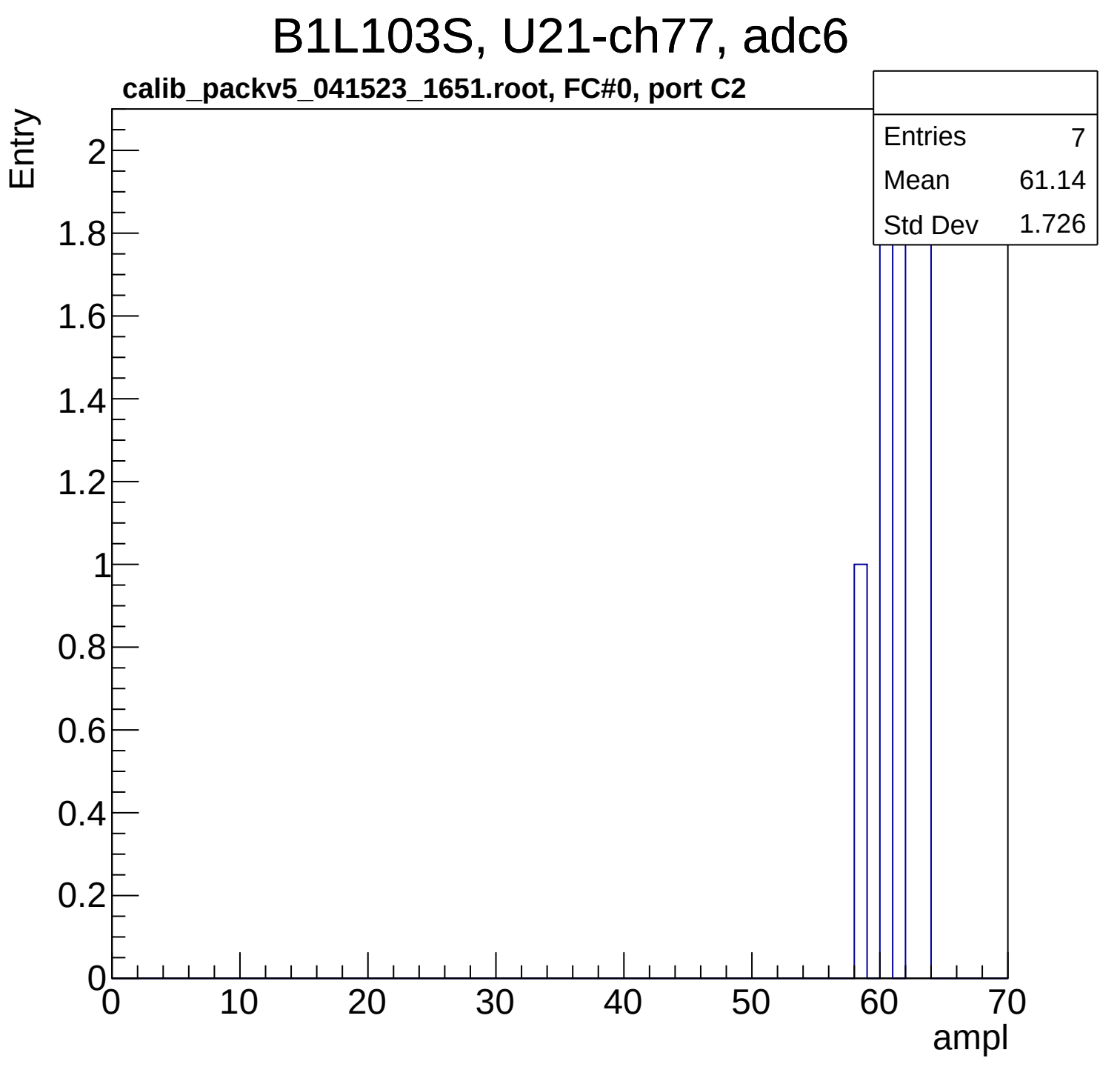
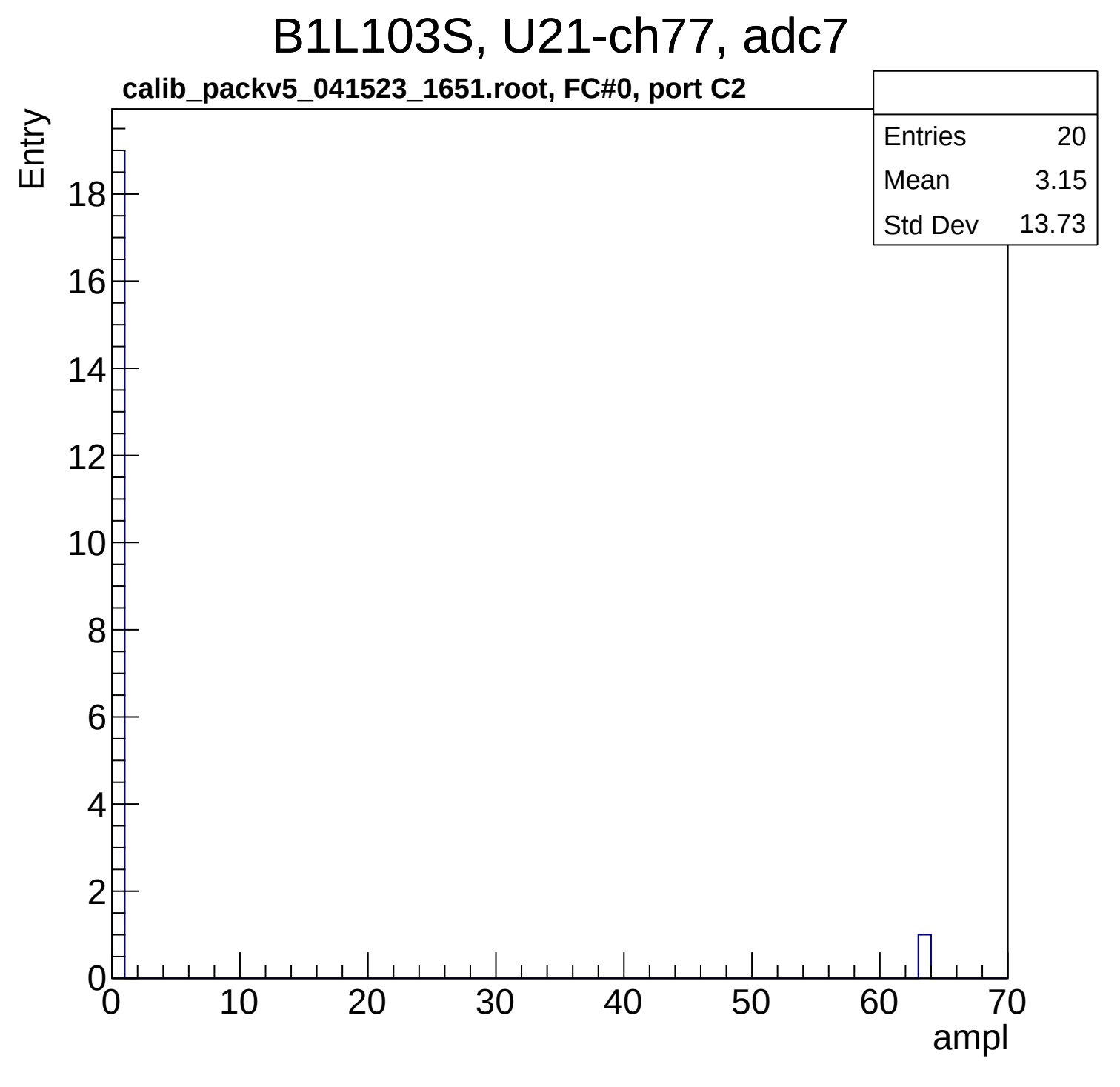
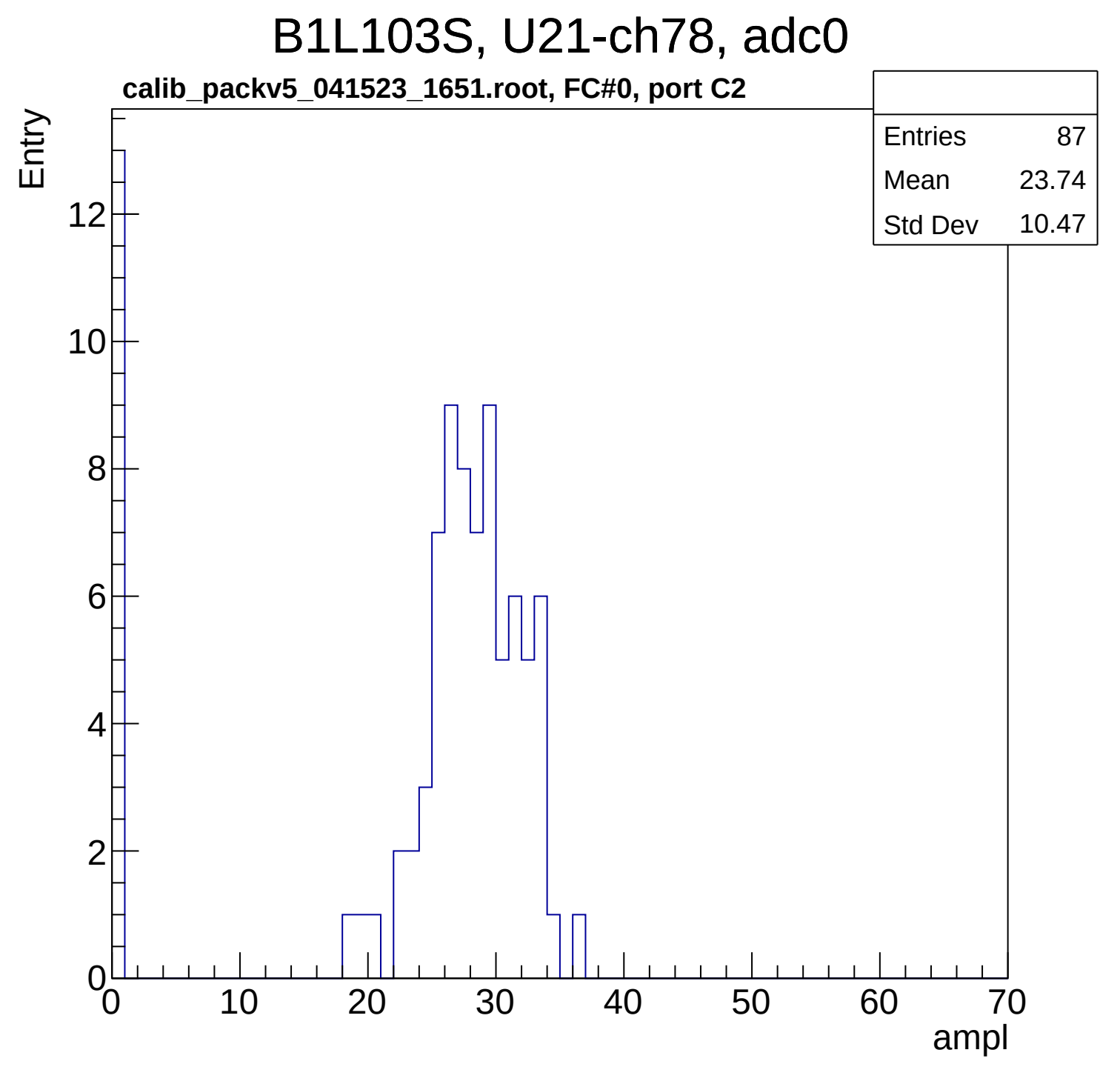
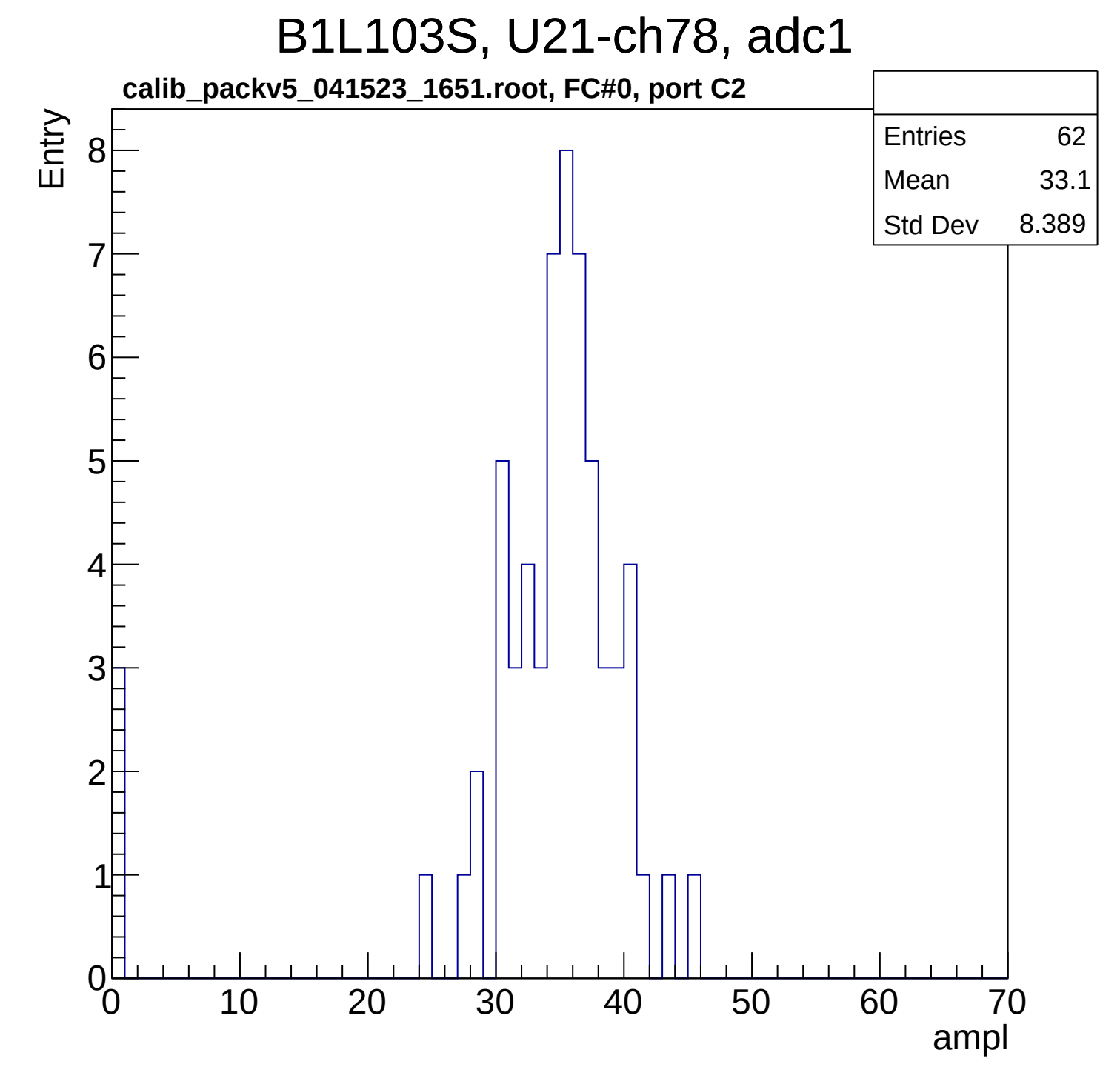
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch77, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 58.62
Std Dev 8.524
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U21-ch77, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 61.14
Std Dev 1.726
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U21-ch77, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch78, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 23.74
Std Dev 10.47
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch78, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 33.1
Std Dev 8.389
Entry
ampl
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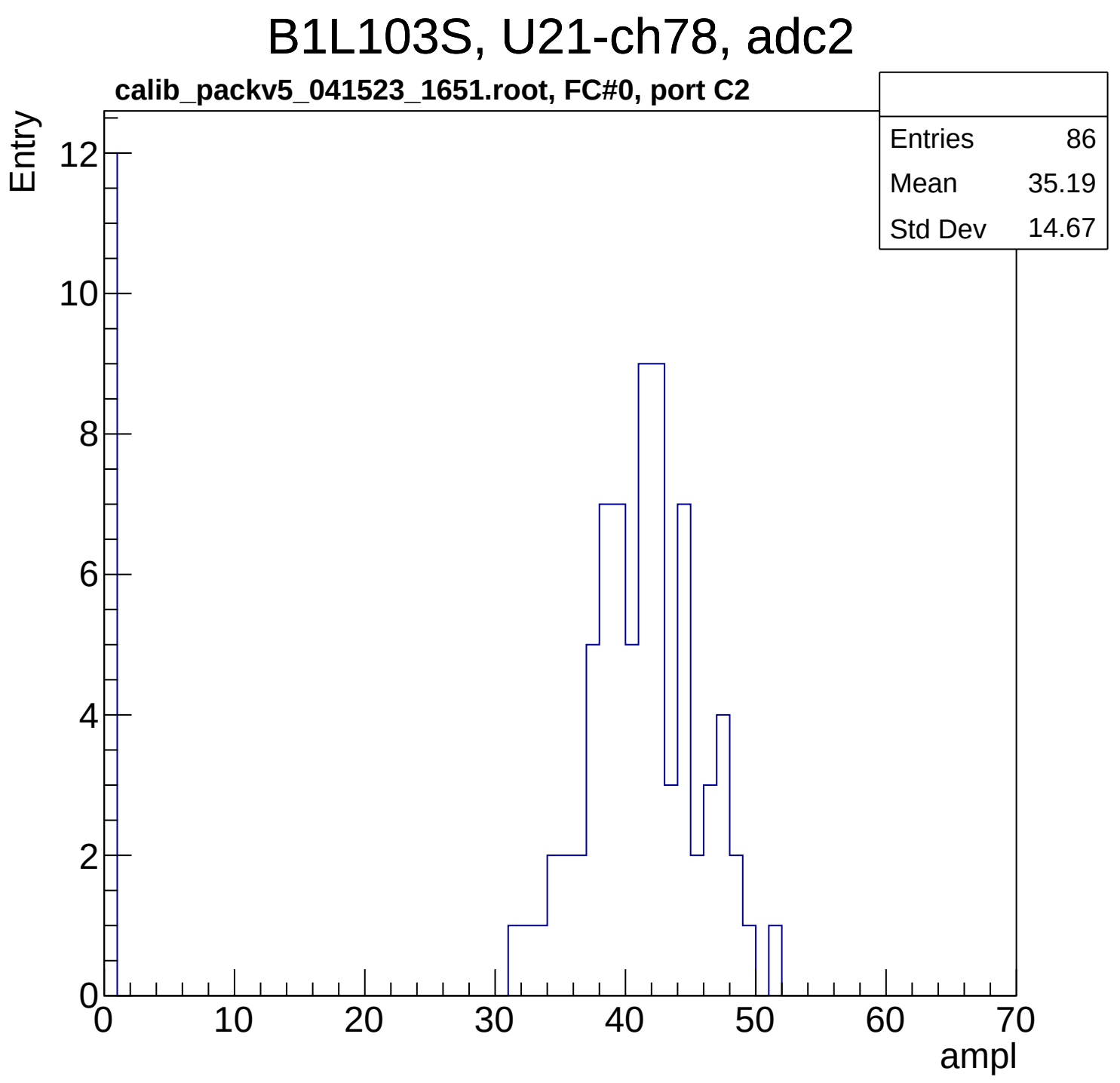
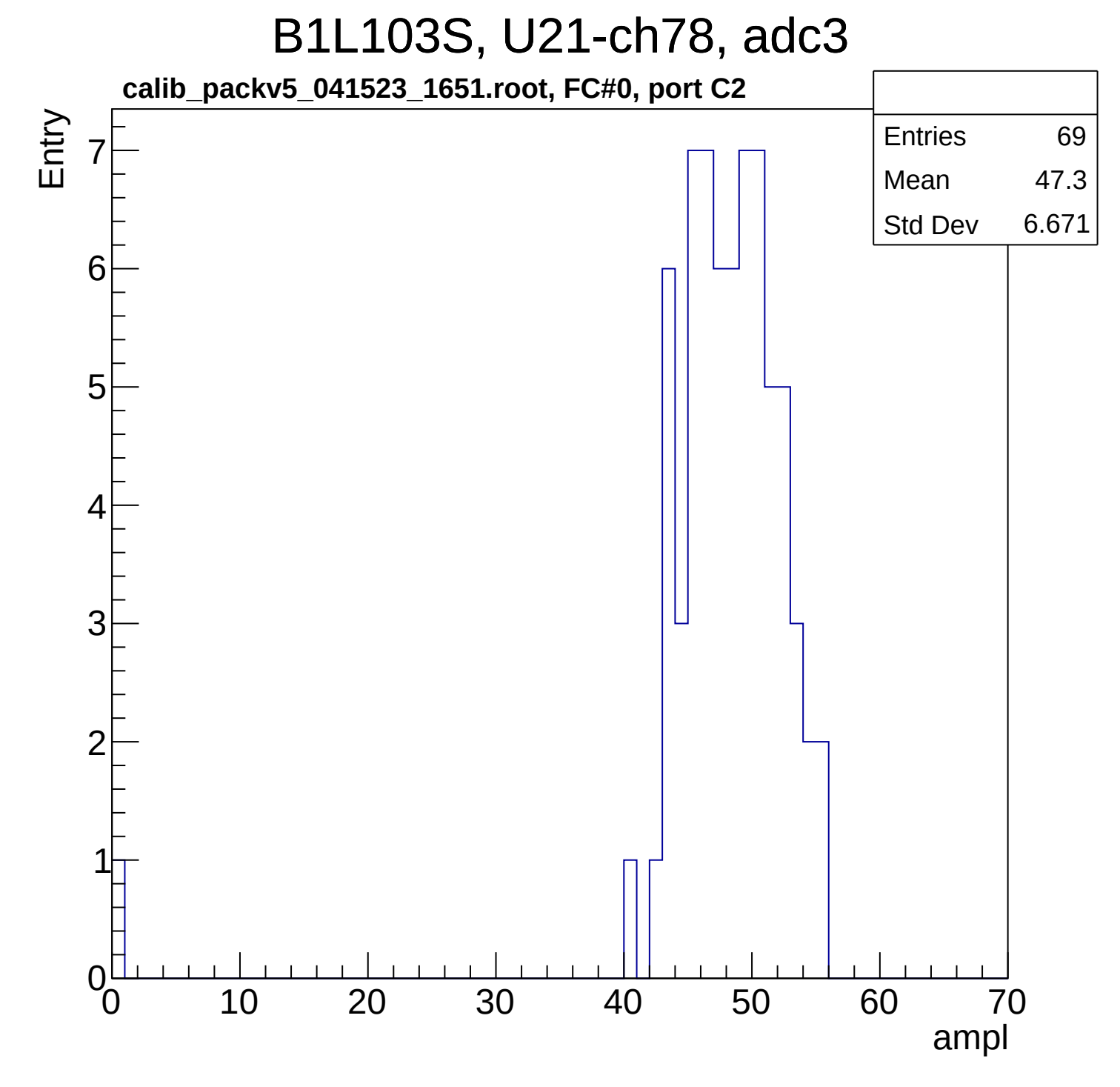
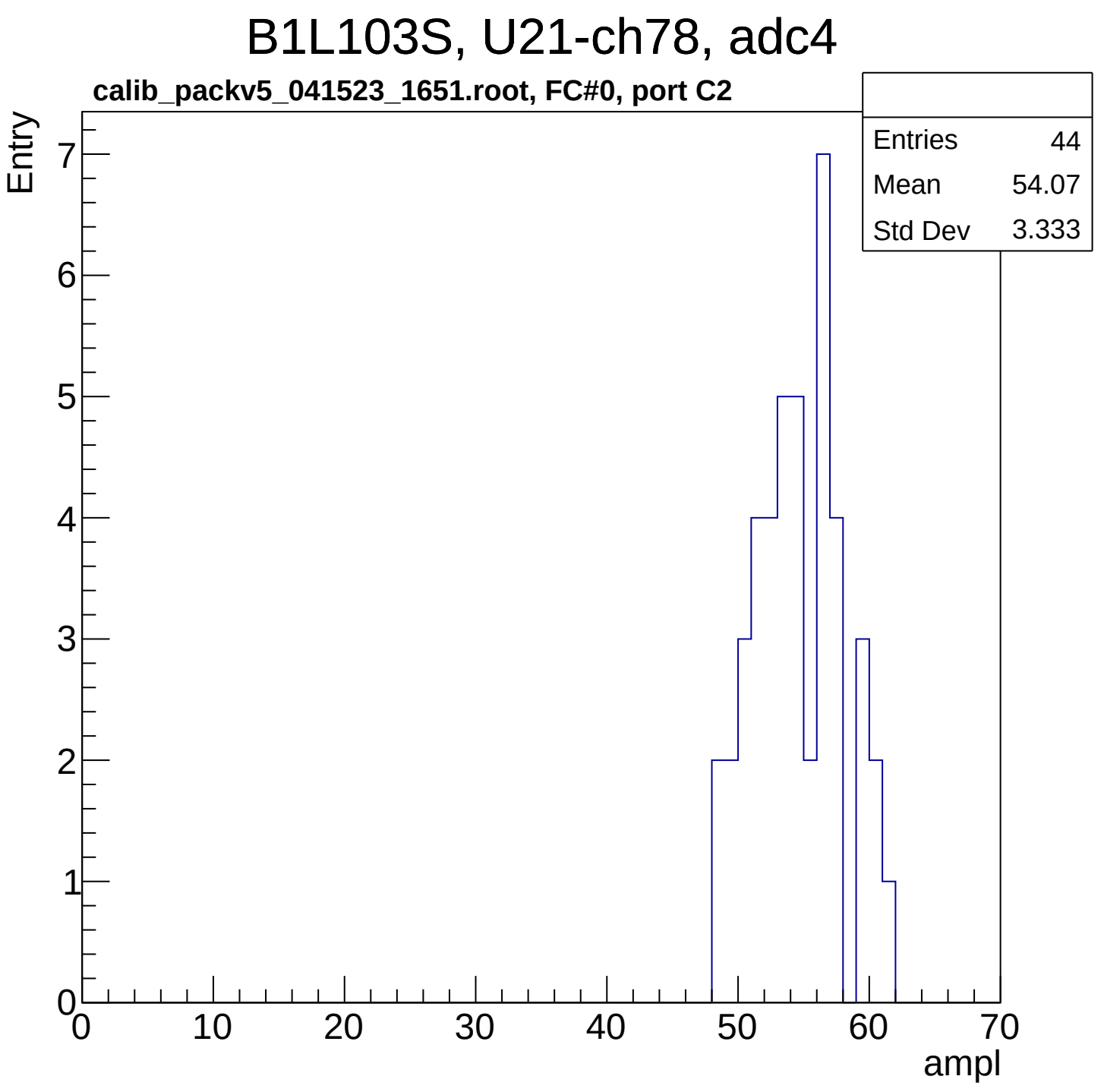
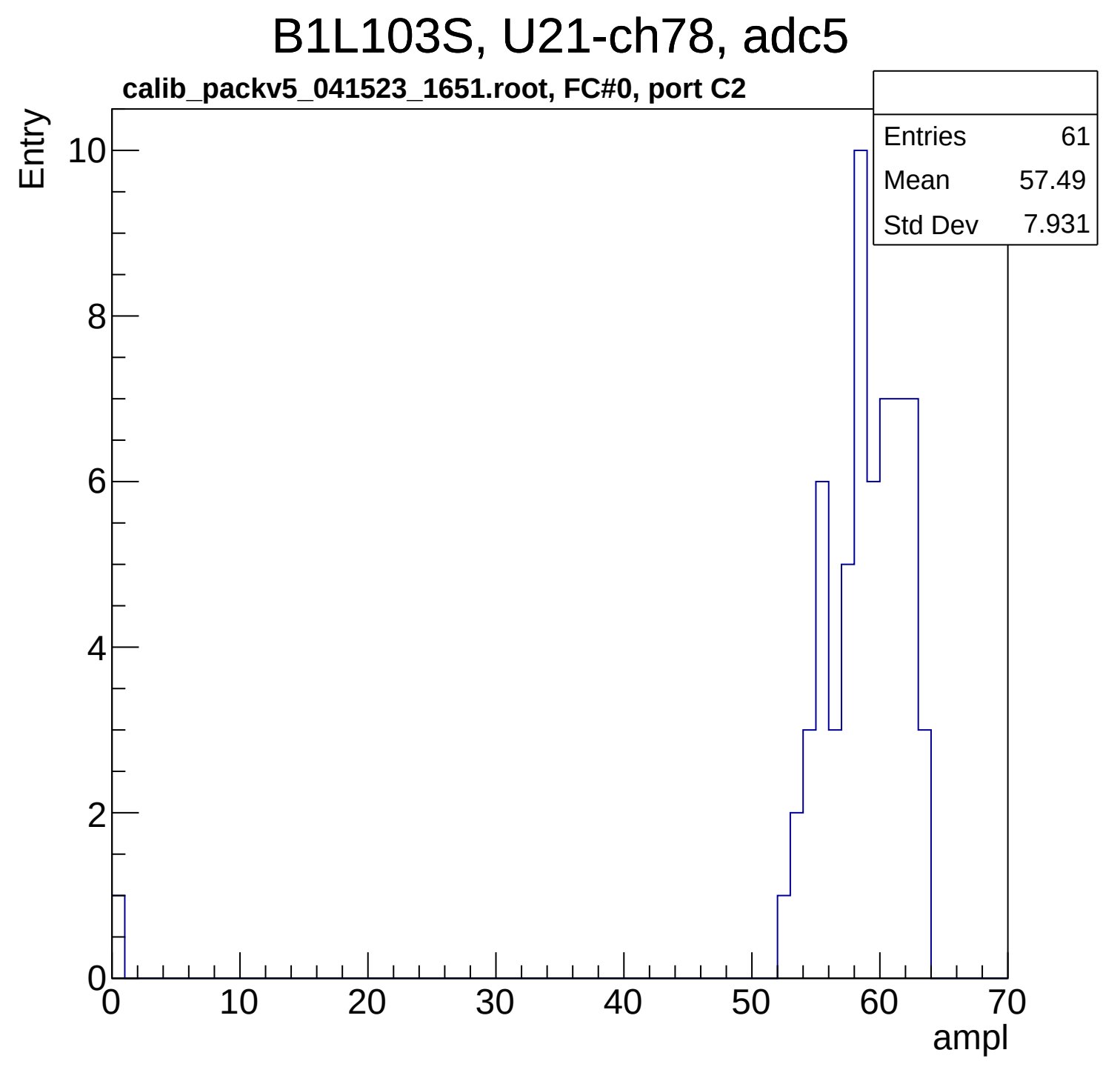
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch78, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 35.19
Std Dev 14.67
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch78, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 47.3
Std Dev 6.671
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U21-ch78, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 54.07
Std Dev 3.333
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U21-ch78, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 57.49
Std Dev 7.931
Entry
ampl
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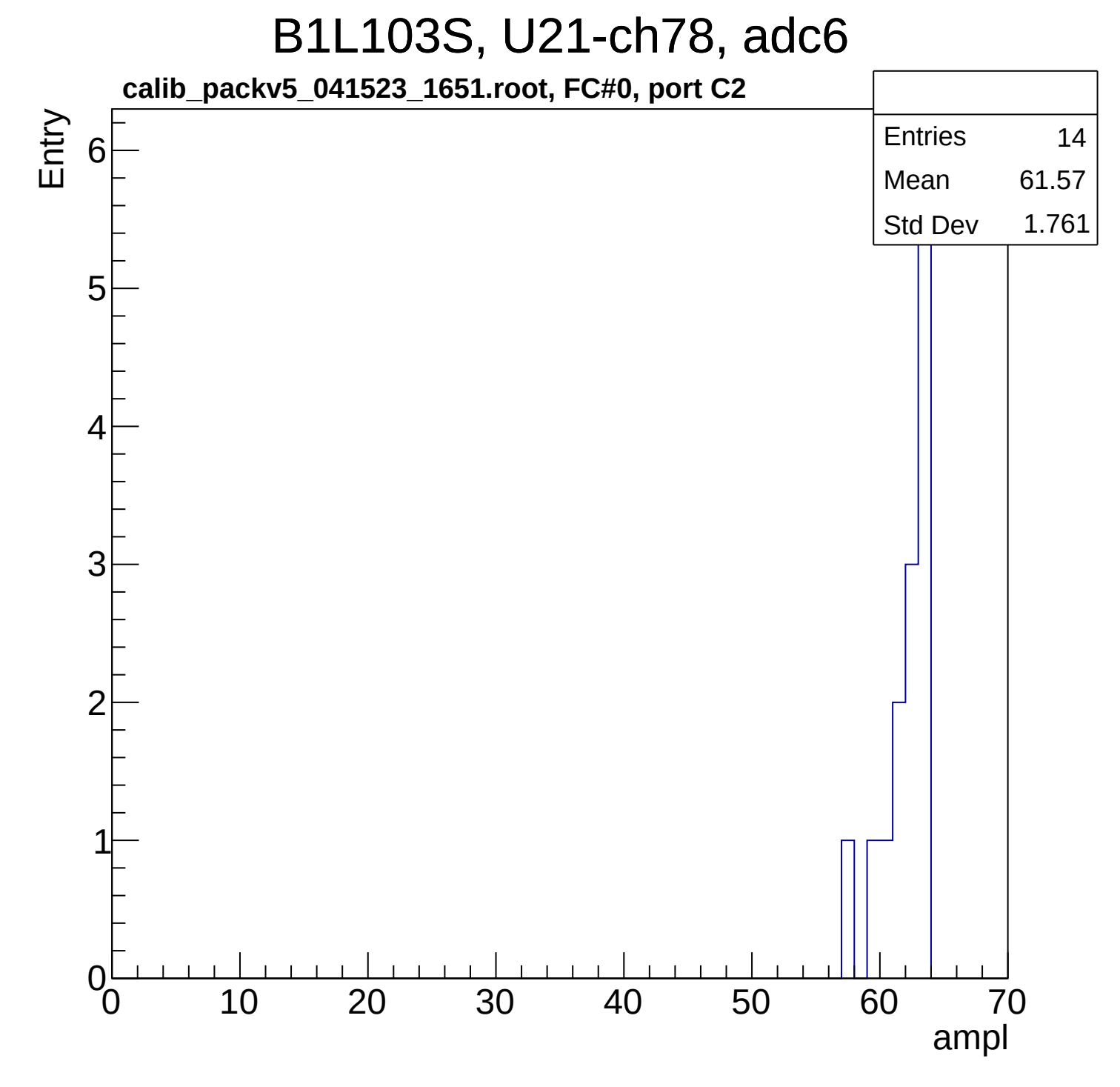
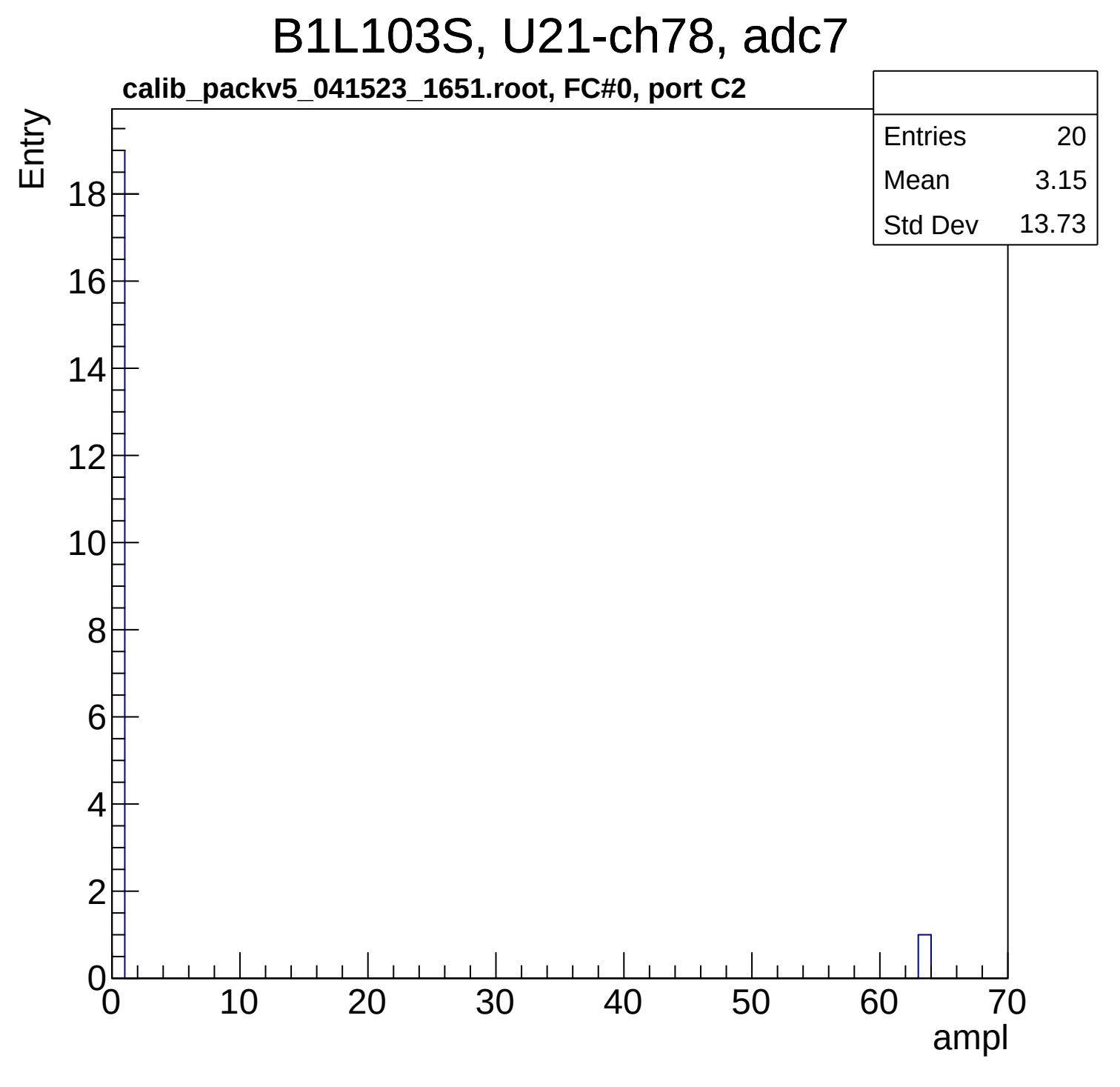
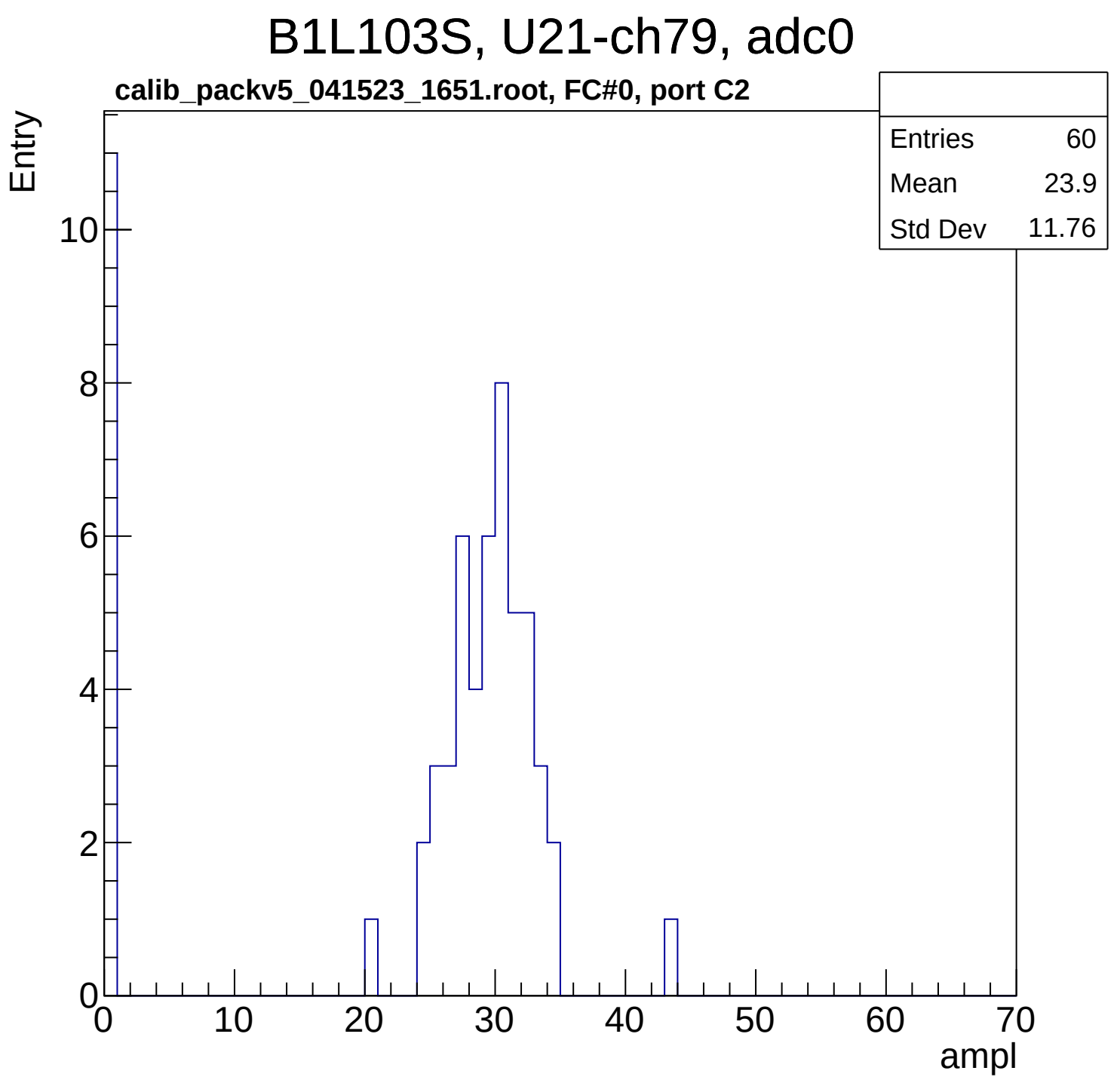
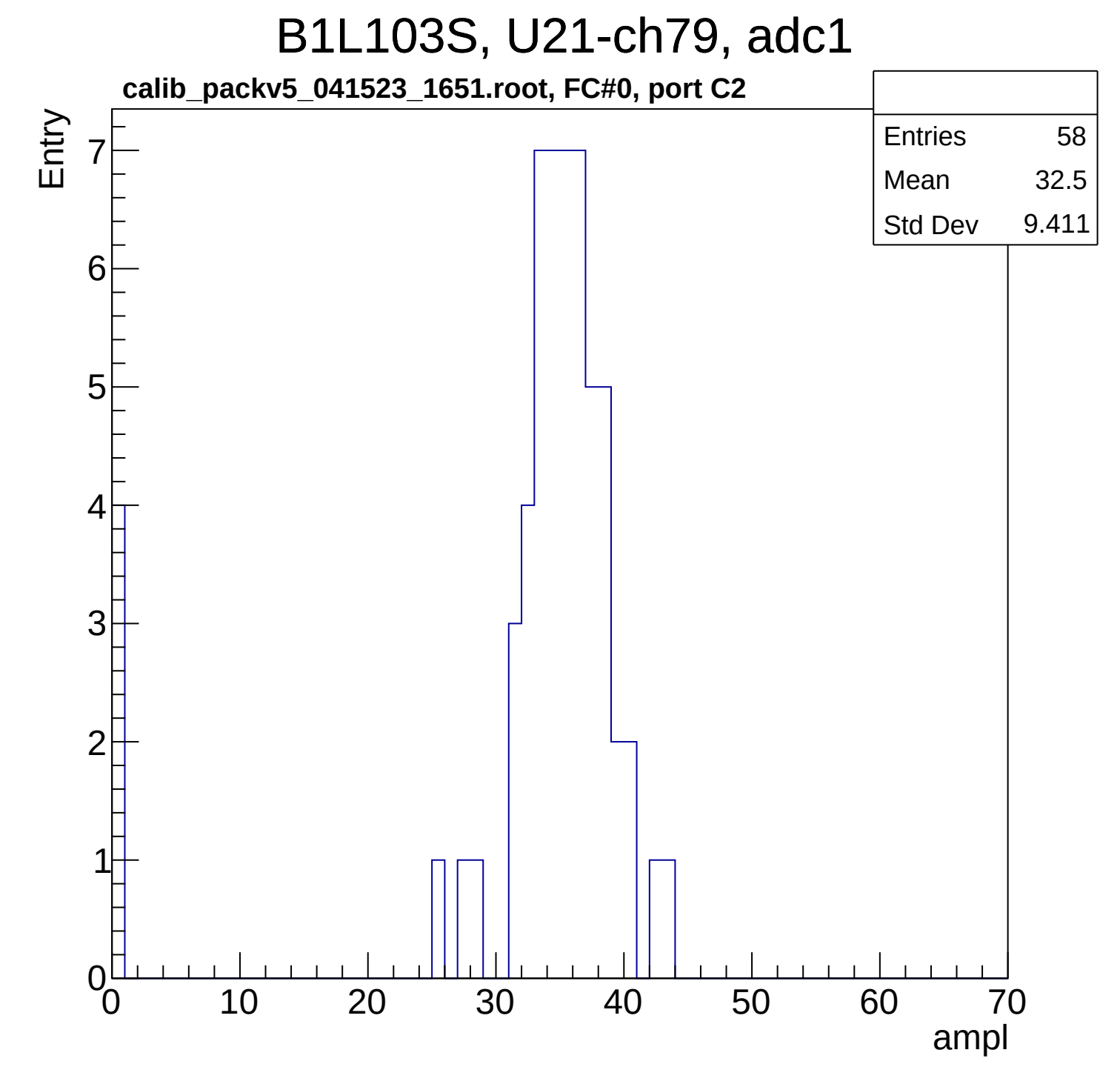
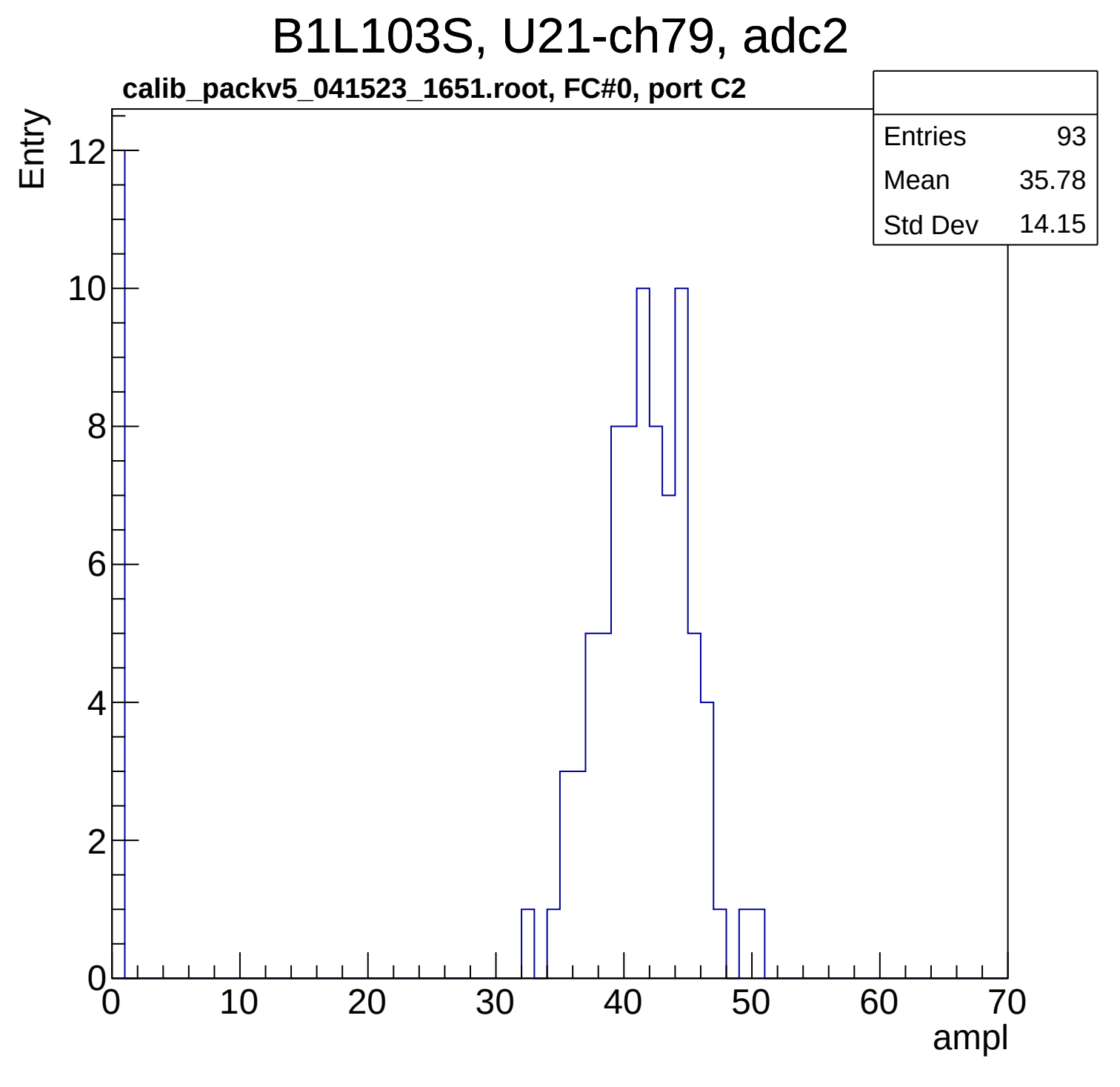
2
4
6
8
10
0
10
20
30
40
50
60
70

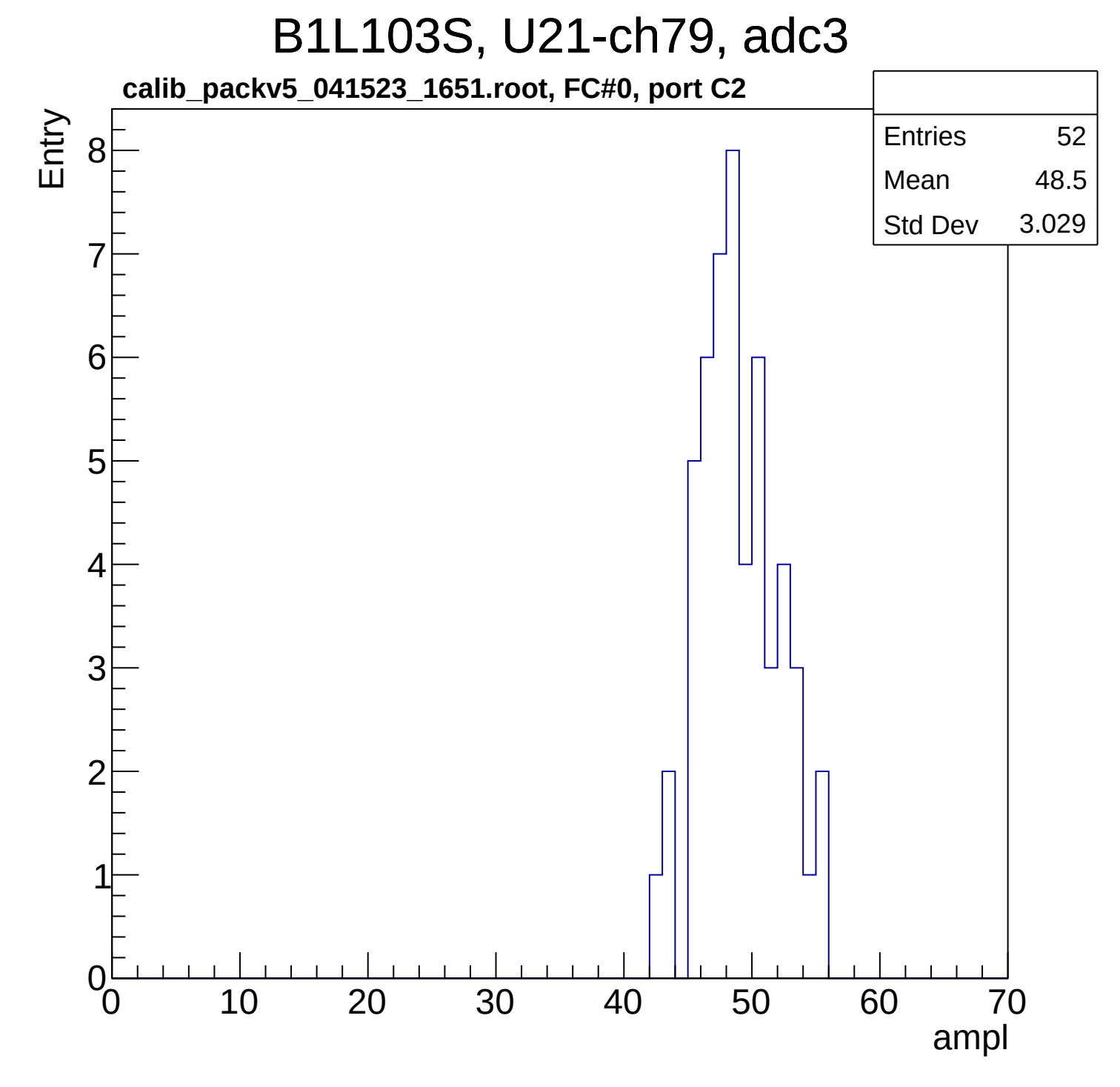

B1L103S, U21-ch78, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 61.57
Std Dev 1.761
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

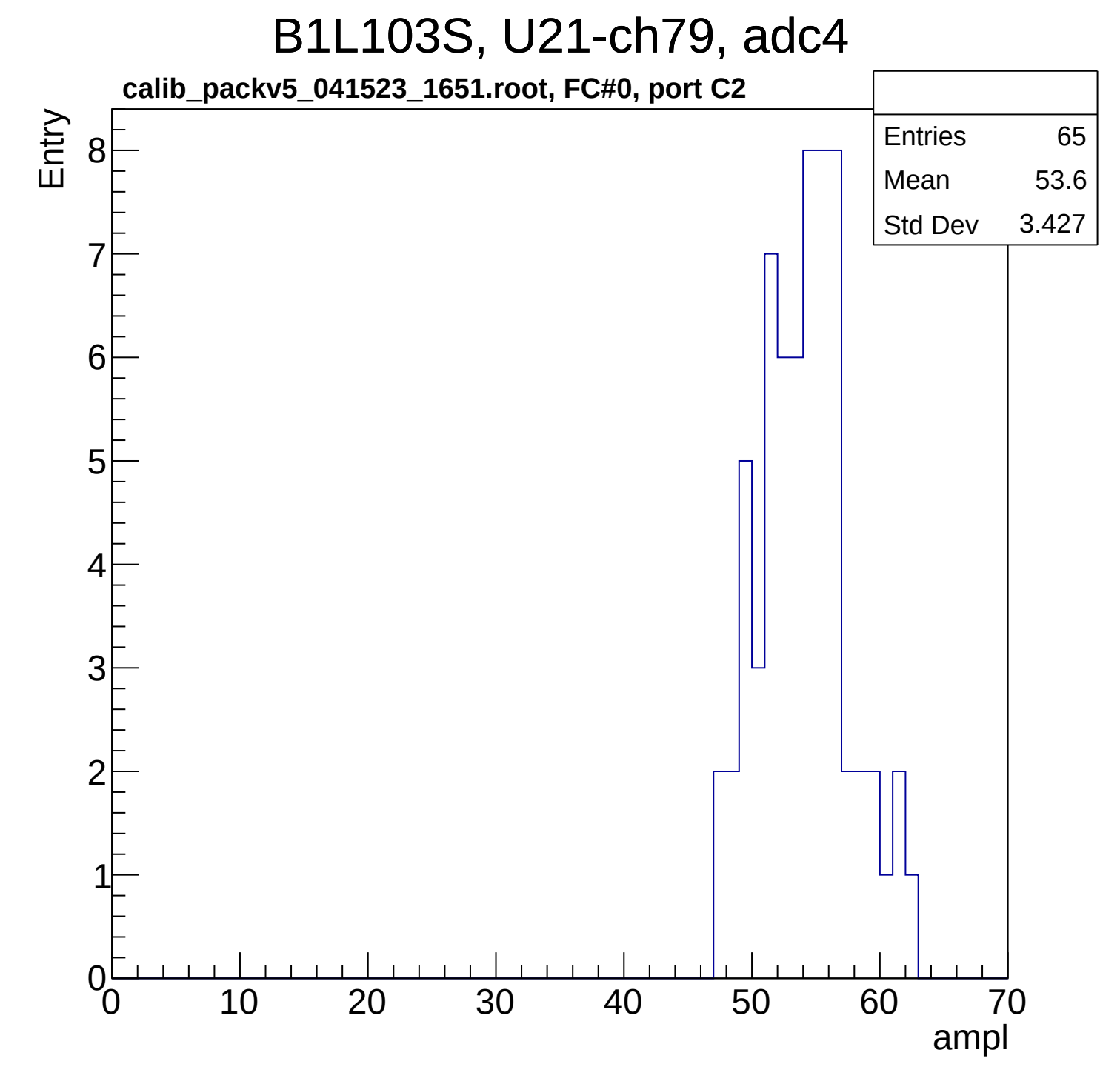

B1L103S, U21-ch78, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch79, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 23.9
Std Dev 11.76
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch79, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 32.5
Std Dev 9.411
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U21-ch79, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 35.78
Std Dev 14.15
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch79, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 48.5
Std Dev 3.029
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch79, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 53.6
Std Dev 3.427
Entry
ampl
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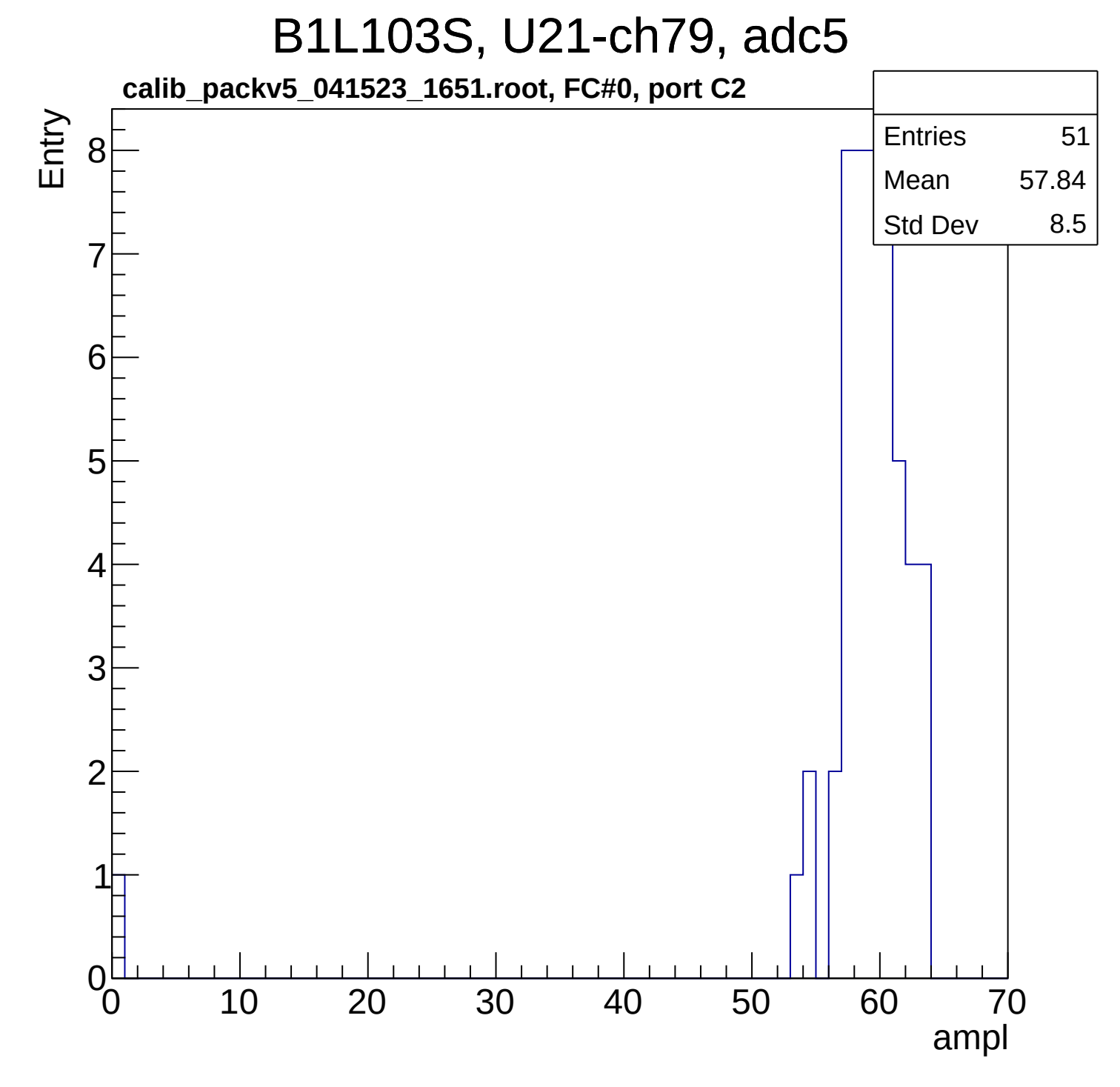
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch79, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 57.84
Std Dev 8.5
Entry
ampl
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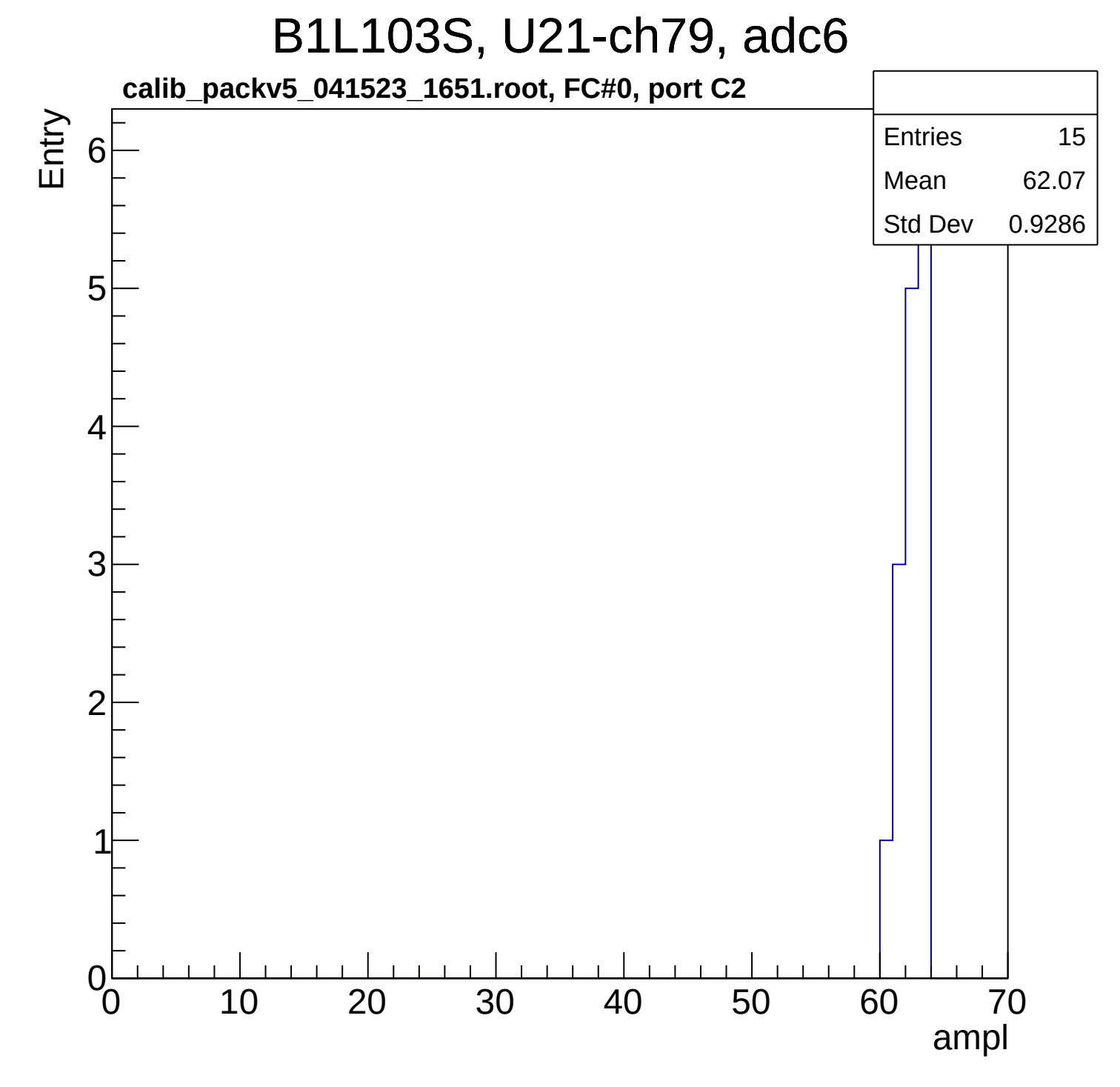
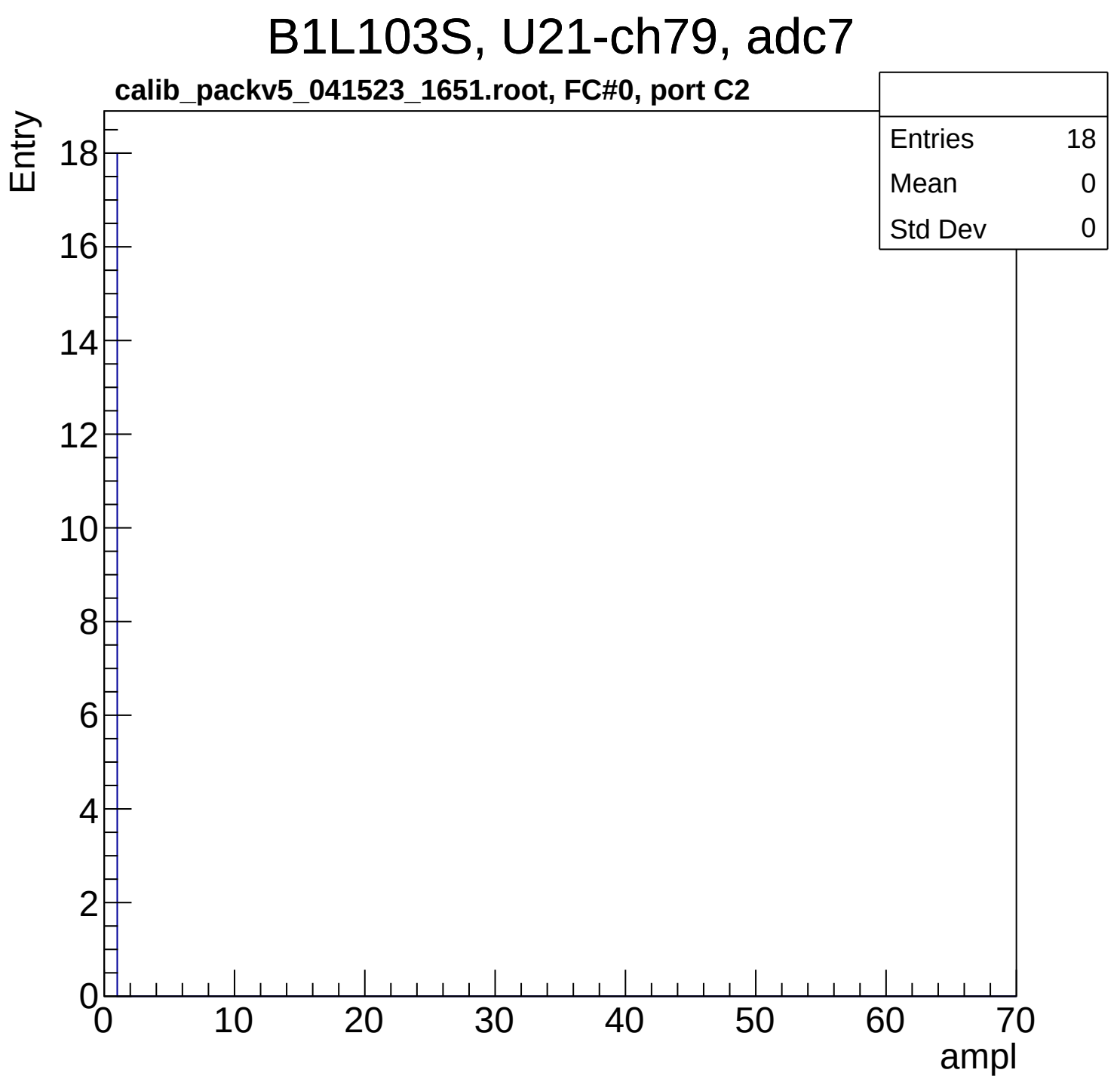
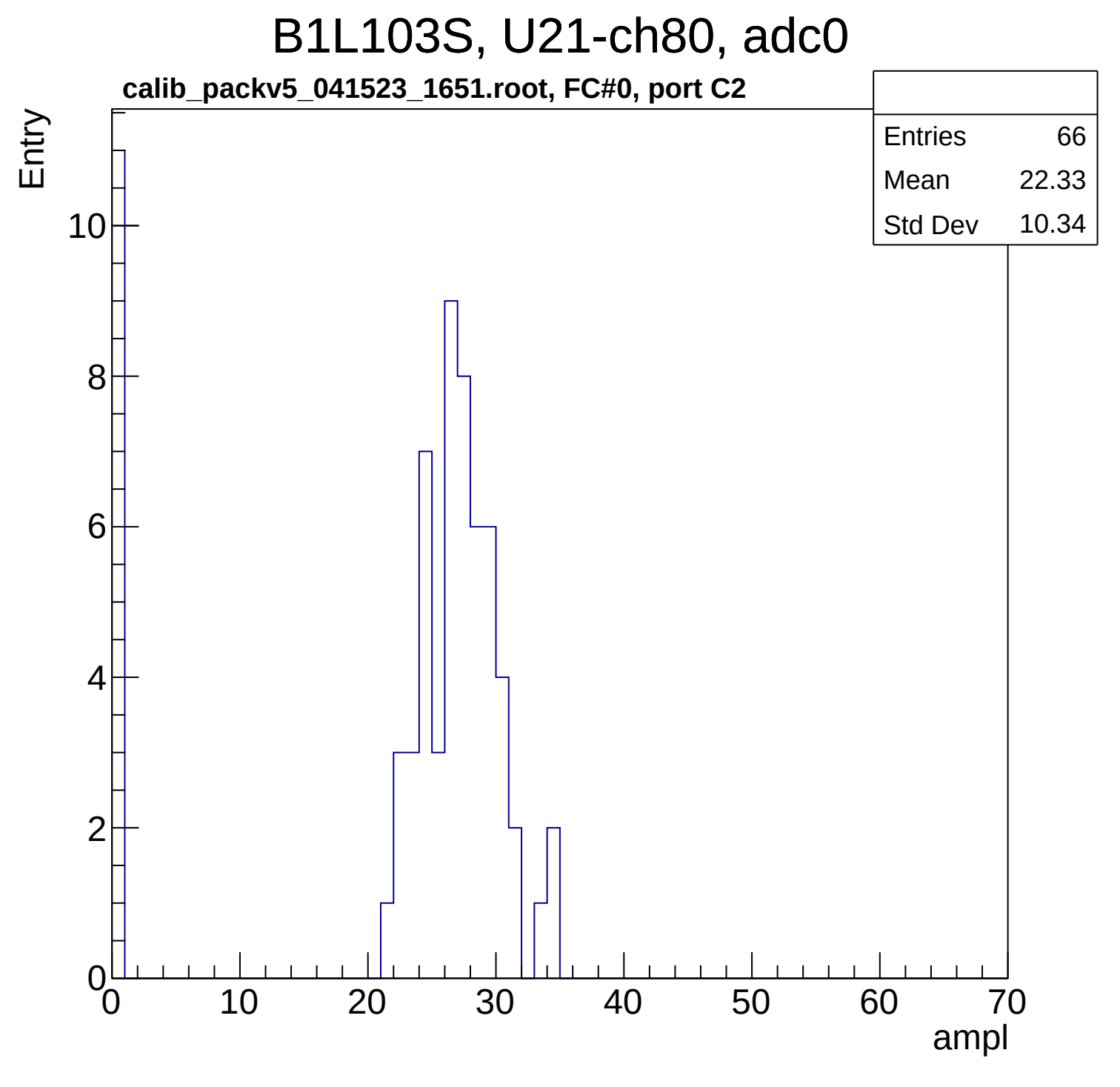
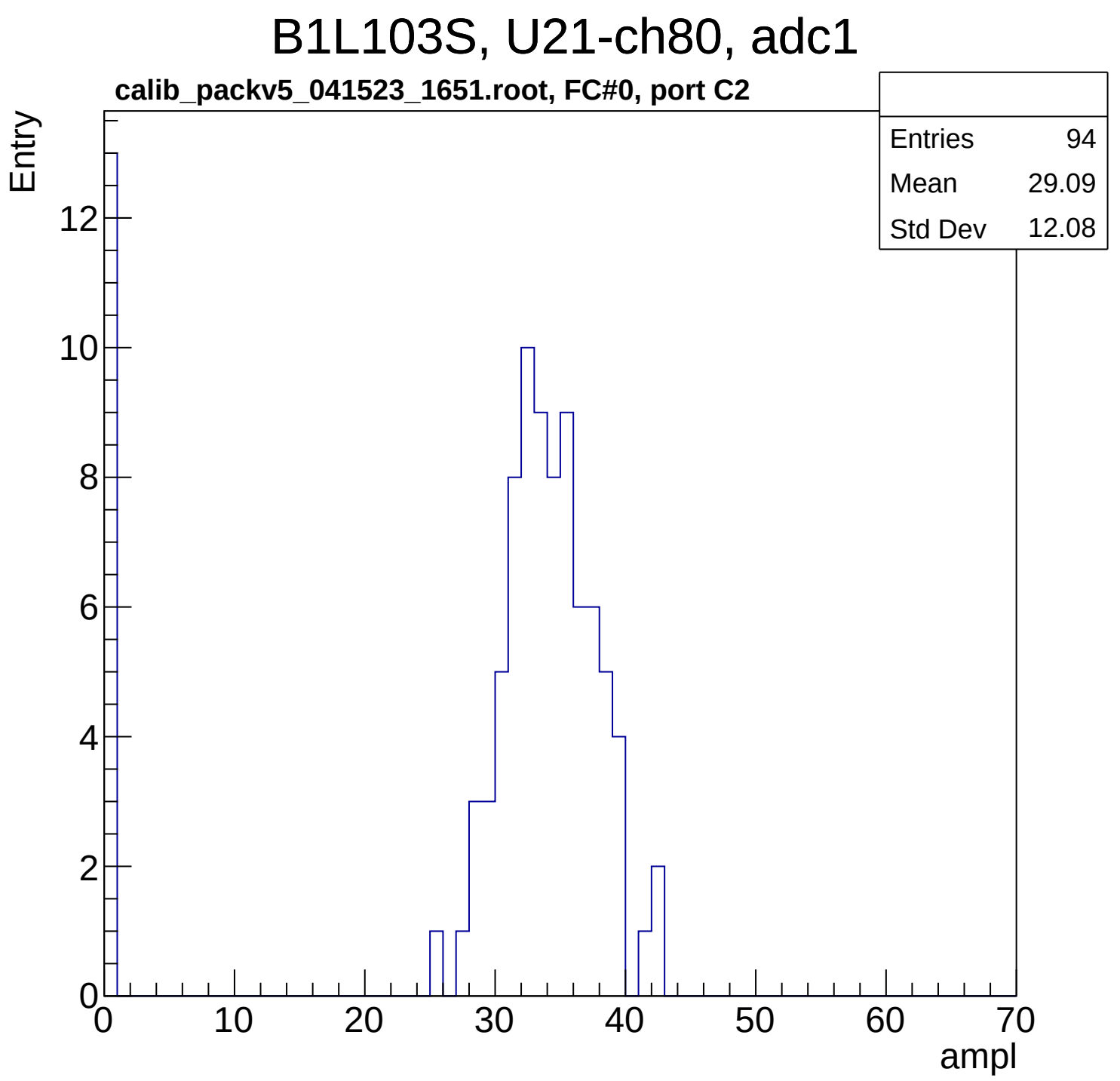
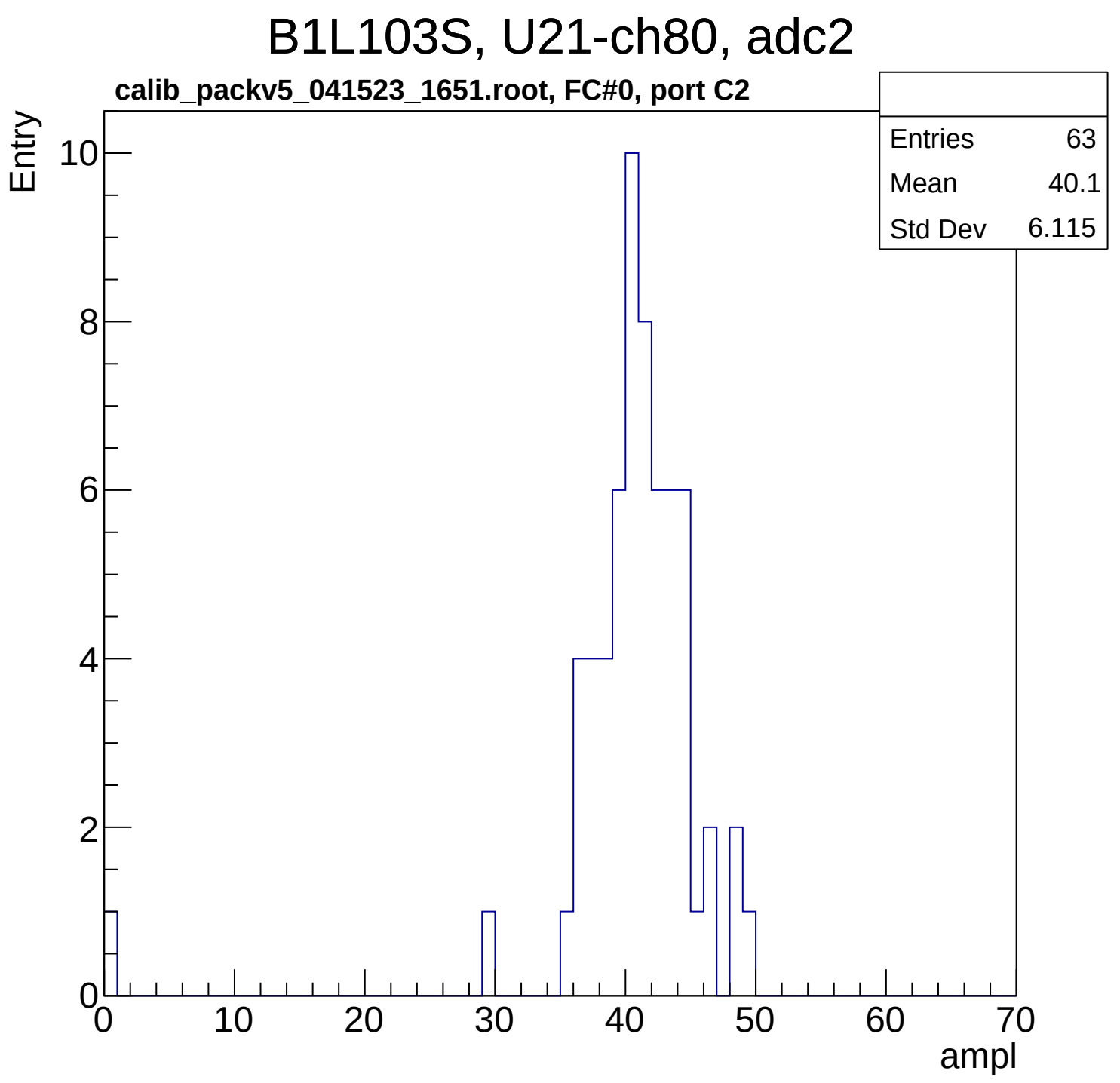
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

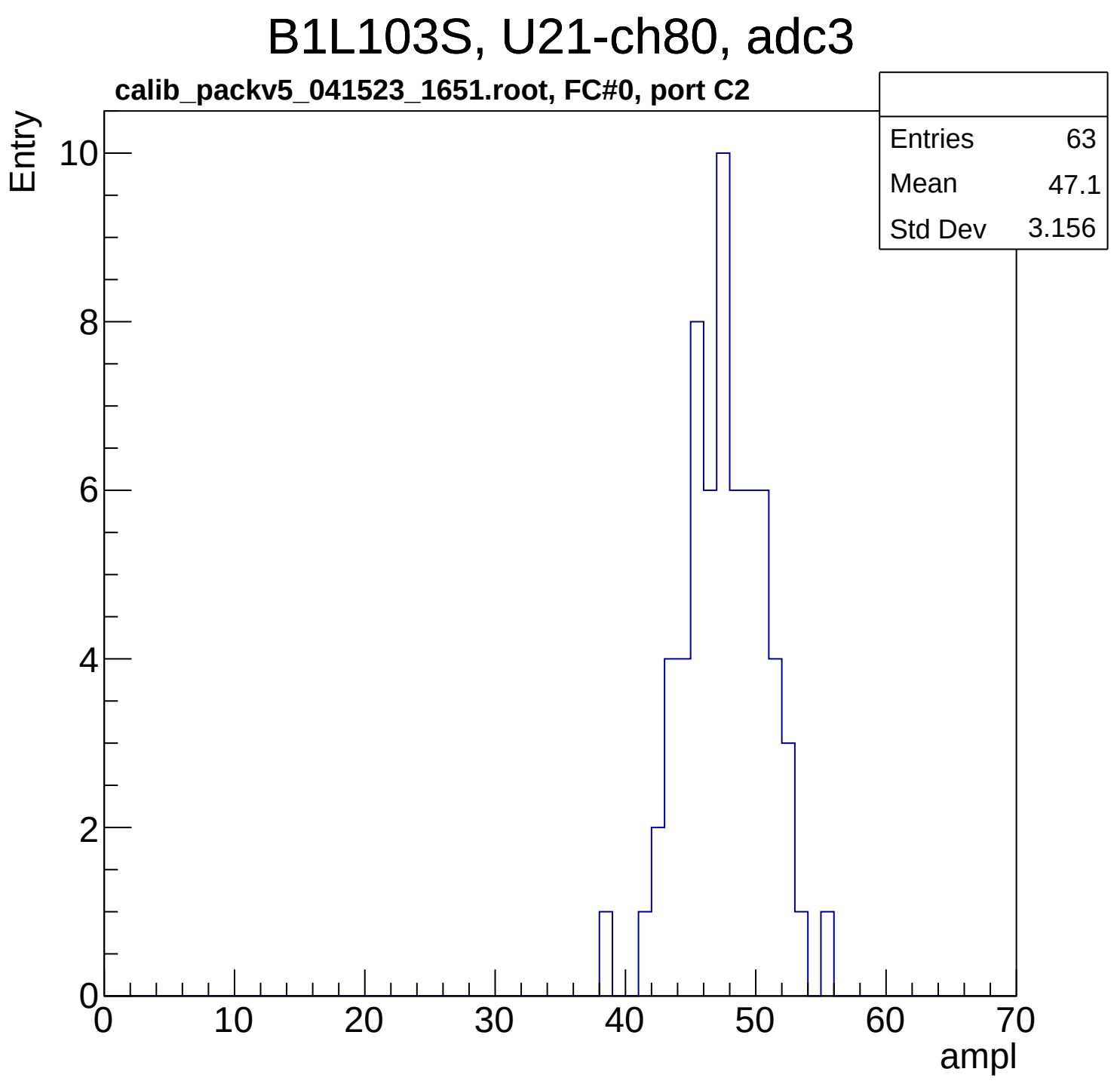

B1L103S, U21-ch79, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 62.07
Std Dev 0.9286
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

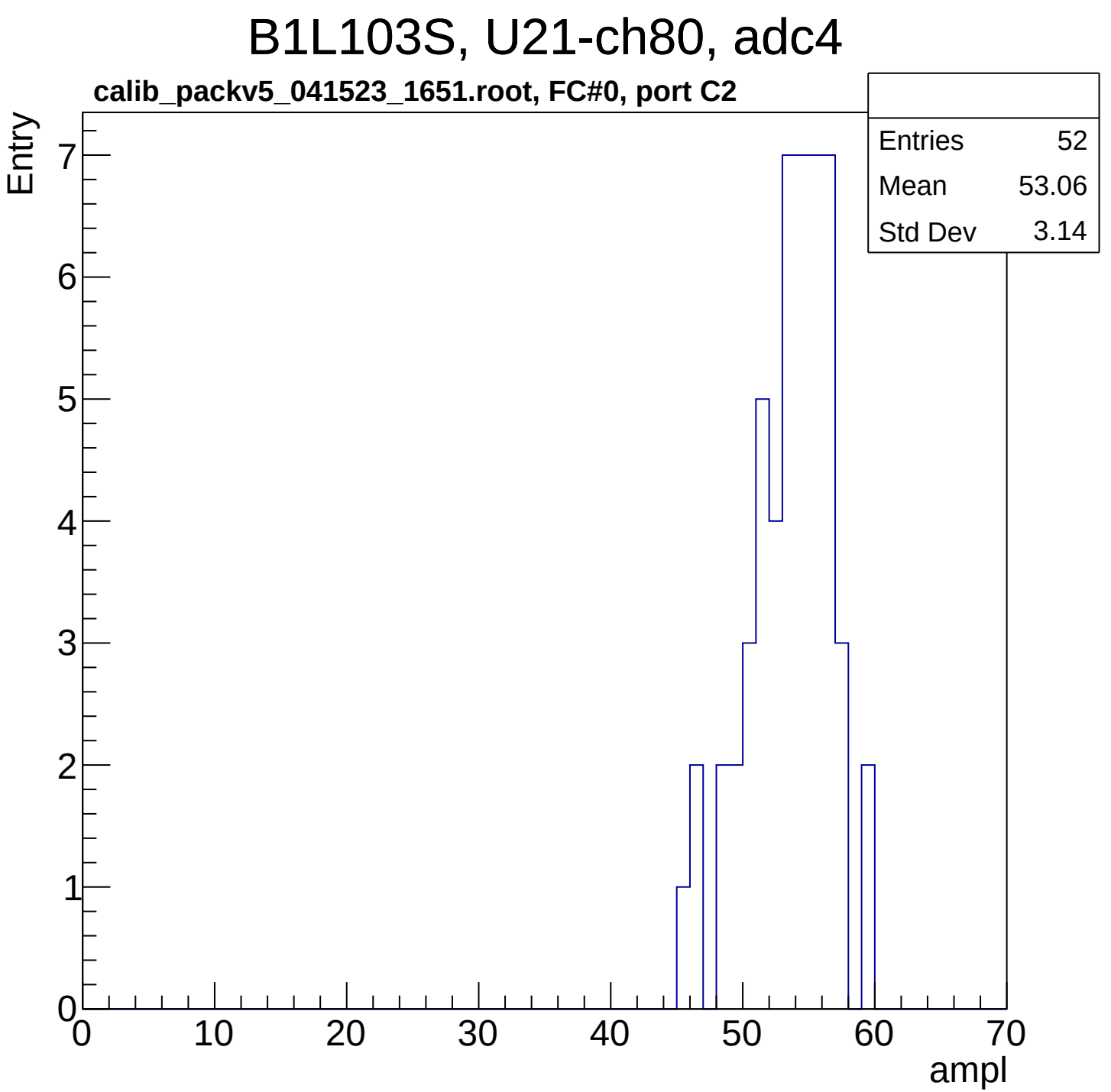

B1L103S, U21-ch79, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

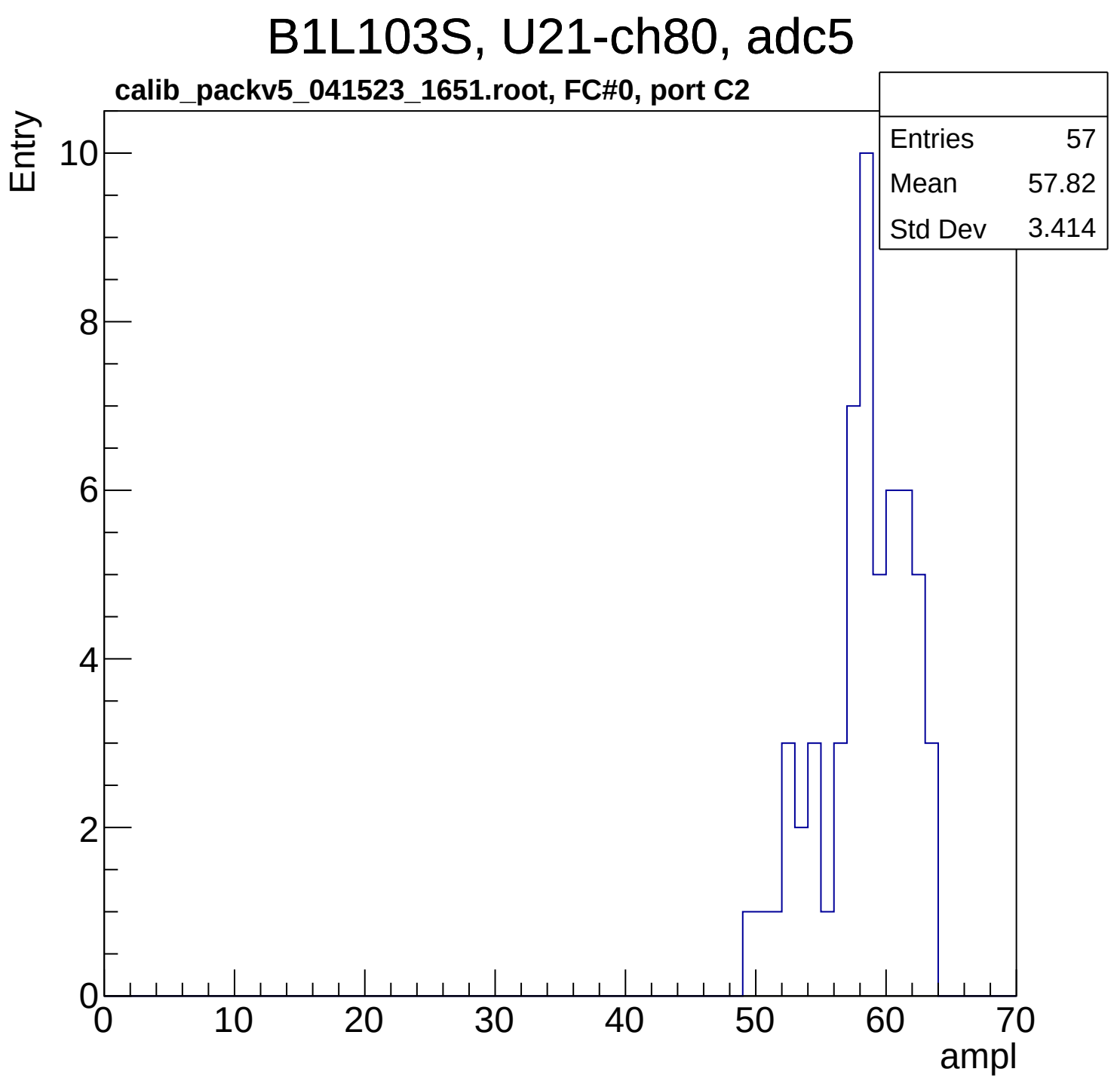

B1L103S, U21-ch80, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 22.33
Std Dev 10.34
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

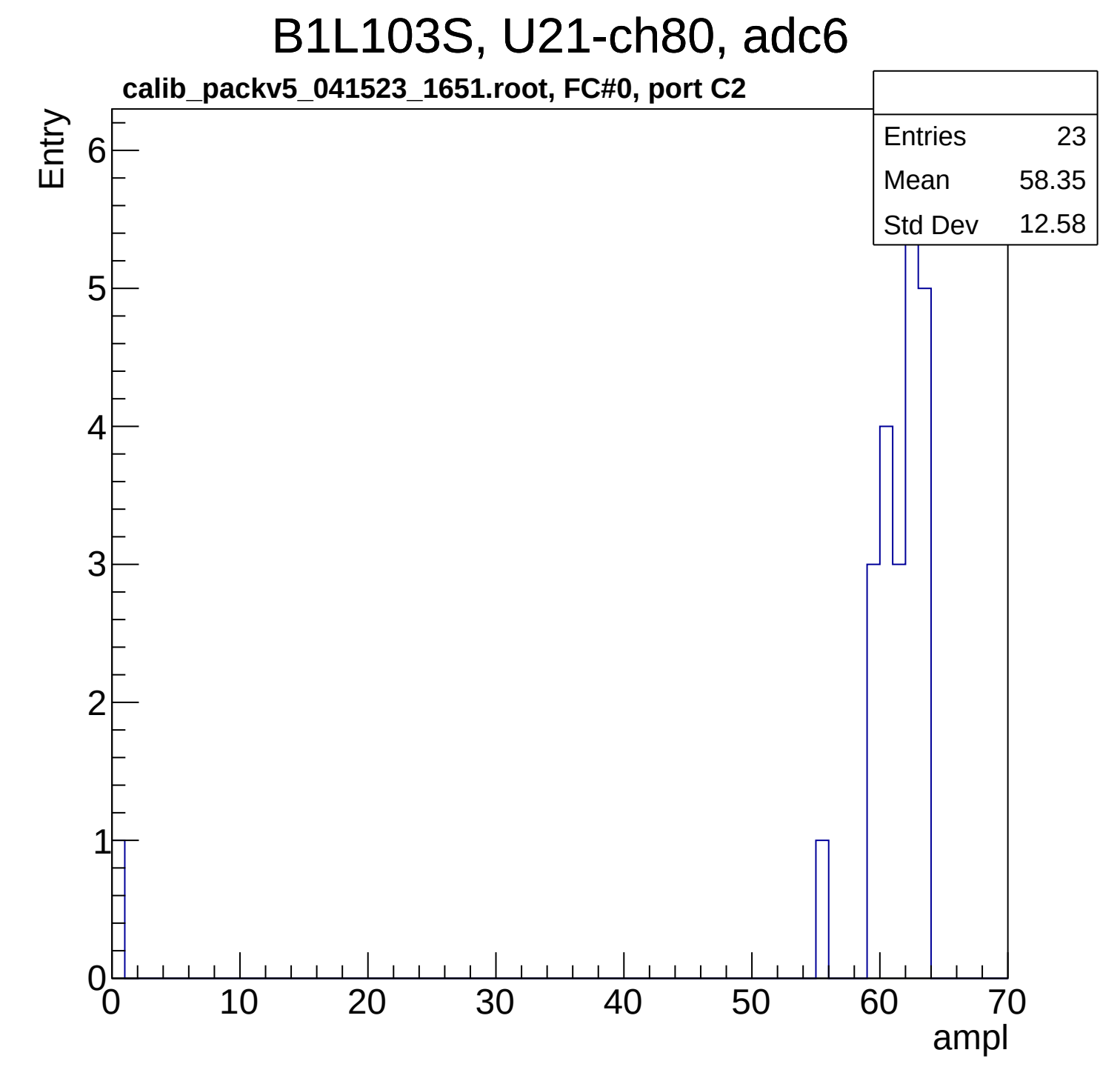

B1L103S, U21-ch80, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 29.09
Std Dev 12.08
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

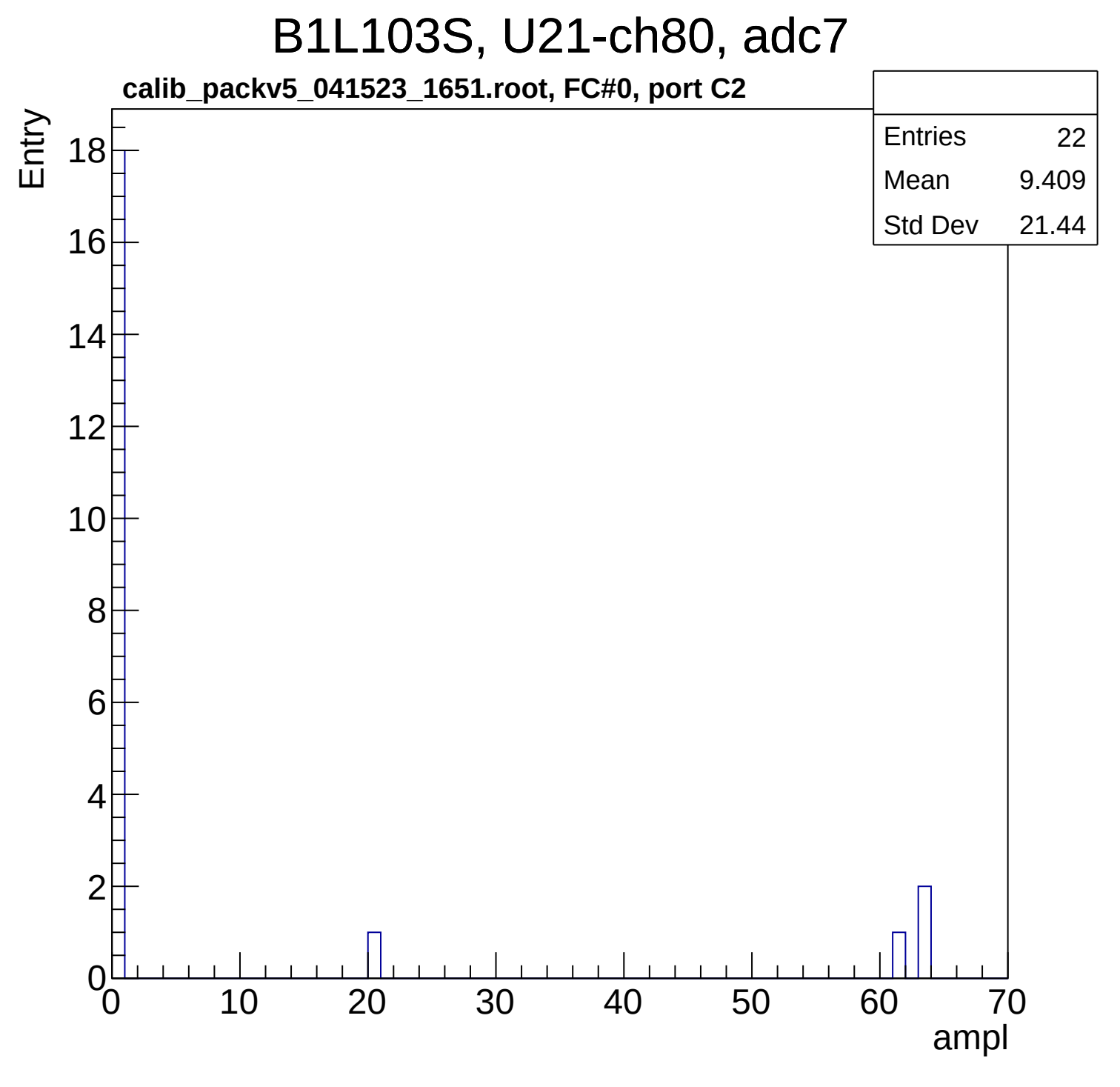

B1L103S, U21-ch80, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 40.1
Std Dev 6.115
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U21-ch80, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 47.1
Std Dev 3.156
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch80, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 53.06
Std Dev 3.14
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U21-ch80, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 57.82
Std Dev 3.414
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch80, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 58.35
Std Dev 12.58
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U21-ch80, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 9.409
Std Dev 21.44
Entry
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4
6
8
10
12
14
16
18
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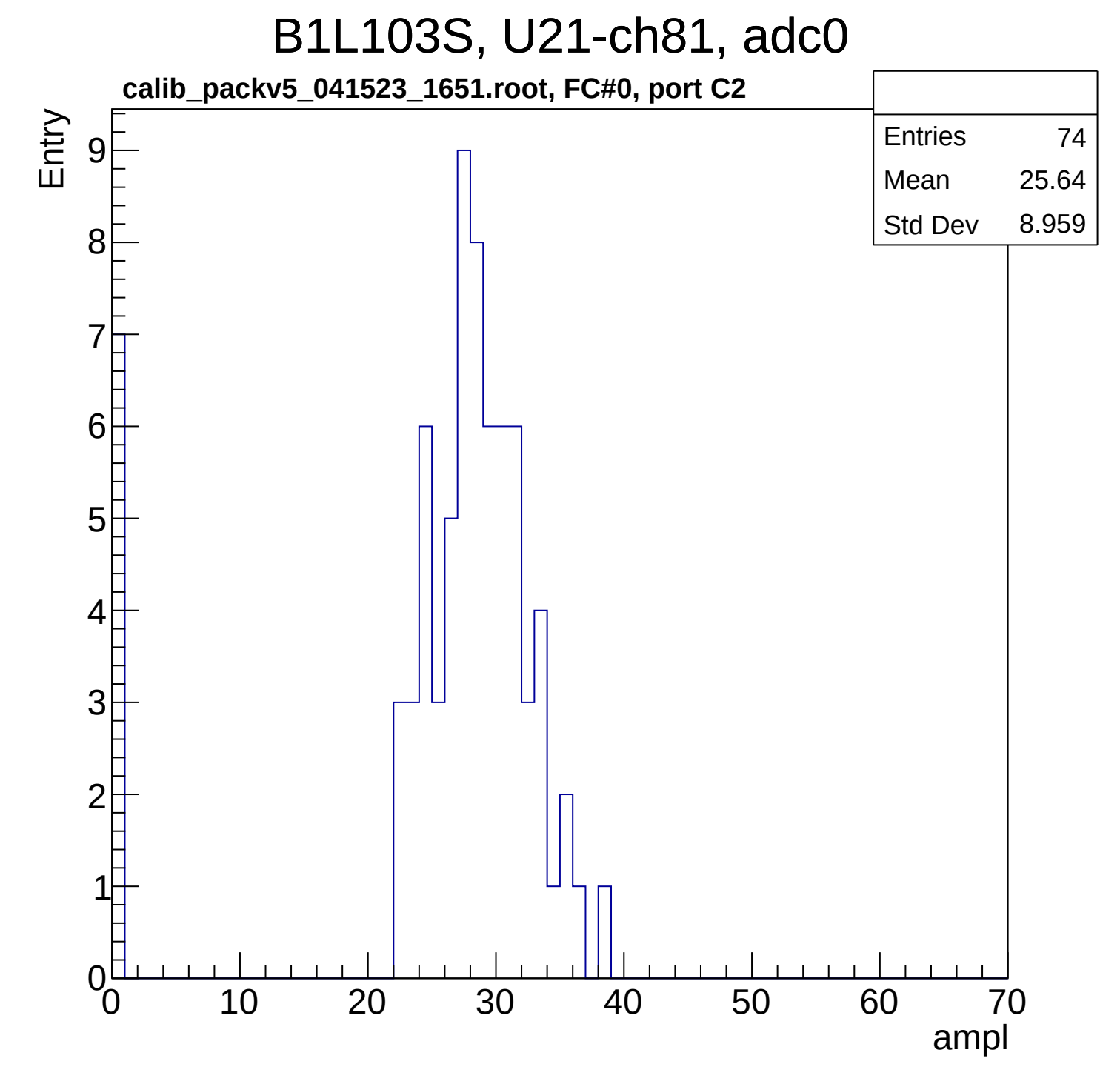
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch81, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 25.64
Std Dev 8.959
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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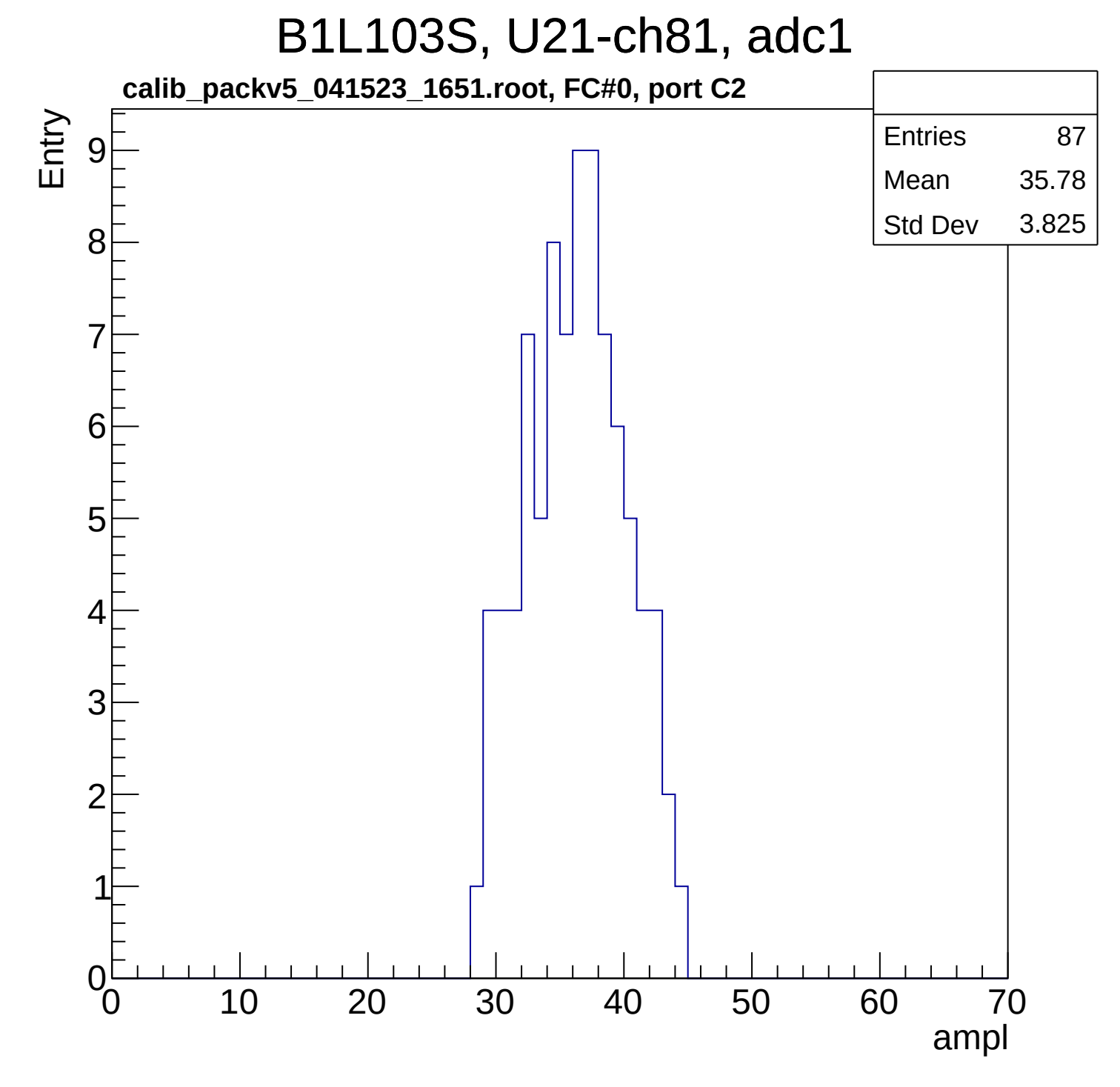
40
50
60
70


B1L103S, U21-ch81, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 35.78
Std Dev 3.825
Entry
ampl
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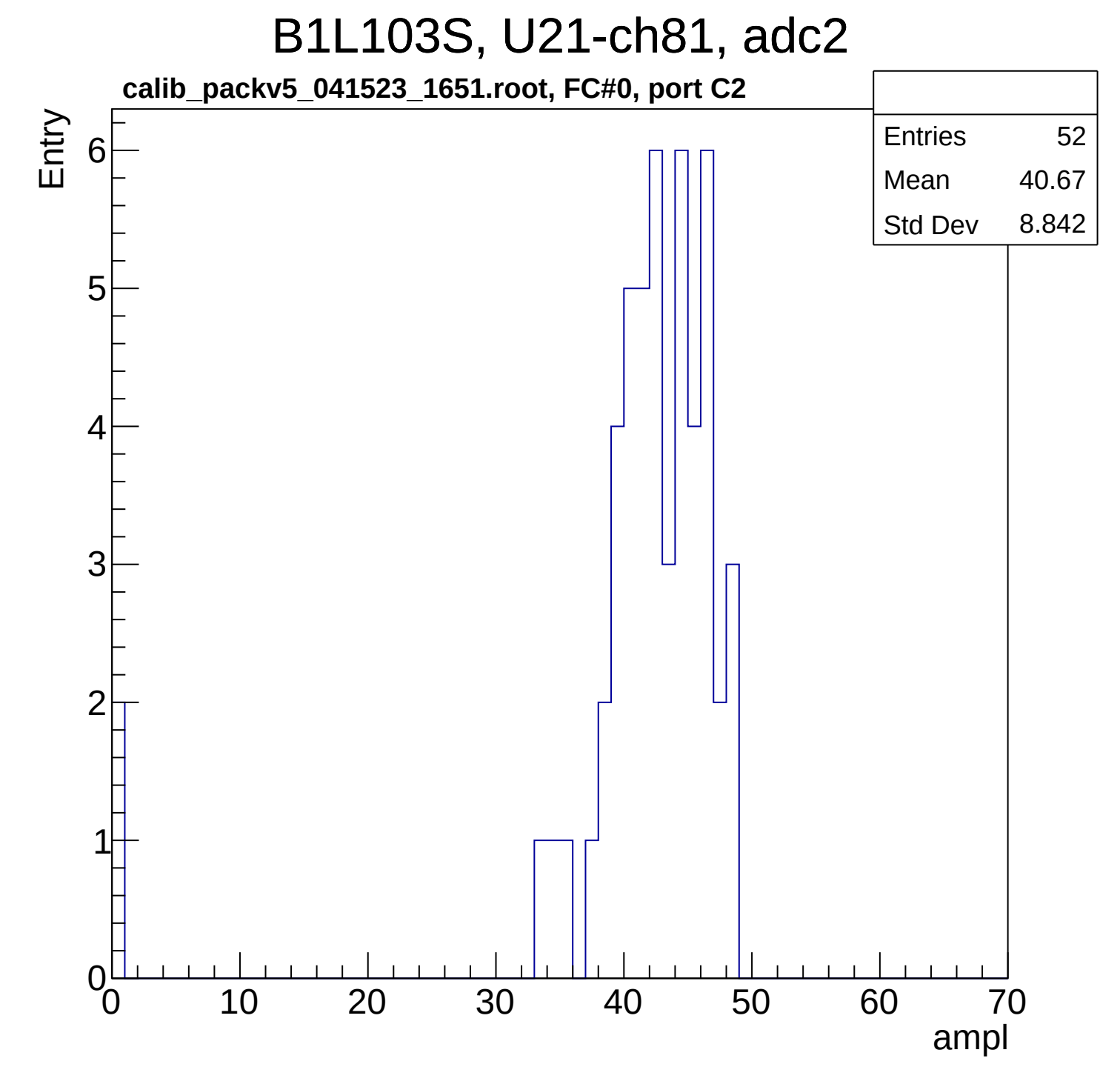
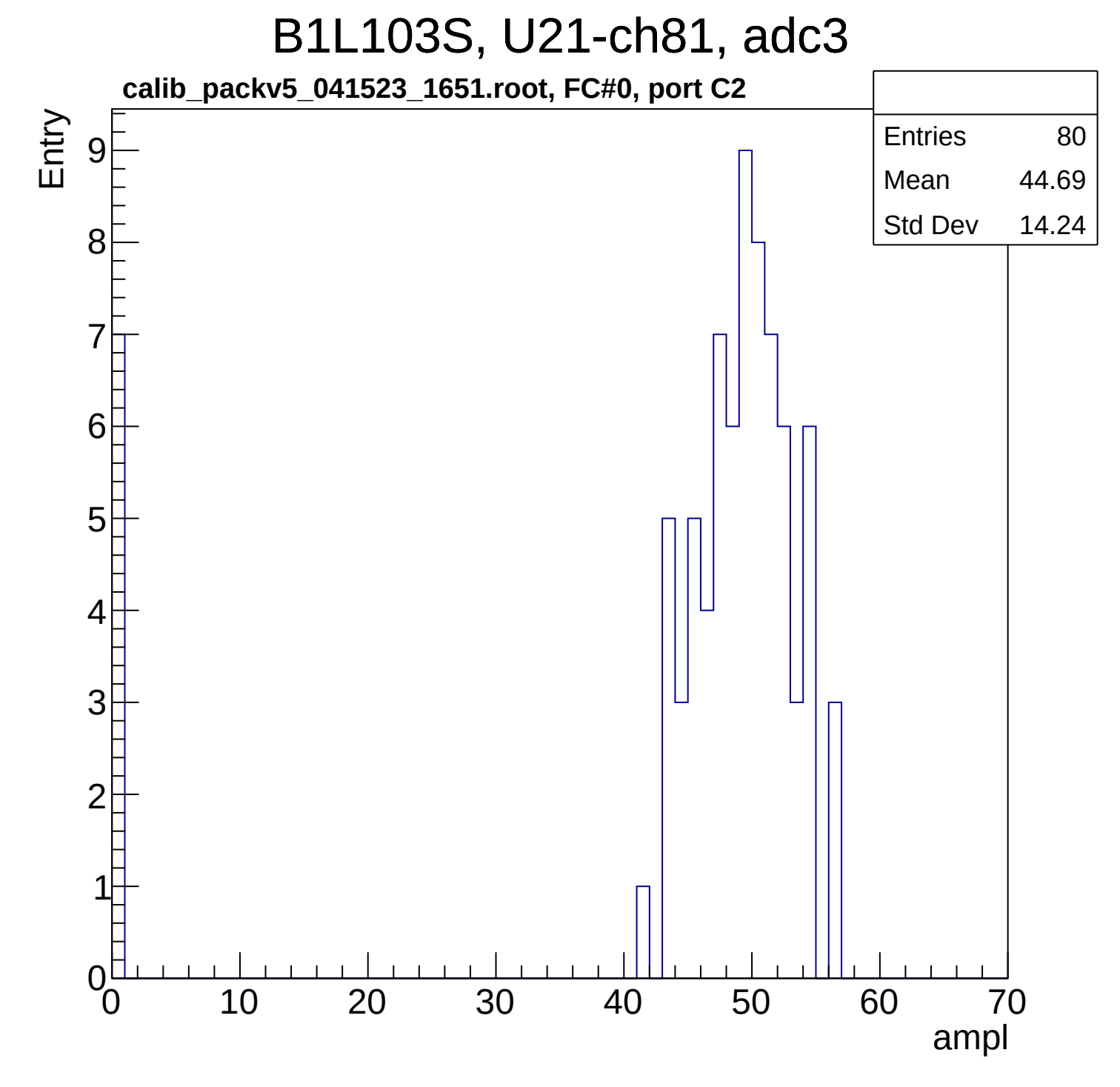
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch81, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 40.67
Std Dev 8.842
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U21-ch81, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 44.69
Std Dev 14.24
Entry
ampl
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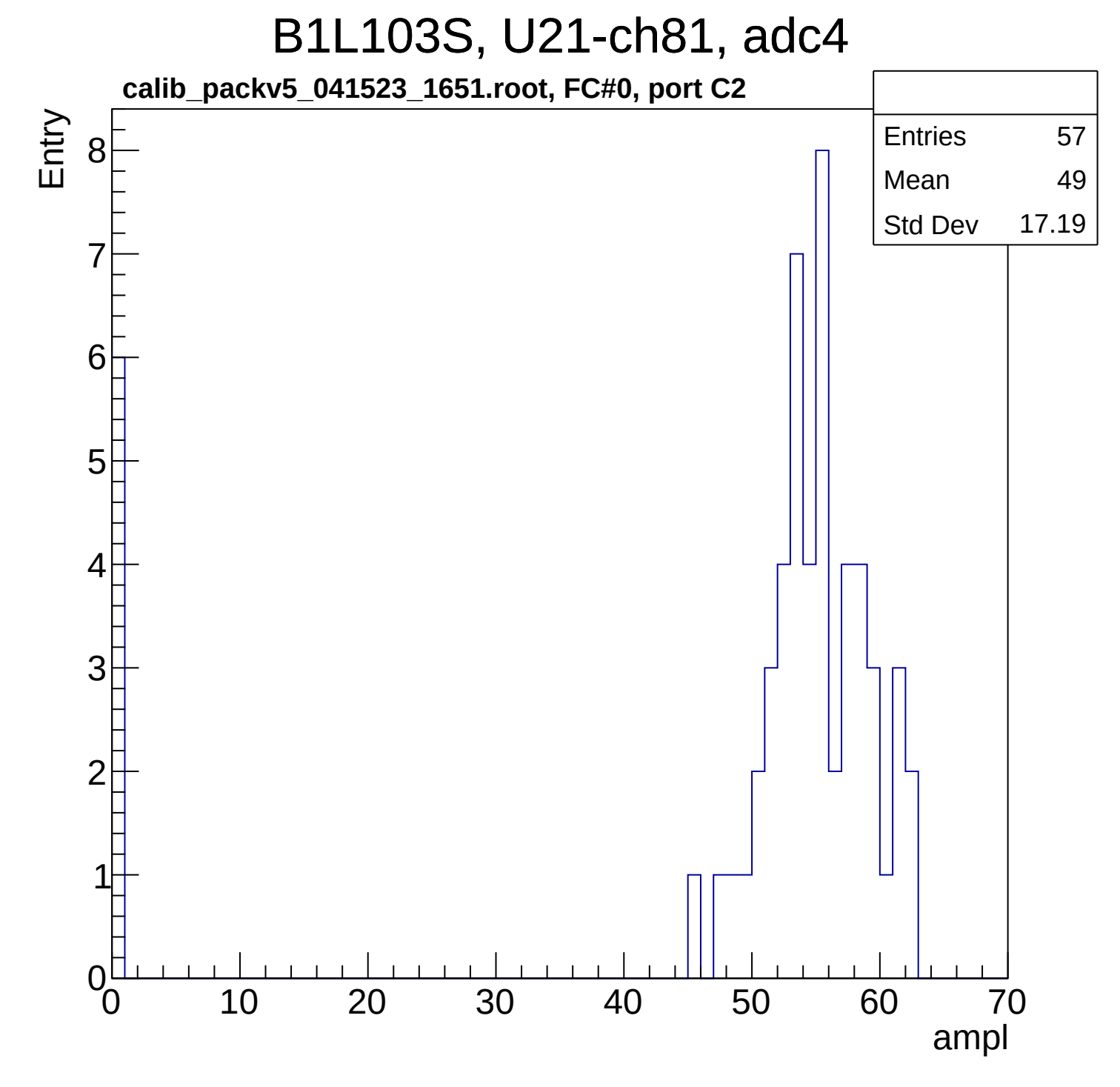
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch81, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 49
Std Dev 17.19
Entry
ampl
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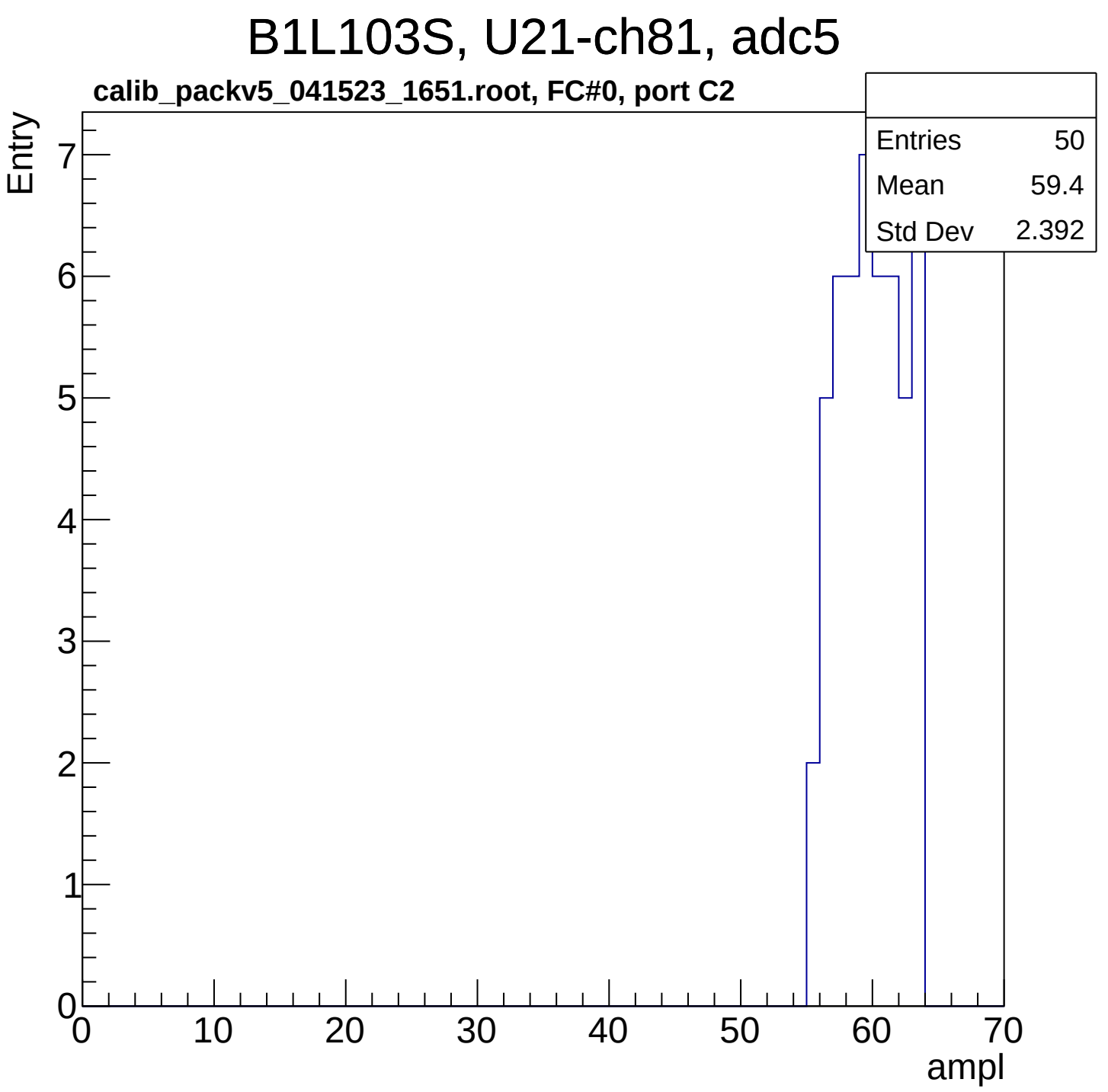
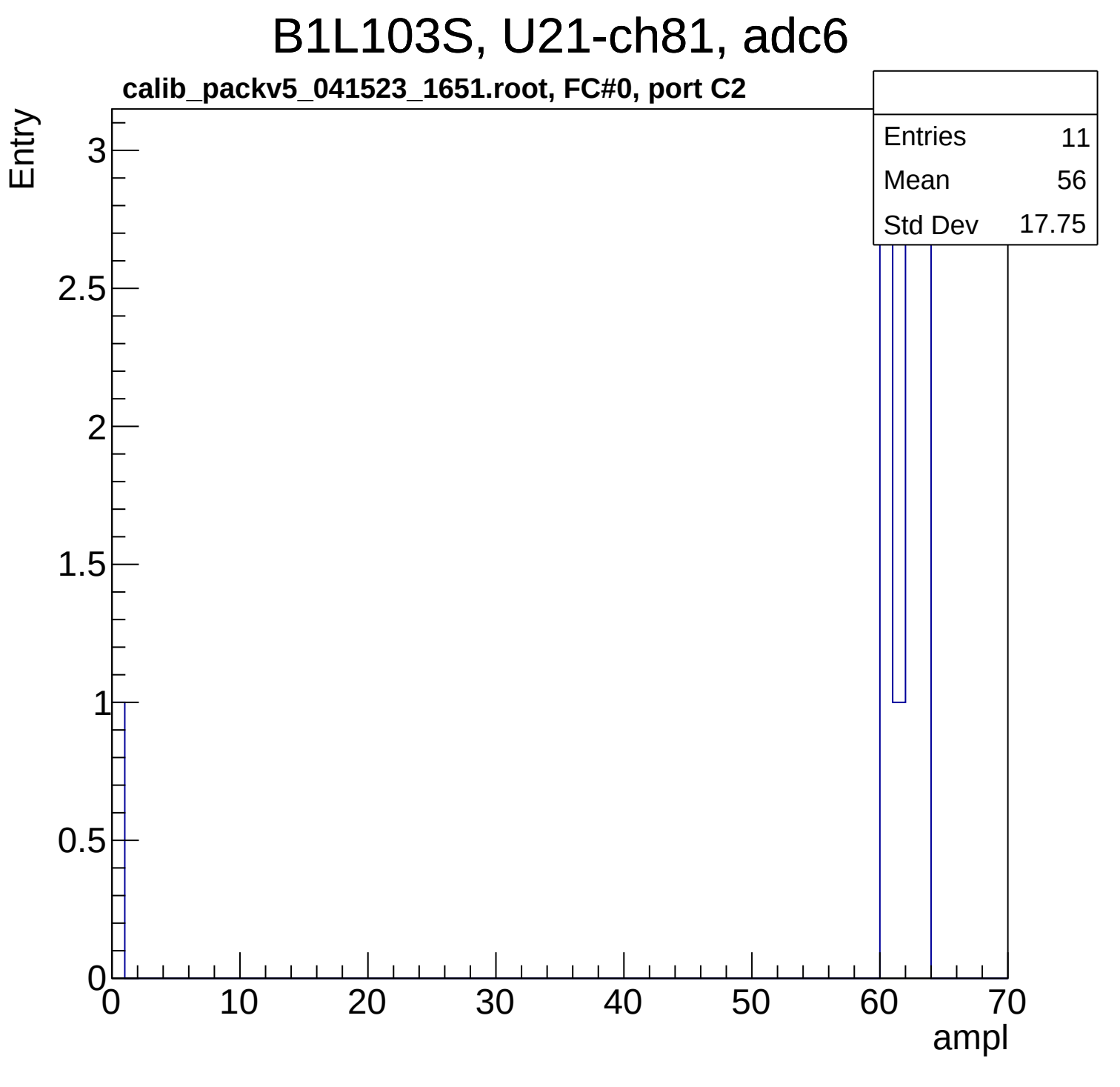
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch81, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 59.4
Std Dev 2.392
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U21-ch81, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 56
Std Dev 17.75
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
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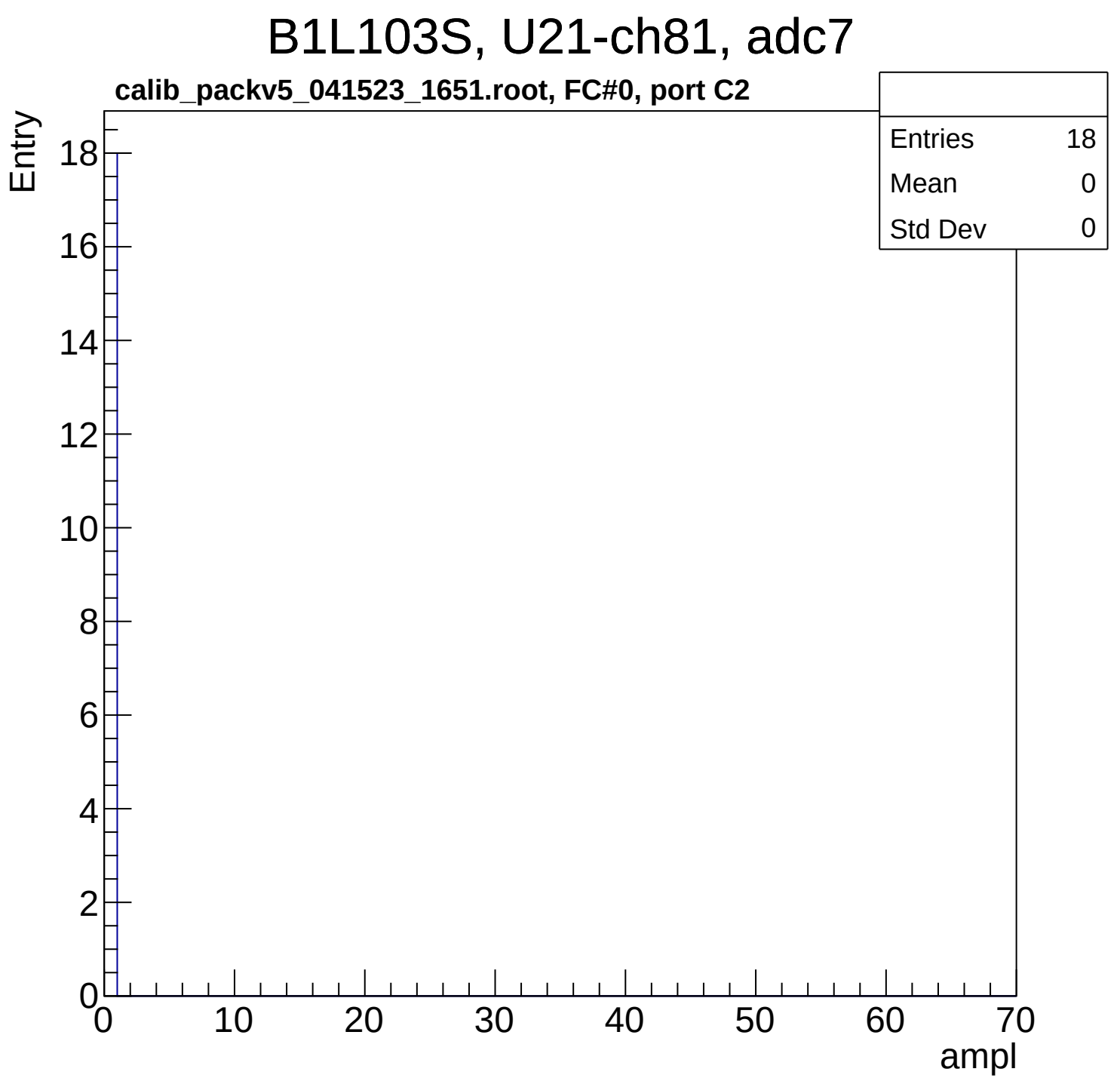
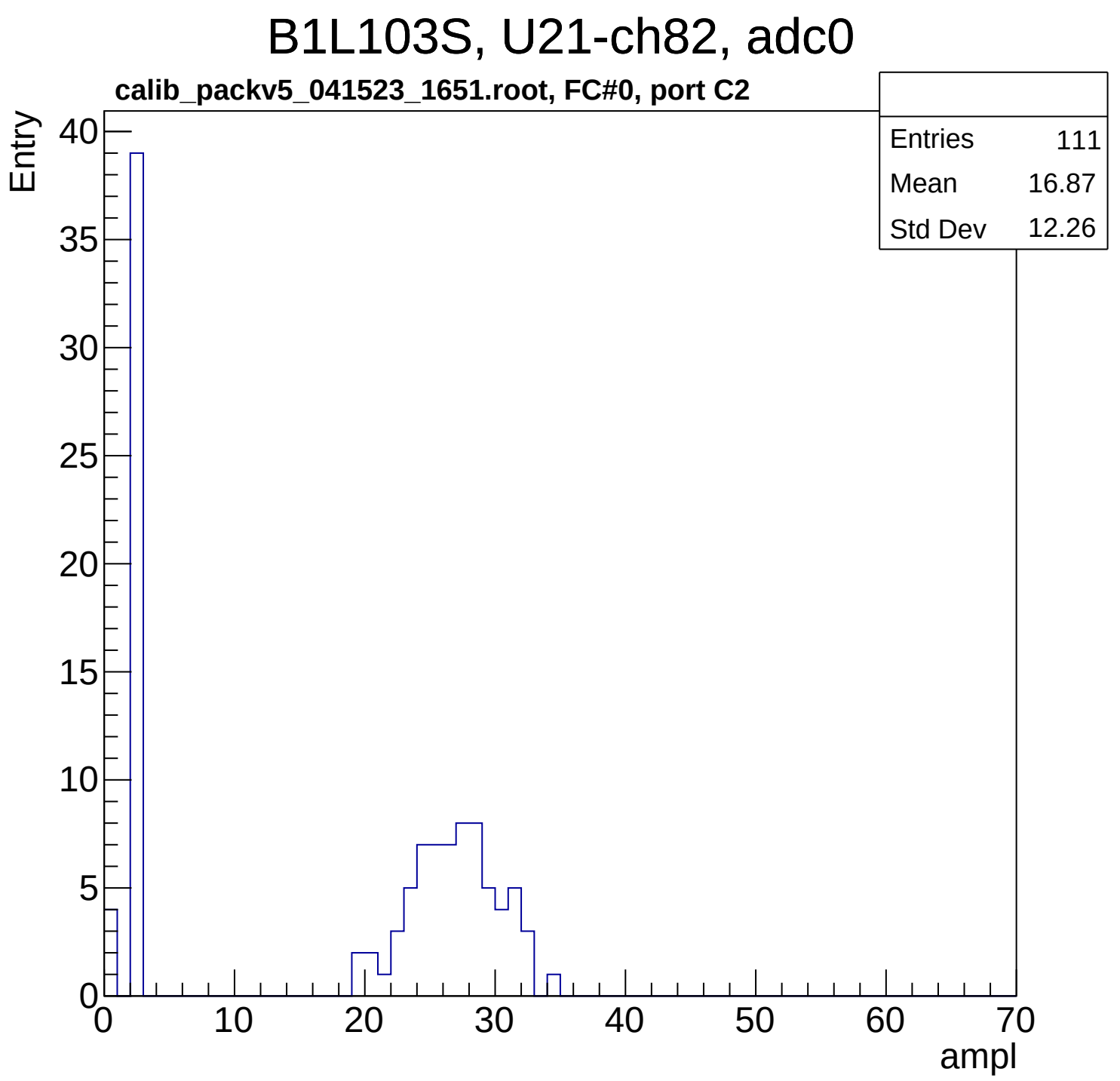

B1L103S, U21-ch81, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch82, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 111
Mean 16.87
Std Dev 12.26
Entry
ampl
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5
10
15
20
25
30
35
40
0
10
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40
50
60
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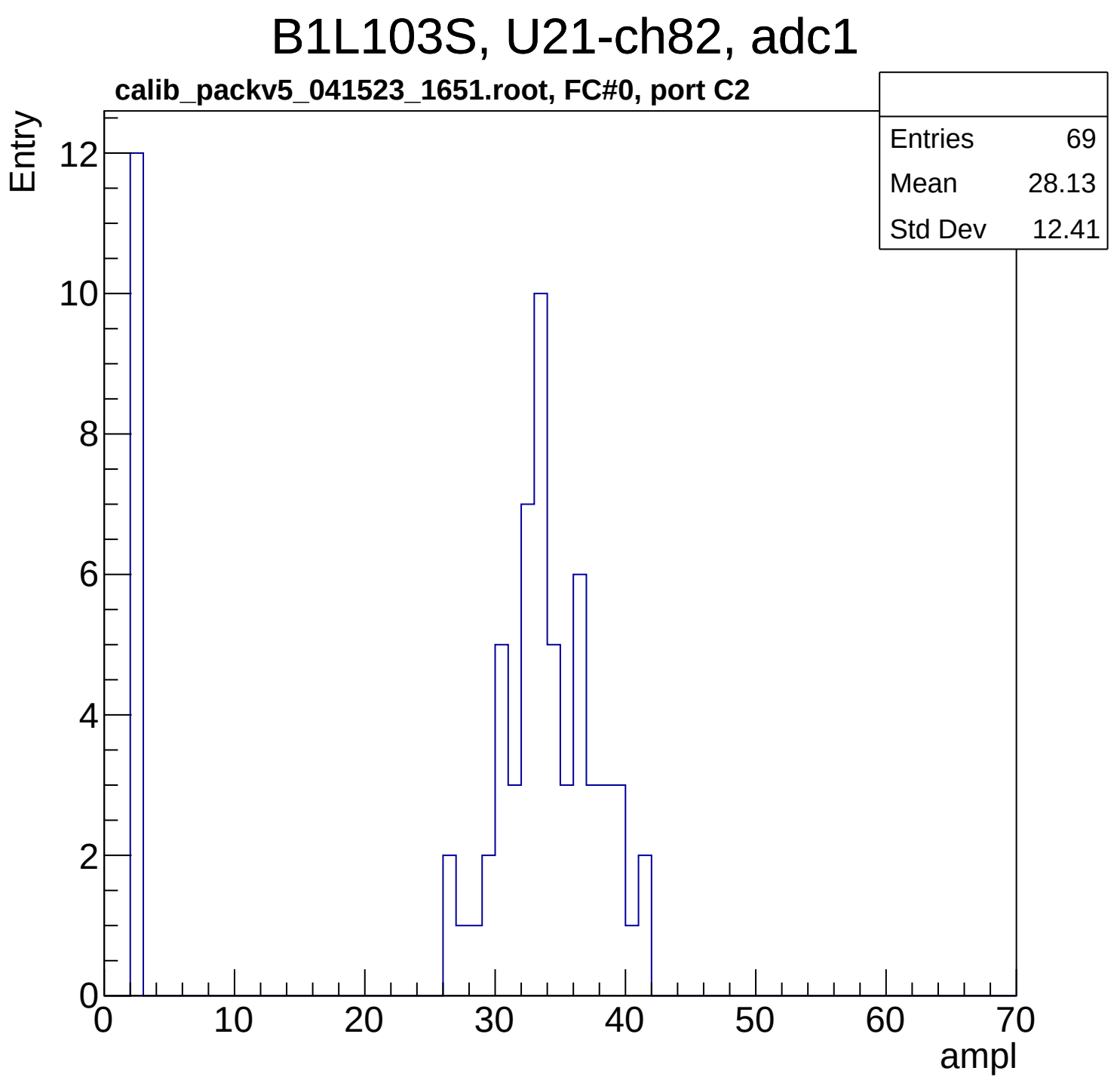
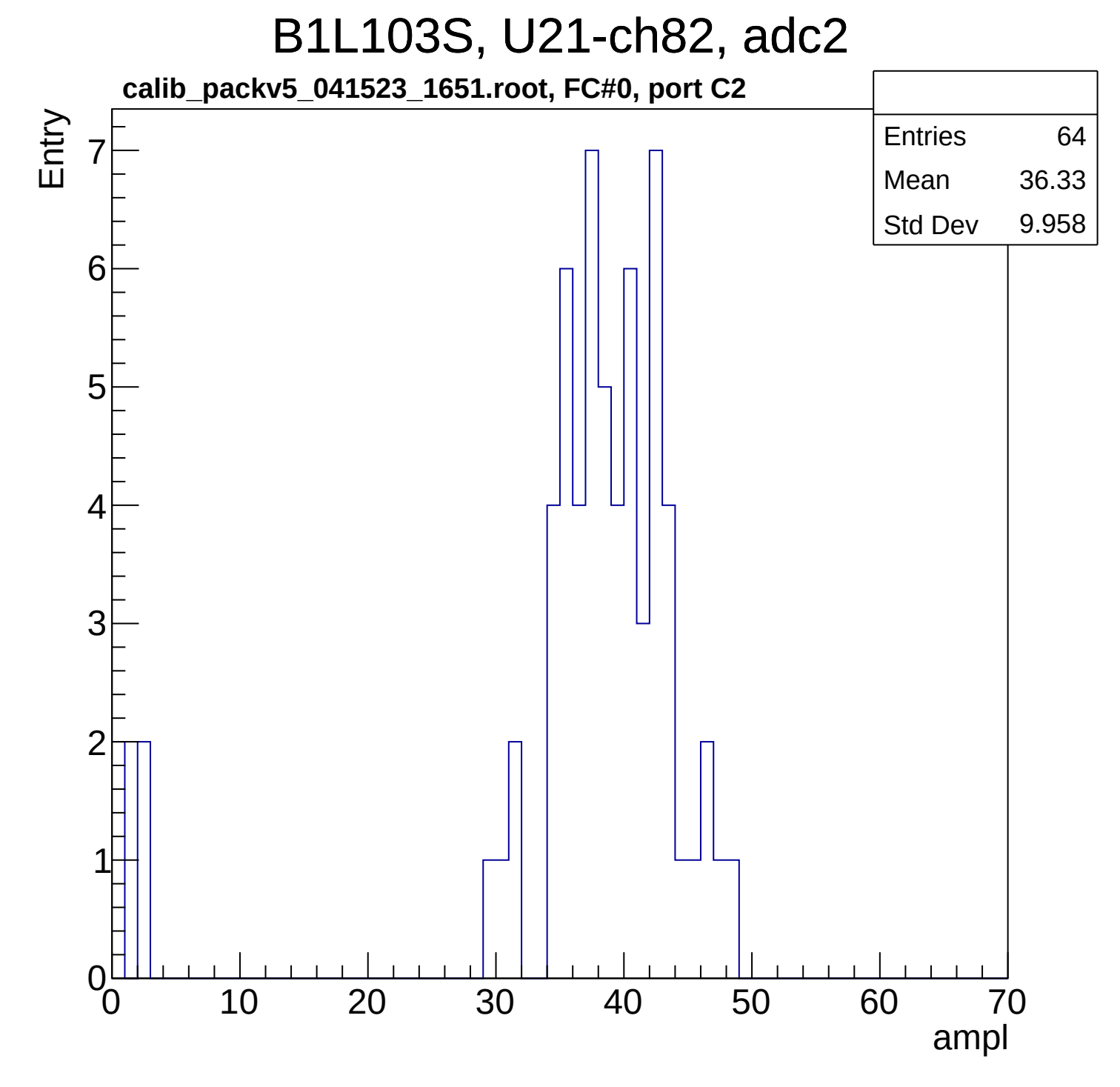
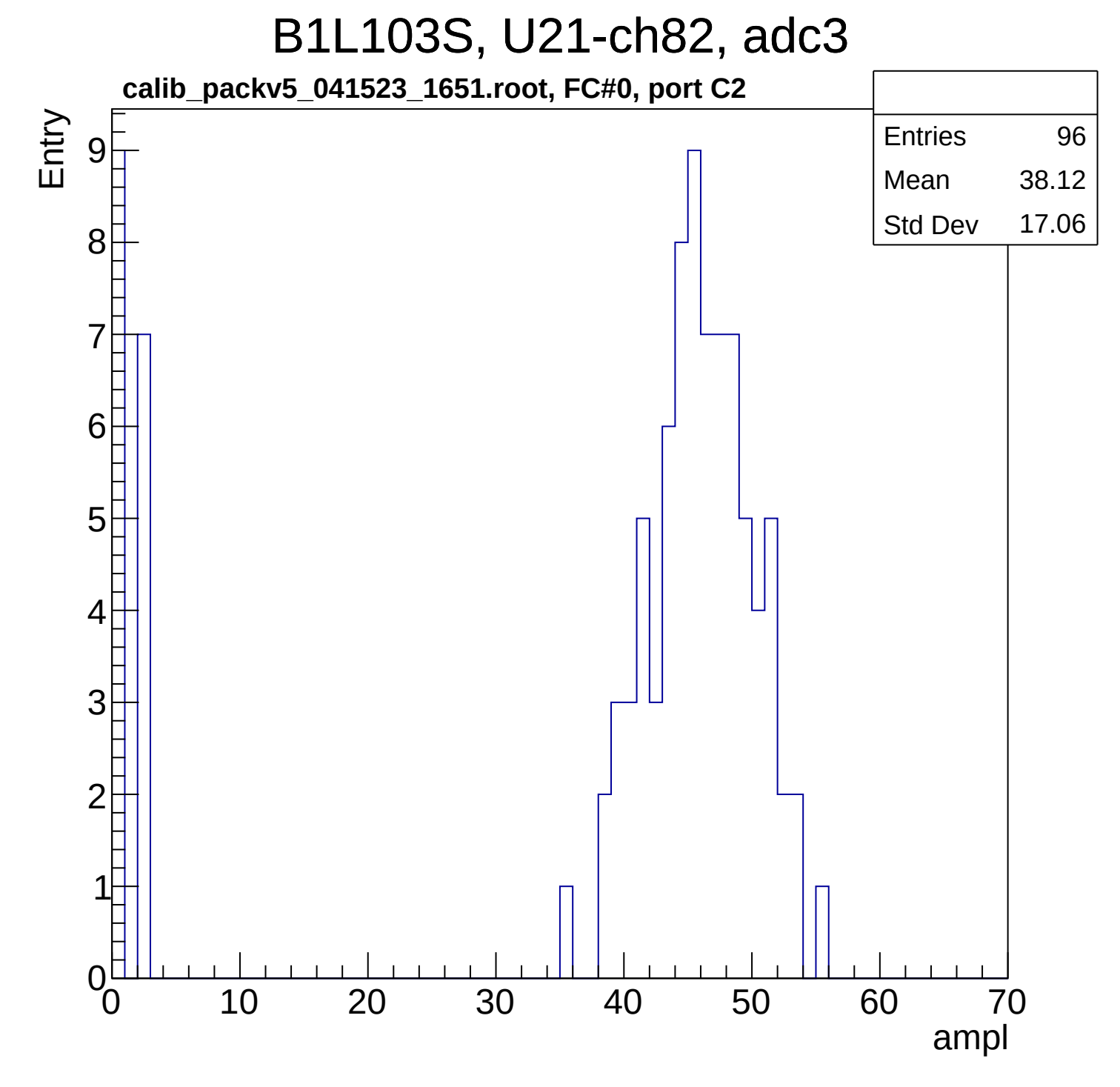

B1L103S, U21-ch82, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 28.13
Std Dev 12.41
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch82, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 36.33
Std Dev 9.958
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U21-ch82, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 96
Mean 38.12
Std Dev 17.06
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
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60
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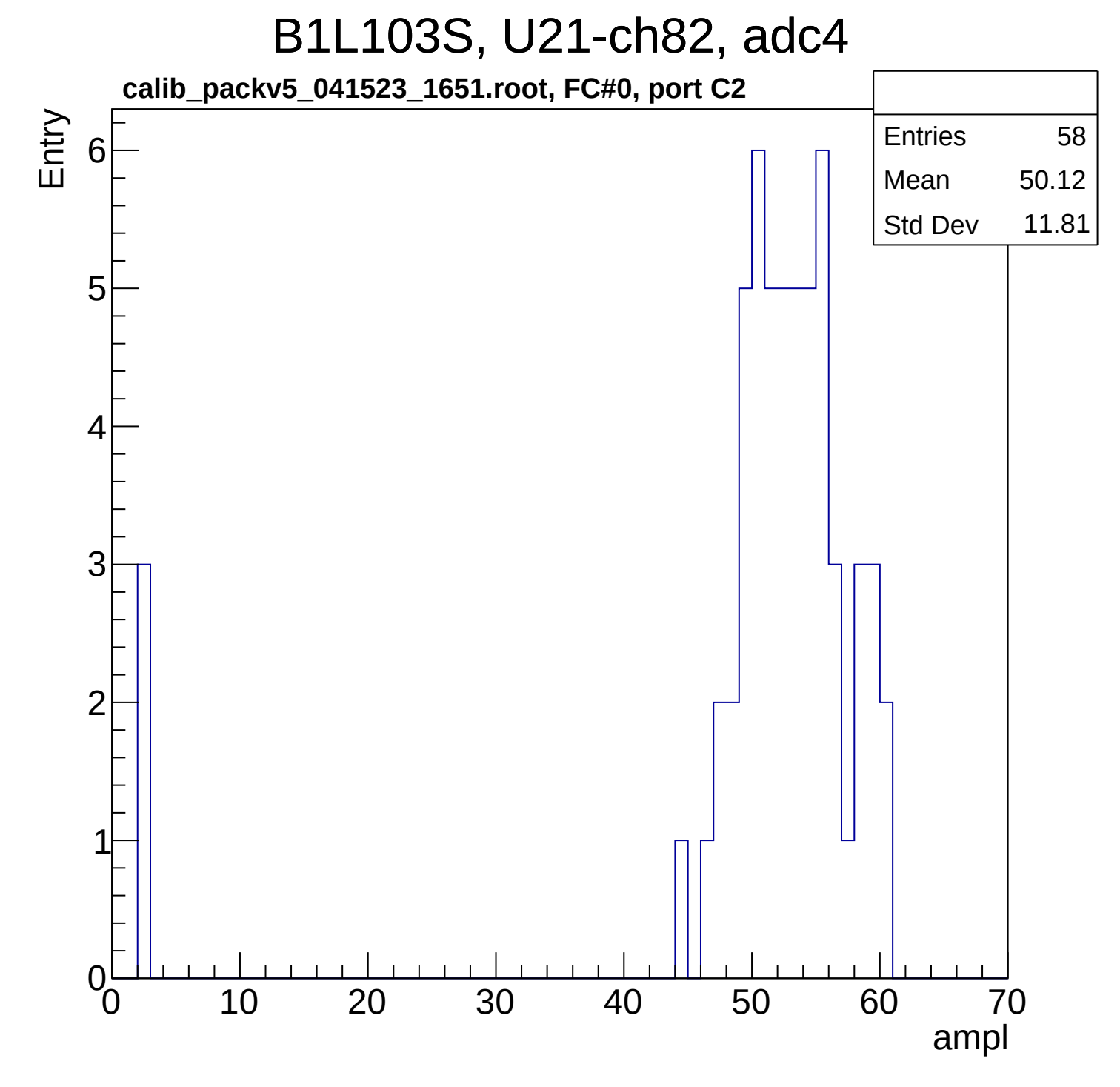
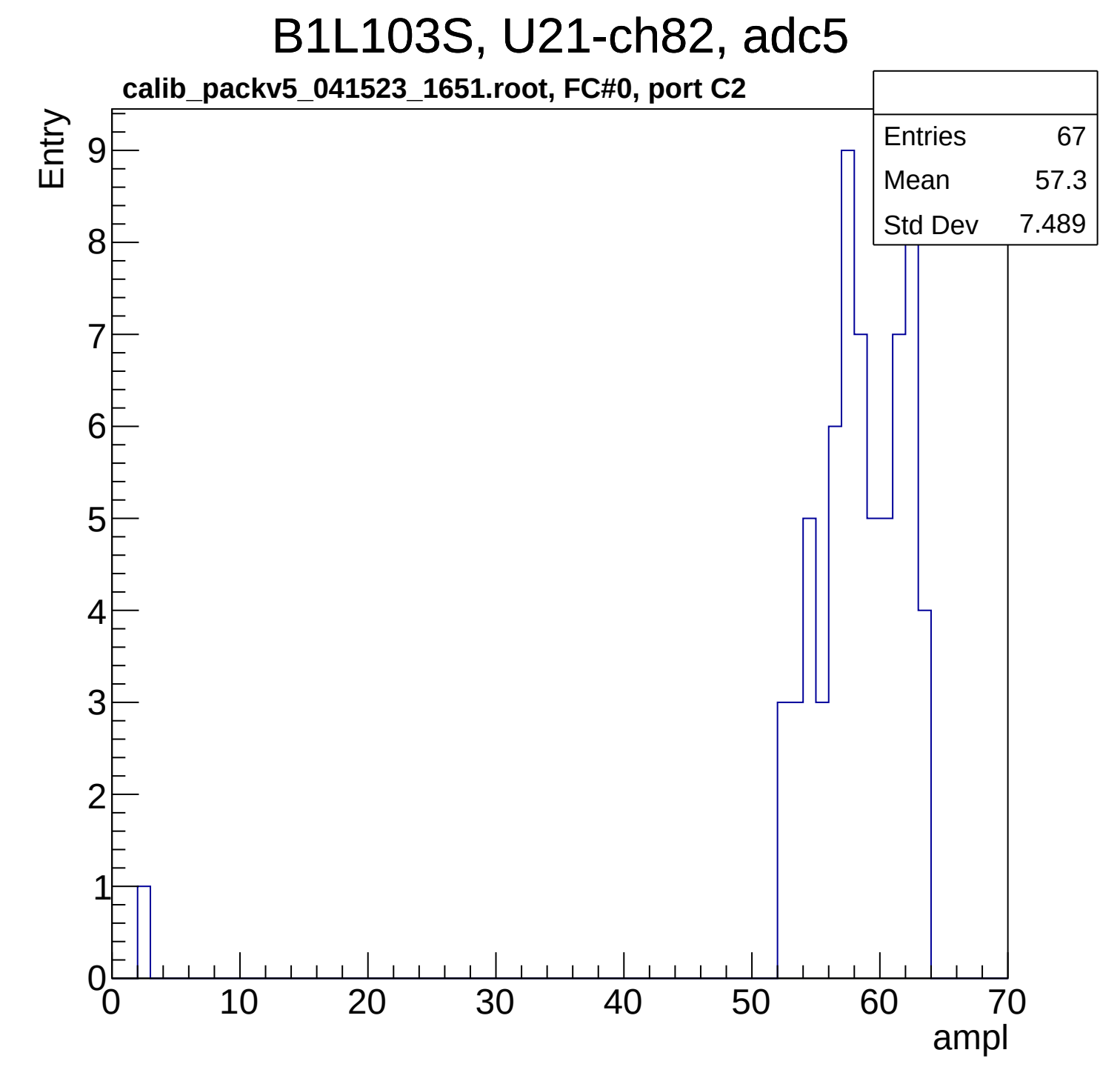

B1L103S, U21-ch82, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 50.12
Std Dev 11.81
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U21-ch82, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 57.3
Std Dev 7.489
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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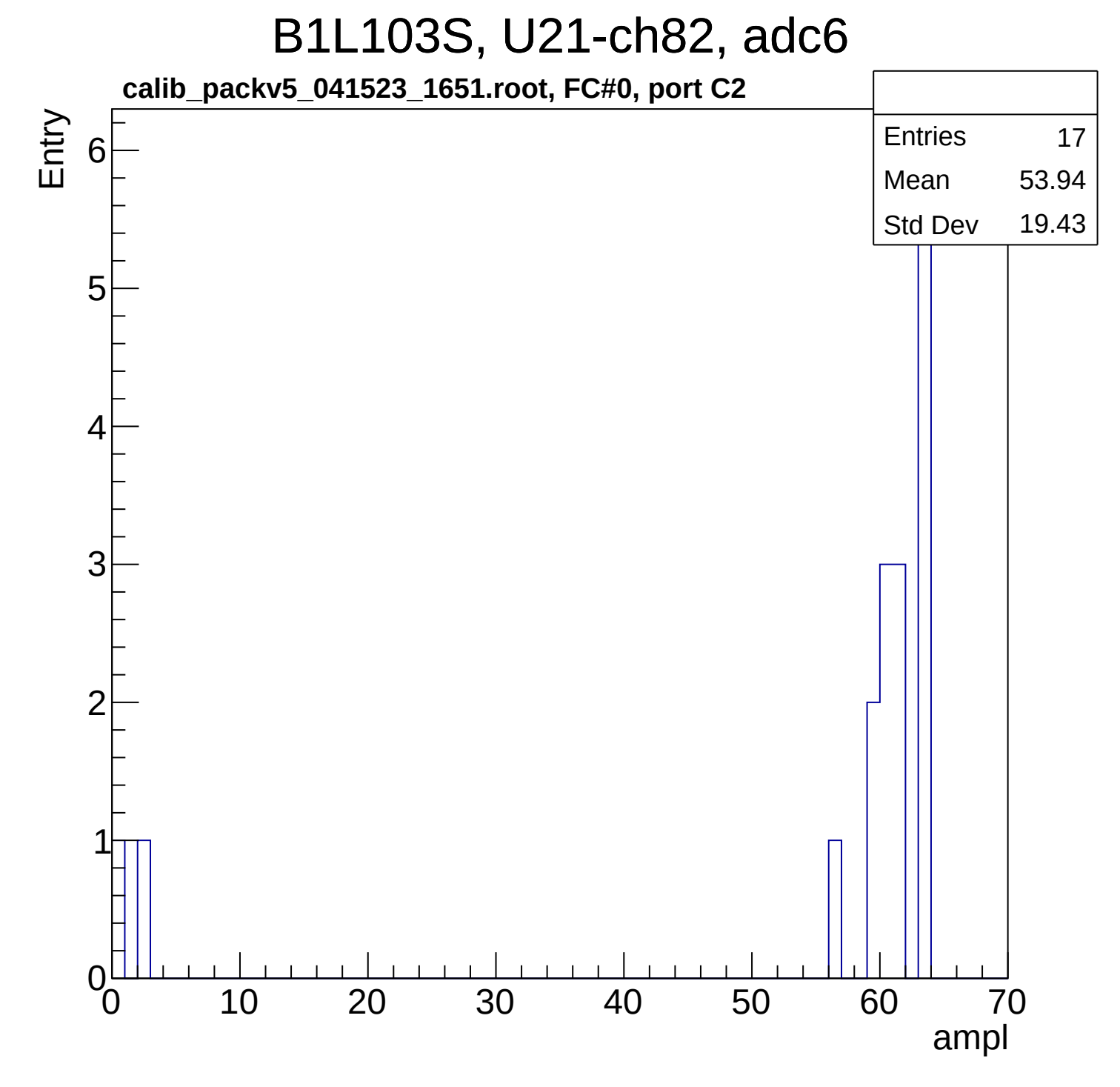
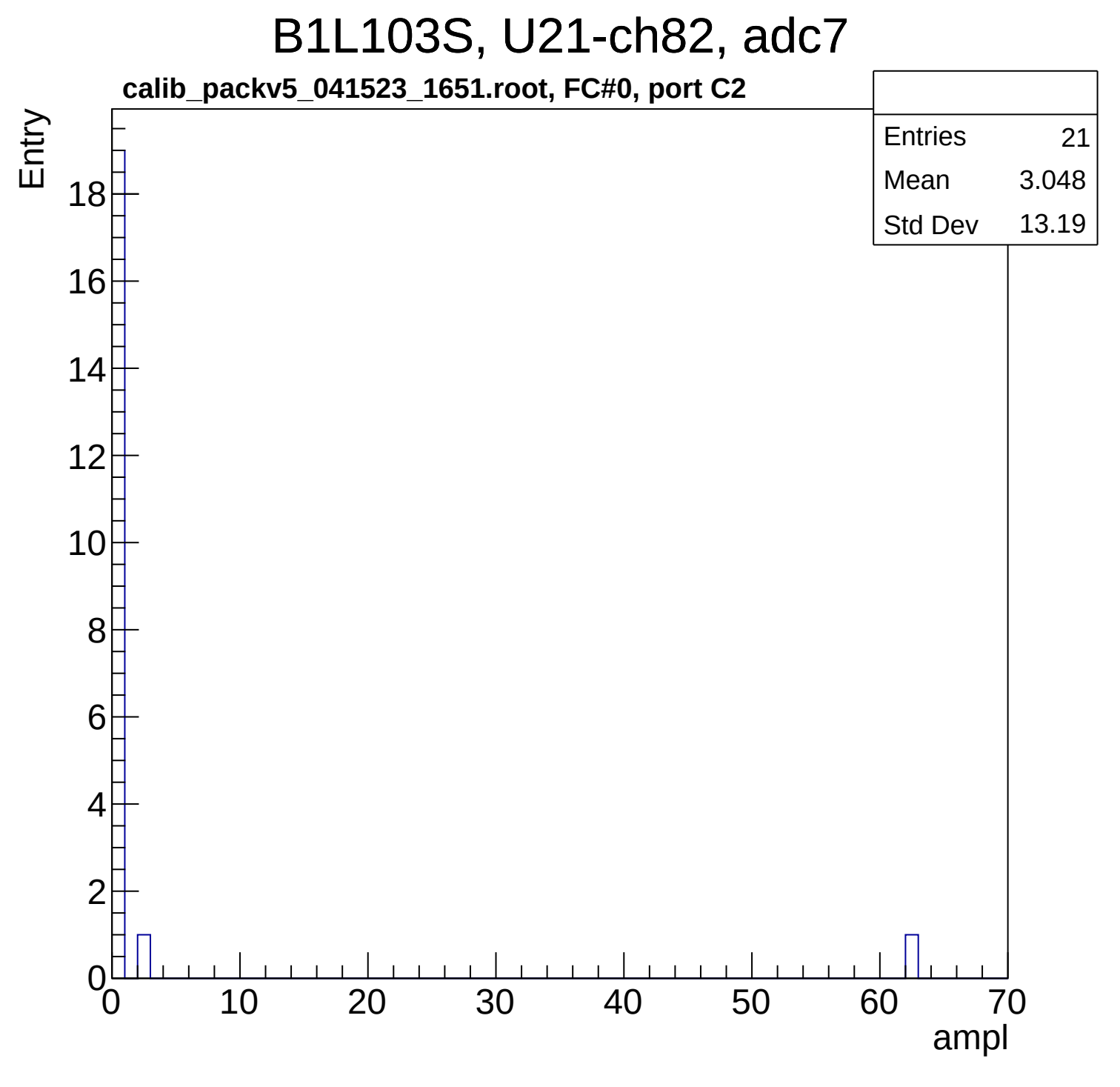
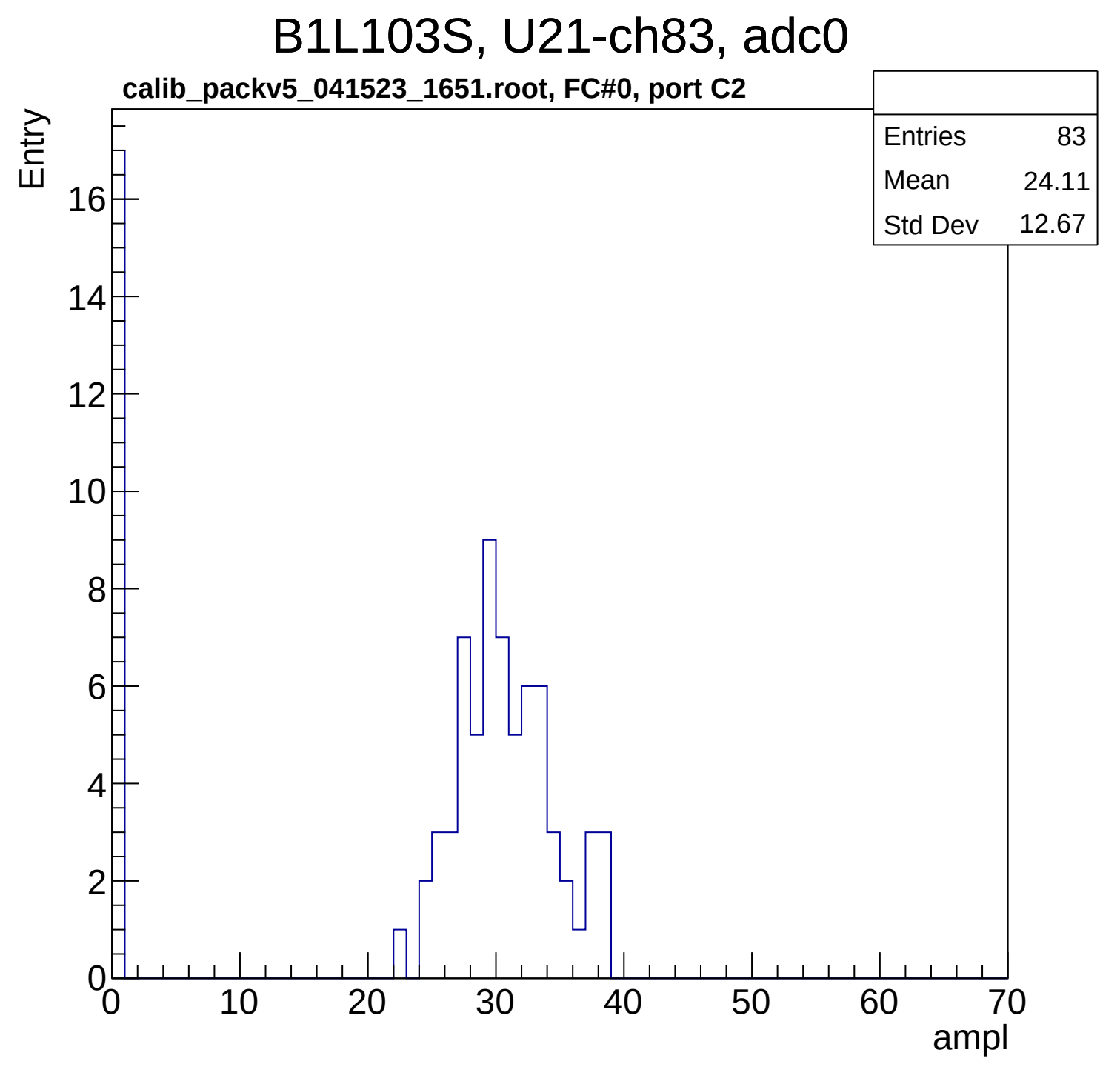
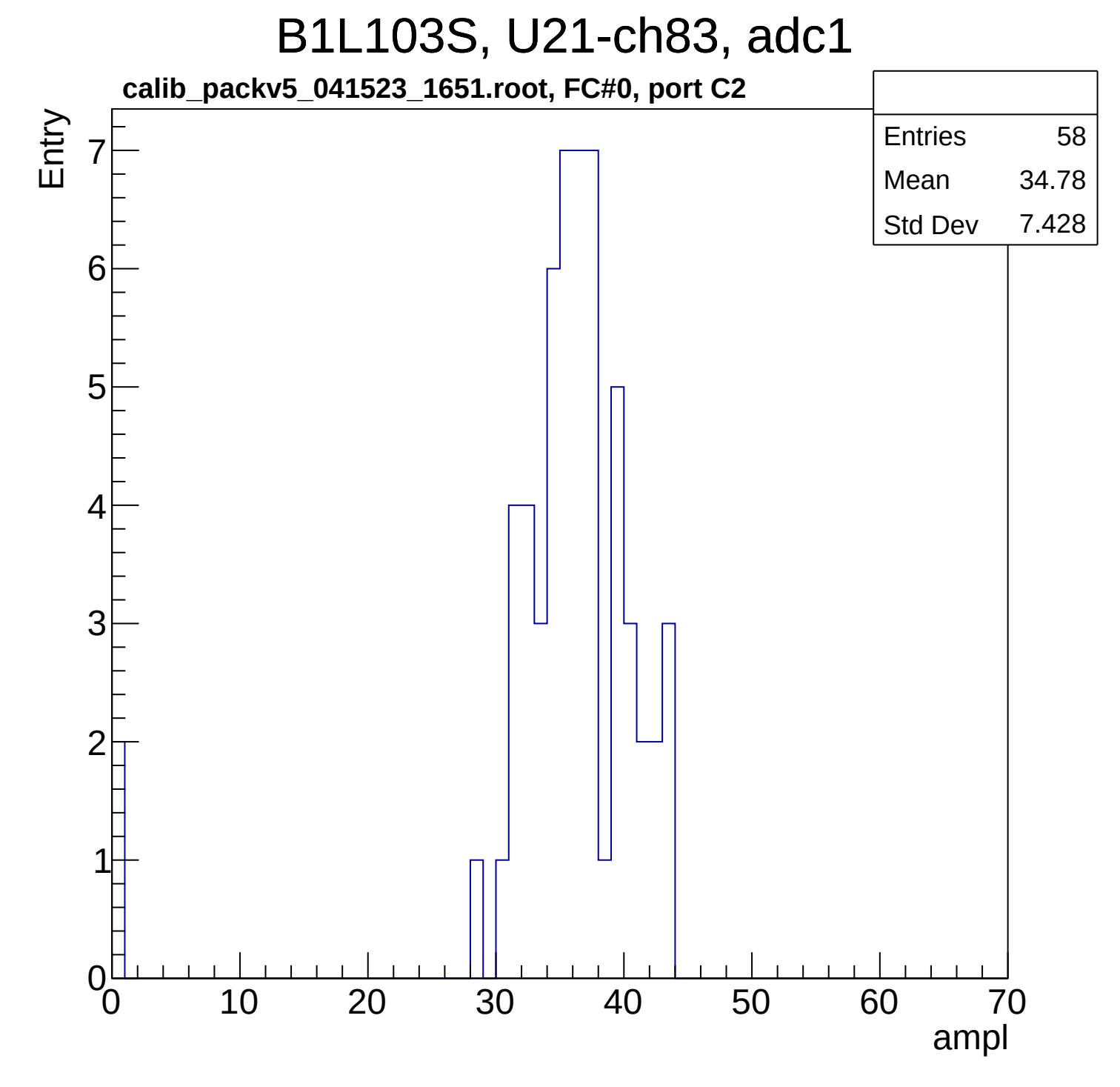
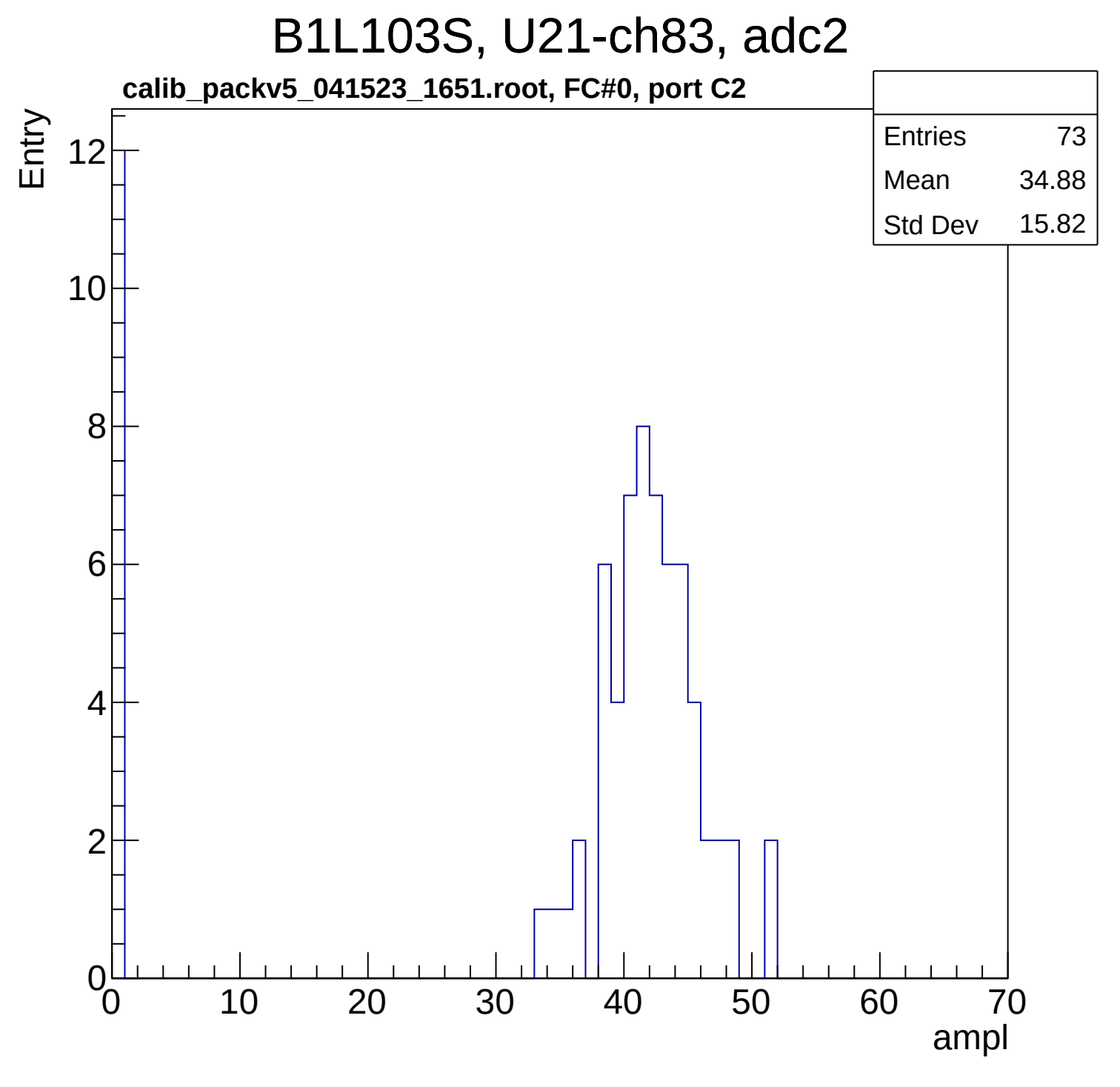
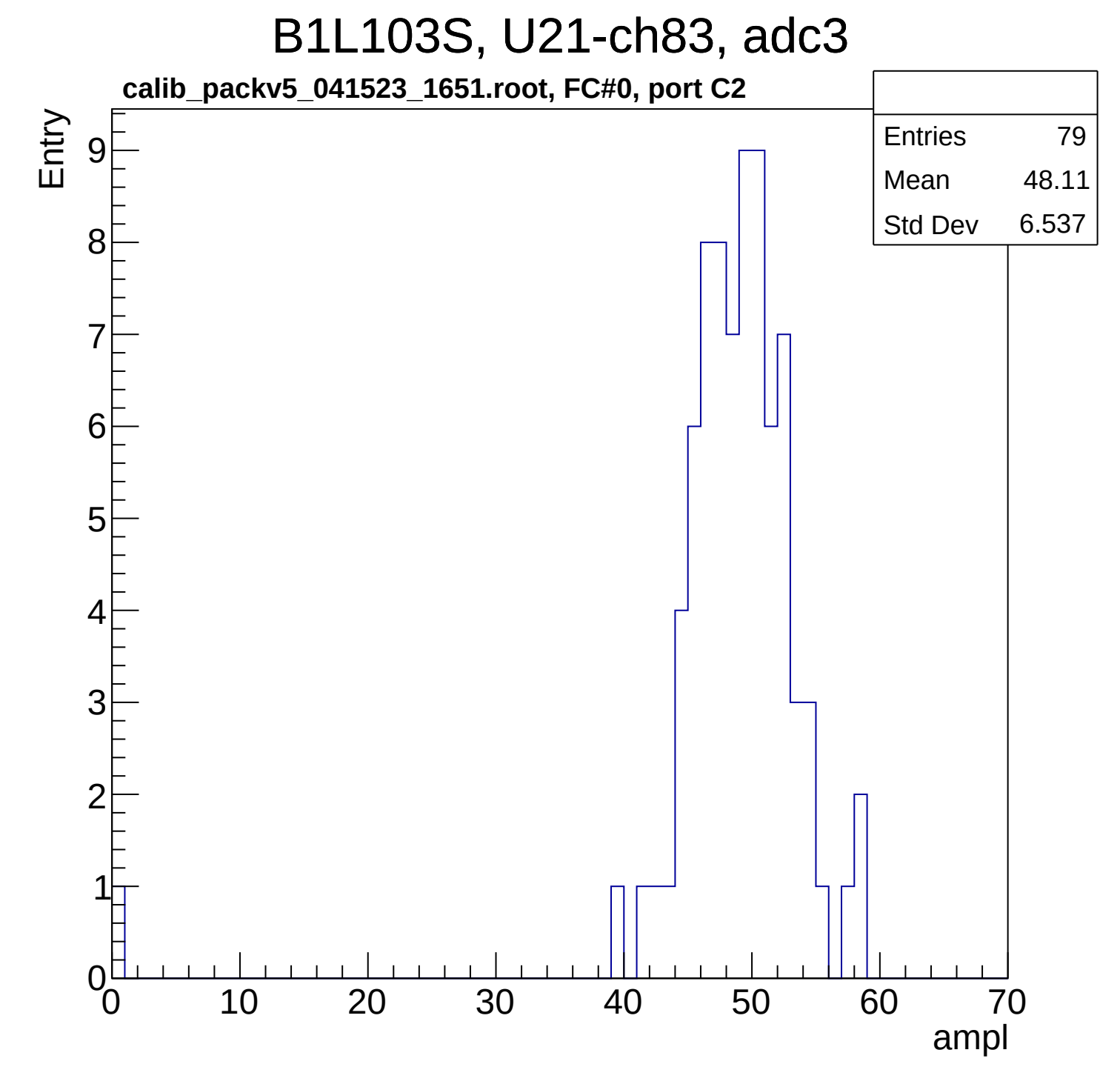

B1L103S, U21-ch82, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 53.94
Std Dev 19.43
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

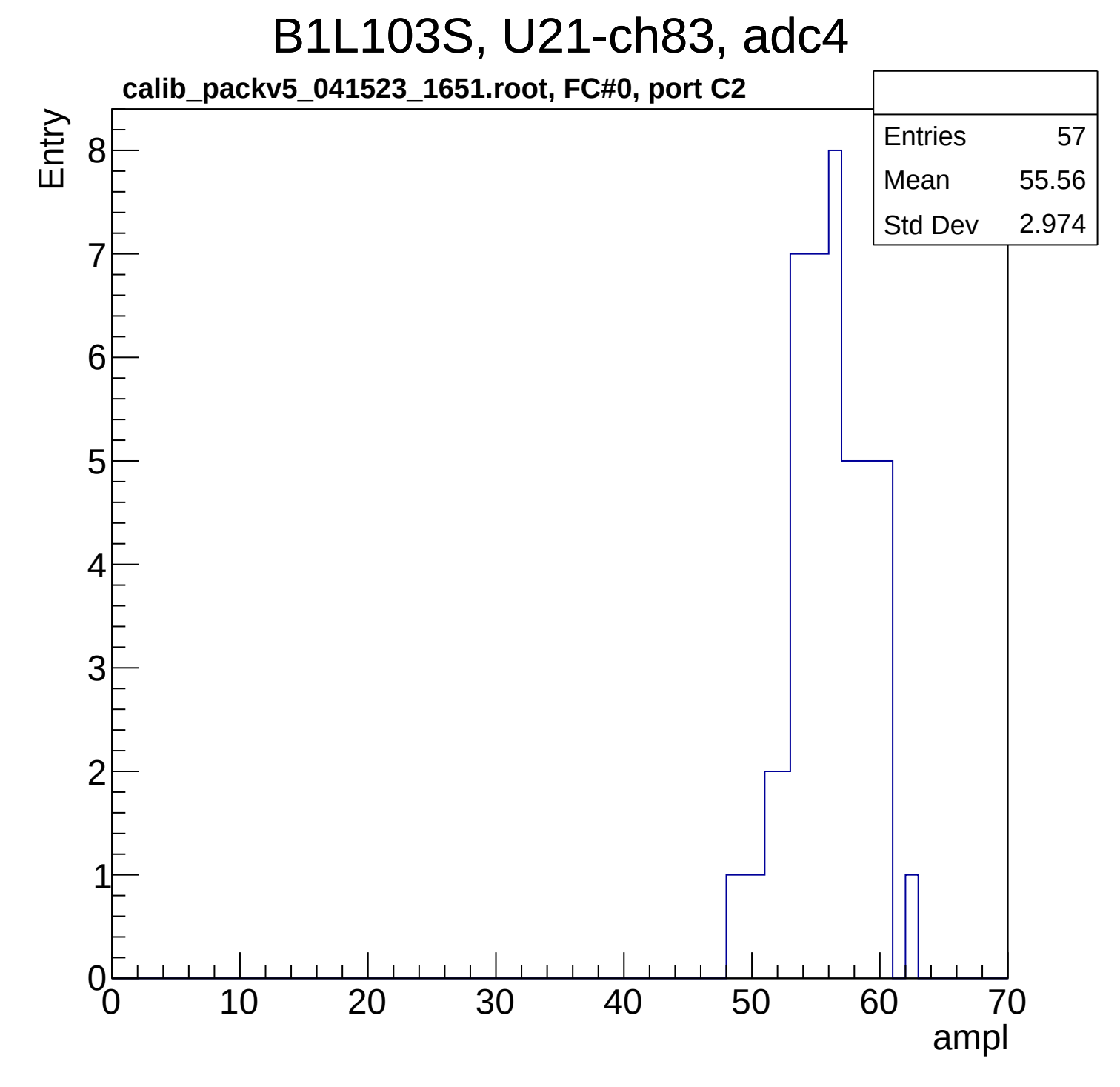

B1L103S, U21-ch82, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 3.048
Std Dev 13.19
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch83, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 24.11
Std Dev 12.67
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch83, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 34.78
Std Dev 7.428
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U21-ch83, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 34.88
Std Dev 15.82
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch83, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 48.11
Std Dev 6.537
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch83, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 55.56
Std Dev 2.974
Entry
ampl
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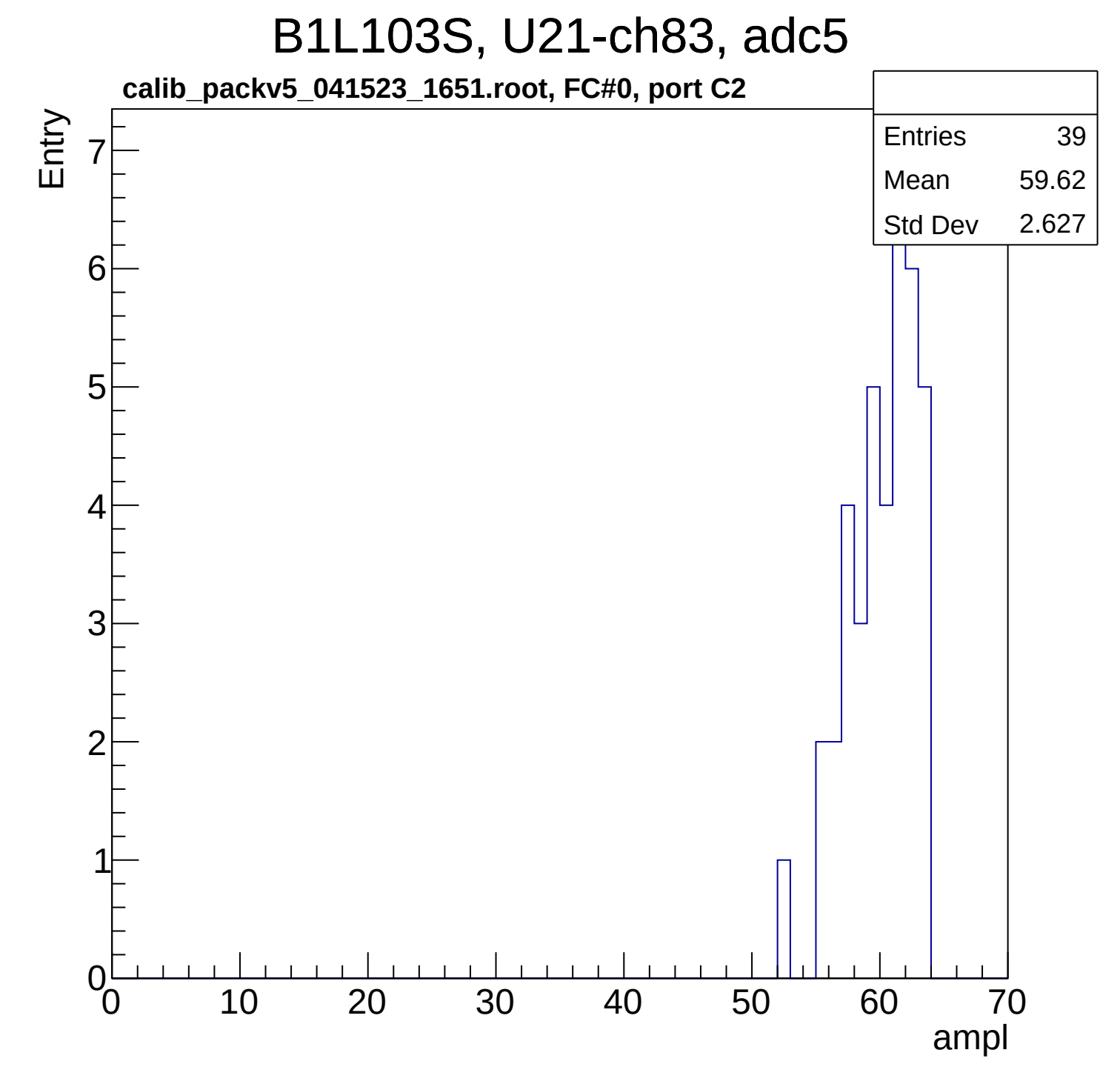
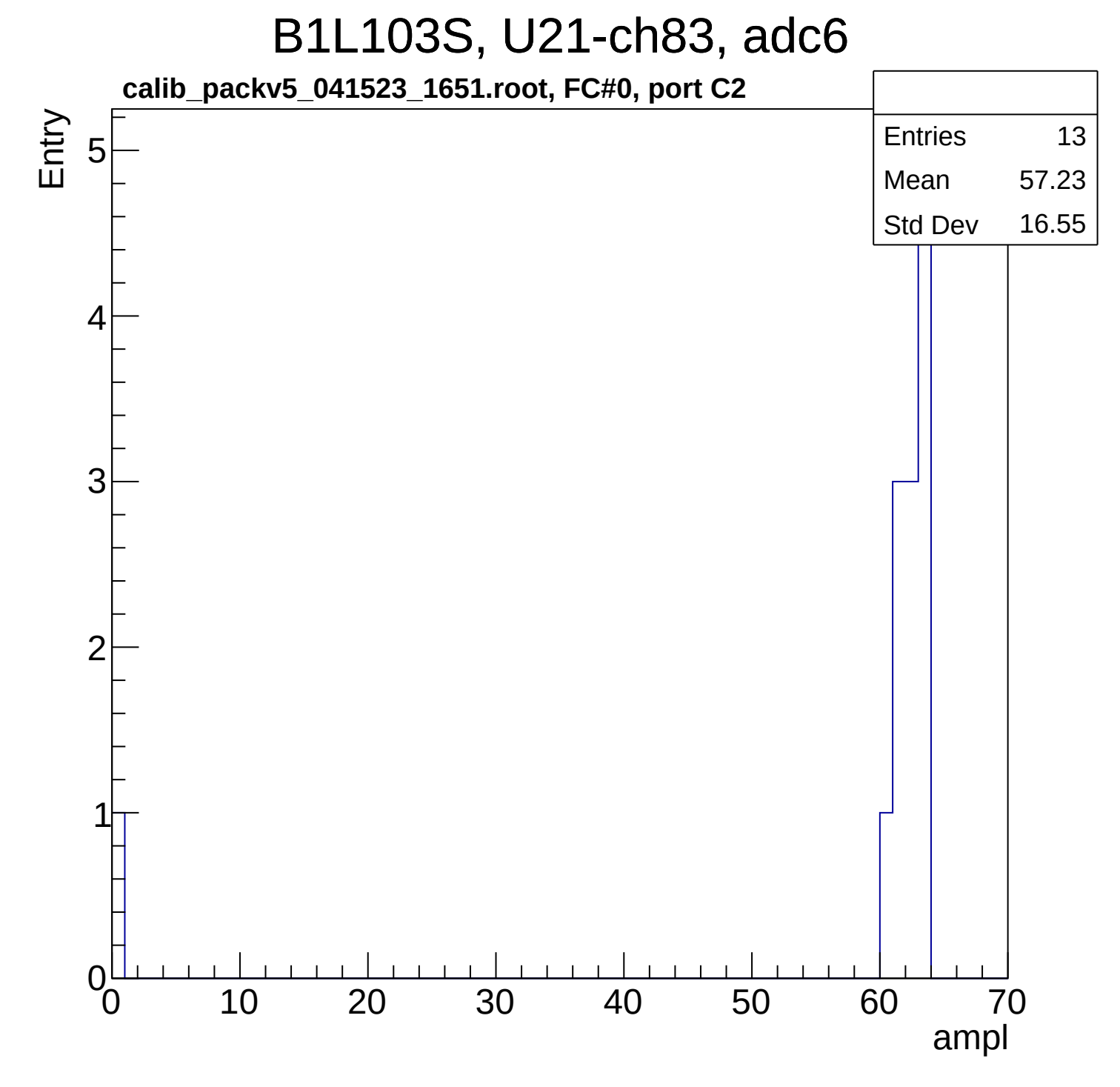
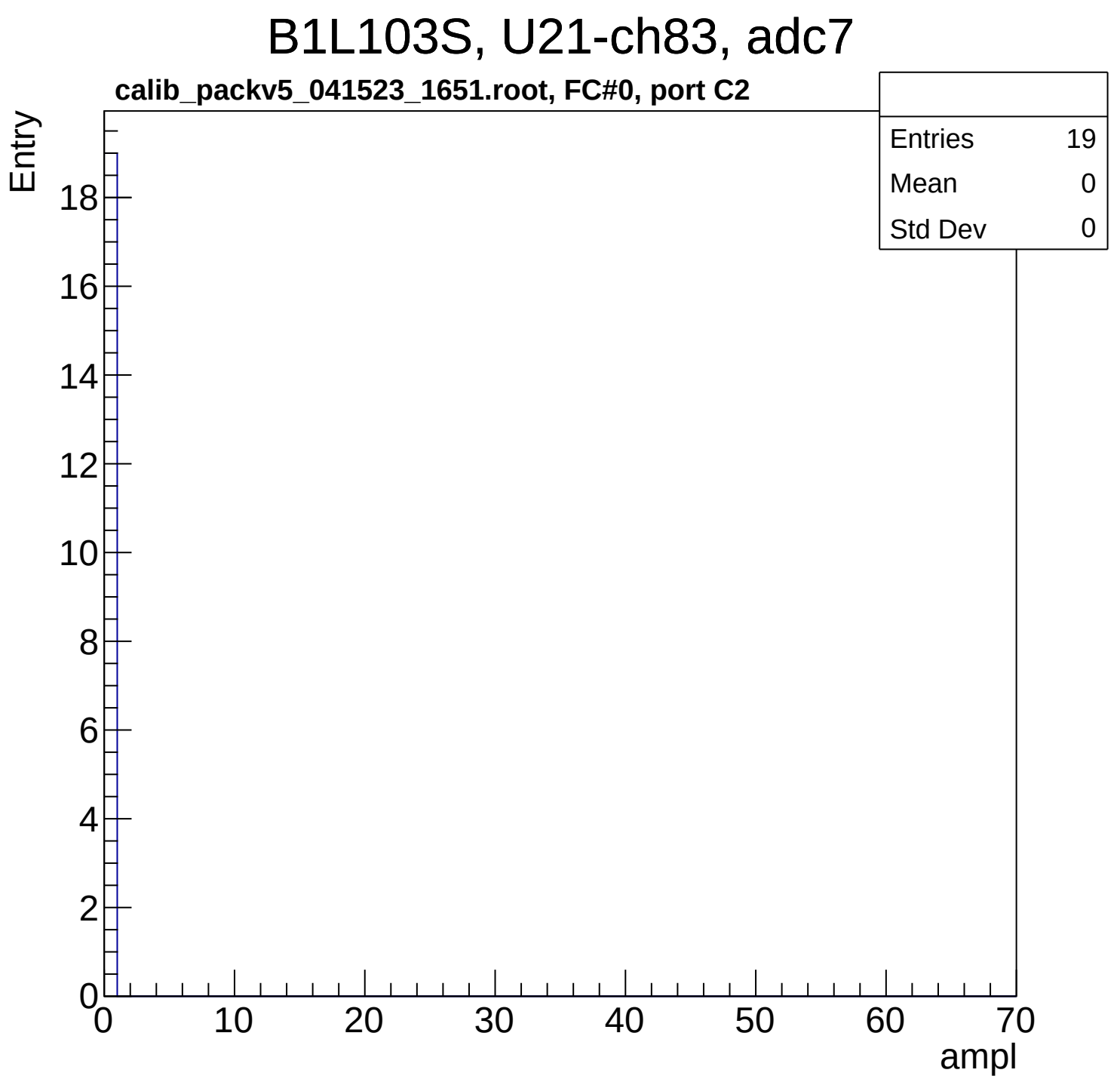
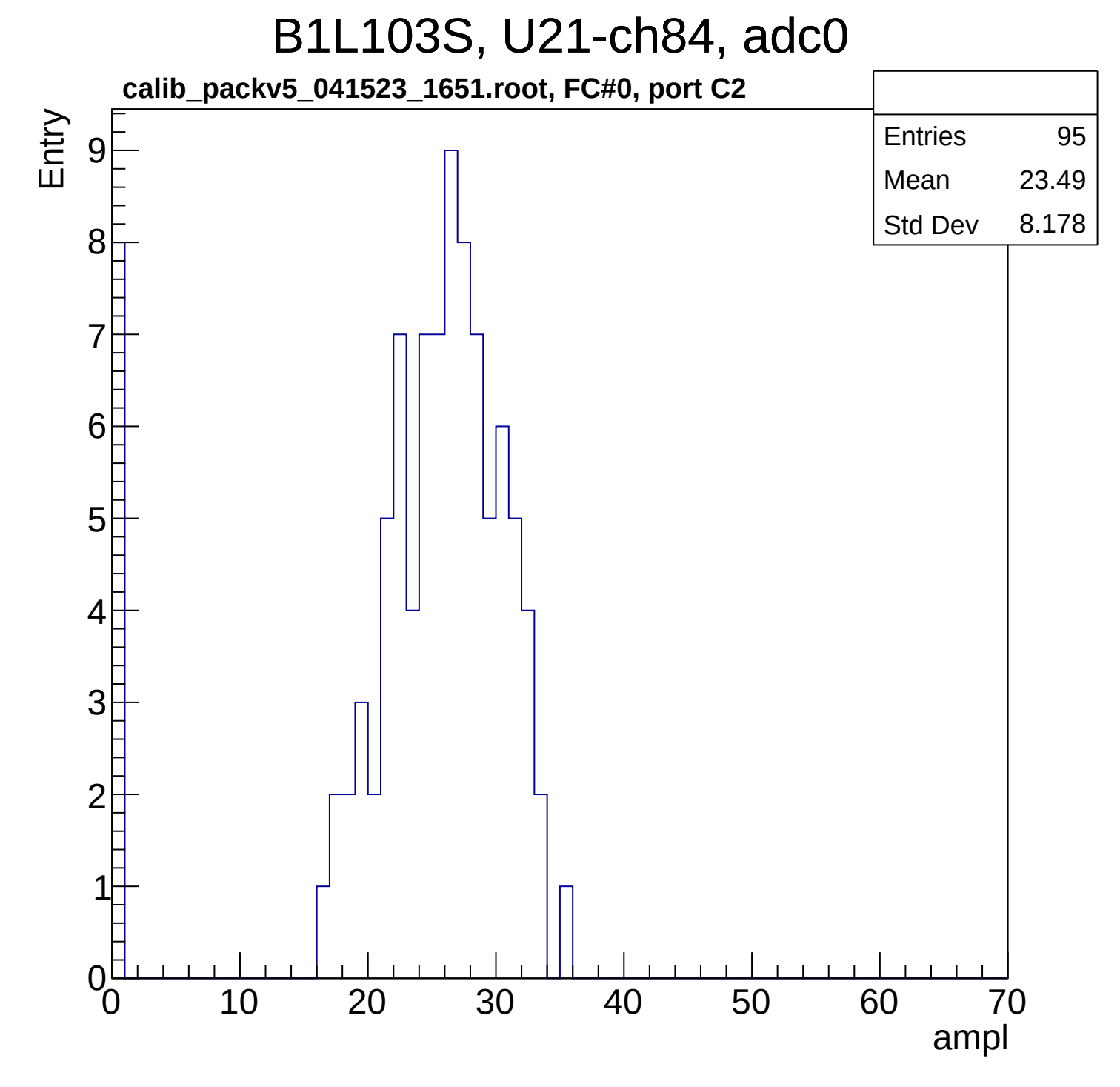
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch83, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 59.62
Std Dev 2.627
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U21-ch83, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 57.23
Std Dev 16.55
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch83, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch84, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 23.49
Std Dev 8.178
Entry
ampl
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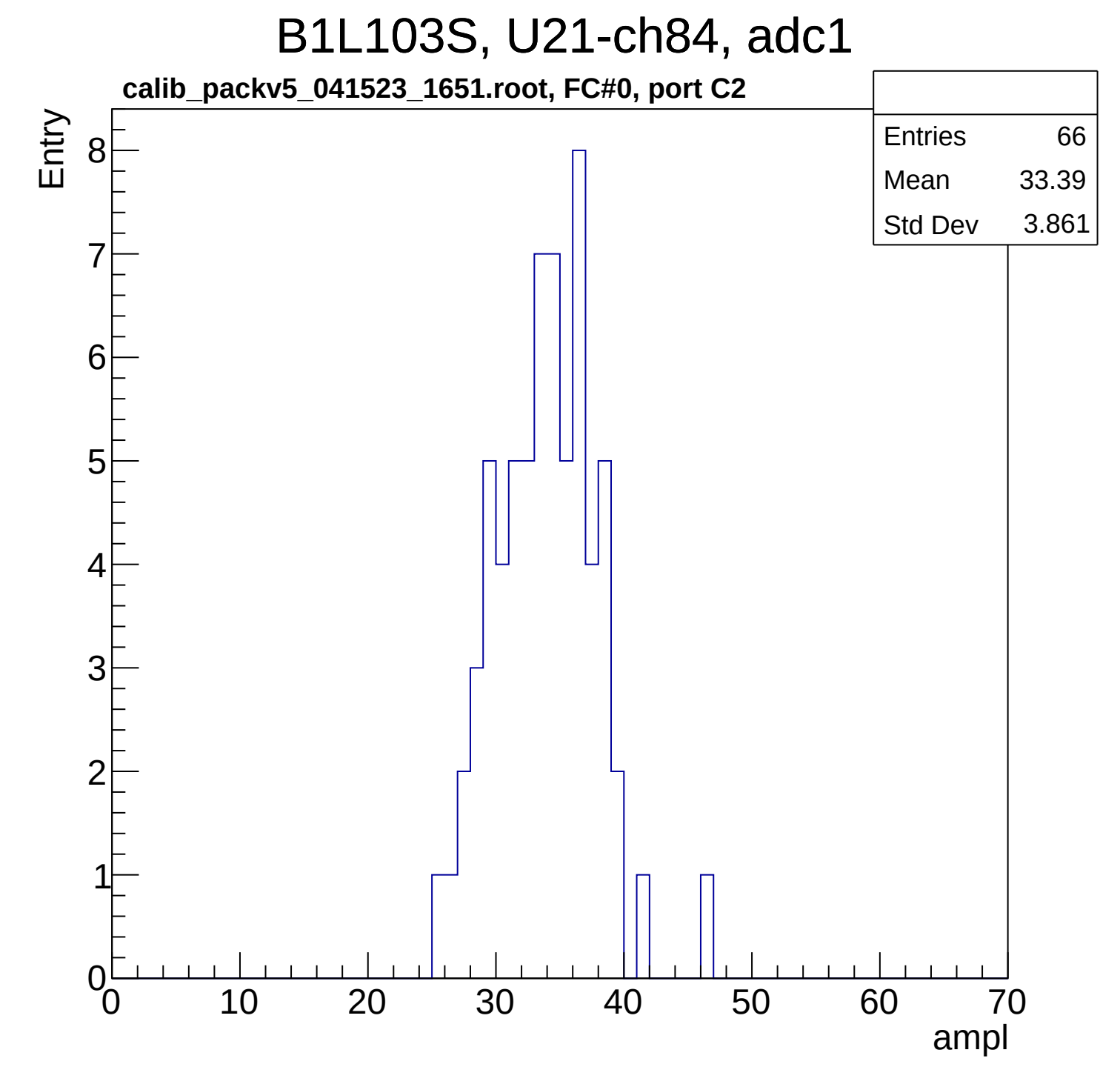
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch84, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 33.39
Std Dev 3.861
Entry
ampl
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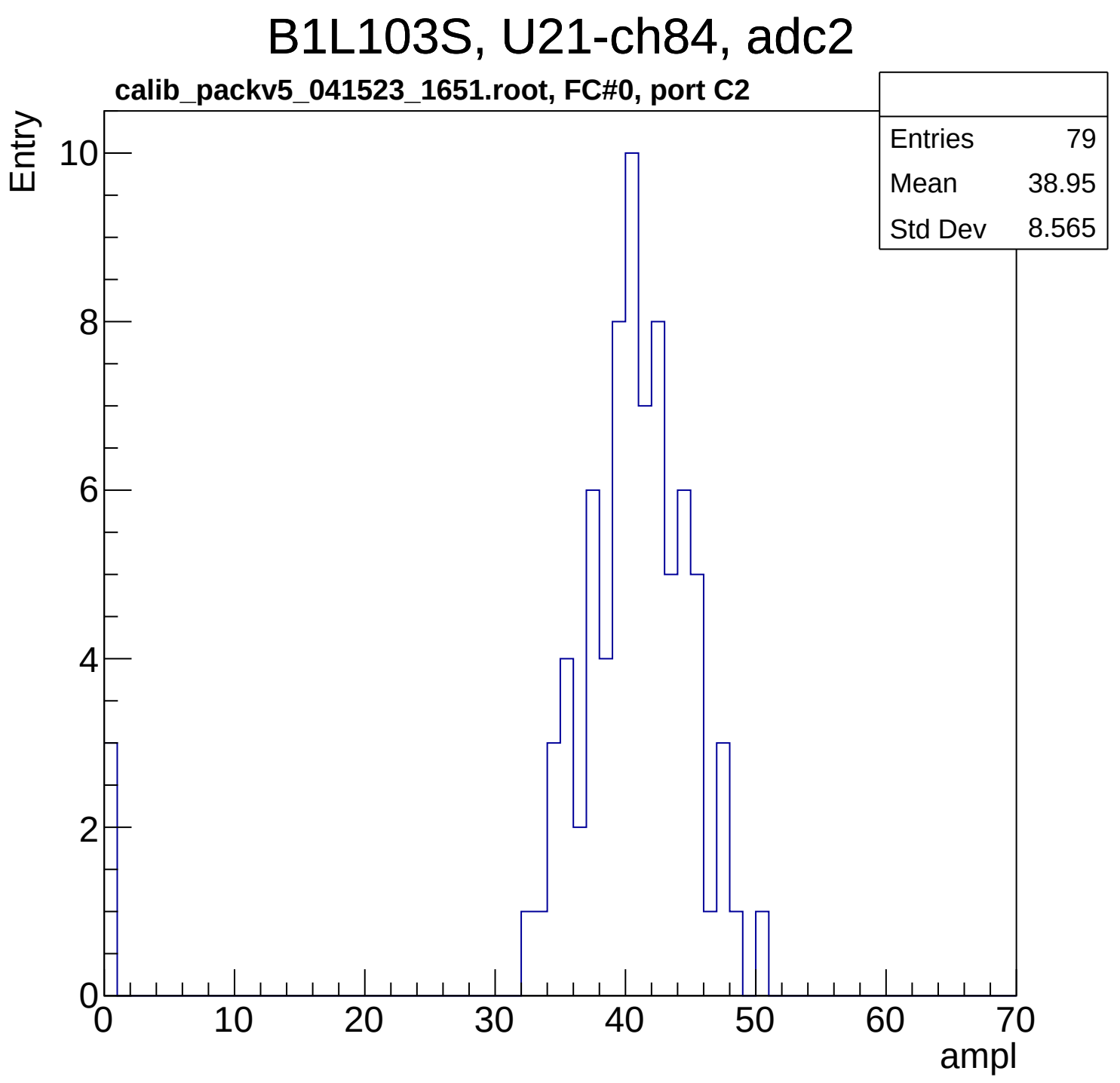
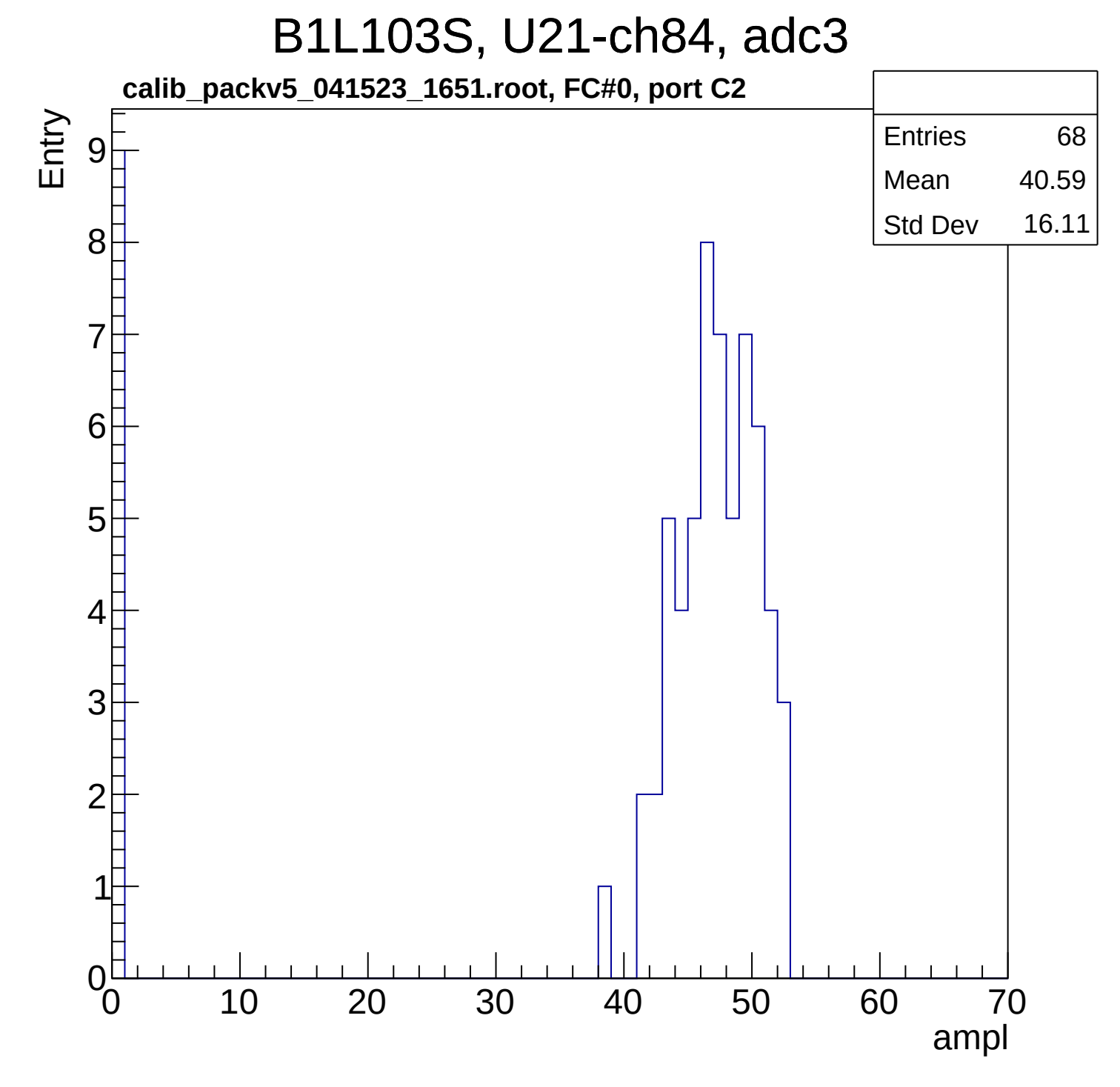
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch84, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 38.95
Std Dev 8.565
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch84, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 40.59
Std Dev 16.11
Entry
ampl
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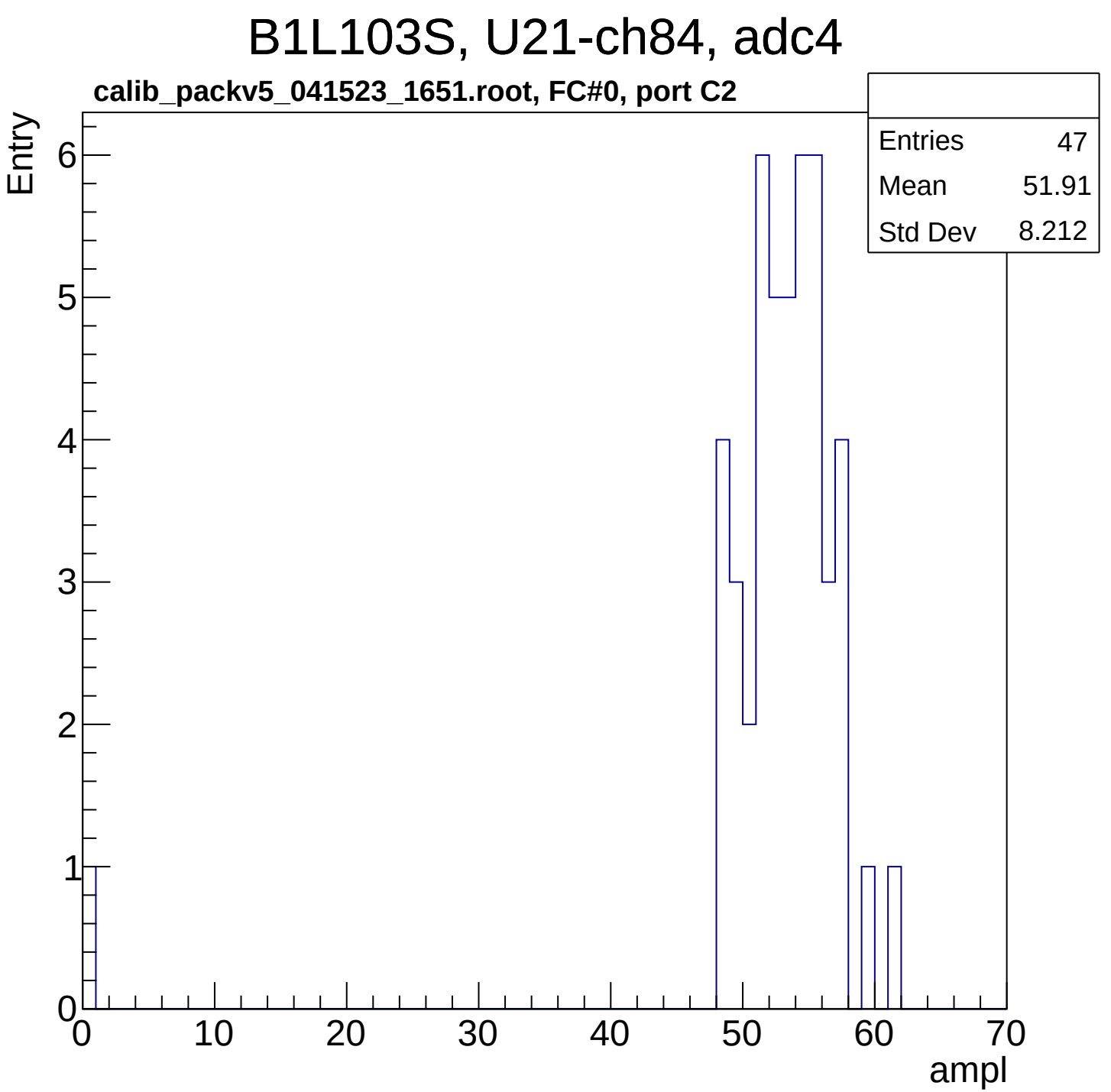
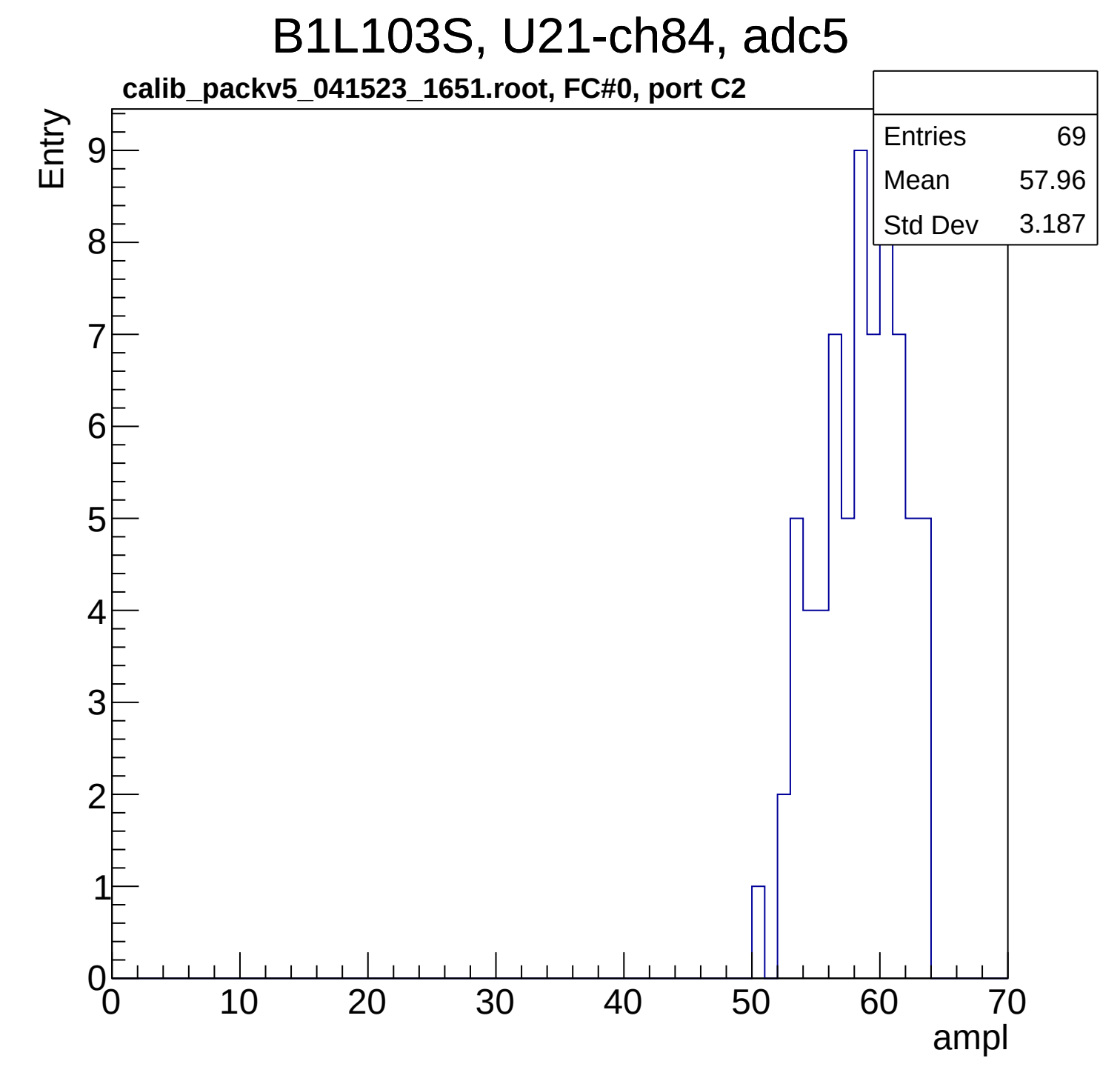
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch84, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 51.91
Std Dev 8.212
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch84, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 57.96
Std Dev 3.187
Entry
ampl
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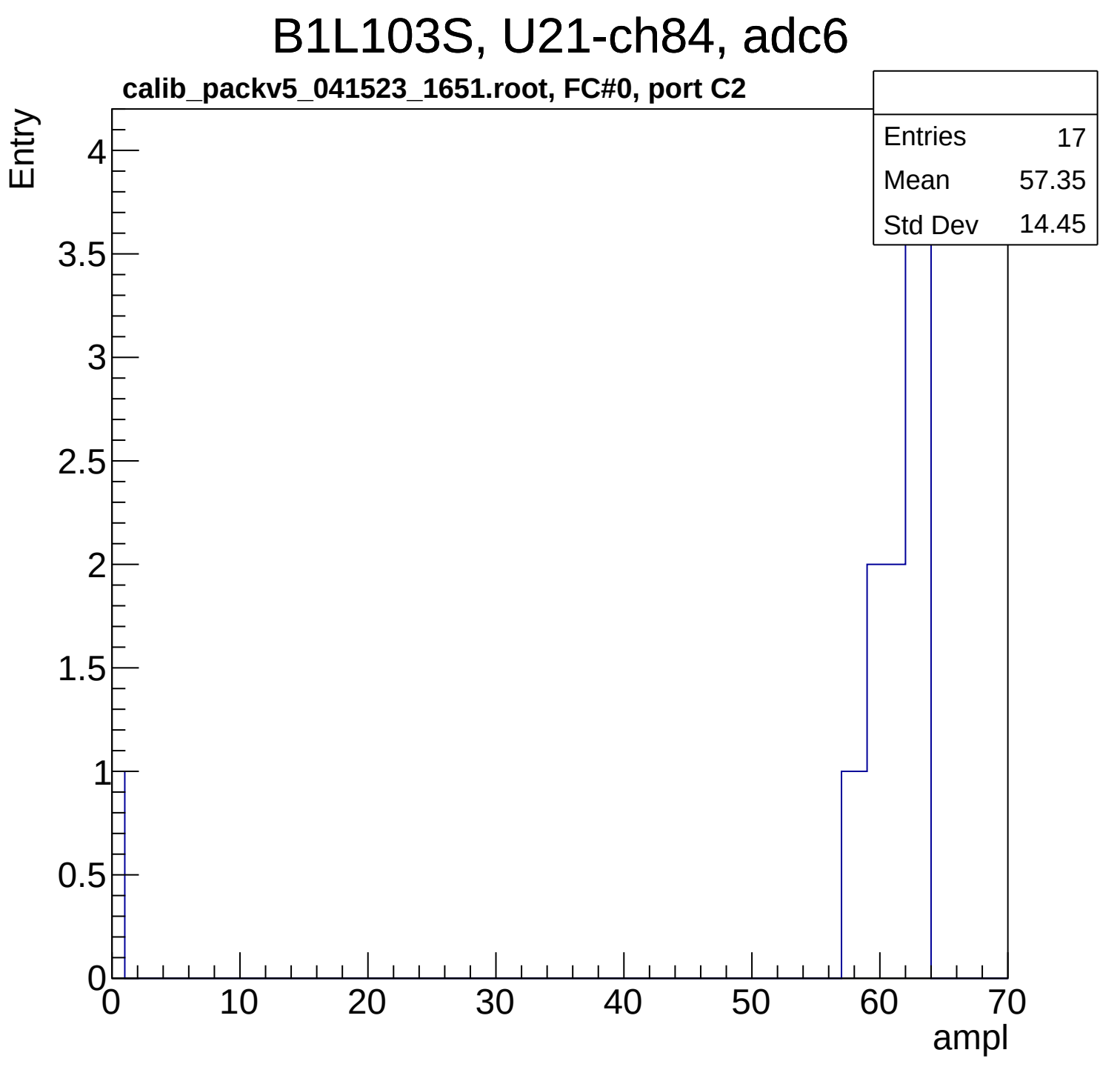
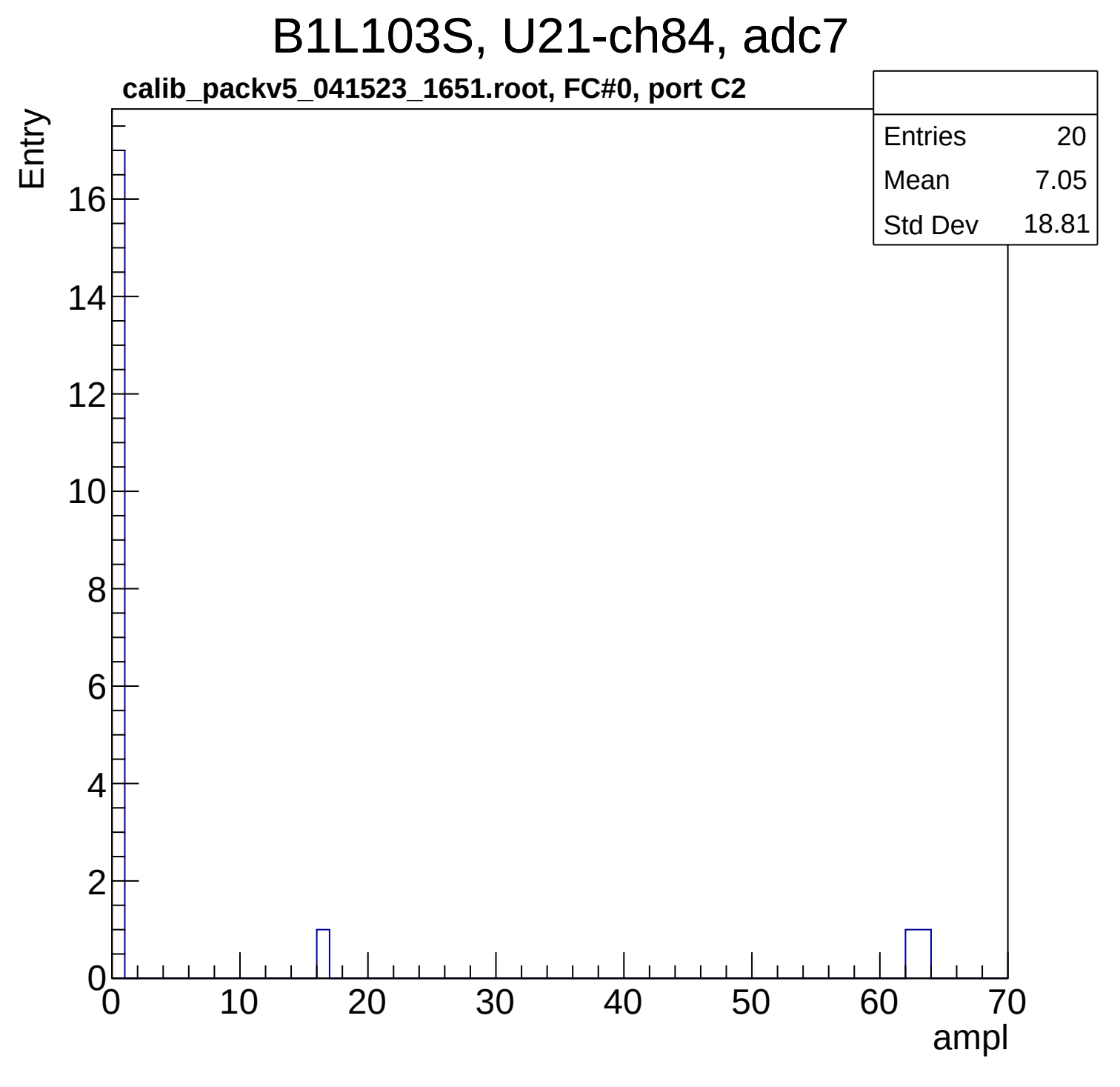
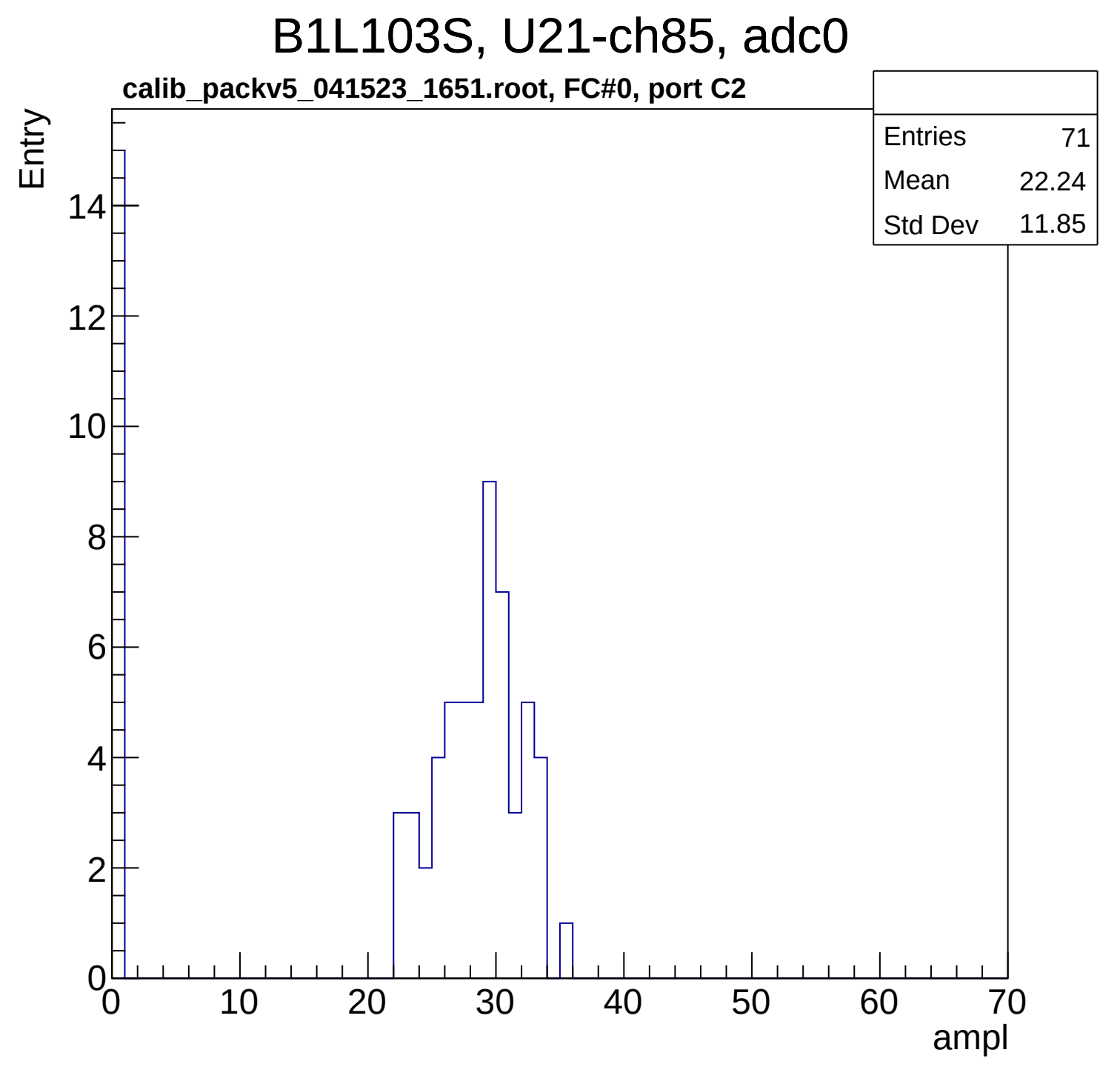
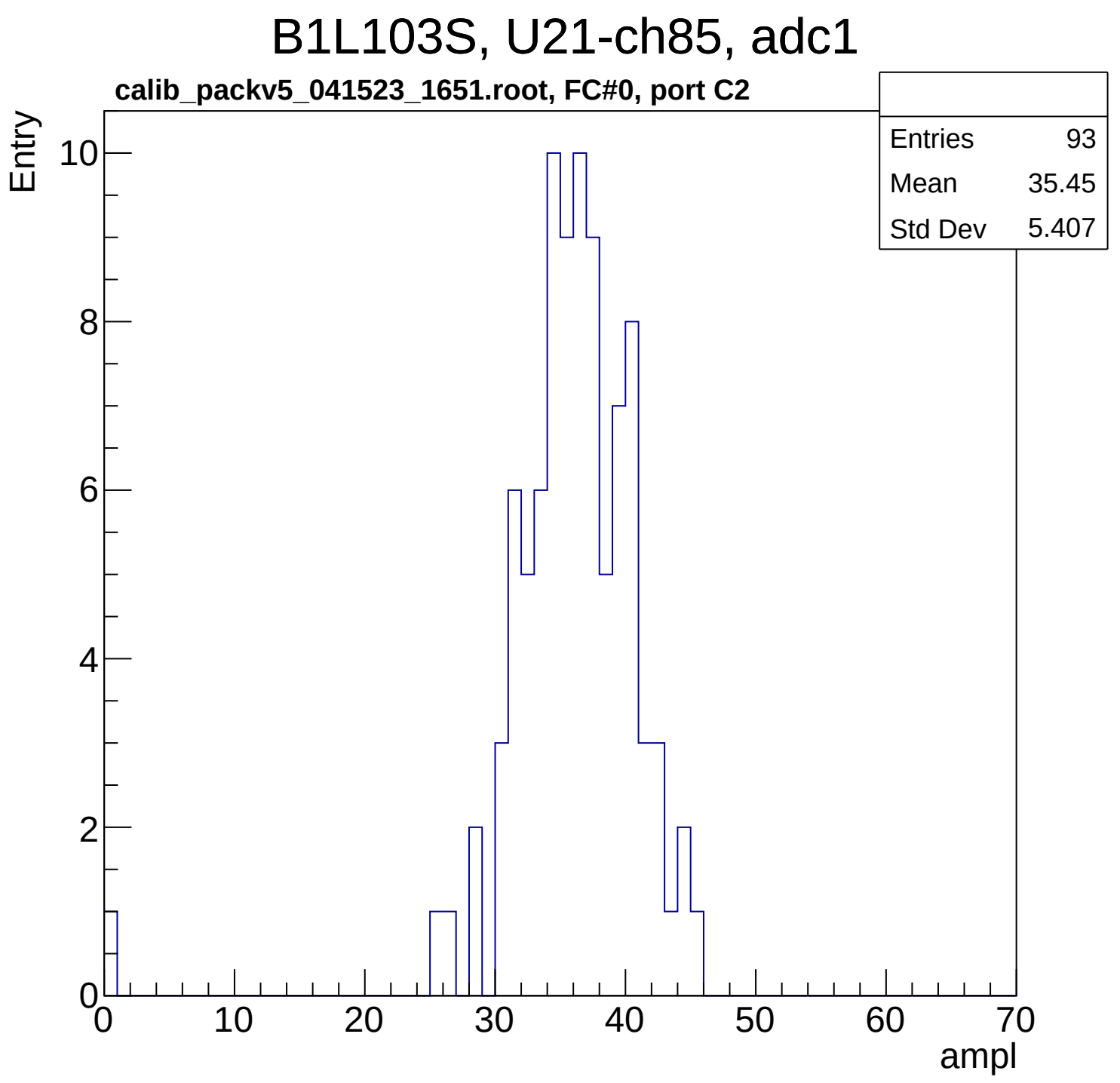
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch84, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 57.35
Std Dev 14.45
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U21-ch84, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 7.05
Std Dev 18.81
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch85, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 22.24
Std Dev 11.85
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch85, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 35.45
Std Dev 5.407
Entry
ampl
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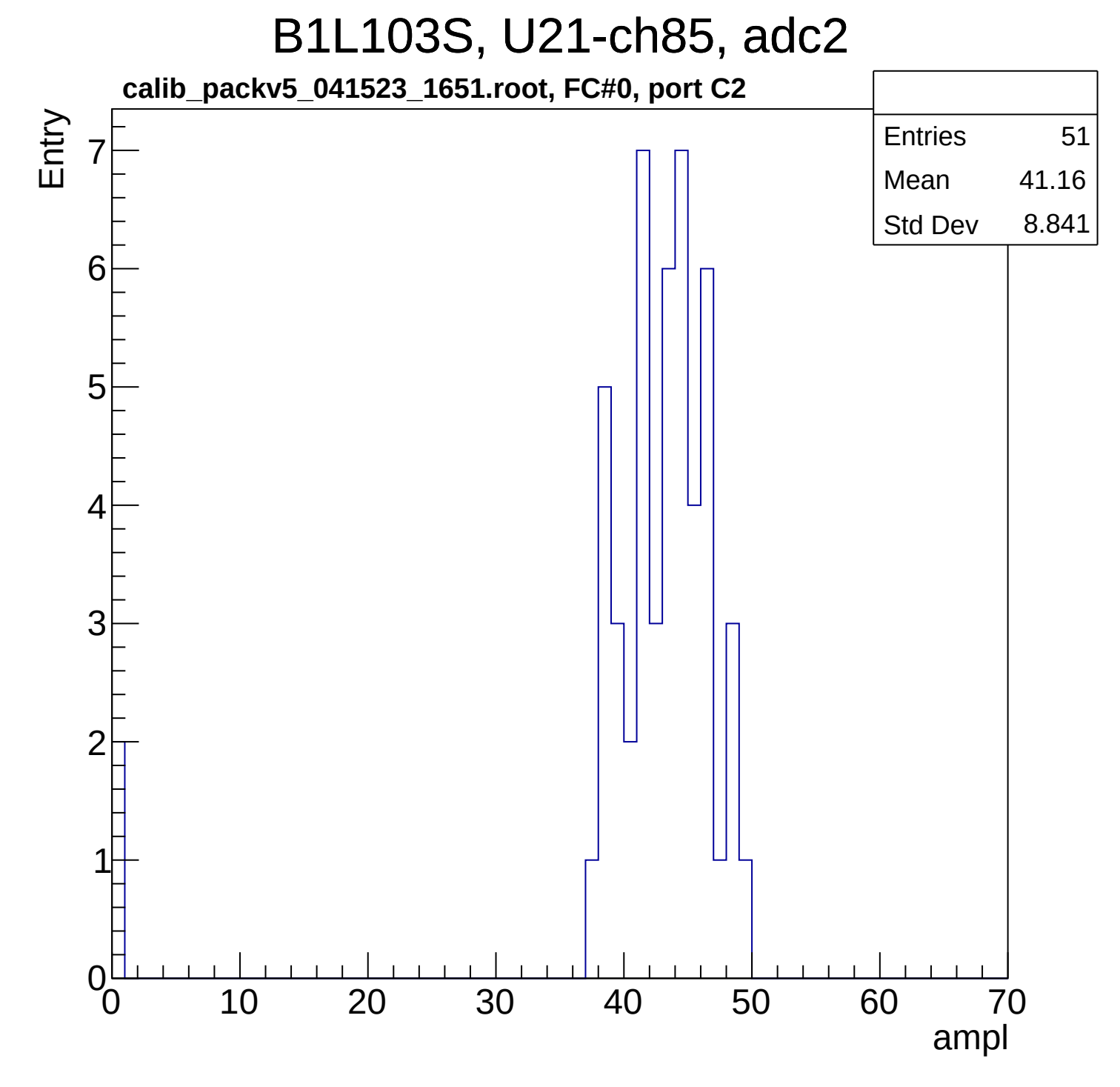
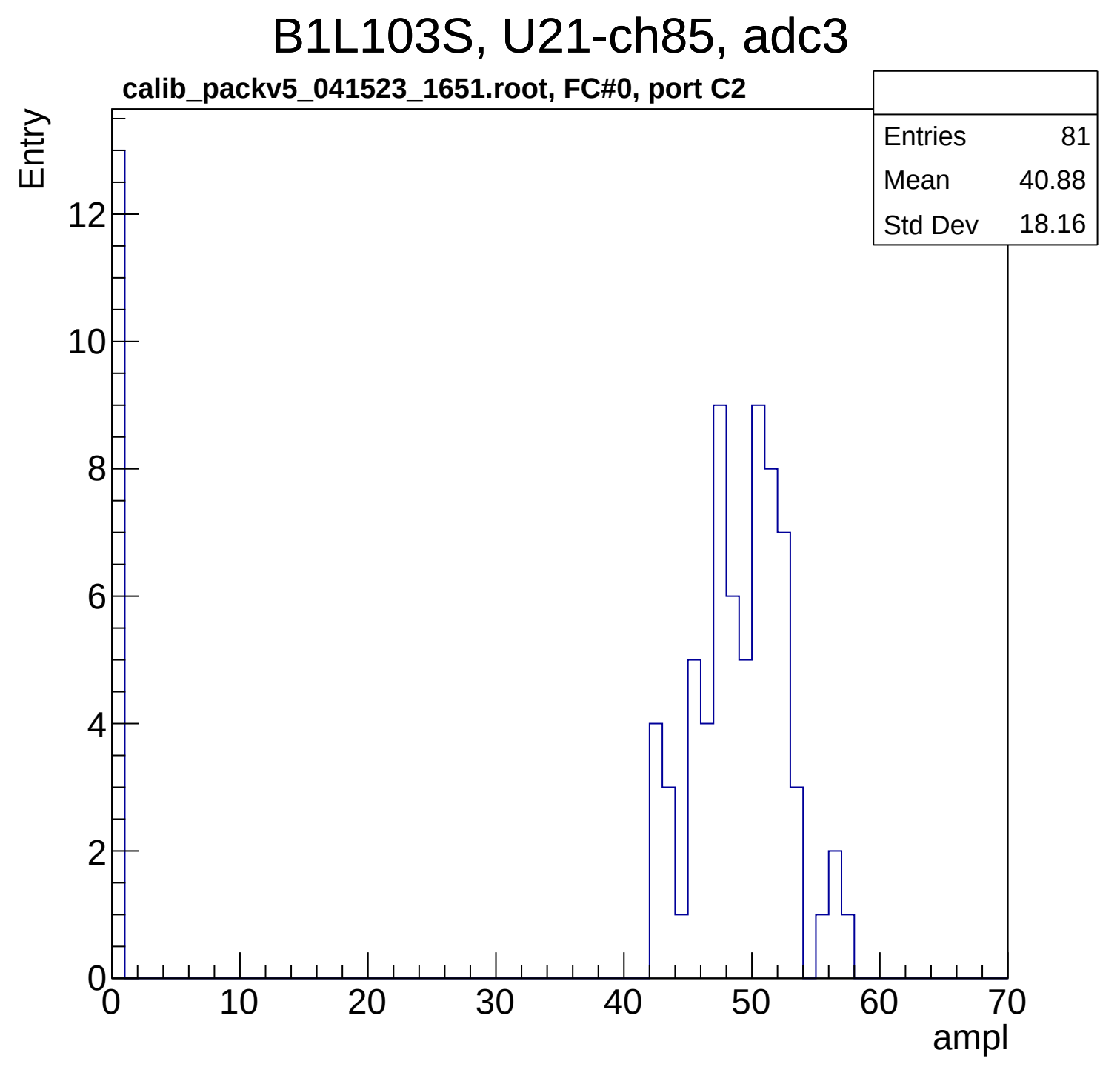
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U21-ch85, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 41.16
Std Dev 8.841
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U21-ch85, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 40.88
Std Dev 18.16
Entry
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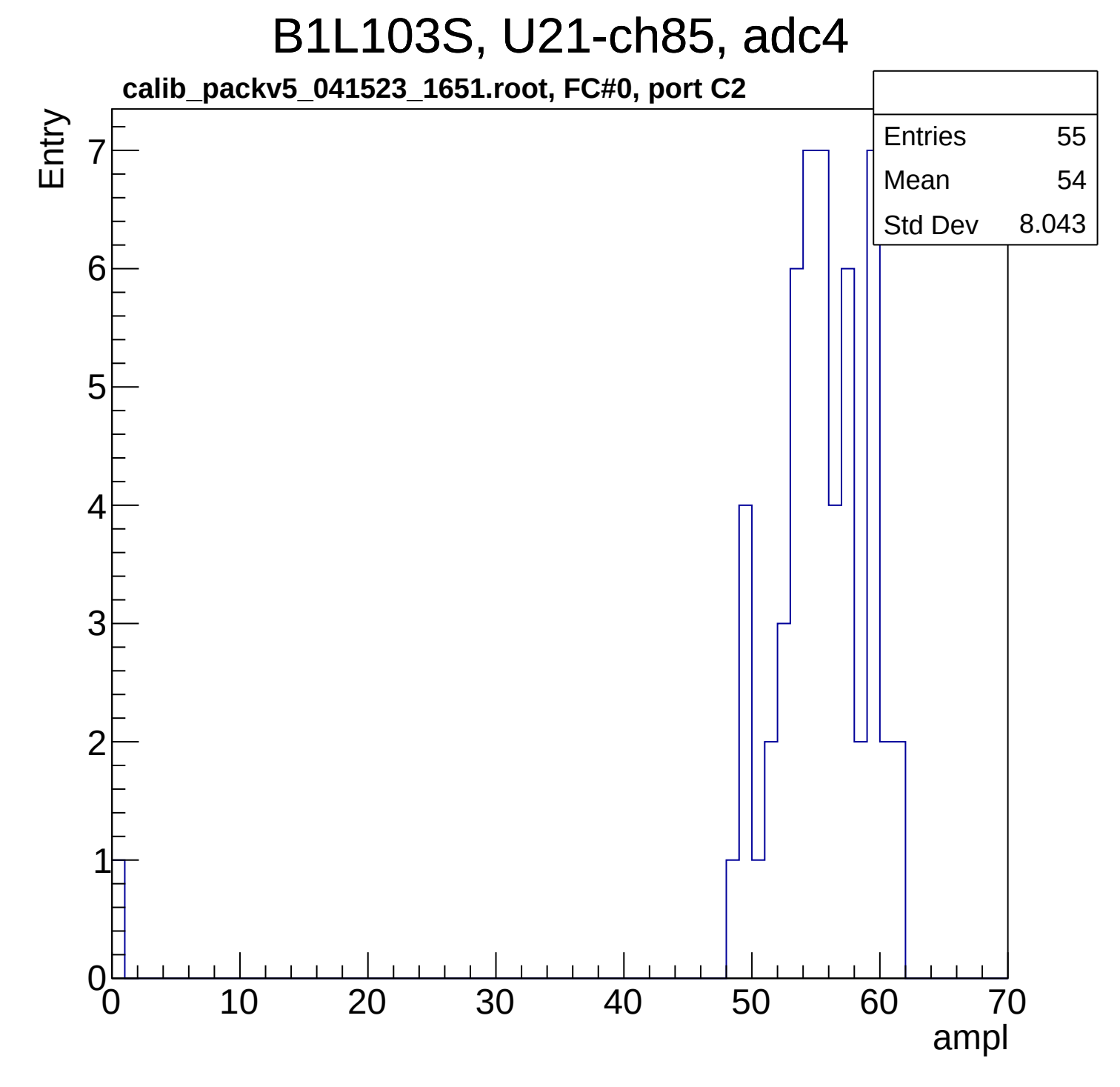
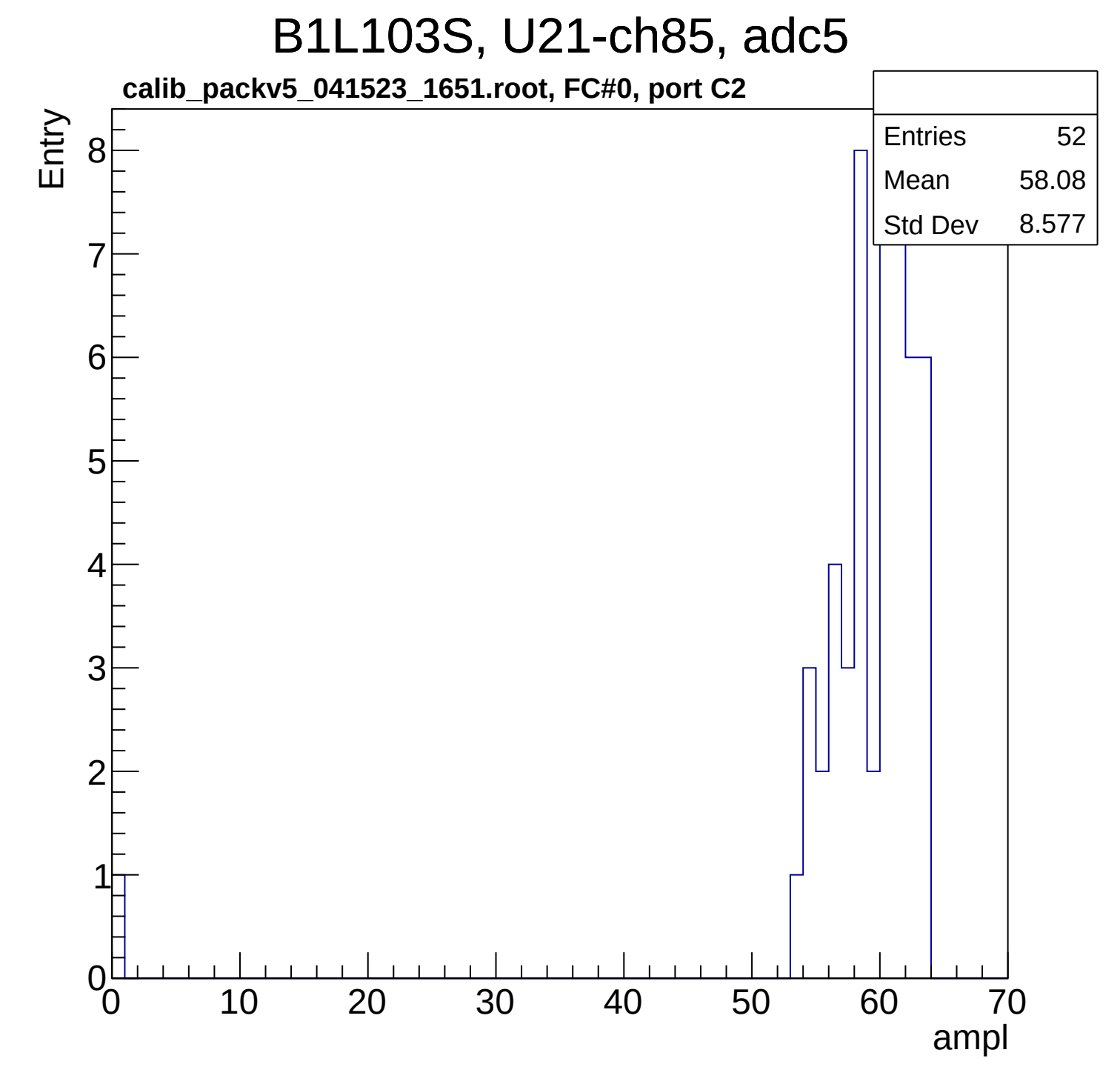
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch85, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 54
Std Dev 8.043
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U21-ch85, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 58.08
Std Dev 8.577
Entry
ampl
0
1
2
3
4
5
6
7
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0
10
20
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40
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60
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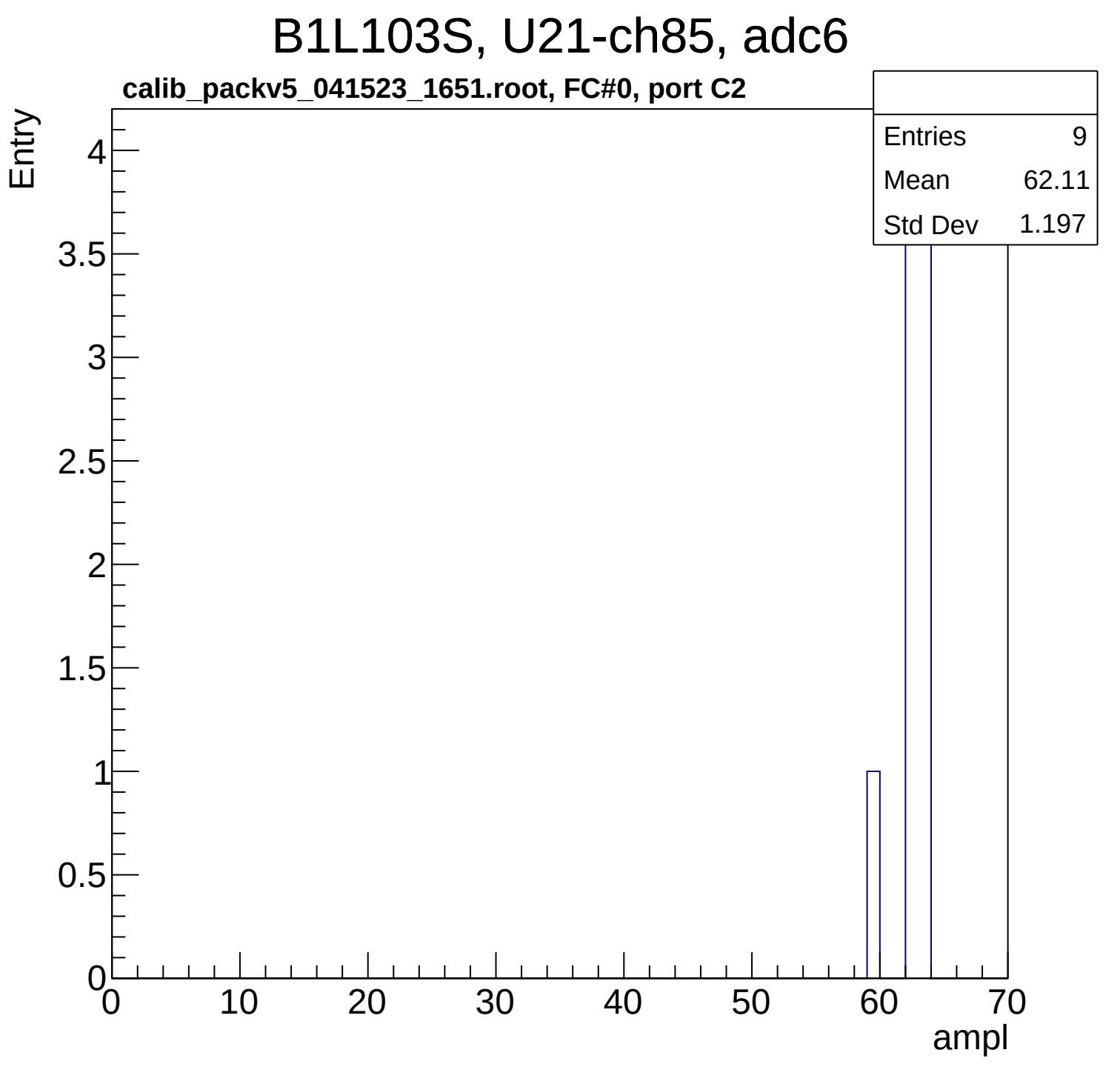
B1L103S, U21-ch85, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 62.11
Std Dev 1.197
Entry
ampl
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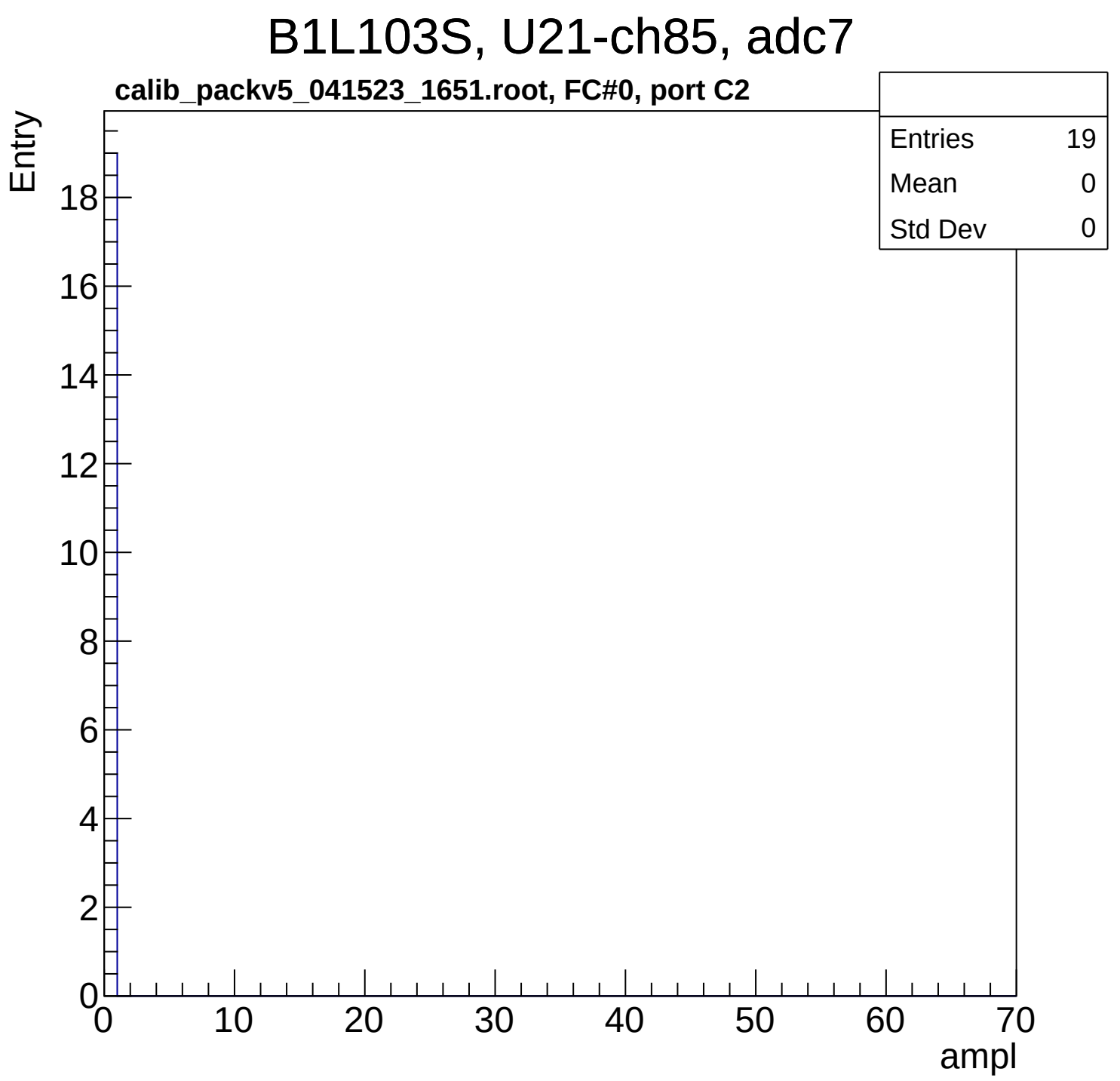
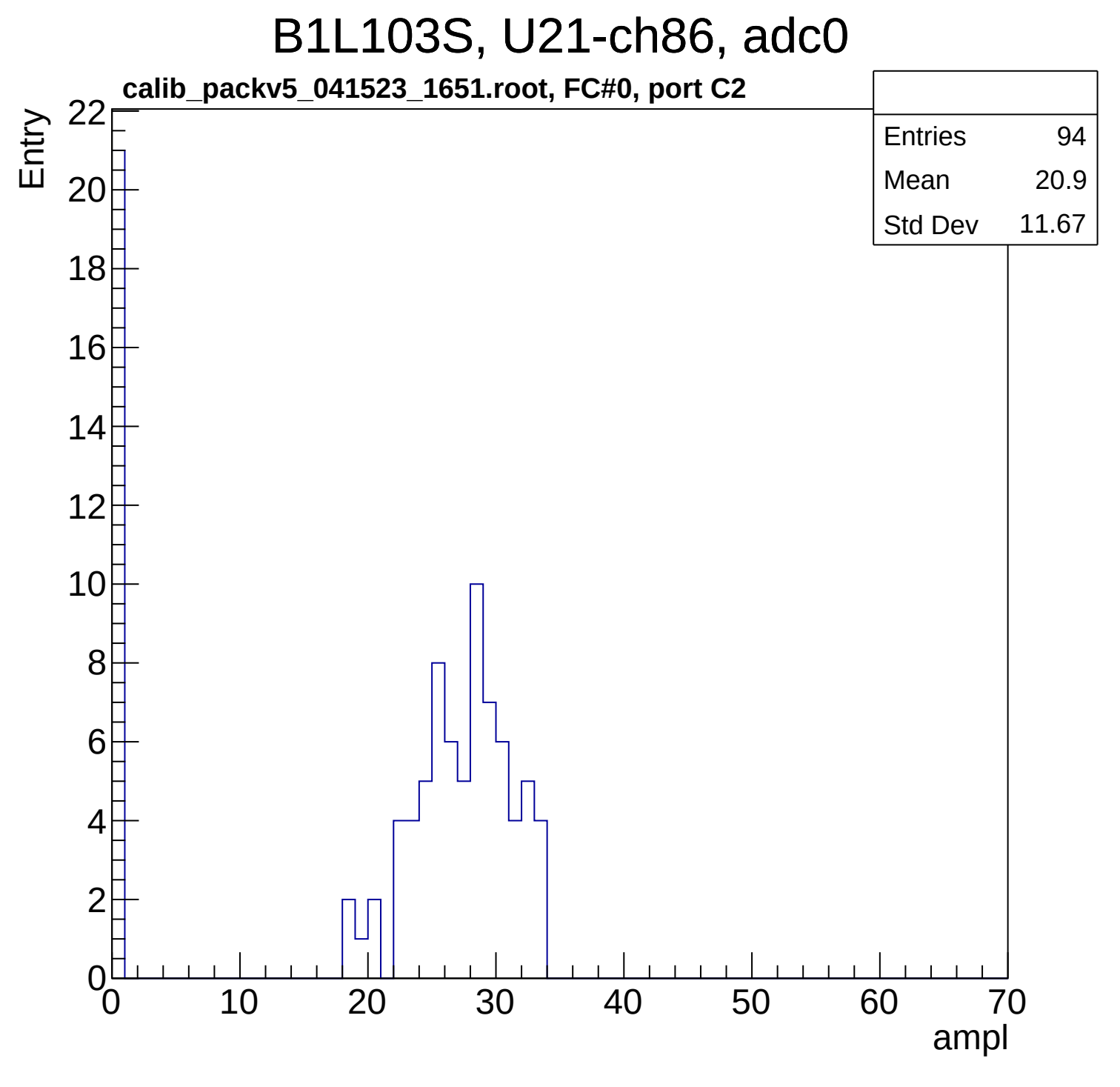
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U21-ch85, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch86, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 20.9
Std Dev 11.67
Entry
ampl
0
2
4
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8
10
12
14
16
18
20
22
0
10
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40
50
60
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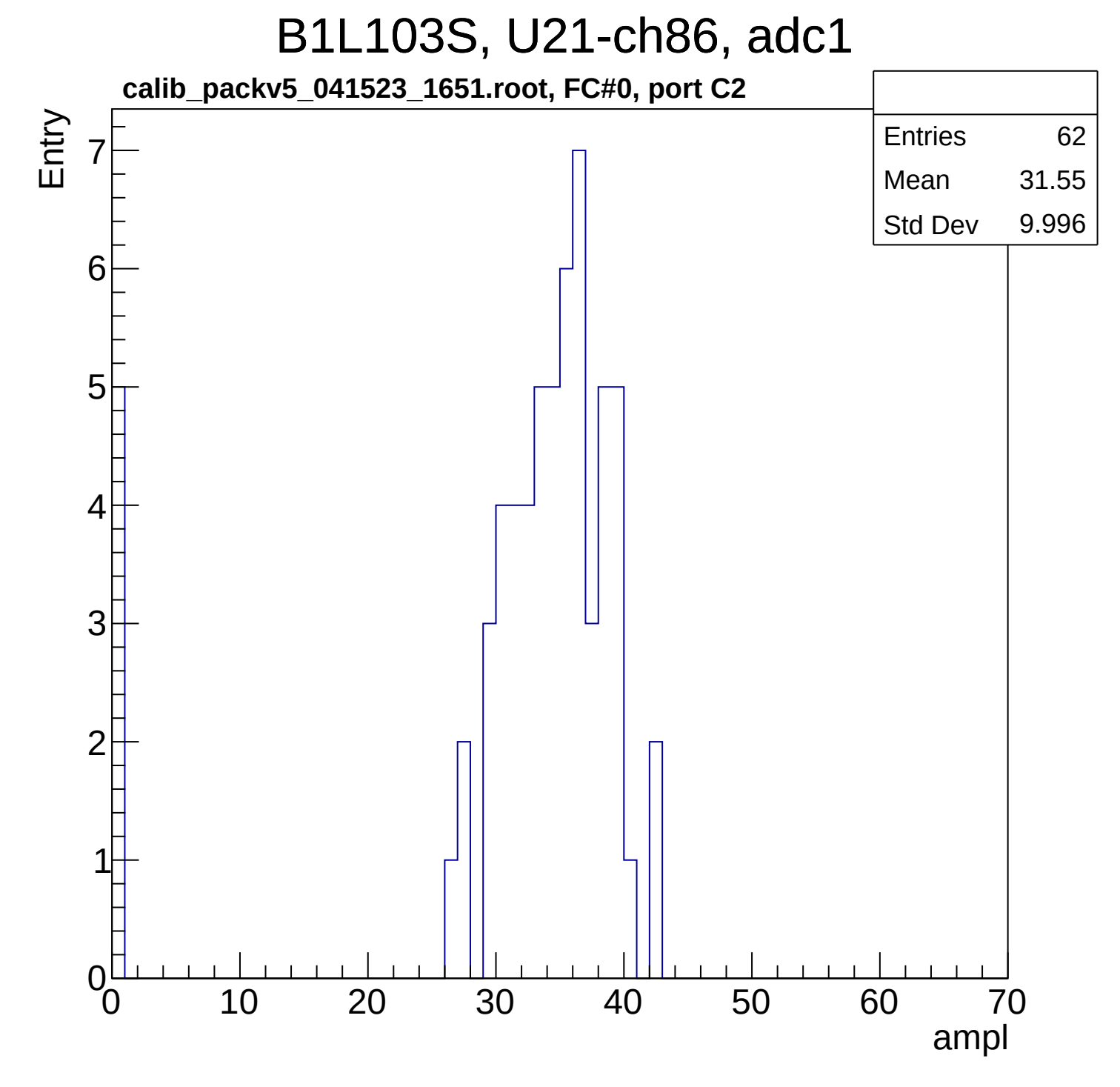
B1L103S, U21-ch86, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 31.55
Std Dev 9.996
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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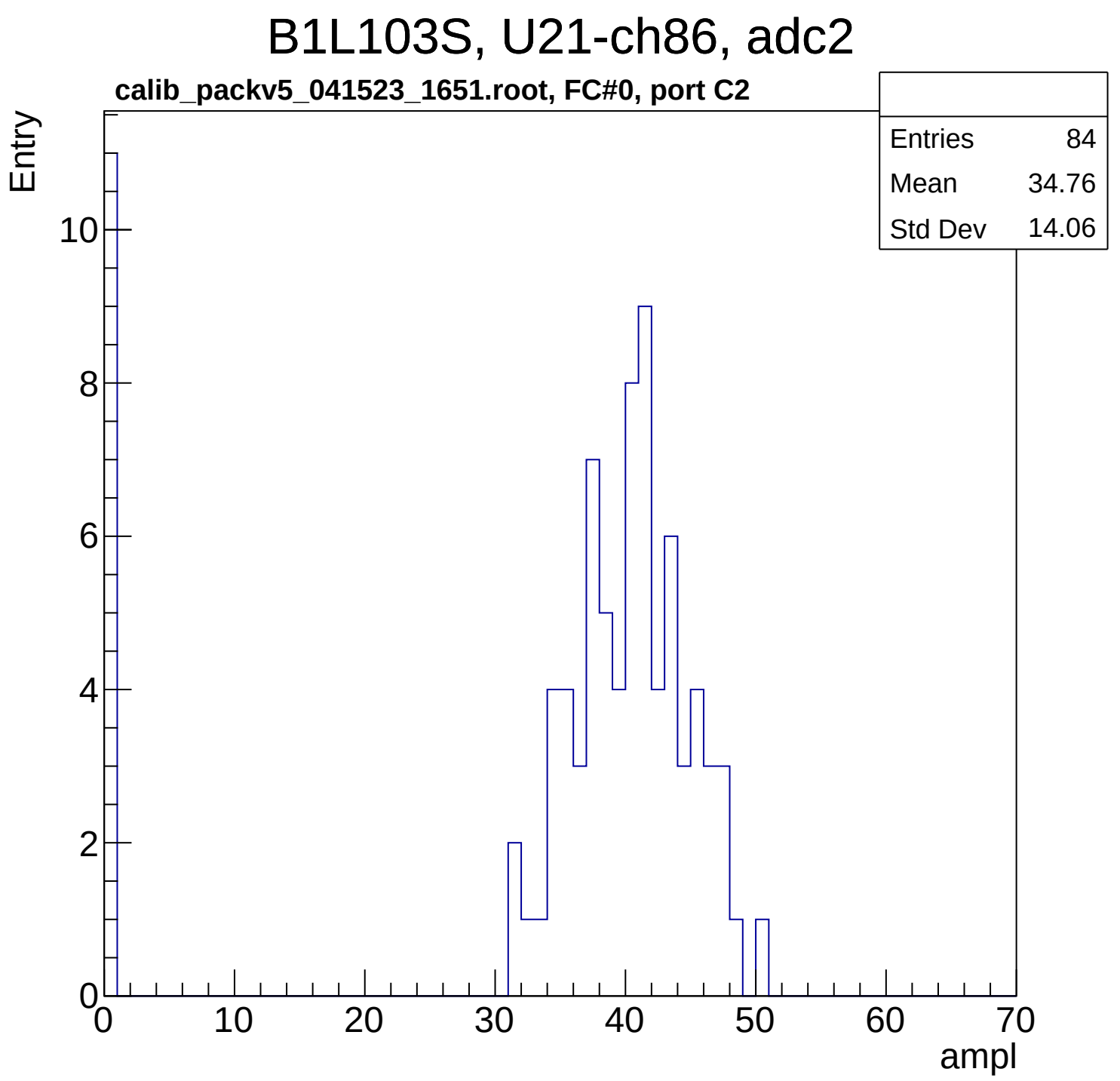
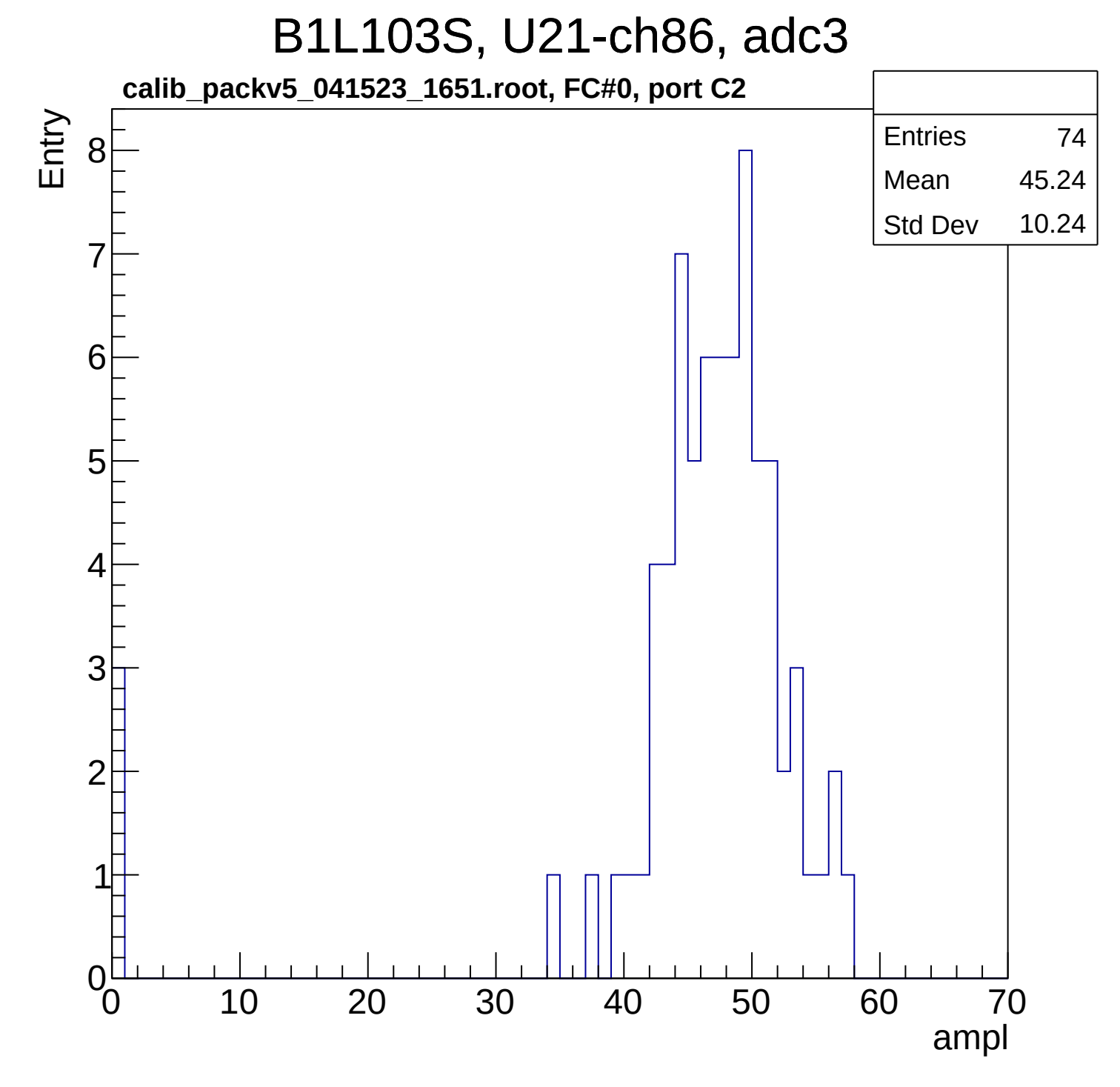

B1L103S, U21-ch86, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 34.76
Std Dev 14.06
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch86, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 45.24
Std Dev 10.24
Entry
ampl
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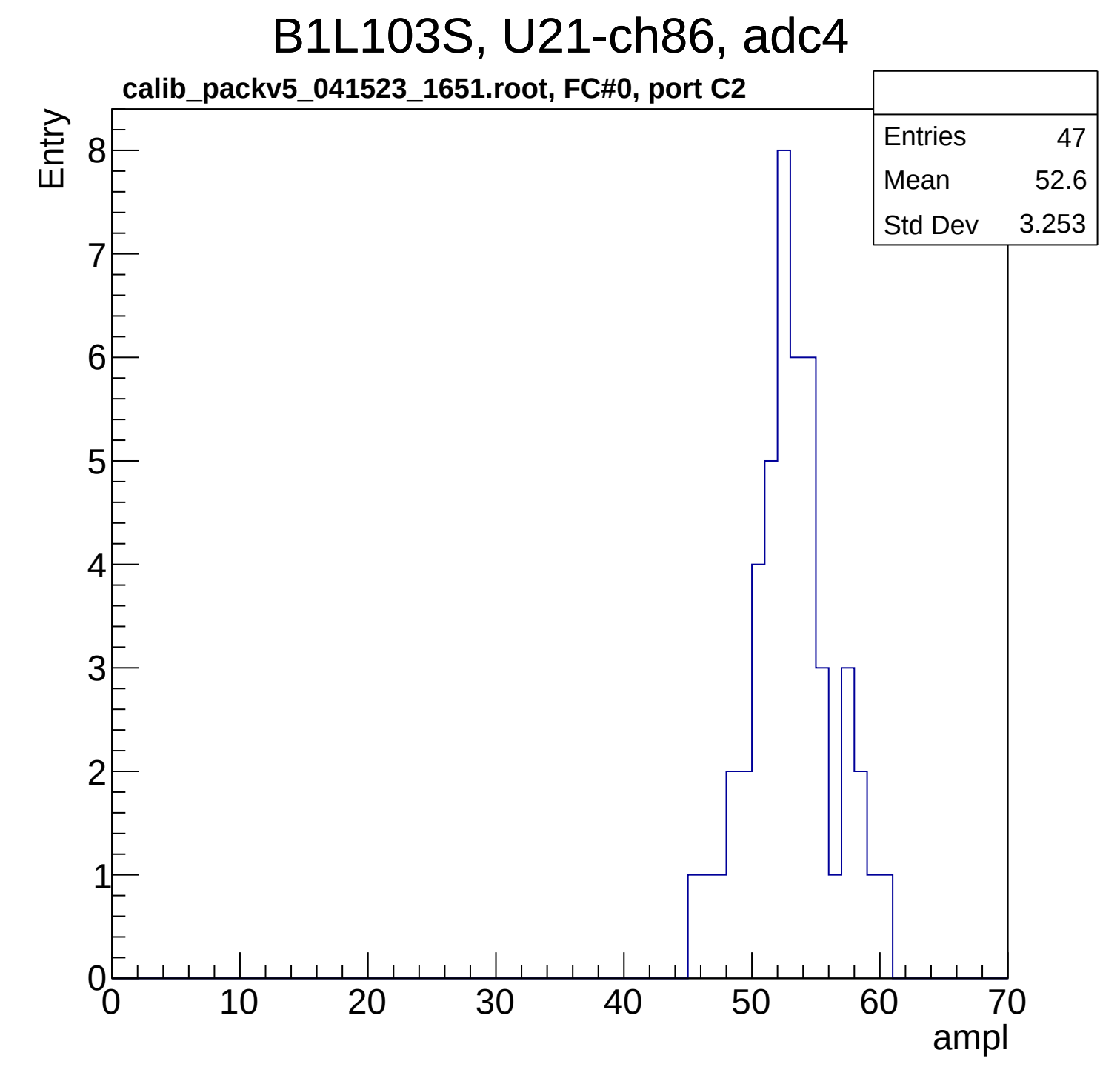
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch86, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 52.6
Std Dev 3.253
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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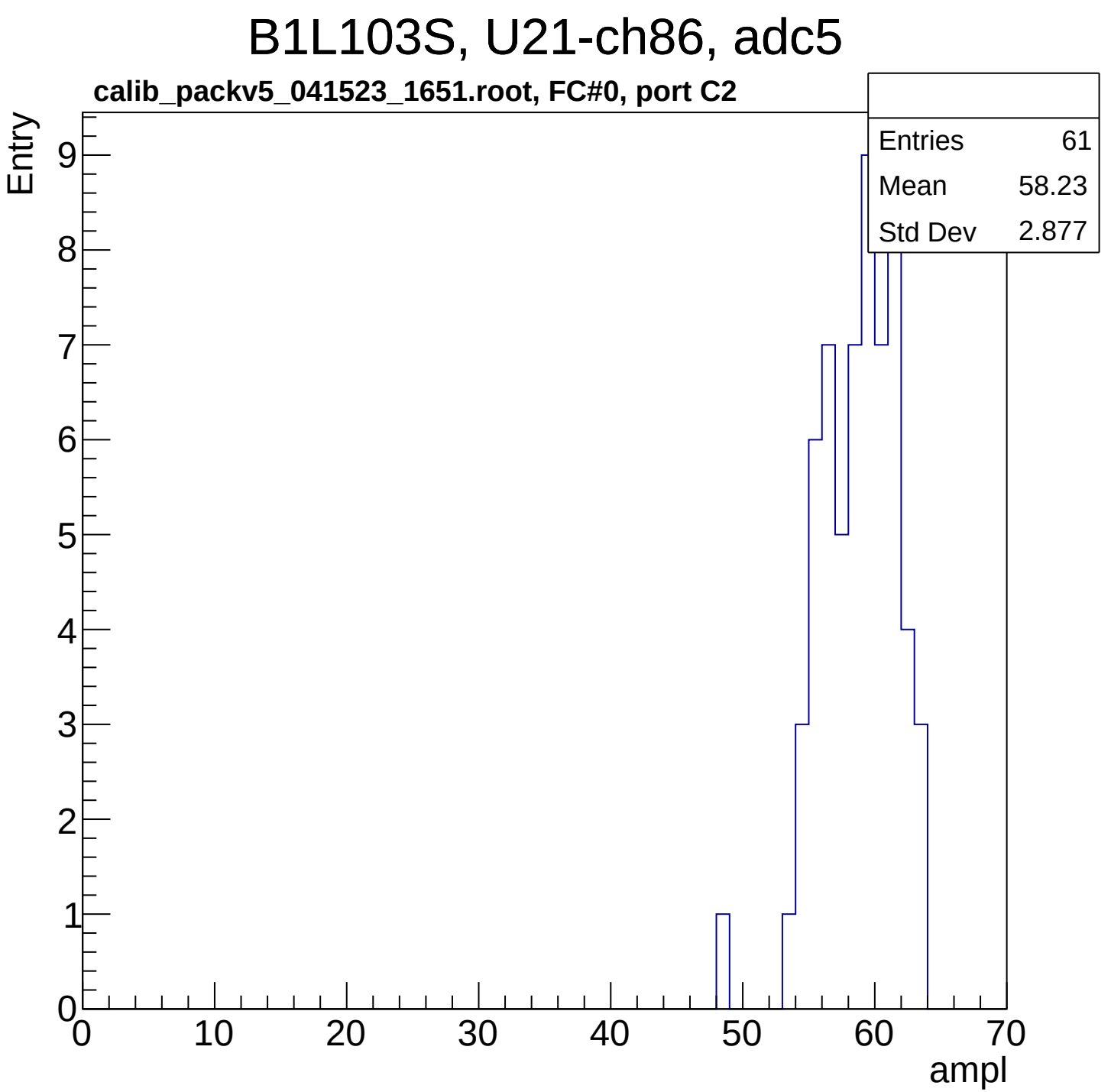
B1L103S, U21-ch86, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 58.23
Std Dev 2.877
Entry
ampl
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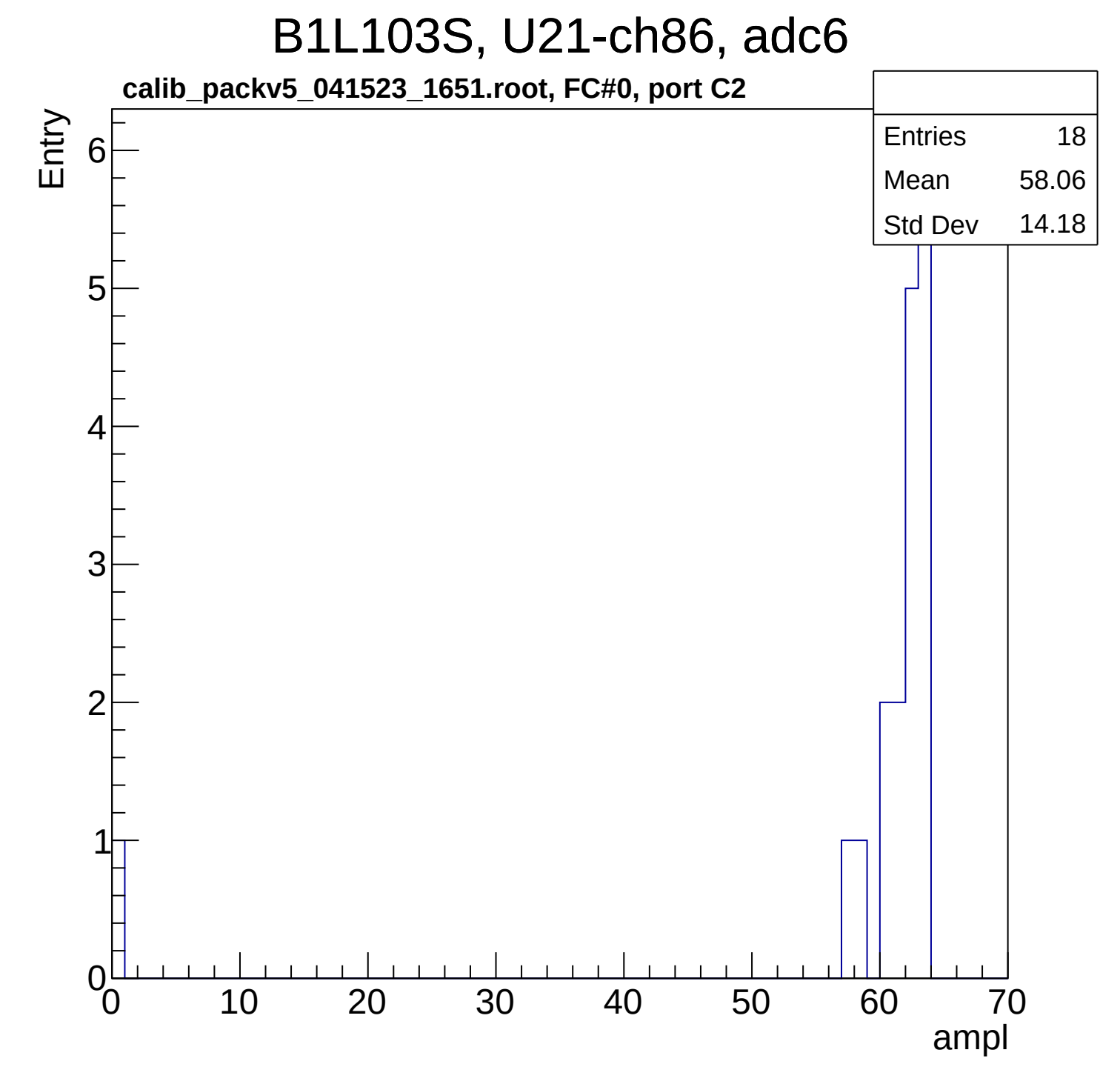
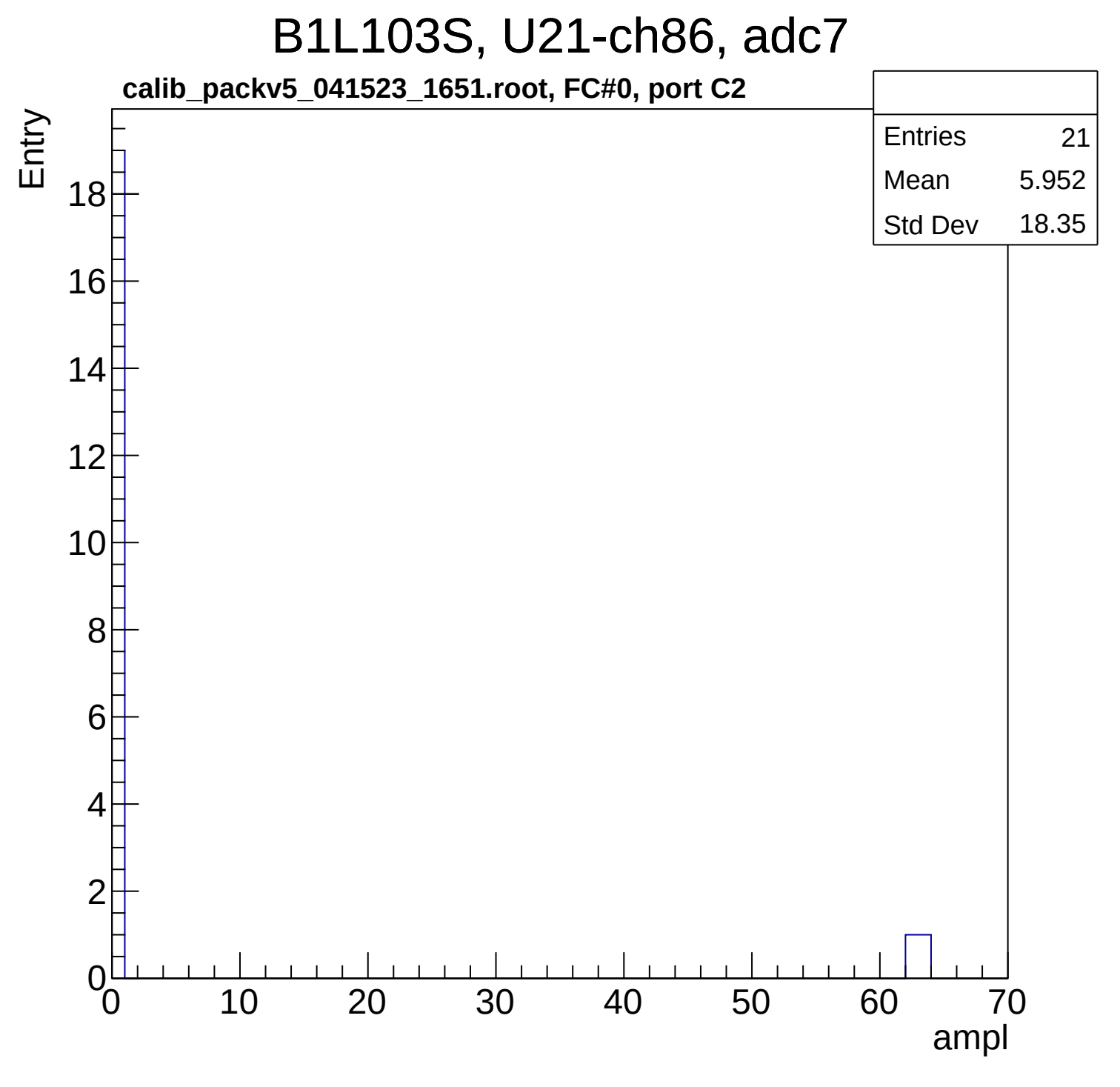
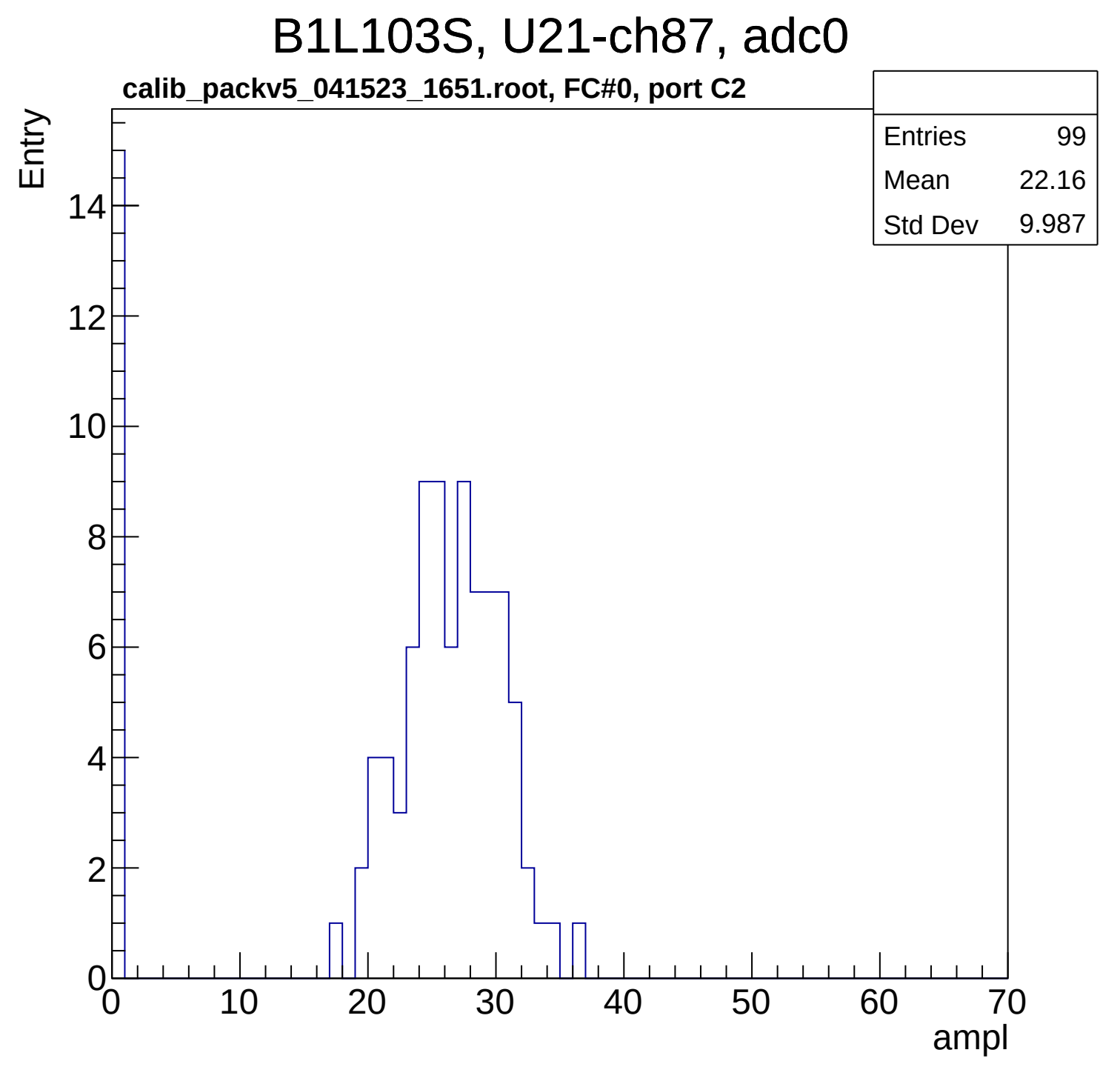
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch86, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 58.06
Std Dev 14.18
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U21-ch86, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.952
Std Dev 18.35
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch87, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 22.16
Std Dev 9.987
Entry
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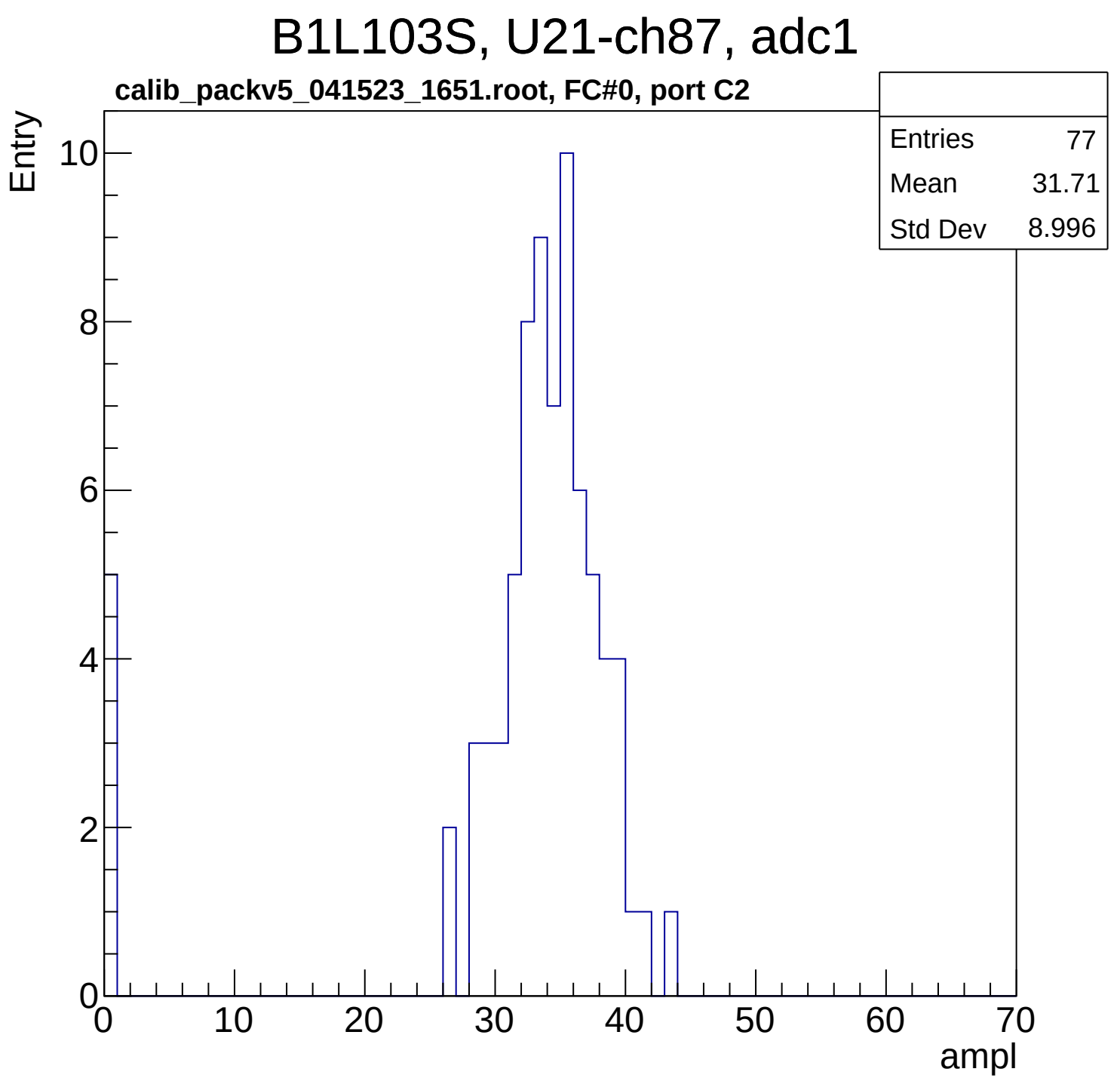
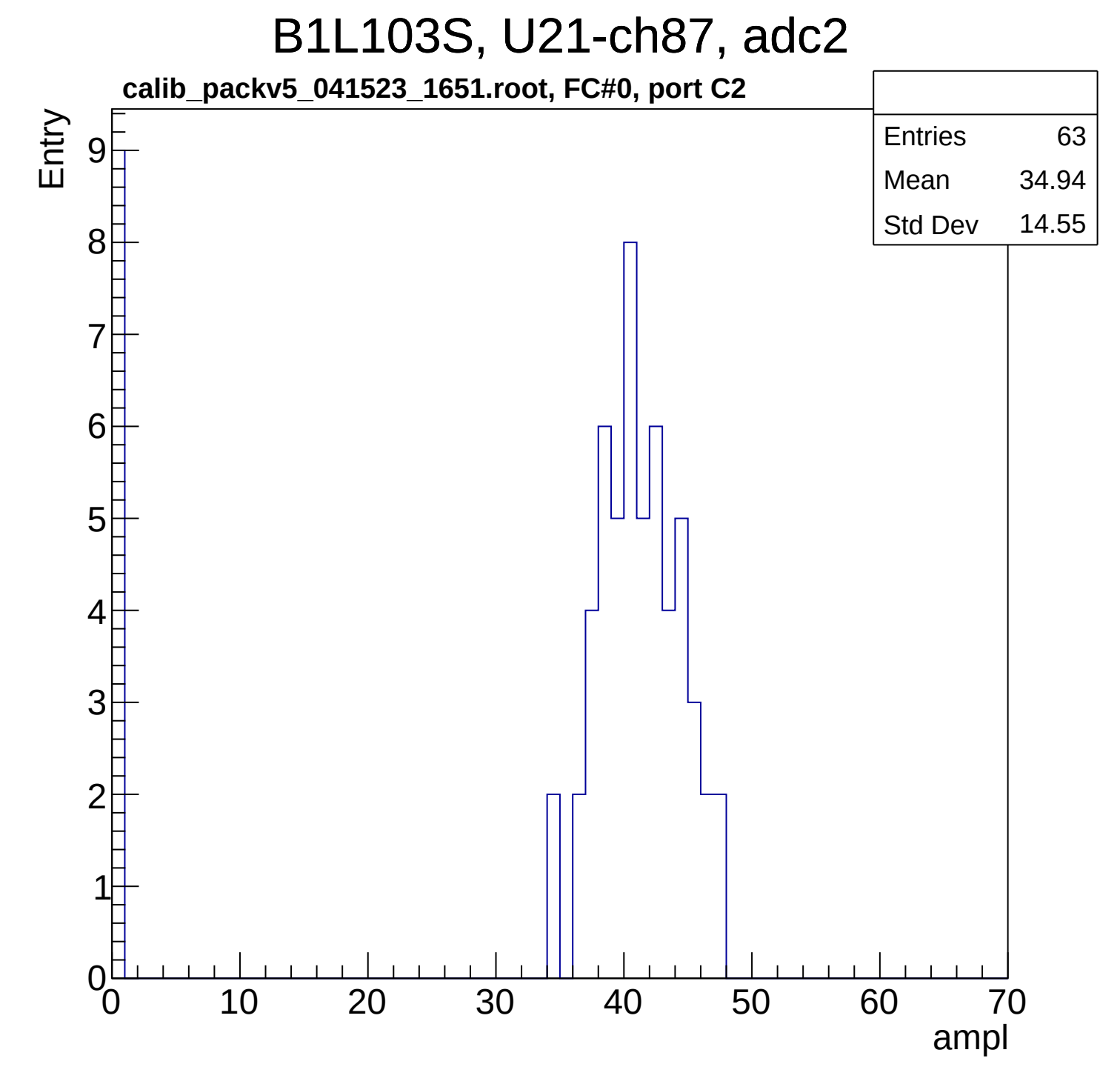
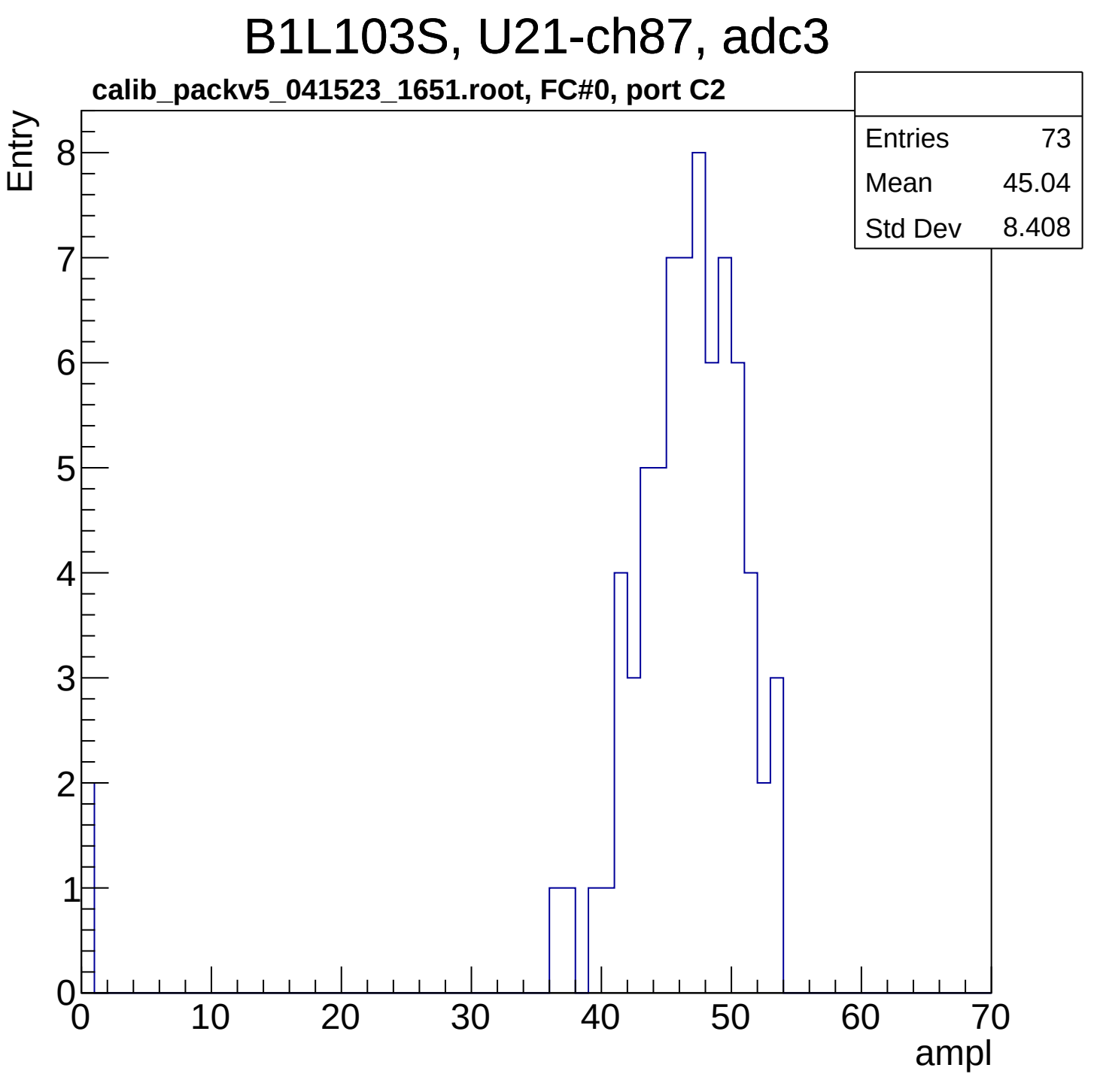
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch87, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 31.71
Std Dev 8.996
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch87, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 34.94
Std Dev 14.55
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch87, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 45.04
Std Dev 8.408
Entry
ampl
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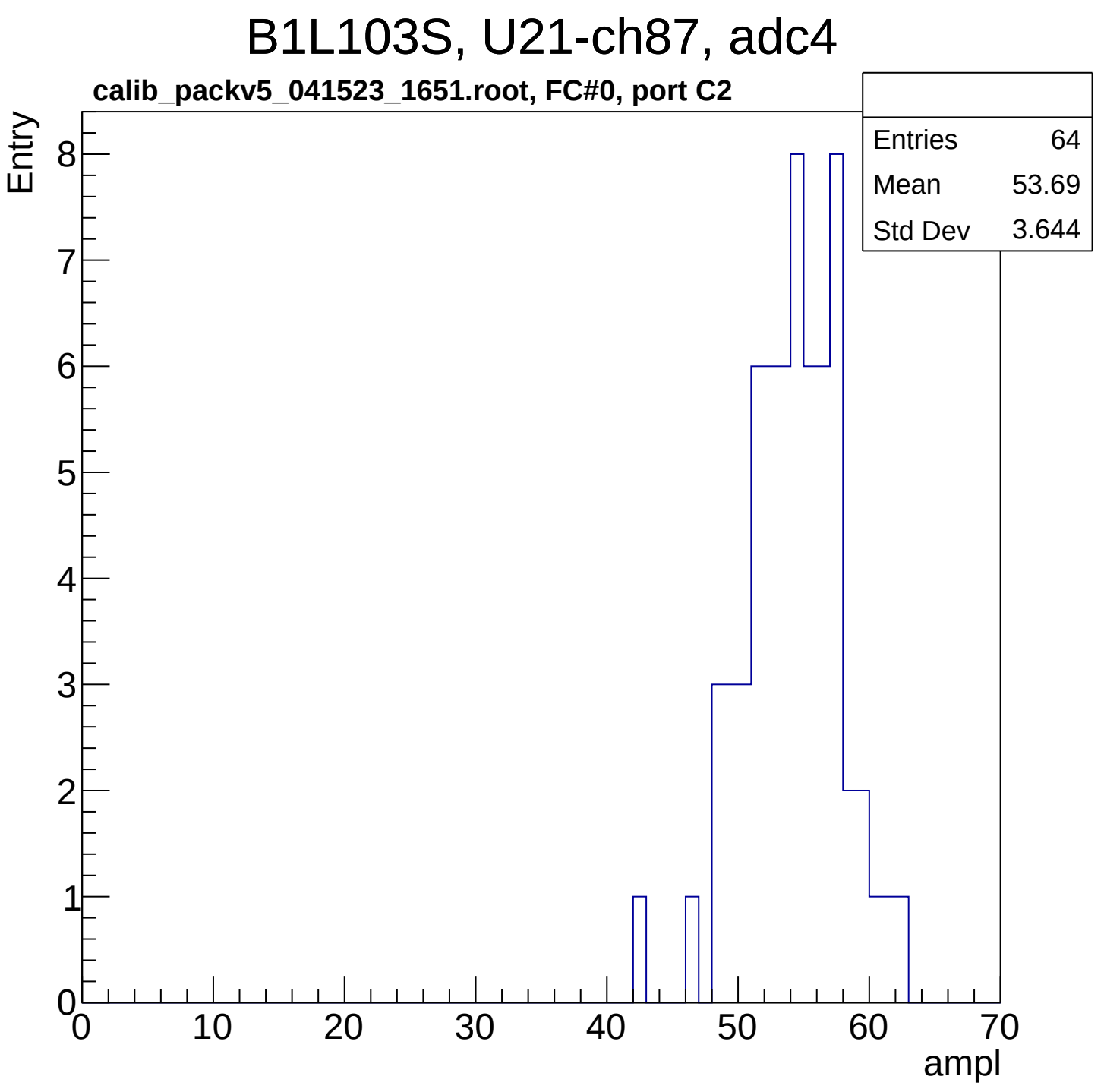
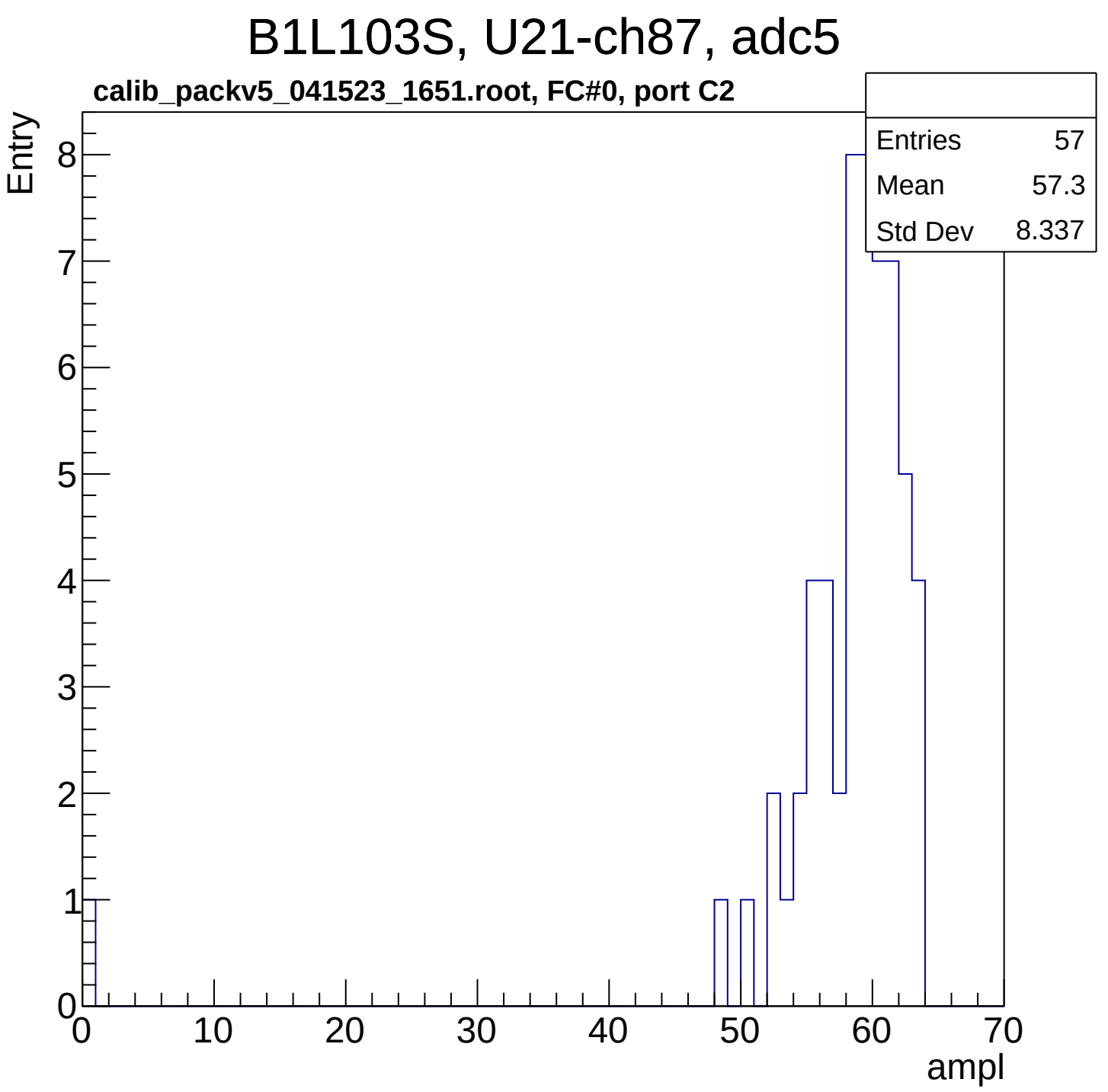
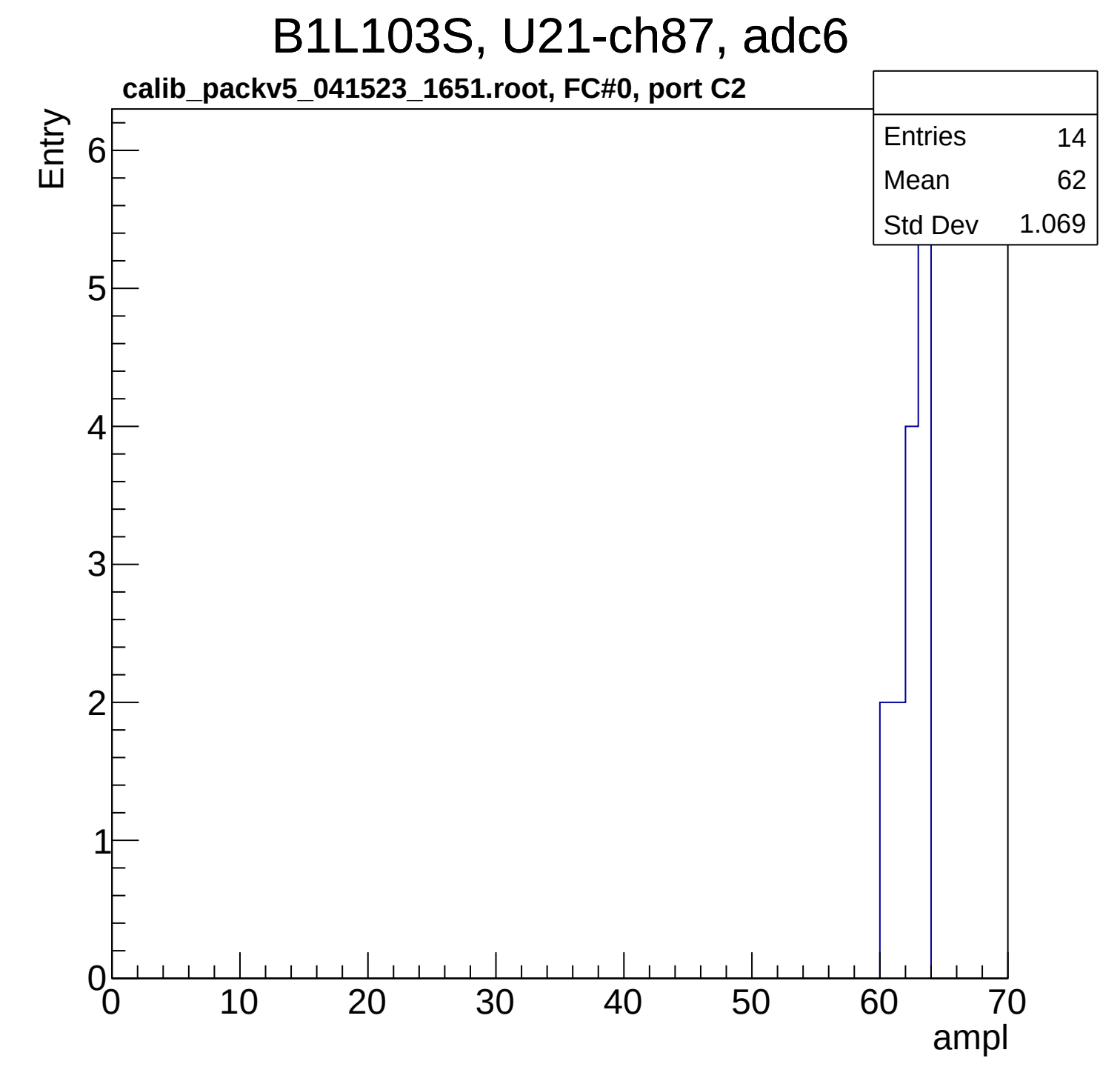
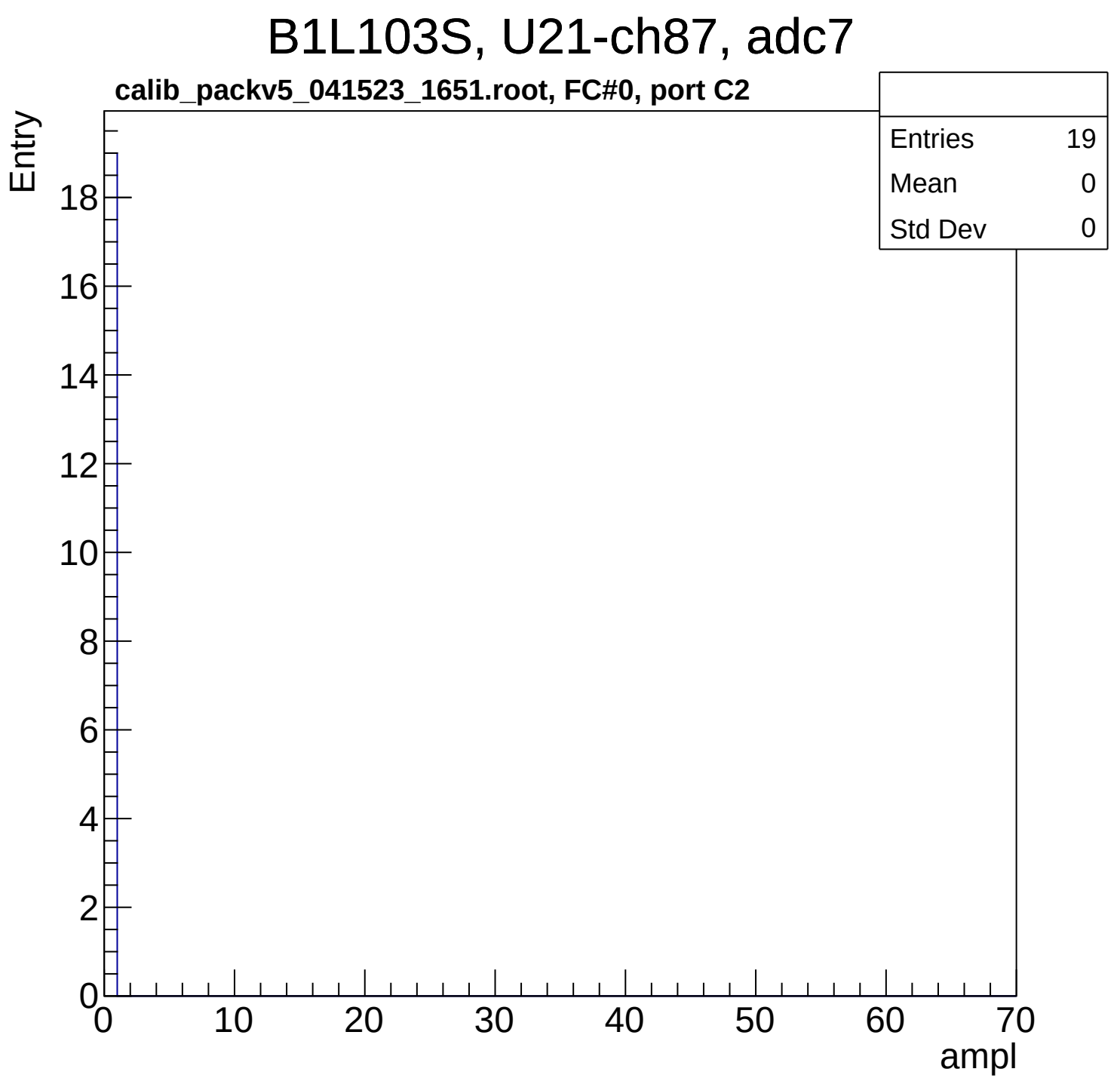
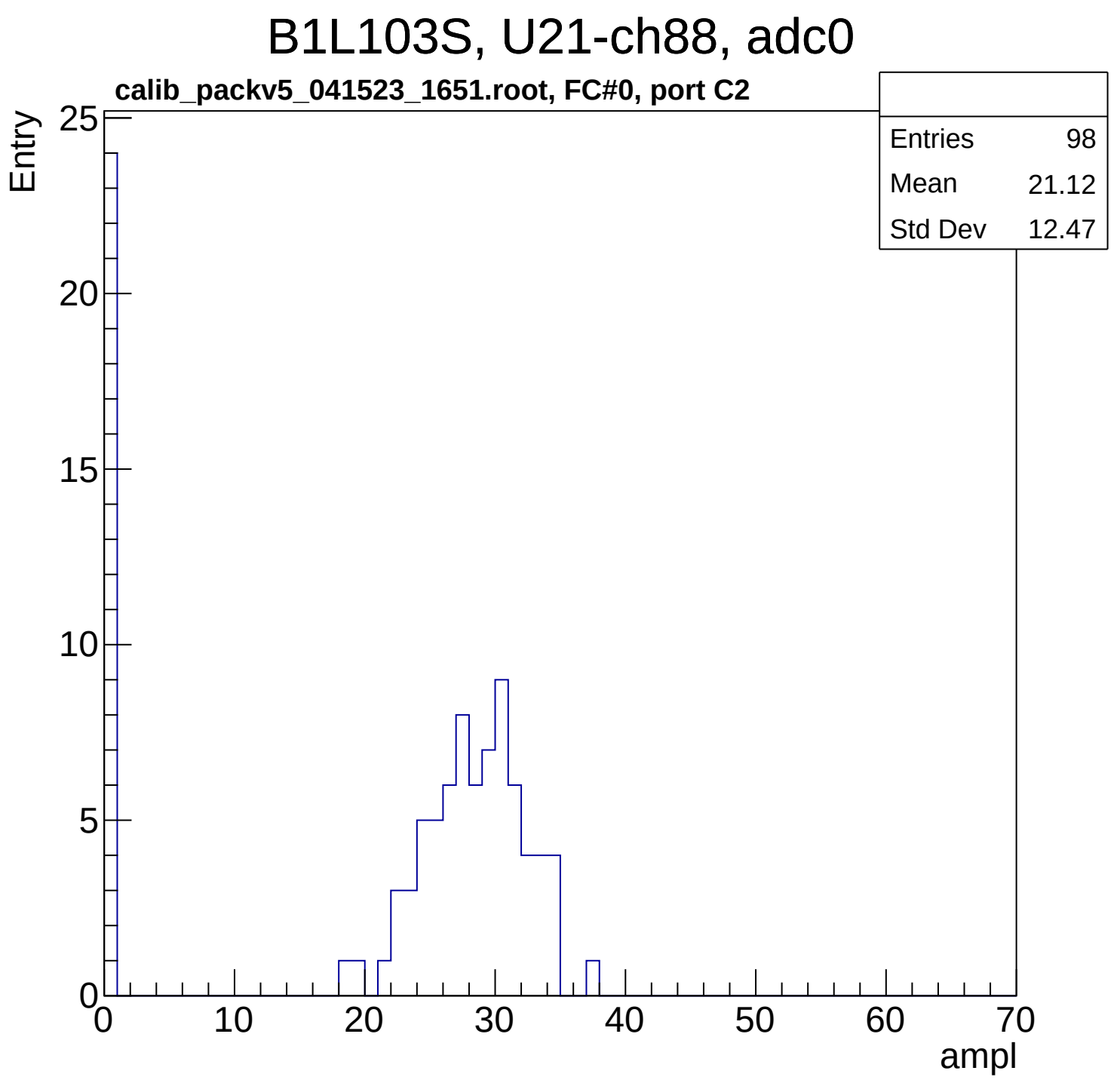
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

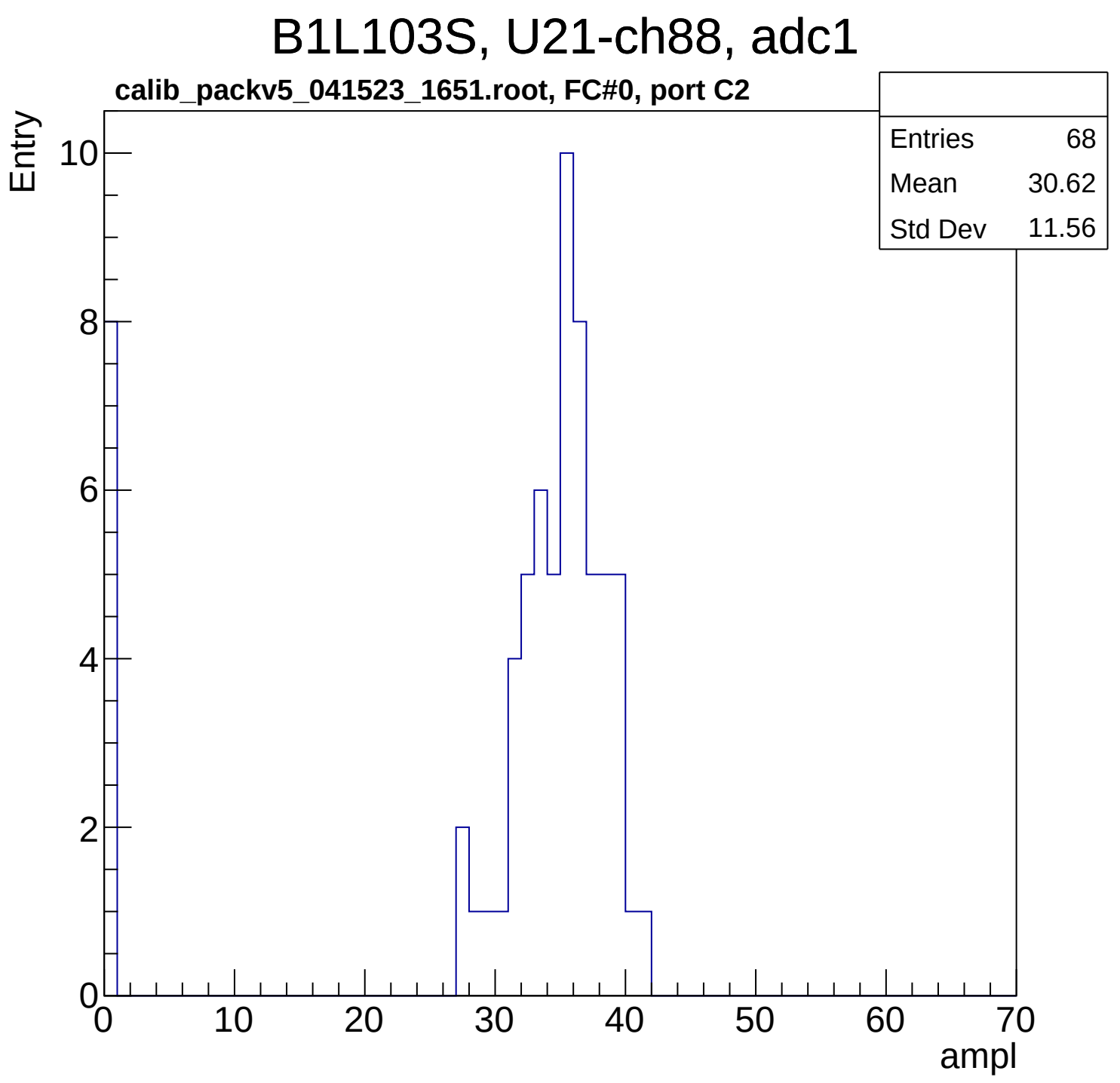

B1L103S, U21-ch87, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 53.69
Std Dev 3.644
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

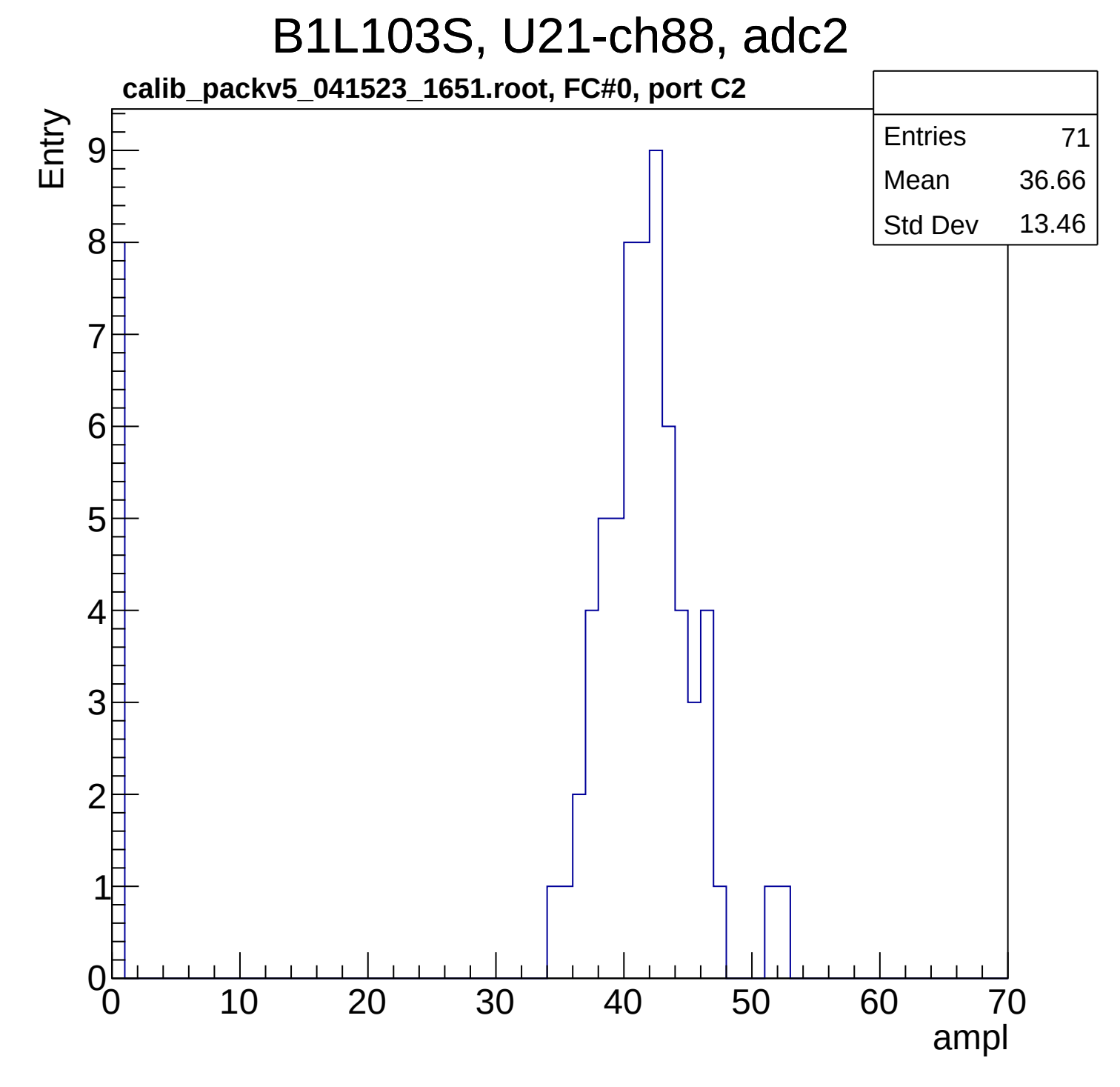

B1L103S, U21-ch87, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 57.3
Std Dev 8.337
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch87, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 62
Std Dev 1.069
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch87, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch88, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 98
Mean 21.12
Std Dev 12.47
Entry
ampl
0
5
10
15
20
25
0
10
20
30
40
50
60
70


B1L103S, U21-ch88, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 30.62
Std Dev 11.56
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U21-ch88, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 36.66
Std Dev 13.46
Entry
ampl
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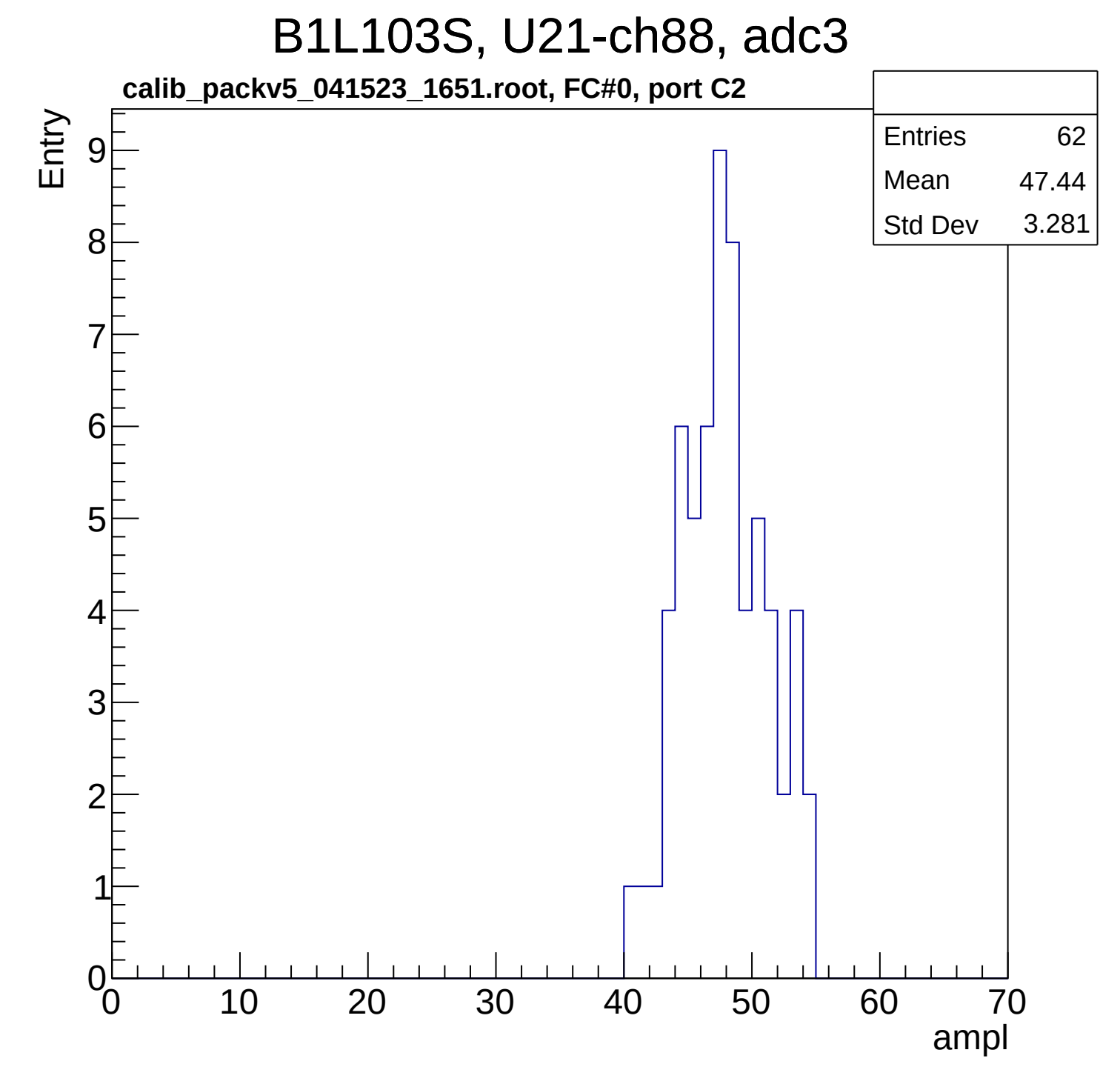
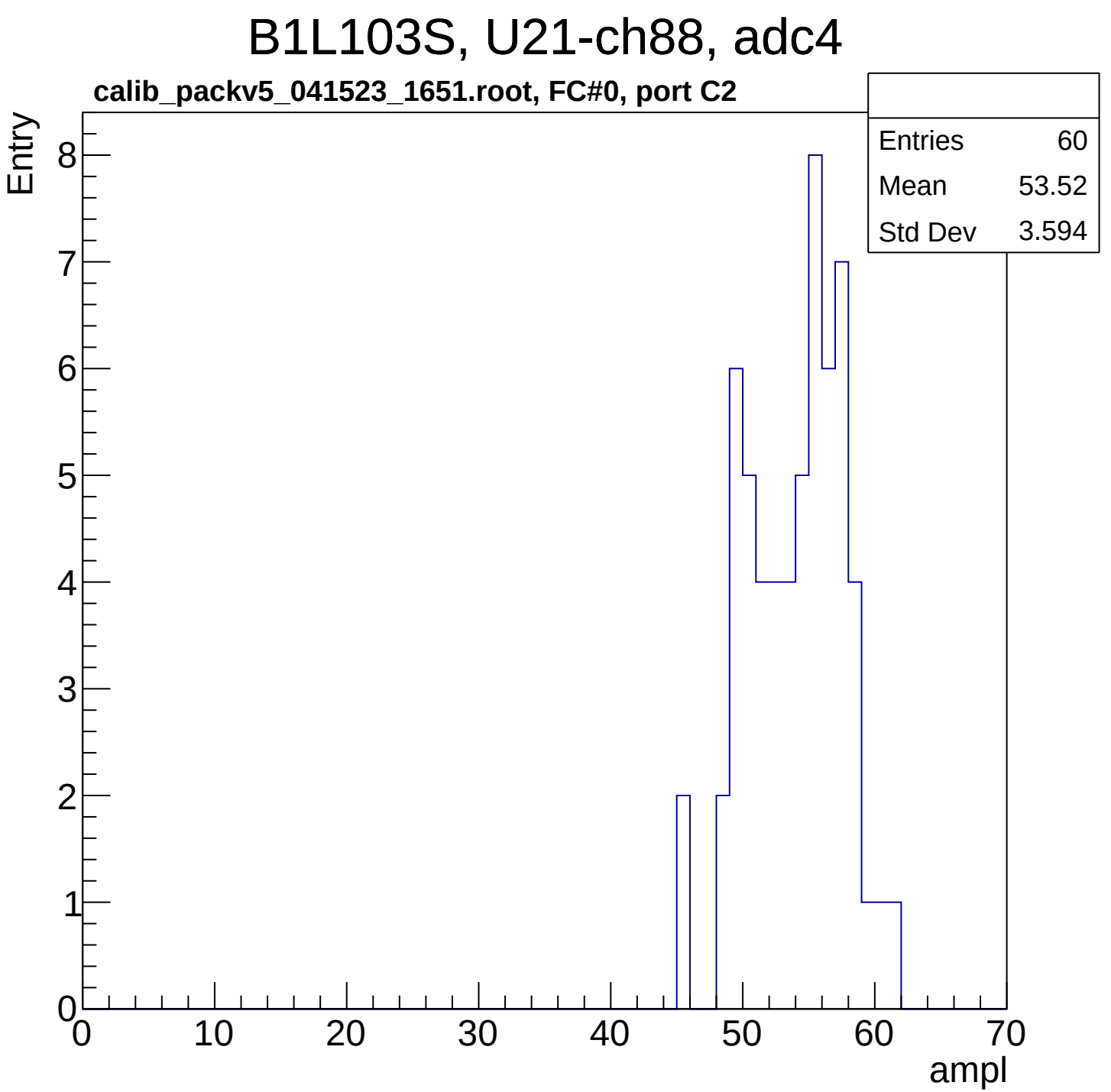
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch88, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 47.44
Std Dev 3.281
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch88, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 53.52
Std Dev 3.594
Entry
ampl
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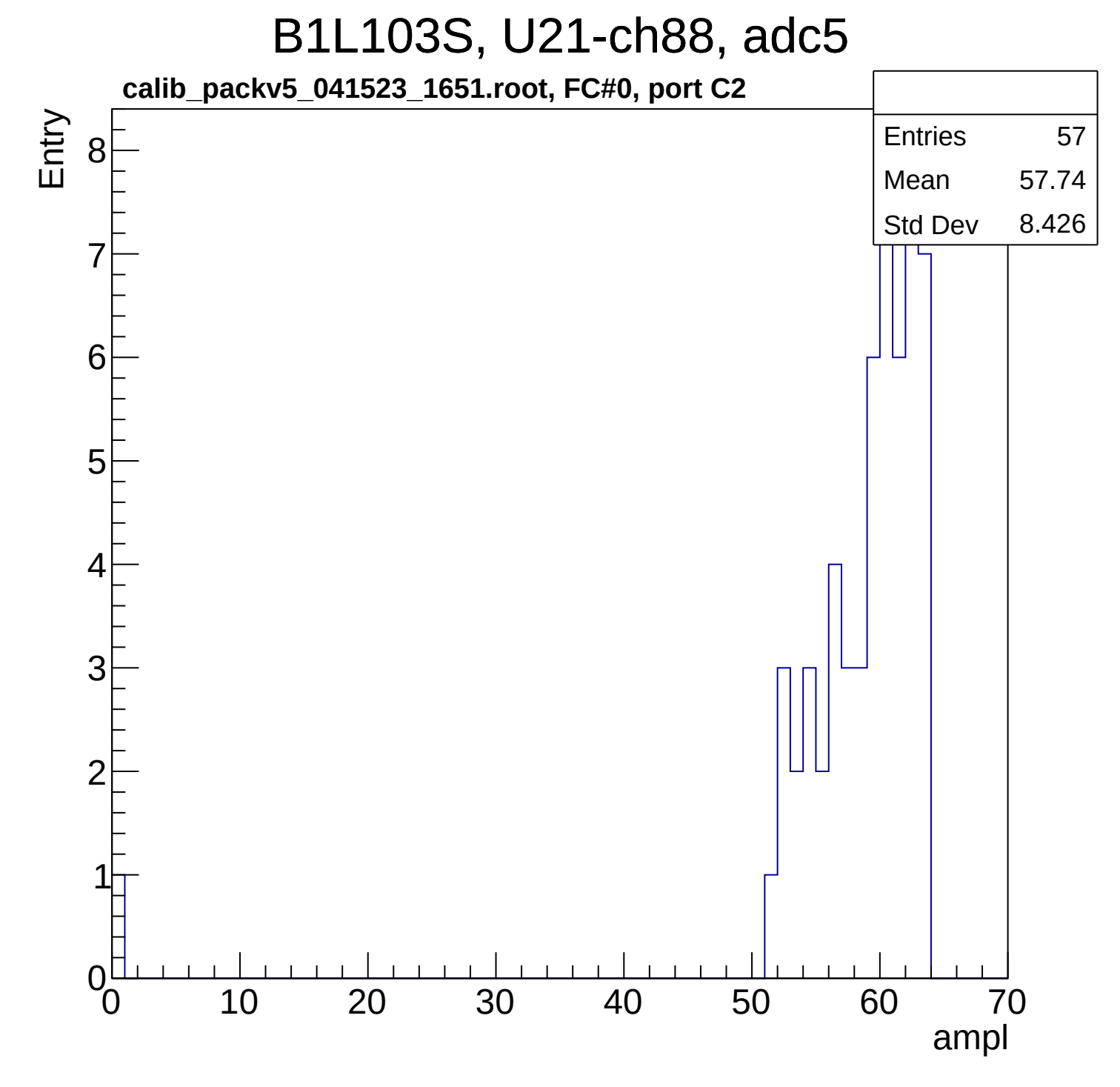
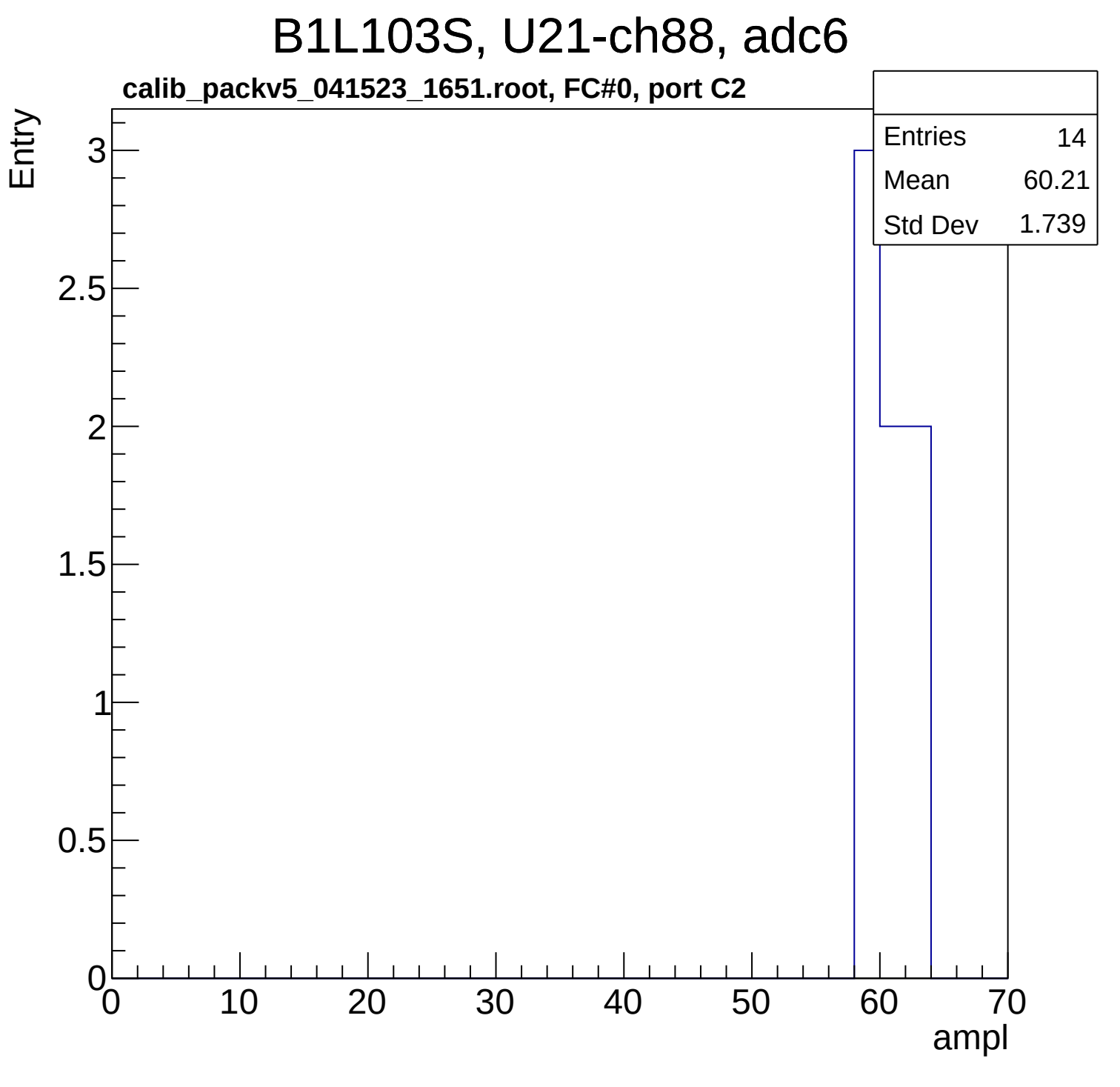
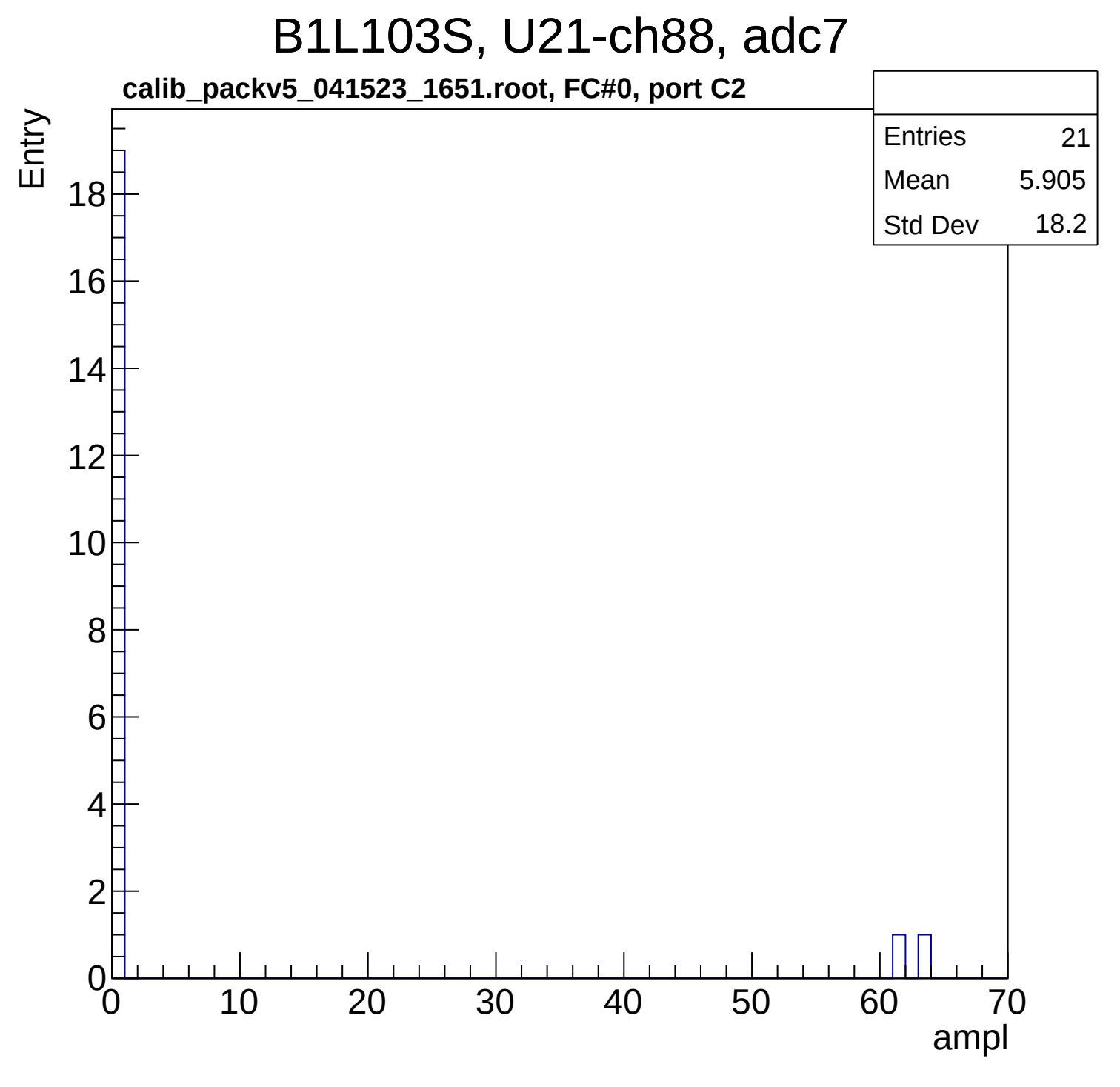
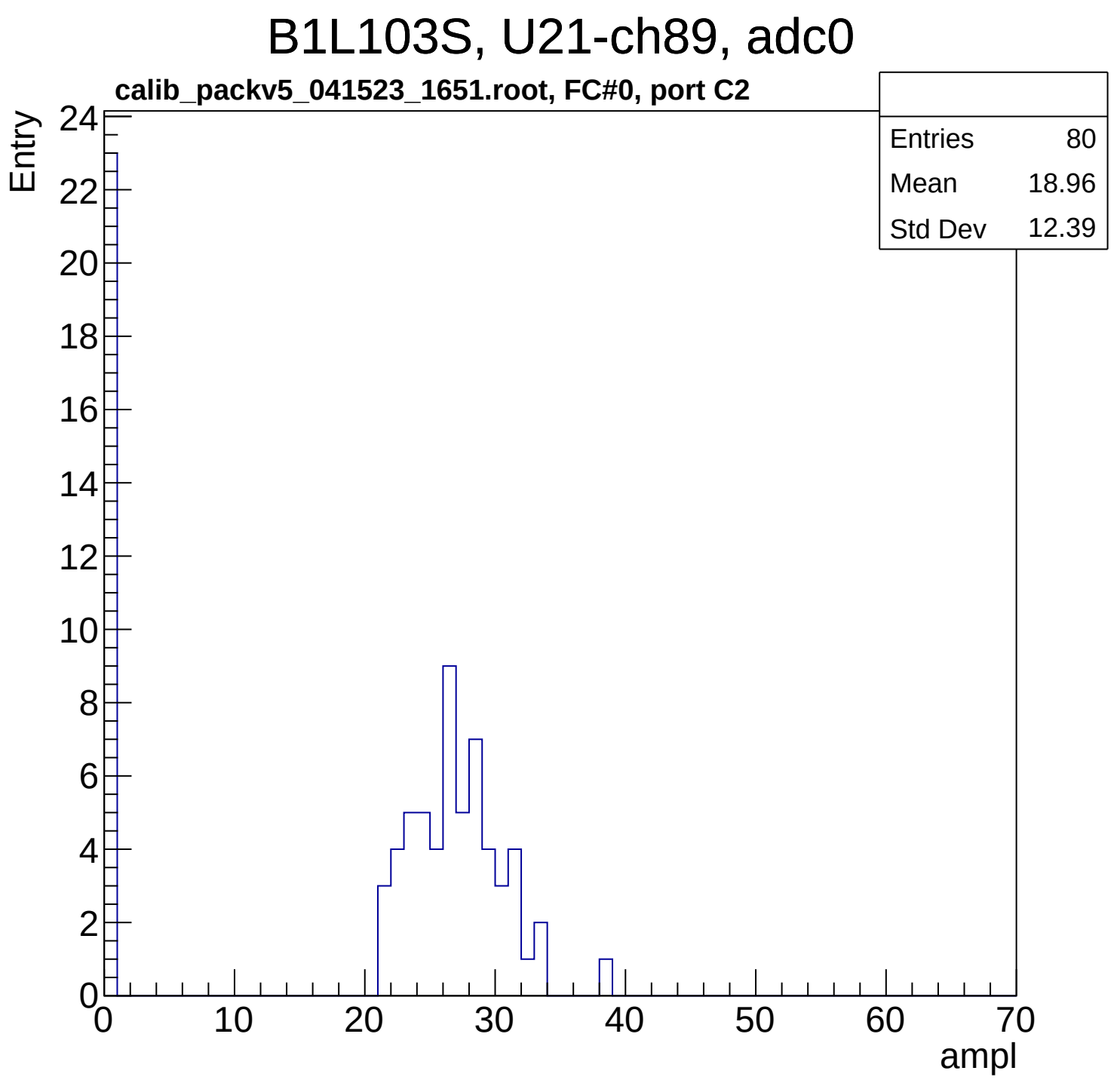
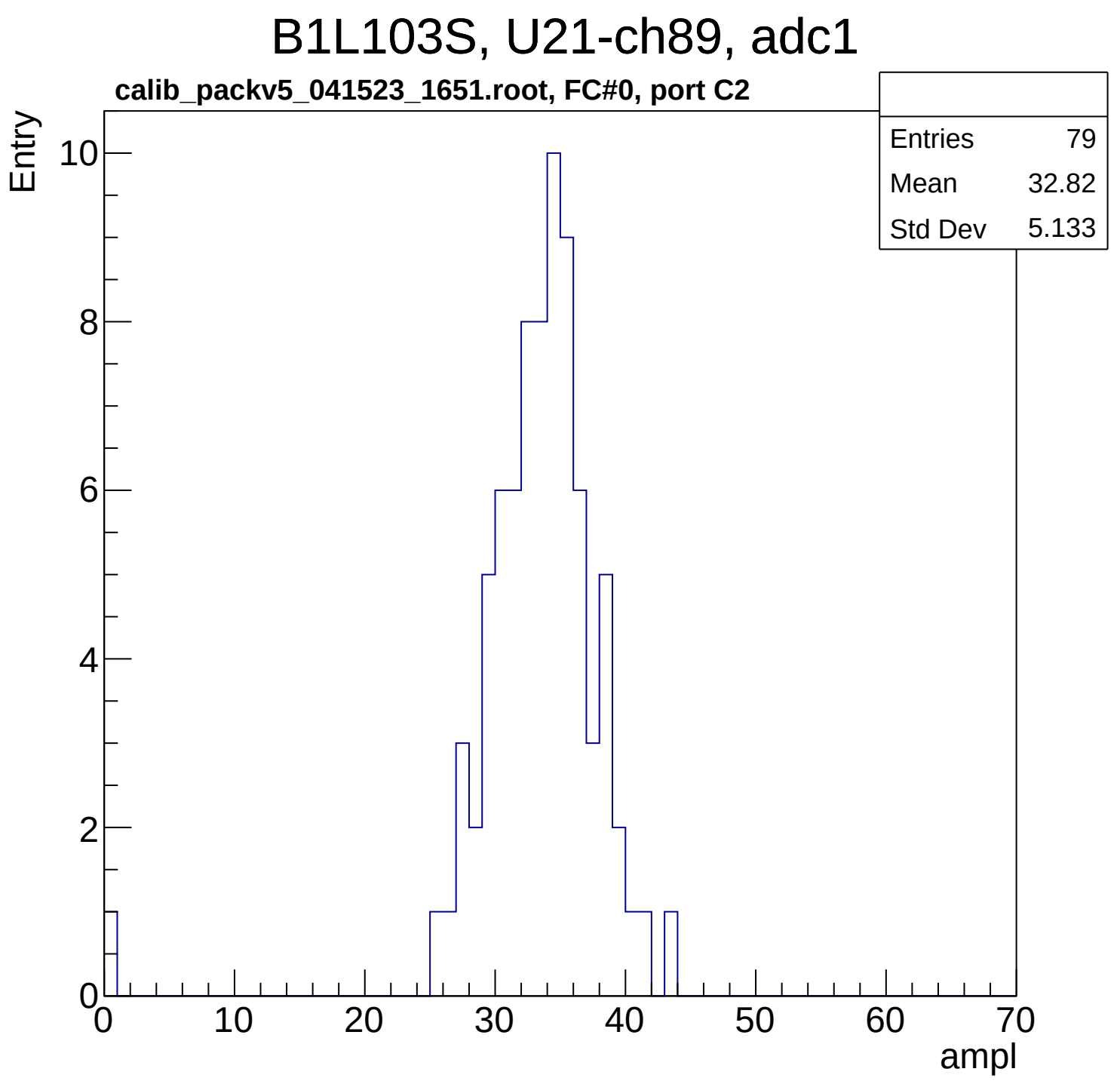
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

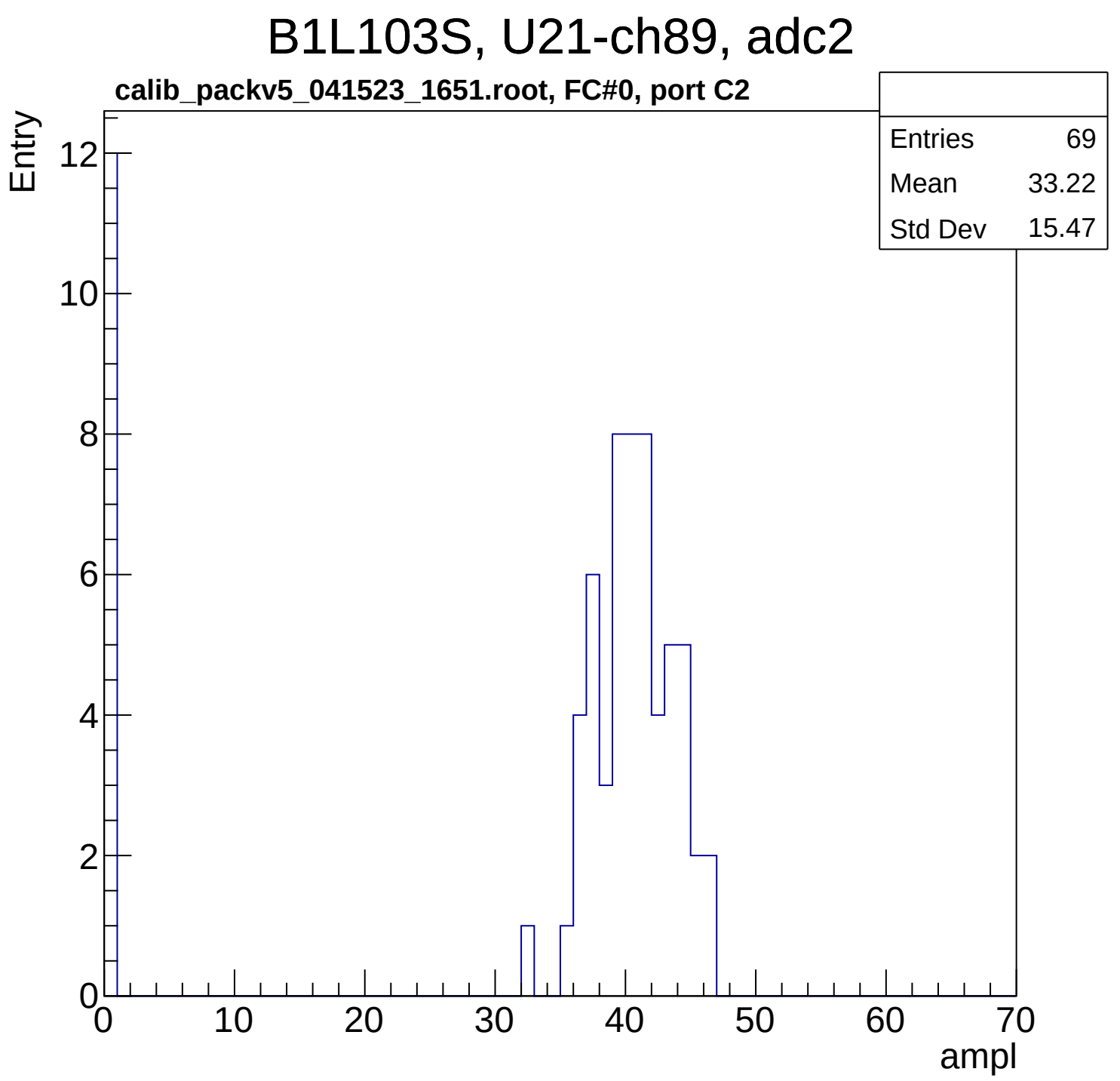

B1L103S, U21-ch88, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 57.74
Std Dev 8.426
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch88, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 60.21
Std Dev 1.739
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U21-ch88, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.905
Std Dev 18.2
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch89, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 18.96
Std Dev 12.39
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
24
0
10
20
30
40
50
60
70


B1L103S, U21-ch89, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 32.82
Std Dev 5.133
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch89, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 33.22
Std Dev 15.47
Entry
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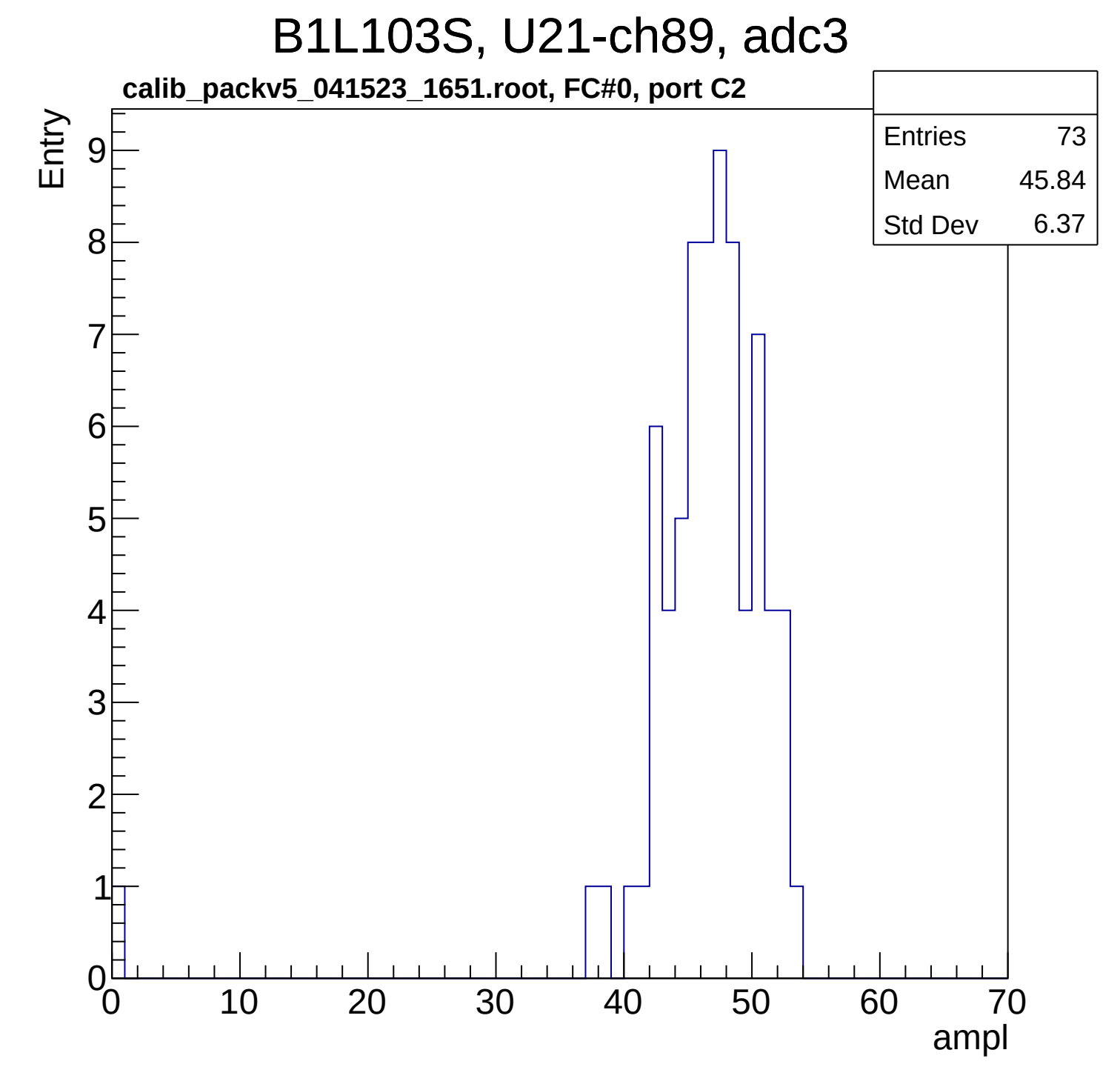
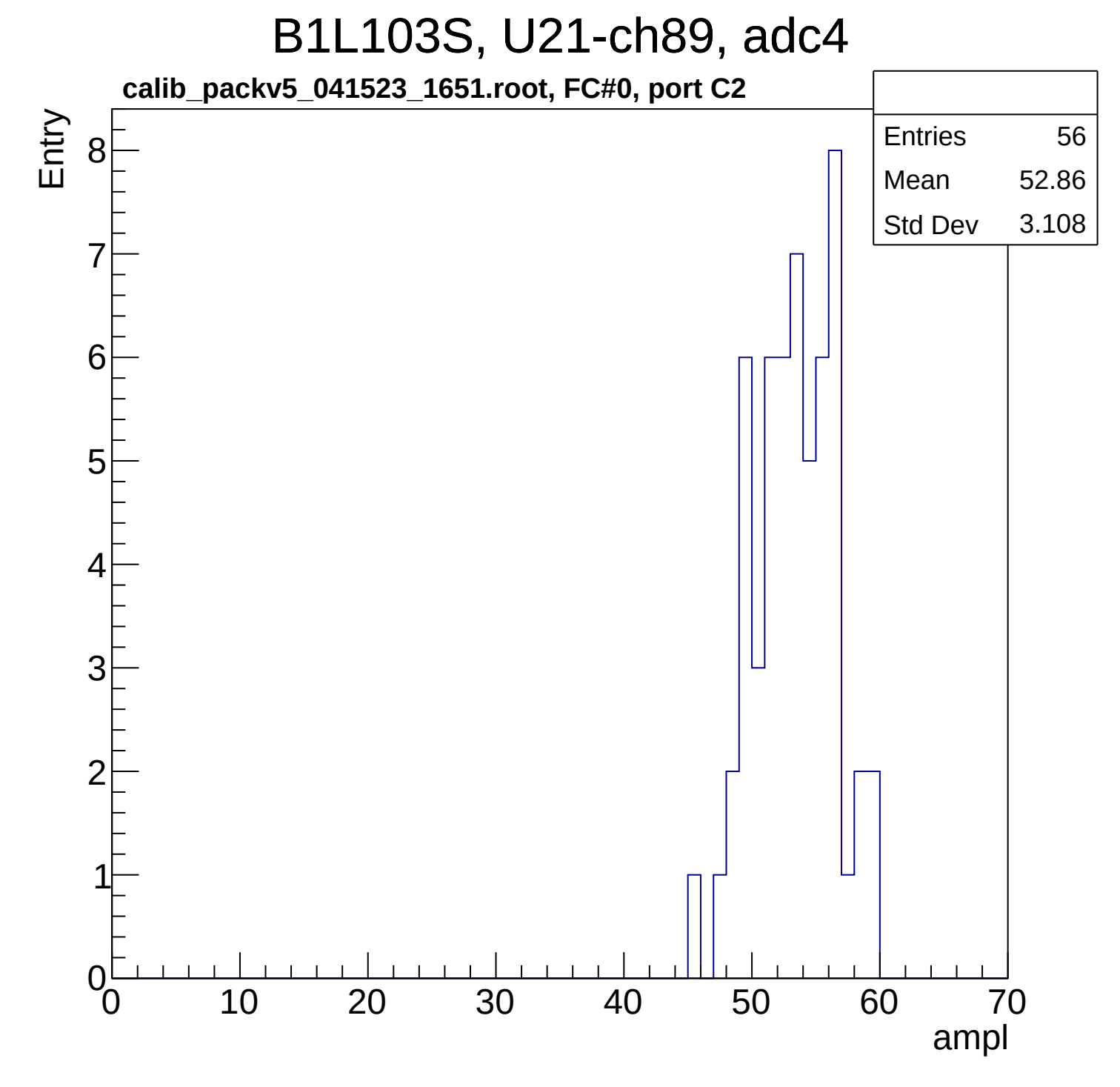
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch89, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 45.84
Std Dev 6.37
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch89, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 52.86
Std Dev 3.108
Entry
ampl
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4
5
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7
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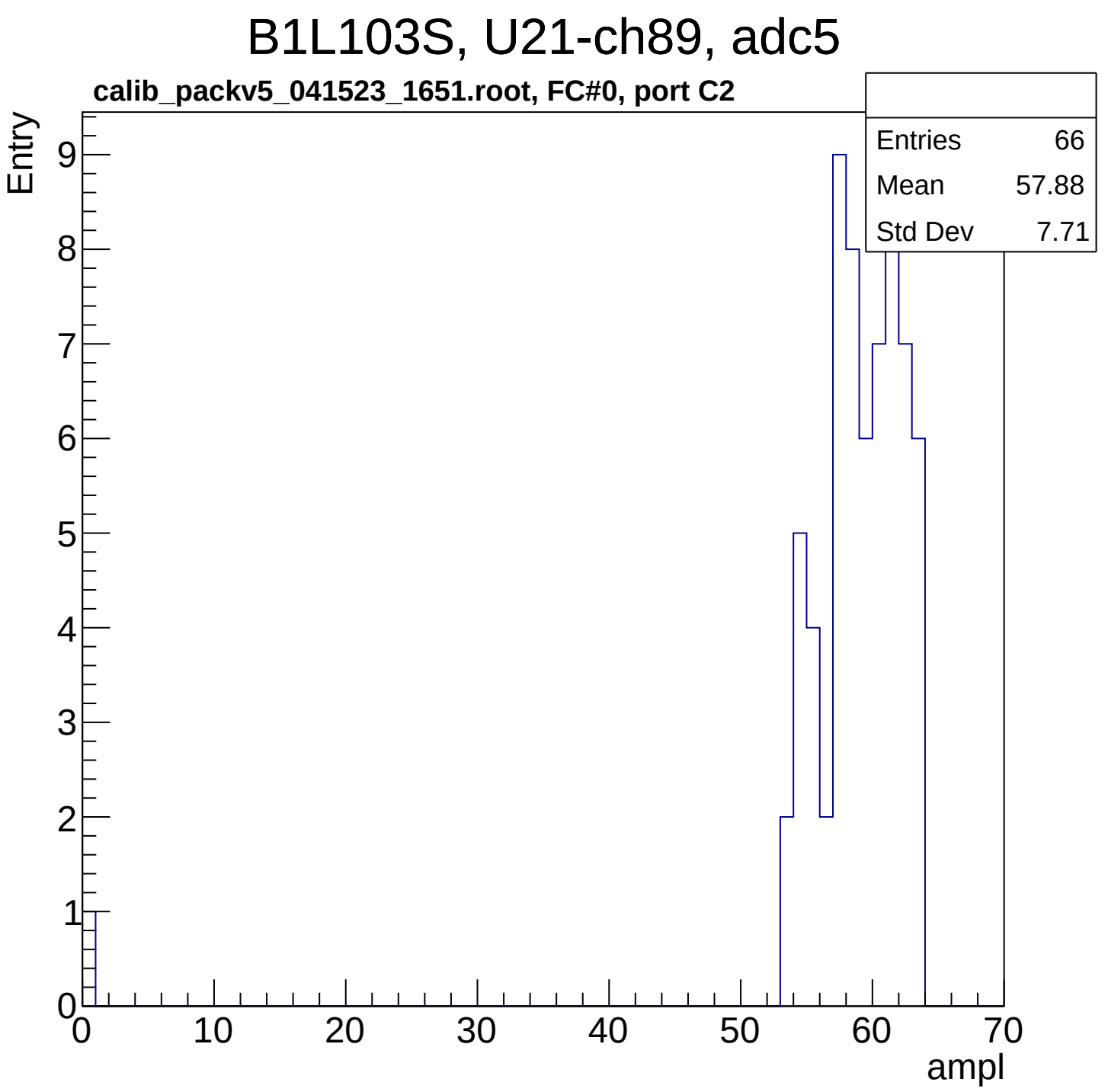
B1L103S, U21-ch89, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 57.88
Std Dev 7.71
Entry
ampl
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3
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6
7
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0
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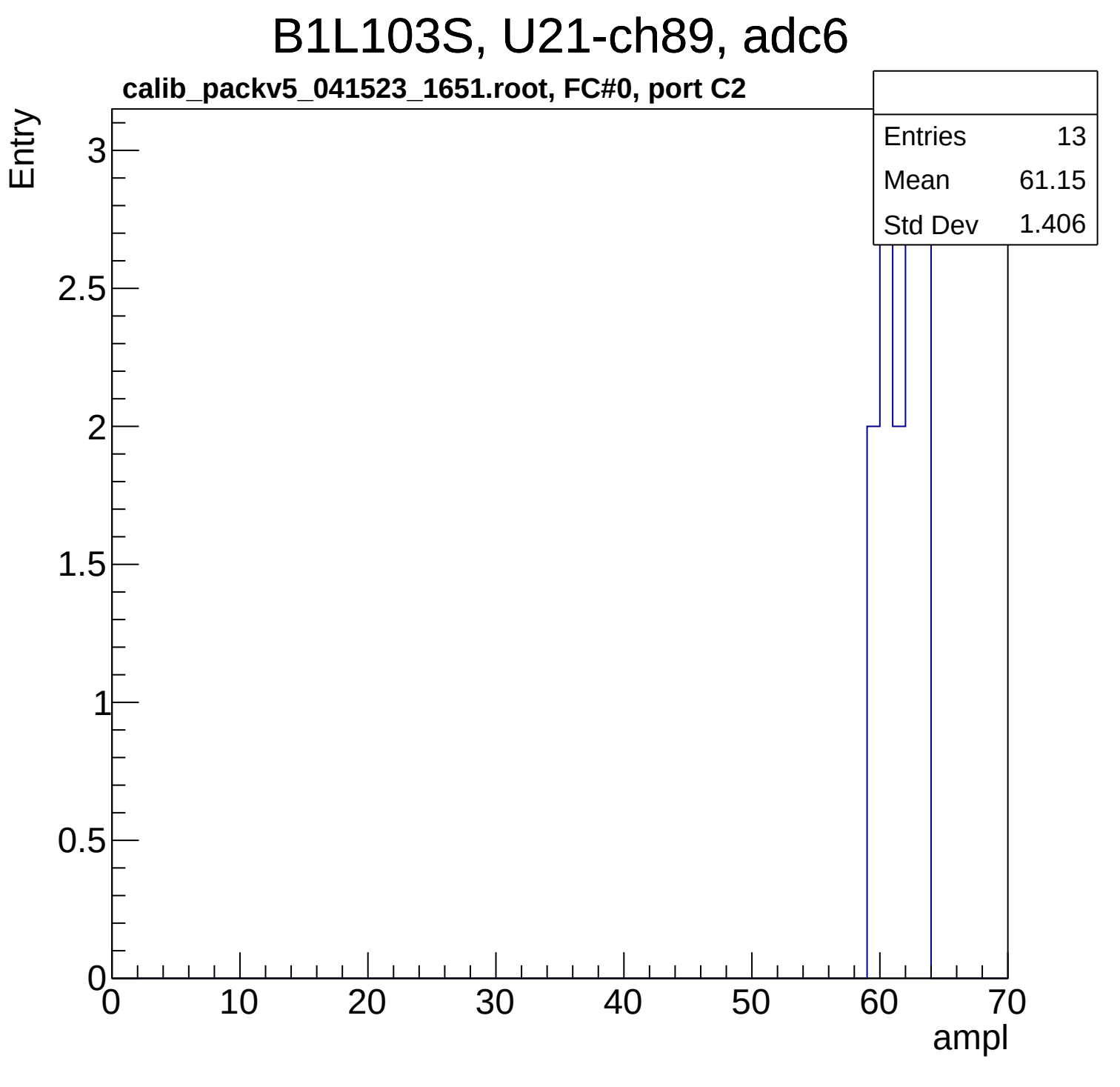
B1L103S, U21-ch89, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 61.15
Std Dev 1.406
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
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40
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60
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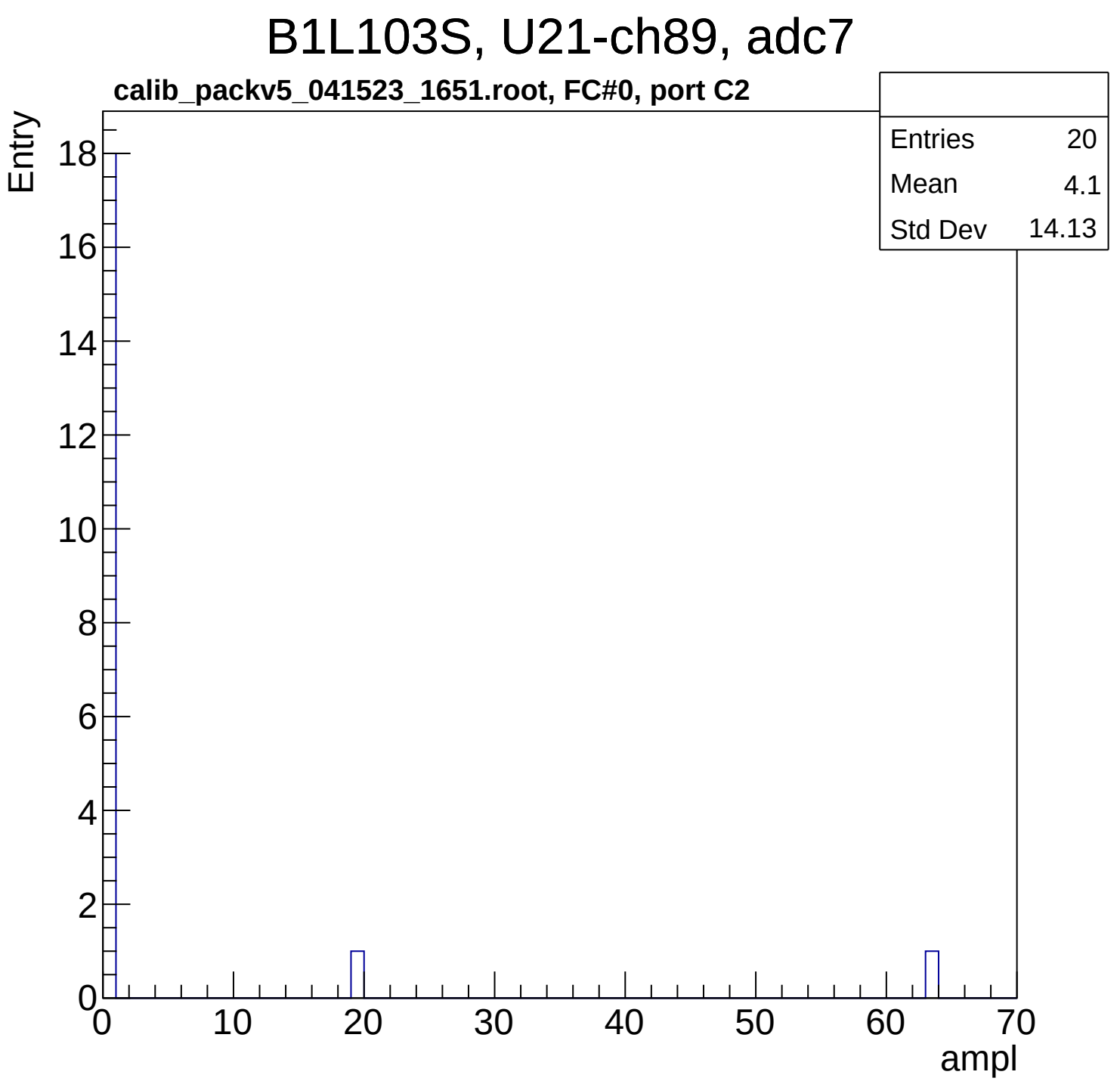
B1L103S, U21-ch89, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4.1
Std Dev 14.13
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
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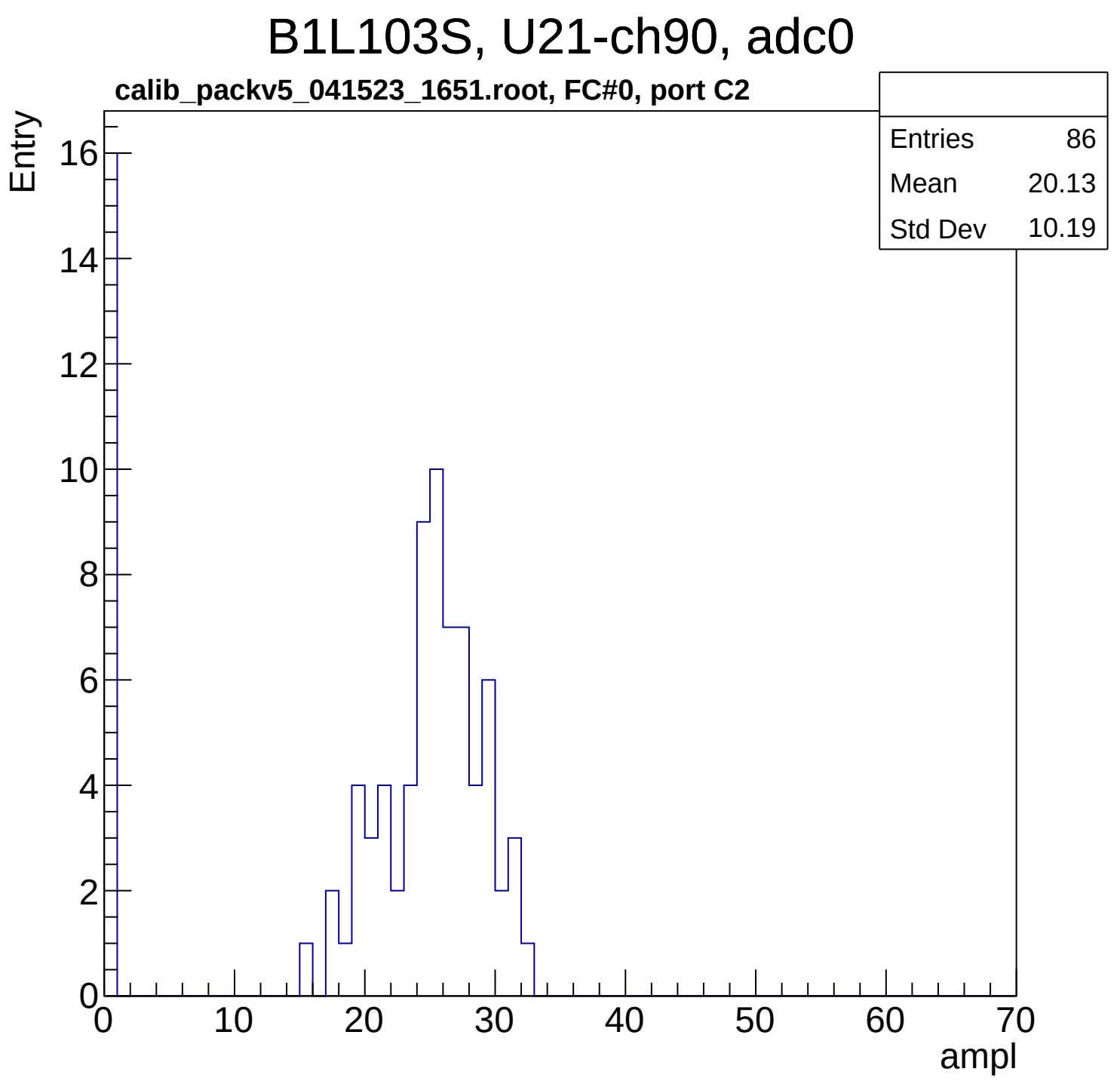
40
50
60
70
ampl


B1L103S, U21-ch90, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 20.13
Std Dev 10.19
Entry
ampl
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4
6
8
10
12
14
16
0
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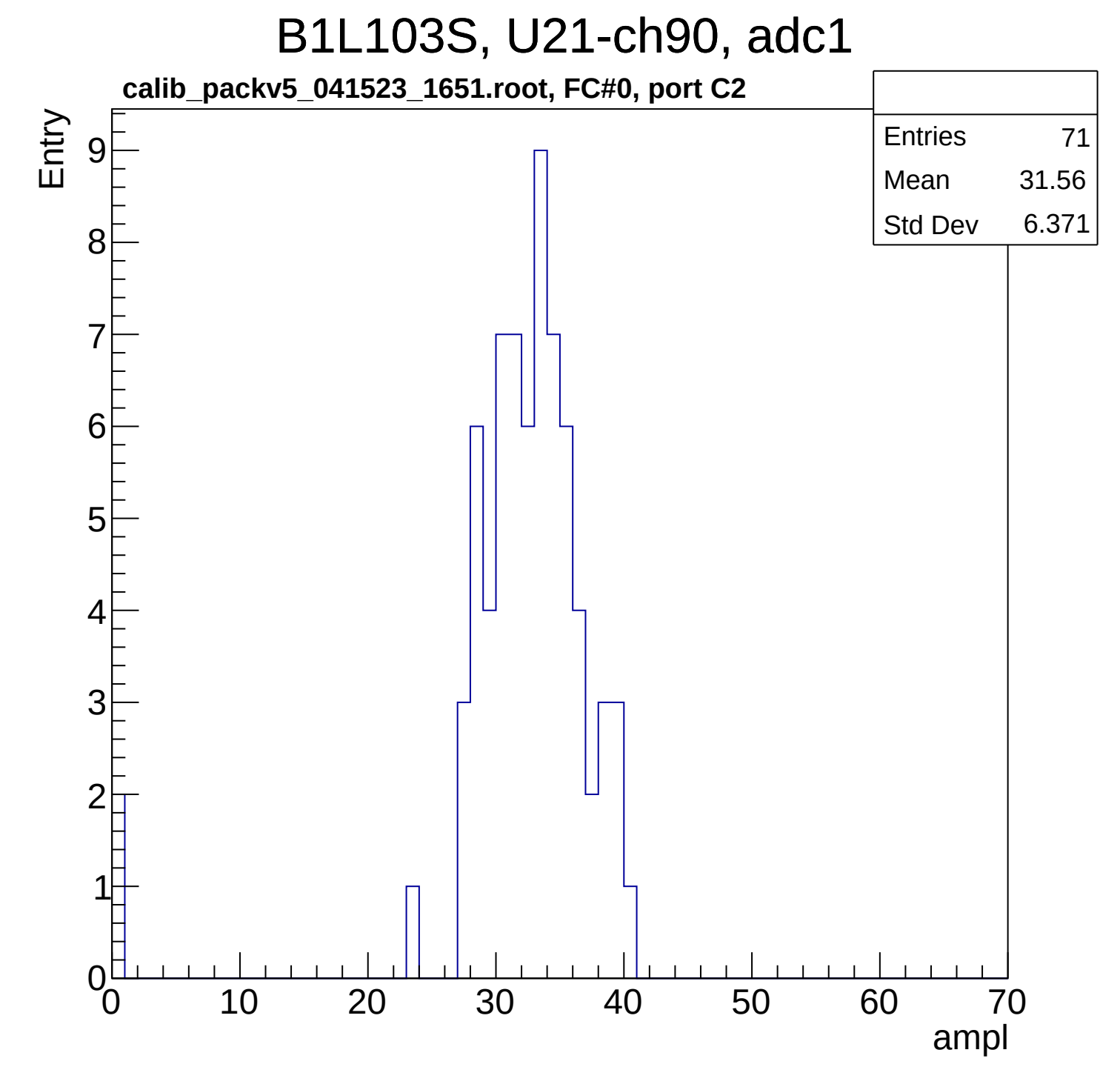
B1L103S, U21-ch90, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 31.56
Std Dev 6.371
Entry
ampl
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3
4
5
6
7
8
9
0
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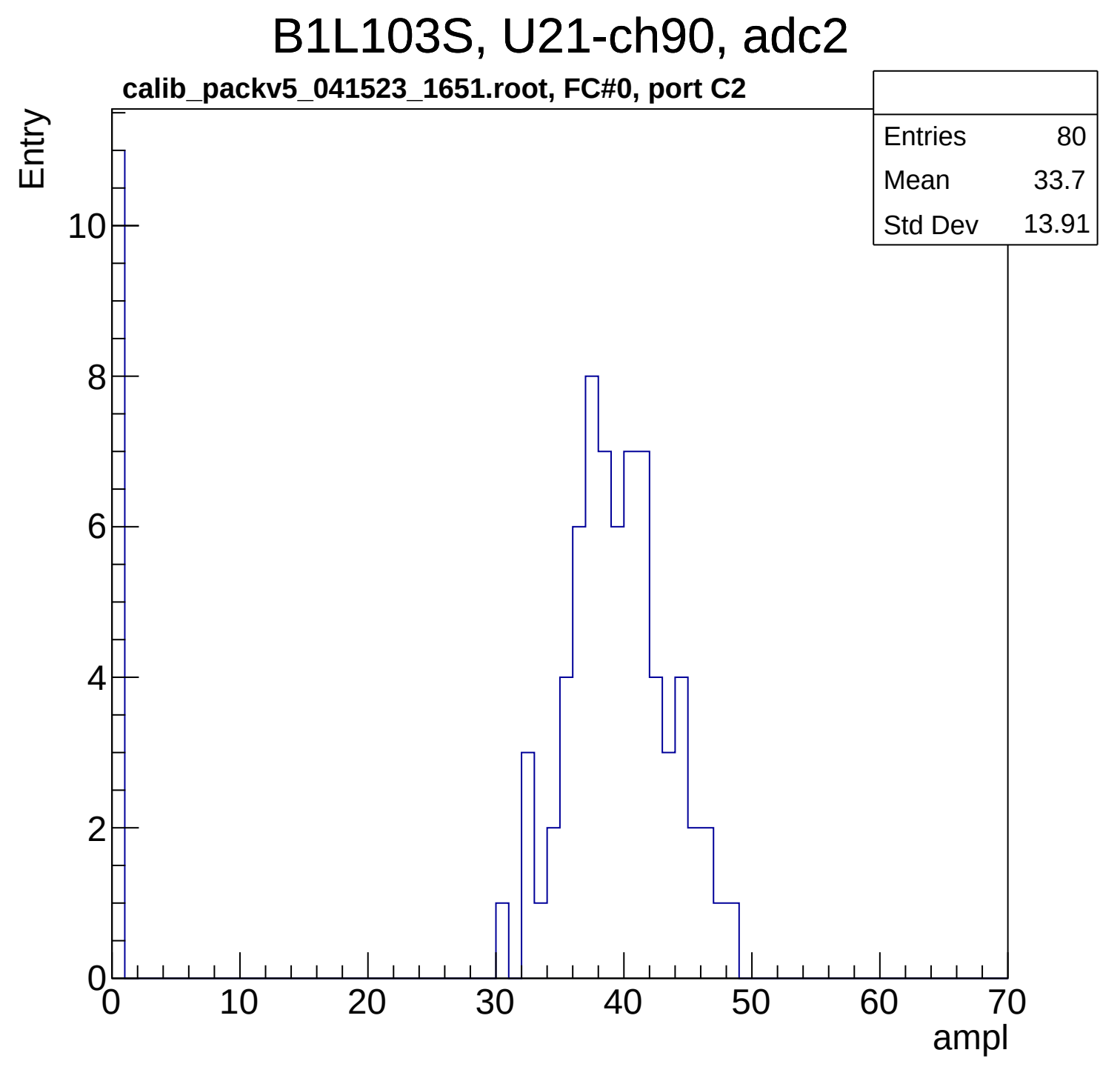
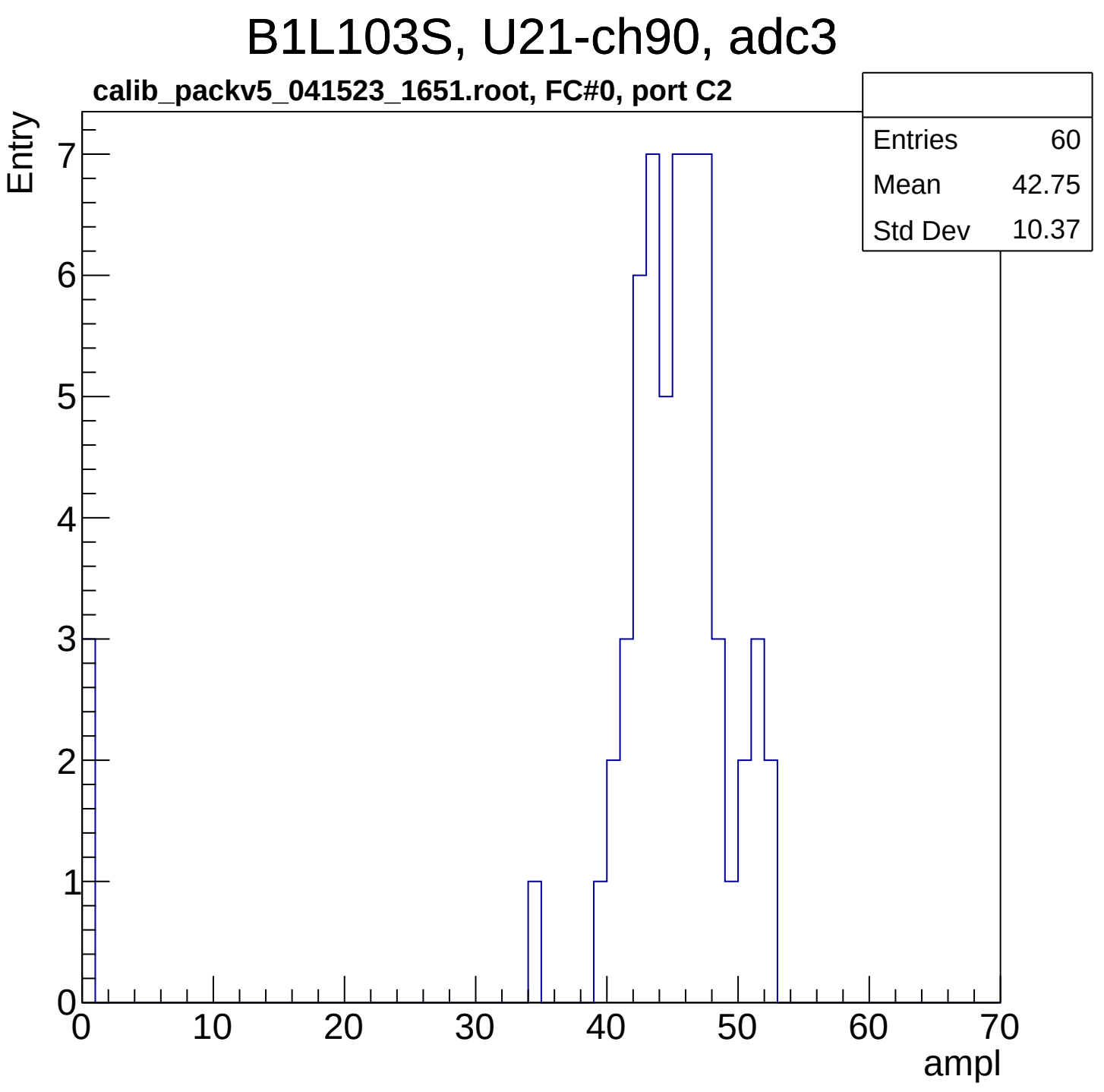

B1L103S, U21-ch90, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 33.7
Std Dev 13.91
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch90, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 42.75
Std Dev 10.37
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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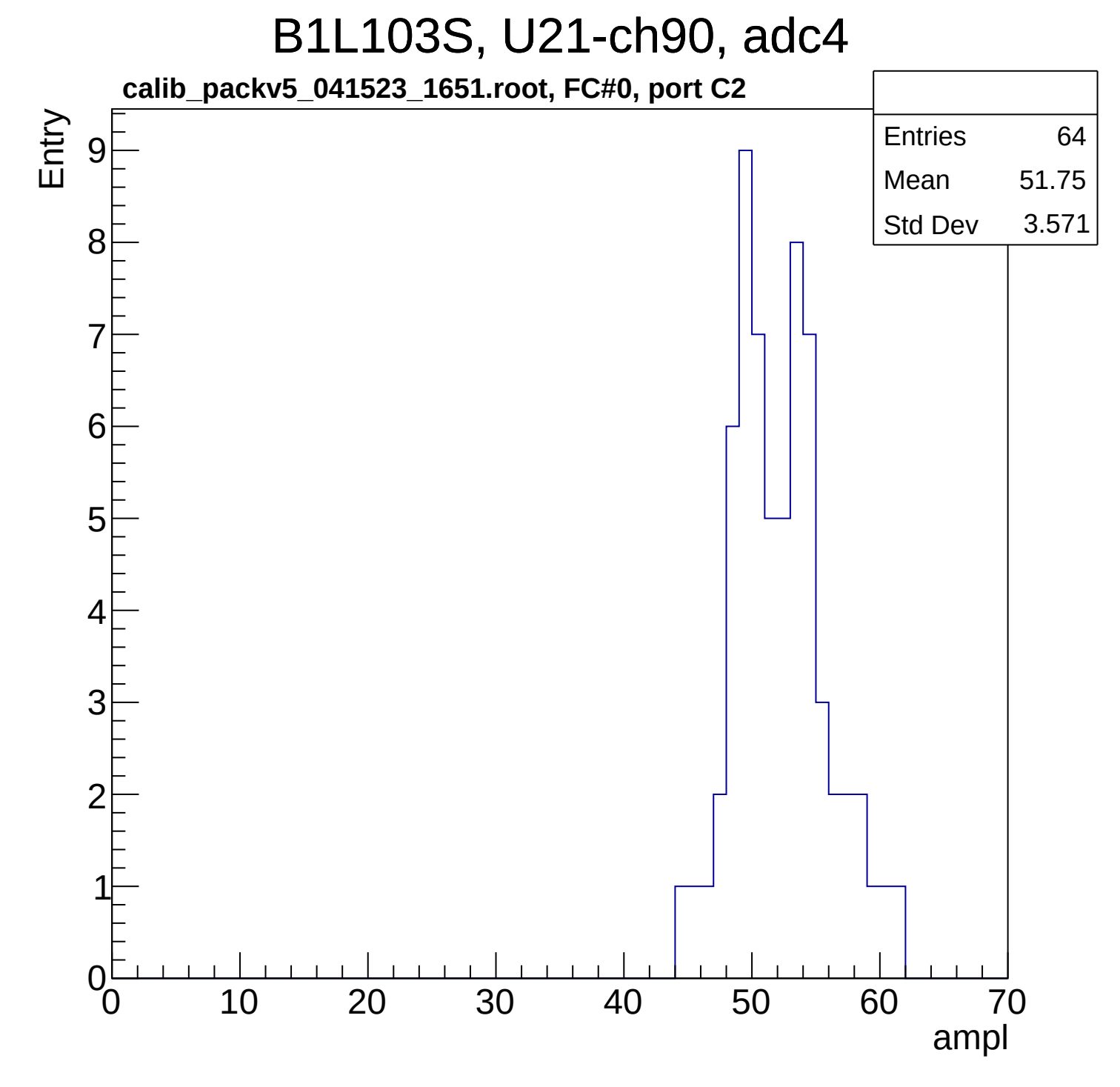
B1L103S, U21-ch90, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 51.75
Std Dev 3.571
Entry
ampl
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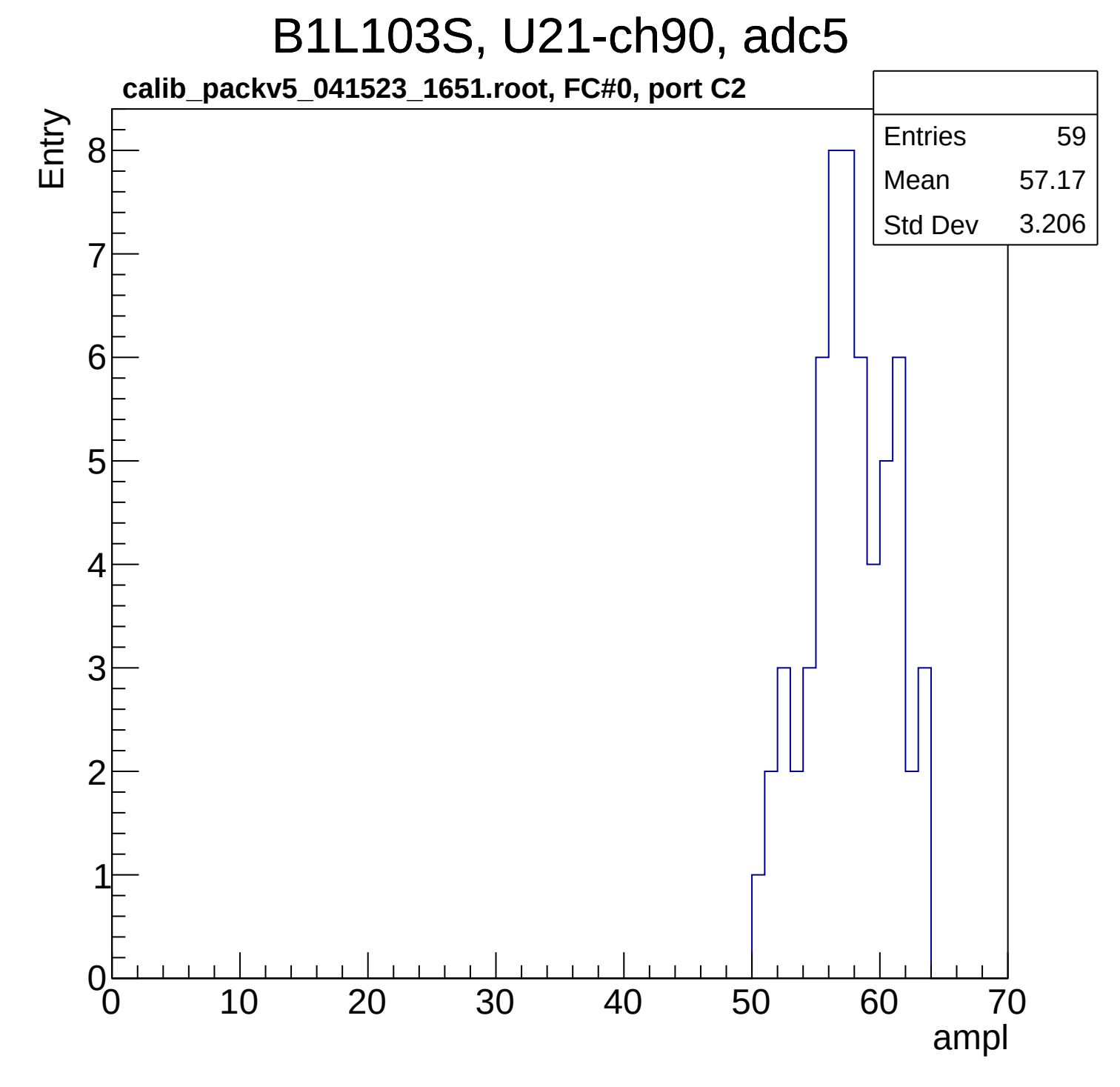
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch90, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 57.17
Std Dev 3.206
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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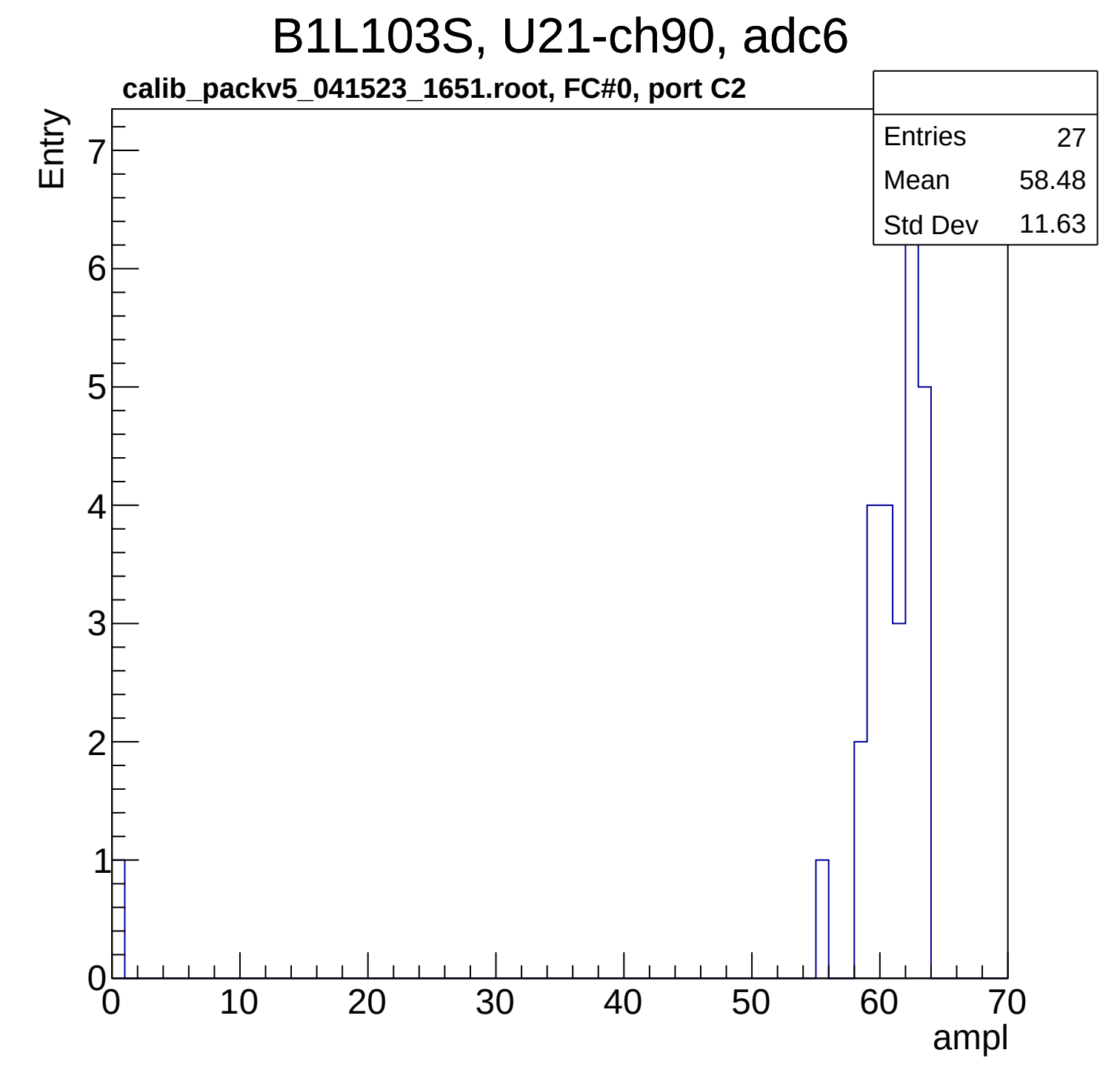
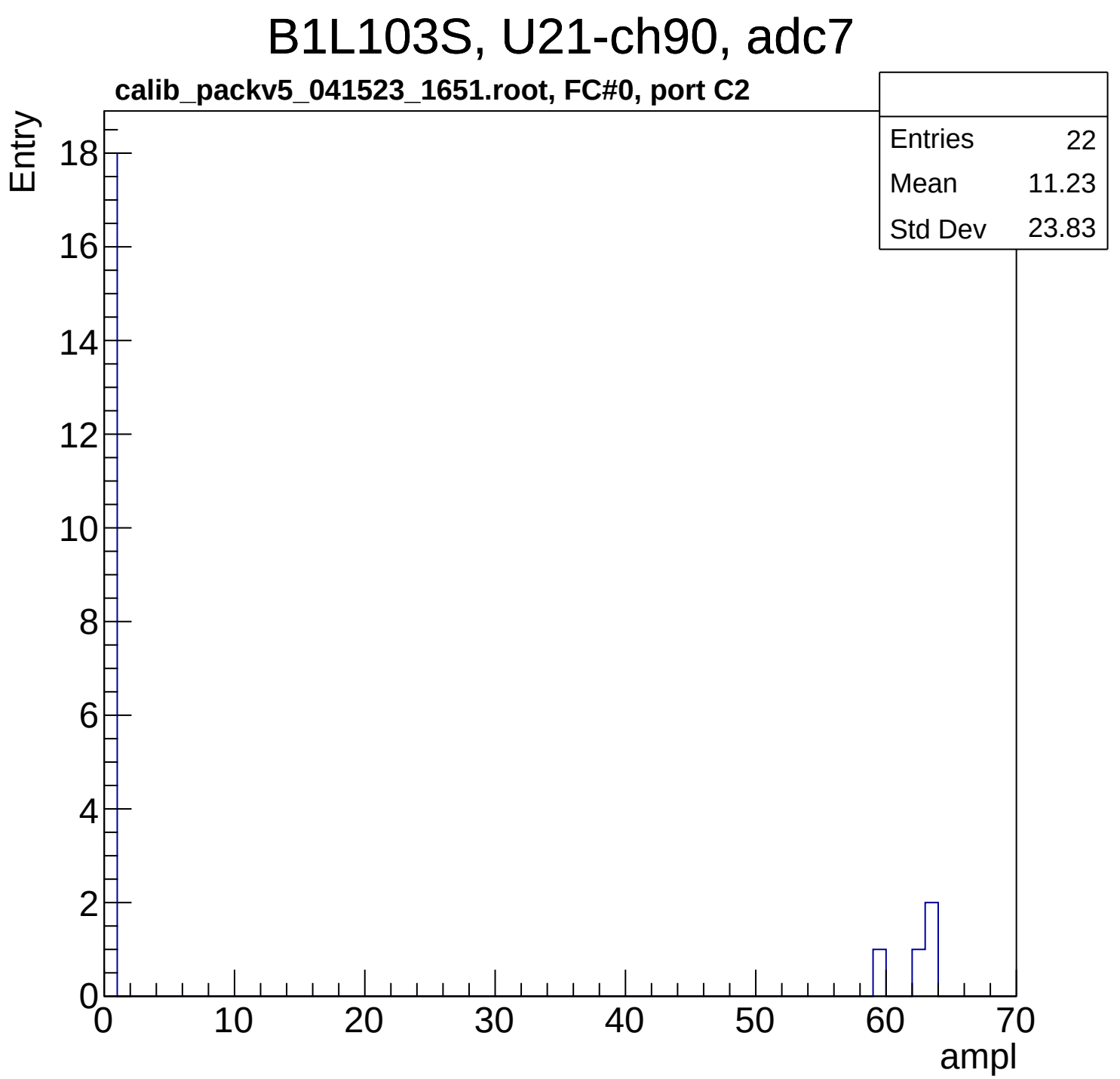
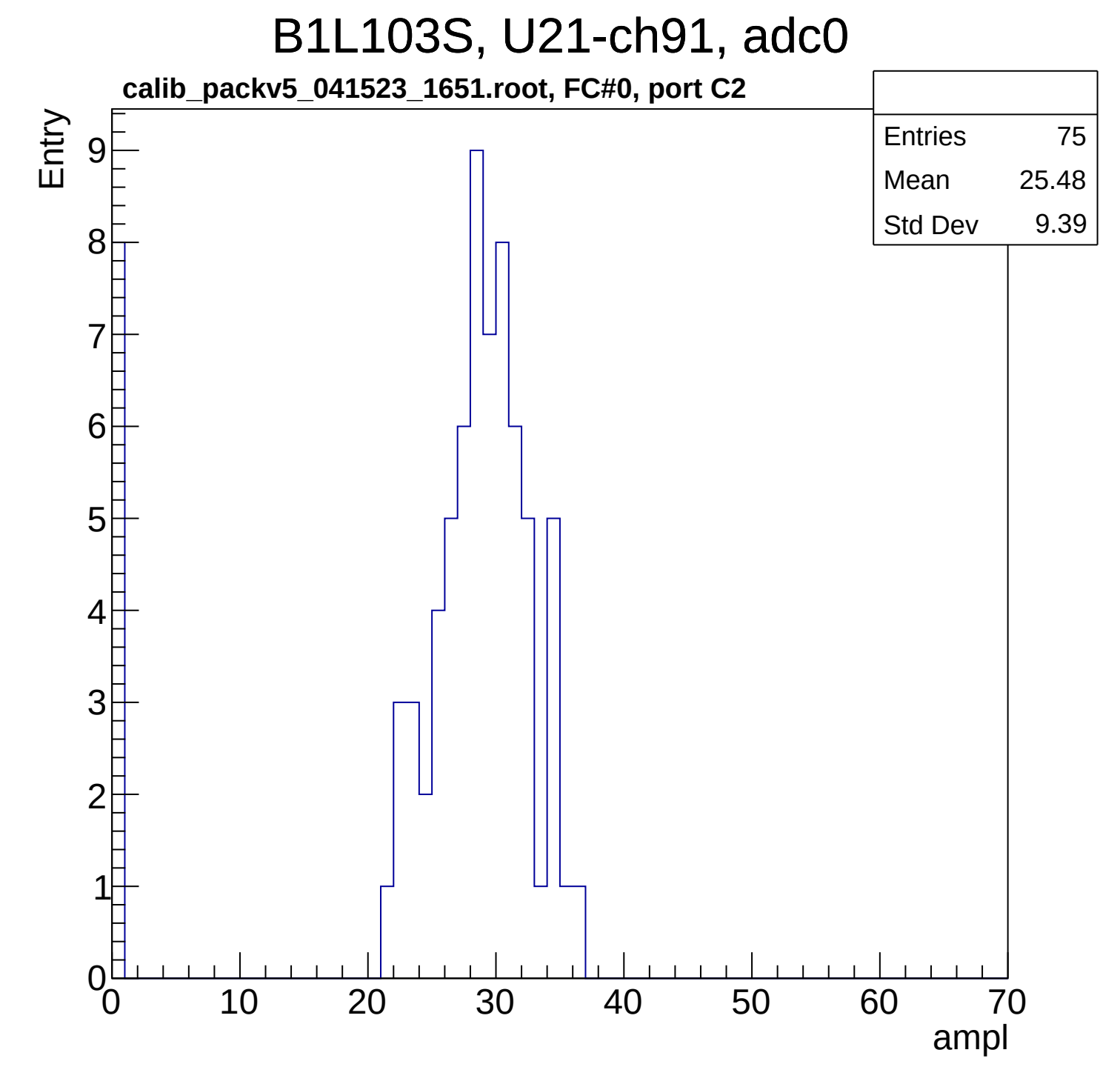

B1L103S, U21-ch90, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 58.48
Std Dev 11.63
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U21-ch90, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 11.23
Std Dev 23.83
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch91, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 25.48
Std Dev 9.39
Entry
ampl
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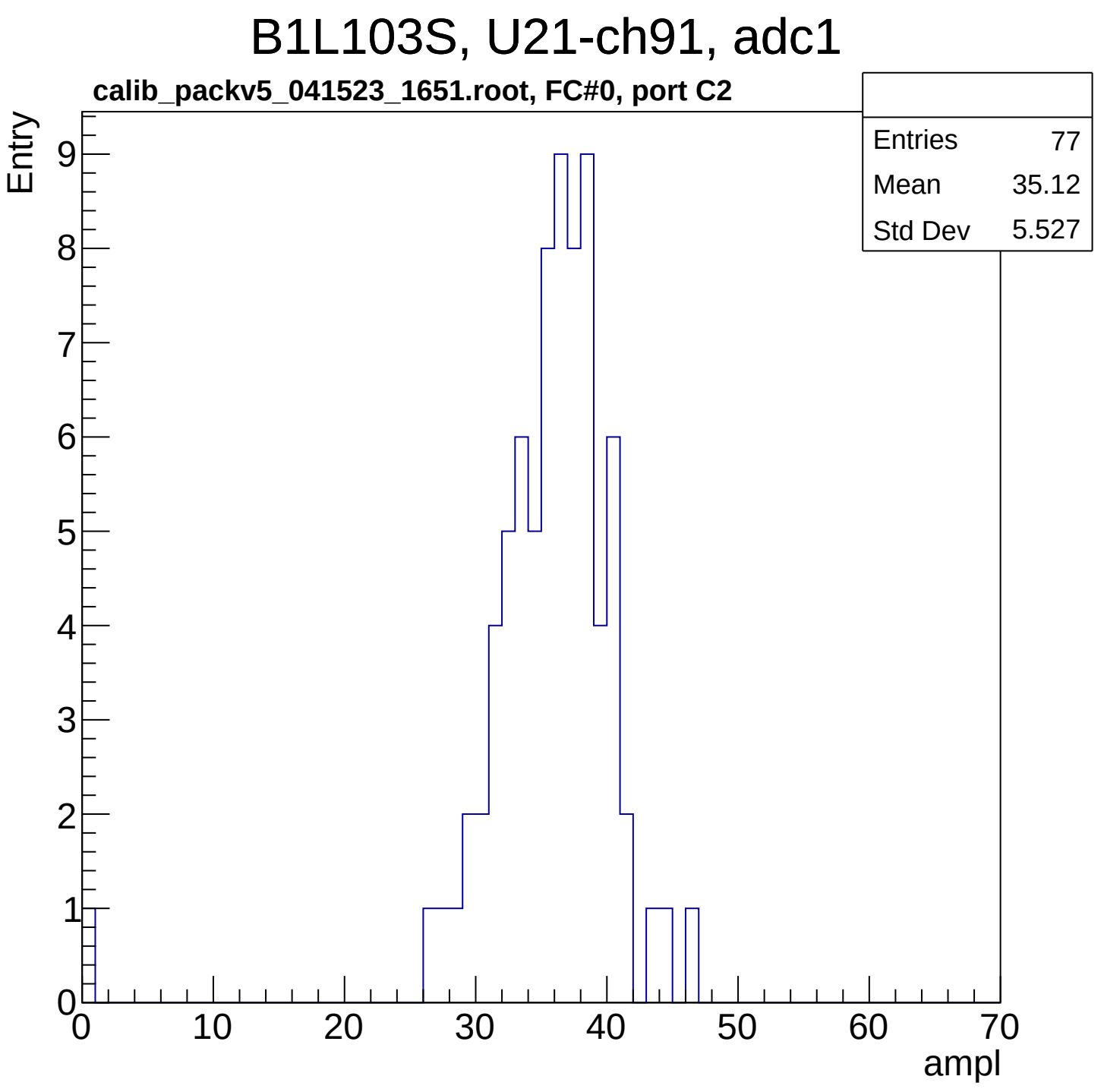
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch91, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 35.12
Std Dev 5.527
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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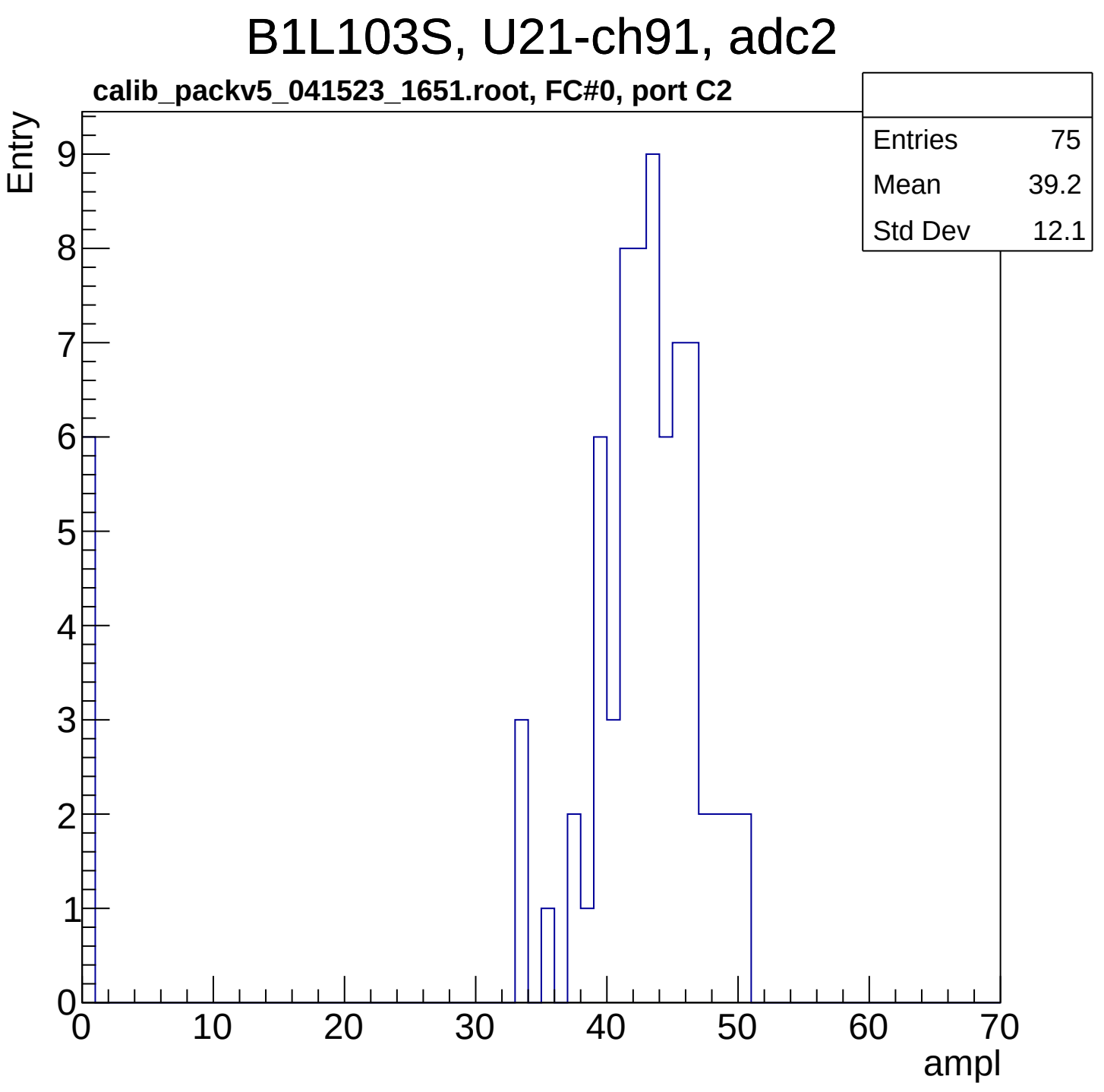
B1L103S, U21-ch91, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 39.2
Std Dev 12.1
Entry
ampl
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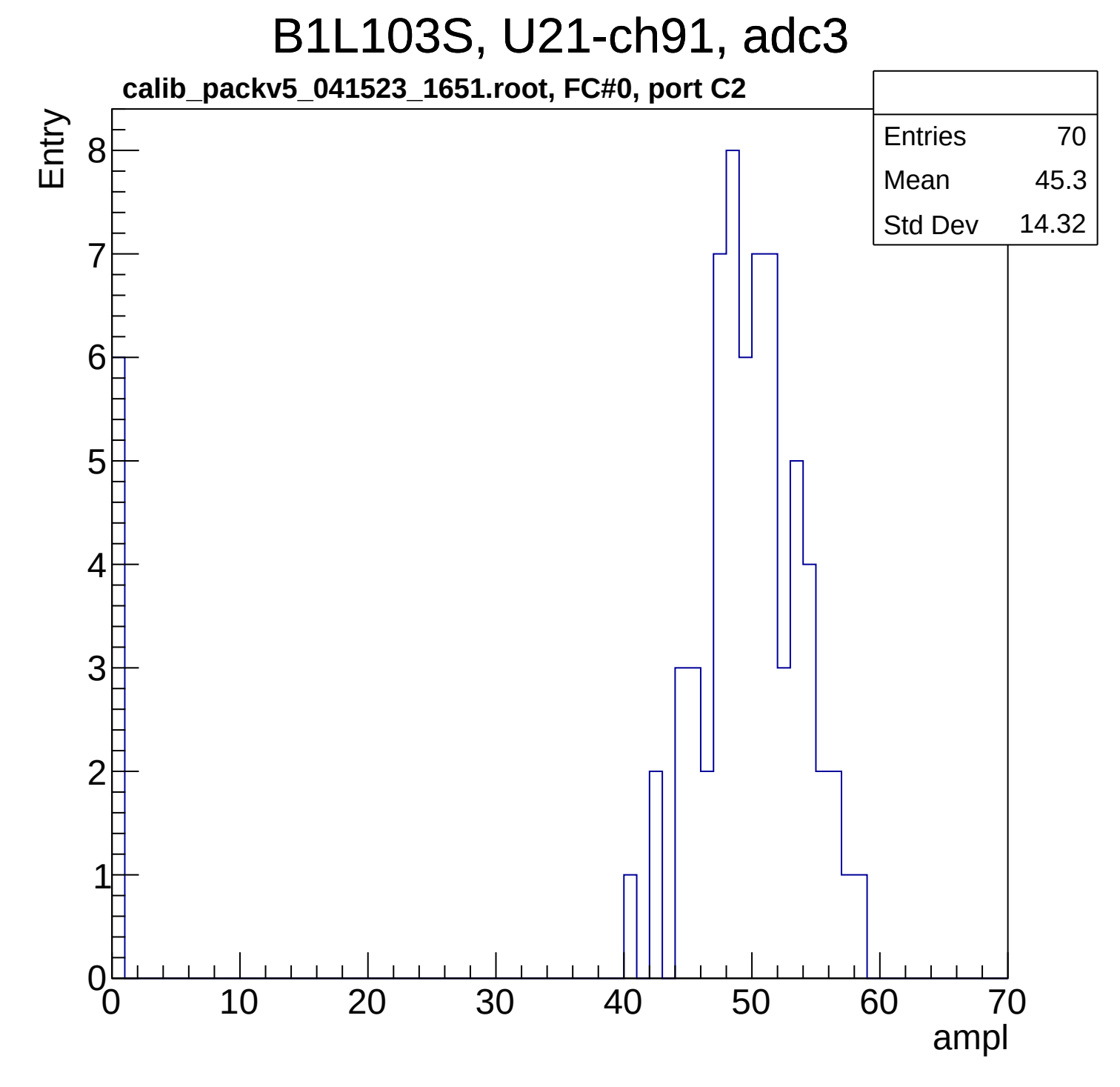
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch91, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 45.3
Std Dev 14.32
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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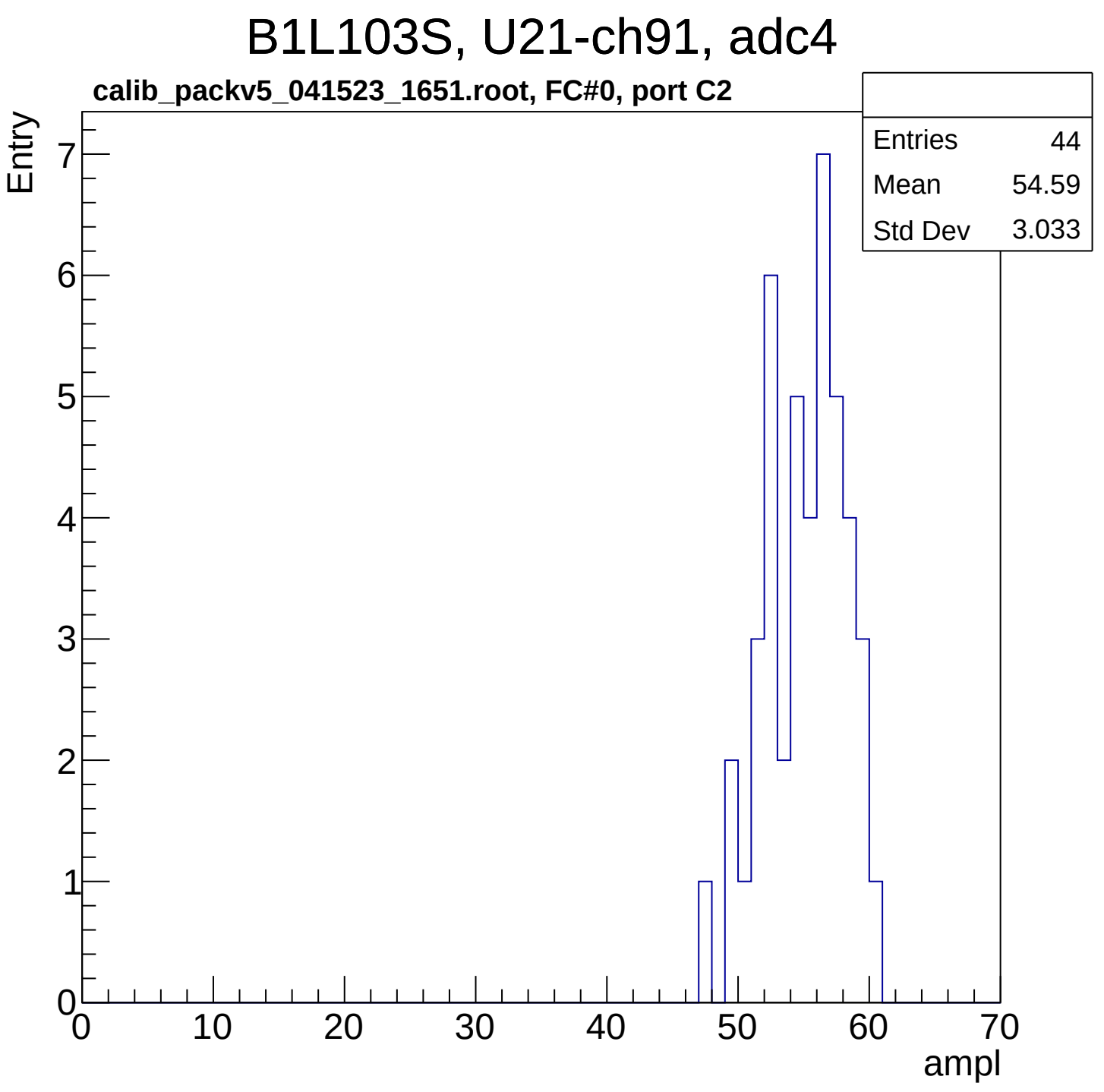
B1L103S, U21-ch91, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 54.59
Std Dev 3.033
Entry
ampl
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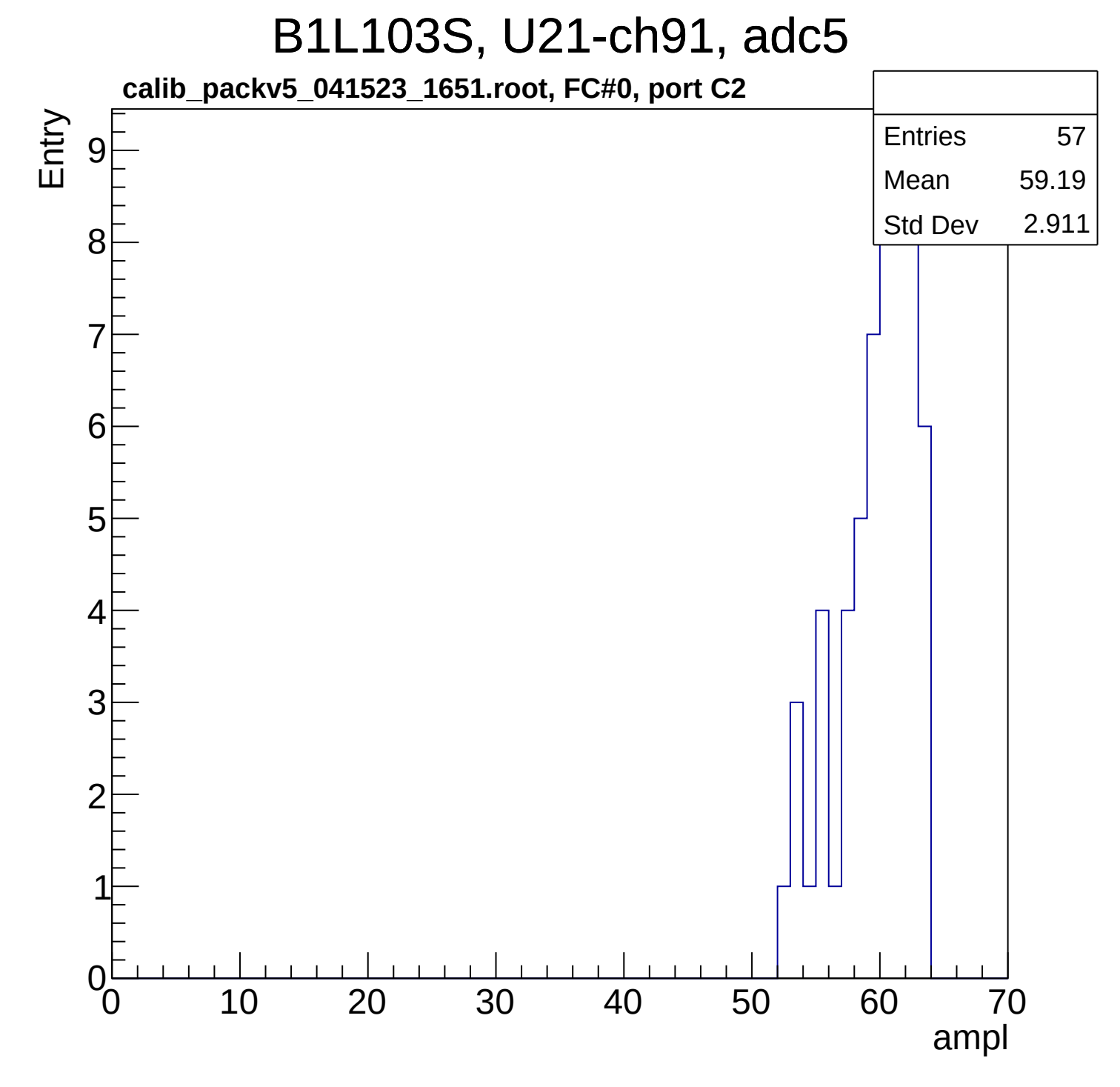
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U21-ch91, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 59.19
Std Dev 2.911
Entry
ampl
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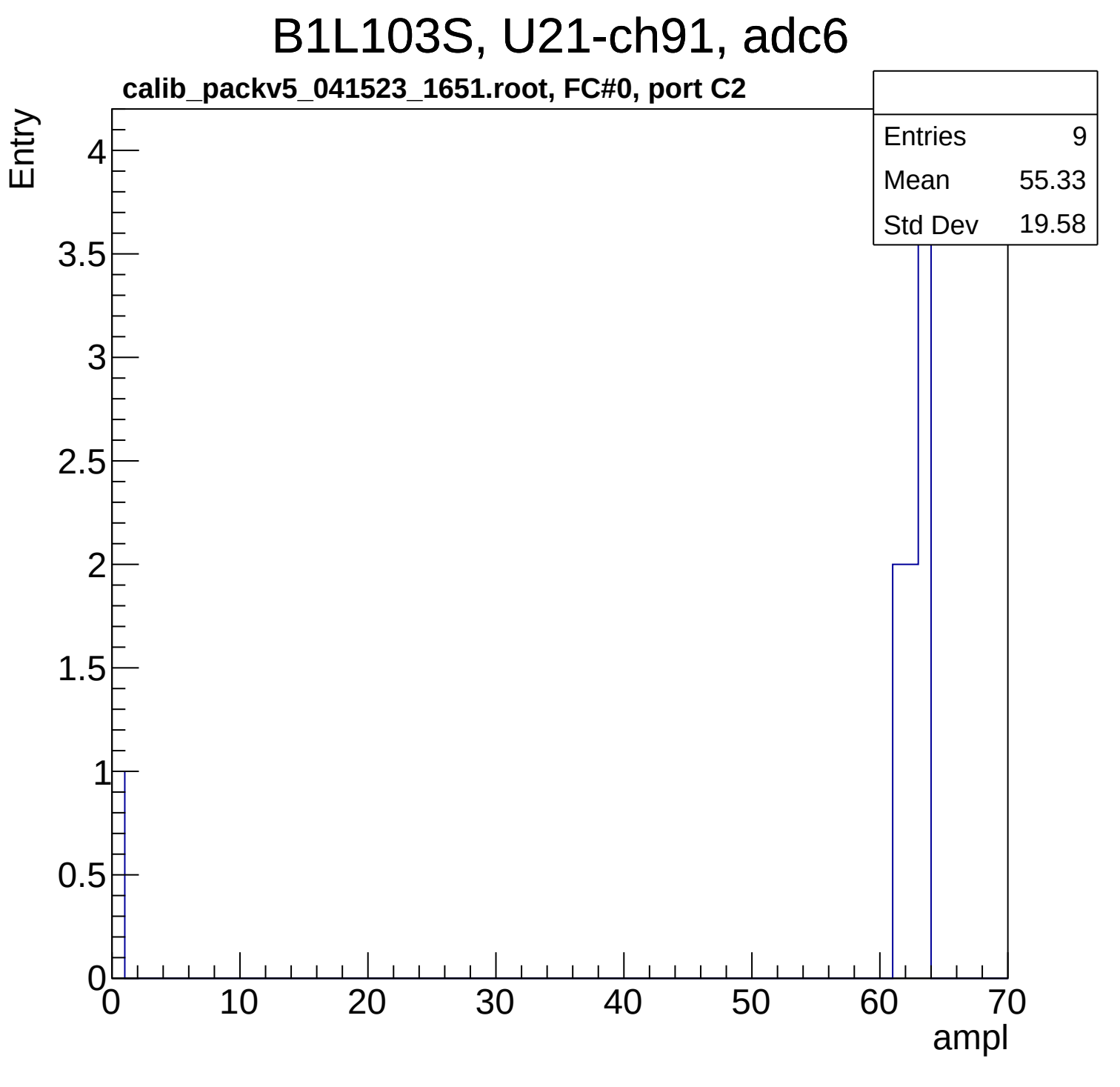
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch91, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 55.33
Std Dev 19.58
Entry
ampl
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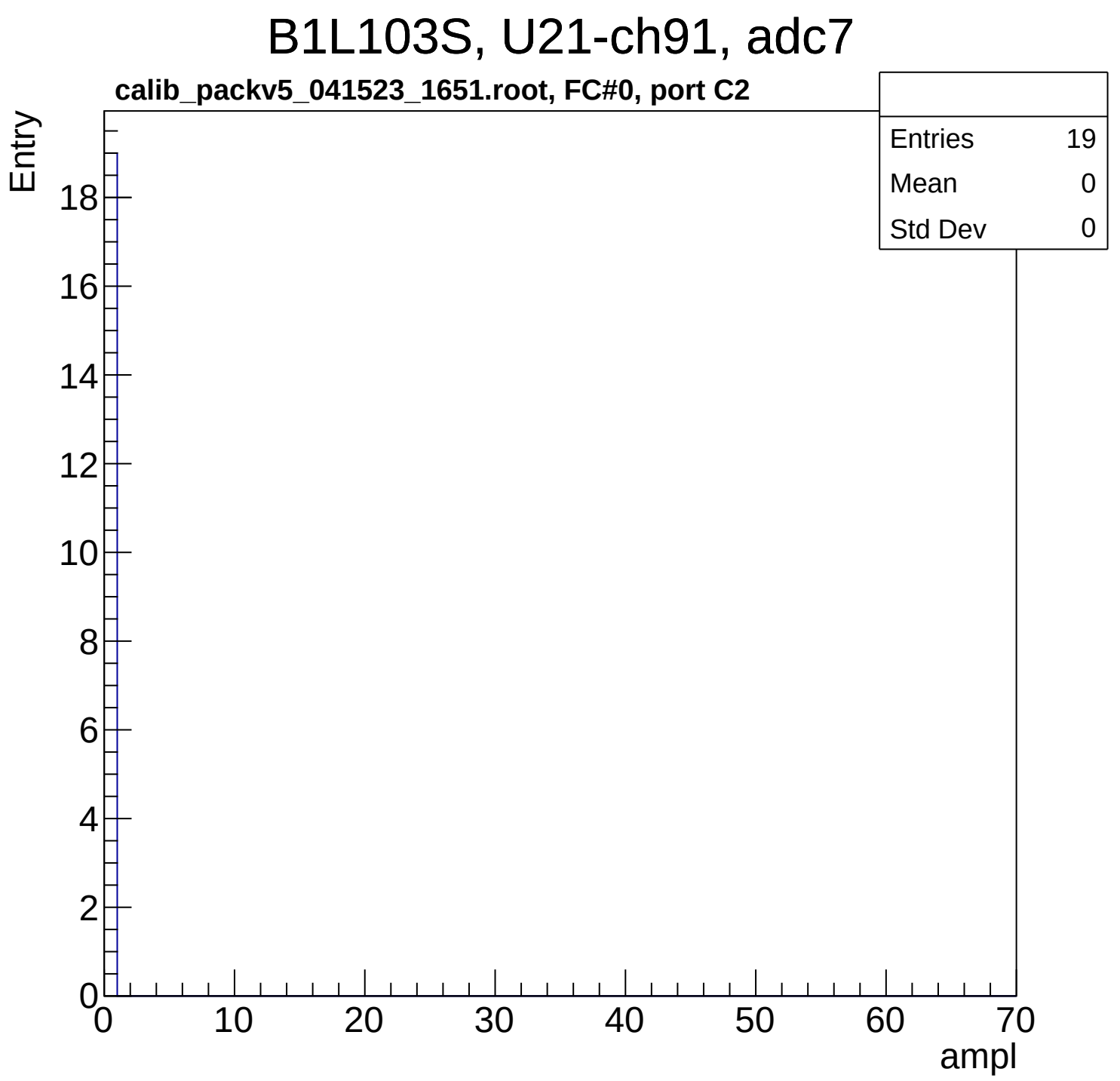
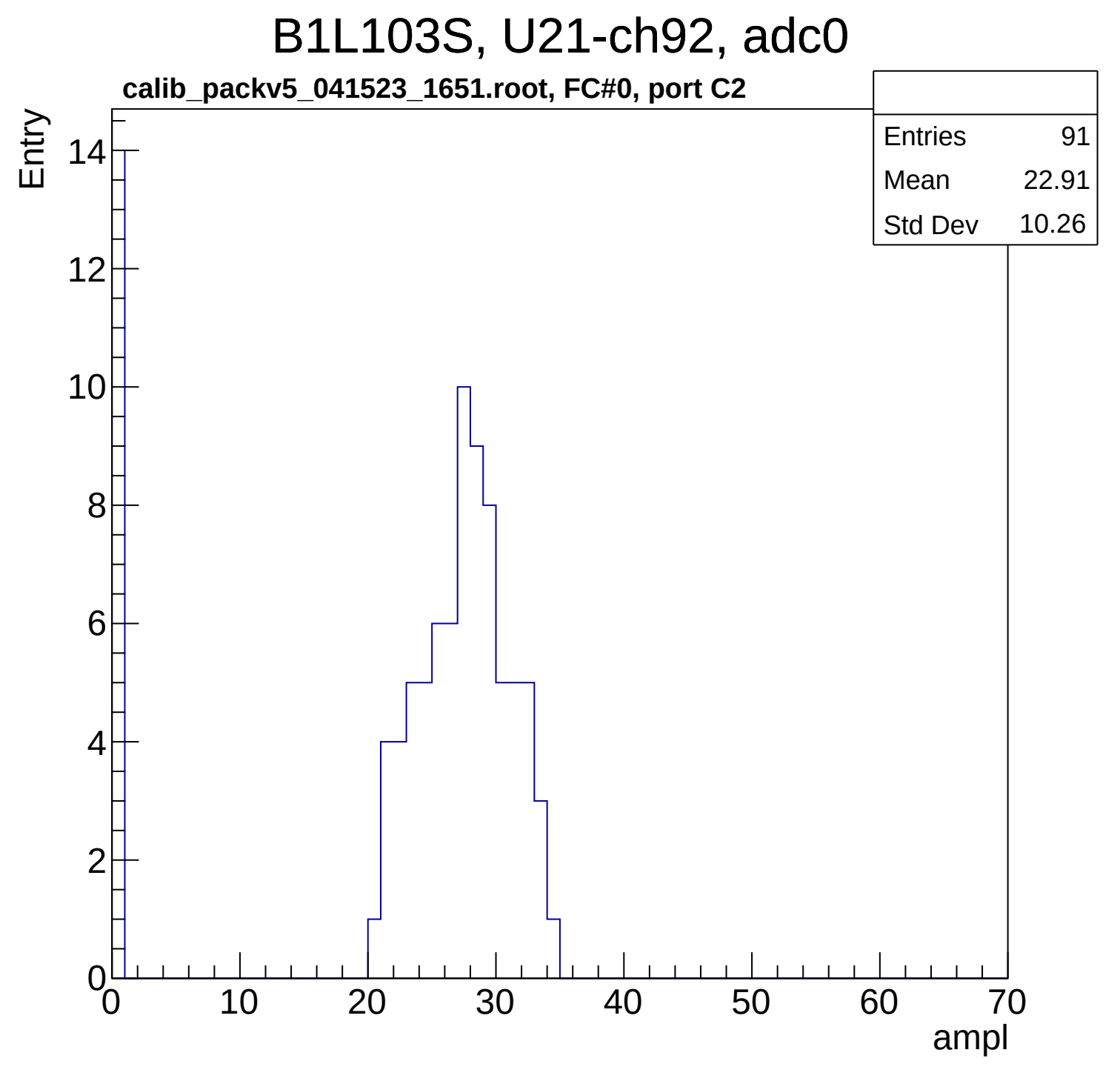
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U21-ch91, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch92, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 22.91
Std Dev 10.26
Entry
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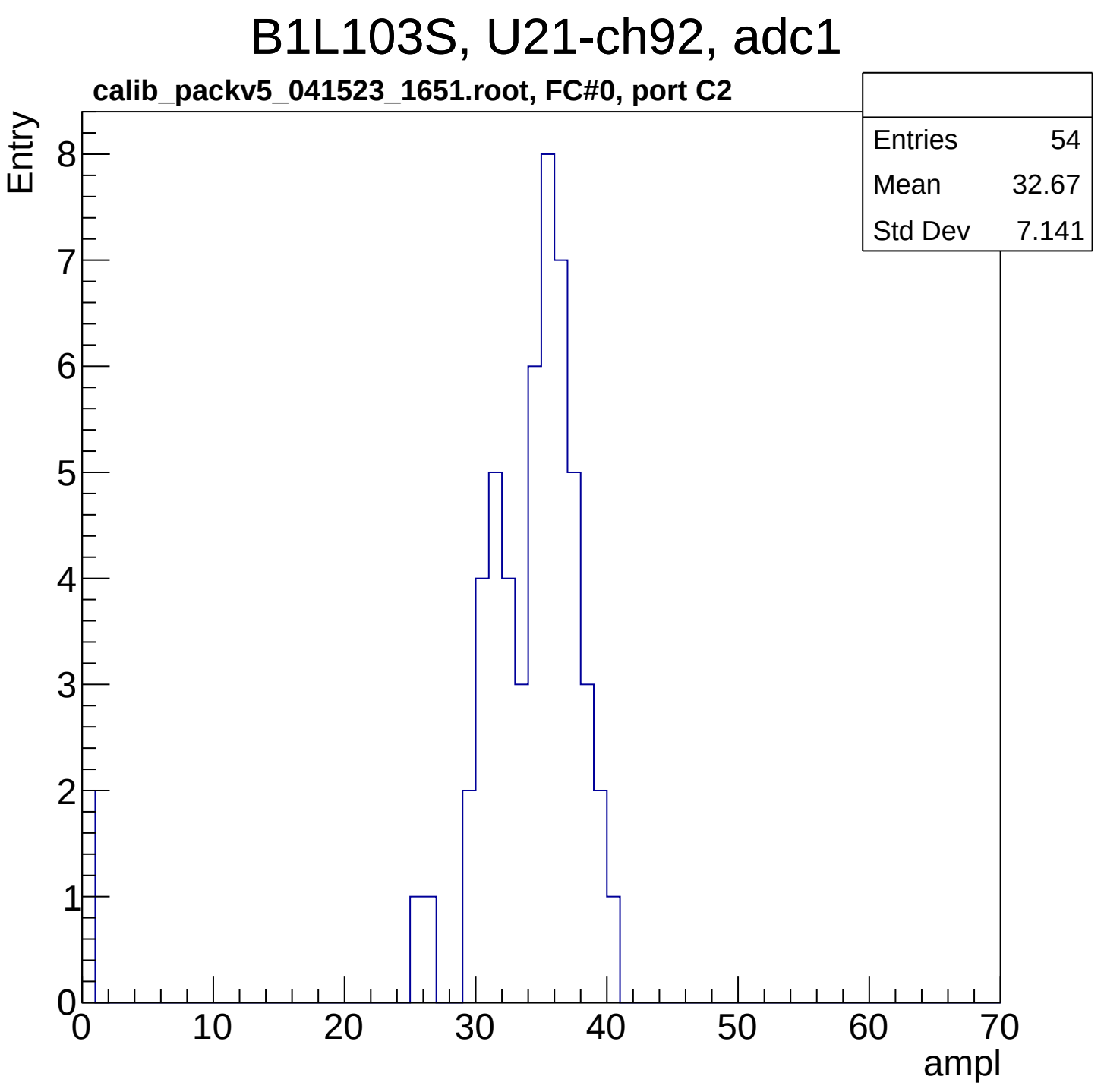
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch92, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 32.67
Std Dev 7.141
Entry
ampl
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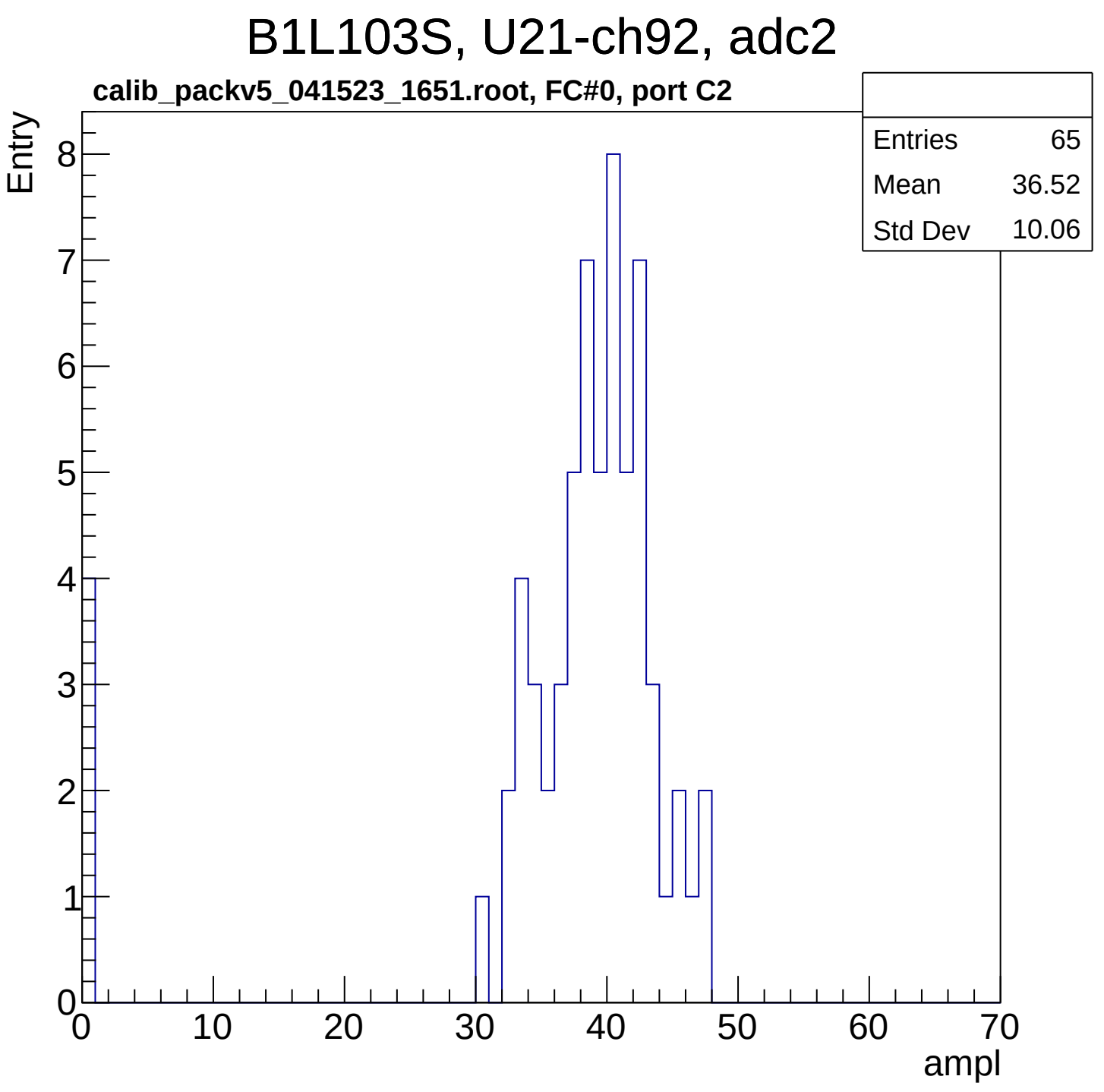
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch92, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 36.52
Std Dev 10.06
Entry
ampl
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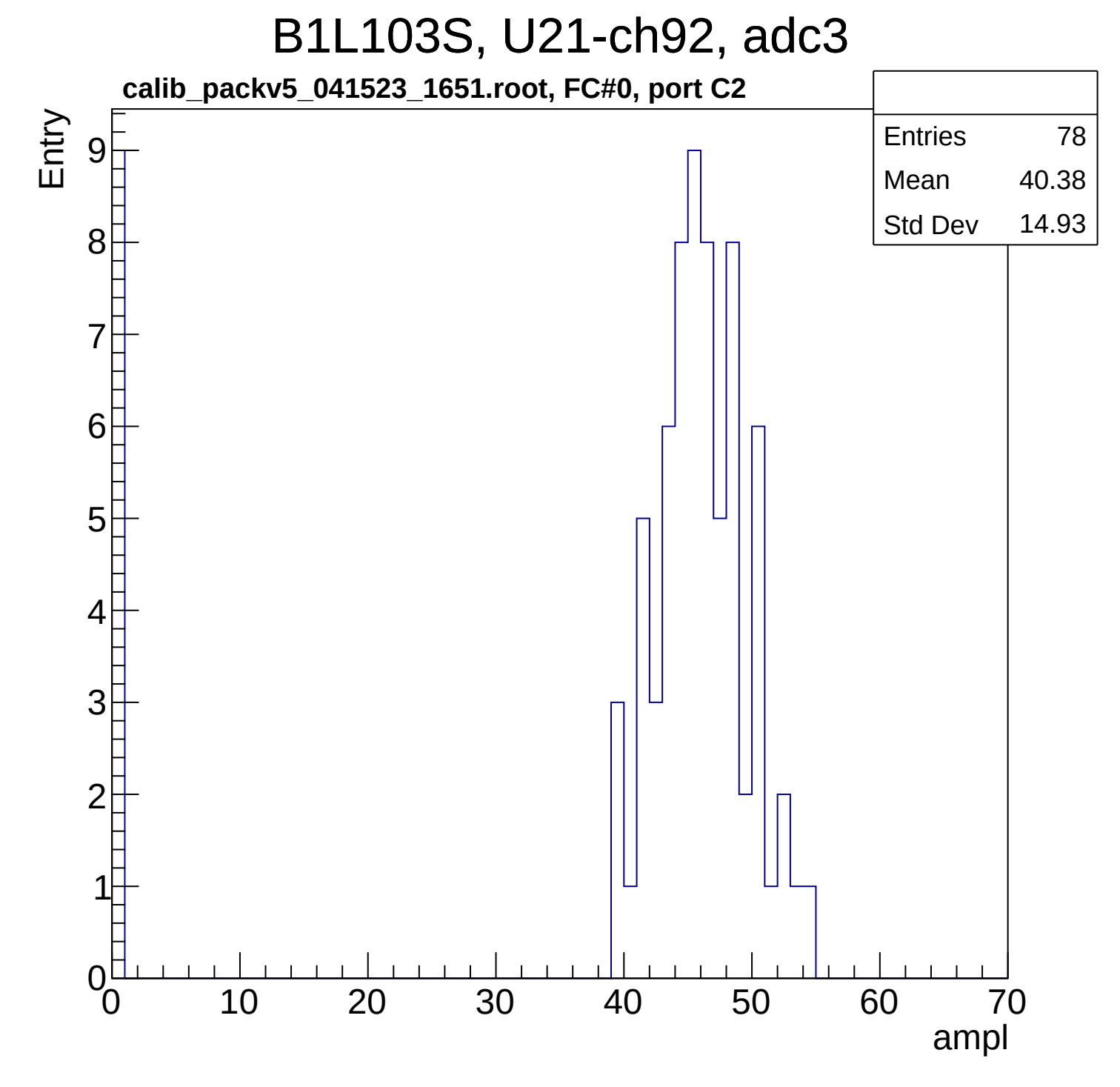
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch92, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 40.38
Std Dev 14.93
Entry
ampl
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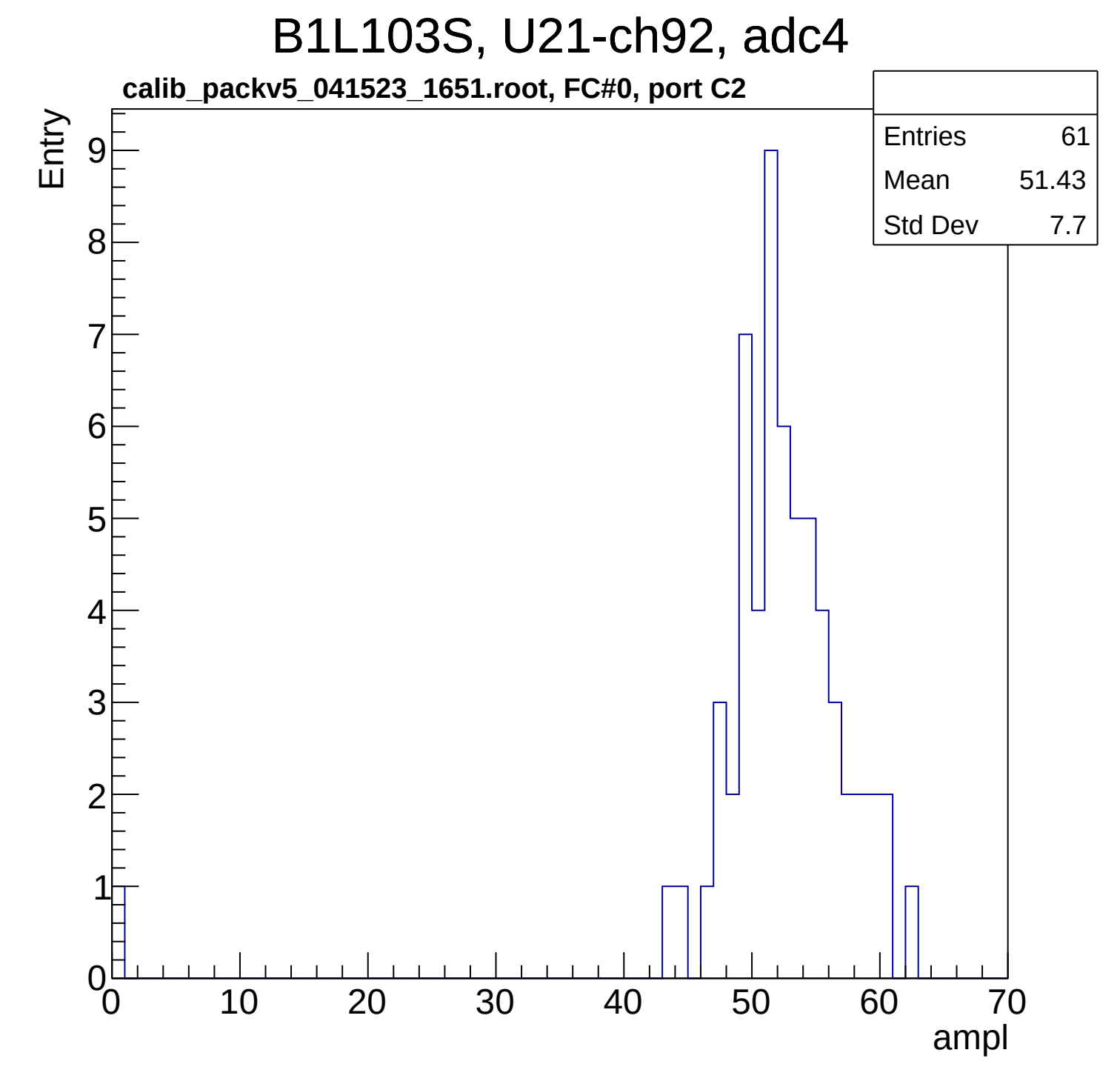
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch92, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 51.43
Std Dev 7.7
Entry
ampl
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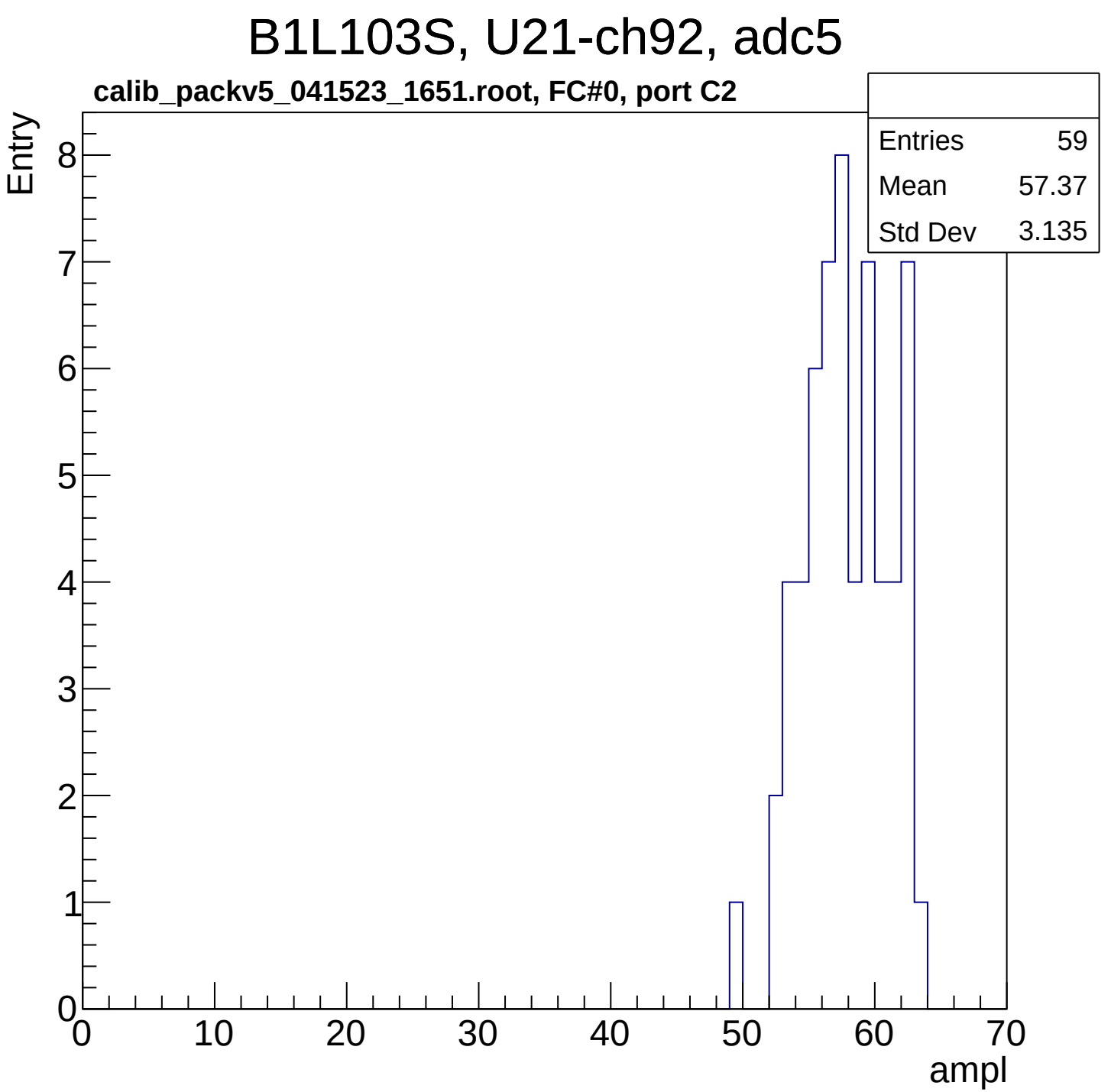
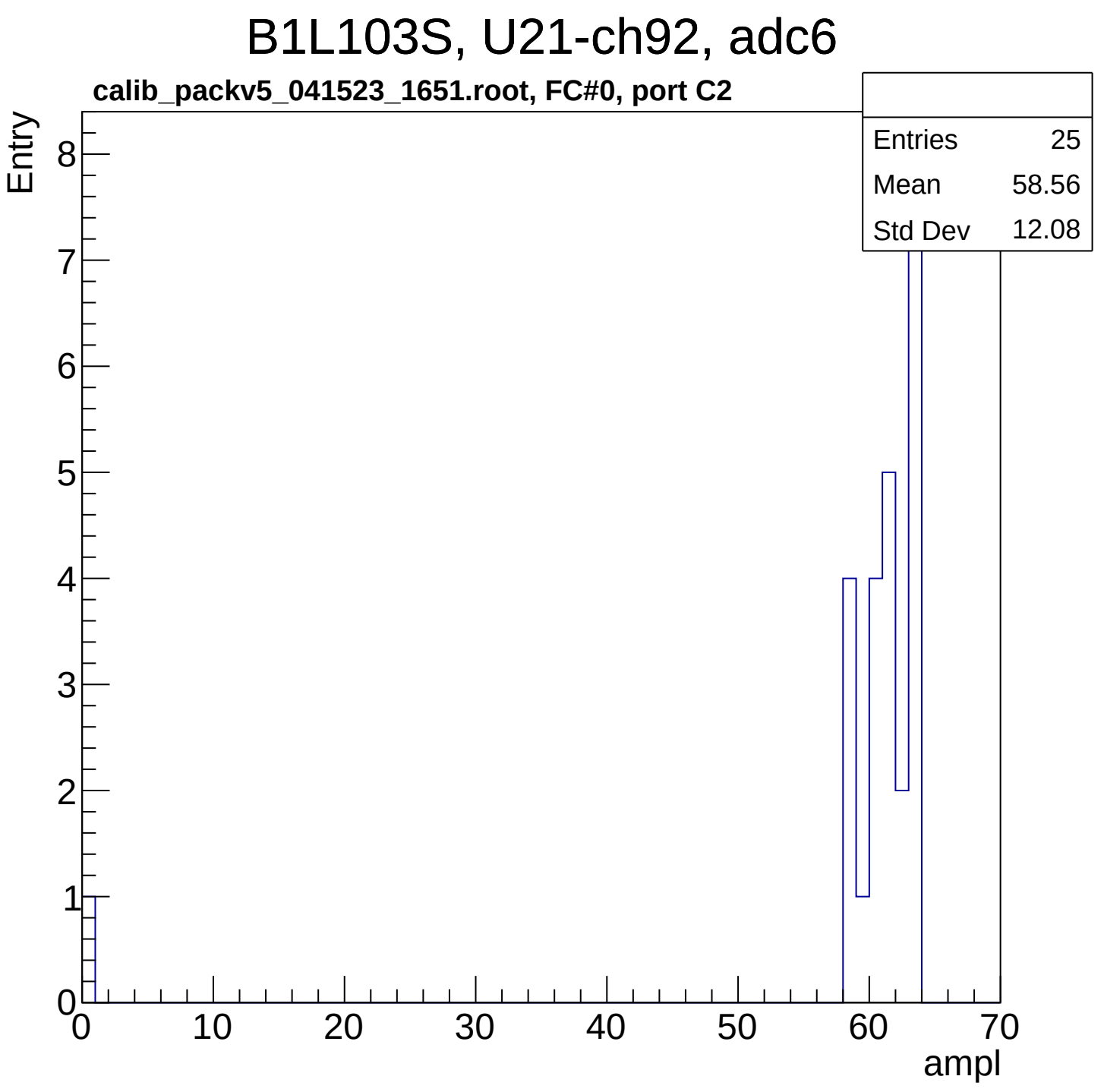
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch92, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 57.37
Std Dev 3.135
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch92, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 58.56
Std Dev 12.08
Entry
ampl
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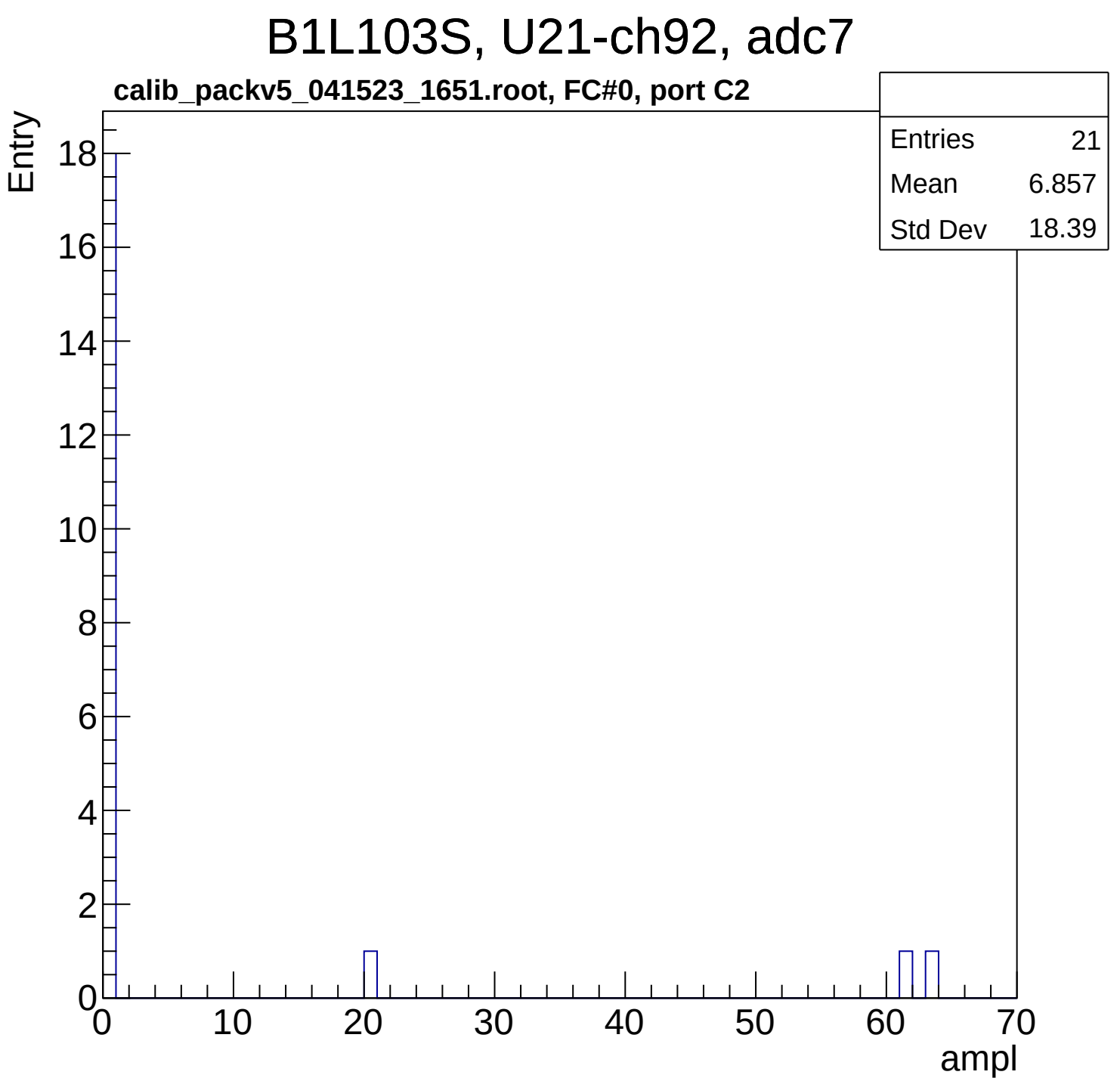
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch92, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 6.857
Std Dev 18.39
Entry
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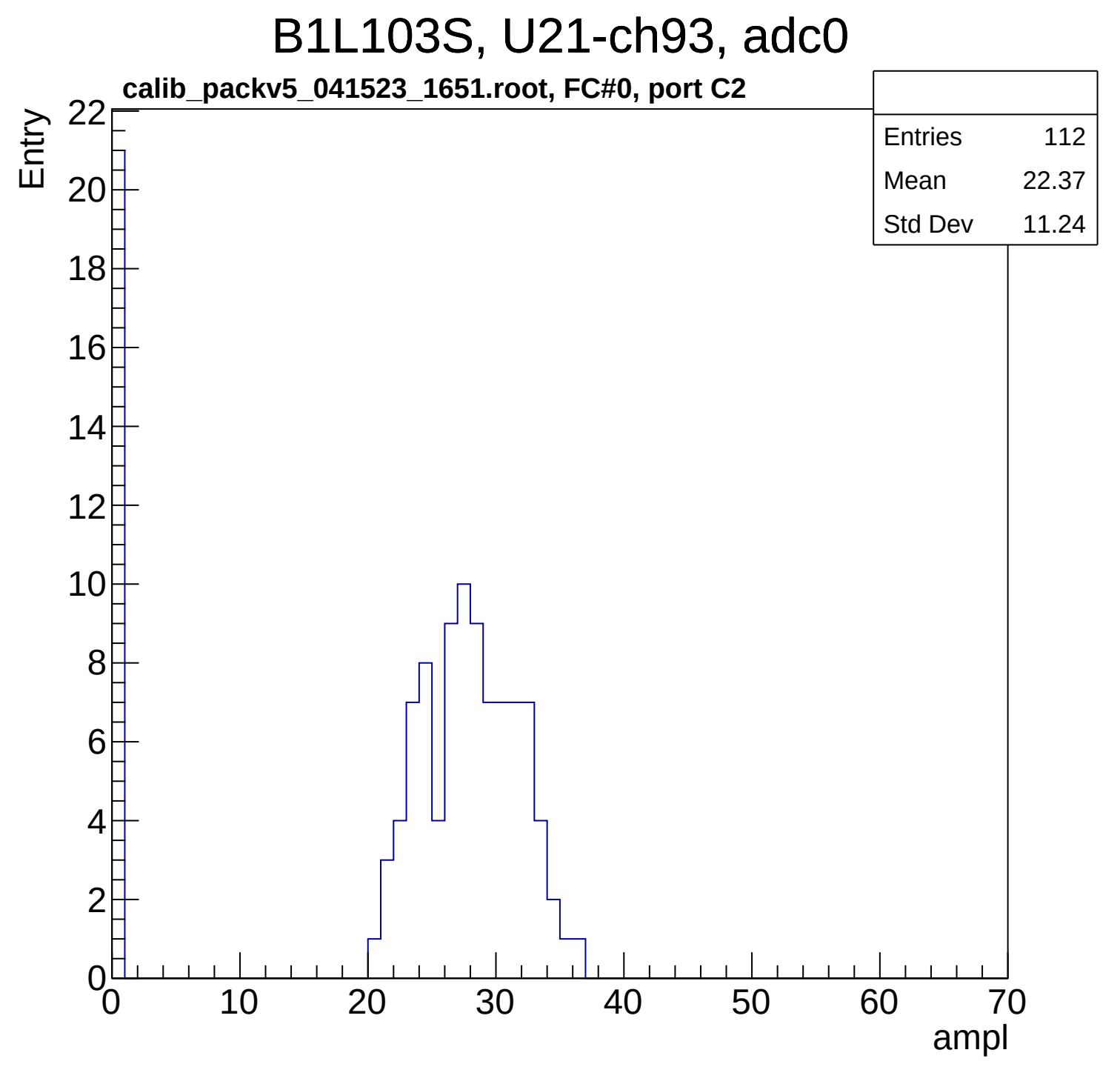
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch93, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 112
Mean 22.37
Std Dev 11.24
Entry
ampl
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2
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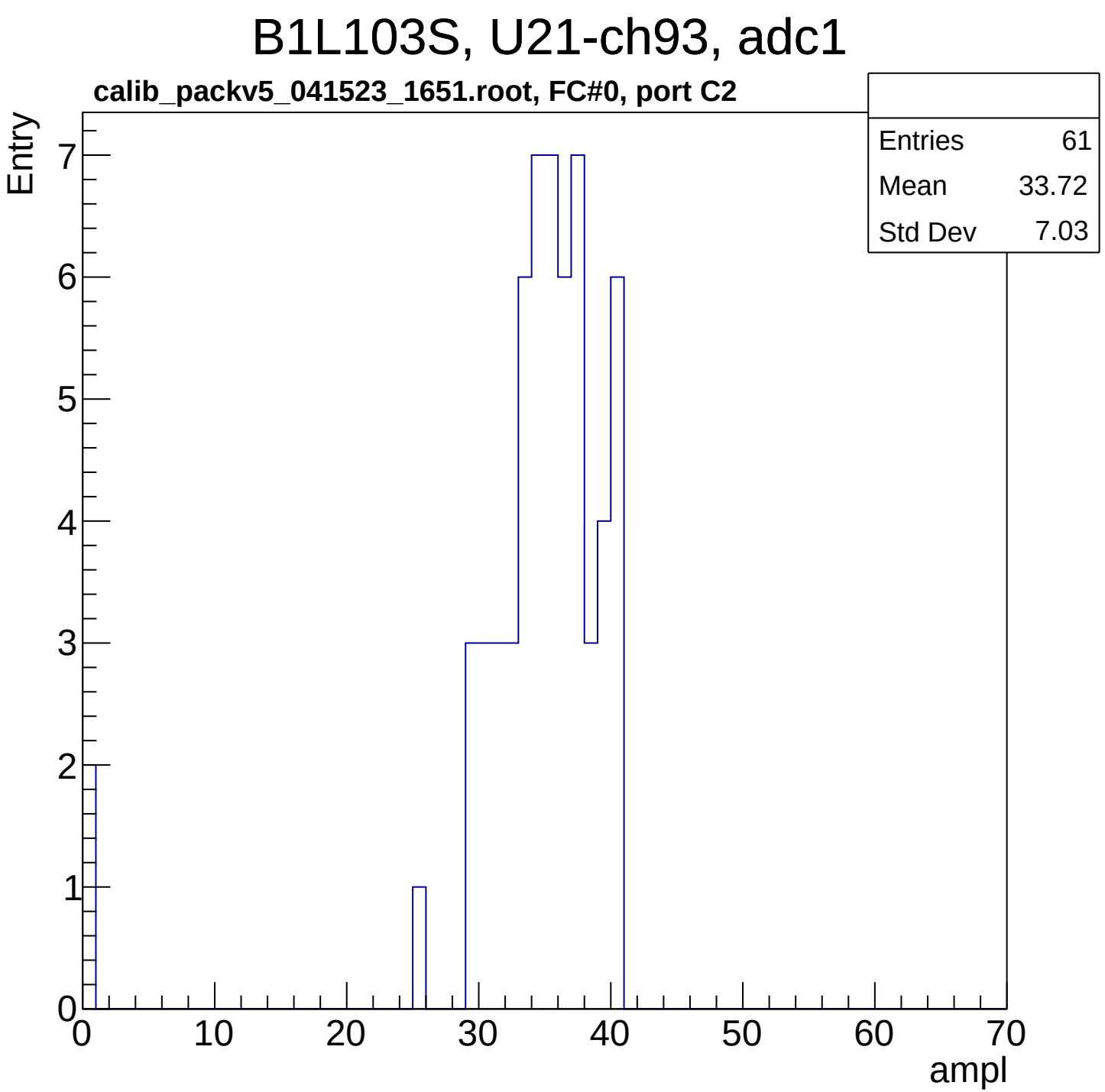
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70


B1L103S, U21-ch93, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 33.72
Std Dev 7.03
Entry
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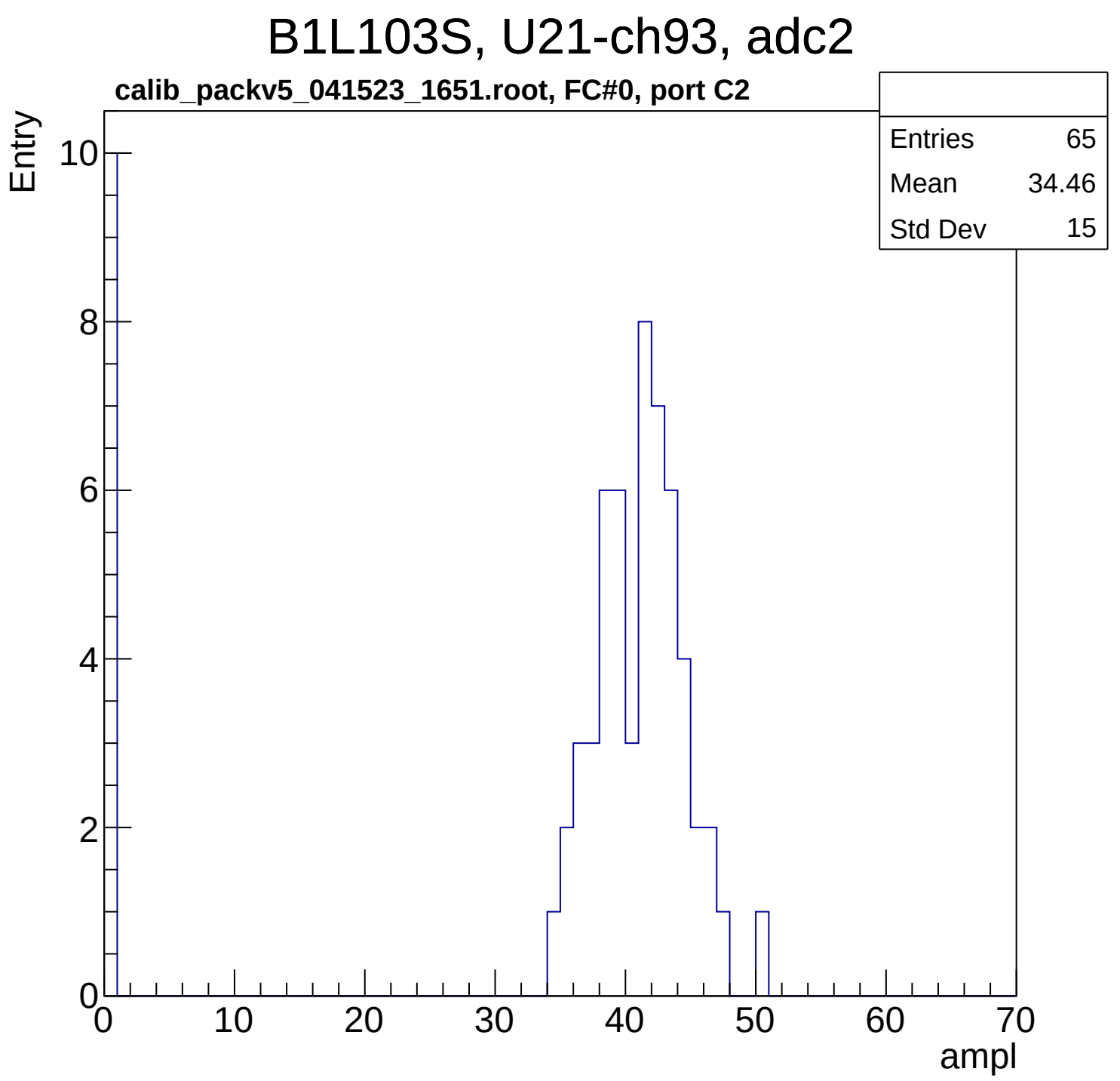
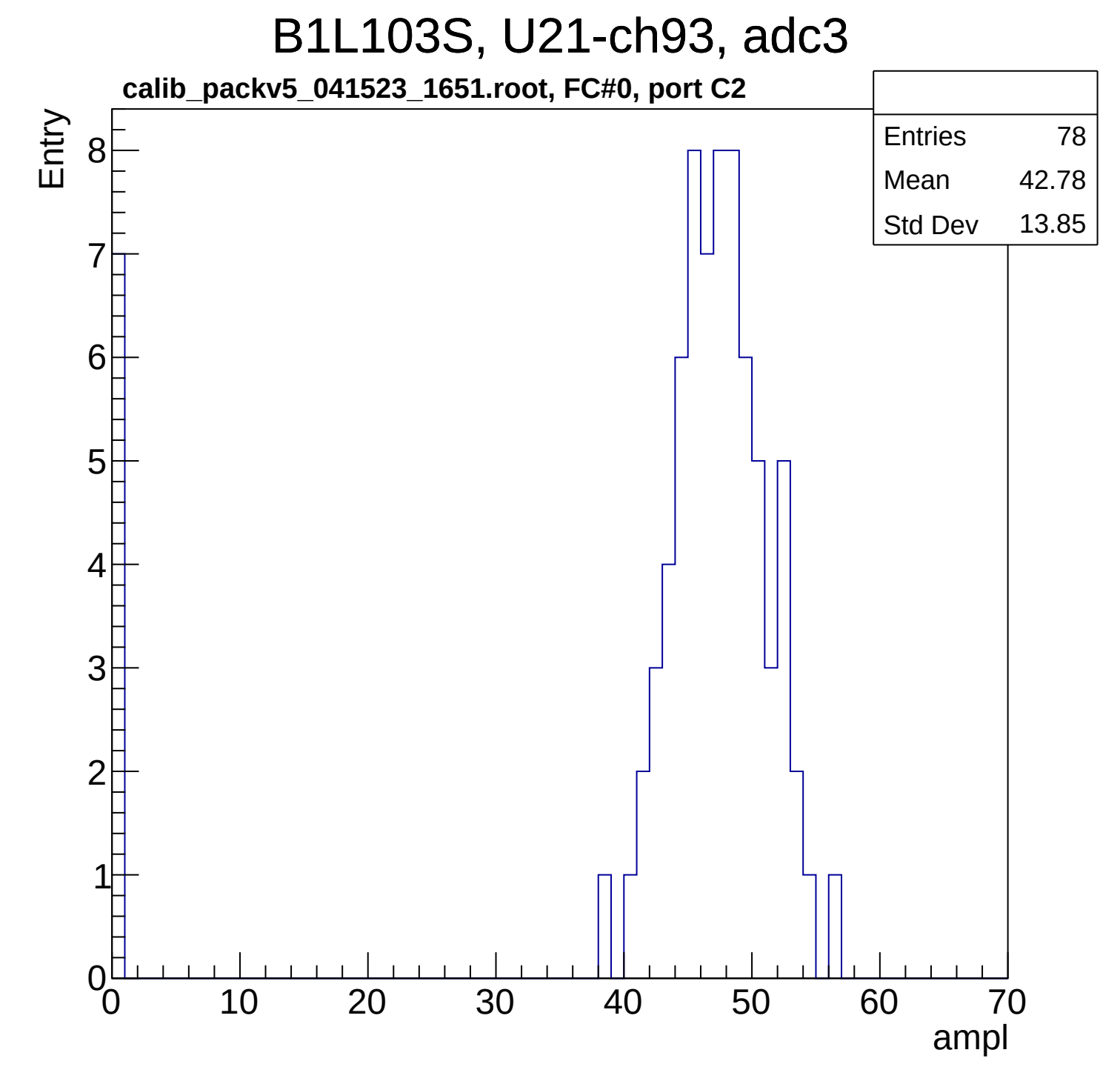
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch93, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 34.46
Std Dev 15
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U21-ch93, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 42.78
Std Dev 13.85
Entry
ampl
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1
2
3
4
5
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7
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0
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40
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60
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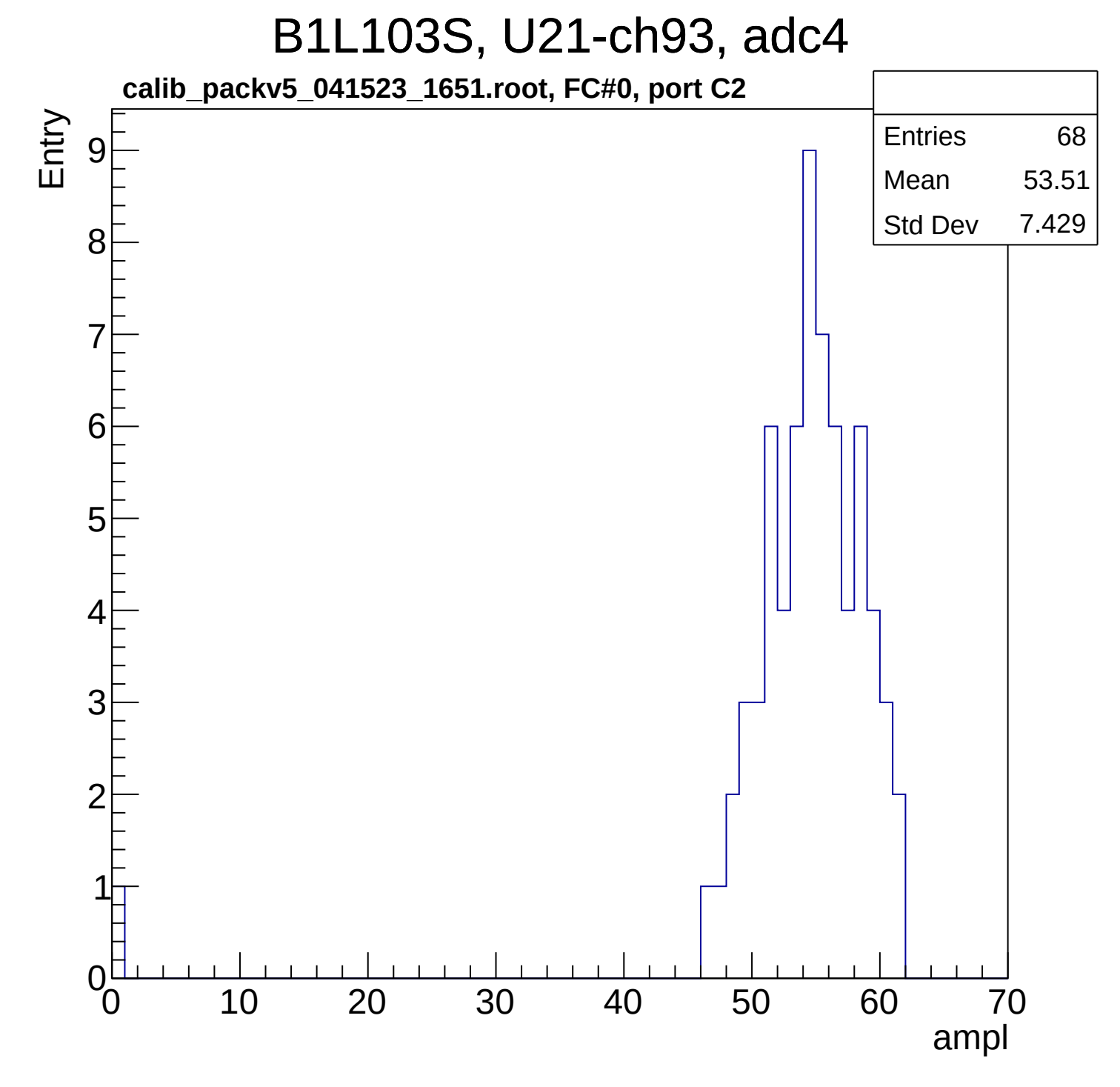
B1L103S, U21-ch93, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 53.51
Std Dev 7.429
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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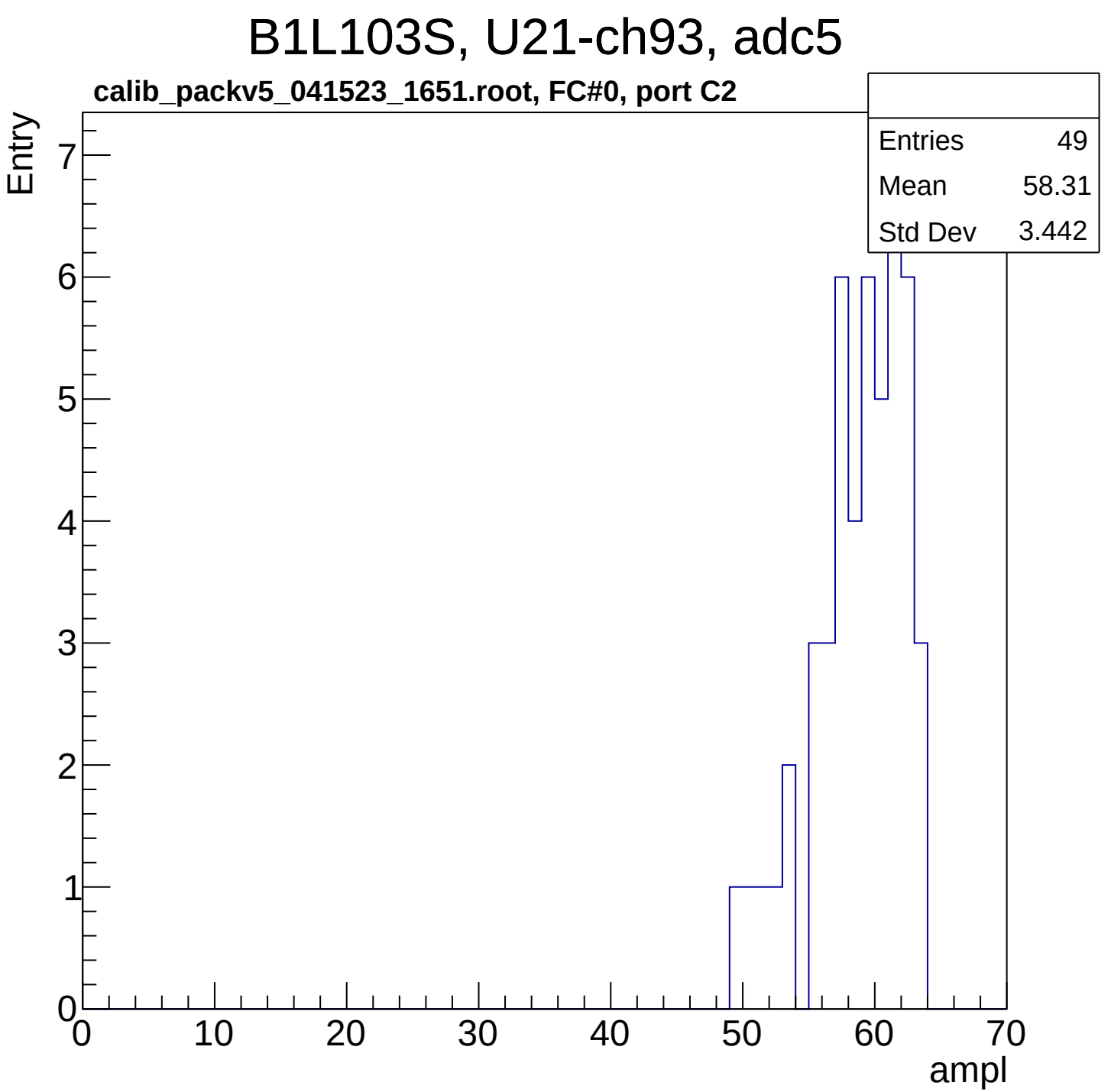
B1L103S, U21-ch93, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 58.31
Std Dev 3.442
Entry
ampl
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2
3
4
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6
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0
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40
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60
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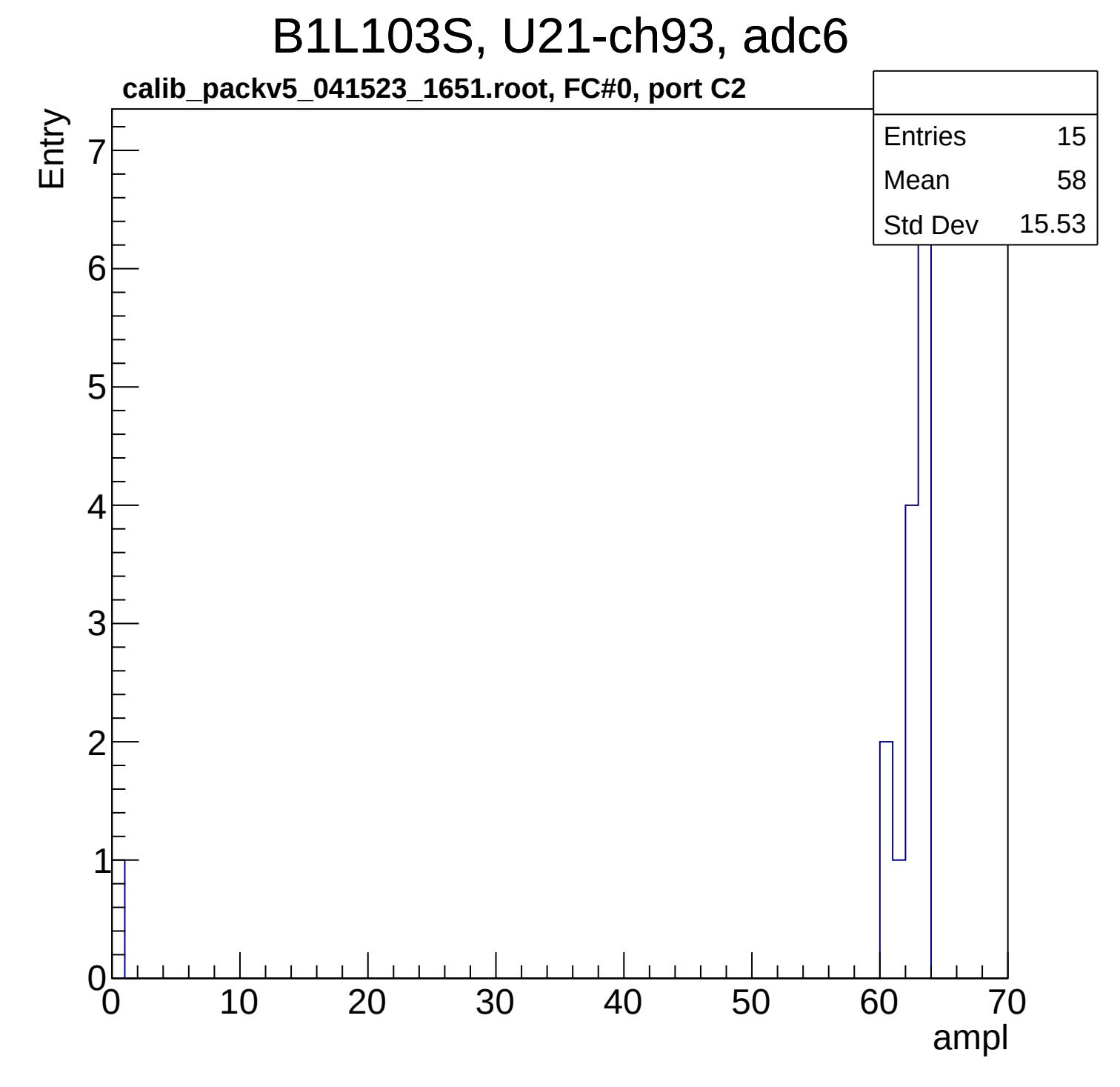
B1L103S, U21-ch93, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 58
Std Dev 15.53
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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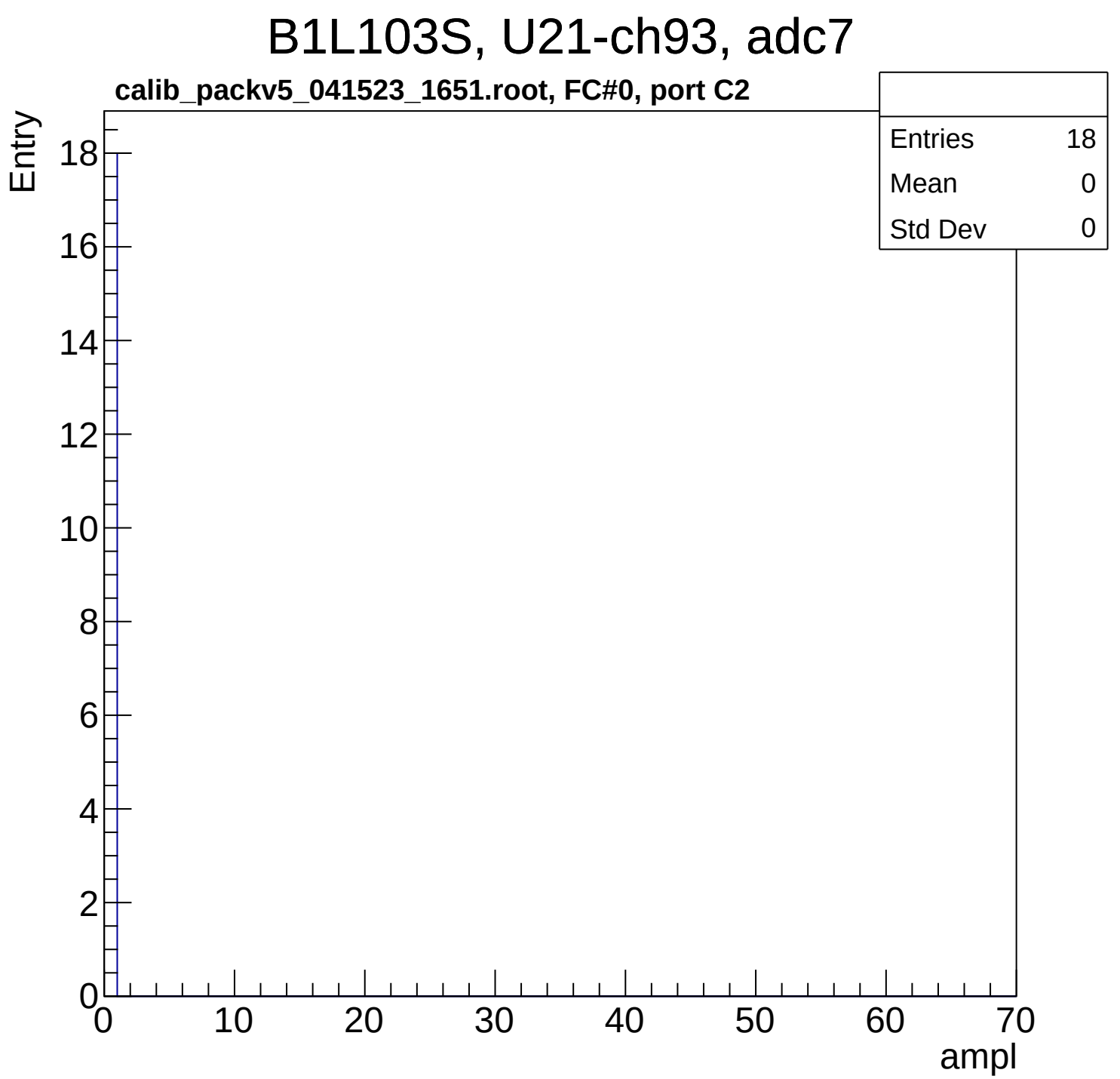
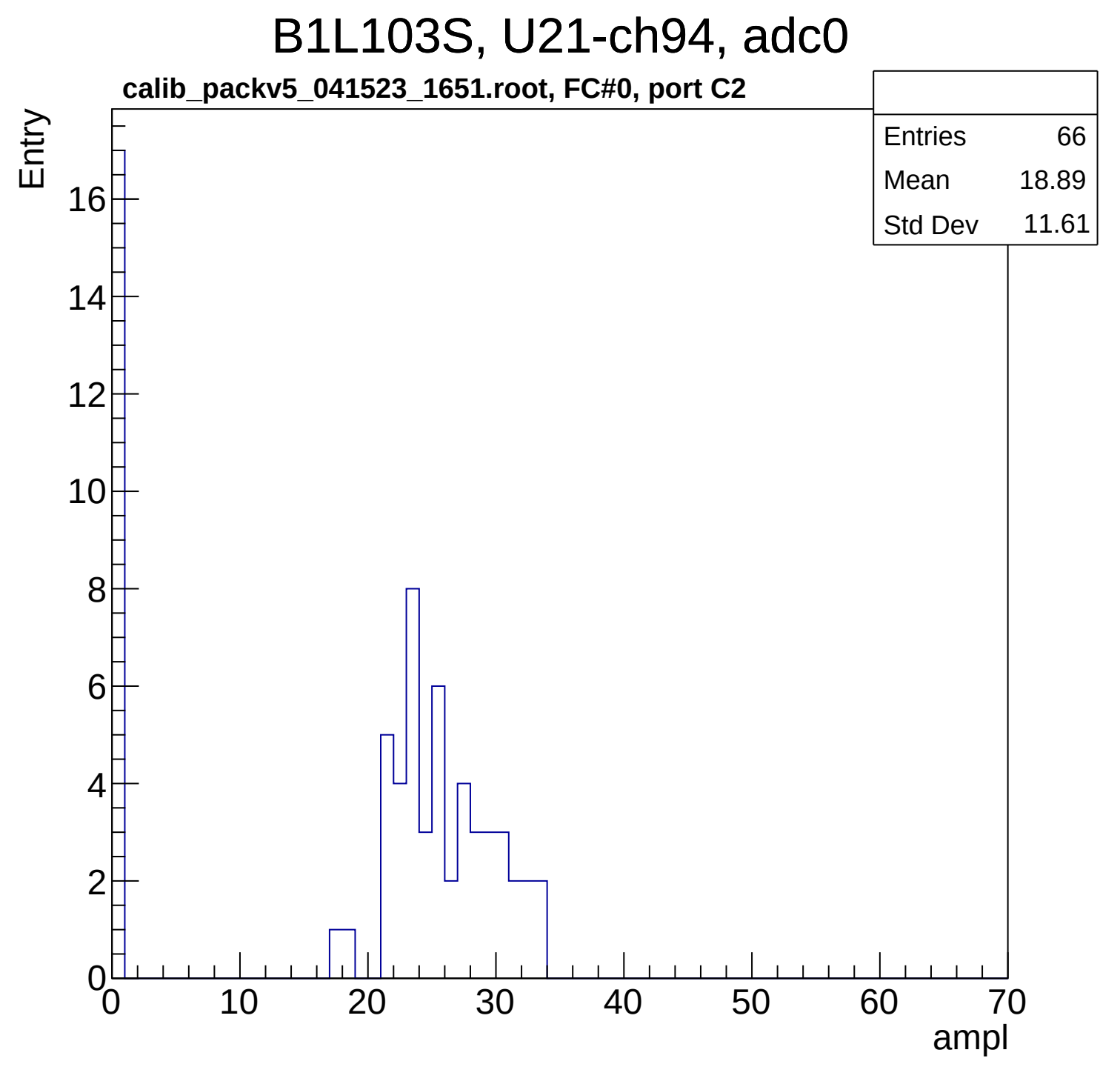
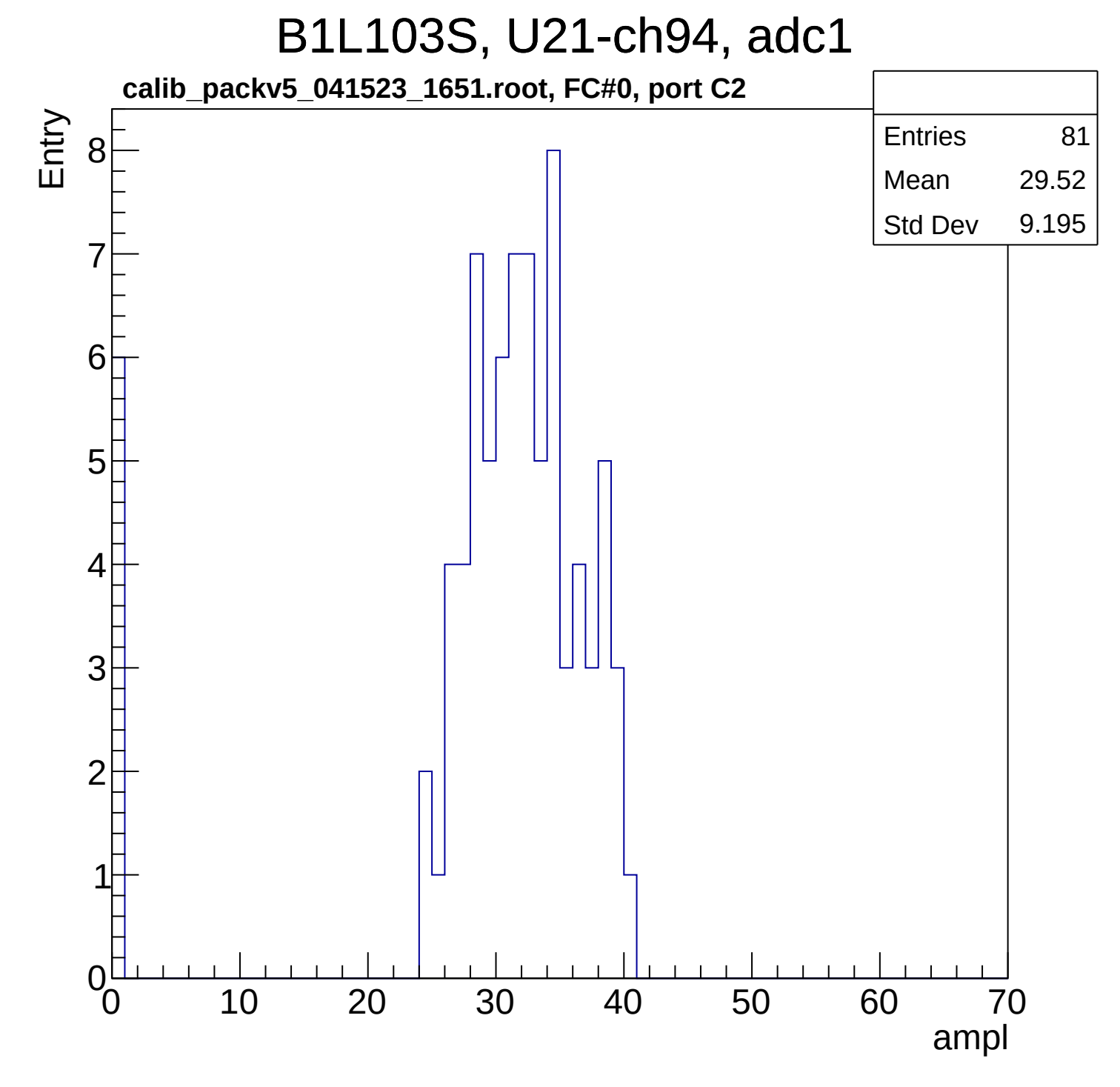
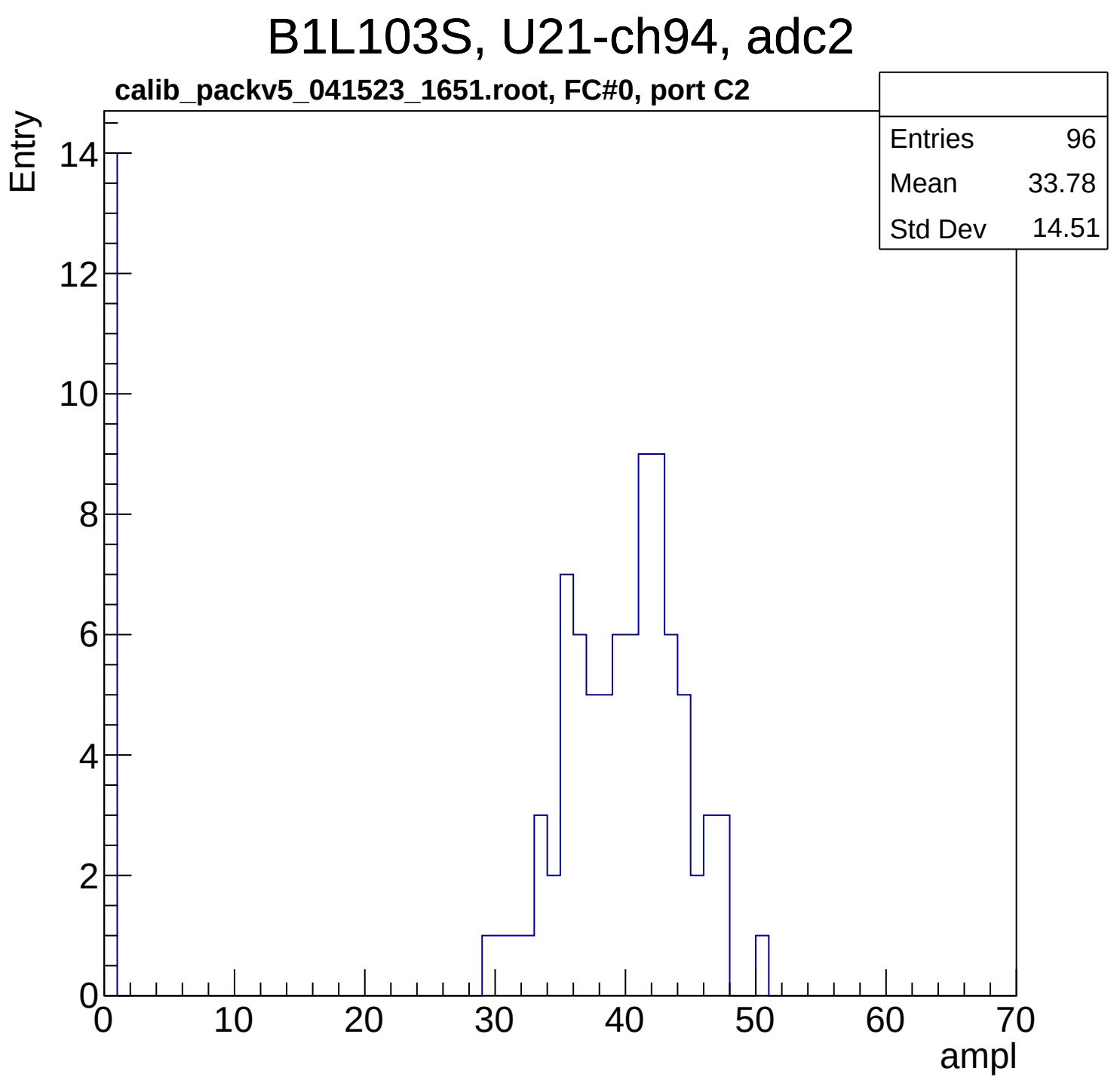
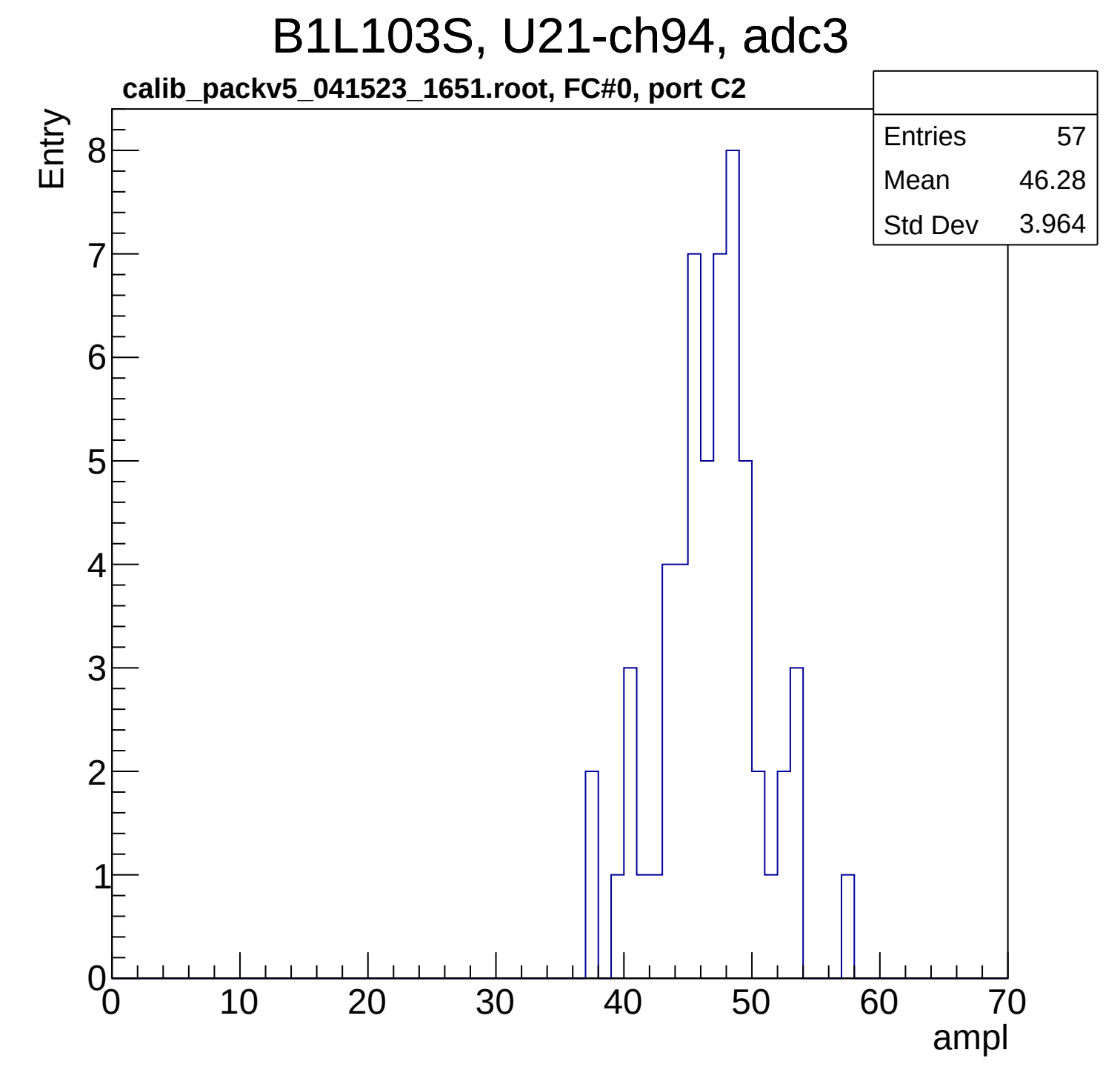
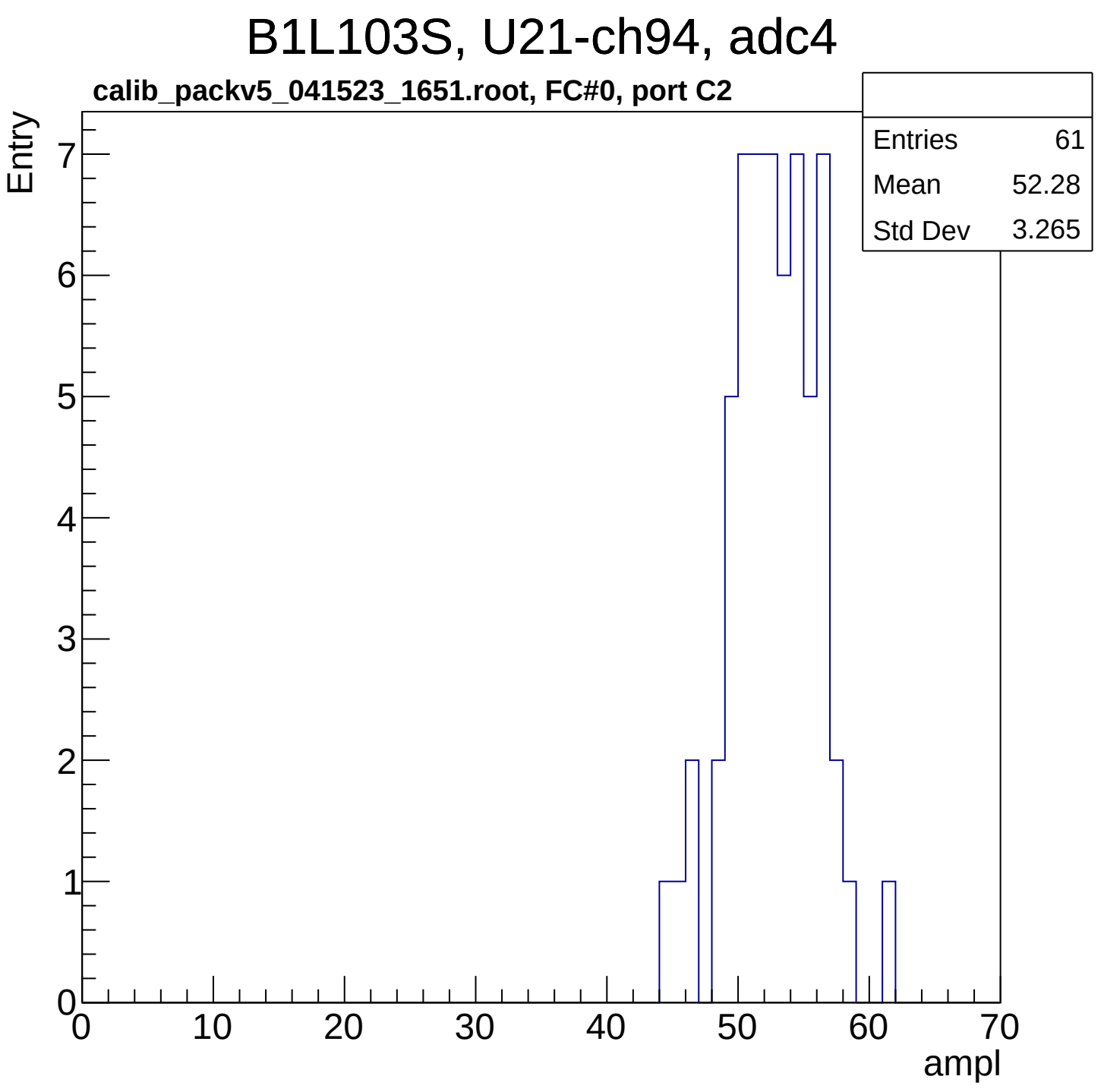

B1L103S, U21-ch93, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

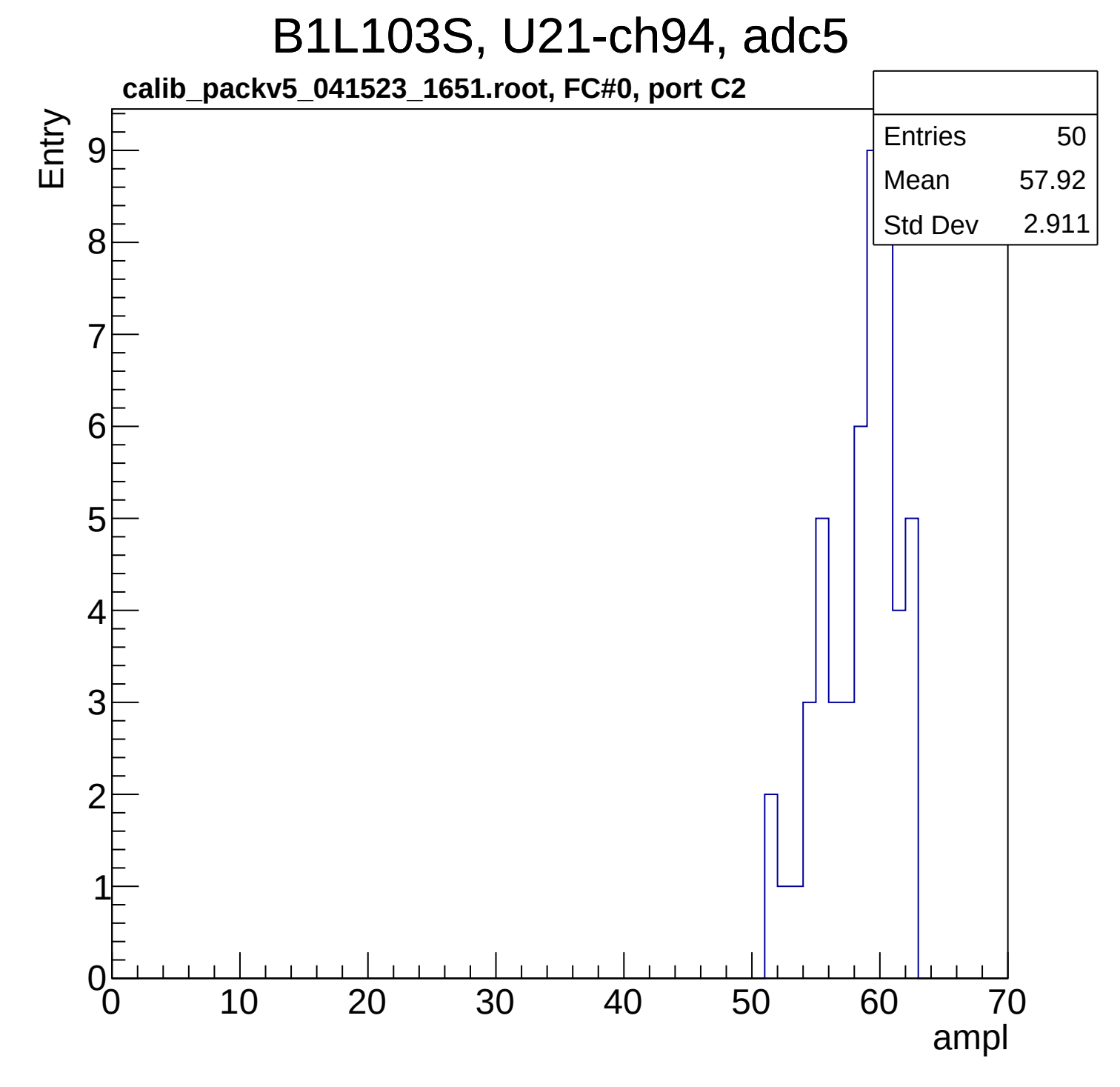

B1L103S, U21-ch94, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 18.89
Std Dev 11.61
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

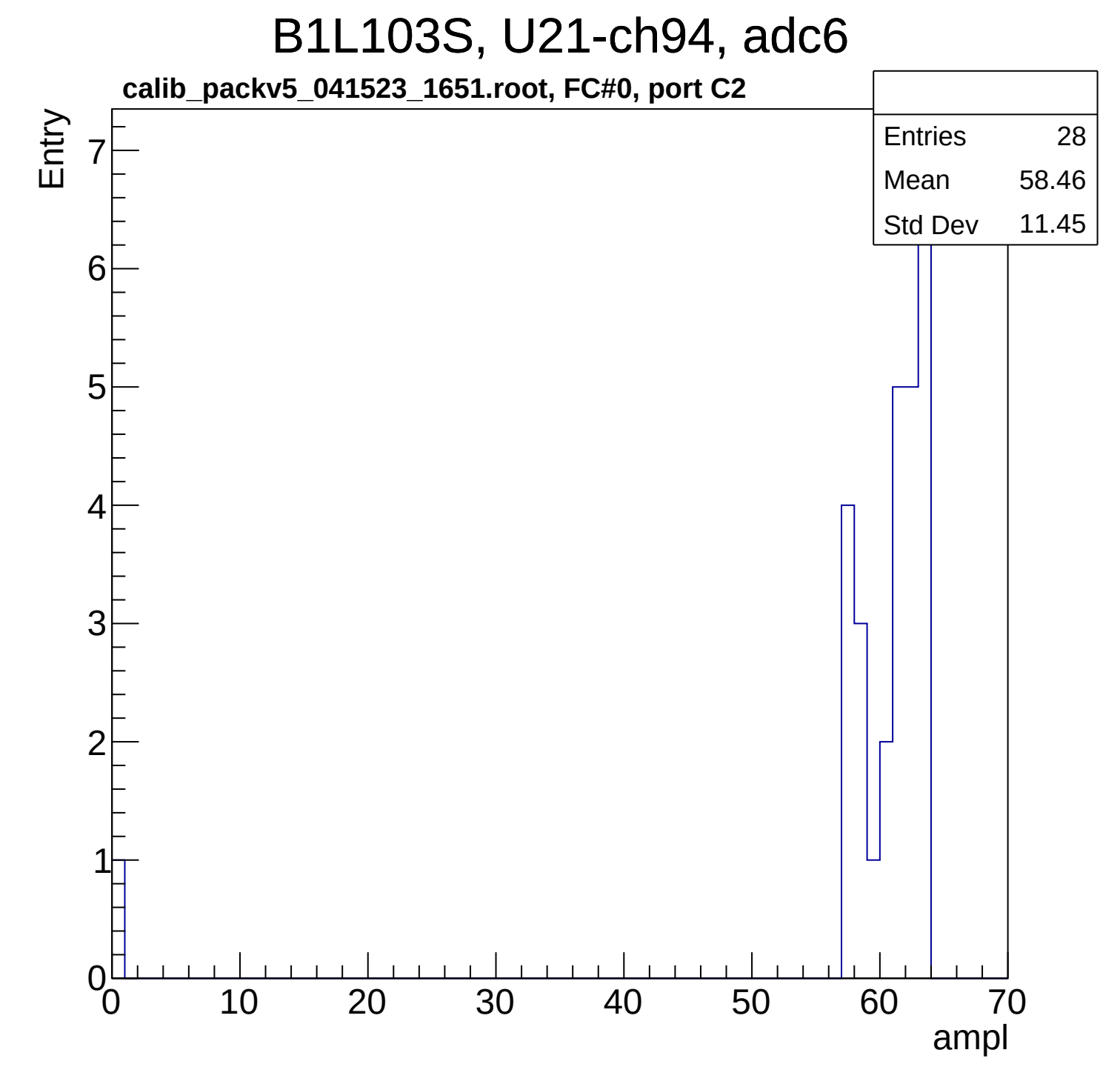

B1L103S, U21-ch94, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 29.52
Std Dev 9.195
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

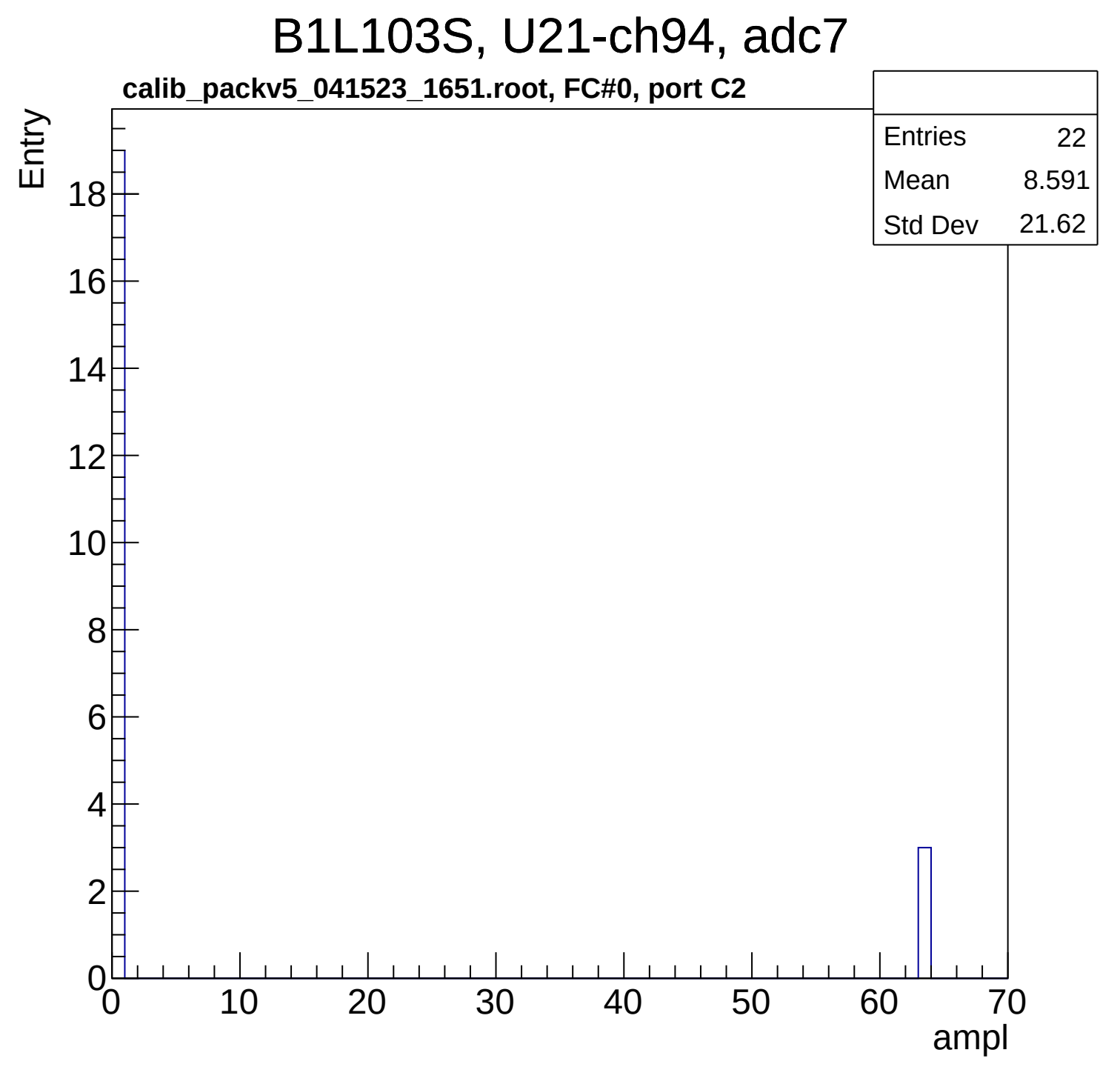

B1L103S, U21-ch94, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 96
Mean 33.78
Std Dev 14.51
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

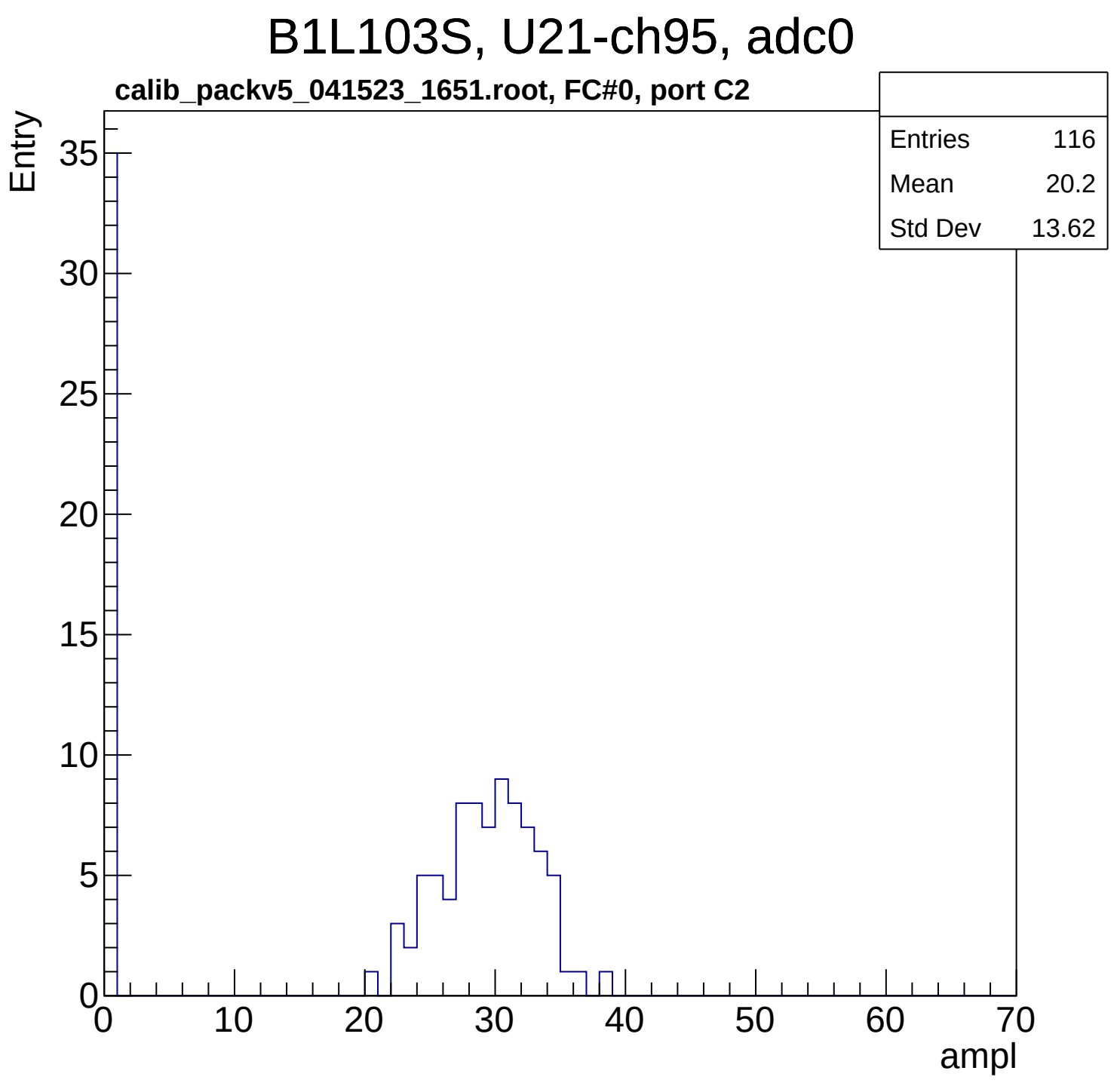

B1L103S, U21-ch94, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 46.28
Std Dev 3.964
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

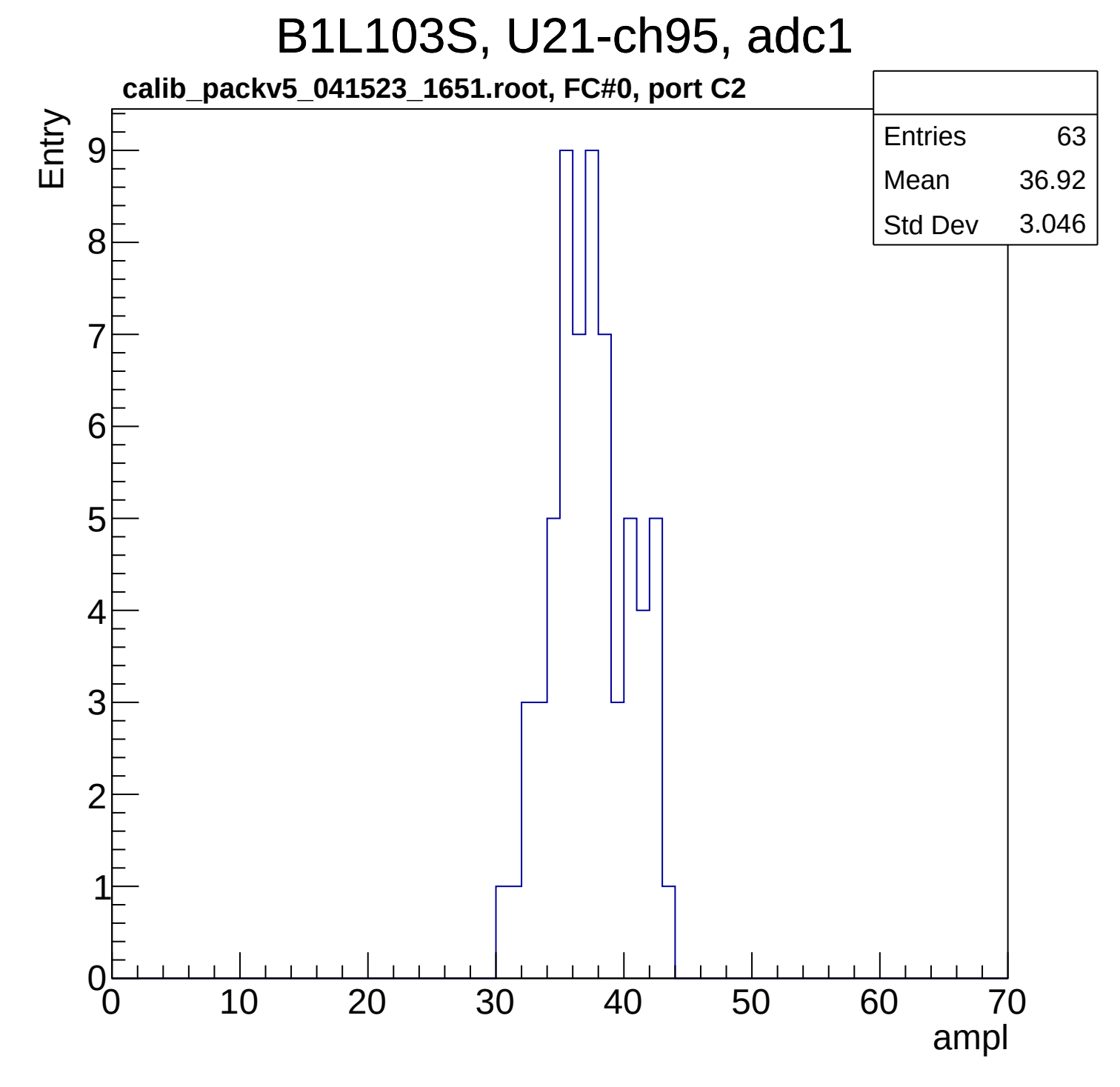

B1L103S, U21-ch94, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 52.28
Std Dev 3.265
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

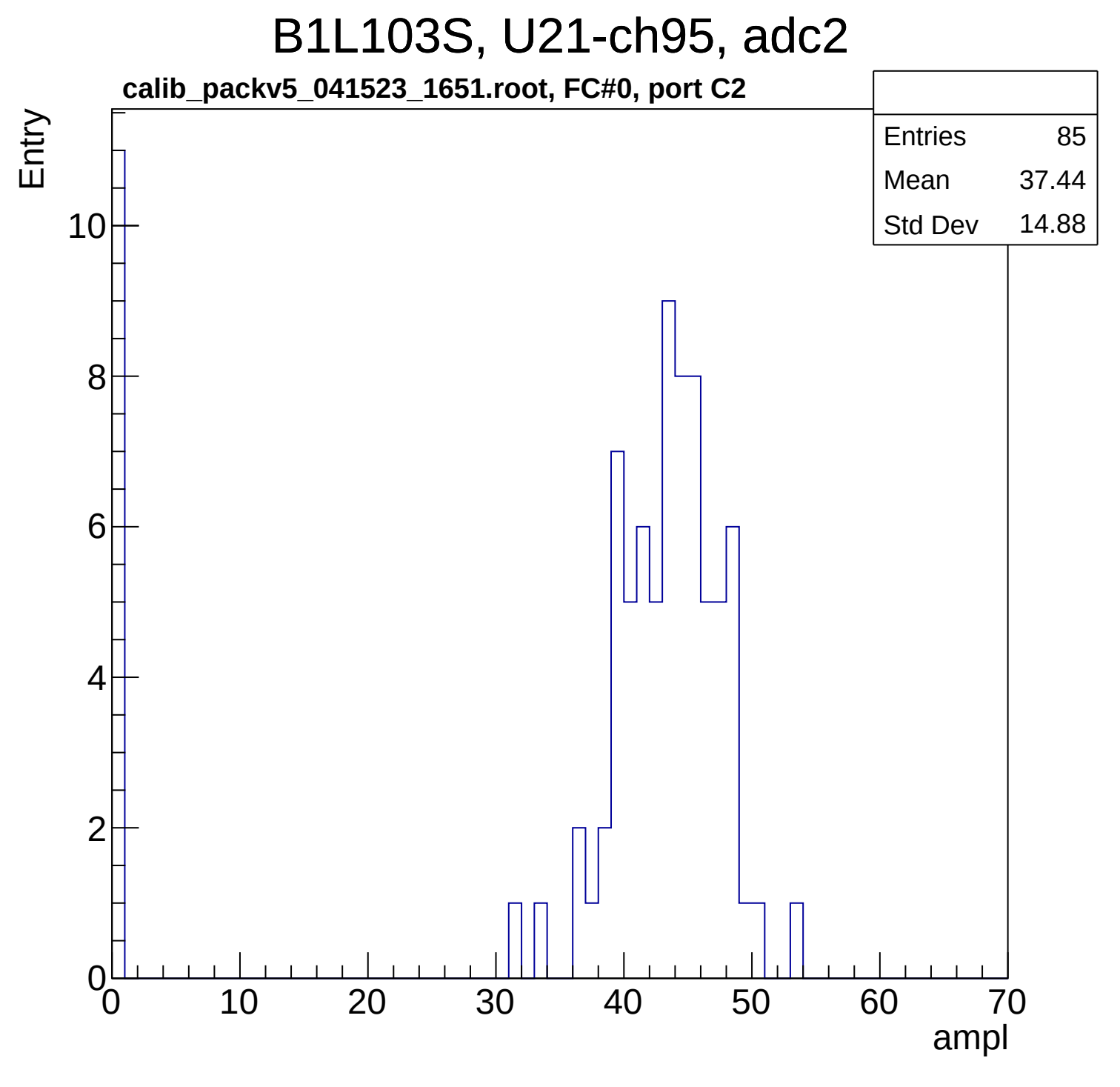

B1L103S, U21-ch94, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 57.92
Std Dev 2.911
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

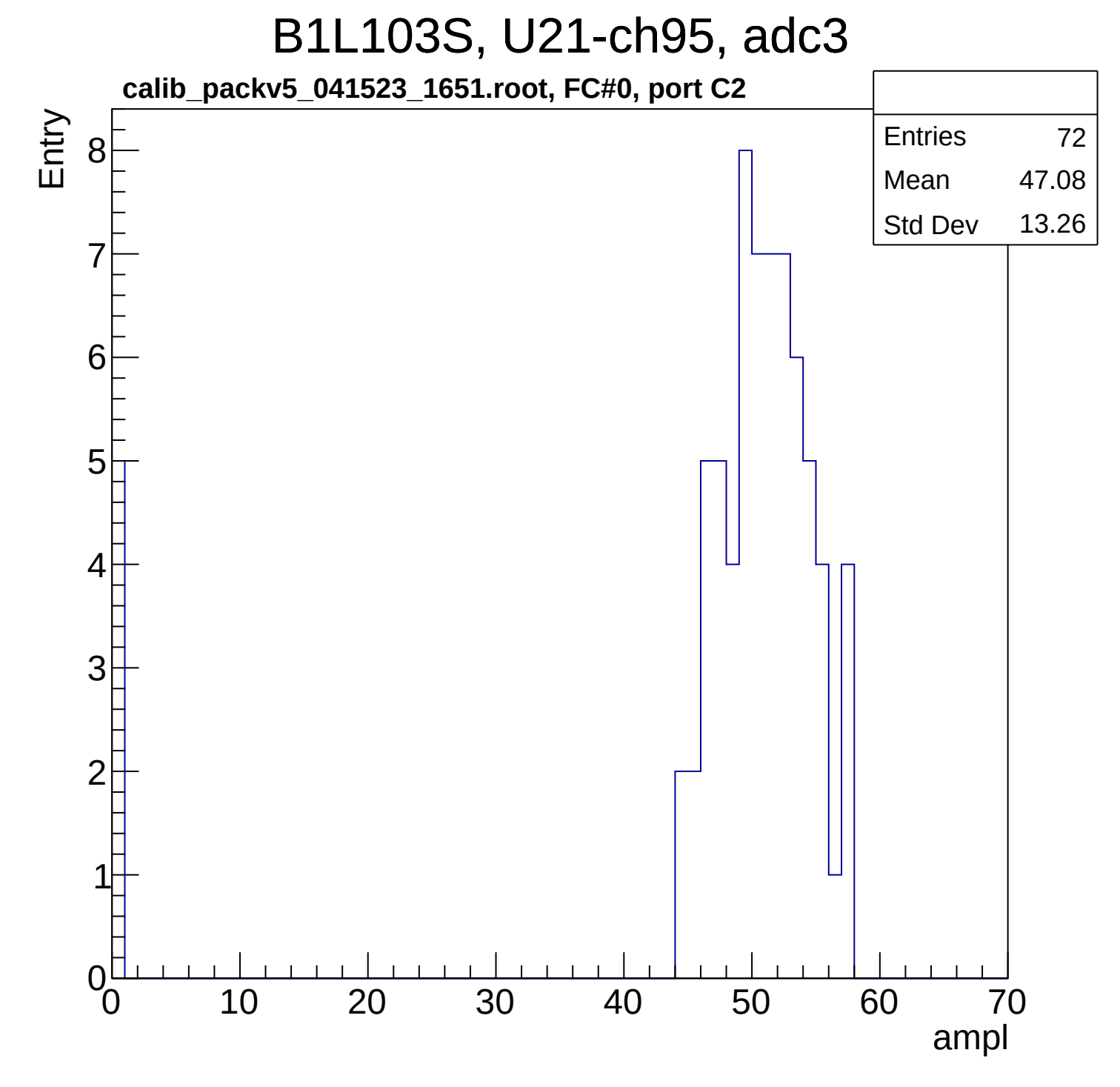

B1L103S, U21-ch94, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 58.46
Std Dev 11.45
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

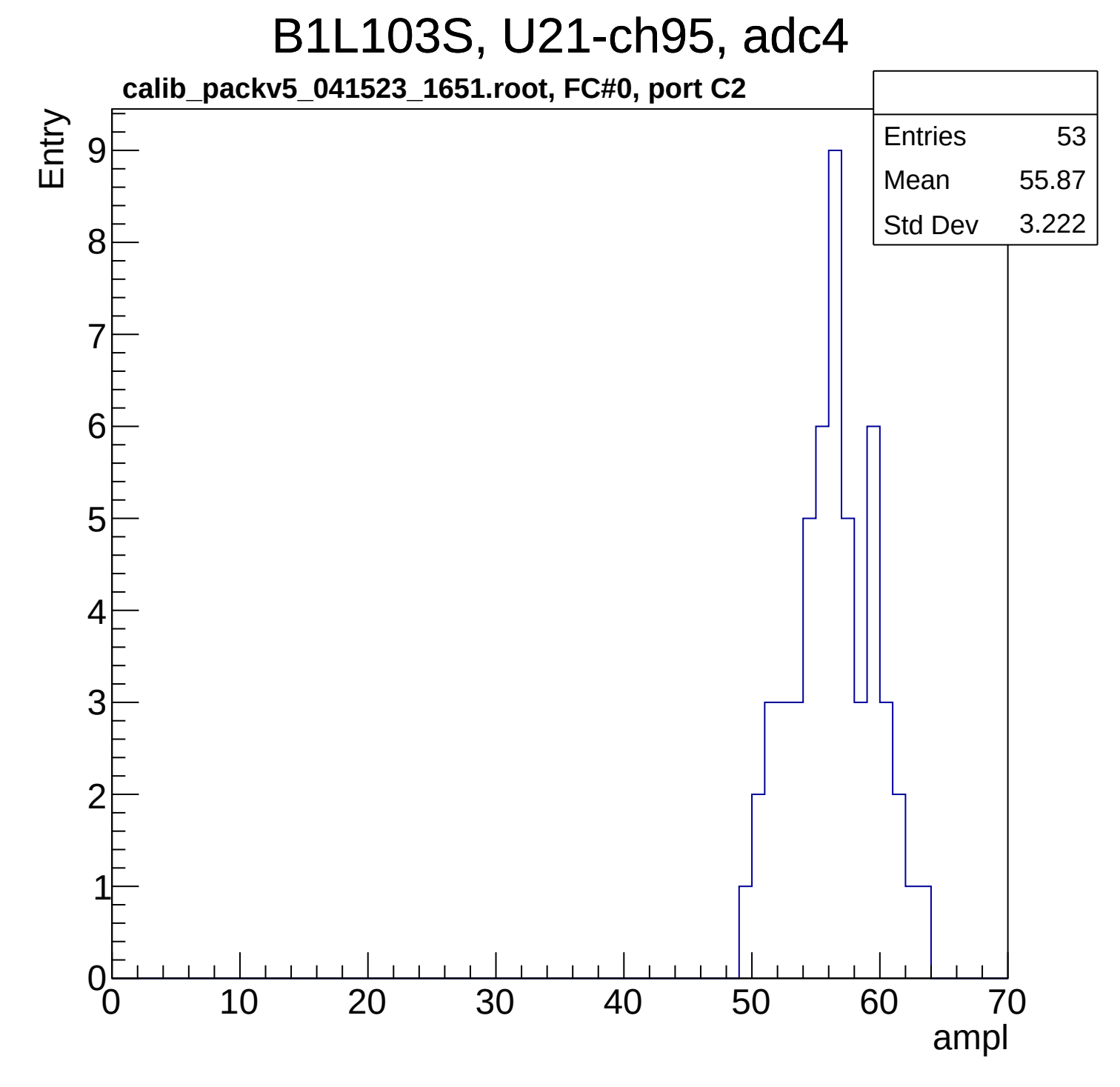

B1L103S, U21-ch94, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.591
Std Dev 21.62
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch95, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 116
Mean 20.2
Std Dev 13.62
Entry
0
5
10
15
20
25
30
35
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch95, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 36.92
Std Dev 3.046
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch95, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 37.44
Std Dev 14.88
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch95, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 47.08
Std Dev 13.26
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch95, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 55.87
Std Dev 3.222
Entry
ampl
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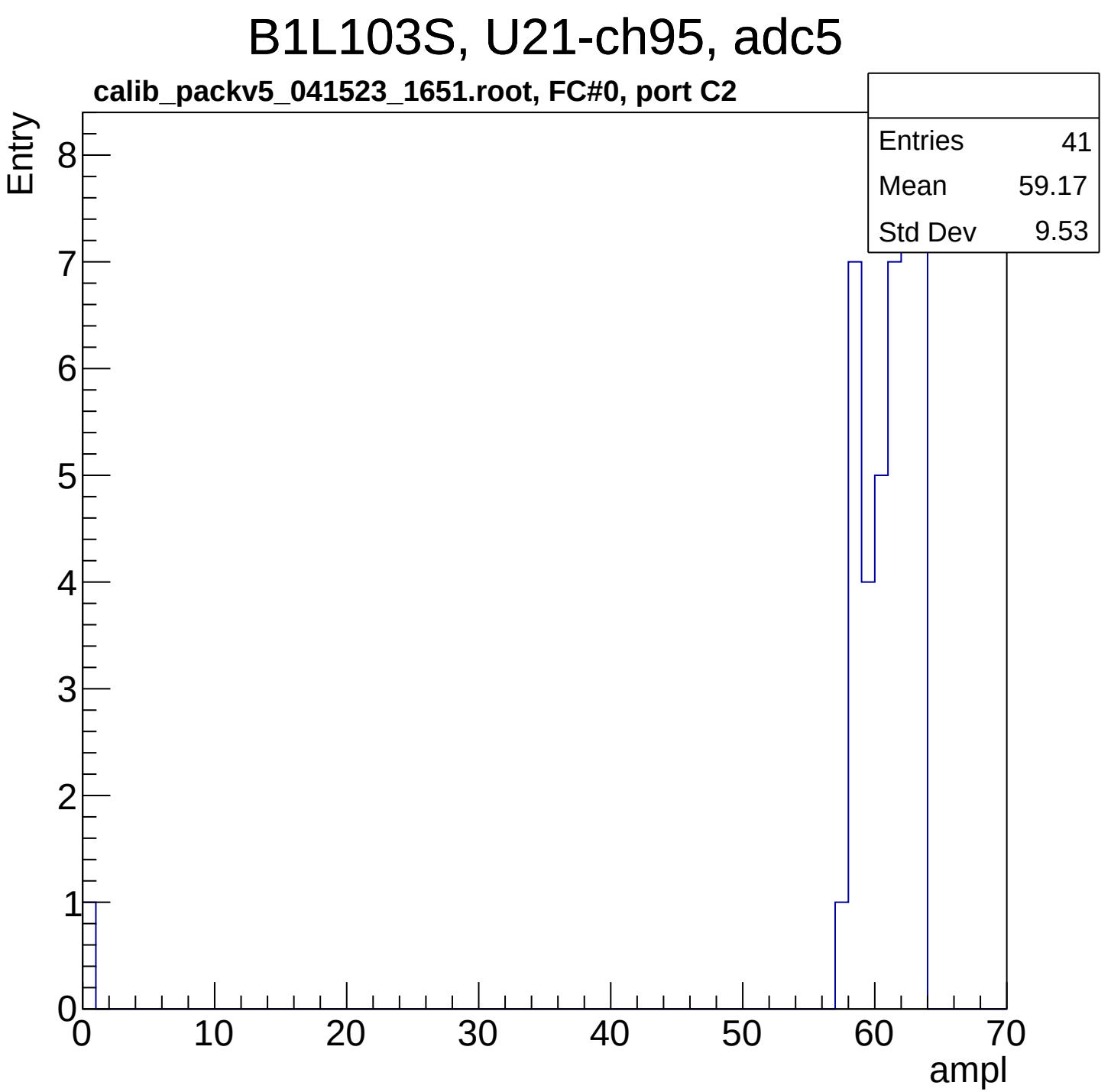
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch95, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 59.17
Std Dev 9.53
Entry
ampl
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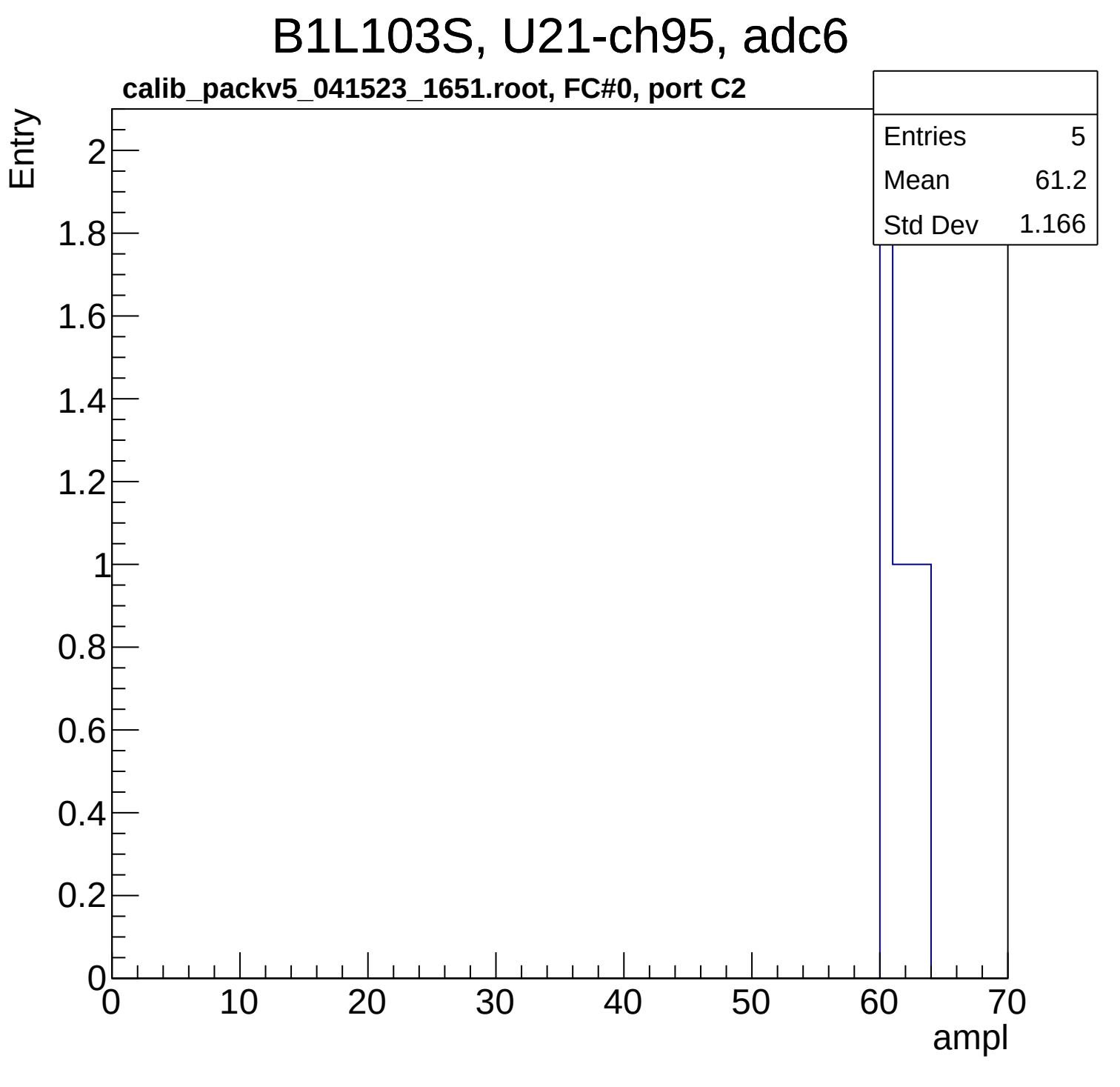
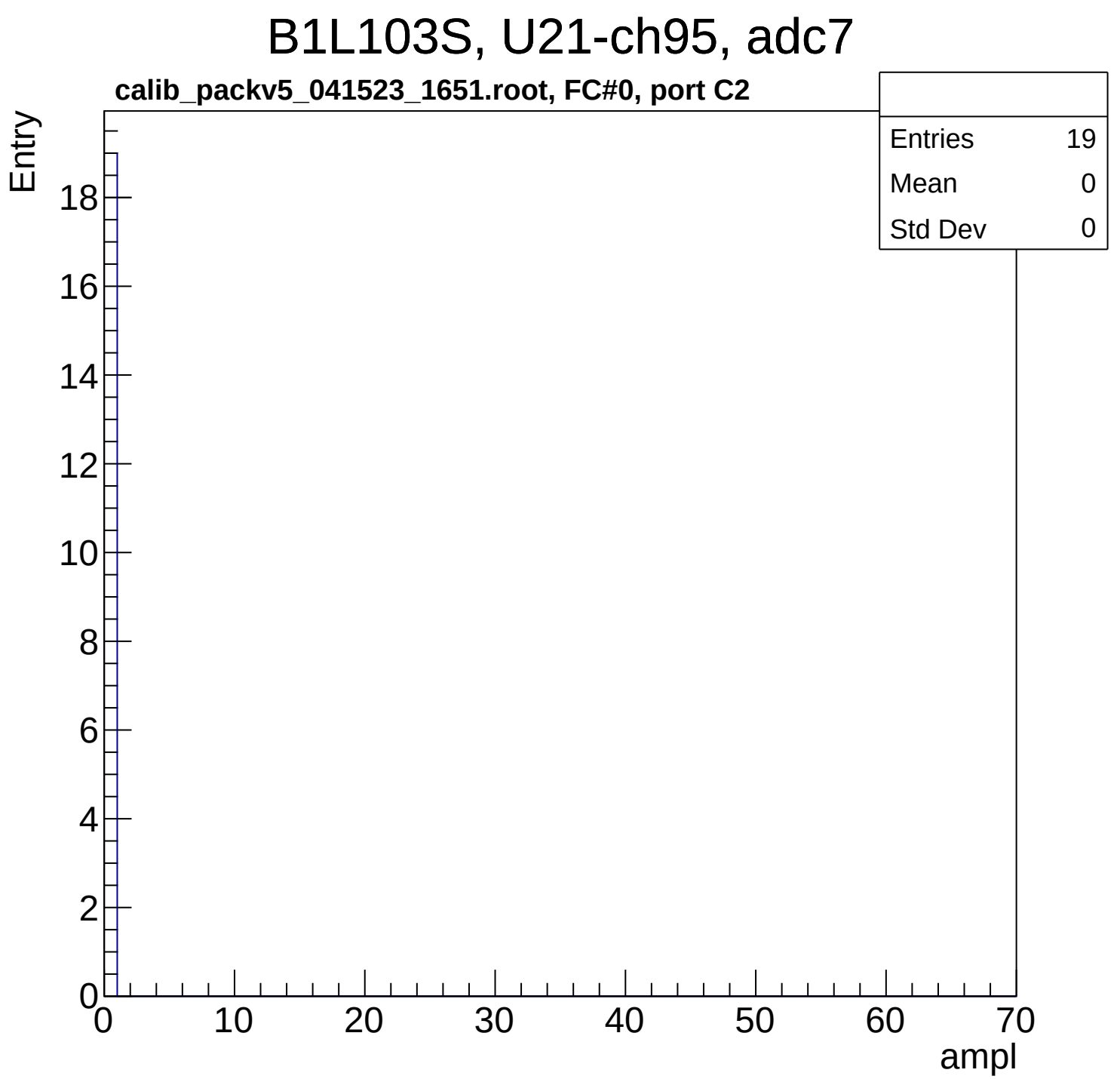
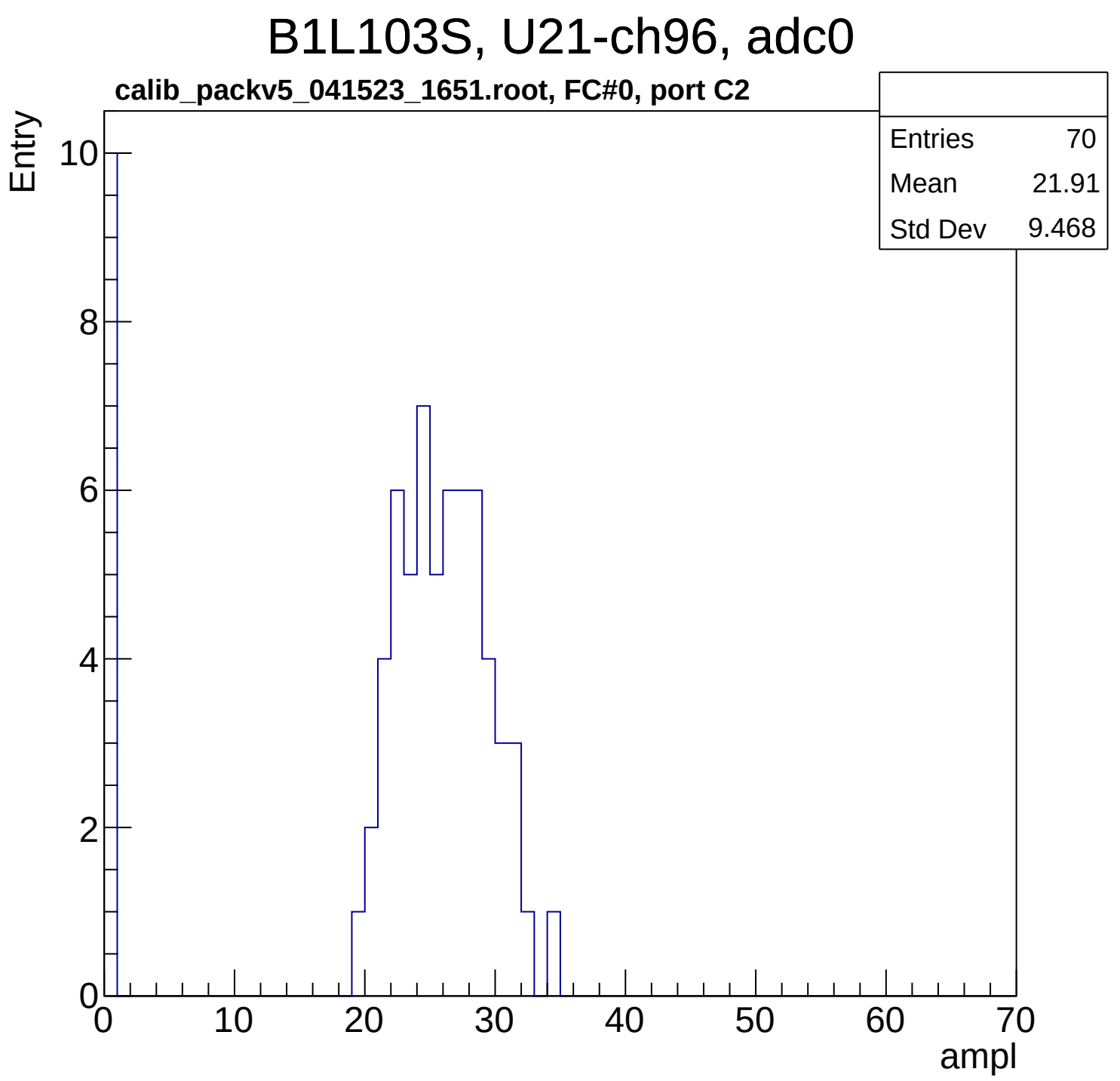
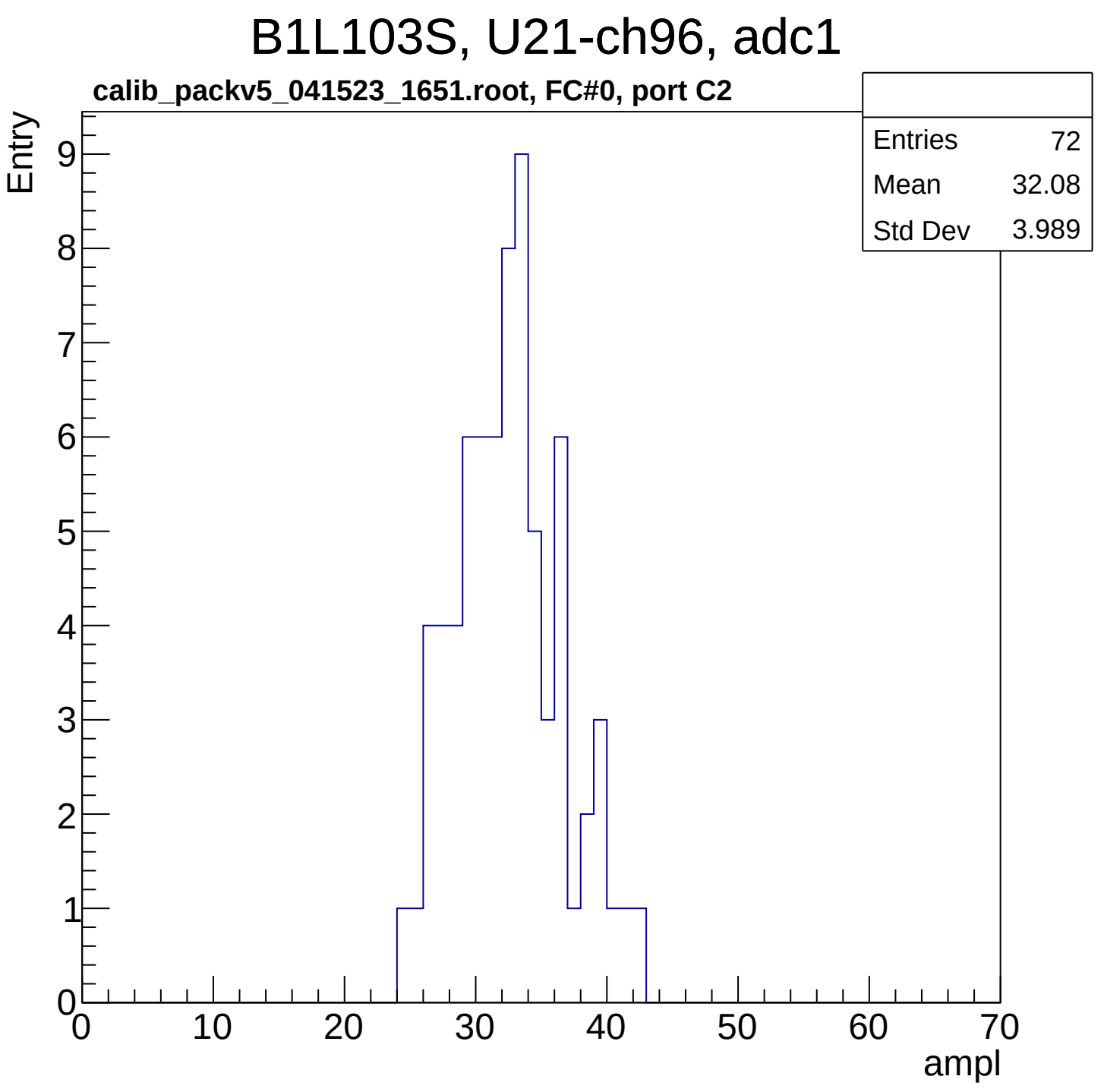
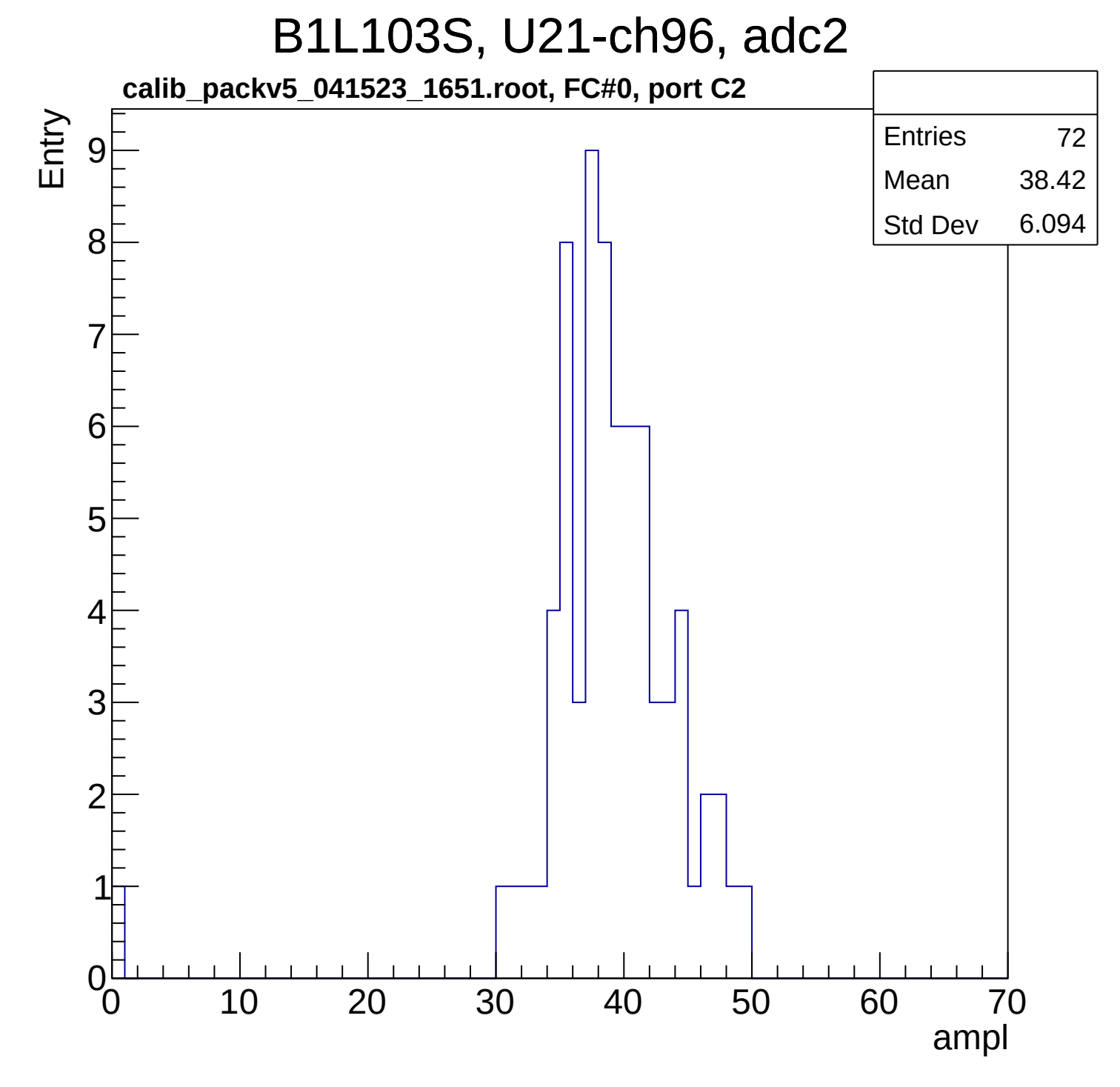
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

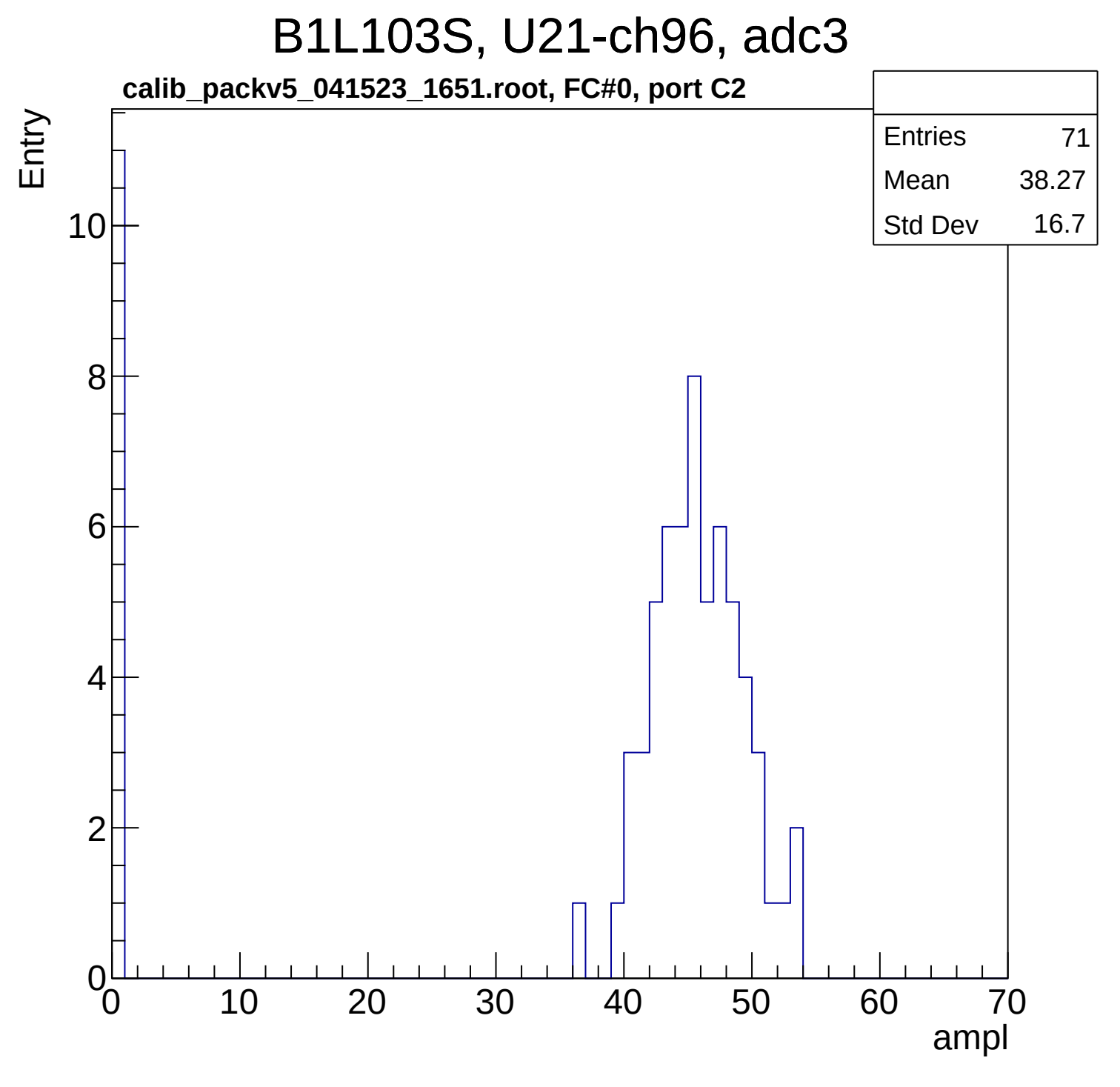

B1L103S, U21-ch95, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 61.2
Std Dev 1.166
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

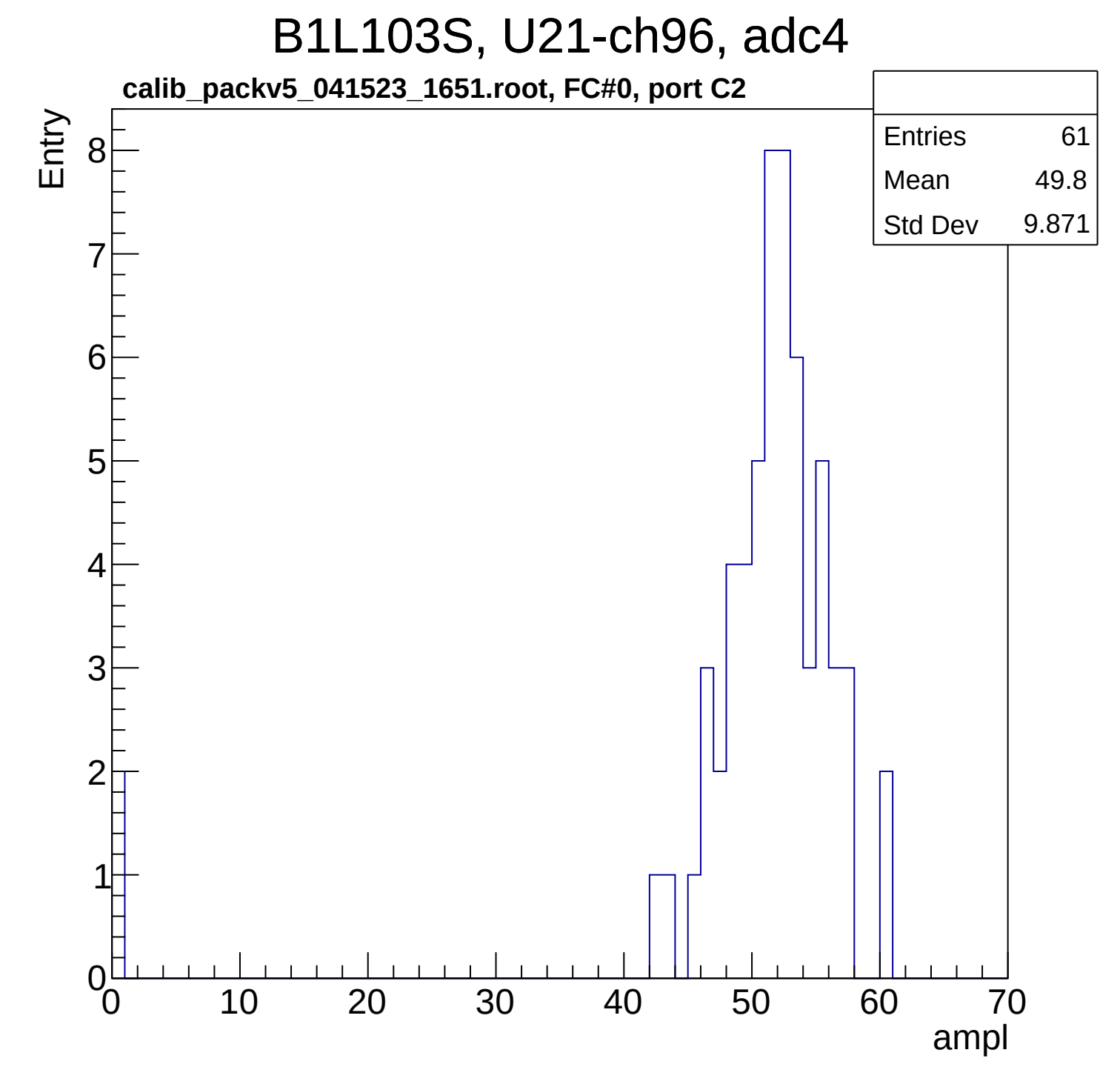

B1L103S, U21-ch95, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

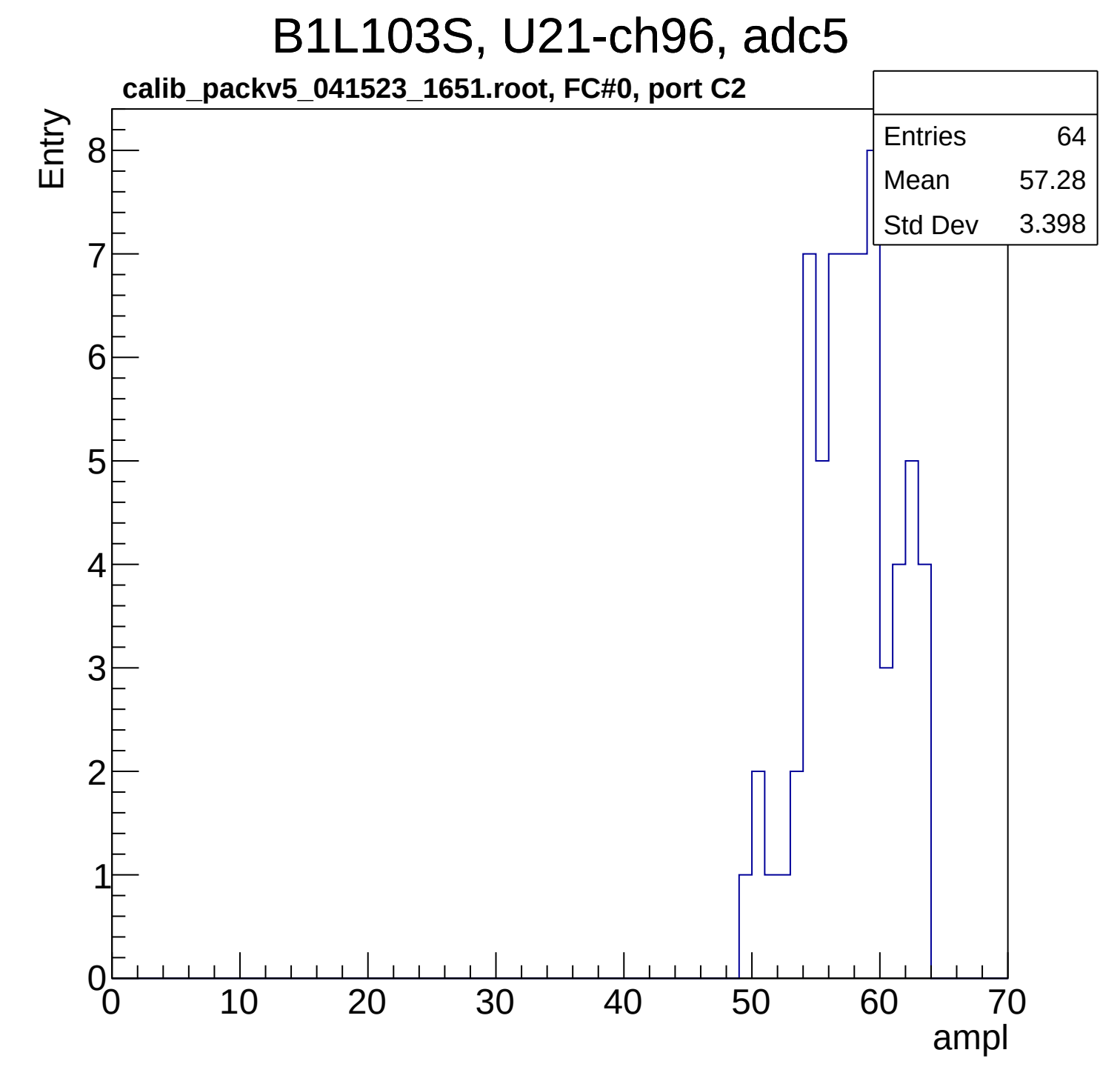

B1L103S, U21-ch96, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 21.91
Std Dev 9.468
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

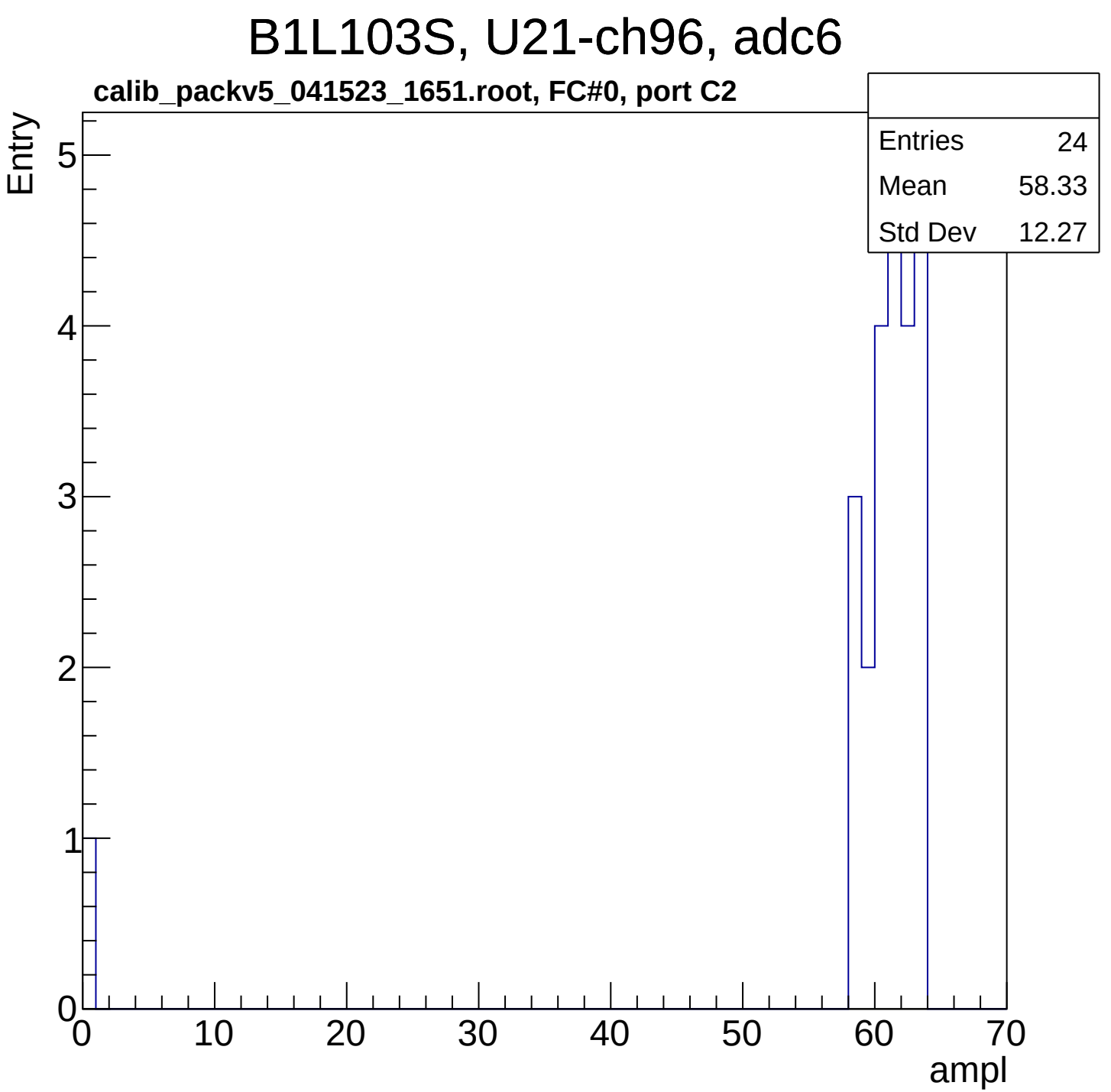

B1L103S, U21-ch96, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 32.08
Std Dev 3.989
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

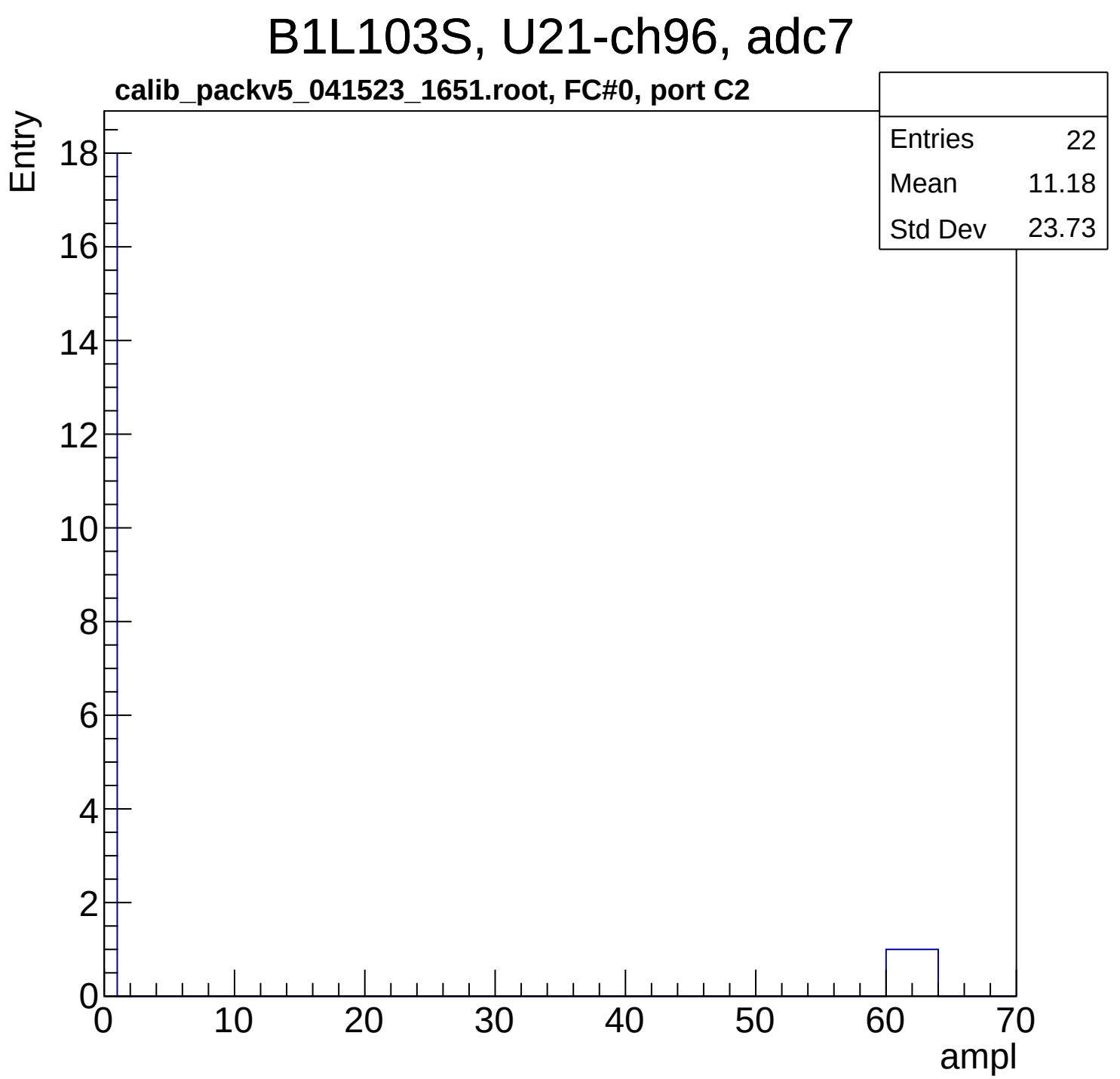

B1L103S, U21-ch96, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 38.42
Std Dev 6.094
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

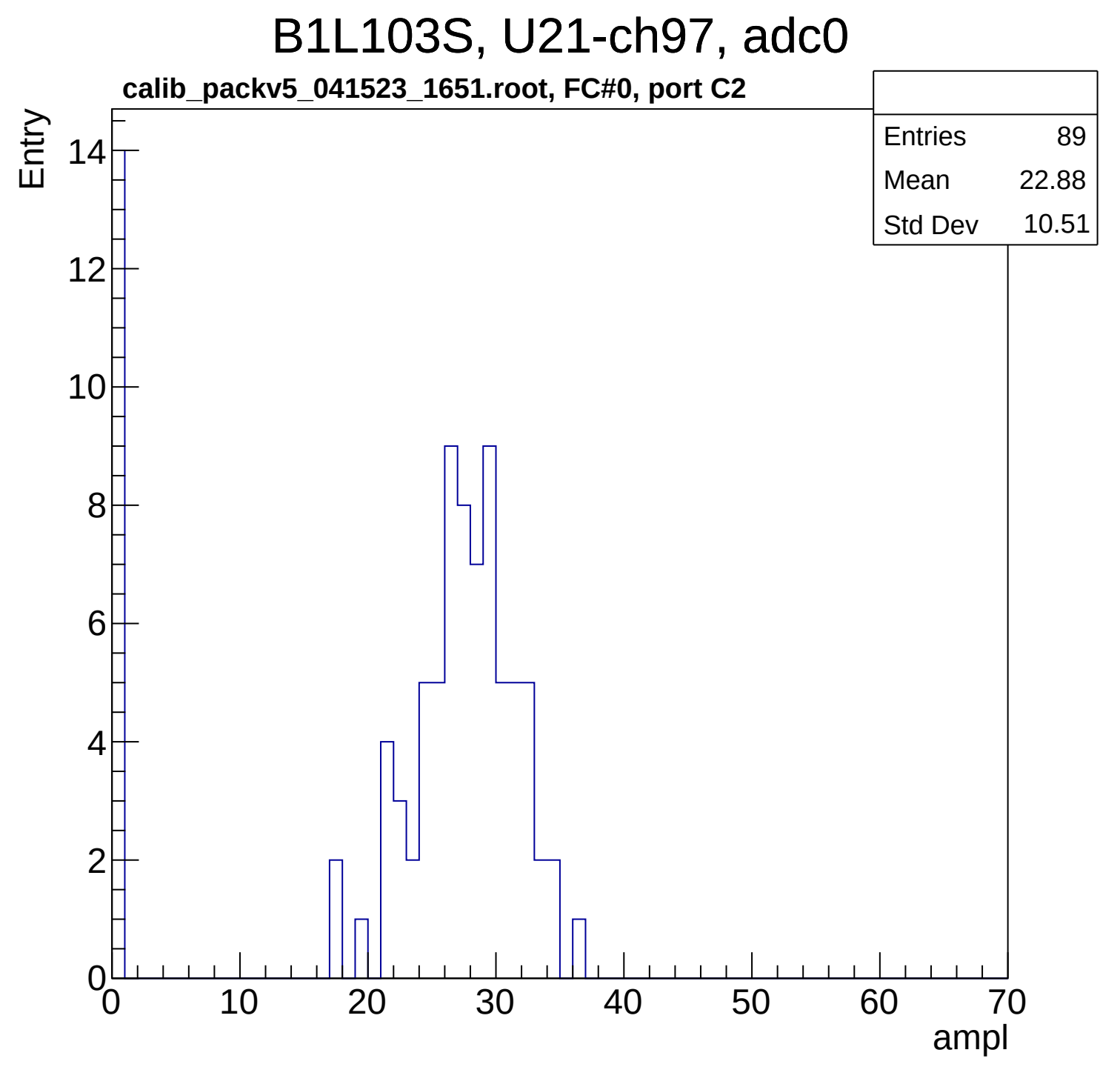

B1L103S, U21-ch96, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 38.27
Std Dev 16.7
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

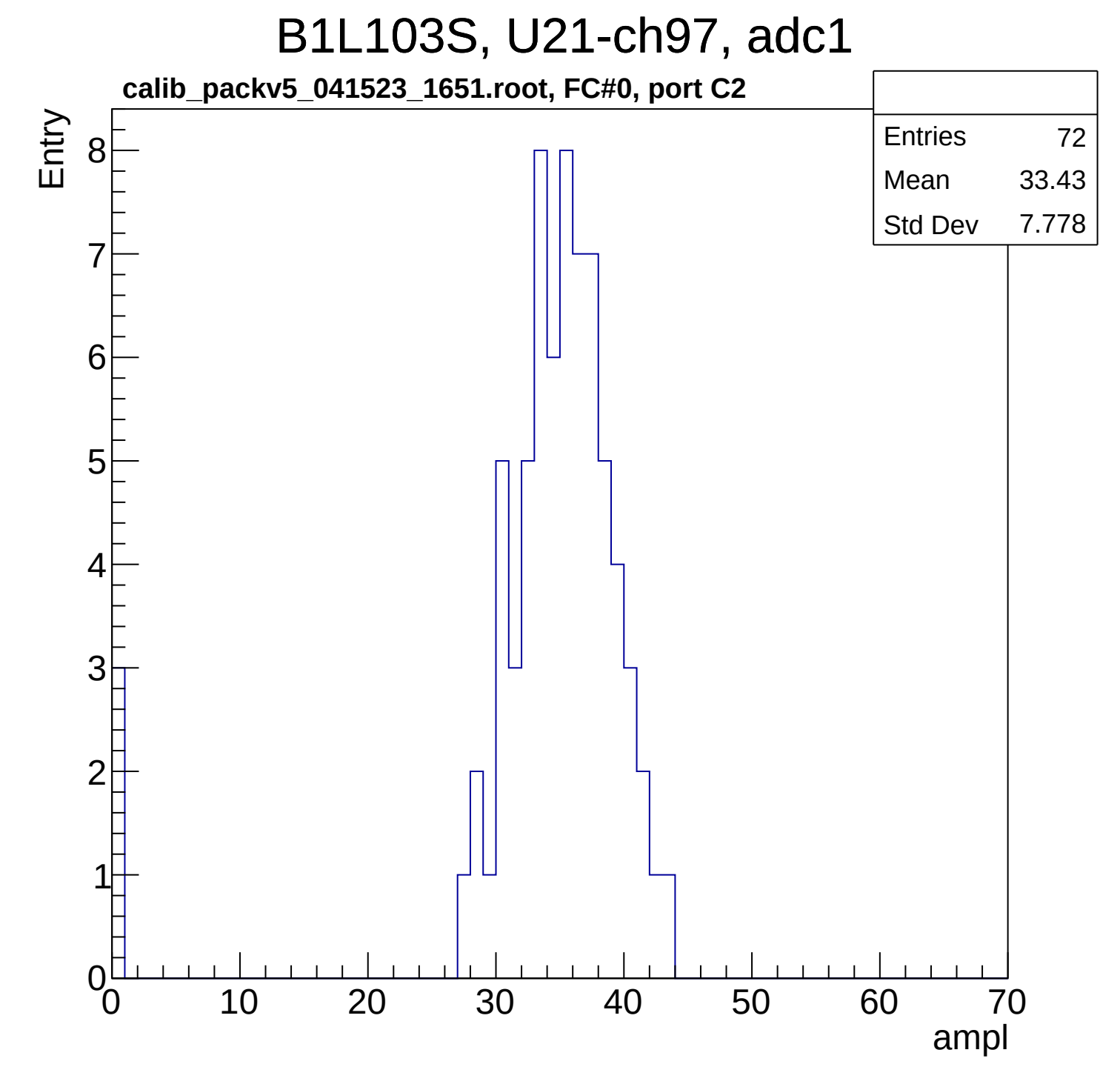

B1L103S, U21-ch96, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 49.8
Std Dev 9.871
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

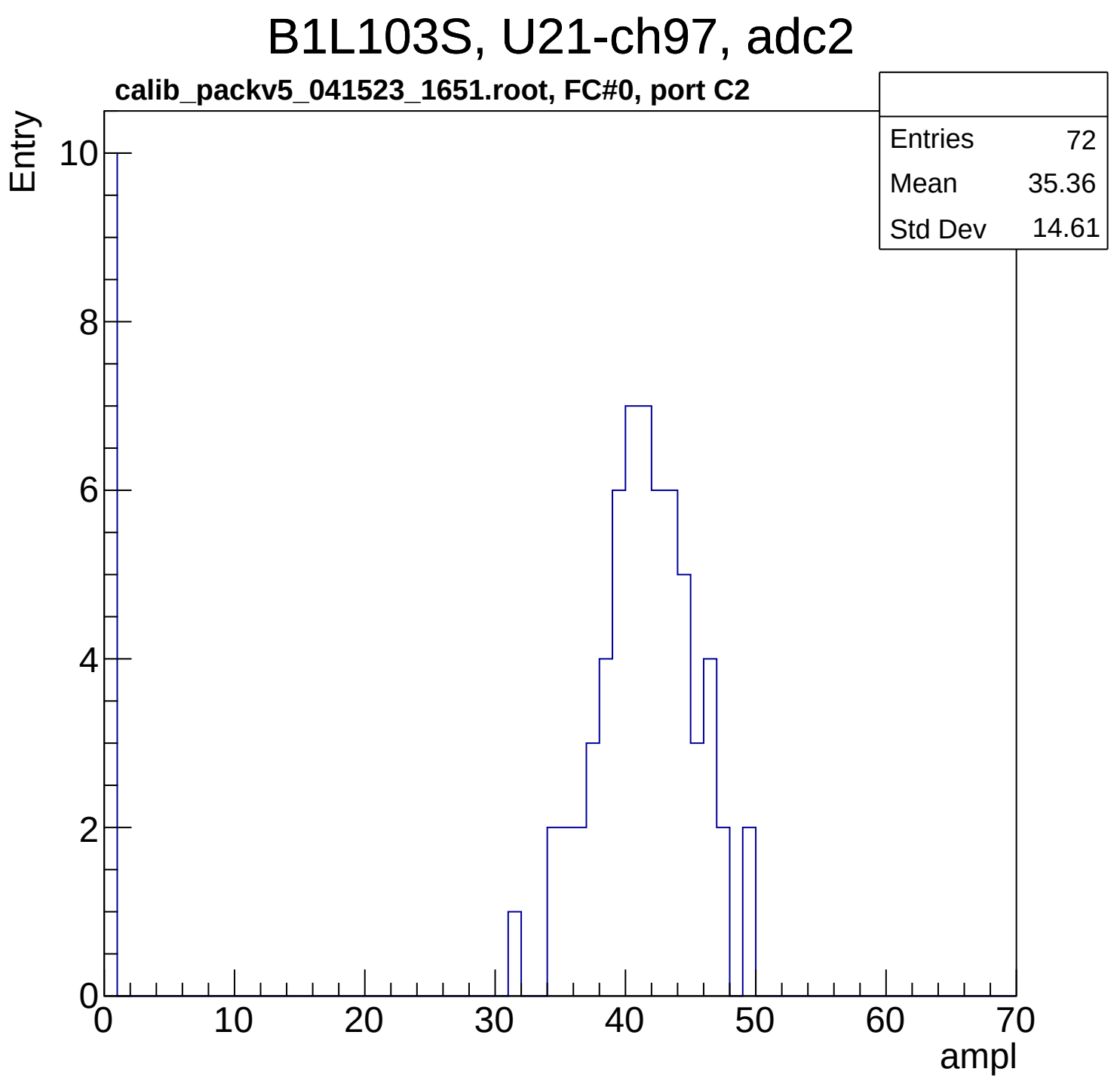

B1L103S, U21-ch96, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 57.28
Std Dev 3.398
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch96, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 58.33
Std Dev 12.27
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch96, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 11.18
Std Dev 23.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch97, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 22.88
Std Dev 10.51
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U21-ch97, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 33.43
Std Dev 7.778
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch97, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 35.36
Std Dev 14.61
Entry
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6
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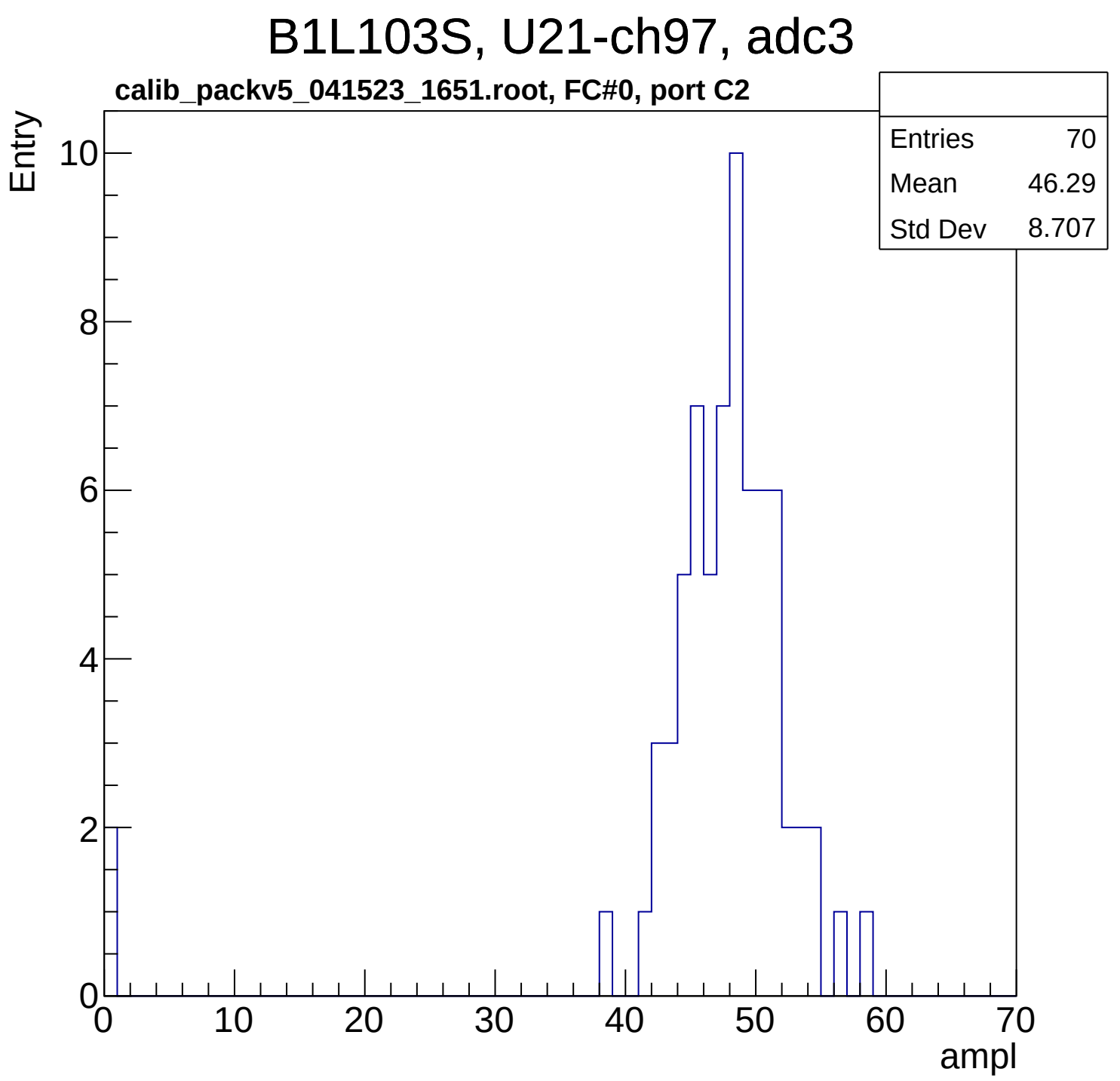
ampl


B1L103S, U21-ch97, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 46.29
Std Dev 8.707
Entry
ampl
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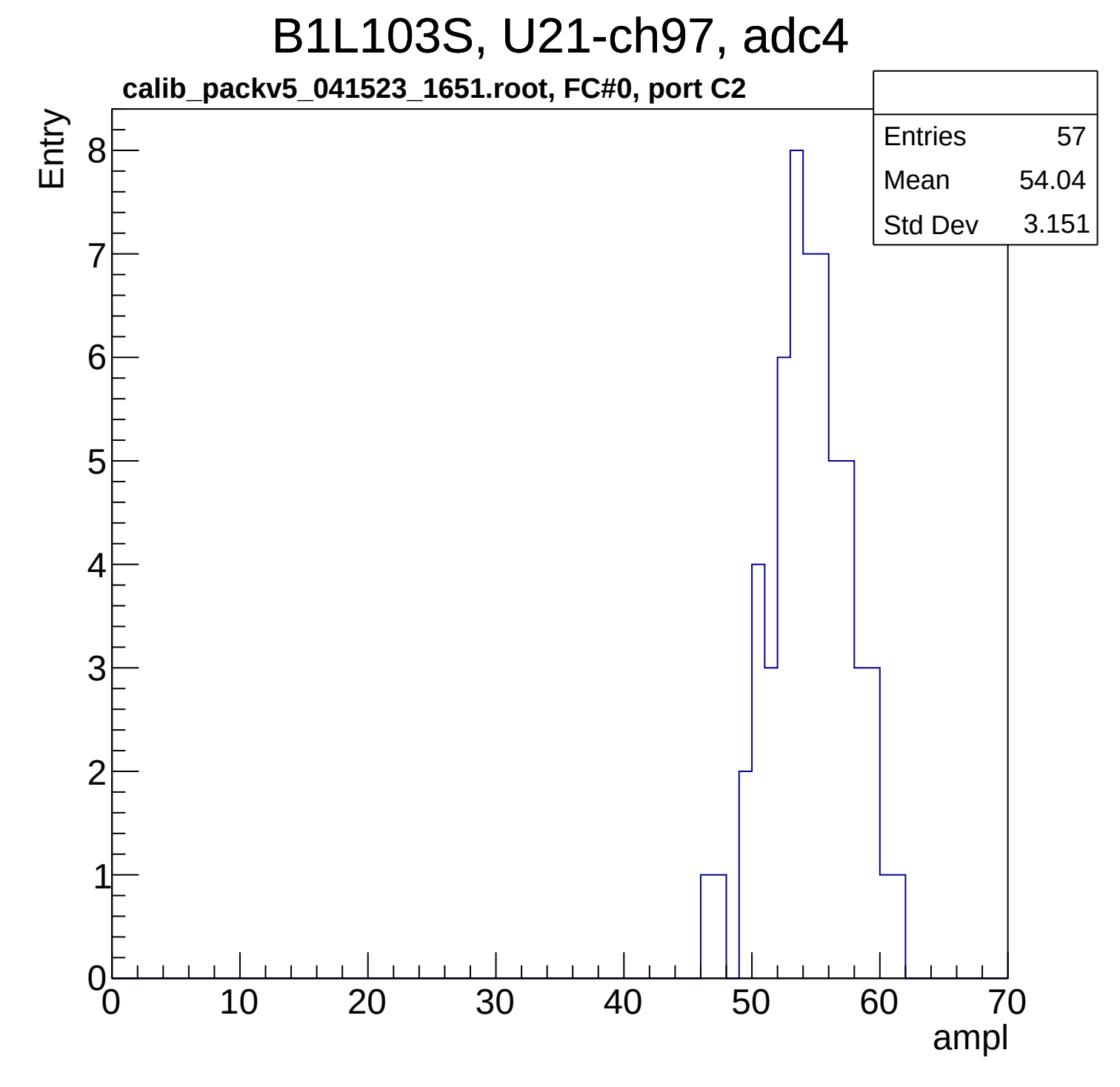
B1L103S, U21-ch97, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 54.04
Std Dev 3.151
Entry
ampl
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2
3
4
5
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0
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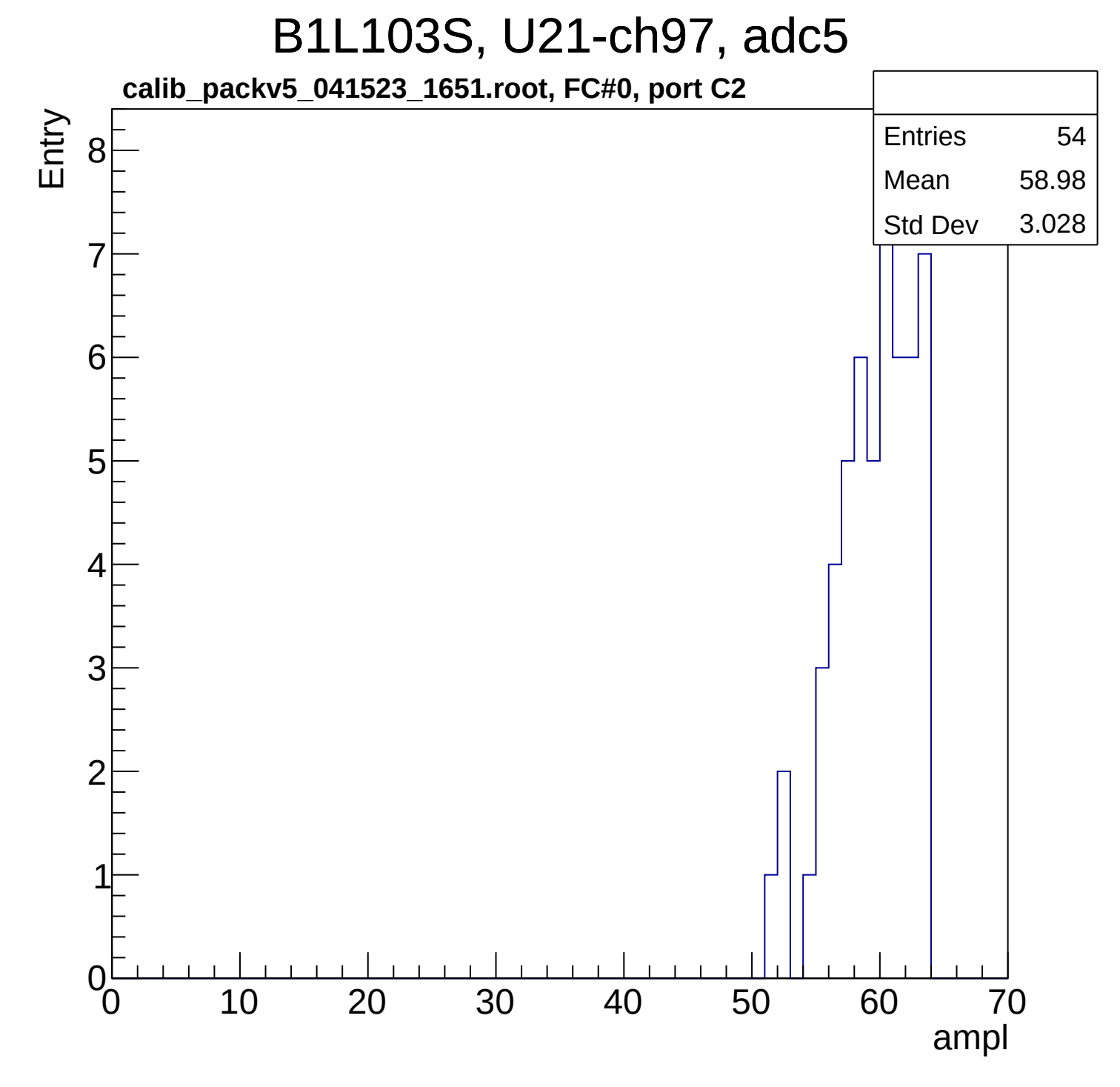
B1L103S, U21-ch97, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 58.98
Std Dev 3.028
Entry
ampl
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0
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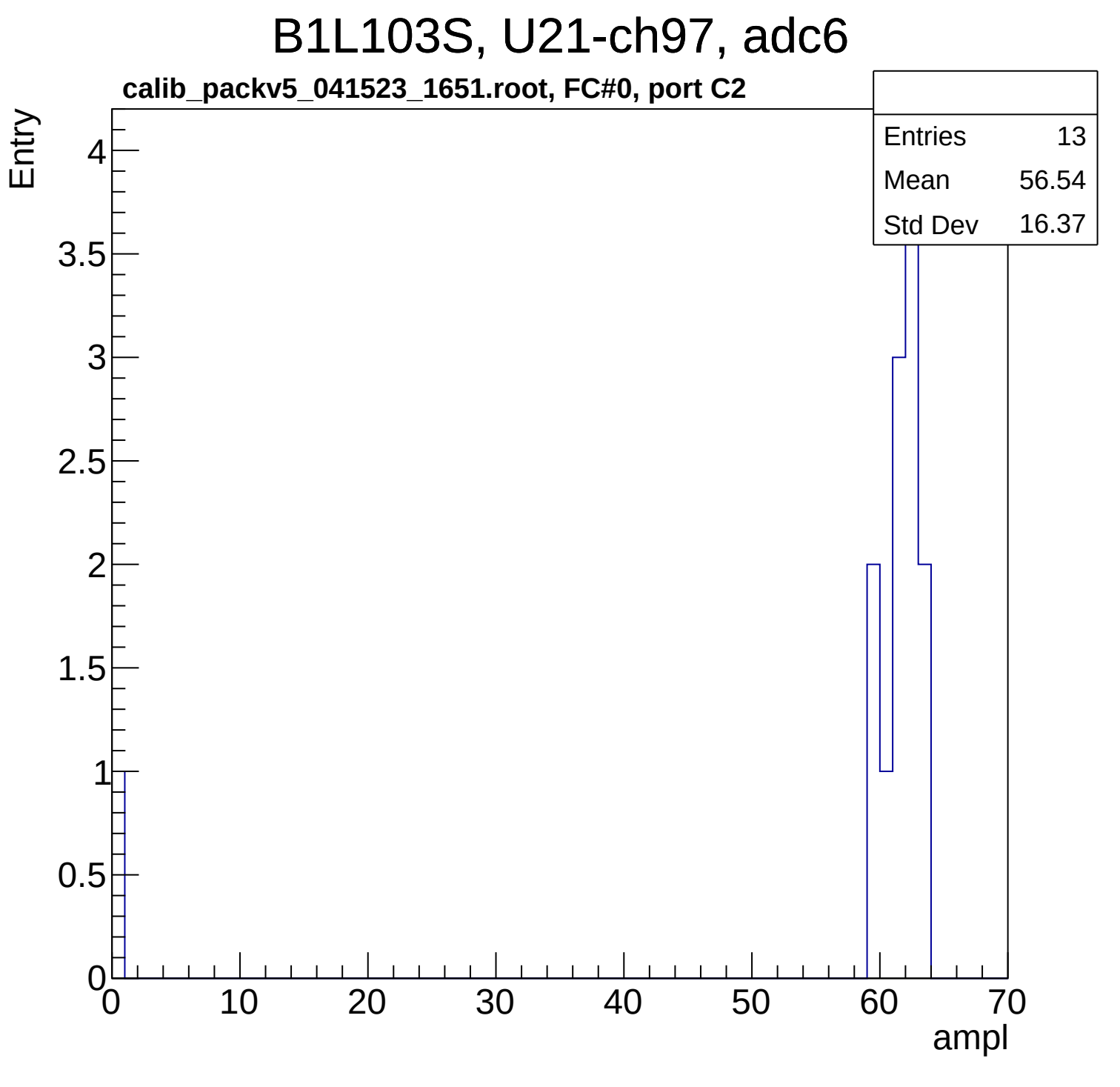
B1L103S, U21-ch97, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 56.54
Std Dev 16.37
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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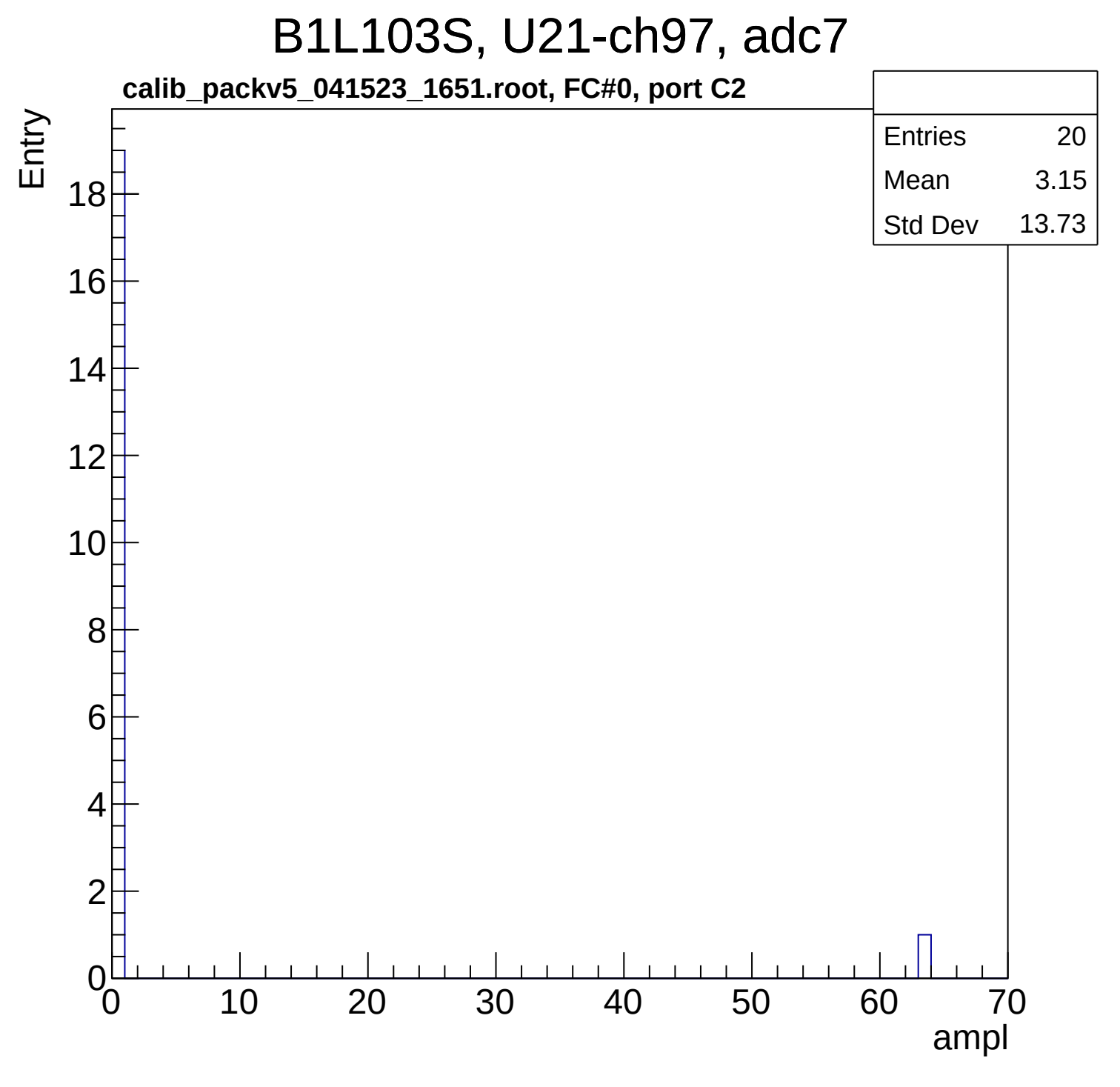
B1L103S, U21-ch97, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
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6
8
10
12
14
16
18
0
10
20
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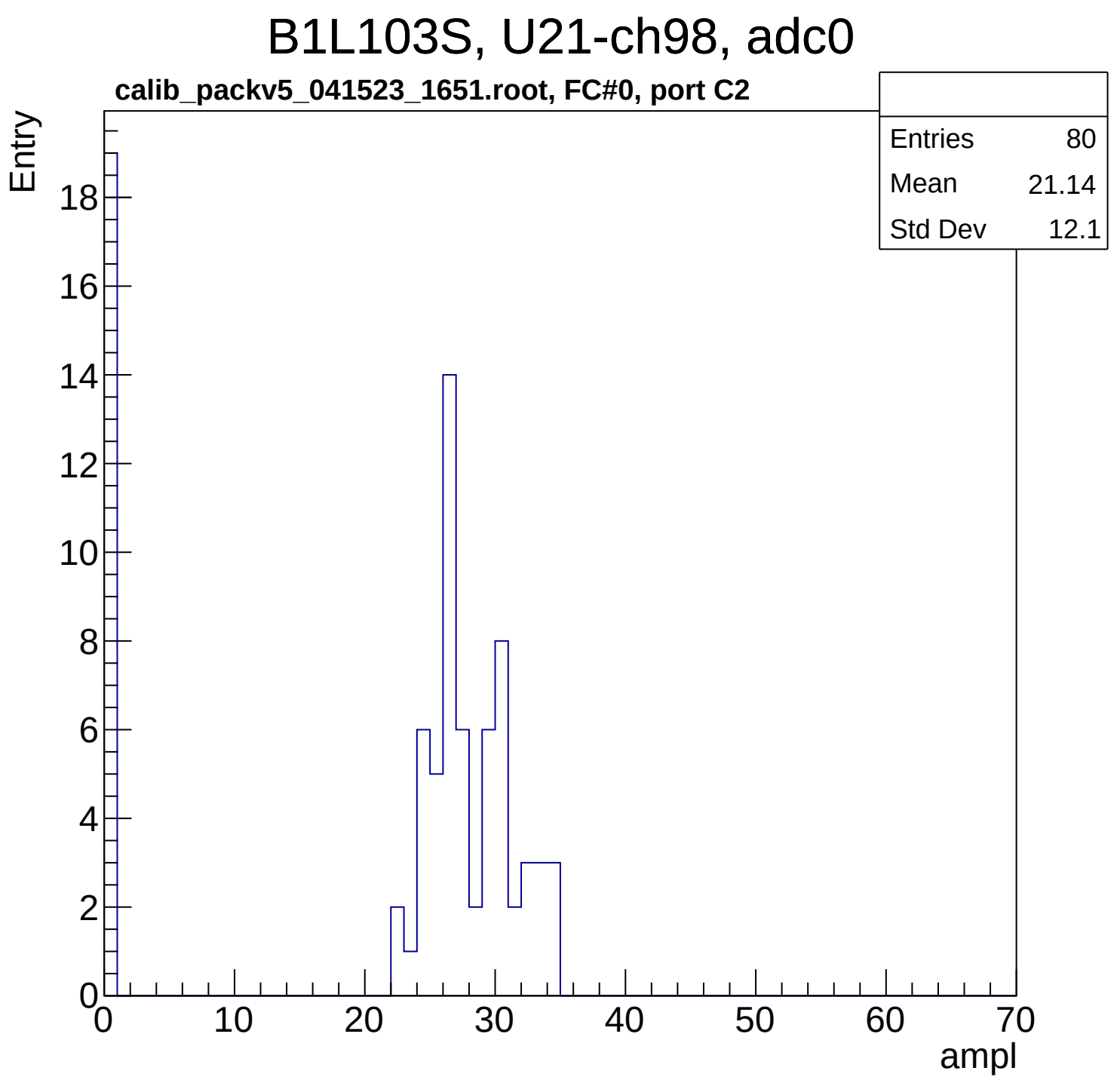
50
60
70
ampl


B1L103S, U21-ch98, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 21.14
Std Dev 12.1
Entry
0
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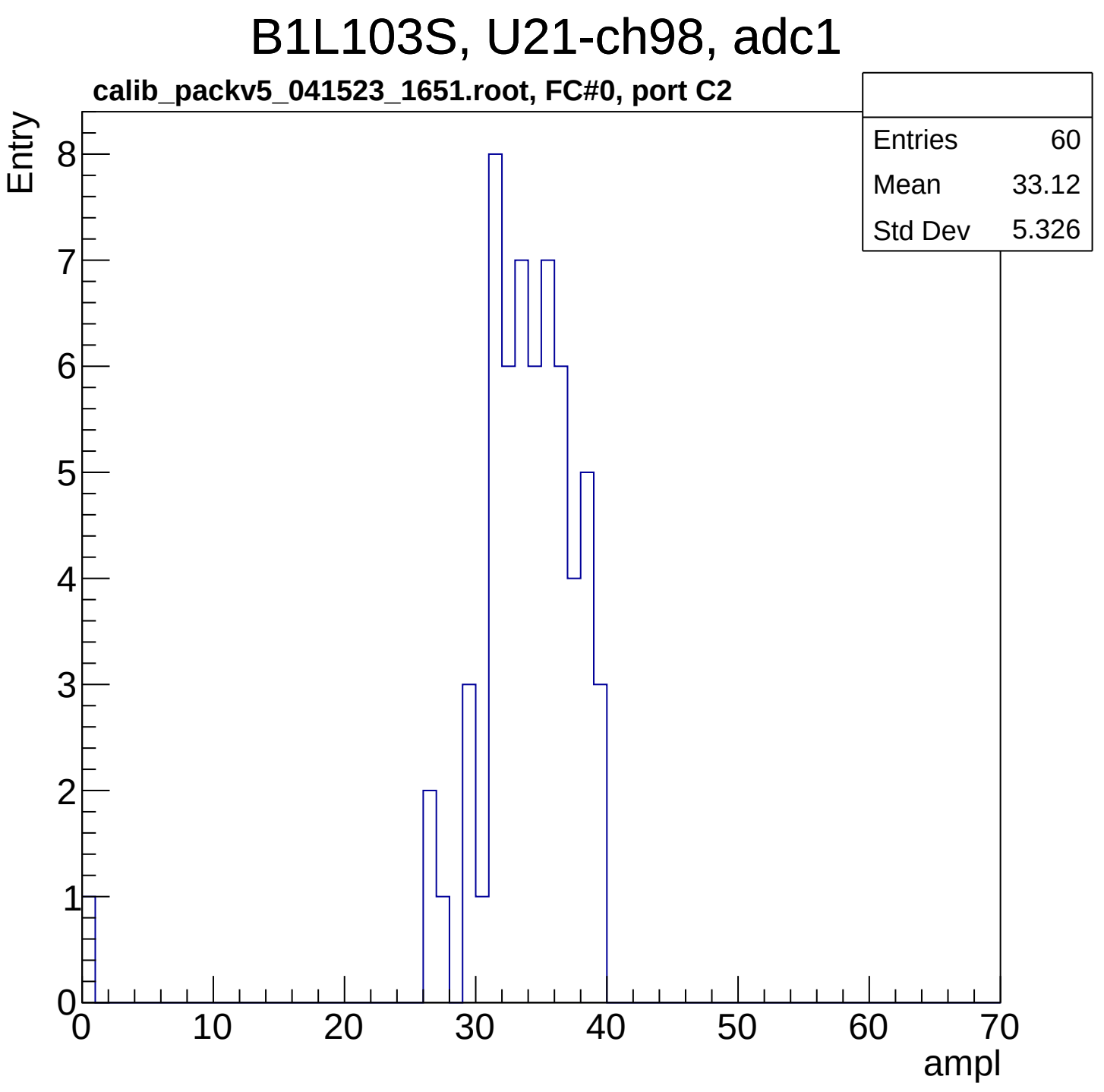
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch98, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 33.12
Std Dev 5.326
Entry
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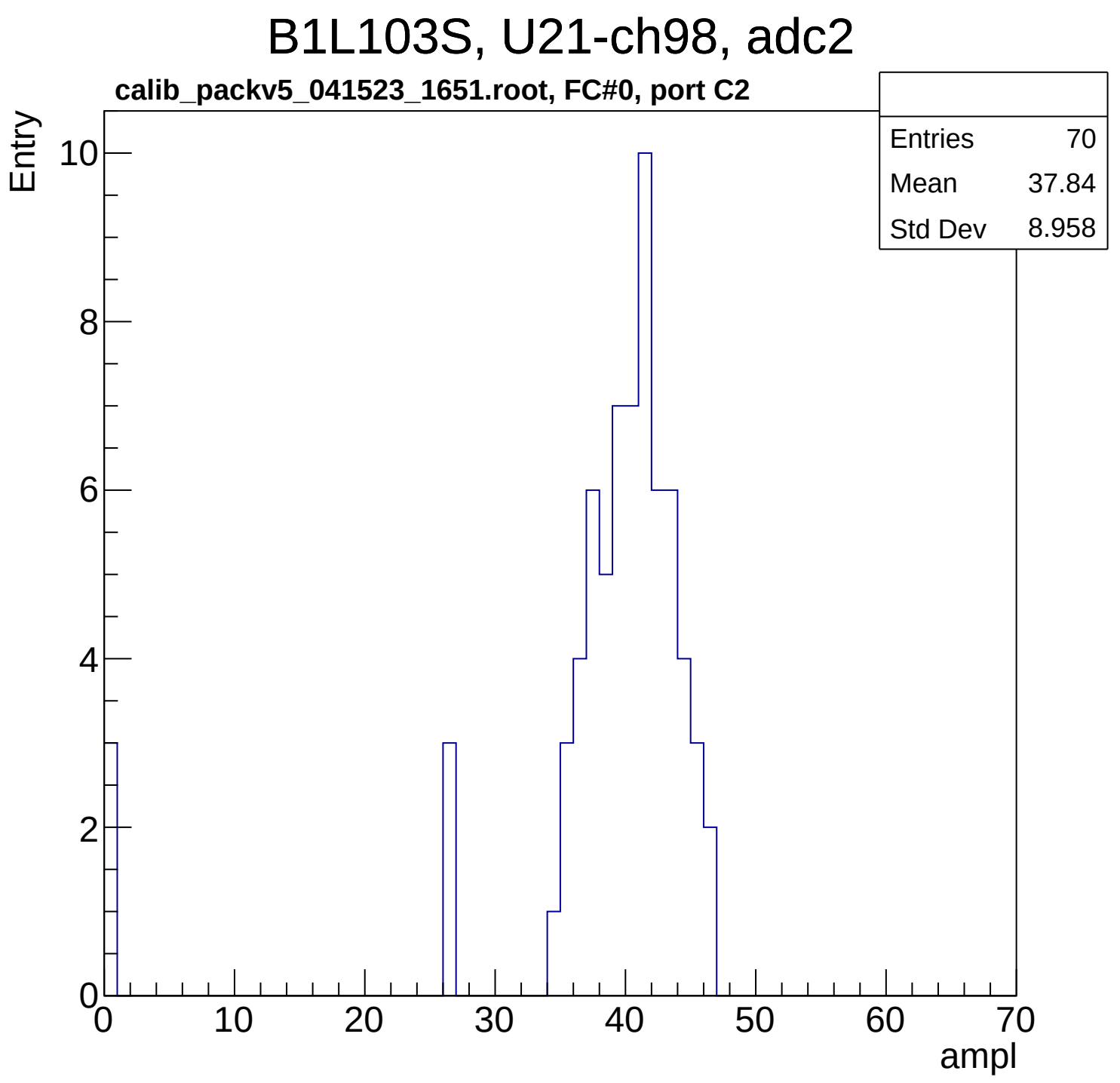
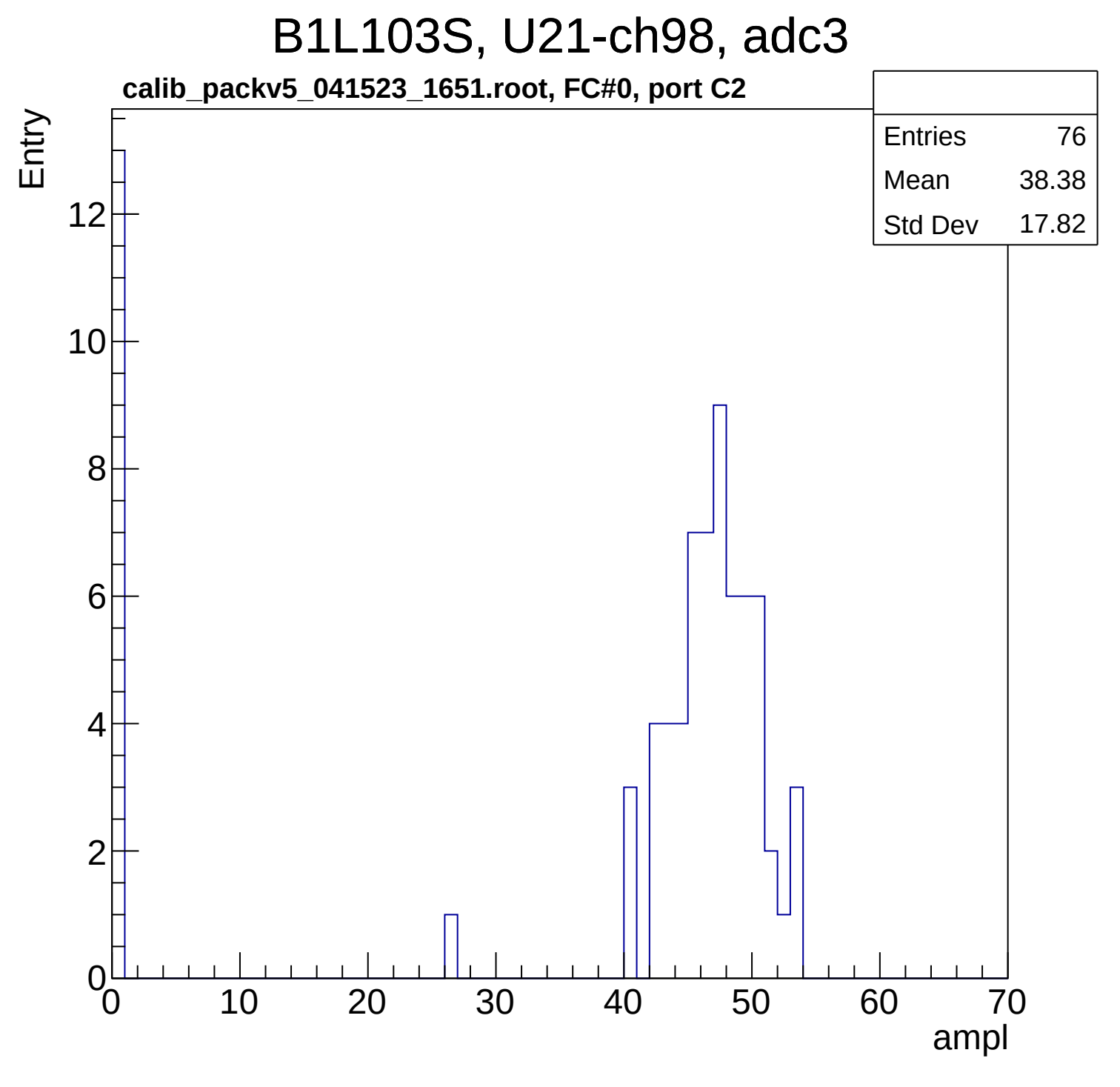
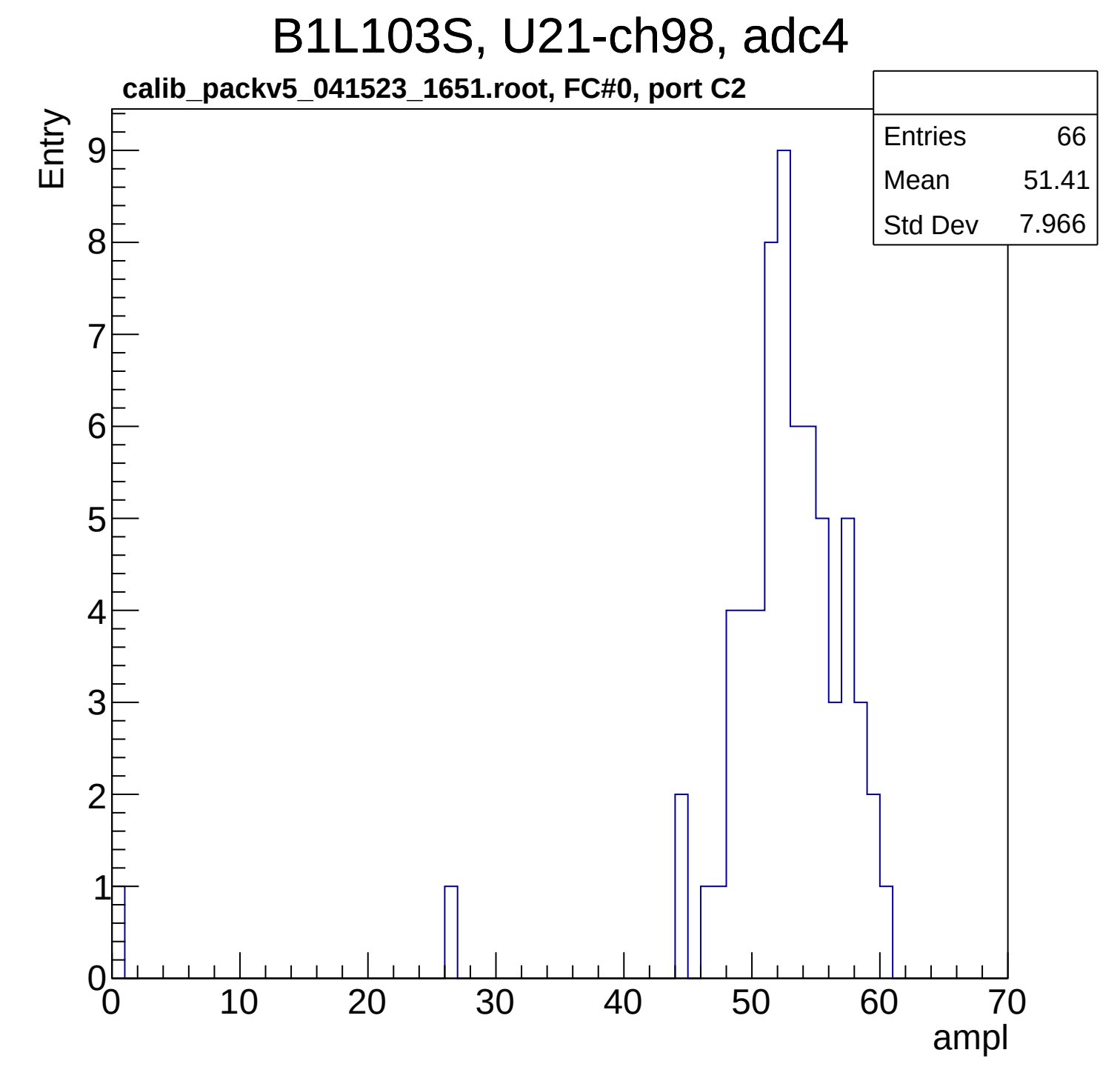
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch98, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 37.84
Std Dev 8.958
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U21-ch98, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 38.38
Std Dev 17.82
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U21-ch98, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 51.41
Std Dev 7.966
Entry
ampl
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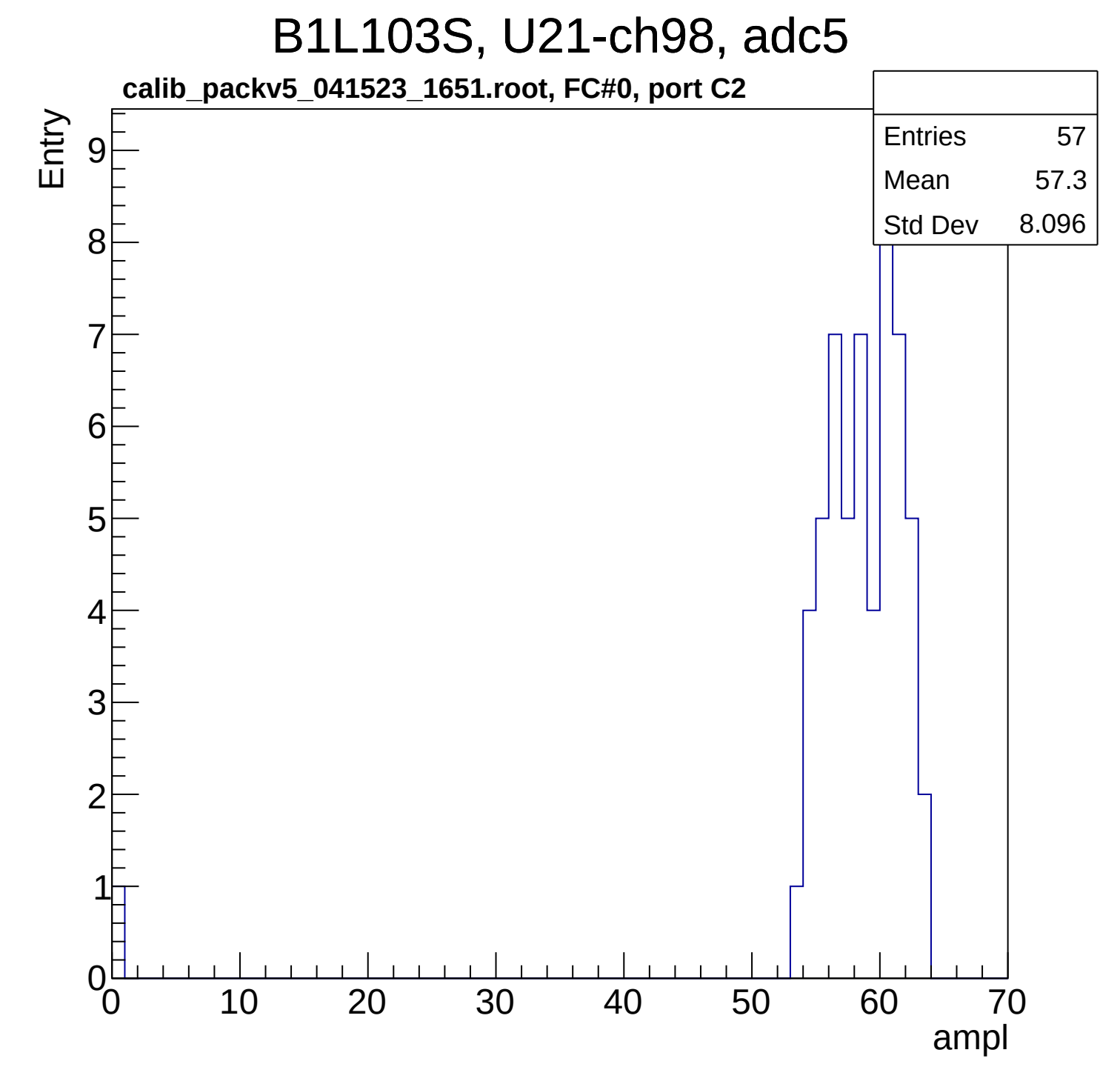
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch98, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 57.3
Std Dev 8.096
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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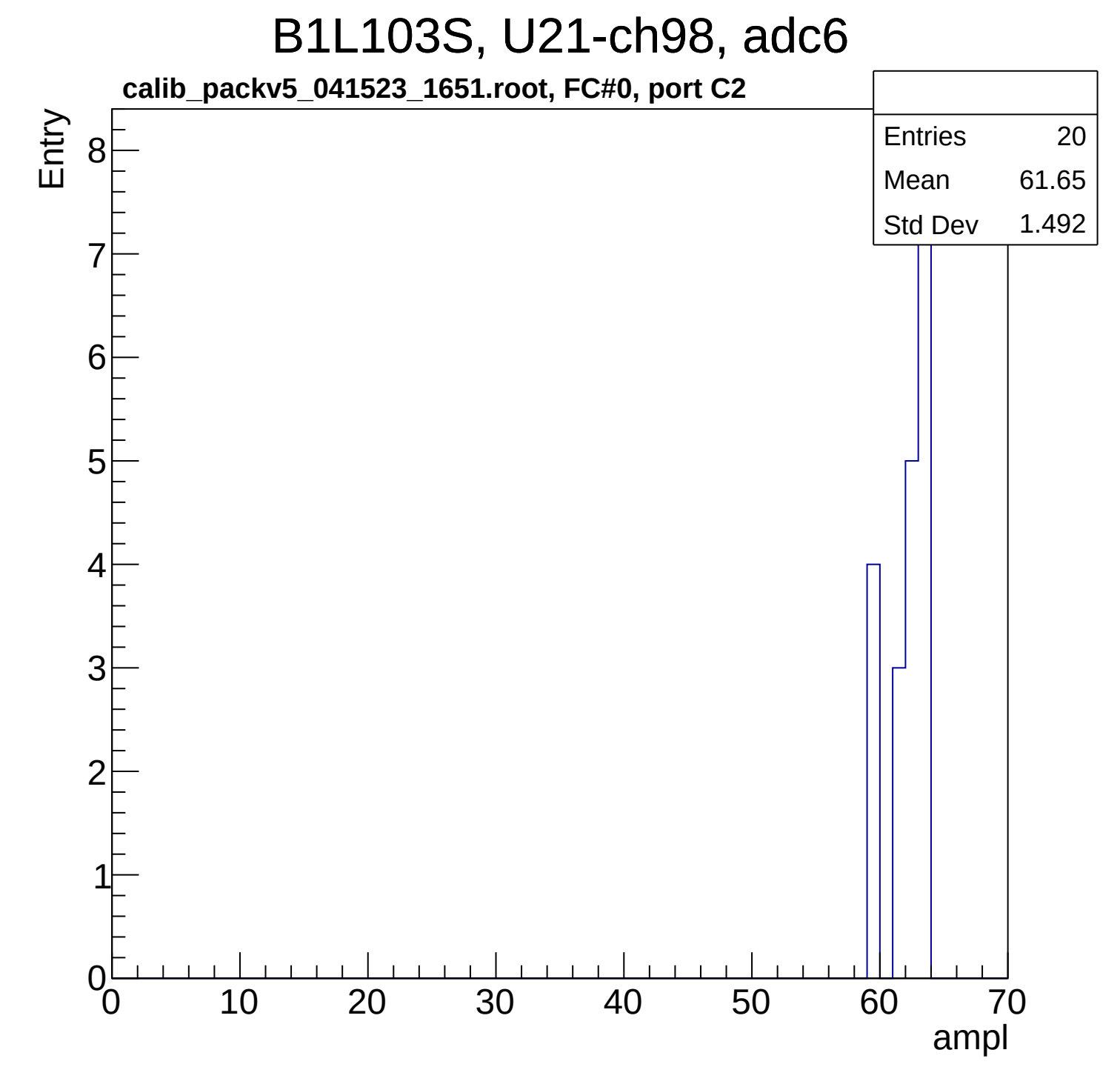
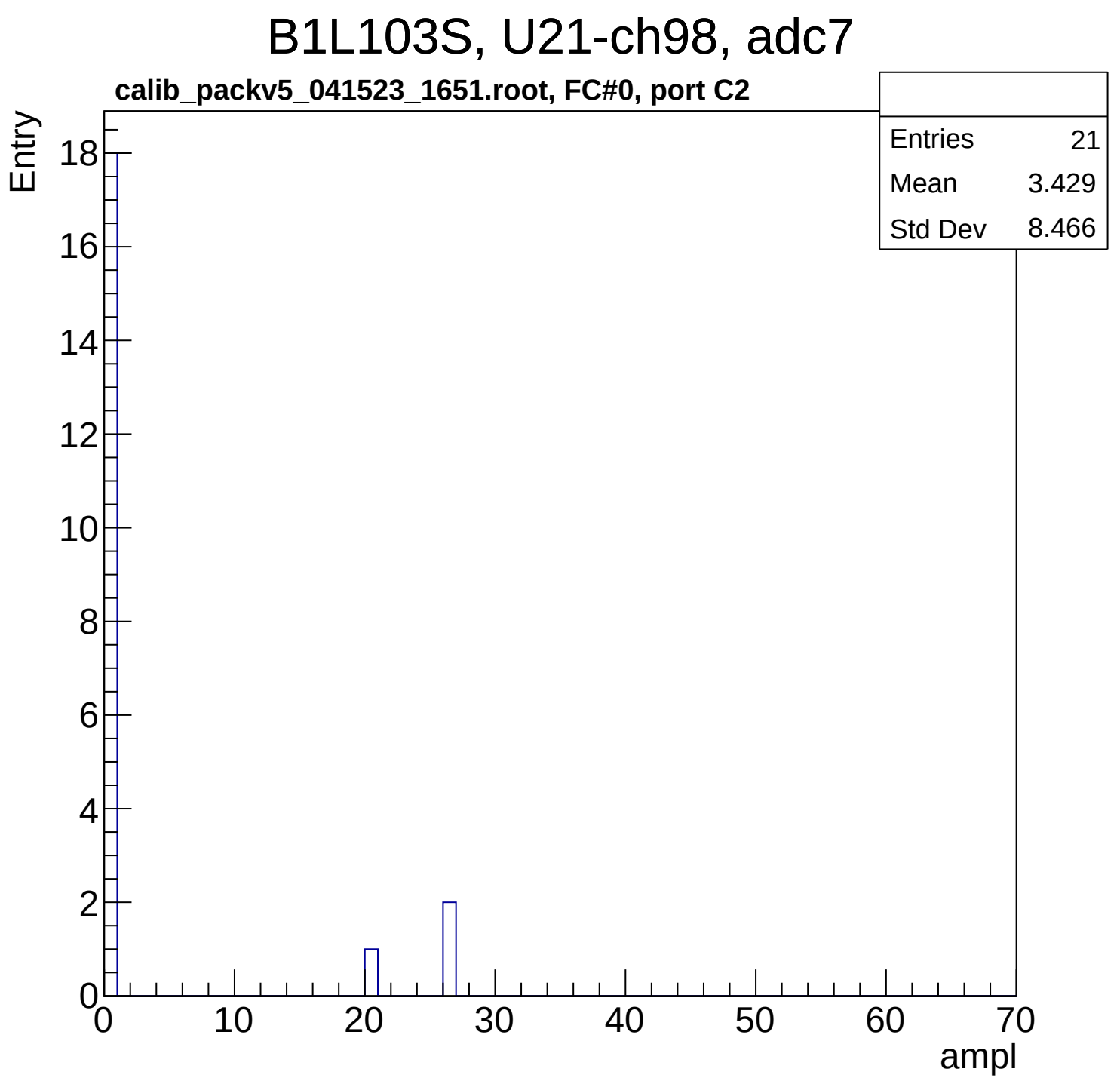

B1L103S, U21-ch98, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 61.65
Std Dev 1.492
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch98, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 3.429
Std Dev 8.466
Entry
ampl
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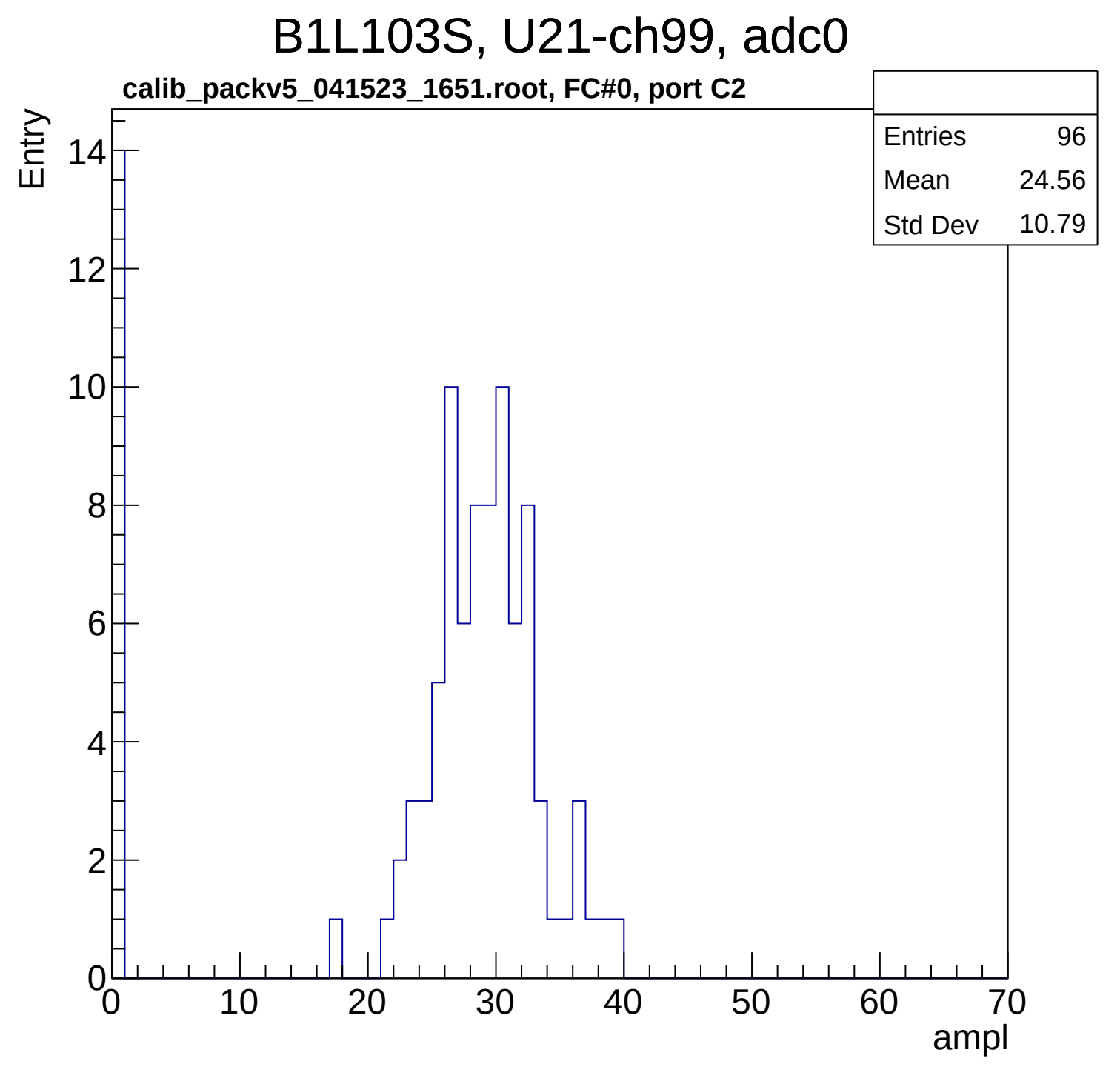
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L103S, U21-ch99, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 96
Mean 24.56
Std Dev 10.79
Entry
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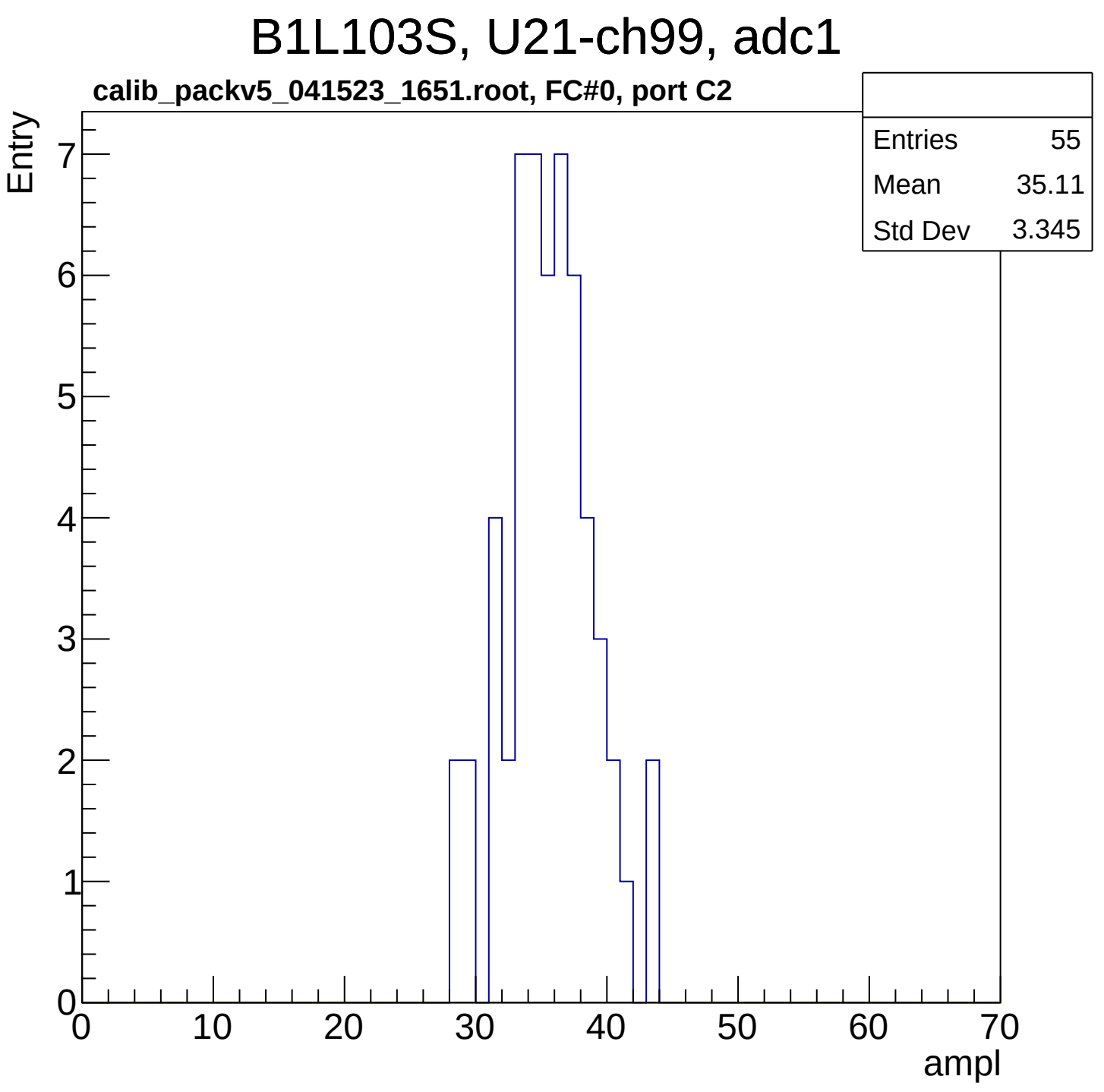
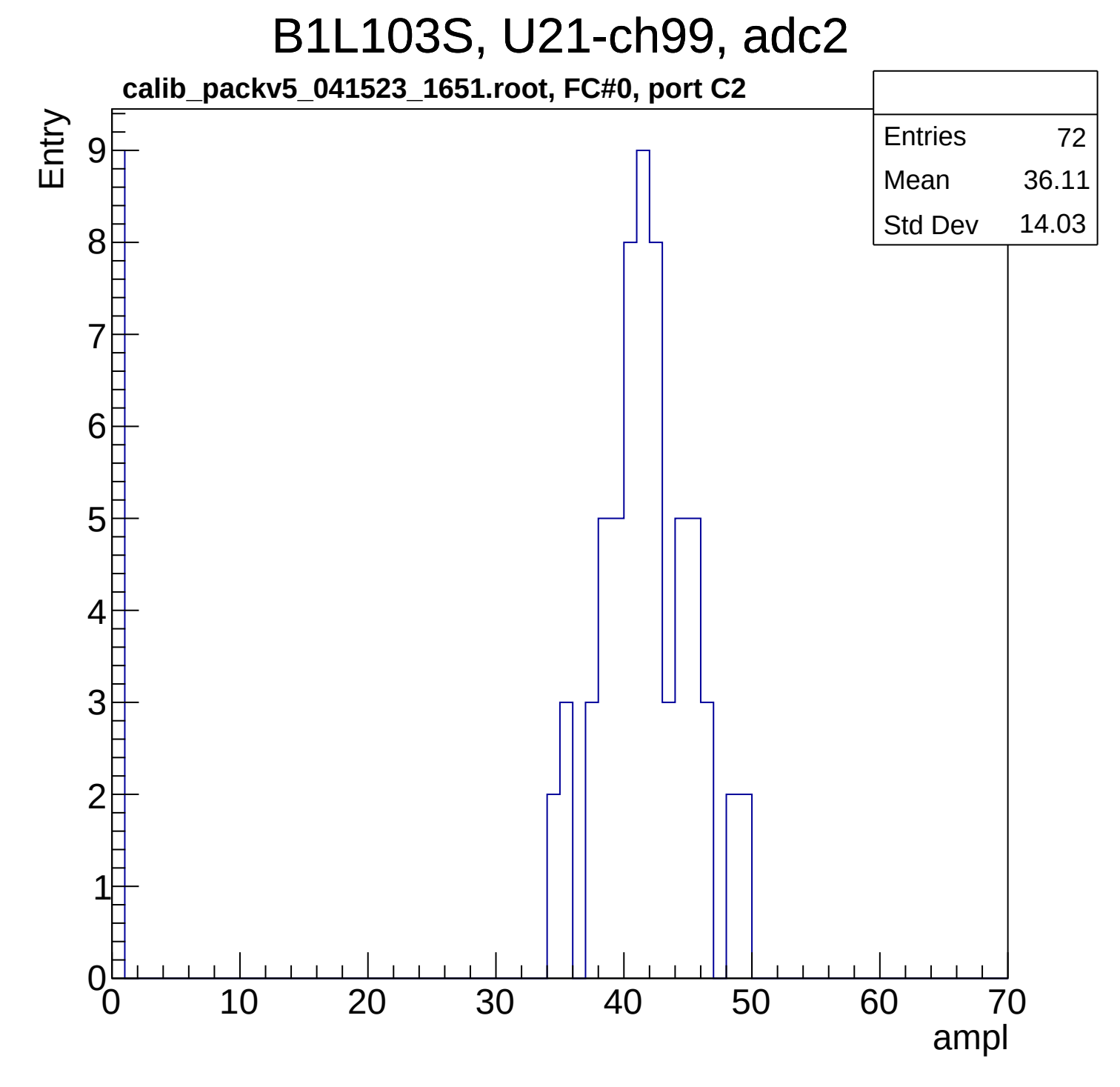
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch99, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 35.11
Std Dev 3.345
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U21-ch99, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 36.11
Std Dev 14.03
Entry
ampl
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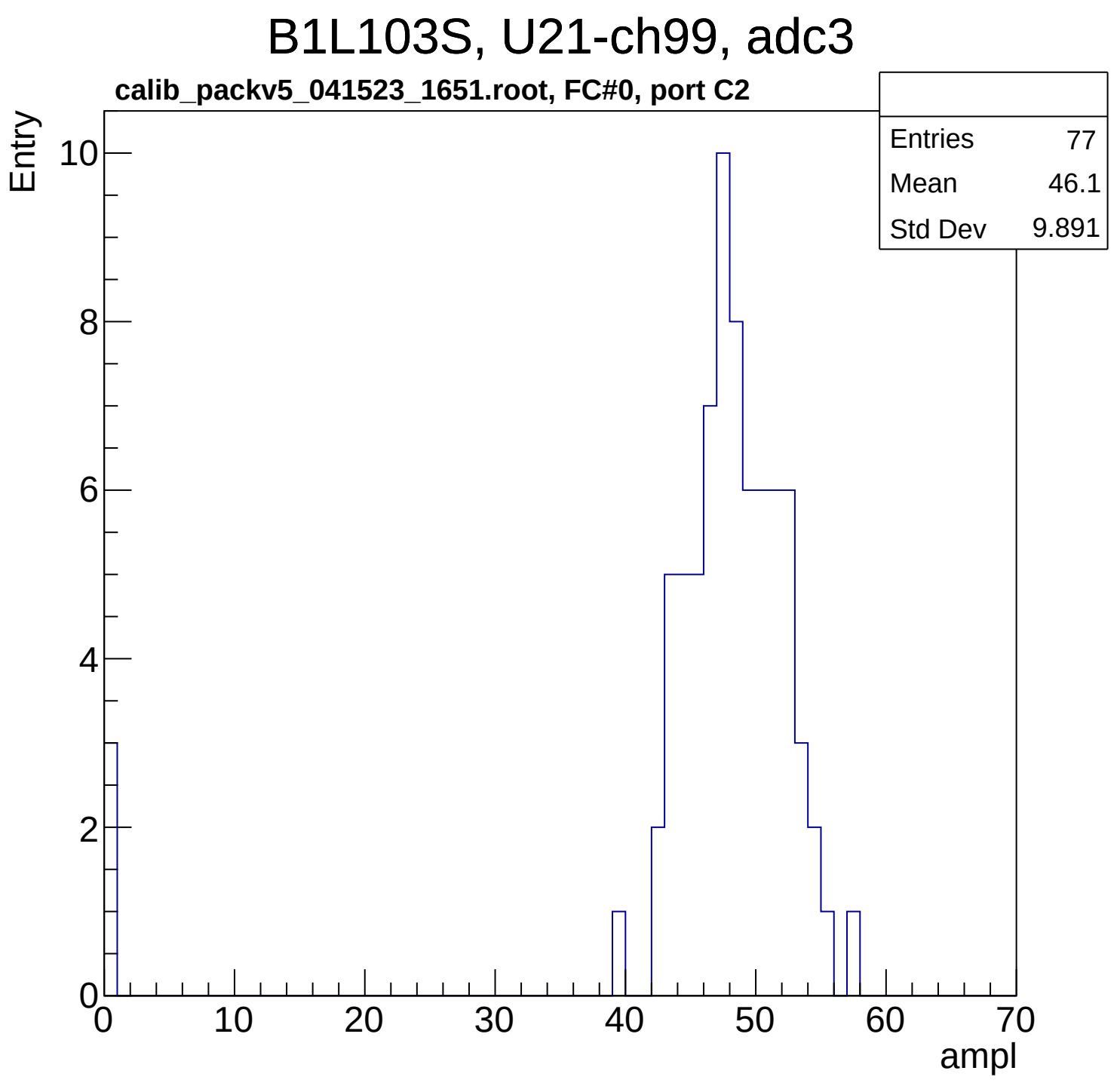
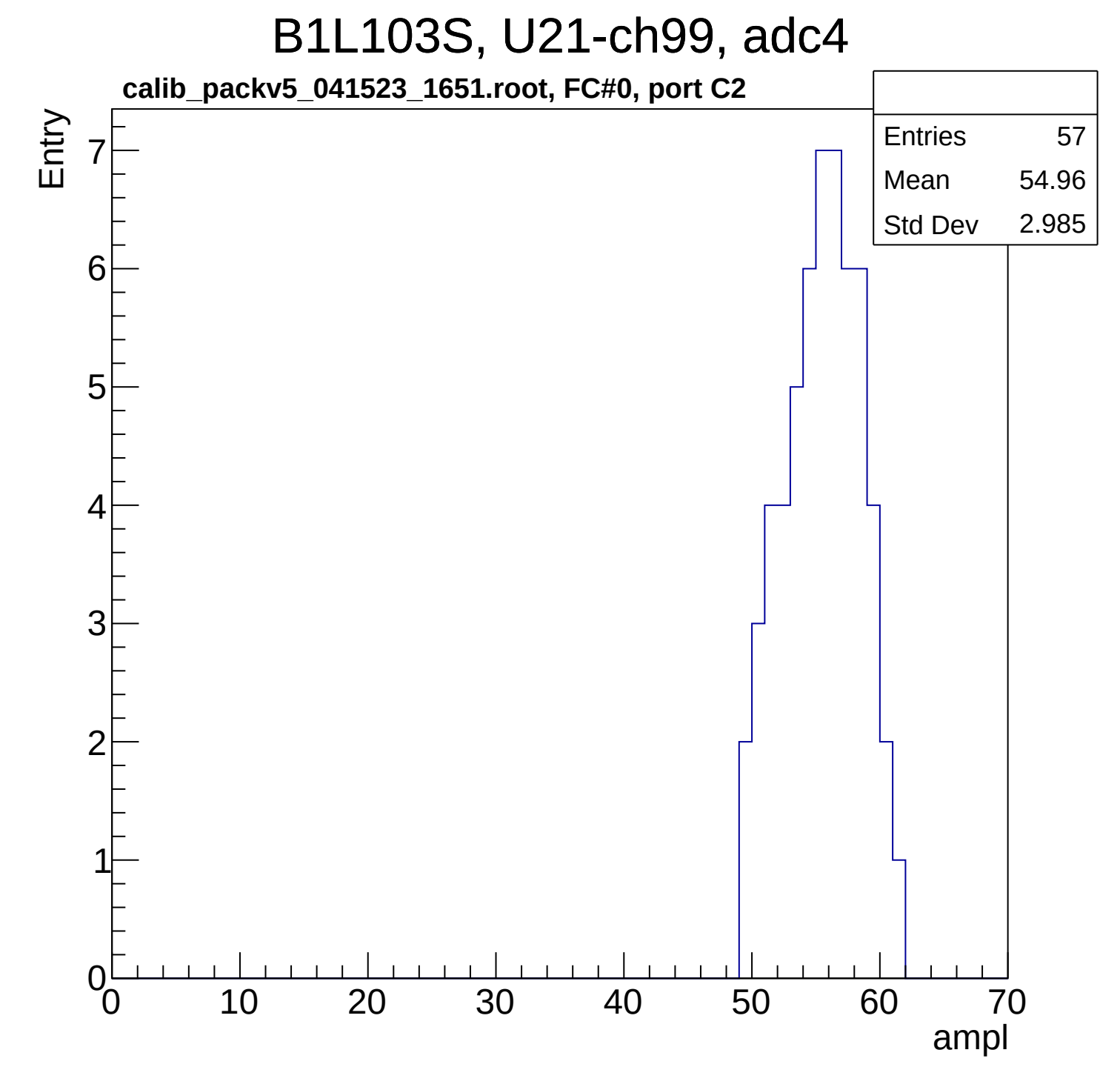
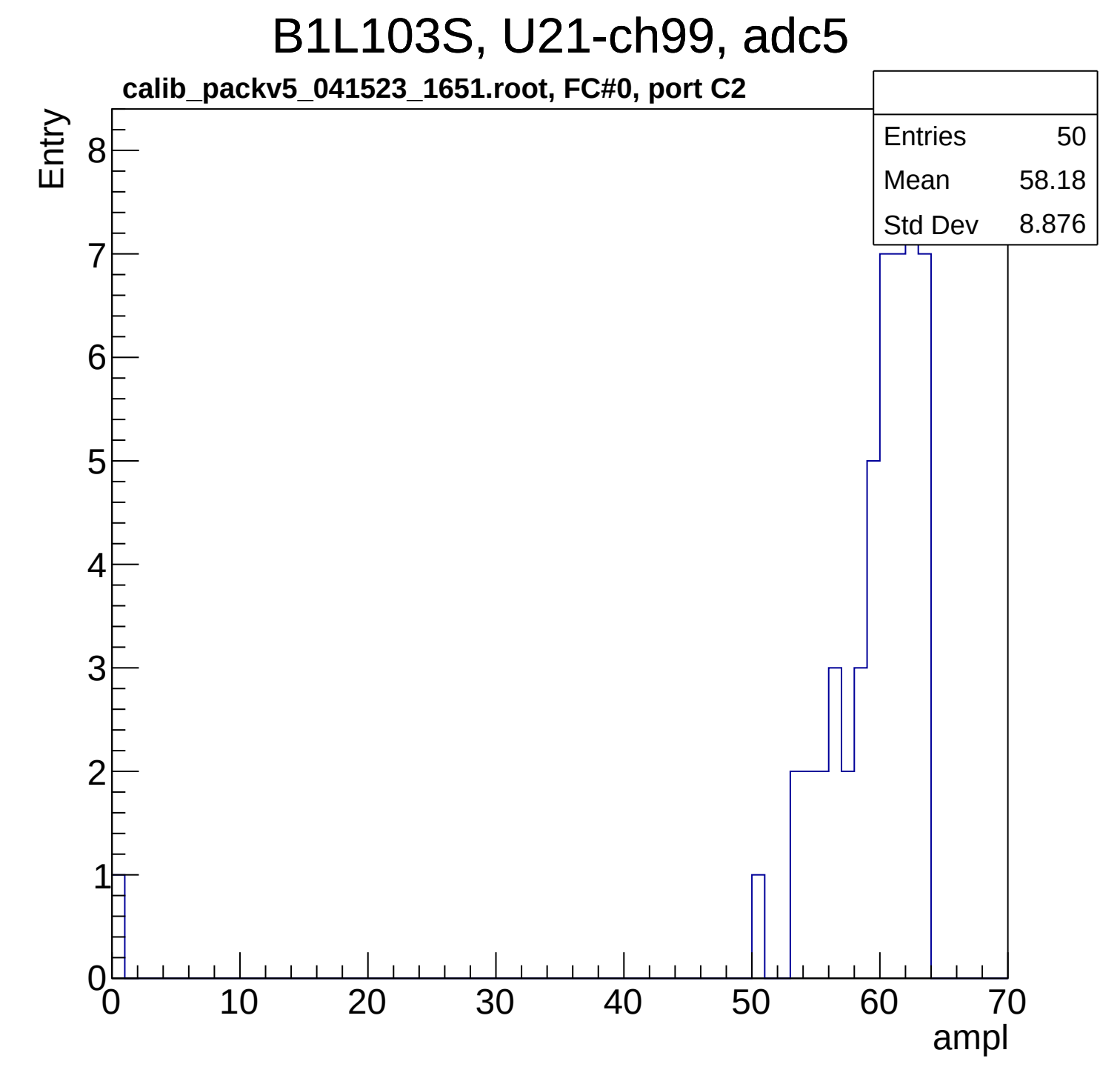
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch99, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 46.1
Std Dev 9.891
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U21-ch99, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 54.96
Std Dev 2.985
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U21-ch99, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 58.18
Std Dev 8.876
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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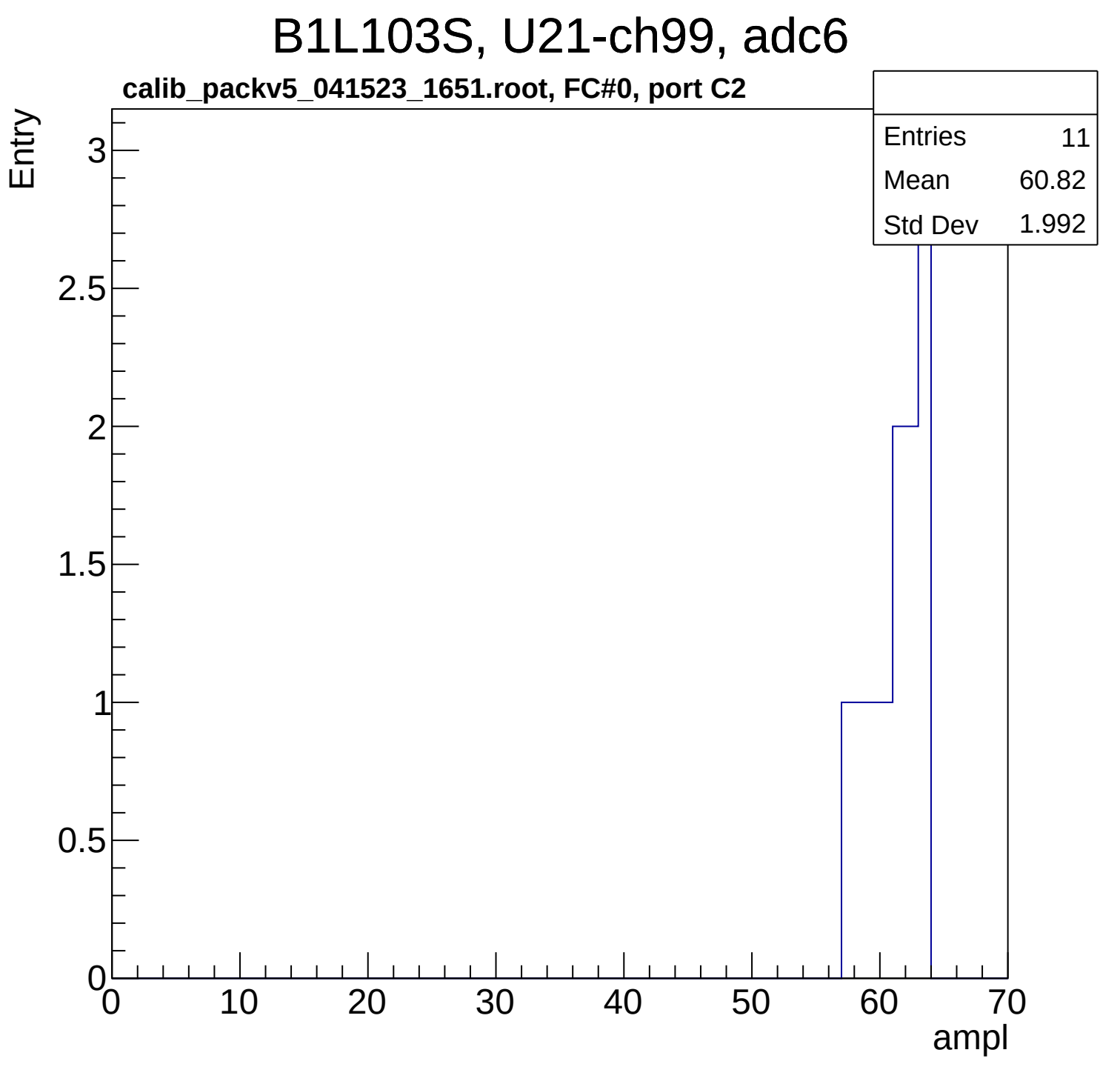
40
50
60
70


B1L103S, U21-ch99, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 60.82
Std Dev 1.992
Entry
ampl
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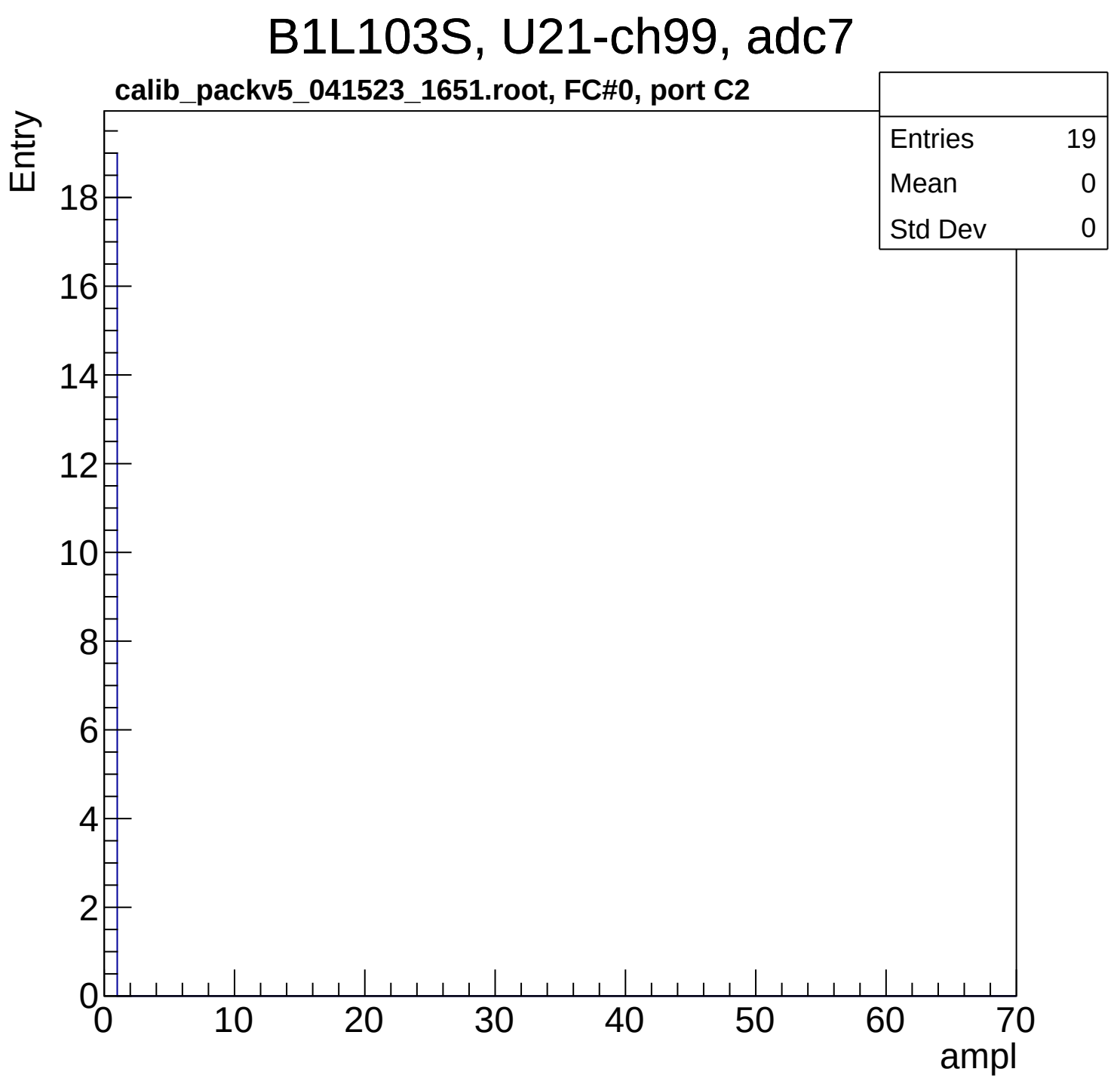
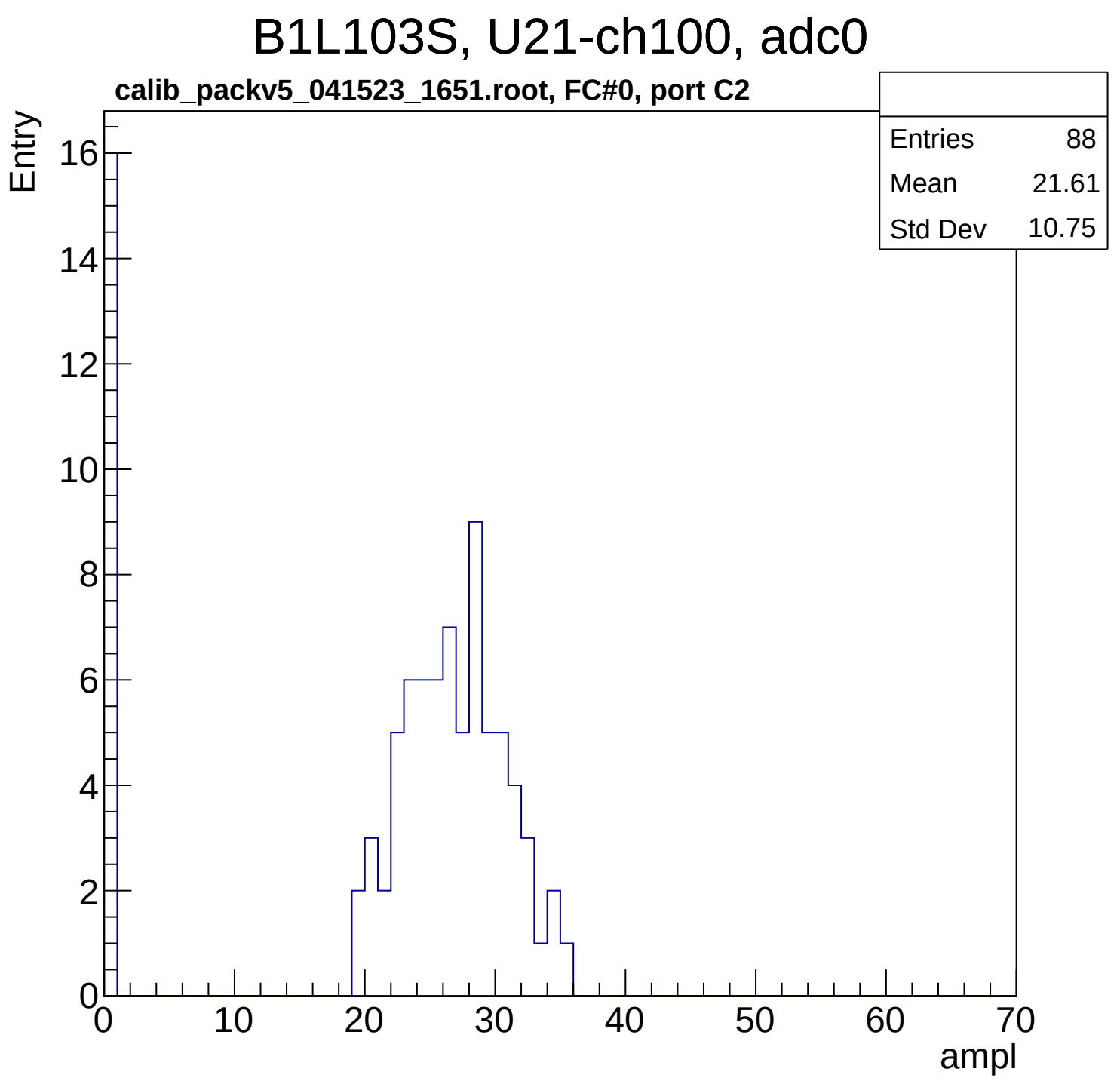
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U21-ch99, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch100, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 21.61
Std Dev 10.75
Entry
ampl
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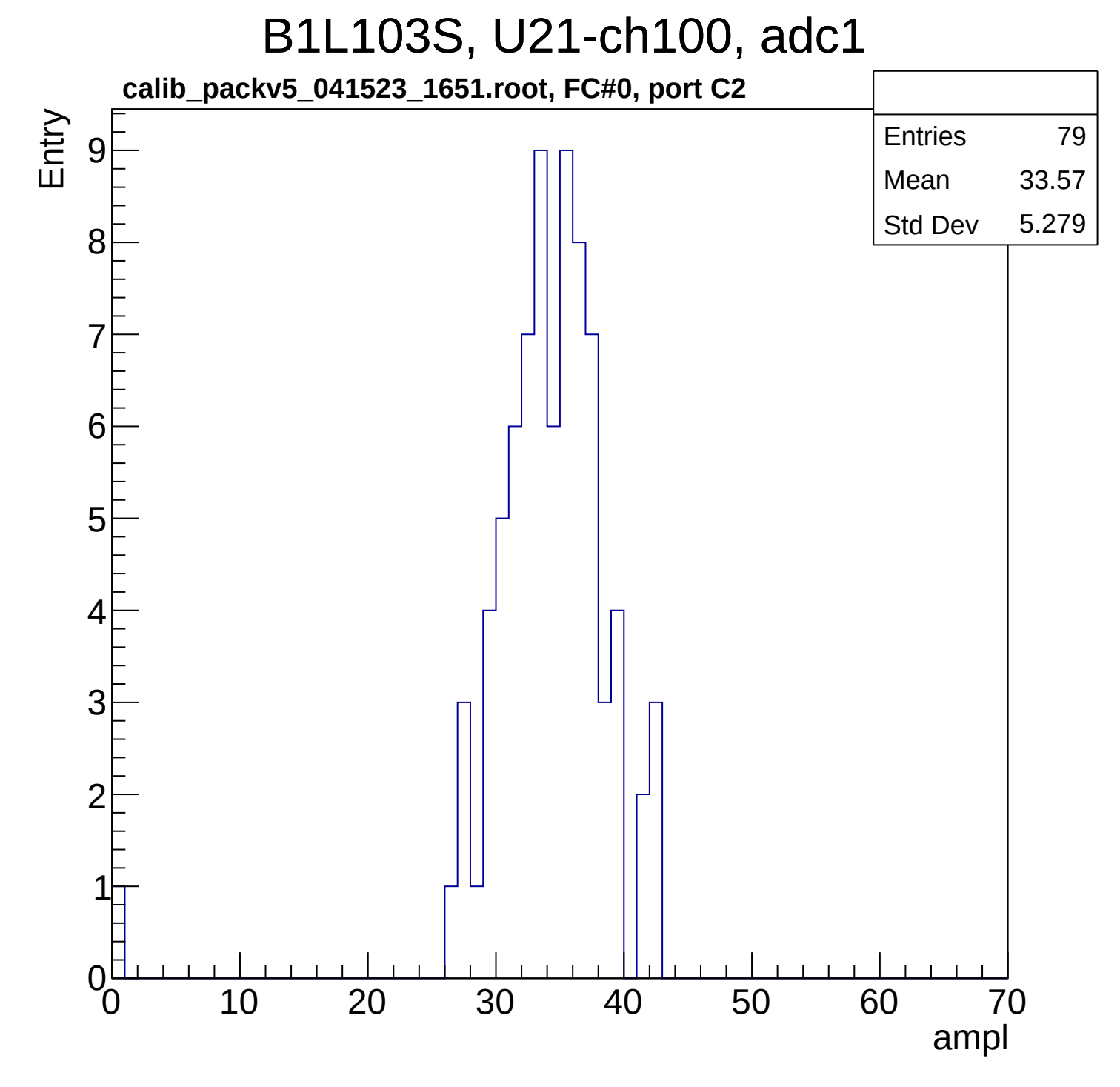
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L103S, U21-ch100, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 33.57
Std Dev 5.279
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
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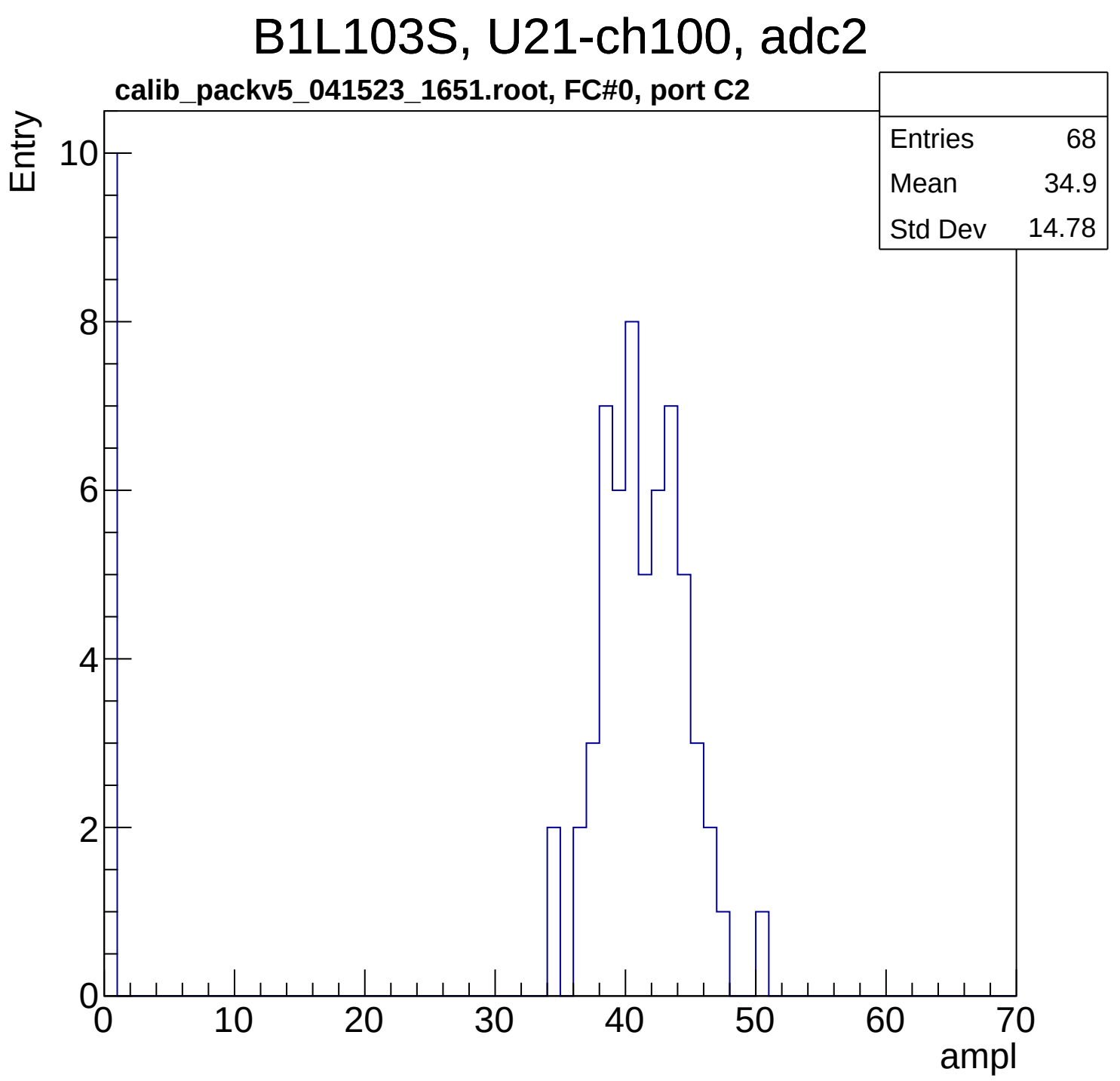
60
70


B1L103S, U21-ch100, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 34.9
Std Dev 14.78
Entry
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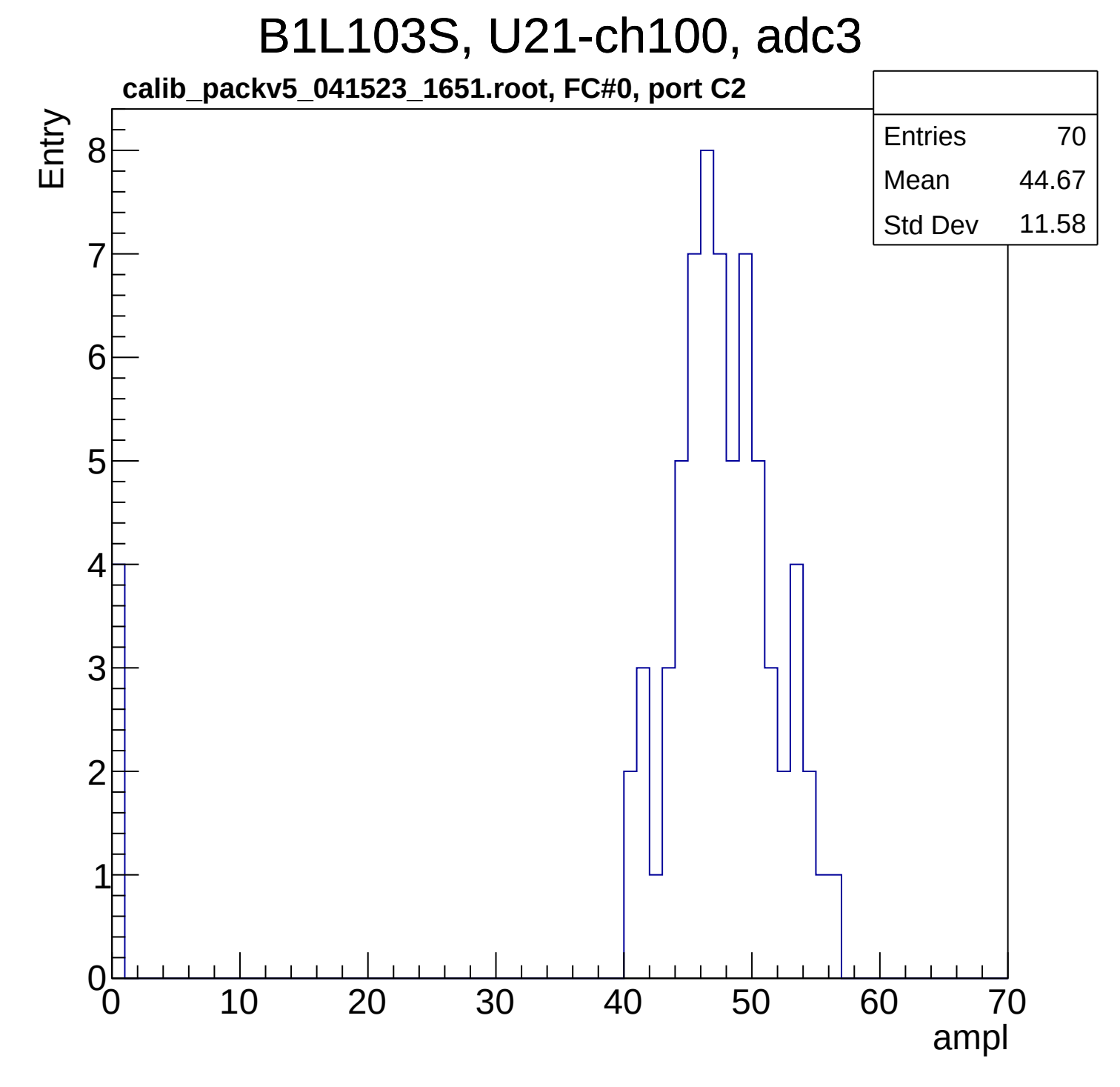
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch100, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 44.67
Std Dev 11.58
Entry
ampl
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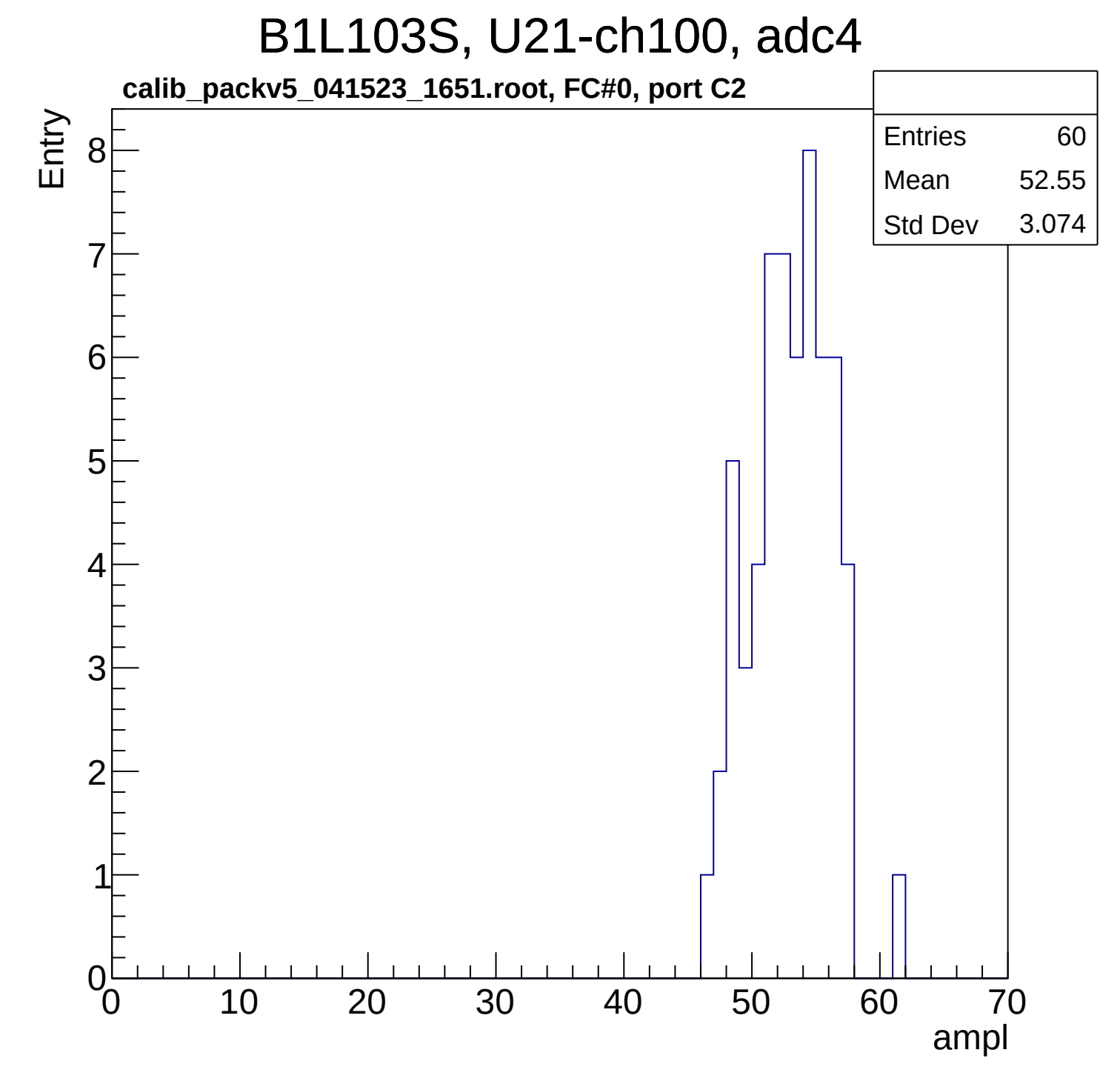
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch100, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 52.55
Std Dev 3.074
Entry
ampl
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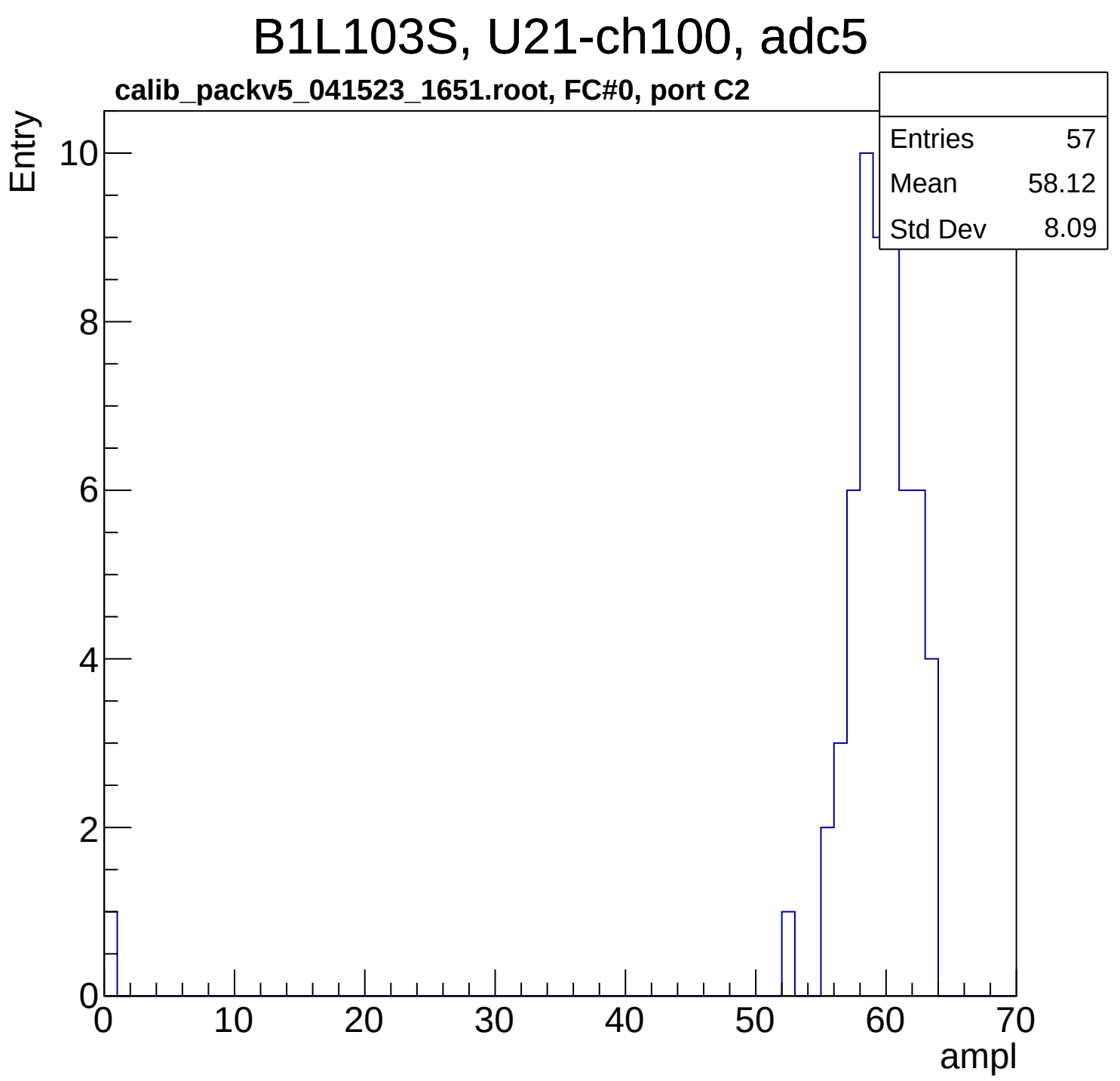
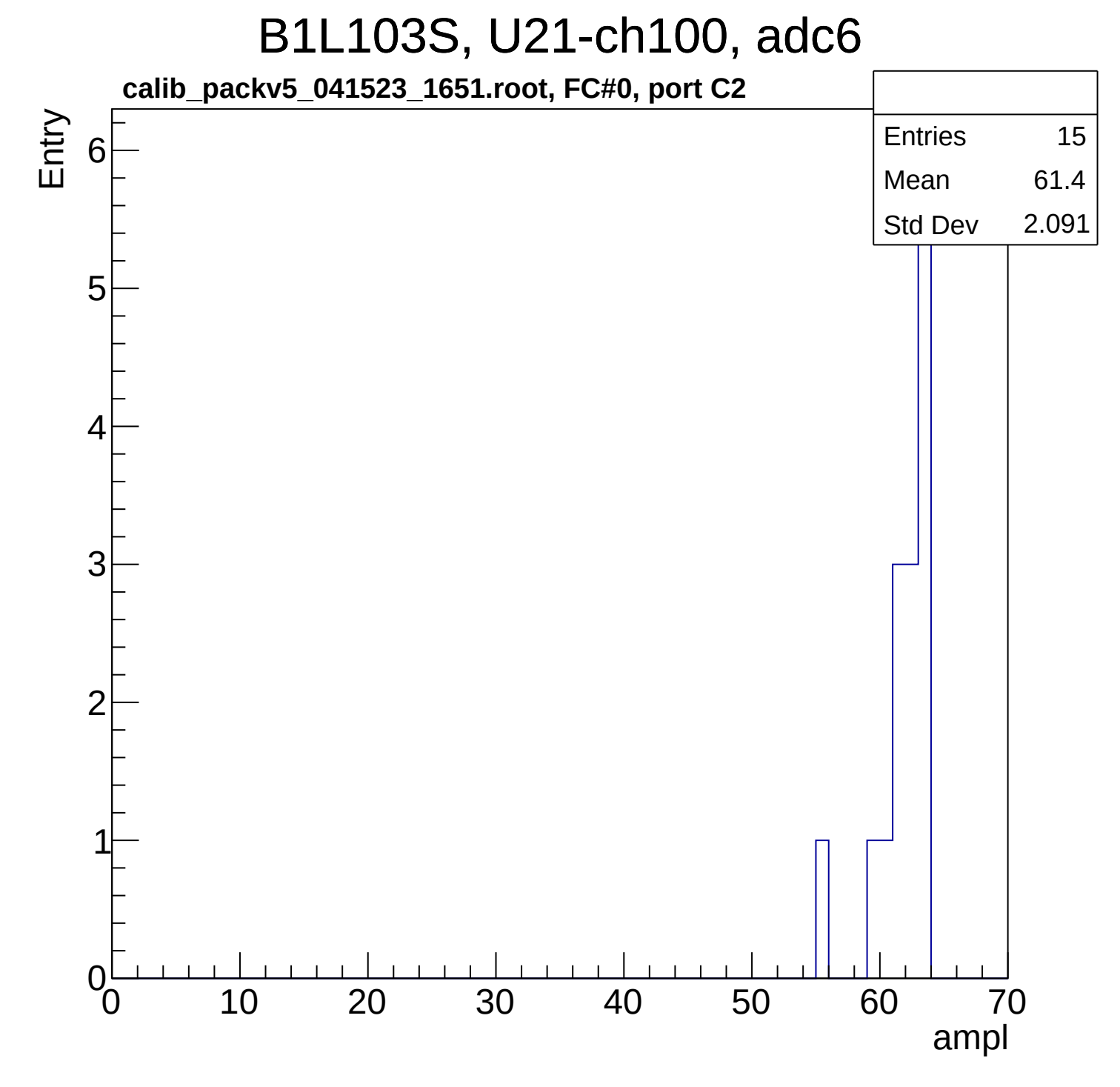
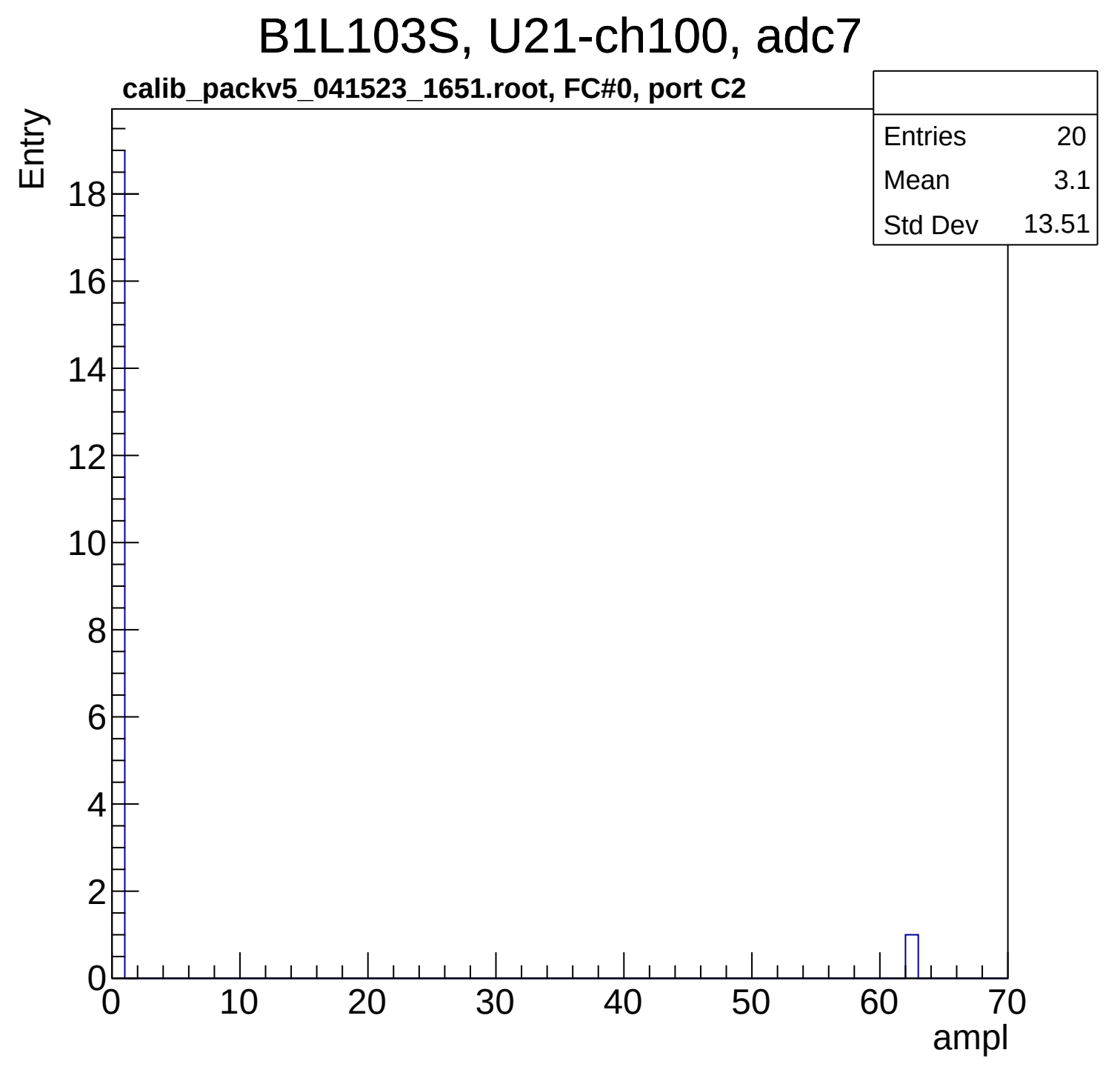
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch100, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 58.12
Std Dev 8.09
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch100, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 61.4
Std Dev 2.091
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch100, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
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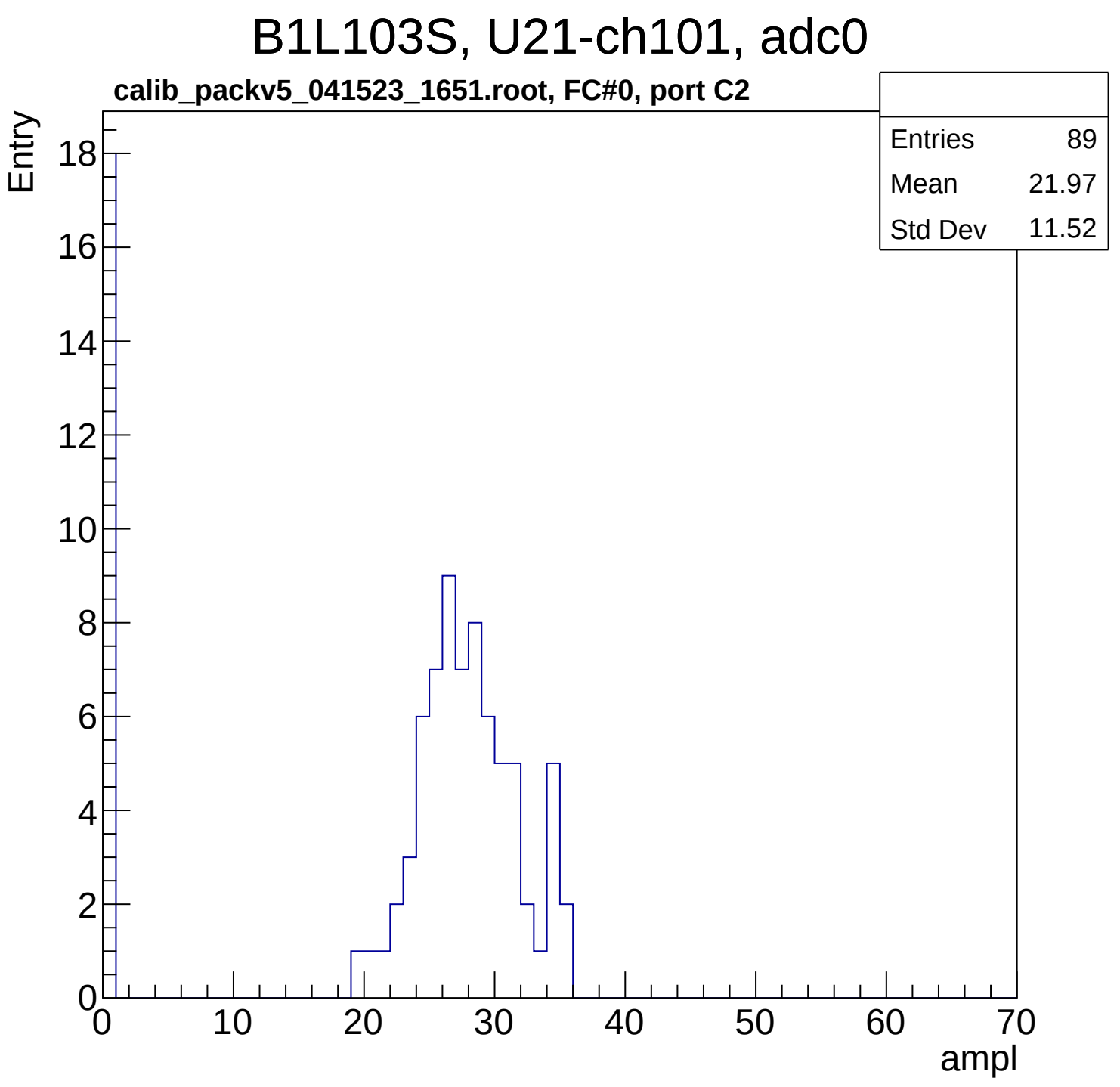
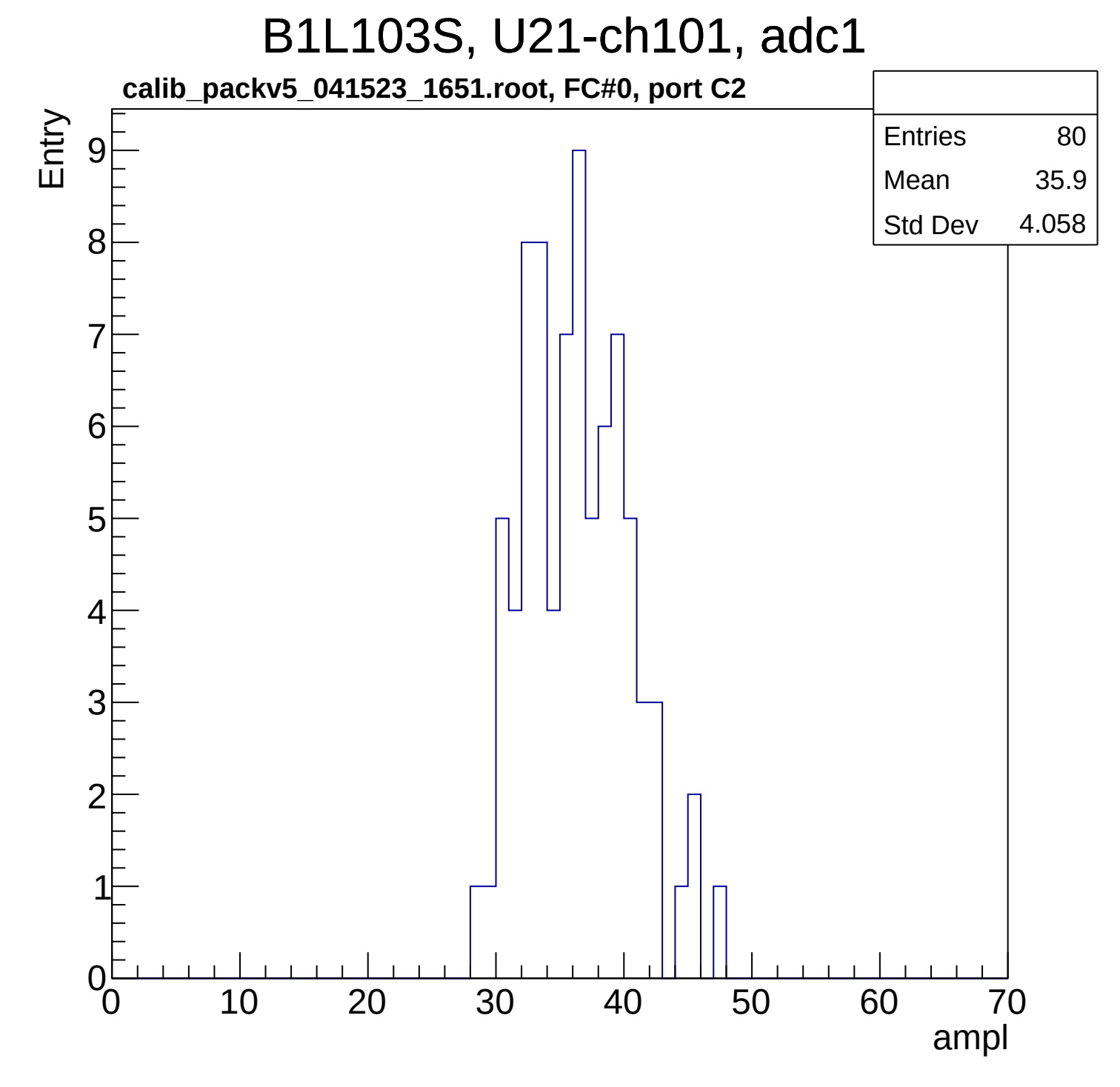
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch101, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 21.97
Std Dev 11.52
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch101, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 35.9
Std Dev 4.058
Entry
ampl
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2
3
4
5
6
7
8
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40
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60
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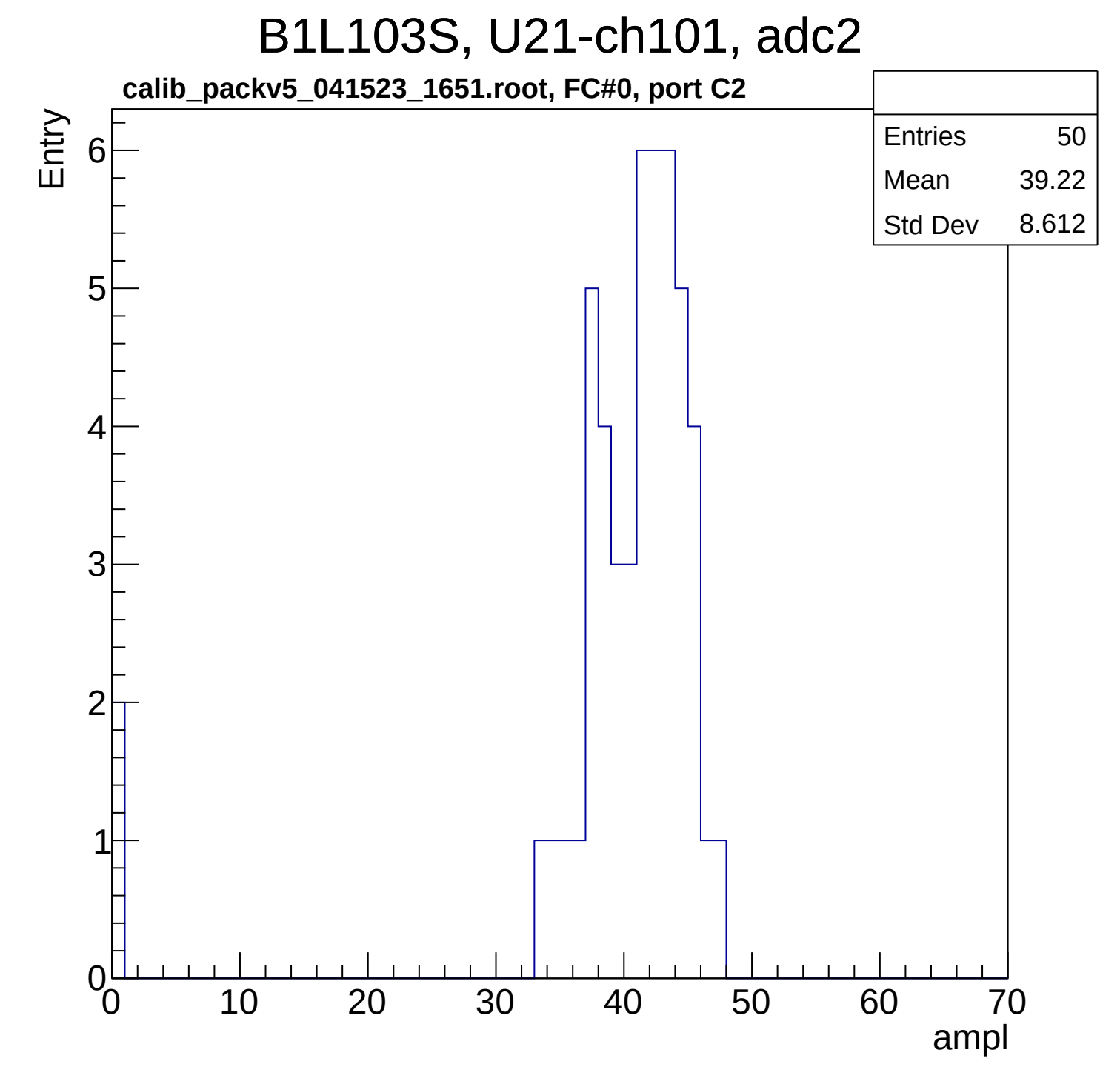
B1L103S, U21-ch101, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 39.22
Std Dev 8.612
Entry
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4
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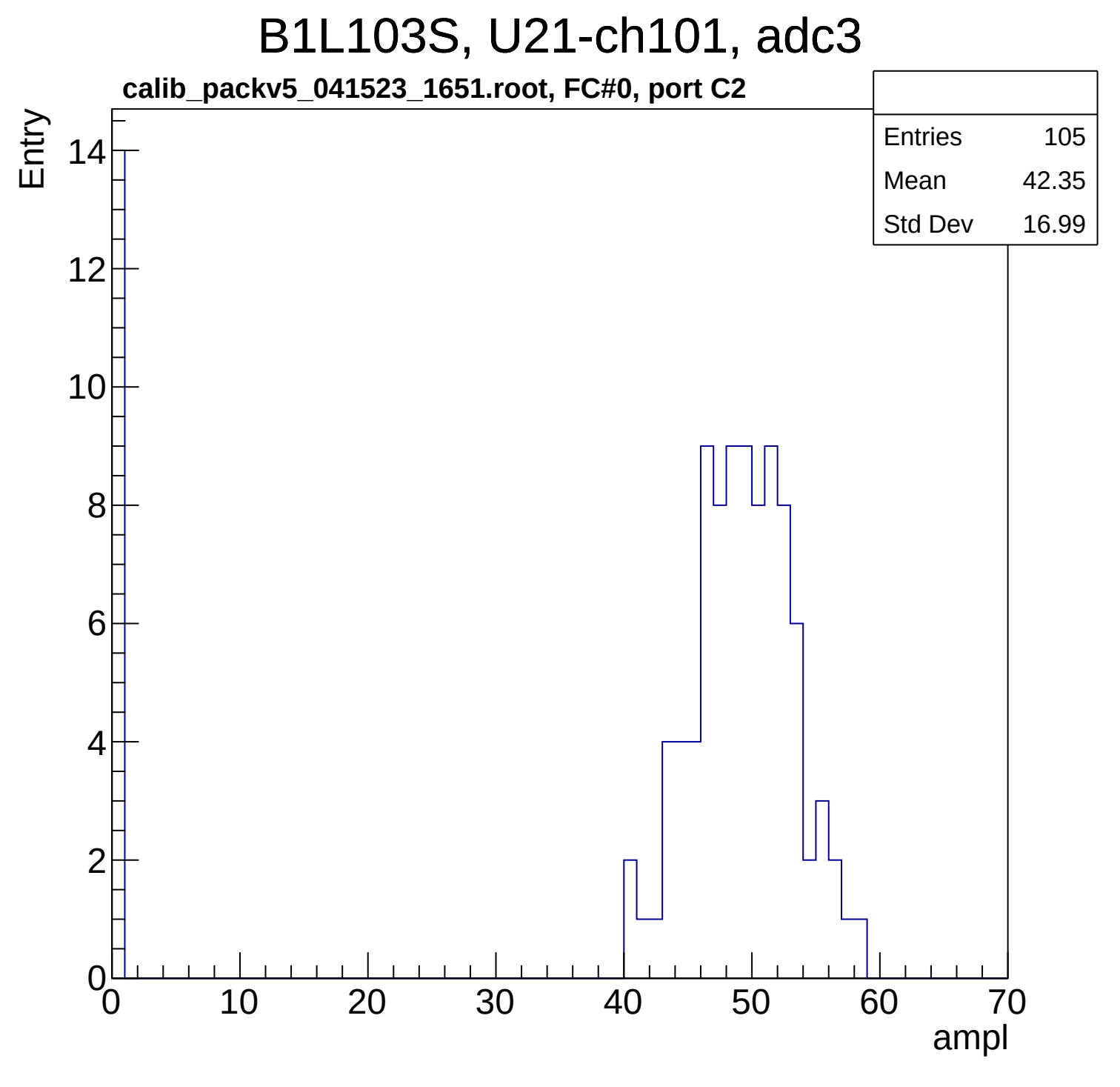
ampl


B1L103S, U21-ch101, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 105
Mean 42.35
Std Dev 16.99
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14
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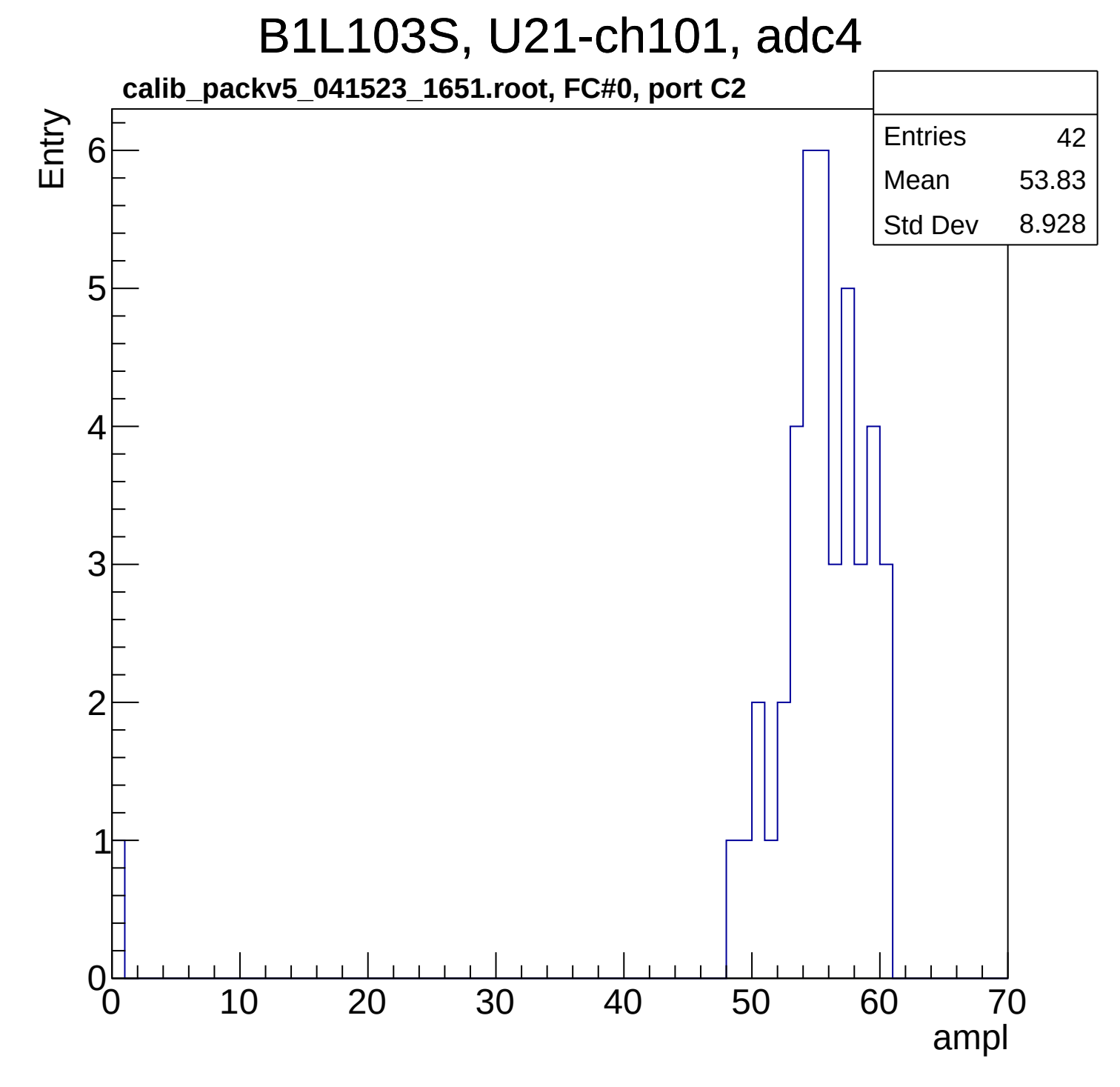
70
ampl


B1L103S, U21-ch101, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 53.83
Std Dev 8.928
Entry
ampl
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2
3
4
5
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0
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40
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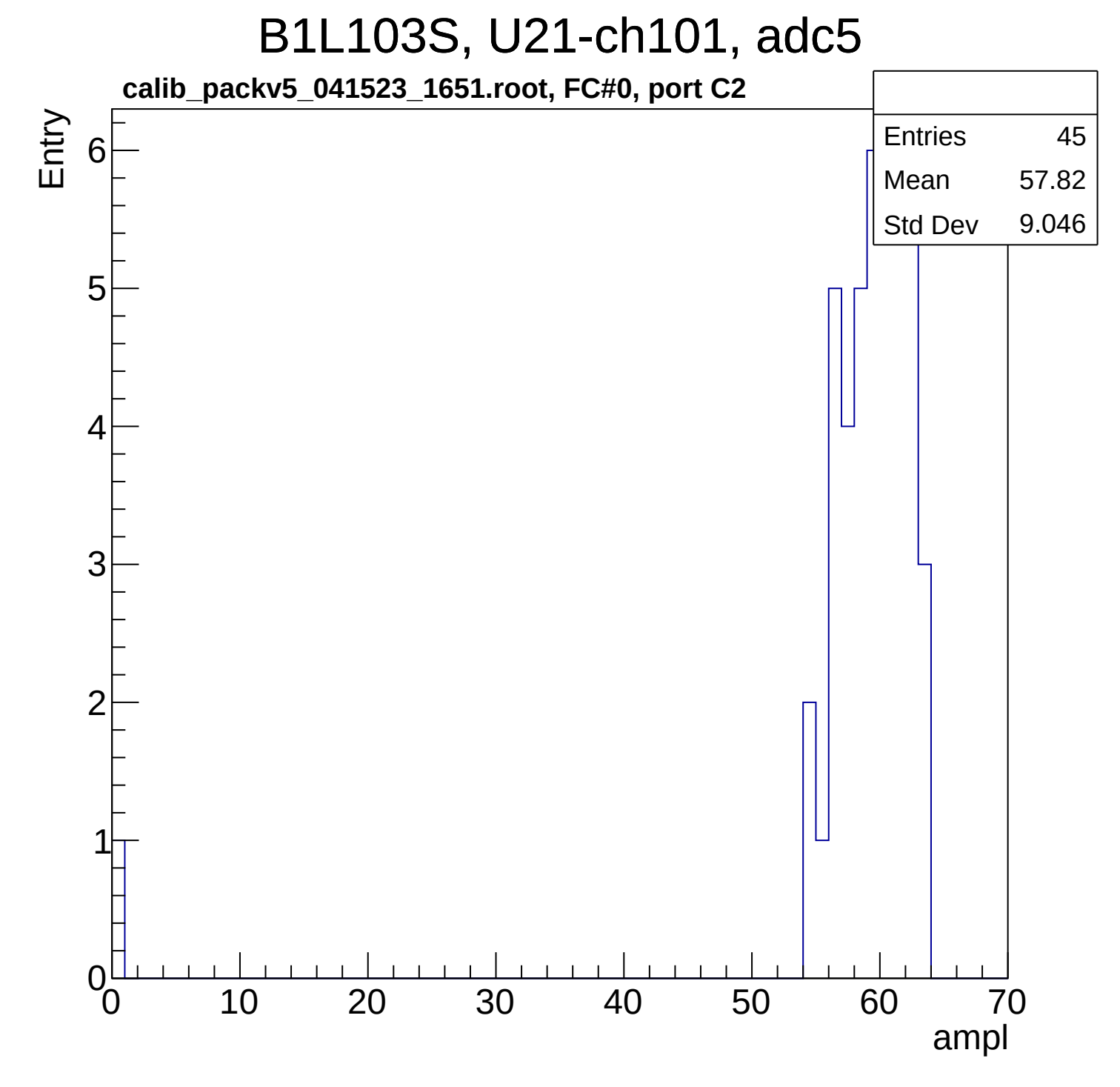
B1L103S, U21-ch101, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 57.82
Std Dev 9.046
Entry
ampl
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0
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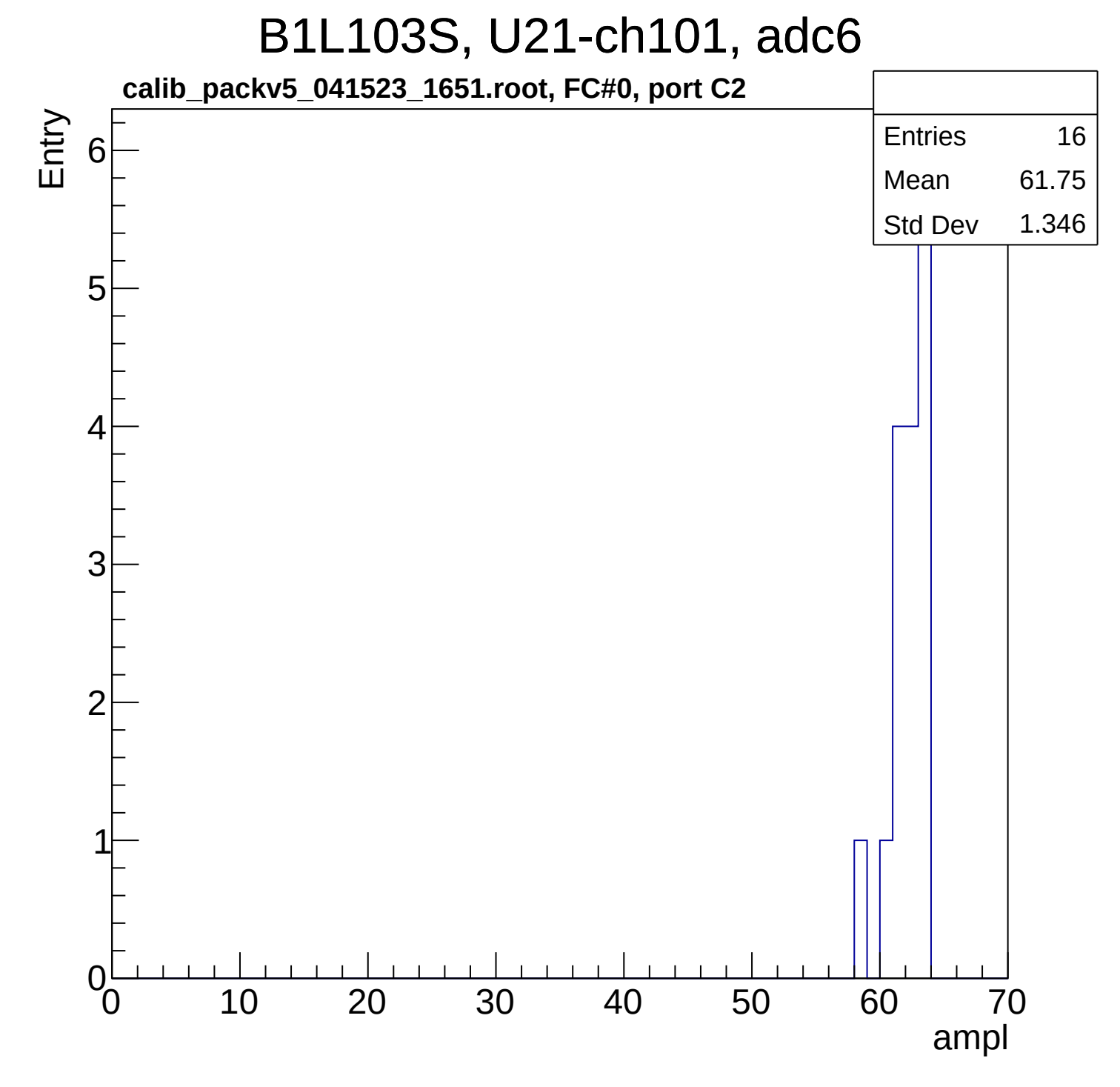
B1L103S, U21-ch101, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 61.75
Std Dev 1.346
Entry
ampl
0
1
2
3
4
5
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0
10
20
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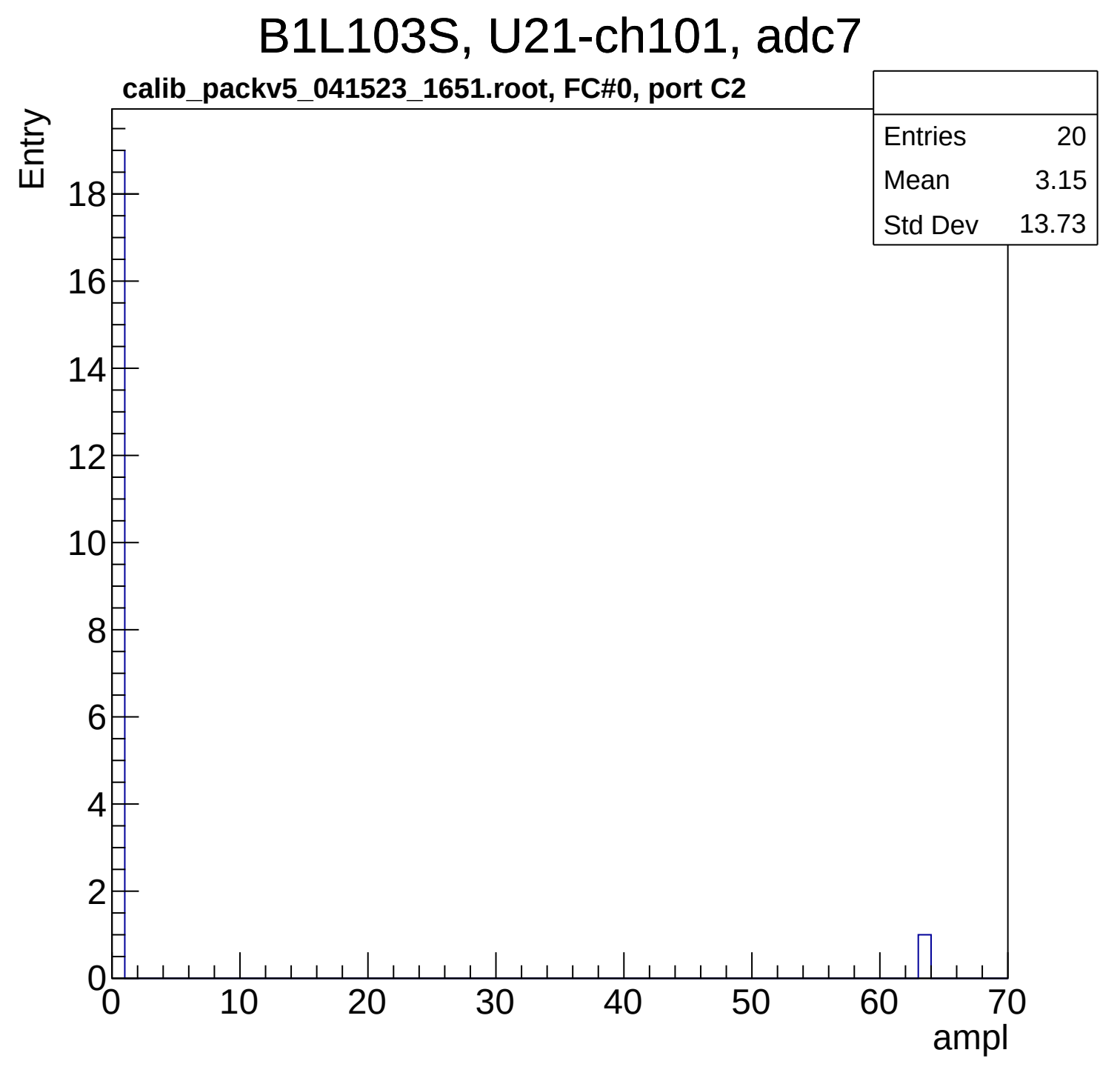
40
50
60
70


B1L103S, U21-ch101, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
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4
6
8
10
12
14
16
18
0
10
20
30
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50
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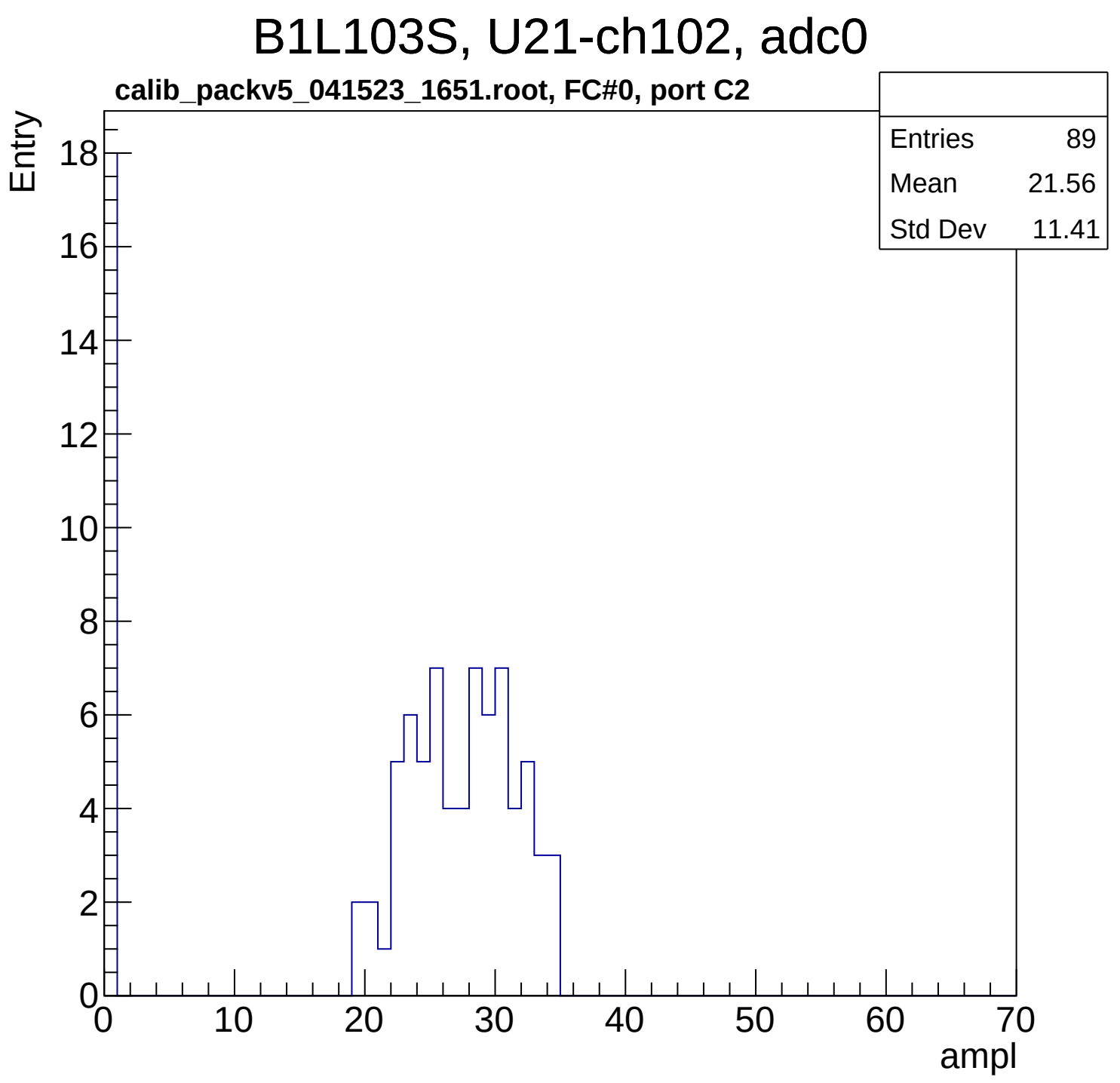
70
ampl


B1L103S, U21-ch102, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 21.56
Std Dev 11.41
Entry
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6
8
10
12
14
16
18
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10
20
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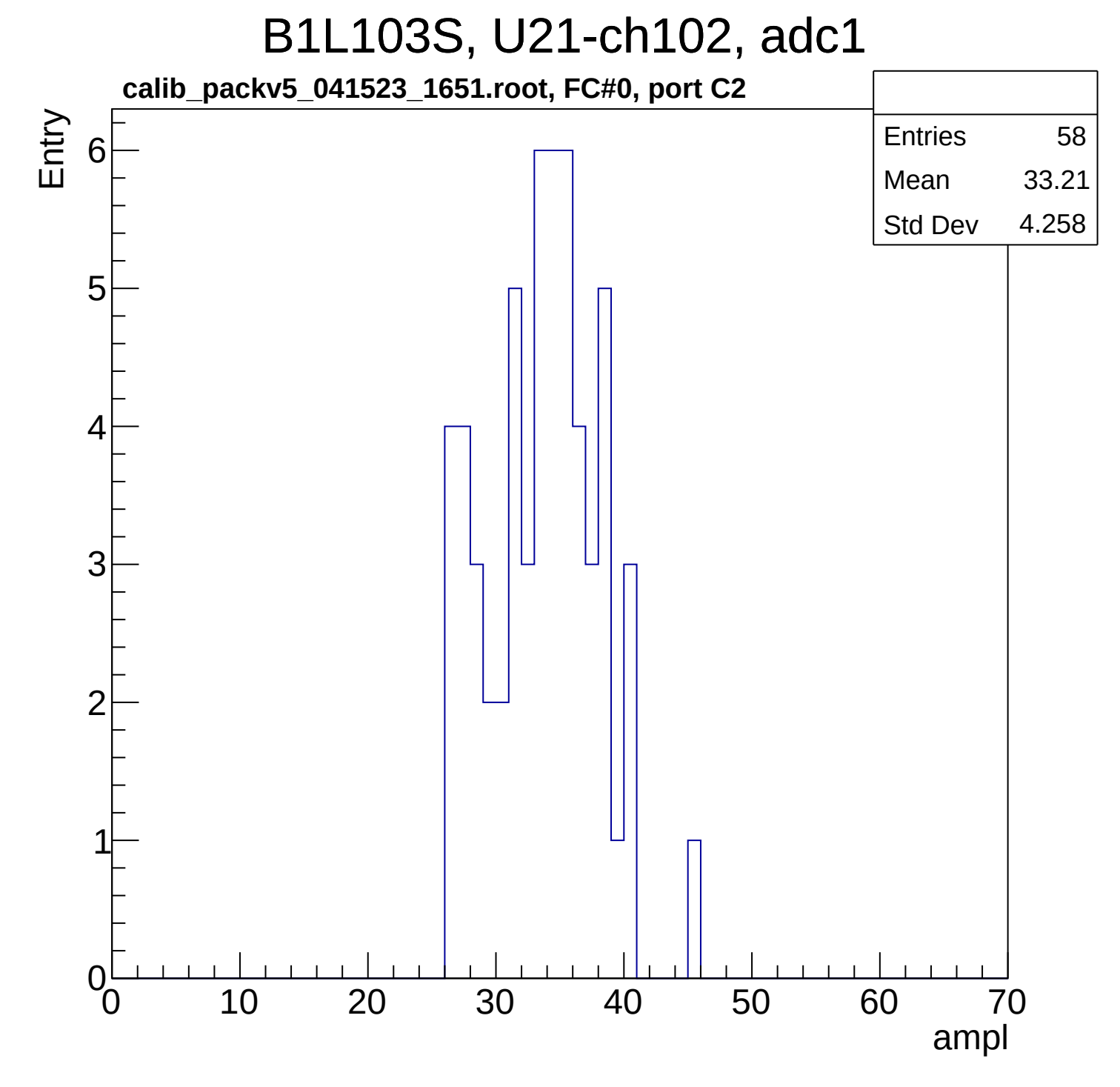
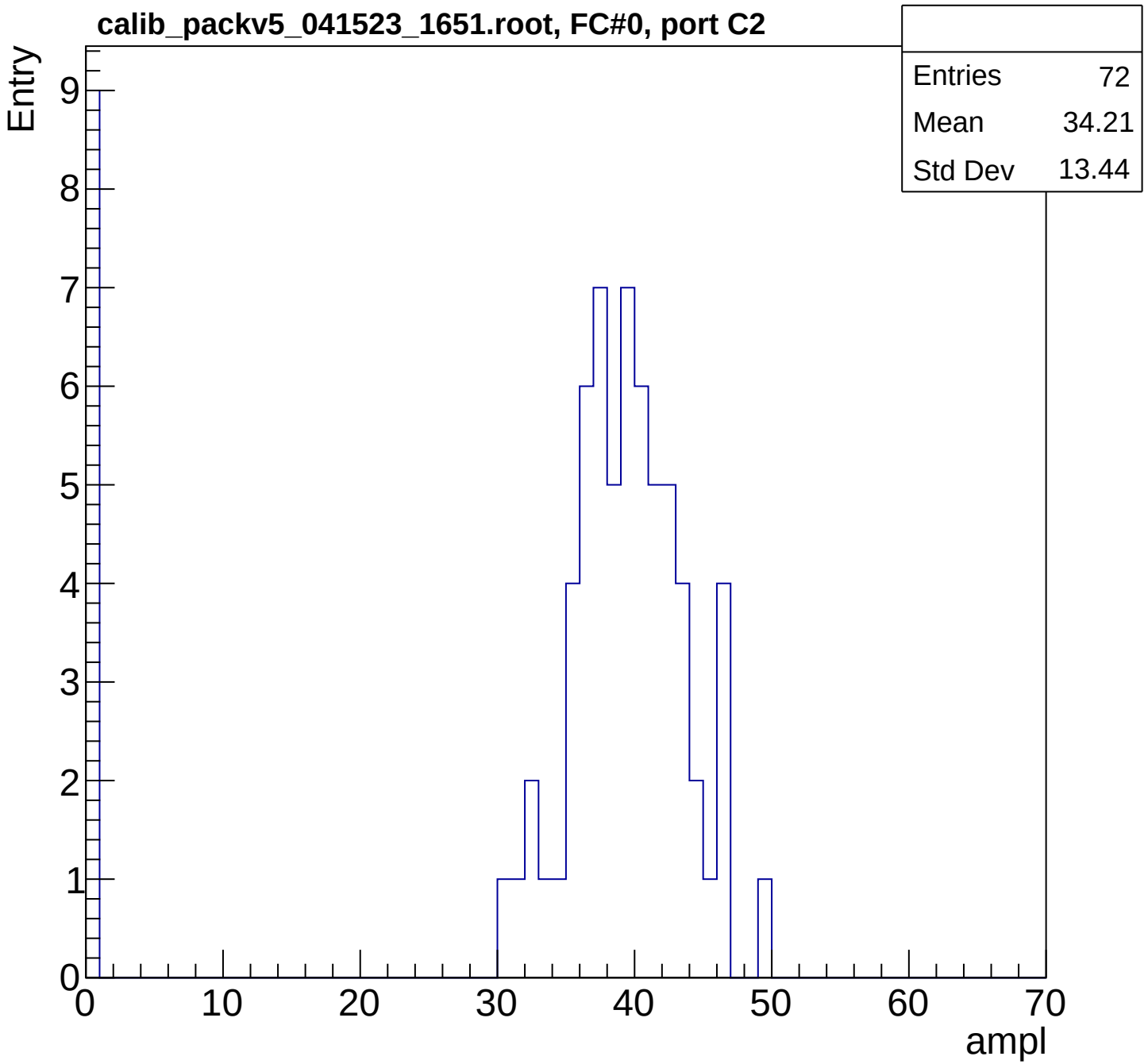
50
60
70
ampl


B1L103S, U21-ch102, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 33.21
Std Dev 4.258
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U21-ch102, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 34.21
Std Dev 13.44
Entry
ampl
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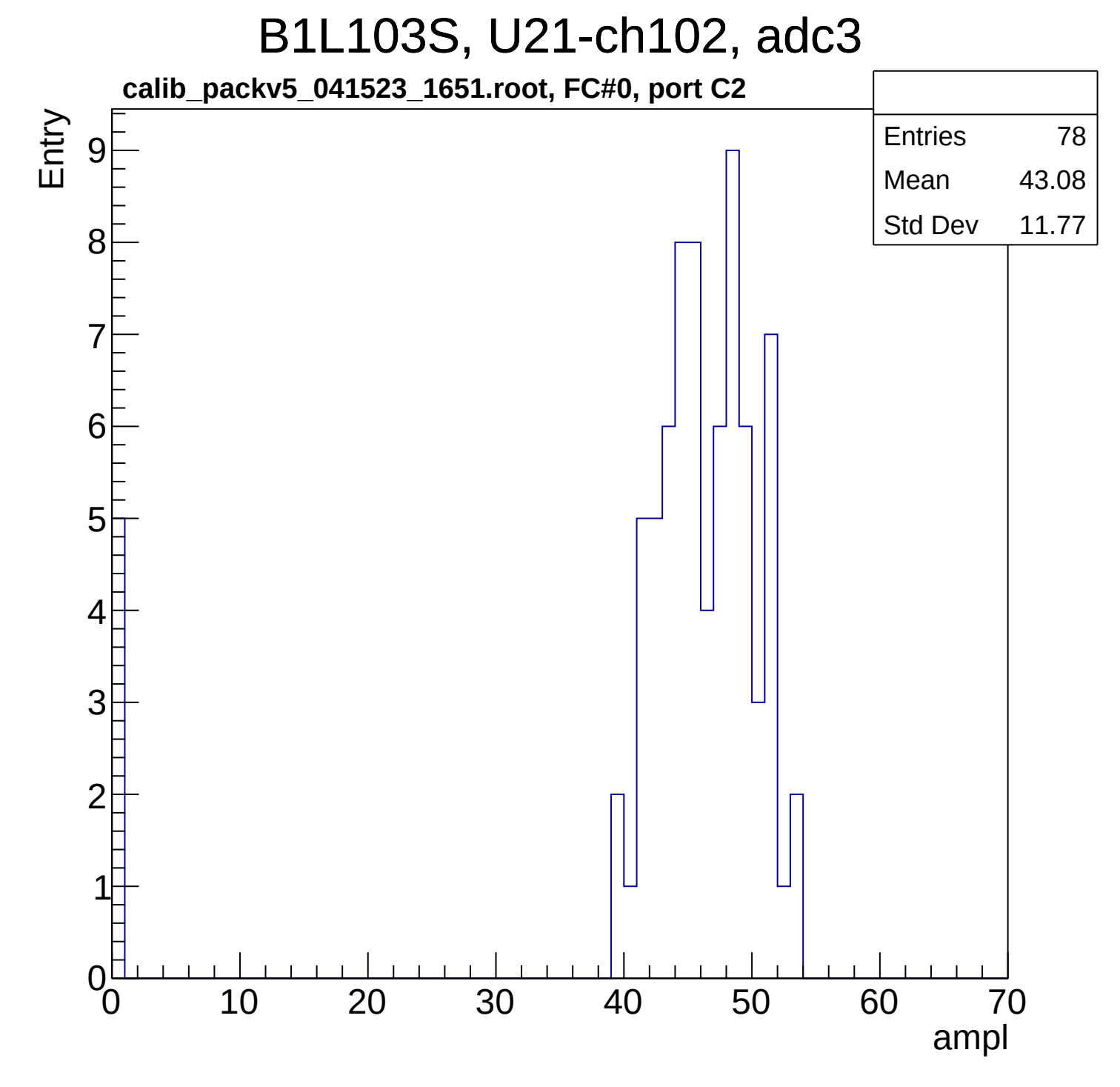
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch102, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 43.08
Std Dev 11.77
Entry
ampl
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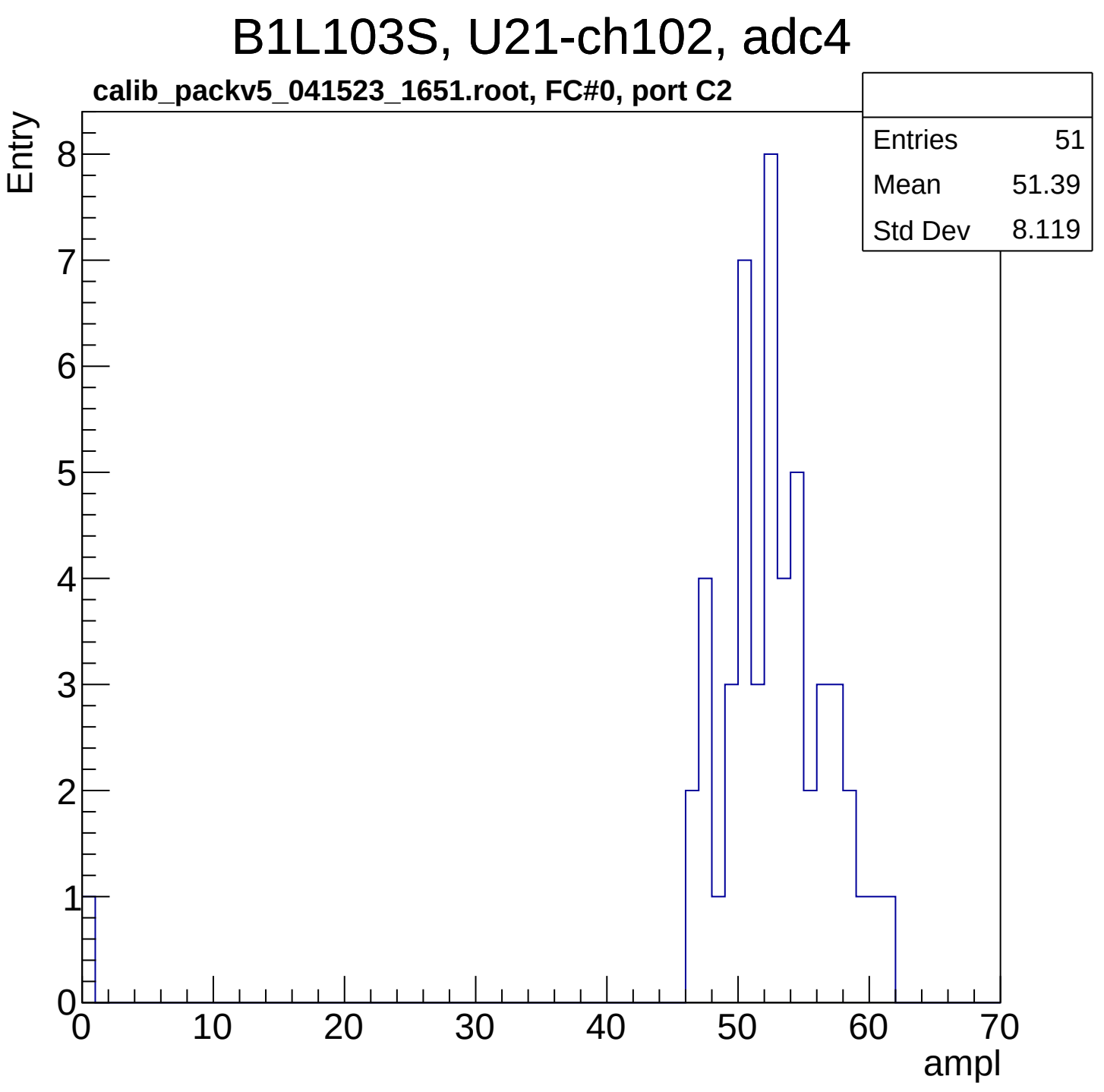
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch102, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 51.39
Std Dev 8.119
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
50
60
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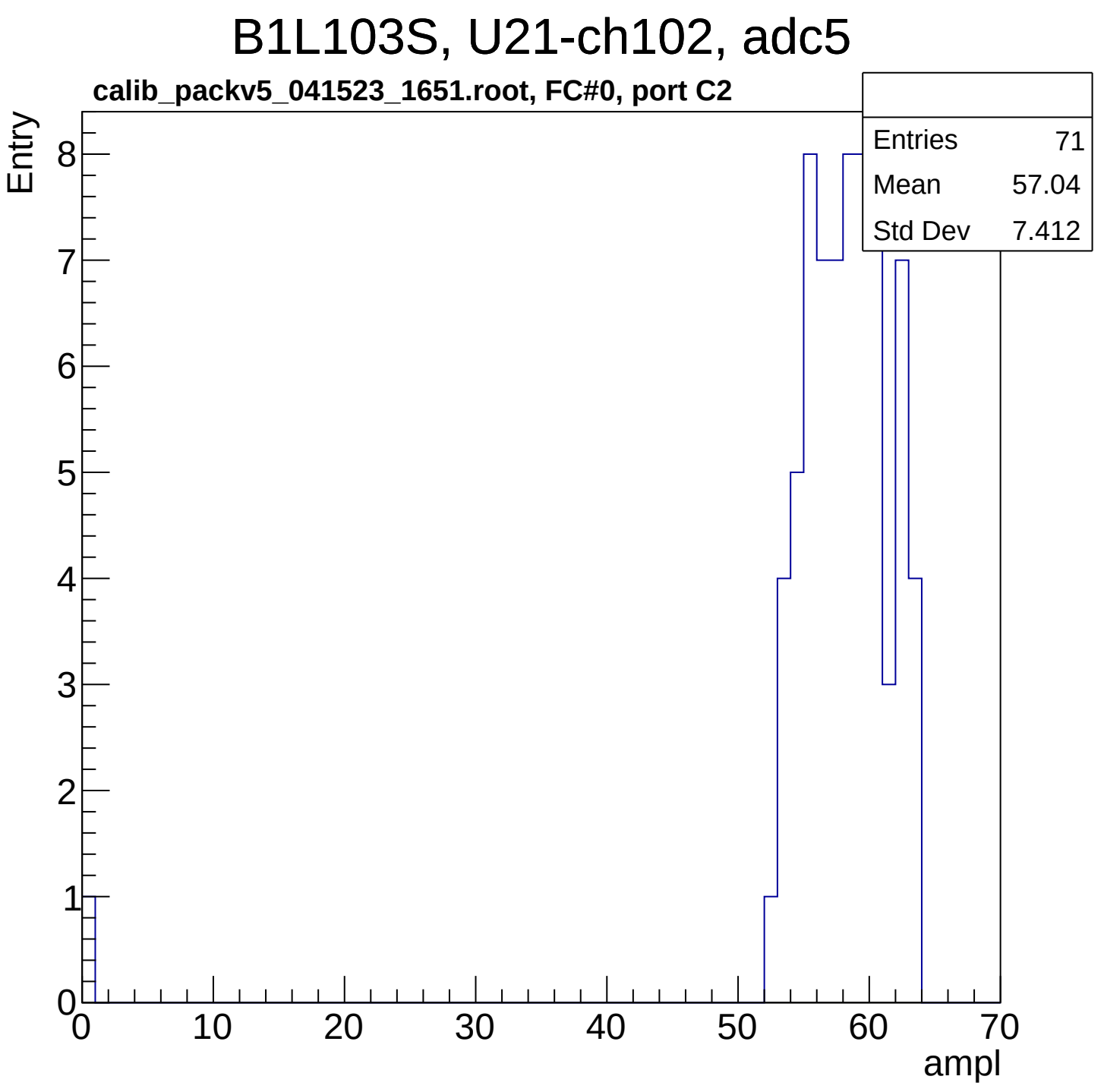
B1L103S, U21-ch102, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 57.04
Std Dev 7.412
Entry
ampl
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2
3
4
5
6
7
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0
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60
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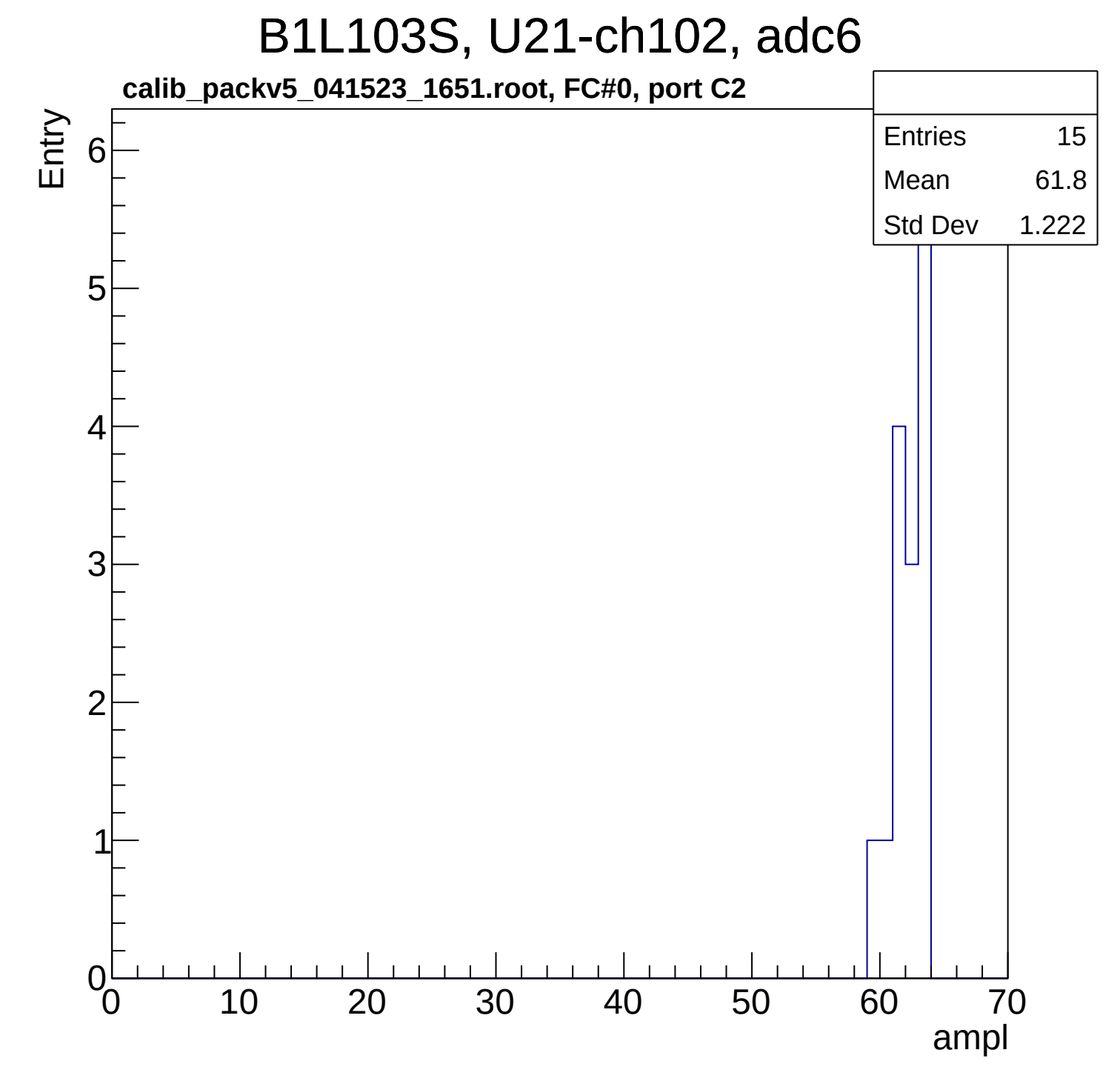
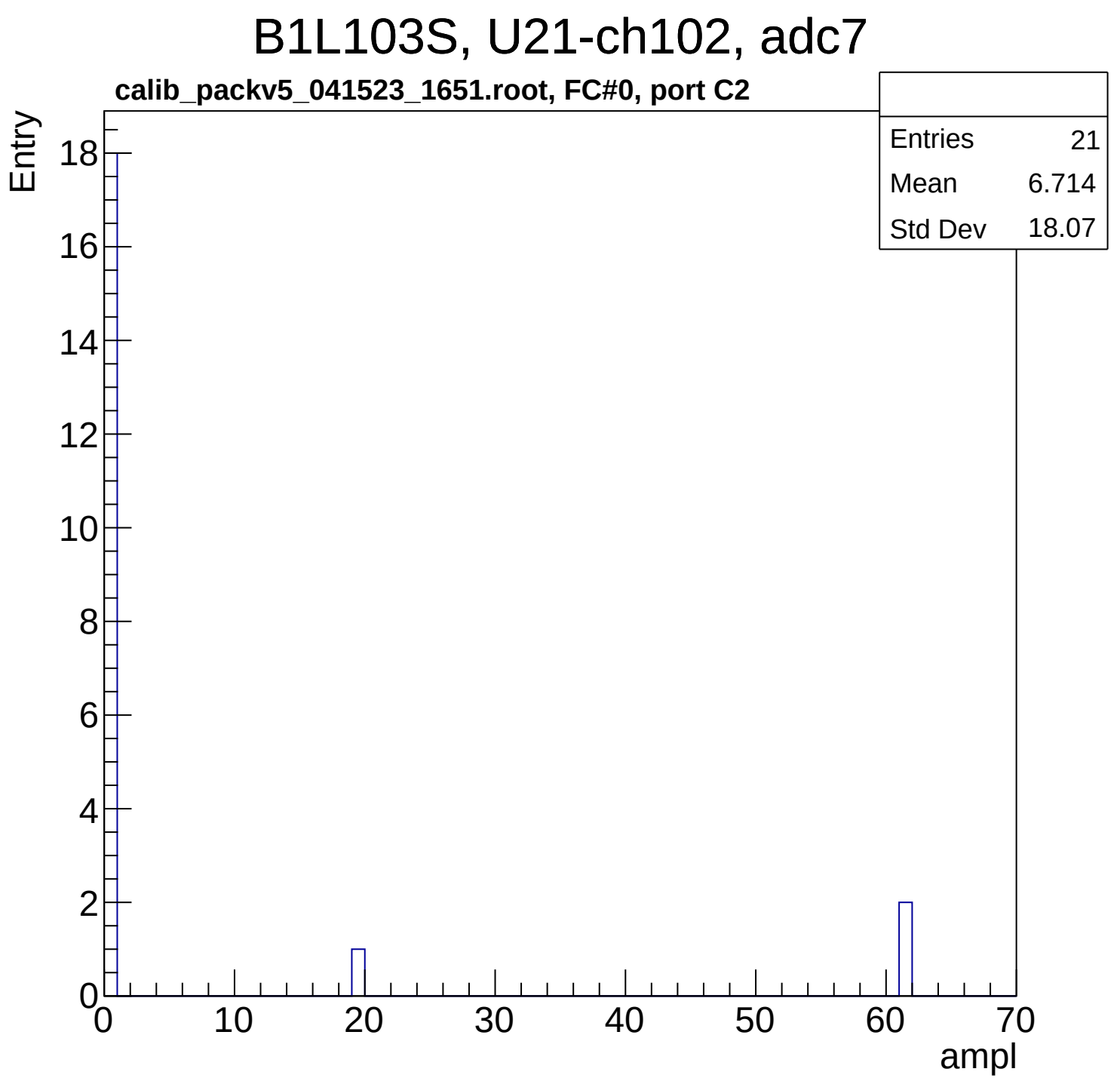

B1L103S, U21-ch102, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 61.8
Std Dev 1.222
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U21-ch102, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 6.714
Std Dev 18.07
Entry
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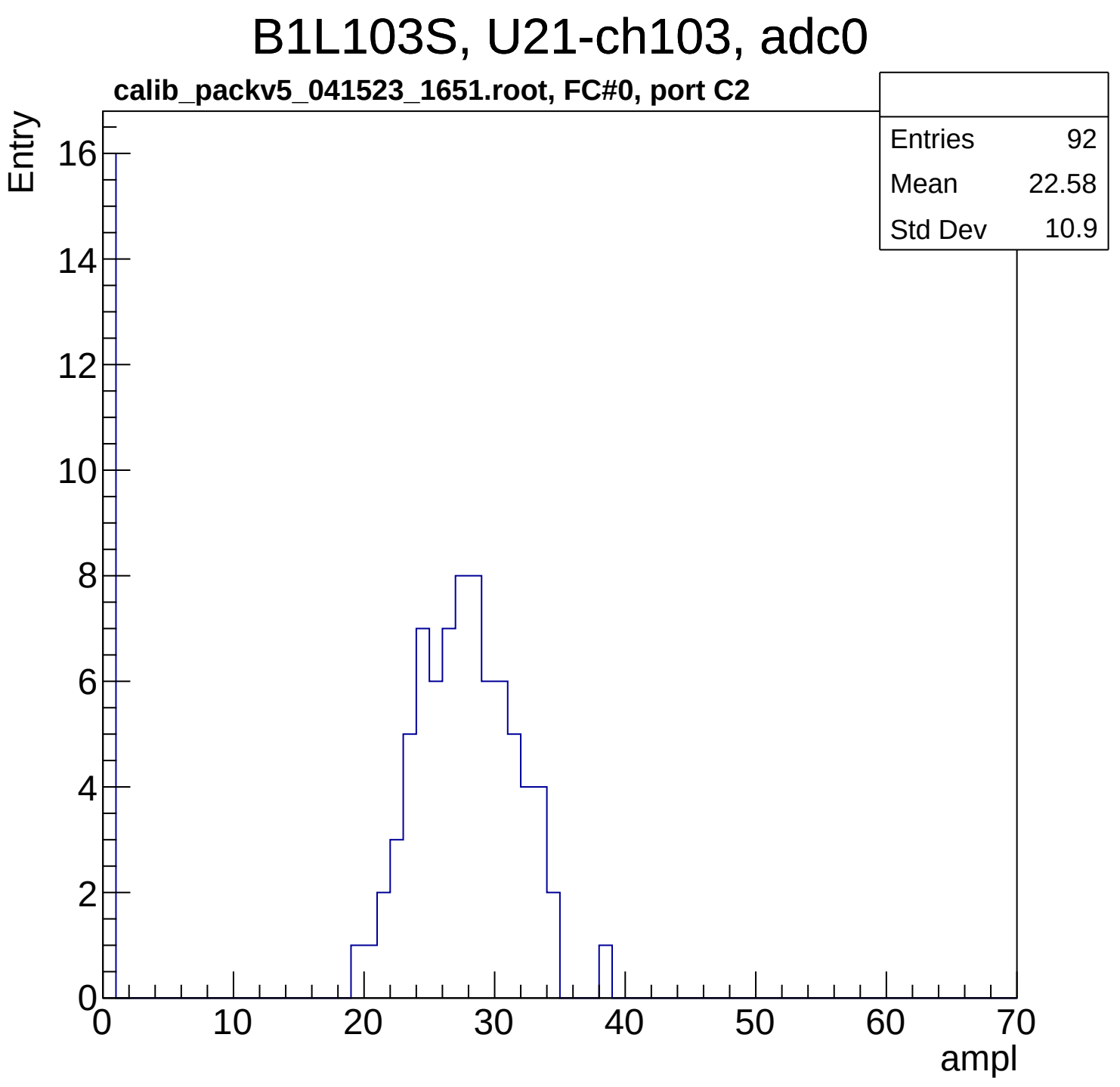
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch103, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 22.58
Std Dev 10.9
Entry
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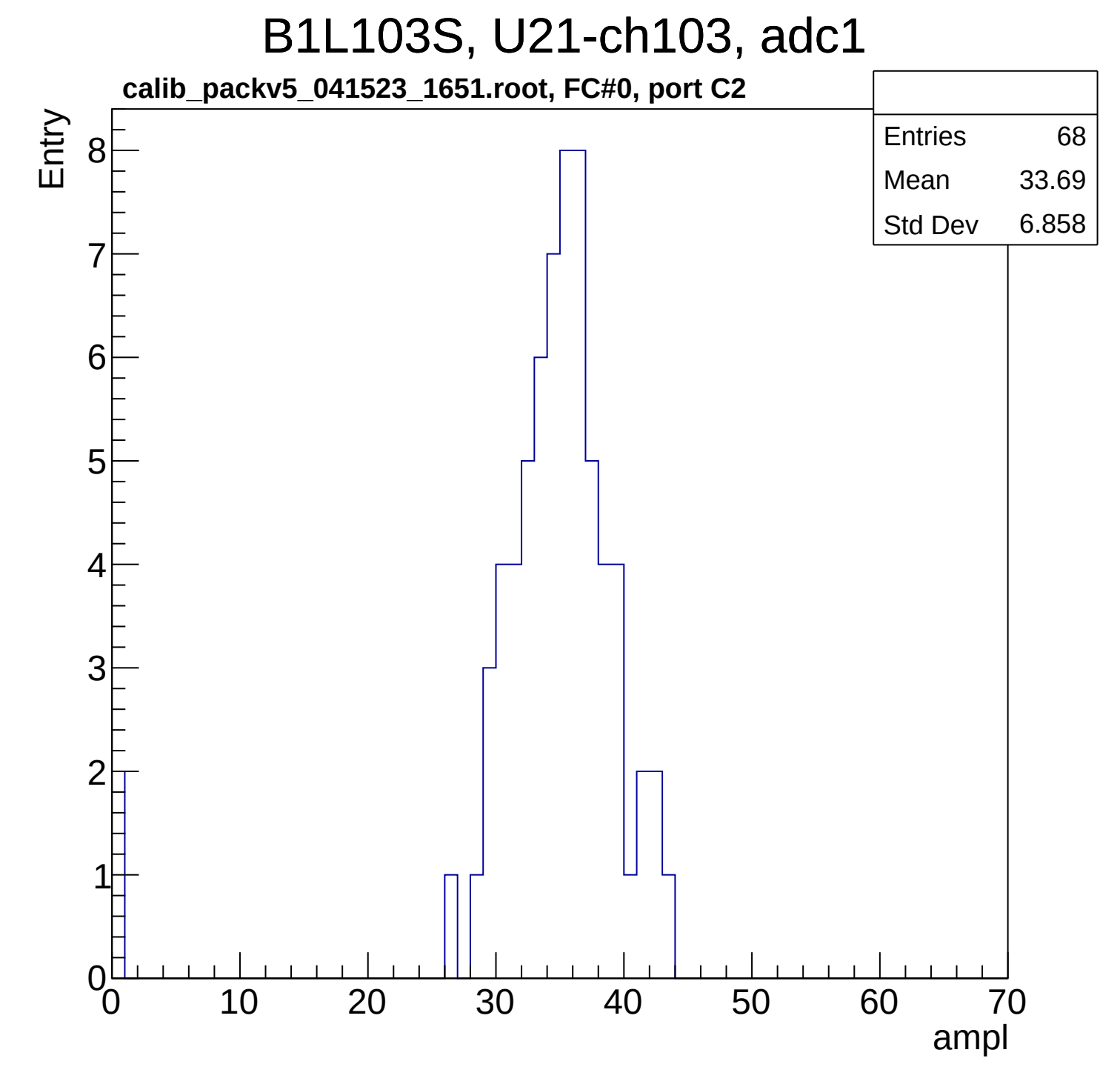
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch103, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 33.69
Std Dev 6.858
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
50
60
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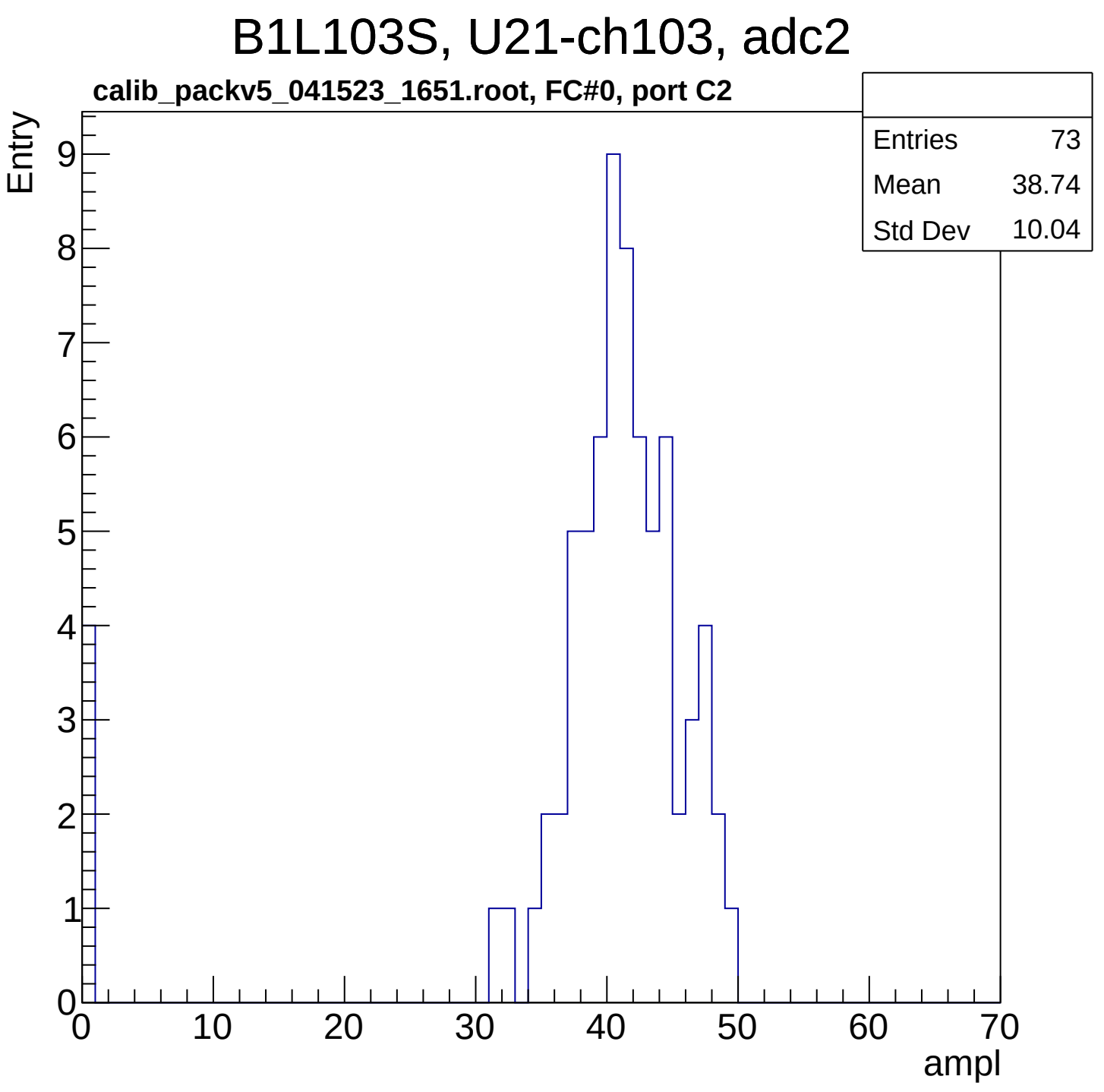
B1L103S, U21-ch103, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 38.74
Std Dev 10.04
Entry
ampl
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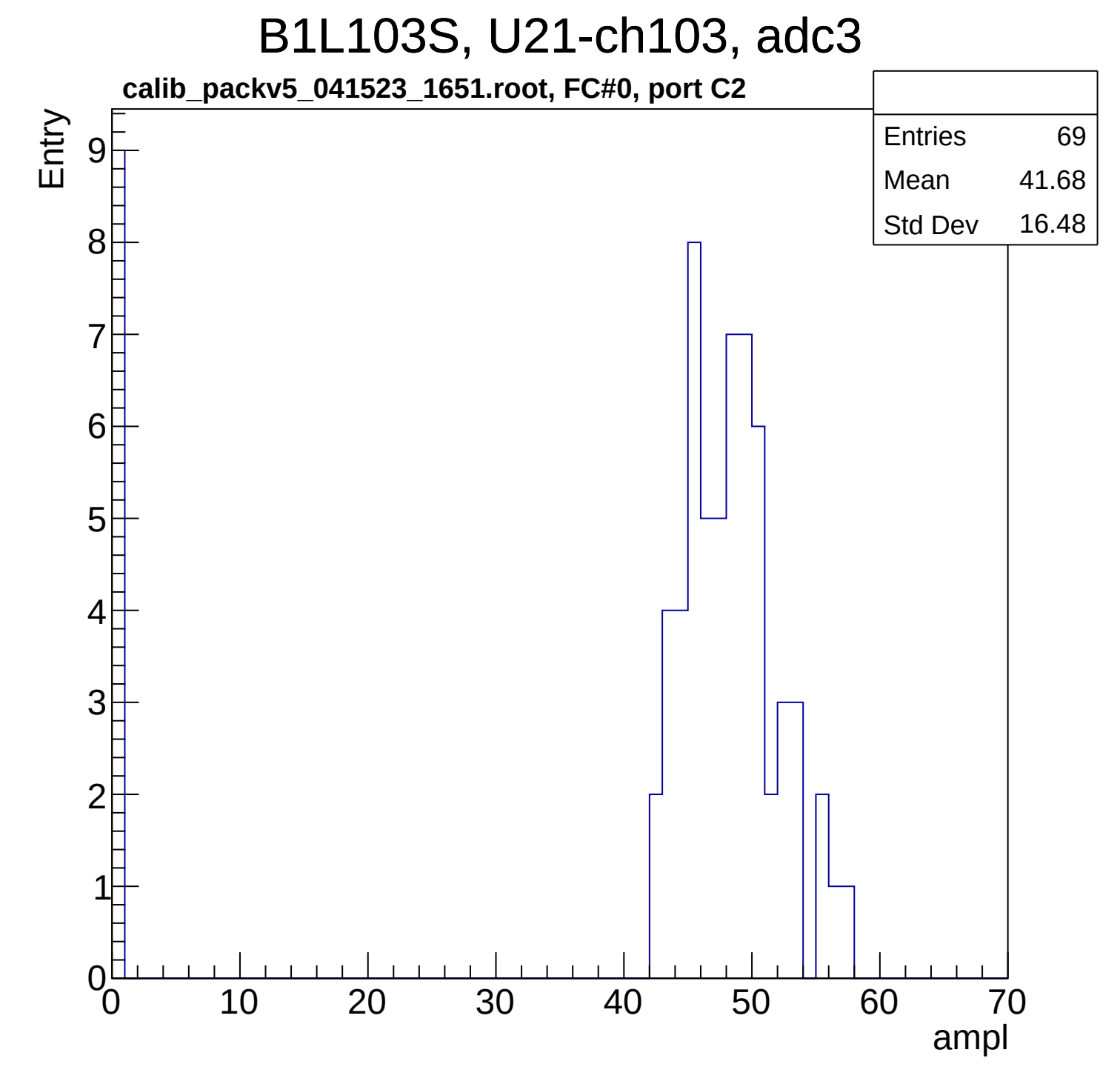
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch103, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 41.68
Std Dev 16.48
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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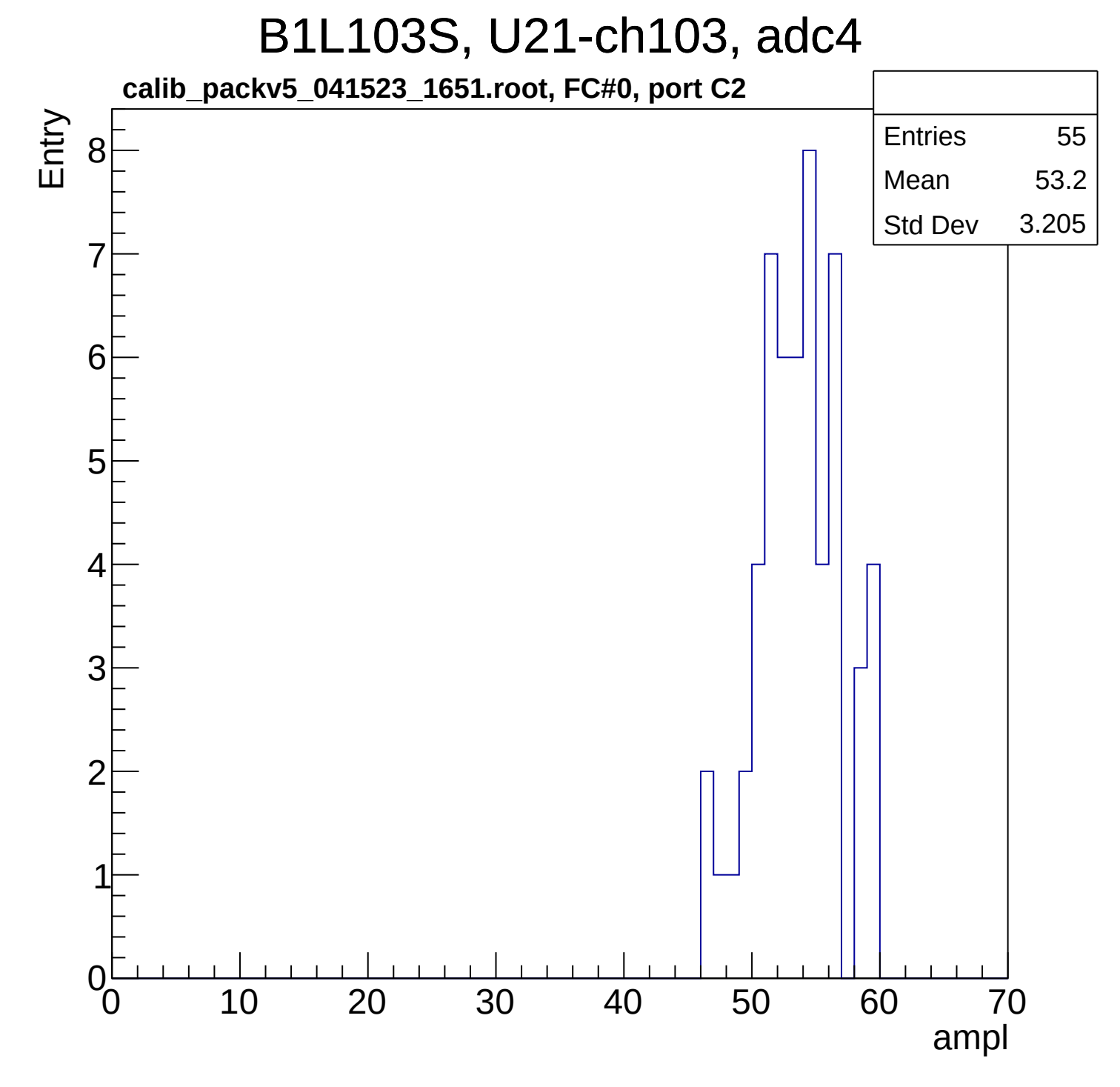
B1L103S, U21-ch103, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 53.2
Std Dev 3.205
Entry
ampl
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2
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4
5
6
7
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0
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60
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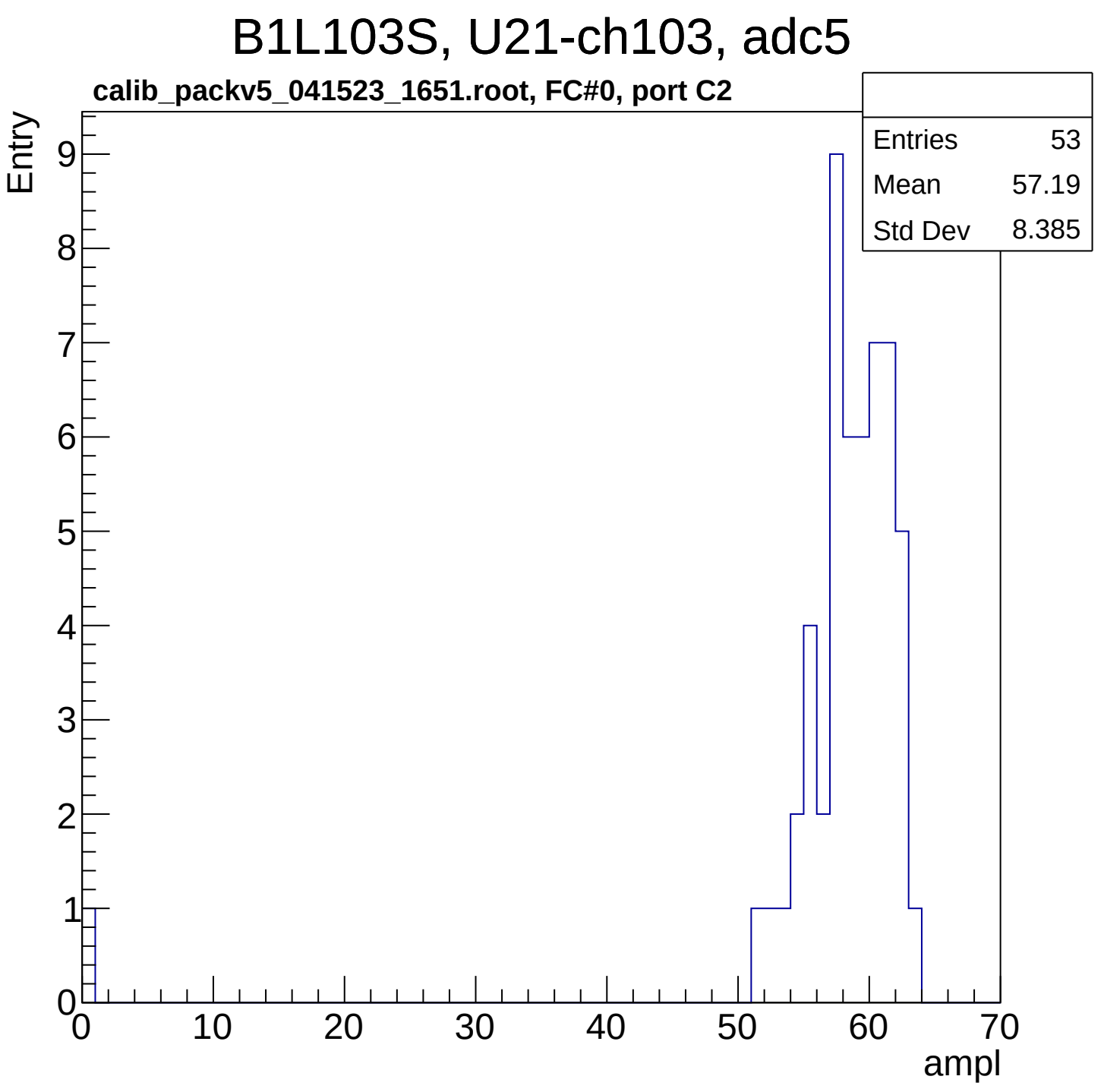
B1L103S, U21-ch103, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 57.19
Std Dev 8.385
Entry
ampl
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5
6
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8
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0
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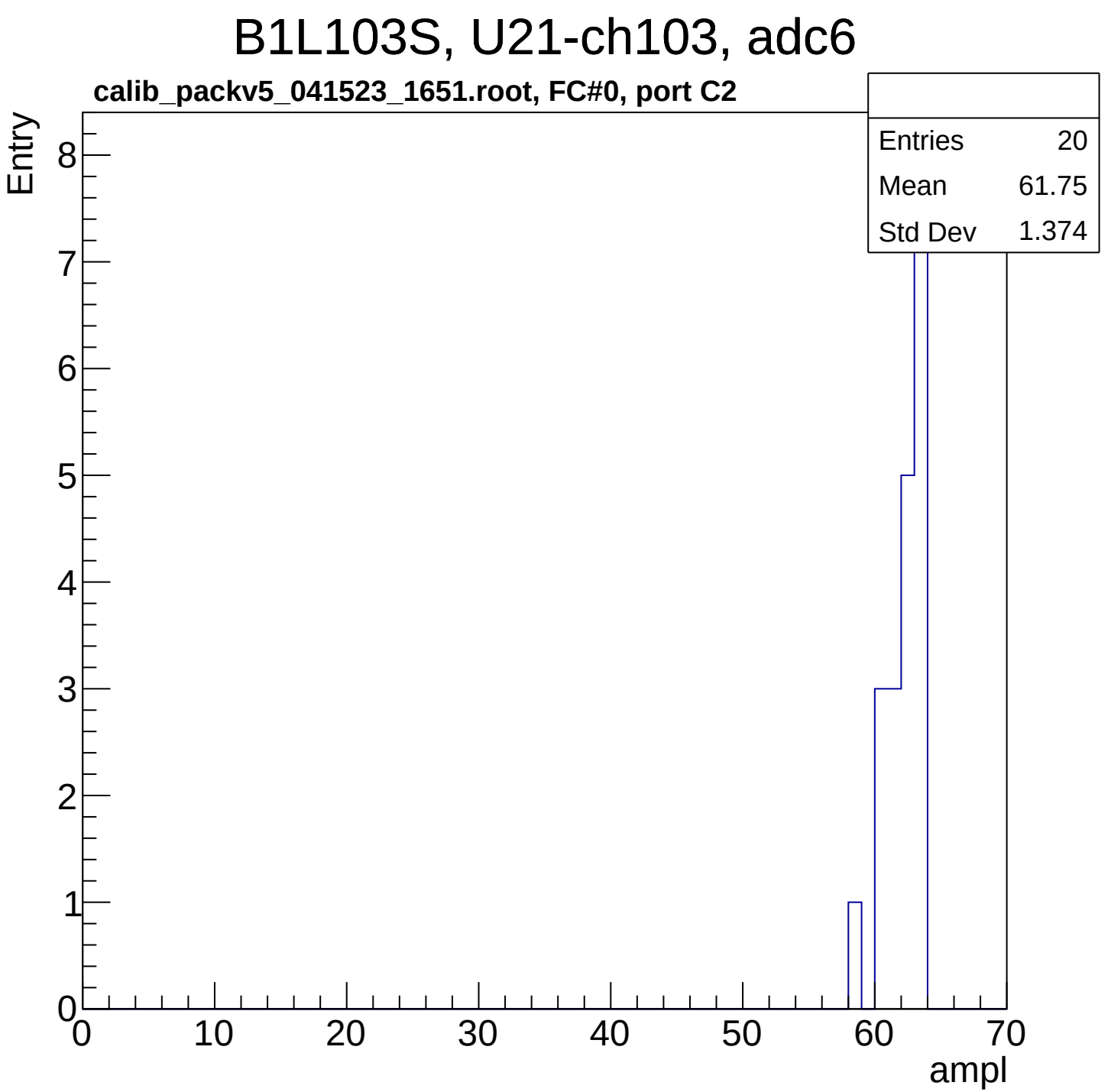
B1L103S, U21-ch103, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 61.75
Std Dev 1.374
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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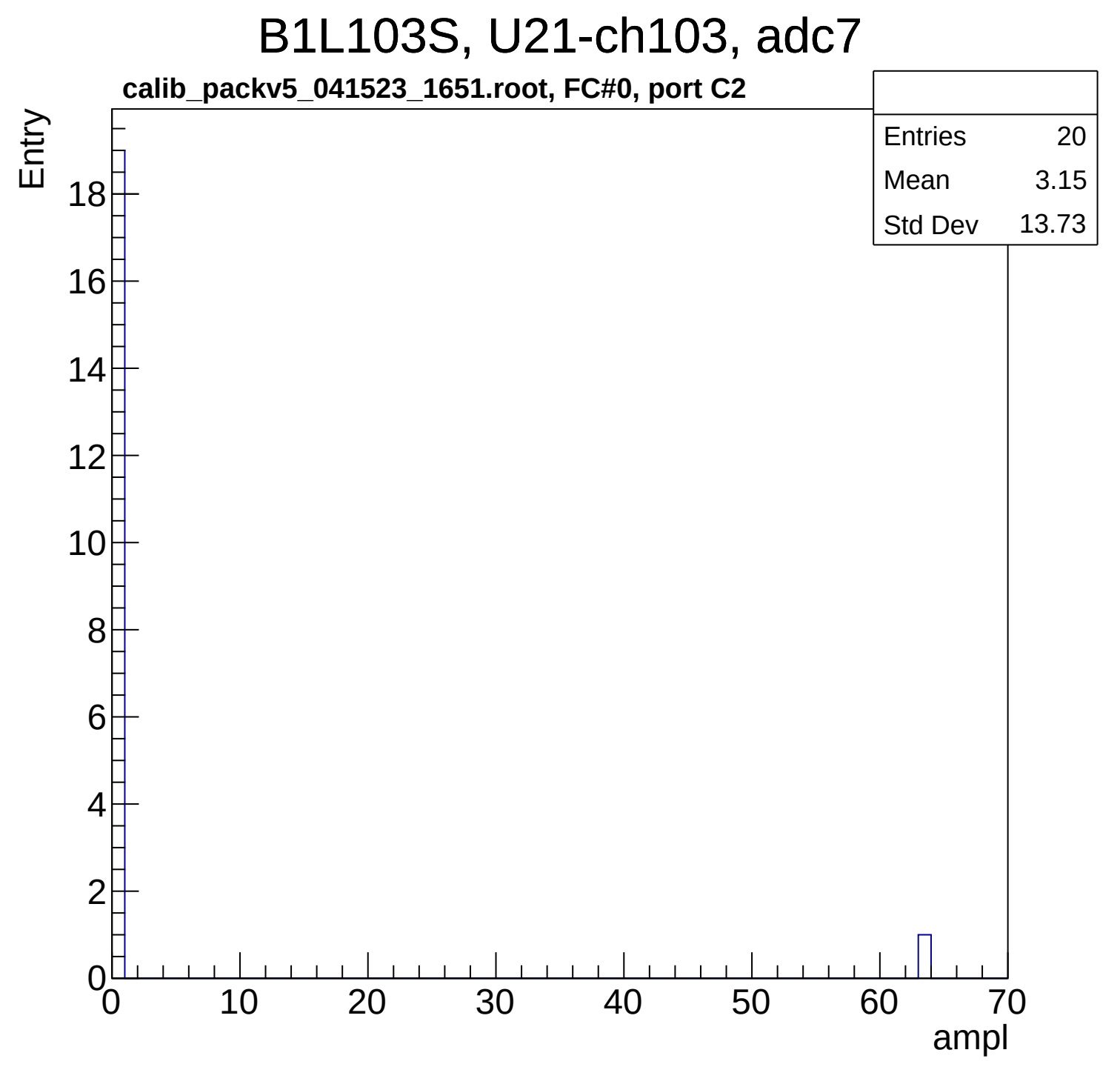
40
50
60
70


B1L103S, U21-ch103, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
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6
8
10
12
14
16
18
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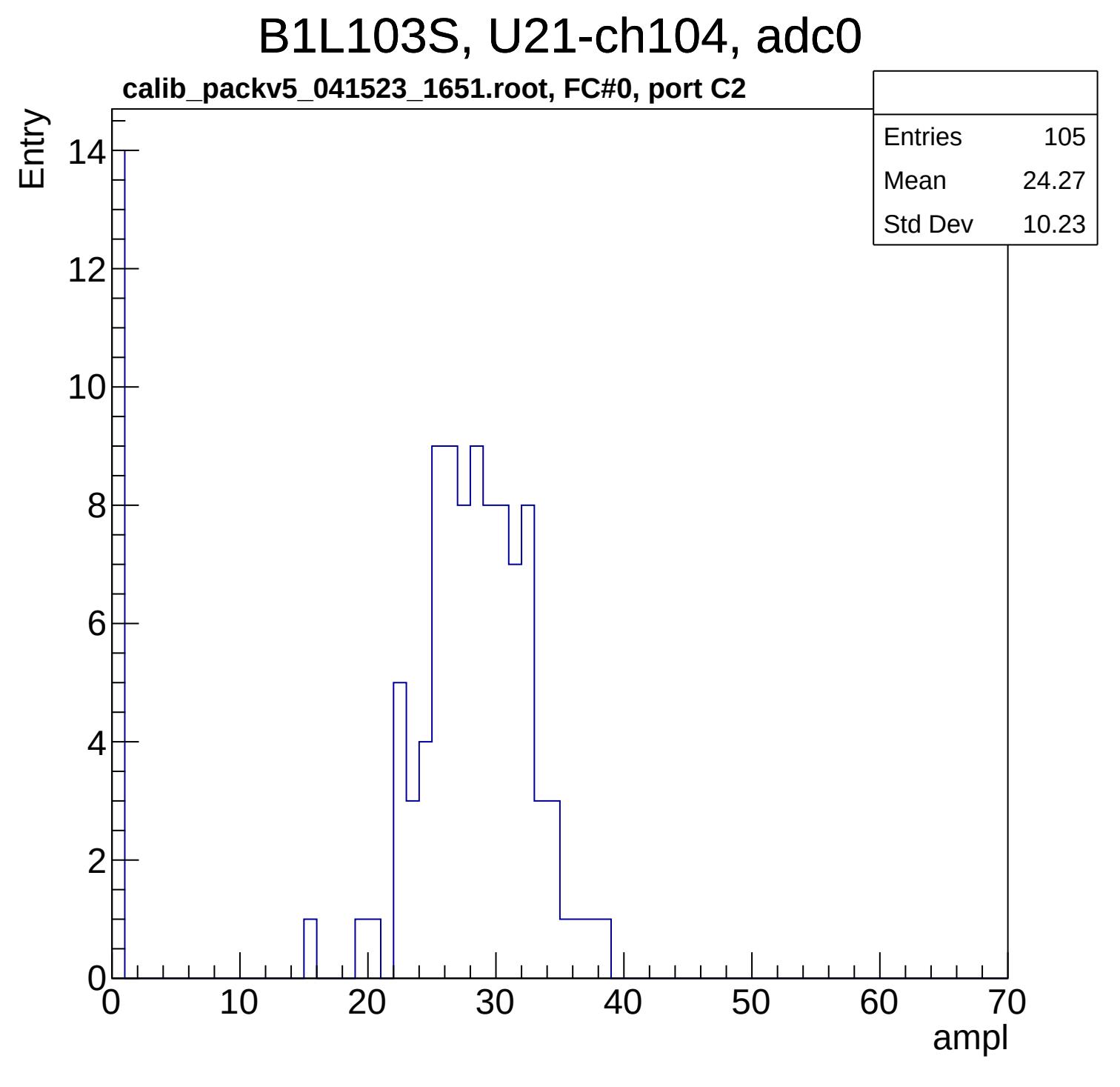
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch104, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 105
Mean 24.27
Std Dev 10.23
Entry
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4
6
8
10
12
14
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10
20
30
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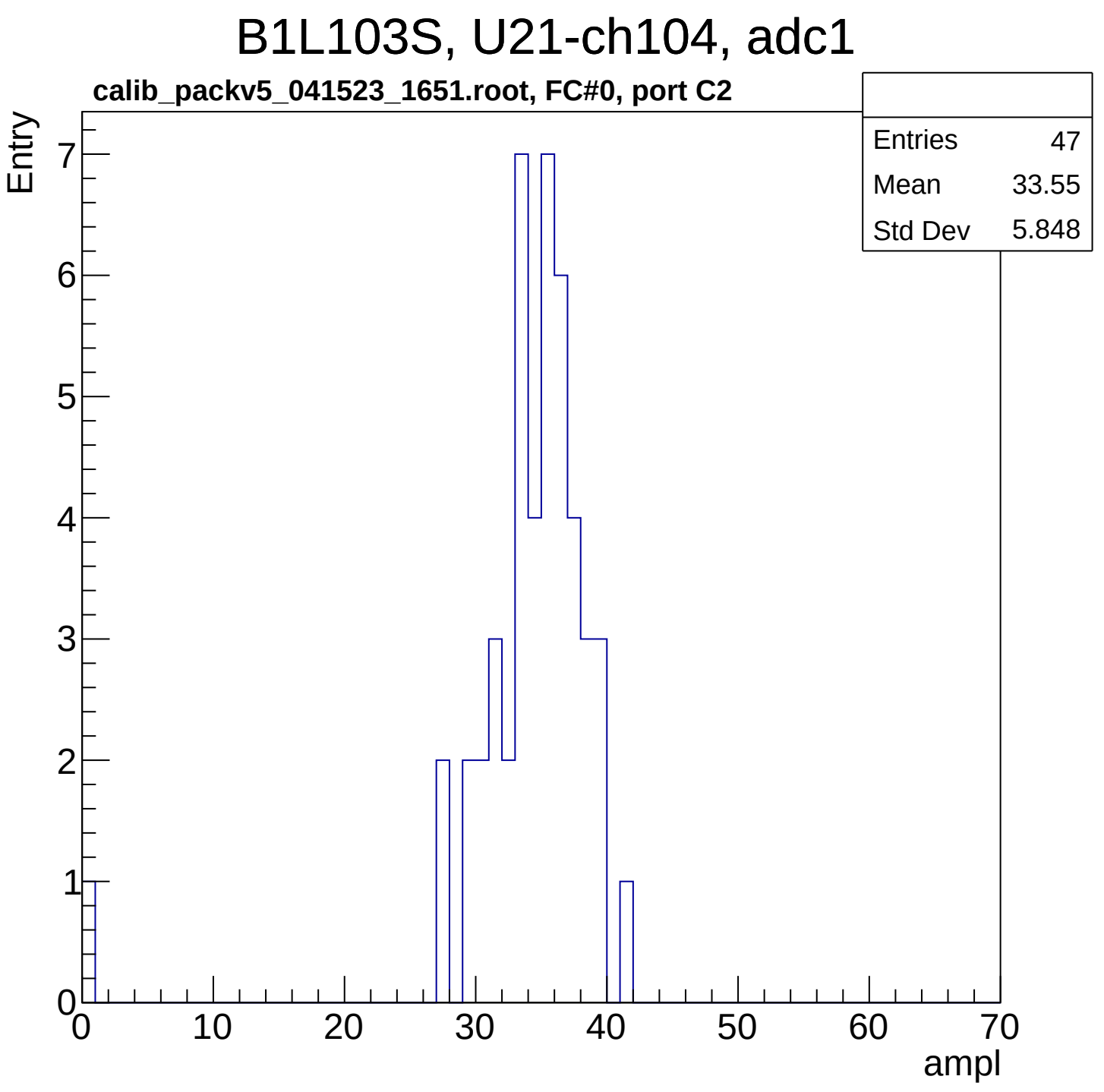
50
60
70
ampl


B1L103S, U21-ch104, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 33.55
Std Dev 5.848
Entry
ampl
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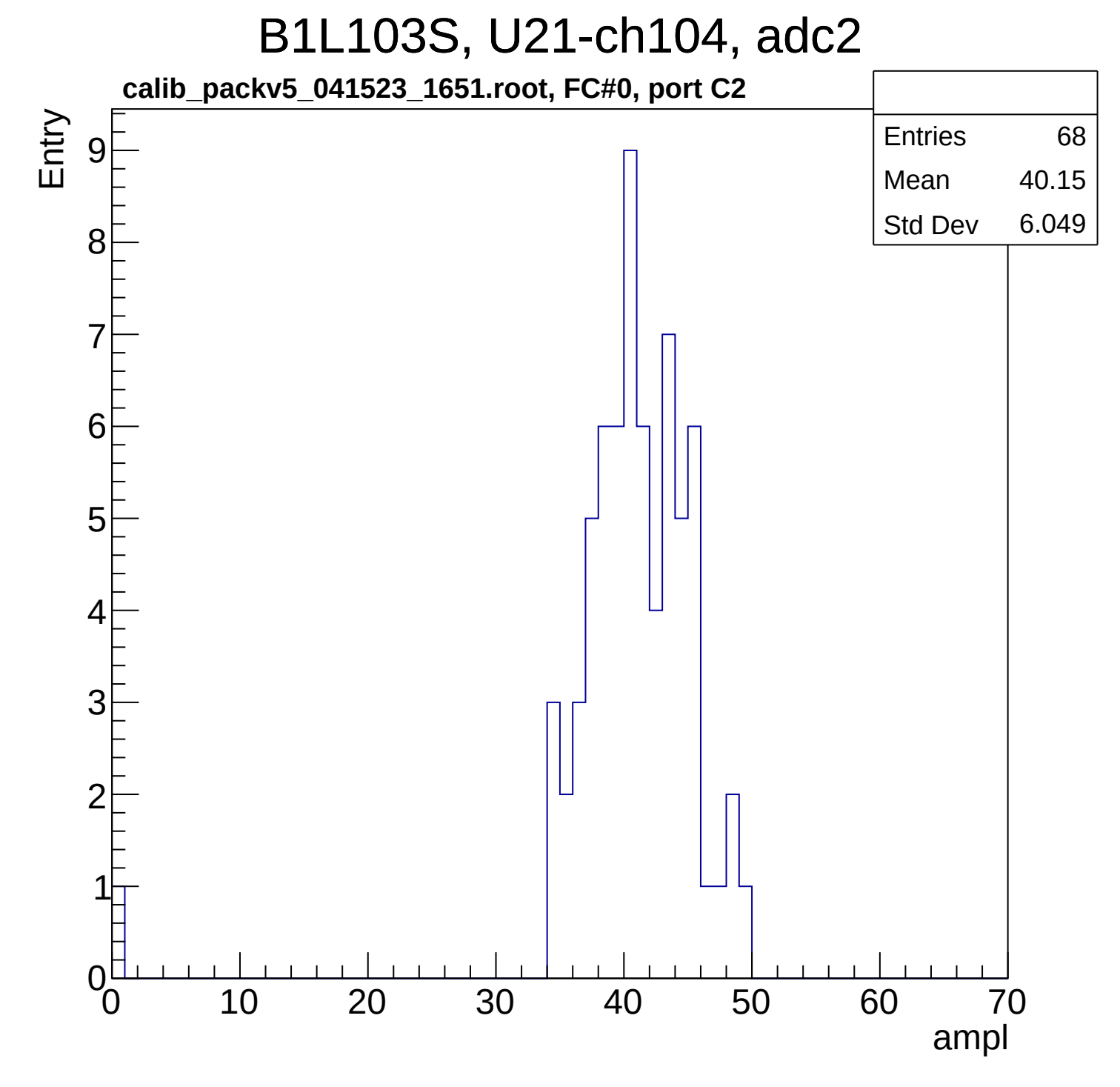
B1L103S, U21-ch104, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 40.15
Std Dev 6.049
Entry
ampl
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2
3
4
5
6
7
8
9
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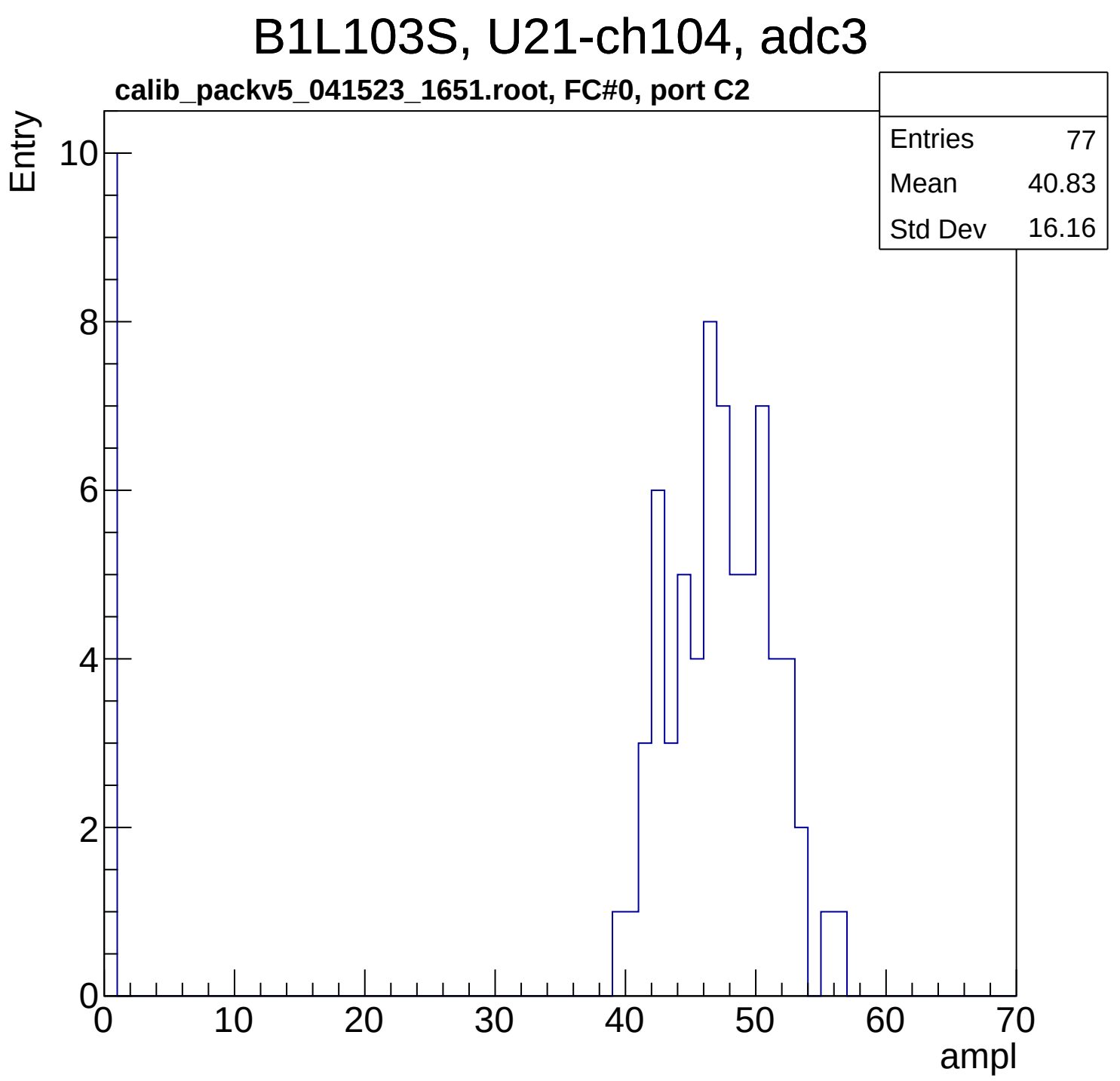
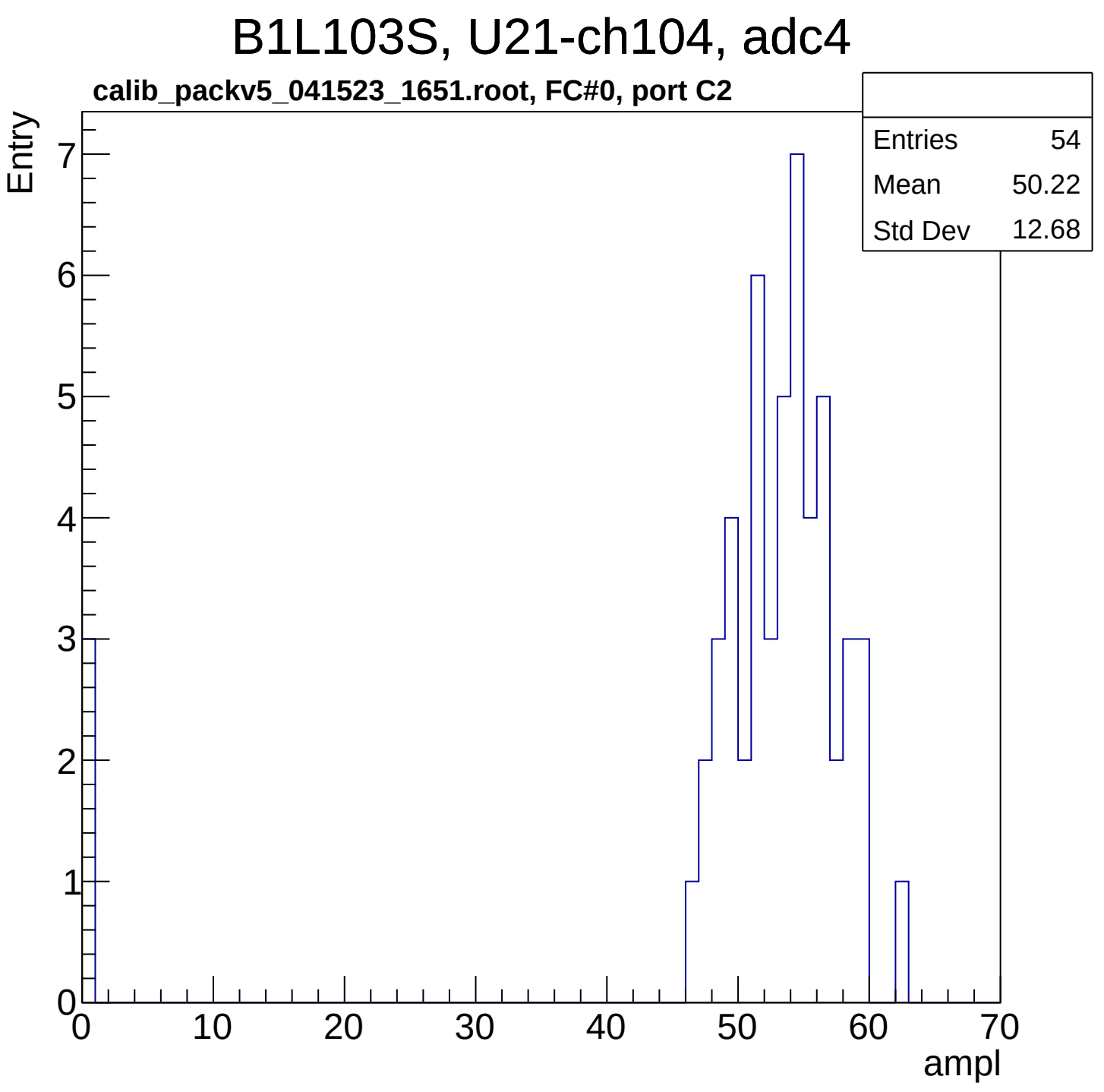
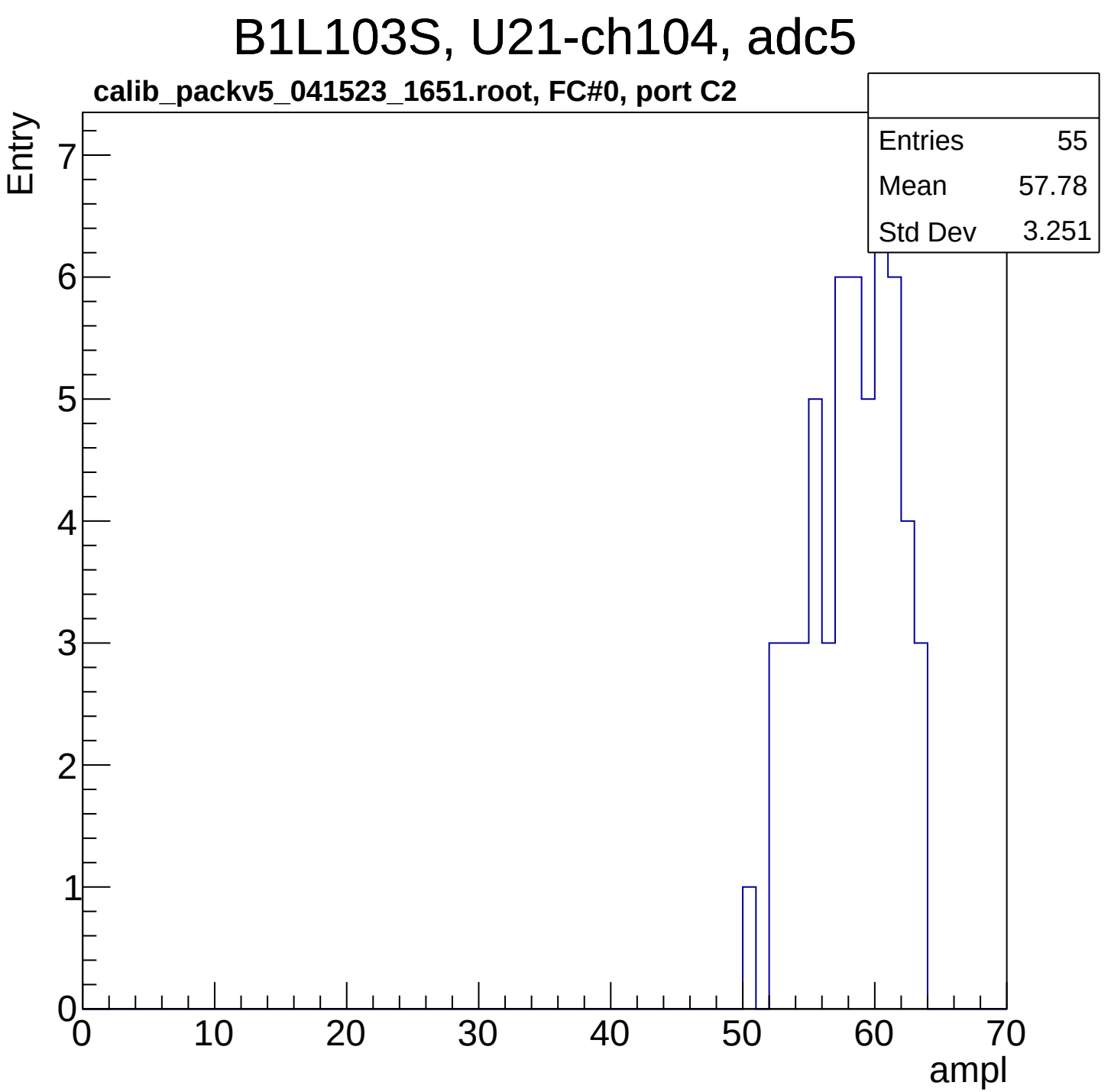
40
50
60
70


B1L103S, U21-ch104, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 40.83
Std Dev 16.16
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U21-ch104, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 50.22
Std Dev 12.68
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U21-ch104, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 57.78
Std Dev 3.251
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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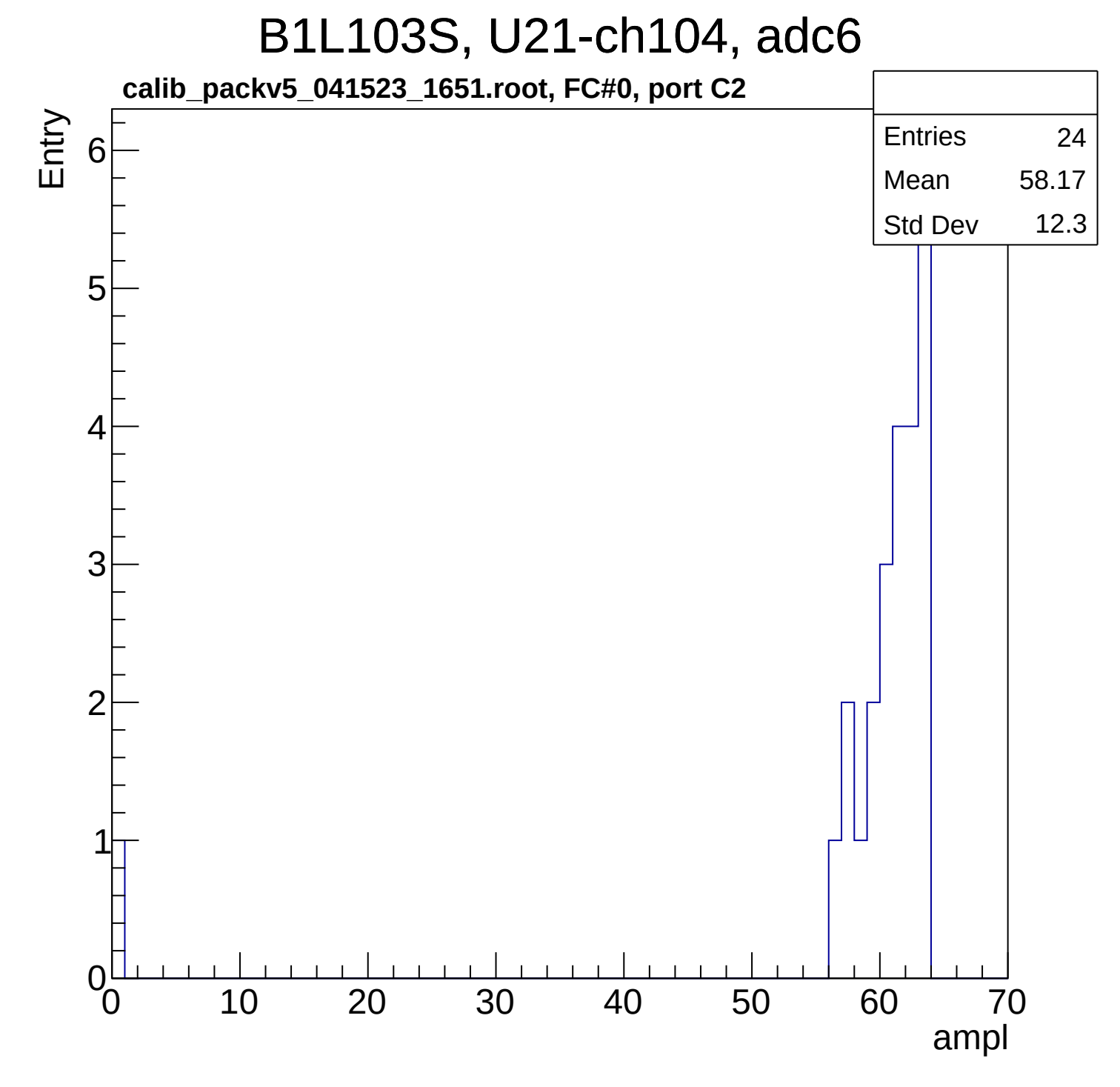
B1L103S, U21-ch104, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 58.17
Std Dev 12.3
Entry
ampl
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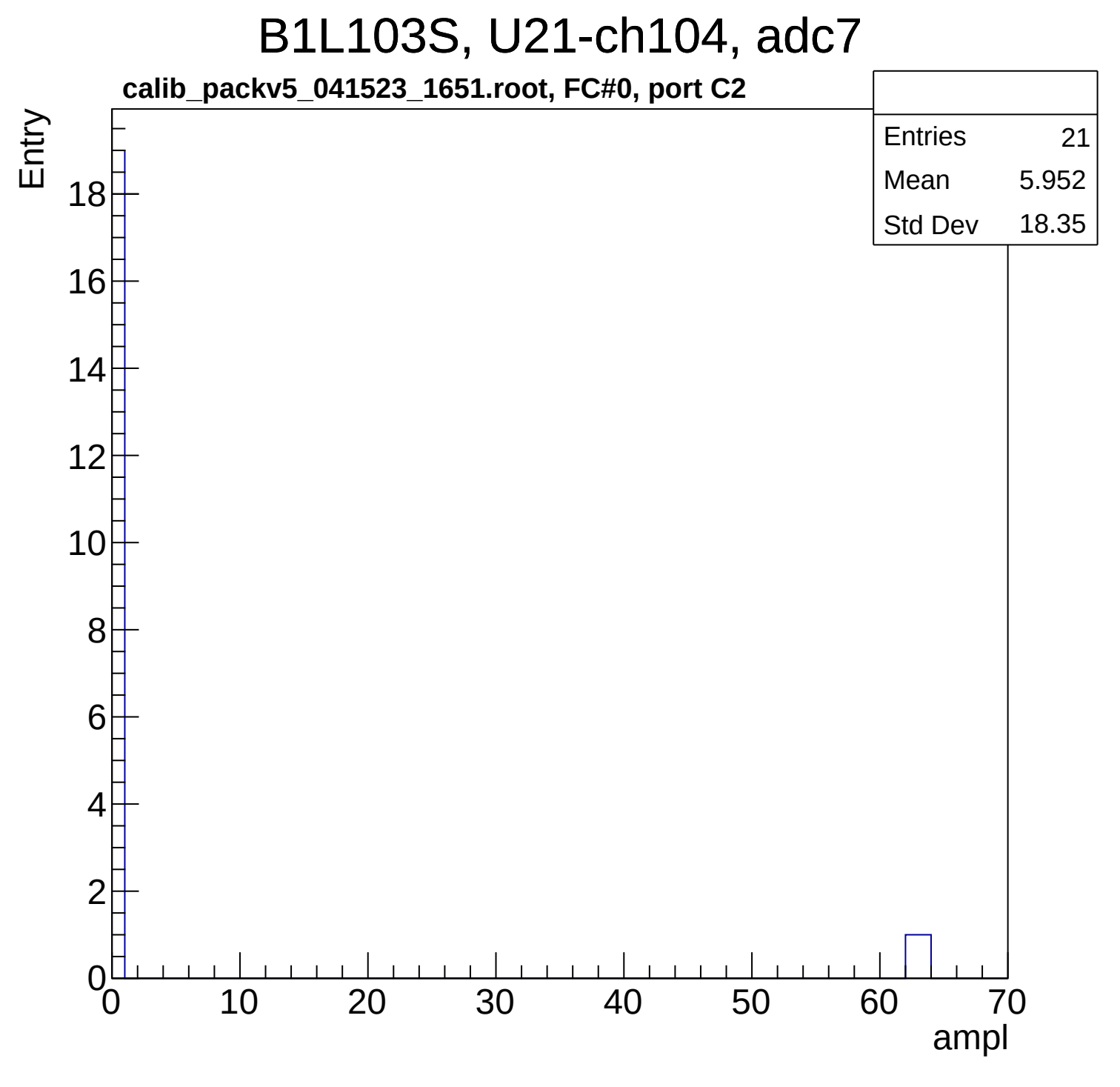
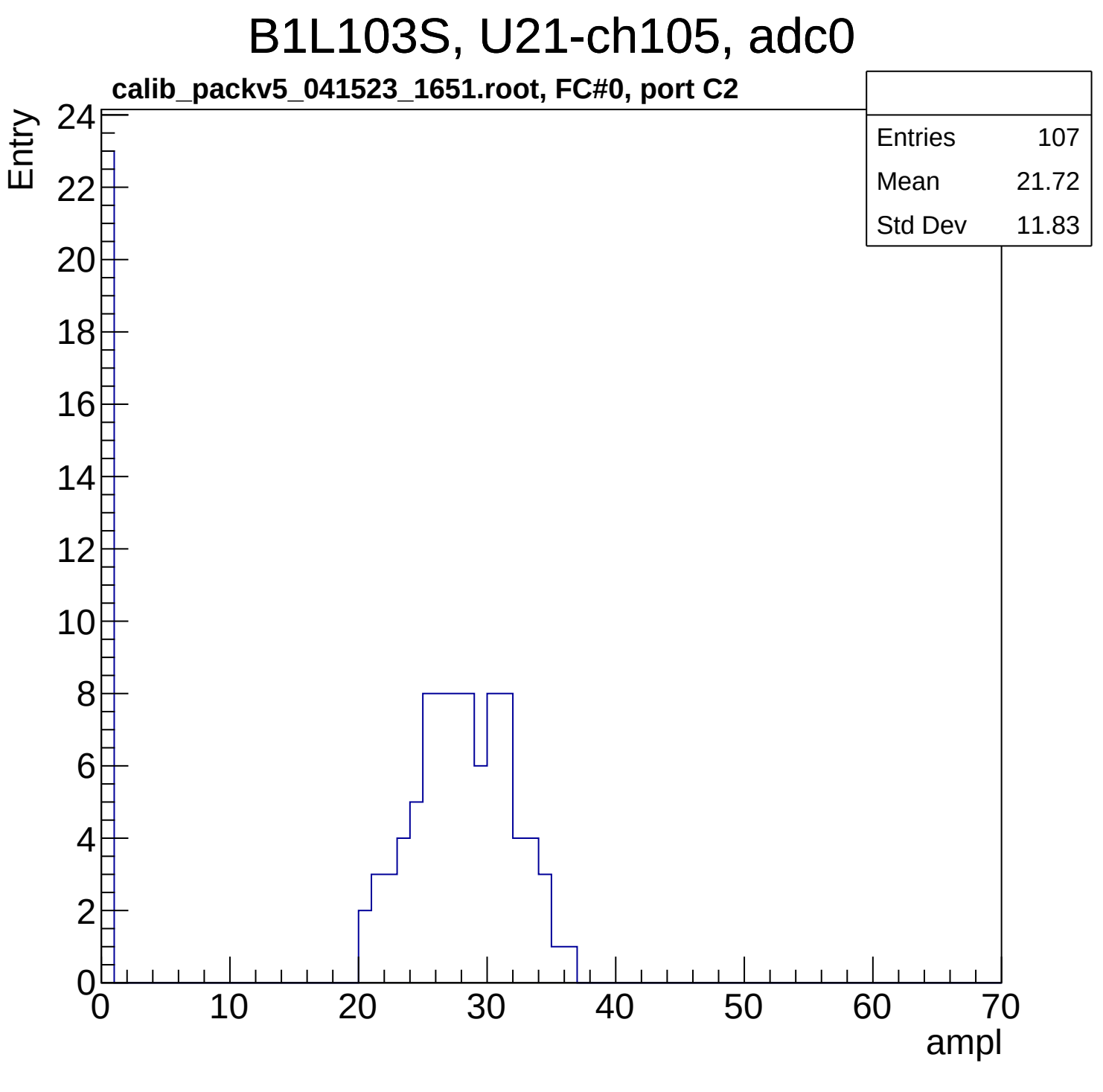
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U21-ch104, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.952
Std Dev 18.35
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch105, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 107
Mean 21.72
Std Dev 11.83
Entry
ampl
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2
4
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8
10
12
14
16
18
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22
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40
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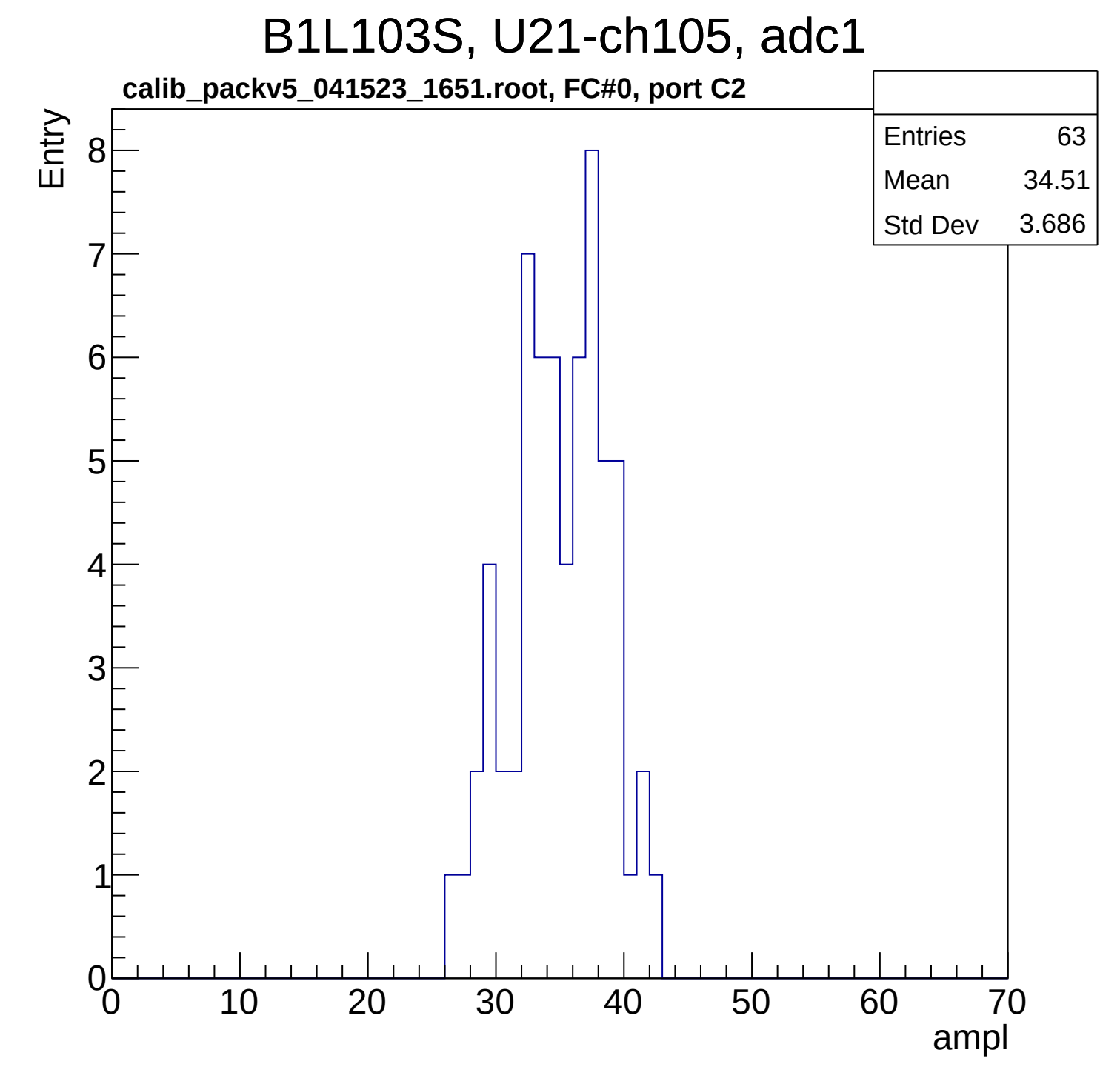
B1L103S, U21-ch105, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 34.51
Std Dev 3.686
Entry
ampl
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2
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5
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7
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0
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40
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60
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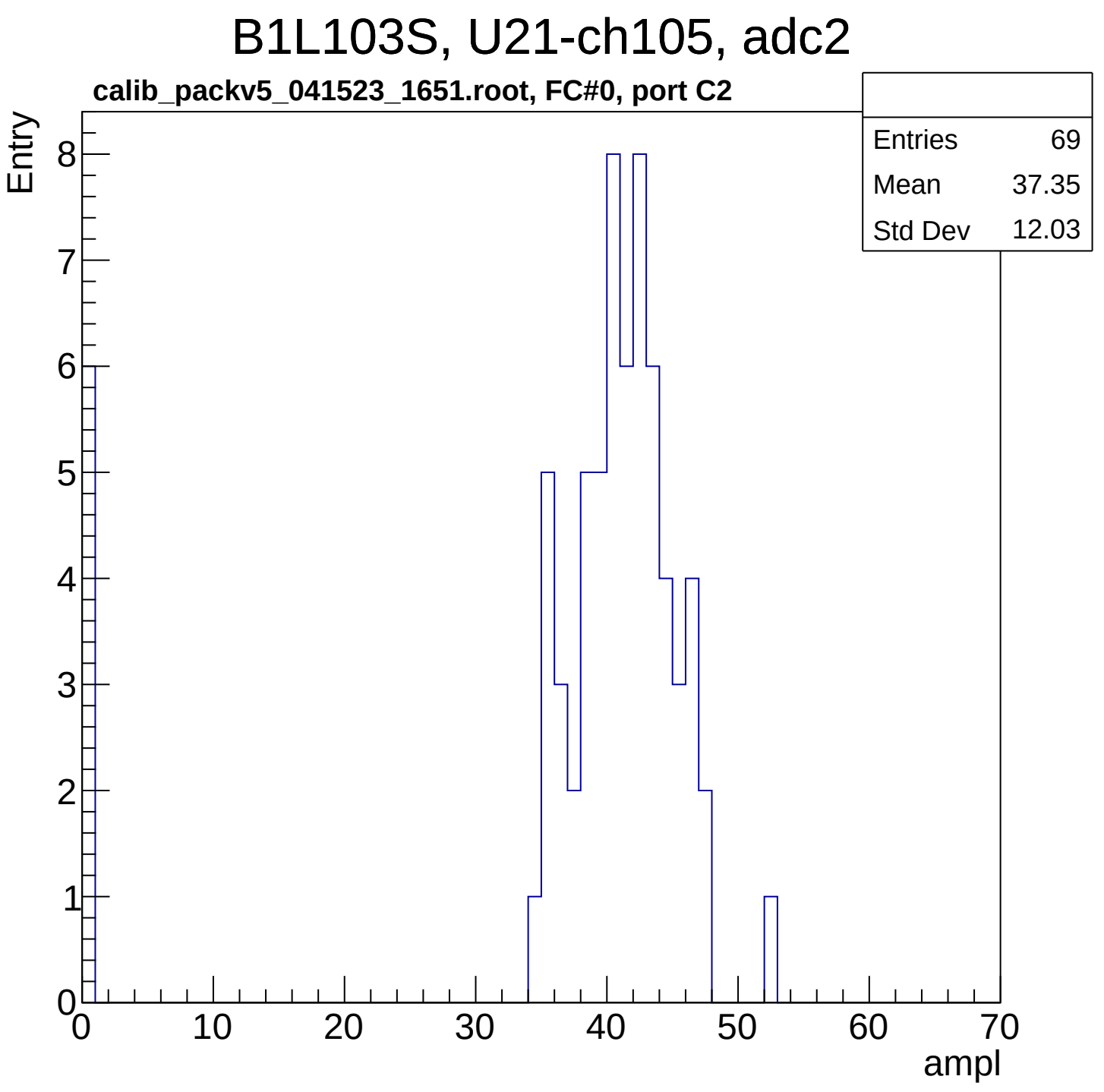
B1L103S, U21-ch105, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 37.35
Std Dev 12.03
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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40
50
60
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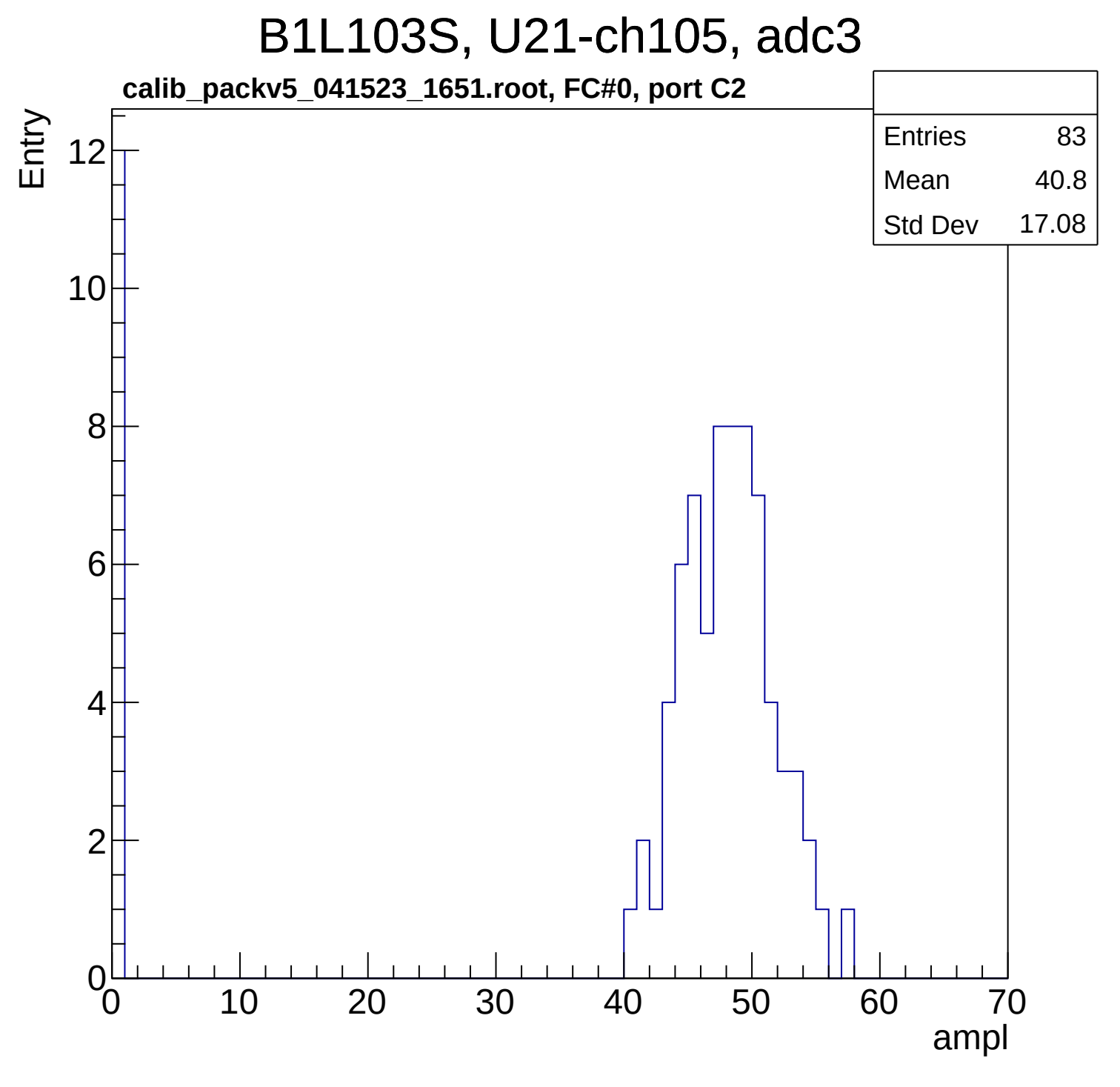
B1L103S, U21-ch105, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 40.8
Std Dev 17.08
Entry
ampl
0
2
4
6
8
10
12
0
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20
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40
50
60
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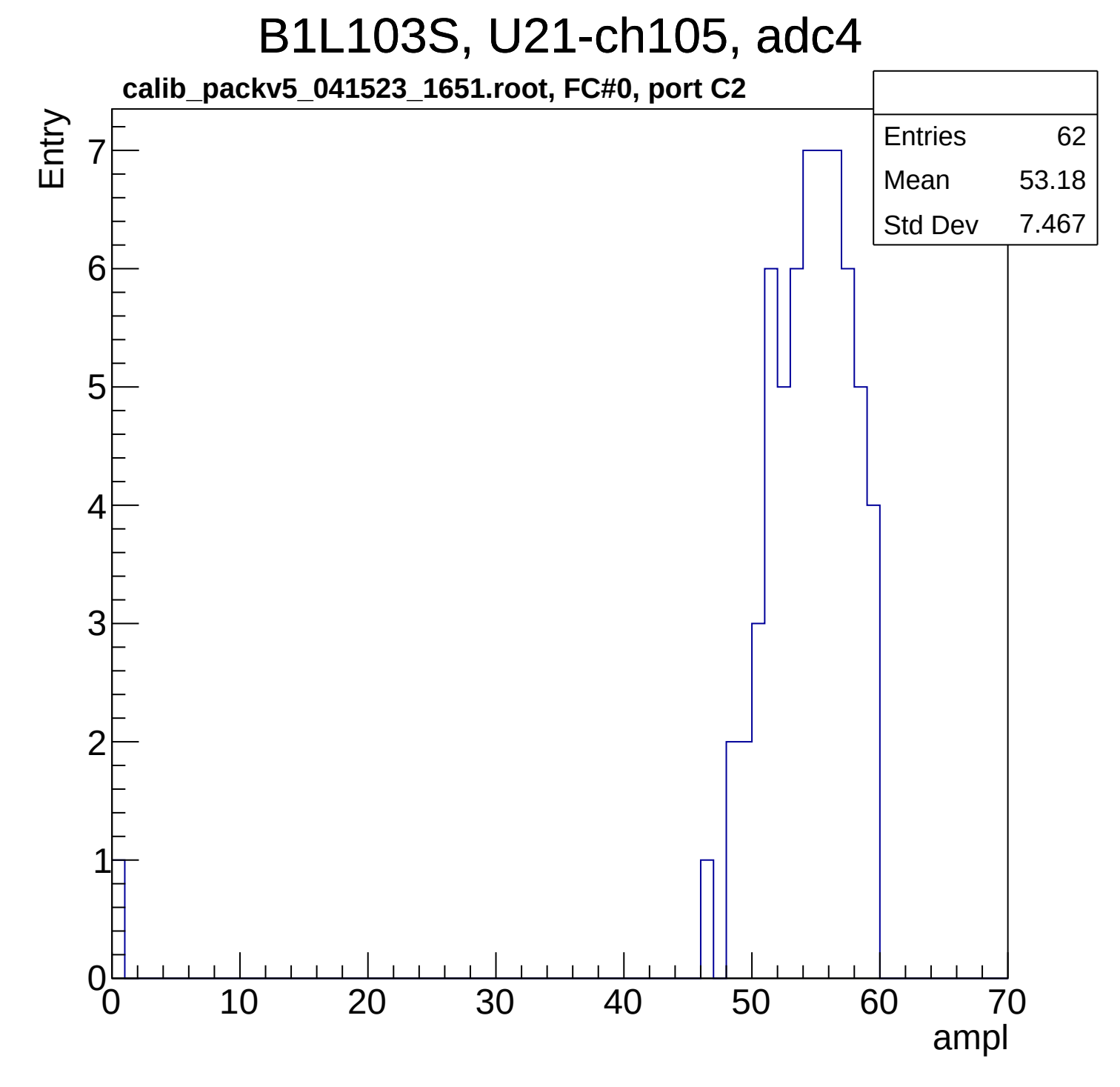
B1L103S, U21-ch105, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 53.18
Std Dev 7.467
Entry
ampl
0
1
2
3
4
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6
7
0
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20
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40
50
60
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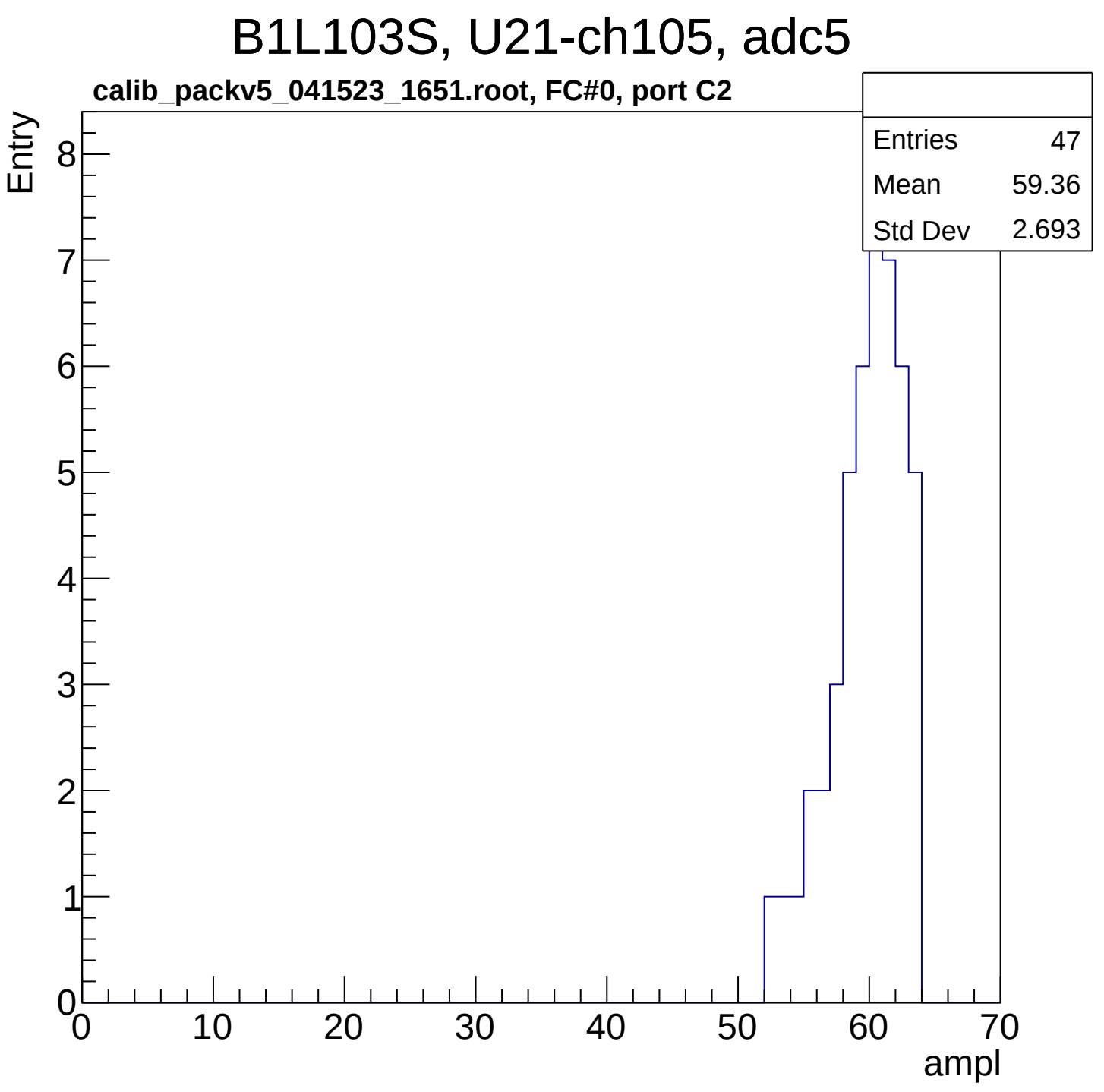
B1L103S, U21-ch105, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 59.36
Std Dev 2.693
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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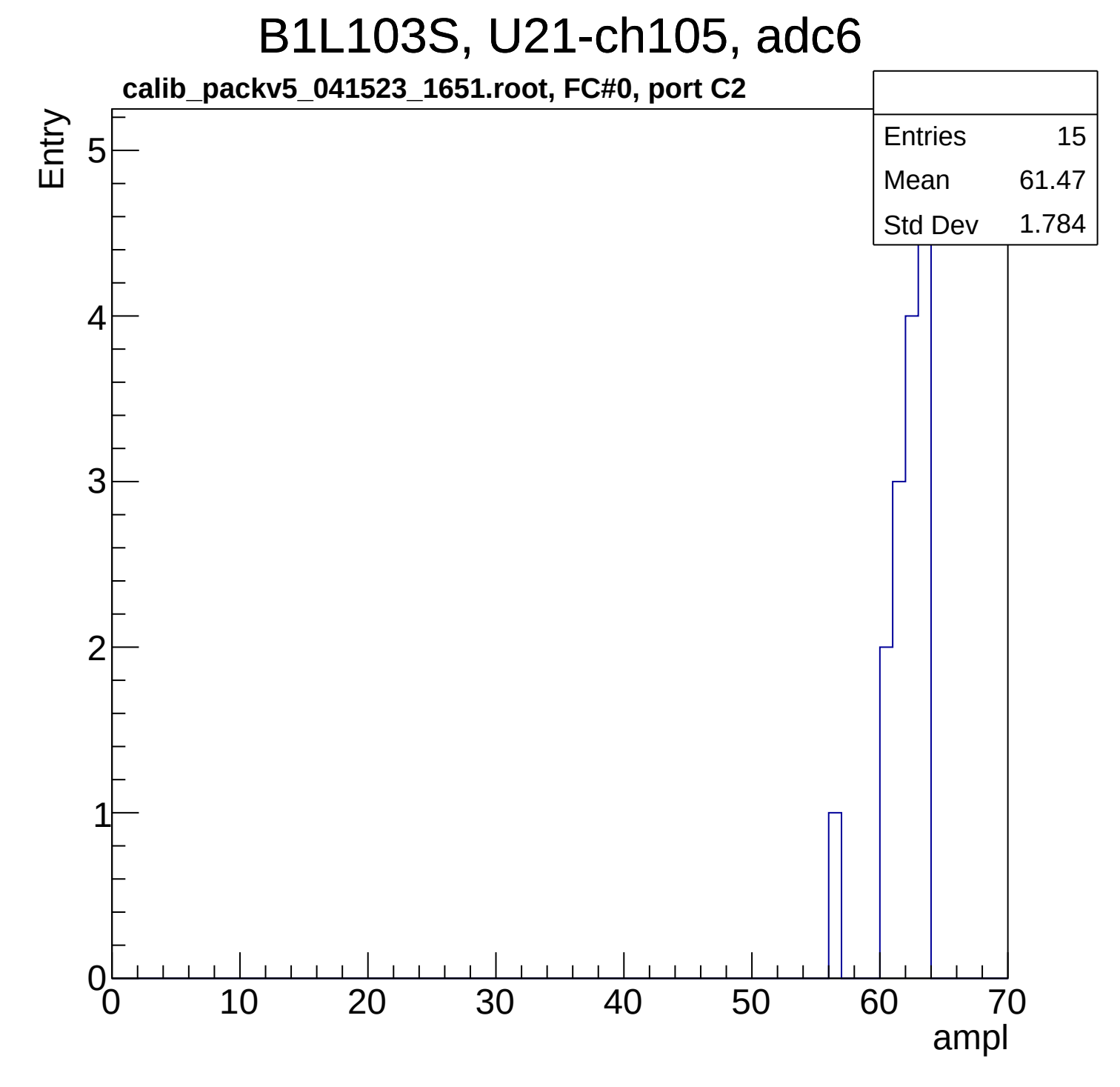
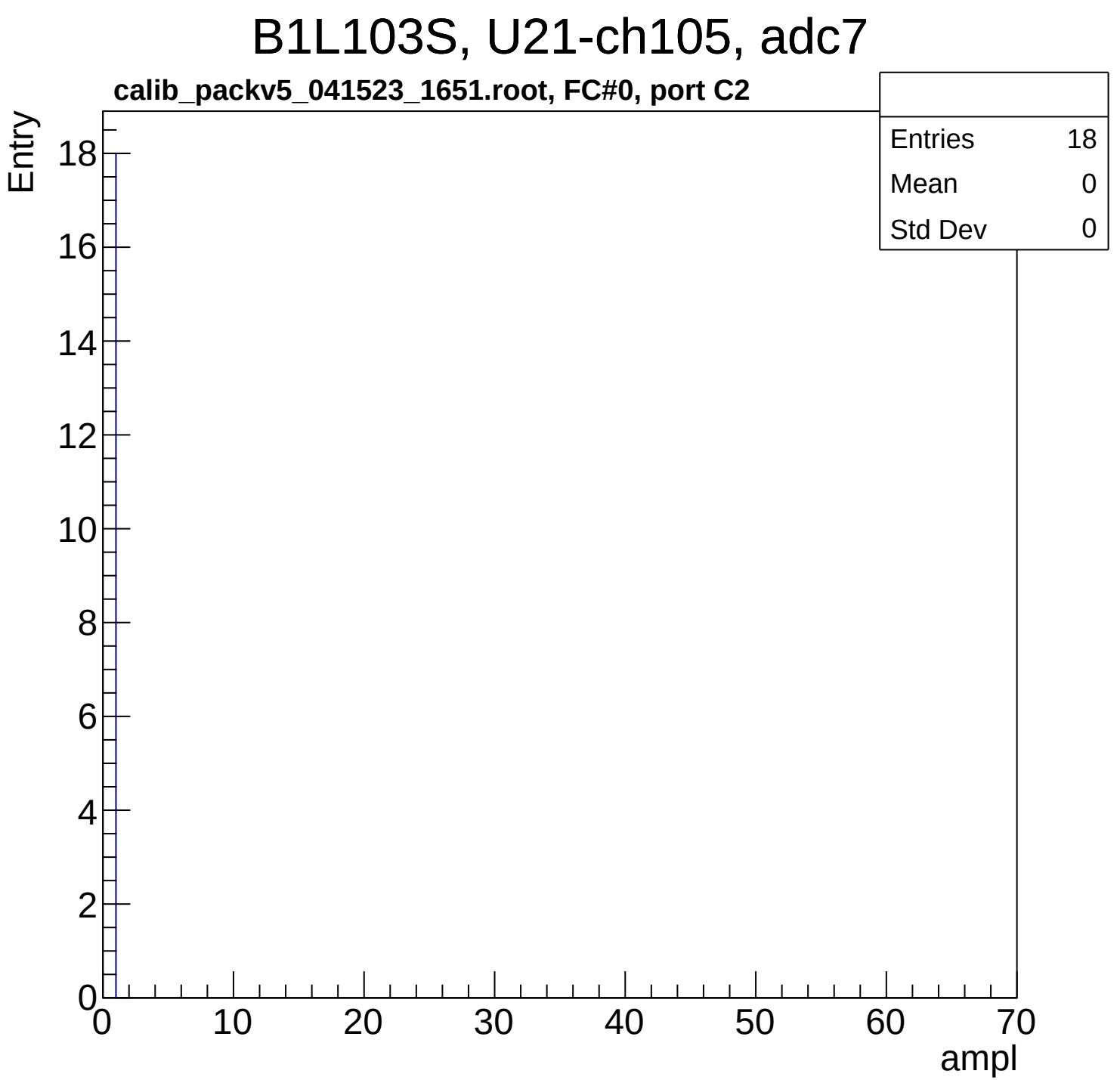

B1L103S, U21-ch105, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 61.47
Std Dev 1.784
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U21-ch105, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
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6
8
10
12
14
16
18
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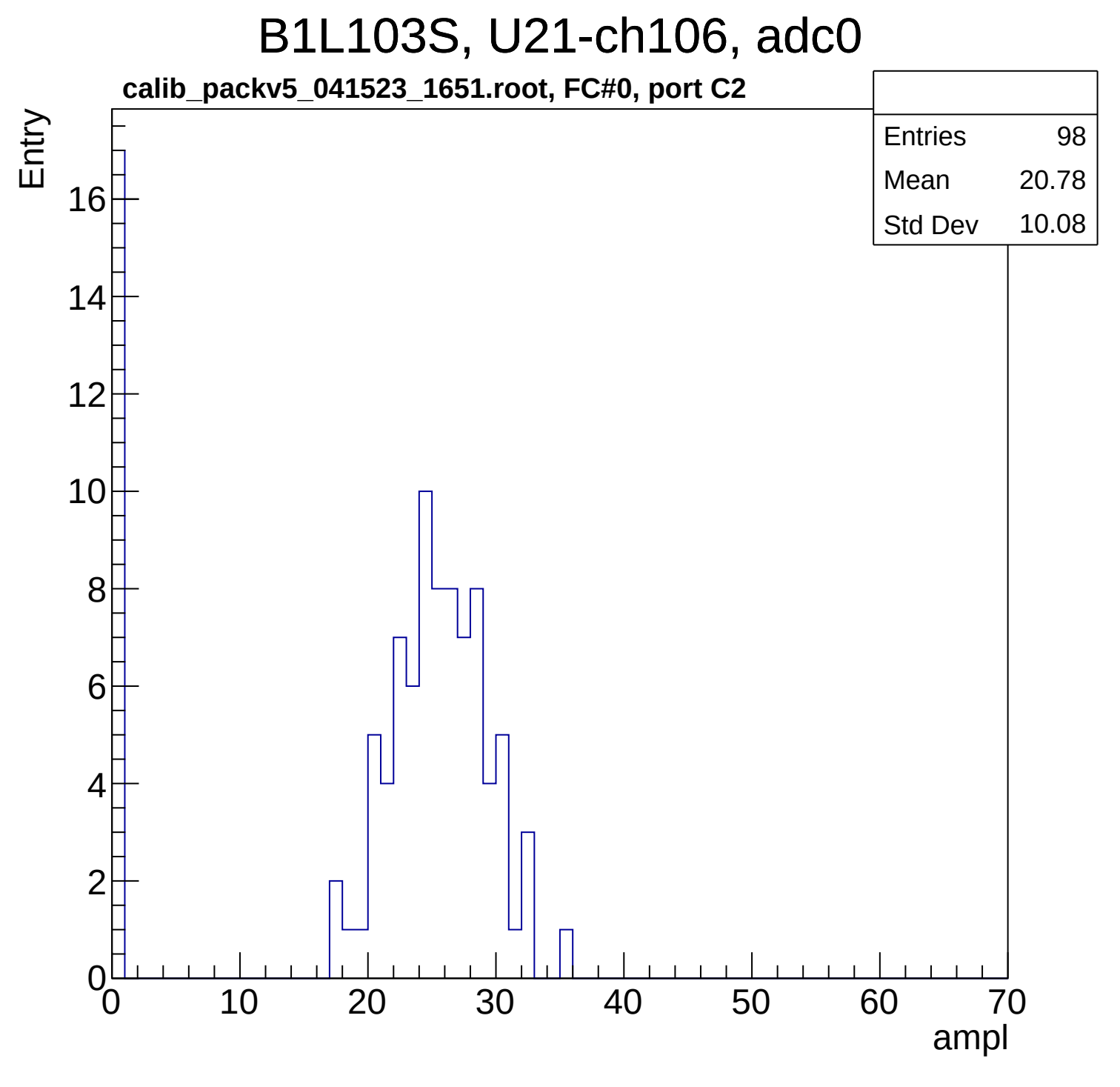
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch106, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 98
Mean 20.78
Std Dev 10.08
Entry
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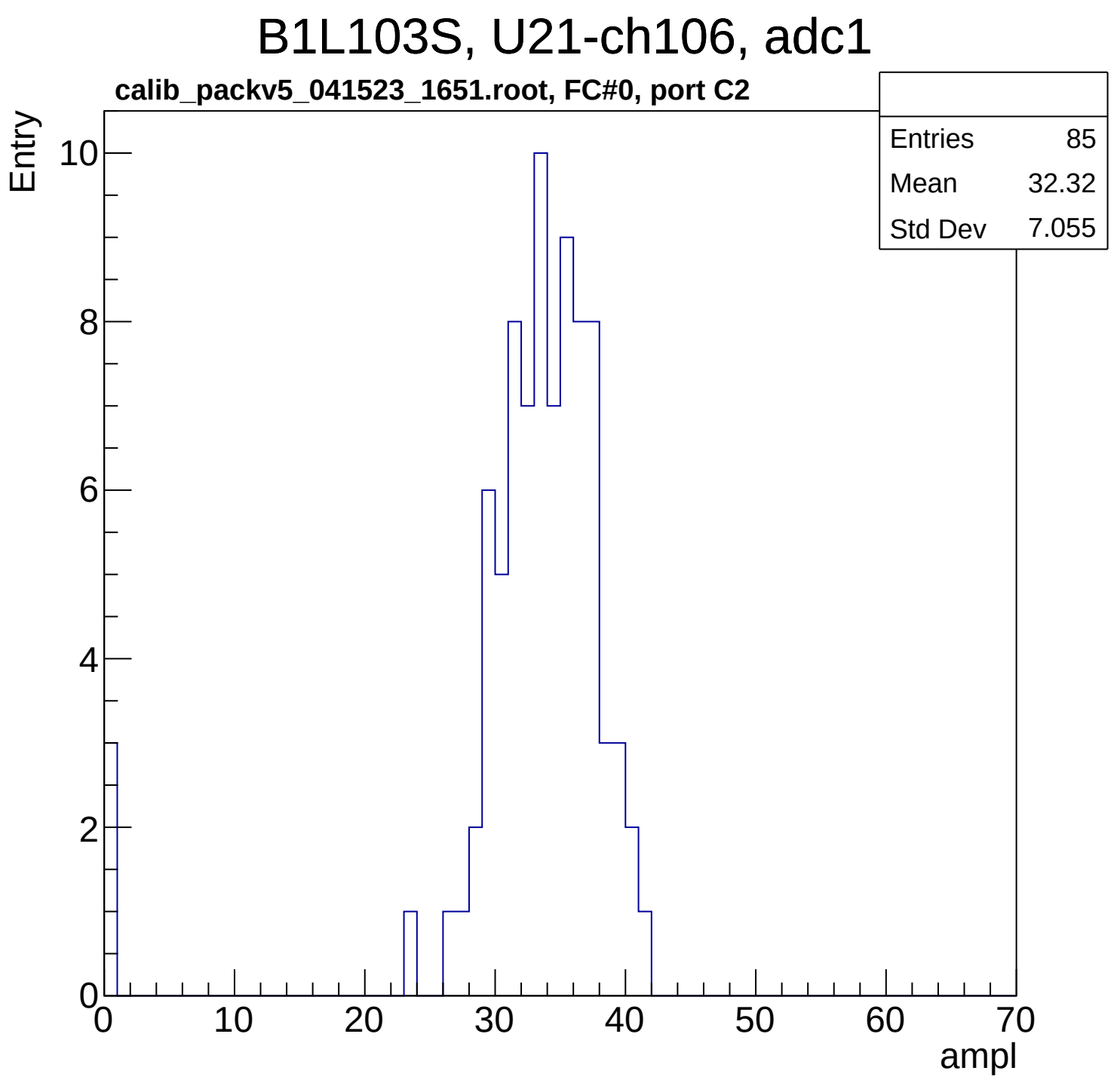
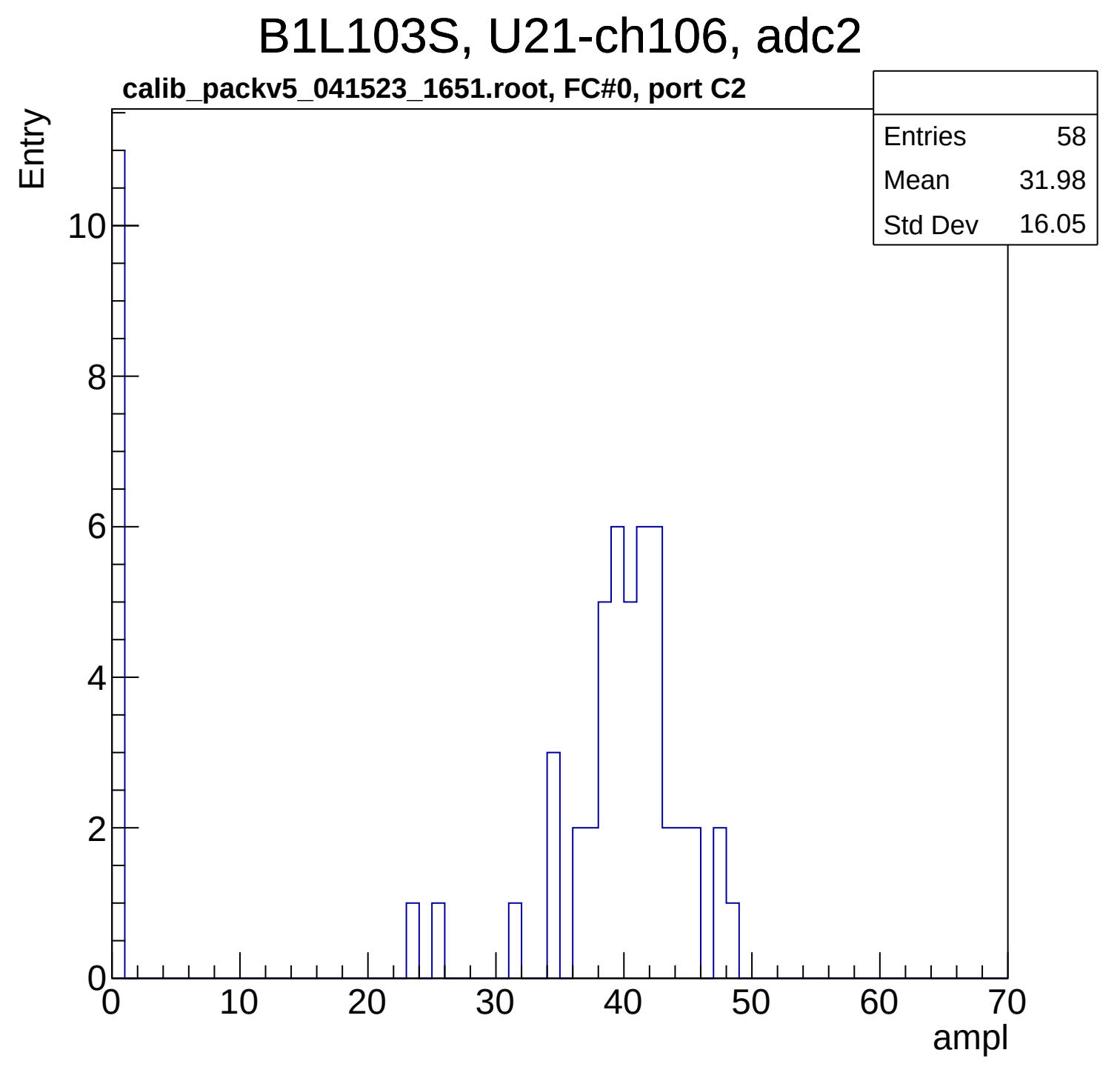
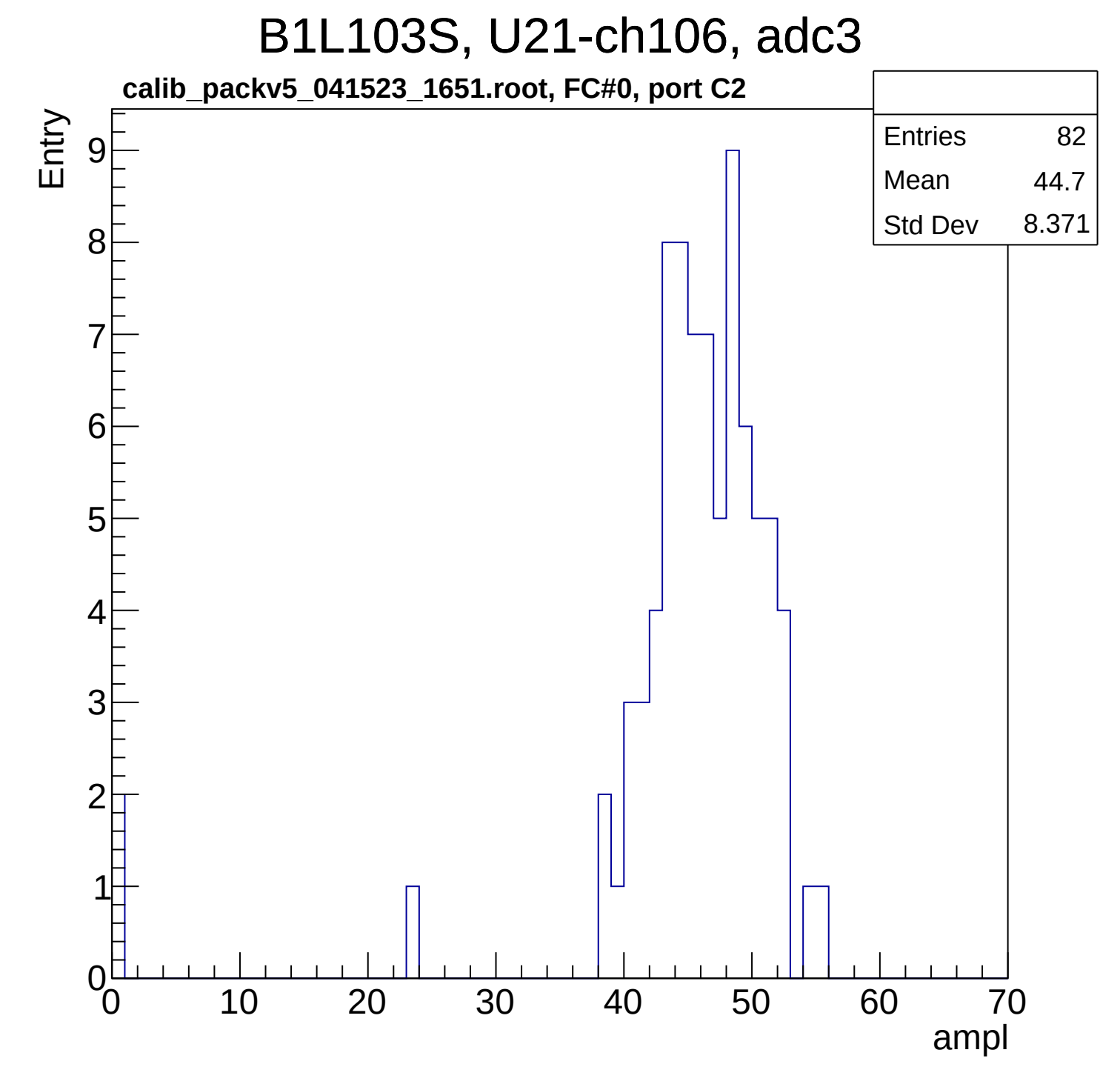
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch106, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 32.32
Std Dev 7.055
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch106, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 31.98
Std Dev 16.05
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch106, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 44.7
Std Dev 8.371
Entry
ampl
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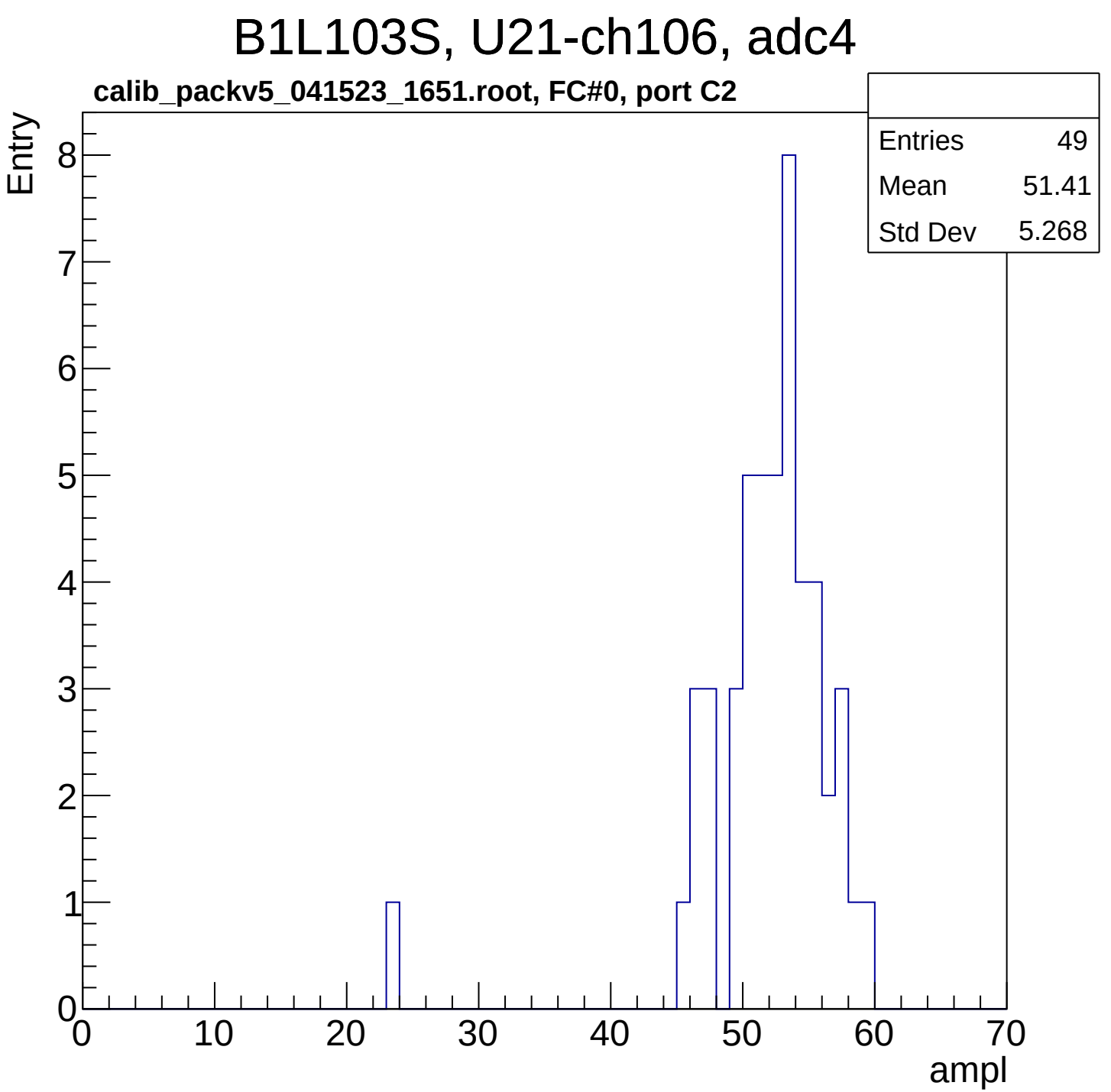
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch106, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 51.41
Std Dev 5.268
Entry
ampl
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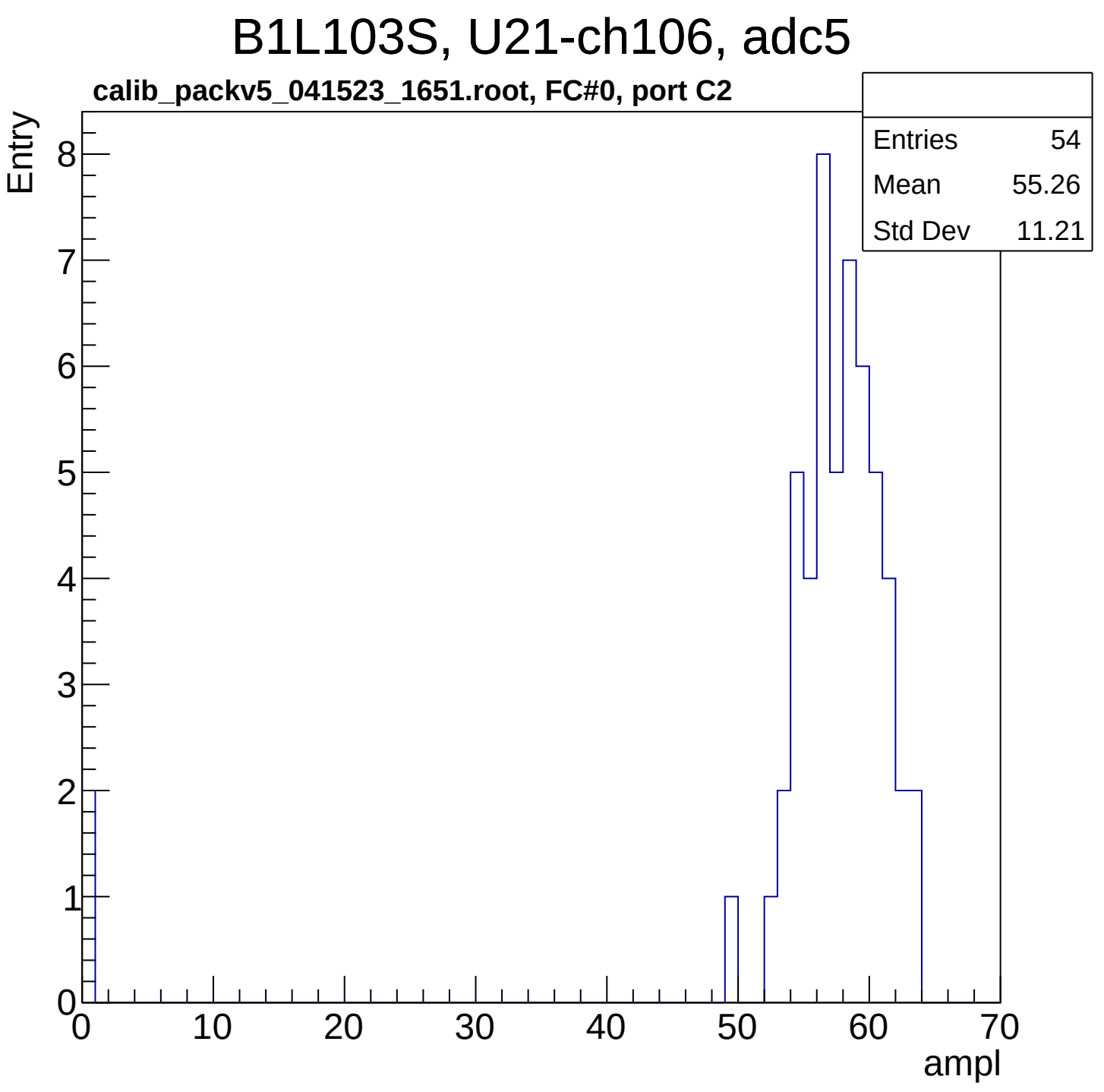
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch106, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 55.26
Std Dev 11.21
Entry
0
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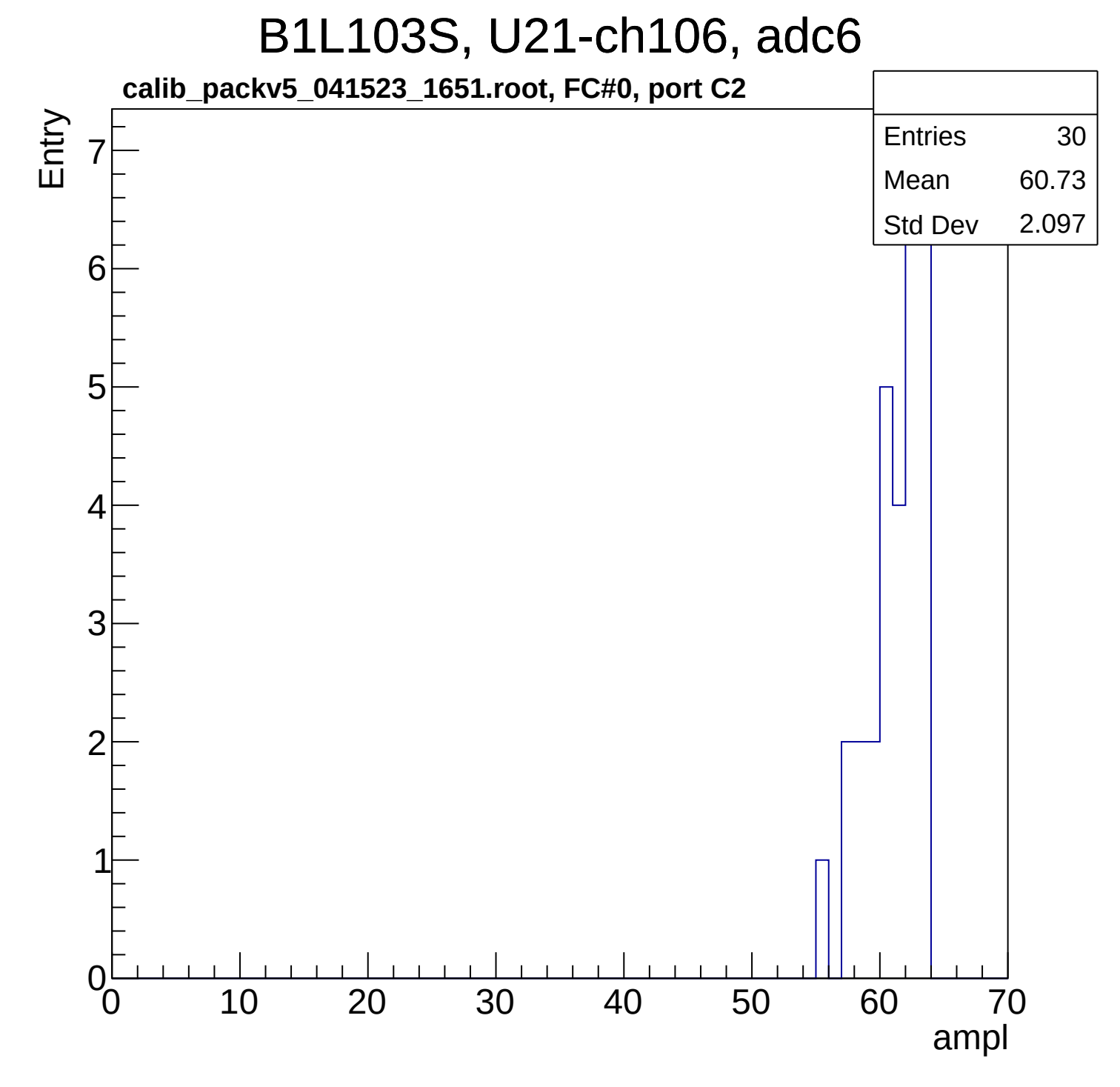
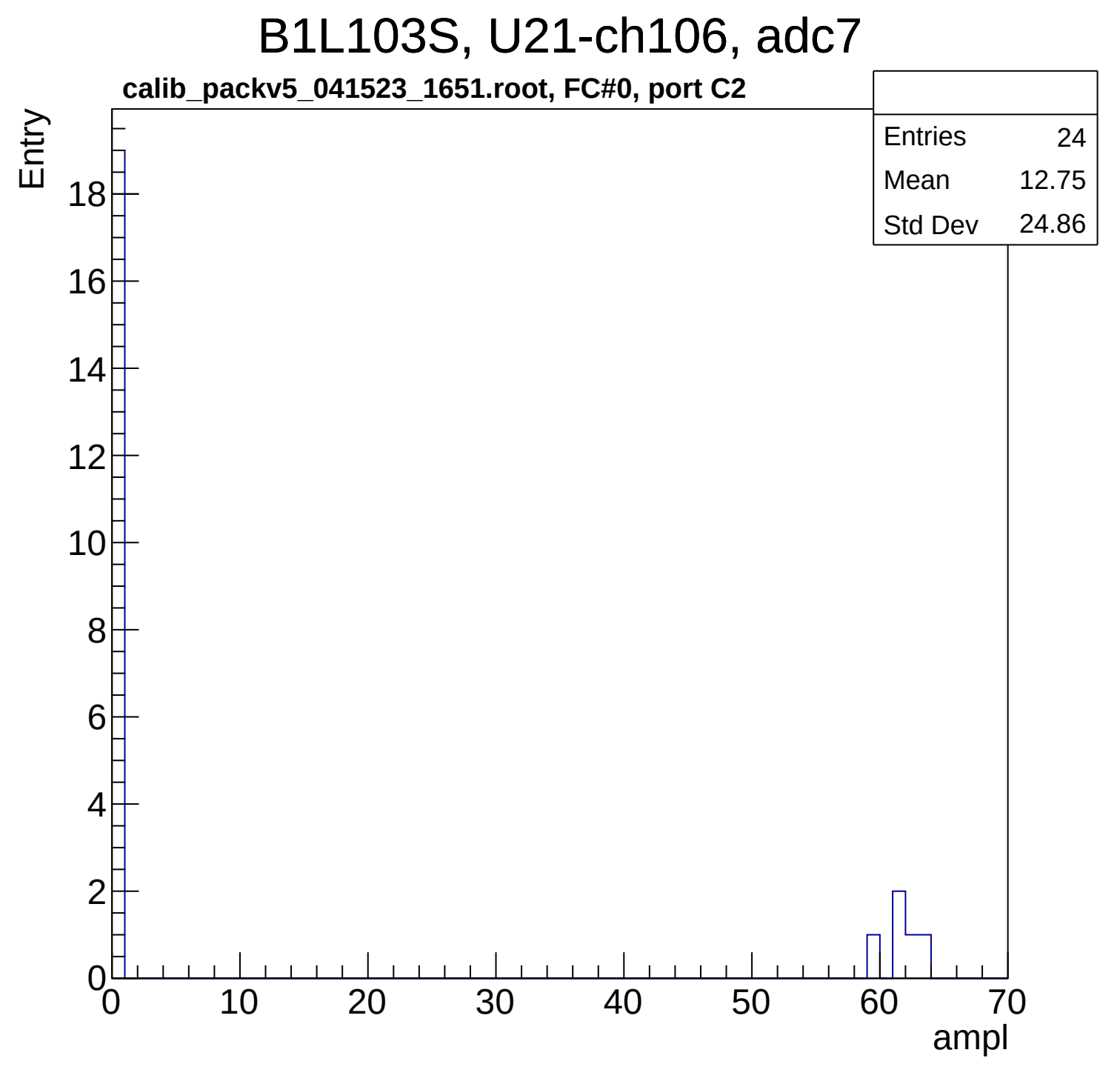
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch106, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 60.73
Std Dev 2.097
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U21-ch106, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 12.75
Std Dev 24.86
Entry
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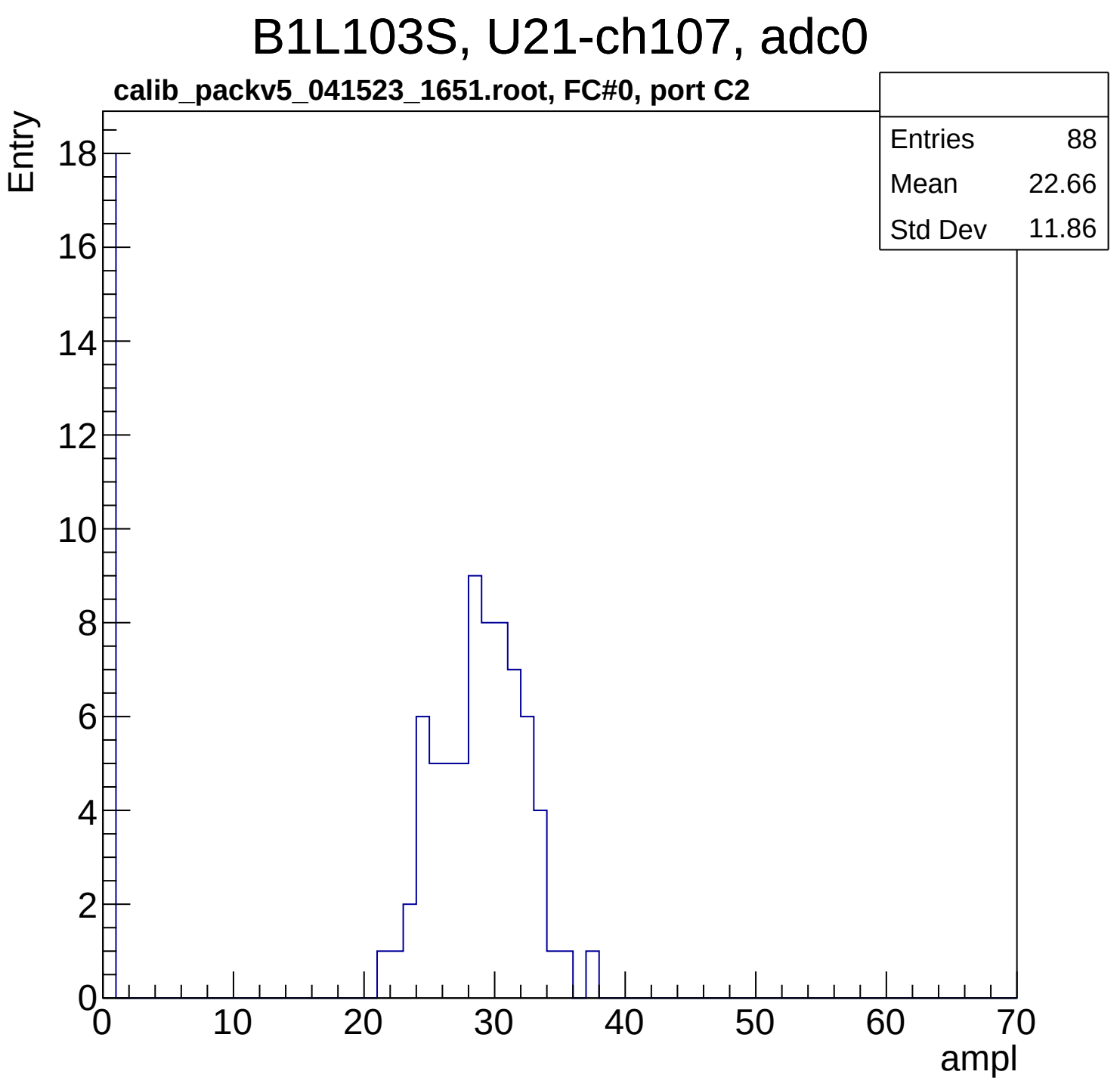
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch107, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 22.66
Std Dev 11.86
Entry
0
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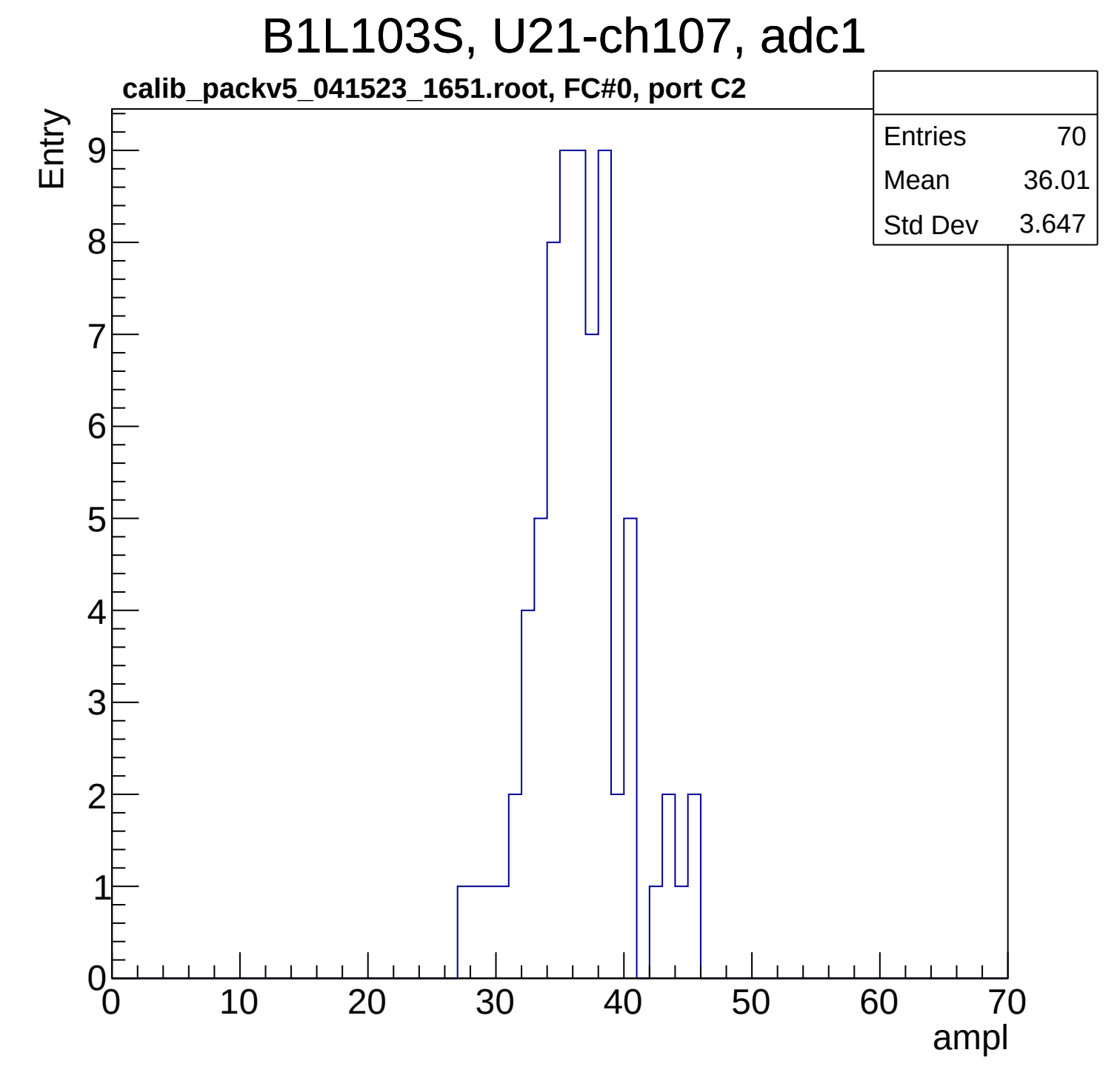
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch107, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 36.01
Std Dev 3.647
Entry
ampl
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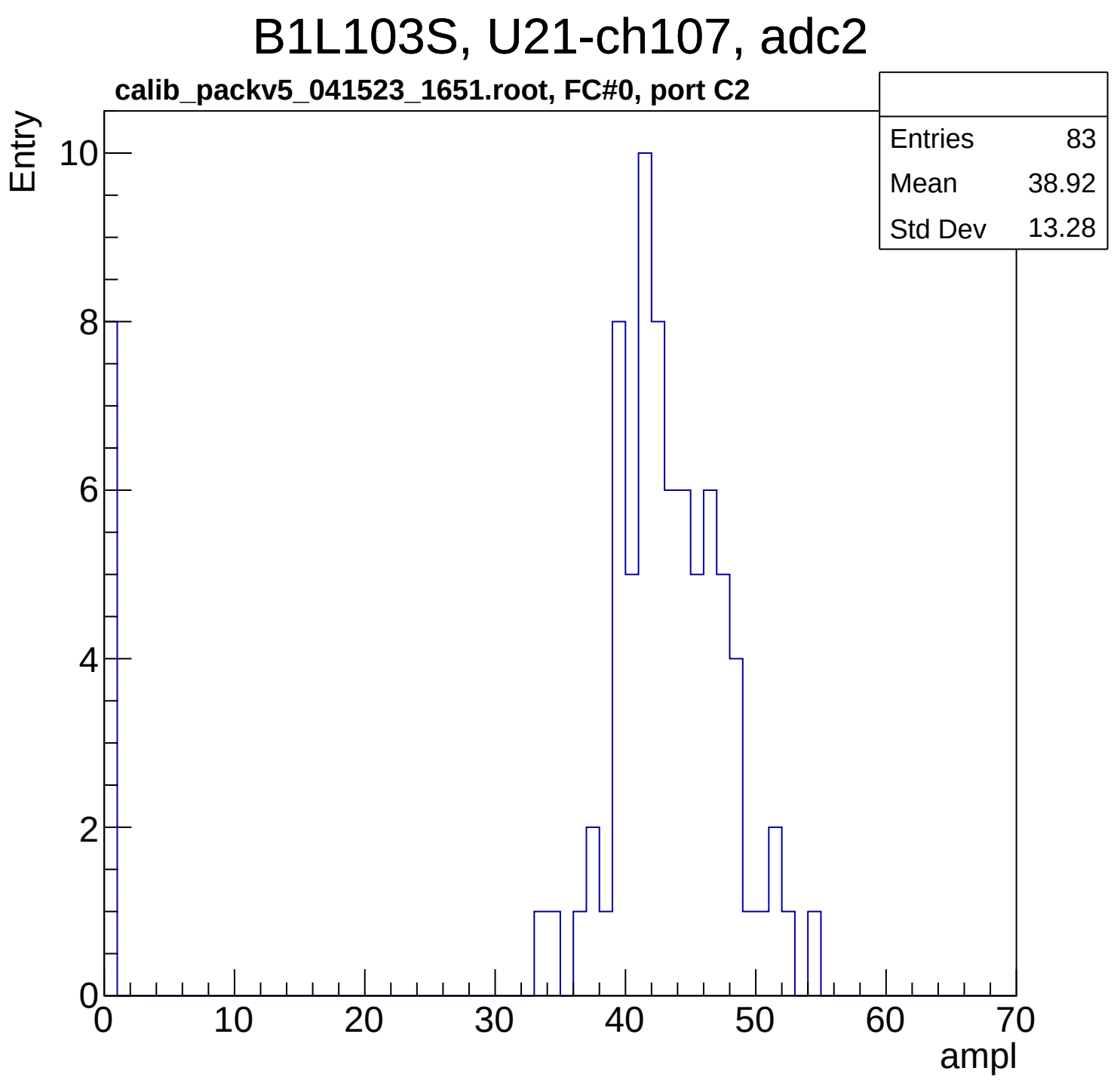
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch107, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 38.92
Std Dev 13.28
Entry
ampl
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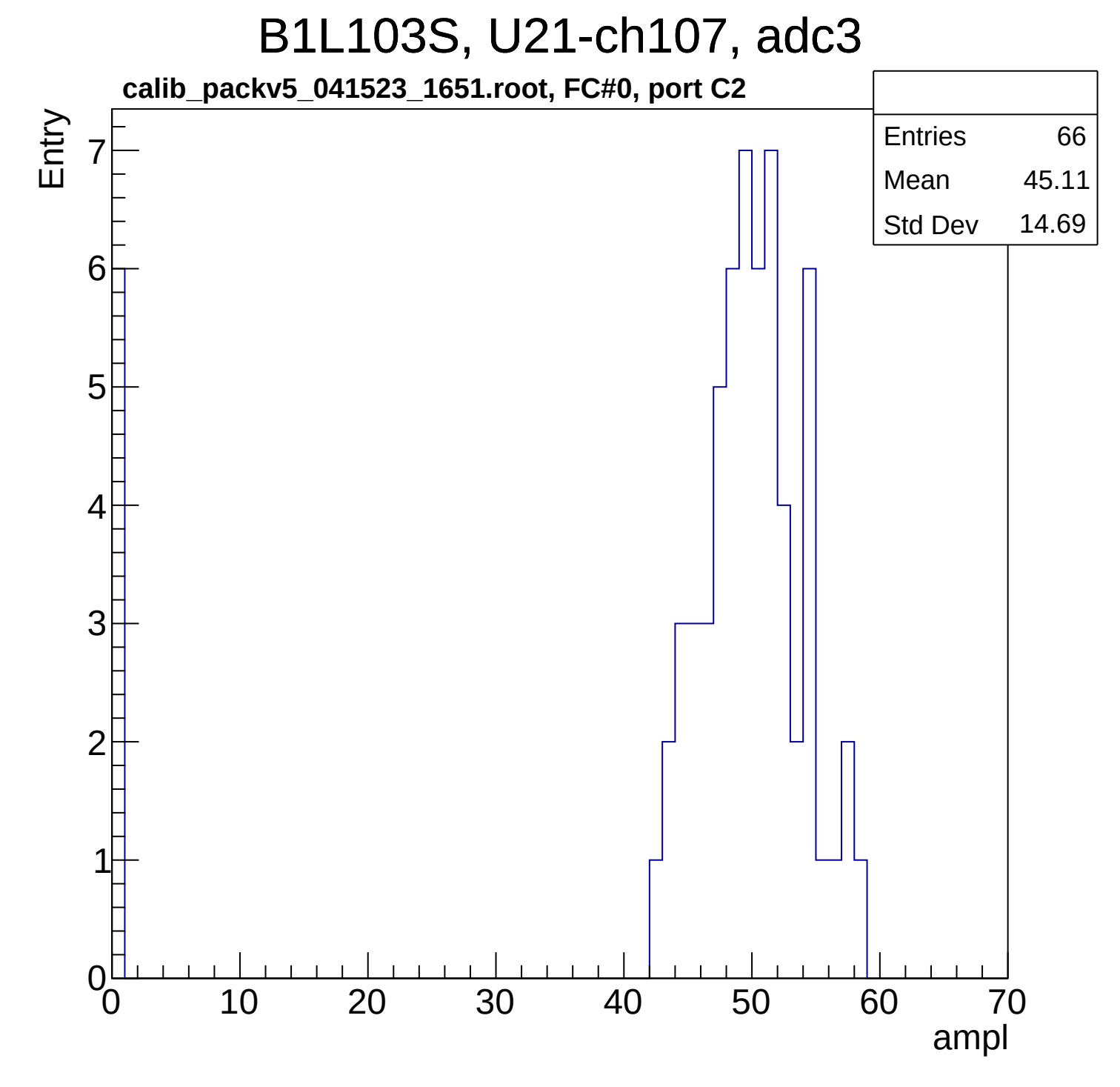
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U21-ch107, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 45.11
Std Dev 14.69
Entry
ampl
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1
2
3
4
5
6
7
0
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20
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40
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60
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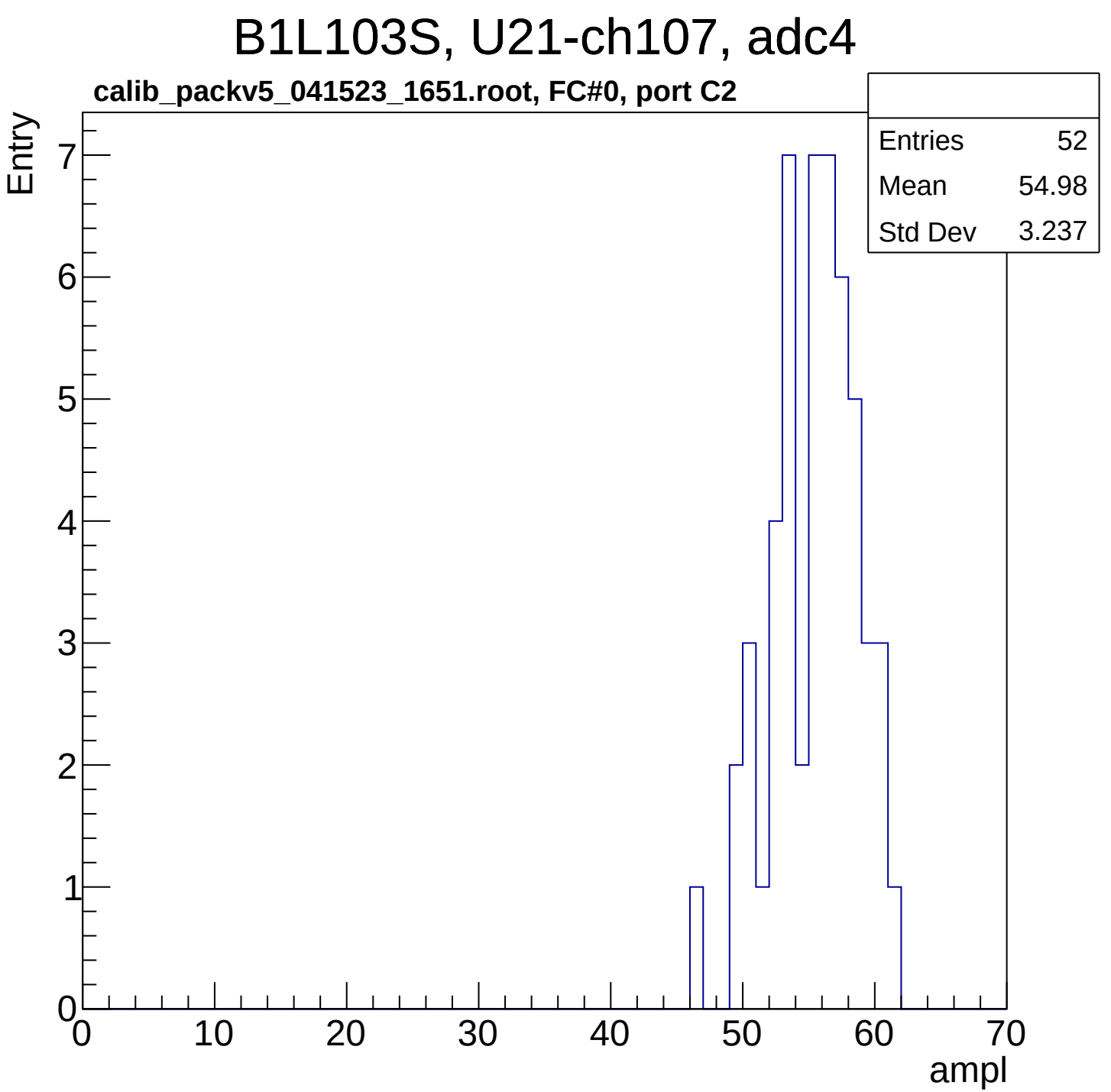
B1L103S, U21-ch107, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 54.98
Std Dev 3.237
Entry
ampl
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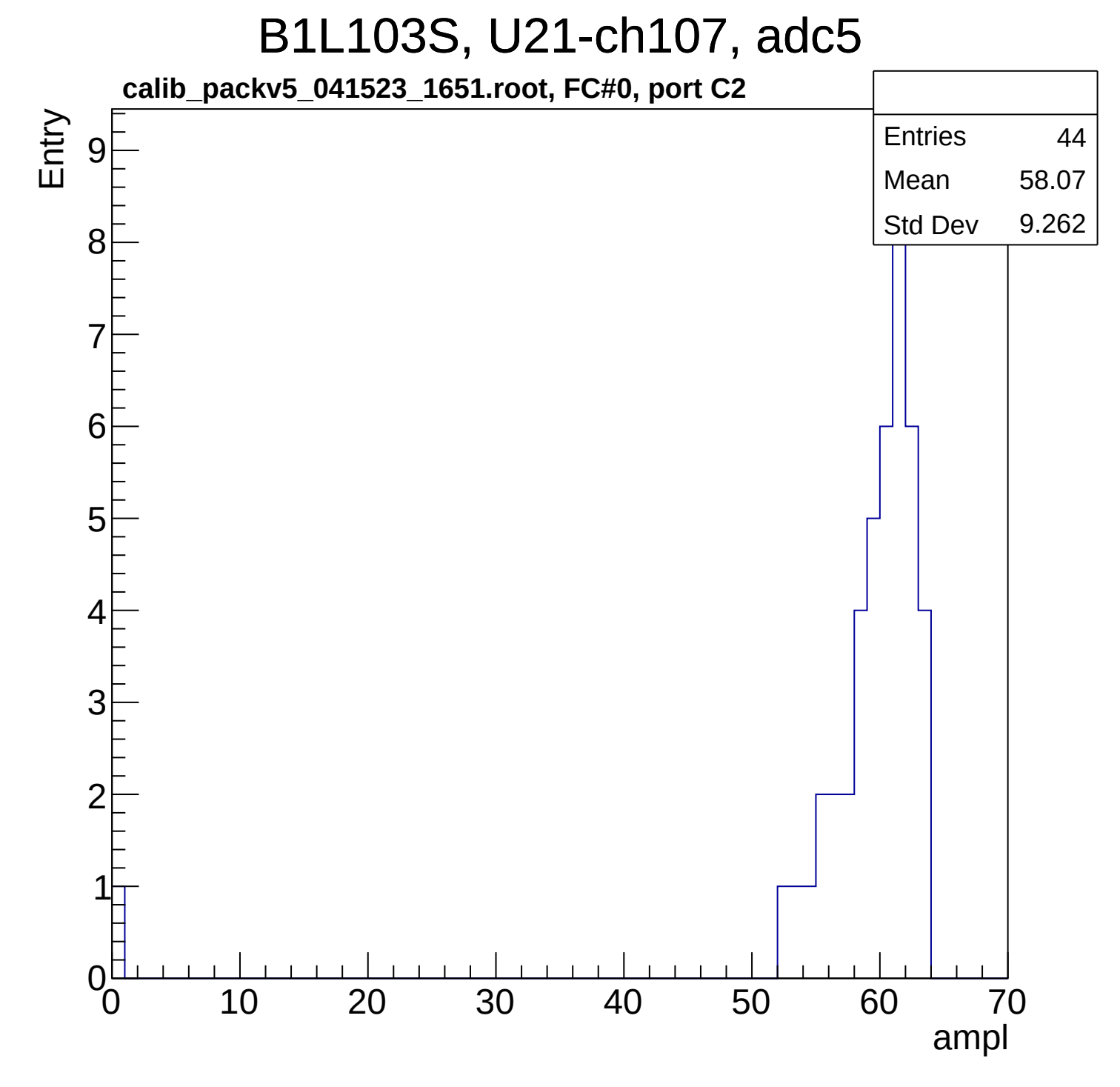
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U21-ch107, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 58.07
Std Dev 9.262
Entry
ampl
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3
4
5
6
7
8
9
0
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60
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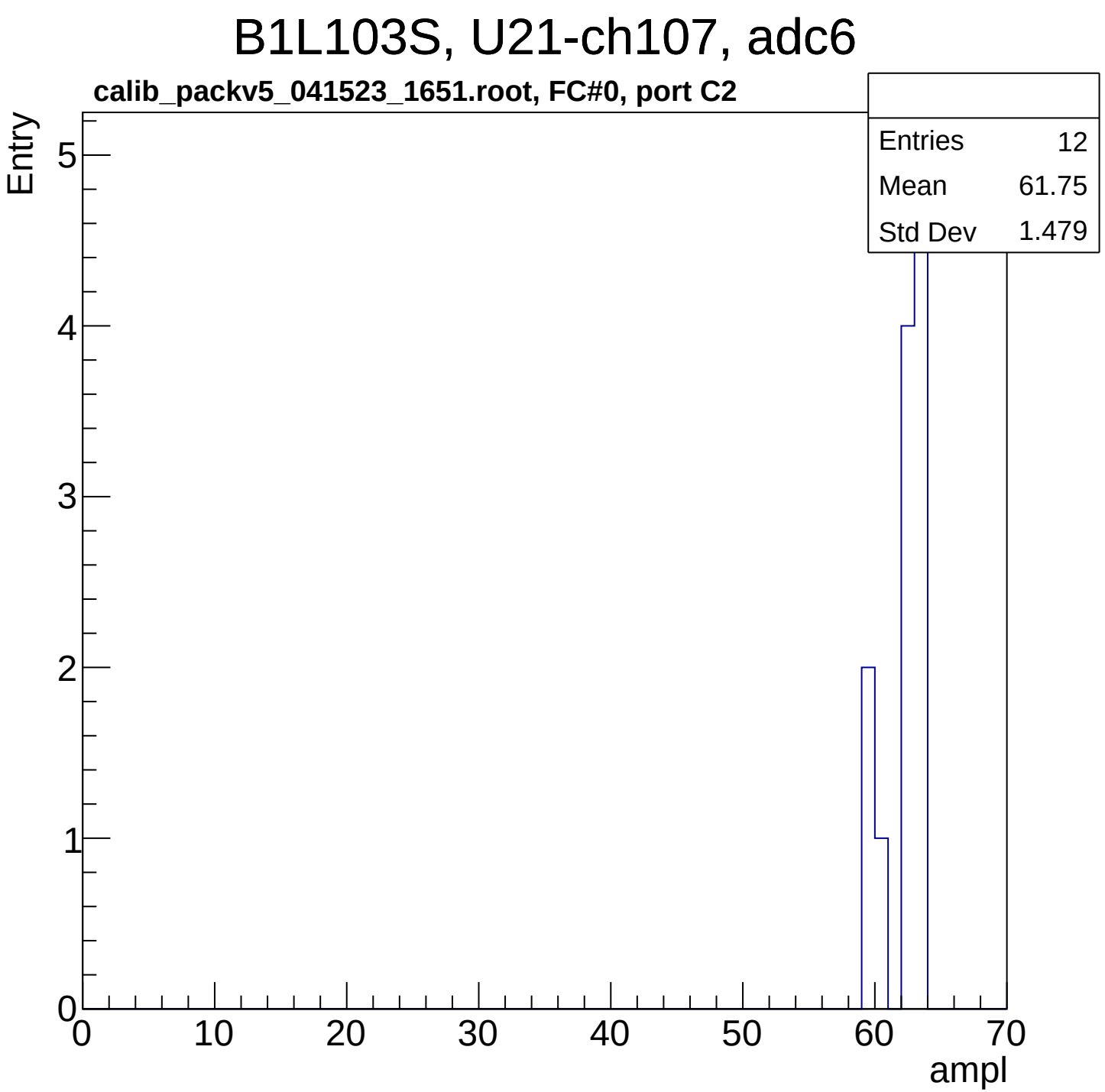
B1L103S, U21-ch107, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.75
Std Dev 1.479
Entry
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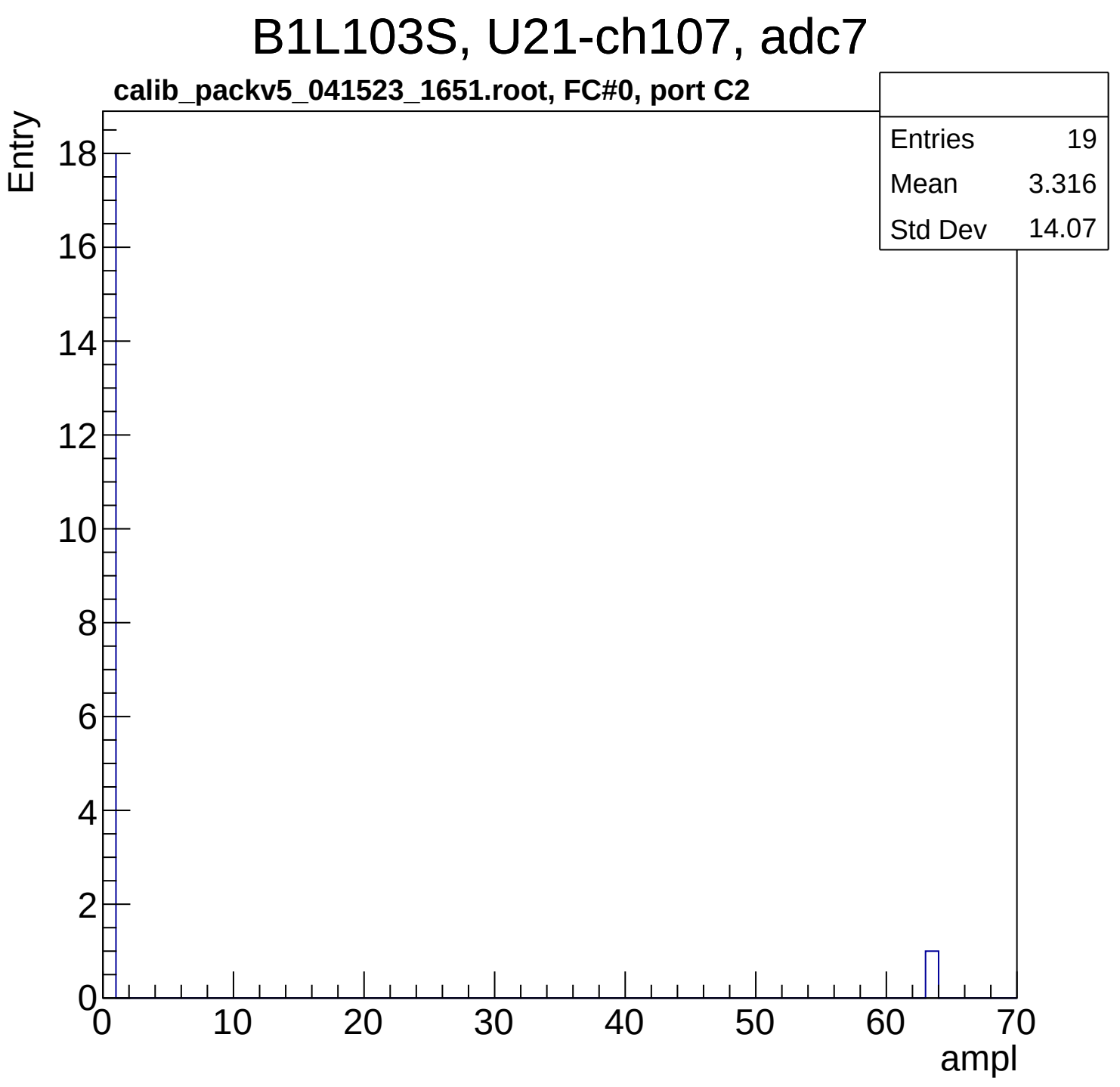
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch107, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.316
Std Dev 14.07
Entry
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6
8
10
12
14
16
18
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10
20
30
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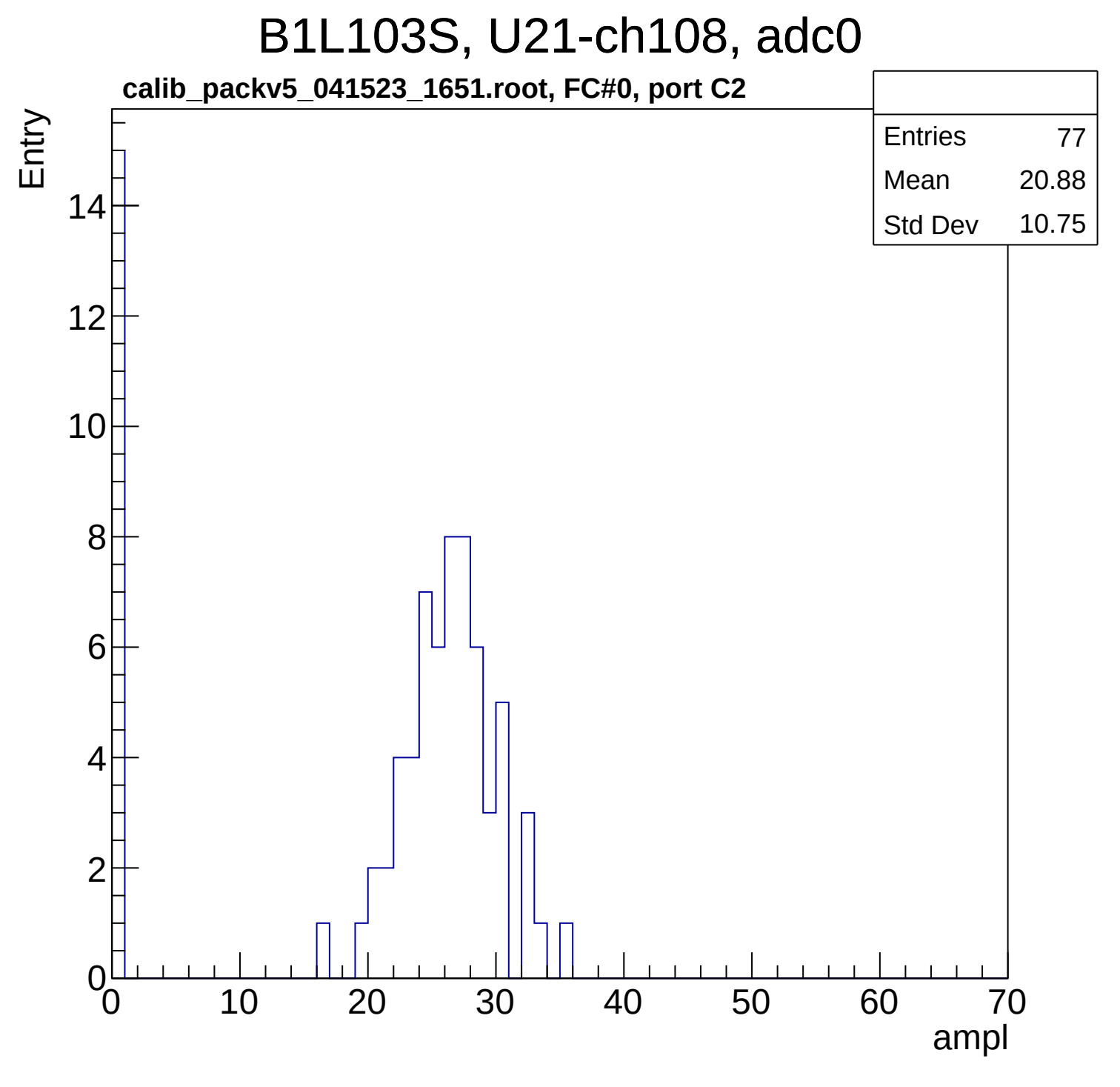
50
60
70
ampl


B1L103S, U21-ch108, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 20.88
Std Dev 10.75
Entry
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4
6
8
10
12
14
0
10
20
30
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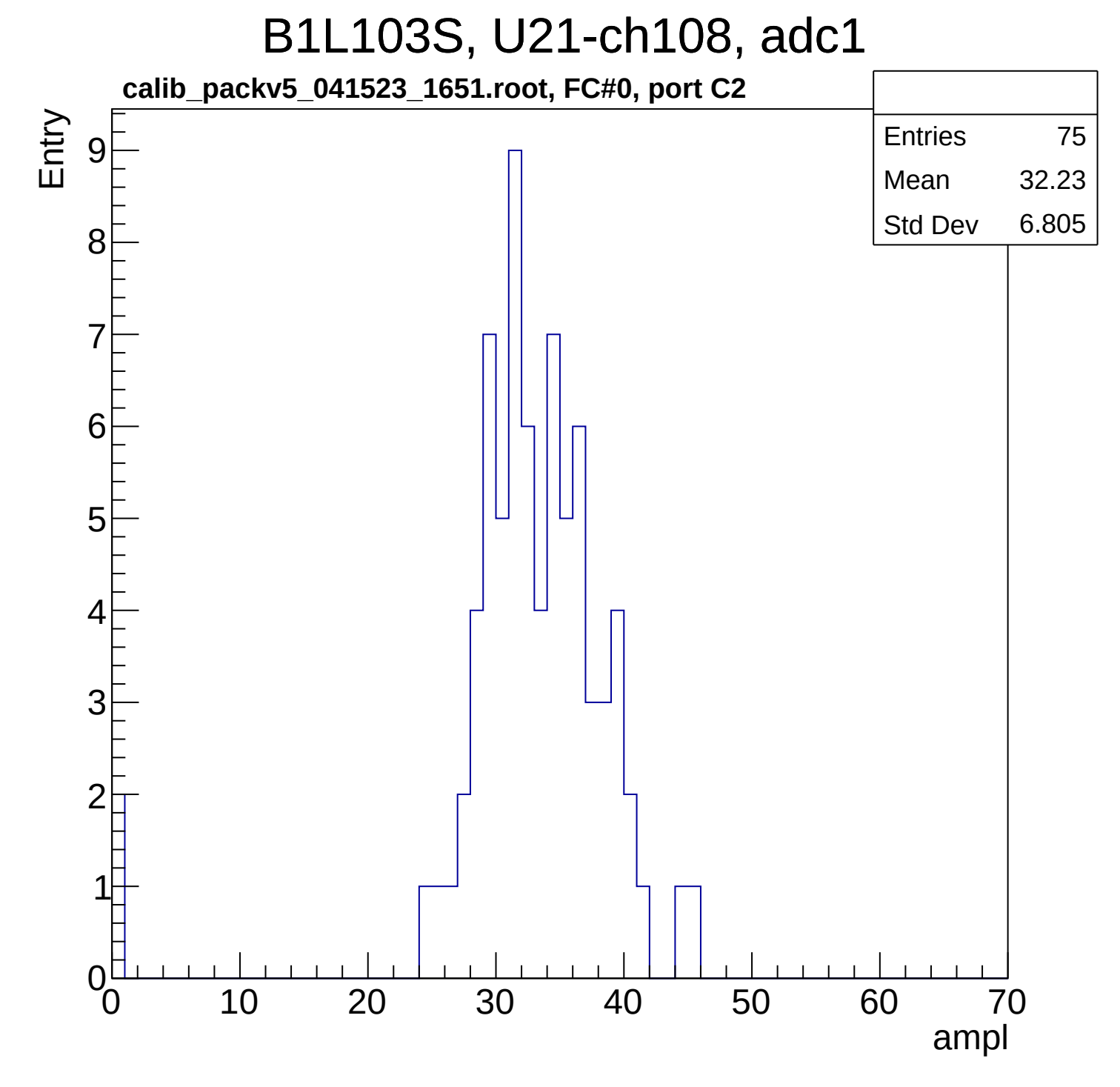
50
60
70
ampl


B1L103S, U21-ch108, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 32.23
Std Dev 6.805
Entry
ampl
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3
4
5
6
7
8
9
0
10
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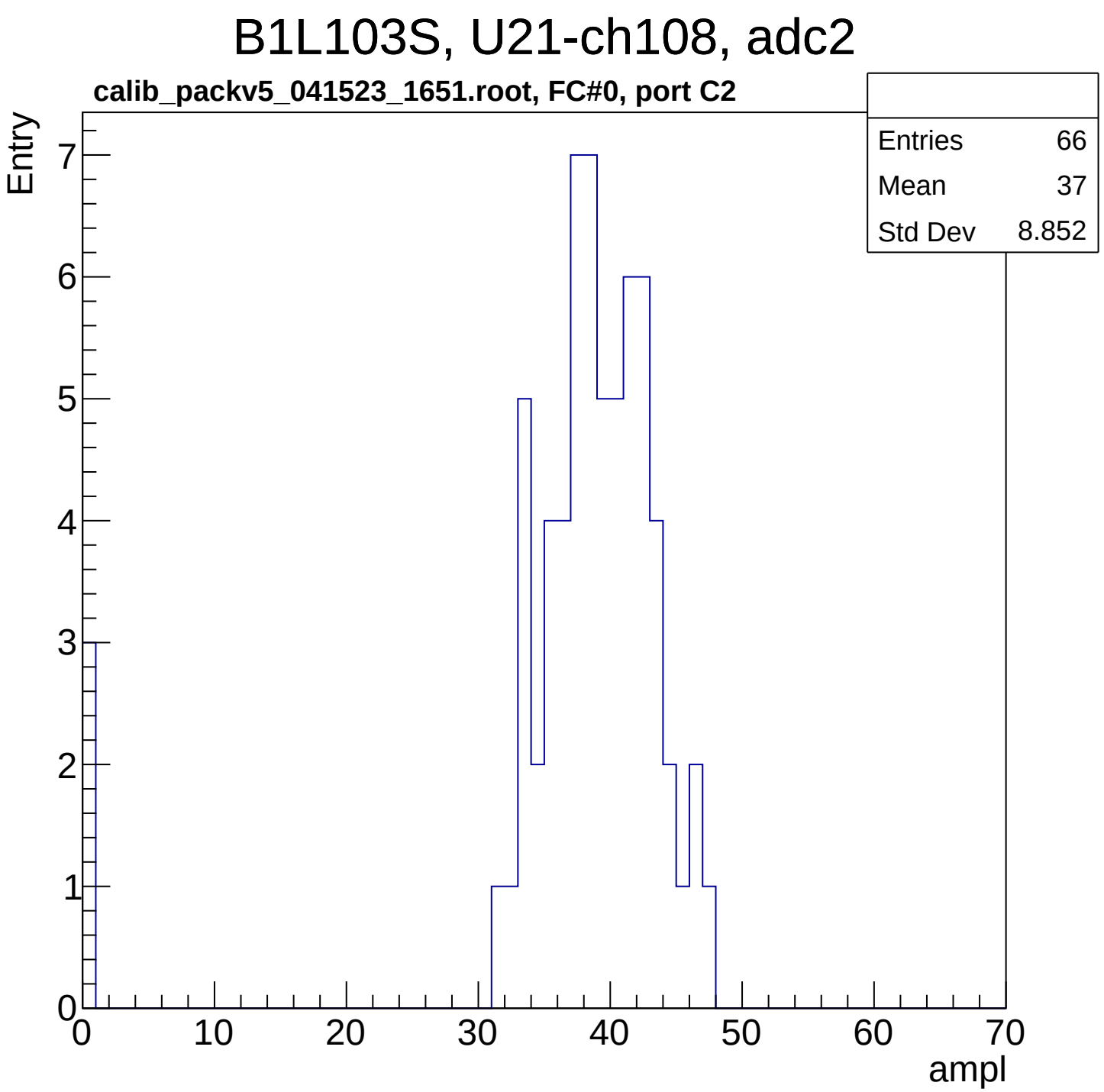
B1L103S, U21-ch108, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 37
Std Dev 8.852
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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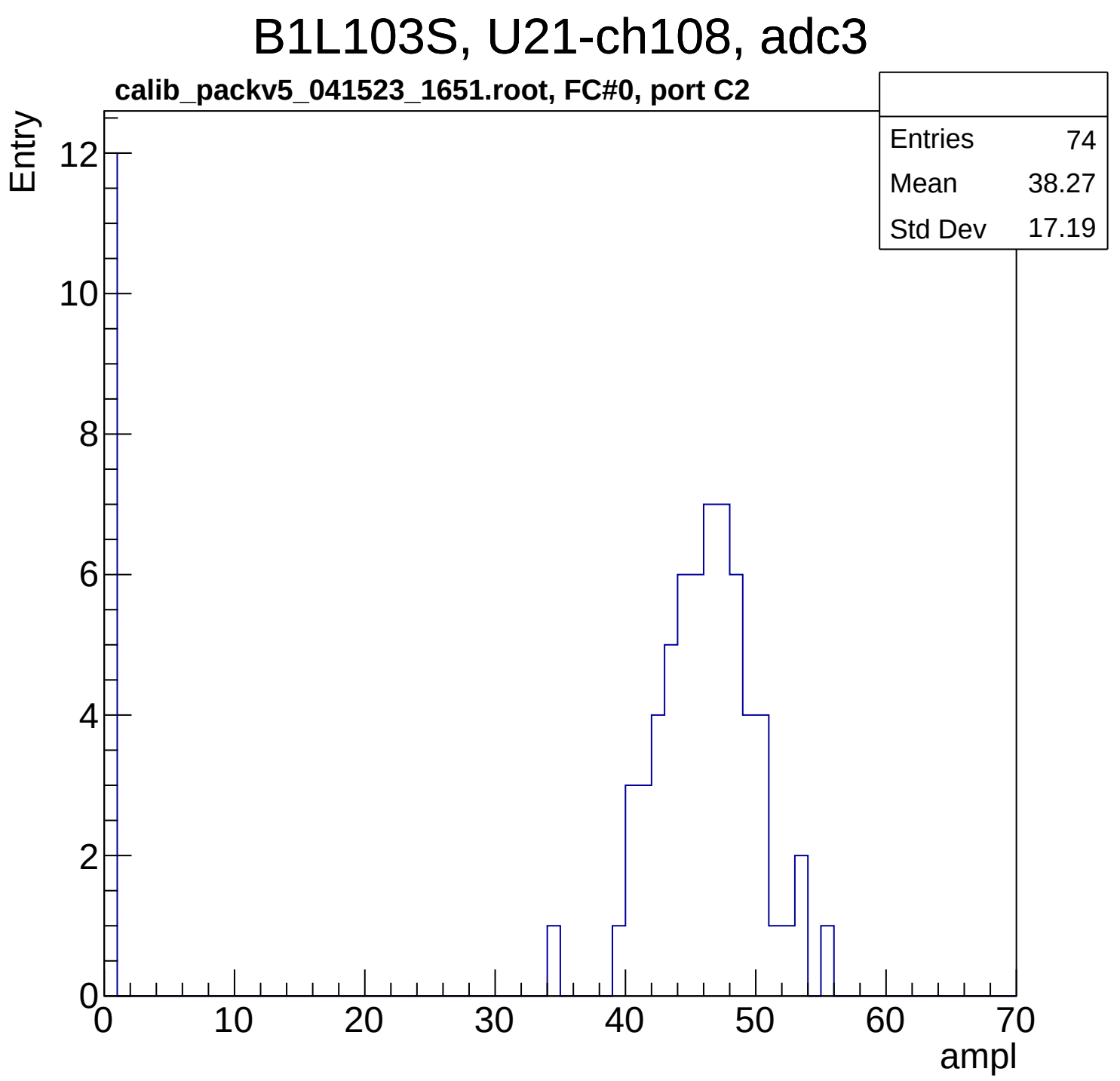
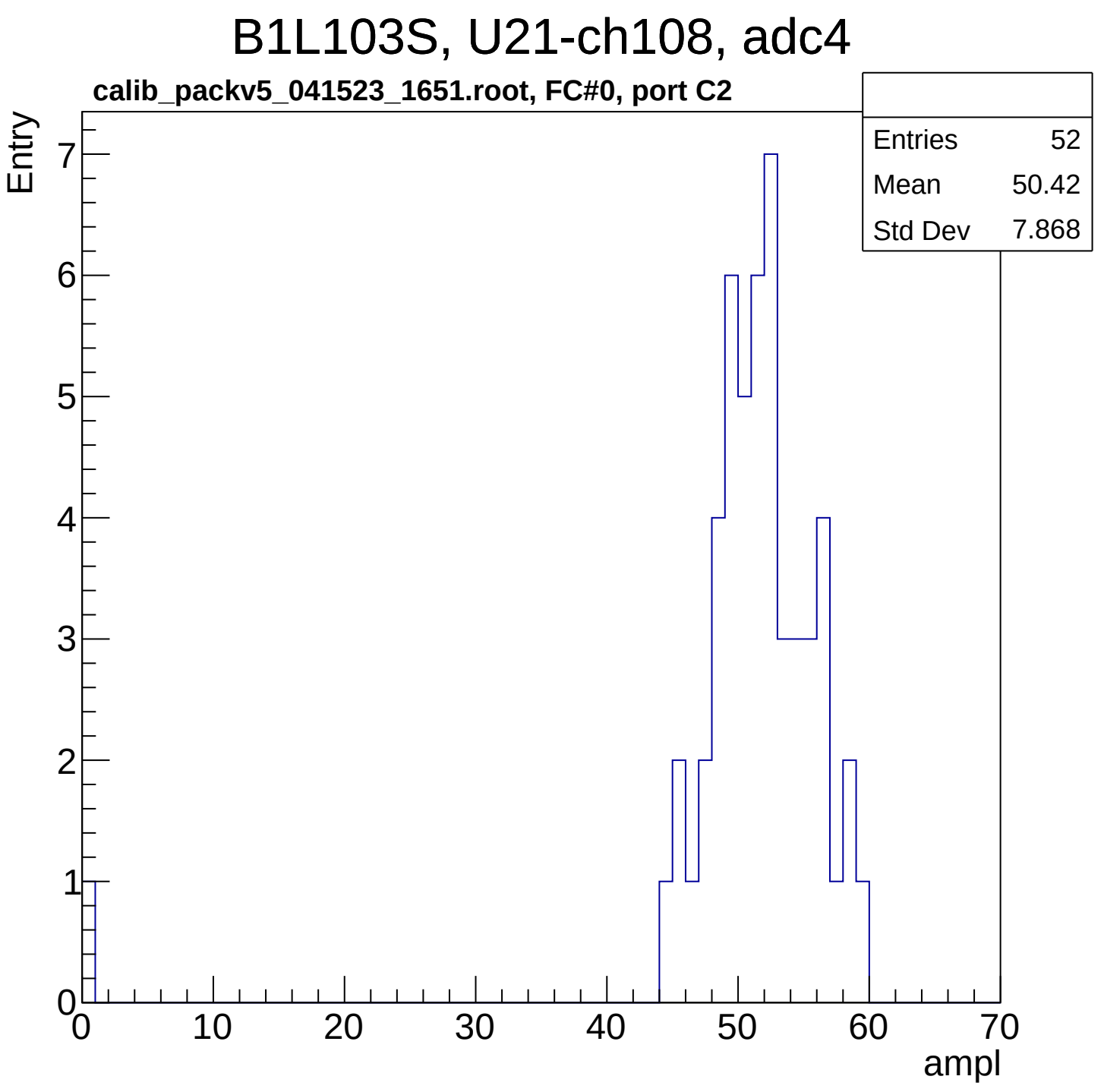
40
50
60
70


B1L103S, U21-ch108, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 38.27
Std Dev 17.19
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U21-ch108, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 50.42
Std Dev 7.868
Entry
ampl
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2
3
4
5
6
7
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10
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40
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60
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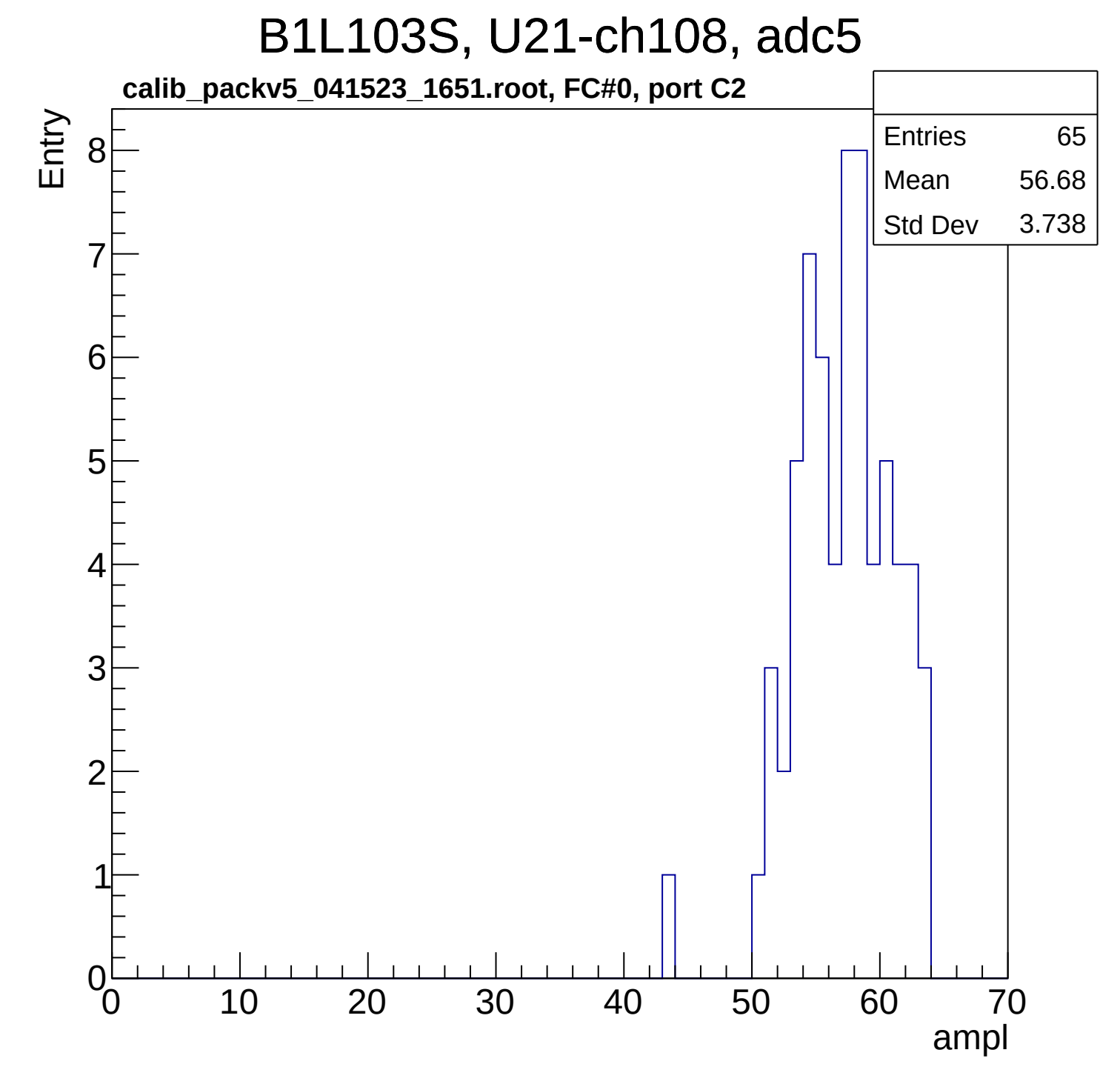
B1L103S, U21-ch108, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 56.68
Std Dev 3.738
Entry
ampl
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4
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6
7
8
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50
60
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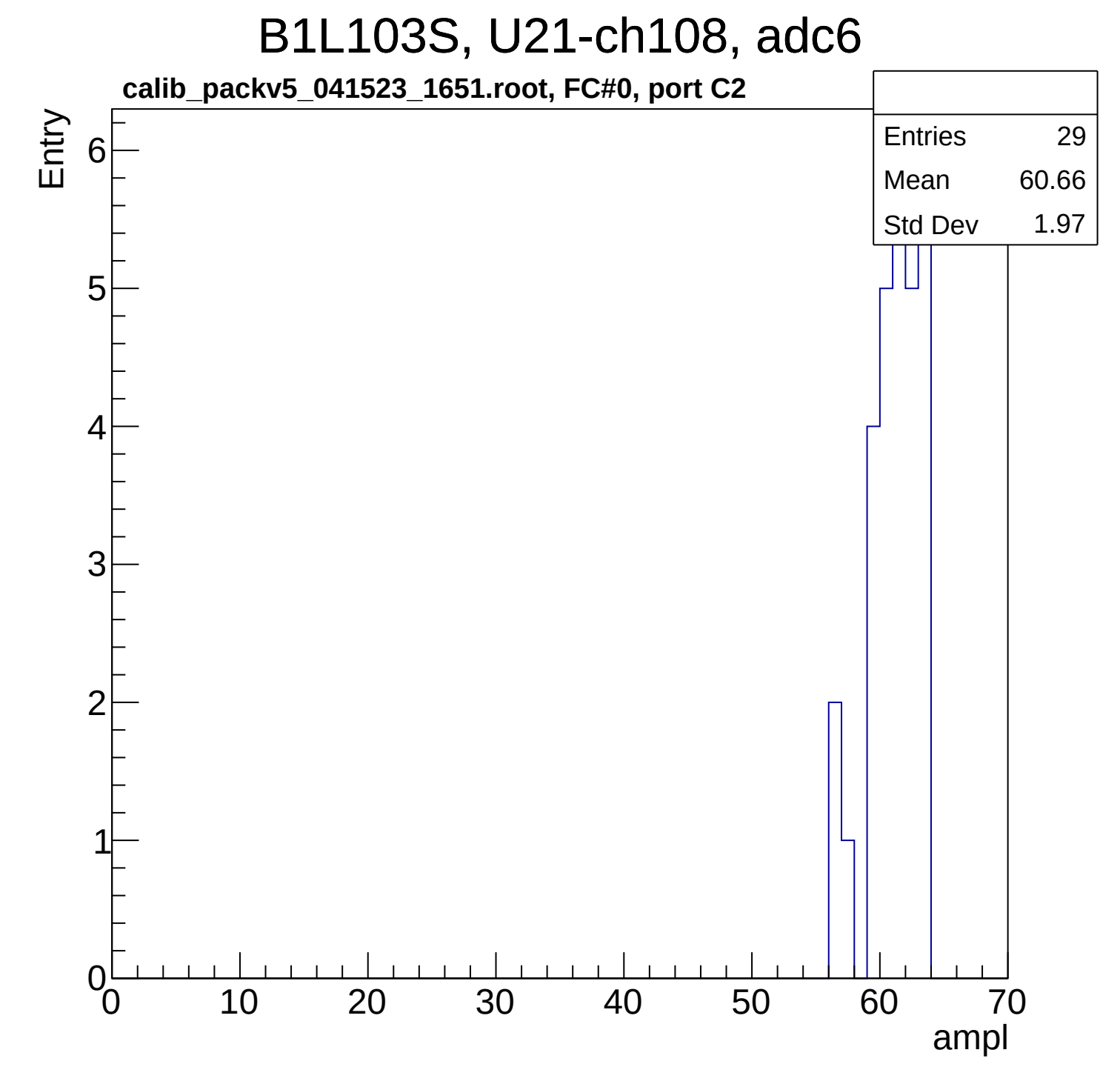
B1L103S, U21-ch108, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 60.66
Std Dev 1.97
Entry
ampl
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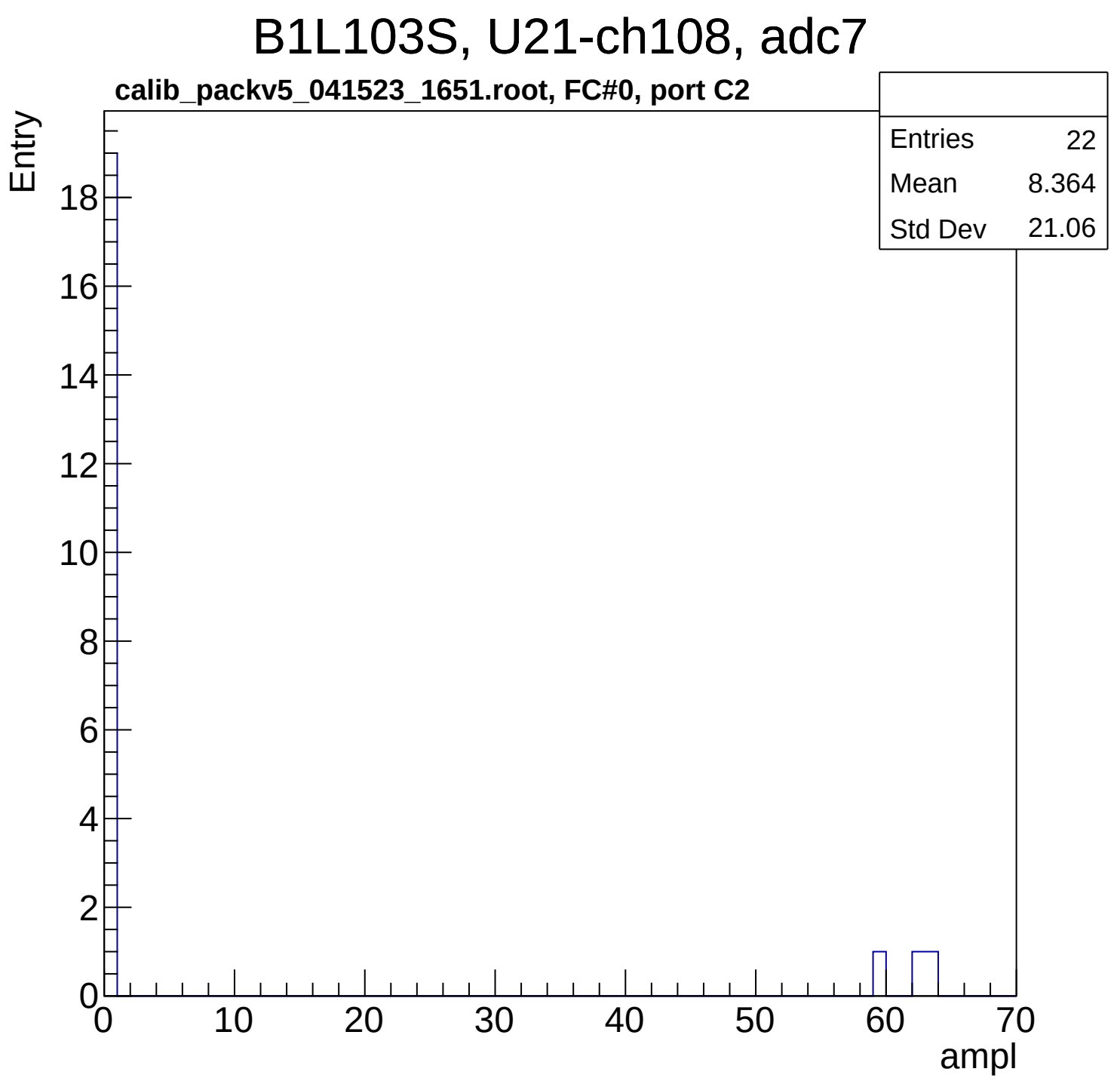
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U21-ch108, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.364
Std Dev 21.06
Entry
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6
8
10
12
14
16
18
0
10
20
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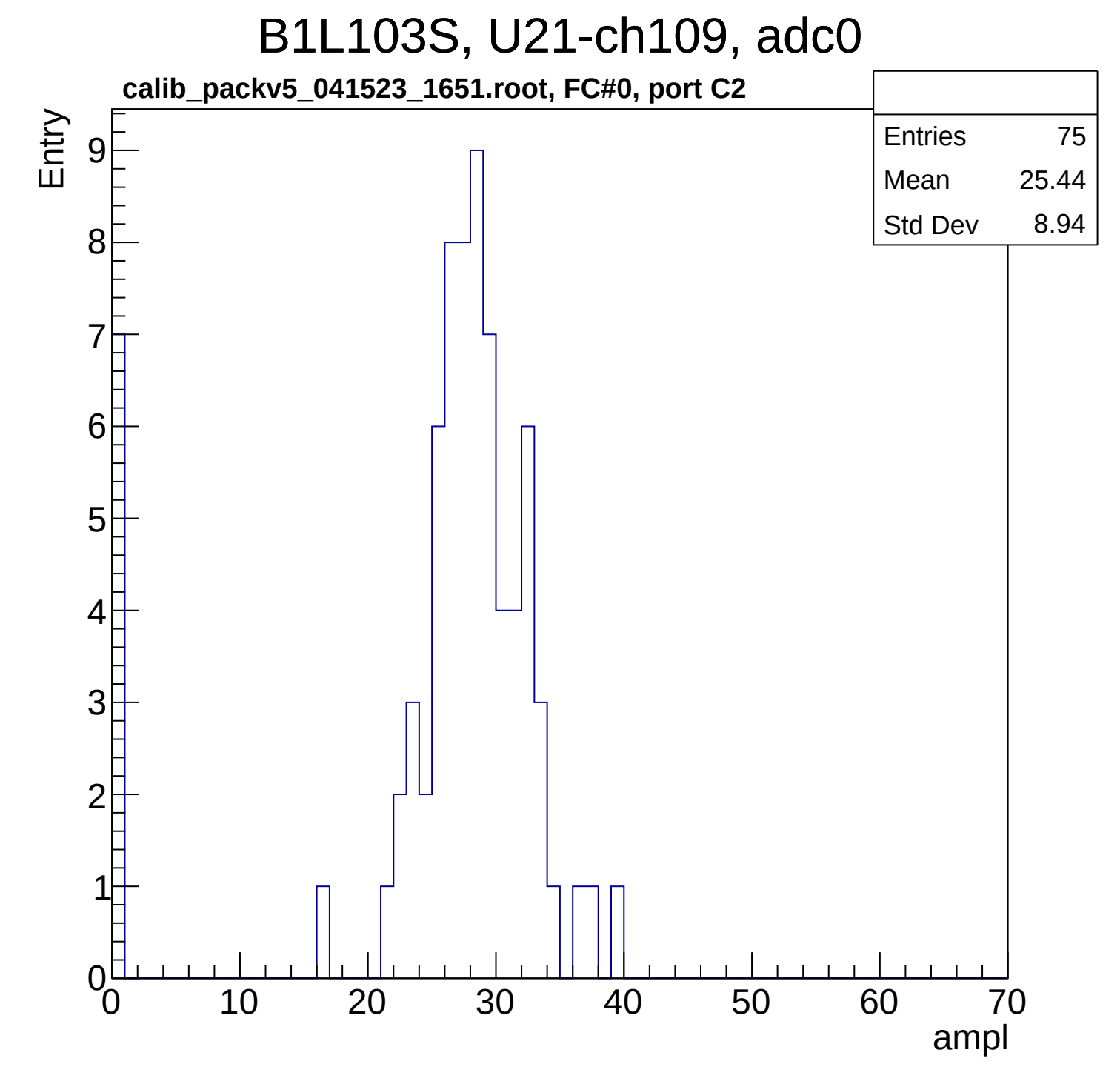
50
60
70
ampl


B1L103S, U21-ch109, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 25.44
Std Dev 8.94
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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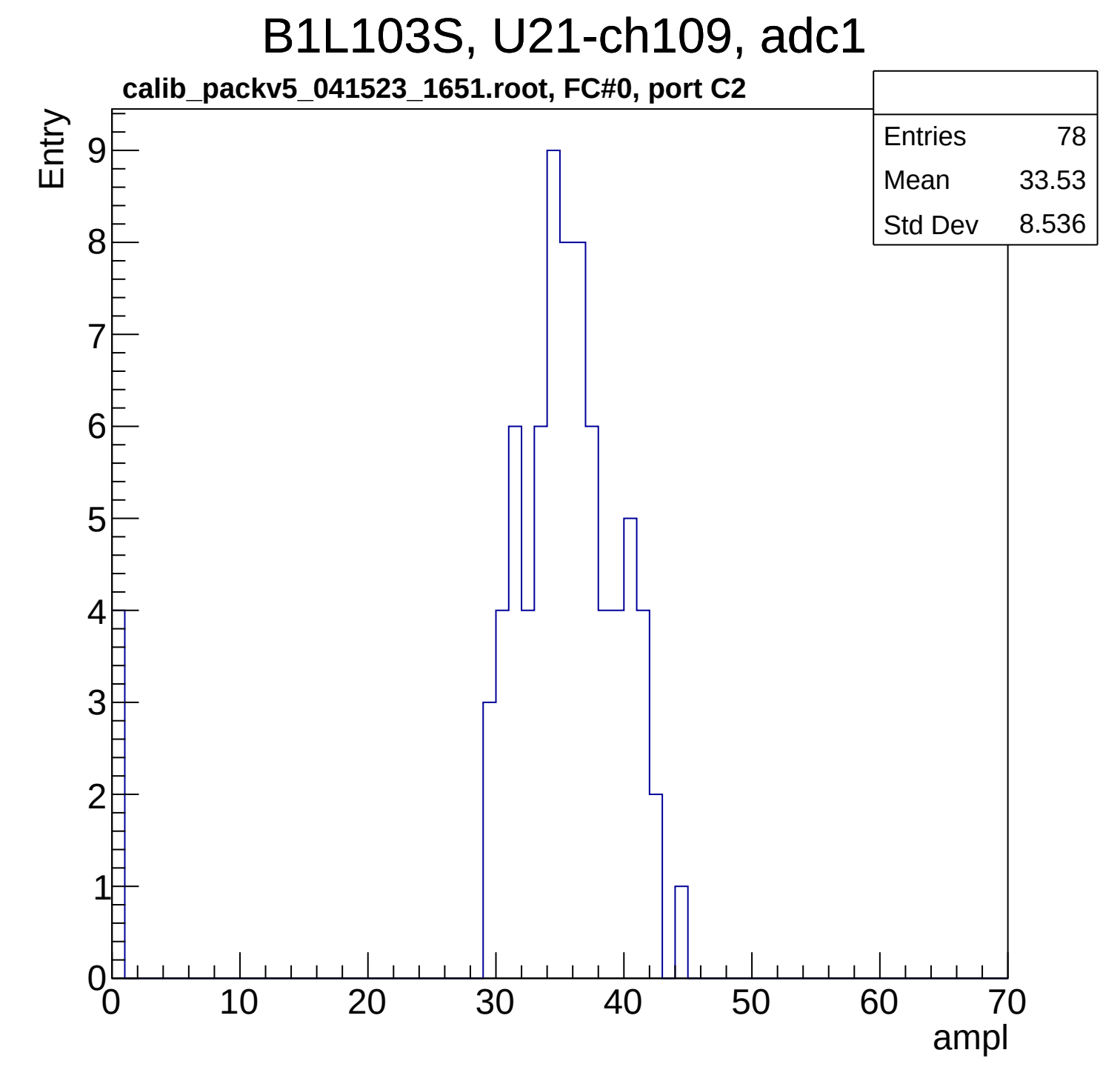
B1L103S, U21-ch109, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 33.53
Std Dev 8.536
Entry
ampl
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2
3
4
5
6
7
8
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0
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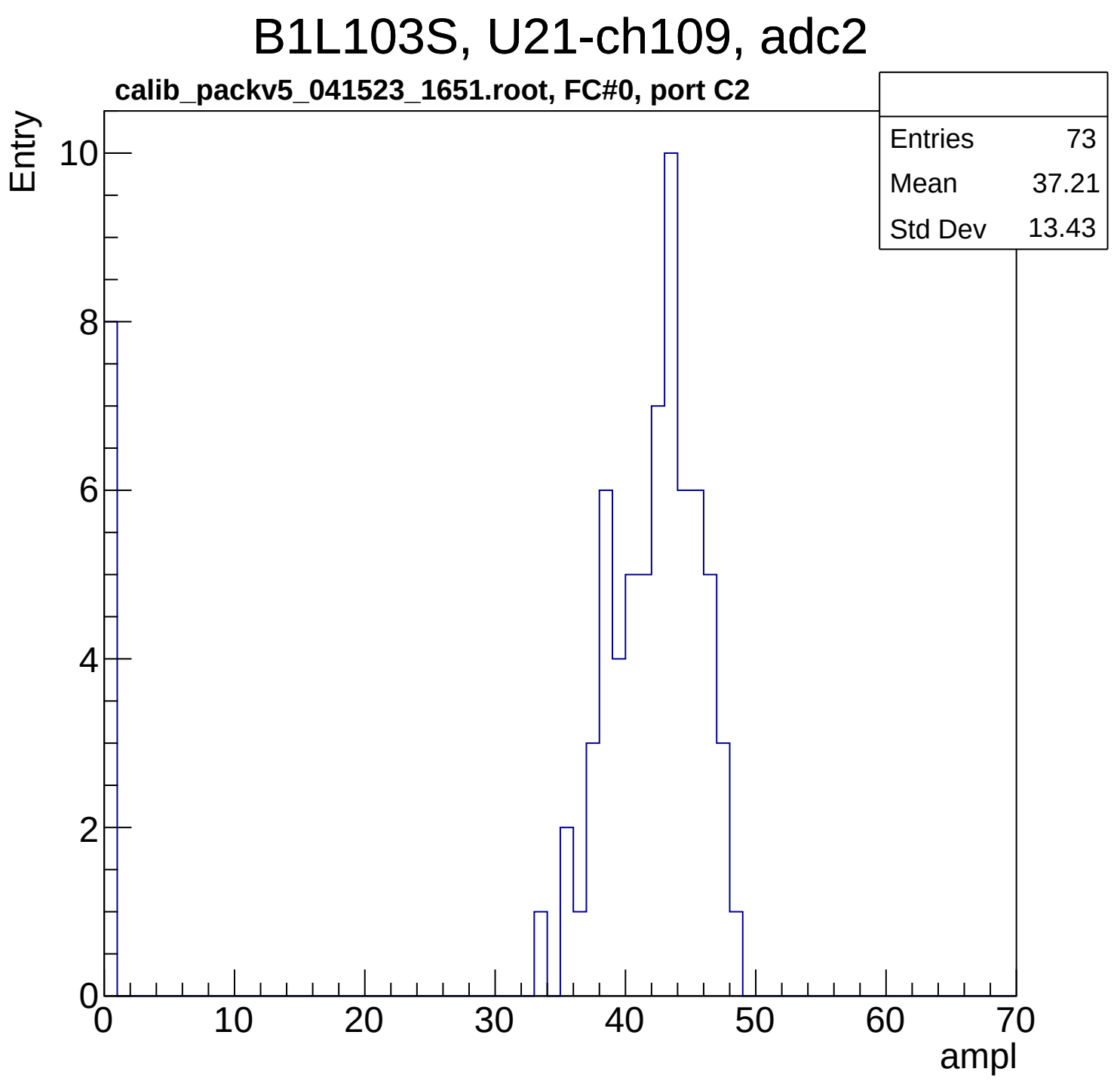
B1L103S, U21-ch109, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 37.21
Std Dev 13.43
Entry
ampl
0
2
4
6
8
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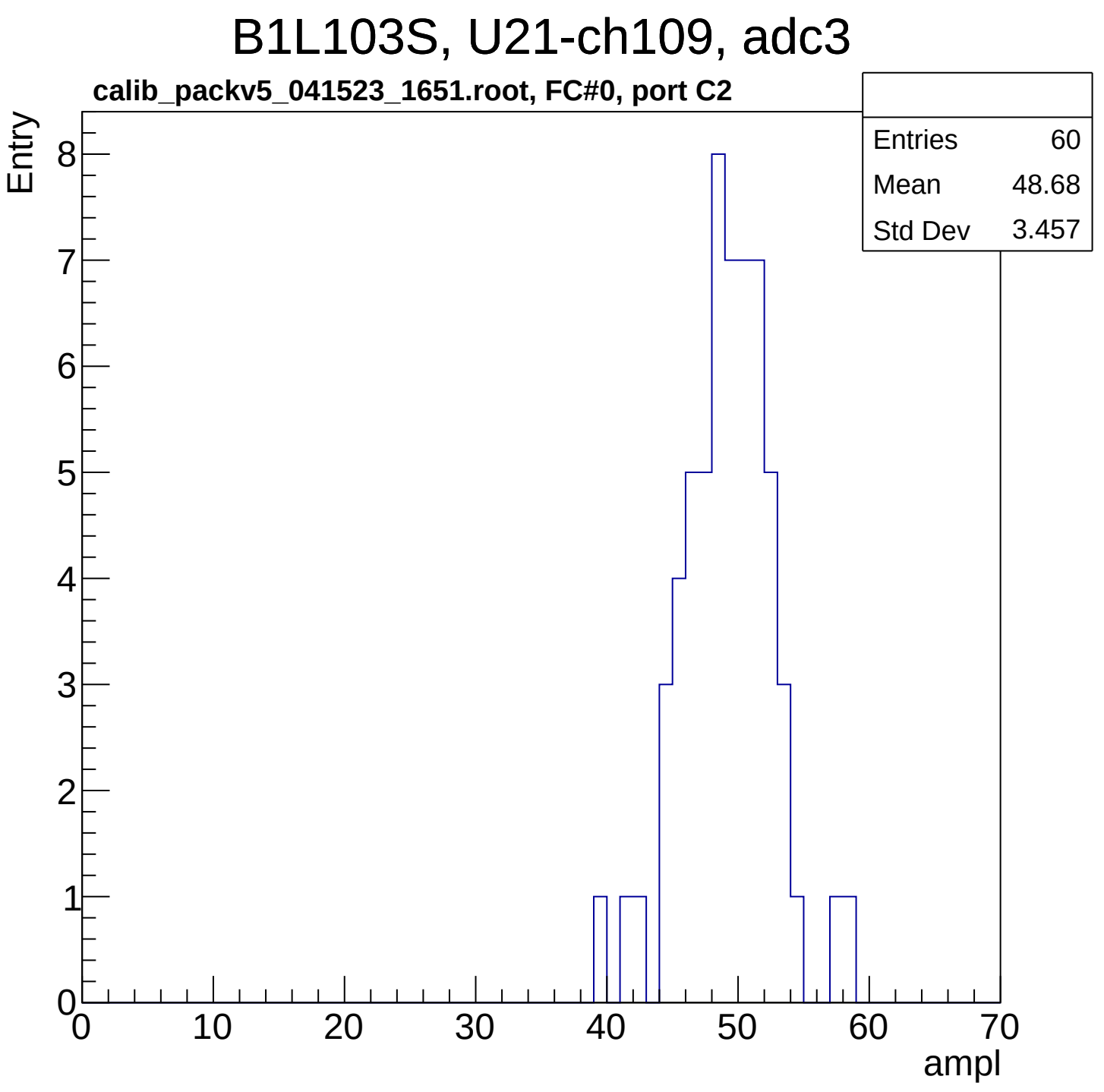
0
10
20
30
40
50
60
70


B1L103S, U21-ch109, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 48.68
Std Dev 3.457
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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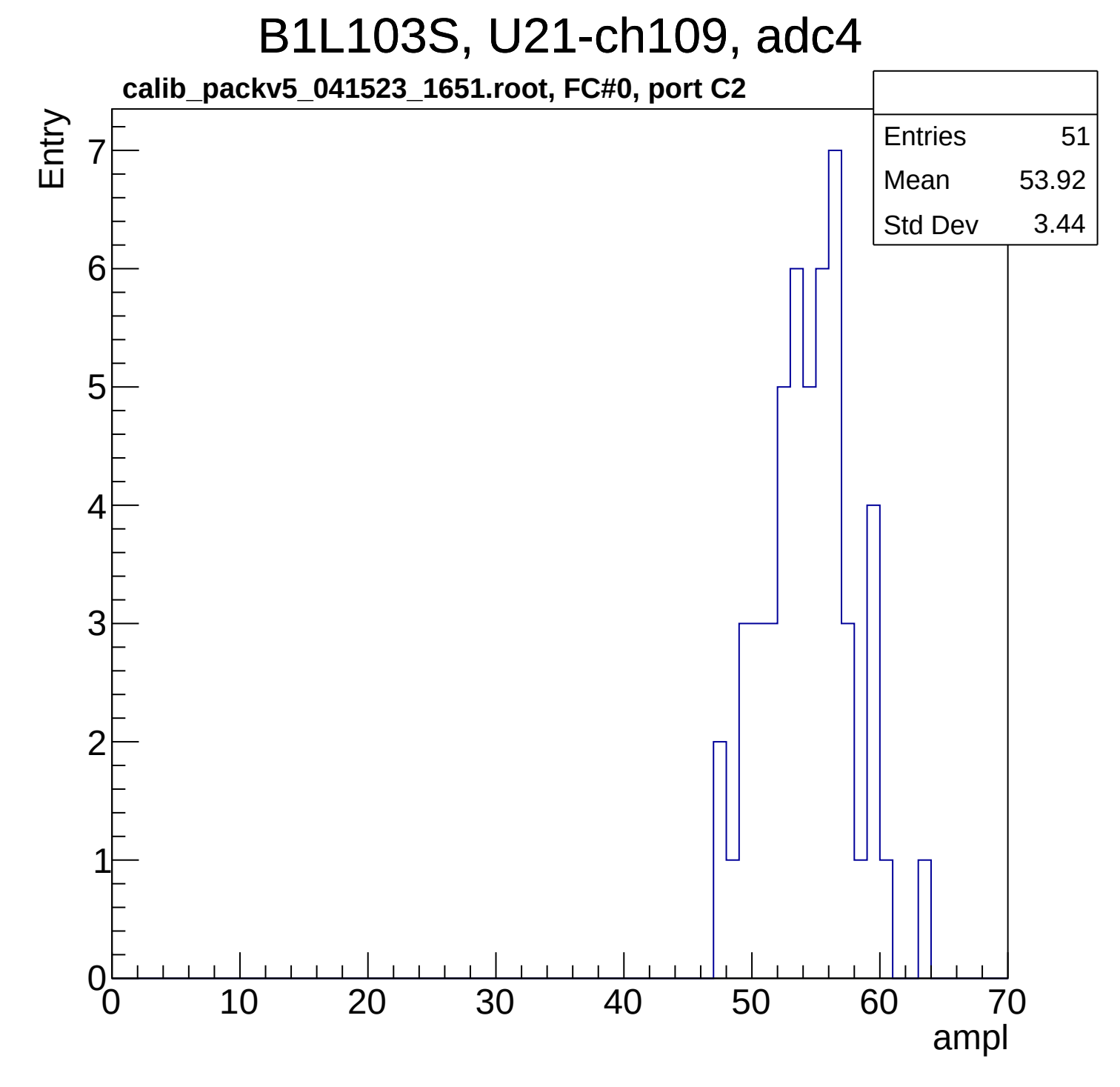
B1L103S, U21-ch109, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 53.92
Std Dev 3.44
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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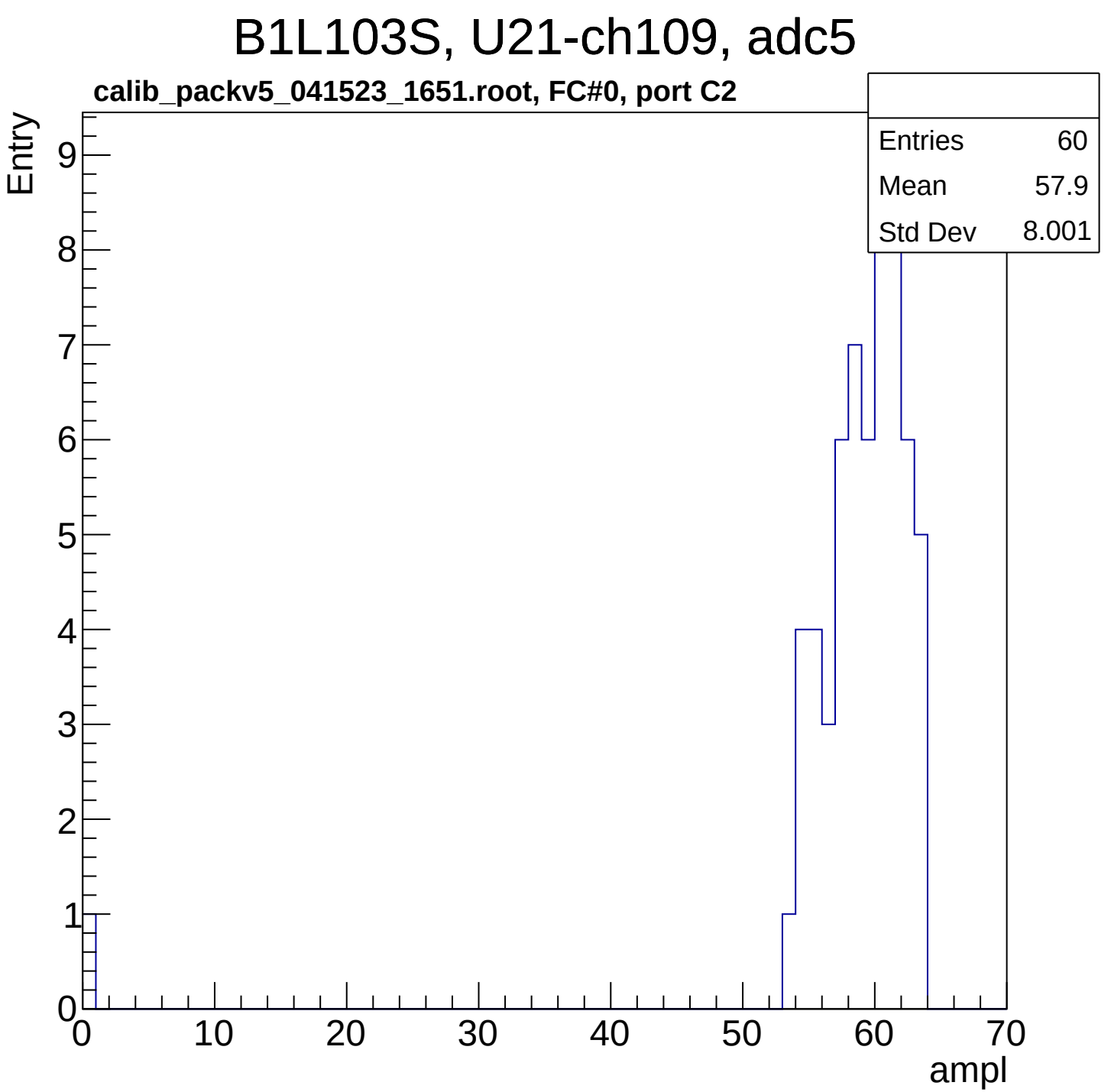
B1L103S, U21-ch109, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 57.9
Std Dev 8.001
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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40
50
60
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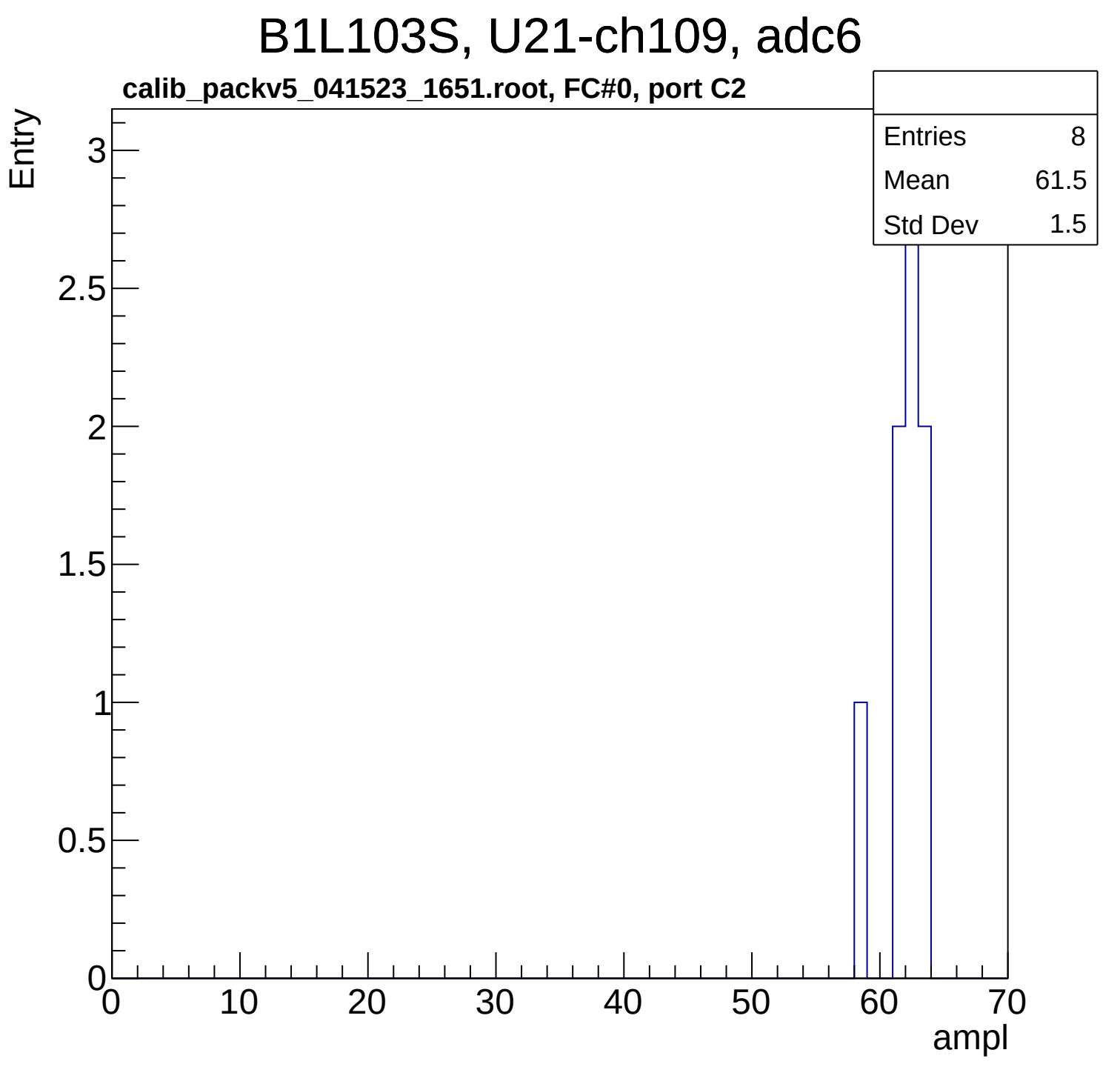
B1L103S, U21-ch109, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 61.5
Std Dev 1.5
Entry
ampl
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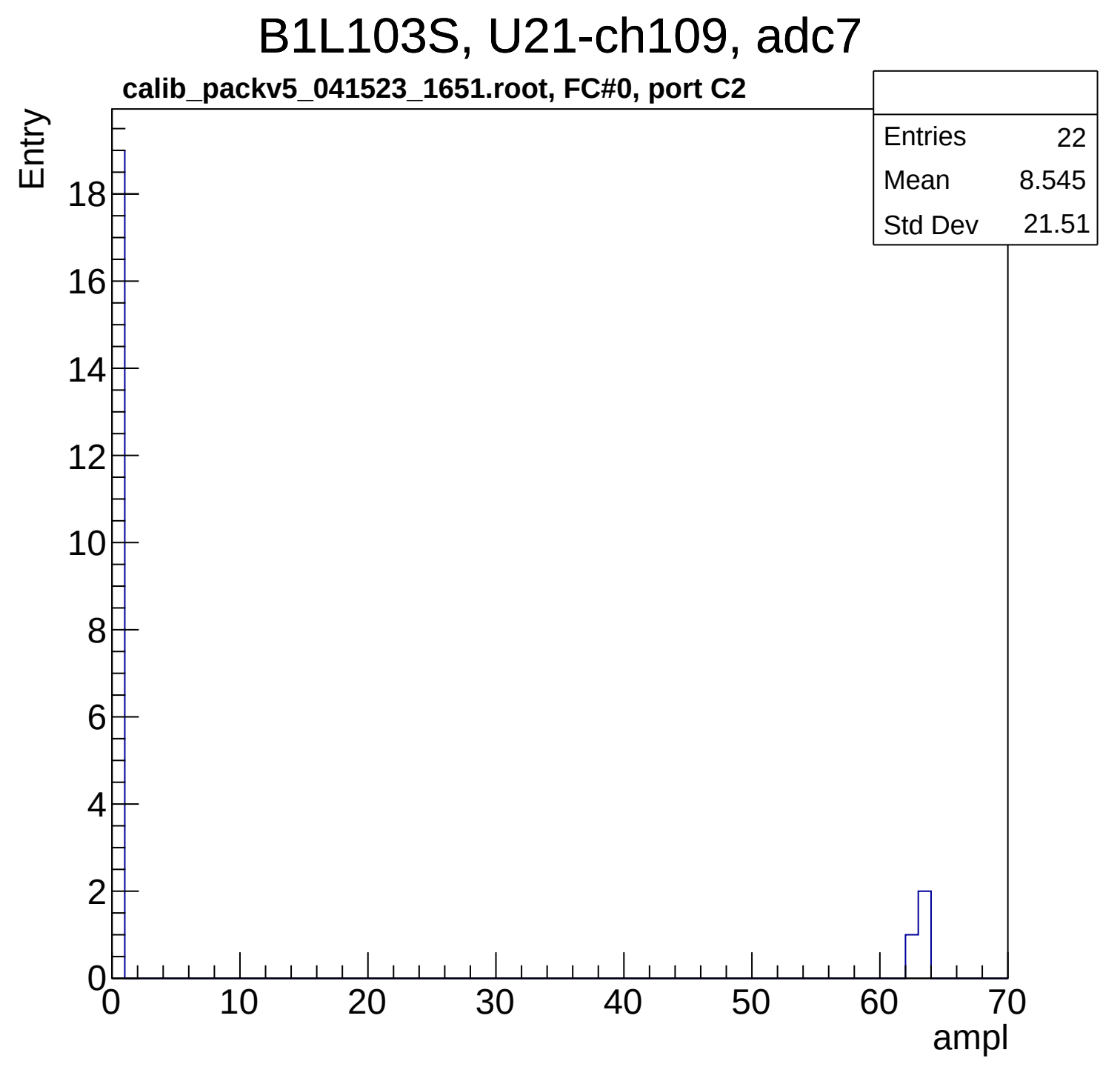
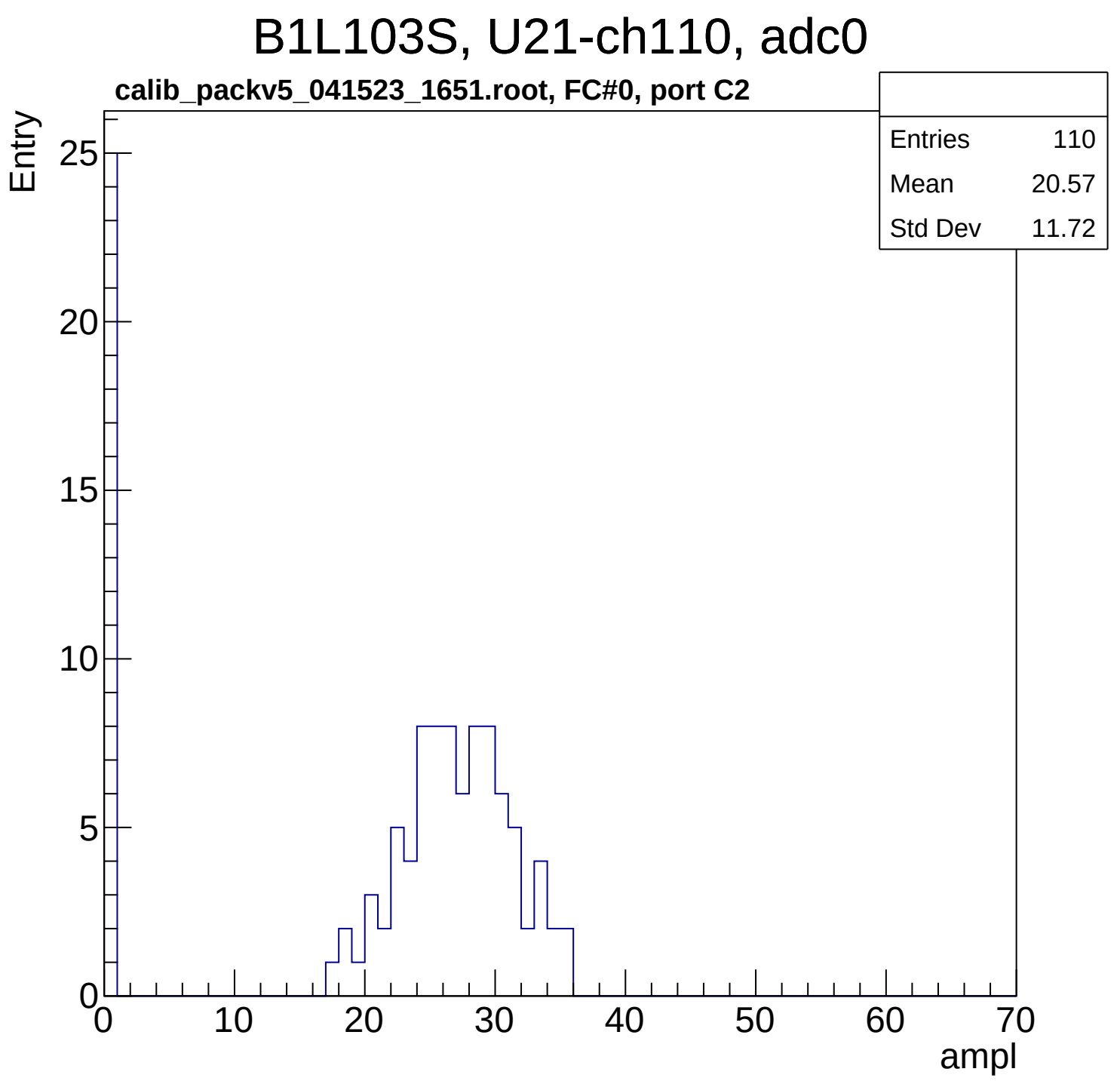
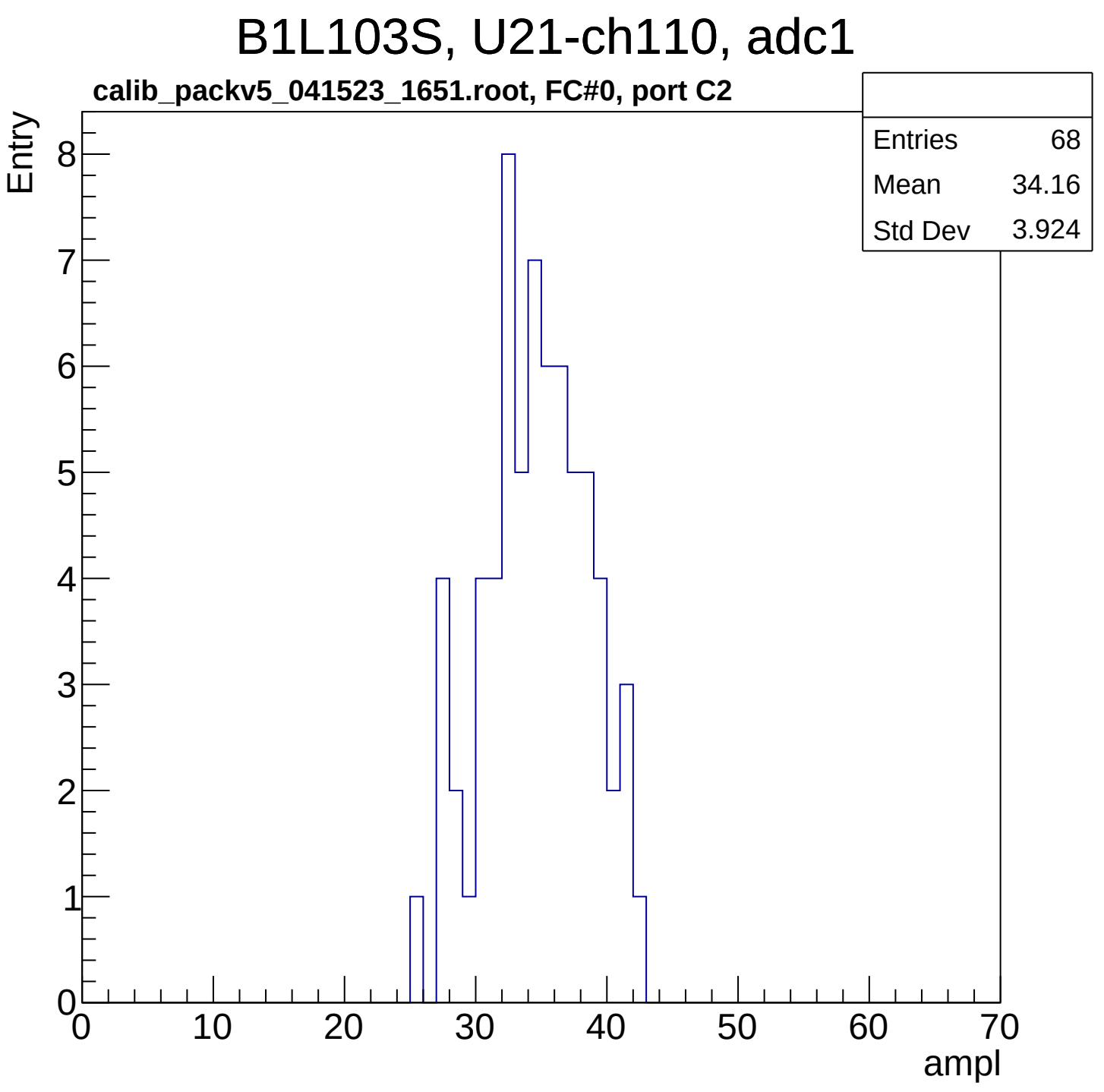
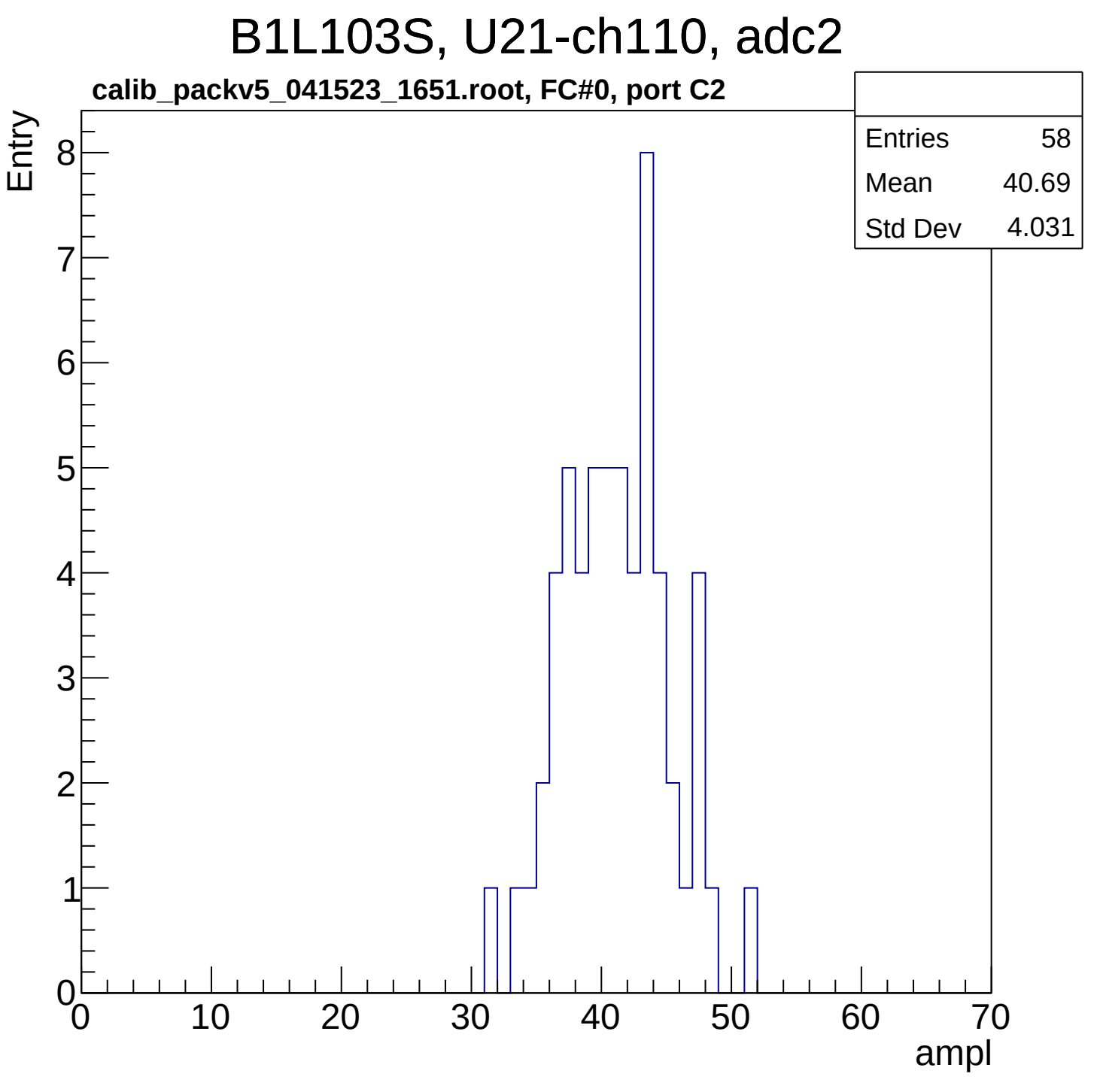
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U21-ch109, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.545
Std Dev 21.51
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch110, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 110
Mean 20.57
Std Dev 11.72
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch110, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 34.16
Std Dev 3.924
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch110, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 40.69
Std Dev 4.031
Entry
ampl
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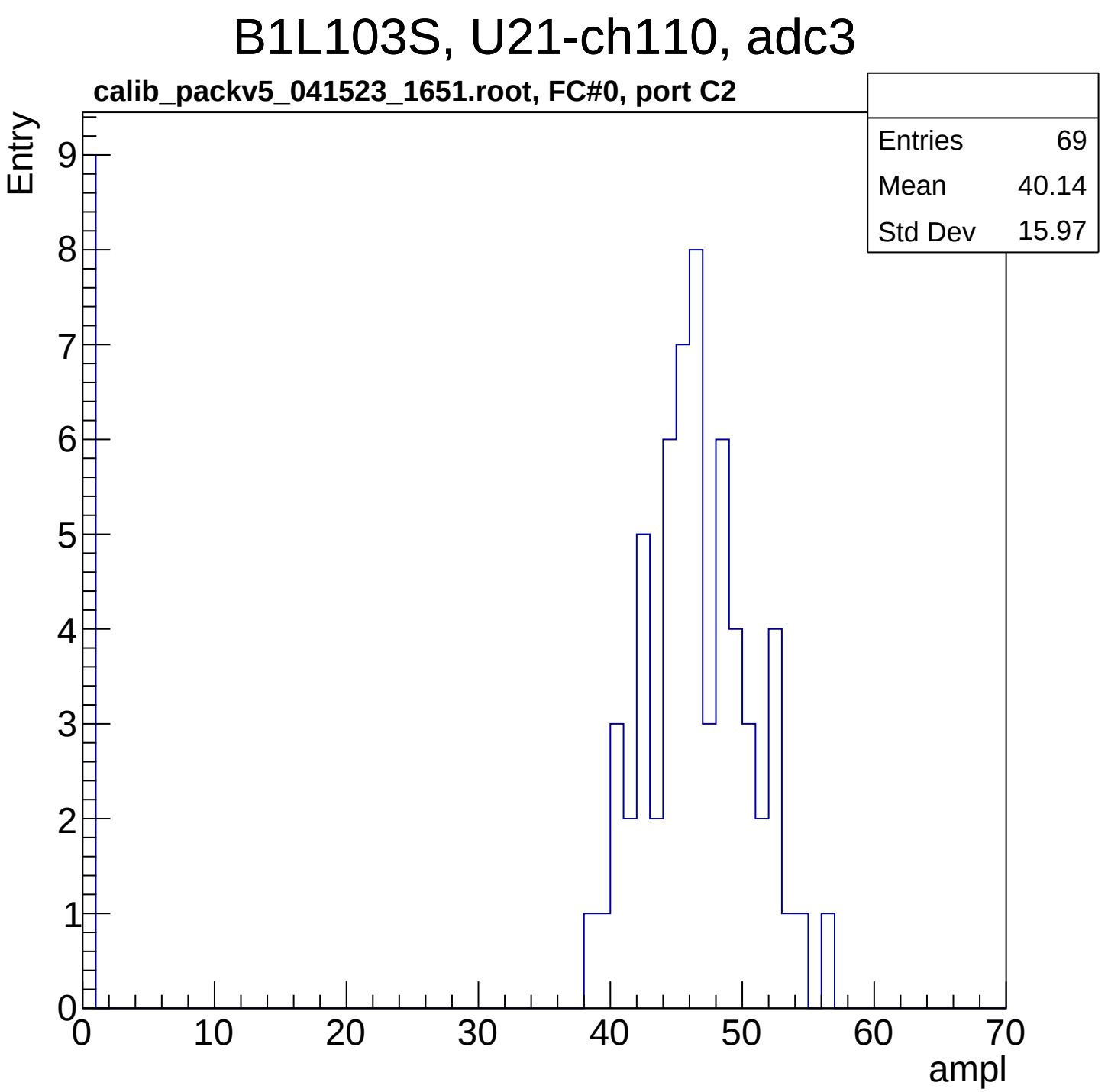
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch110, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 40.14
Std Dev 15.97
Entry
ampl
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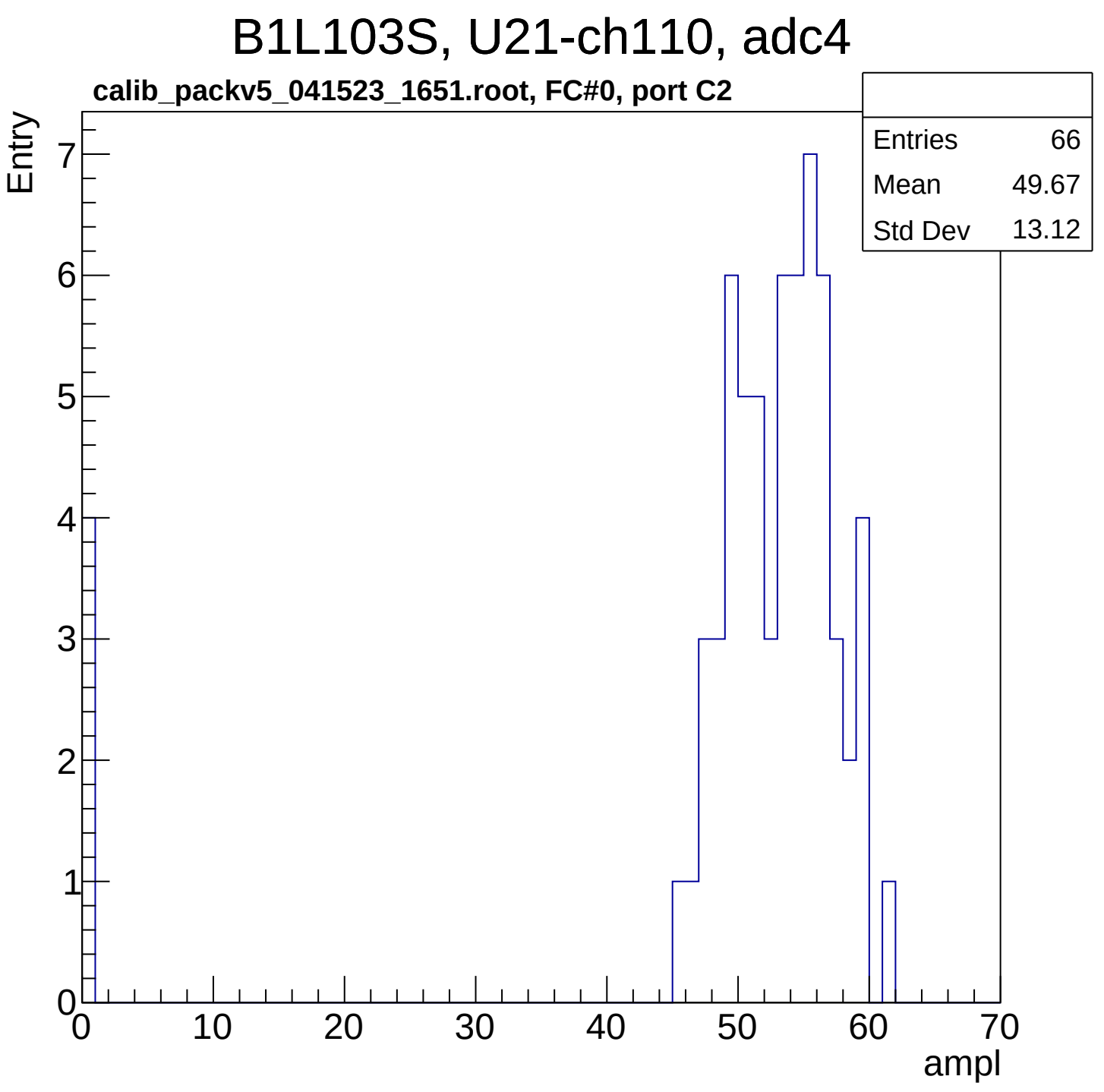
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch110, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 49.67
Std Dev 13.12
Entry
ampl
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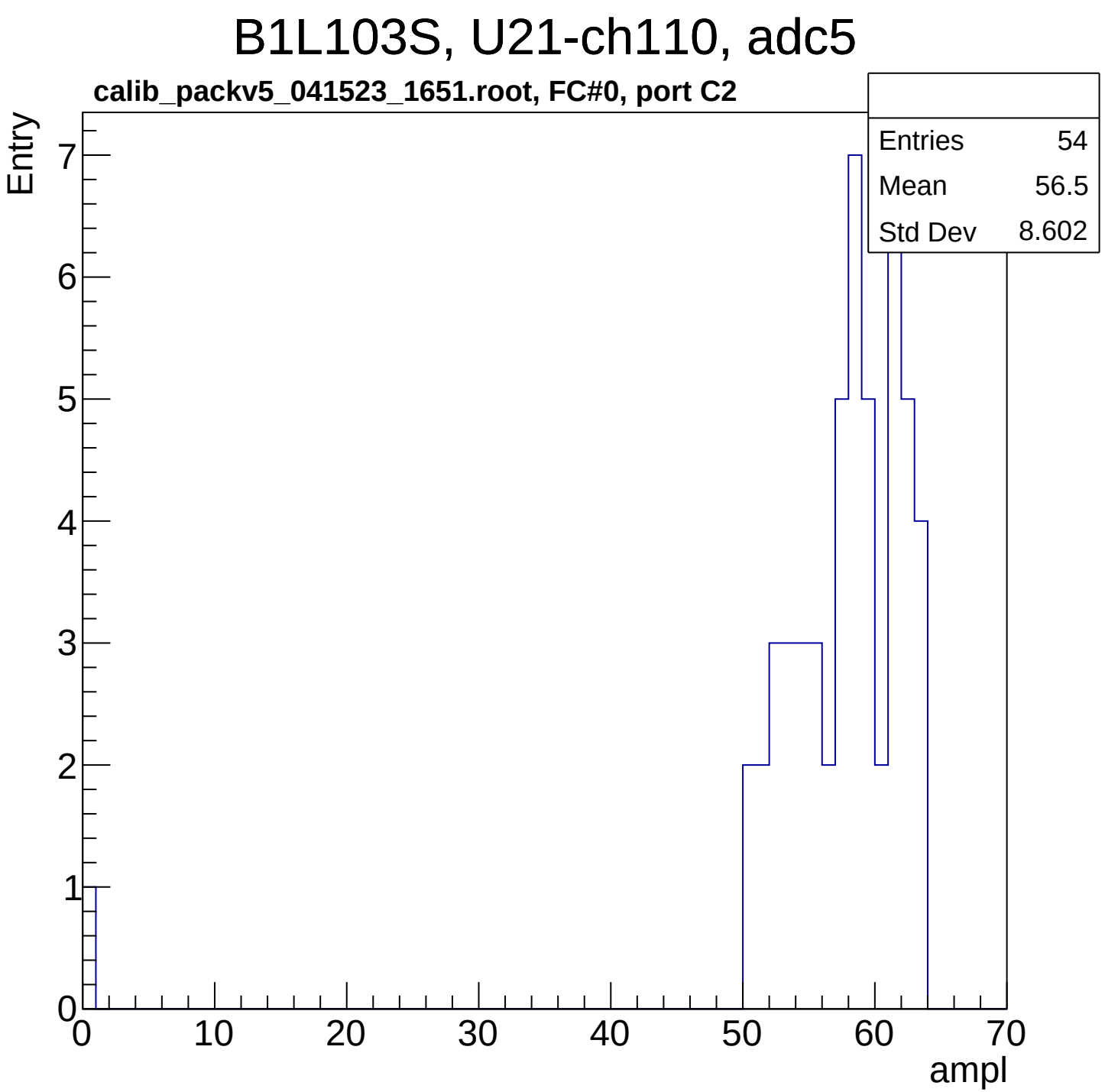
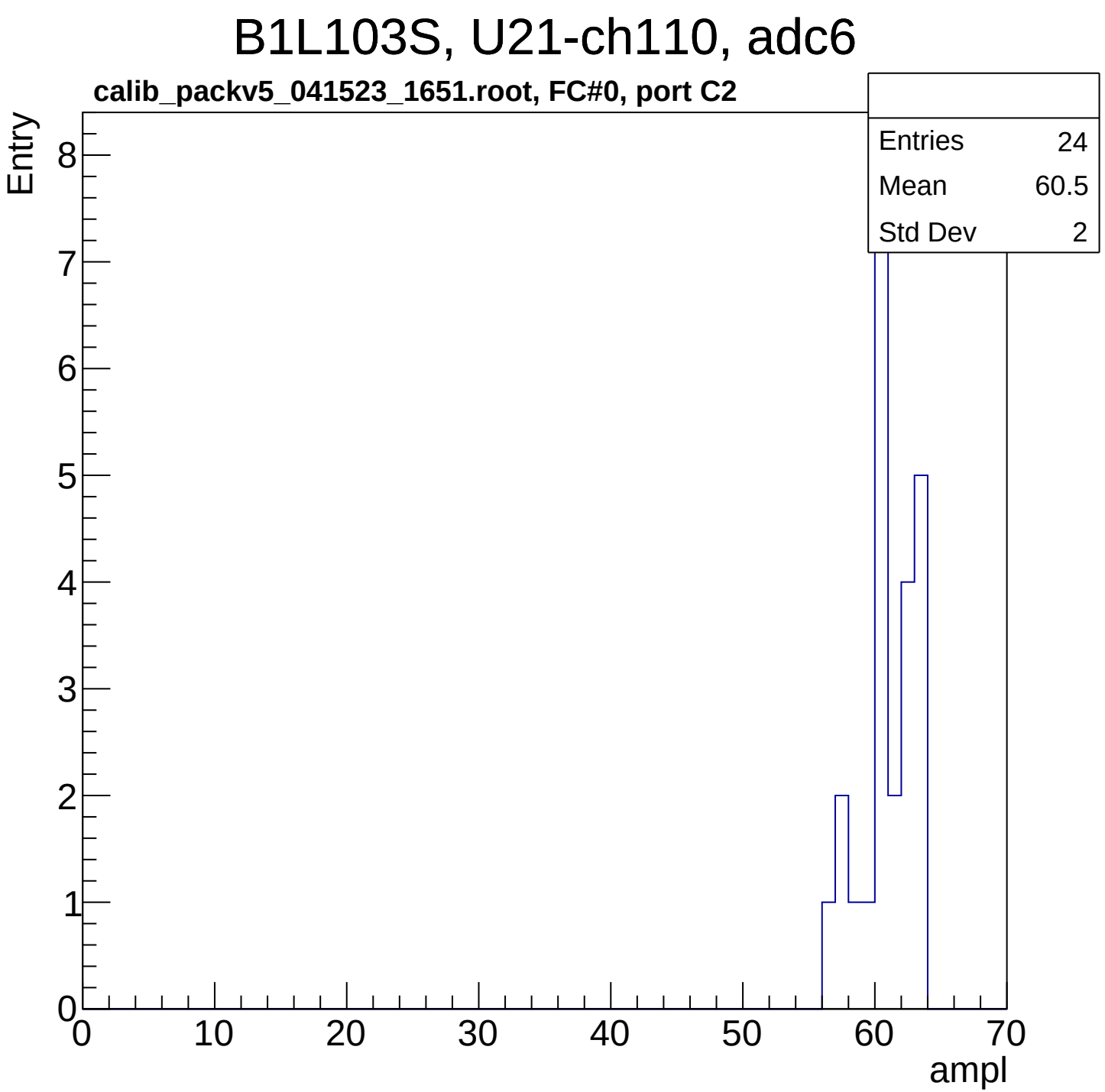
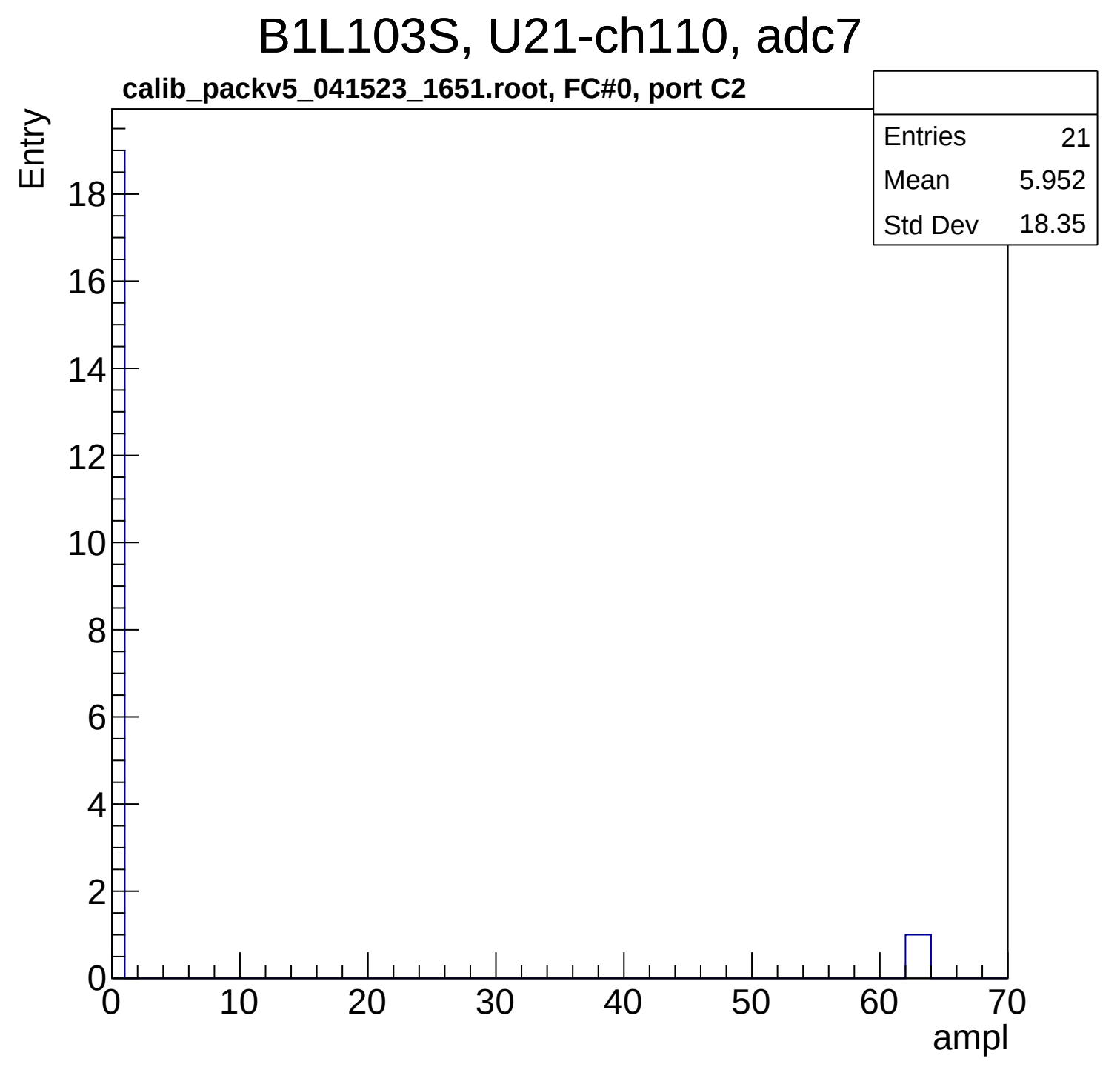
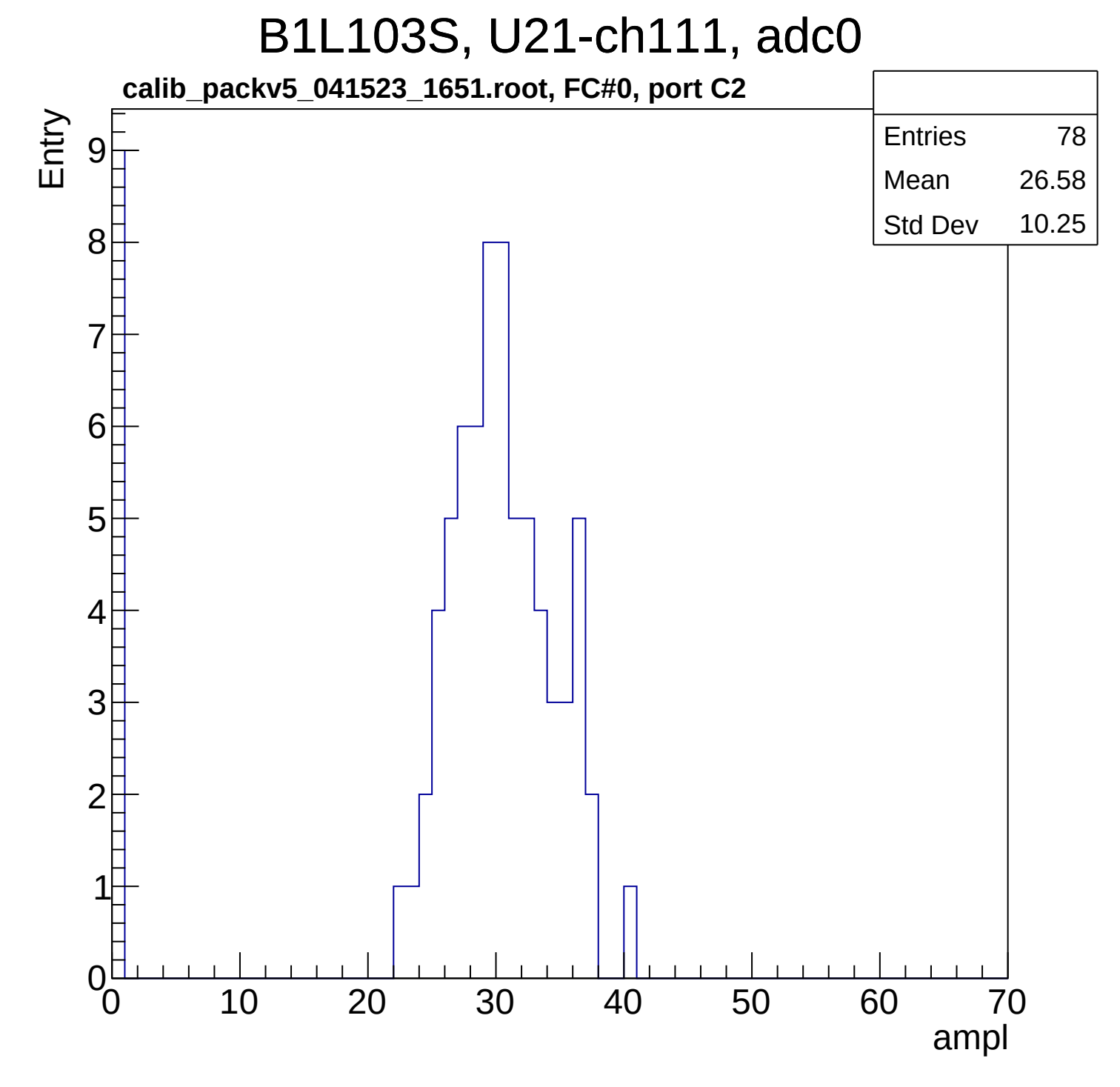
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U21-ch110, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 56.5
Std Dev 8.602
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U21-ch110, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 60.5
Std Dev 2
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch110, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.952
Std Dev 18.35
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch111, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 26.58
Std Dev 10.25
Entry
ampl
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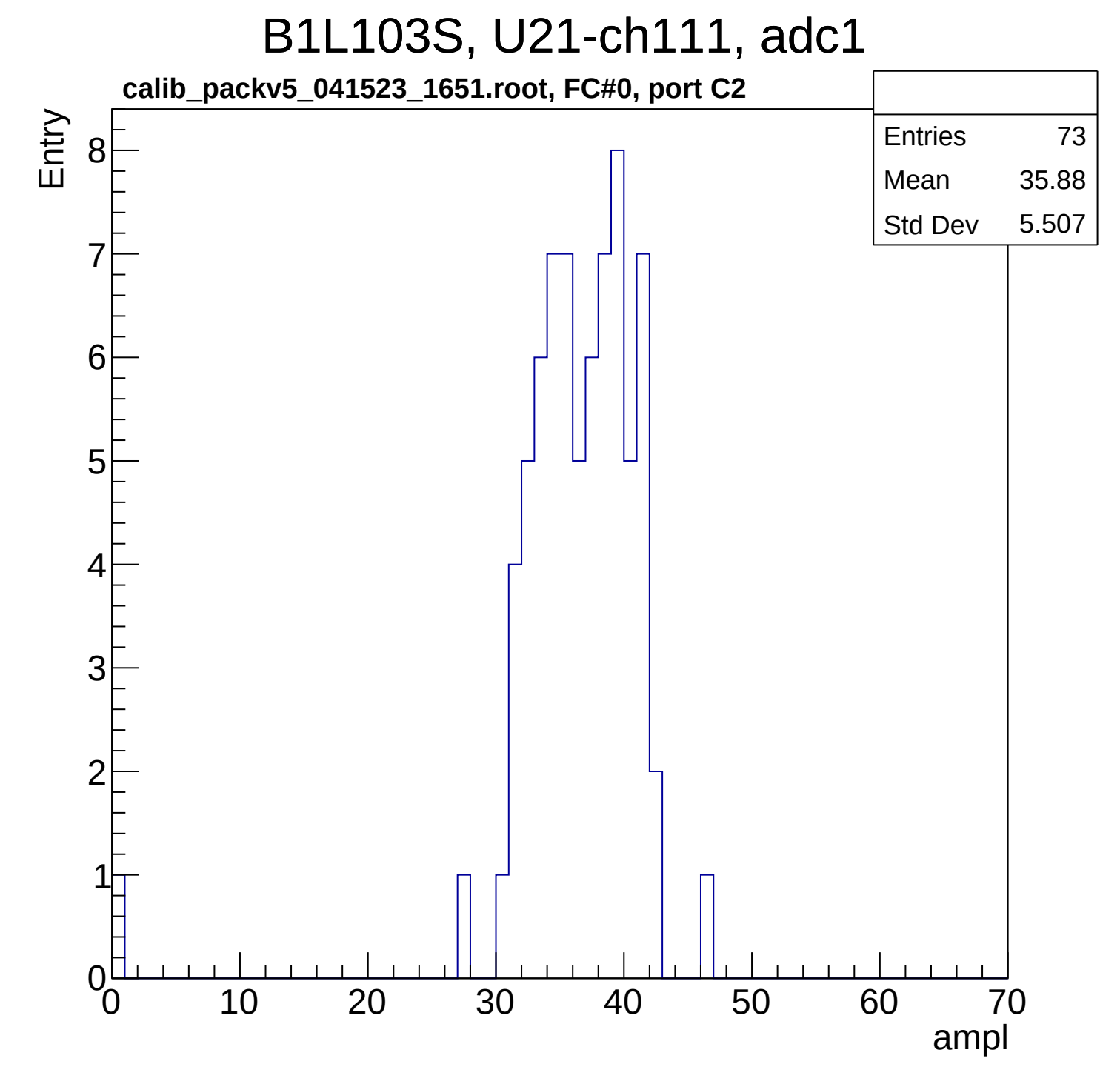
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch111, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 35.88
Std Dev 5.507
Entry
ampl
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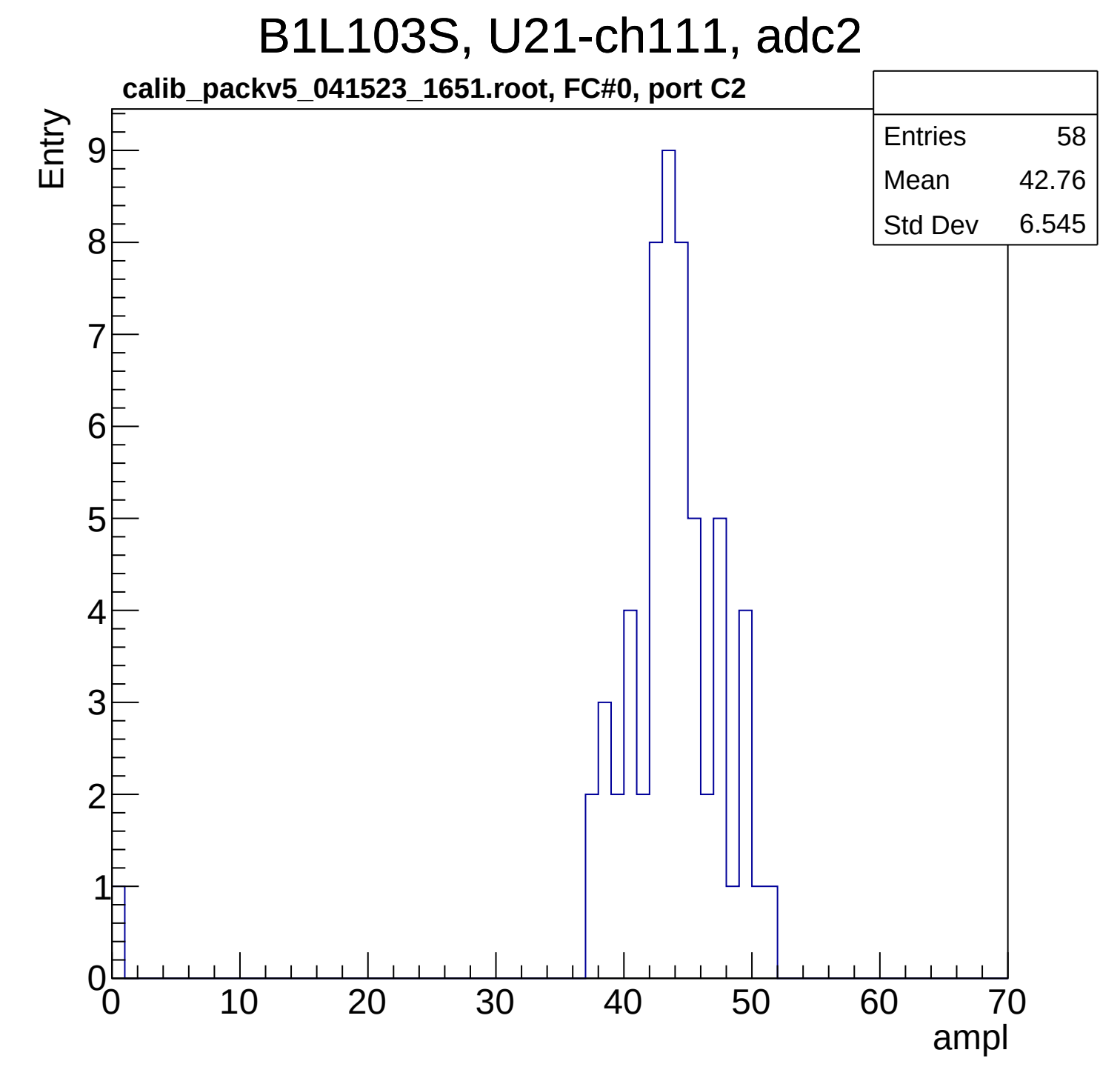
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch111, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 42.76
Std Dev 6.545
Entry
ampl
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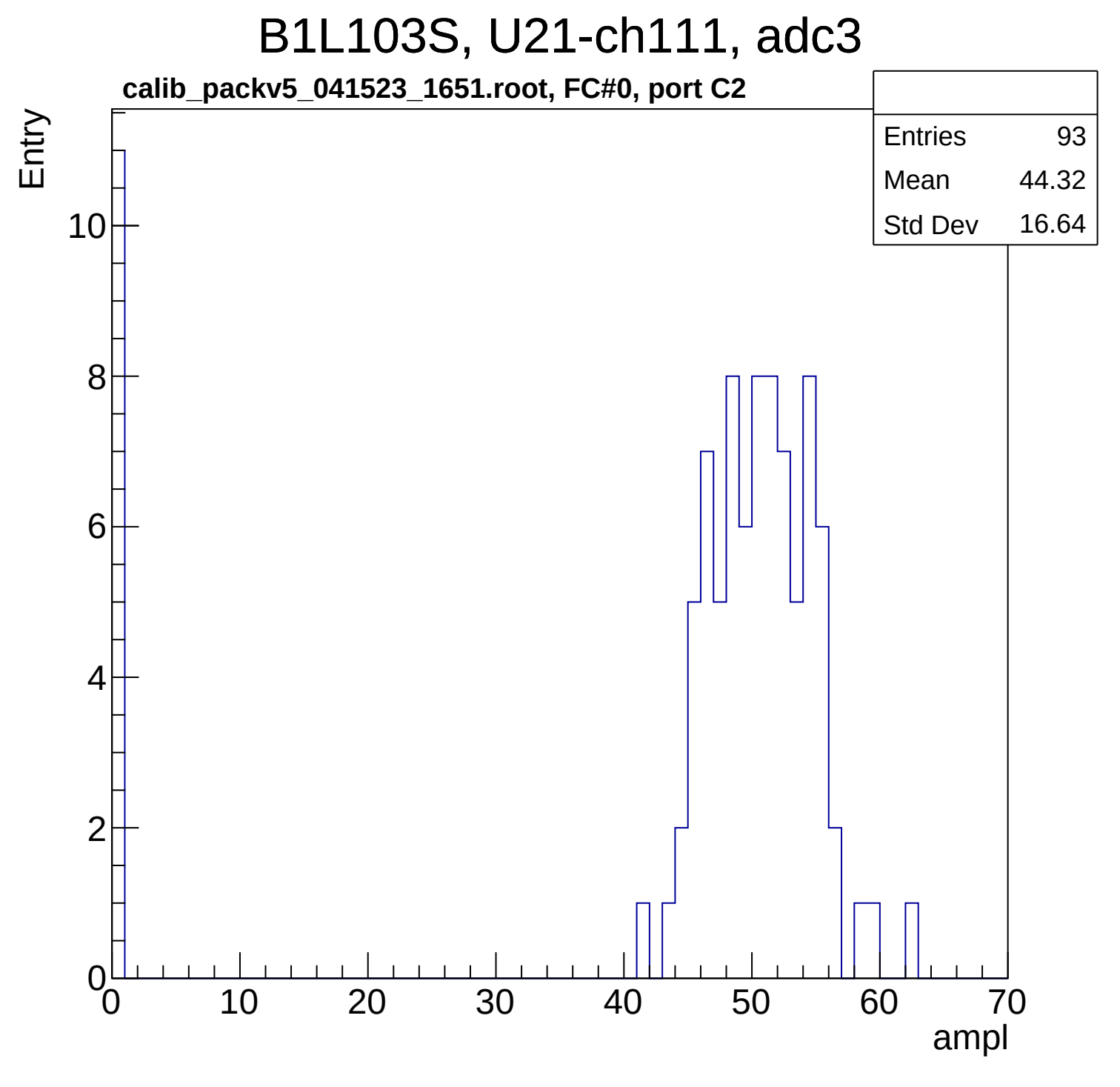
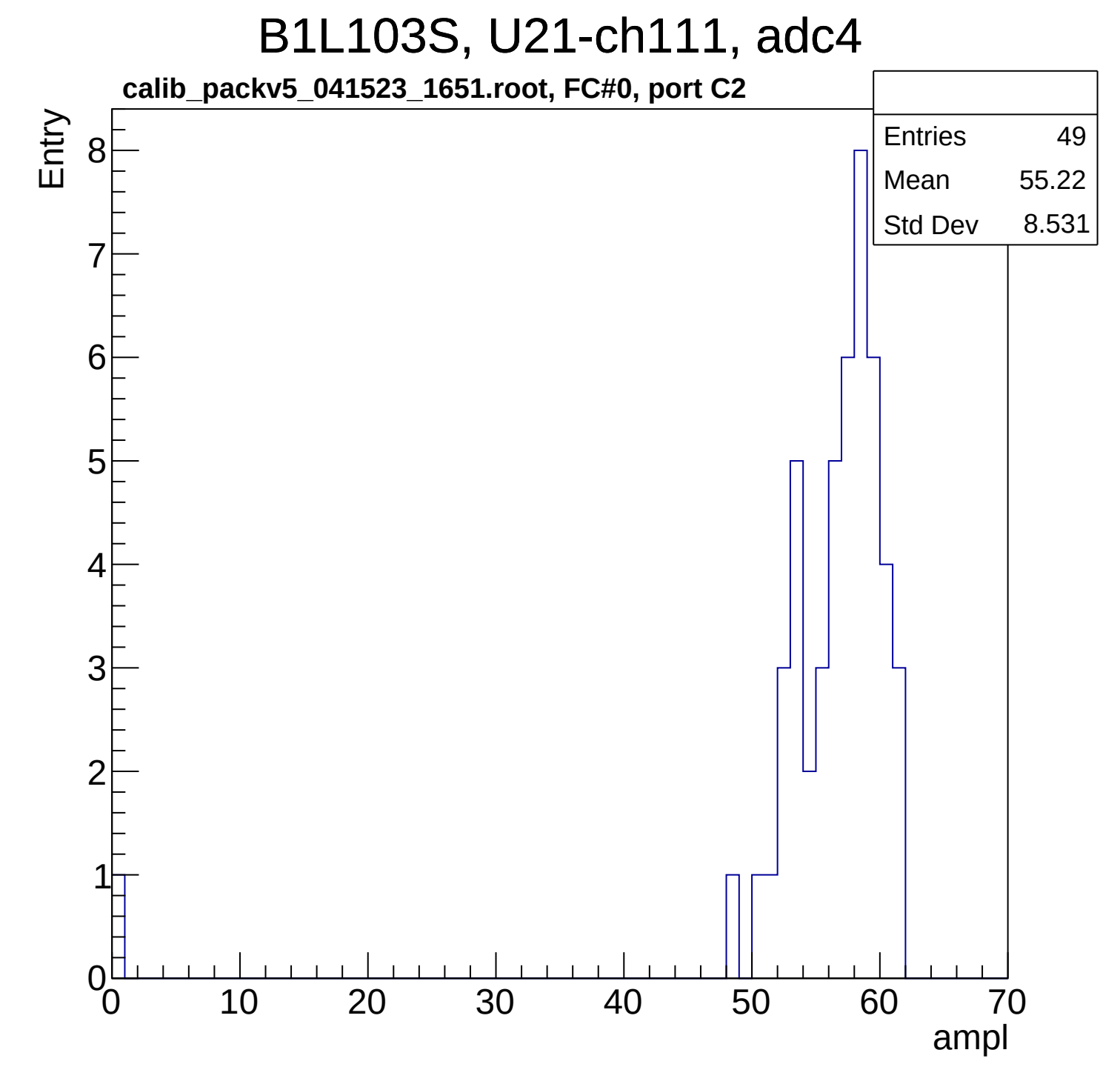
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch111, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 44.32
Std Dev 16.64
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U21-ch111, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 55.22
Std Dev 8.531
Entry
ampl
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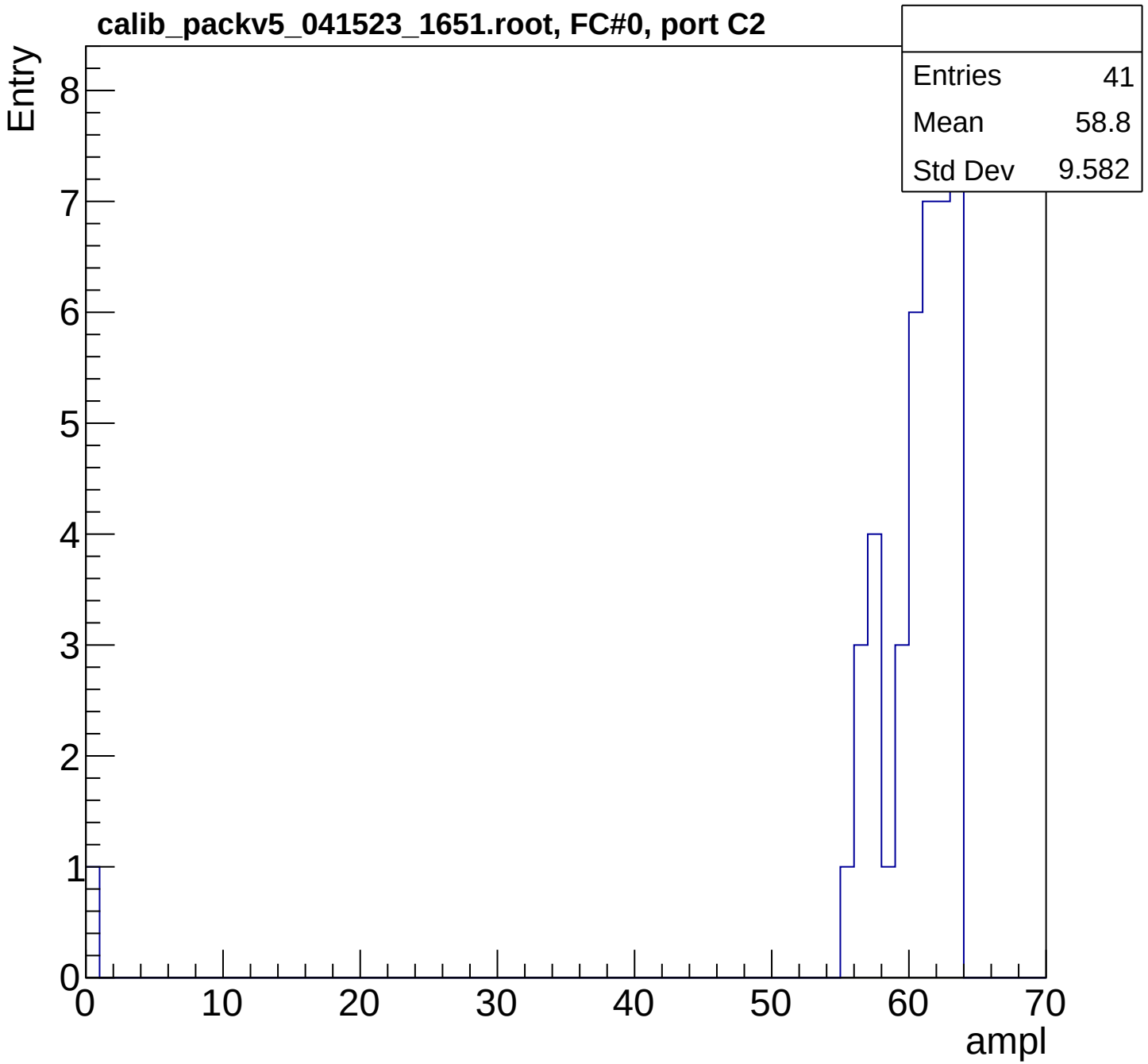
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch111, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 58.8
Std Dev 9.582
Entry
ampl
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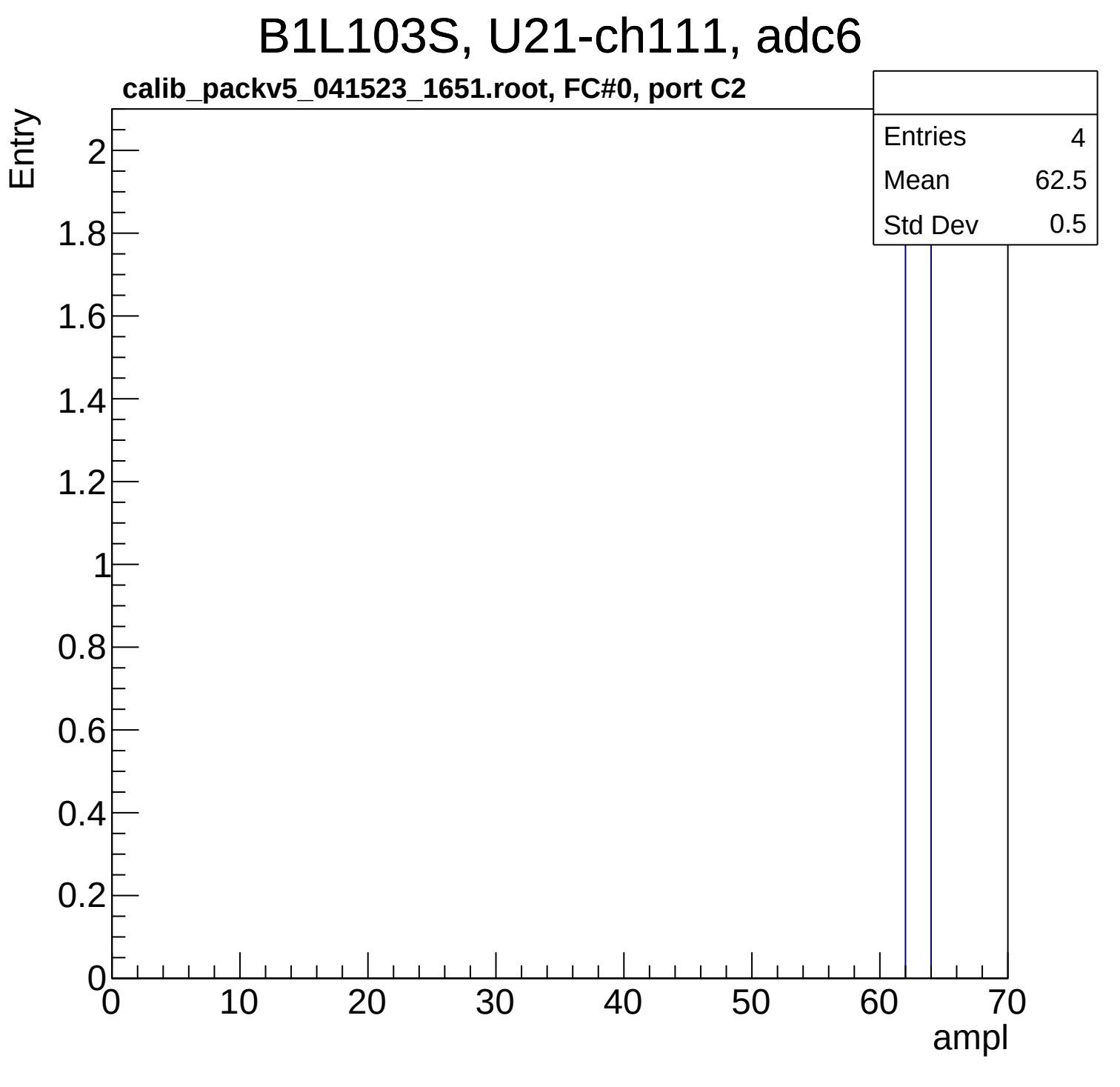
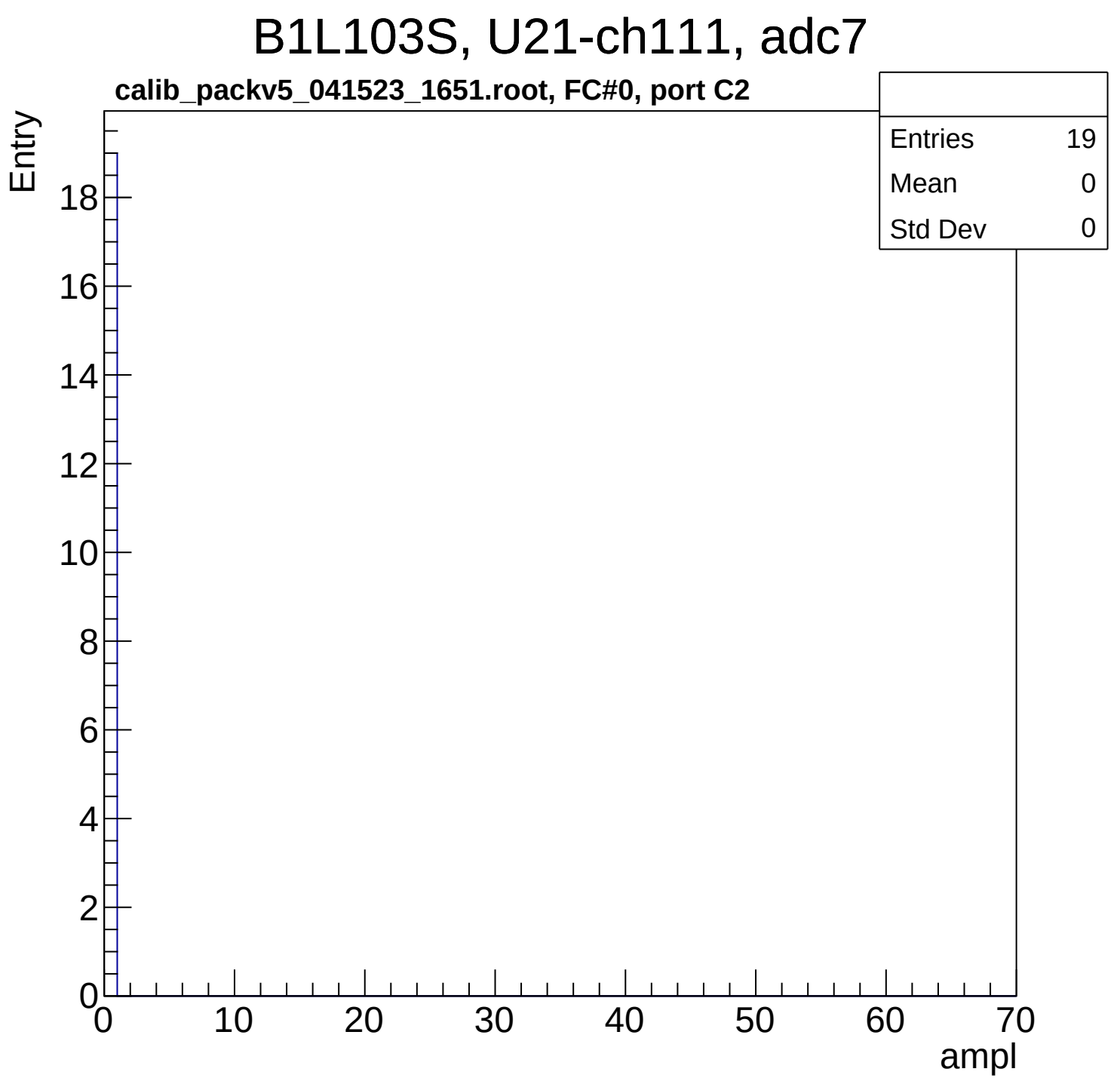
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch111, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 62.5
Std Dev 0.5
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U21-ch111, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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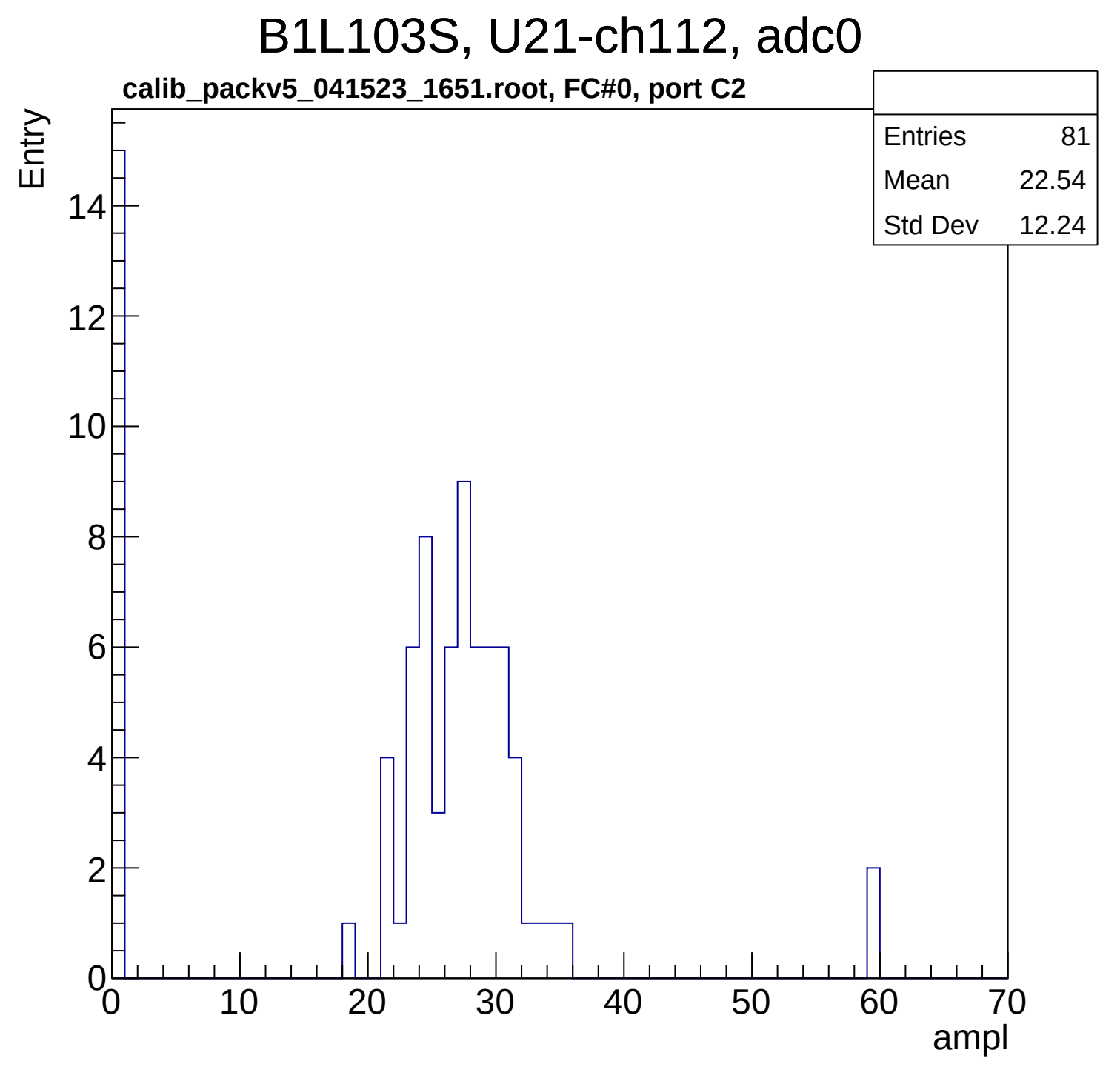
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch112, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 22.54
Std Dev 12.24
Entry
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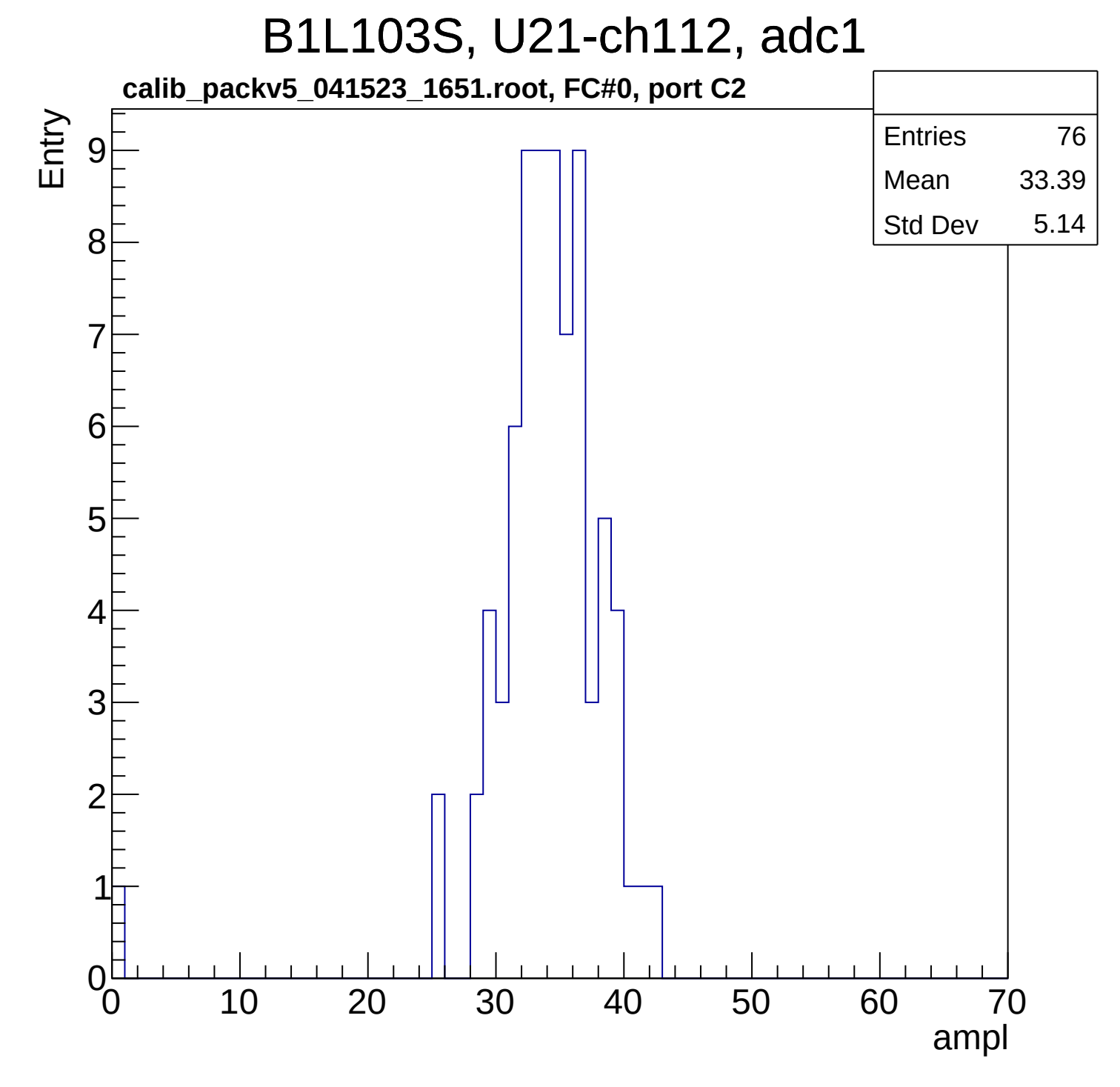
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch112, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 33.39
Std Dev 5.14
Entry
ampl
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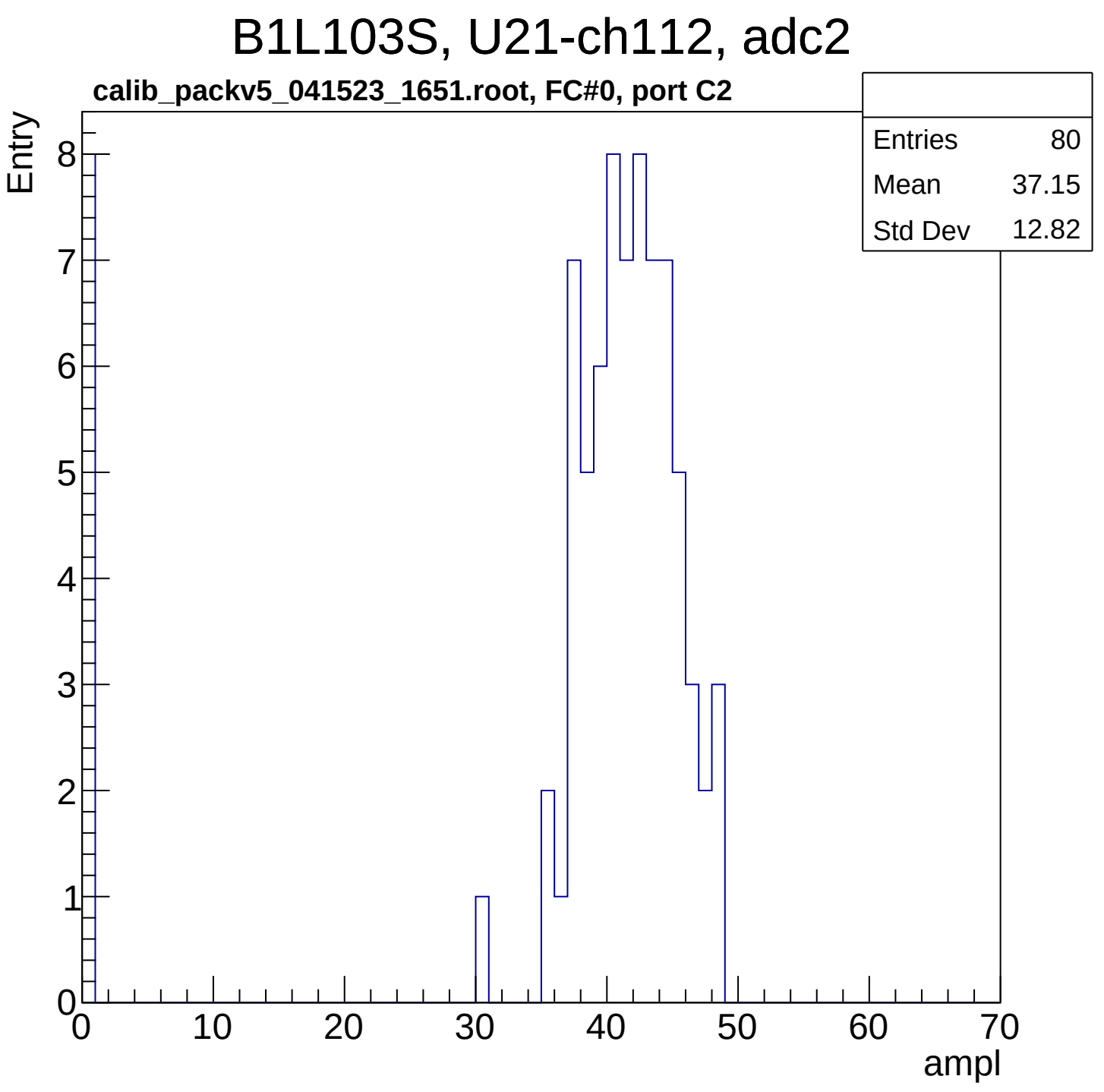
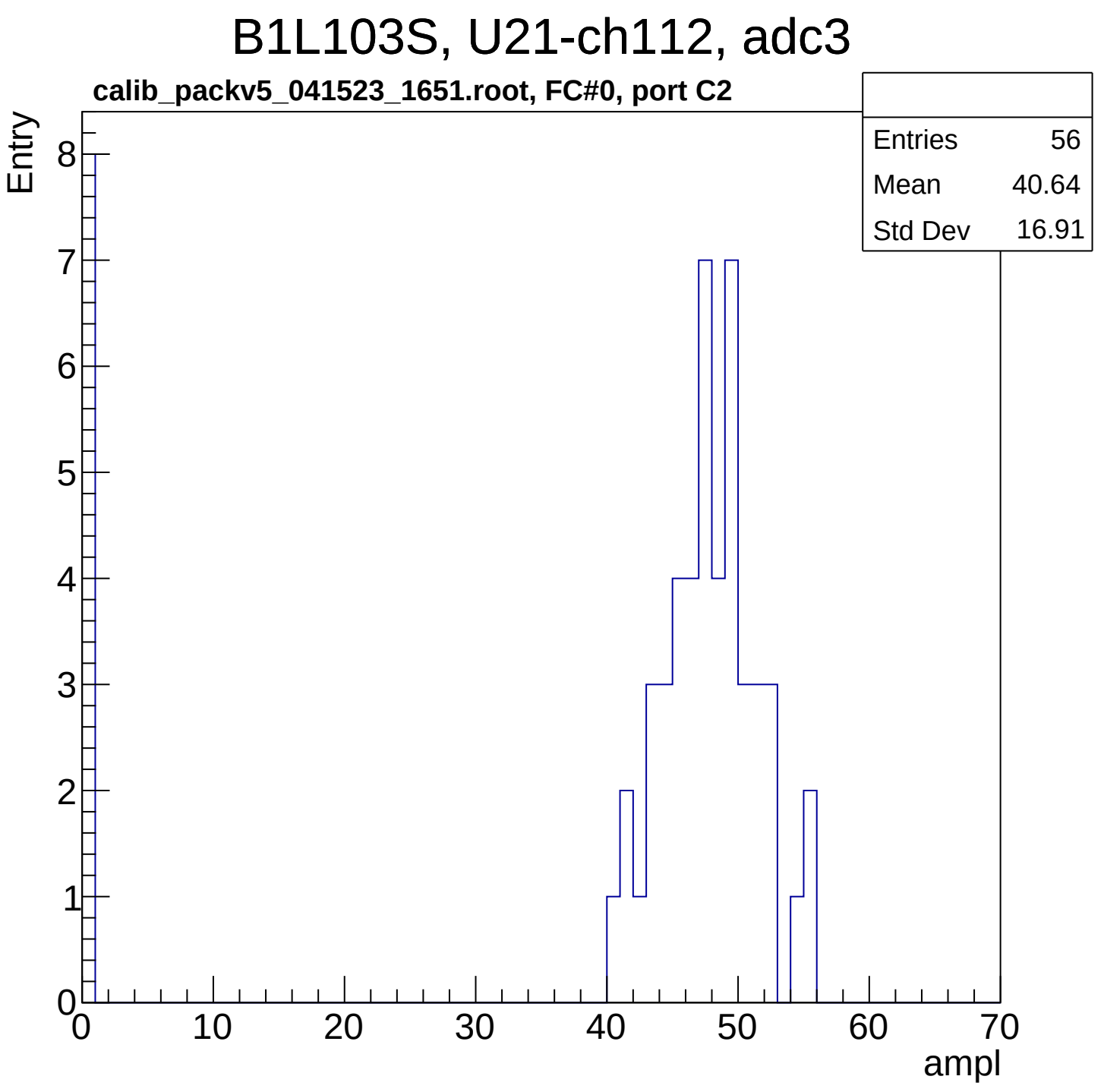
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch112, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 37.15
Std Dev 12.82
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch112, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 40.64
Std Dev 16.91
Entry
ampl
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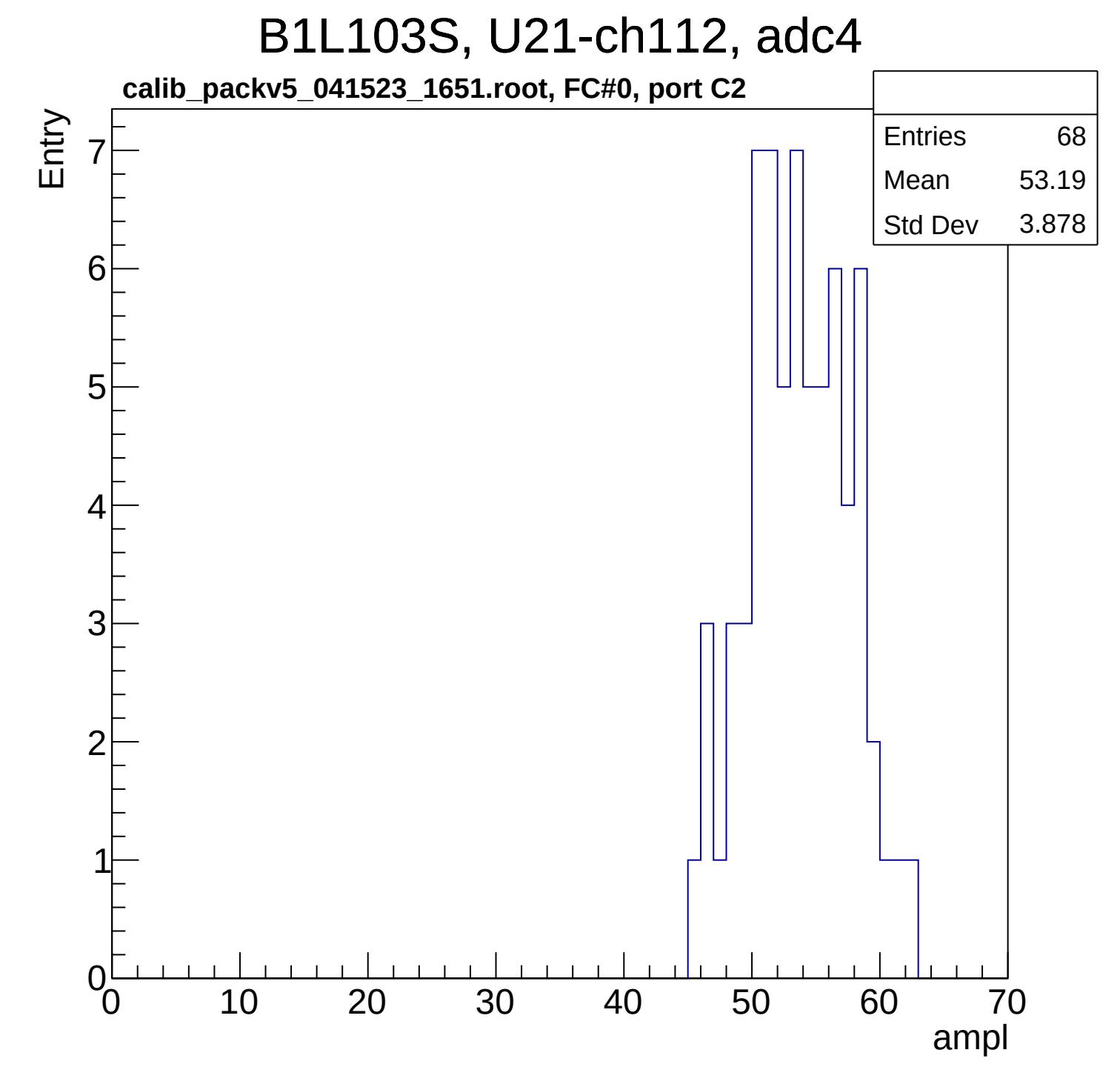
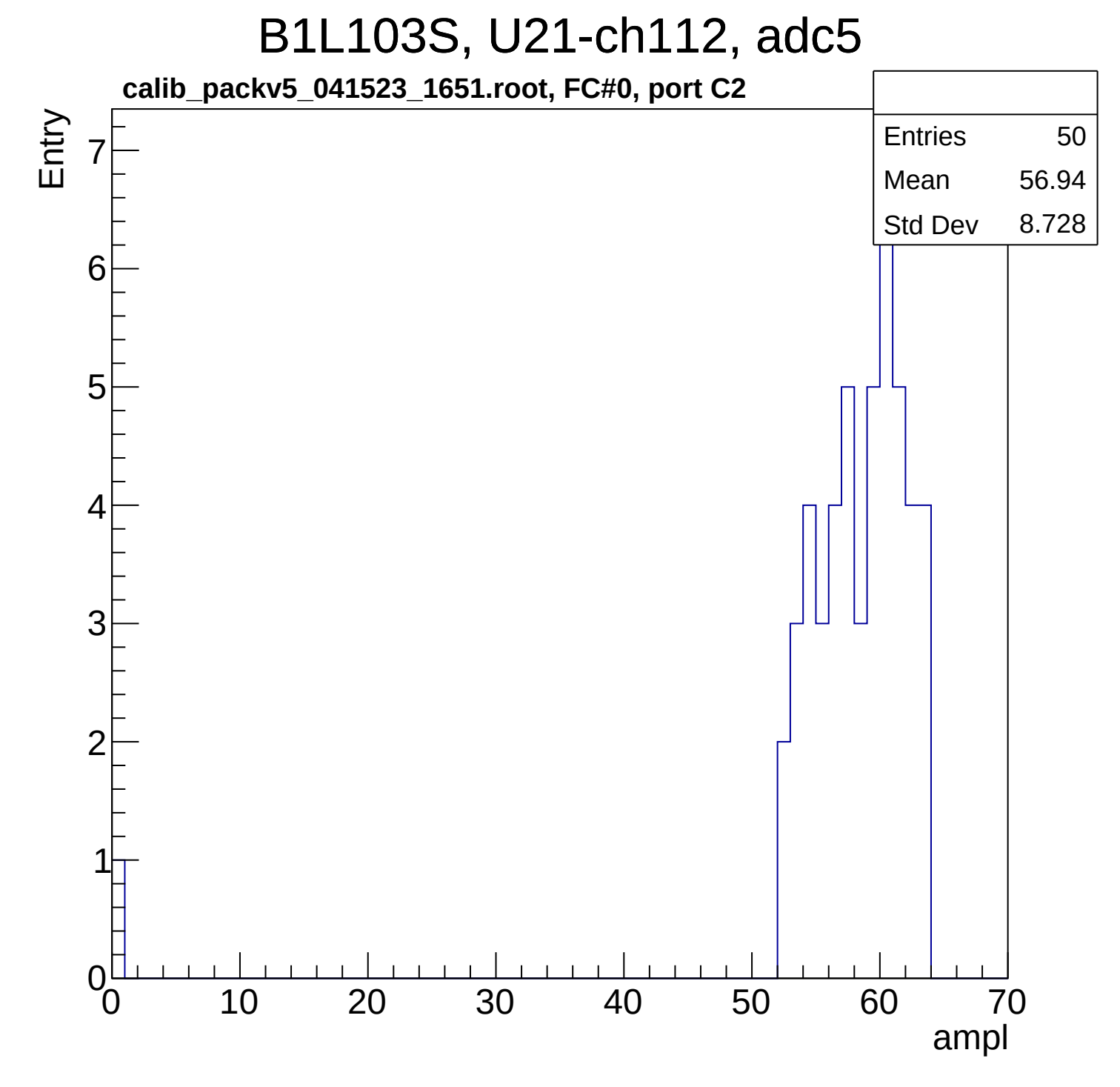
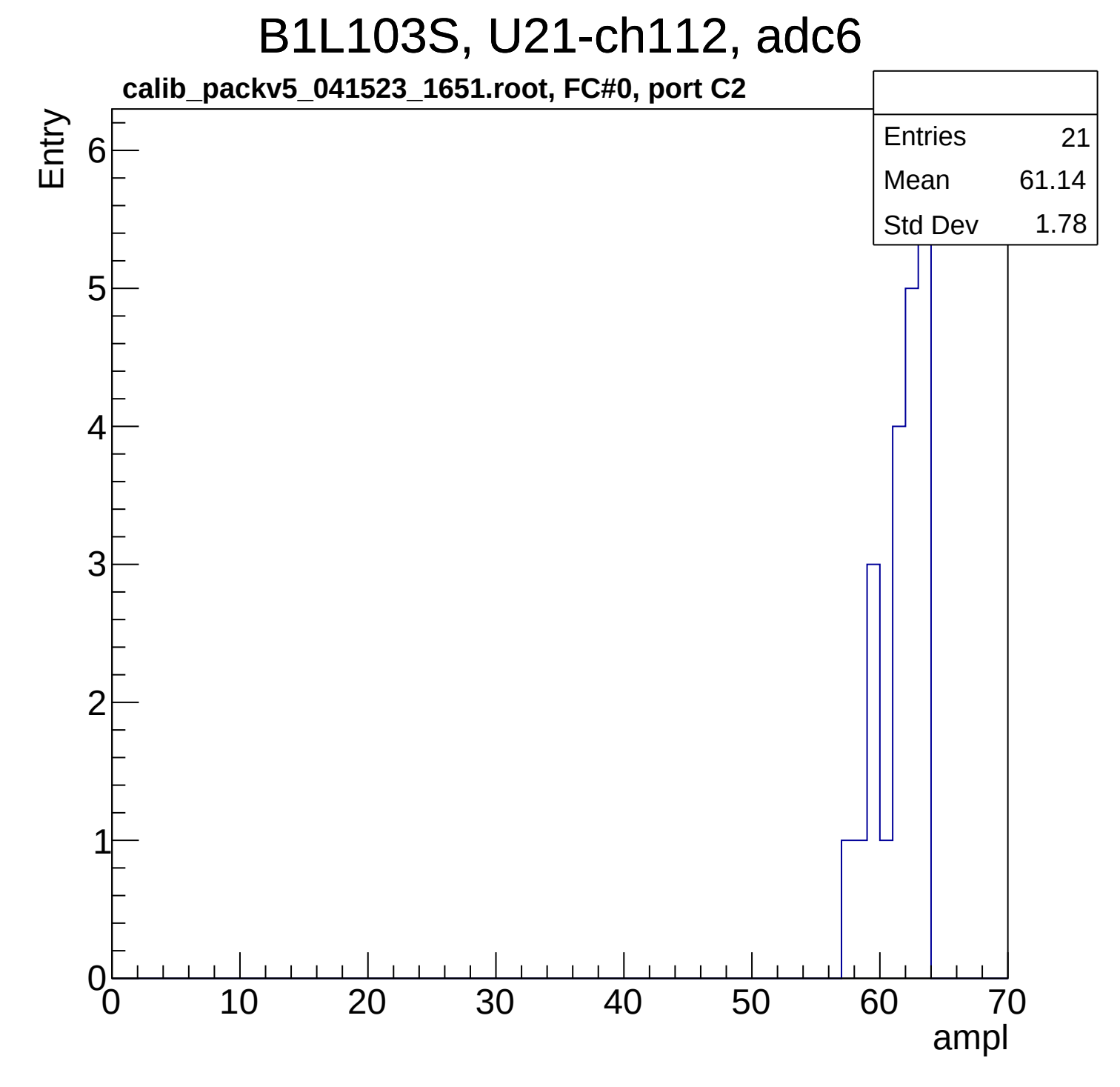
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch112, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 53.19
Std Dev 3.878
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U21-ch112, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 56.94
Std Dev 8.728
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U21-ch112, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 61.14
Std Dev 1.78
Entry
ampl
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3
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0
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40
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60
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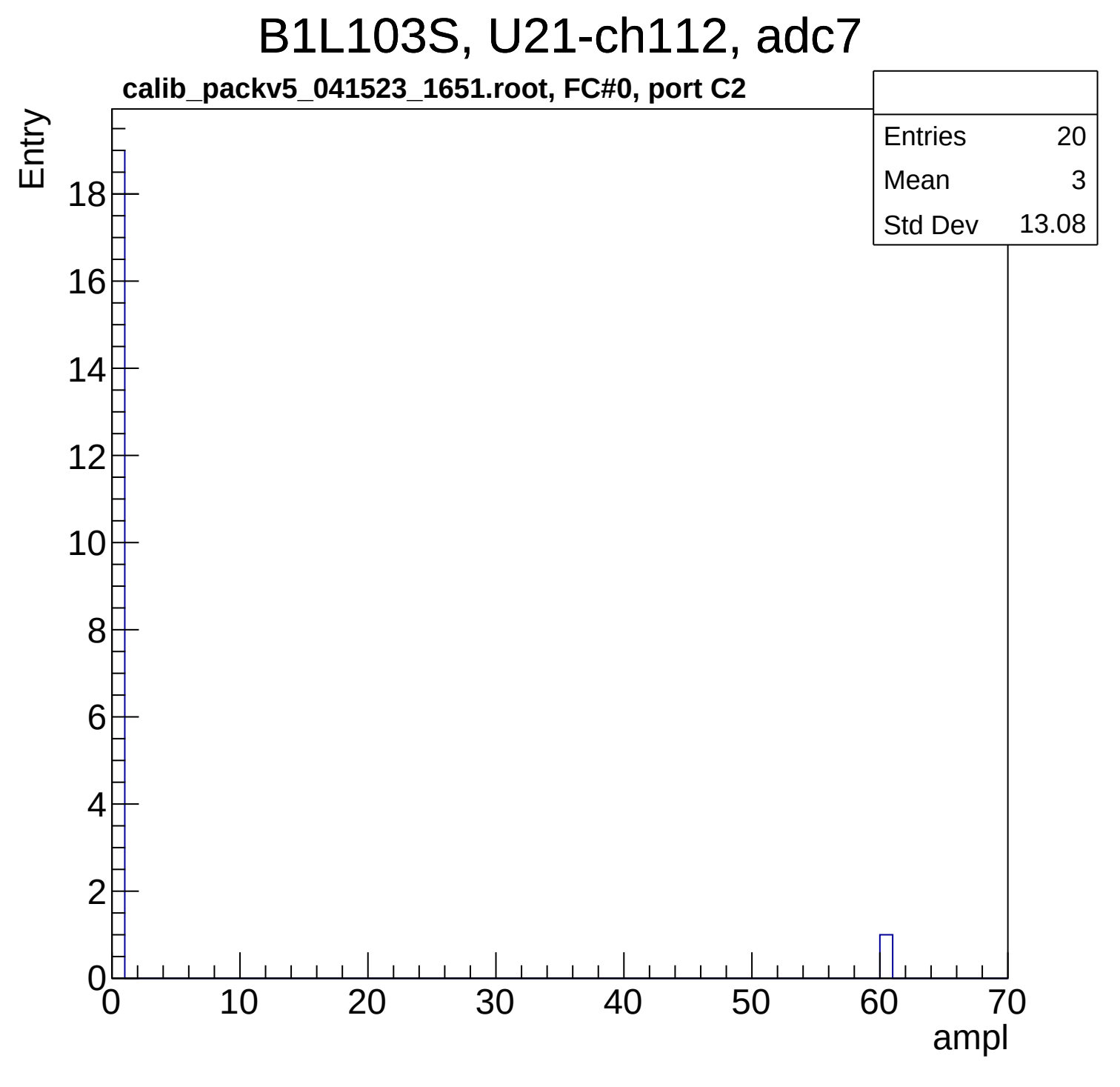
B1L103S, U21-ch112, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3
Std Dev 13.08
Entry
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14
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18
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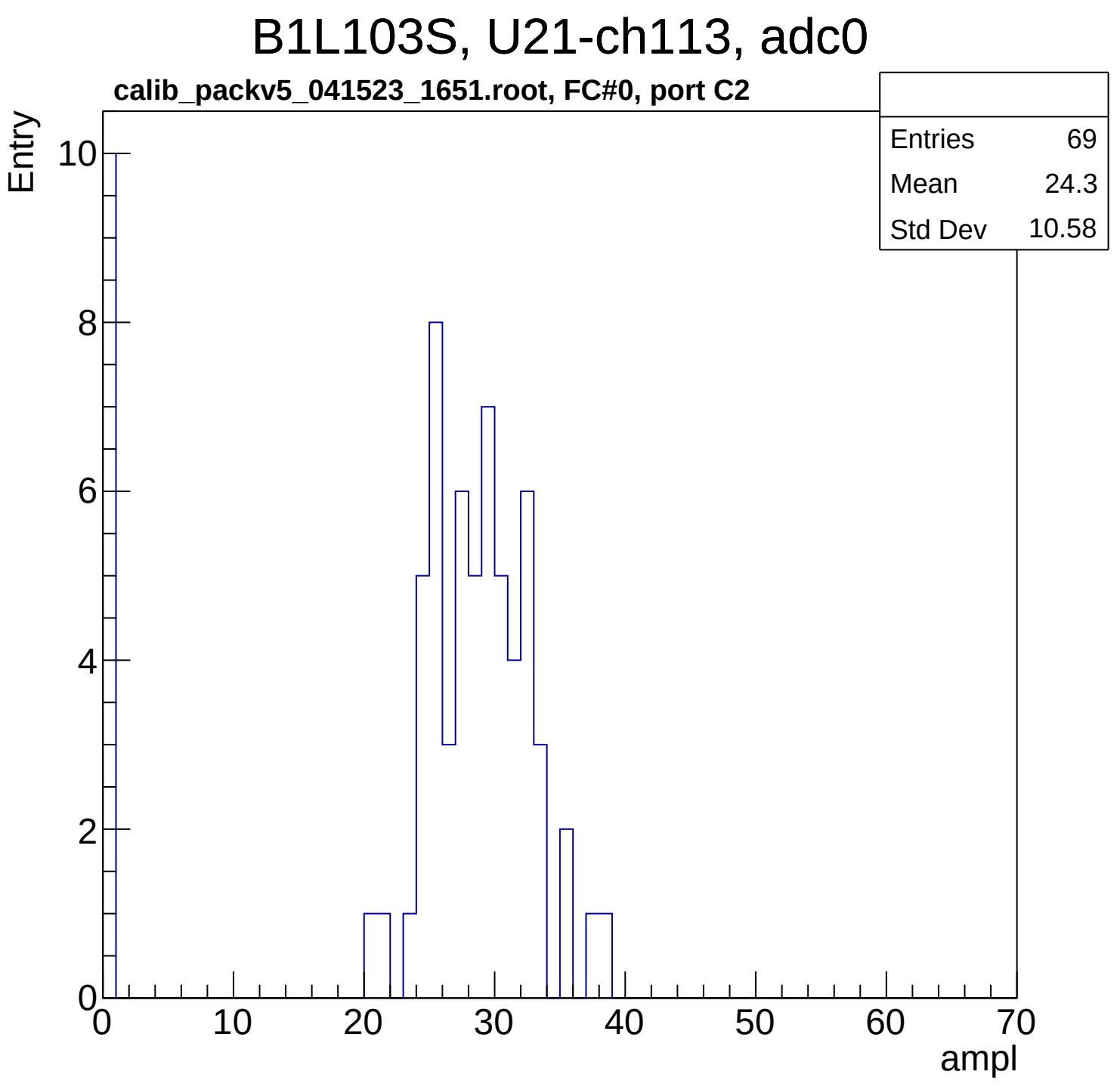
ampl


B1L103S, U21-ch113, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 24.3
Std Dev 10.58
Entry
0
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10
0
10
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50
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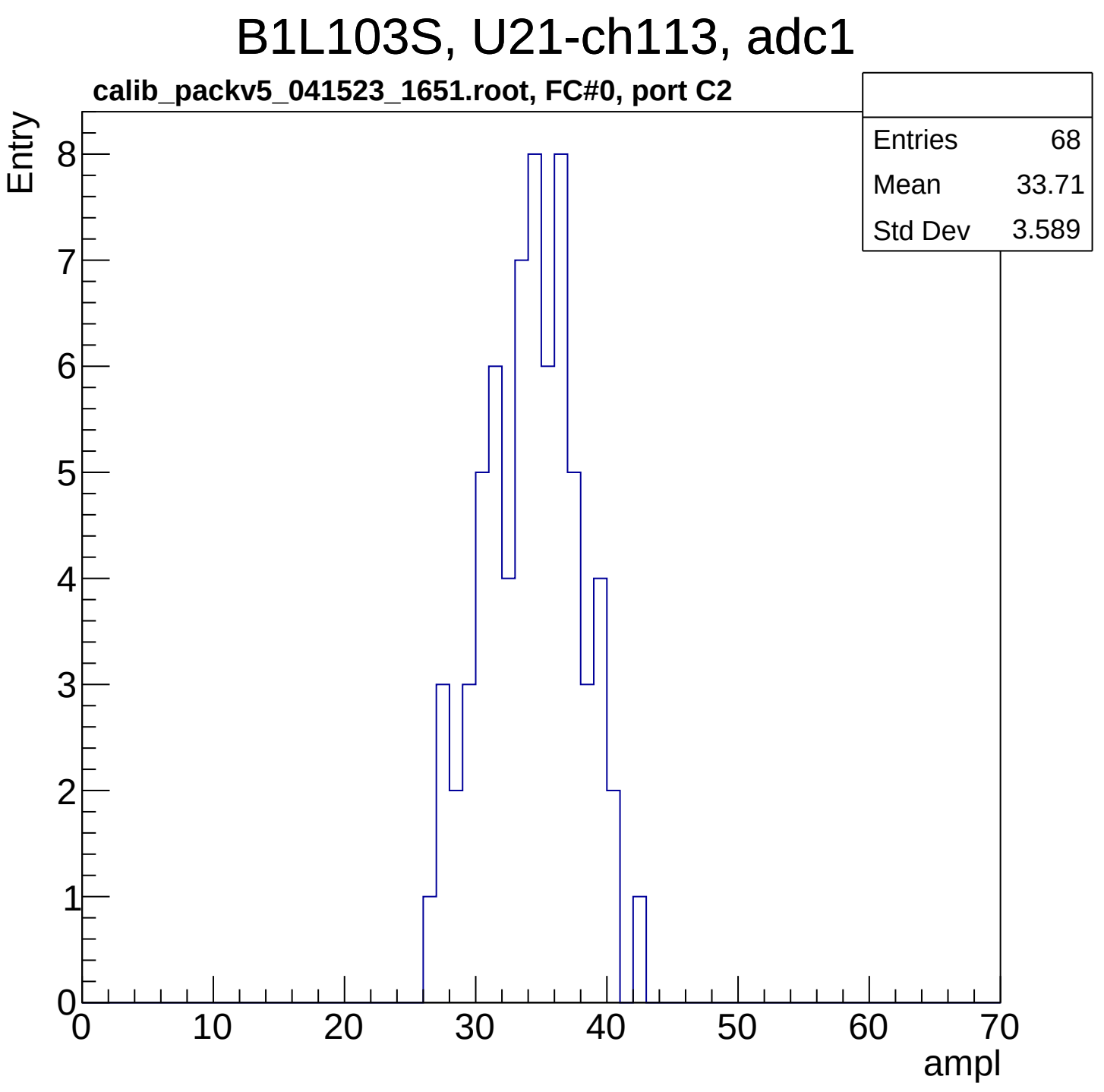
70
ampl


B1L103S, U21-ch113, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 33.71
Std Dev 3.589
Entry
ampl
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7
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0
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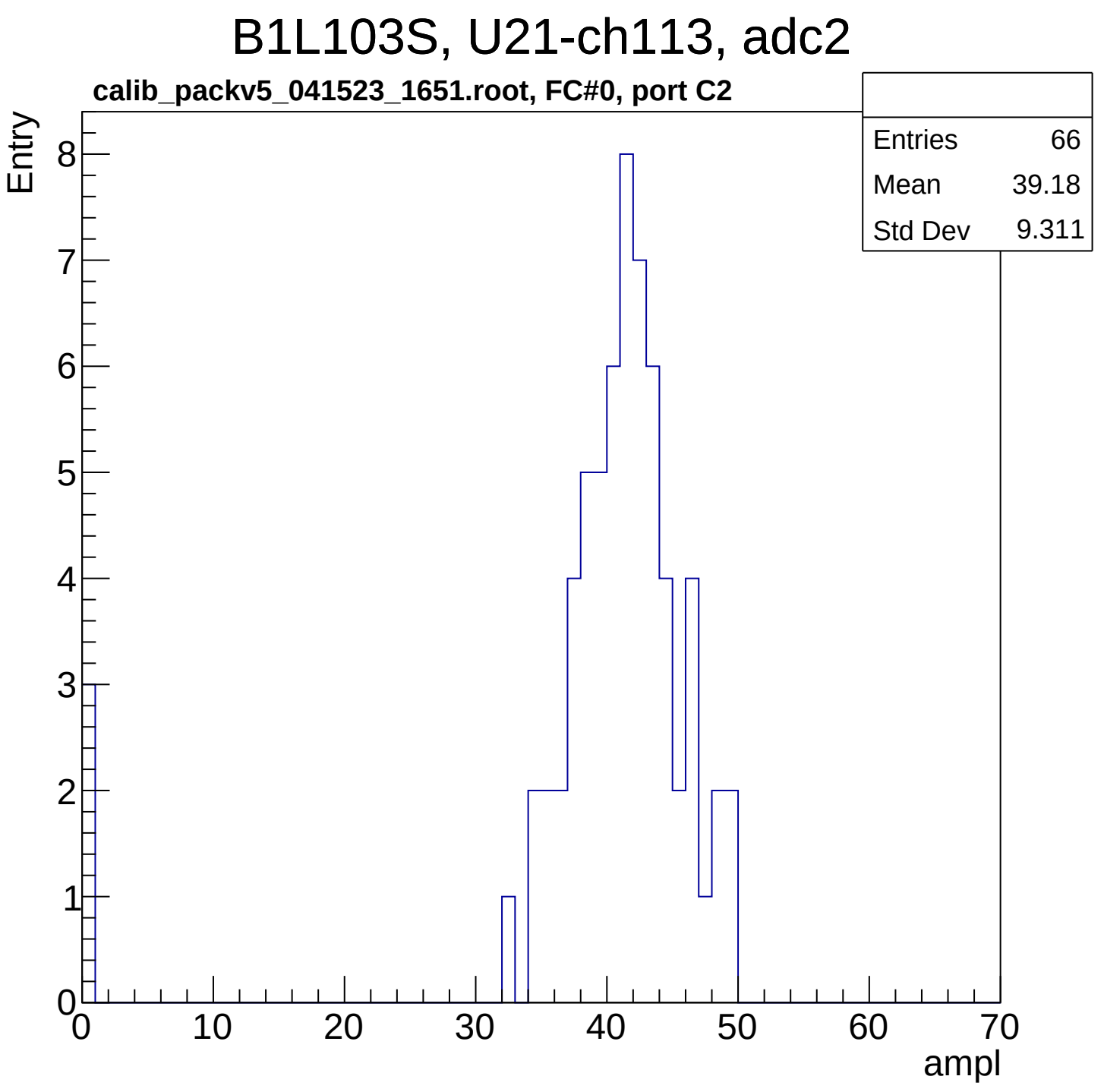
B1L103S, U21-ch113, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 39.18
Std Dev 9.311
Entry
ampl
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7
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0
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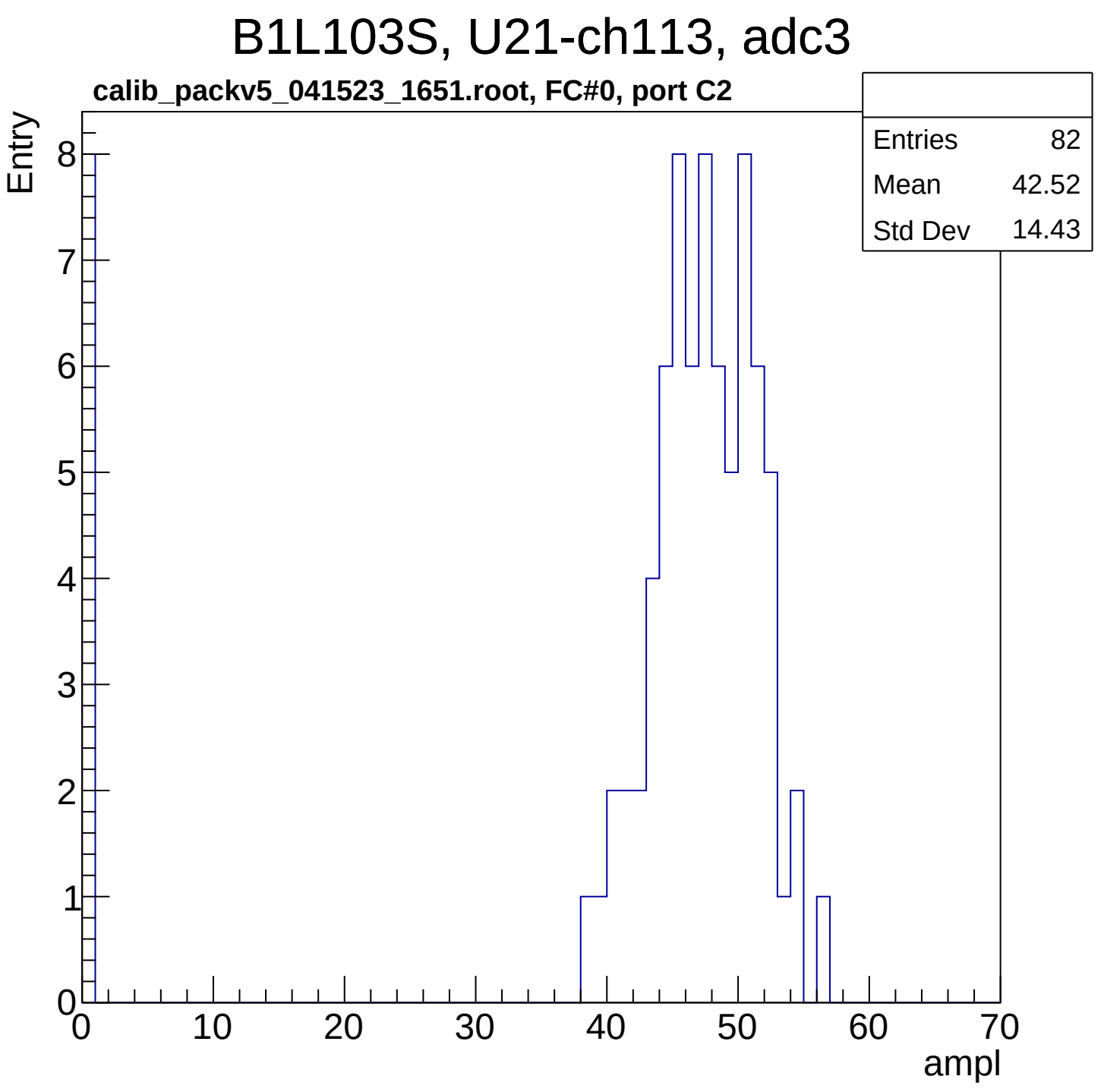
B1L103S, U21-ch113, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 42.52
Std Dev 14.43
Entry
ampl
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2
3
4
5
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7
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0
10
20
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40
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60
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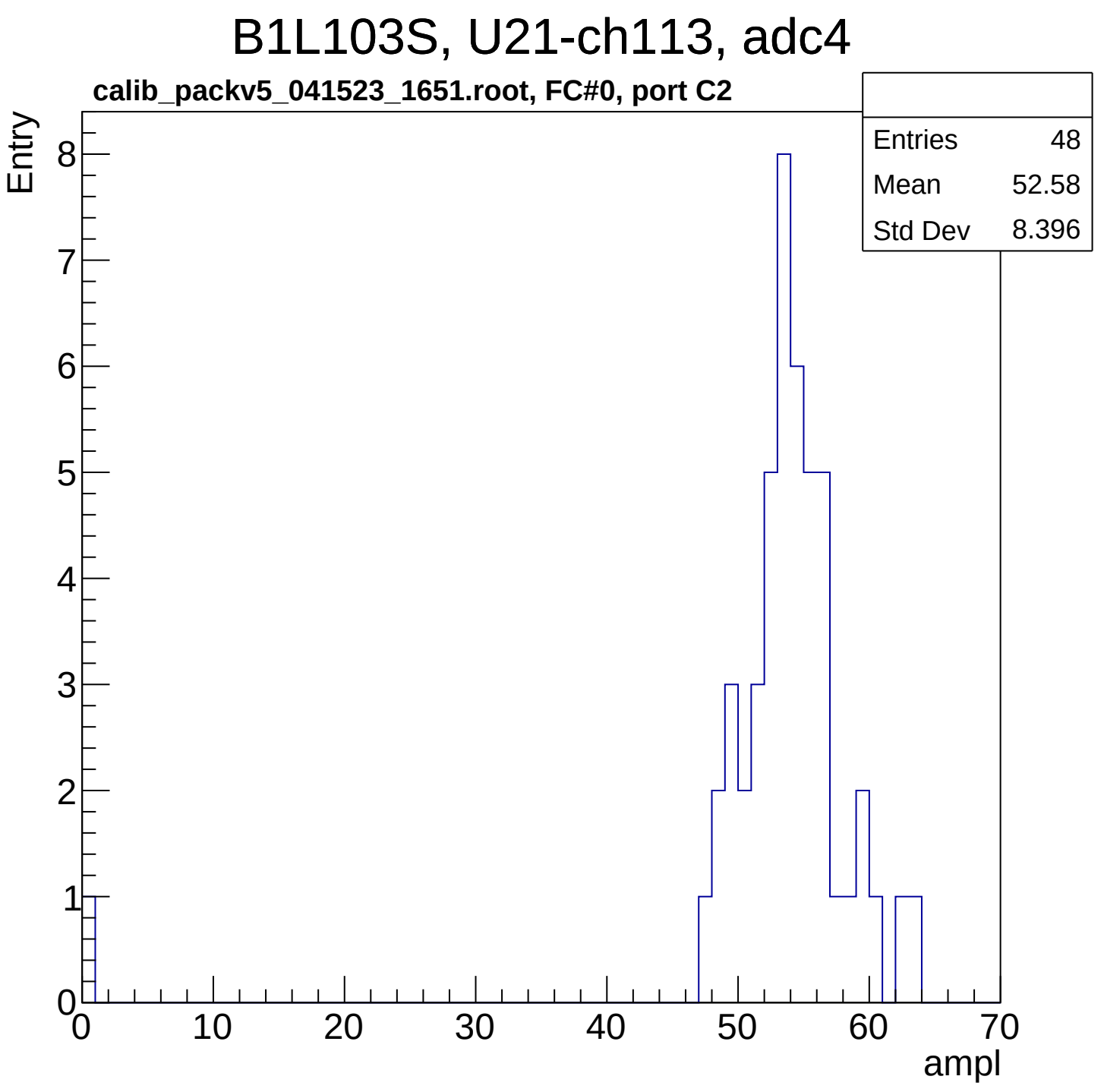
B1L103S, U21-ch113, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 52.58
Std Dev 8.396
Entry
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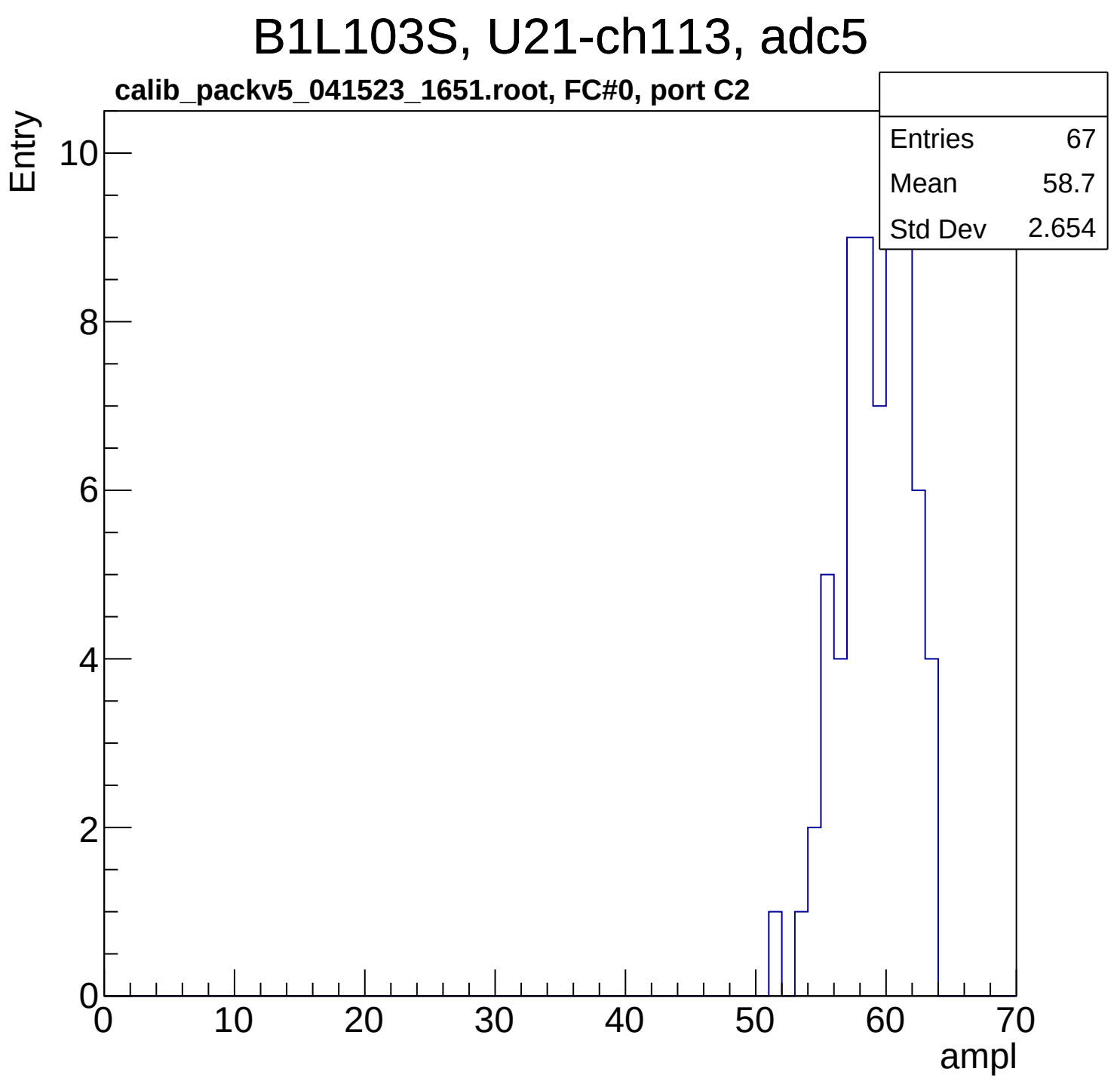
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch113, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 58.7
Std Dev 2.654
Entry
ampl
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2
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8
10
0
10
20
30
40
50
60
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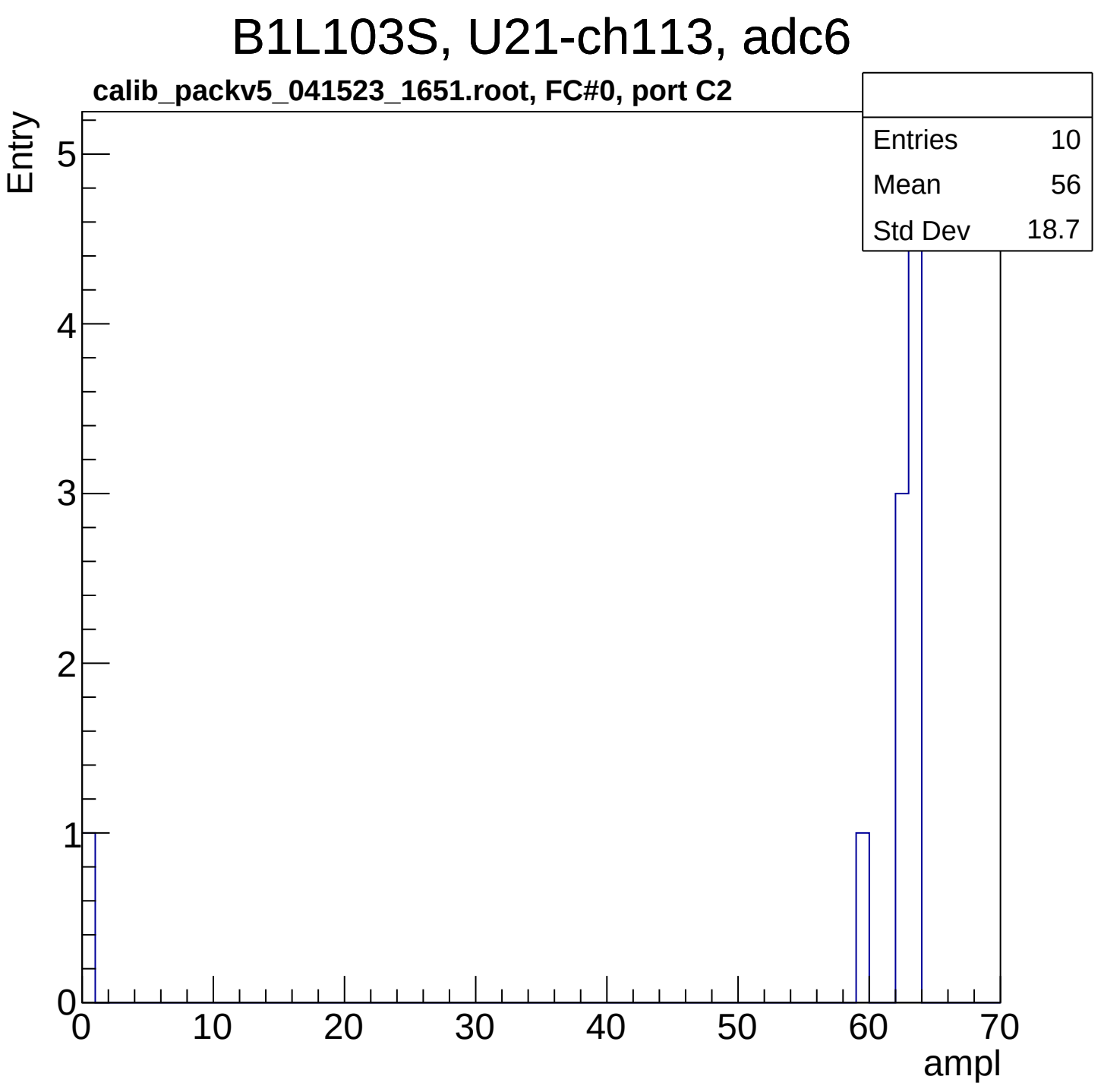
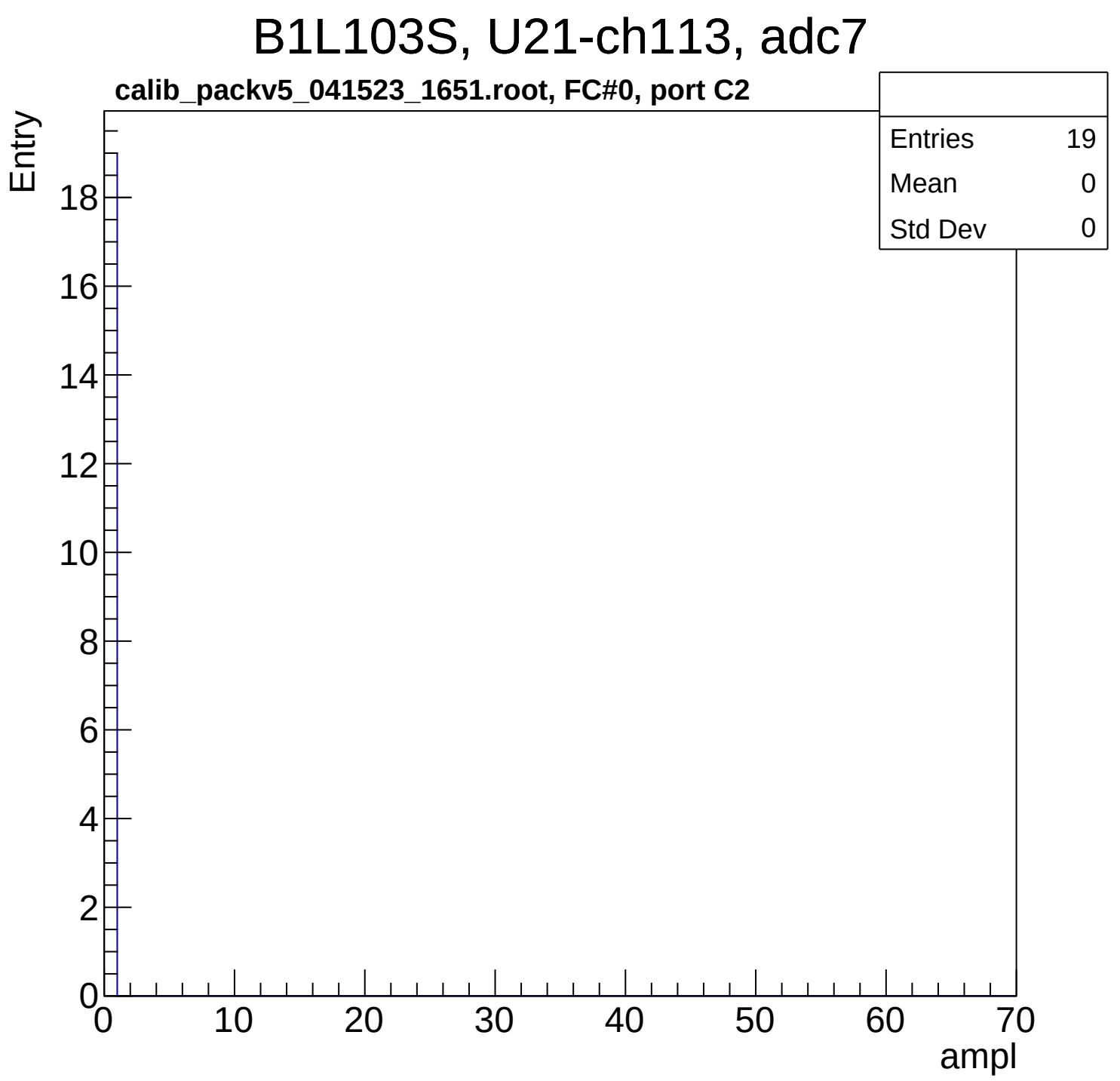

B1L103S, U21-ch113, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 56
Std Dev 18.7
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch113, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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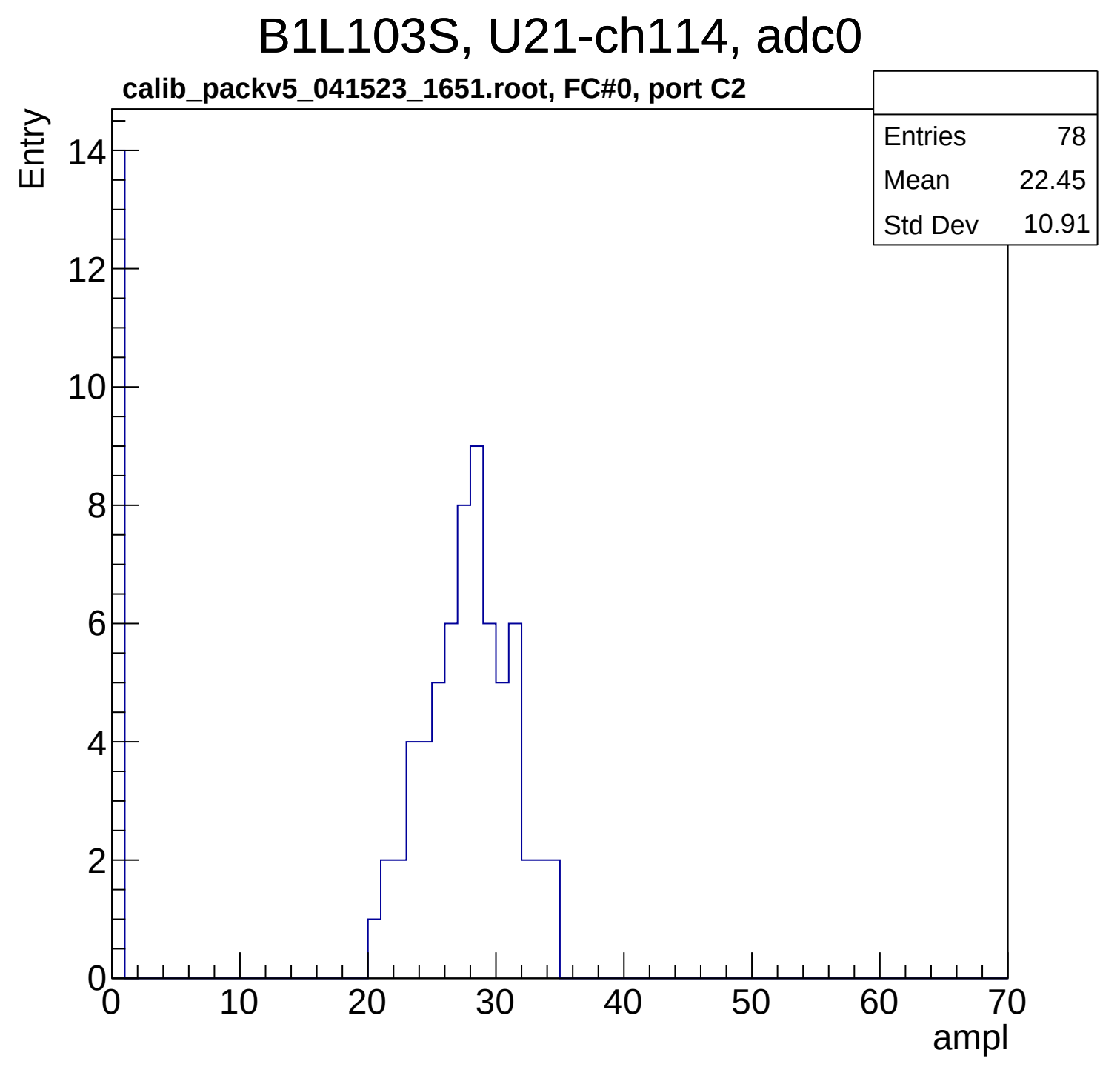
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch114, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 22.45
Std Dev 10.91
Entry
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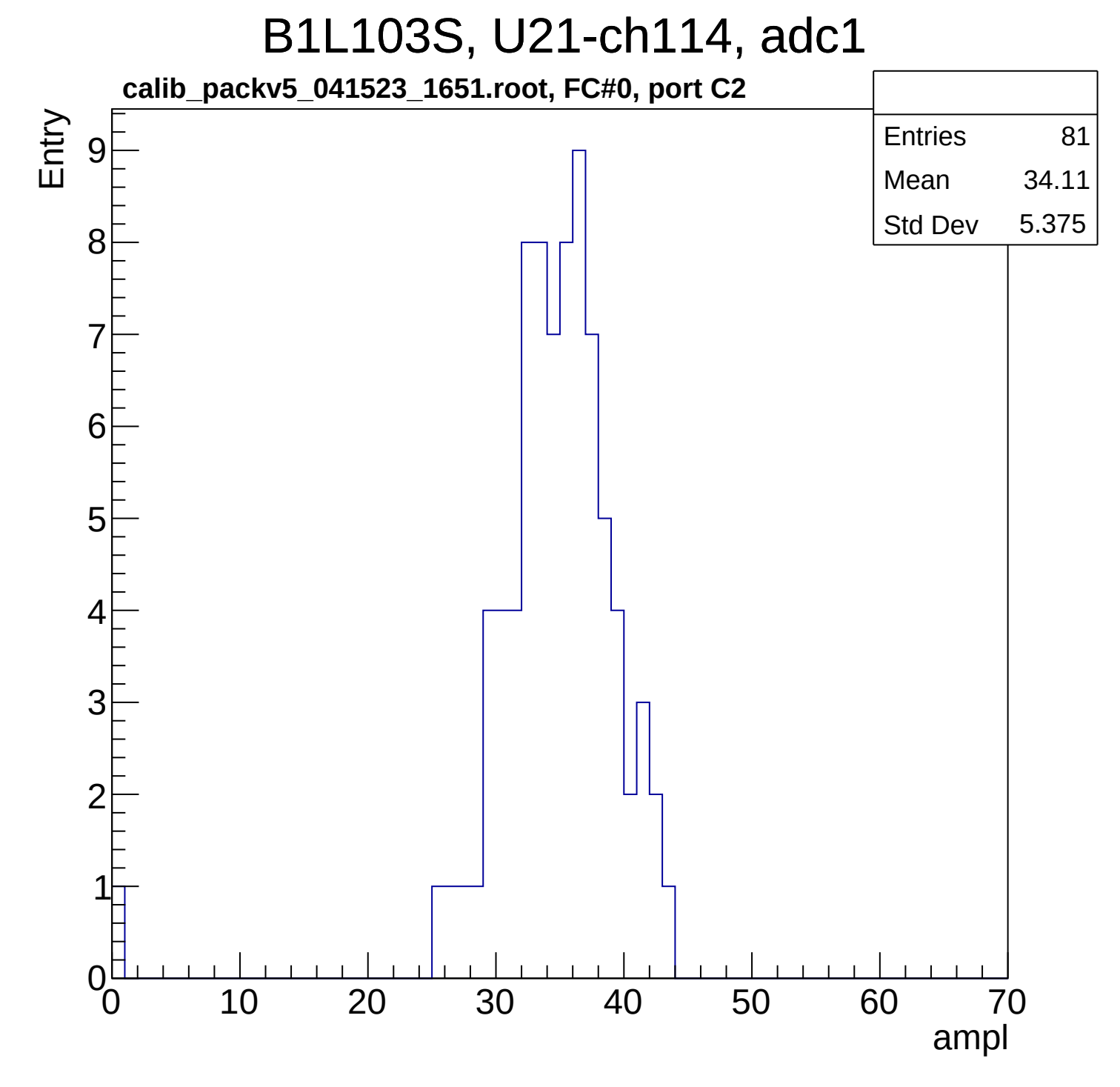
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch114, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 34.11
Std Dev 5.375
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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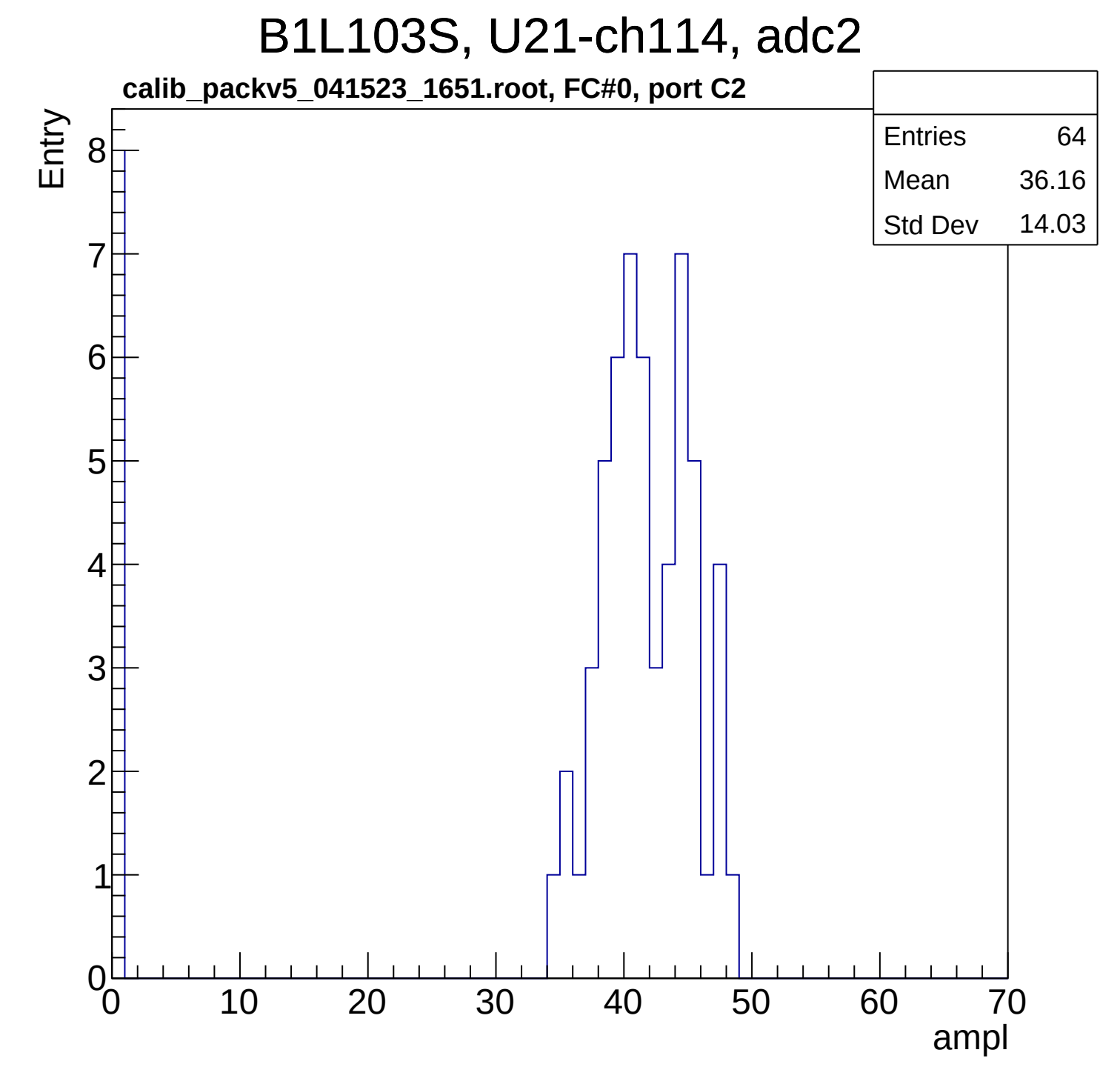
B1L103S, U21-ch114, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 36.16
Std Dev 14.03
Entry
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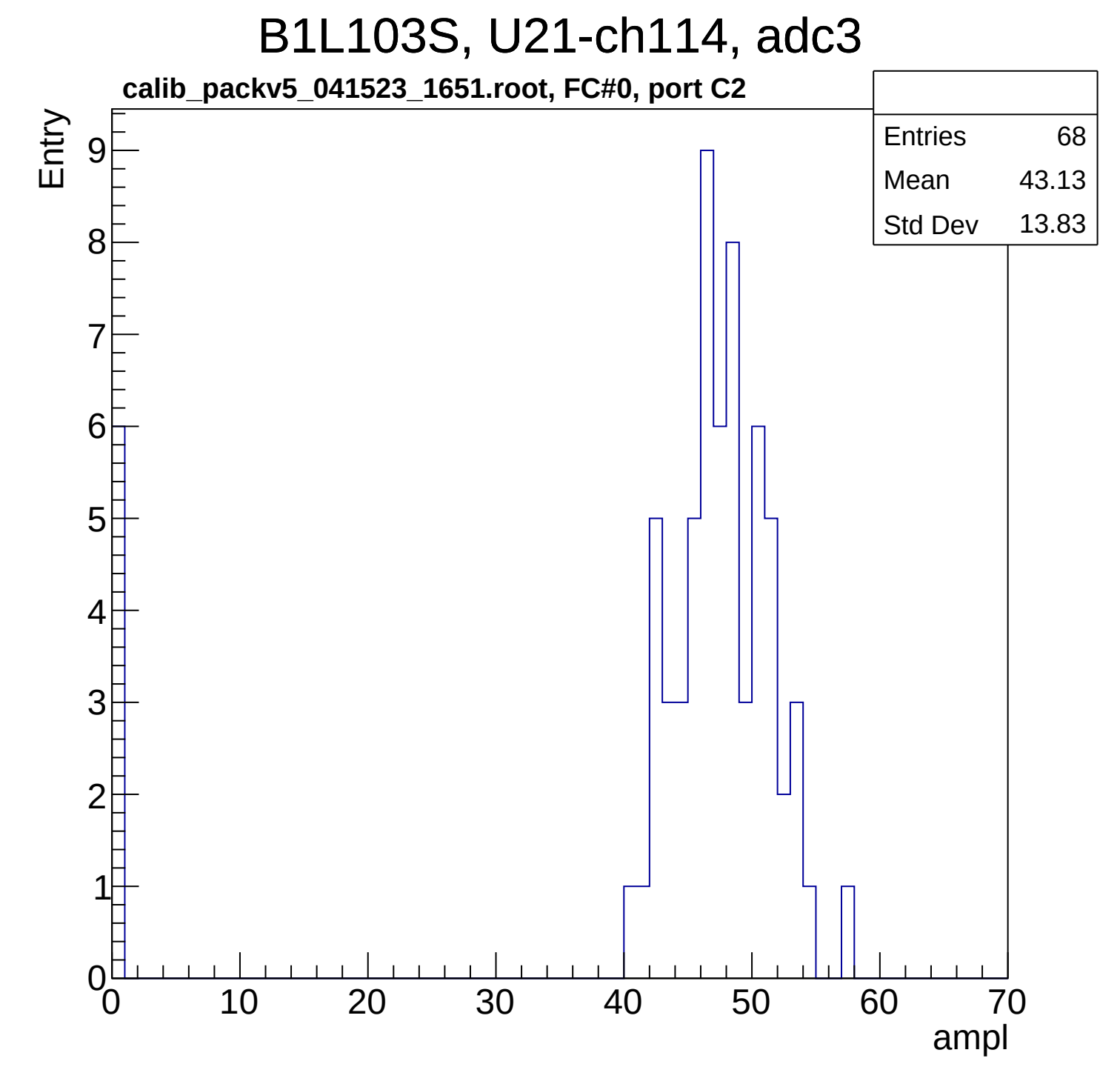
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch114, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 43.13
Std Dev 13.83
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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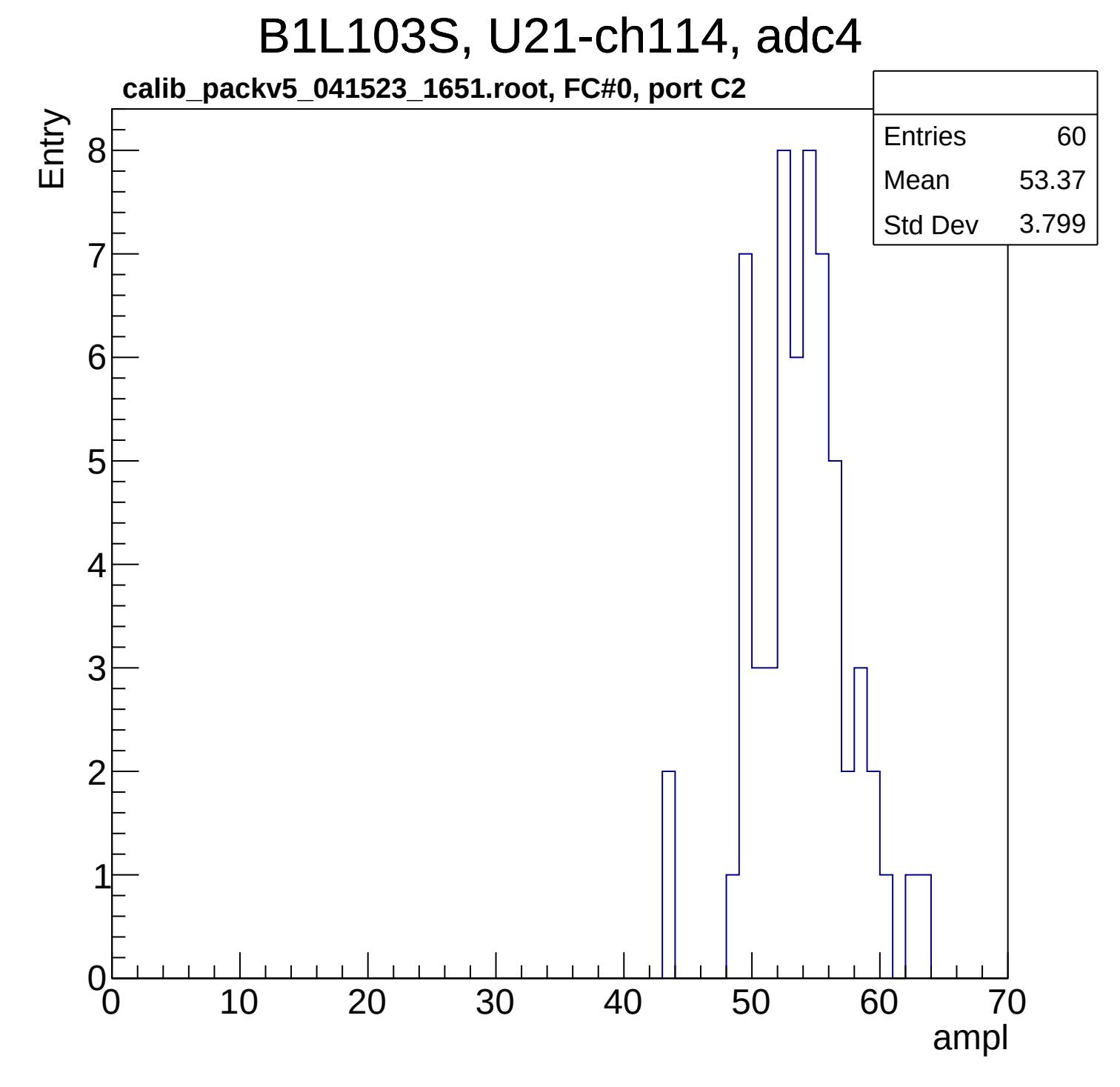
B1L103S, U21-ch114, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 53.37
Std Dev 3.799
Entry
ampl
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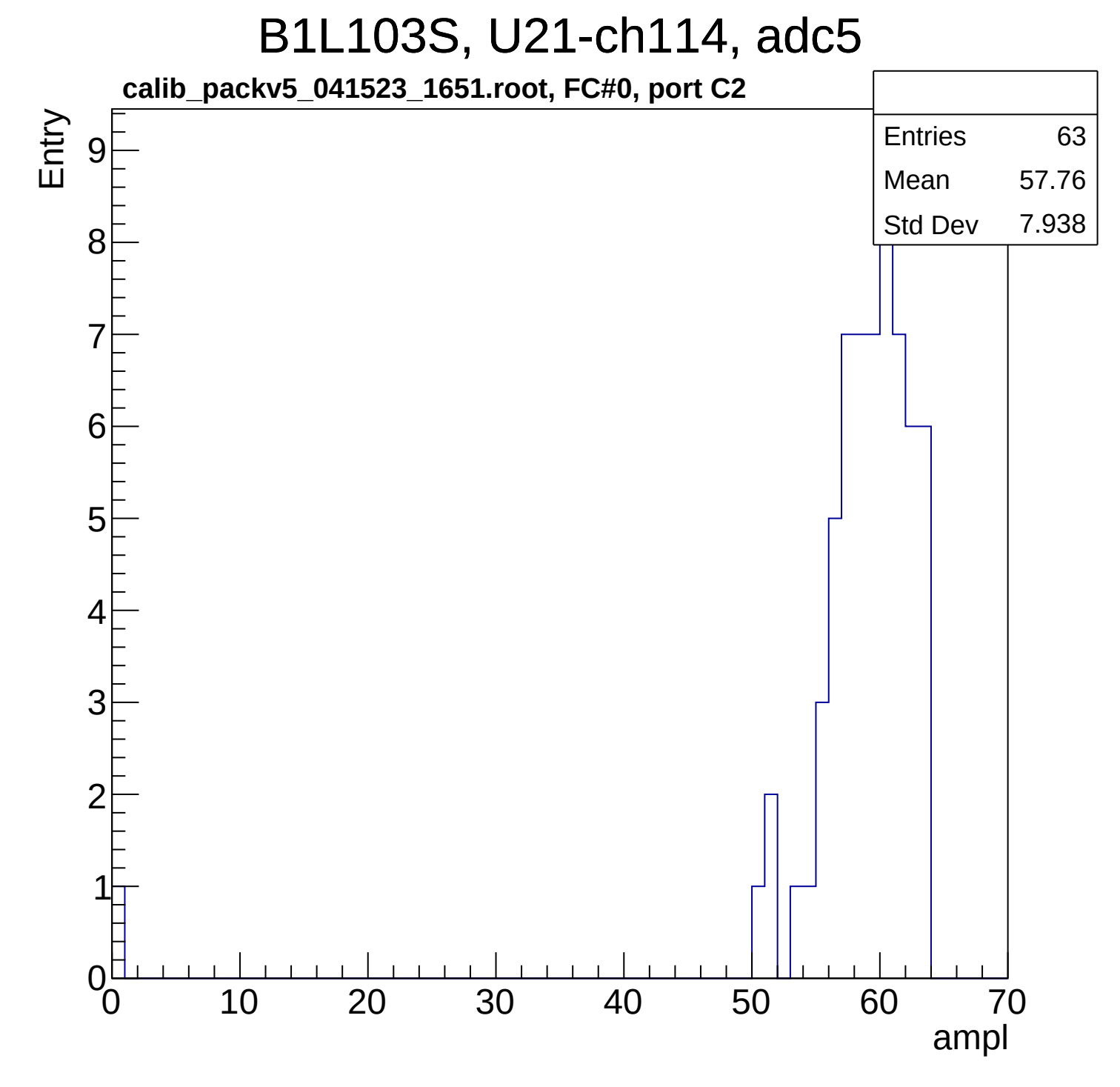
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch114, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 57.76
Std Dev 7.938
Entry
ampl
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2
3
4
5
6
7
8
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0
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60
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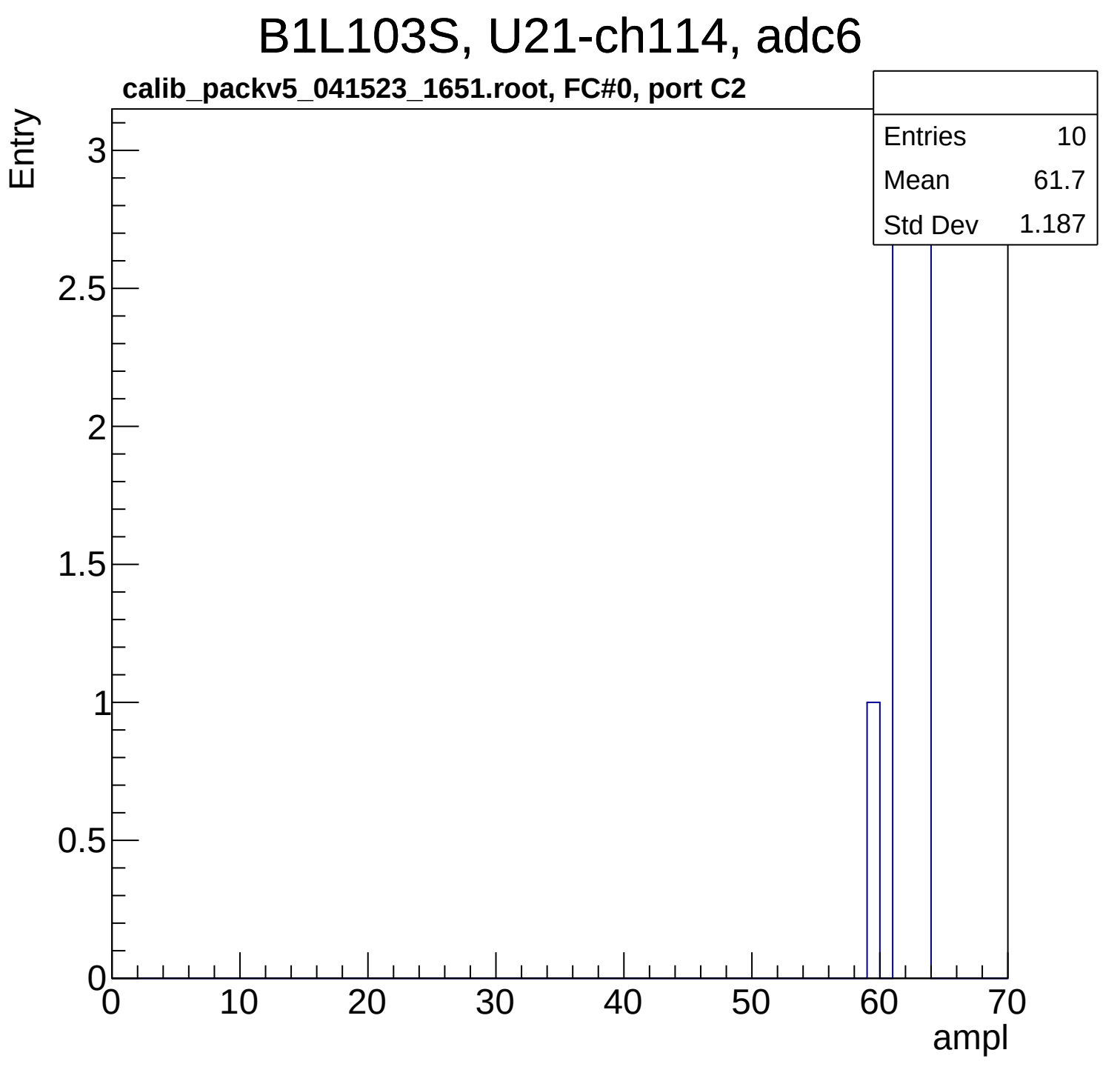
B1L103S, U21-ch114, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61.7
Std Dev 1.187
Entry
ampl
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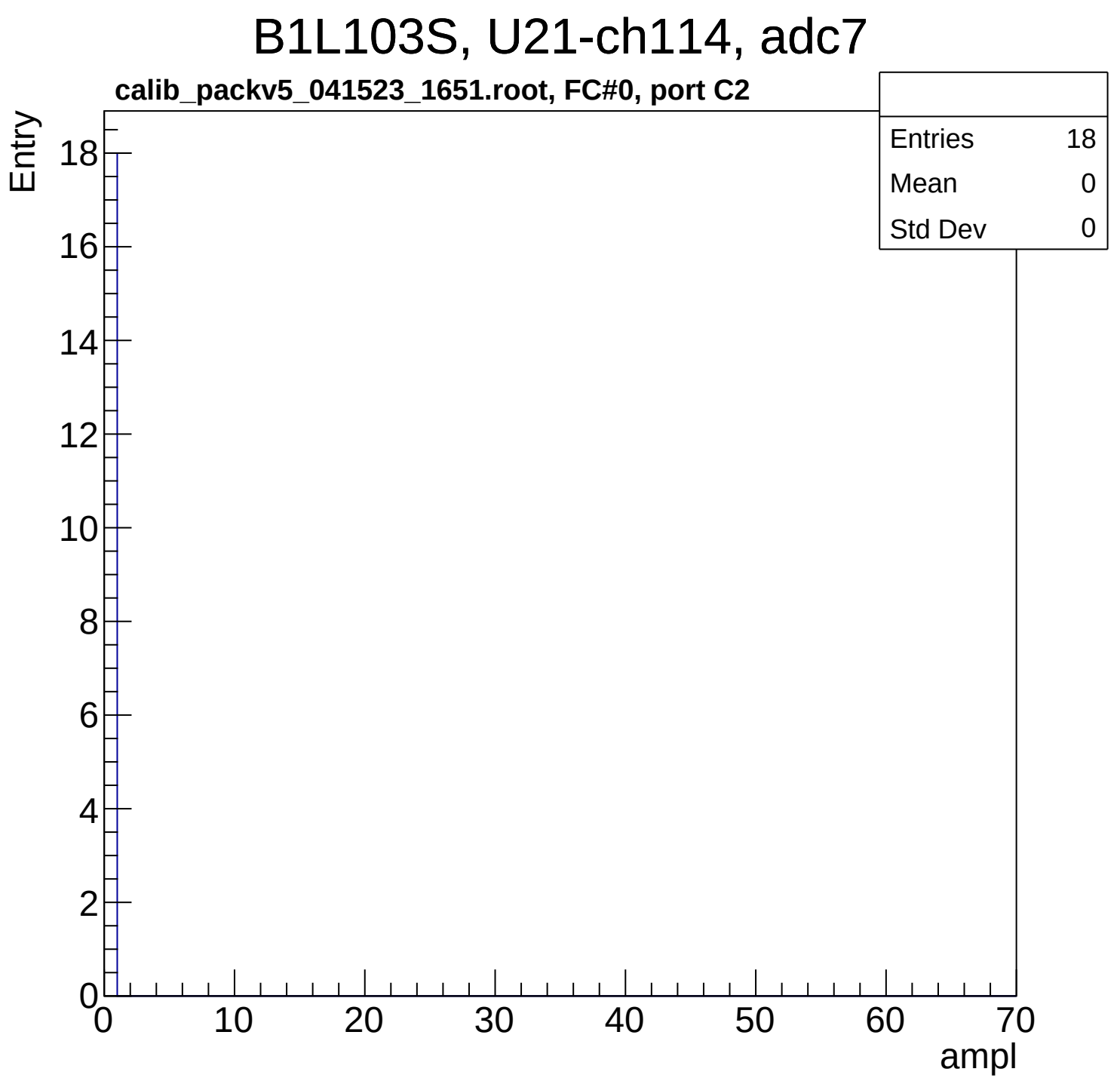
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U21-ch114, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
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2
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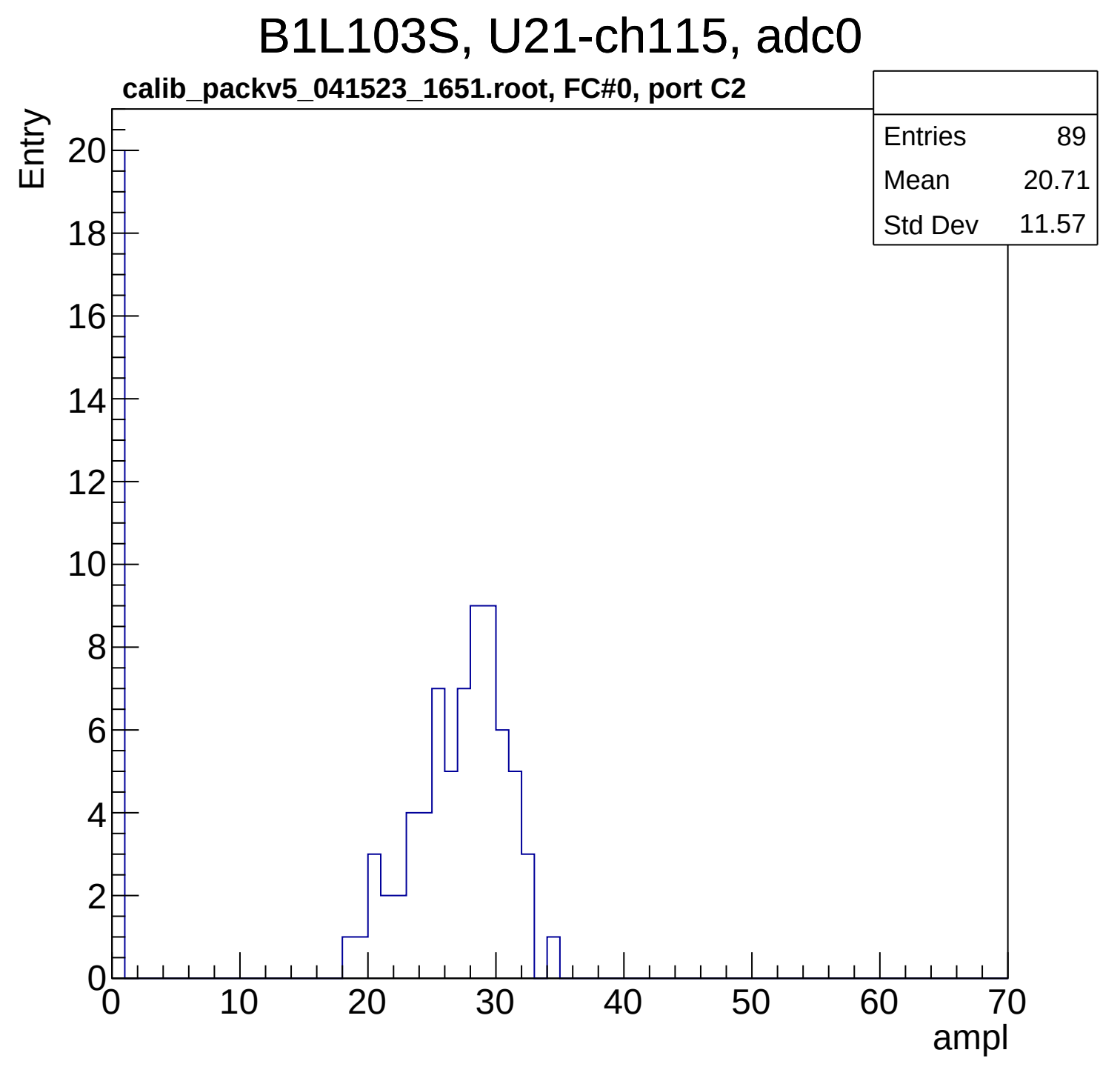
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch115, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 20.71
Std Dev 11.57
Entry
ampl
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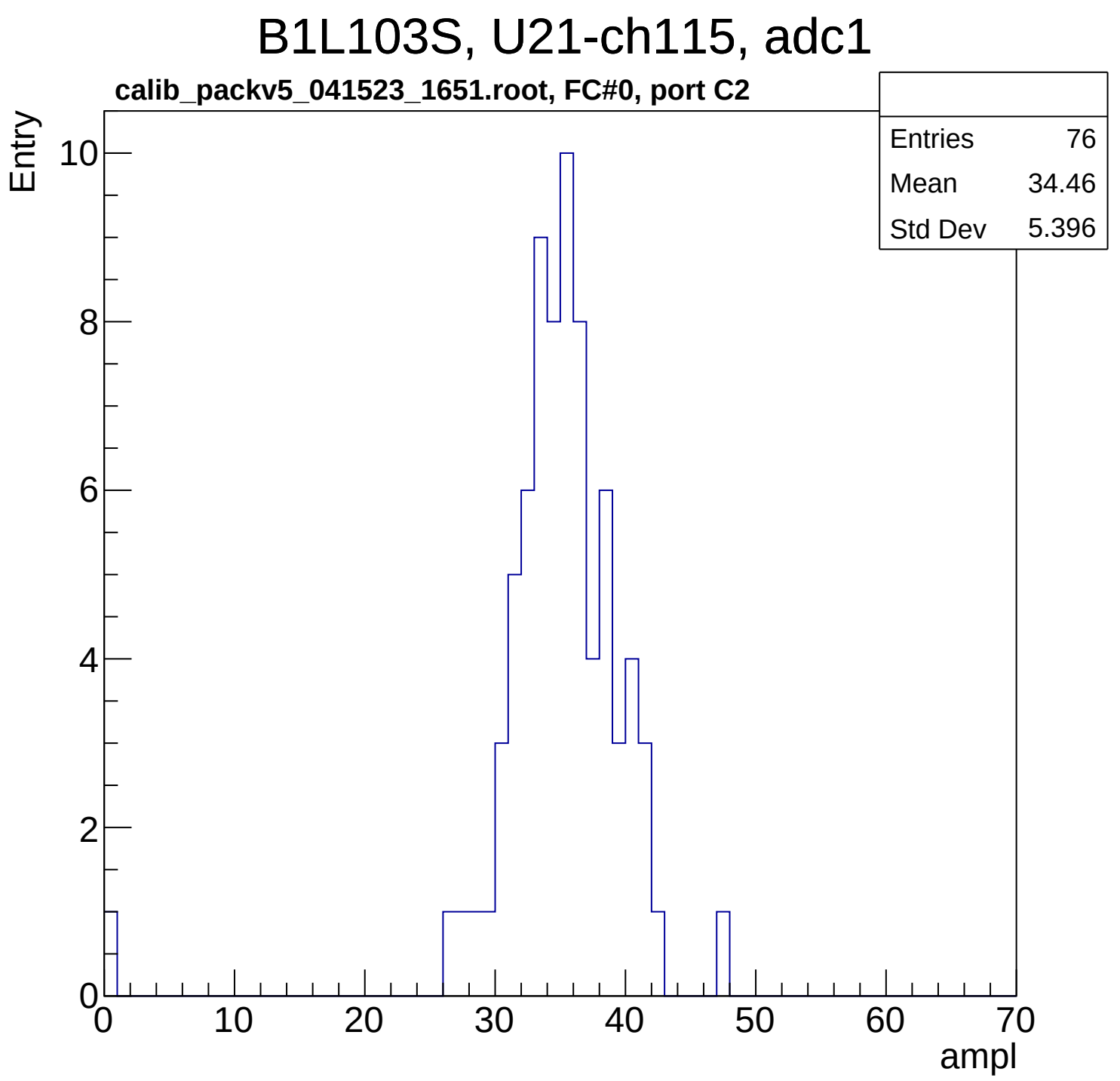
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70


B1L103S, U21-ch115, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 34.46
Std Dev 5.396
Entry
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2
4
6
8
10
0
10
20
30
40
50
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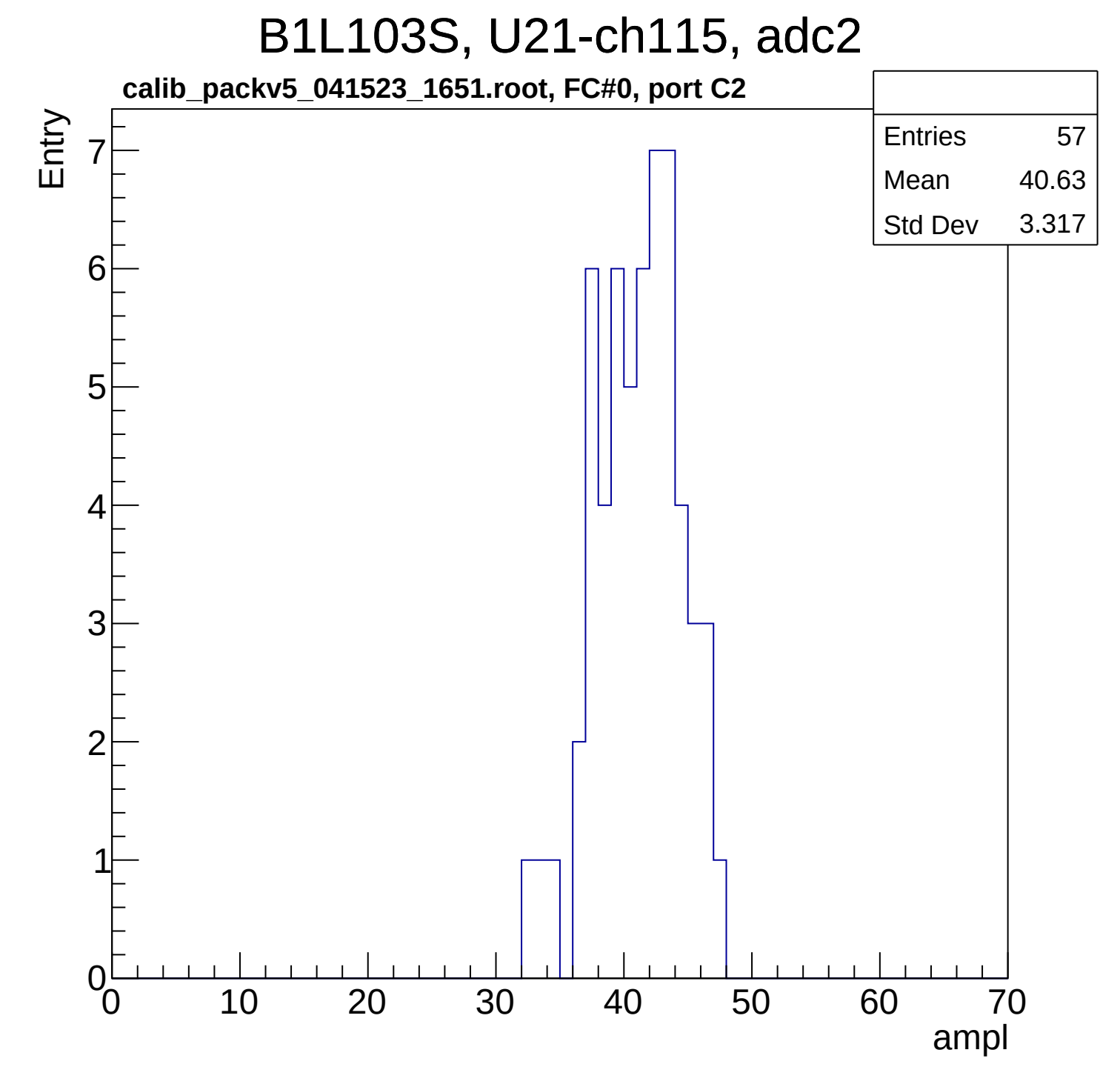
70
ampl


B1L103S, U21-ch115, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 40.63
Std Dev 3.317
Entry
ampl
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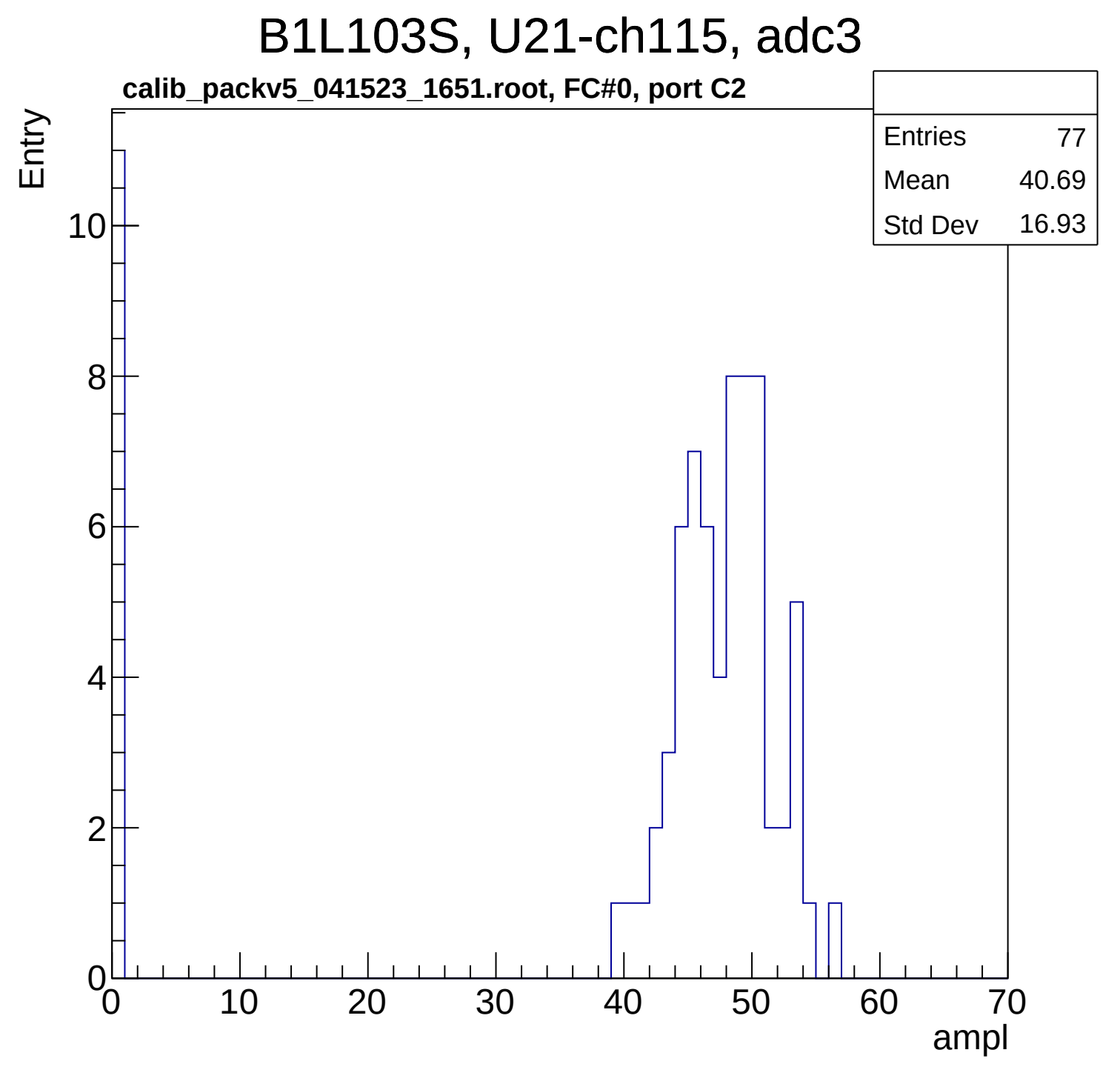
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U21-ch115, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 40.69
Std Dev 16.93
Entry
ampl
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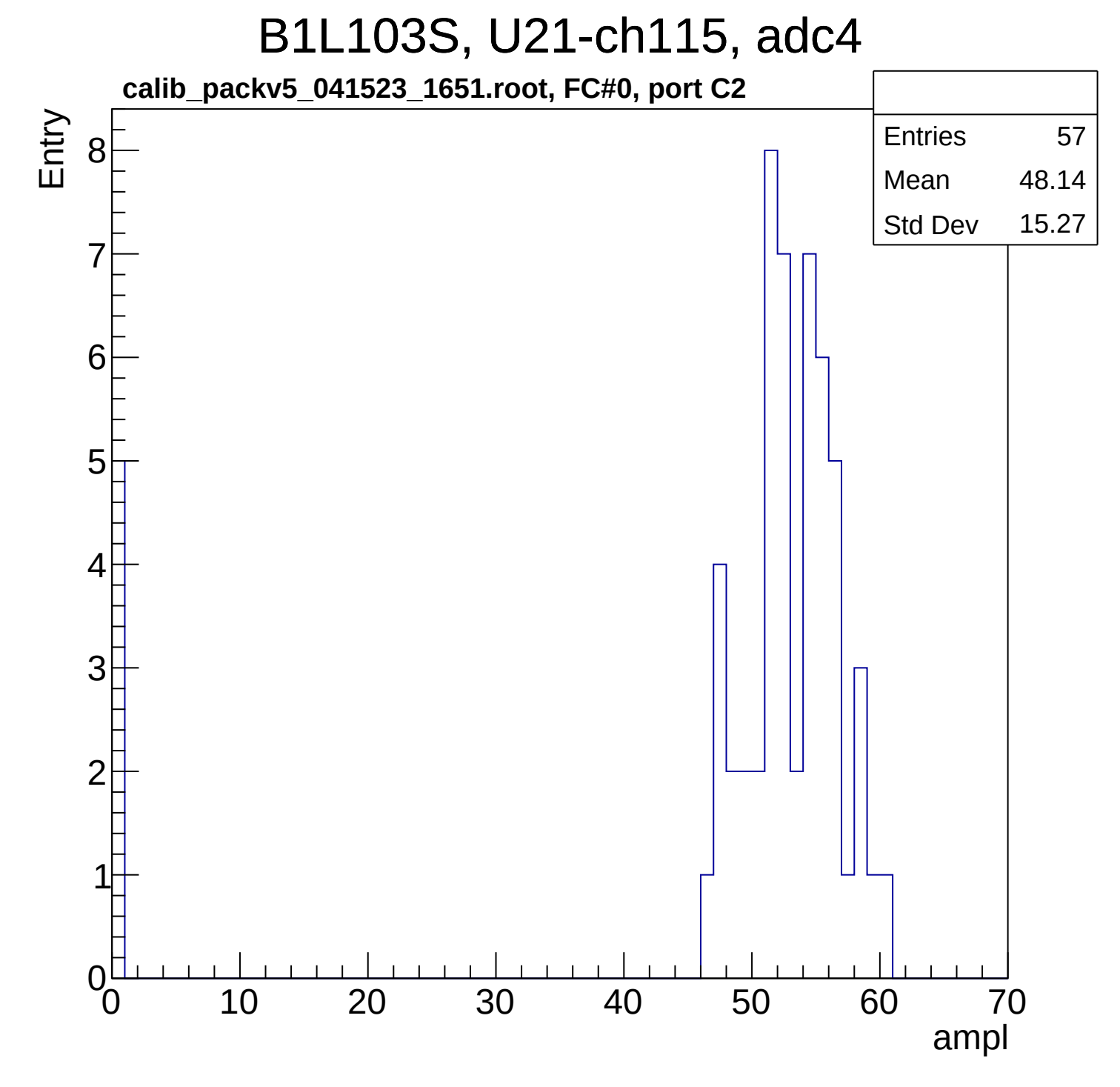
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U21-ch115, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 48.14
Std Dev 15.27
Entry
ampl
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2
3
4
5
6
7
8
0
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40
50
60
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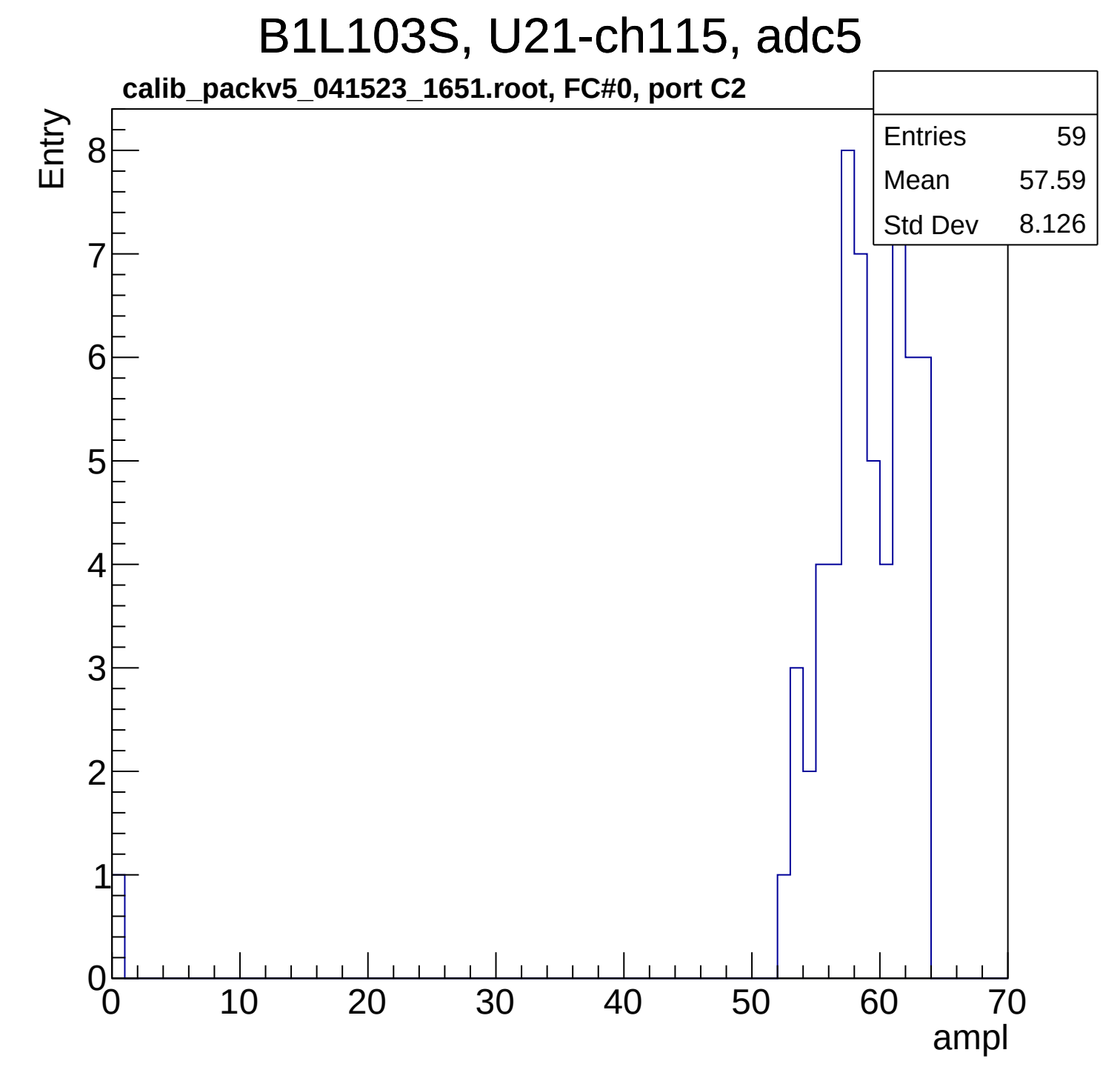
B1L103S, U21-ch115, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 57.59
Std Dev 8.126
Entry
ampl
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2
3
4
5
6
7
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0
10
20
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40
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60
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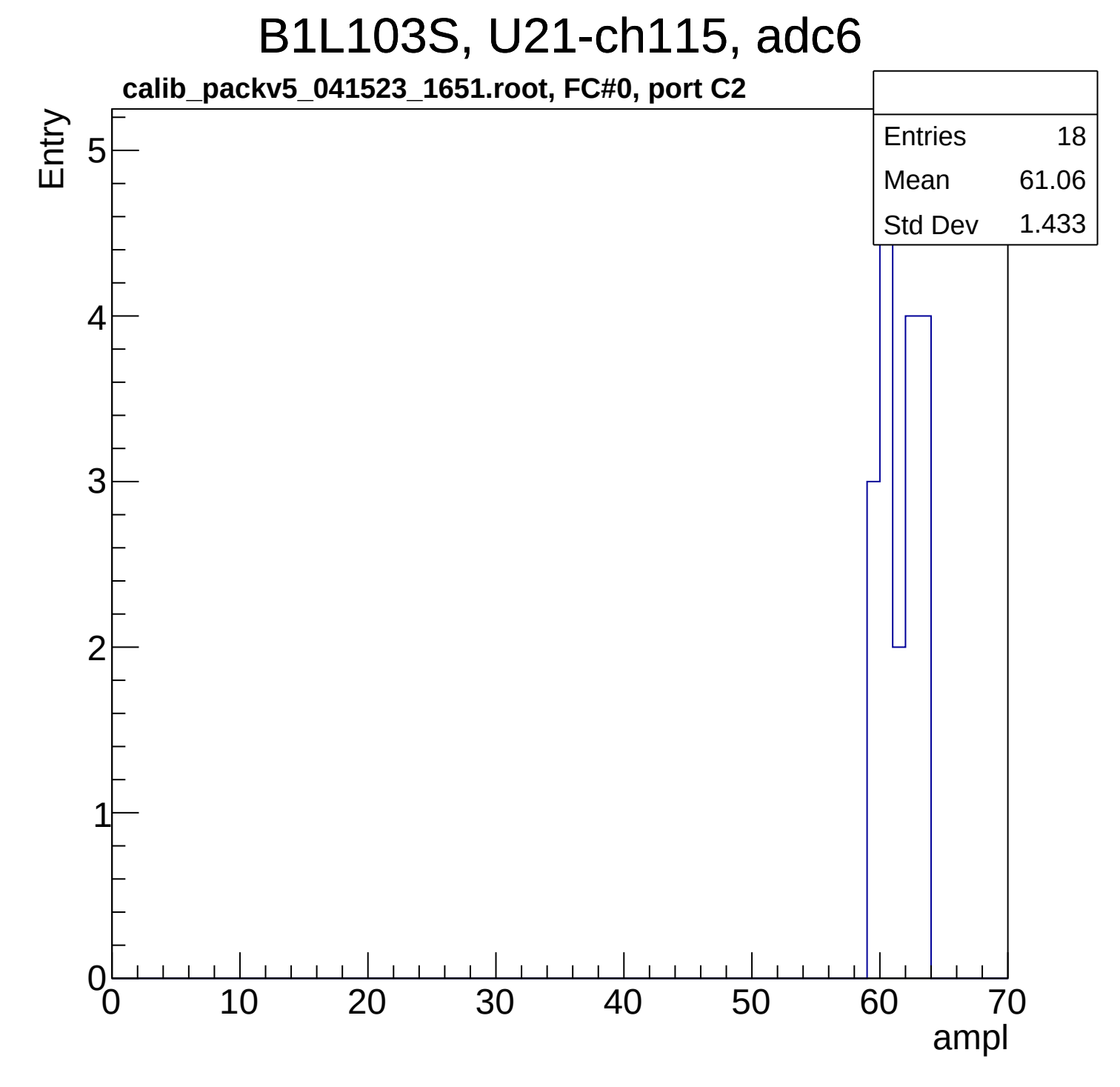
B1L103S, U21-ch115, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 61.06
Std Dev 1.433
Entry
ampl
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2
3
4
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0
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40
50
60
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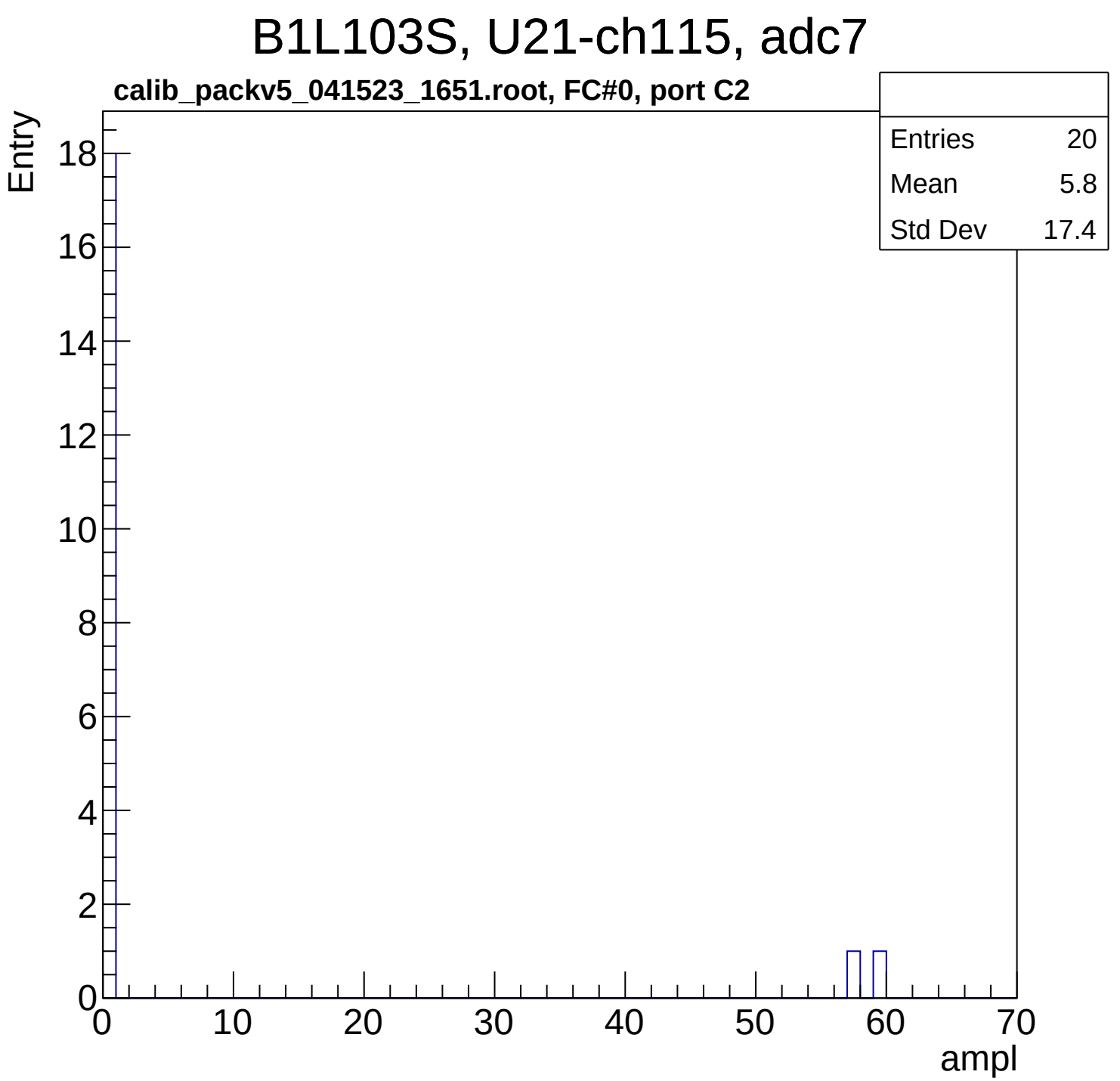
B1L103S, U21-ch115, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 5.8
Std Dev 17.4
Entry
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6
8
10
12
14
16
18
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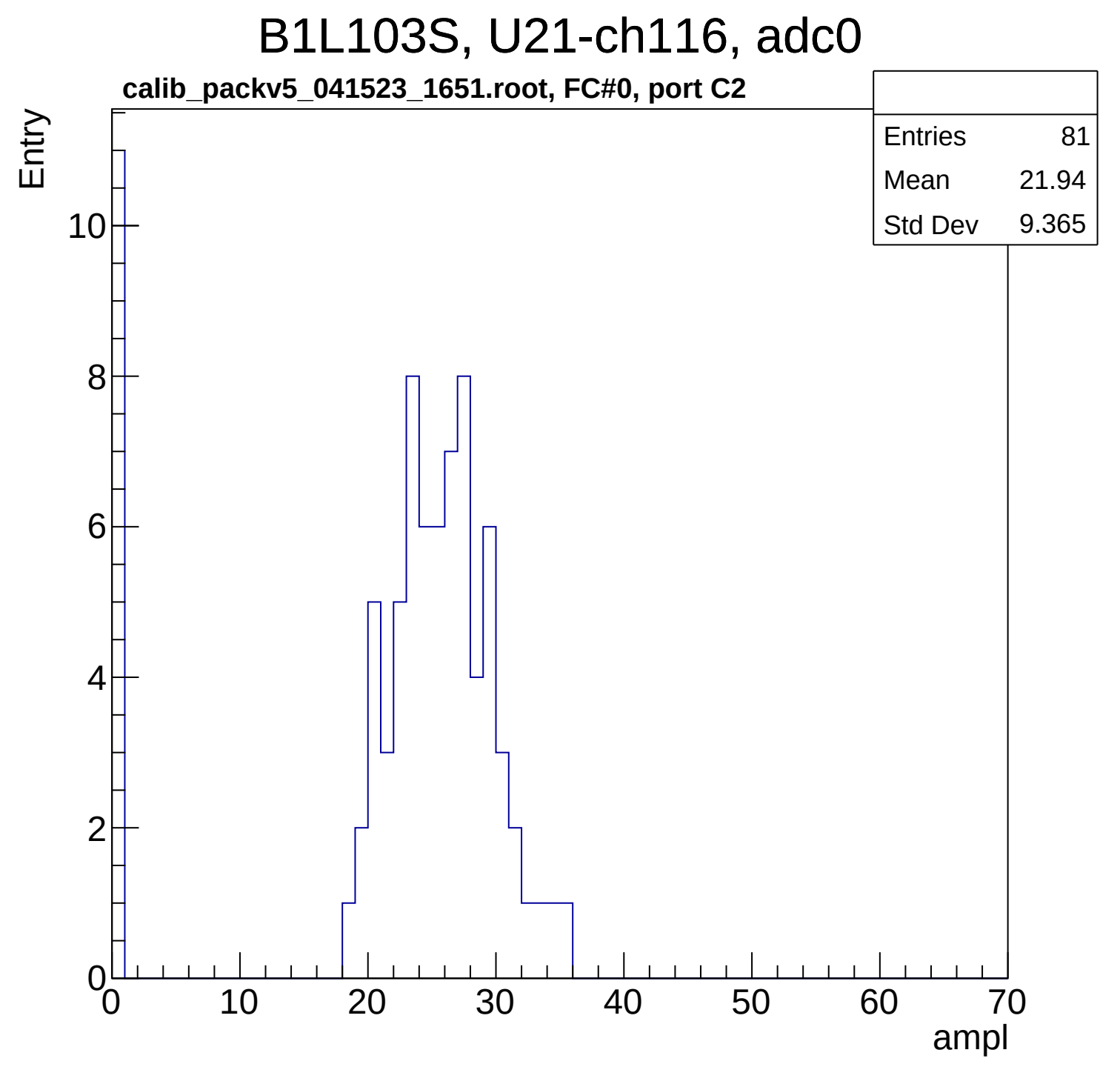
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch116, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 21.94
Std Dev 9.365
Entry
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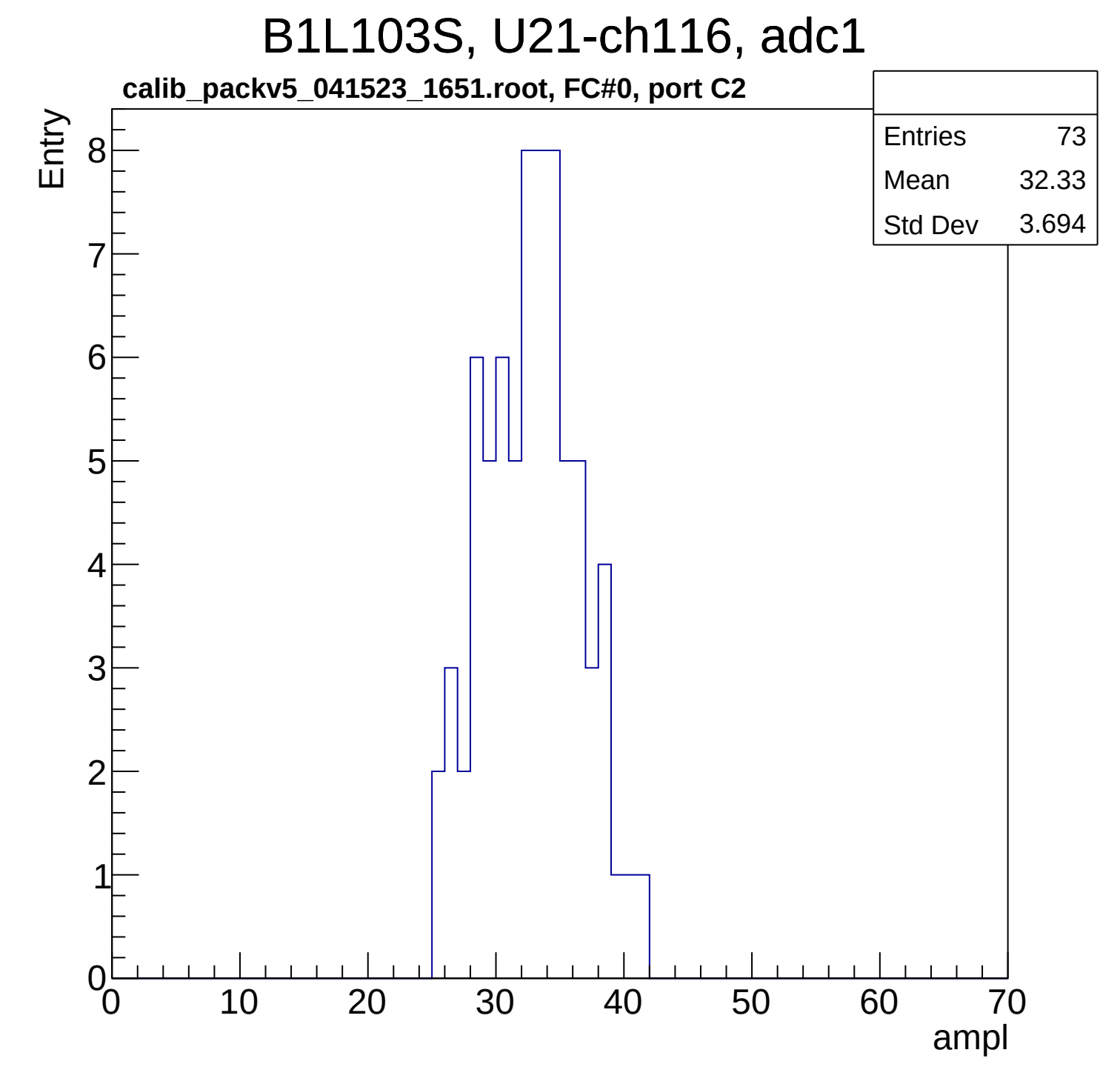
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch116, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 32.33
Std Dev 3.694
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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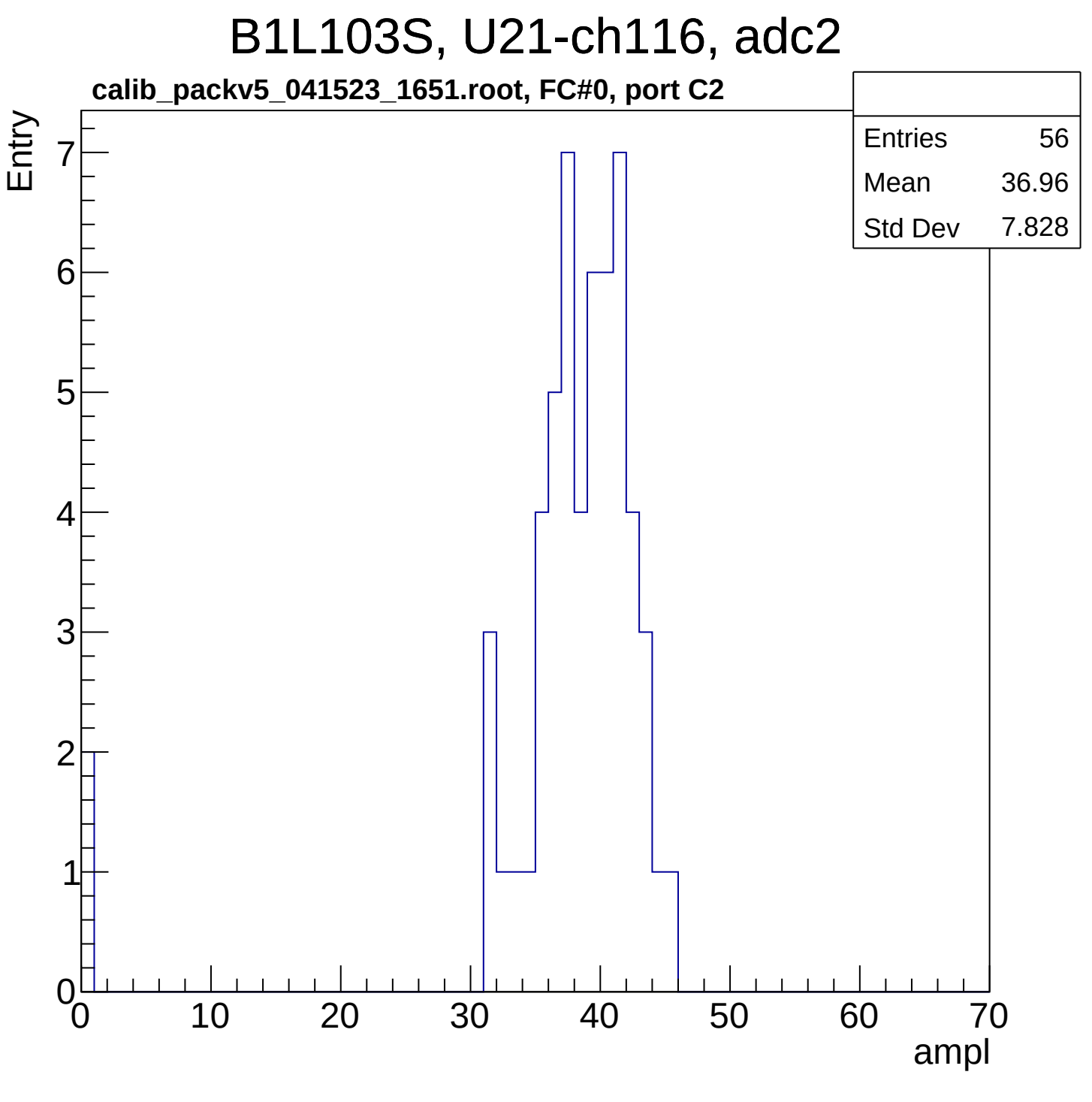
40
50
60
70


B1L103S, U21-ch116, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 36.96
Std Dev 7.828
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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40
50
60
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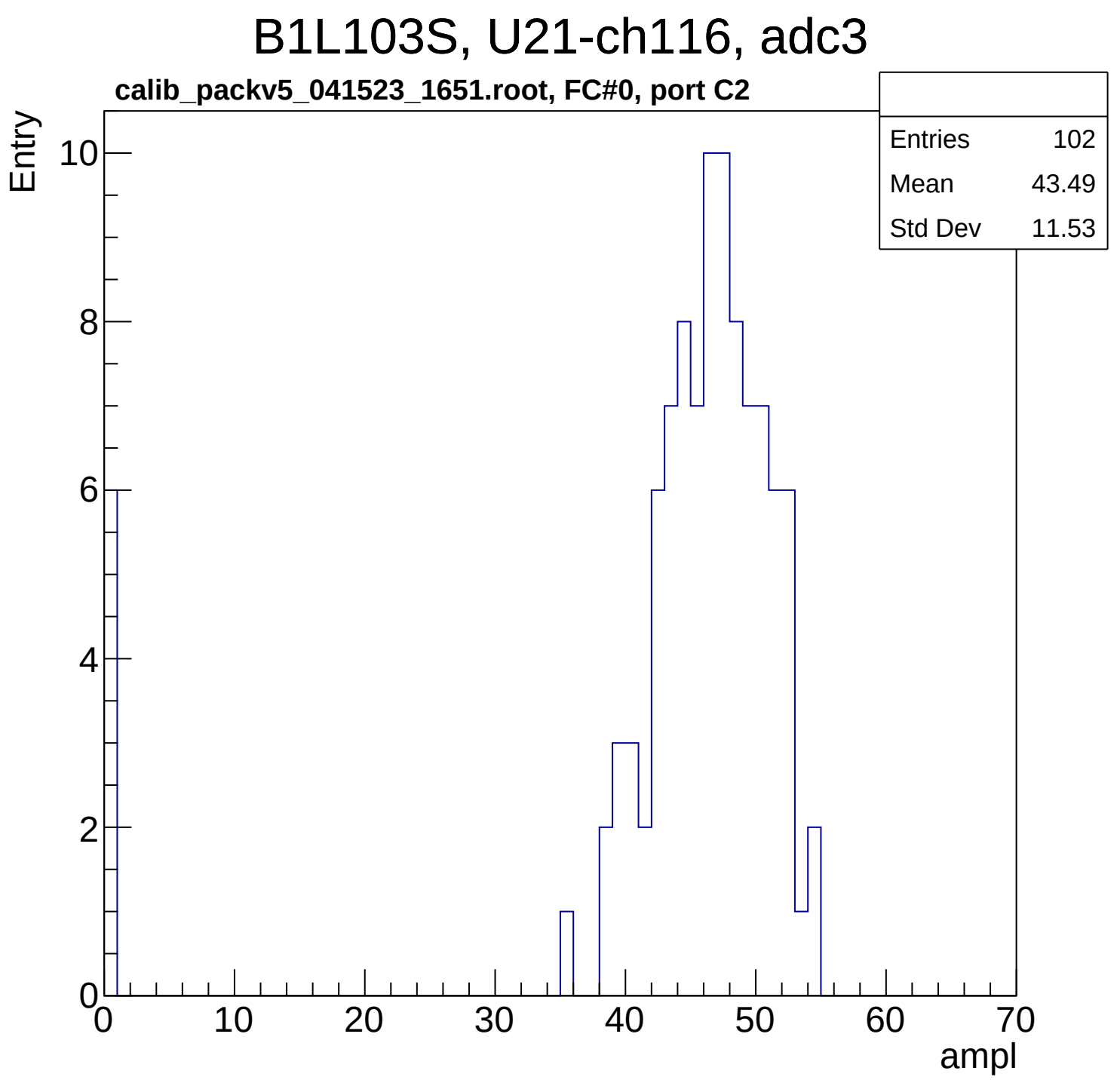
B1L103S, U21-ch116, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 102
Mean 43.49
Std Dev 11.53
Entry
ampl
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2
4
6
8
10
0
10
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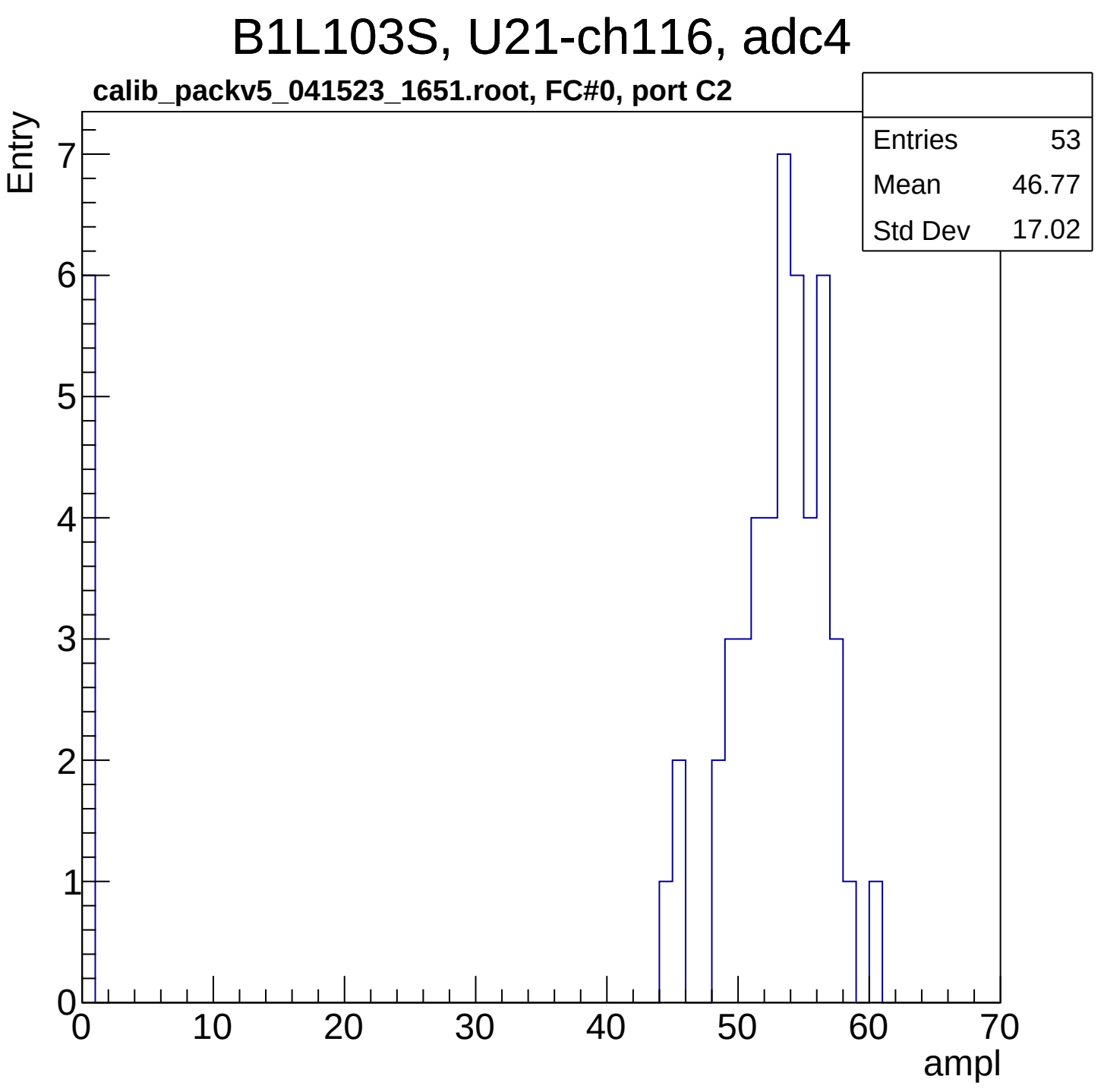
40
50
60
70


B1L103S, U21-ch116, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 46.77
Std Dev 17.02
Entry
ampl
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2
3
4
5
6
7
0
10
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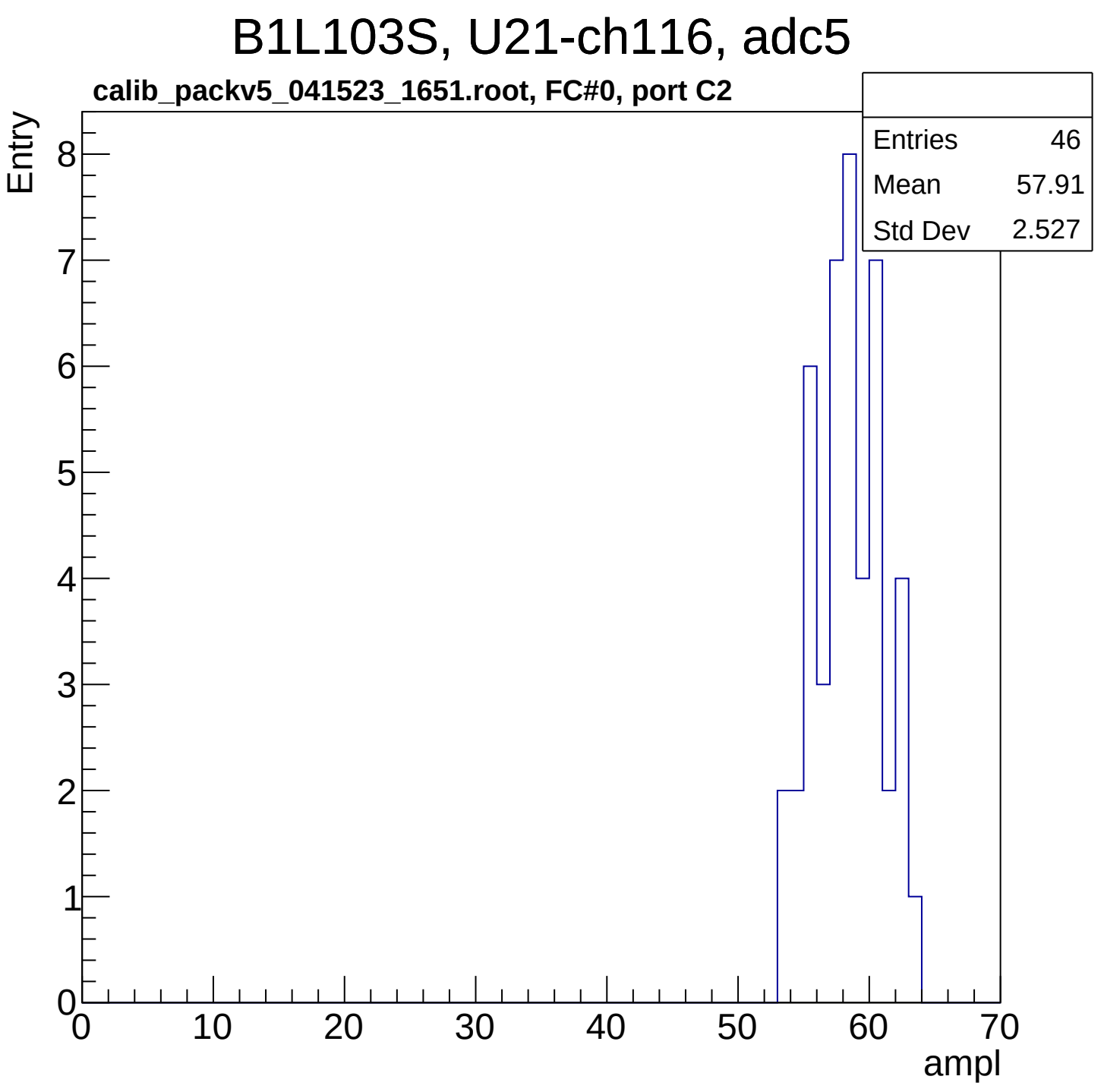
40
50
60
70


B1L103S, U21-ch116, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 57.91
Std Dev 2.527
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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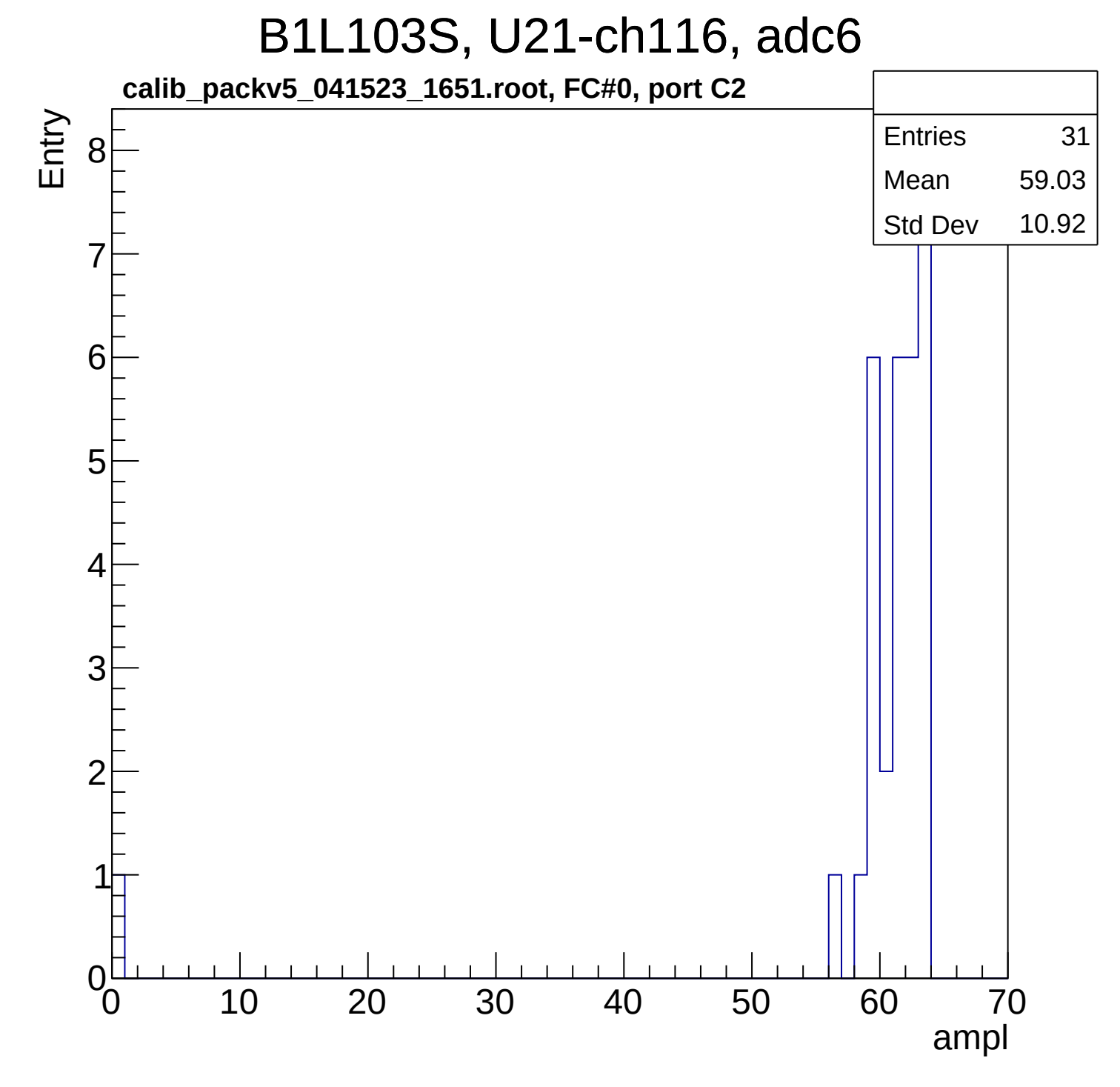
B1L103S, U21-ch116, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 59.03
Std Dev 10.92
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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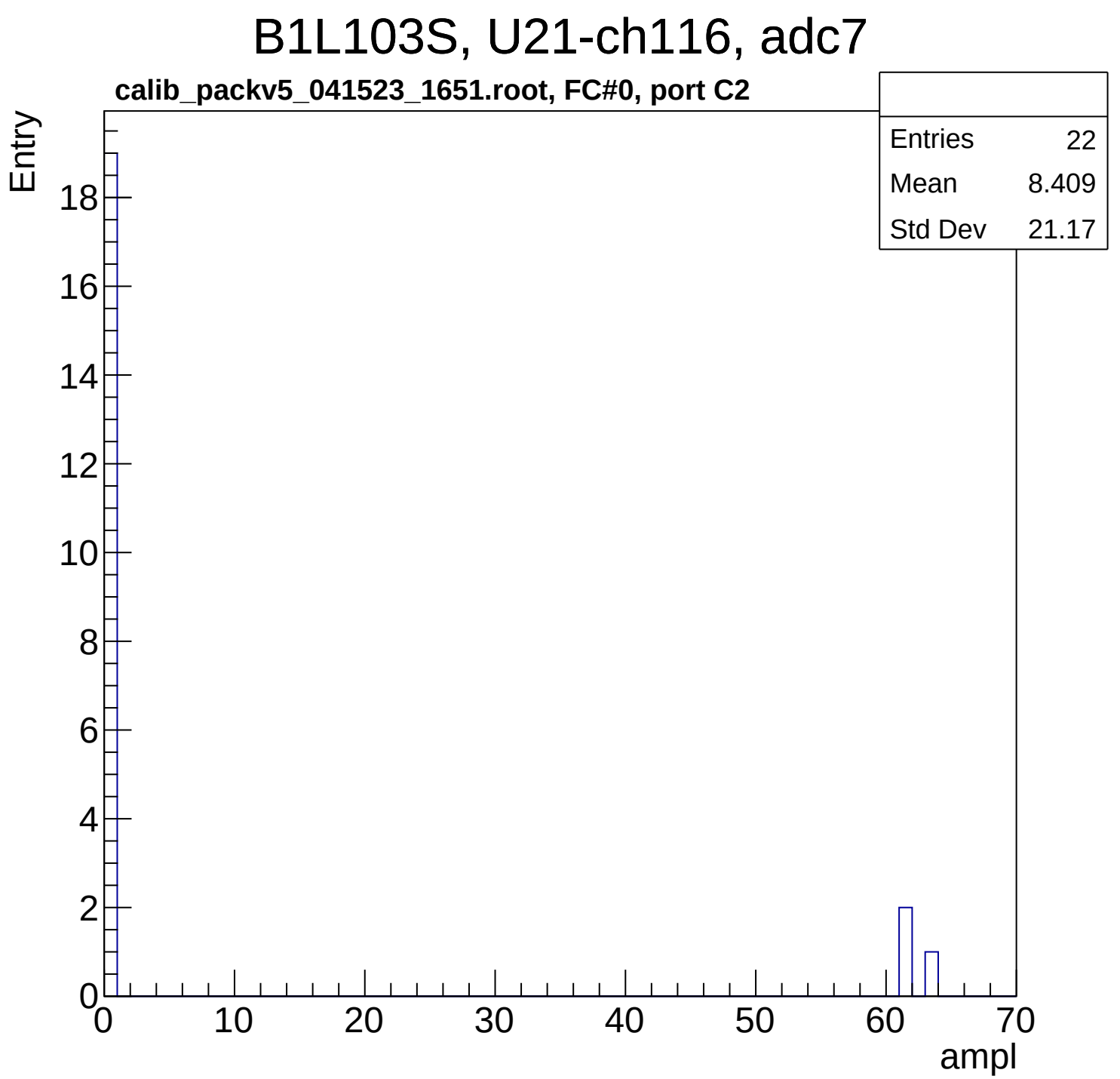
B1L103S, U21-ch116, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.409
Std Dev 21.17
Entry
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6
8
10
12
14
16
18
0
10
20
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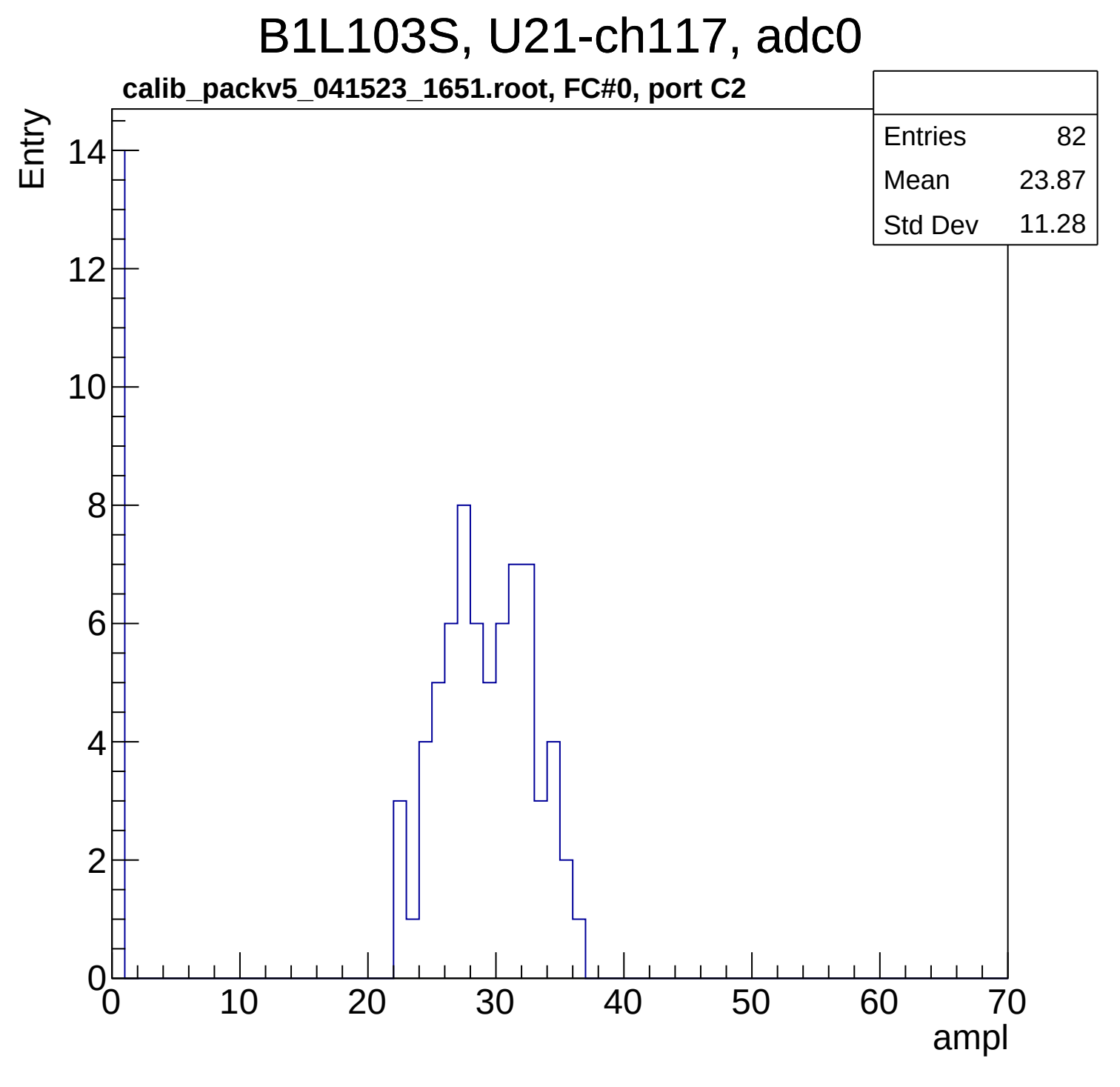
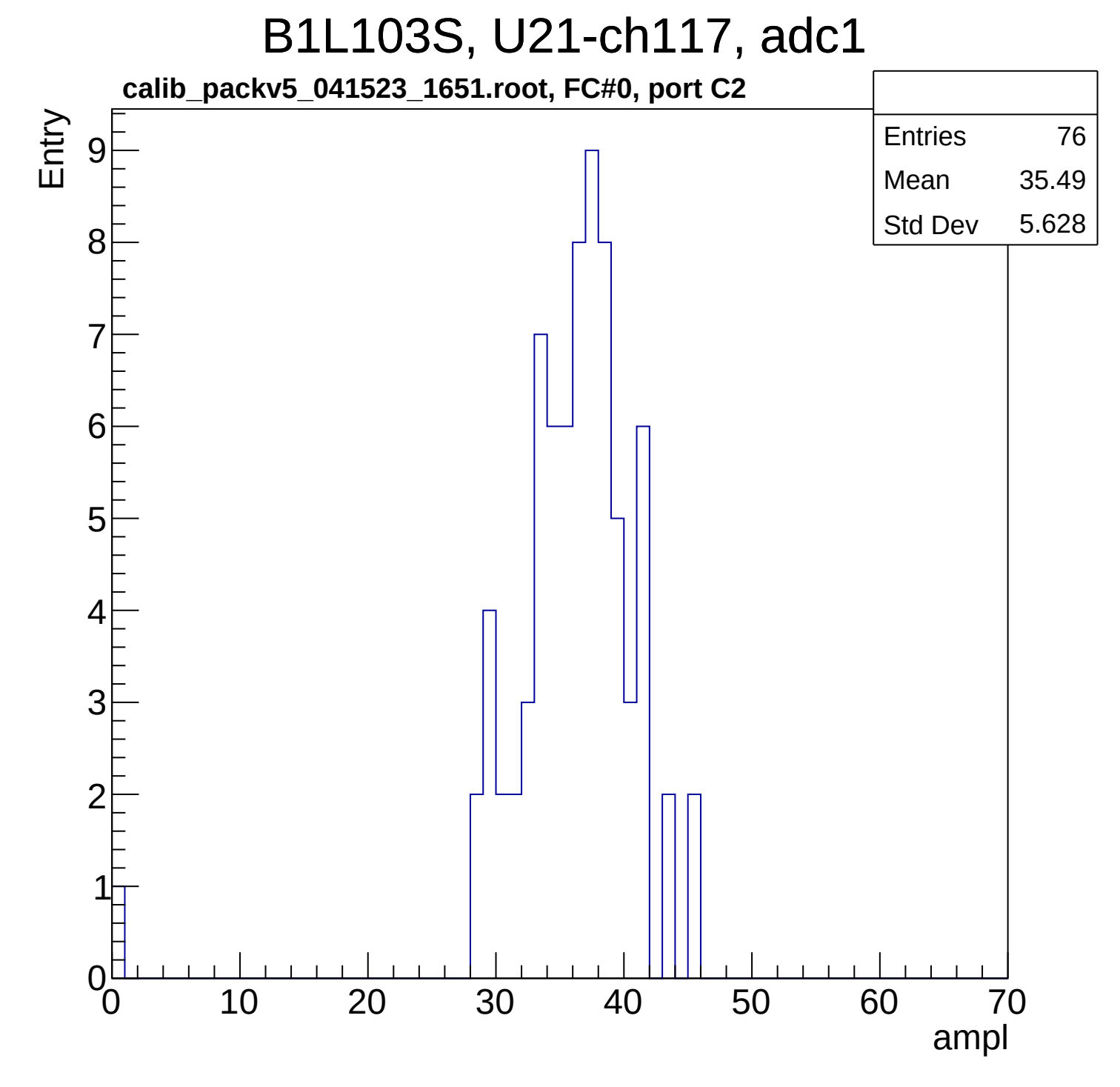
50
60
70
ampl


B1L103S, U21-ch117, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 23.87
Std Dev 11.28
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch117, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 35.49
Std Dev 5.628
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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20
30
40
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60
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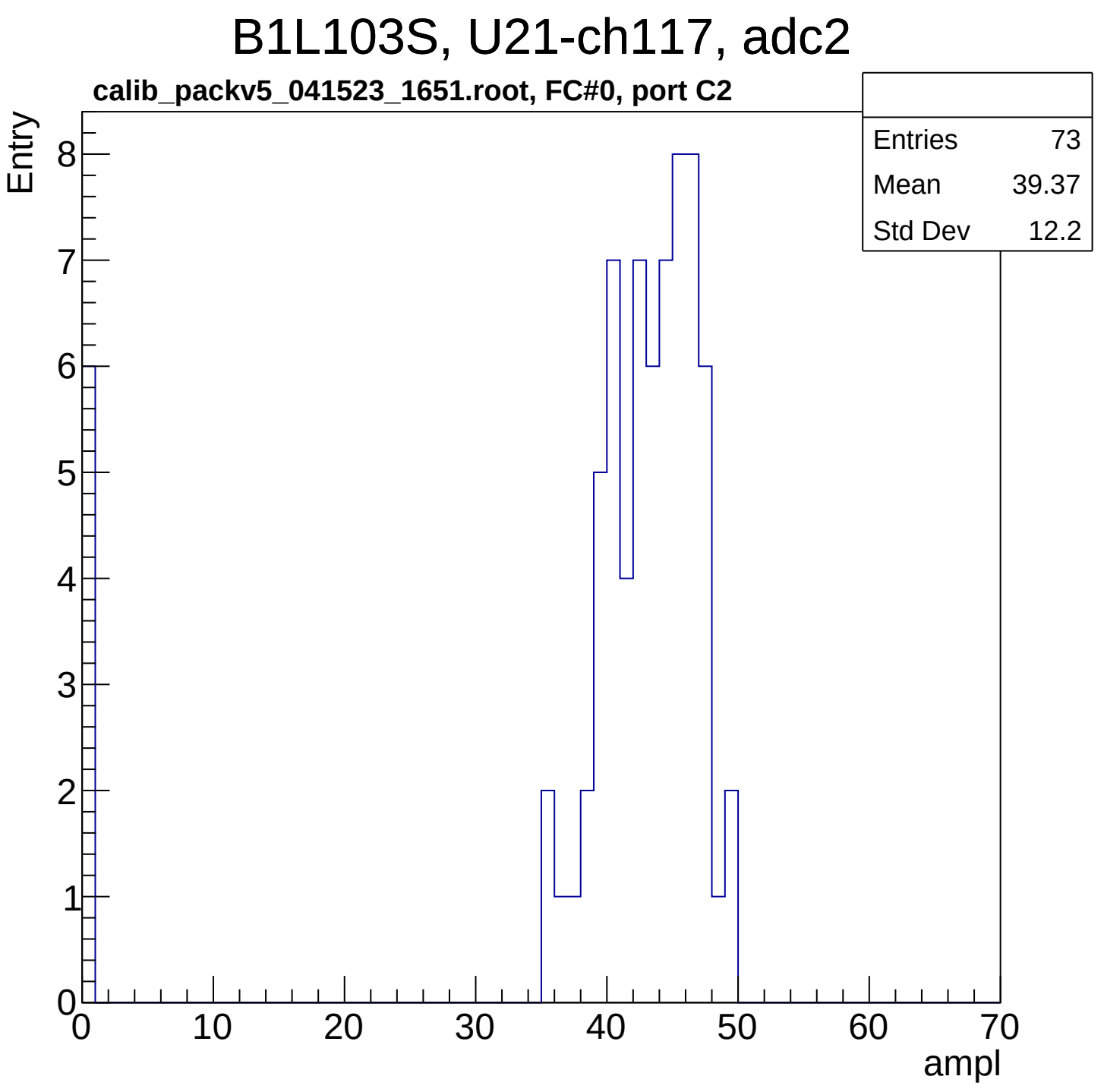
B1L103S, U21-ch117, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 39.37
Std Dev 12.2
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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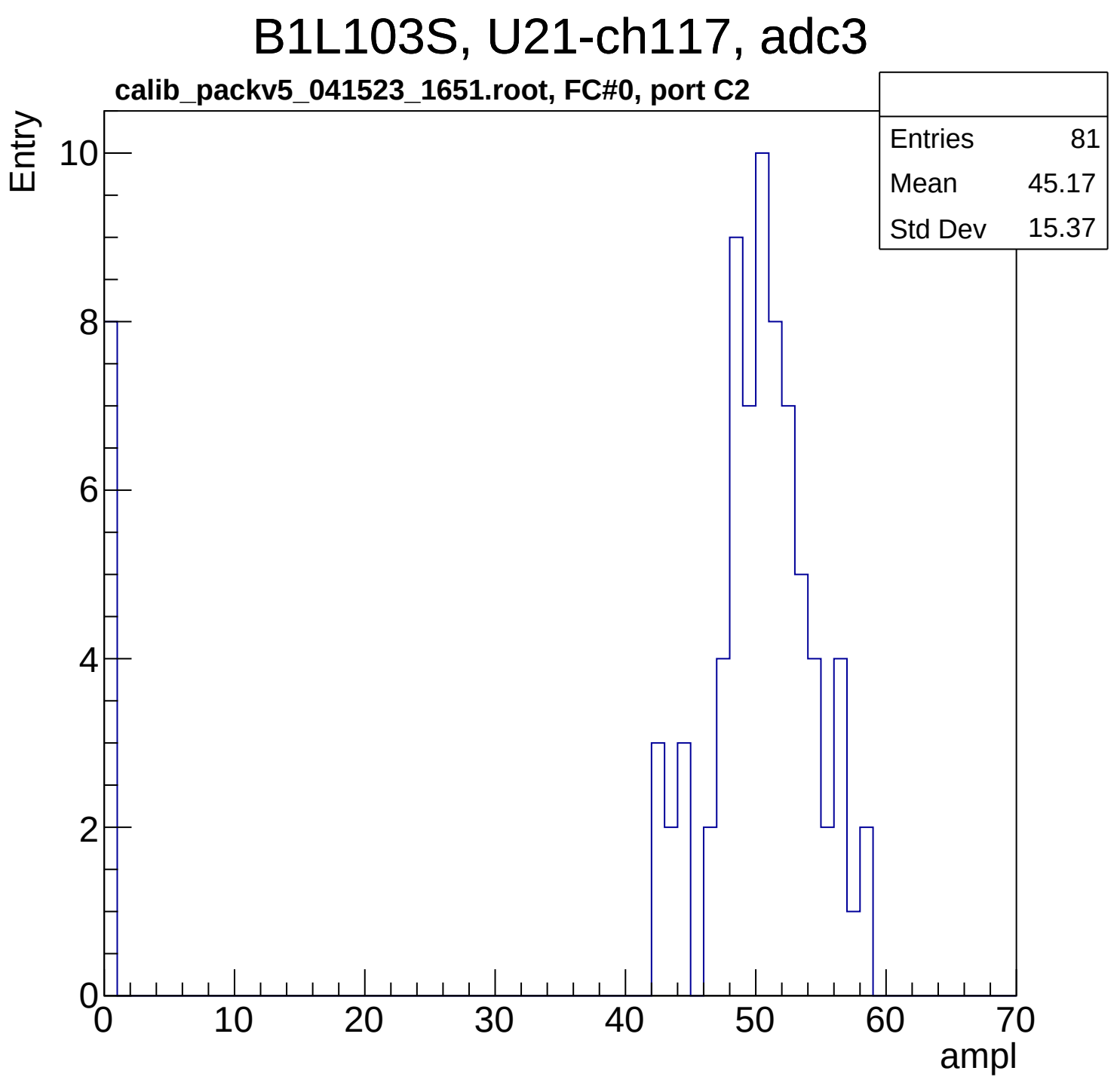
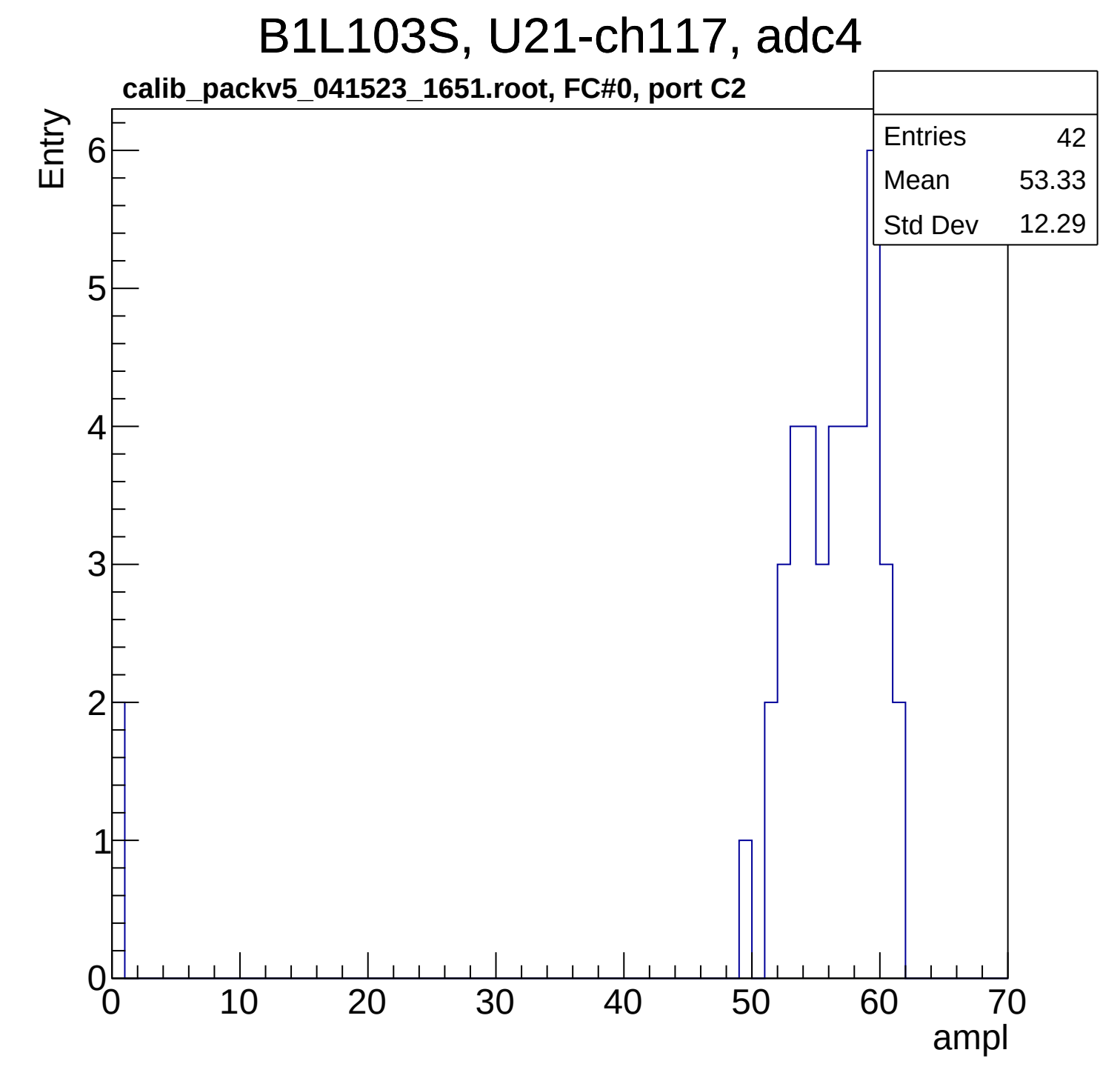

B1L103S, U21-ch117, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 45.17
Std Dev 15.37
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U21-ch117, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 53.33
Std Dev 12.29
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
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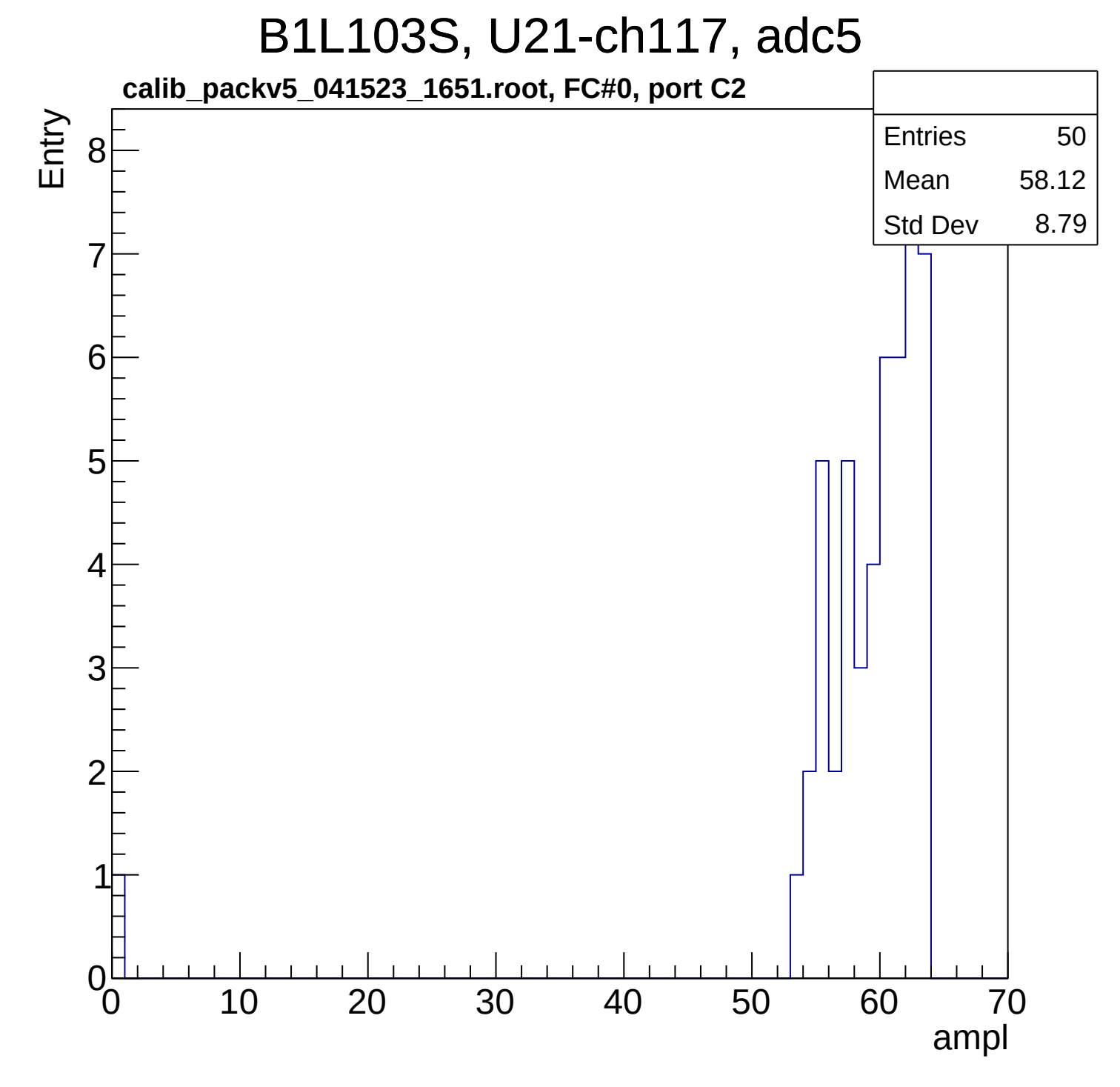
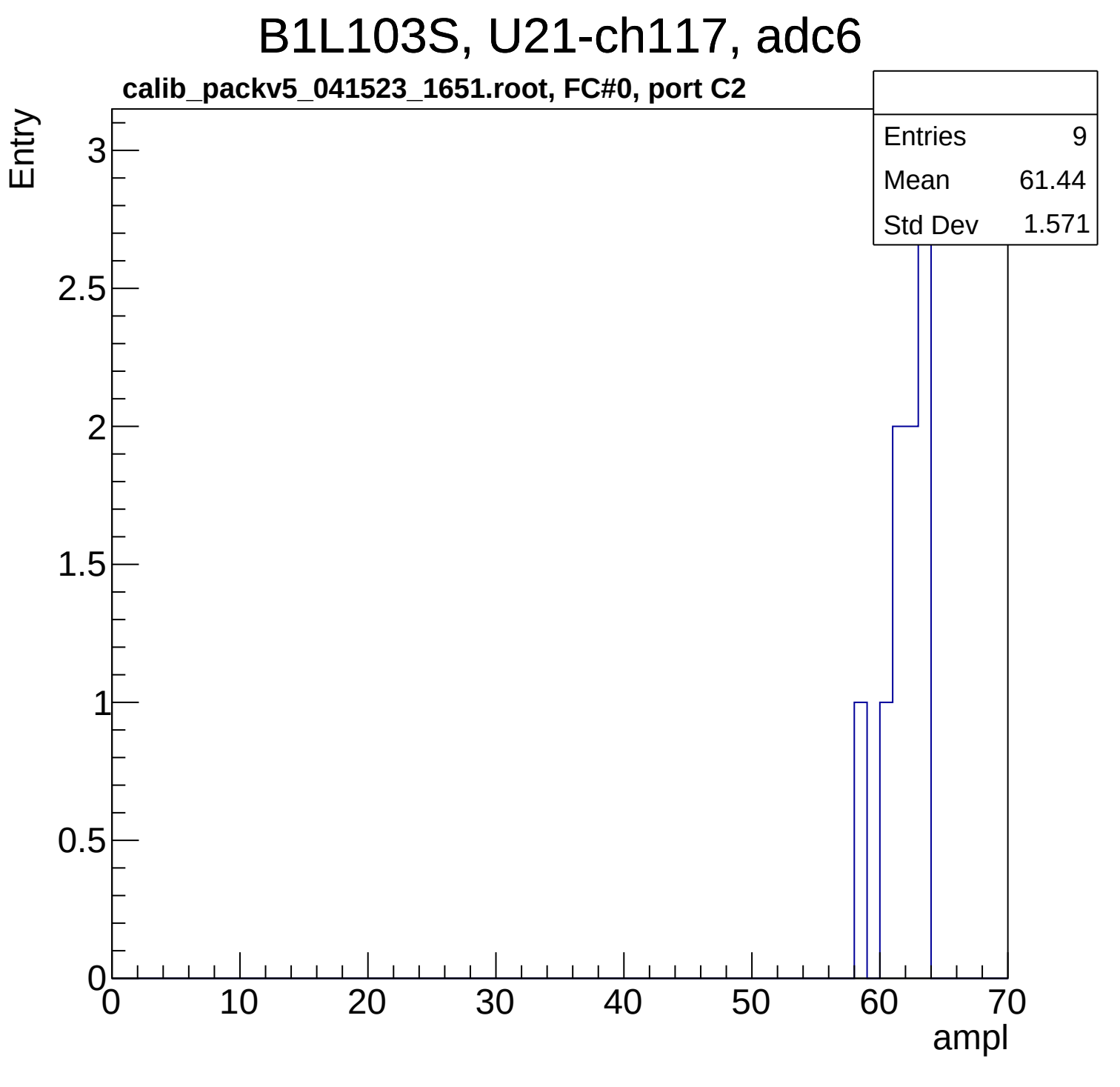

B1L103S, U21-ch117, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 58.12
Std Dev 8.79
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch117, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 61.44
Std Dev 1.571
Entry
ampl
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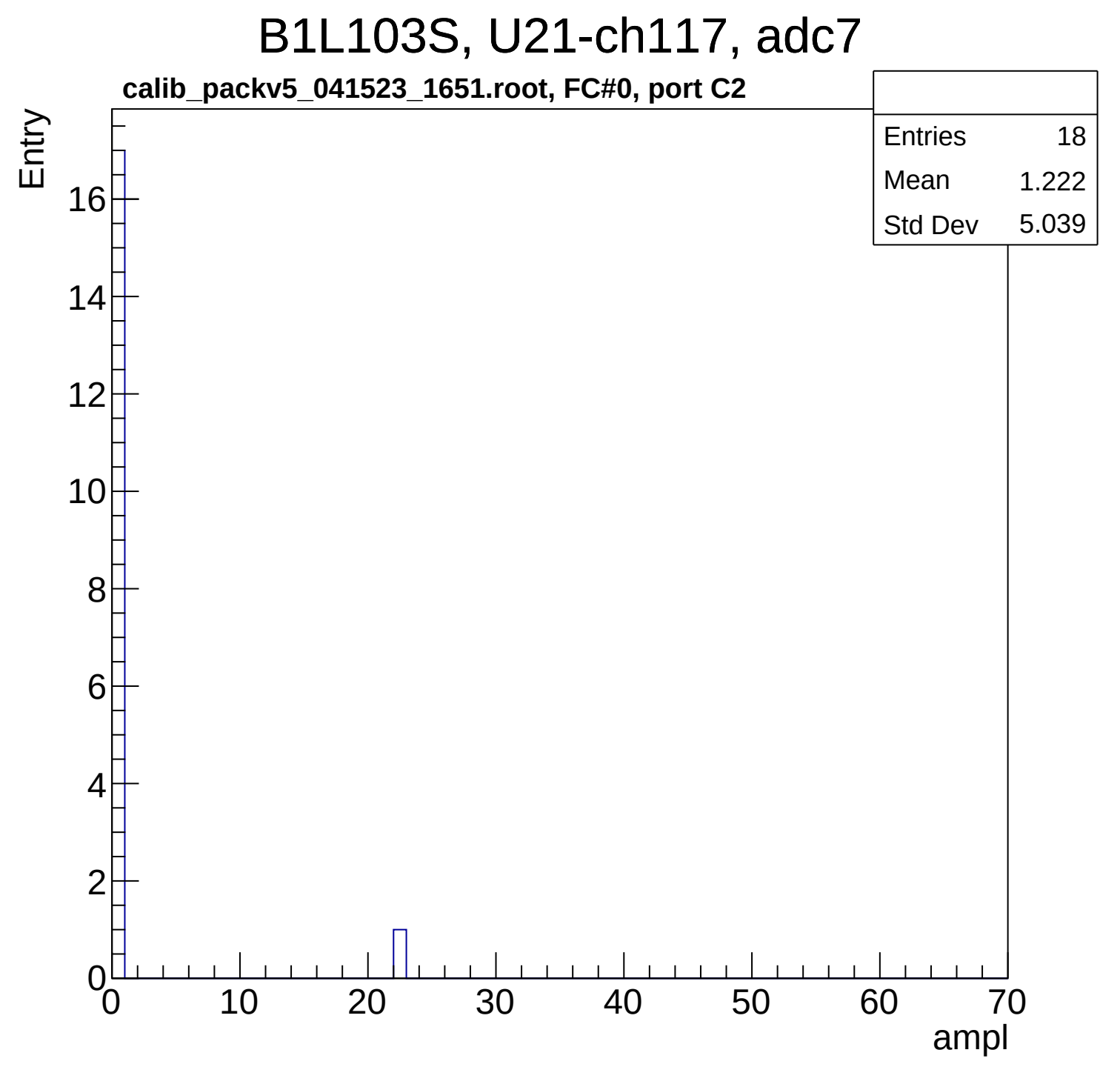
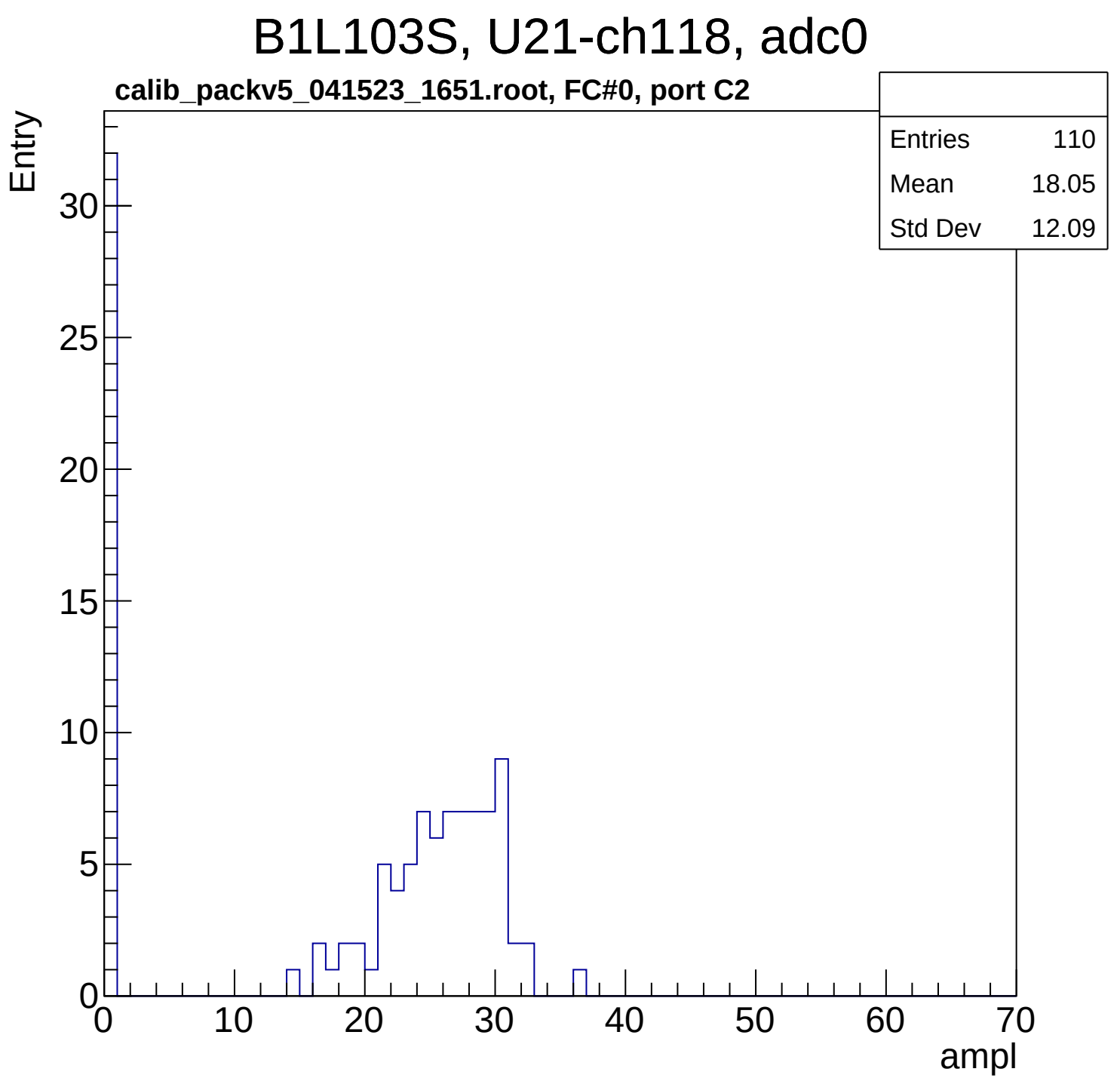
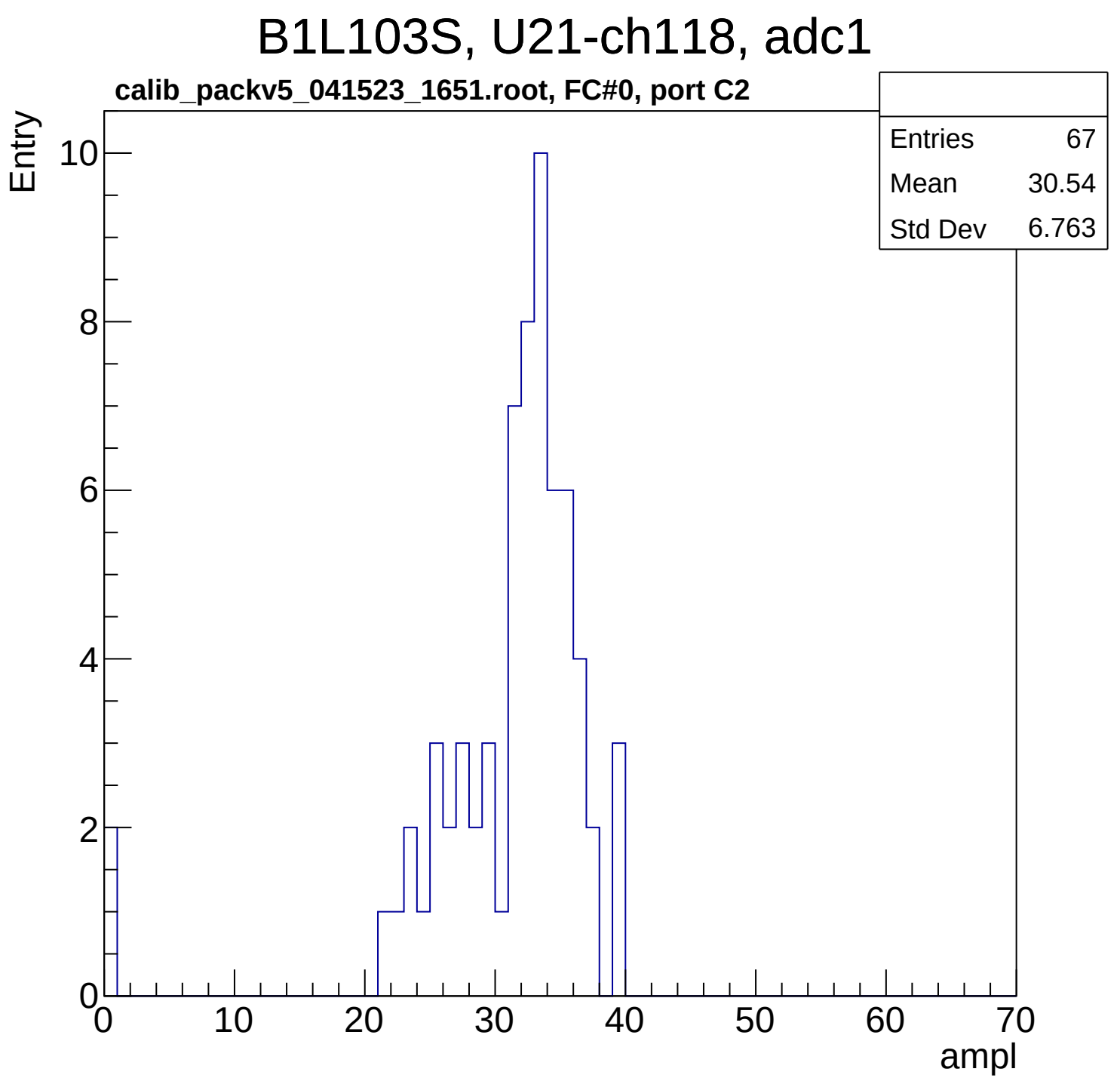
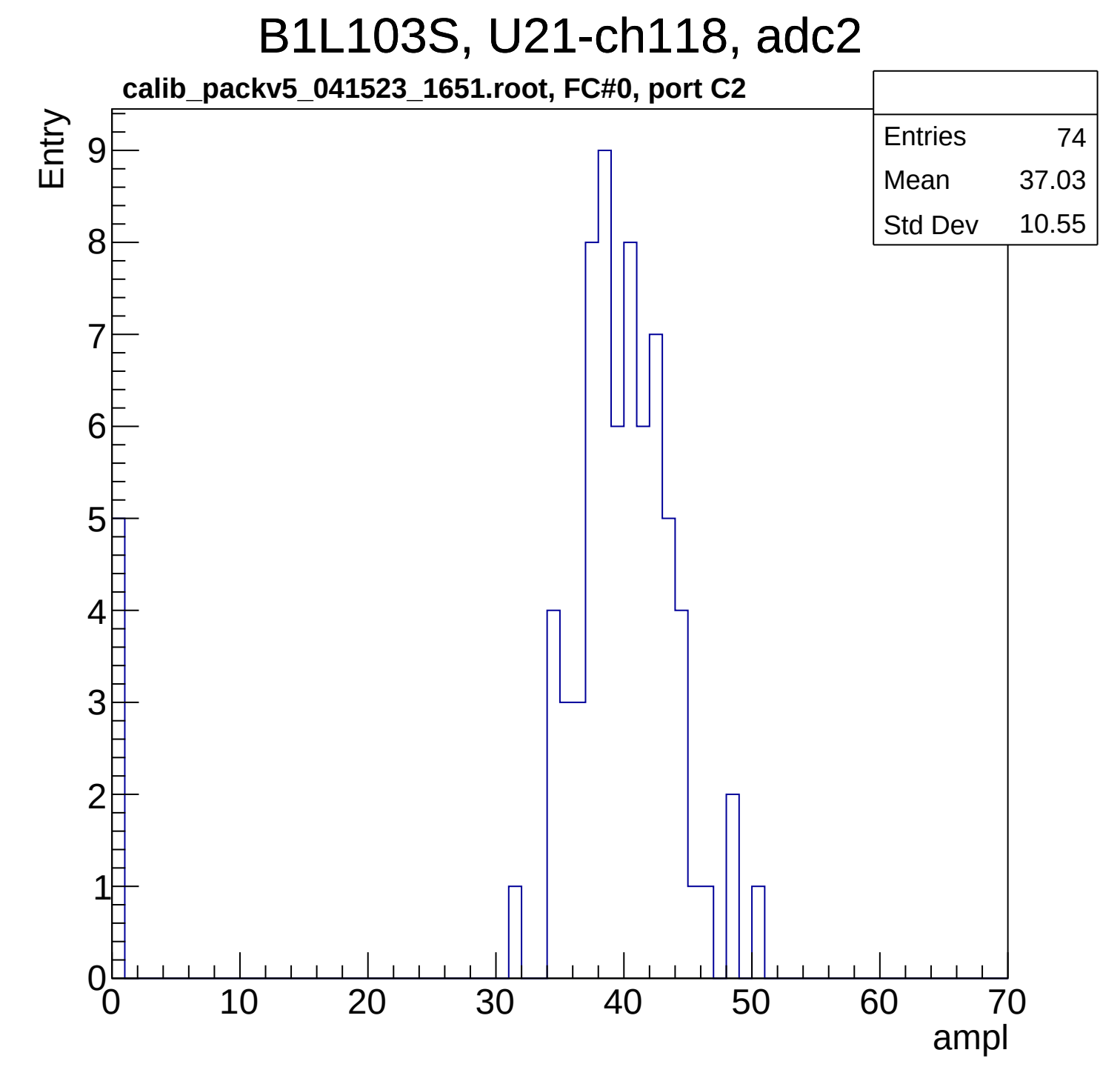
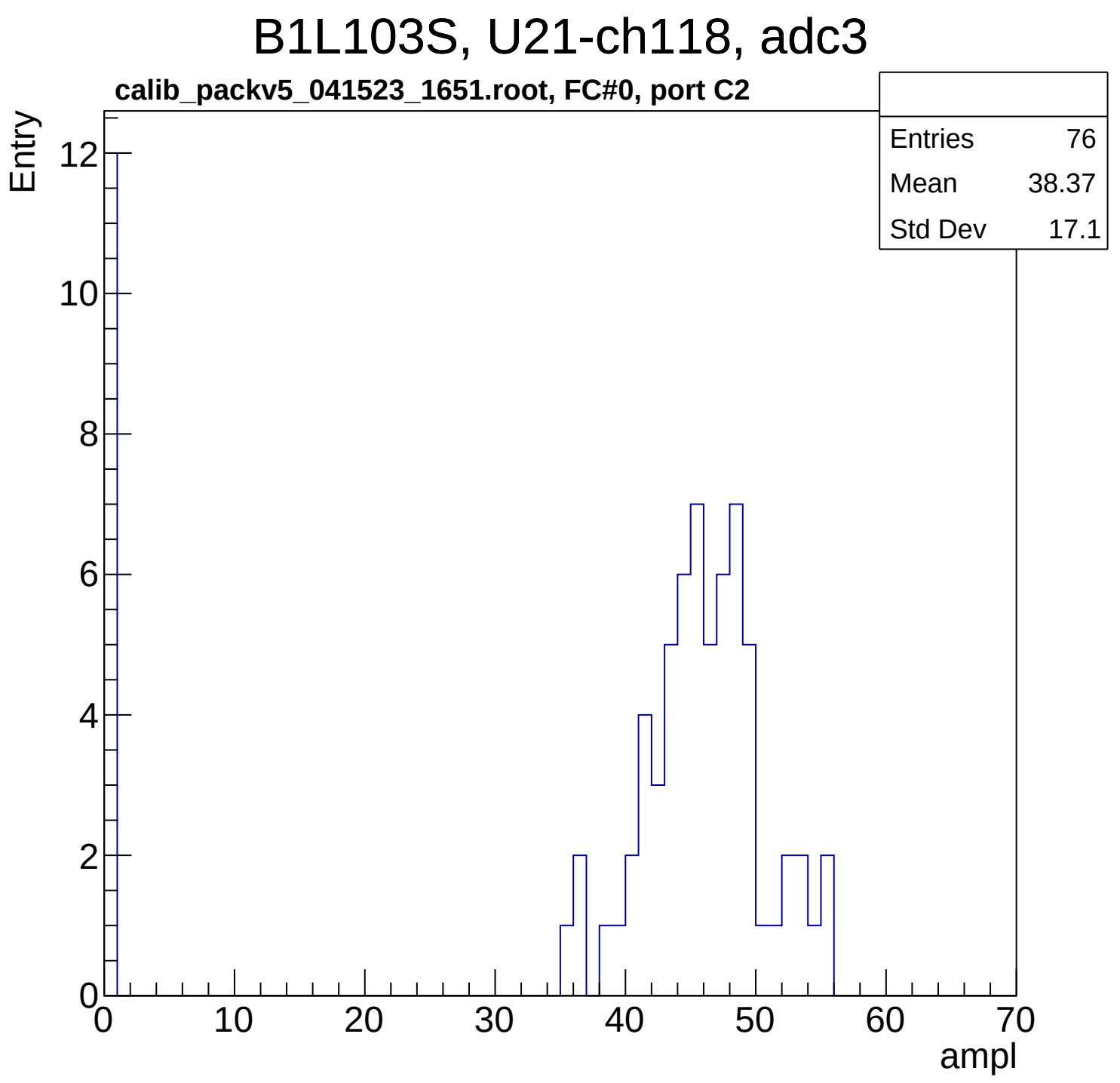
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

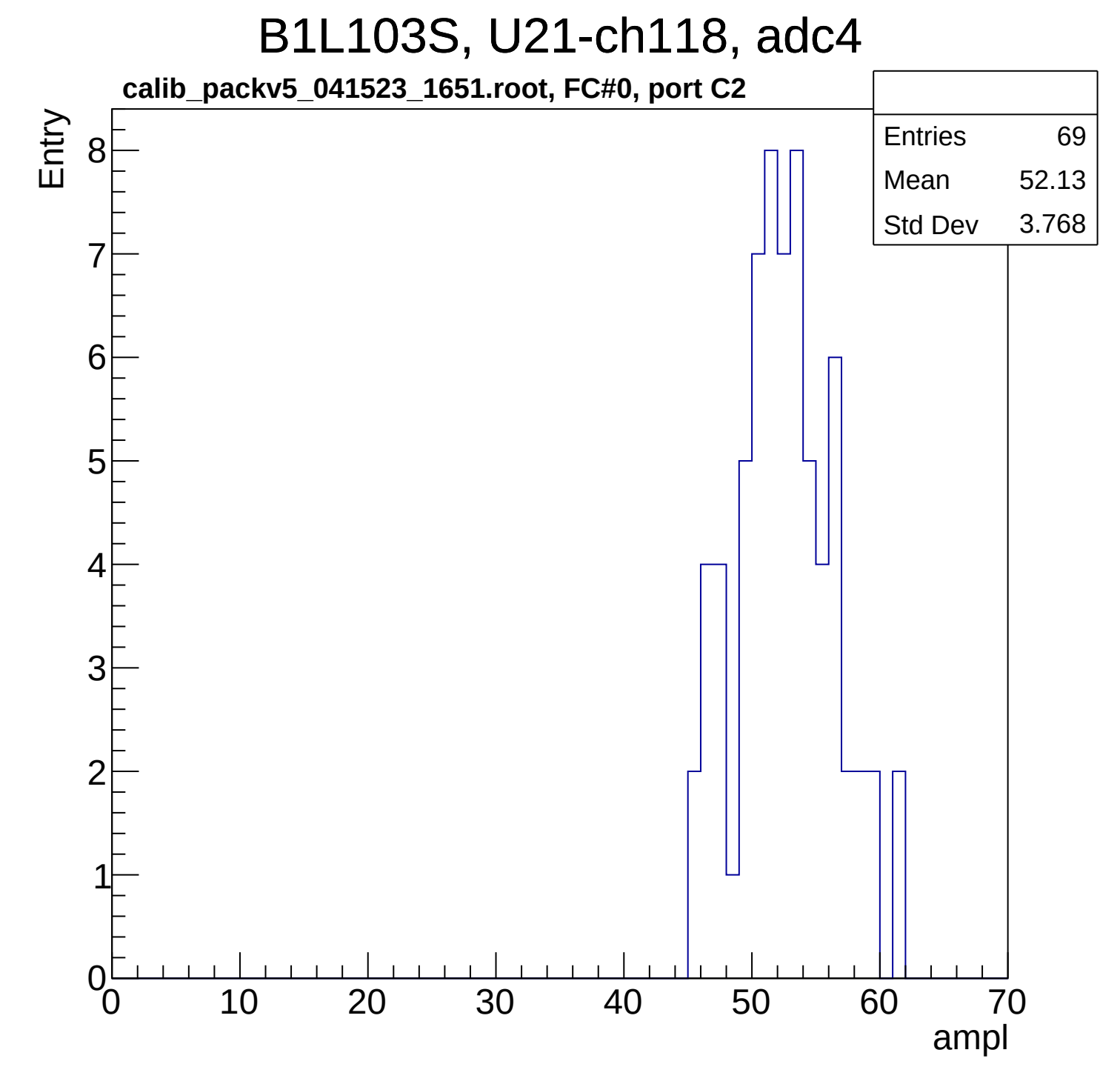

B1L103S, U21-ch117, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.222
Std Dev 5.039
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch118, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 110
Mean 18.05
Std Dev 12.09
Entry
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch118, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 30.54
Std Dev 6.763
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch118, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 37.03
Std Dev 10.55
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch118, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 38.37
Std Dev 17.1
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch118, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 52.13
Std Dev 3.768
Entry
ampl
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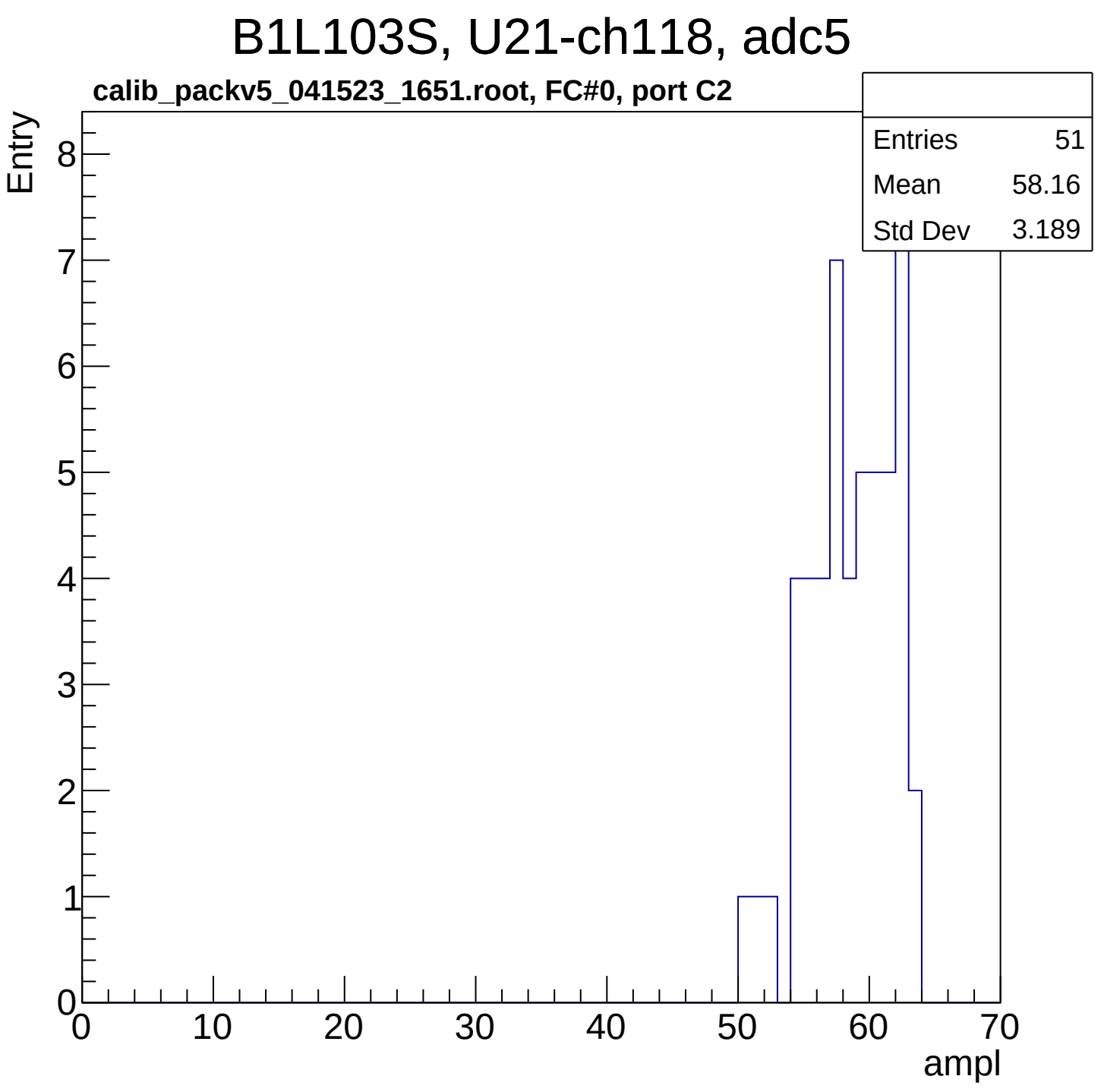
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch118, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 58.16
Std Dev 3.189
Entry
ampl
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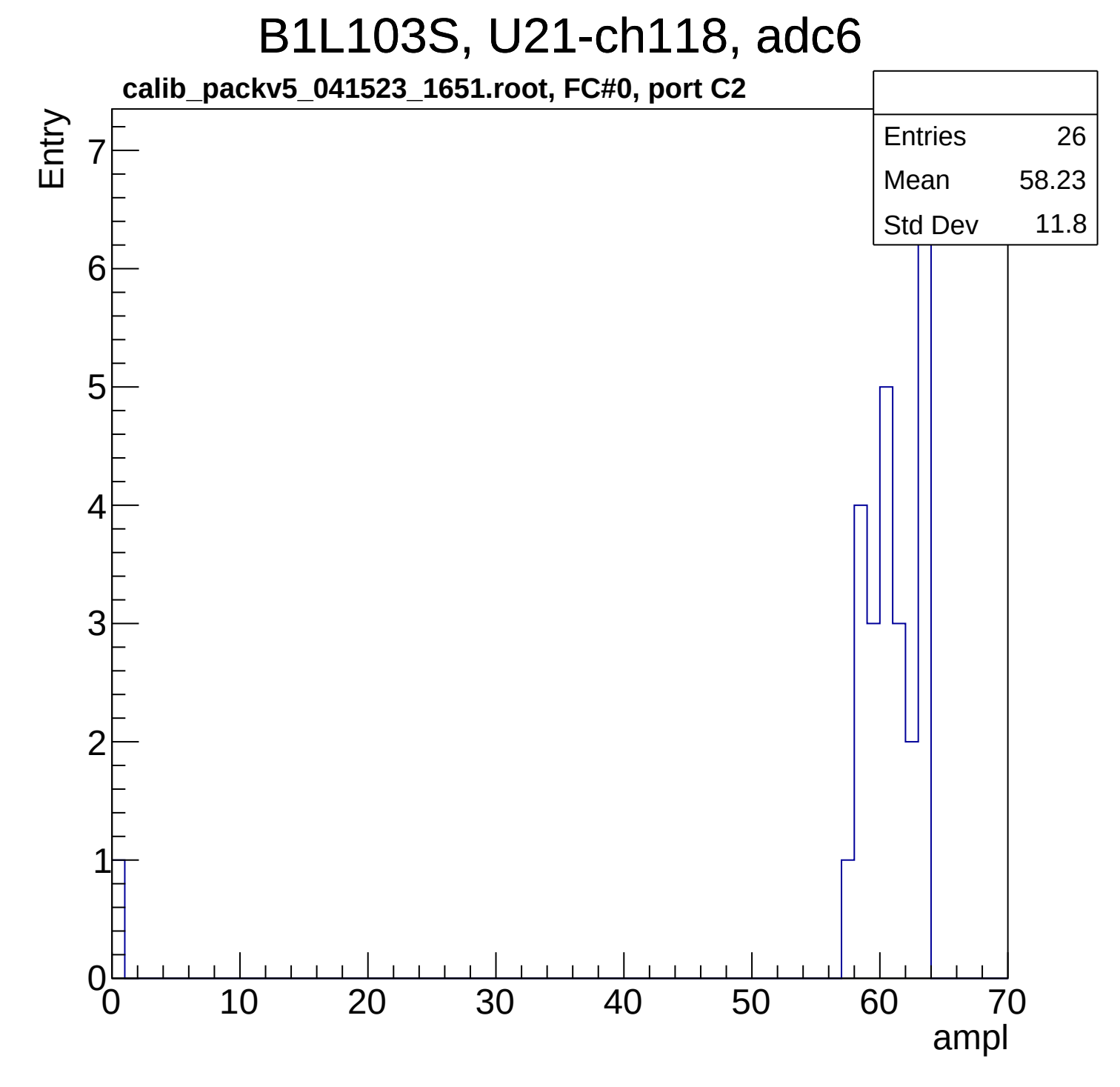
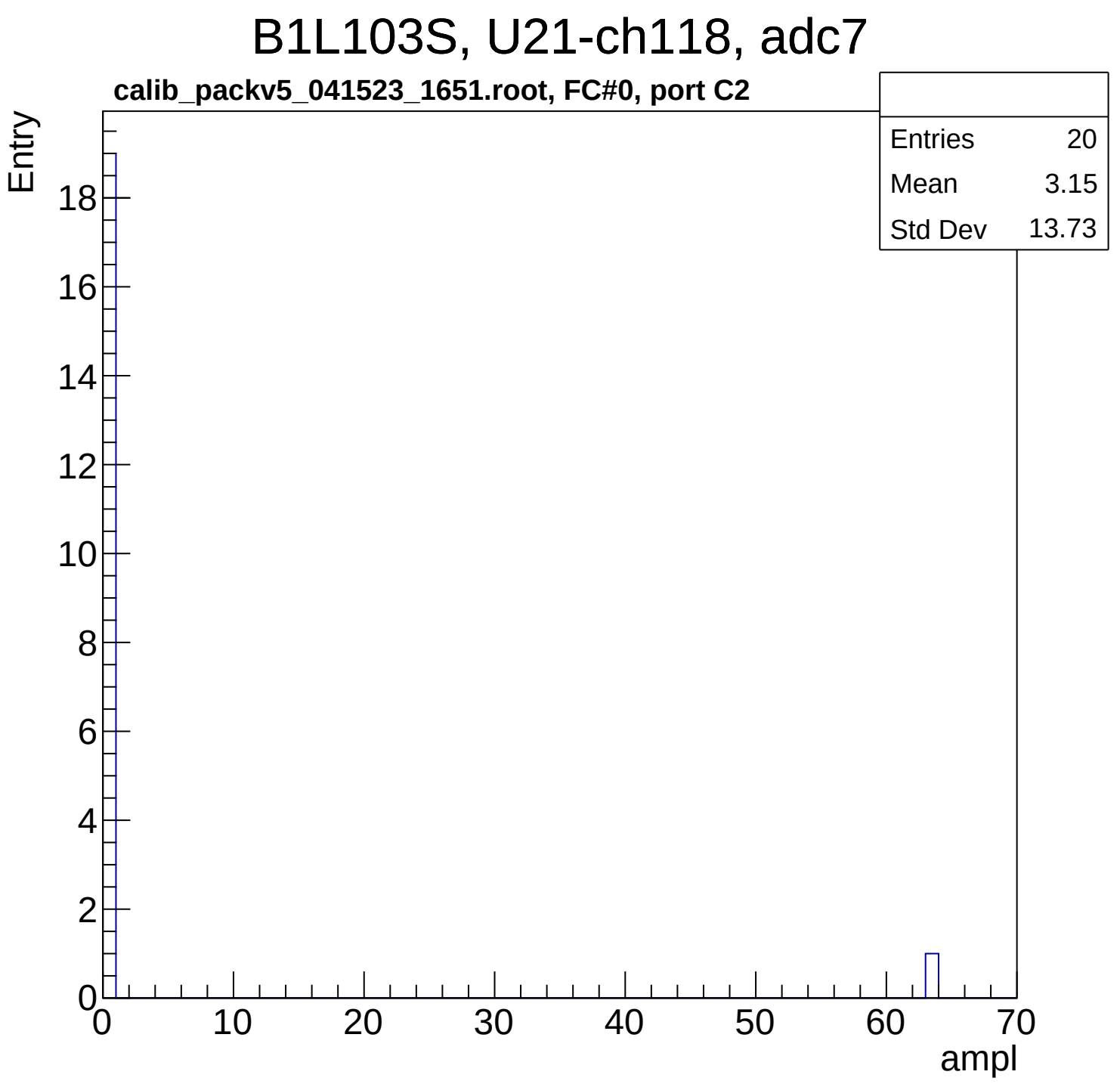
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch118, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 58.23
Std Dev 11.8
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U21-ch118, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
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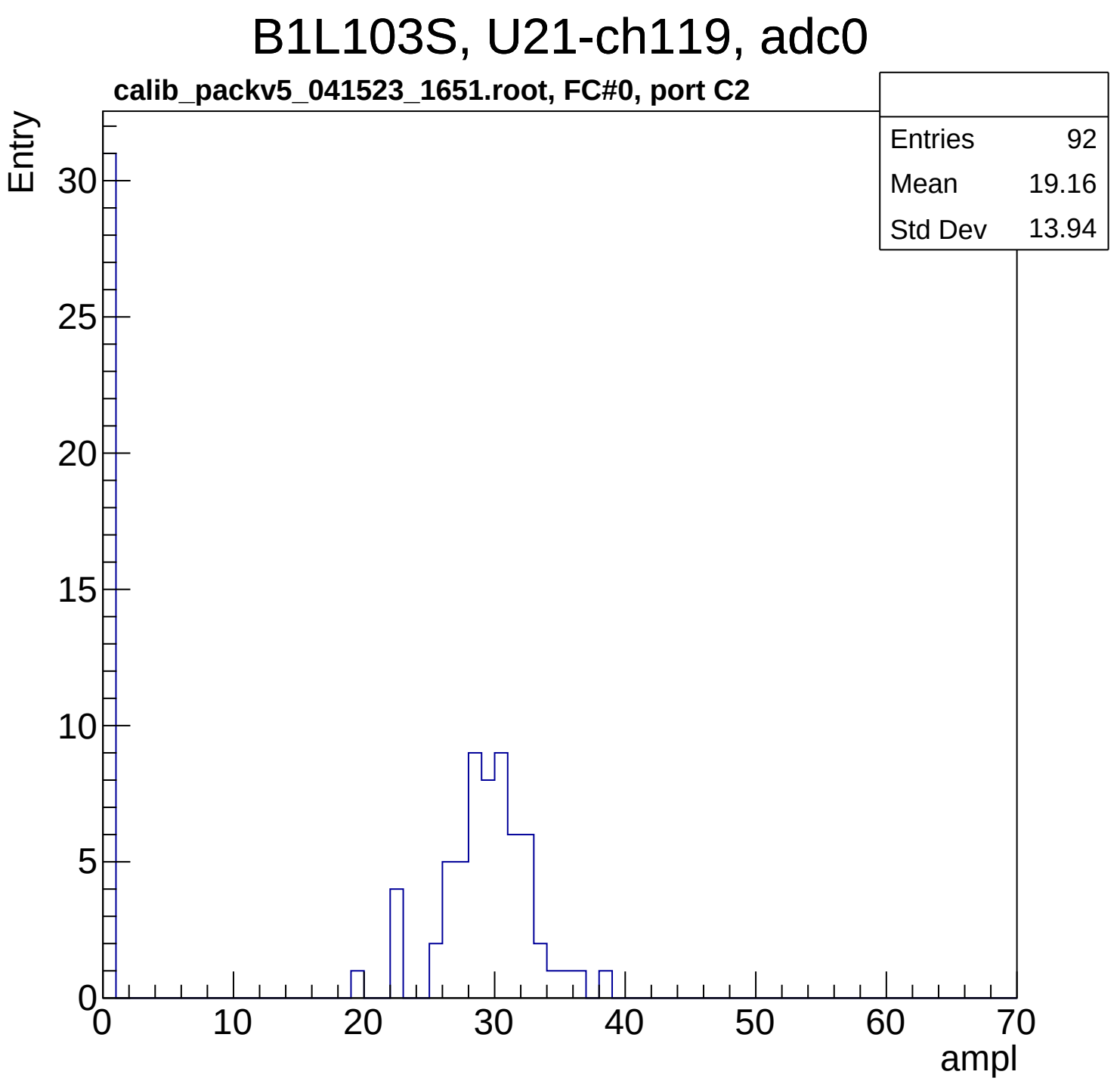
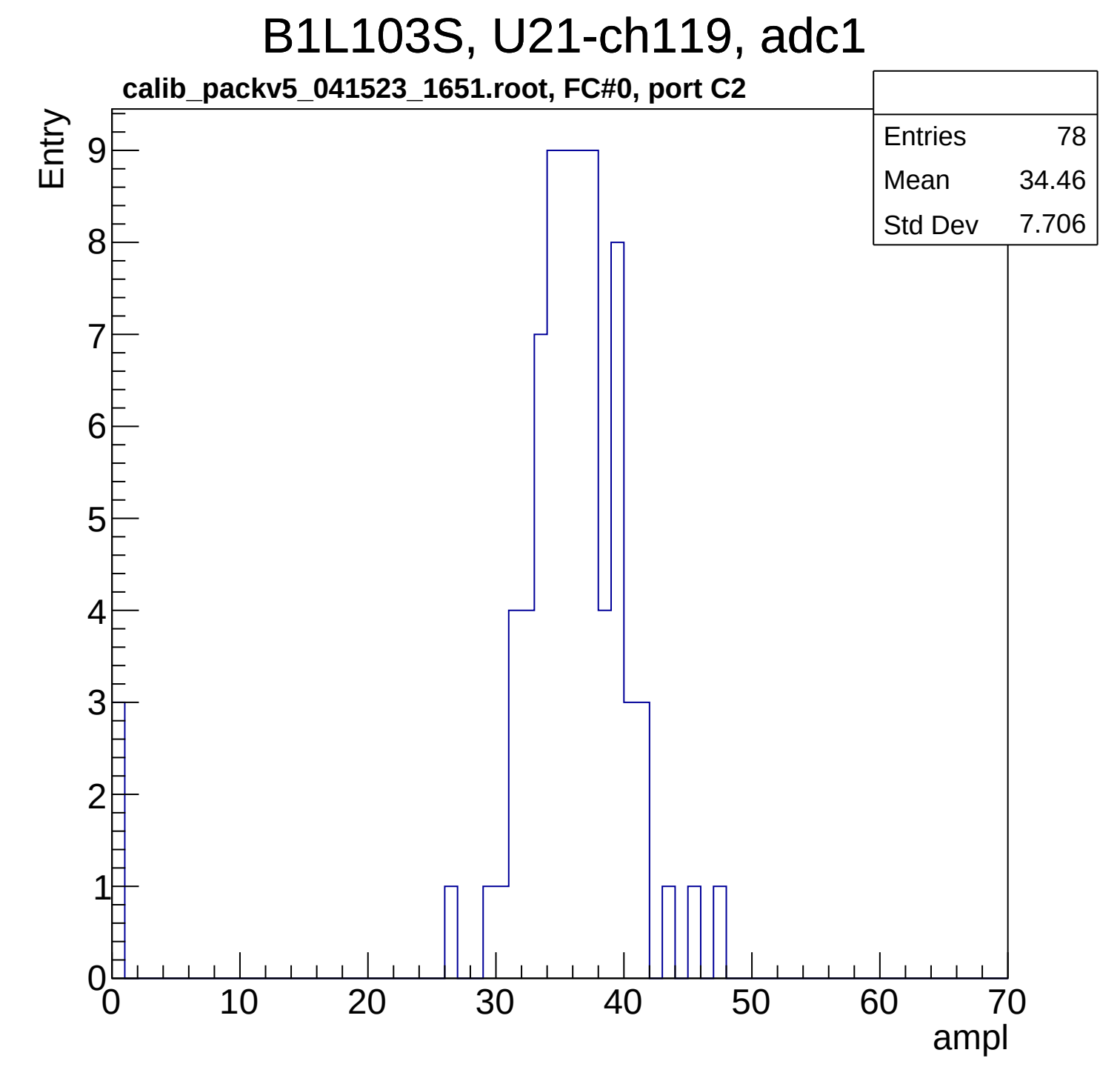
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch119, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 19.16
Std Dev 13.94
Entry
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch119, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 34.46
Std Dev 7.706
Entry
ampl
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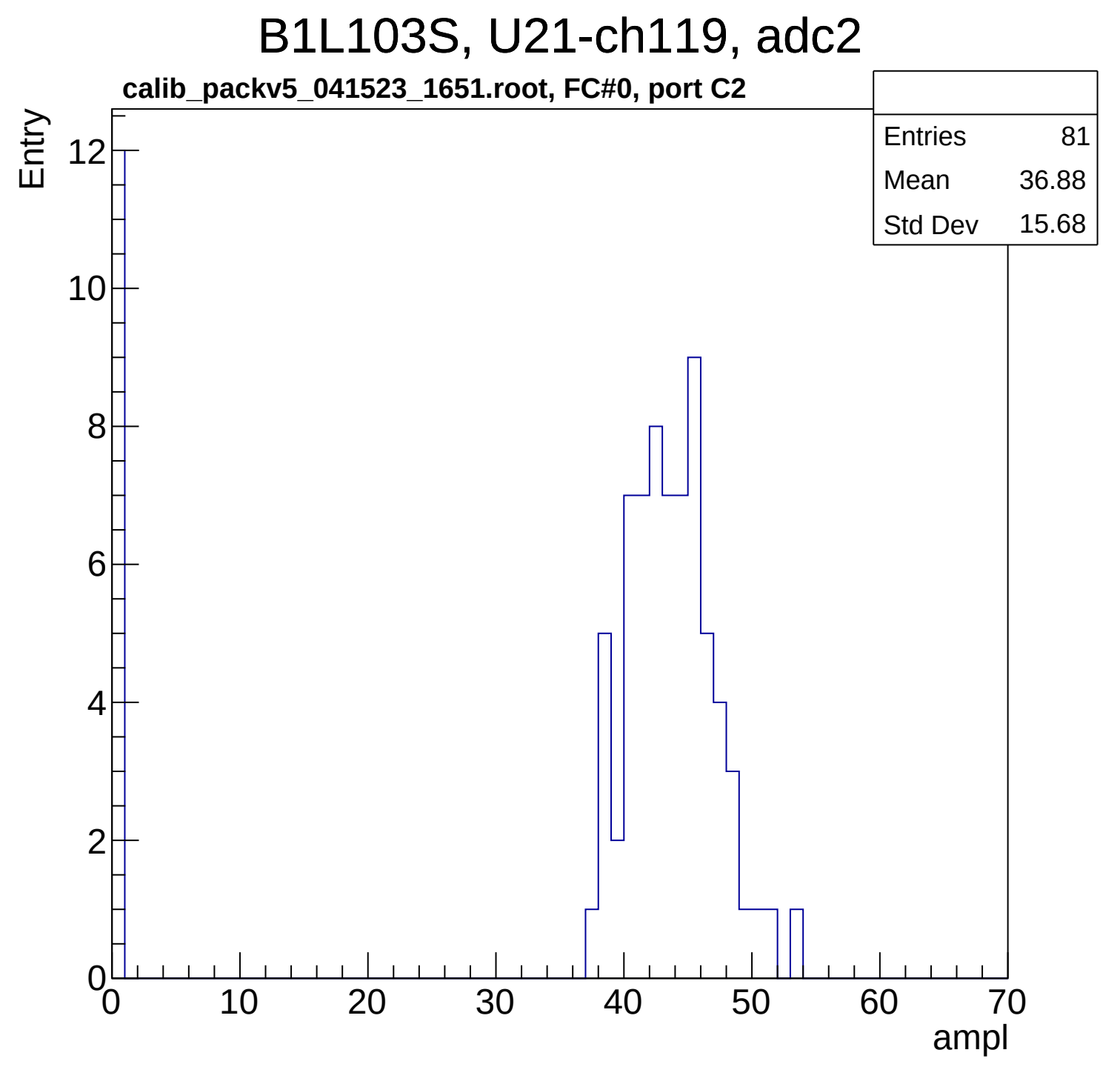
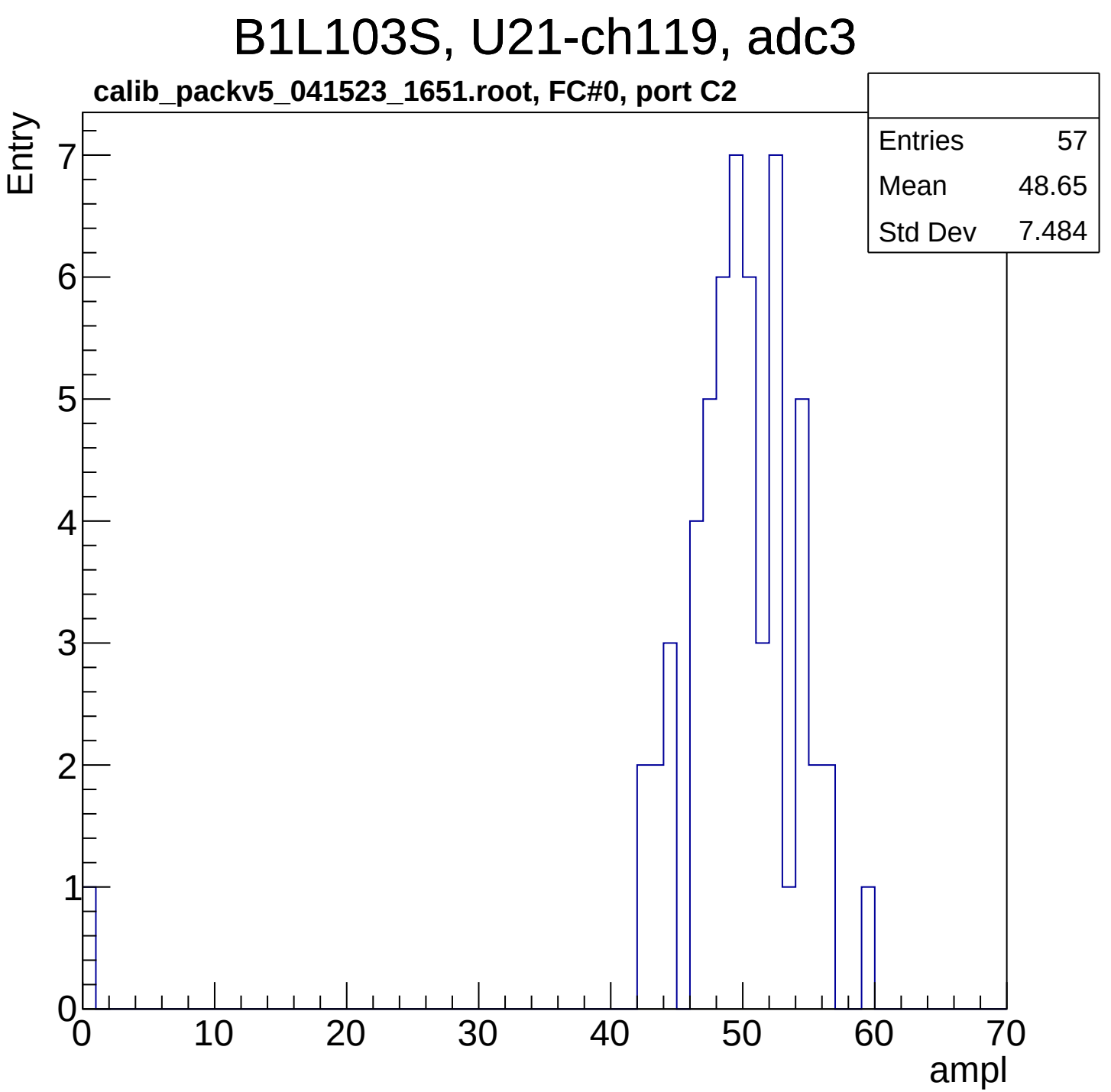
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch119, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 36.88
Std Dev 15.68
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch119, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 48.65
Std Dev 7.484
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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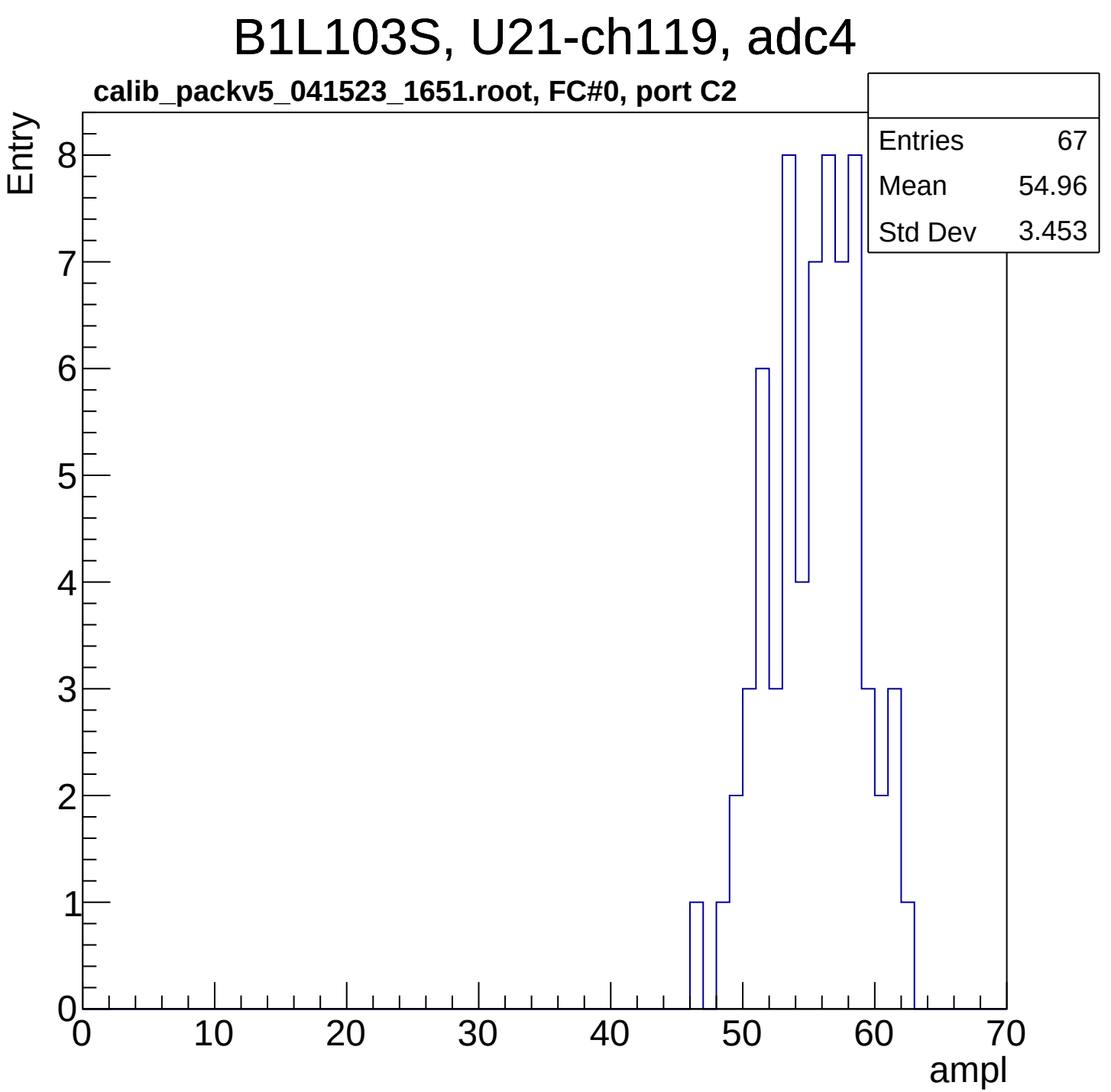
40
50
60
70


B1L103S, U21-ch119, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 54.96
Std Dev 3.453
Entry
ampl
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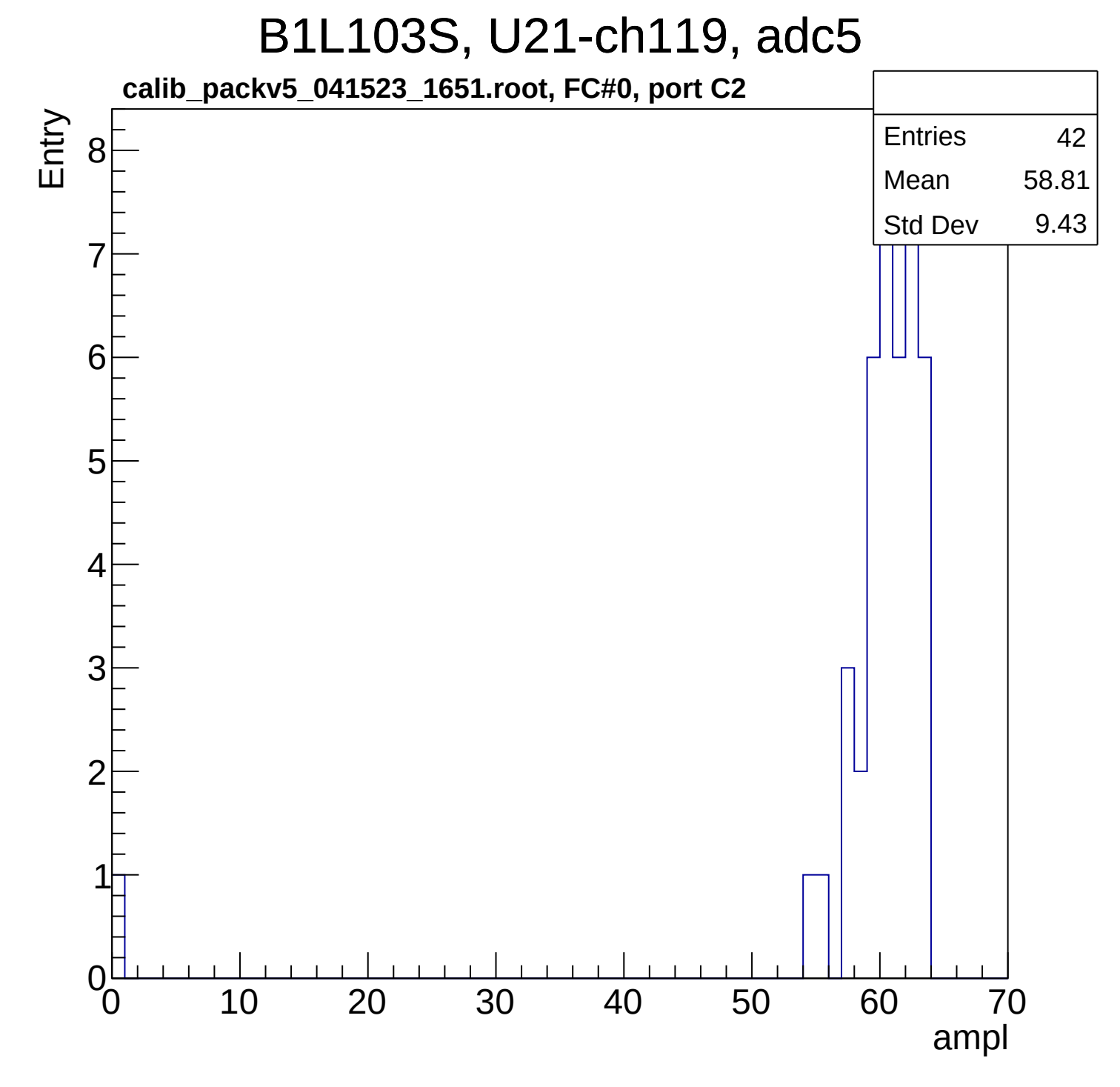
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch119, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 58.81
Std Dev 9.43
Entry
ampl
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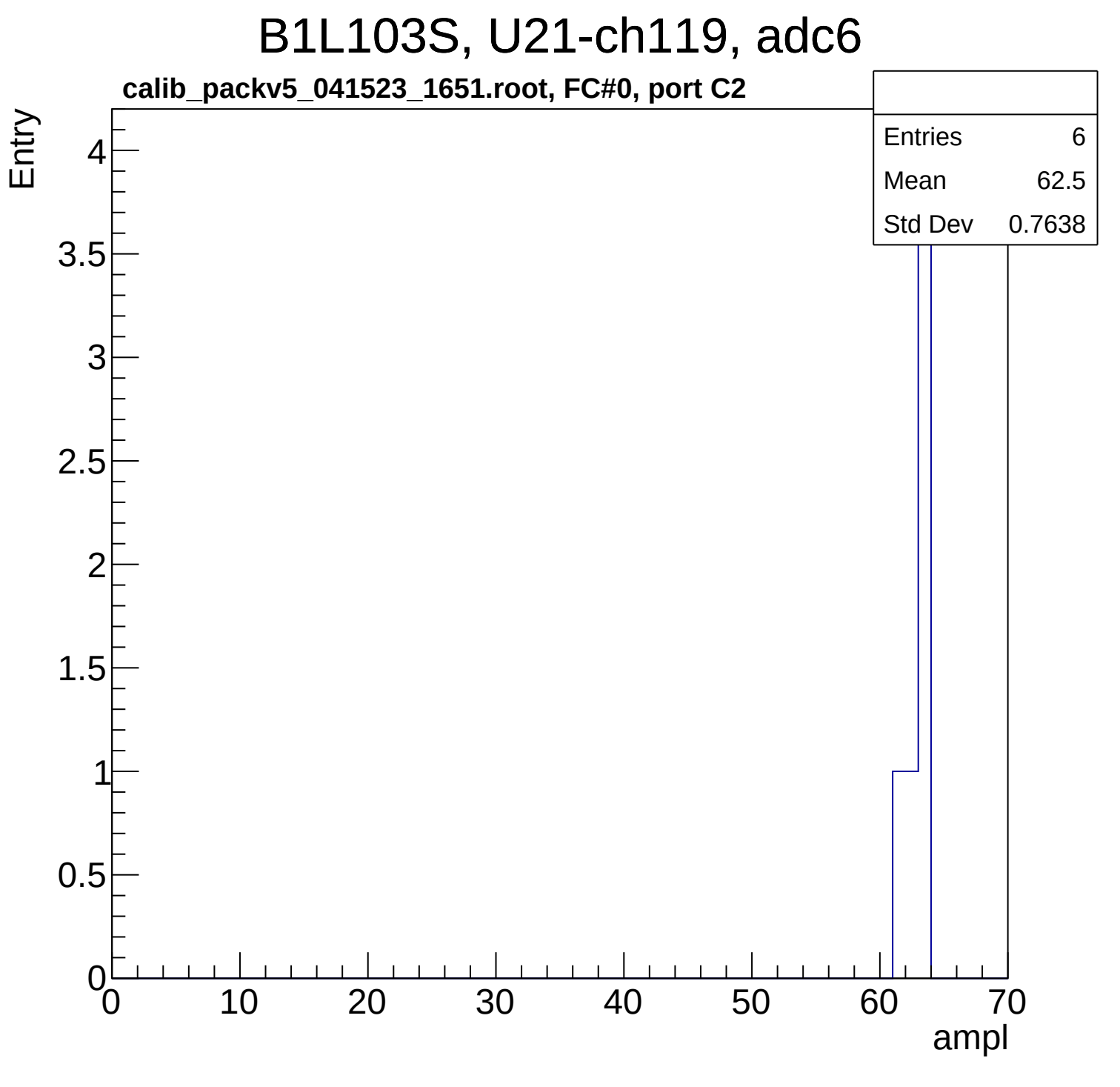
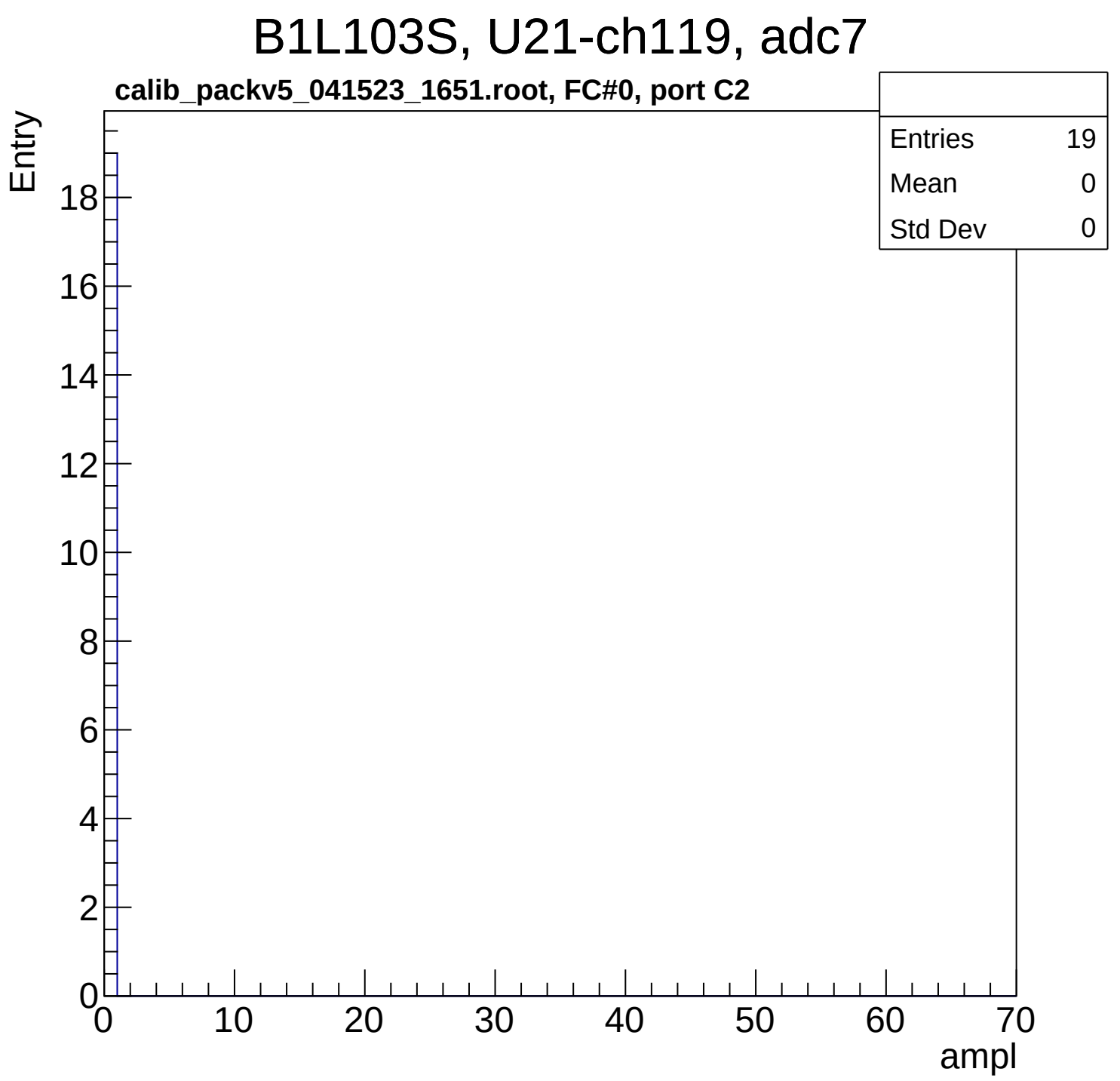
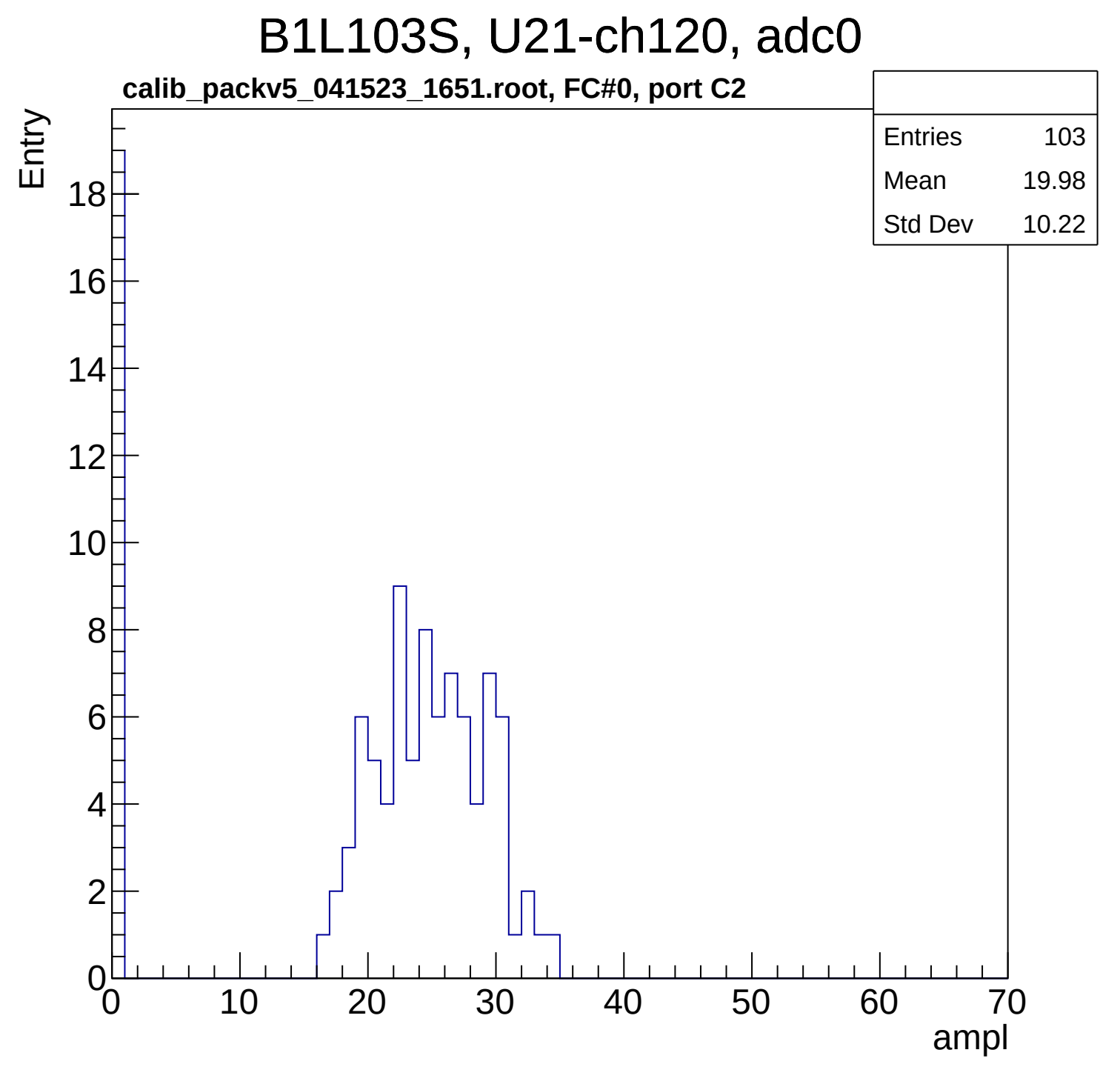
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch119, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 62.5
Std Dev 0.7638
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U21-ch119, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch120, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 103
Mean 19.98
Std Dev 10.22
Entry
0
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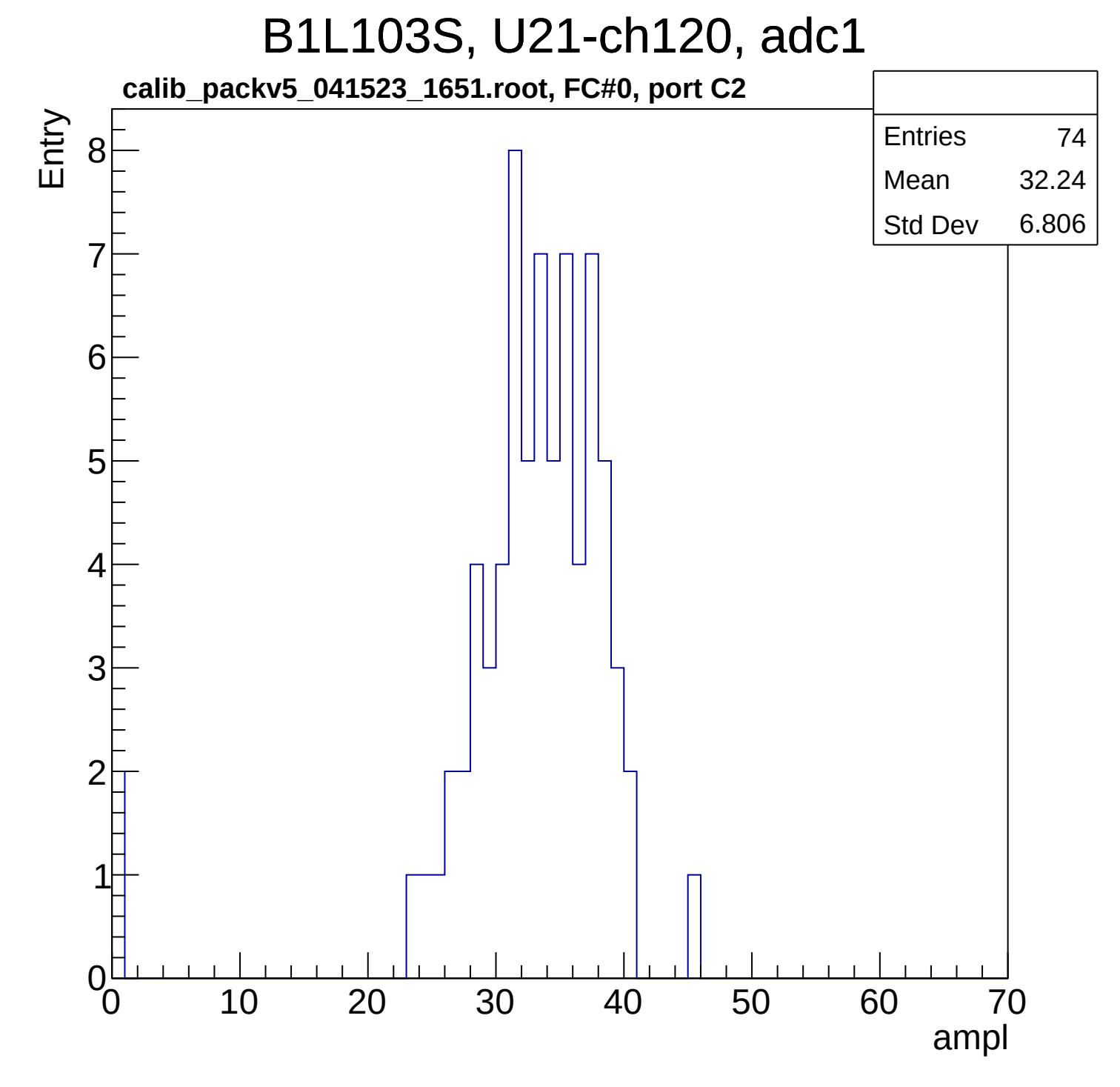
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch120, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 32.24
Std Dev 6.806
Entry
ampl
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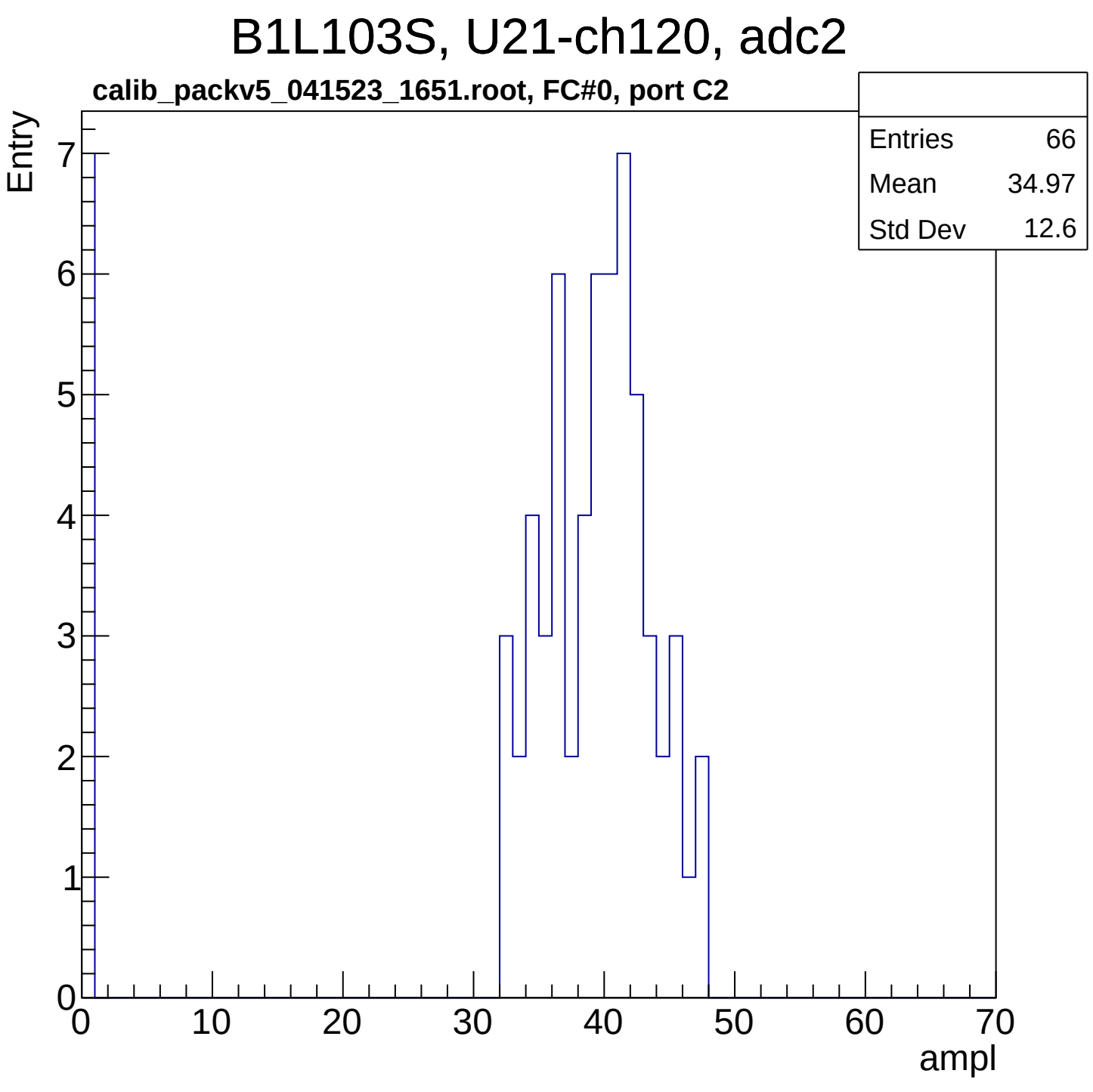
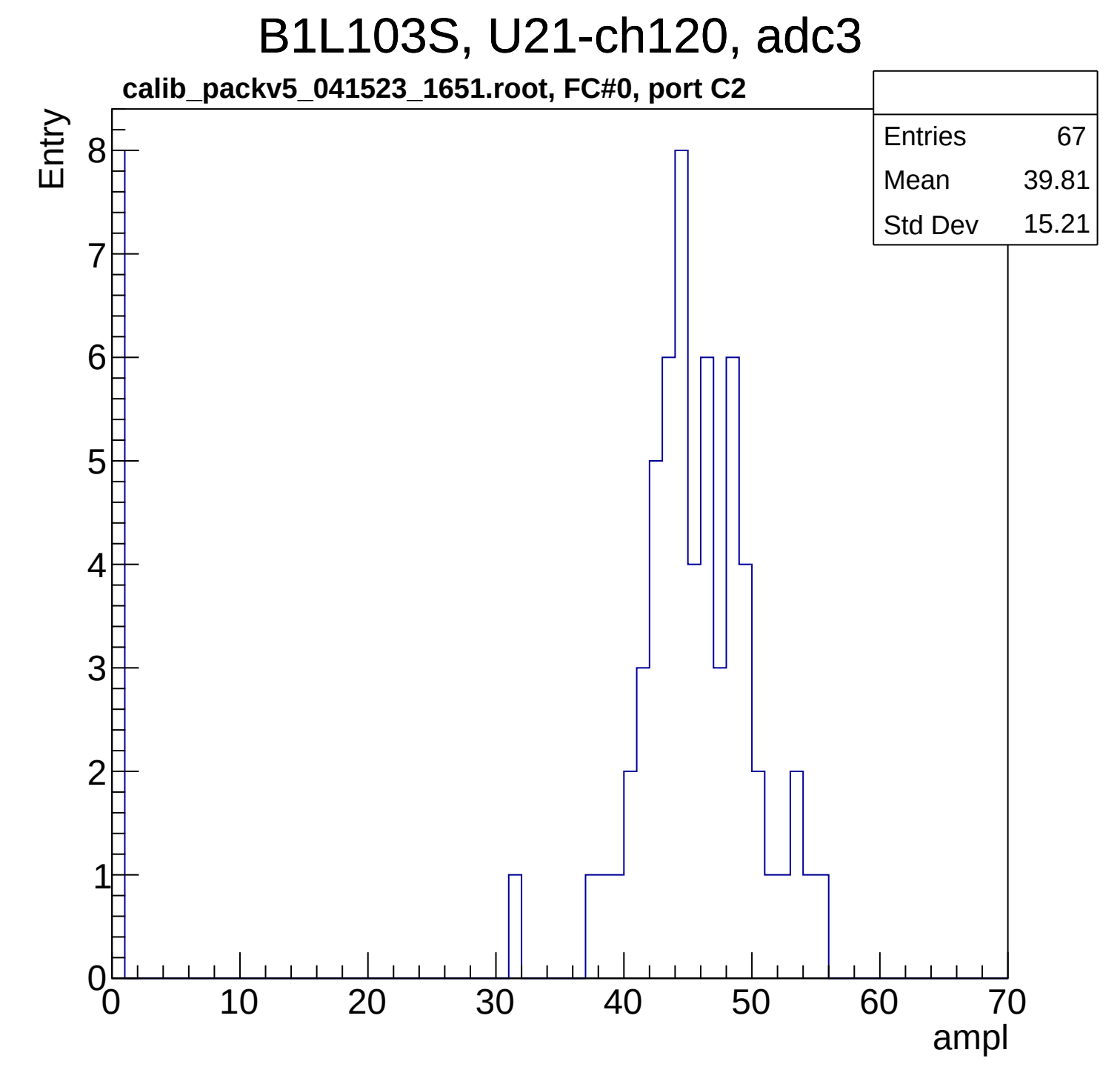
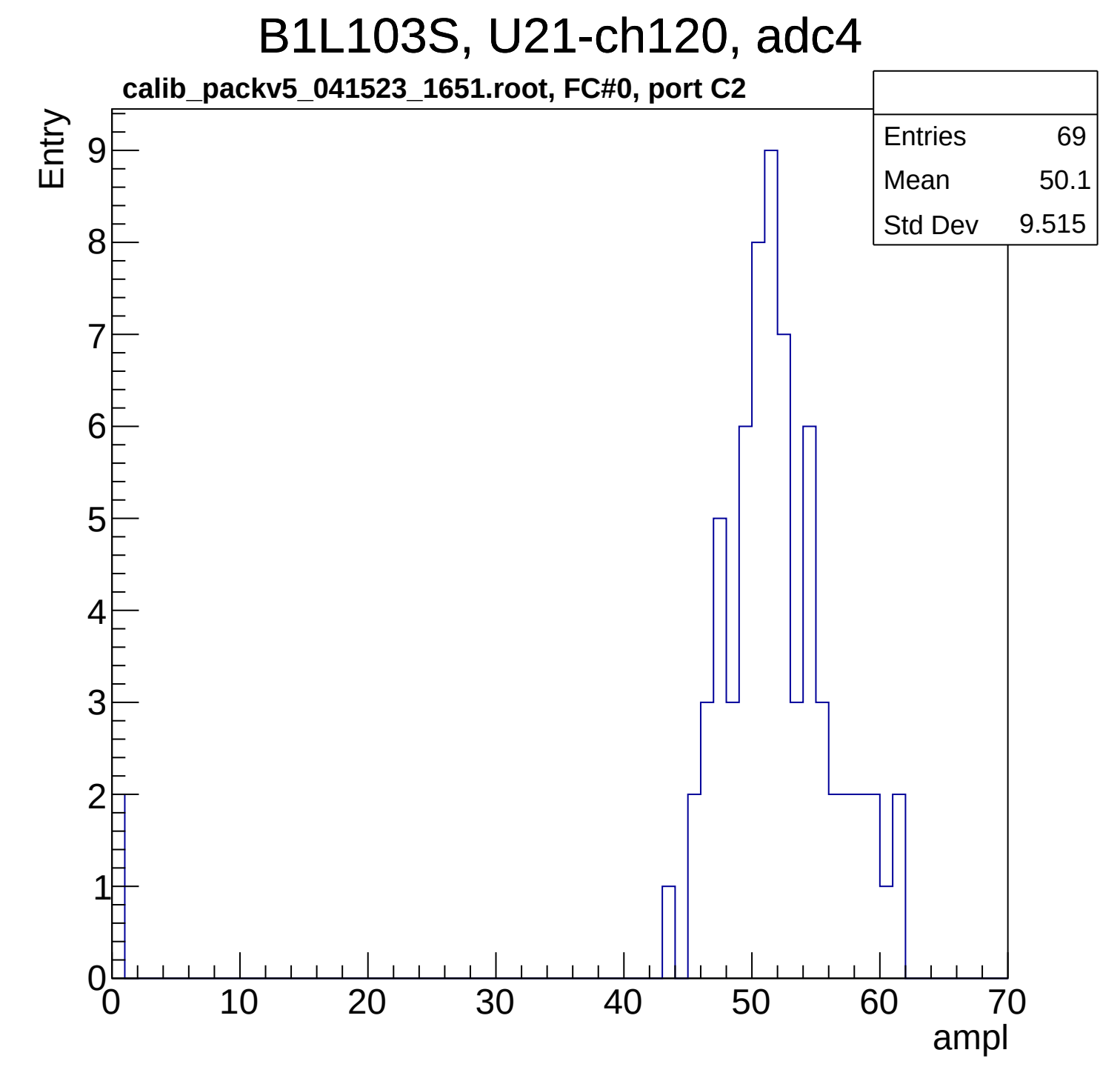
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch120, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 34.97
Std Dev 12.6
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U21-ch120, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 39.81
Std Dev 15.21
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch120, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 50.1
Std Dev 9.515
Entry
ampl
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2
3
4
5
6
7
8
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0
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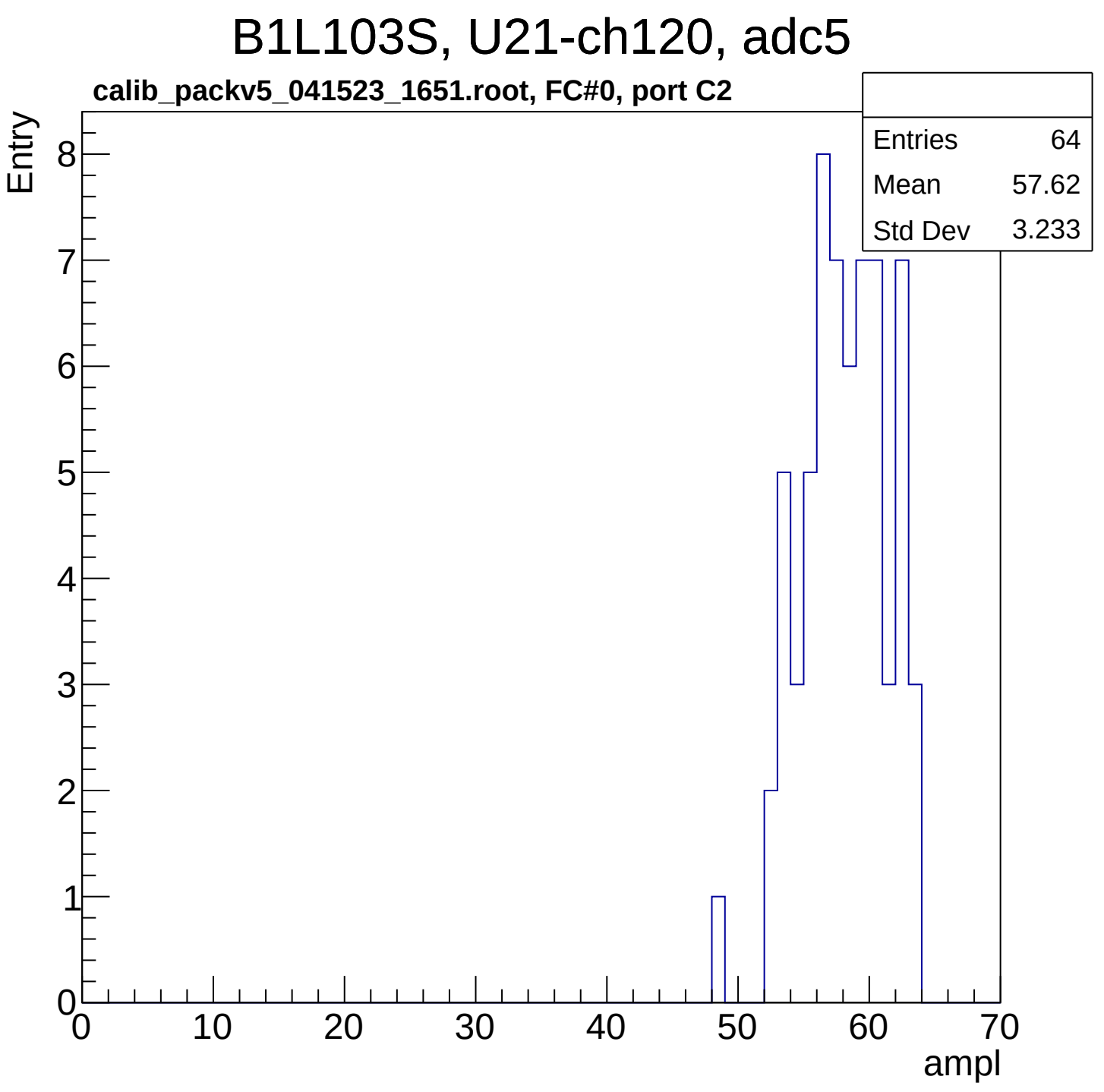
B1L103S, U21-ch120, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 57.62
Std Dev 3.233
Entry
ampl
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2
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4
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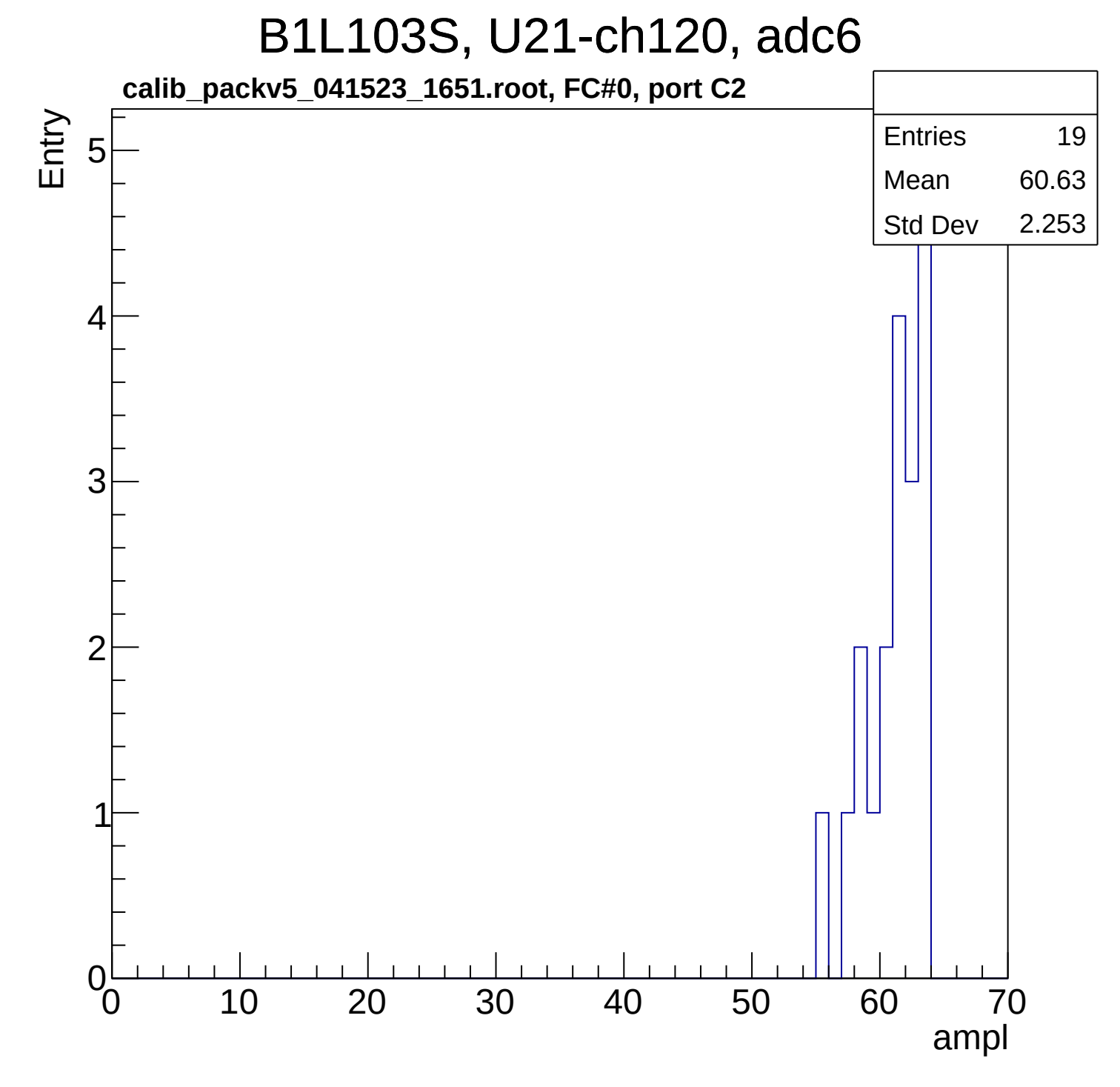
B1L103S, U21-ch120, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 60.63
Std Dev 2.253
Entry
ampl
0
1
2
3
4
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0
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40
50
60
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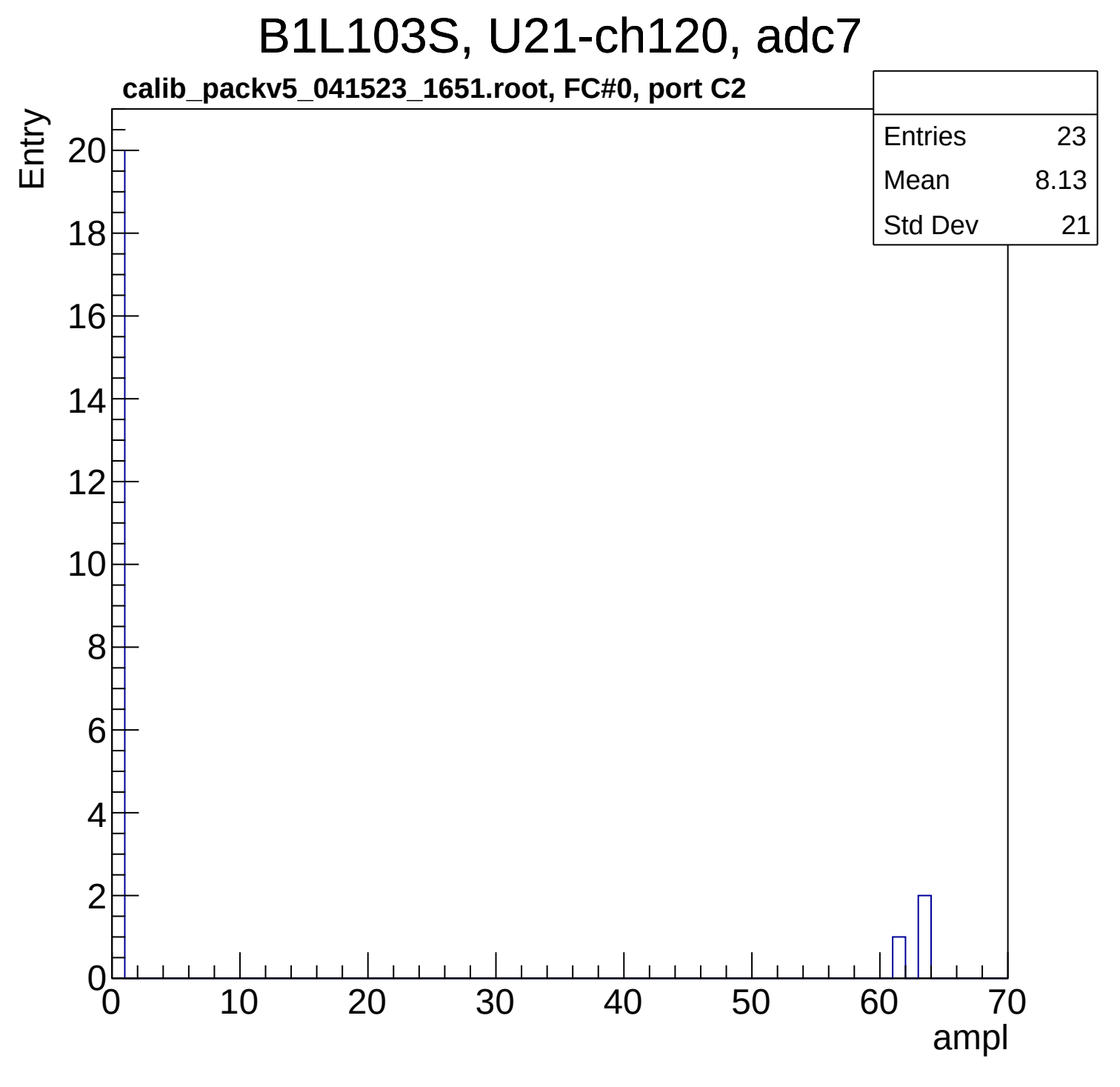
B1L103S, U21-ch120, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 8.13
Std Dev 21
Entry
0
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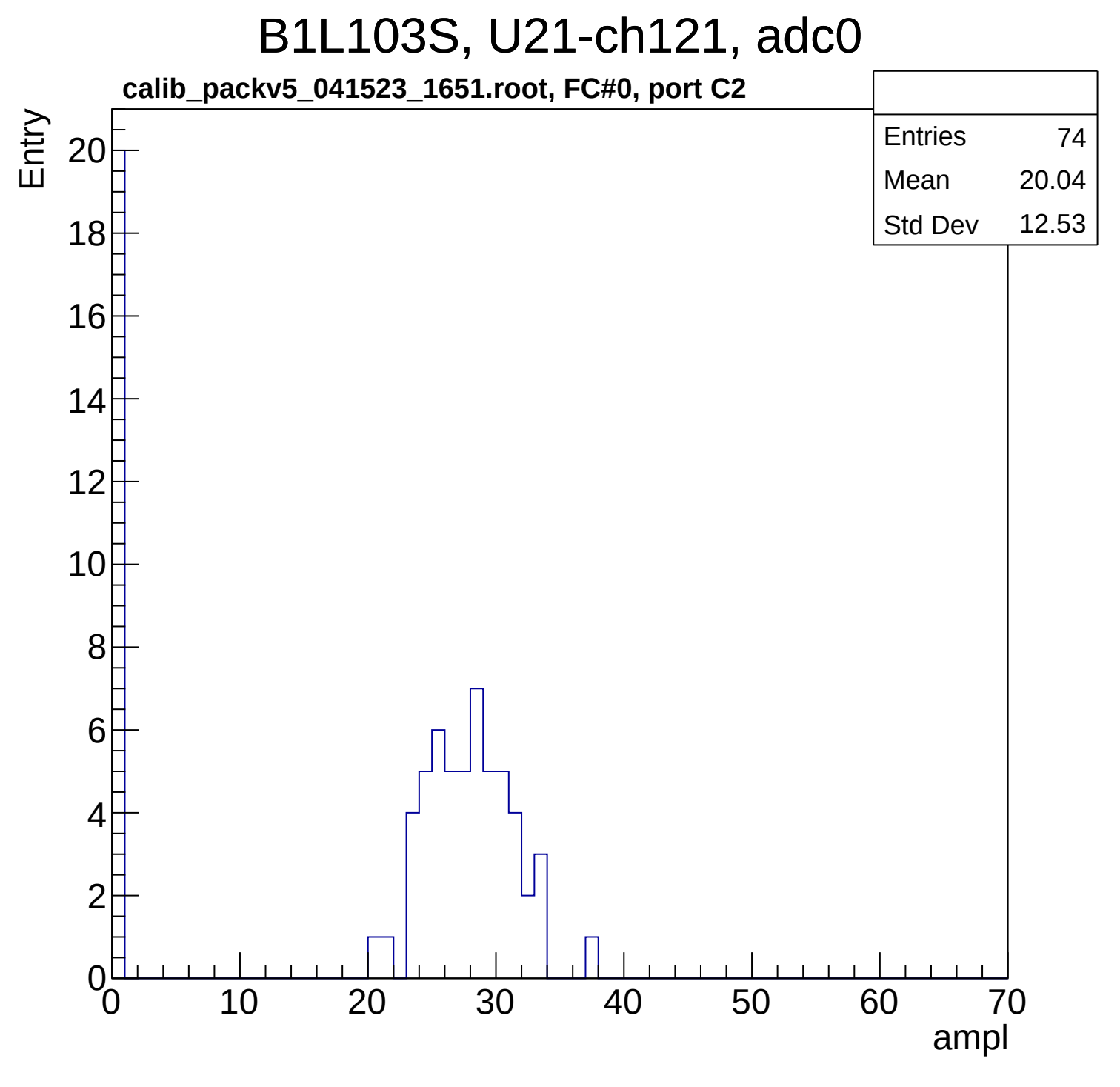
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch121, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 20.04
Std Dev 12.53
Entry
ampl
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6
8
10
12
14
16
18
20
0
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40
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60
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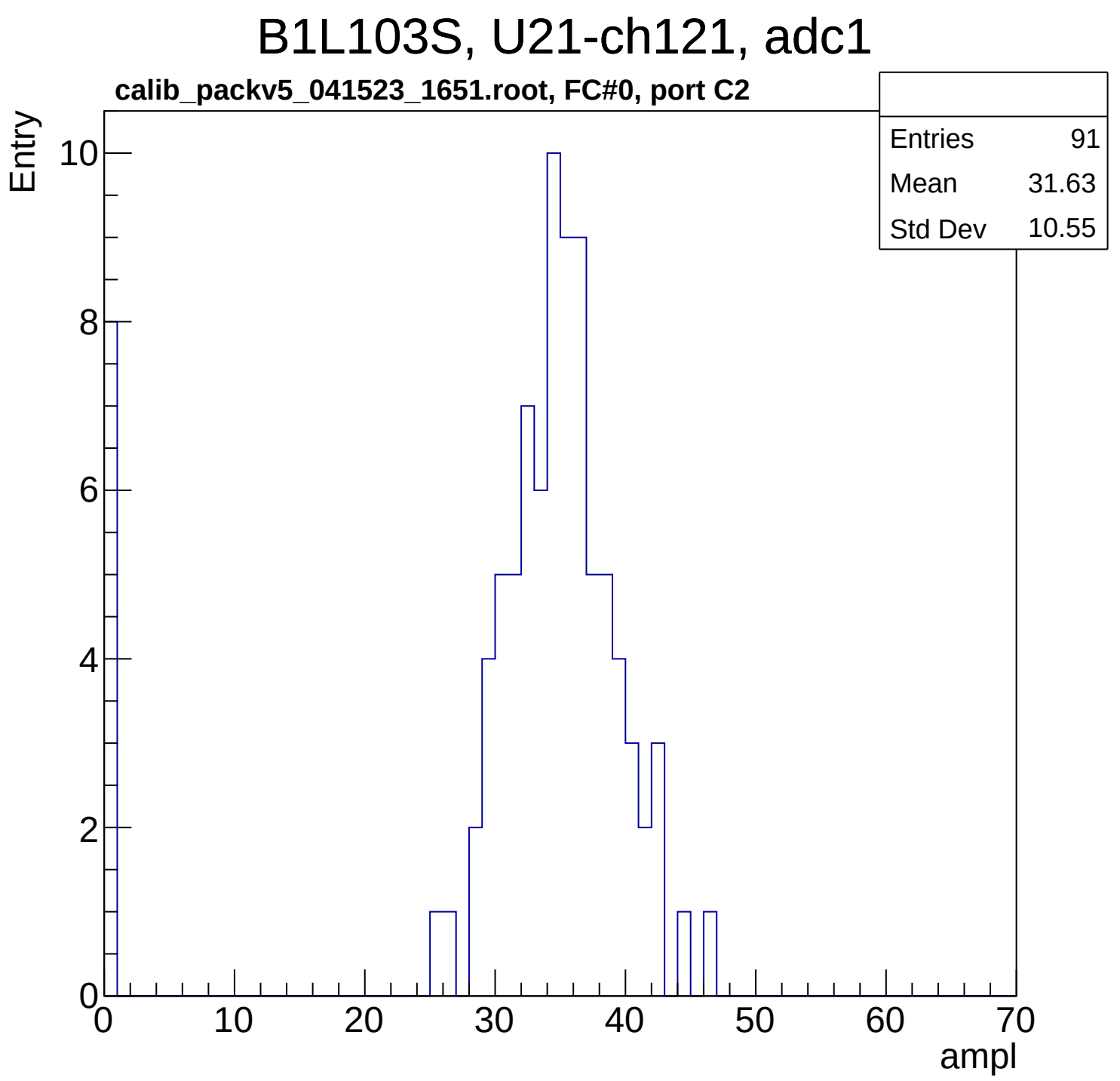
B1L103S, U21-ch121, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 31.63
Std Dev 10.55
Entry
ampl
0
2
4
6
8
10
0
10
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30
40
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60
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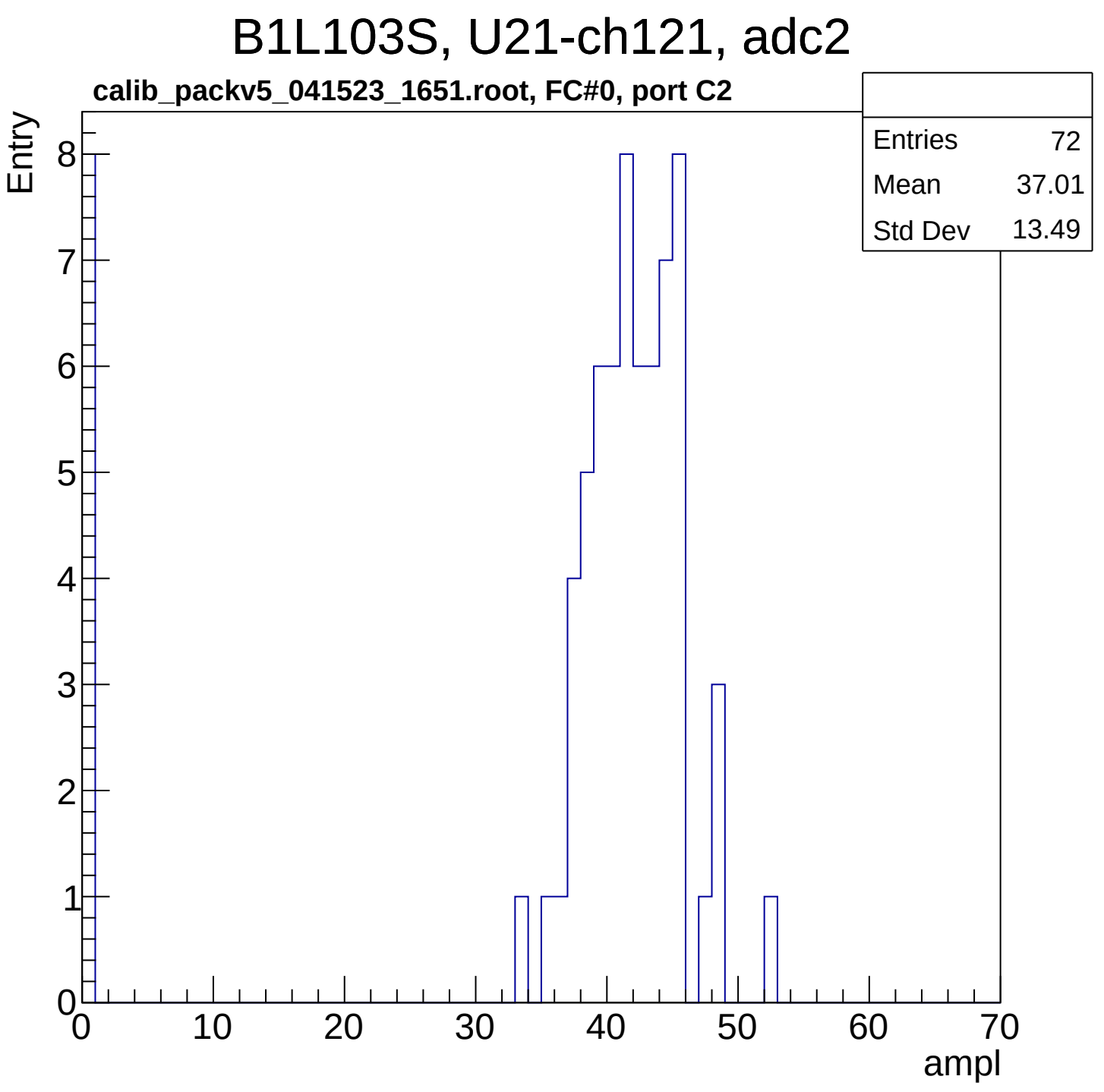
B1L103S, U21-ch121, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 37.01
Std Dev 13.49
Entry
ampl
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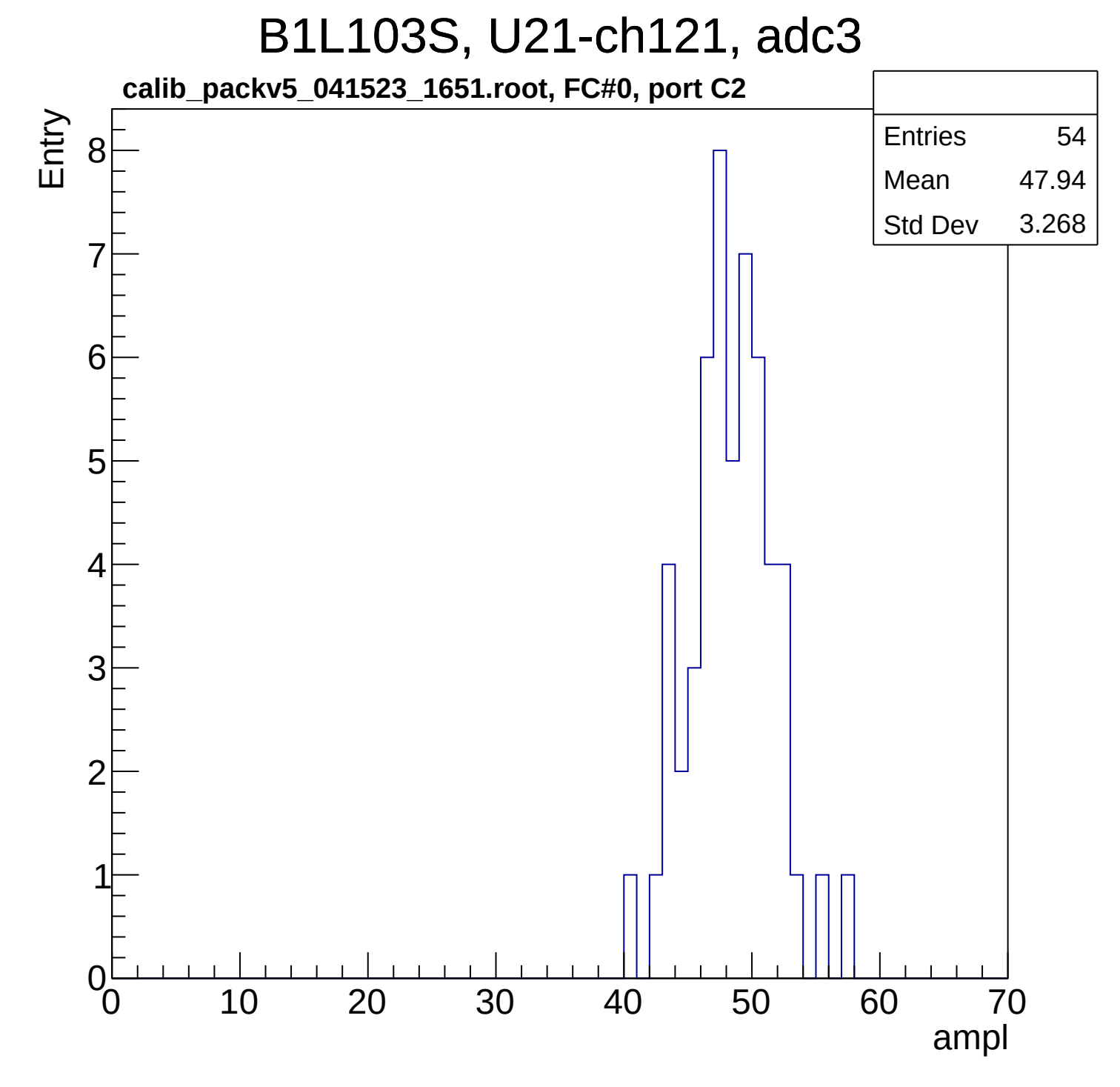
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch121, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 47.94
Std Dev 3.268
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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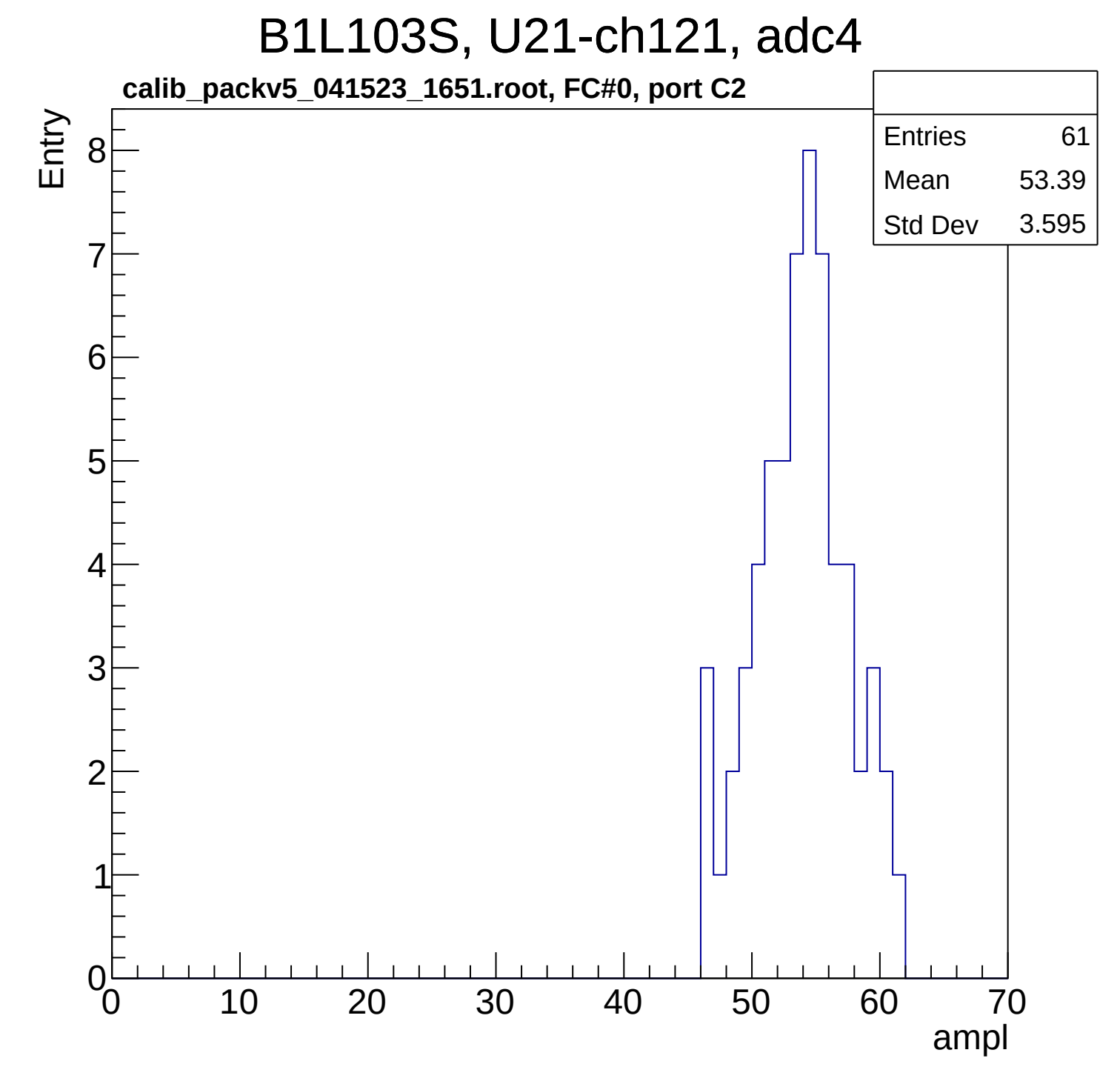
B1L103S, U21-ch121, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 53.39
Std Dev 3.595
Entry
ampl
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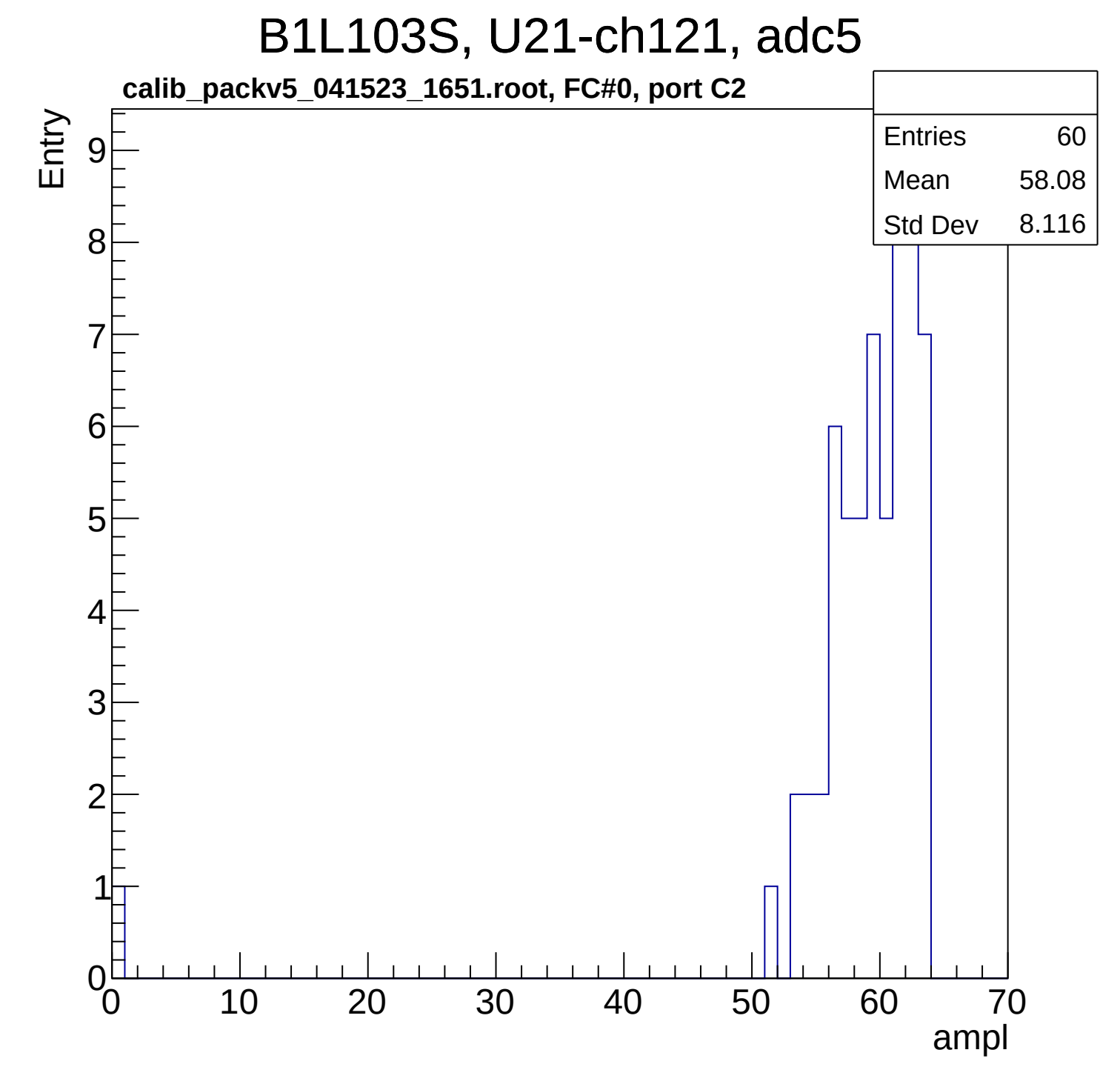
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch121, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 58.08
Std Dev 8.116
Entry
ampl
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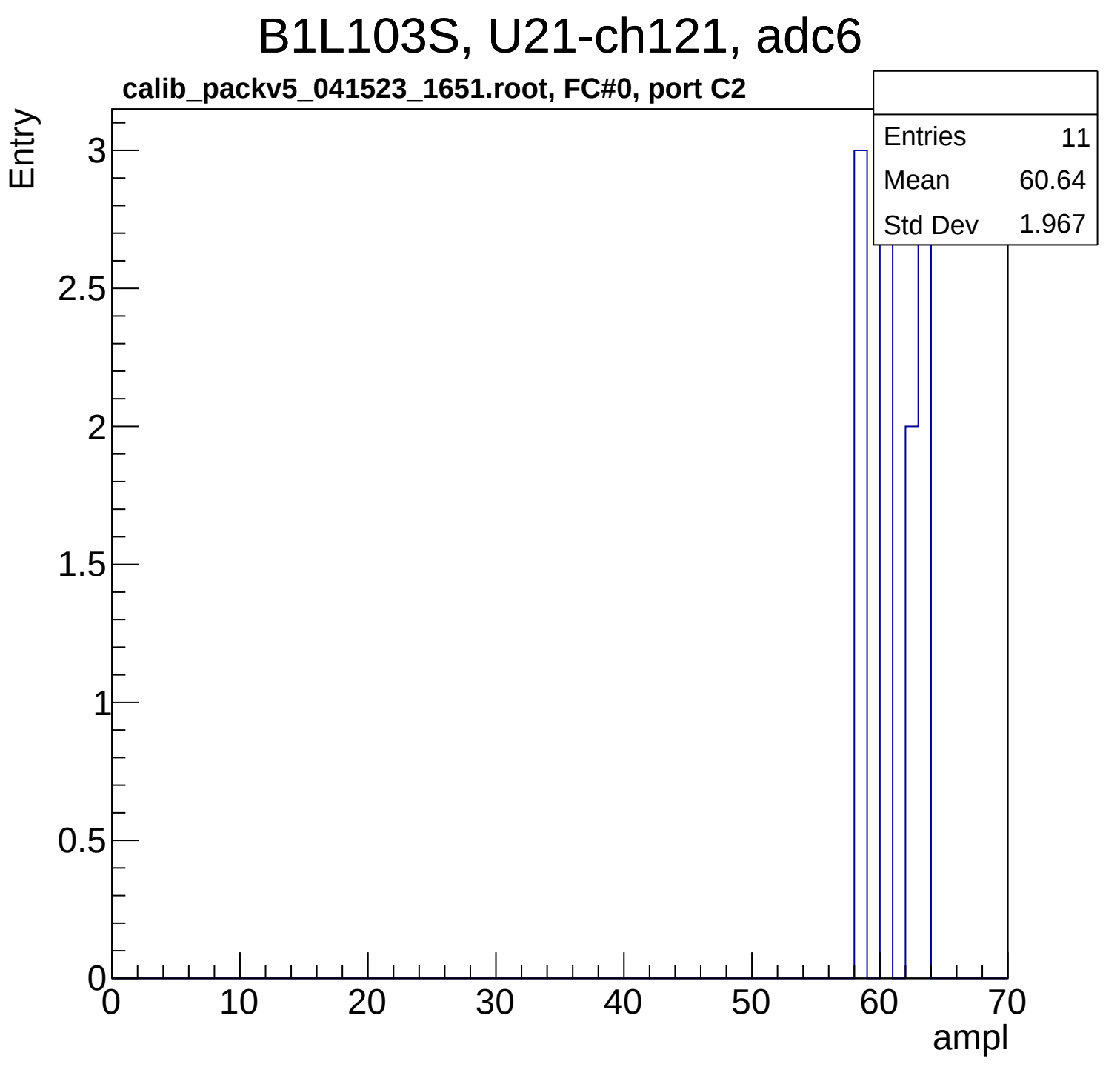
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch121, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 60.64
Std Dev 1.967
Entry
ampl
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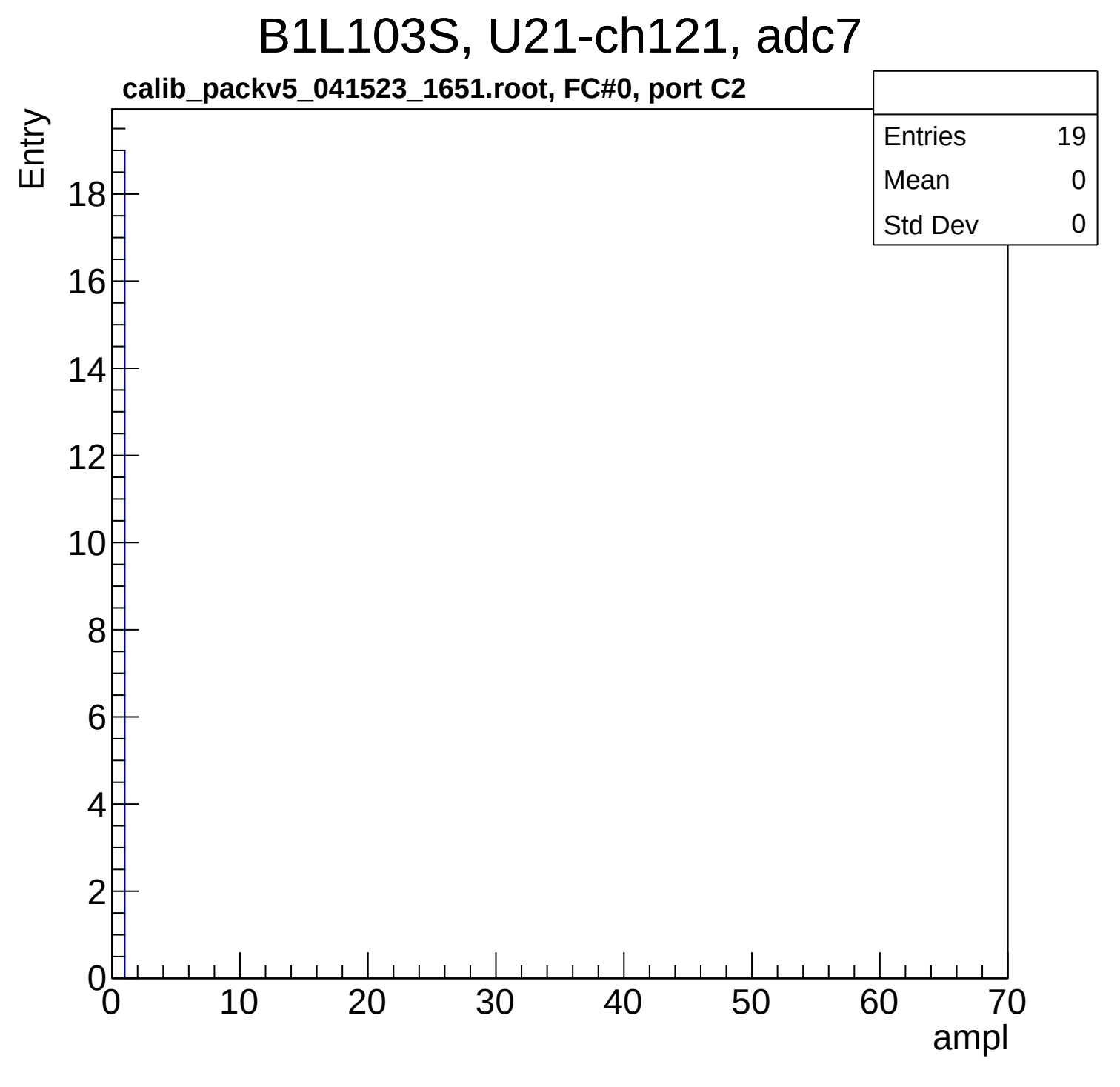
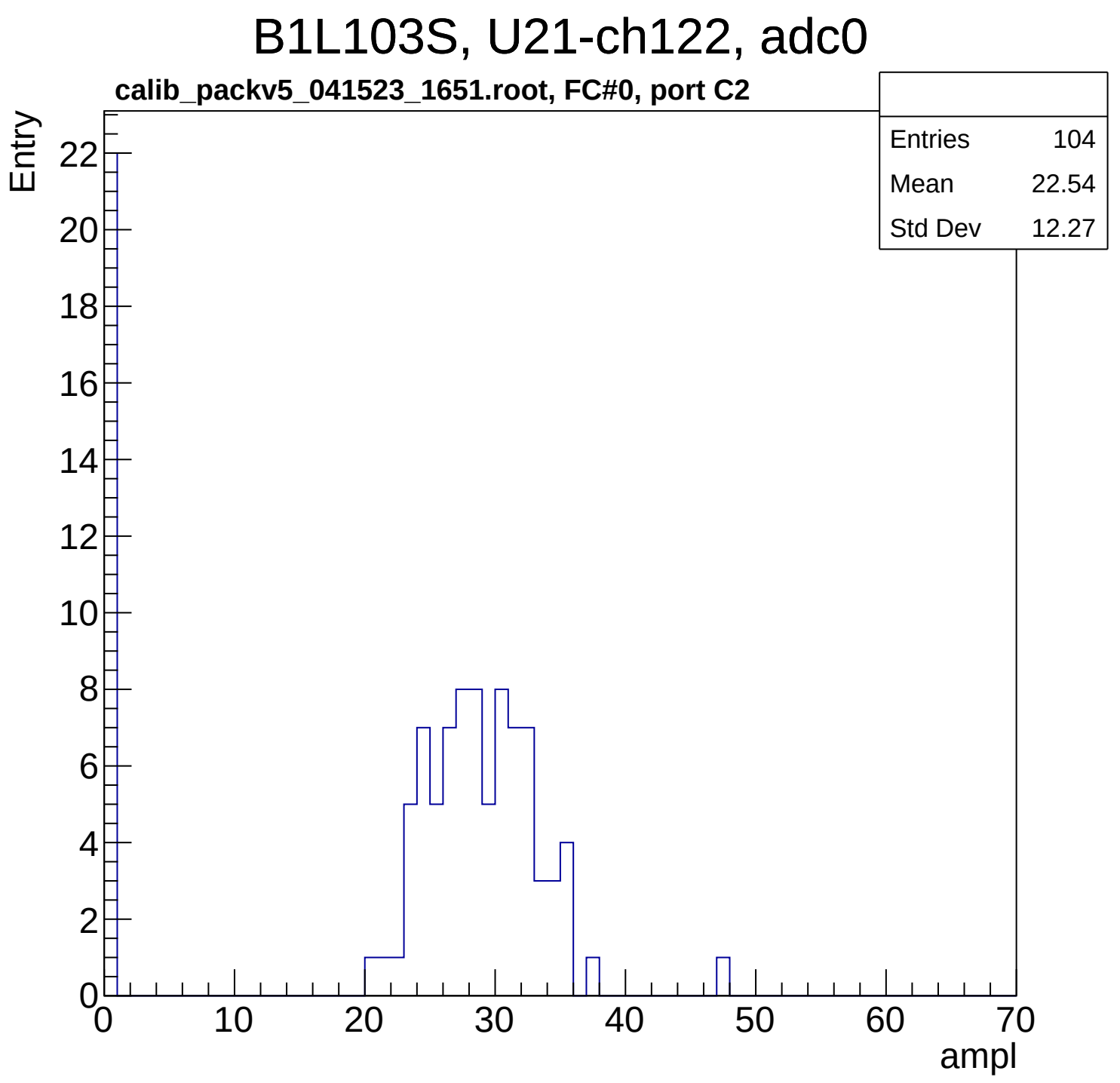
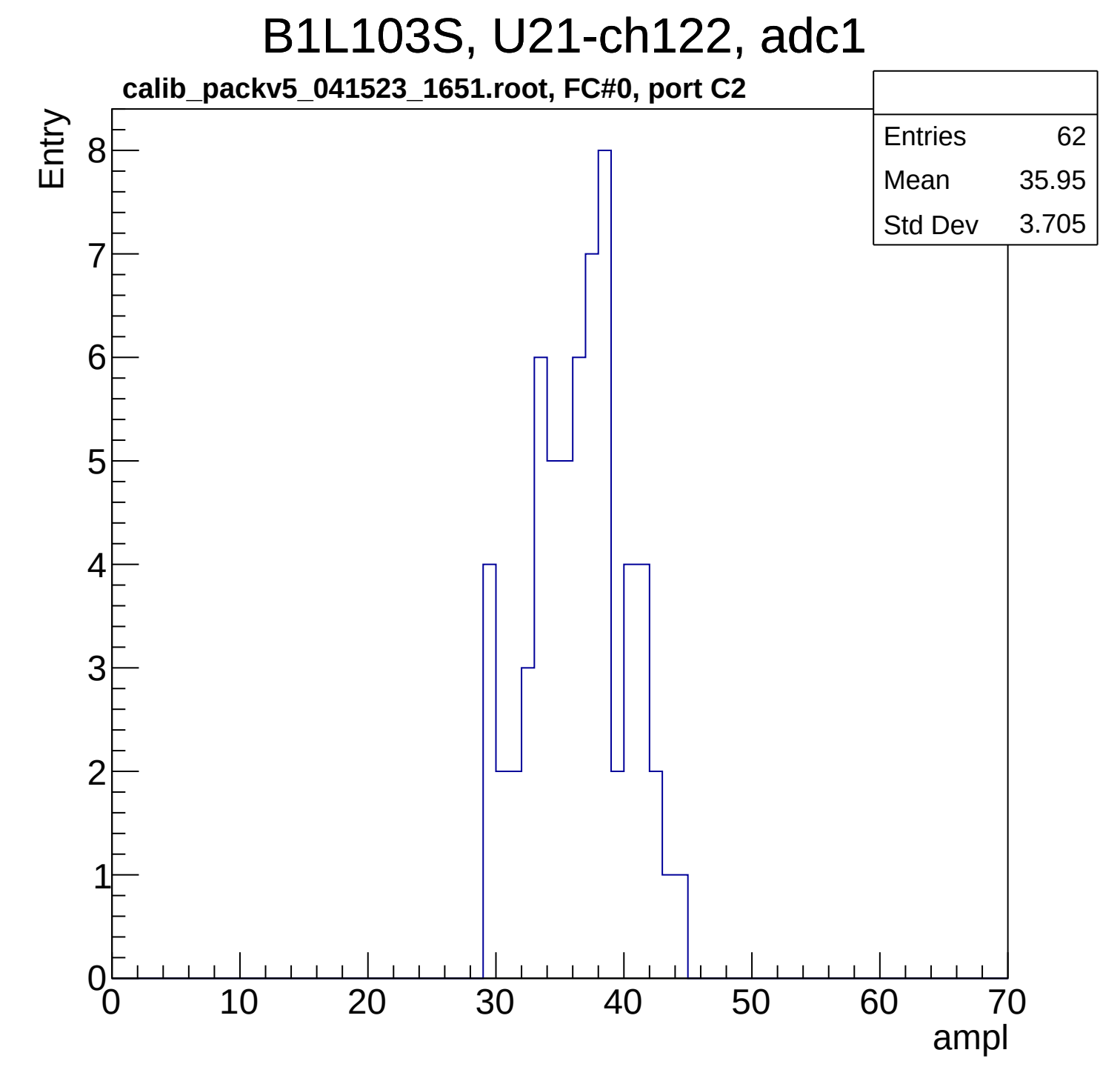
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U21-ch121, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch122, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 104
Mean 22.54
Std Dev 12.27
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70


B1L103S, U21-ch122, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 35.95
Std Dev 3.705
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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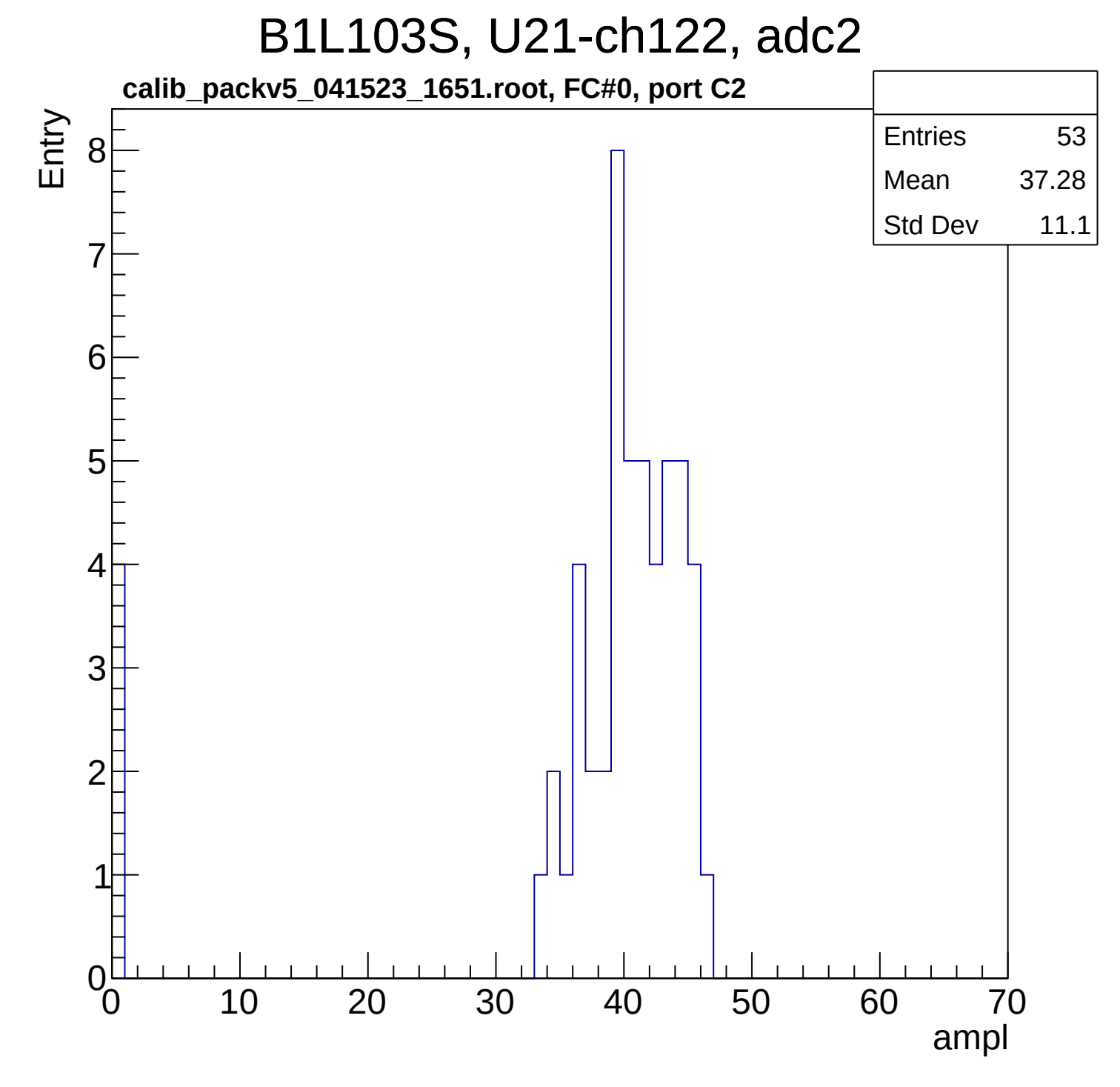
B1L103S, U21-ch122, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 37.28
Std Dev 11.1
Entry
ampl
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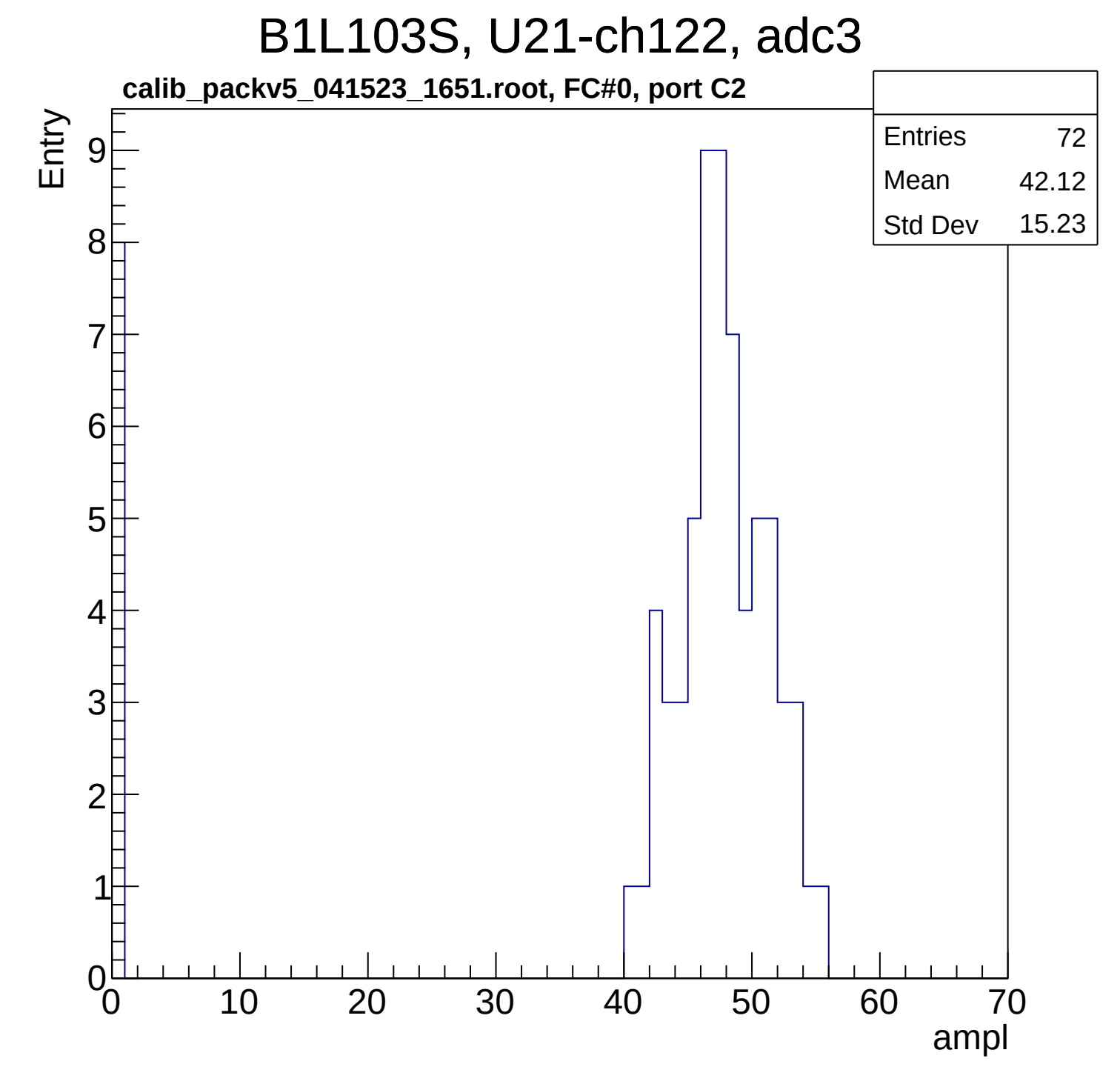
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch122, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 42.12
Std Dev 15.23
Entry
ampl
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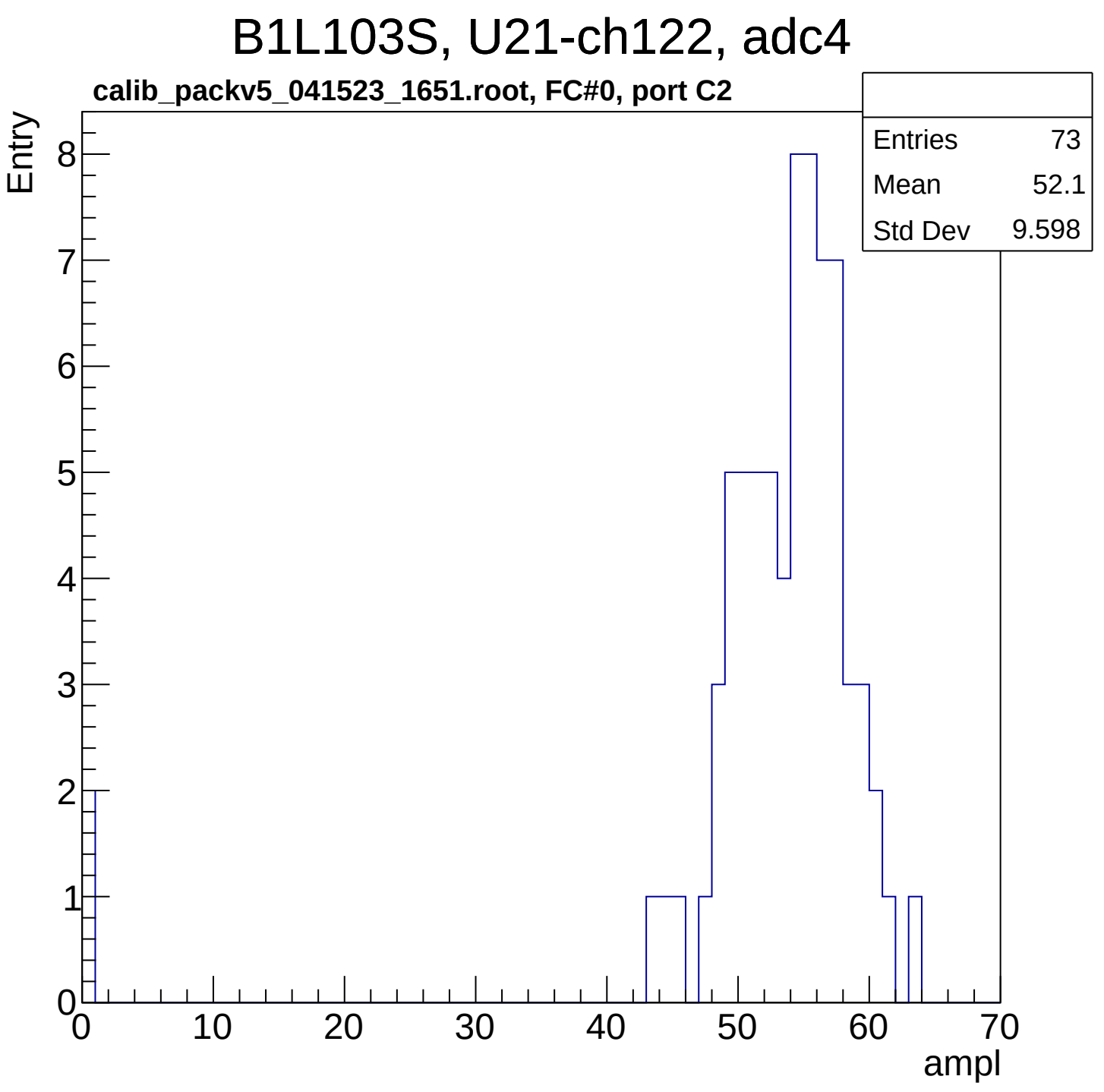
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch122, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 52.1
Std Dev 9.598
Entry
ampl
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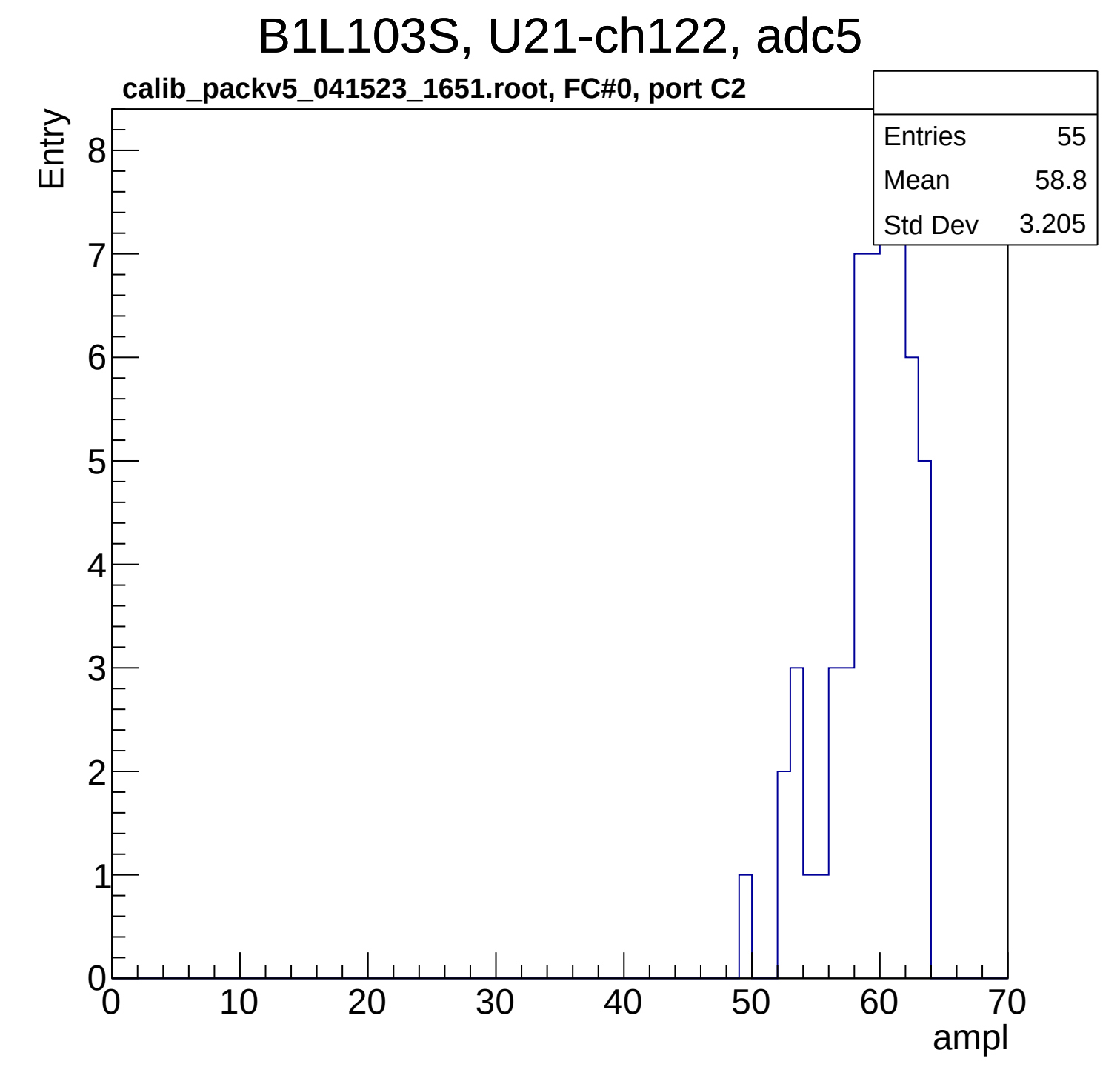
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch122, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 58.8
Std Dev 3.205
Entry
ampl
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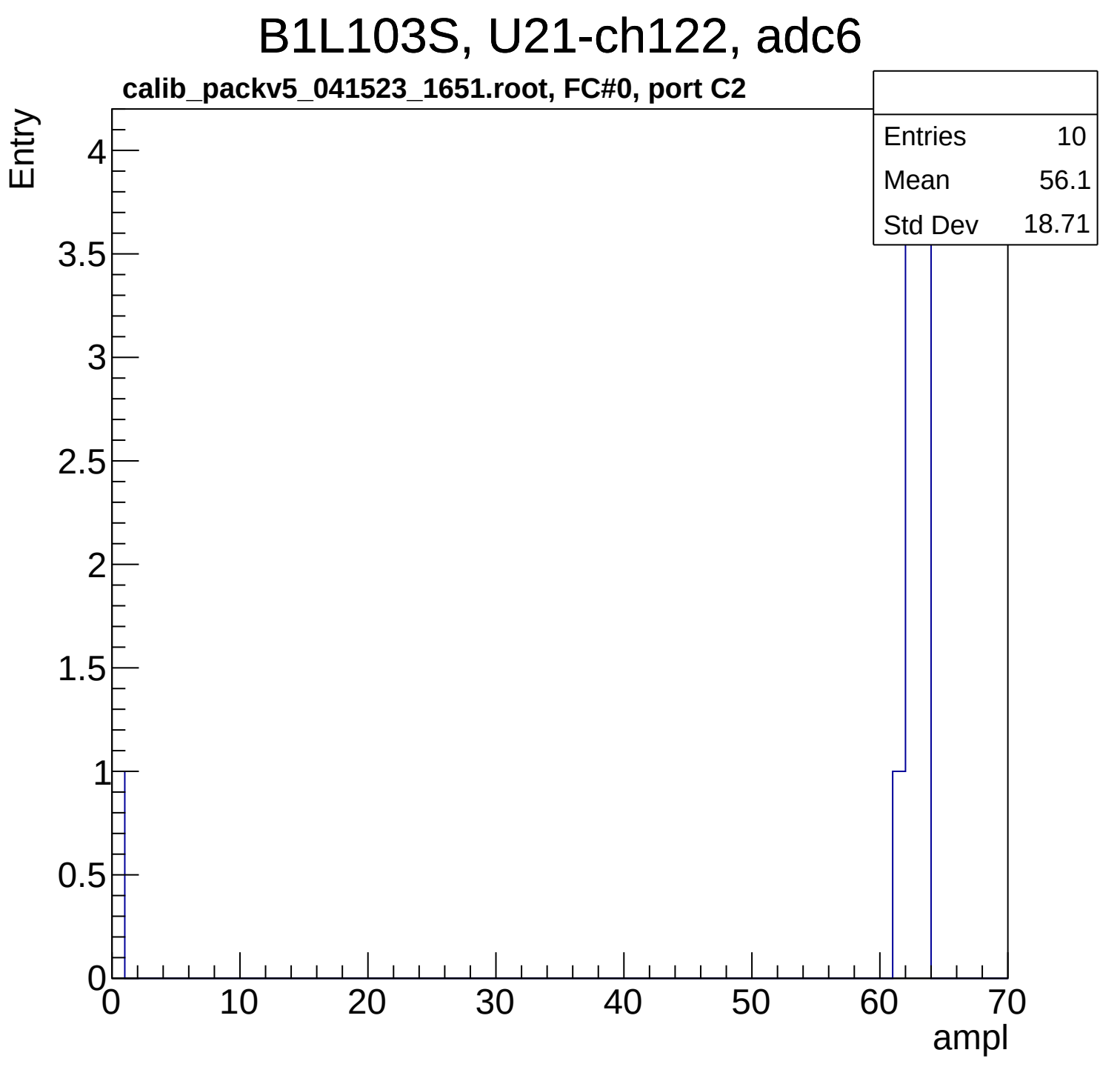
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch122, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 56.1
Std Dev 18.71
Entry
ampl
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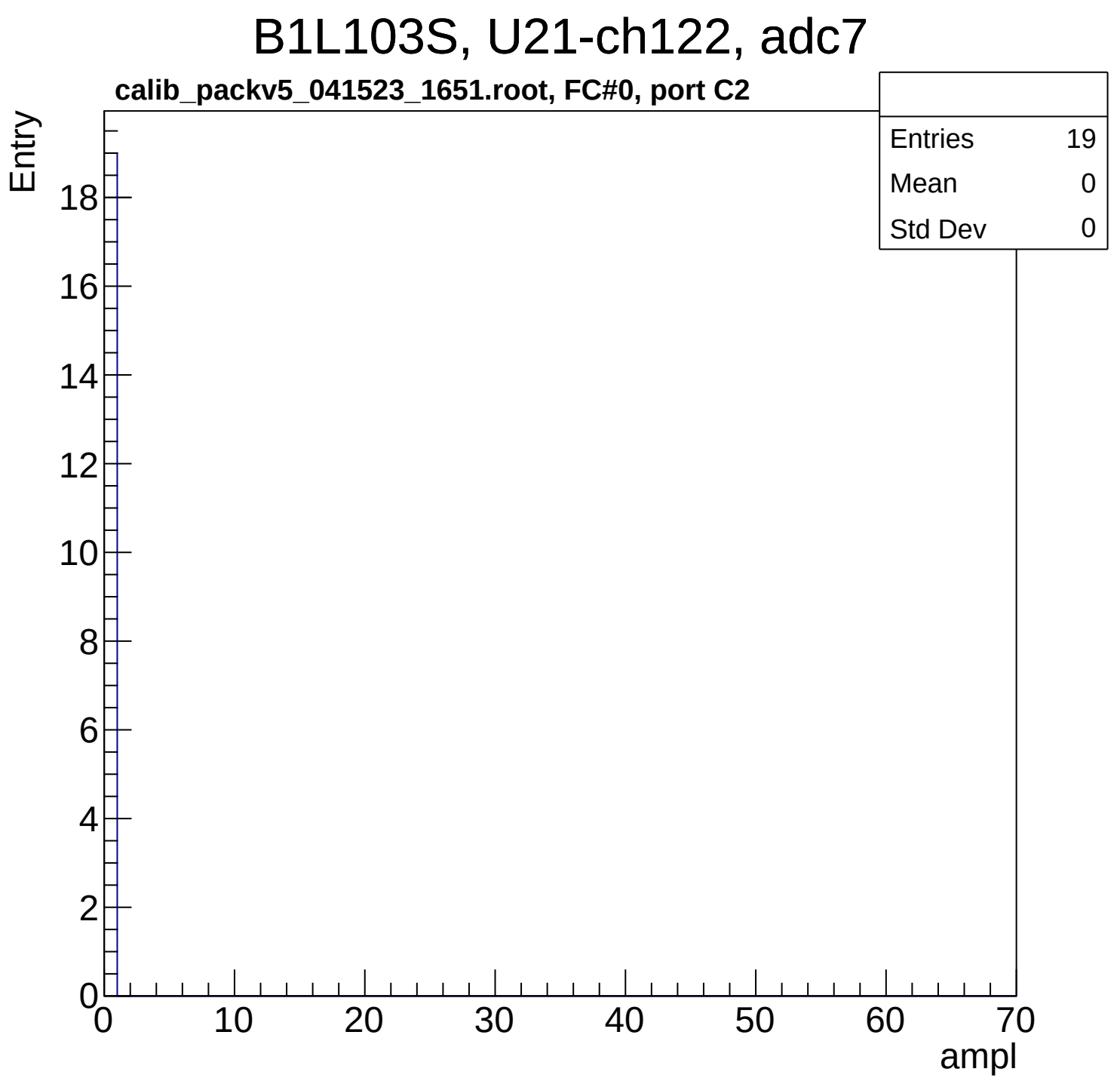
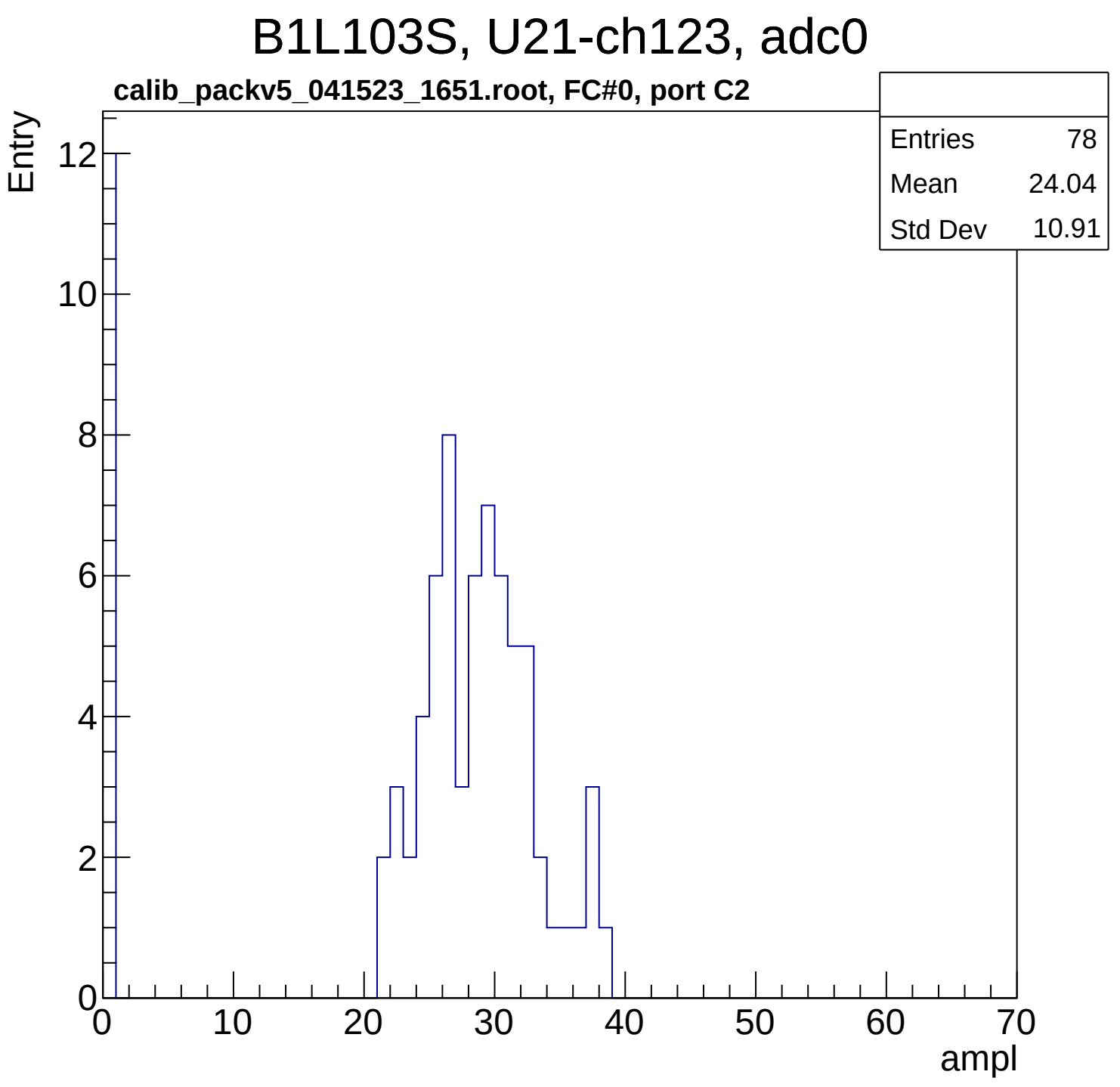
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U21-ch122, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch123, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 24.04
Std Dev 10.91
Entry
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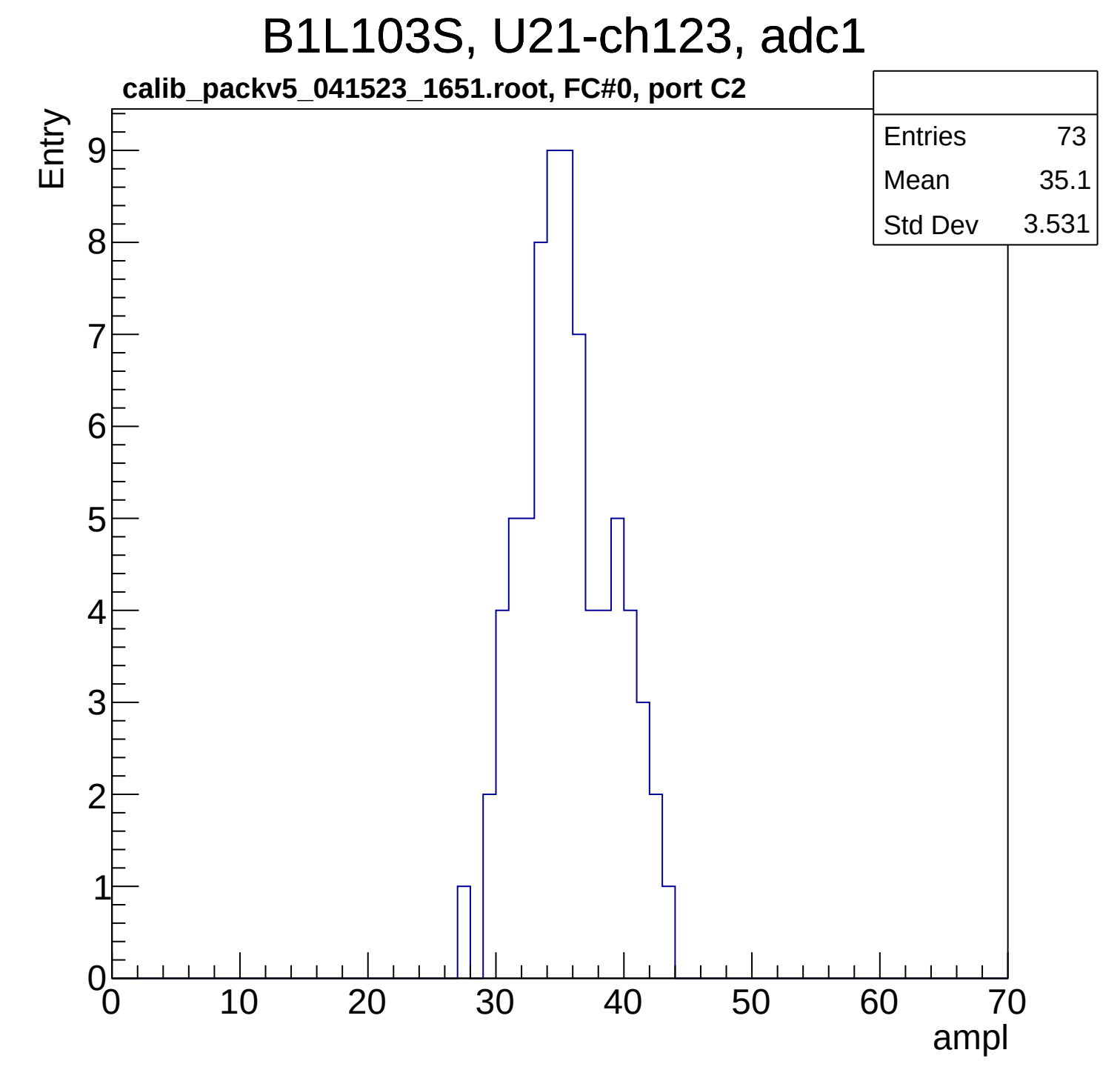
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch123, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 35.1
Std Dev 3.531
Entry
ampl
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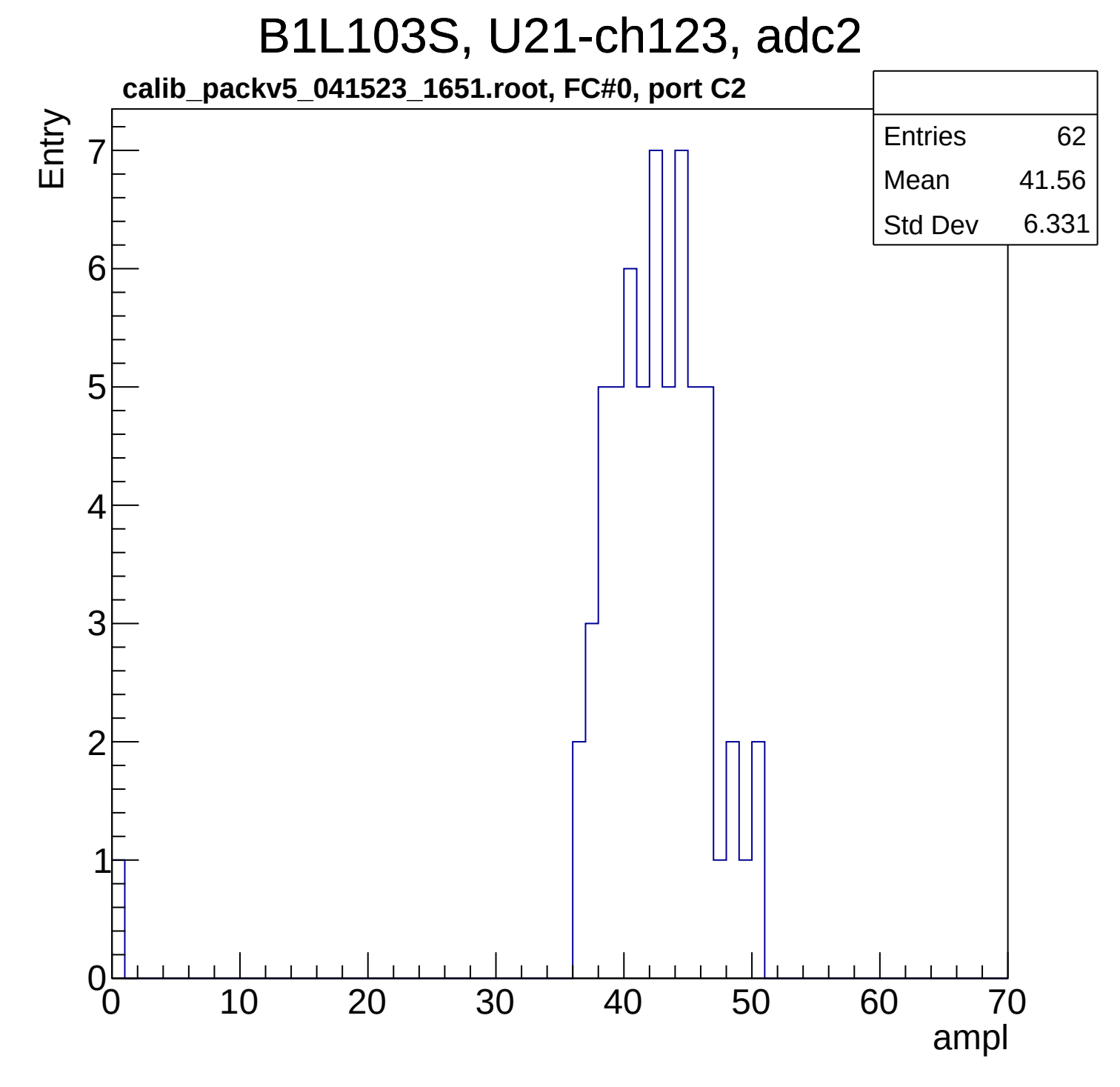
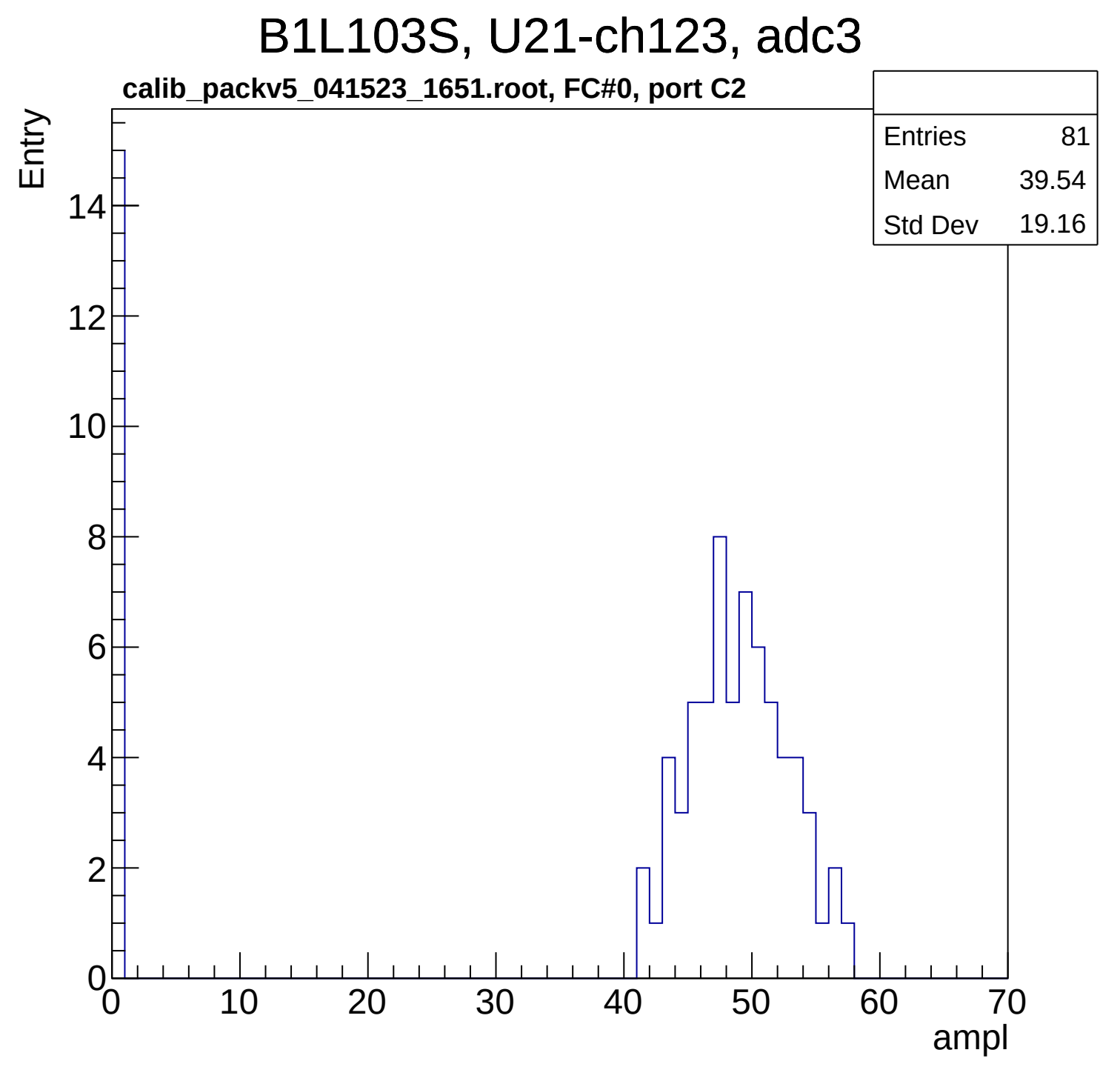
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch123, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 41.56
Std Dev 6.331
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U21-ch123, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 39.54
Std Dev 19.16
Entry
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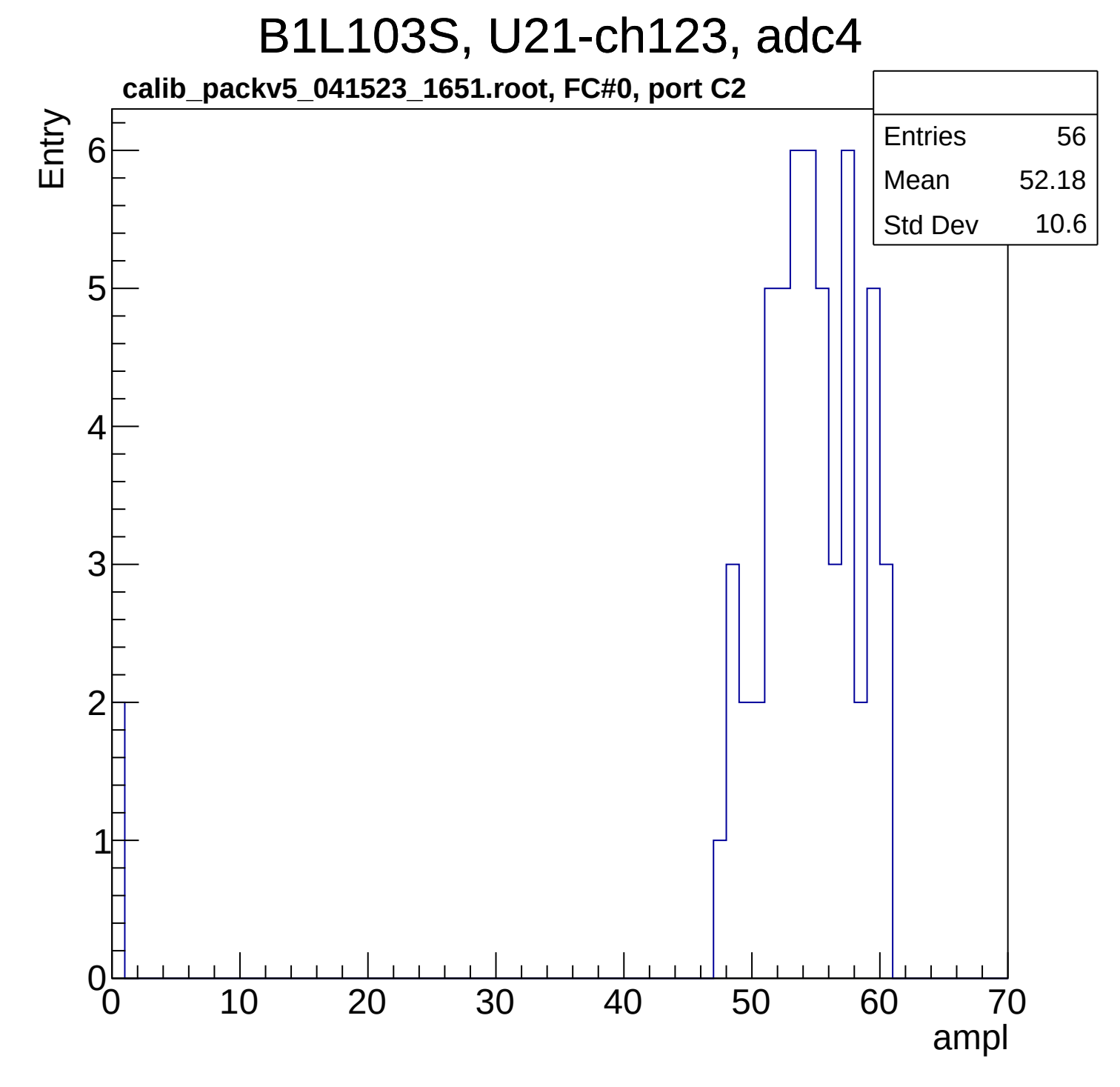
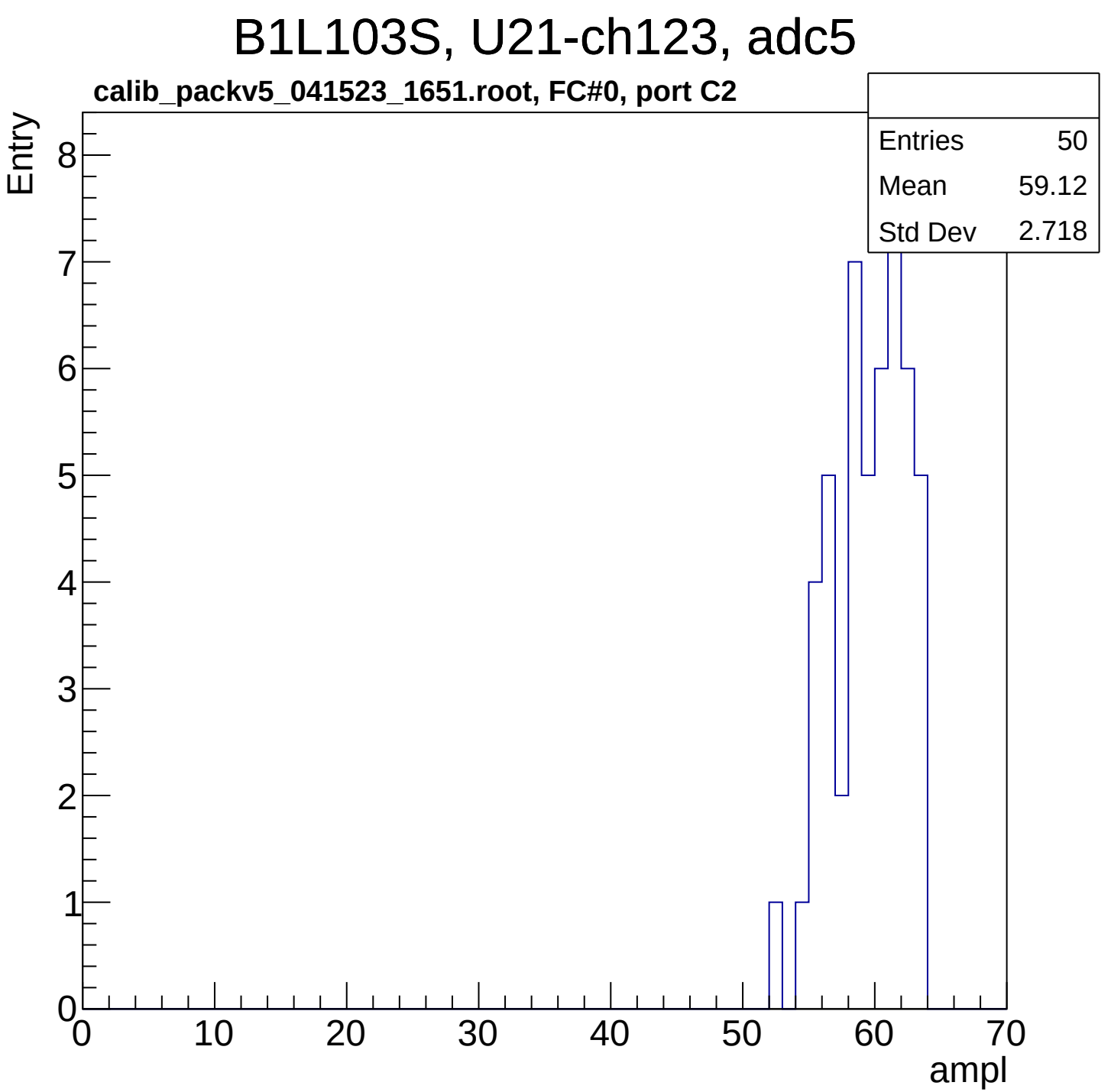
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch123, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 52.18
Std Dev 10.6
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U21-ch123, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 59.12
Std Dev 2.718
Entry
ampl
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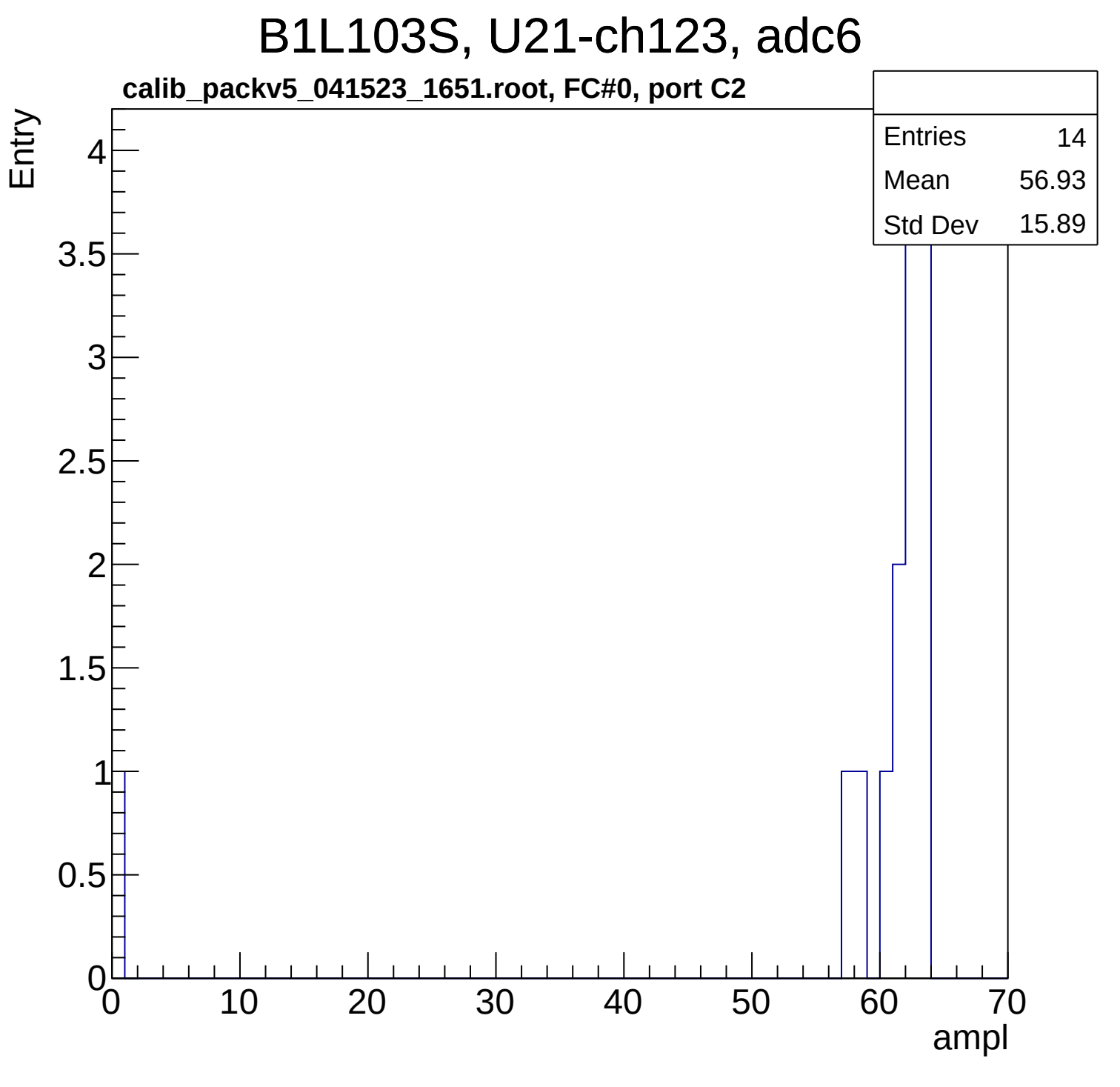
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch123, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 56.93
Std Dev 15.89
Entry
ampl
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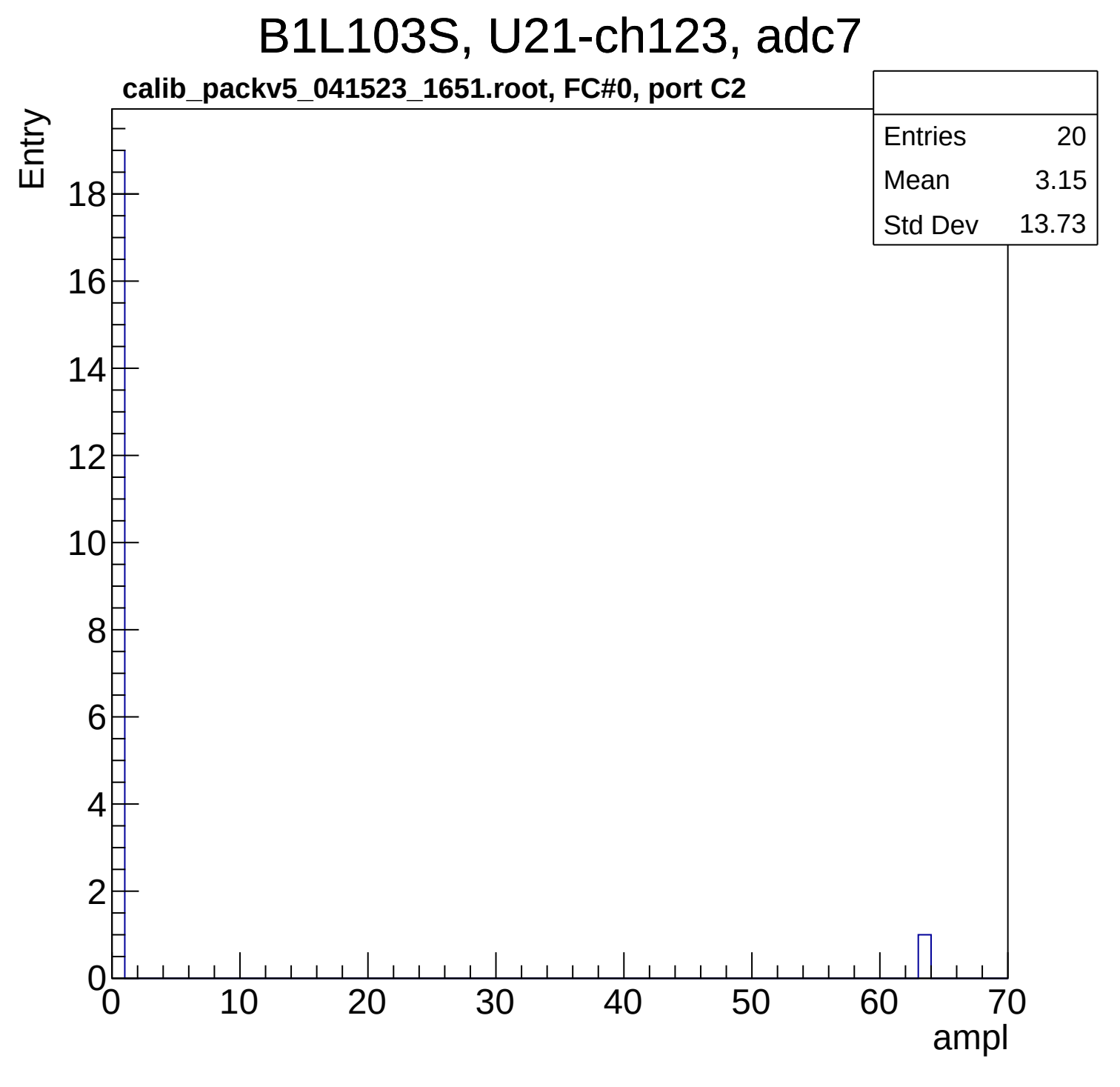
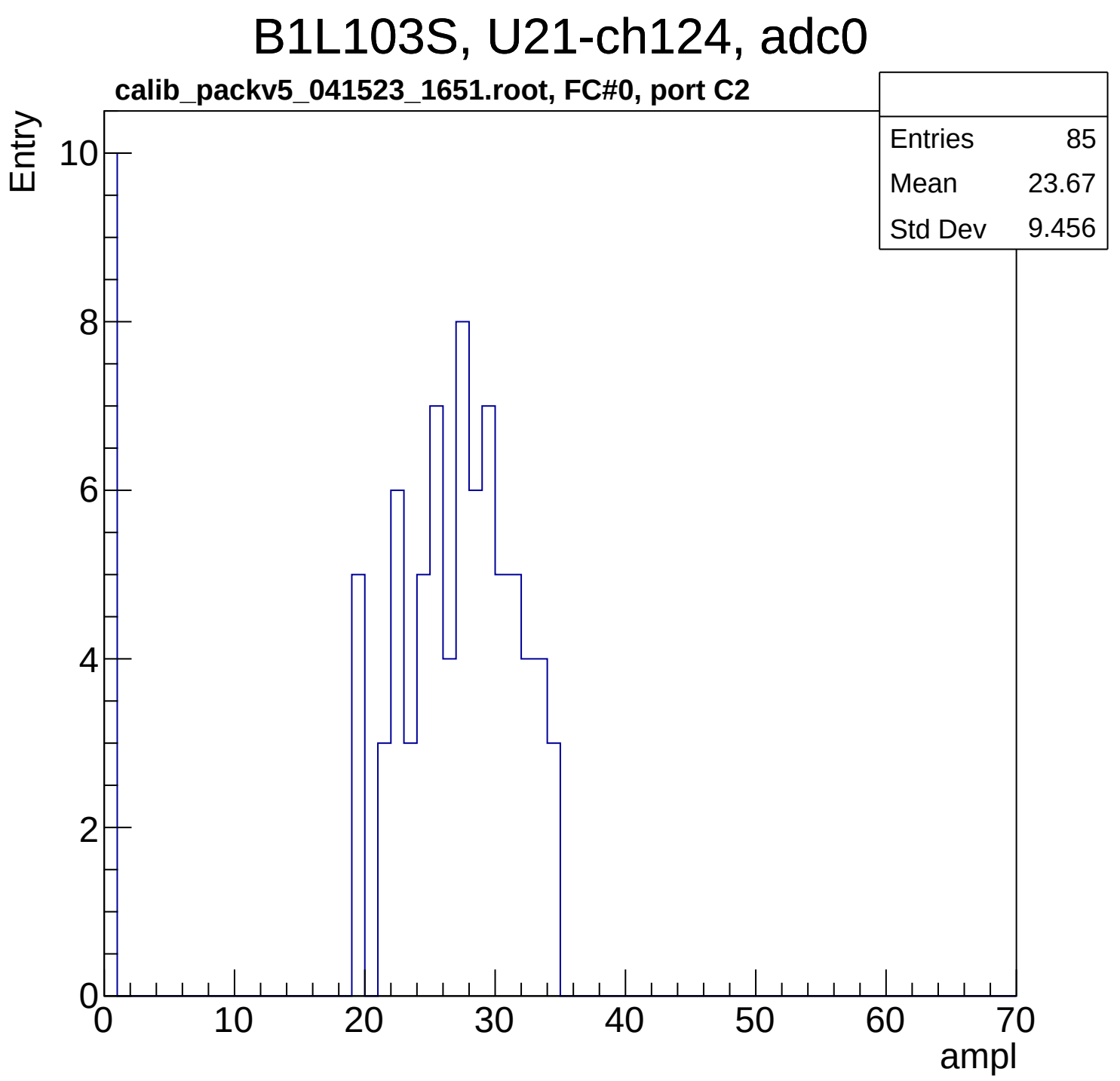
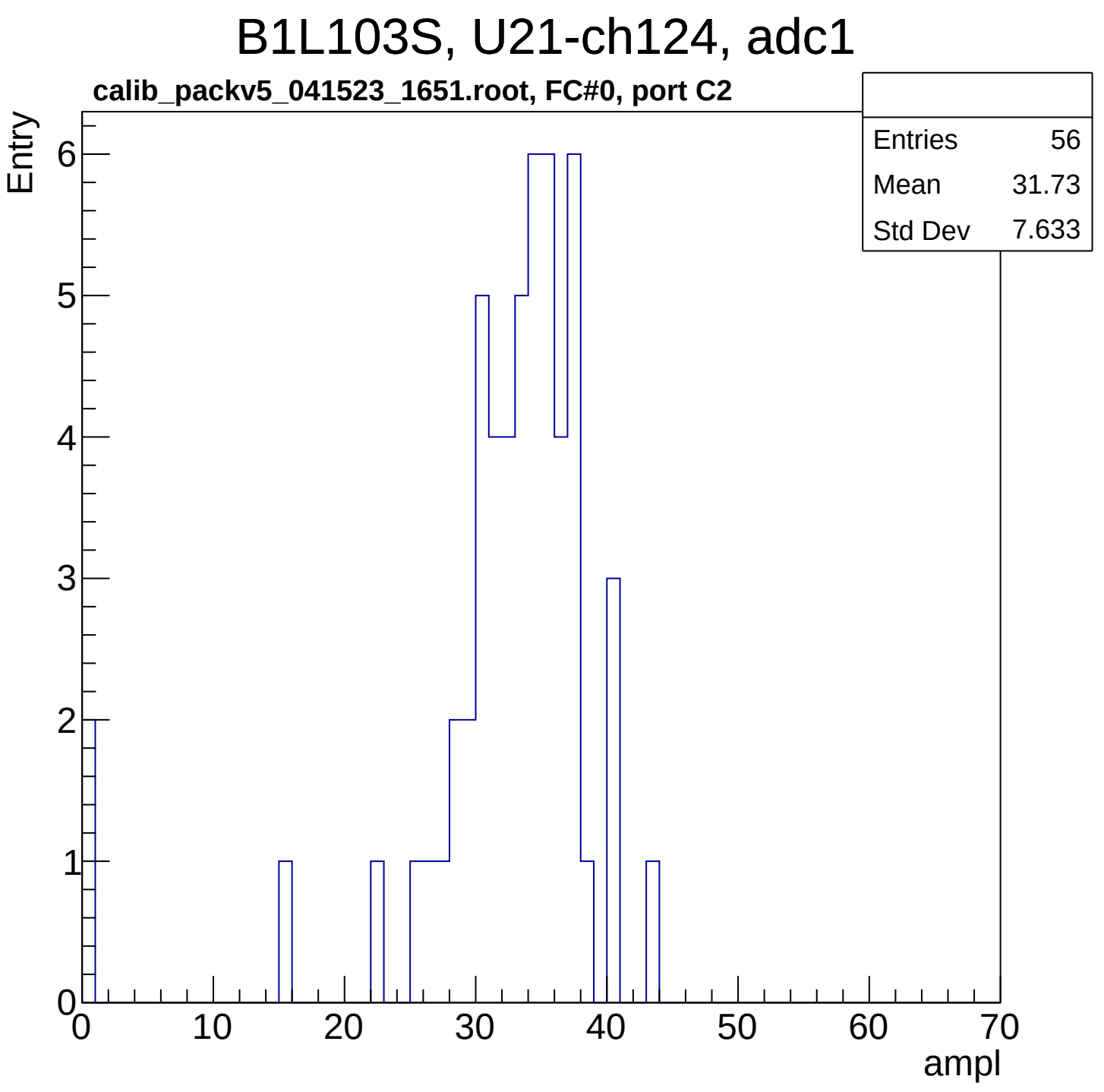
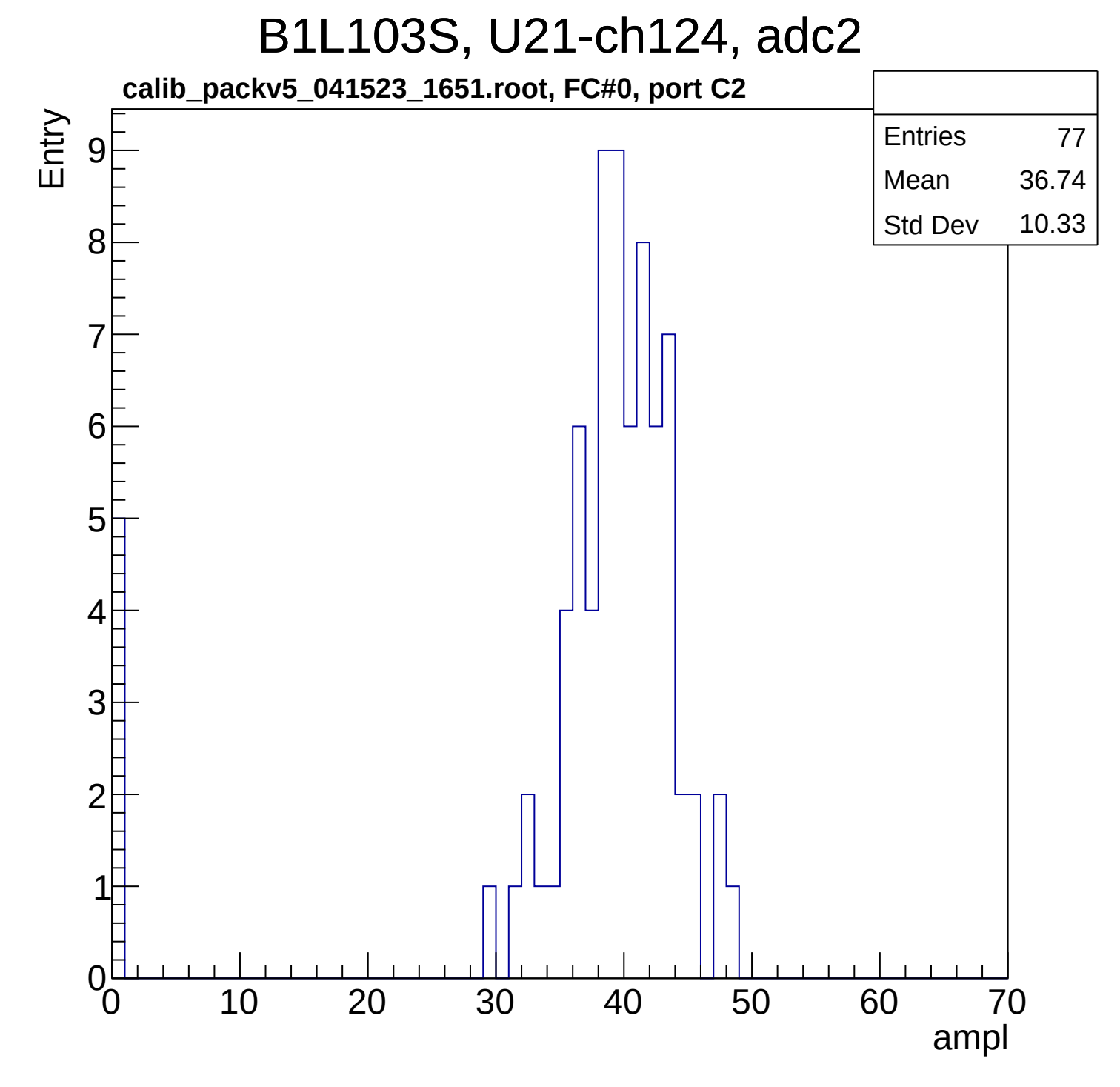
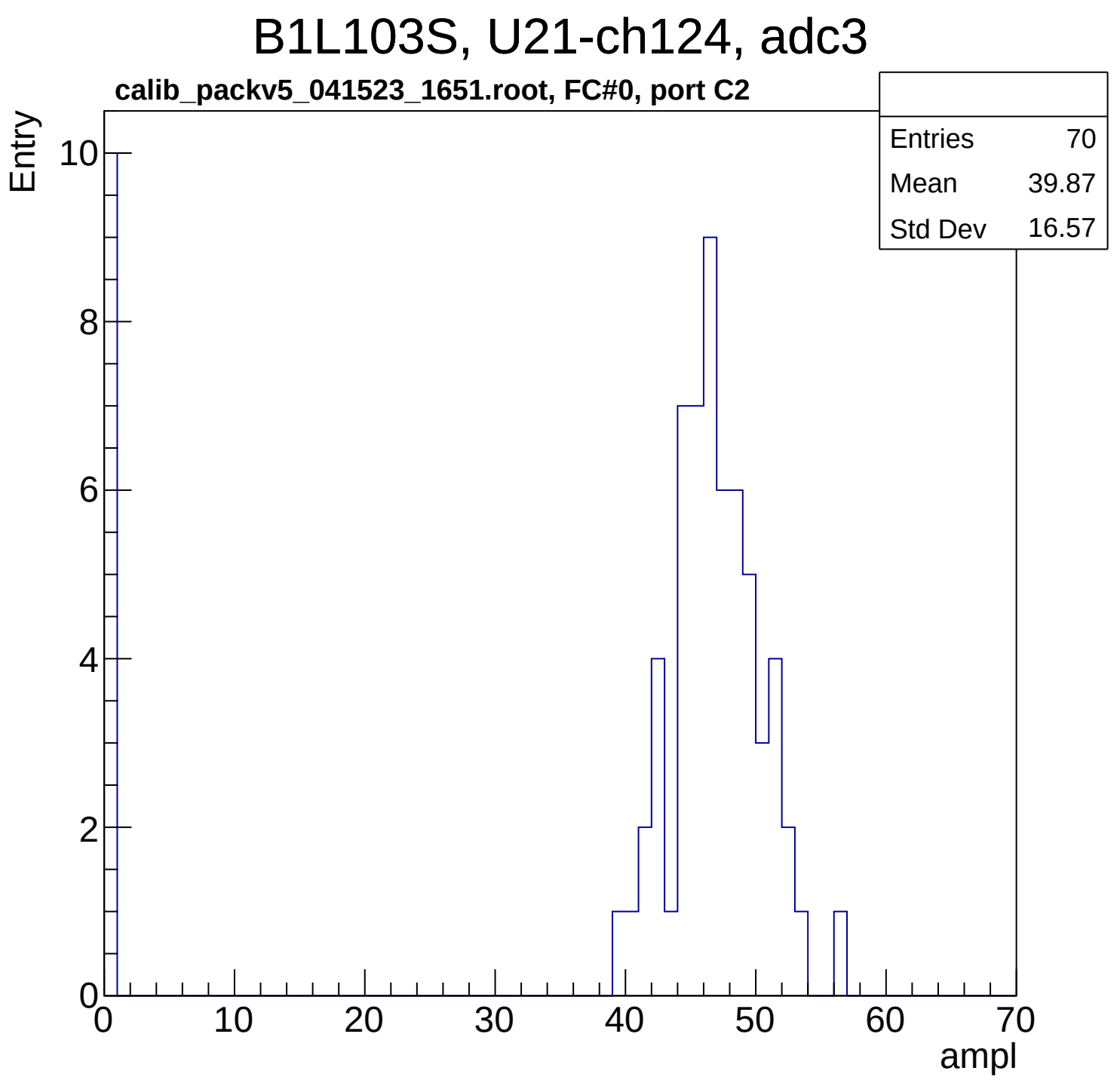
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U21-ch123, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch124, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 23.67
Std Dev 9.456
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch124, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 31.73
Std Dev 7.633
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch124, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 36.74
Std Dev 10.33
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch124, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 39.87
Std Dev 16.57
Entry
ampl
0
2
4
6
8
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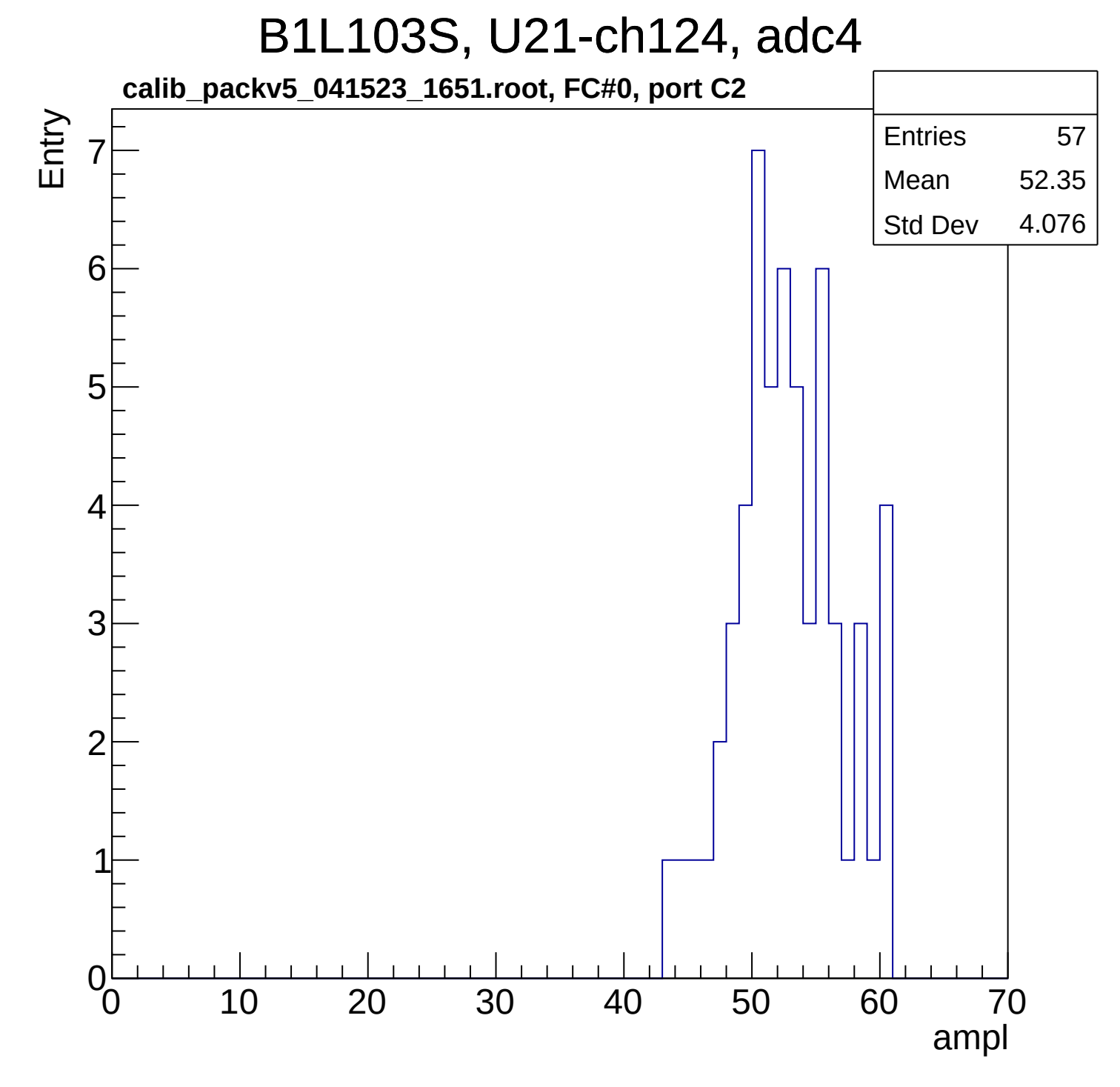
0
10
20
30
40
50
60
70


B1L103S, U21-ch124, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 52.35
Std Dev 4.076
Entry
ampl
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4
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0
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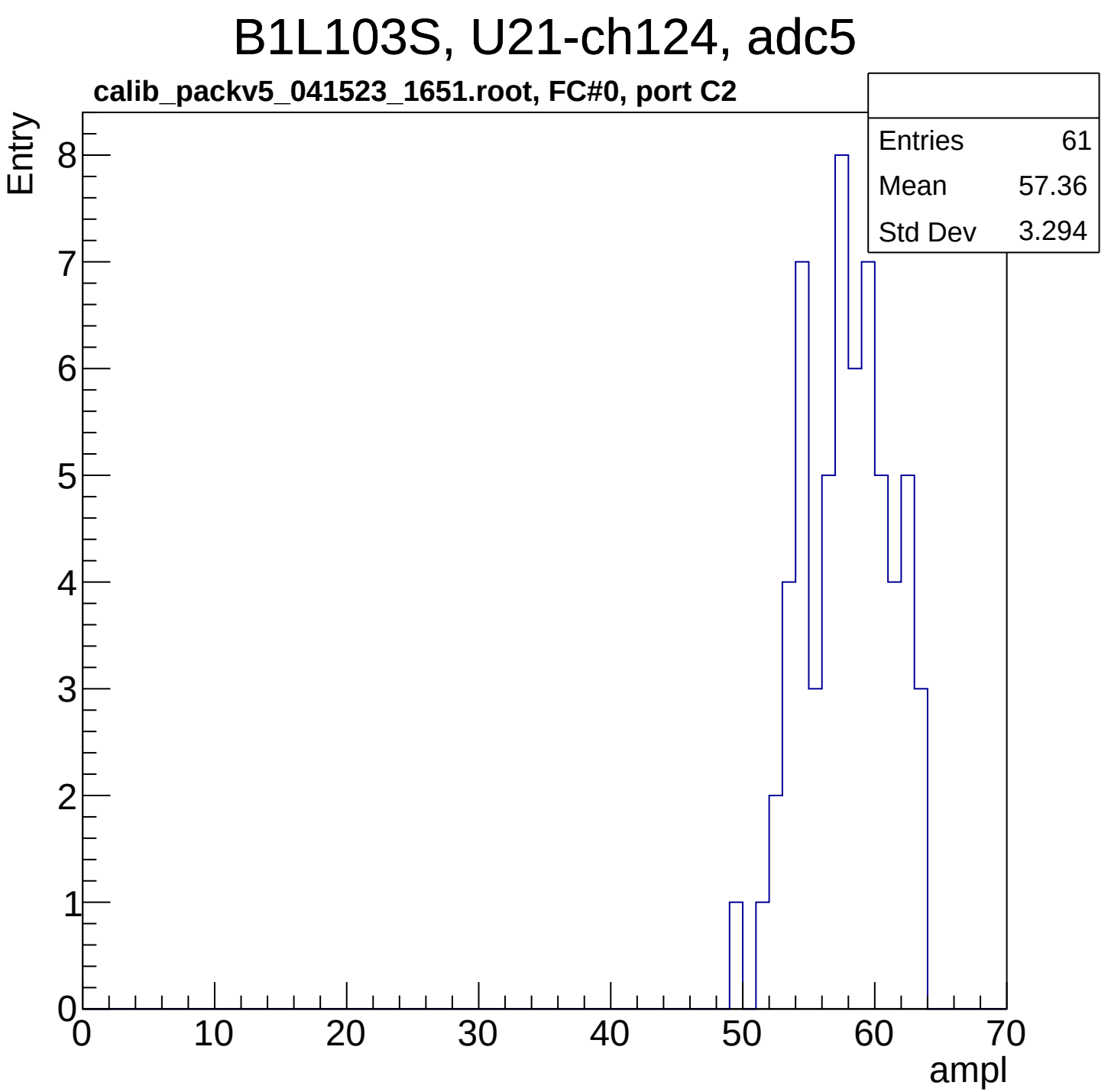
B1L103S, U21-ch124, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 57.36
Std Dev 3.294
Entry
ampl
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2
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0
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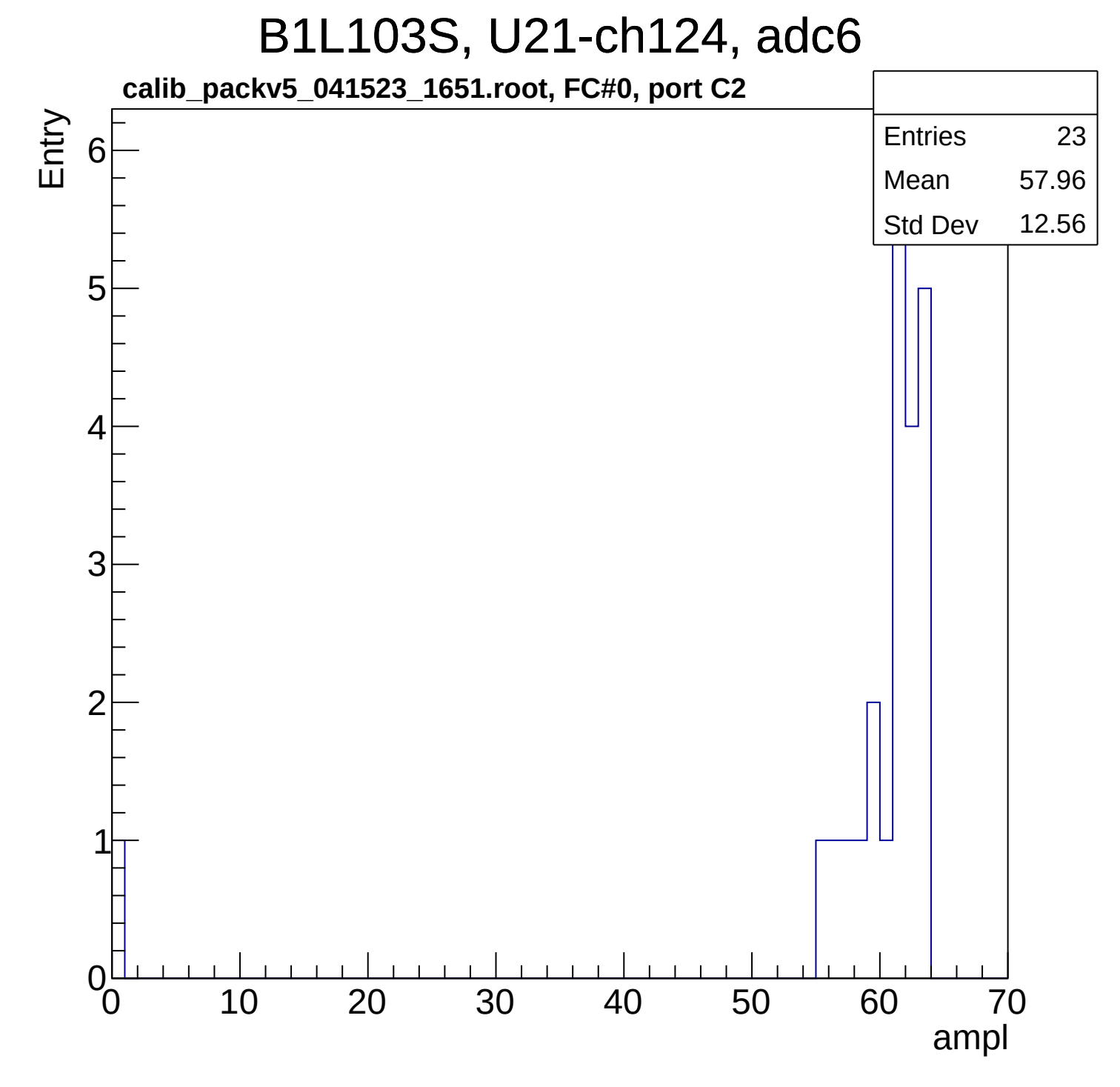
B1L103S, U21-ch124, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 57.96
Std Dev 12.56
Entry
ampl
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2
3
4
5
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0
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40
50
60
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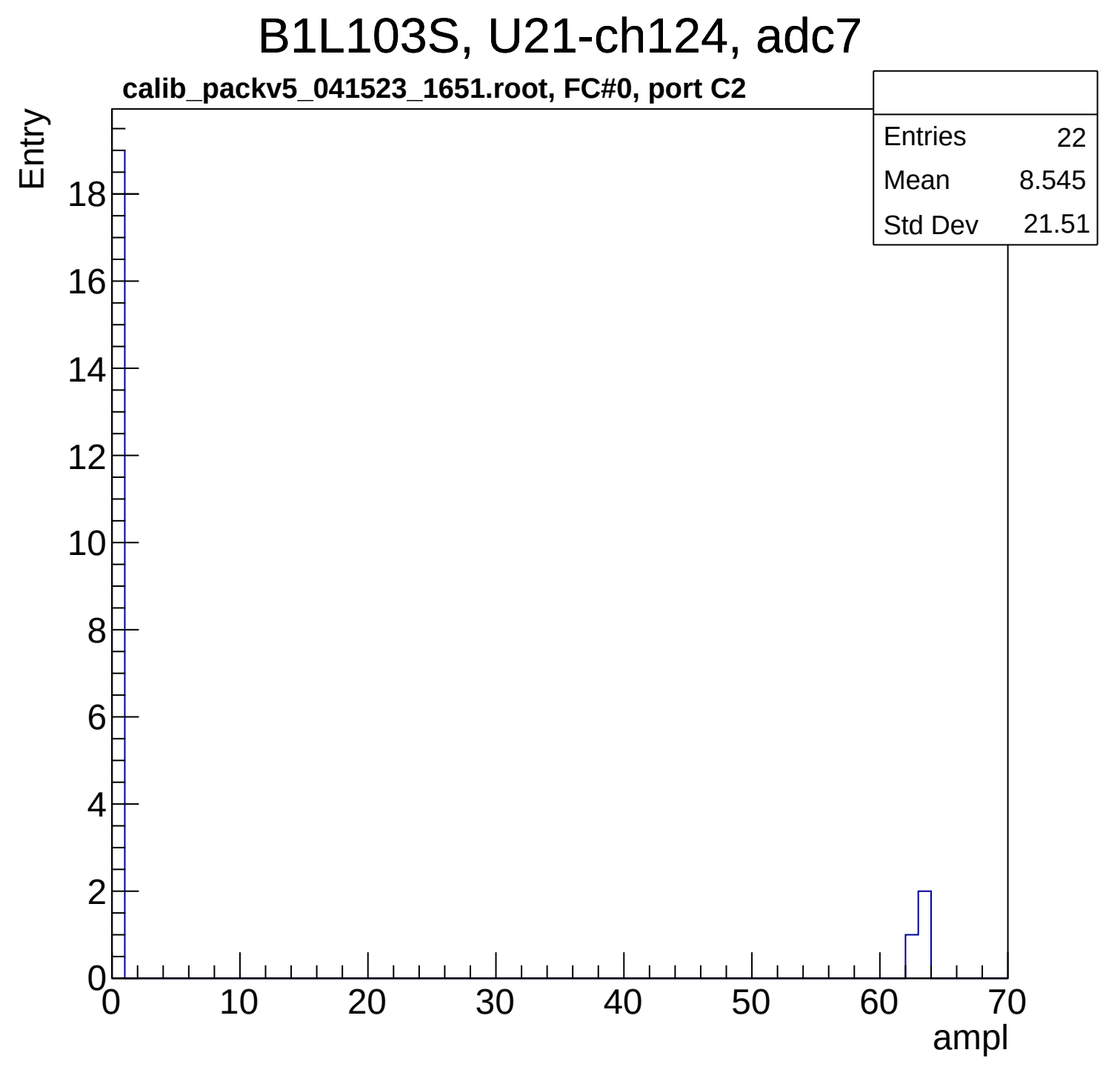
B1L103S, U21-ch124, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.545
Std Dev 21.51
Entry
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6
8
10
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14
16
18
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10
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50
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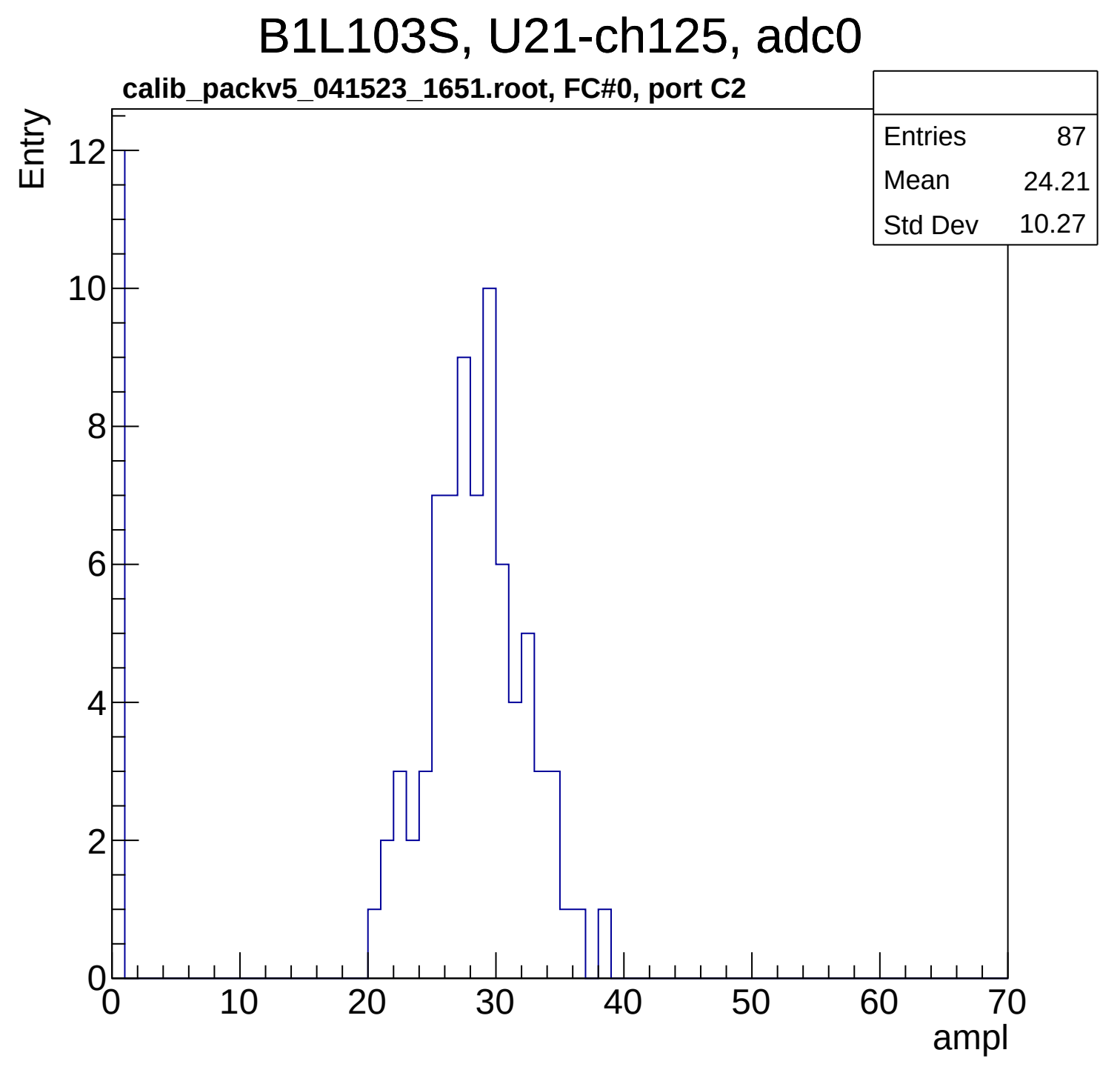
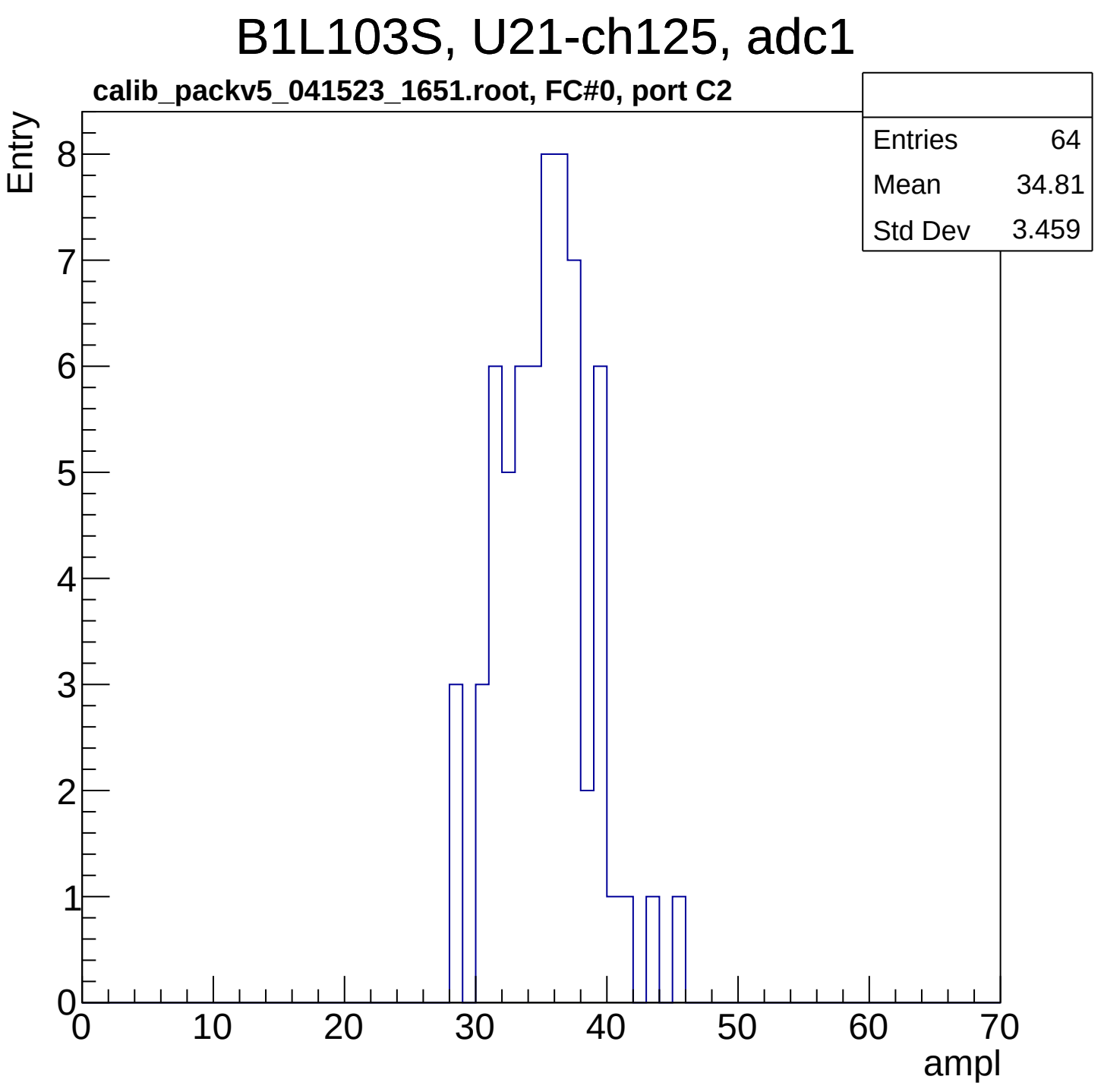
70
ampl


B1L103S, U21-ch125, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 24.21
Std Dev 10.27
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch125, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 34.81
Std Dev 3.459
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
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60
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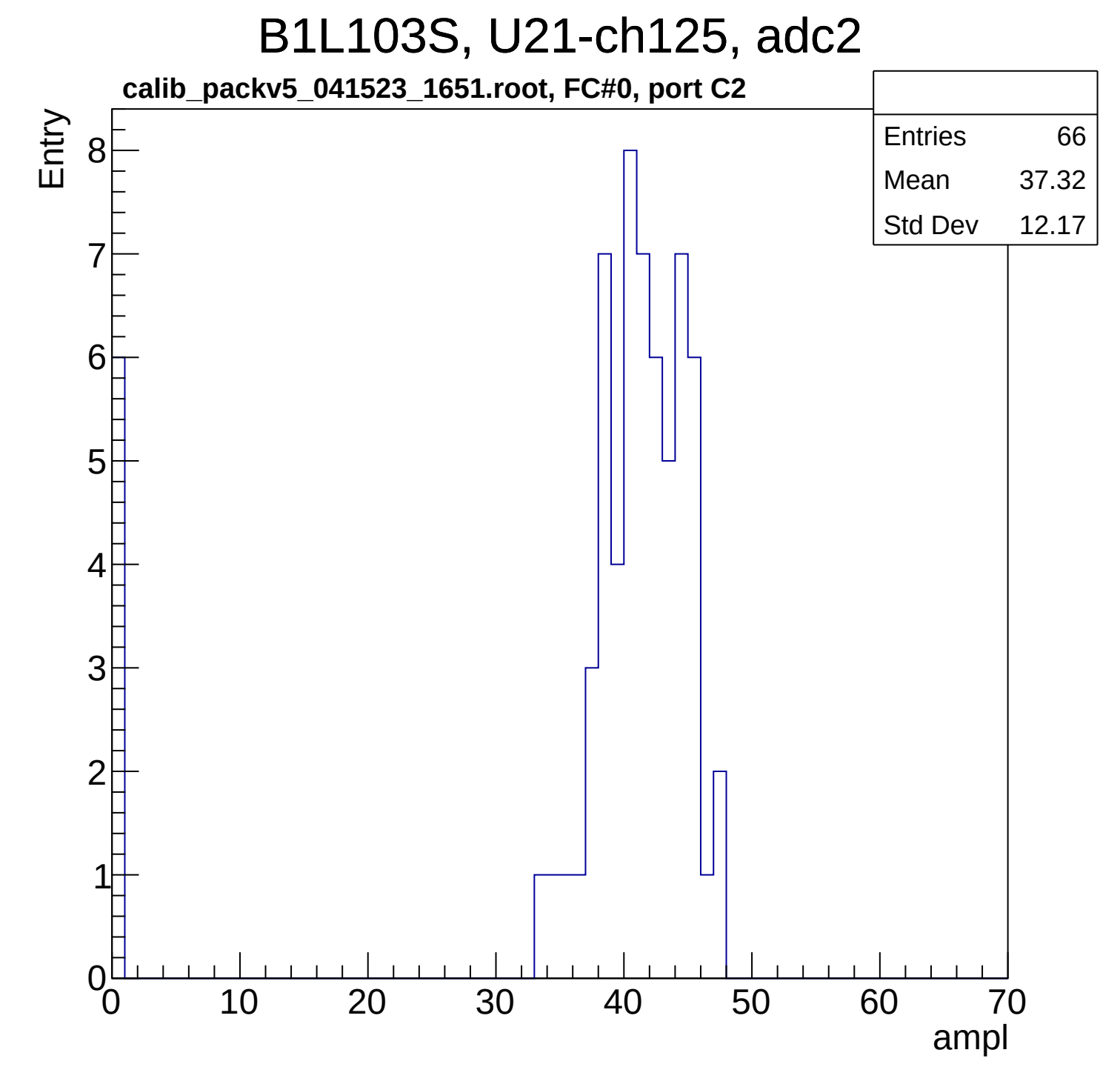
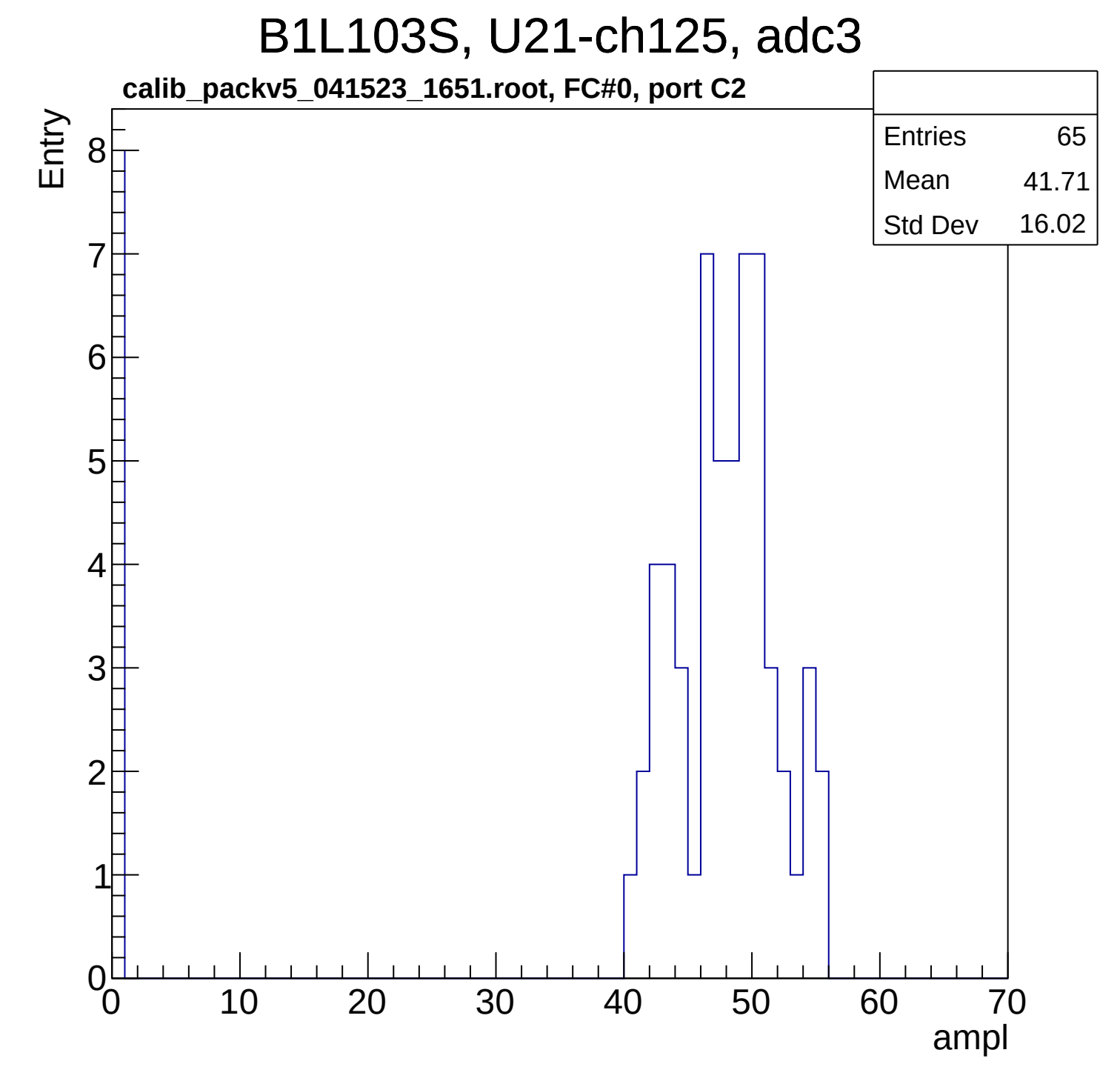

B1L103S, U21-ch125, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 37.32
Std Dev 12.17
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch125, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 41.71
Std Dev 16.02
Entry
ampl
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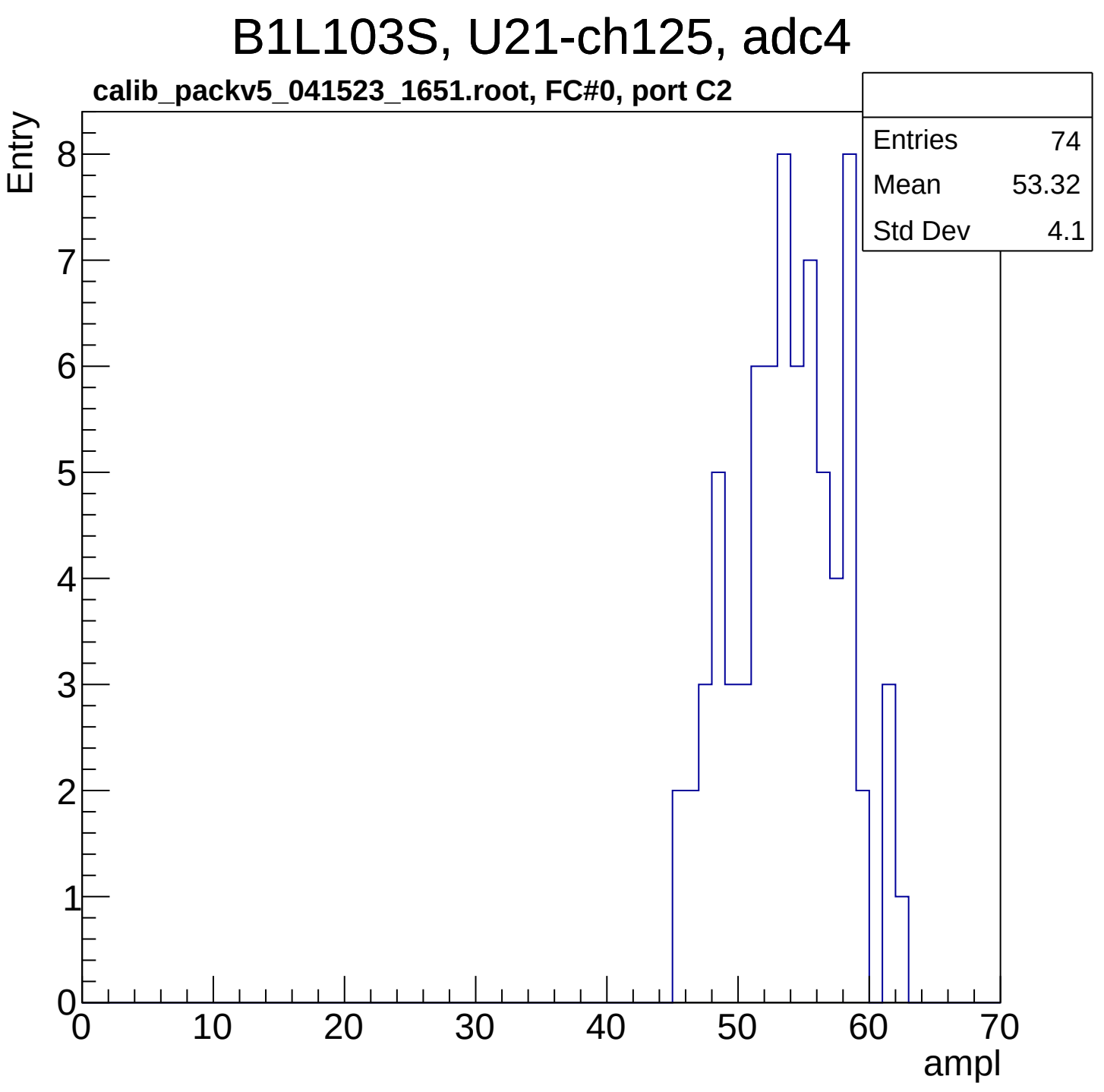
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch125, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 53.32
Std Dev 4.1
Entry
ampl
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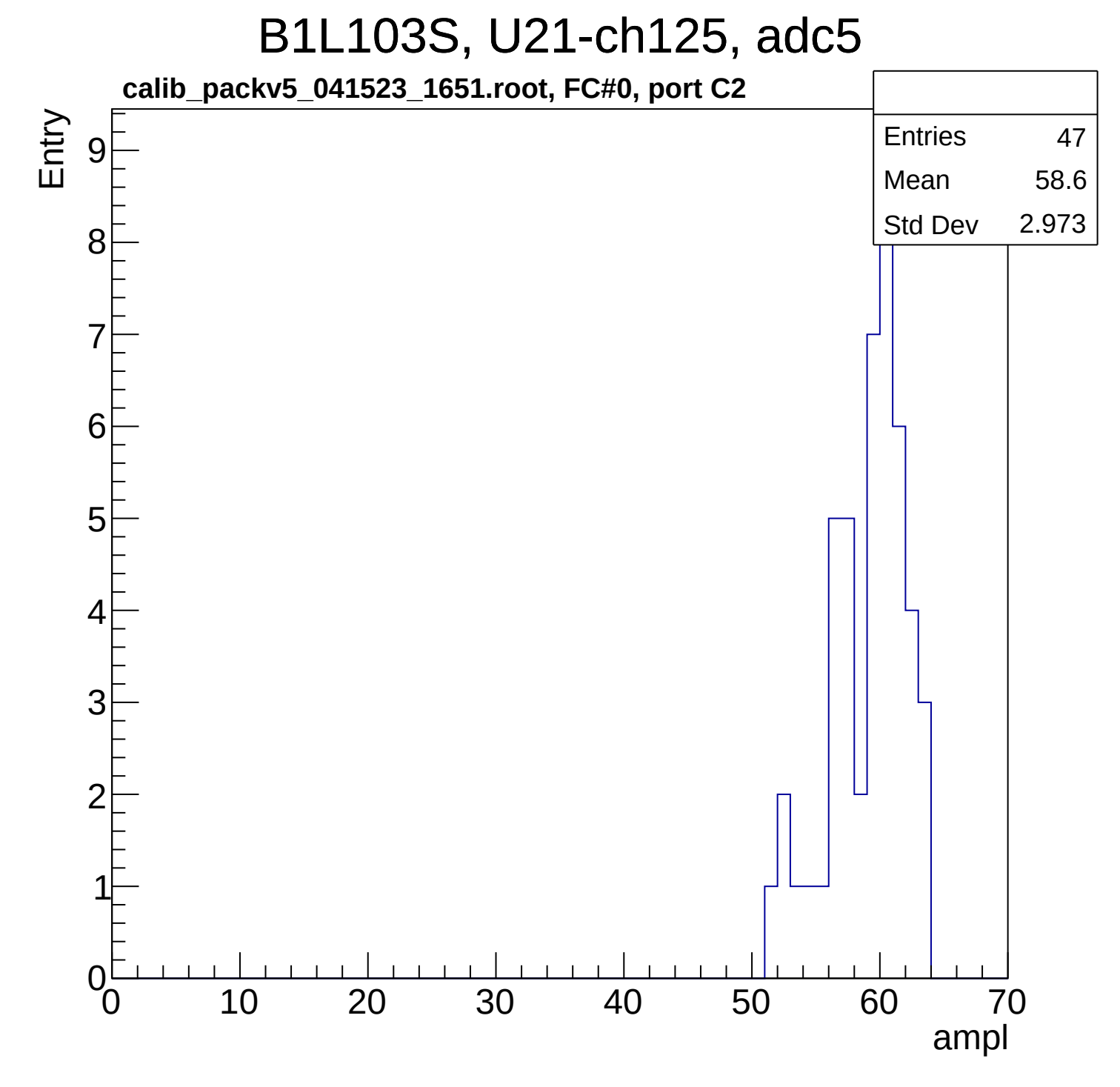
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch125, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 58.6
Std Dev 2.973
Entry
ampl
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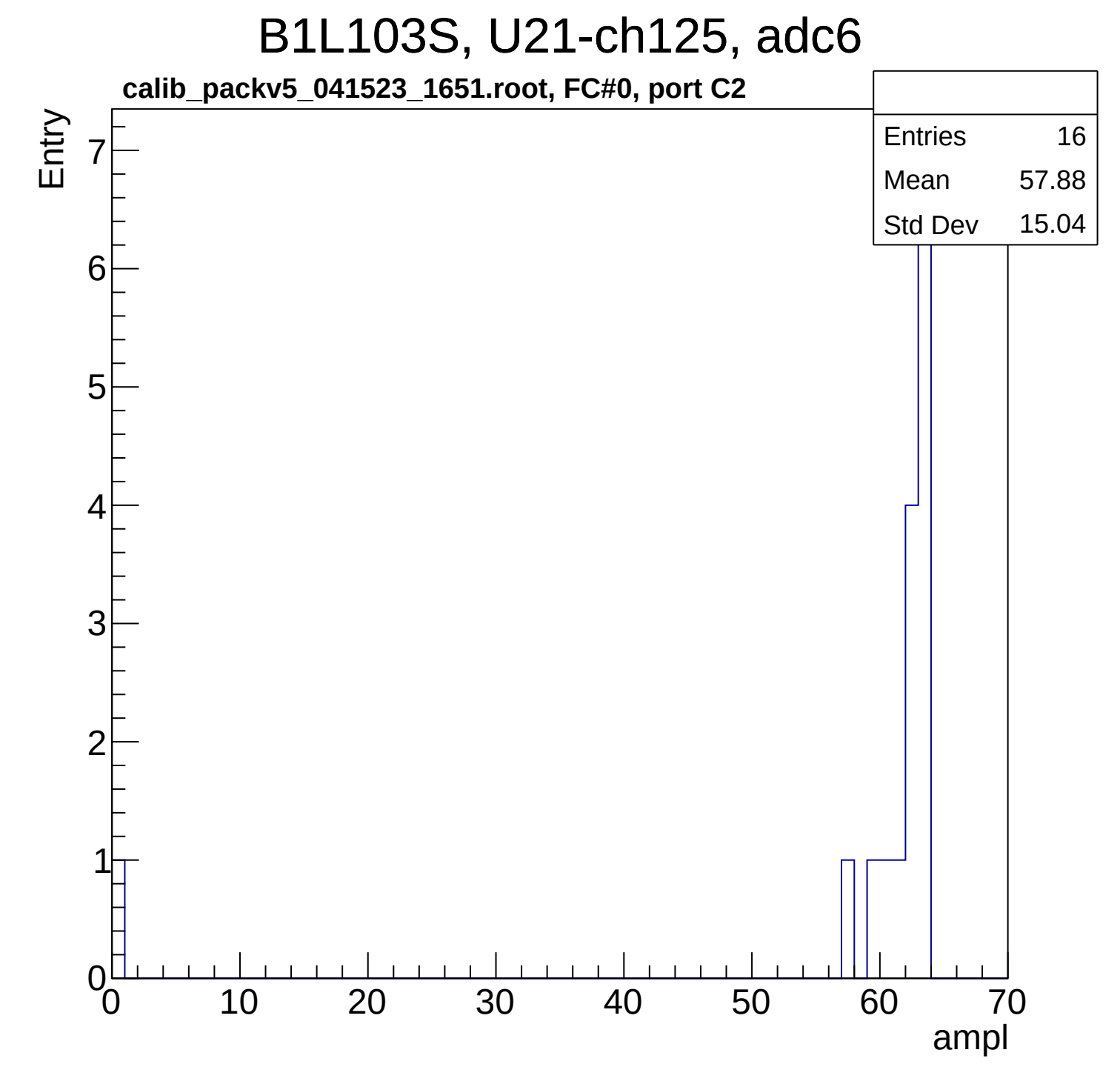
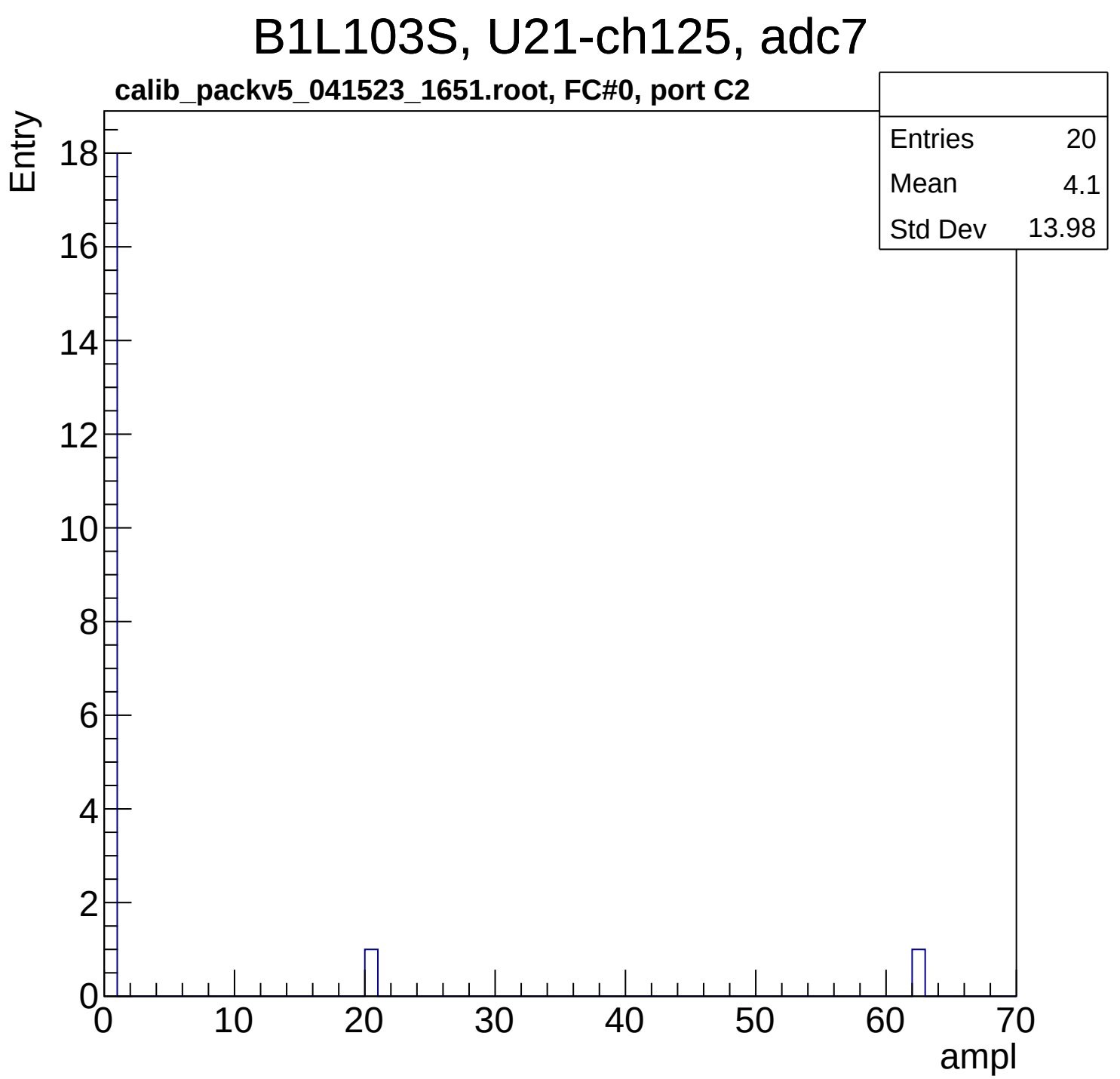
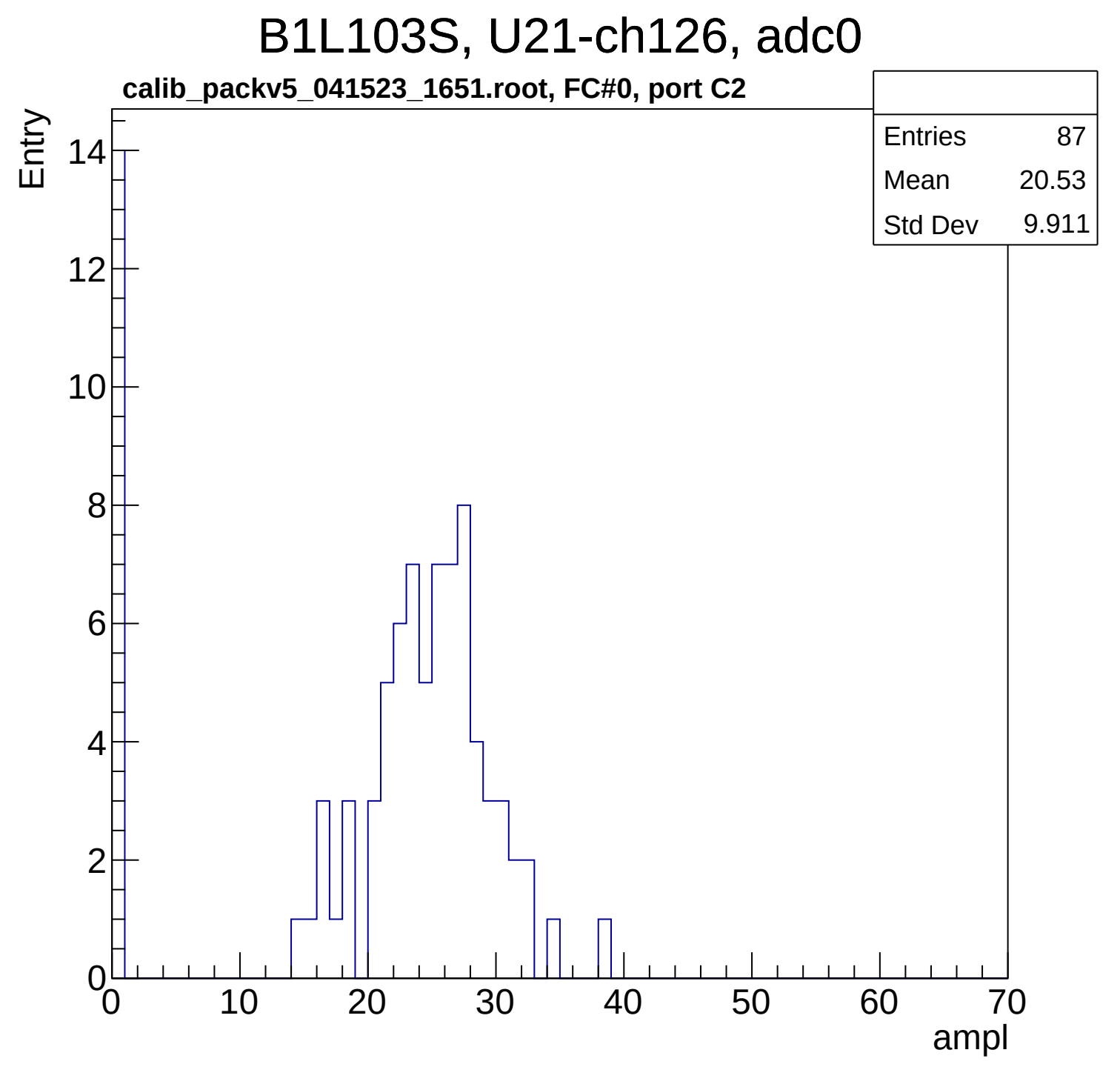
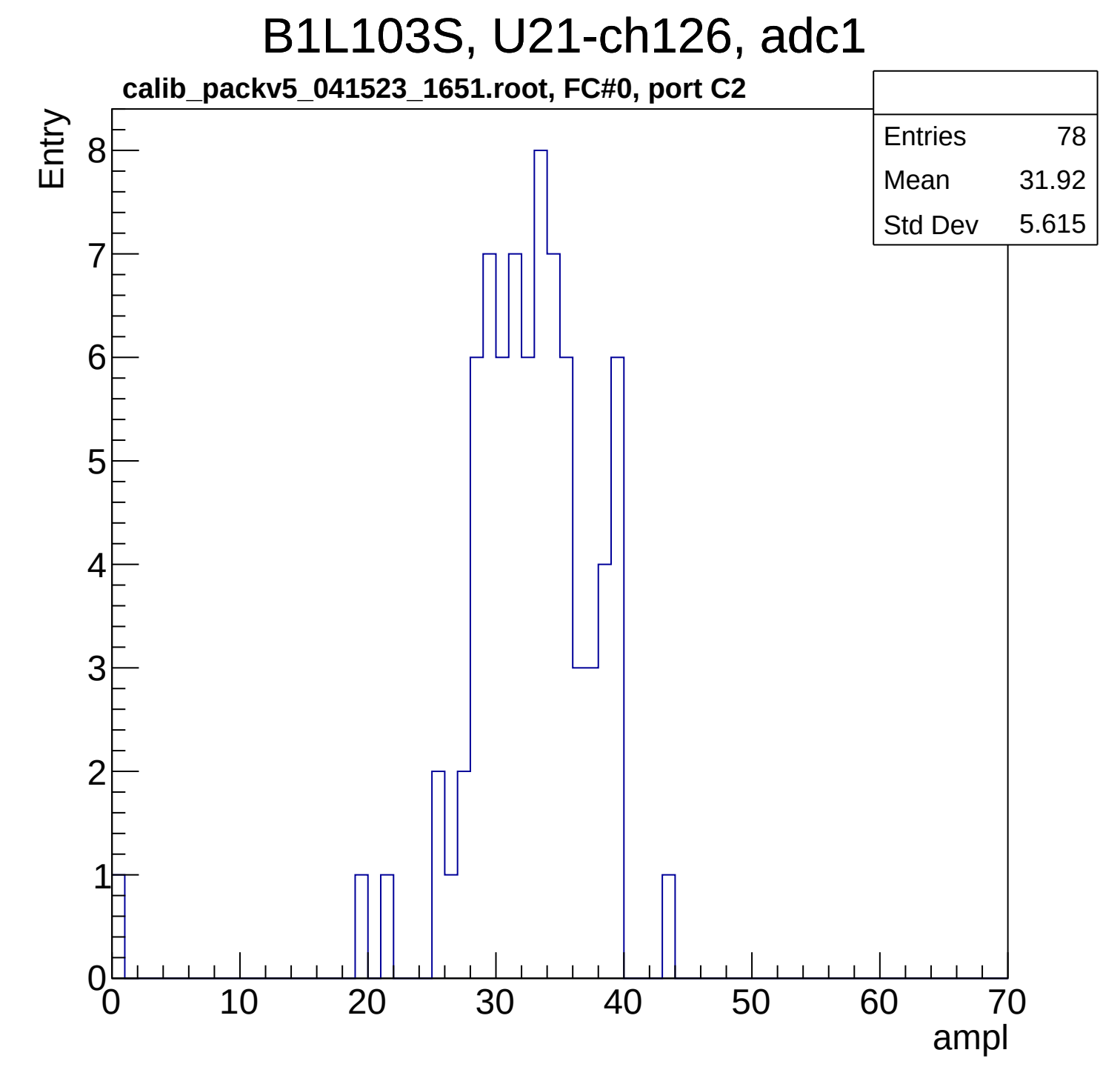
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch125, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 57.88
Std Dev 15.04
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U21-ch125, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4.1
Std Dev 13.98
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch126, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 20.53
Std Dev 9.911
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U21-ch126, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 31.92
Std Dev 5.615
Entry
ampl
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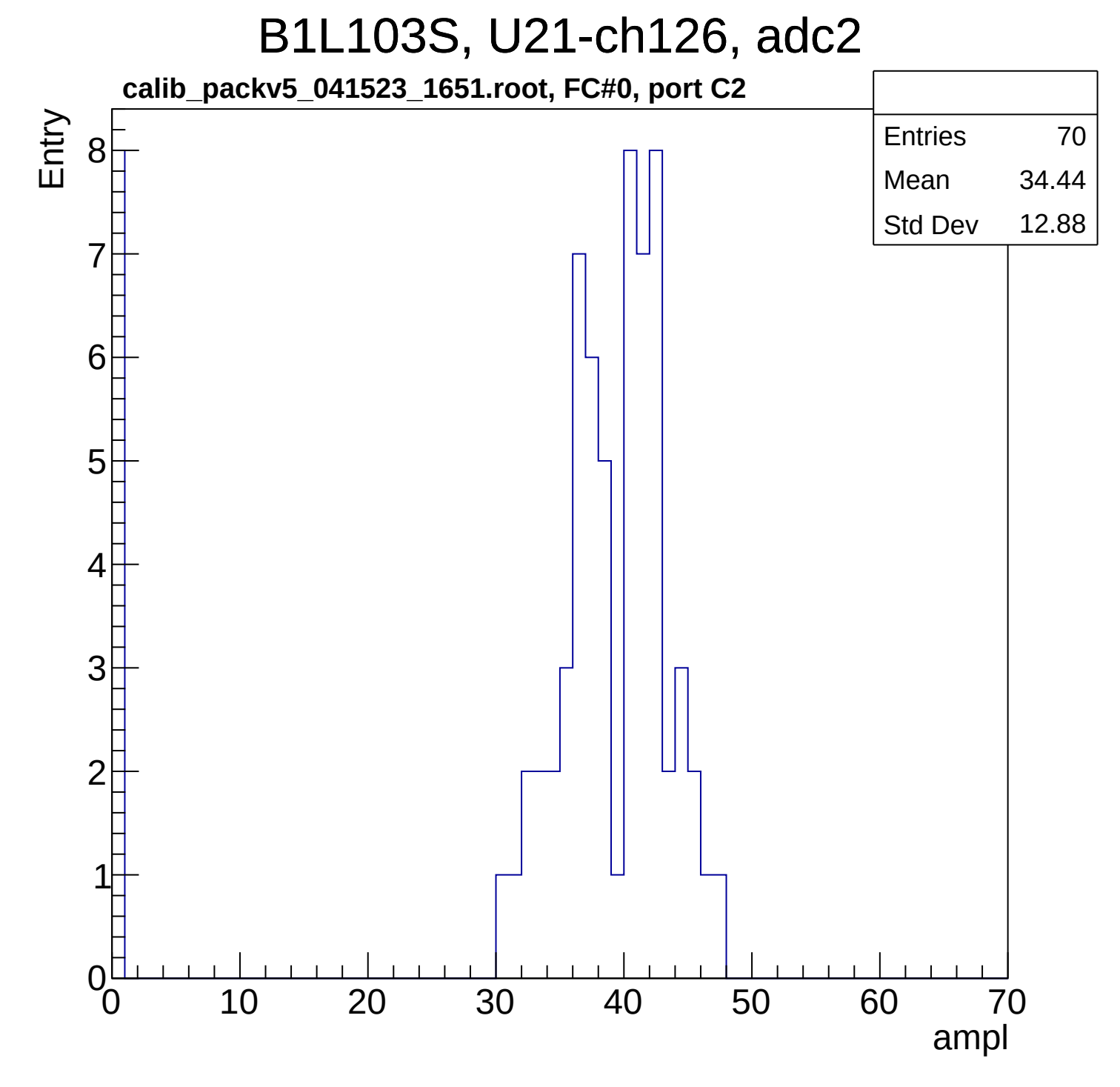
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch126, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 34.44
Std Dev 12.88
Entry
ampl
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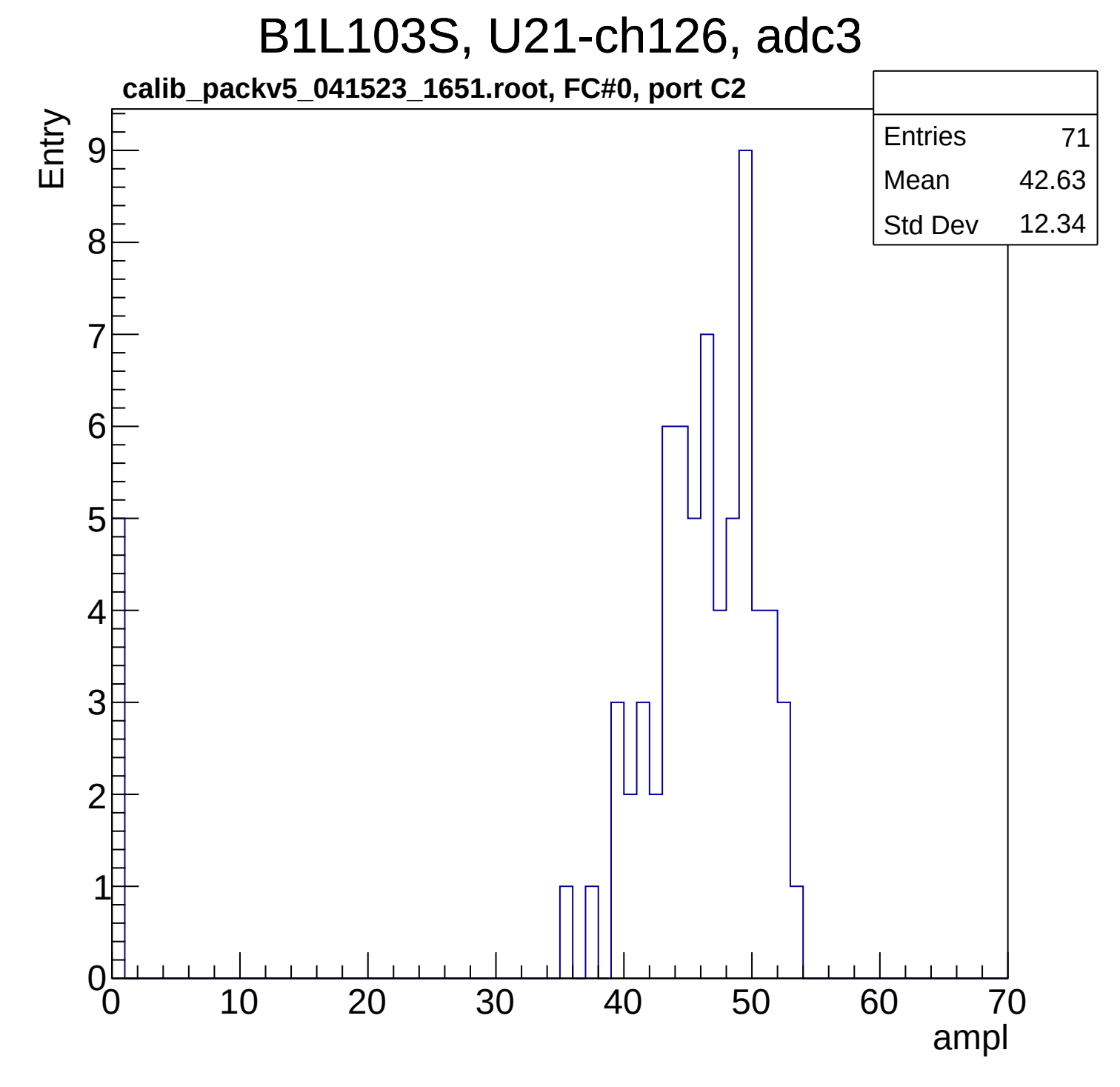
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U21-ch126, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 42.63
Std Dev 12.34
Entry
ampl
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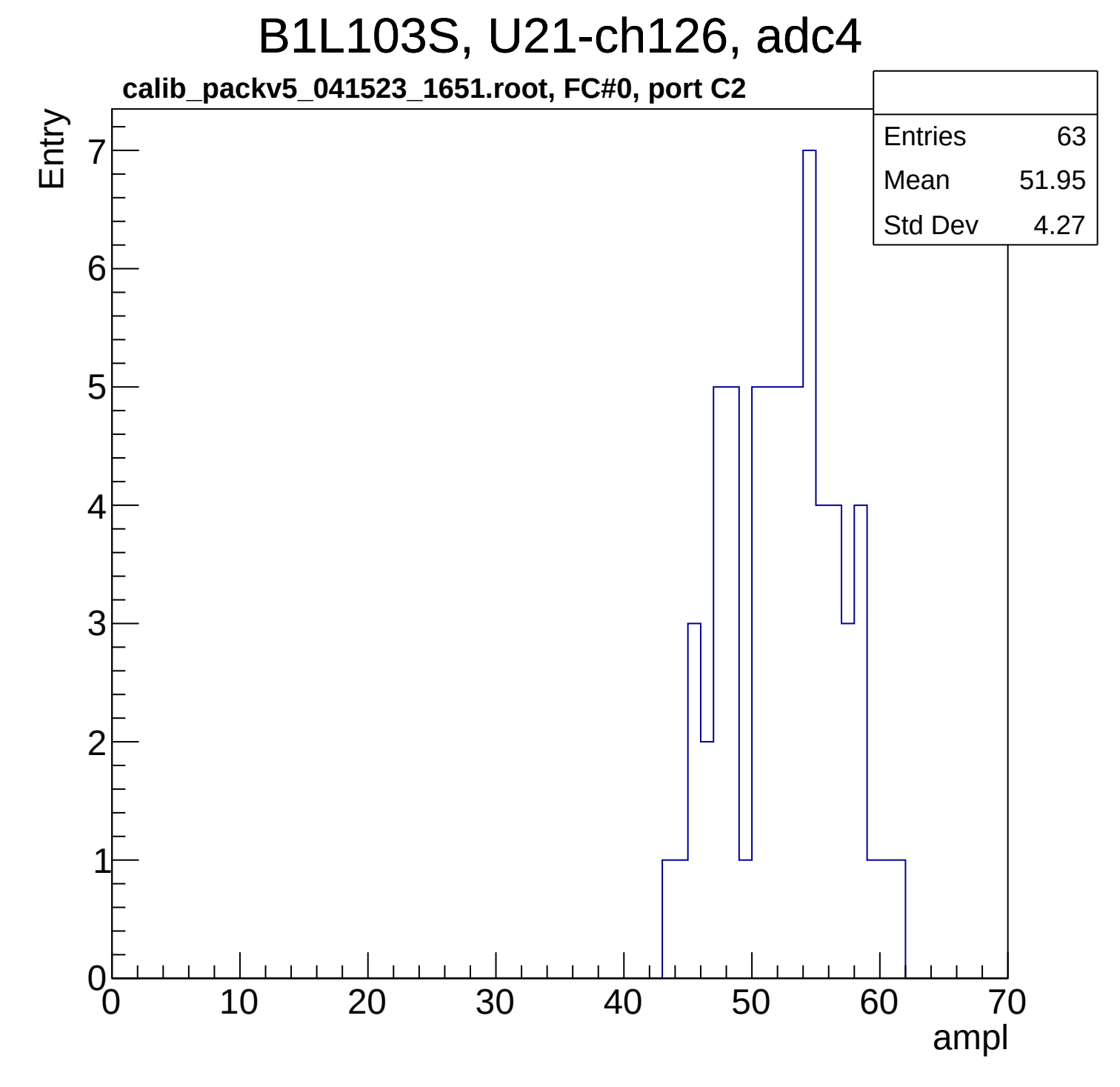
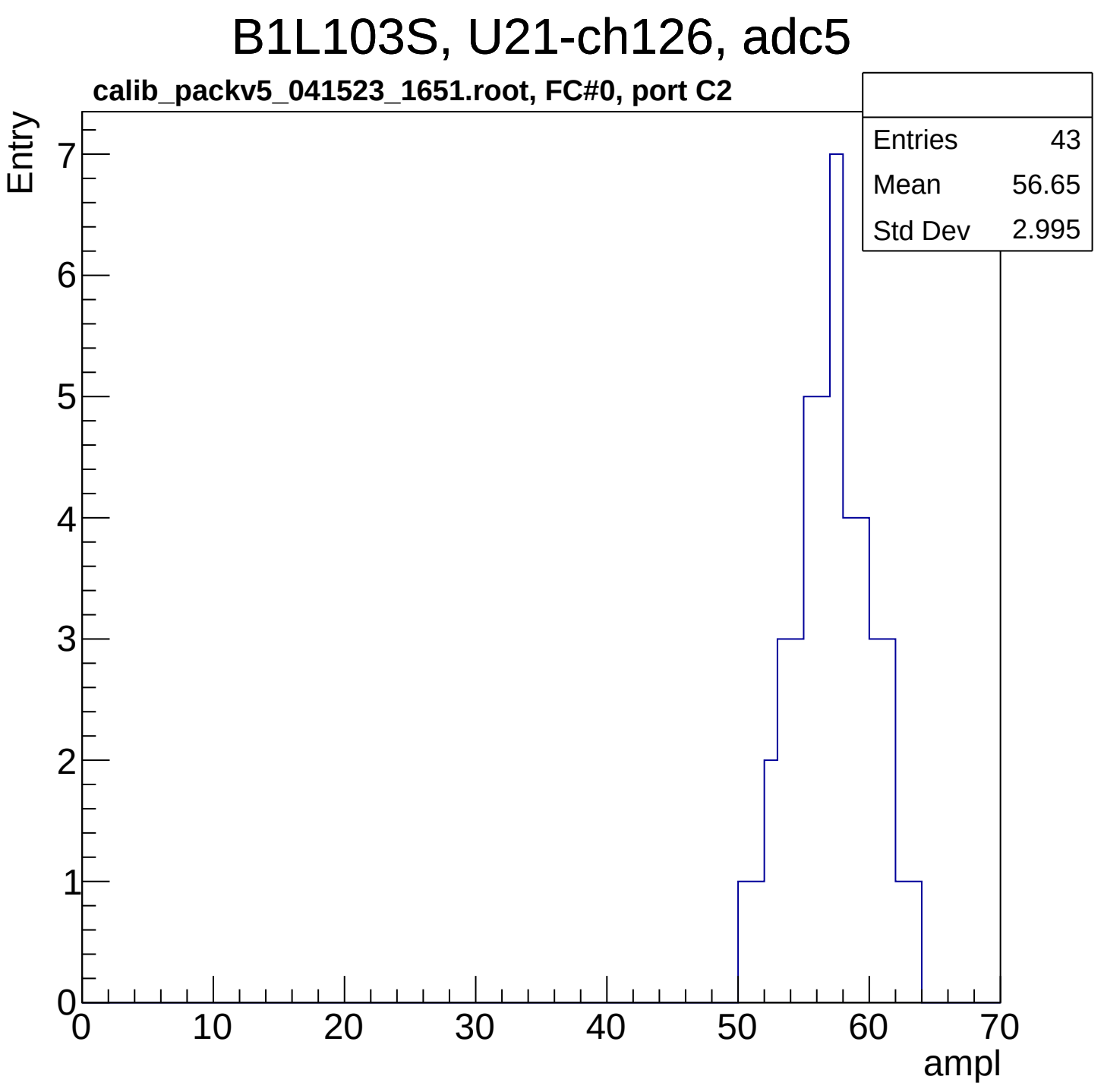
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U21-ch126, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 51.95
Std Dev 4.27
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U21-ch126, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 56.65
Std Dev 2.995
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
50
60
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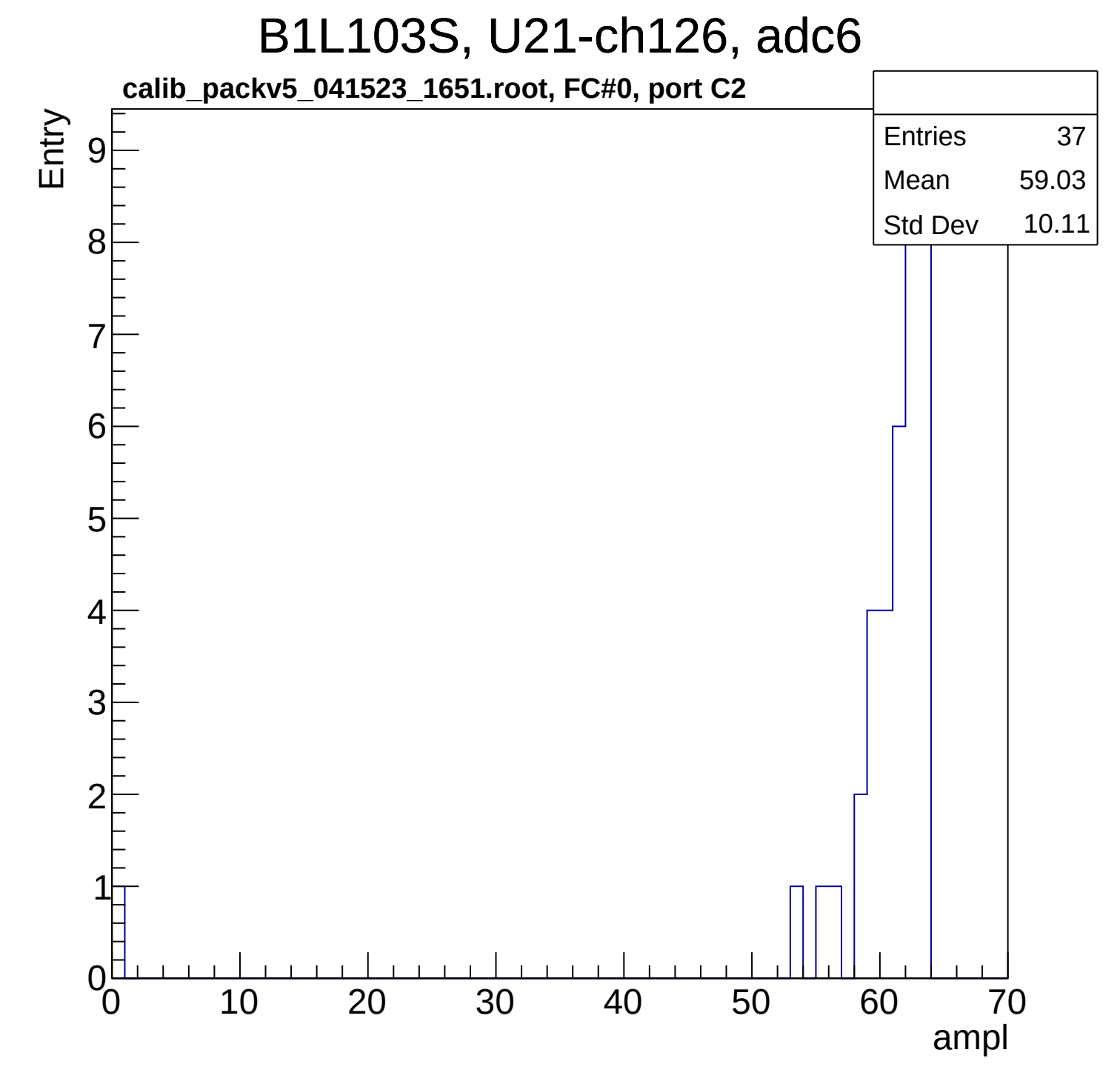
B1L103S, U21-ch126, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 59.03
Std Dev 10.11
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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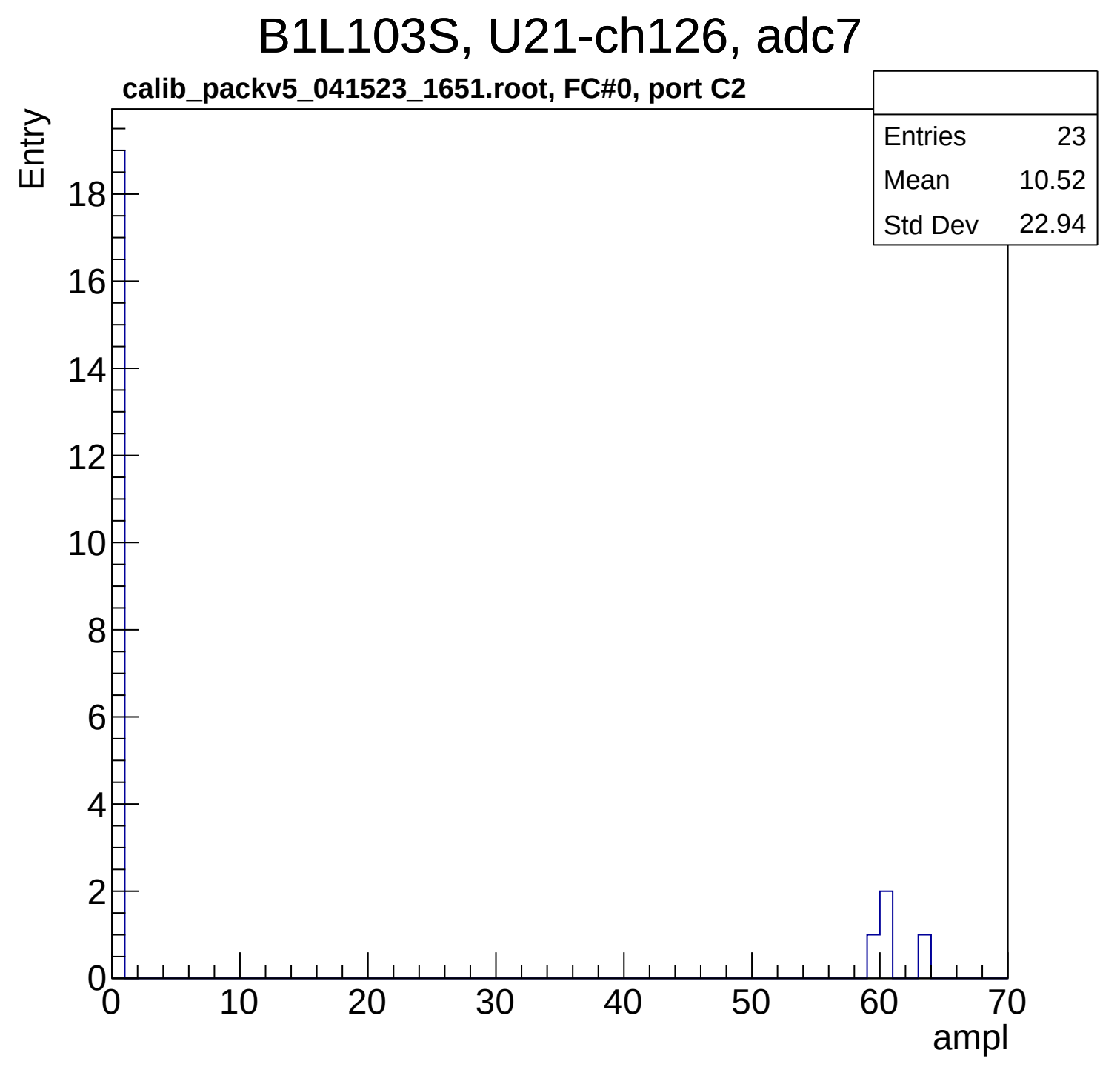
40
50
60
70


B1L103S, U21-ch126, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 10.52
Std Dev 22.94
Entry
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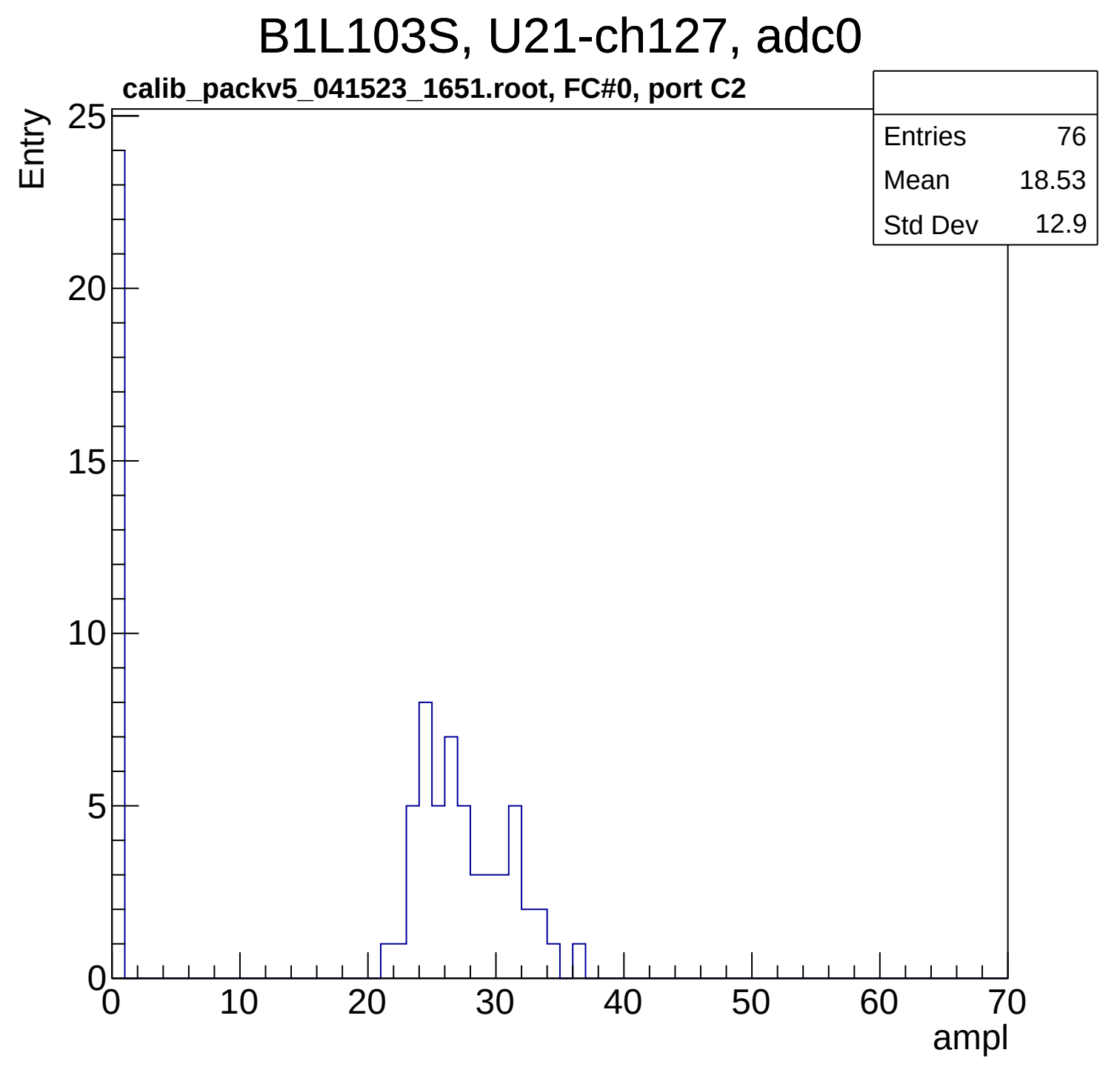
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch127, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 18.53
Std Dev 12.9
Entry
ampl
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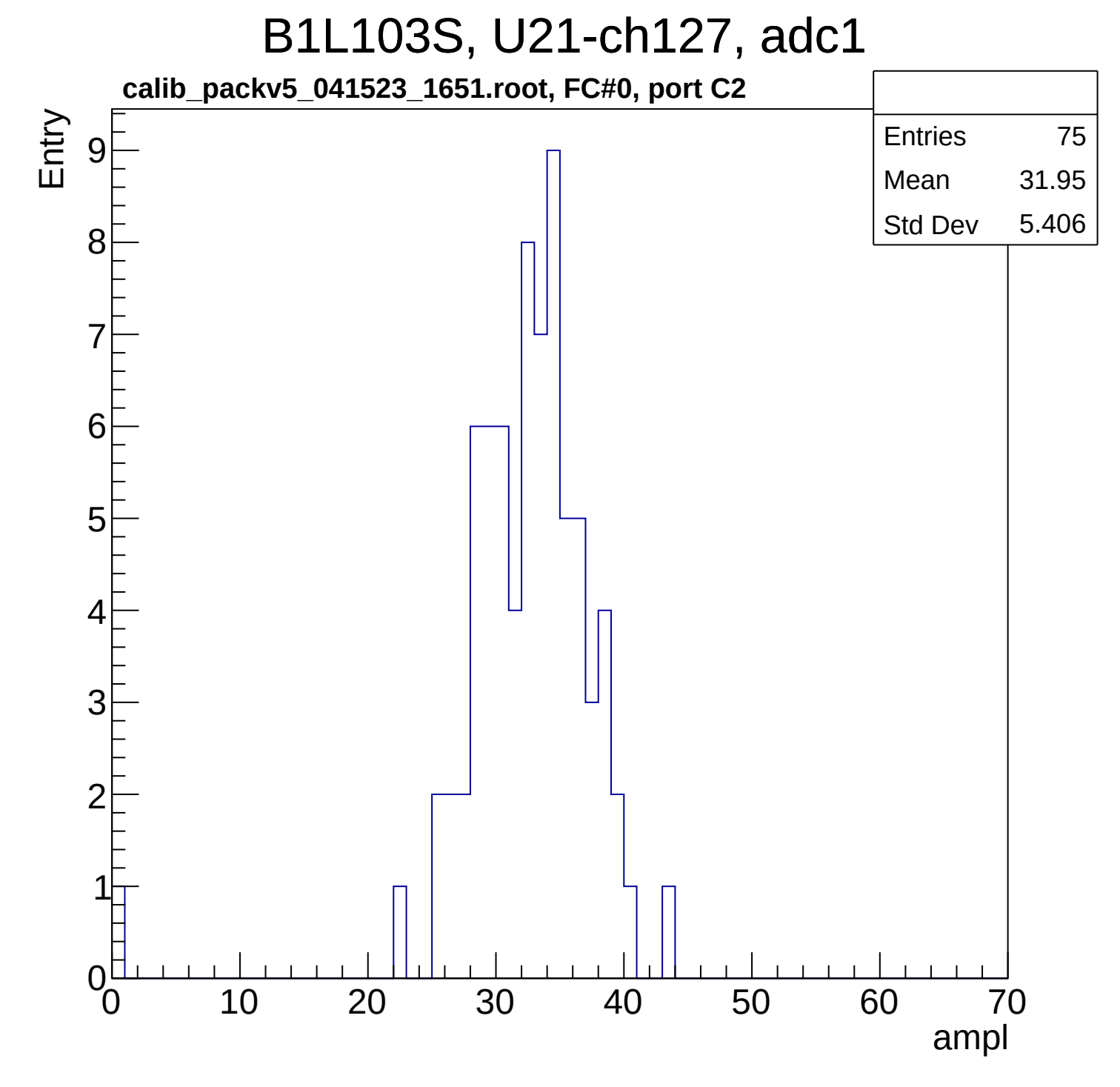
5
10
15
20
25
0
10
20
30
40
50
60
70


B1L103S, U21-ch127, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 31.95
Std Dev 5.406
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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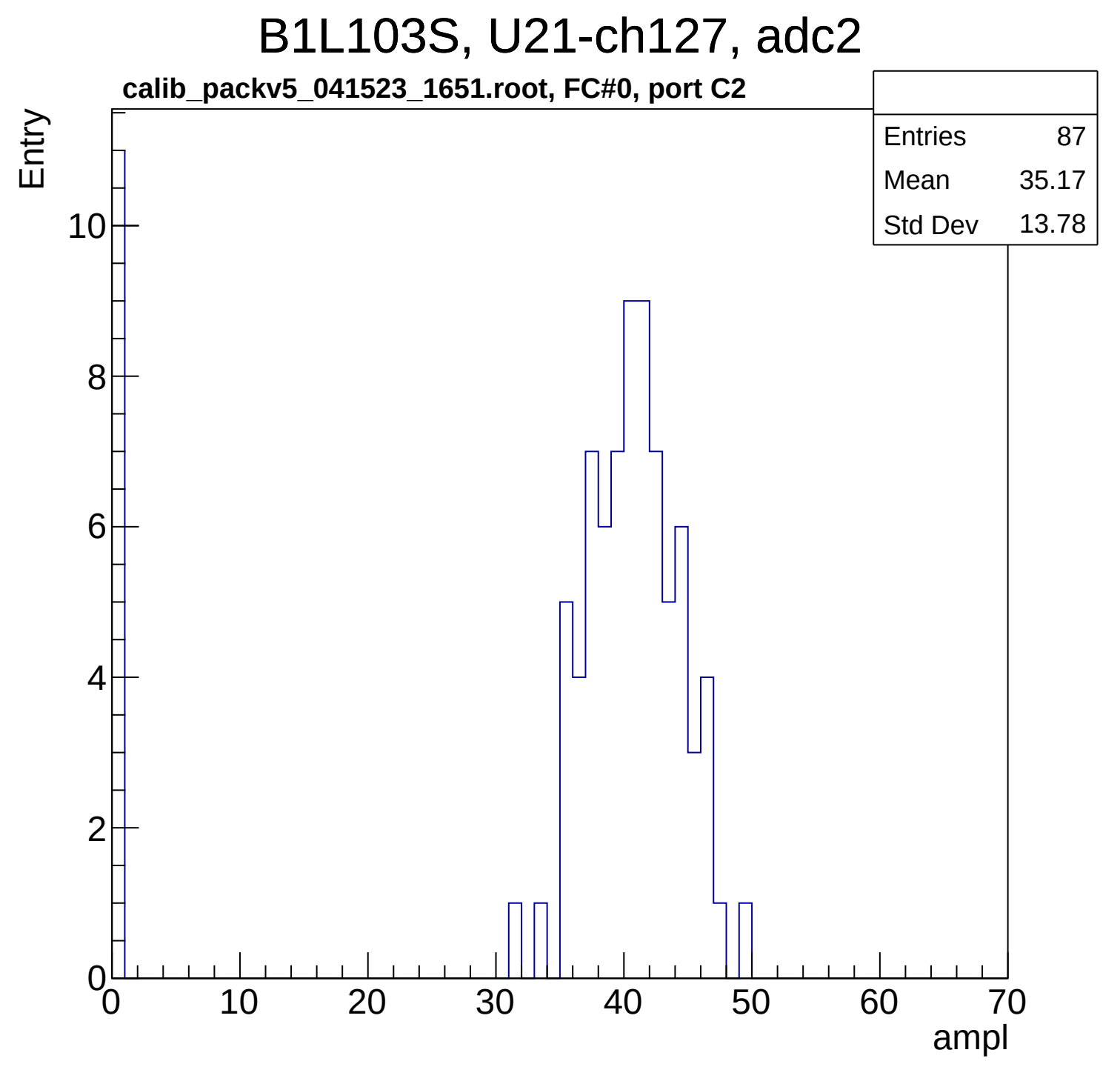
40
50
60
70


B1L103S, U21-ch127, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 35.17
Std Dev 13.78
Entry
0
2
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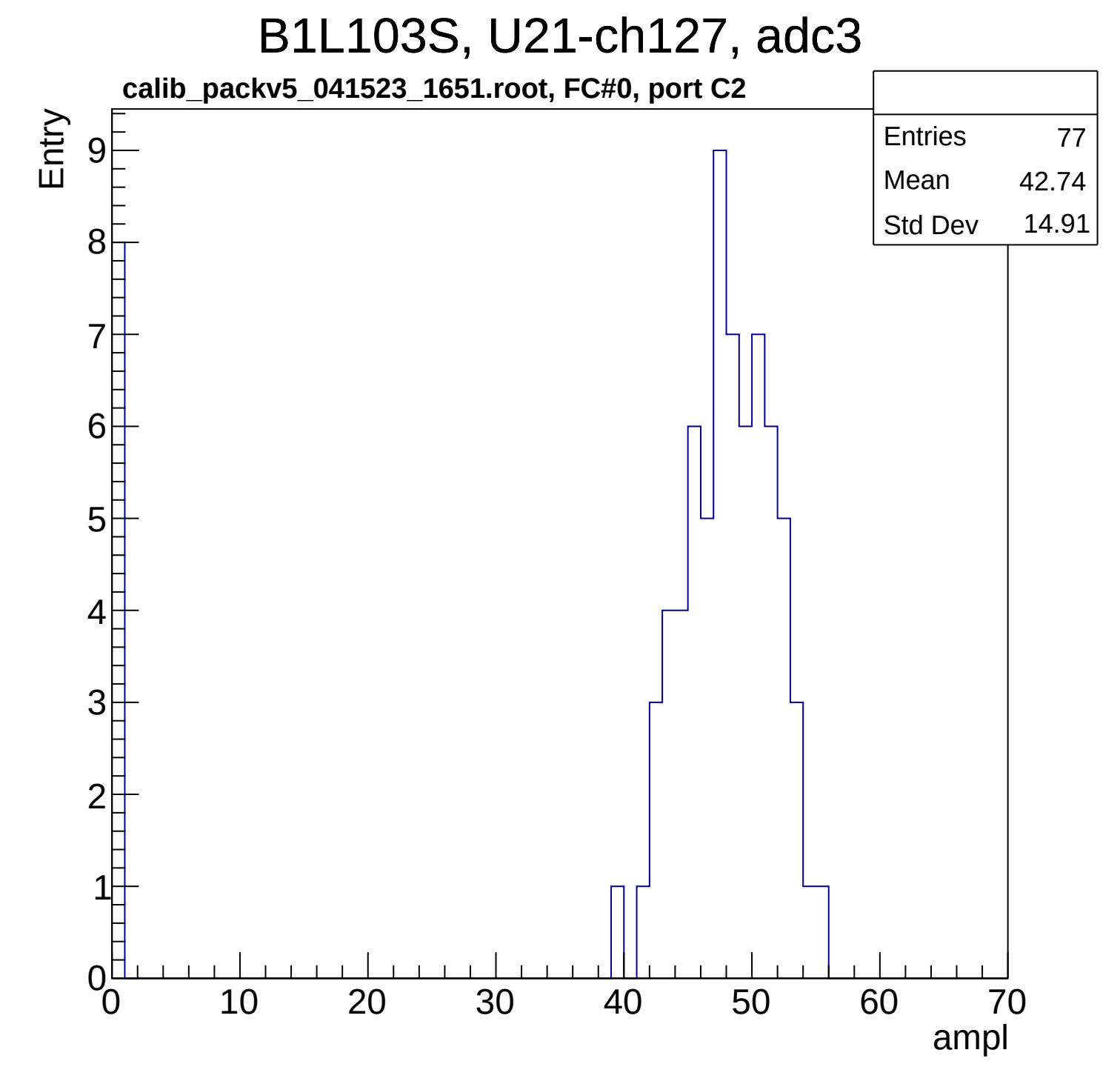
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch127, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 42.74
Std Dev 14.91
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
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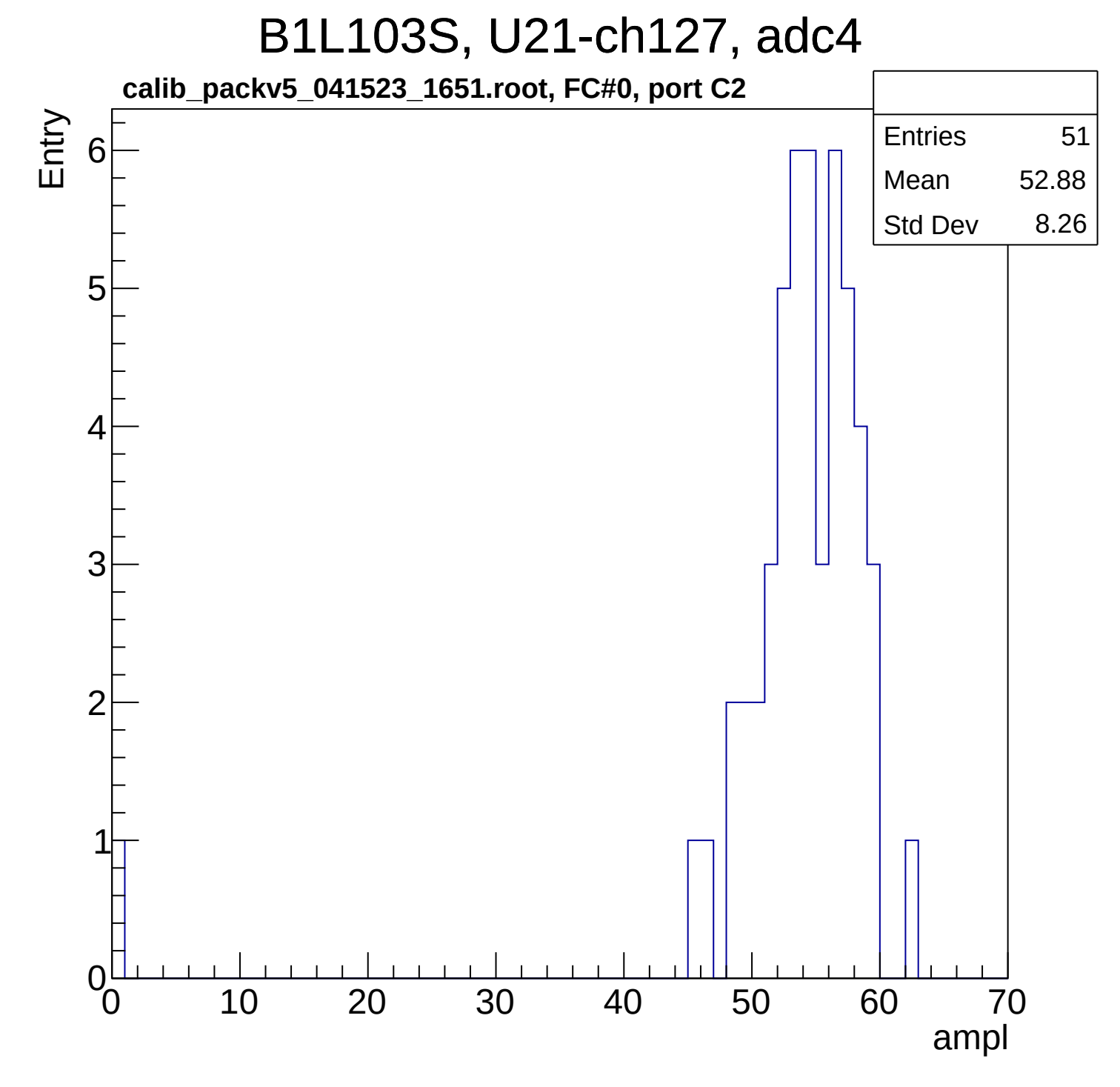
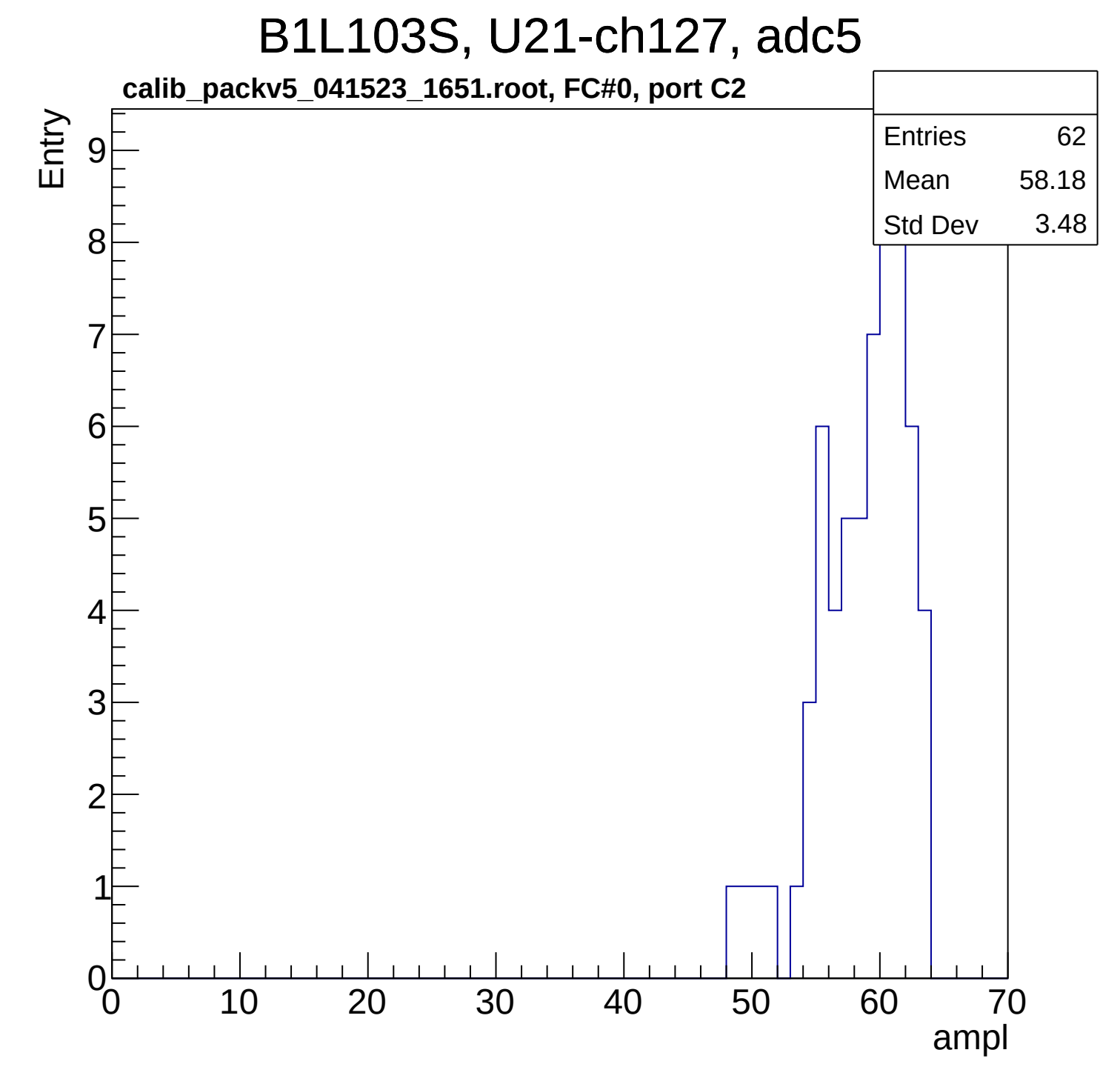
60
70


B1L103S, U21-ch127, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 52.88
Std Dev 8.26
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U21-ch127, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 58.18
Std Dev 3.48
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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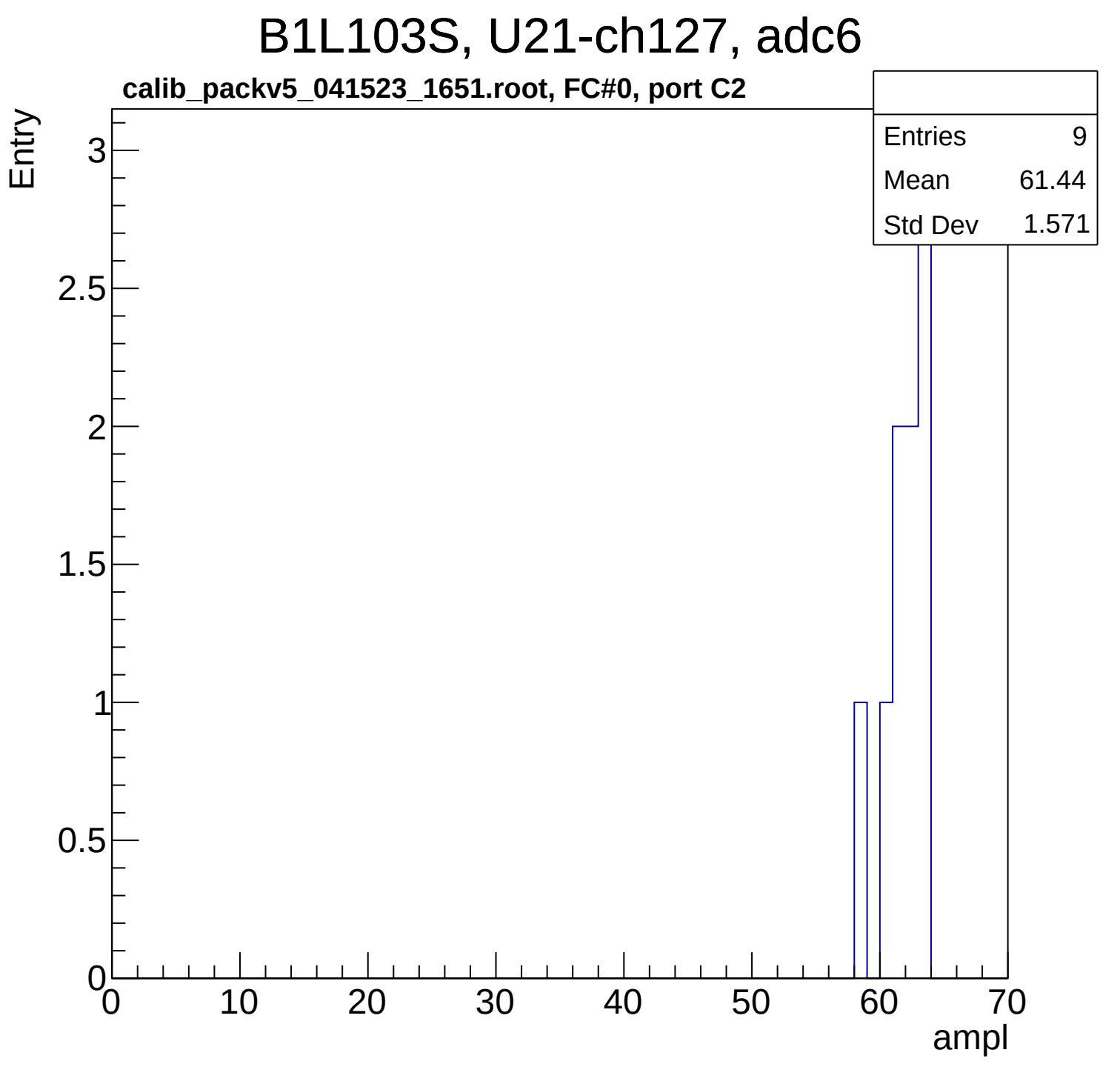
60
70


B1L103S, U21-ch127, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 61.44
Std Dev 1.571
Entry
ampl
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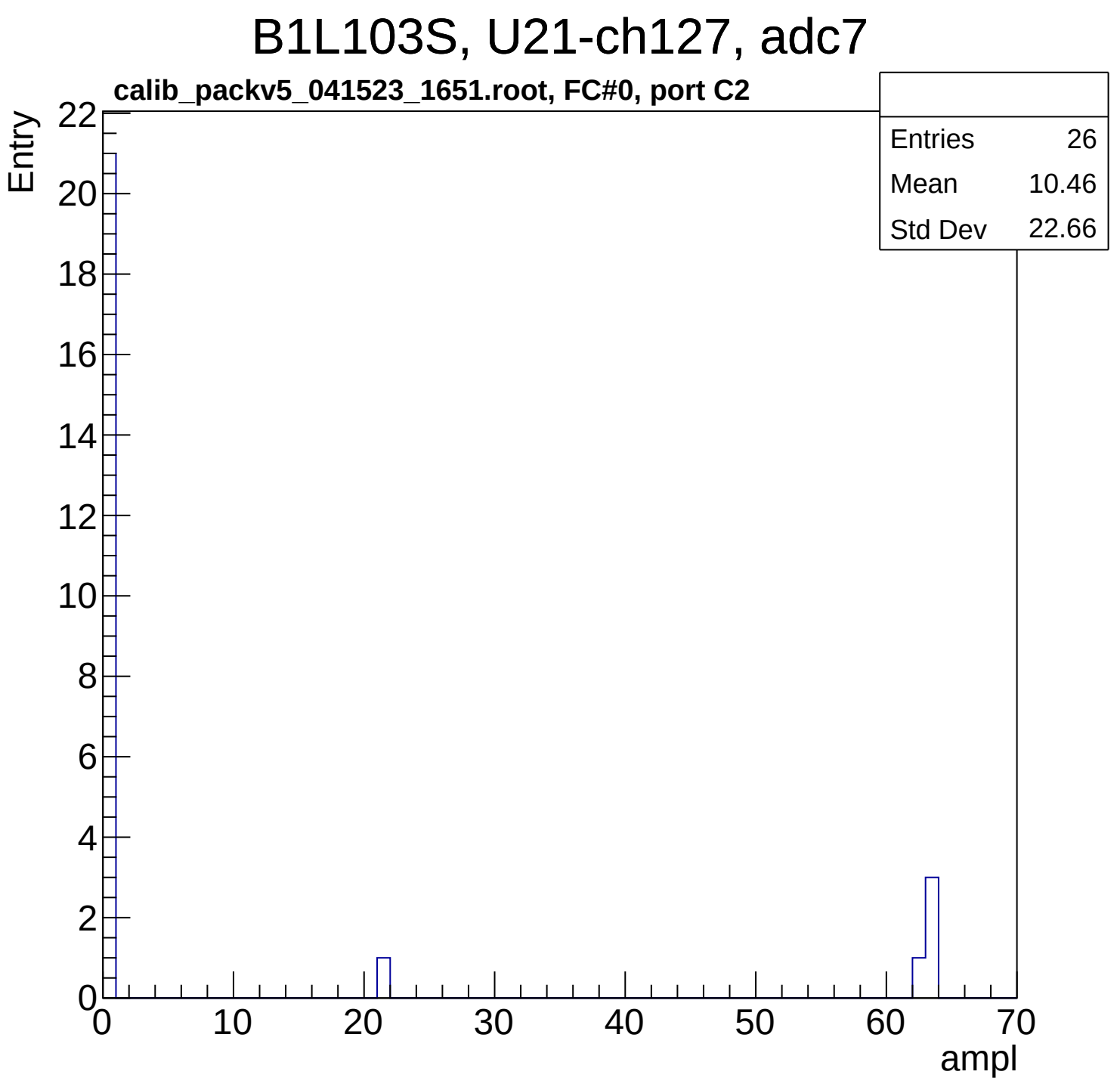
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U21-ch127, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 10.46
Std Dev 22.66
Entry
ampl
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2
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6
8
10
12
14
16
18
20
22
0
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20
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40
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60
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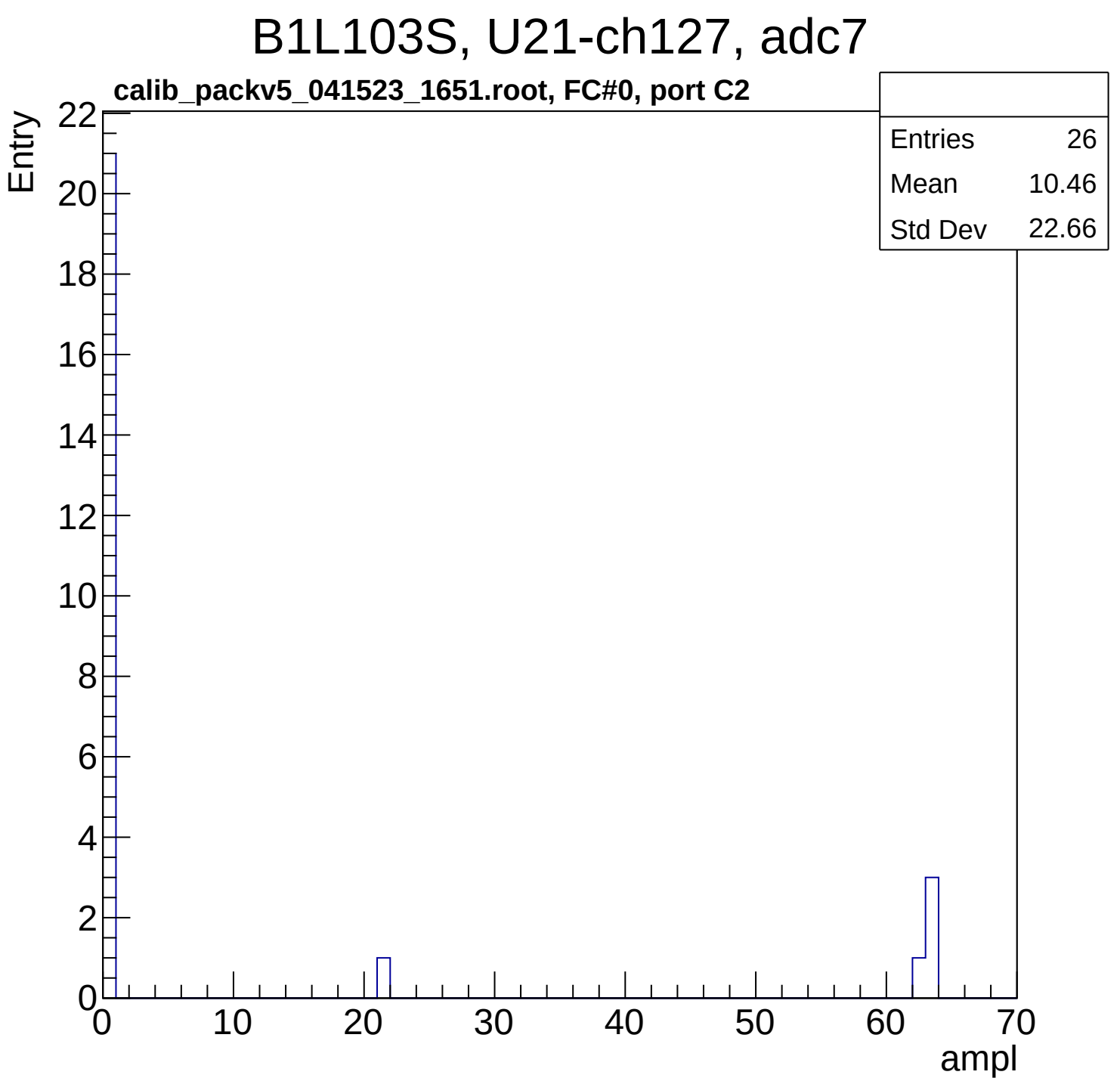
B1L103S, U21-ch127, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 10.46
Std Dev 22.66
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70