



# B1L000S, U7-ch0

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	392
Mean	43.71
Std Dev	11.69

**Turn on : 24.9358**

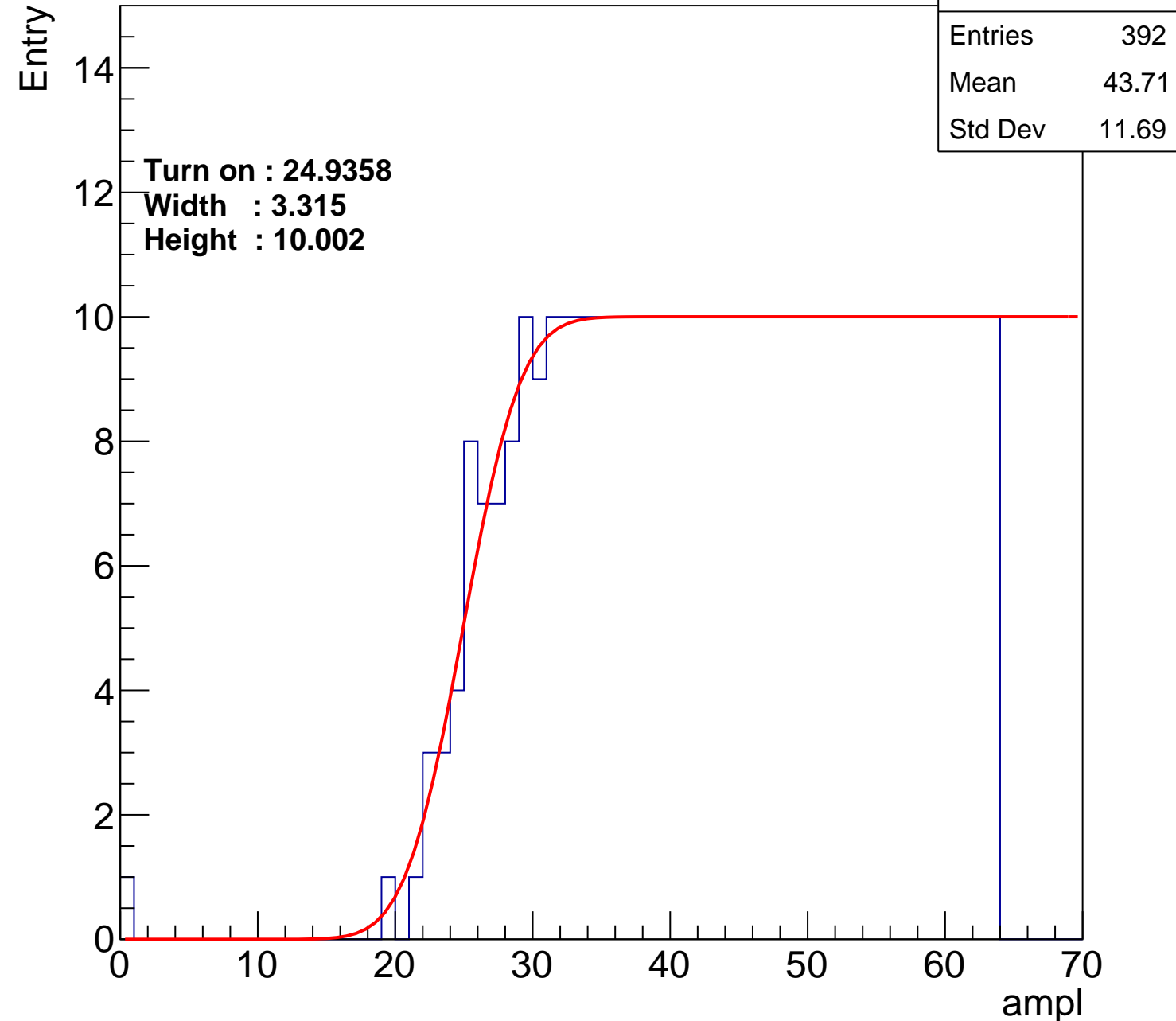
**Width : 3.315**

**Height : 10.002**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch1

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	393
Mean	43.44
Std Dev	12.33

Turn on : 25.6960

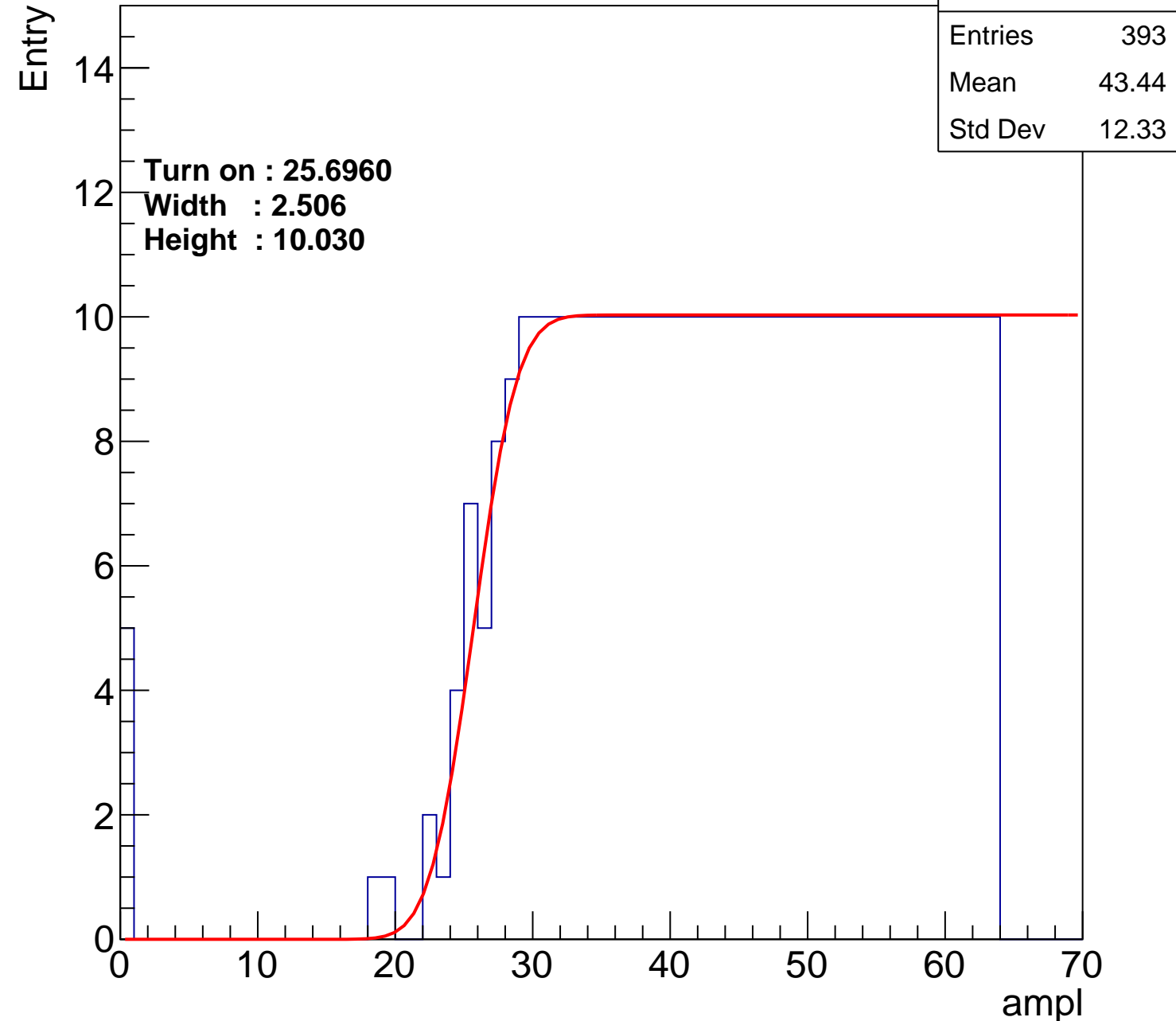
Width : 2.506

Height : 10.030

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch2

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	397
Mean	43.46
Std Dev	11.9

**Turn on : 24.5297**

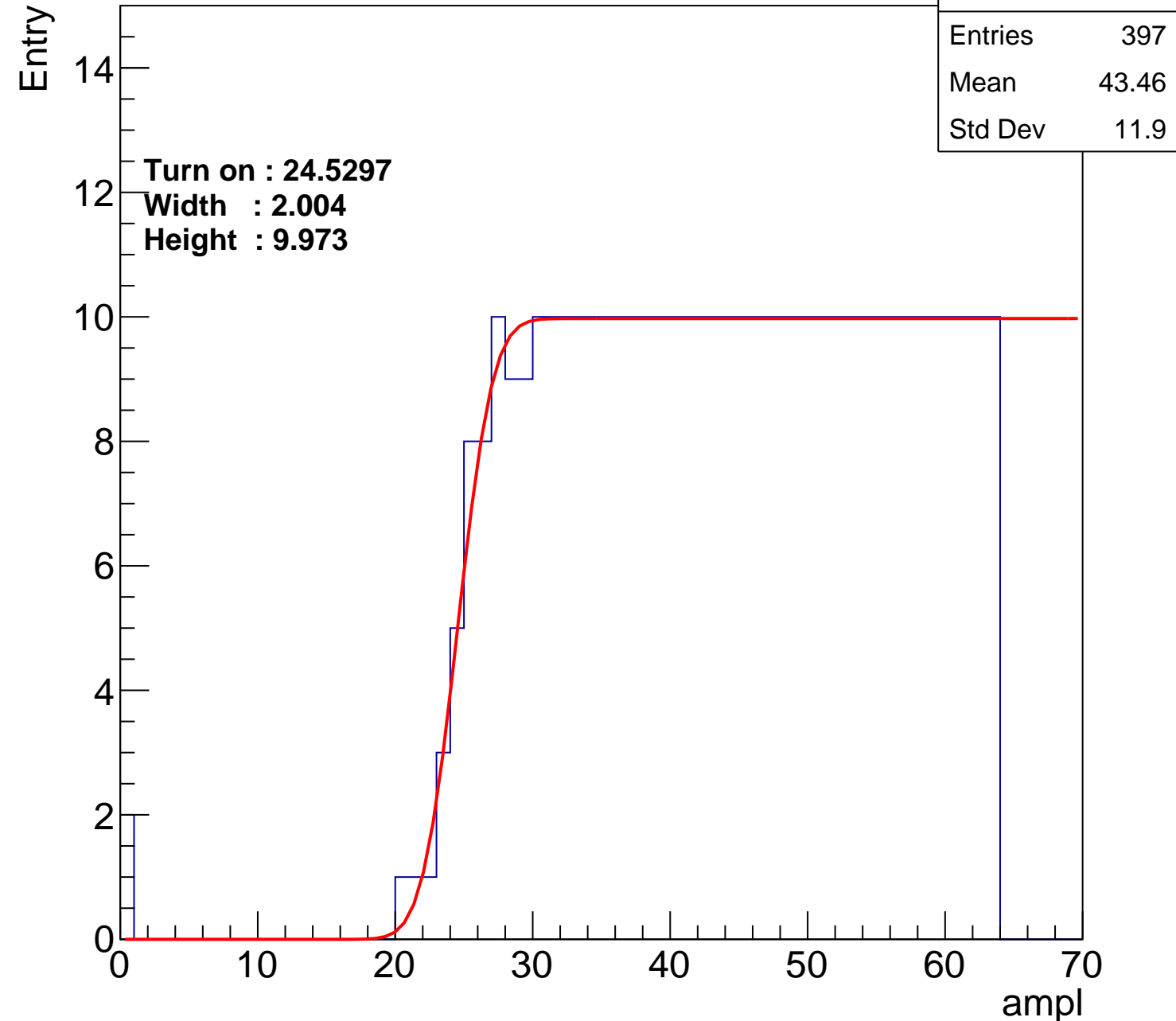
**Width : 2.004**

**Height : 9.973**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch3

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	378
Mean	44.39
Std Dev	11.42

Turn on : 26.5223

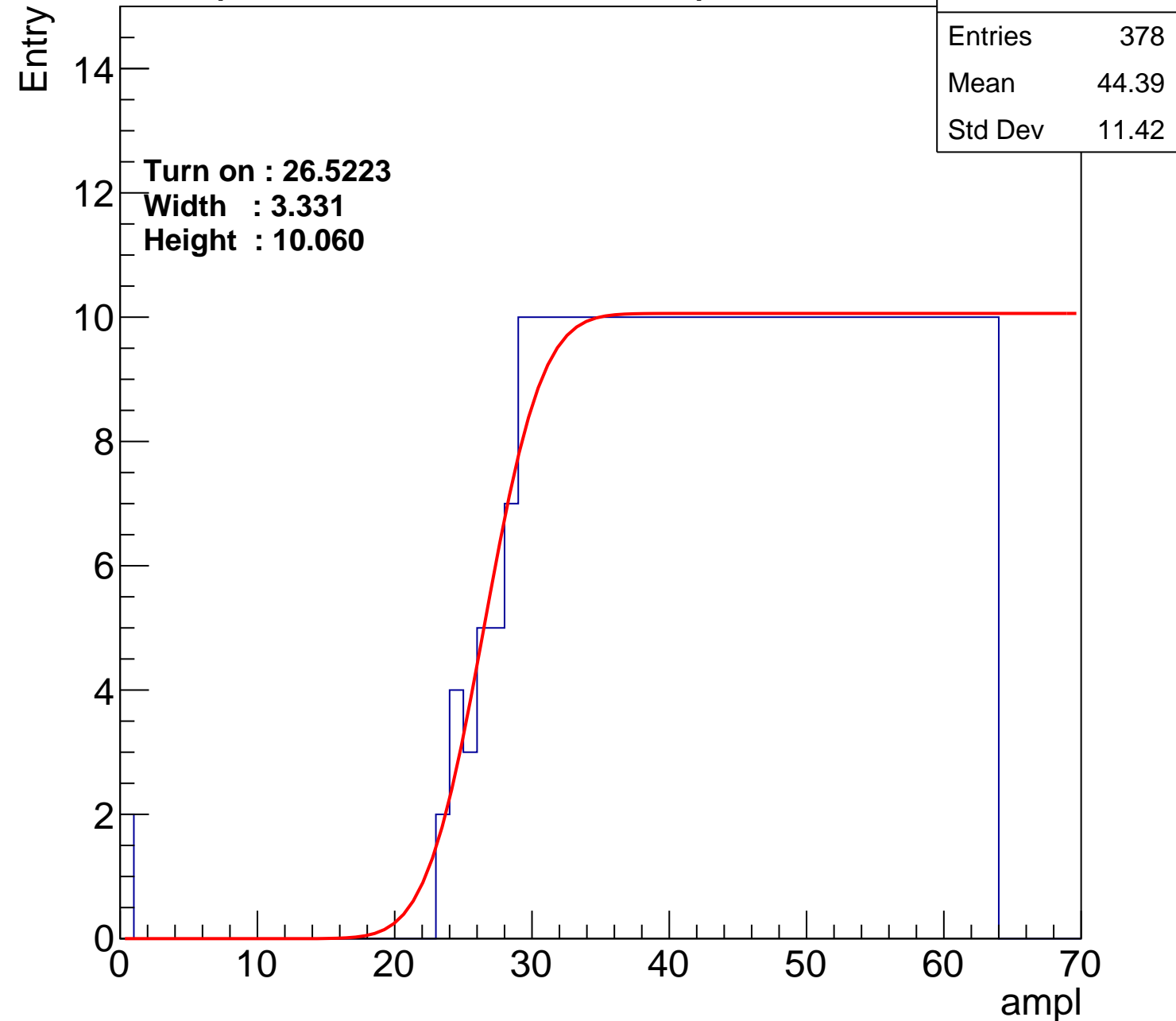
Width : 3.331

Height : 10.060

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch4

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	389
Mean	43.78
Std Dev	11.81

Turn on : 25.5964

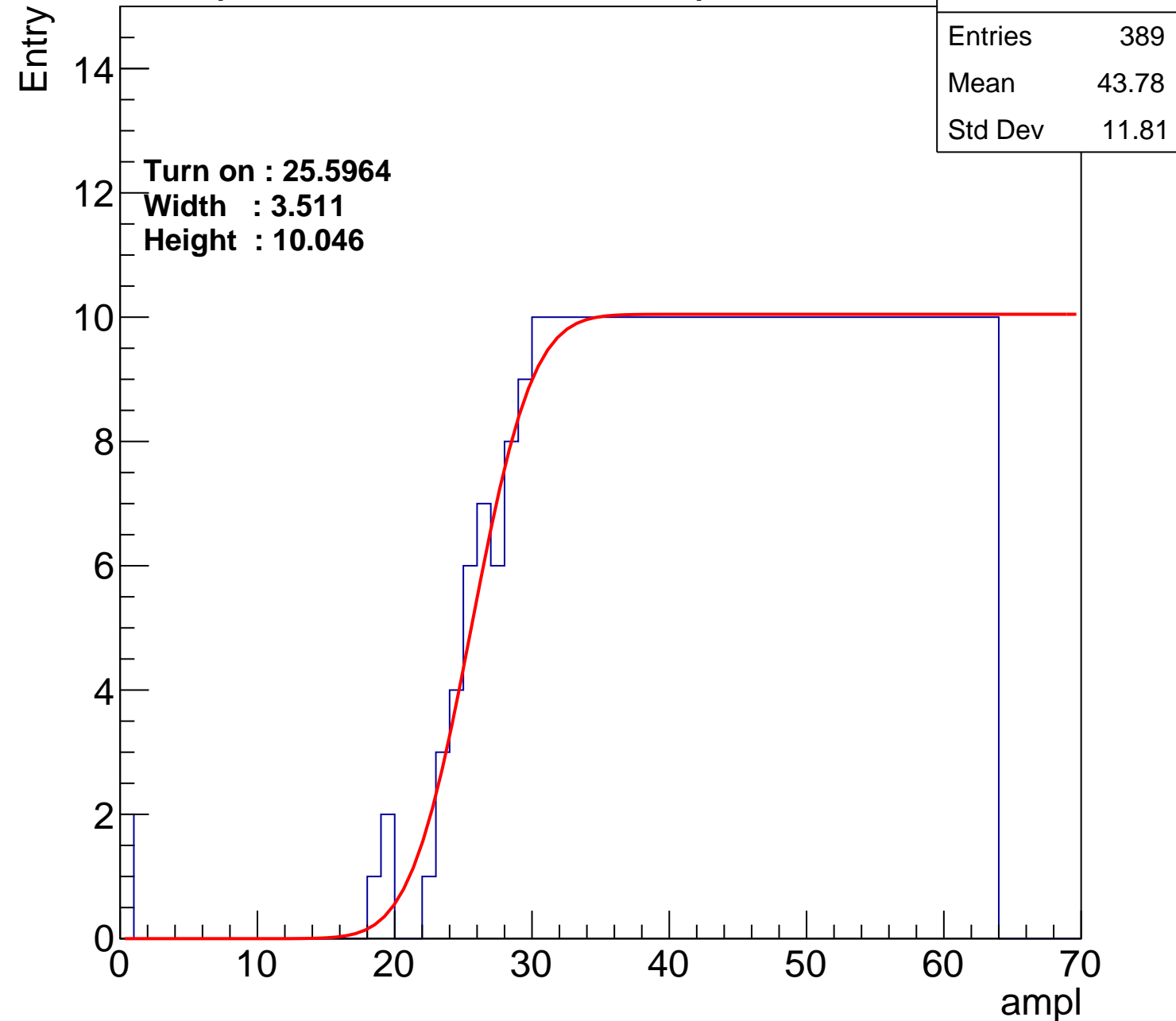
Width : 3.511

Height : 10.046

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch5

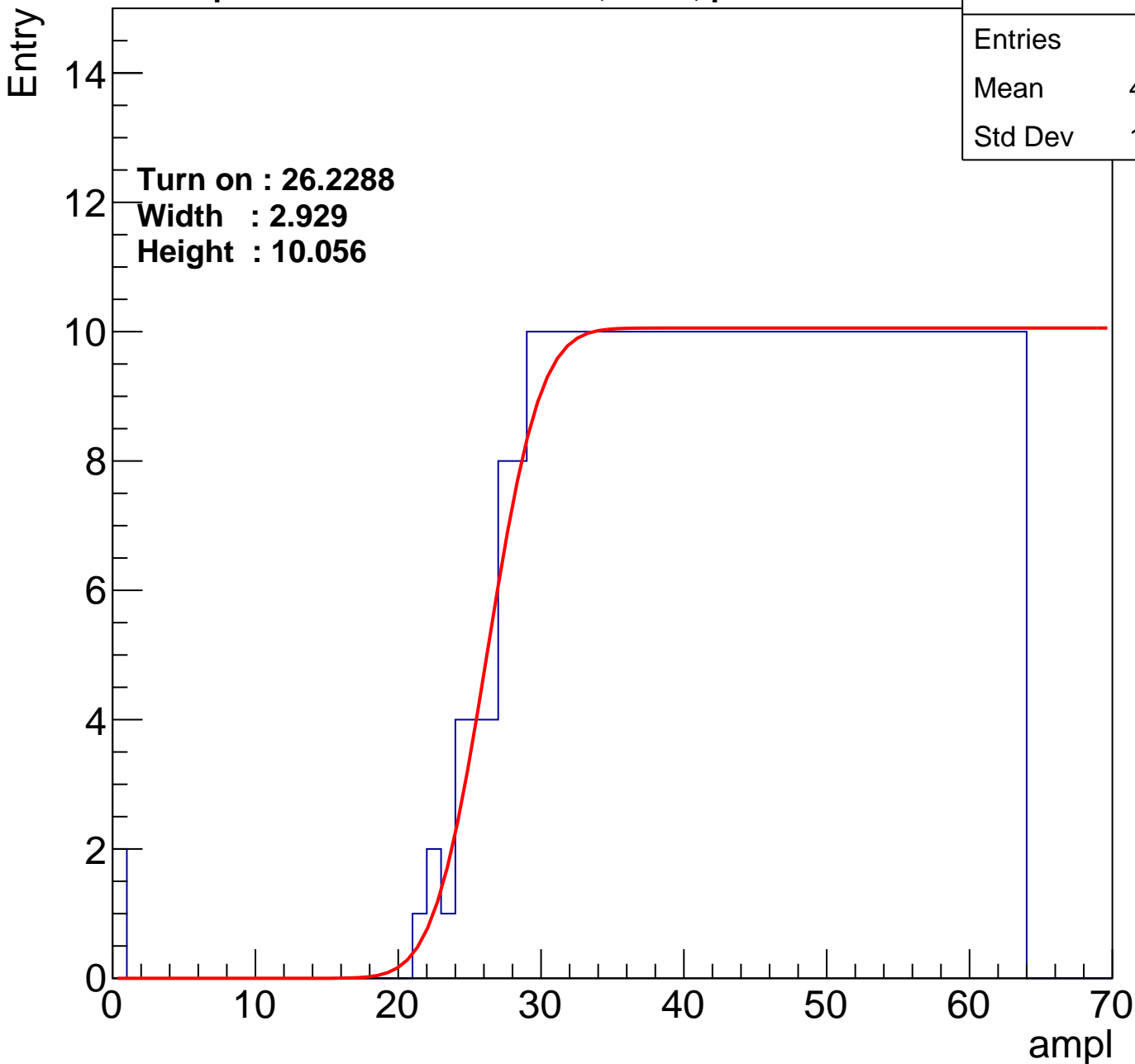
calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	384
Mean	44.08
Std Dev	11.59

Turn on : 26.2288

Width : 2.929

Height : 10.056



# B1L000S, U7-ch6

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	377
Mean	44.49
Std Dev	11.23

Turn on : 26.8558

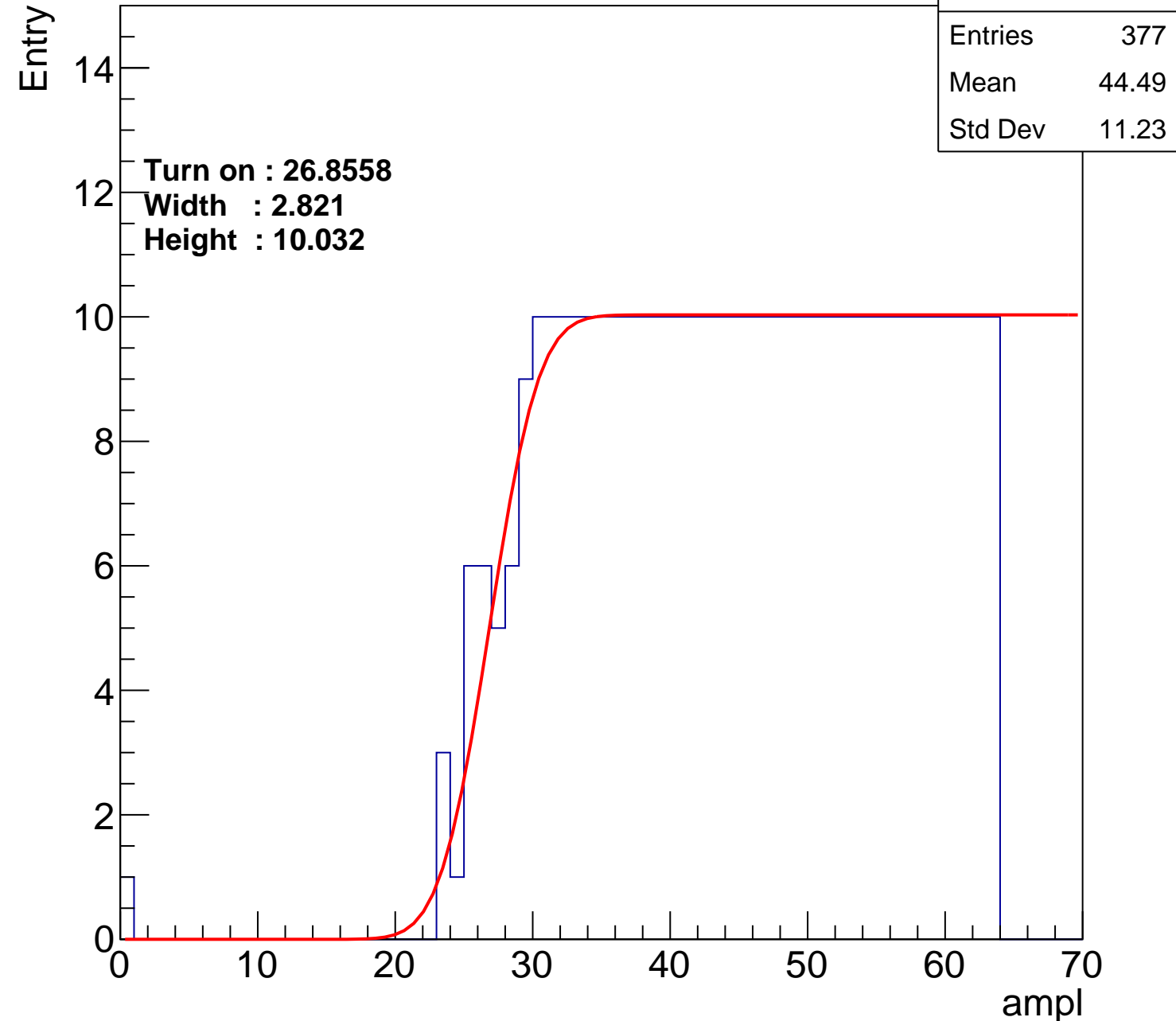
Width : 2.821

Height : 10.032

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L000S, U7-ch7

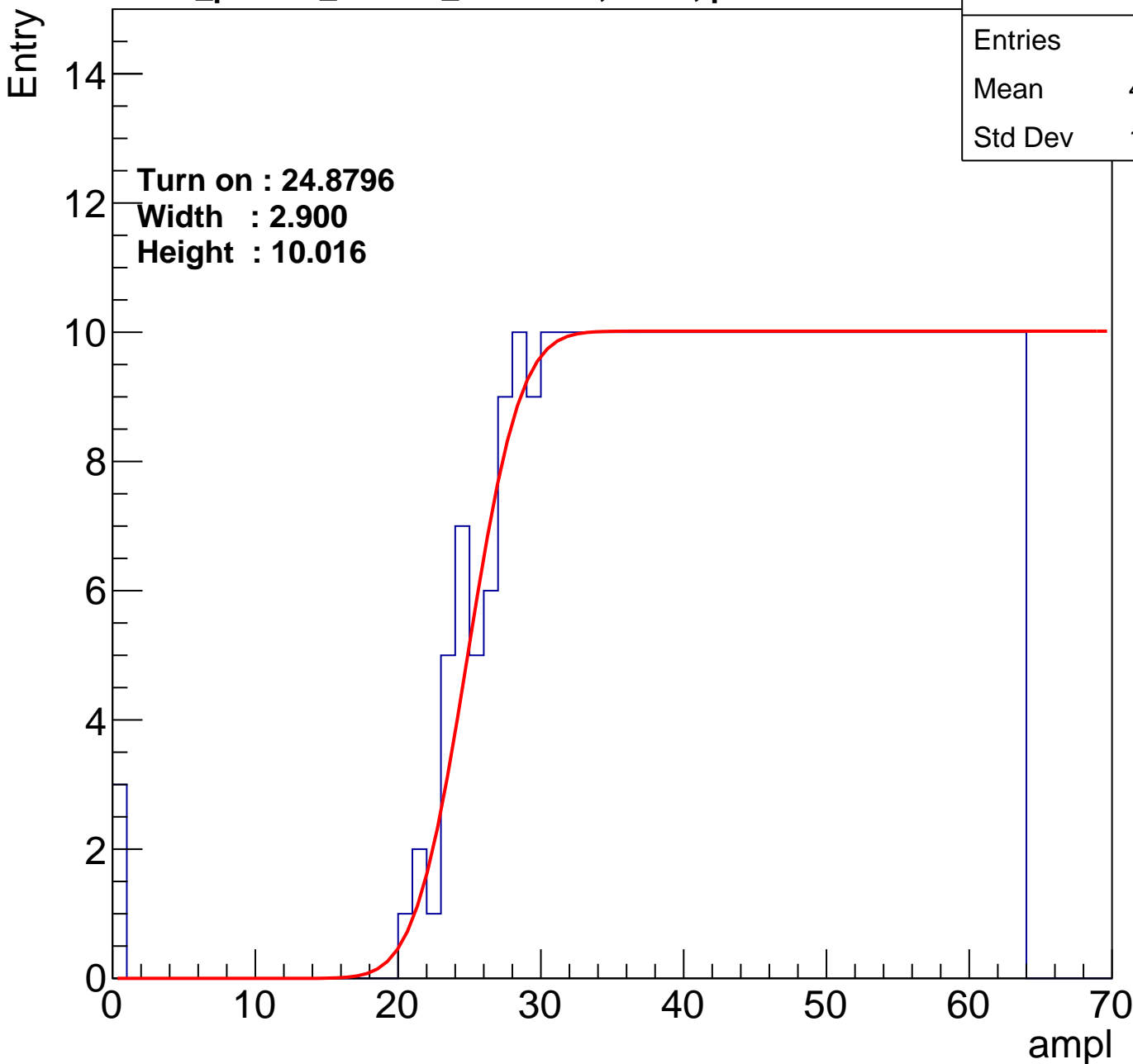
**calib\_packv5\_042523\_0143.root, FC#3, port B3**

Entries	398
Mean	43.32
Std Dev	12.13

**Turn on : 24.8796**

**Width : 2.900**

**Height : 10.016**



# B1L000S, U7-ch8

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	395
Mean	43.4
Std Dev	12.22

**Turn on : 24.9847**

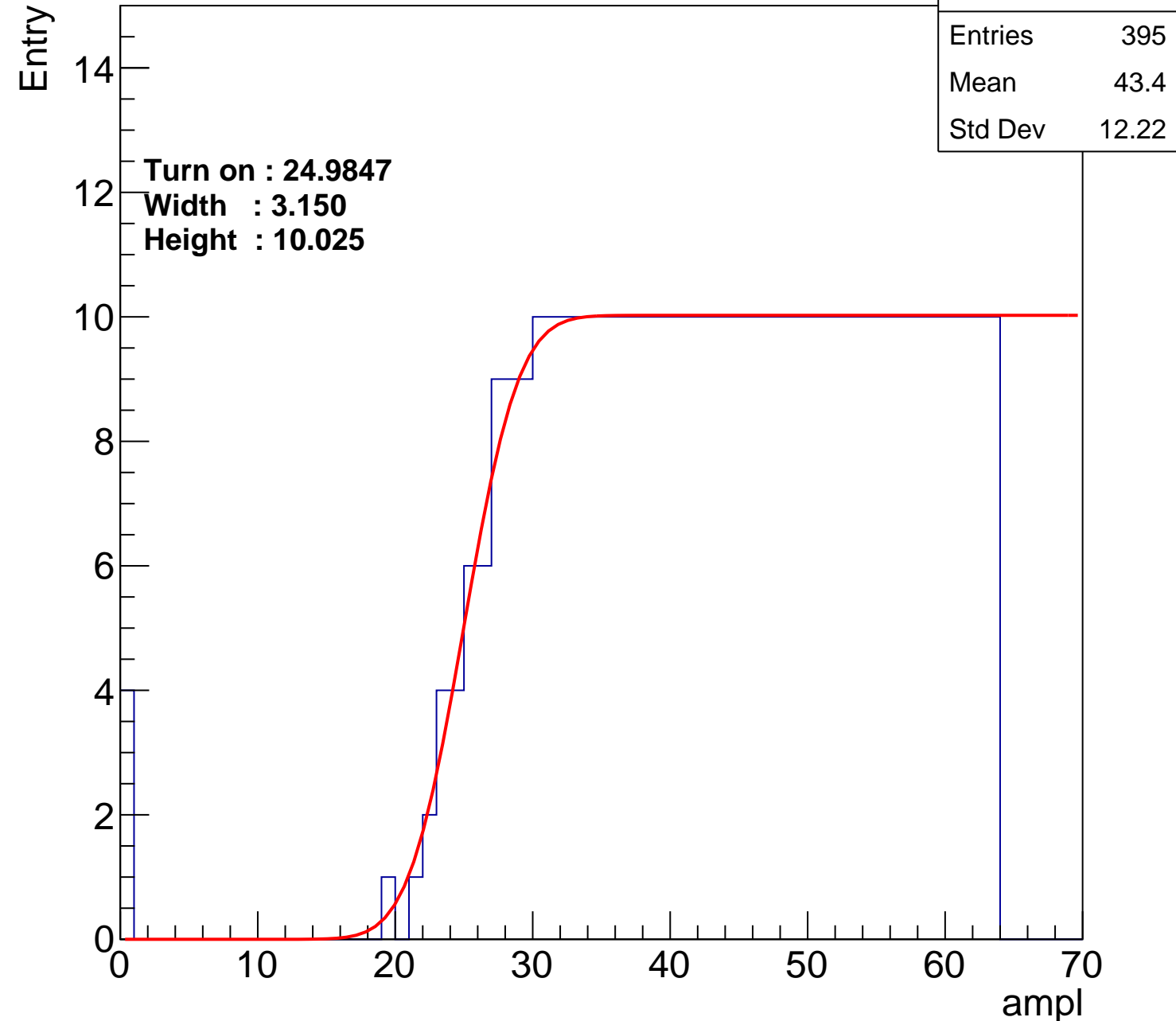
**Width : 3.150**

**Height : 10.025**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch9

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	380
Mean	44.14
Std Dev	11.86

**Turn on : 26.8395**

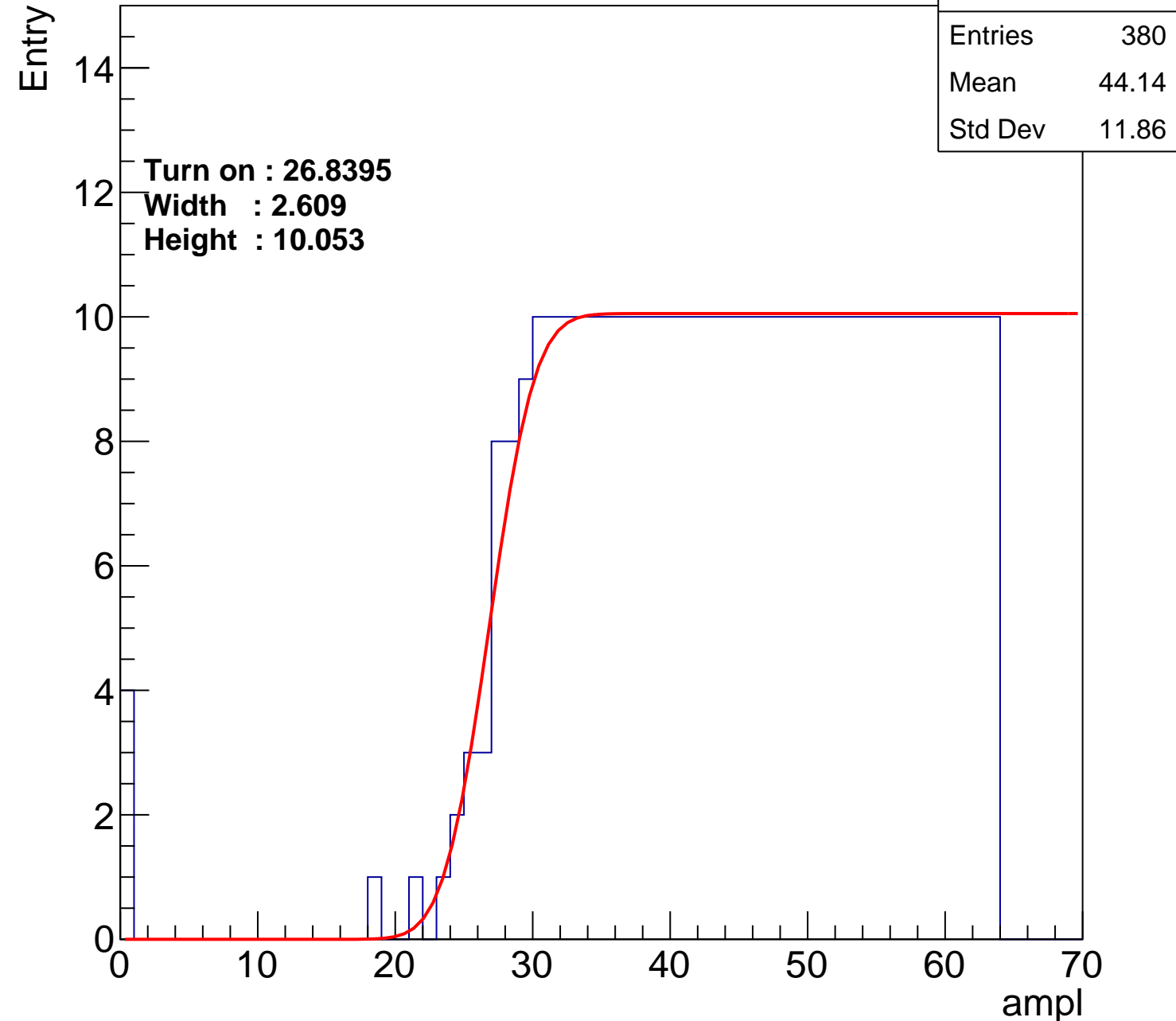
**Width : 2.609**

**Height : 10.053**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch10

**calib\_packv5\_042523\_0143.root, FC#3, port B3**

Entries 376

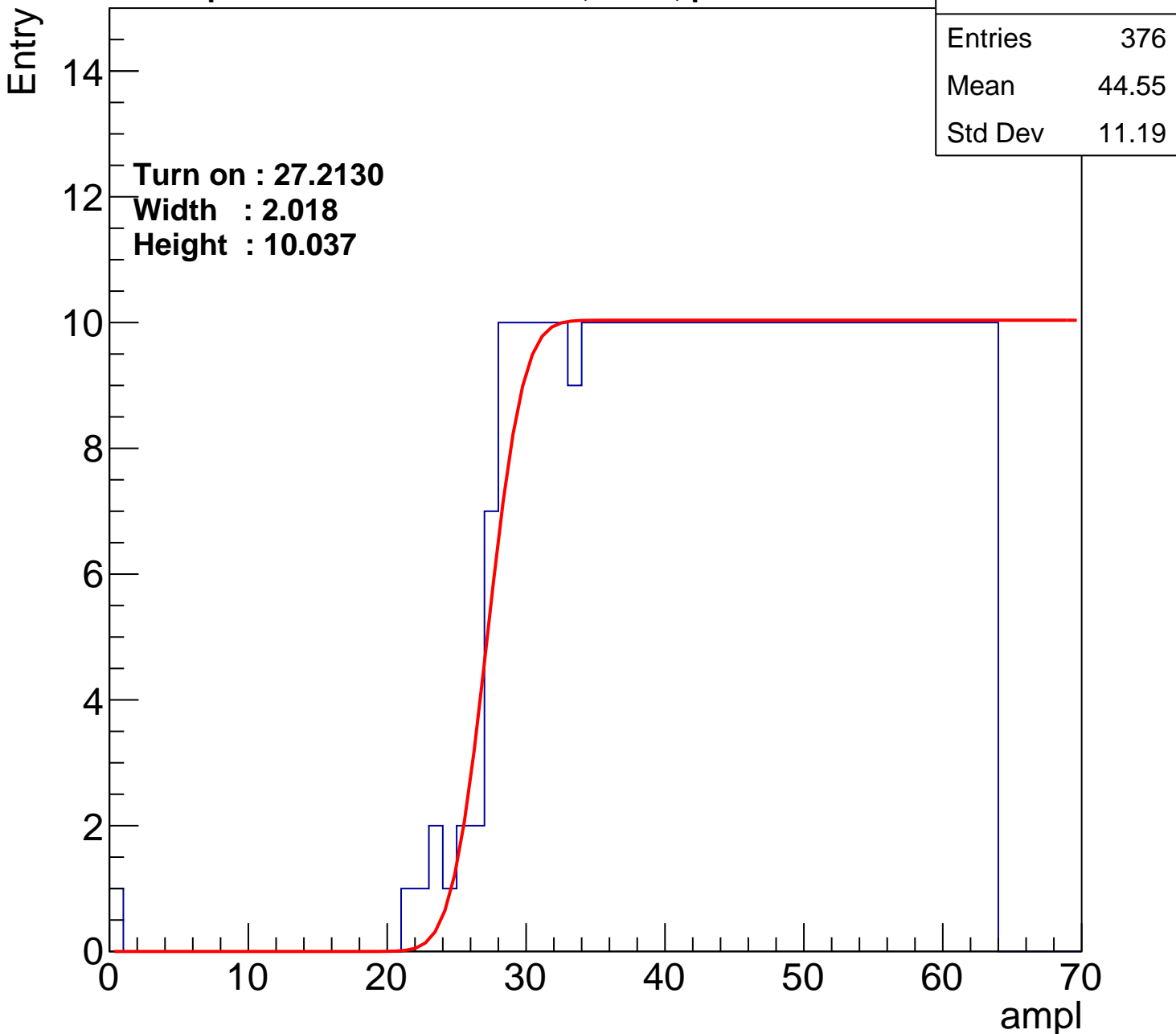
Mean 44.55

Std Dev 11.19

**Turn on : 27.2130**

**Width : 2.018**

**Height : 10.037**



# B1L000S, U7-ch11

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	392
Mean	43.71
Std Dev	11.75

**Turn on : 24.9446**

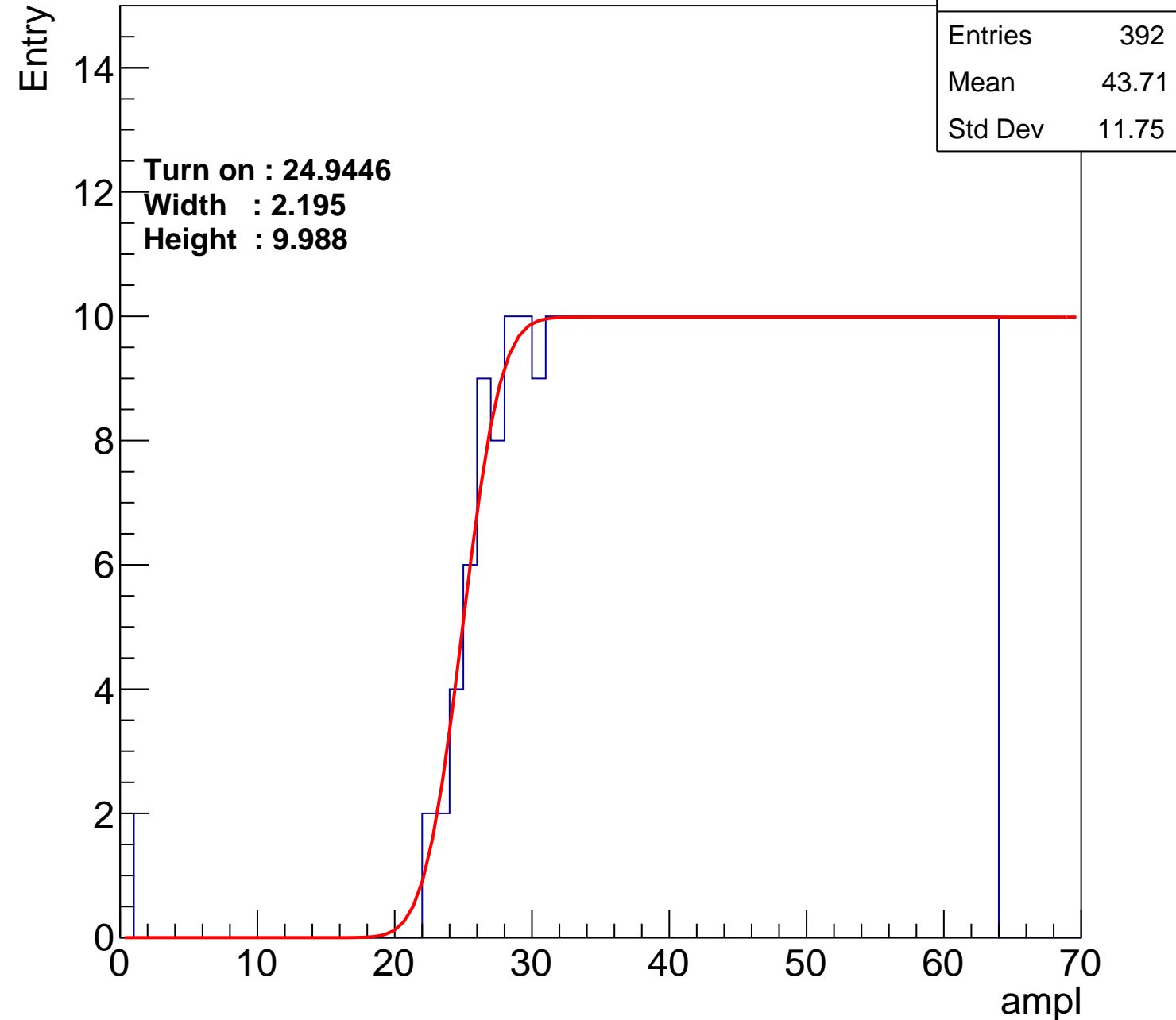
**Width : 2.195**

**Height : 9.988**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch12

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	400
Mean	43.18
Std Dev	12.3

Turn on : 24.6502

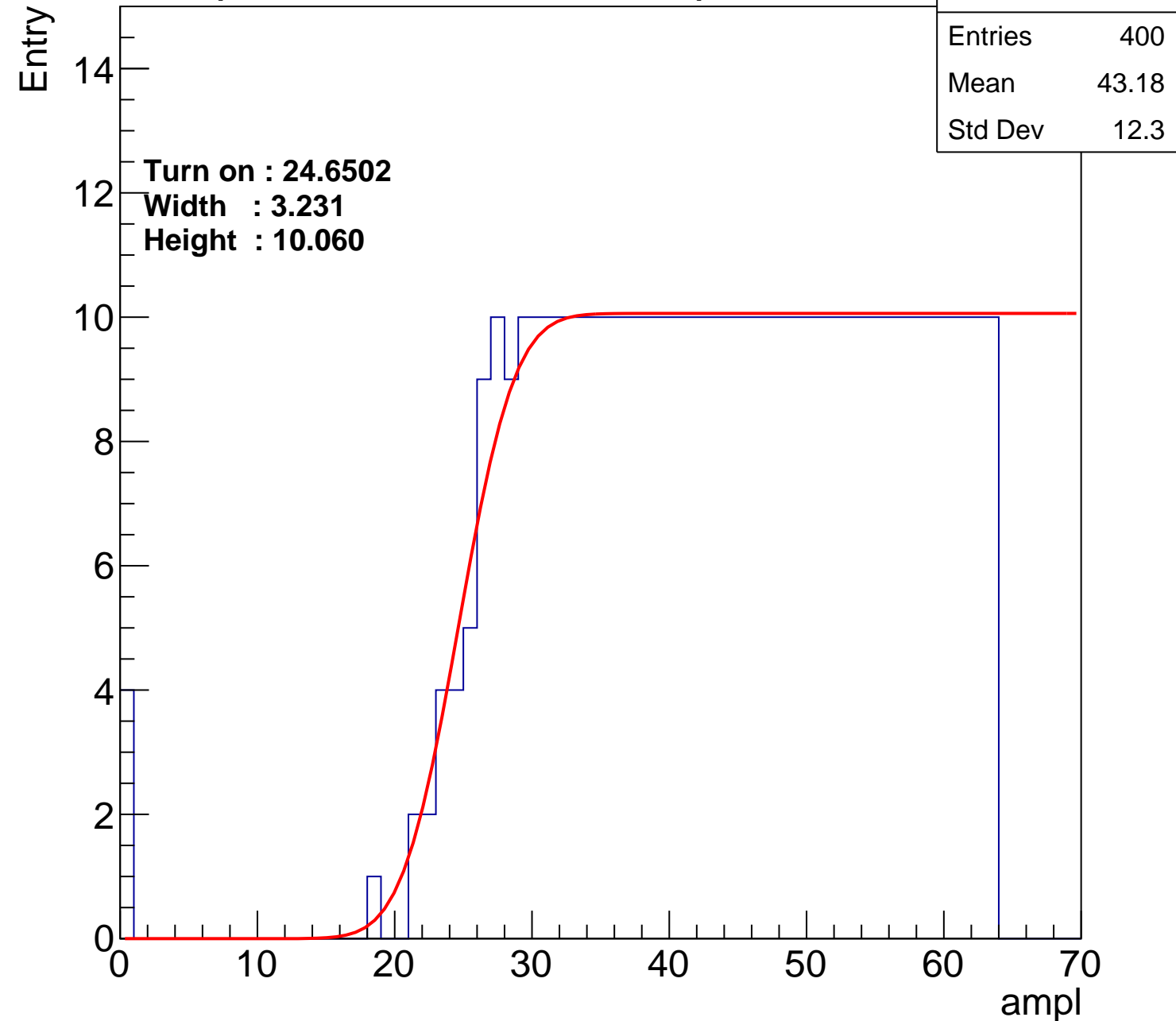
Width : 3.231

Height : 10.060

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch13

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	385
Mean	43.91
Std Dev	11.94

**Turn on : 25.9289**

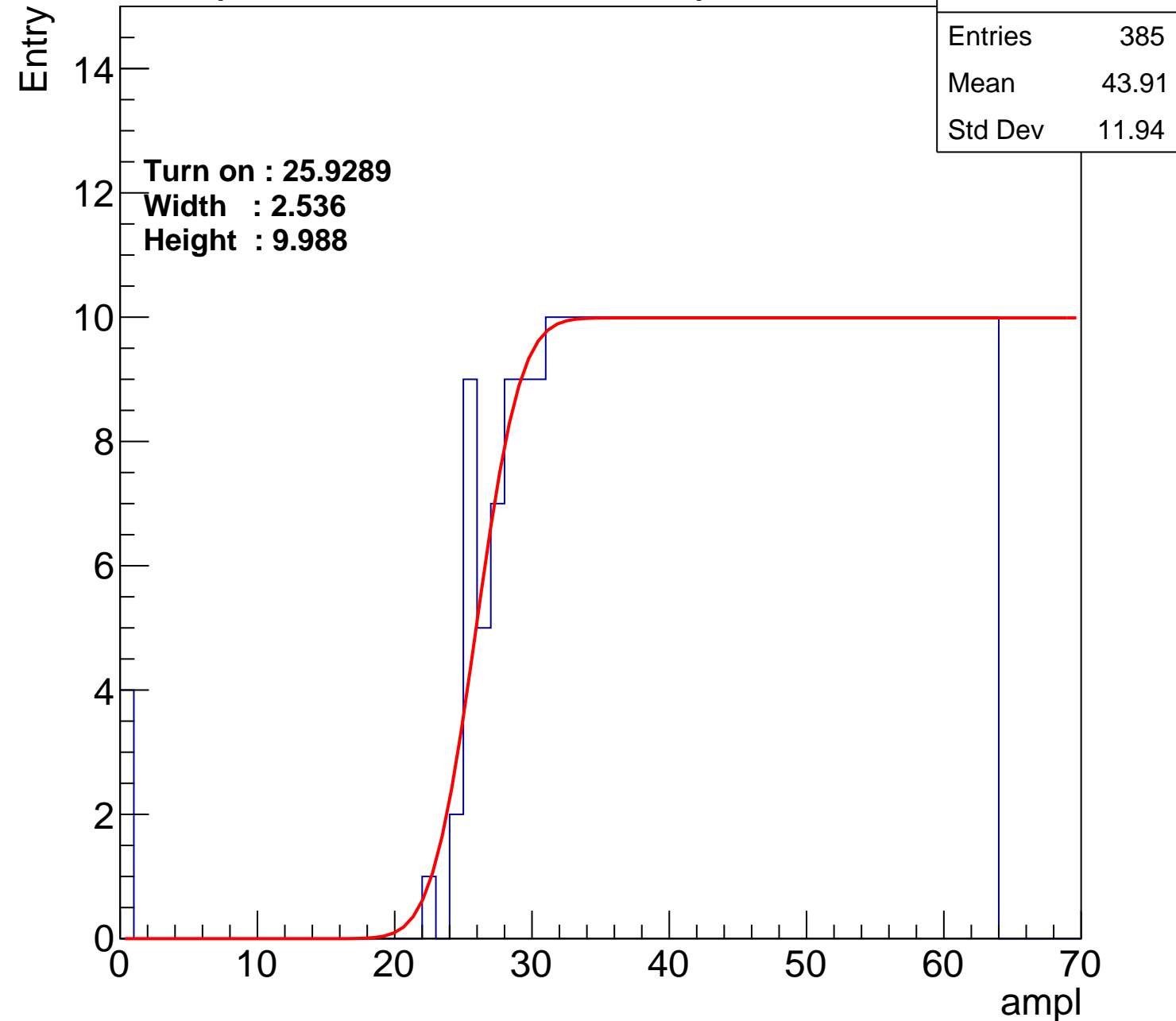
**Width : 2.536**

**Height : 9.988**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch14

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	379
Mean	44.42
Std Dev	11.24

Turn on : 26.5151

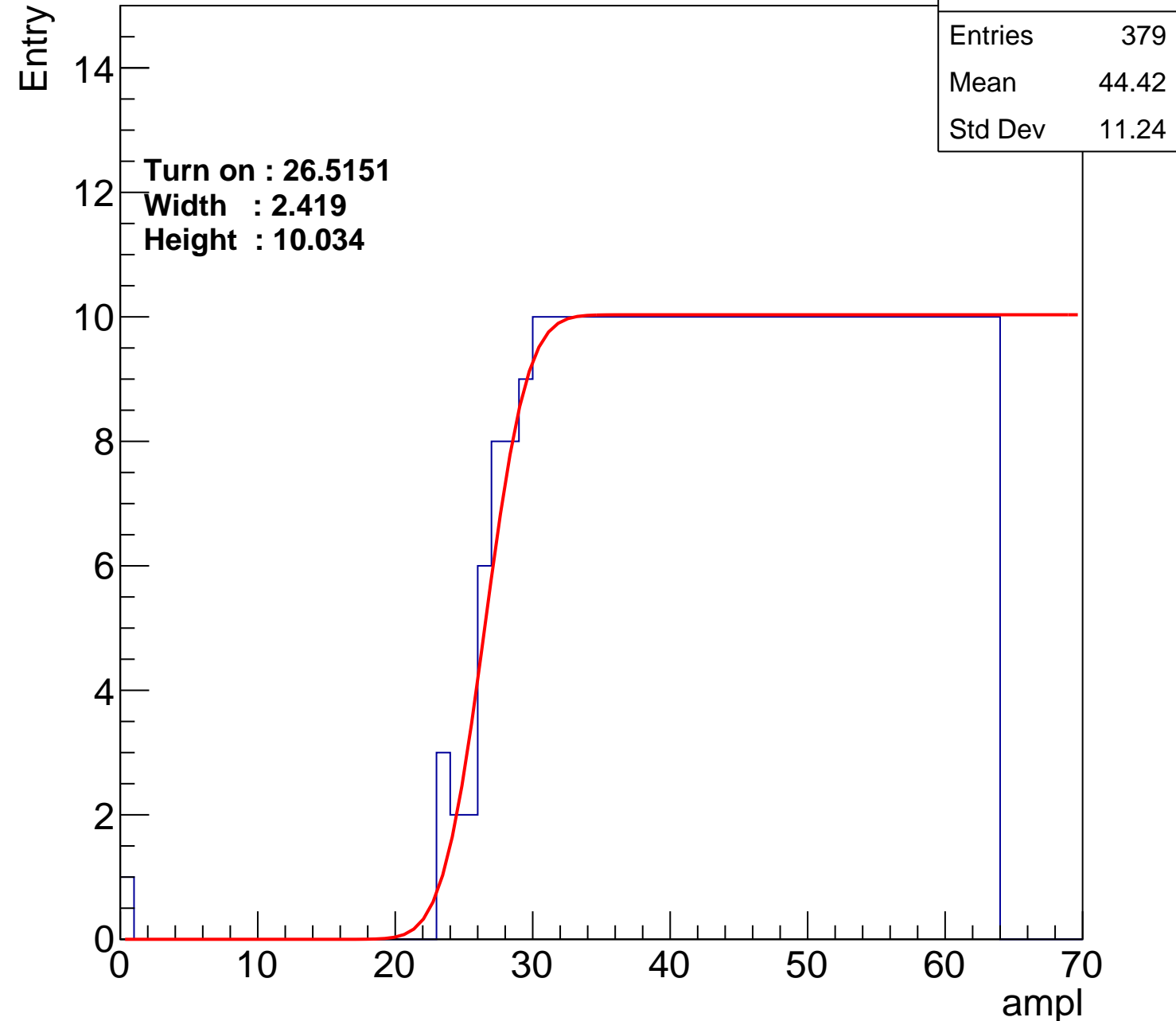
Width : 2.419

Height : 10.034

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L000S, U7-ch15

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	391
Mean	43.71
Std Dev	11.82

**Turn on : 25.6332**

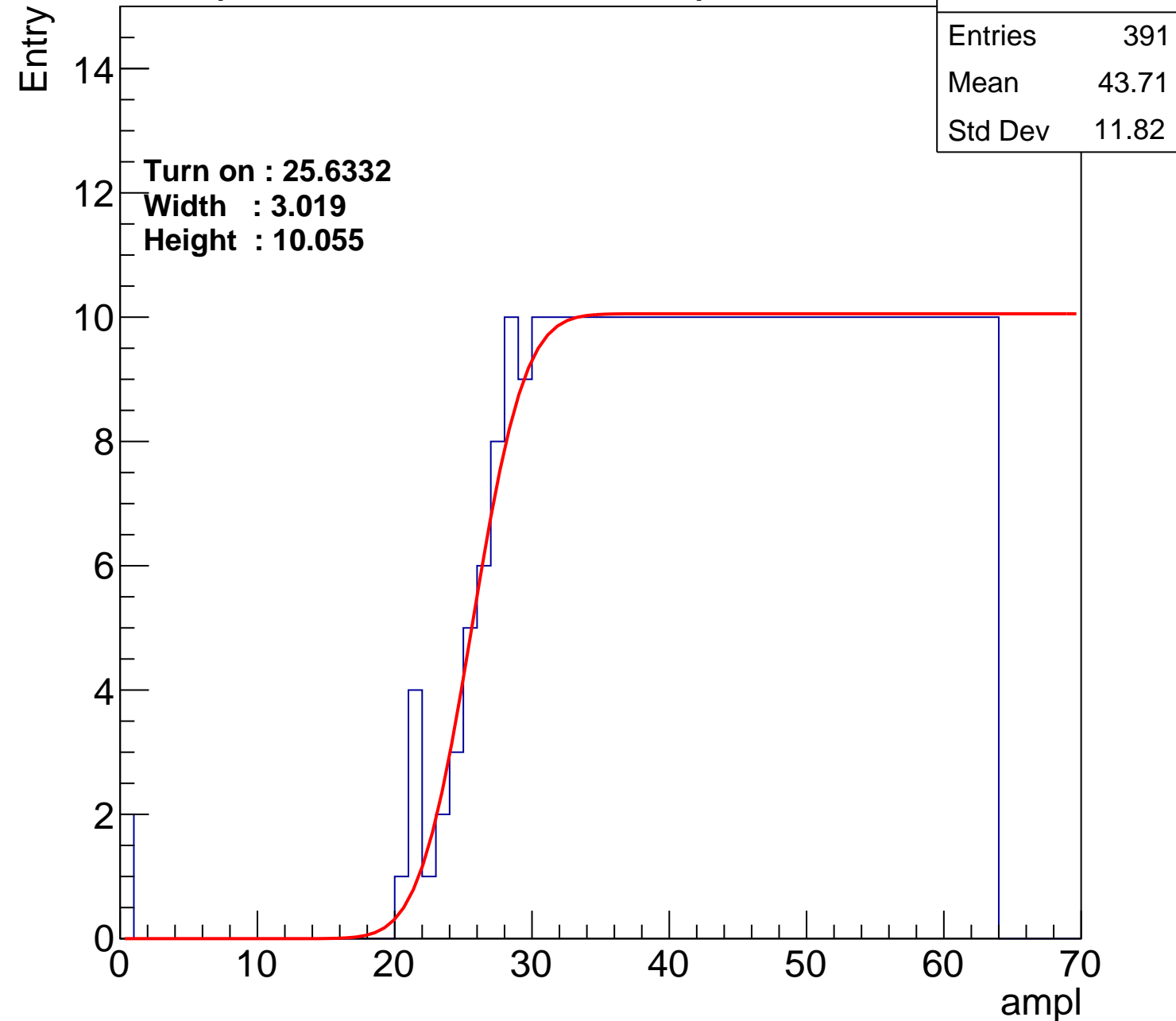
**Width : 3.019**

**Height : 10.055**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch16

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	386
Mean	43.83
Std Dev	12.02

Turn on : 26.1218

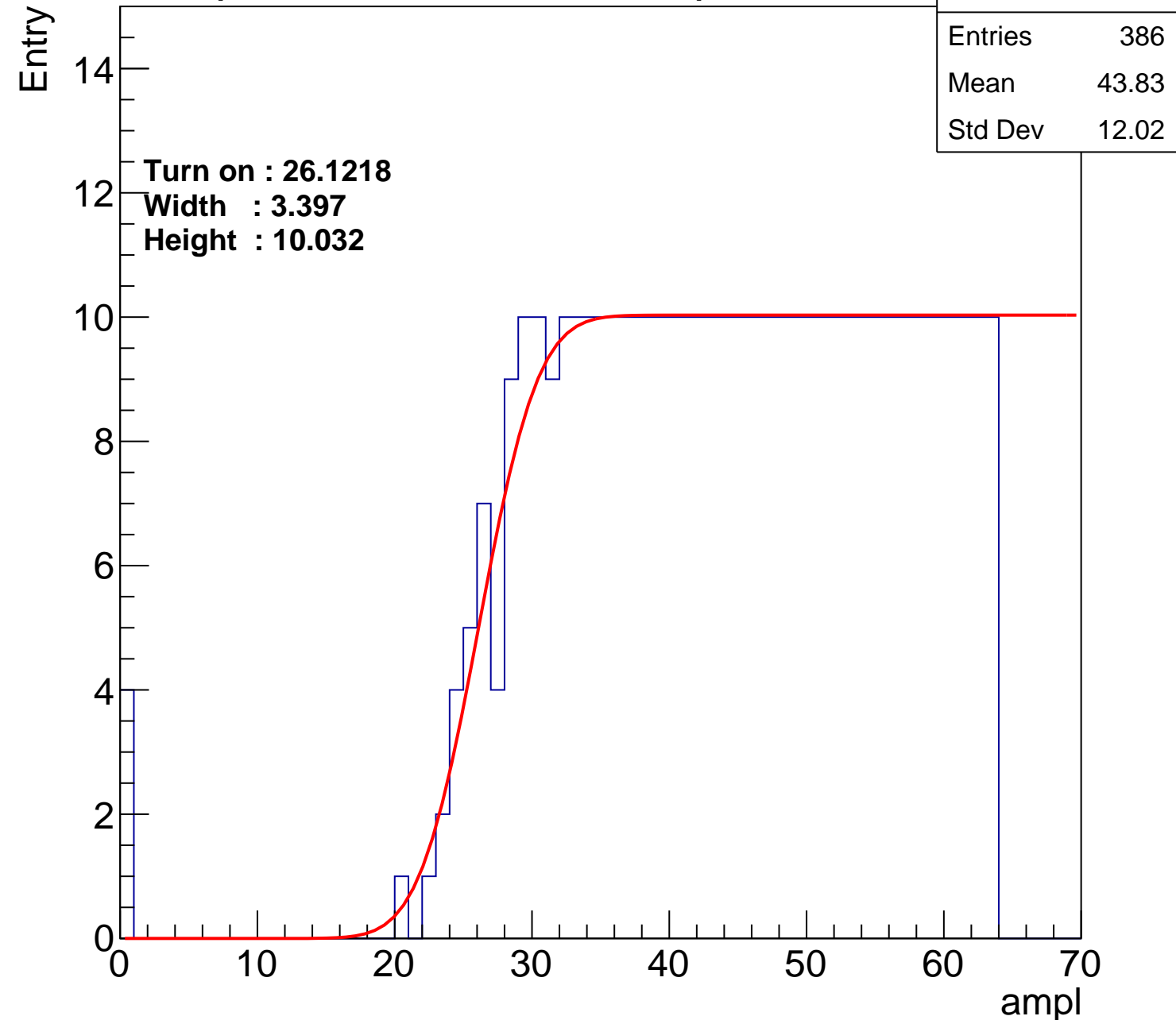
Width : 3.397

Height : 10.032

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch17

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	390
Mean	43.56
Std Dev	12.31

Turn on : 25.8252

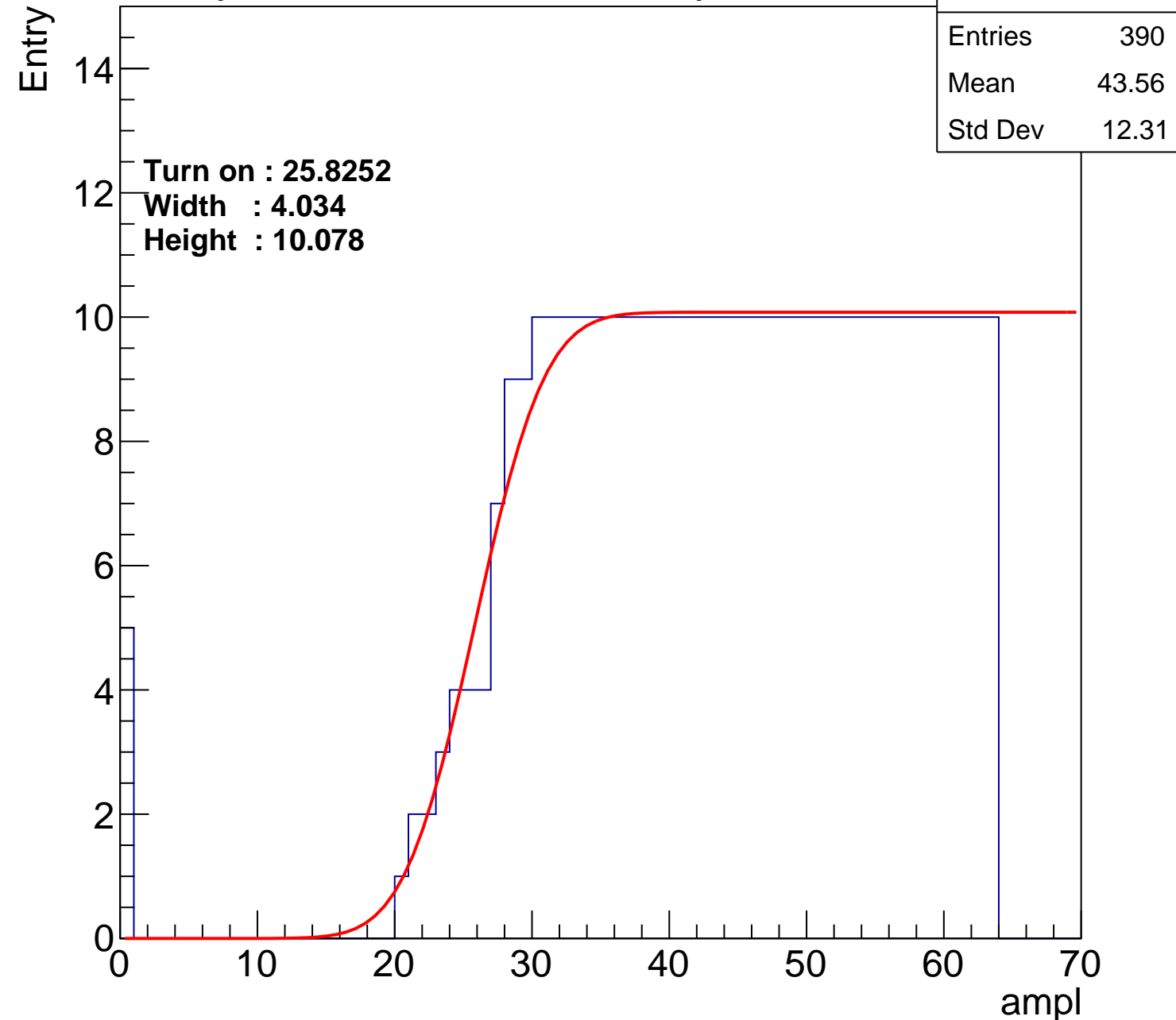
Width : 4.034

Height : 10.078

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch18

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	388
Mean	43.98
Std Dev	11.46

**Turn on : 25.9027**

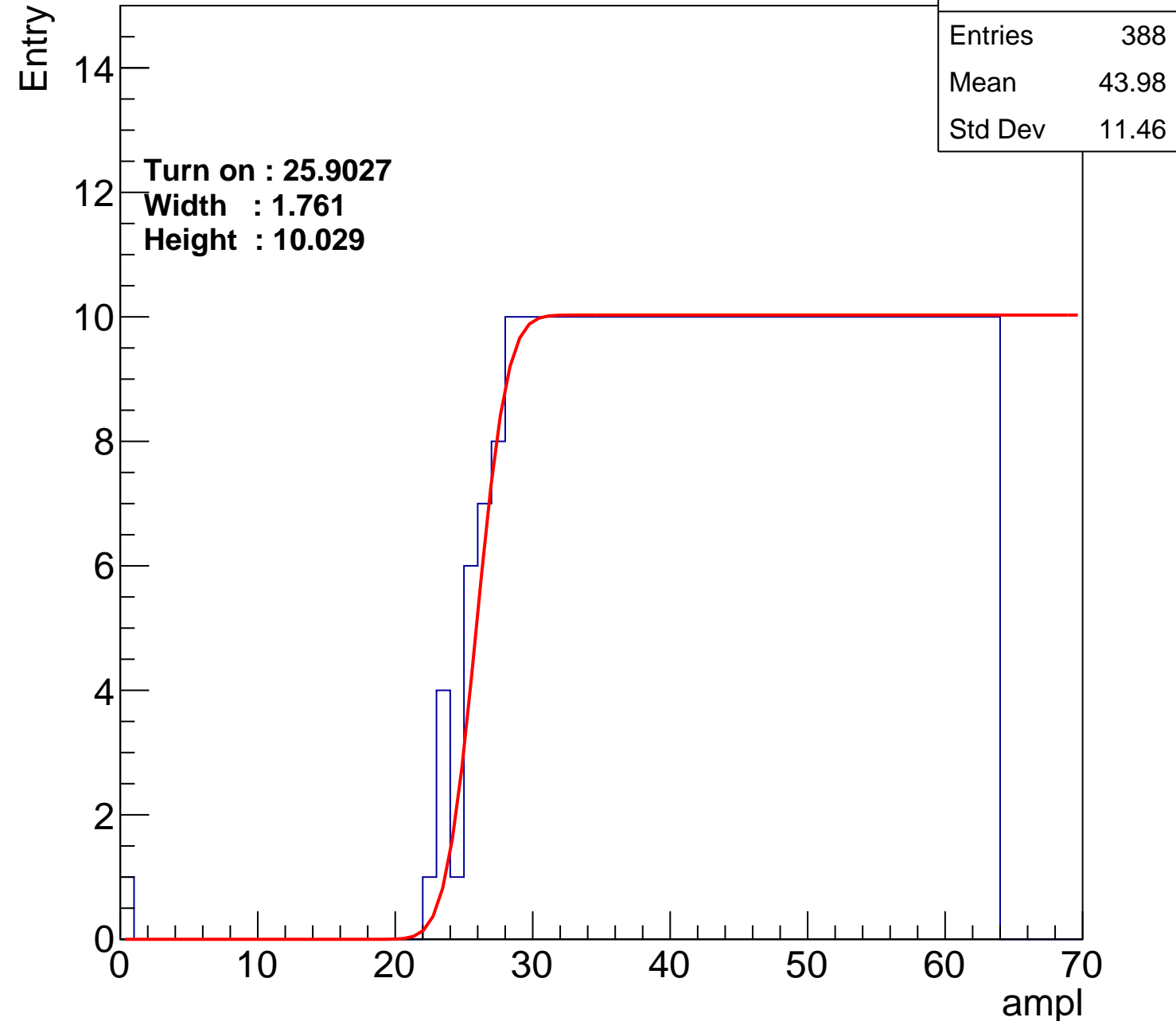
**Width : 1.761**

**Height : 10.029**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch19

calib\_packv5\_042523\_0143.root, FC#3, port B3

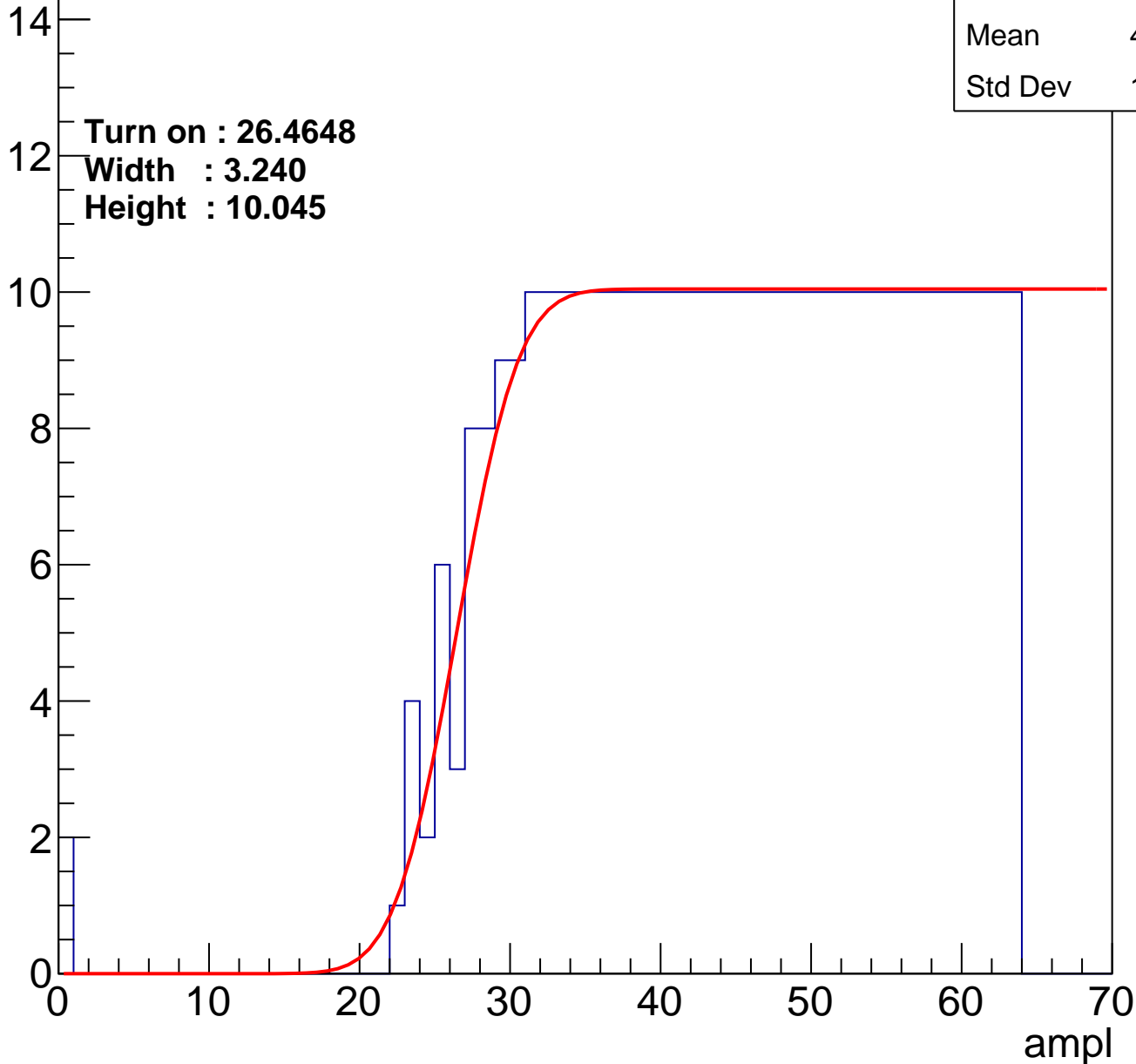
Entries	382
Mean	44.16
Std Dev	11.56

**Turn on : 26.4648**

**Width : 3.240**

**Height : 10.045**

Entry



# B1L000S, U7-ch20

calib\_packv5\_042523\_0143.root, FC#3, port B3

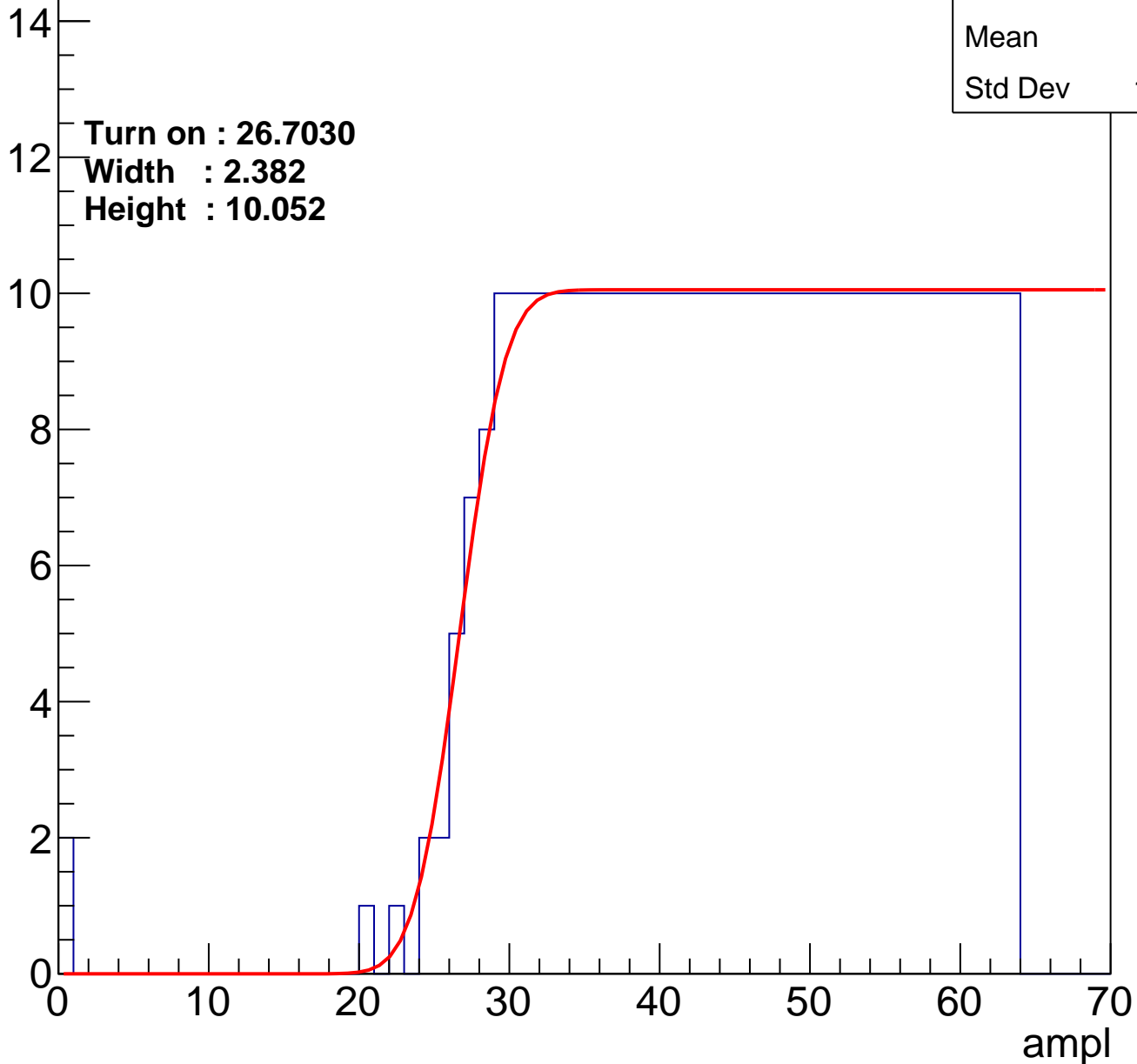
Entries	378
Mean	44.4
Std Dev	11.41

Turn on : 26.7030

Width : 2.382

Height : 10.052

Entry



# B1L000S, U7-ch21

calib\_packv5\_042523\_0143.root, FC#3, port B3

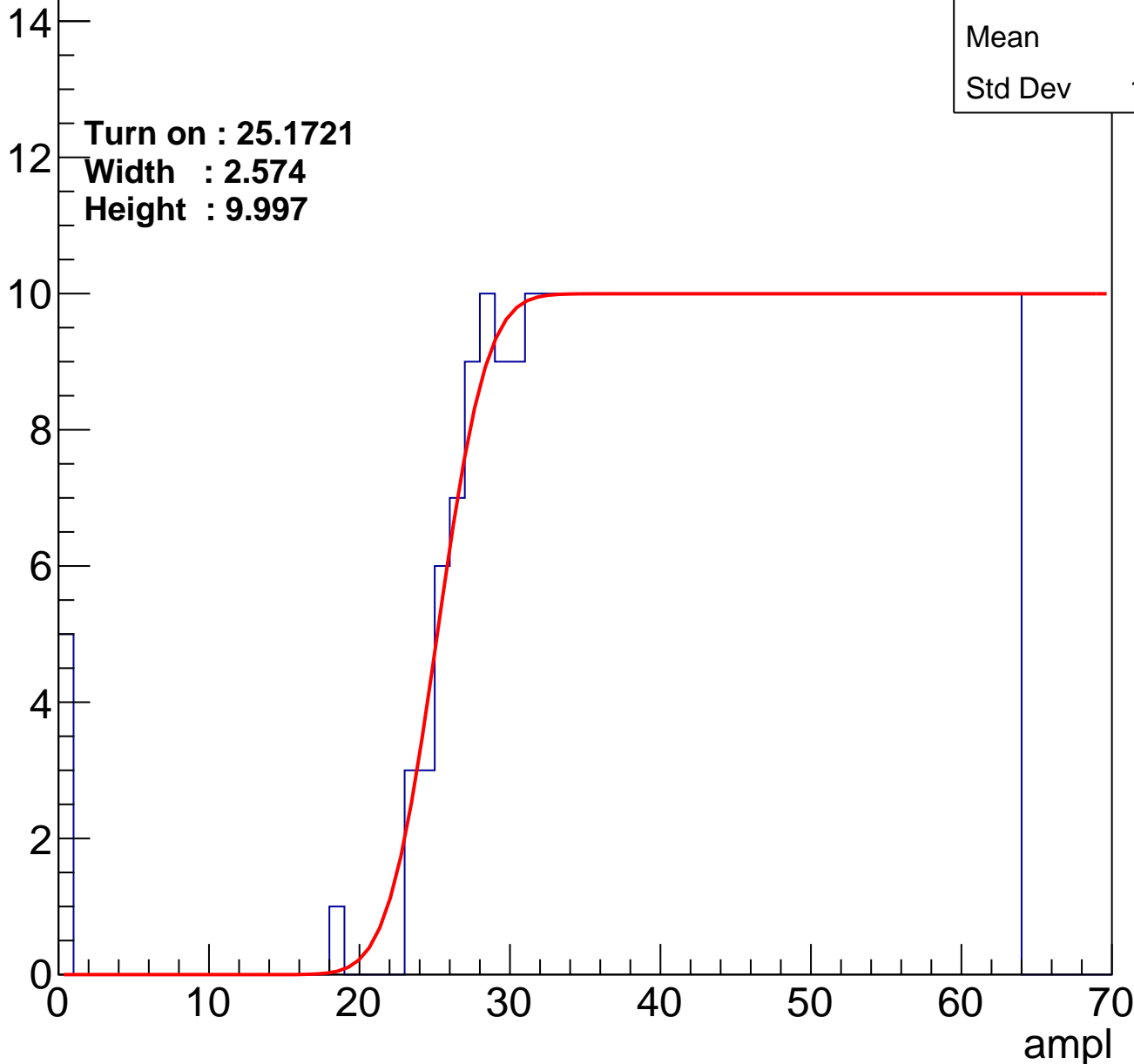
Entries	392
Mean	43.51
Std Dev	12.27

Turn on : 25.1721

Width : 2.574

Height : 9.997

Entry



# B1L000S, U7-ch22

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	390
Mean	43.79
Std Dev	11.74

Turn on : 25.2849

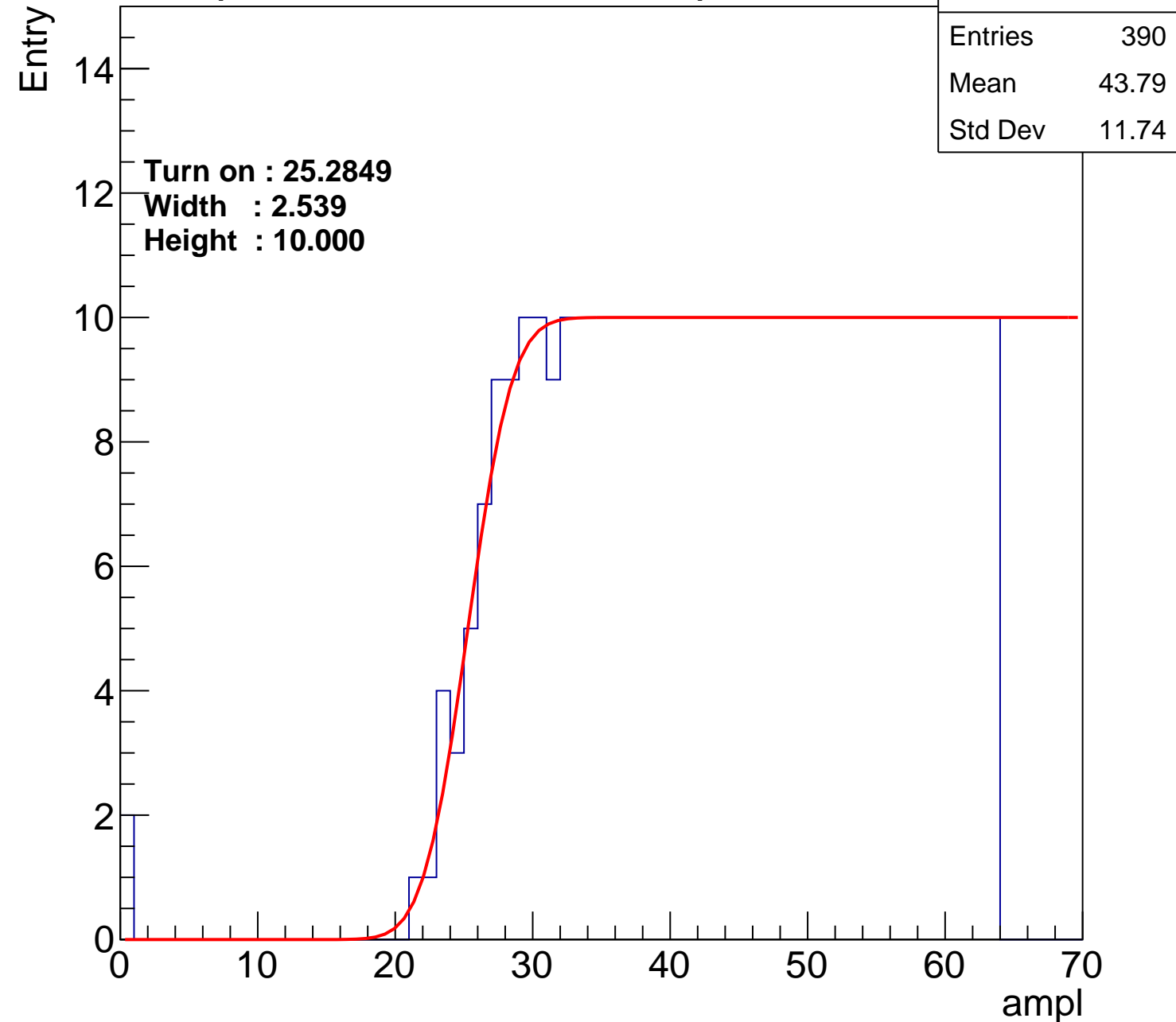
Width : 2.539

Height : 10.000

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L000S, U7-ch23

calib\_packv5\_042523\_0143.root, FC#3, port B3

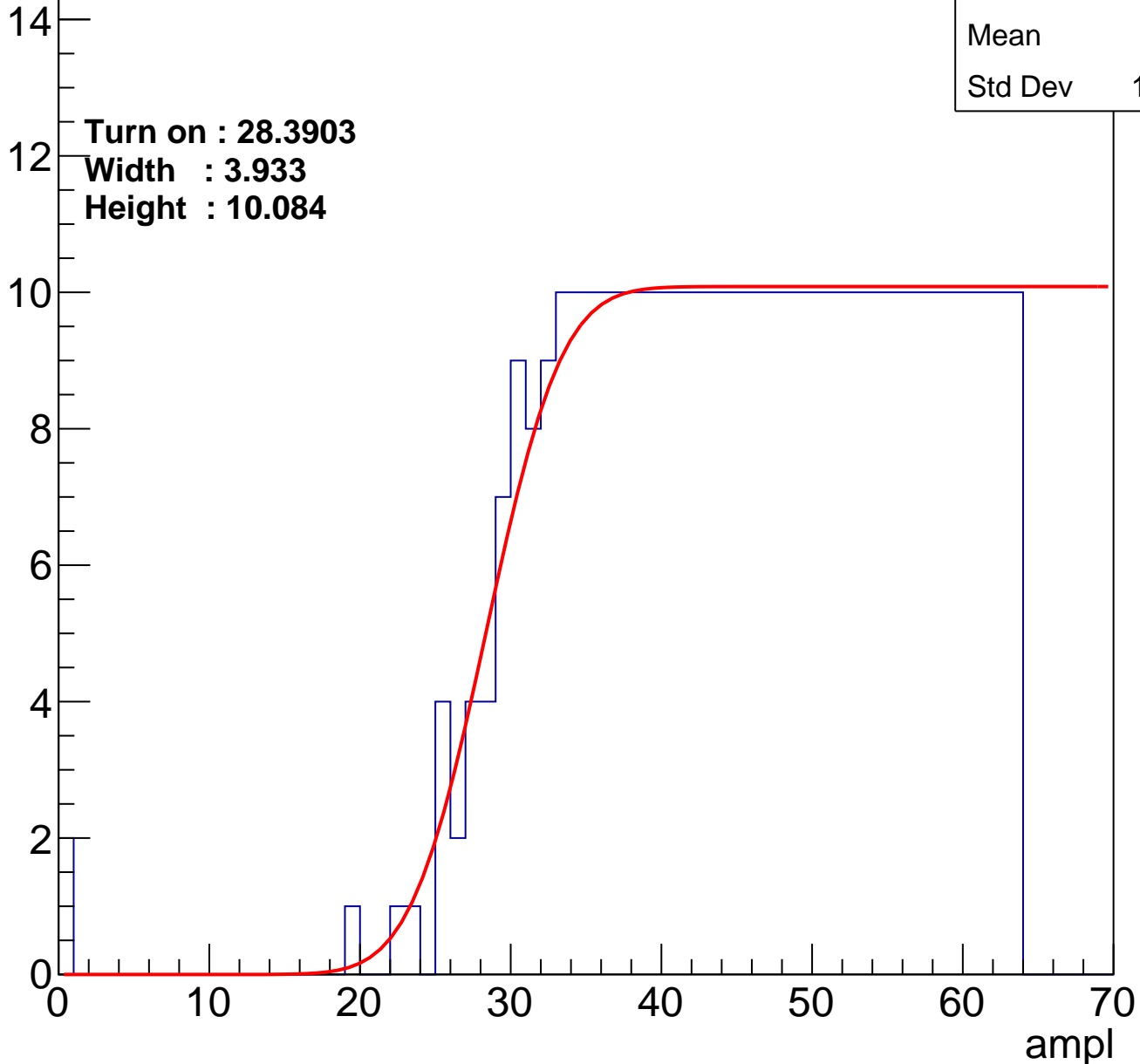
Entries	362
Mean	45.1
Std Dev	11.15

**Turn on : 28.3903**

**Width : 3.933**

**Height : 10.084**

Entry



# B1L000S, U7-ch24

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	394
Mean	43.57
Std Dev	11.88

Turn on : 24.9998

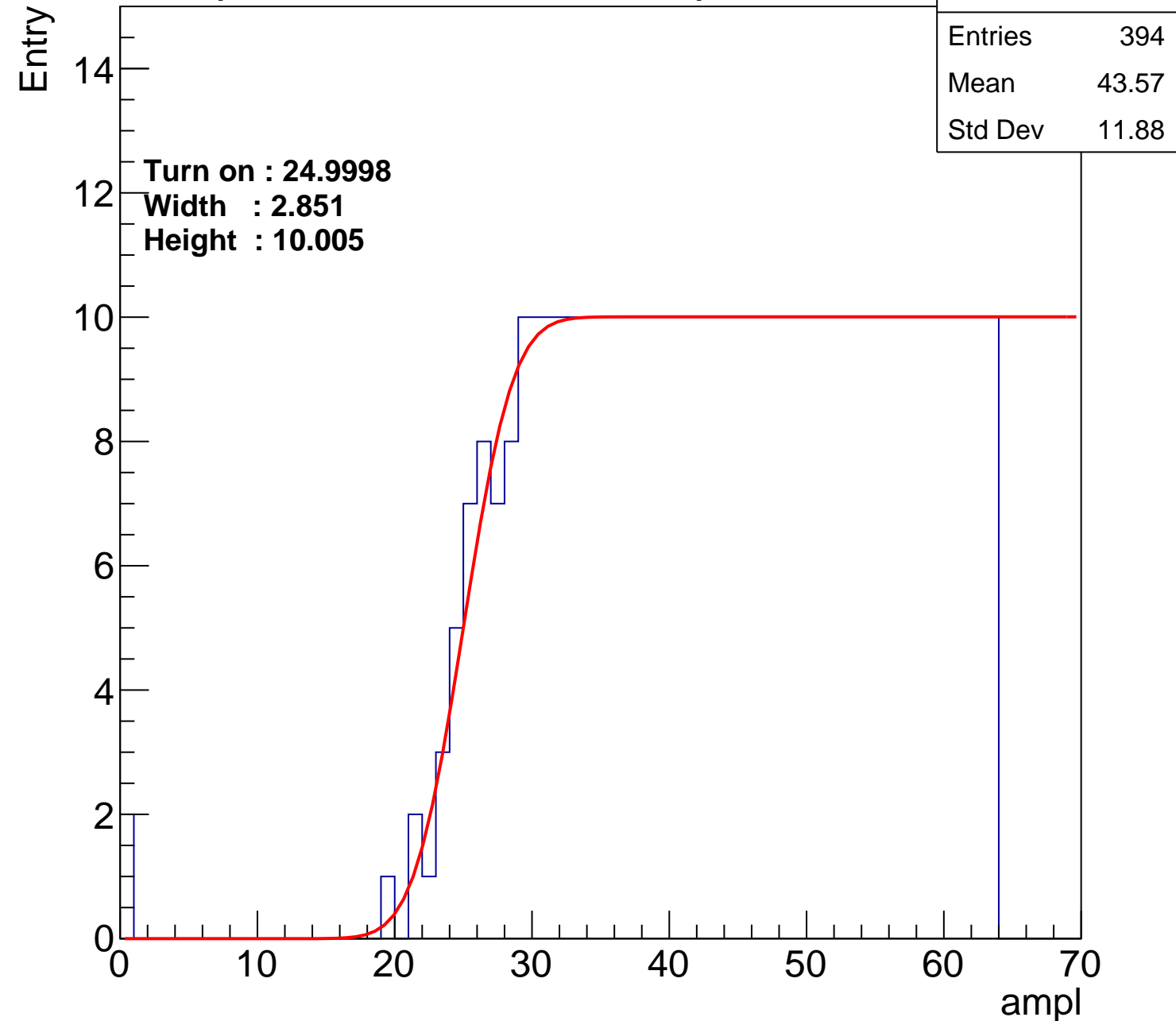
Width : 2.851

Height : 10.005

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch25

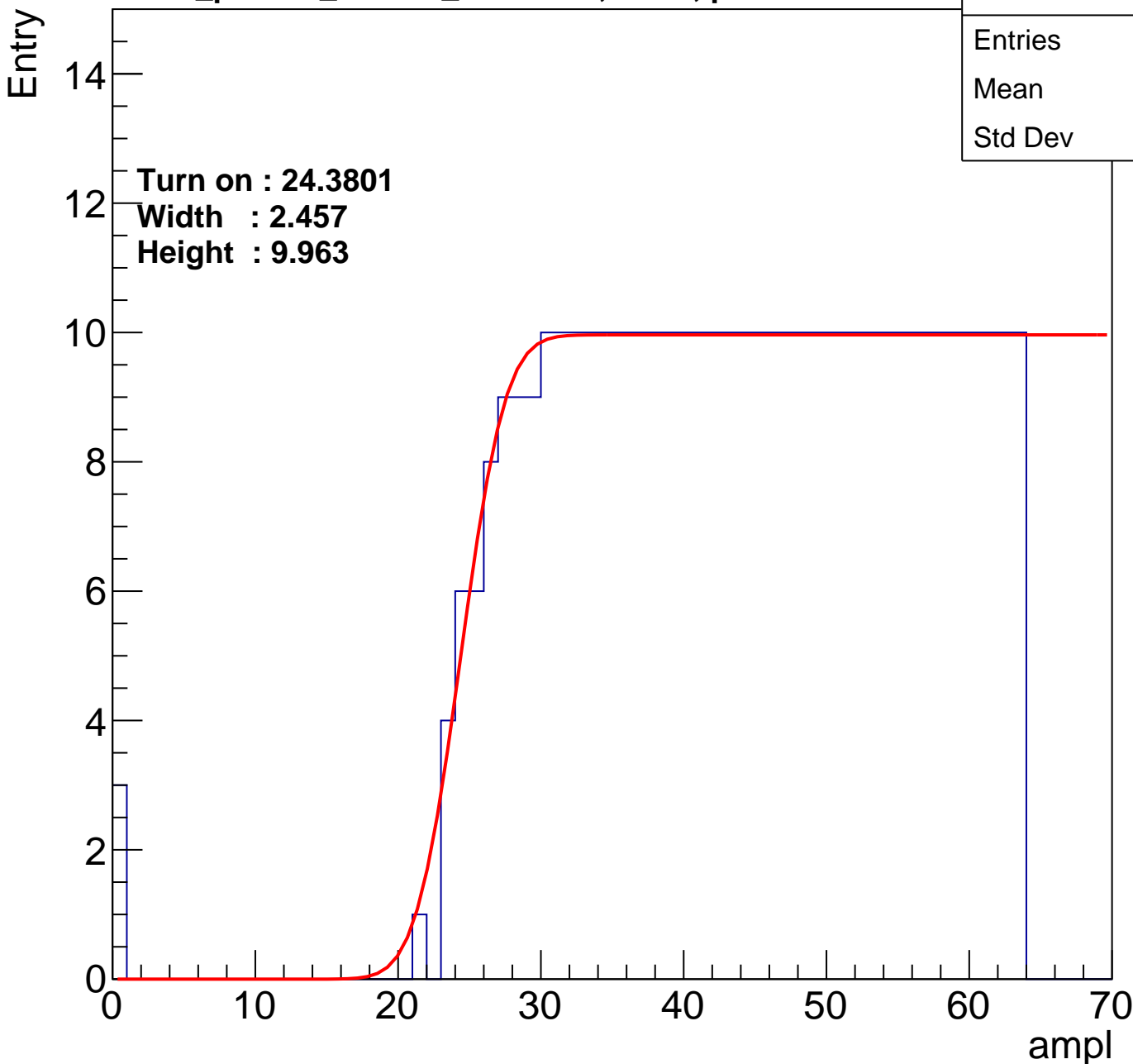
**calib\_packv5\_042523\_0143.root, FC#3, port B3**

**Turn on : 24.3801**

**Width : 2.457**

**Height : 9.963**

Entries	395
Mean	43.5
Std Dev	12.01



# B1L000S, U7-ch26

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	375
Mean	44.53
Std Dev	11.35

**Turn on : 26.8404**

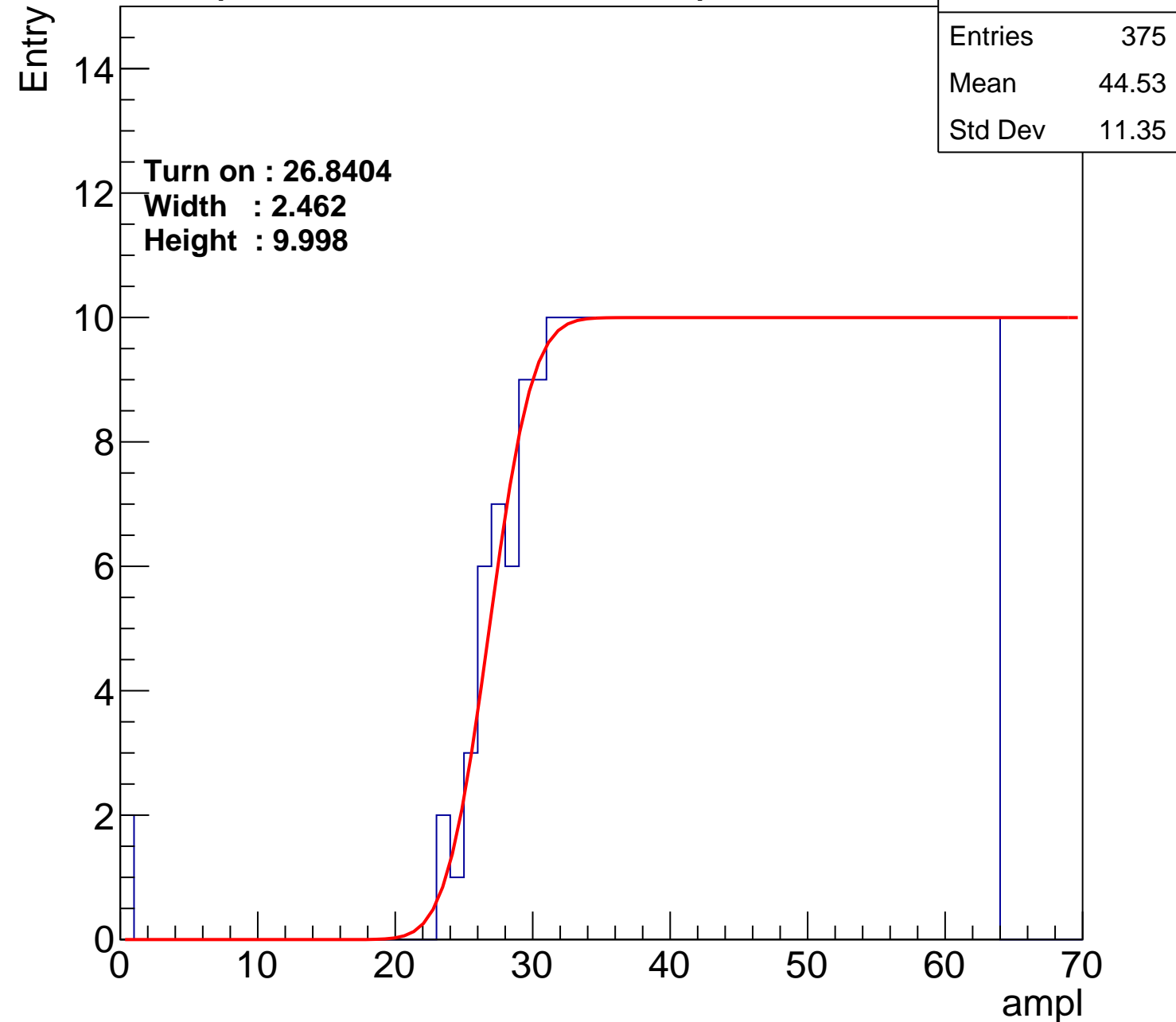
**Width : 2.462**

**Height : 9.998**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch27

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	369
Mean	44.82
Std Dev	11.21

Turn on : 27.0802

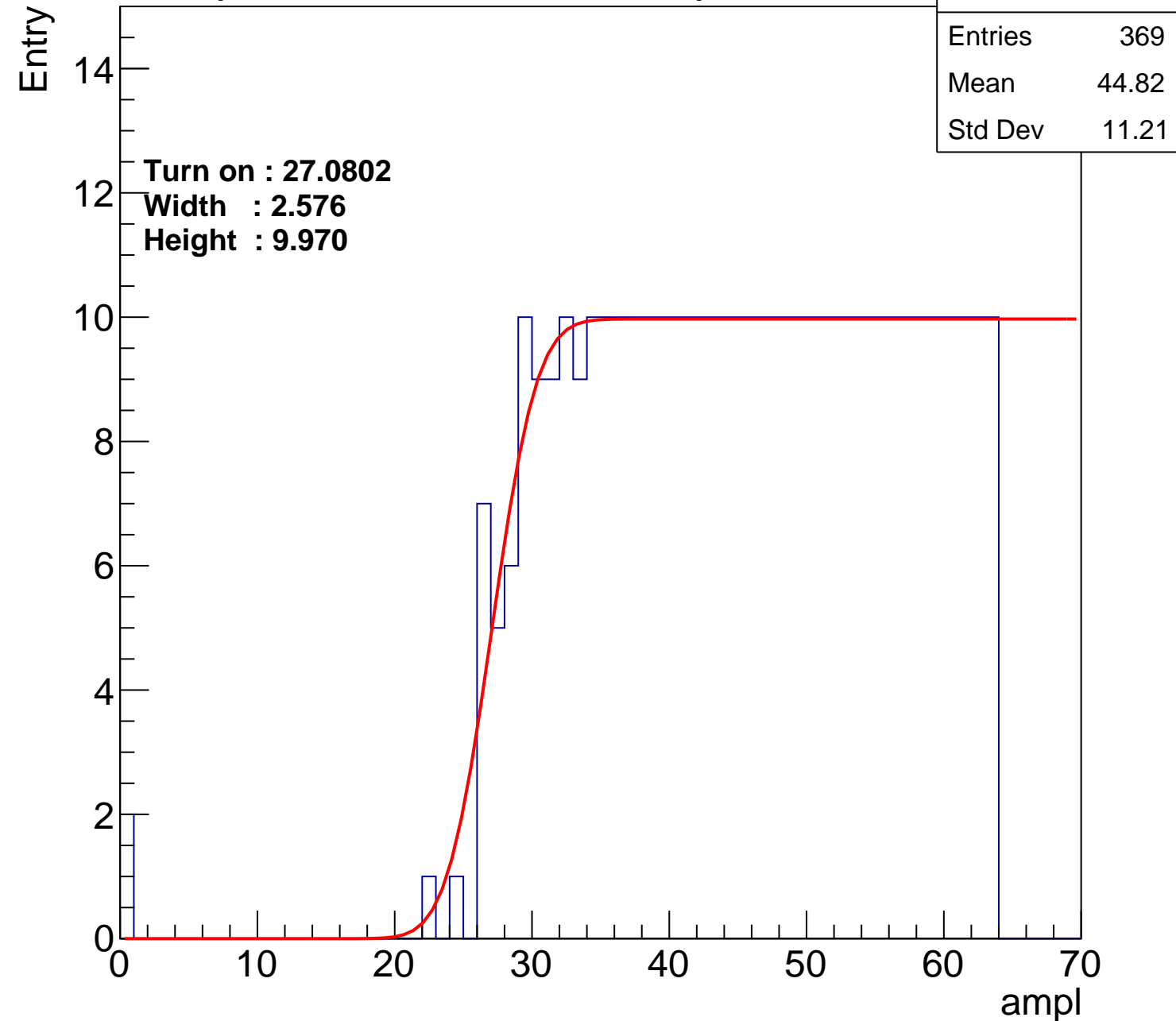
Width : 2.576

Height : 9.970

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch28

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	384
Mean	44.1
Std Dev	11.56

**Turn on : 26.0656**

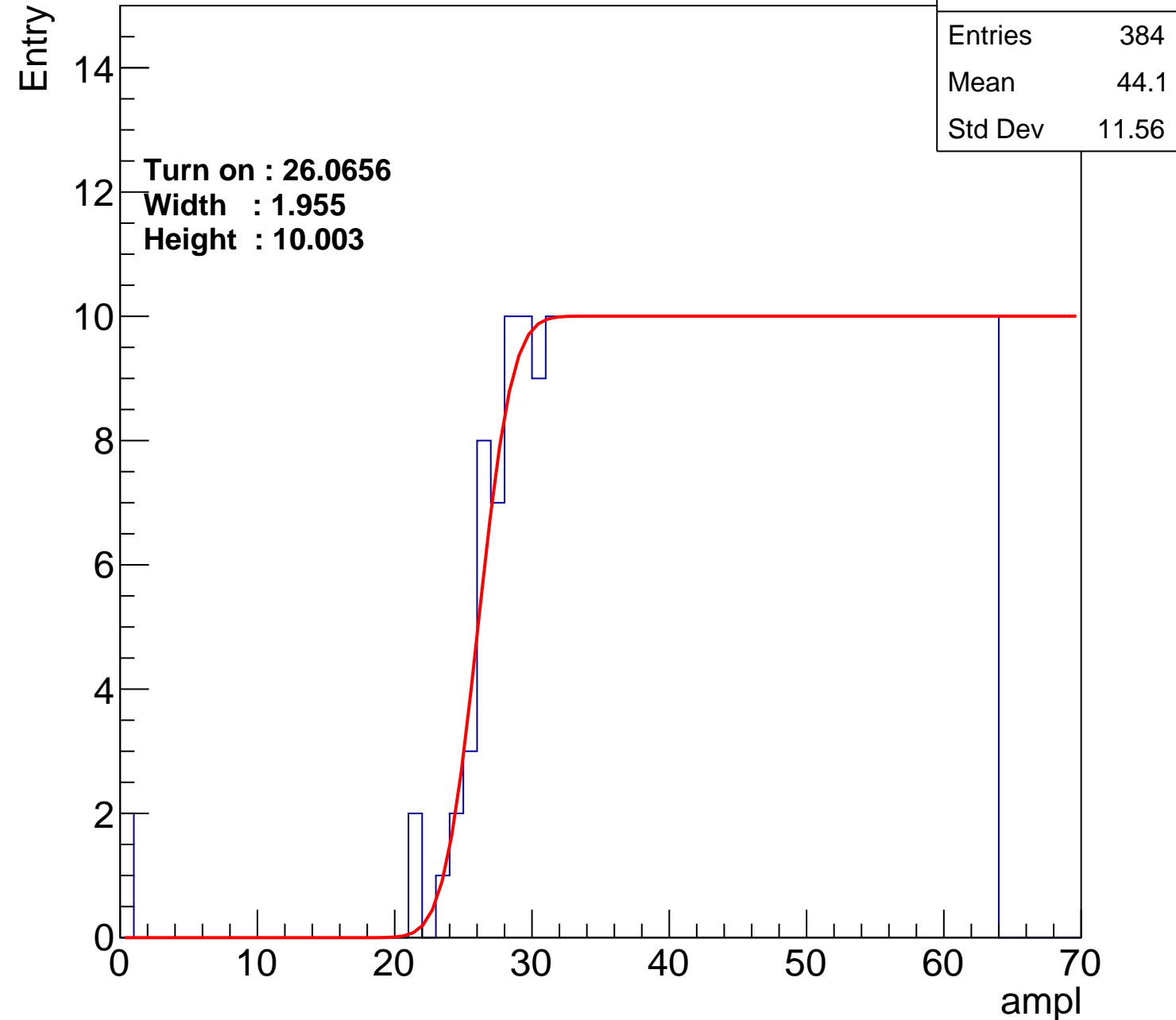
**Width : 1.955**

**Height : 10.003**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch29

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	387
Mean	43.93
Std Dev	11.69

Turn on : 25.8369

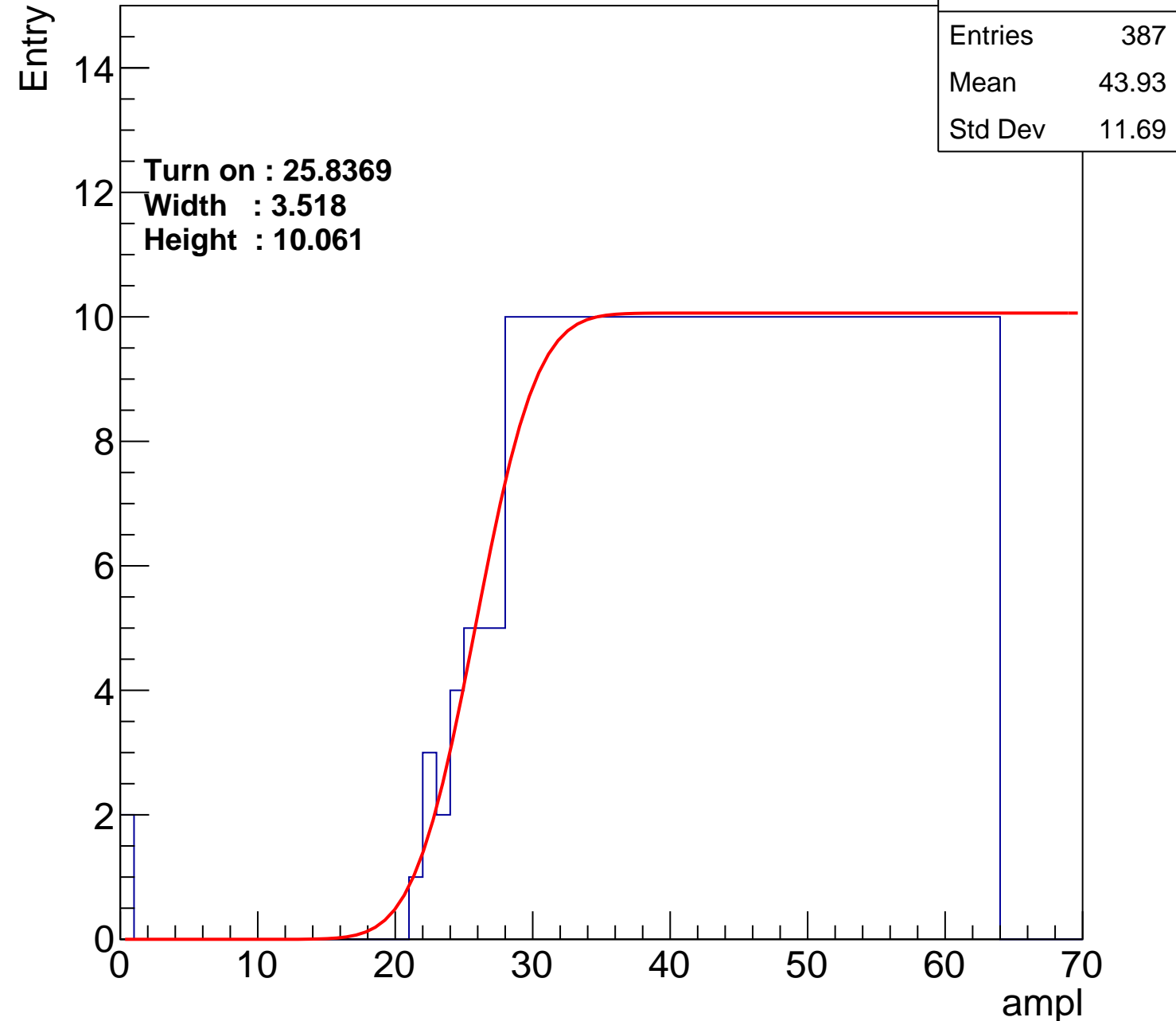
Width : 3.518

Height : 10.061

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch30

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	385
Mean	44.12
Std Dev	11.4

**Turn on : 25.4437**

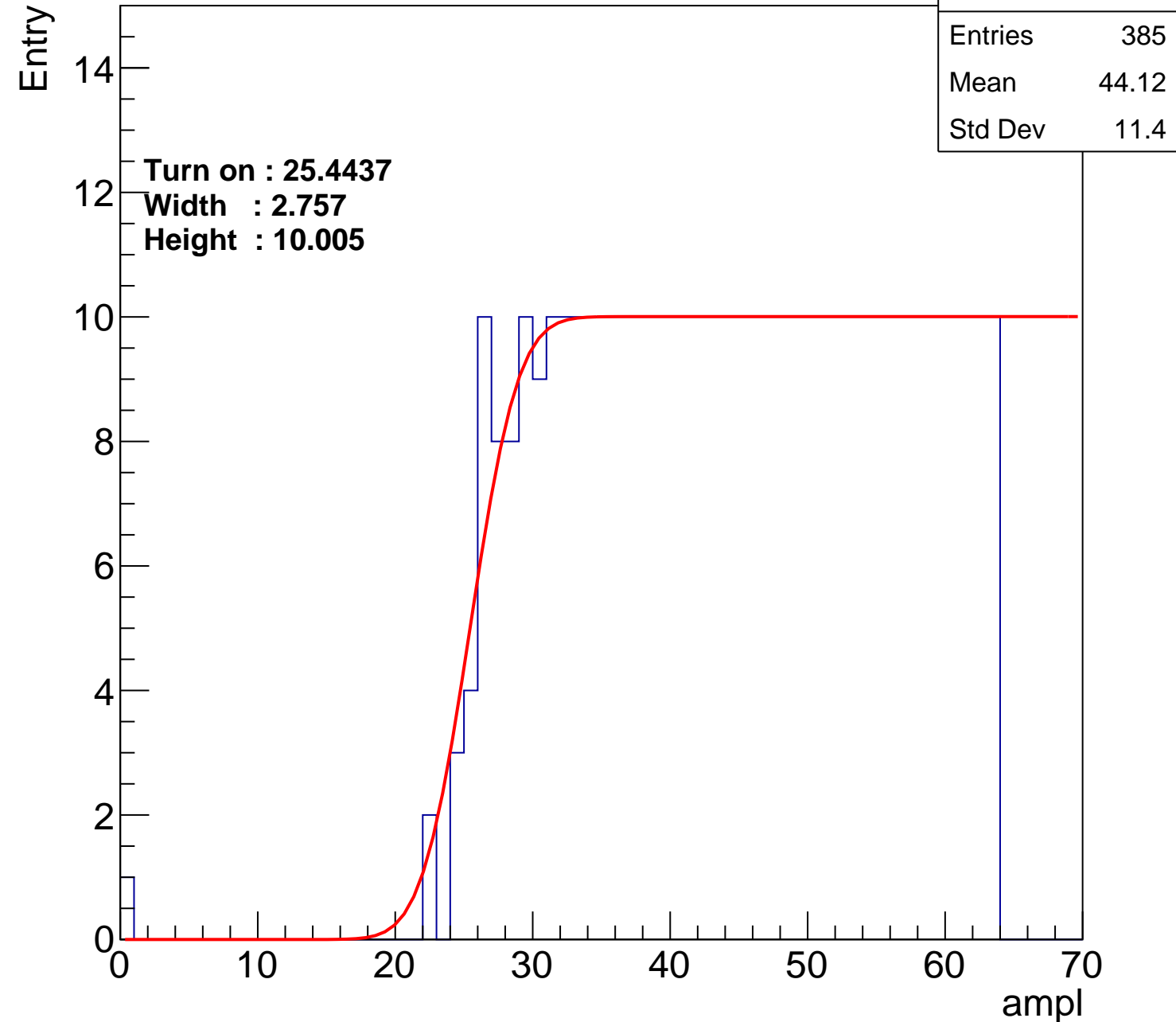
**Width : 2.757**

**Height : 10.005**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L000S, U7-ch31

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	377
Mean	44.45
Std Dev	11.37

Turn on : 26.5741

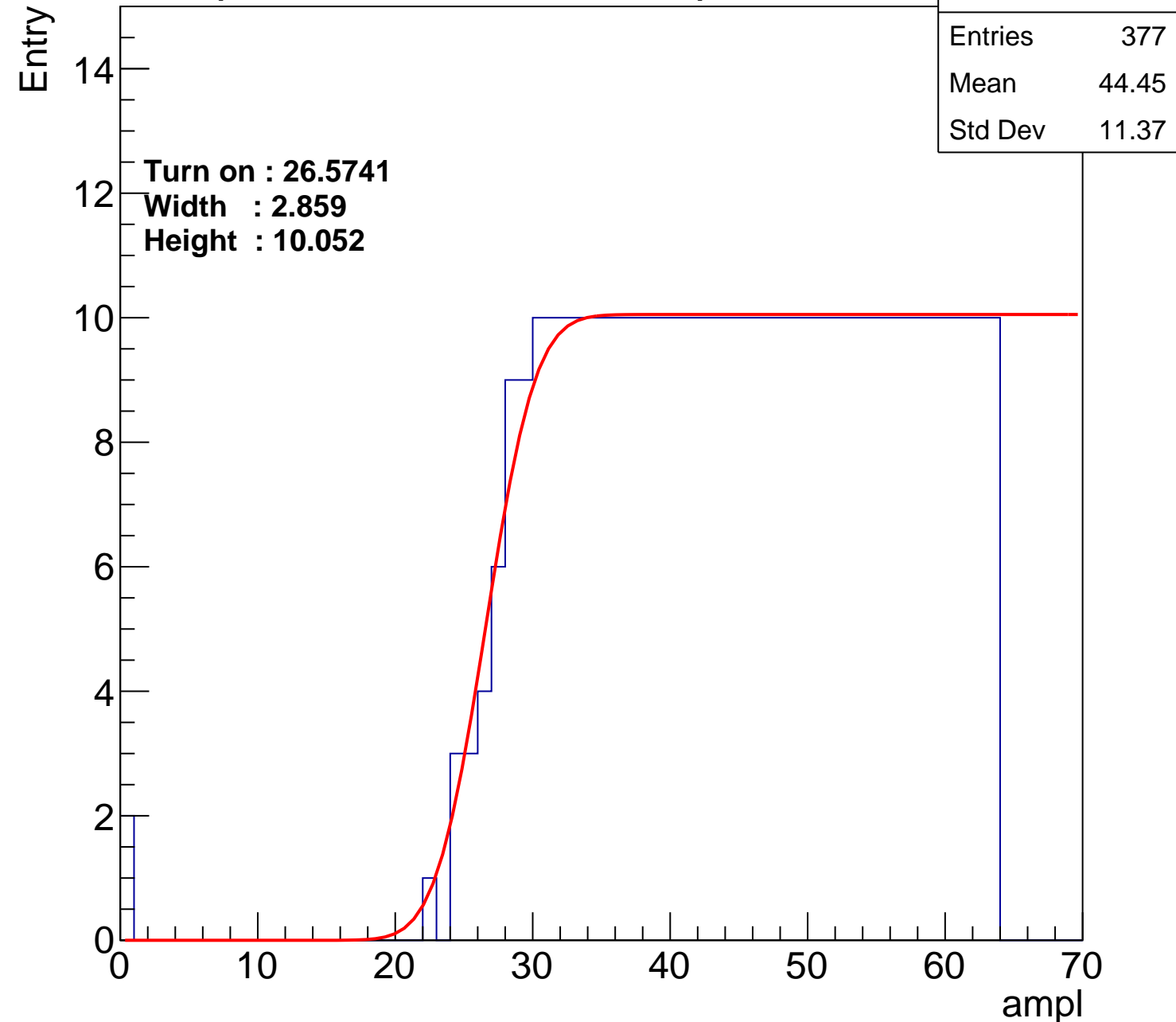
Width : 2.859

Height : 10.052

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch32

calib\_packv5\_042523\_0143.root, FC#3, port B3

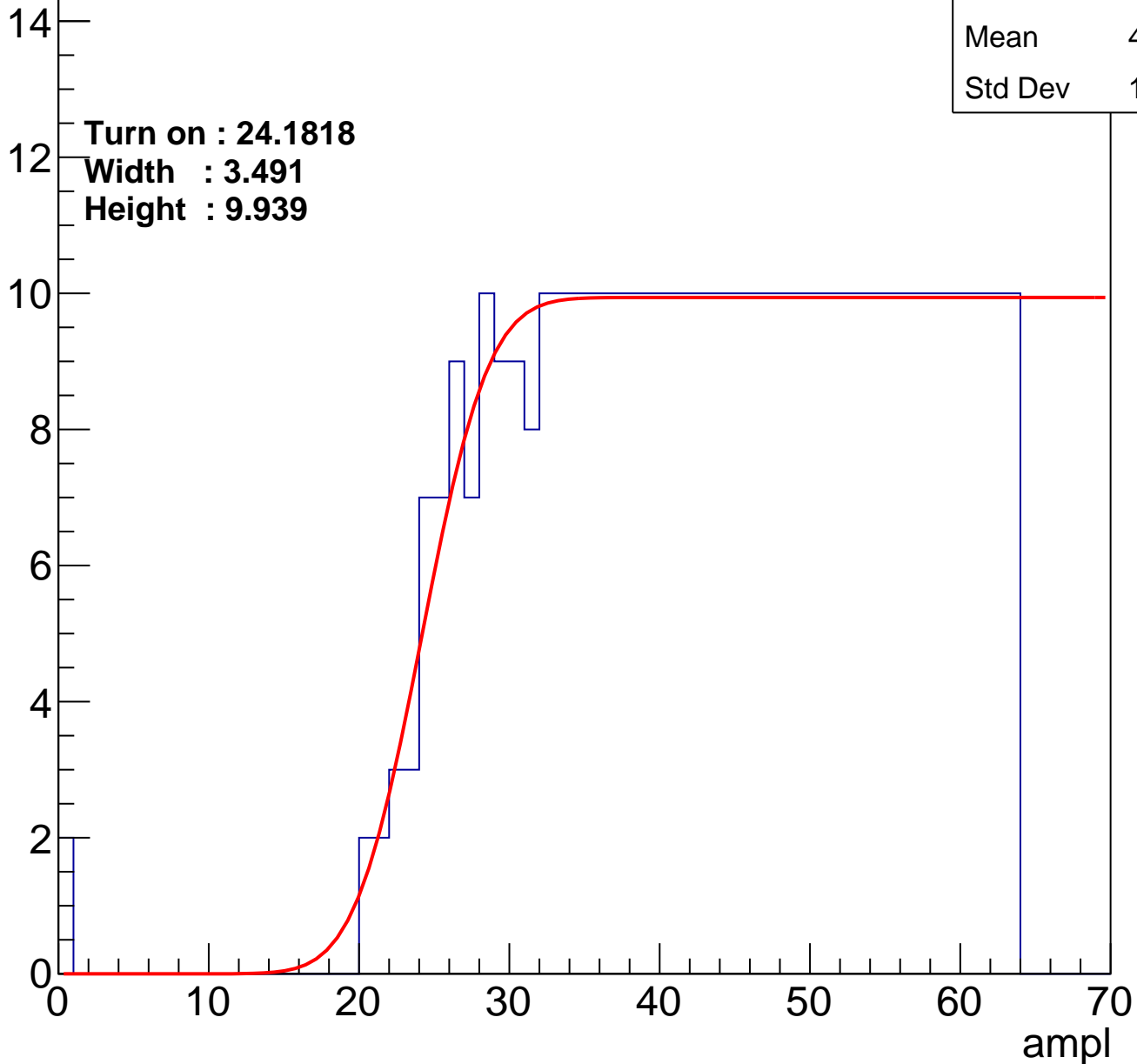
Entry

Entries	398
Mean	43.32
Std Dev	12.06

Turn on : 24.1818

Width : 3.491

Height : 9.939



# B1L000S, U7-ch33

calib\_packv5\_042523\_0143.root, FC#3, port B3

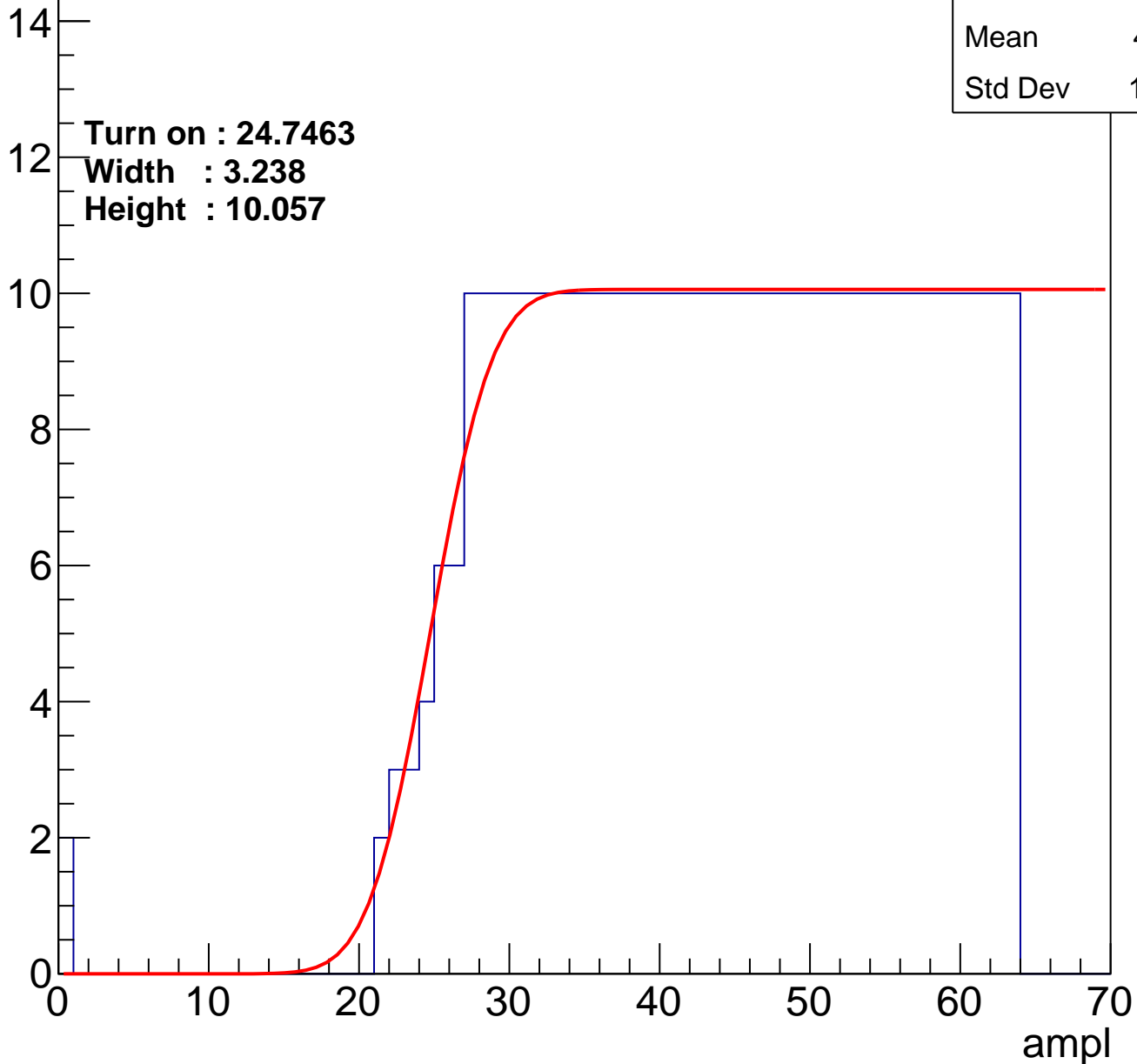
Entries	396
Mean	43.51
Std Dev	11.88

Turn on : 24.7463

Width : 3.238

Height : 10.057

Entry



# B1L000S, U7-ch34

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	384
Mean	44.16
Std Dev	11.4

**Turn on : 26.0025**

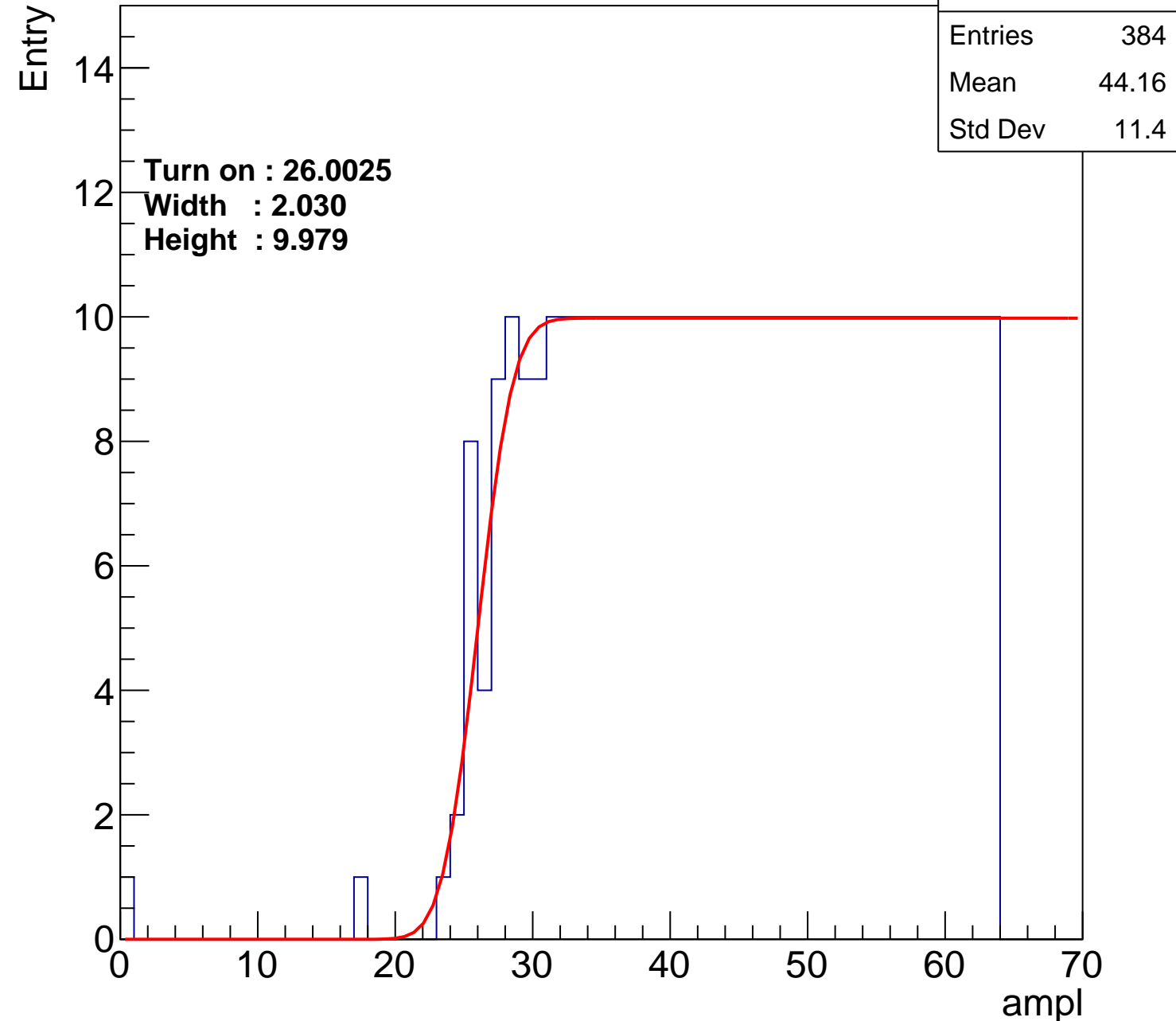
**Width : 2.030**

**Height : 9.979**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch35

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	386
Mean	44.01
Std Dev	11.6

**Turn on : 25.6504**

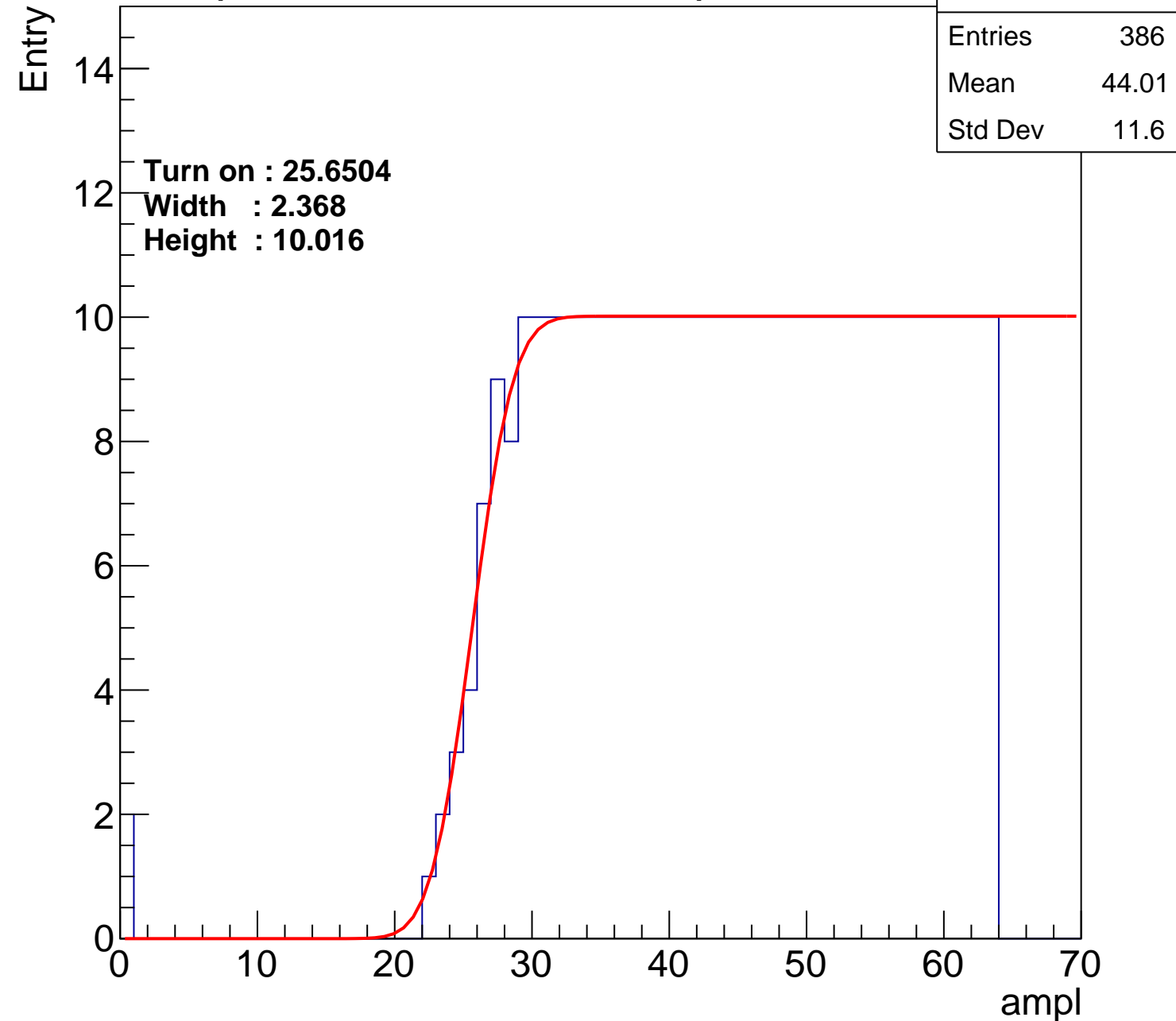
**Width : 2.368**

**Height : 10.016**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch36

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	371
Mean	44.81
Std Dev	11.03

**Turn on : 27.3290**

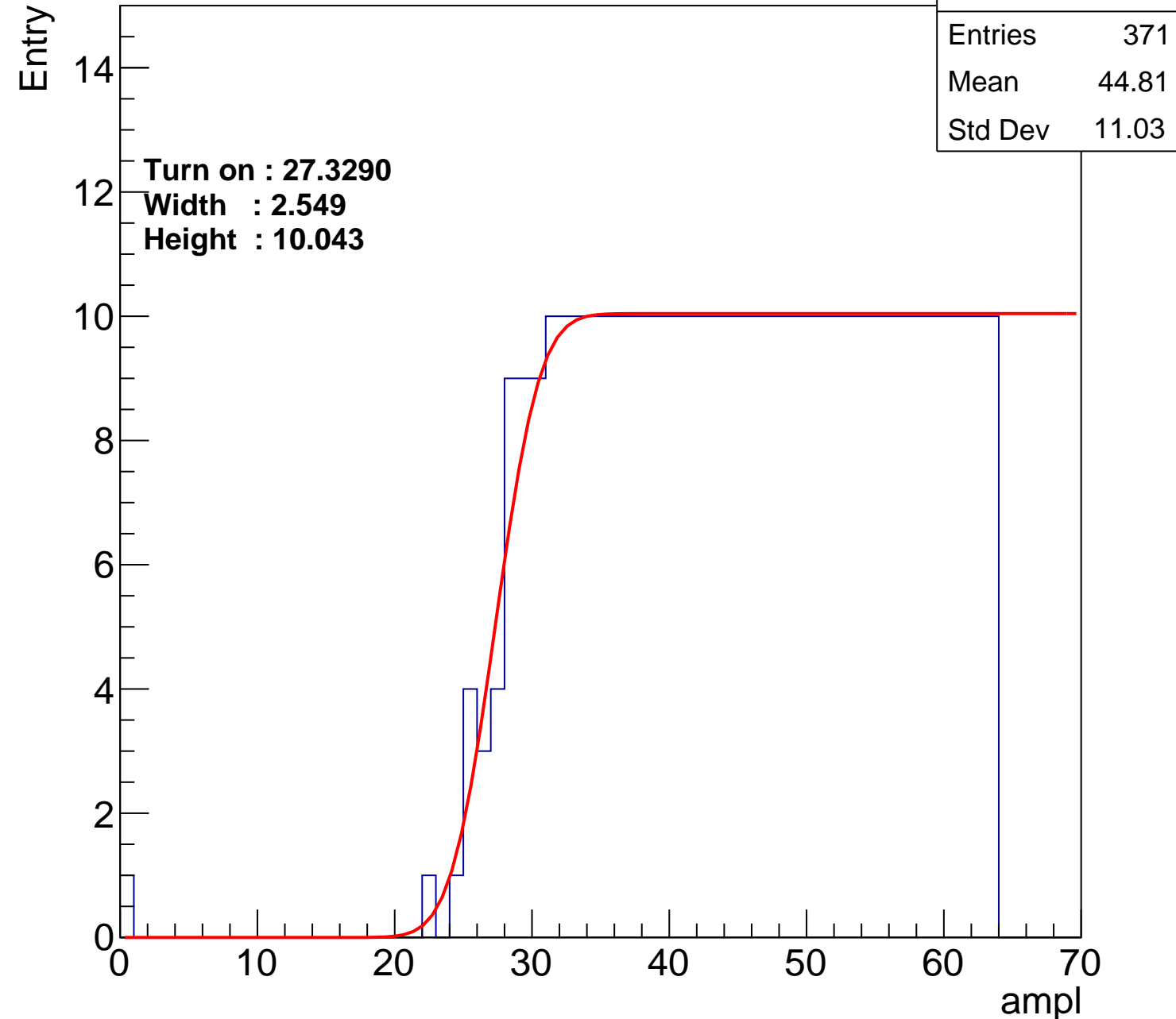
**Width : 2.549**

**Height : 10.043**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch37

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	390
Mean	43.73
Std Dev	11.91

Turn on : 25.1629

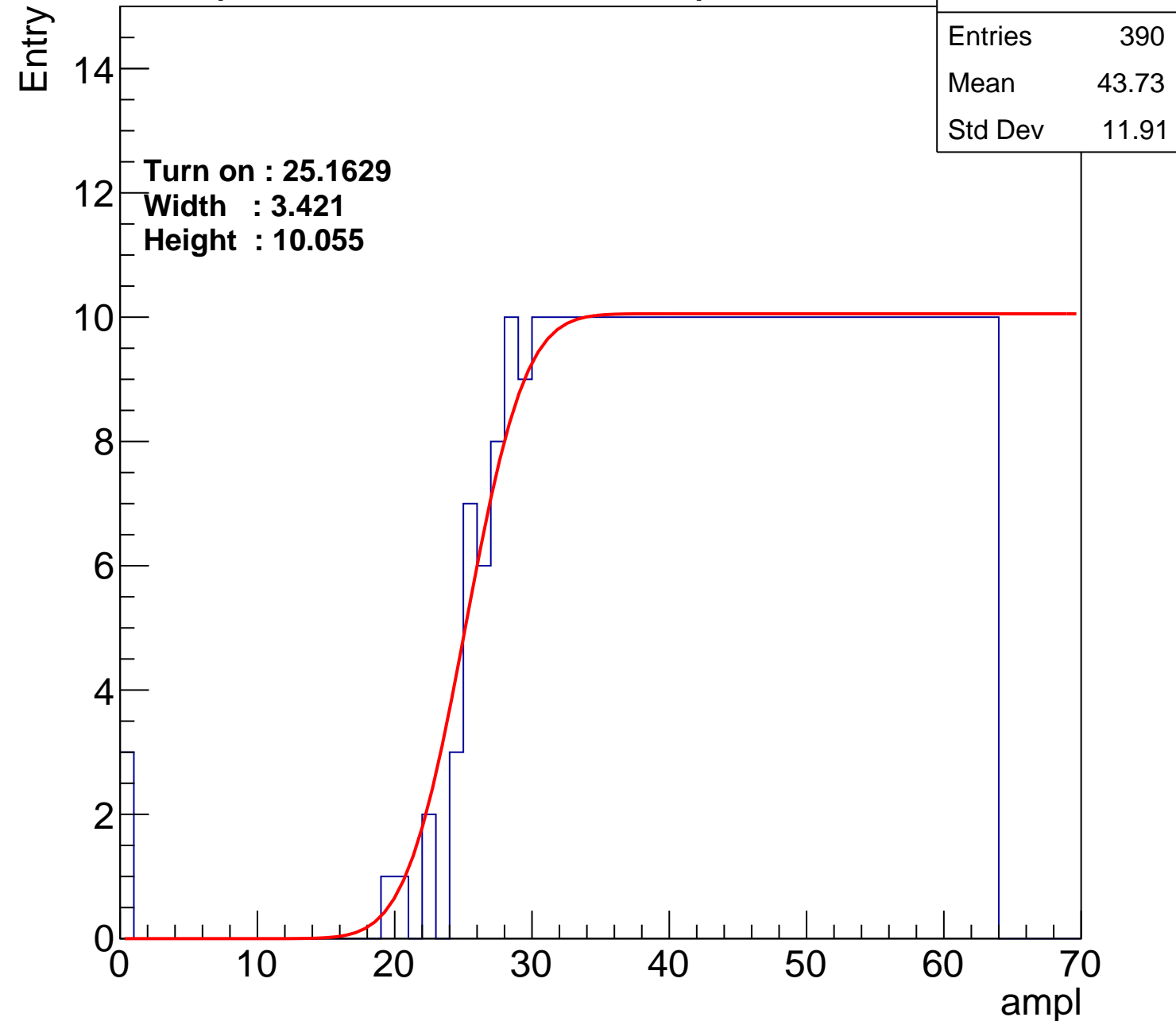
Width : 3.421

Height : 10.055

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch38

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	402
Mean	43.12
Std Dev	12.3

Turn on : 24.2501

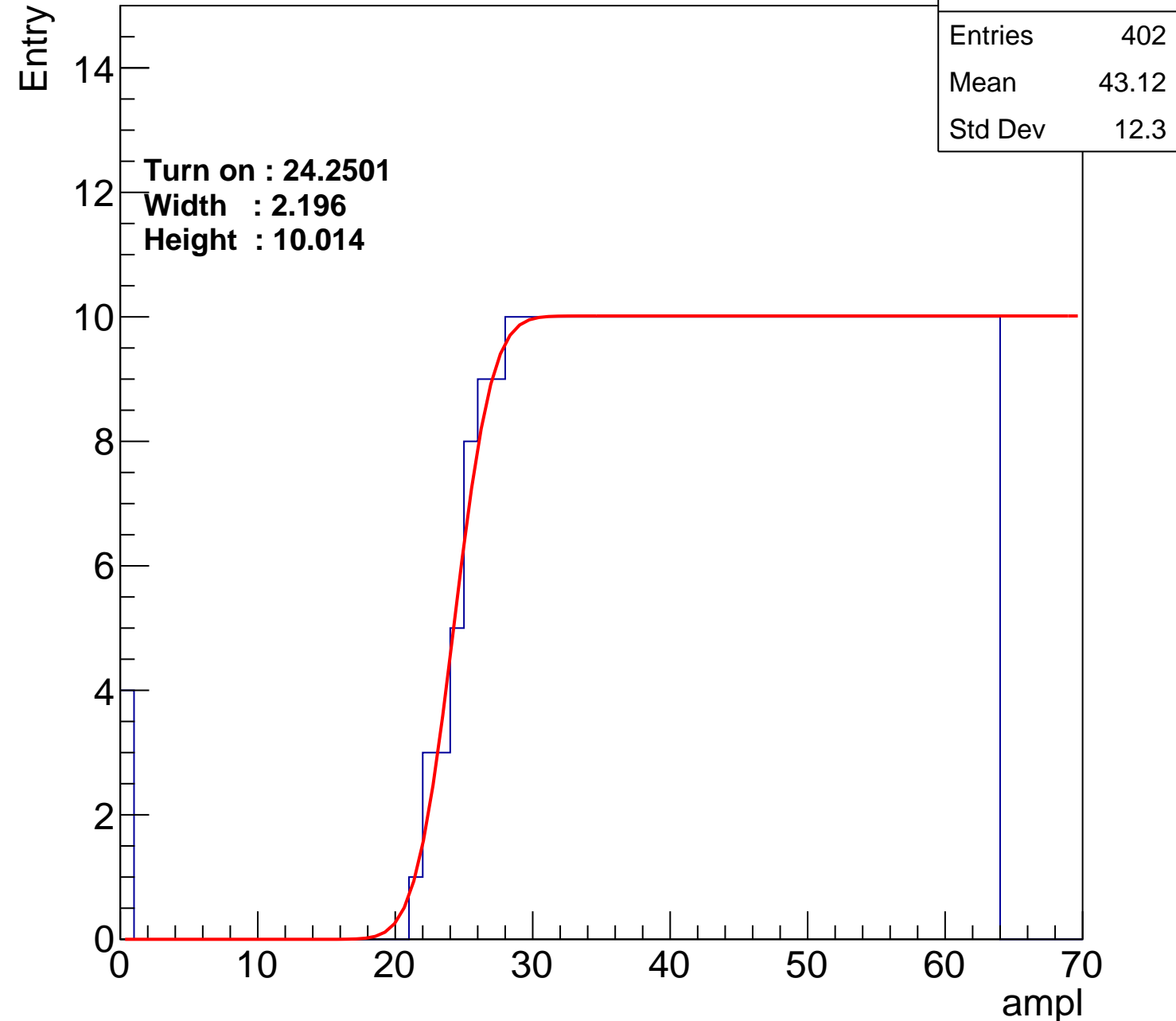
Width : 2.196

Height : 10.014

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L000S, U7-ch39

calib\_packv5\_042523\_0143.root, FC#3, port B3

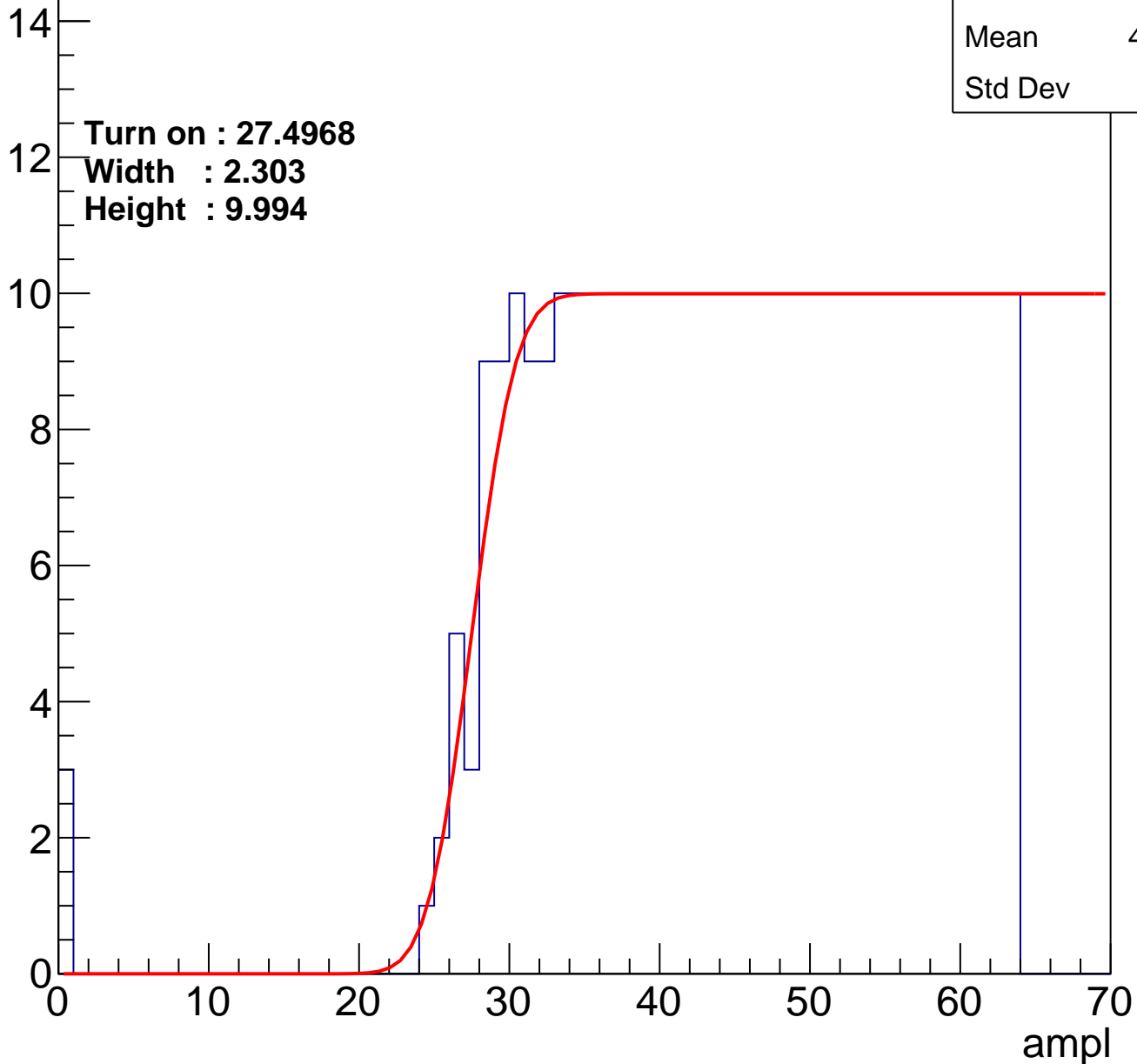
Entry

Entries	370
Mean	44.72
Std Dev	11.4

Turn on : 27.4968

Width : 2.303

Height : 9.994



# B1L000S, U7-ch40

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	385
Mean	44
Std Dev	11.66

Turn on : 25.2361

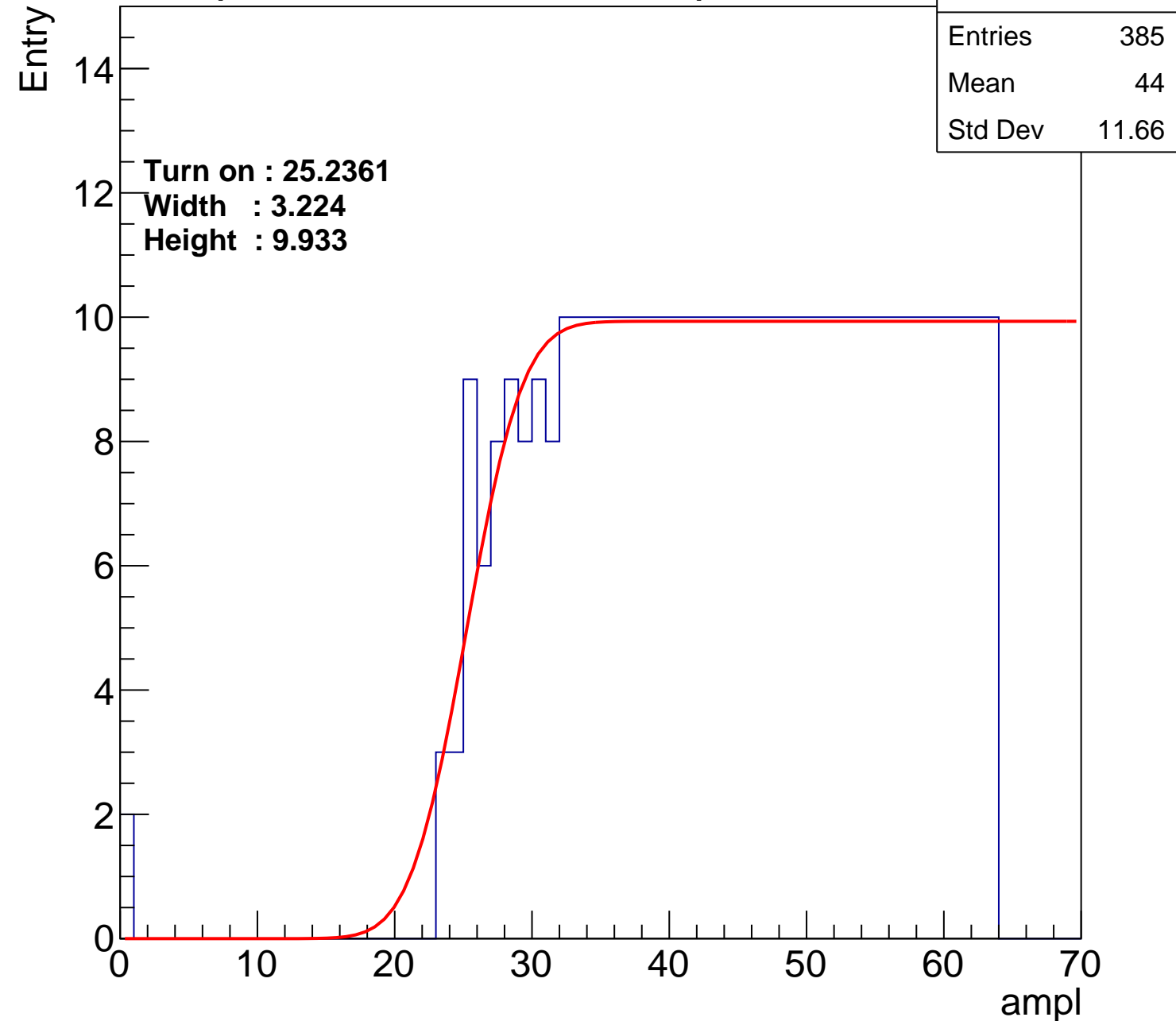
Width : 3.224

Height : 9.933

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch41

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	374
Mean	44.51
Std Dev	11.52

**Turn on : 27.5409**

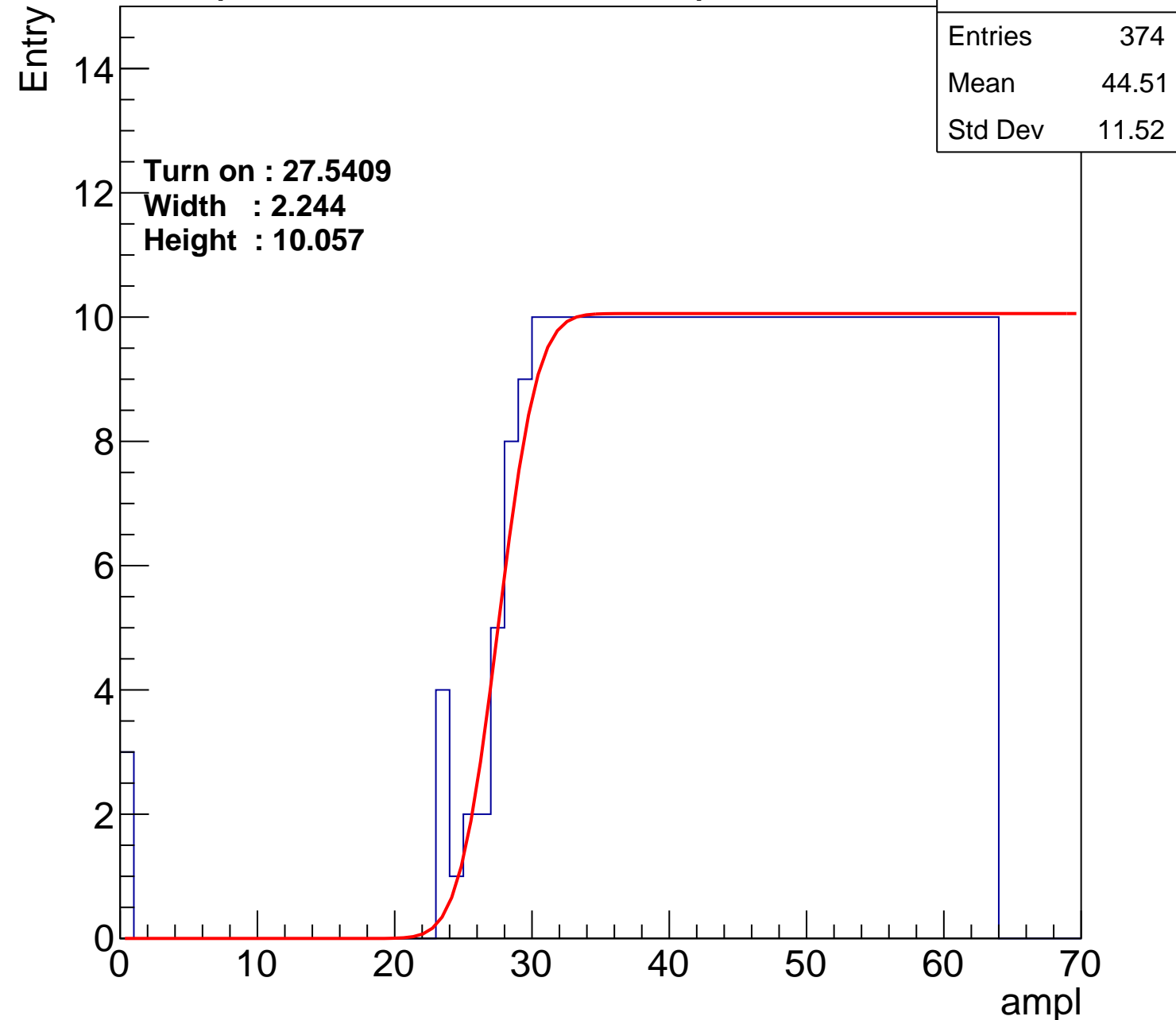
**Width : 2.244**

**Height : 10.057**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch42

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	386
Mean	44.03
Std Dev	11.57

**Turn on : 24.7128**

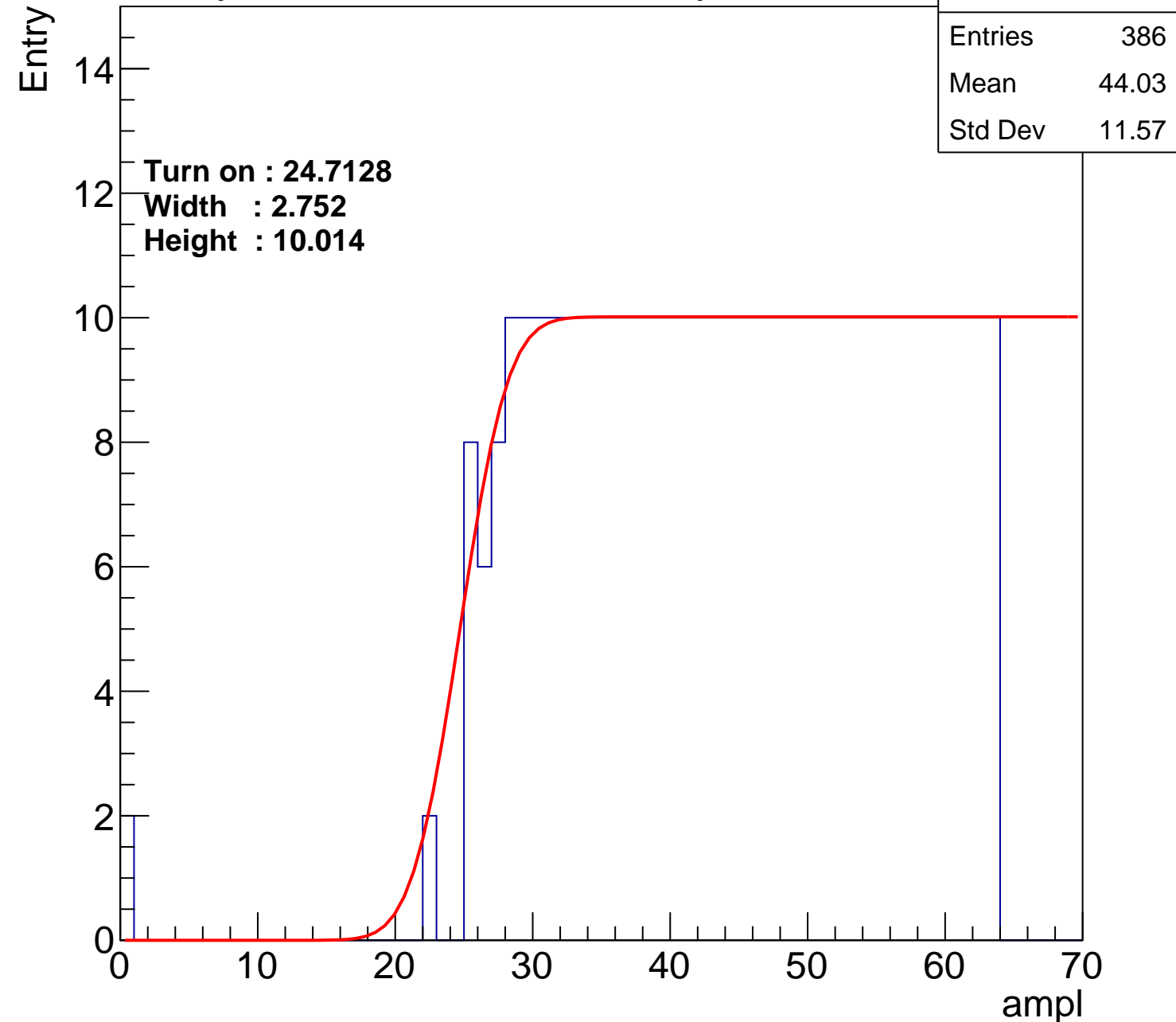
**Width : 2.752**

**Height : 10.014**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch43

calib\_packv5\_042523\_0143.root, FC#3, port B3

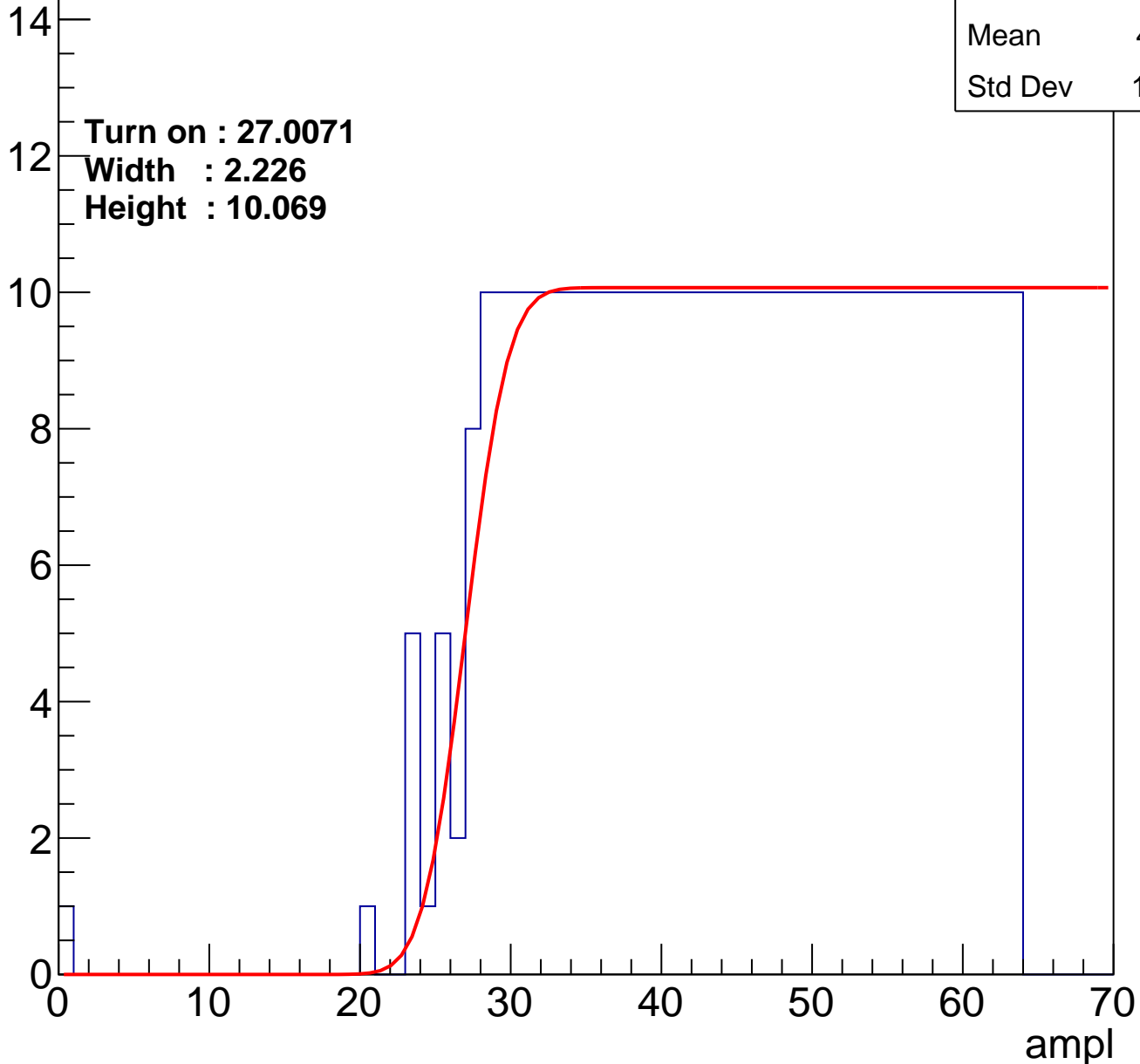
Entries	383
Mean	44.21
Std Dev	11.37

Turn on : 27.0071

Width : 2.226

Height : 10.069

Entry



# B1L000S, U7-ch44

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	403
Mean	43.09
Std Dev	12.23

Turn on : 24.1802

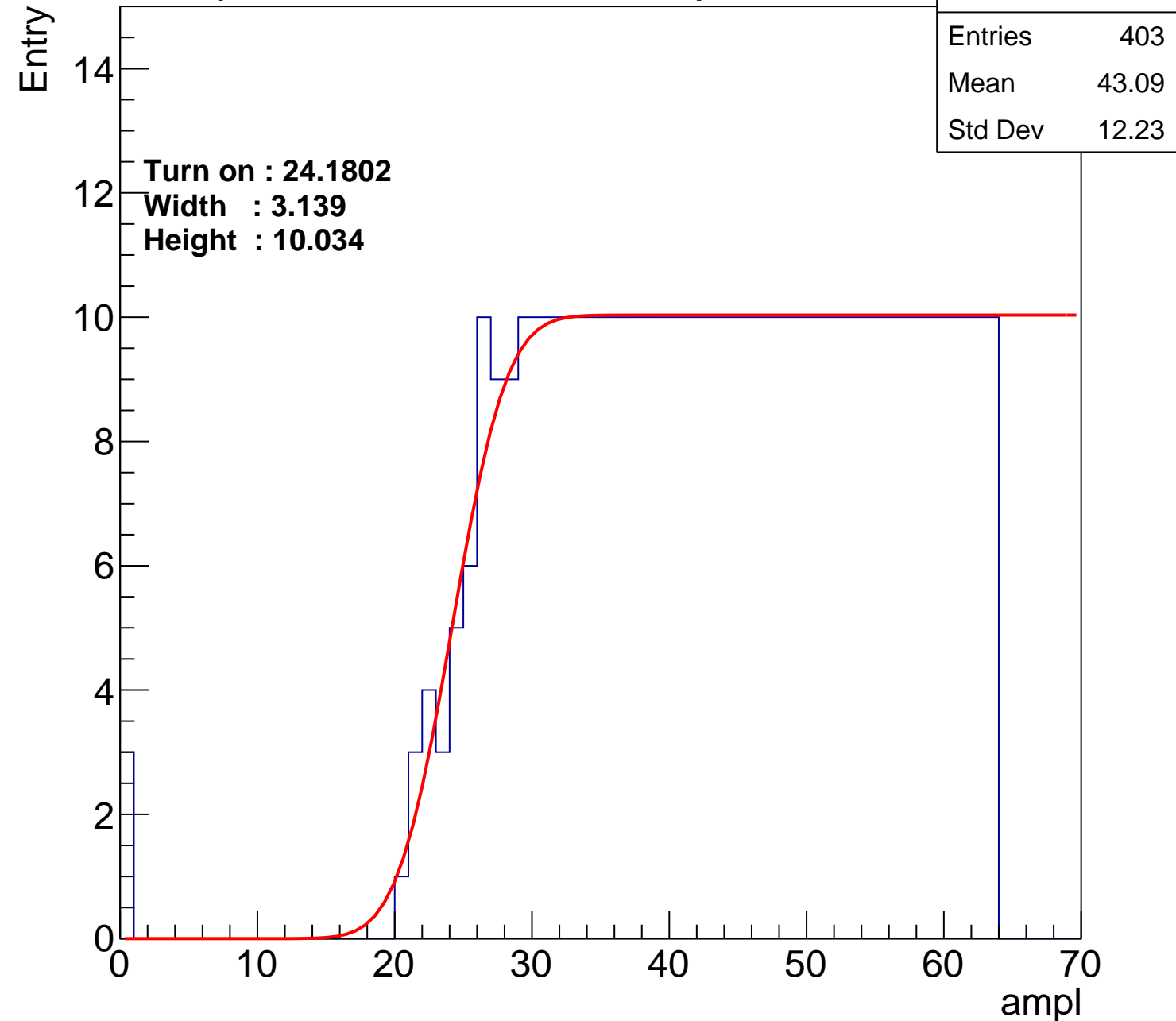
Width : 3.139

Height : 10.034

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch45

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	380
Mean	44.33
Std Dev	11.32

Turn on : 26.1104

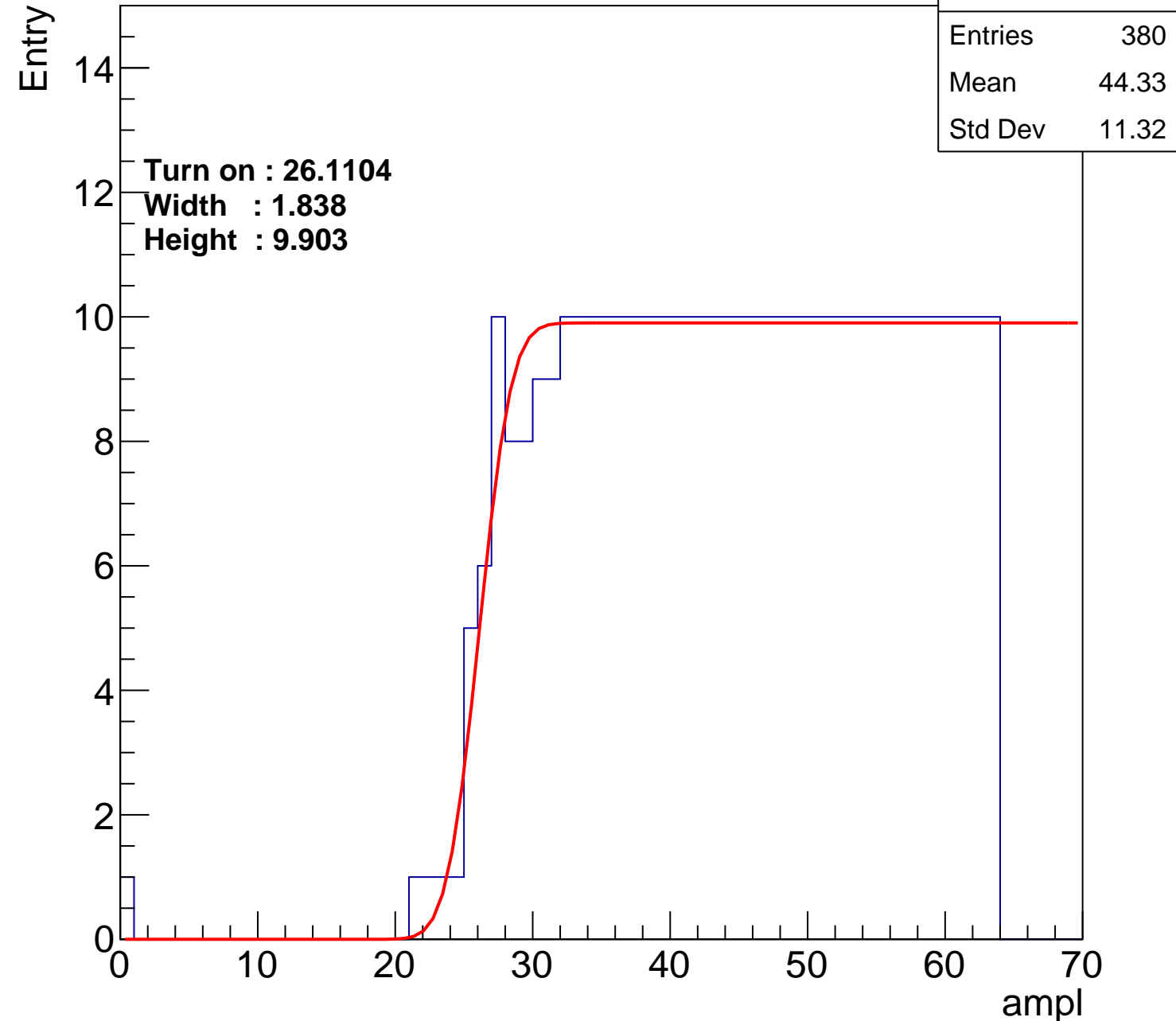
Width : 1.838

Height : 9.903

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch46

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	385
Mean	44.08
Std Dev	11.46

**Turn on : 25.5550**

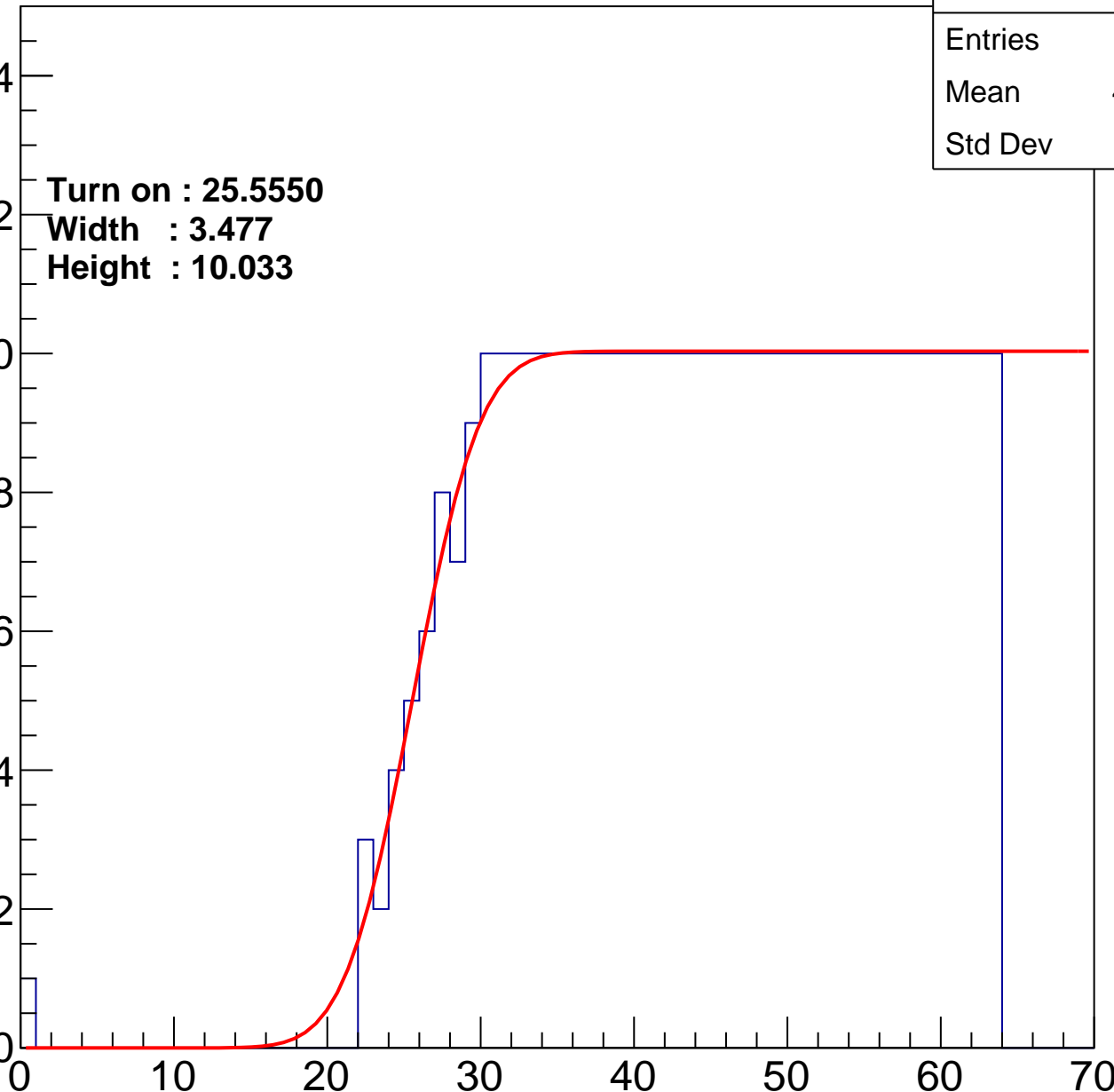
**Width : 3.477**

**Height : 10.033**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L000S, U7-ch47

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	370
Mean	44.66
Std Dev	11.5

Turn on : 27.9714

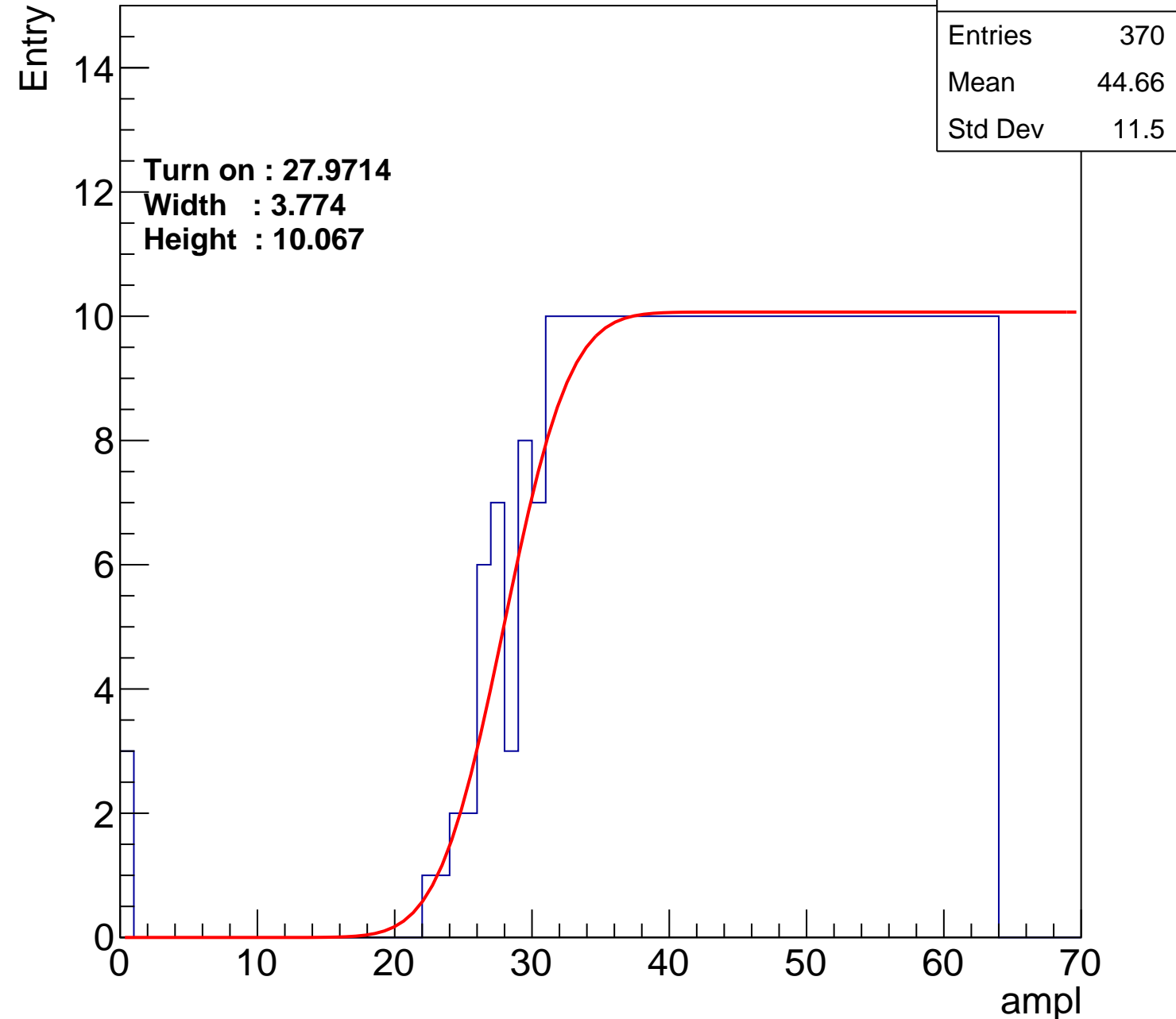
Width : 3.774

Height : 10.067

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch48

calib\_packv5\_042523\_0143.root, FC#3, port B3

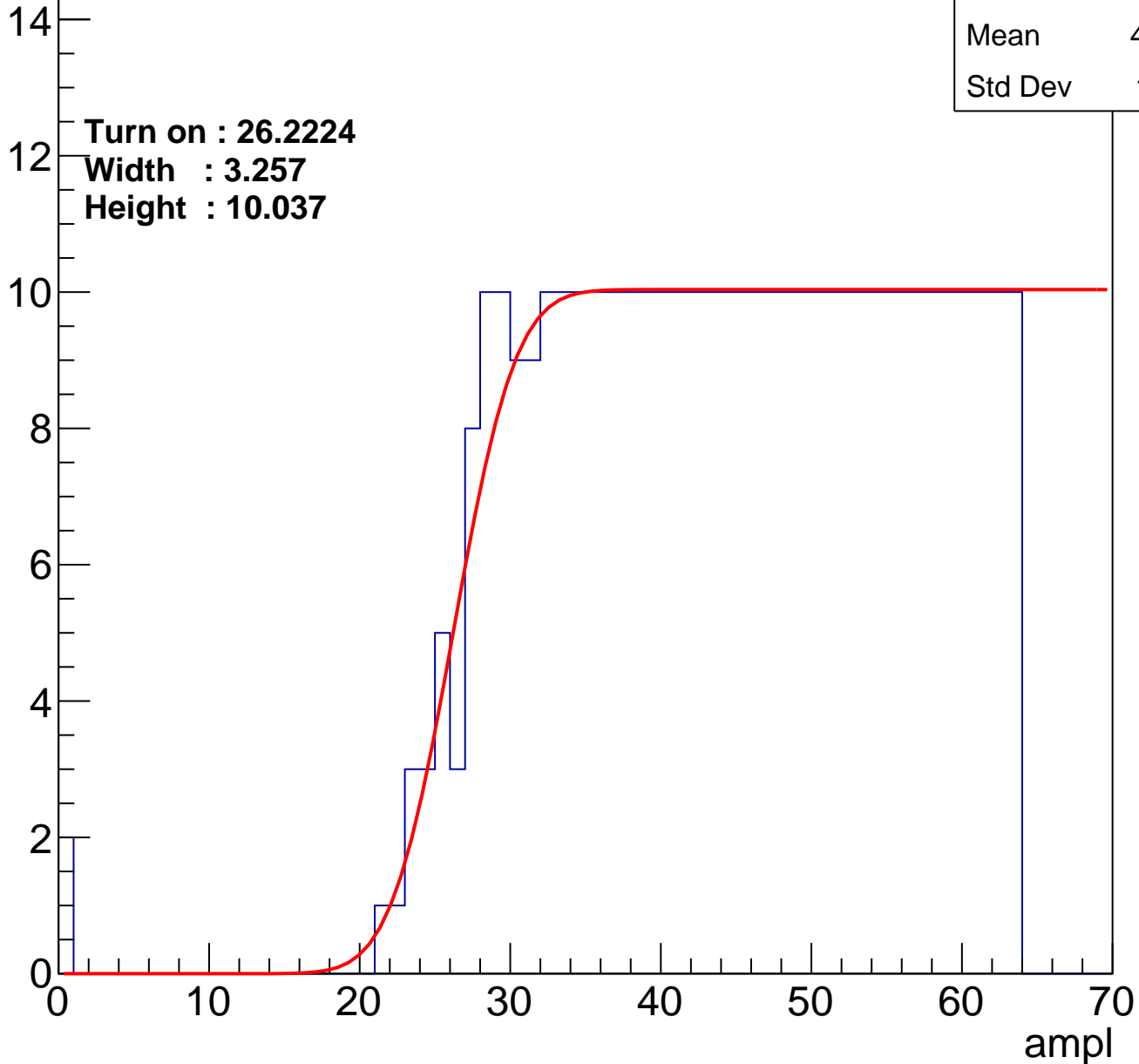
Entries	384
Mean	44.07
Std Dev	11.61

Turn on : 26.2224

Width : 3.257

Height : 10.037

Entry



# B1L000S, U7-ch49

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	391
Mean	43.74
Std Dev	11.76

**Turn on : 25.4403**

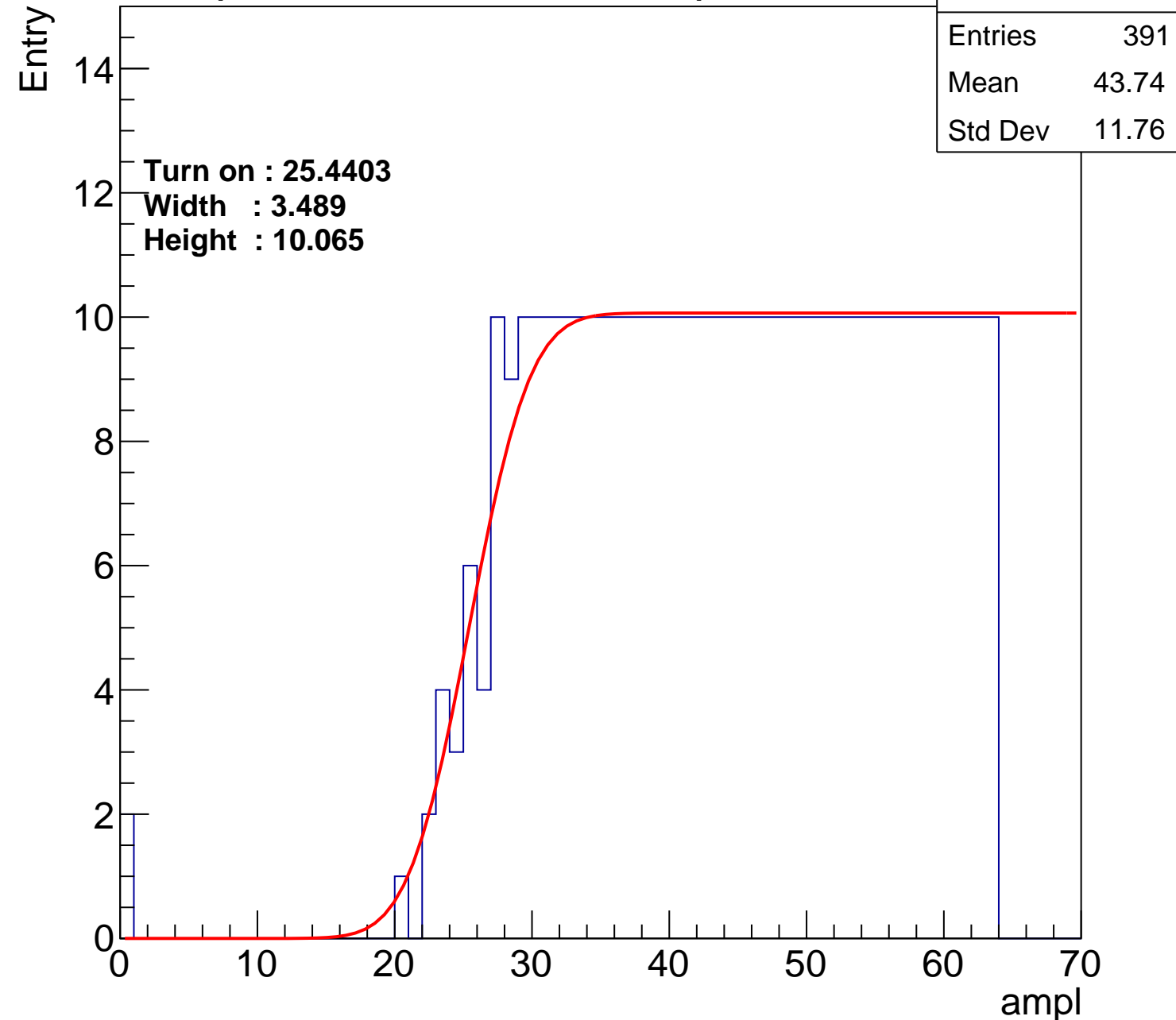
**Width : 3.489**

**Height : 10.065**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch50

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	386
Mean	43.84
Std Dev	12

Turn on : 26.5625

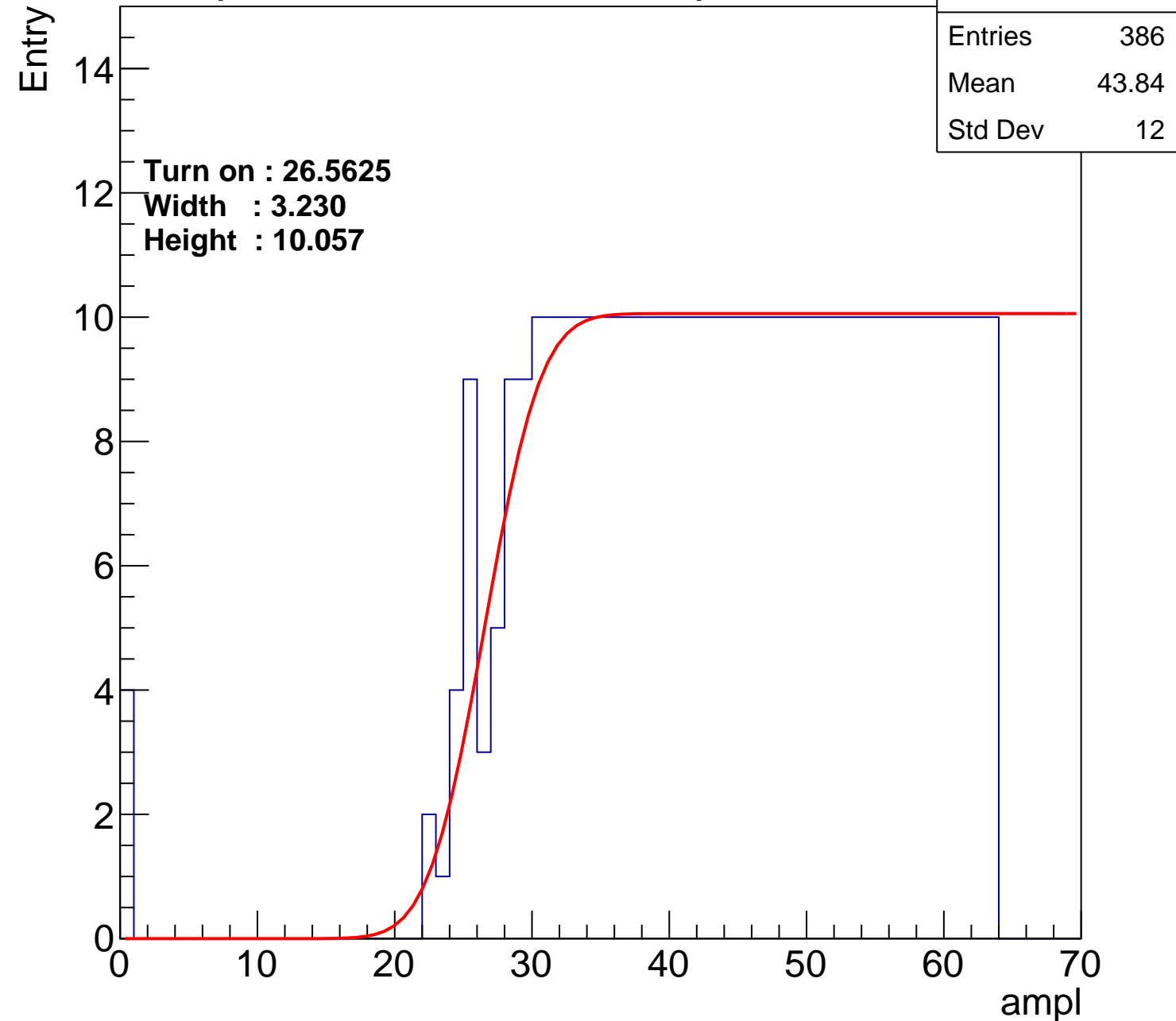
Width : 3.230

Height : 10.057

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch51

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	390
Mean	43.81
Std Dev	11.7

Turn on : 24.7453

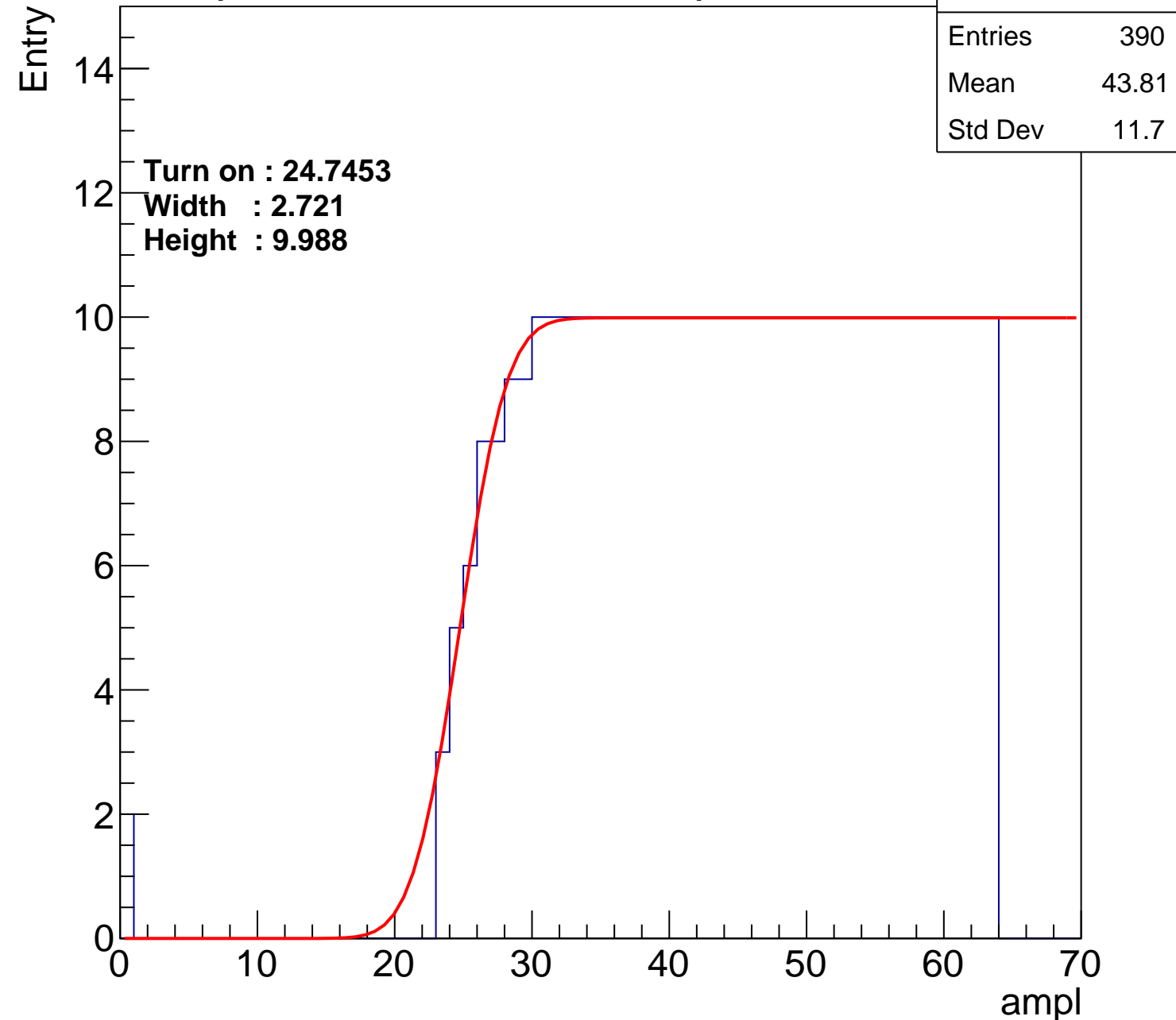
Width : 2.721

Height : 9.988

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch52

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	377
Mean	44.43
Std Dev	11.41

**Turn on : 26.7782**

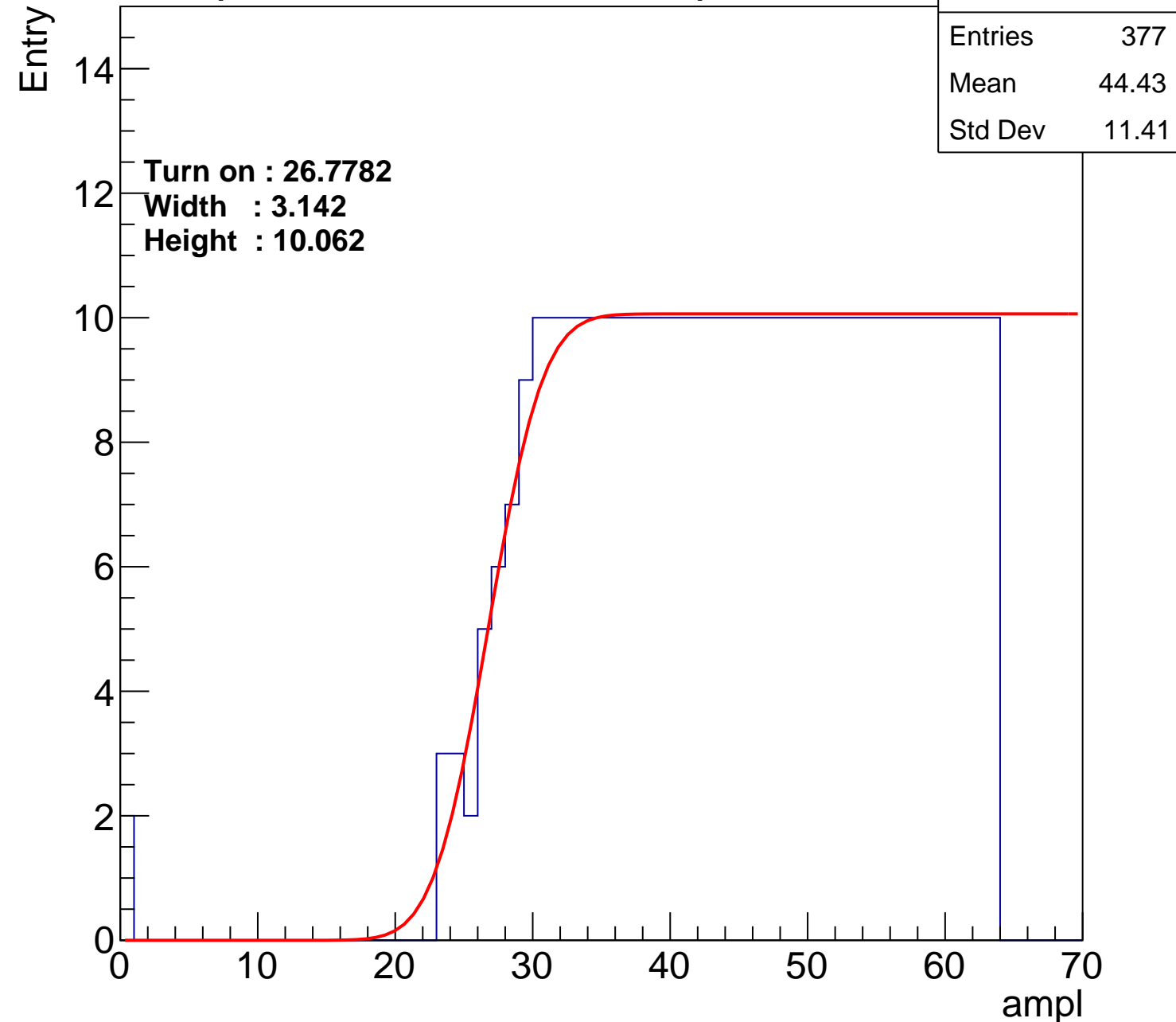
**Width : 3.142**

**Height : 10.062**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch53

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	404
Mean	43
Std Dev	12.38

Turn on : 24.5796

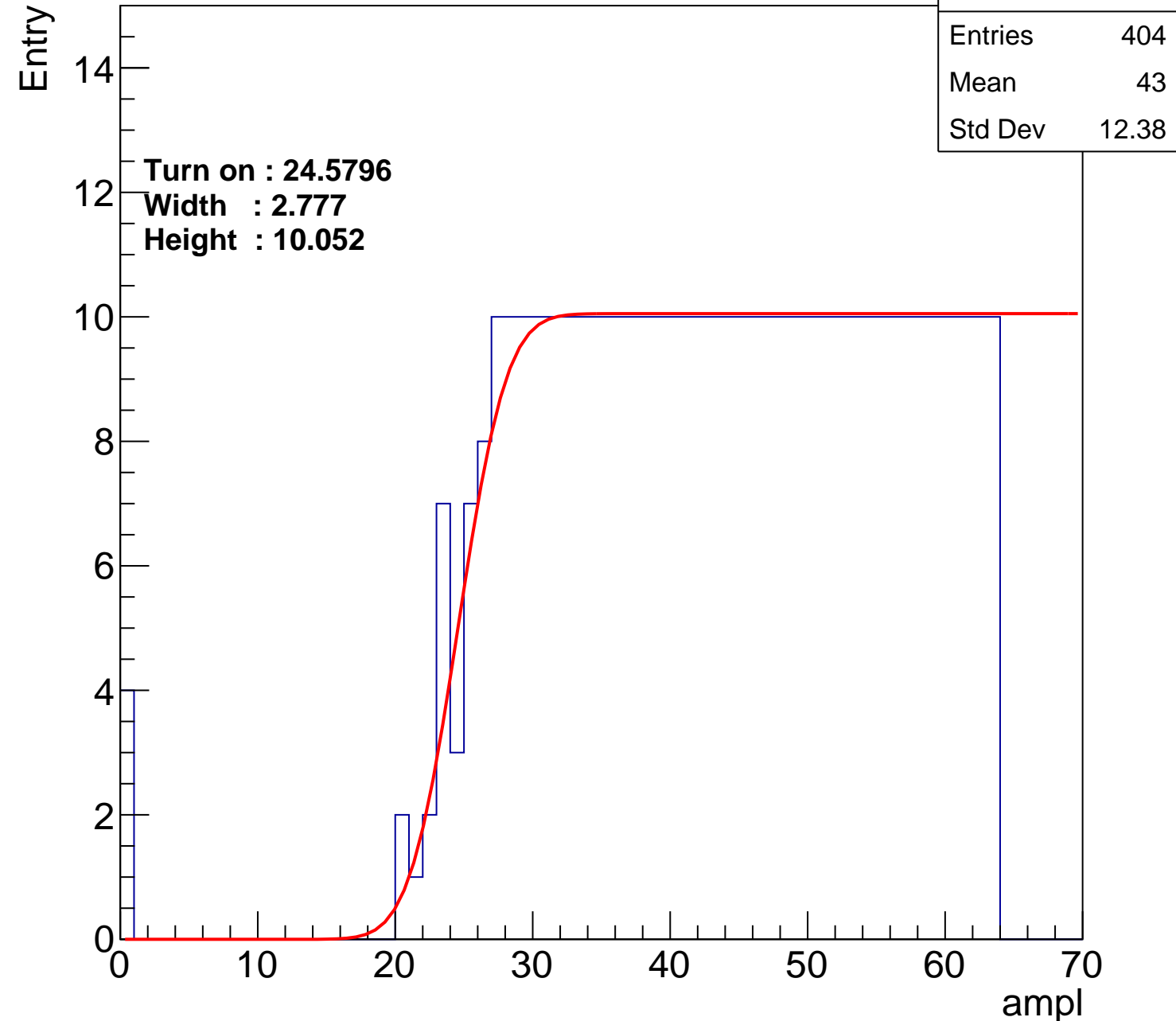
Width : 2.777

Height : 10.052

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch54

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	374
Mean	44.44
Std Dev	11.71

Turn on : 27.1564

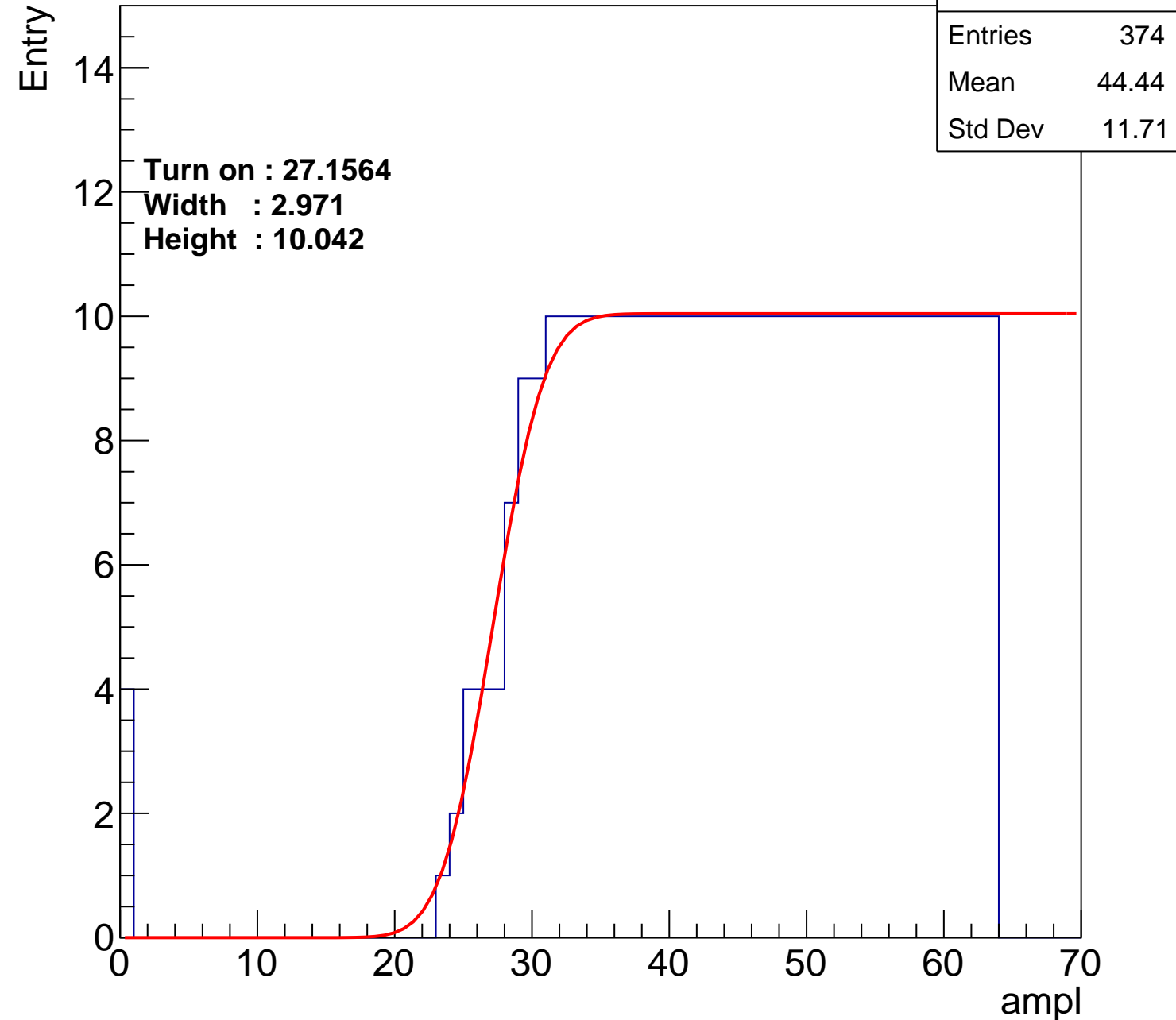
Width : 2.971

Height : 10.042

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L000S, U7-ch55

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	381
Mean	44.22
Std Dev	11.54

**Turn on : 26.2398**

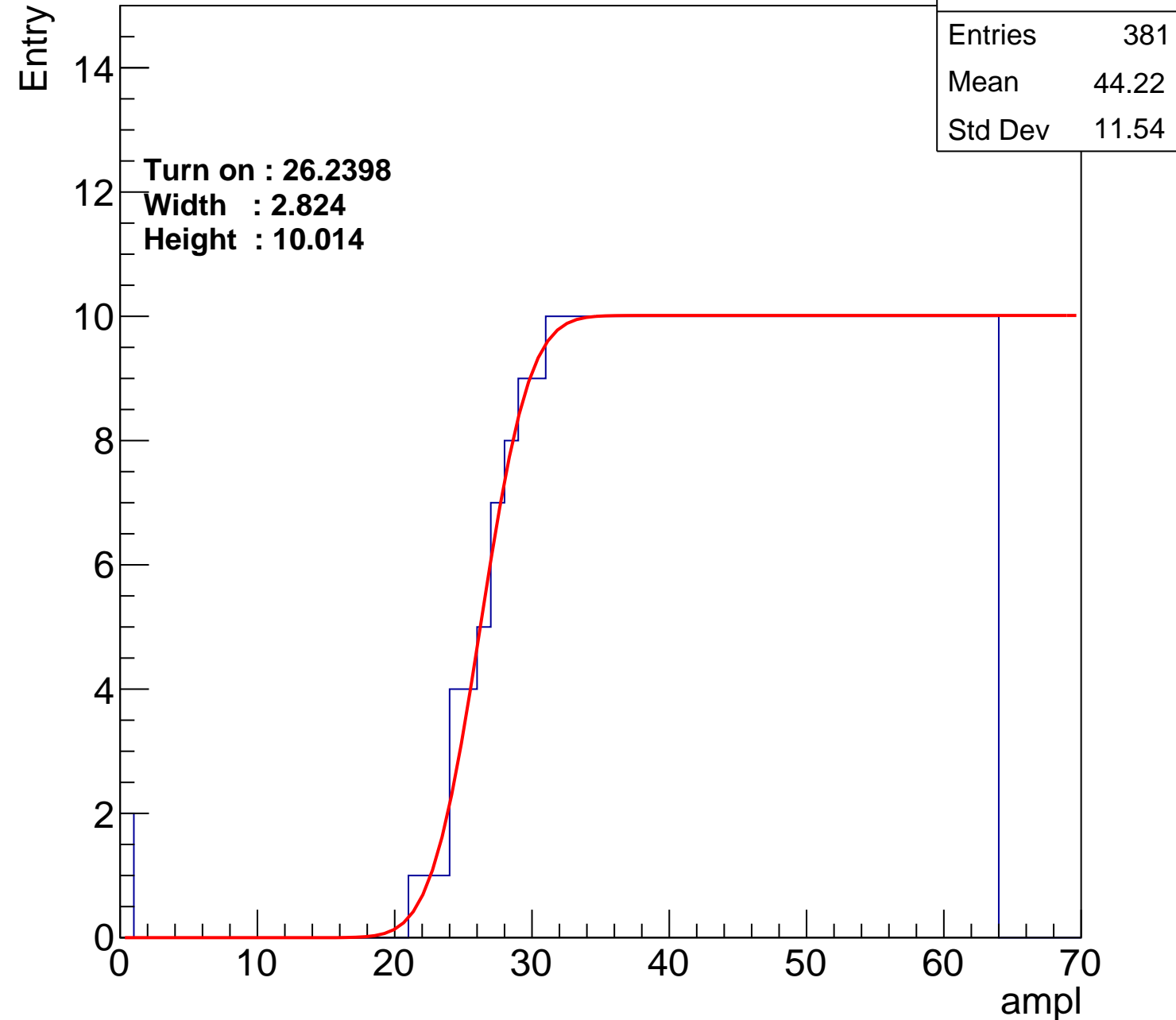
**Width : 2.824**

**Height : 10.014**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch56

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	385
Mean	44.02
Std Dev	11.72

**Turn on : 25.8054**

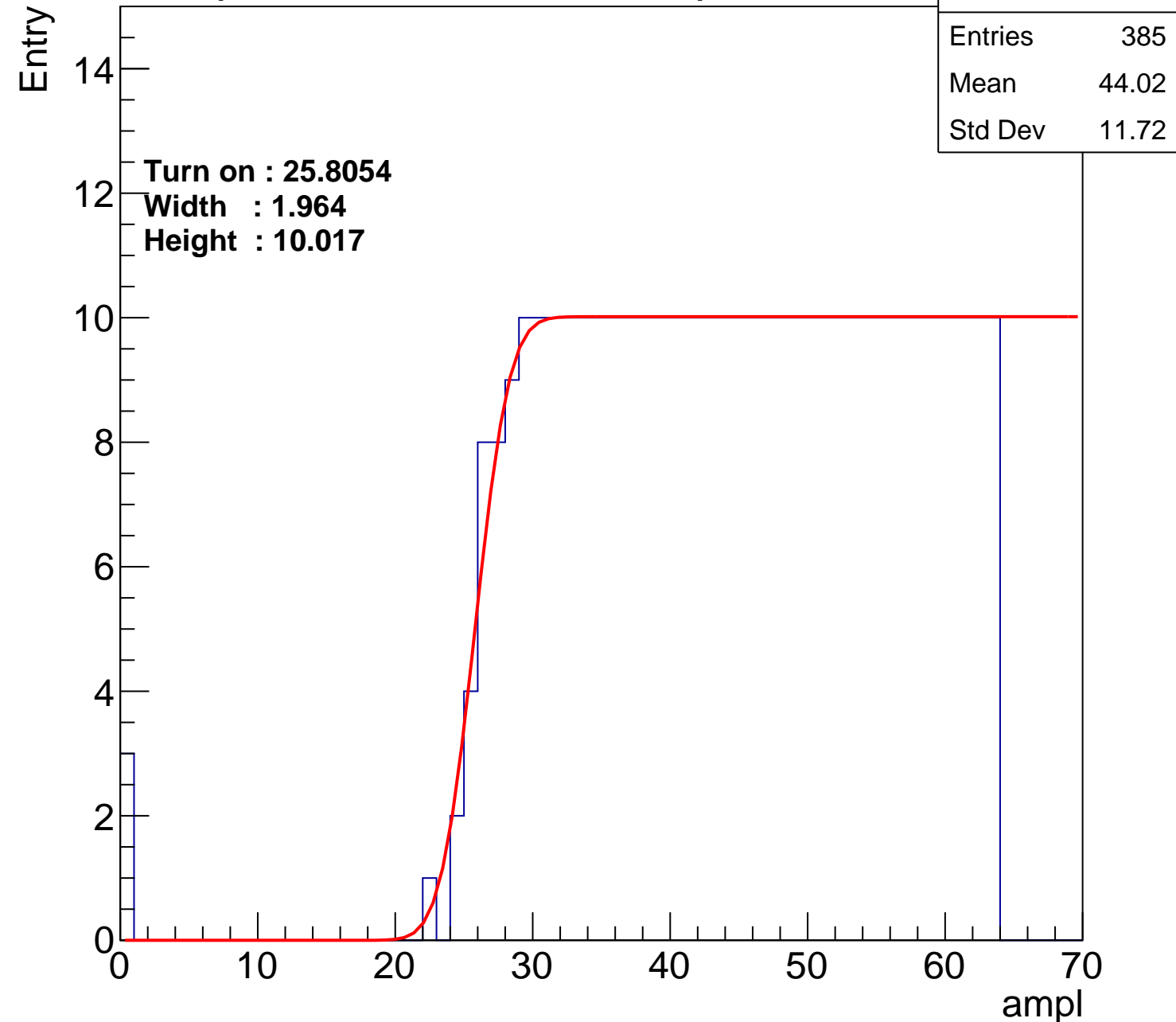
**Width : 1.964**

**Height : 10.017**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch57

calib\_packv5\_042523\_0143.root, FC#3, port B3

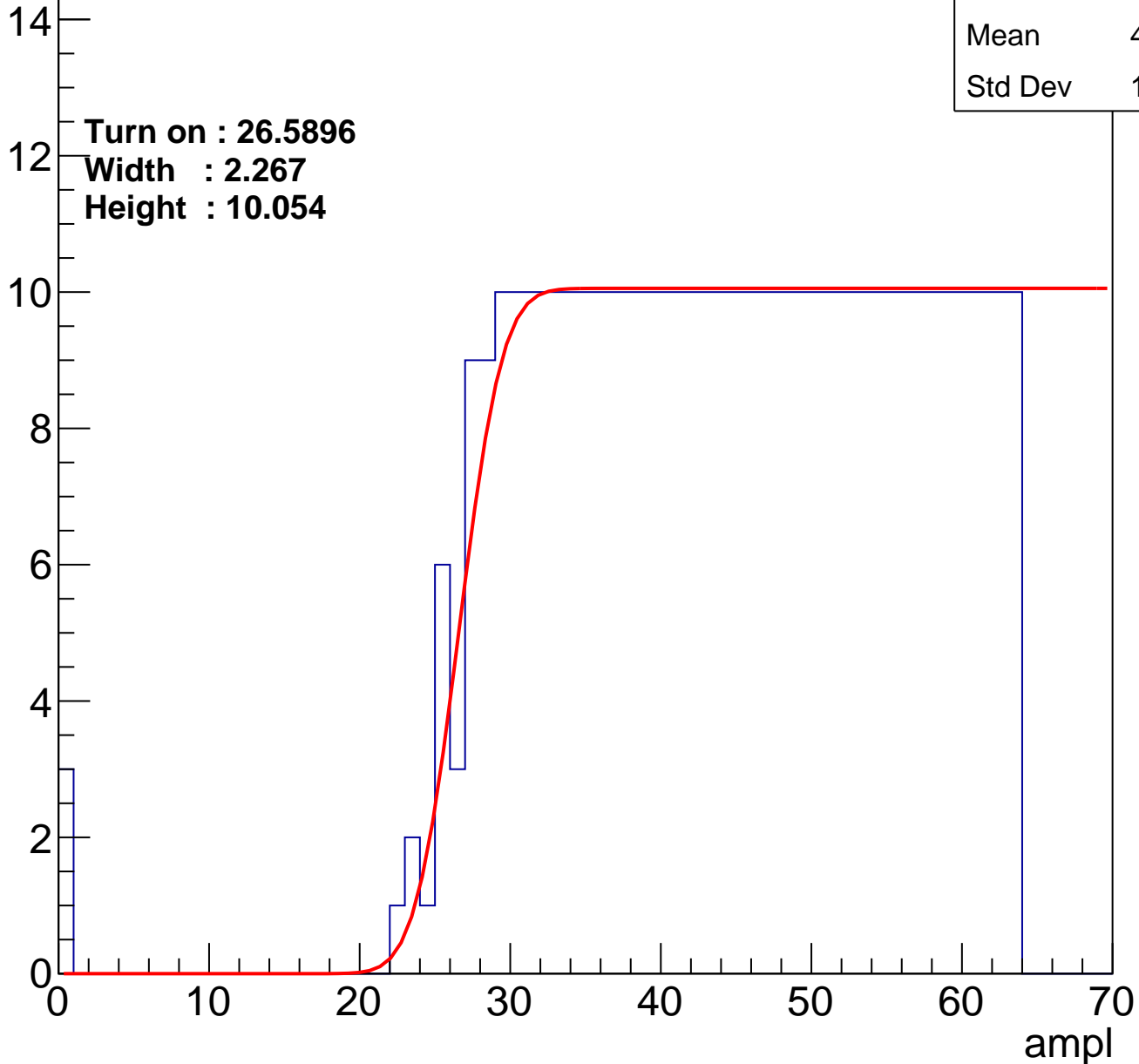
Entries	384
Mean	44.05
Std Dev	11.72

Turn on : 26.5896

Width : 2.267

Height : 10.054

Entry



# B1L000S, U7-ch58

calib\_packv5\_042523\_0143.root, FC#3, port B3

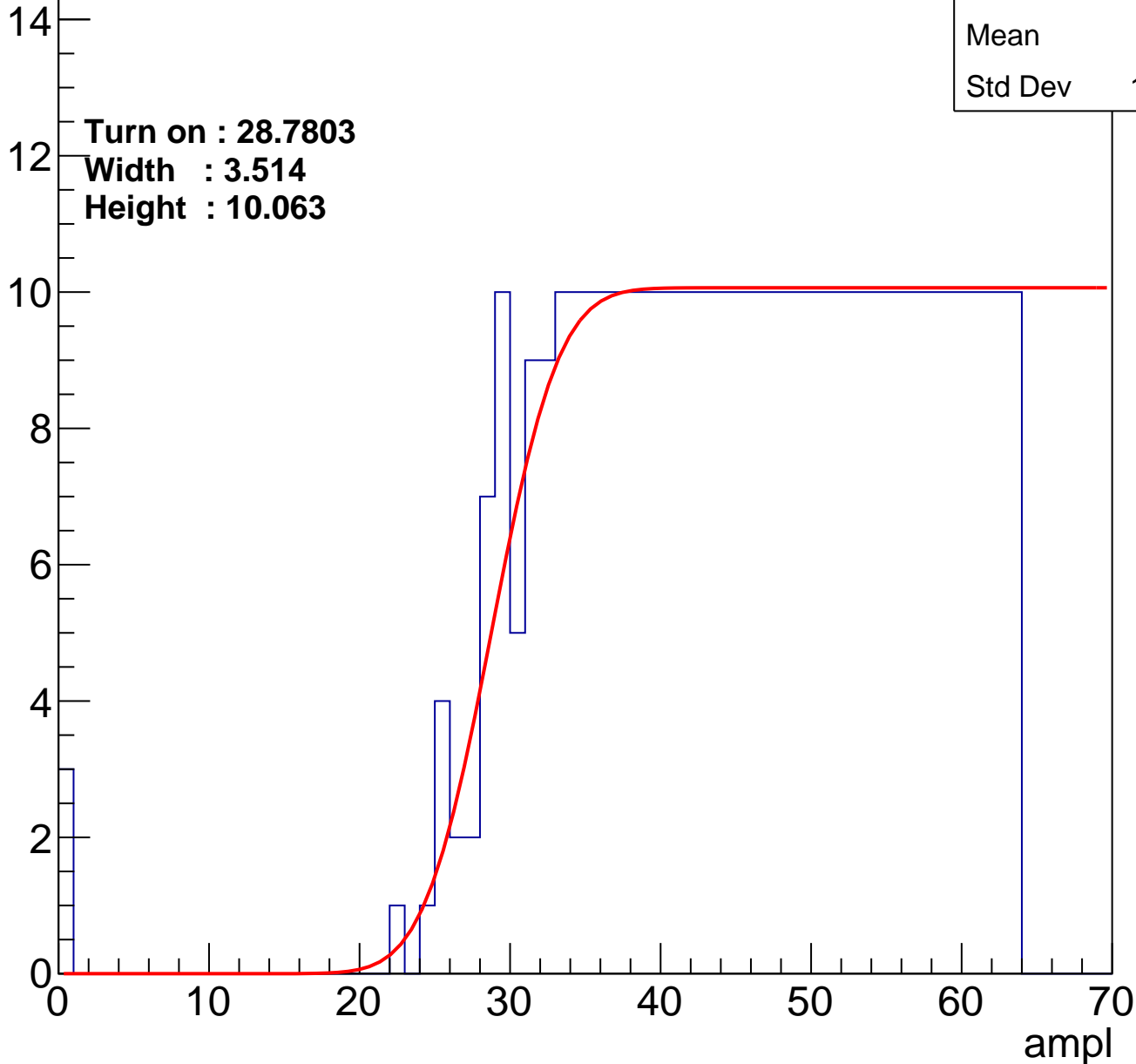
Entries	363
Mean	45
Std Dev	11.33

**Turn on : 28.7803**

**Width : 3.514**

**Height : 10.063**

Entry



# B1L000S, U7-ch59

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	394
Mean	43.67
Std Dev	11.66

Turn on : 24.7336

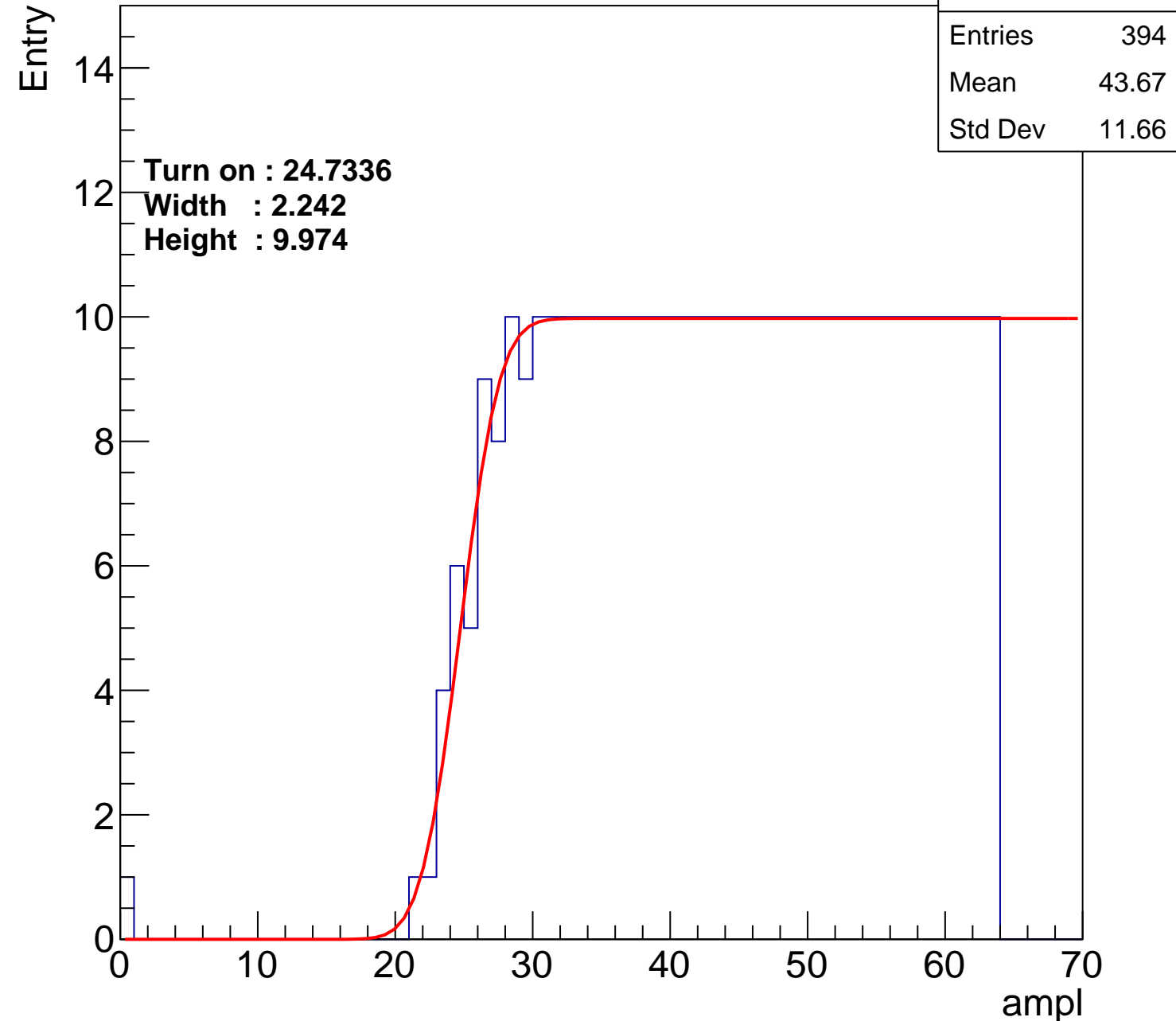
Width : 2.242

Height : 9.974

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch60

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	374
Mean	44.28
Std Dev	12.1

Turn on : 28.1974

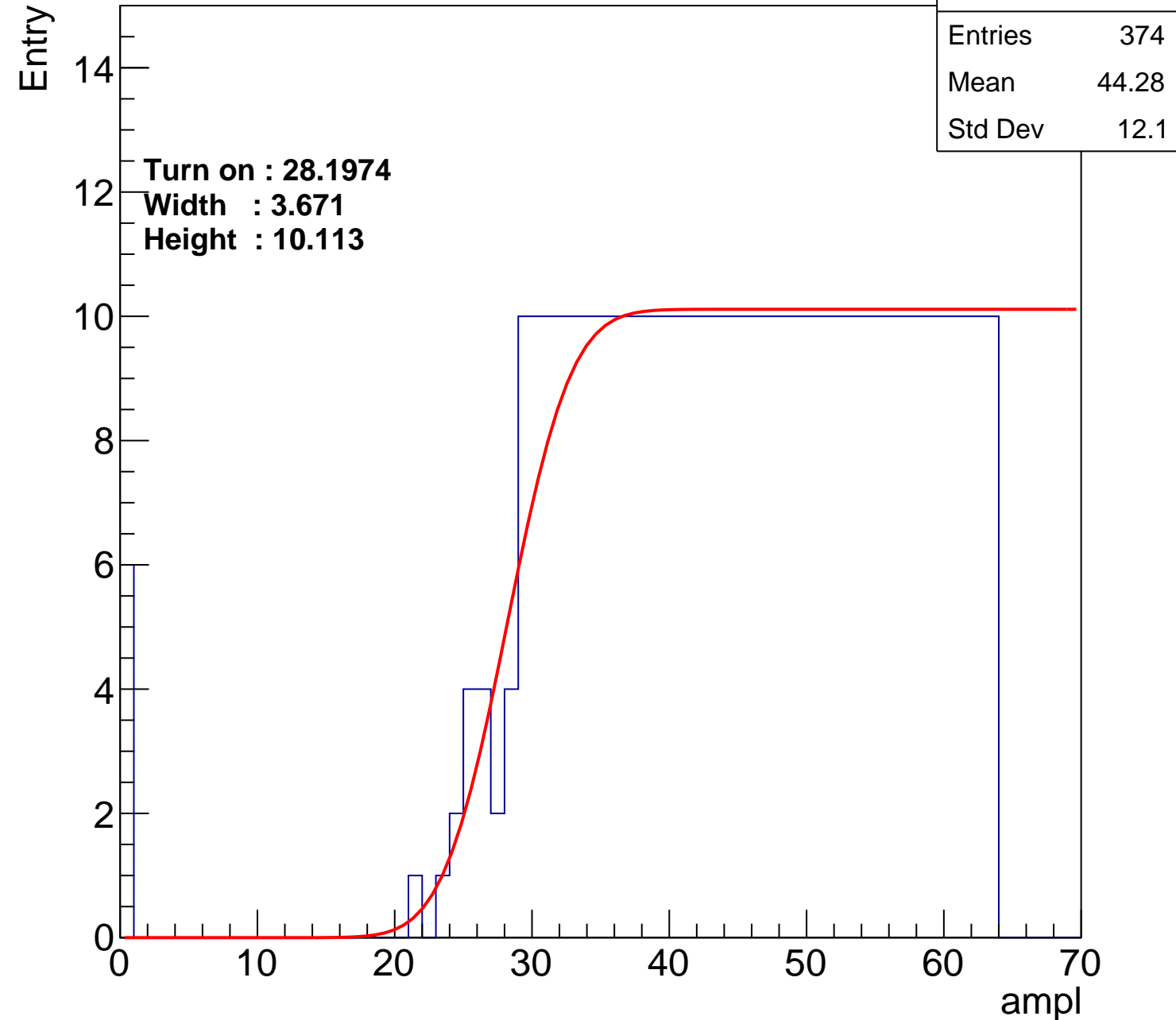
Width : 3.671

Height : 10.113

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch61

calib\_packv5\_042523\_0143.root, FC#3, port B3

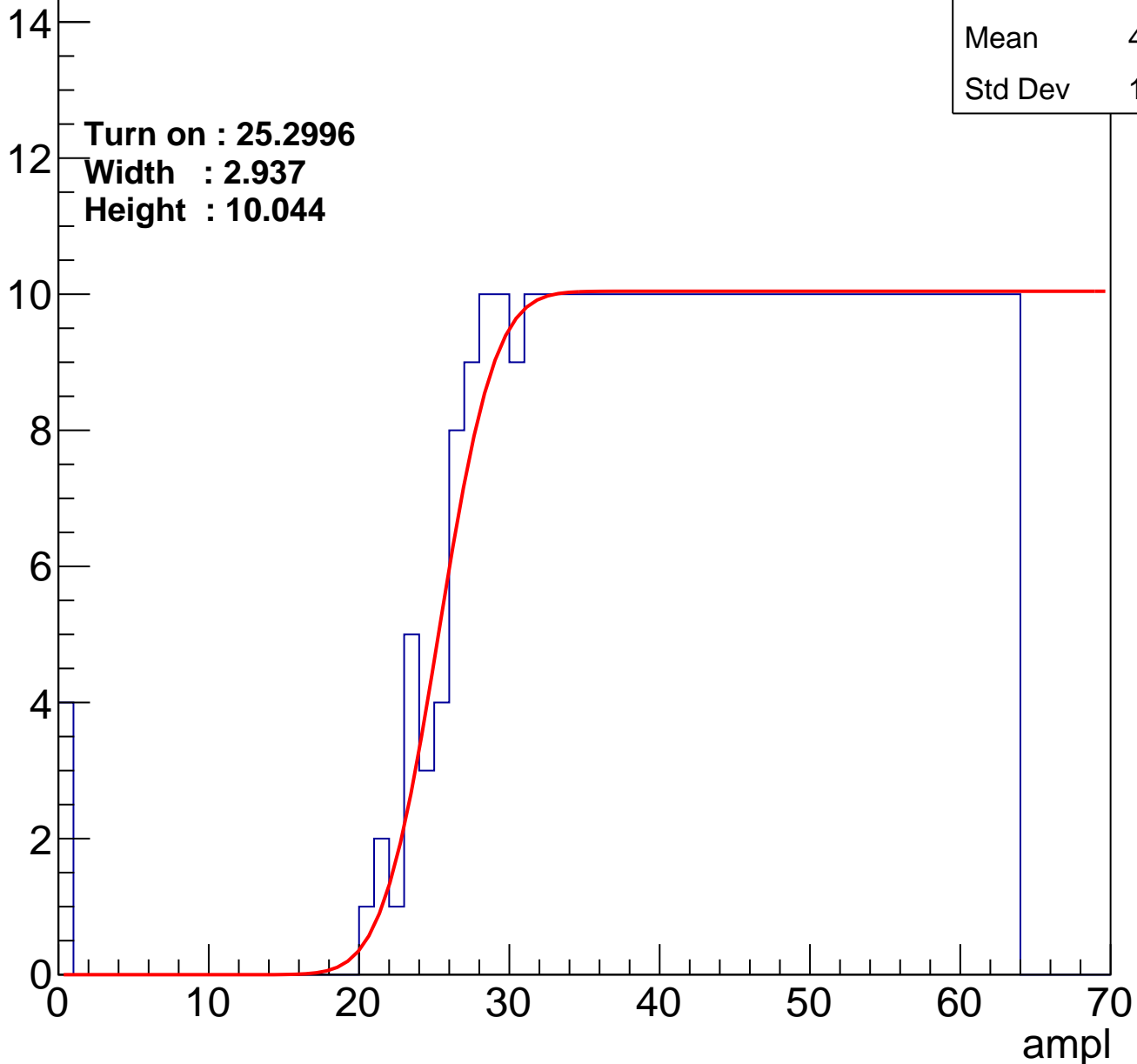
Entries	396
Mean	43.36
Std Dev	12.23

Turn on : 25.2996

Width : 2.937

Height : 10.044

Entry



# B1L000S, U7-ch62

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	394
Mean	43.55
Std Dev	11.98

Turn on : 25.0540

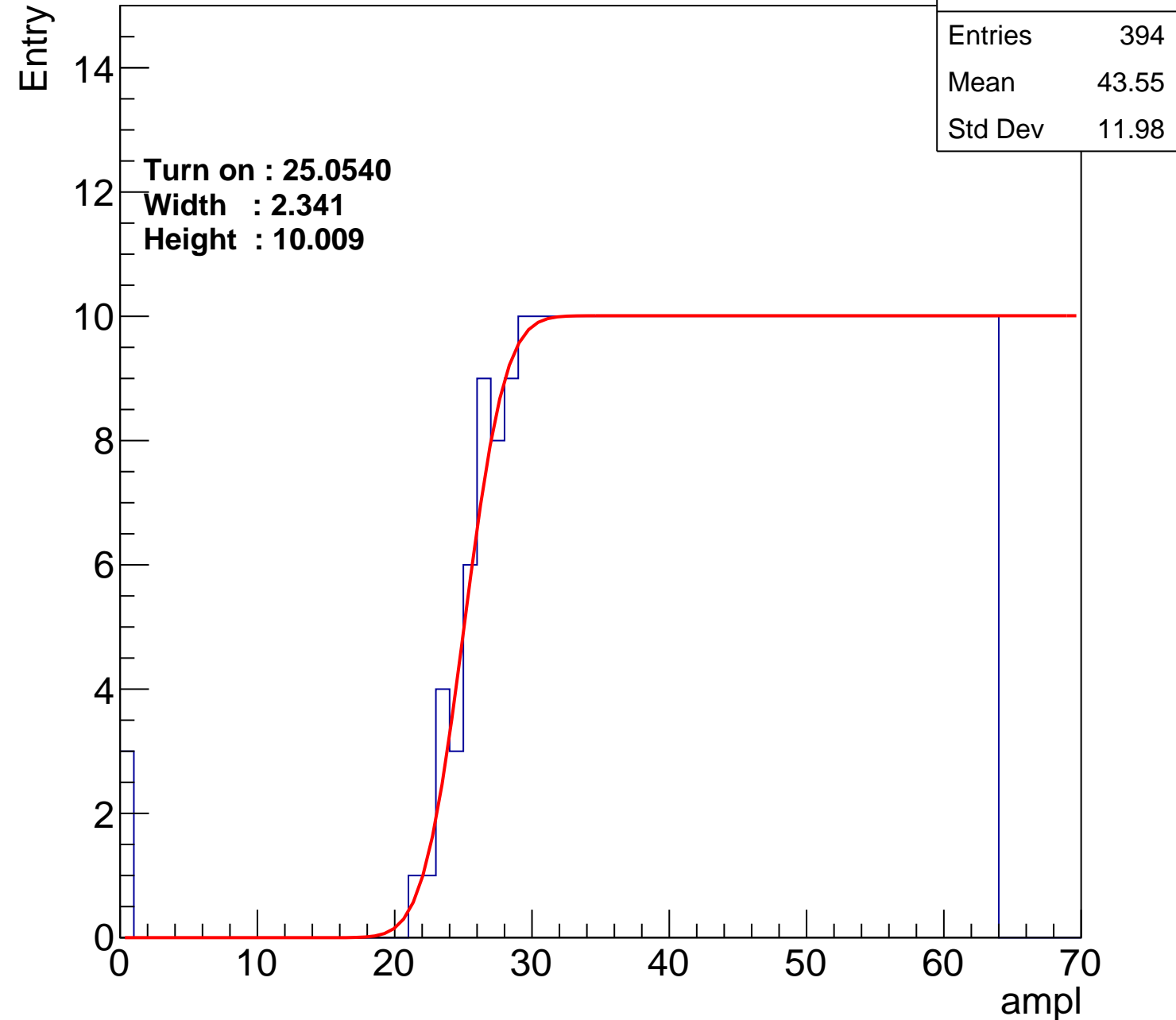
Width : 2.341

Height : 10.009

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L000S, U7-ch63

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	365
Mean	45.01
Std Dev	11.11

Turn on : 27.5347

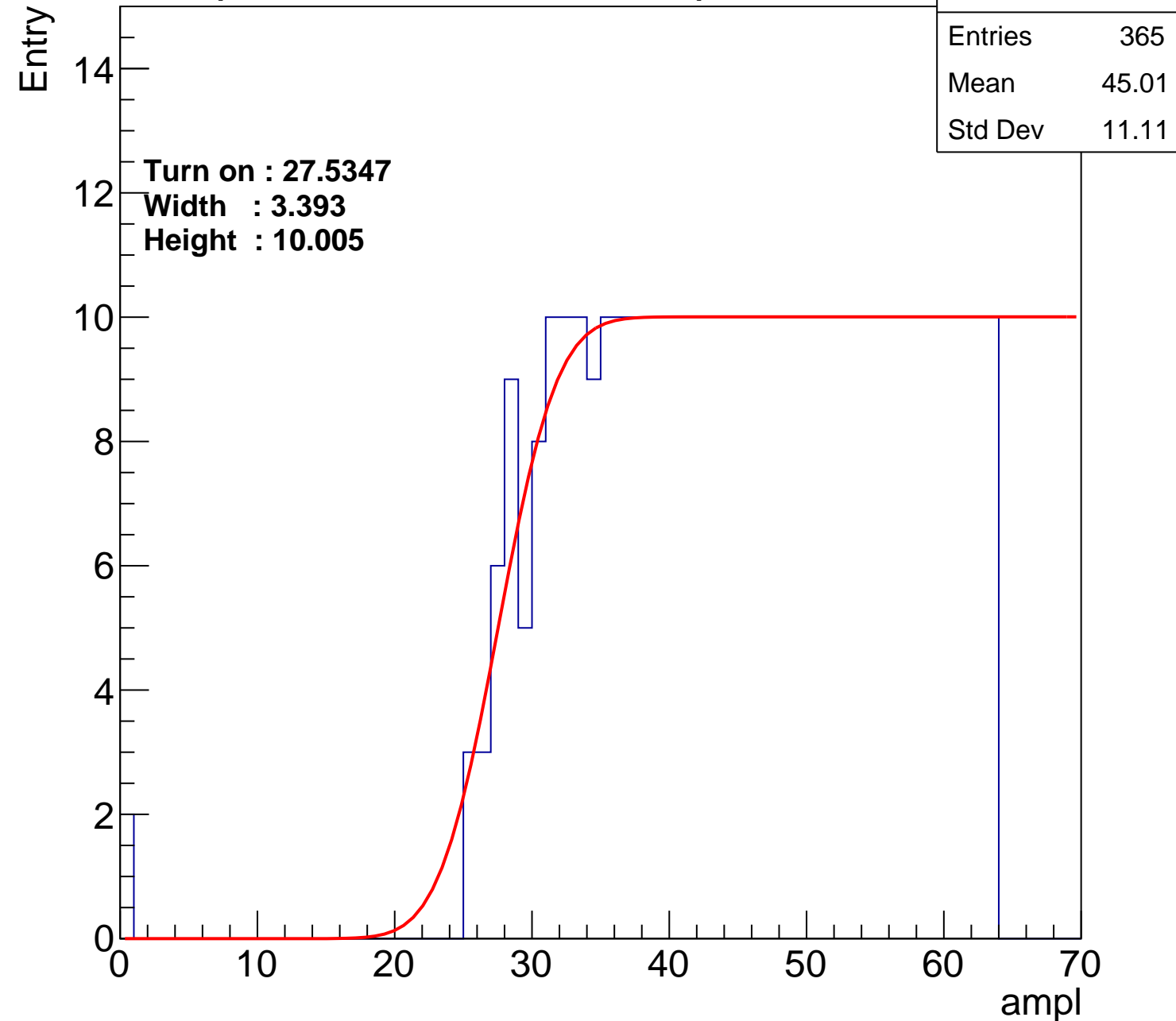
Width : 3.393

Height : 10.005

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch64

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	383
Mean	44.14
Std Dev	11.56

Turn on : 26.0485

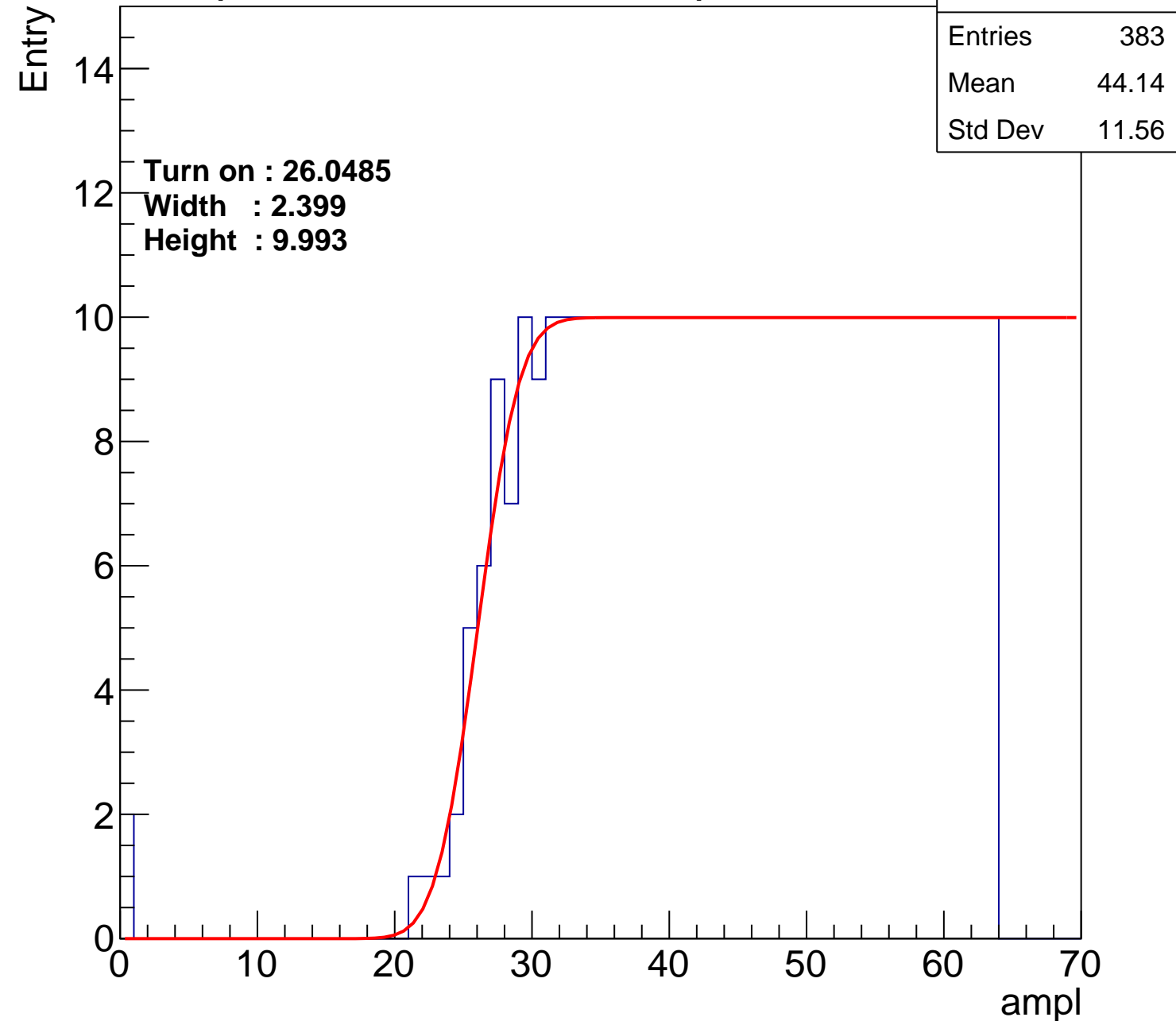
Width : 2.399

Height : 9.993

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch65

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	398
Mean	43.39
Std Dev	11.97

**Turn on : 24.3438**

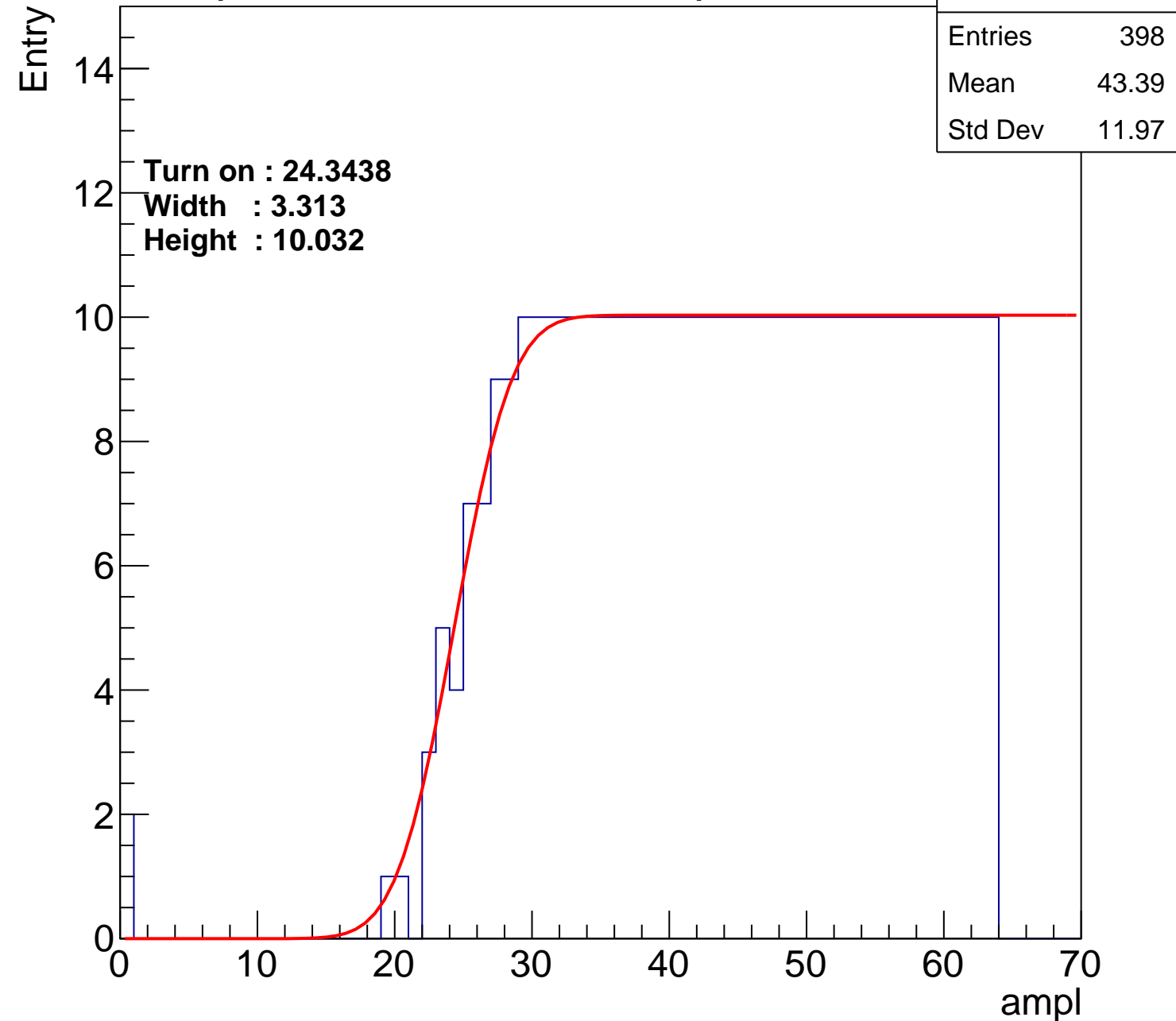
**Width : 3.313**

**Height : 10.032**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch66

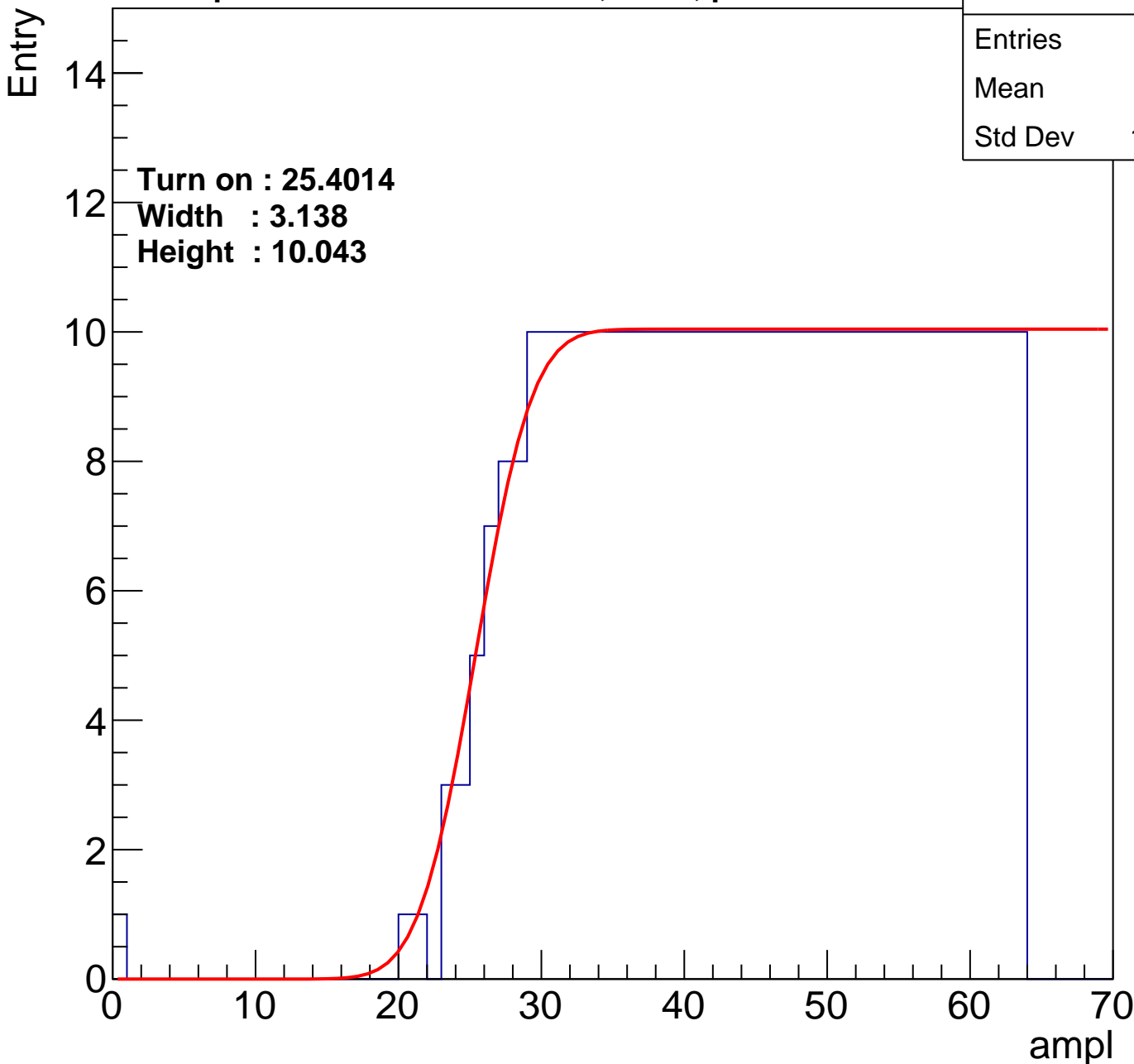
**calib\_packv5\_042523\_0143.root, FC#3, port B3**

Entries	387
Mean	44
Std Dev	11.49

**Turn on : 25.4014**

**Width : 3.138**

**Height : 10.043**



# B1L000S, U7-ch67

**calib\_packv5\_042523\_0143.root, FC#3, port B3**

Entries	377
---------	-----

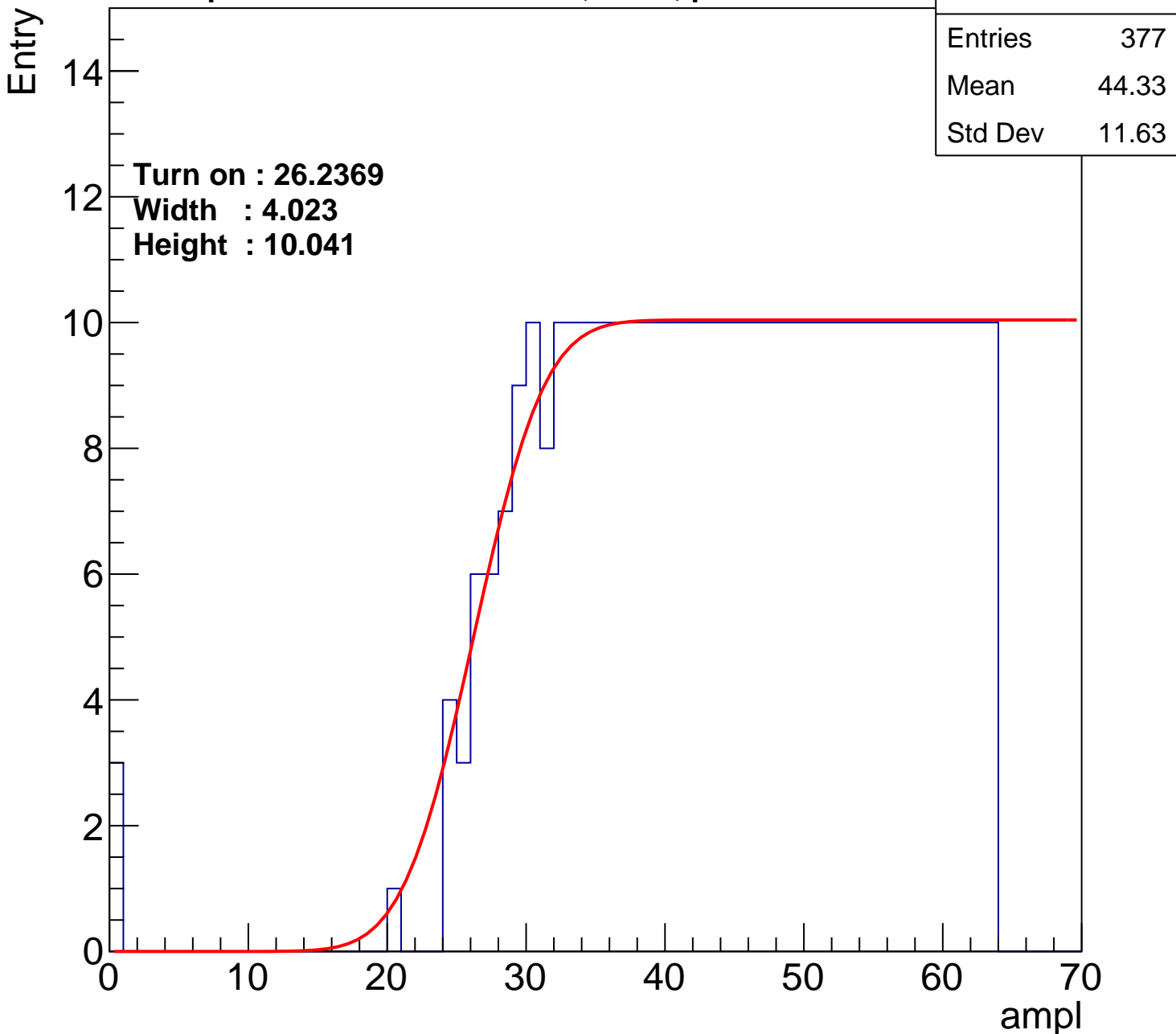
Mean	44.33
------	-------

Std Dev	11.63
---------	-------

**Turn on : 26.2369**

**Width : 4.023**

**Height : 10.041**



# B1L000S, U7-ch68

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	389
Mean	43.81
Std Dev	11.76

**Turn on : 25.2185**

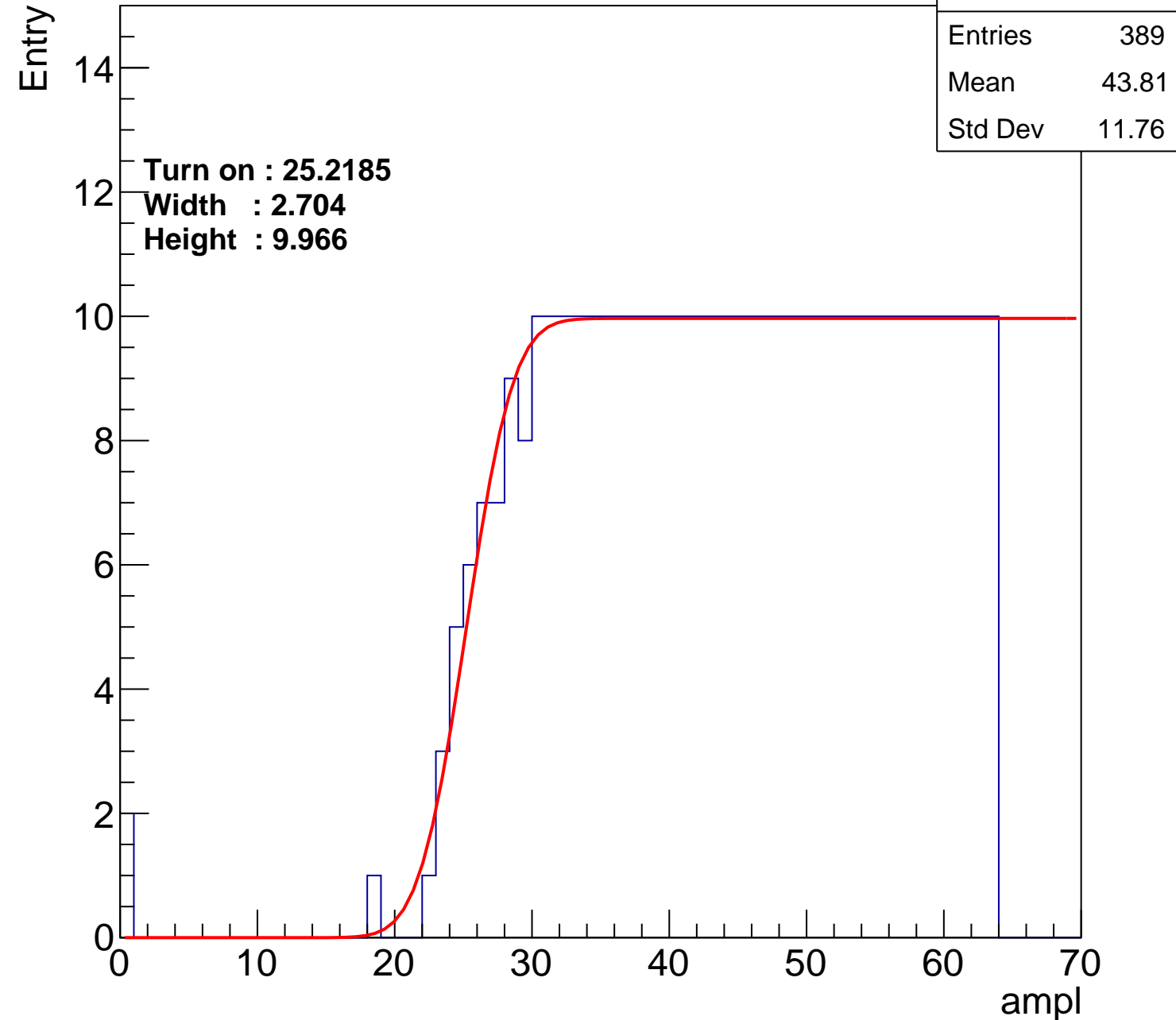
**Width : 2.704**

**Height : 9.966**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch69

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	398
Mean	43.36
Std Dev	12.06

**Turn on : 24.3115**

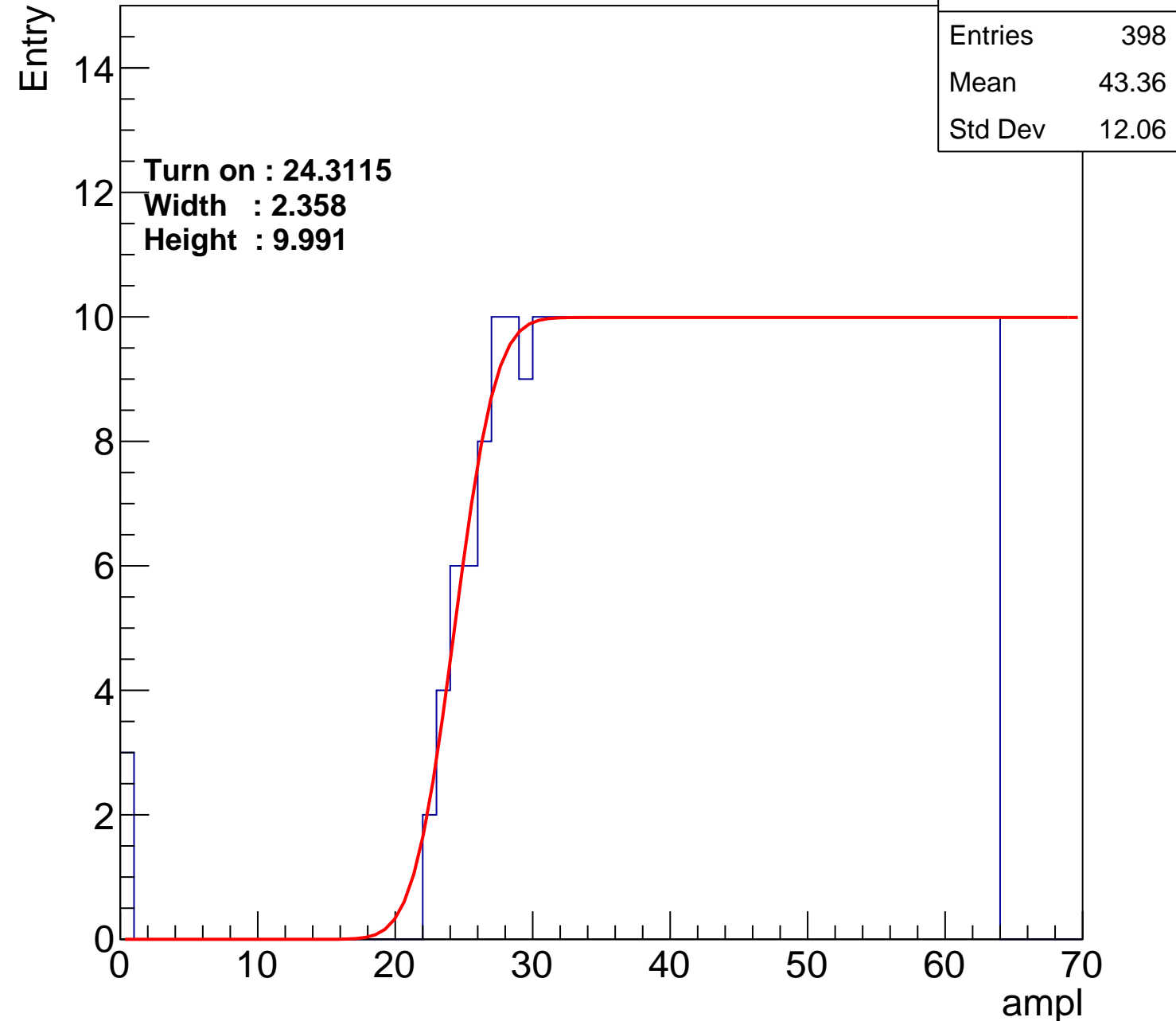
**Width : 2.358**

**Height : 9.991**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch70

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	389
Mean	43.87
Std Dev	11.67

Turn on : 25.0653

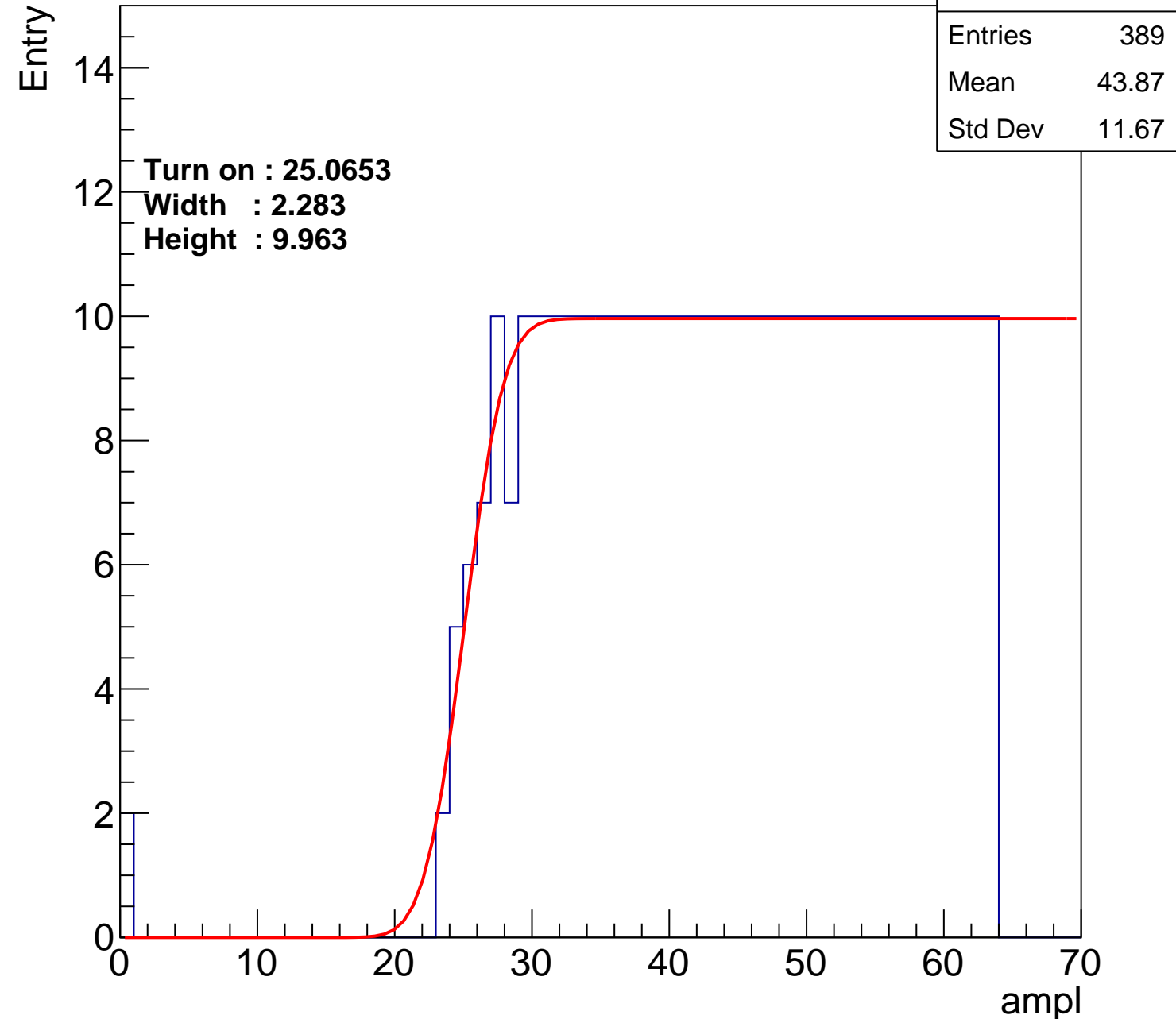
Width : 2.283

Height : 9.963

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L000S, U7-ch71

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	375
Mean	44.54
Std Dev	11.34

Turn on : 27.0034

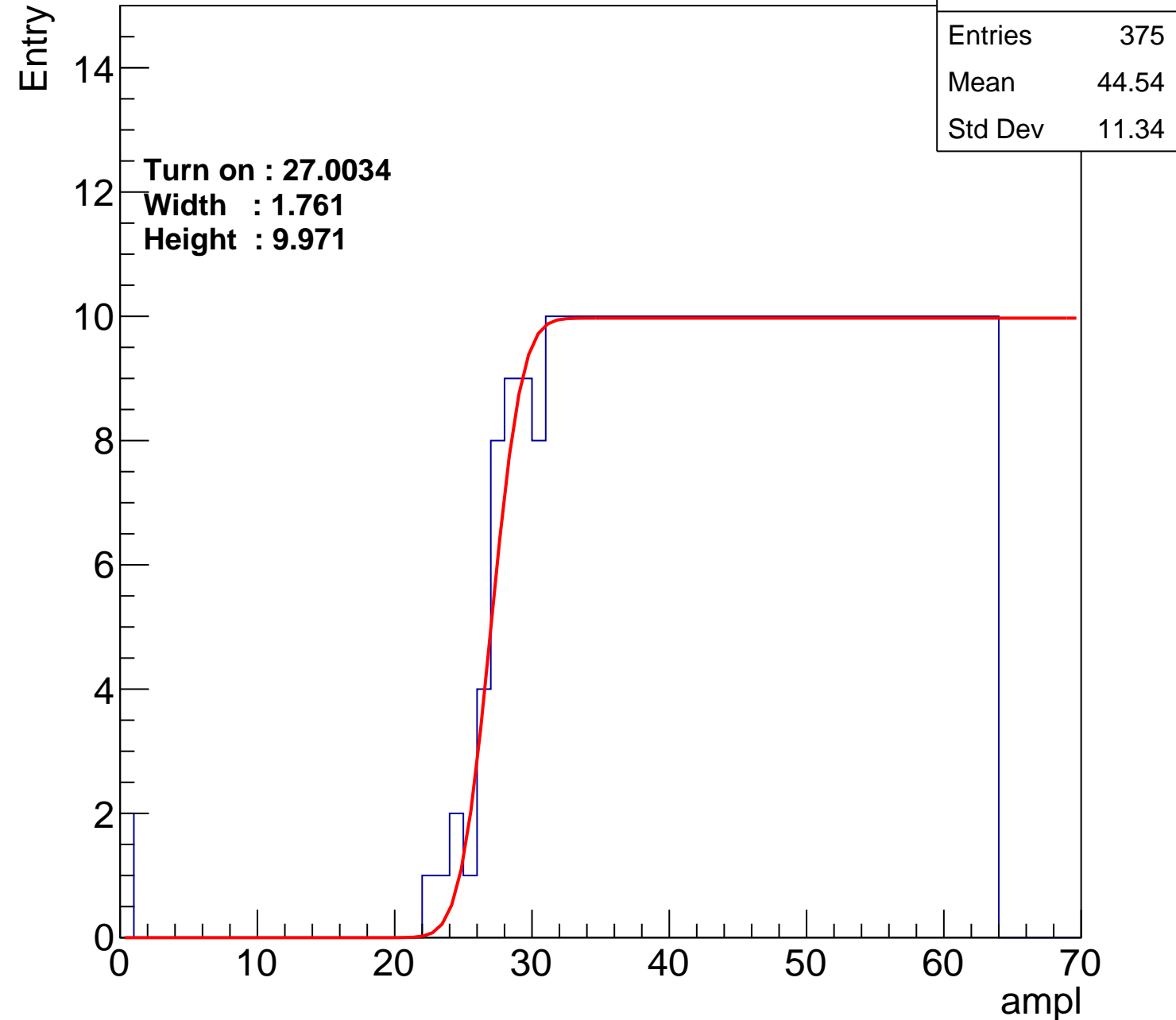
Width : 1.761

Height : 9.971

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch72

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	394
Mean	43.57
Std Dev	11.94

Turn on : 25.2596

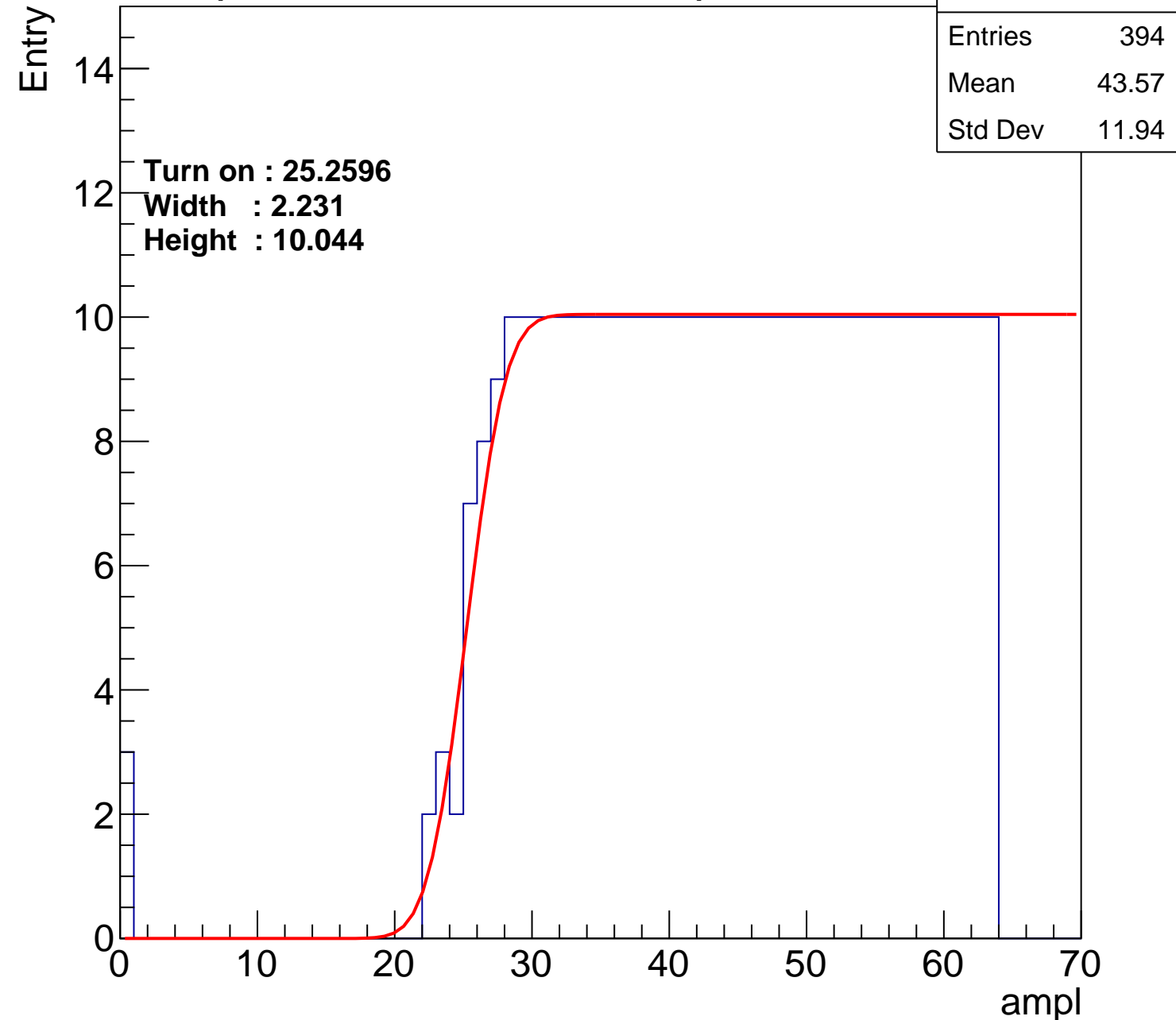
Width : 2.231

Height : 10.044

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch73

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	405
Mean	42.9
Std Dev	12.54

Turn on : 23.9564

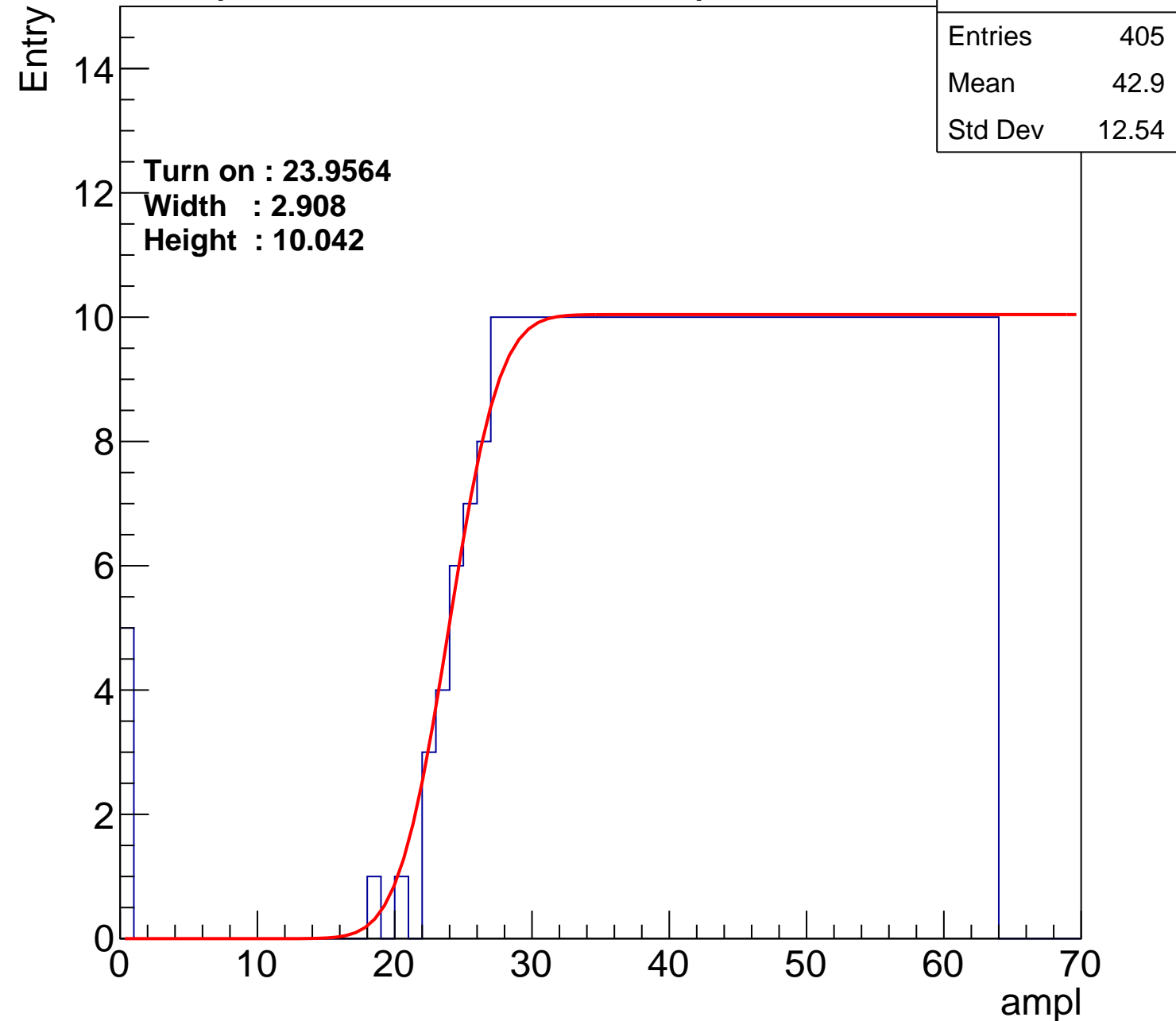
Width : 2.908

Height : 10.042

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch74

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	385
Mean	43.96
Std Dev	11.81

Turn on : 25.7234

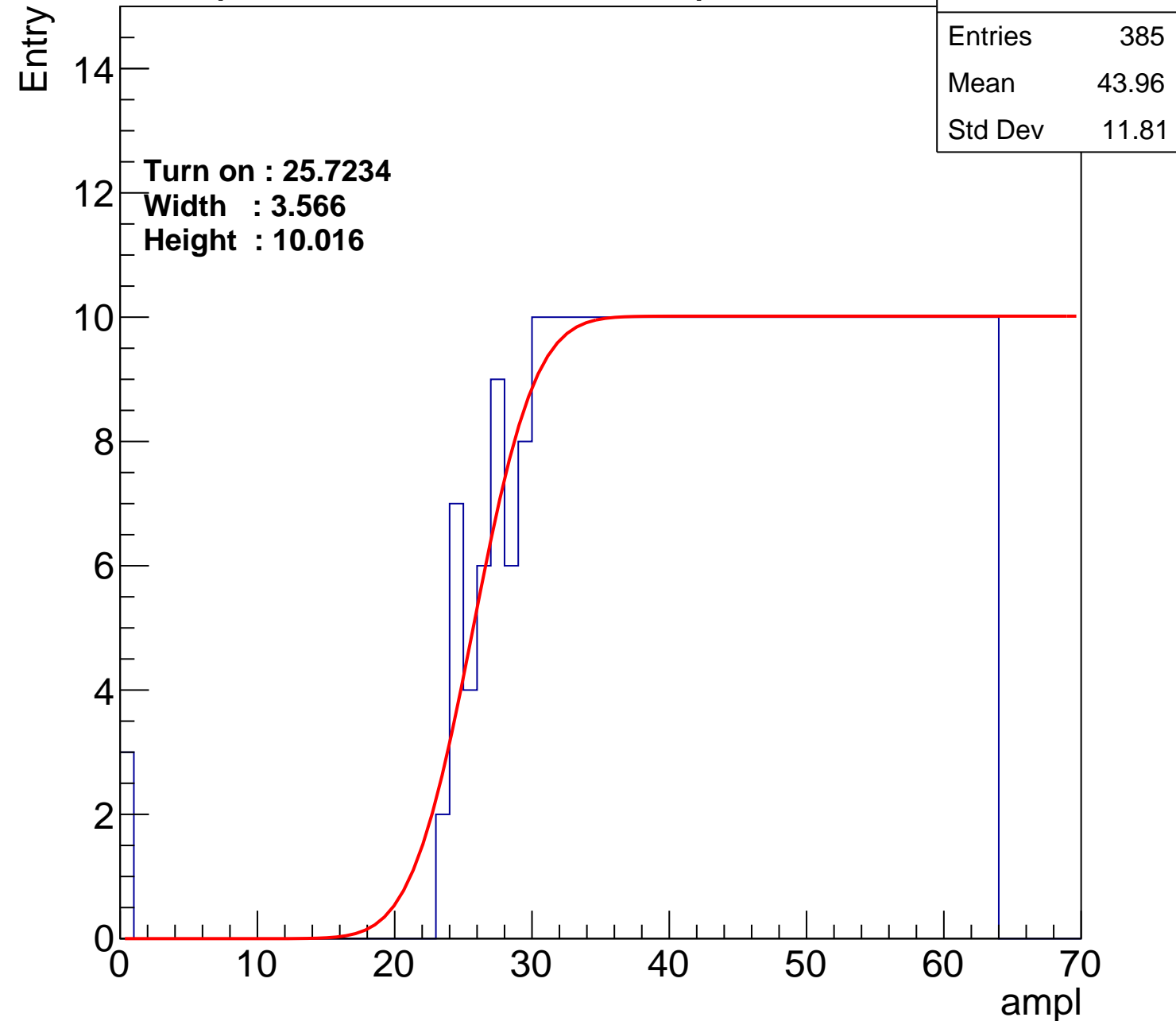
Width : 3.566

Height : 10.016

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch75

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	375
Mean	44.49
Std Dev	11.41

**Turn on : 26.9537**

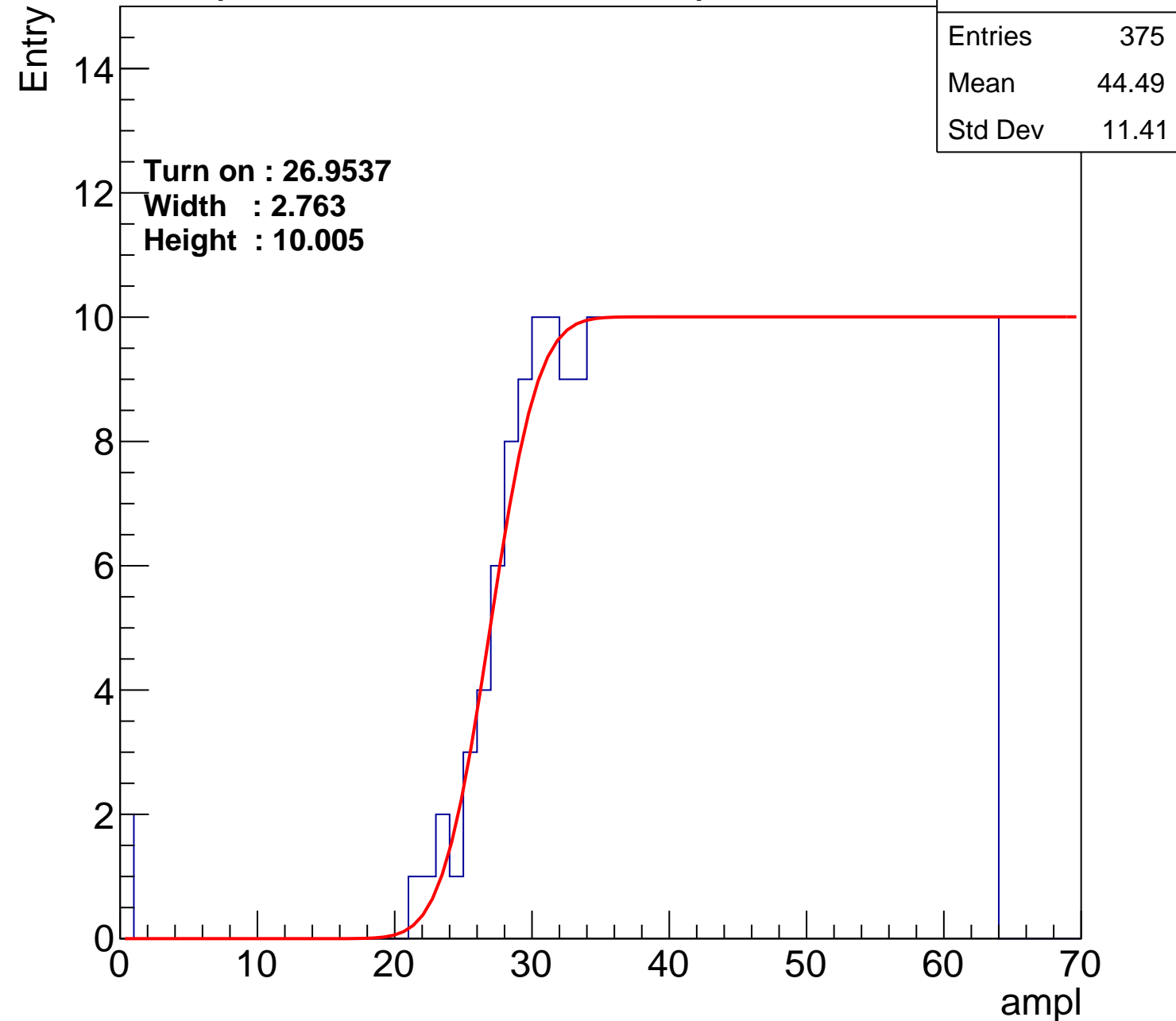
**Width : 2.763**

**Height : 10.005**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch76

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	375
Mean	44.39
Std Dev	11.73

**Turn on : 27.3797**

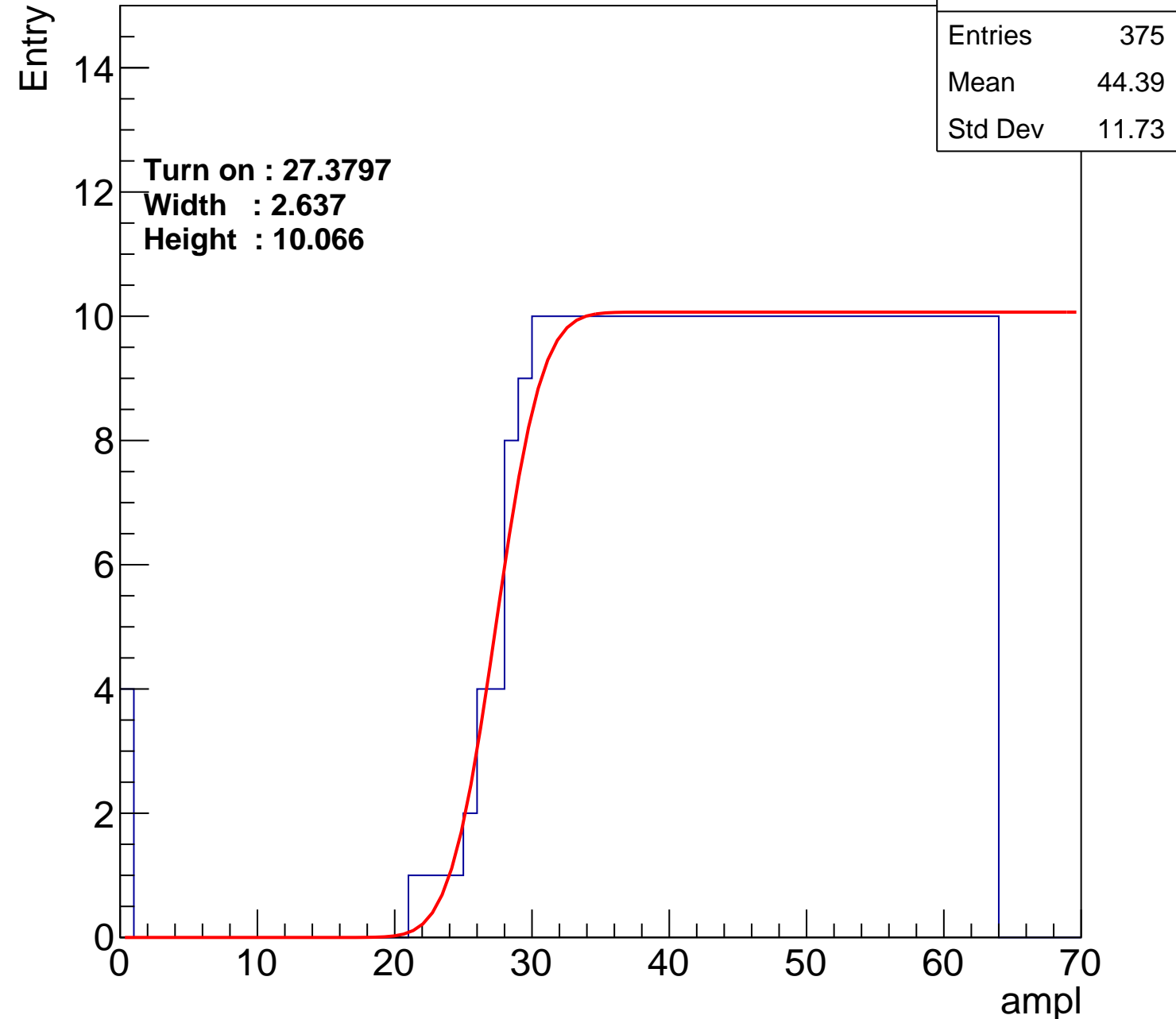
**Width : 2.637**

**Height : 10.066**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch77

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	380
Mean	44.28
Std Dev	11.49

**Turn on : 26.7657**

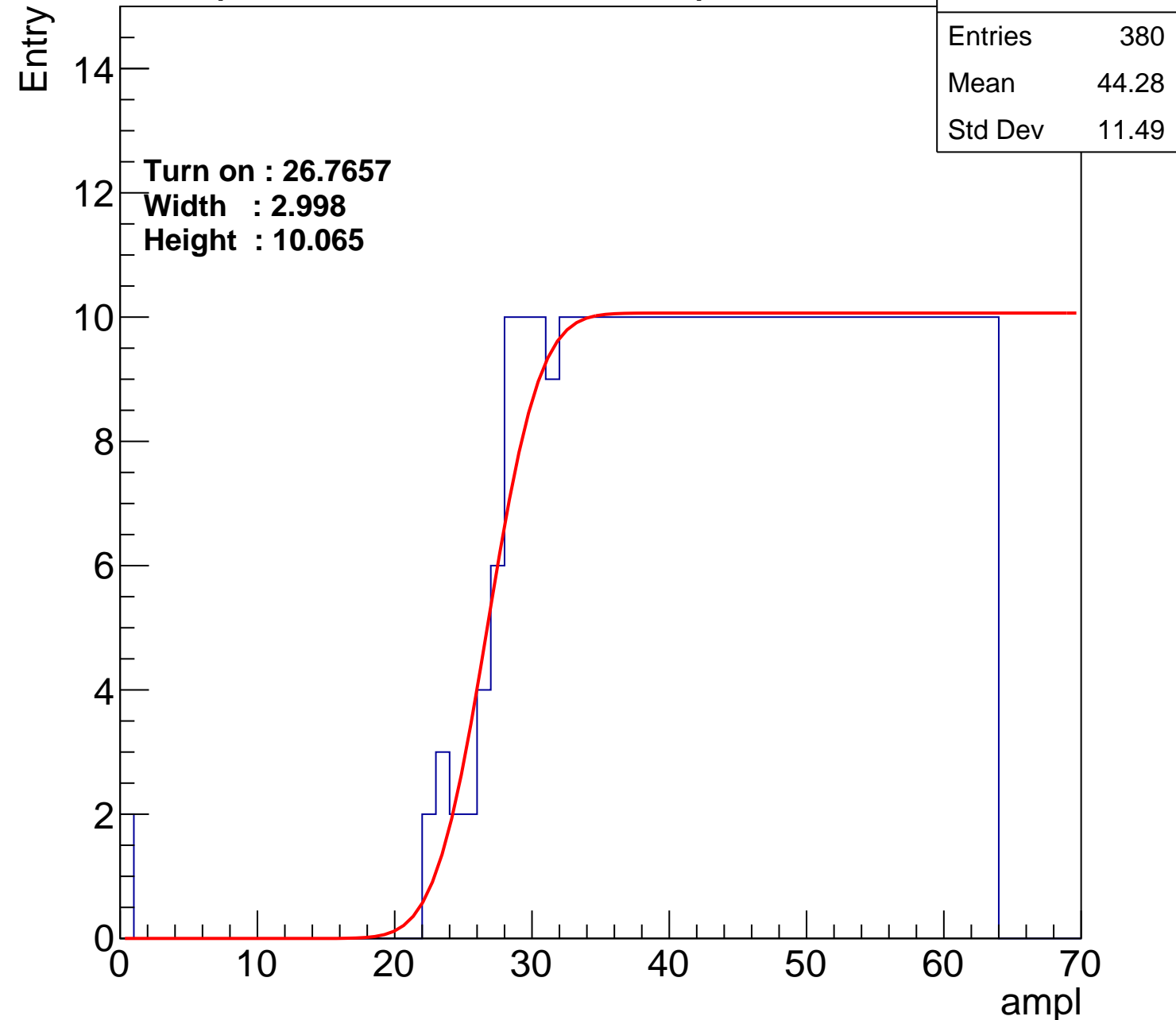
**Width : 2.998**

**Height : 10.065**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch78

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	394
Mean	43.54
Std Dev	11.99

Turn on : 25.3406

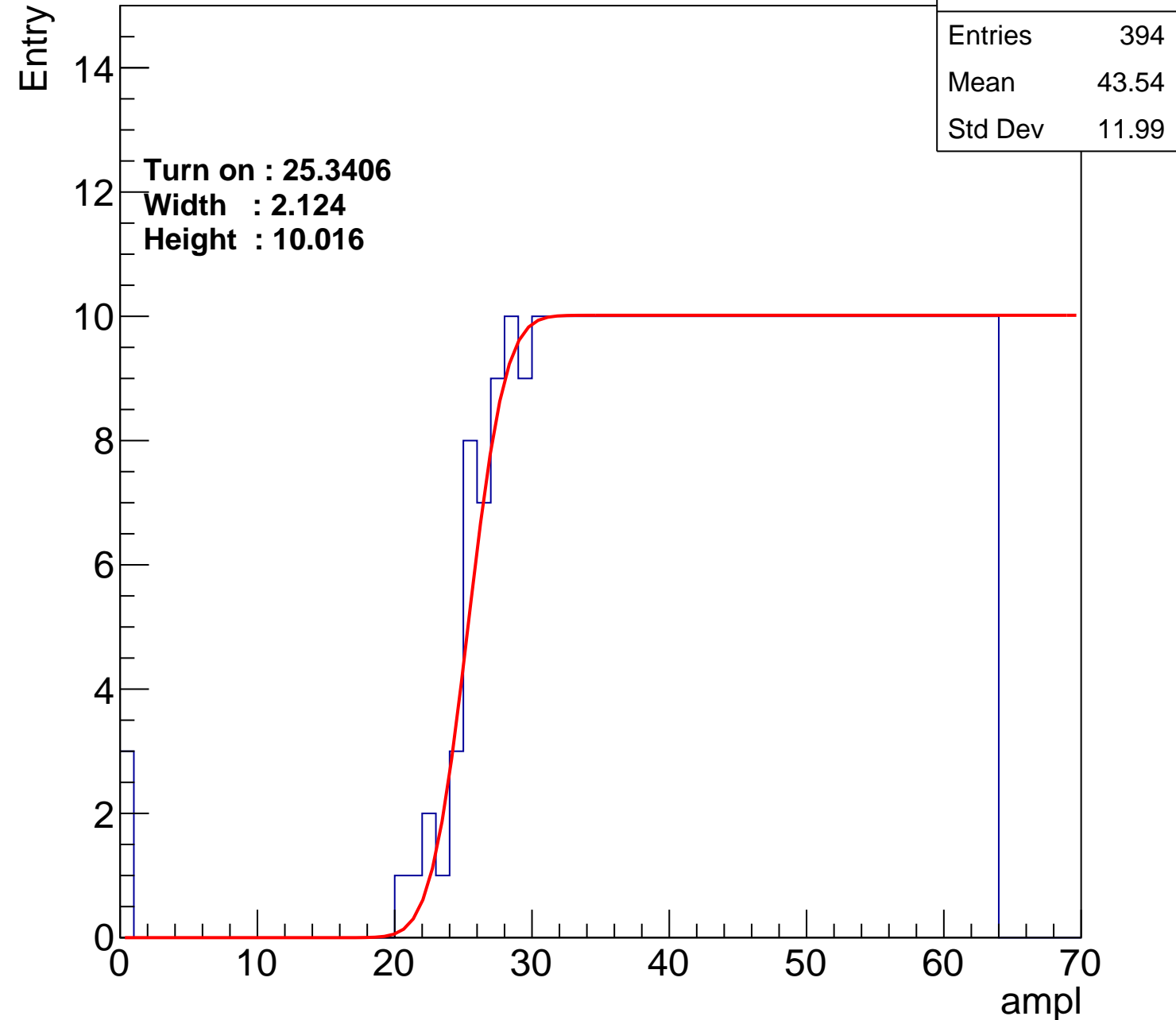
Width : 2.124

Height : 10.016

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L000S, U7-ch79

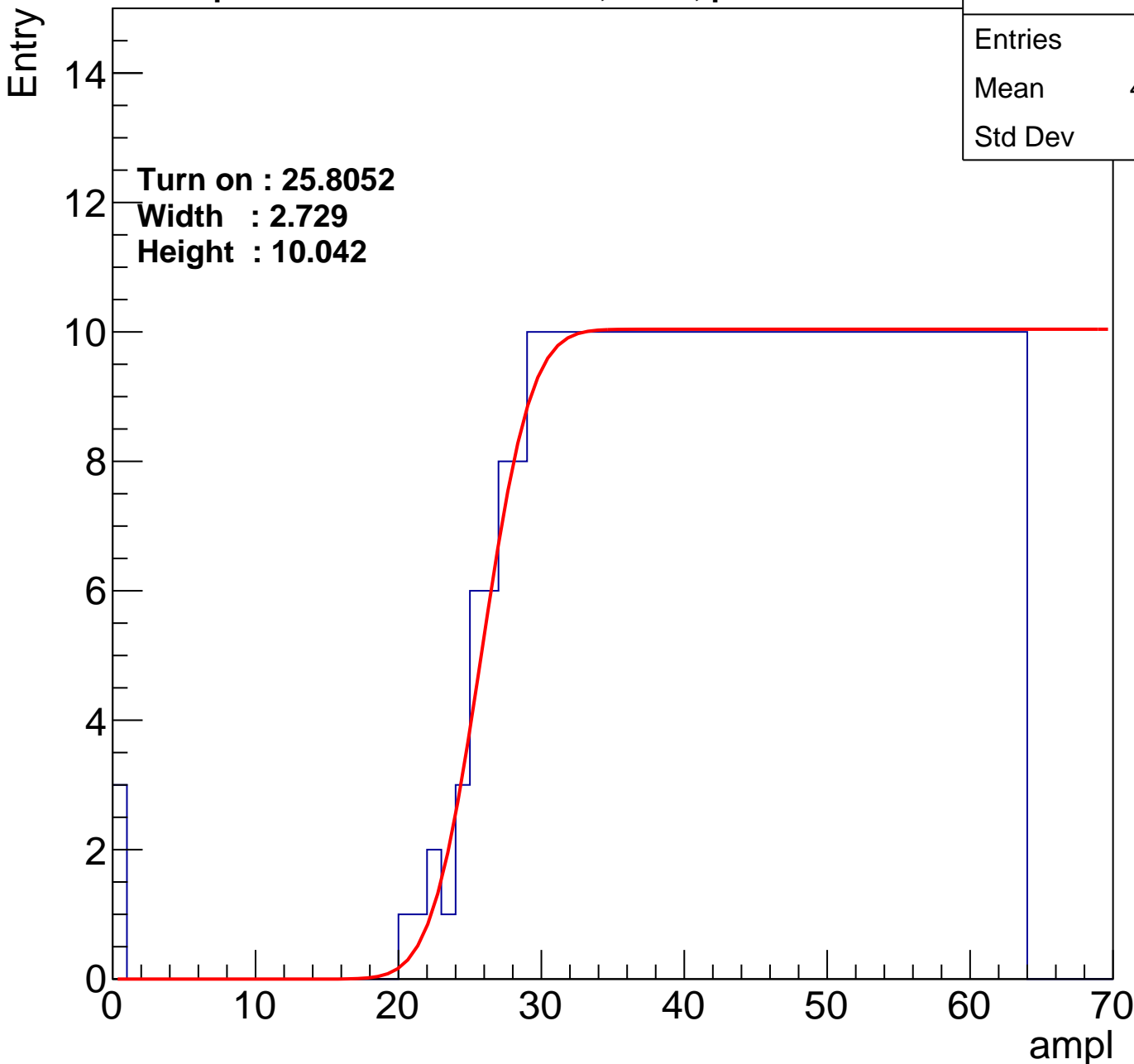
**calib\_packv5\_042523\_0143.root, FC#3, port B3**

Entries	389
Mean	43.77
Std Dev	11.9

**Turn on : 25.8052**

**Width : 2.729**

**Height : 10.042**



# B1L000S, U7-ch80

calib\_packv5\_042523\_0143.root, FC#3, port B3

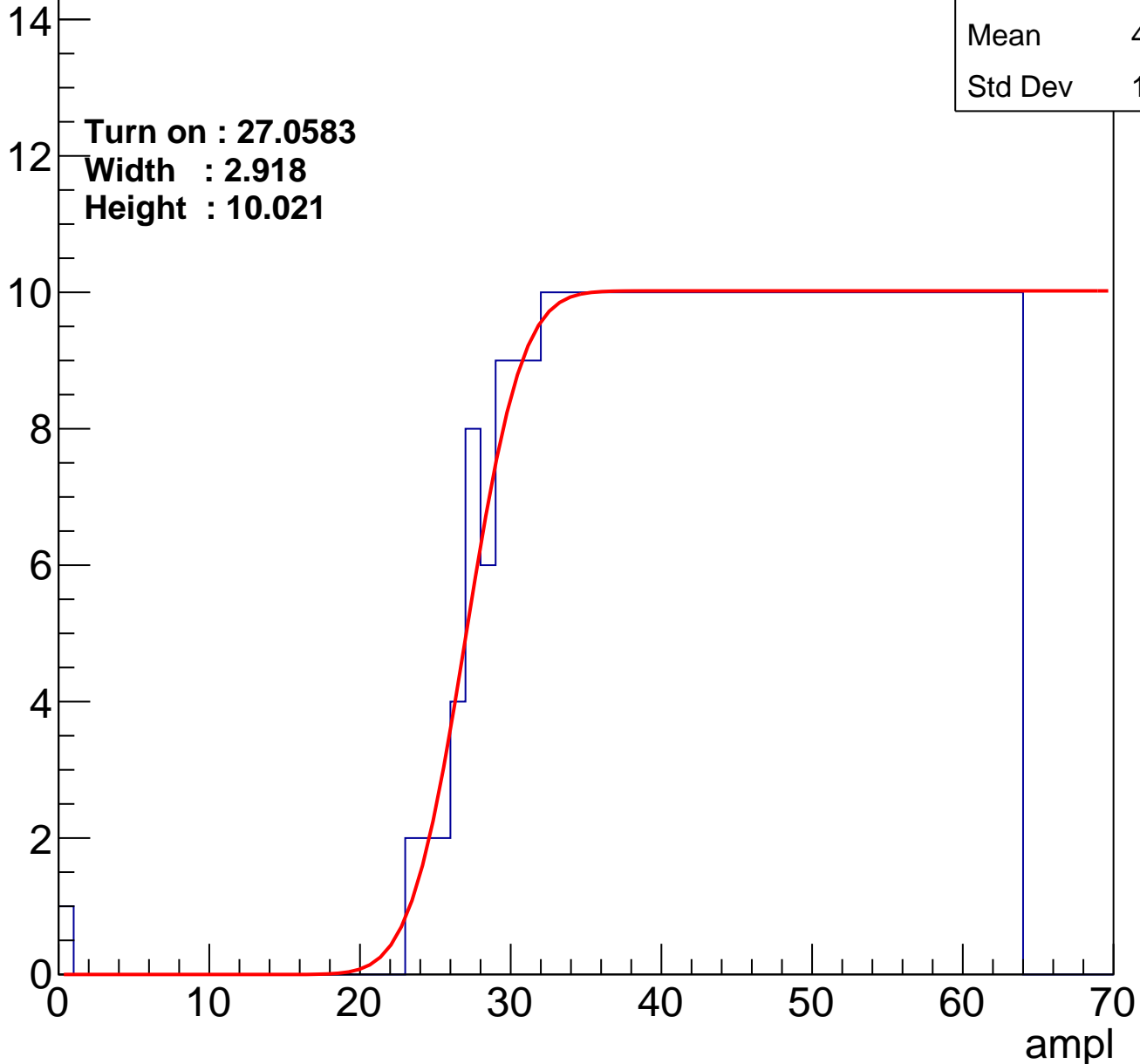
Entries	372
Mean	44.74
Std Dev	11.09

Turn on : 27.0583

Width : 2.918

Height : 10.021

Entry



# B1L000S, U7-ch81

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	370
Mean	44.7
Std Dev	11.43

**Turn on : 27.4965**

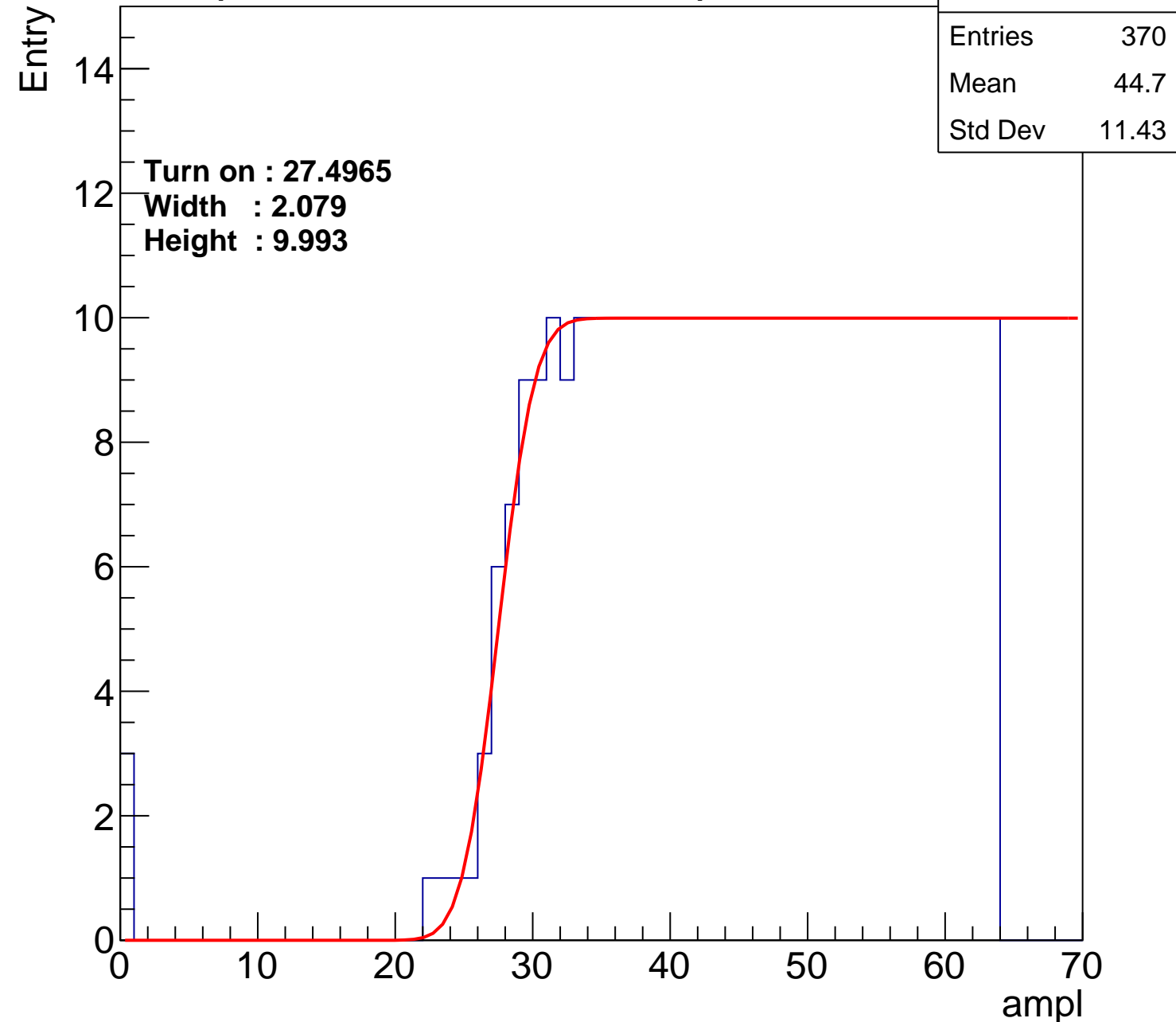
**Width : 2.079**

**Height : 9.993**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch82

calib\_packv5\_042523\_0143.root, FC#3, port B3

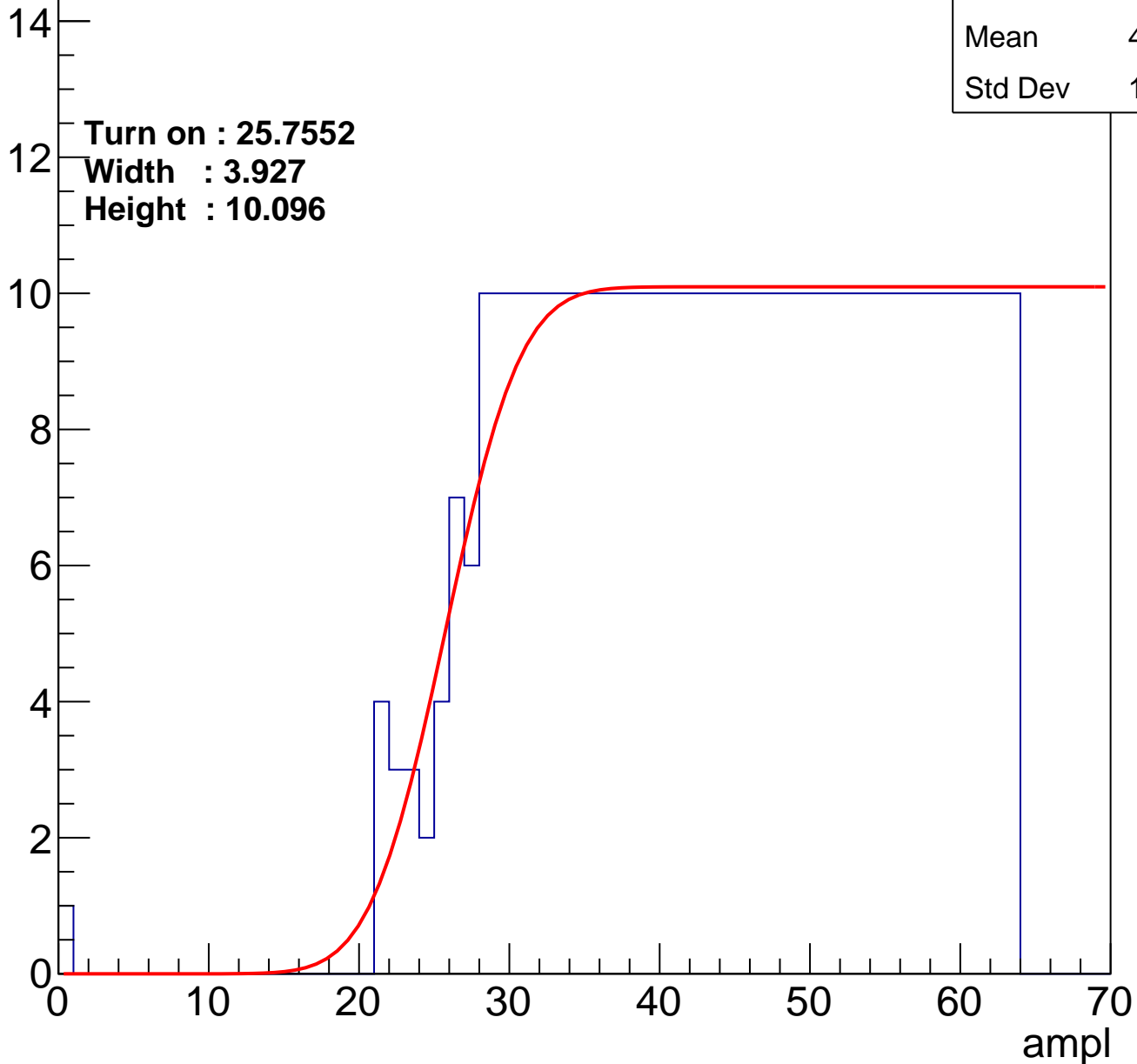
Entries	390
Mean	43.82
Std Dev	11.63

Turn on : 25.7552

Width : 3.927

Height : 10.096

Entry



# B1L000S, U7-ch83

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	379
Mean	44.3
Std Dev	11.52

Turn on : 26.2637

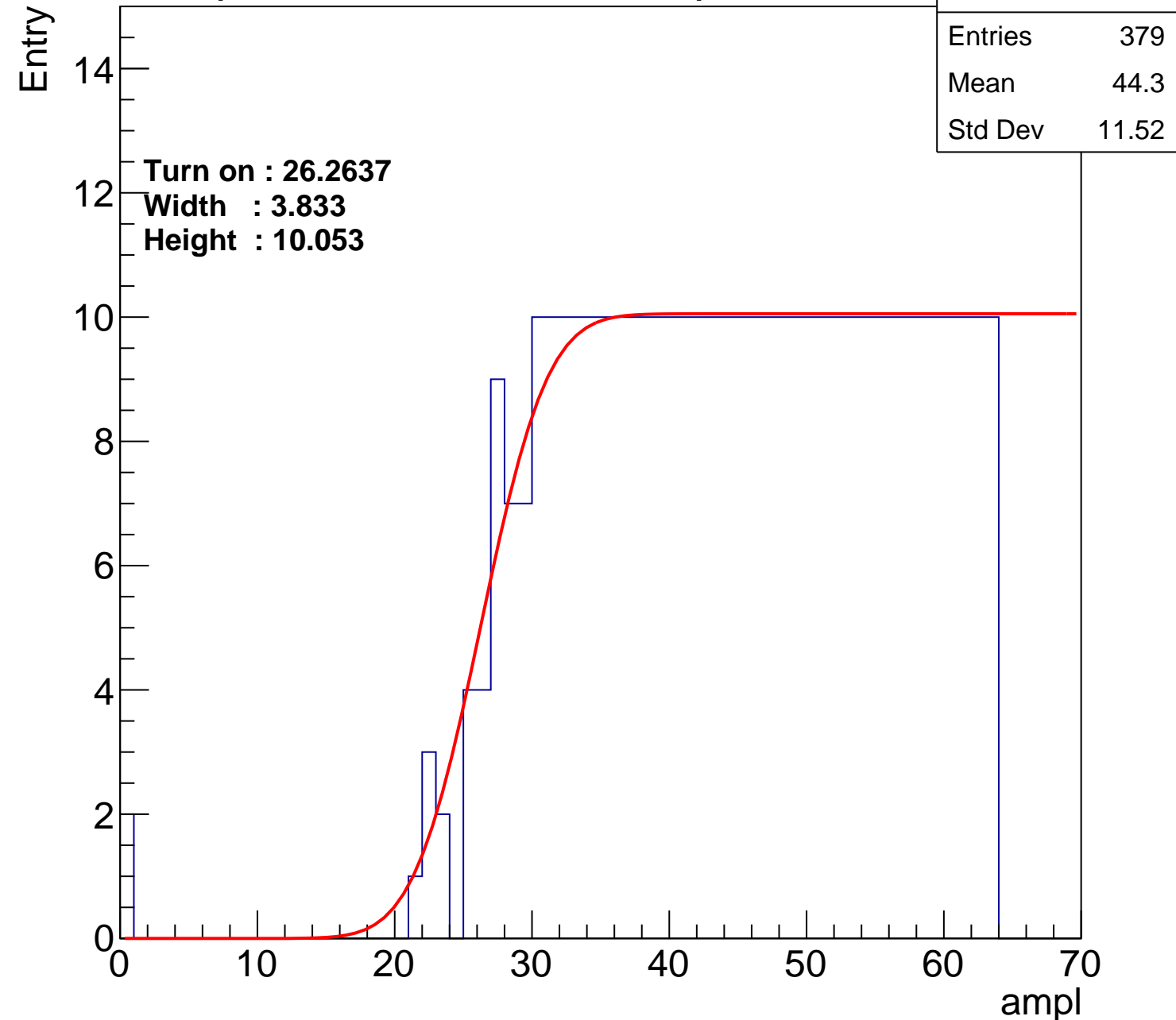
Width : 3.833

Height : 10.053

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch84

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	364
Mean	44.96
Std Dev	11.44

Turn on : 27.7966

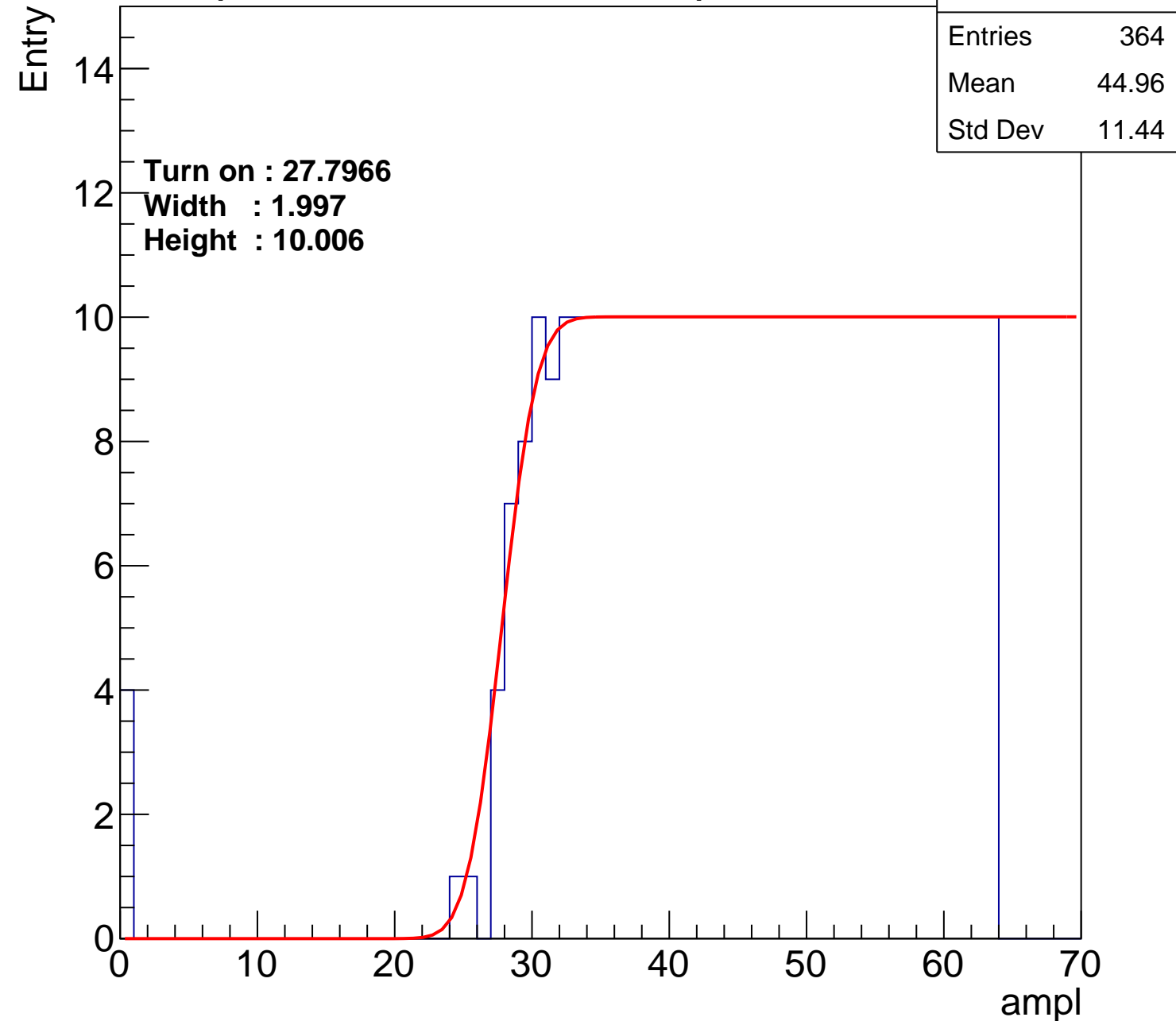
Width : 1.997

Height : 10.006

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch85

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	396
Mean	43.34
Std Dev	12.27

Turn on : 25.4791

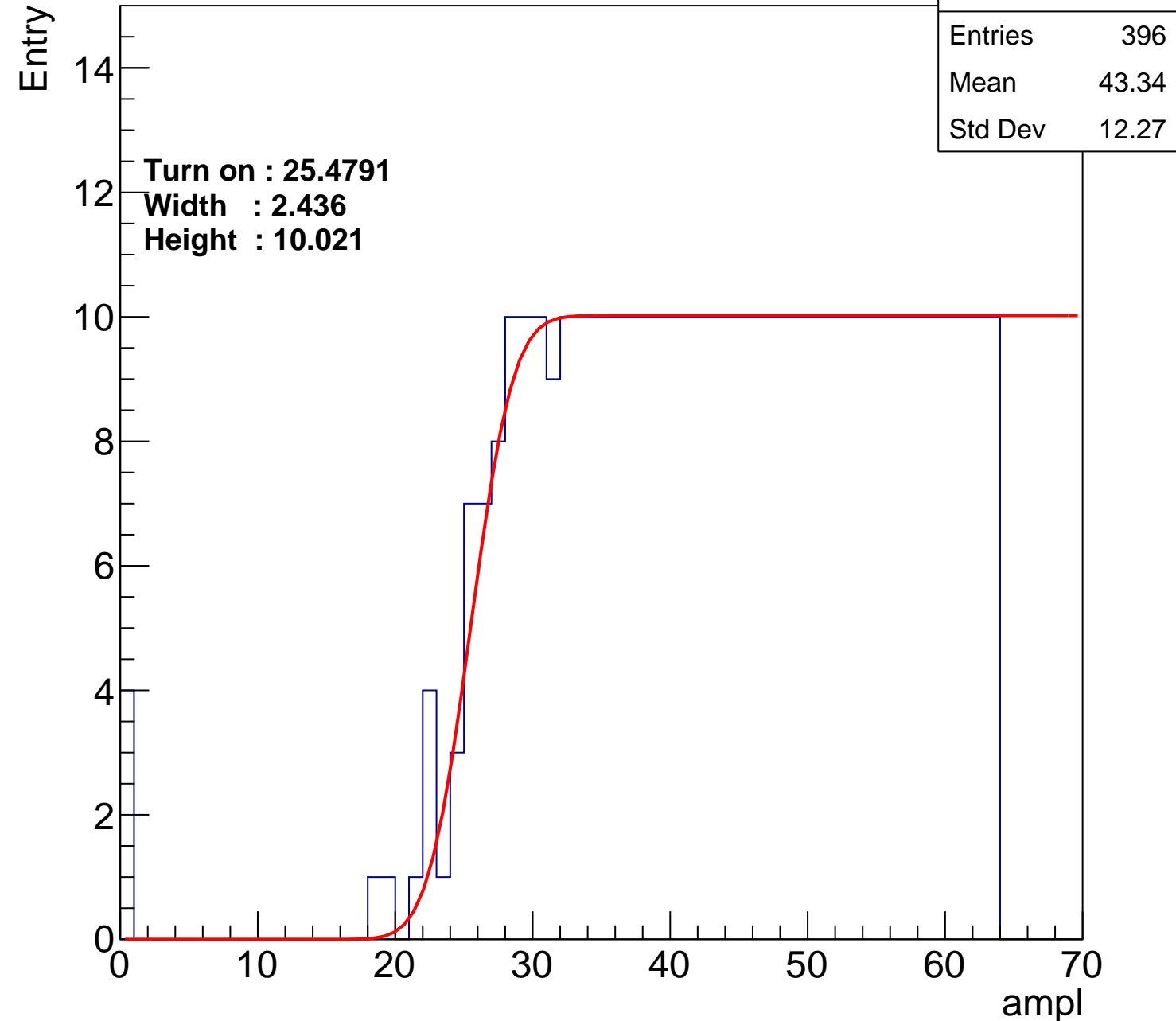
Width : 2.436

Height : 10.021

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch86

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	392
Mean	43.49
Std Dev	12.24

Turn on : 26.0218

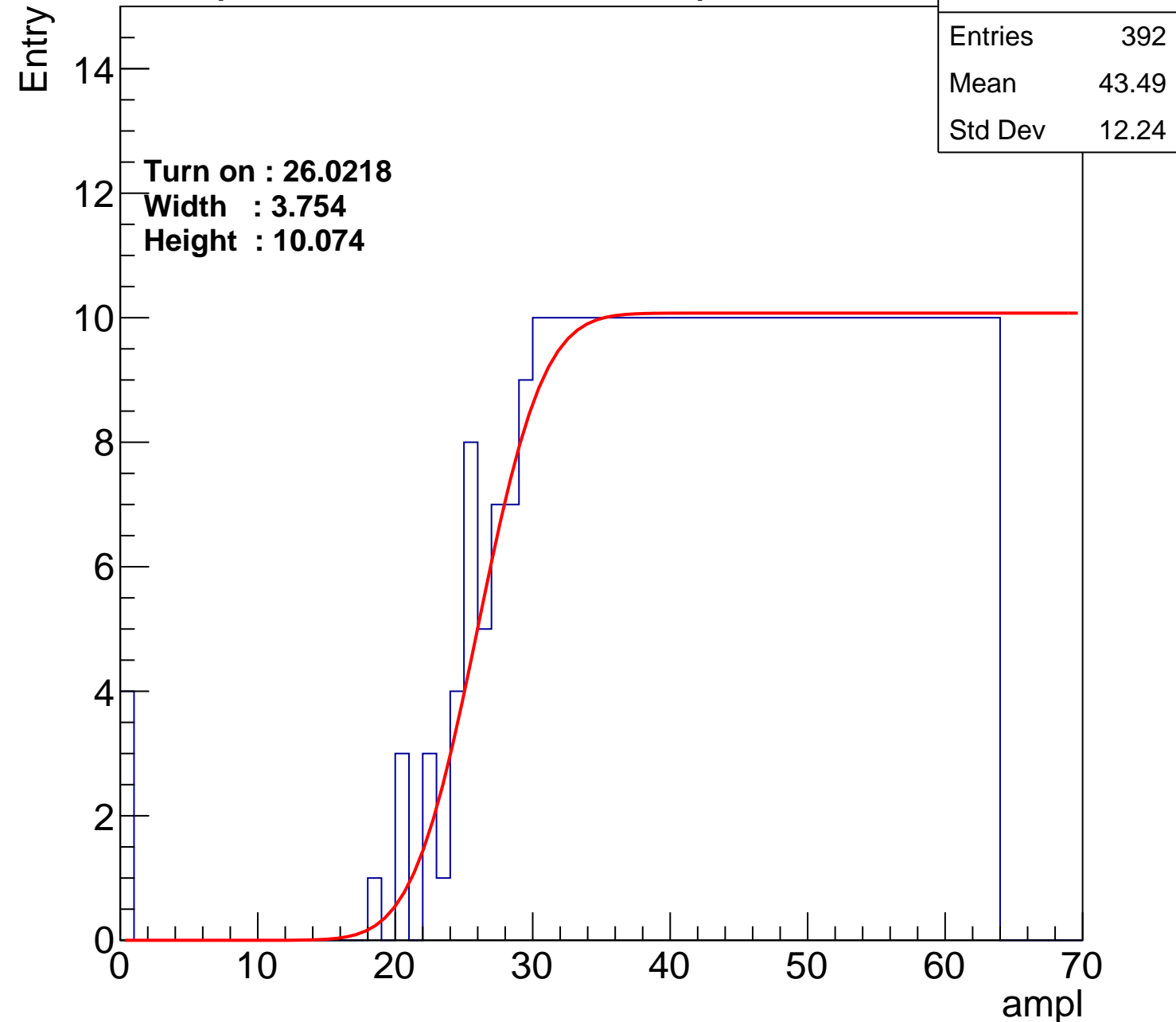
Width : 3.754

Height : 10.074

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L000S, U7-ch87

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	392
Mean	43.7
Std Dev	11.78

Turn on : 25.8739

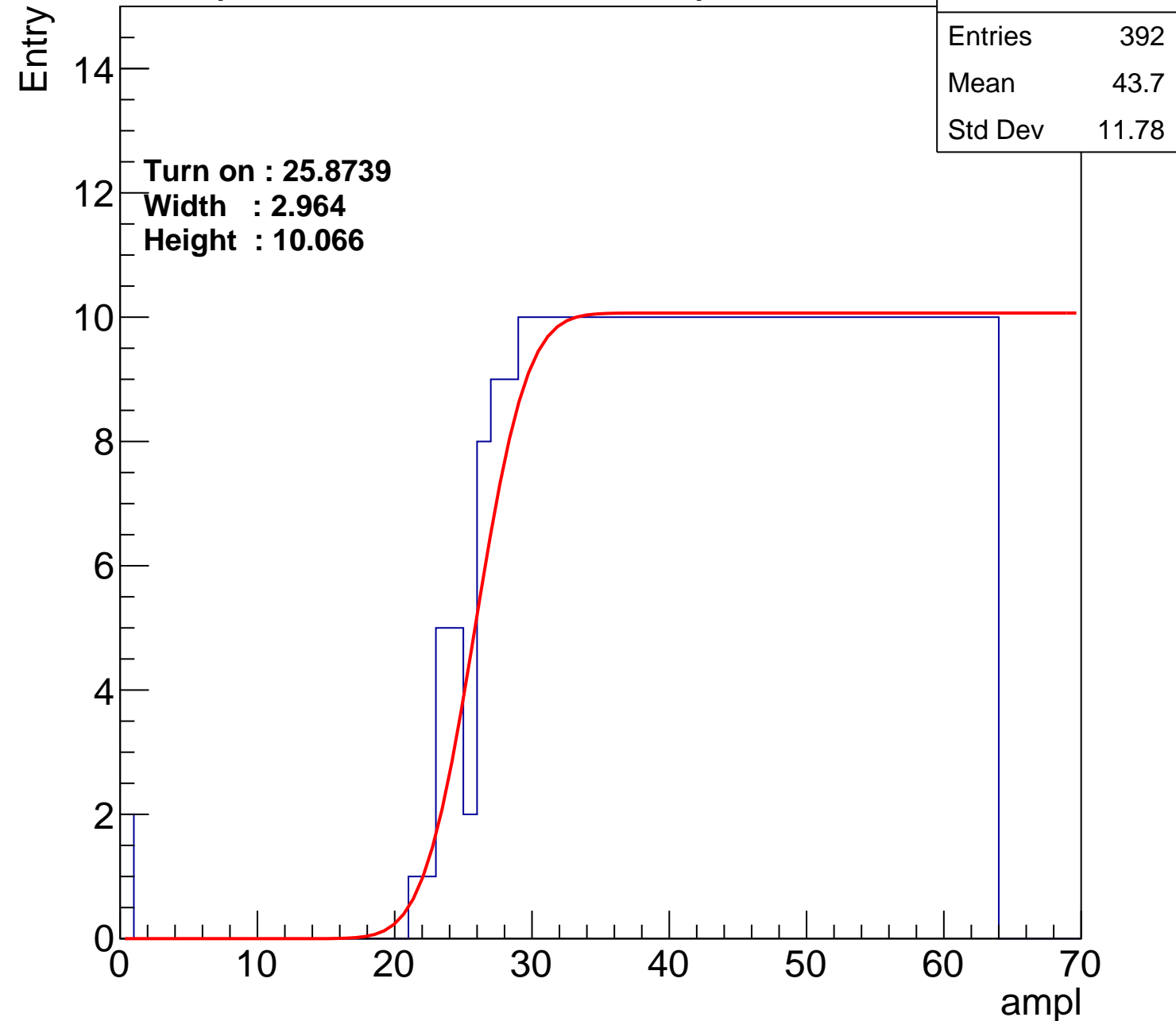
Width : 2.964

Height : 10.066

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch88

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	392
Mean	43.58
Std Dev	12.03

**Turn on : 26.1900**

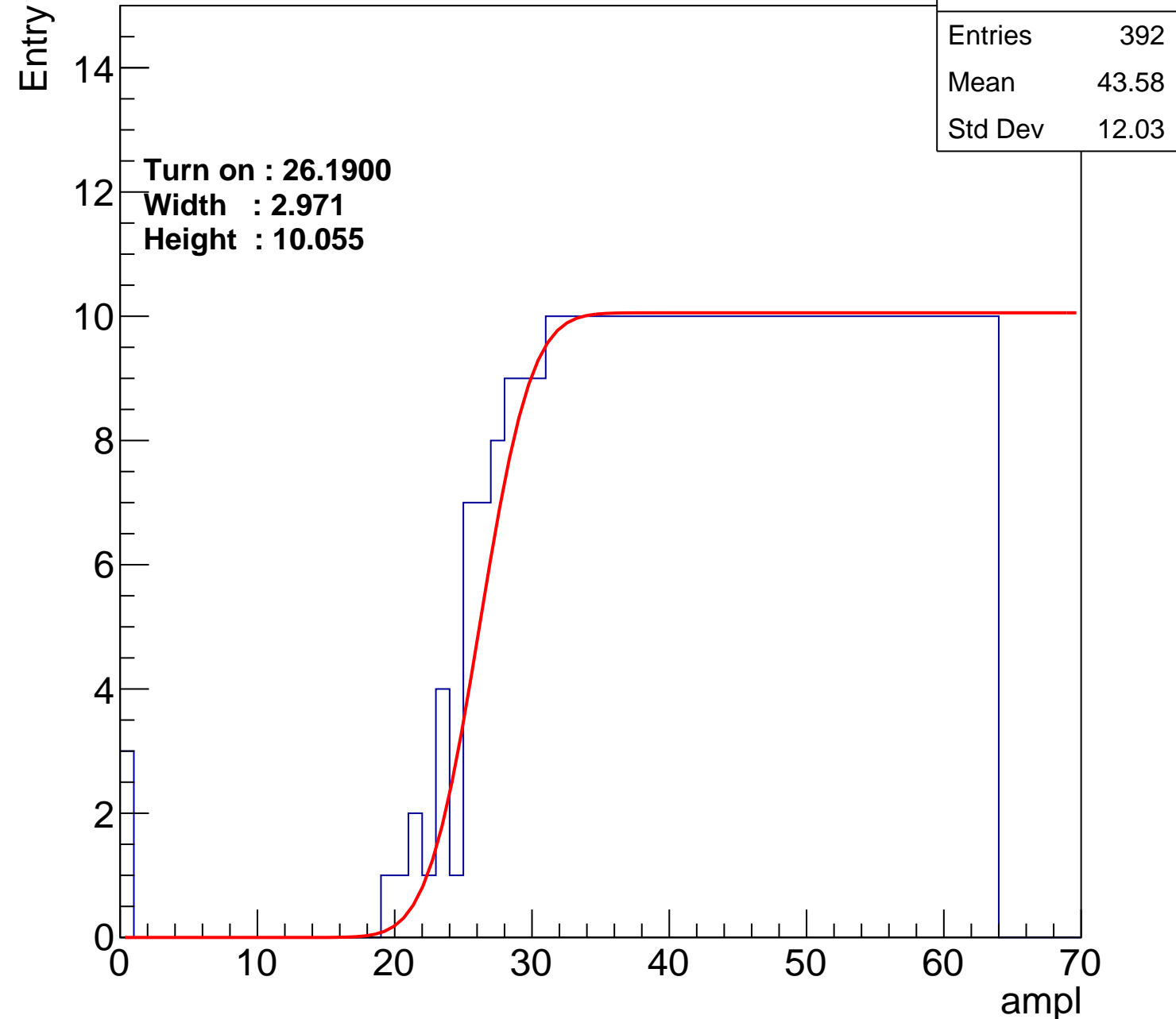
**Width : 2.971**

**Height : 10.055**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch89

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	391
Mean	43.77
Std Dev	11.65

Turn on : 25.7261

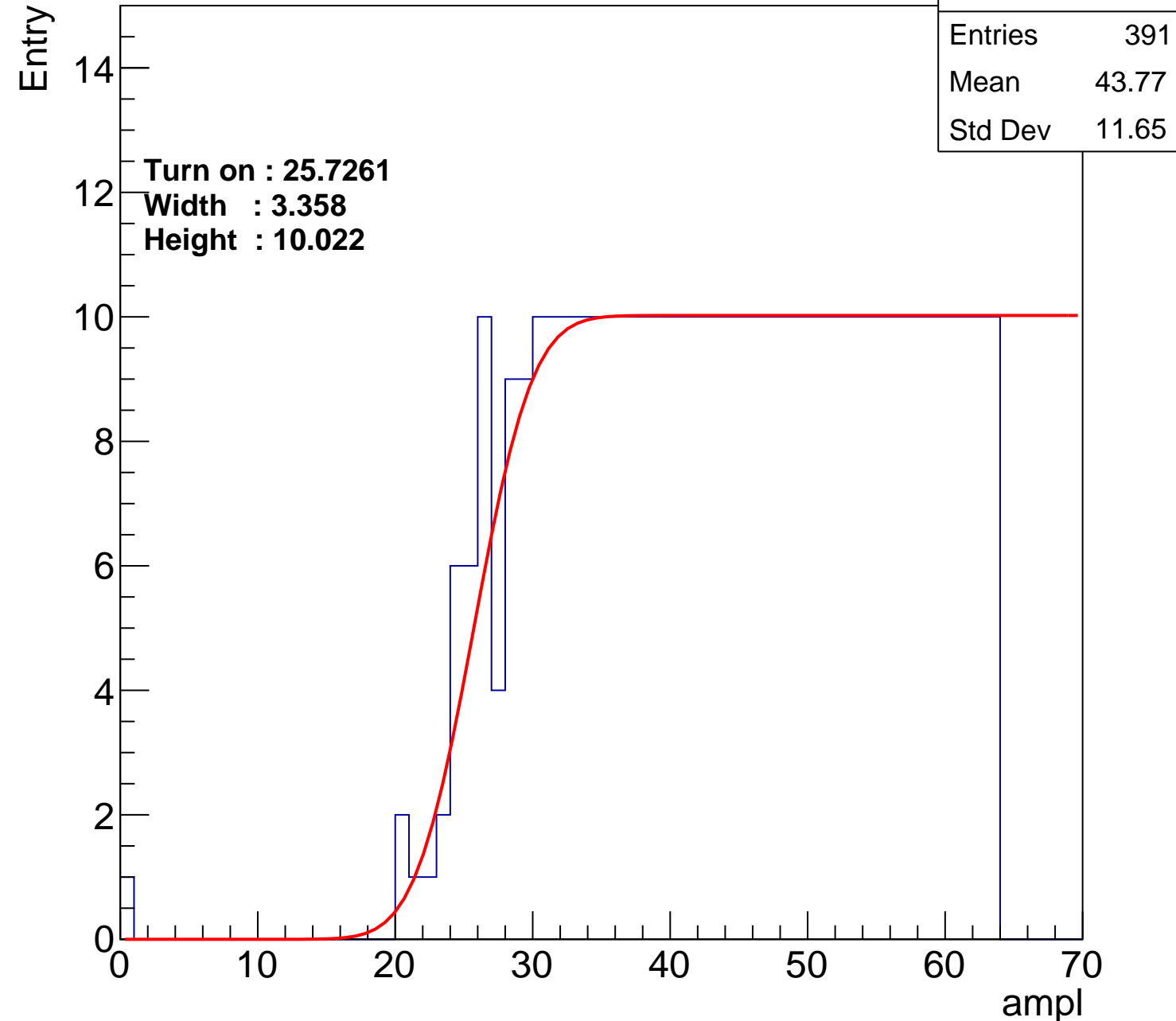
Width : 3.358

Height : 10.022

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch90

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	390
Mean	43.65
Std Dev	12.09

Turn on : 25.4580

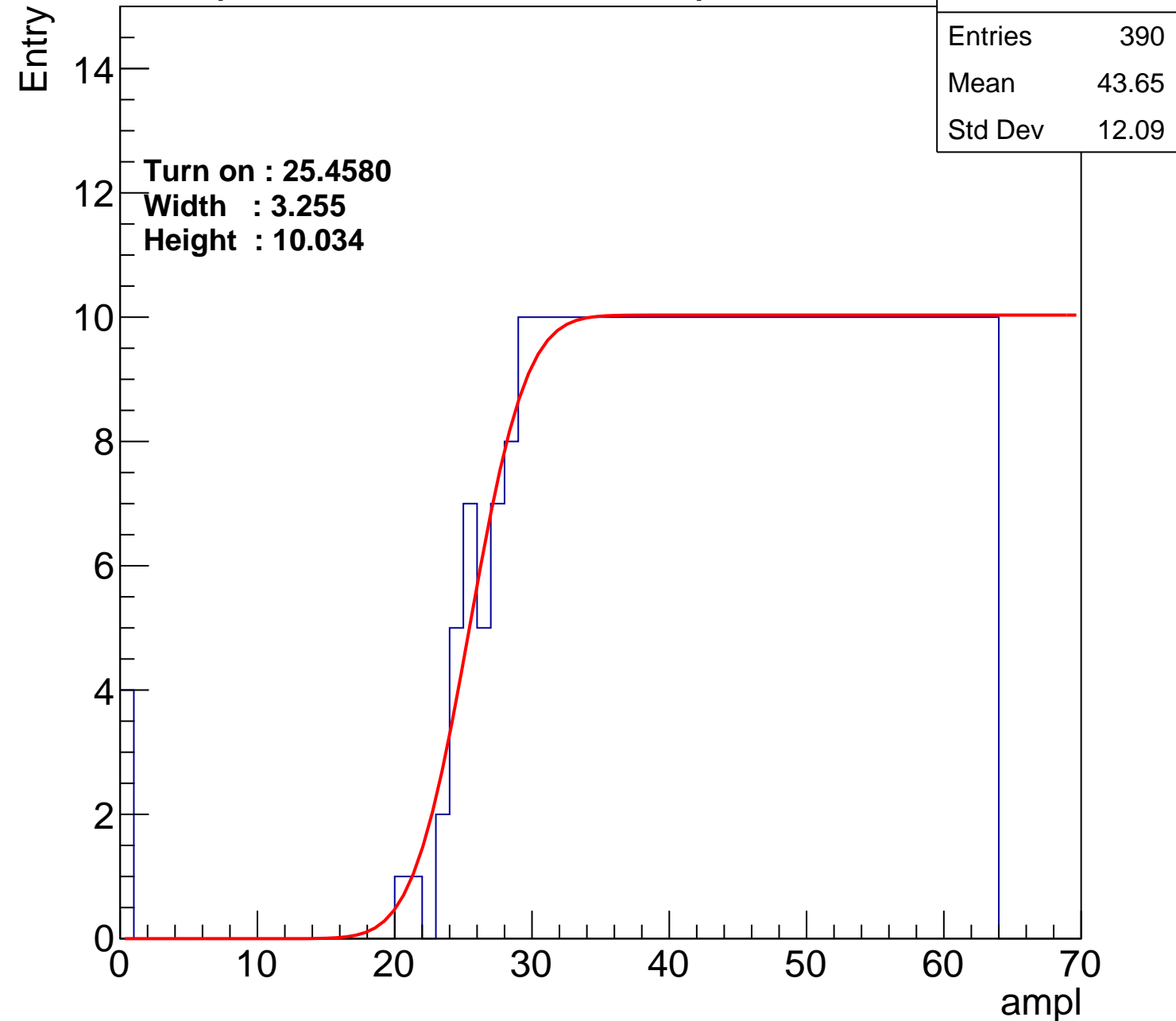
Width : 3.255

Height : 10.034

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch91

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	378
Mean	44.46
Std Dev	11.23

**Turn on : 26.8830**

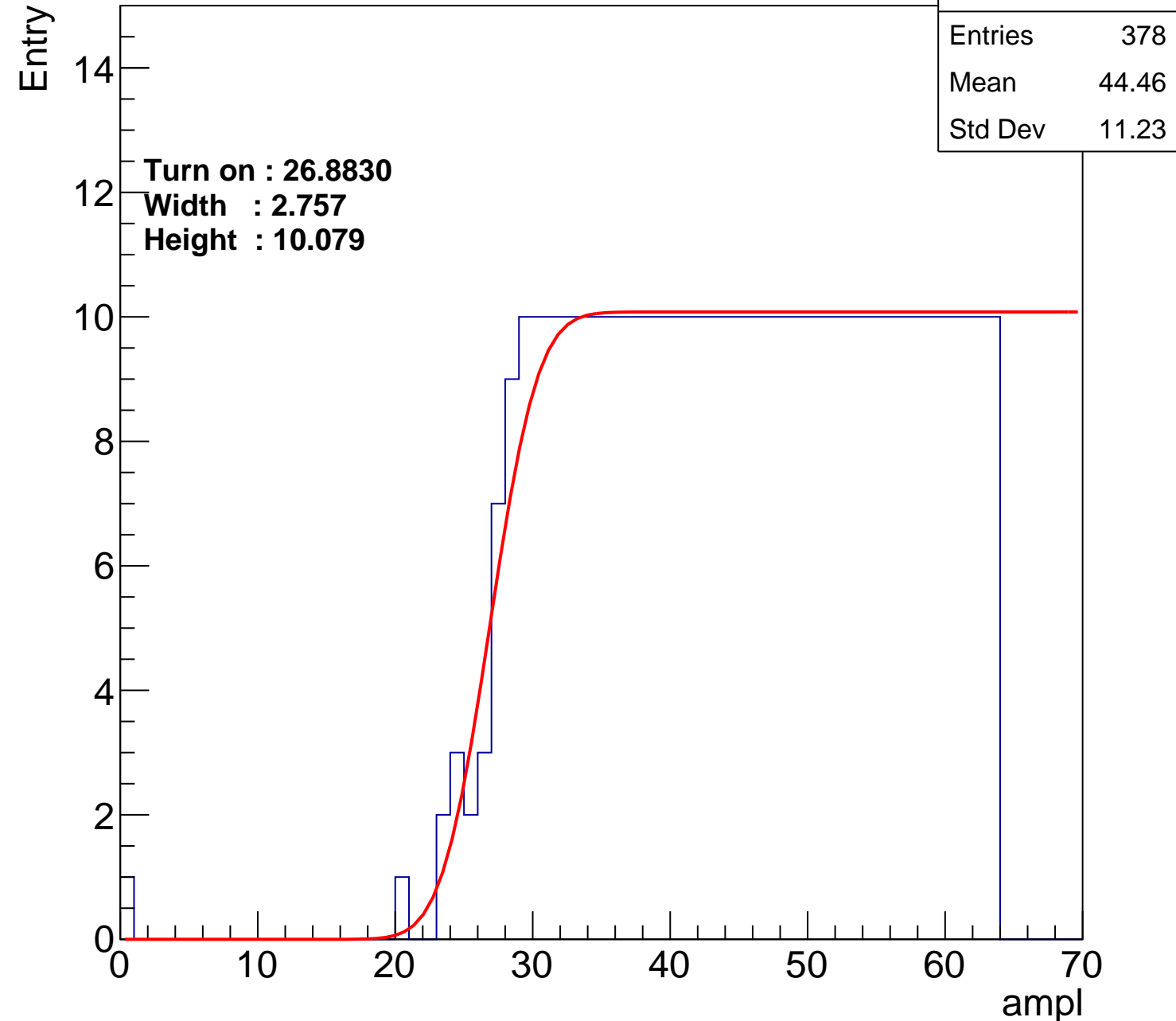
**Width : 2.757**

**Height : 10.079**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch92

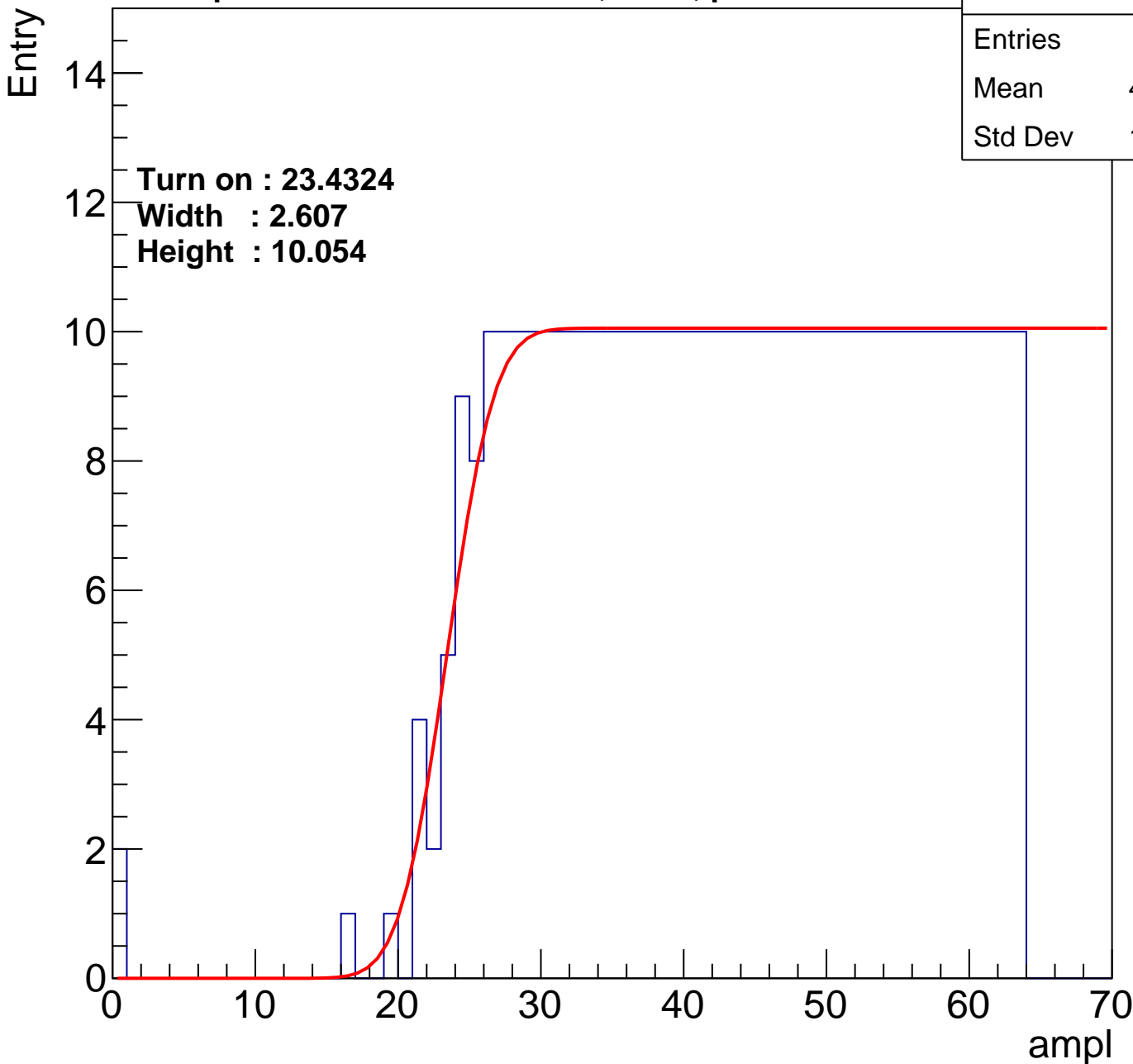
**calib\_packv5\_042523\_0143.root, FC#3, port B3**

Entries	412
Mean	42.73
Std Dev	12.29

**Turn on : 23.4324**

**Width : 2.607**

**Height : 10.054**



# B1L000S, U7-ch93

calib\_packv5\_042523\_0143.root, FC#3, port B3

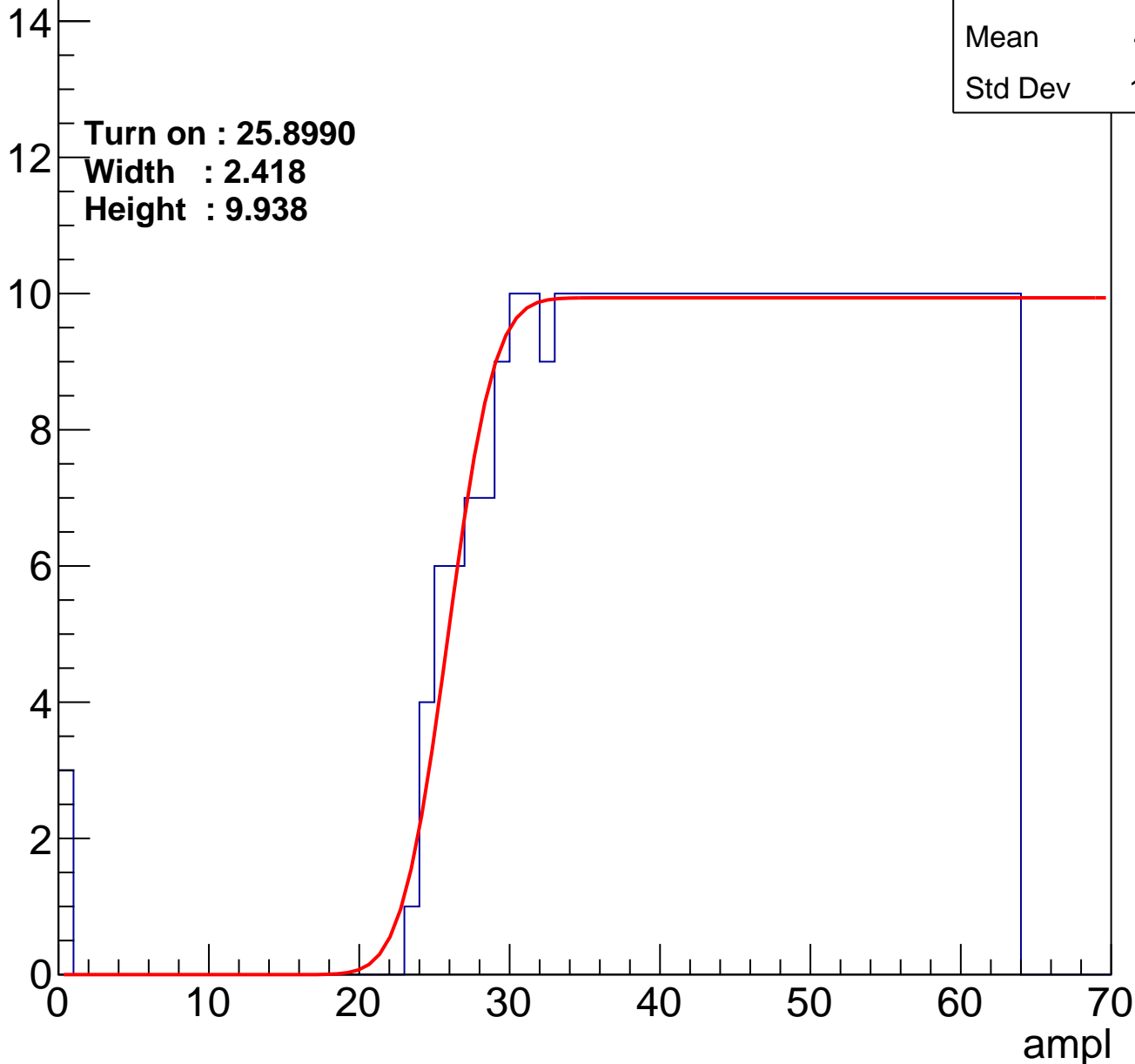
Entry

Entries	382
Mean	44.11
Std Dev	11.72

Turn on : 25.8990

Width : 2.418

Height : 9.938



# B1L000S, U7-ch94

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	397
Mean	43.37
Std Dev	12.11

**Turn on : 24.9691**

**Width : 3.402**

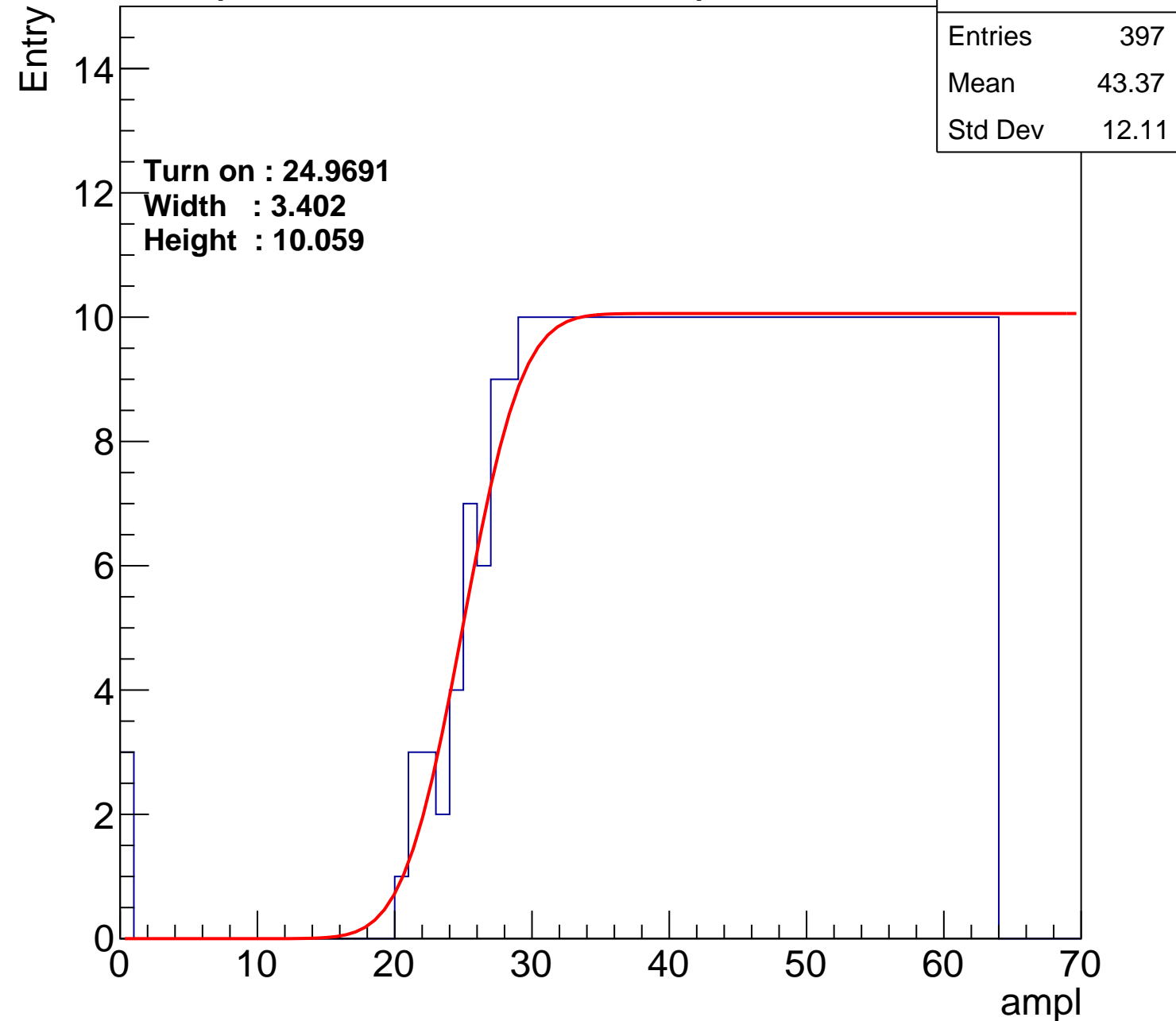
**Height : 10.059**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70





# B1L000S, U7-ch95

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	381
Mean	44.25
Std Dev	11.47

**Turn on : 26.3108**

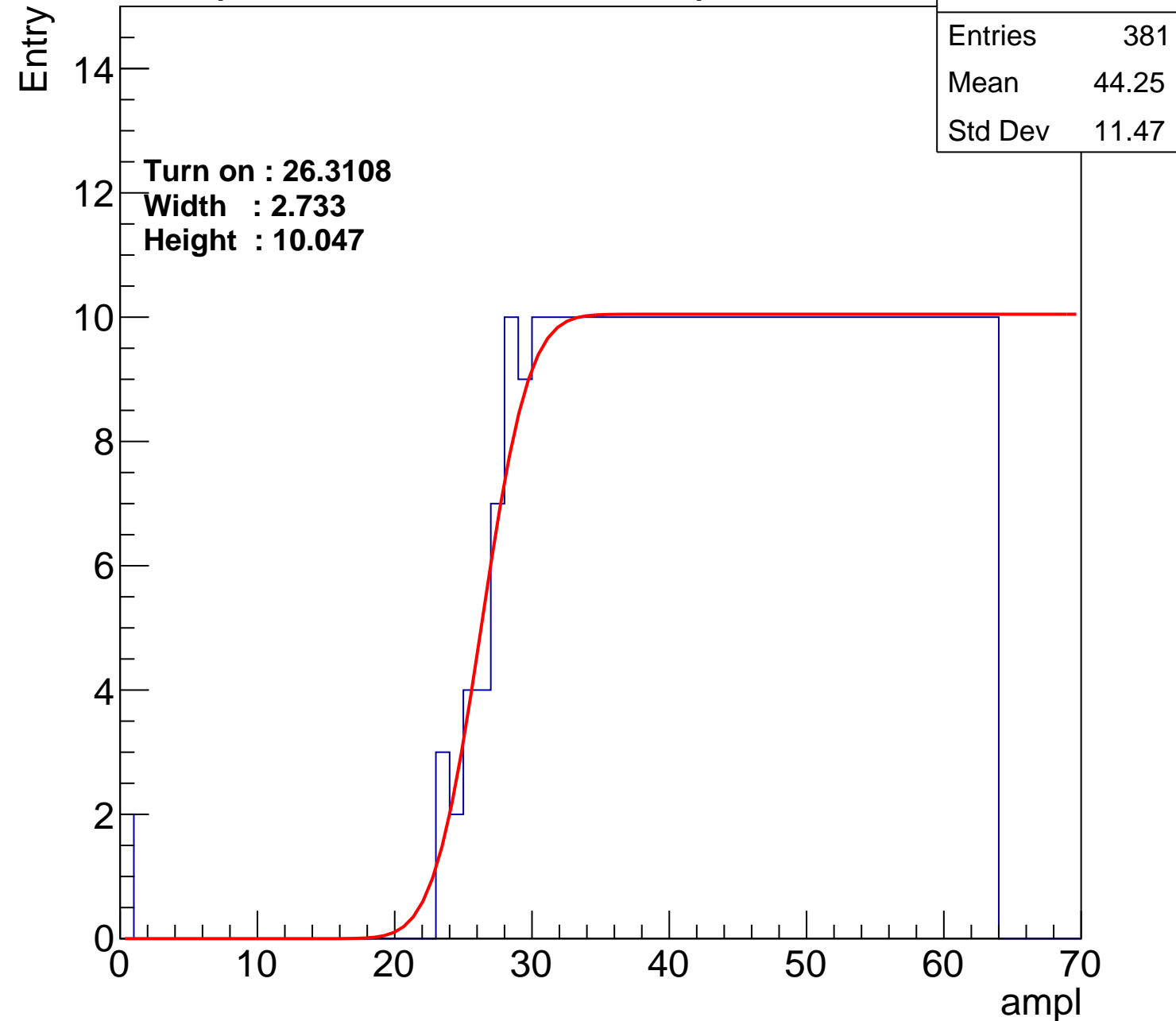
**Width : 2.733**

**Height : 10.047**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch96

calib\_packv5\_042523\_0143.root, FC#3, port B3

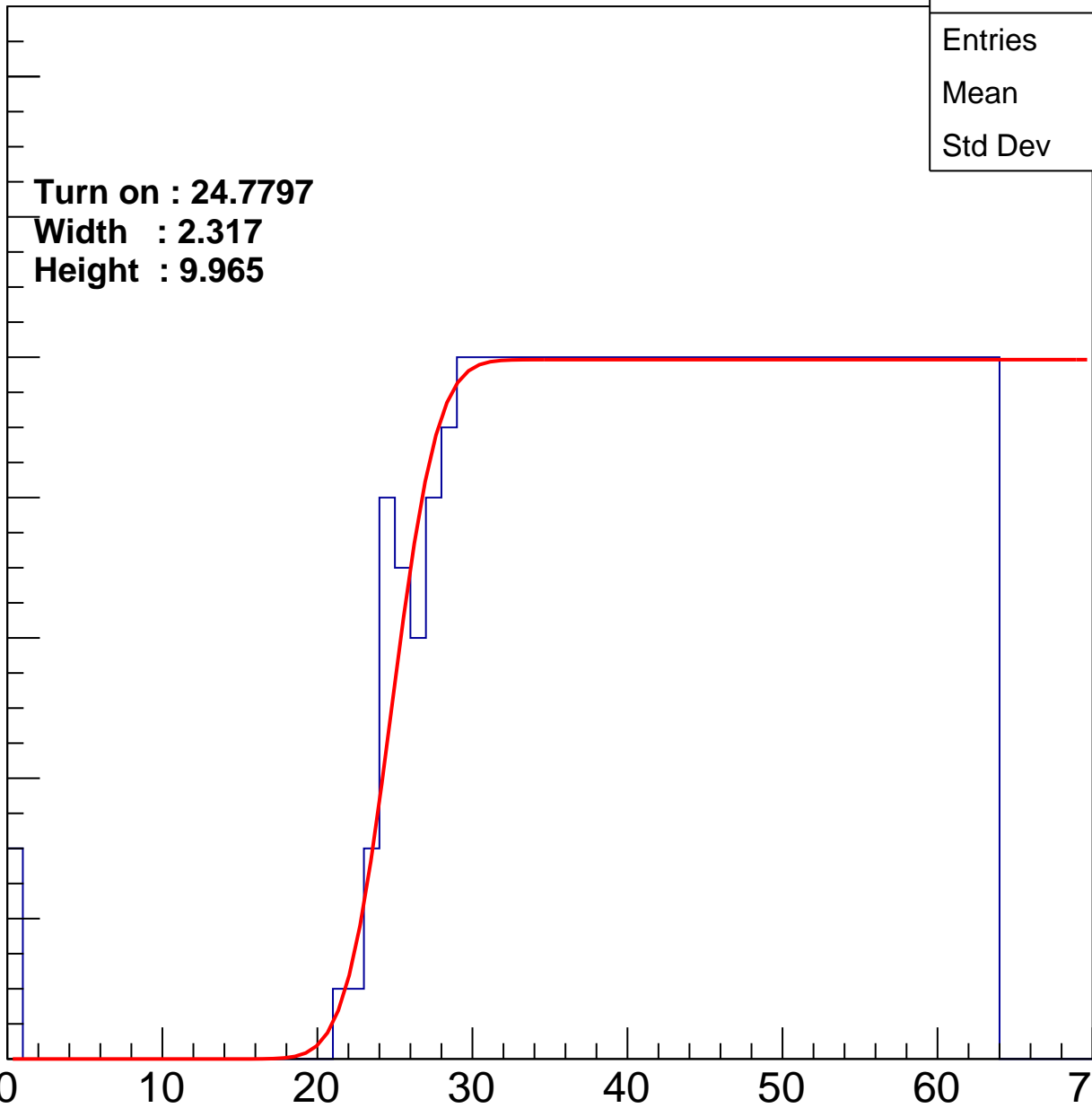
Entry

14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 24.7797**  
**Width : 2.317**  
**Height : 9.965**

Entries	396
Mean	43.44
Std Dev	12.04

ampl



# B1L000S, U7-ch97

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	376
Mean	44.08
Std Dev	12.38

Turn on : 27.7404

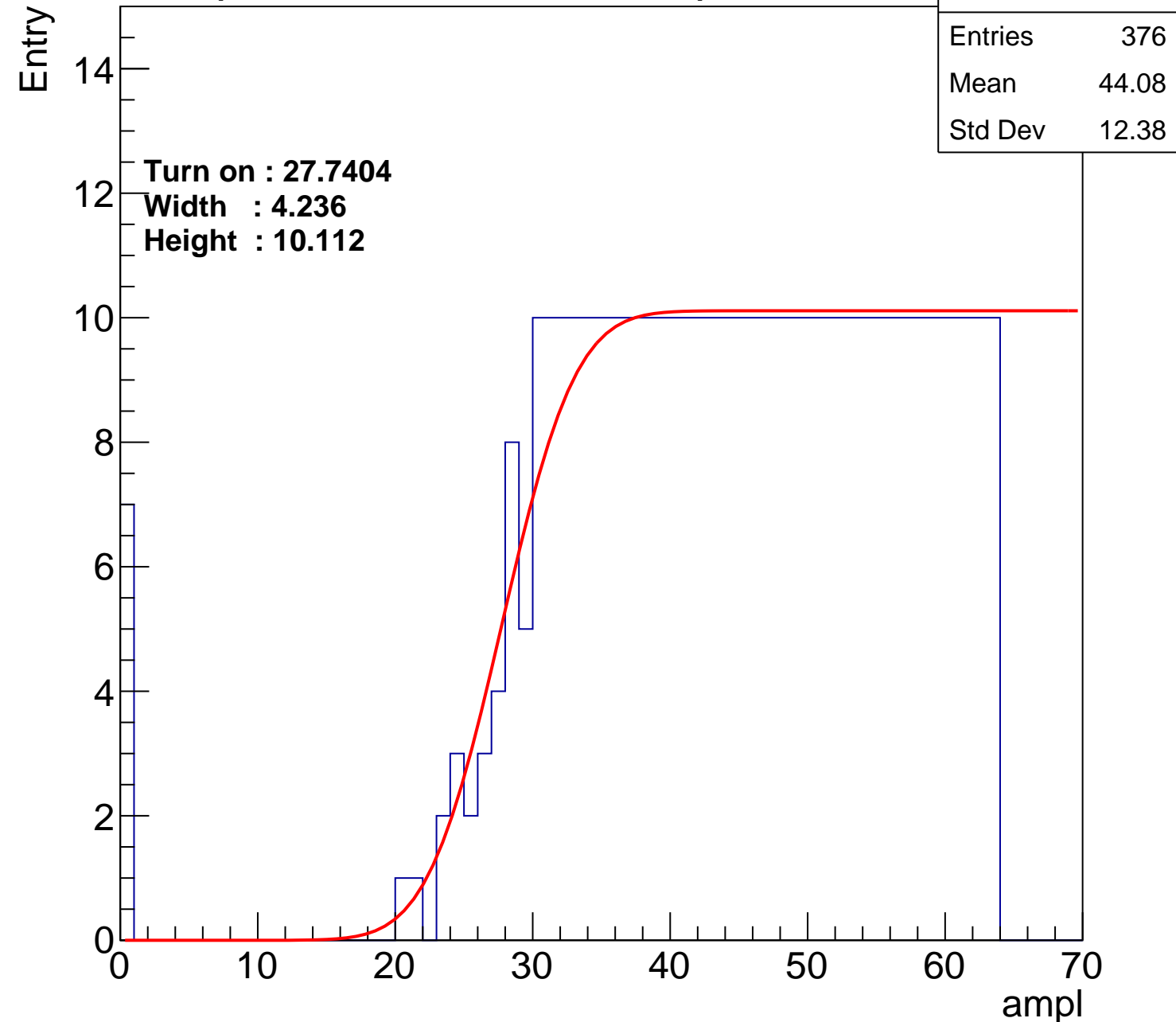
Width : 4.236

Height : 10.112

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch98

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	387
Mean	43.96
Std Dev	11.62

Turn on : 25.3412

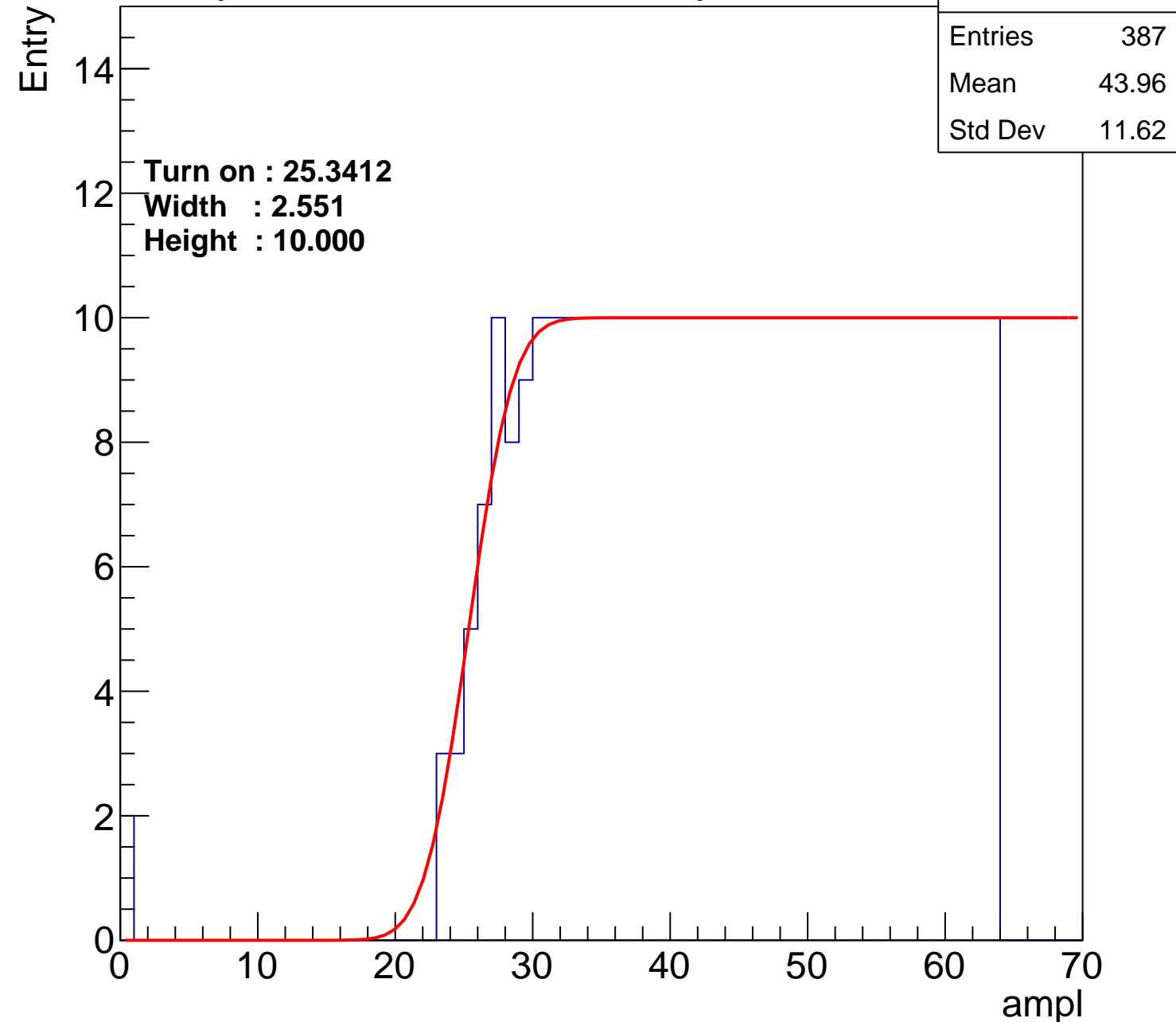
Width : 2.551

Height : 10.000

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch99

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	361
Mean	45.21
Std Dev	11.02

**Turn on : 28.6299**

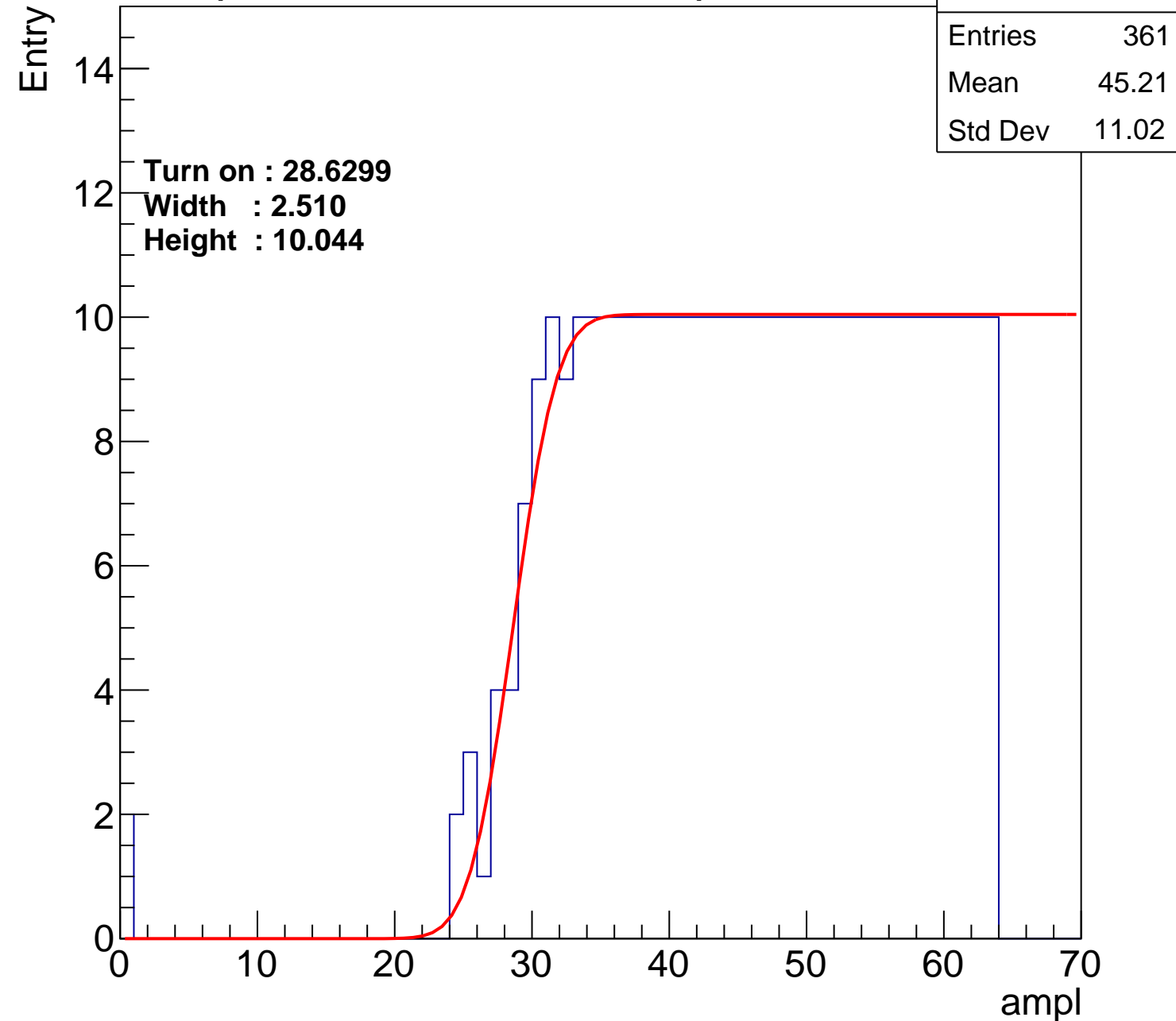
**Width : 2.510**

**Height : 10.044**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch100

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	394
Mean	43.59
Std Dev	11.84

**Turn on : 24.6653**

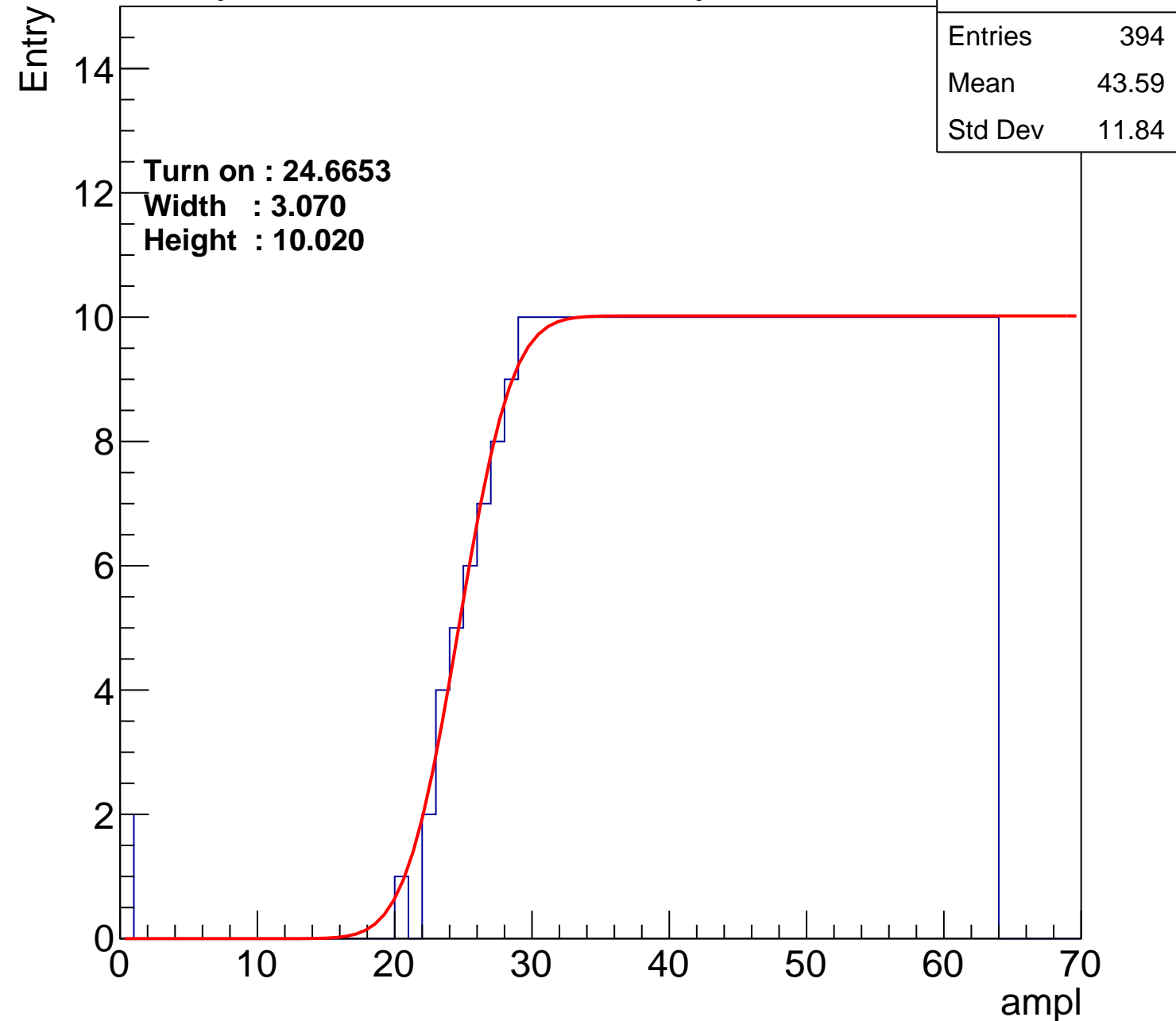
**Width : 3.070**

**Height : 10.020**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch101

calib\_packv5\_042523\_0143.root, FC#3, port B3

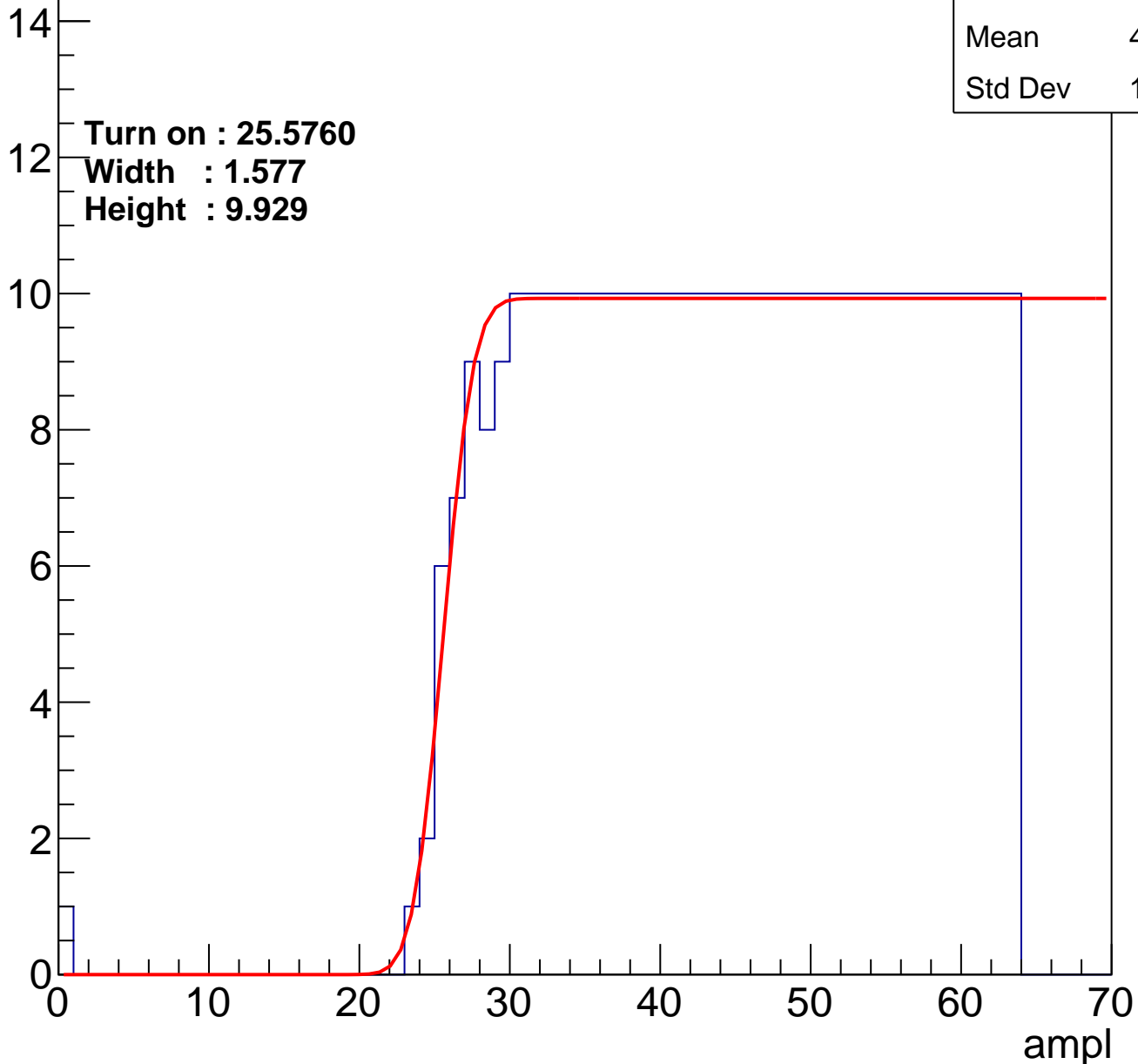
Entries	383
Mean	44.23
Std Dev	11.32

Turn on : 25.5760

Width : 1.577

Height : 9.929

Entry



# B1L000S, U7-ch102

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	385
Mean	43.99
Std Dev	11.75

Turn on : 24.8292

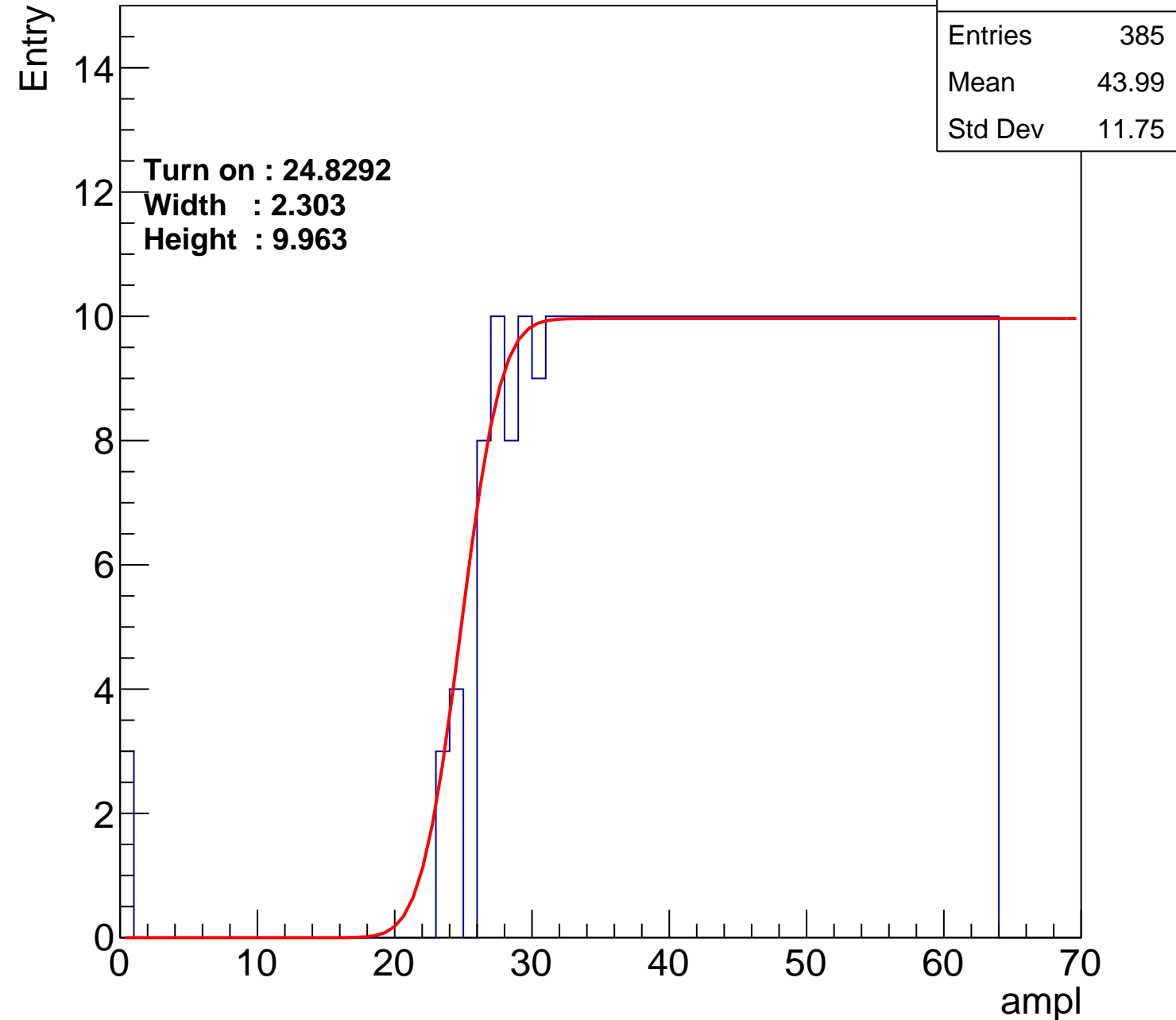
Width : 2.303

Height : 9.963

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L000S, U7-ch103

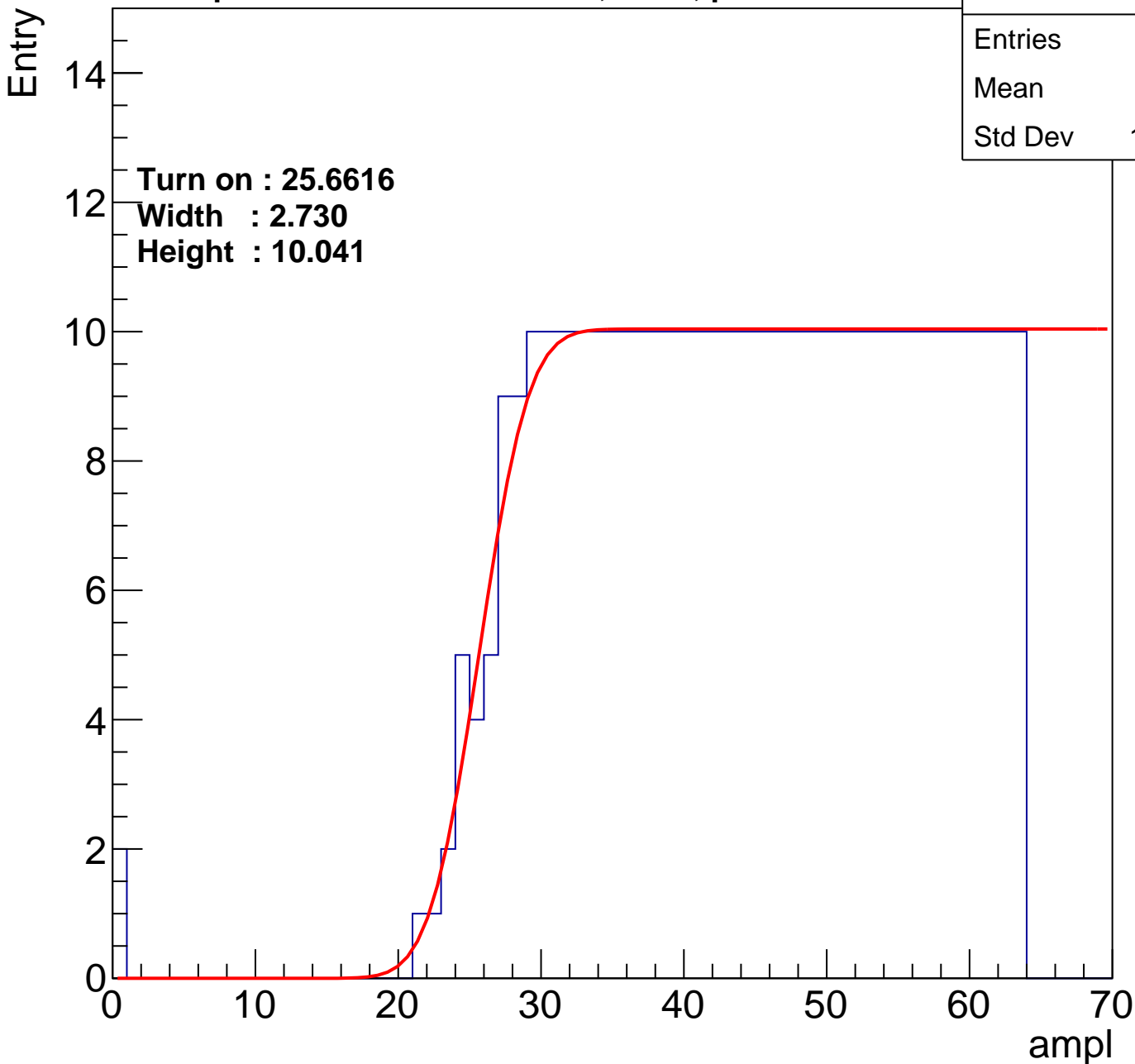
calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	388
Mean	43.9
Std Dev	11.67

Turn on : 25.6616

Width : 2.730

Height : 10.041



# B1L000S, U7-ch104

calib\_packv5\_042523\_0143.root, FC#3, port B3

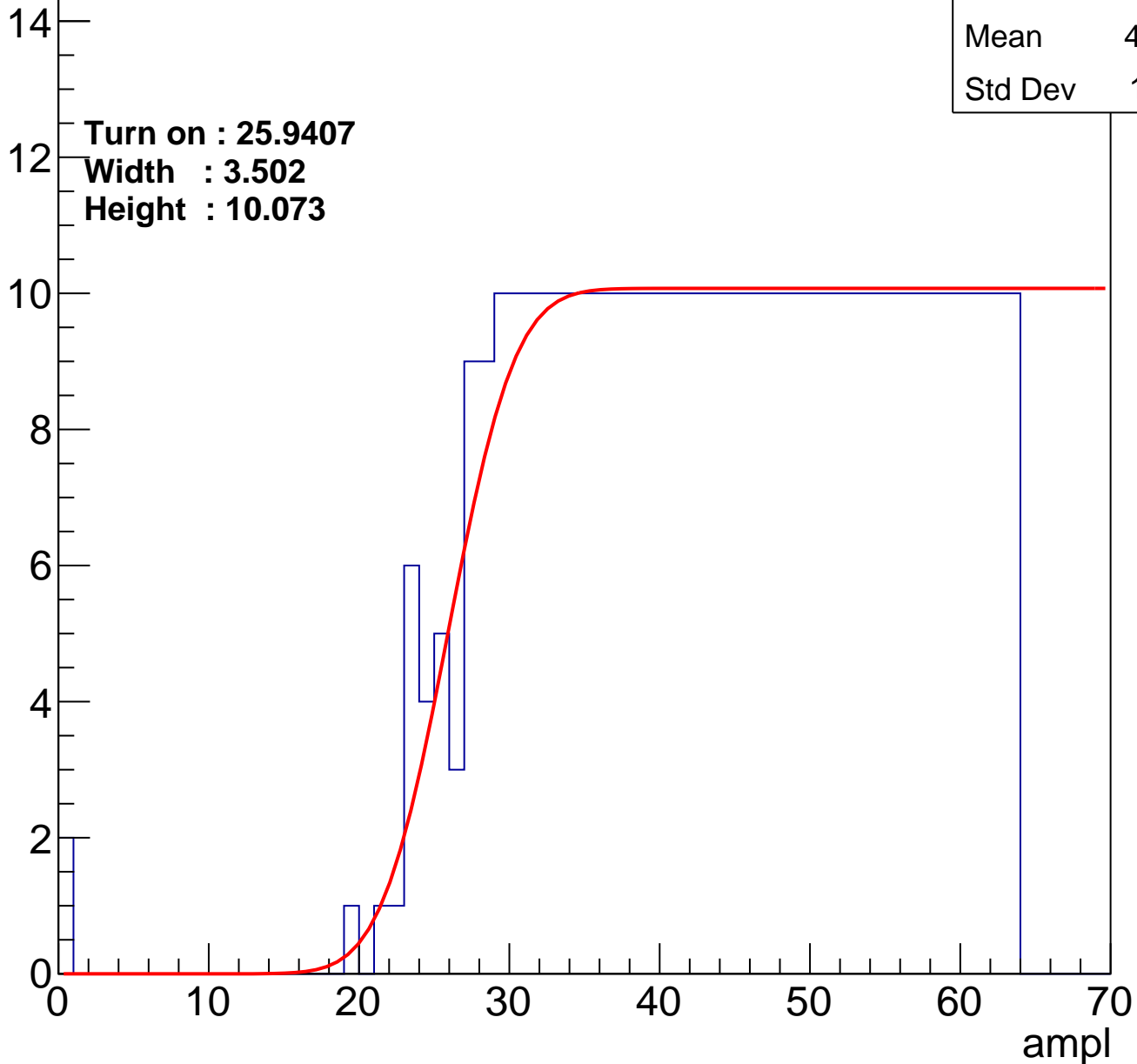
Entries	391
Mean	43.72
Std Dev	11.81

Turn on : 25.9407

Width : 3.502

Height : 10.073

Entry



# B1L000S, U7-ch105

calib\_packv5\_042523\_0143.root, FC#3, port B3

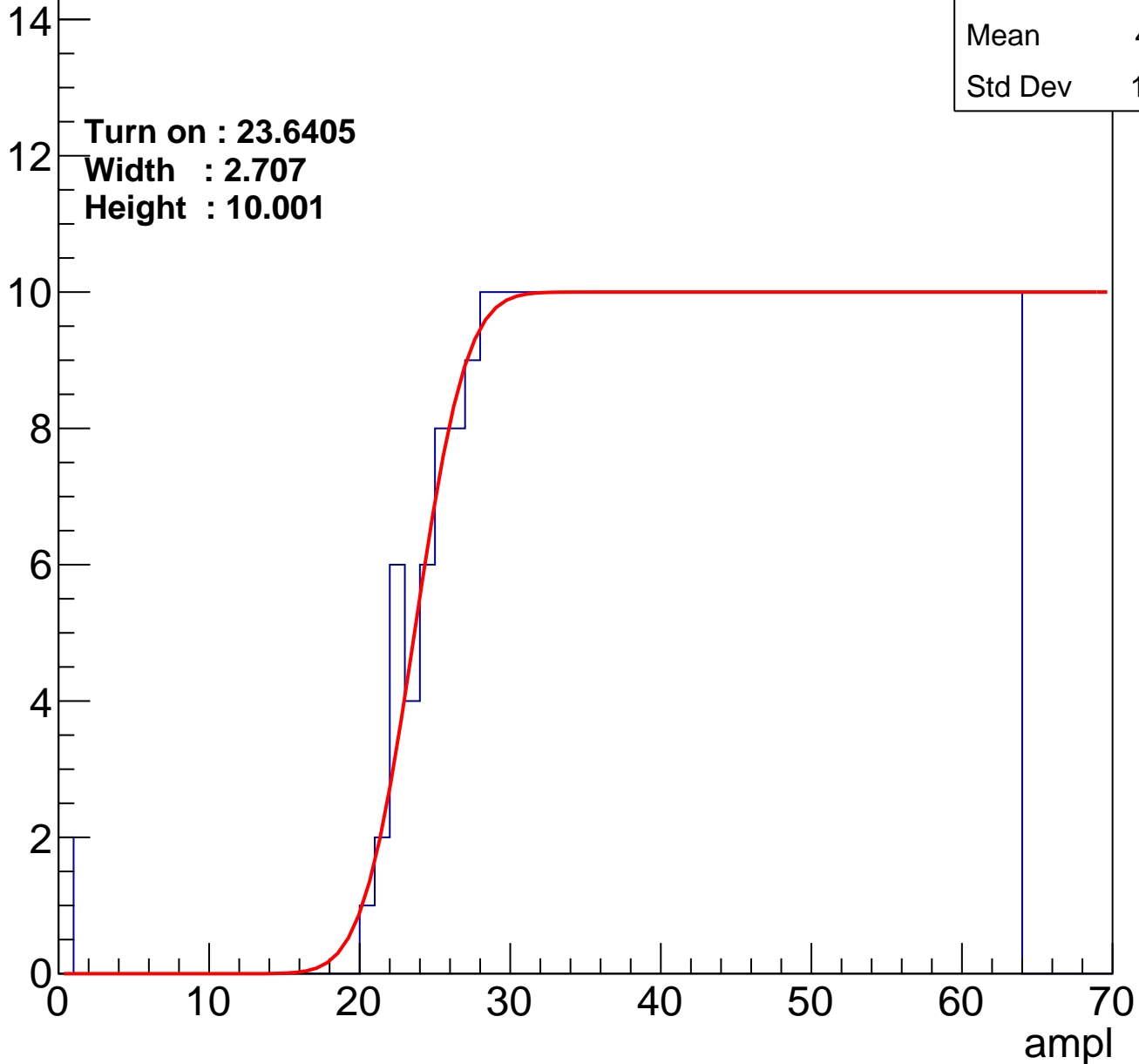
Entries	406
Mean	43.01
Std Dev	12.15

**Turn on : 23.6405**

**Width : 2.707**

**Height : 10.001**

Entry



# B1L000S, U7-ch106

calib\_packv5\_042523\_0143.root, FC#3, port B3

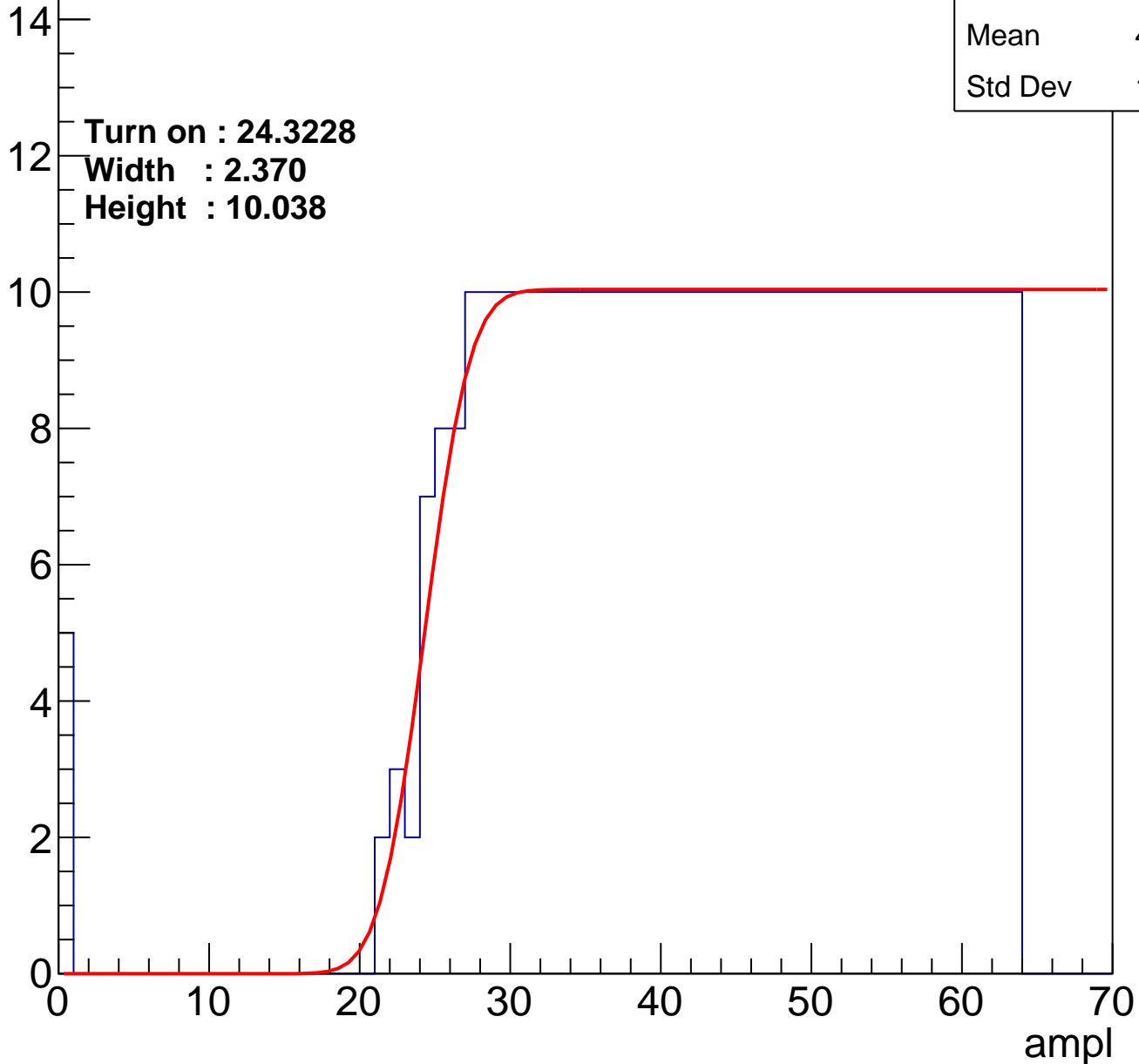
Entries	405
Mean	42.91
Std Dev	12.51

Turn on : 24.3228

Width : 2.370

Height : 10.038

Entry



# B1L000S, U7-ch107

calib\_packv5\_042523\_0143.root, FC#3, port B3

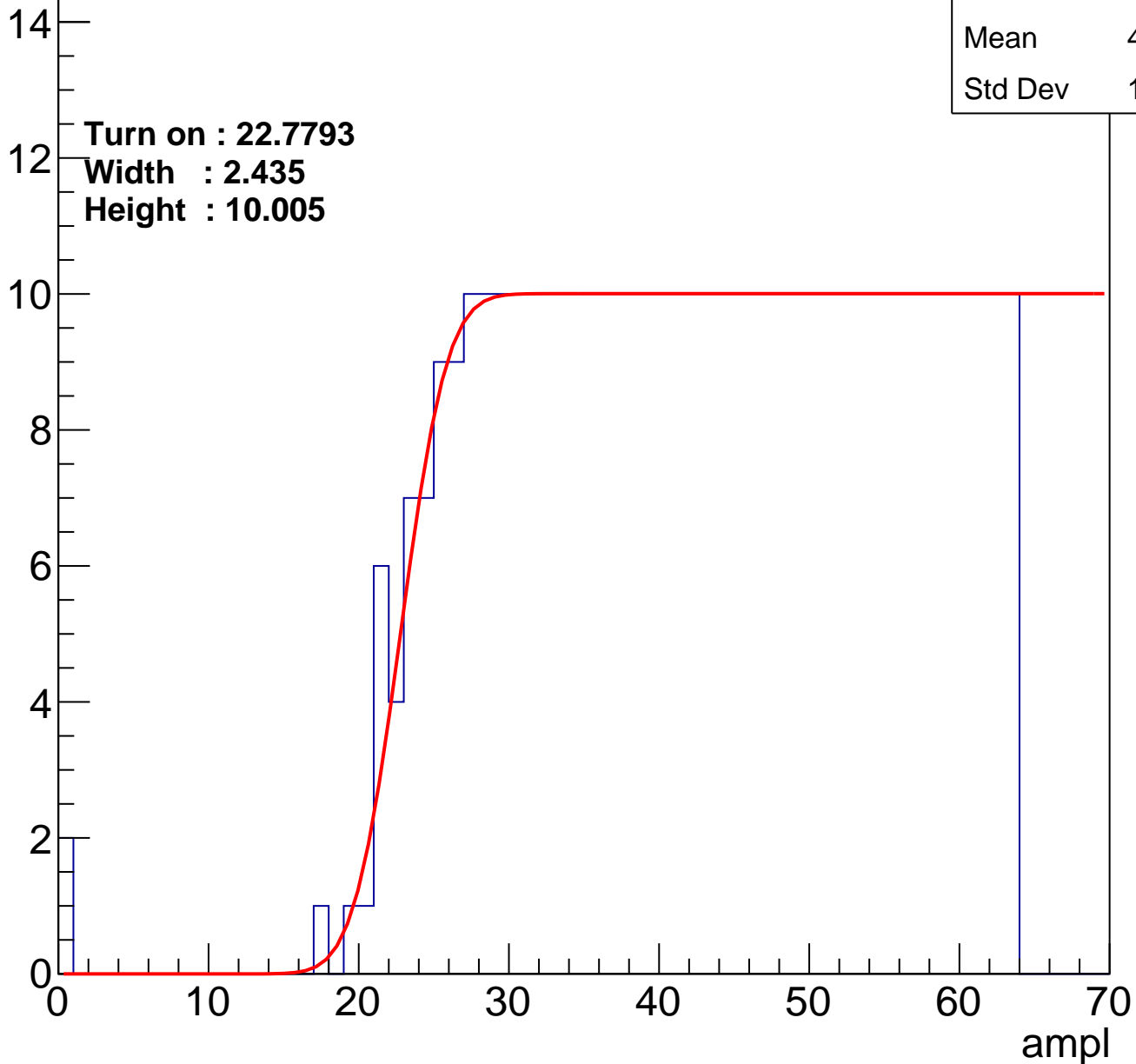
Entries	417
Mean	42.47
Std Dev	12.44

Turn on : 22.7793

Width : 2.435

Height : 10.005

Entry



# B1L000S, U7-ch108

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	392
Mean	43.51
Std Dev	12.26

Turn on : 25.8990

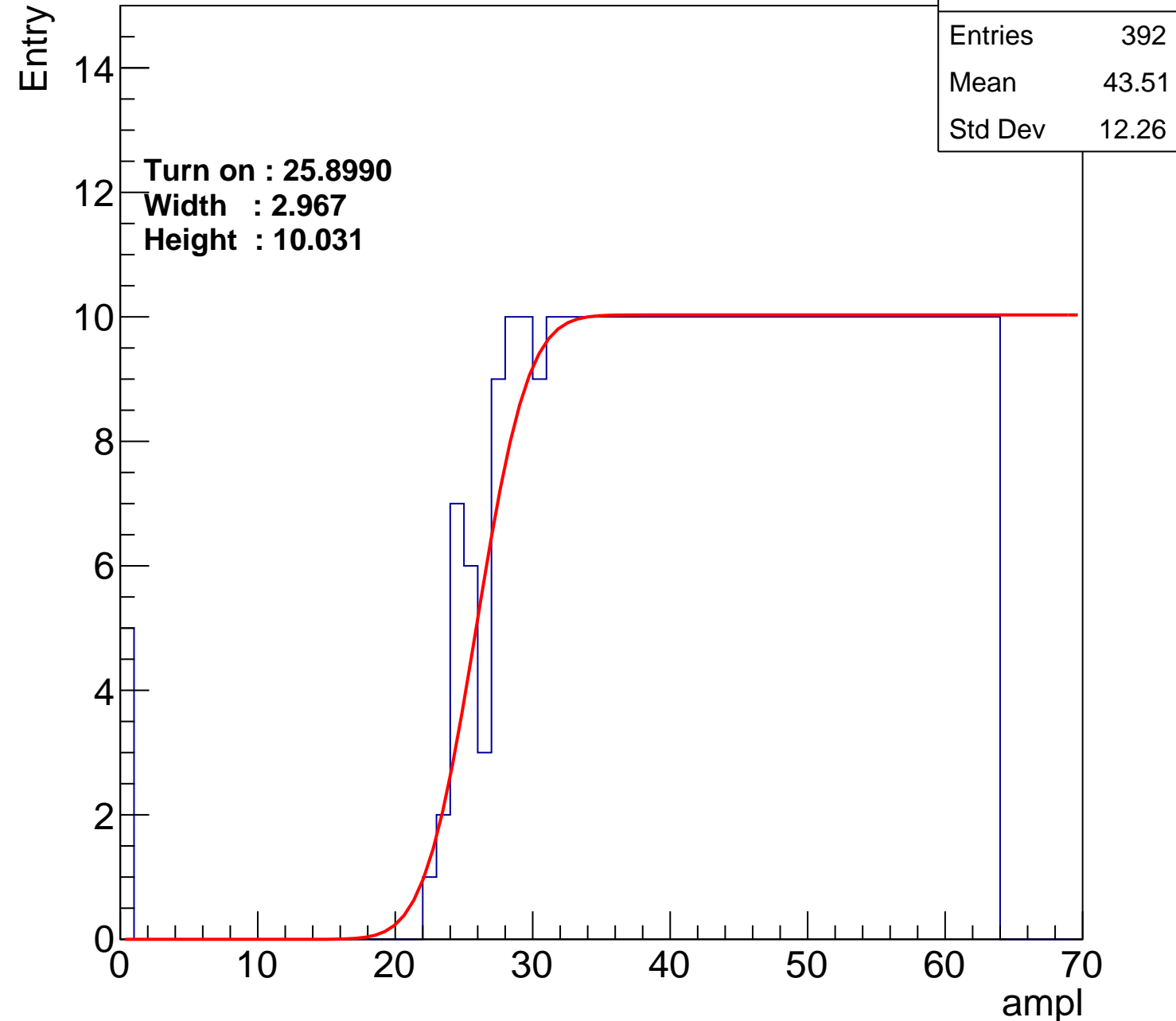
Width : 2.967

Height : 10.031

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch109

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	387
Mean	43.9
Std Dev	11.79

Turn on : 25.3337

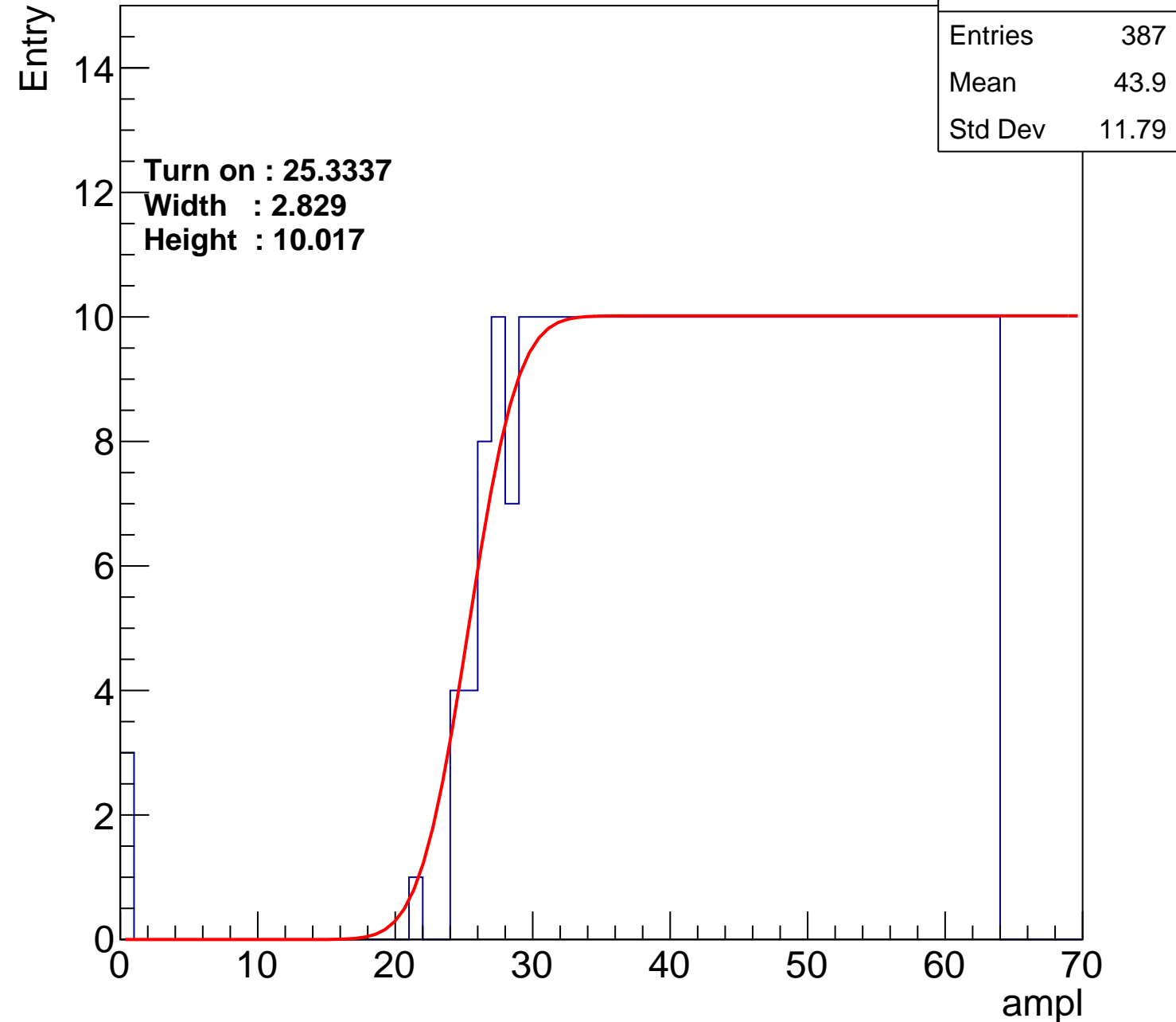
Width : 2.829

Height : 10.017

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch110

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	404
Mean	42.99
Std Dev	12.39

Turn on : 24.2638

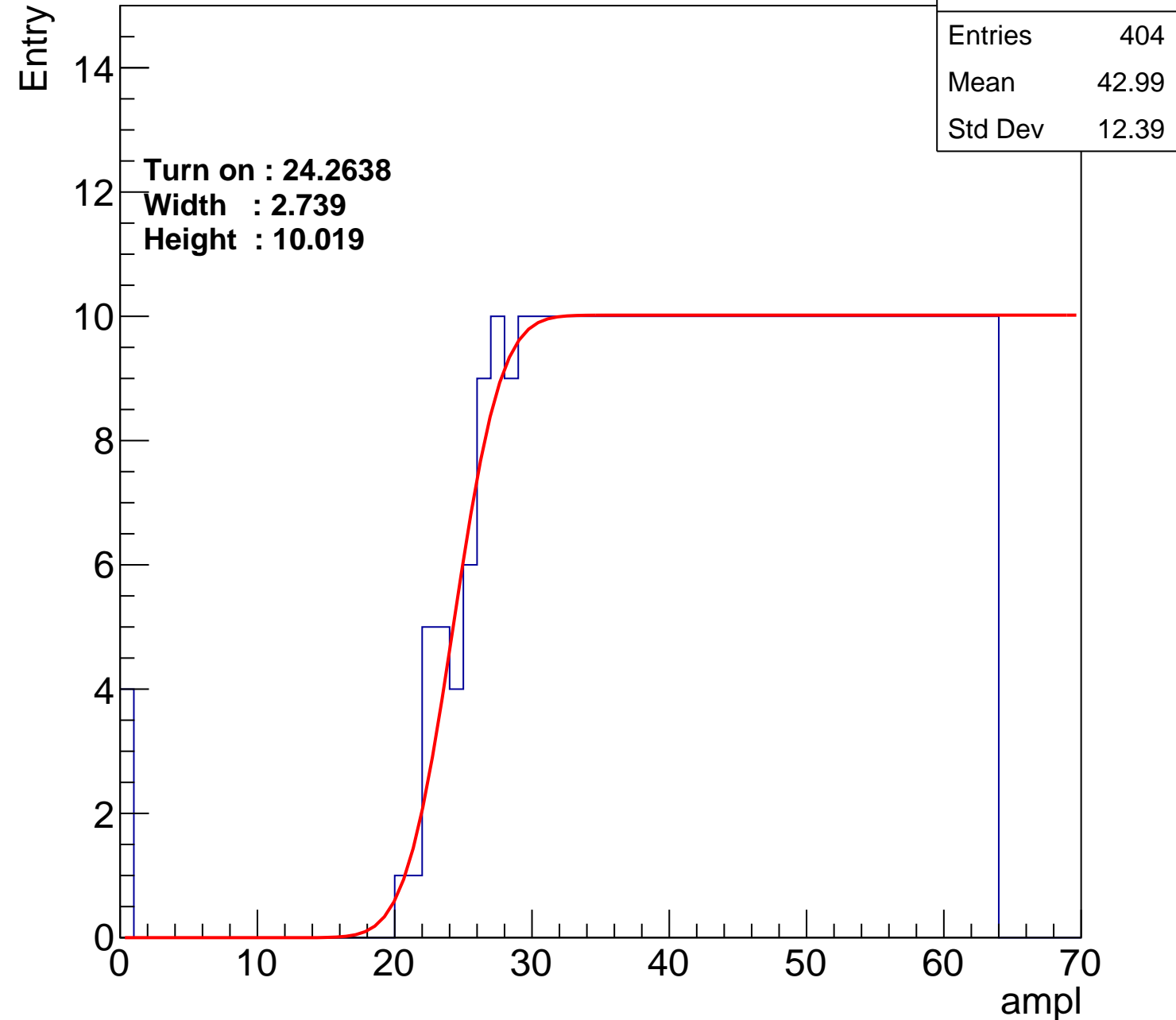
Width : 2.739

Height : 10.019

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L000S, U7-ch111

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	393
Mean	43.5
Std Dev	12.17

Turn on : 25.3843

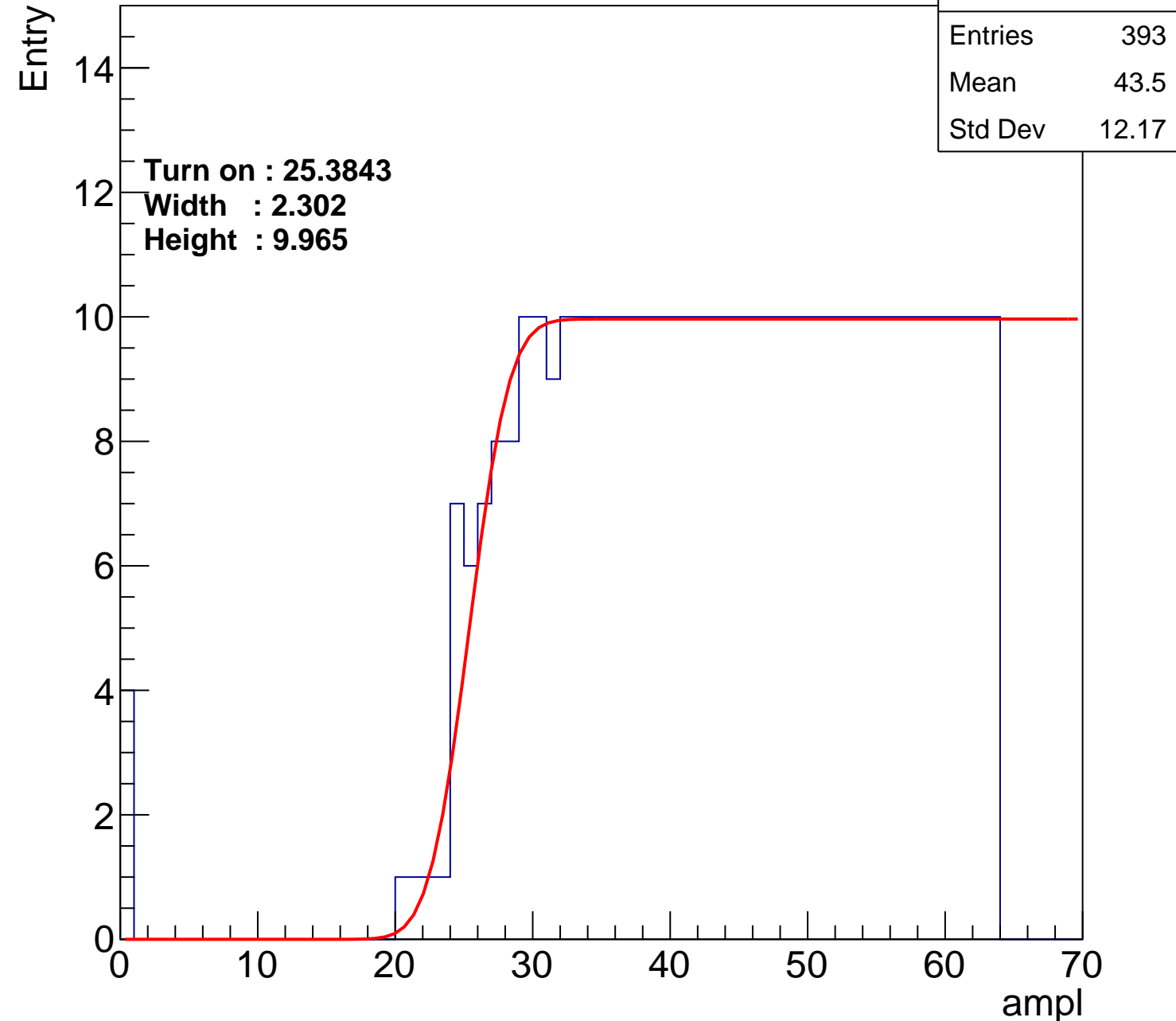
Width : 2.302

Height : 9.965

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch112

calib\_packv5\_042523\_0143.root, FC#3, port B3

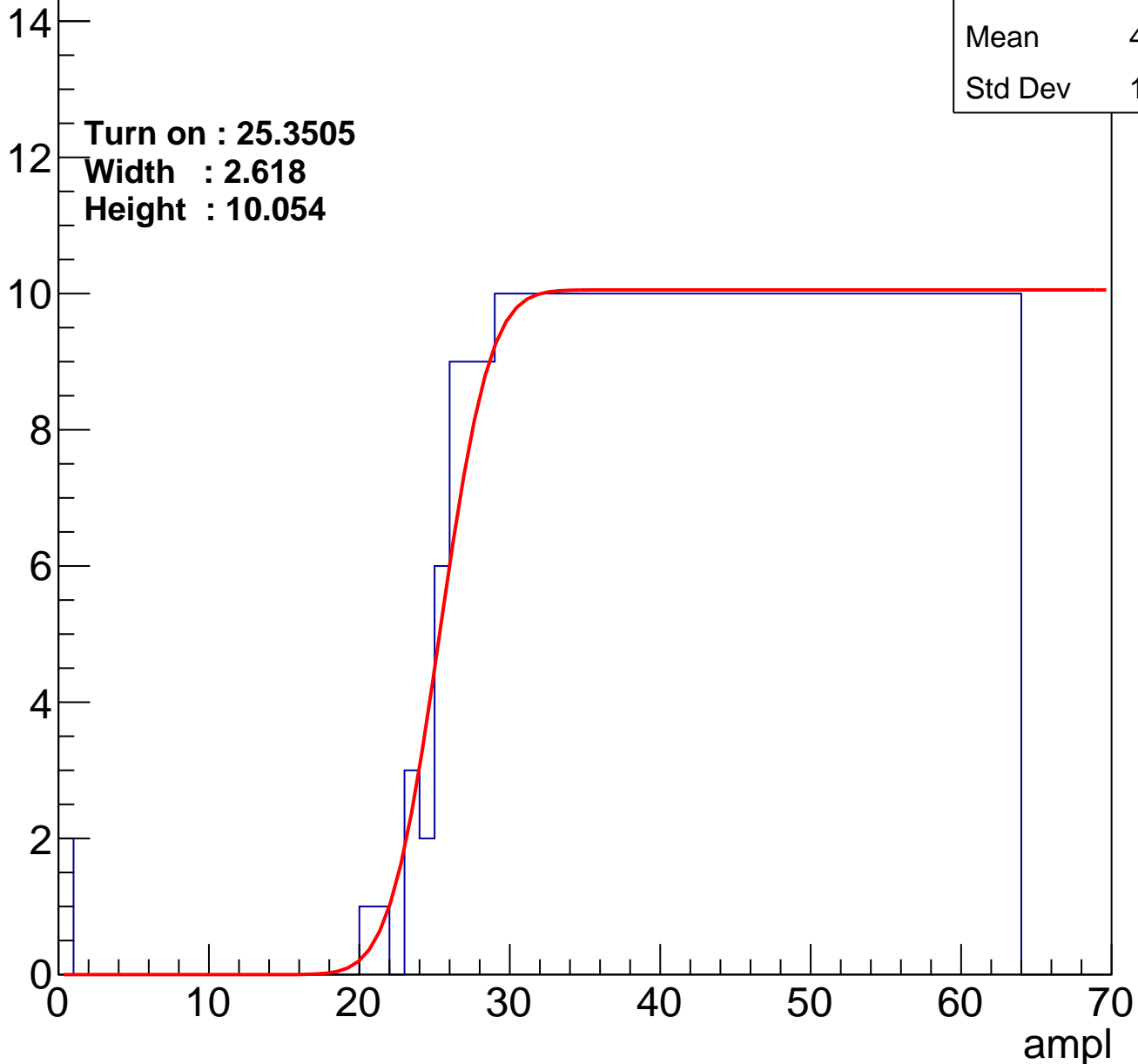
Entries	392
Mean	43.72
Std Dev	11.75

**Turn on : 25.3505**

**Width : 2.618**

**Height : 10.054**

Entry



# B1L000S, U7-ch113

calib\_packv5\_042523\_0143.root, FC#3, port B3

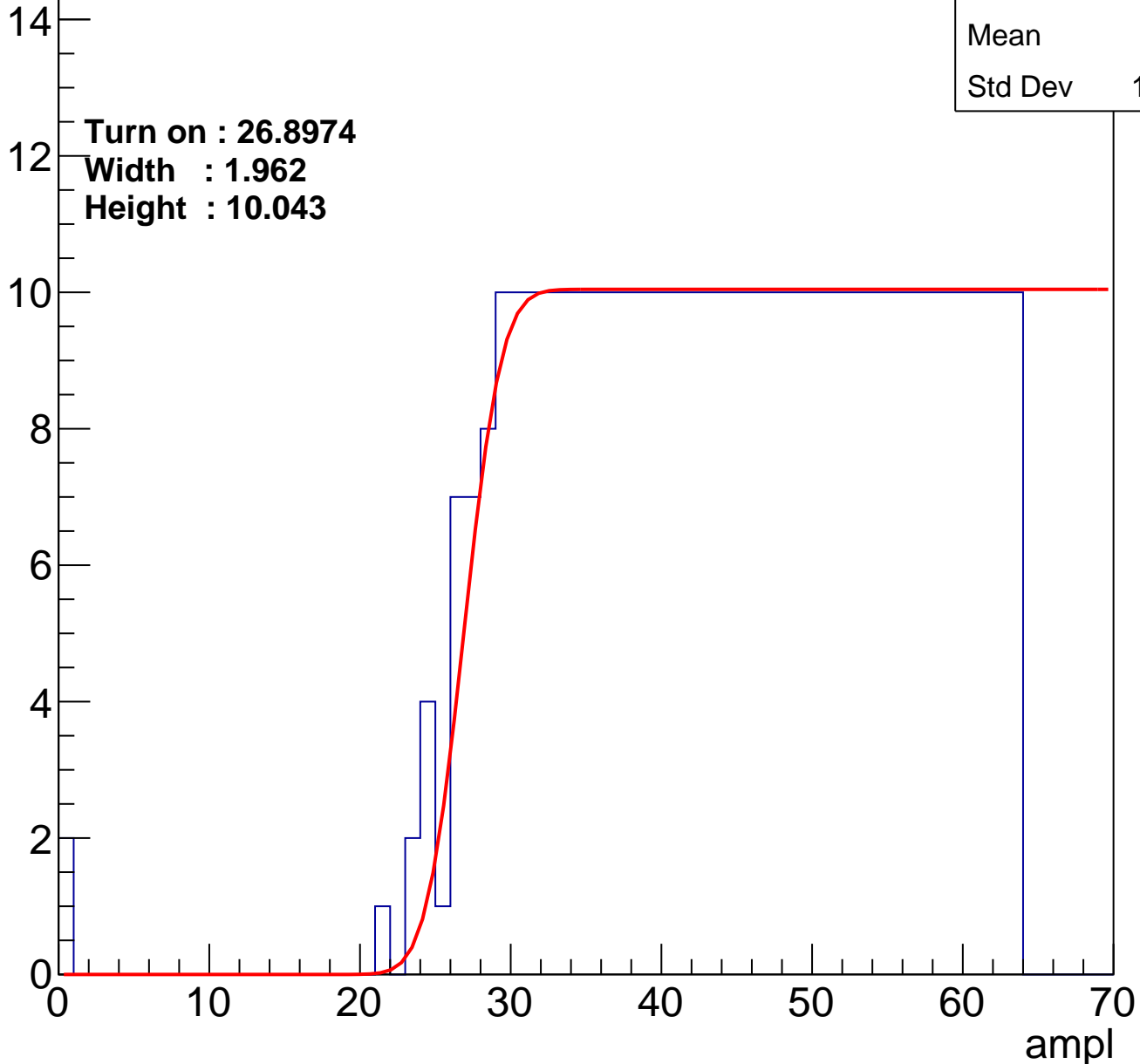
Entries	382
Mean	44.2
Std Dev	11.52

**Turn on : 26.8974**

**Width : 1.962**

**Height : 10.043**

Entry



# B1L000S, U7-ch114

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	385
Mean	43.87
Std Dev	12.01

**Turn on : 25.9749**

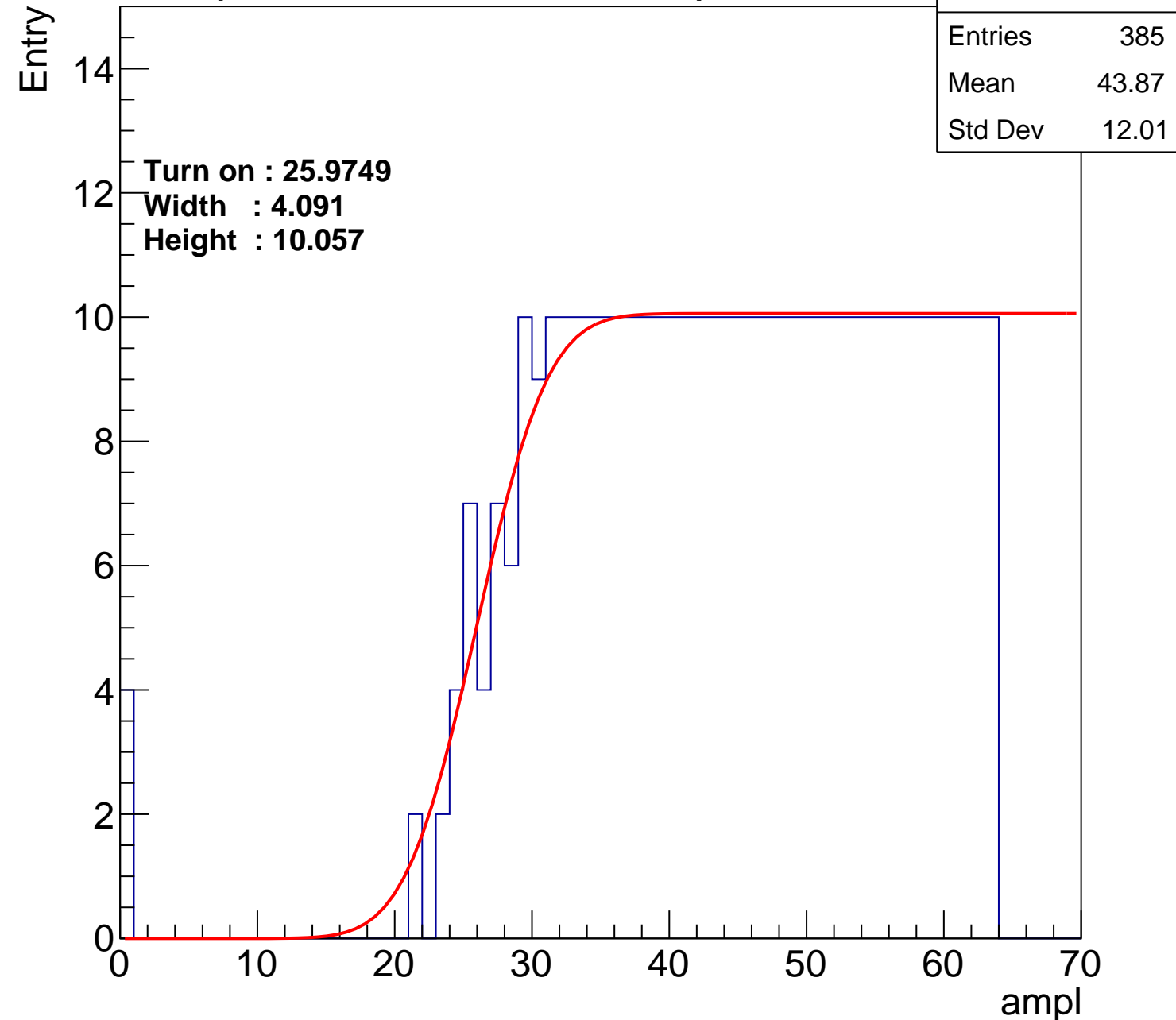
**Width : 4.091**

**Height : 10.057**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch115

calib\_packv5\_042523\_0143.root, FC#3, port B3

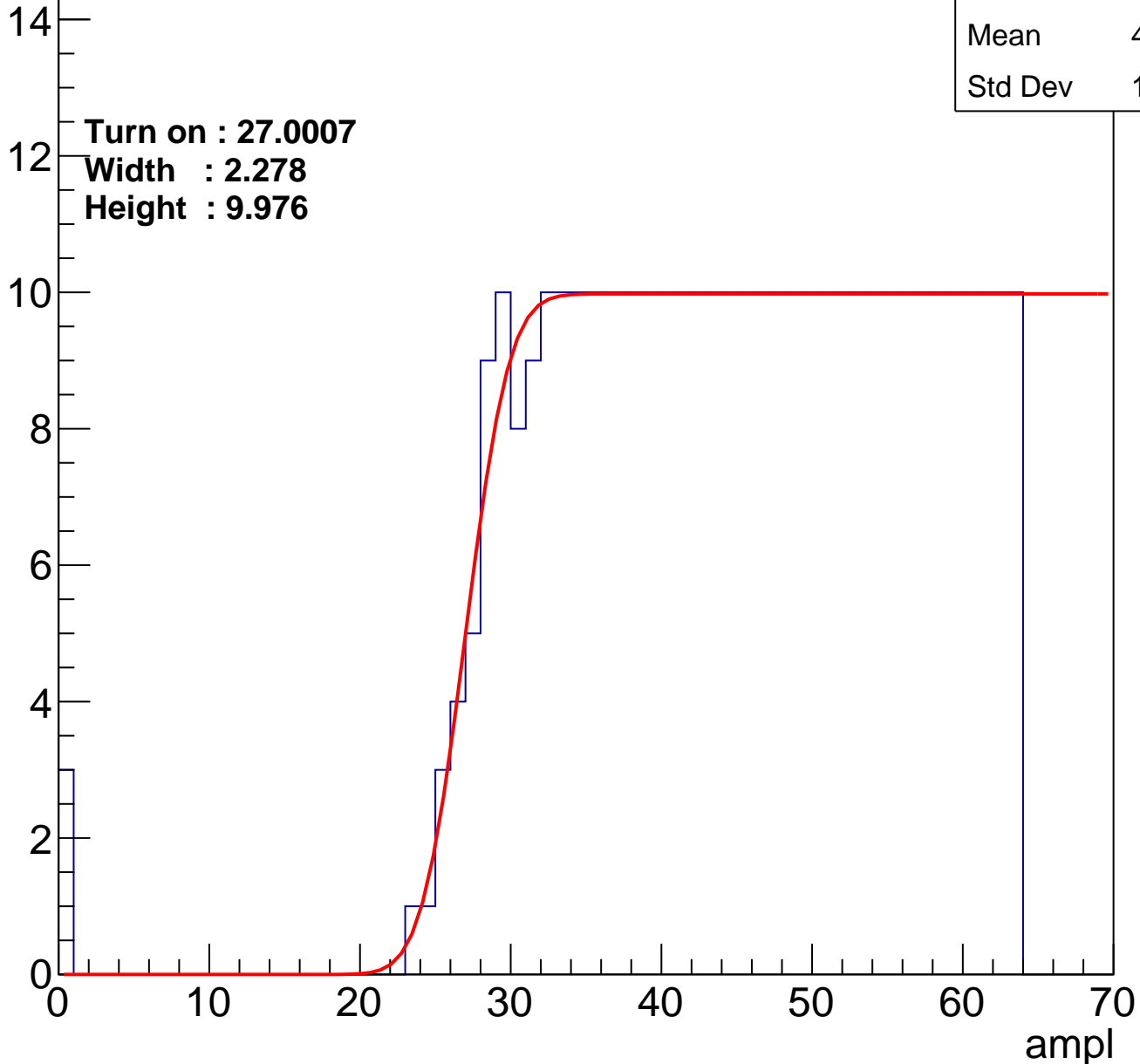
Entries	373
Mean	44.56
Std Dev	11.48

Turn on : 27.0007

Width : 2.278

Height : 9.976

Entry



**calib\_packv5\_042523\_0143.root, FC#3, port B3**

Entries	386
Mean	43.99
Std Dev	11.63

Mean	43.99
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Std Dev	11.63
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**Width : 2.821**

**Height : 10.004**



# B1L000S, U7-ch117

calib\_packv5\_042523\_0143.root, FC#3, port B3

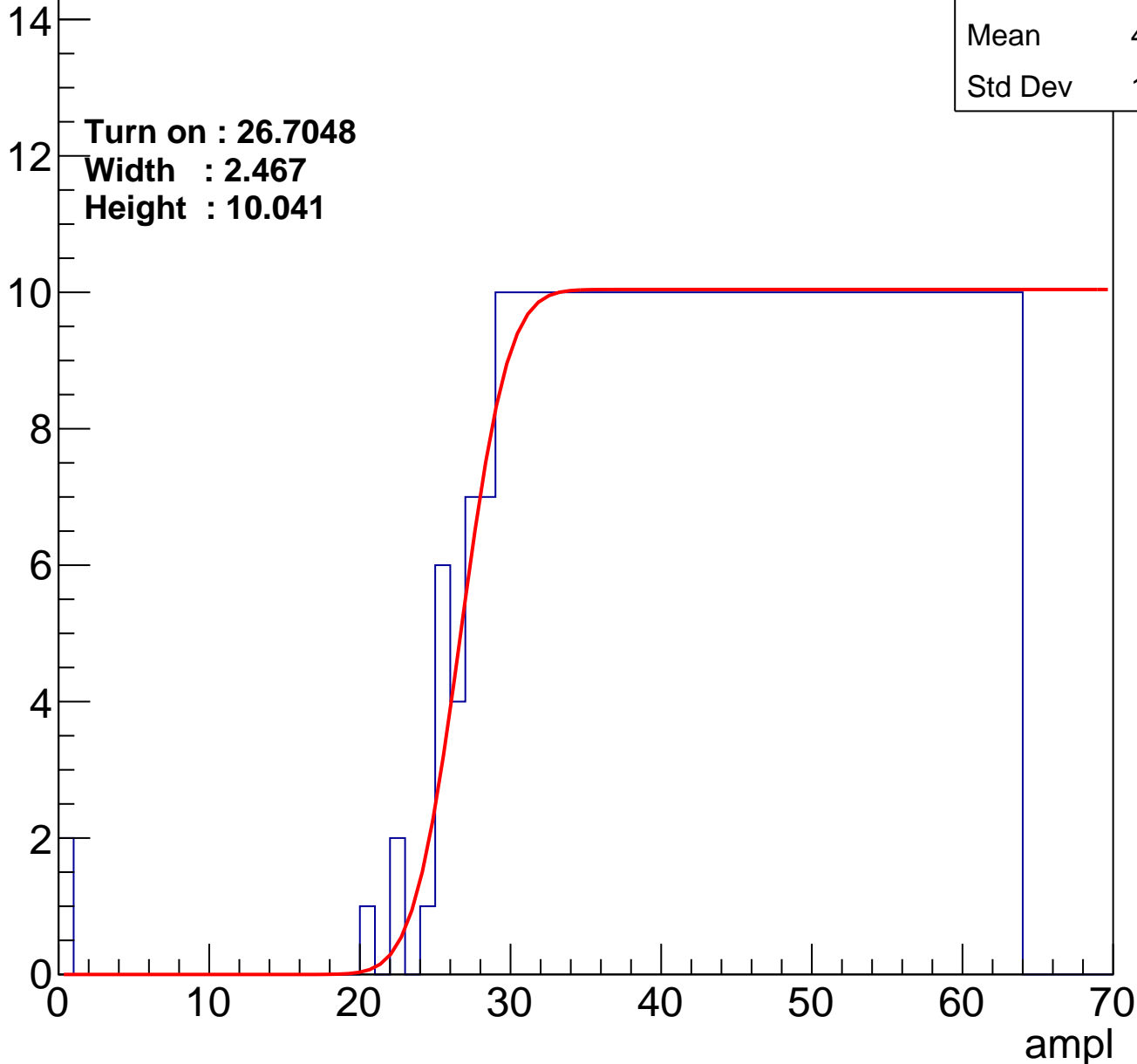
Entries	380
Mean	44.28
Std Dev	11.49

Turn on : 26.7048

Width : 2.467

Height : 10.041

Entry



# B1L000S, U7-ch118

calib\_packv5\_042523\_0143.root, FC#3, port B3

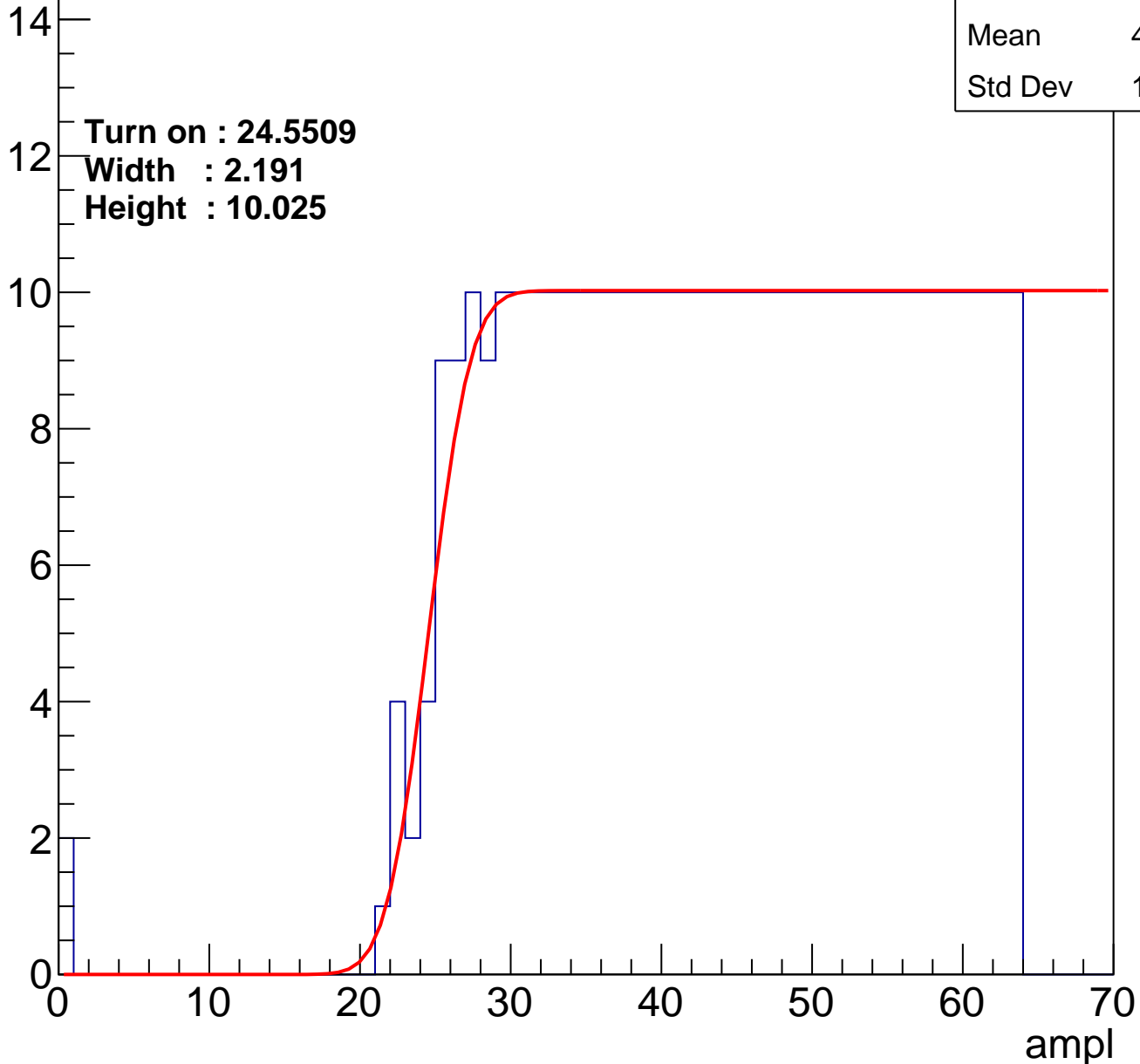
Entries	400
Mean	43.33
Std Dev	11.95

Turn on : 24.5509

Width : 2.191

Height : 10.025

Entry





# B1L000S, U7-ch119

calib\_packv5\_042523\_0143.root, FC#3, port B3

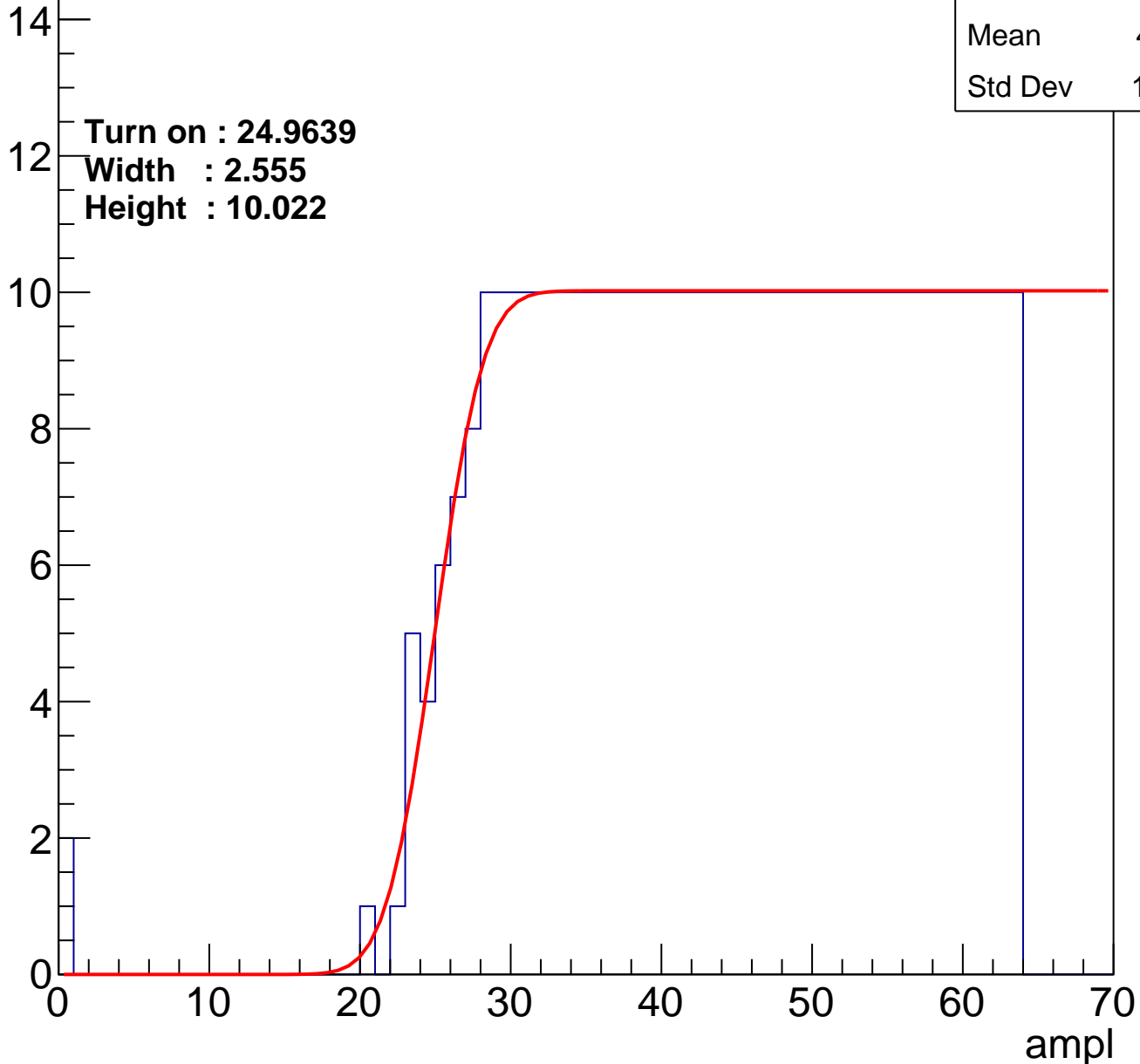
Entries	394
Mean	43.61
Std Dev	11.82

Turn on : 24.9639

Width : 2.555

Height : 10.022

Entry



# B1L000S, U7-ch120

calib\_packv5\_042523\_0143.root, FC#3, port B3

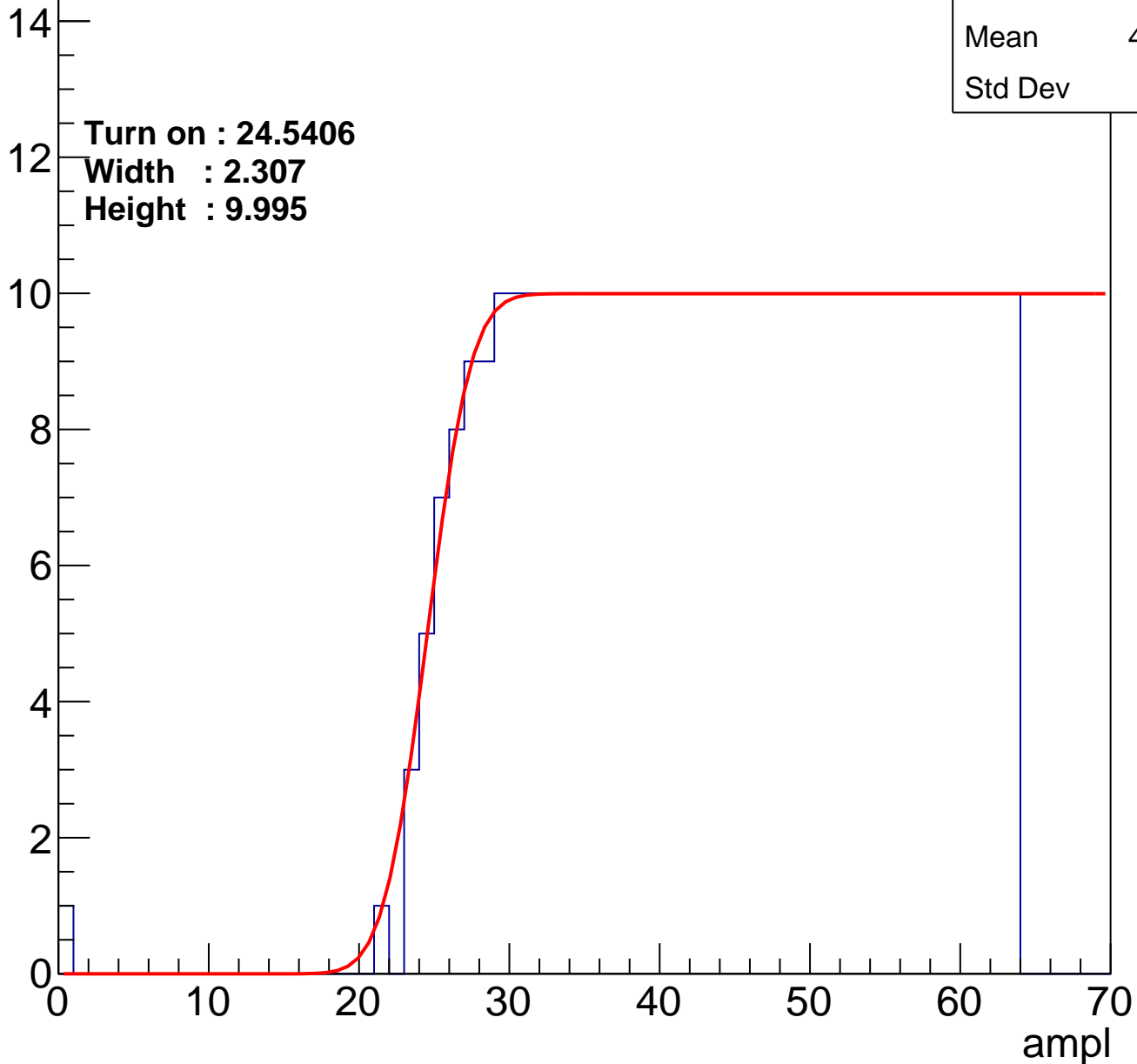
Entries	393
Mean	43.74
Std Dev	11.6

Turn on : 24.5406

Width : 2.307

Height : 9.995

Entry



# B1L000S, U7-ch121

calib\_packv5\_042523\_0143.root, FC#3, port B3

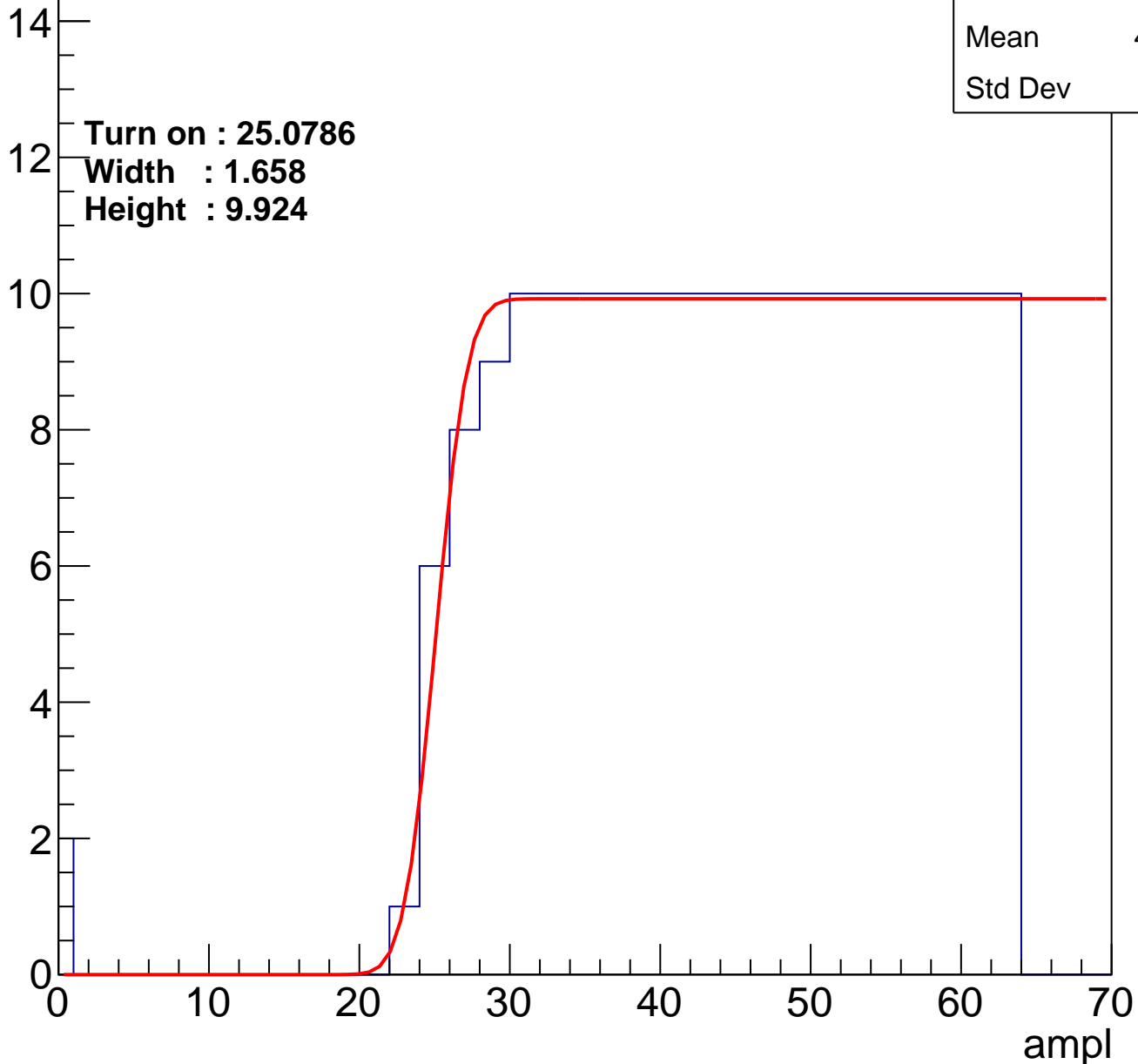
Entries	390
Mean	43.81
Std Dev	11.7

Turn on : 25.0786

Width : 1.658

Height : 9.924

Entry



# B1L000S, U7-ch122

calib\_packv5\_042523\_0143.root, FC#3, port B3

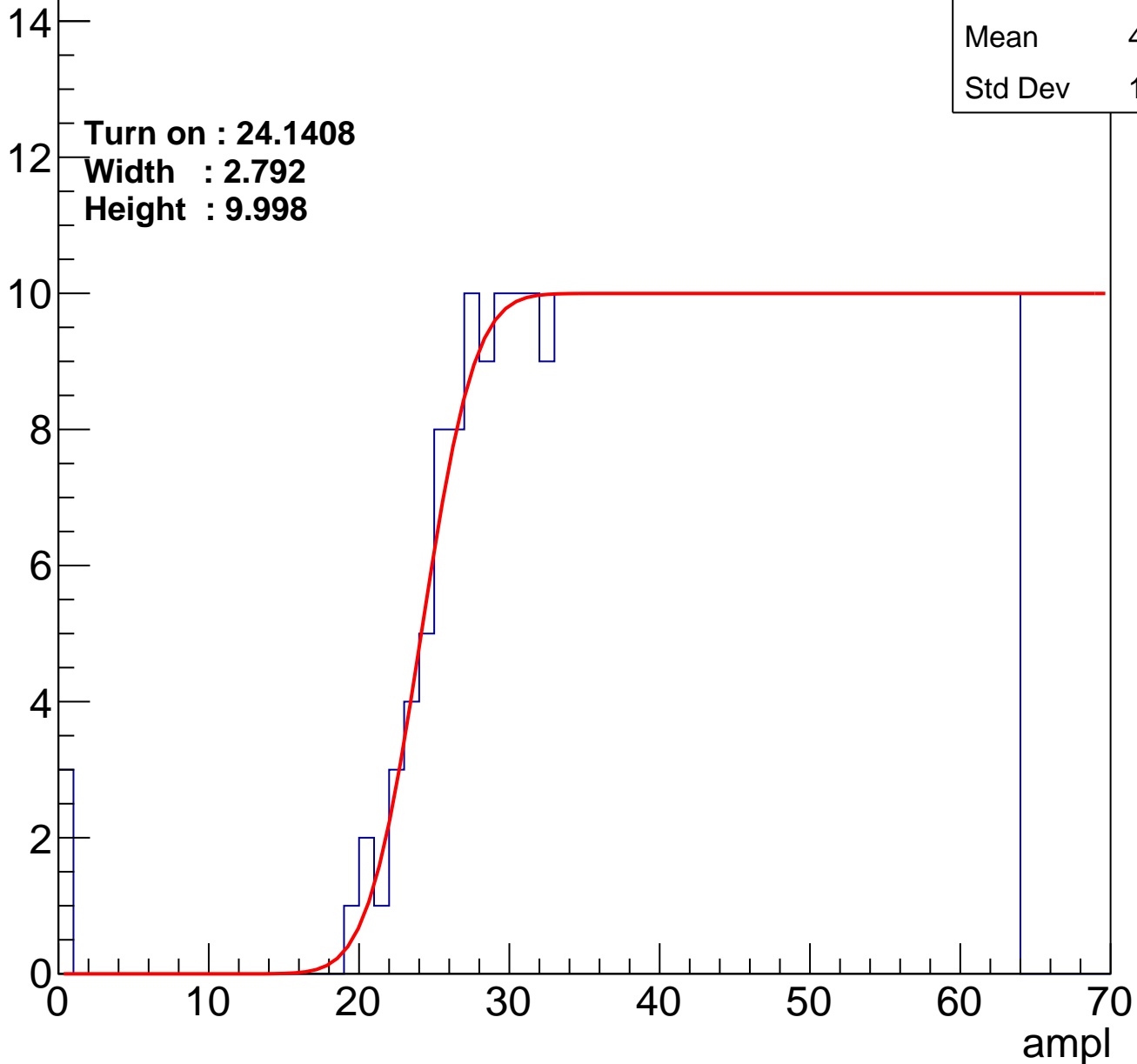
Entries	403
Mean	43.07
Std Dev	12.26

Turn on : 24.1408

Width : 2.792

Height : 9.998

Entry



# B1L000S, U7-ch123

calib\_packv5\_042523\_0143.root, FC#3, port B3

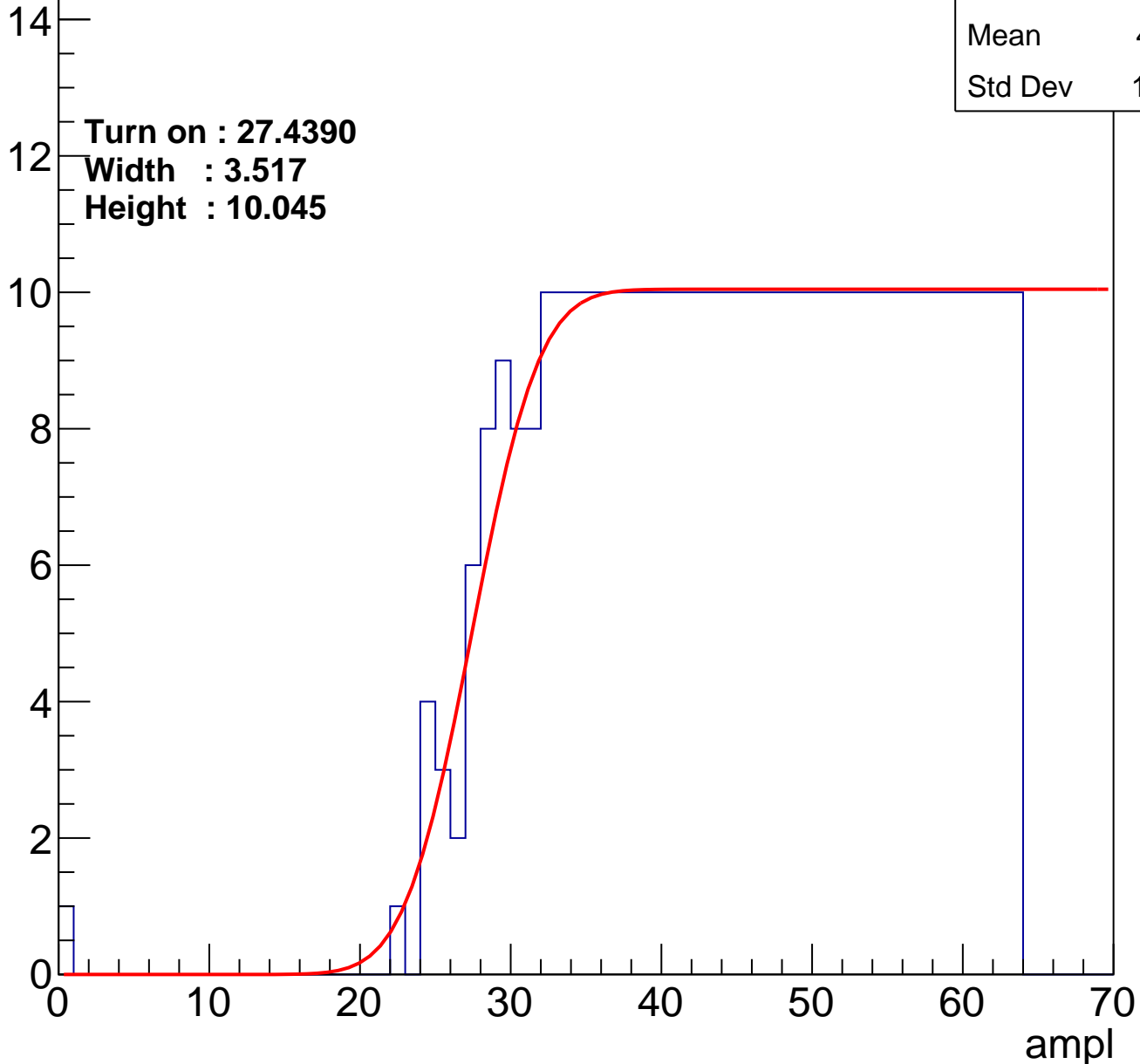
Entries	370
Mean	44.81
Std Dev	11.08

Turn on : 27.4390

Width : 3.517

Height : 10.045

Entry



# B1L000S, U7-ch124

**calib\_packv5\_042523\_0143.root, FC#3, port B3**

Entries	384
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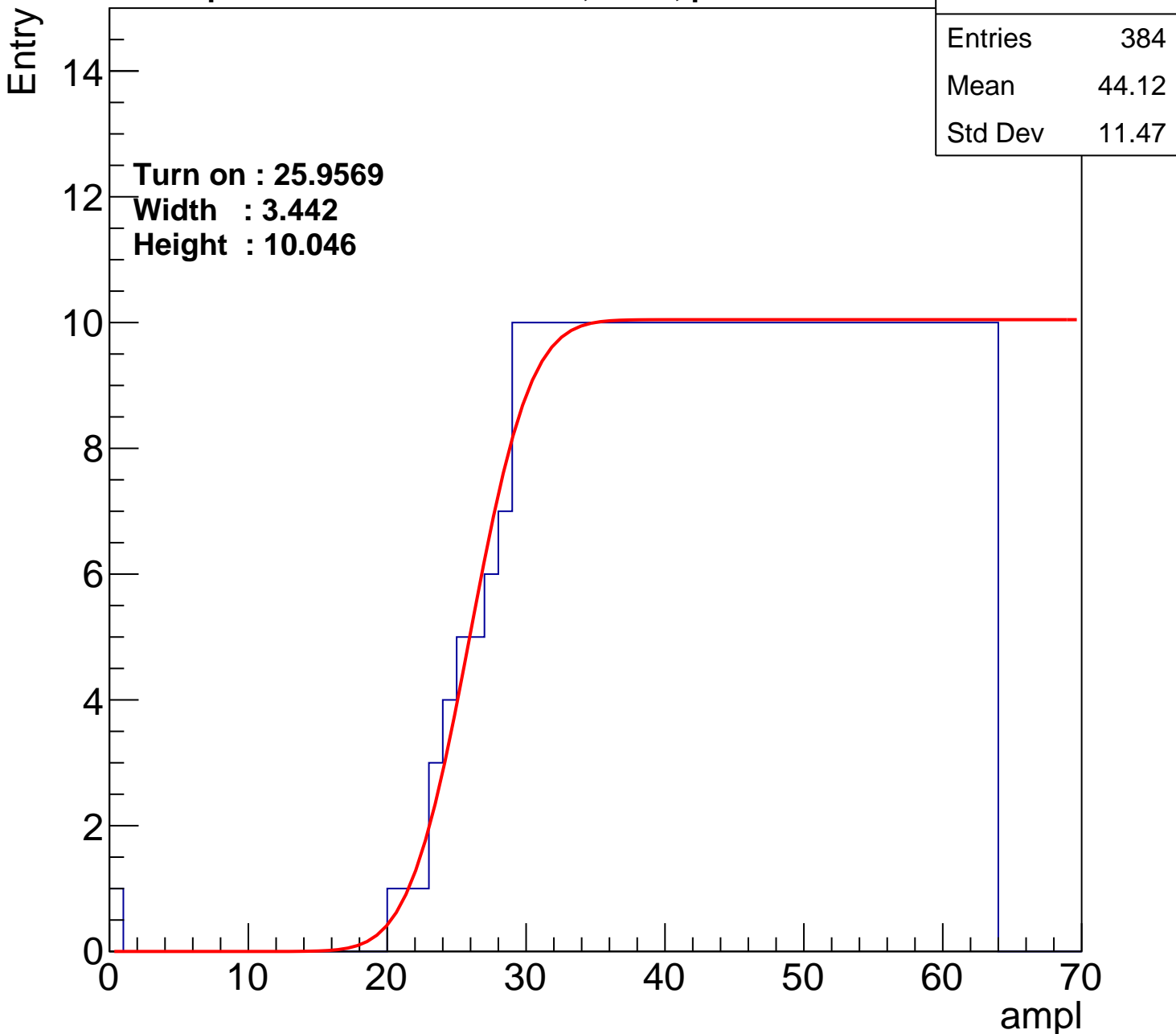
Mean	44.12
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Std Dev	11.47
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**Turn on : 25.9569**

**Width : 3.442**

**Height : 10.046**



# B1L000S, U7-ch125

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	372
Mean	44.61
Std Dev	11.48

**Turn on : 27.5338**

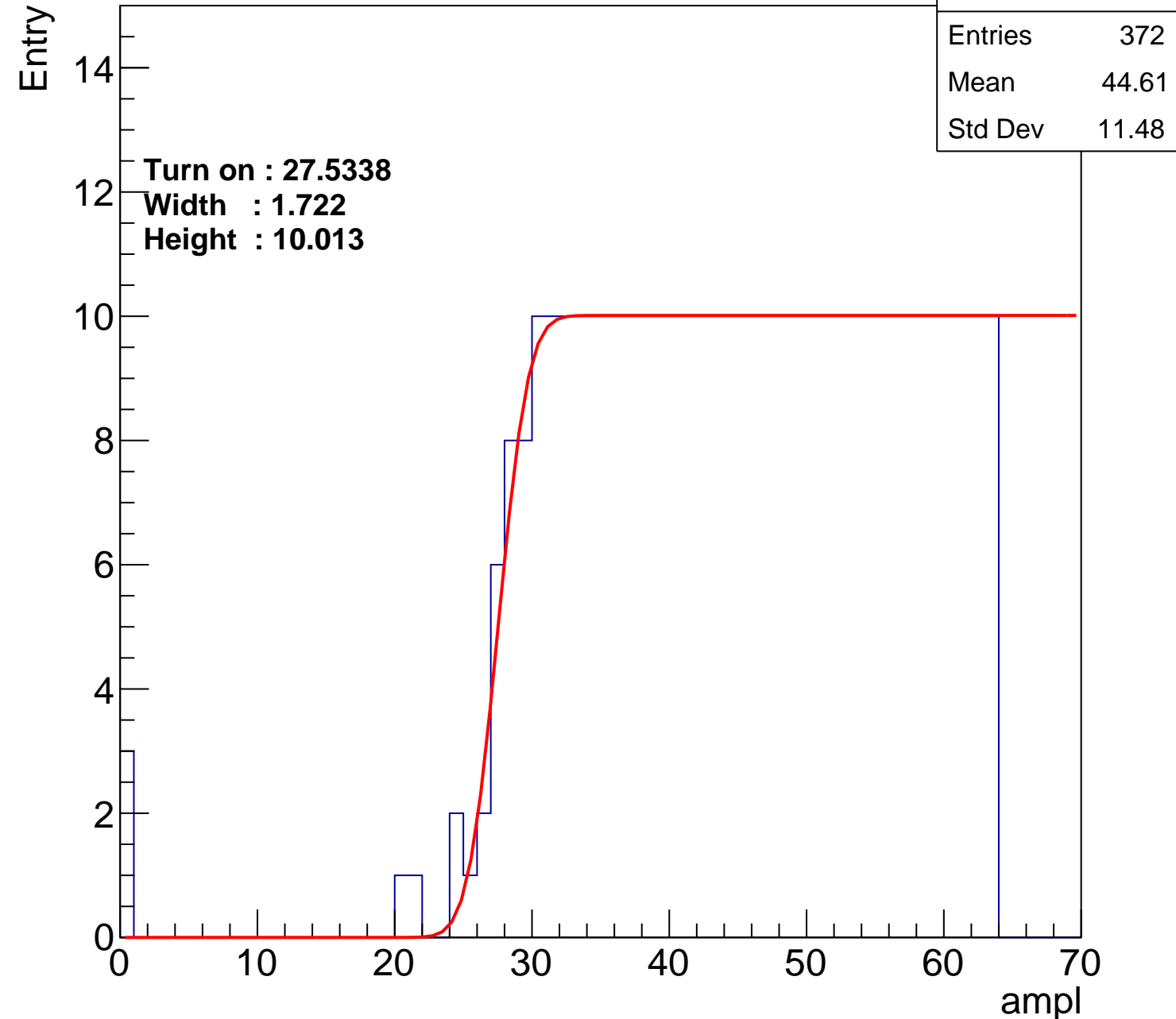
**Width : 1.722**

**Height : 10.013**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch126

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	383
Mean	44.22
Std Dev	11.35

**Turn on : 25.8759**

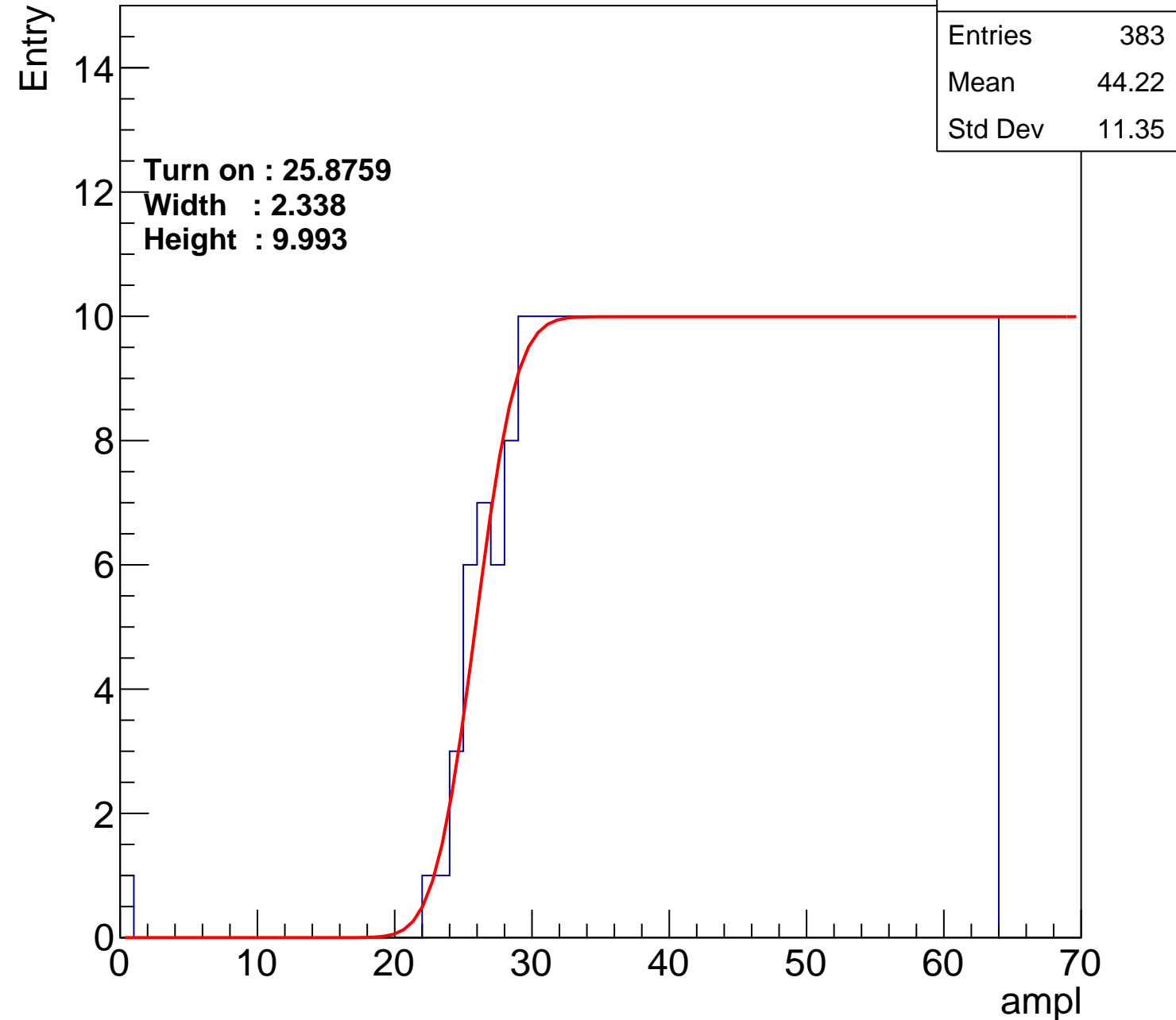
**Width : 2.338**

**Height : 9.993**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L000S, U7-ch127

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	367
Mean	44.98
Std Dev	10.98

**Turn on : 27.8703**

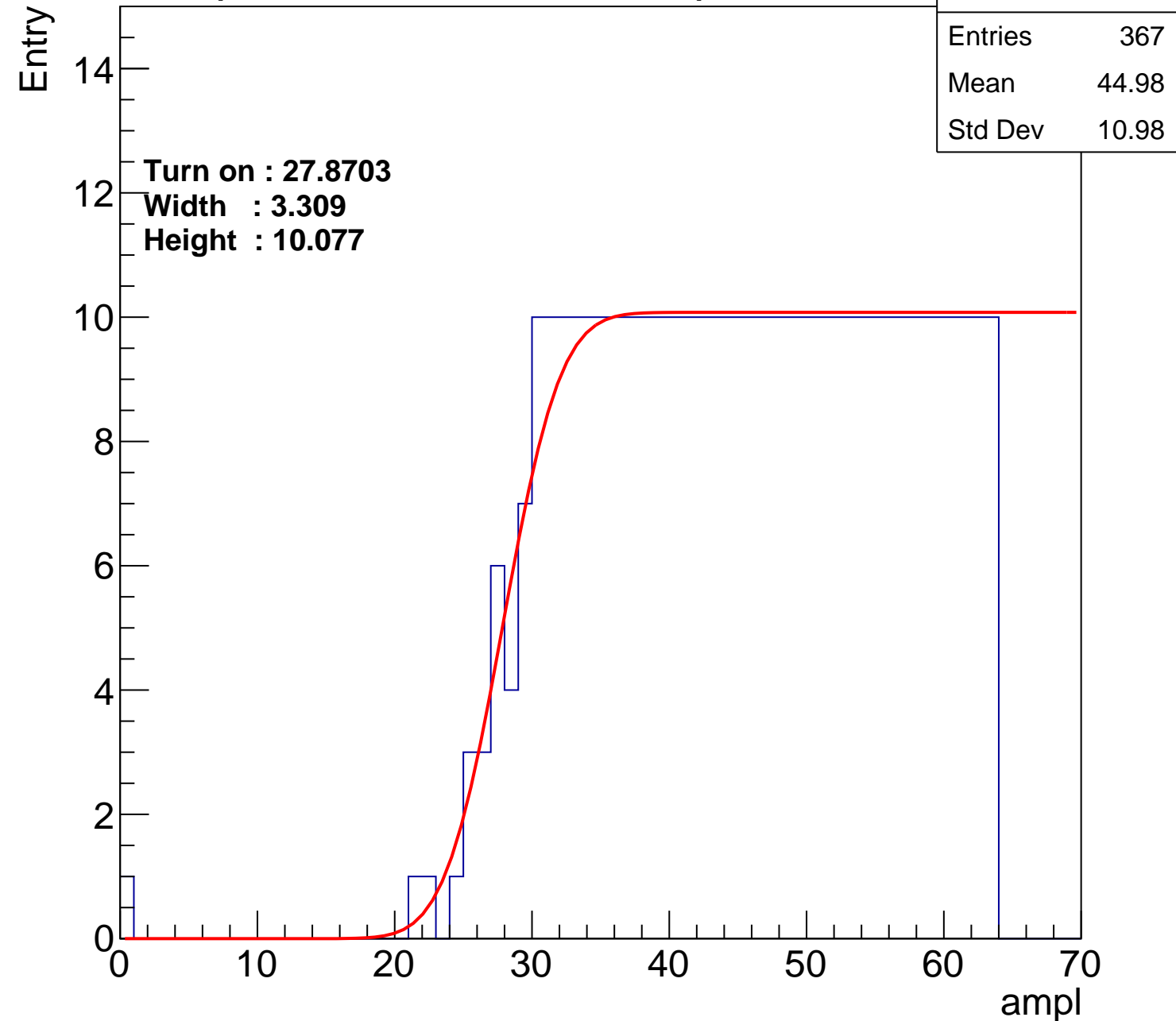
**Width : 3.309**

**Height : 10.077**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U7-ch127

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entry

Entries	367
Mean	44.98
Std Dev	10.98

Turn on : 27.8703

Width : 3.309

Height : 10.077

