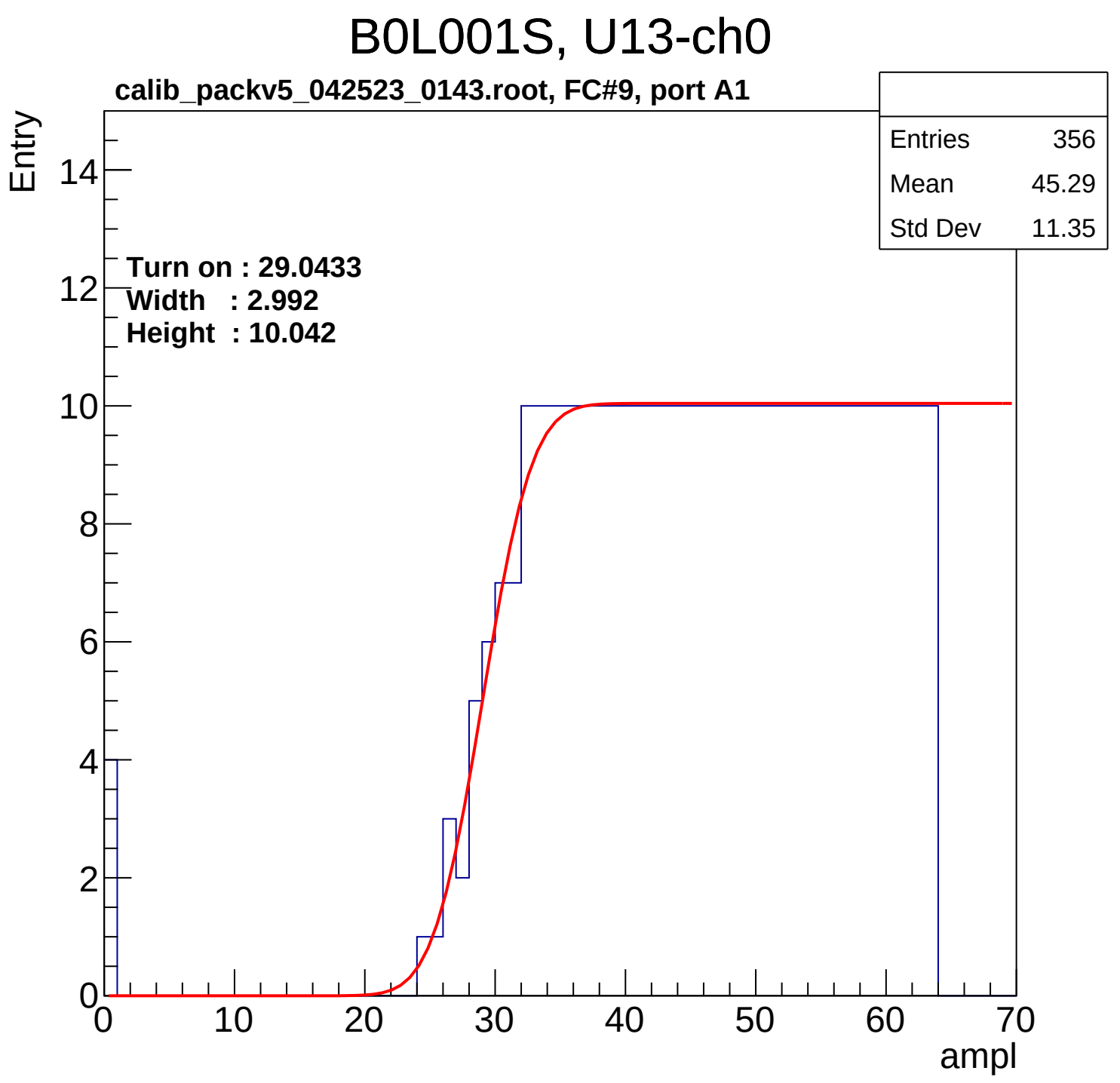
B0L001S, U13-ch0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 356
Mean 45.29
Std Dev 11.35
Turn on : 29.0433
Width : 2.992
Height : 10.042
Entry
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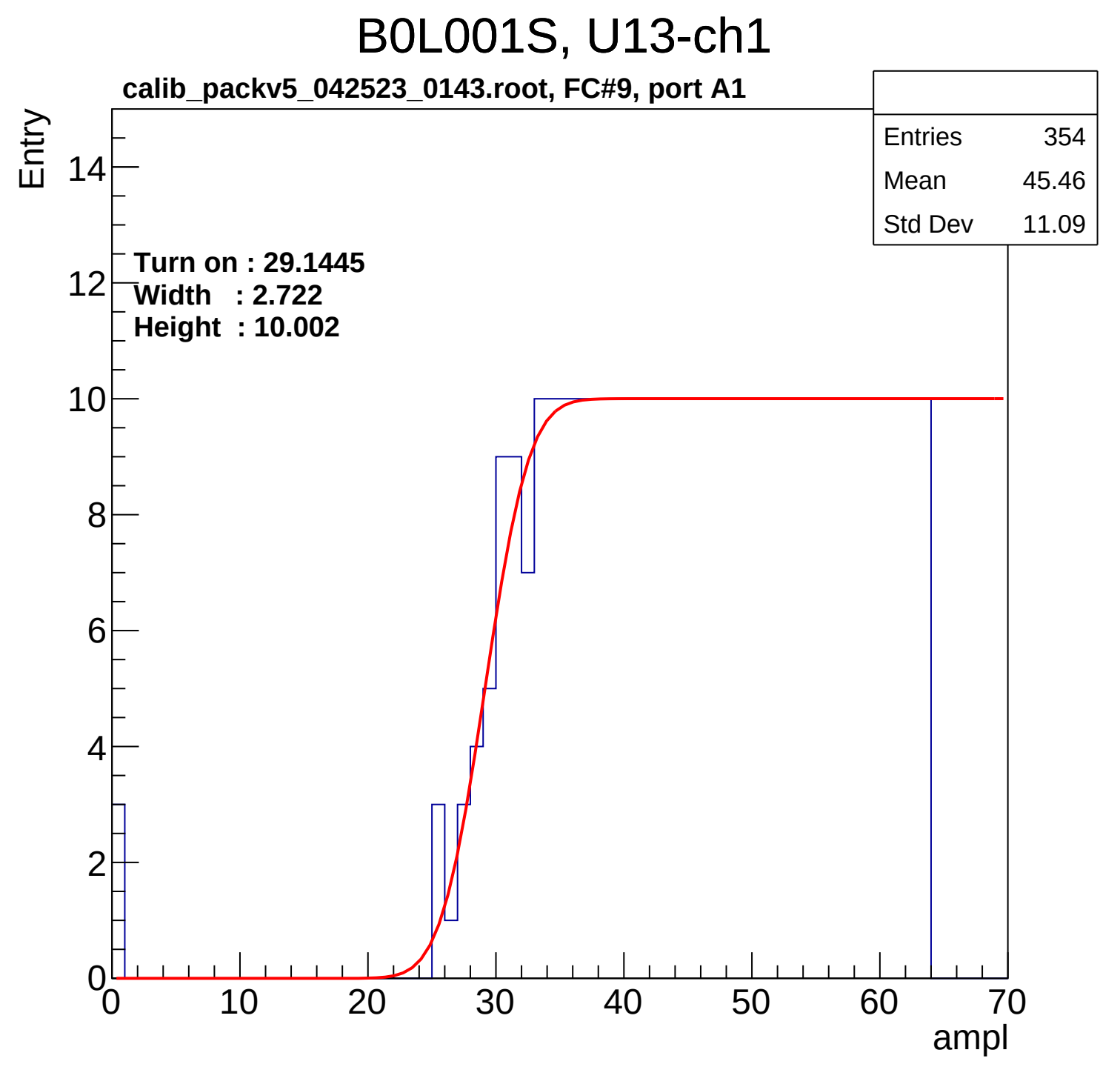
B0L001S, U13-ch1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 354
Mean 45.46
Std Dev 11.09
Turn on : 29.1445
Width : 2.722
Height : 10.002
Entry
ampl
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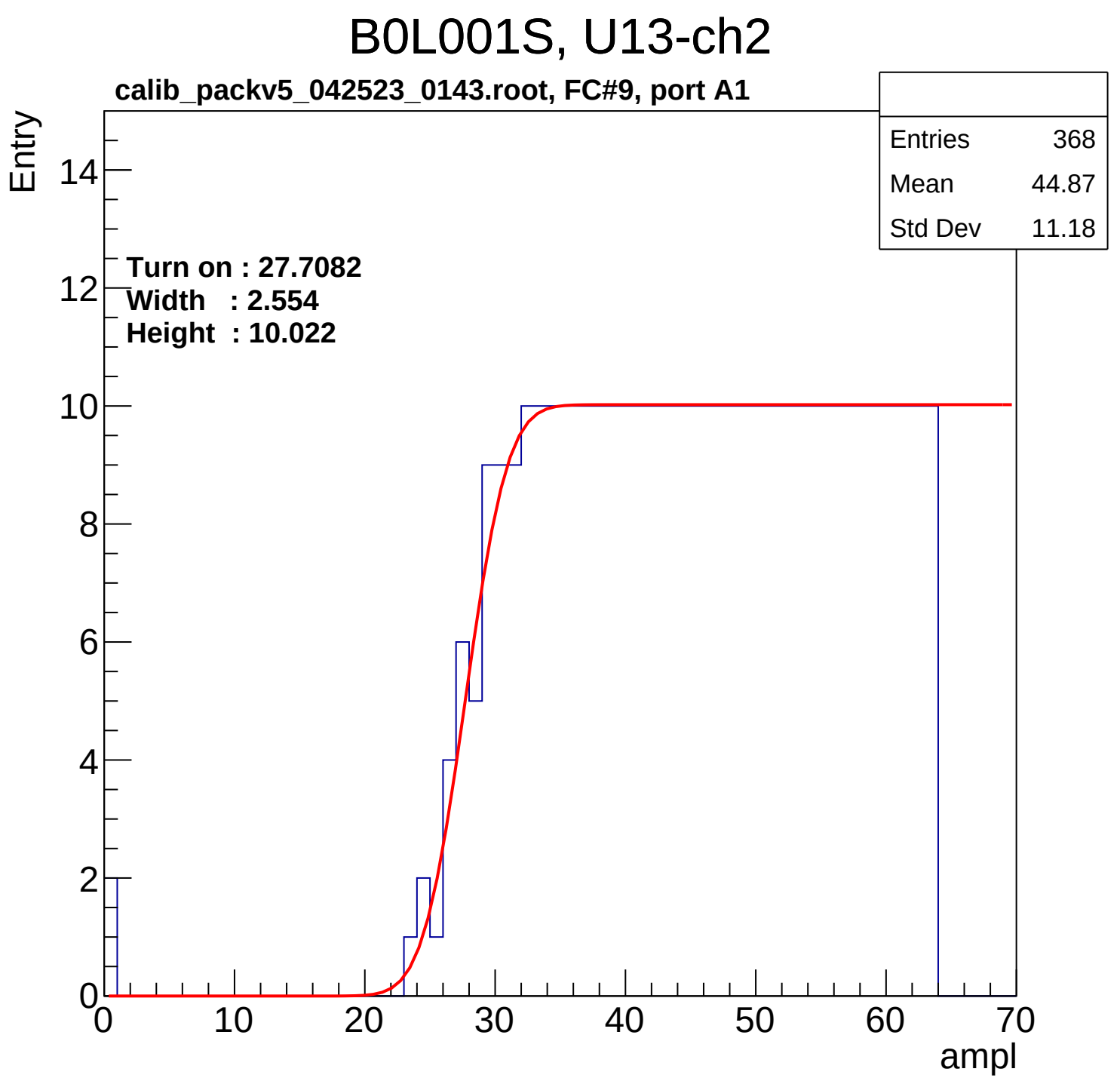
B0L001S, U13-ch2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.87
Std Dev 11.18
Turn on : 27.7082
Width : 2.554
Height : 10.022
Entry
ampl
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4
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8
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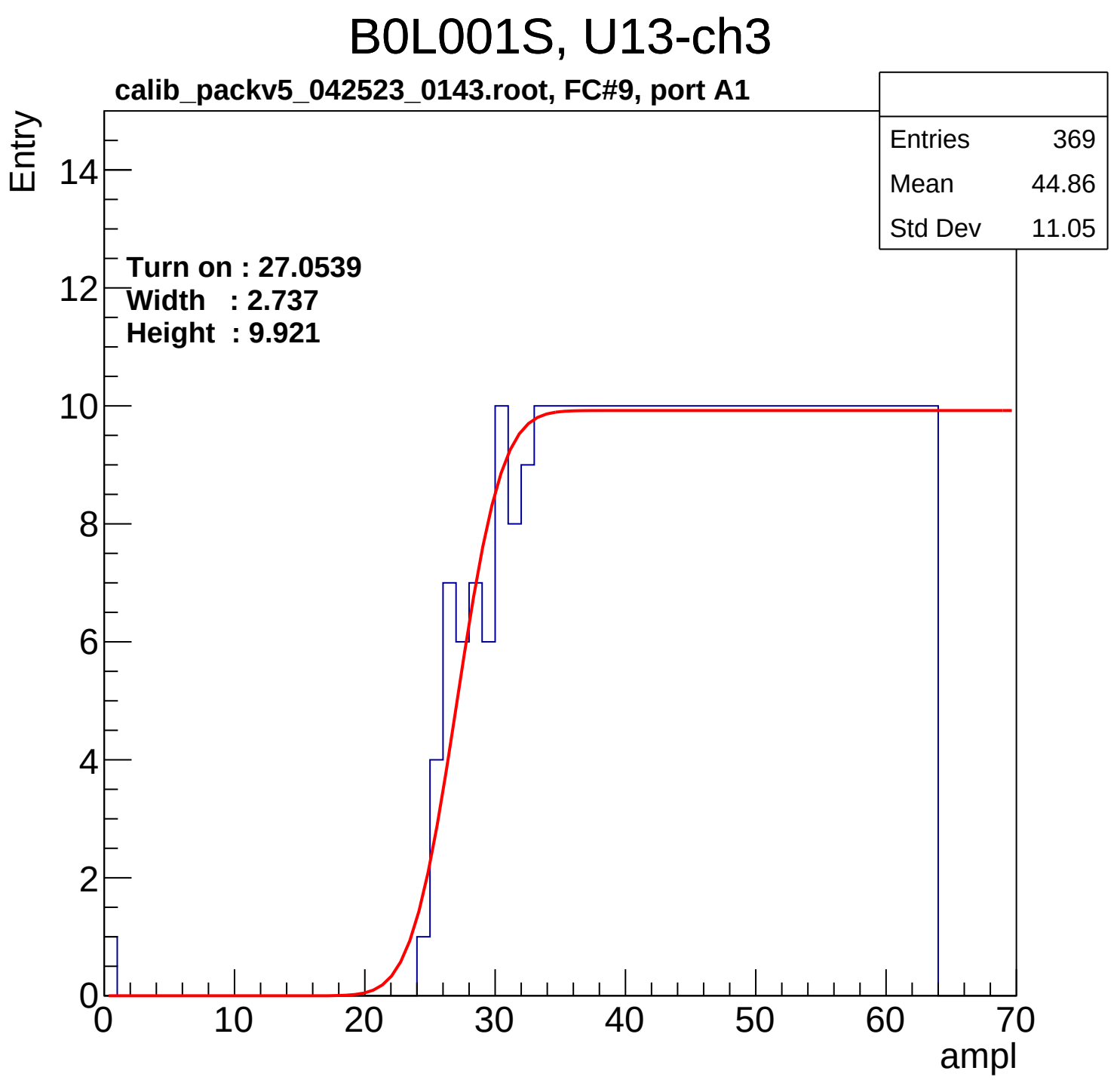
B0L001S, U13-ch3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.86
Std Dev 11.05
Turn on : 27.0539
Width : 2.737
Height : 9.921
Entry
ampl
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2
4
6
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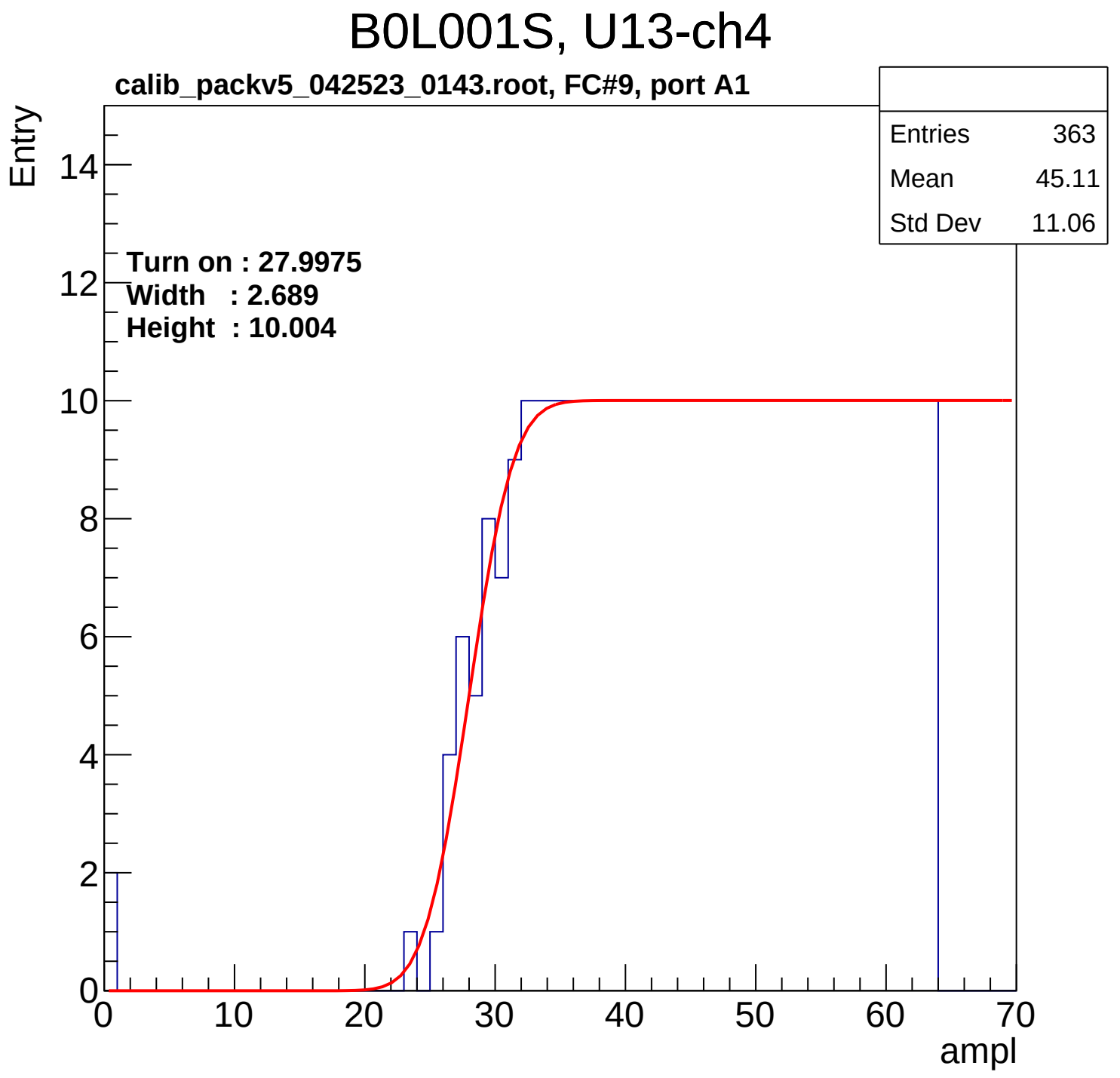
B0L001S, U13-ch4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 45.11
Std Dev 11.06
Turn on : 27.9975
Width : 2.689
Height : 10.004
Entry
ampl
0
2
4
6
8
10
12
14
0
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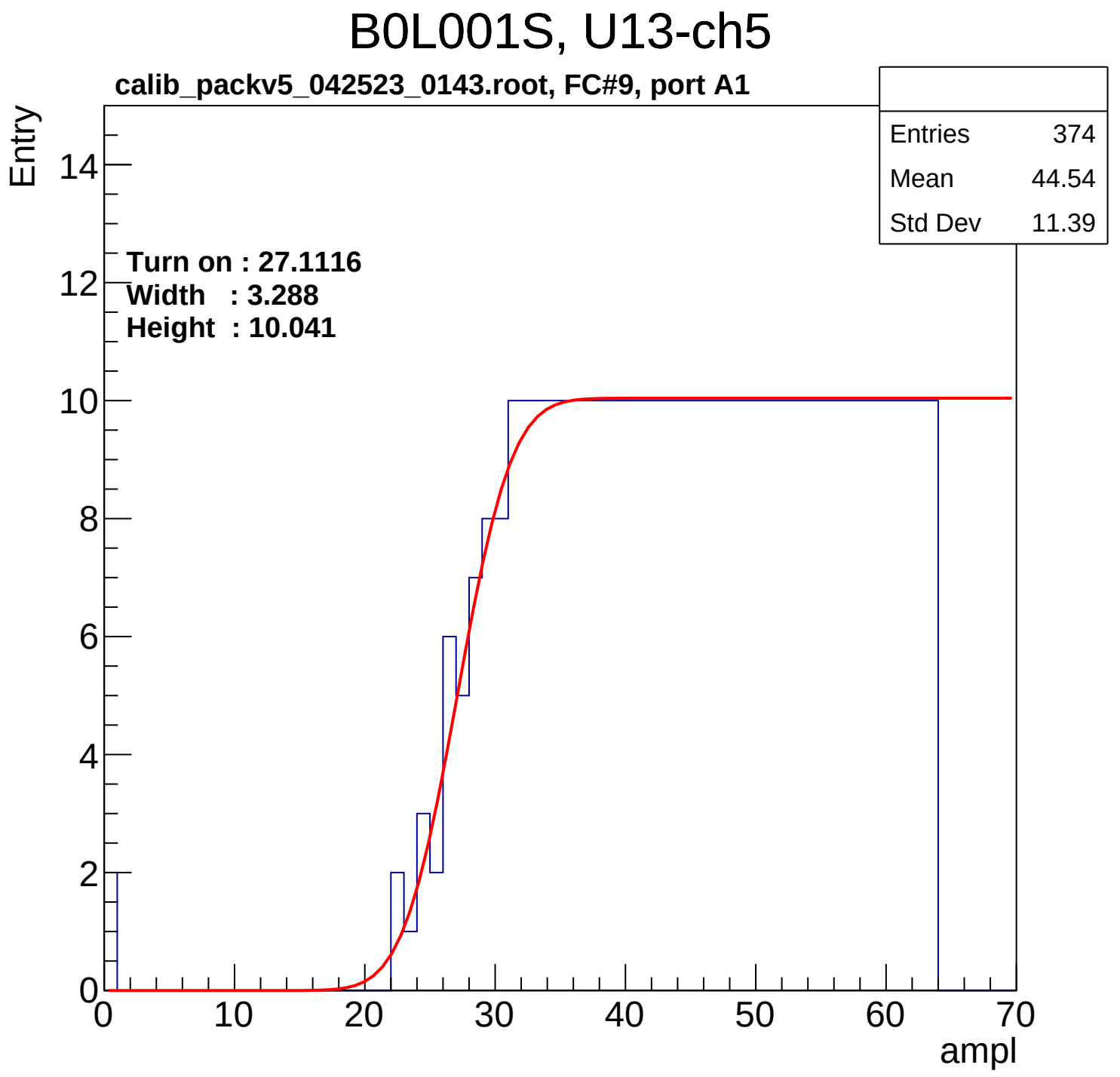
B0L001S, U13-ch5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 374
Mean 44.54
Std Dev 11.39
Turn on : 27.1116
Width : 3.288
Height : 10.041
Entry
ampl
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2
4
6
8
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0
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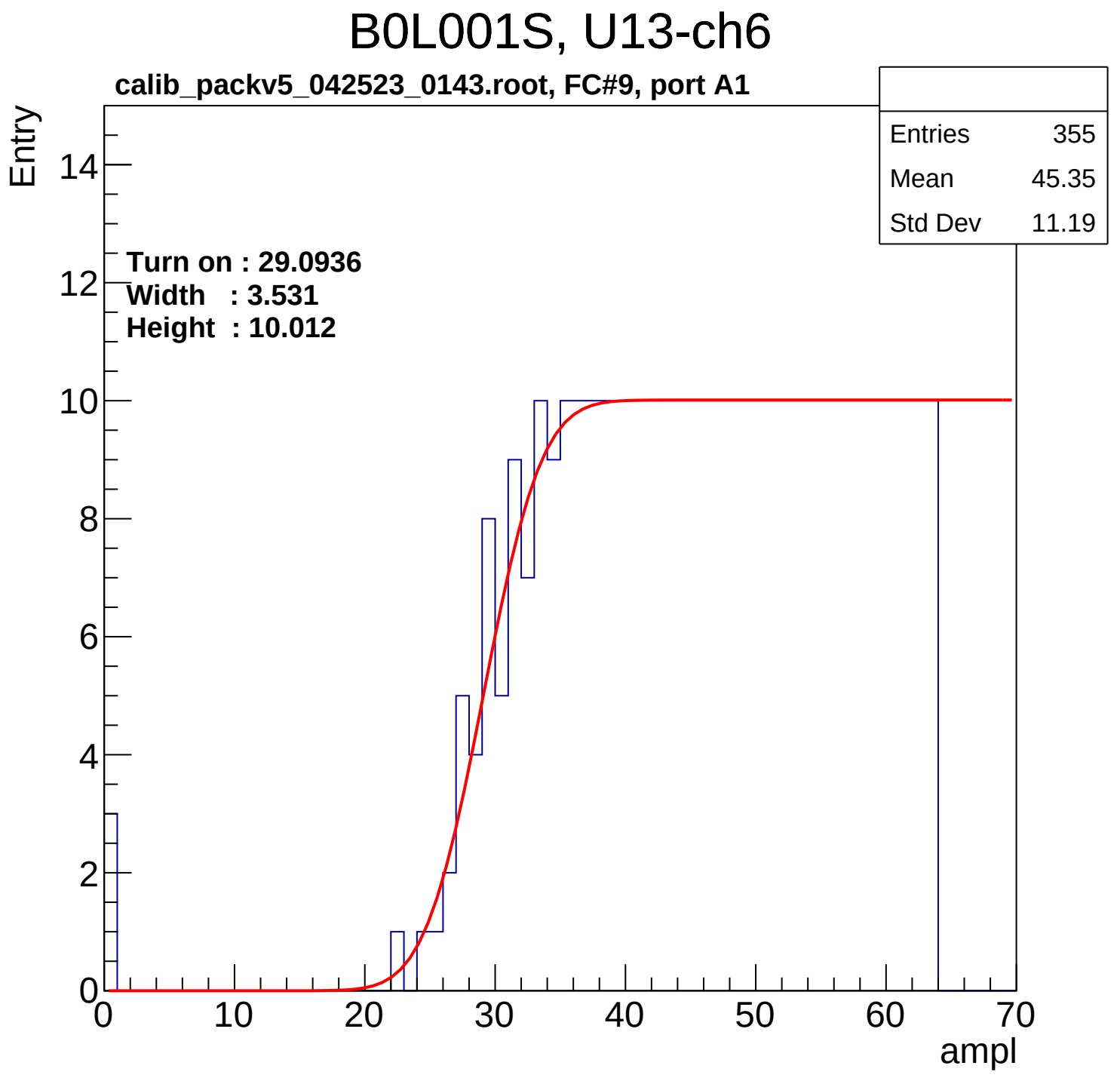
B0L001S, U13-ch6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 355
Mean 45.35
Std Dev 11.19
Turn on : 29.0936
Width : 3.531
Height : 10.012
Entry
ampl
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2
4
6
8
10
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0
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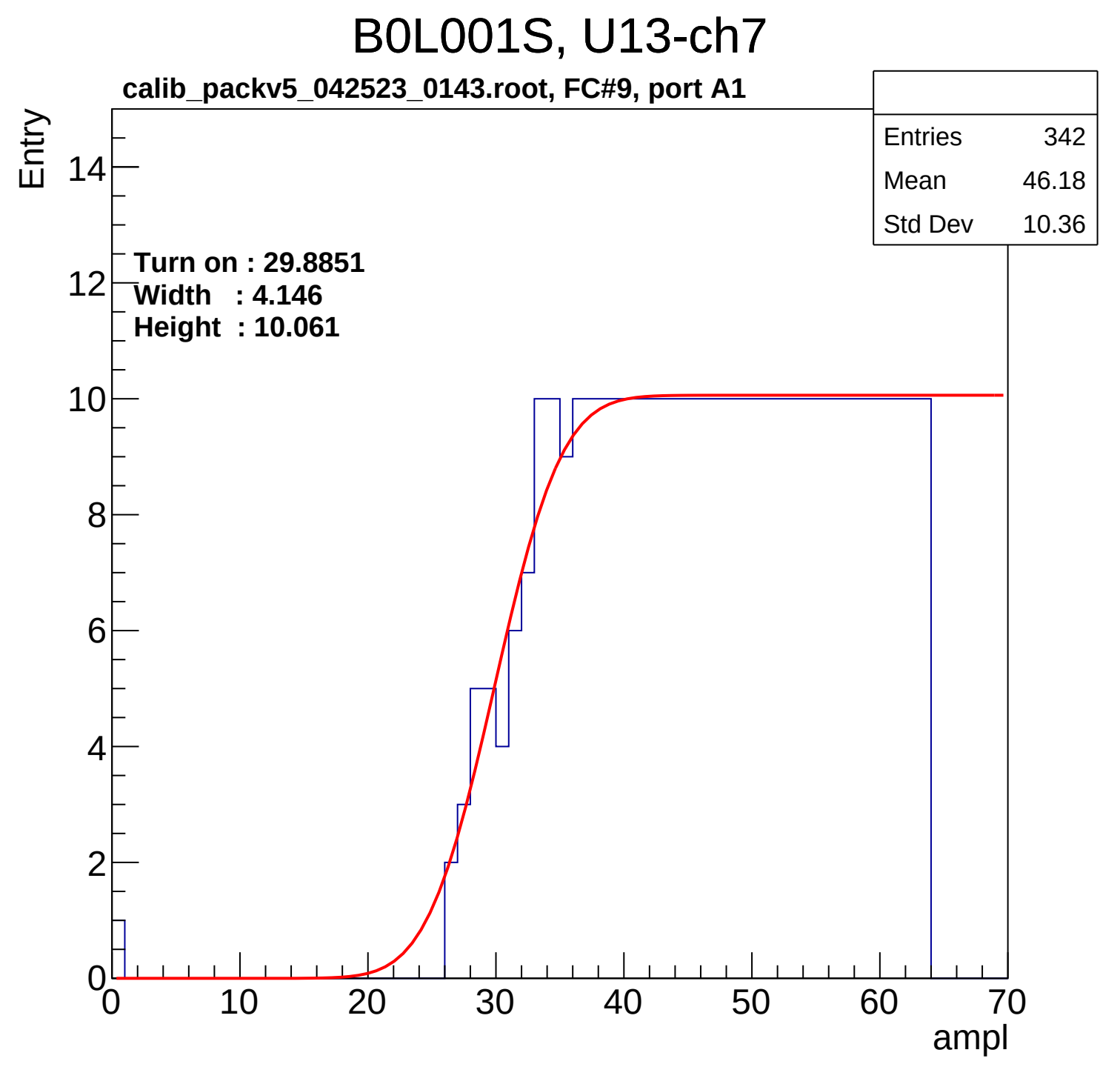
B0L001S, U13-ch7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 342
Mean 46.18
Std Dev 10.36
Turn on : 29.8851
Width : 4.146
Height : 10.061
Entry
ampl
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4
6
8
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12
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0
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60
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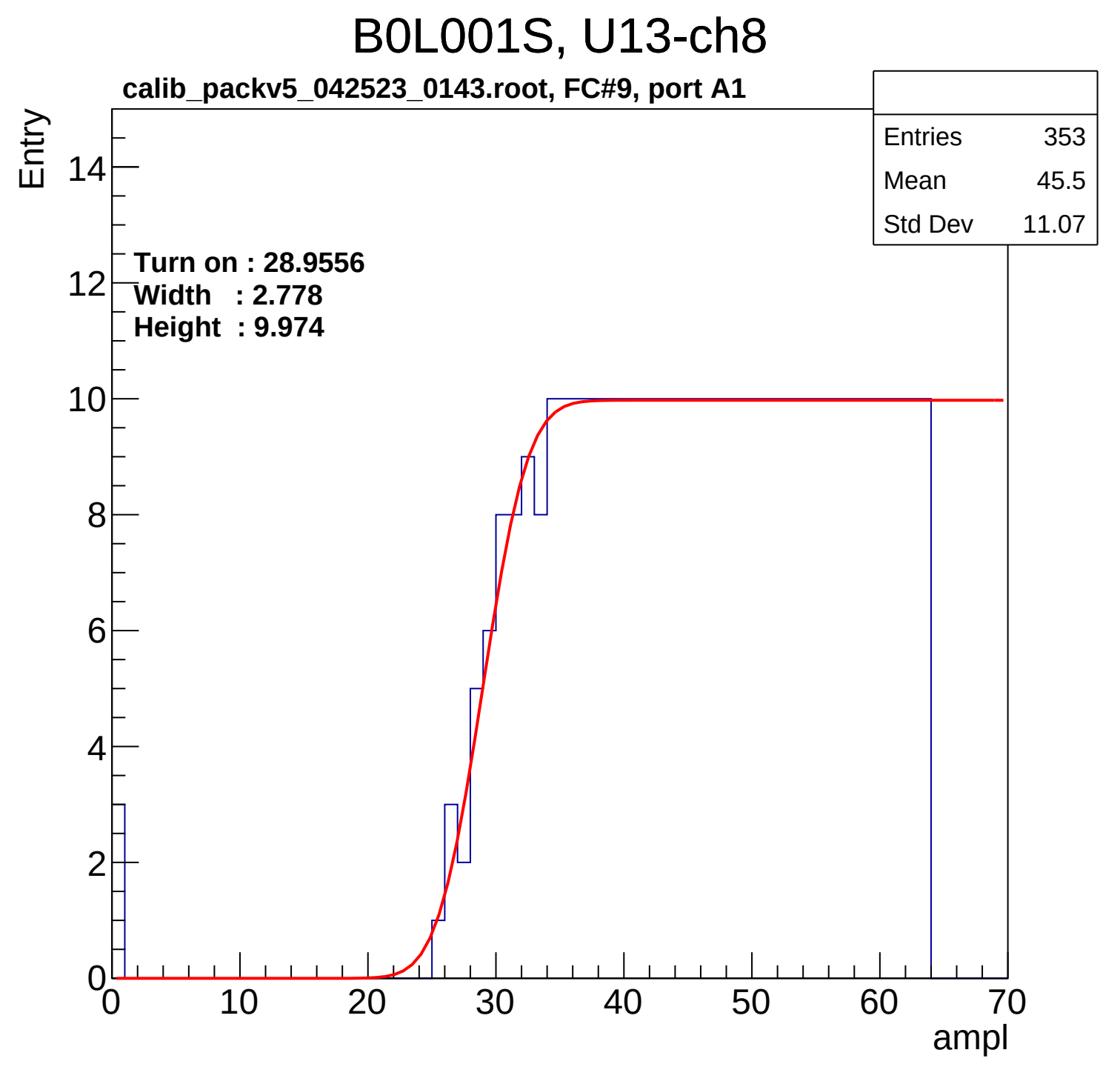
B0L001S, U13-ch8
calib_packv5_042523_0143.root, FC#9, port A1
Entries 353
Mean 45.5
Std Dev 11.07
Turn on : 28.9556
Width : 2.778
Height : 9.974
Entry
ampl
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4
6
8
10
12
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0
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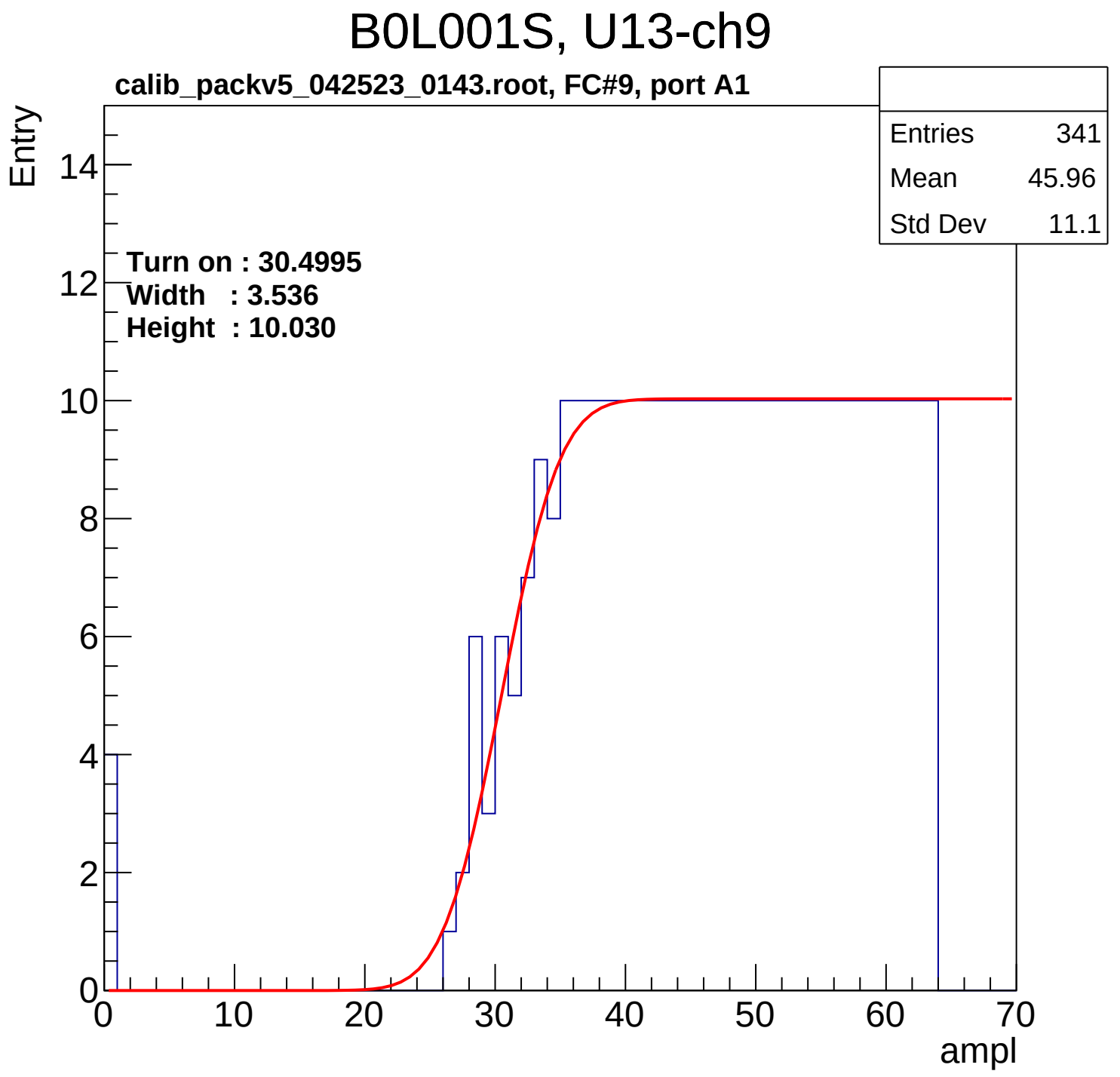
B0L001S, U13-ch9
calib_packv5_042523_0143.root, FC#9, port A1
Entries 341
Mean 45.96
Std Dev 11.1
Turn on : 30.4995
Width : 3.536
Height : 10.030
Entry
ampl
0
2
4
6
8
10
12
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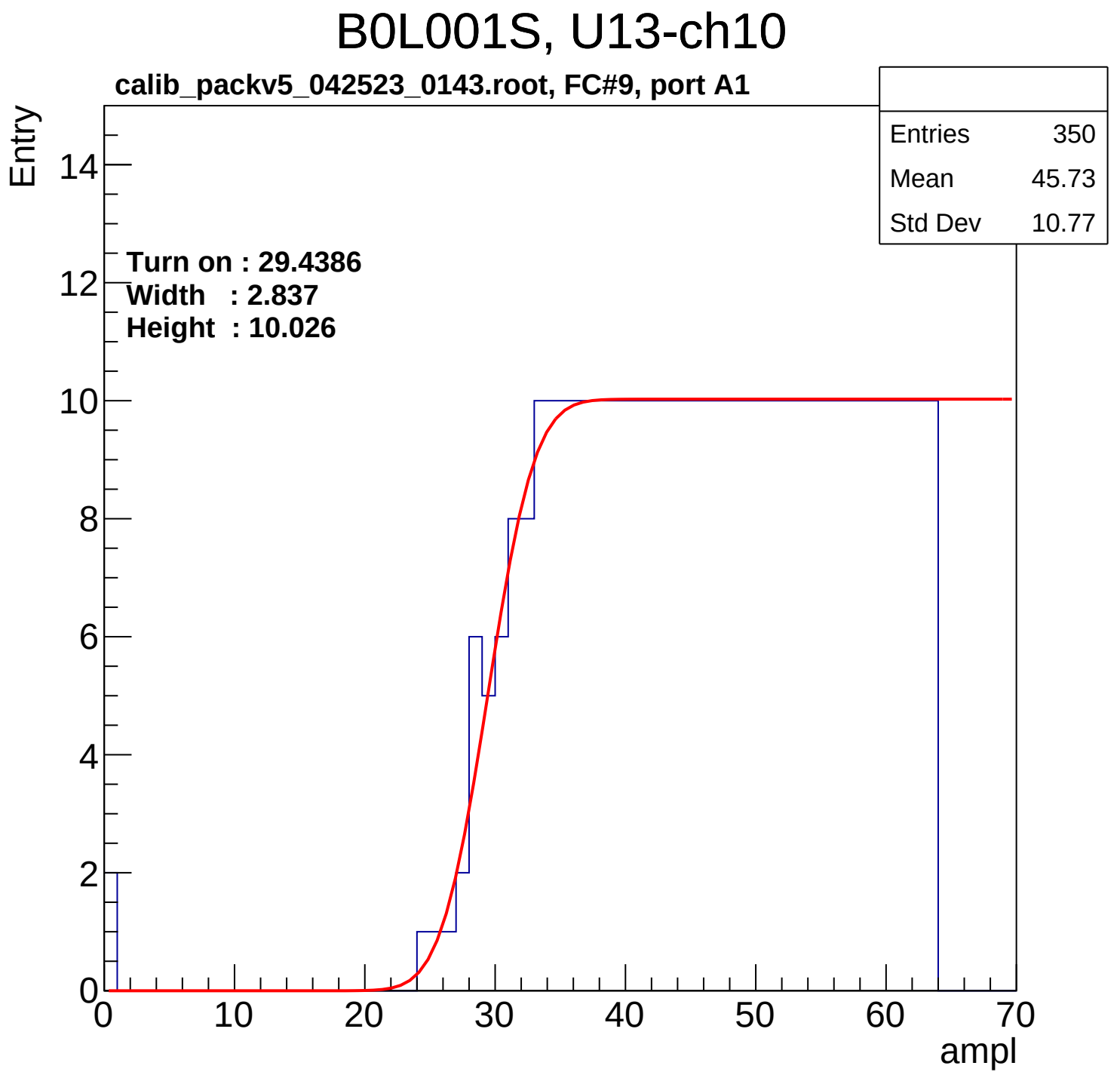
B0L001S, U13-ch10
calib_packv5_042523_0143.root, FC#9, port A1
Entries 350
Mean 45.73
Std Dev 10.77
Turn on : 29.4386
Width : 2.837
Height : 10.026
Entry
ampl
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2
4
6
8
10
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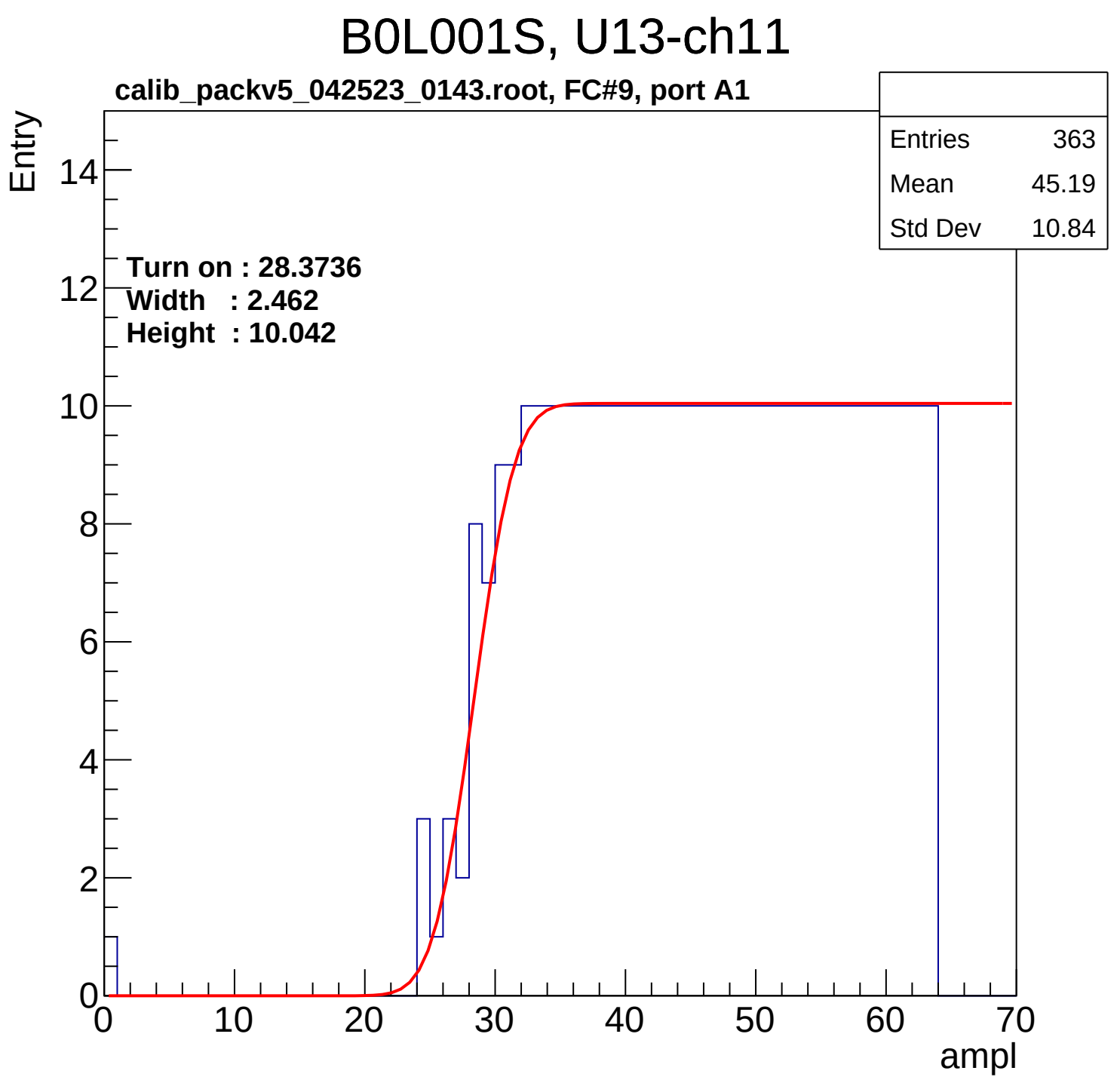
B0L001S, U13-ch11
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 45.19
Std Dev 10.84
Turn on : 28.3736
Width : 2.462
Height : 10.042
Entry
ampl
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4
6
8
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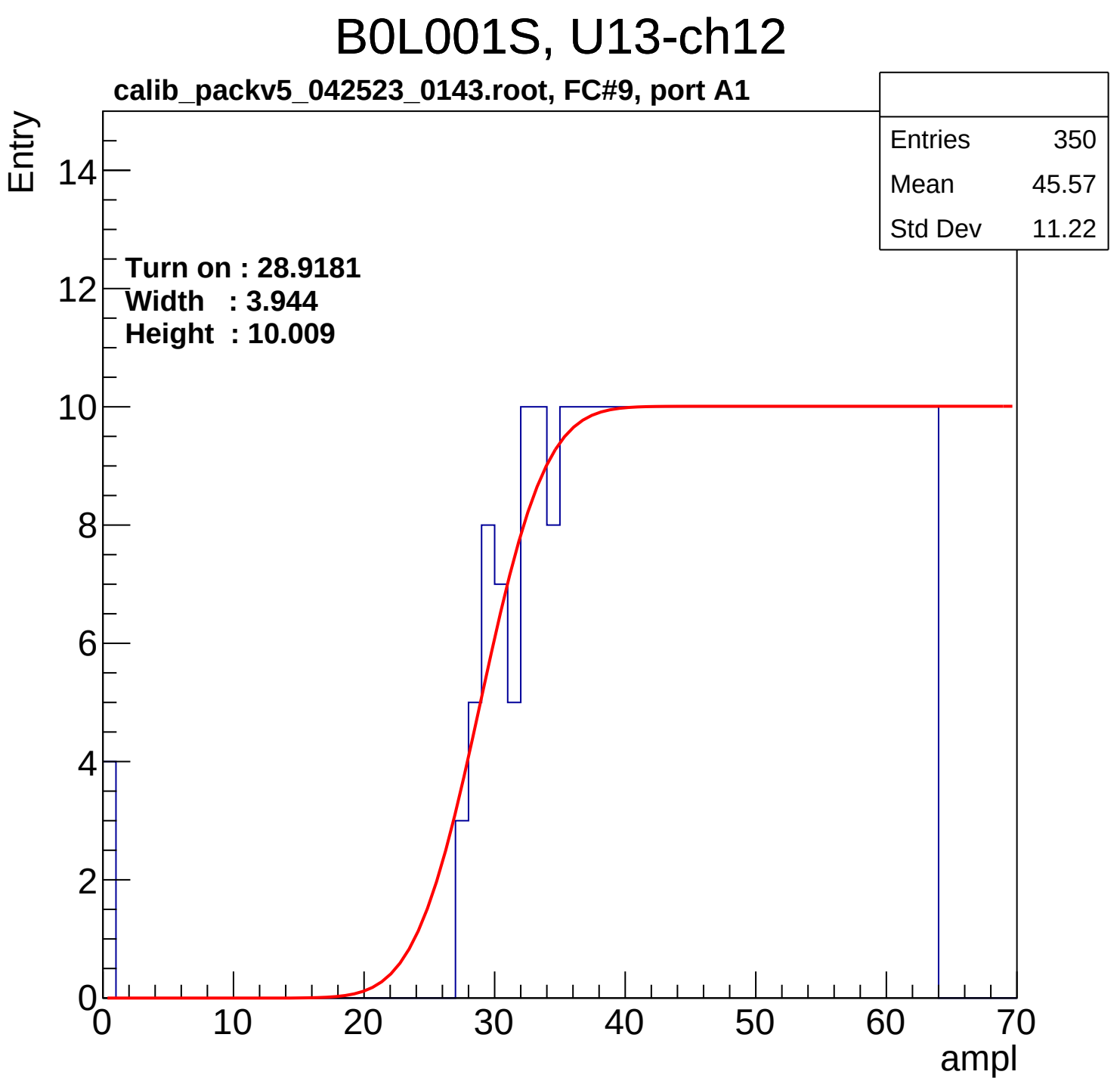
B0L001S, U13-ch12
calib_packv5_042523_0143.root, FC#9, port A1
Entries 350
Mean 45.57
Std Dev 11.22
Turn on : 28.9181
Width : 3.944
Height : 10.009
Entry
ampl
0
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4
6
8
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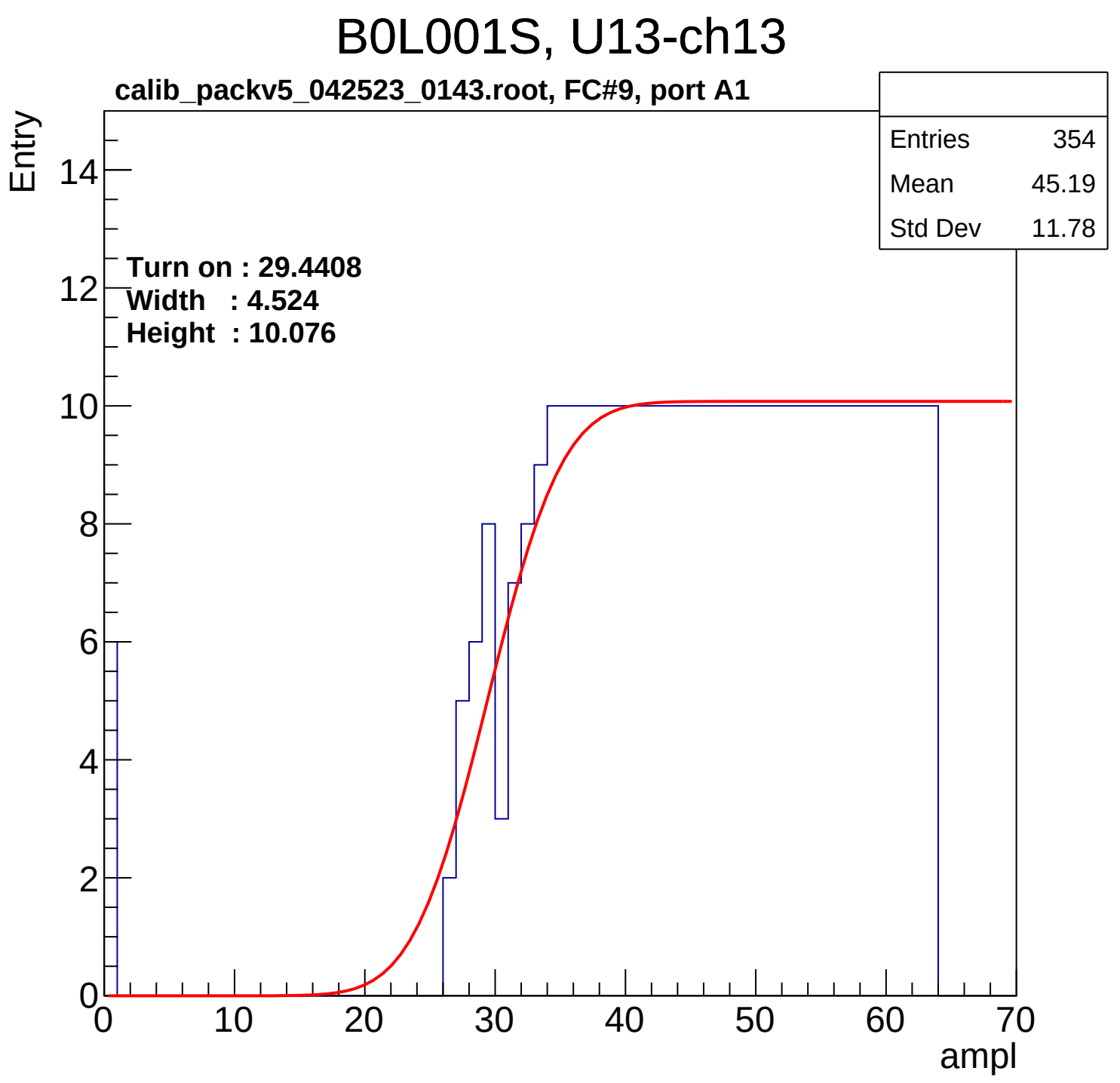
B0L001S, U13-ch13
calib_packv5_042523_0143.root, FC#9, port A1
Entries 354
Mean 45.19
Std Dev 11.78
Turn on : 29.4408
Width : 4.524
Height : 10.076
Entry
ampl
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6
8
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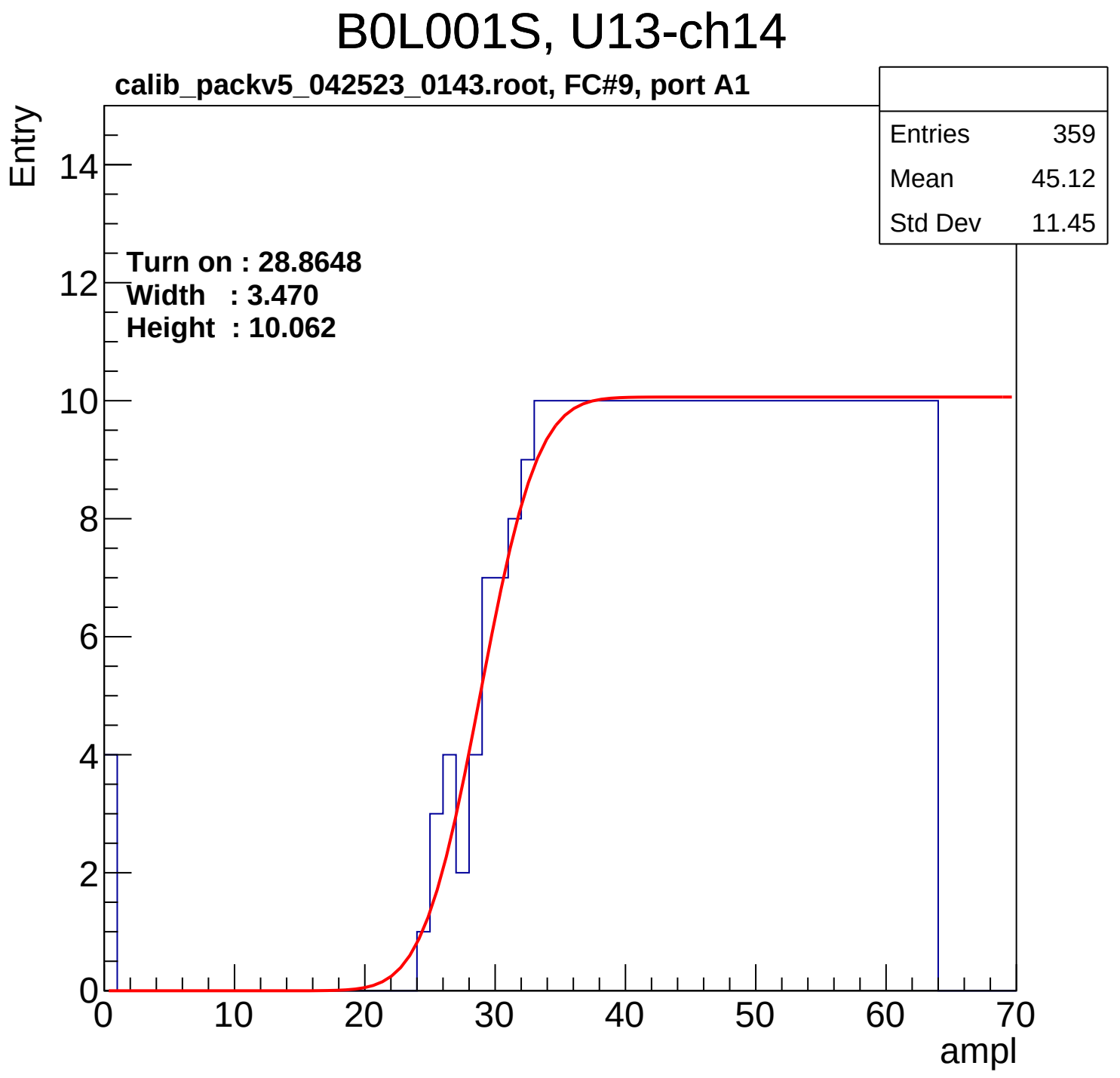
B0L001S, U13-ch14
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 45.12
Std Dev 11.45
Turn on : 28.8648
Width : 3.470
Height : 10.062
Entry
ampl
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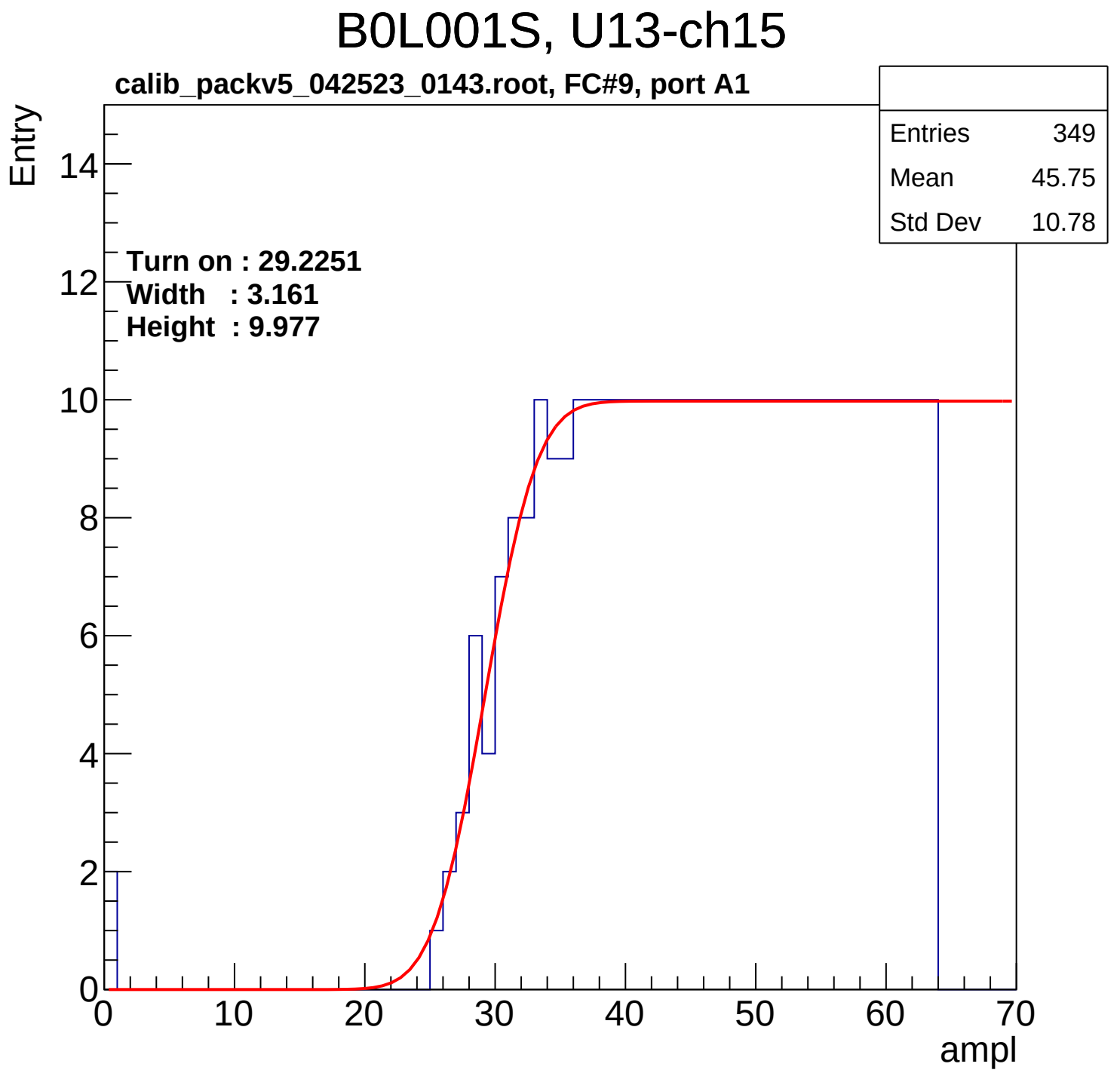
B0L001S, U13-ch15
calib_packv5_042523_0143.root, FC#9, port A1
Entries 349
Mean 45.75
Std Dev 10.78
Turn on : 29.2251
Width : 3.161
Height : 9.977
Entry
ampl
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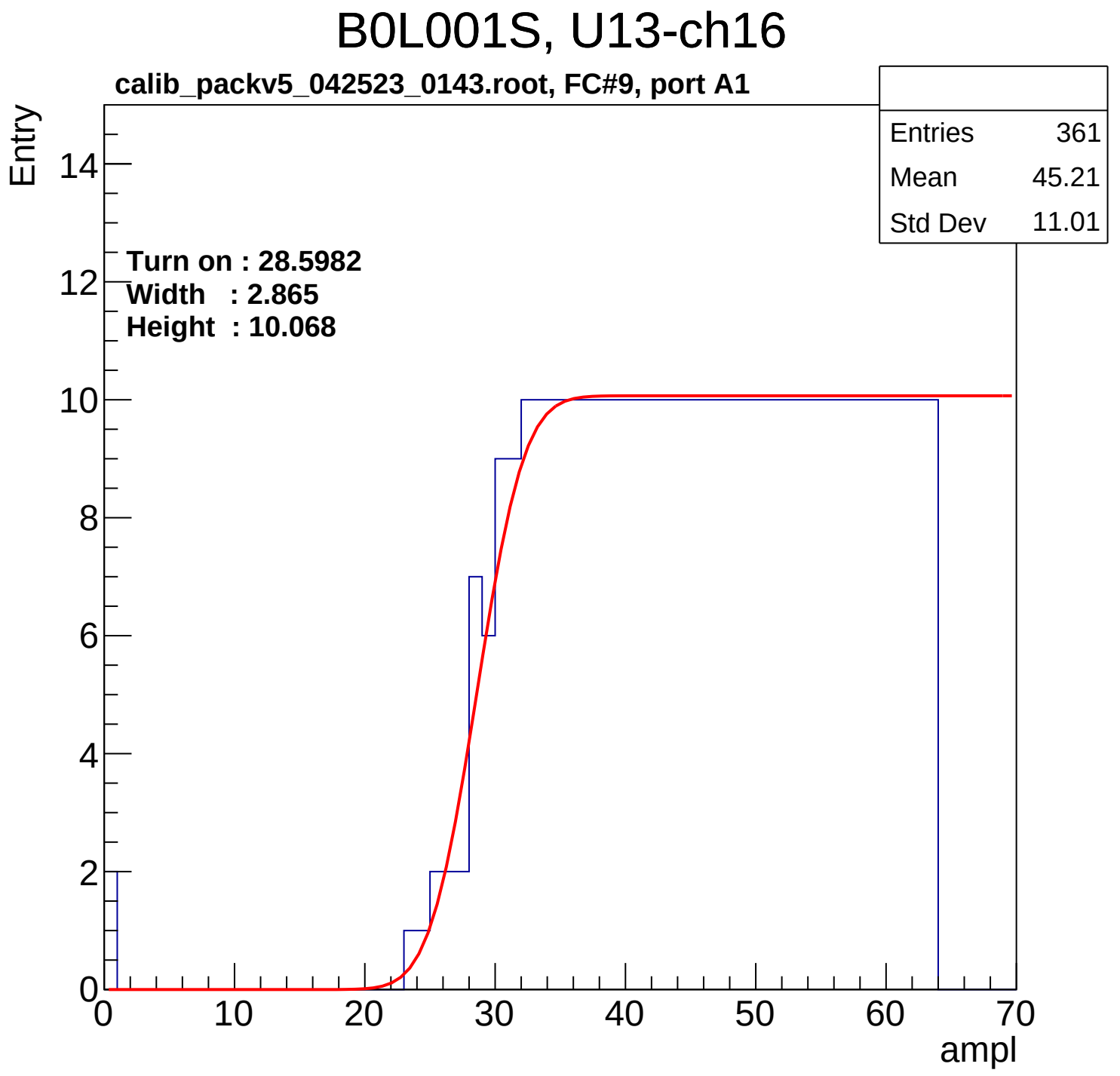
B0L001S, U13-ch16
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 45.21
Std Dev 11.01
Turn on : 28.5982
Width : 2.865
Height : 10.068
Entry
ampl
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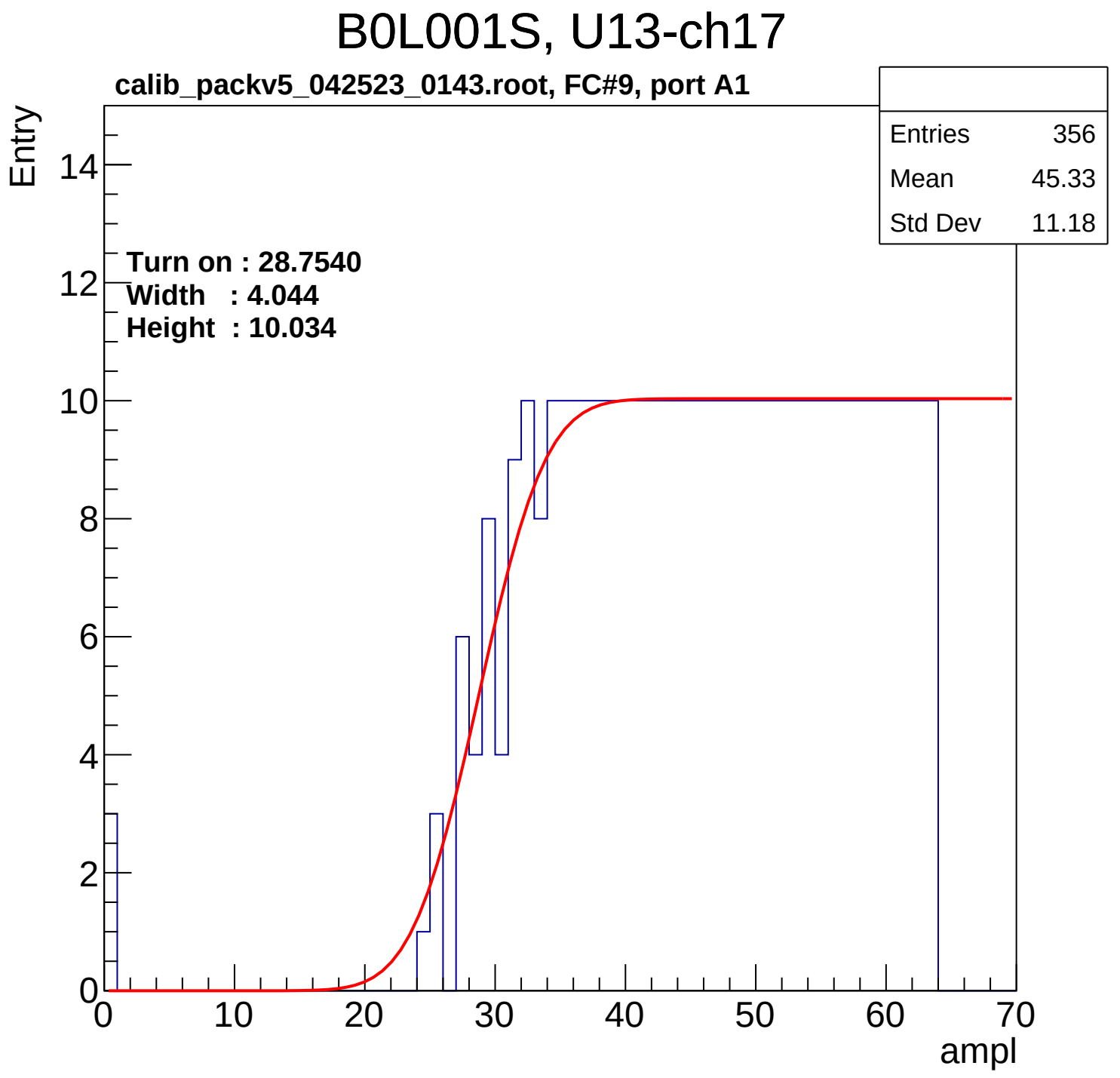
B0L001S, U13-ch17
calib_packv5_042523_0143.root, FC#9, port A1
Entries 356
Mean 45.33
Std Dev 11.18
Turn on : 28.7540
Width : 4.044
Height : 10.034
Entry
ampl
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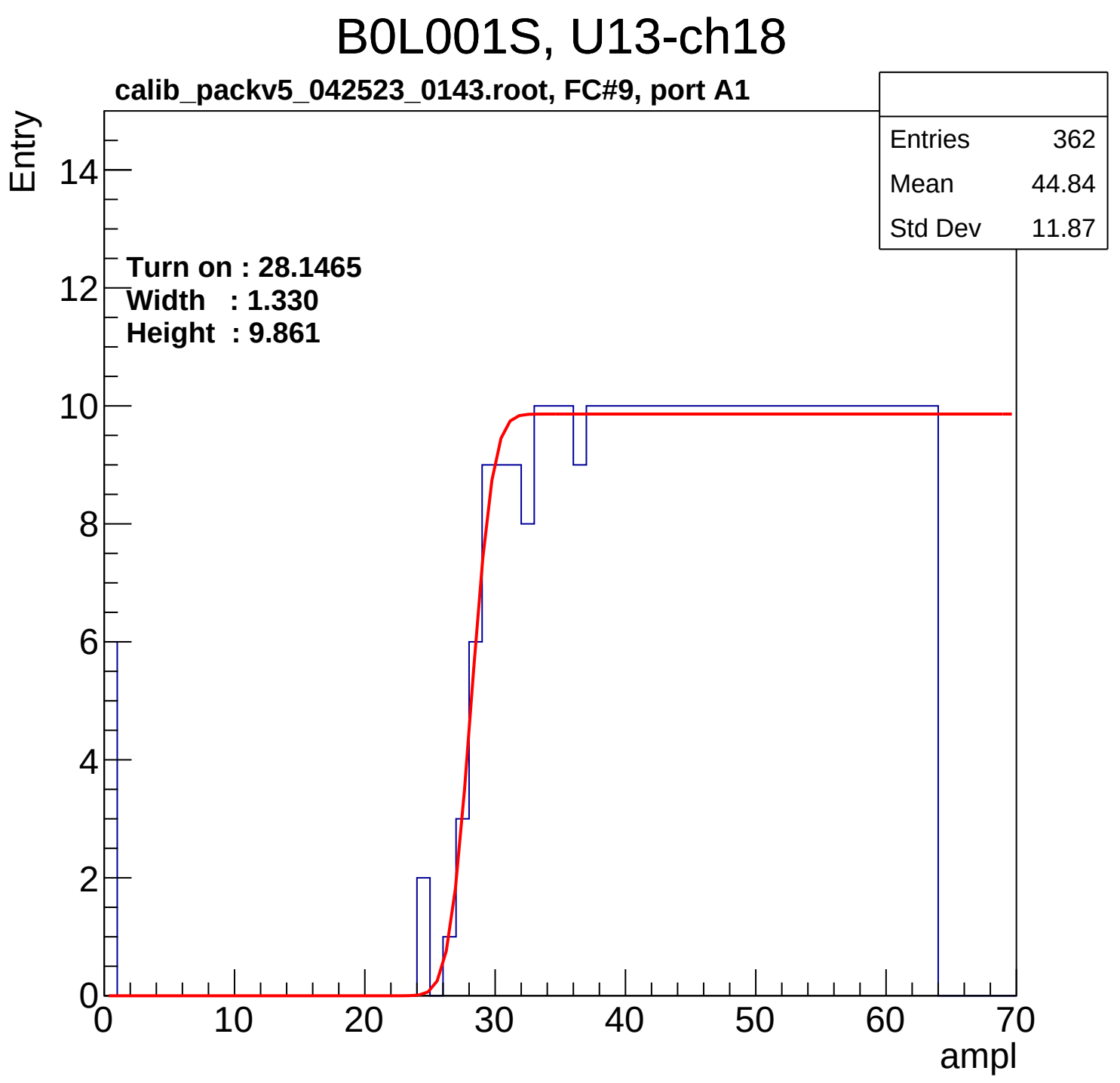
B0L001S, U13-ch18
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 44.84
Std Dev 11.87
Turn on : 28.1465
Width : 1.330
Height : 9.861
Entry
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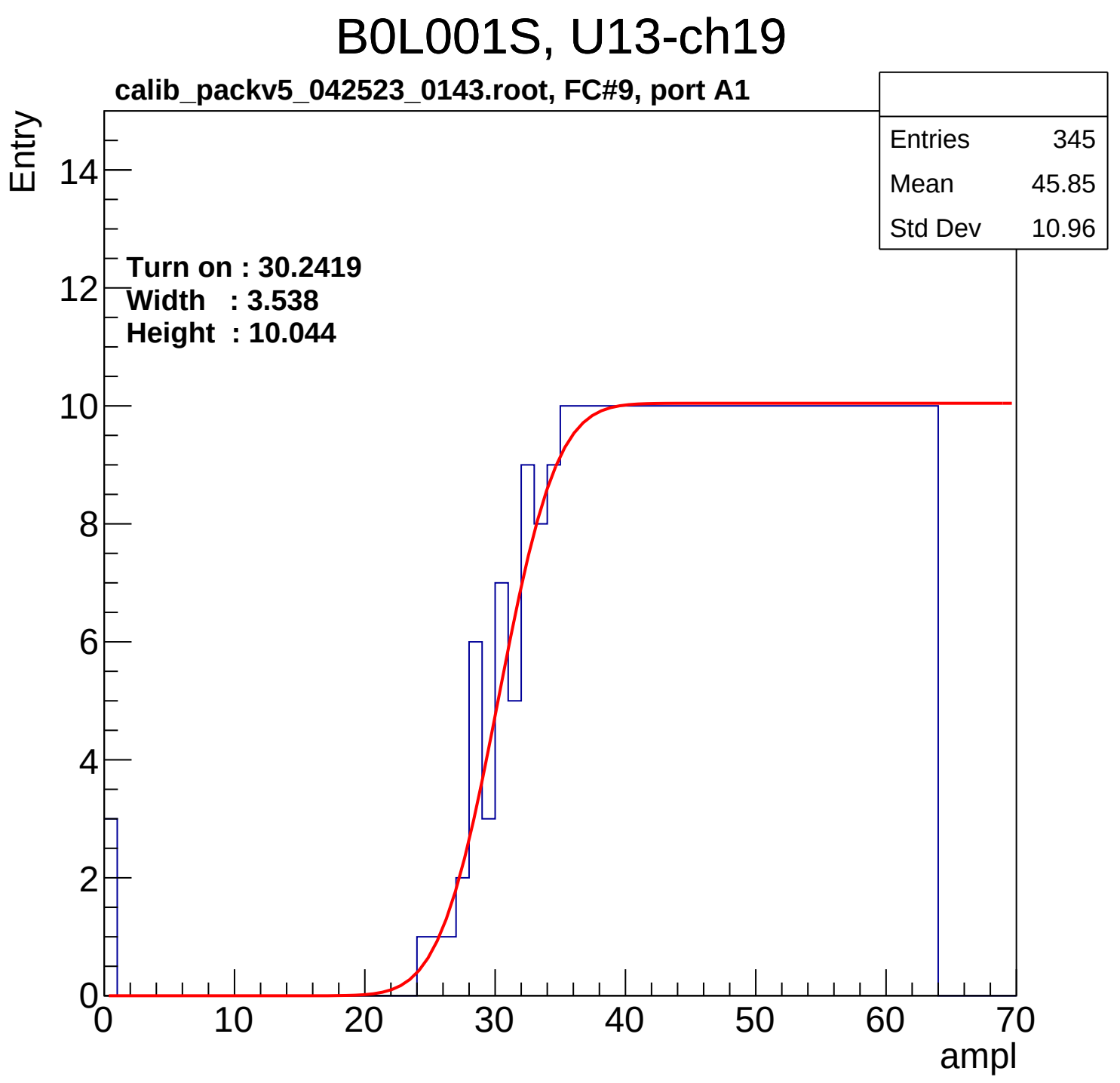
B0L001S, U13-ch19
calib_packv5_042523_0143.root, FC#9, port A1
Entries 345
Mean 45.85
Std Dev 10.96
Turn on : 30.2419
Width : 3.538
Height : 10.044
Entry
ampl
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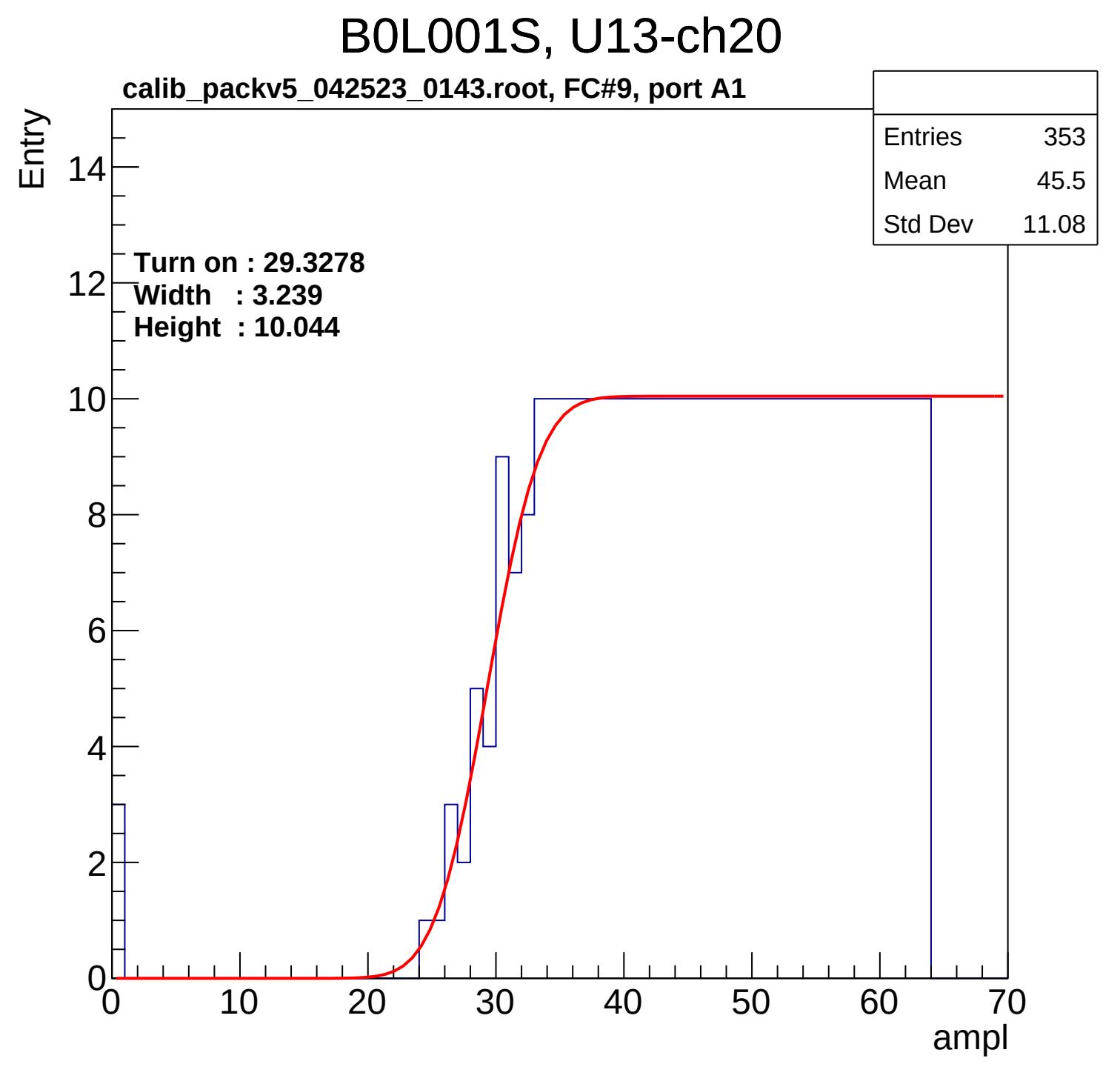
B0L001S, U13-ch20
calib_packv5_042523_0143.root, FC#9, port A1
Entries 353
Mean 45.5
Std Dev 11.08
Turn on : 29.3278
Width : 3.239
Height : 10.044
Entry
ampl
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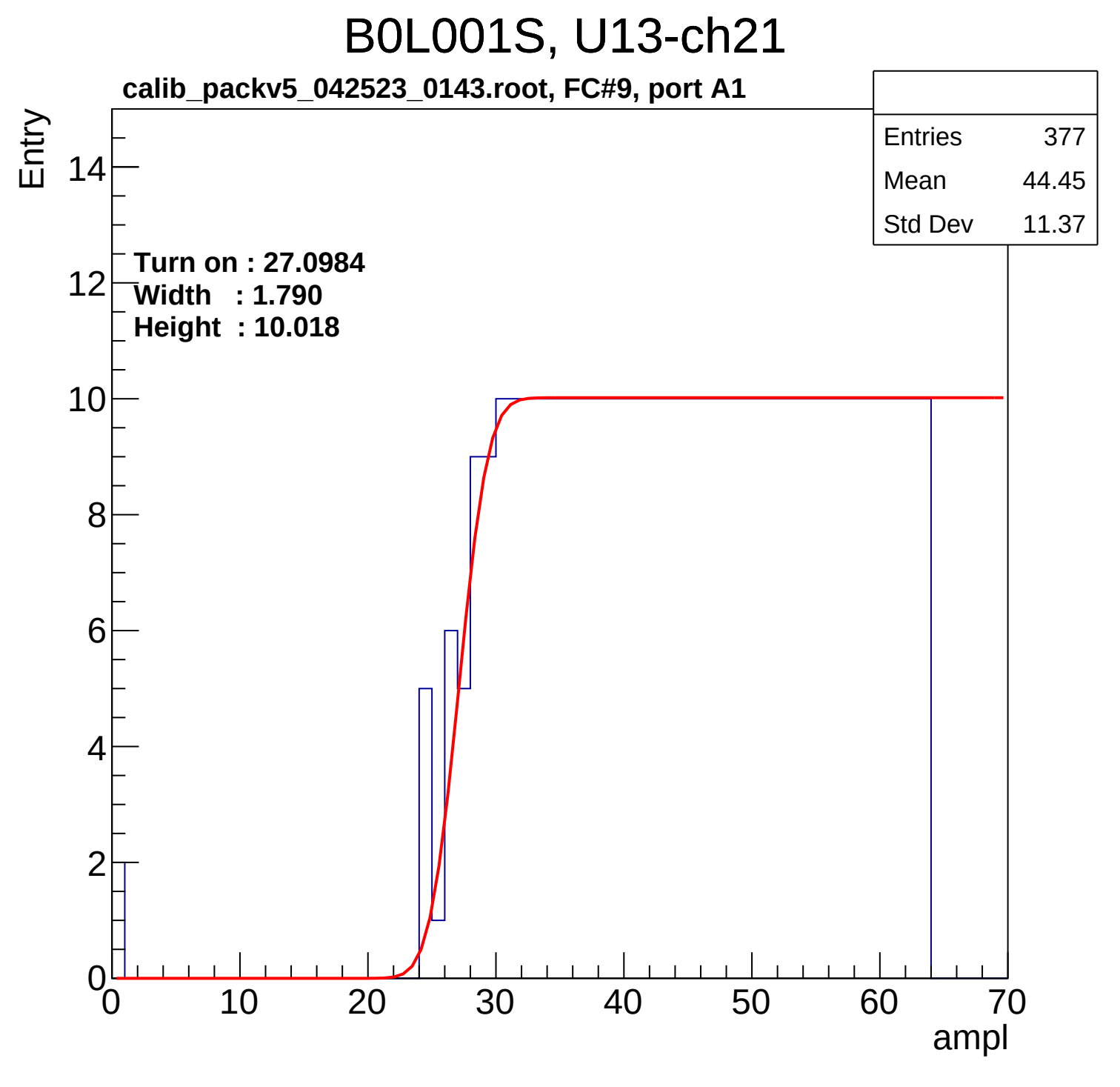
B0L001S, U13-ch21
calib_packv5_042523_0143.root, FC#9, port A1
Entries 377
Mean 44.45
Std Dev 11.37
Turn on : 27.0984
Width : 1.790
Height : 10.018
Entry
ampl
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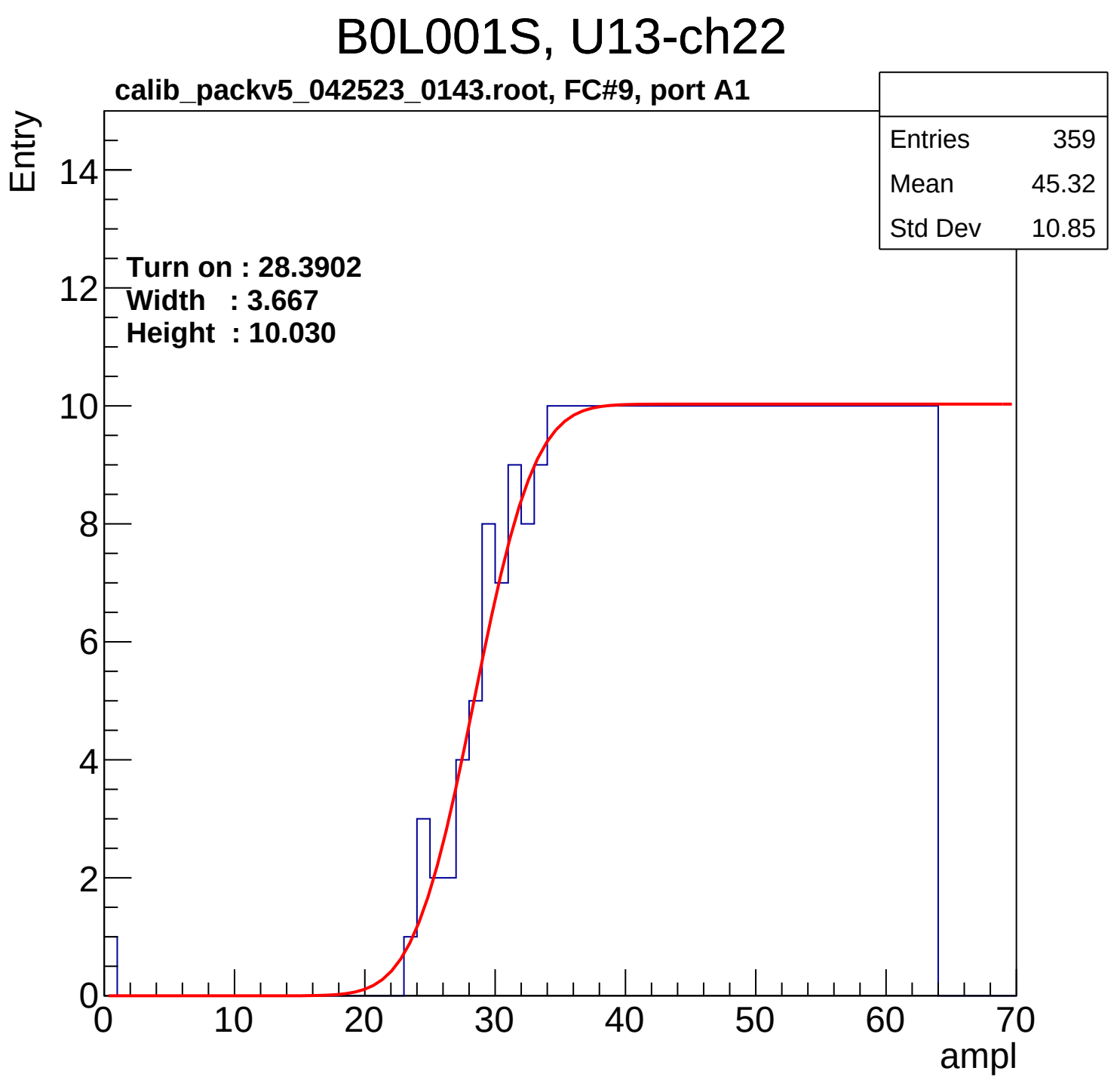
B0L001S, U13-ch22
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 45.32
Std Dev 10.85
Turn on : 28.3902
Width : 3.667
Height : 10.030
Entry
ampl
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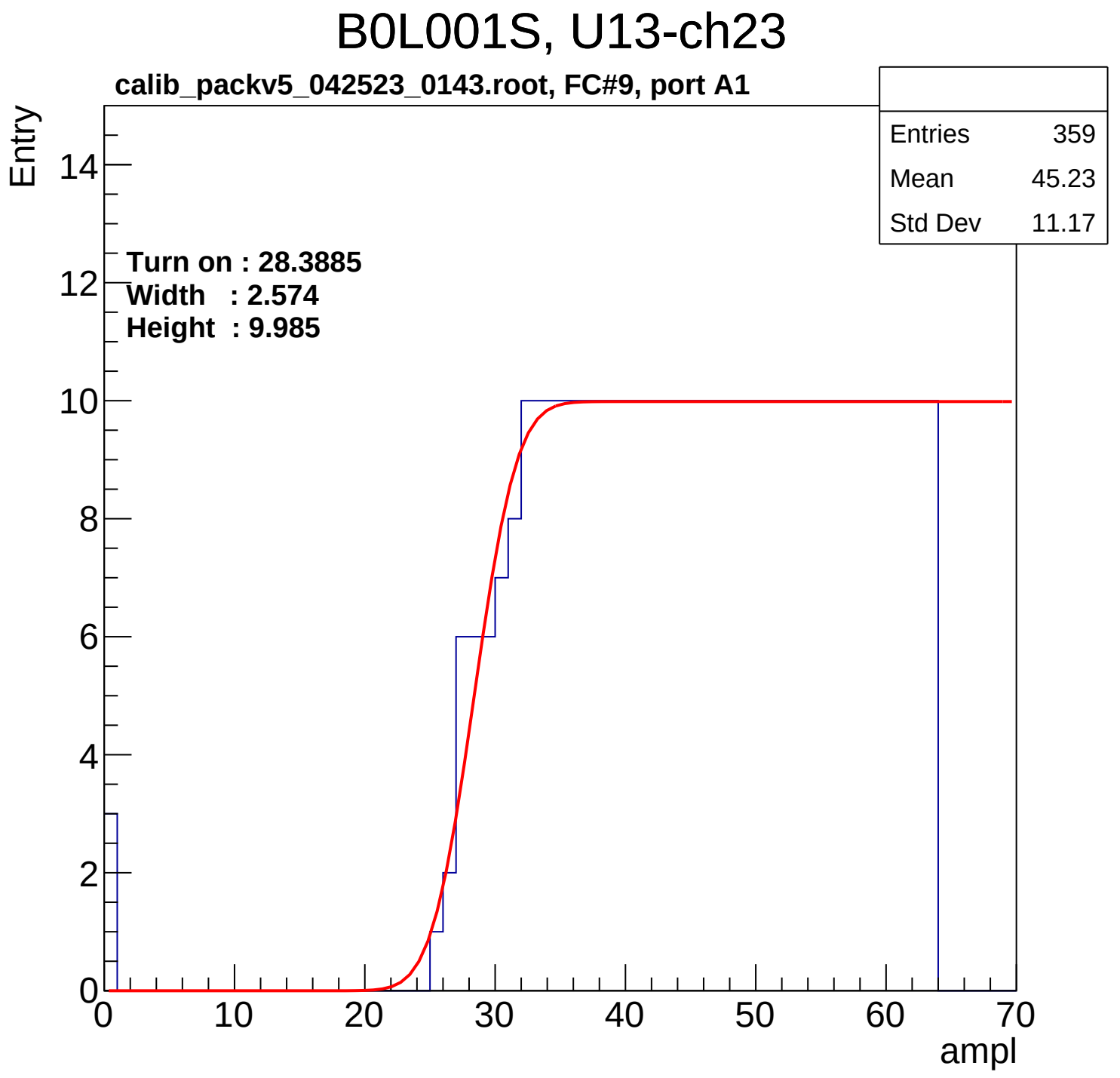
B0L001S, U13-ch23
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 45.23
Std Dev 11.17
Turn on : 28.3885
Width : 2.574
Height : 9.985
Entry
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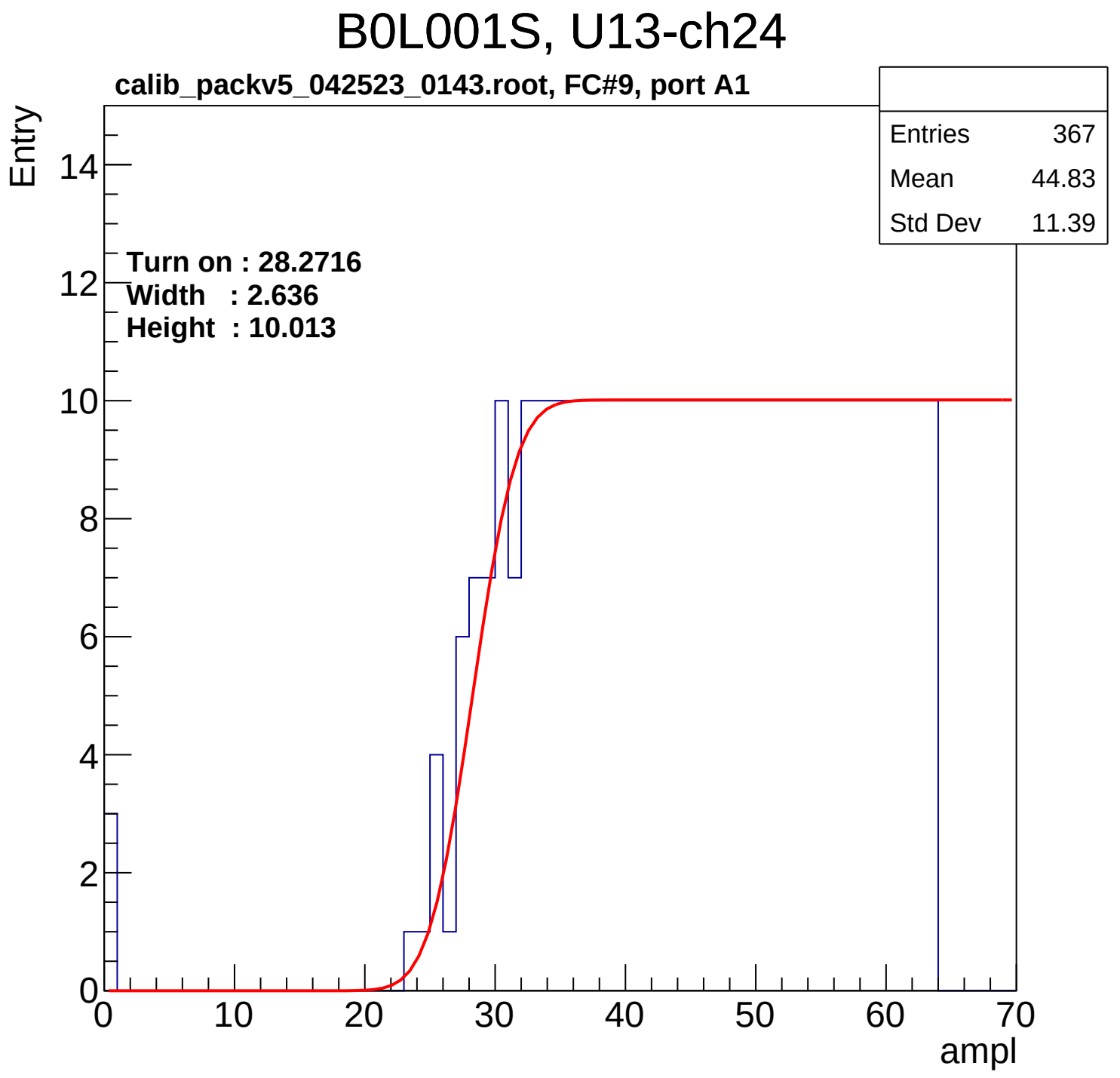
B0L001S, U13-ch24
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.83
Std Dev 11.39
Turn on : 28.2716
Width : 2.636
Height : 10.013
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ampl
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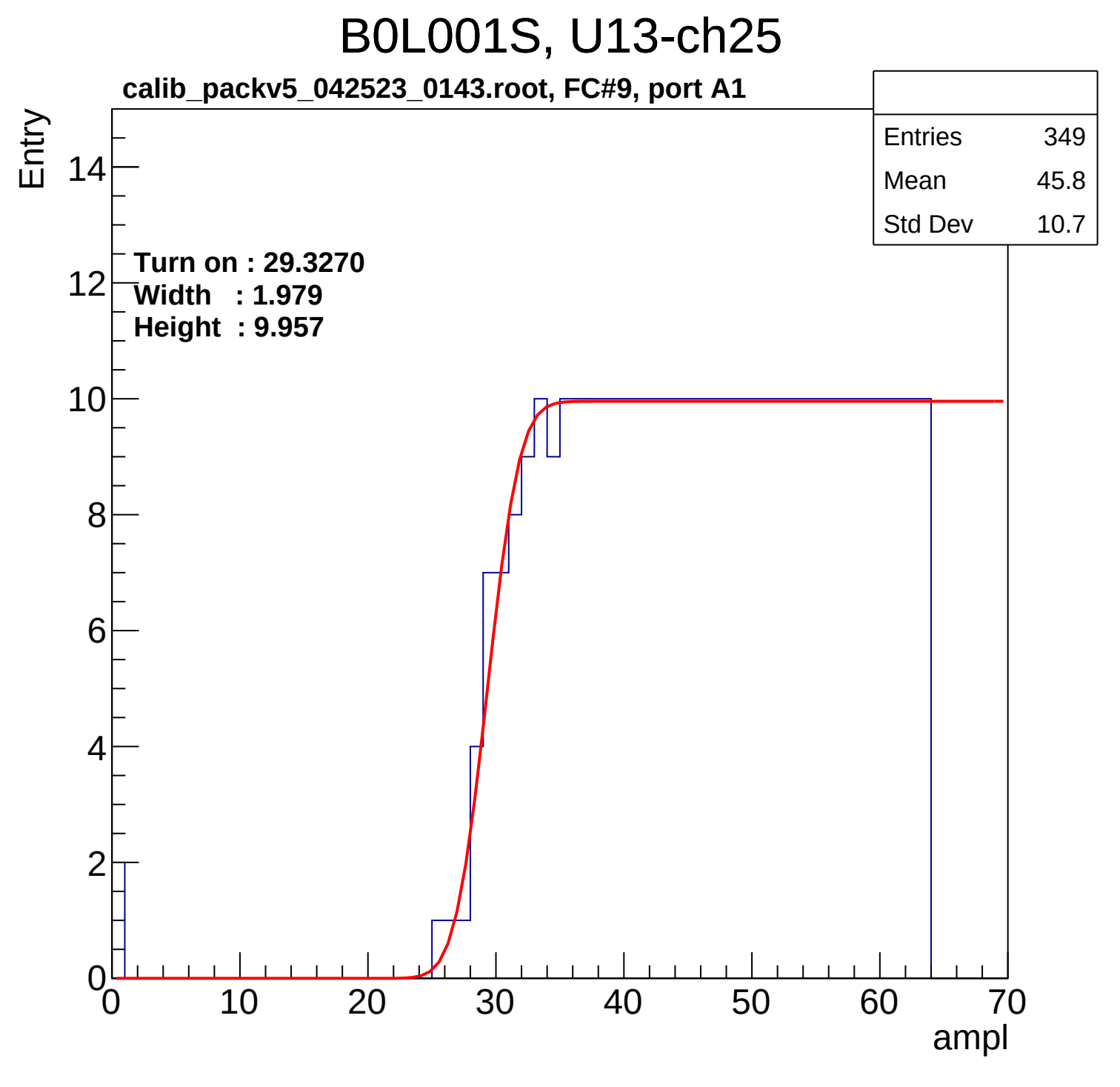
B0L001S, U13-ch25
calib_packv5_042523_0143.root, FC#9, port A1
Entries 349
Mean 45.8
Std Dev 10.7
Turn on : 29.3270
Width : 1.979
Height : 9.957
Entry
ampl
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2
4
6
8
10
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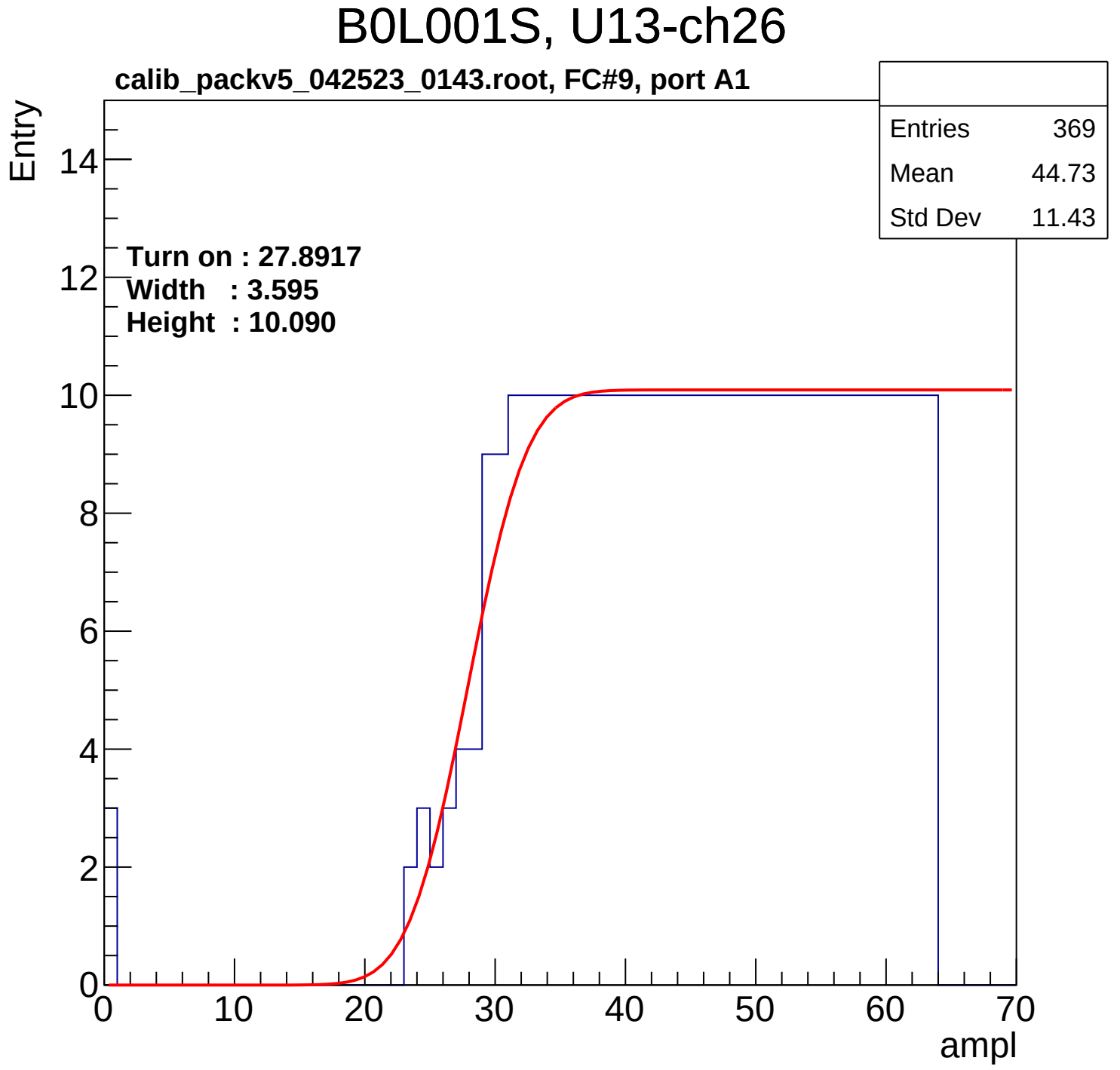
B0L001S, U13-ch26
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.73
Std Dev 11.43
Turn on : 27.8917
Width : 3.595
Height : 10.090
Entry
ampl
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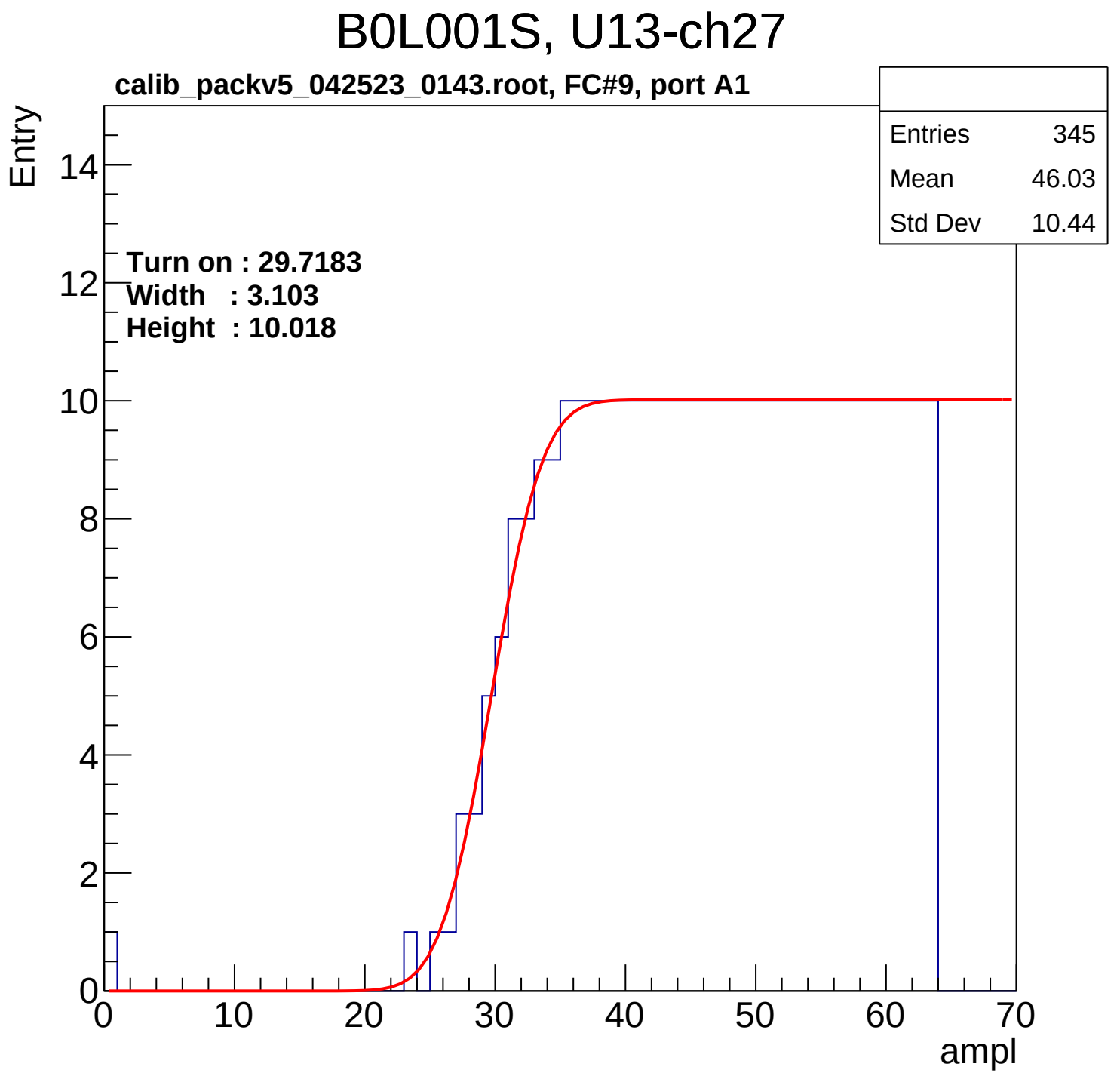
B0L001S, U13-ch27
calib_packv5_042523_0143.root, FC#9, port A1
Entries 345
Mean 46.03
Std Dev 10.44
Turn on : 29.7183
Width : 3.103
Height : 10.018
Entry
ampl
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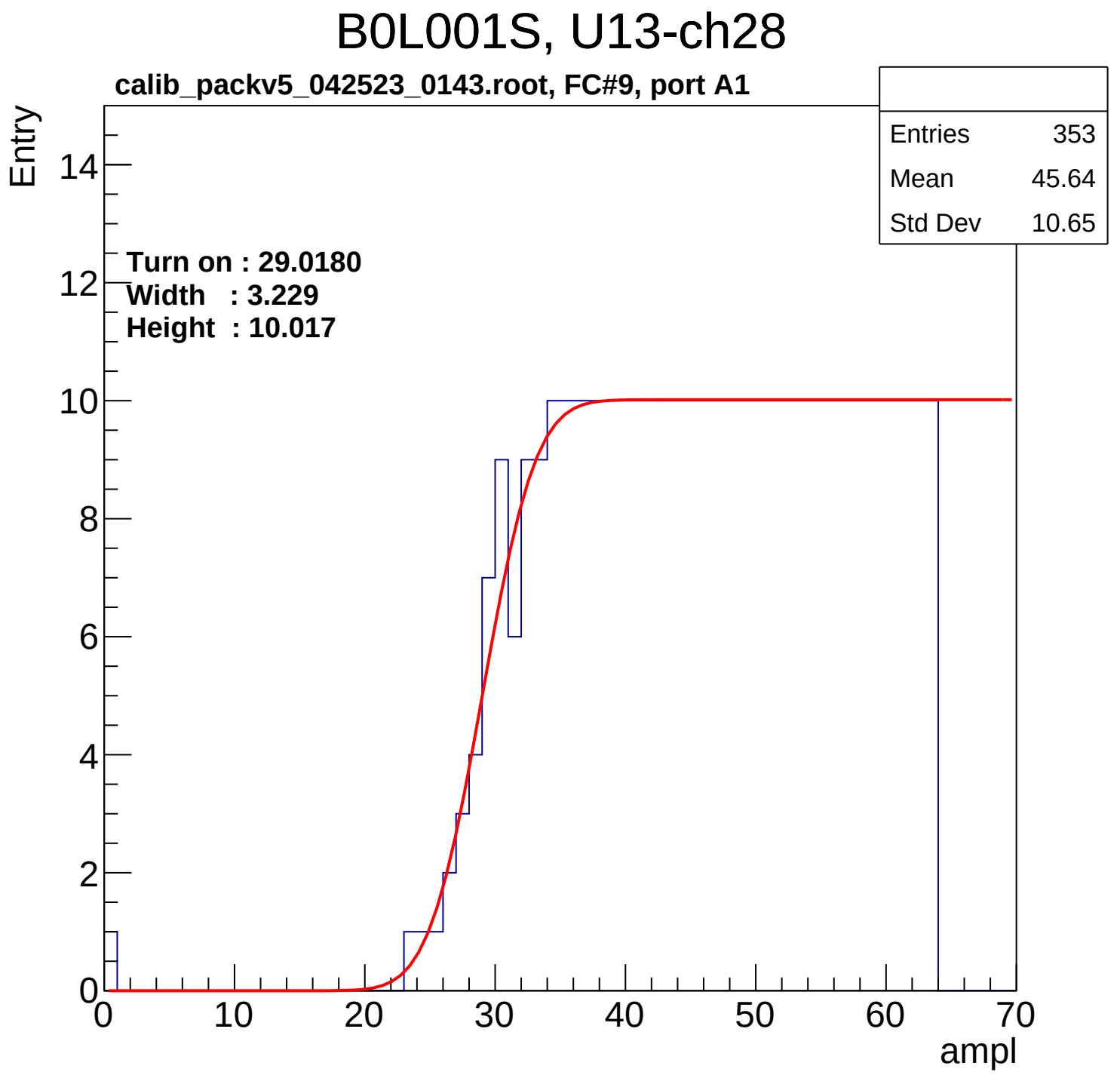
B0L001S, U13-ch28
calib_packv5_042523_0143.root, FC#9, port A1
Entries 353
Mean 45.64
Std Dev 10.65
Turn on : 29.0180
Width : 3.229
Height : 10.017
Entry
ampl
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4
6
8
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20
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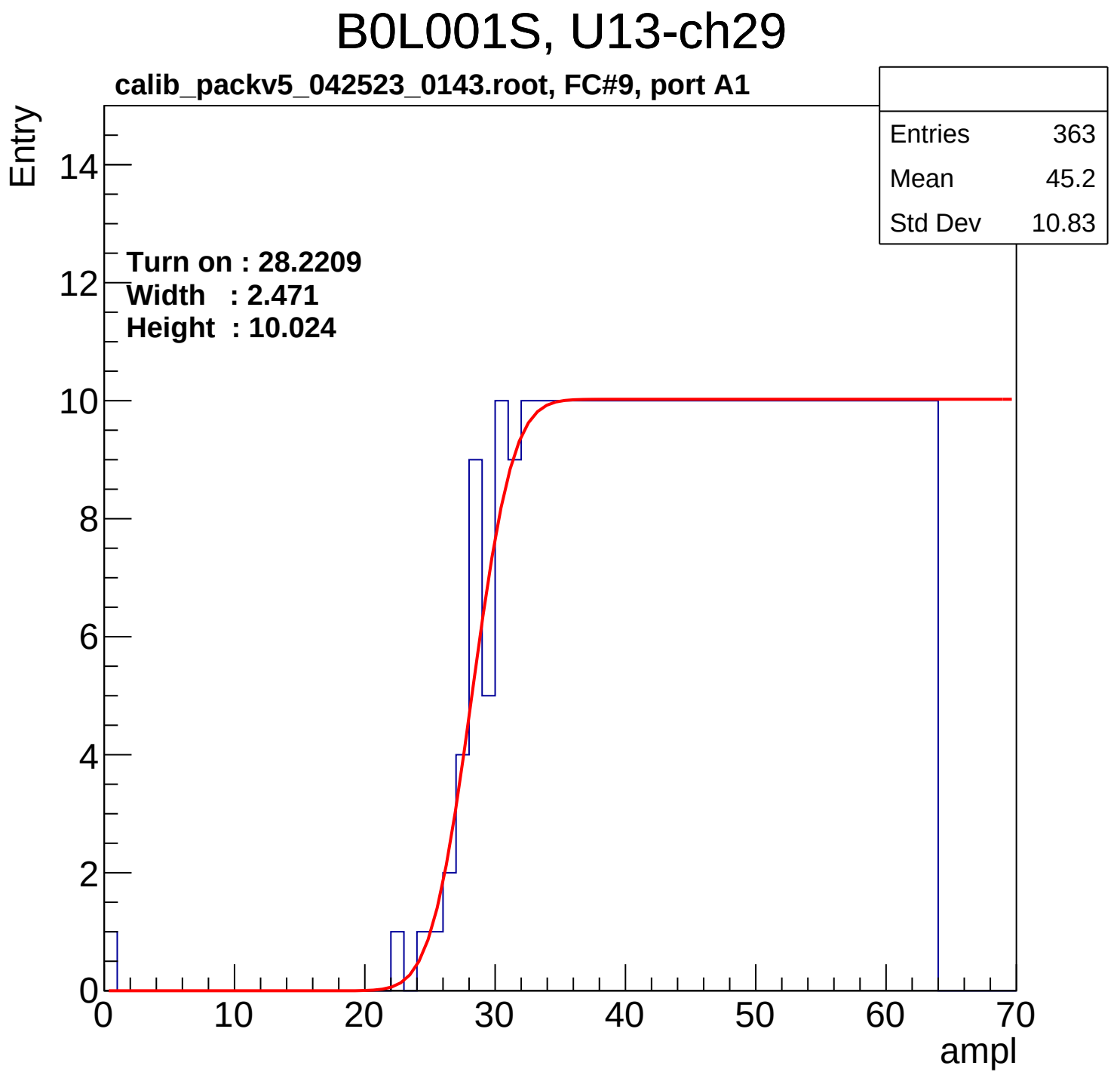
B0L001S, U13-ch29
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 45.2
Std Dev 10.83
Turn on : 28.2209
Width : 2.471
Height : 10.024
Entry
ampl
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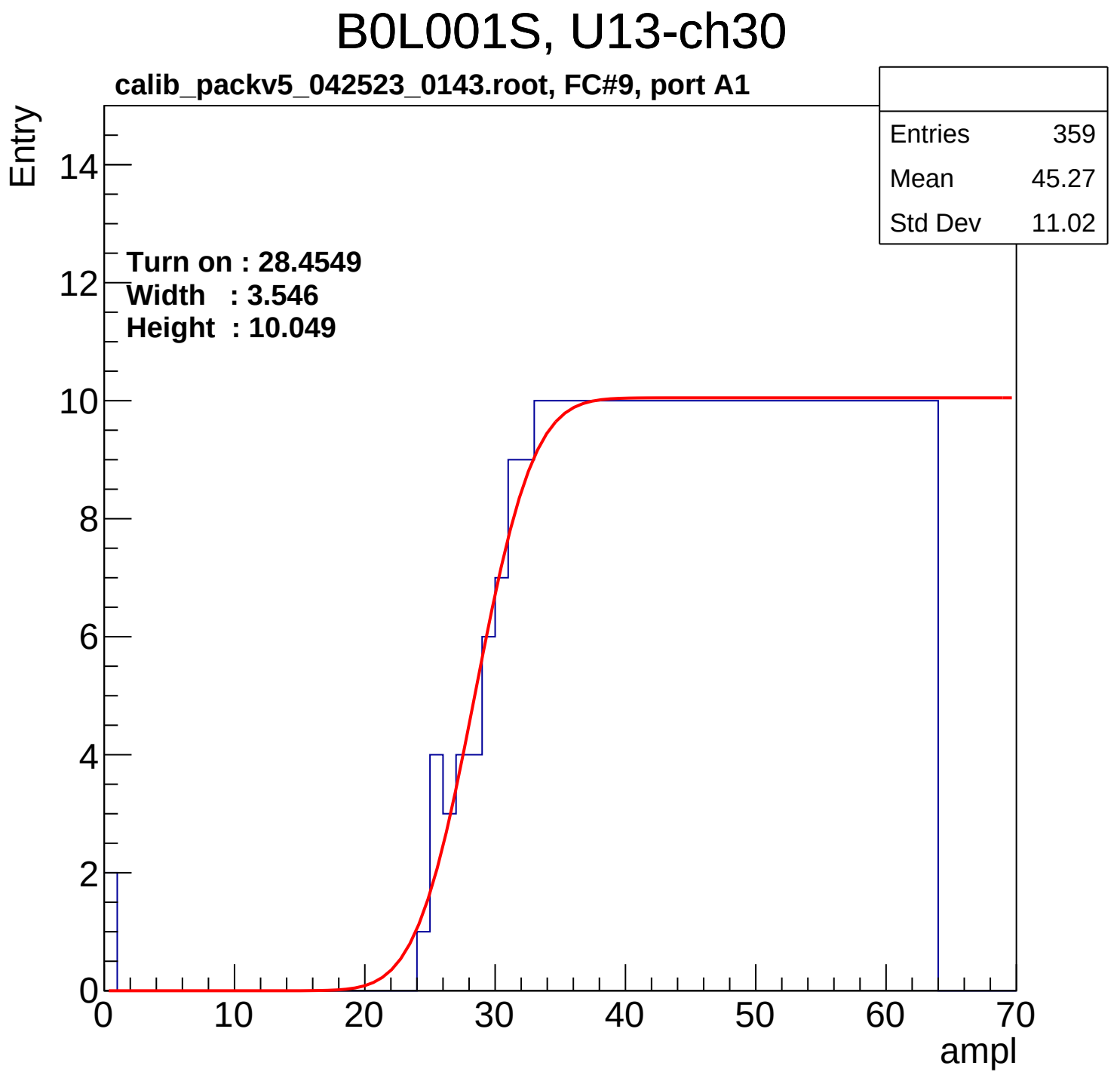
B0L001S, U13-ch30
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 45.27
Std Dev 11.02
Turn on : 28.4549
Width : 3.546
Height : 10.049
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ampl
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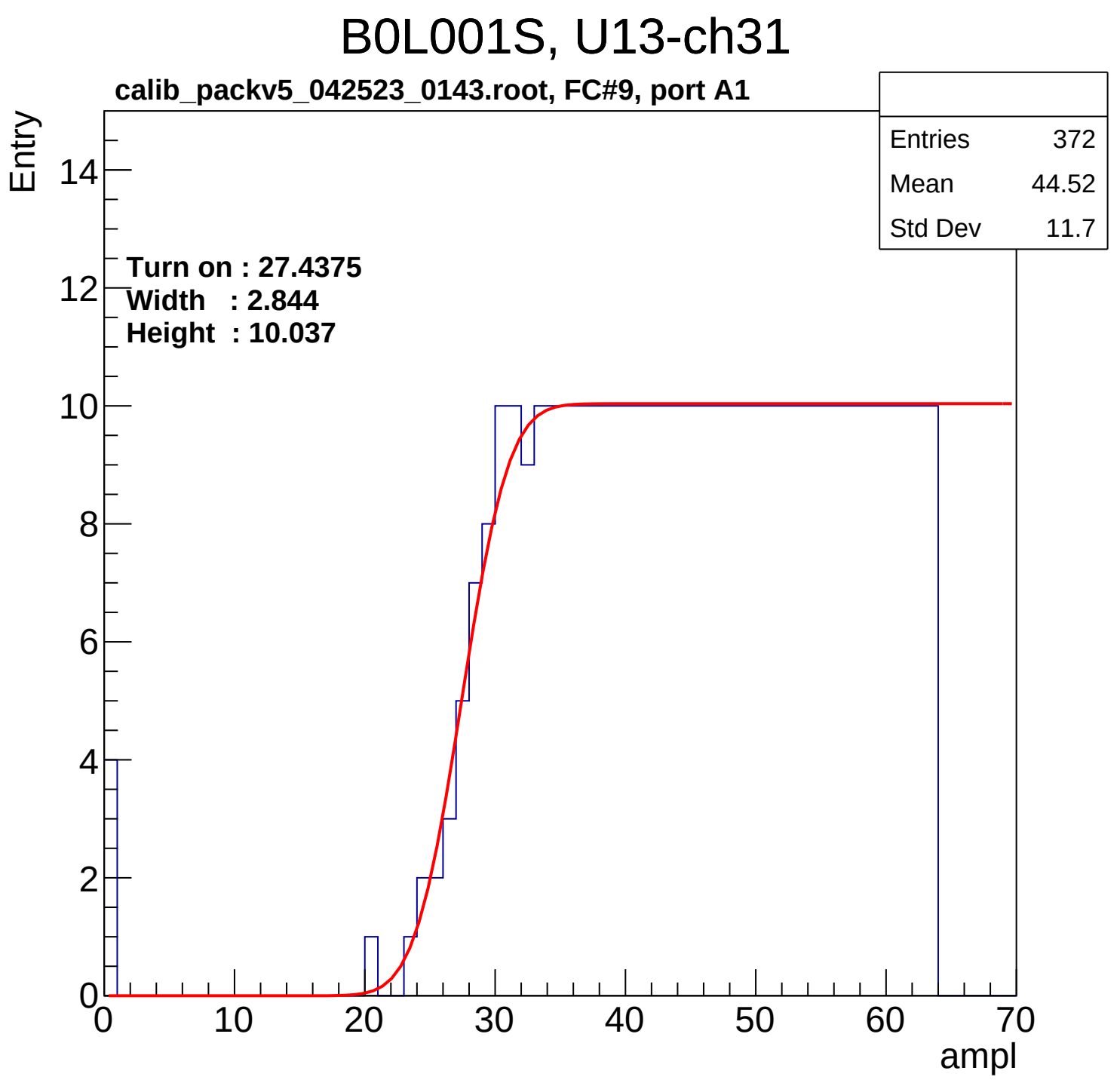
B0L001S, U13-ch31
calib_packv5_042523_0143.root, FC#9, port A1
Entries 372
Mean 44.52
Std Dev 11.7
Turn on : 27.4375
Width : 2.844
Height : 10.037
Entry
ampl
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8
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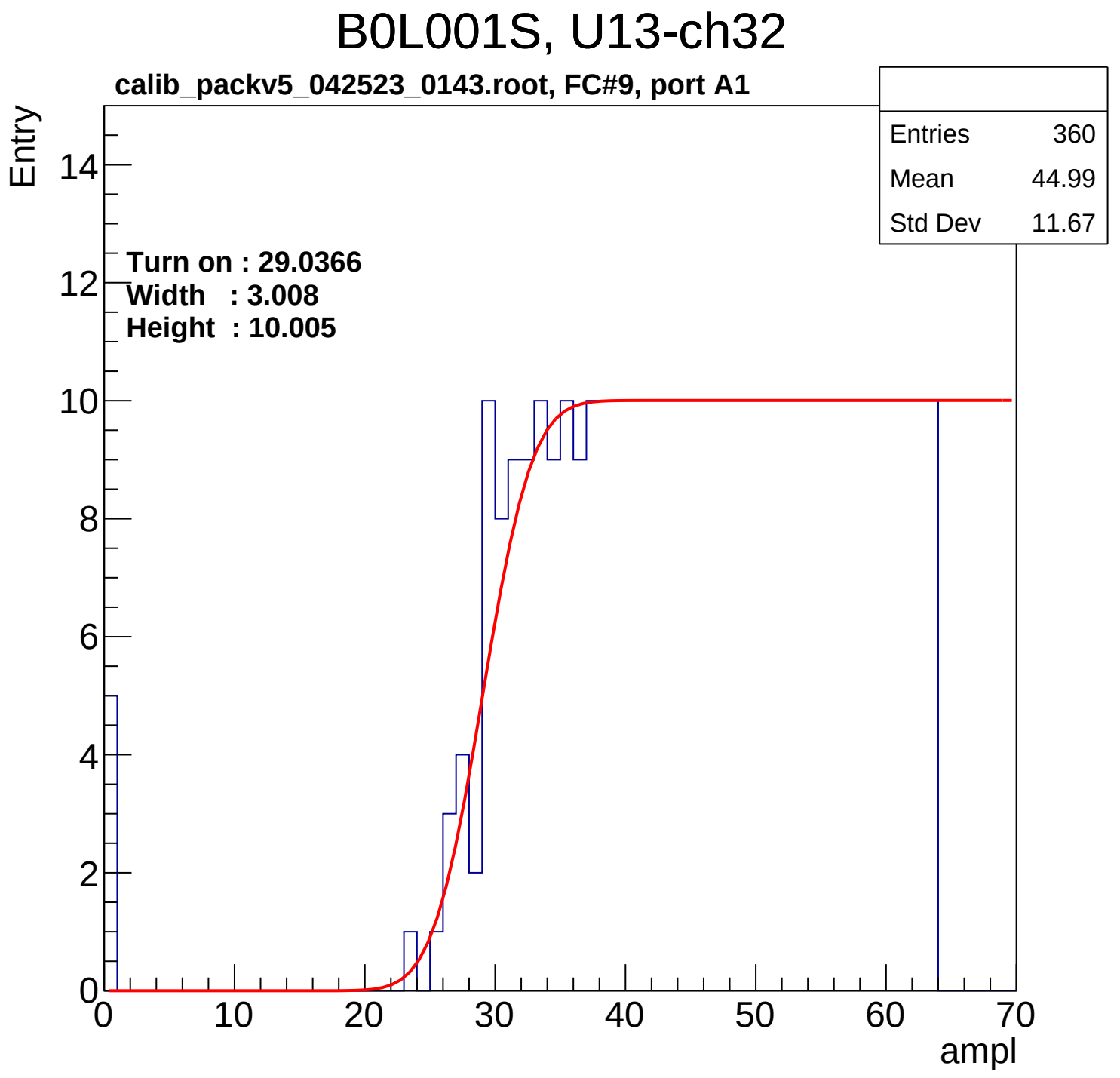
B0L001S, U13-ch32
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 44.99
Std Dev 11.67
Turn on : 29.0366
Width : 3.008
Height : 10.005
Entry
ampl
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6
8
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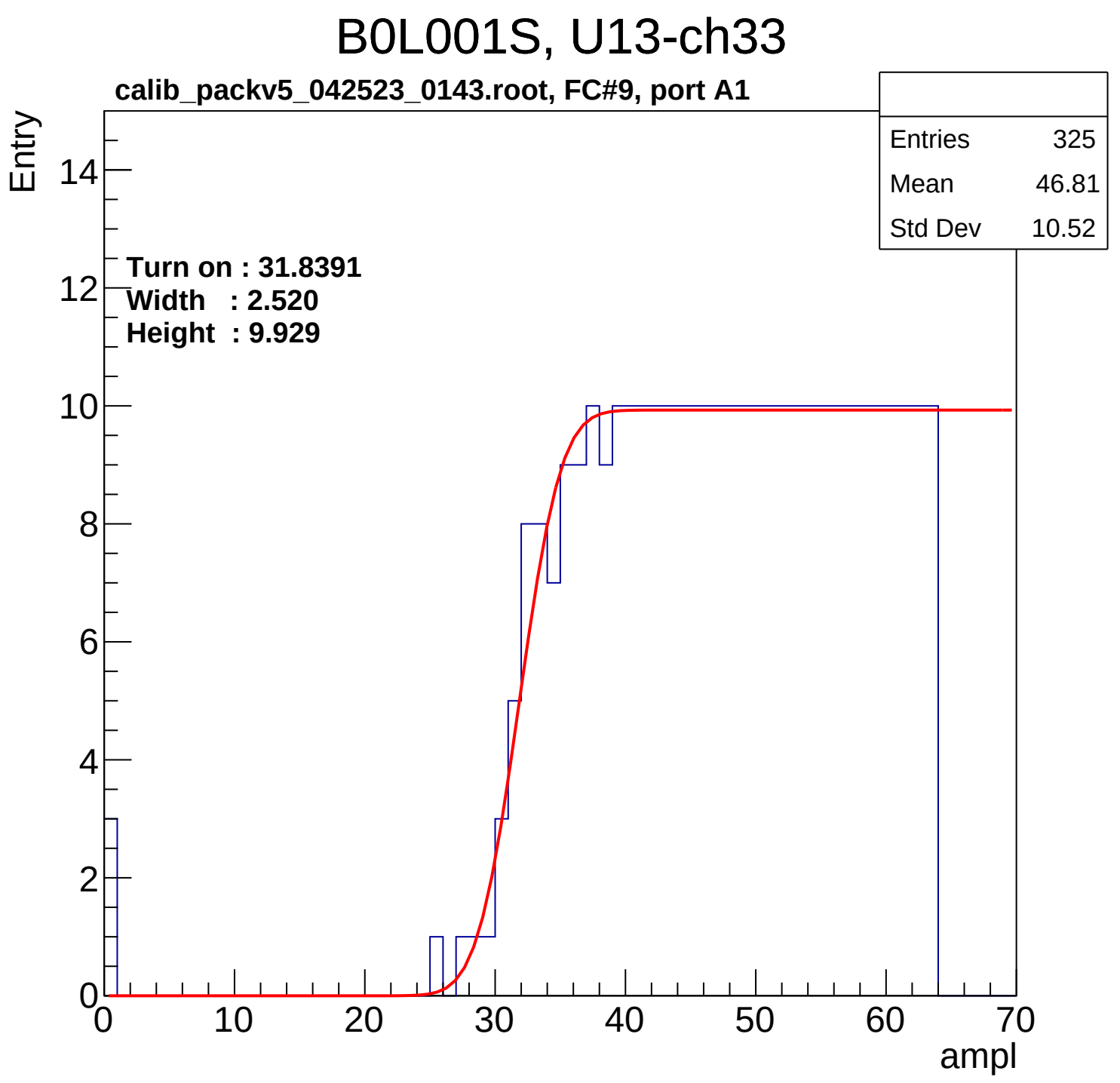
B0L001S, U13-ch33
calib_packv5_042523_0143.root, FC#9, port A1
Entries 325
Mean 46.81
Std Dev 10.52
Turn on : 31.8391
Width : 2.520
Height : 9.929
Entry
ampl
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2
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6
8
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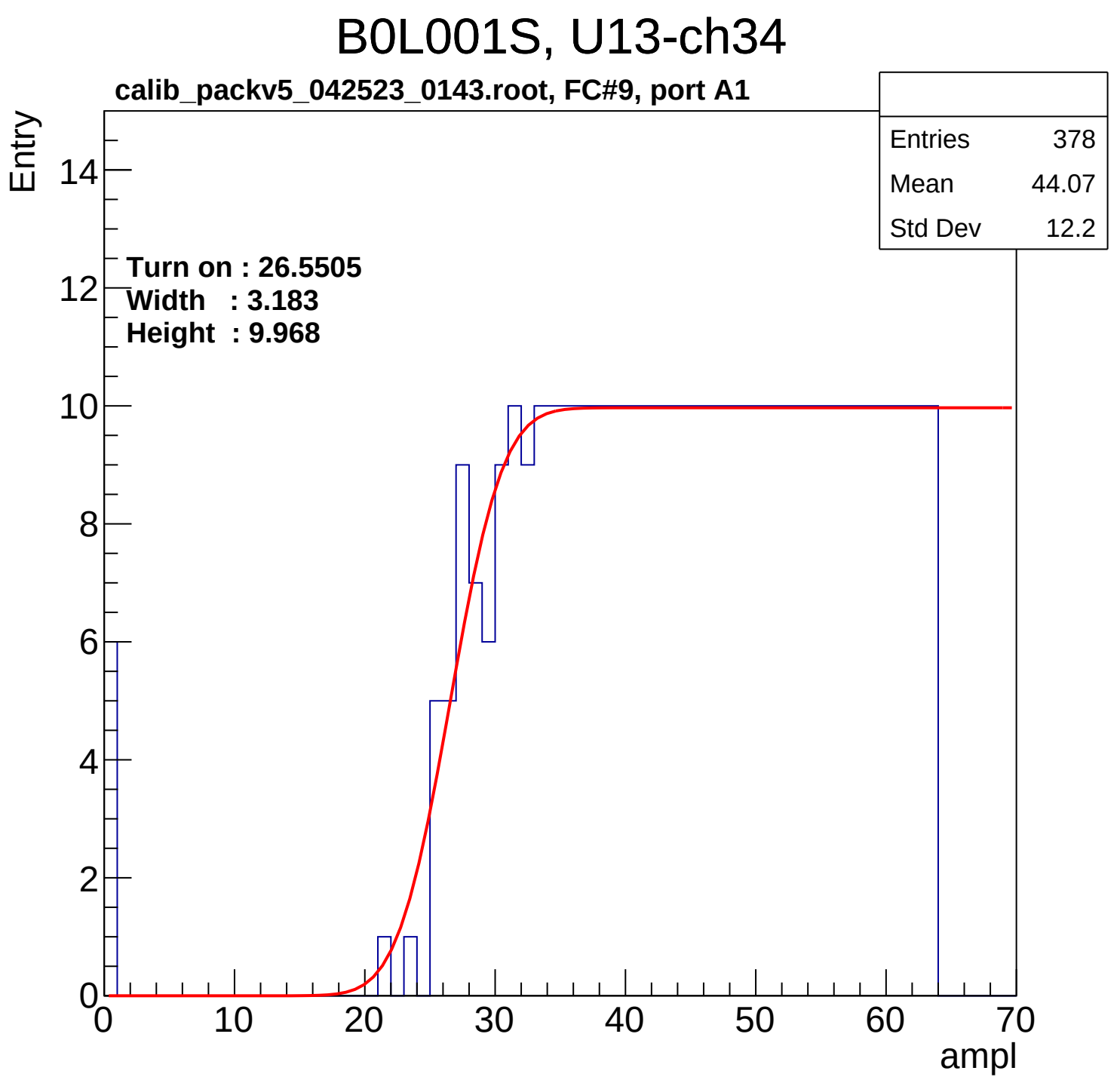
B0L001S, U13-ch34
calib_packv5_042523_0143.root, FC#9, port A1
Entries 378
Mean 44.07
Std Dev 12.2
Turn on : 26.5505
Width : 3.183
Height : 9.968
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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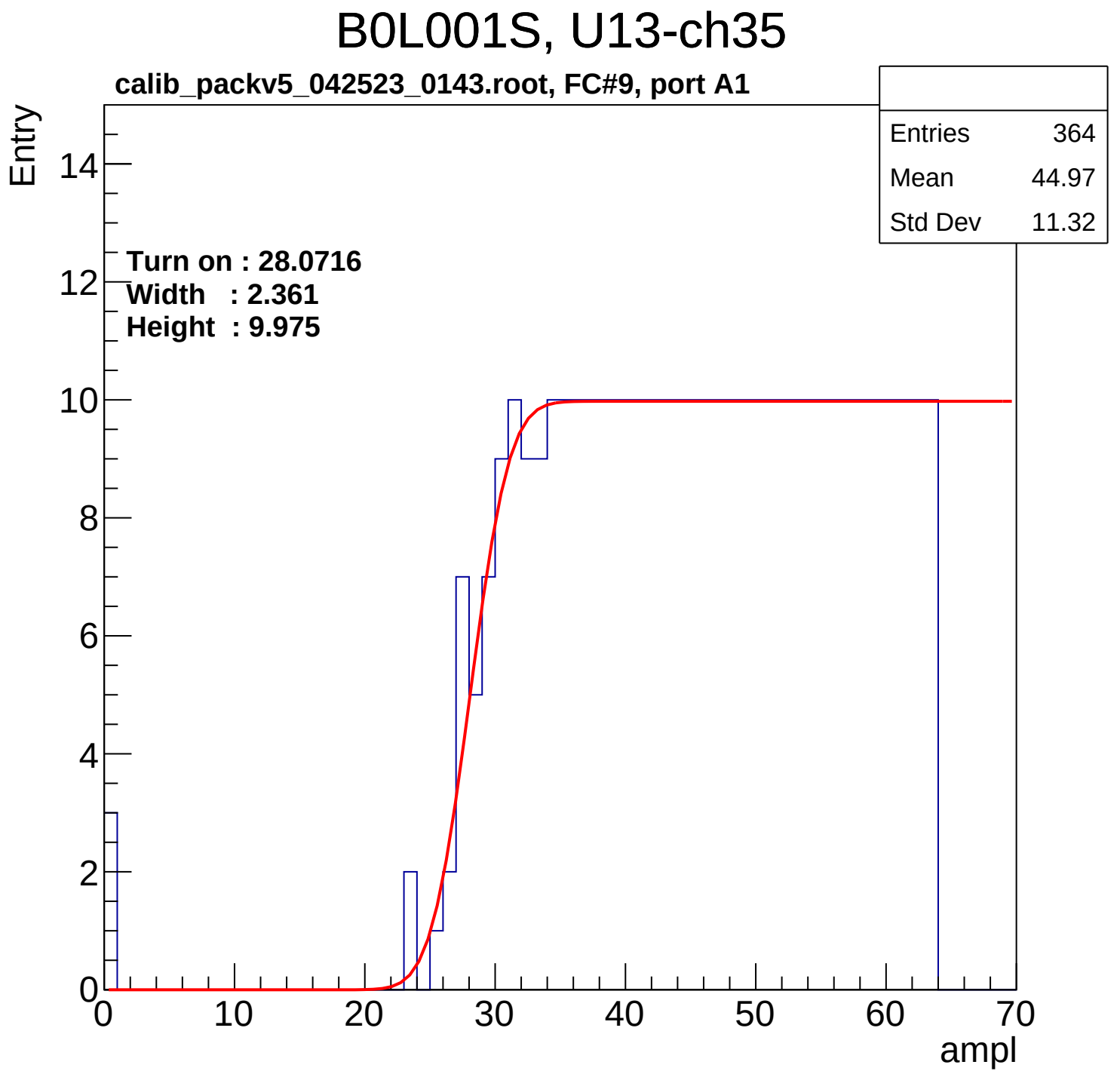
B0L001S, U13-ch35
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 44.97
Std Dev 11.32
Turn on : 28.0716
Width : 2.361
Height : 9.975
Entry
ampl
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6
8
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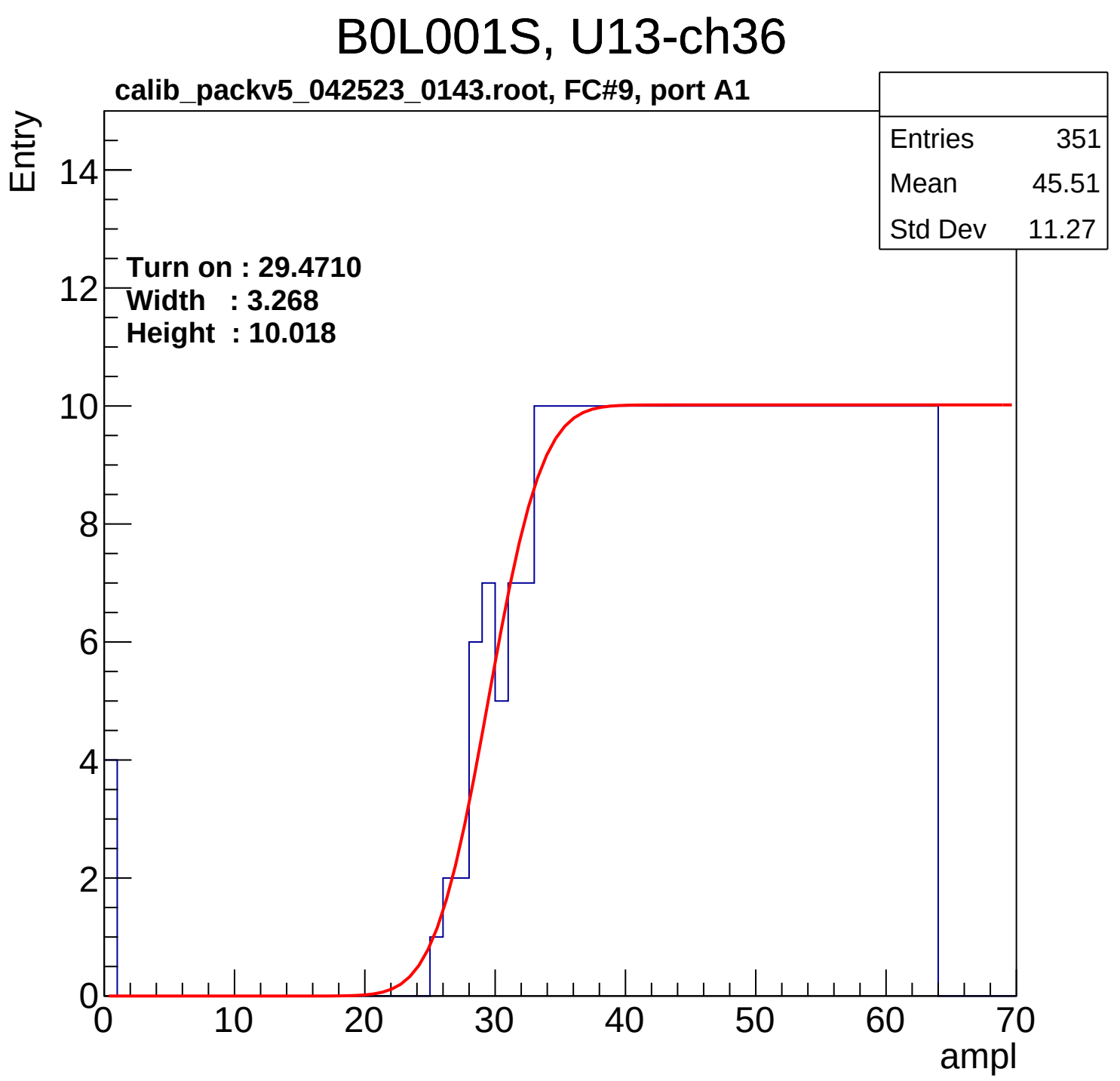
B0L001S, U13-ch36
calib_packv5_042523_0143.root, FC#9, port A1
Entries 351
Mean 45.51
Std Dev 11.27
Turn on : 29.4710
Width : 3.268
Height : 10.018
Entry
ampl
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4
6
8
10
12
14
0
10
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60
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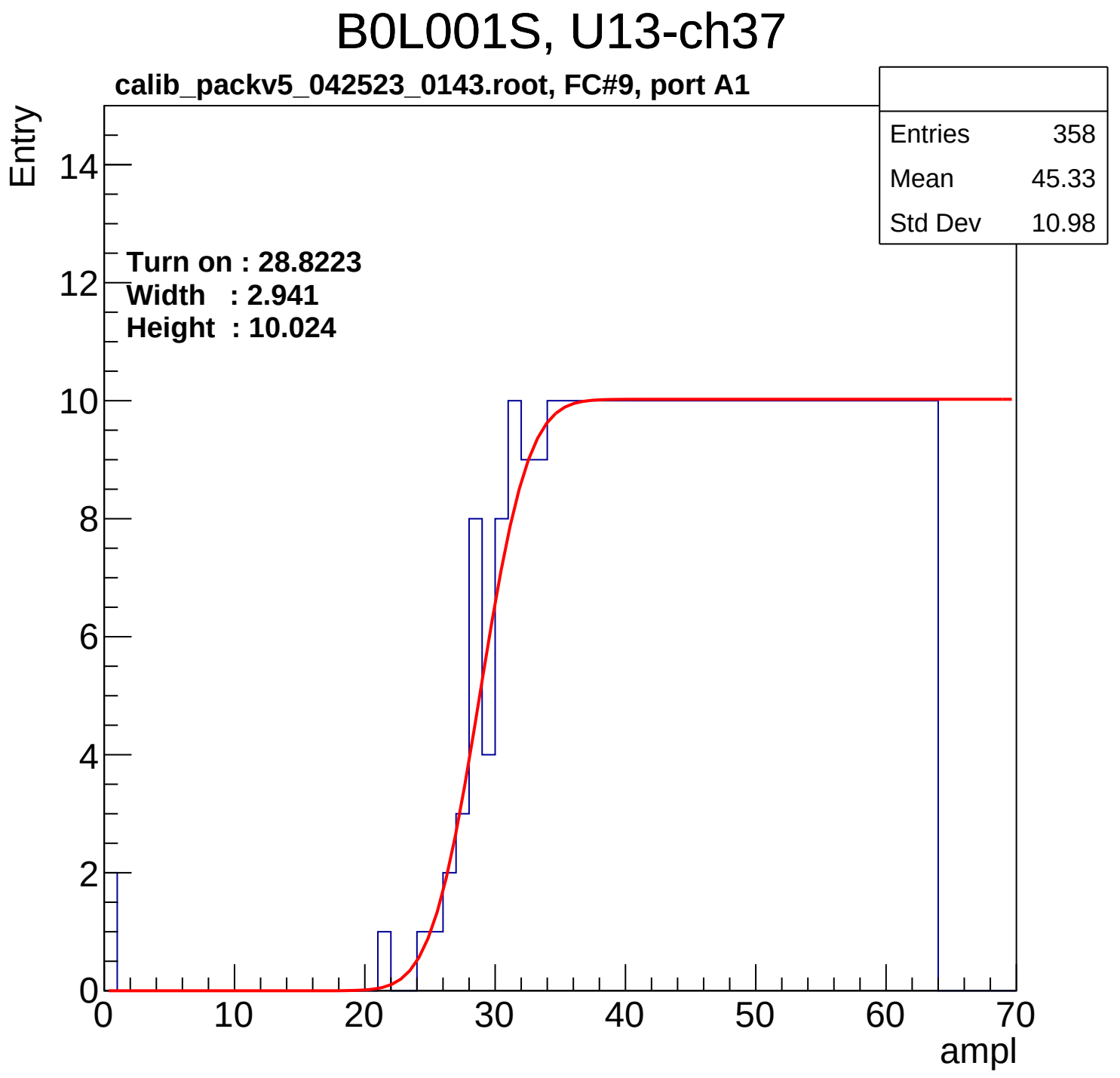
B0L001S, U13-ch37
calib_packv5_042523_0143.root, FC#9, port A1
Entries 358
Mean 45.33
Std Dev 10.98
Turn on : 28.8223
Width : 2.941
Height : 10.024
Entry
ampl
0
2
4
6
8
10
12
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0
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20
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60
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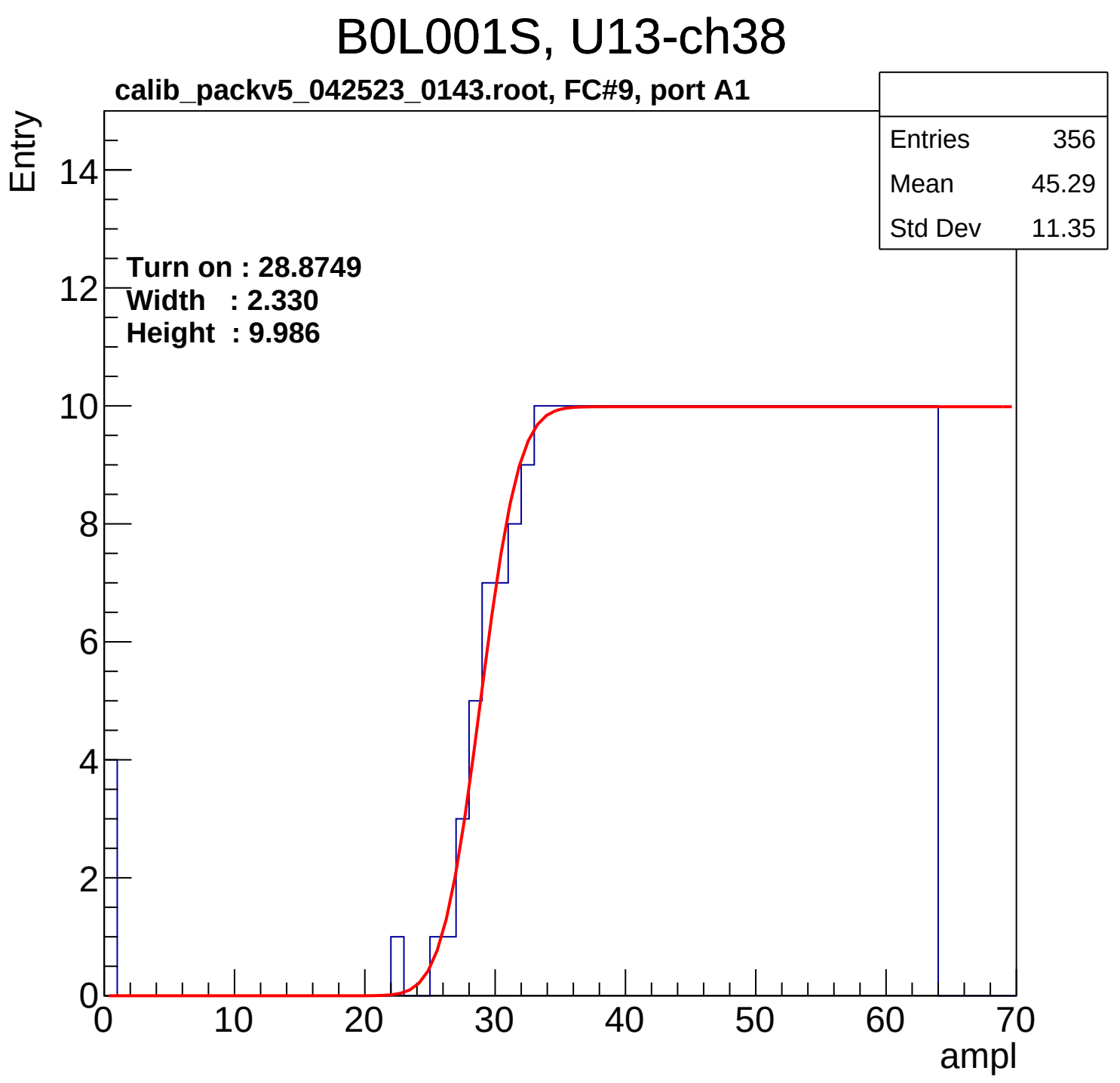
B0L001S, U13-ch38
calib_packv5_042523_0143.root, FC#9, port A1
Entries 356
Mean 45.29
Std Dev 11.35
Turn on : 28.8749
Width : 2.330
Height : 9.986
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
50
60
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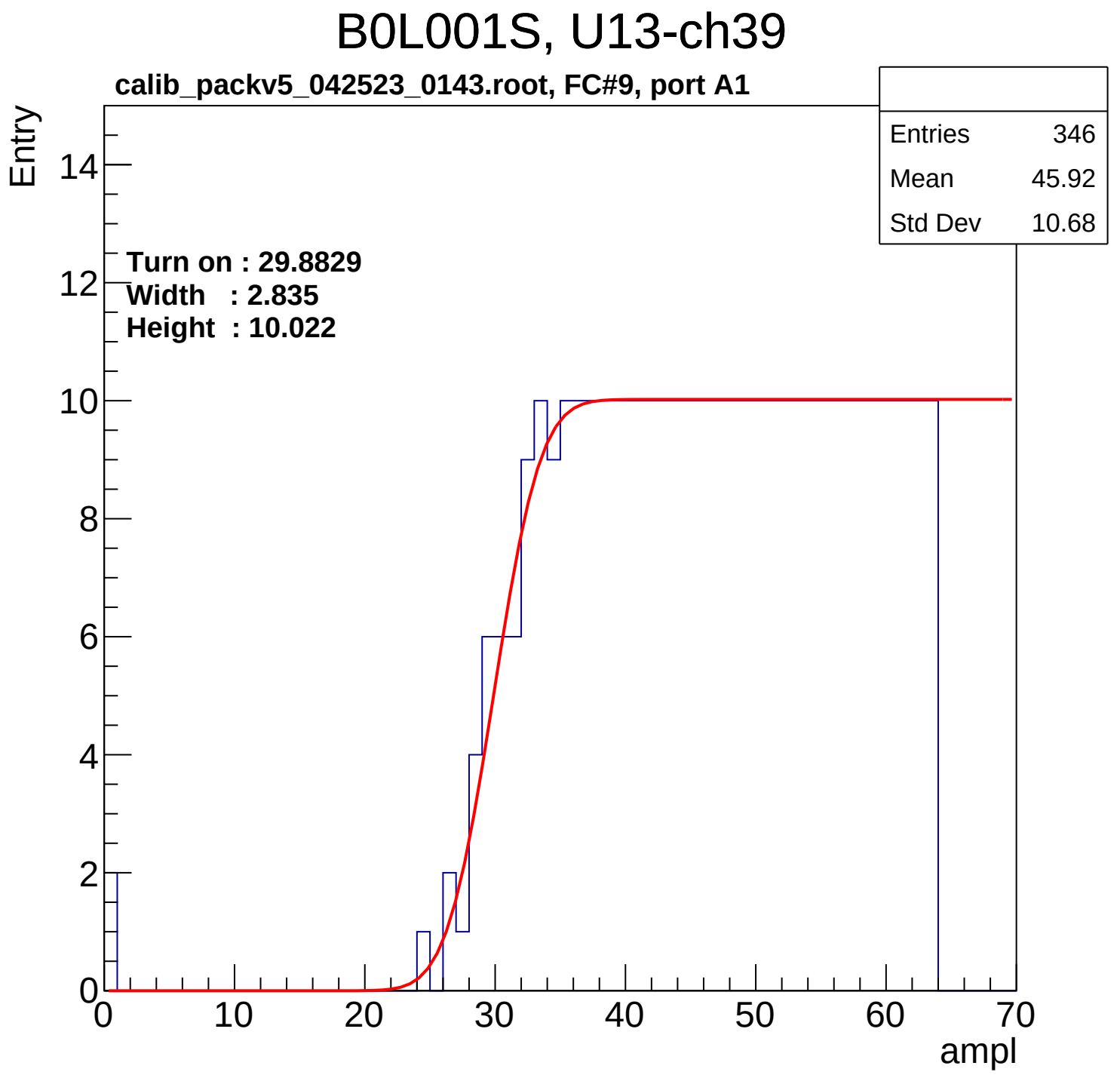
B0L001S, U13-ch39
calib_packv5_042523_0143.root, FC#9, port A1
Entries 346
Mean 45.92
Std Dev 10.68
Turn on : 29.8829
Width : 2.835
Height : 10.022
Entry
ampl
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4
6
8
10
12
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0
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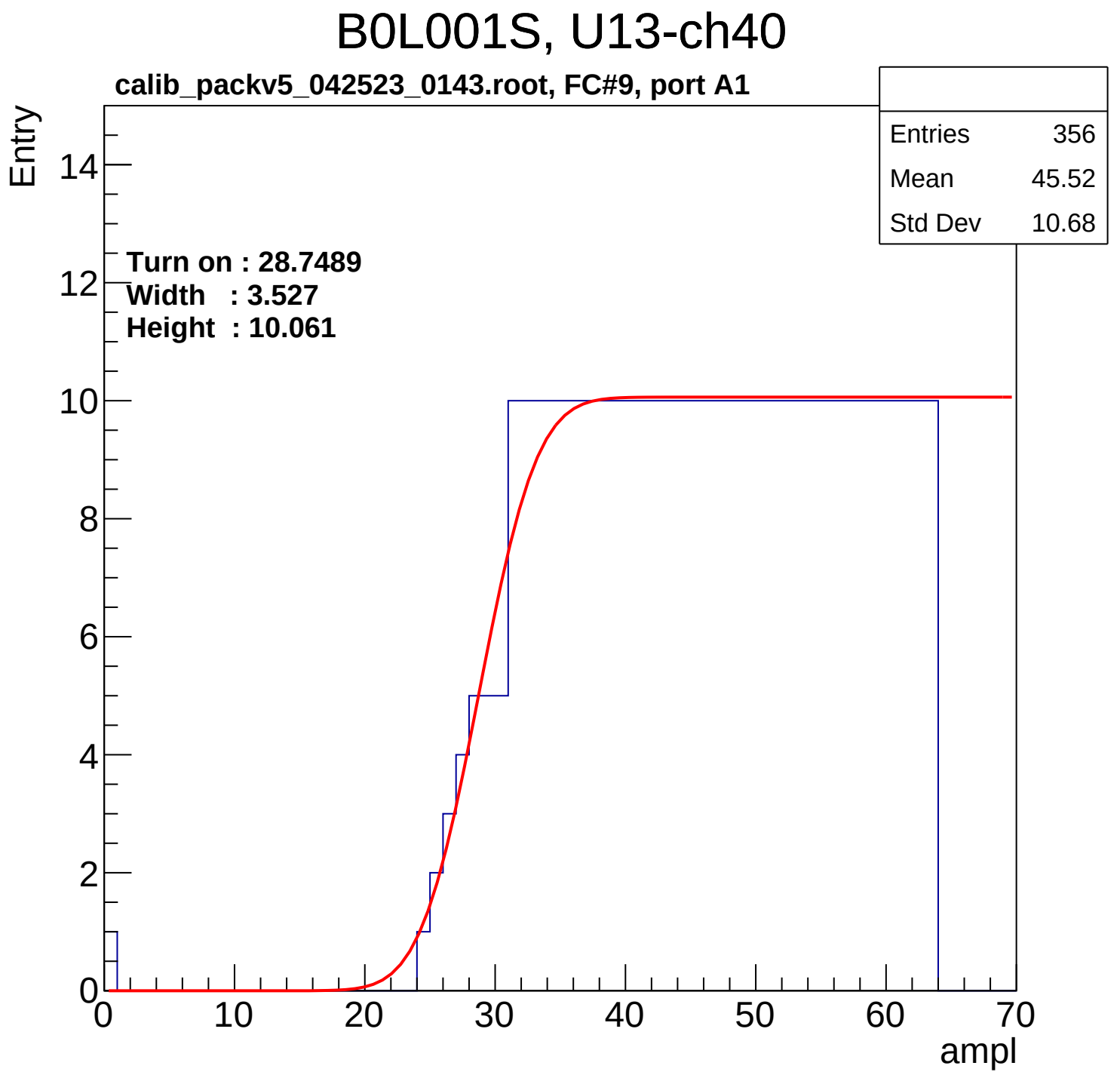
B0L001S, U13-ch40
calib_packv5_042523_0143.root, FC#9, port A1
Entries 356
Mean 45.52
Std Dev 10.68
Turn on : 28.7489
Width : 3.527
Height : 10.061
Entry
ampl
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2
4
6
8
10
12
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0
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20
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60
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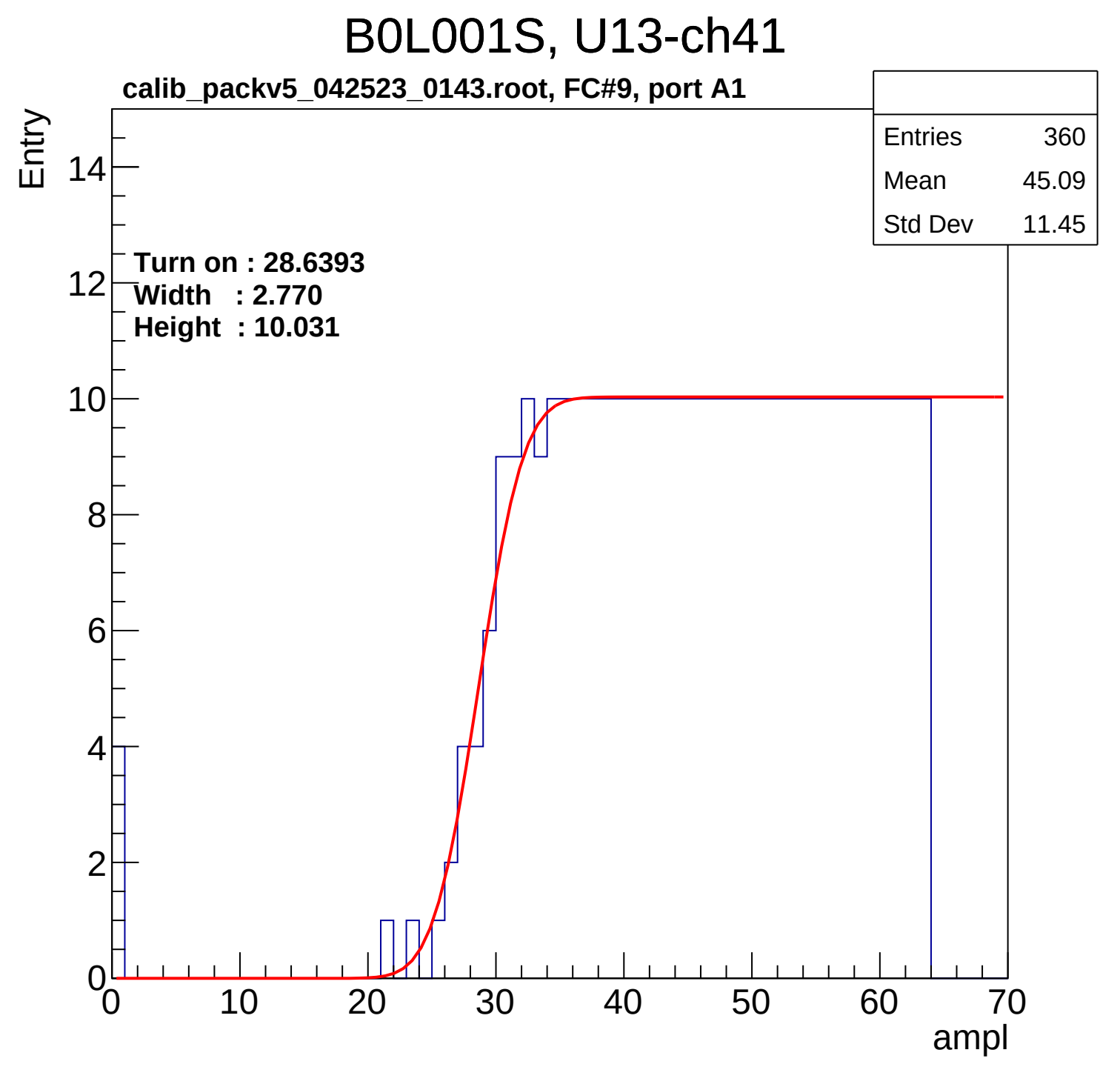
B0L001S, U13-ch41
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 45.09
Std Dev 11.45
Turn on : 28.6393
Width : 2.770
Height : 10.031
Entry
ampl
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6
8
10
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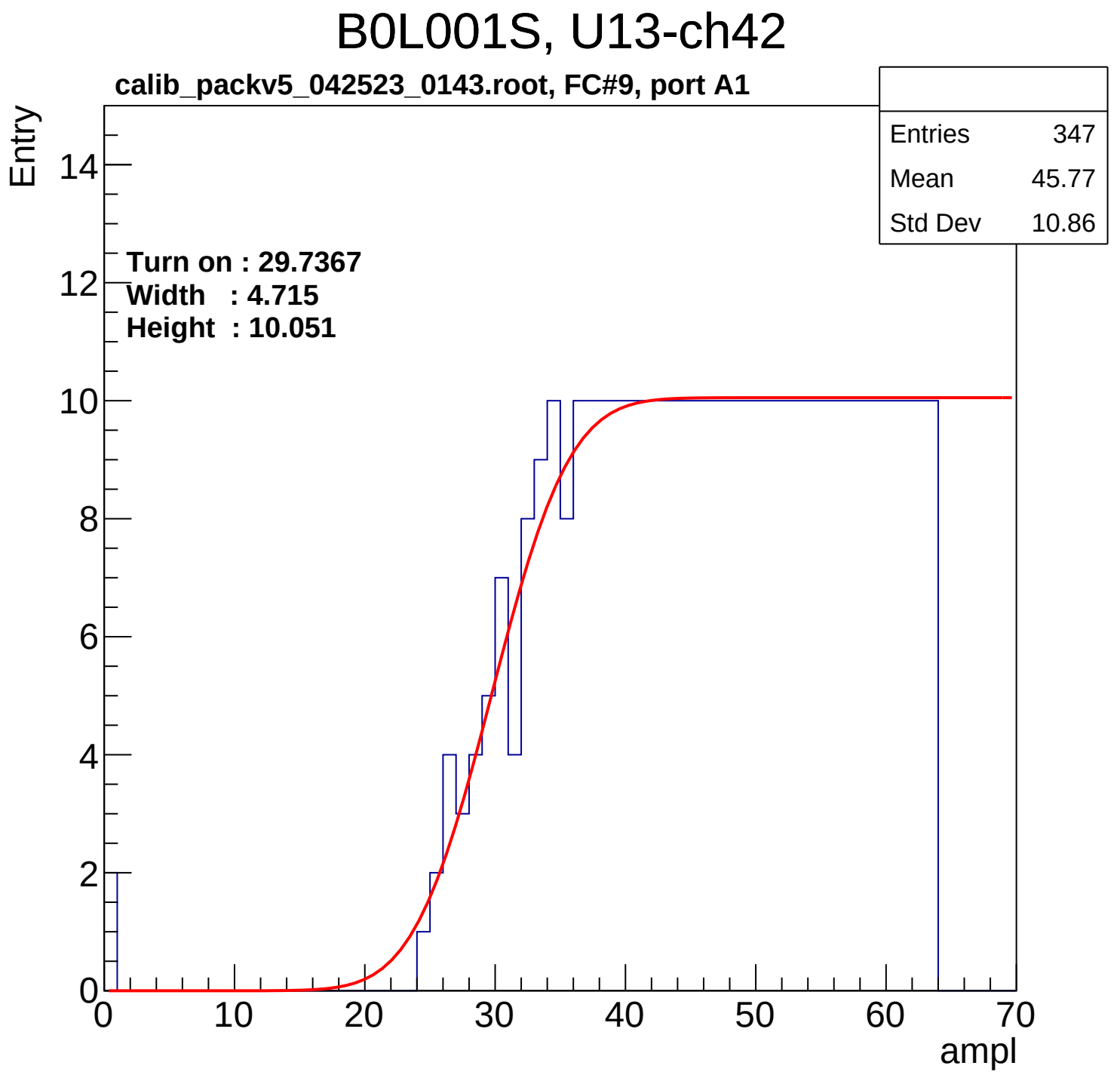
B0L001S, U13-ch42
calib_packv5_042523_0143.root, FC#9, port A1
Entries 347
Mean 45.77
Std Dev 10.86
Turn on : 29.7367
Width : 4.715
Height : 10.051
Entry
ampl
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2
4
6
8
10
12
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0
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60
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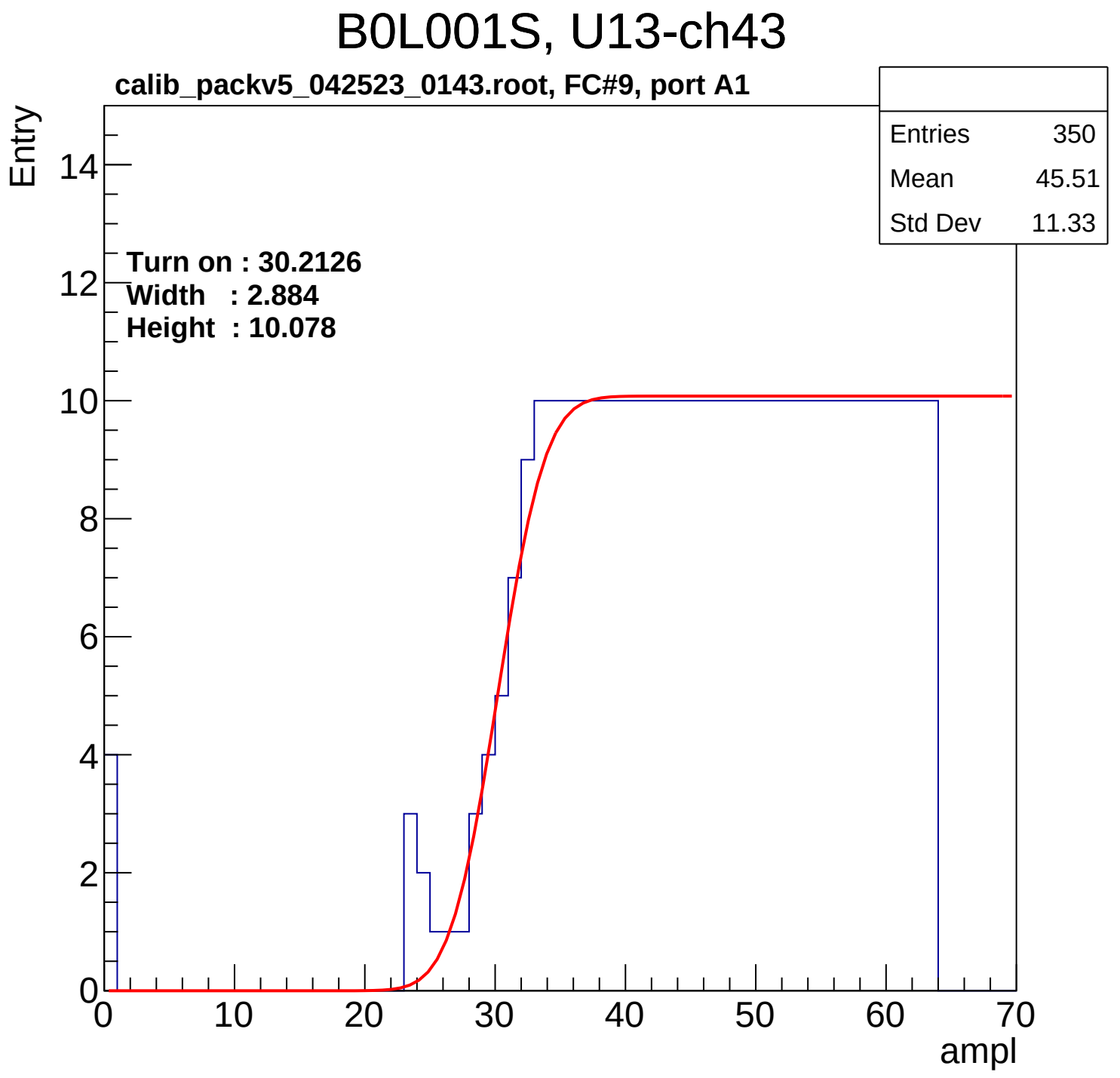
B0L001S, U13-ch43
calib_packv5_042523_0143.root, FC#9, port A1
Entries 350
Mean 45.51
Std Dev 11.33
Turn on : 30.2126
Width : 2.884
Height : 10.078
Entry
ampl
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6
8
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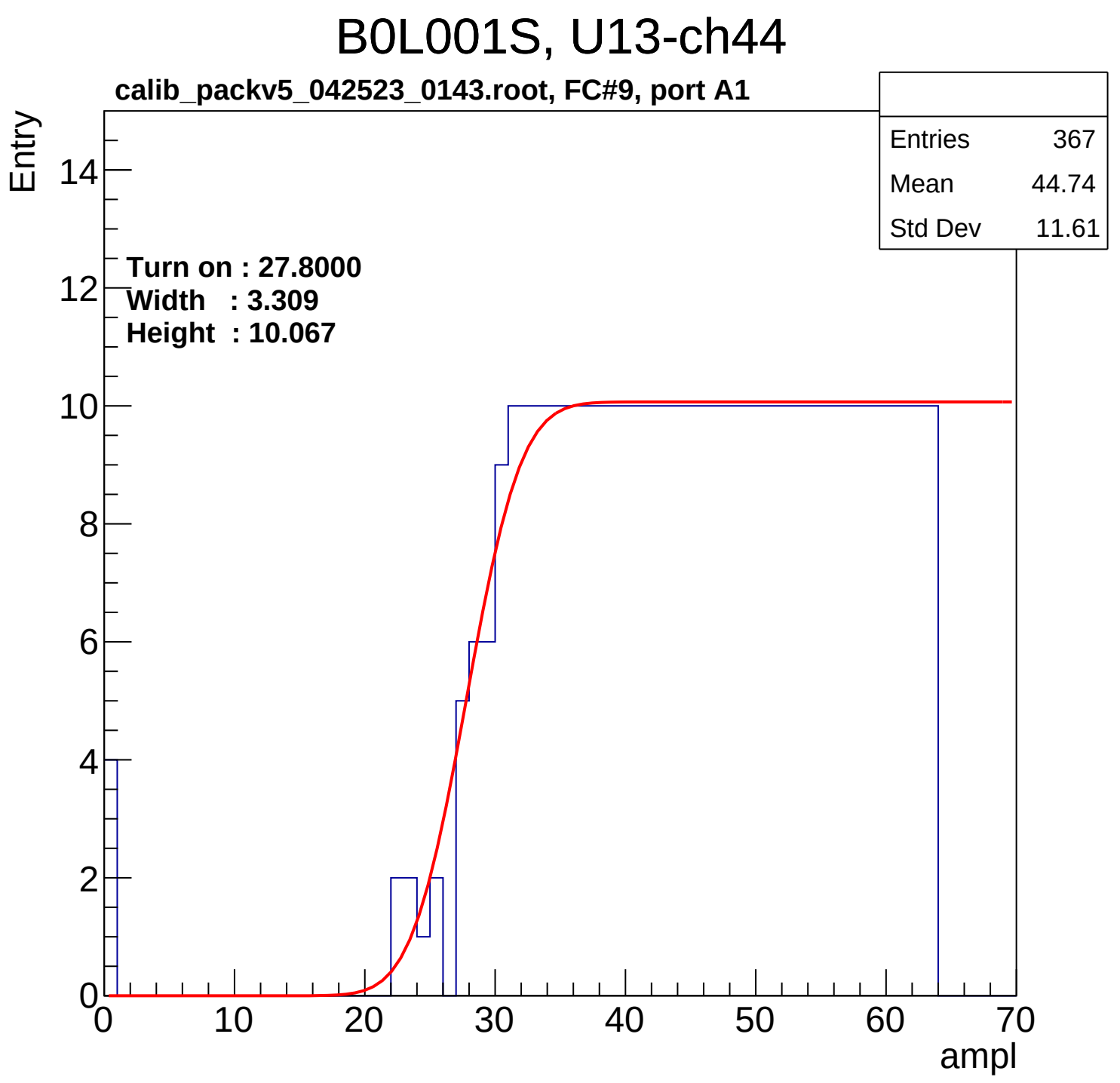
B0L001S, U13-ch44
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.74
Std Dev 11.61
Turn on : 27.8000
Width : 3.309
Height : 10.067
Entry
ampl
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6
8
10
12
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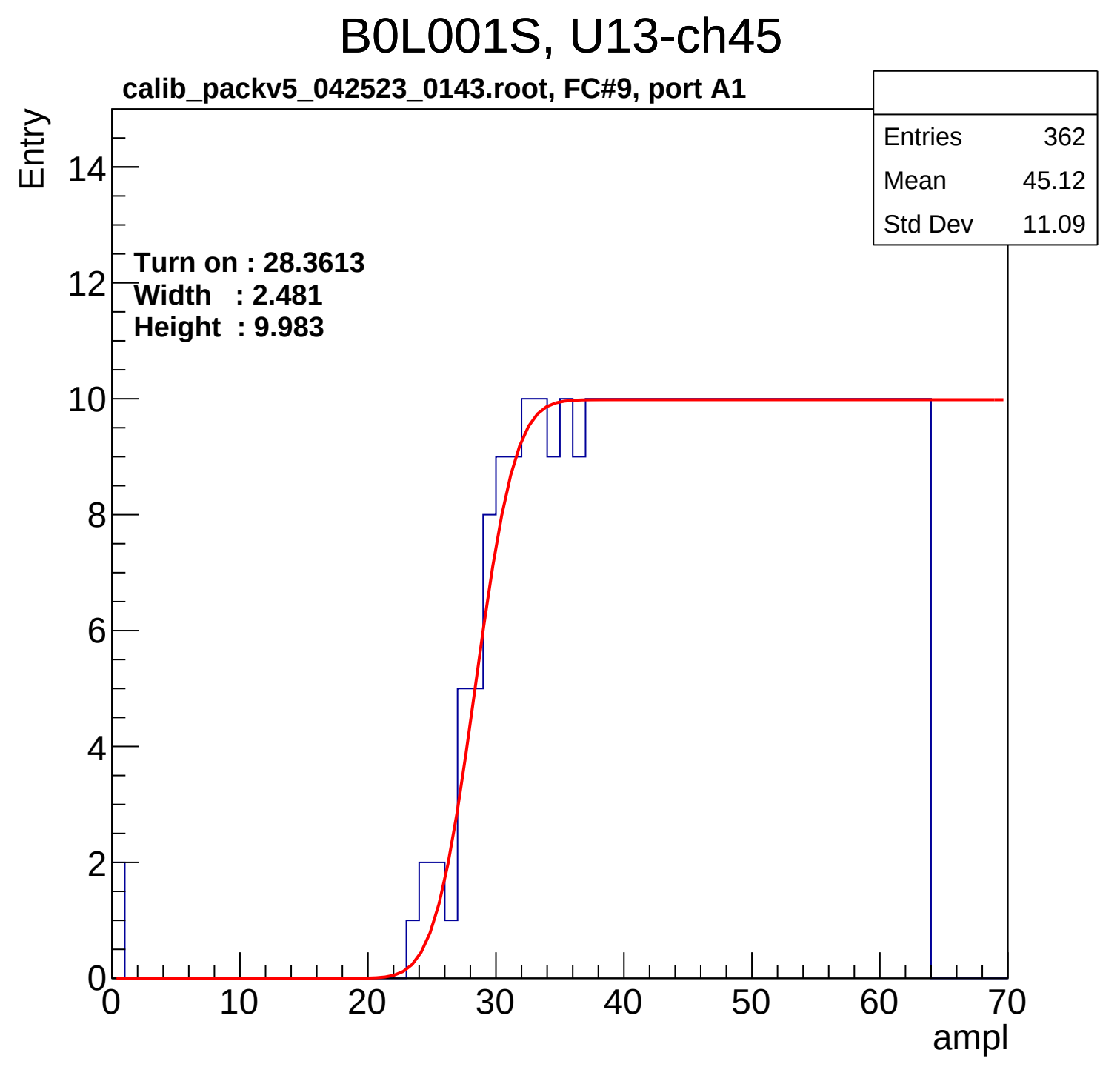
B0L001S, U13-ch45
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 45.12
Std Dev 11.09
Turn on : 28.3613
Width : 2.481
Height : 9.983
Entry
ampl
0
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6
8
10
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0
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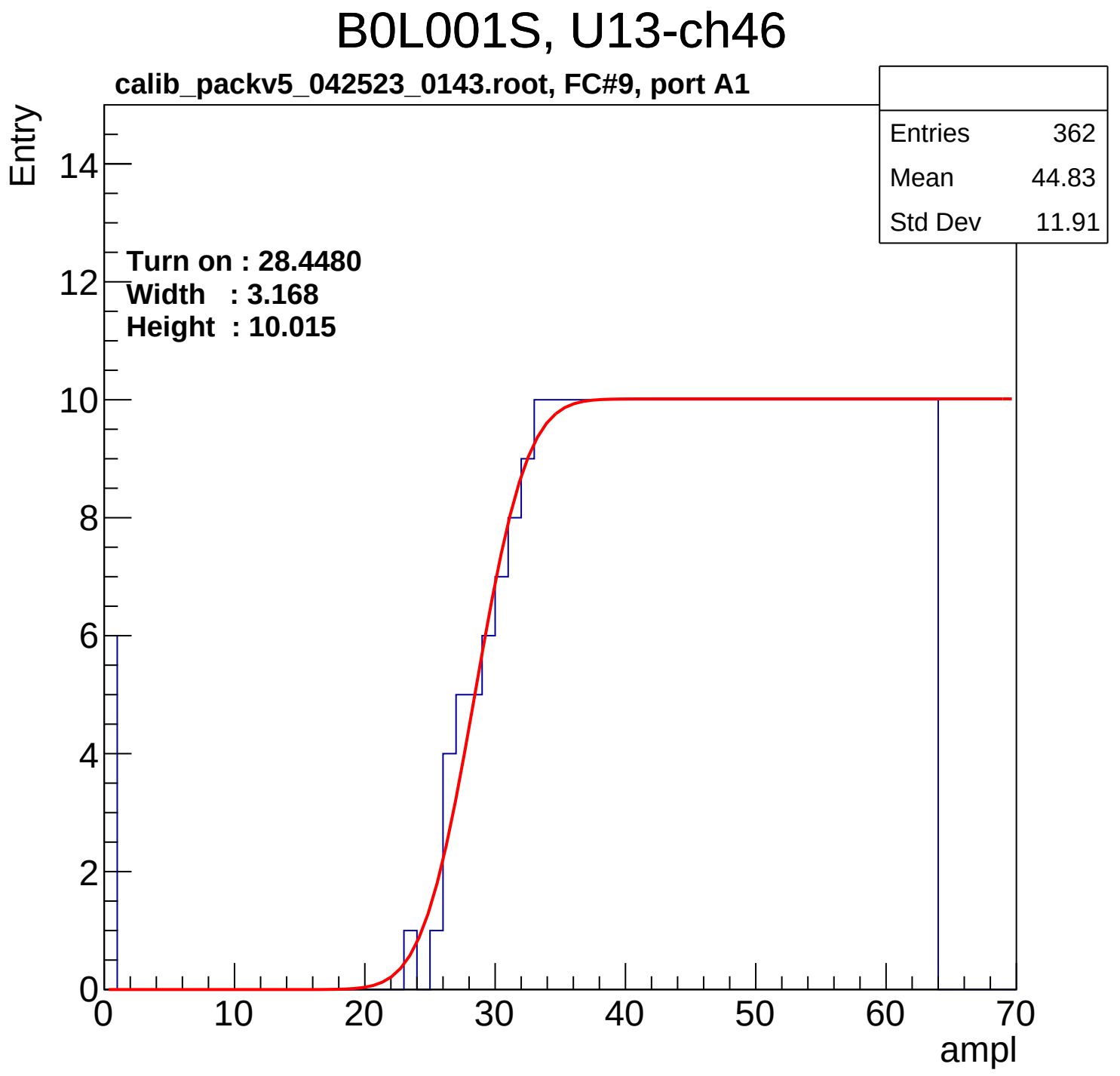
B0L001S, U13-ch46
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 44.83
Std Dev 11.91
Turn on : 28.4480
Width : 3.168
Height : 10.015
Entry
ampl
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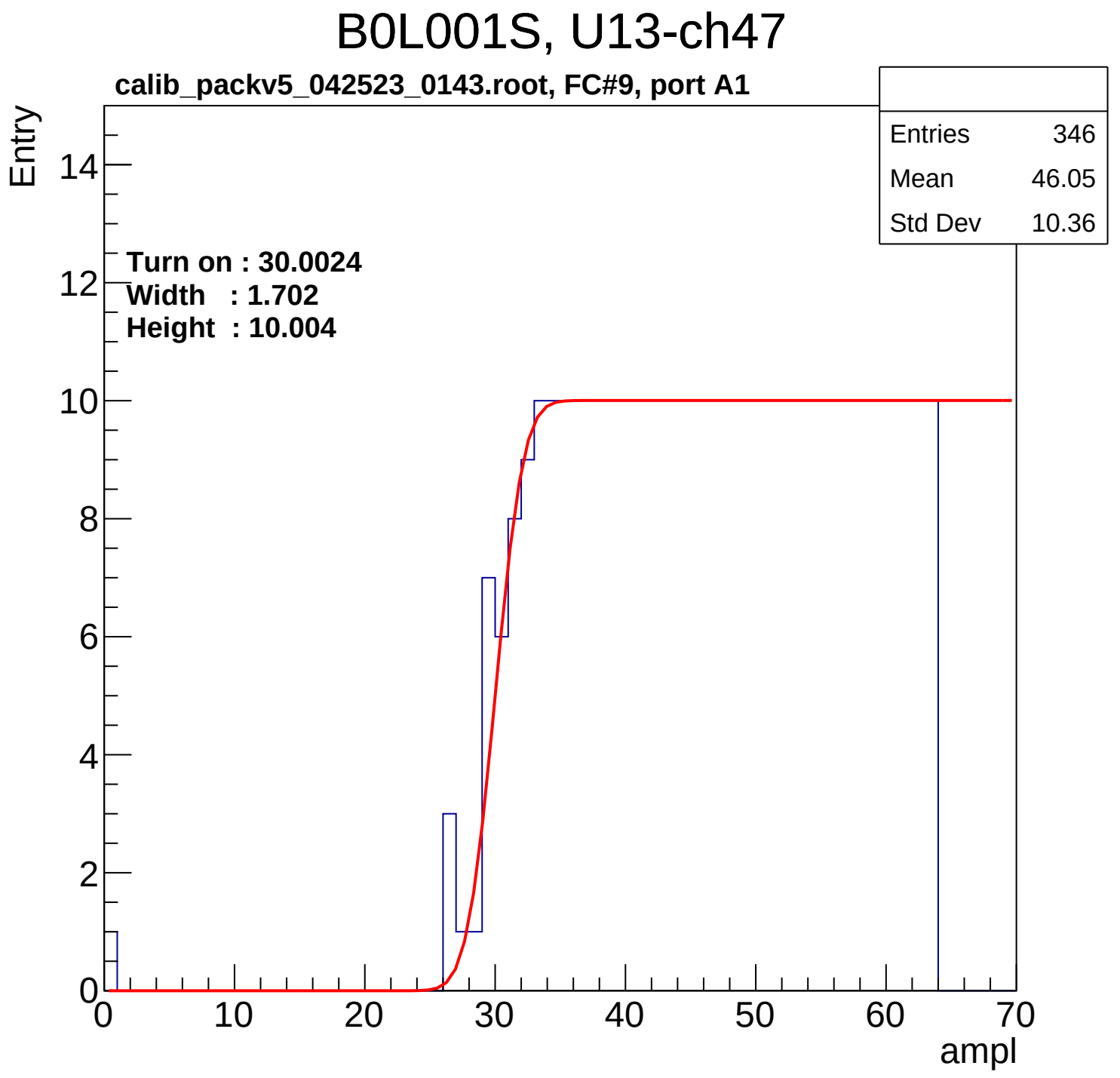
B0L001S, U13-ch47
calib_packv5_042523_0143.root, FC#9, port A1
Entries 346
Mean 46.05
Std Dev 10.36
Turn on : 30.0024
Width : 1.702
Height : 10.004
Entry
ampl
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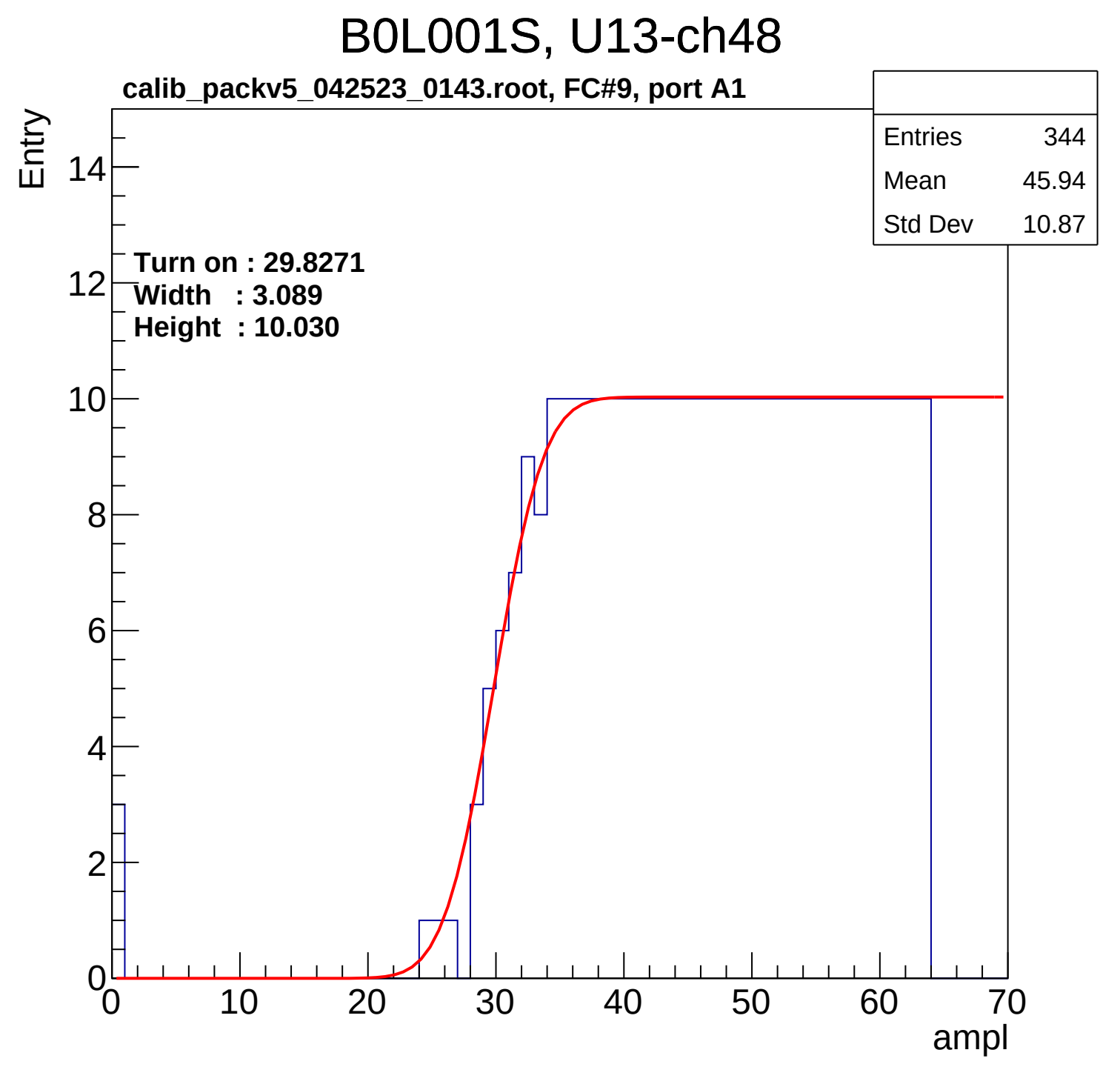
B0L001S, U13-ch48
calib_packv5_042523_0143.root, FC#9, port A1
Entries 344
Mean 45.94
Std Dev 10.87
Turn on : 29.8271
Width : 3.089
Height : 10.030
Entry
ampl
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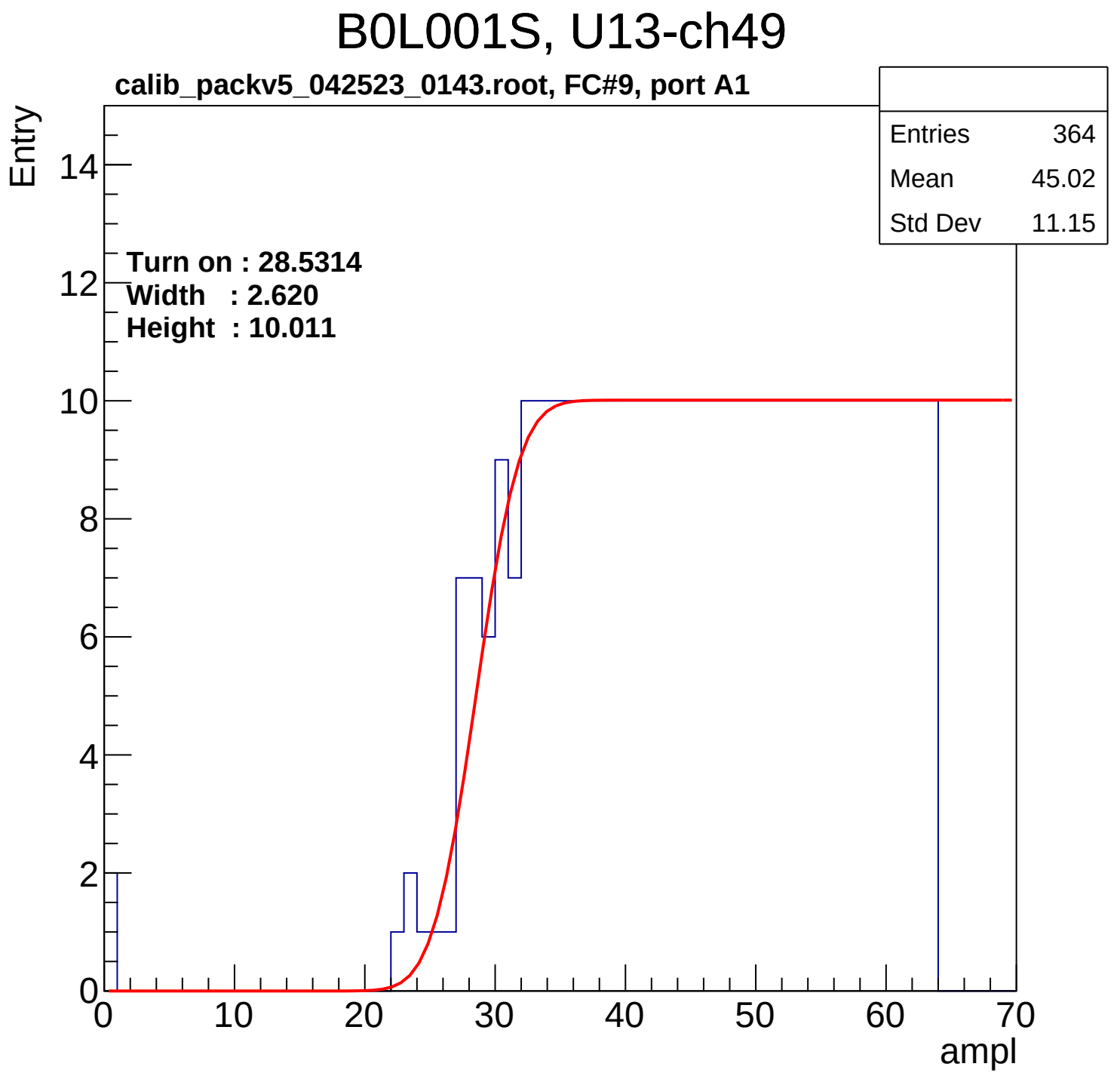
B0L001S, U13-ch49
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 45.02
Std Dev 11.15
Turn on : 28.5314
Width : 2.620
Height : 10.011
Entry
ampl
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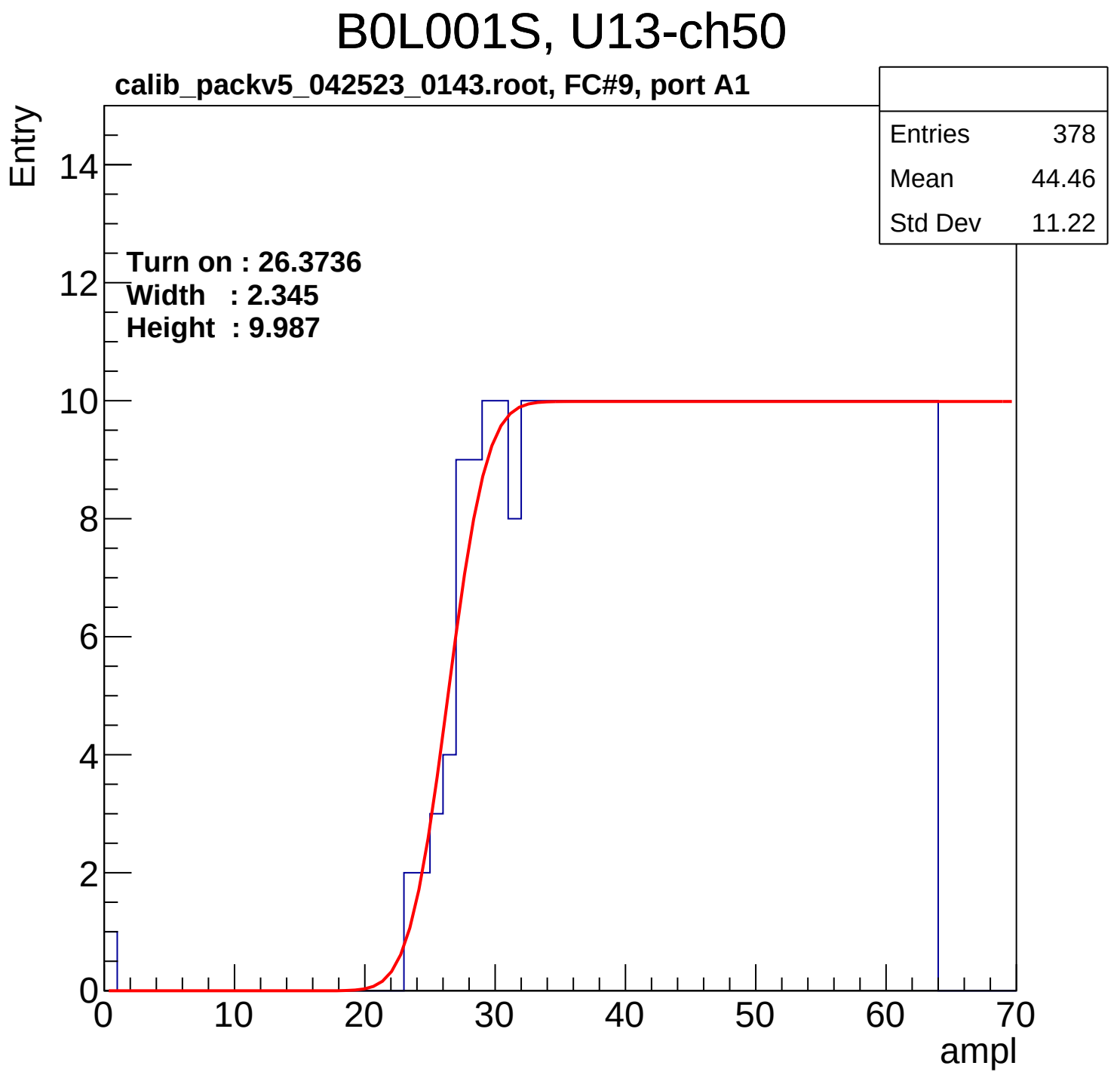
B0L001S, U13-ch50
calib_packv5_042523_0143.root, FC#9, port A1
Entries 378
Mean 44.46
Std Dev 11.22
Turn on : 26.3736
Width : 2.345
Height : 9.987
Entry
ampl
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8
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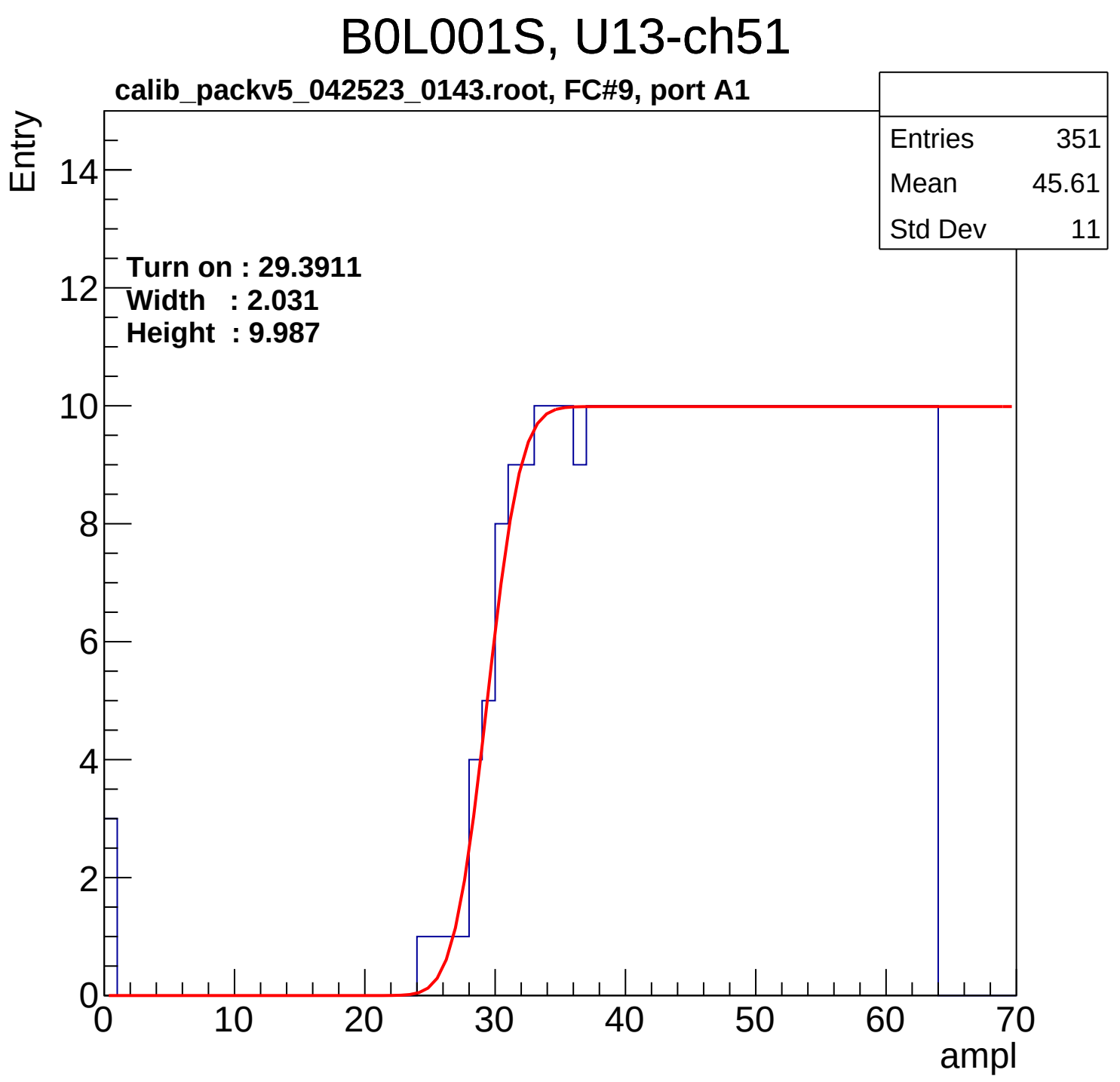
B0L001S, U13-ch51
calib_packv5_042523_0143.root, FC#9, port A1
Entries 351
Mean 45.61
Std Dev 11
Turn on : 29.3911
Width : 2.031
Height : 9.987
Entry
ampl
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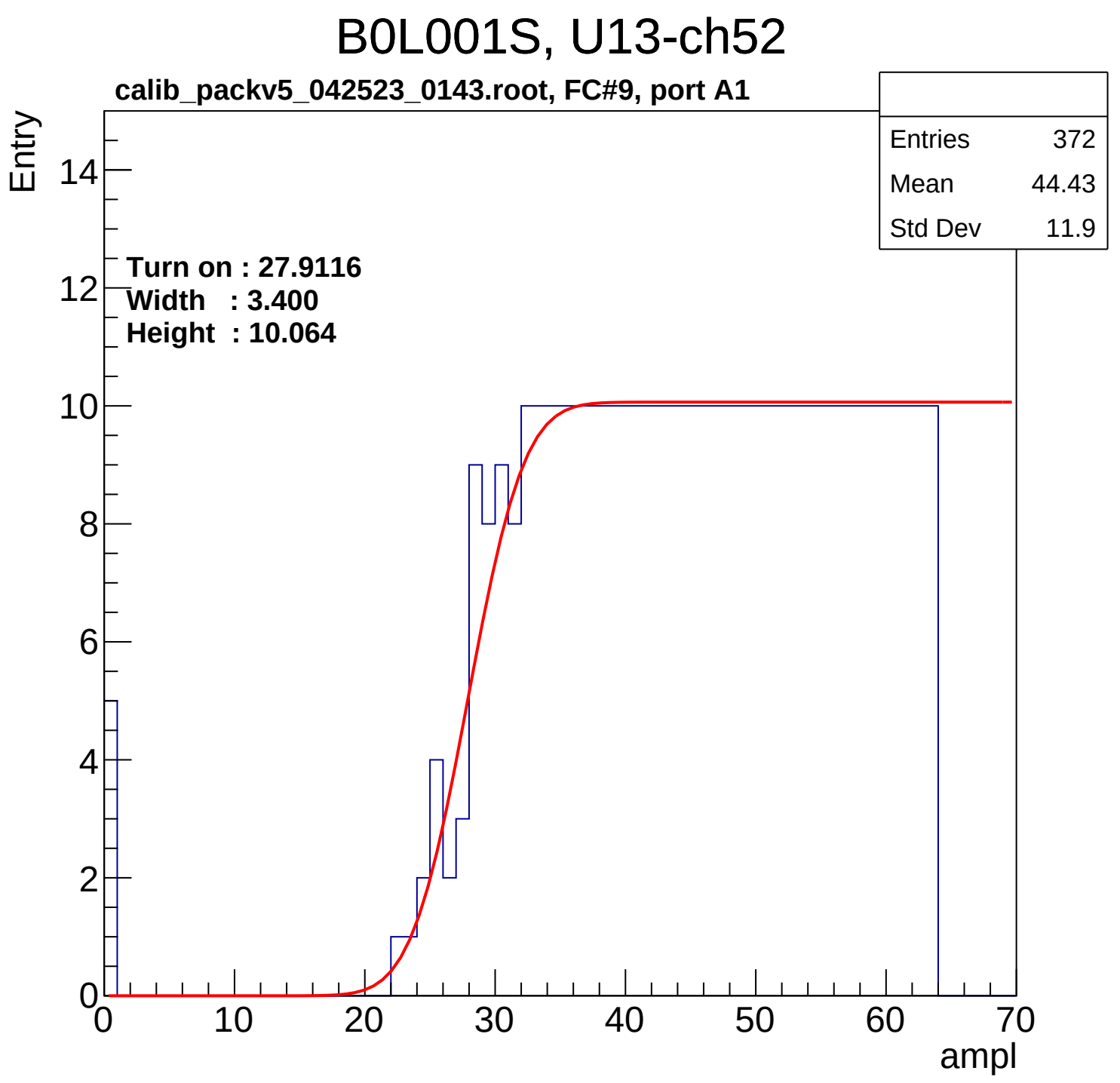
B0L001S, U13-ch52
calib_packv5_042523_0143.root, FC#9, port A1
Entries 372
Mean 44.43
Std Dev 11.9
Turn on : 27.9116
Width : 3.400
Height : 10.064
Entry
ampl
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8
10
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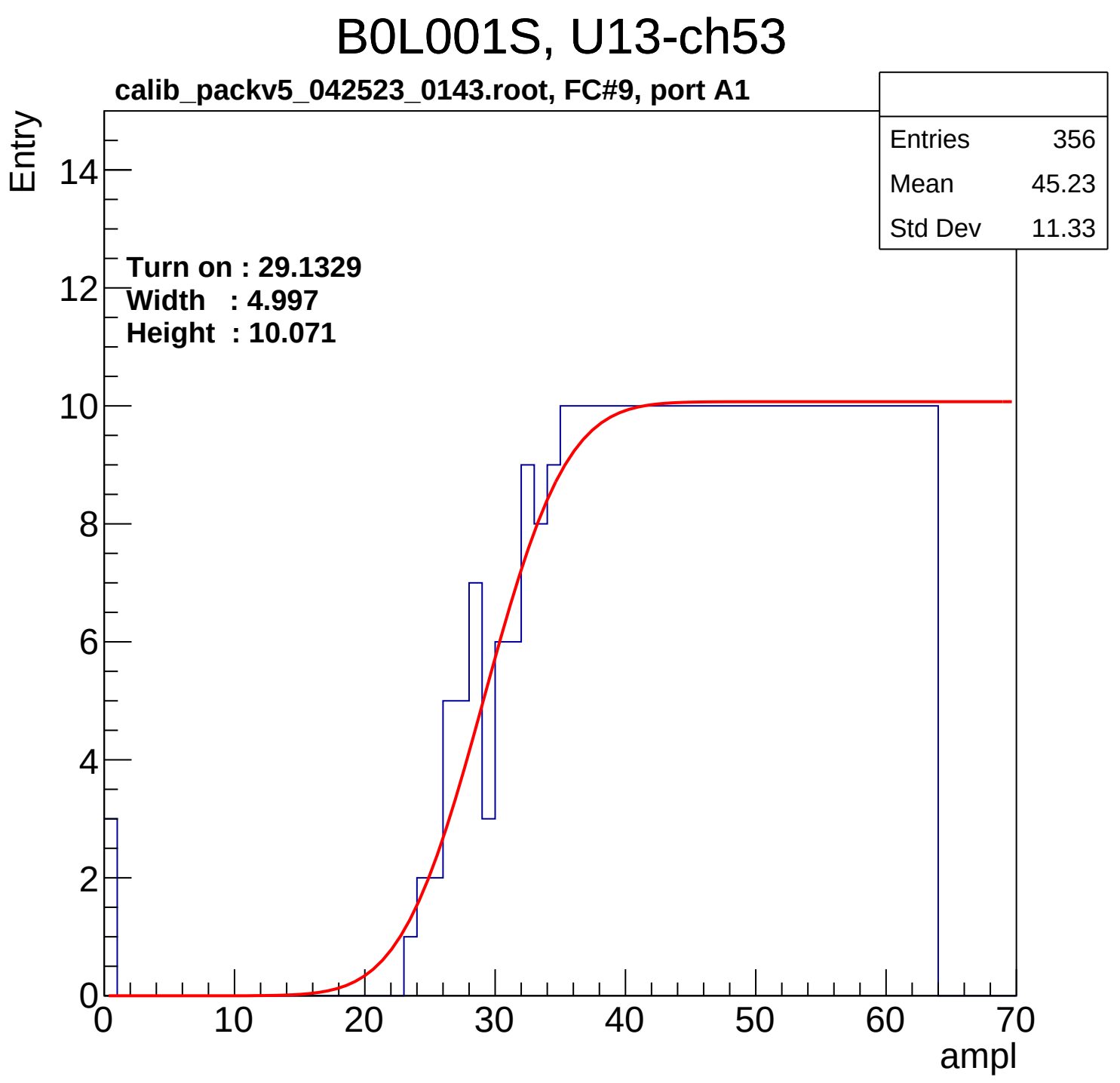
B0L001S, U13-ch53
calib_packv5_042523_0143.root, FC#9, port A1
Entries 356
Mean 45.23
Std Dev 11.33
Turn on : 29.1329
Width : 4.997
Height : 10.071
Entry
ampl
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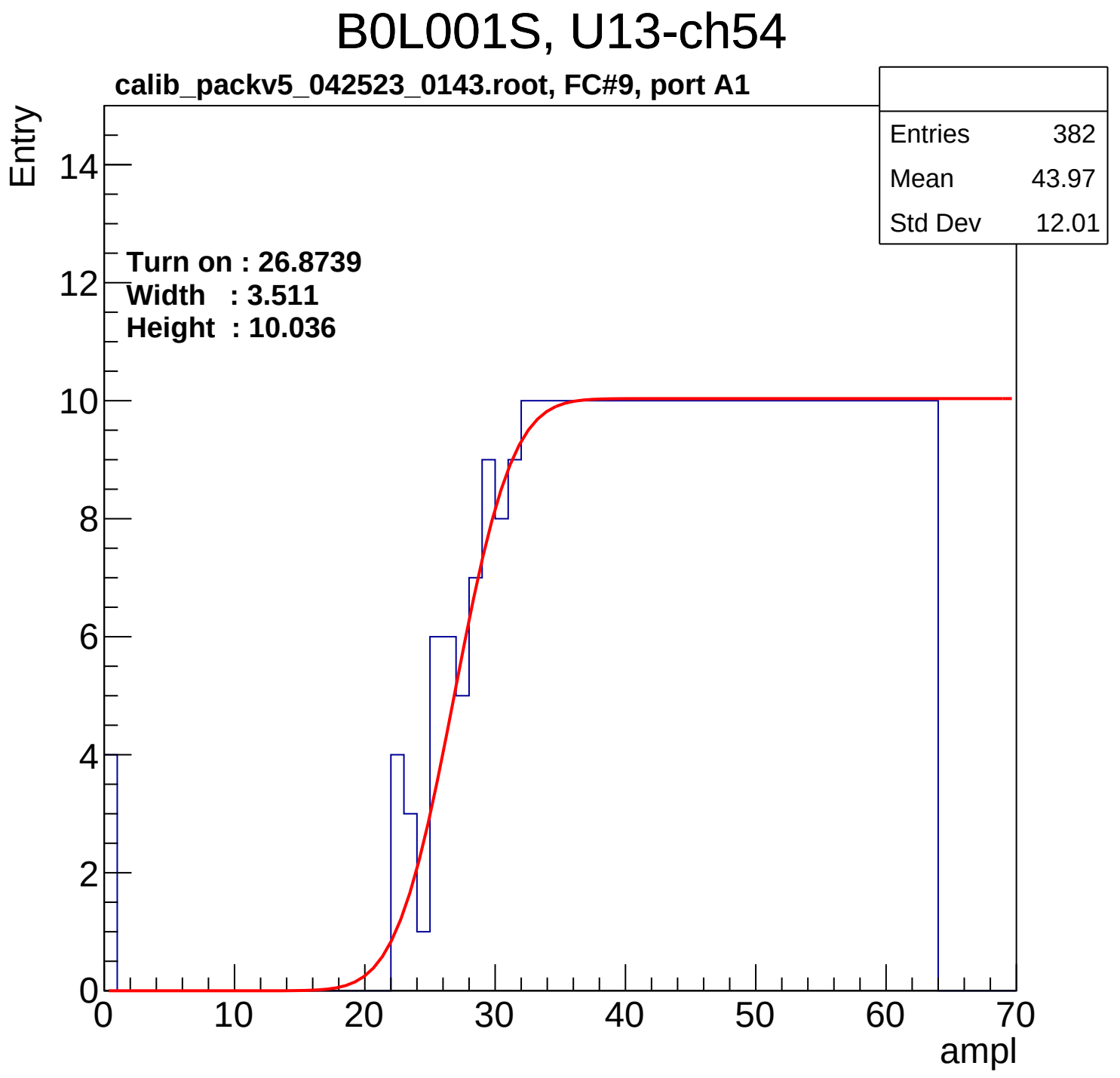
B0L001S, U13-ch54
calib_packv5_042523_0143.root, FC#9, port A1
Entries 382
Mean 43.97
Std Dev 12.01
Turn on : 26.8739
Width : 3.511
Height : 10.036
Entry
ampl
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4
6
8
10
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0
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20
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60
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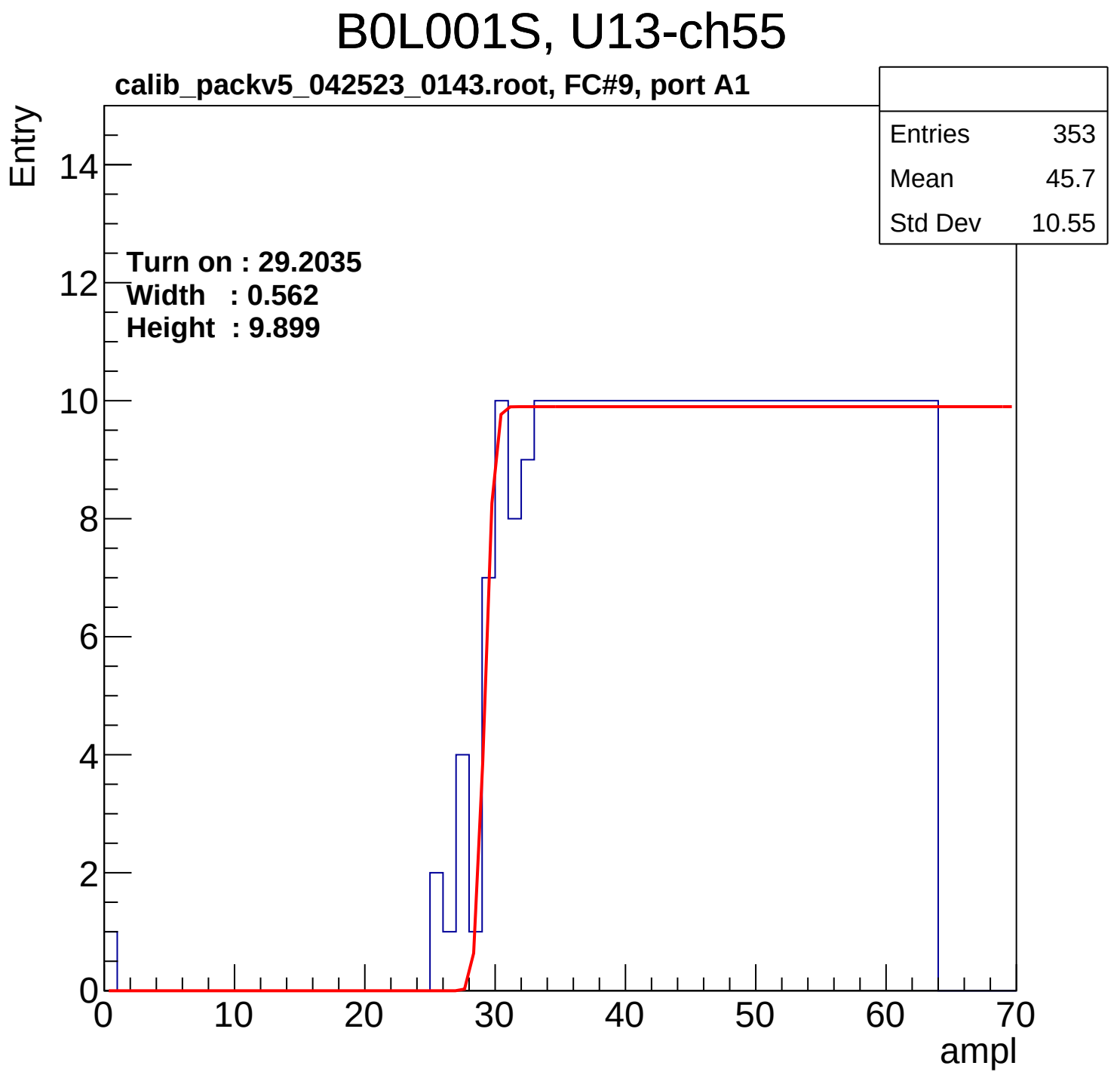
B0L001S, U13-ch55
calib_packv5_042523_0143.root, FC#9, port A1
Entries 353
Mean 45.7
Std Dev 10.55
Turn on : 29.2035
Width : 0.562
Height : 9.899
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ampl
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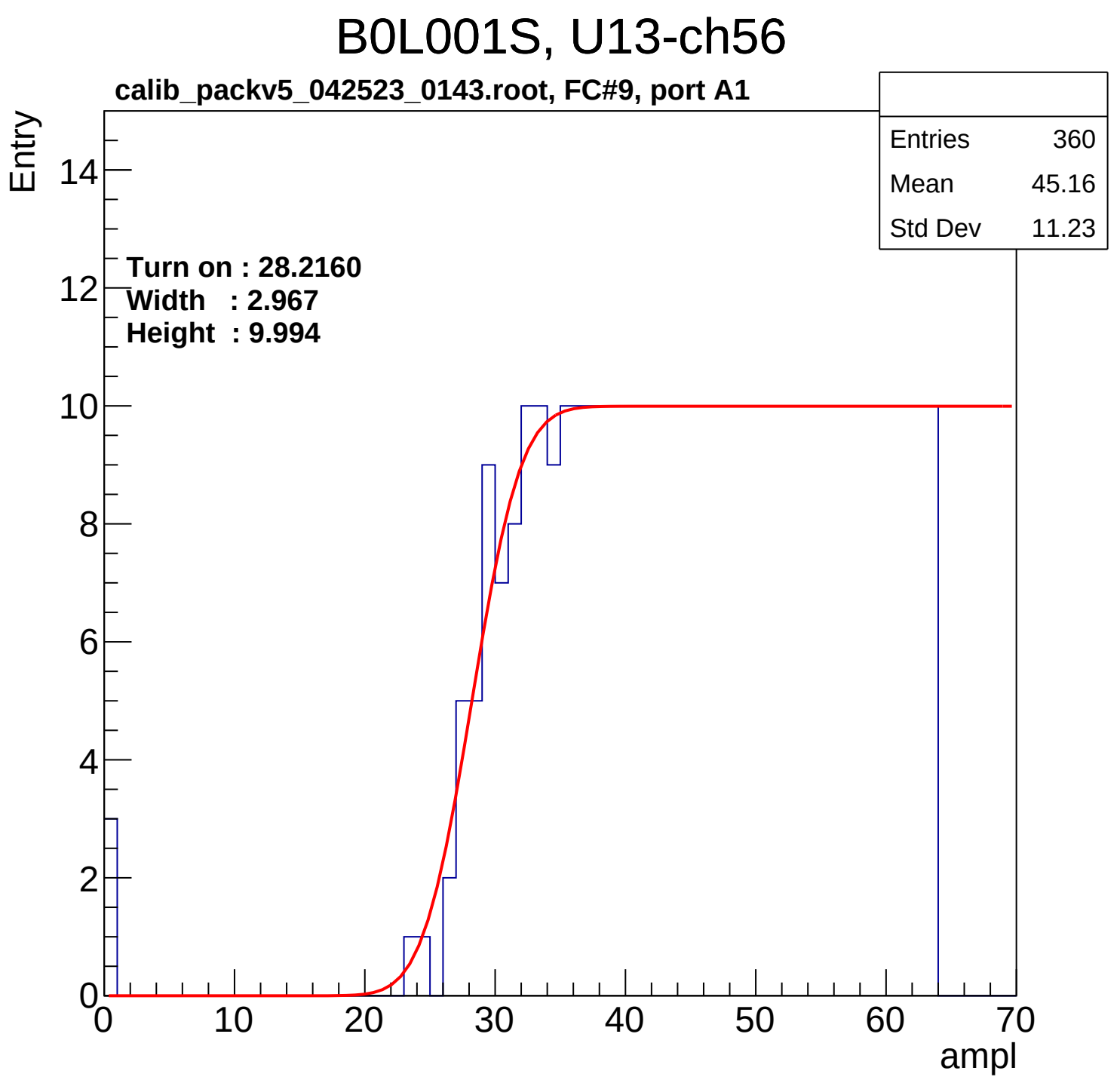
B0L001S, U13-ch56
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 45.16
Std Dev 11.23
Turn on : 28.2160
Width : 2.967
Height : 9.994
Entry
ampl
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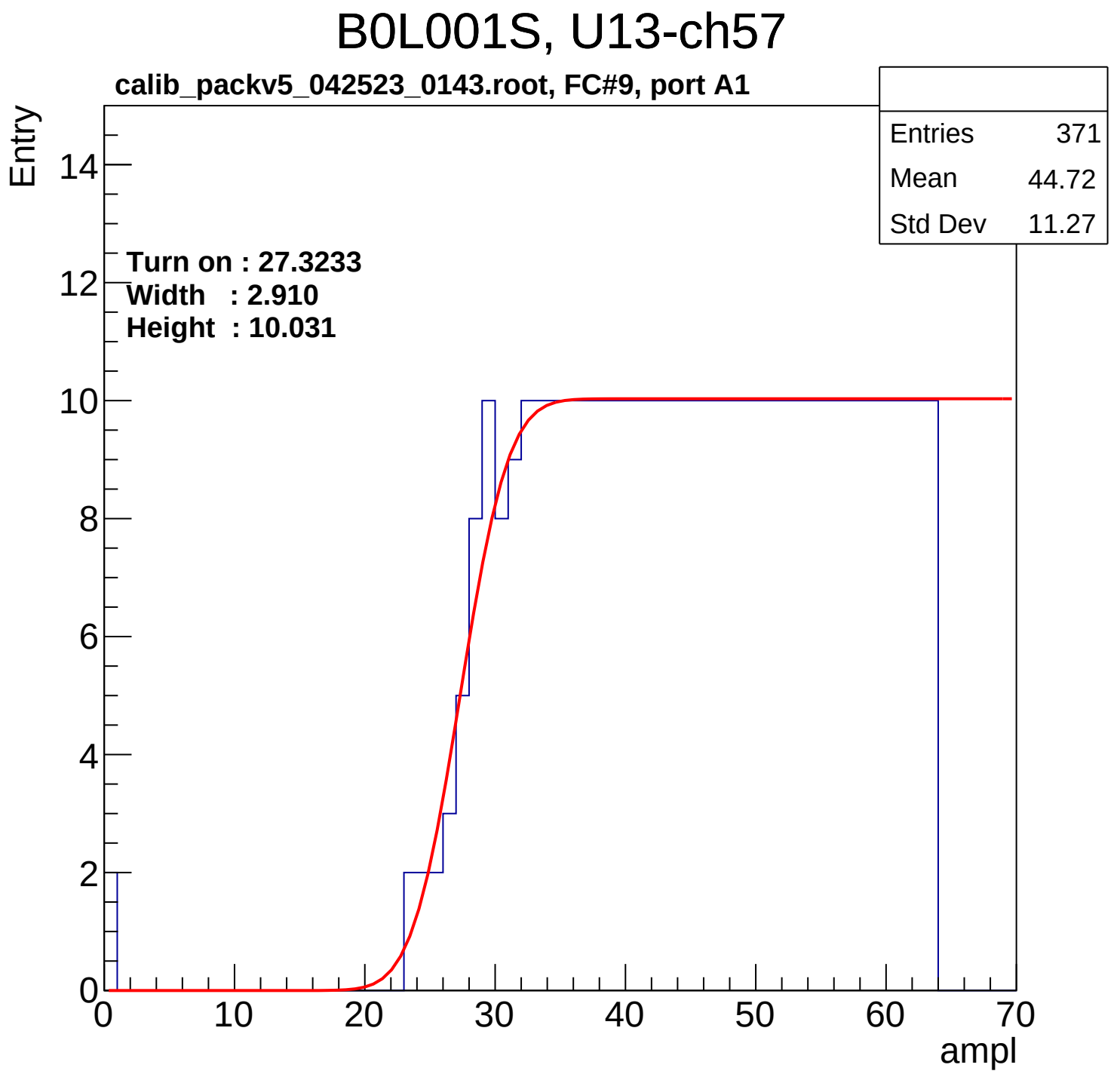
B0L001S, U13-ch57
calib_packv5_042523_0143.root, FC#9, port A1
Entries 371
Mean 44.72
Std Dev 11.27
Turn on : 27.3233
Width : 2.910
Height : 10.031
Entry
ampl
0
2
4
6
8
10
12
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10
20
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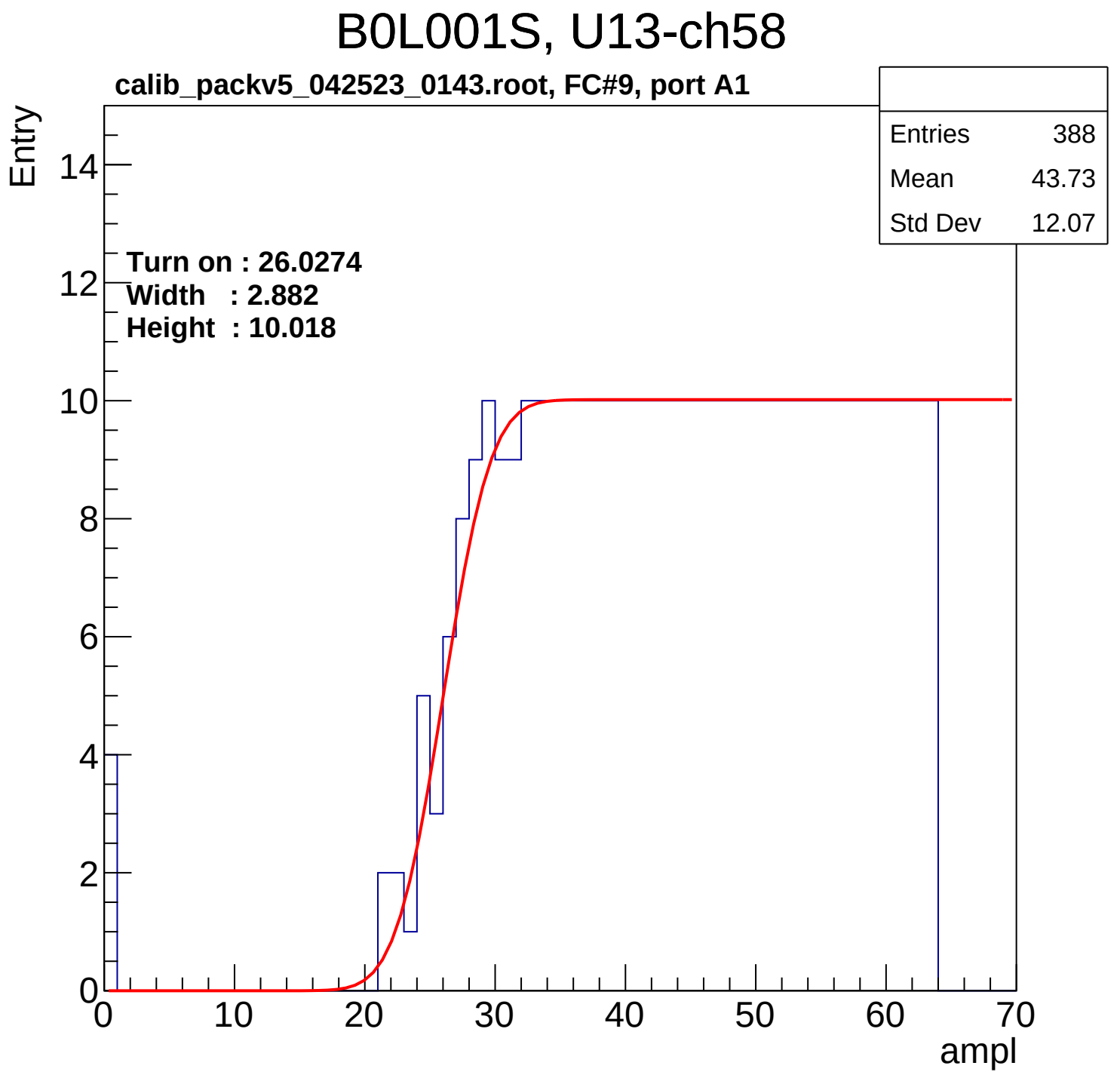
B0L001S, U13-ch58
calib_packv5_042523_0143.root, FC#9, port A1
Entries 388
Mean 43.73
Std Dev 12.07
Turn on : 26.0274
Width : 2.882
Height : 10.018
Entry
ampl
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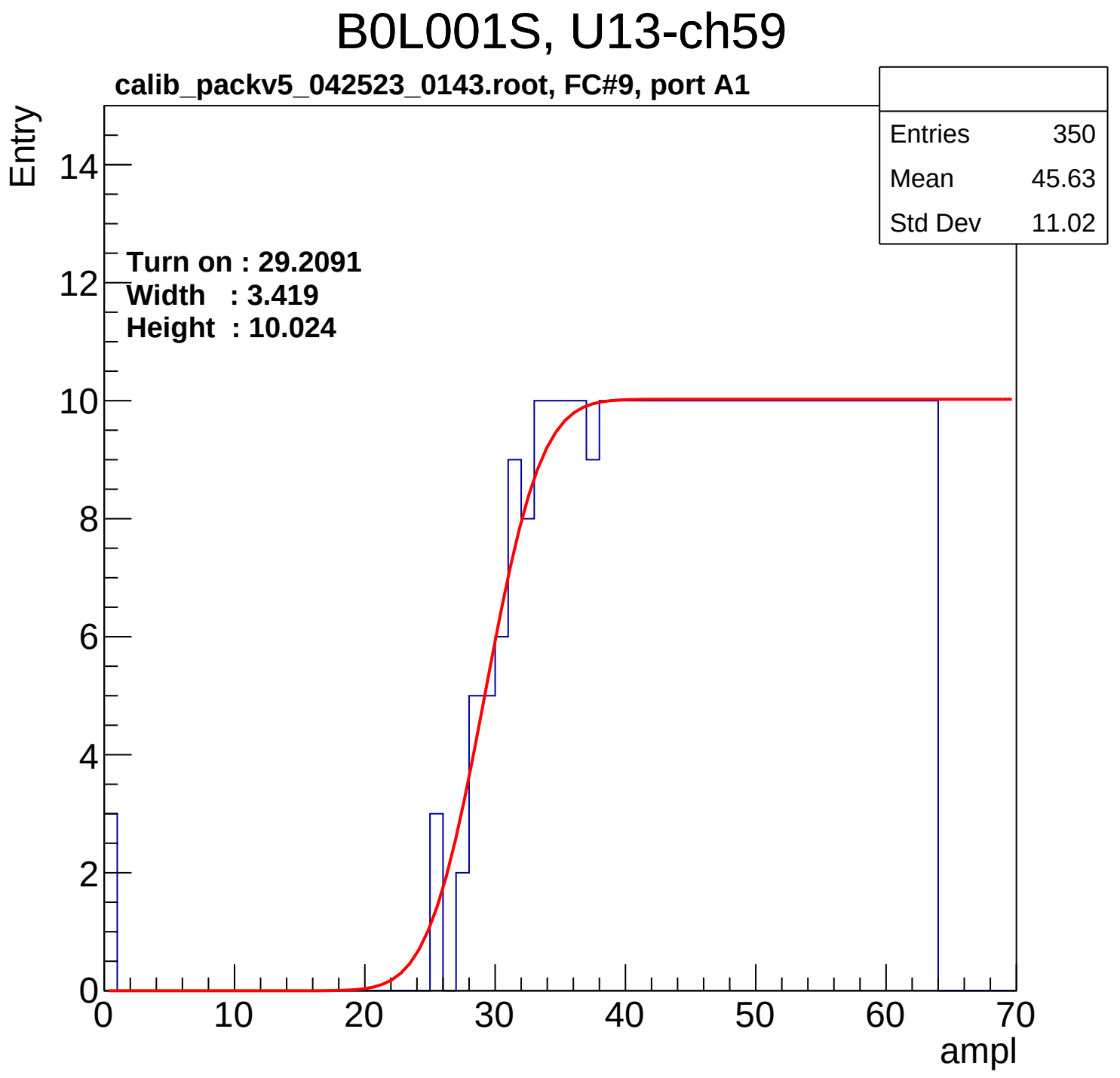
B0L001S, U13-ch59
calib_packv5_042523_0143.root, FC#9, port A1
Entries 350
Mean 45.63
Std Dev 11.02
Turn on : 29.2091
Width : 3.419
Height : 10.024
Entry
ampl
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2
4
6
8
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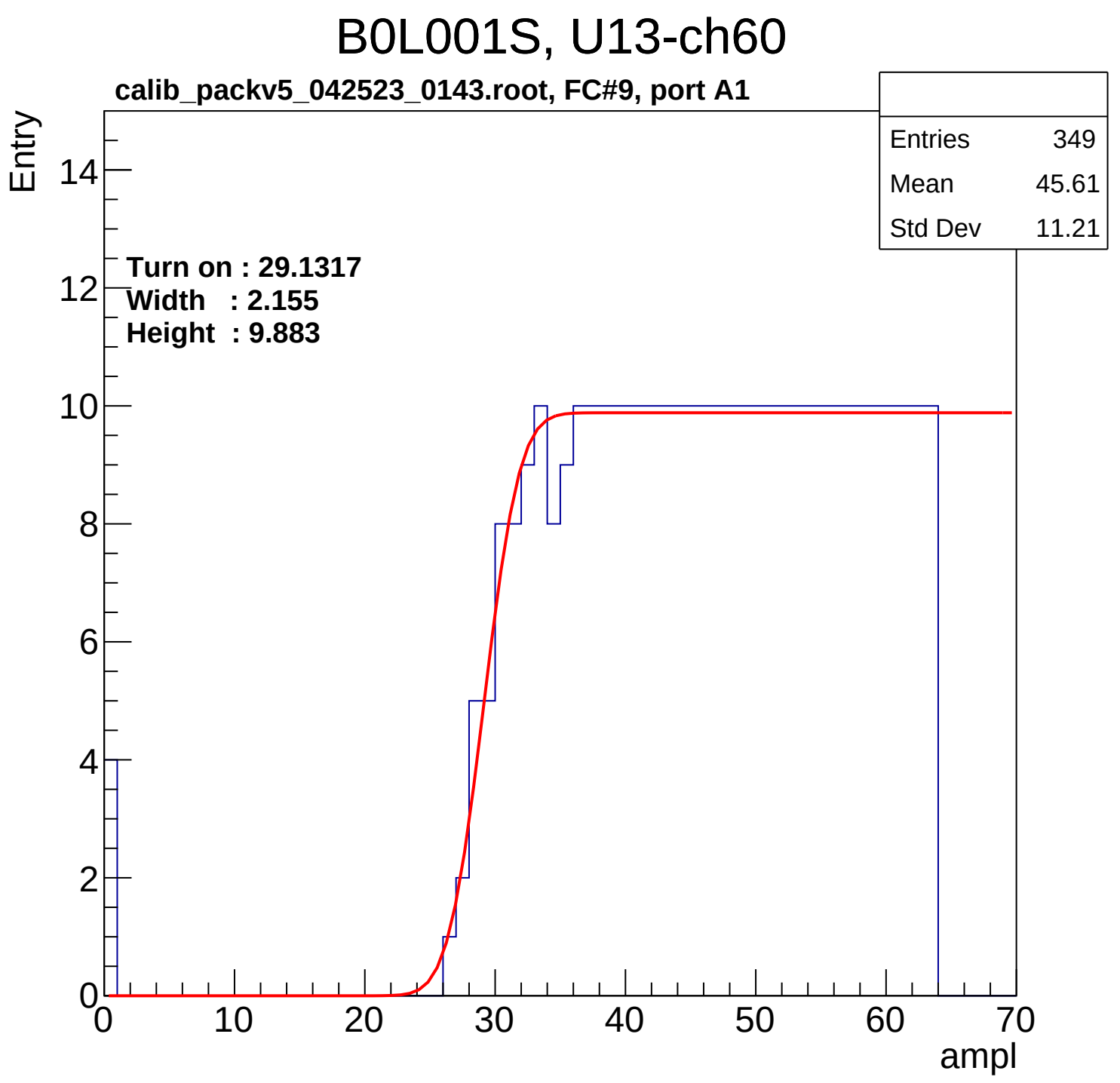
B0L001S, U13-ch60
calib_packv5_042523_0143.root, FC#9, port A1
Entries 349
Mean 45.61
Std Dev 11.21
Turn on : 29.1317
Width : 2.155
Height : 9.883
Entry
ampl
0
2
4
6
8
10
12
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0
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40
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60
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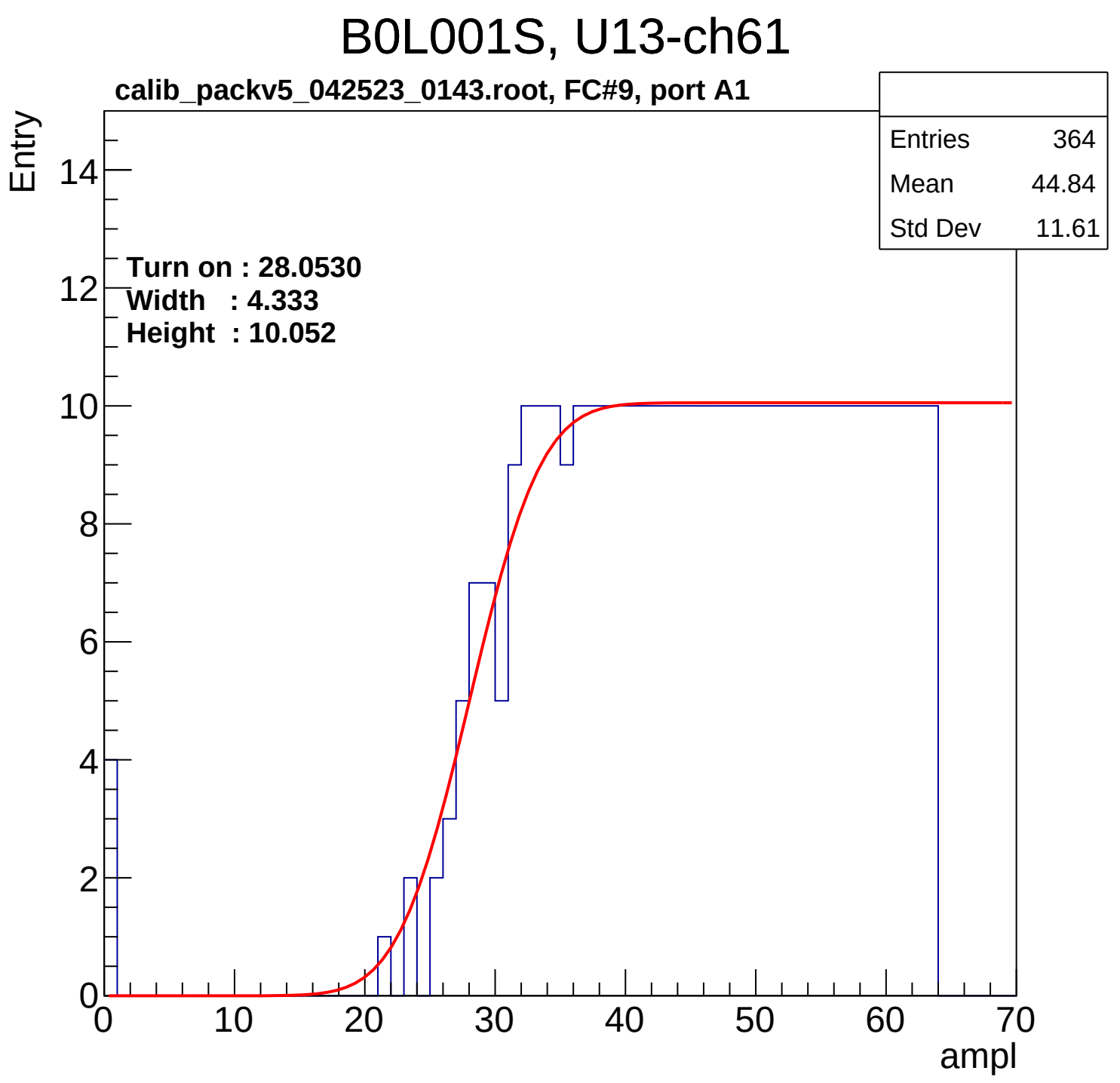
B0L001S, U13-ch61
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 44.84
Std Dev 11.61
Turn on : 28.0530
Width : 4.333
Height : 10.052
Entry
ampl
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2
4
6
8
10
12
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0
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60
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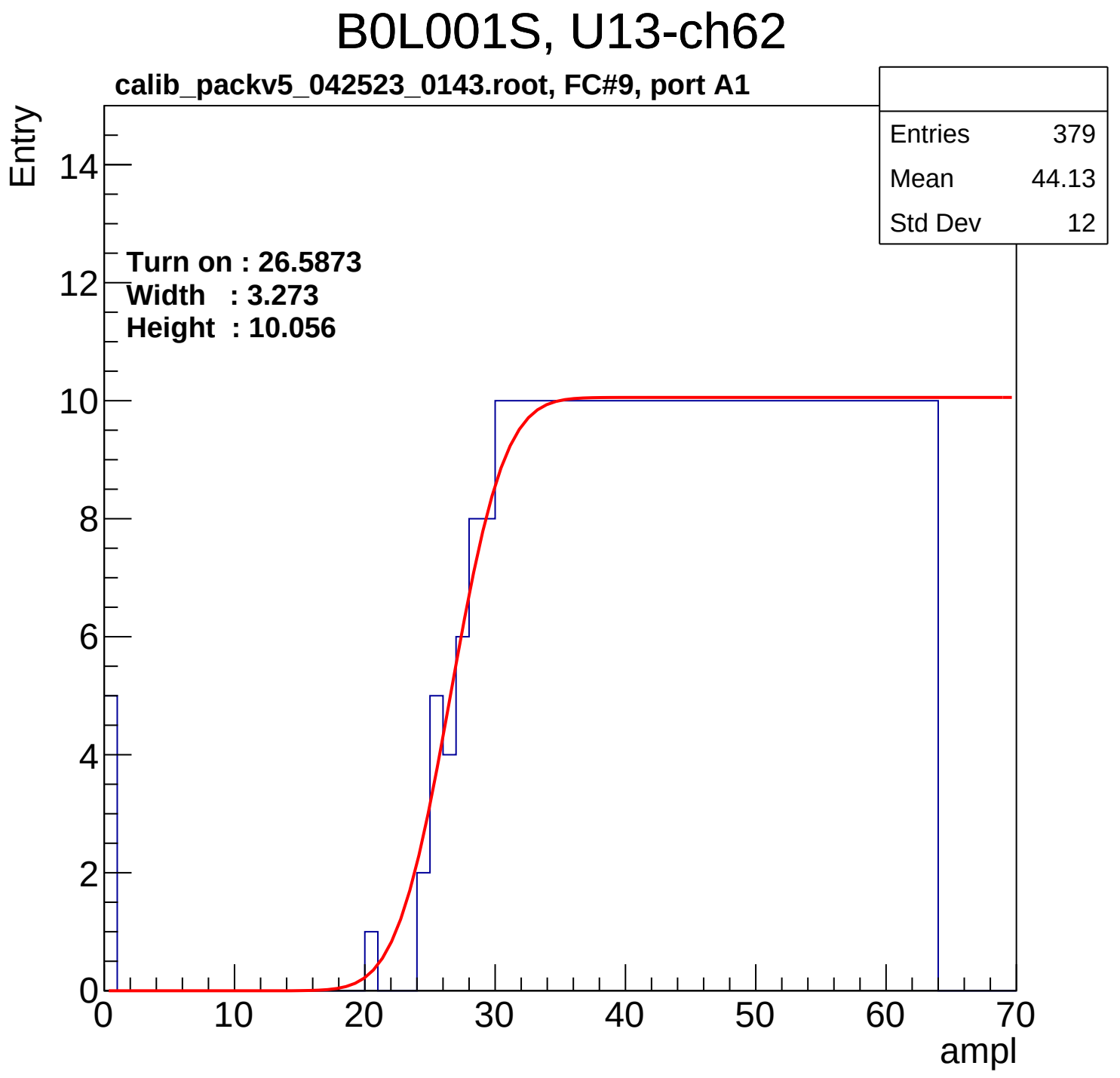
B0L001S, U13-ch62
calib_packv5_042523_0143.root, FC#9, port A1
Entries 379
Mean 44.13
Std Dev 12
Turn on : 26.5873
Width : 3.273
Height : 10.056
Entry
ampl
0
2
4
6
8
10
12
14
0
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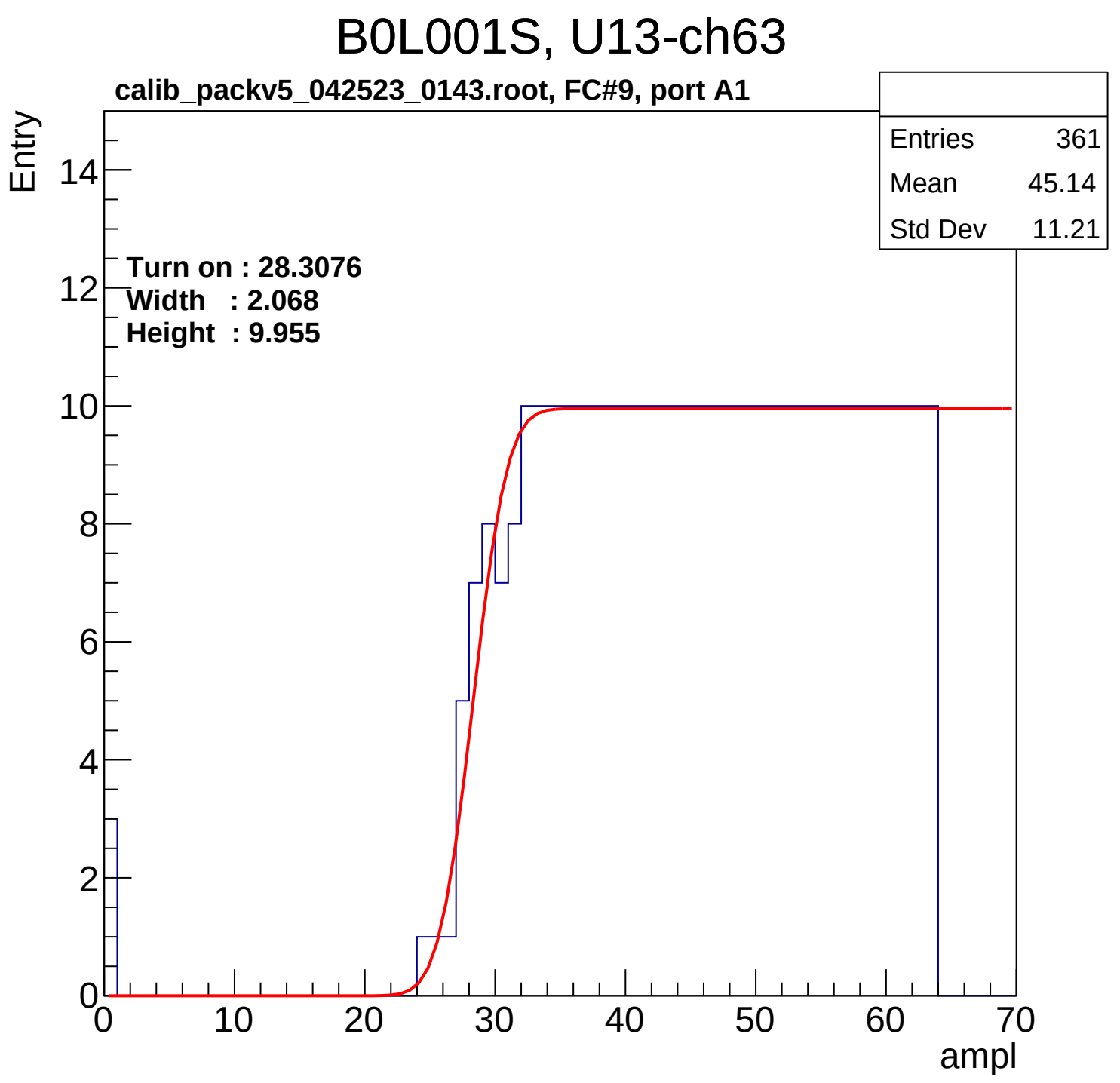
B0L001S, U13-ch63
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 45.14
Std Dev 11.21
Turn on : 28.3076
Width : 2.068
Height : 9.955
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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60
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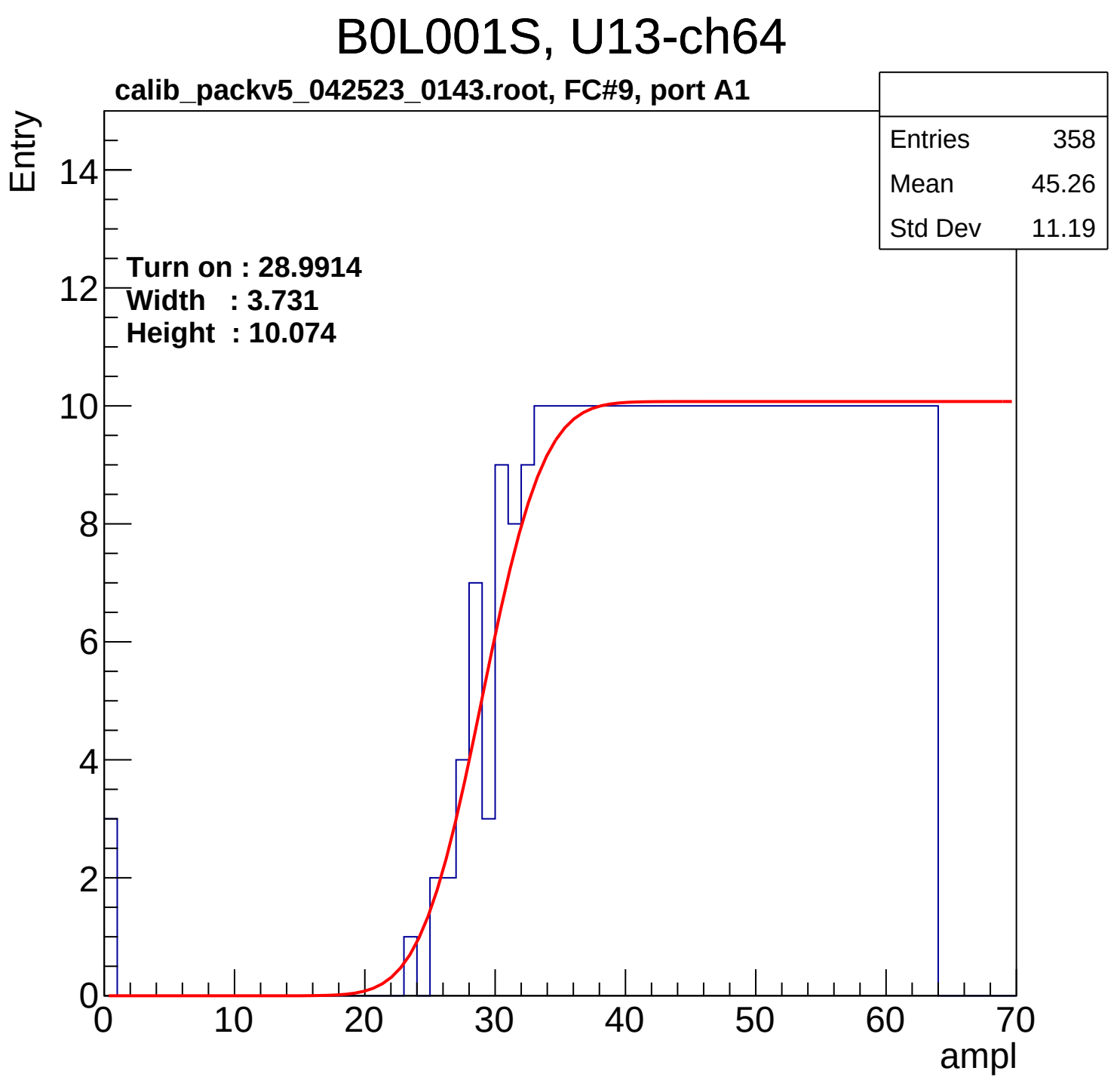
B0L001S, U13-ch64
calib_packv5_042523_0143.root, FC#9, port A1
Entries 358
Mean 45.26
Std Dev 11.19
Turn on : 28.9914
Width : 3.731
Height : 10.074
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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60
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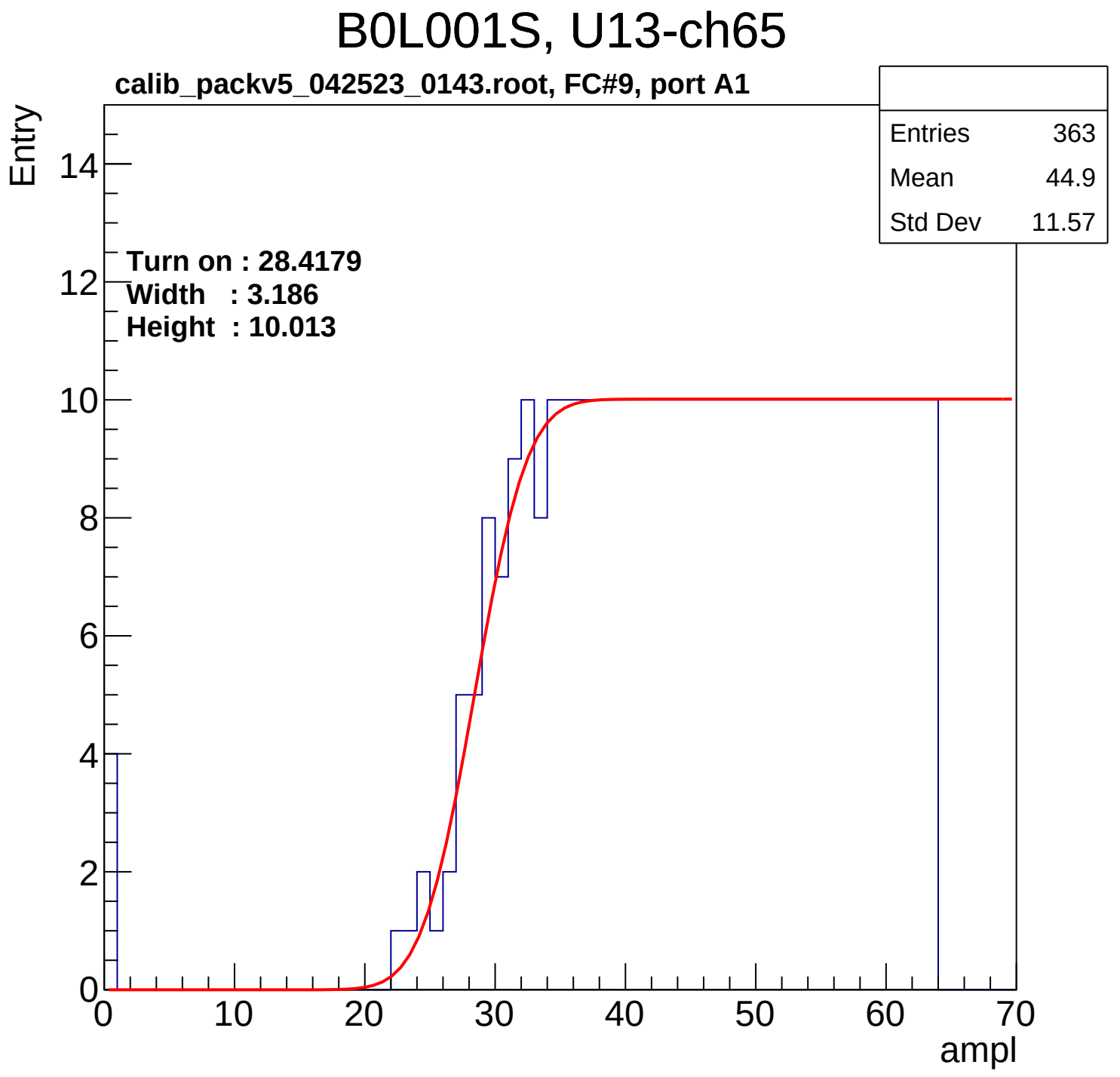
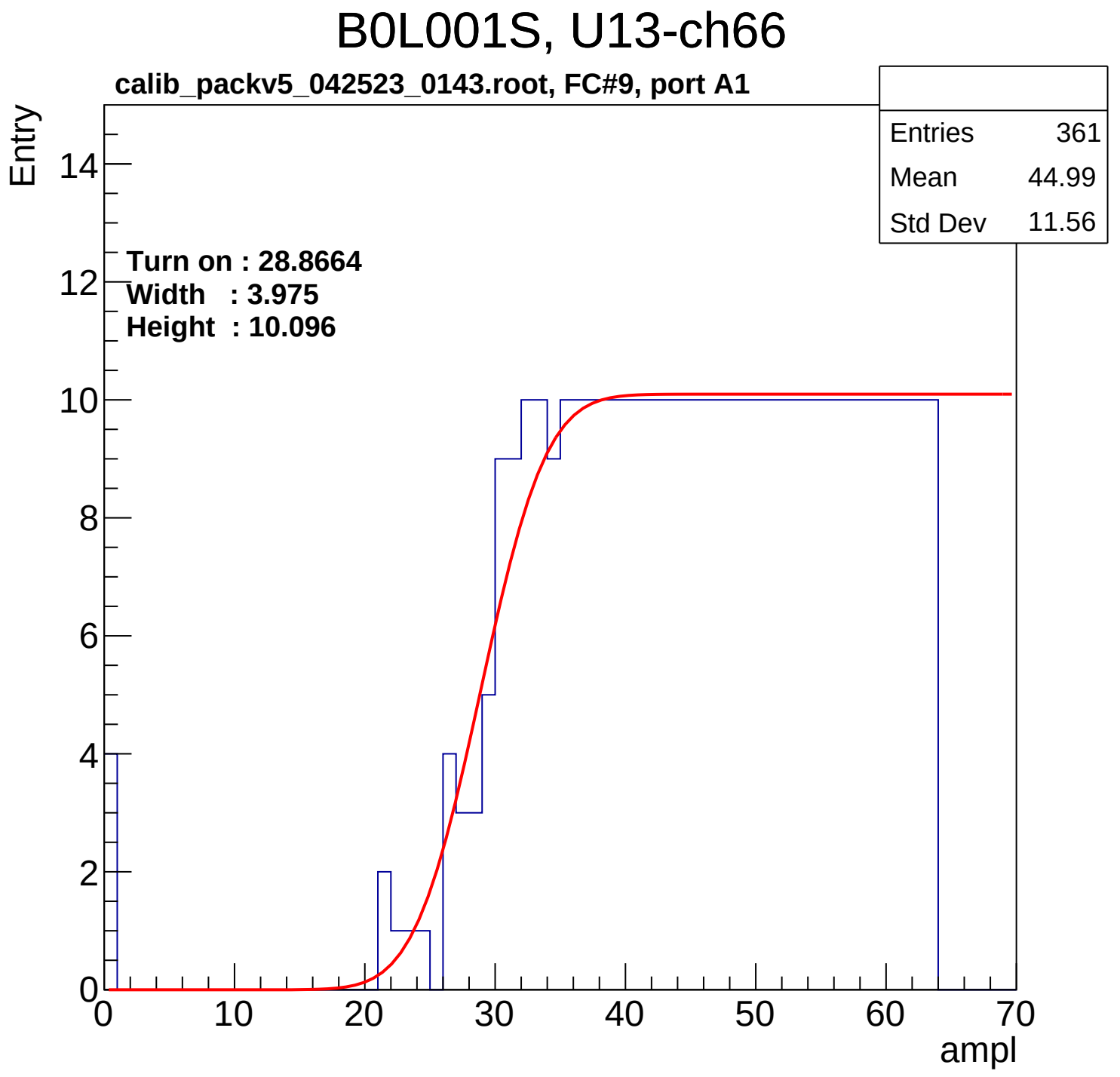

B0L001S, U13-ch65
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 44.9
Std Dev 11.57
Turn on : 28.4179
Width : 3.186
Height : 10.013
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U13-ch66
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 44.99
Std Dev 11.56
Turn on : 28.8664
Width : 3.975
Height : 10.096
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
50
60
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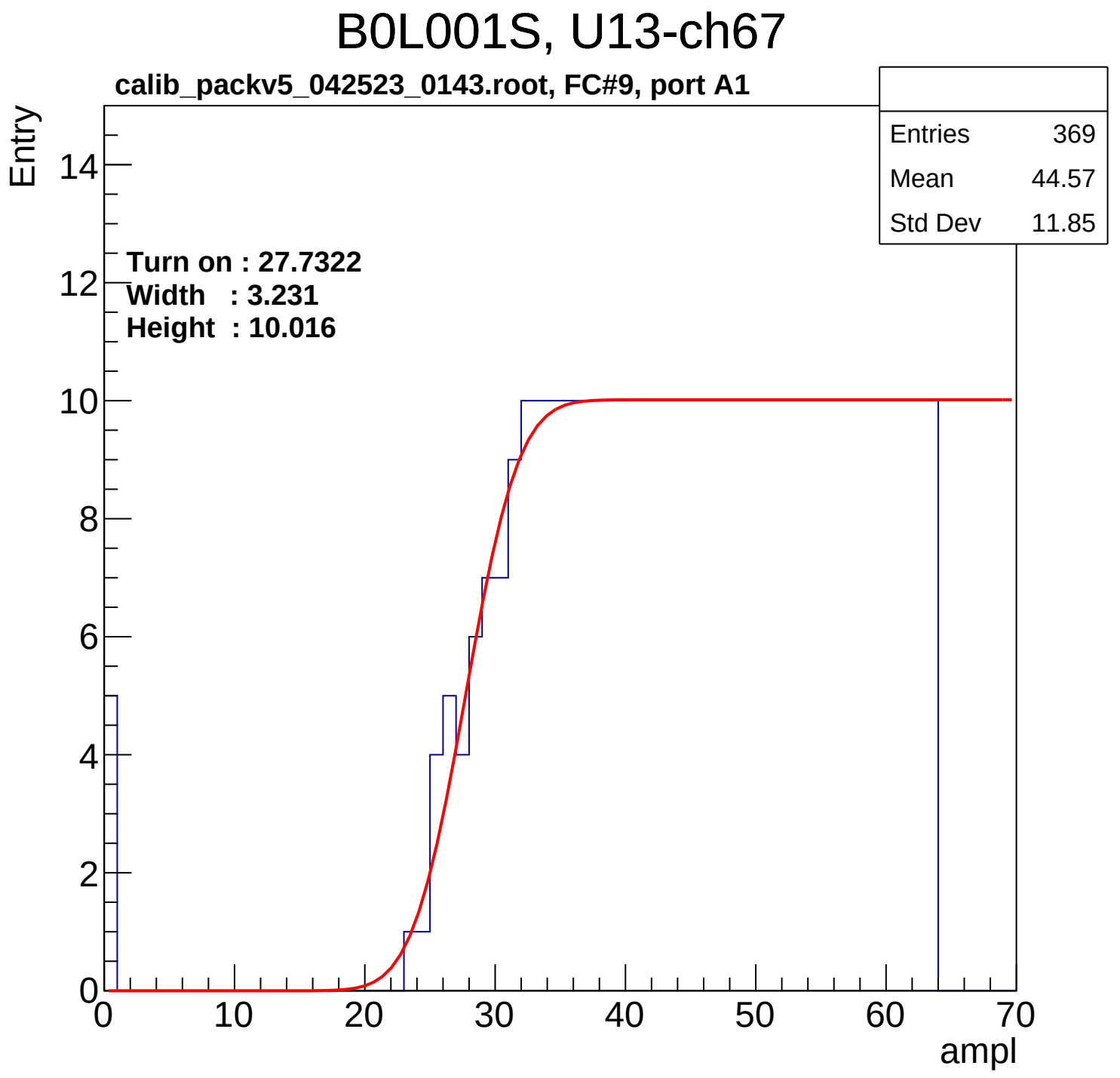
B0L001S, U13-ch67
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.57
Std Dev 11.85
Turn on : 27.7322
Width : 3.231
Height : 10.016
Entry
ampl
0
2
4
6
8
10
12
14
0
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40
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60
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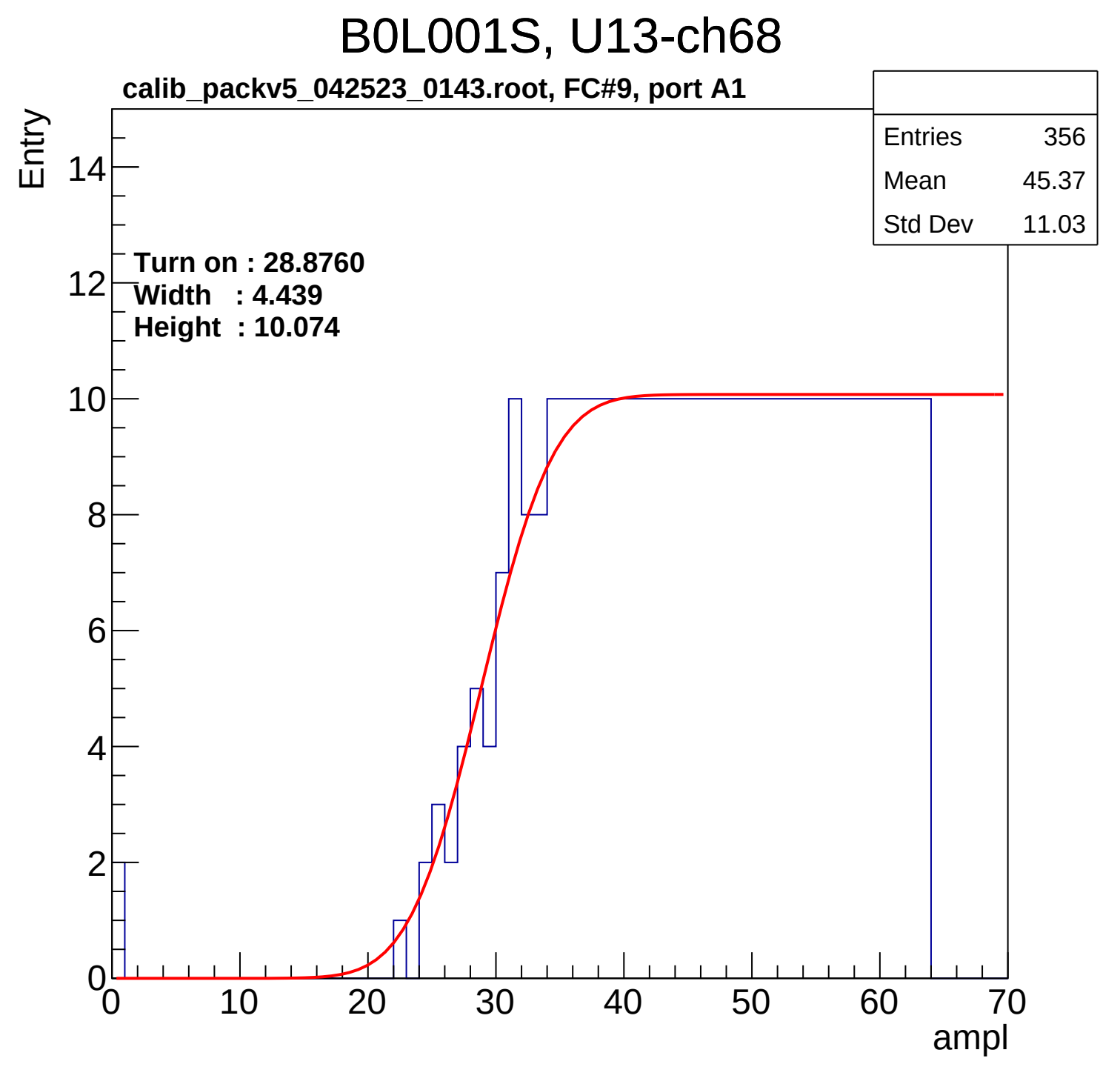
B0L001S, U13-ch68
calib_packv5_042523_0143.root, FC#9, port A1
Entries 356
Mean 45.37
Std Dev 11.03
Turn on : 28.8760
Width : 4.439
Height : 10.074
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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40
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60
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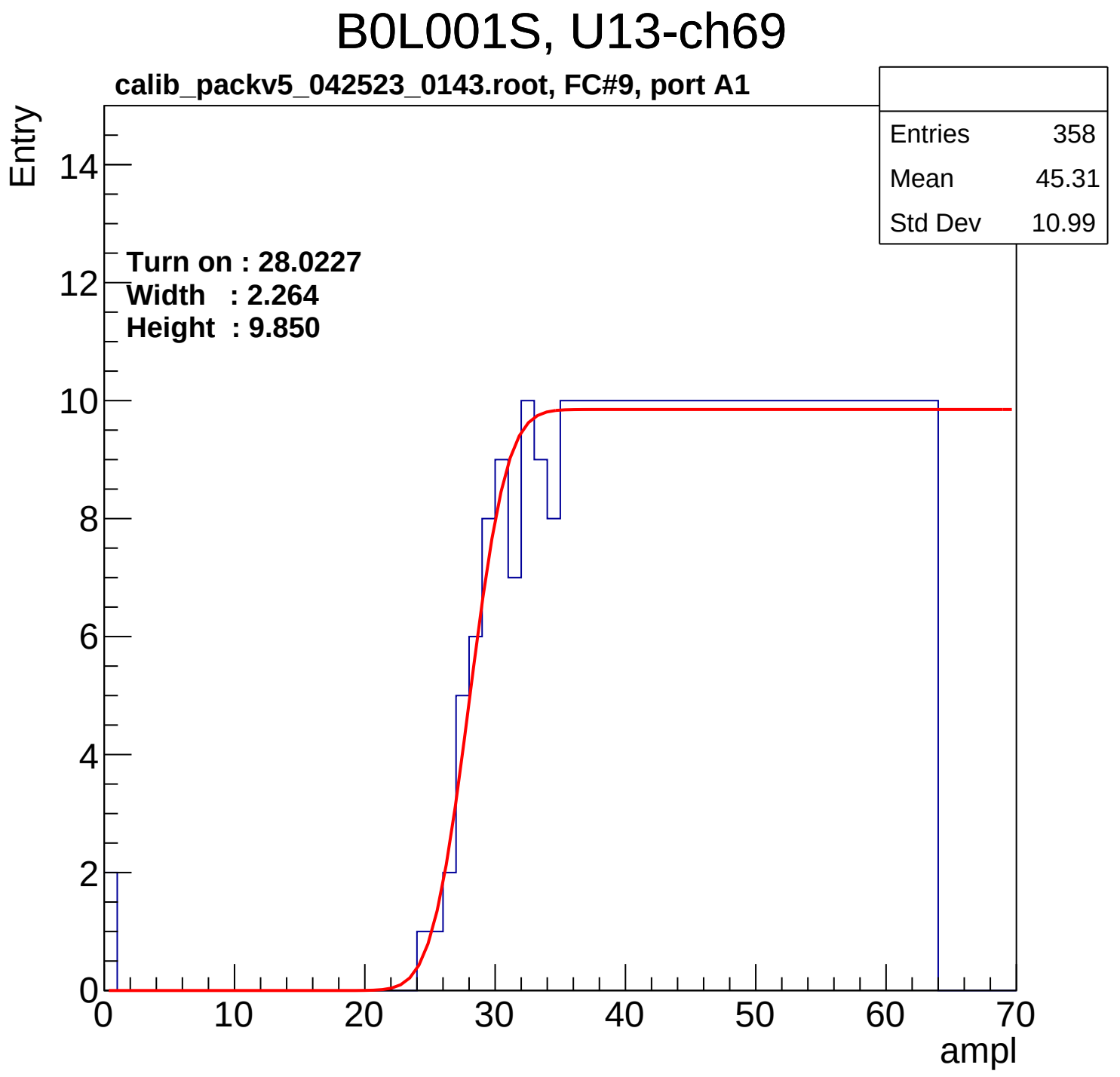
B0L001S, U13-ch69
calib_packv5_042523_0143.root, FC#9, port A1
Entries 358
Mean 45.31
Std Dev 10.99
Turn on : 28.0227
Width : 2.264
Height : 9.850
Entry
ampl
0
2
4
6
8
10
12
14
0
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60
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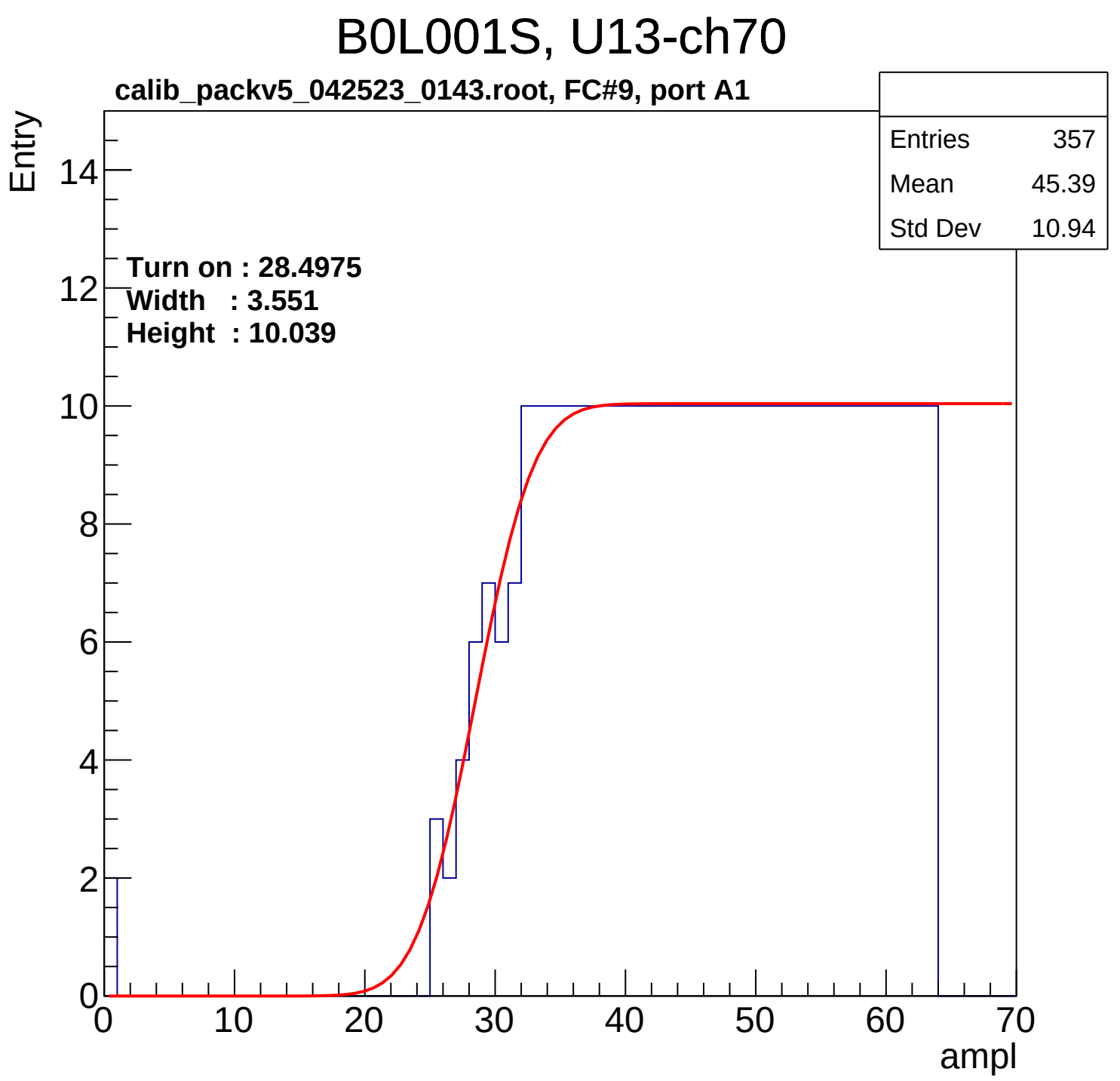
B0L001S, U13-ch70
calib_packv5_042523_0143.root, FC#9, port A1
Entries 357
Mean 45.39
Std Dev 10.94
Turn on : 28.4975
Width : 3.551
Height : 10.039
Entry
ampl
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2
4
6
8
10
12
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0
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60
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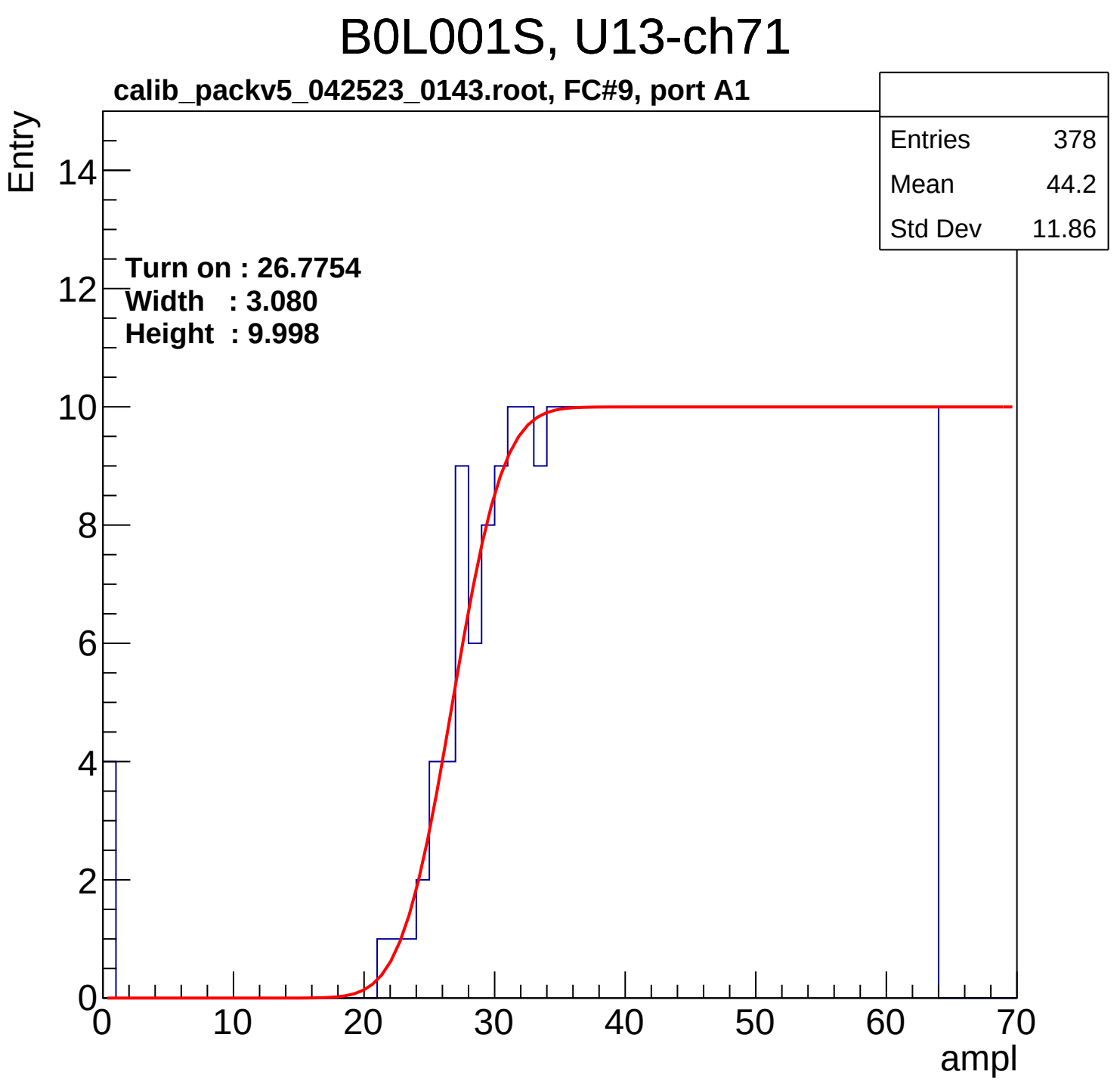
B0L001S, U13-ch71
calib_packv5_042523_0143.root, FC#9, port A1
Entries 378
Mean 44.2
Std Dev 11.86
Turn on : 26.7754
Width : 3.080
Height : 9.998
Entry
ampl
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2
4
6
8
10
12
14
0
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20
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60
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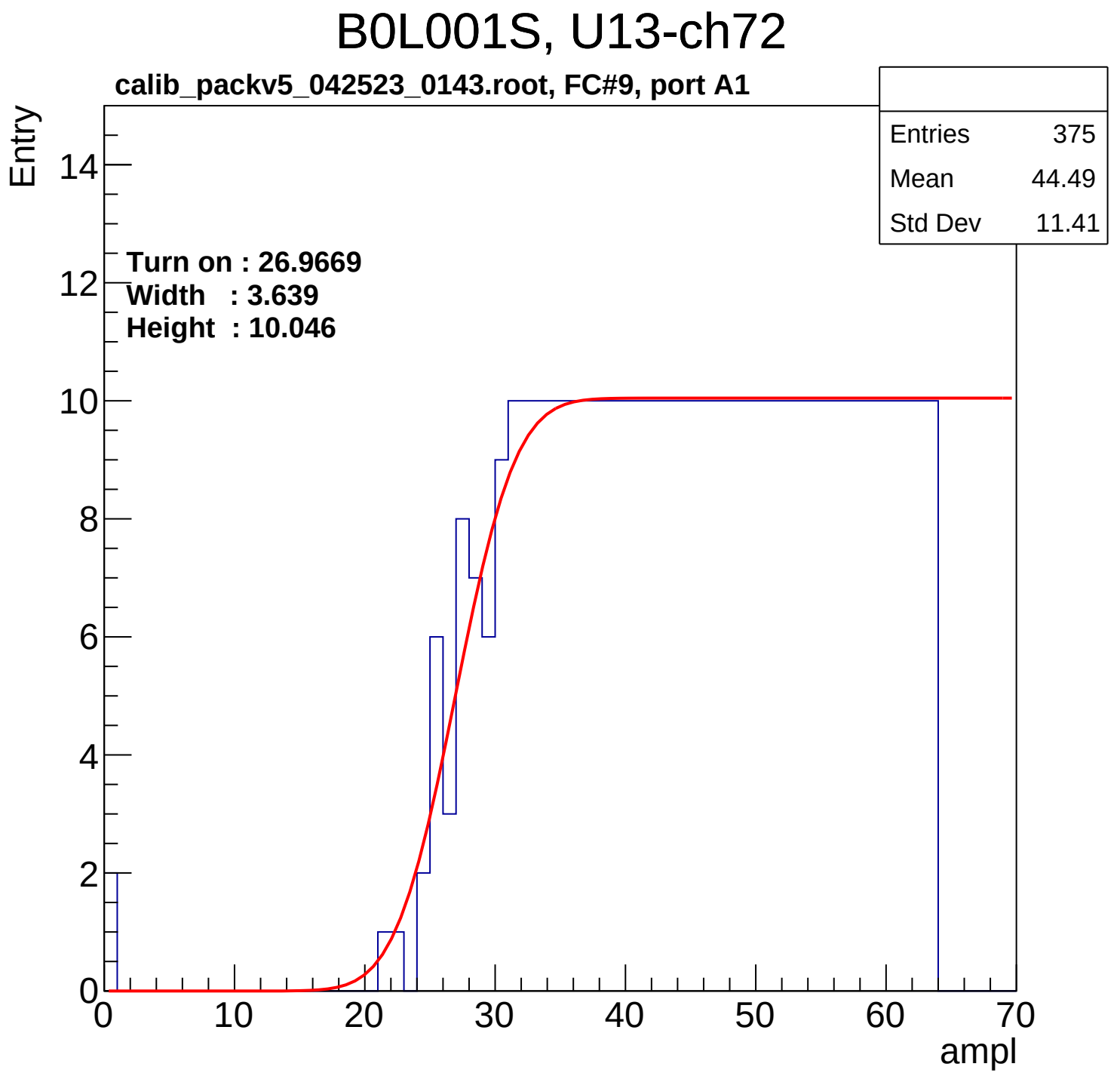
B0L001S, U13-ch72
calib_packv5_042523_0143.root, FC#9, port A1
Entries 375
Mean 44.49
Std Dev 11.41
Turn on : 26.9669
Width : 3.639
Height : 10.046
Entry
ampl
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6
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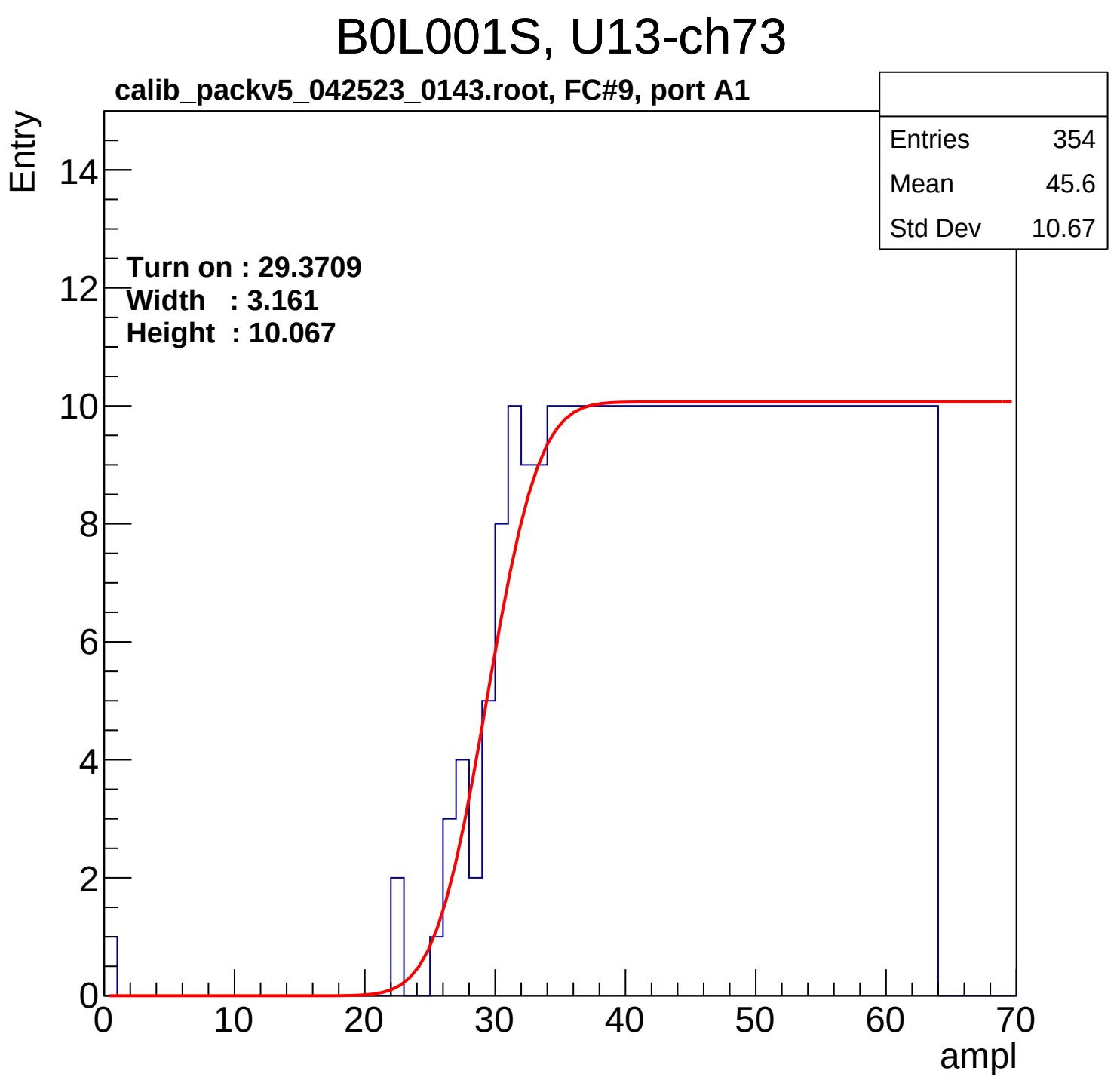
B0L001S, U13-ch73
calib_packv5_042523_0143.root, FC#9, port A1
Entries 354
Mean 45.6
Std Dev 10.67
Turn on : 29.3709
Width : 3.161
Height : 10.067
Entry
ampl
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4
6
8
10
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0
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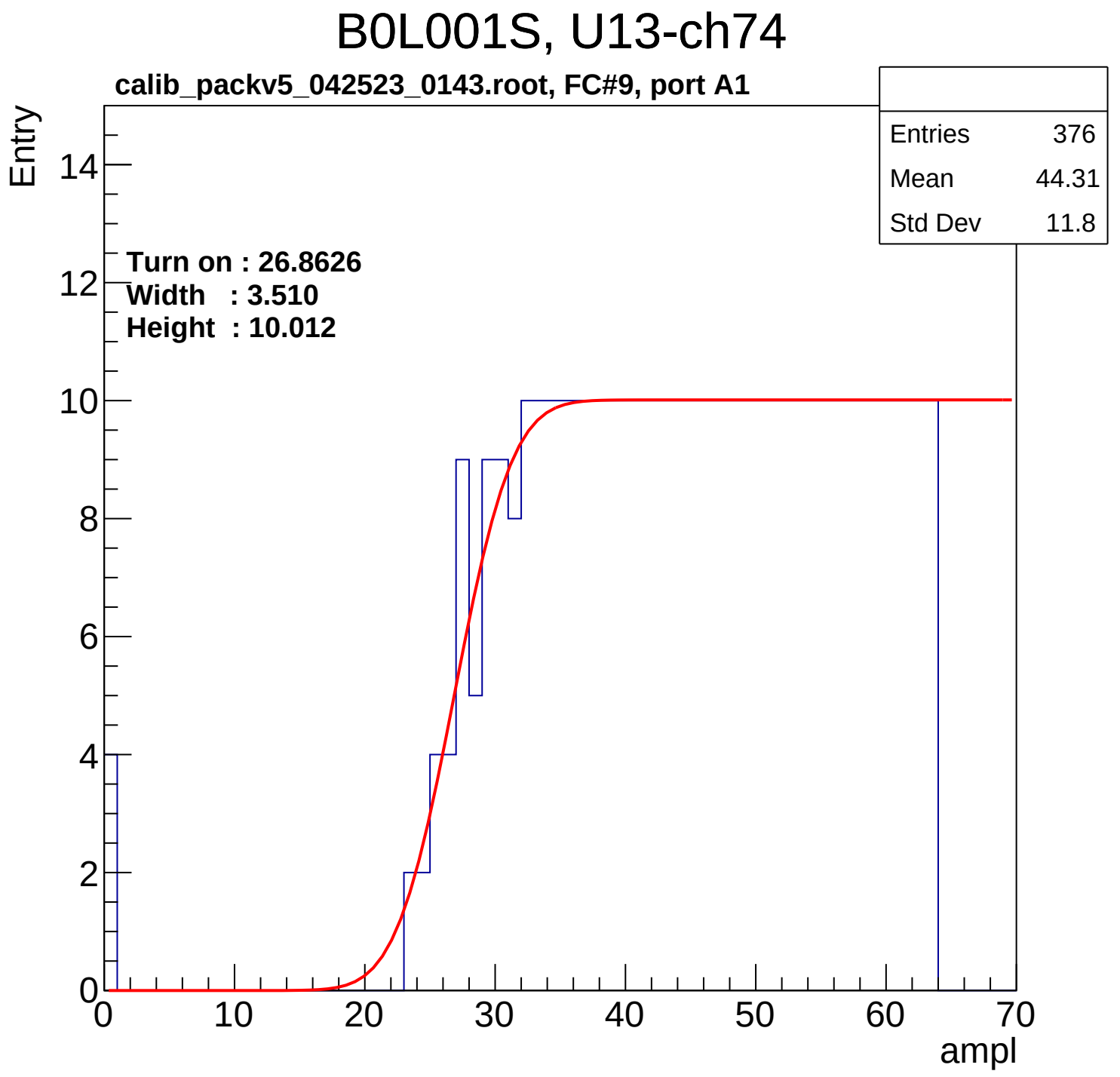
B0L001S, U13-ch74
calib_packv5_042523_0143.root, FC#9, port A1
Entries 376
Mean 44.31
Std Dev 11.8
Turn on : 26.8626
Width : 3.510
Height : 10.012
Entry
ampl
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8
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0
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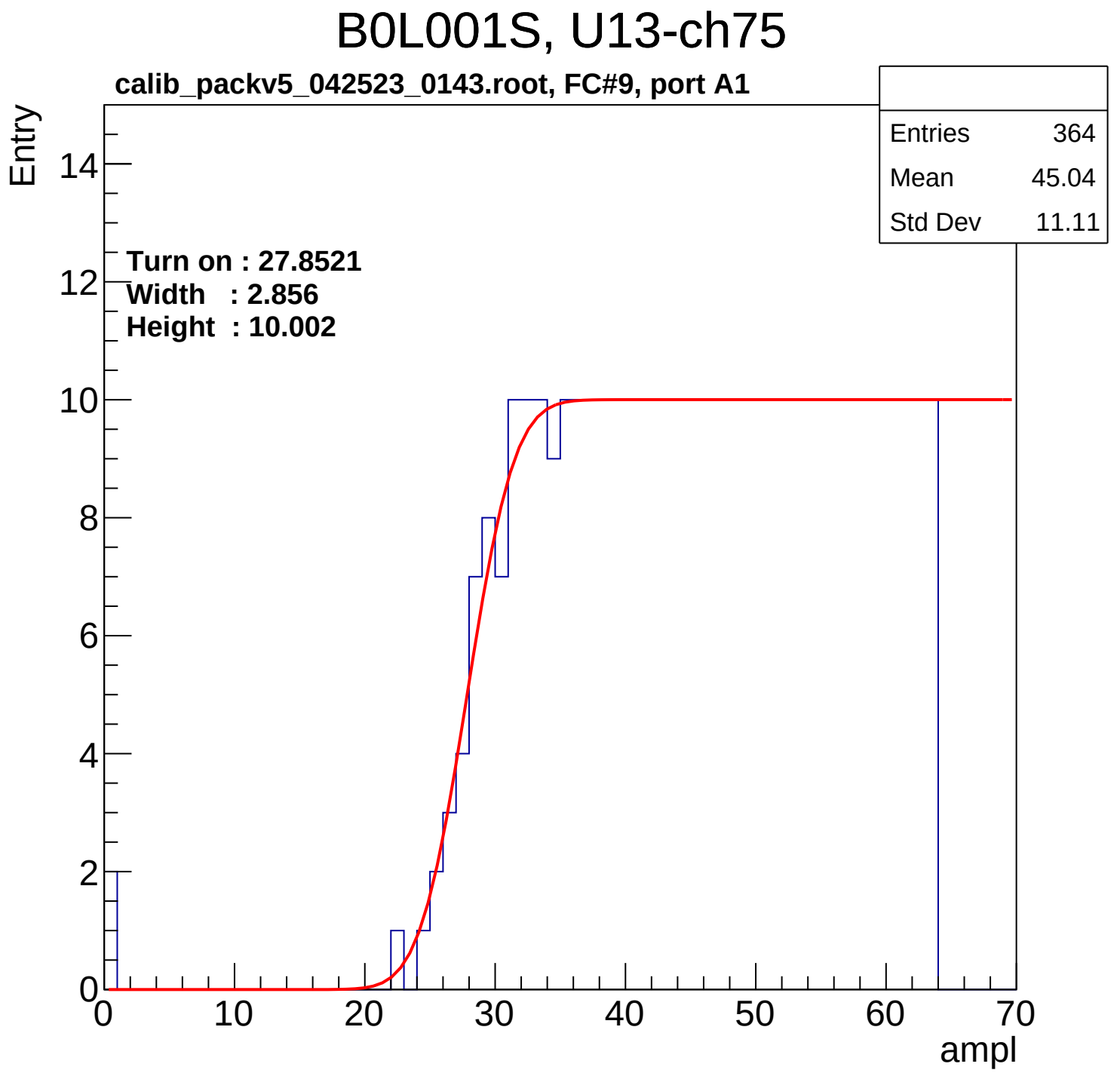
B0L001S, U13-ch75
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 45.04
Std Dev 11.11
Turn on : 27.8521
Width : 2.856
Height : 10.002
Entry
ampl
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2
4
6
8
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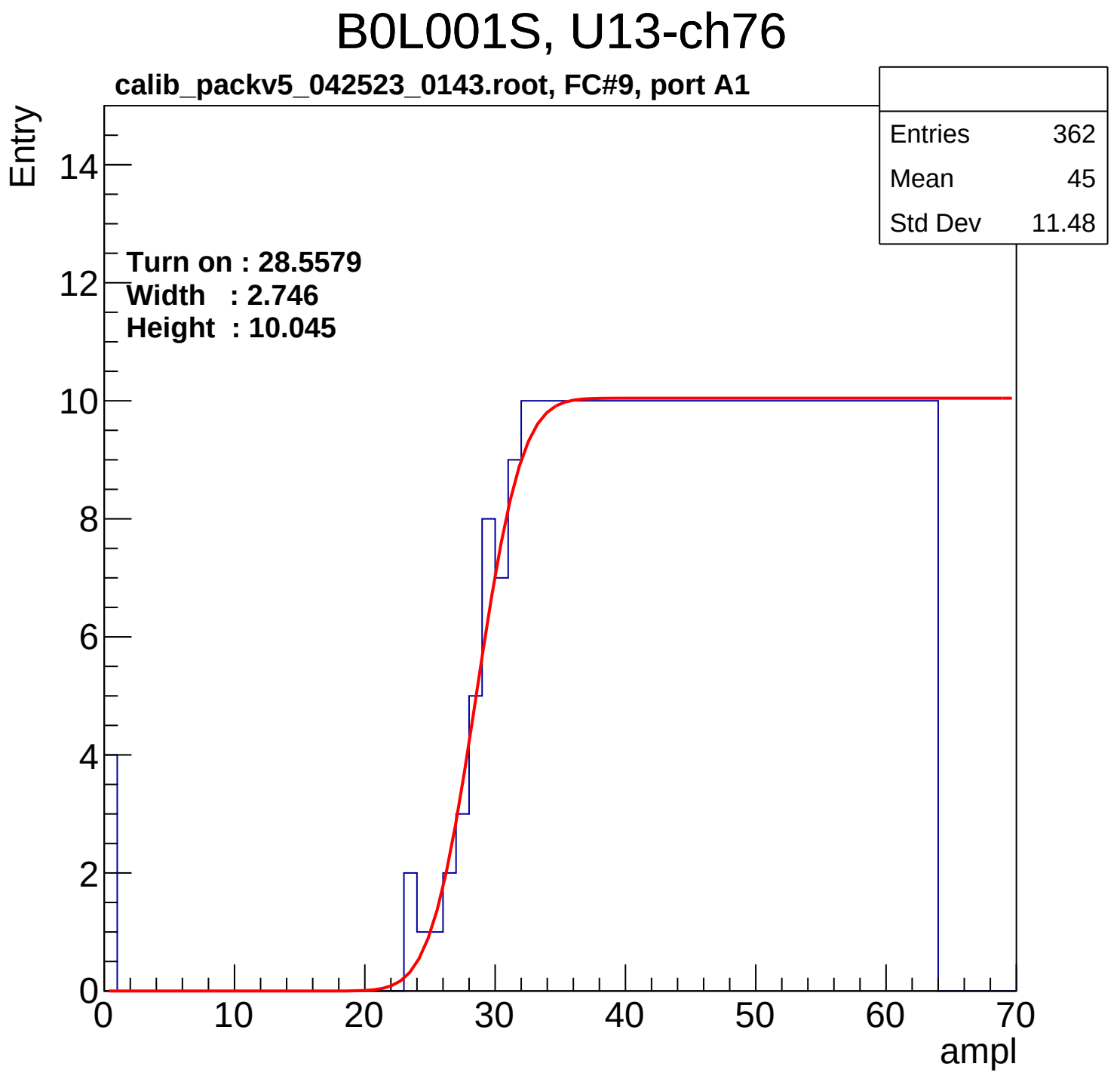
B0L001S, U13-ch76
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 45
Std Dev 11.48
Turn on : 28.5579
Width : 2.746
Height : 10.045
Entry
ampl
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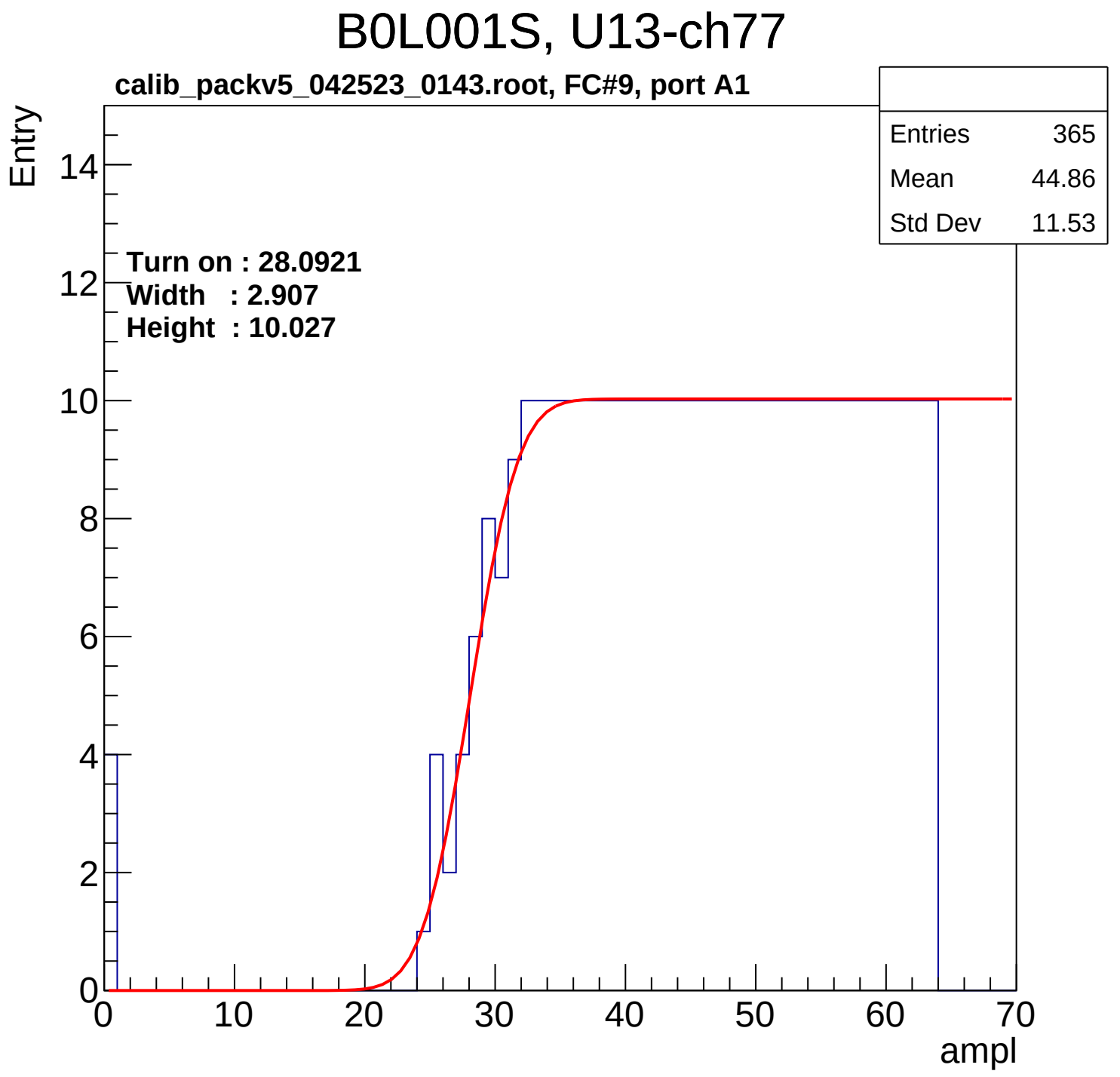
B0L001S, U13-ch77
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 44.86
Std Dev 11.53
Turn on : 28.0921
Width : 2.907
Height : 10.027
Entry
ampl
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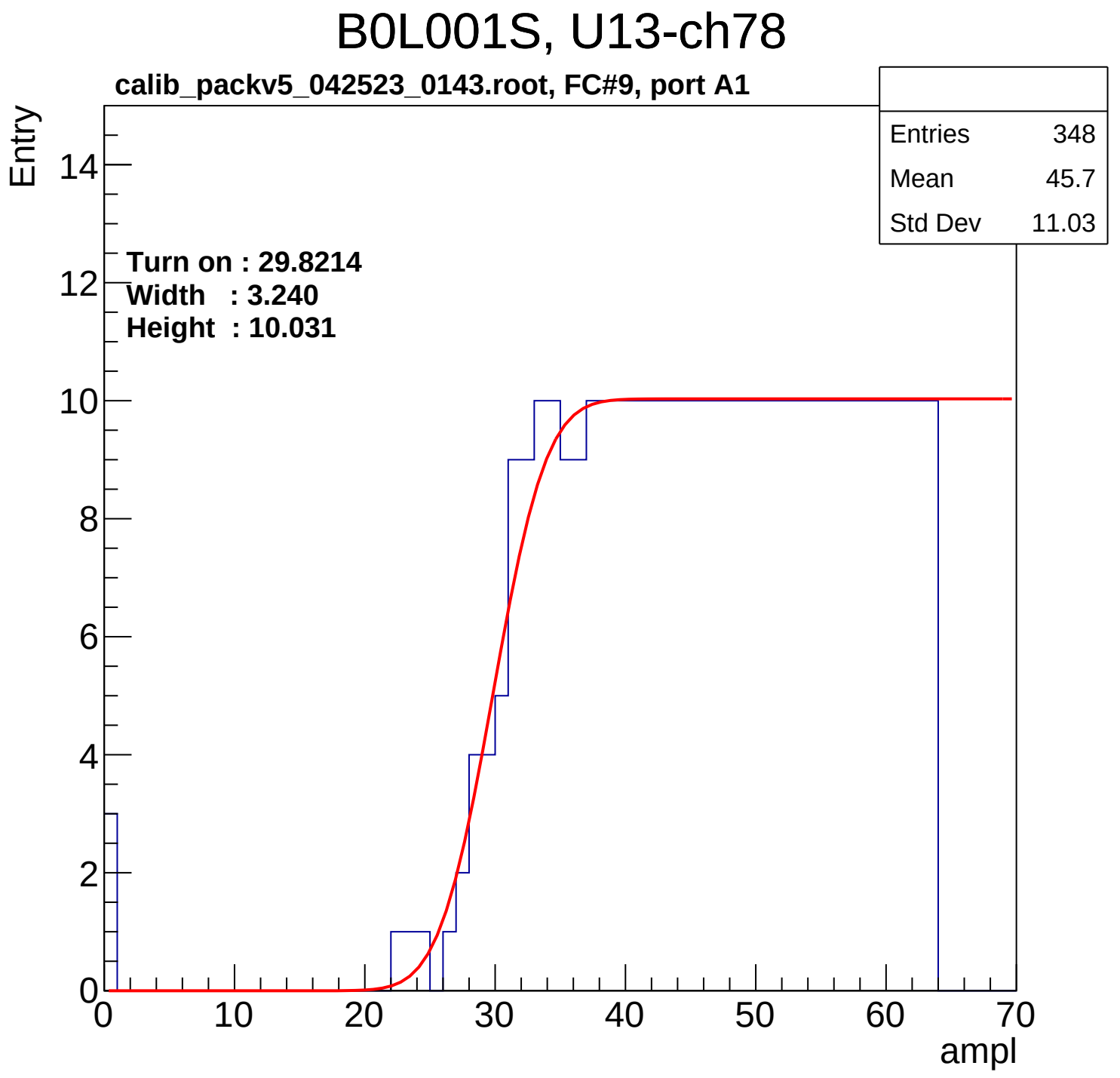
B0L001S, U13-ch78
calib_packv5_042523_0143.root, FC#9, port A1
Entries 348
Mean 45.7
Std Dev 11.03
Turn on : 29.8214
Width : 3.240
Height : 10.031
Entry
ampl
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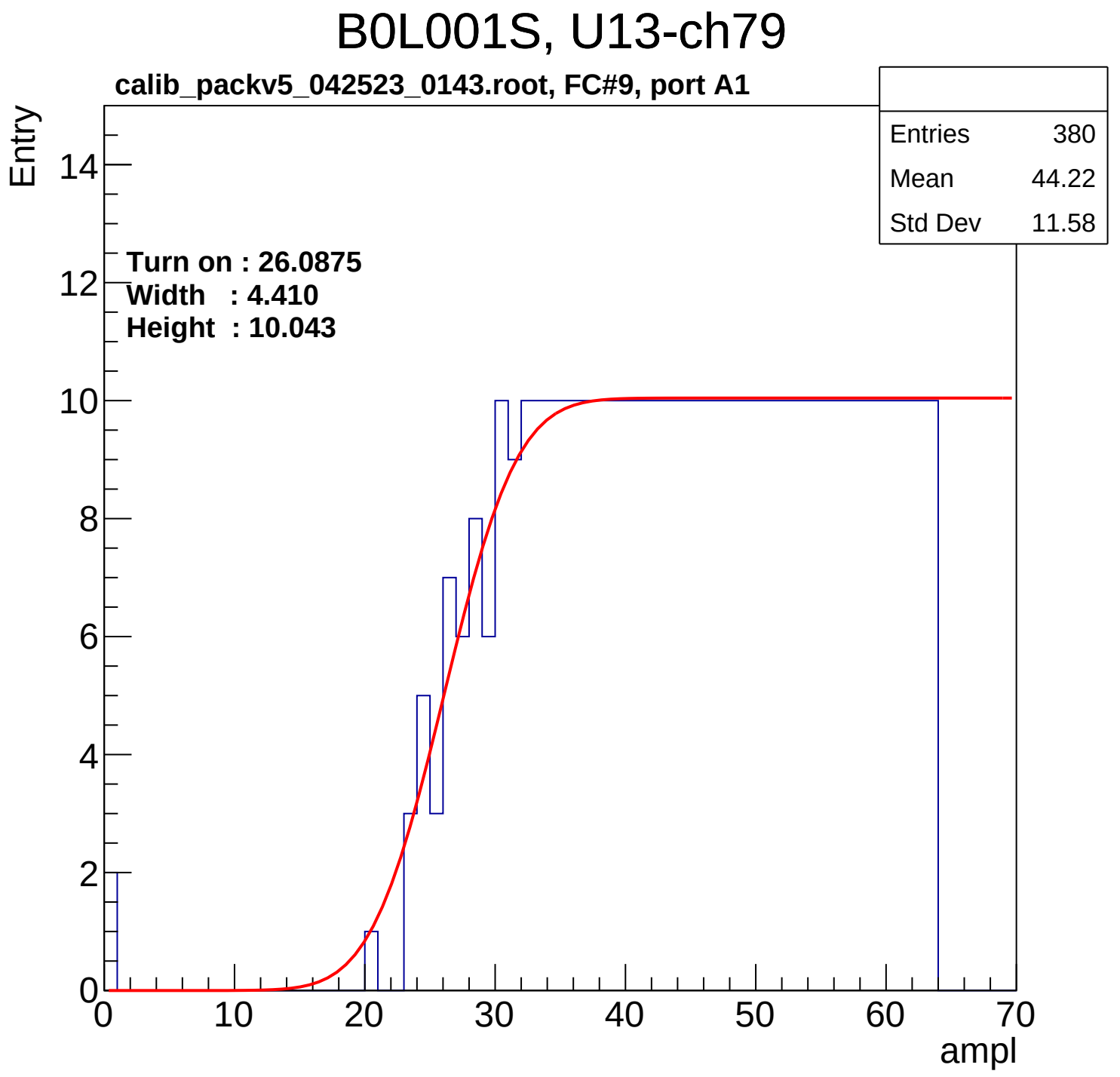
B0L001S, U13-ch79
calib_packv5_042523_0143.root, FC#9, port A1
Entries 380
Mean 44.22
Std Dev 11.58
Turn on : 26.0875
Width : 4.410
Height : 10.043
Entry
ampl
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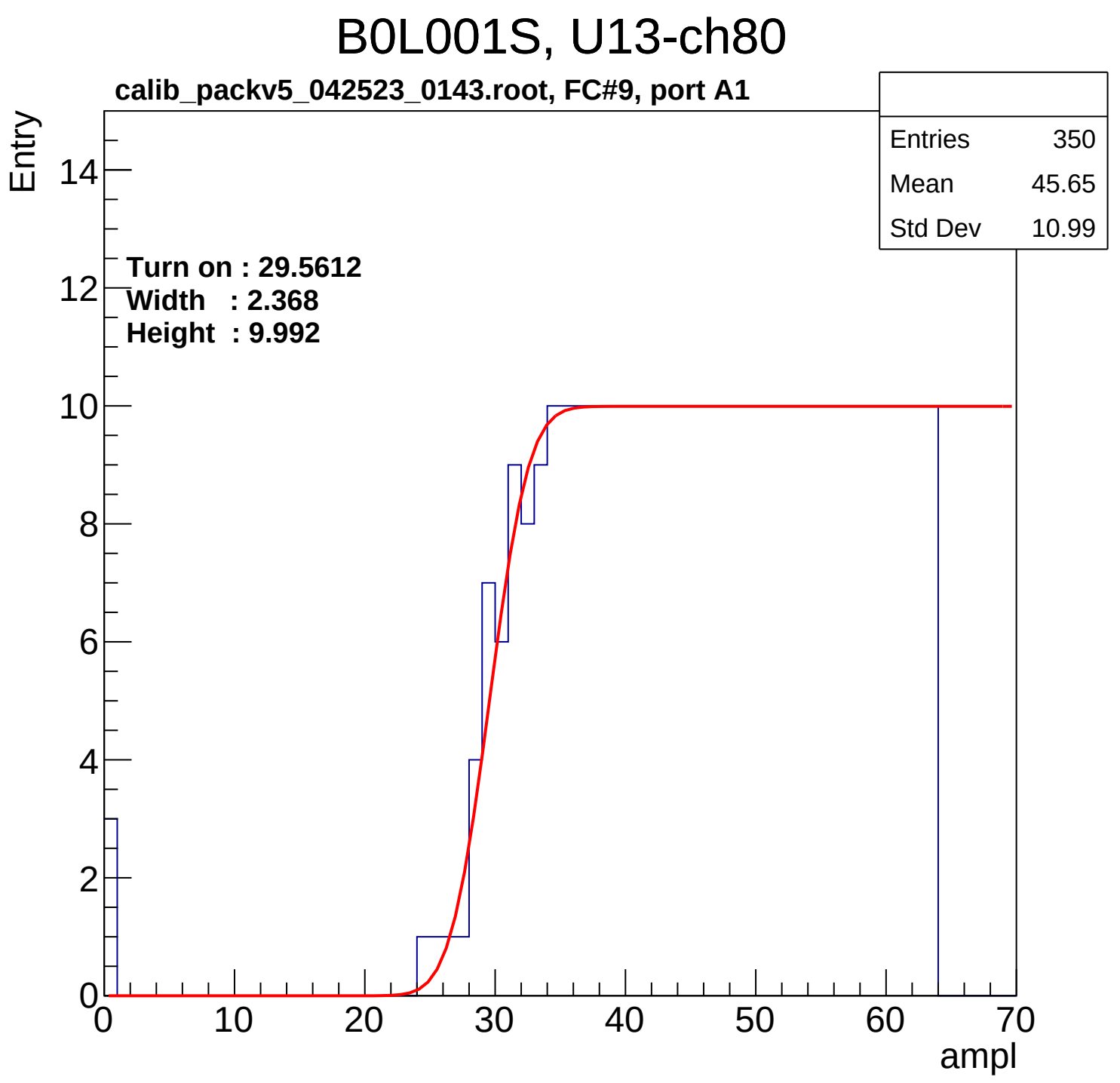
B0L001S, U13-ch80
calib_packv5_042523_0143.root, FC#9, port A1
Entries 350
Mean 45.65
Std Dev 10.99
Turn on : 29.5612
Width : 2.368
Height : 9.992
Entry
ampl
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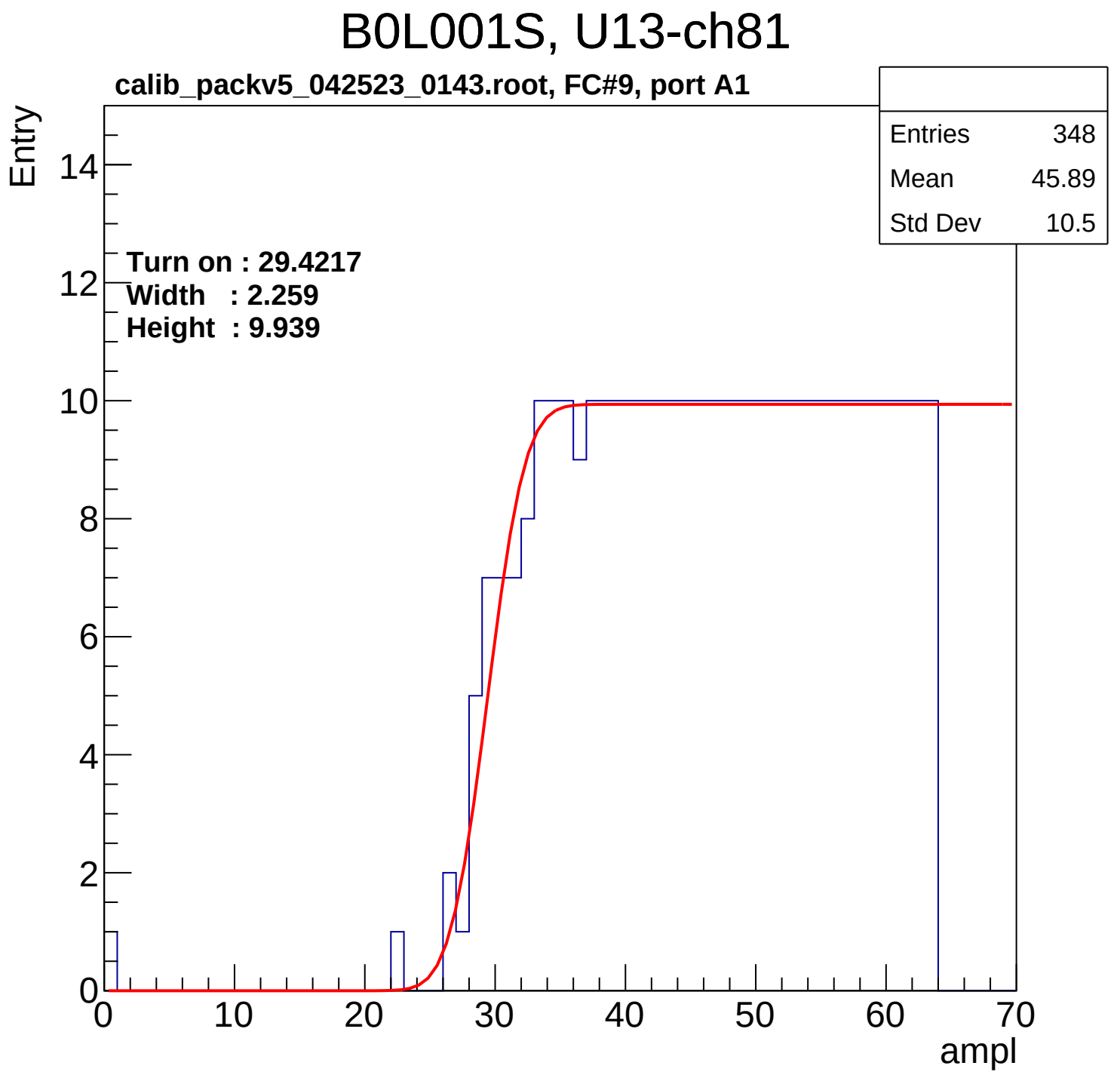
B0L001S, U13-ch81
calib_packv5_042523_0143.root, FC#9, port A1
Entries 348
Mean 45.89
Std Dev 10.5
Turn on : 29.4217
Width : 2.259
Height : 9.939
Entry
ampl
0
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4
6
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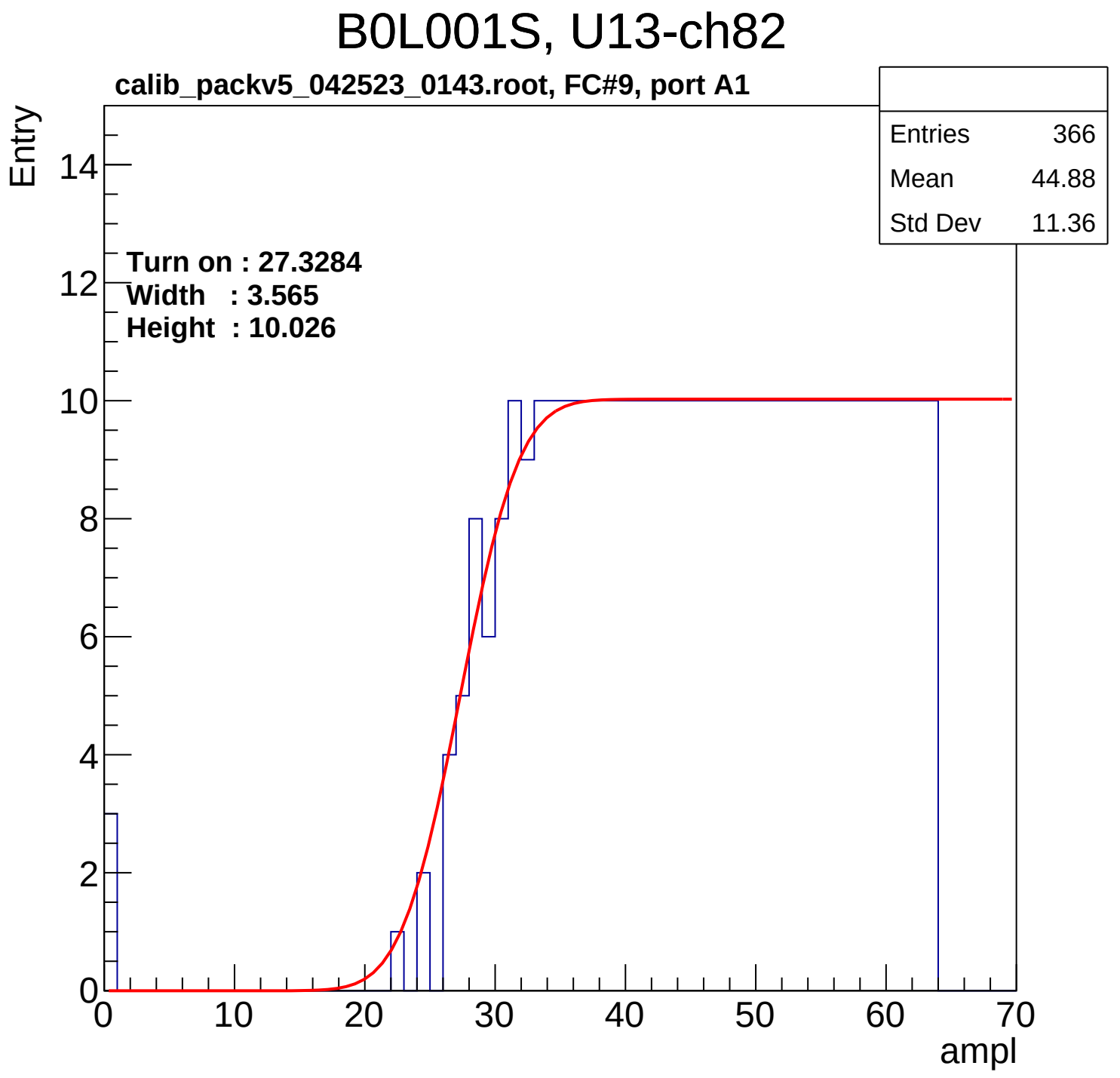
B0L001S, U13-ch82
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.88
Std Dev 11.36
Turn on : 27.3284
Width : 3.565
Height : 10.026
Entry
ampl
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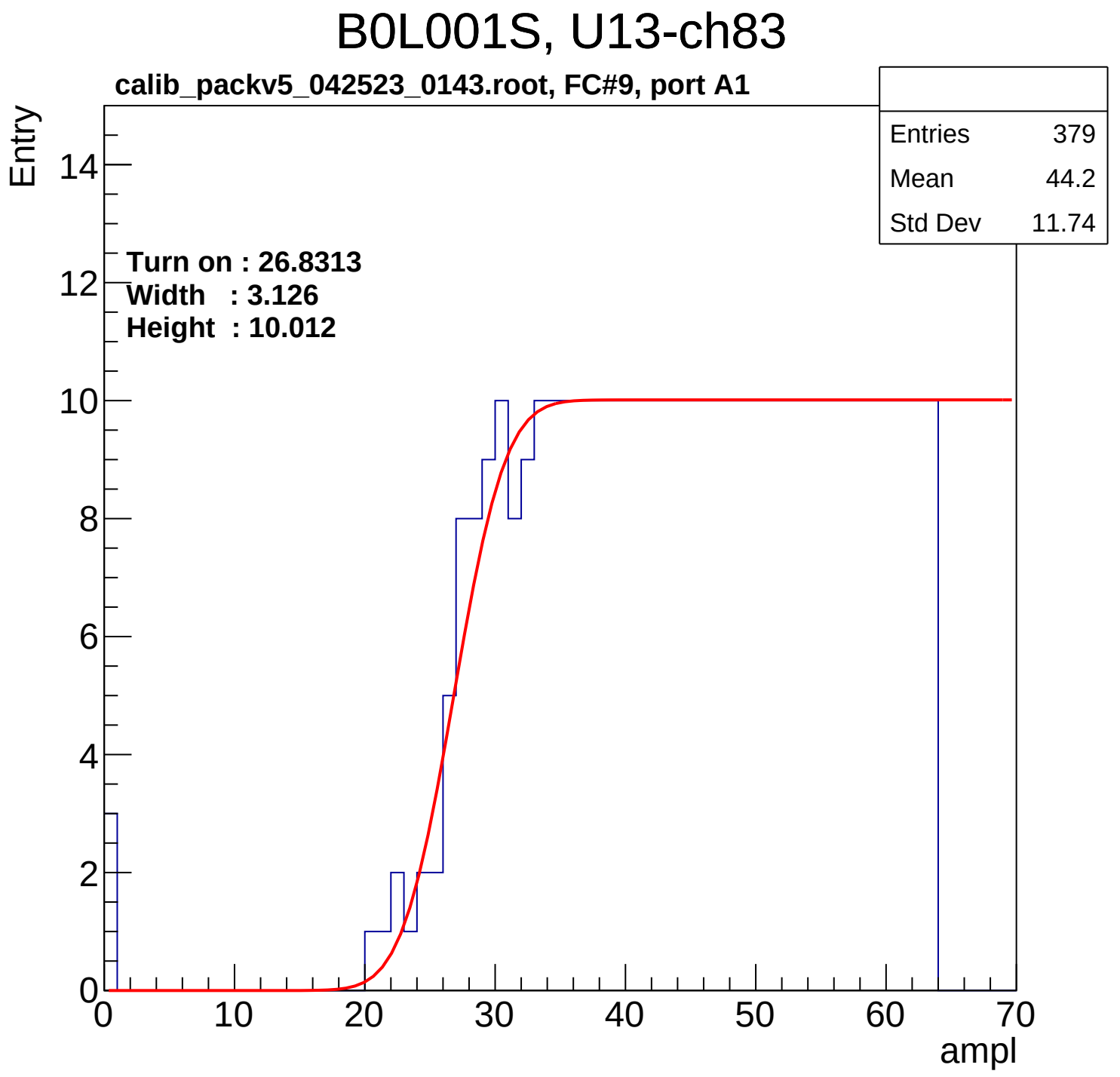
B0L001S, U13-ch83
calib_packv5_042523_0143.root, FC#9, port A1
Entries 379
Mean 44.2
Std Dev 11.74
Turn on : 26.8313
Width : 3.126
Height : 10.012
Entry
ampl
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2
4
6
8
10
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0
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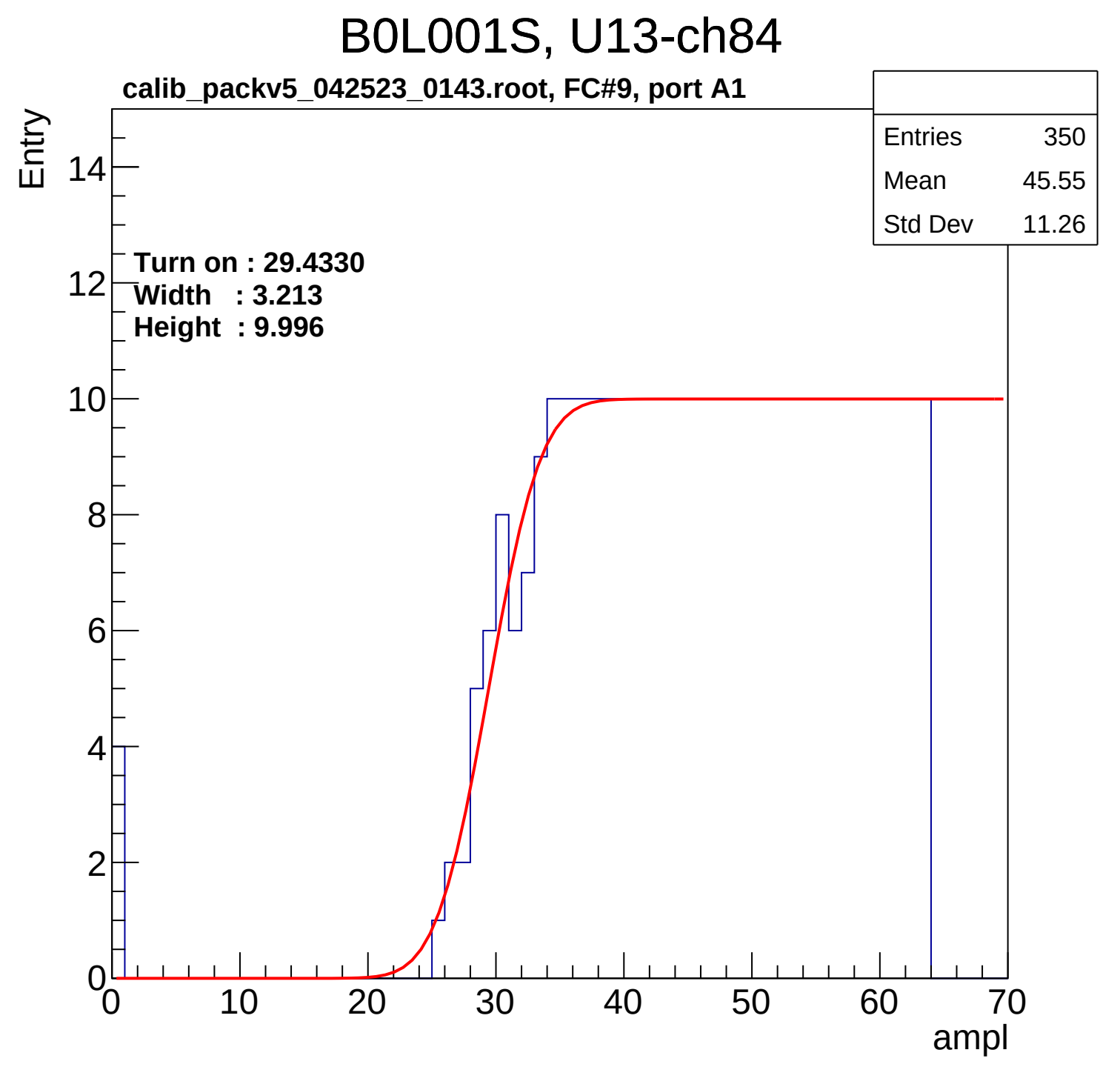
B0L001S, U13-ch84
calib_packv5_042523_0143.root, FC#9, port A1
Entries 350
Mean 45.55
Std Dev 11.26
Turn on : 29.4330
Width : 3.213
Height : 9.996
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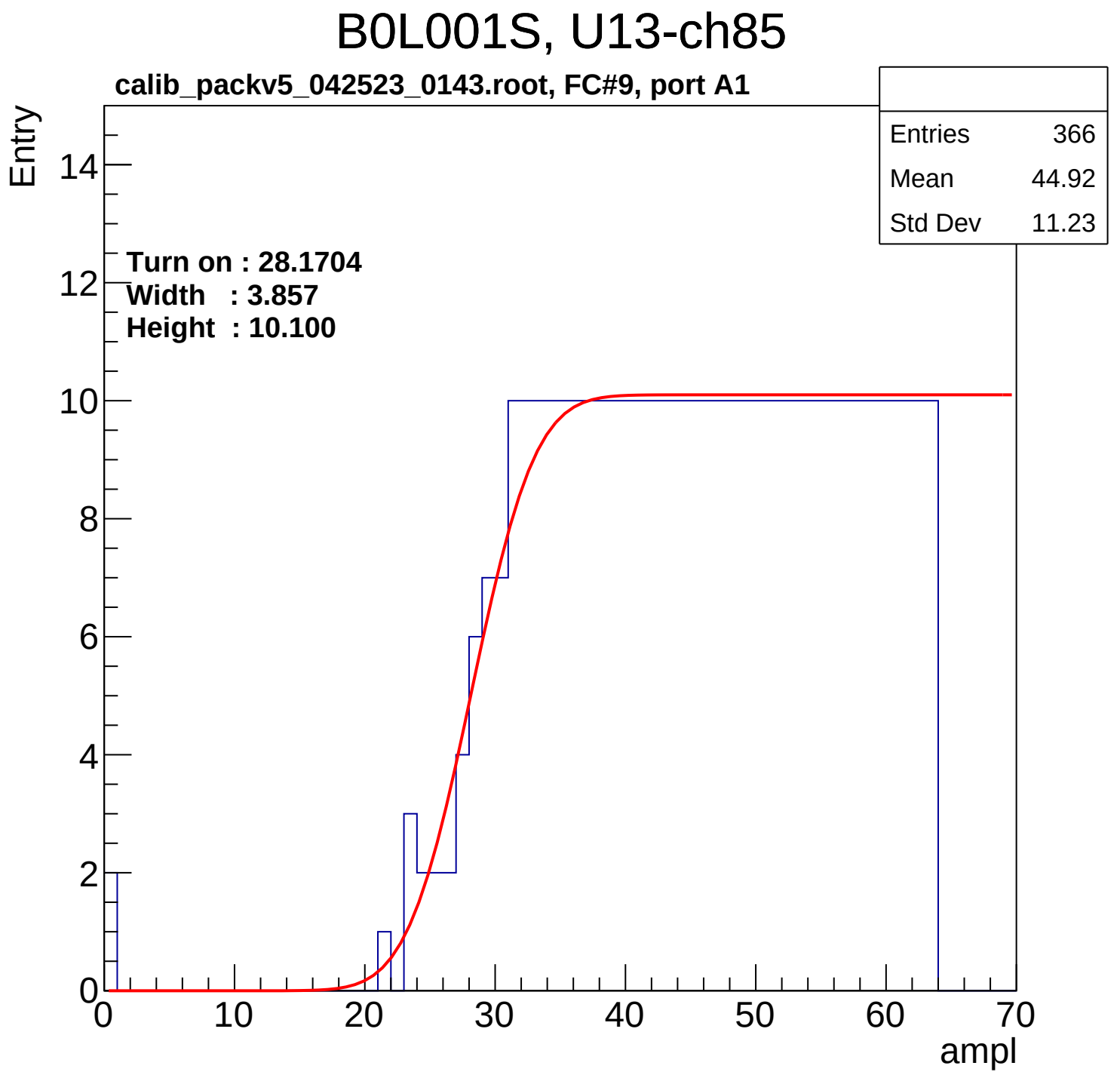
B0L001S, U13-ch85
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.92
Std Dev 11.23
Turn on : 28.1704
Width : 3.857
Height : 10.100
Entry
ampl
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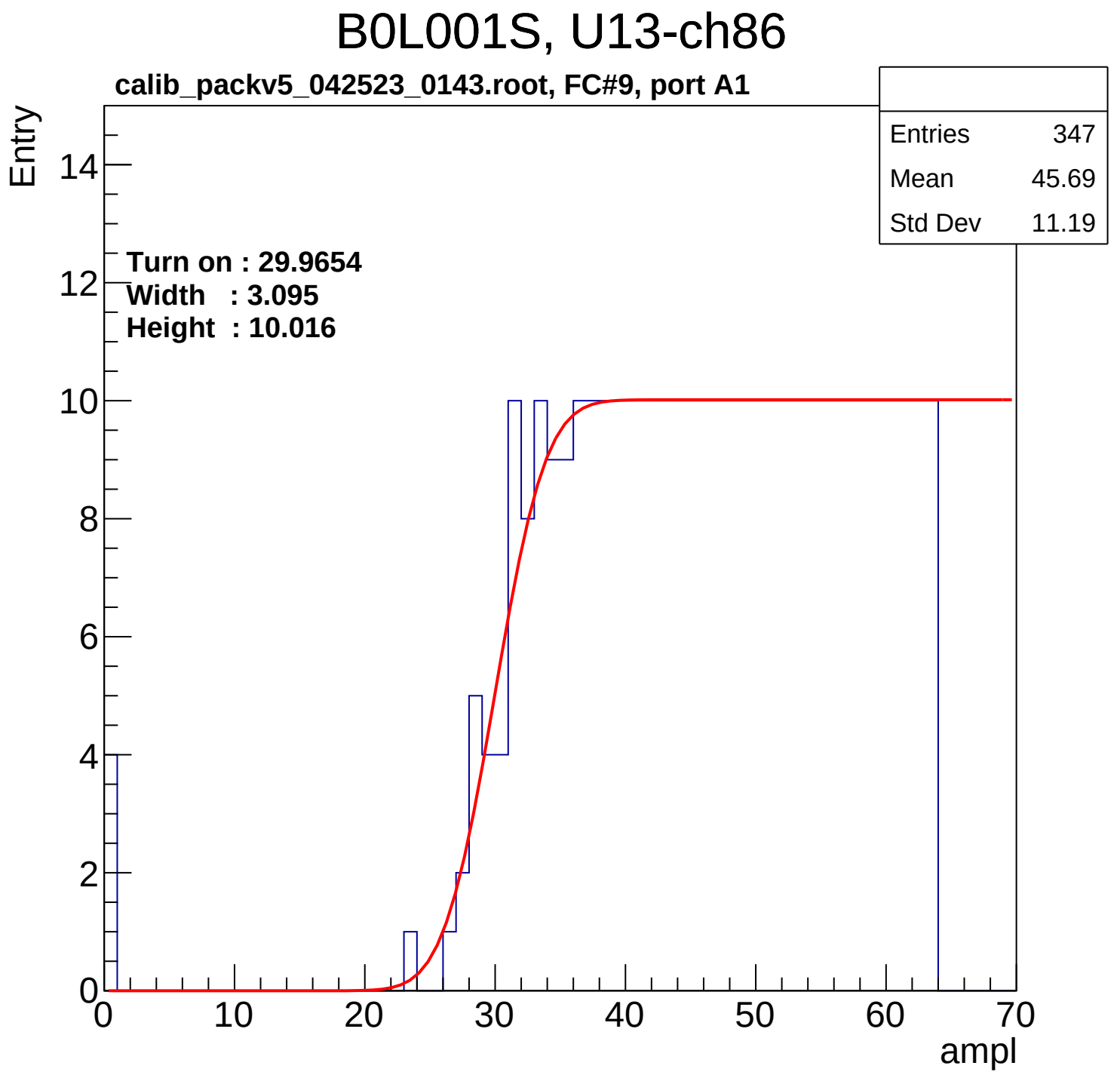
B0L001S, U13-ch86
calib_packv5_042523_0143.root, FC#9, port A1
Entries 347
Mean 45.69
Std Dev 11.19
Turn on : 29.9654
Width : 3.095
Height : 10.016
Entry
ampl
0
2
4
6
8
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12
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10
20
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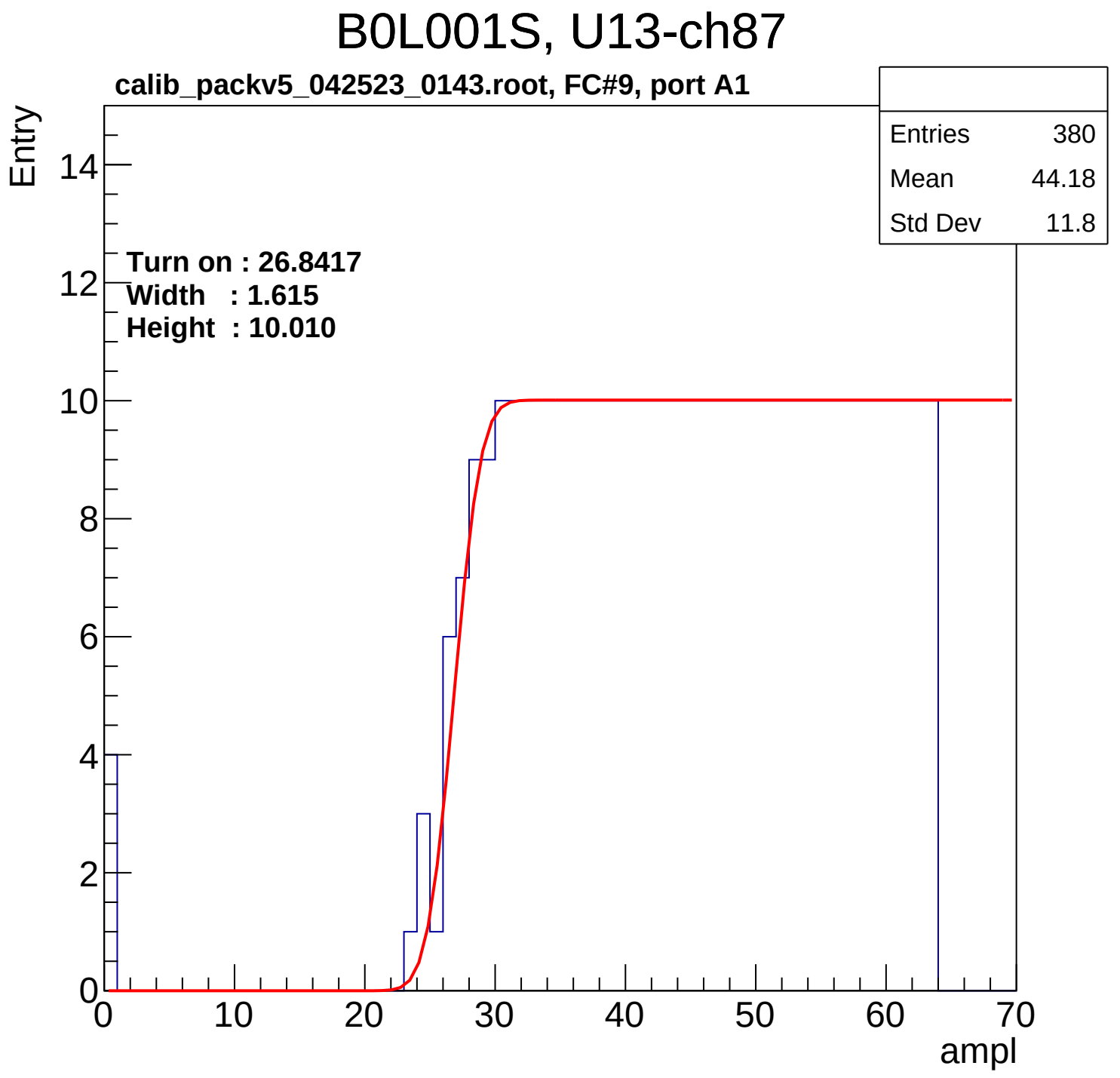
B0L001S, U13-ch87
calib_packv5_042523_0143.root, FC#9, port A1
Entries 380
Mean 44.18
Std Dev 11.8
Turn on : 26.8417
Width : 1.615
Height : 10.010
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ampl
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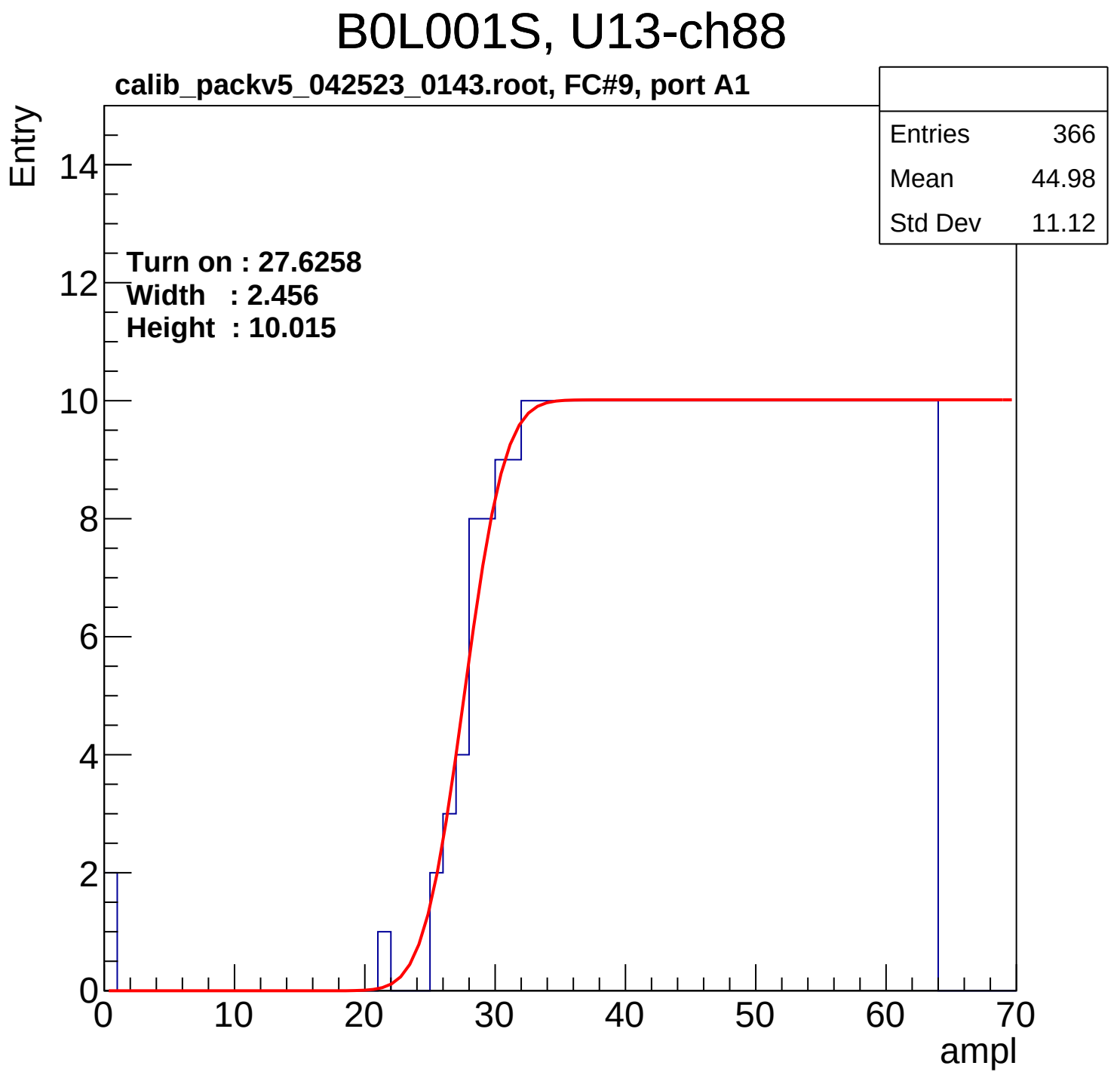
B0L001S, U13-ch88
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.98
Std Dev 11.12
Turn on : 27.6258
Width : 2.456
Height : 10.015
Entry
ampl
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2
4
6
8
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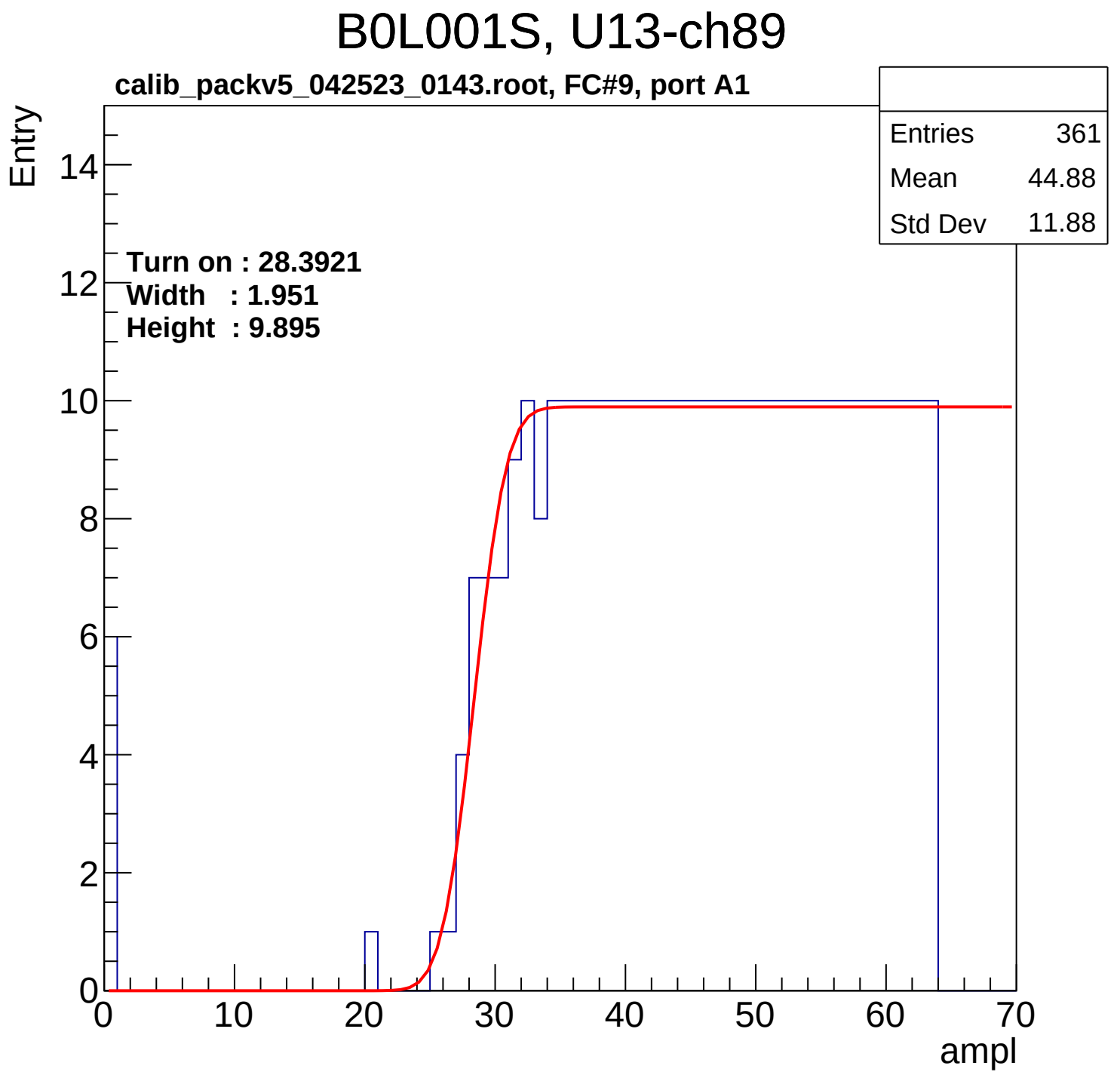
B0L001S, U13-ch89
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 44.88
Std Dev 11.88
Turn on : 28.3921
Width : 1.951
Height : 9.895
Entry
ampl
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2
4
6
8
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12
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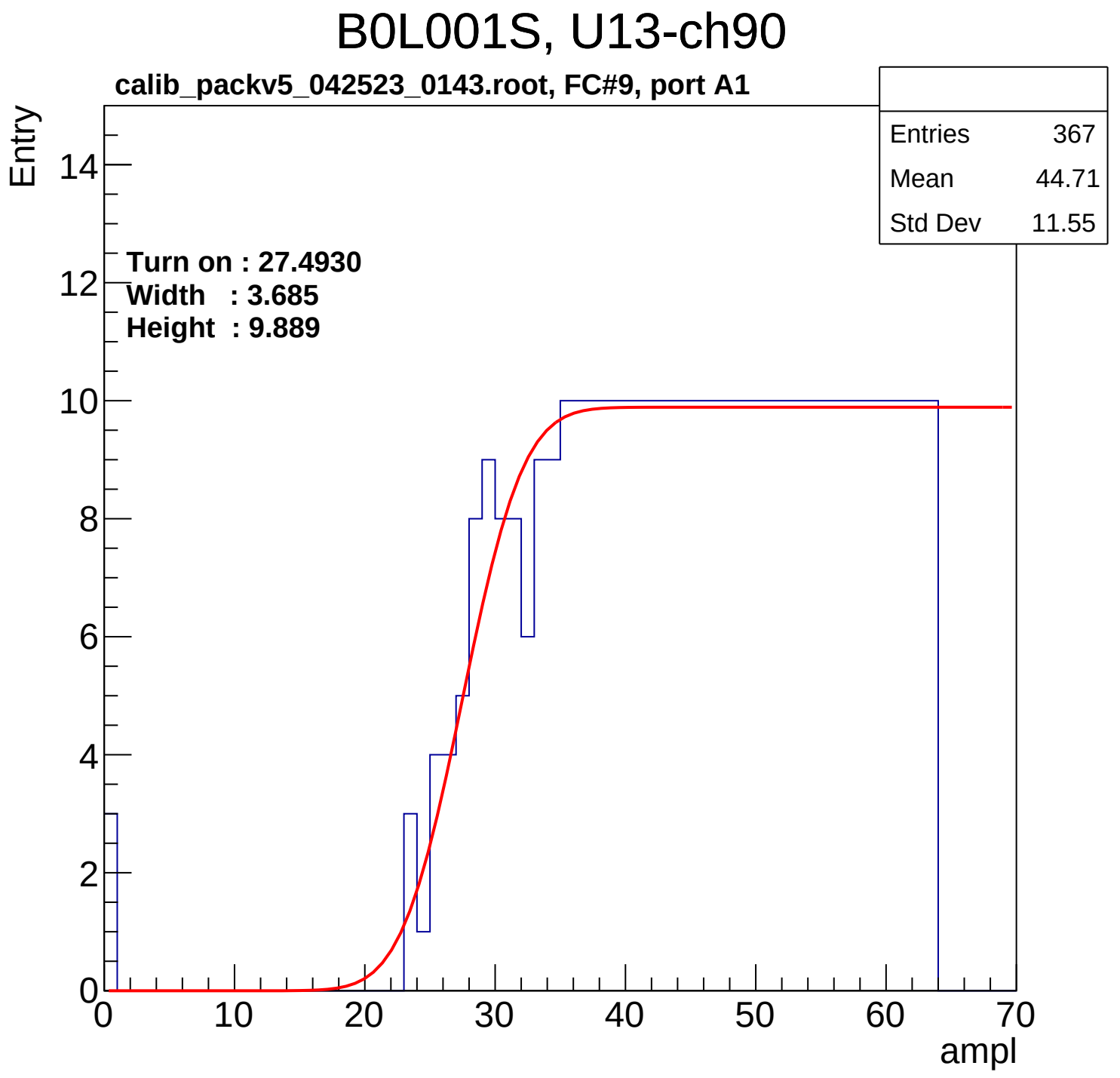
B0L001S, U13-ch90
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.71
Std Dev 11.55
Turn on : 27.4930
Width : 3.685
Height : 9.889
Entry
ampl
0
2
4
6
8
10
12
14
0
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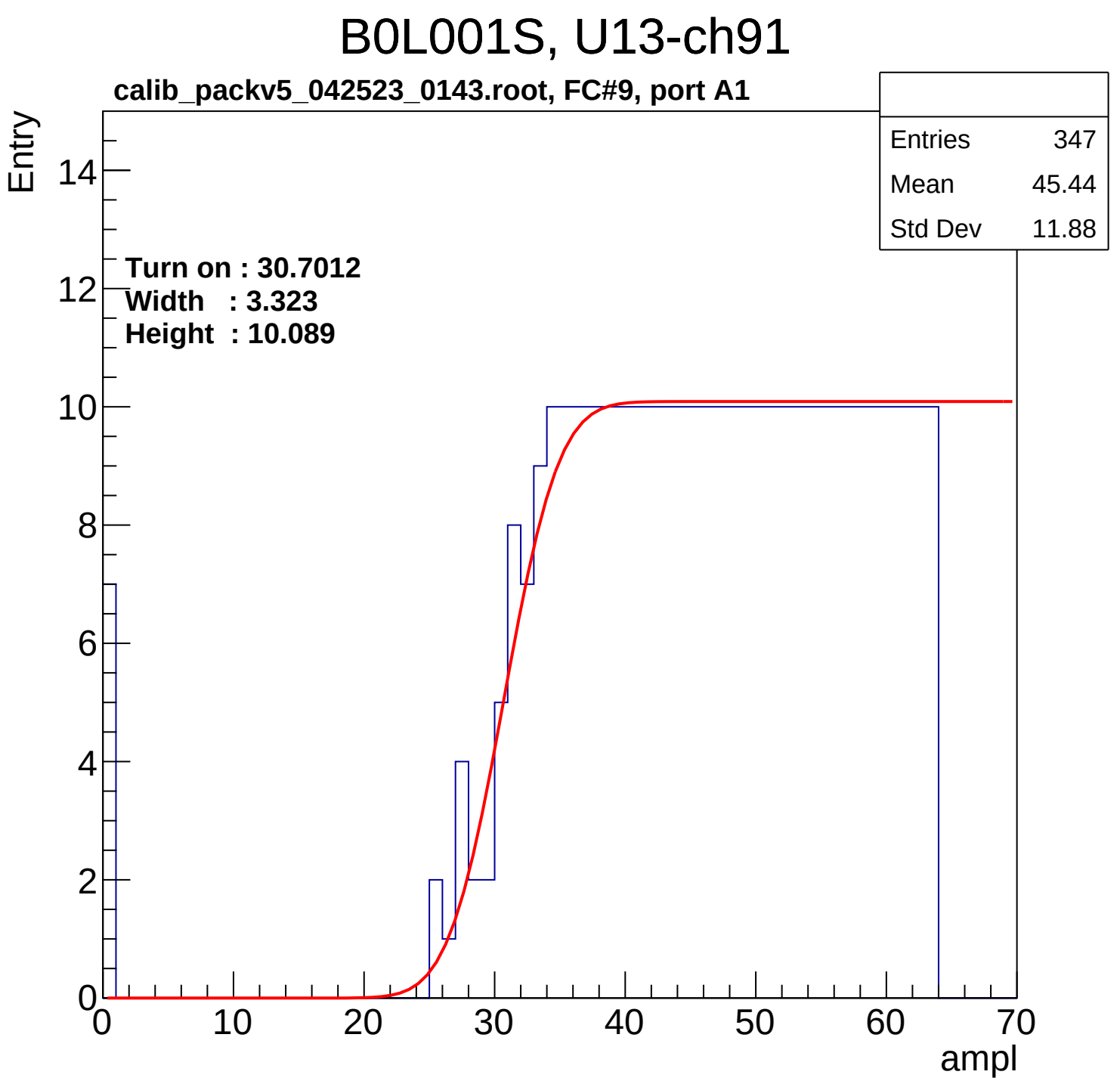
B0L001S, U13-ch91
calib_packv5_042523_0143.root, FC#9, port A1
Entries 347
Mean 45.44
Std Dev 11.88
Turn on : 30.7012
Width : 3.323
Height : 10.089
Entry
ampl
0
2
4
6
8
10
12
14
0
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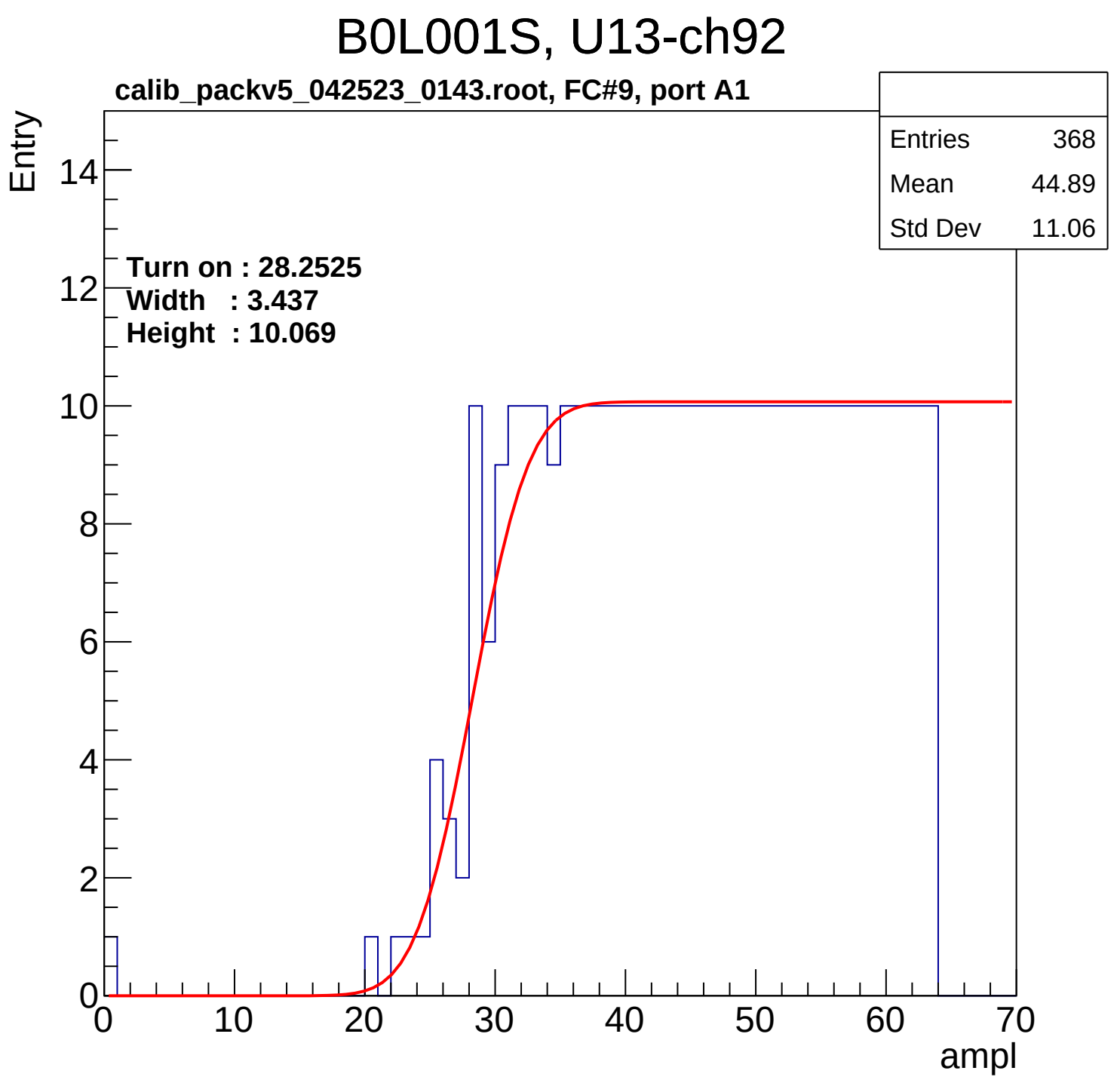
B0L001S, U13-ch92
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.89
Std Dev 11.06
Turn on : 28.2525
Width : 3.437
Height : 10.069
Entry
ampl
0
2
4
6
8
10
12
14
0
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60
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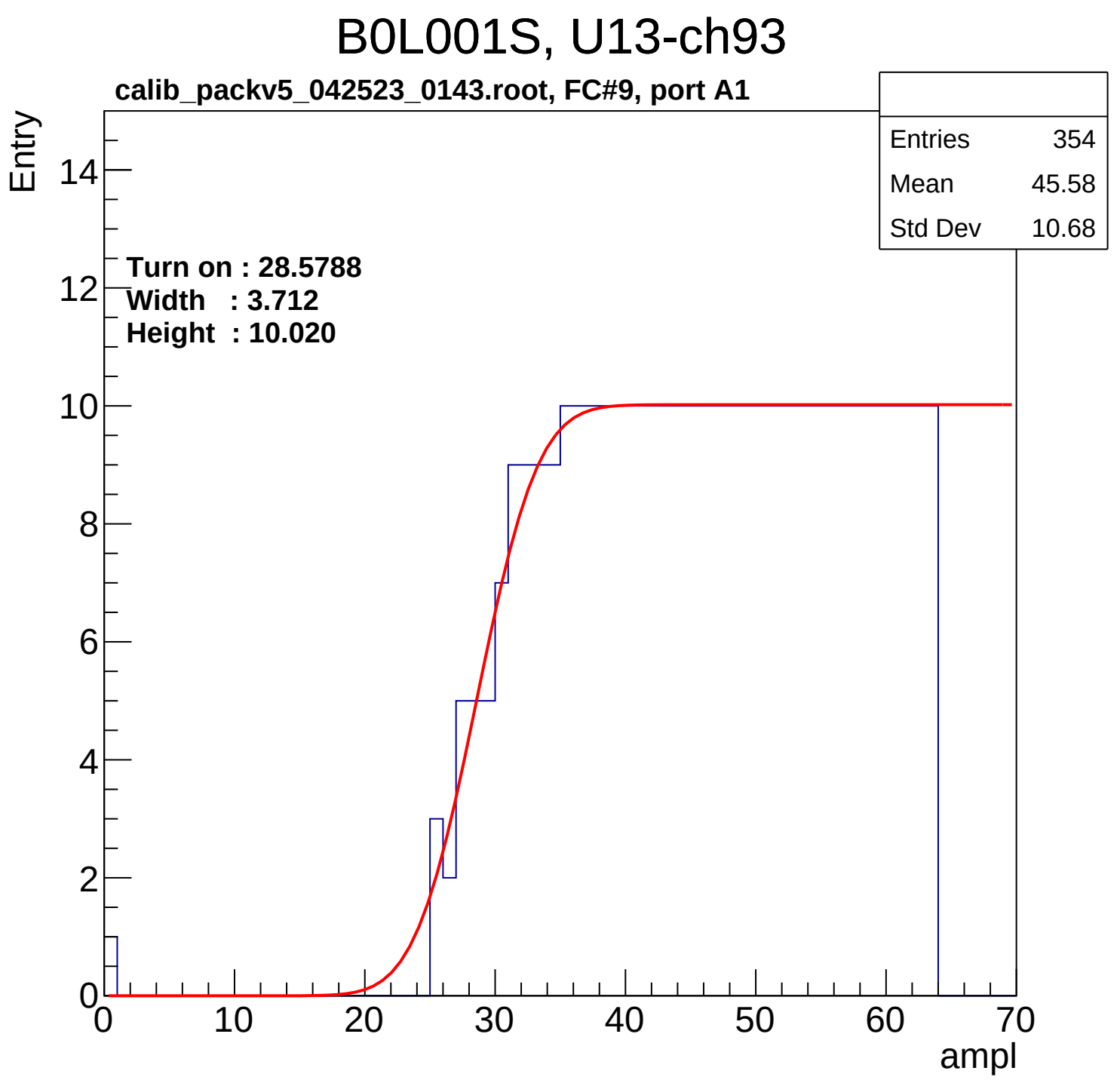
B0L001S, U13-ch93
calib_packv5_042523_0143.root, FC#9, port A1
Entries 354
Mean 45.58
Std Dev 10.68
Turn on : 28.5788
Width : 3.712
Height : 10.020
Entry
ampl
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2
4
6
8
10
12
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0
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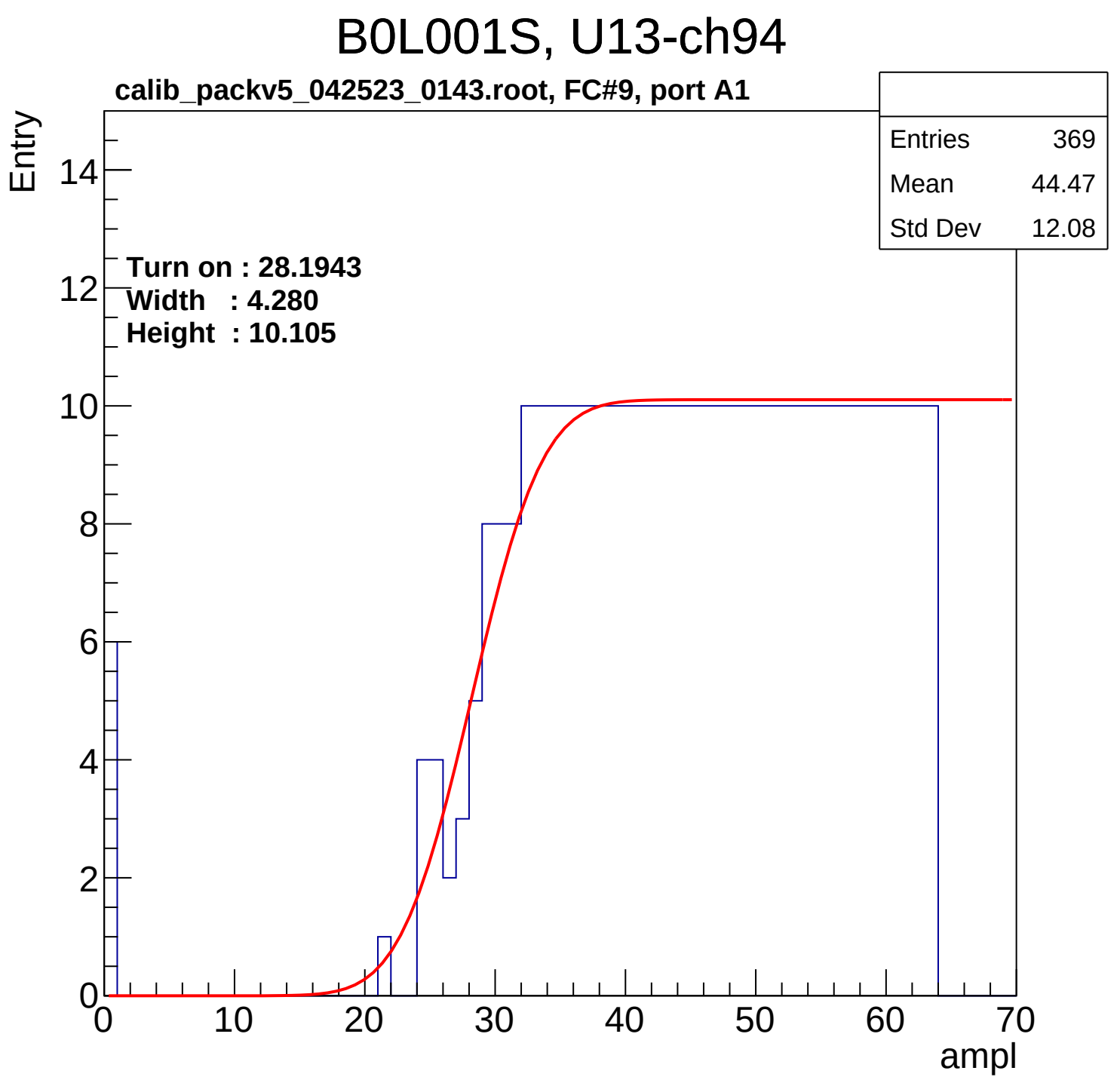
B0L001S, U13-ch94
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.47
Std Dev 12.08
Turn on : 28.1943
Width : 4.280
Height : 10.105
Entry
ampl
0
2
4
6
8
10
12
14
0
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40
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60
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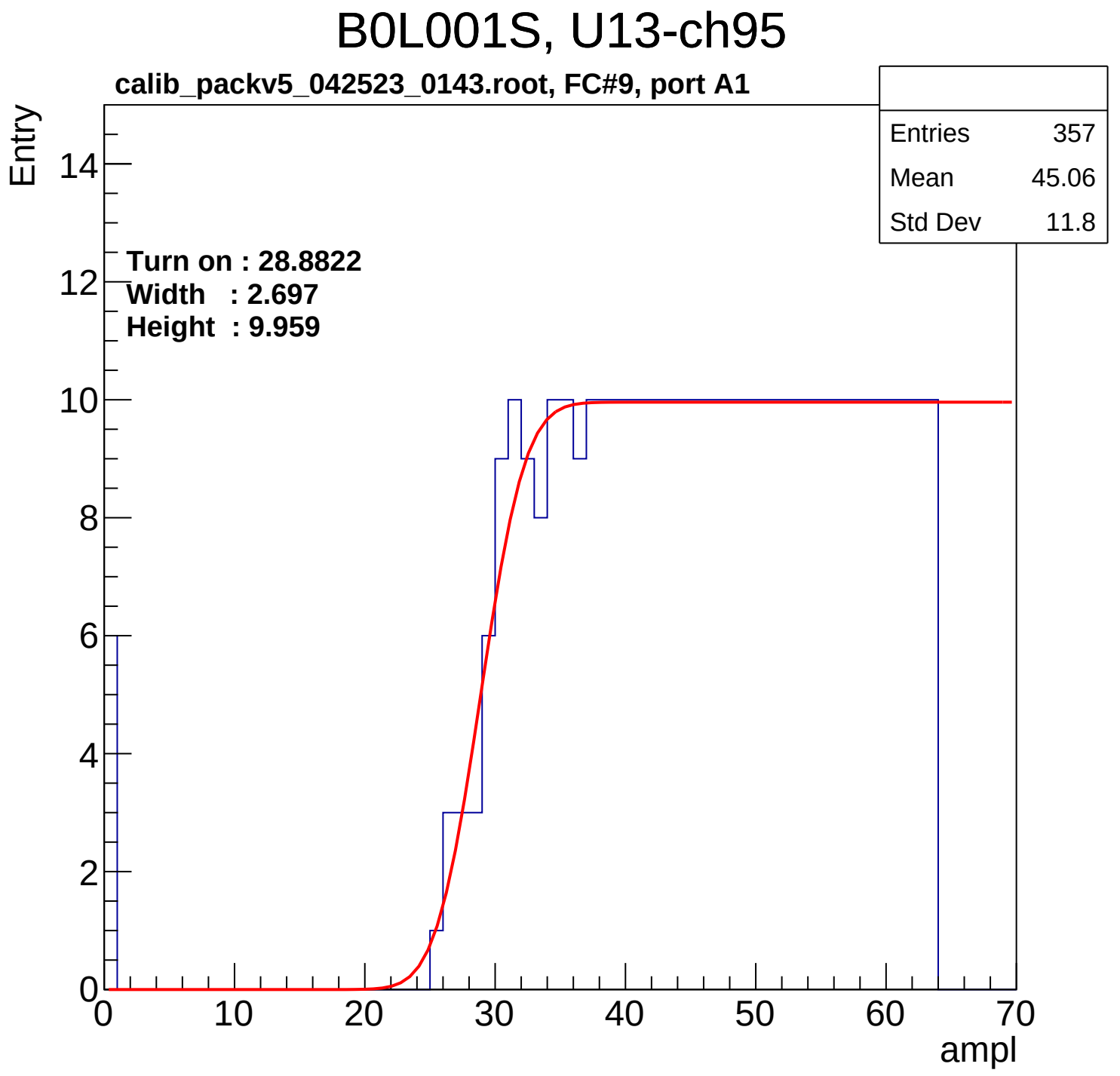
B0L001S, U13-ch95
calib_packv5_042523_0143.root, FC#9, port A1
Entries 357
Mean 45.06
Std Dev 11.8
Turn on : 28.8822
Width : 2.697
Height : 9.959
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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60
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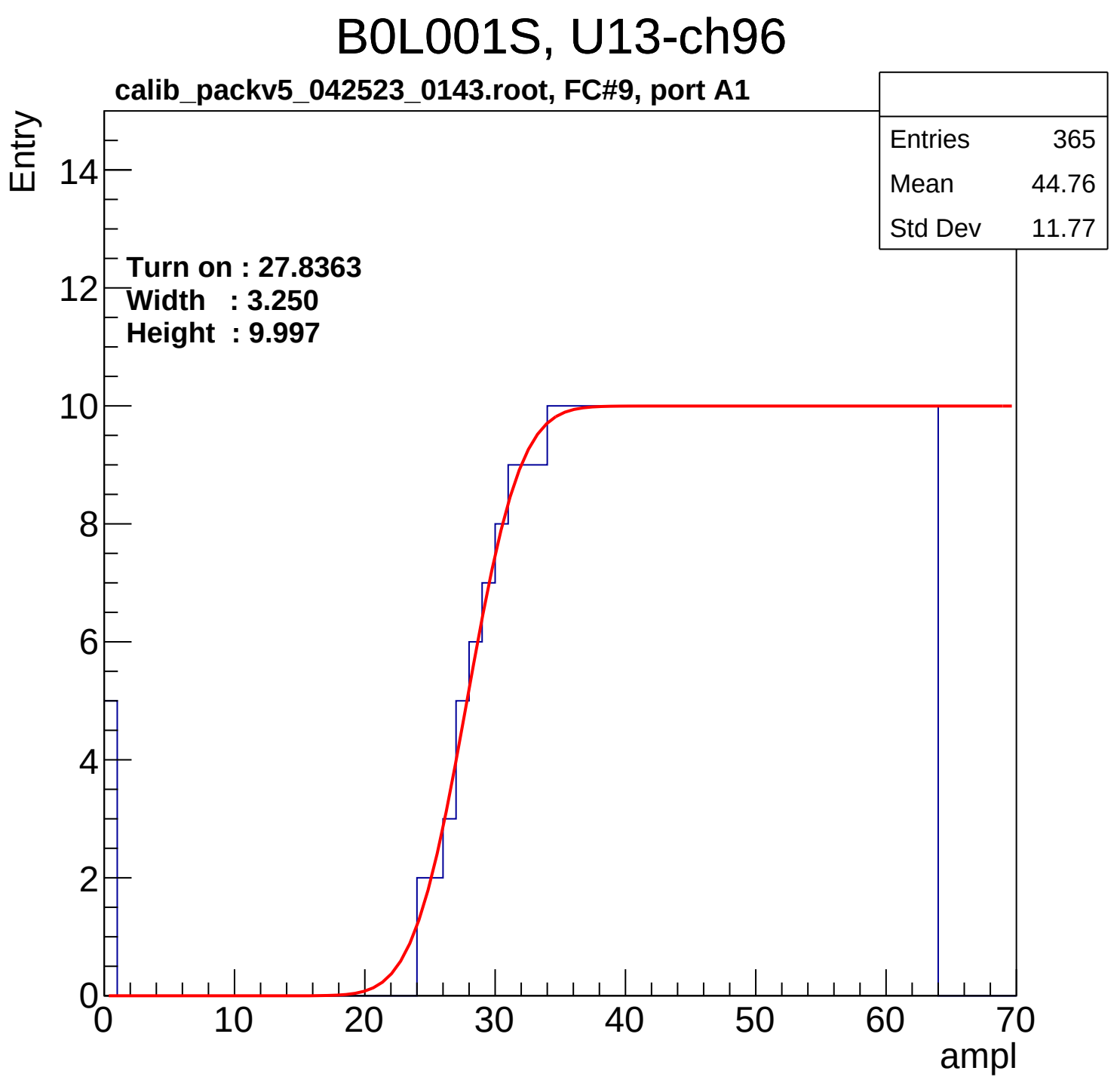
B0L001S, U13-ch96
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 44.76
Std Dev 11.77
Turn on : 27.8363
Width : 3.250
Height : 9.997
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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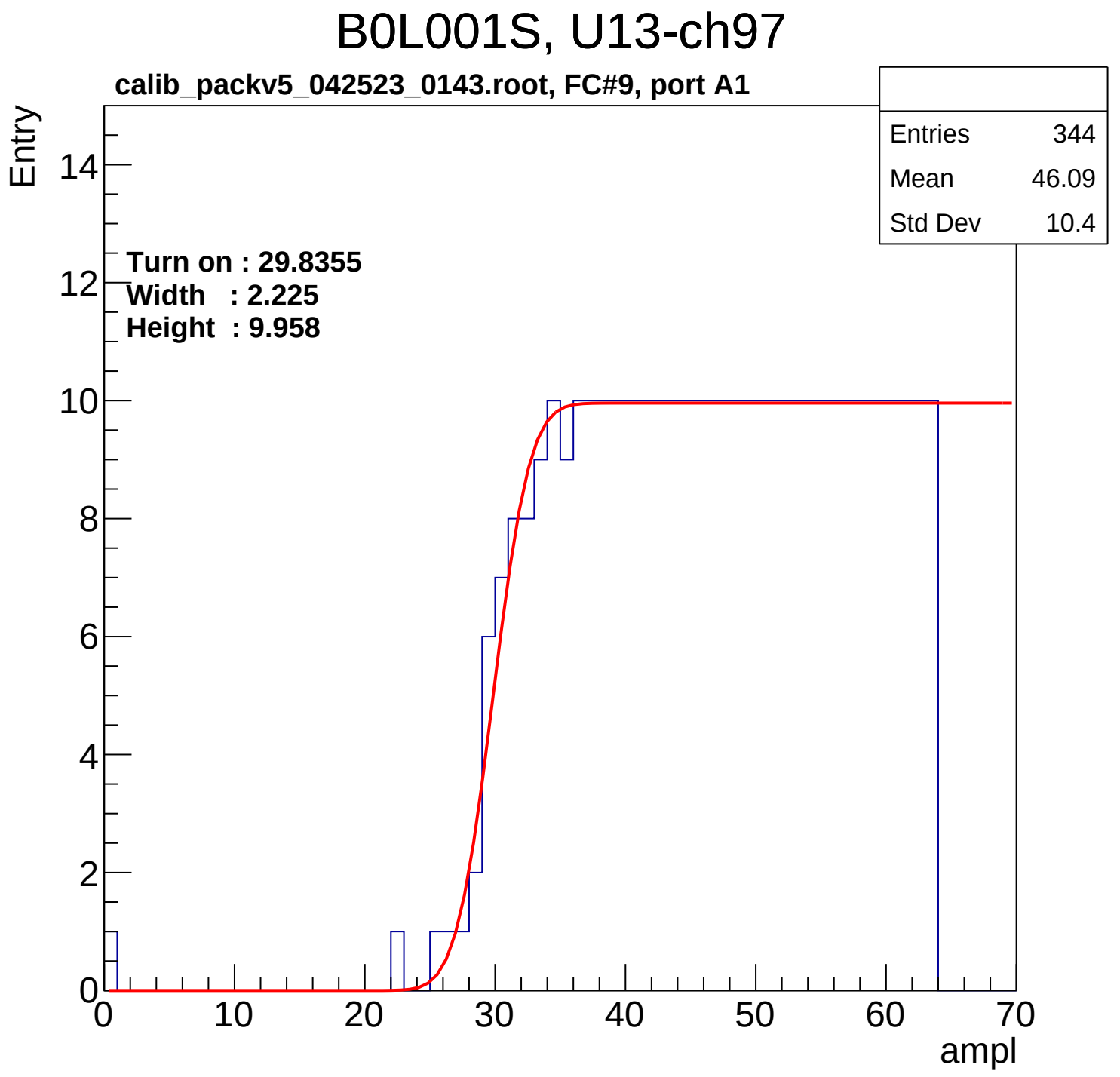
B0L001S, U13-ch97
calib_packv5_042523_0143.root, FC#9, port A1
Entries 344
Mean 46.09
Std Dev 10.4
Turn on : 29.8355
Width : 2.225
Height : 9.958
Entry
ampl
0
2
4
6
8
10
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0
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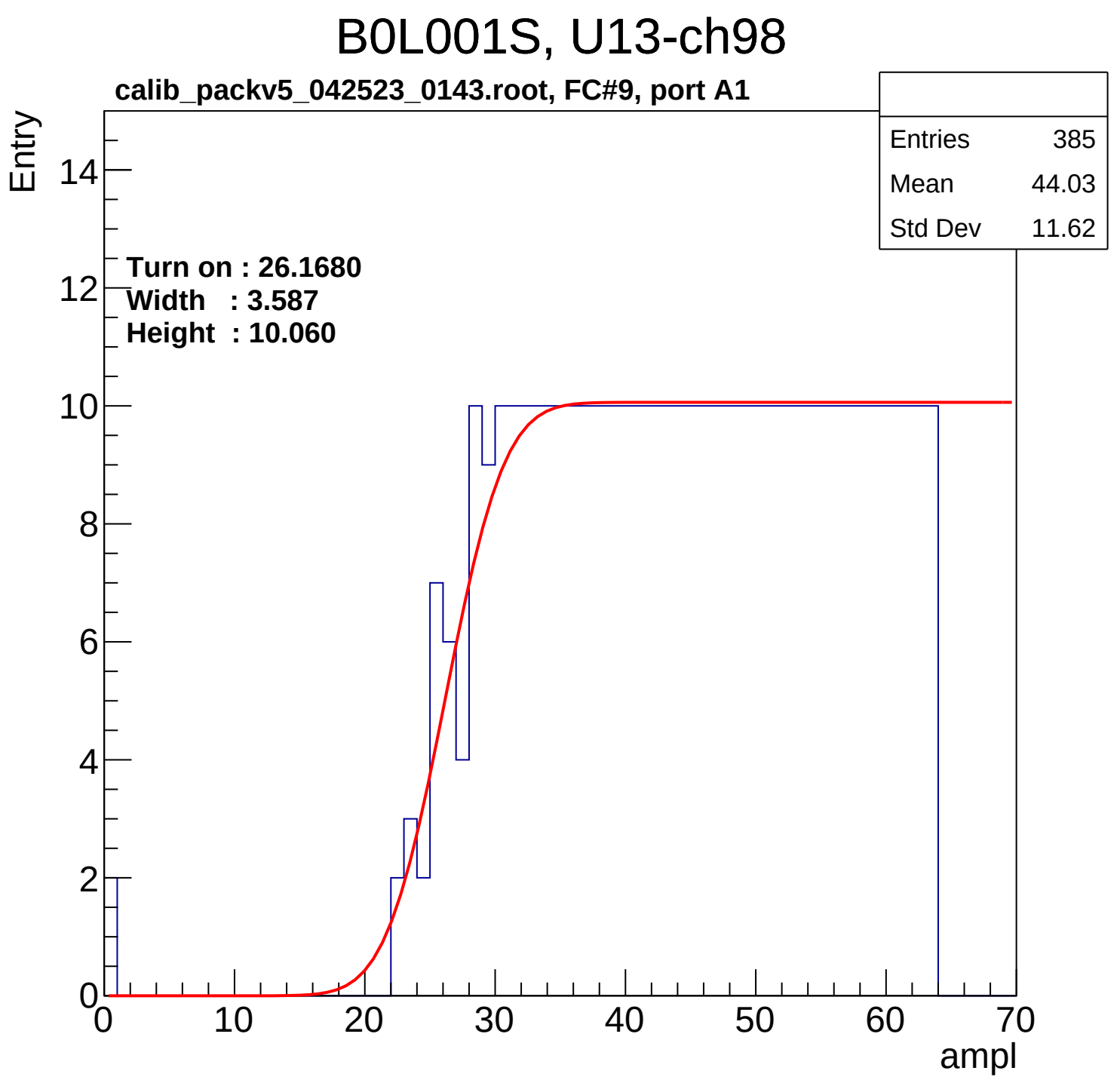
B0L001S, U13-ch98
calib_packv5_042523_0143.root, FC#9, port A1
Entries 385
Mean 44.03
Std Dev 11.62
Turn on : 26.1680
Width : 3.587
Height : 10.060
Entry
ampl
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2
4
6
8
10
12
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0
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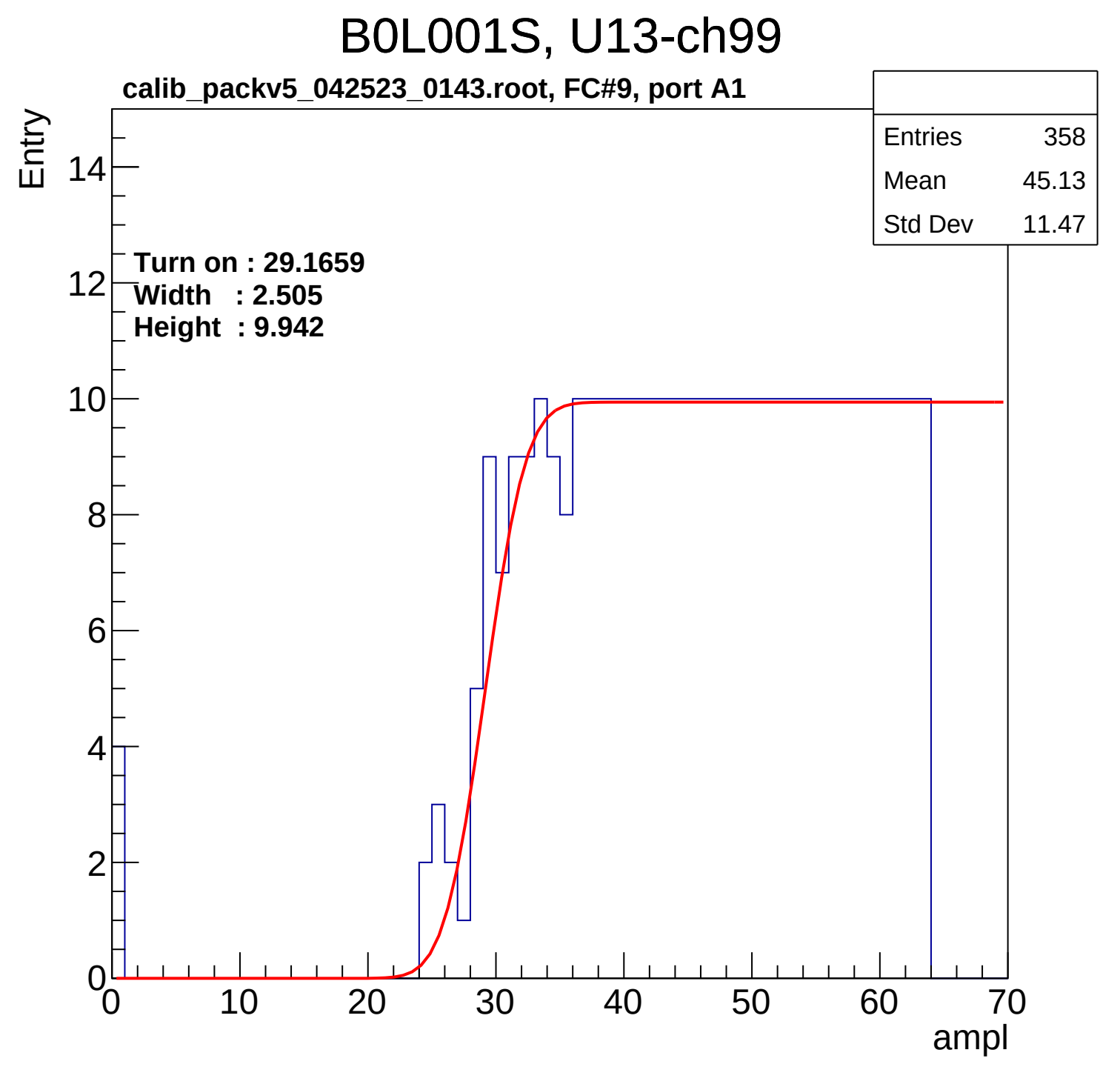
B0L001S, U13-ch99
calib_packv5_042523_0143.root, FC#9, port A1
Entries 358
Mean 45.13
Std Dev 11.47
Turn on : 29.1659
Width : 2.505
Height : 9.942
Entry
ampl
0
2
4
6
8
10
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0
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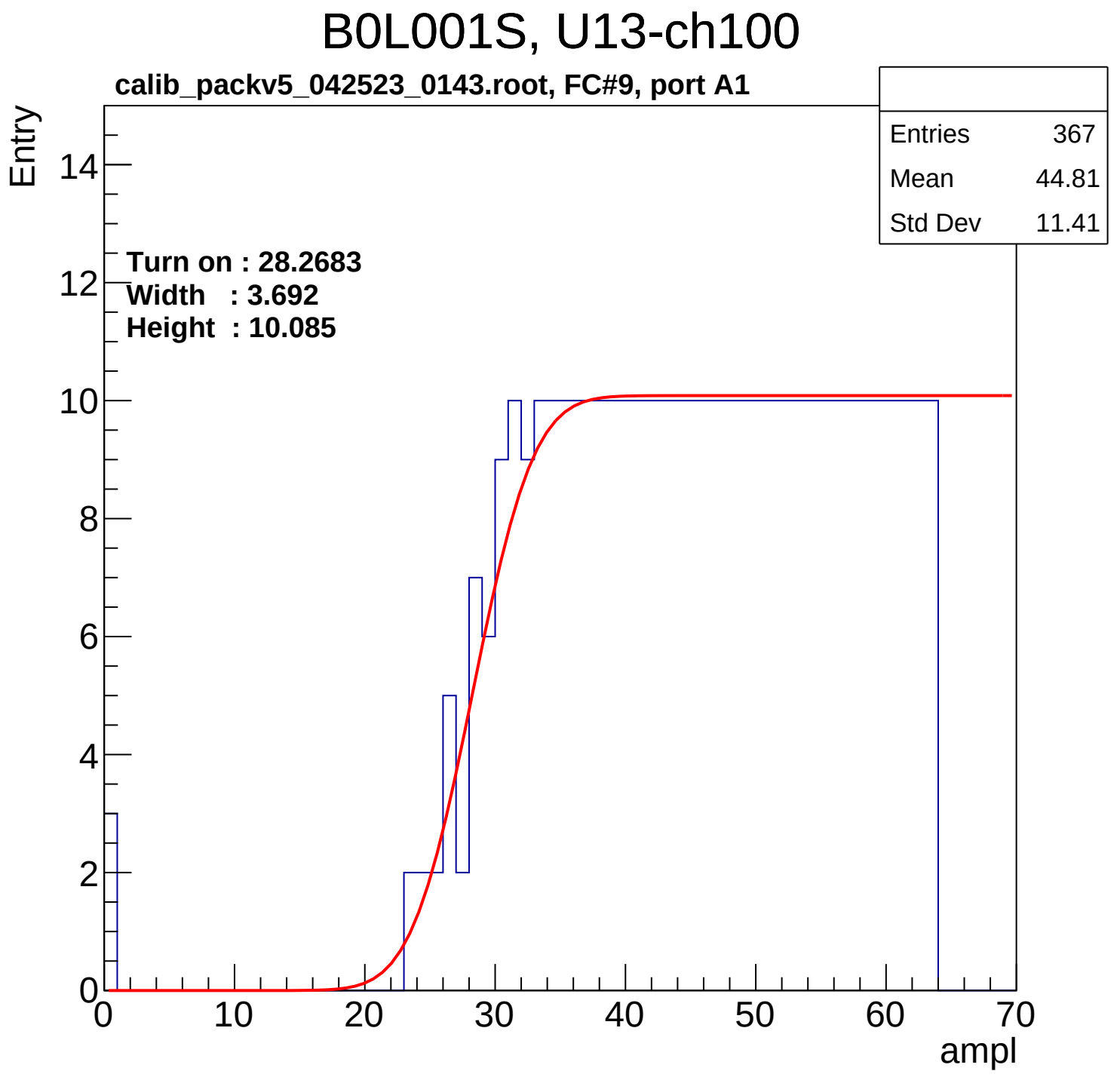
B0L001S, U13-ch100
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.81
Std Dev 11.41
Turn on : 28.2683
Width : 3.692
Height : 10.085
Entry
ampl
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6
8
10
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0
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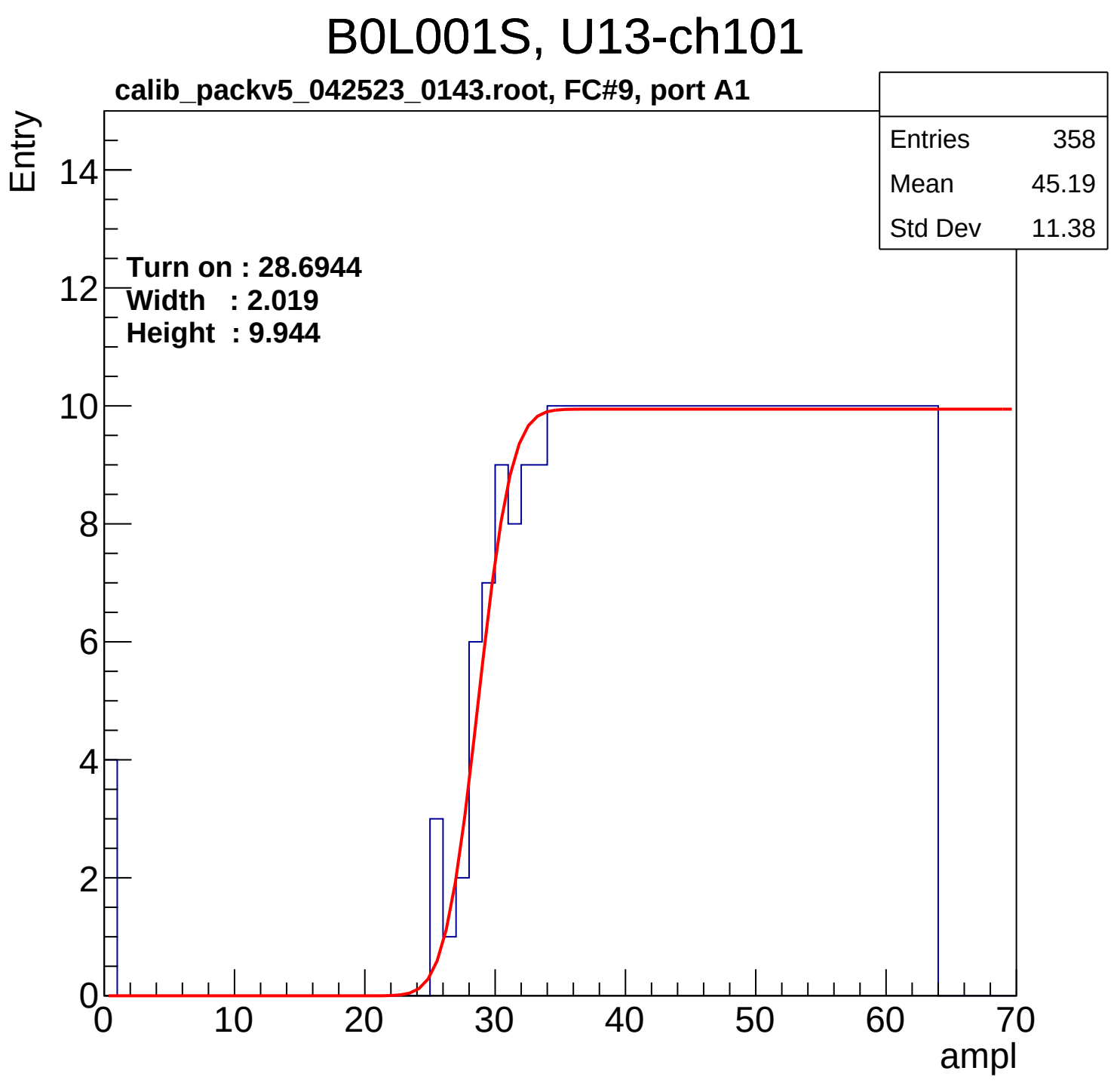
B0L001S, U13-ch101
calib_packv5_042523_0143.root, FC#9, port A1
Entries 358
Mean 45.19
Std Dev 11.38
Turn on : 28.6944
Width : 2.019
Height : 9.944
Entry
ampl
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6
8
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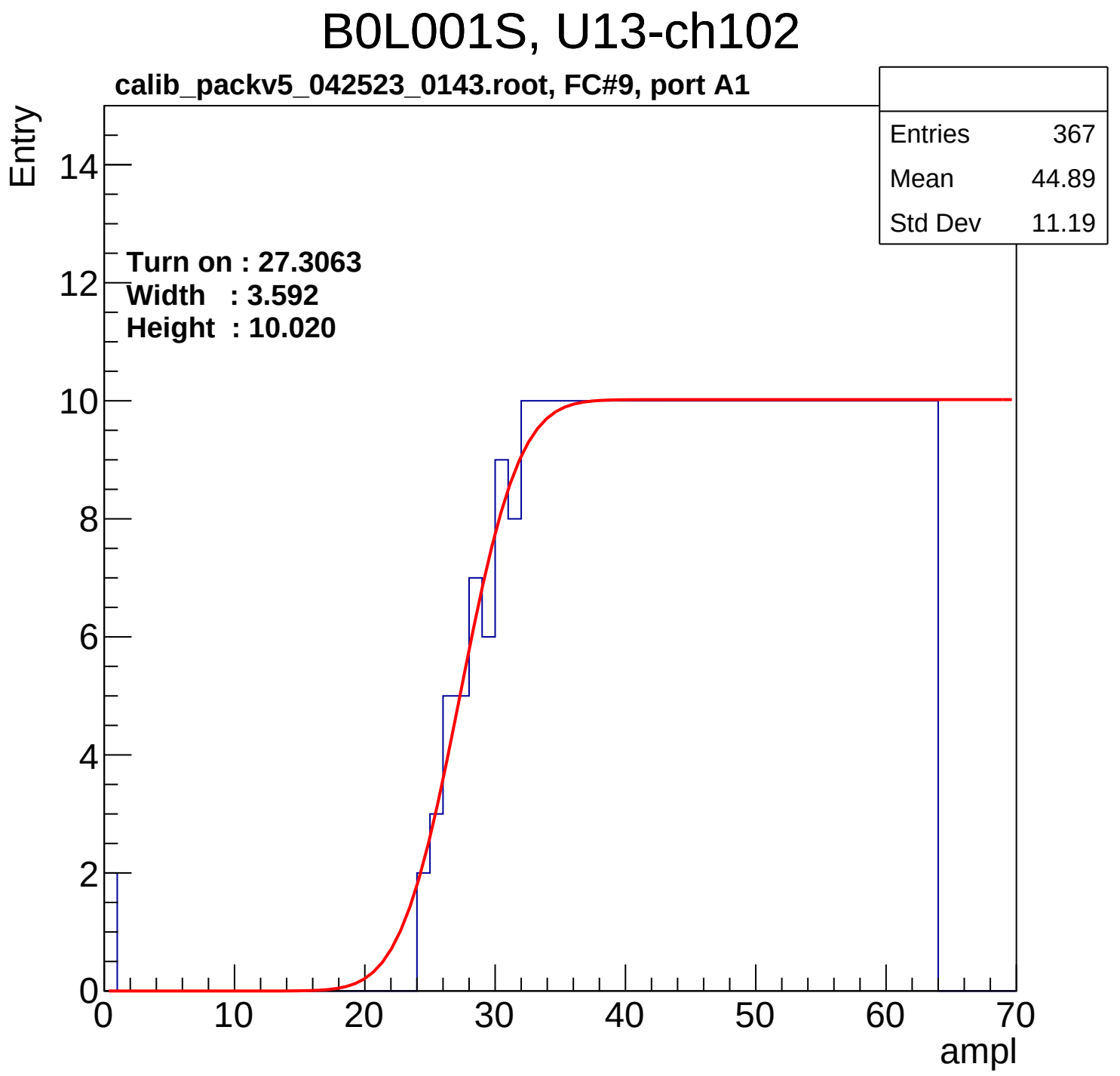
B0L001S, U13-ch102
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.89
Std Dev 11.19
Turn on : 27.3063
Width : 3.592
Height : 10.020
Entry
ampl
0
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4
6
8
10
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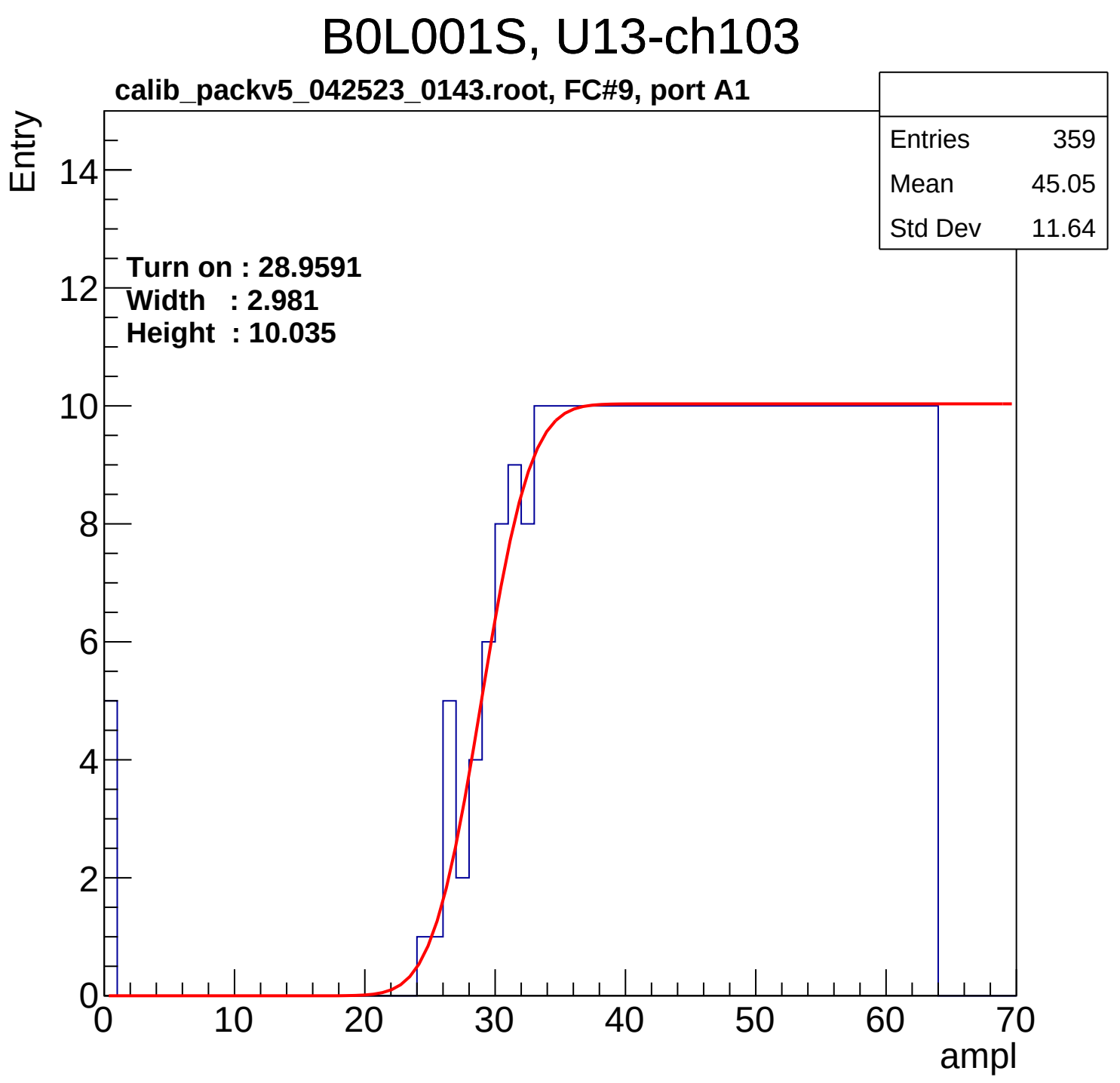
B0L001S, U13-ch103
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 45.05
Std Dev 11.64
Turn on : 28.9591
Width : 2.981
Height : 10.035
Entry
ampl
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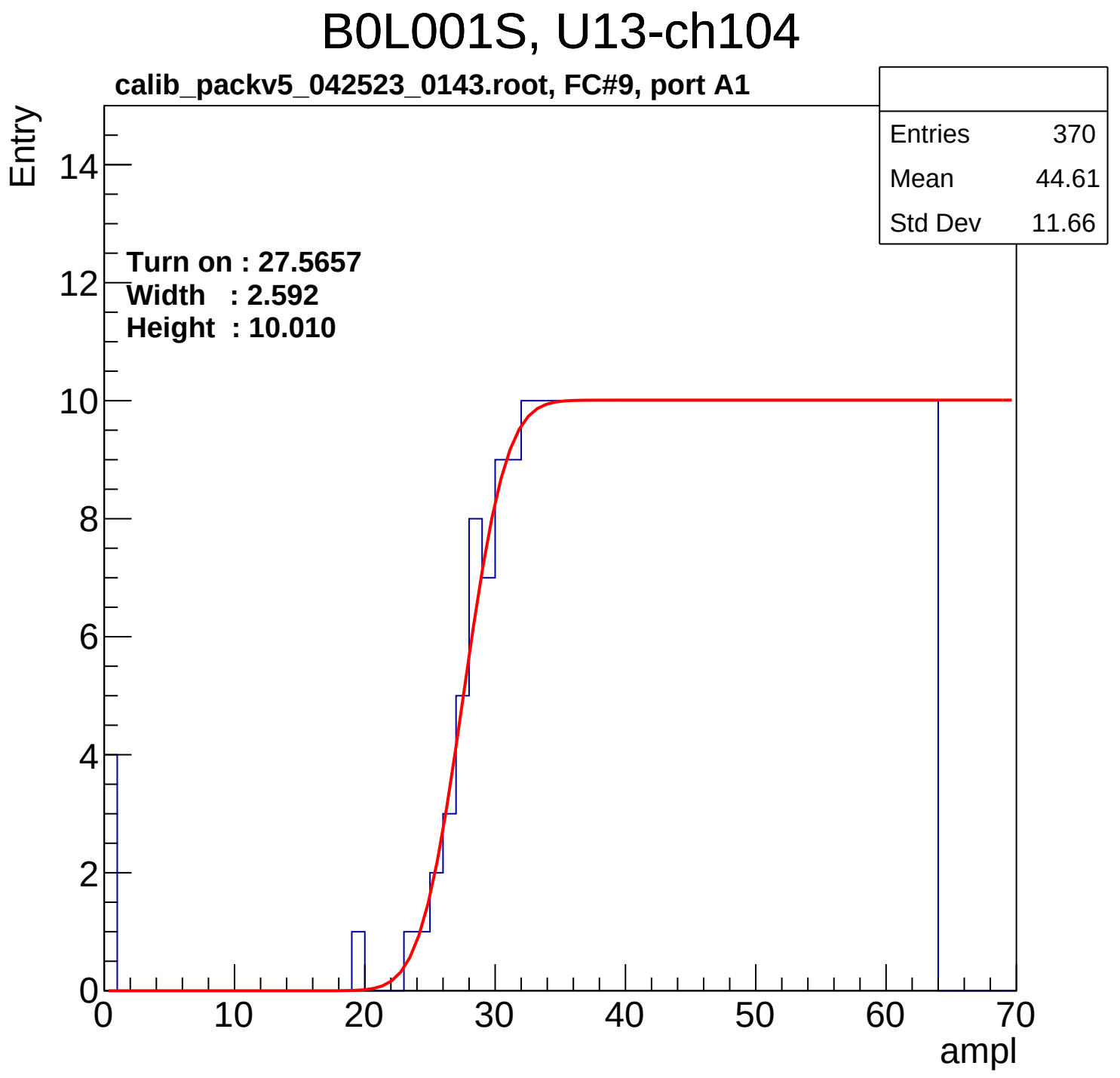
B0L001S, U13-ch104
calib_packv5_042523_0143.root, FC#9, port A1
Entries 370
Mean 44.61
Std Dev 11.66
Turn on : 27.5657
Width : 2.592
Height : 10.010
Entry
ampl
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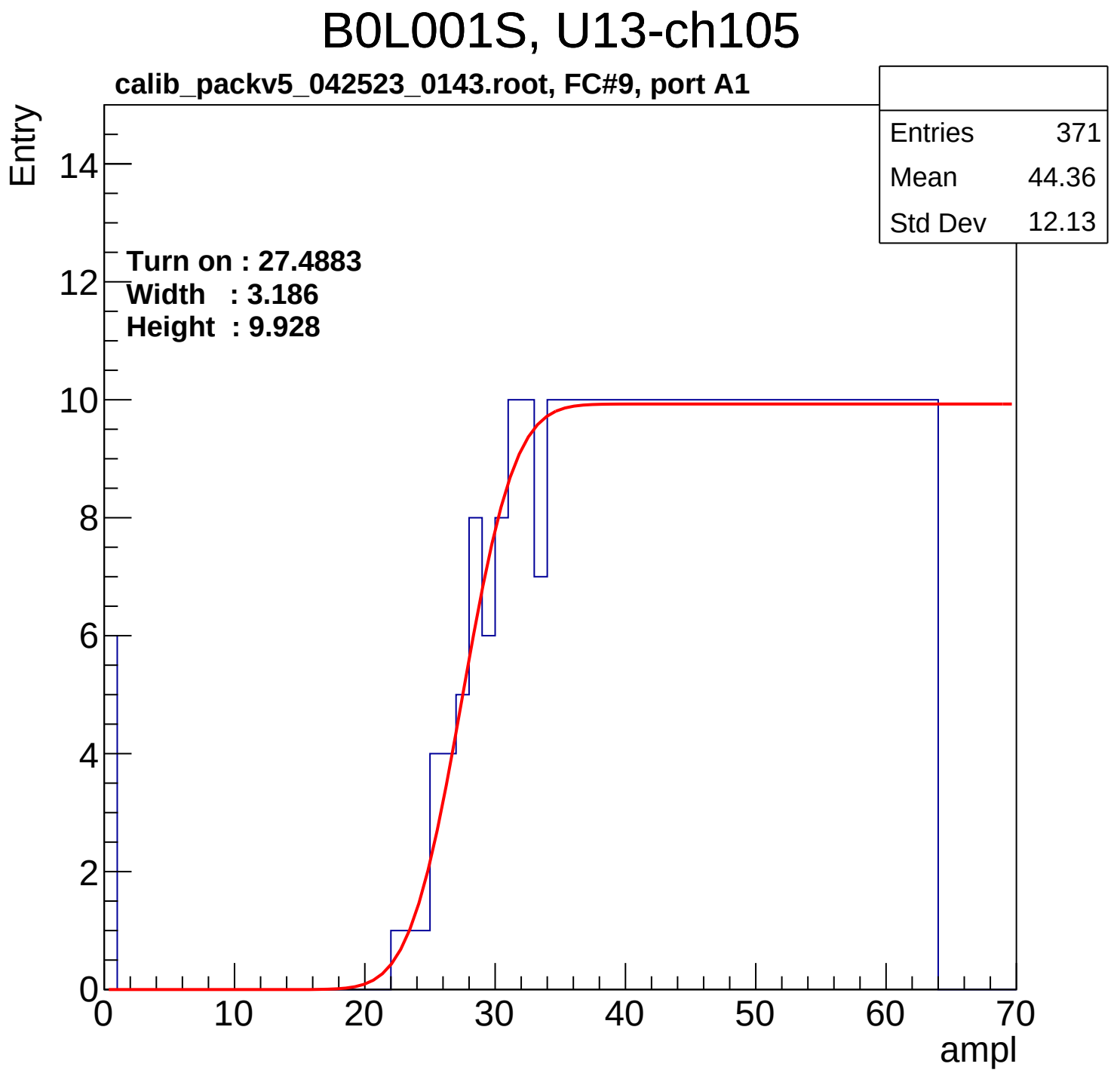
B0L001S, U13-ch105
calib_packv5_042523_0143.root, FC#9, port A1
Entries 371
Mean 44.36
Std Dev 12.13
Turn on : 27.4883
Width : 3.186
Height : 9.928
Entry
ampl
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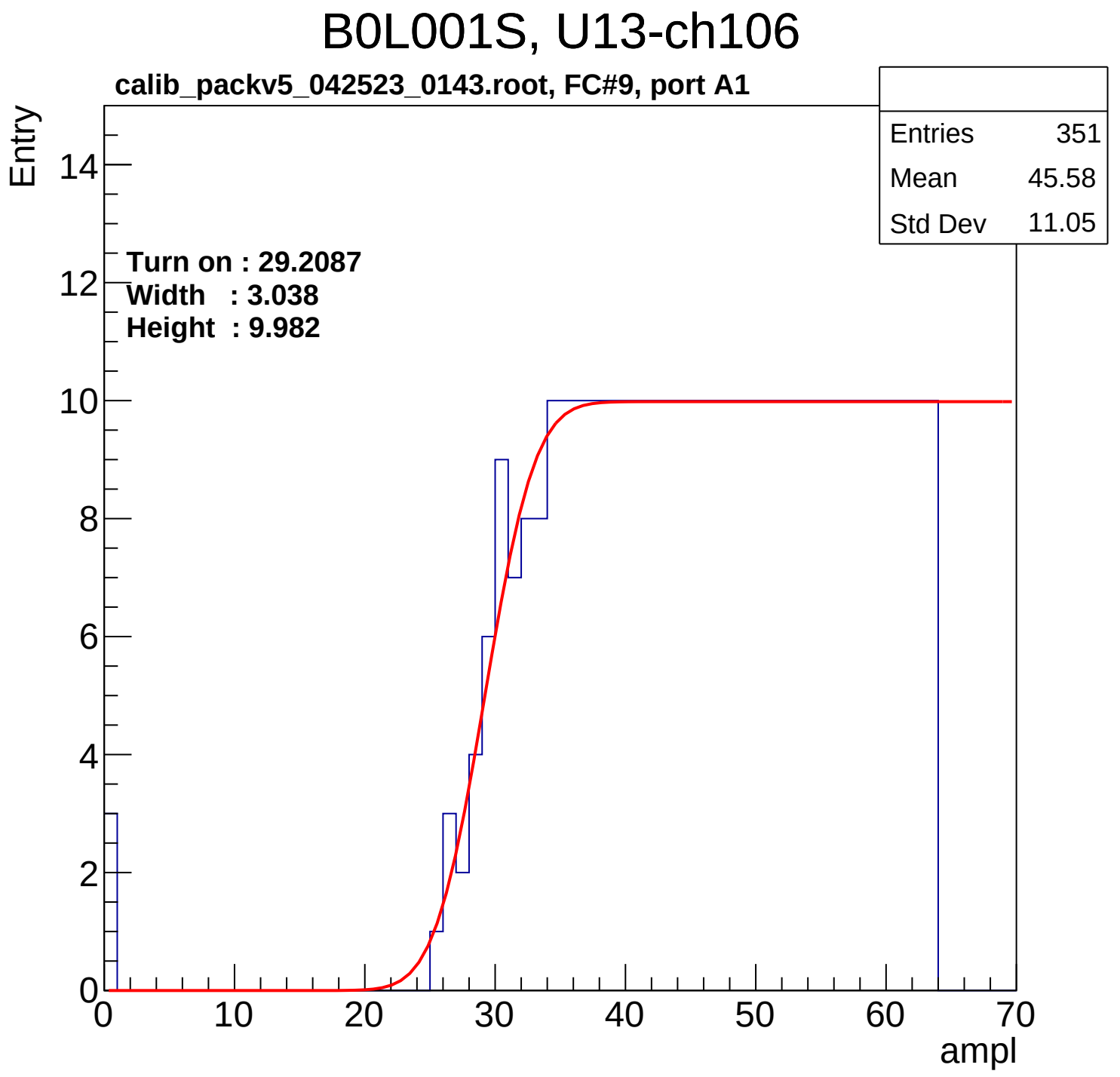
B0L001S, U13-ch106
calib_packv5_042523_0143.root, FC#9, port A1
Entries 351
Mean 45.58
Std Dev 11.05
Turn on : 29.2087
Width : 3.038
Height : 9.982
Entry
ampl
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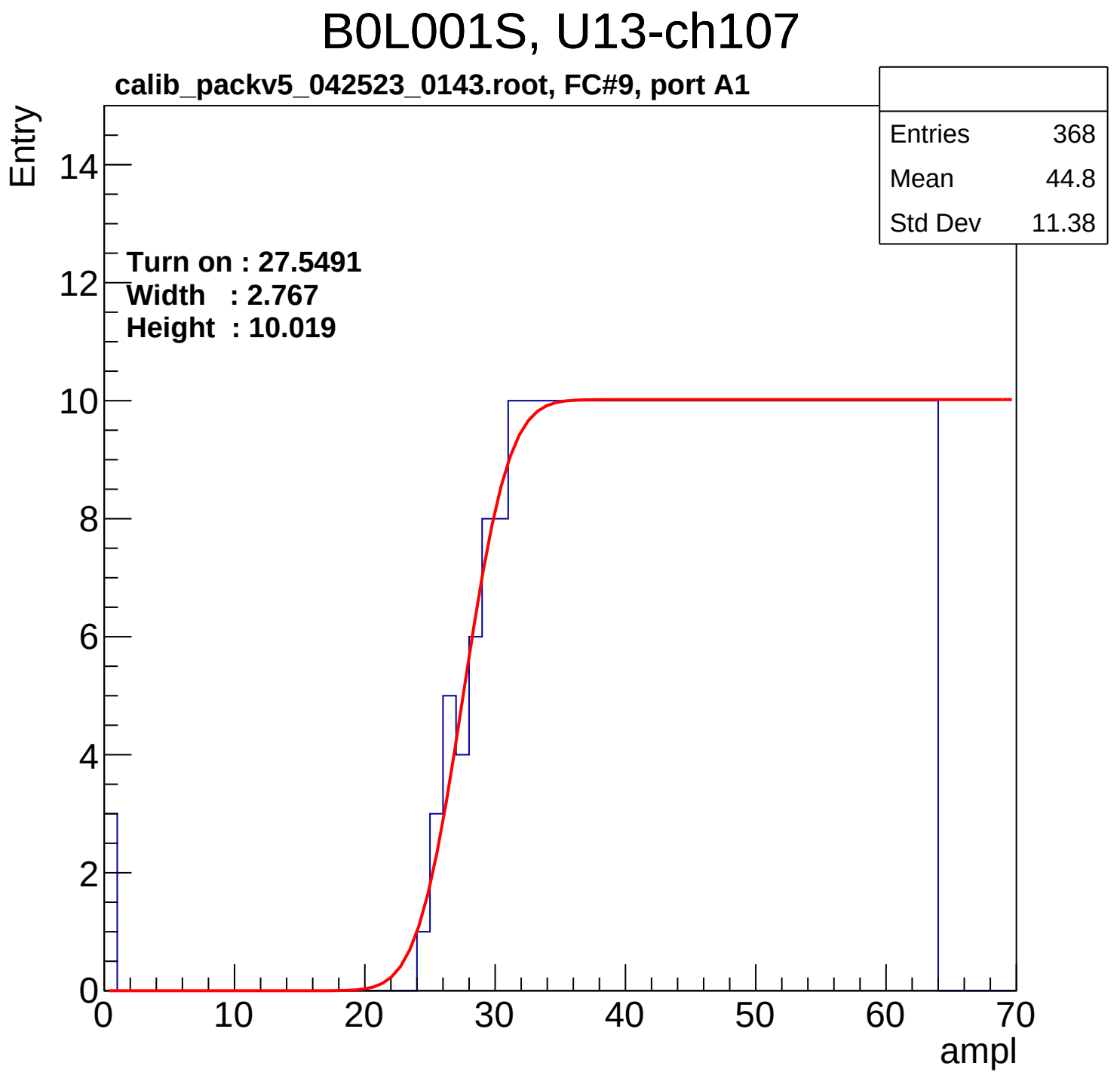
B0L001S, U13-ch107
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.8
Std Dev 11.38
Turn on : 27.5491
Width : 2.767
Height : 10.019
Entry
ampl
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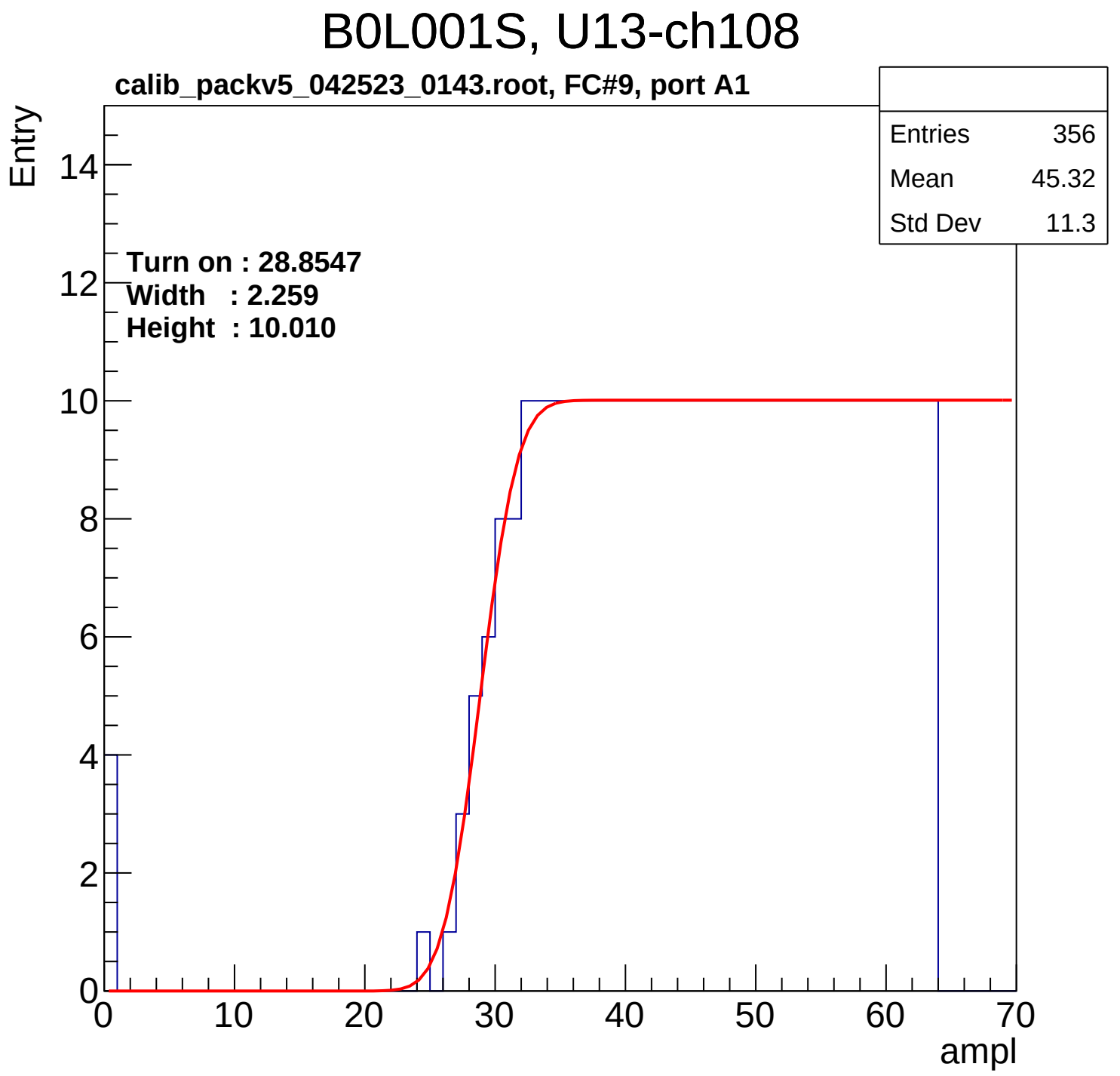
B0L001S, U13-ch108
calib_packv5_042523_0143.root, FC#9, port A1
Entries 356
Mean 45.32
Std Dev 11.3
Turn on : 28.8547
Width : 2.259
Height : 10.010
Entry
ampl
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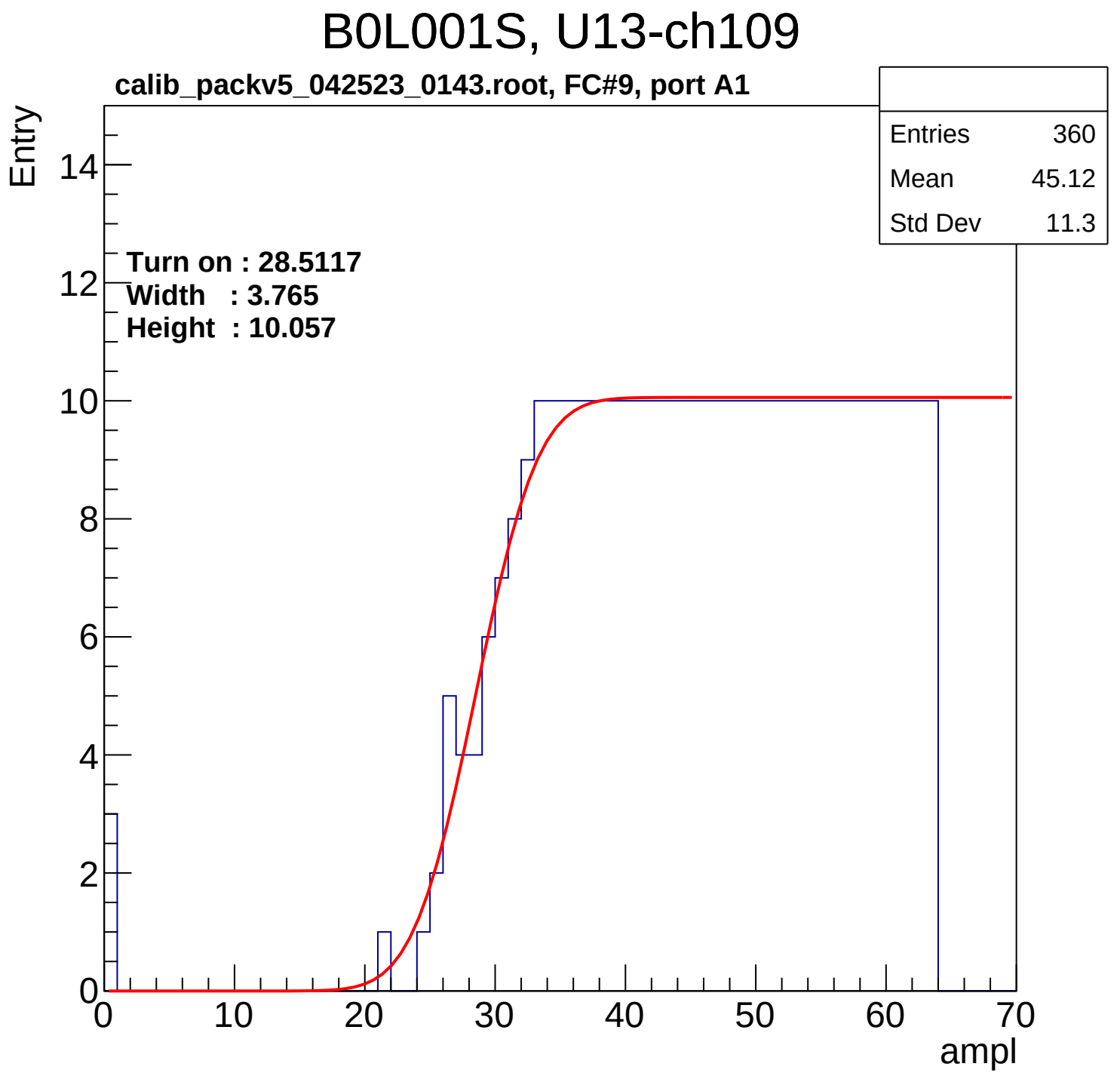
B0L001S, U13-ch109
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 45.12
Std Dev 11.3
Turn on : 28.5117
Width : 3.765
Height : 10.057
Entry
ampl
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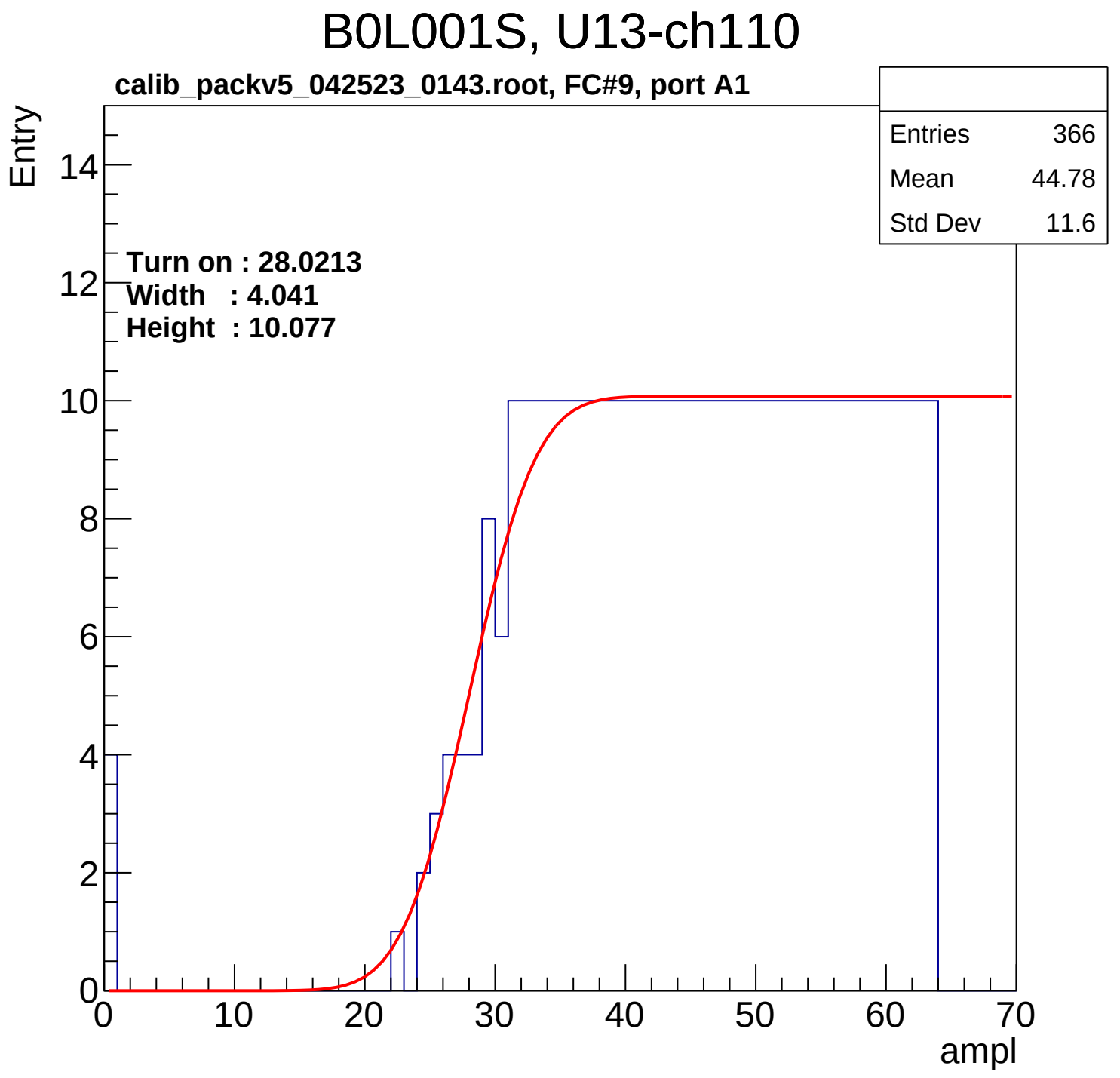
B0L001S, U13-ch110
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.78
Std Dev 11.6
Turn on : 28.0213
Width : 4.041
Height : 10.077
Entry
ampl
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6
8
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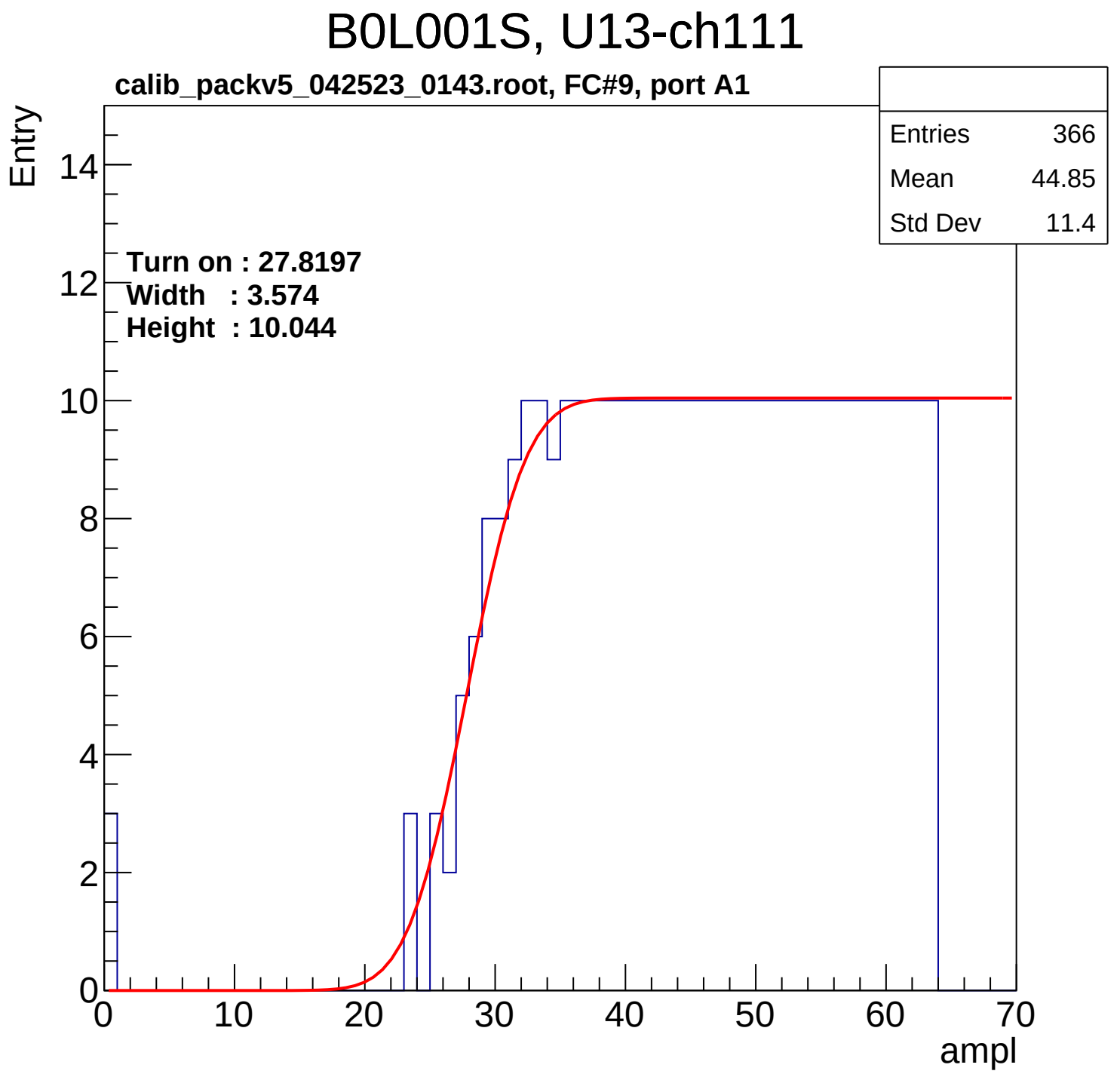
B0L001S, U13-ch111
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.85
Std Dev 11.4
Turn on : 27.8197
Width : 3.574
Height : 10.044
Entry
ampl
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6
8
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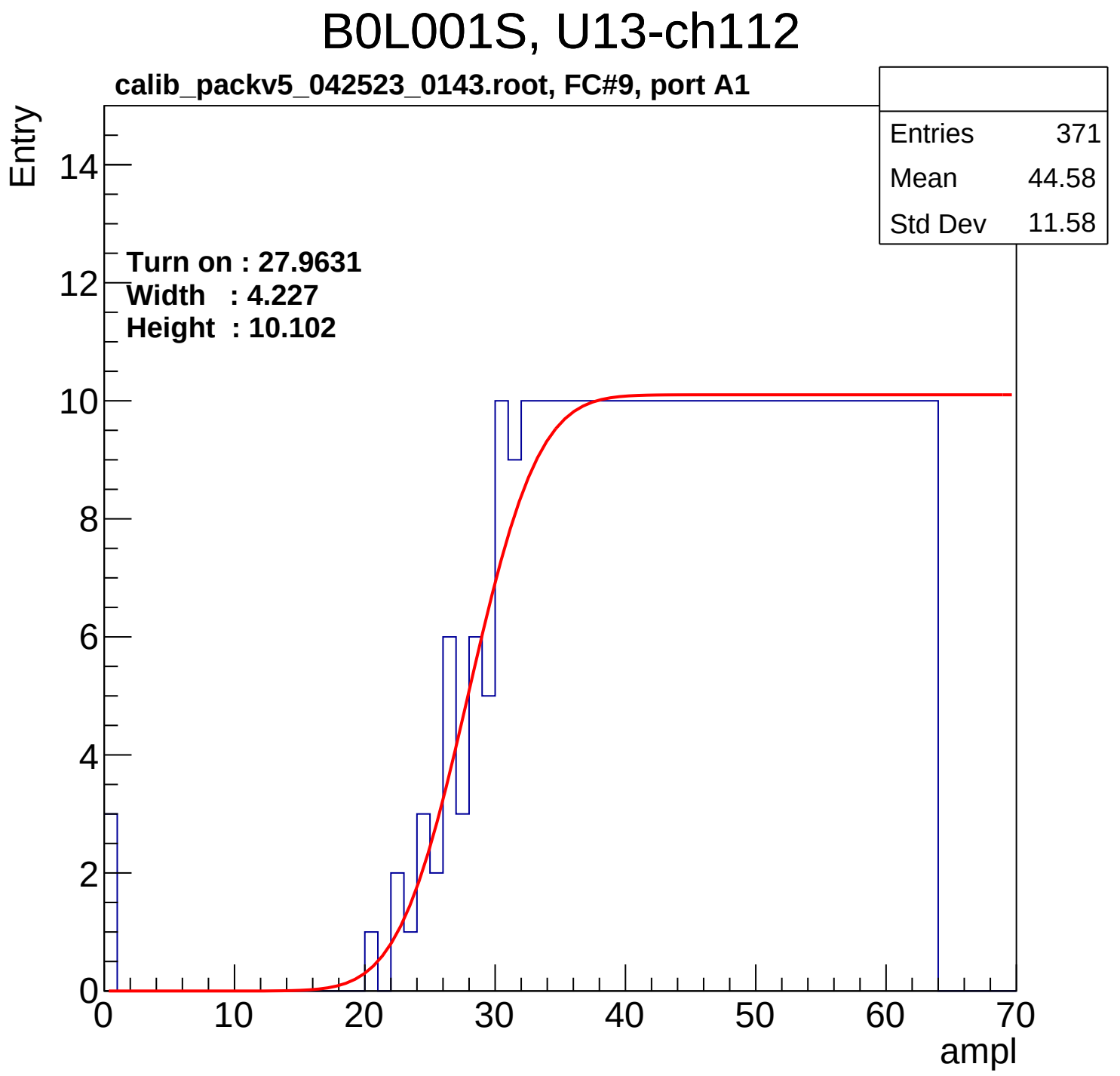
B0L001S, U13-ch112
calib_packv5_042523_0143.root, FC#9, port A1
Entries 371
Mean 44.58
Std Dev 11.58
Turn on : 27.9631
Width : 4.227
Height : 10.102
Entry
ampl
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6
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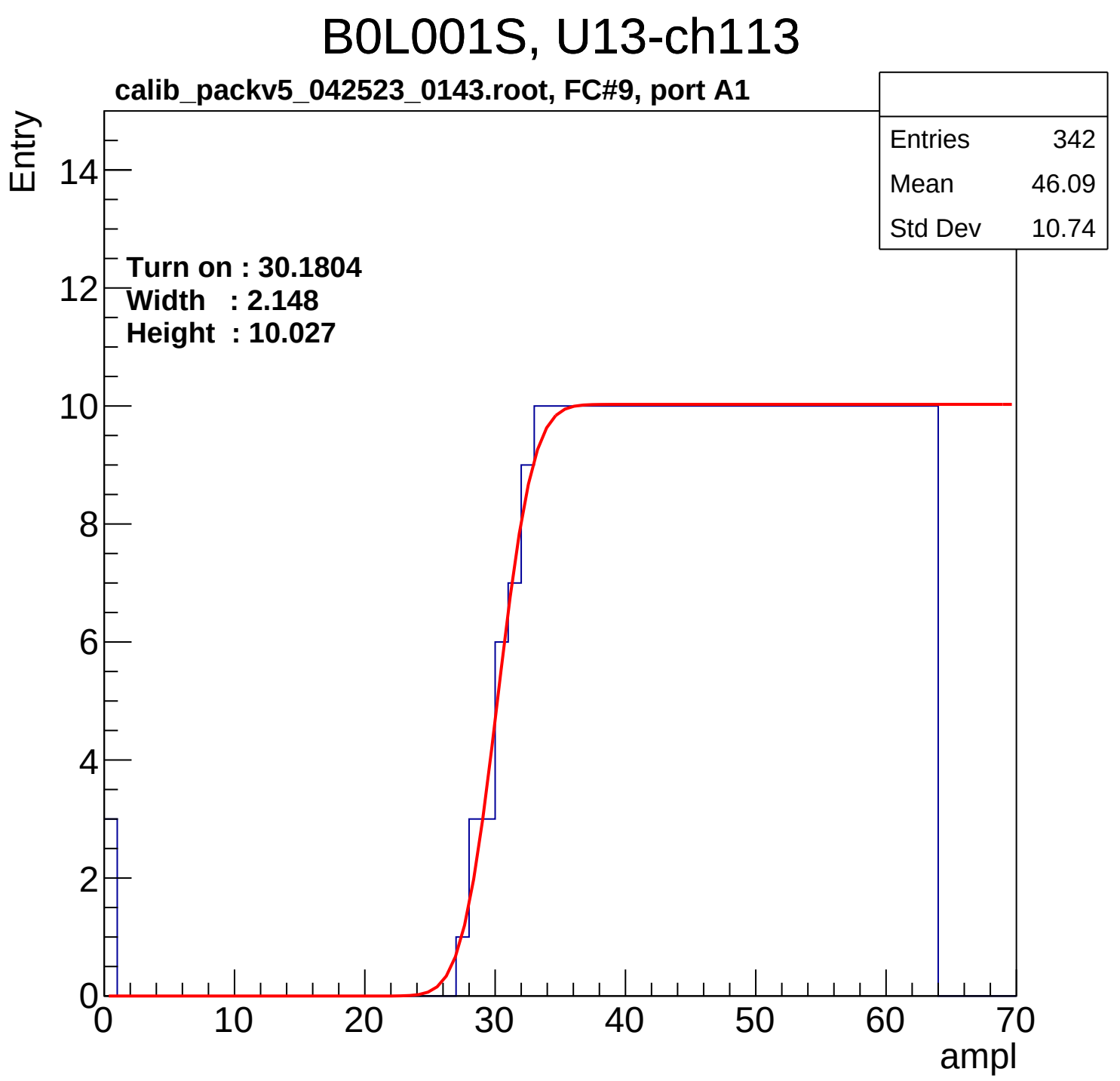
B0L001S, U13-ch113
calib_packv5_042523_0143.root, FC#9, port A1
Entries 342
Mean 46.09
Std Dev 10.74
Turn on : 30.1804
Width : 2.148
Height : 10.027
Entry
ampl
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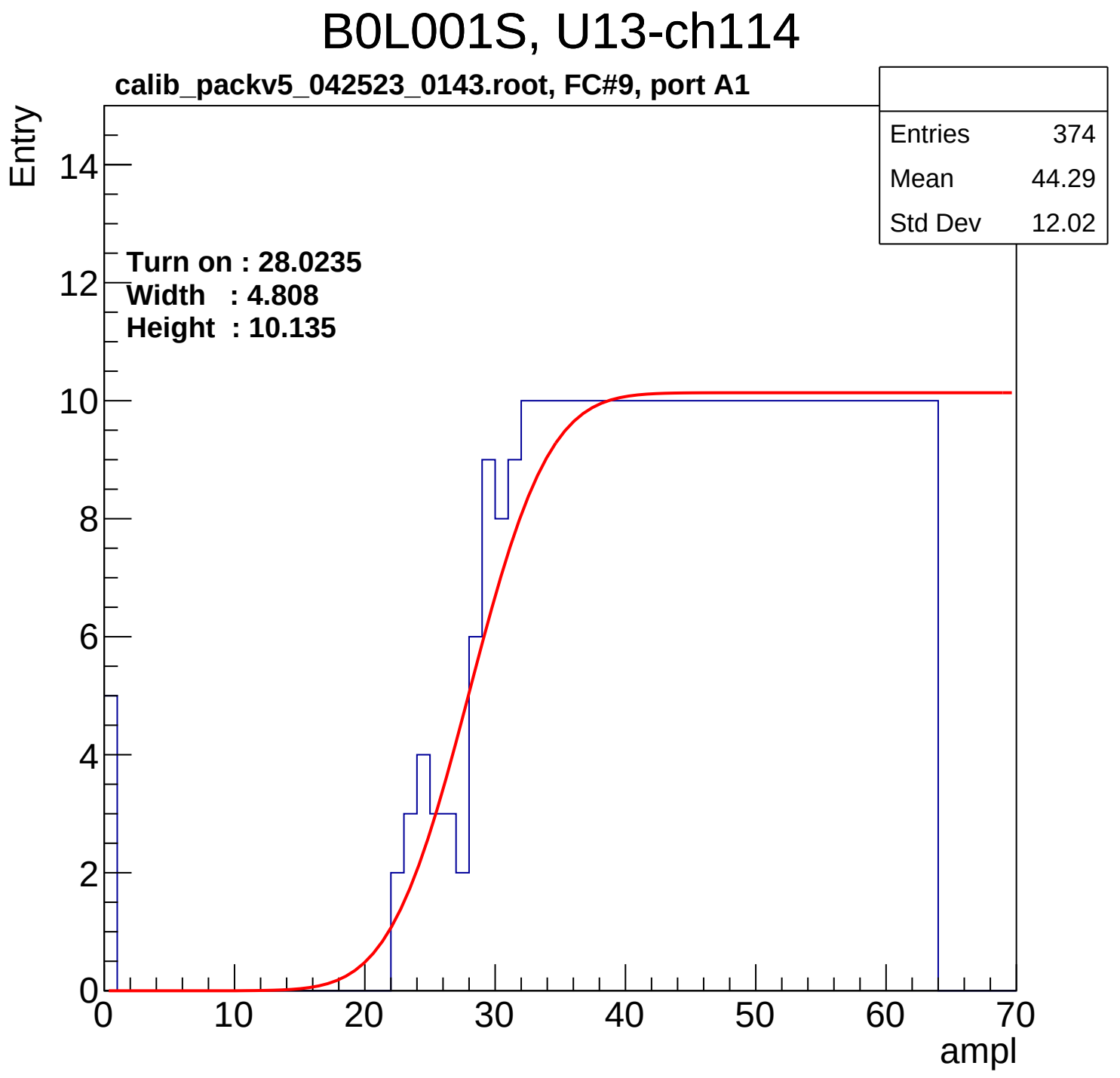
B0L001S, U13-ch114
calib_packv5_042523_0143.root, FC#9, port A1
Entries 374
Mean 44.29
Std Dev 12.02
Turn on : 28.0235
Width : 4.808
Height : 10.135
Entry
ampl
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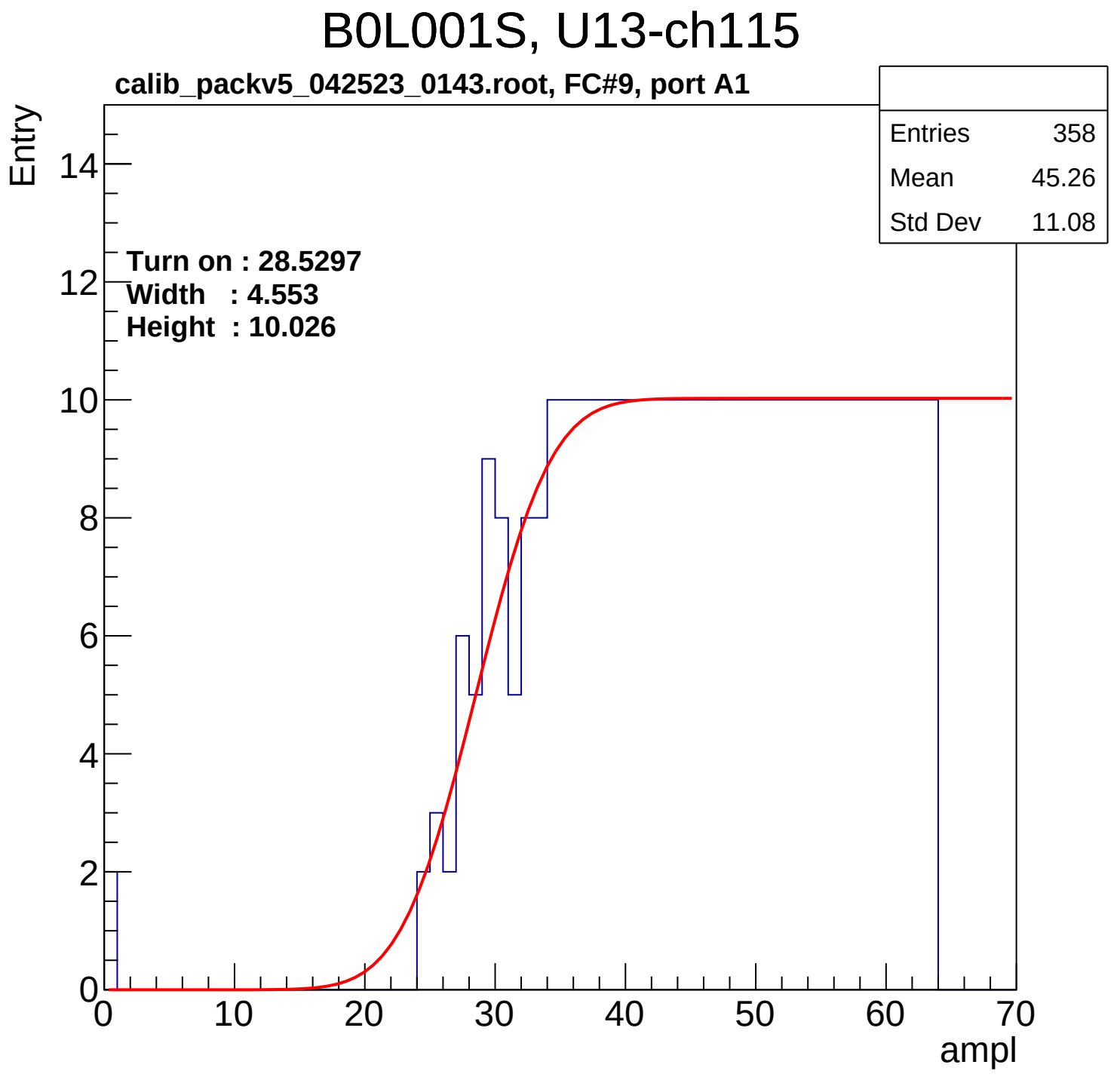
B0L001S, U13-ch115
calib_packv5_042523_0143.root, FC#9, port A1
Entries 358
Mean 45.26
Std Dev 11.08
Turn on : 28.5297
Width : 4.553
Height : 10.026
Entry
ampl
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4
6
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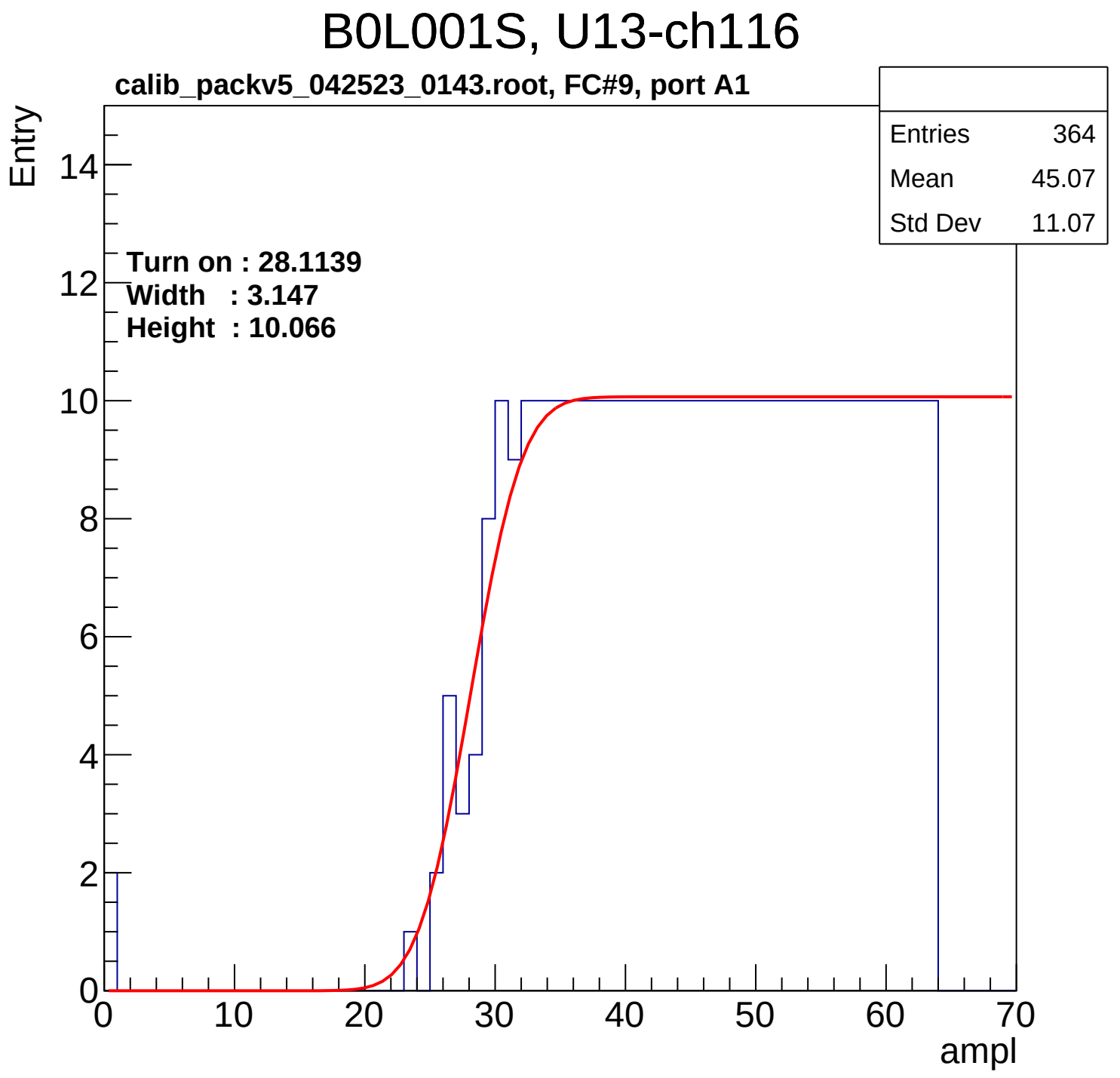
B0L001S, U13-ch116
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 45.07
Std Dev 11.07
Turn on : 28.1139
Width : 3.147
Height : 10.066
Entry
ampl
0
2
4
6
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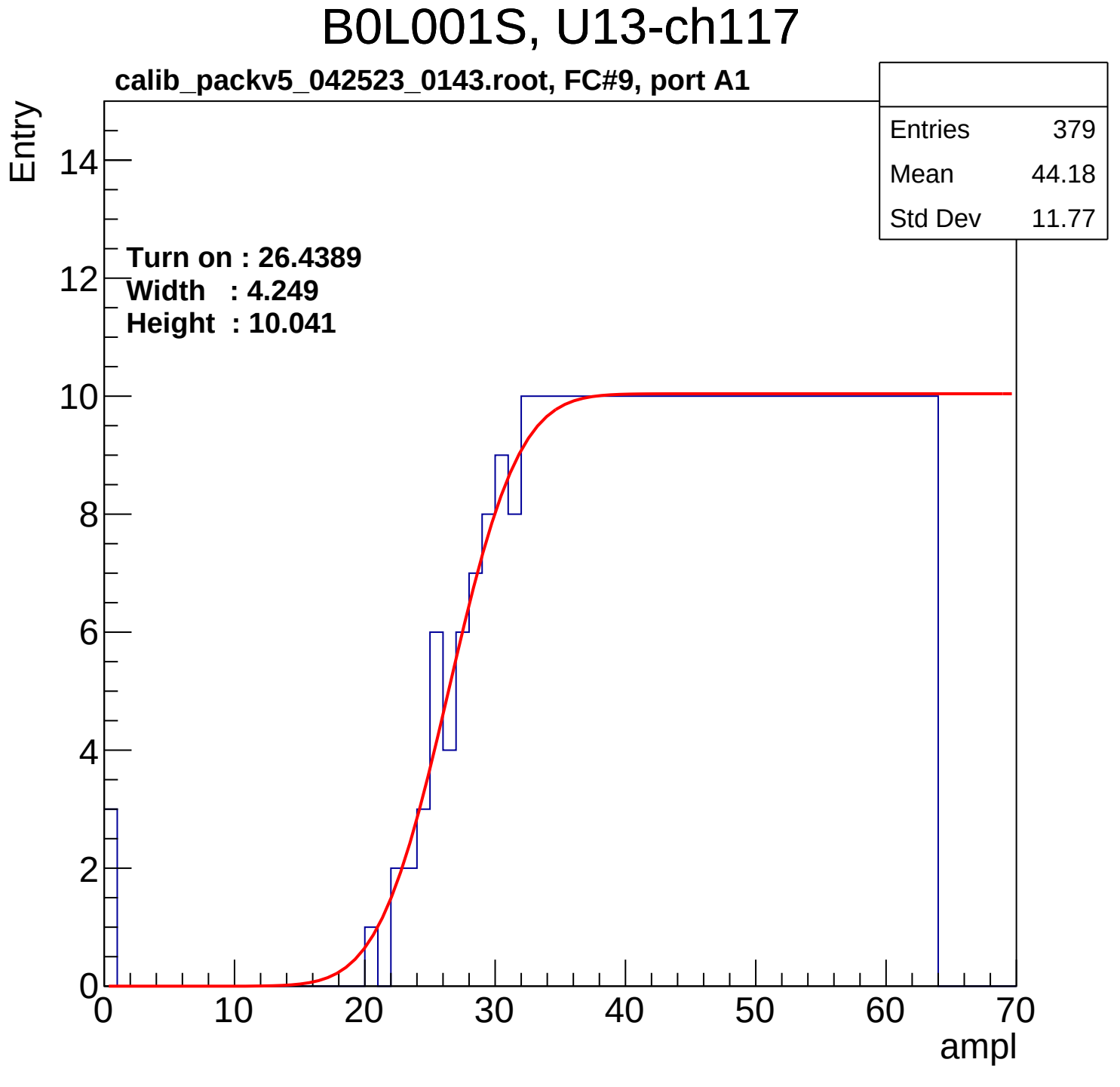
B0L001S, U13-ch117
calib_packv5_042523_0143.root, FC#9, port A1
Entries 379
Mean 44.18
Std Dev 11.77
Turn on : 26.4389
Width : 4.249
Height : 10.041
Entry
ampl
0
2
4
6
8
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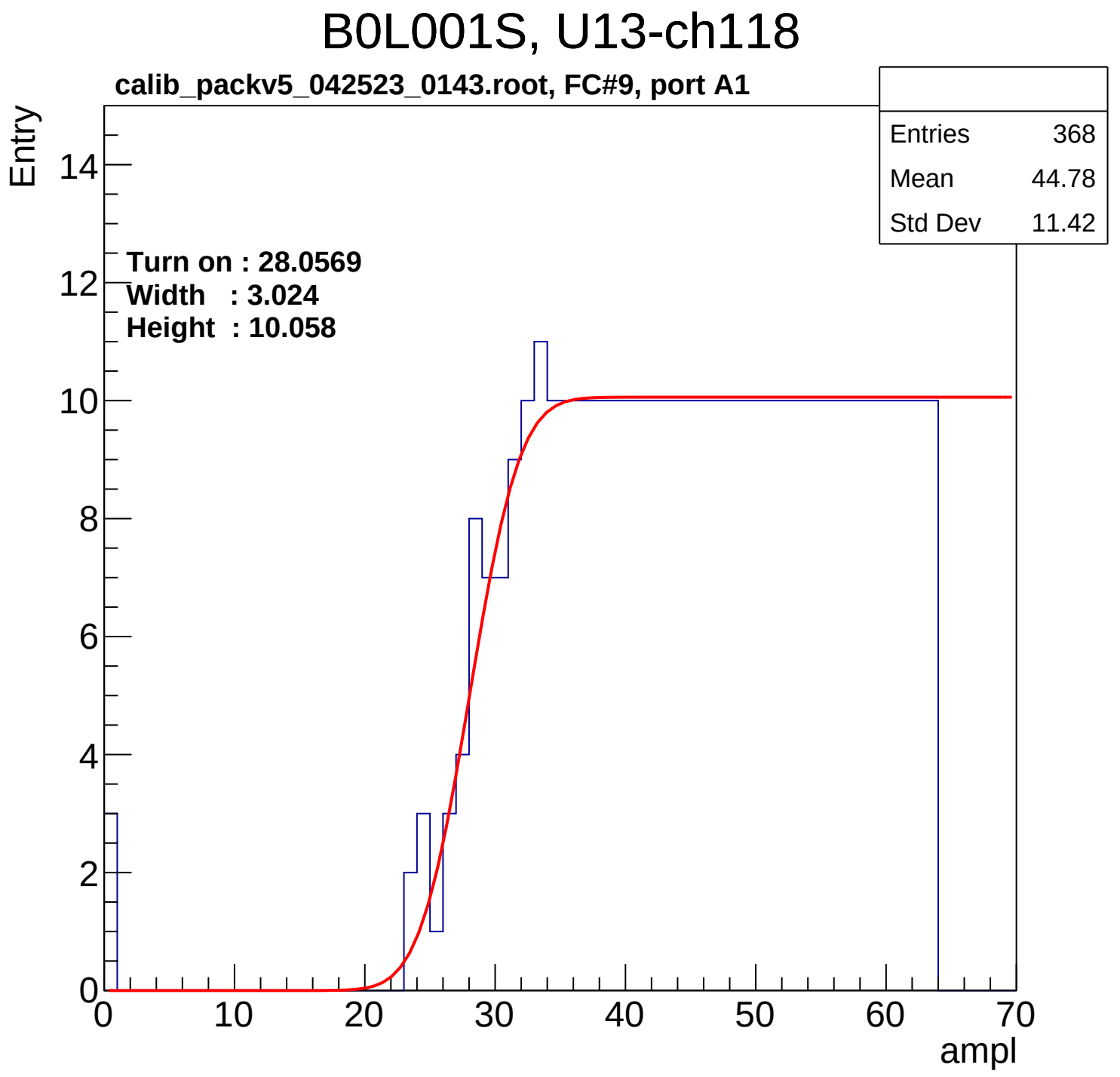
B0L001S, U13-ch118
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.78
Std Dev 11.42
Turn on : 28.0569
Width : 3.024
Height : 10.058
Entry
ampl
0
2
4
6
8
10
12
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0
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40
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60
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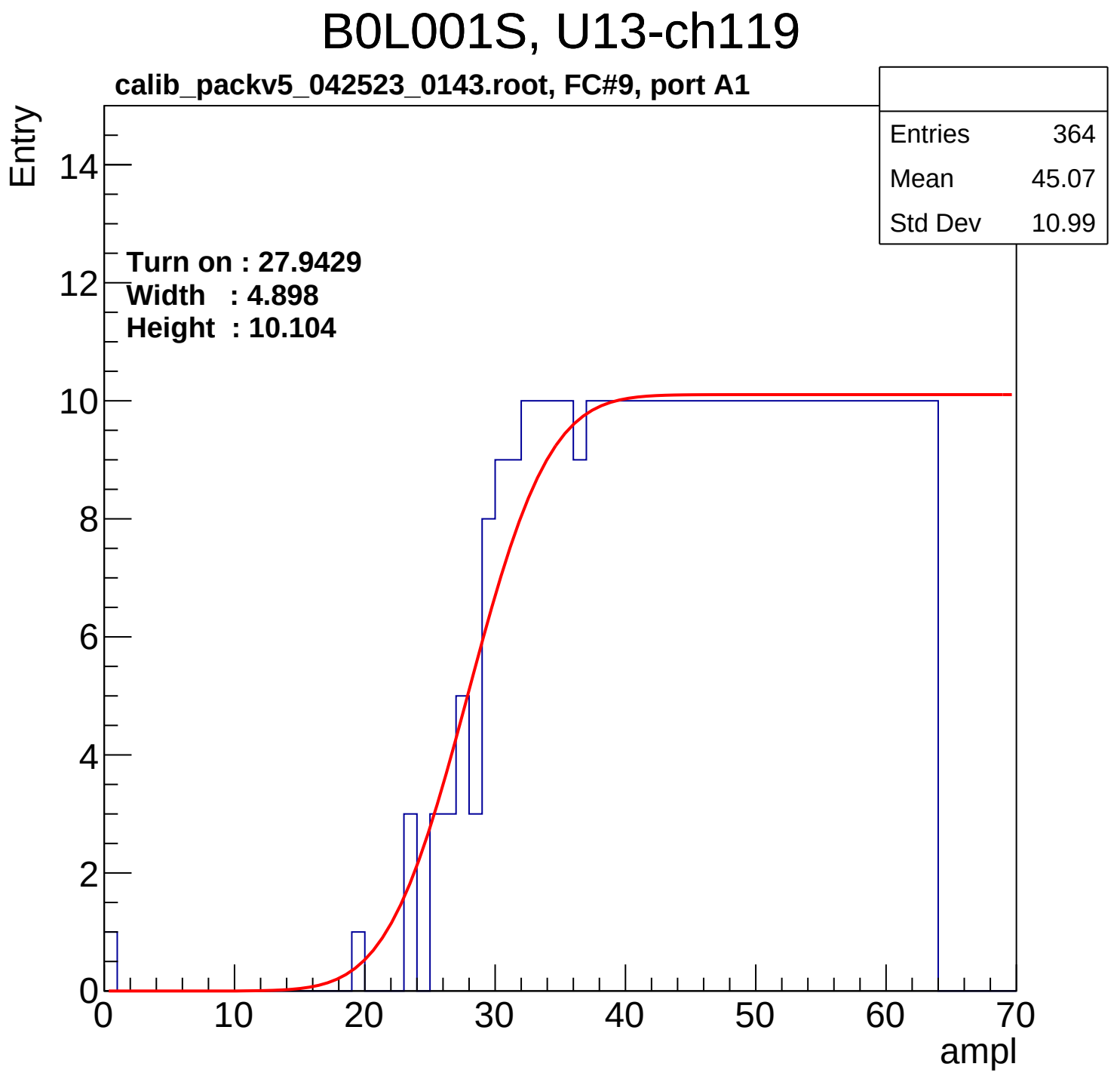
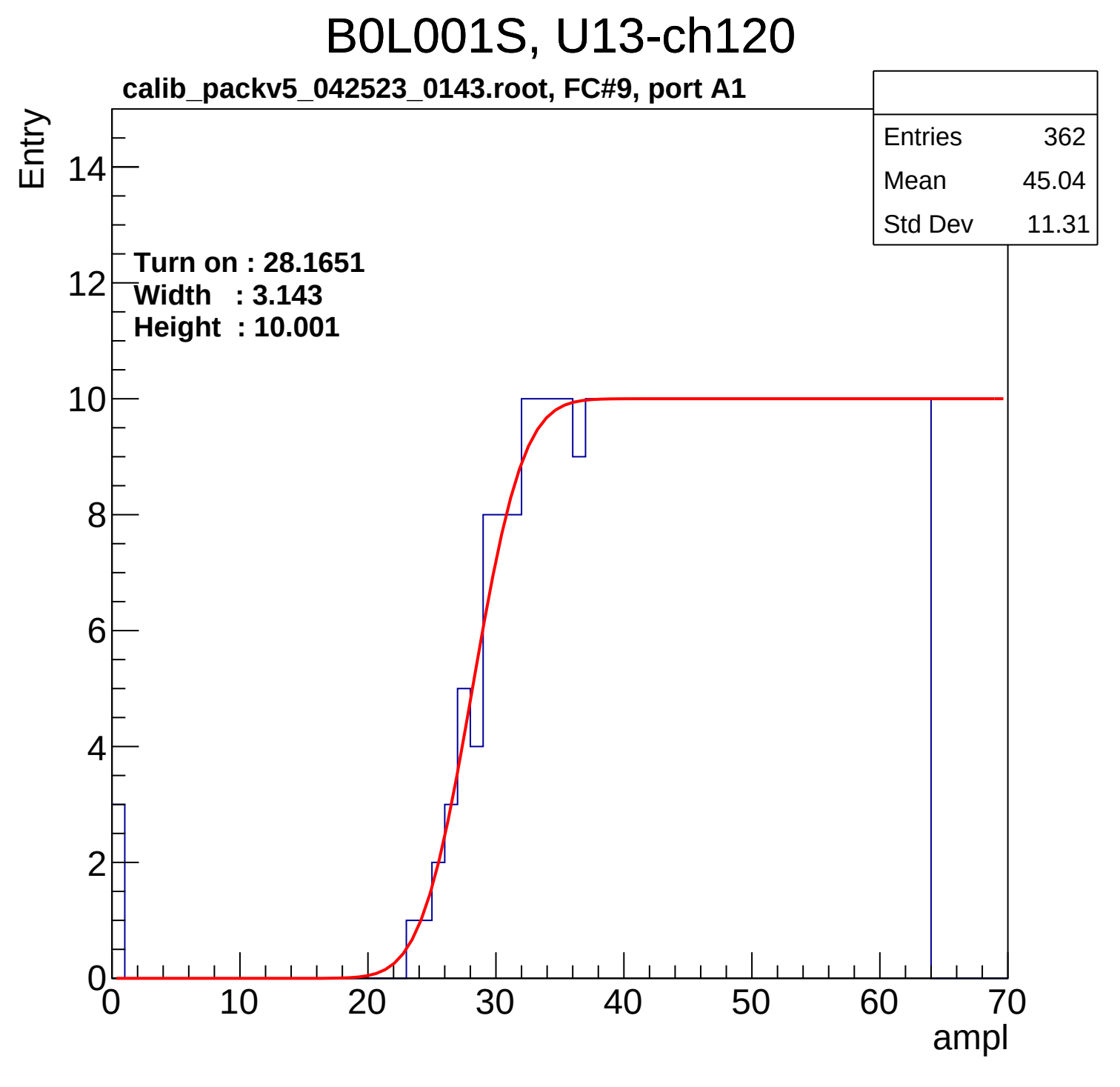

B0L001S, U13-ch119
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 45.07
Std Dev 10.99
Turn on : 27.9429
Width : 4.898
Height : 10.104
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U13-ch120
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 45.04
Std Dev 11.31
Turn on : 28.1651
Width : 3.143
Height : 10.001
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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40
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60
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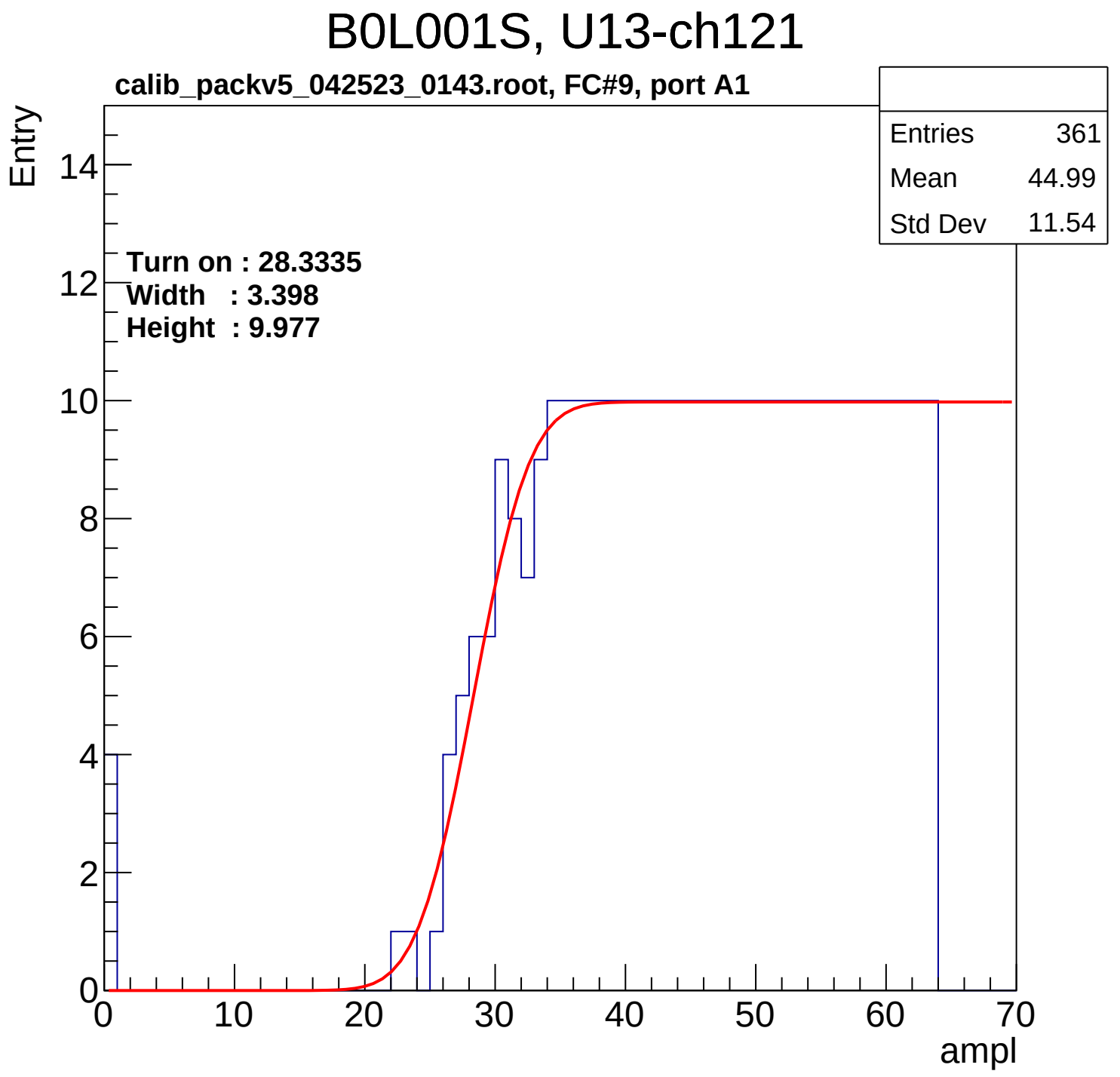
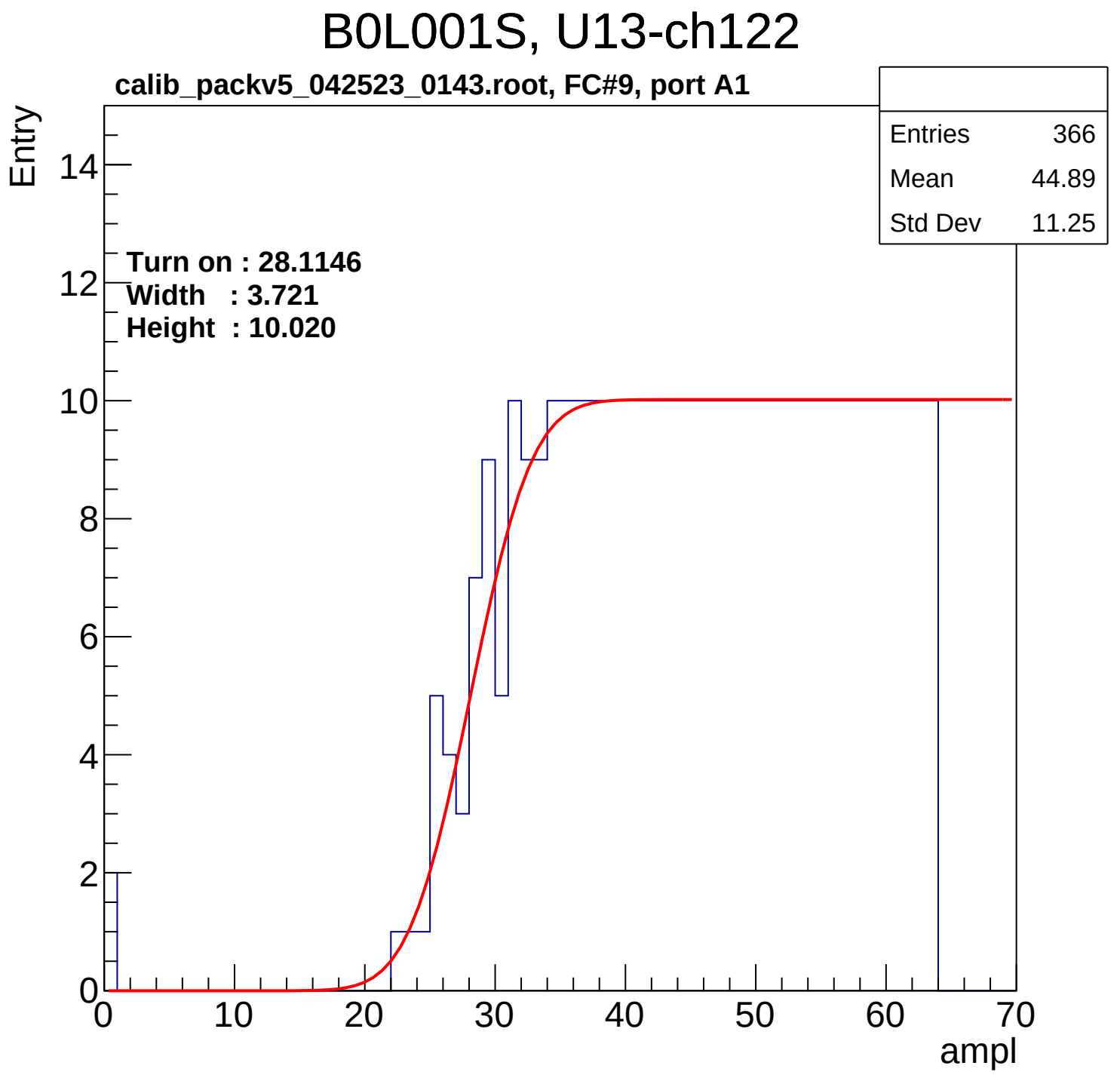

B0L001S, U13-ch121
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 44.99
Std Dev 11.54
Turn on : 28.3335
Width : 3.398
Height : 9.977
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U13-ch122
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.89
Std Dev 11.25
Turn on : 28.1146
Width : 3.721
Height : 10.020
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
30
40
50
60
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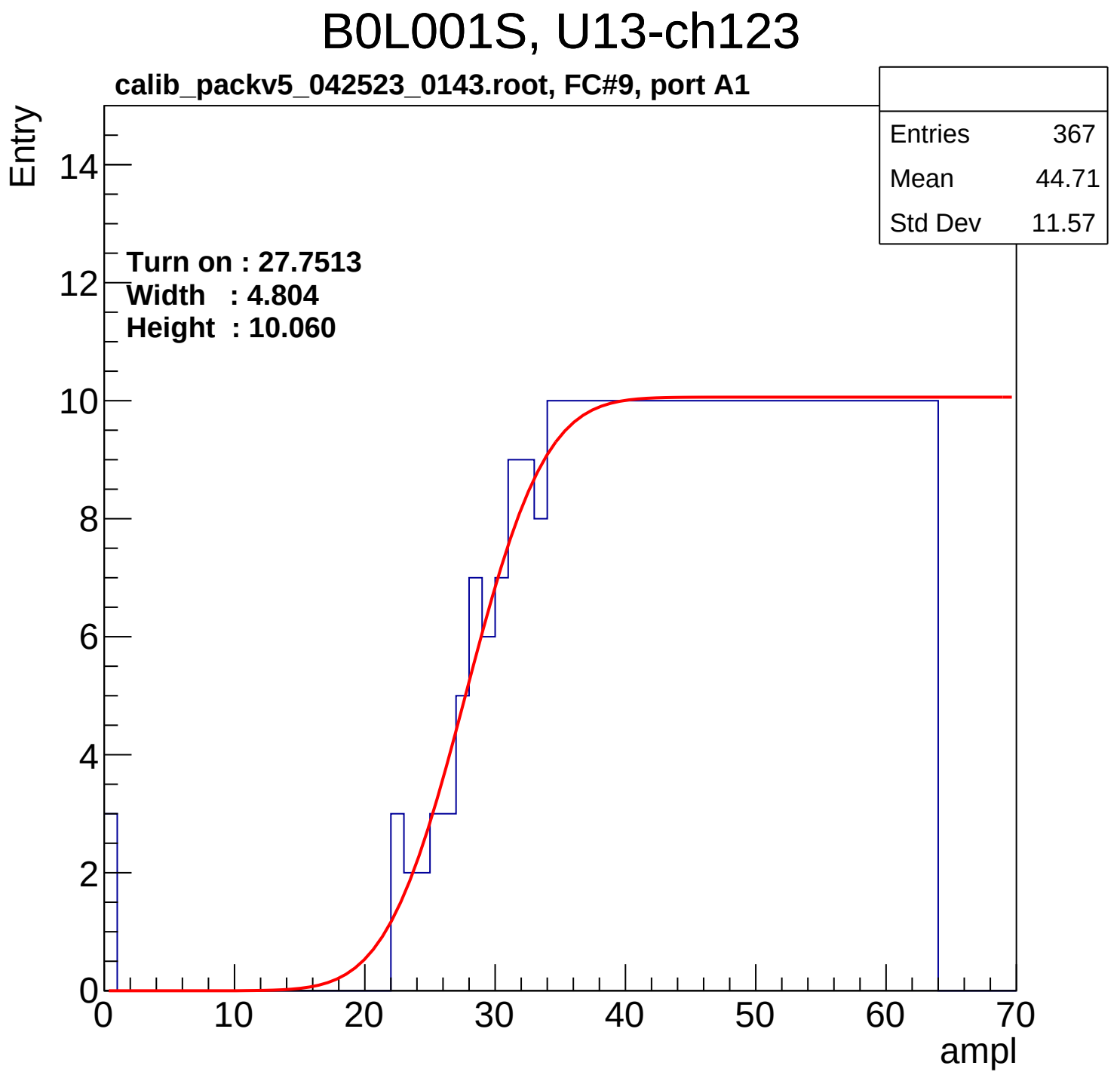
B0L001S, U13-ch123
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.71
Std Dev 11.57
Turn on : 27.7513
Width : 4.804
Height : 10.060
Entry
ampl
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2
4
6
8
10
12
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0
10
20
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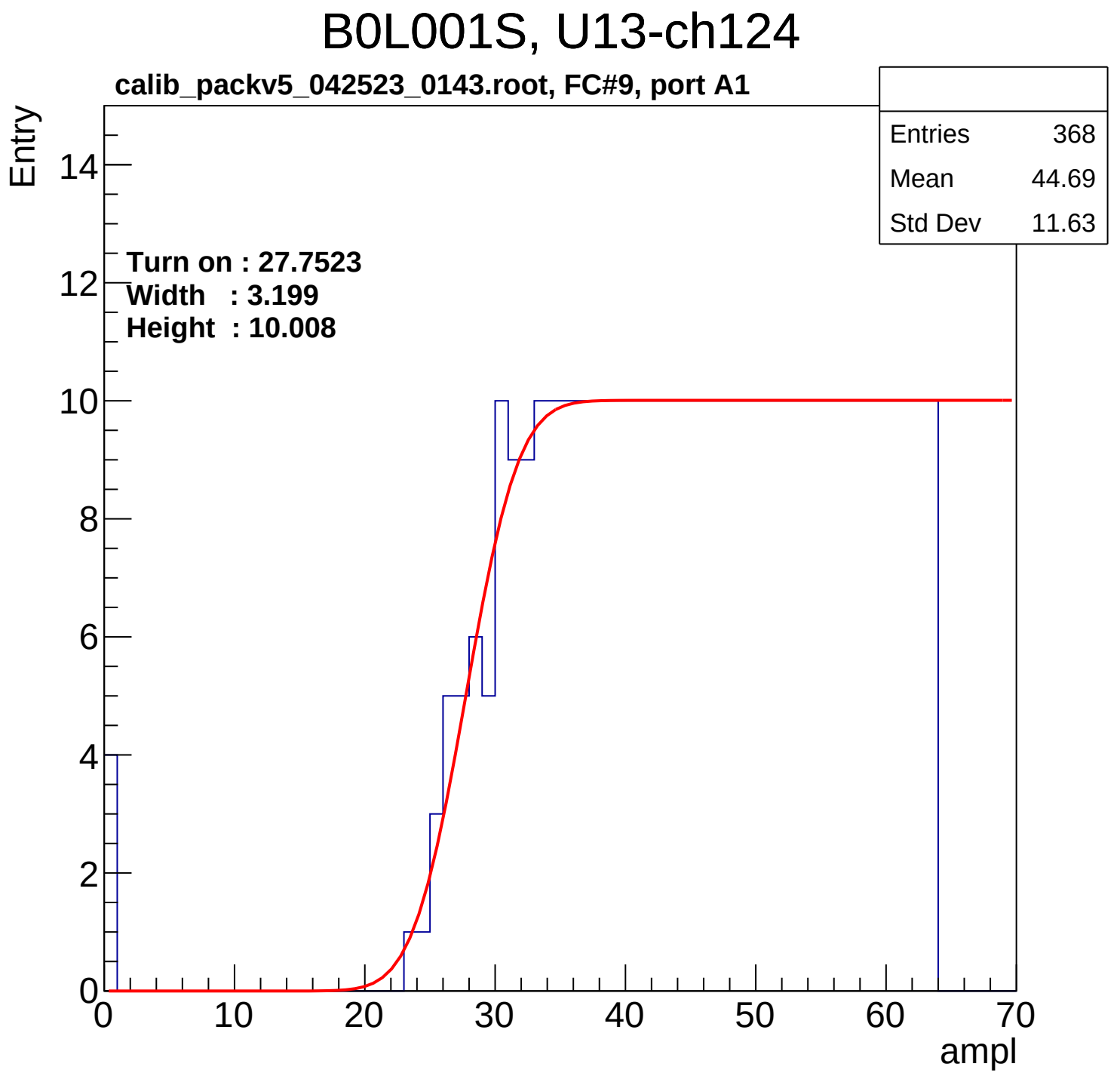
40
50
60
70


B0L001S, U13-ch124
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.69
Std Dev 11.63
Turn on : 27.7523
Width : 3.199
Height : 10.008
Entry
ampl
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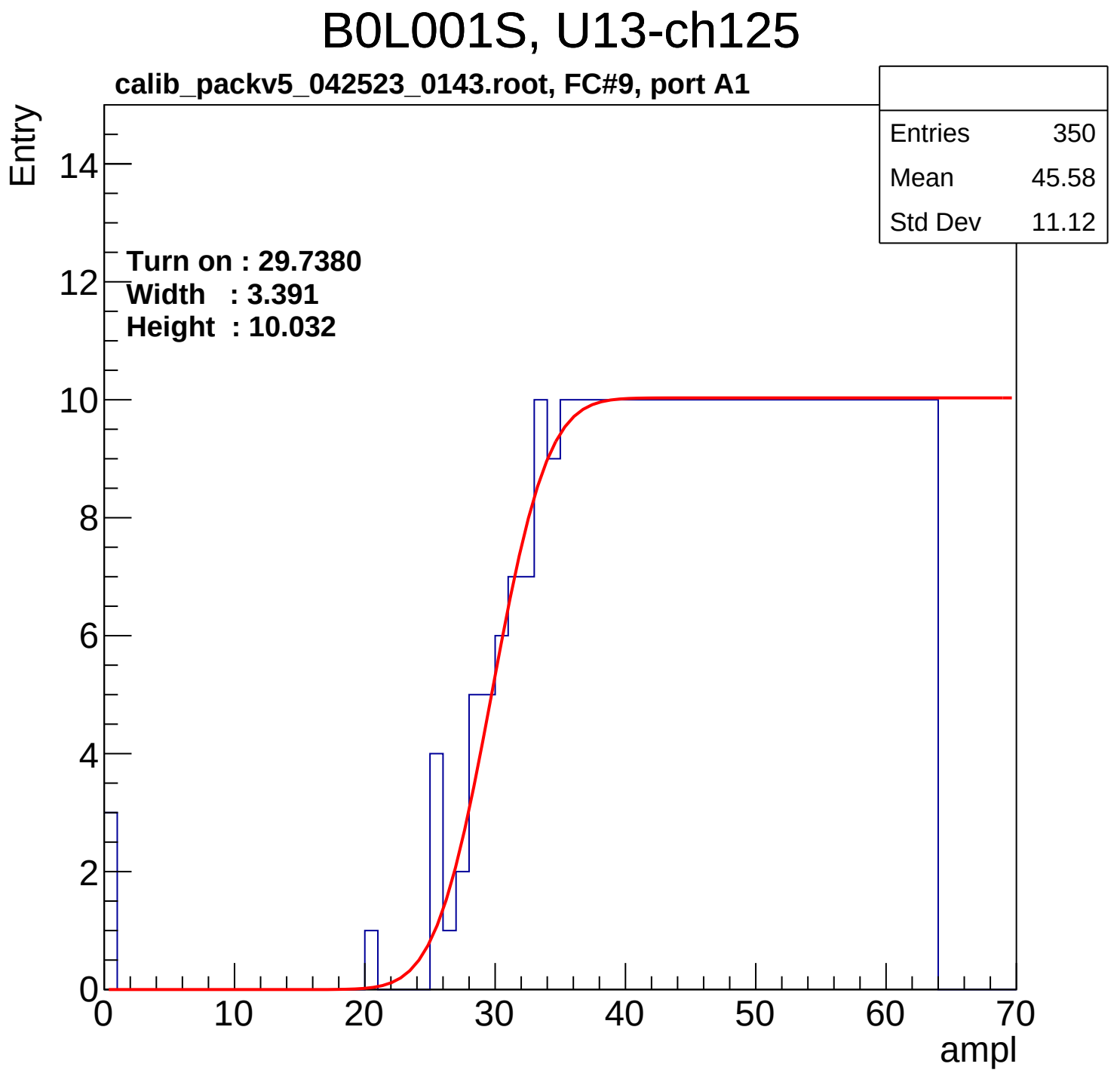
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U13-ch125
calib_packv5_042523_0143.root, FC#9, port A1
Entries 350
Mean 45.58
Std Dev 11.12
Turn on : 29.7380
Width : 3.391
Height : 10.032
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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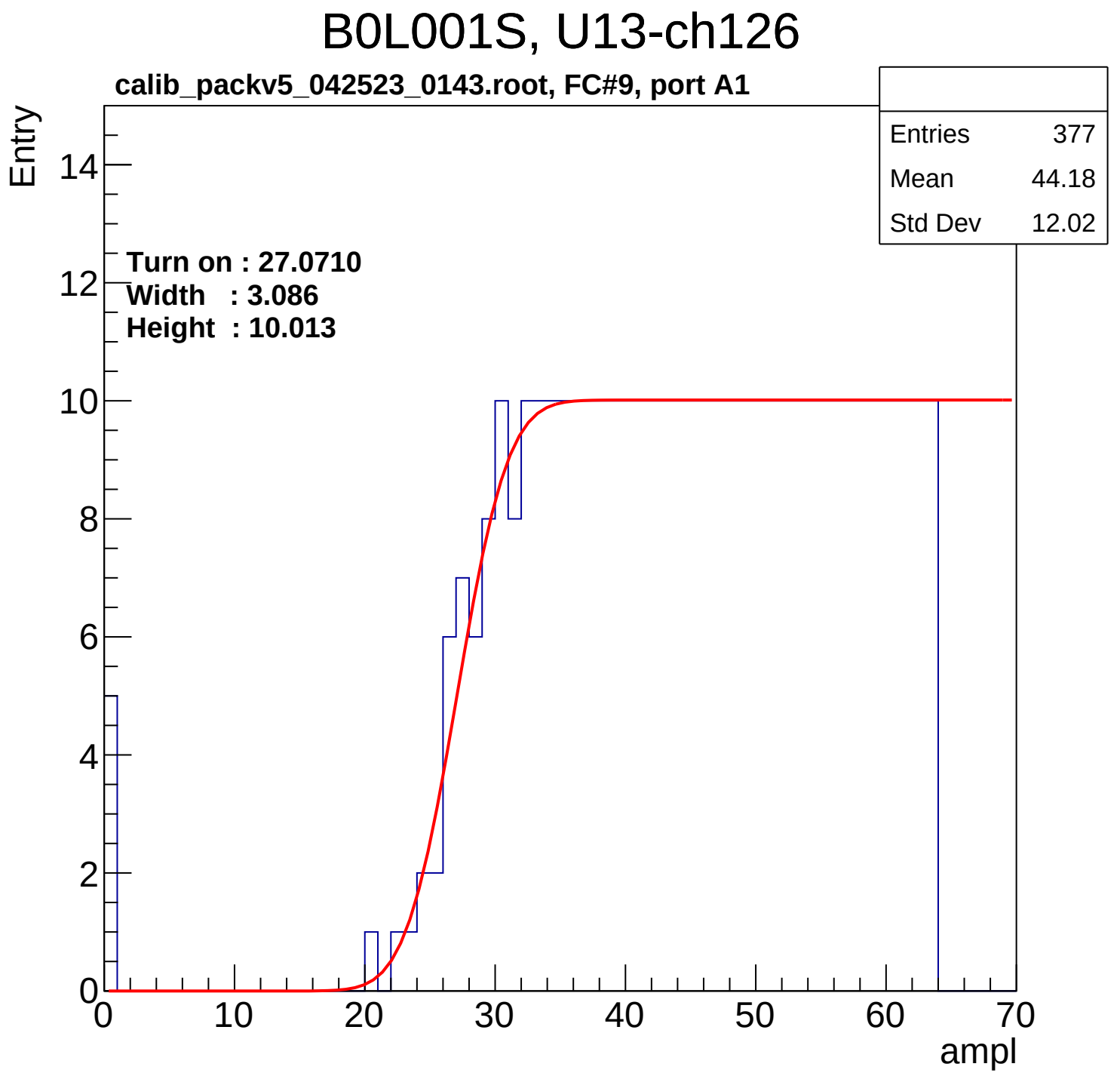
40
50
60
70


B0L001S, U13-ch126
calib_packv5_042523_0143.root, FC#9, port A1
Entries 377
Mean 44.18
Std Dev 12.02
Turn on : 27.0710
Width : 3.086
Height : 10.013
Entry
ampl
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6
8
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60
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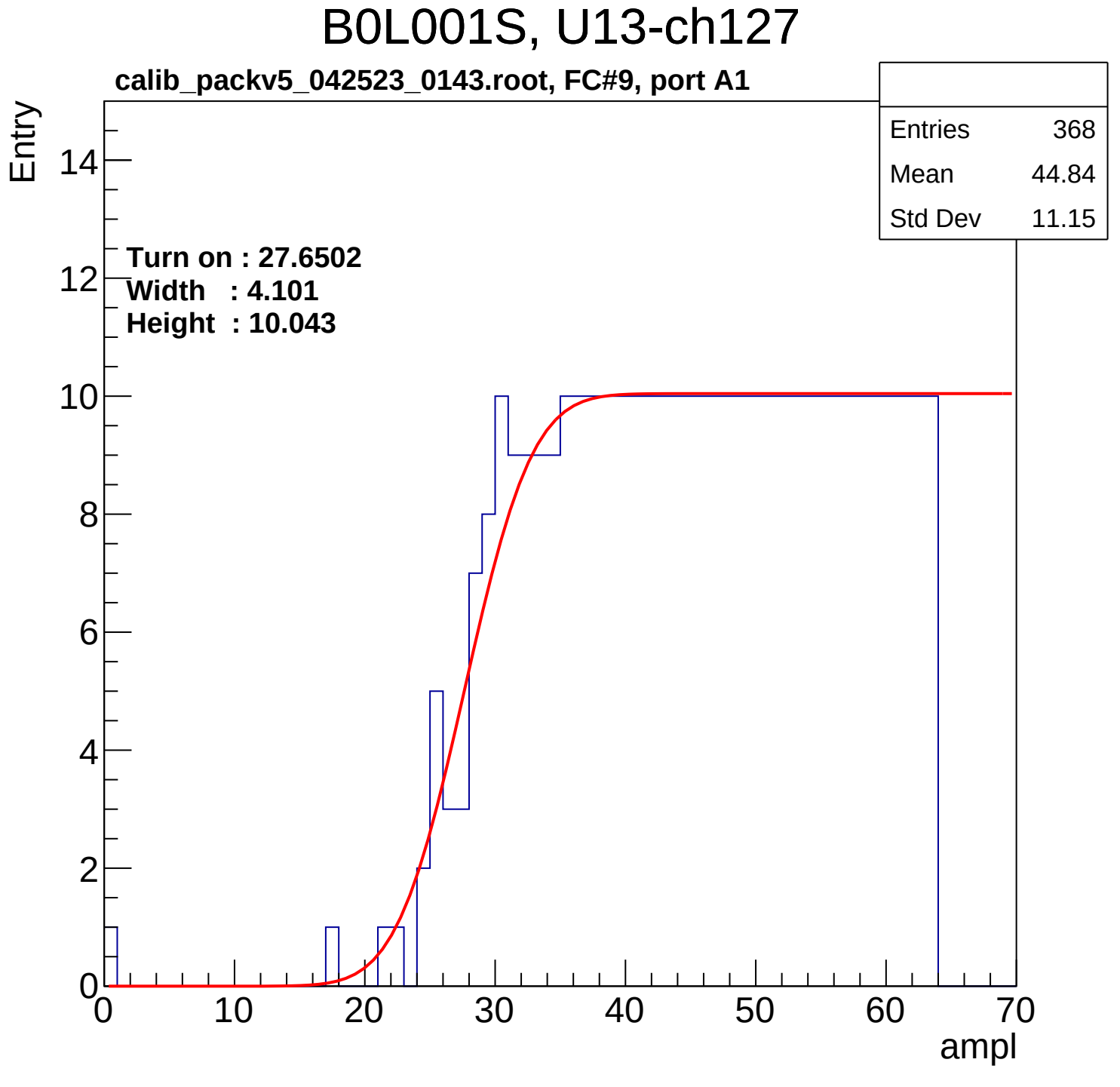
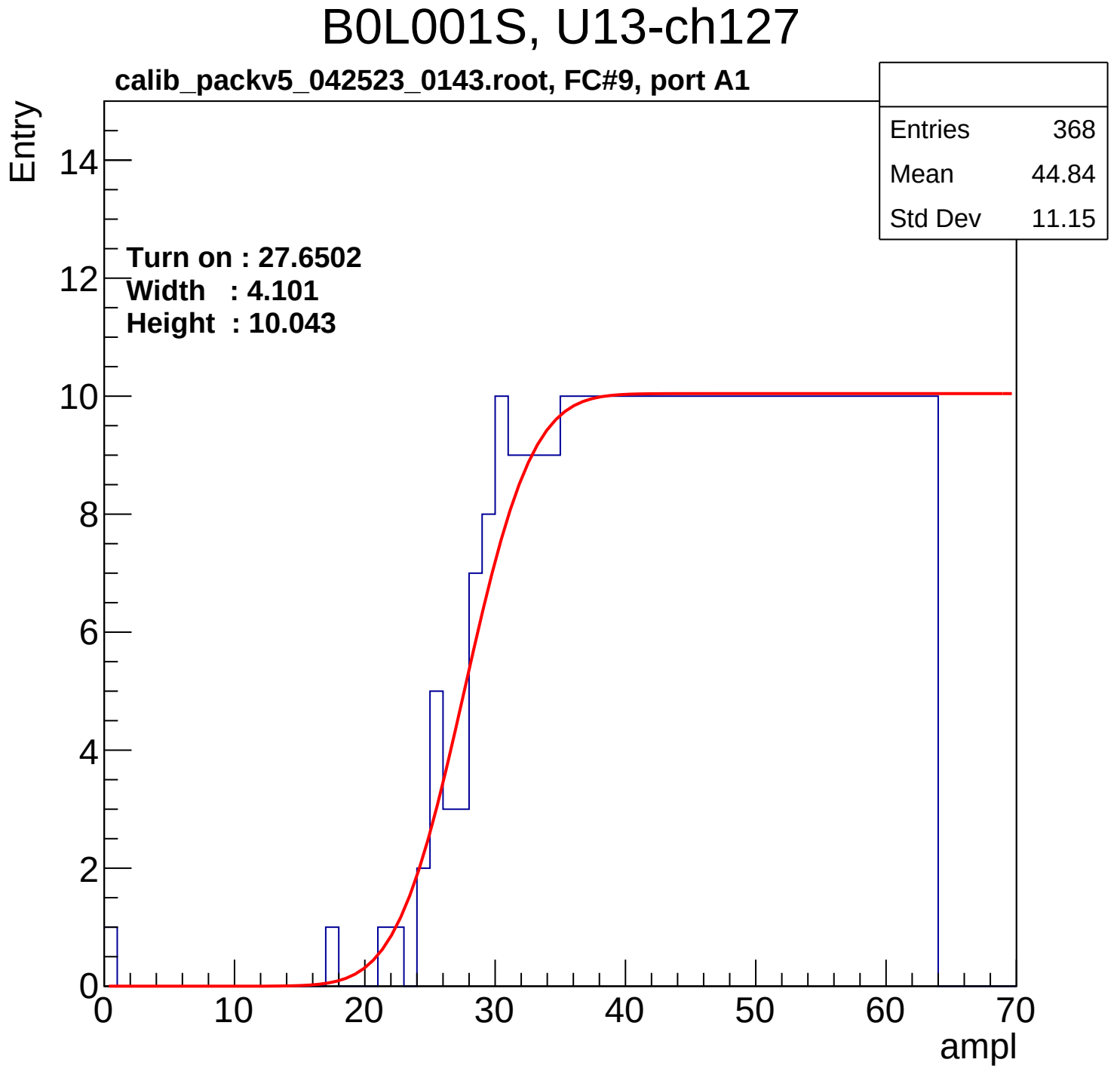

B0L001S, U13-ch127
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.84
Std Dev 11.15
Turn on : 27.6502
Width : 4.101
Height : 10.043
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U13-ch127
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.84
Std Dev 11.15
Turn on : 27.6502
Width : 4.101
Height : 10.043
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70