



# B1L100S, U7-ch0

calib\_packv5\_042523\_0143.root, FC#4, port A2

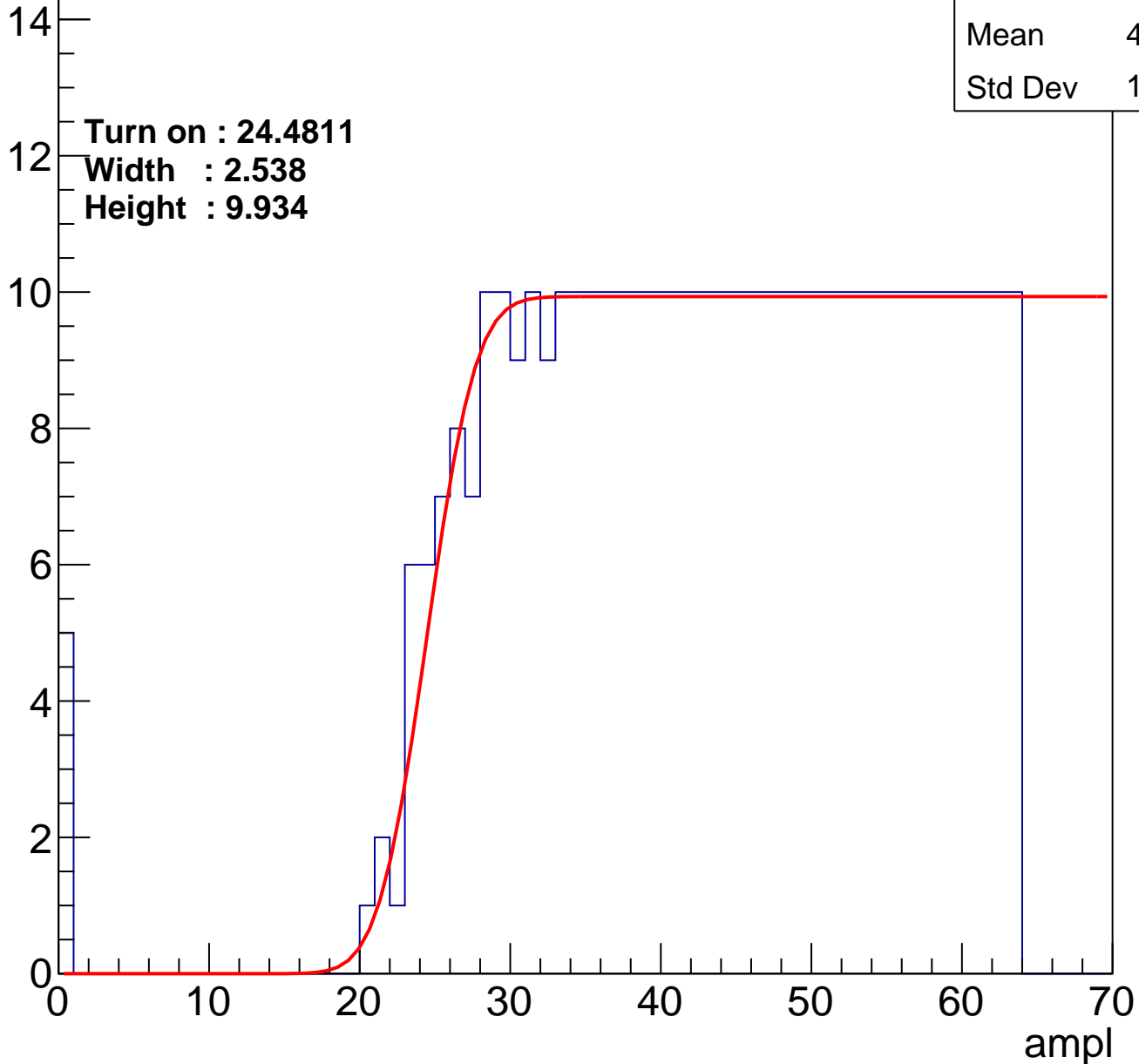
Entries	401
Mean	43.03
Std Dev	12.53

Turn on : 24.4811

Width : 2.538

Height : 9.934

Entry



# B1L100S, U7-ch1

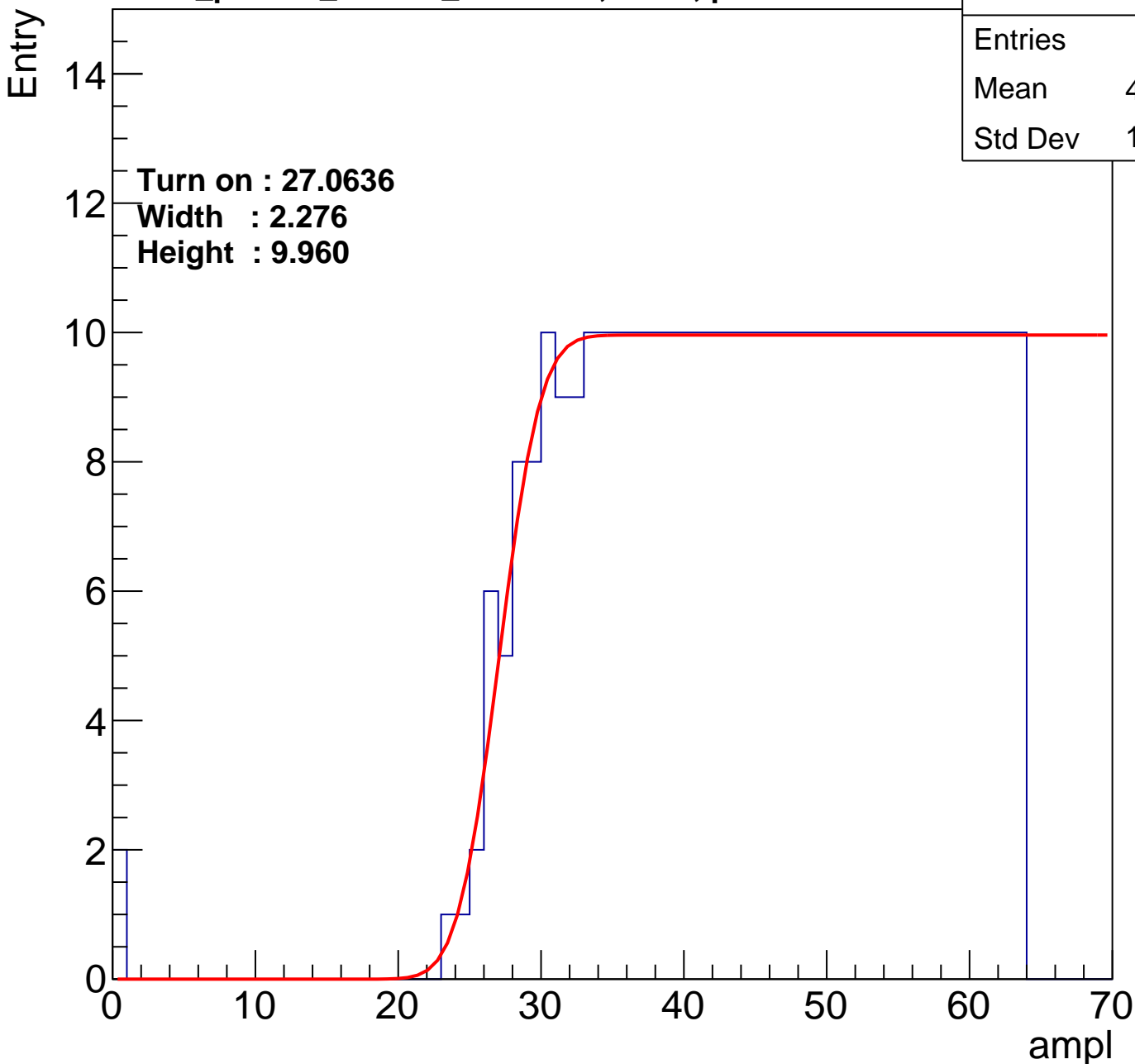
**calib\_packv5\_042523\_0143.root, FC#4, port A2**

Entries	371
Mean	44.72
Std Dev	11.26

Turn on : 27.0636

**Width : 2.276**

**Height : 9.960**



# B1L100S, U7-ch2

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	382
Mean	44.27
Std Dev	11.33

Turn on : 26.3949

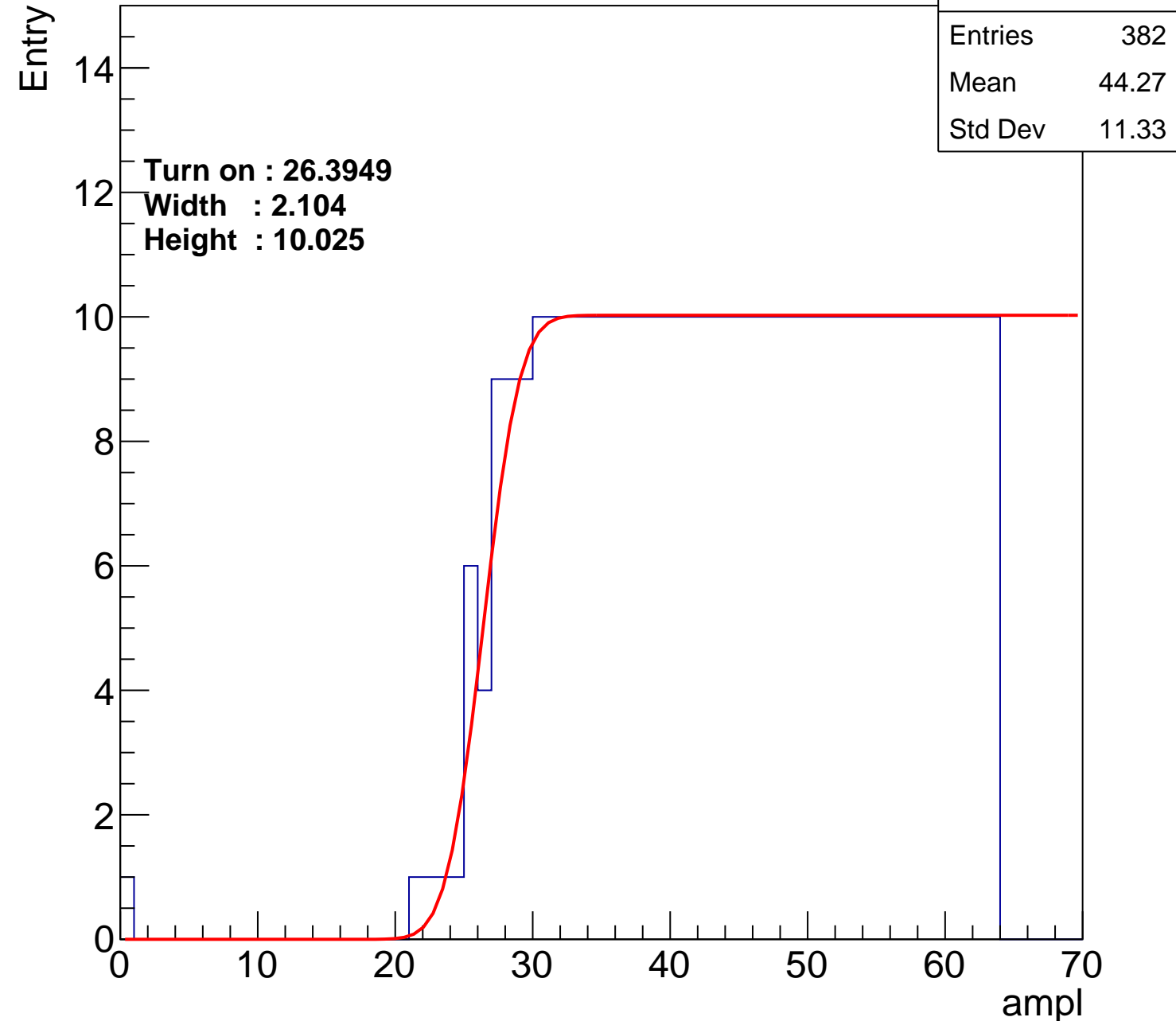
Width : 2.104

Height : 10.025

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	387
Mean	43.87
Std Dev	11.85

Turn on : 26.2020

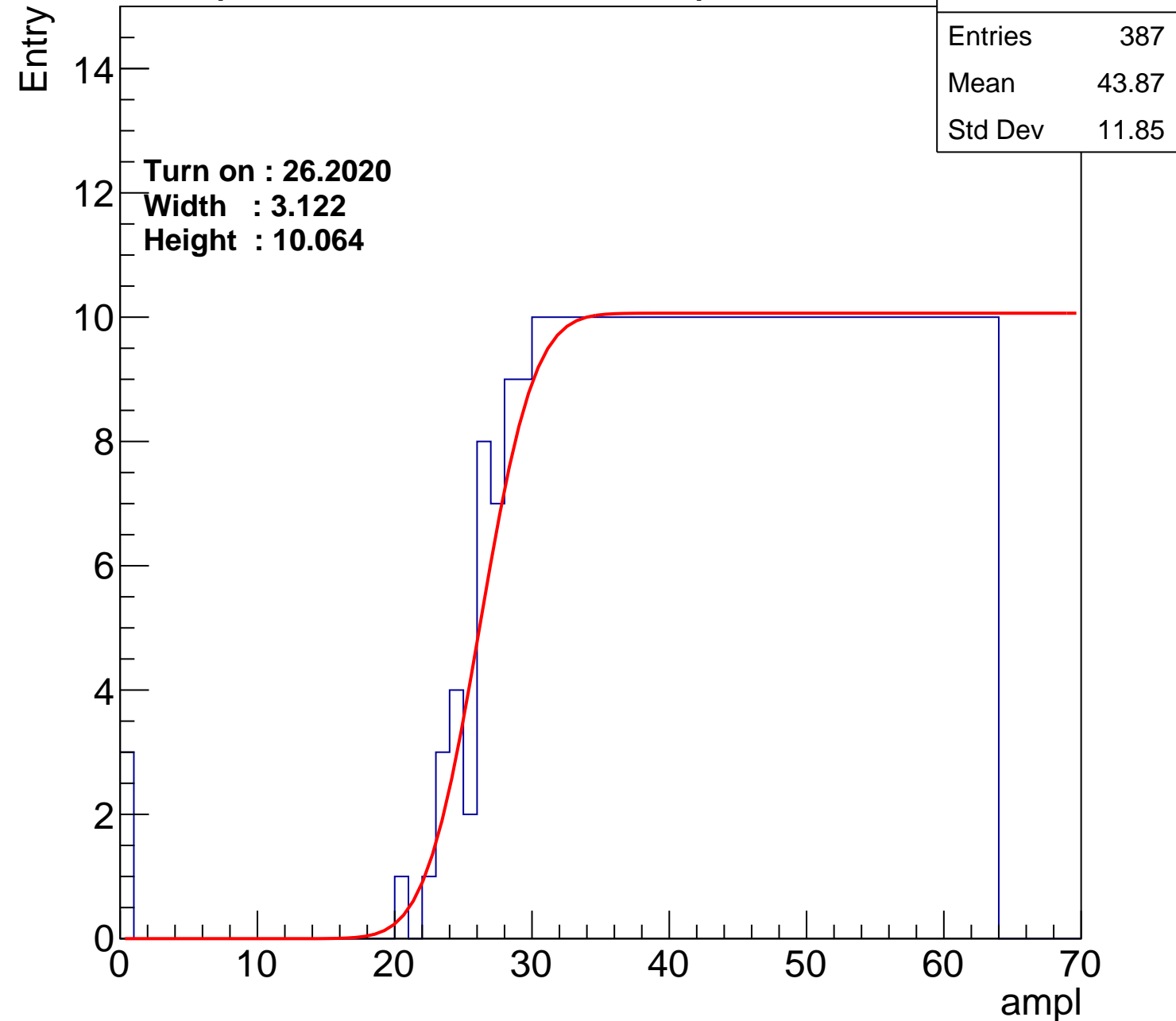
Width : 3.122

Height : 10.064

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch4

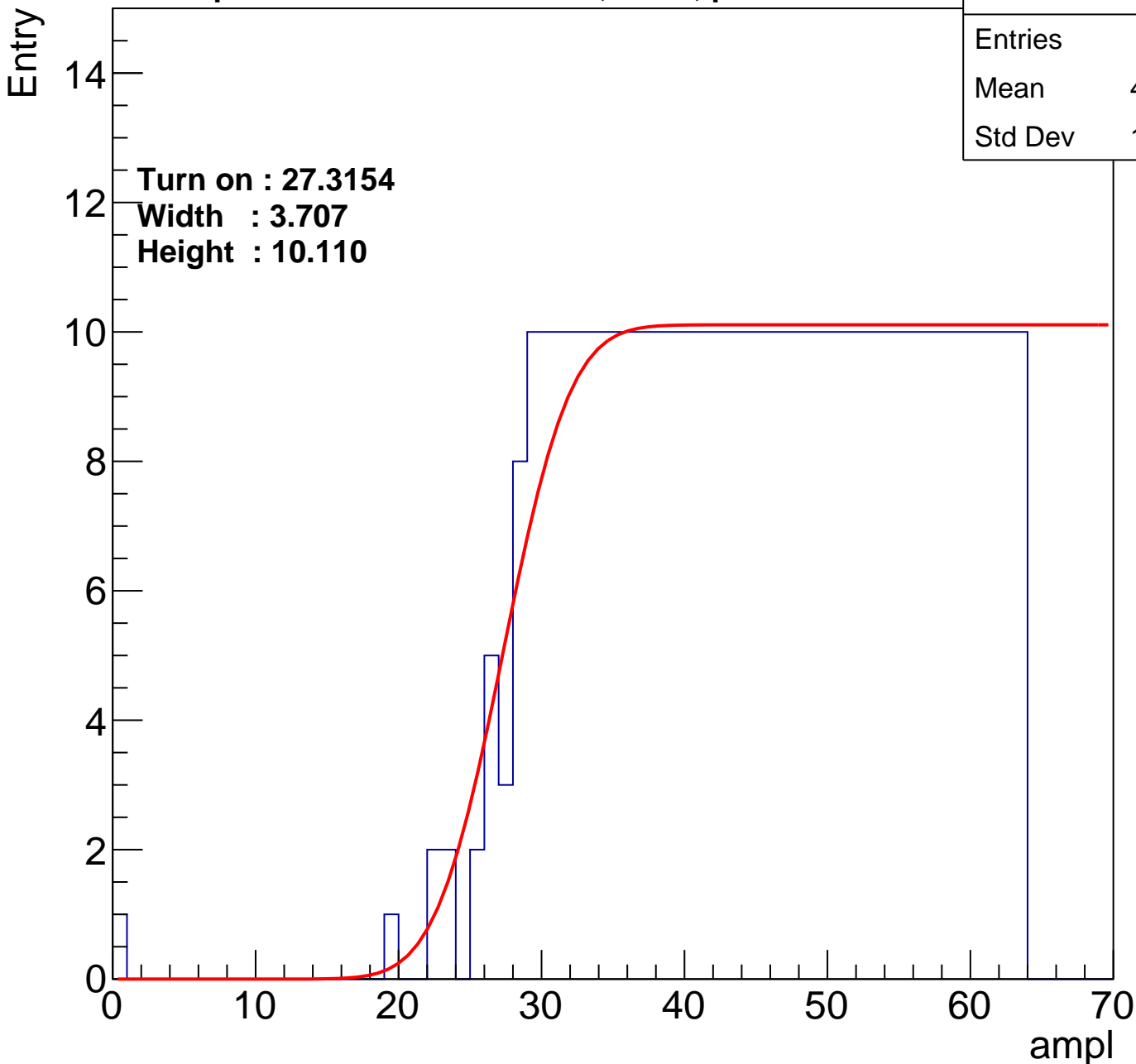
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	374
Mean	44.64
Std Dev	11.16

Turn on : 27.3154

Width : 3.707

Height : 10.110



# B1L100S, U7-ch5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	350
Mean	45.69
Std Dev	10.84

Turn on : 30.3954

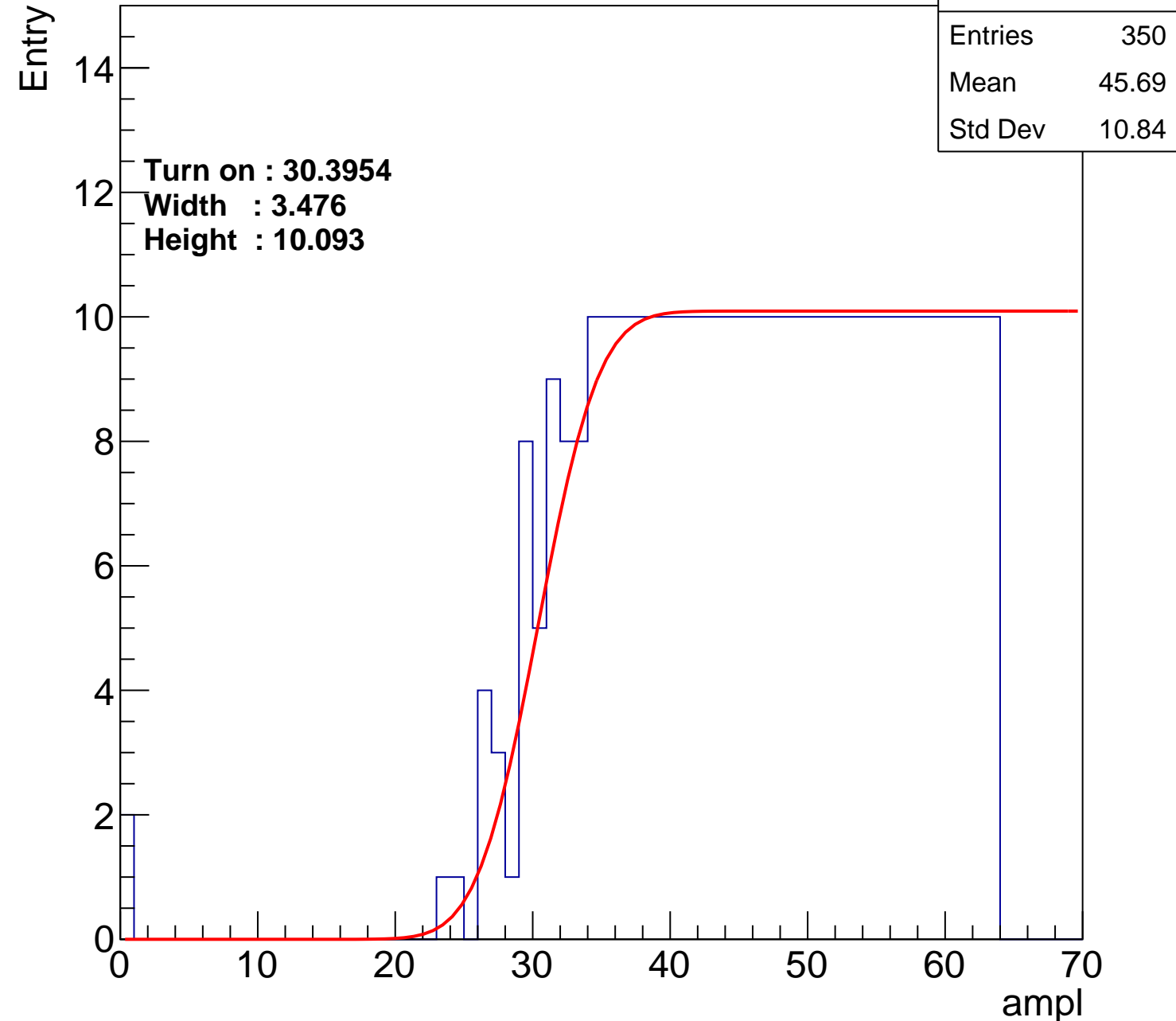
Width : 3.476

Height : 10.093

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch6

**calib\_packv5\_042523\_0143.root, FC#4, port A2**

Entries	394
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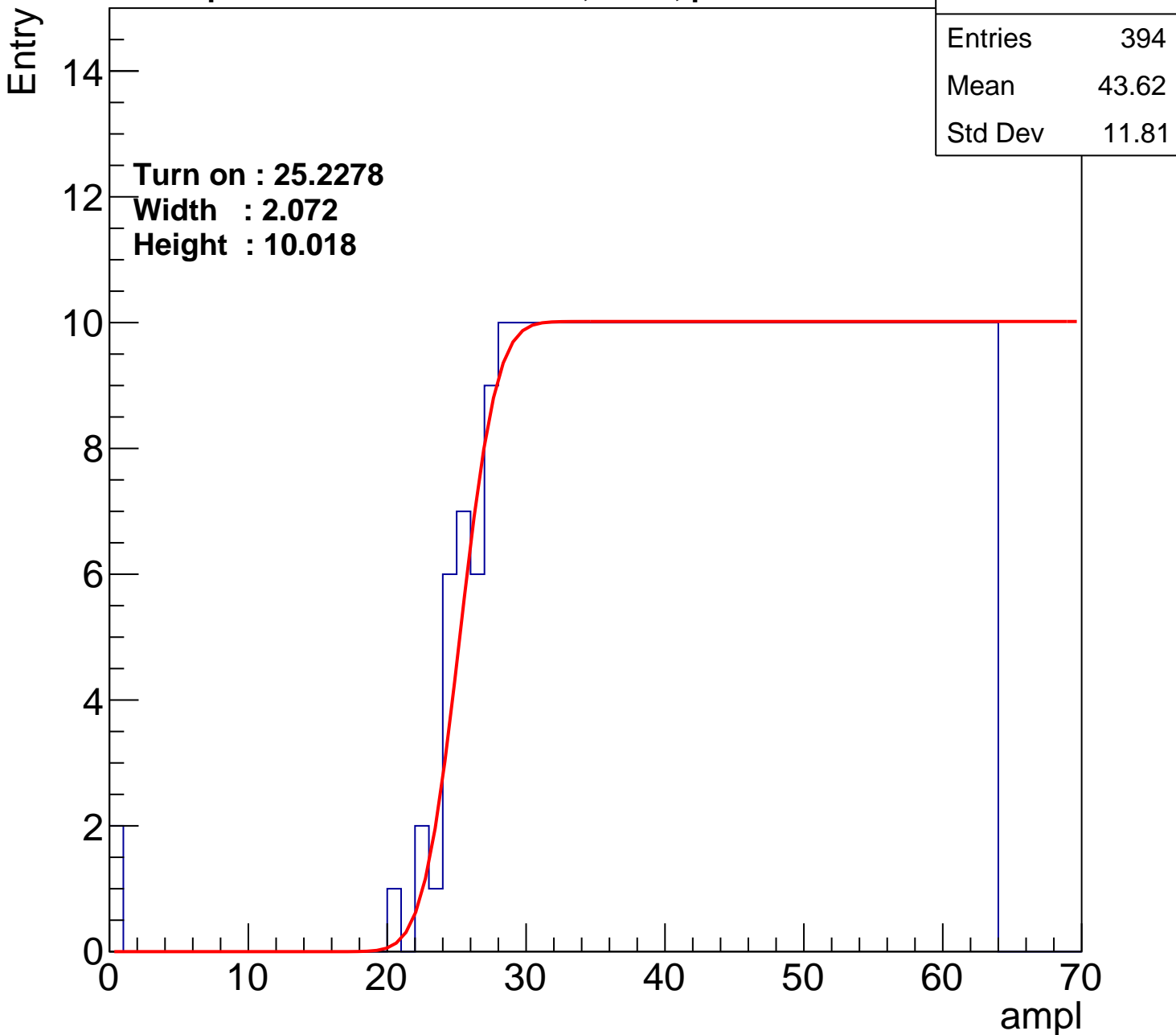
Mean	43.62
------	-------

Std Dev	11.81
---------	-------

**Turn on : 25.2278**

**Width : 2.072**

**Height : 10.018**





# B1L100S, U7-ch7

calib\_packv5\_042523\_0143.root, FC#4, port A2

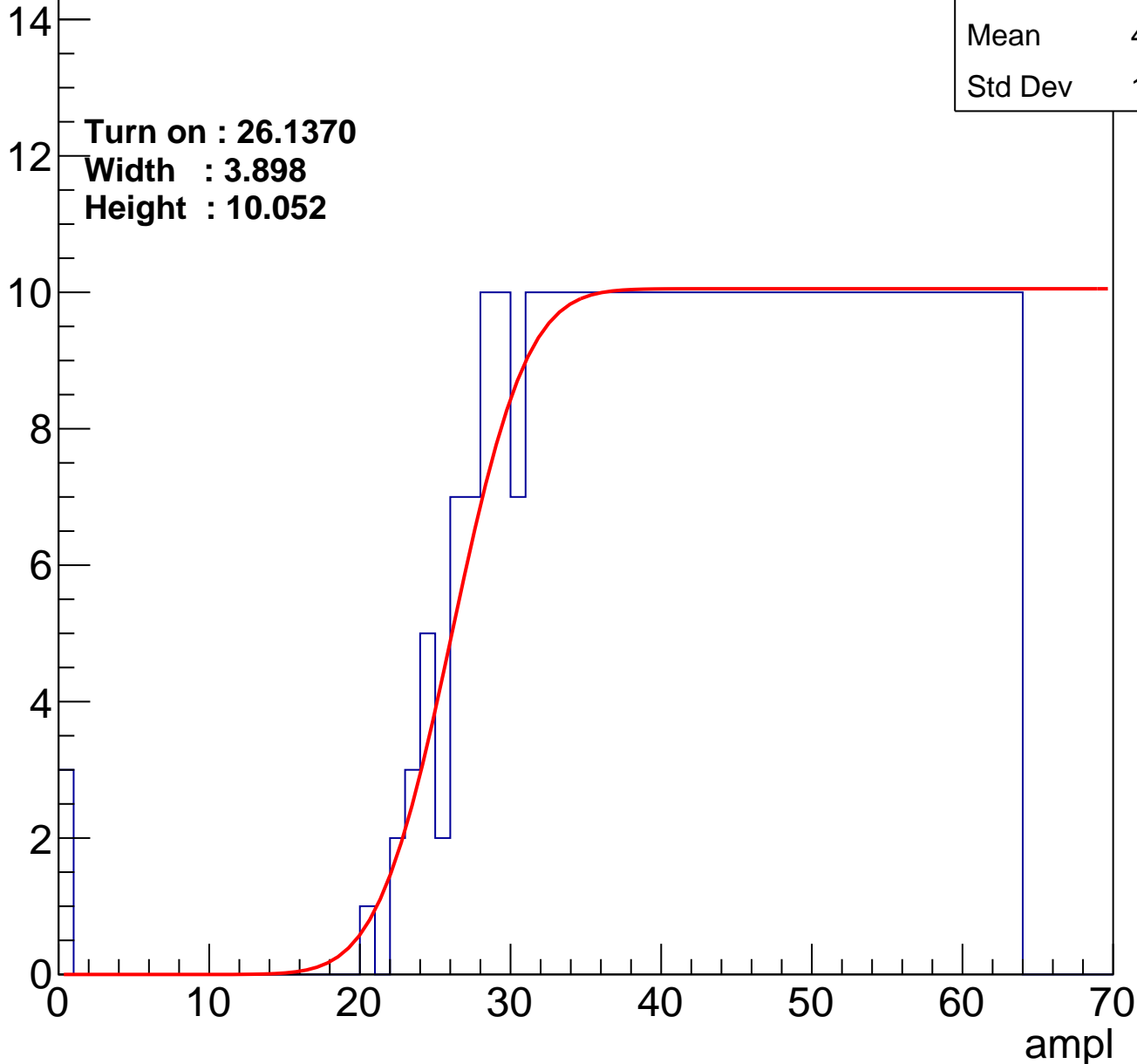
Entries	387
Mean	43.83
Std Dev	11.89

**Turn on : 26.1370**

**Width : 3.898**

**Height : 10.052**

Entry



# B1L100S, U7-ch8

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	361
Mean	45.32
Std Dev	10.74

**Turn on : 28.2486**

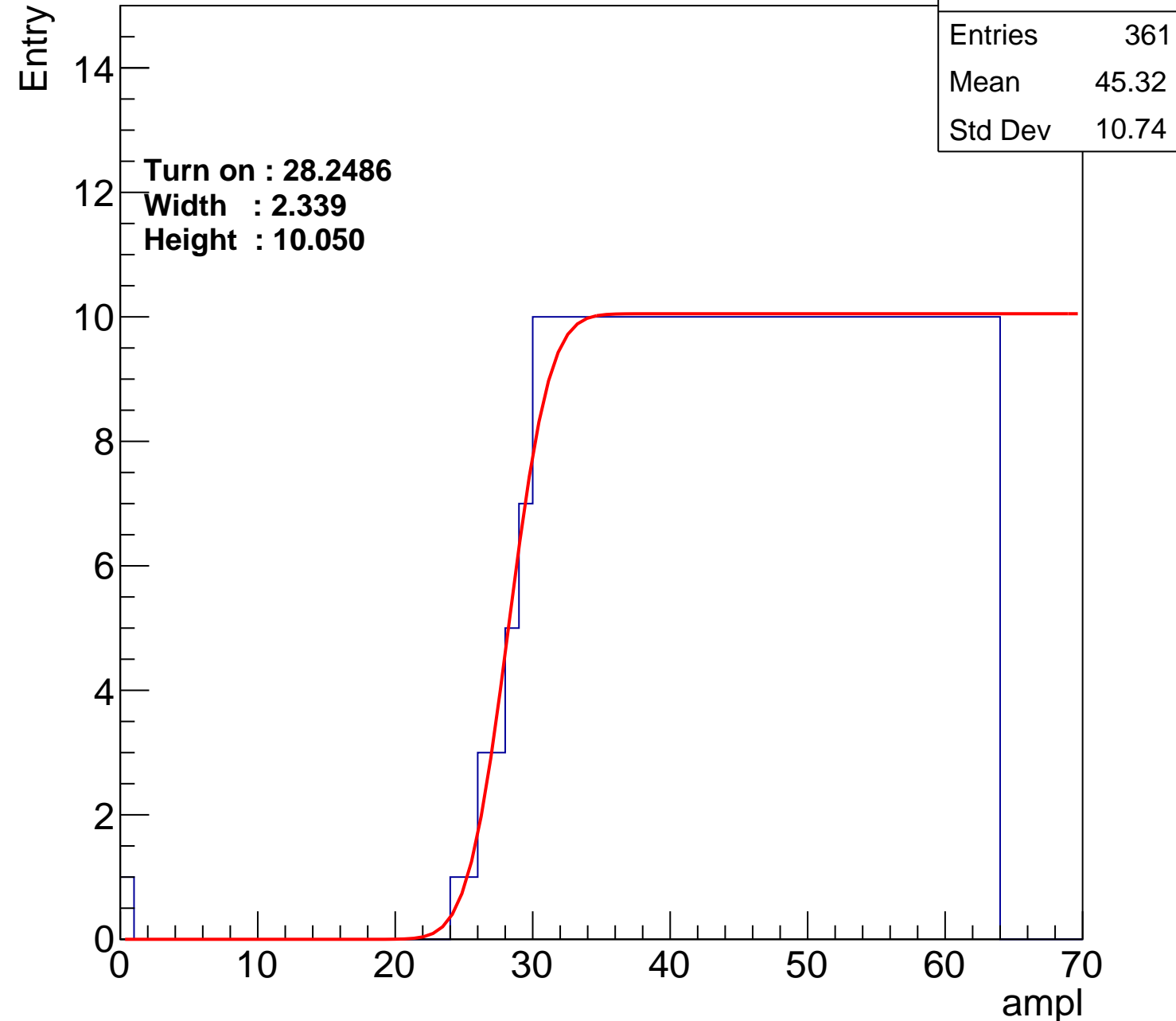
**Width : 2.339**

**Height : 10.050**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch9

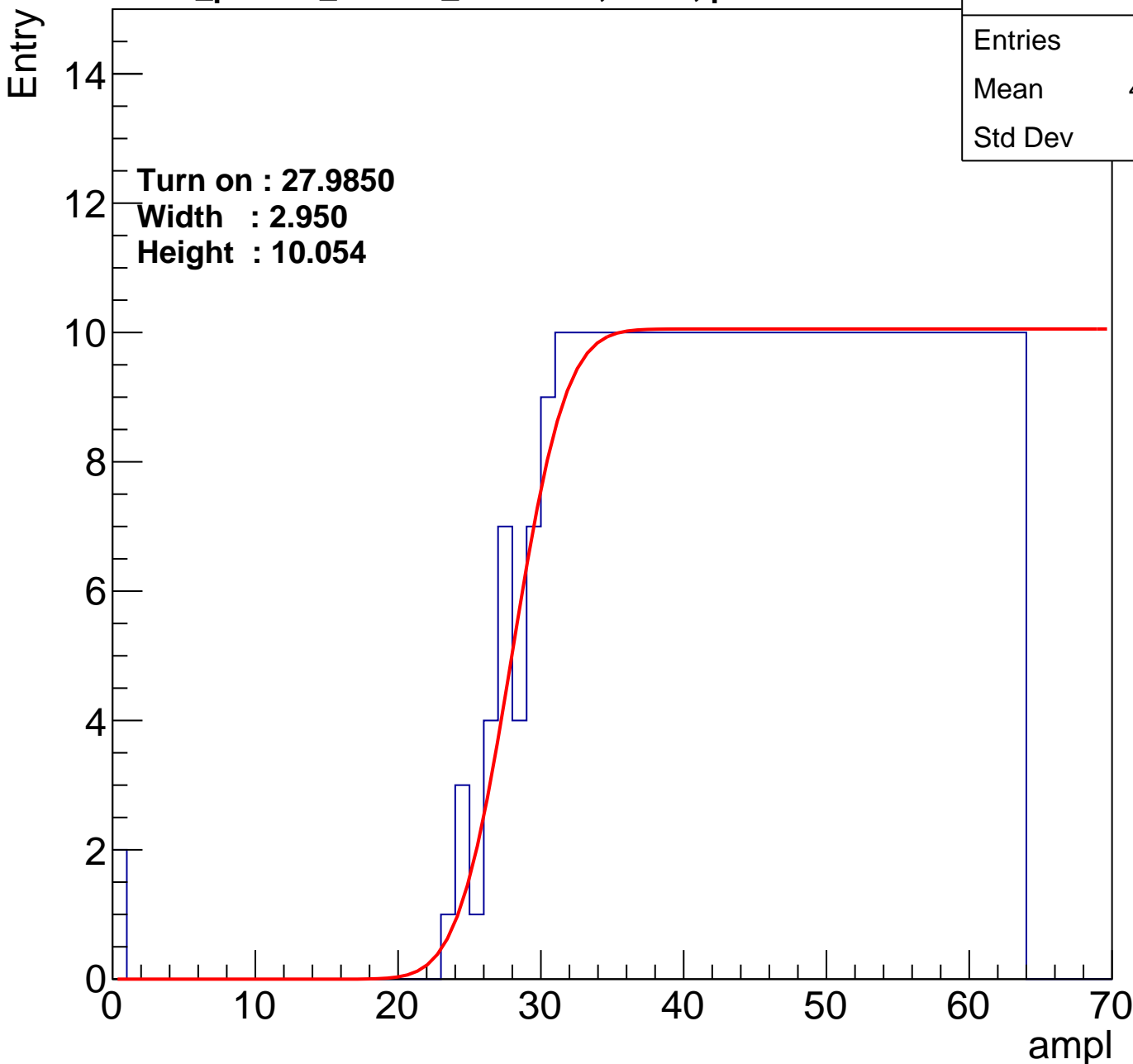
**calib\_packv5\_042523\_0143.root, FC#4, port A2**

**Turn on : 27.9850**

**Width : 2.950**

**Height : 10.054**

Entries	368
Mean	44.86
Std Dev	11.2



# B1L100S, U7-ch10

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	375
Mean	44.63
Std Dev	11.1

Turn on : 26.8768

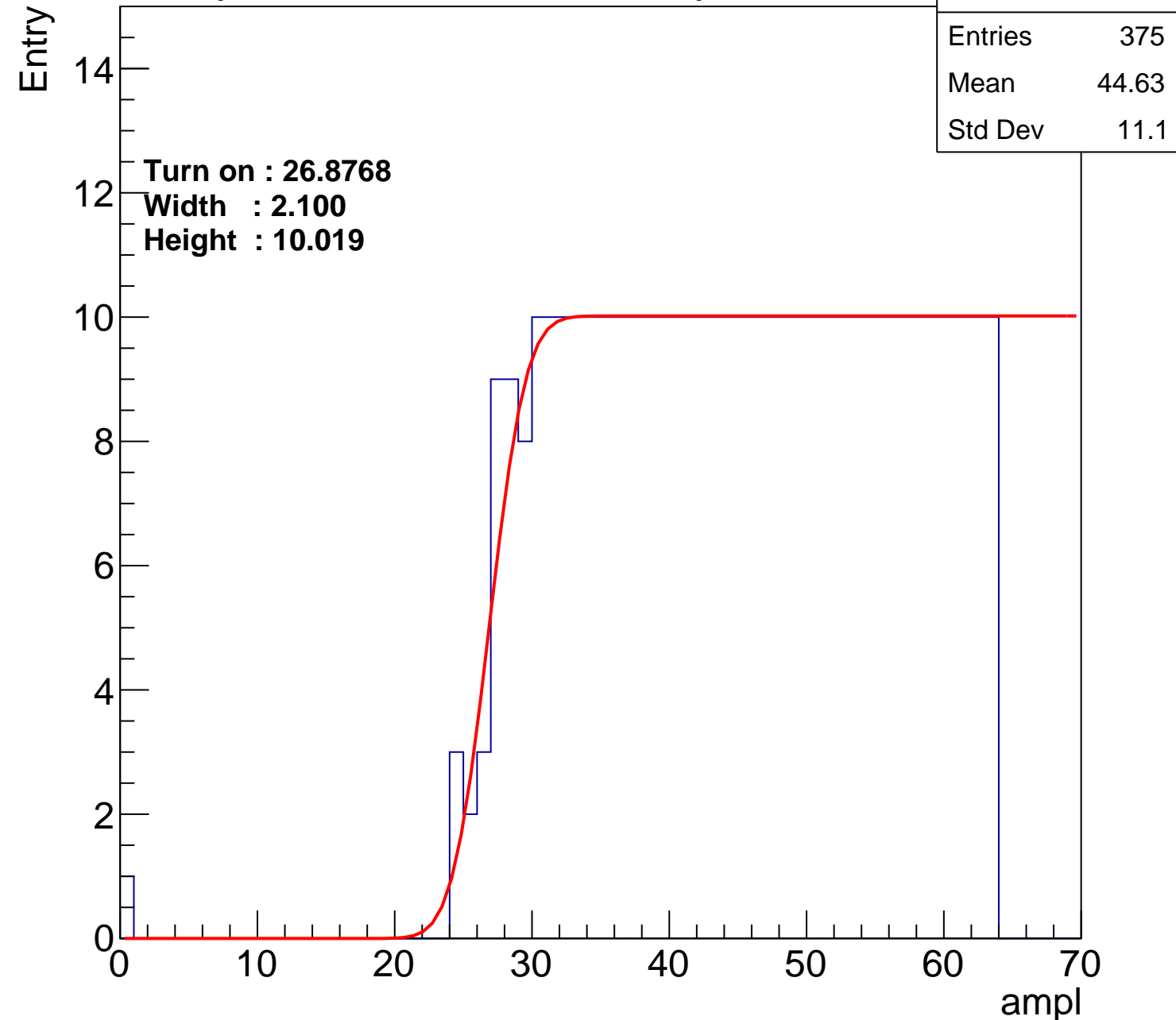
Width : 2.100

Height : 10.019

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch11

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	358
Mean	45.42
Std Dev	10.74

Turn on : 28.2635

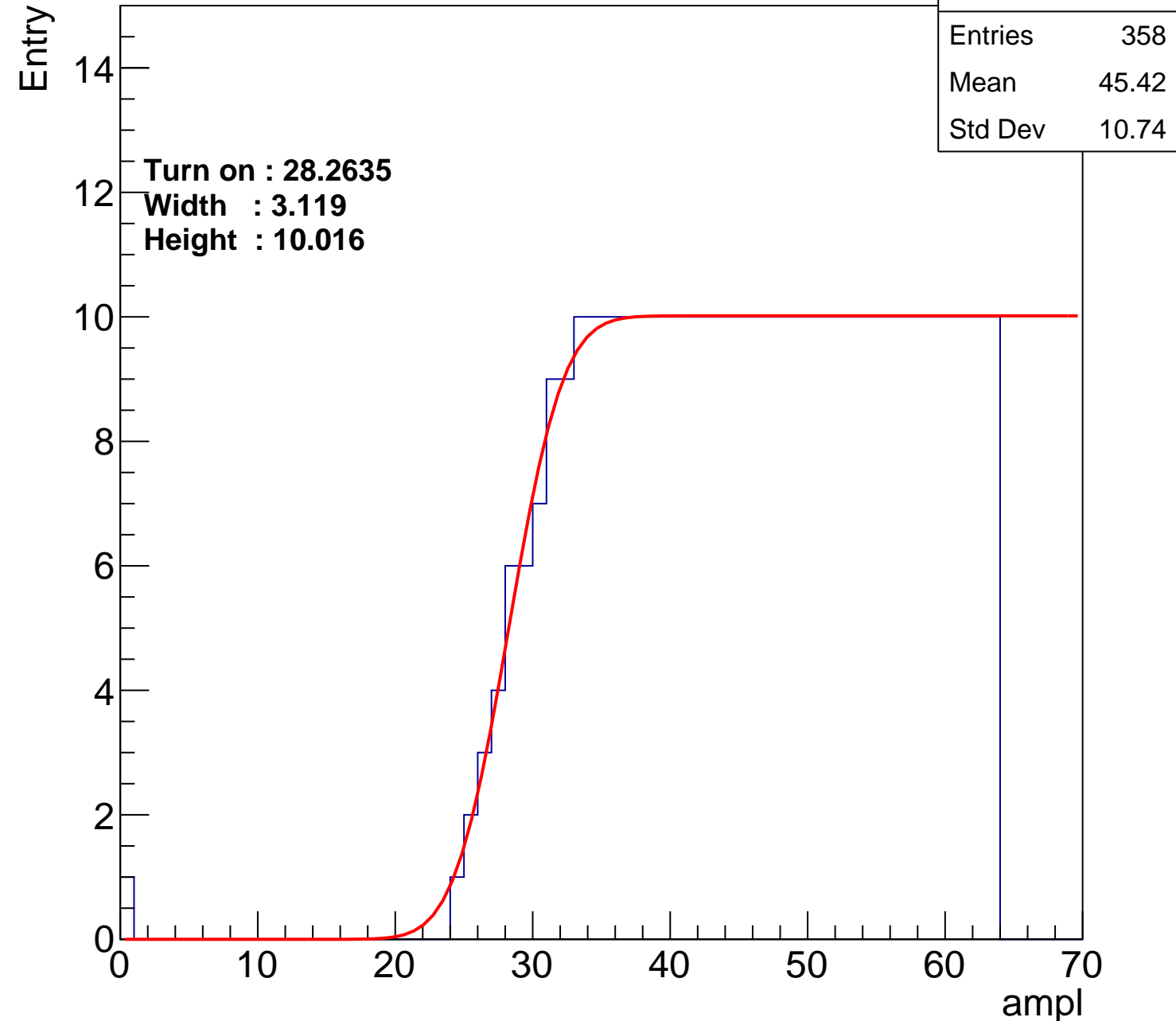
Width : 3.119

Height : 10.016

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch12

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	400
Mean	43.27
Std Dev	12.04

**Turn on : 24.4528**

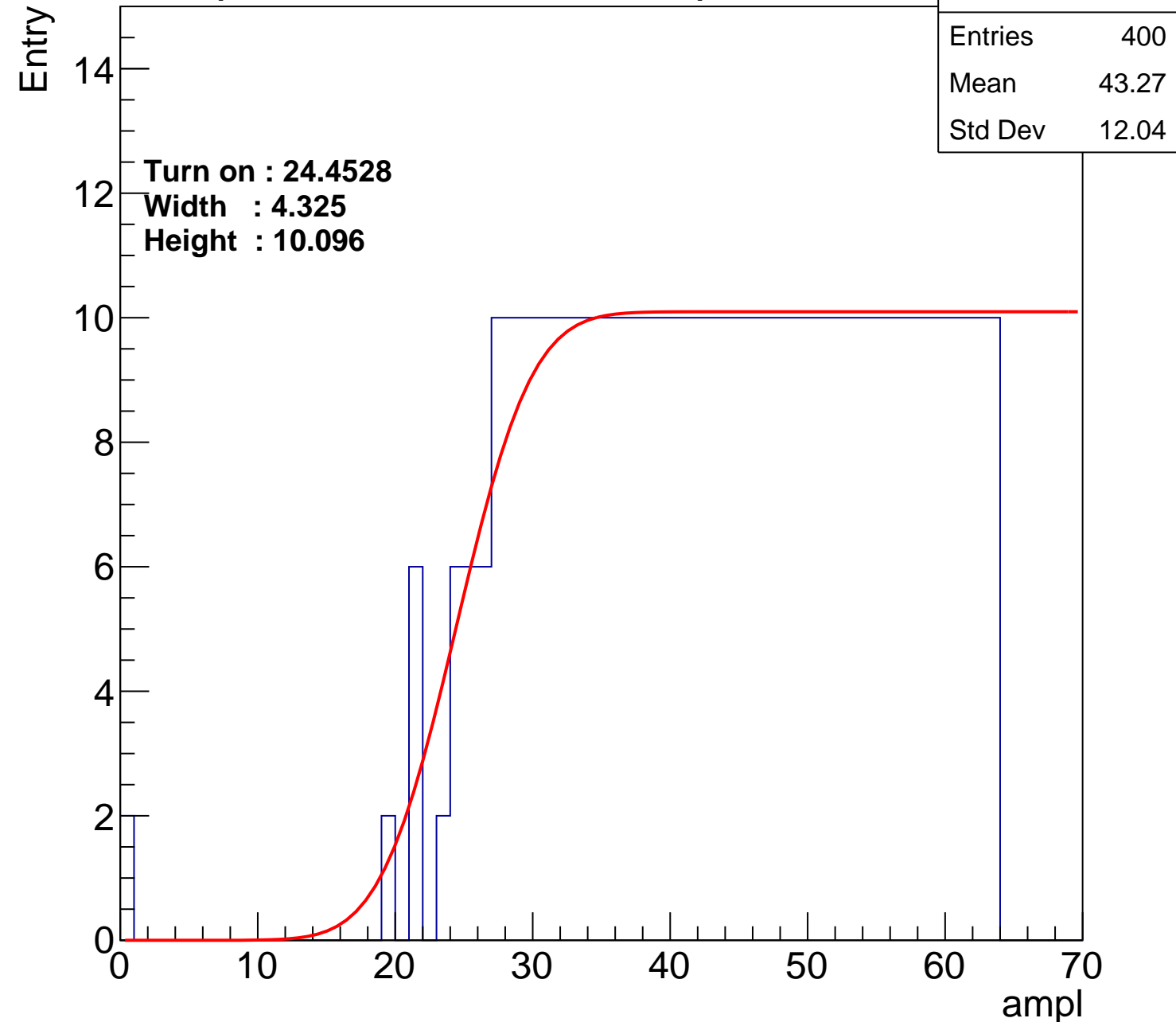
**Width : 4.325**

**Height : 10.096**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch13

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	376
Mean	44.41
Std Dev	11.56

Turn on : 27.0482

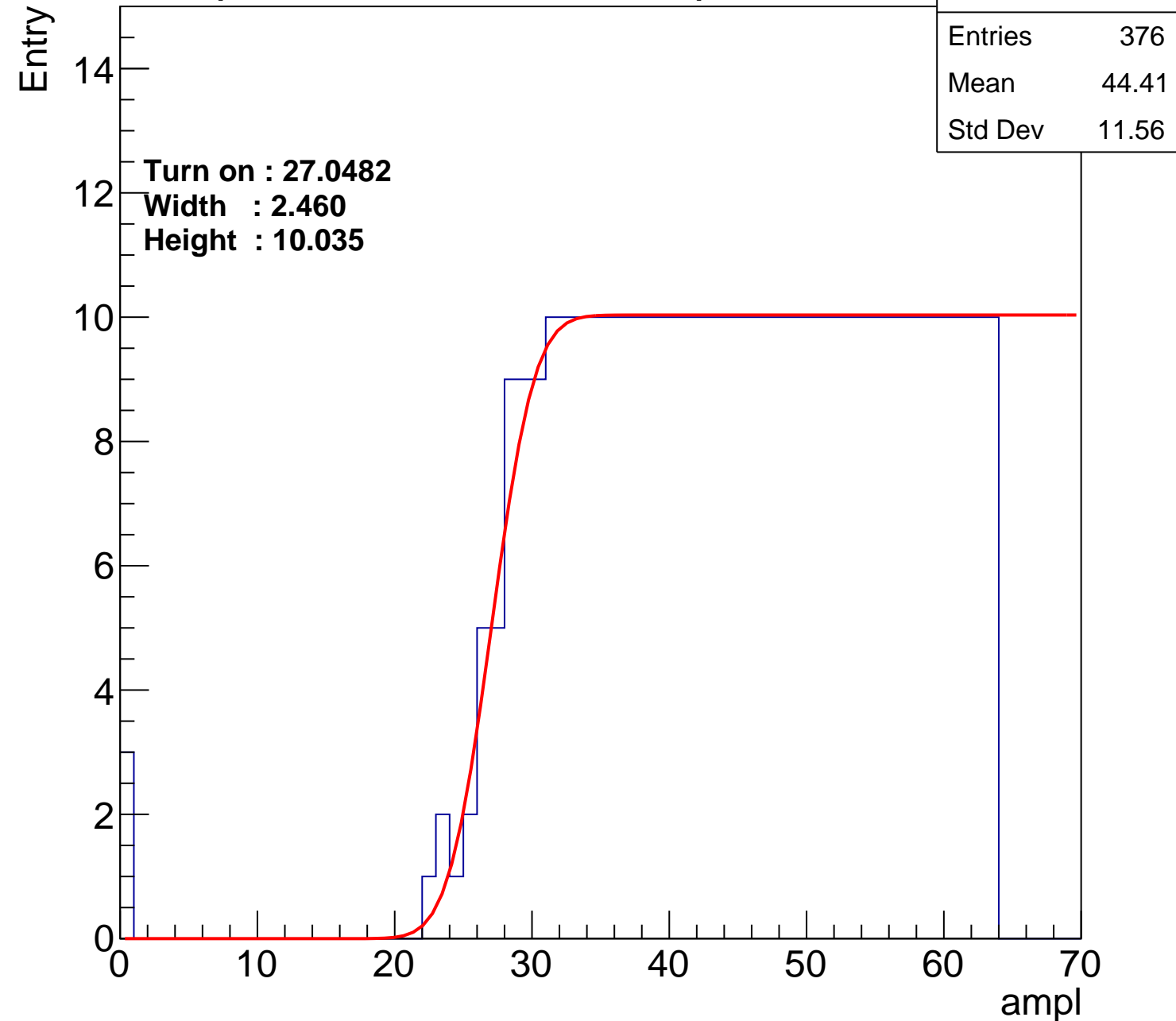
Width : 2.460

Height : 10.035

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch14

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	382
Mean	44.01
Std Dev	11.94

Turn on : 25.6453

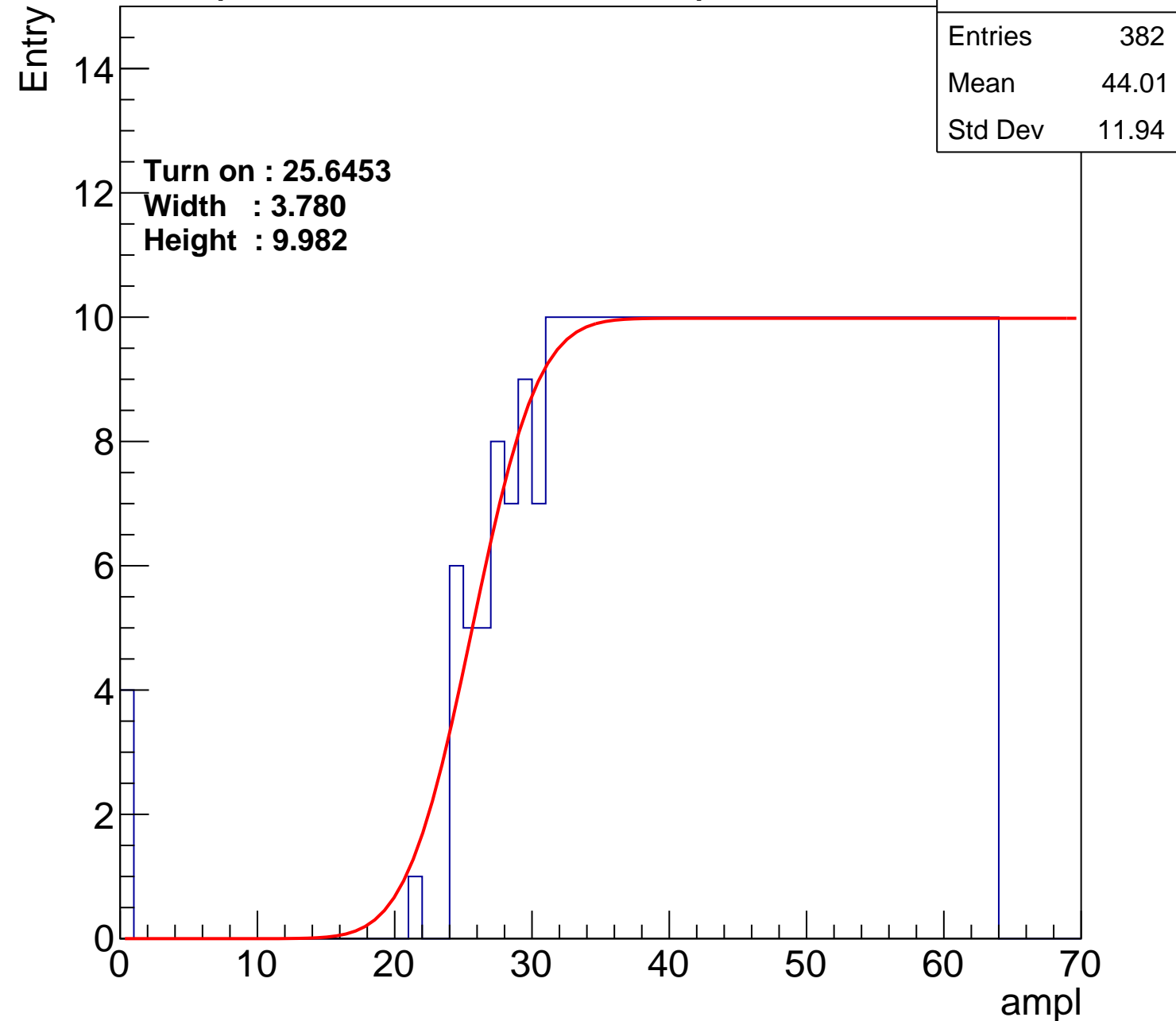
Width : 3.780

Height : 9.982

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L100S, U7-ch15

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	360
Mean	45.31
Std Dev	10.82

Turn on : 28.3358

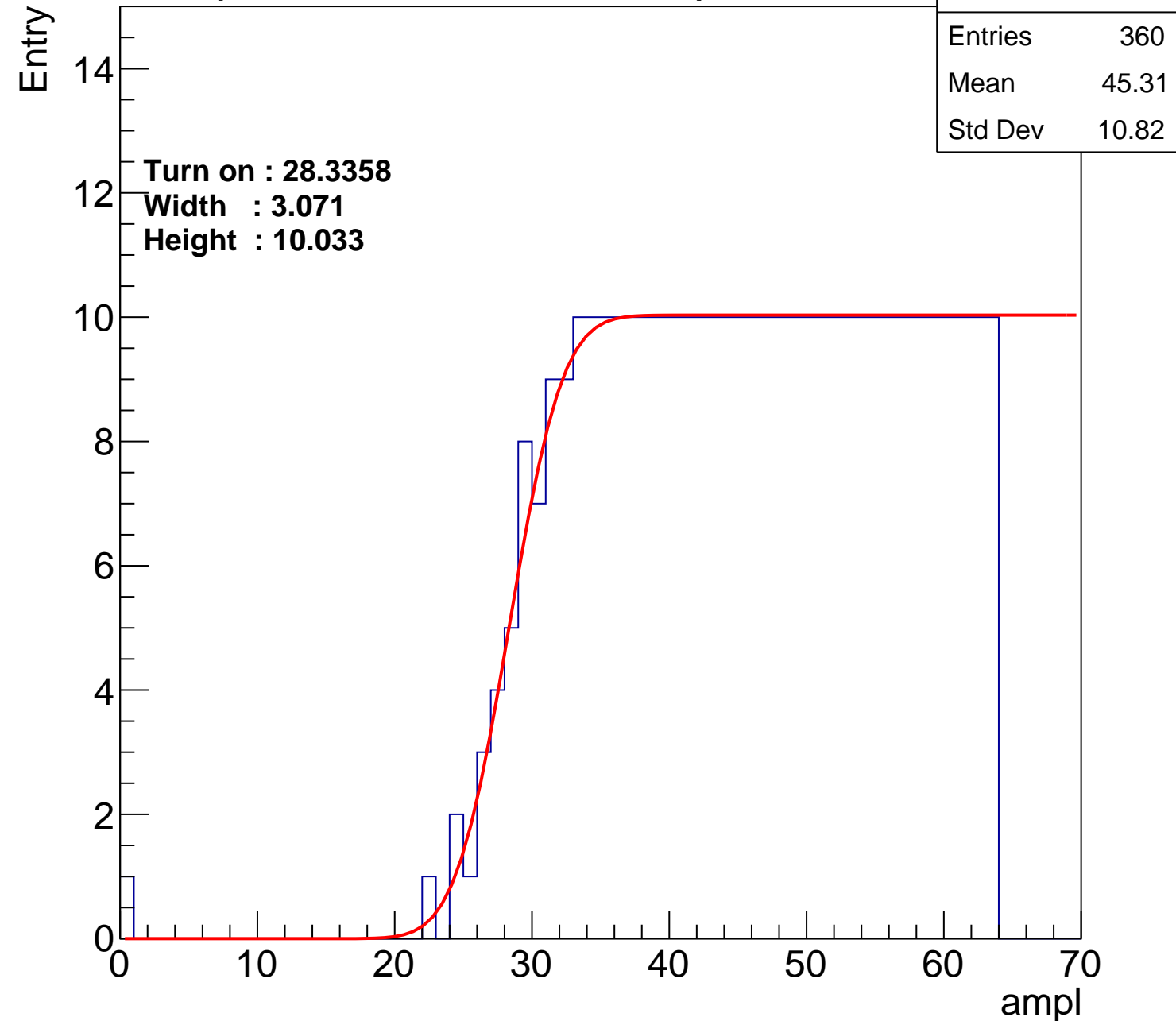
Width : 3.071

Height : 10.033

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch16

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	384
Mean	44.07
Std Dev	11.61

Turn on : 26.0342

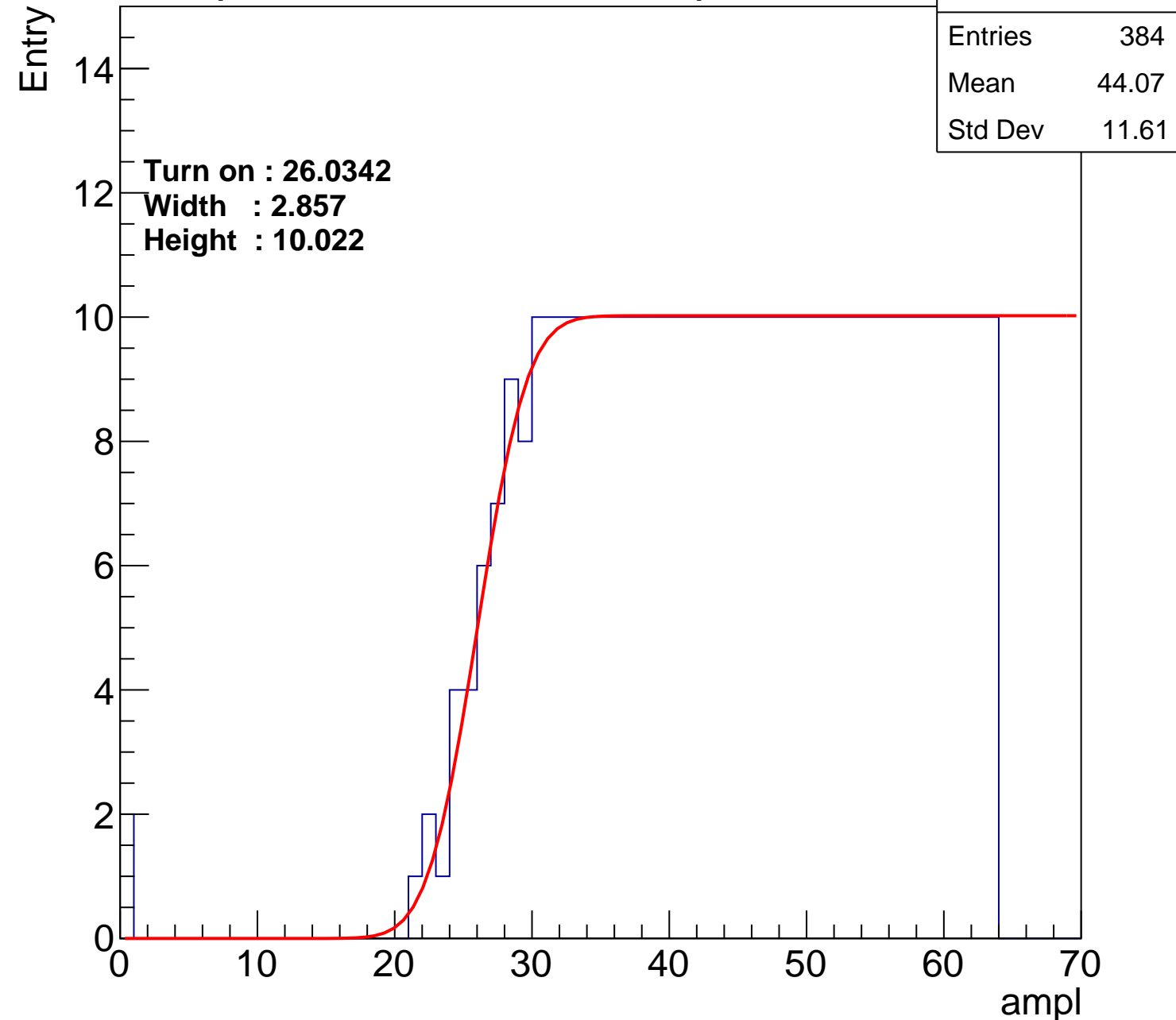
Width : 2.857

Height : 10.022

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch17

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	392
Mean	43.56
Std Dev	12.13

Turn on : 25.3411

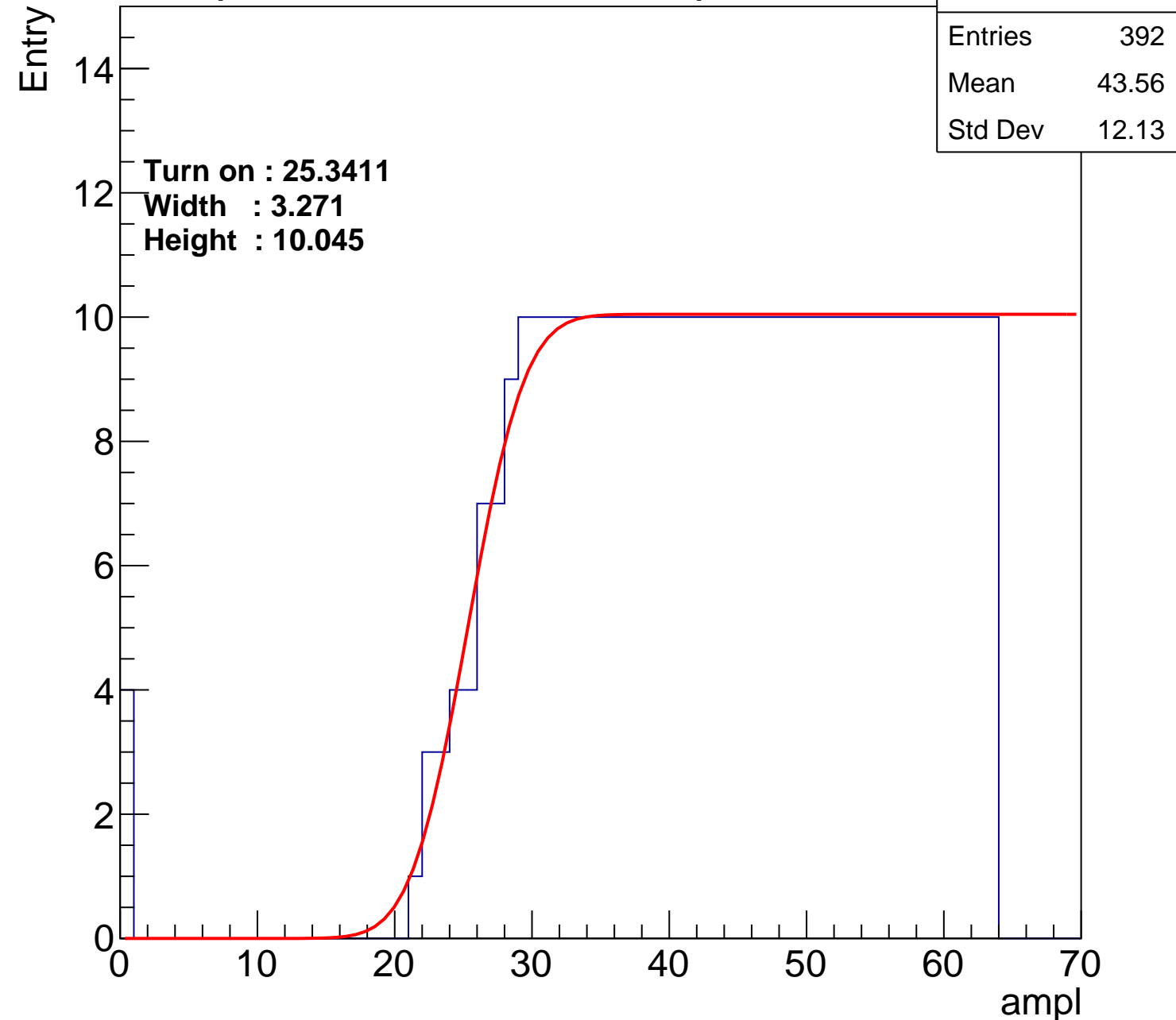
Width : 3.271

Height : 10.045

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch18

**calib\_packv5\_042523\_0143.root, FC#4, port A2**

Entries	361
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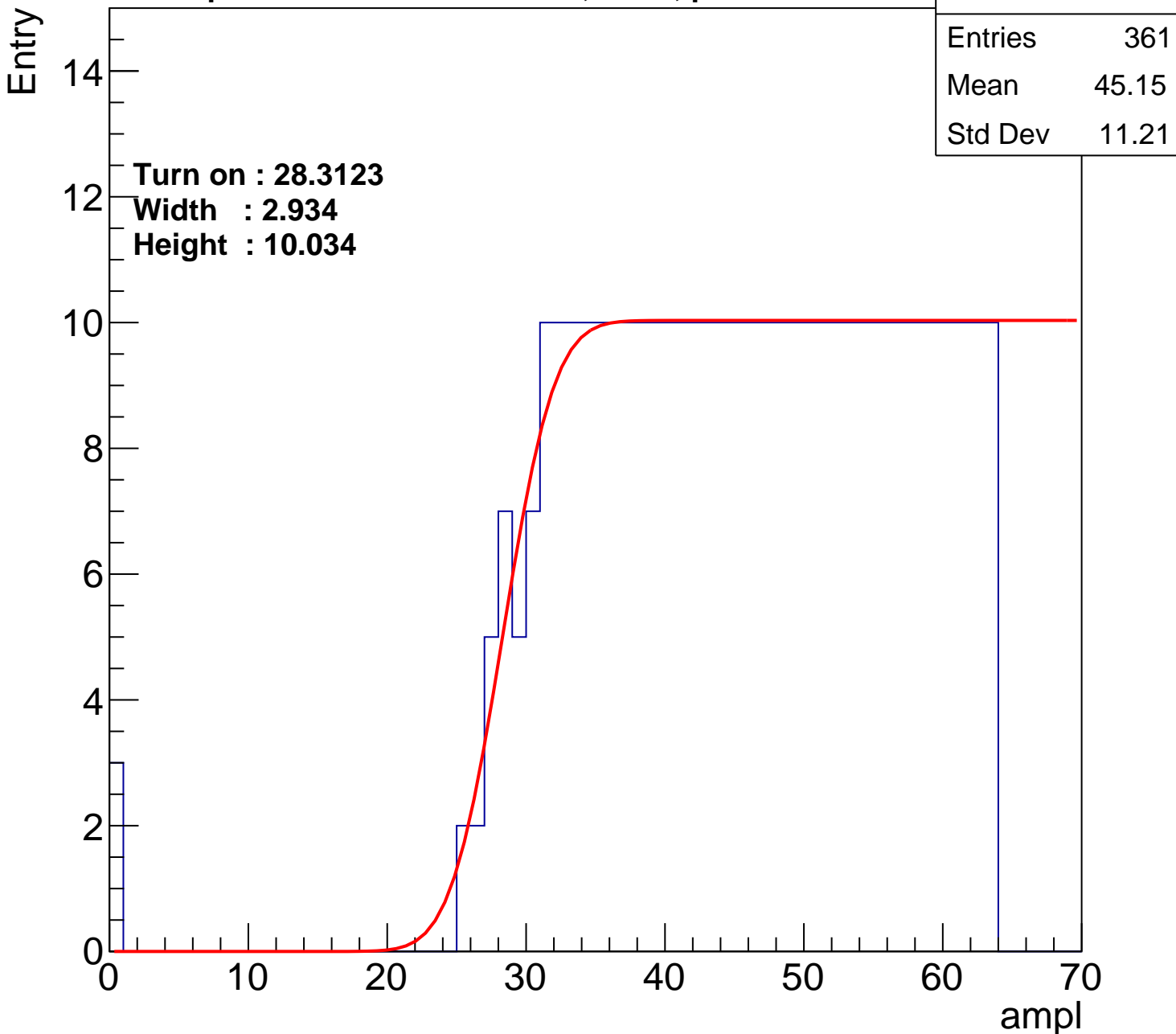
Mean	45.15
------	-------

Std Dev	11.21
---------	-------

**Turn on : 28.3123**

**Width : 2.934**

**Height : 10.034**



# B1L100S, U7-ch19

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	391
Mean	43.7
Std Dev	11.84

Turn on : 25.4640

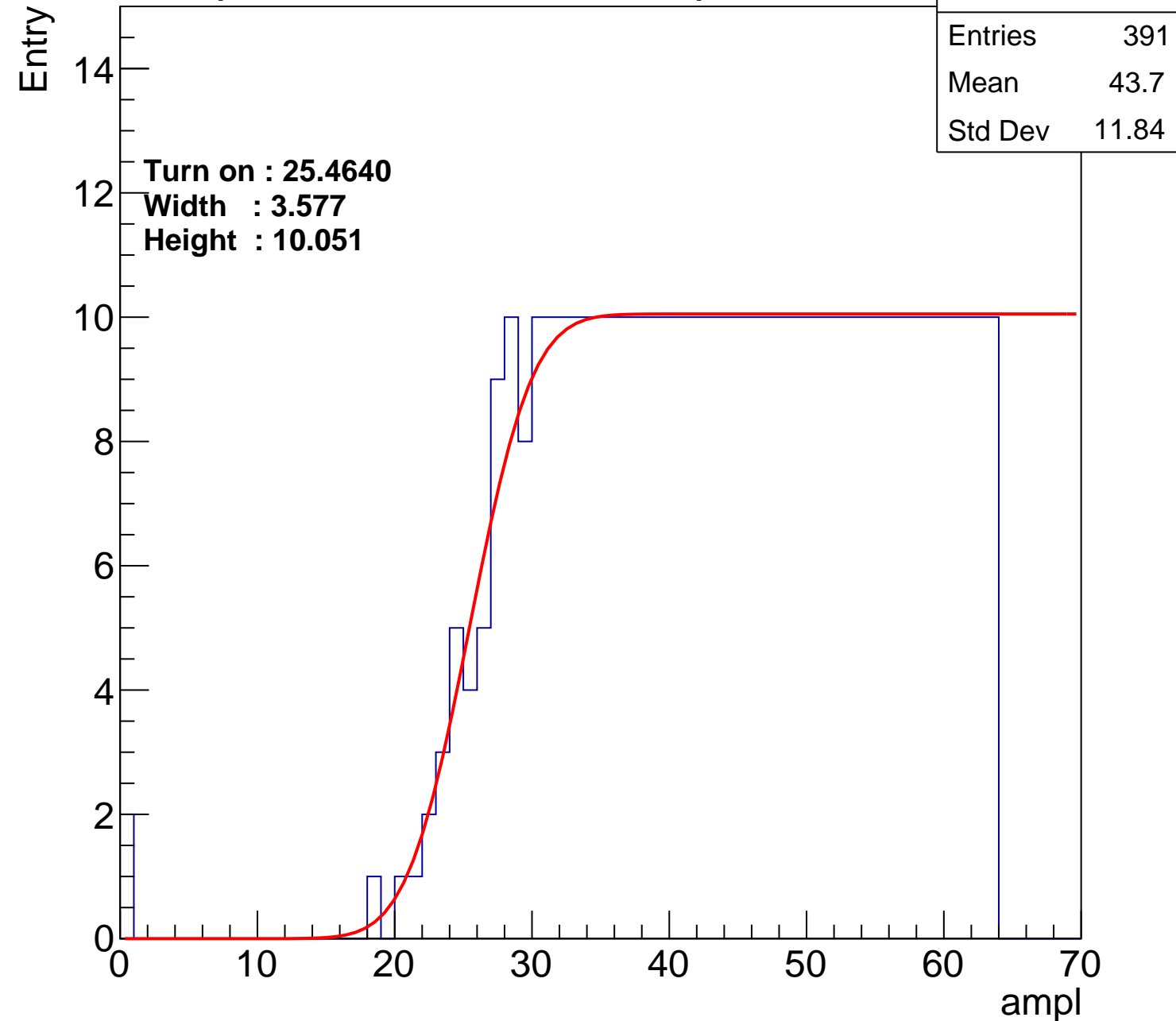
Width : 3.577

Height : 10.051

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch20

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	402
Mean	43.13
Std Dev	12.22

Turn on : 24.3386

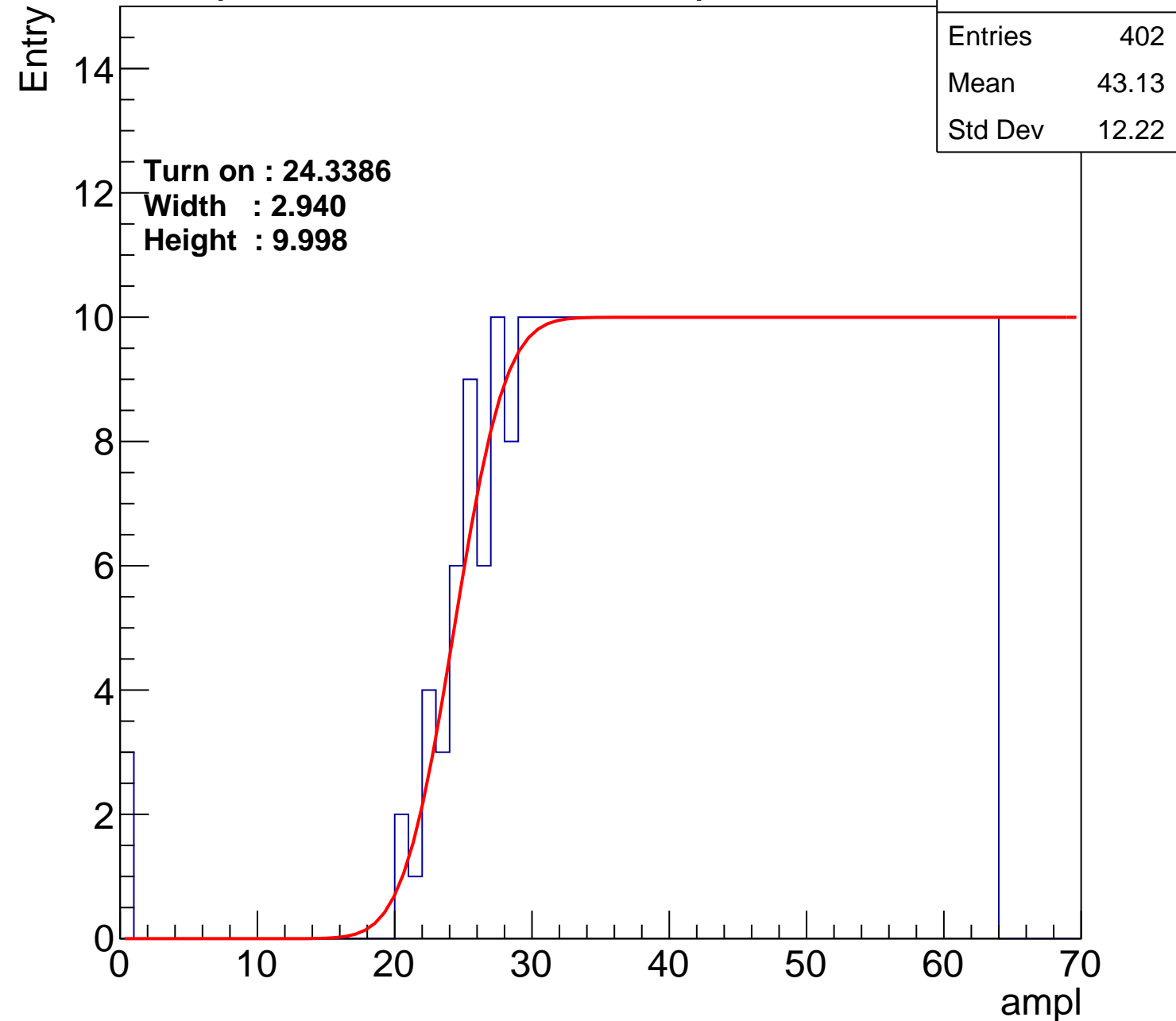
Width : 2.940

Height : 9.998

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch21

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	381
Mean	44.11
Std Dev	11.84

Turn on : 25.5607

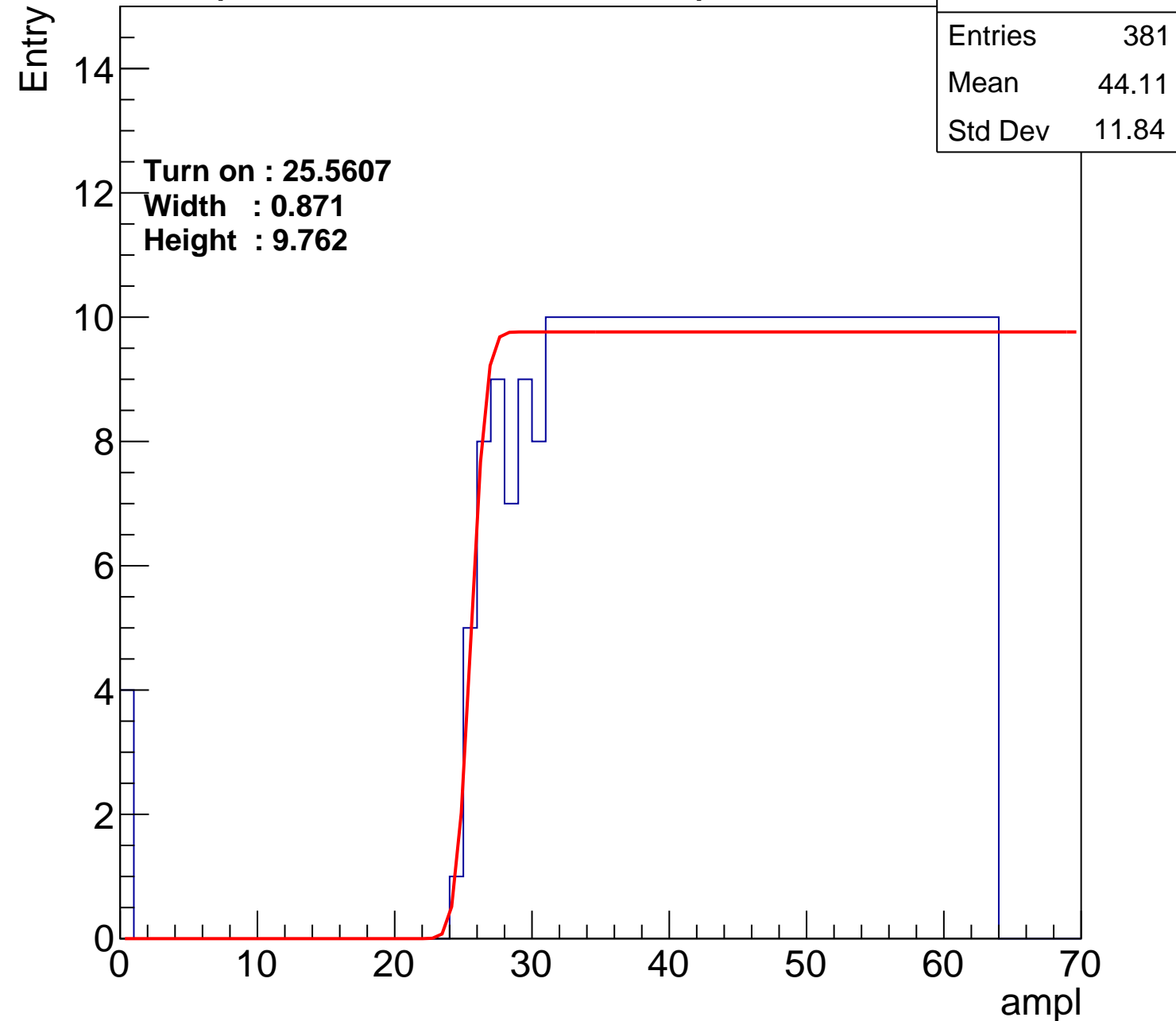
Width : 0.871

Height : 9.762

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch22

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	384
Mean	44.07
Std Dev	11.61

Turn on : 25.9823

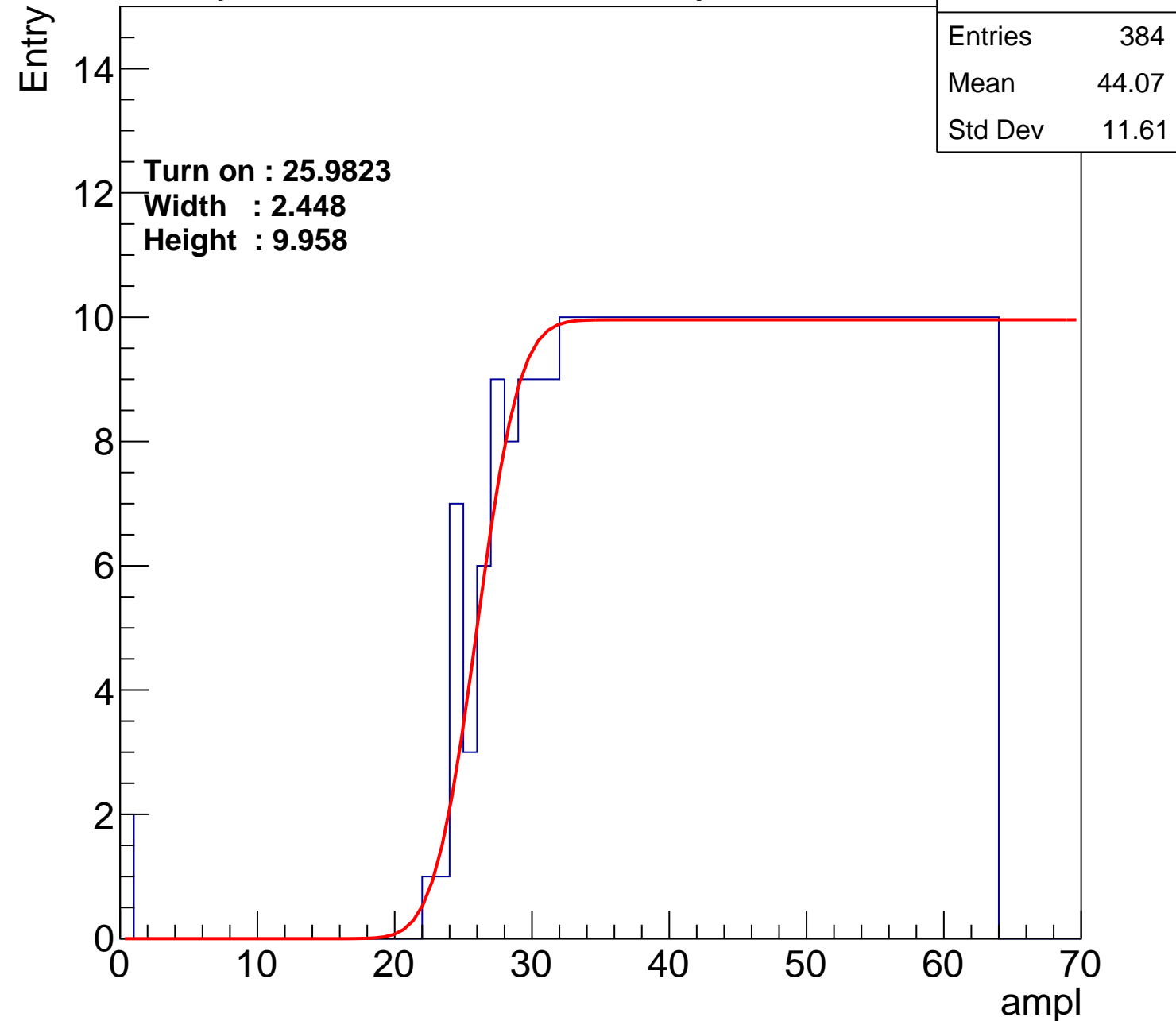
Width : 2.448

Height : 9.958

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L100S, U7-ch23

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	381
Mean	44.09
Std Dev	11.88

Turn on : 27.1408

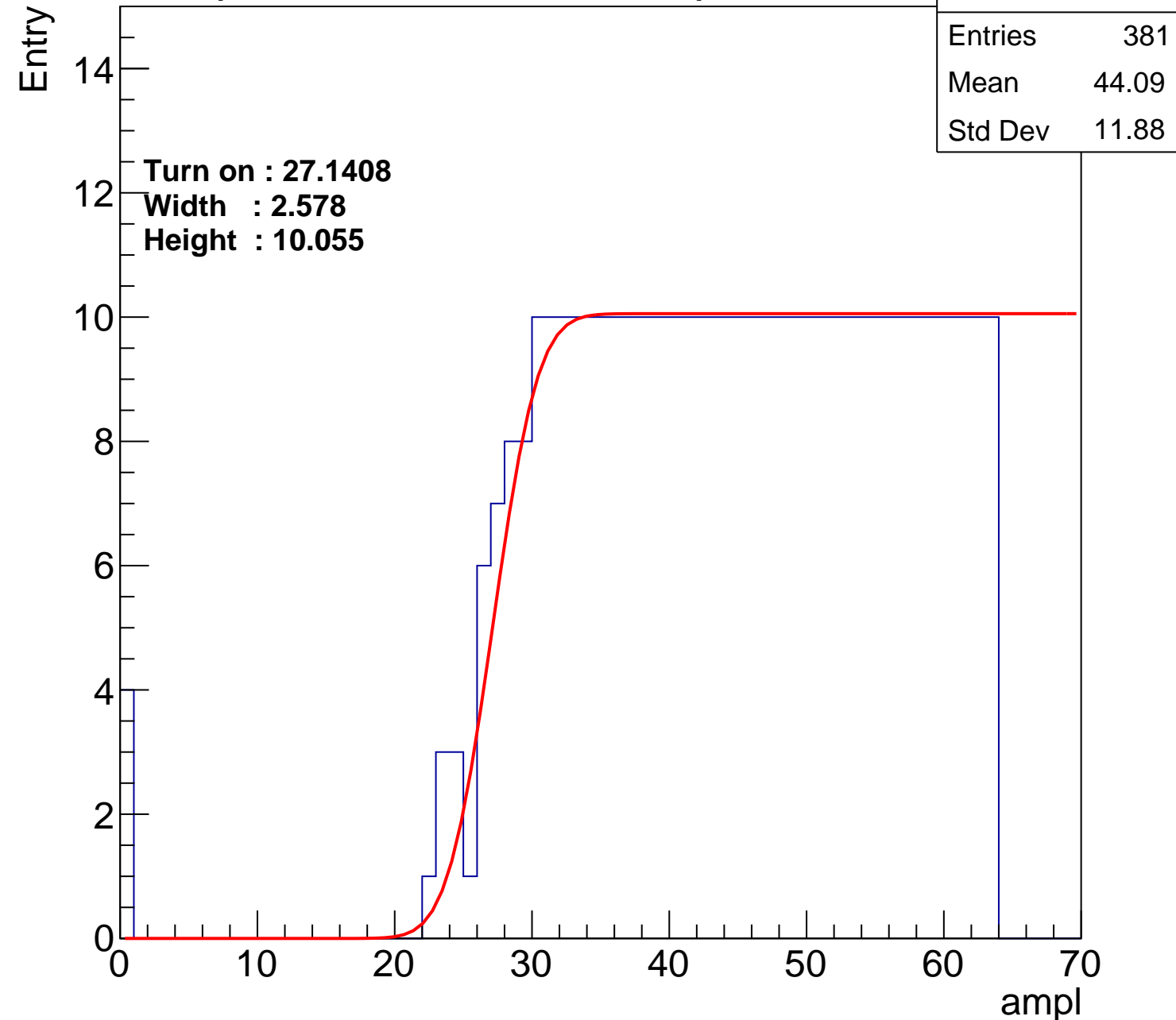
Width : 2.578

Height : 10.055

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch24

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	387
Mean	43.81
Std Dev	12

Turn on : 25.6144

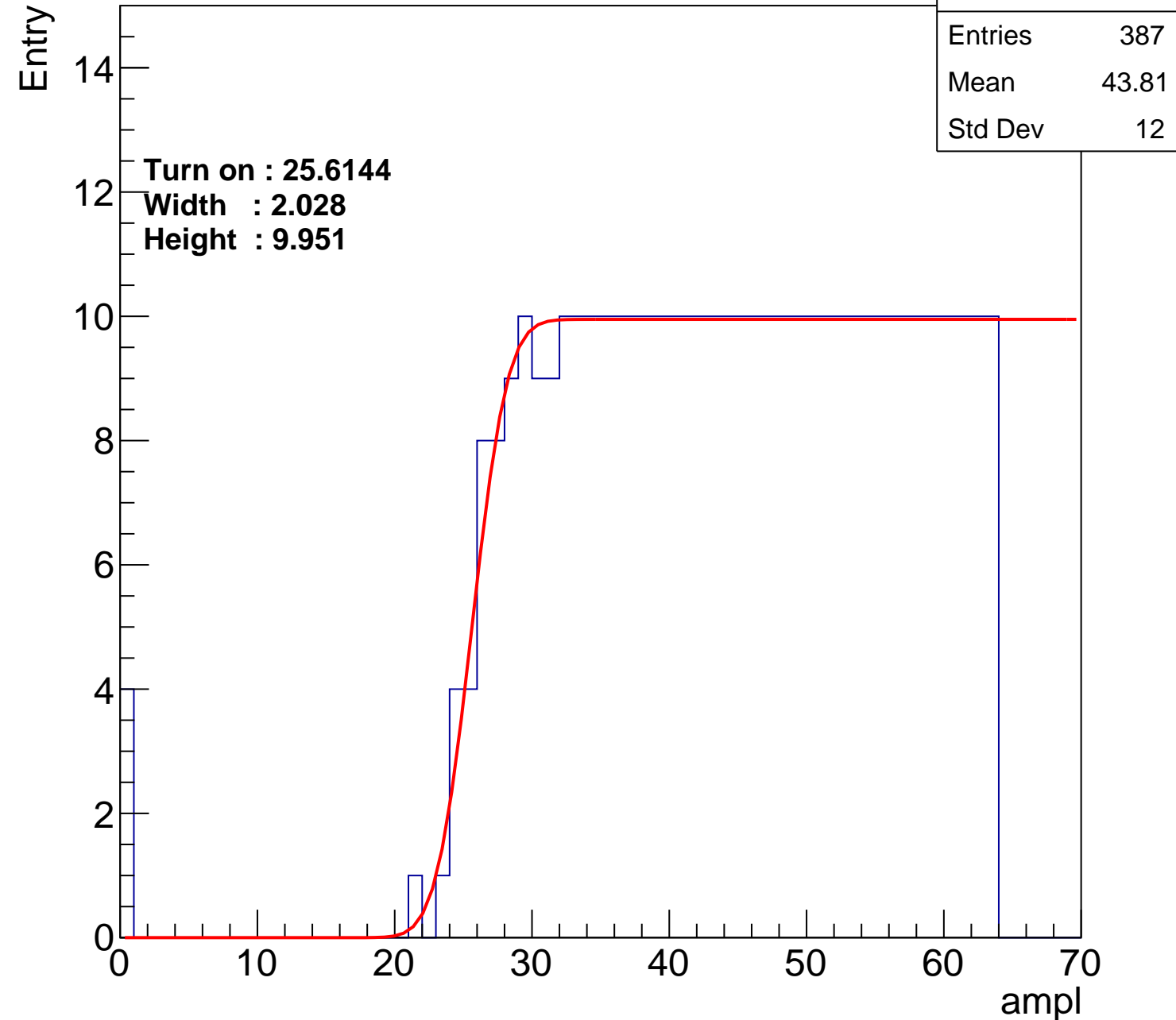
Width : 2.028

Height : 9.951

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch25

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	362
Mean	45.18
Std Dev	11

Turn on : 28.0949

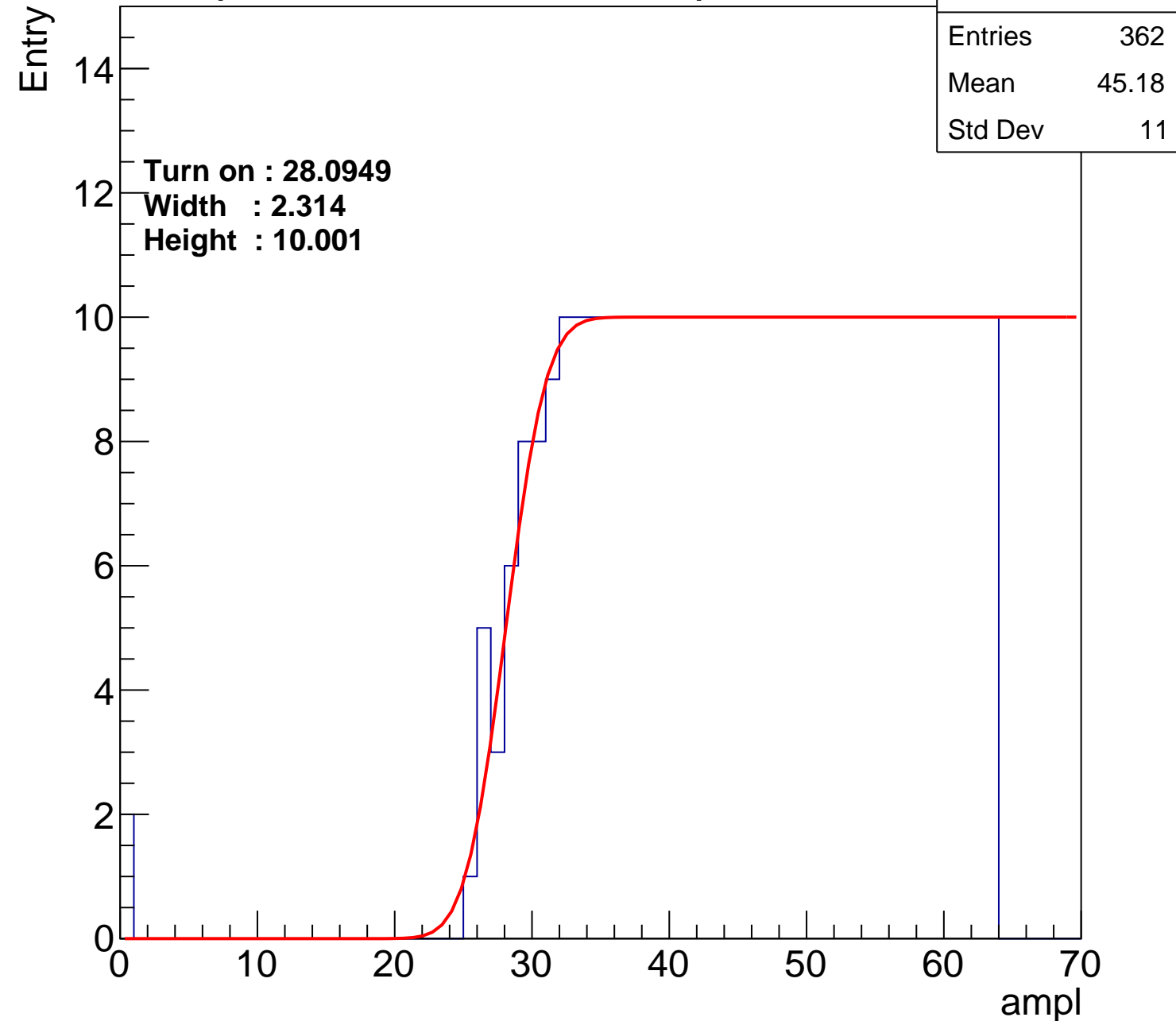
Width : 2.314

Height : 10.001

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch26

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	384
Mean	44.06
Std Dev	11.63

Turn on : 26.1076

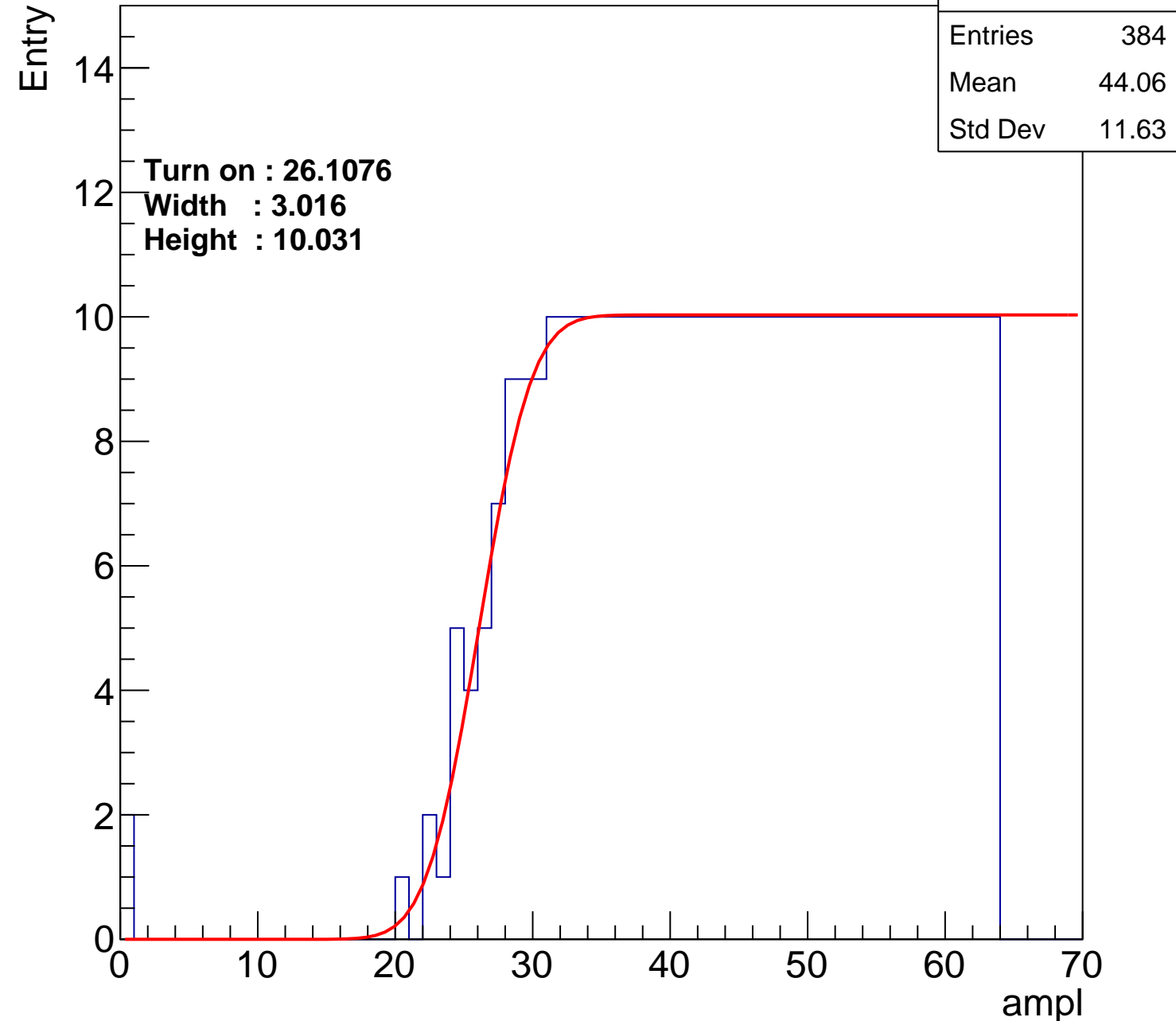
Width : 3.016

Height : 10.031

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch27

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	376
Mean	44.42
Std Dev	11.56

Turn on : 26.9492

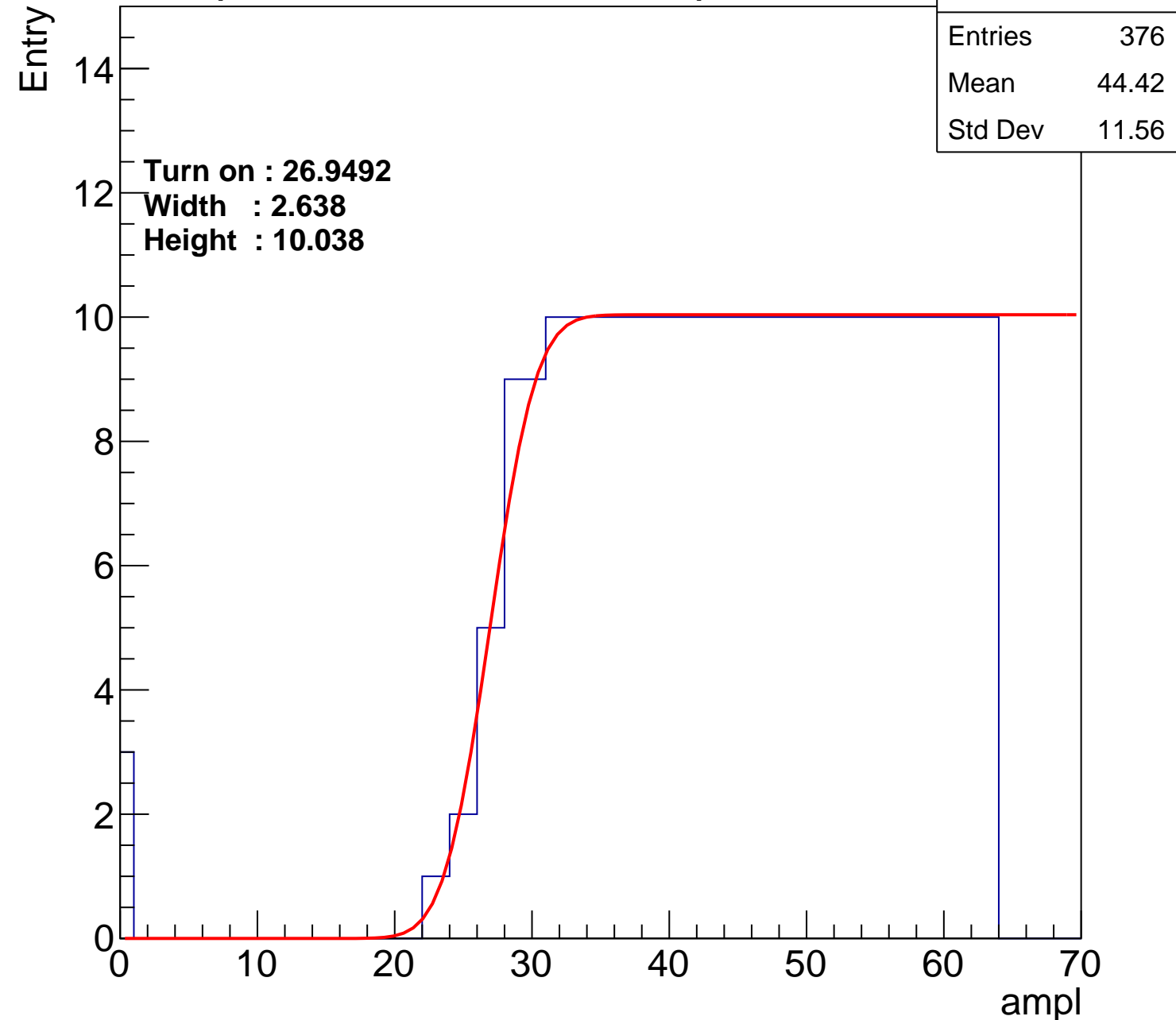
Width : 2.638

Height : 10.038

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch28

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	377
Mean	44.49
Std Dev	11.23

Turn on : 26.6900

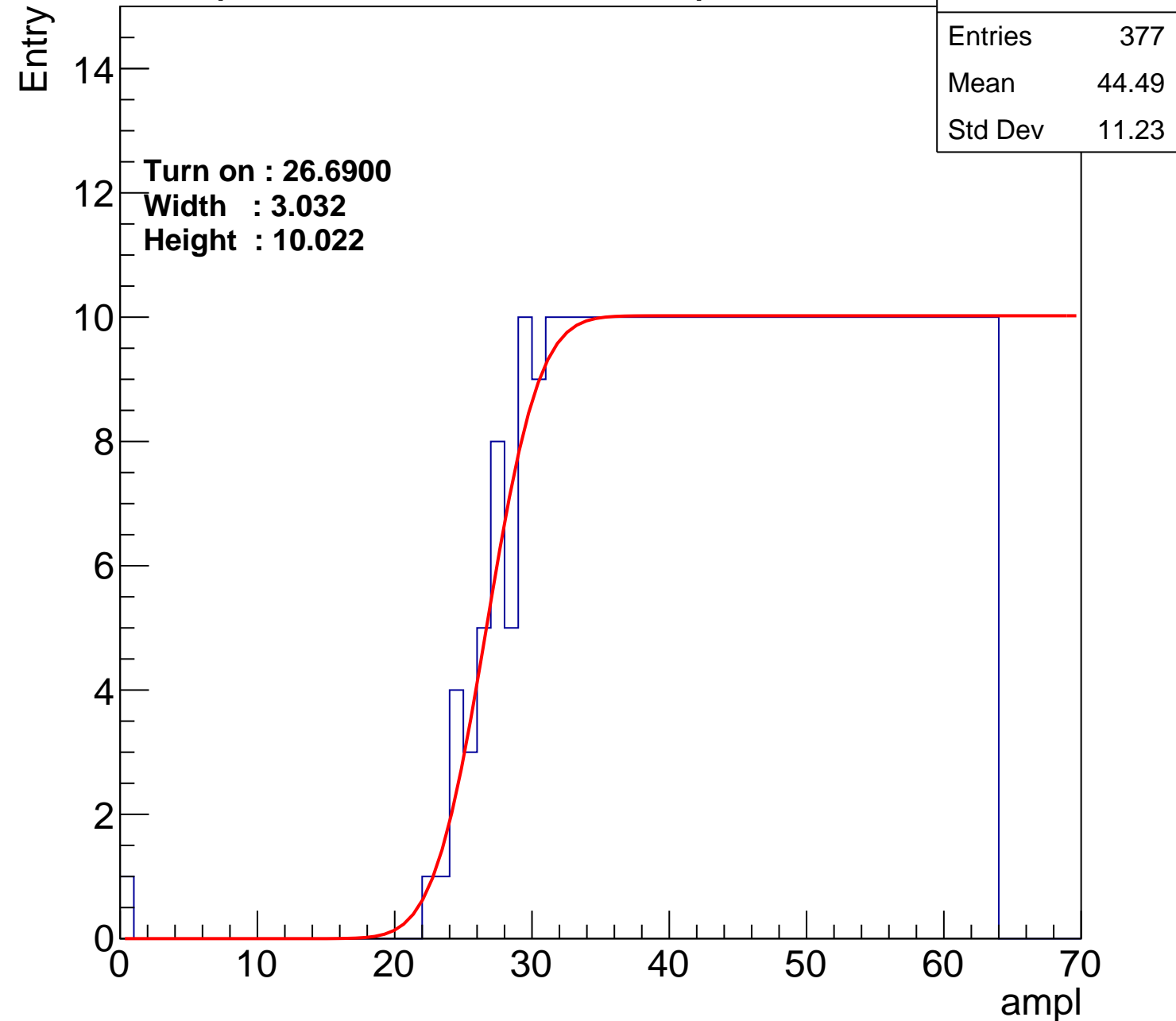
Width : 3.032

Height : 10.022

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch29

calib\_packv5\_042523\_0143.root, FC#4, port A2

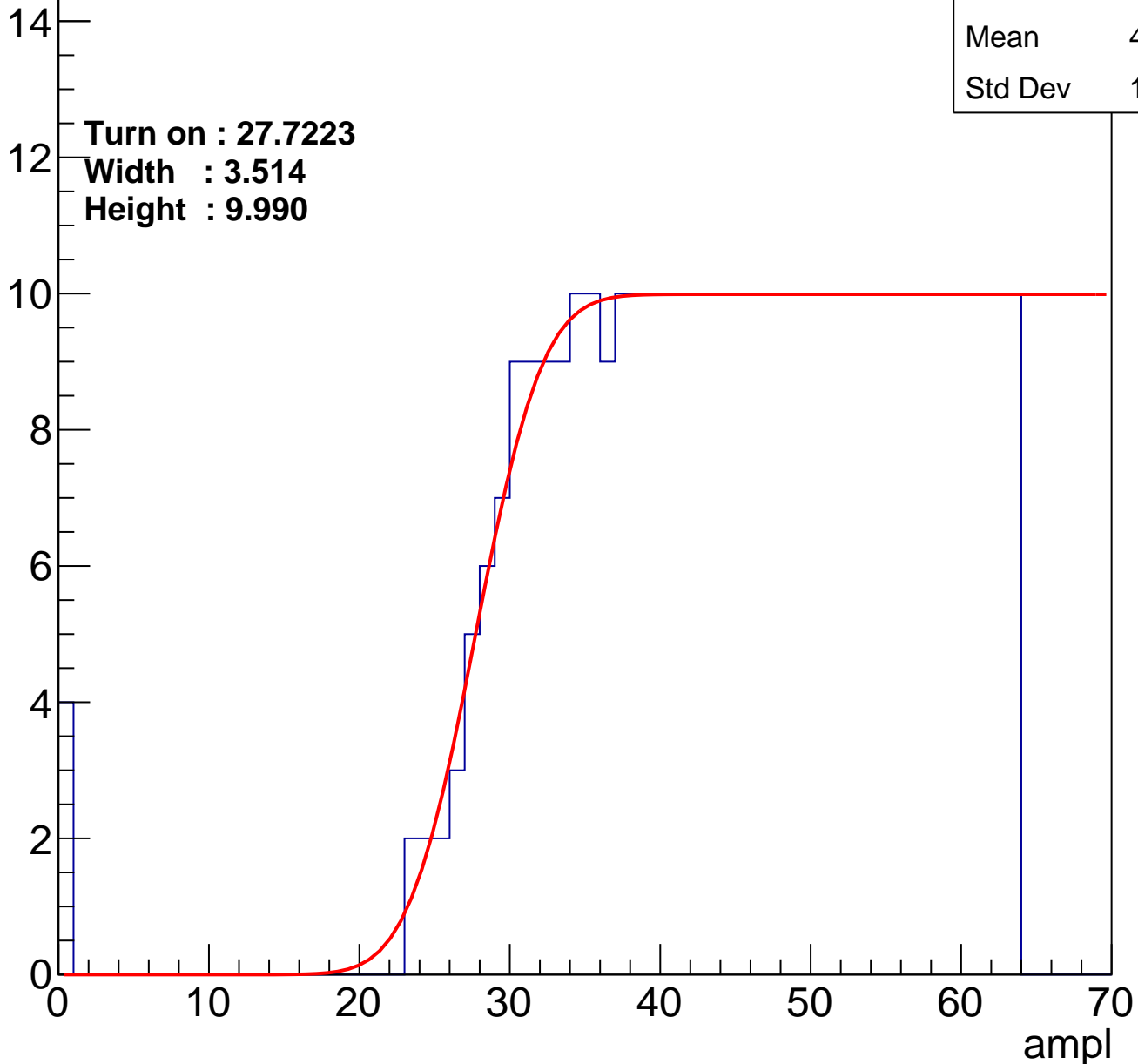
Entries	366
Mean	44.74
Std Dev	11.64

**Turn on : 27.7223**

**Width : 3.514**

**Height : 9.990**

Entry



# B1L100S, U7-ch30

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	371
Mean	44.74
Std Dev	11.24

**Turn on : 27.5133**

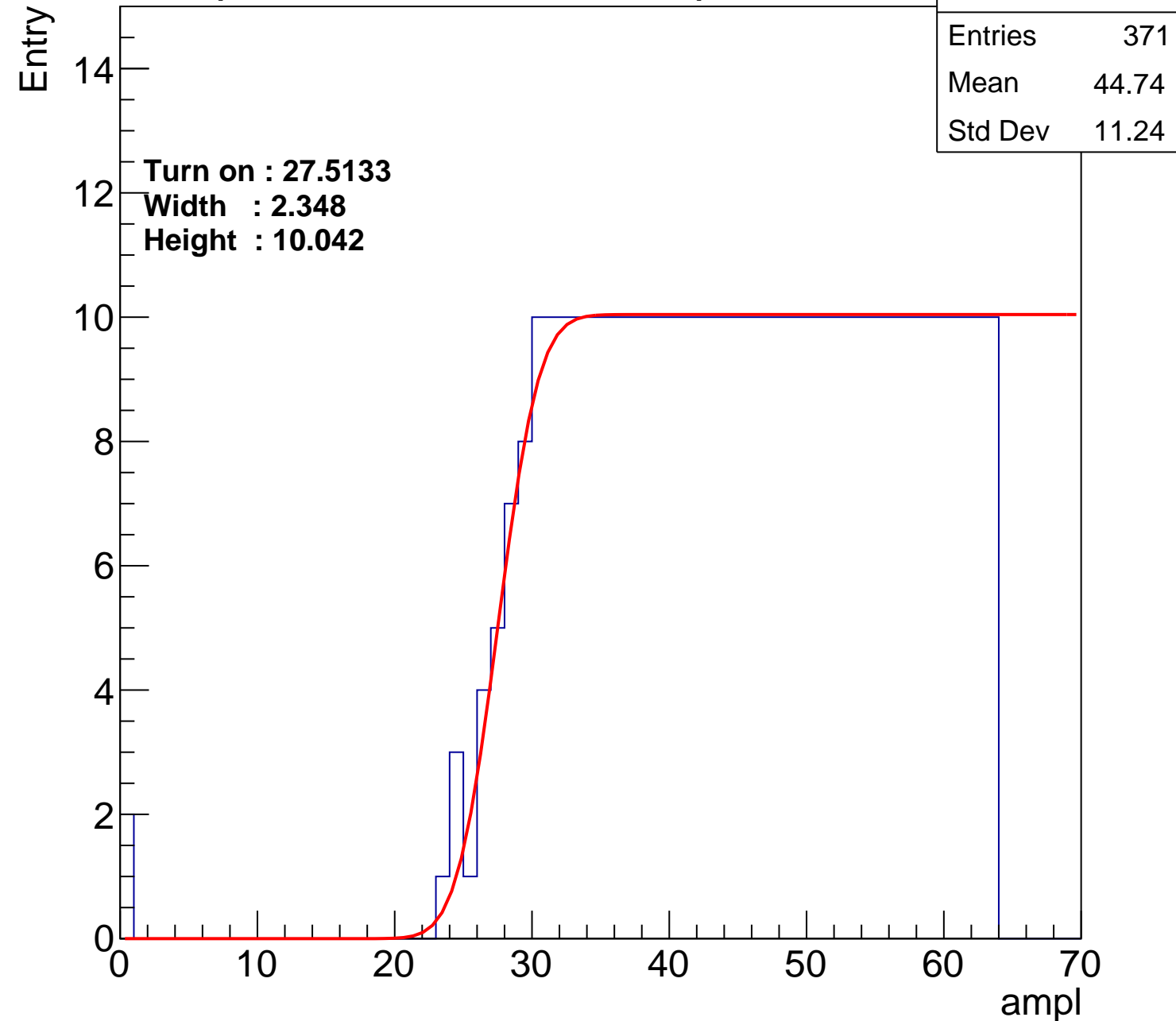
**Width : 2.348**

**Height : 10.042**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L100S, U7-ch31

calib\_packv5\_042523\_0143.root, FC#4, port A2

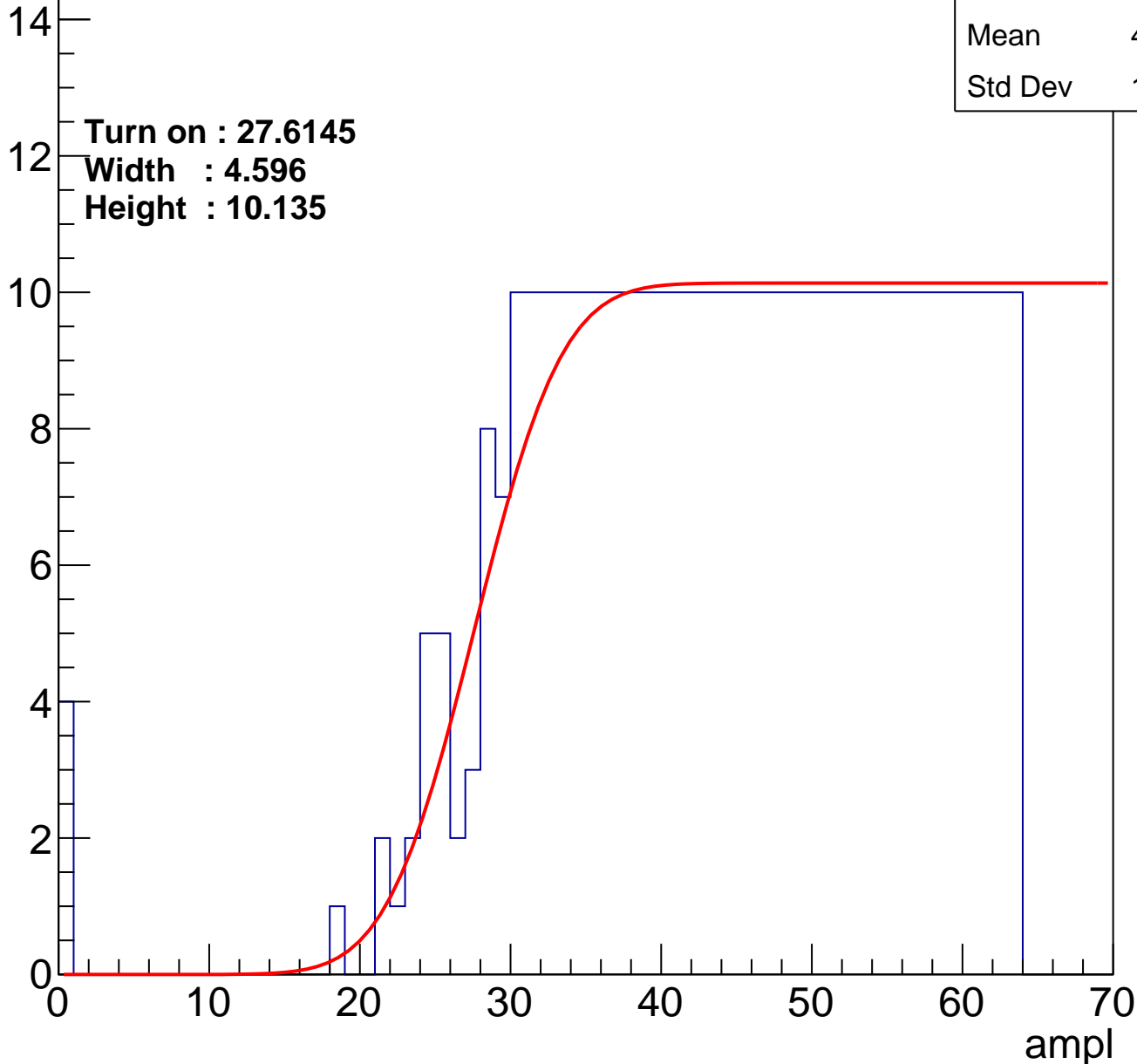
Entries	380
Mean	44.06
Std Dev	11.99

Turn on : 27.6145

Width : 4.596

Height : 10.135

Entry



# B1L100S, U7-ch32

calib\_packv5\_042523\_0143.root, FC#4, port A2

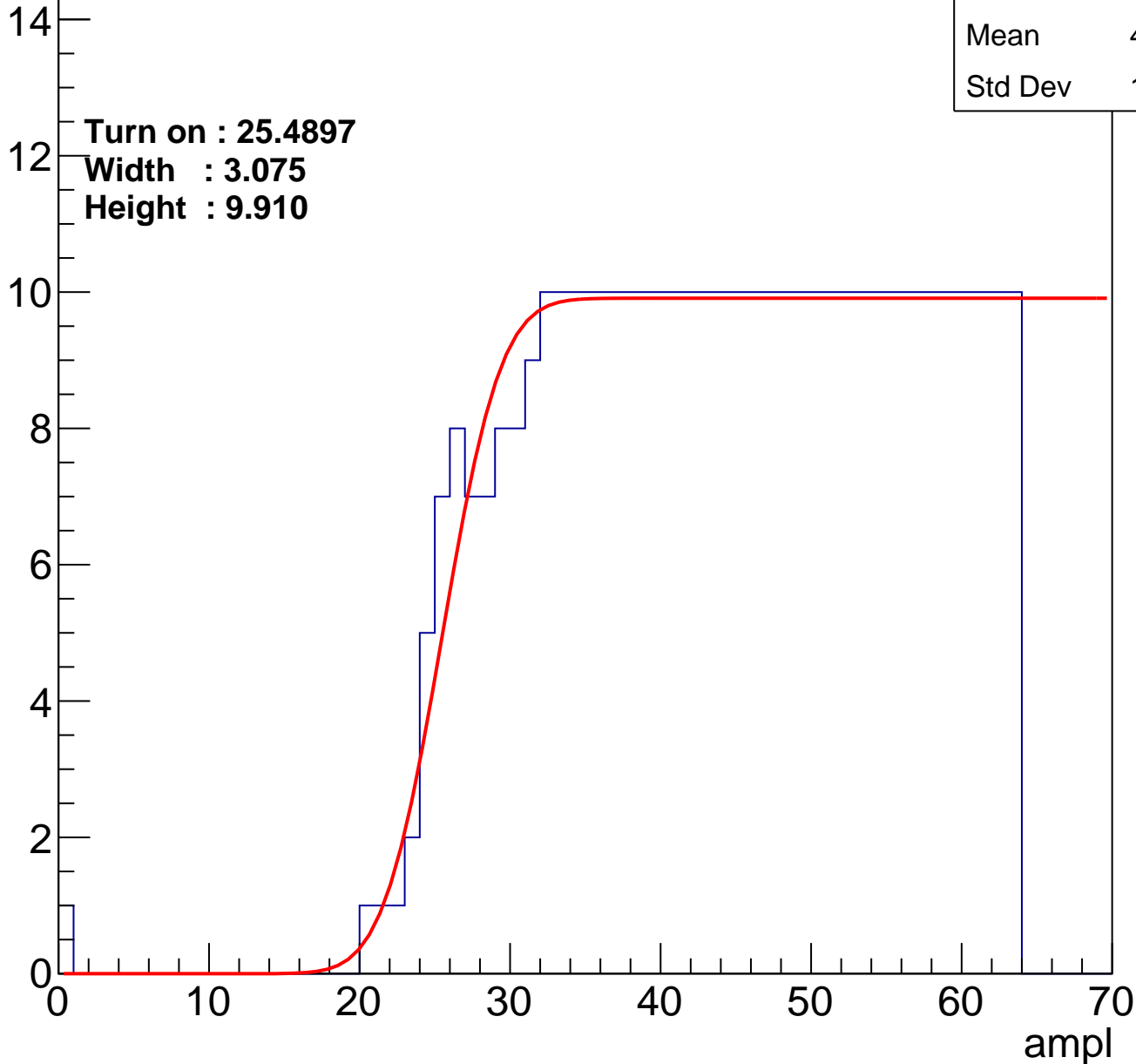
Entries	385
Mean	44.02
Std Dev	11.56

**Turn on : 25.4897**

**Width : 3.075**

**Height : 9.910**

Entry



# B1L100S, U7-ch33

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	390
Mean	43.79
Std Dev	11.73

Turn on : 25.3006

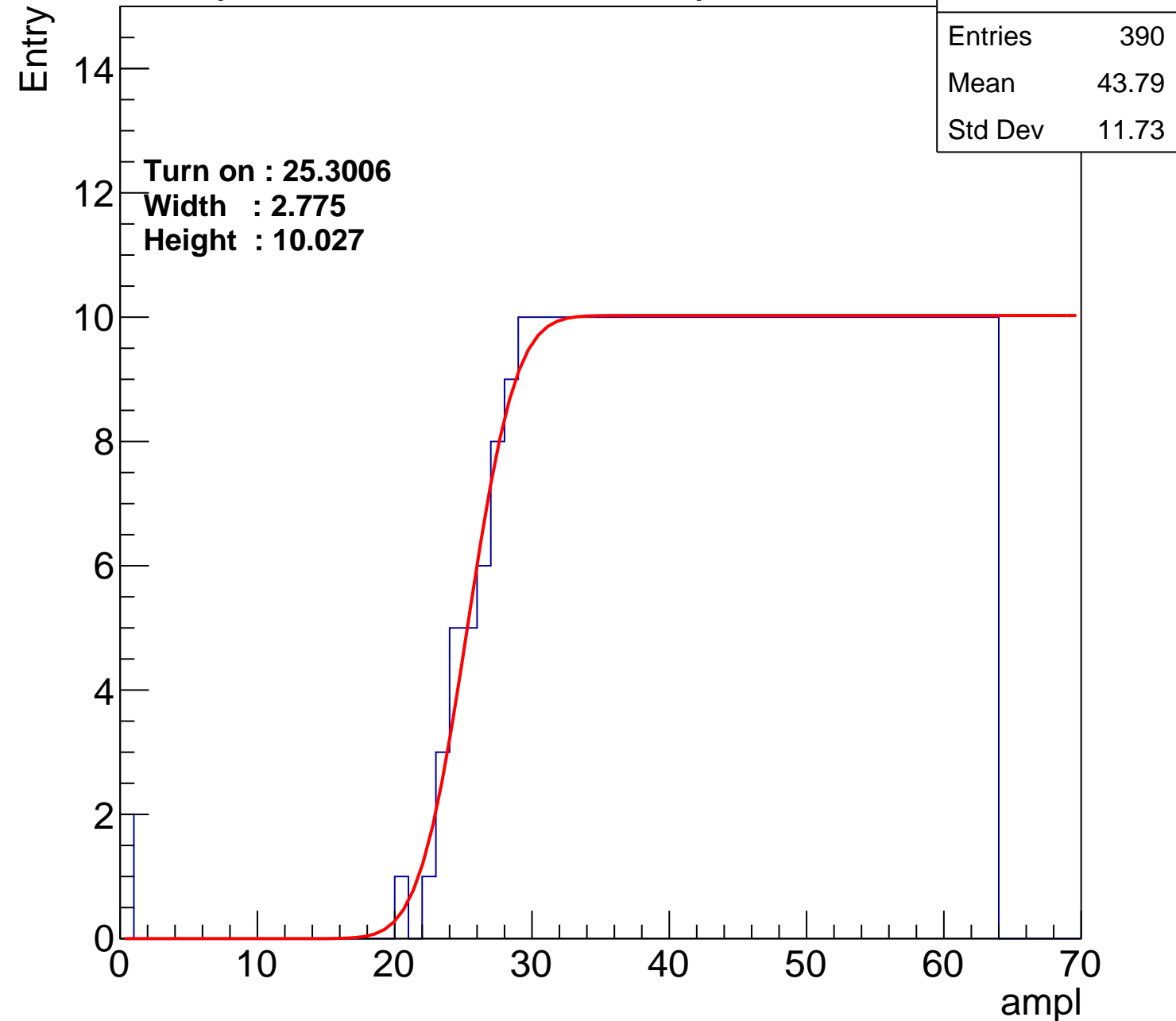
Width : 2.775

Height : 10.027

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch34

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	394
Mean	43.59
Std Dev	11.85

Turn on : 24.8089

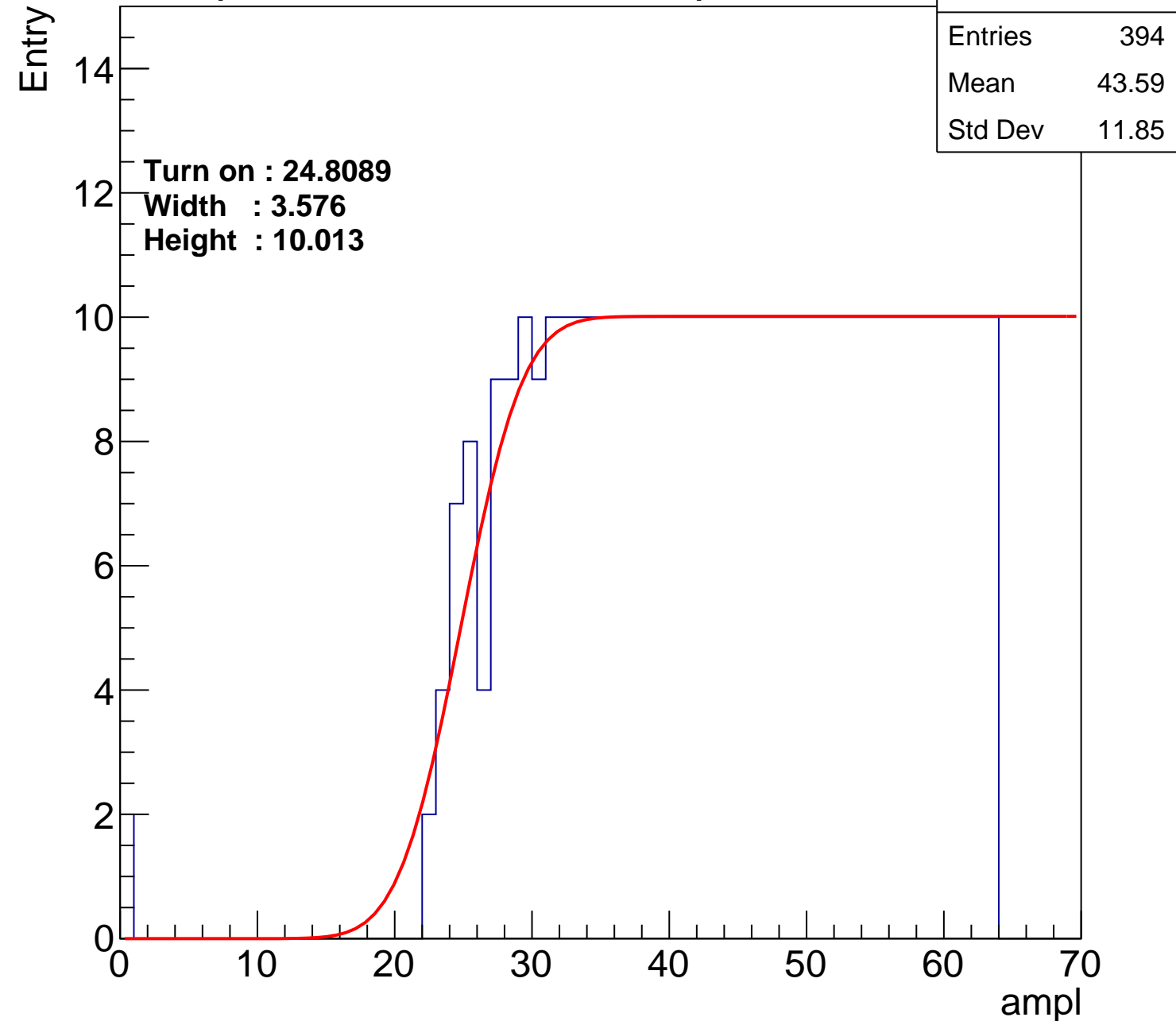
Width : 3.576

Height : 10.013

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch35

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	366
Mean	44.97
Std Dev	11.13

Turn on : 28.8226

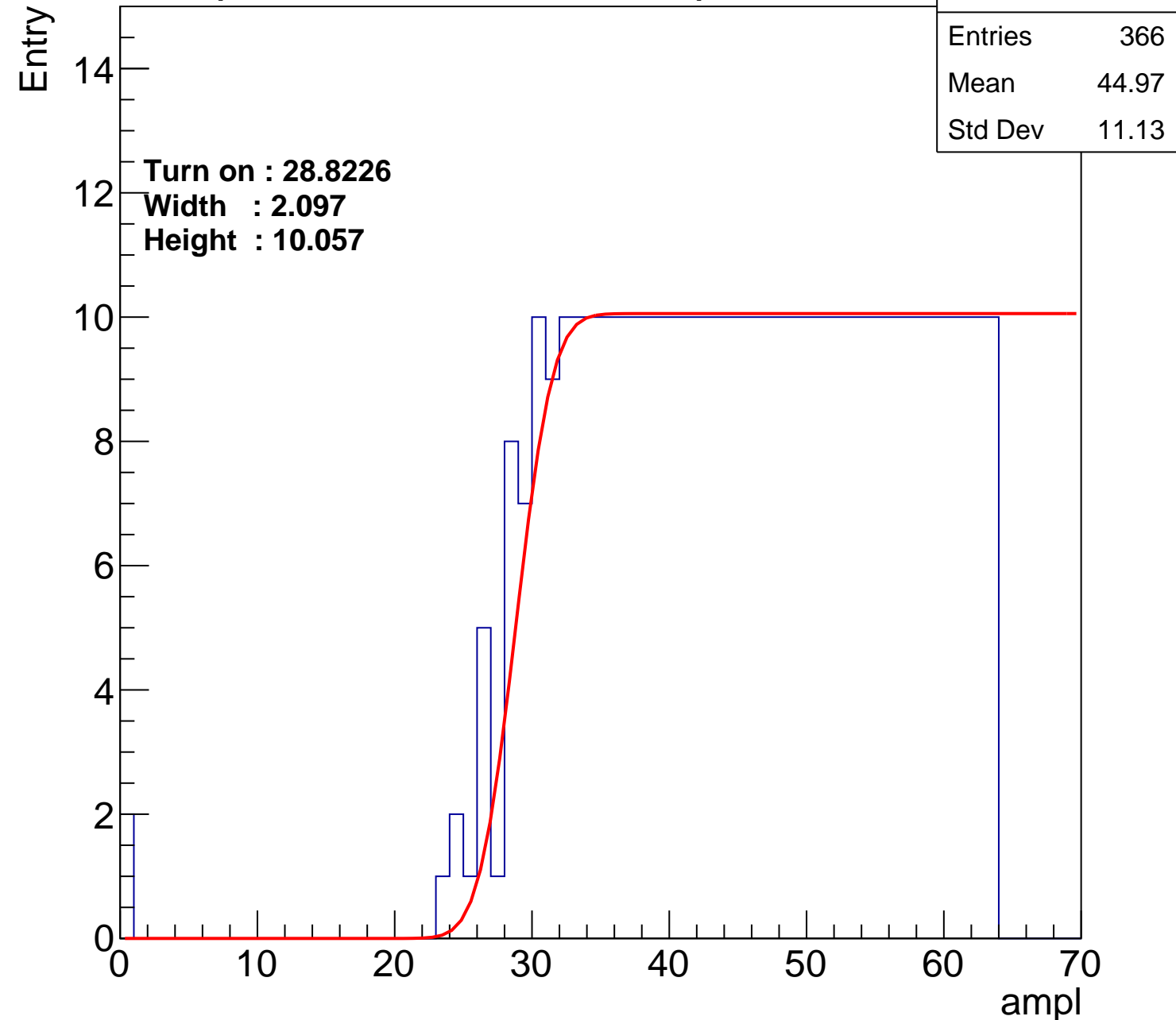
Width : 2.097

Height : 10.057

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch36

calib\_packv5\_042523\_0143.root, FC#4, port A2

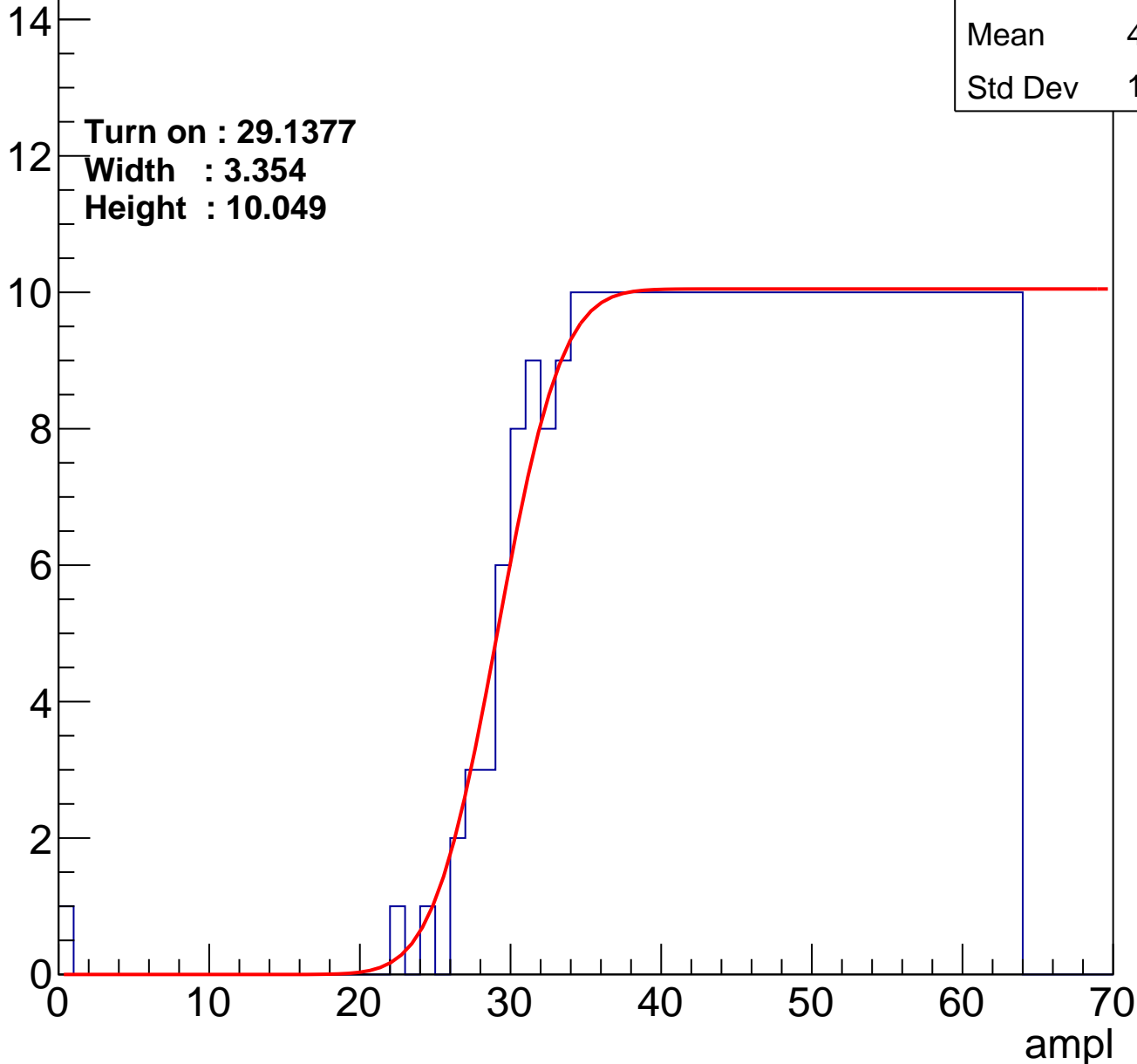
Entries	351
Mean	45.75
Std Dev	10.58

Turn on : 29.1377

Width : 3.354

Height : 10.049

Entry



# B1L100S, U7-ch37

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	367
Mean	45.03
Std Dev	10.89

**Turn on : 28.0989**

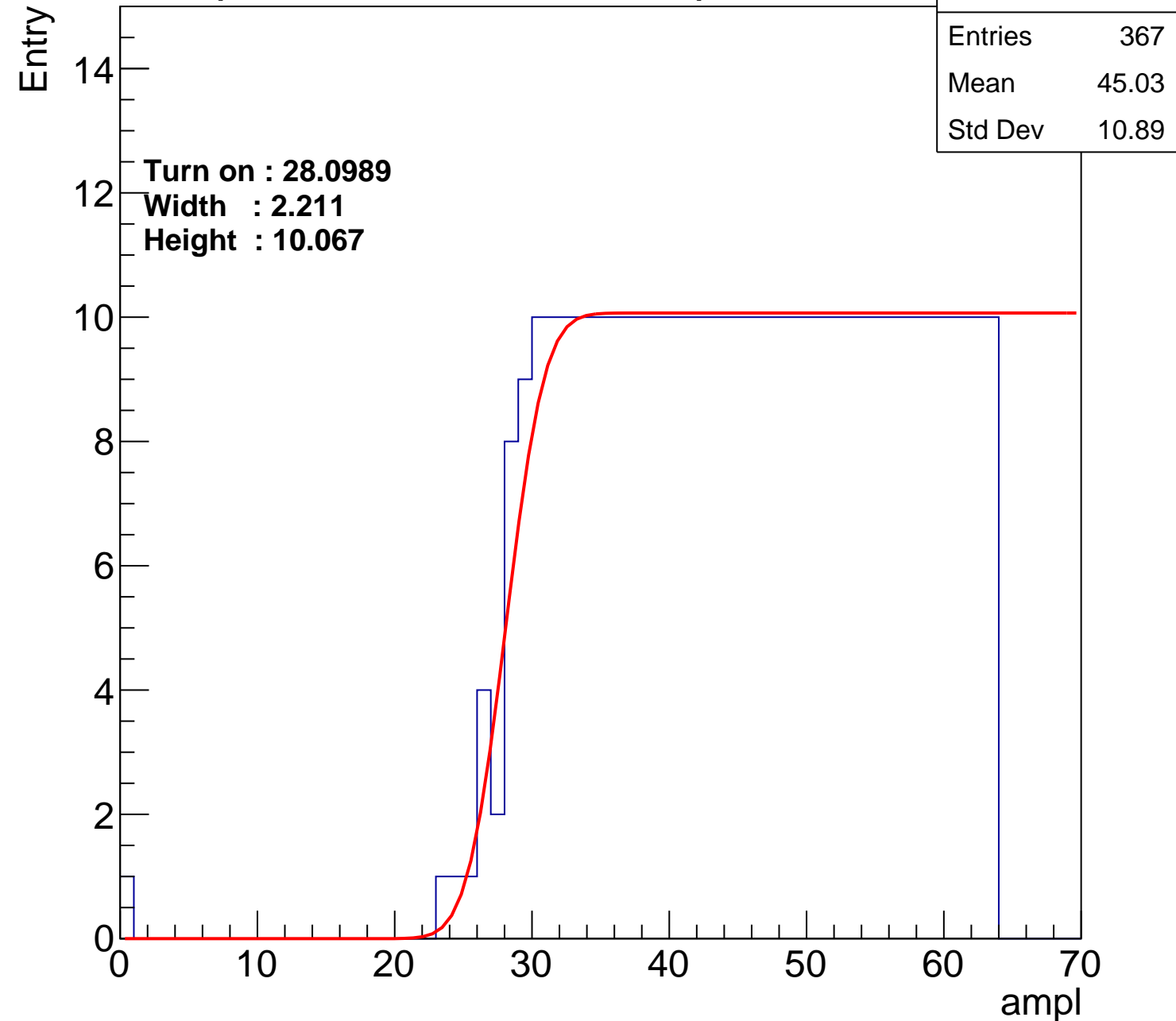
**Width : 2.211**

**Height : 10.067**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch38

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	362
Mean	45.15
Std Dev	11.06

**Turn on : 28.2908**

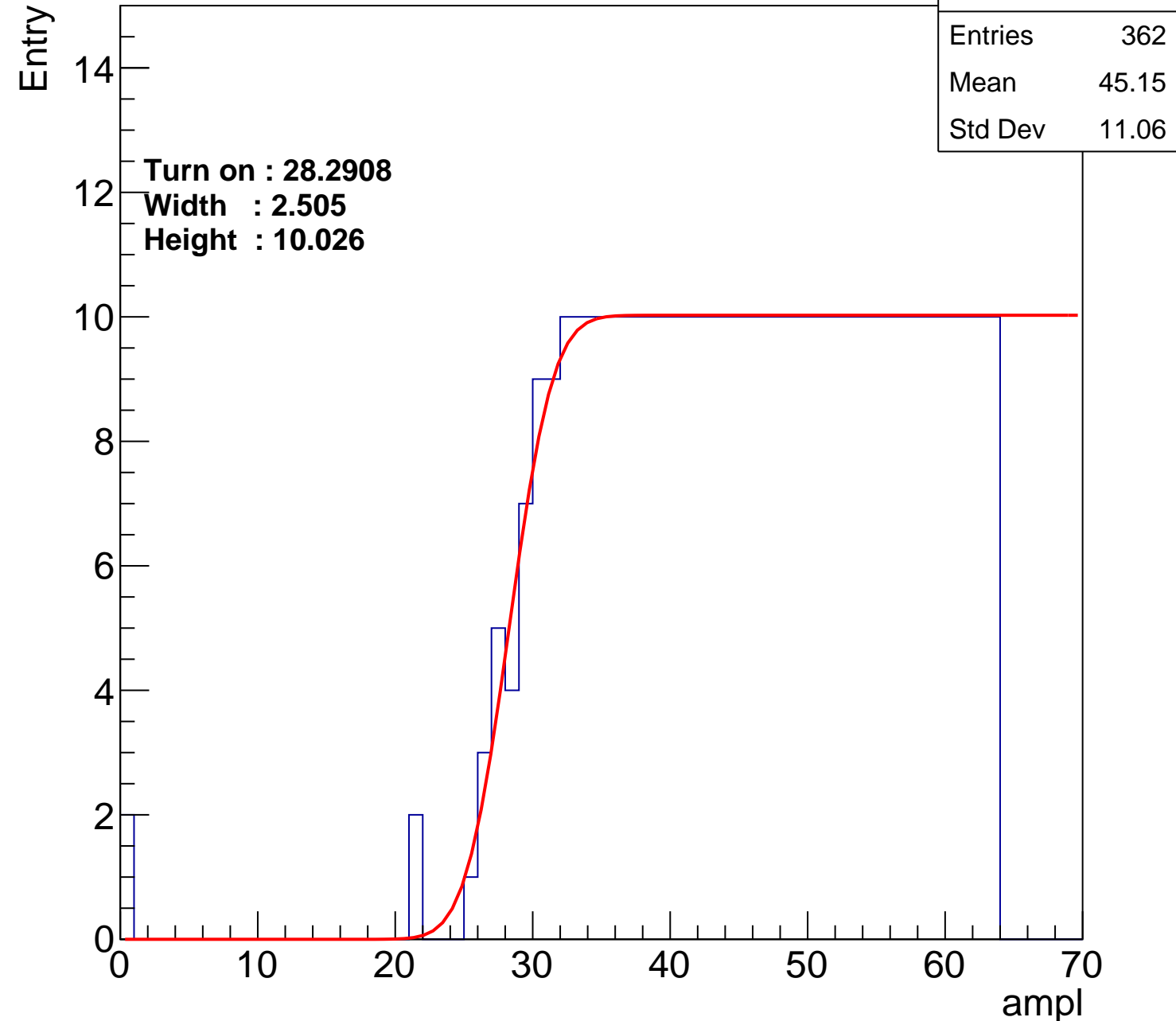
**Width : 2.505**

**Height : 10.026**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L100S, U7-ch39

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	393
Mean	43.69
Std Dev	11.67

Turn on : 24.7632

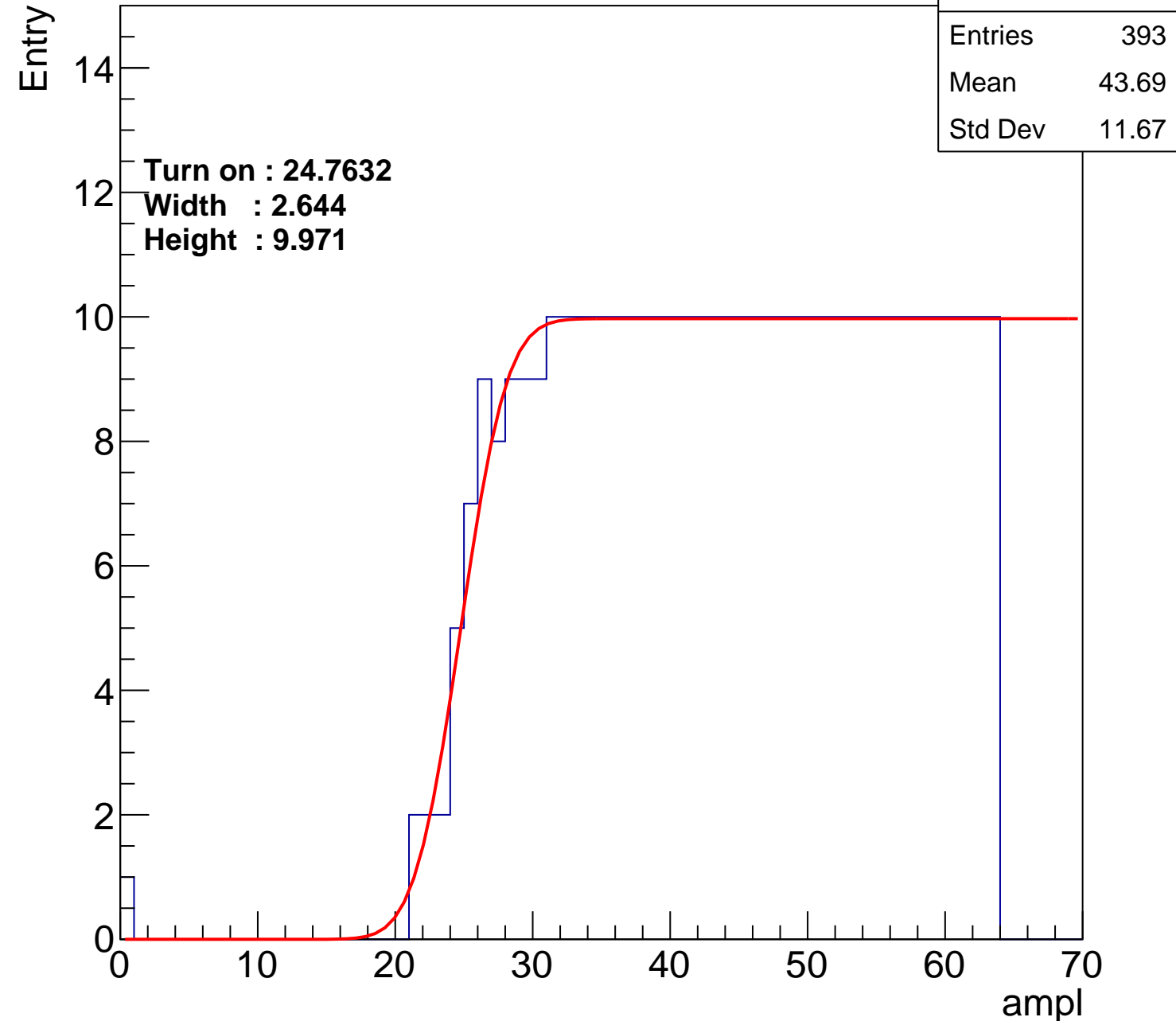
Width : 2.644

Height : 9.971

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch40

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	377
Mean	44.47
Std Dev	11.27

Turn on : 26.9769

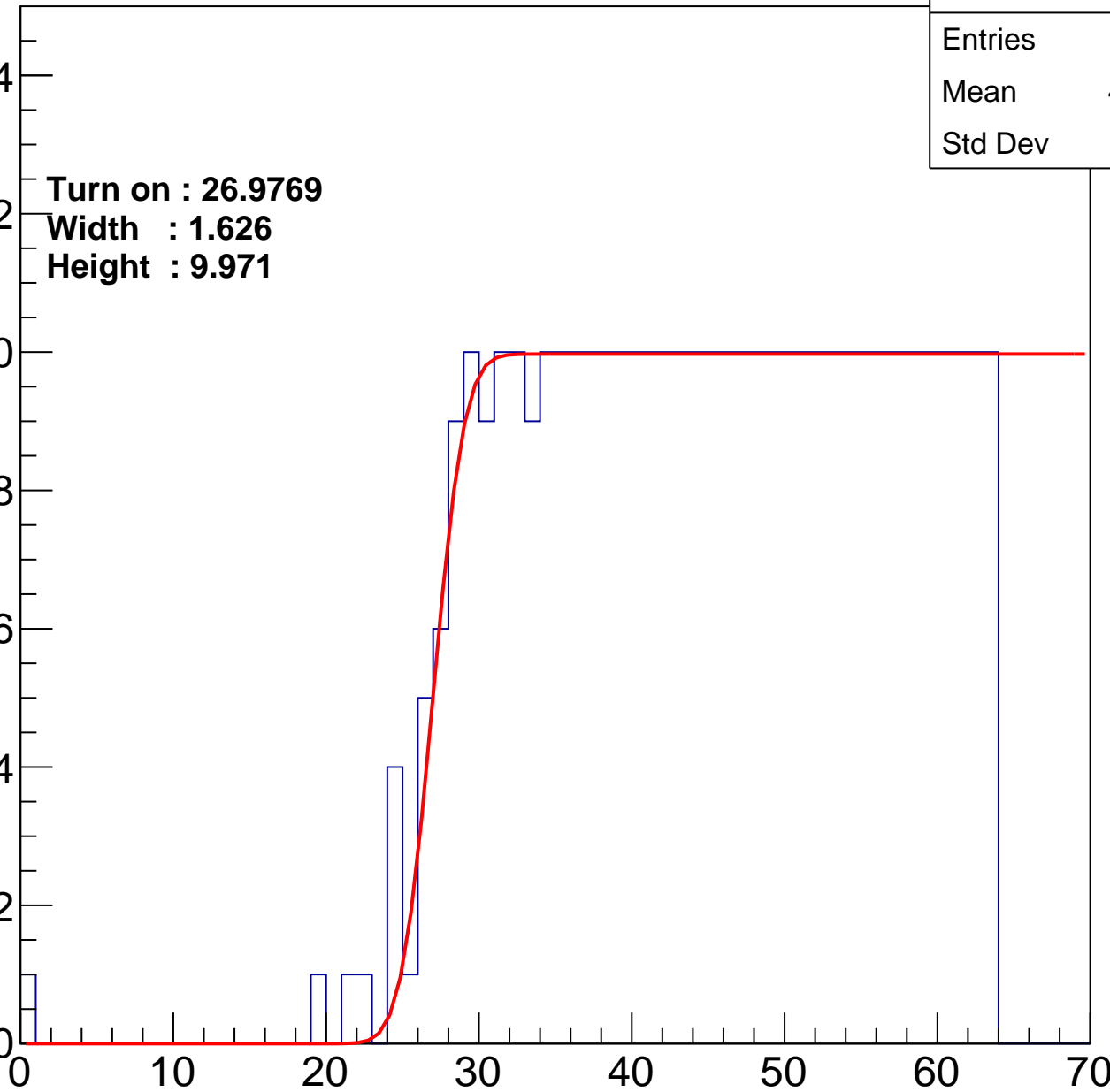
Width : 1.626

Height : 9.971

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch41

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	395
Mean	43.63
Std Dev	11.67

Turn on : 24.8890

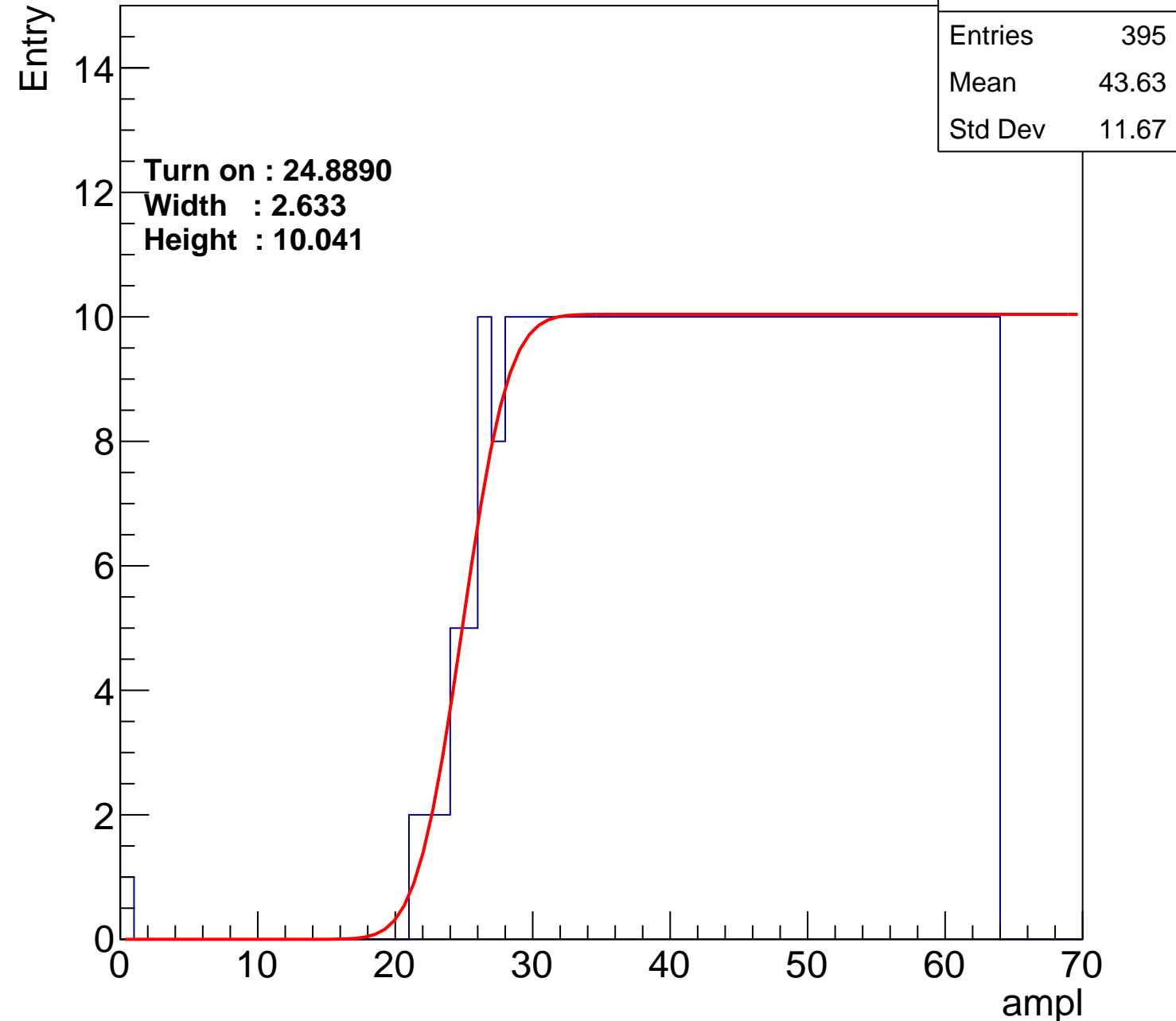
Width : 2.633

Height : 10.041

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch42

calib\_packv5\_042523\_0143.root, FC#4, port A2

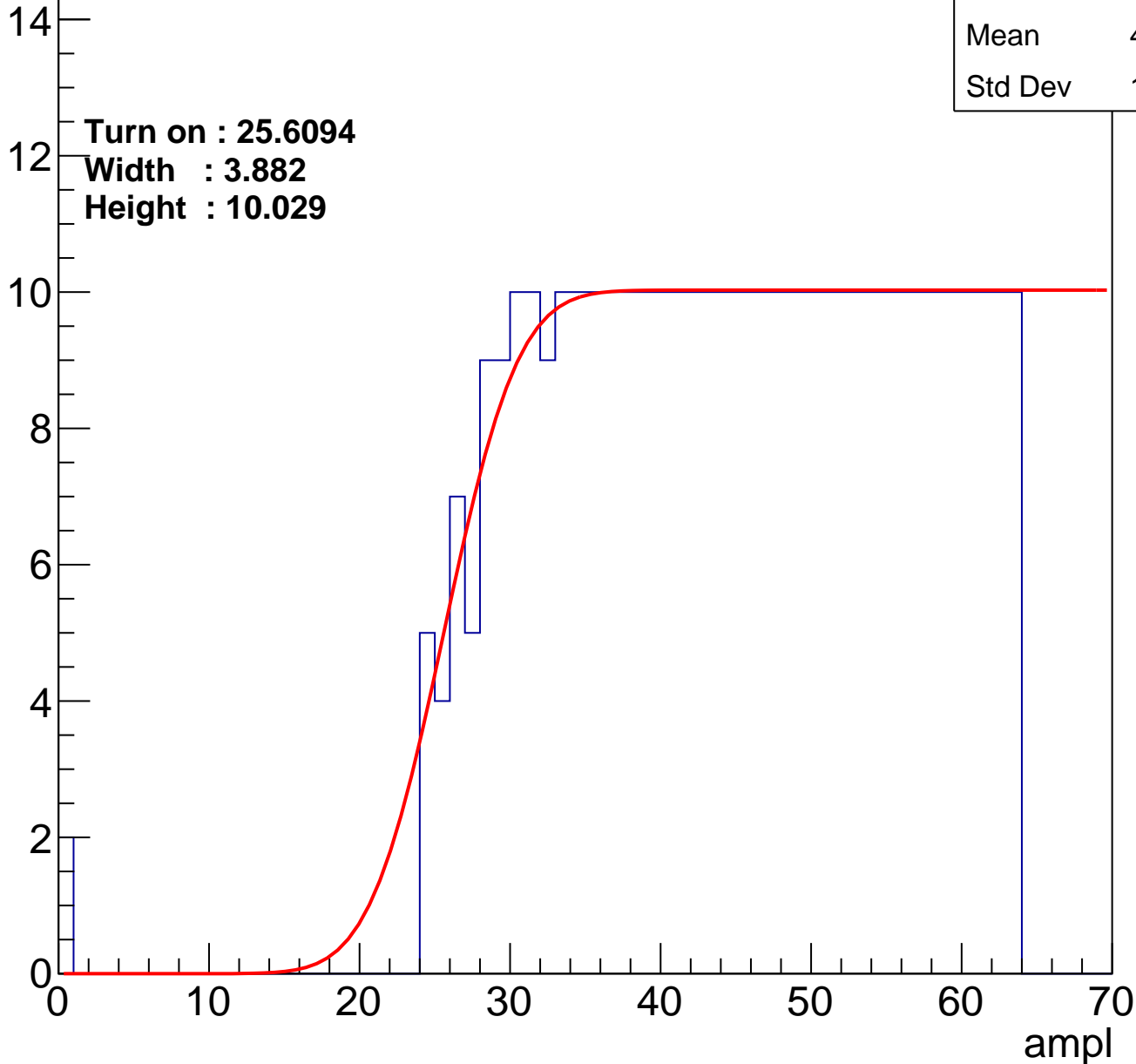
Entries	380
Mean	44.28
Std Dev	11.47

Turn on : 25.6094

Width : 3.882

Height : 10.029

Entry



# B1L100S, U7-ch43

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	348
Mean	45.77
Std Dev	10.92

Turn on : 30.0635

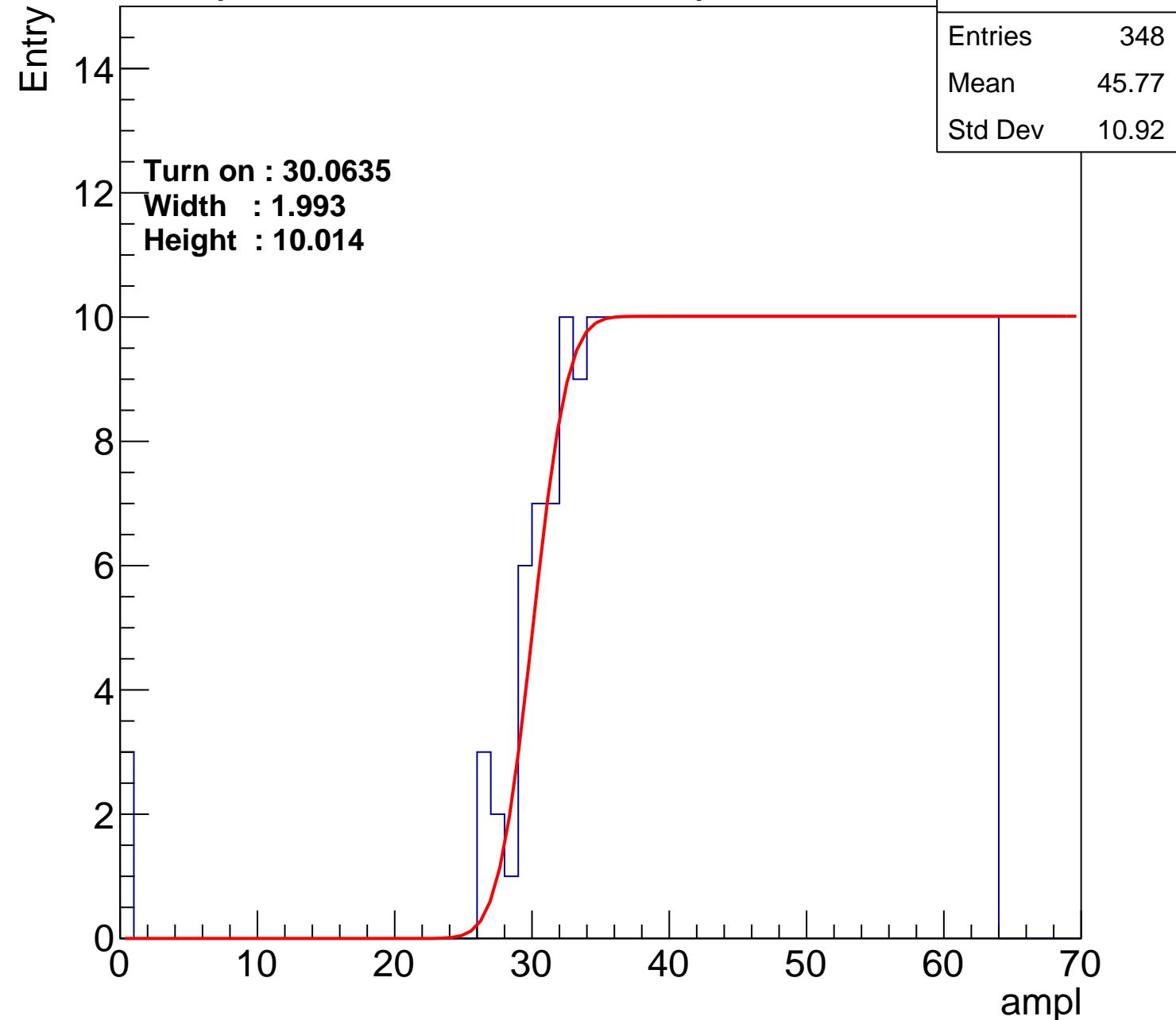
Width : 1.993

Height : 10.014

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch44

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	382
Mean	44.27
Std Dev	11.32

**Turn on : 26.1301**

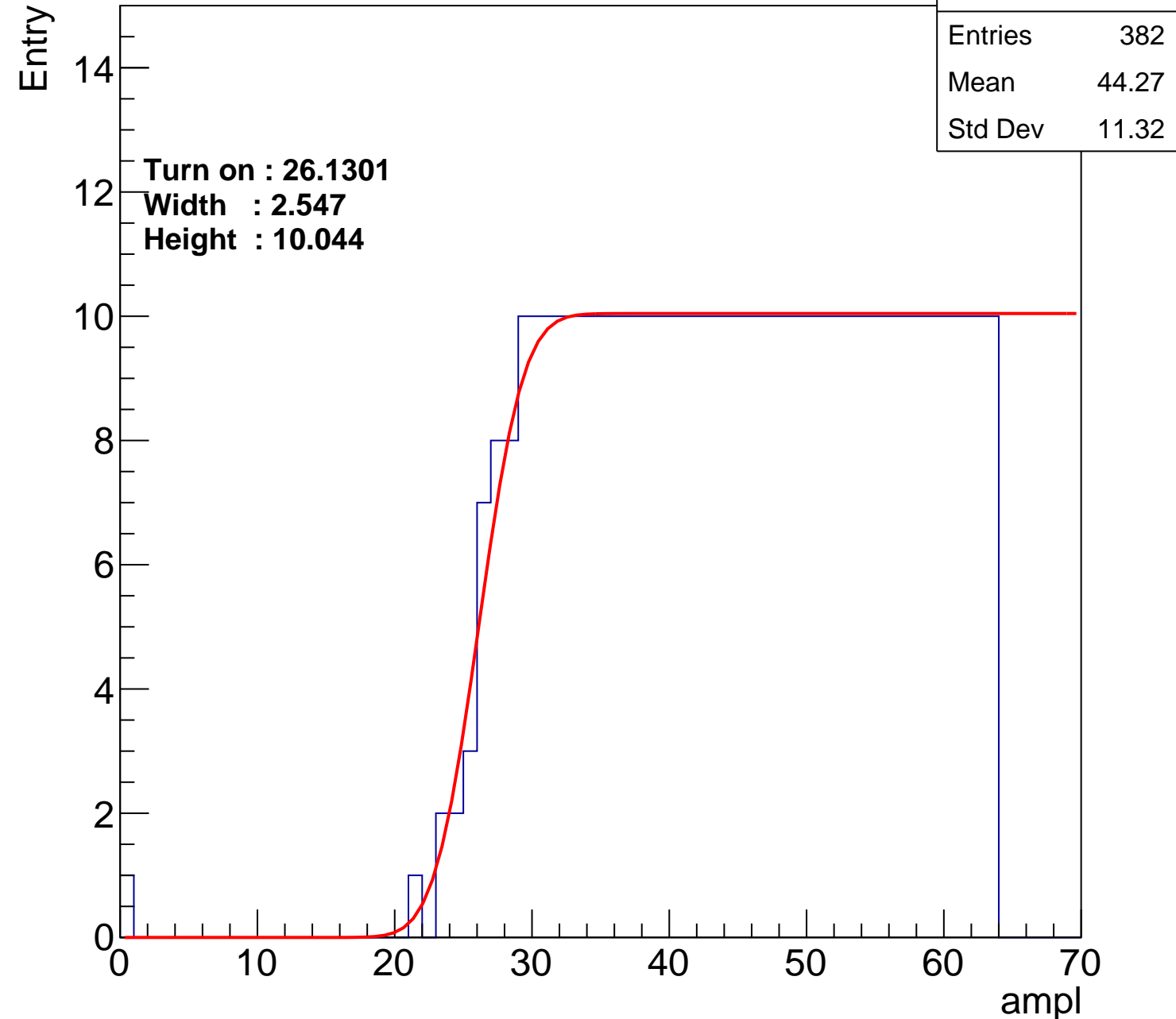
**Width : 2.547**

**Height : 10.044**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch45

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	373
Mean	44.69
Std Dev	11.11

Turn on : 26.9132

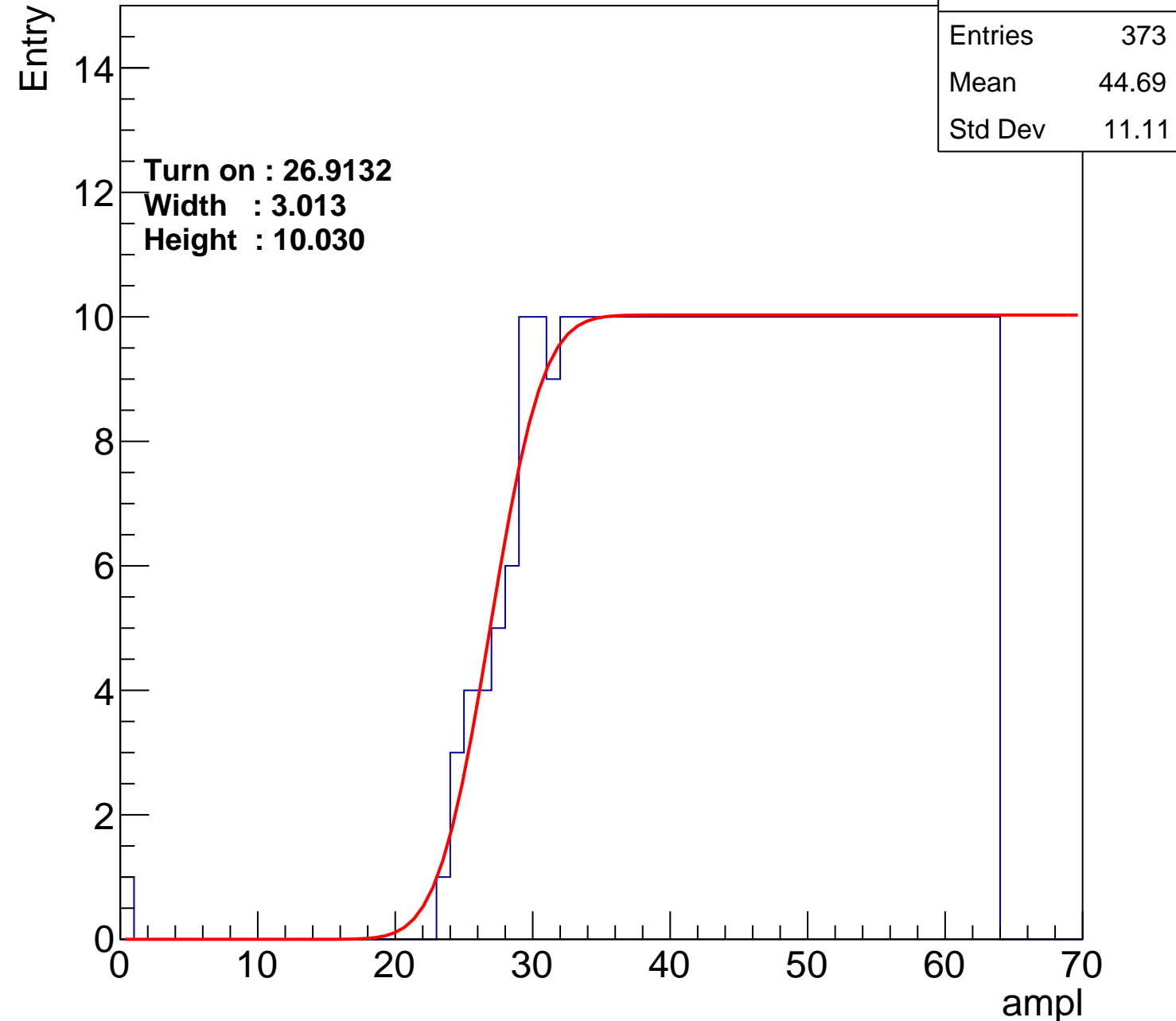
Width : 3.013

Height : 10.030

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch46

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	391
Mean	43.79
Std Dev	11.69

Turn on : 25.1470

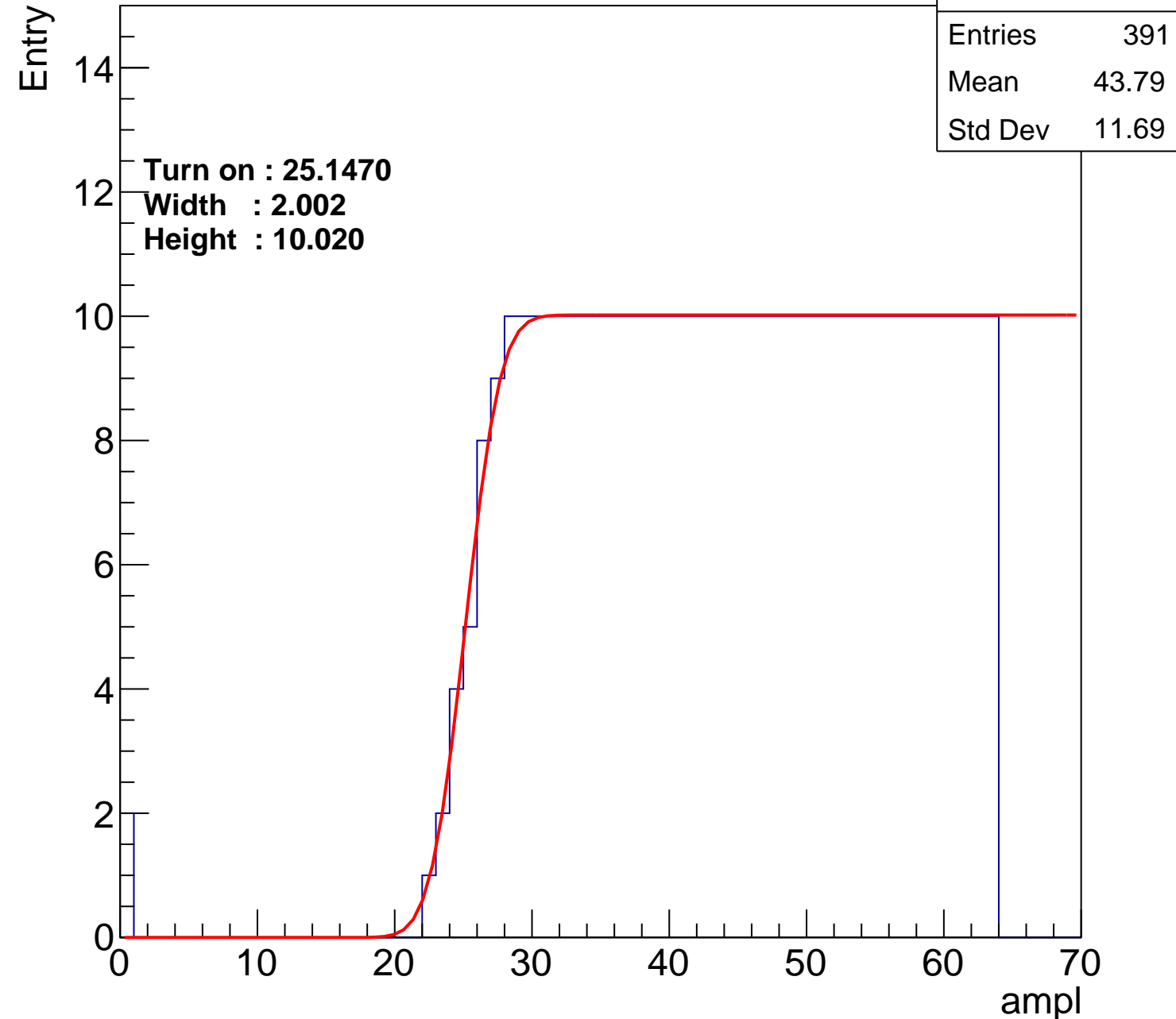
Width : 2.002

Height : 10.020

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L100S, U7-ch47

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	395
Mean	43.53
Std Dev	11.89

Turn on : 23.5465

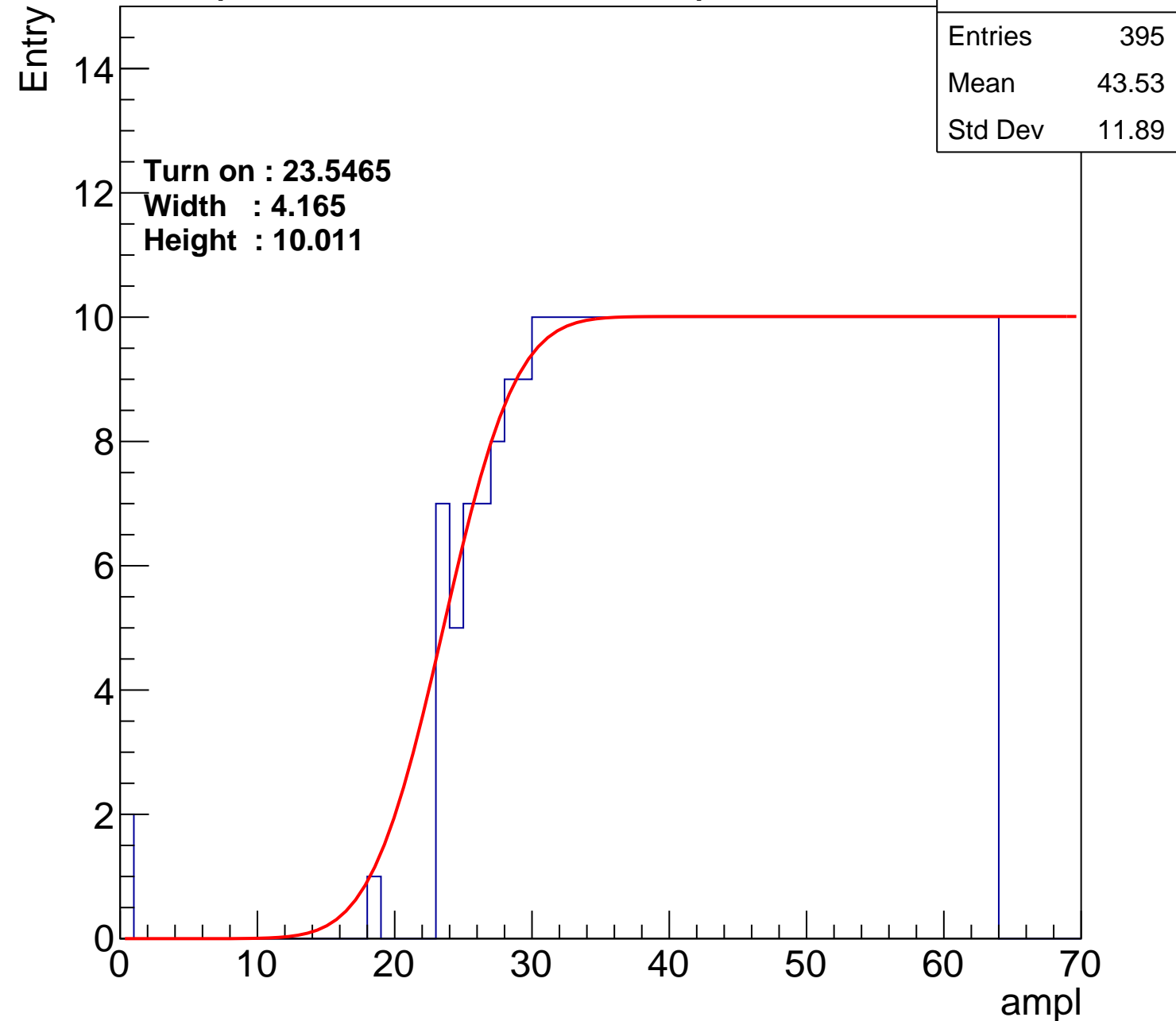
Width : 4.165

Height : 10.011

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch48

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	374
Mean	44.61
Std Dev	11.18

Turn on : 26.4113

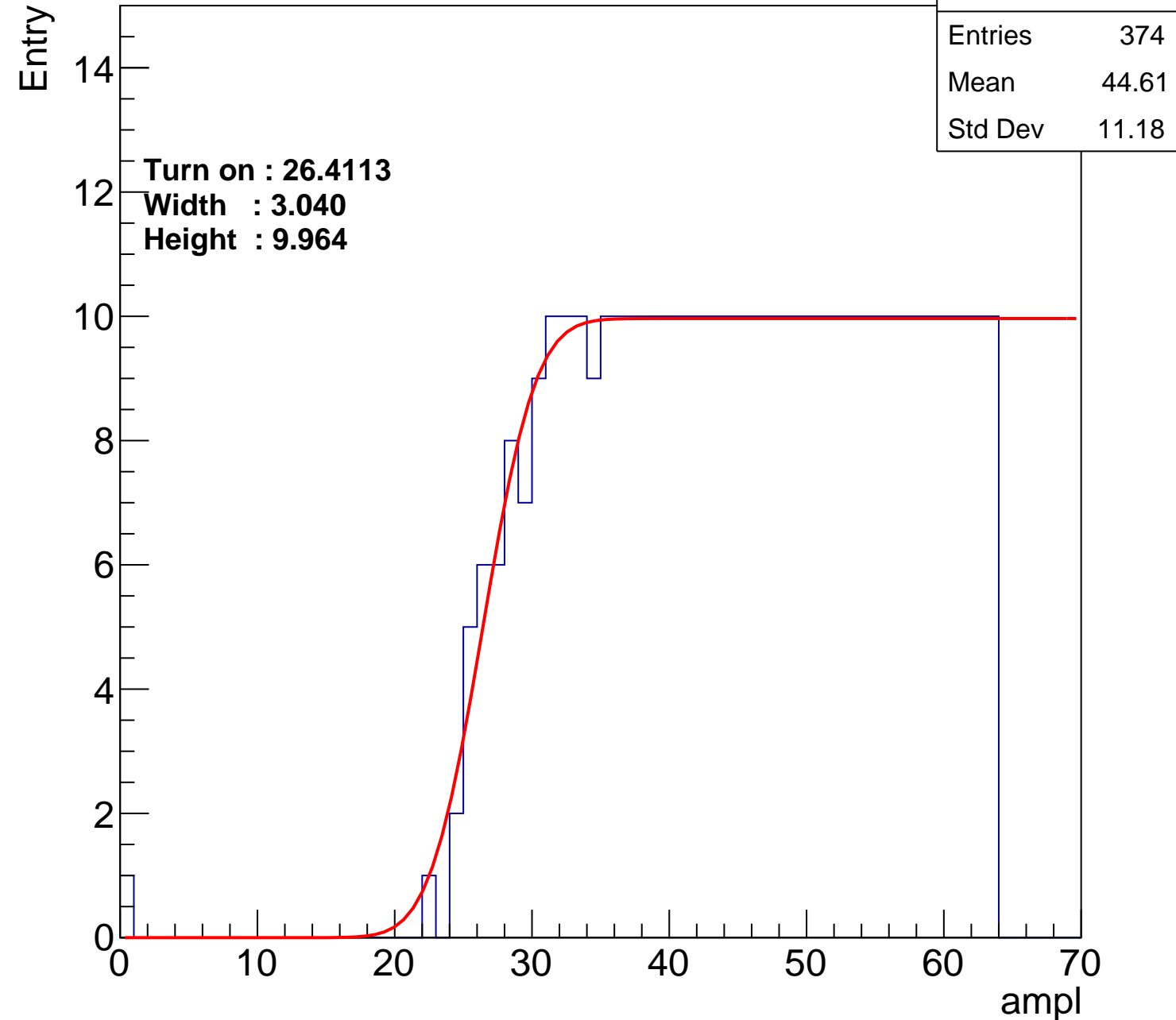
Width : 3.040

Height : 9.964

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch49

calib\_packv5\_042523\_0143.root, FC#4, port A2

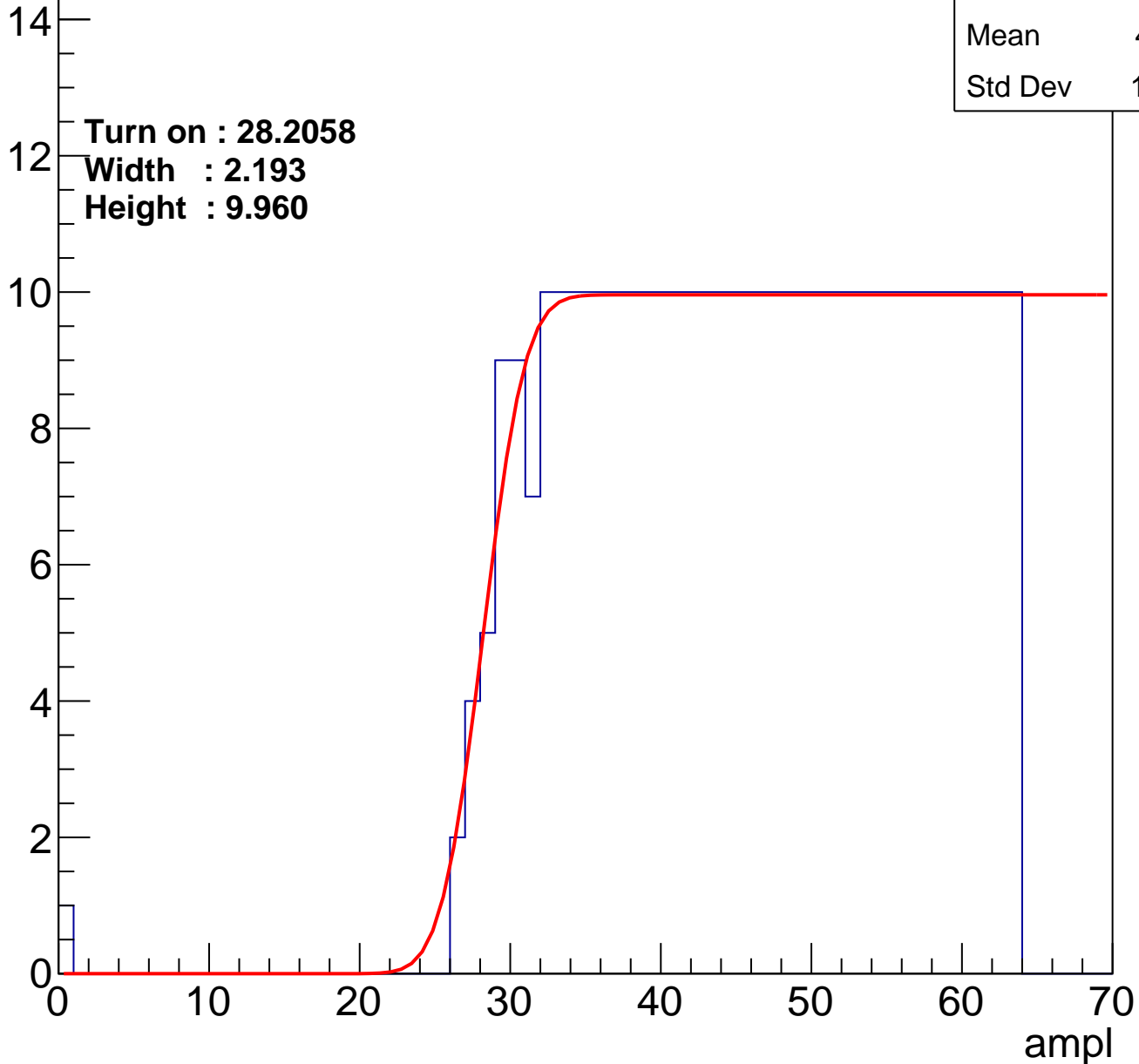
Entries	357
Mean	45.51
Std Dev	10.63

**Turn on : 28.2058**

**Width : 2.193**

**Height : 9.960**

Entry



# B1L100S, U7-ch50

calib\_packv5\_042523\_0143.root, FC#4, port A2

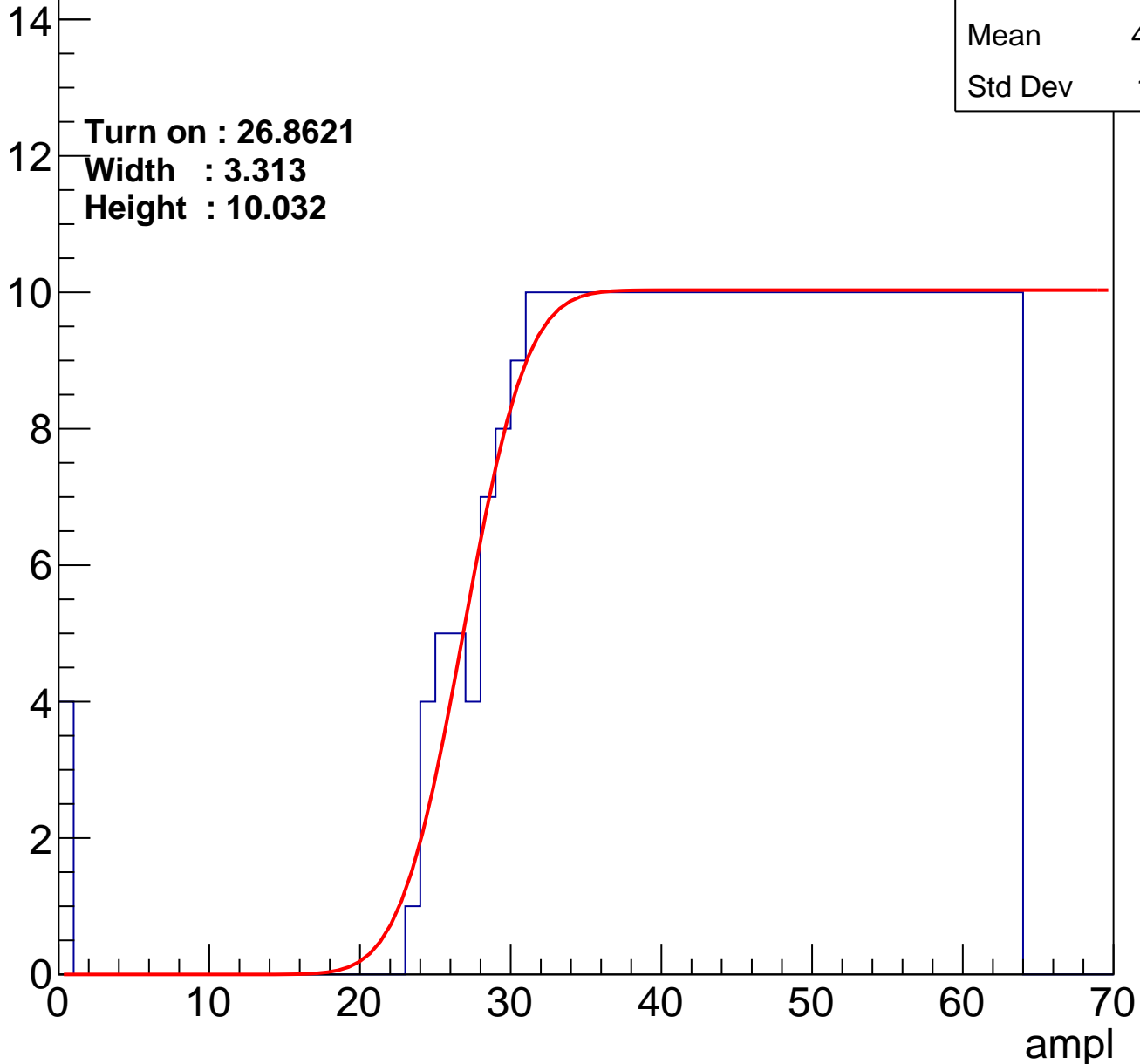
Entries	377
Mean	44.27
Std Dev	11.81

Turn on : 26.8621

Width : 3.313

Height : 10.032

Entry



# B1L100S, U7-ch51

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	383
Mean	44.09
Std Dev	11.7

**Turn on : 26.0246**

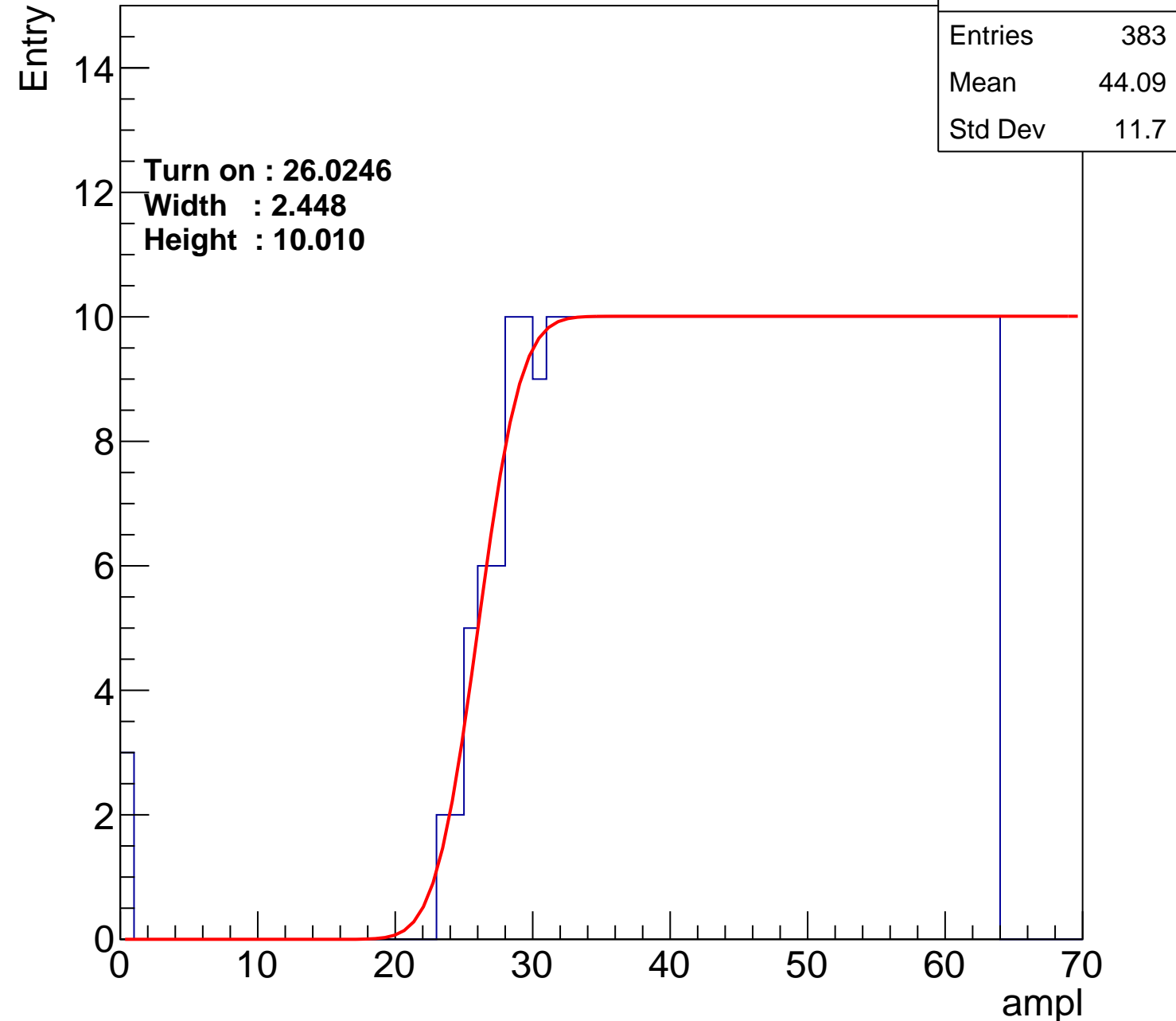
**Width : 2.448**

**Height : 10.010**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch52

calib\_packv5\_042523\_0143.root, FC#4, port A2

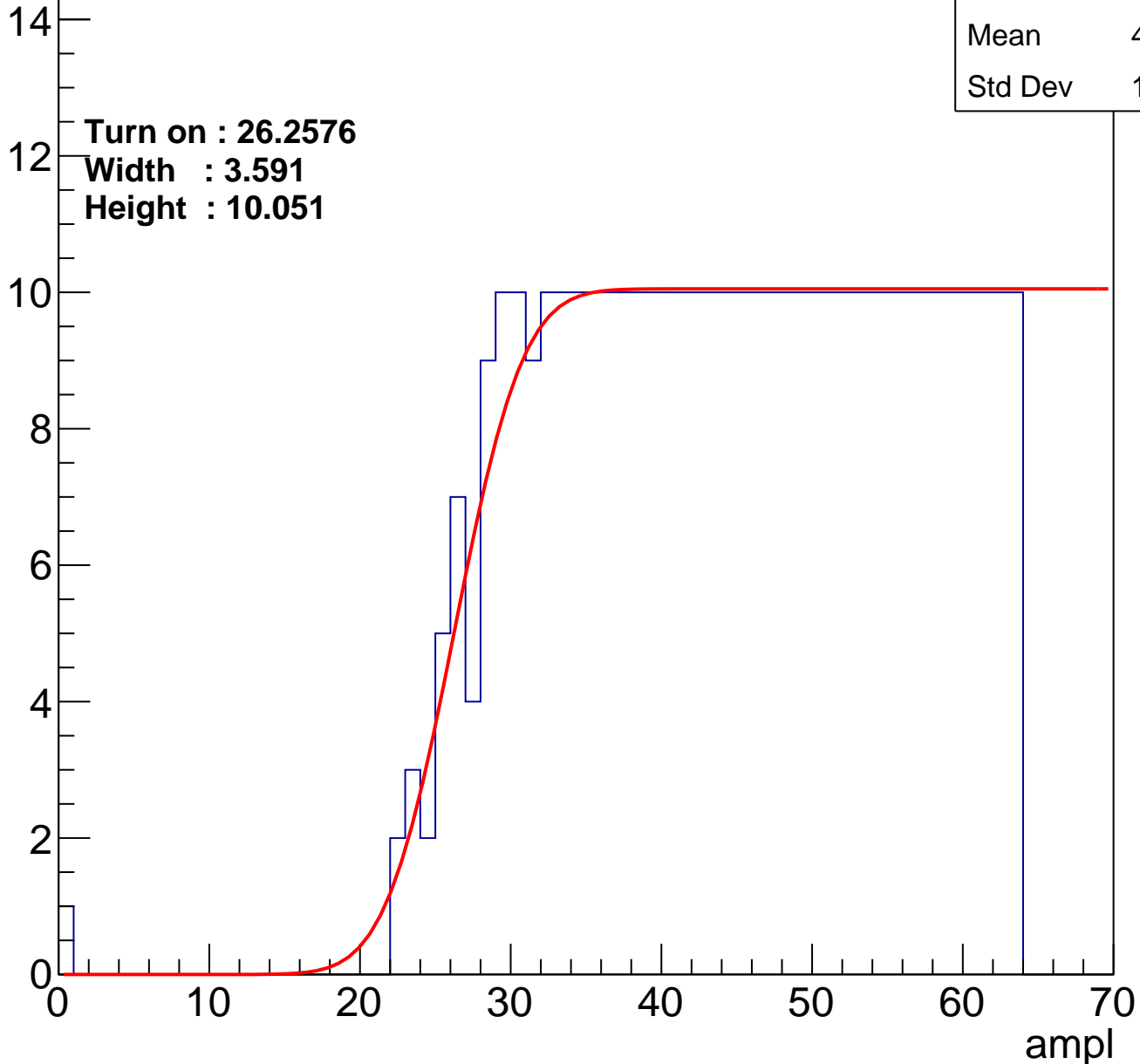
Entries	382
Mean	44.23
Std Dev	11.38

Turn on : 26.2576

Width : 3.591

Height : 10.051

Entry



# B1L100S, U7-ch53

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	381
Mean	44.23
Std Dev	11.5

**Turn on : 26.1523**

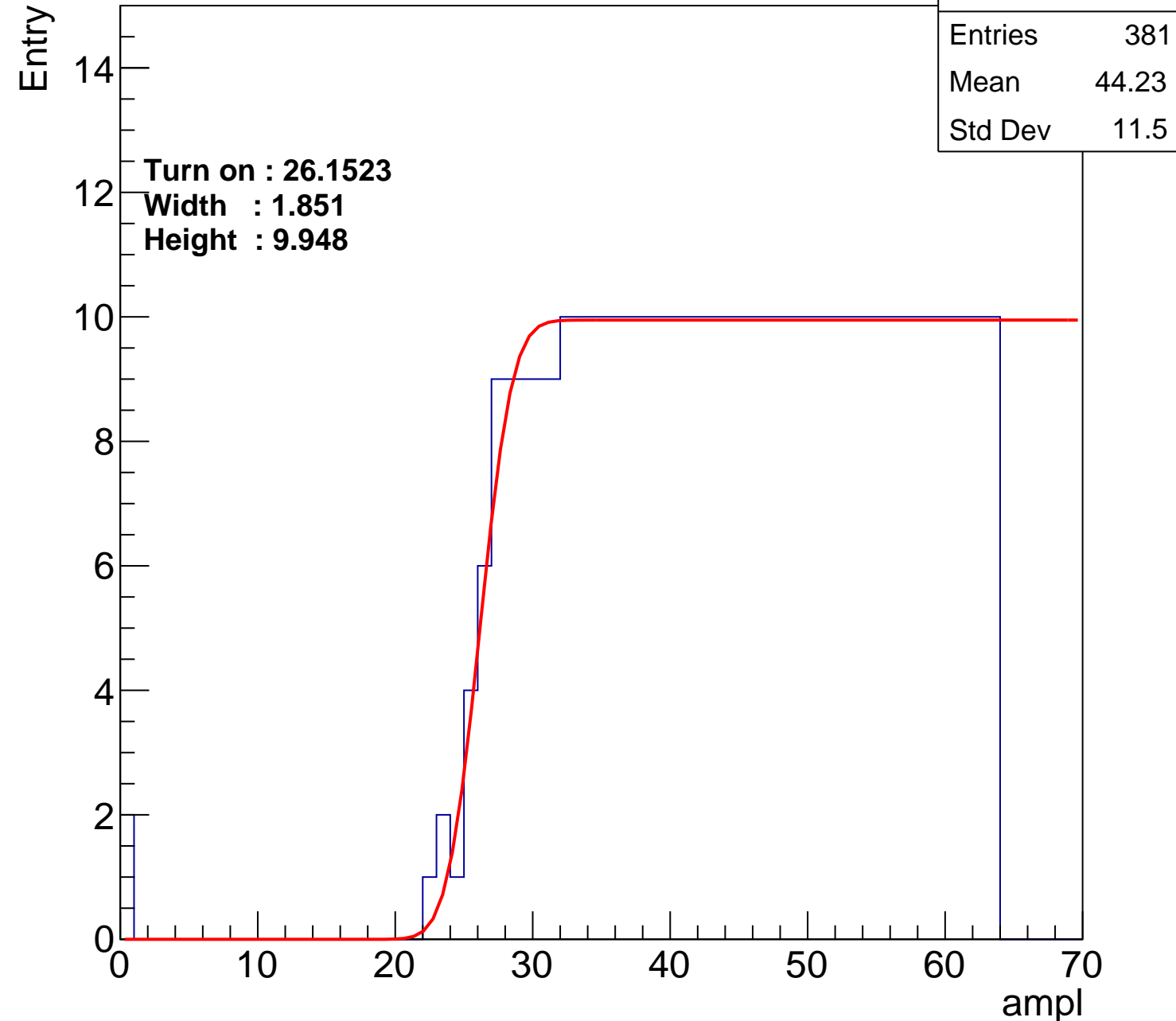
**Width : 1.851**

**Height : 9.948**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch54

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	370
Mean	44.74
Std Dev	11.28

Turn on : 27.0982

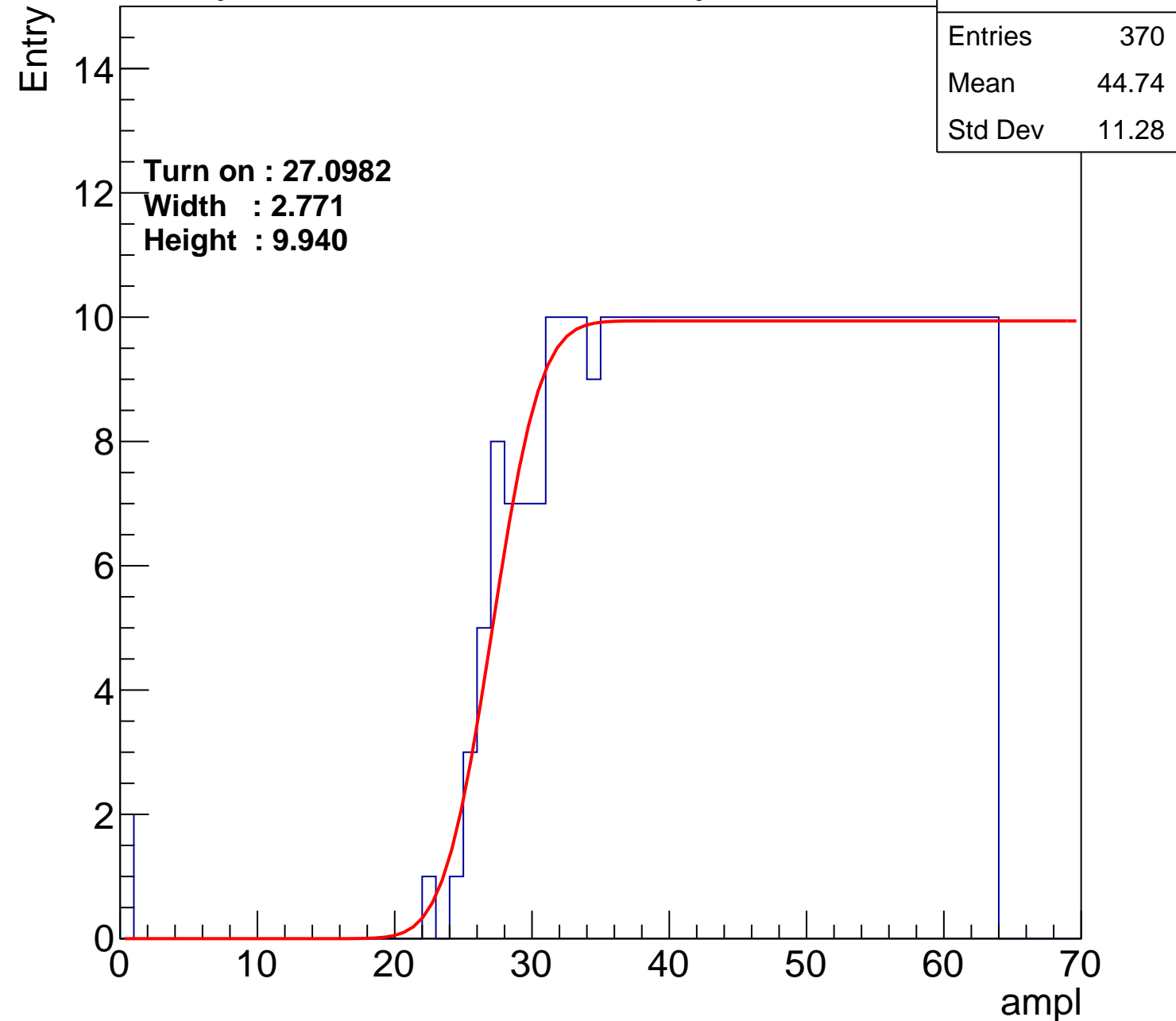
Width : 2.771

Height : 9.940

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L100S, U7-ch55

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	360
Mean	45.37
Std Dev	10.71

Turn on : 28.1625

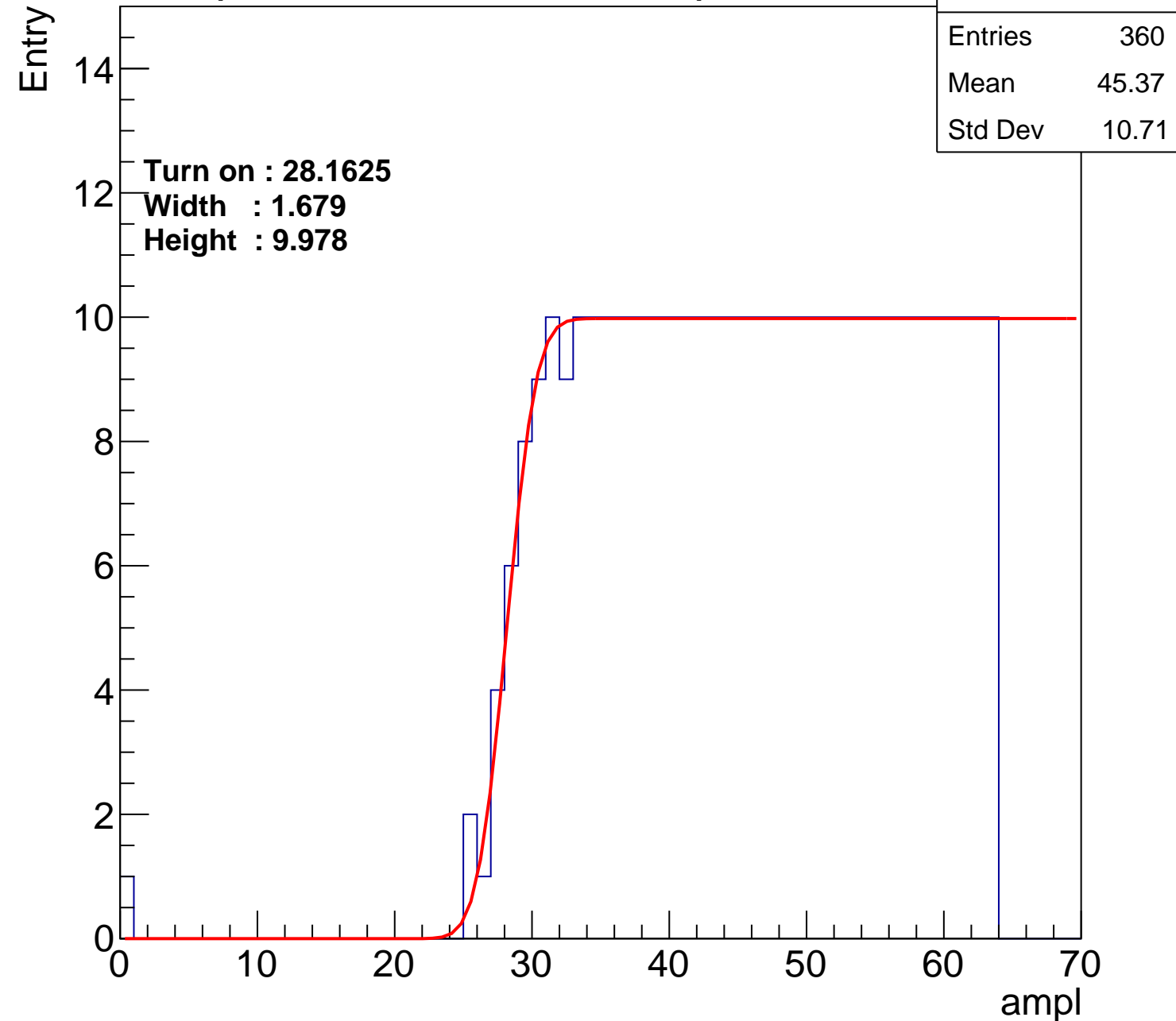
Width : 1.679

Height : 9.978

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch56

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	381
Mean	44.14
Std Dev	11.74

Turn on : 26.3781

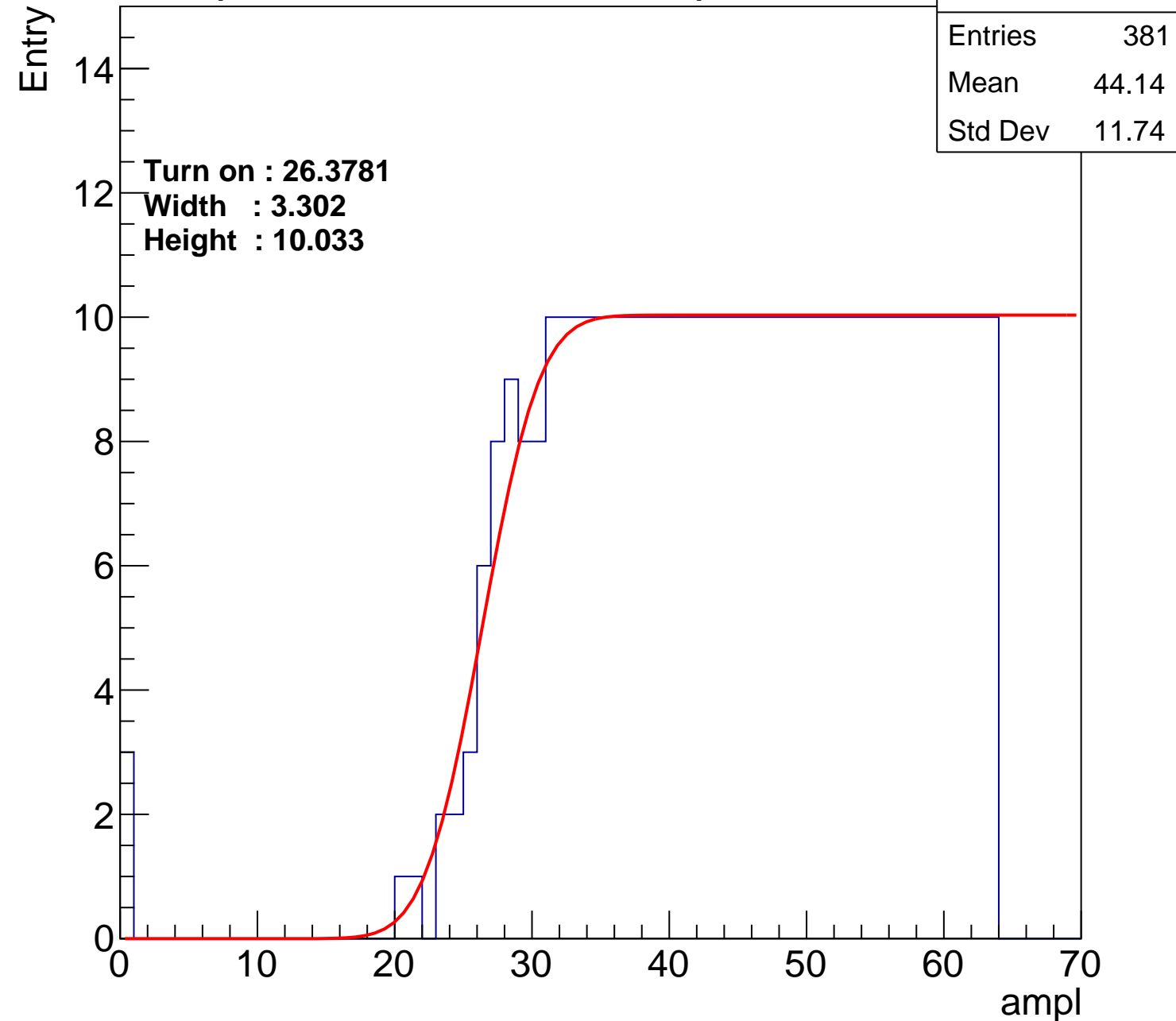
Width : 3.302

Height : 10.033

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch57

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	382
Mean	44.15
Std Dev	11.59

**Turn on : 26.6008**

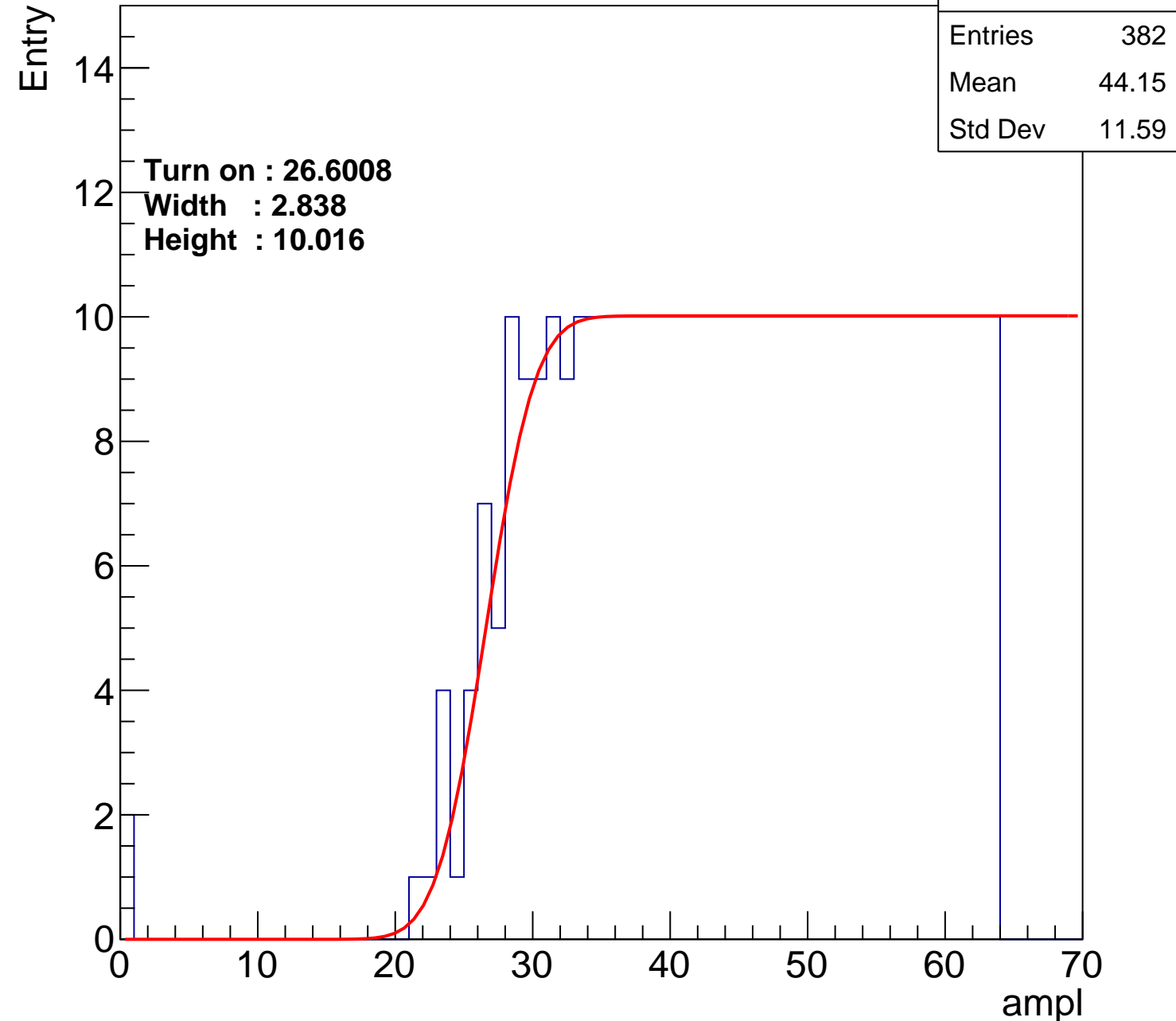
**Width : 2.838**

**Height : 10.016**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch58

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	388
Mean	43.86
Std Dev	11.74

Turn on : 25.8212

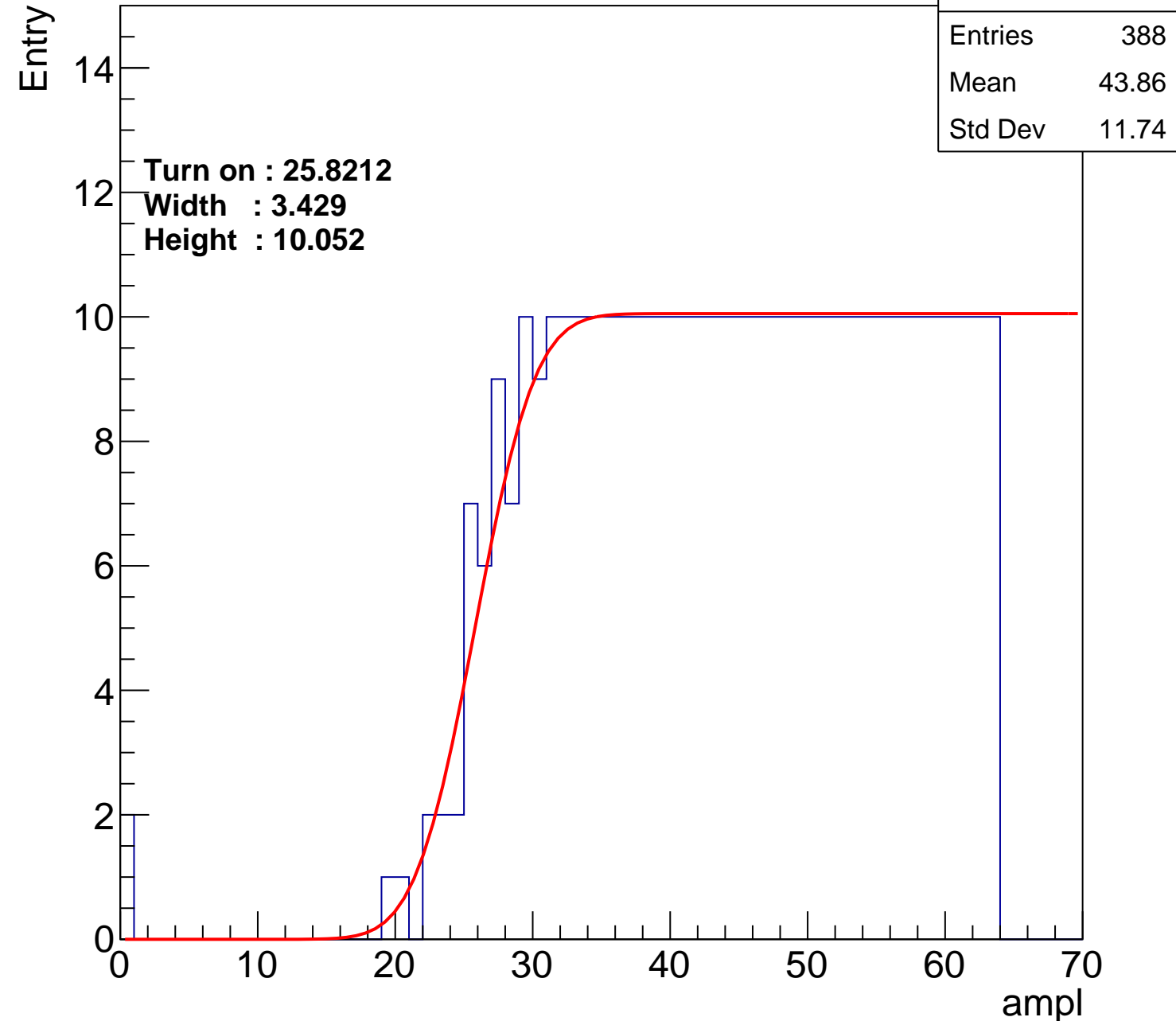
Width : 3.429

Height : 10.052

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch59

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	386
Mean	43.81
Std Dev	12.12

Turn on : 26.1014

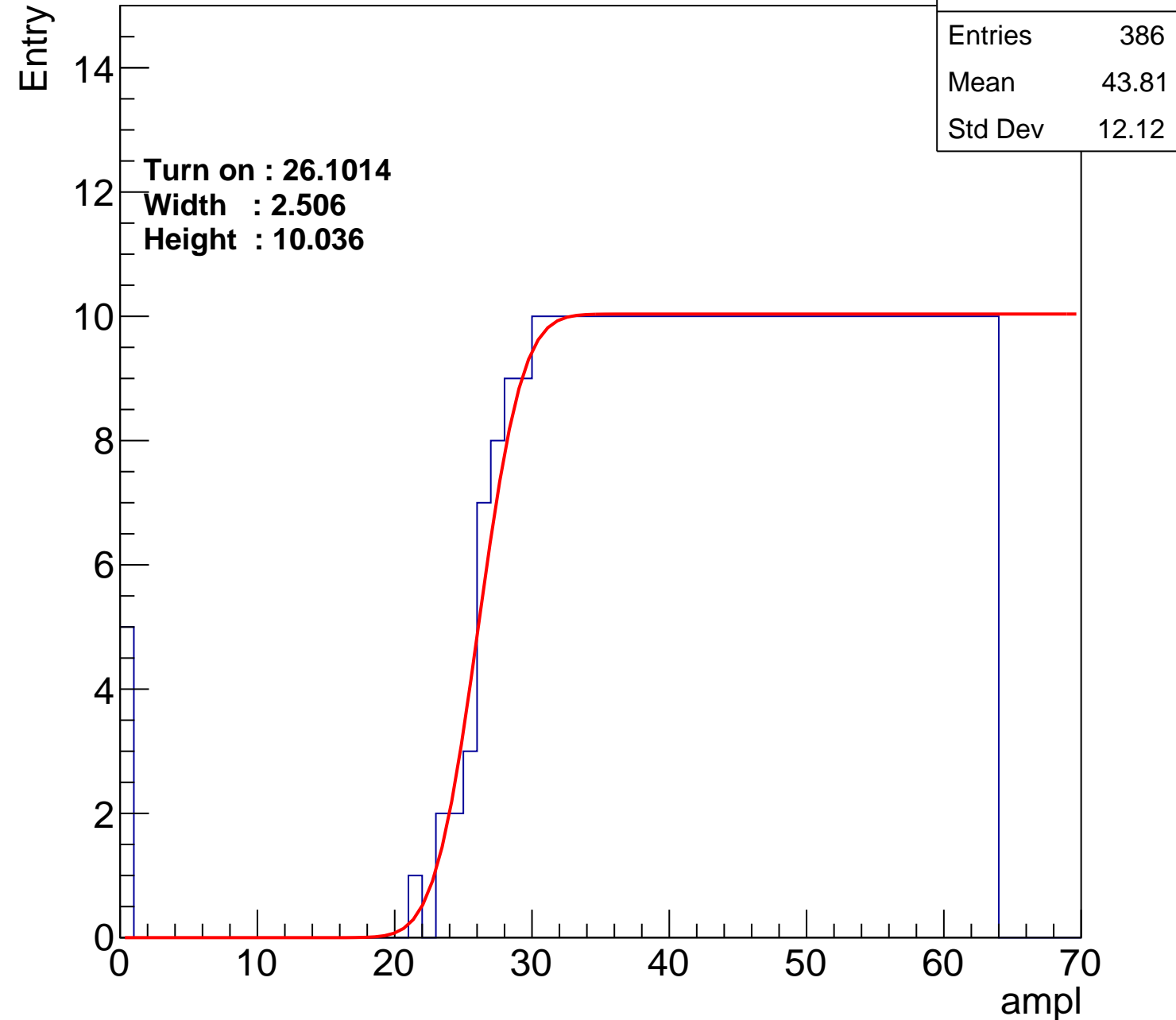
Width : 2.506

Height : 10.036

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch60

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	378
Mean	44.31
Std Dev	11.63

**Turn on : 26.9864**

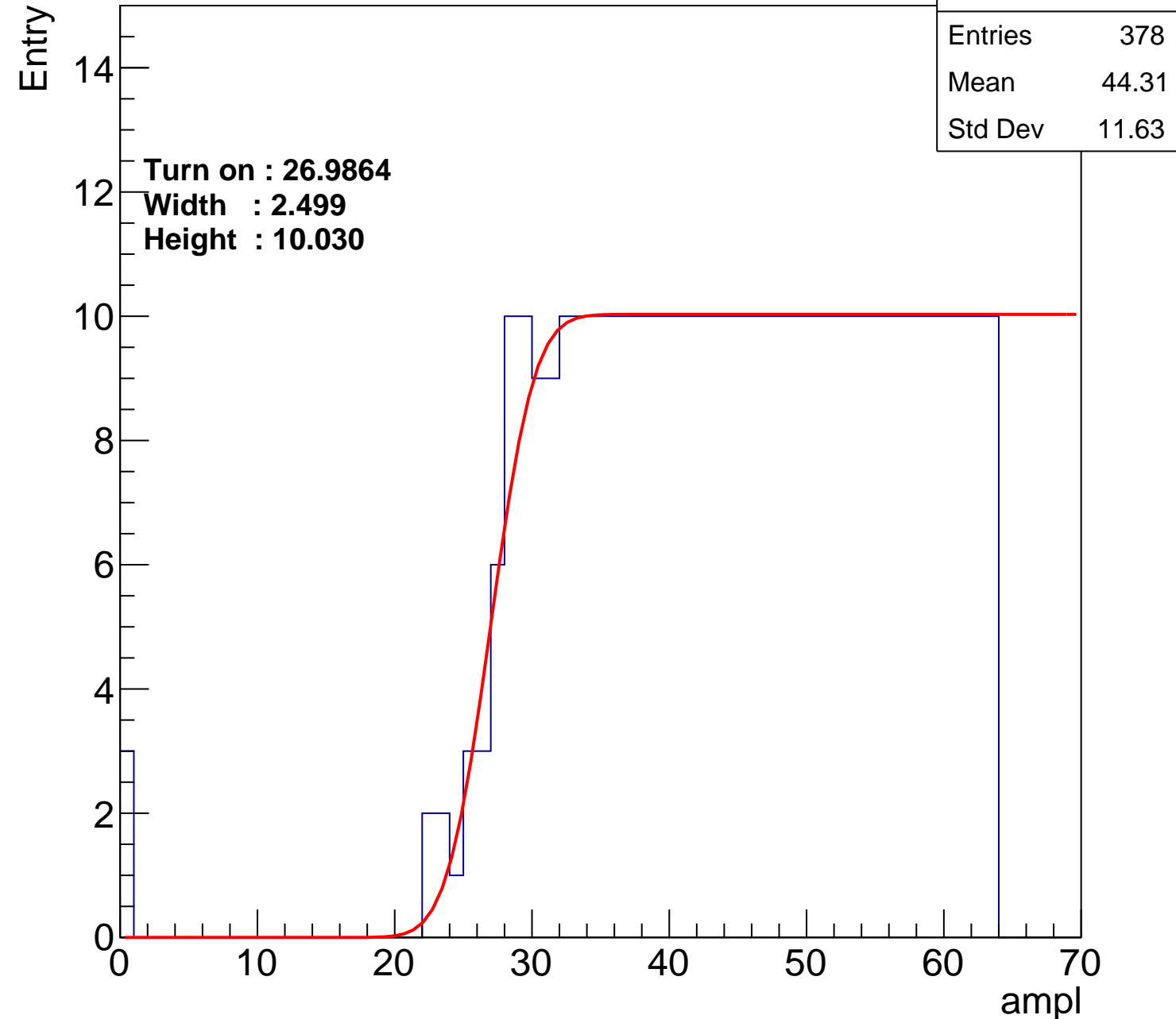
**Width : 2.499**

**Height : 10.030**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch61

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	356
Mean	45.45
Std Dev	10.9

Turn on : 29.0325

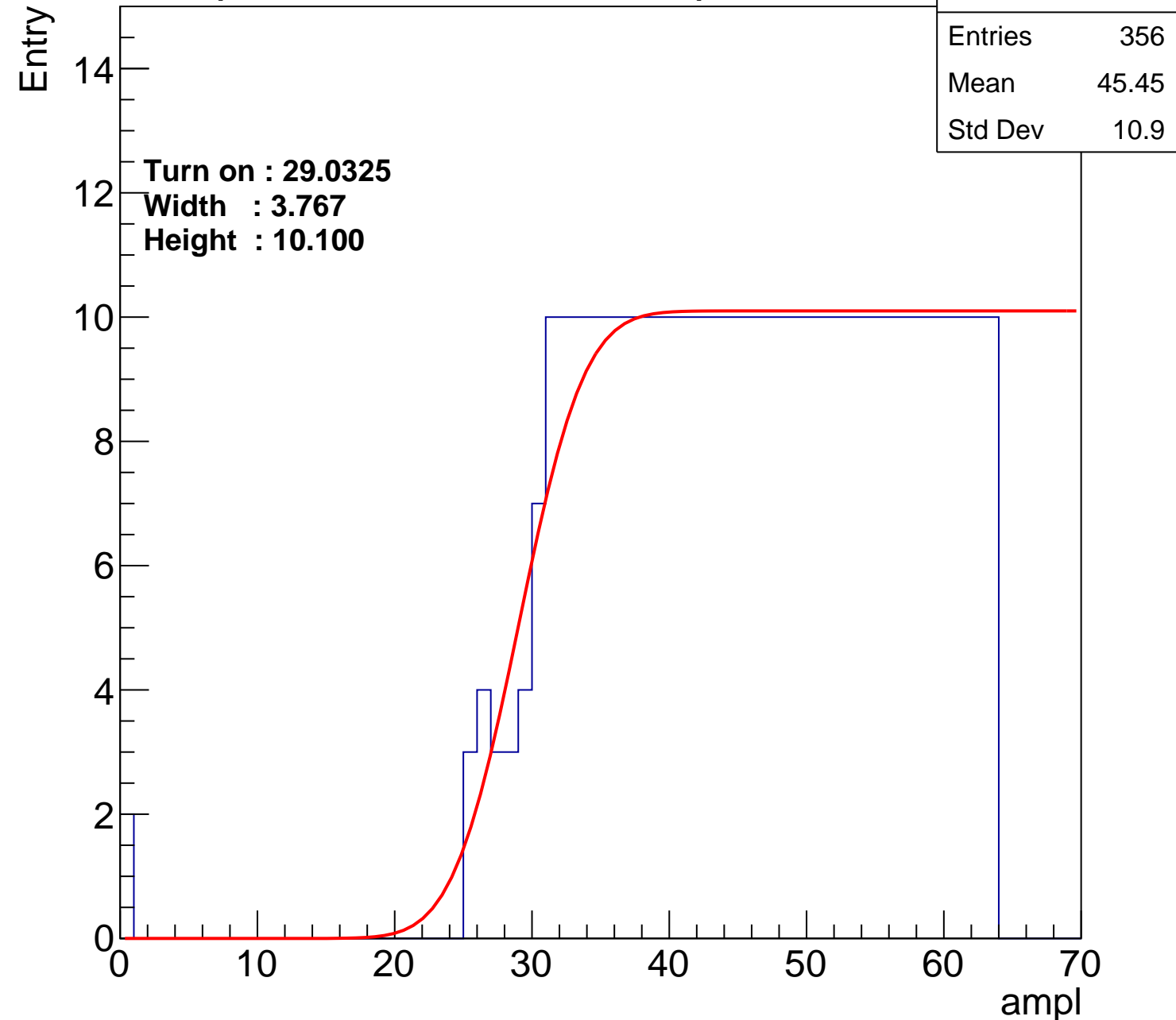
Width : 3.767

Height : 10.100

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch62

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	383
Mean	43.97
Std Dev	11.96

Turn on : 26.3234

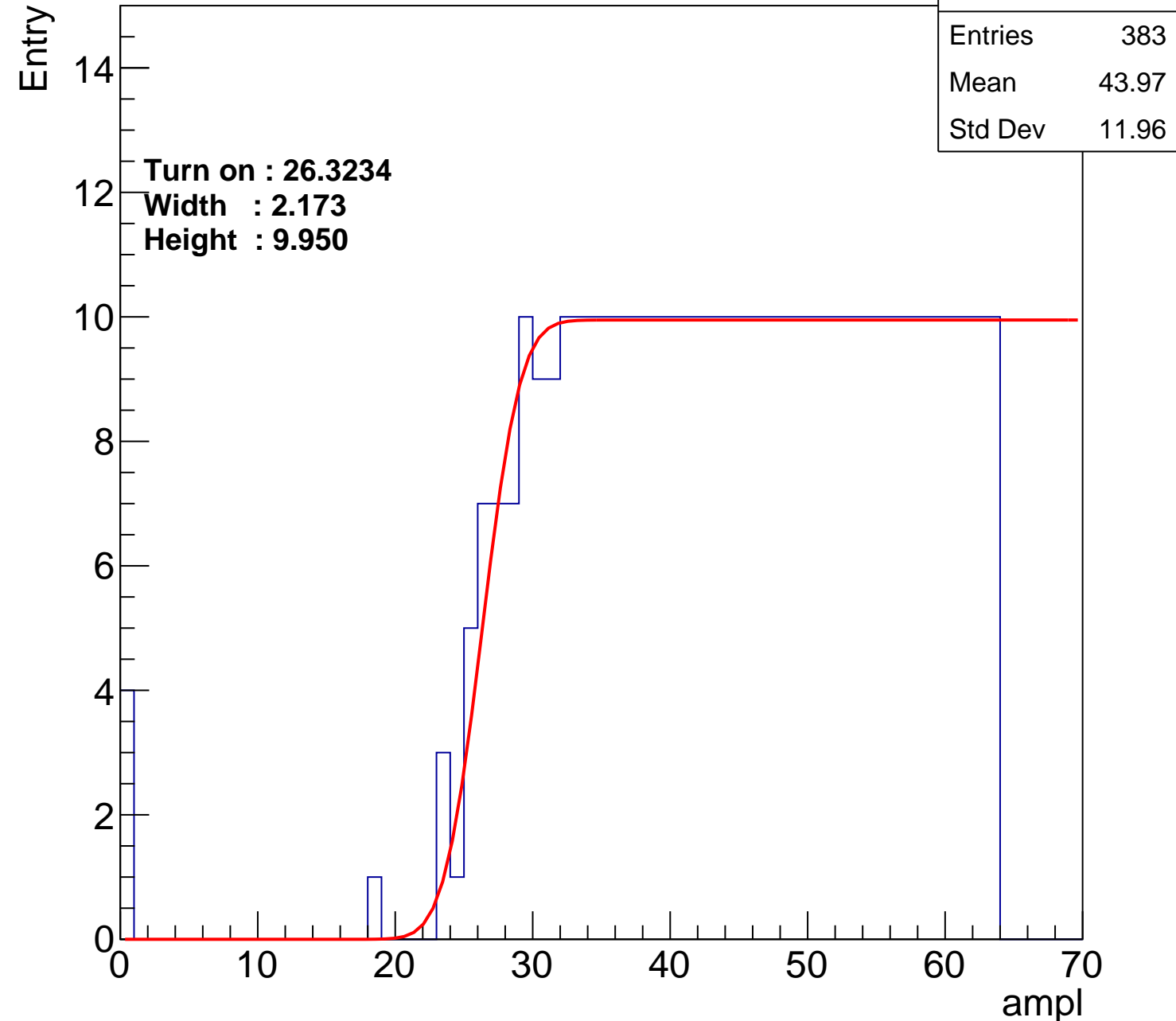
Width : 2.173

Height : 9.950

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L100S, U7-ch63

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	370
Mean	44.8
Std Dev	11.11

Turn on : 26.8625

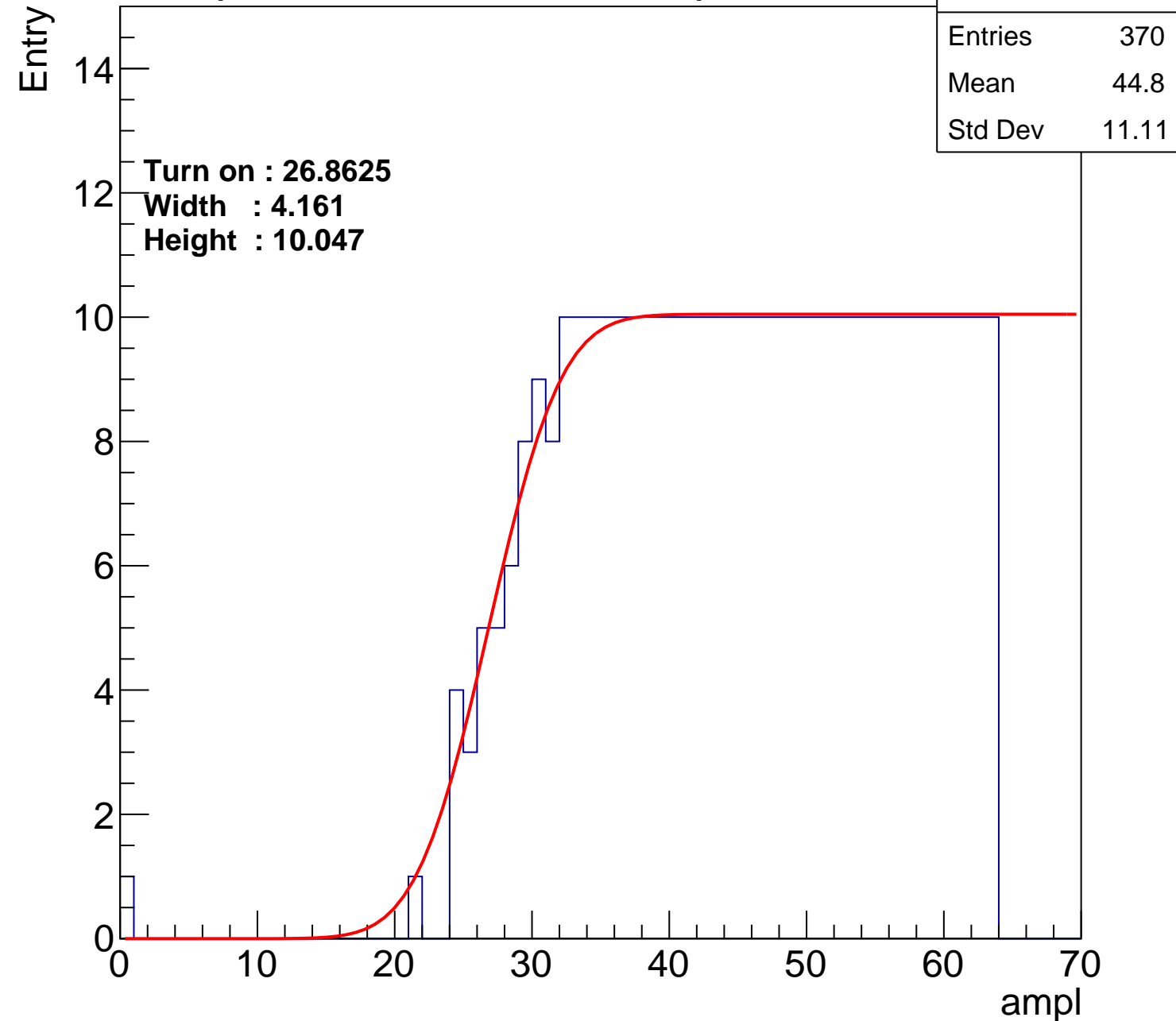
Width : 4.161

Height : 10.047

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch64

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	383
Mean	44.2
Std Dev	11.38

Turn on : 26.4574

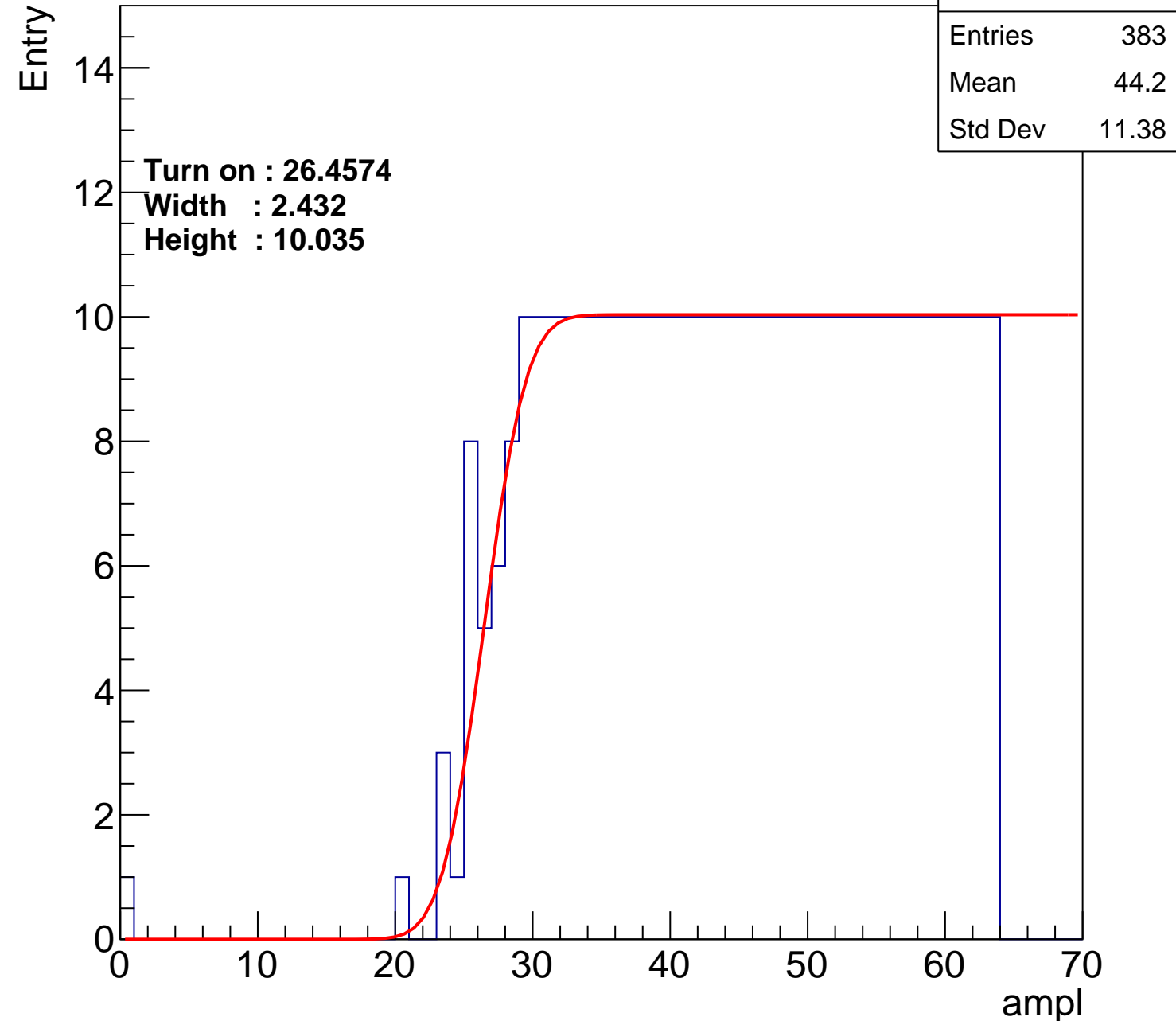
Width : 2.432

Height : 10.035

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch65

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	397
Mean	43.35
Std Dev	12.14

Turn on : 24.6074

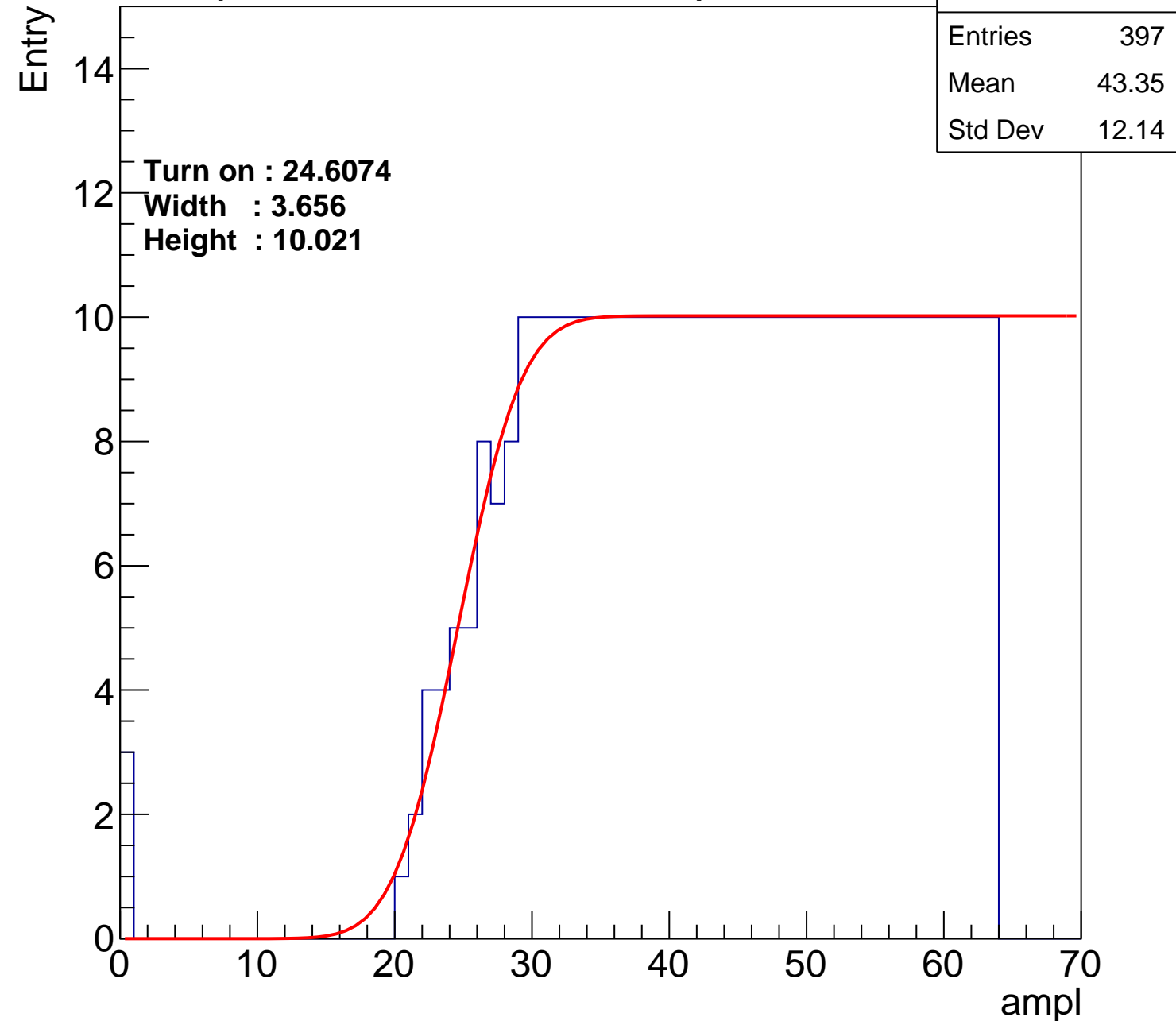
Width : 3.656

Height : 10.021

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch66

calib\_packv5\_042523\_0143.root, FC#4, port A2

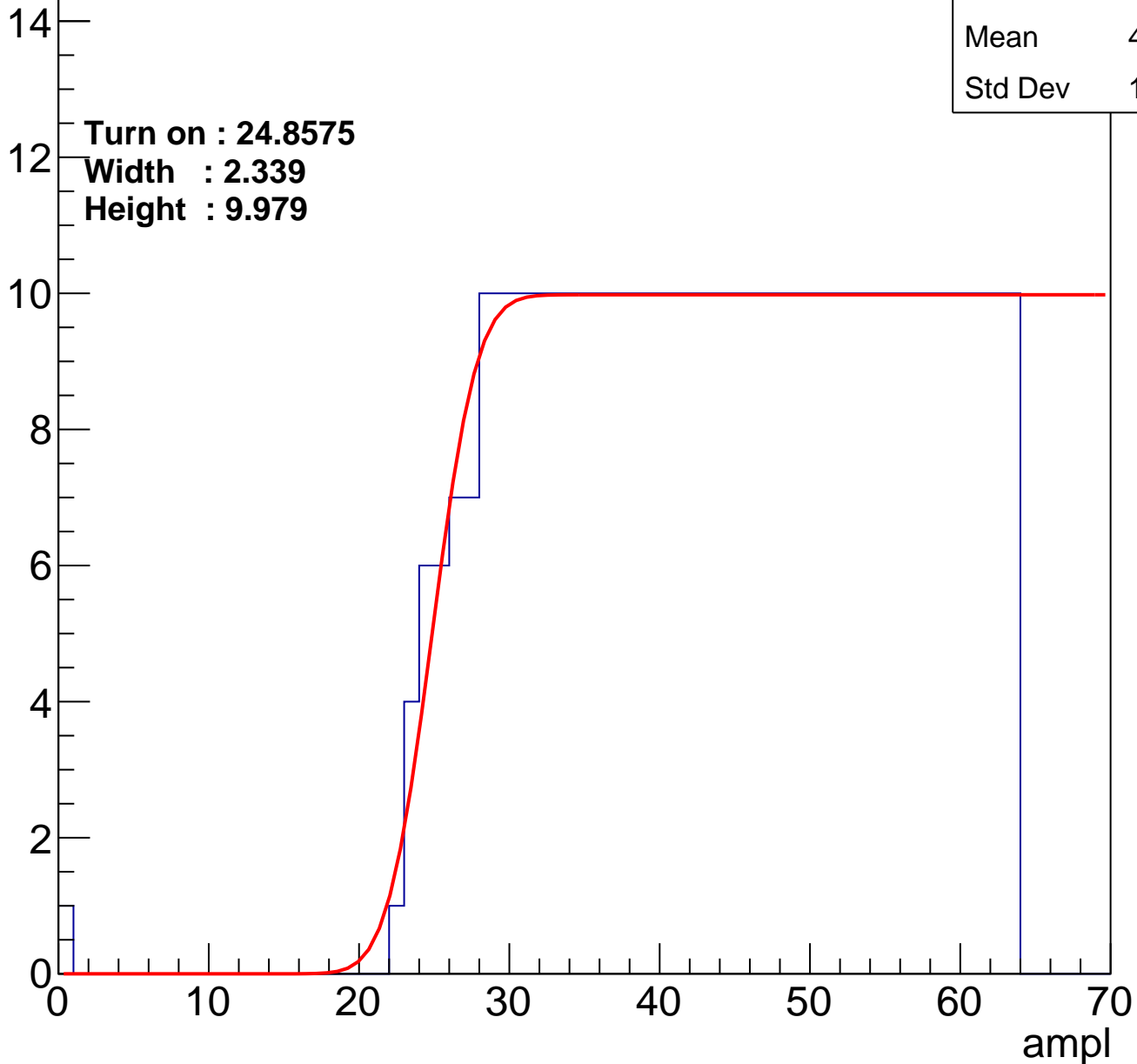
Entries	392
Mean	43.77
Std Dev	11.59

Turn on : 24.8575

Width : 2.339

Height : 9.979

Entry



# B1L100S, U7-ch67

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	373
Mean	44.61
Std Dev	11.33

Turn on : 27.1371

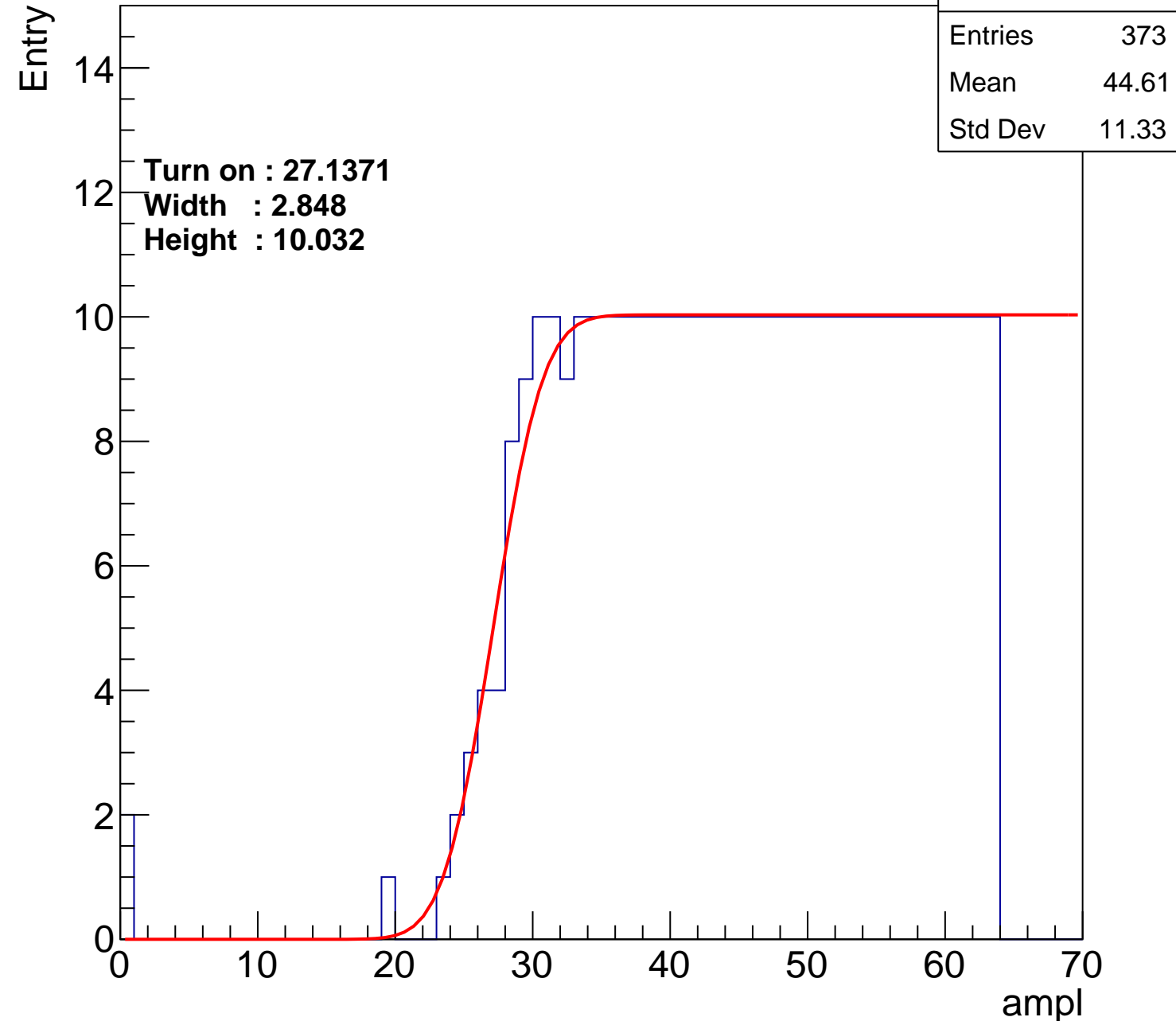
Width : 2.848

Height : 10.032

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch68

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	369
Mean	44.86
Std Dev	11.06

**Turn on : 27.5974**

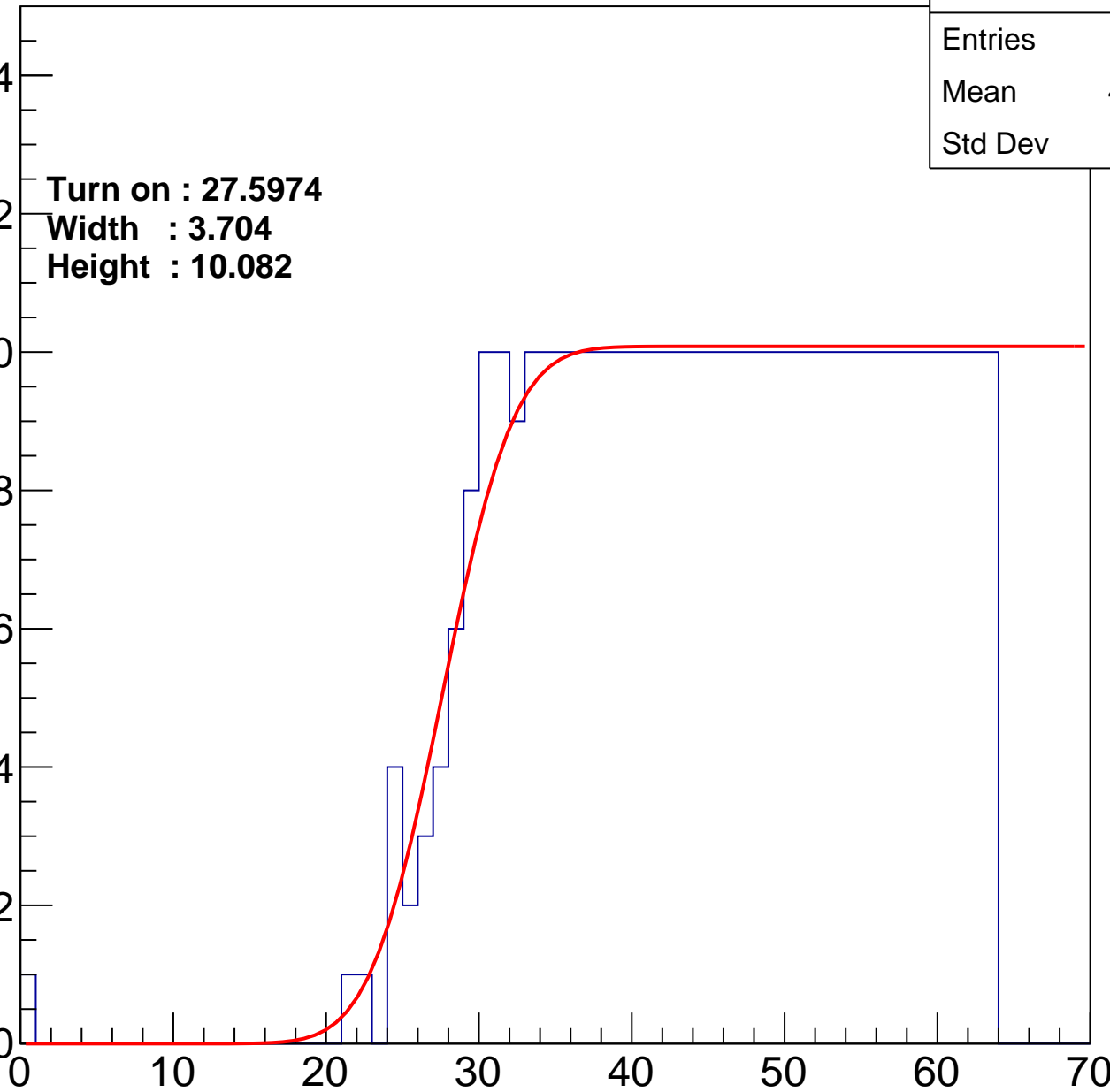
**Width : 3.704**

**Height : 10.082**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch69

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	358
Mean	45.35
Std Dev	10.95

**Turn on : 28.6282**

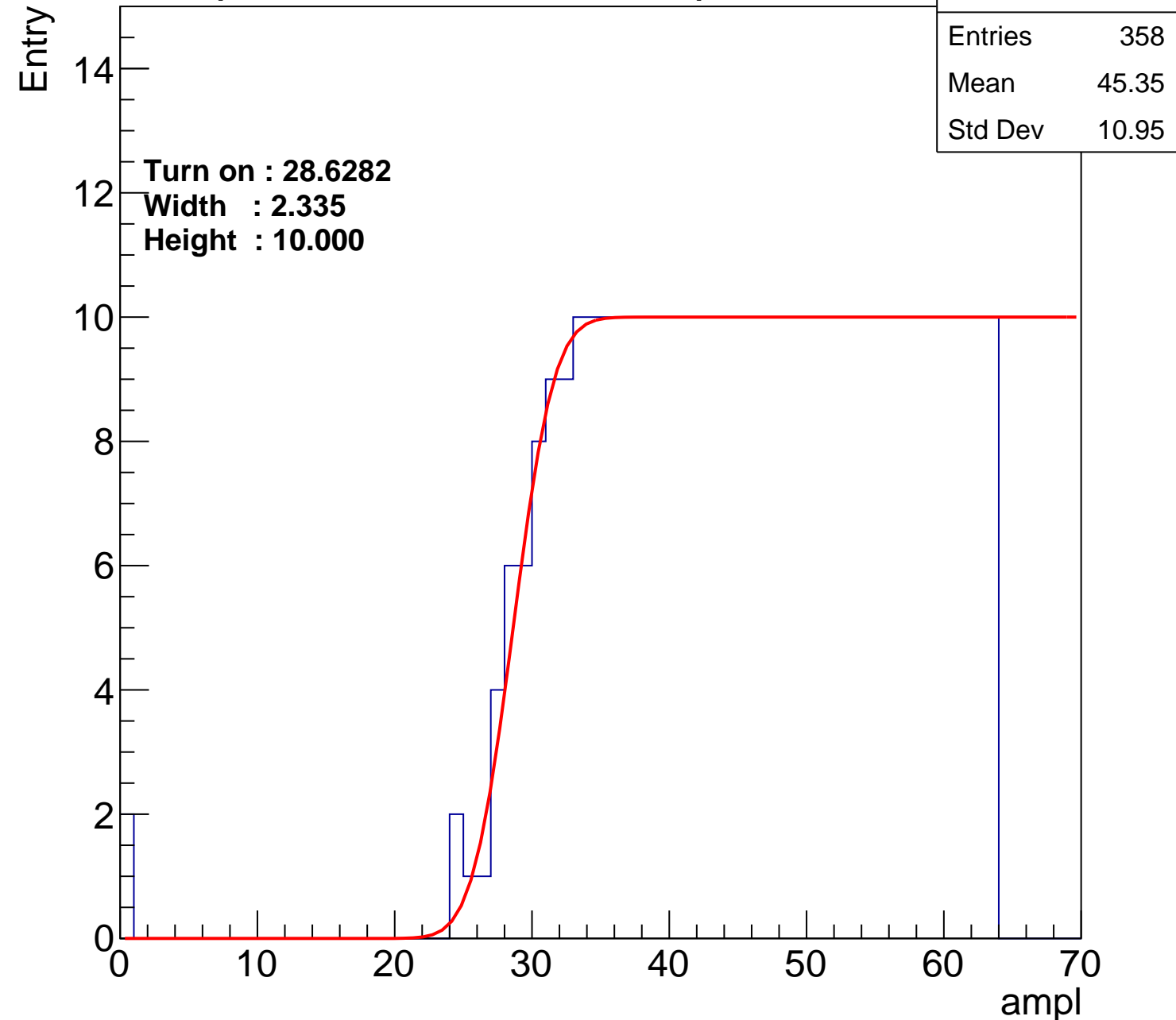
**Width : 2.335**

**Height : 10.000**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch70

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	370
Mean	44.57
Std Dev	11.71

Turn on : 27.0816

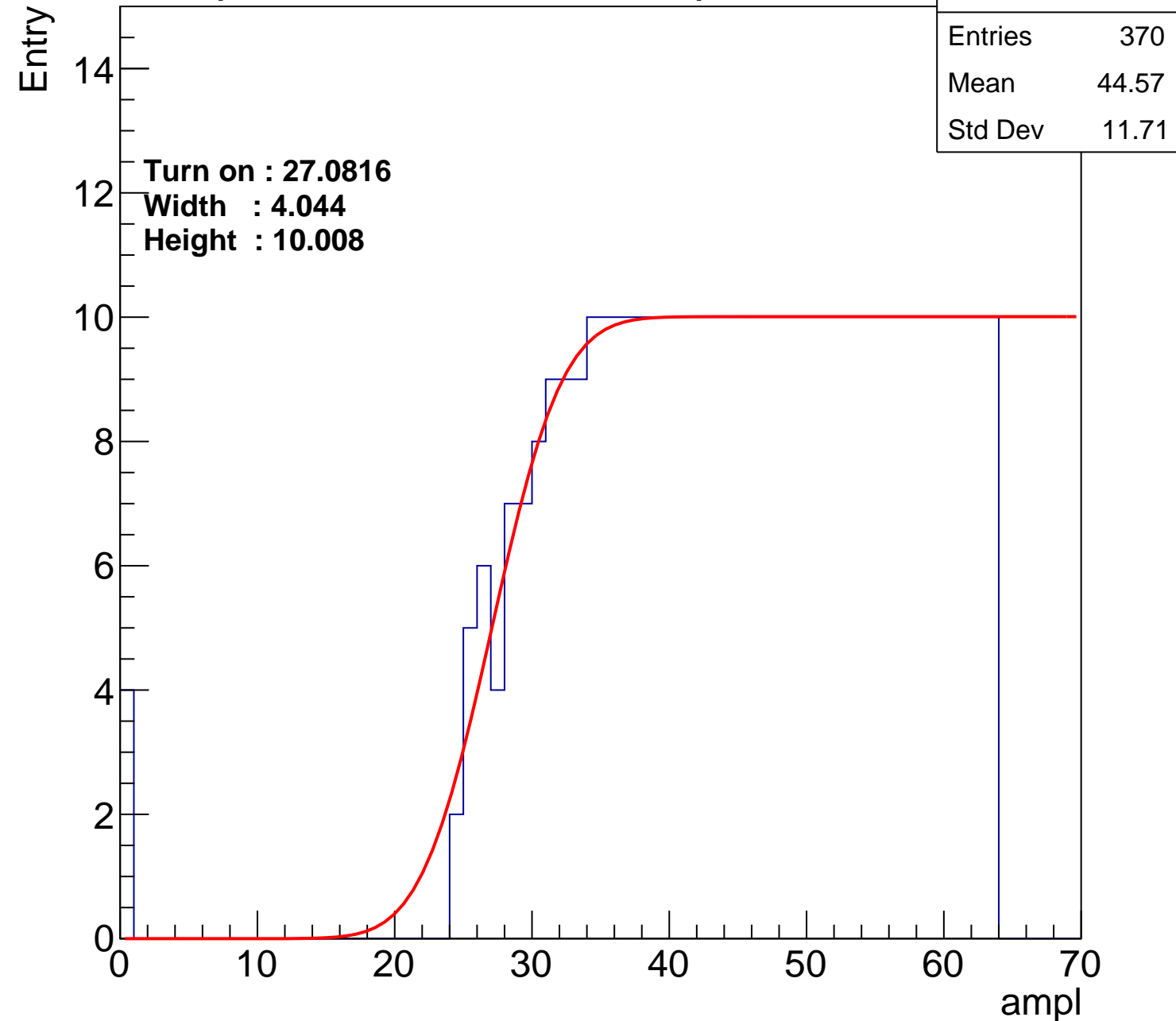
Width : 4.044

Height : 10.008

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L100S, U7-ch71

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	374
Mean	44.68
Std Dev	11.08

**Turn on : 26.9166**

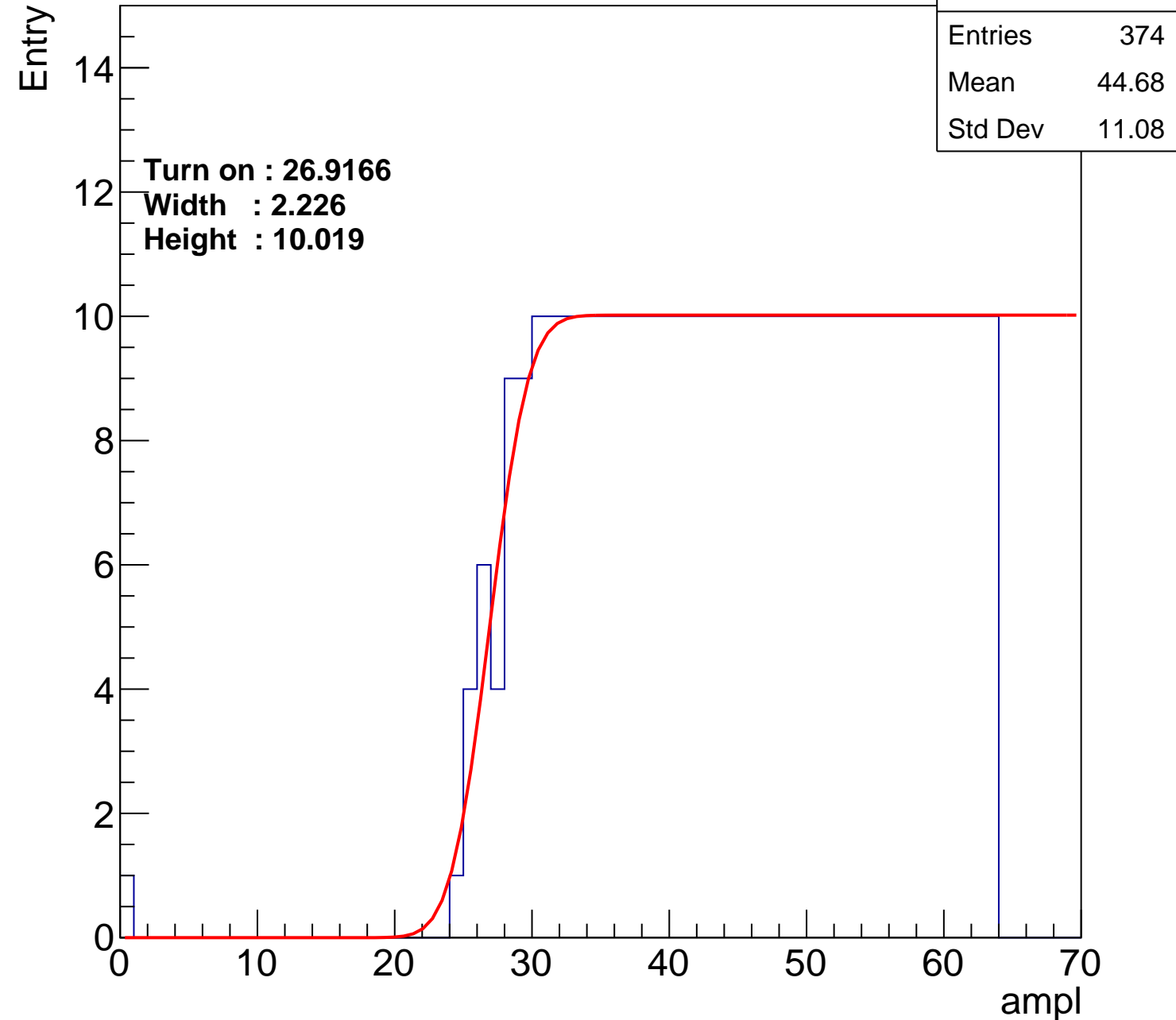
**Width : 2.226**

**Height : 10.019**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch72

**calib\_packv5\_042523\_0143.root, FC#4, port A2**

Entries 346

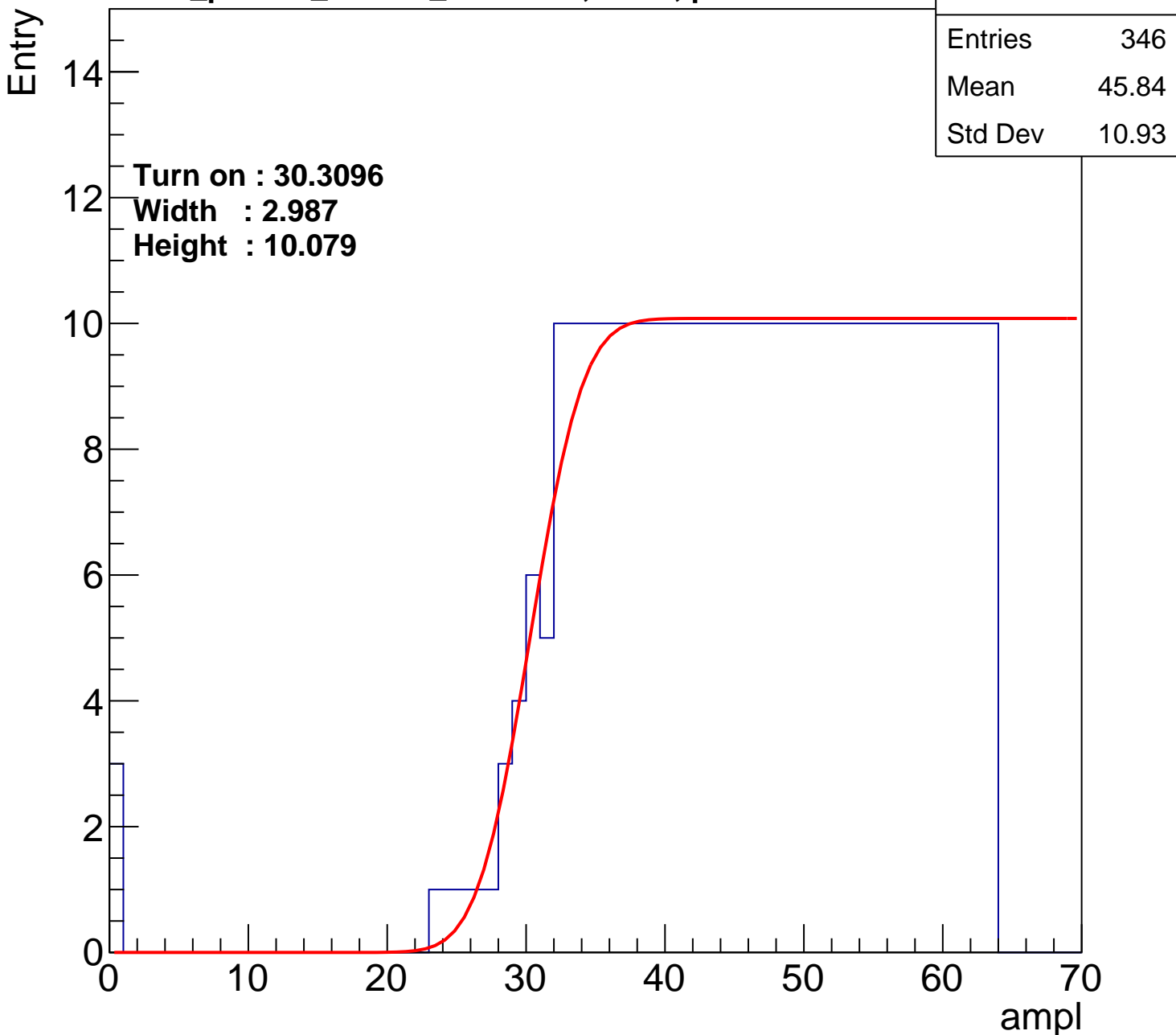
Mean 45.84

Std Dev 10.93

**Turn on : 30.3096**

**Width : 2.987**

**Height : 10.079**



# B1L100S, U7-ch73

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	375
Mean	44.41
Std Dev	11.7

Turn on : 26.9156

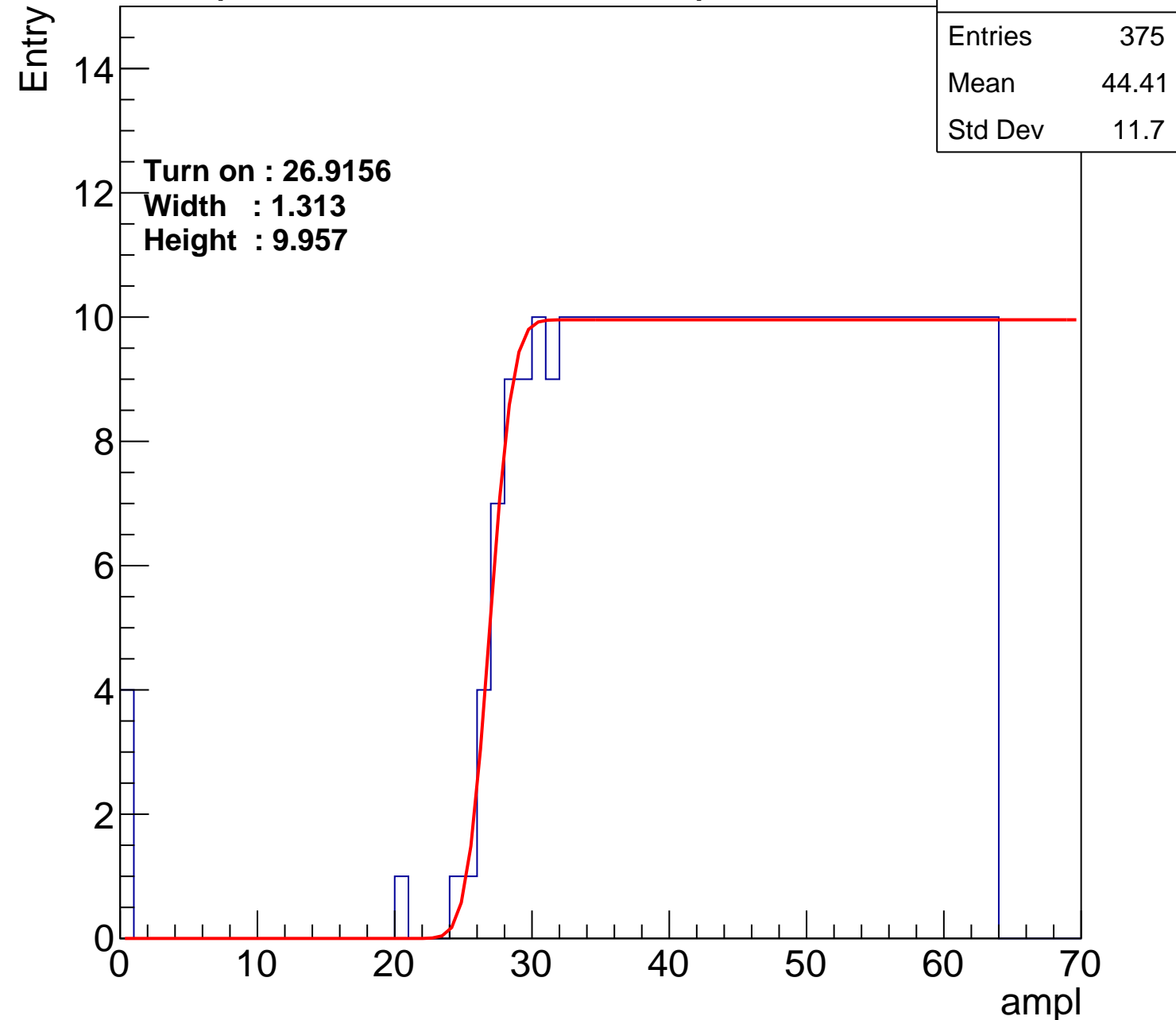
Width : 1.313

Height : 9.957

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch74

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	381
Mean	44.31
Std Dev	11.3

Turn on : 25.6456

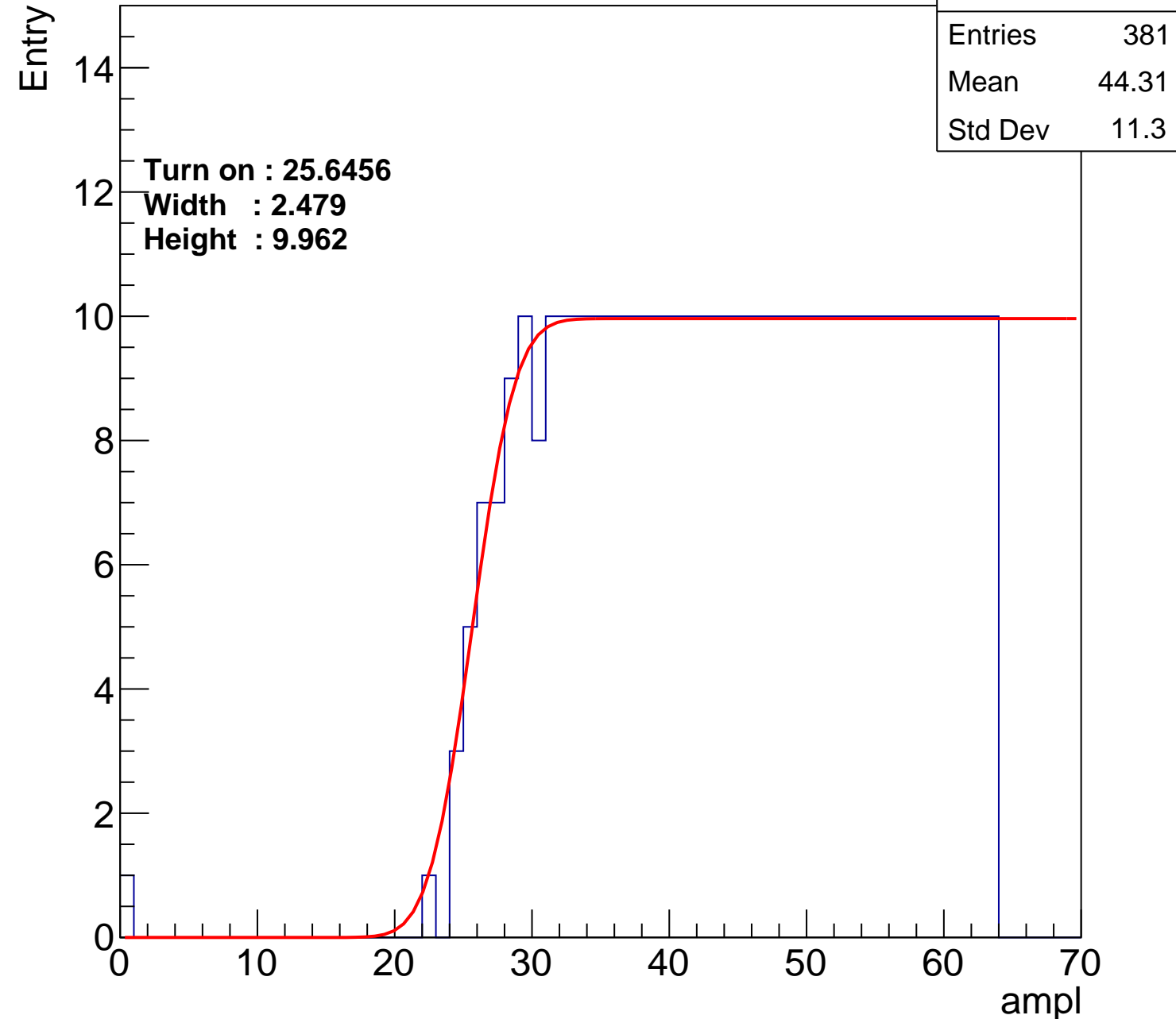
Width : 2.479

Height : 9.962

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch75

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	386
Mean	44.04
Std Dev	11.49

Turn on : 26.1857

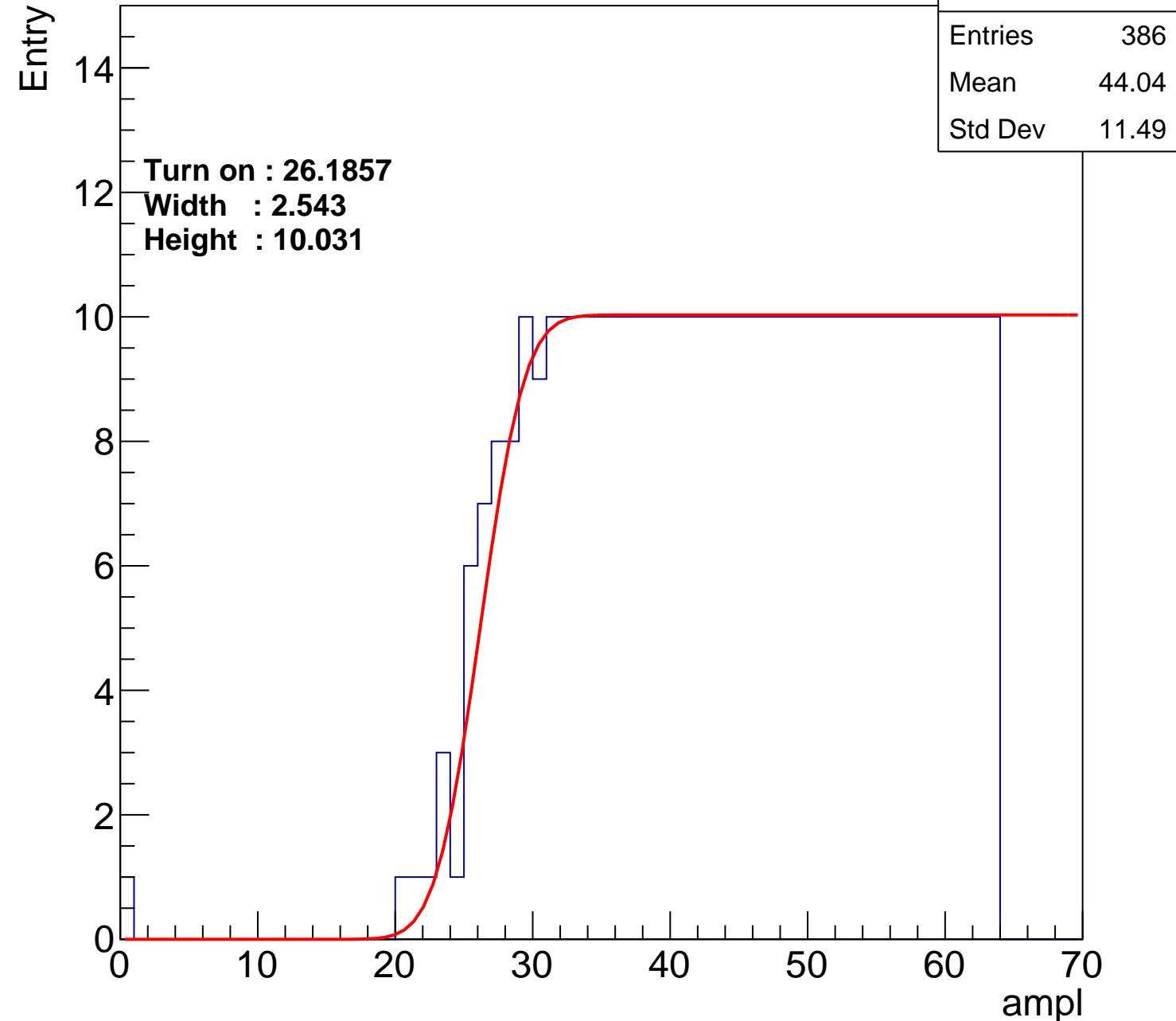
Width : 2.543

Height : 10.031

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch76

calib\_packv5\_042523\_0143.root, FC#4, port A2

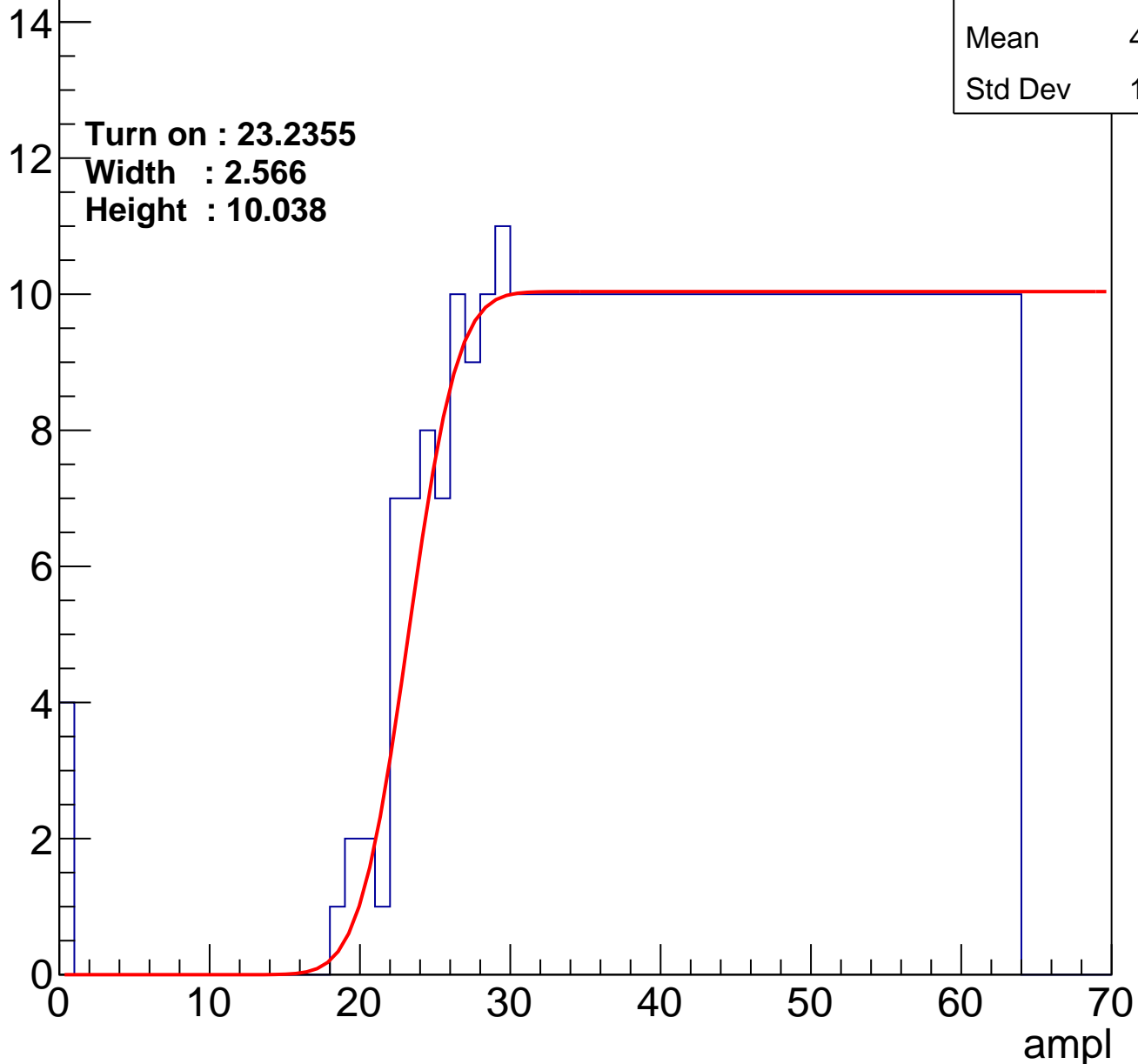
Entries	419
Mean	42.27
Std Dev	12.74

Turn on : 23.2355

Width : 2.566

Height : 10.038

Entry



# B1L100S, U7-ch77

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	369
Mean	44.88
Std Dev	11.03

Turn on : 27.2935

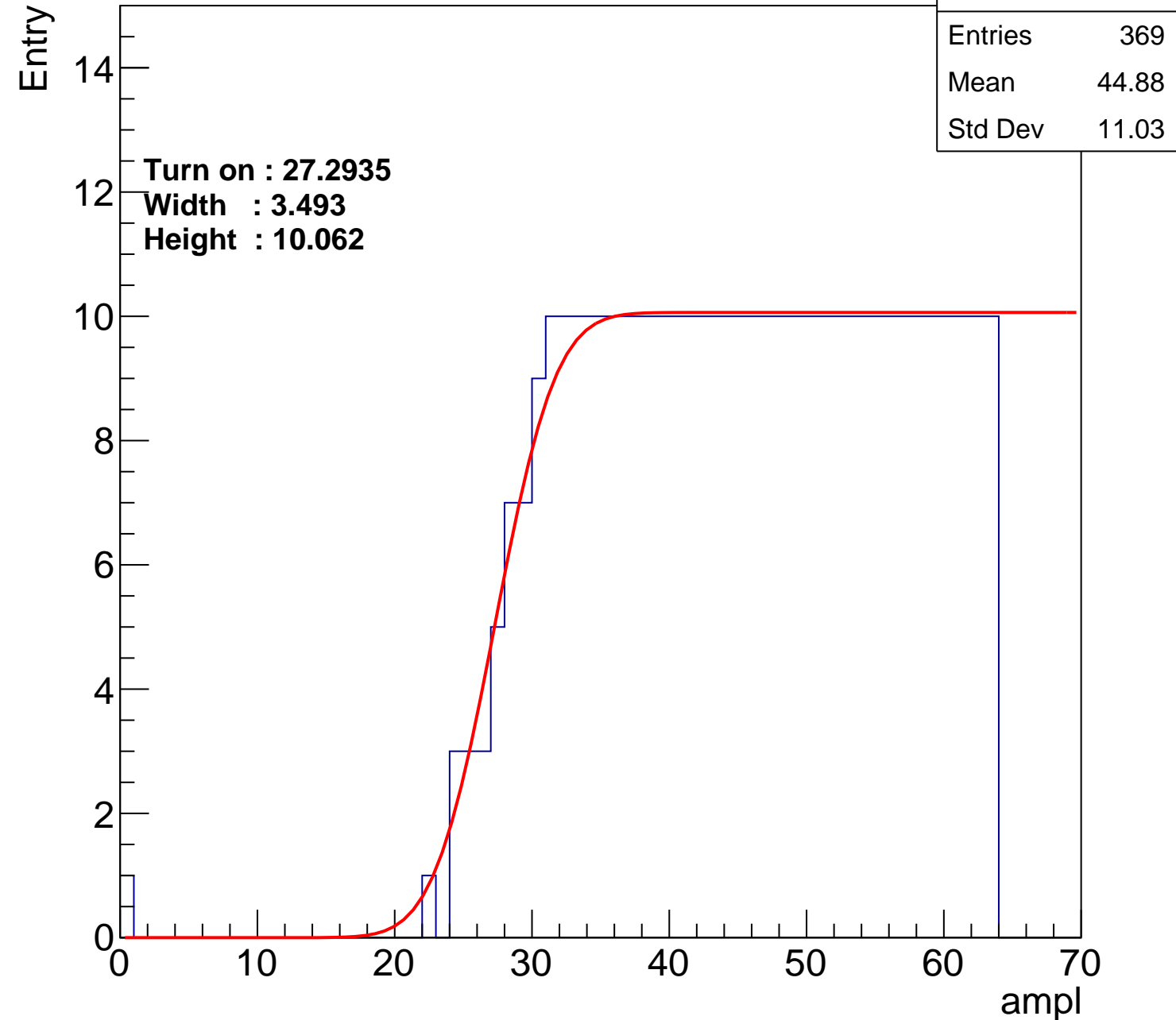
Width : 3.493

Height : 10.062

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch78

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	377
Mean	44.27
Std Dev	11.83

Turn on : 26.8300

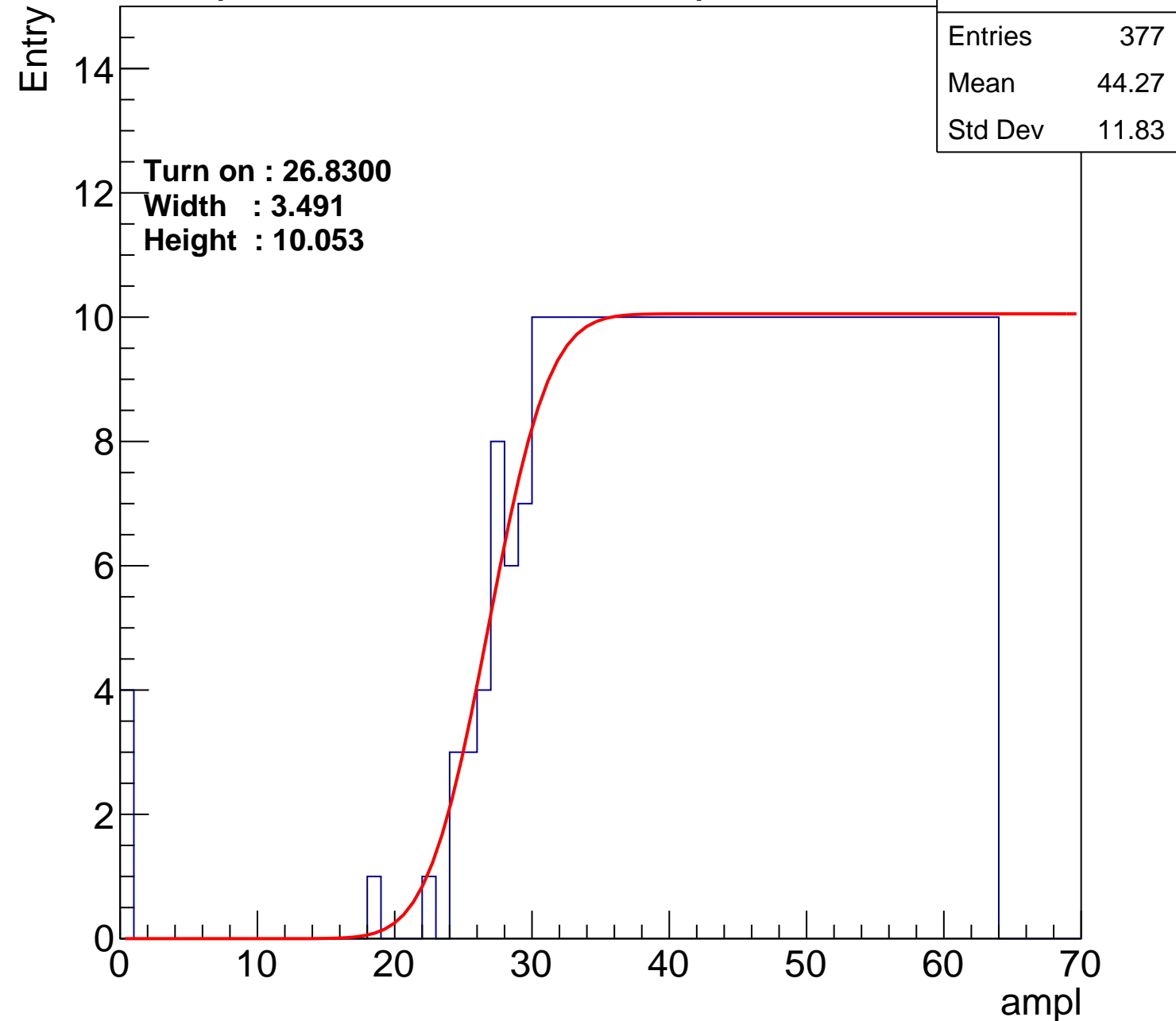
Width : 3.491

Height : 10.053

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L100S, U7-ch79

calib\_packv5\_042523\_0143.root, FC#4, port A2

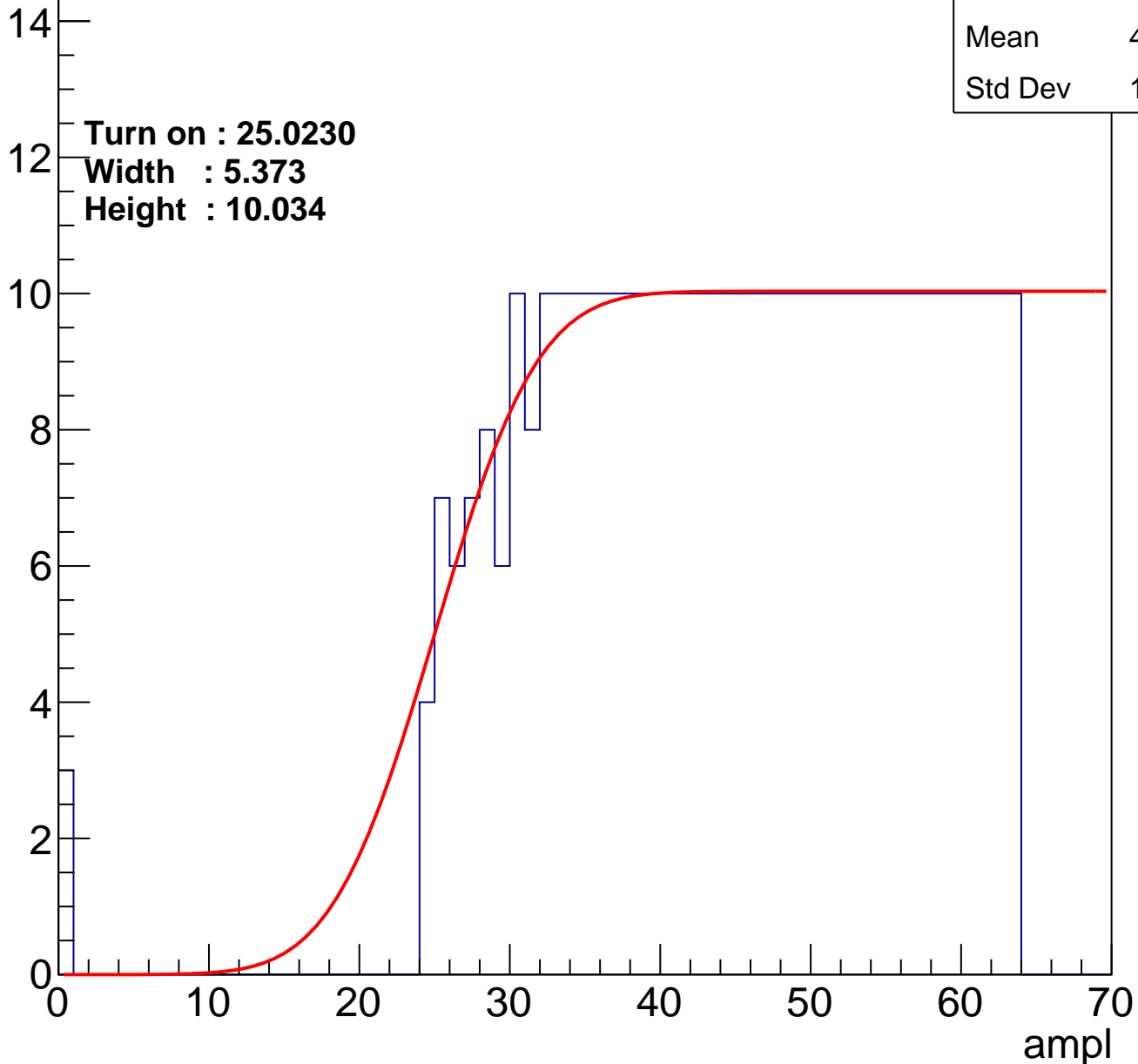
Entries	379
Mean	44.23
Std Dev	11.69

Turn on : 25.0230

Width : 5.373

Height : 10.034

Entry



# B1L100S, U7-ch80

calib\_packv5\_042523\_0143.root, FC#4, port A2

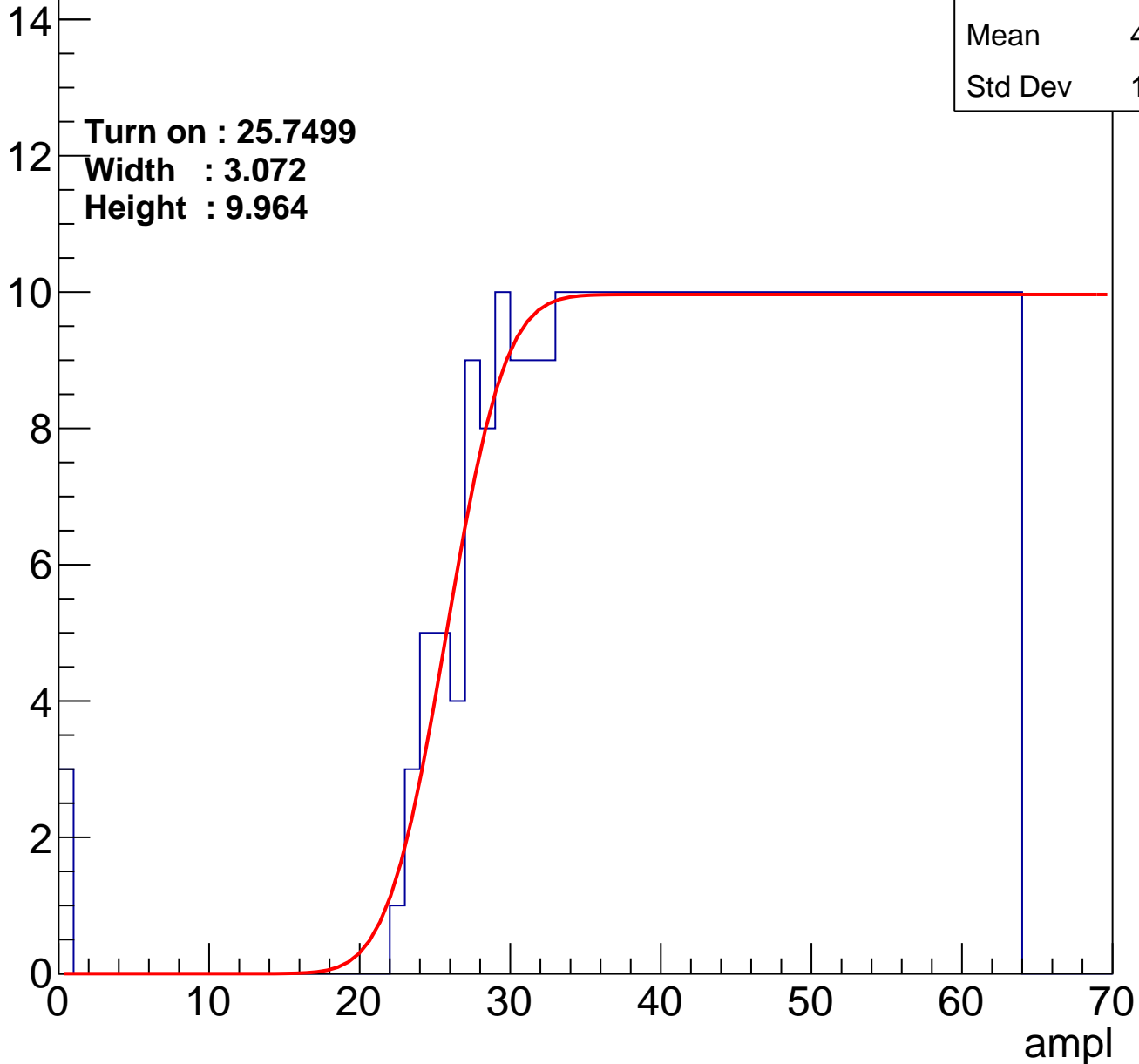
Entries	385
Mean	43.93
Std Dev	11.84

Turn on : 25.7499

Width : 3.072

Height : 9.964

Entry



# B1L100S, U7-ch81

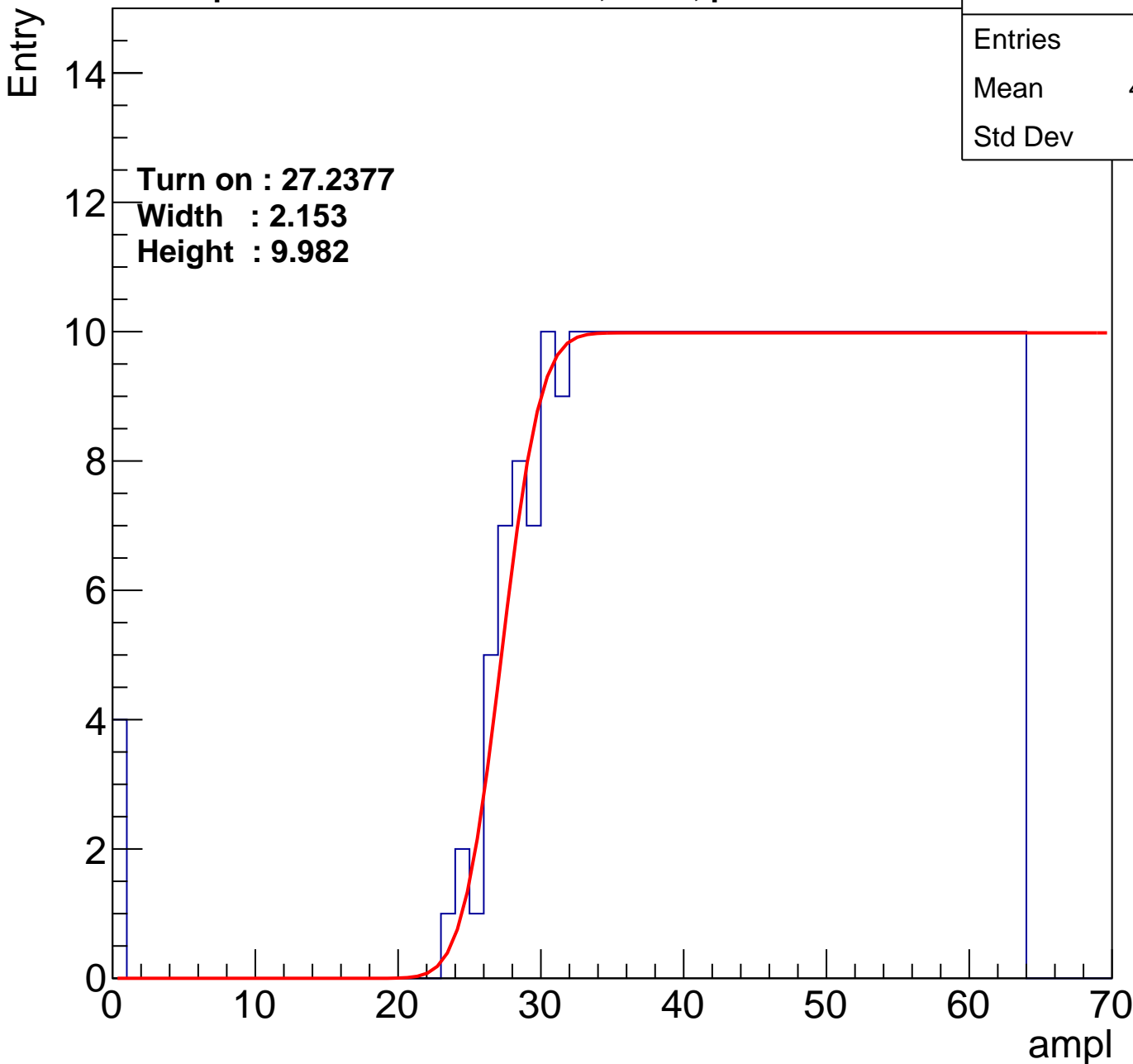
**calib\_packv5\_042523\_0143.root, FC#4, port A2**

Entries	374
Mean	44.44
Std Dev	11.7

**Turn on : 27.2377**

**Width : 2.153**

**Height : 9.982**



# B1L100S, U7-ch82

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	394
Mean	43.52
Std Dev	12.03

**Turn on : 25.0757**

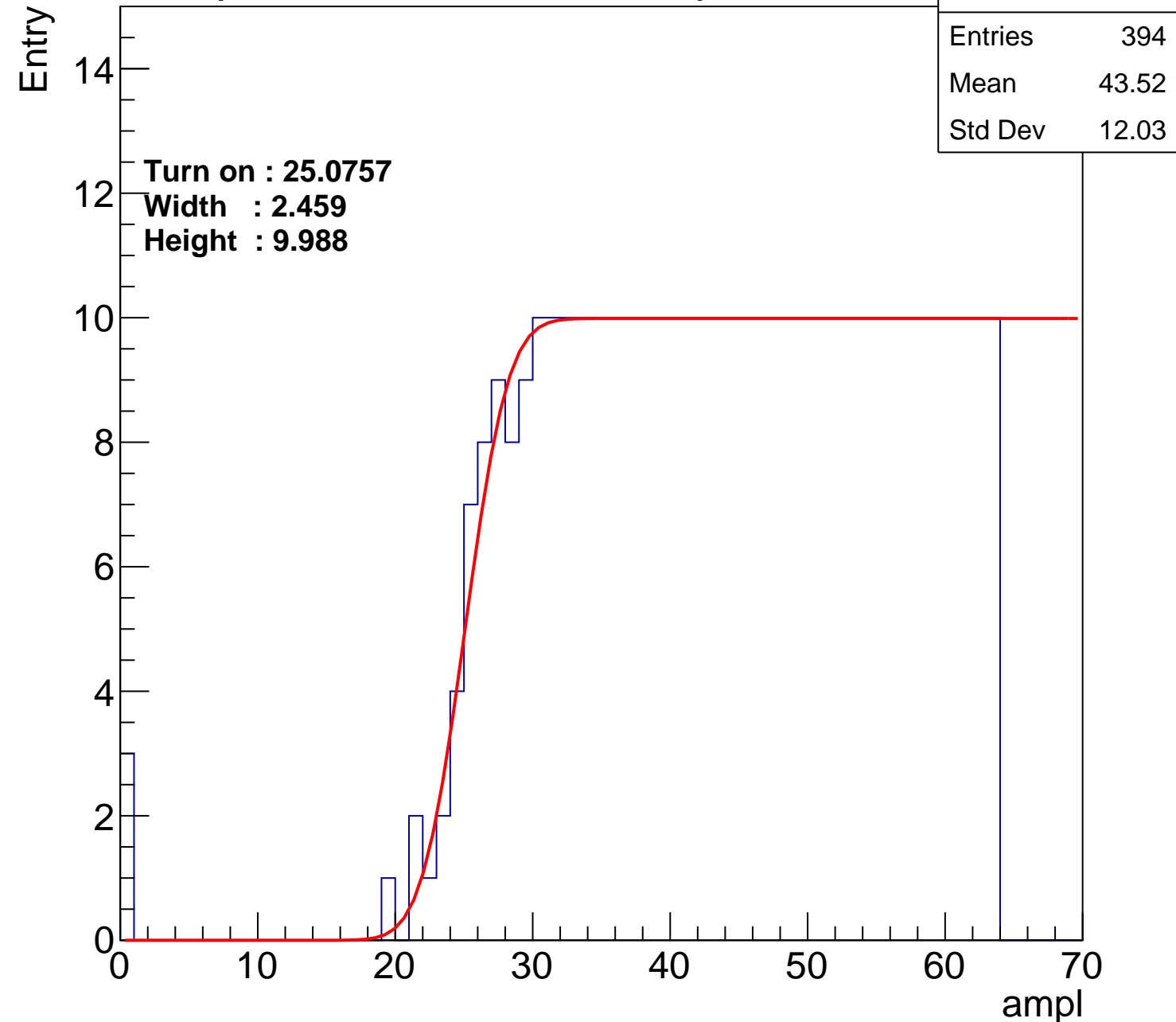
**Width : 2.459**

**Height : 9.988**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch83

calib\_packv5\_042523\_0143.root, FC#4, port A2

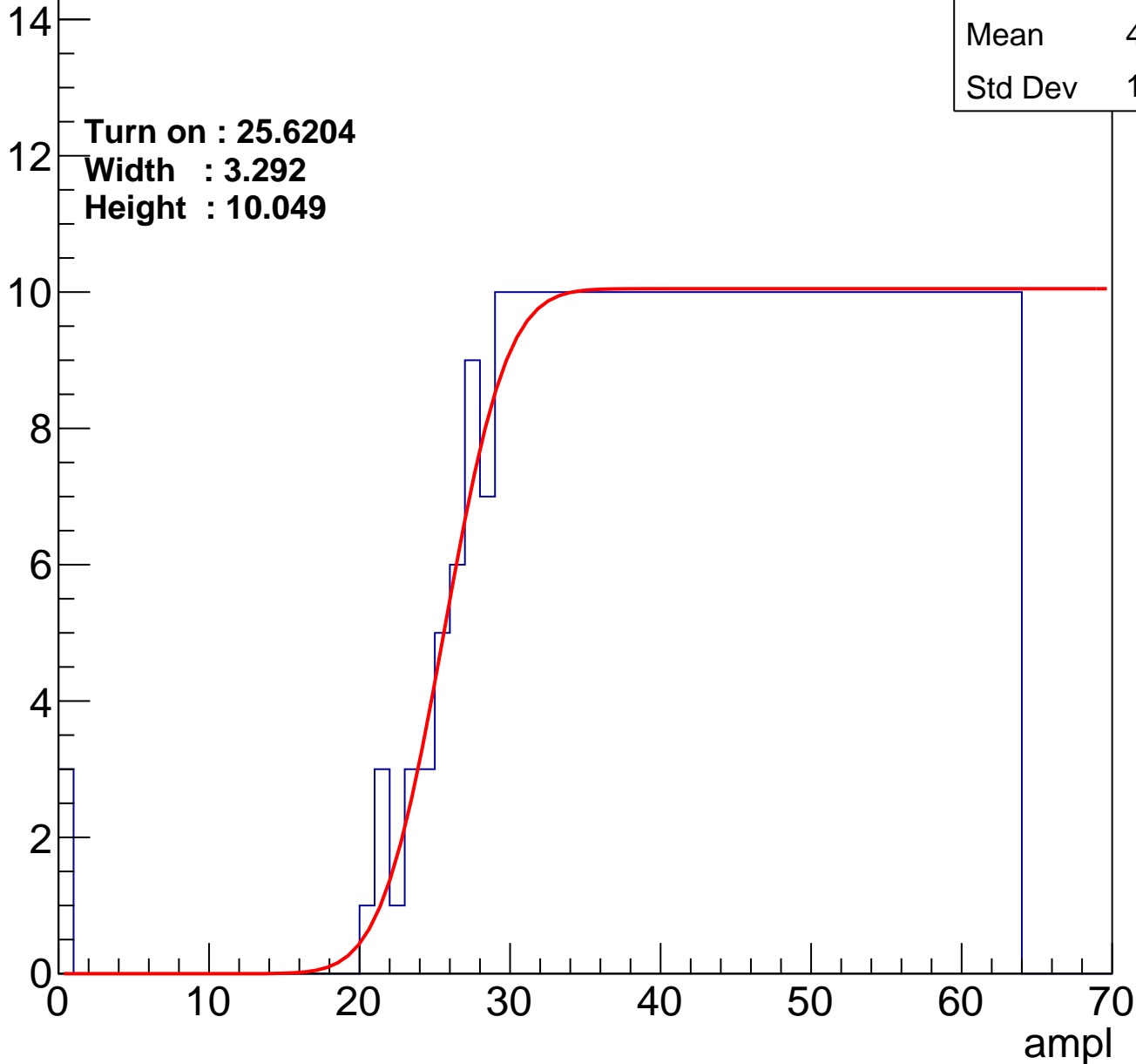
Entries	391
Mean	43.65
Std Dev	11.99

Turn on : 25.6204

Width : 3.292

Height : 10.049

Entry



# B1L100S, U7-ch84

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	373
Mean	44.6
Std Dev	11.34

Turn on : 26.6335

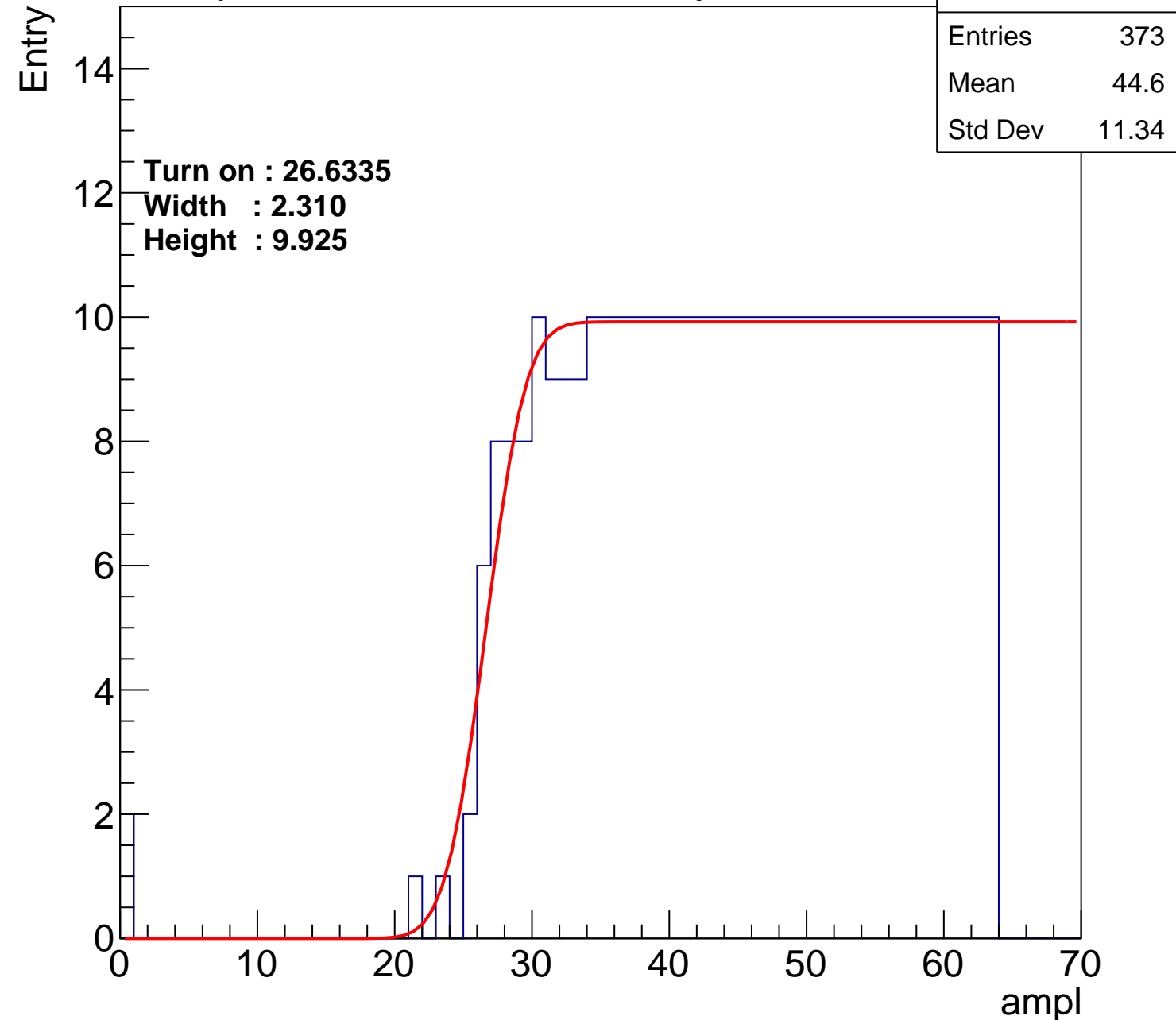
Width : 2.310

Height : 9.925

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch85

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	372
Mean	44.69
Std Dev	11.17

Turn on : 26.9707

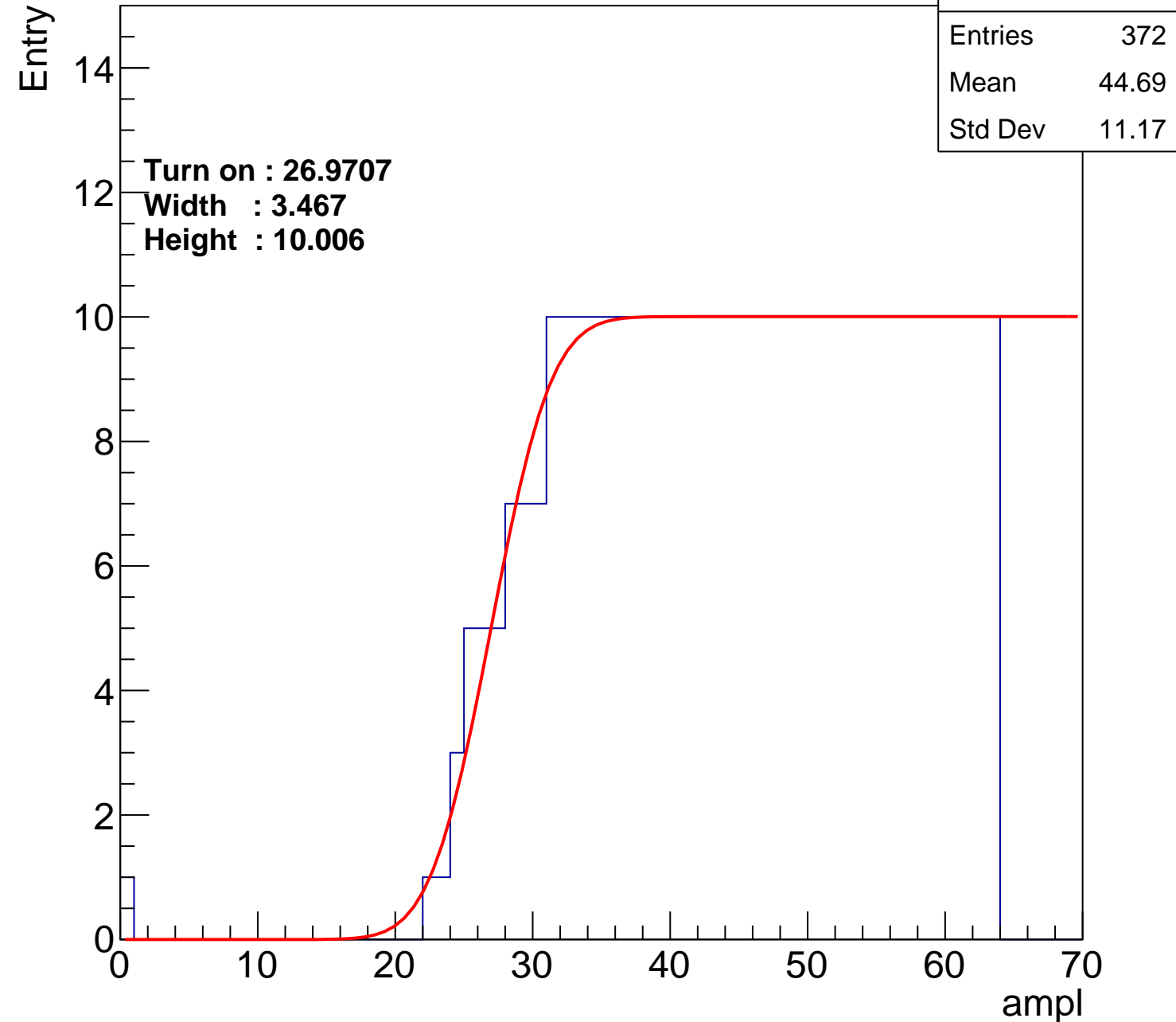
Width : 3.467

Height : 10.006

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch86

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	384
Mean	43.95
Std Dev	11.95

Turn on : 25.7533

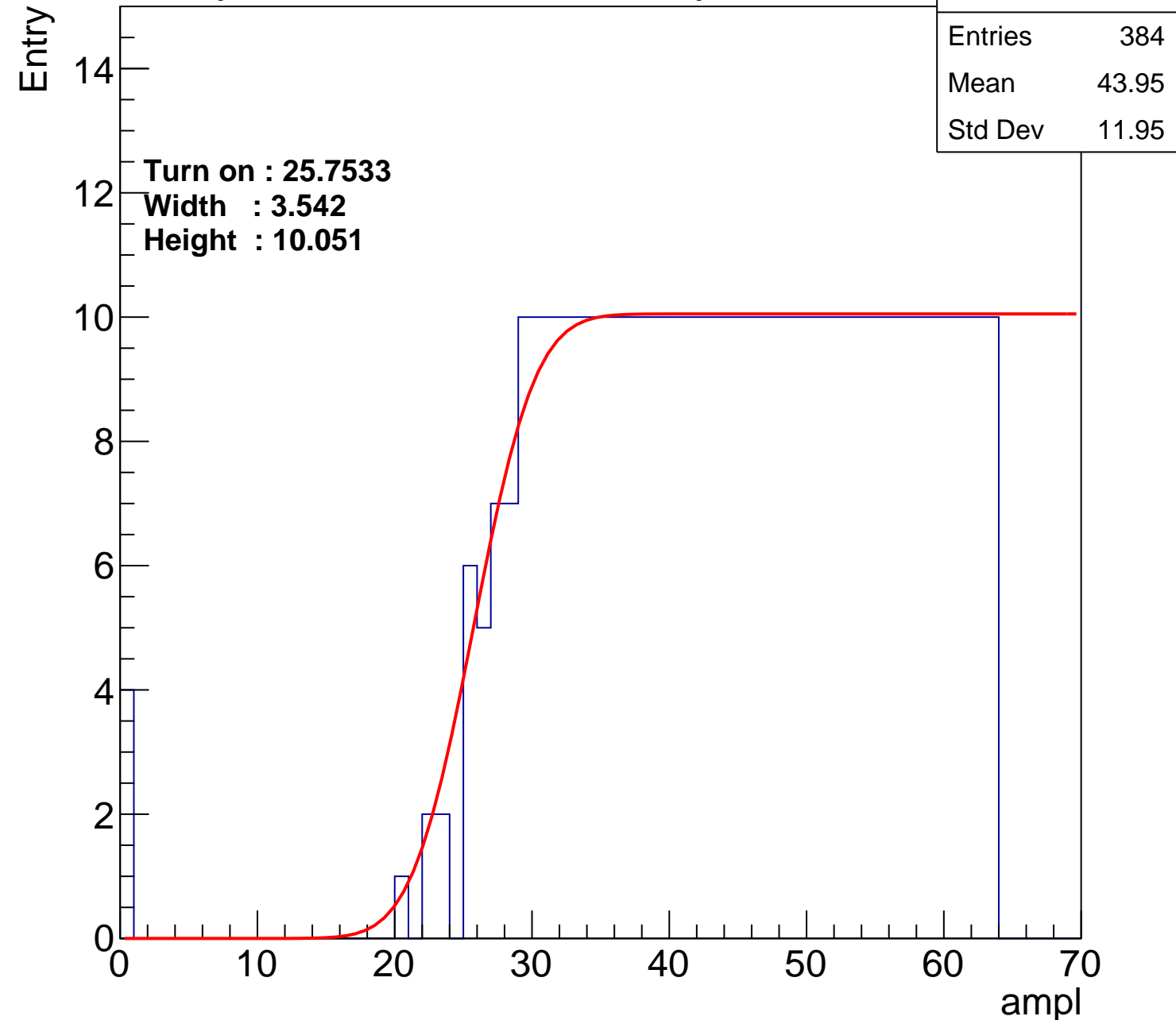
Width : 3.542

Height : 10.051

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L100S, U7-ch87

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	383
Mean	44.17
Std Dev	11.42

Turn on : 25.6657

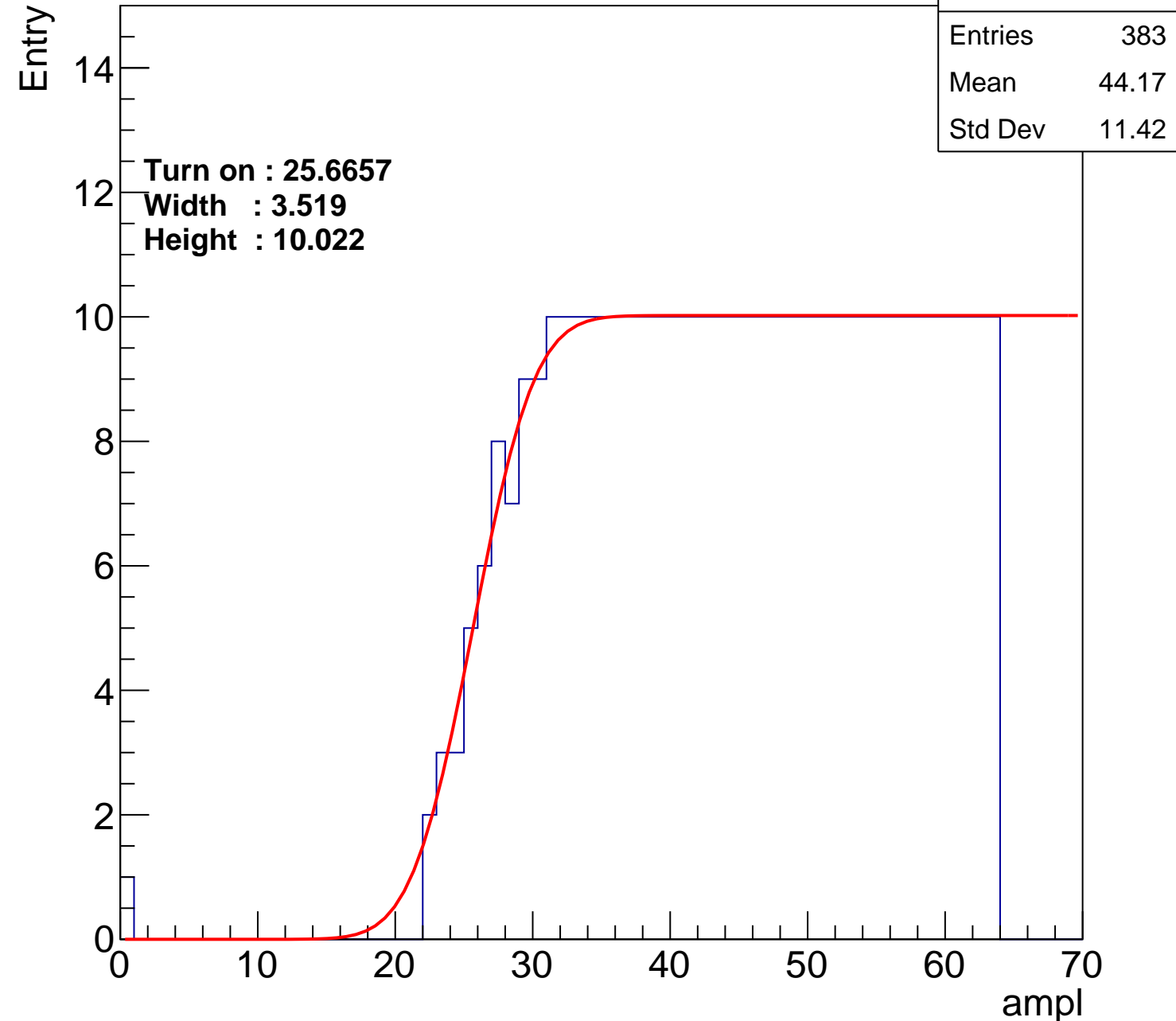
Width : 3.519

Height : 10.022

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch88

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	391
Mean	43.83
Std Dev	11.55

Turn on : 25.3696

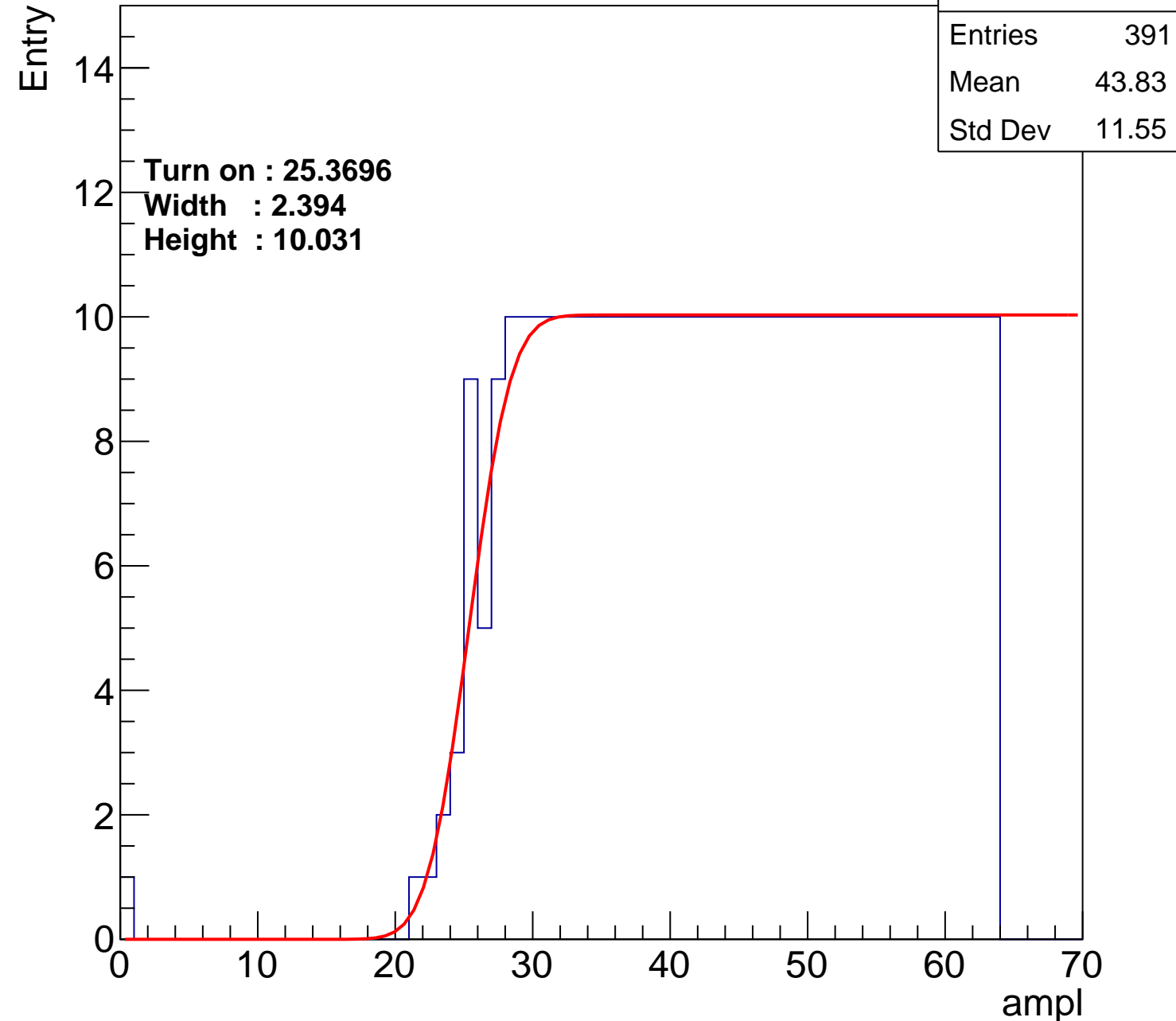
Width : 2.394

Height : 10.031

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch89

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	374
Mean	44.55
Std Dev	11.38

Turn on : 27.1268

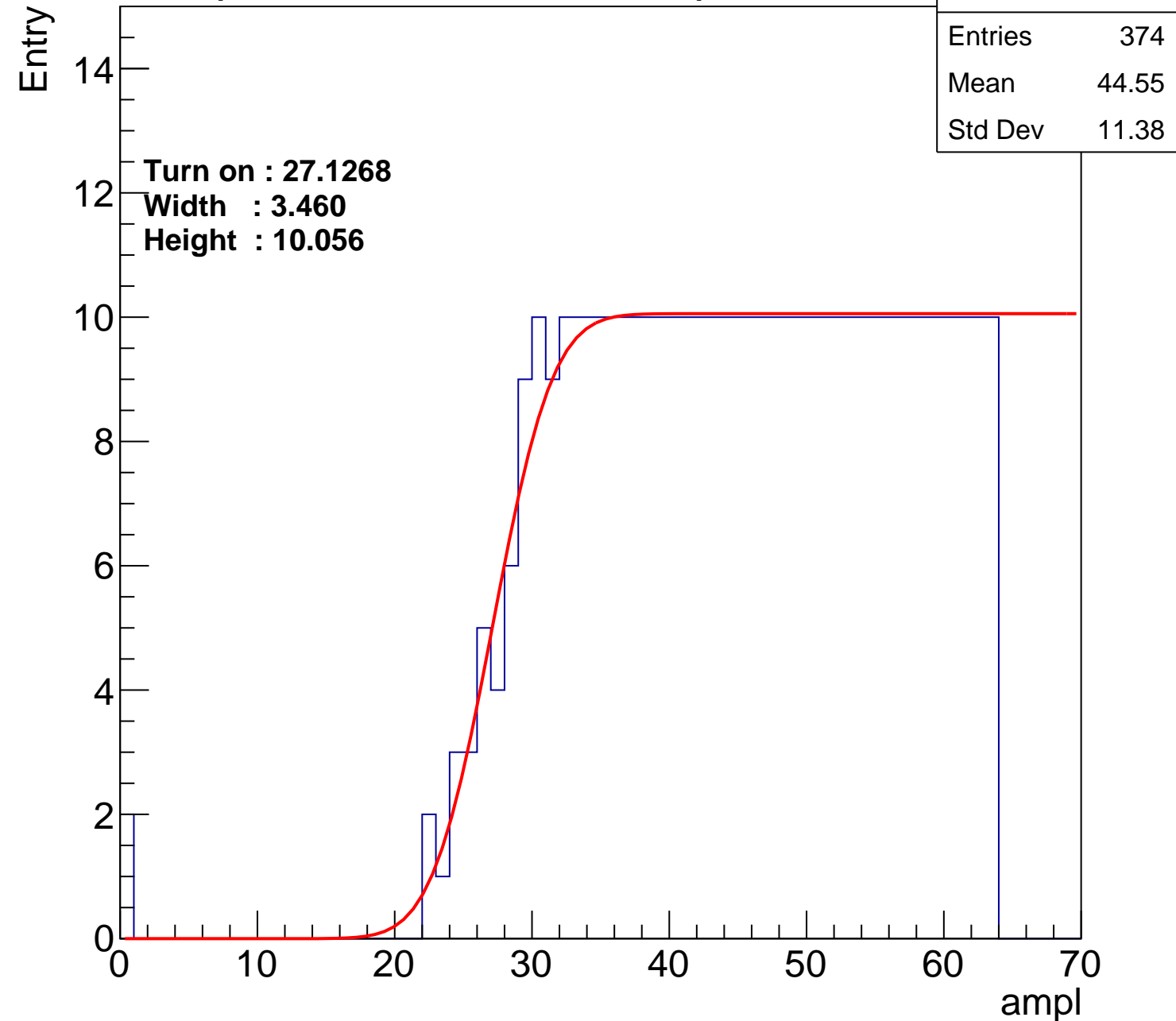
Width : 3.460

Height : 10.056

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch90

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	392
Mean	43.66
Std Dev	11.85

Turn on : 25.0170

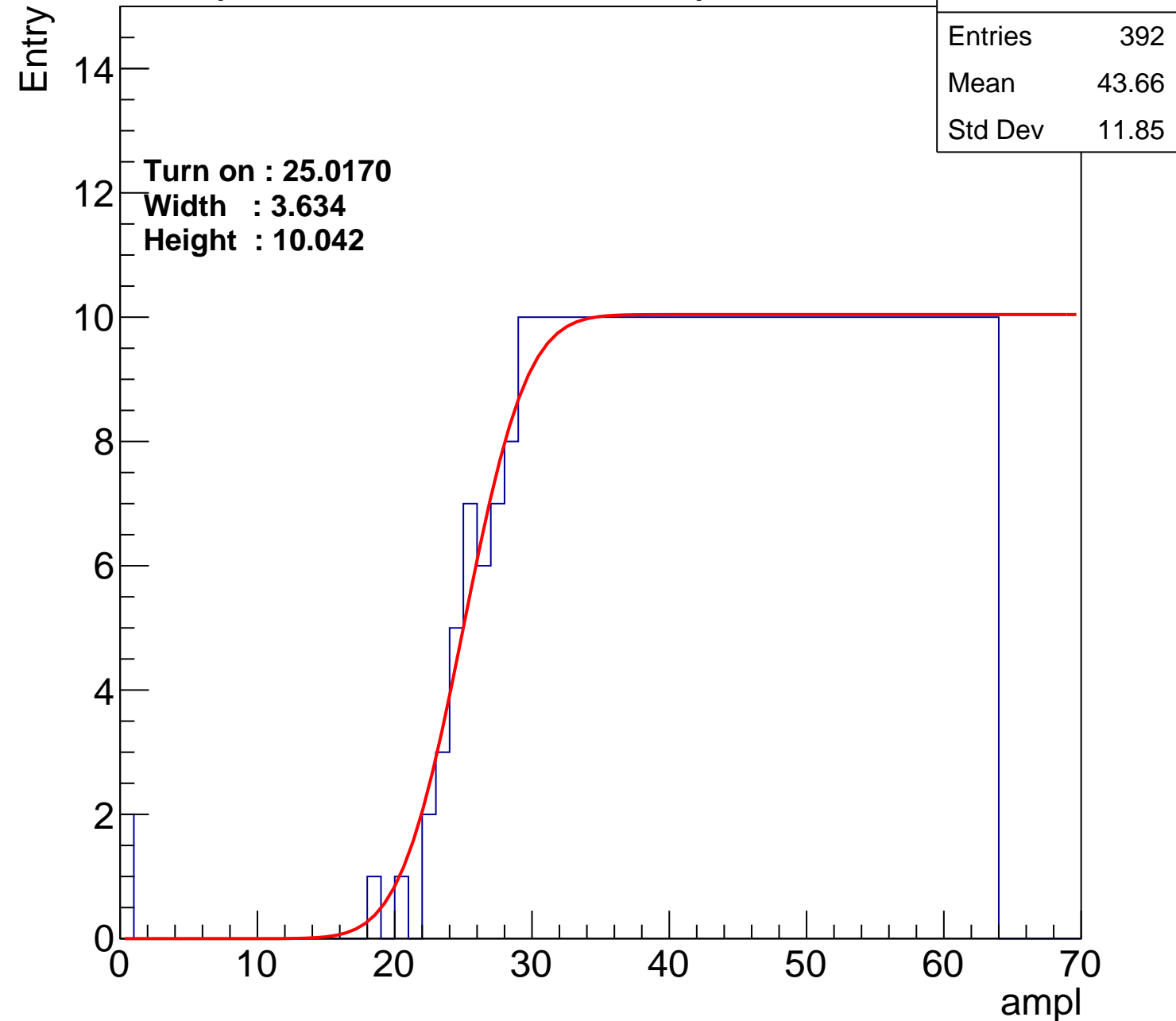
Width : 3.634

Height : 10.042

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch91

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	387
Mean	43.76
Std Dev	12.08

Turn on : 25.9895

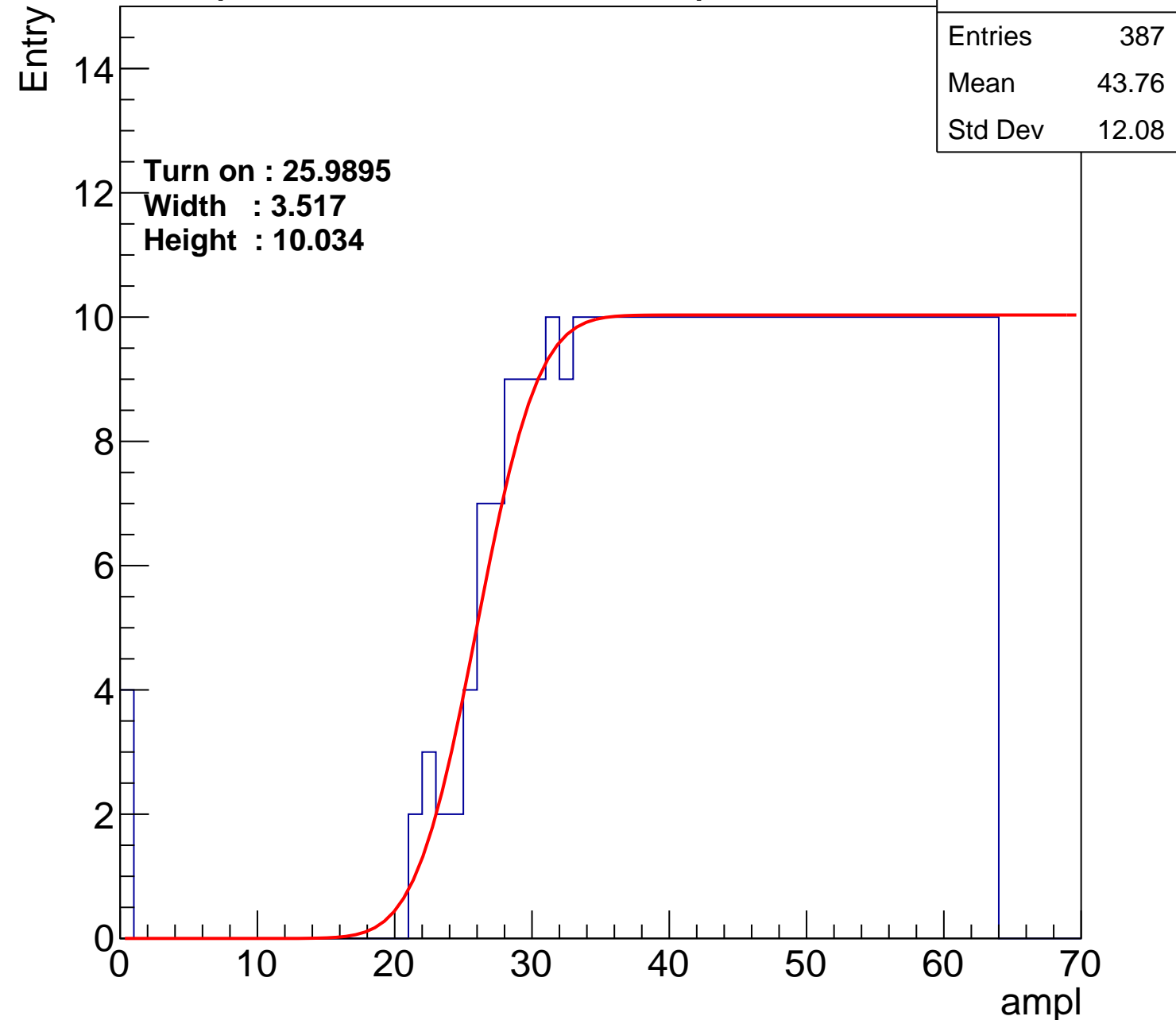
Width : 3.517

Height : 10.034

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch92

calib\_packv5\_042523\_0143.root, FC#4, port A2

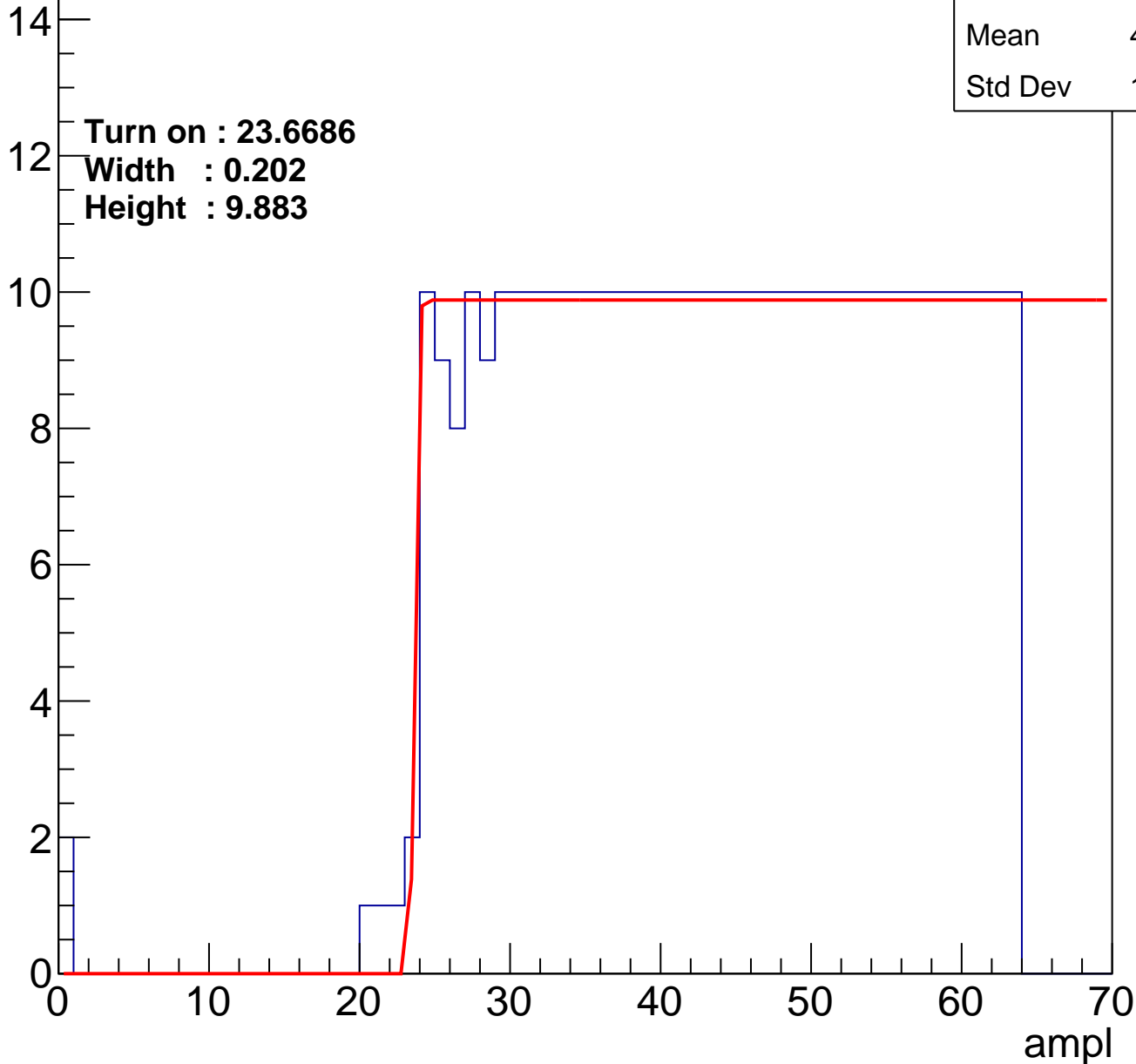
Entry

Entries	403
Mean	43.19
Std Dev	12.02

Turn on : 23.6686

Width : 0.202

Height : 9.883



# B1L100S, U7-ch93

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	389
Mean	43.87
Std Dev	11.59

Turn on : 25.3640

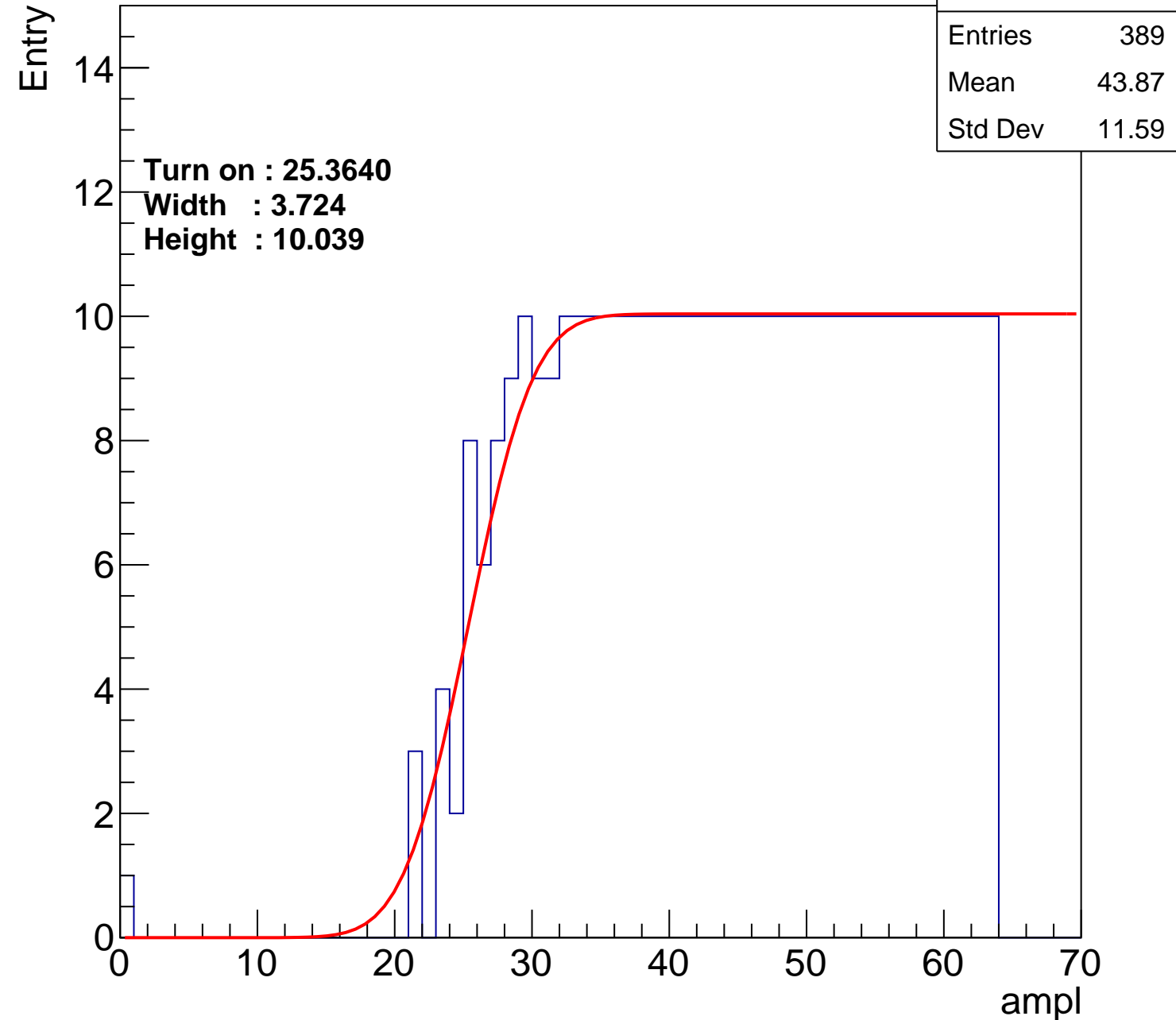
Width : 3.724

Height : 10.039

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch94

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	369
Mean	44.78
Std Dev	11.28

Turn on : 27.4755

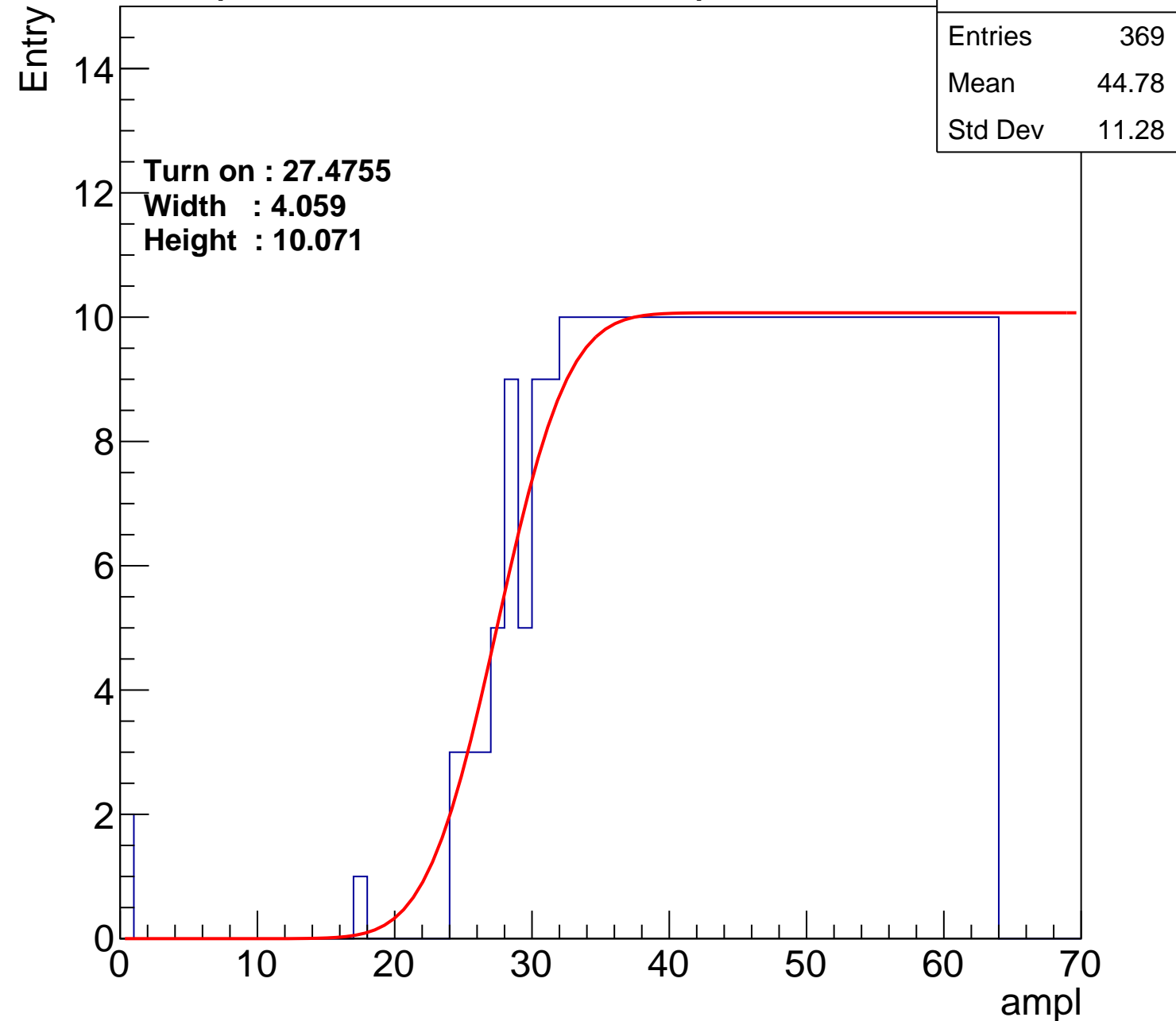
Width : 4.059

Height : 10.071

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L100S, U7-ch95

calib\_packv5\_042523\_0143.root, FC#4, port A2

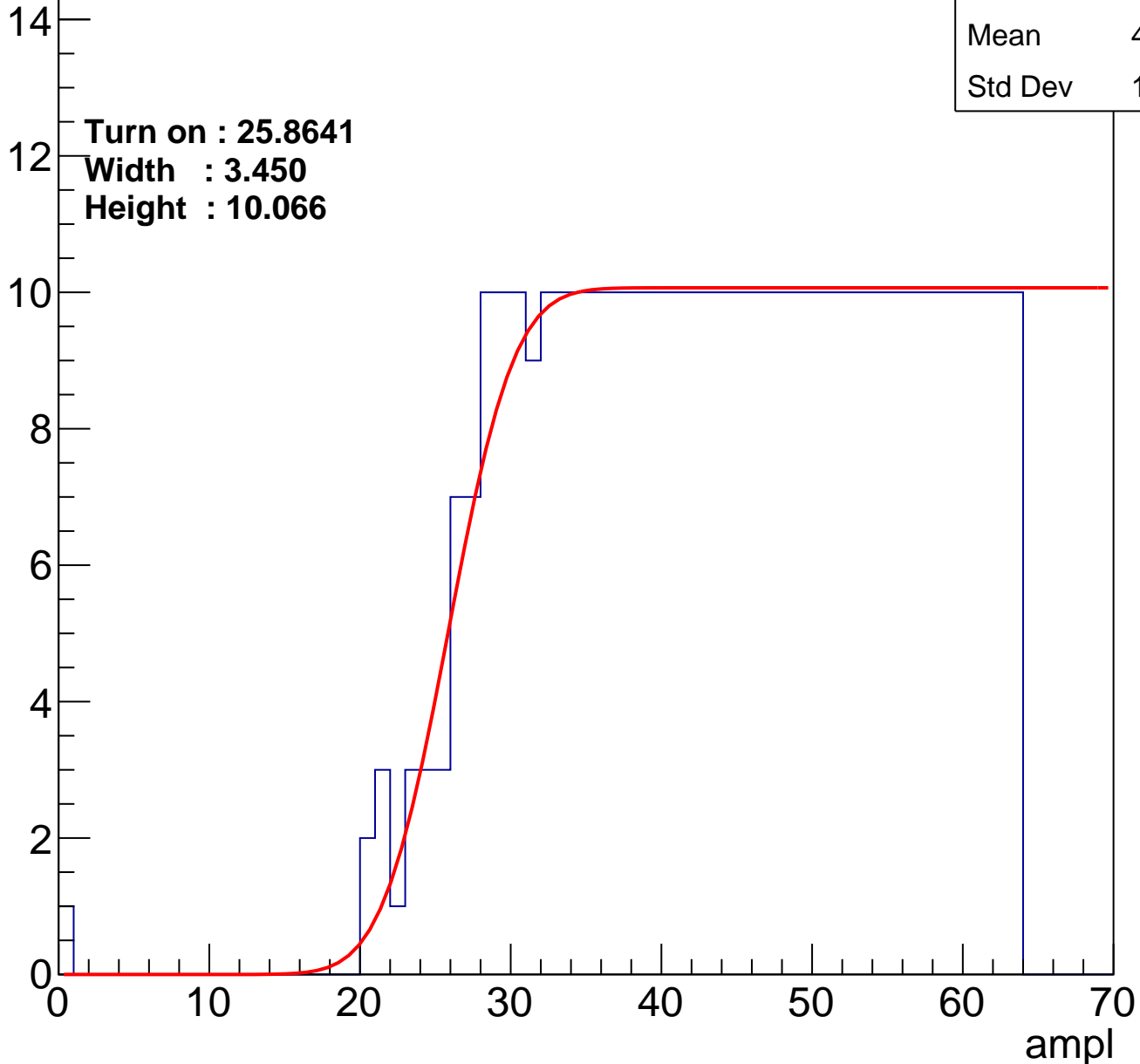
Entries	389
Mean	43.86
Std Dev	11.62

Turn on : 25.8641

Width : 3.450

Height : 10.066

Entry



# B1L100S, U7-ch96

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	382
Mean	44.01
Std Dev	11.96

**Turn on : 26.4099**

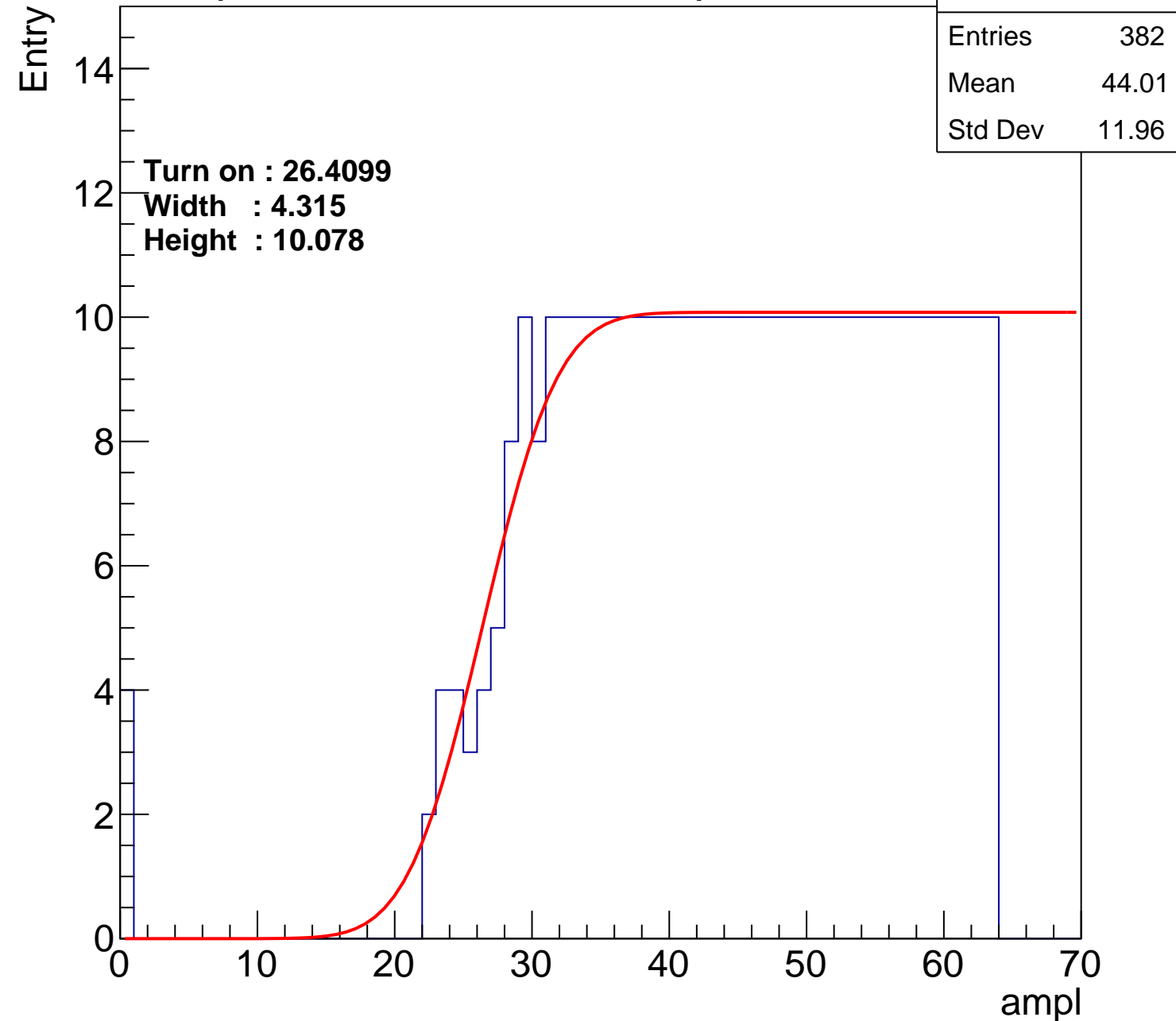
**Width : 4.315**

**Height : 10.078**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch97

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	383
Mean	44.04
Std Dev	11.78

Turn on : 26.4581

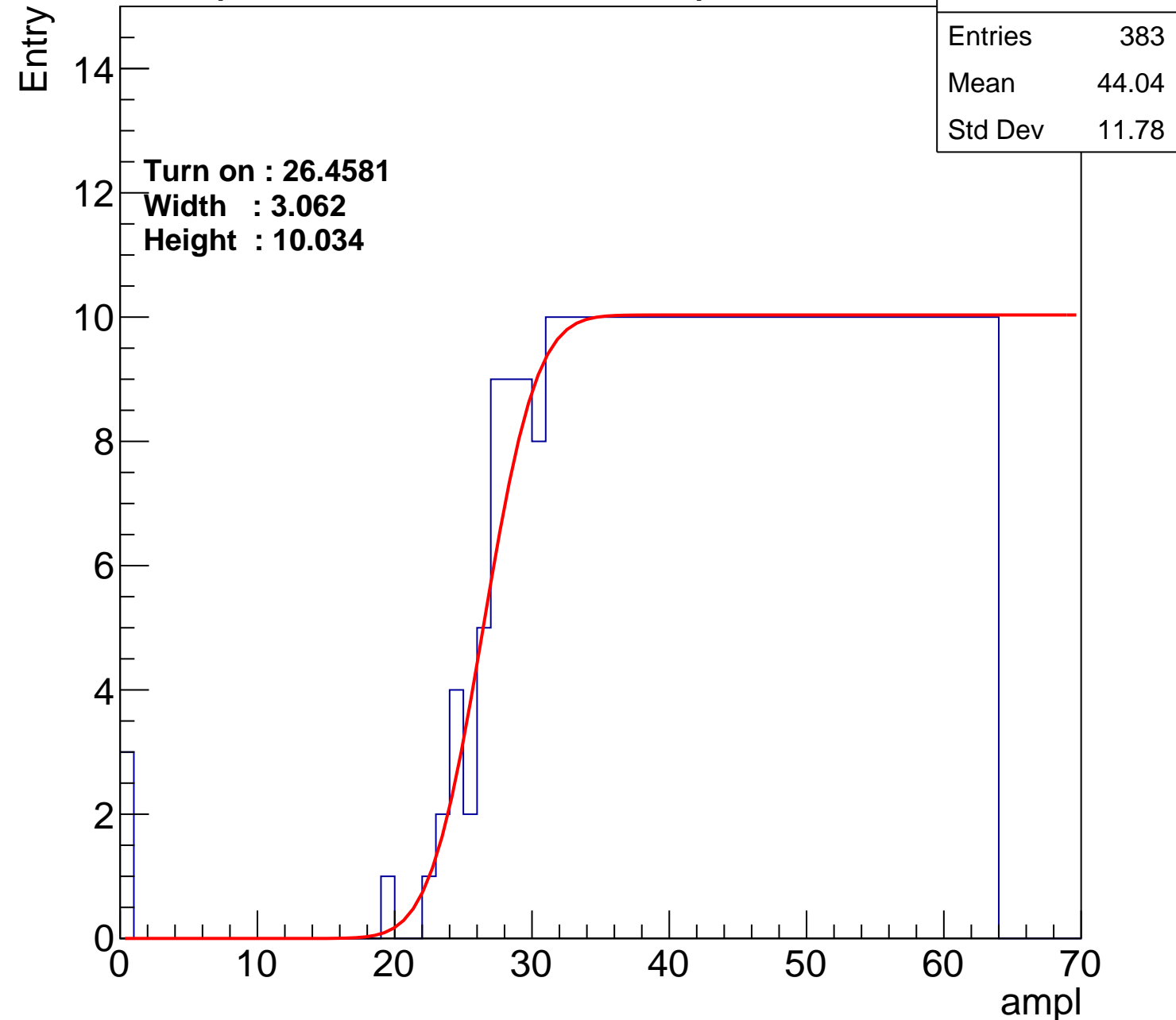
Width : 3.062

Height : 10.034

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch98

calib\_packv5\_042523\_0143.root, FC#4, port A2

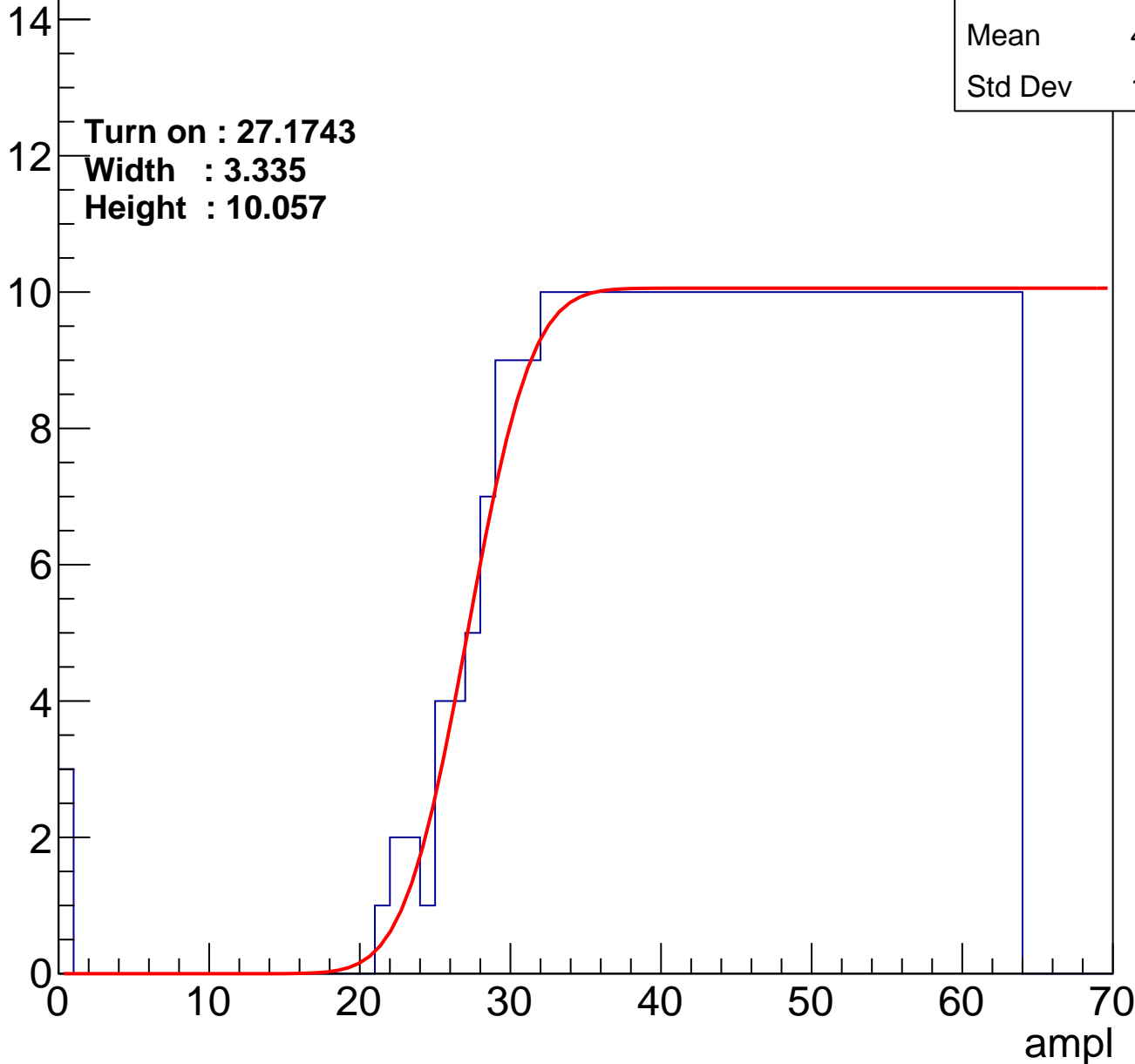
Entries	376
Mean	44.36
Std Dev	11.65

Turn on : 27.1743

Width : 3.335

Height : 10.057

Entry



# B1L100S, U7-ch99

calib\_packv5\_042523\_0143.root, FC#4, port A2

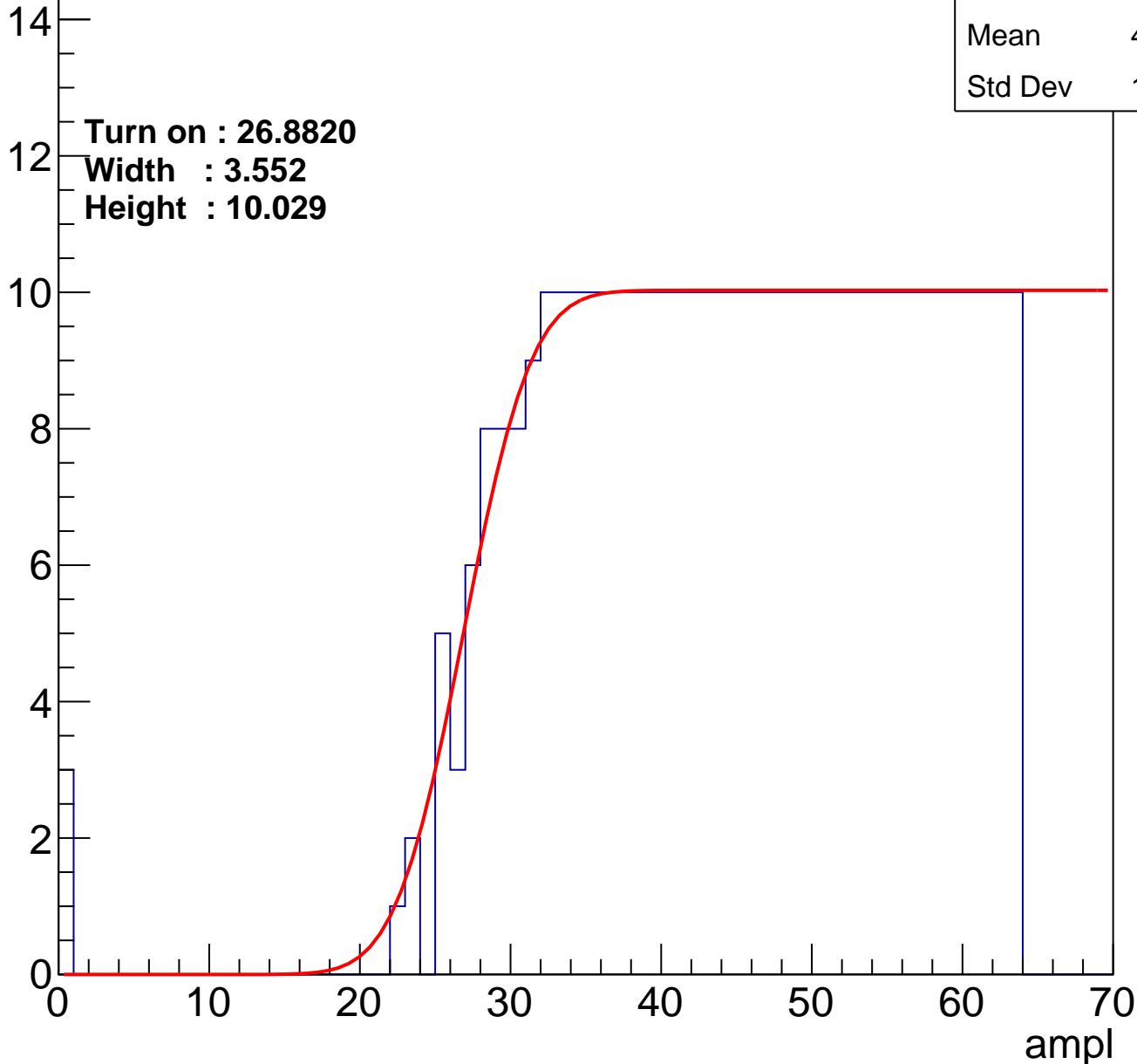
Entries	373
Mean	44.53
Std Dev	11.55

**Turn on : 26.8820**

**Width : 3.552**

**Height : 10.029**

Entry



# B1L100S, U7-ch100

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	384
Mean	43.91
Std Dev	12.01

Turn on : 26.0914

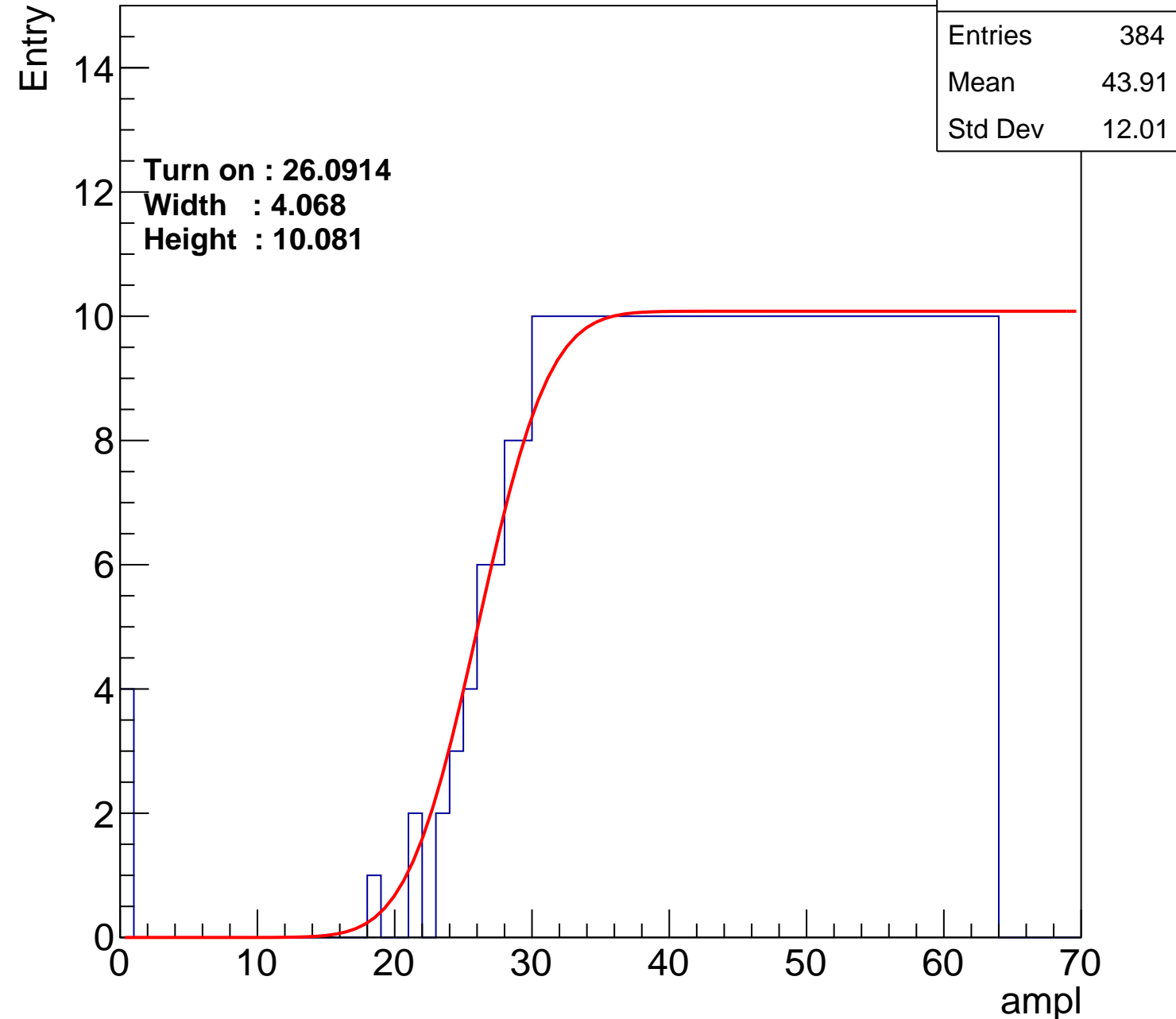
Width : 4.068

Height : 10.081

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch101

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	377
Mean	44.38
Std Dev	11.56

Turn on : 26.5749

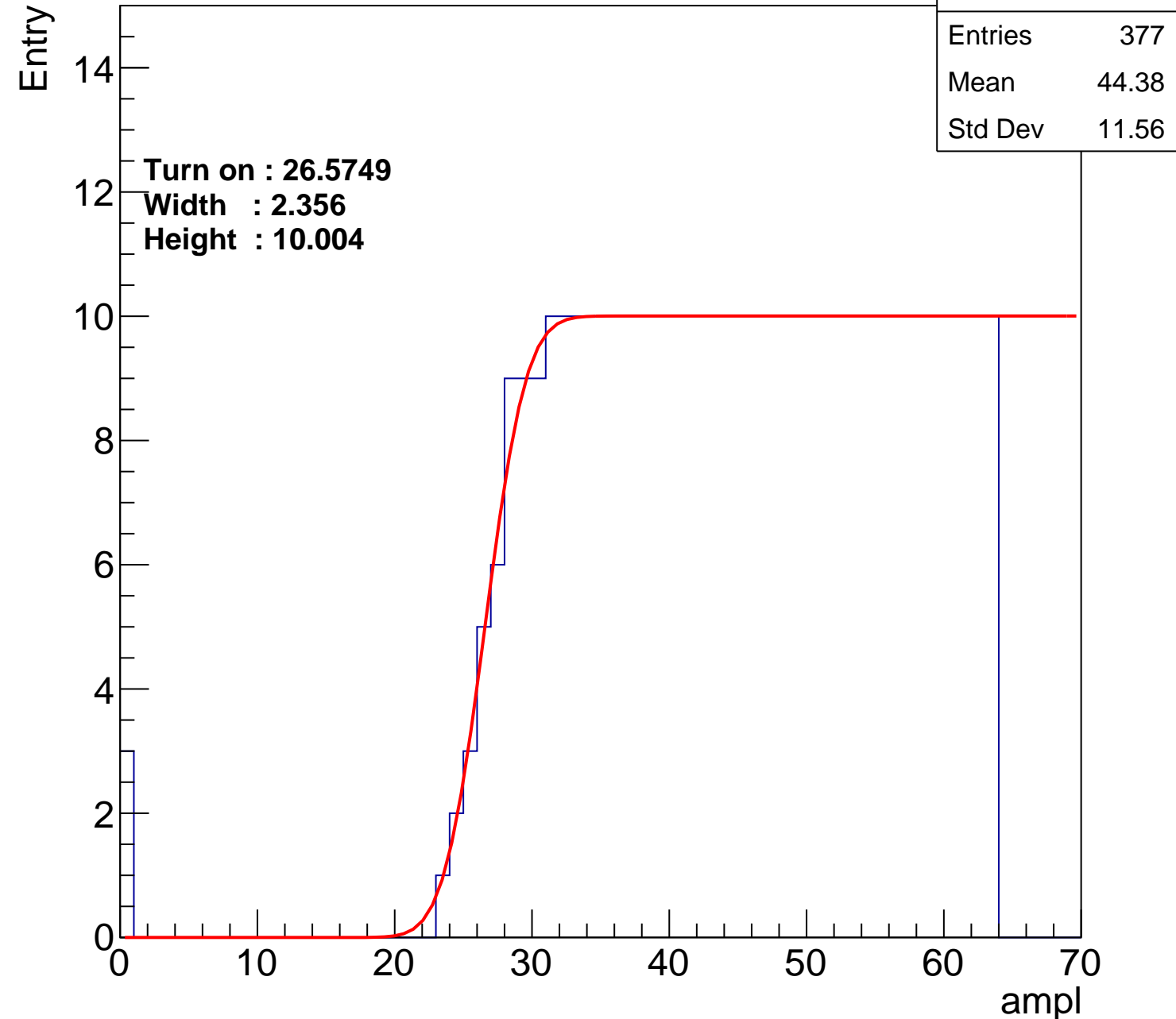
Width : 2.356

Height : 10.004

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch102

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	369
Mean	44.86
Std Dev	11.06

Turn on : 27.2820

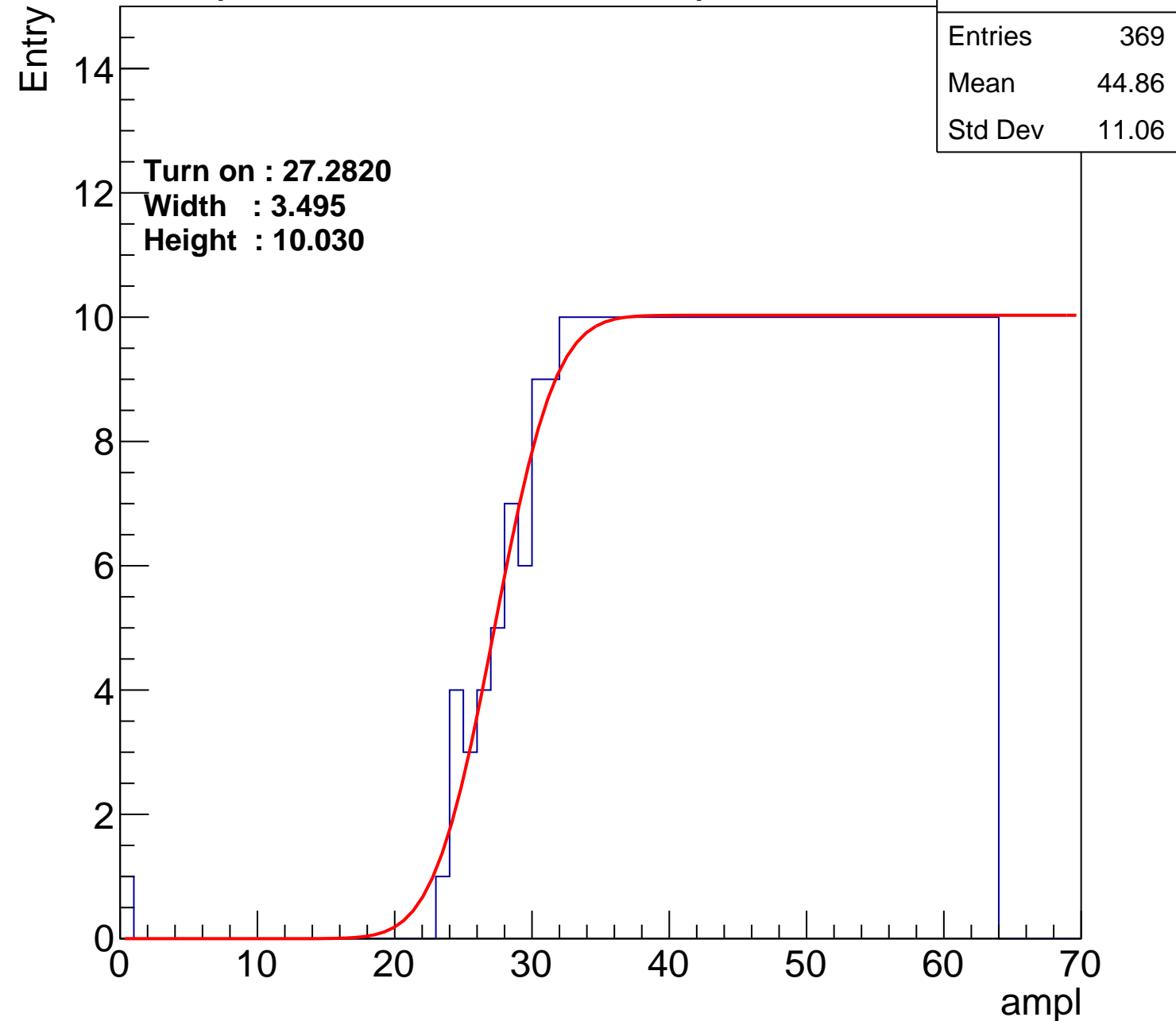
Width : 3.495

Height : 10.030

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L100S, U7-ch103

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	364
Mean	45.12
Std Dev	10.91

Turn on : 28.1843

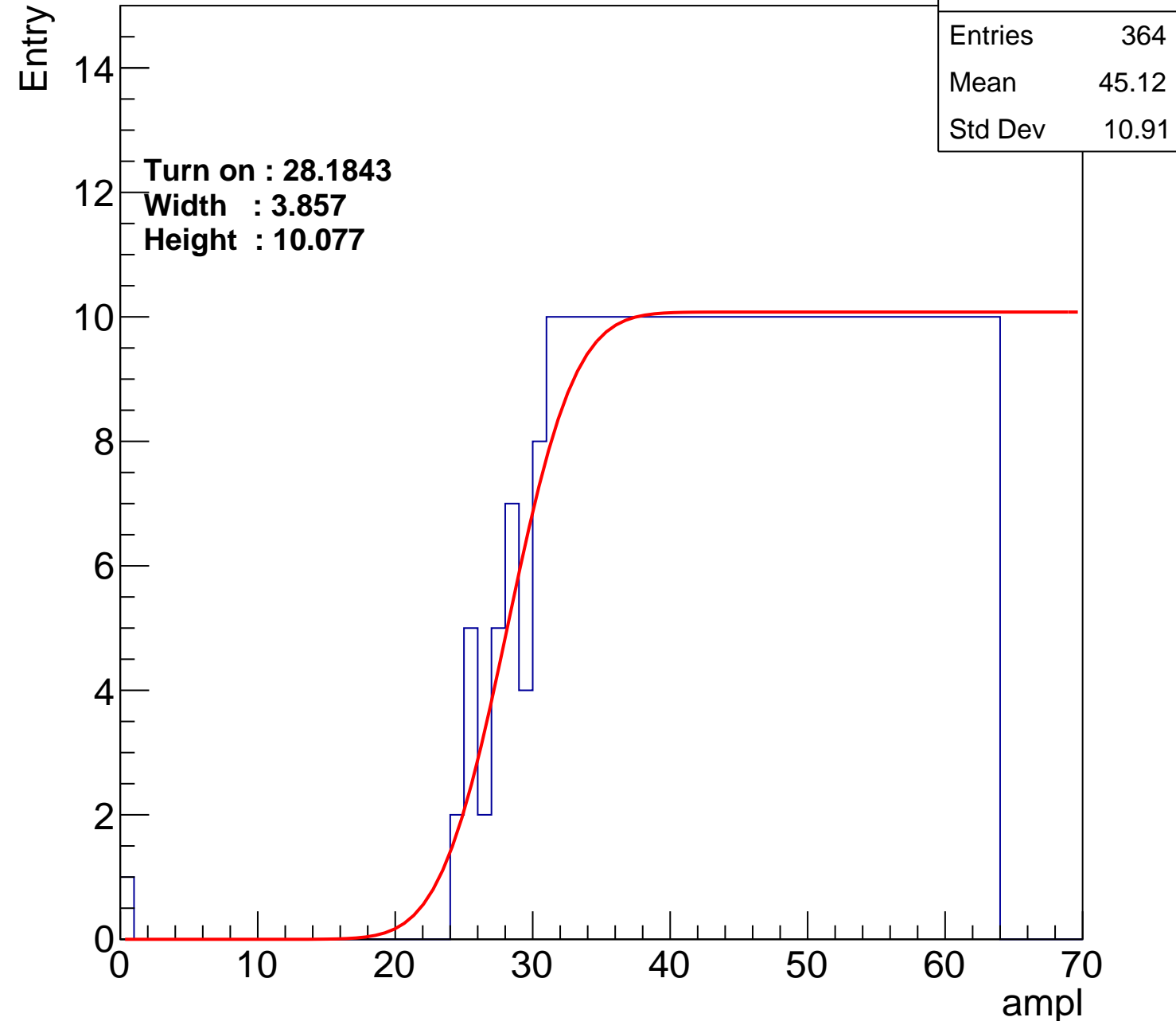
Width : 3.857

Height : 10.077

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch104

calib\_packv5\_042523\_0143.root, FC#4, port A2

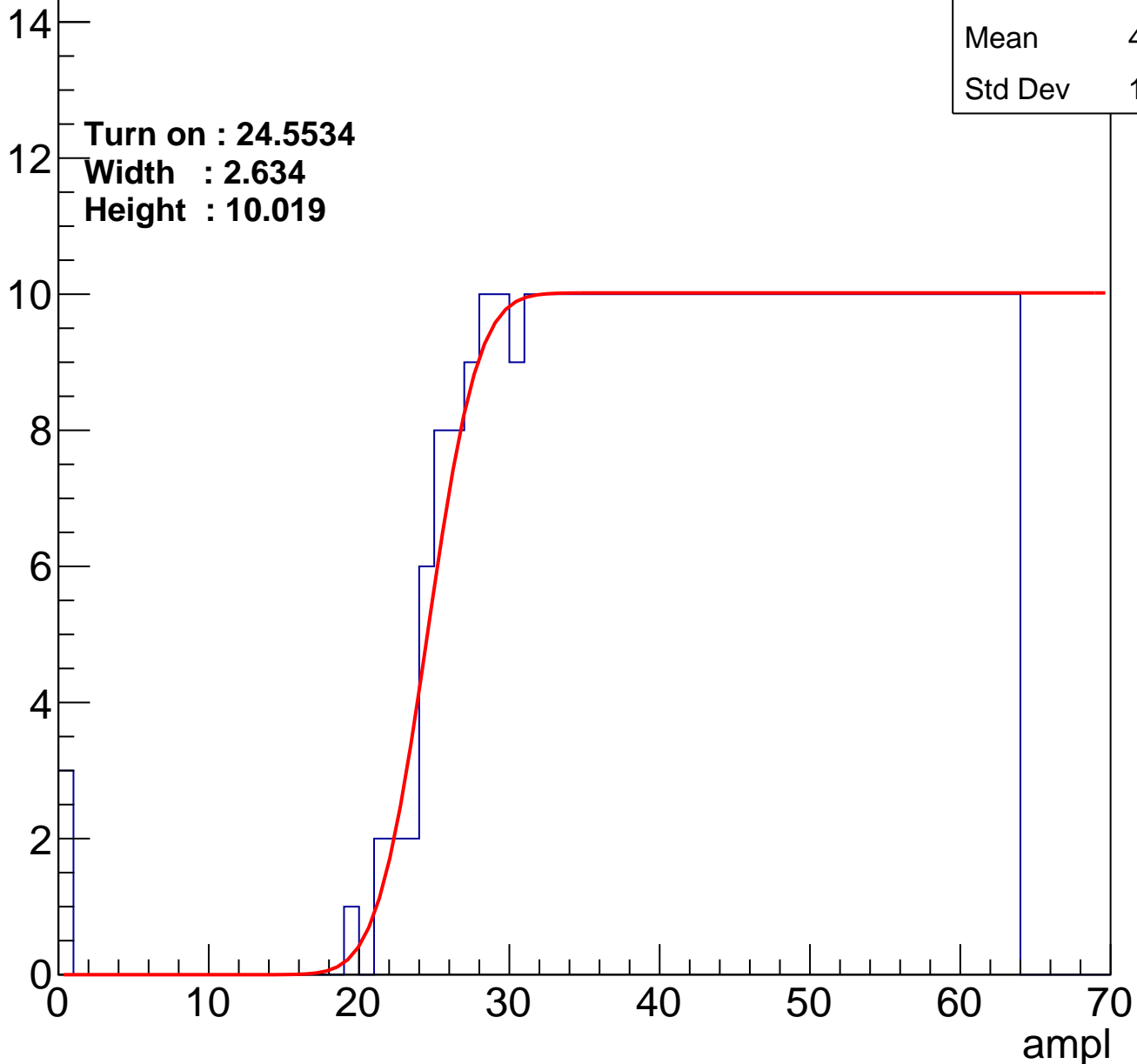
Entries	400
Mean	43.24
Std Dev	12.15

**Turn on : 24.5534**

**Width : 2.634**

**Height : 10.019**

Entry



# B1L100S, U7-ch105

calib\_packv5\_042523\_0143.root, FC#4, port A2

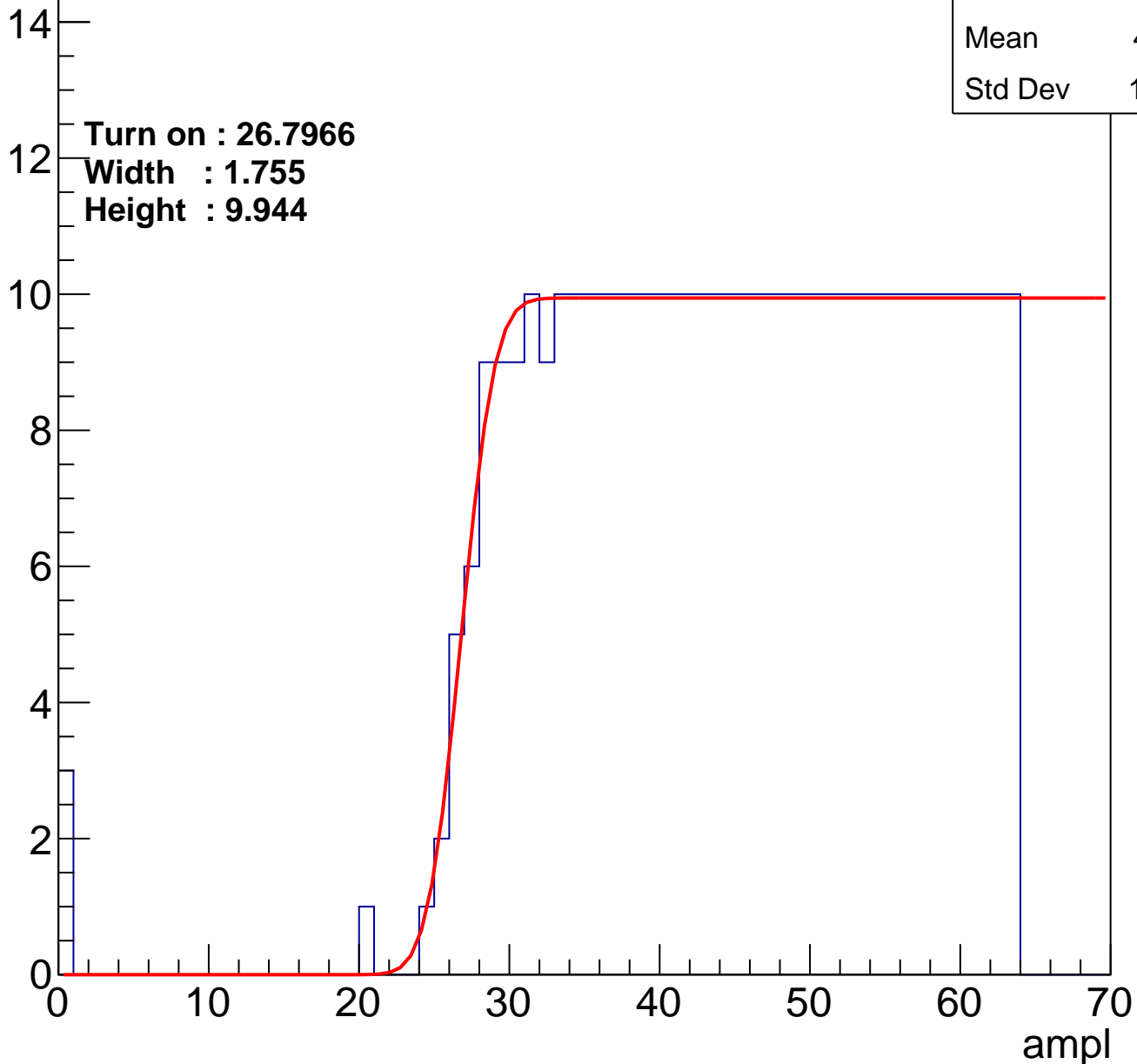
Entries	374
Mean	44.51
Std Dev	11.52

Turn on : 26.7966

Width : 1.755

Height : 9.944

Entry



# B1L100S, U7-ch106

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	363
Mean	45.17
Std Dev	10.87

Turn on : 27.9229

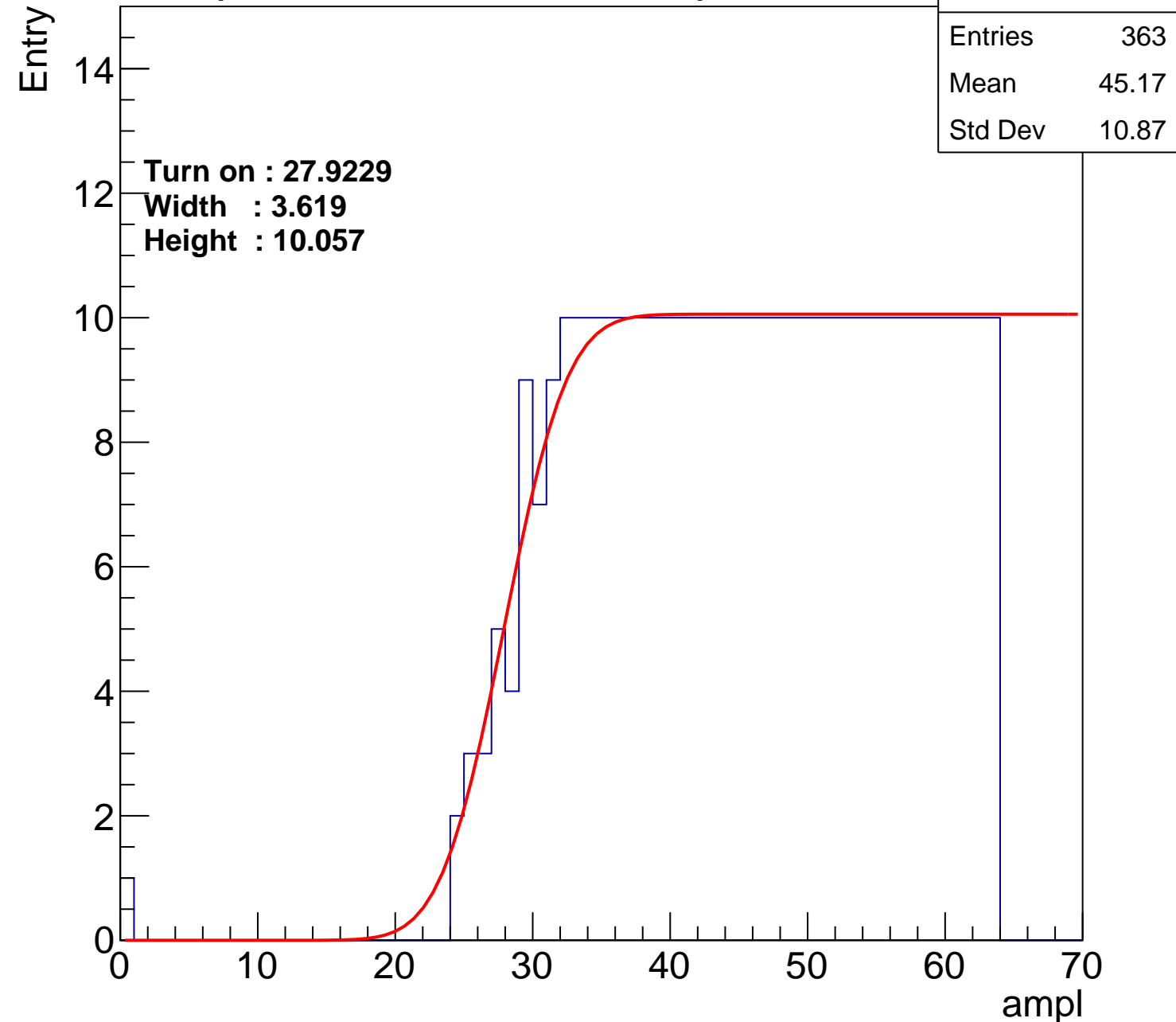
Width : 3.619

Height : 10.057

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch107

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	370
Mean	44.79
Std Dev	11.2

Turn on : 27.9418

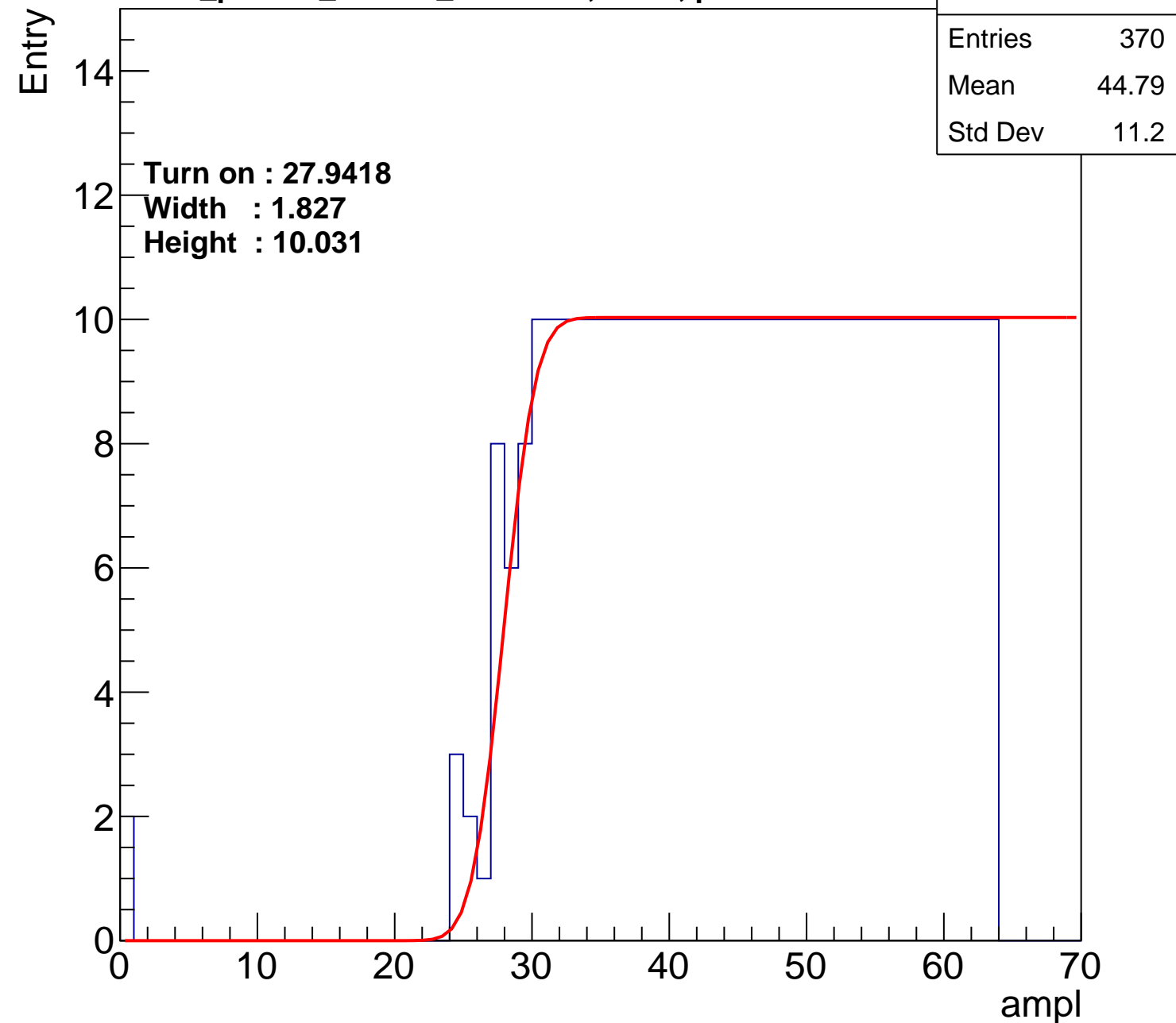
Width : 1.827

Height : 10.031

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch108

calib\_packv5\_042523\_0143.root, FC#4, port A2

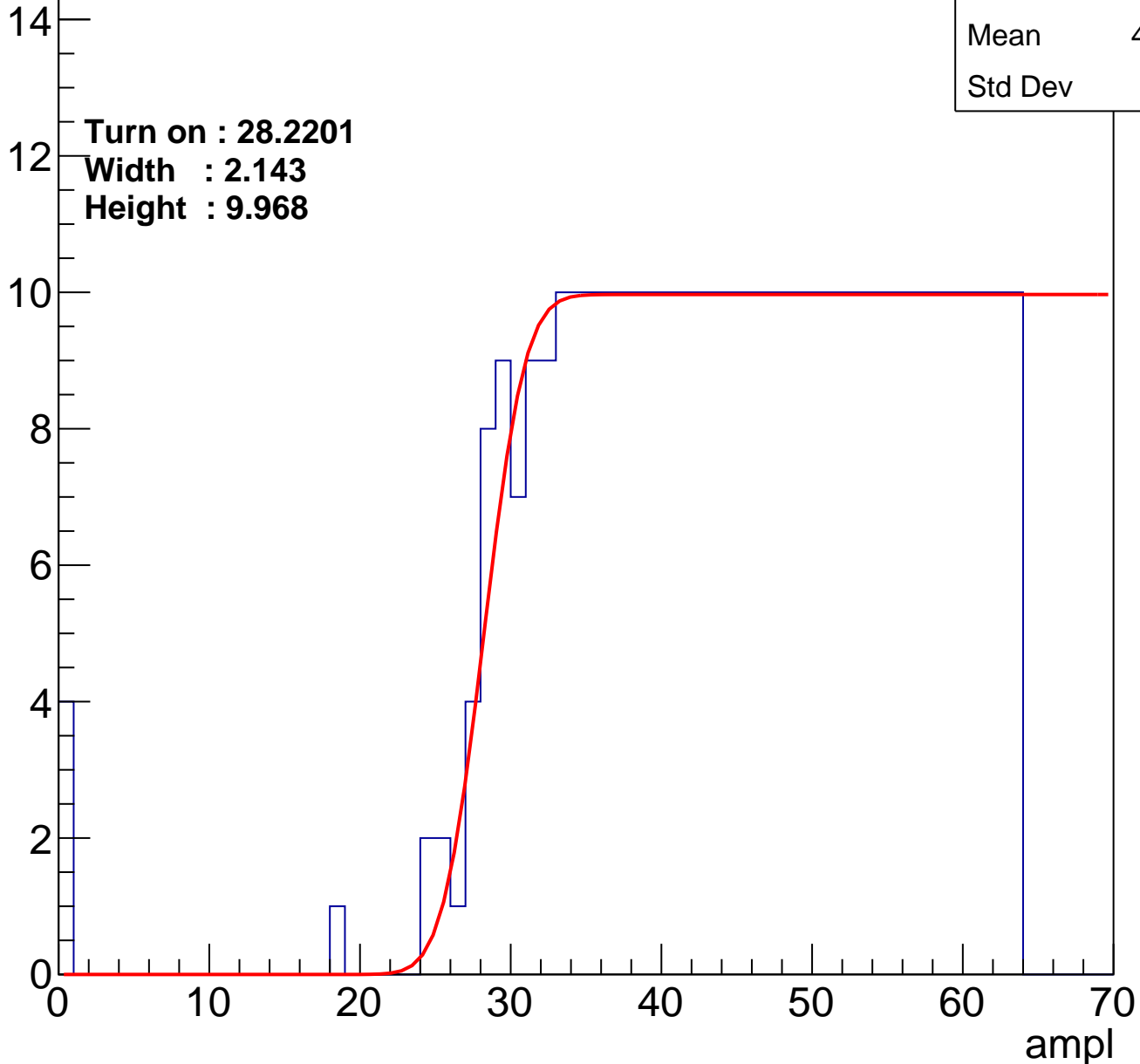
Entries	366
Mean	44.79
Std Dev	11.6

Turn on : 28.2201

Width : 2.143

Height : 9.968

Entry



# B1L100S, U7-ch109

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	368
Mean	44.79
Std Dev	11.4

Turn on : 27.7668

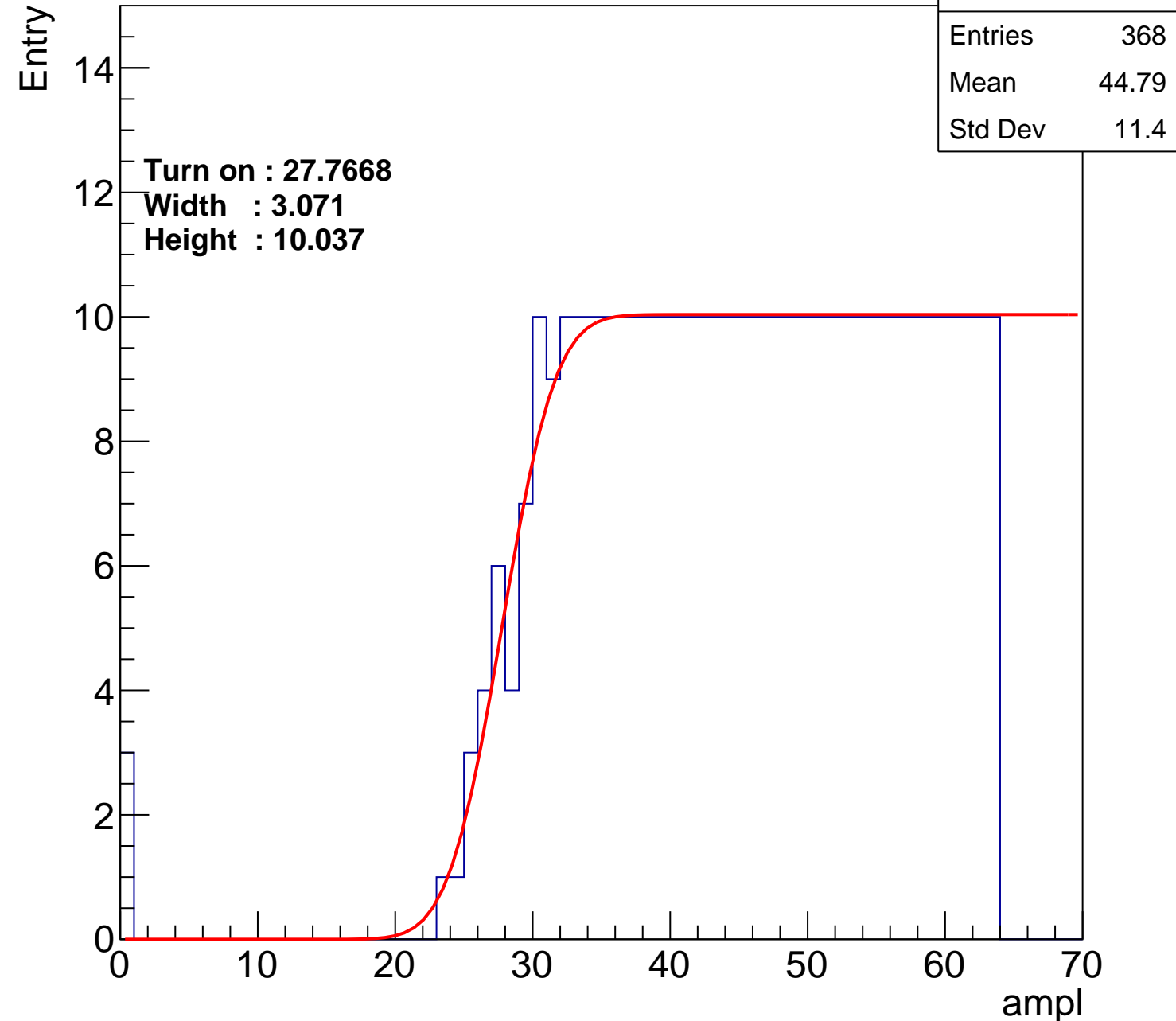
Width : 3.071

Height : 10.037

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch110

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	391
Mean	43.75
Std Dev	11.76

**Turn on : 25.6146**

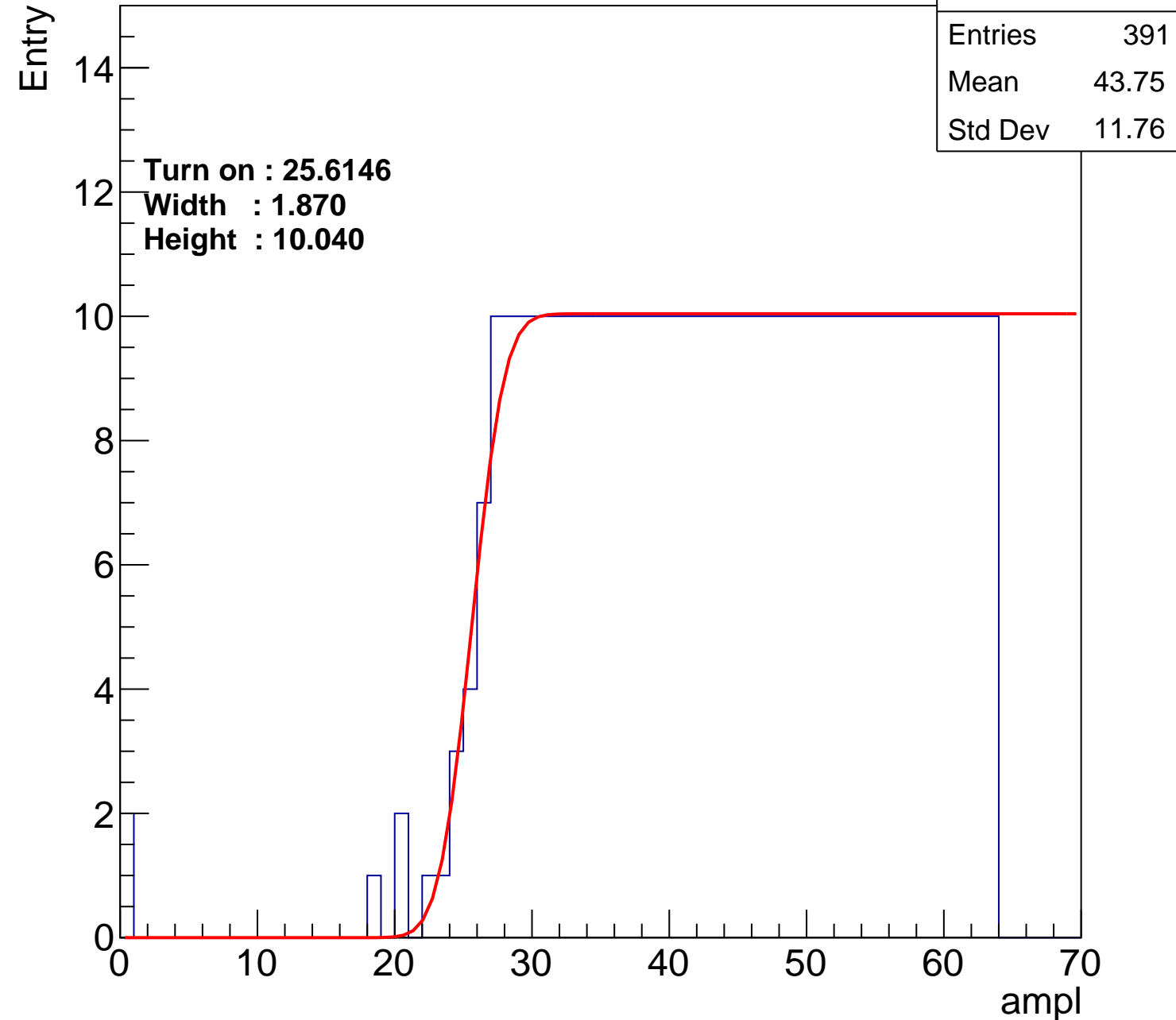
**Width : 1.870**

**Height : 10.040**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L100S, U7-ch111

calib\_packv5\_042523\_0143.root, FC#4, port A2

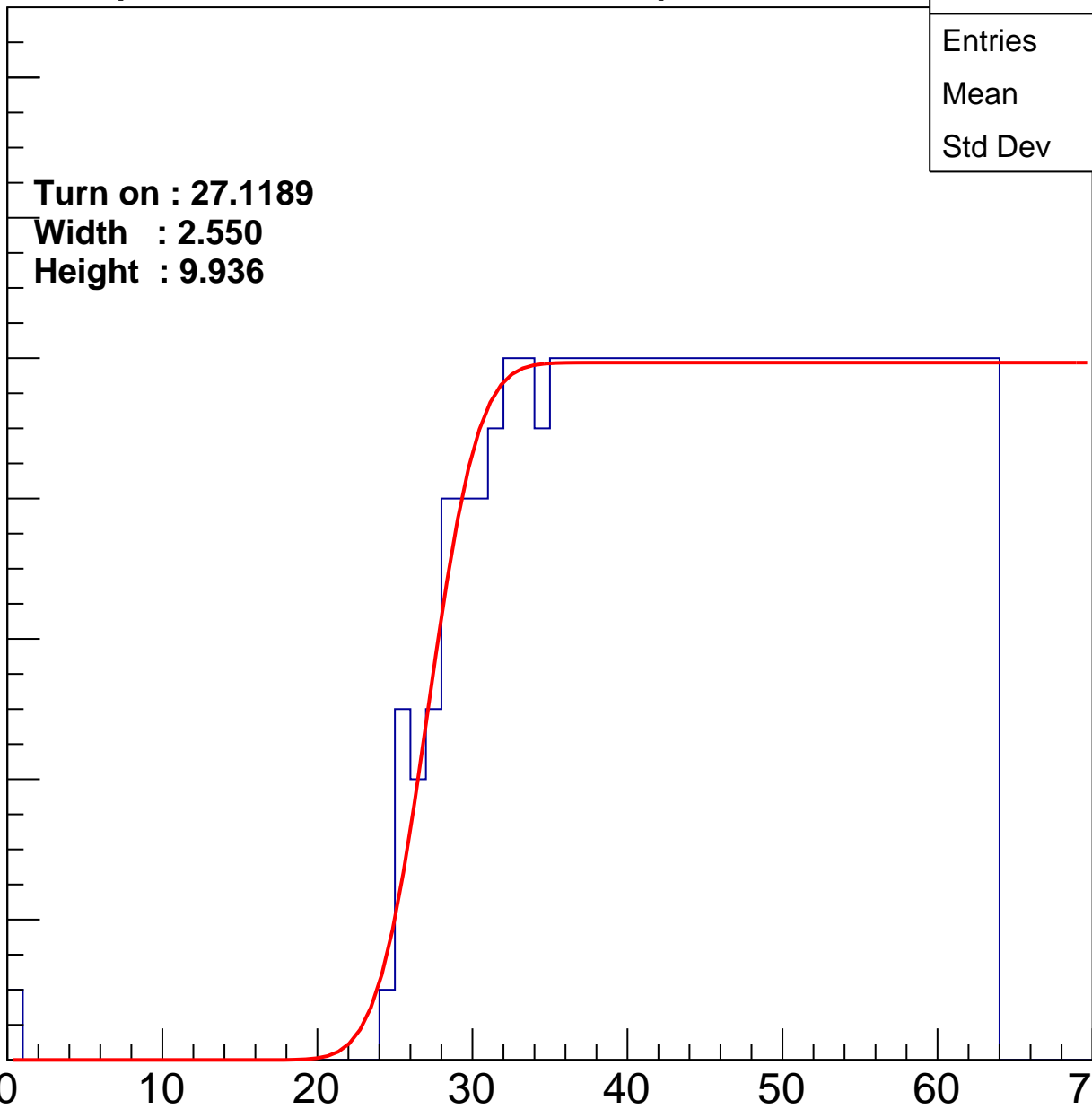
Entry

14  
12  
10  
8  
6  
4  
2  
0

Turn on : 27.1189  
Width : 2.550  
Height : 9.936

Entries	368
Mean	44.92
Std Dev	11.01

ampl



# B1L100S, U7-ch112

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	366
Mean	44.82
Std Dev	11.44

Turn on : 27.8836

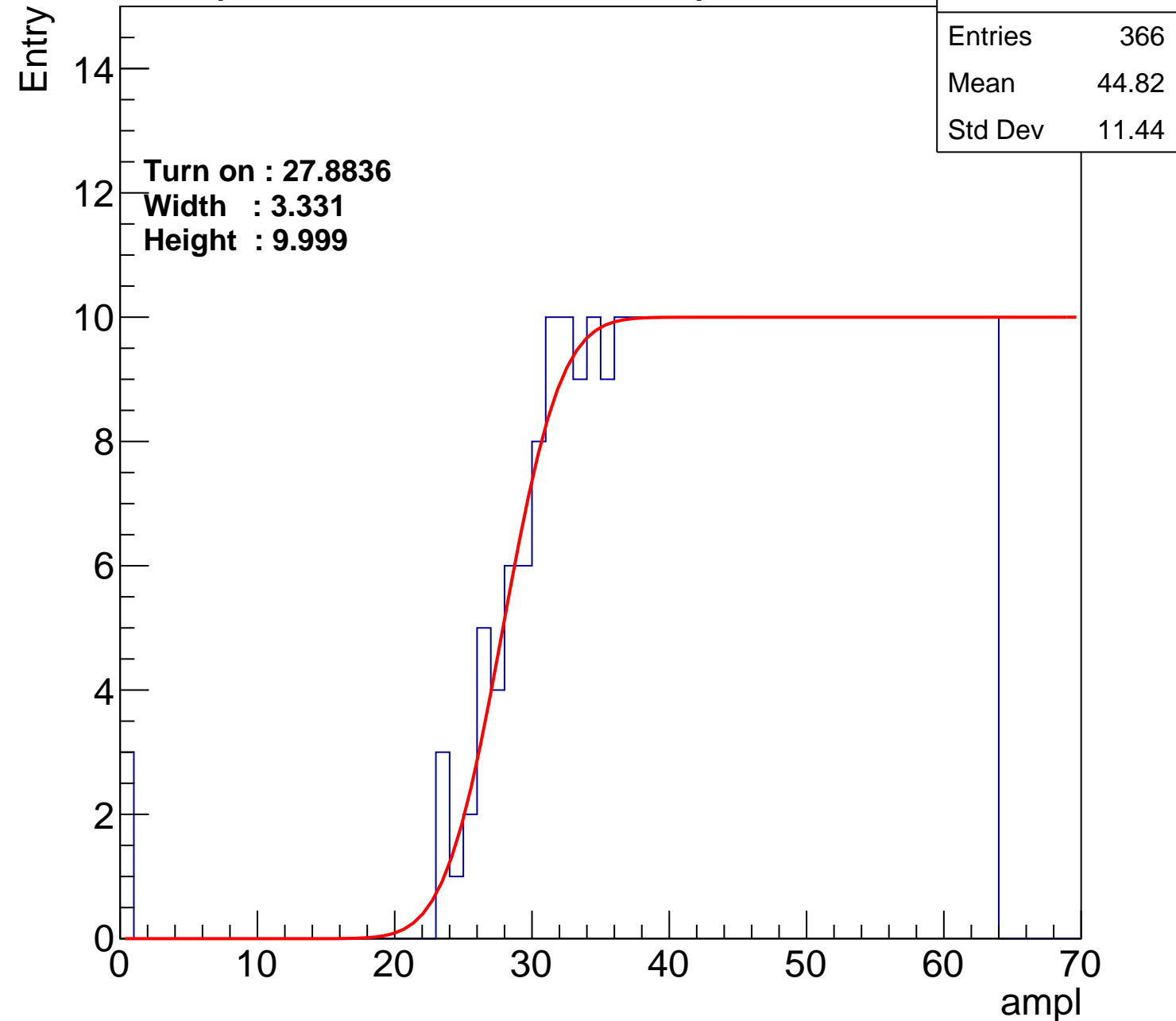
Width : 3.331

Height : 9.999

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch113

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	384
Mean	43.92
Std Dev	11.98

Turn on : 26.0138

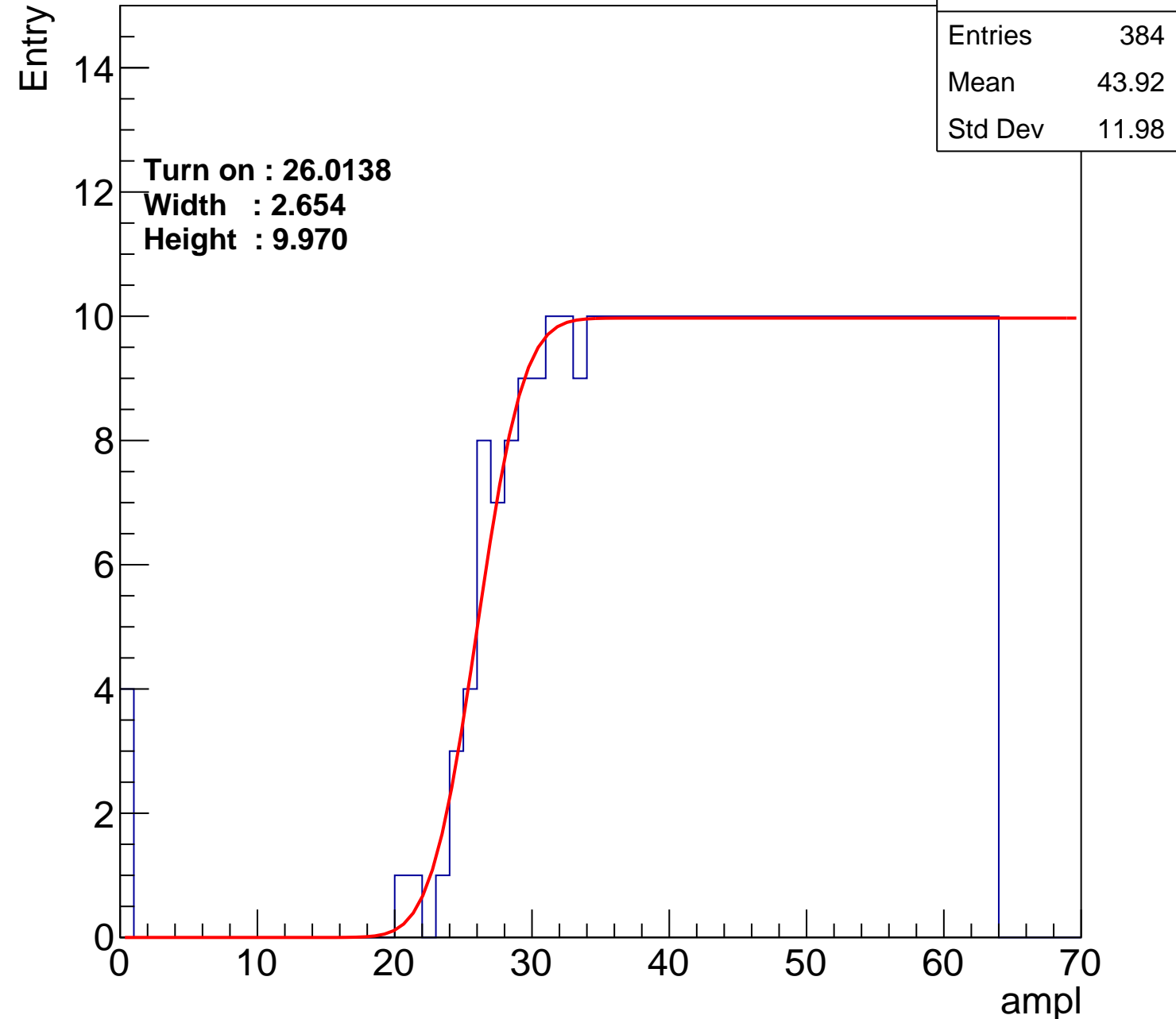
Width : 2.654

Height : 9.970

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch114

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	378
Mean	44.36
Std Dev	11.46

Turn on : 26.2218

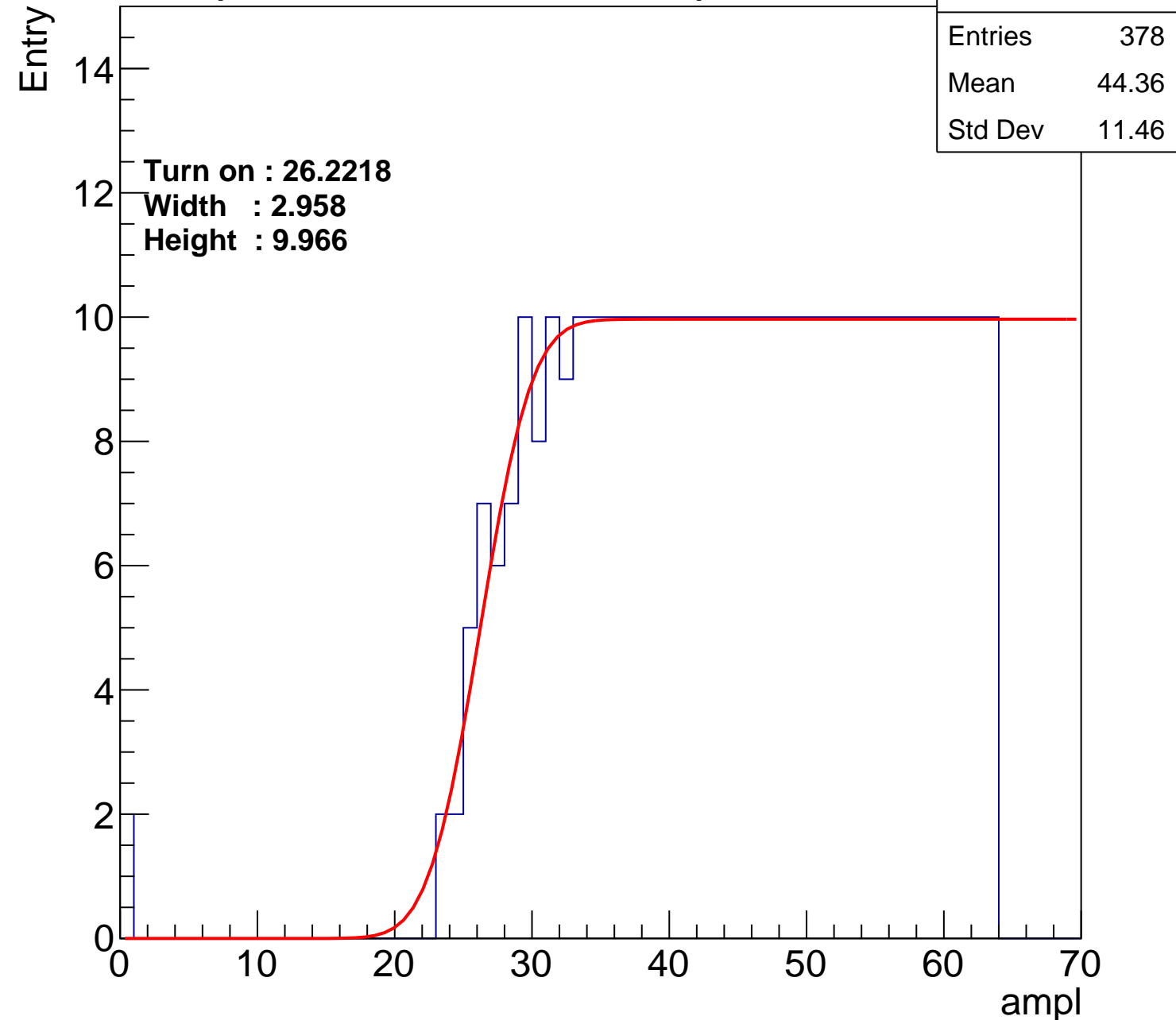
Width : 2.958

Height : 9.966

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch115

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	380
Mean	44.15
Std Dev	11.77

Turn on : 26.5113

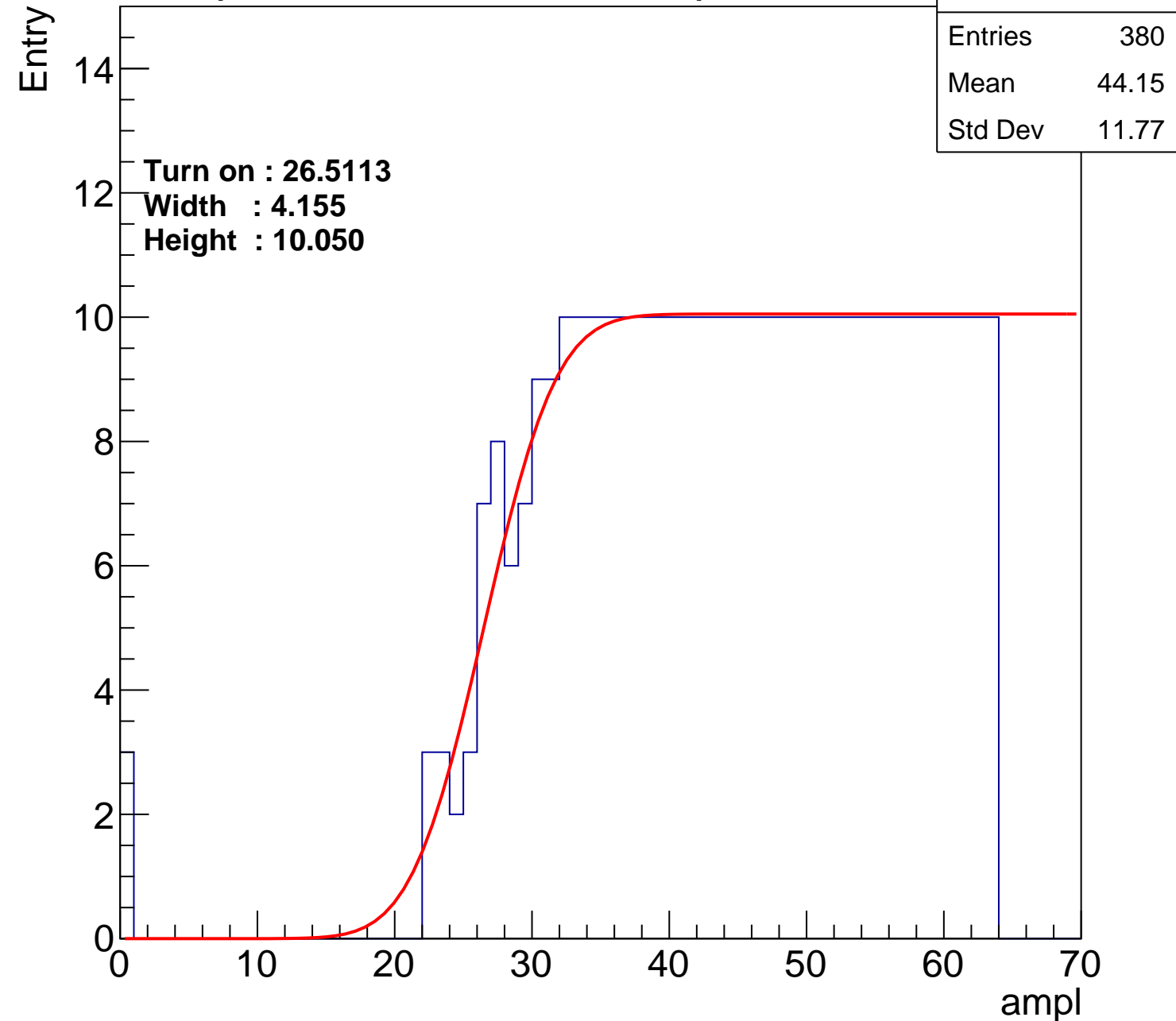
Width : 4.155

Height : 10.050

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch116

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	380
Mean	44.27
Std Dev	11.51

Turn on : 26.3644

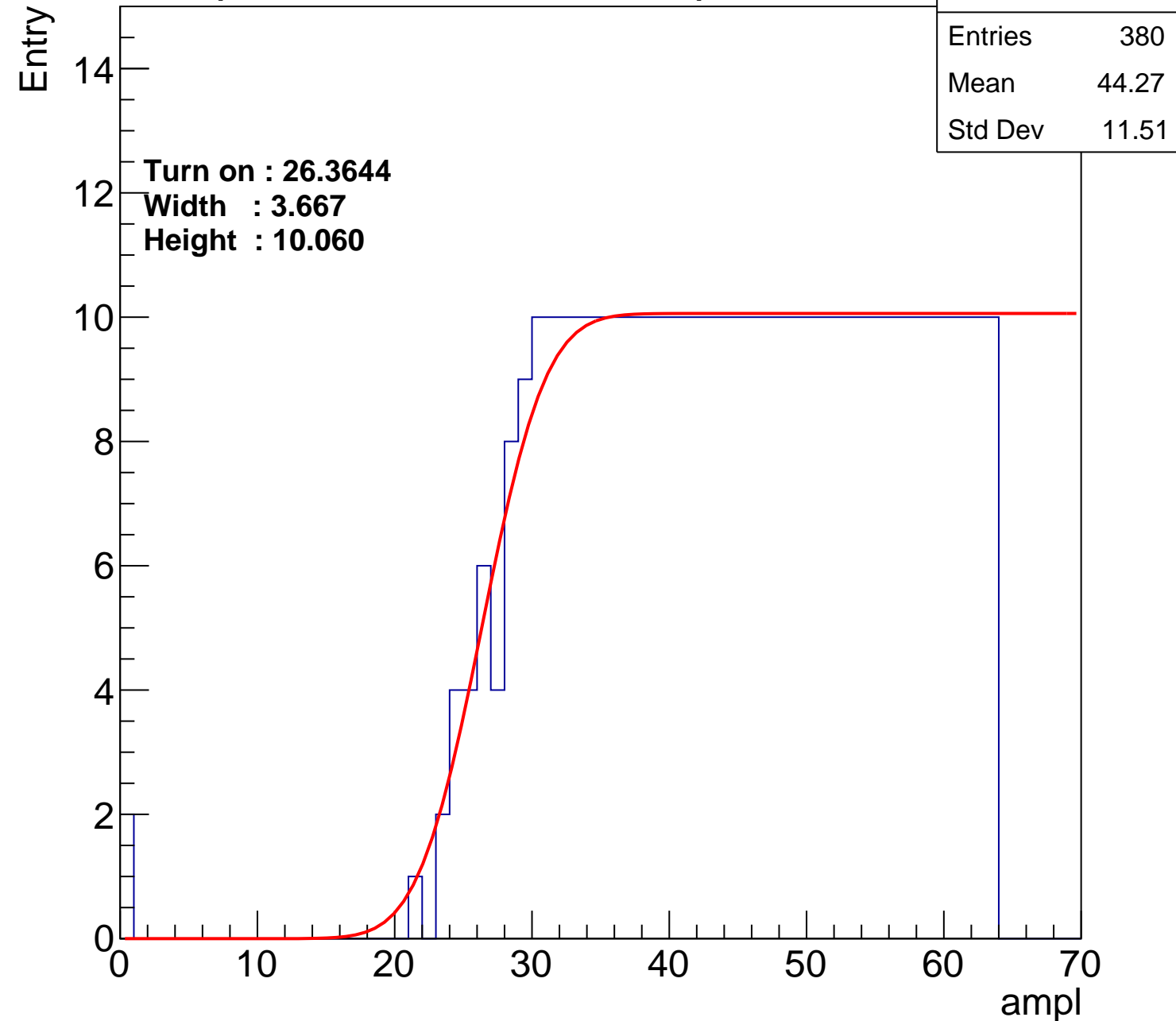
Width : 3.667

Height : 10.060

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch117

calib\_packv5\_042523\_0143.root, FC#4, port A2

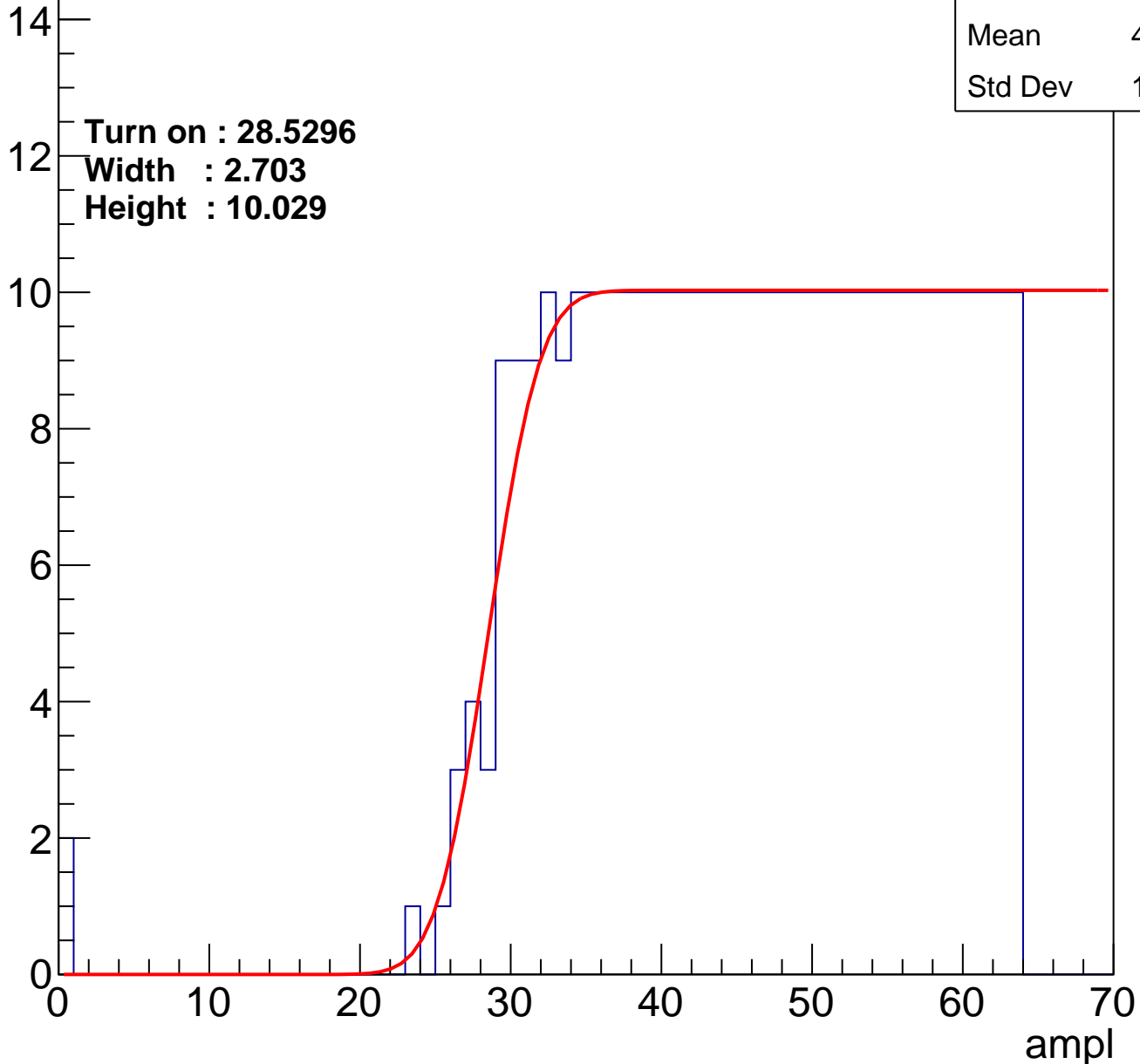
Entries	360
Mean	45.26
Std Dev	10.98

Turn on : 28.5296

Width : 2.703

Height : 10.029

Entry



# B1L100S, U7-ch118

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	395
Mean	43.47
Std Dev	12.05

Turn on : 25.0938

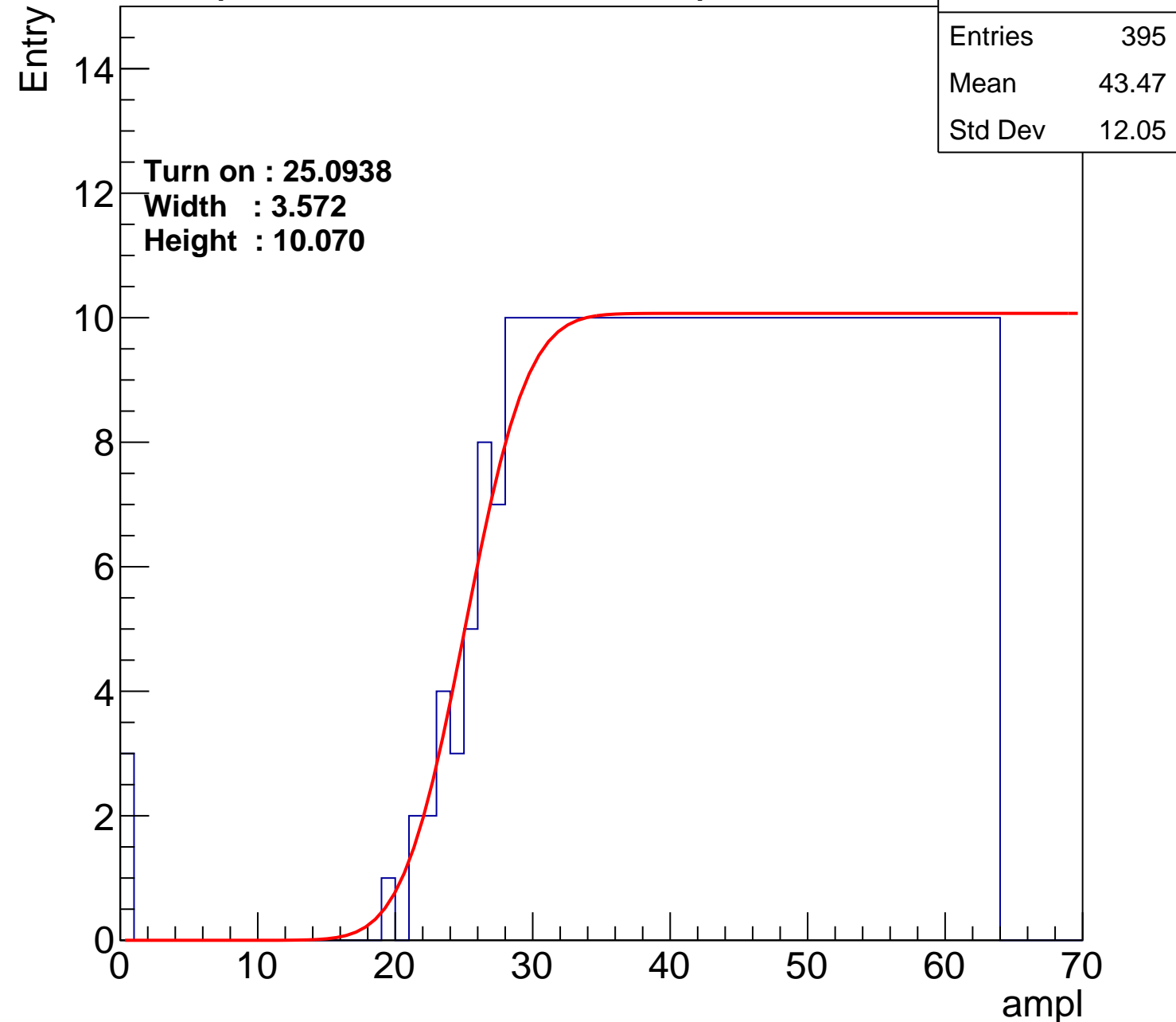
Width : 3.572

Height : 10.070

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L100S, U7-ch119

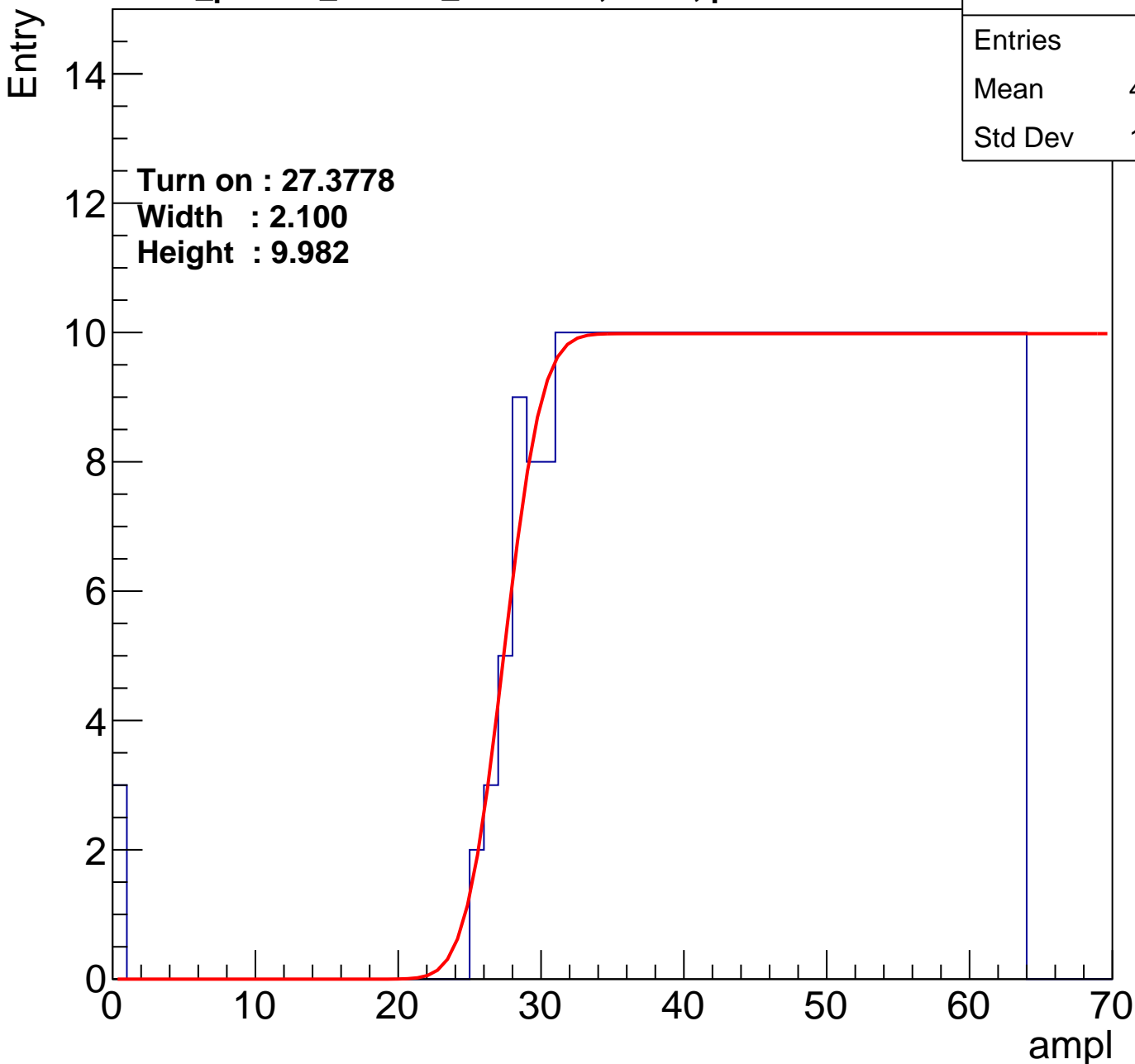
**calib\_packv5\_042523\_0143.root, FC#4, port A2**

Entries	368
Mean	44.83
Std Dev	11.33

**Turn on : 27.3778**

**Width : 2.100**

**Height : 9.982**



# B1L100S, U7-ch120

calib\_packv5\_042523\_0143.root, FC#4, port A2

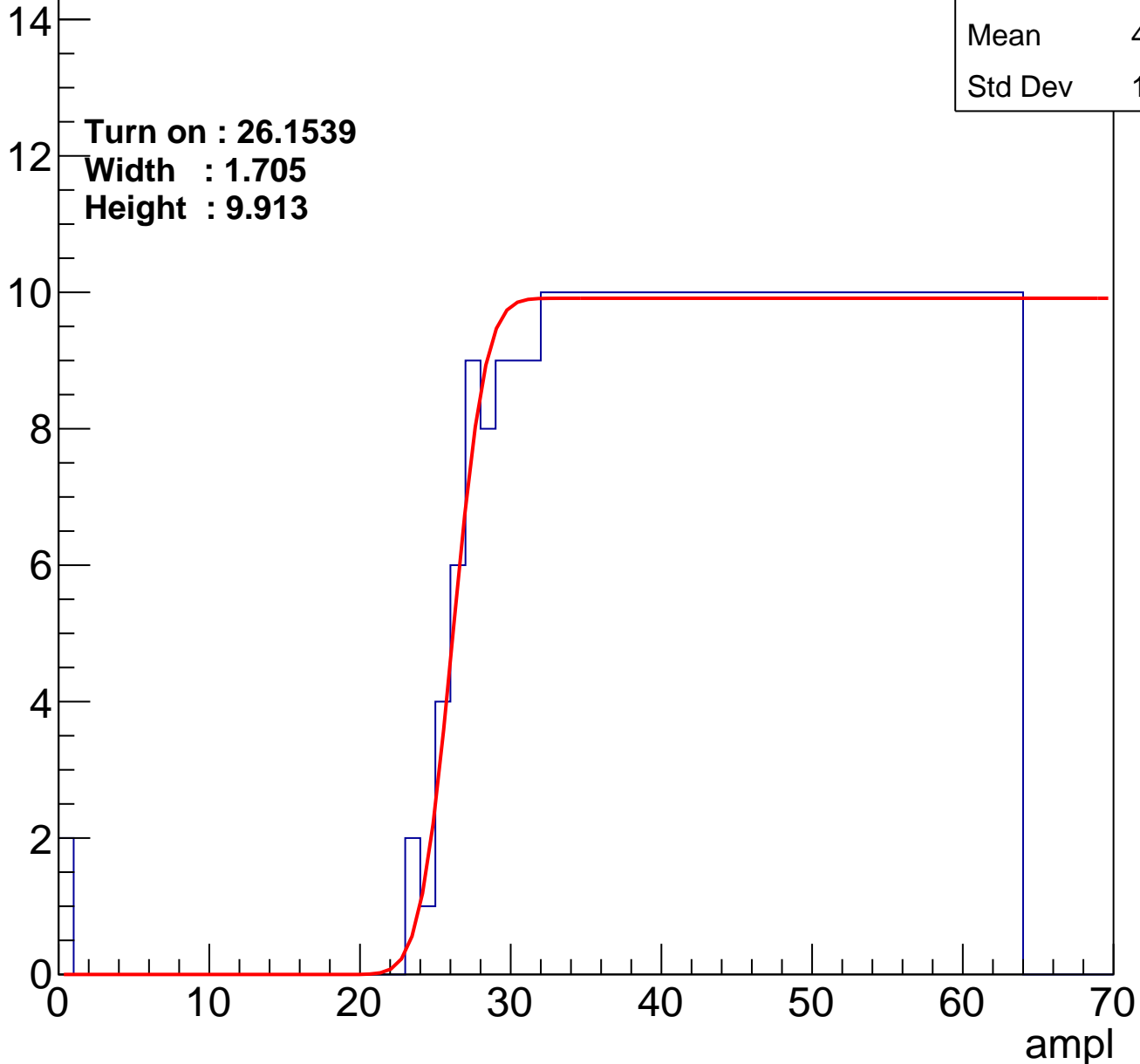
Entries	379
Mean	44.34
Std Dev	11.45

Turn on : 26.1539

Width : 1.705

Height : 9.913

Entry



# B1L100S, U7-ch121

calib\_packv5\_042523\_0143.root, FC#4, port A2

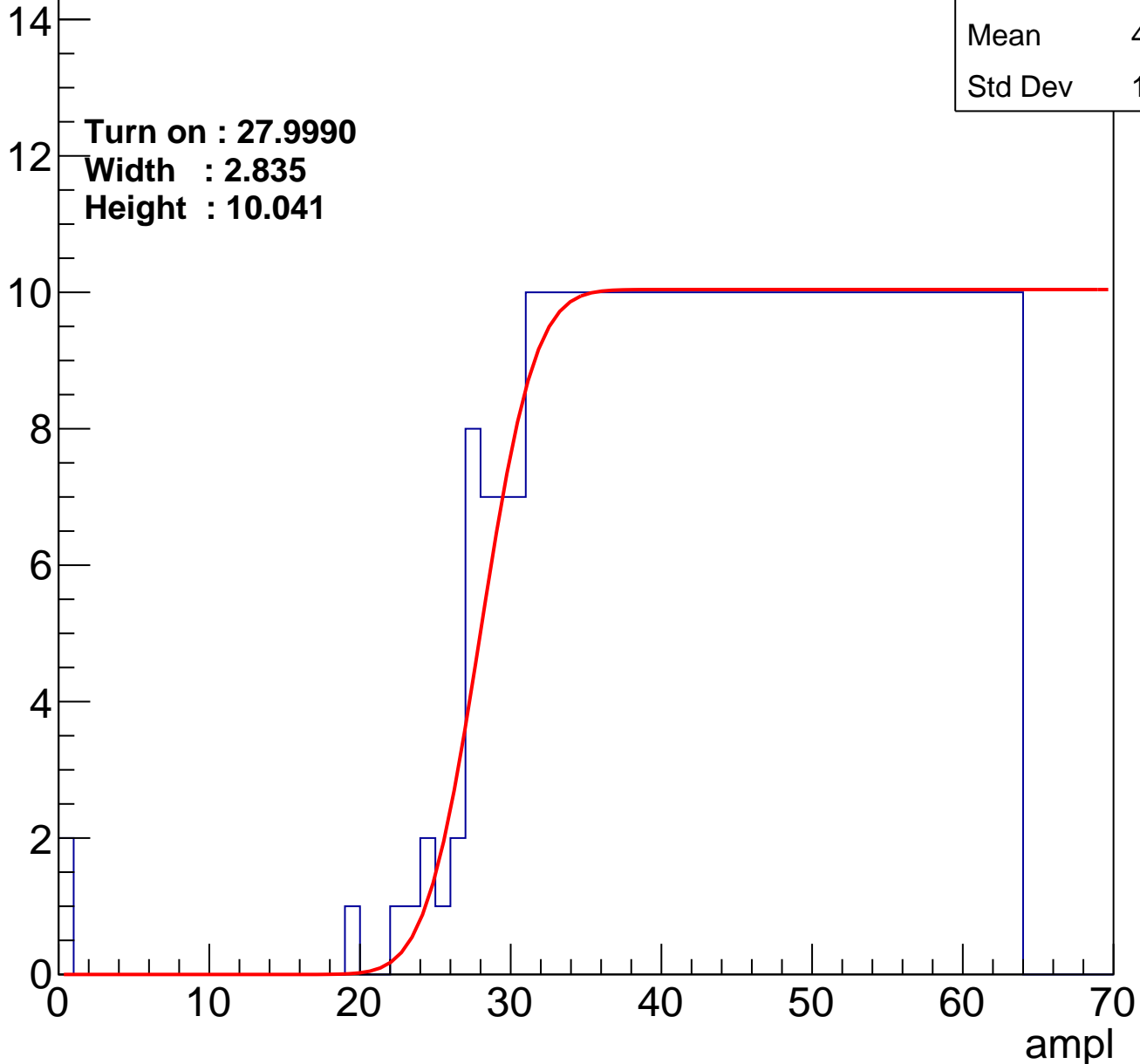
Entries	369
Mean	44.78
Std Dev	11.28

Turn on : 27.9990

Width : 2.835

Height : 10.041

Entry



# B1L100S, U7-ch122

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	385
Mean	43.9
Std Dev	11.97

Turn on : 25.8173

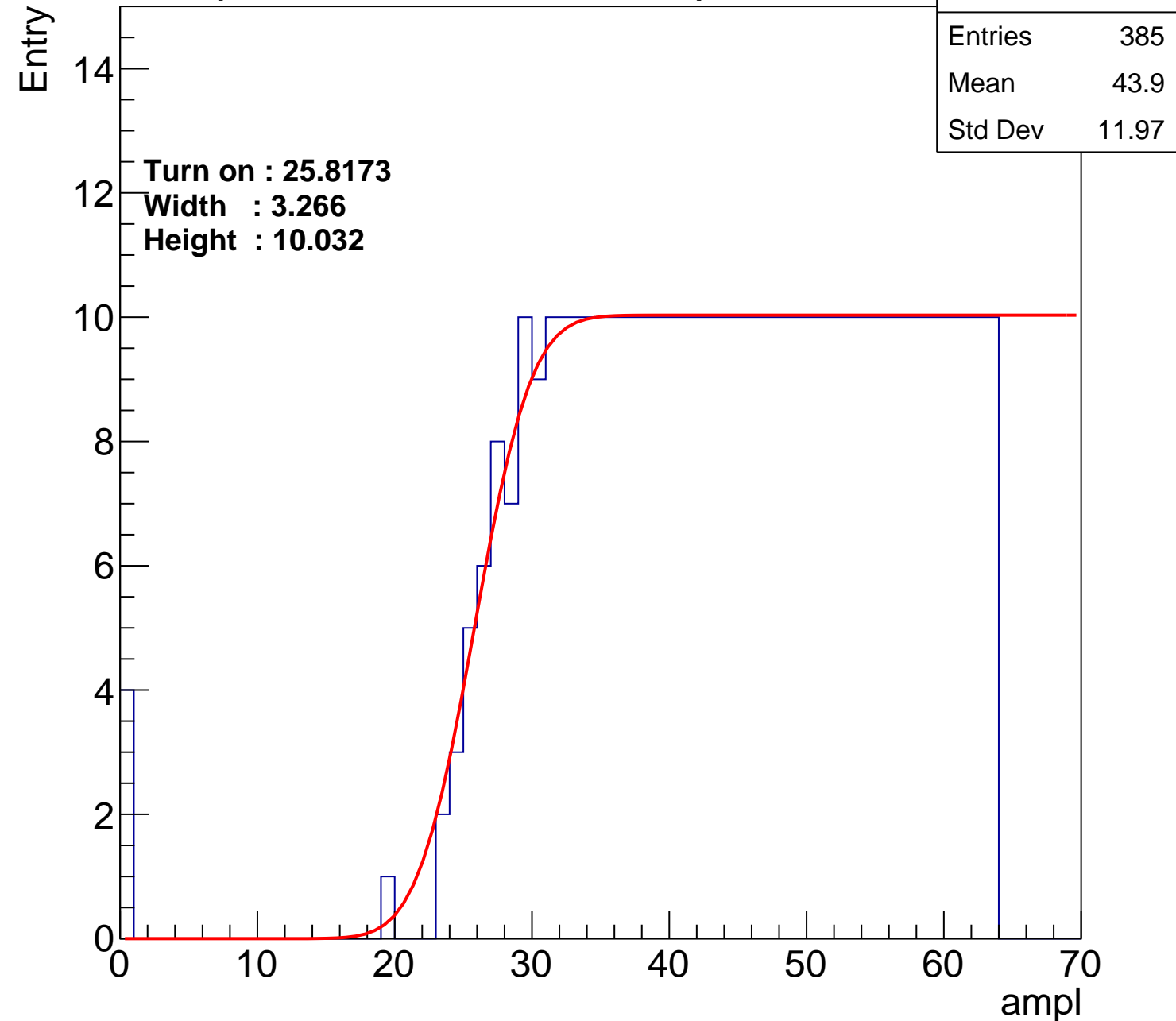
Width : 3.266

Height : 10.032

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch123

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	386
Mean	43.98
Std Dev	11.64

**Turn on : 25.4973**

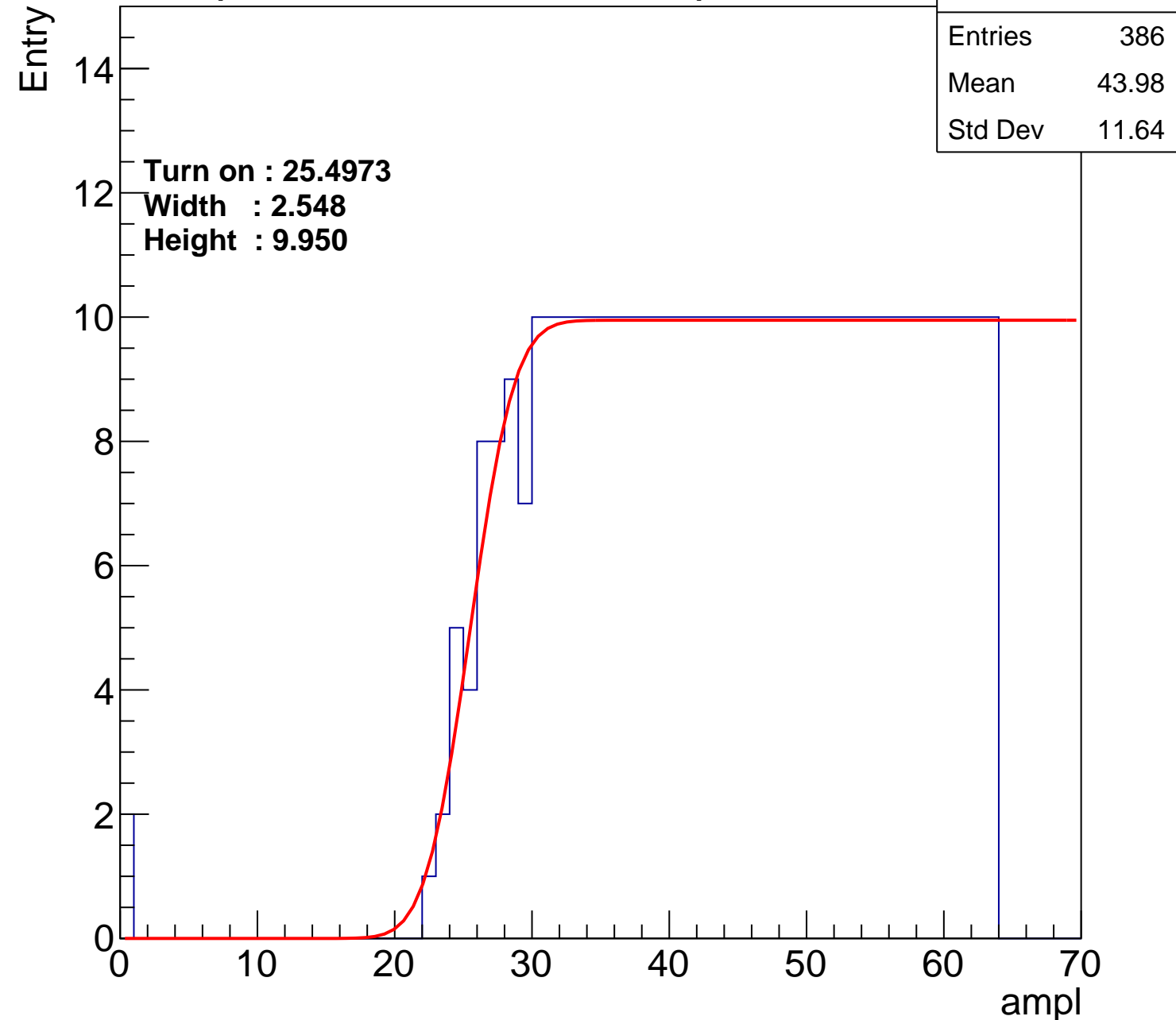
**Width : 2.548**

**Height : 9.950**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch124

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	375
Mean	44.39
Std Dev	11.65

Turn on : 27.4084

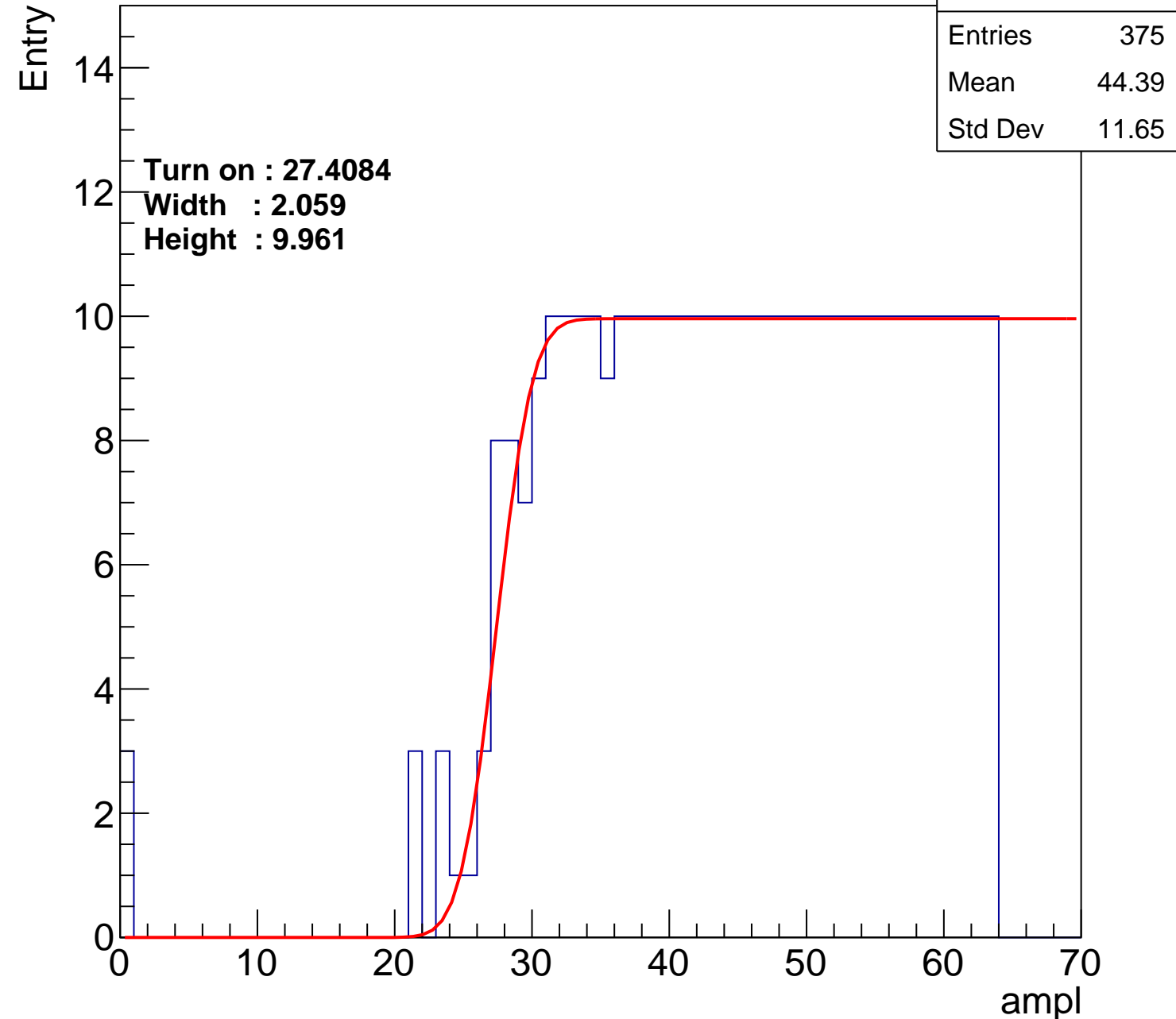
Width : 2.059

Height : 9.961

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch125

calib\_packv5\_042523\_0143.root, FC#4, port A2

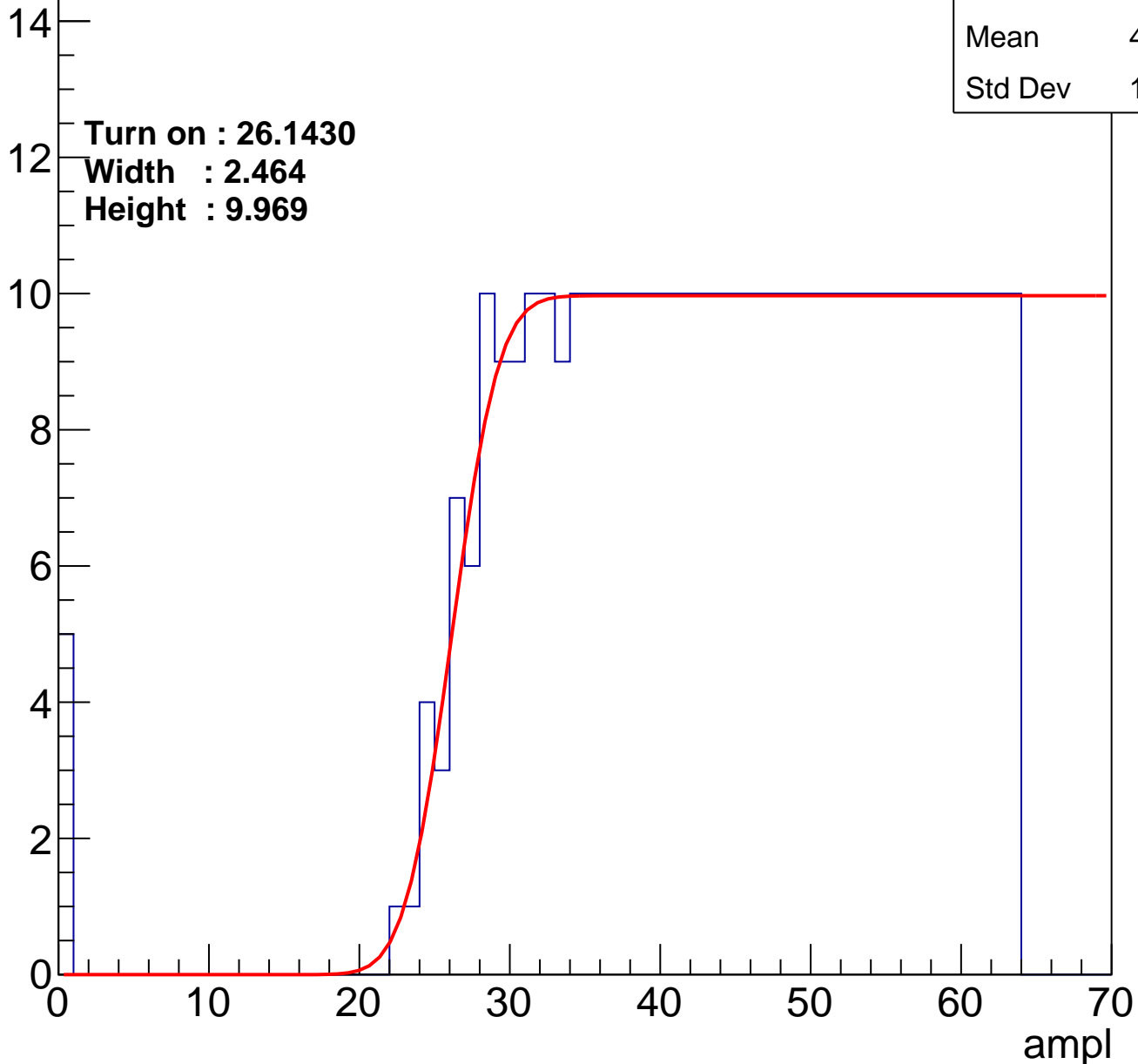
Entries	384
Mean	43.88
Std Dev	12.12

Turn on : 26.1430

Width : 2.464

Height : 9.969

Entry



# B1L100S, U7-ch126

calib\_packv5\_042523\_0143.root, FC#4, port A2

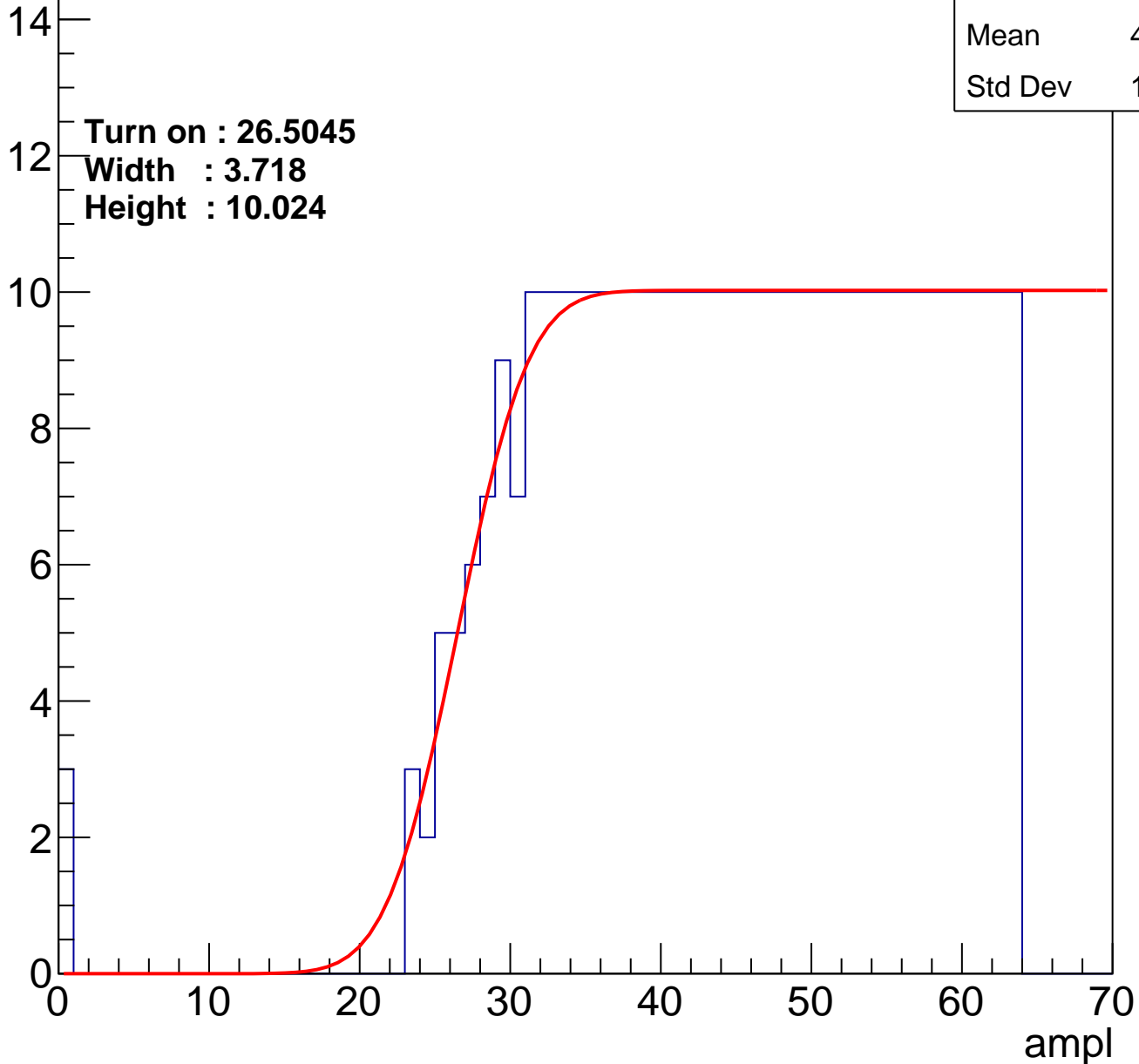
Entries	377
Mean	44.33
Std Dev	11.65

Turn on : 26.5045

Width : 3.718

Height : 10.024

Entry





# B1L100S, U7-ch127

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	367
Mean	44.95
Std Dev	11.02

Turn on : 27.3473

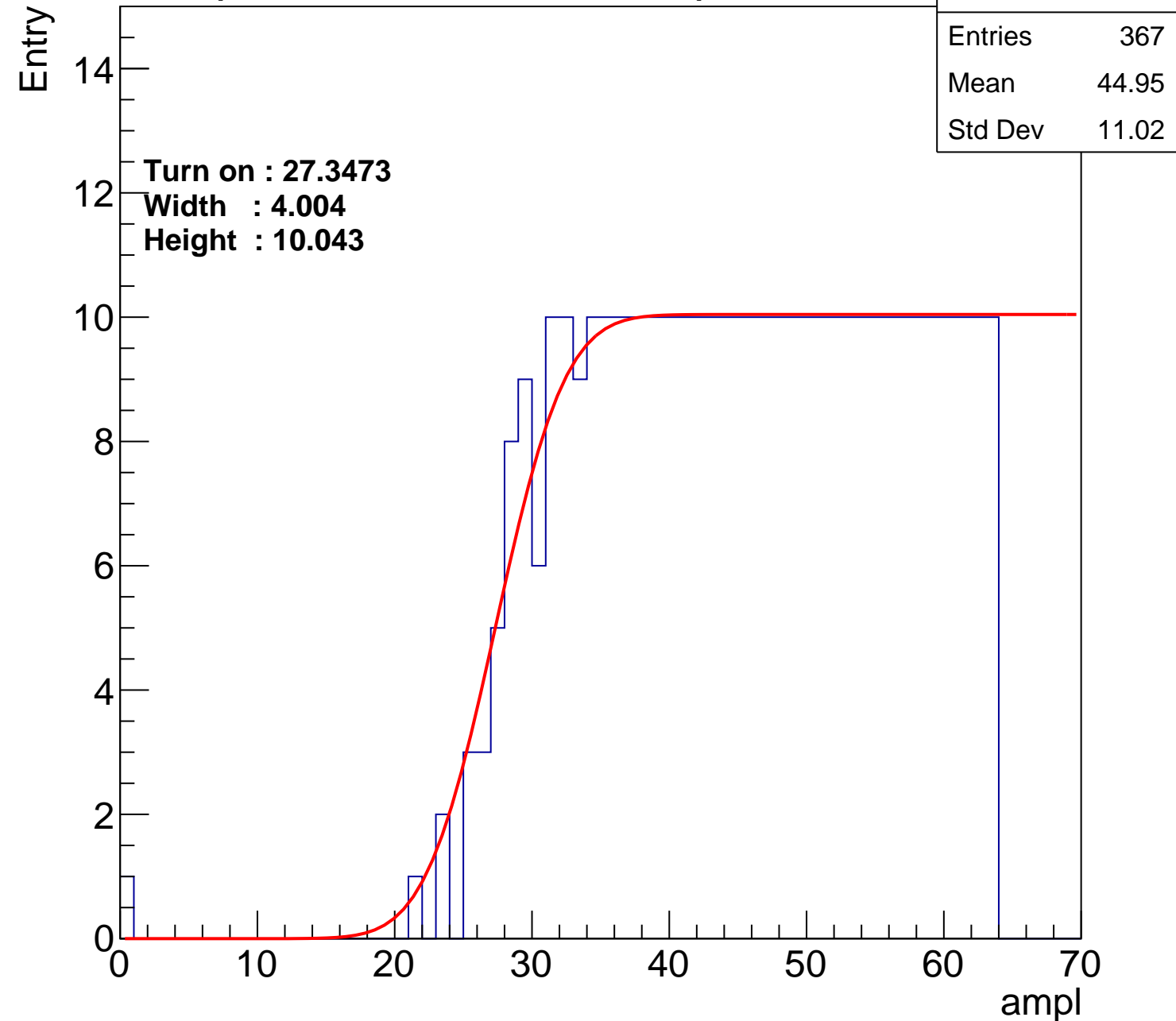
Width : 4.004

Height : 10.043

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U7-ch127

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	367
Mean	44.95
Std Dev	11.02

Turn on : 27.3473

Width : 4.004

Height : 10.043

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl

