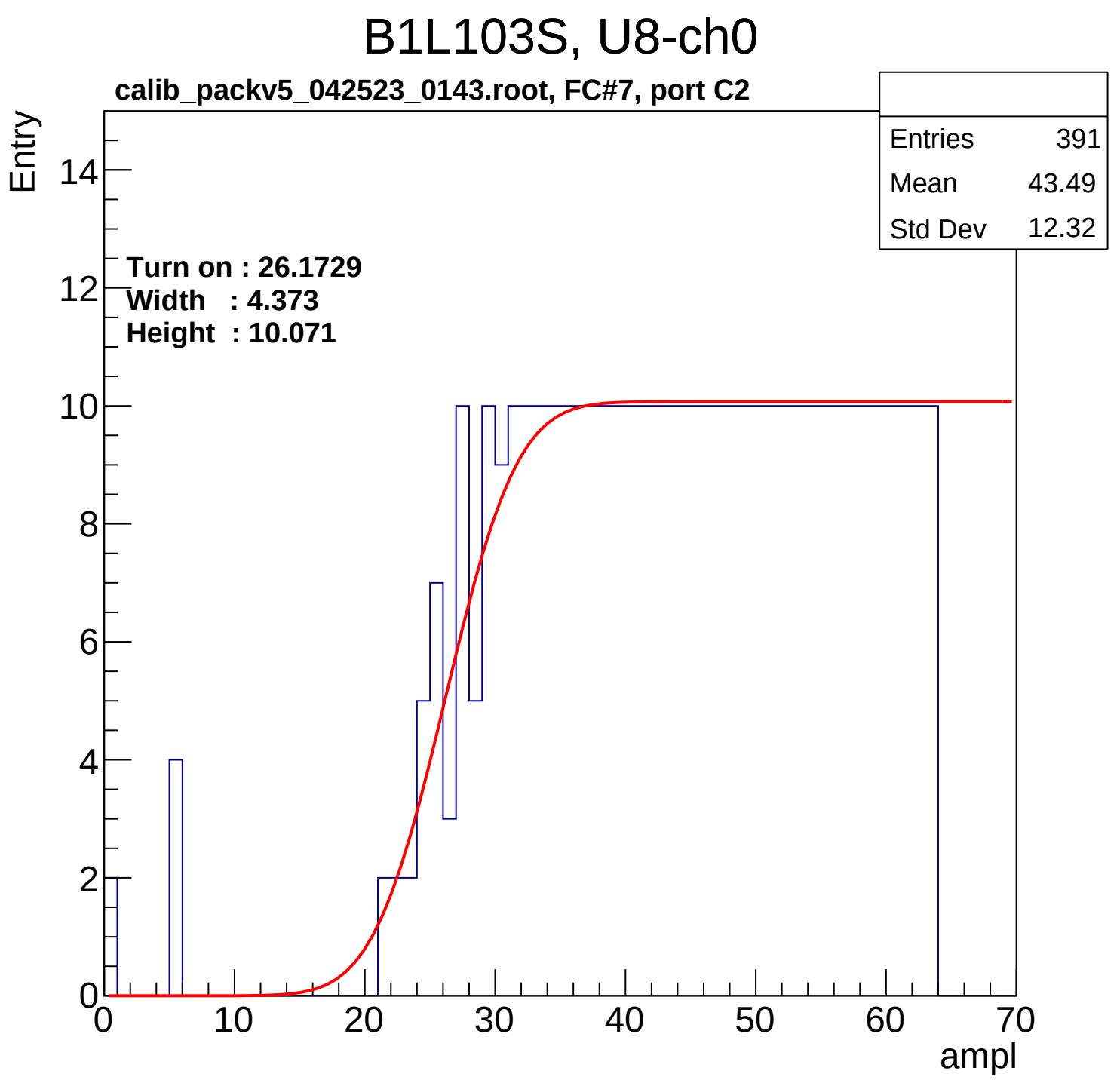
B1L103S, U8-ch0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 391
Mean 43.49
Std Dev 12.32
Turn on : 26.1729
Width : 4.373
Height : 10.071
Entry
ampl
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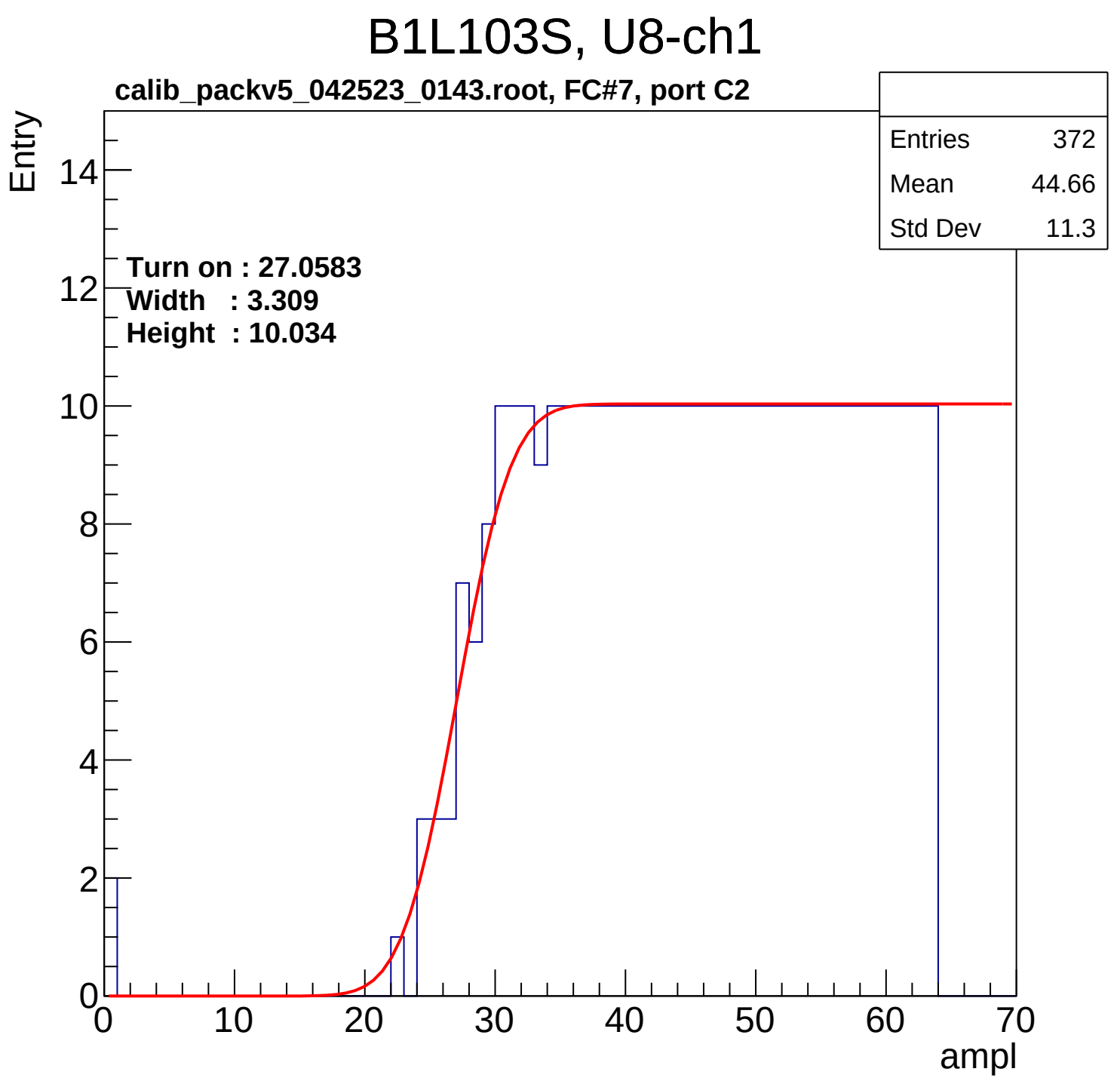
B1L103S, U8-ch1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 372
Mean 44.66
Std Dev 11.3
Turn on : 27.0583
Width : 3.309
Height : 10.034
Entry
ampl
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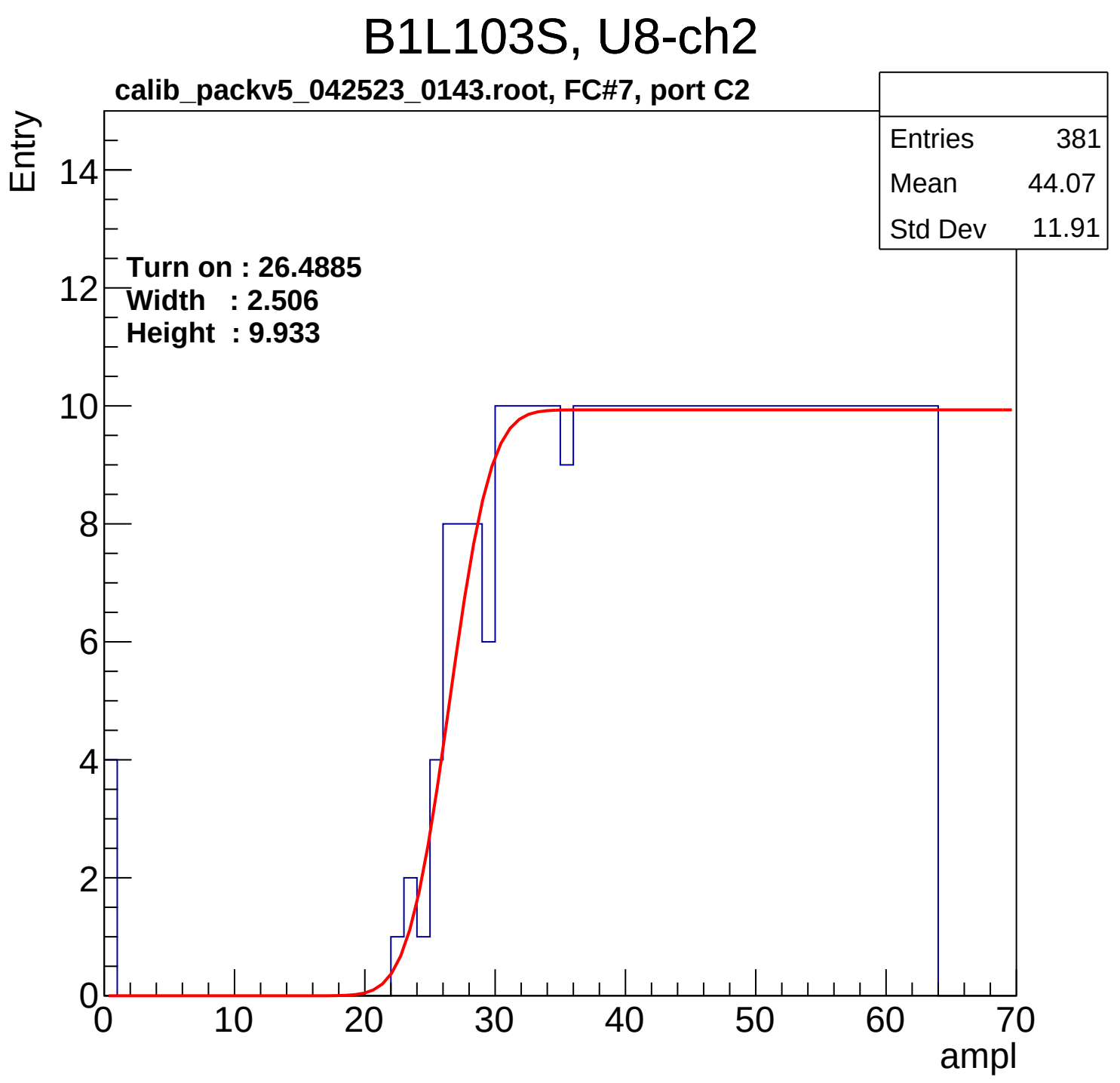
B1L103S, U8-ch2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 381
Mean 44.07
Std Dev 11.91
Turn on : 26.4885
Width : 2.506
Height : 9.933
Entry
ampl
0
2
4
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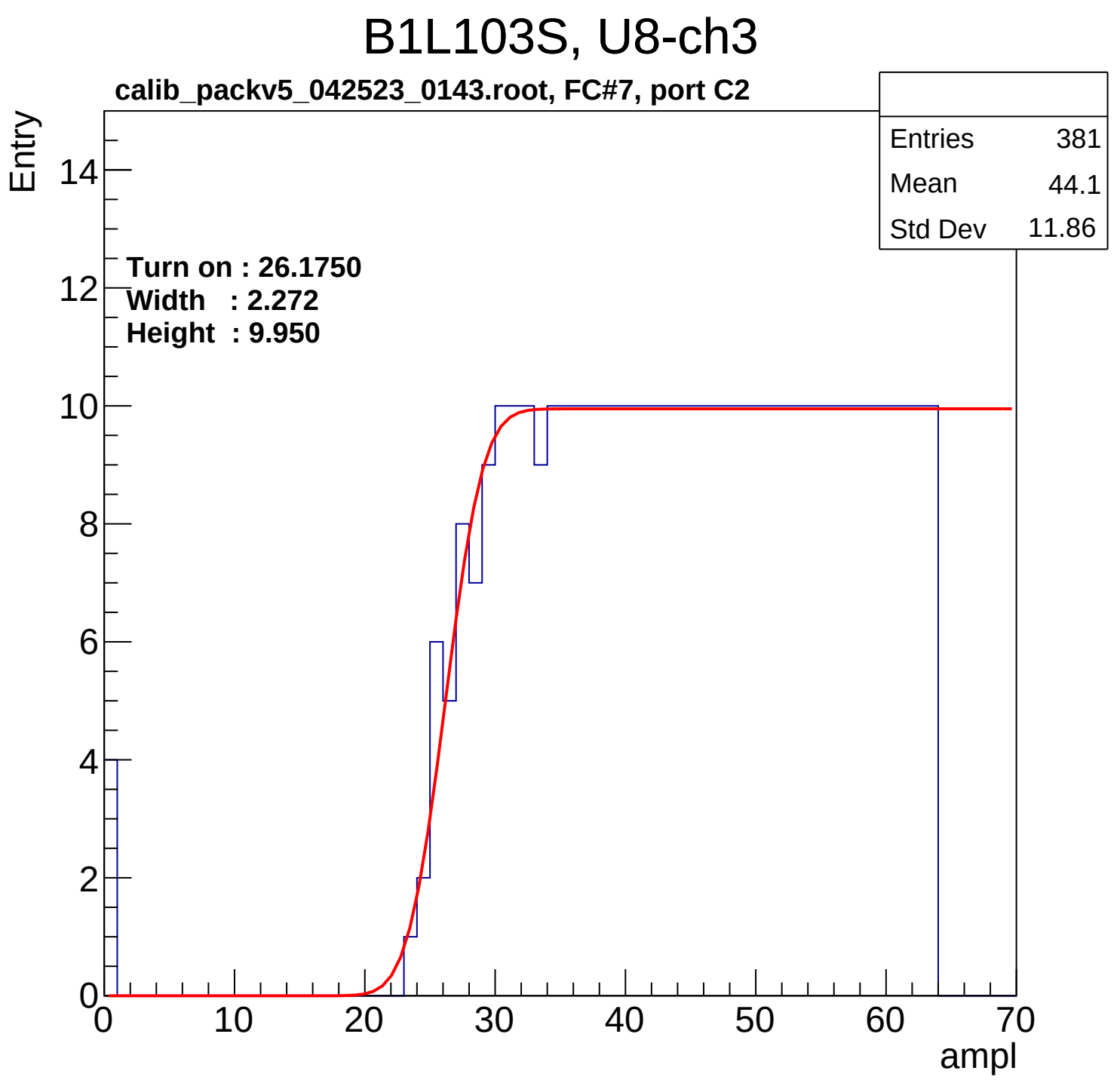
B1L103S, U8-ch3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 381
Mean 44.1
Std Dev 11.86
Turn on : 26.1750
Width : 2.272
Height : 9.950
Entry
ampl
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2
4
6
8
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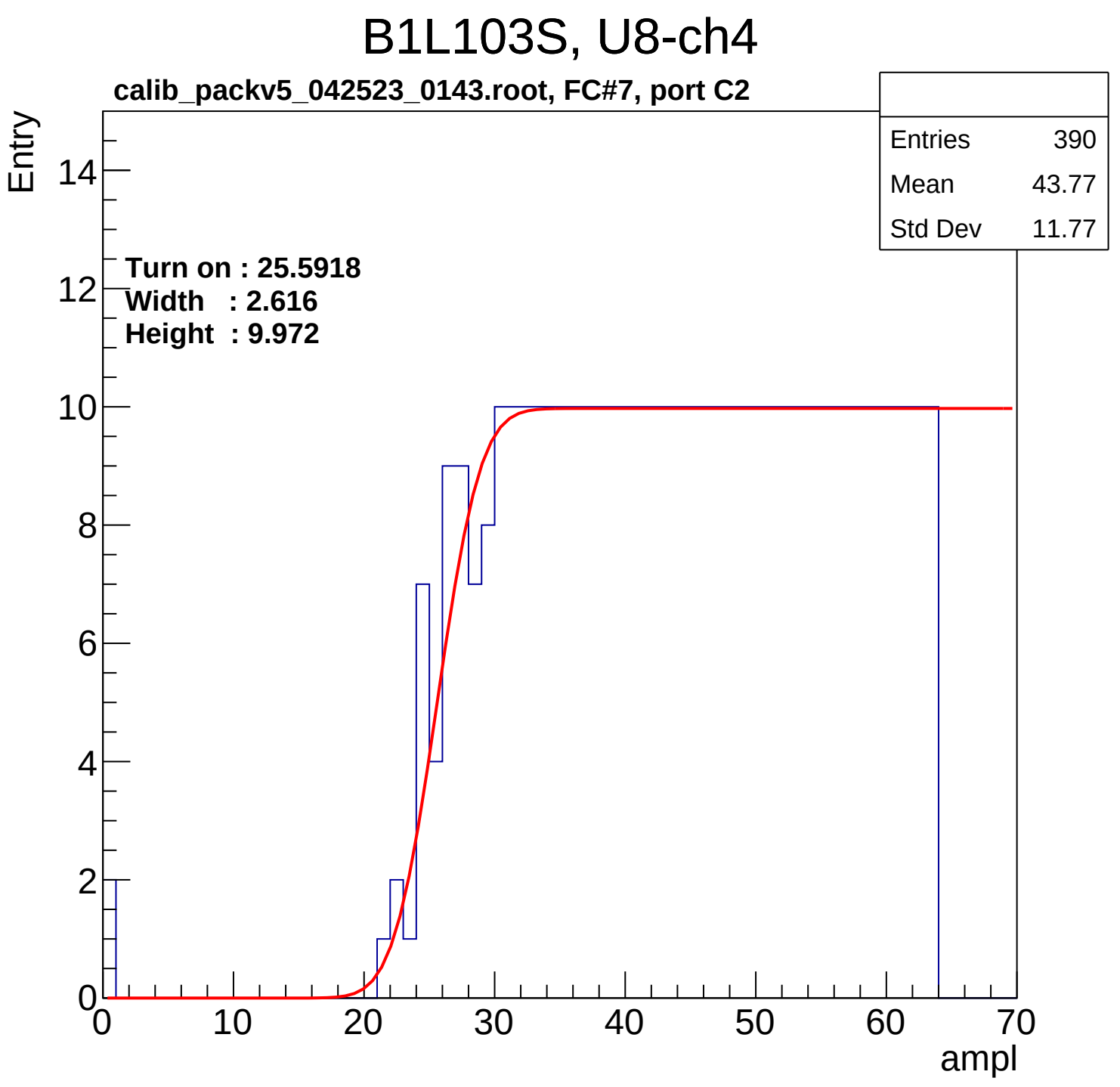
B1L103S, U8-ch4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 390
Mean 43.77
Std Dev 11.77
Turn on : 25.5918
Width : 2.616
Height : 9.972
Entry
ampl
0
2
4
6
8
10
12
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0
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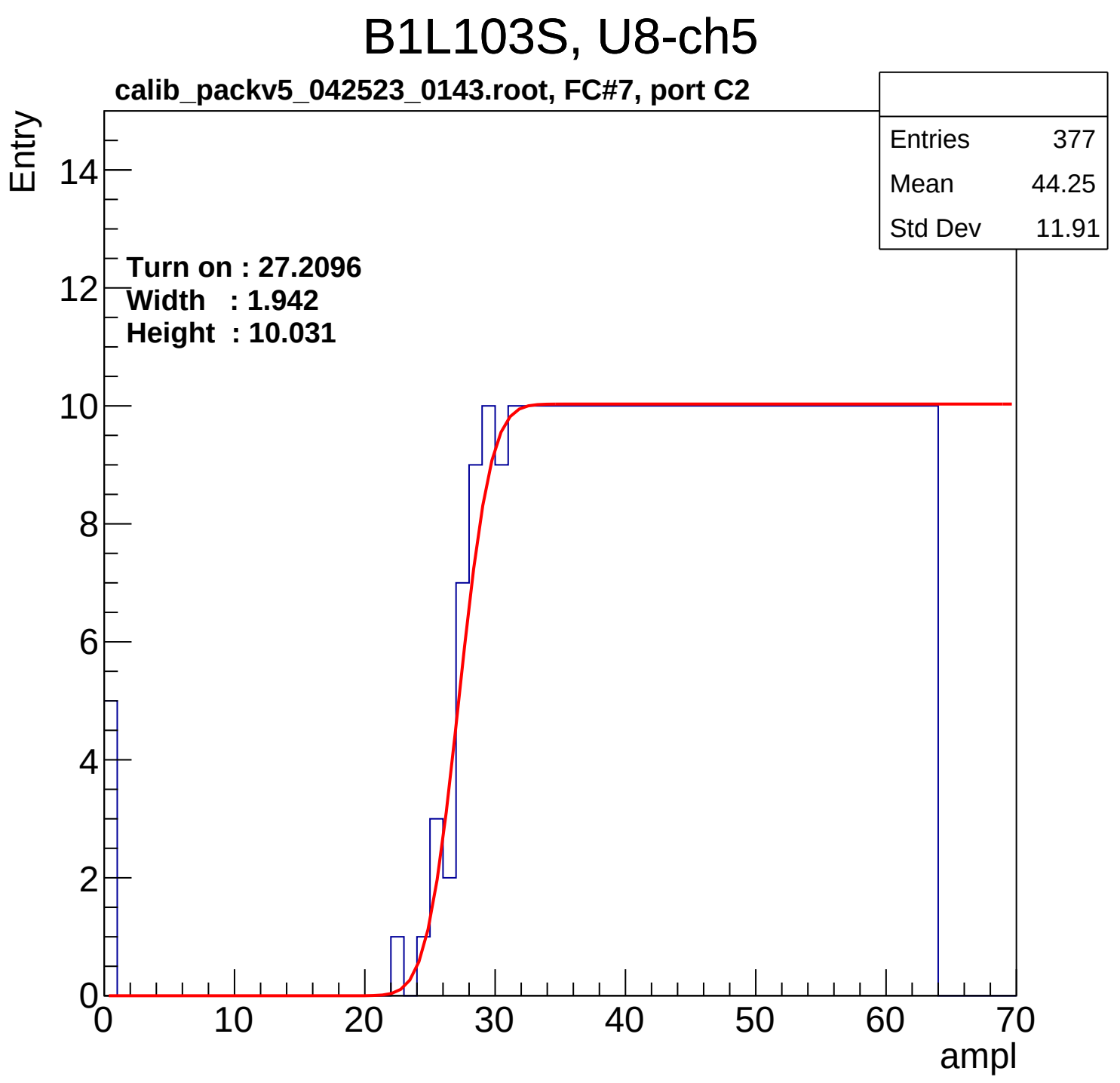
B1L103S, U8-ch5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 377
Mean 44.25
Std Dev 11.91
Turn on : 27.2096
Width : 1.942
Height : 10.031
Entry
ampl
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6
8
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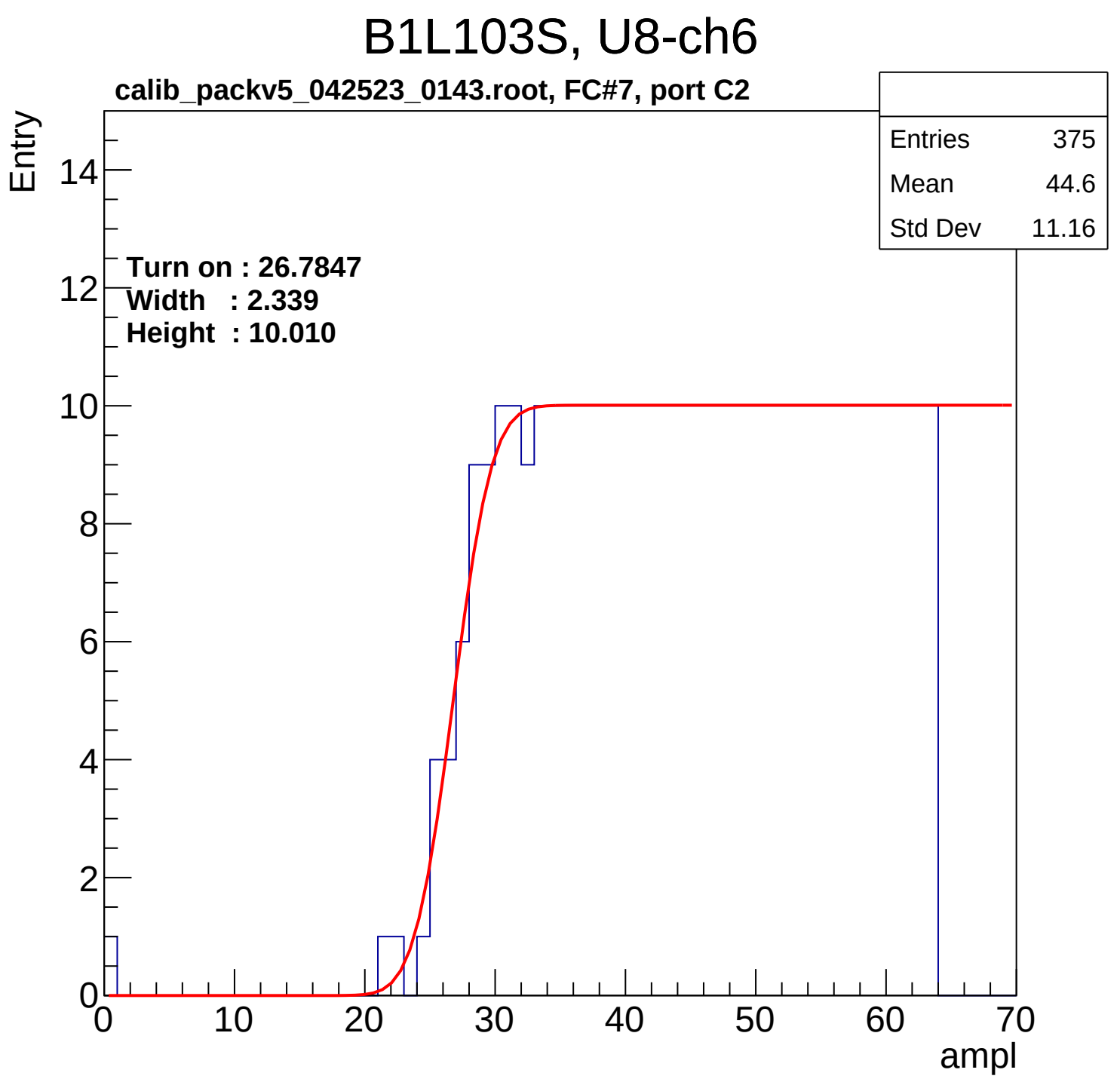
B1L103S, U8-ch6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 375
Mean 44.6
Std Dev 11.16
Turn on : 26.7847
Width : 2.339
Height : 10.010
Entry
ampl
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2
4
6
8
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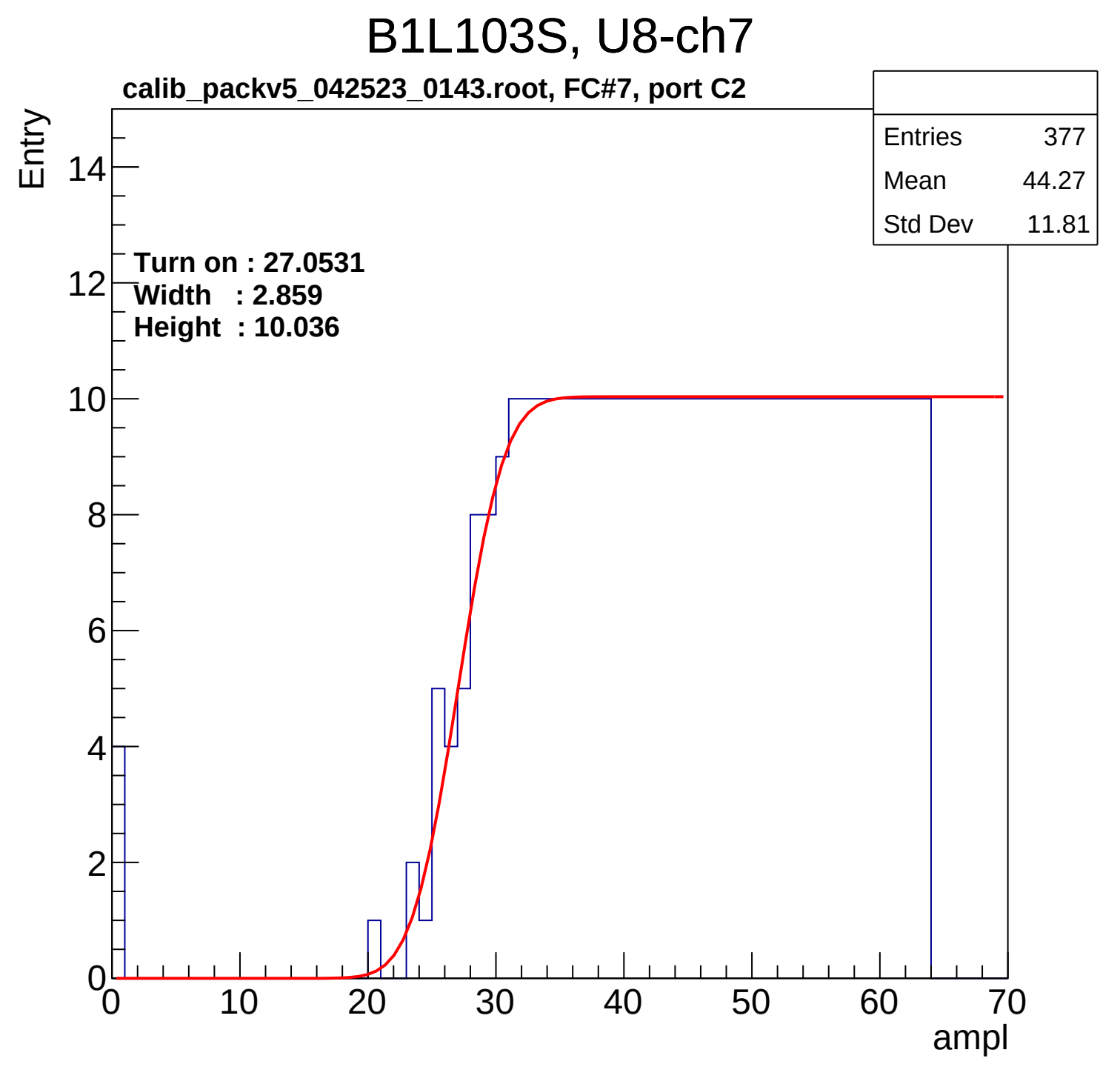
B1L103S, U8-ch7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 377
Mean 44.27
Std Dev 11.81
Turn on : 27.0531
Width : 2.859
Height : 10.036
Entry
ampl
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2
4
6
8
10
12
14
0
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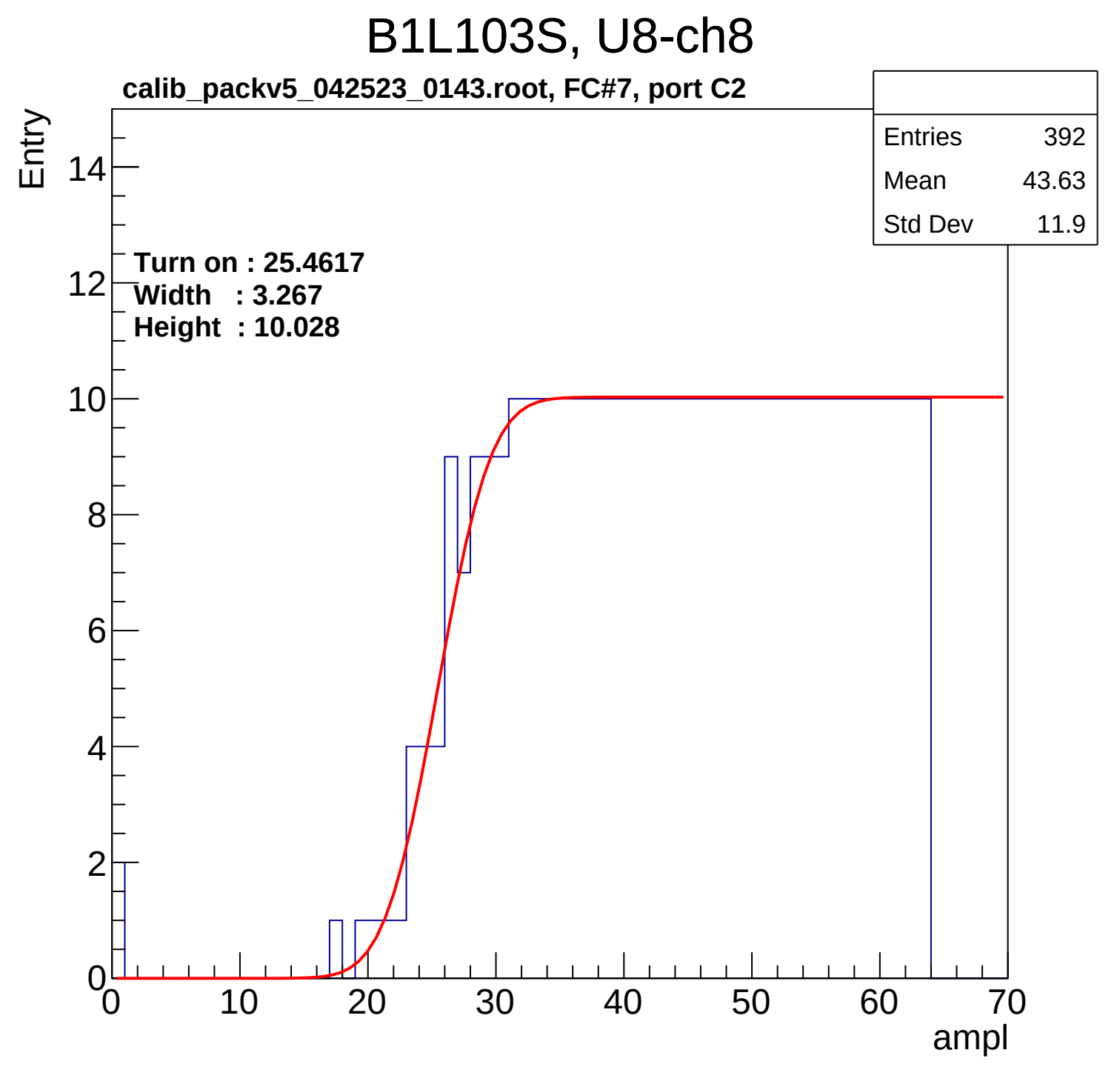
B1L103S, U8-ch8
calib_packv5_042523_0143.root, FC#7, port C2
Entries 392
Mean 43.63
Std Dev 11.9
Turn on : 25.4617
Width : 3.267
Height : 10.028
Entry
ampl
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6
8
10
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0
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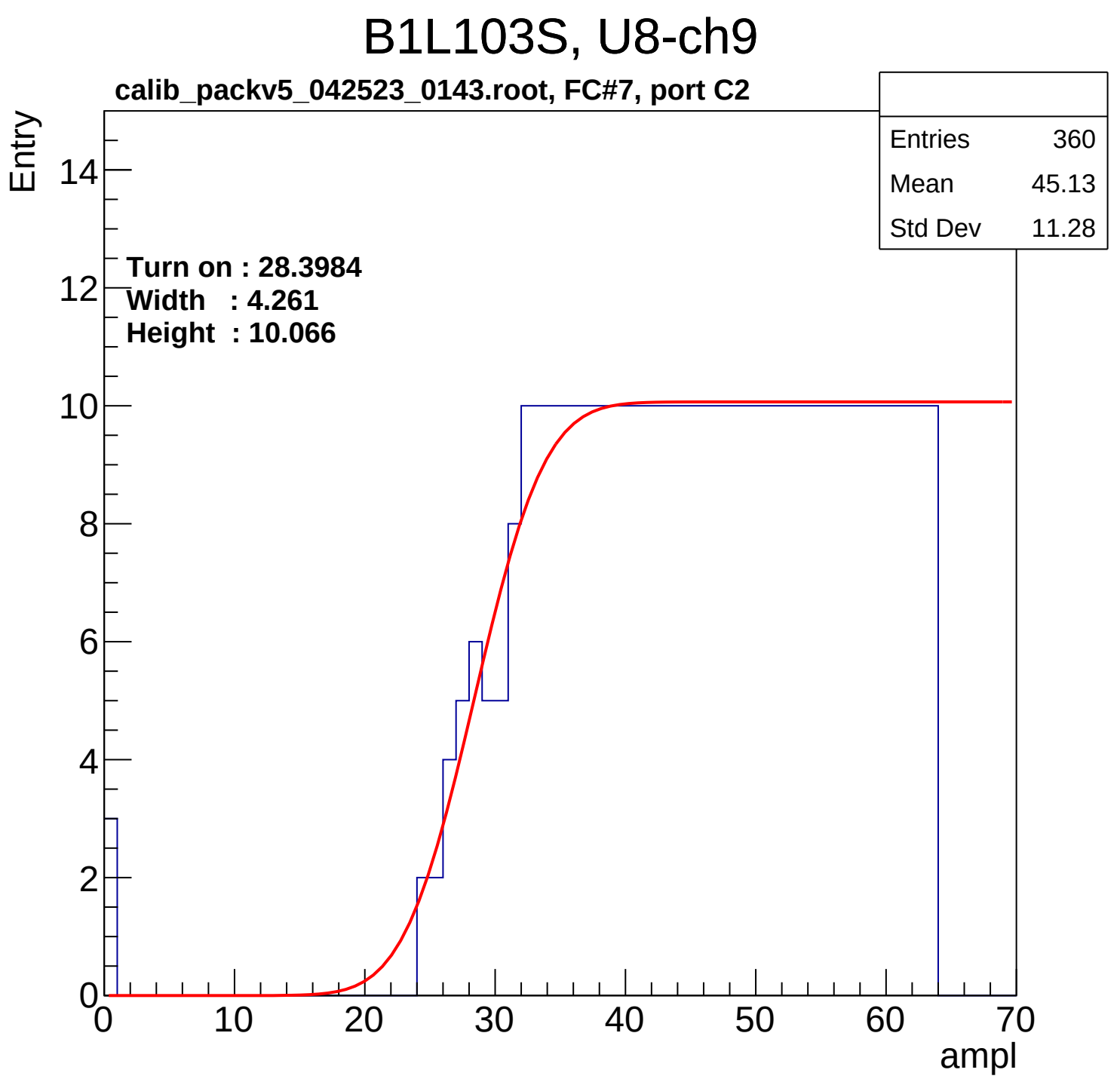
B1L103S, U8-ch9
calib_packv5_042523_0143.root, FC#7, port C2
Entries 360
Mean 45.13
Std Dev 11.28
Turn on : 28.3984
Width : 4.261
Height : 10.066
Entry
ampl
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2
4
6
8
10
12
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0
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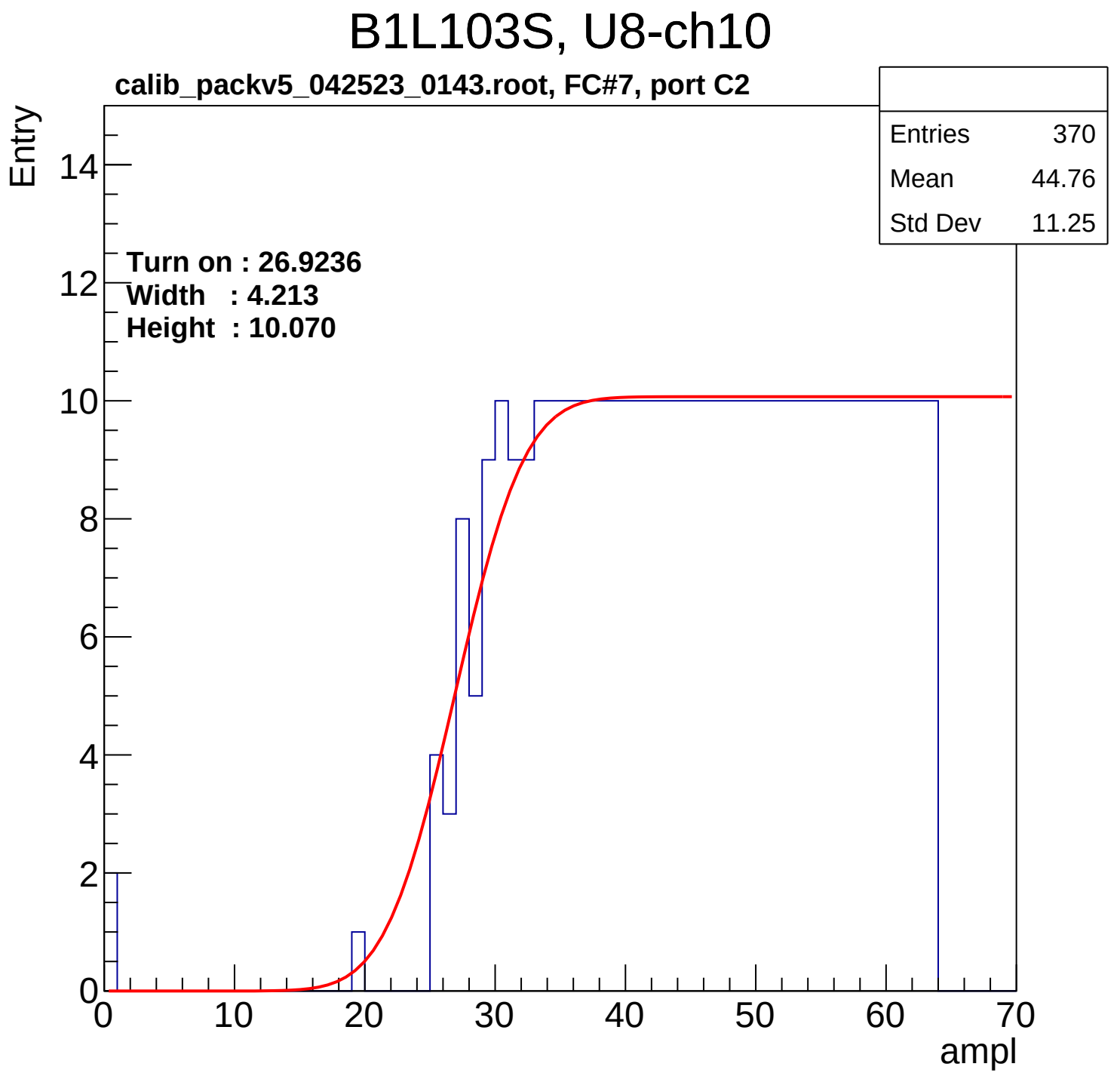
B1L103S, U8-ch10
calib_packv5_042523_0143.root, FC#7, port C2
Entries 370
Mean 44.76
Std Dev 11.25
Turn on : 26.9236
Width : 4.213
Height : 10.070
Entry
ampl
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6
8
10
12
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0
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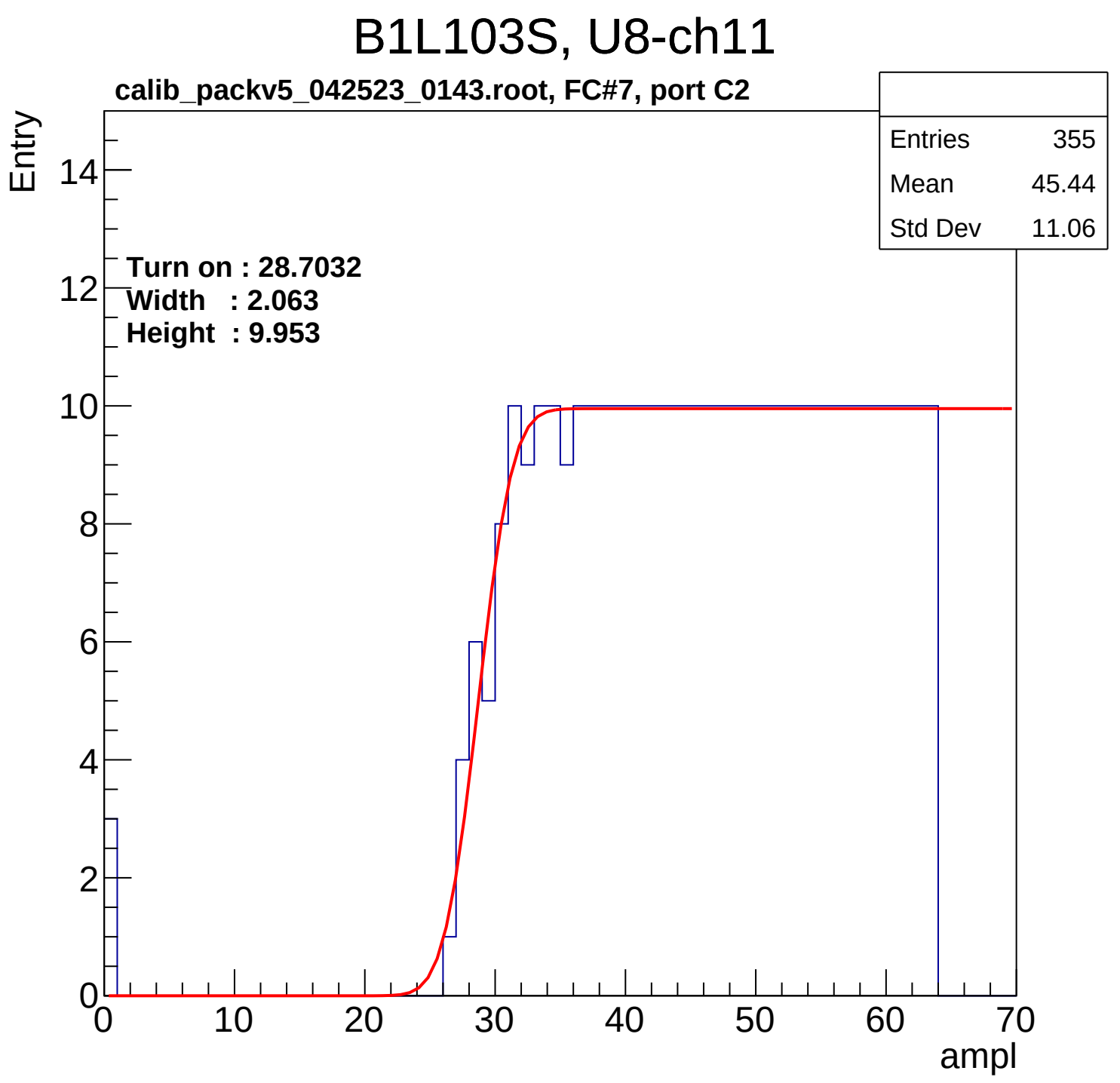
B1L103S, U8-ch11
calib_packv5_042523_0143.root, FC#7, port C2
Entries 355
Mean 45.44
Std Dev 11.06
Turn on : 28.7032
Width : 2.063
Height : 9.953
Entry
ampl
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6
8
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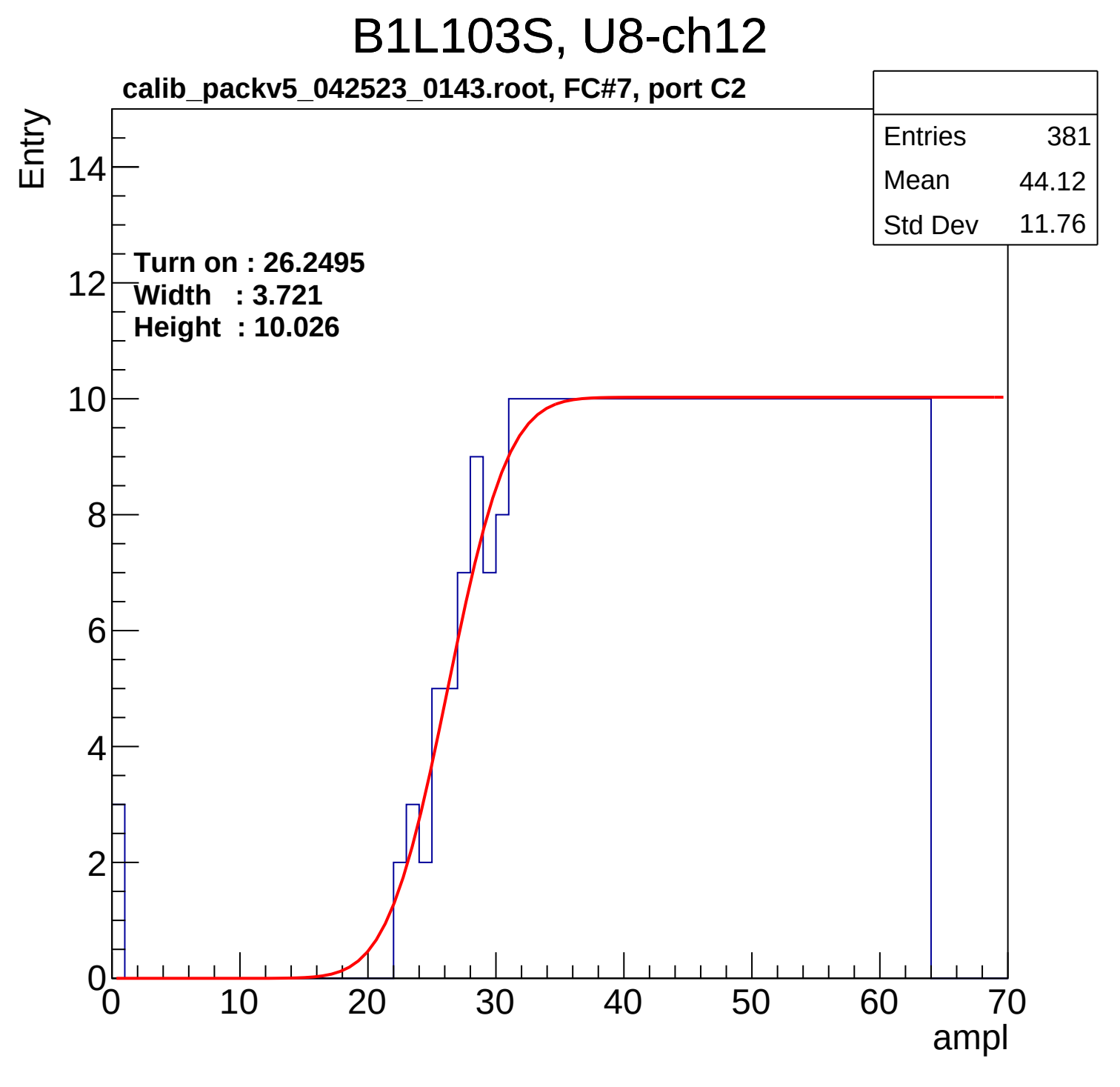
B1L103S, U8-ch12
calib_packv5_042523_0143.root, FC#7, port C2
Entries 381
Mean 44.12
Std Dev 11.76
Turn on : 26.2495
Width : 3.721
Height : 10.026
Entry
ampl
0
2
4
6
8
10
12
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0
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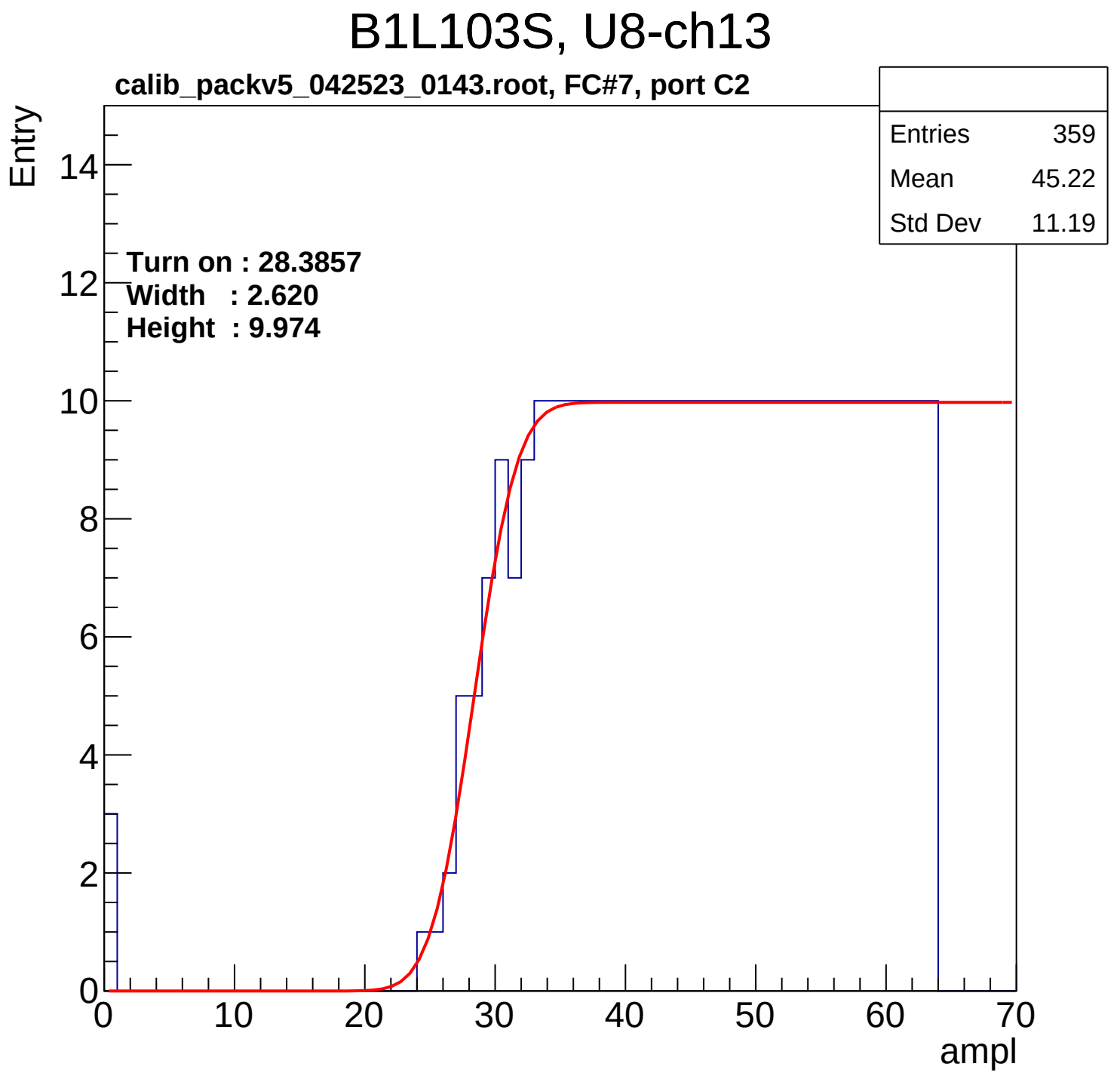
B1L103S, U8-ch13
calib_packv5_042523_0143.root, FC#7, port C2
Entries 359
Mean 45.22
Std Dev 11.19
Turn on : 28.3857
Width : 2.620
Height : 9.974
Entry
ampl
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6
8
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0
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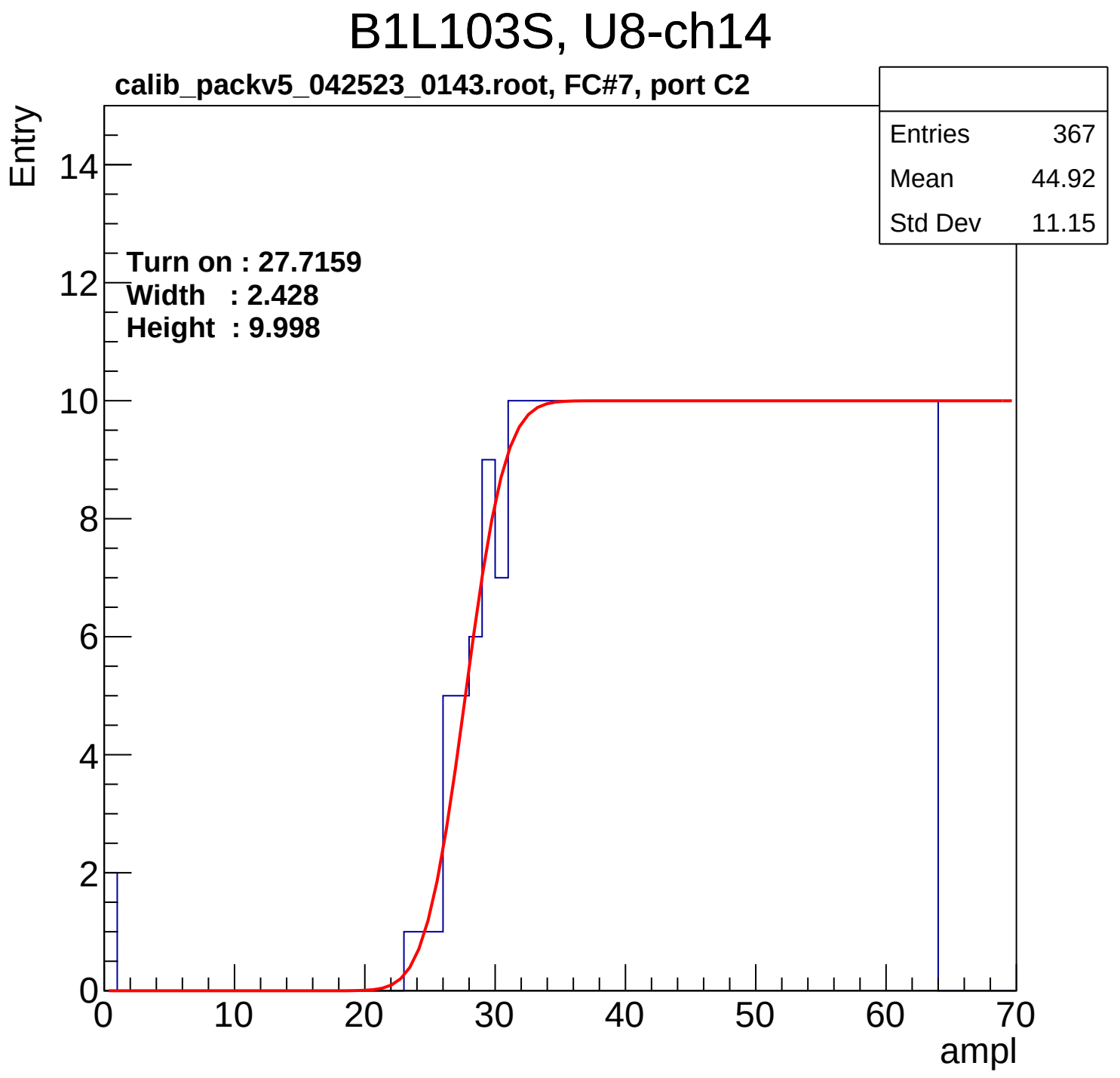
B1L103S, U8-ch14
calib_packv5_042523_0143.root, FC#7, port C2
Entries 367
Mean 44.92
Std Dev 11.15
Turn on : 27.7159
Width : 2.428
Height : 9.998
Entry
ampl
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6
8
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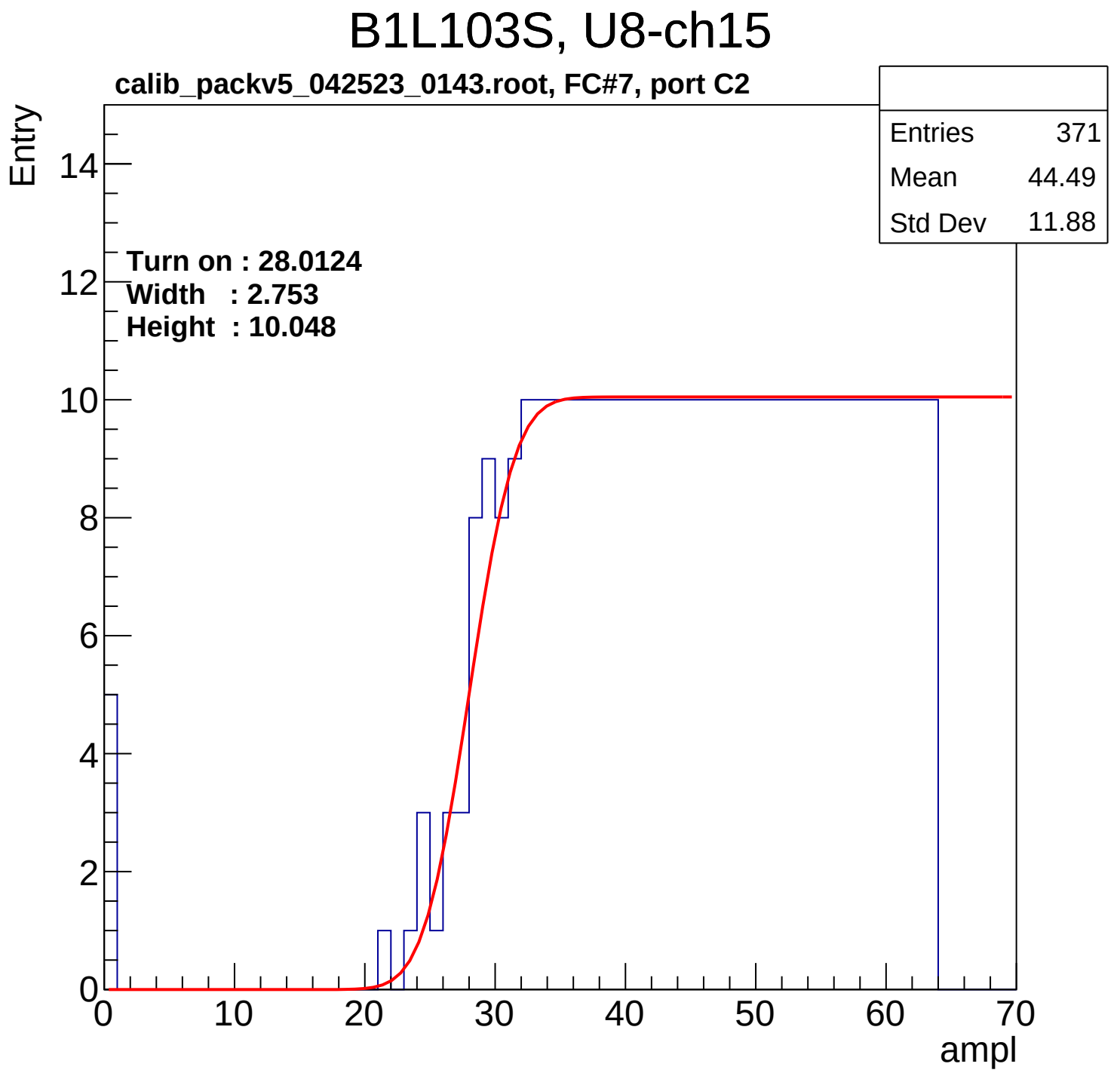
B1L103S, U8-ch15
calib_packv5_042523_0143.root, FC#7, port C2
Entries 371
Mean 44.49
Std Dev 11.88
Turn on : 28.0124
Width : 2.753
Height : 10.048
Entry
ampl
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8
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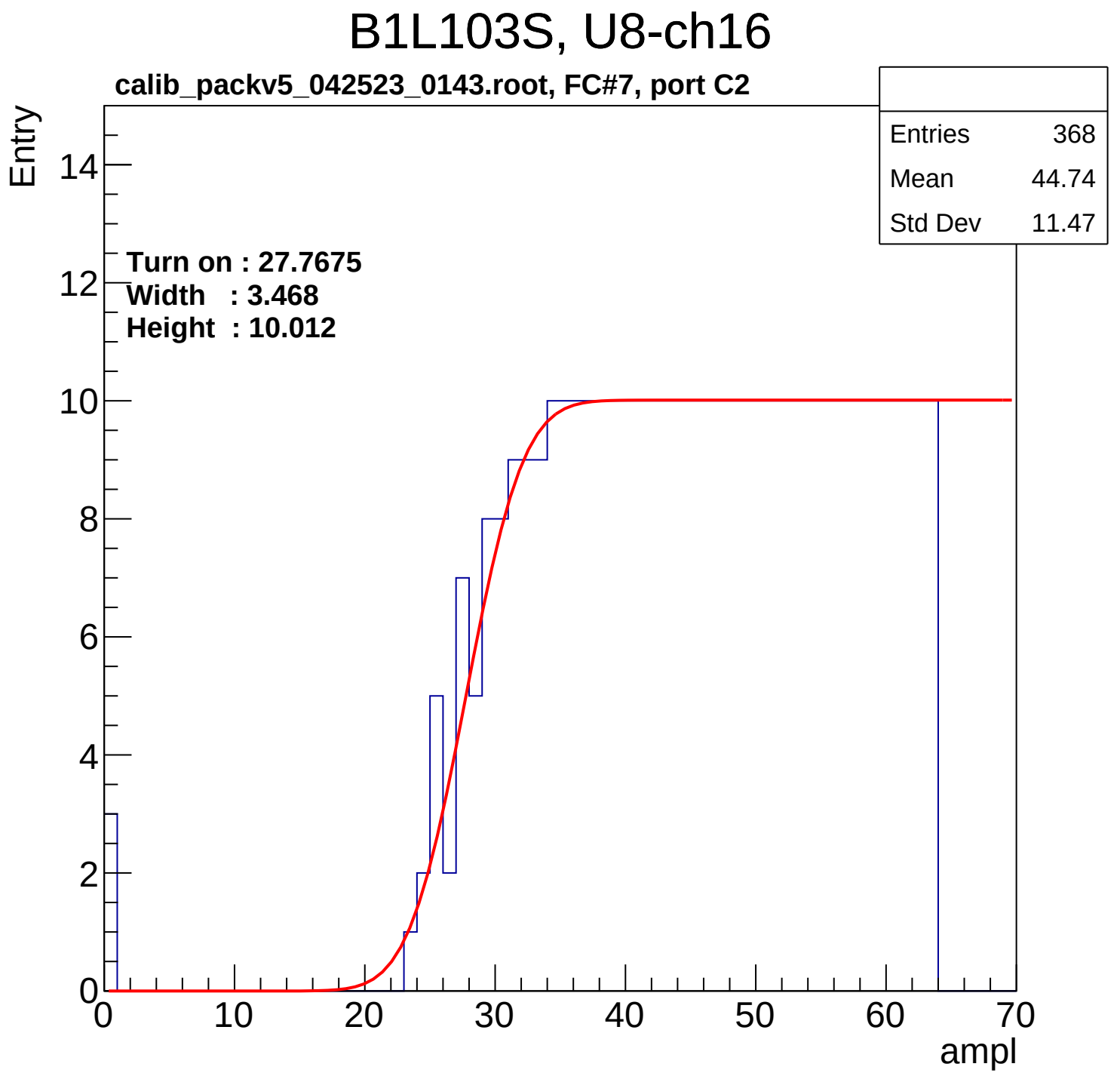
B1L103S, U8-ch16
calib_packv5_042523_0143.root, FC#7, port C2
Entries 368
Mean 44.74
Std Dev 11.47
Turn on : 27.7675
Width : 3.468
Height : 10.012
Entry
ampl
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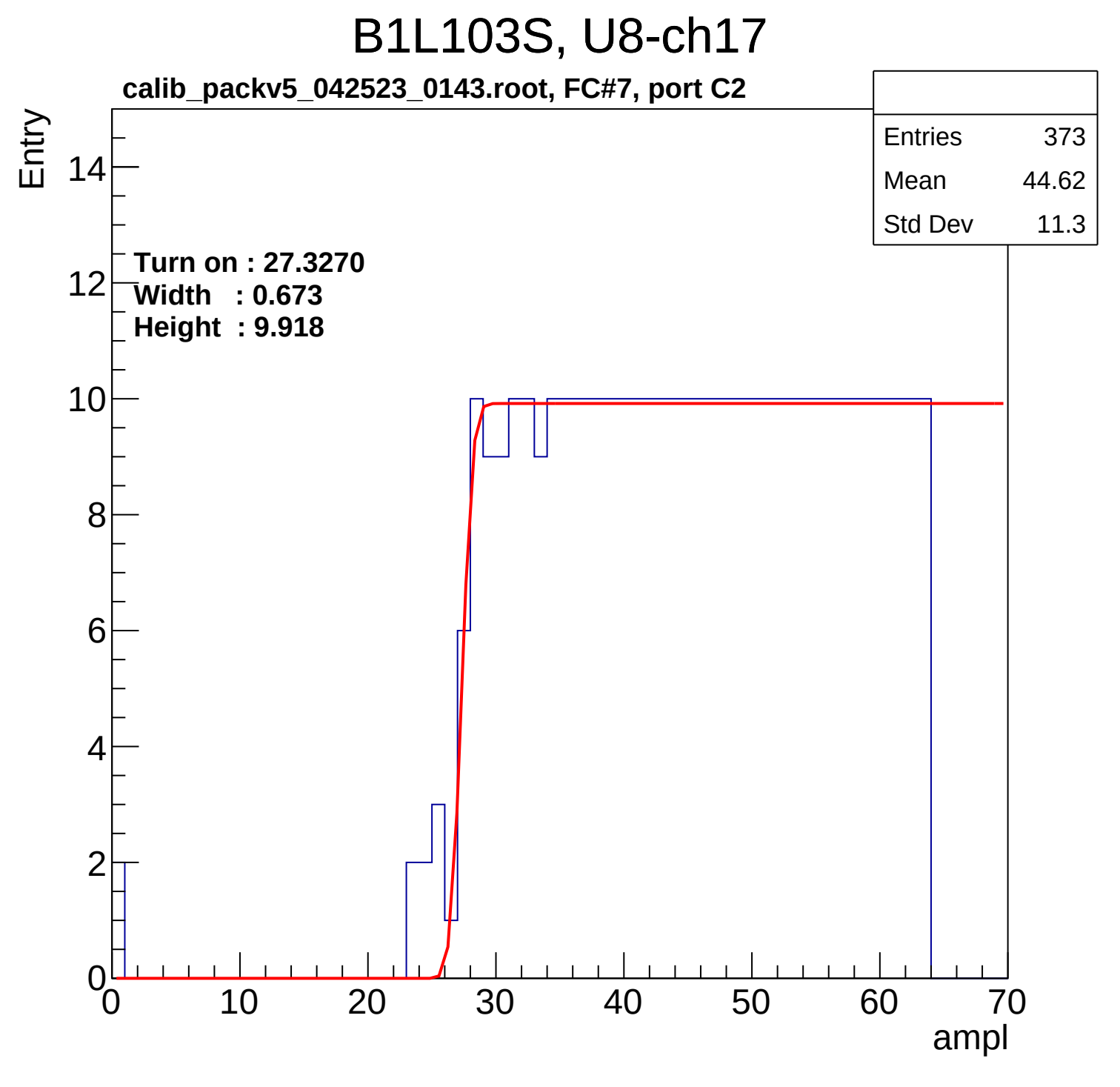
B1L103S, U8-ch17
calib_packv5_042523_0143.root, FC#7, port C2
Entries 373
Mean 44.62
Std Dev 11.3
Turn on : 27.3270
Width : 0.673
Height : 9.918
Entry
ampl
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6
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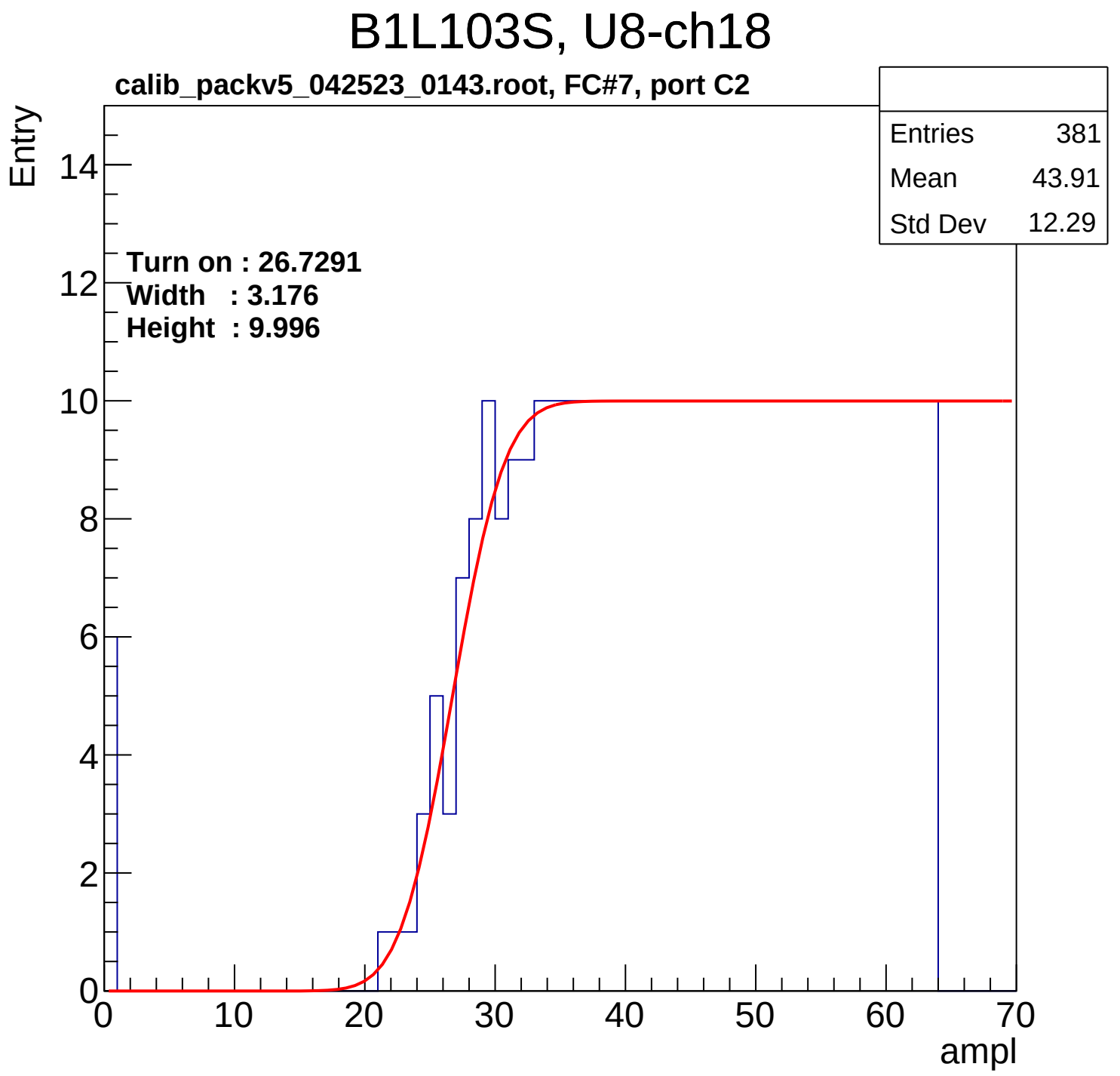
B1L103S, U8-ch18
calib_packv5_042523_0143.root, FC#7, port C2
Entries 381
Mean 43.91
Std Dev 12.29
Turn on : 26.7291
Width : 3.176
Height : 9.996
Entry
ampl
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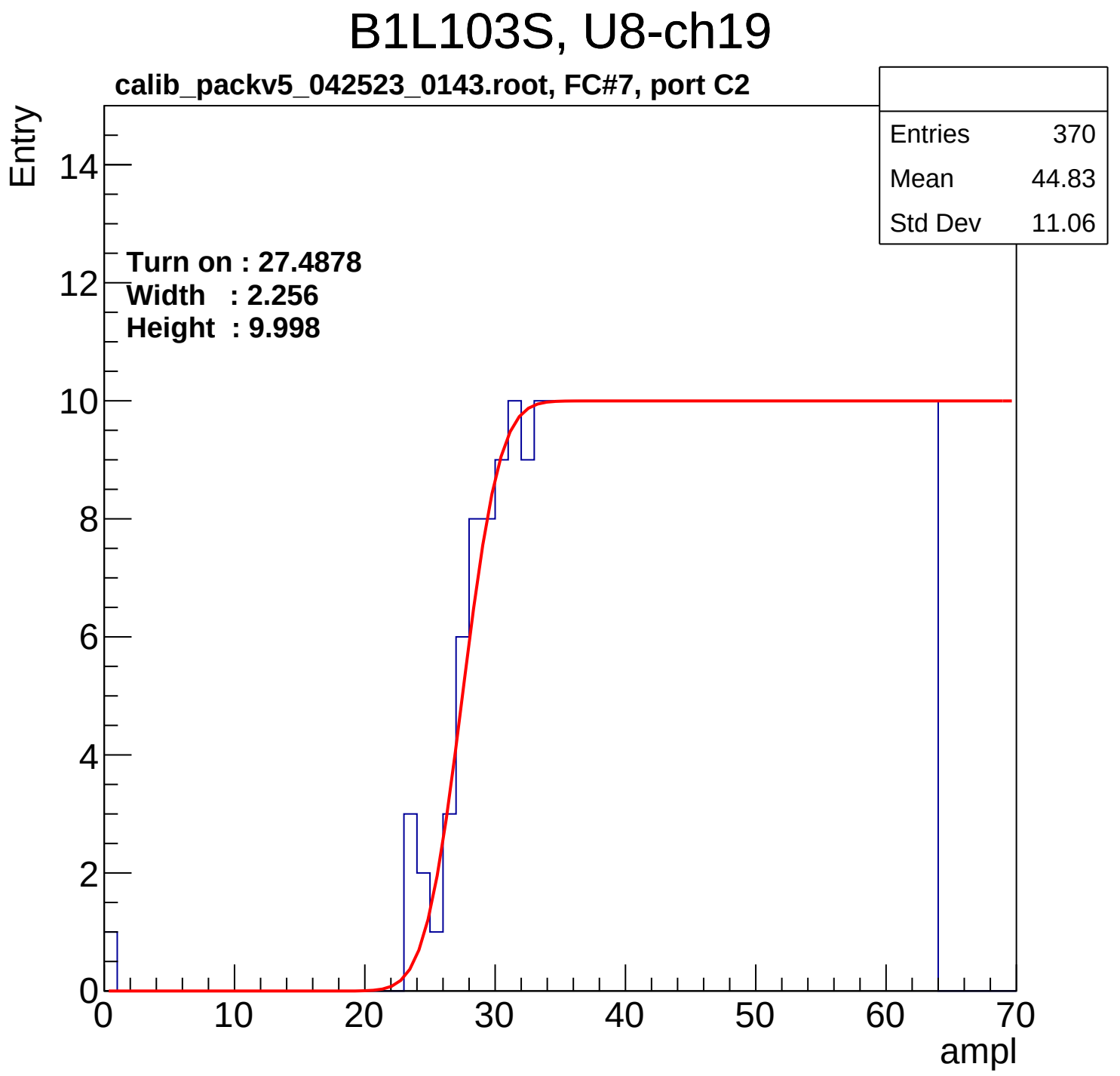
B1L103S, U8-ch19
calib_packv5_042523_0143.root, FC#7, port C2
Entries 370
Mean 44.83
Std Dev 11.06
Turn on : 27.4878
Width : 2.256
Height : 9.998
Entry
ampl
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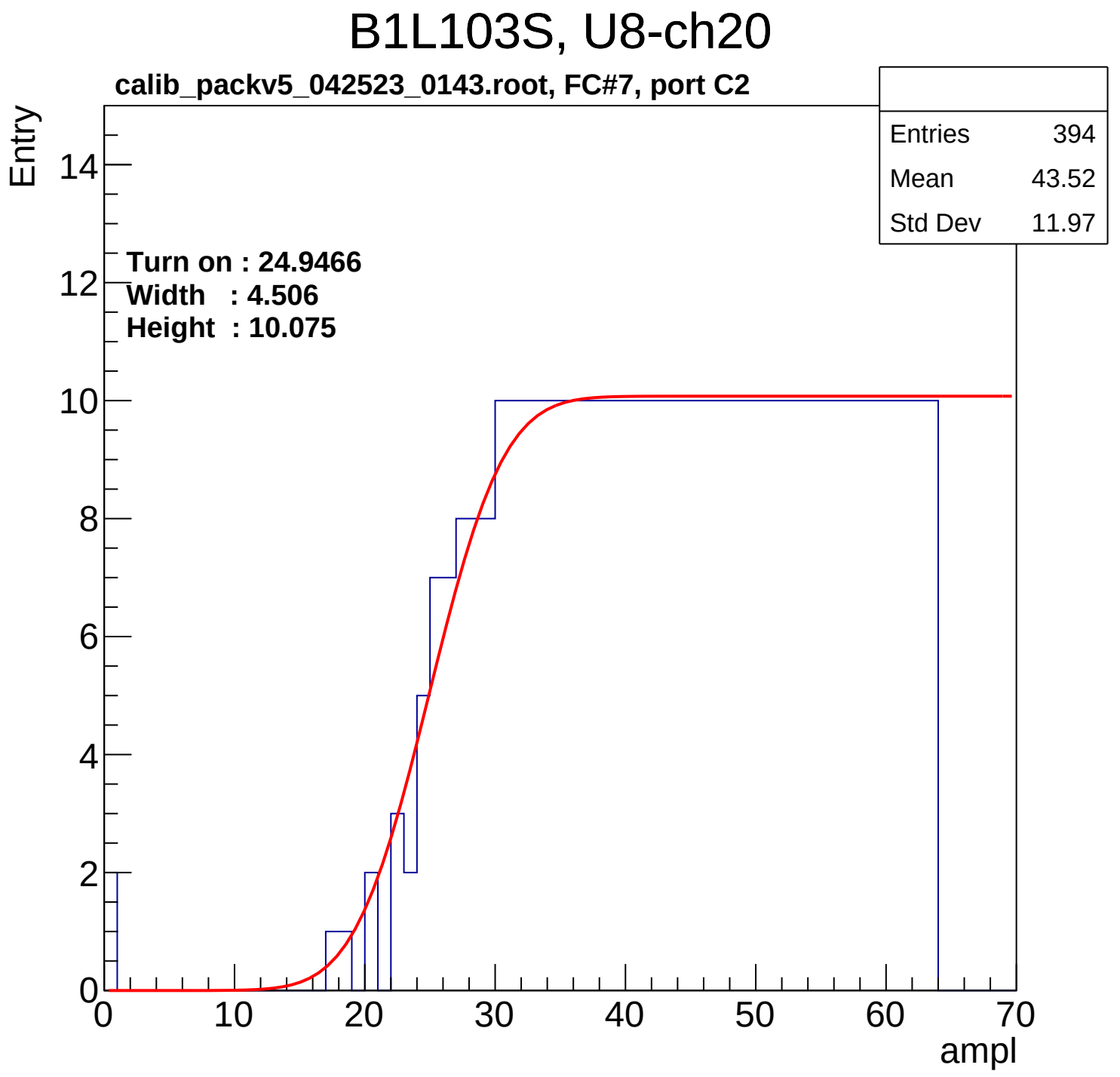
B1L103S, U8-ch20
calib_packv5_042523_0143.root, FC#7, port C2
Entries 394
Mean 43.52
Std Dev 11.97
Turn on : 24.9466
Width : 4.506
Height : 10.075
Entry
ampl
0
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8
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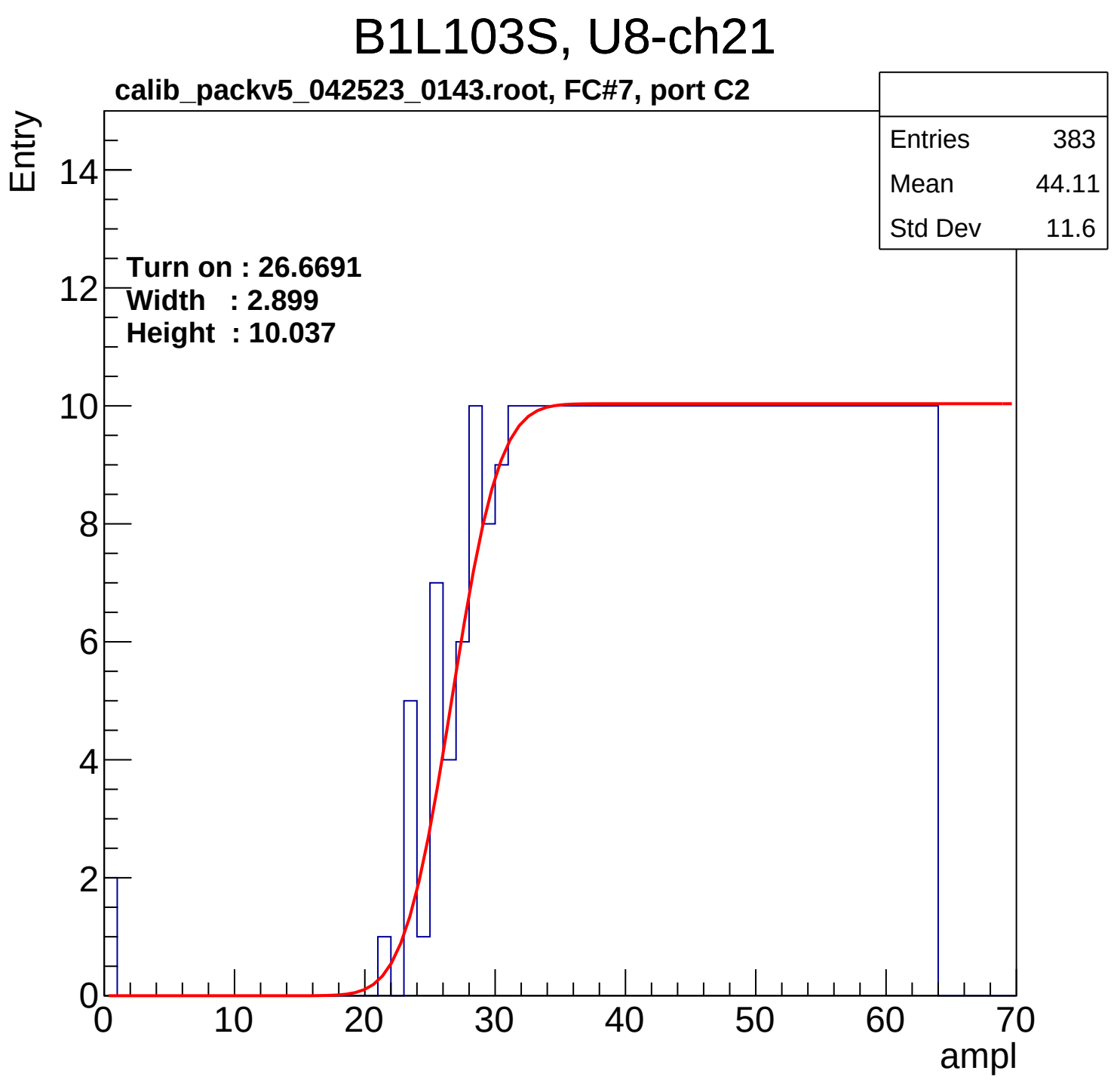
B1L103S, U8-ch21
calib_packv5_042523_0143.root, FC#7, port C2
Entries 383
Mean 44.11
Std Dev 11.6
Turn on : 26.6691
Width : 2.899
Height : 10.037
Entry
ampl
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8
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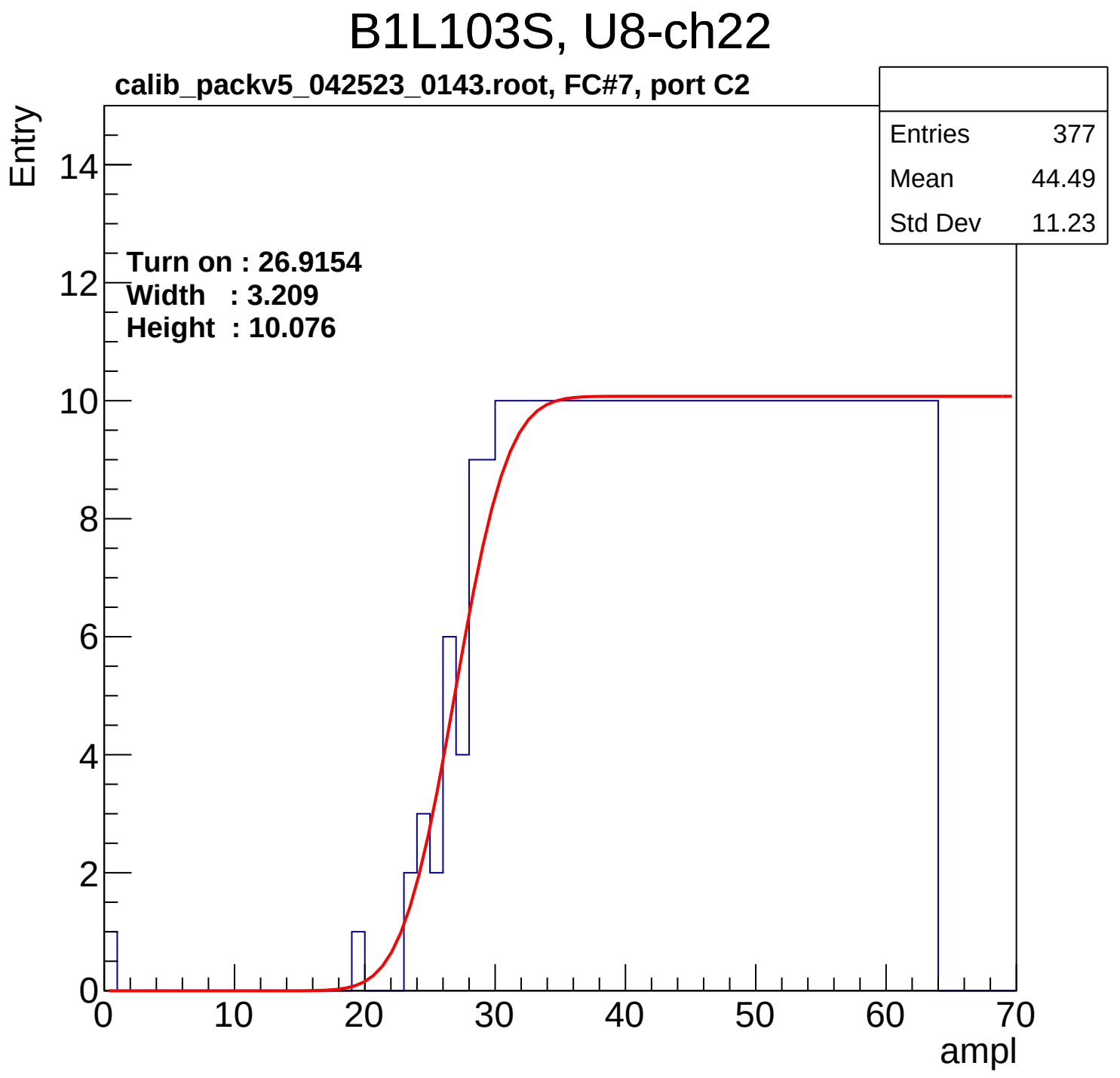
B1L103S, U8-ch22
calib_packv5_042523_0143.root, FC#7, port C2
Entries 377
Mean 44.49
Std Dev 11.23
Turn on : 26.9154
Width : 3.209
Height : 10.076
Entry
ampl
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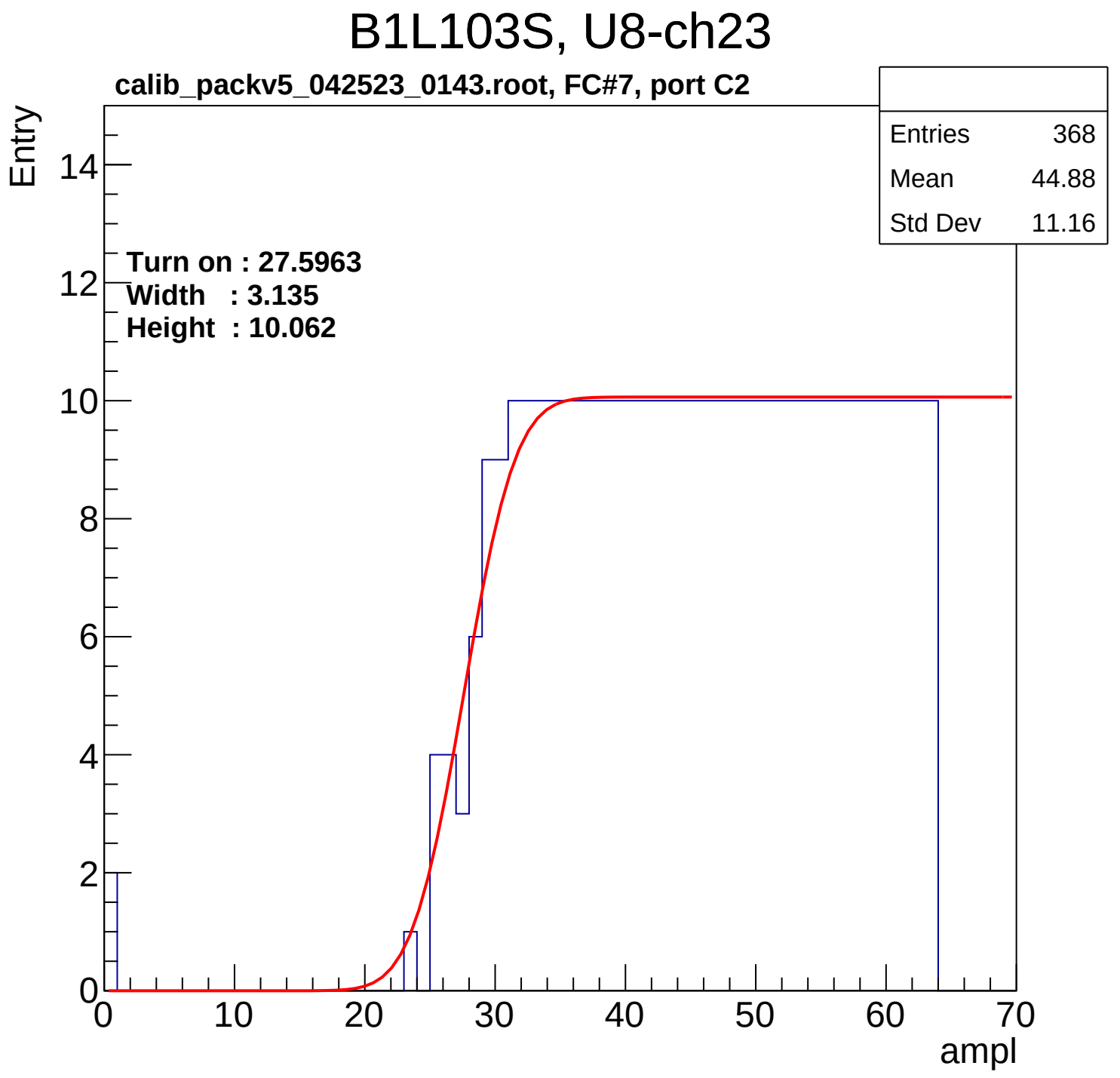
B1L103S, U8-ch23
calib_packv5_042523_0143.root, FC#7, port C2
Entries 368
Mean 44.88
Std Dev 11.16
Turn on : 27.5963
Width : 3.135
Height : 10.062
Entry
ampl
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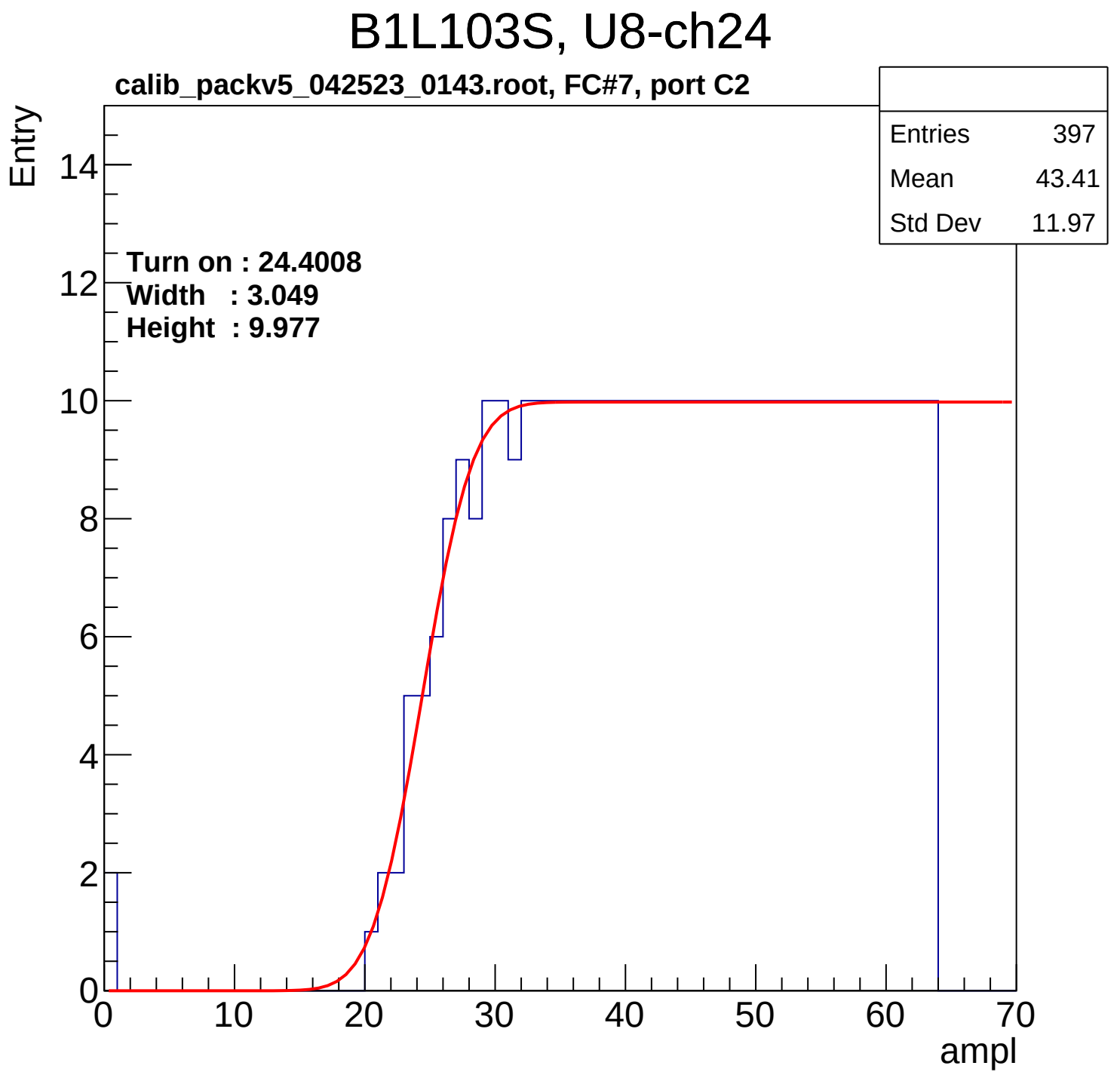
B1L103S, U8-ch24
calib_packv5_042523_0143.root, FC#7, port C2
Entries 397
Mean 43.41
Std Dev 11.97
Turn on : 24.4008
Width : 3.049
Height : 9.977
Entry
ampl
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6
8
10
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0
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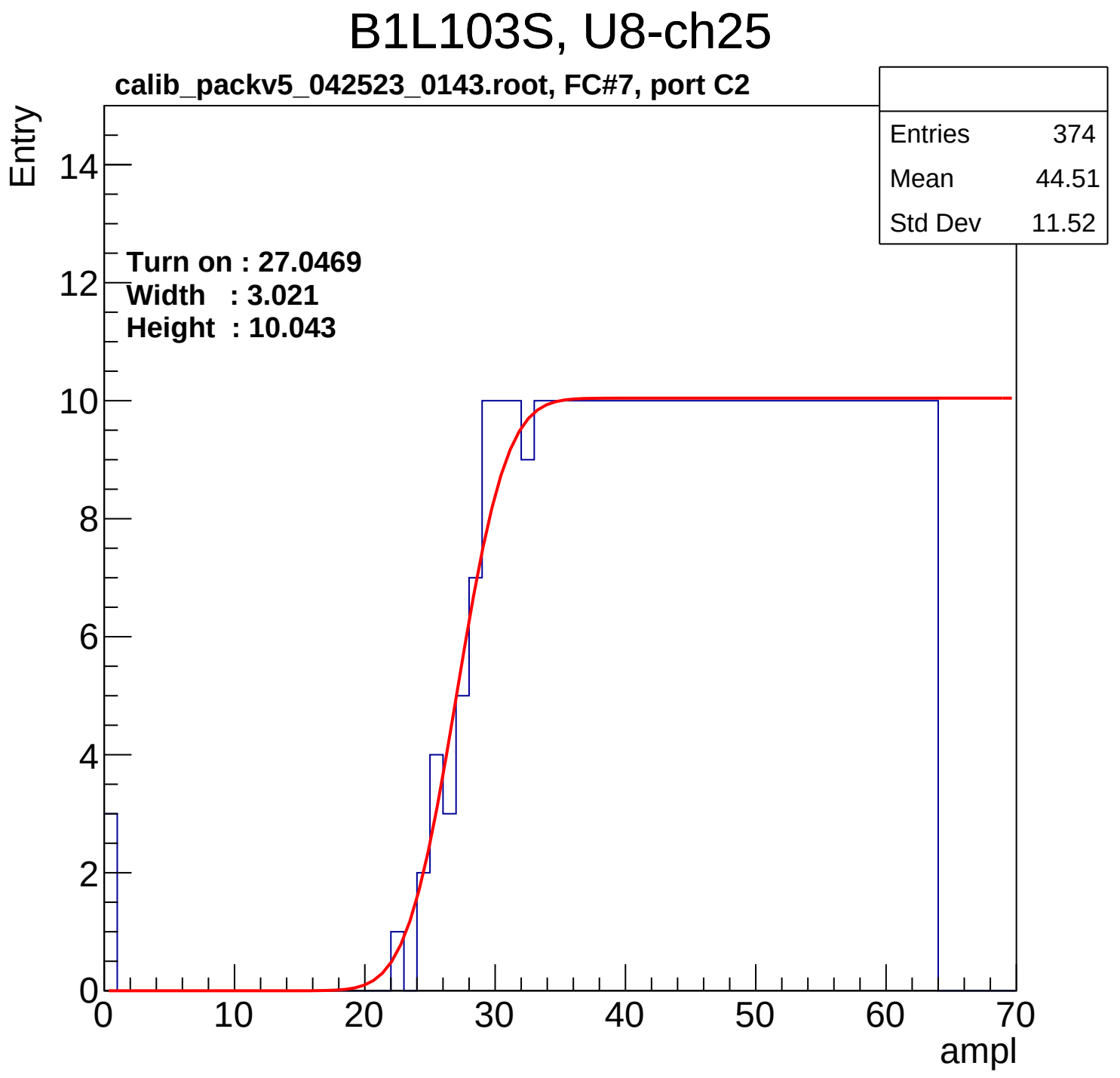
B1L103S, U8-ch25
calib_packv5_042523_0143.root, FC#7, port C2
Entries 374
Mean 44.51
Std Dev 11.52
Turn on : 27.0469
Width : 3.021
Height : 10.043
Entry
ampl
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6
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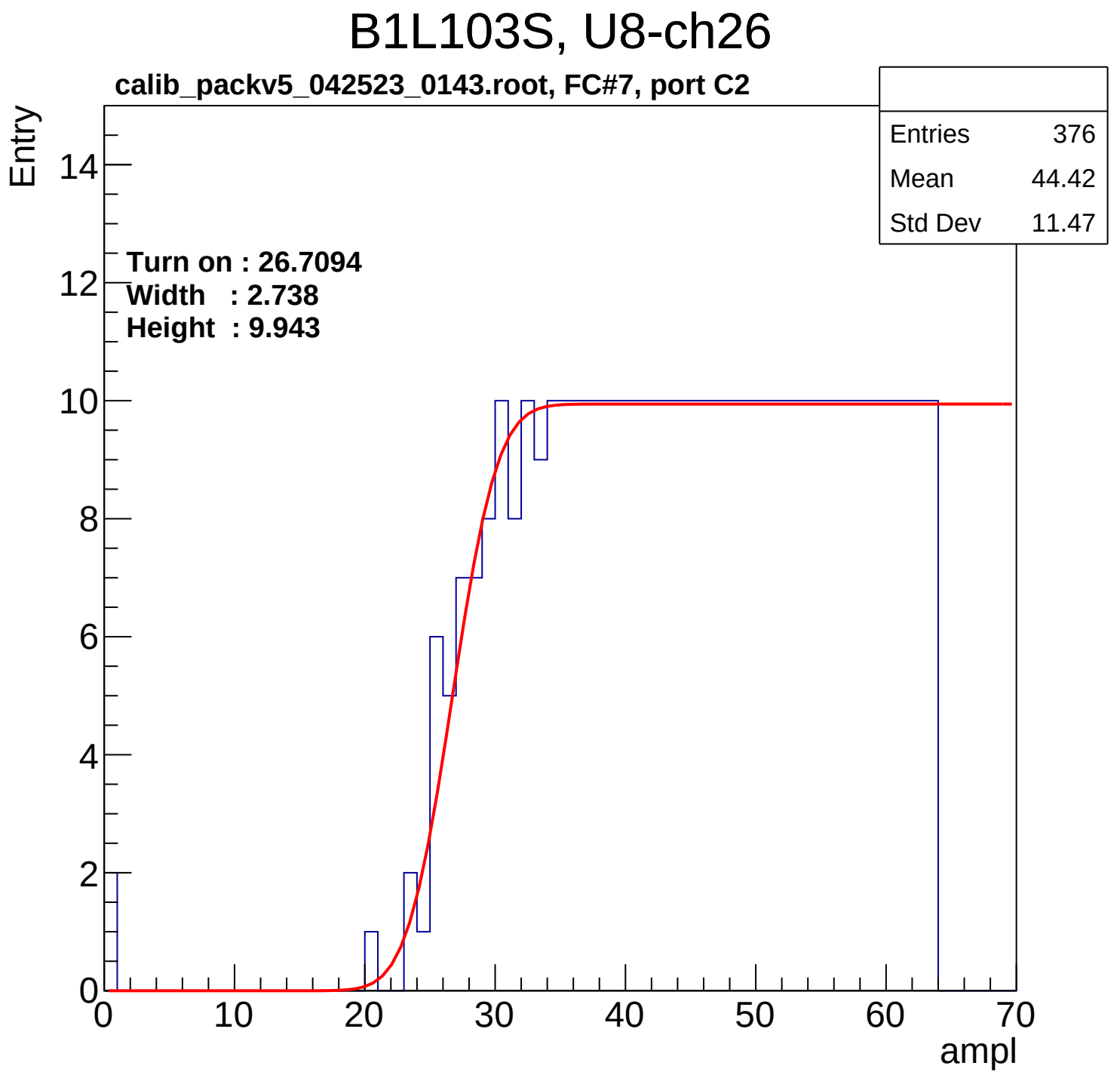
B1L103S, U8-ch26
calib_packv5_042523_0143.root, FC#7, port C2
Entries 376
Mean 44.42
Std Dev 11.47
Turn on : 26.7094
Width : 2.738
Height : 9.943
Entry
ampl
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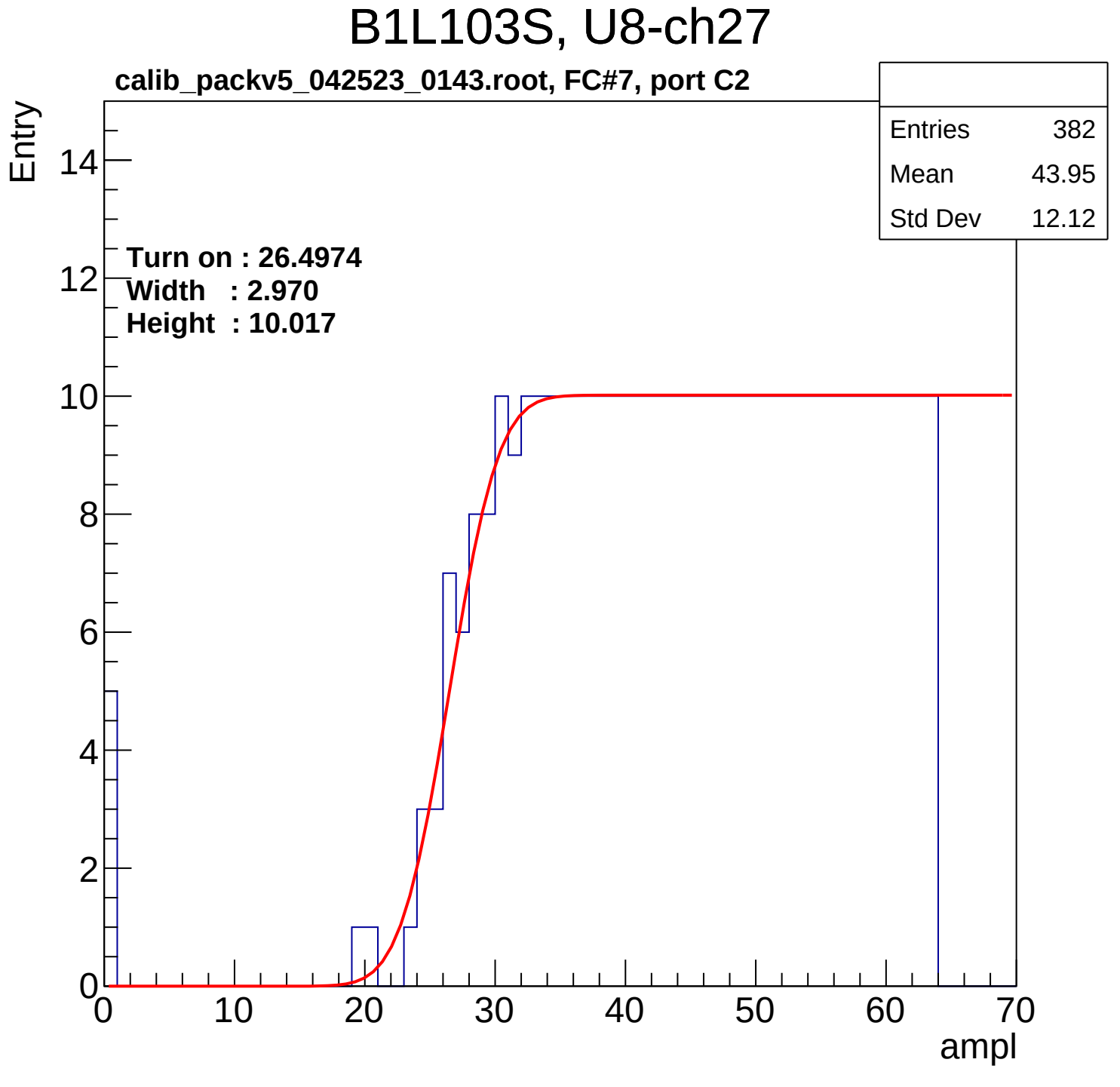
B1L103S, U8-ch27
calib_packv5_042523_0143.root, FC#7, port C2
Entries 382
Mean 43.95
Std Dev 12.12
Turn on : 26.4974
Width : 2.970
Height : 10.017
Entry
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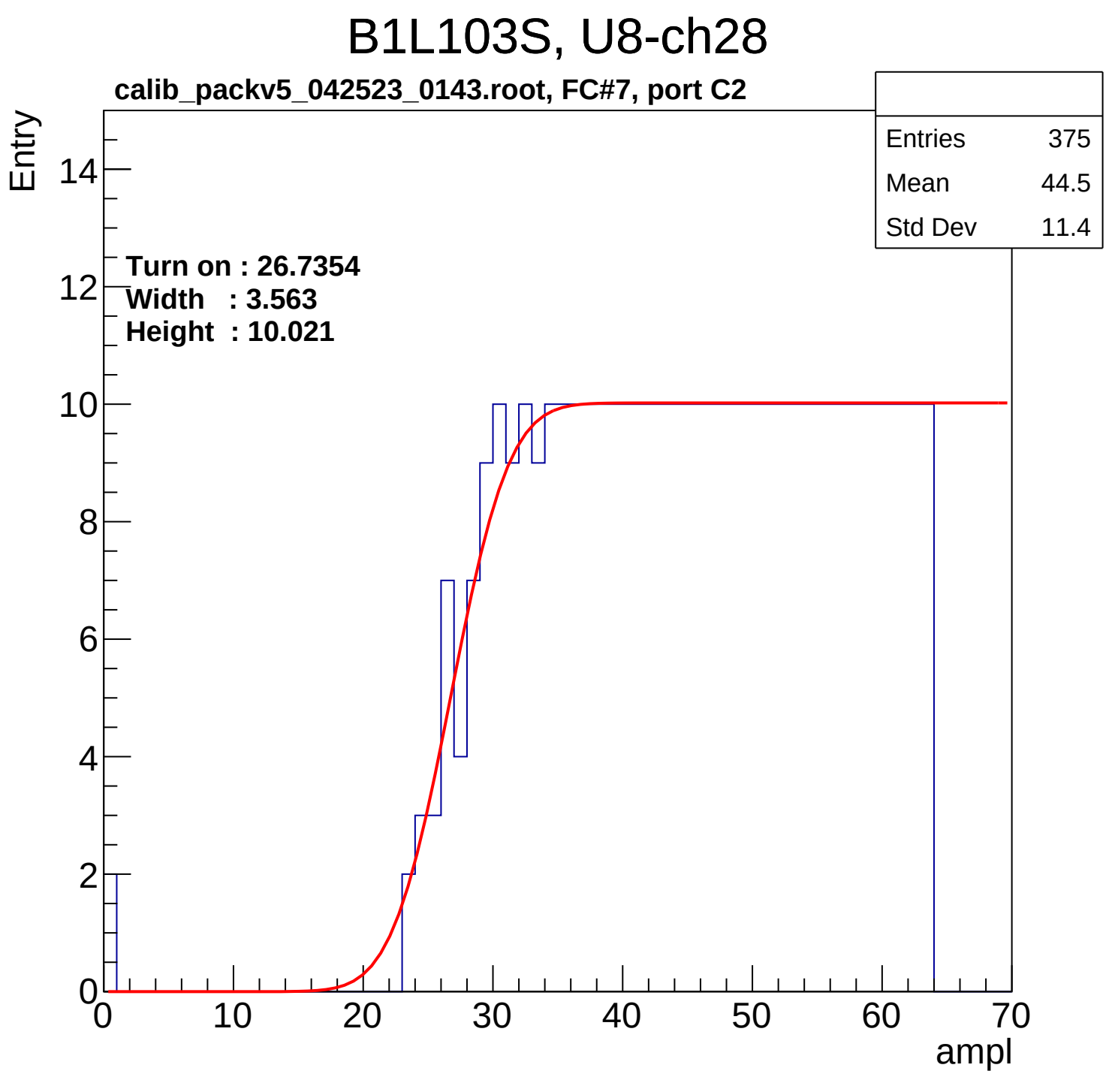
B1L103S, U8-ch28
calib_packv5_042523_0143.root, FC#7, port C2
Entries 375
Mean 44.5
Std Dev 11.4
Turn on : 26.7354
Width : 3.563
Height : 10.021
Entry
ampl
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4
6
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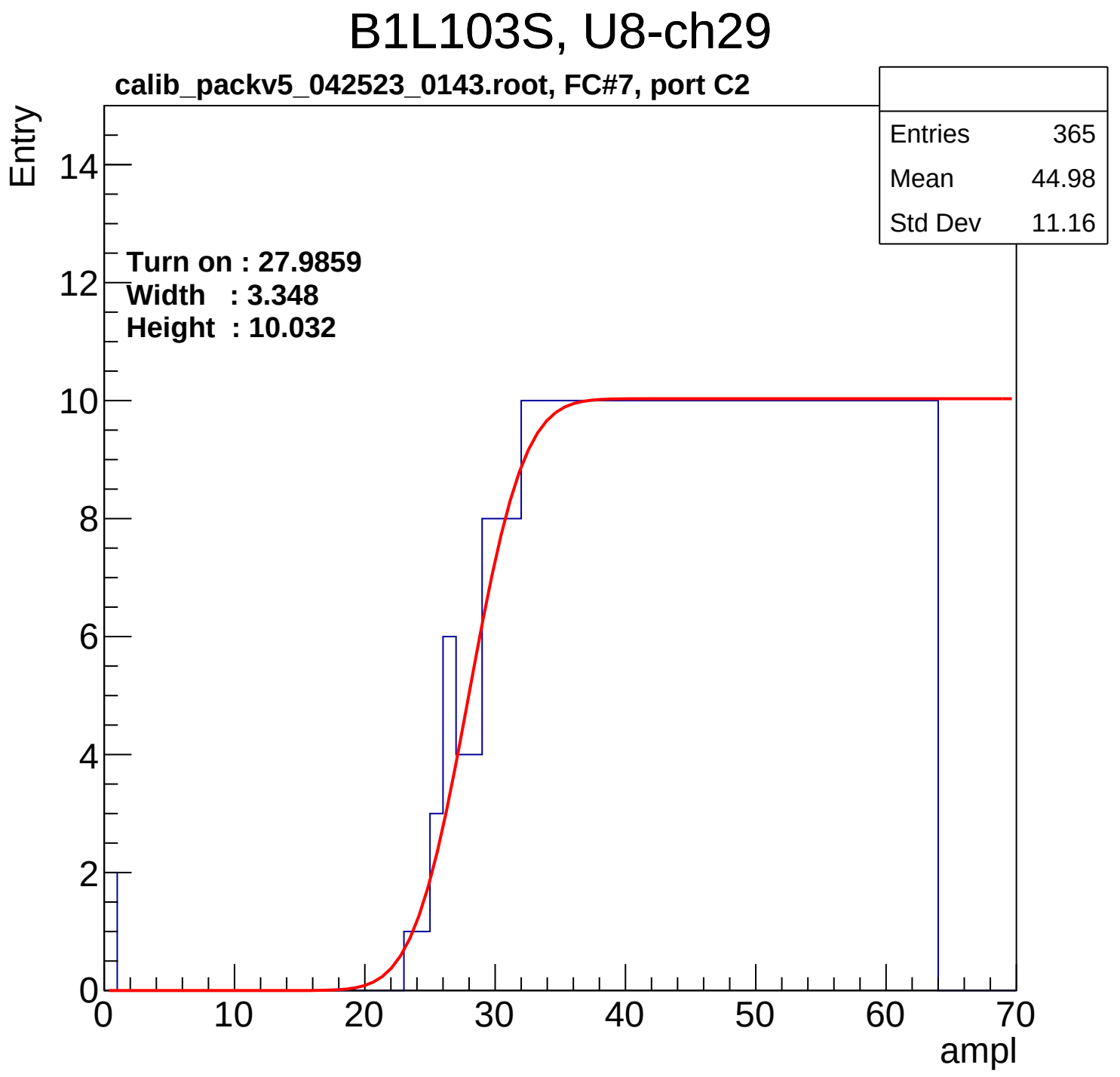
B1L103S, U8-ch29
calib_packv5_042523_0143.root, FC#7, port C2
Entries 365
Mean 44.98
Std Dev 11.16
Turn on : 27.9859
Width : 3.348
Height : 10.032
Entry
ampl
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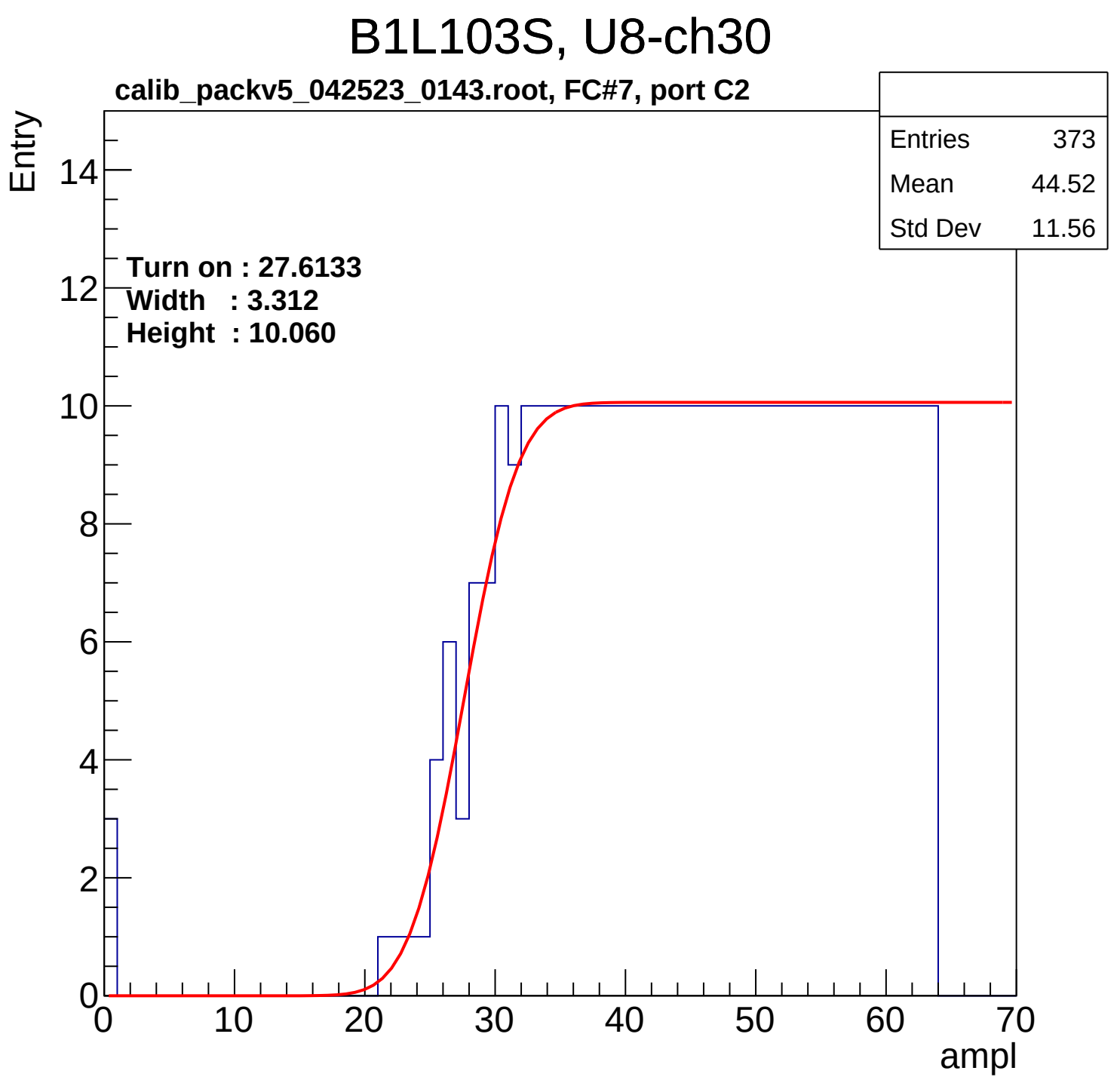
B1L103S, U8-ch30
calib_packv5_042523_0143.root, FC#7, port C2
Entries 373
Mean 44.52
Std Dev 11.56
Turn on : 27.6133
Width : 3.312
Height : 10.060
Entry
ampl
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2
4
6
8
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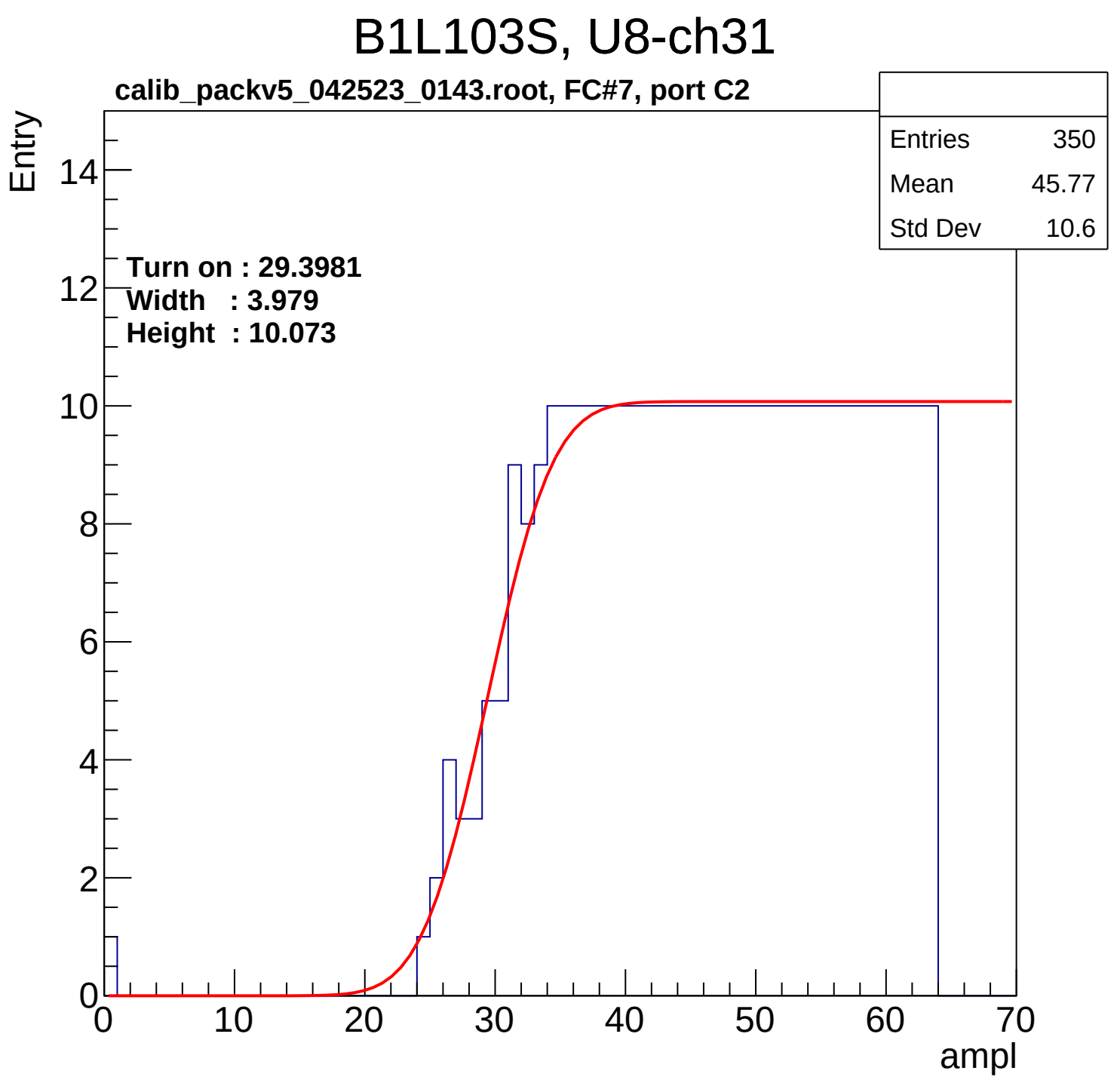
B1L103S, U8-ch31
calib_packv5_042523_0143.root, FC#7, port C2
Entries 350
Mean 45.77
Std Dev 10.6
Turn on : 29.3981
Width : 3.979
Height : 10.073
Entry
ampl
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2
4
6
8
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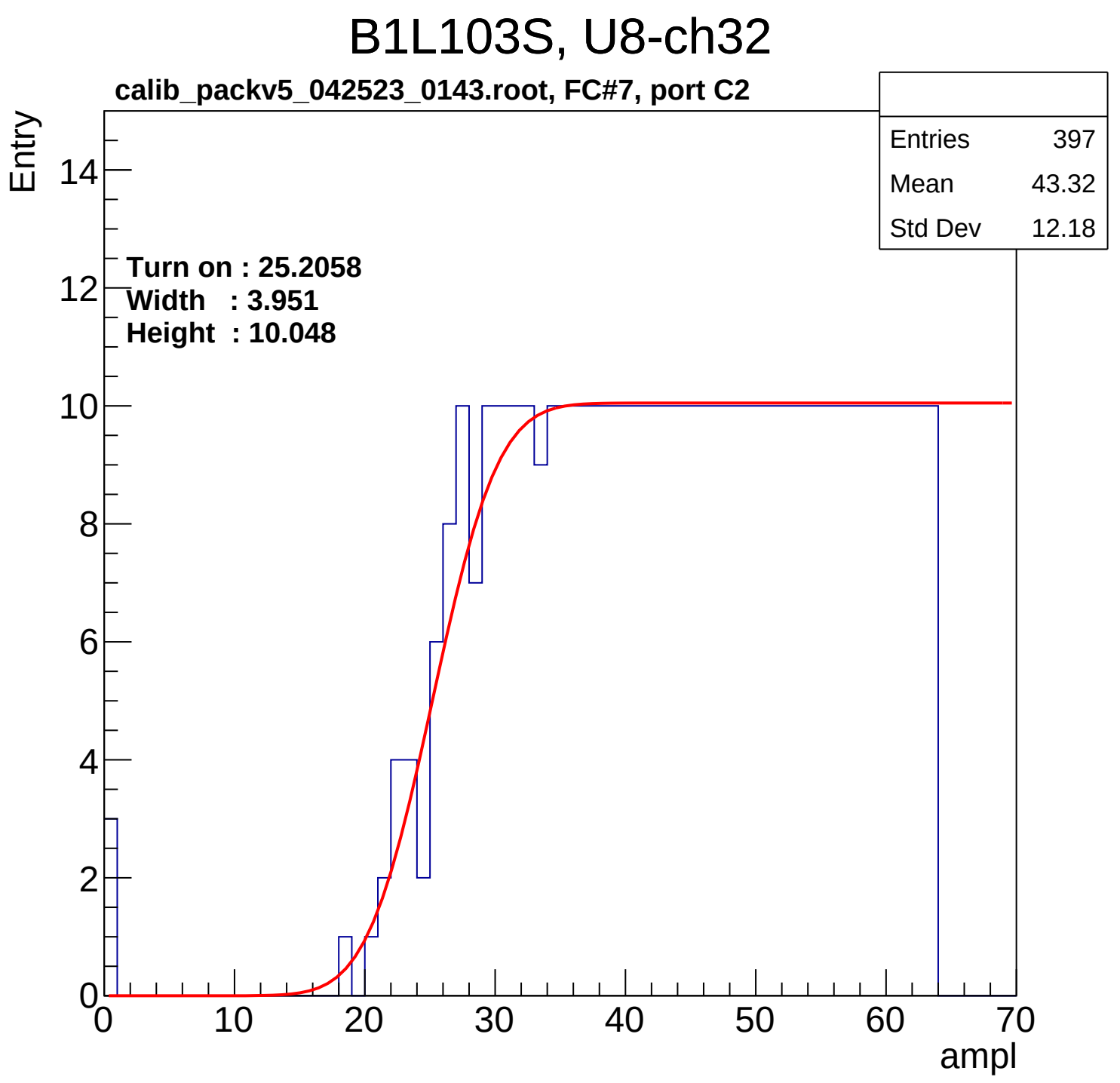
B1L103S, U8-ch32
calib_packv5_042523_0143.root, FC#7, port C2
Entries 397
Mean 43.32
Std Dev 12.18
Turn on : 25.2058
Width : 3.951
Height : 10.048
Entry
ampl
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2
4
6
8
10
12
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0
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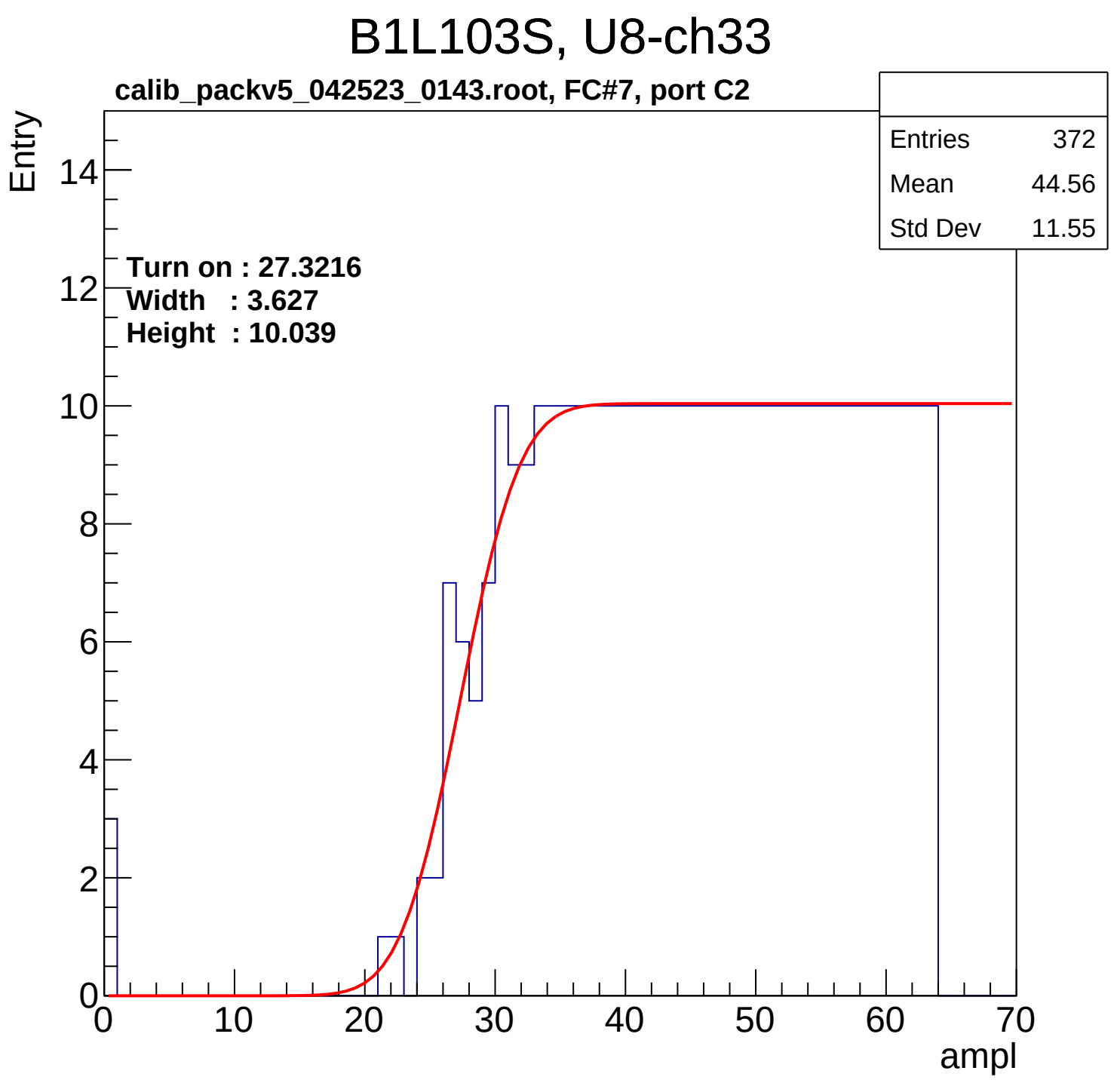
B1L103S, U8-ch33
calib_packv5_042523_0143.root, FC#7, port C2
Entries 372
Mean 44.56
Std Dev 11.55
Turn on : 27.3216
Width : 3.627
Height : 10.039
Entry
ampl
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8
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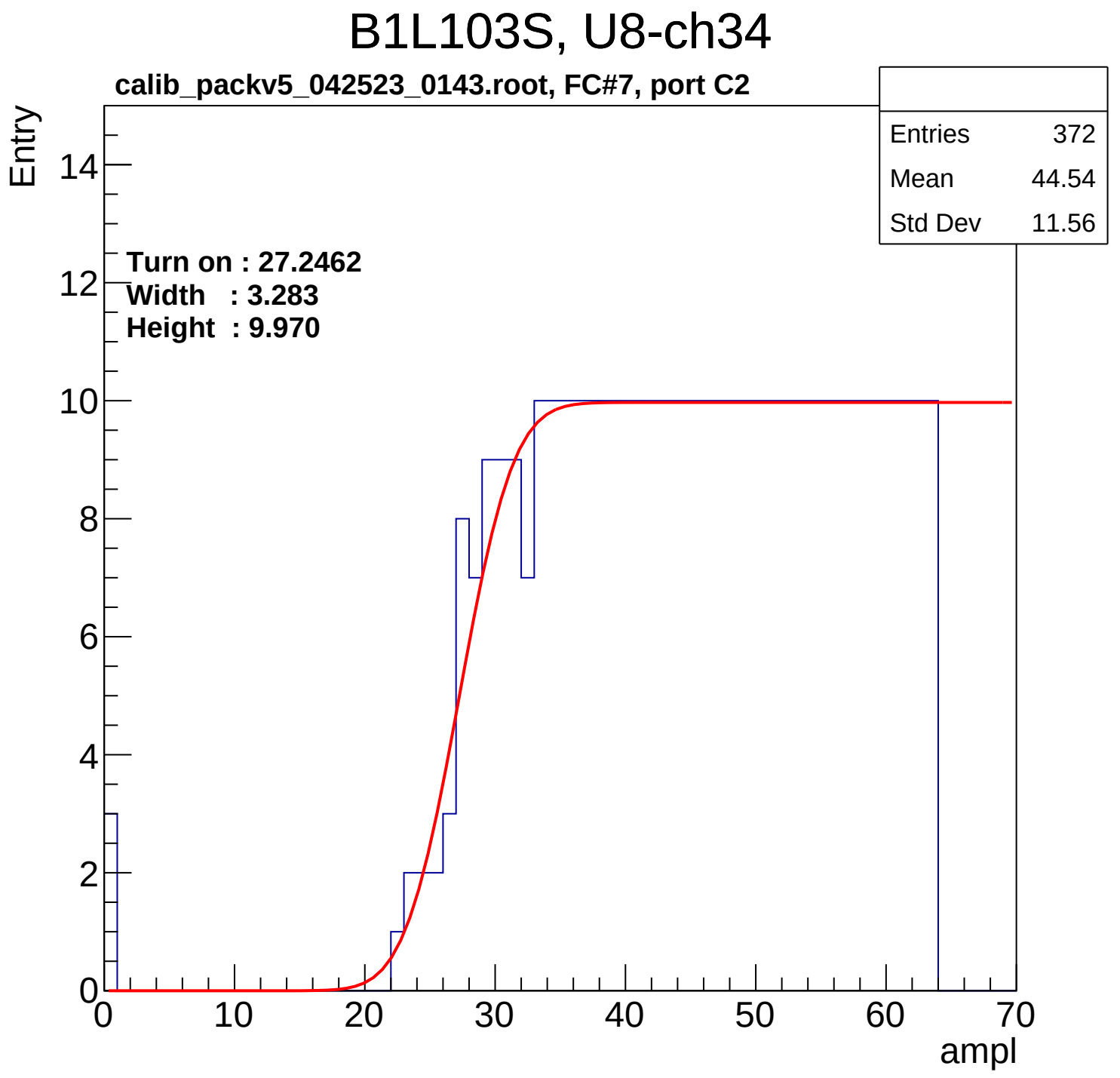
B1L103S, U8-ch34
calib_packv5_042523_0143.root, FC#7, port C2
Entries 372
Mean 44.54
Std Dev 11.56
Turn on : 27.2462
Width : 3.283
Height : 9.970
Entry
ampl
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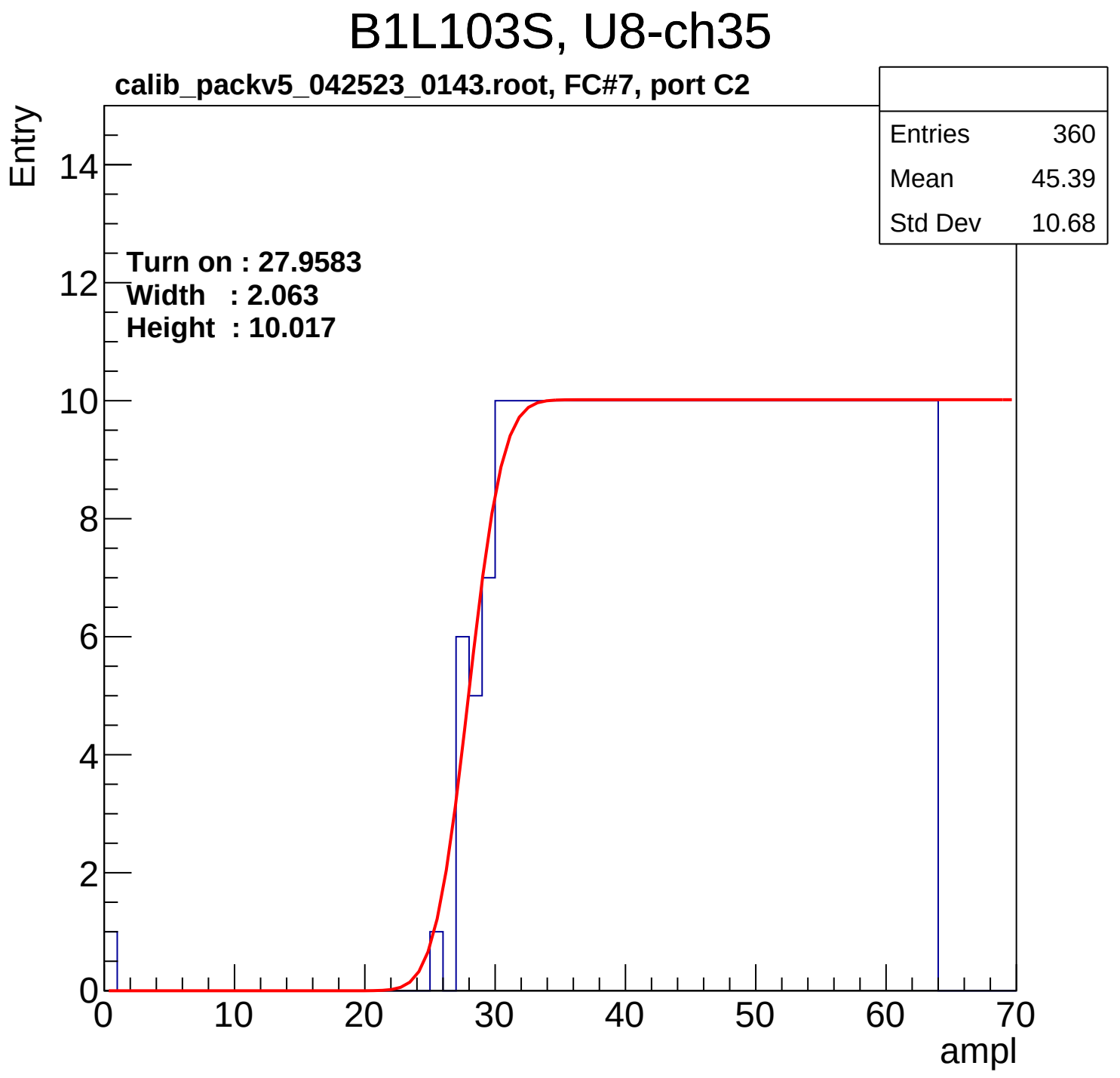
B1L103S, U8-ch35
calib_packv5_042523_0143.root, FC#7, port C2
Entries 360
Mean 45.39
Std Dev 10.68
Turn on : 27.9583
Width : 2.063
Height : 10.017
Entry
ampl
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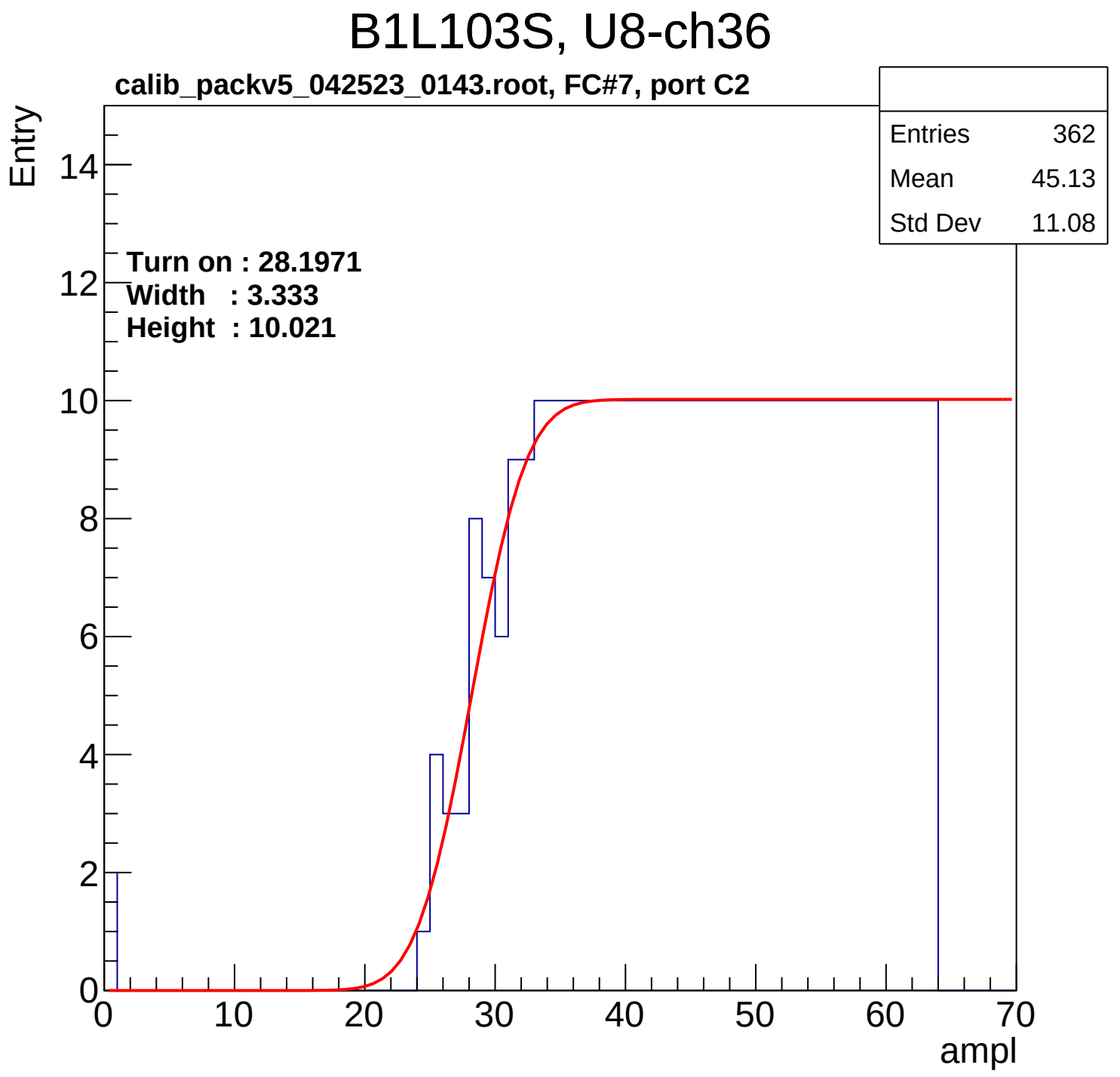
B1L103S, U8-ch36
calib_packv5_042523_0143.root, FC#7, port C2
Entries 362
Mean 45.13
Std Dev 11.08
Turn on : 28.1971
Width : 3.333
Height : 10.021
Entry
ampl
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6
8
10
12
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0
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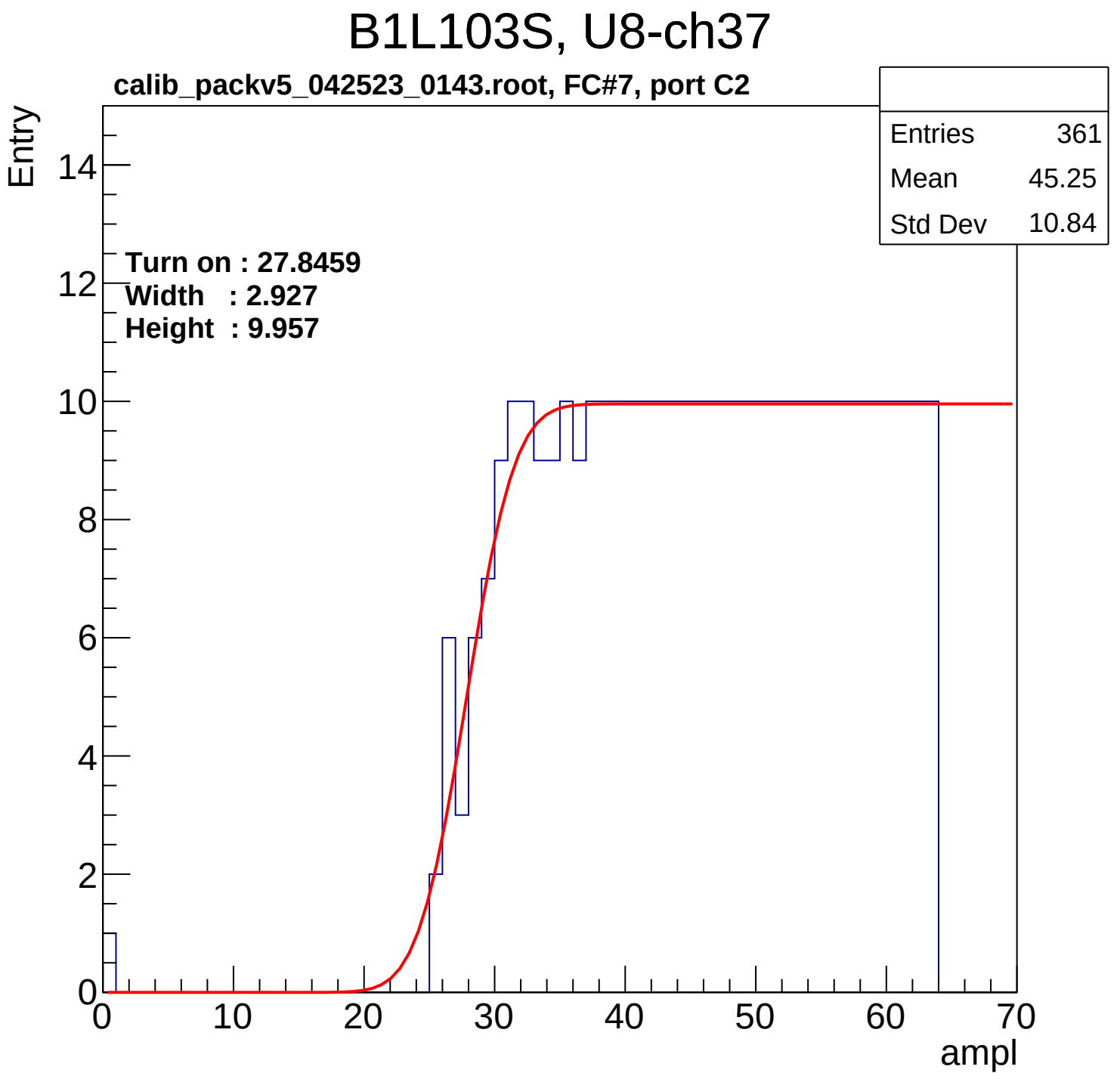
B1L103S, U8-ch37
calib_packv5_042523_0143.root, FC#7, port C2
Entries 361
Mean 45.25
Std Dev 10.84
Turn on : 27.8459
Width : 2.927
Height : 9.957
Entry
ampl
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2
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6
8
10
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0
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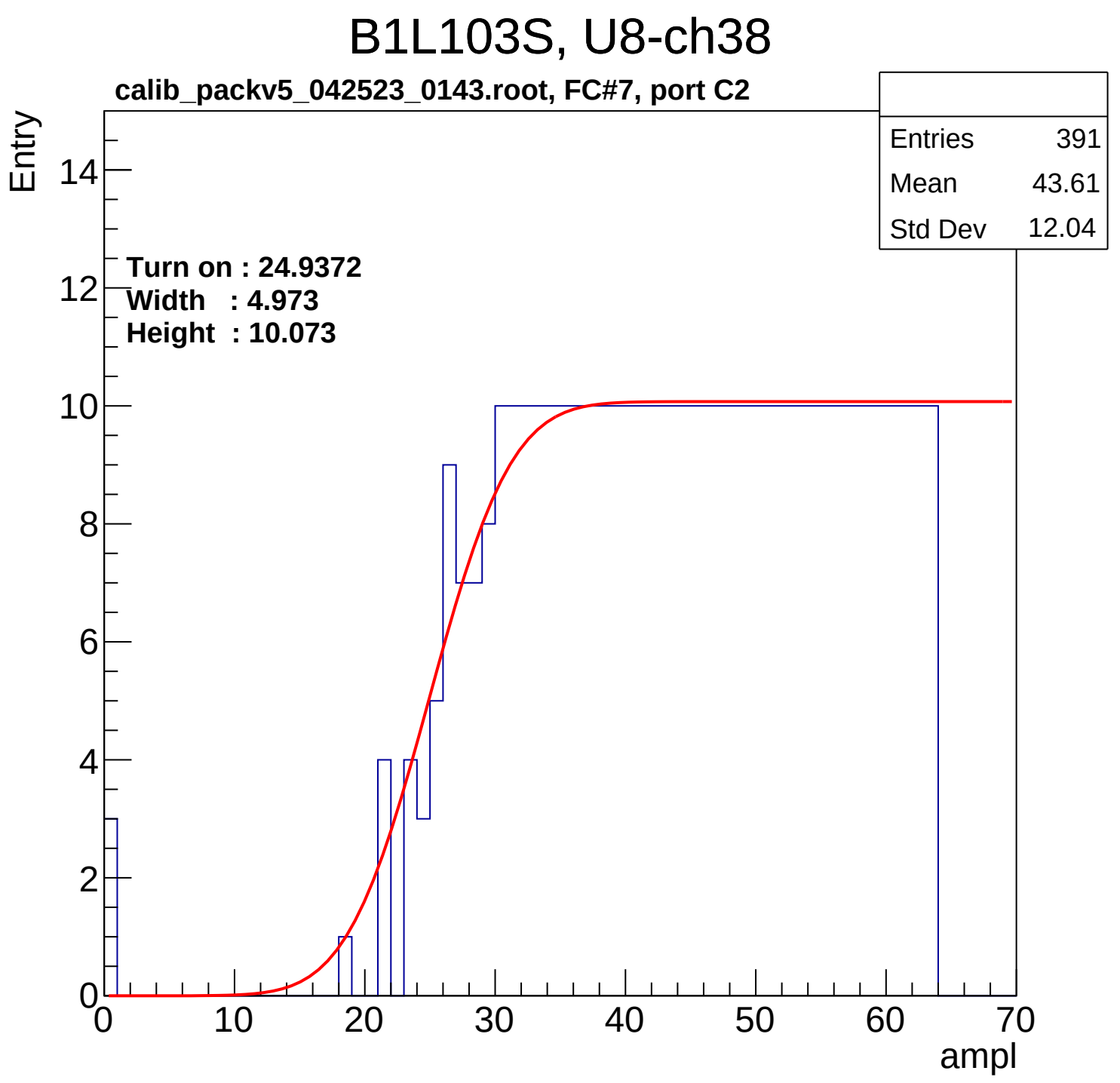
B1L103S, U8-ch38
calib_packv5_042523_0143.root, FC#7, port C2
Entries 391
Mean 43.61
Std Dev 12.04
Turn on : 24.9372
Width : 4.973
Height : 10.073
Entry
ampl
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2
4
6
8
10
12
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0
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60
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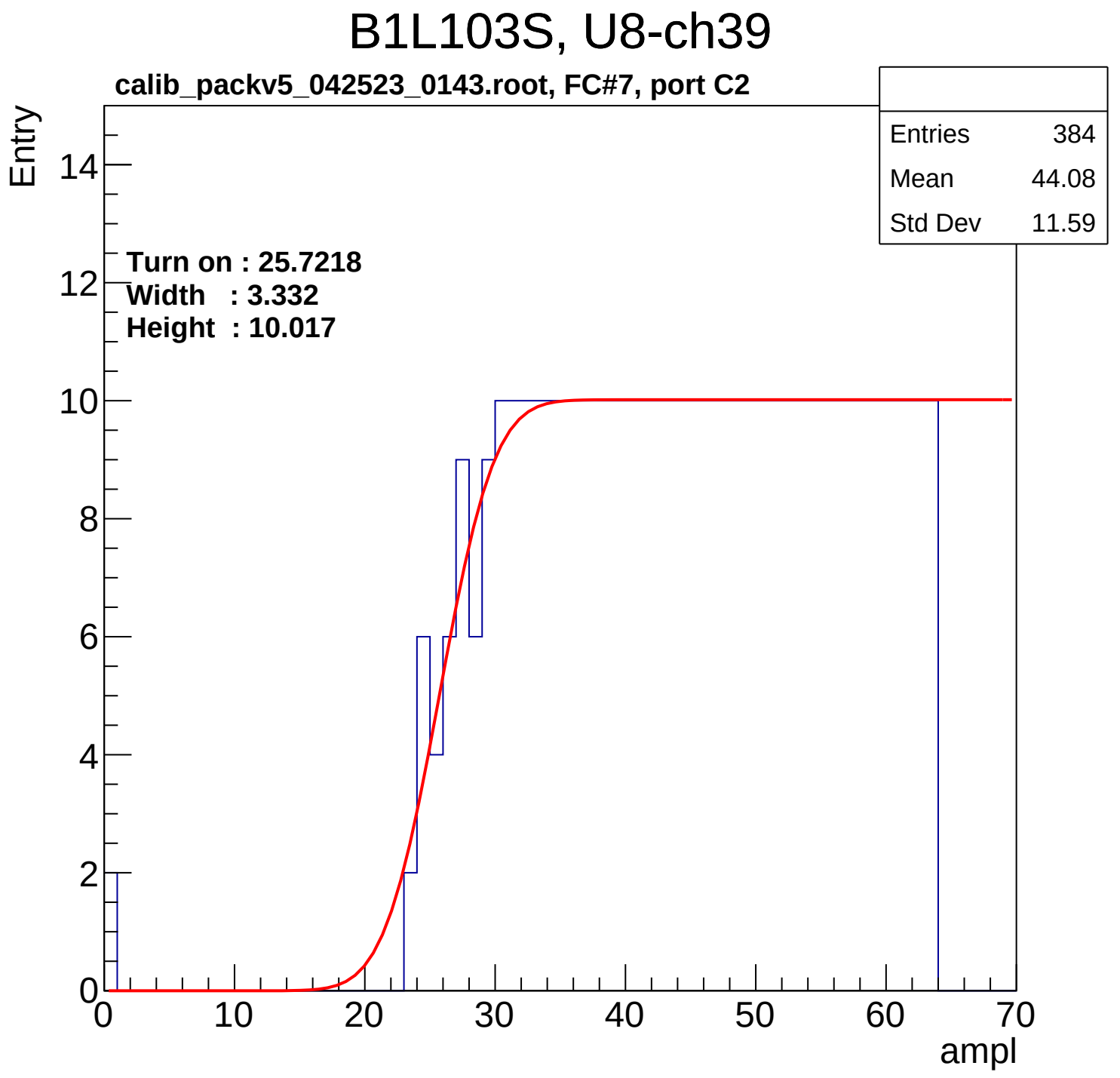
B1L103S, U8-ch39
calib_packv5_042523_0143.root, FC#7, port C2
Entries 384
Mean 44.08
Std Dev 11.59
Turn on : 25.7218
Width : 3.332
Height : 10.017
Entry
ampl
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6
8
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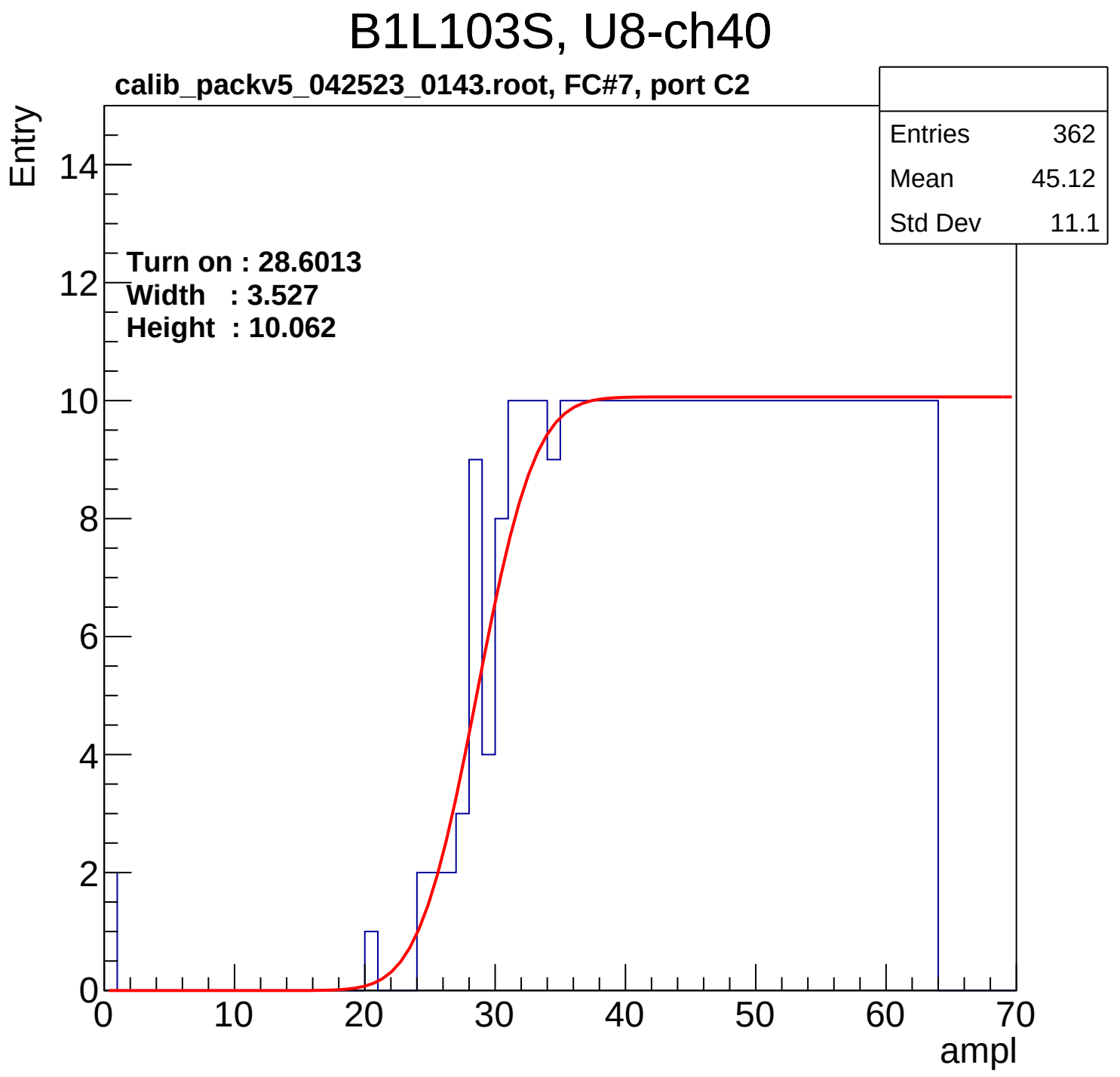
B1L103S, U8-ch40
calib_packv5_042523_0143.root, FC#7, port C2
Entries 362
Mean 45.12
Std Dev 11.1
Turn on : 28.6013
Width : 3.527
Height : 10.062
Entry
ampl
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6
8
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0
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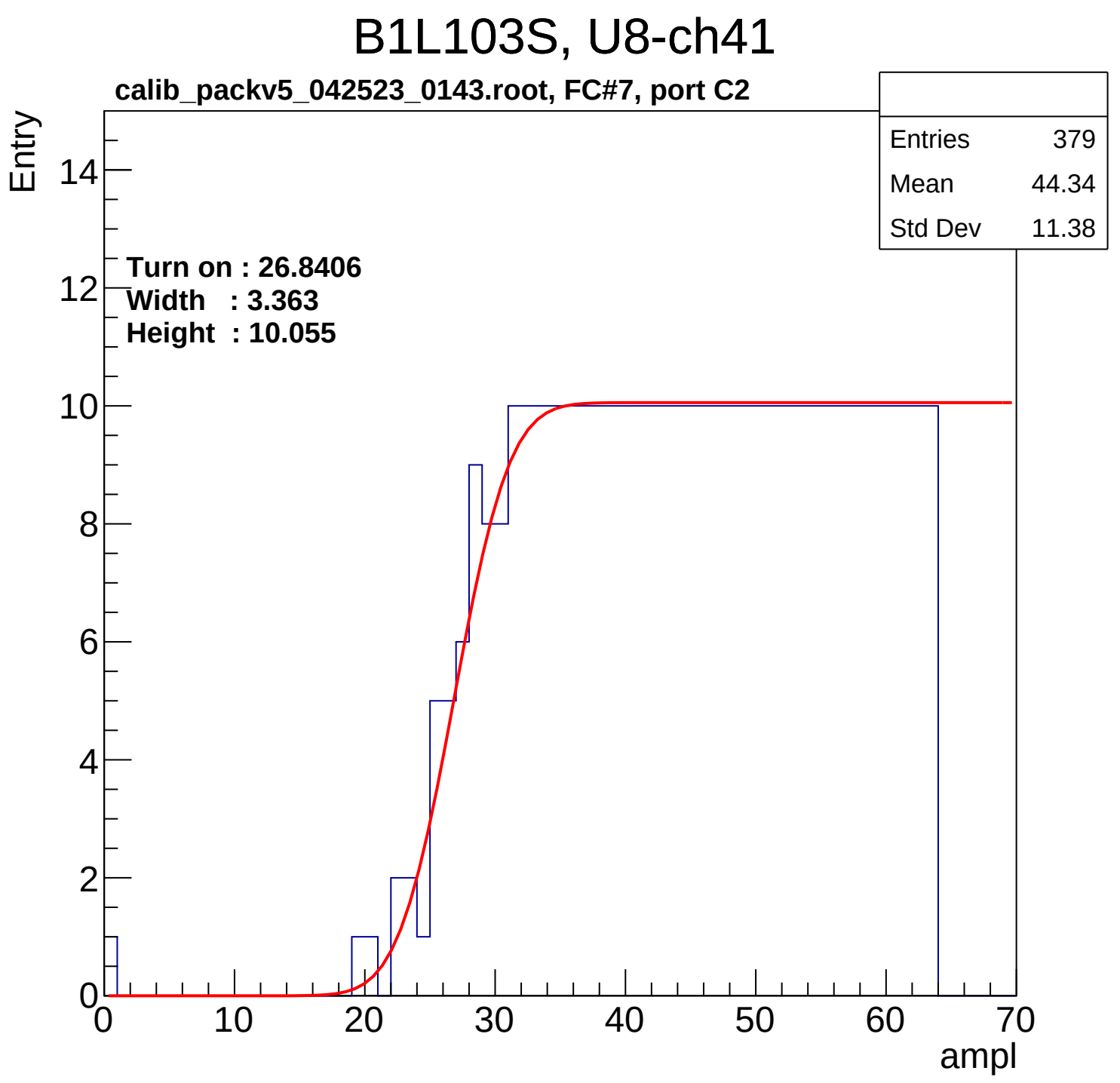
B1L103S, U8-ch41
calib_packv5_042523_0143.root, FC#7, port C2
Entries 379
Mean 44.34
Std Dev 11.38
Turn on : 26.8406
Width : 3.363
Height : 10.055
Entry
ampl
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6
8
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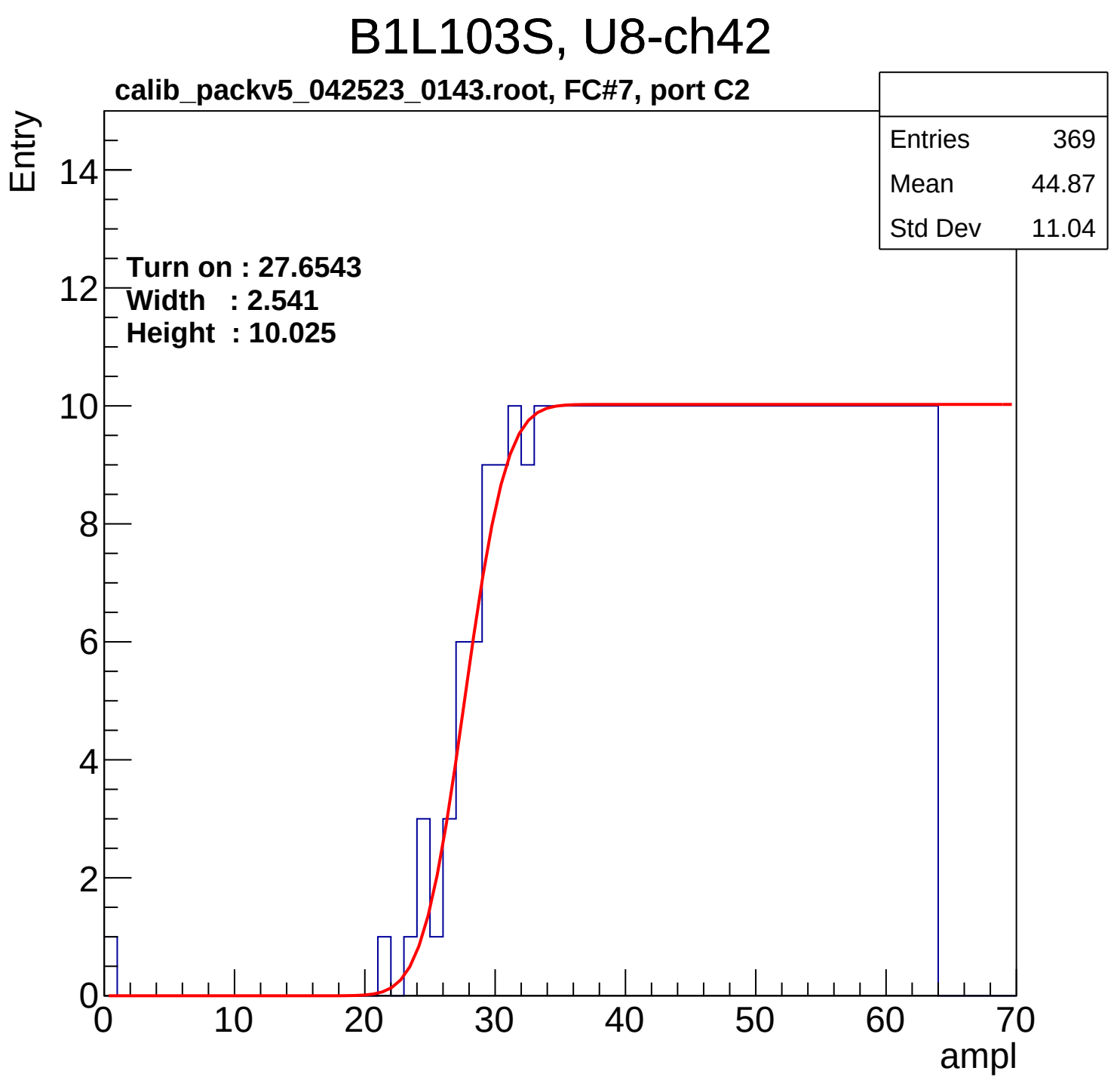
B1L103S, U8-ch42
calib_packv5_042523_0143.root, FC#7, port C2
Entries 369
Mean 44.87
Std Dev 11.04
Turn on : 27.6543
Width : 2.541
Height : 10.025
Entry
ampl
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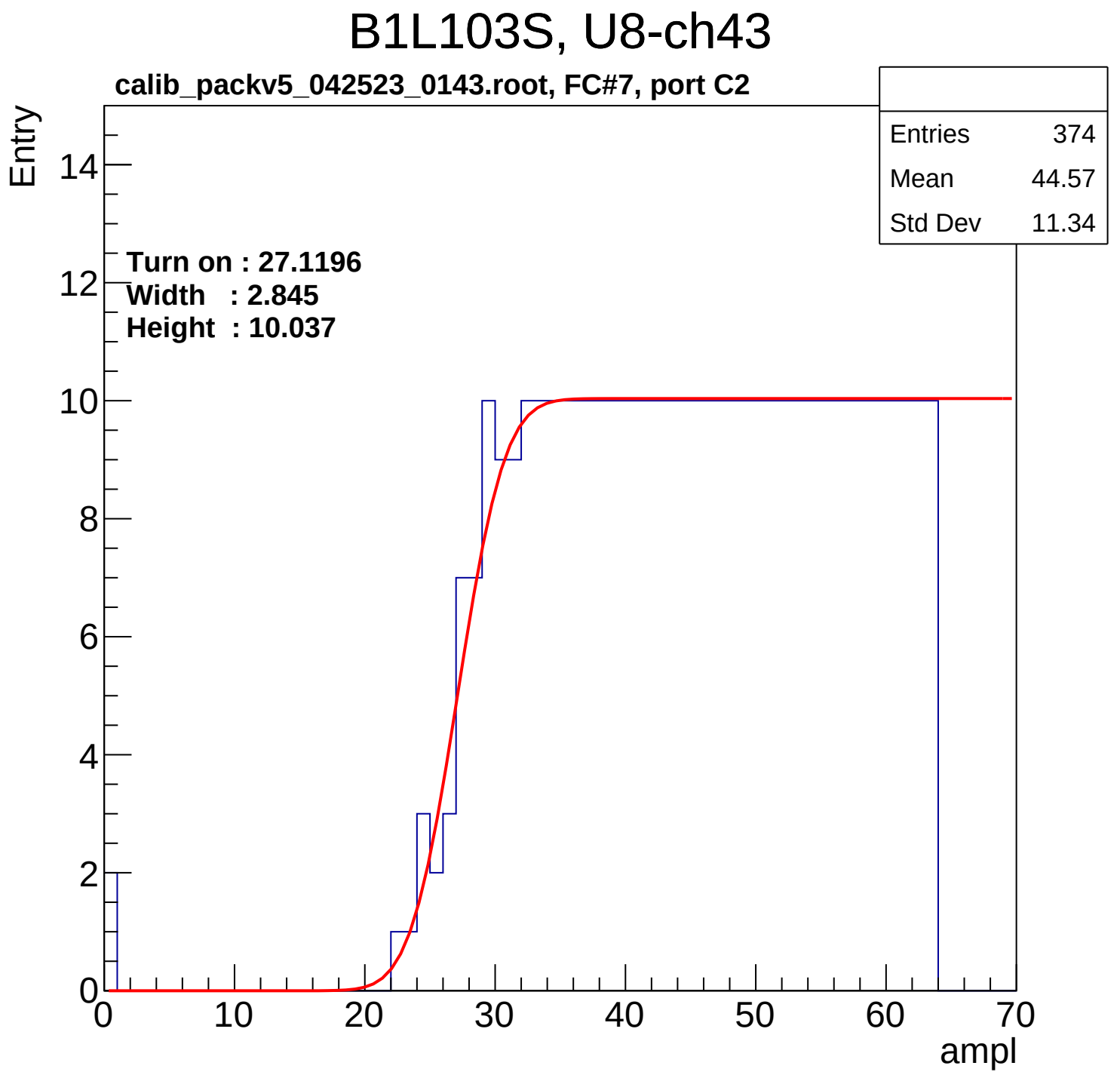
B1L103S, U8-ch43
calib_packv5_042523_0143.root, FC#7, port C2
Entries 374
Mean 44.57
Std Dev 11.34
Turn on : 27.1196
Width : 2.845
Height : 10.037
Entry
ampl
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6
8
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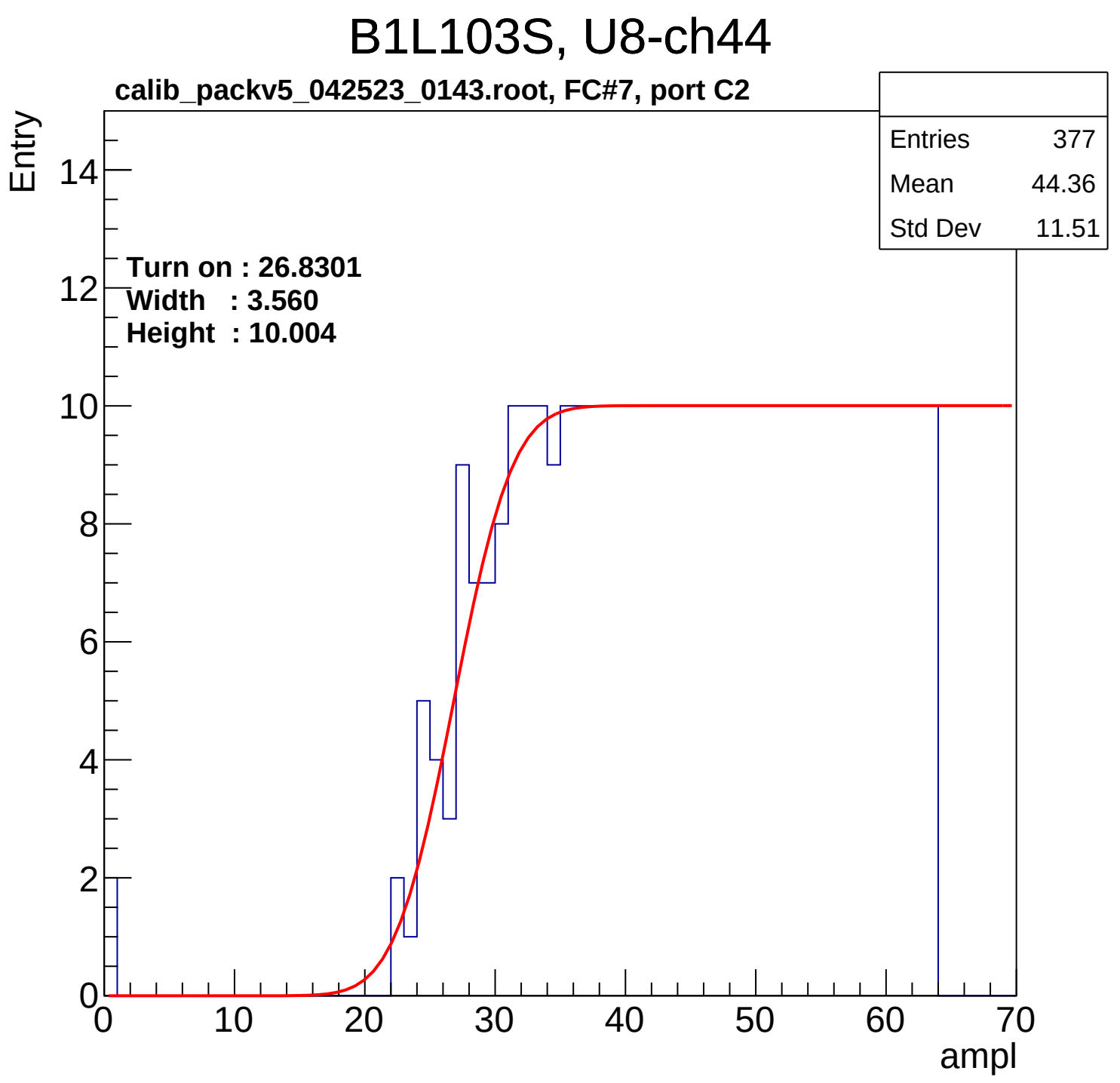
B1L103S, U8-ch44
calib_packv5_042523_0143.root, FC#7, port C2
Entries 377
Mean 44.36
Std Dev 11.51
Turn on : 26.8301
Width : 3.560
Height : 10.004
Entry
ampl
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6
8
10
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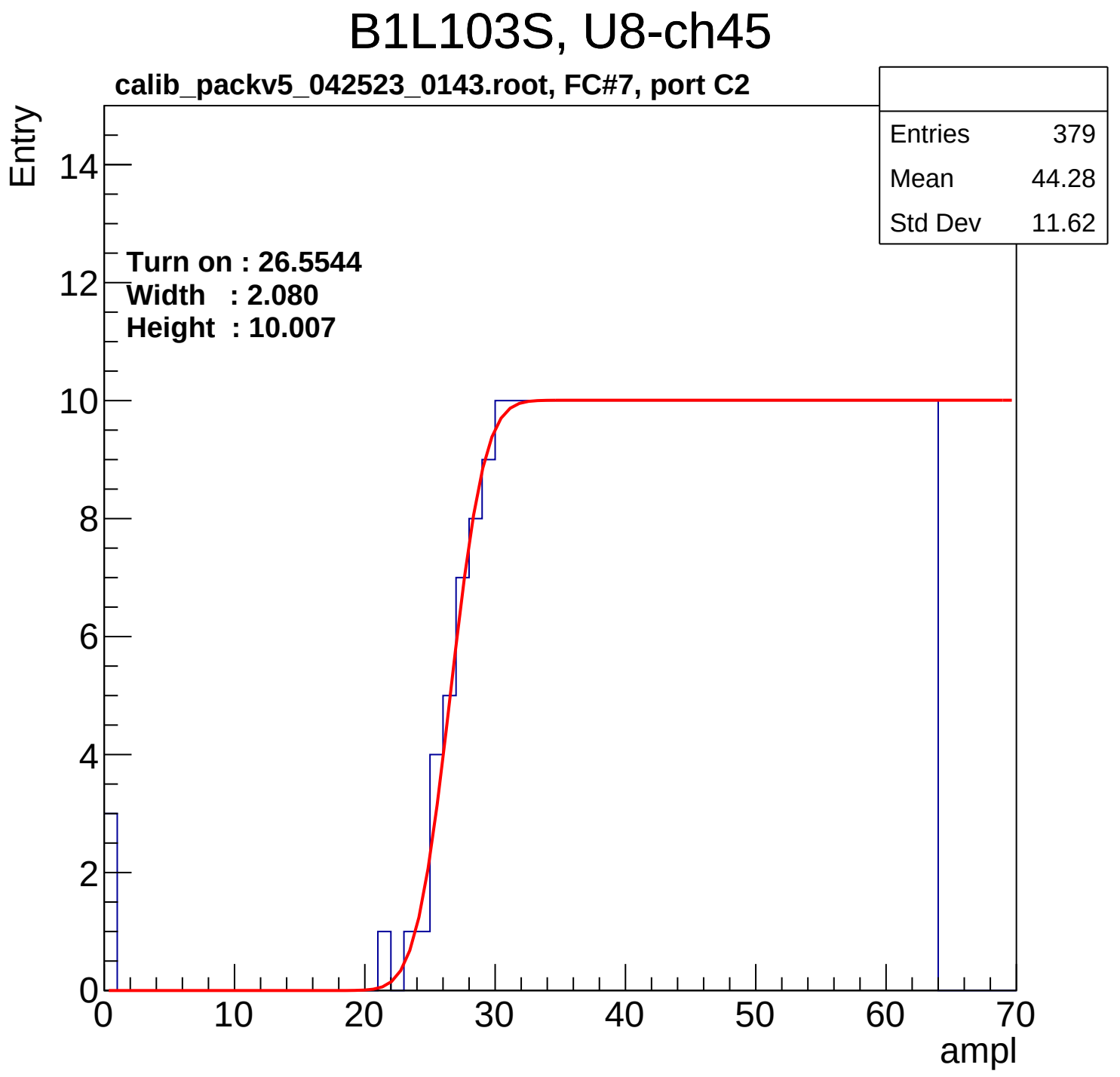
B1L103S, U8-ch45
calib_packv5_042523_0143.root, FC#7, port C2
Entries 379
Mean 44.28
Std Dev 11.62
Turn on : 26.5544
Width : 2.080
Height : 10.007
Entry
ampl
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8
10
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0
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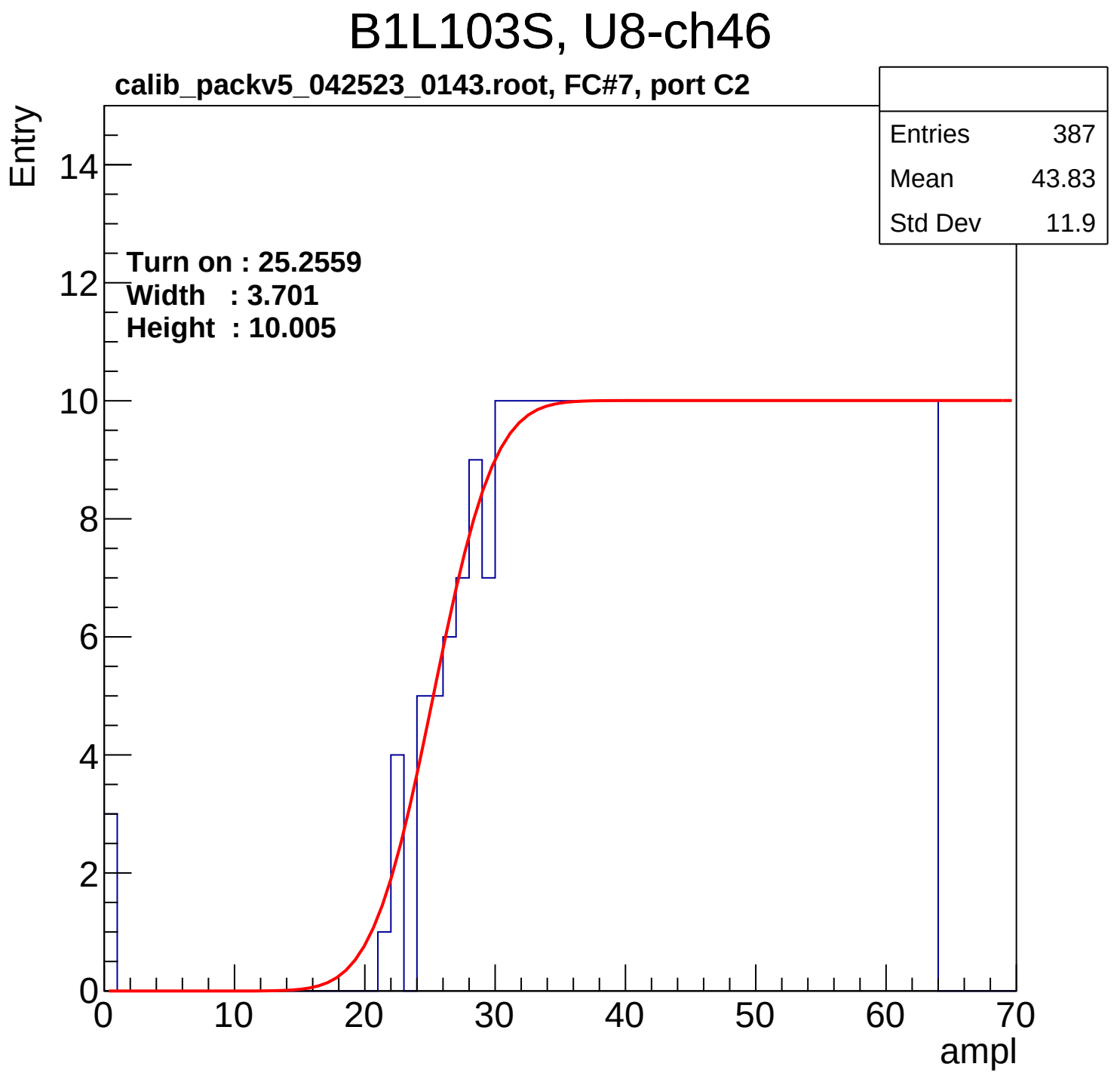
B1L103S, U8-ch46
calib_packv5_042523_0143.root, FC#7, port C2
Entries 387
Mean 43.83
Std Dev 11.9
Turn on : 25.2559
Width : 3.701
Height : 10.005
Entry
ampl
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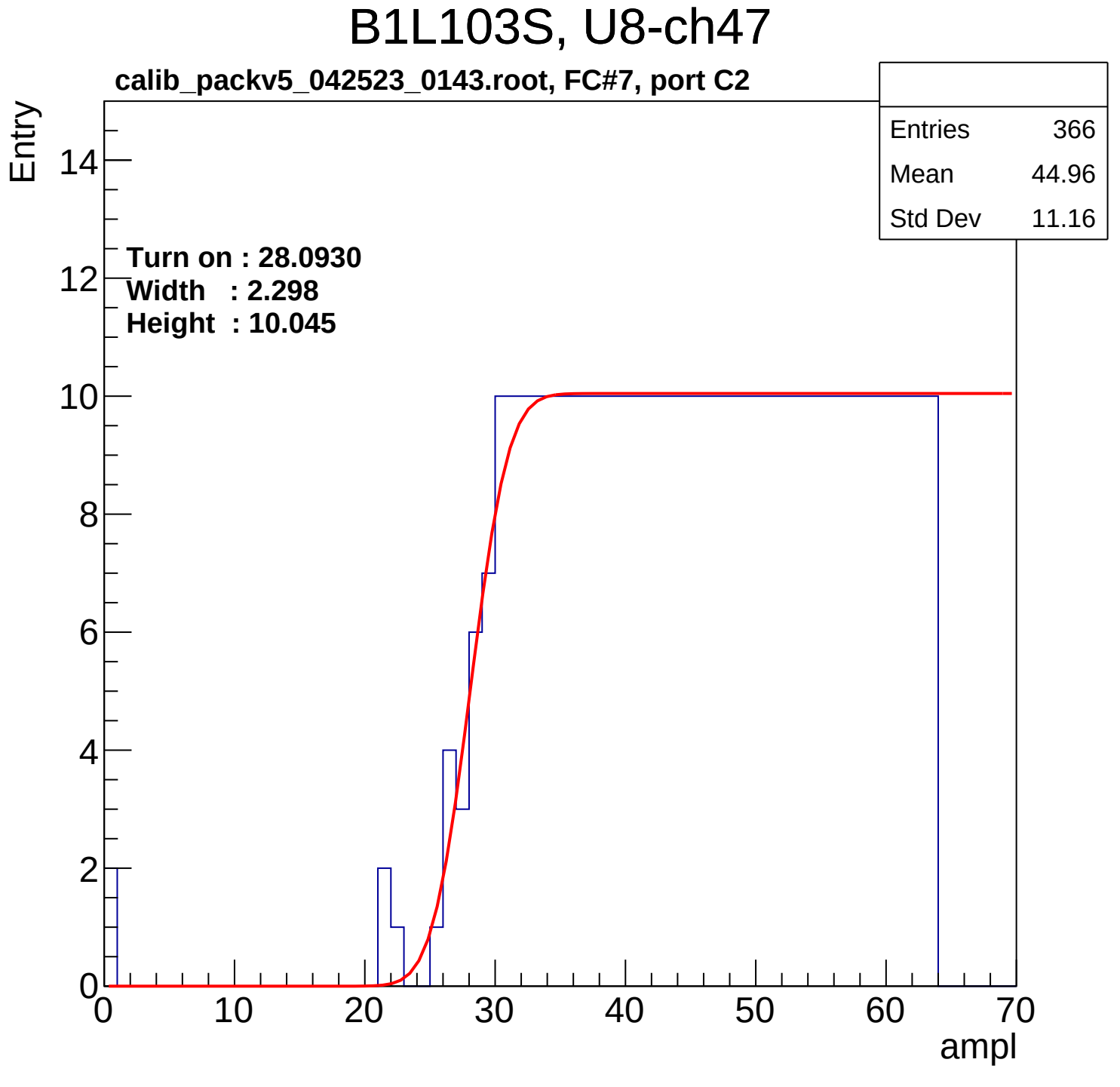
B1L103S, U8-ch47
calib_packv5_042523_0143.root, FC#7, port C2
Entries 366
Mean 44.96
Std Dev 11.16
Turn on : 28.0930
Width : 2.298
Height : 10.045
Entry
ampl
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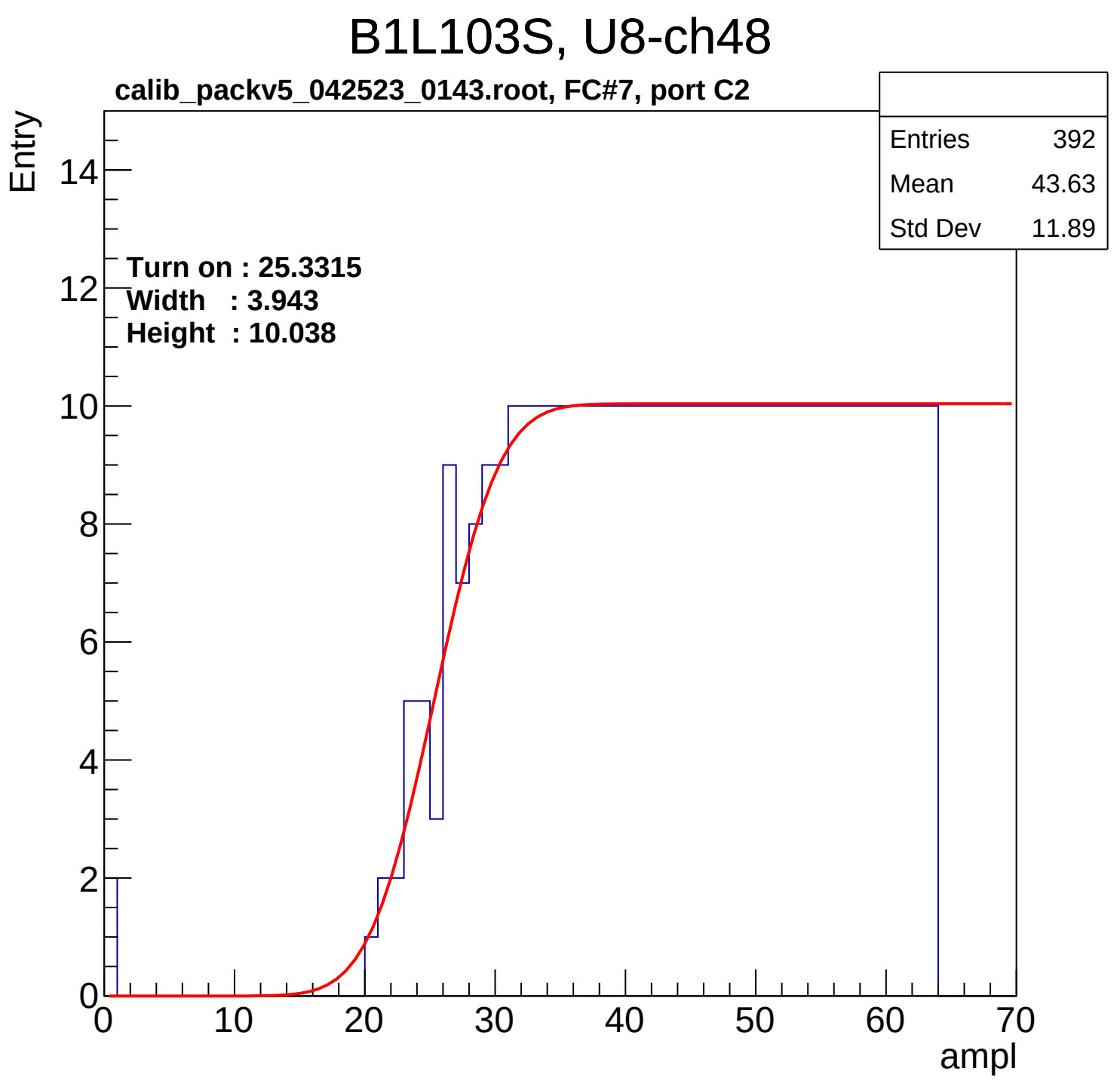
B1L103S, U8-ch48
calib_packv5_042523_0143.root, FC#7, port C2
Entries 392
Mean 43.63
Std Dev 11.89
Turn on : 25.3315
Width : 3.943
Height : 10.038
Entry
ampl
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8
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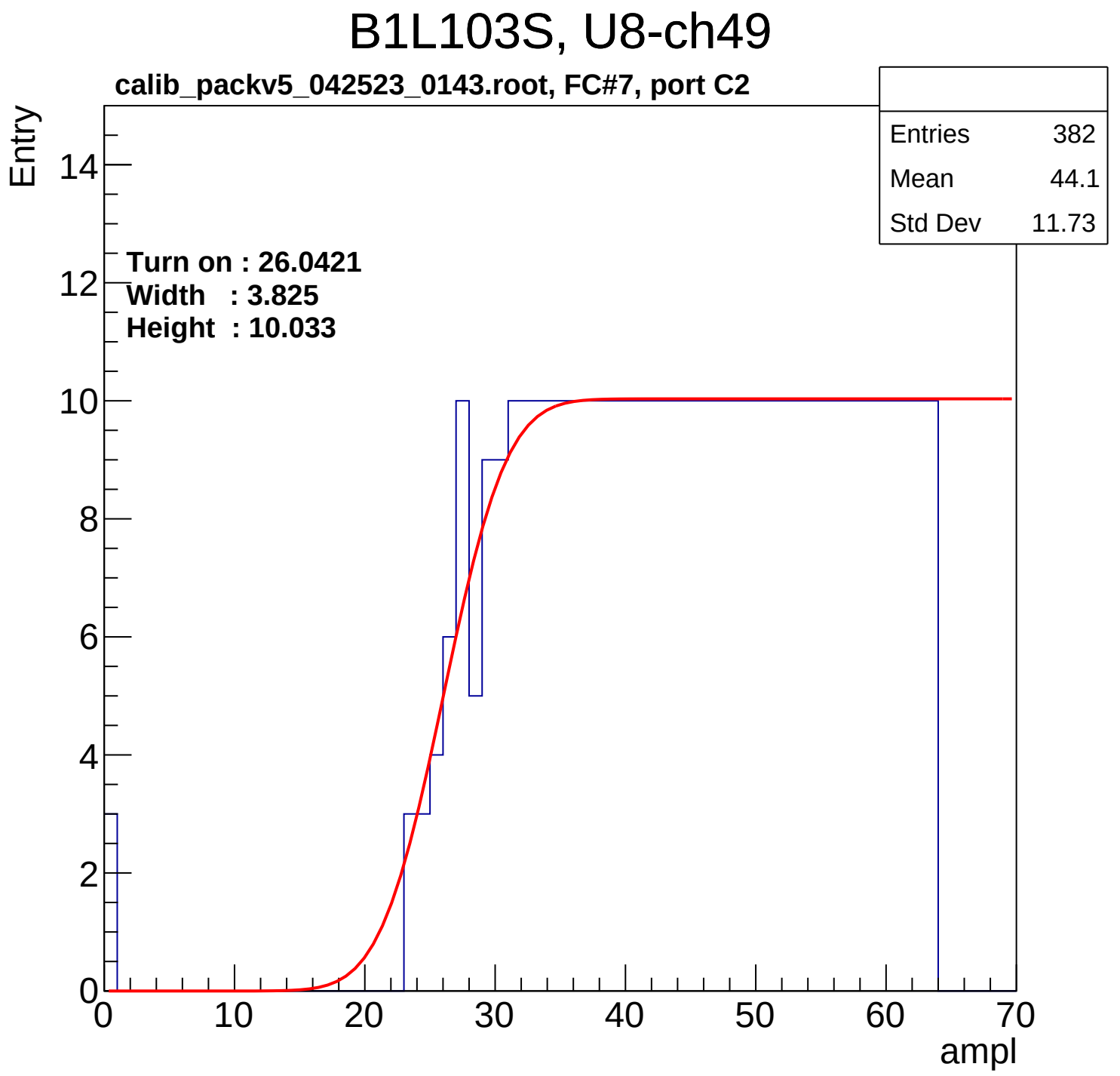
B1L103S, U8-ch49
calib_packv5_042523_0143.root, FC#7, port C2
Entries 382
Mean 44.1
Std Dev 11.73
Turn on : 26.0421
Width : 3.825
Height : 10.033
Entry
ampl
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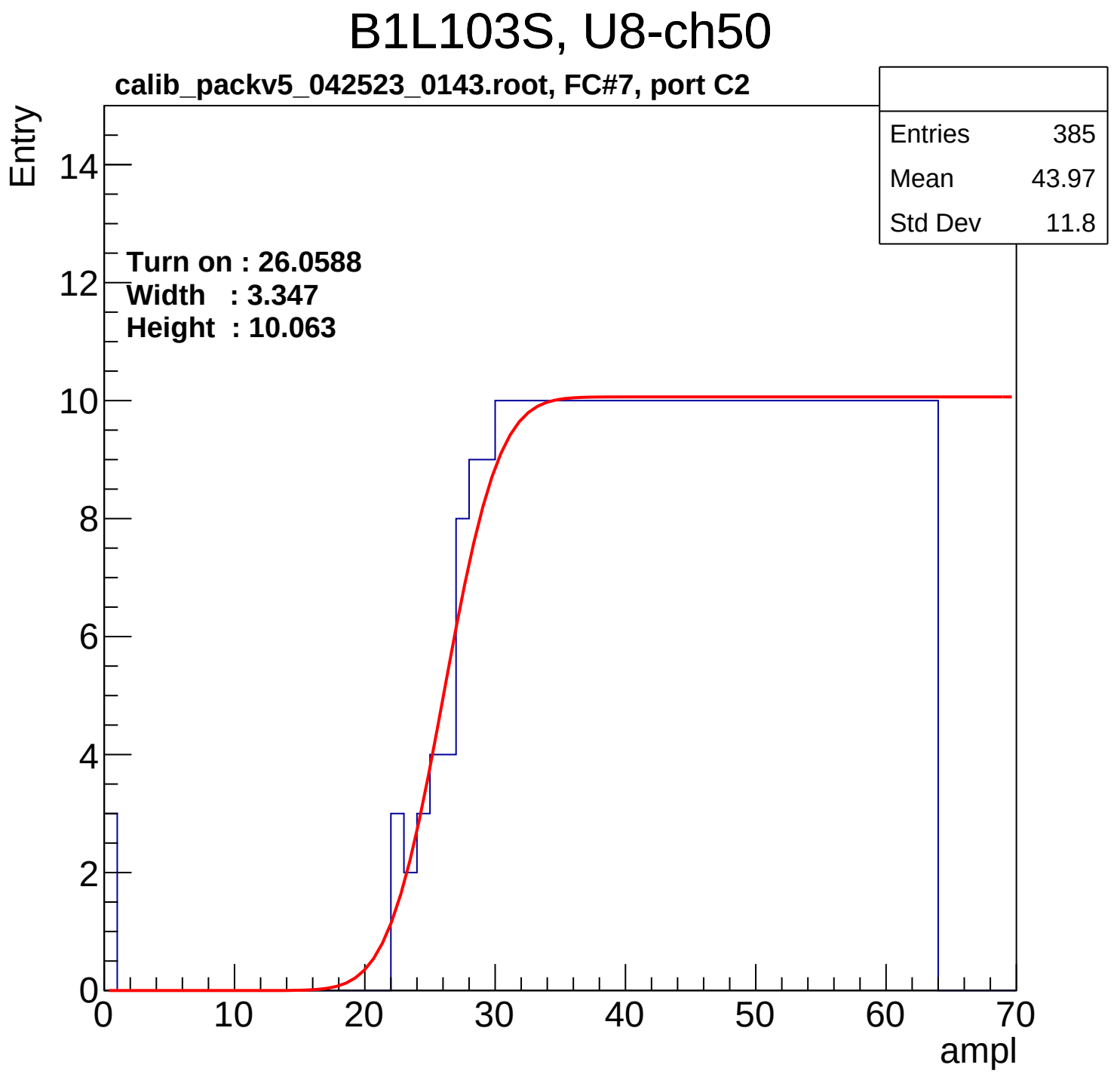
B1L103S, U8-ch50
calib_packv5_042523_0143.root, FC#7, port C2
Entries 385
Mean 43.97
Std Dev 11.8
Turn on : 26.0588
Width : 3.347
Height : 10.063
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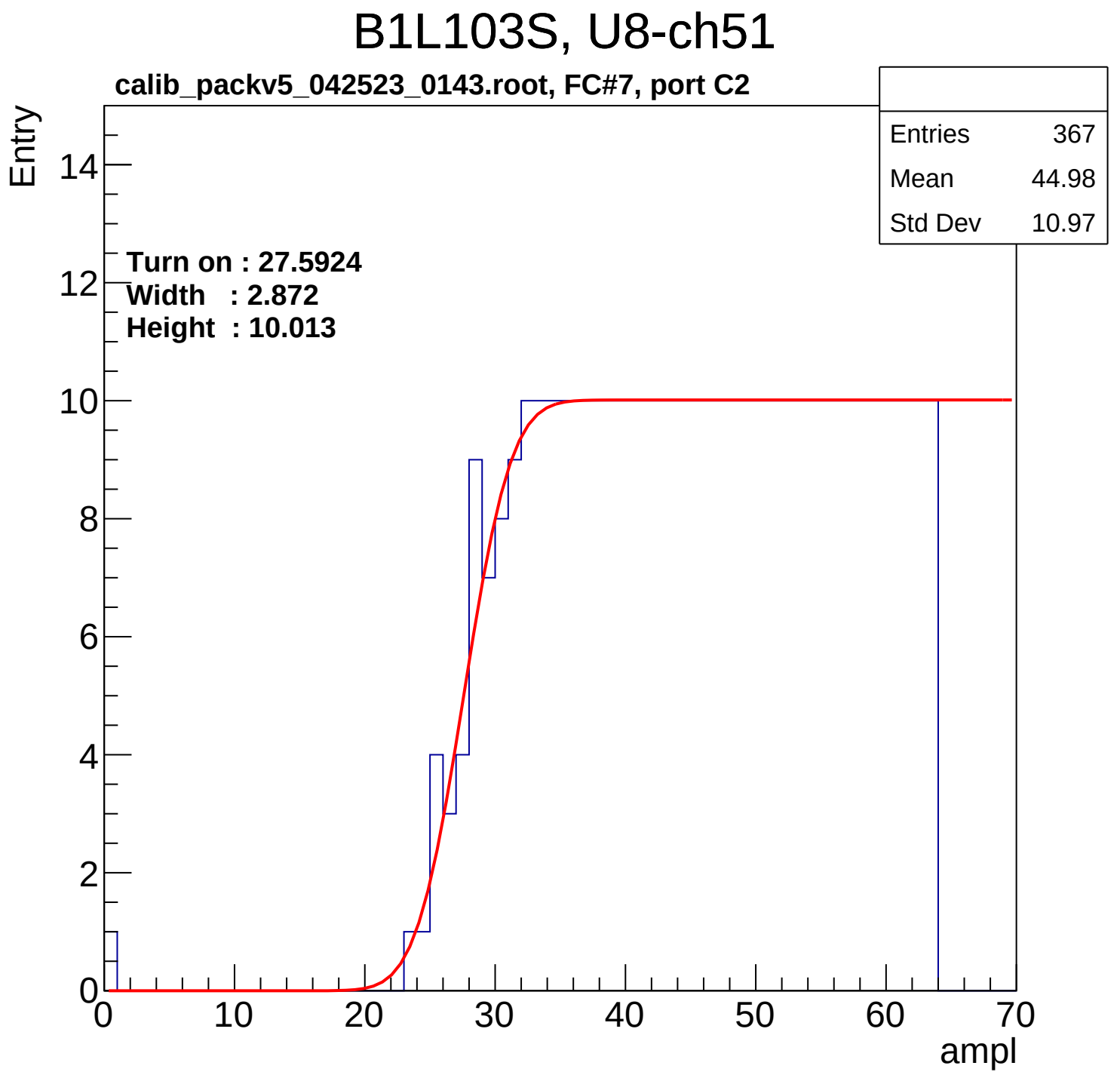
B1L103S, U8-ch51
calib_packv5_042523_0143.root, FC#7, port C2
Entries 367
Mean 44.98
Std Dev 10.97
Turn on : 27.5924
Width : 2.872
Height : 10.013
Entry
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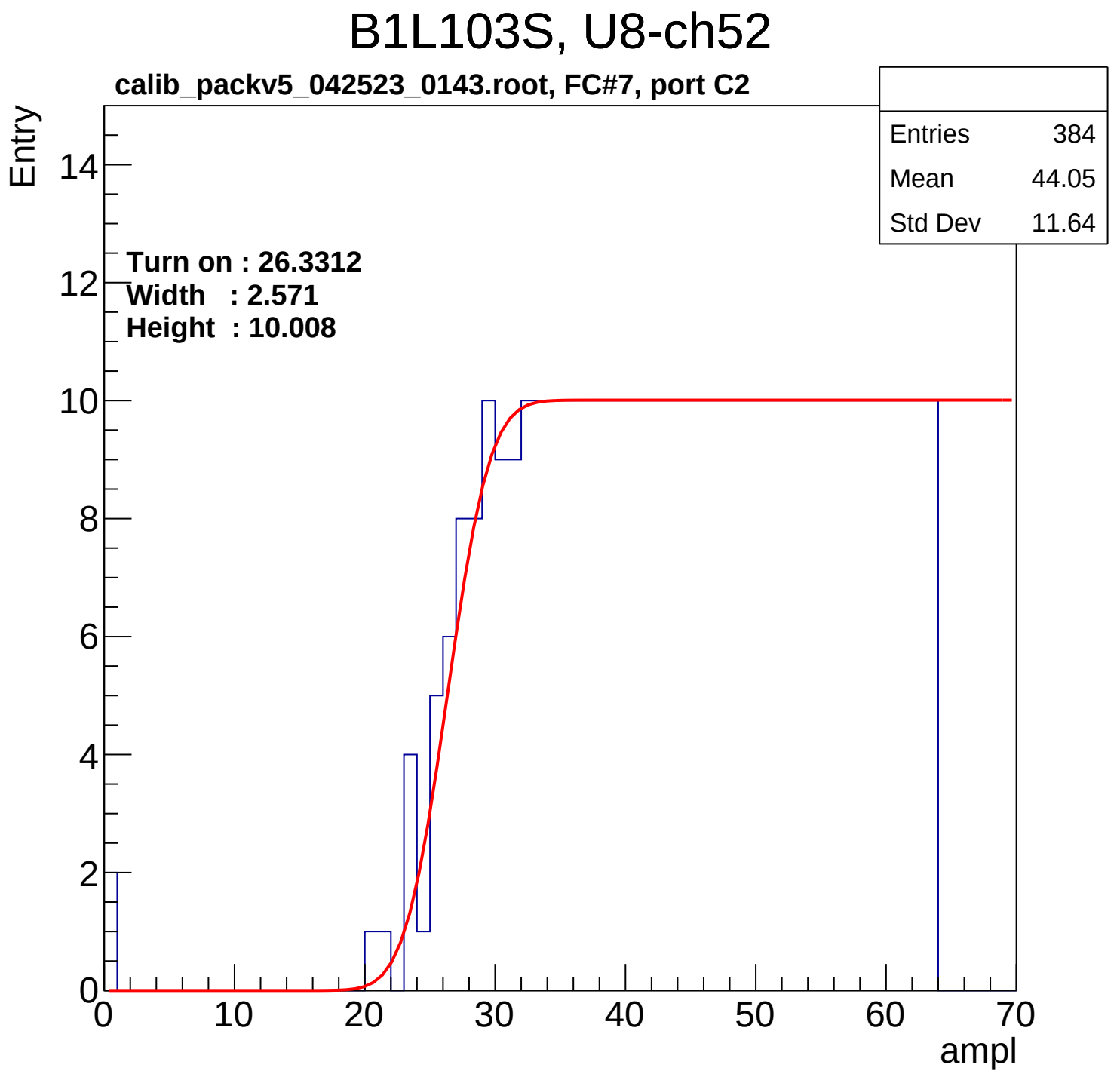
B1L103S, U8-ch52
calib_packv5_042523_0143.root, FC#7, port C2
Entries 384
Mean 44.05
Std Dev 11.64
Turn on : 26.3312
Width : 2.571
Height : 10.008
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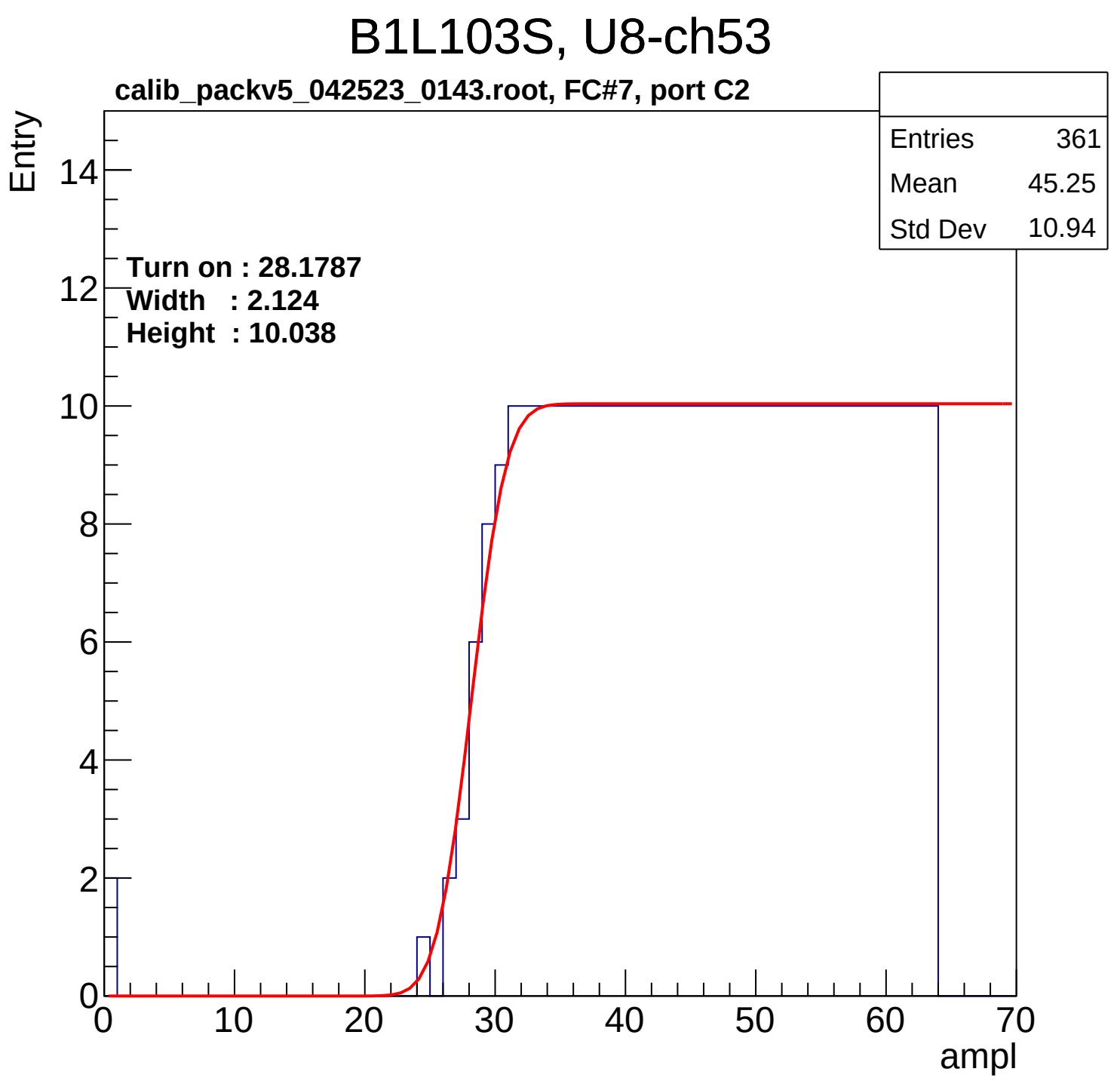
B1L103S, U8-ch53
calib_packv5_042523_0143.root, FC#7, port C2
Entries 361
Mean 45.25
Std Dev 10.94
Turn on : 28.1787
Width : 2.124
Height : 10.038
Entry
ampl
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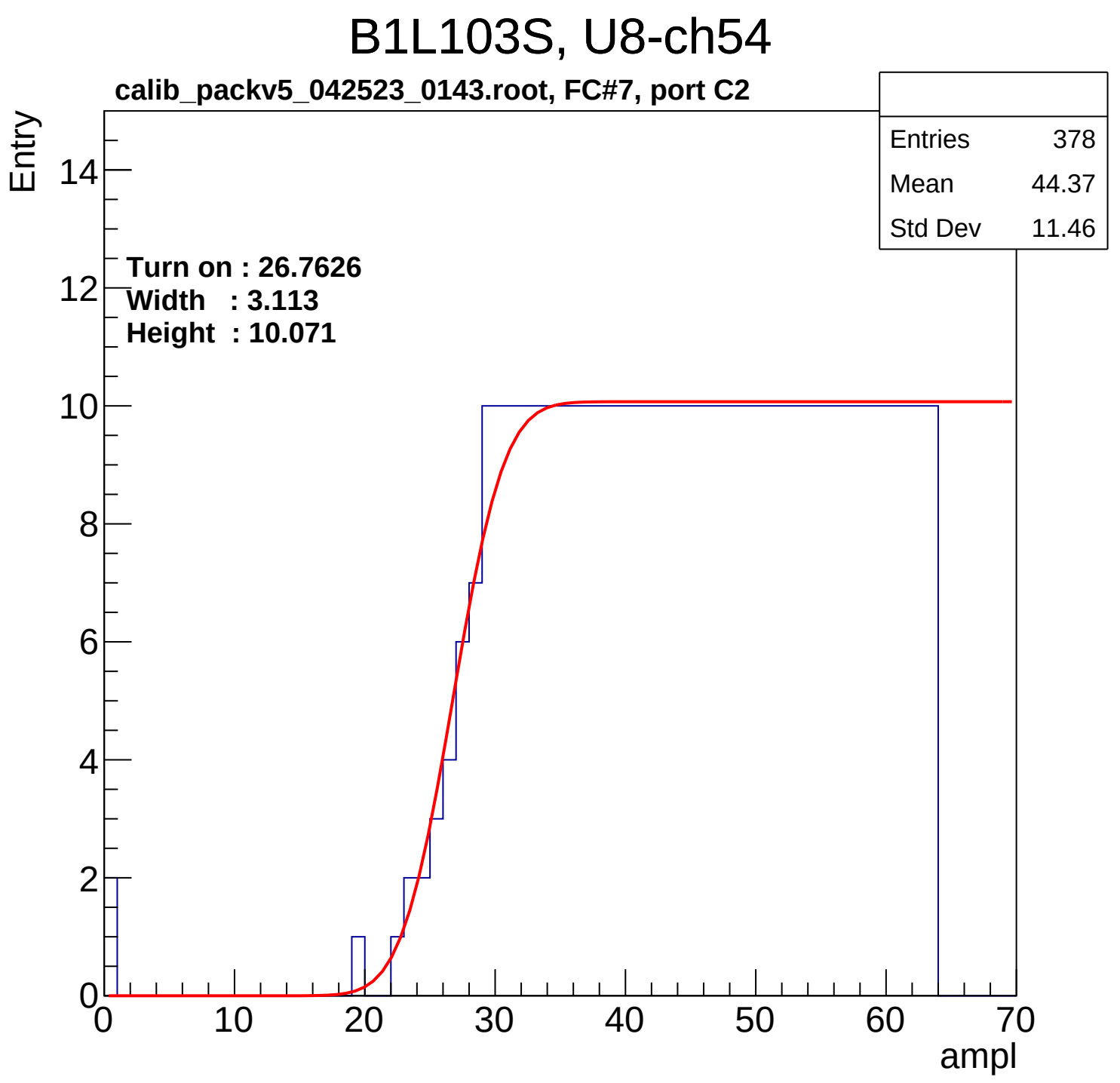
B1L103S, U8-ch54
calib_packv5_042523_0143.root, FC#7, port C2
Entries 378
Mean 44.37
Std Dev 11.46
Turn on : 26.7626
Width : 3.113
Height : 10.071
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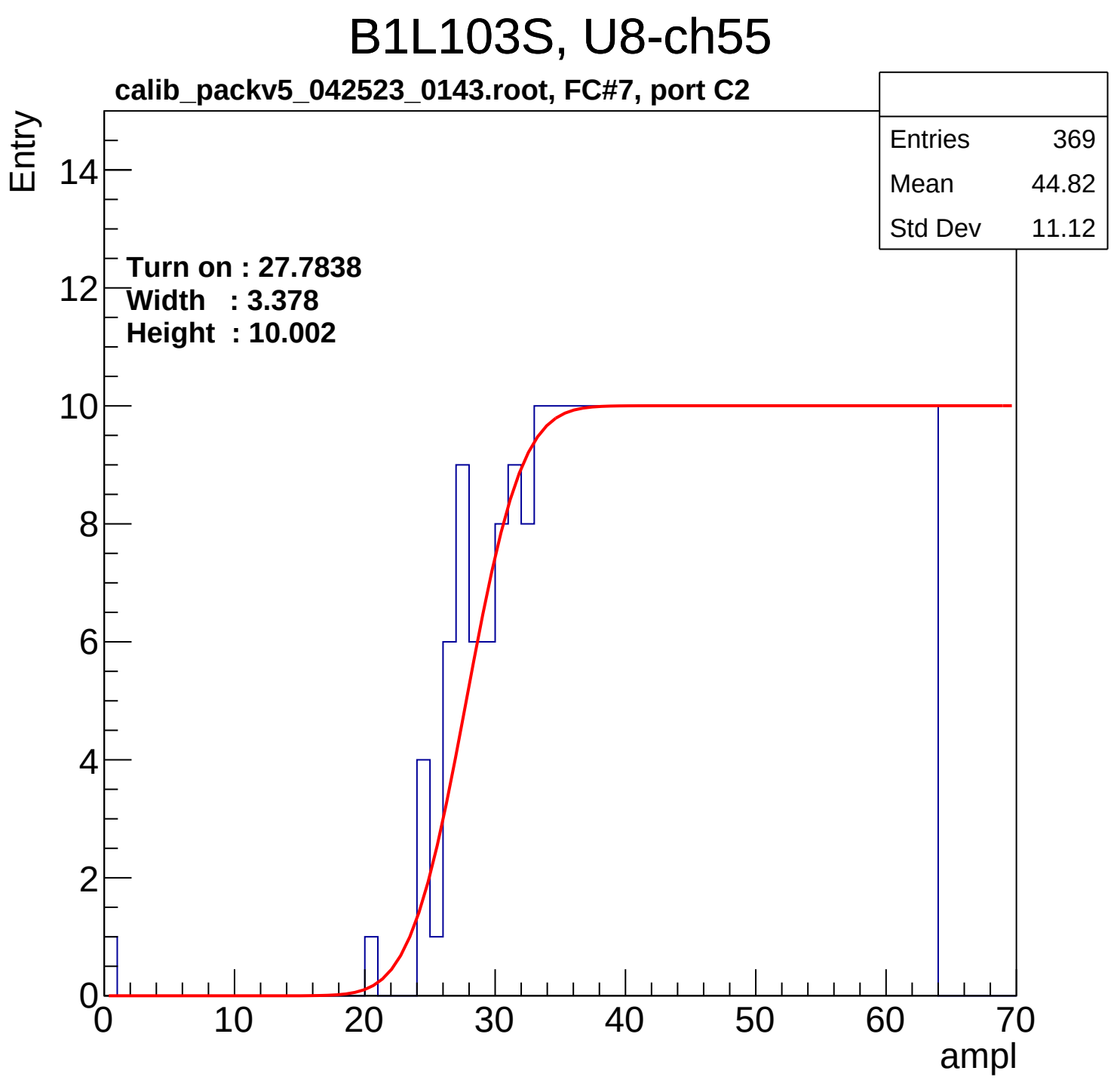
B1L103S, U8-ch55
calib_packv5_042523_0143.root, FC#7, port C2
Entries 369
Mean 44.82
Std Dev 11.12
Turn on : 27.7838
Width : 3.378
Height : 10.002
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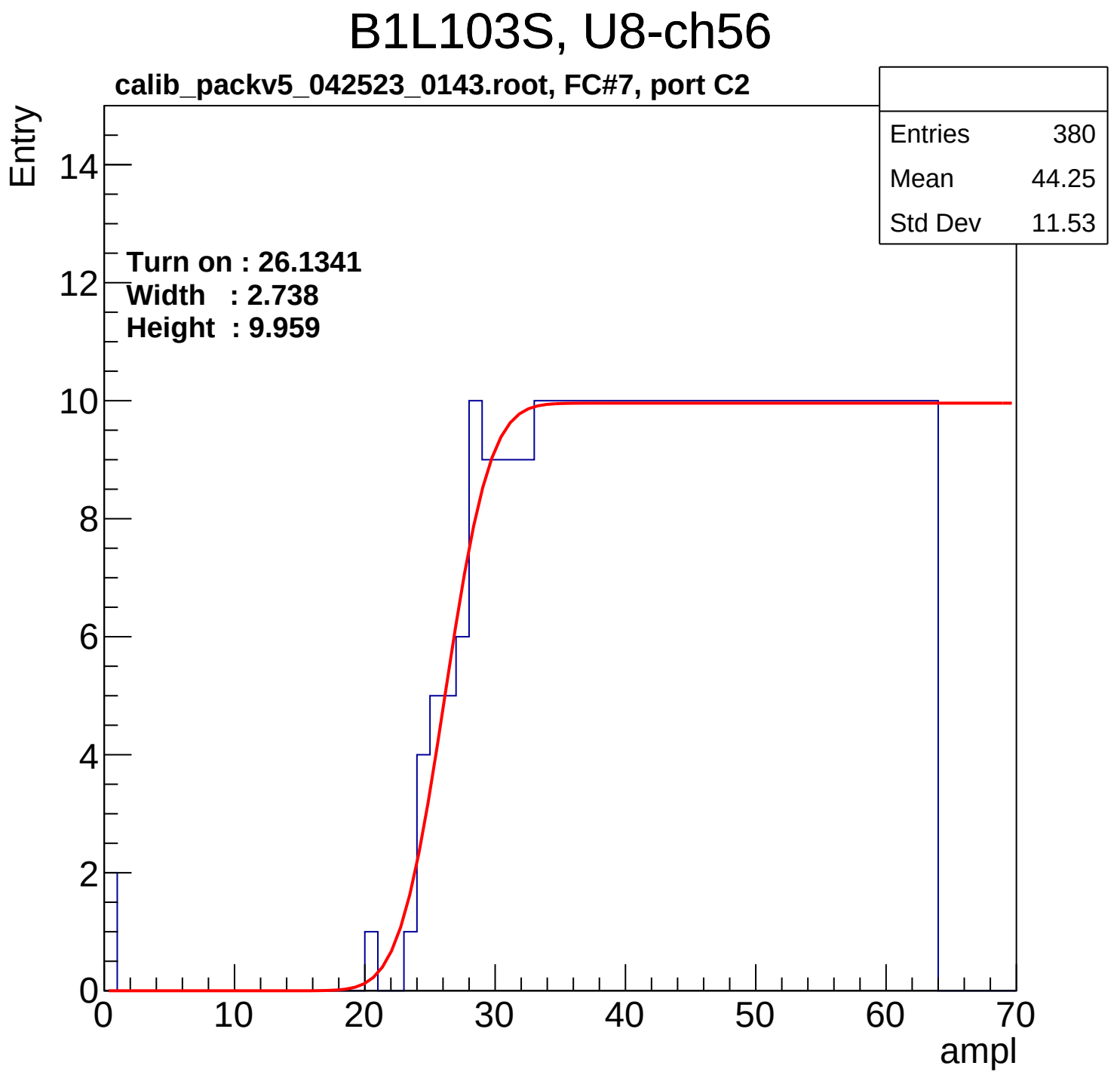
B1L103S, U8-ch56
calib_packv5_042523_0143.root, FC#7, port C2
Entries 380
Mean 44.25
Std Dev 11.53
Turn on : 26.1341
Width : 2.738
Height : 9.959
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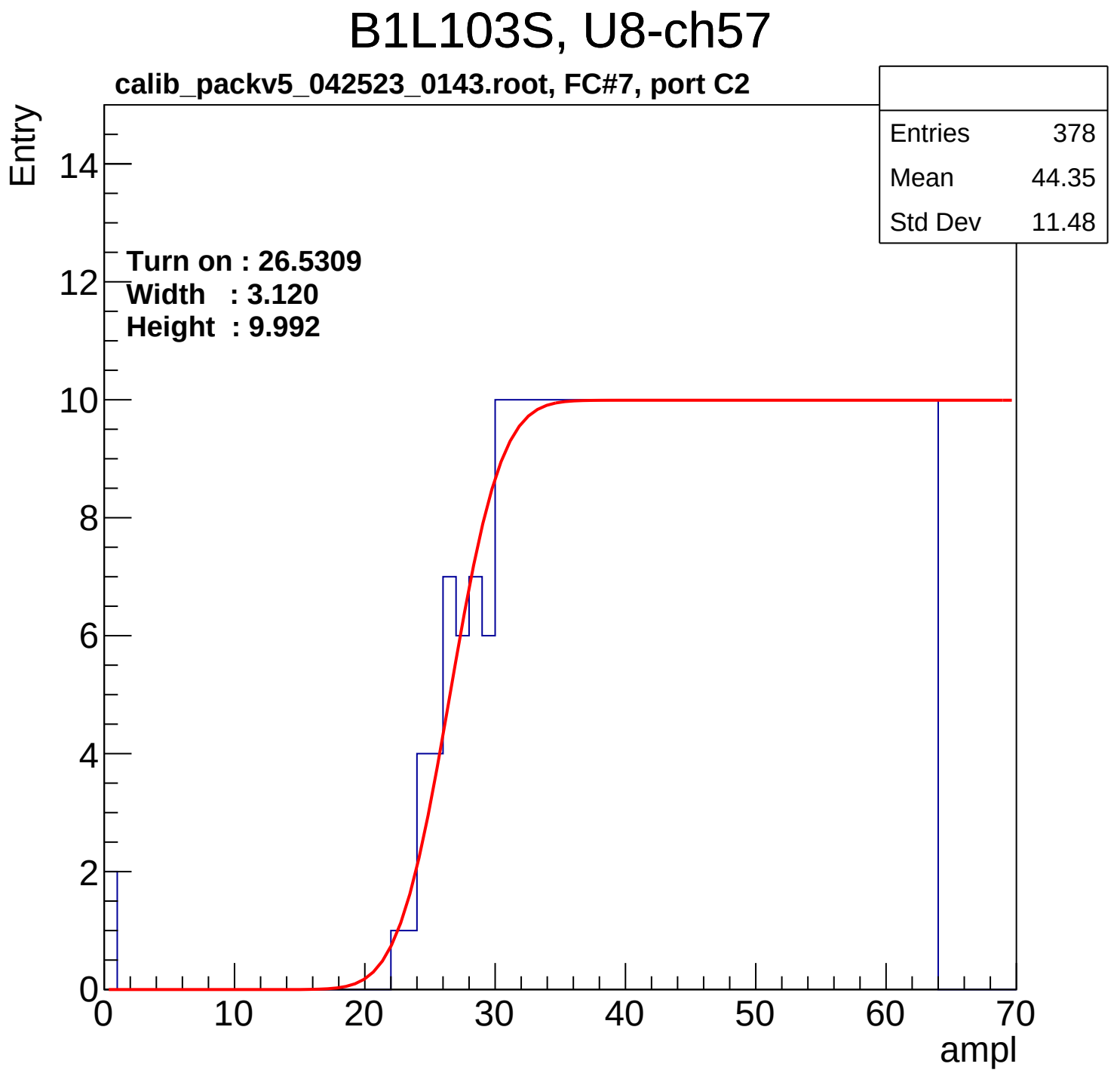
B1L103S, U8-ch57
calib_packv5_042523_0143.root, FC#7, port C2
Entries 378
Mean 44.35
Std Dev 11.48
Turn on : 26.5309
Width : 3.120
Height : 9.992
Entry
ampl
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4
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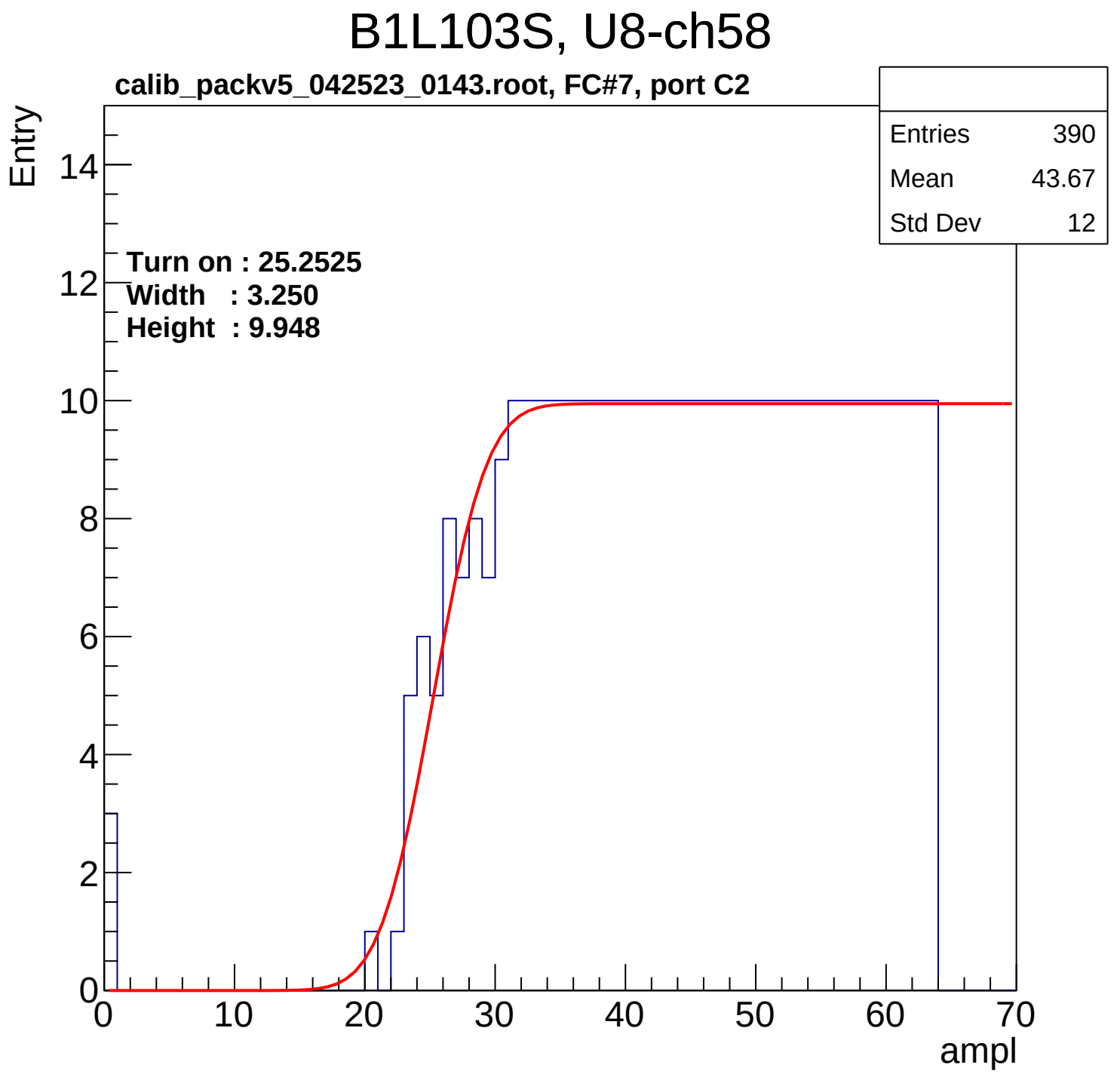
B1L103S, U8-ch58
calib_packv5_042523_0143.root, FC#7, port C2
Entries 390
Mean 43.67
Std Dev 12
Turn on : 25.2525
Width : 3.250
Height : 9.948
Entry
ampl
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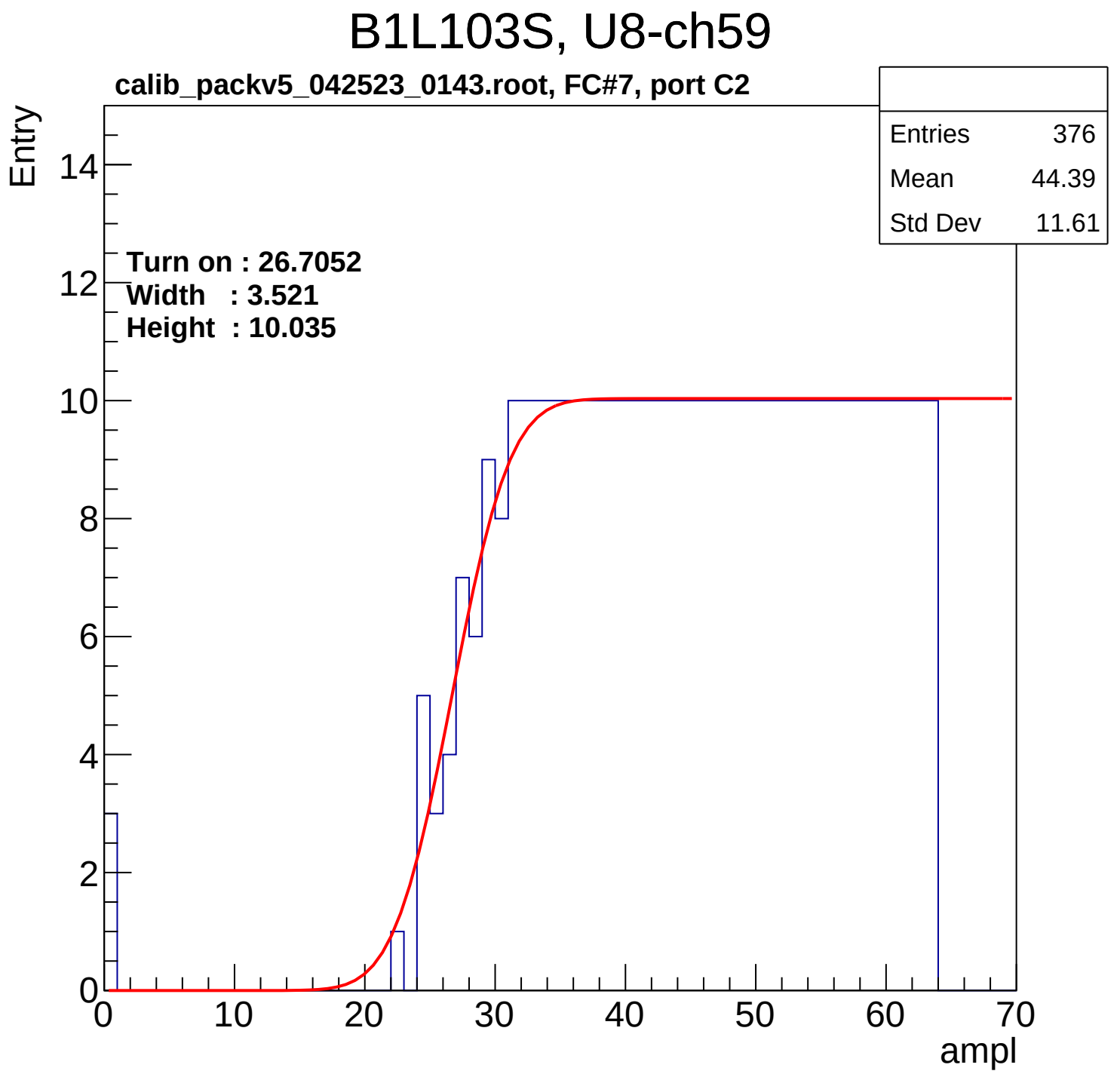
B1L103S, U8-ch59
calib_packv5_042523_0143.root, FC#7, port C2
Entries 376
Mean 44.39
Std Dev 11.61
Turn on : 26.7052
Width : 3.521
Height : 10.035
Entry
ampl
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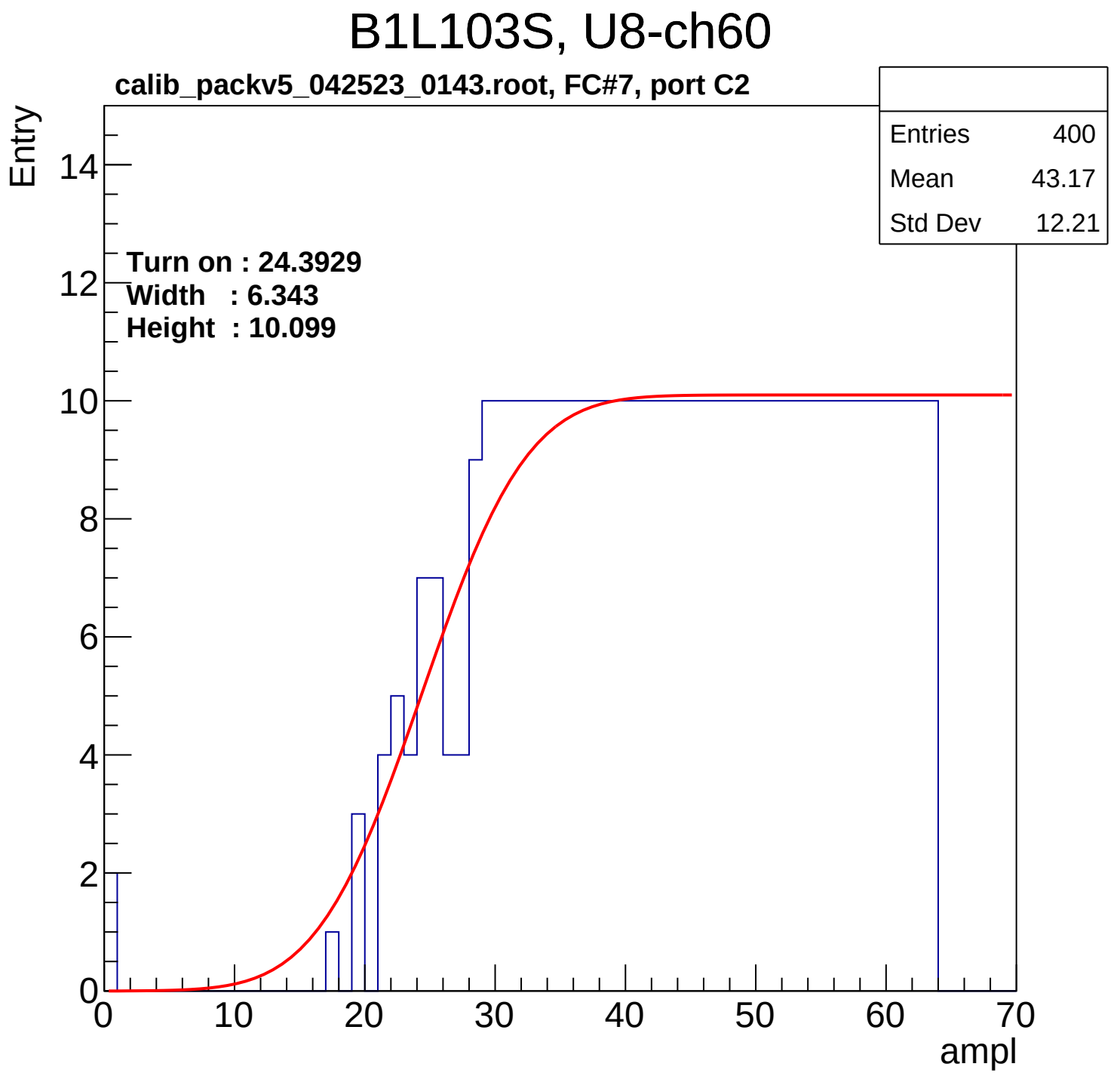
B1L103S, U8-ch60
calib_packv5_042523_0143.root, FC#7, port C2
Entries 400
Mean 43.17
Std Dev 12.21
Turn on : 24.3929
Width : 6.343
Height : 10.099
Entry
ampl
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2
4
6
8
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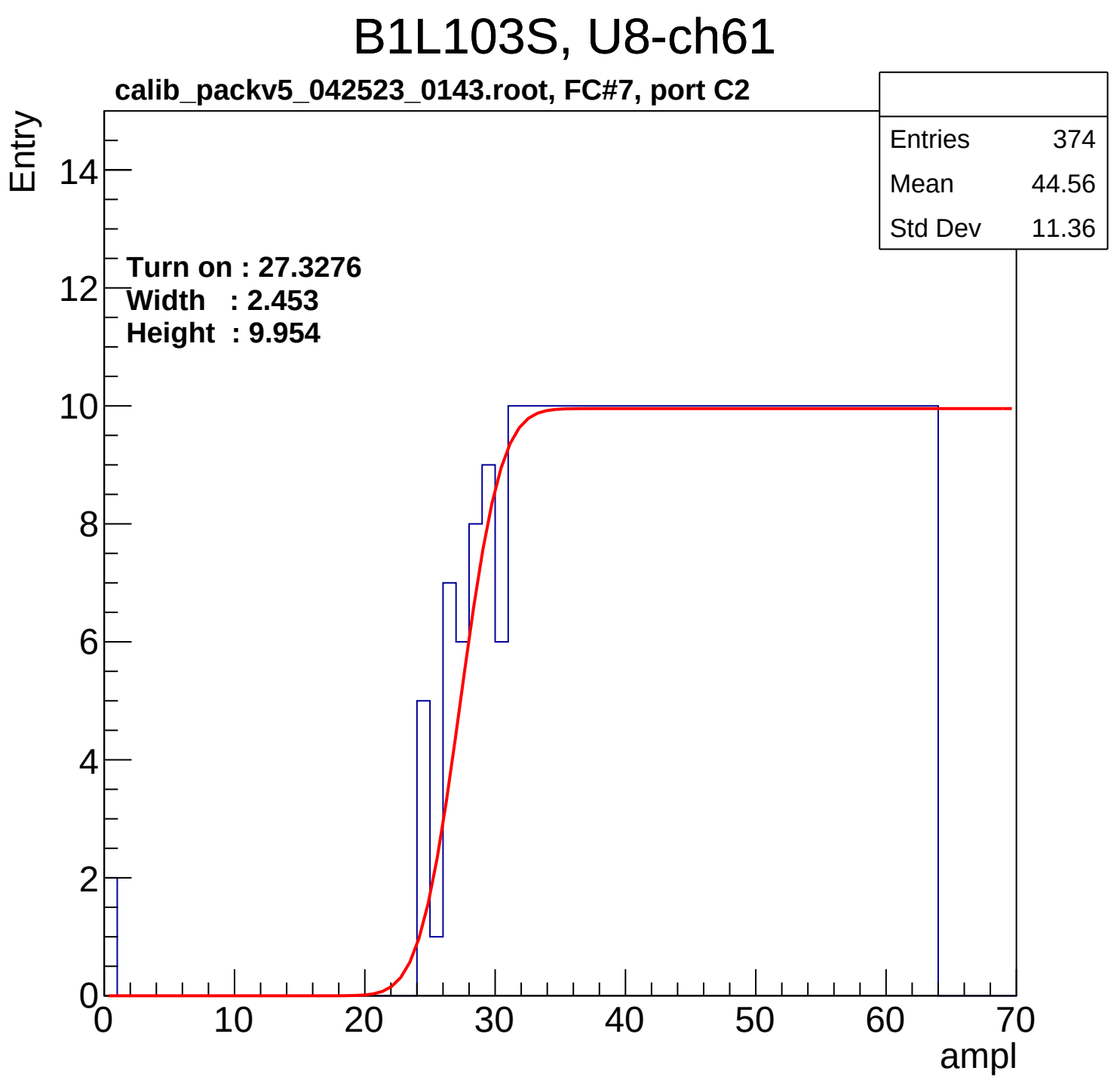
B1L103S, U8-ch61
calib_packv5_042523_0143.root, FC#7, port C2
Entries 374
Mean 44.56
Std Dev 11.36
Turn on : 27.3276
Width : 2.453
Height : 9.954
Entry
ampl
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8
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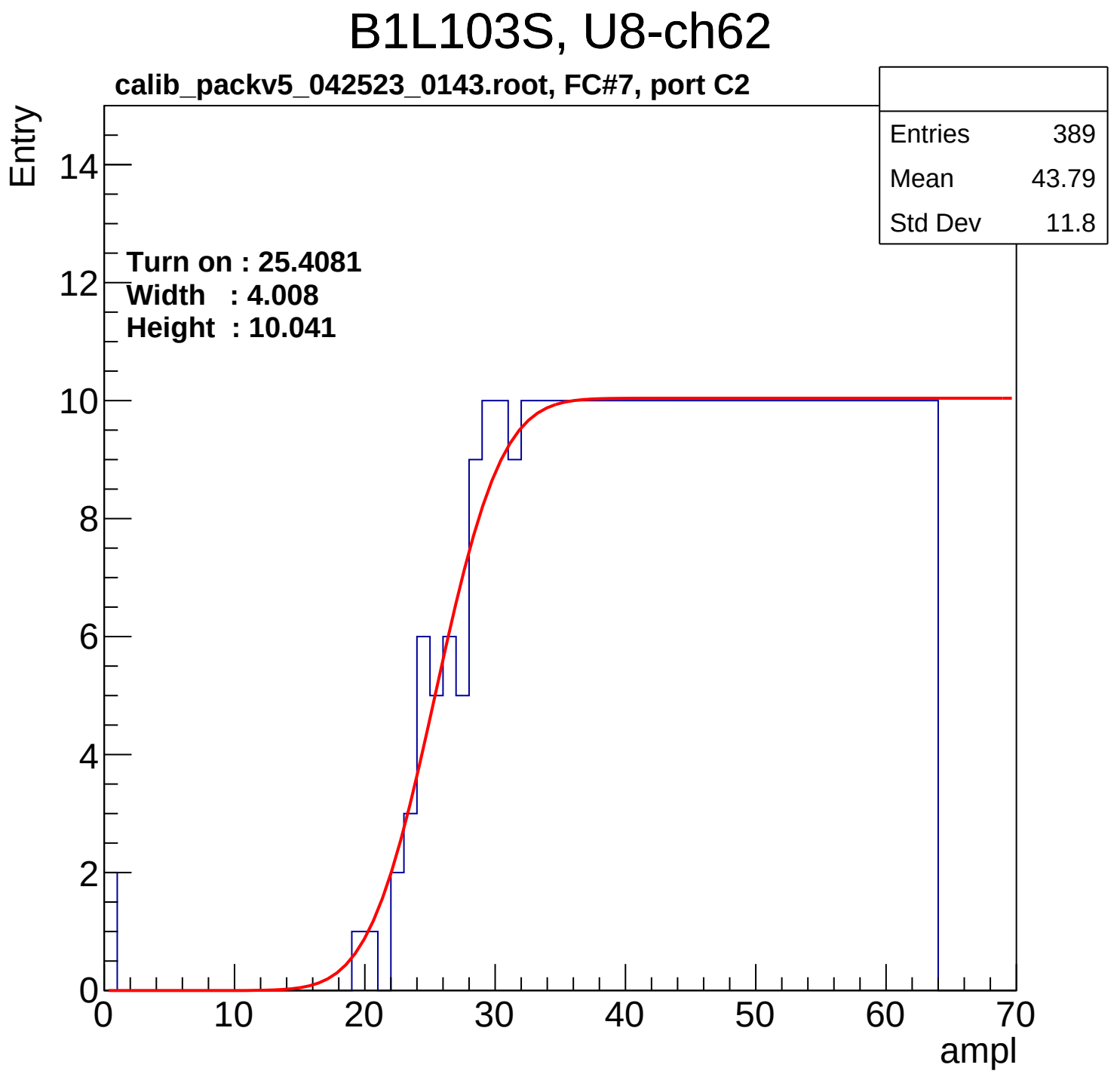
B1L103S, U8-ch62
calib_packv5_042523_0143.root, FC#7, port C2
Entries 389
Mean 43.79
Std Dev 11.8
Turn on : 25.4081
Width : 4.008
Height : 10.041
Entry
ampl
0
2
4
6
8
10
12
14
0
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60
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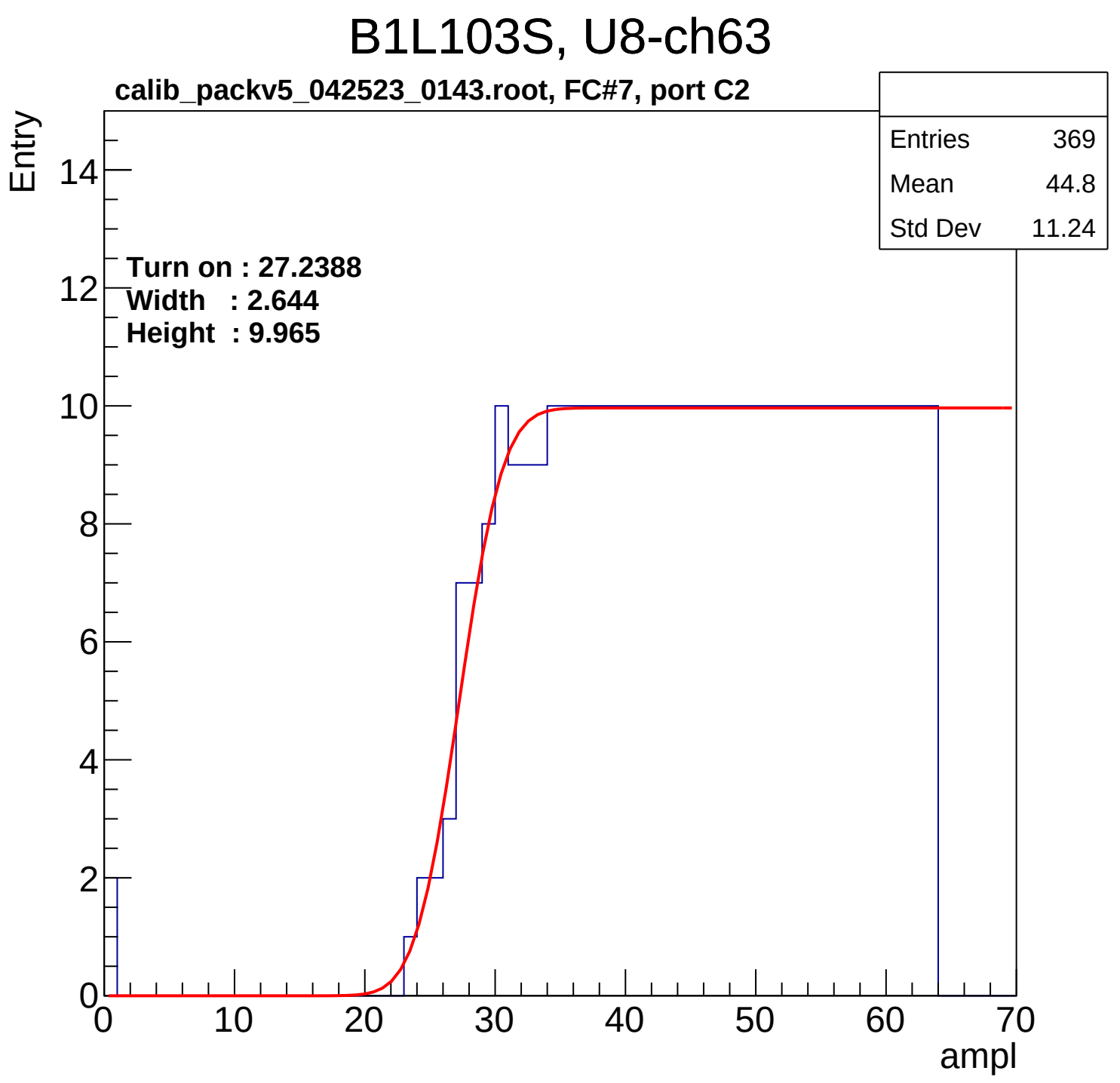
B1L103S, U8-ch63
calib_packv5_042523_0143.root, FC#7, port C2
Entries 369
Mean 44.8
Std Dev 11.24
Turn on : 27.2388
Width : 2.644
Height : 9.965
Entry
ampl
0
2
4
6
8
10
12
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0
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20
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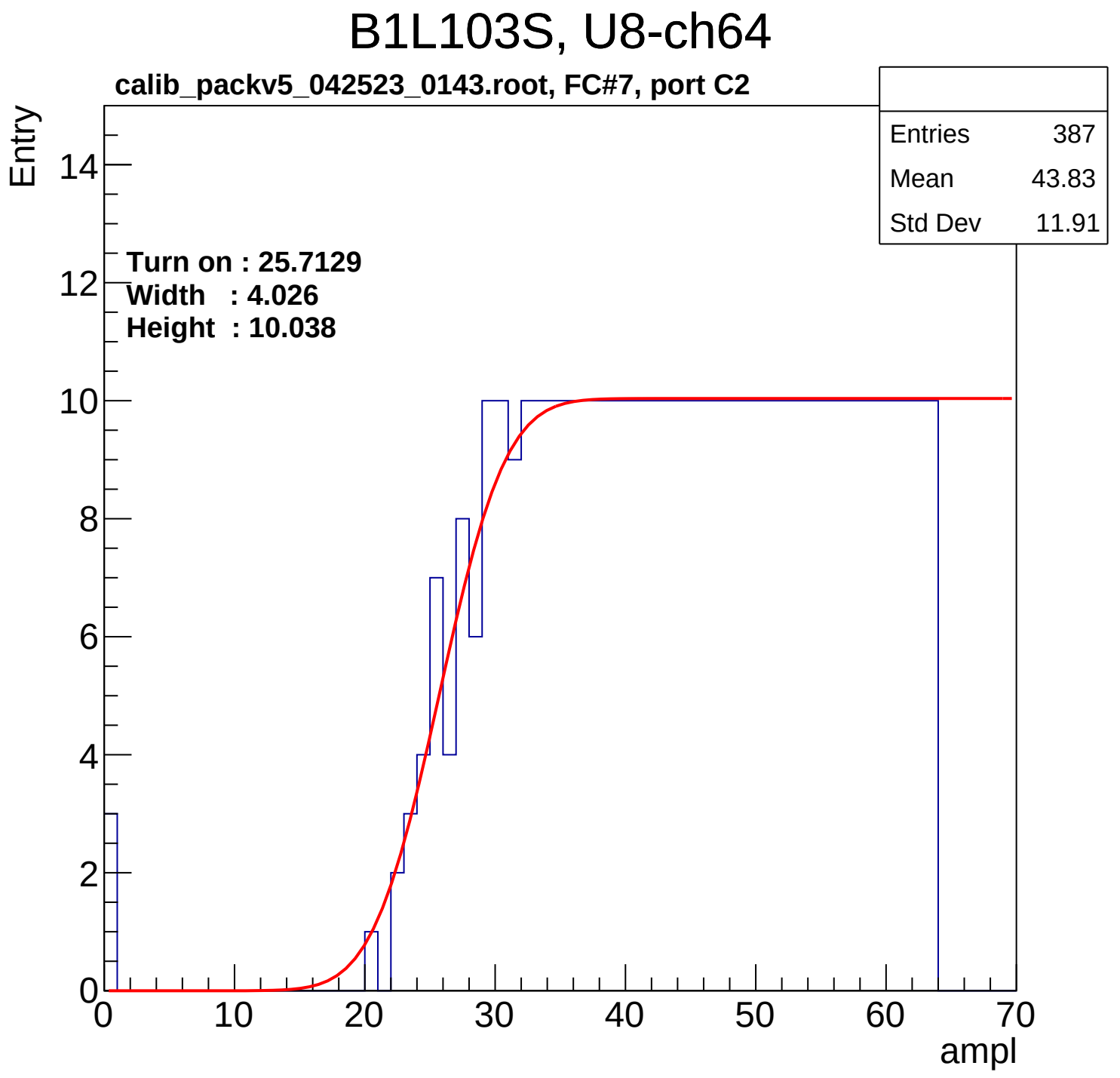
B1L103S, U8-ch64
calib_packv5_042523_0143.root, FC#7, port C2
Entries 387
Mean 43.83
Std Dev 11.91
Turn on : 25.7129
Width : 4.026
Height : 10.038
Entry
ampl
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4
6
8
10
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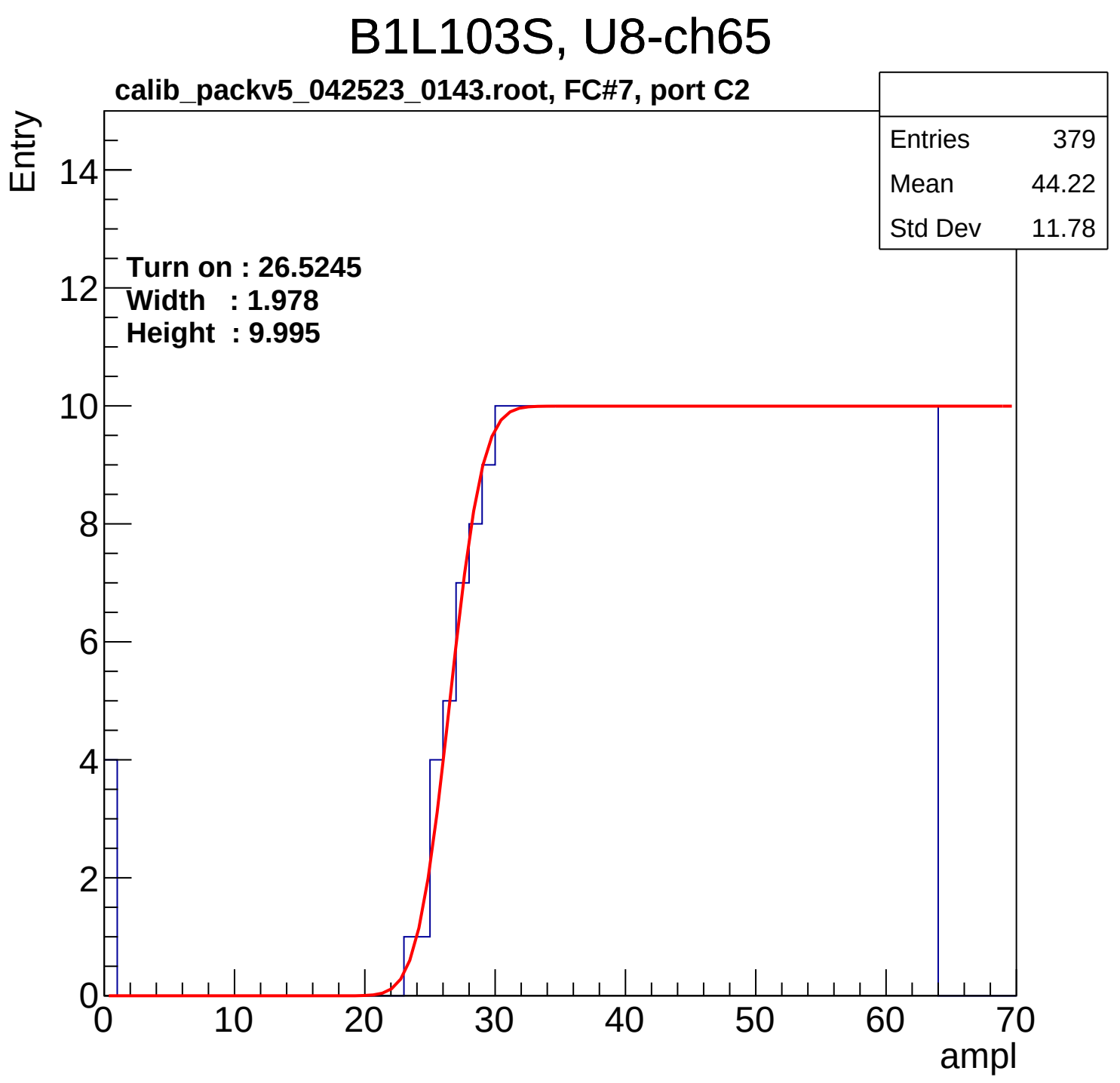
B1L103S, U8-ch65
calib_packv5_042523_0143.root, FC#7, port C2
Entries 379
Mean 44.22
Std Dev 11.78
Turn on : 26.5245
Width : 1.978
Height : 9.995
Entry
ampl
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2
4
6
8
10
12
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0
10
20
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40
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60
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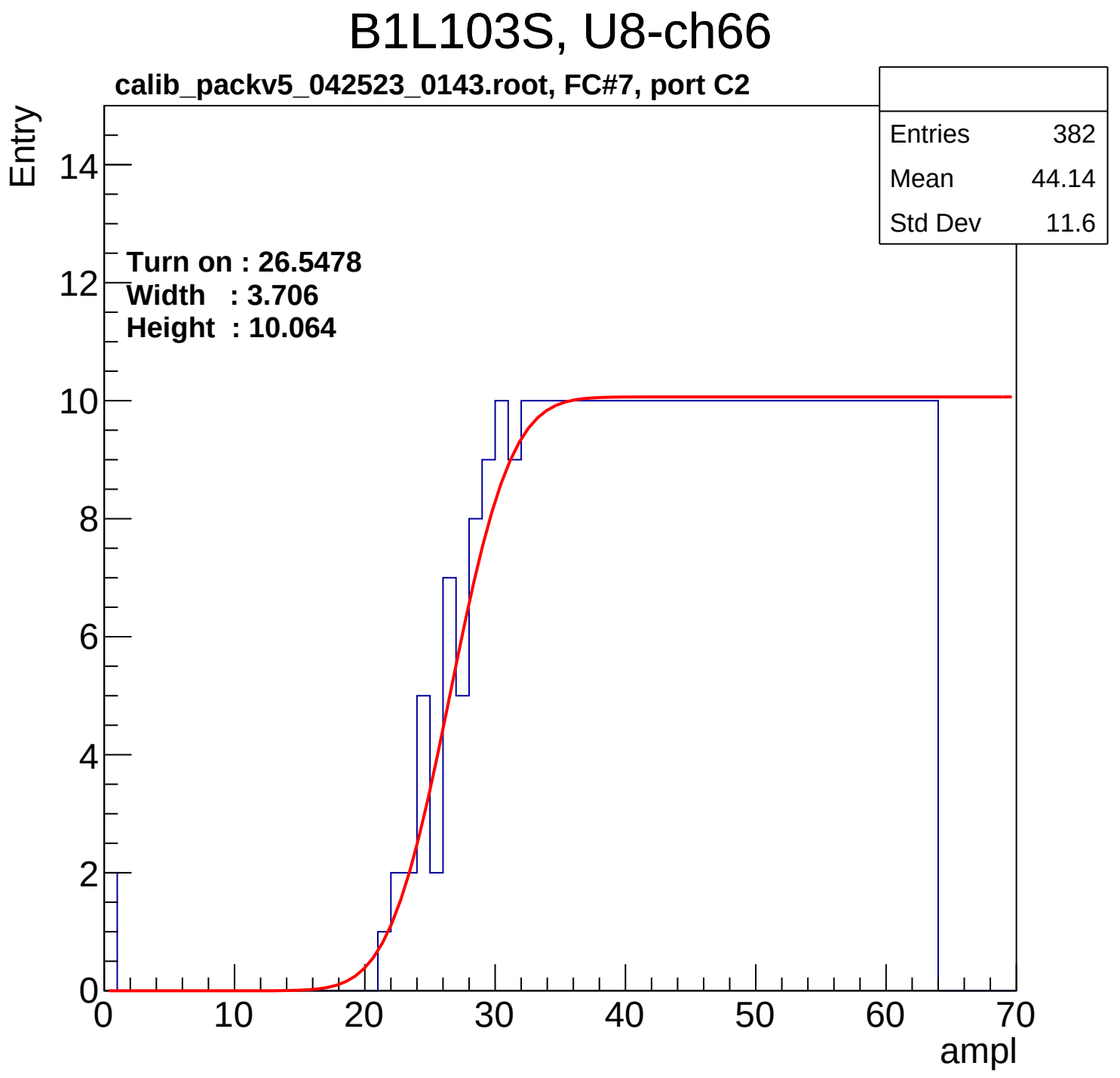
B1L103S, U8-ch66
calib_packv5_042523_0143.root, FC#7, port C2
Entries 382
Mean 44.14
Std Dev 11.6
Turn on : 26.5478
Width : 3.706
Height : 10.064
Entry
ampl
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6
8
10
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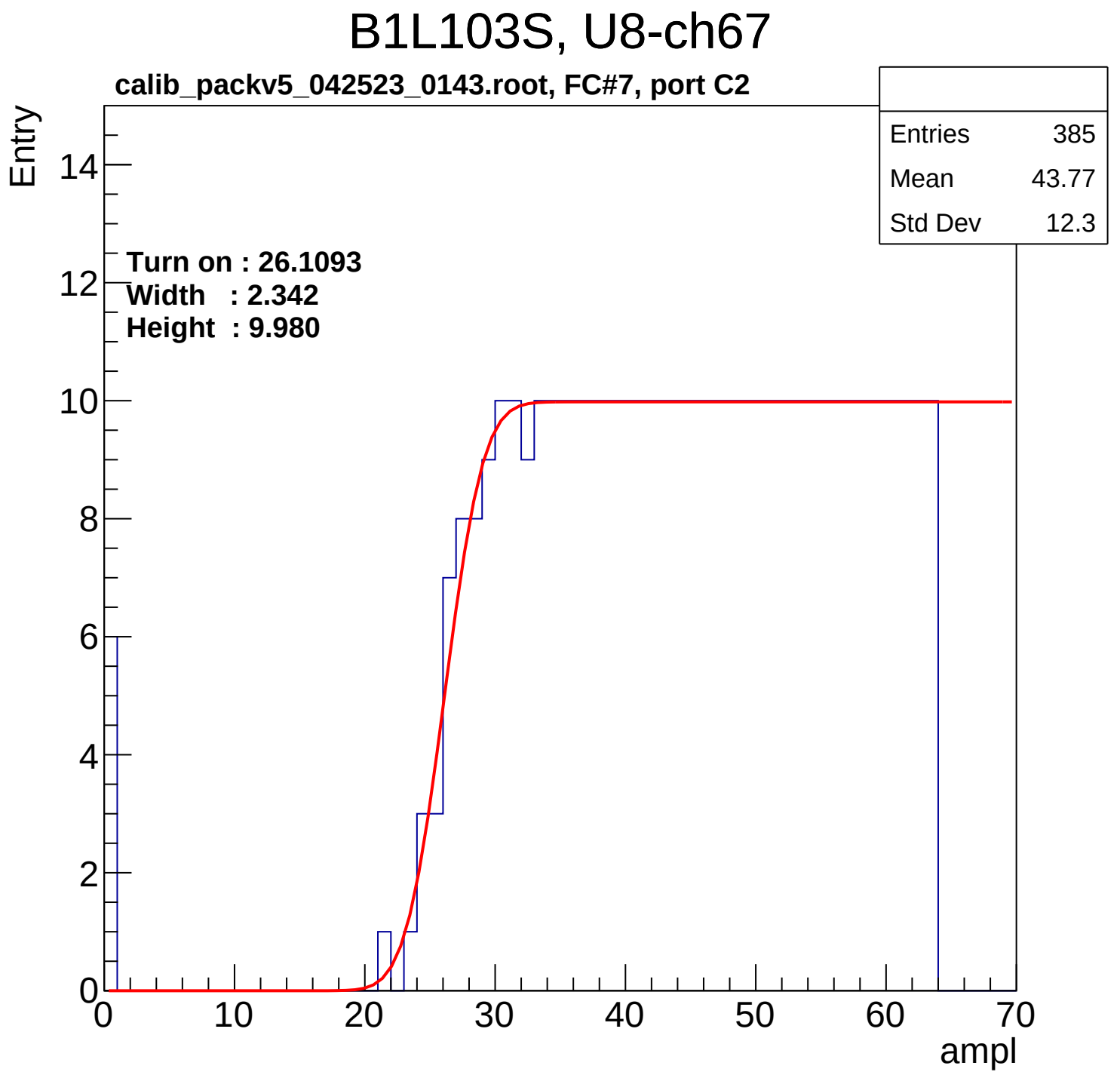
B1L103S, U8-ch67
calib_packv5_042523_0143.root, FC#7, port C2
Entries 385
Mean 43.77
Std Dev 12.3
Turn on : 26.1093
Width : 2.342
Height : 9.980
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
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60
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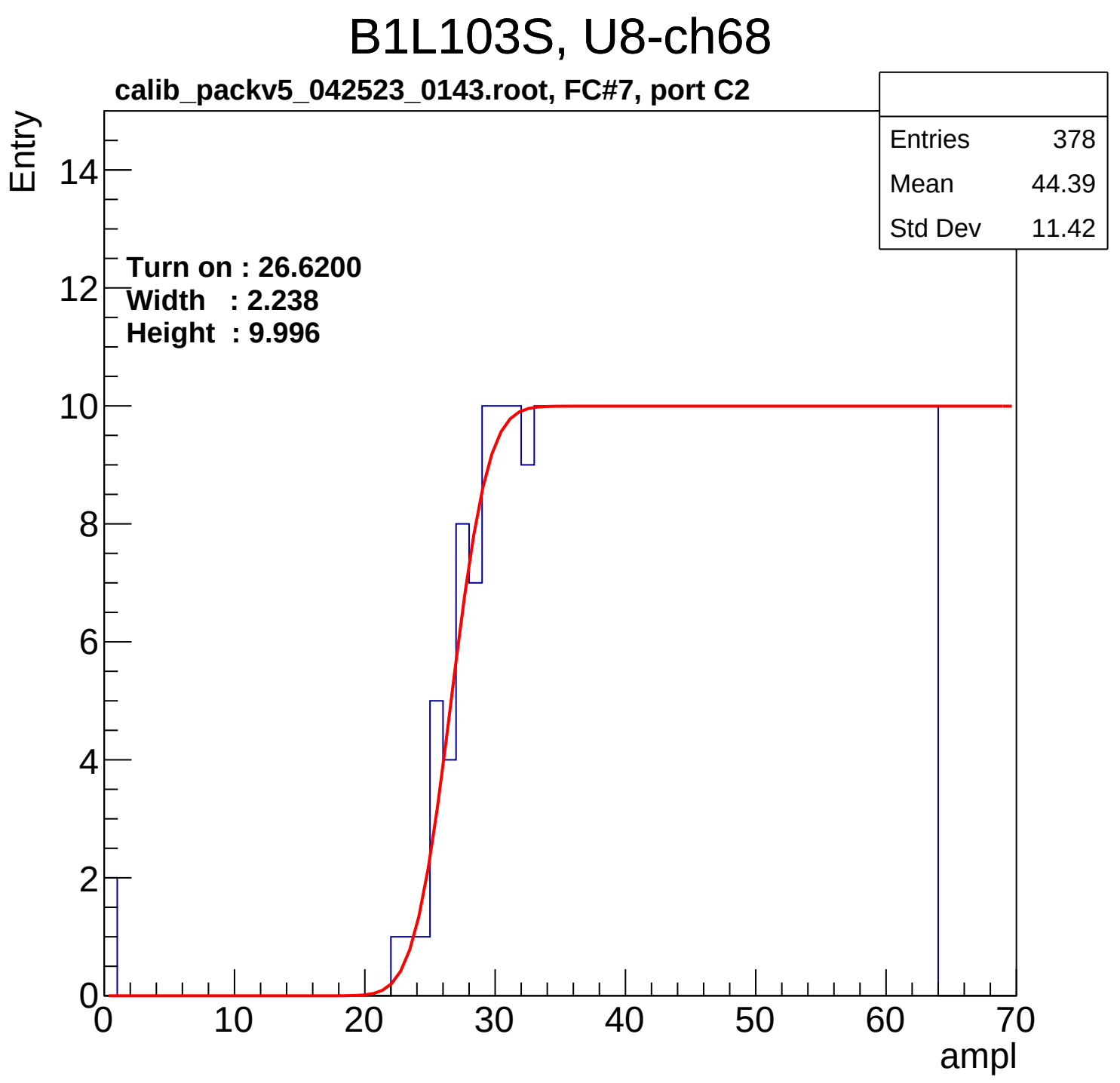
B1L103S, U8-ch68
calib_packv5_042523_0143.root, FC#7, port C2
Entries 378
Mean 44.39
Std Dev 11.42
Turn on : 26.6200
Width : 2.238
Height : 9.996
Entry
ampl
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2
4
6
8
10
12
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0
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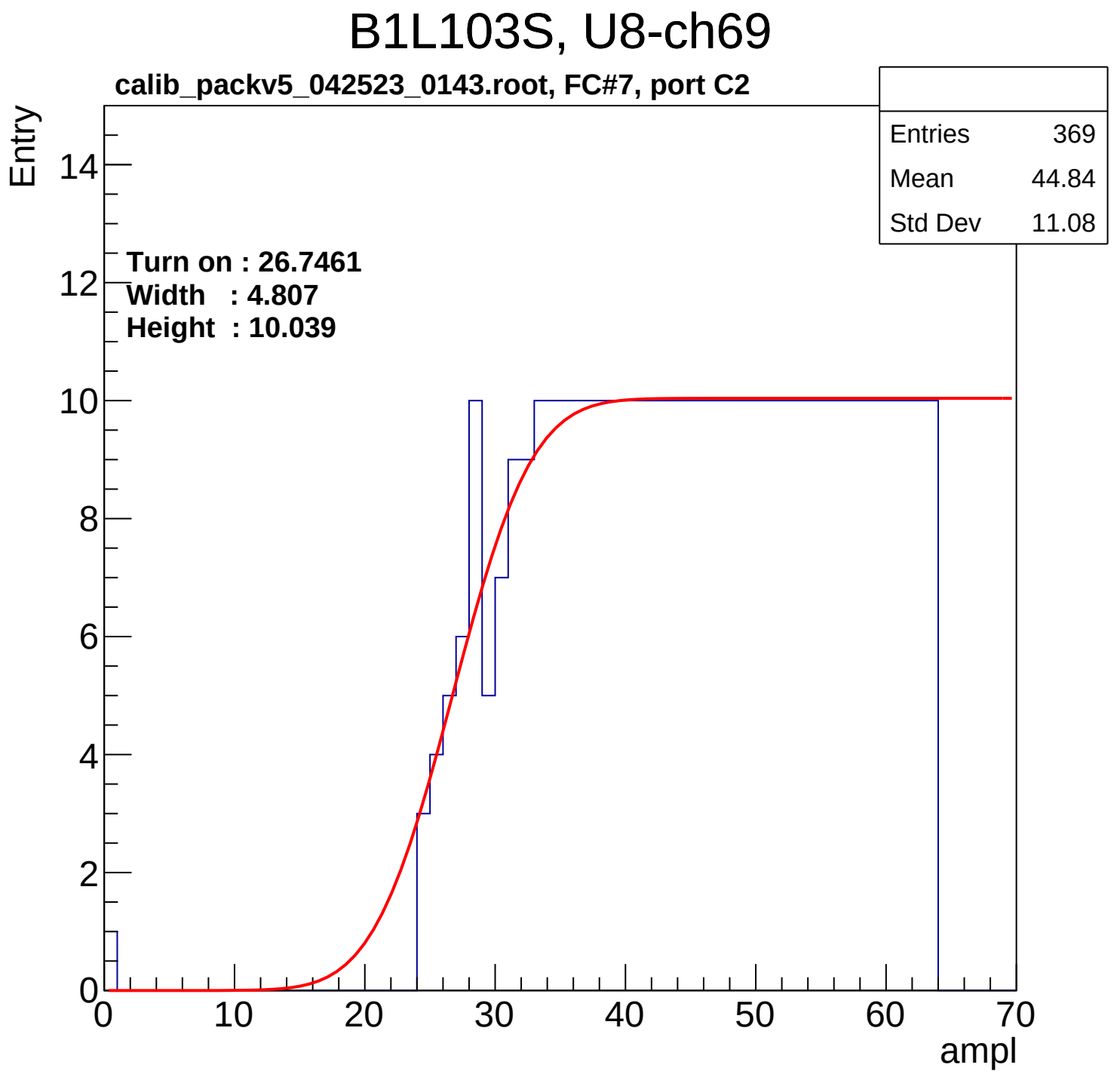
B1L103S, U8-ch69
calib_packv5_042523_0143.root, FC#7, port C2
Entries 369
Mean 44.84
Std Dev 11.08
Turn on : 26.7461
Width : 4.807
Height : 10.039
Entry
ampl
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4
6
8
10
12
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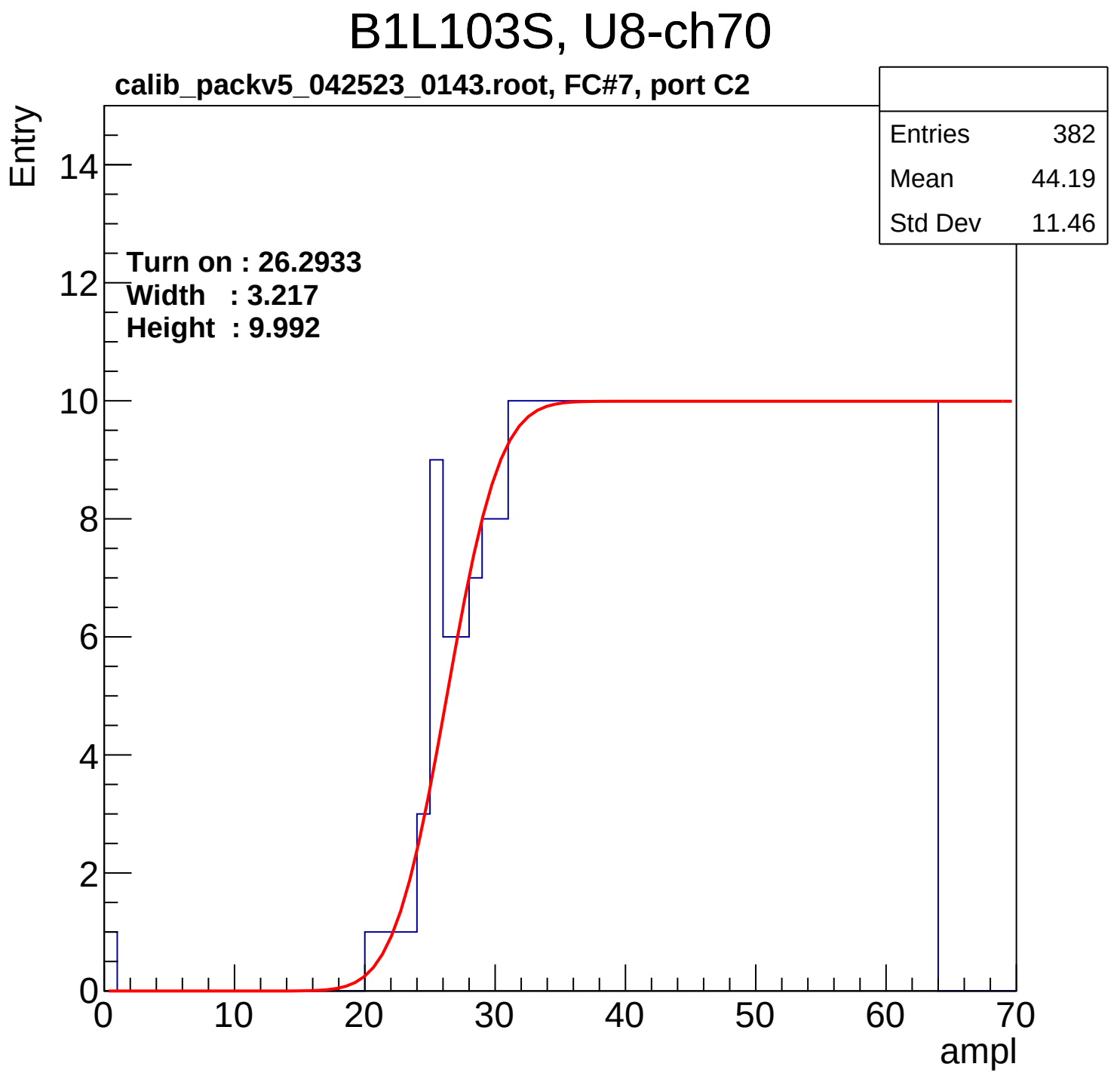
B1L103S, U8-ch70
calib_packv5_042523_0143.root, FC#7, port C2
Entries 382
Mean 44.19
Std Dev 11.46
Turn on : 26.2933
Width : 3.217
Height : 9.992
Entry
ampl
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2
4
6
8
10
12
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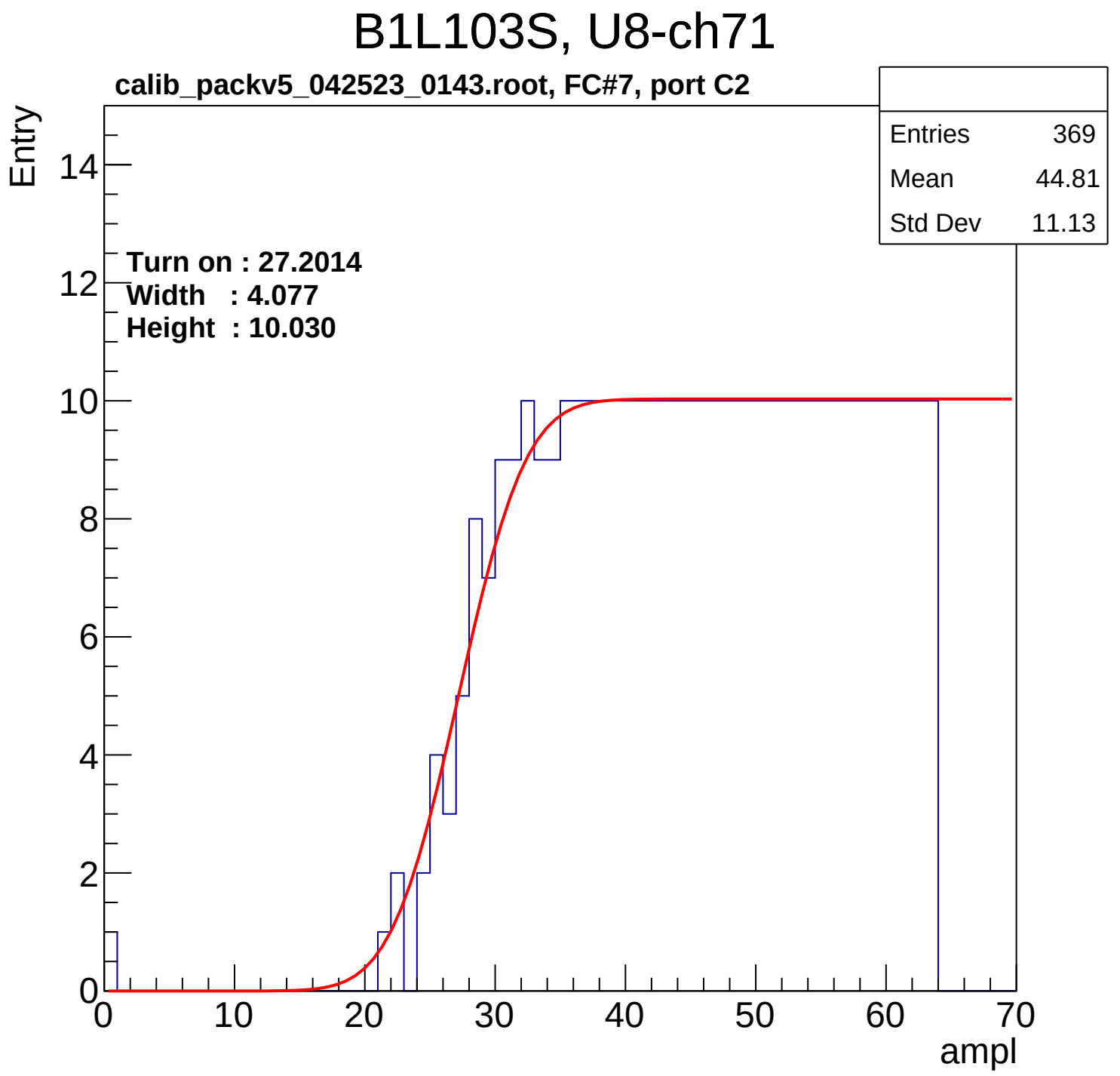
B1L103S, U8-ch71
calib_packv5_042523_0143.root, FC#7, port C2
Entries 369
Mean 44.81
Std Dev 11.13
Turn on : 27.2014
Width : 4.077
Height : 10.030
Entry
ampl
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4
6
8
10
12
14
0
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20
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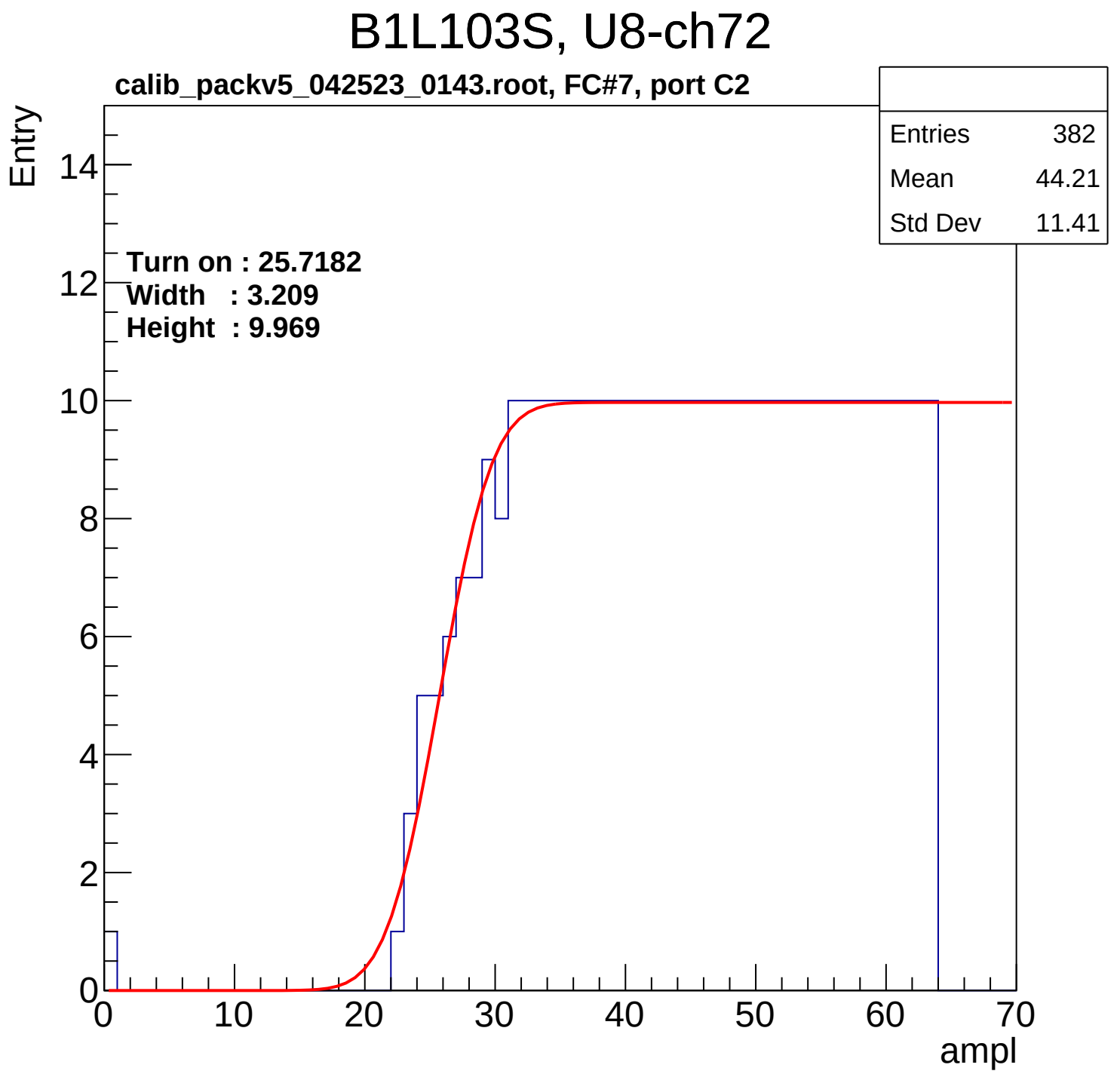
B1L103S, U8-ch72
calib_packv5_042523_0143.root, FC#7, port C2
Entries 382
Mean 44.21
Std Dev 11.41
Turn on : 25.7182
Width : 3.209
Height : 9.969
Entry
ampl
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4
6
8
10
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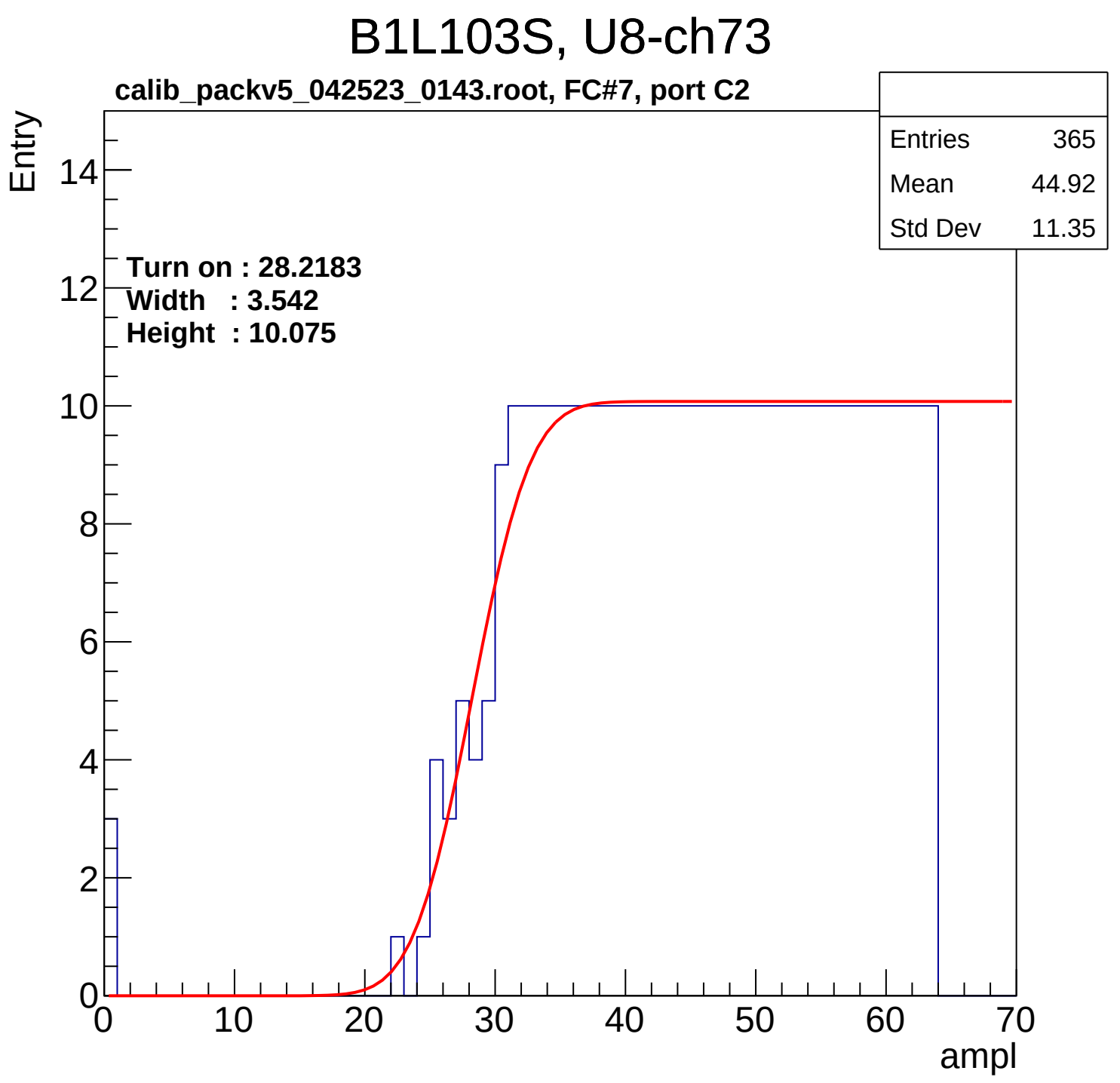
B1L103S, U8-ch73
calib_packv5_042523_0143.root, FC#7, port C2
Entries 365
Mean 44.92
Std Dev 11.35
Turn on : 28.2183
Width : 3.542
Height : 10.075
Entry
ampl
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8
10
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0
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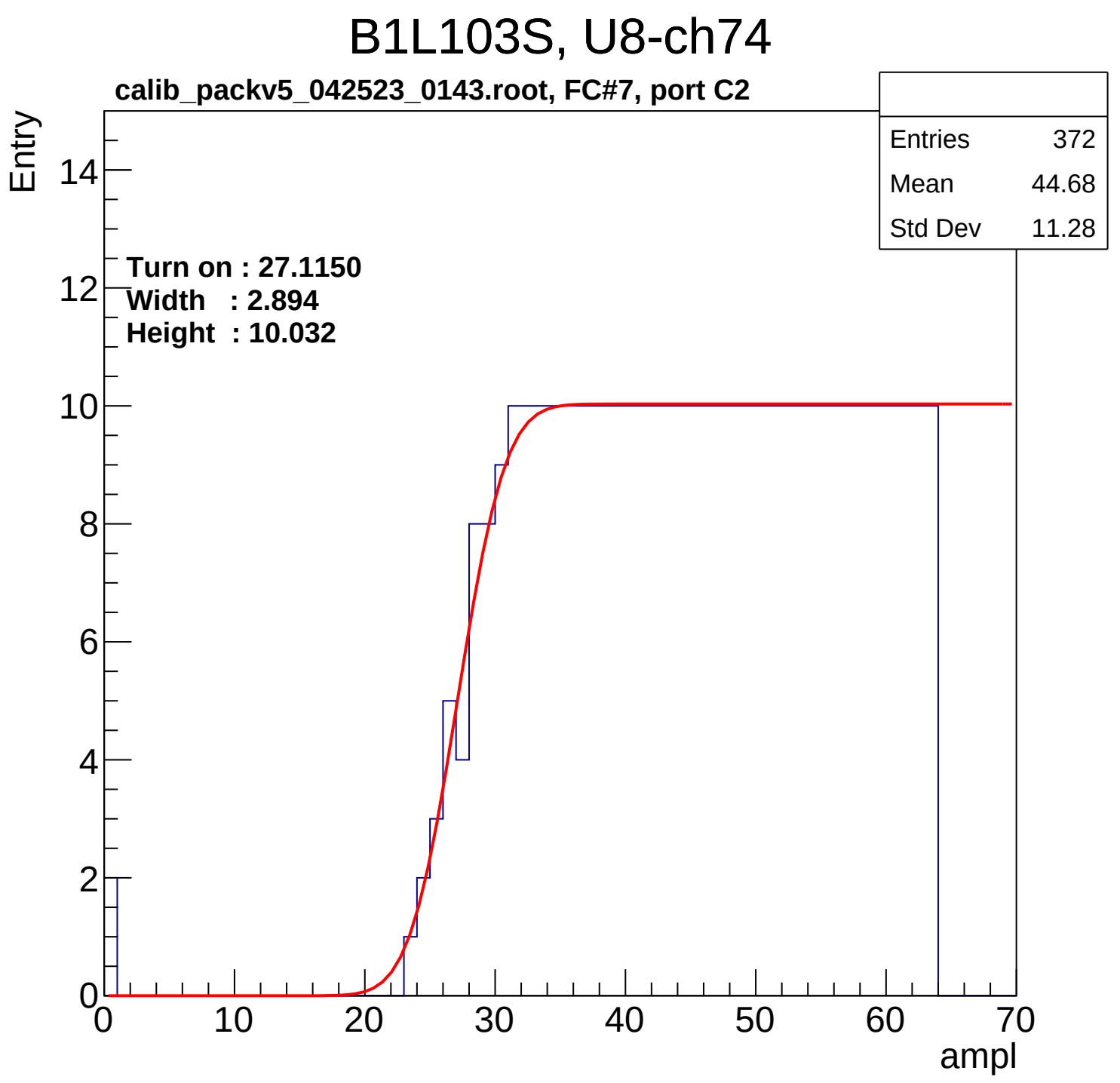
B1L103S, U8-ch74
calib_packv5_042523_0143.root, FC#7, port C2
Entries 372
Mean 44.68
Std Dev 11.28
Turn on : 27.1150
Width : 2.894
Height : 10.032
Entry
ampl
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6
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10
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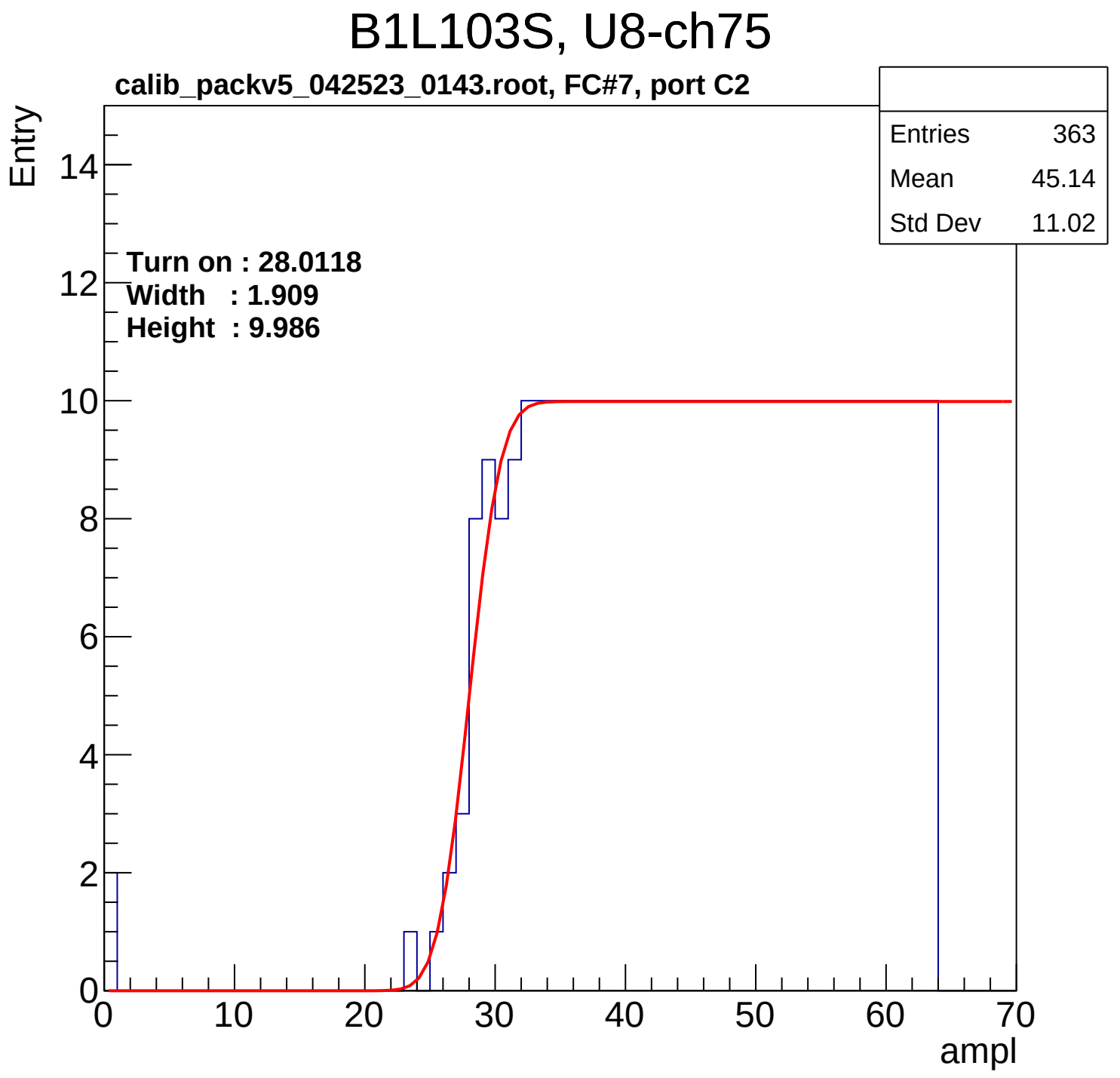
B1L103S, U8-ch75
calib_packv5_042523_0143.root, FC#7, port C2
Entries 363
Mean 45.14
Std Dev 11.02
Turn on : 28.0118
Width : 1.909
Height : 9.986
Entry
ampl
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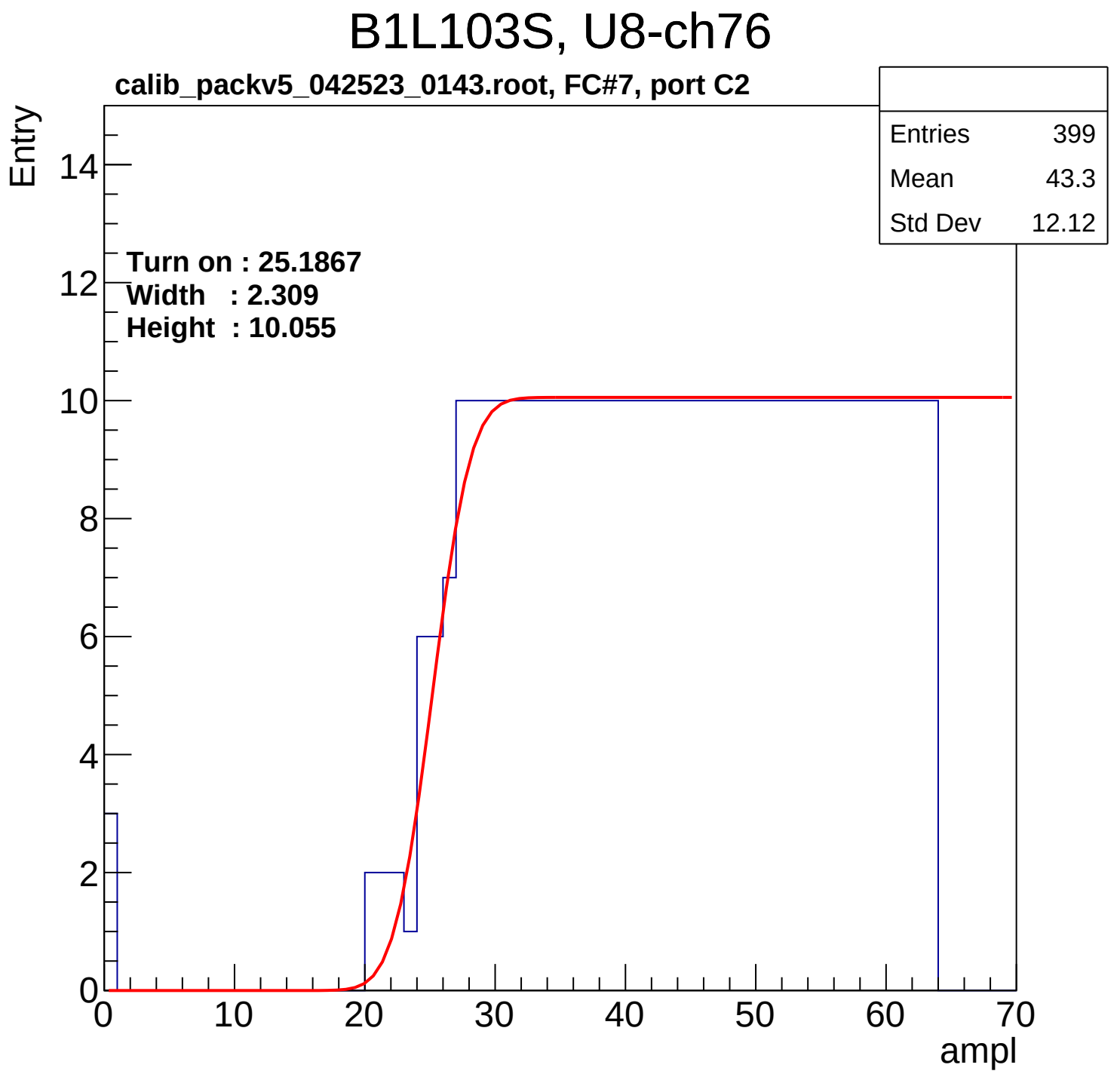
B1L103S, U8-ch76
calib_packv5_042523_0143.root, FC#7, port C2
Entries 399
Mean 43.3
Std Dev 12.12
Turn on : 25.1867
Width : 2.309
Height : 10.055
Entry
ampl
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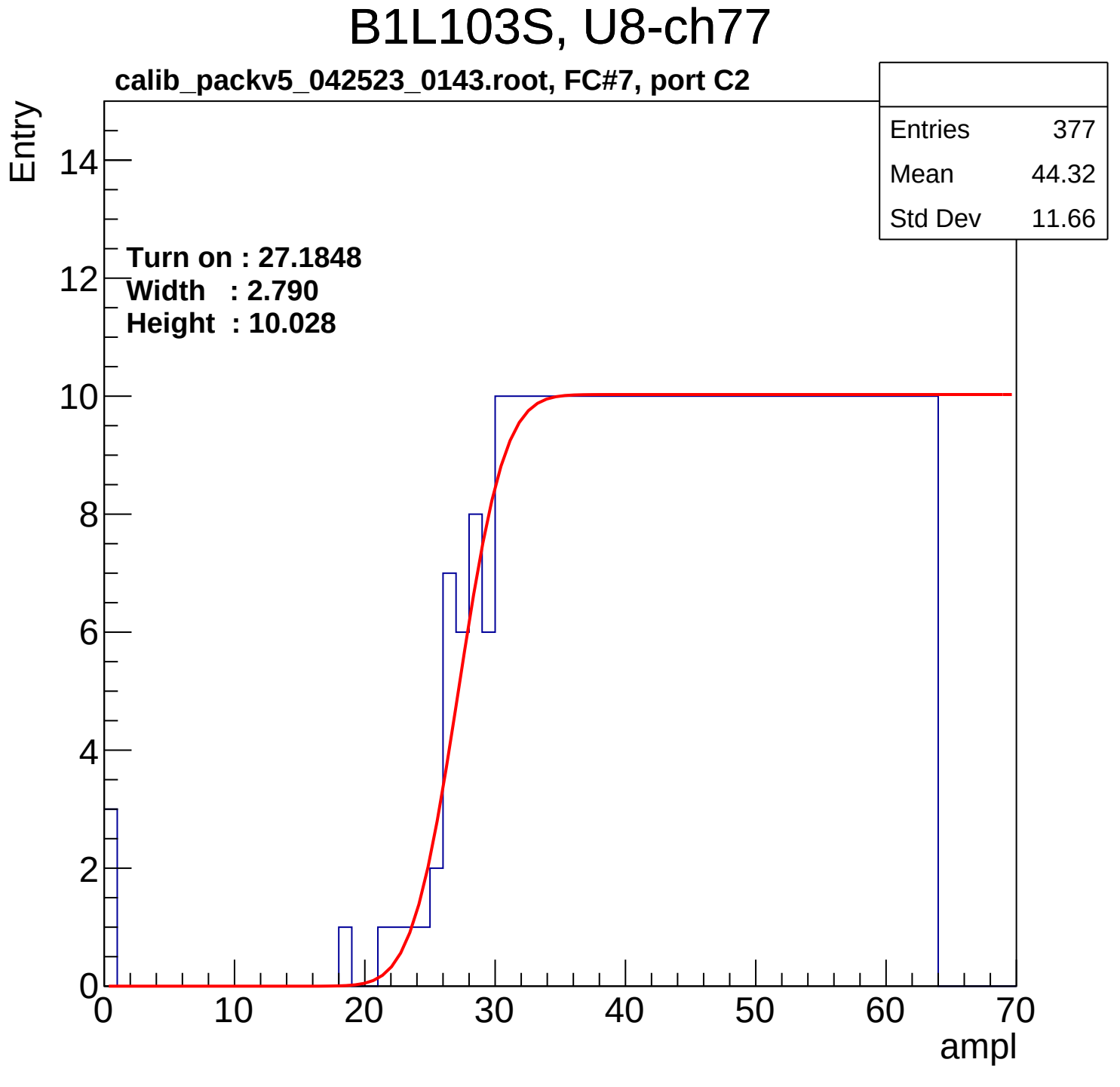
B1L103S, U8-ch77
calib_packv5_042523_0143.root, FC#7, port C2
Entries 377
Mean 44.32
Std Dev 11.66
Turn on : 27.1848
Width : 2.790
Height : 10.028
Entry
ampl
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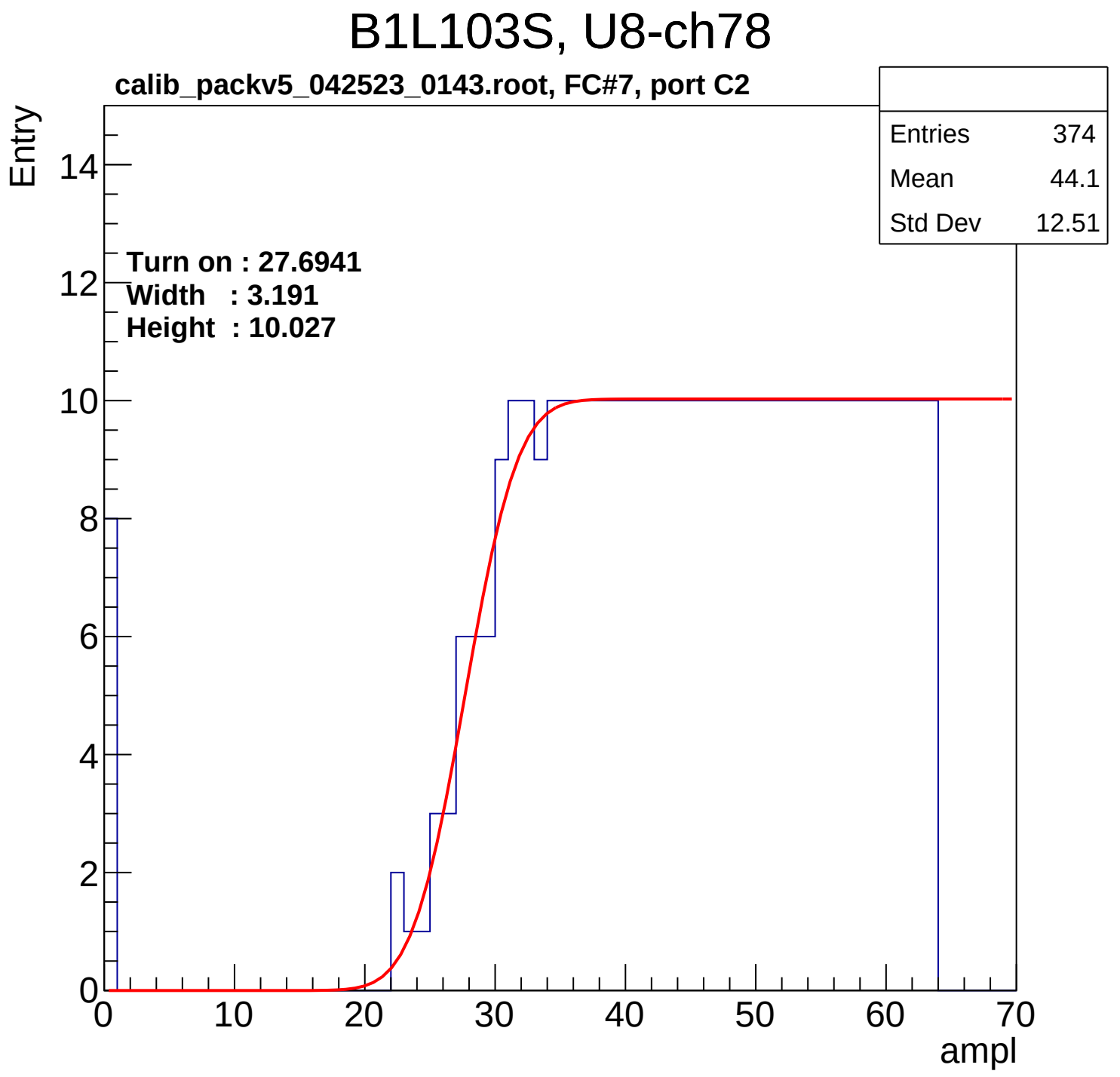
B1L103S, U8-ch78
calib_packv5_042523_0143.root, FC#7, port C2
Entries 374
Mean 44.1
Std Dev 12.51
Turn on : 27.6941
Width : 3.191
Height : 10.027
Entry
ampl
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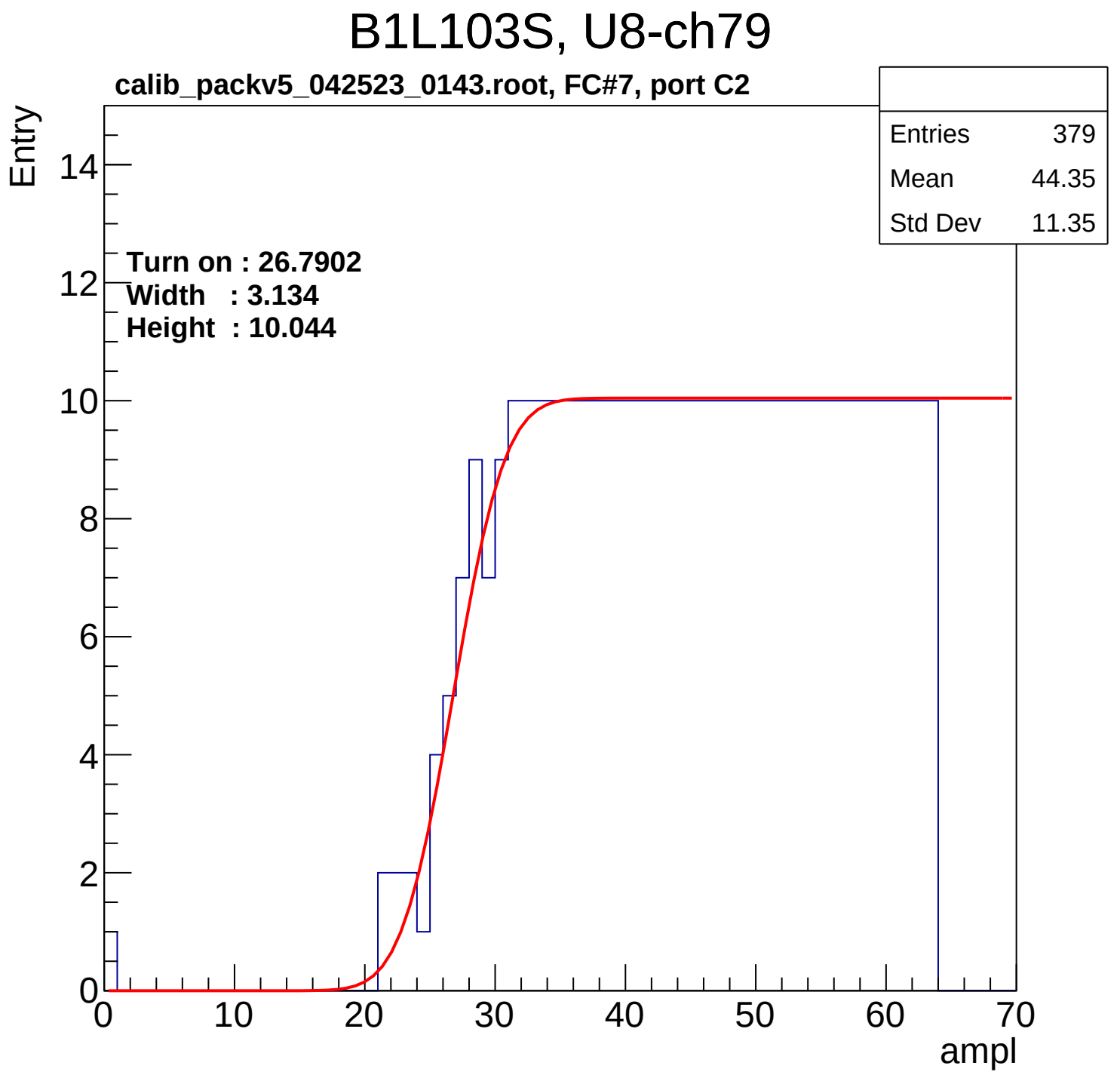
B1L103S, U8-ch79
calib_packv5_042523_0143.root, FC#7, port C2
Entries 379
Mean 44.35
Std Dev 11.35
Turn on : 26.7902
Width : 3.134
Height : 10.044
Entry
ampl
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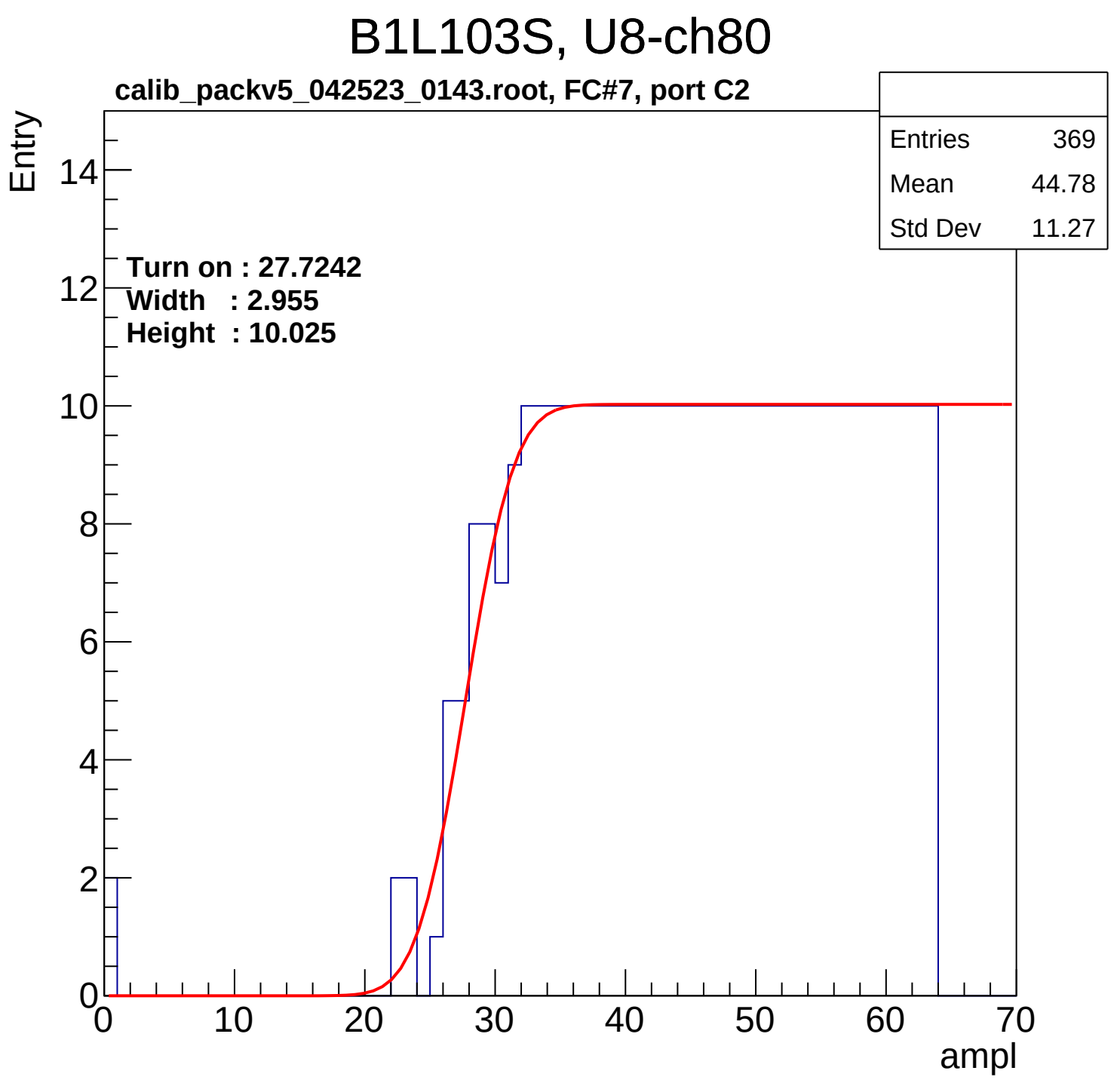
B1L103S, U8-ch80
calib_packv5_042523_0143.root, FC#7, port C2
Entries 369
Mean 44.78
Std Dev 11.27
Turn on : 27.7242
Width : 2.955
Height : 10.025
Entry
ampl
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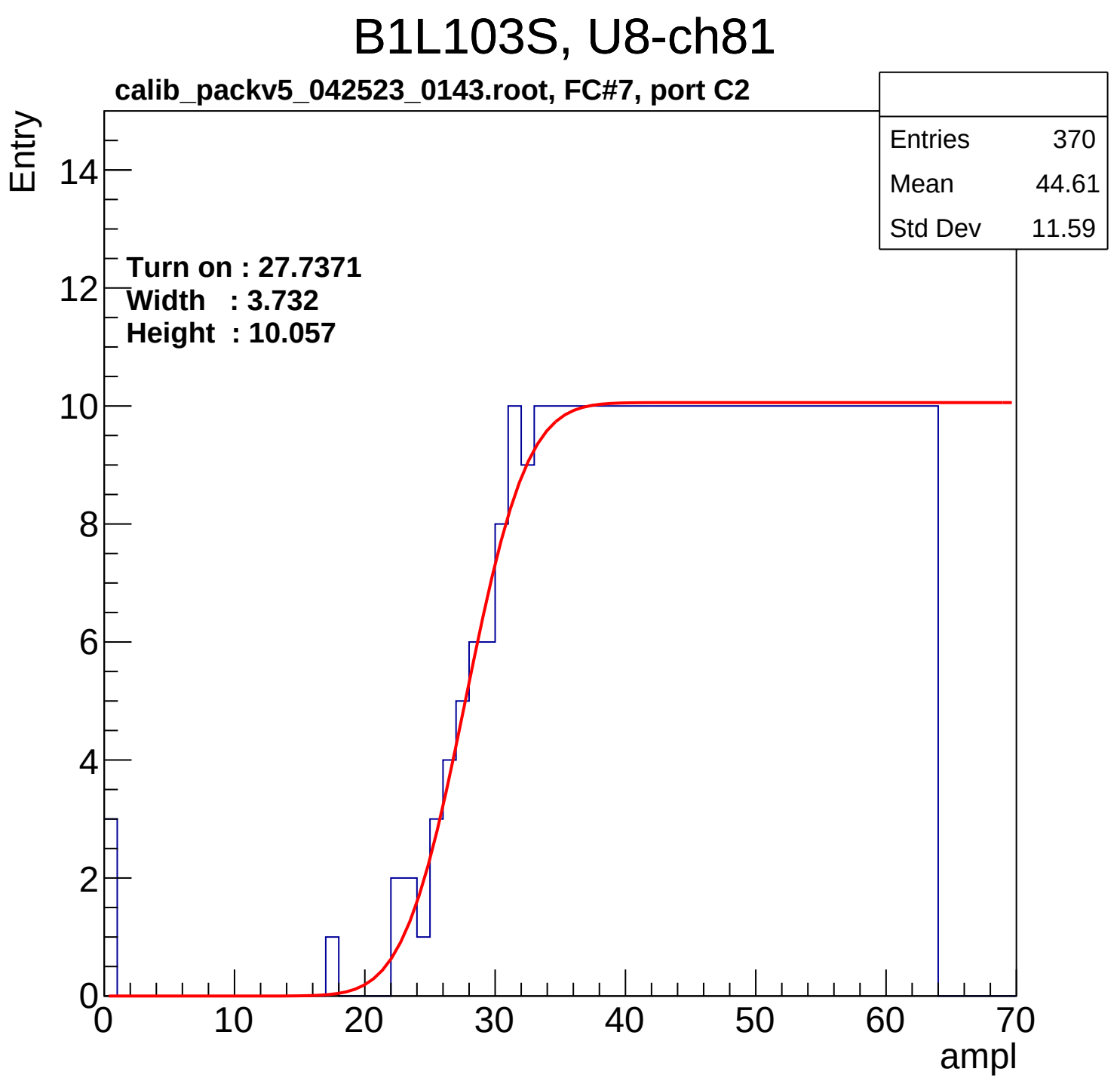
B1L103S, U8-ch81
calib_packv5_042523_0143.root, FC#7, port C2
Entries 370
Mean 44.61
Std Dev 11.59
Turn on : 27.7371
Width : 3.732
Height : 10.057
Entry
ampl
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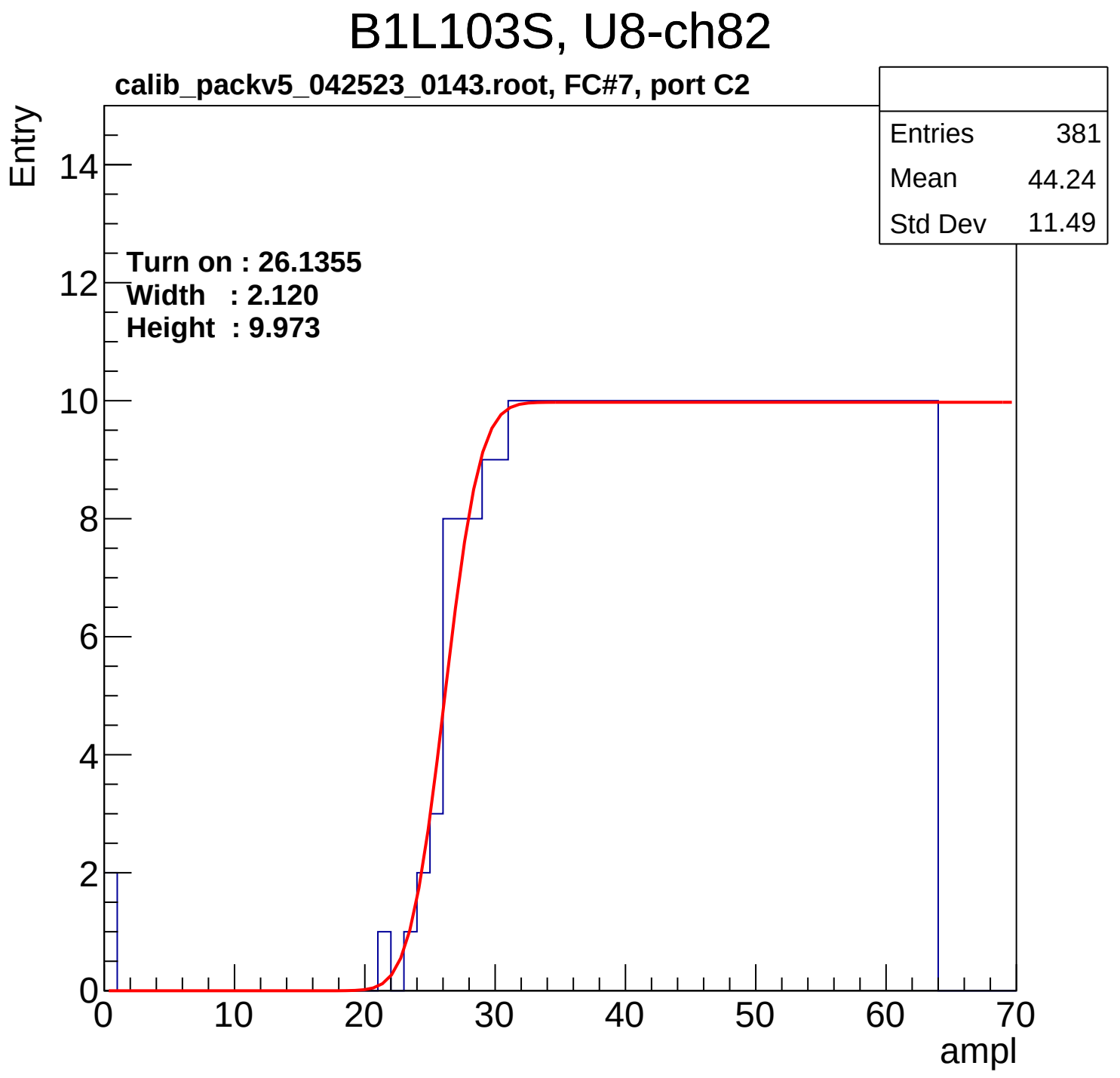
B1L103S, U8-ch82
calib_packv5_042523_0143.root, FC#7, port C2
Entries 381
Mean 44.24
Std Dev 11.49
Turn on : 26.1355
Width : 2.120
Height : 9.973
Entry
ampl
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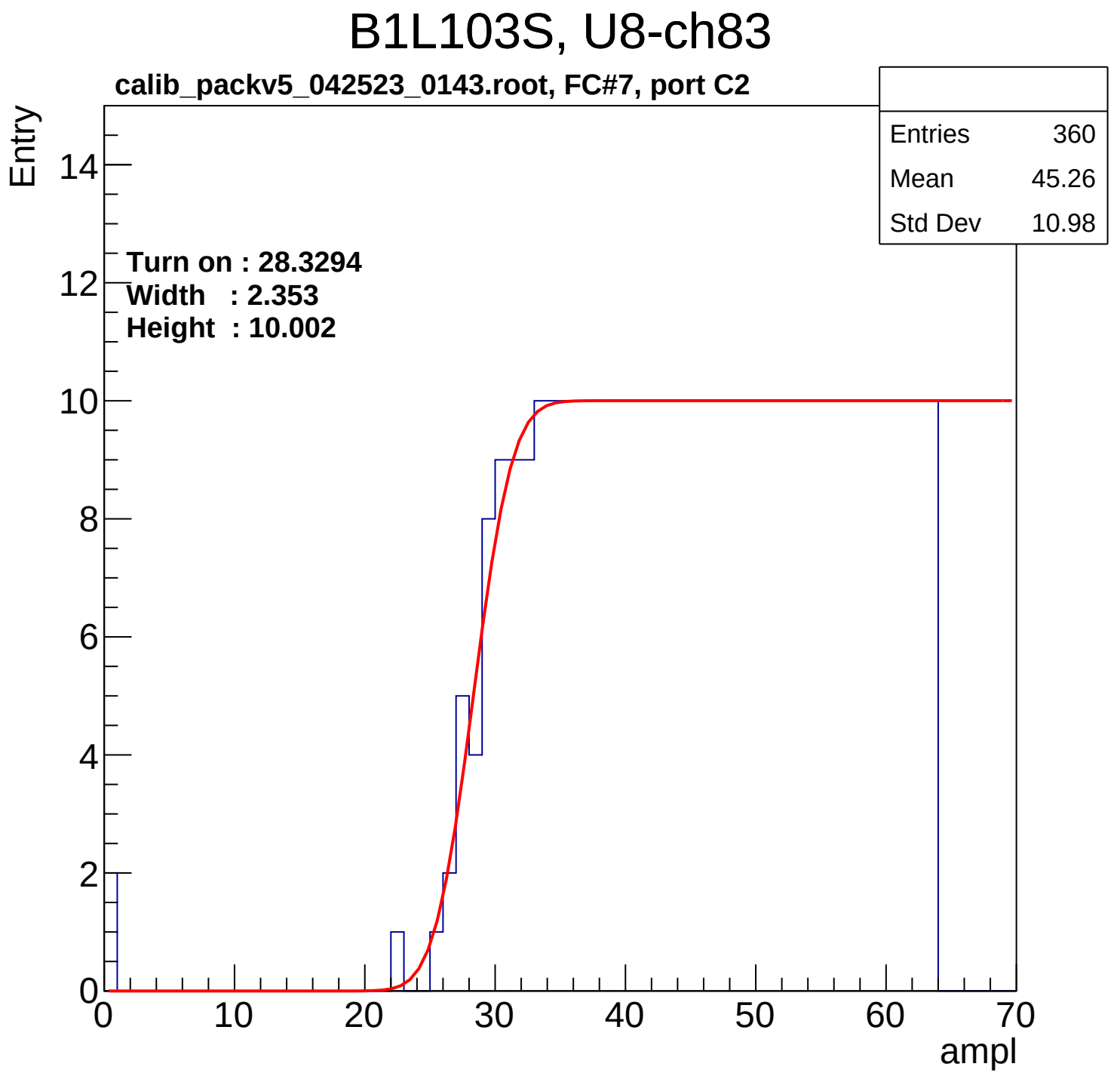
B1L103S, U8-ch83
calib_packv5_042523_0143.root, FC#7, port C2
Entries 360
Mean 45.26
Std Dev 10.98
Turn on : 28.3294
Width : 2.353
Height : 10.002
Entry
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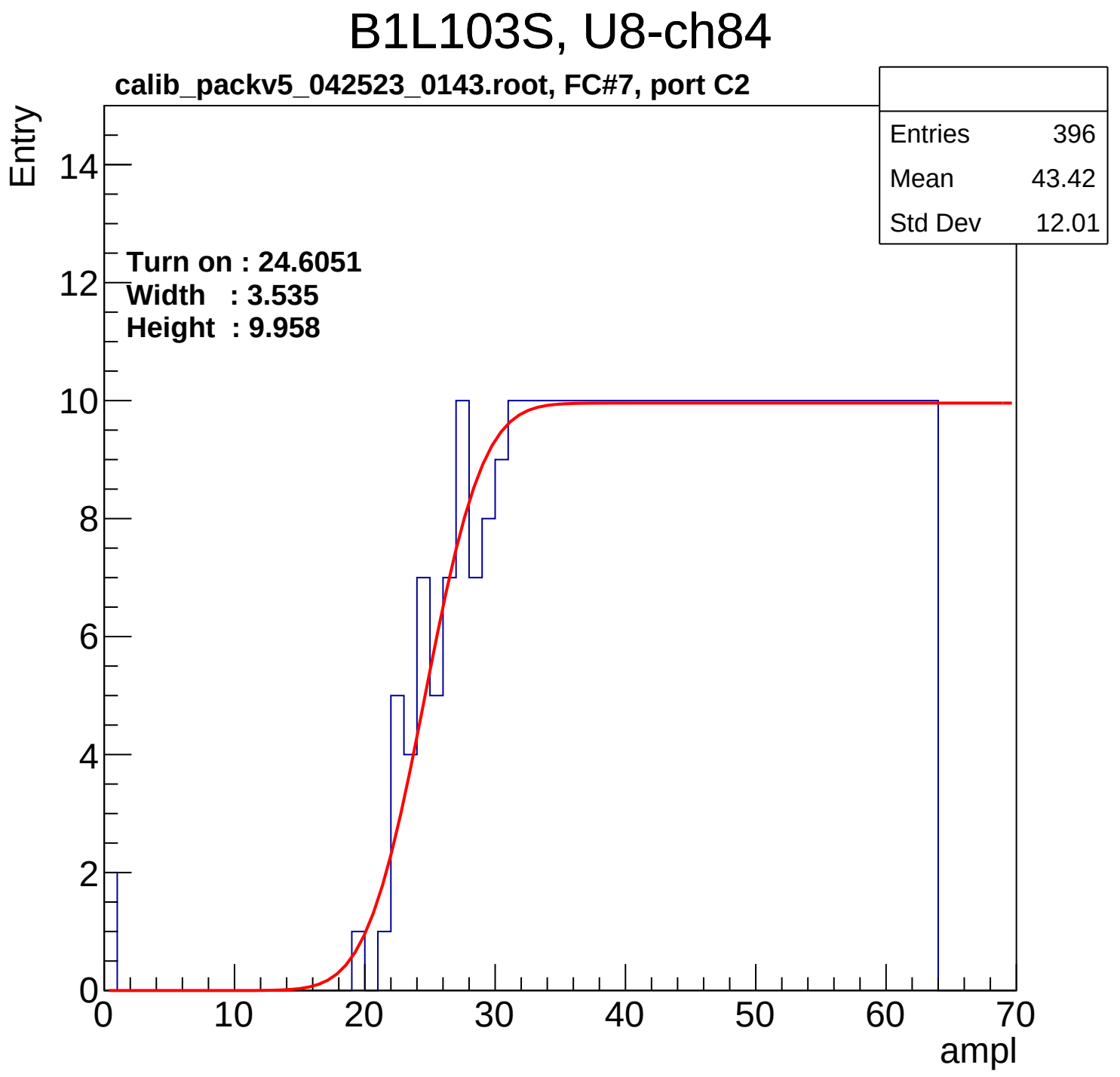
B1L103S, U8-ch84
calib_packv5_042523_0143.root, FC#7, port C2
Entries 396
Mean 43.42
Std Dev 12.01
Turn on : 24.6051
Width : 3.535
Height : 9.958
Entry
ampl
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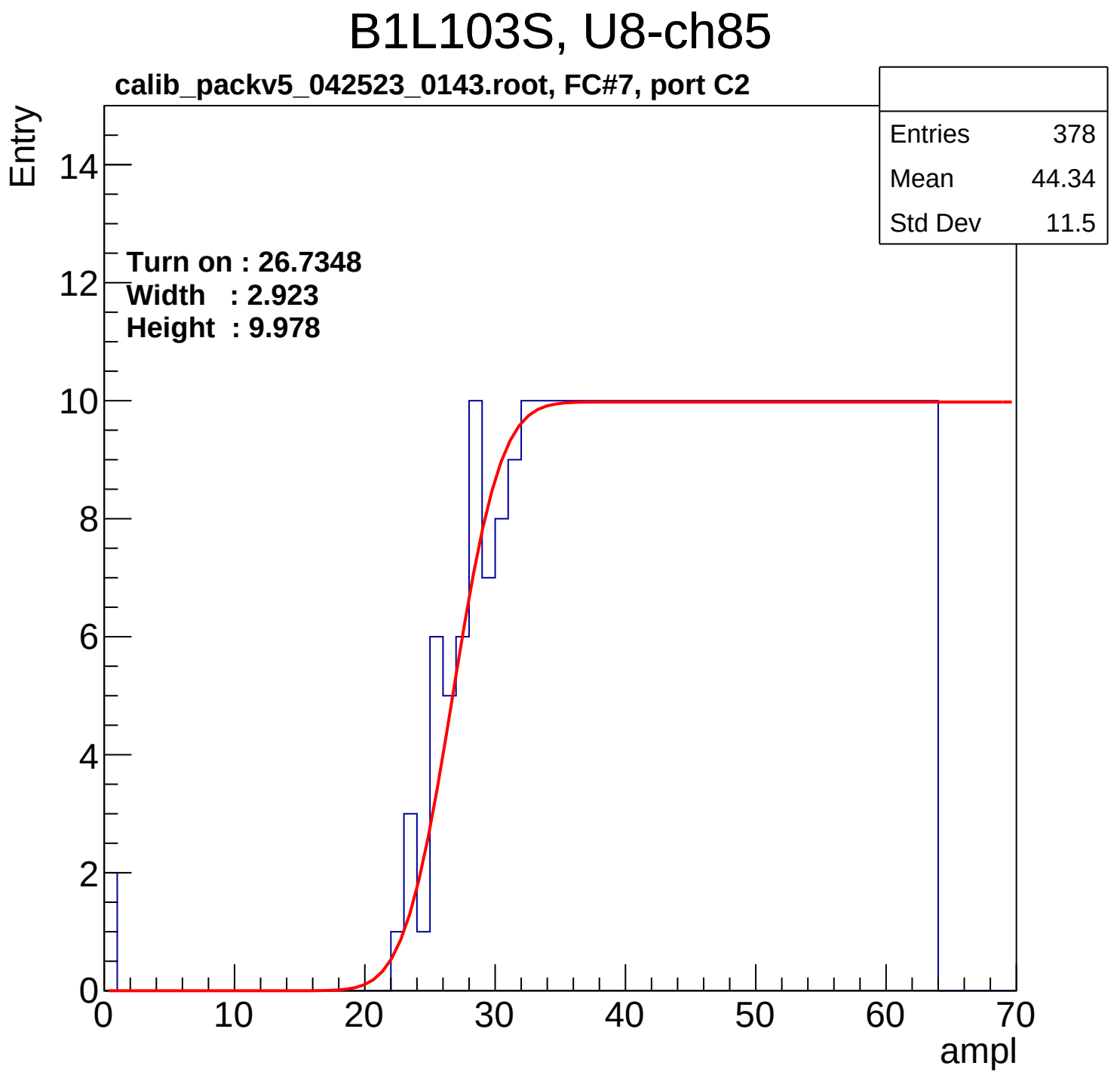
B1L103S, U8-ch85
calib_packv5_042523_0143.root, FC#7, port C2
Entries 378
Mean 44.34
Std Dev 11.5
Turn on : 26.7348
Width : 2.923
Height : 9.978
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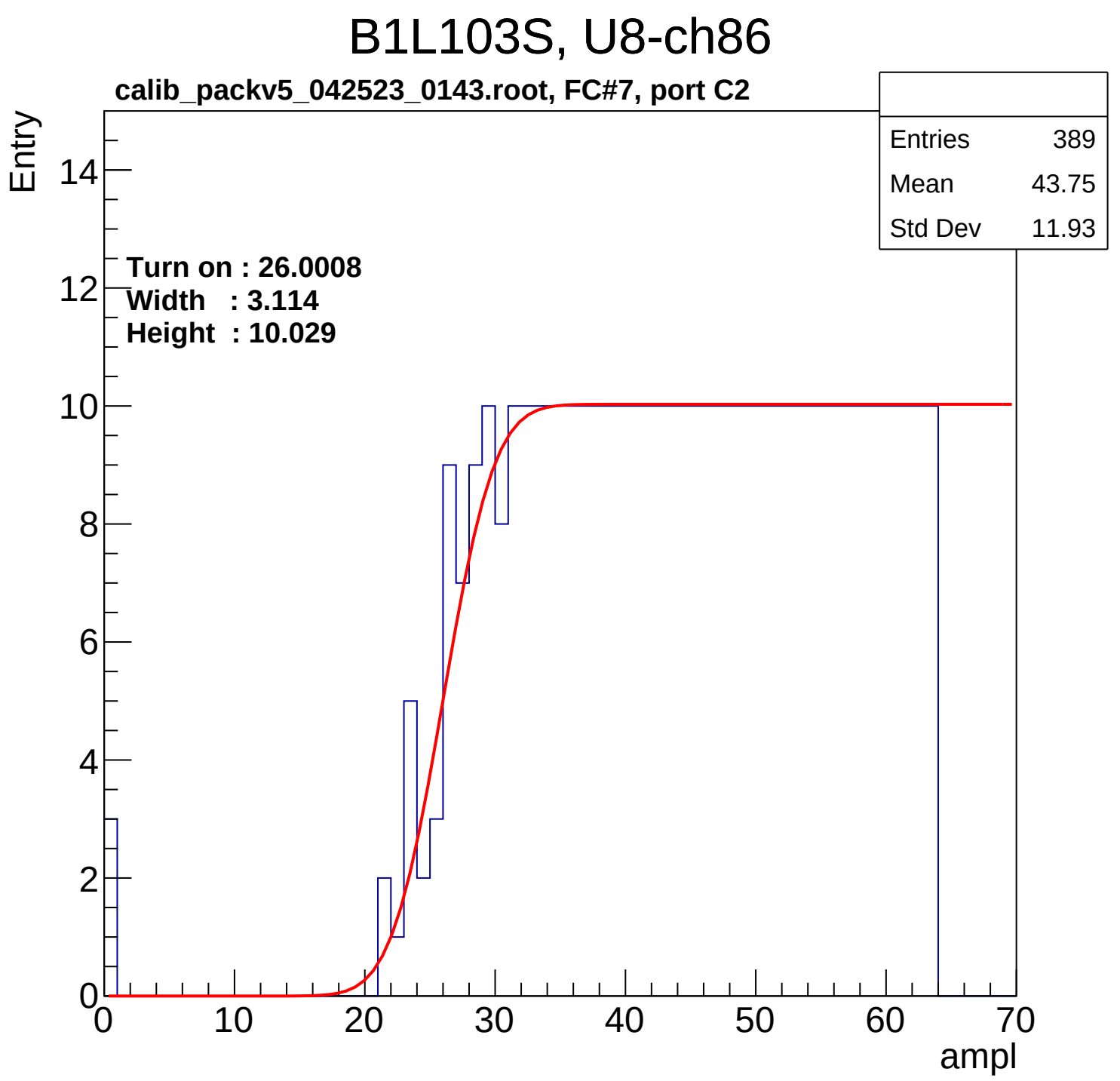
B1L103S, U8-ch86
calib_packv5_042523_0143.root, FC#7, port C2
Entries 389
Mean 43.75
Std Dev 11.93
Turn on : 26.0008
Width : 3.114
Height : 10.029
Entry
ampl
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4
6
8
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12
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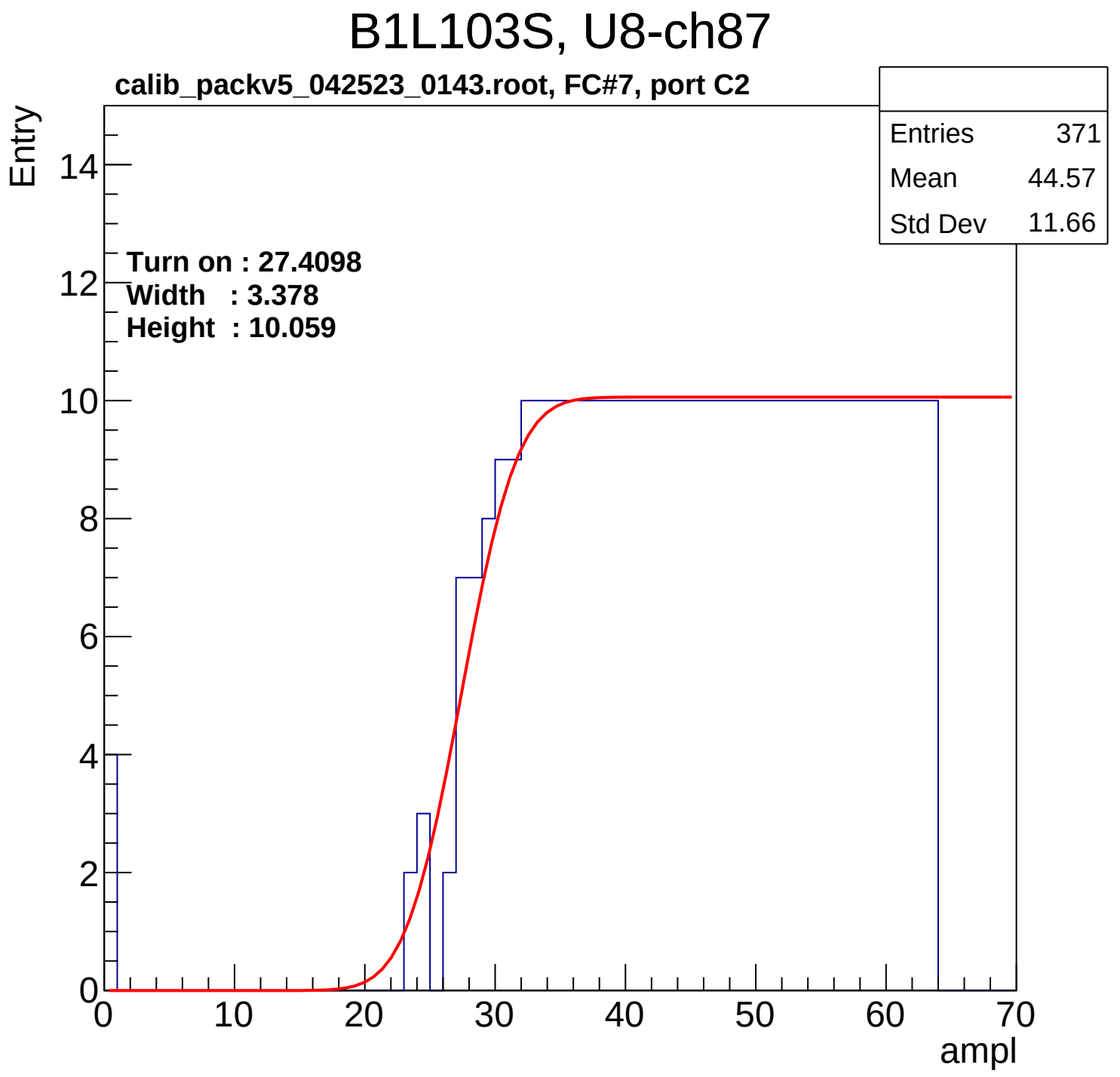
B1L103S, U8-ch87
calib_packv5_042523_0143.root, FC#7, port C2
Entries 371
Mean 44.57
Std Dev 11.66
Turn on : 27.4098
Width : 3.378
Height : 10.059
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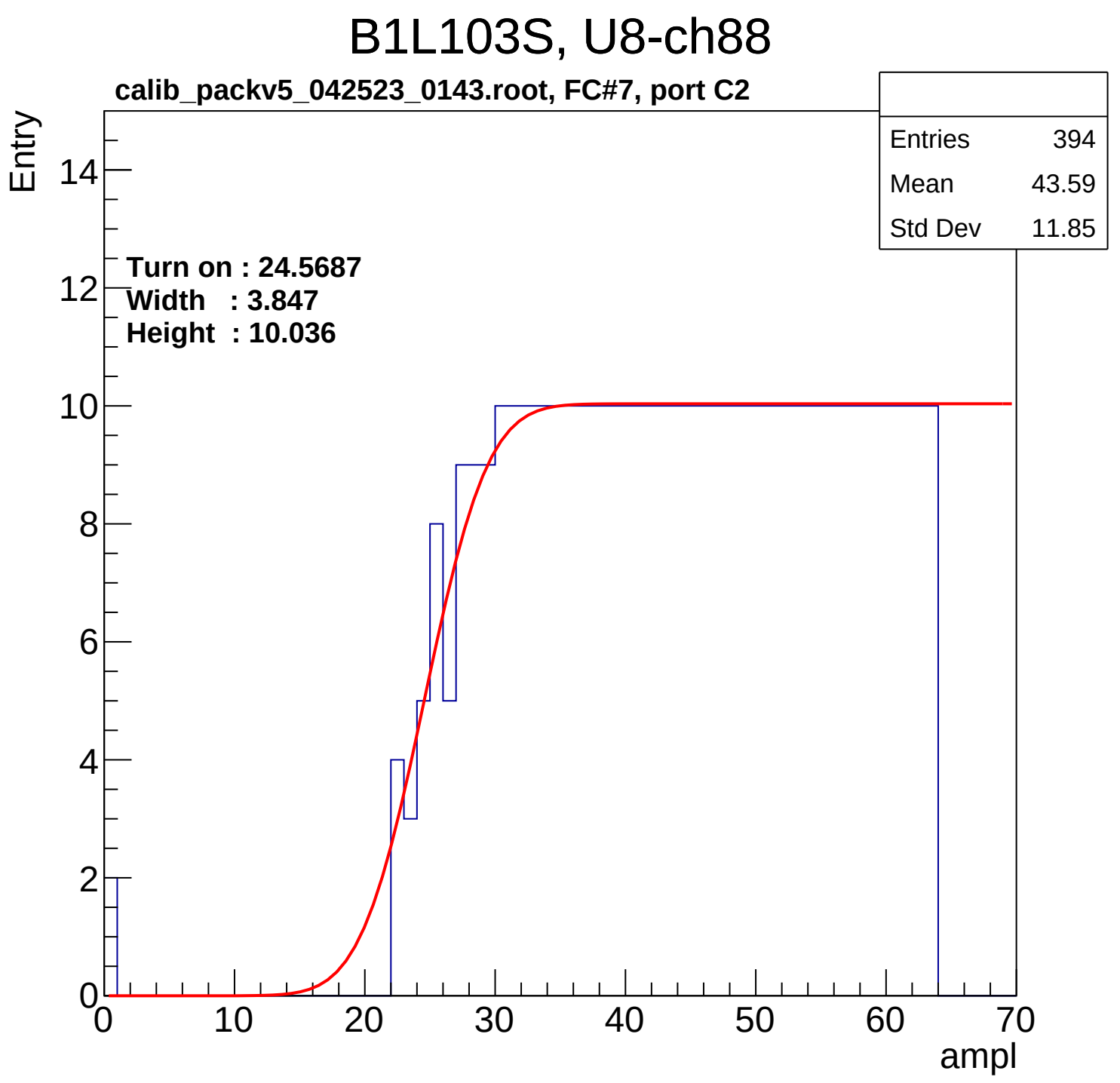
B1L103S, U8-ch88
calib_packv5_042523_0143.root, FC#7, port C2
Entries 394
Mean 43.59
Std Dev 11.85
Turn on : 24.5687
Width : 3.847
Height : 10.036
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ampl
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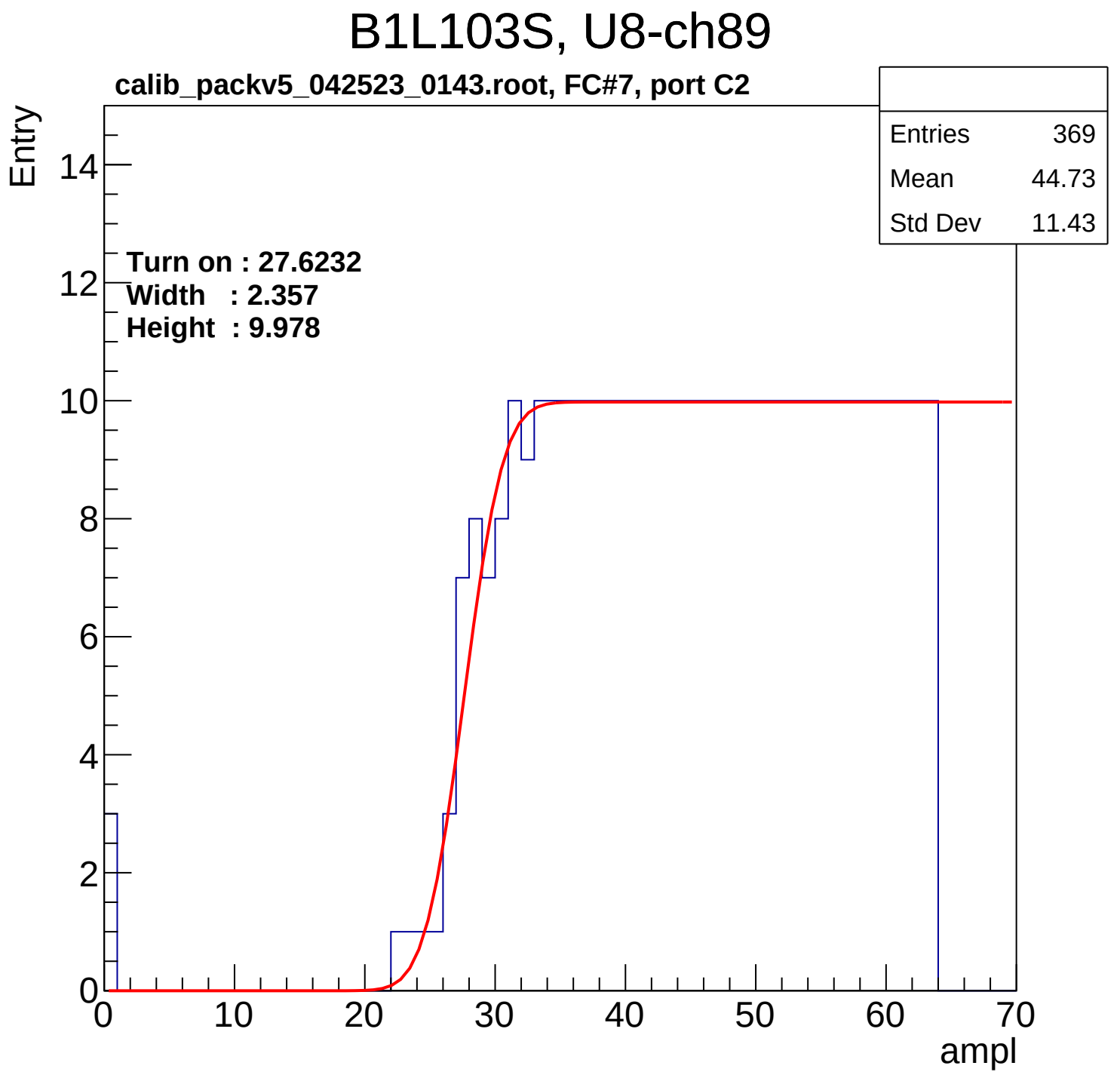
B1L103S, U8-ch89
calib_packv5_042523_0143.root, FC#7, port C2
Entries 369
Mean 44.73
Std Dev 11.43
Turn on : 27.6232
Width : 2.357
Height : 9.978
Entry
ampl
0
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4
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8
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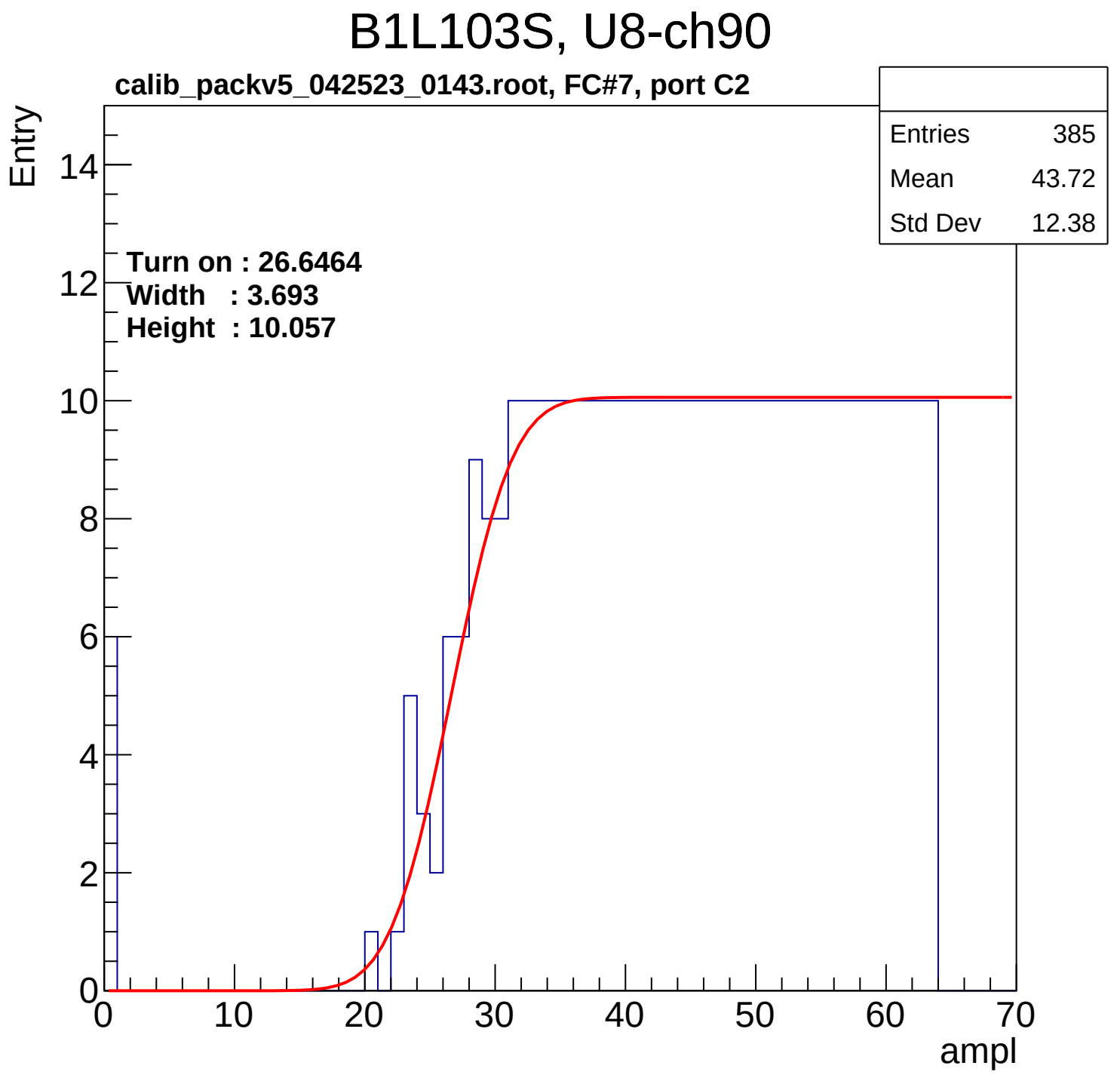
B1L103S, U8-ch90
calib_packv5_042523_0143.root, FC#7, port C2
Entries 385
Mean 43.72
Std Dev 12.38
Turn on : 26.6464
Width : 3.693
Height : 10.057
Entry
ampl
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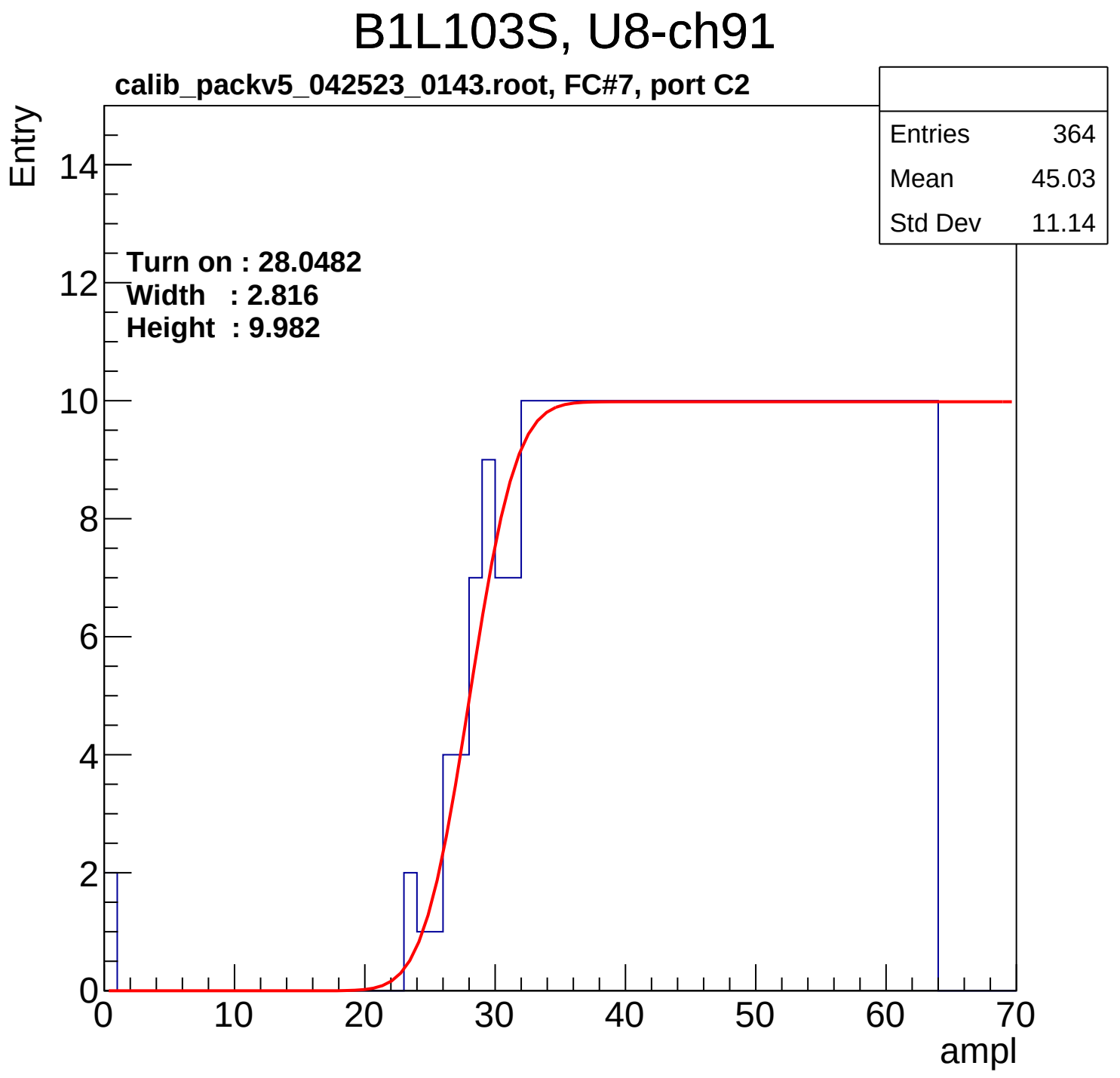
B1L103S, U8-ch91
calib_packv5_042523_0143.root, FC#7, port C2
Entries 364
Mean 45.03
Std Dev 11.14
Turn on : 28.0482
Width : 2.816
Height : 9.982
Entry
ampl
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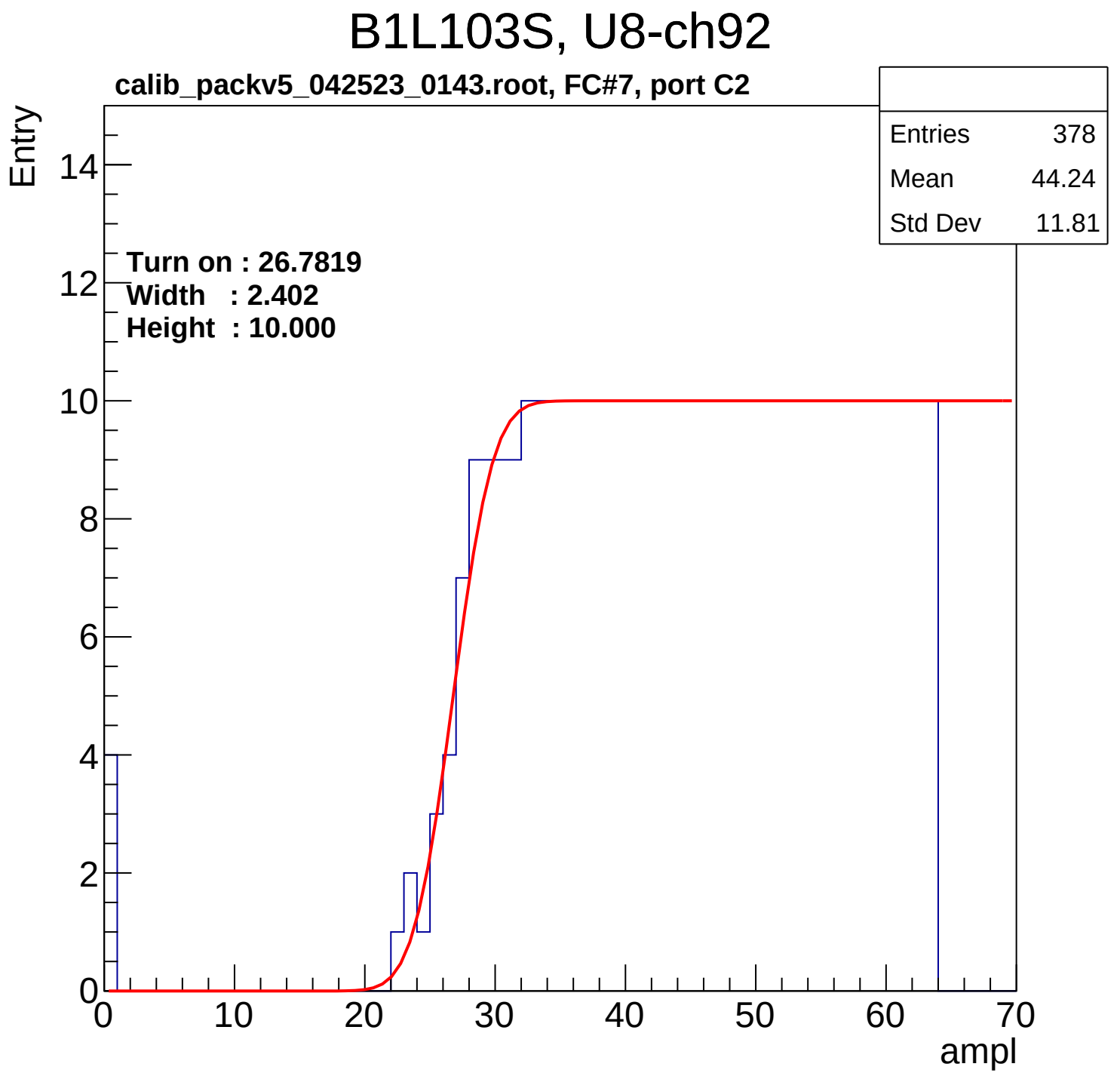
B1L103S, U8-ch92
calib_packv5_042523_0143.root, FC#7, port C2
Entries 378
Mean 44.24
Std Dev 11.81
Turn on : 26.7819
Width : 2.402
Height : 10.000
Entry
ampl
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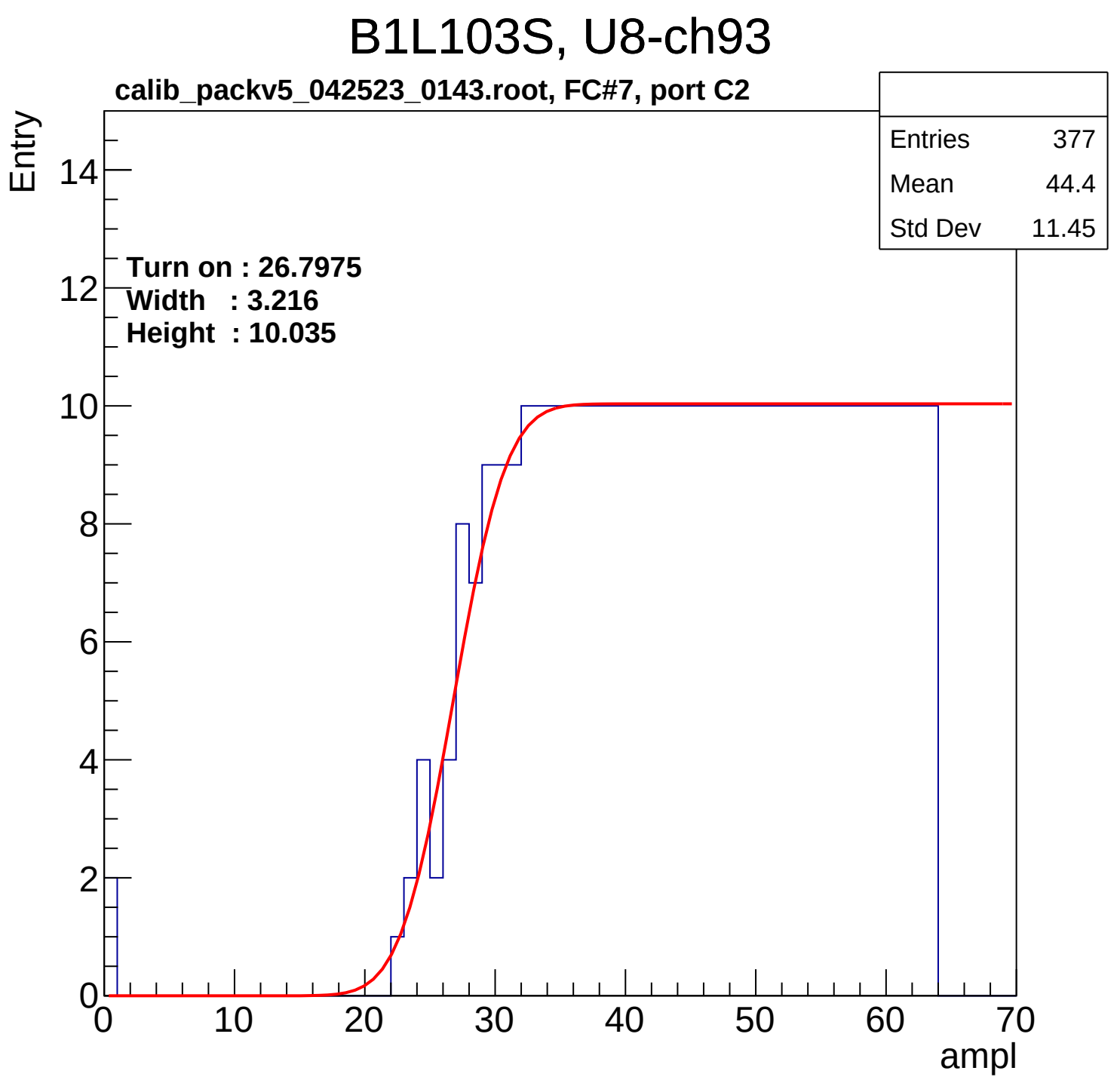
B1L103S, U8-ch93
calib_packv5_042523_0143.root, FC#7, port C2
Entries 377
Mean 44.4
Std Dev 11.45
Turn on : 26.7975
Width : 3.216
Height : 10.035
Entry
ampl
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6
8
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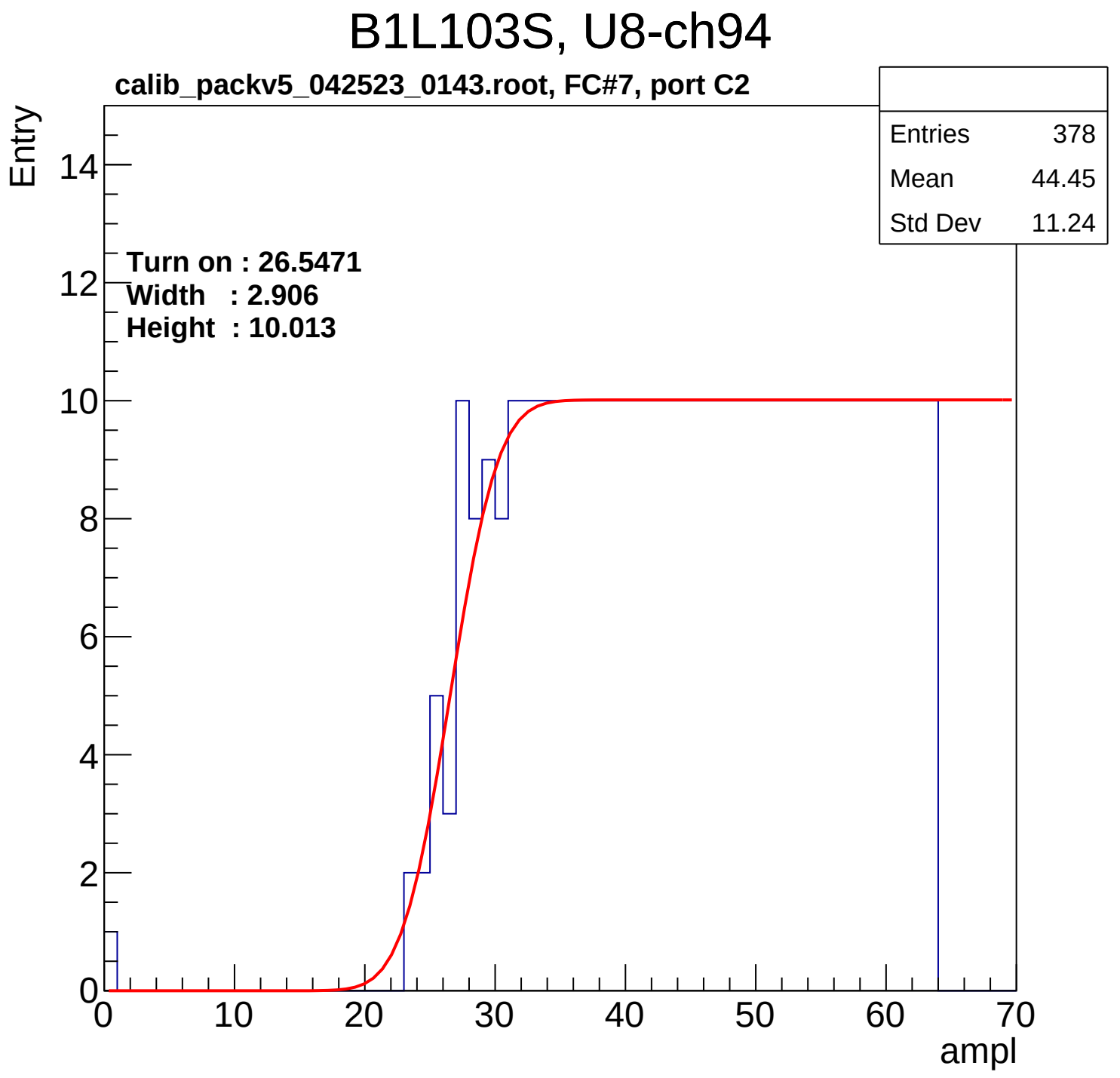
B1L103S, U8-ch94
calib_packv5_042523_0143.root, FC#7, port C2
Entries 378
Mean 44.45
Std Dev 11.24
Turn on : 26.5471
Width : 2.906
Height : 10.013
Entry
ampl
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6
8
10
12
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60
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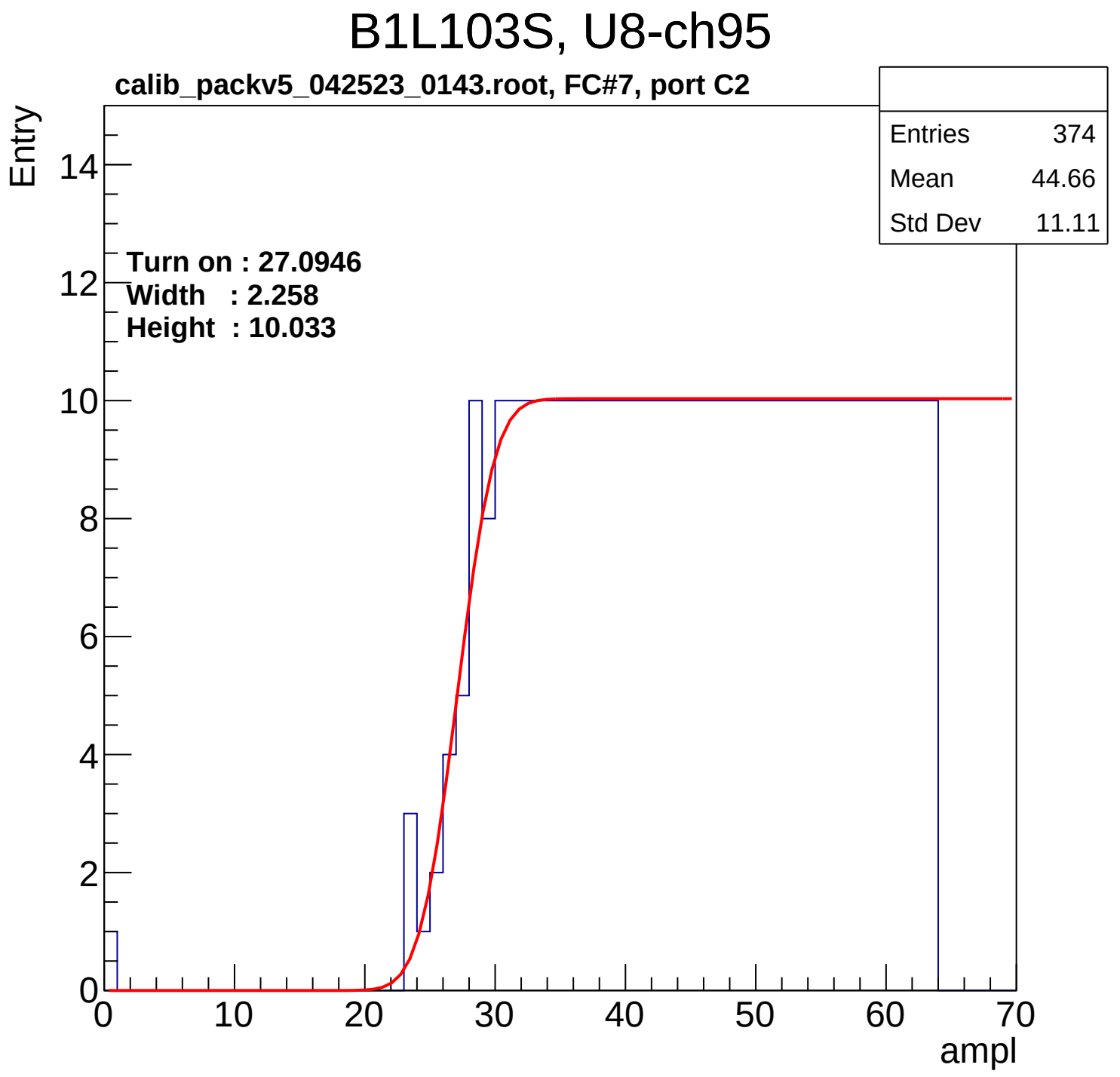
B1L103S, U8-ch95
calib_packv5_042523_0143.root, FC#7, port C2
Entries 374
Mean 44.66
Std Dev 11.11
Turn on : 27.0946
Width : 2.258
Height : 10.033
Entry
ampl
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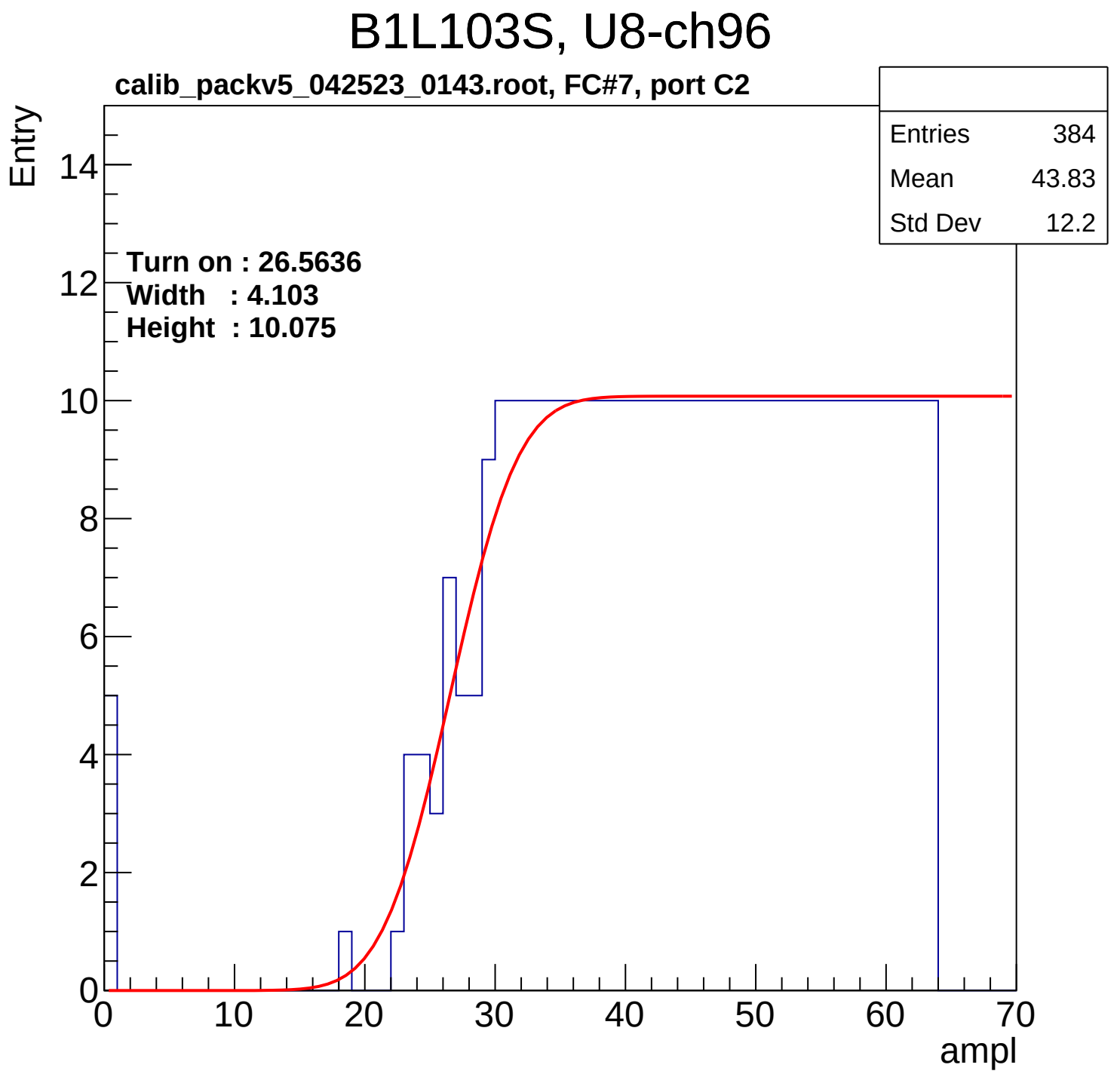
B1L103S, U8-ch96
calib_packv5_042523_0143.root, FC#7, port C2
Entries 384
Mean 43.83
Std Dev 12.2
Turn on : 26.5636
Width : 4.103
Height : 10.075
Entry
ampl
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6
8
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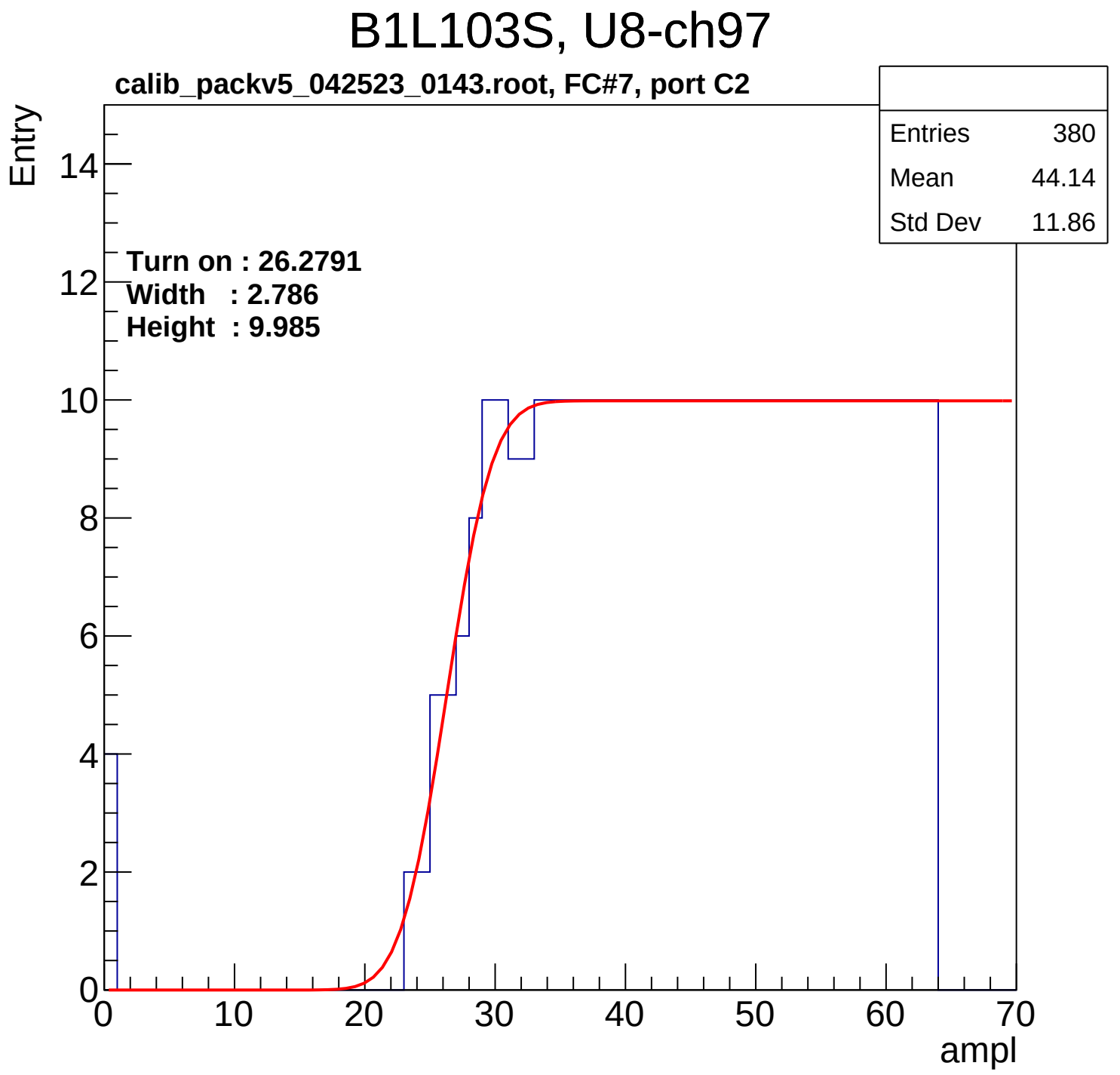
B1L103S, U8-ch97
calib_packv5_042523_0143.root, FC#7, port C2
Entries 380
Mean 44.14
Std Dev 11.86
Turn on : 26.2791
Width : 2.786
Height : 9.985
Entry
ampl
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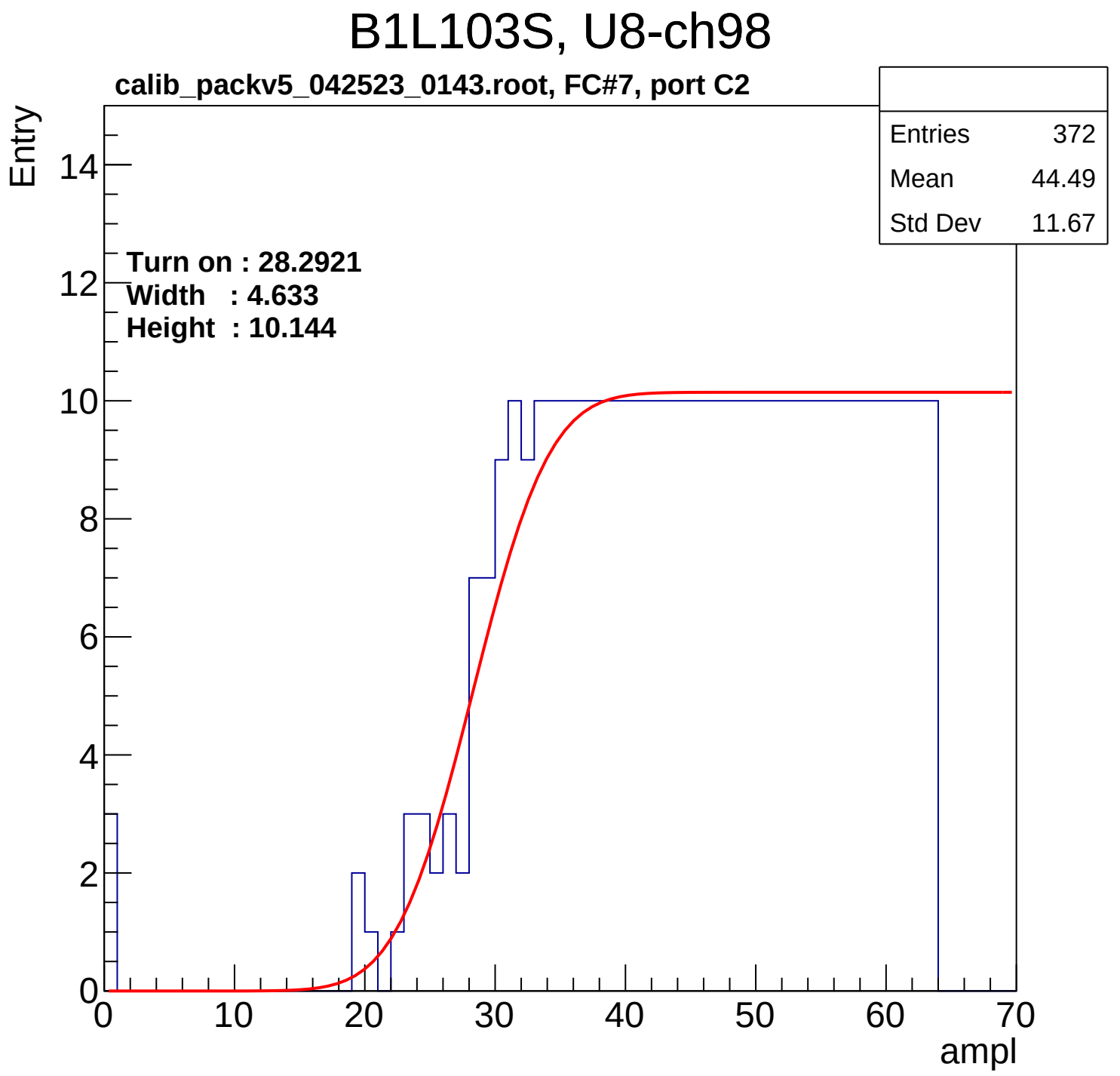
B1L103S, U8-ch98
calib_packv5_042523_0143.root, FC#7, port C2
Entries 372
Mean 44.49
Std Dev 11.67
Turn on : 28.2921
Width : 4.633
Height : 10.144
Entry
ampl
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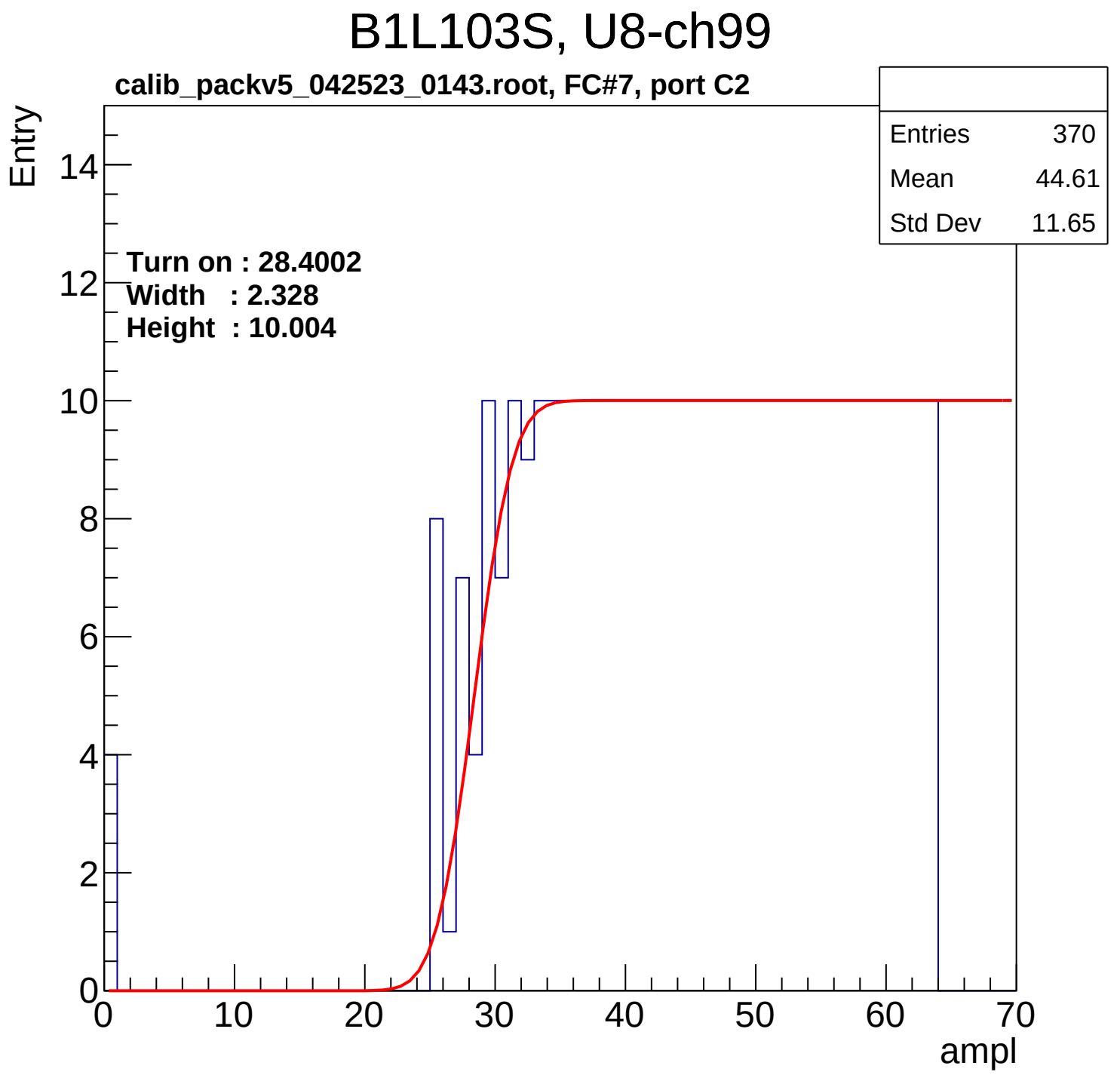
B1L103S, U8-ch99
calib_packv5_042523_0143.root, FC#7, port C2
Entries 370
Mean 44.61
Std Dev 11.65
Turn on : 28.4002
Width : 2.328
Height : 10.004
Entry
ampl
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6
8
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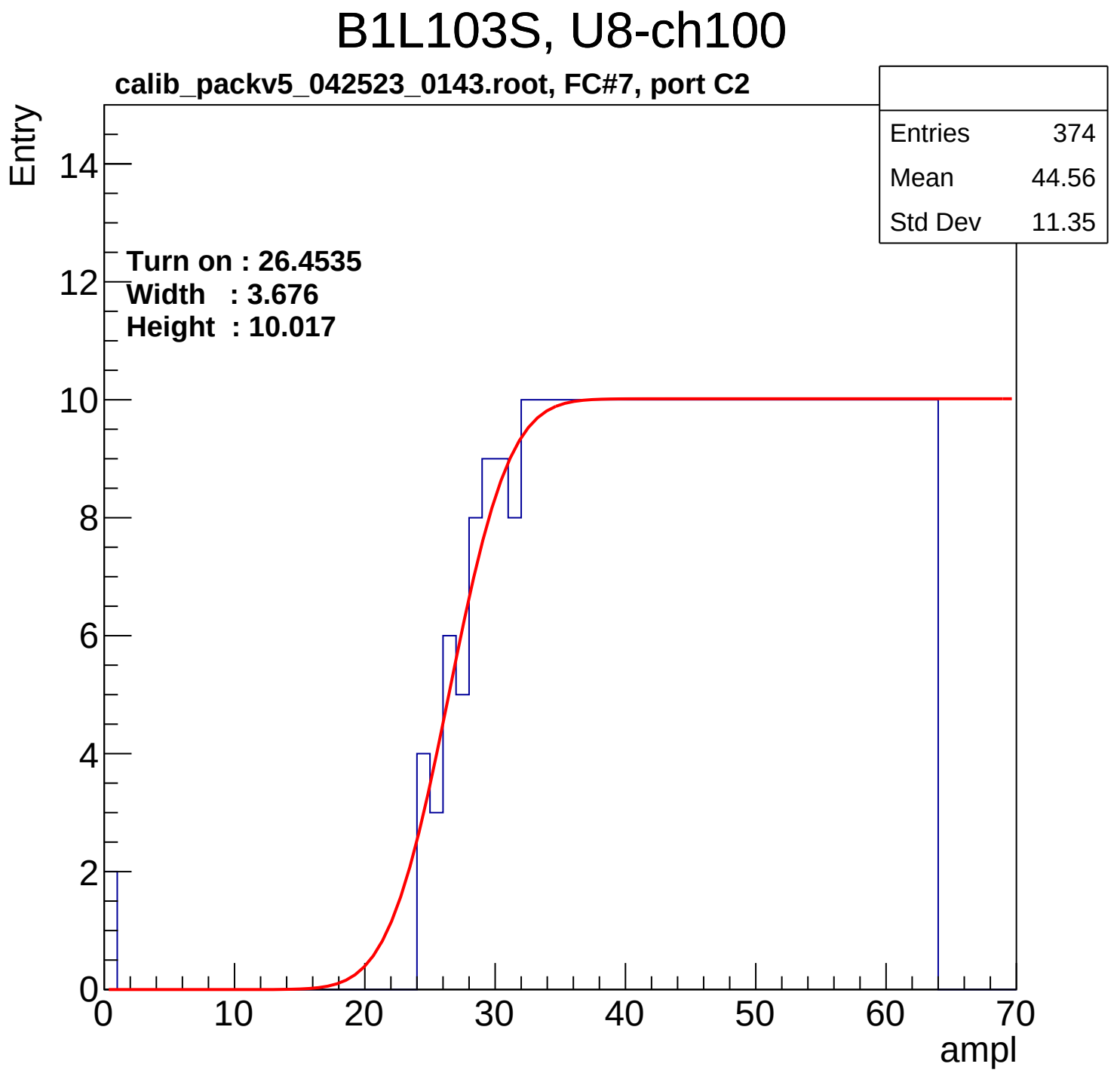
B1L103S, U8-ch100
calib_packv5_042523_0143.root, FC#7, port C2
Entries 374
Mean 44.56
Std Dev 11.35
Turn on : 26.4535
Width : 3.676
Height : 10.017
Entry
ampl
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6
8
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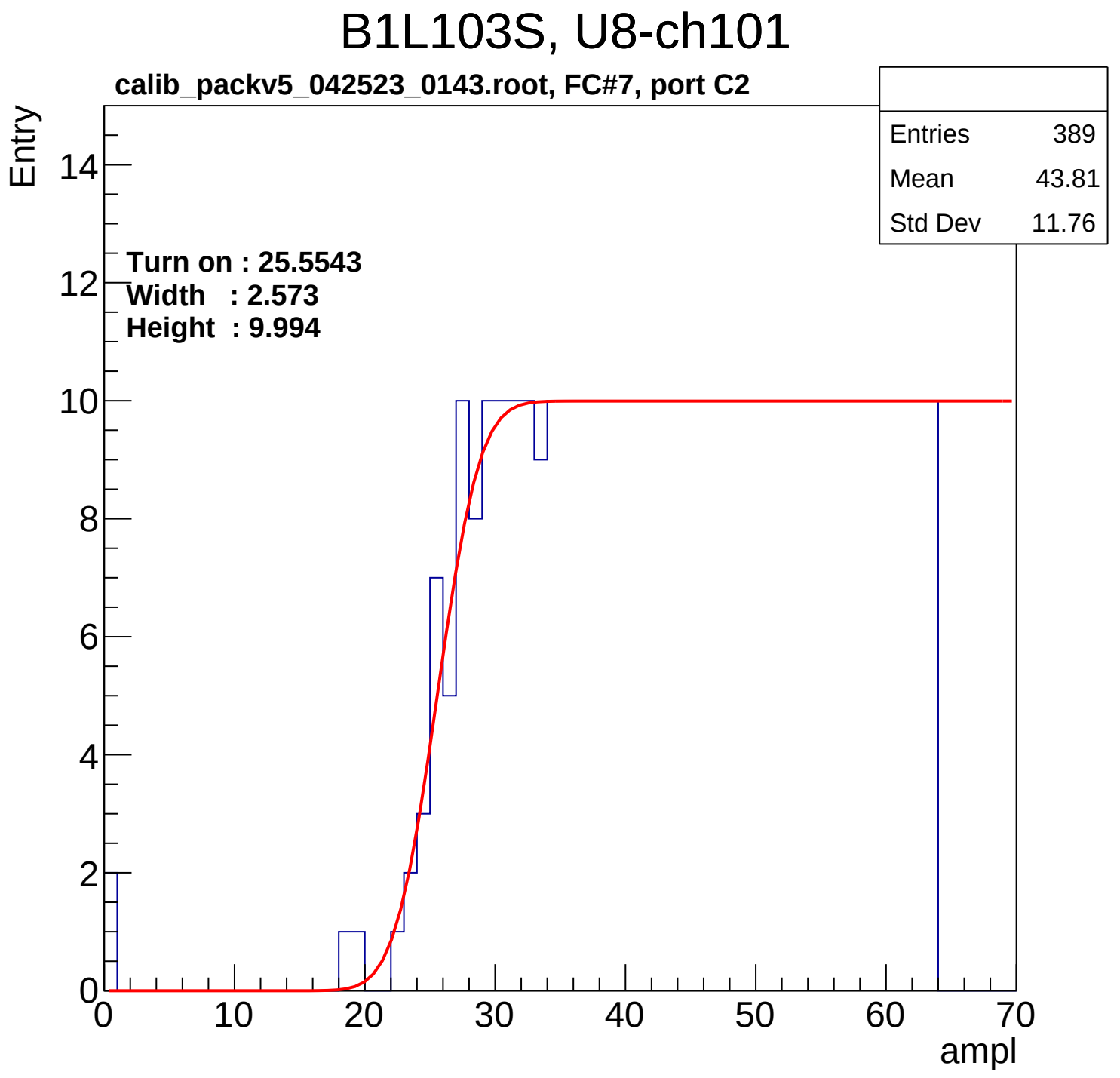
B1L103S, U8-ch101
calib_packv5_042523_0143.root, FC#7, port C2
Entries 389
Mean 43.81
Std Dev 11.76
Turn on : 25.5543
Width : 2.573
Height : 9.994
Entry
ampl
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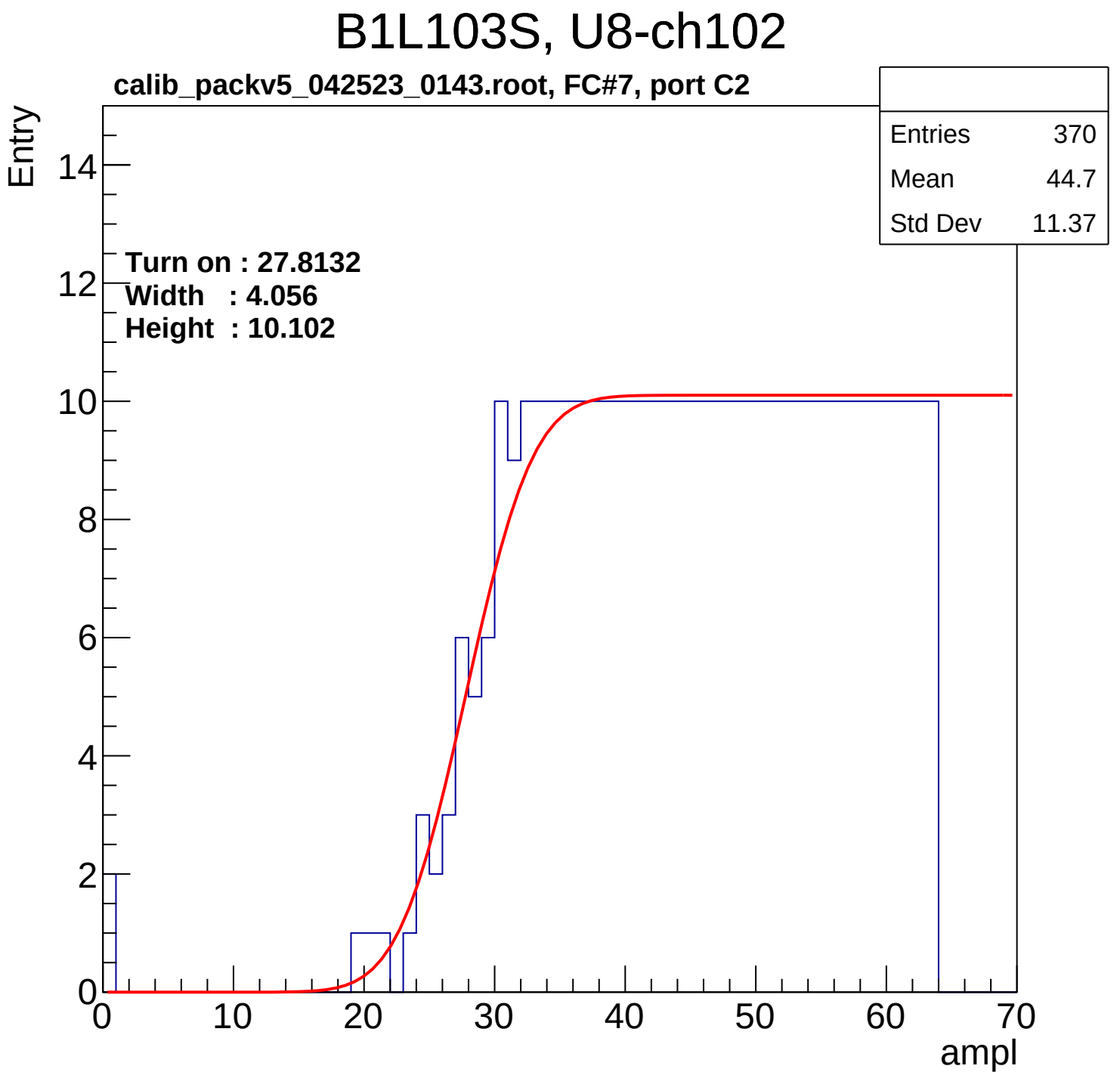
B1L103S, U8-ch102
calib_packv5_042523_0143.root, FC#7, port C2
Entries 370
Mean 44.7
Std Dev 11.37
Turn on : 27.8132
Width : 4.056
Height : 10.102
Entry
ampl
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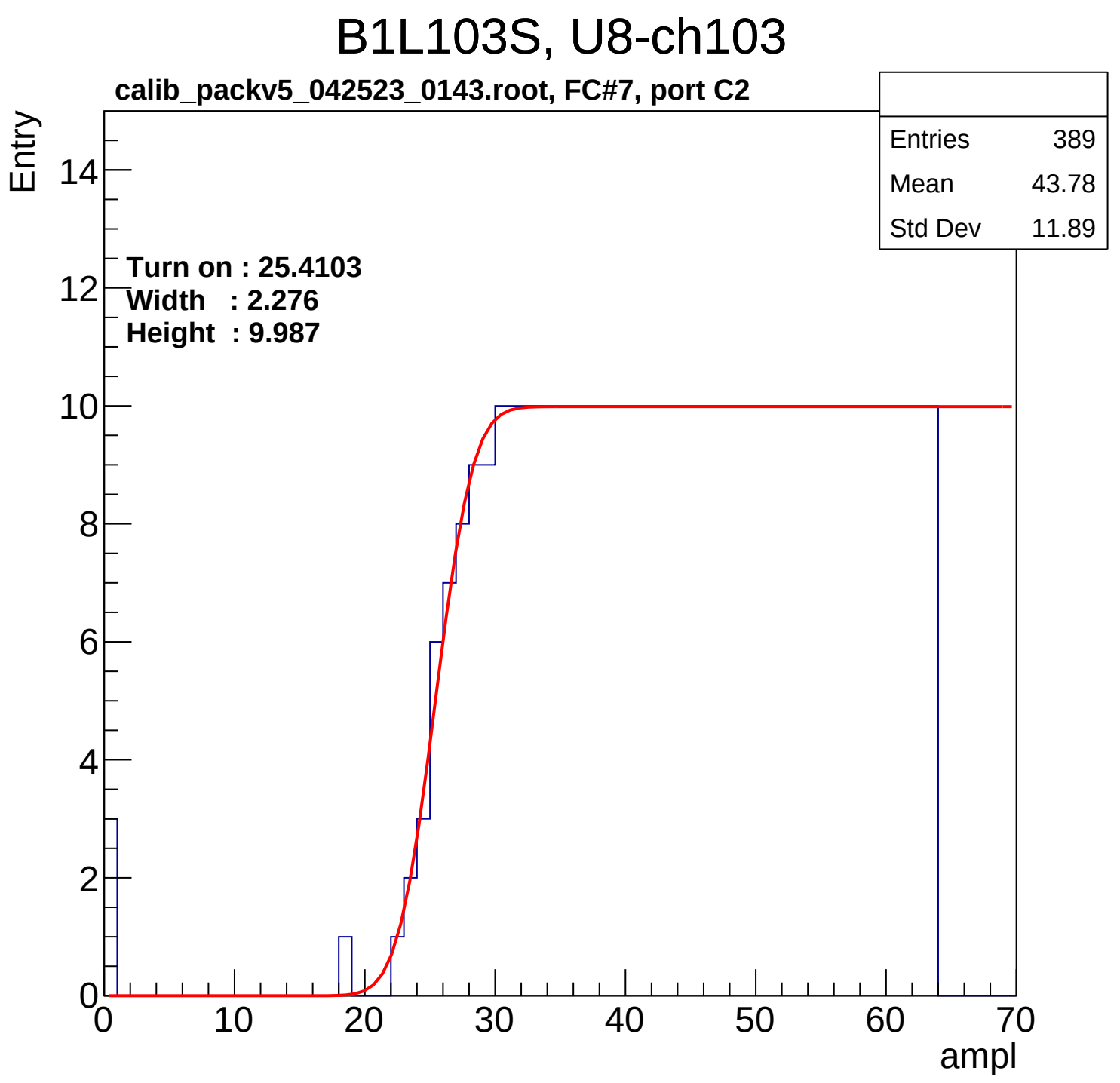
B1L103S, U8-ch103
calib_packv5_042523_0143.root, FC#7, port C2
Entries 389
Mean 43.78
Std Dev 11.89
Turn on : 25.4103
Width : 2.276
Height : 9.987
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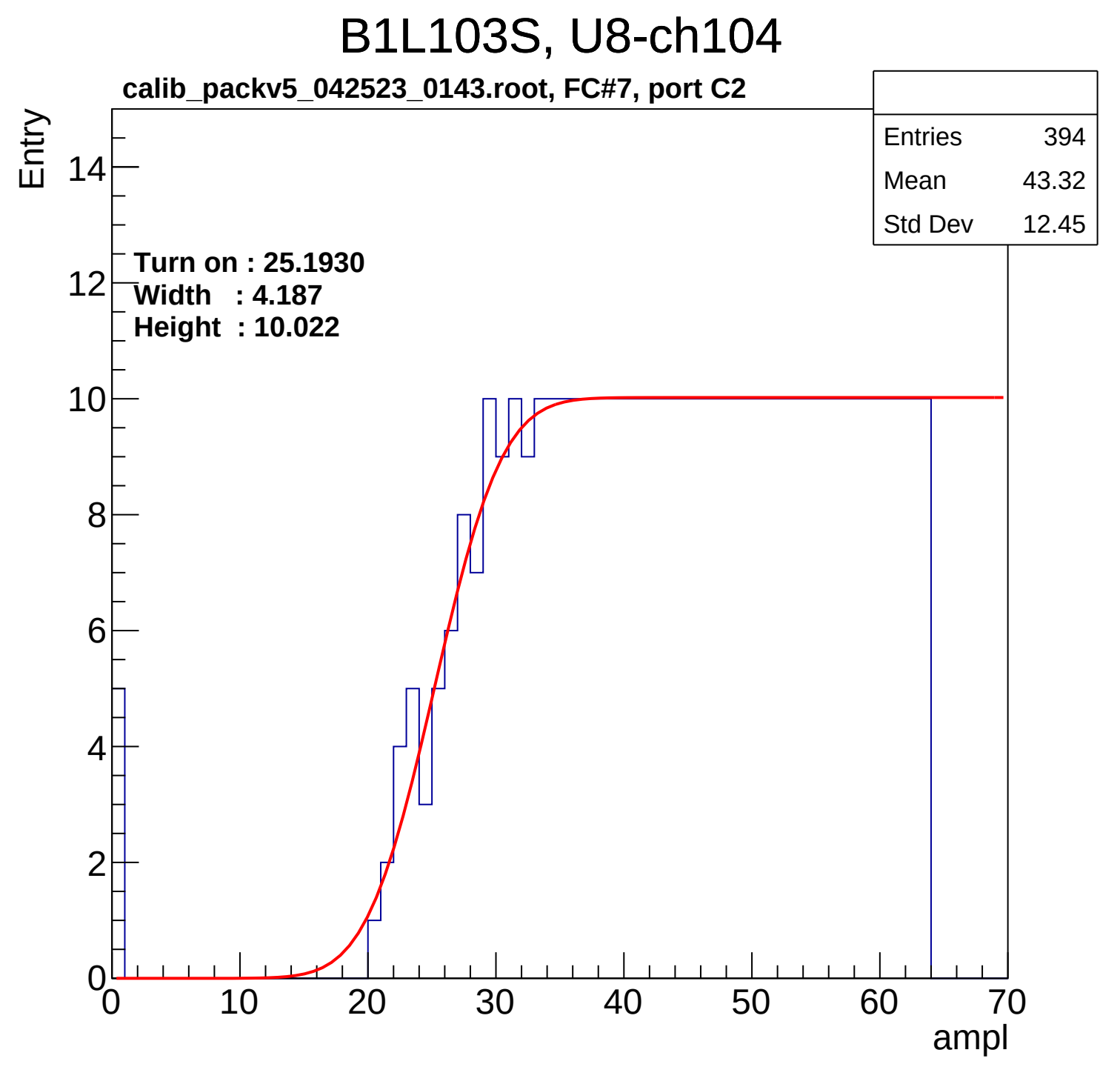
B1L103S, U8-ch104
calib_packv5_042523_0143.root, FC#7, port C2
Entries 394
Mean 43.32
Std Dev 12.45
Turn on : 25.1930
Width : 4.187
Height : 10.022
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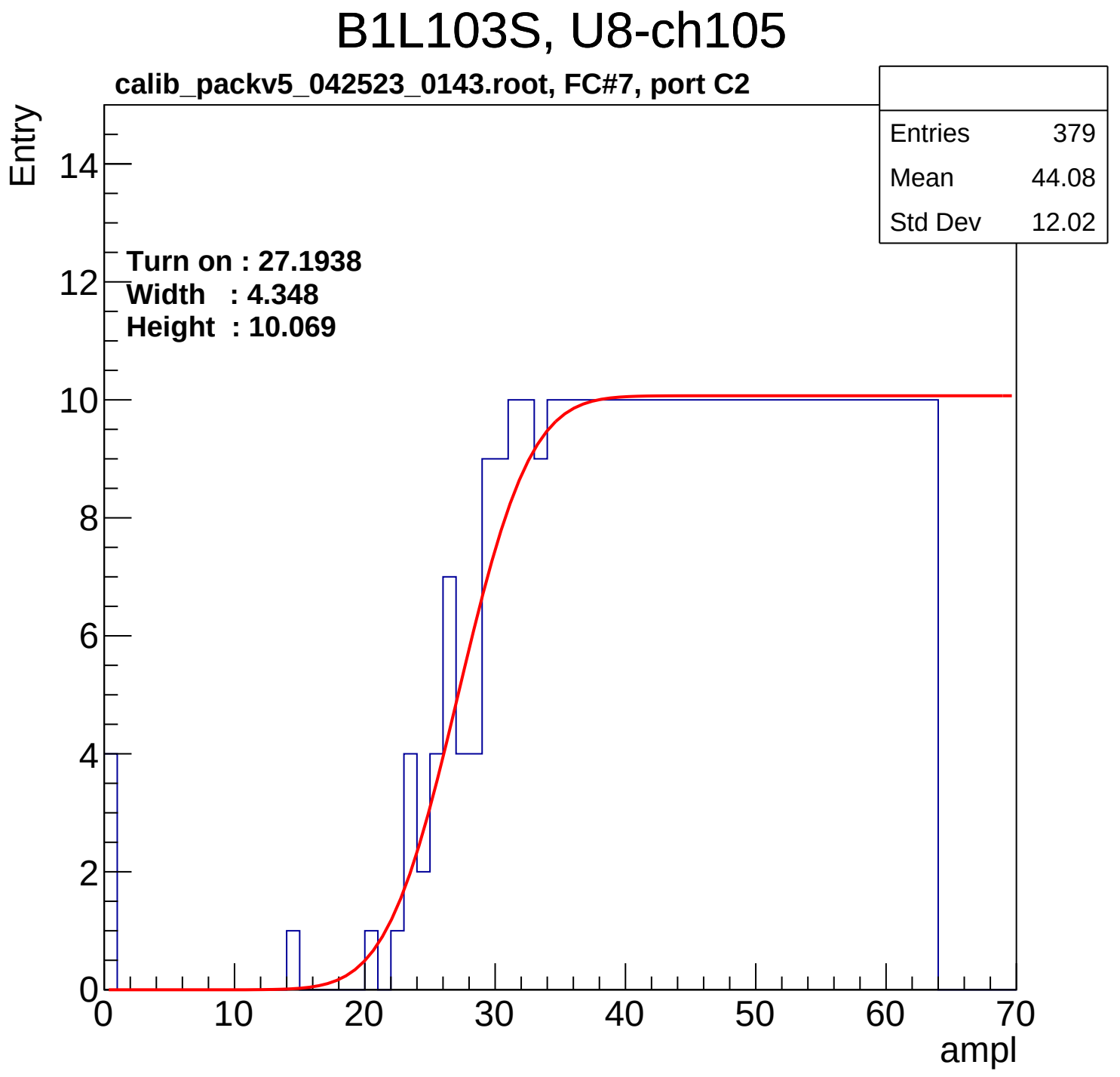
B1L103S, U8-ch105
calib_packv5_042523_0143.root, FC#7, port C2
Entries 379
Mean 44.08
Std Dev 12.02
Turn on : 27.1938
Width : 4.348
Height : 10.069
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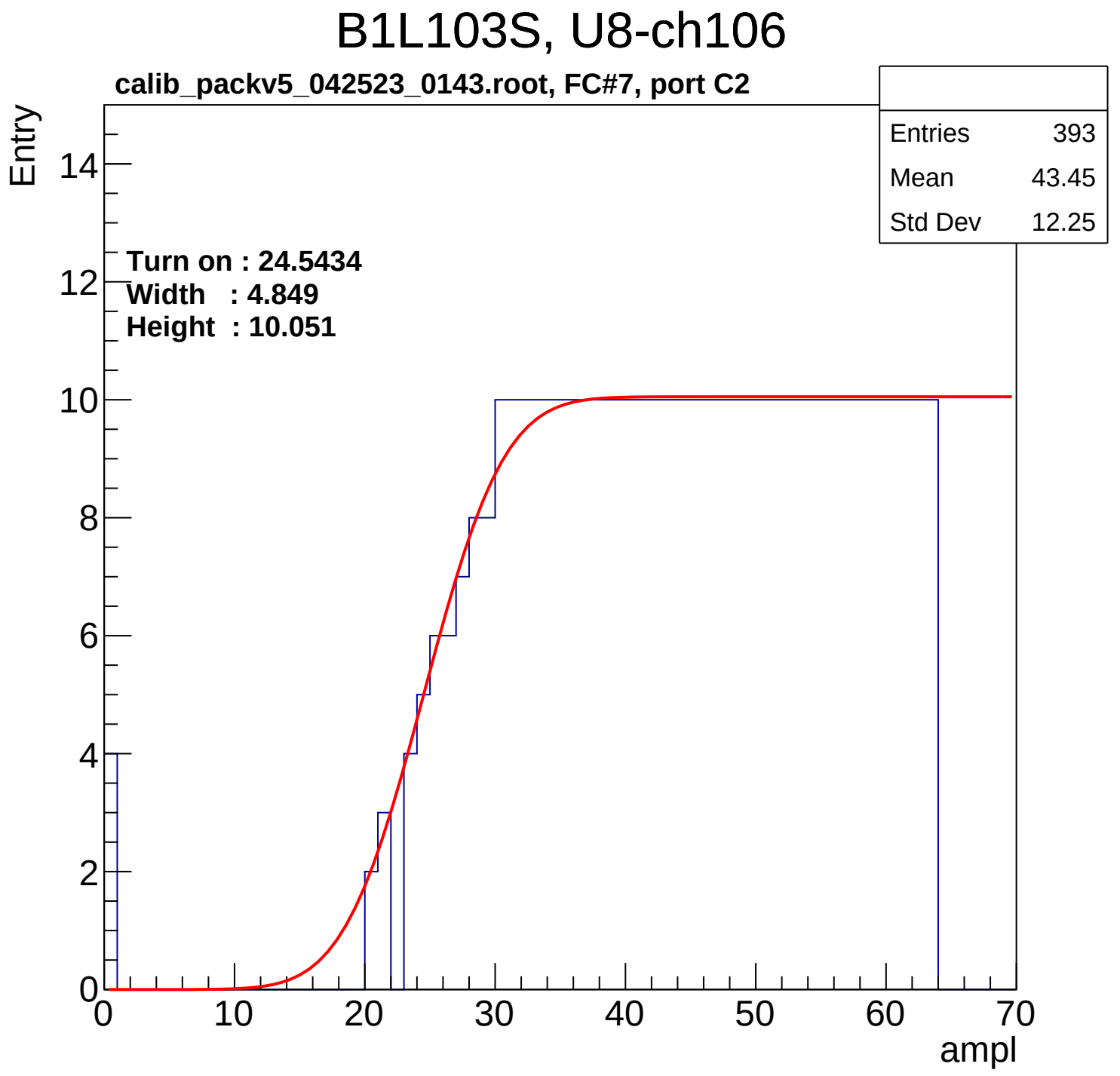
B1L103S, U8-ch106
calib_packv5_042523_0143.root, FC#7, port C2
Entries 393
Mean 43.45
Std Dev 12.25
Turn on : 24.5434
Width : 4.849
Height : 10.051
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ampl
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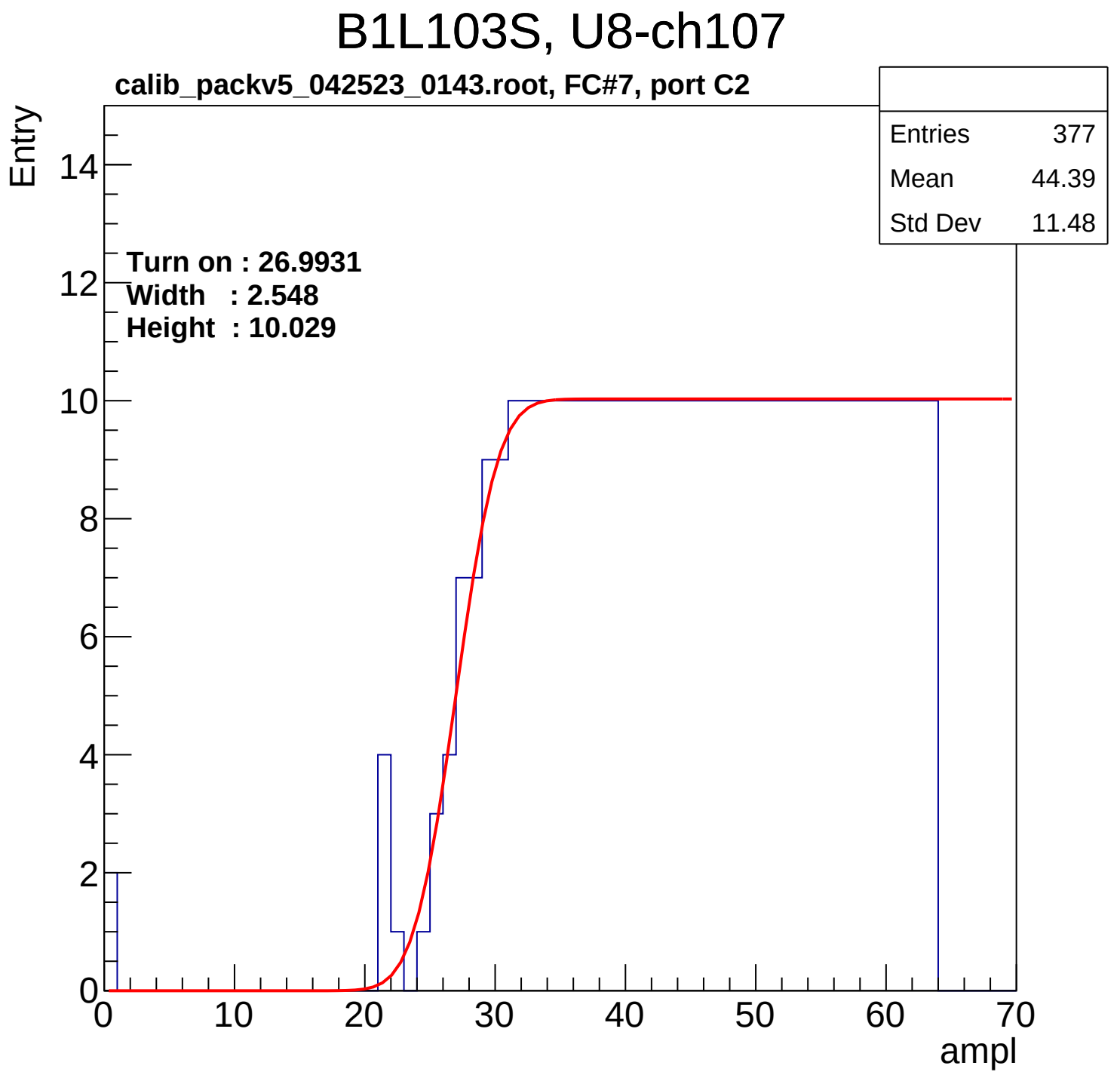
B1L103S, U8-ch107
calib_packv5_042523_0143.root, FC#7, port C2
Entries 377
Mean 44.39
Std Dev 11.48
Turn on : 26.9931
Width : 2.548
Height : 10.029
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ampl
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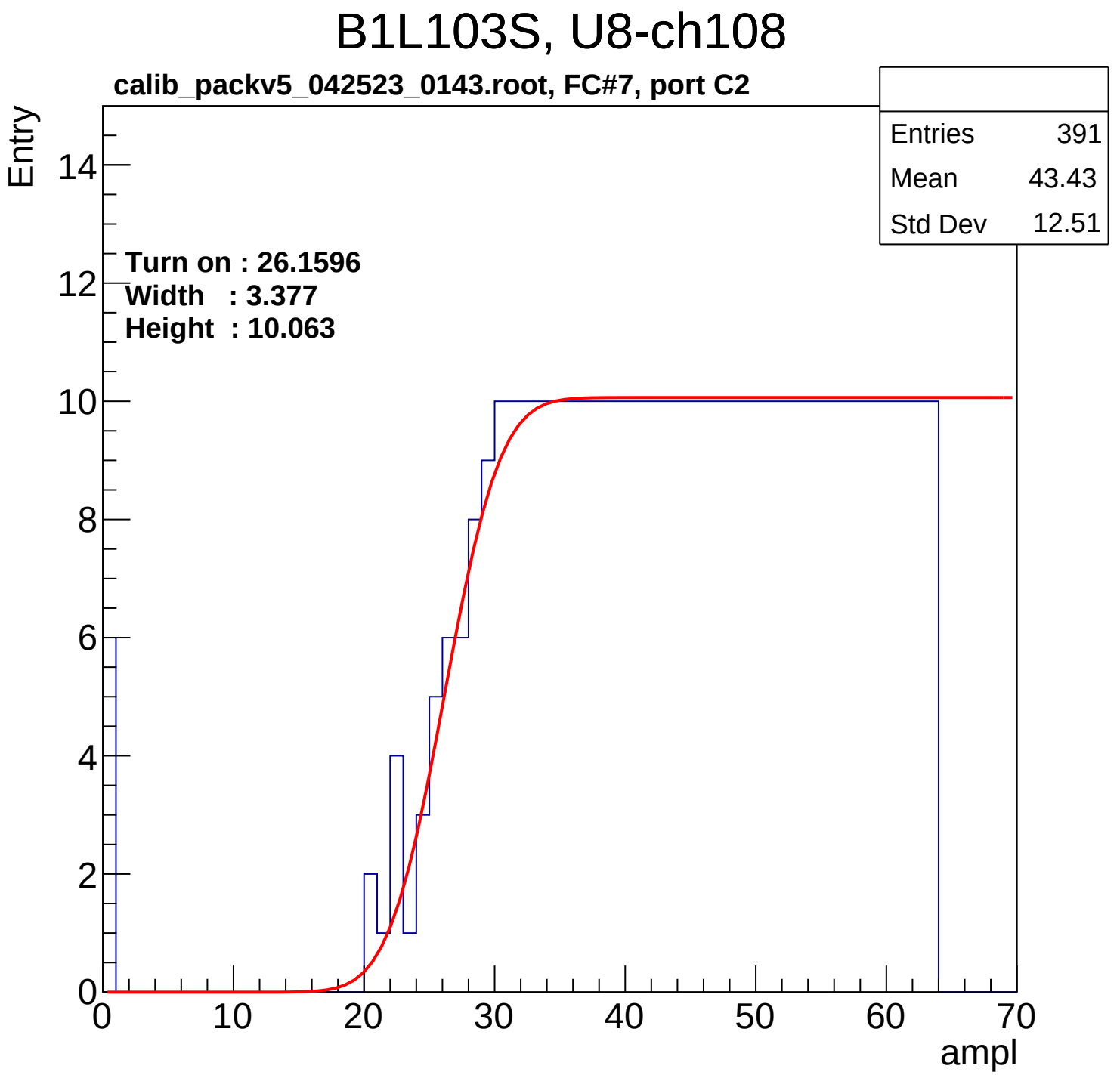
B1L103S, U8-ch108
calib_packv5_042523_0143.root, FC#7, port C2
Entries 391
Mean 43.43
Std Dev 12.51
Turn on : 26.1596
Width : 3.377
Height : 10.063
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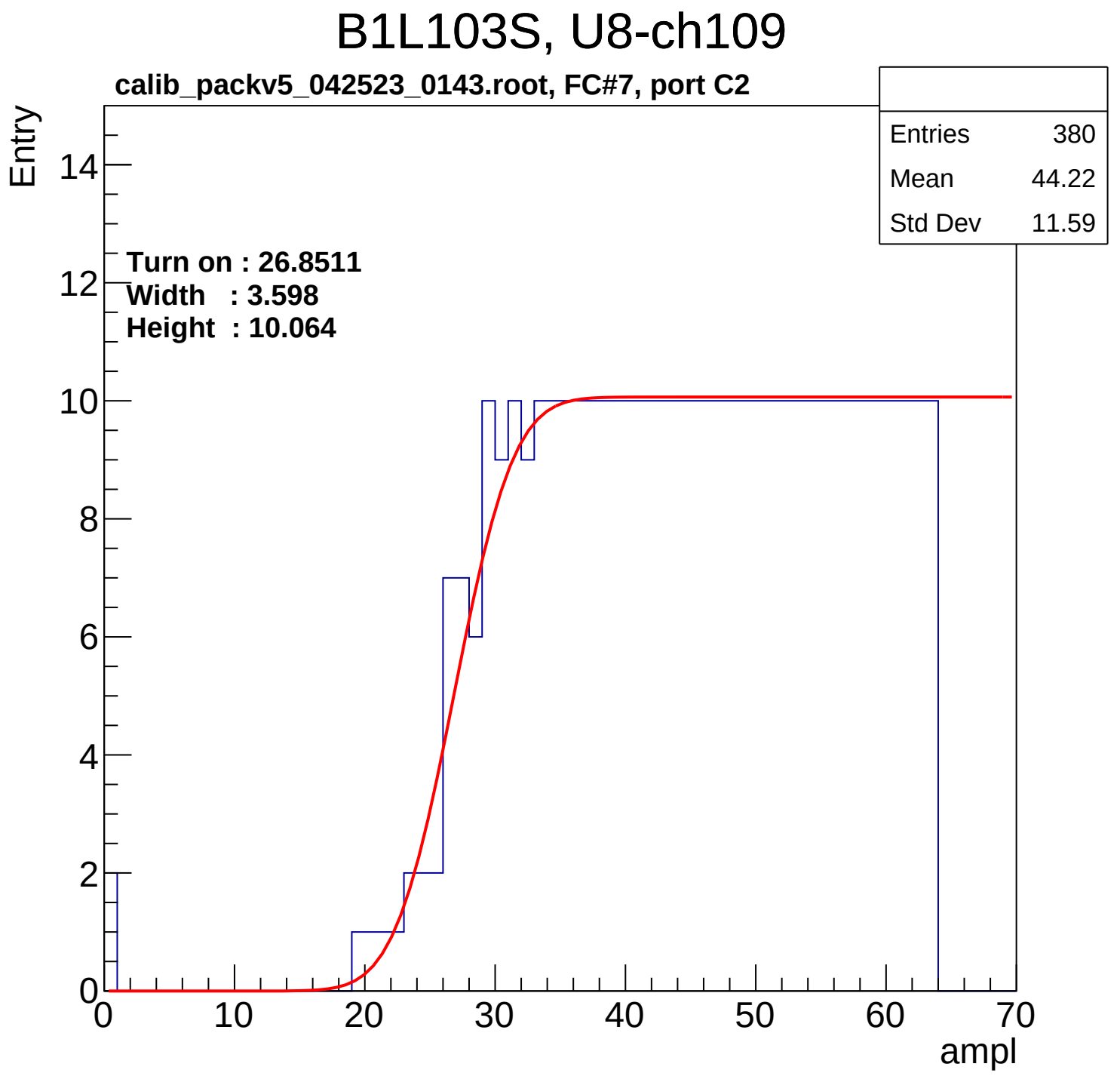
B1L103S, U8-ch109
calib_packv5_042523_0143.root, FC#7, port C2
Entries 380
Mean 44.22
Std Dev 11.59
Turn on : 26.8511
Width : 3.598
Height : 10.064
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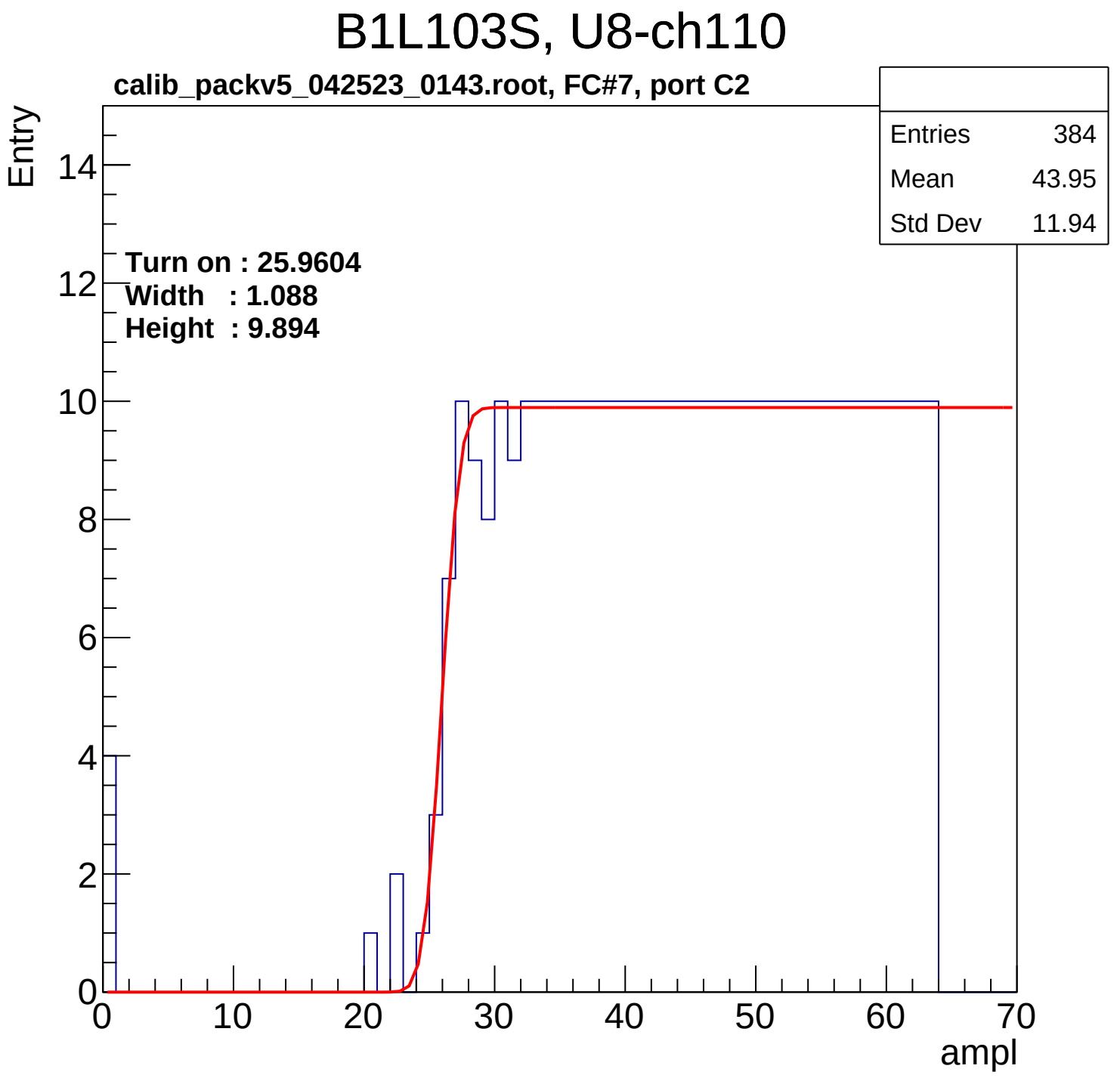
B1L103S, U8-ch110
calib_packv5_042523_0143.root, FC#7, port C2
Entries 384
Mean 43.95
Std Dev 11.94
Turn on : 25.9604
Width : 1.088
Height : 9.894
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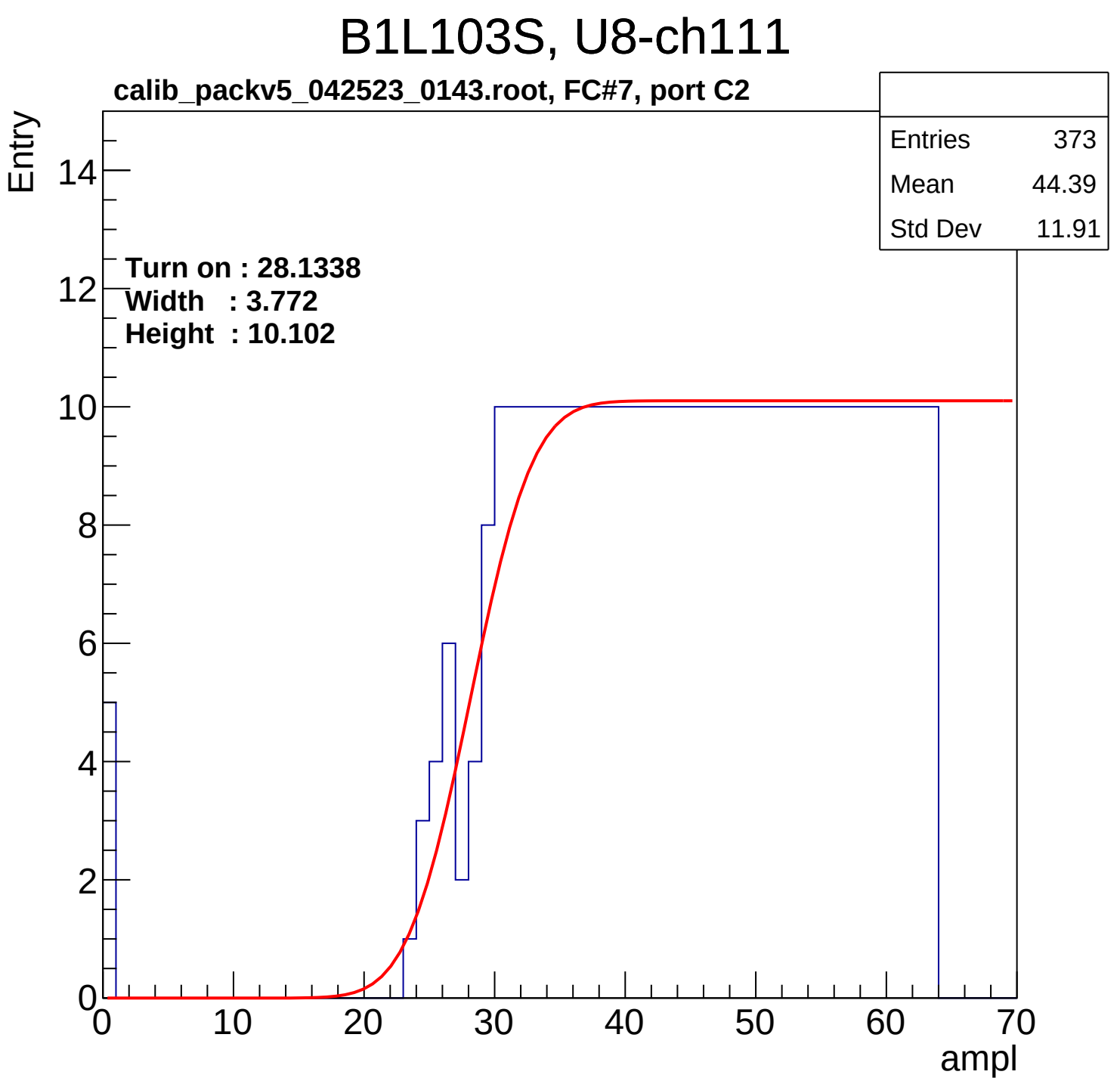
B1L103S, U8-ch111
calib_packv5_042523_0143.root, FC#7, port C2
Entries 373
Mean 44.39
Std Dev 11.91
Turn on : 28.1338
Width : 3.772
Height : 10.102
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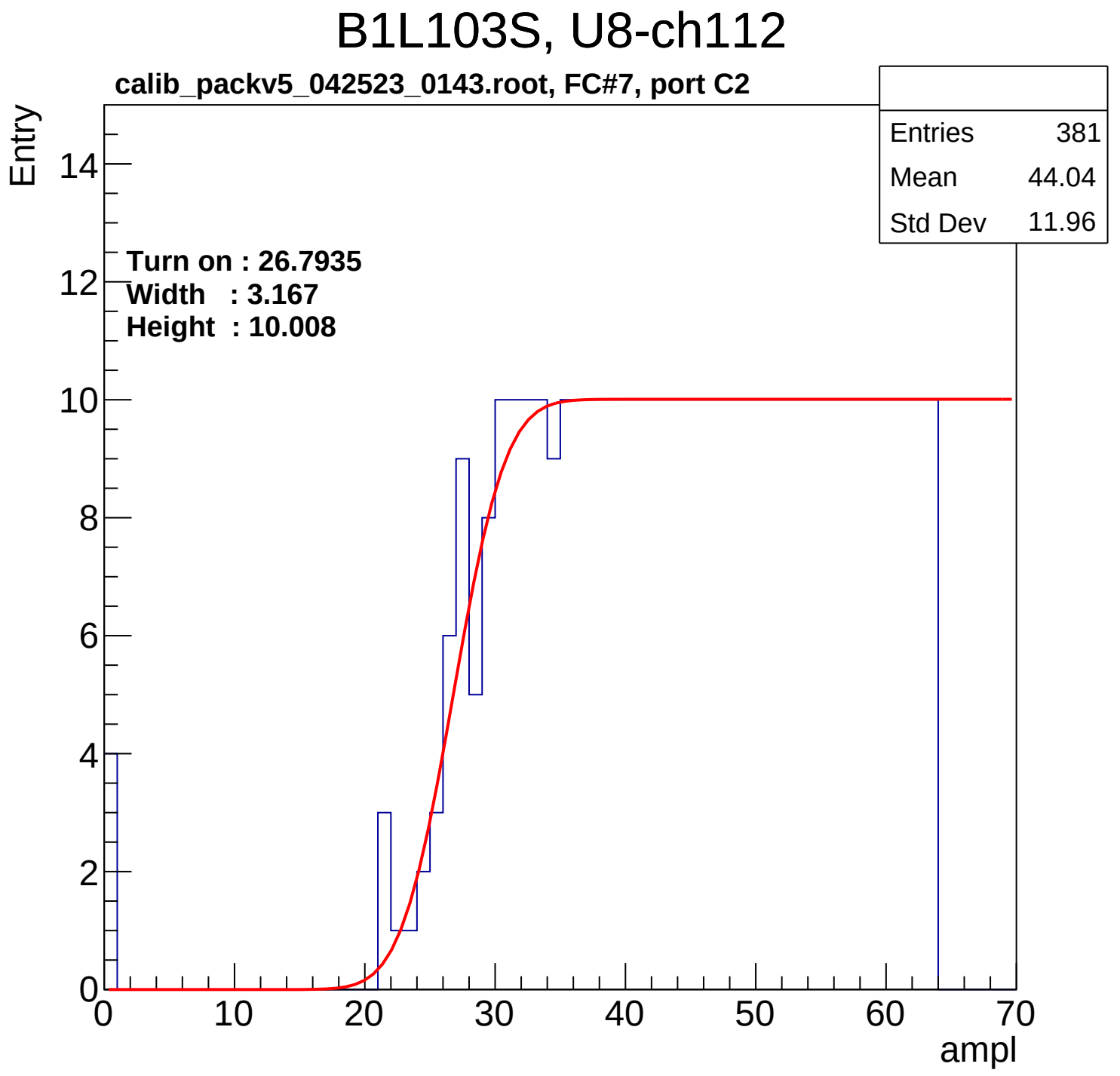
B1L103S, U8-ch112
calib_packv5_042523_0143.root, FC#7, port C2
Entries 381
Mean 44.04
Std Dev 11.96
Turn on : 26.7935
Width : 3.167
Height : 10.008
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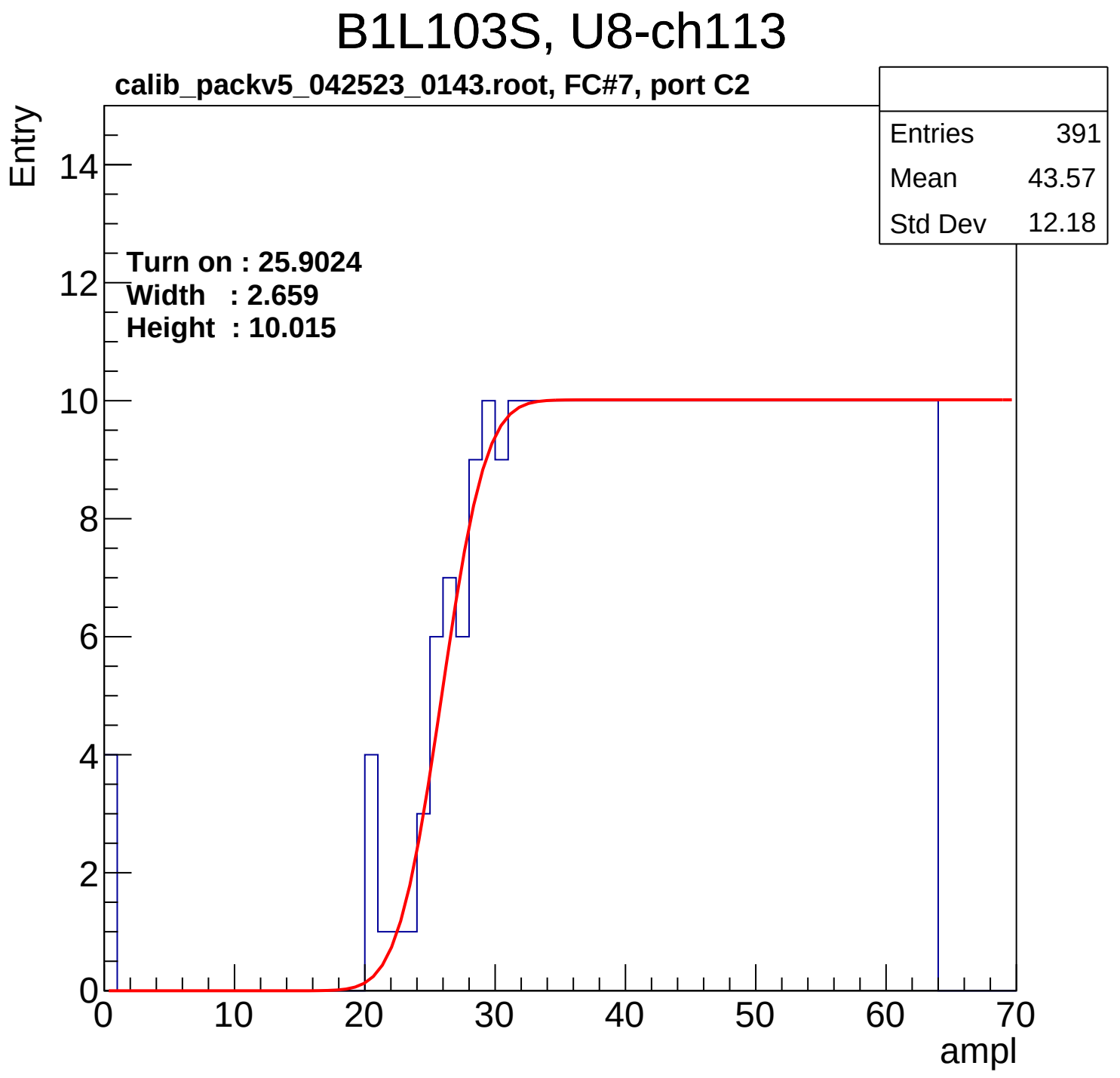
B1L103S, U8-ch113
calib_packv5_042523_0143.root, FC#7, port C2
Entries 391
Mean 43.57
Std Dev 12.18
Turn on : 25.9024
Width : 2.659
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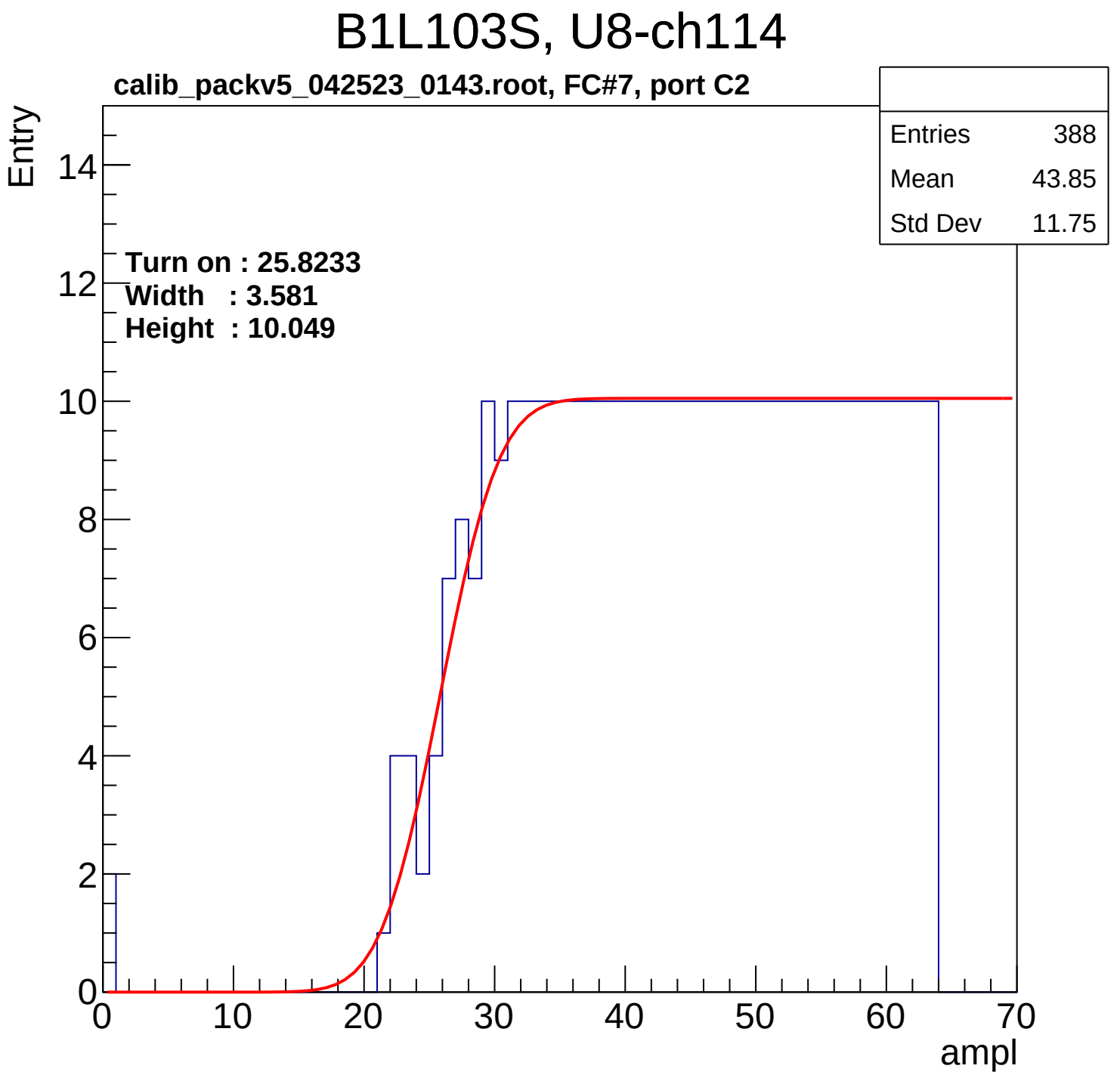
B1L103S, U8-ch114
calib_packv5_042523_0143.root, FC#7, port C2
Entries 388
Mean 43.85
Std Dev 11.75
Turn on : 25.8233
Width : 3.581
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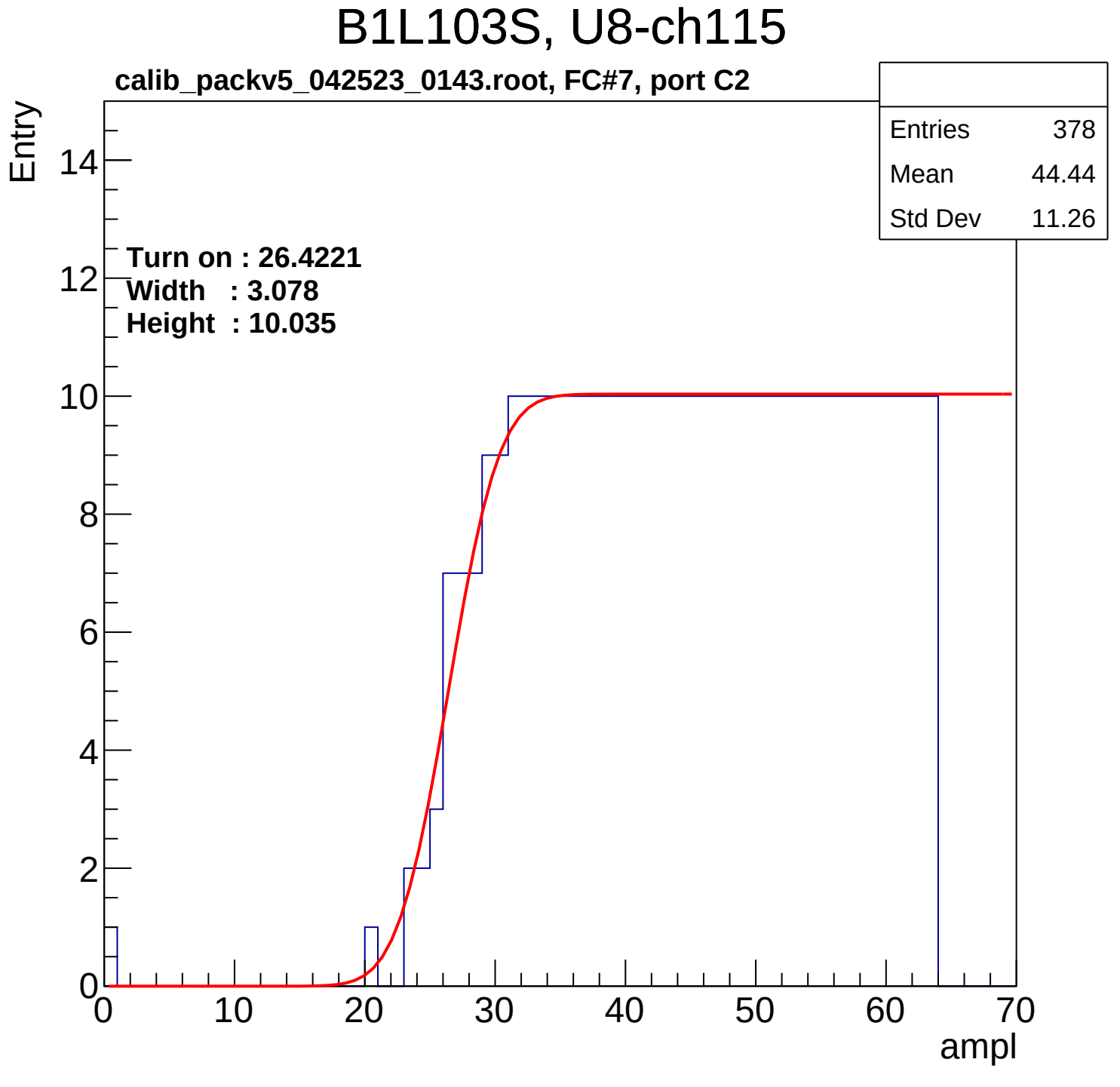
B1L103S, U8-ch115
calib_packv5_042523_0143.root, FC#7, port C2
Entries 378
Mean 44.44
Std Dev 11.26
Turn on : 26.4221
Width : 3.078
Height : 10.035
Entry
ampl
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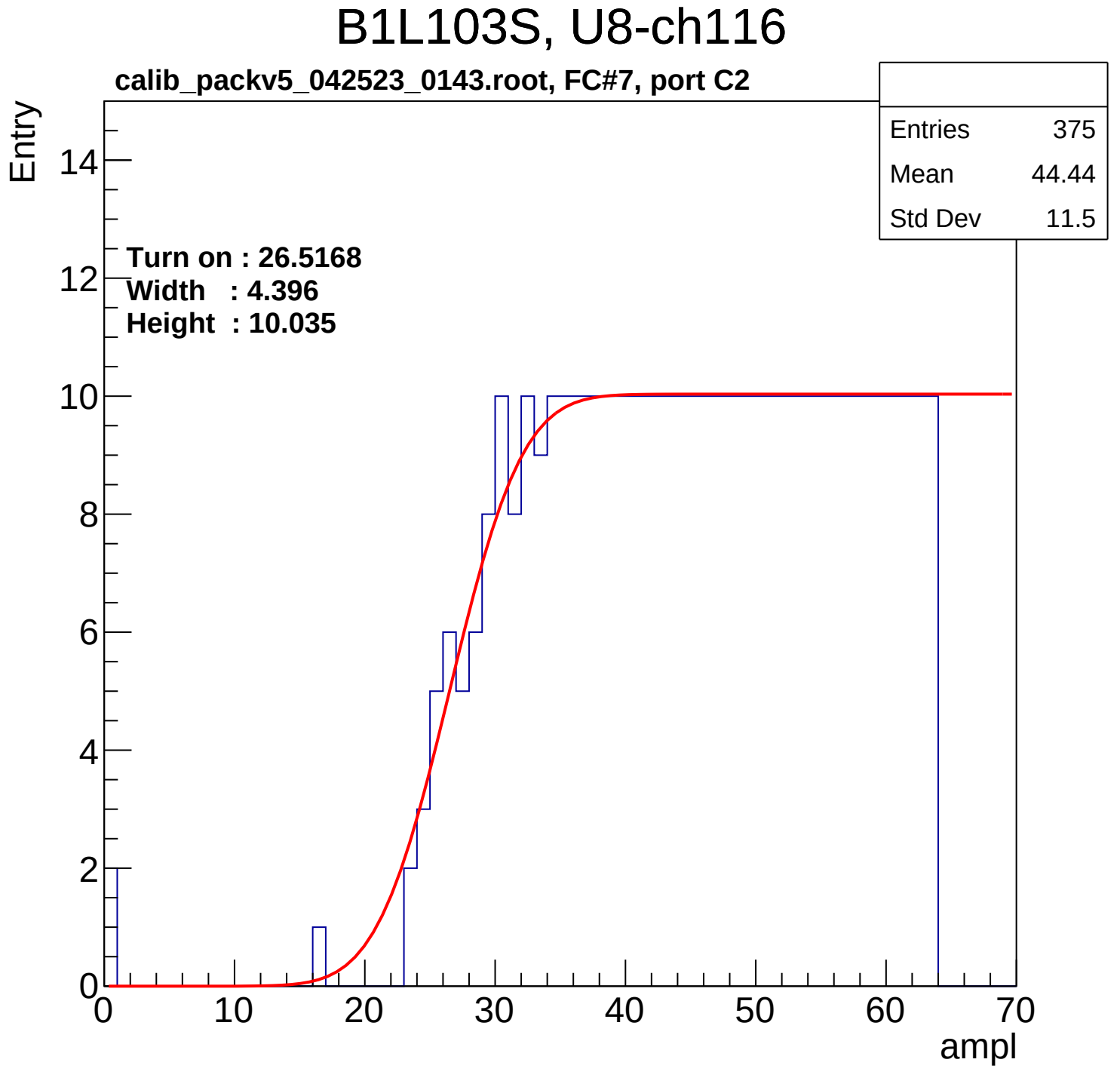
B1L103S, U8-ch116
calib_packv5_042523_0143.root, FC#7, port C2
Entries 375
Mean 44.44
Std Dev 11.5
Turn on : 26.5168
Width : 4.396
Height : 10.035
Entry
ampl
0
2
4
6
8
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12
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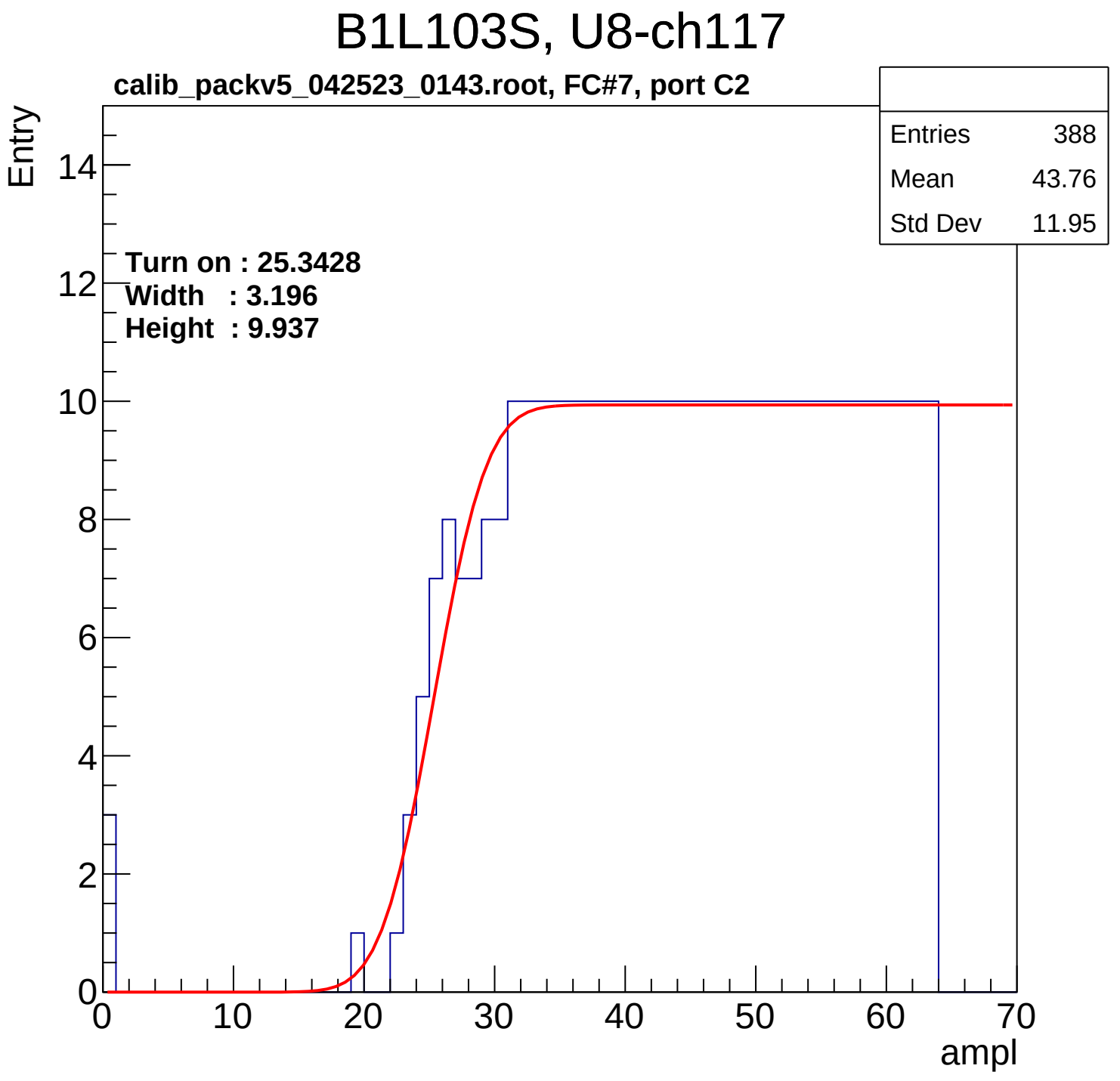
B1L103S, U8-ch117
calib_packv5_042523_0143.root, FC#7, port C2
Entries 388
Mean 43.76
Std Dev 11.95
Turn on : 25.3428
Width : 3.196
Height : 9.937
Entry
ampl
0
2
4
6
8
10
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20
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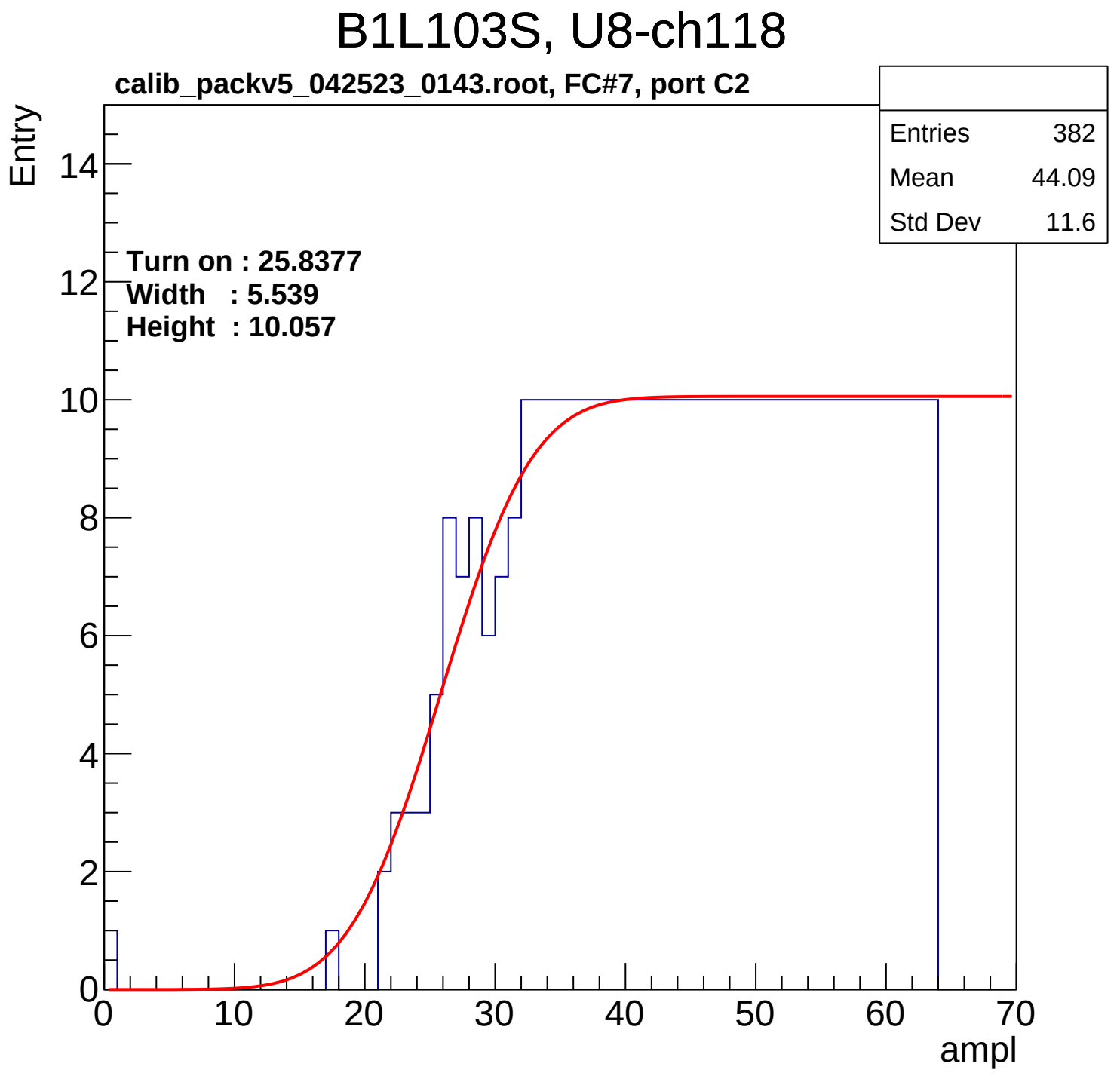
B1L103S, U8-ch118
calib_packv5_042523_0143.root, FC#7, port C2
Entries 382
Mean 44.09
Std Dev 11.6
Turn on : 25.8377
Width : 5.539
Height : 10.057
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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40
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60
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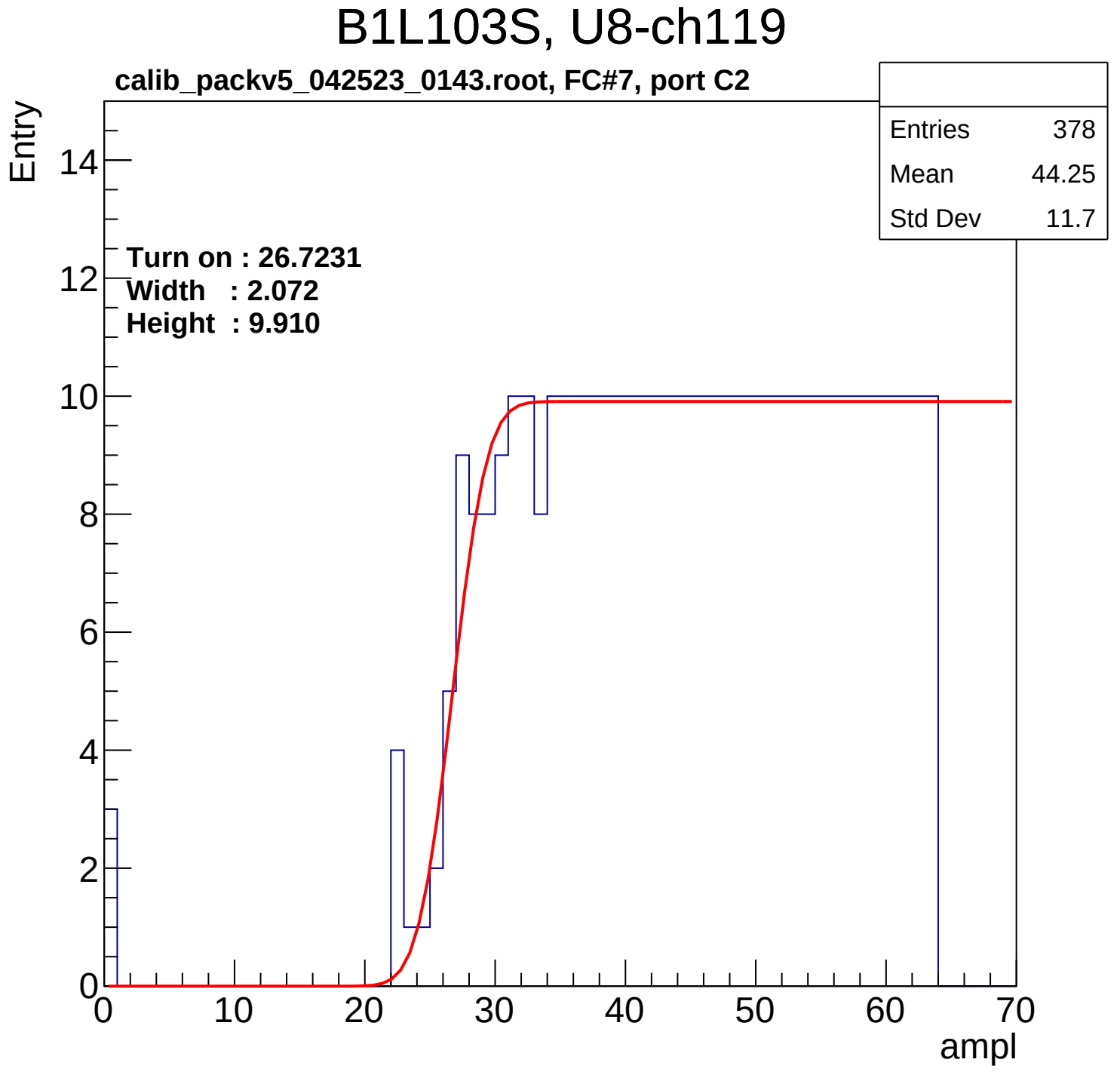
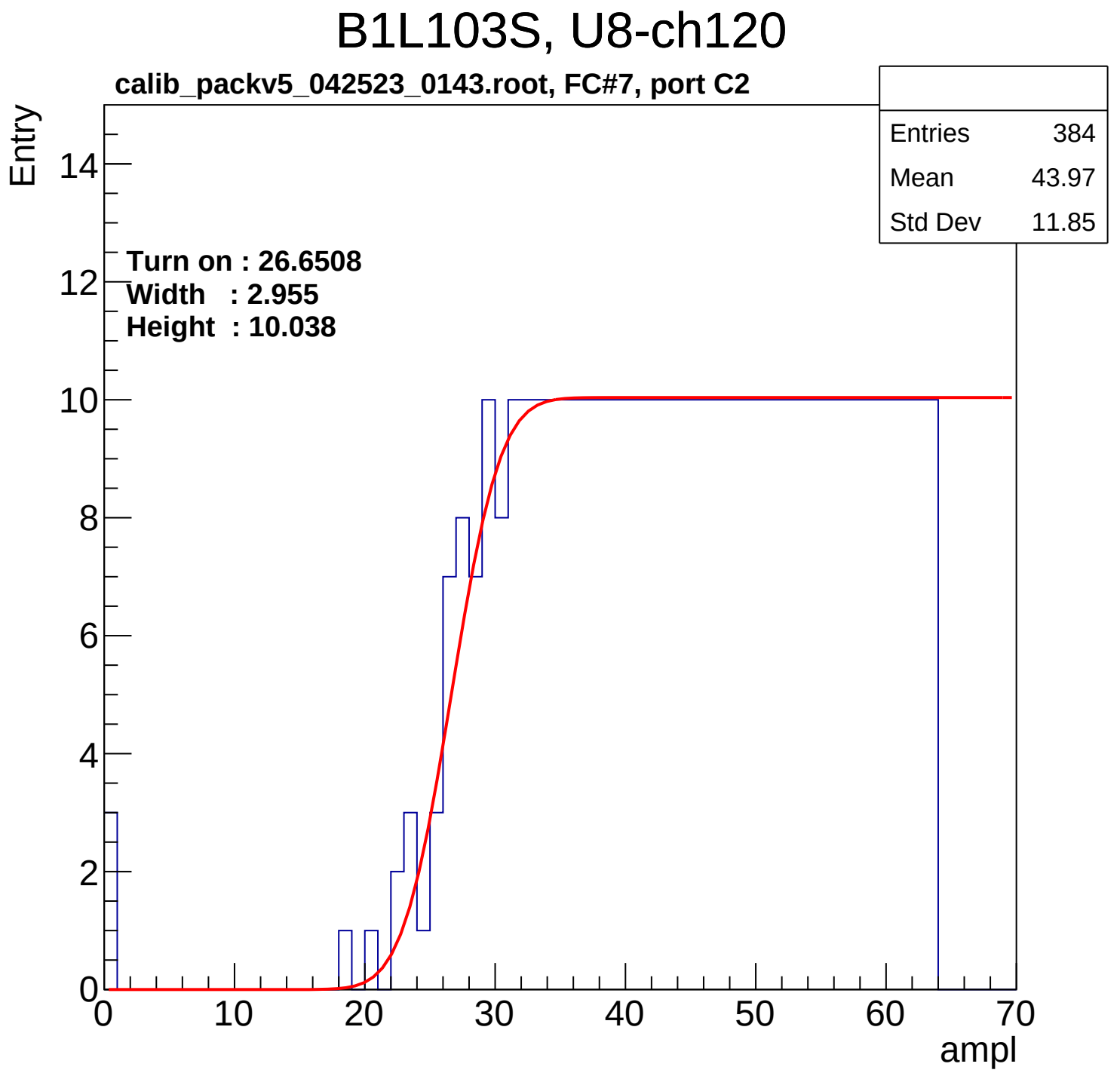

B1L103S, U8-ch119
calib_packv5_042523_0143.root, FC#7, port C2
Entries 378
Mean 44.25
Std Dev 11.7
Turn on : 26.7231
Width : 2.072
Height : 9.910
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U8-ch120
calib_packv5_042523_0143.root, FC#7, port C2
Entries 384
Mean 43.97
Std Dev 11.85
Turn on : 26.6508
Width : 2.955
Height : 10.038
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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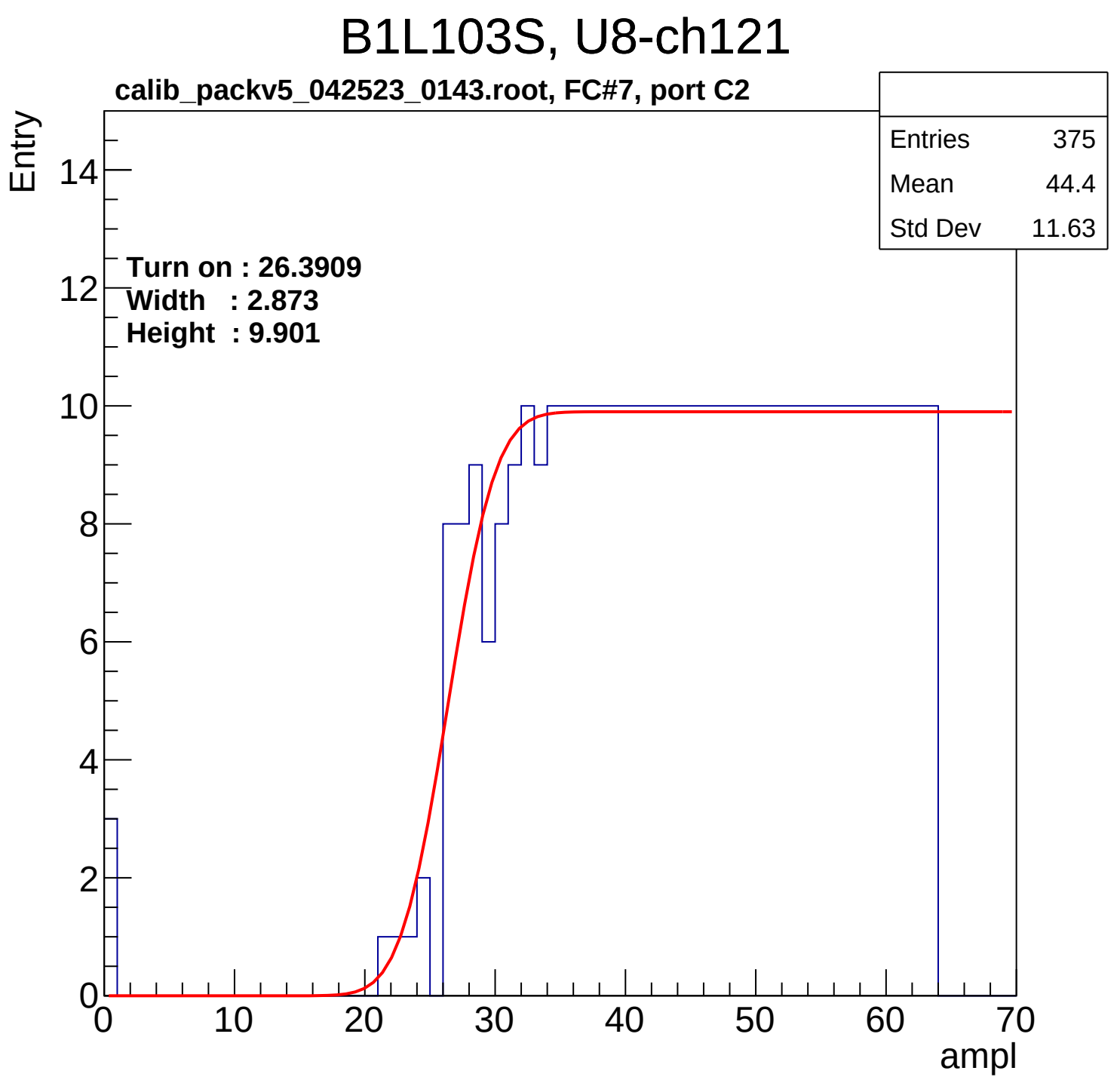
B1L103S, U8-ch121
calib_packv5_042523_0143.root, FC#7, port C2
Entries 375
Mean 44.4
Std Dev 11.63
Turn on : 26.3909
Width : 2.873
Height : 9.901
Entry
ampl
0
2
4
6
8
10
12
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0
10
20
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40
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60
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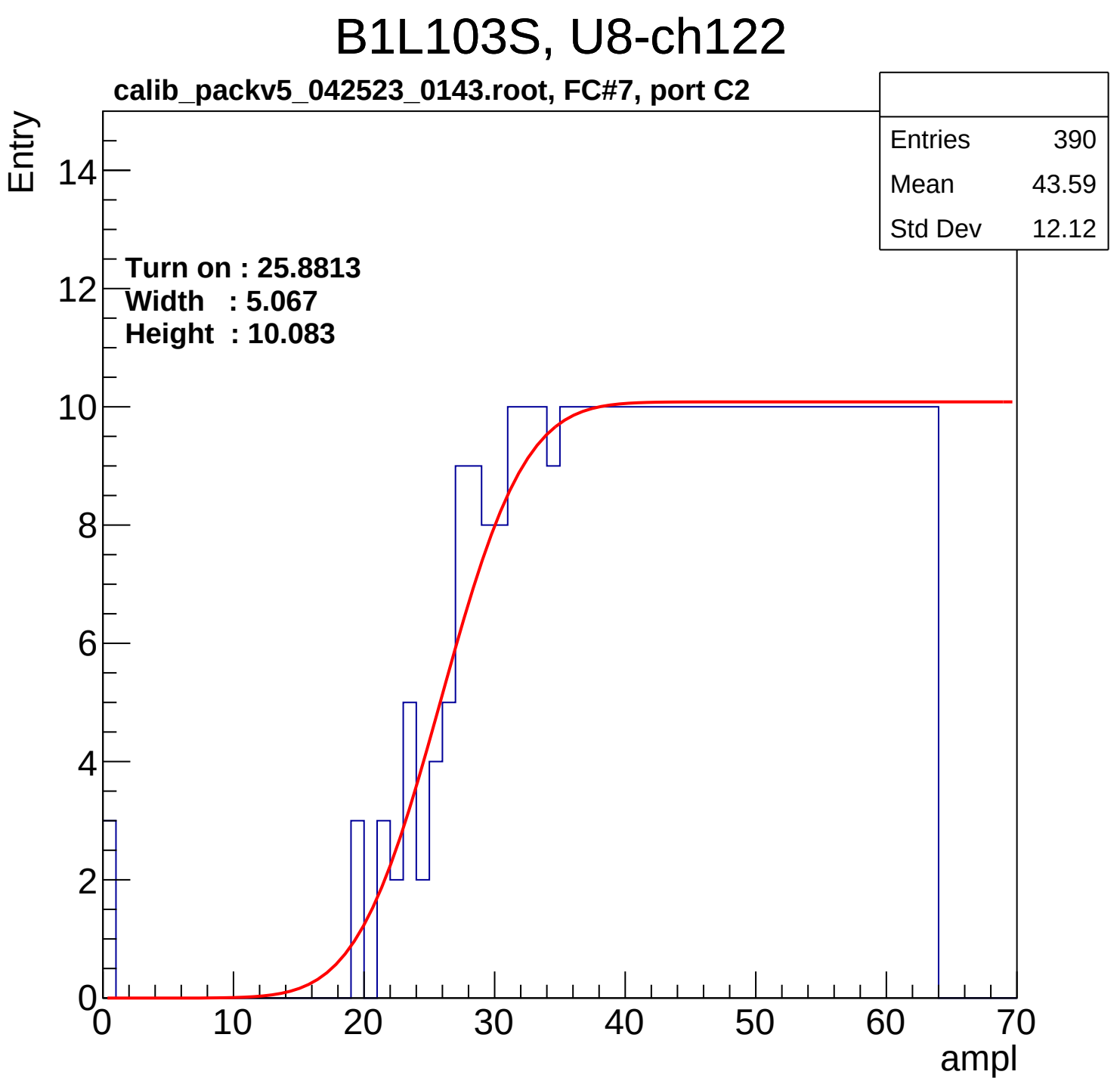
B1L103S, U8-ch122
calib_packv5_042523_0143.root, FC#7, port C2
Entries 390
Mean 43.59
Std Dev 12.12
Turn on : 25.8813
Width : 5.067
Height : 10.083
Entry
ampl
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2
4
6
8
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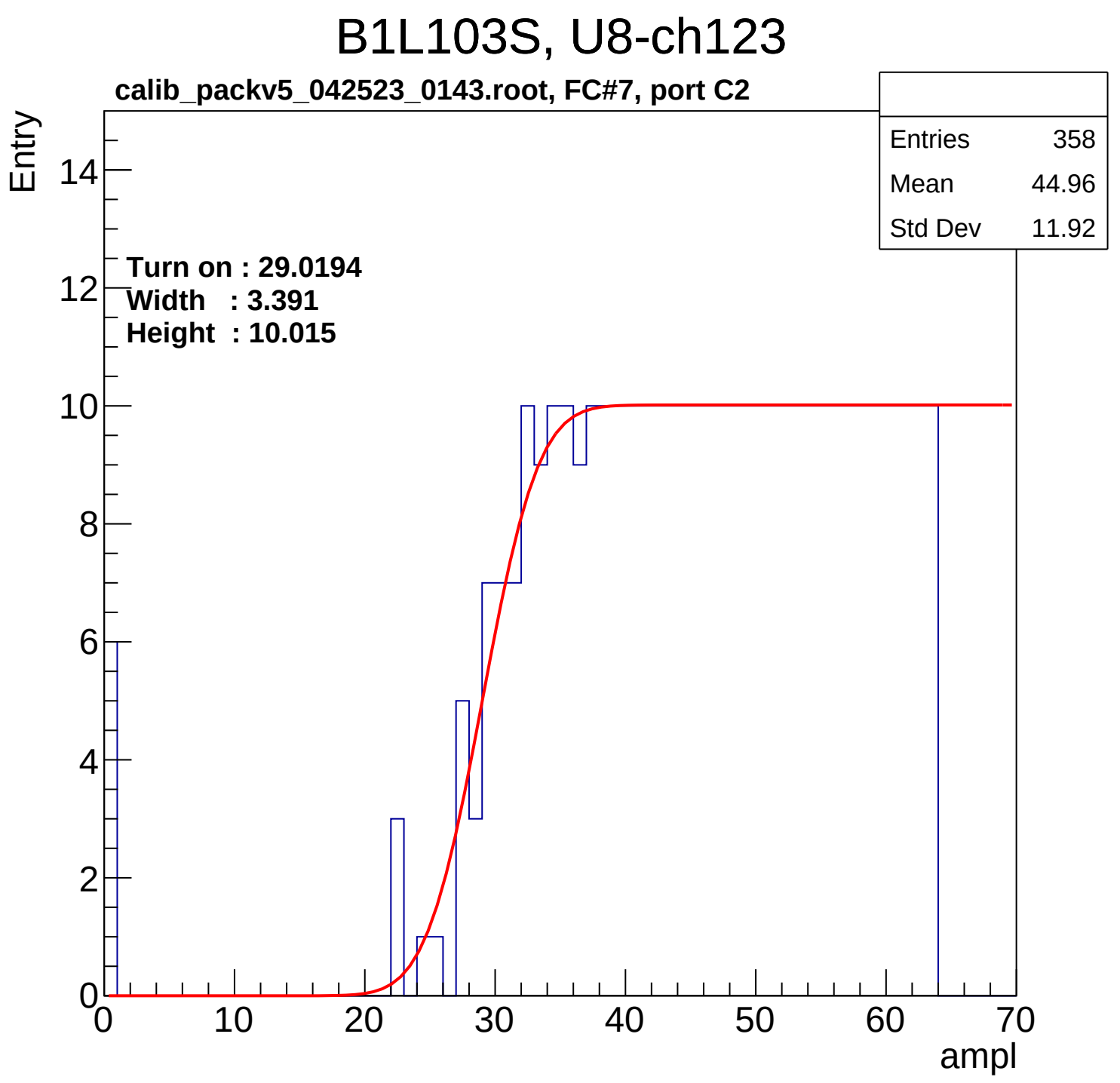
B1L103S, U8-ch123
calib_packv5_042523_0143.root, FC#7, port C2
Entries 358
Mean 44.96
Std Dev 11.92
Turn on : 29.0194
Width : 3.391
Height : 10.015
Entry
ampl
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6
8
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10
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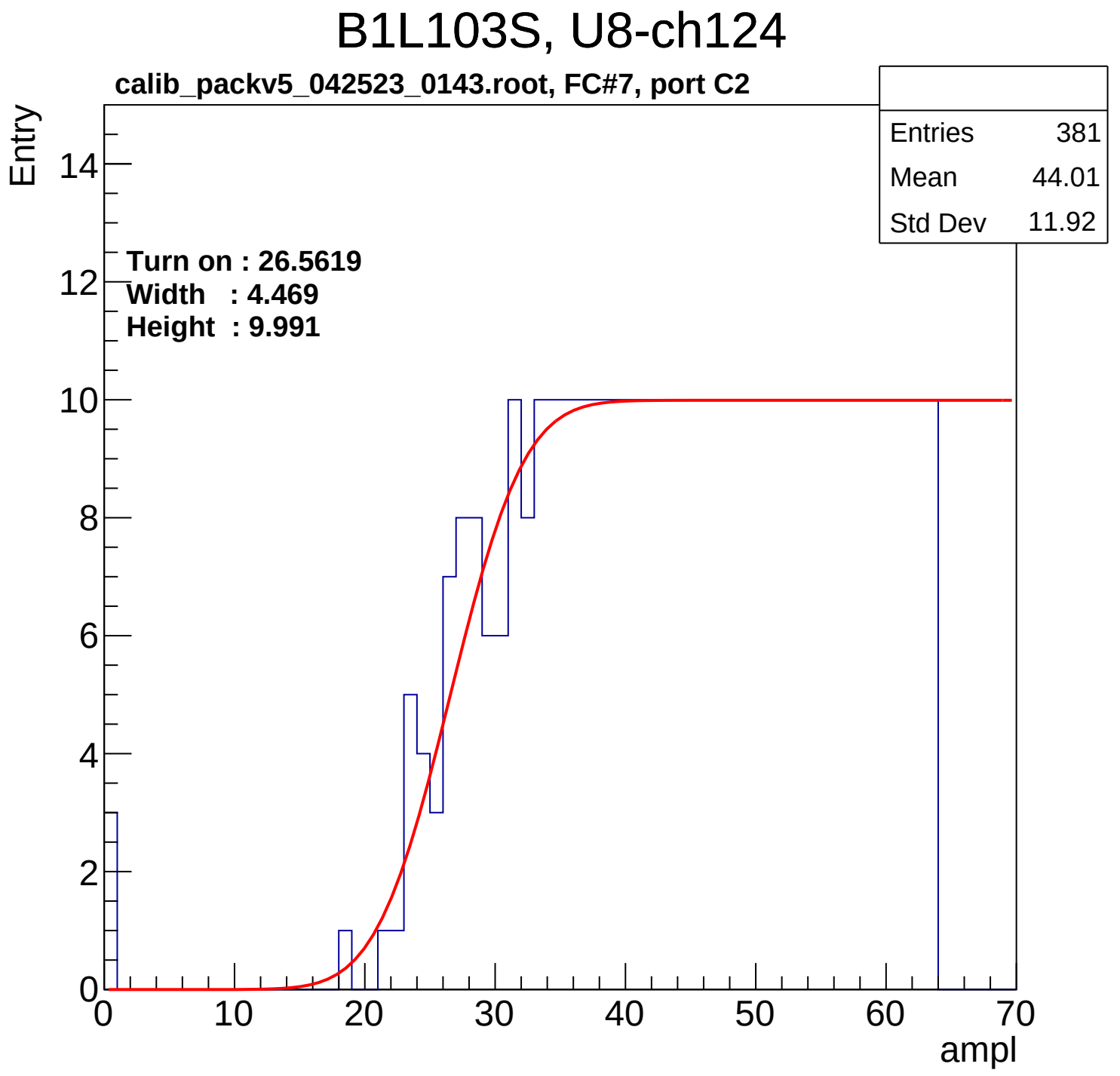
B1L103S, U8-ch124
calib_packv5_042523_0143.root, FC#7, port C2
Entries 381
Mean 44.01
Std Dev 11.92
Turn on : 26.5619
Width : 4.469
Height : 9.991
Entry
ampl
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2
4
6
8
10
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0
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20
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40
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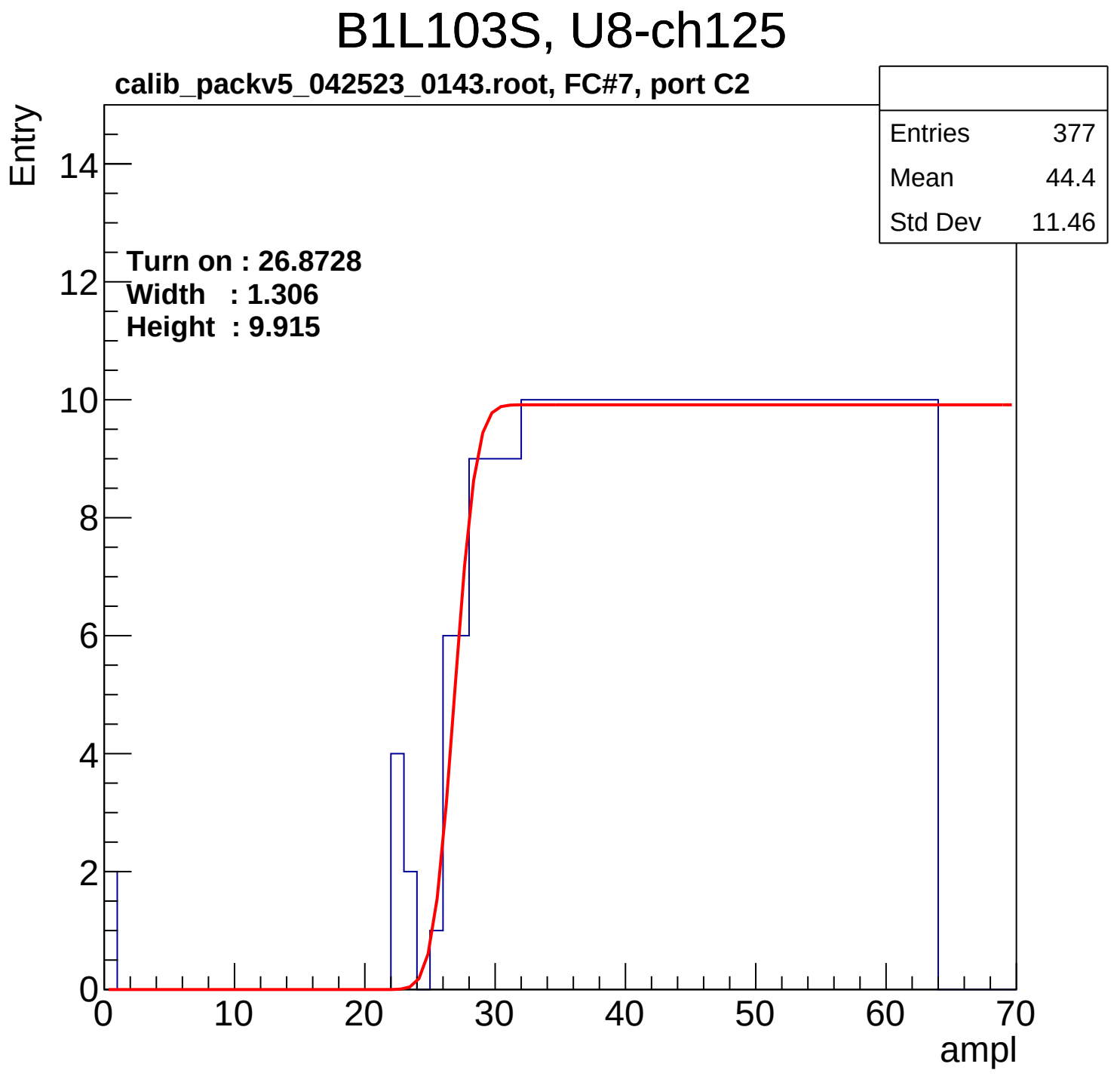
60
70


B1L103S, U8-ch125
calib_packv5_042523_0143.root, FC#7, port C2
Entries 377
Mean 44.4
Std Dev 11.46
Turn on : 26.8728
Width : 1.306
Height : 9.915
Entry
ampl
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2
4
6
8
10
12
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0
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20
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40
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60
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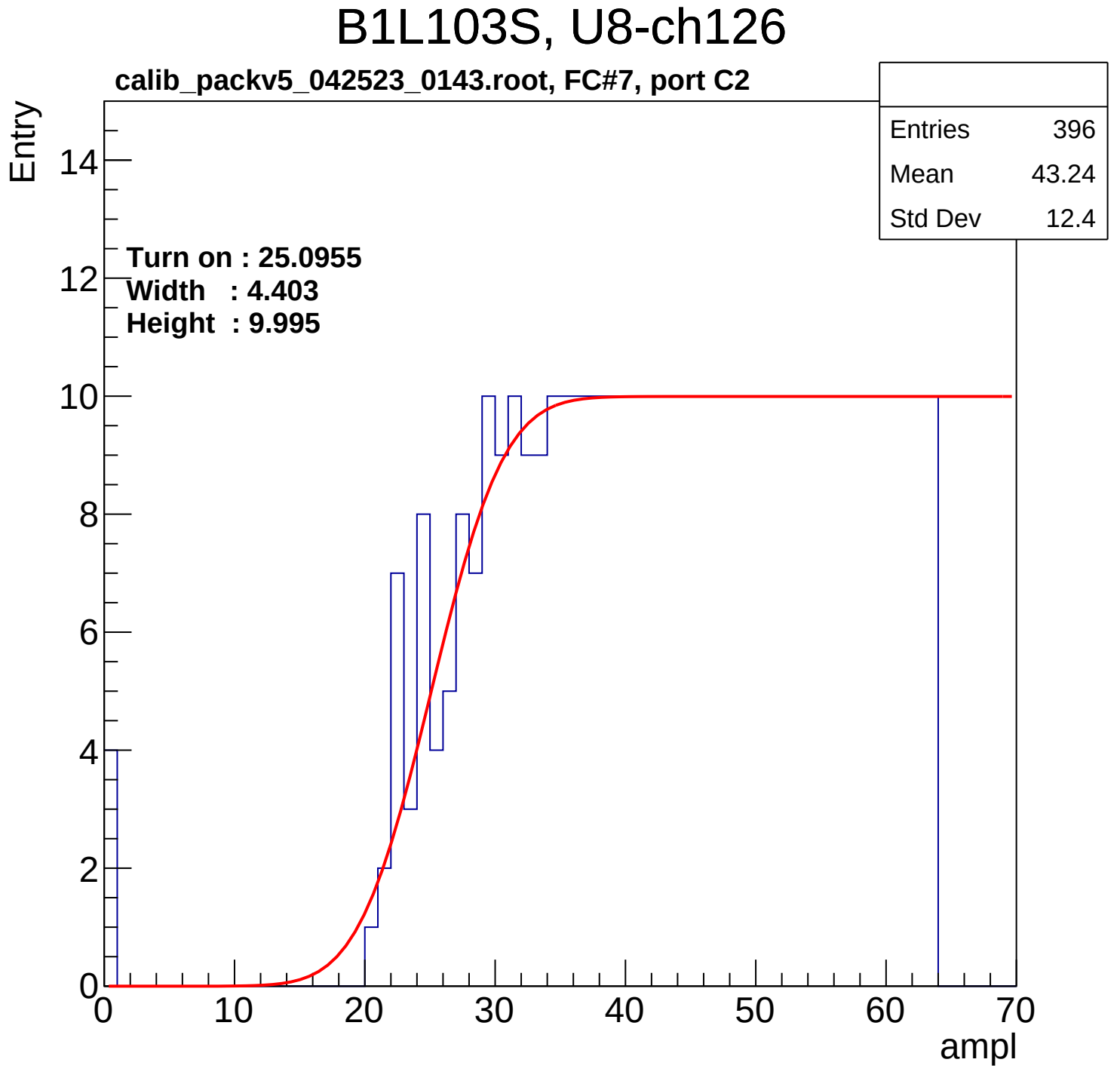
B1L103S, U8-ch126
calib_packv5_042523_0143.root, FC#7, port C2
Entries 396
Mean 43.24
Std Dev 12.4
Turn on : 25.0955
Width : 4.403
Height : 9.995
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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60
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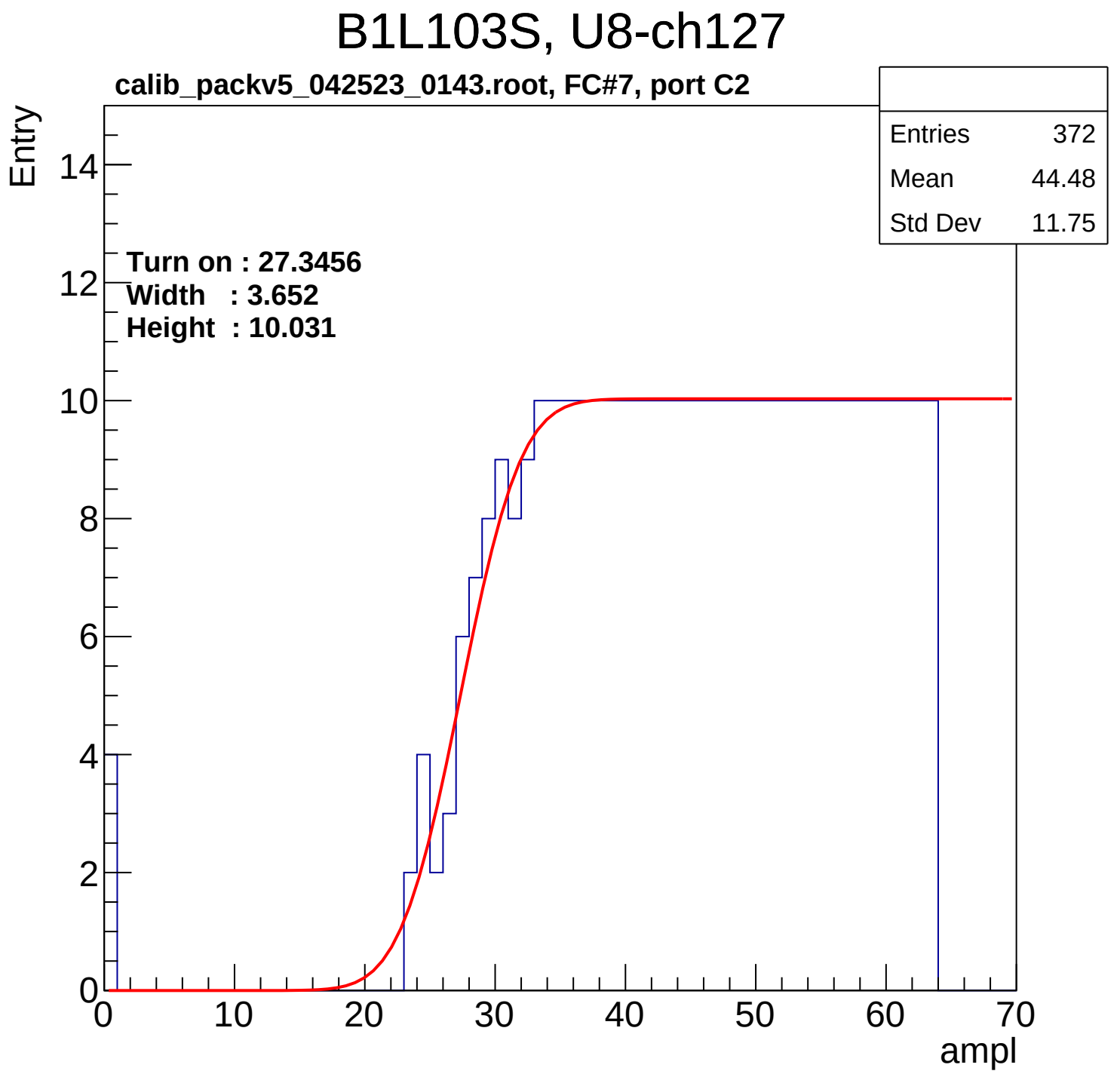
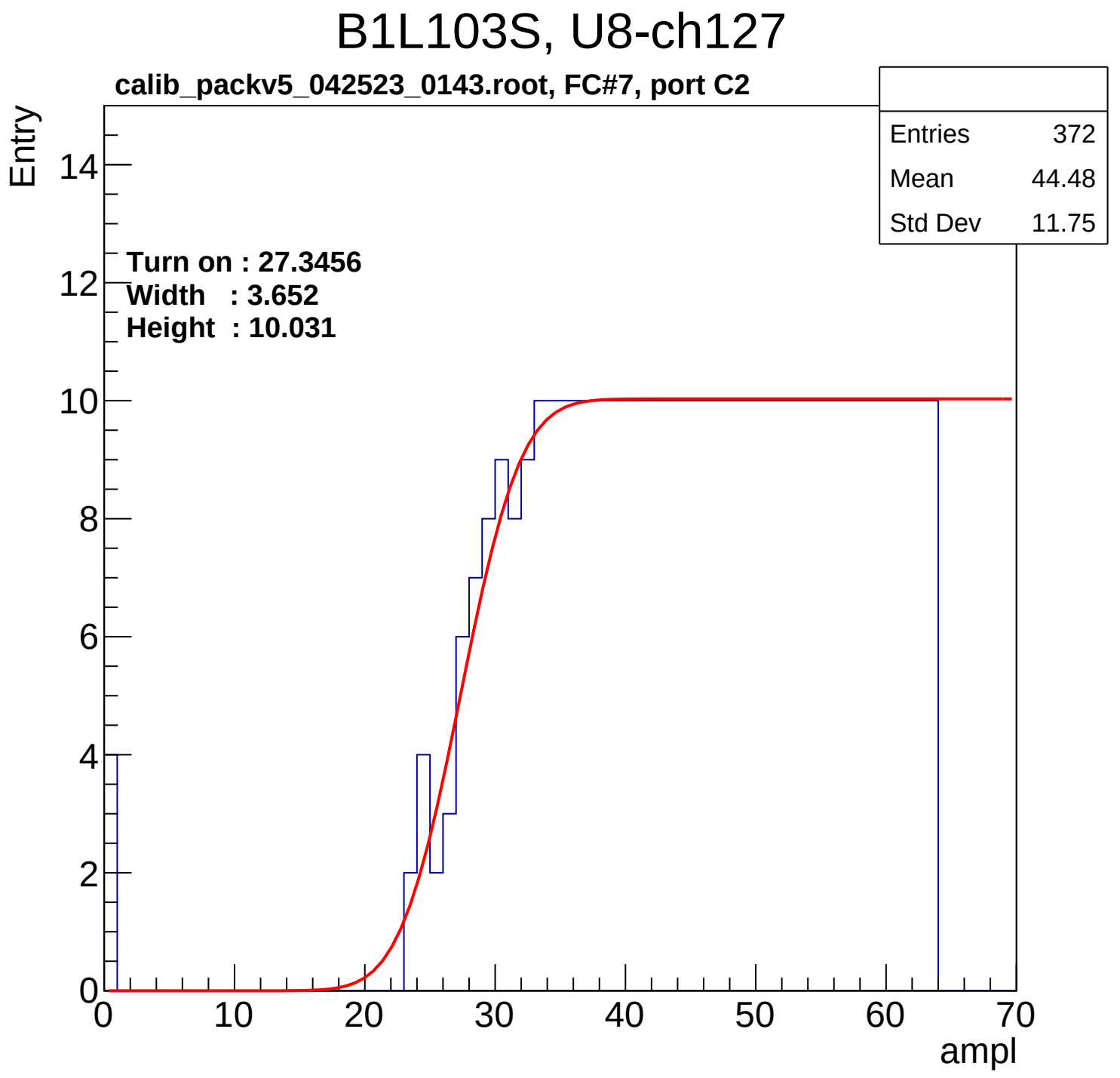

B1L103S, U8-ch127
calib_packv5_042523_0143.root, FC#7, port C2
Entries 372
Mean 44.48
Std Dev 11.75
Turn on : 27.3456
Width : 3.652
Height : 10.031
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U8-ch127
calib_packv5_042523_0143.root, FC#7, port C2
Entries 372
Mean 44.48
Std Dev 11.75
Turn on : 27.3456
Width : 3.652
Height : 10.031
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70