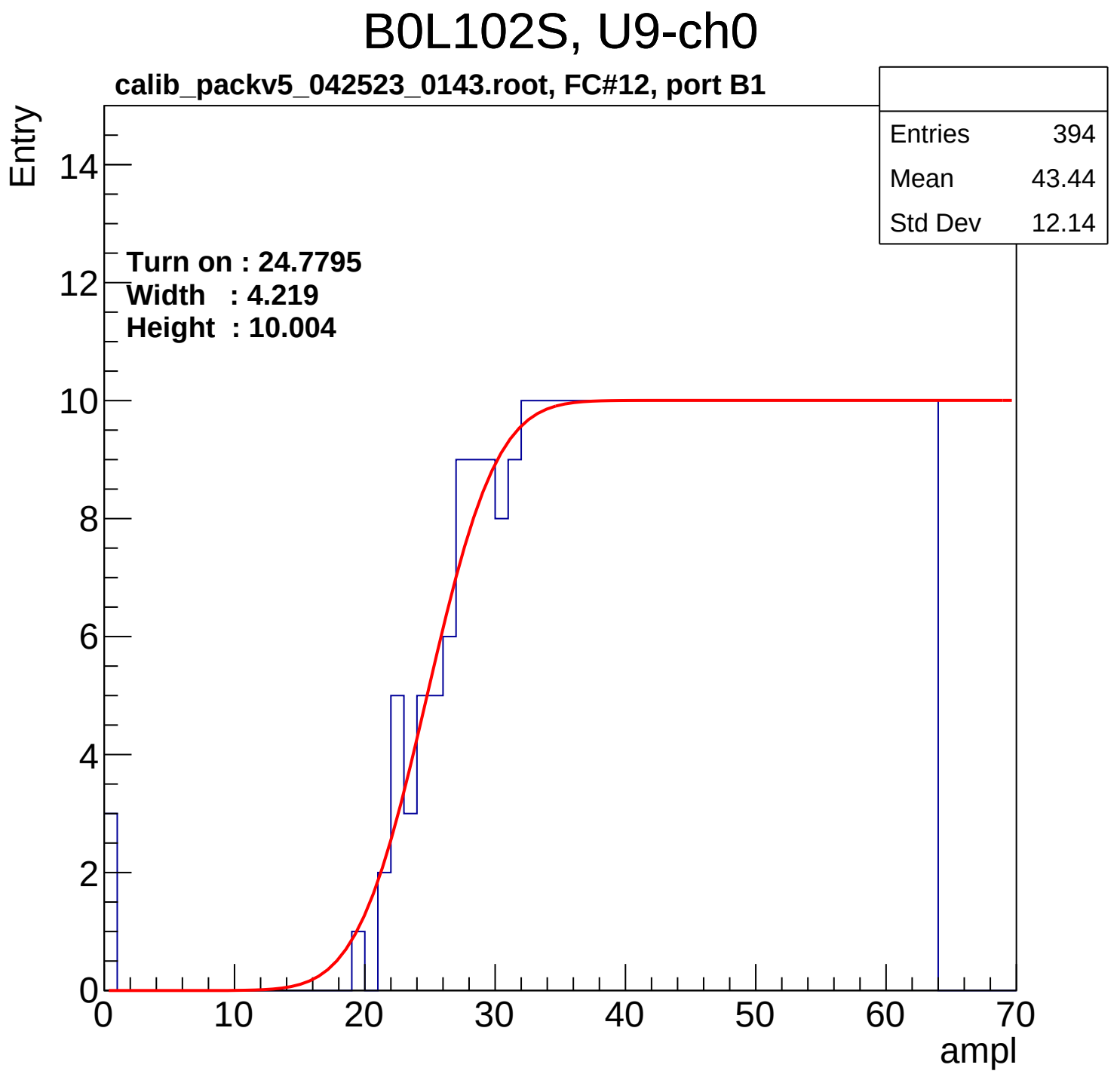
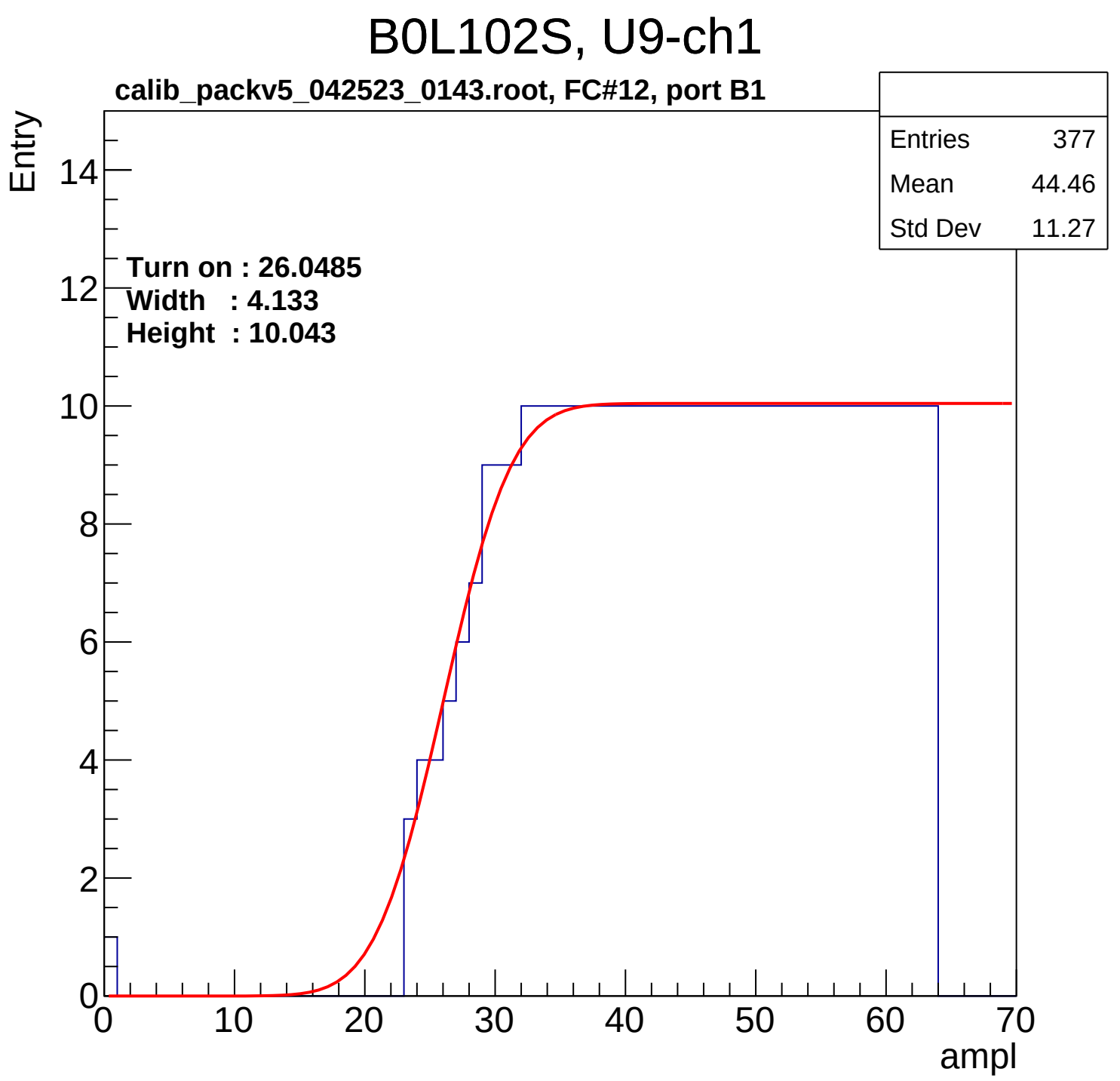
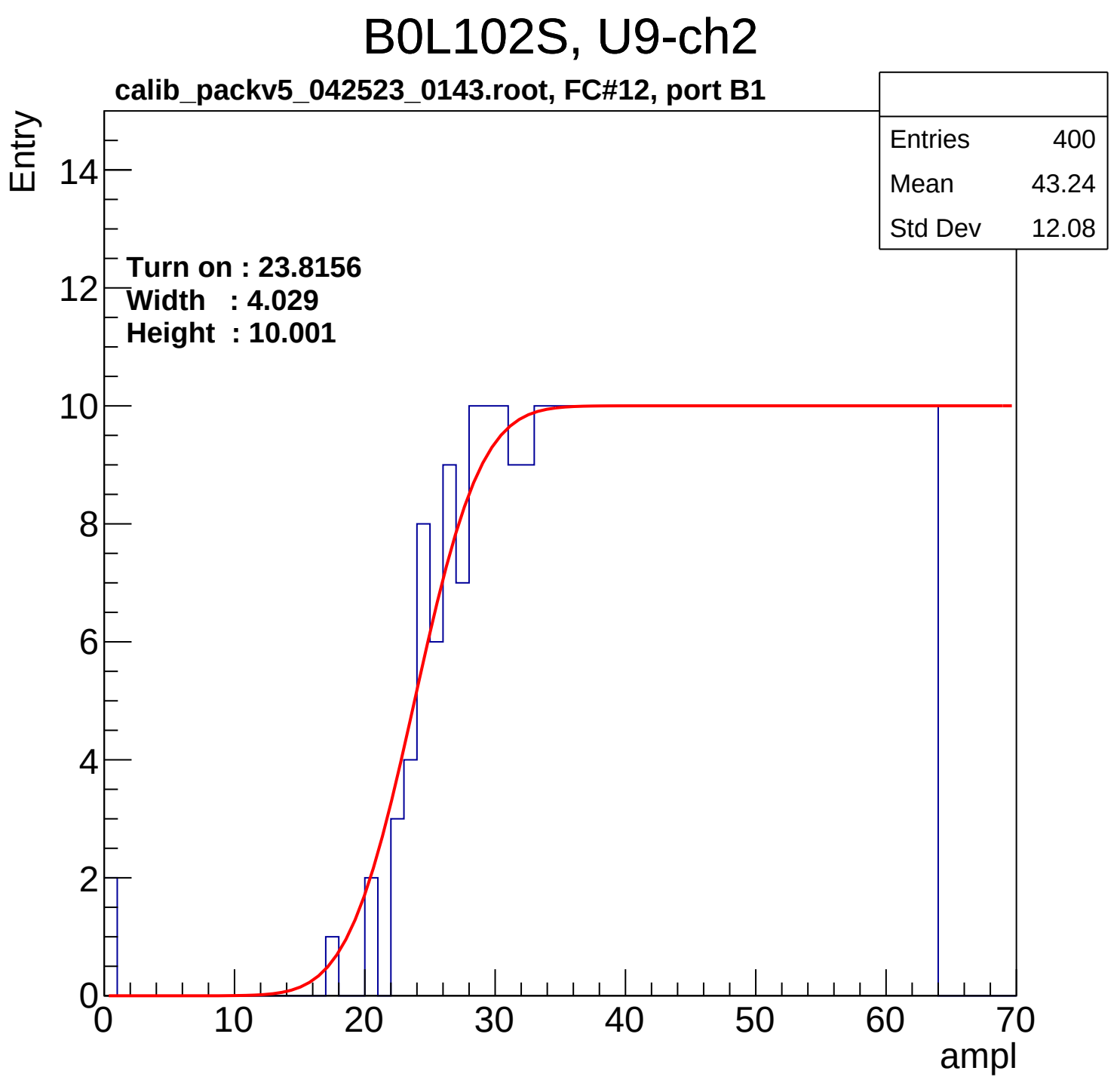
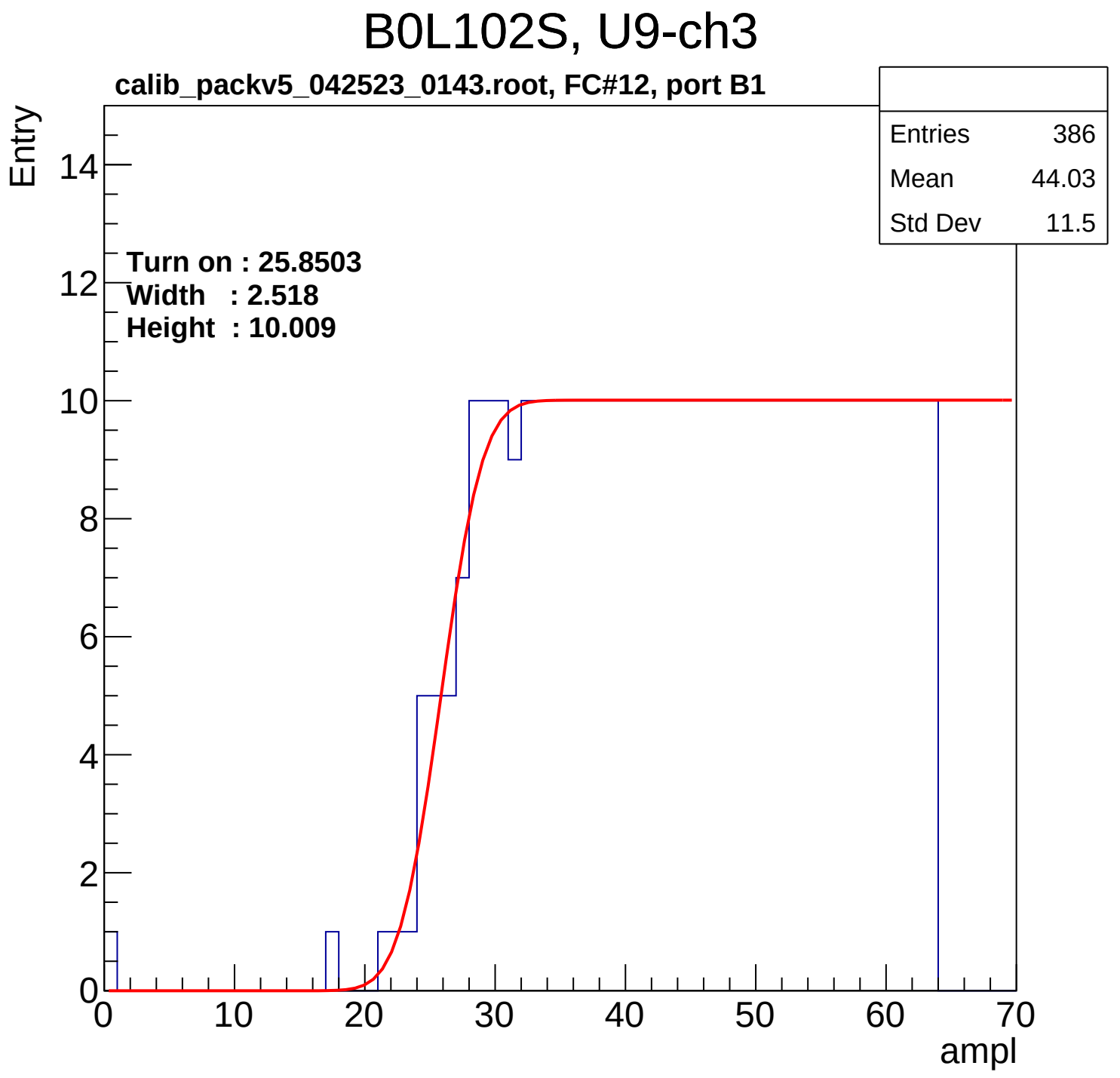
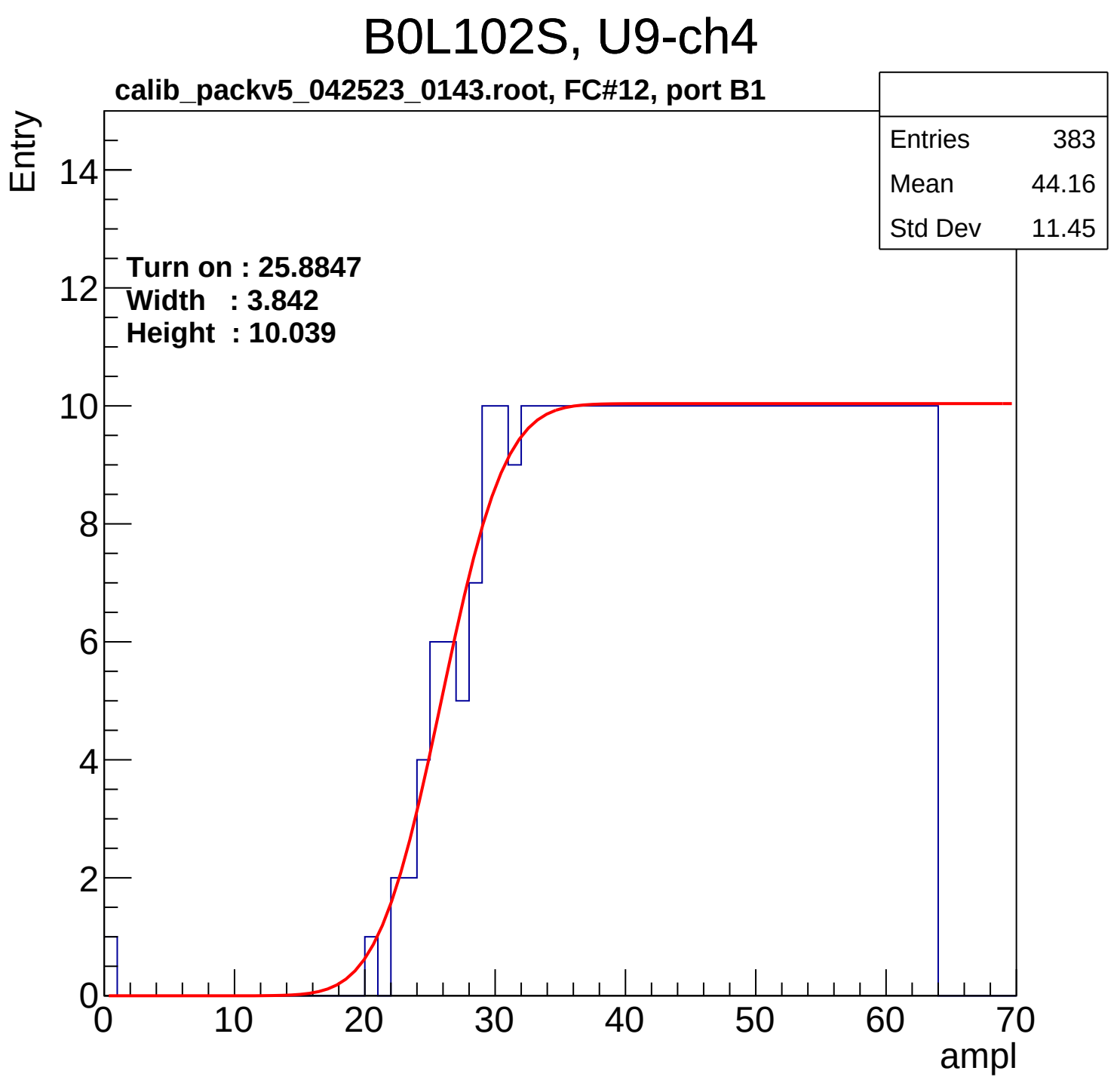
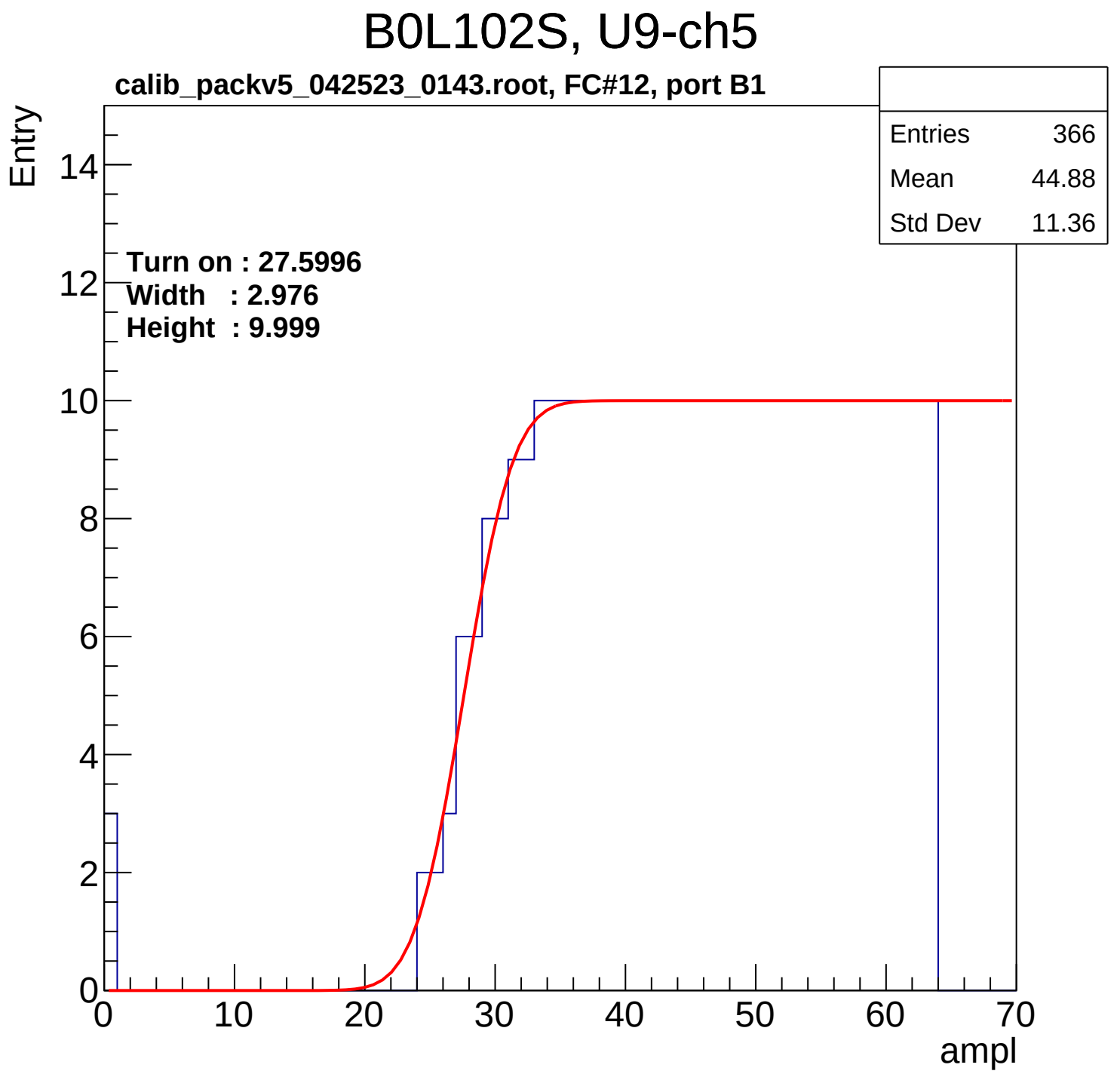

B0L102S, U9-ch0
calib_packv5_042523_0143.root, FC#12, port B1
Entries 394
Mean 43.44
Std Dev 12.14
Turn on : 24.7795
Width : 4.219
Height : 10.004
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

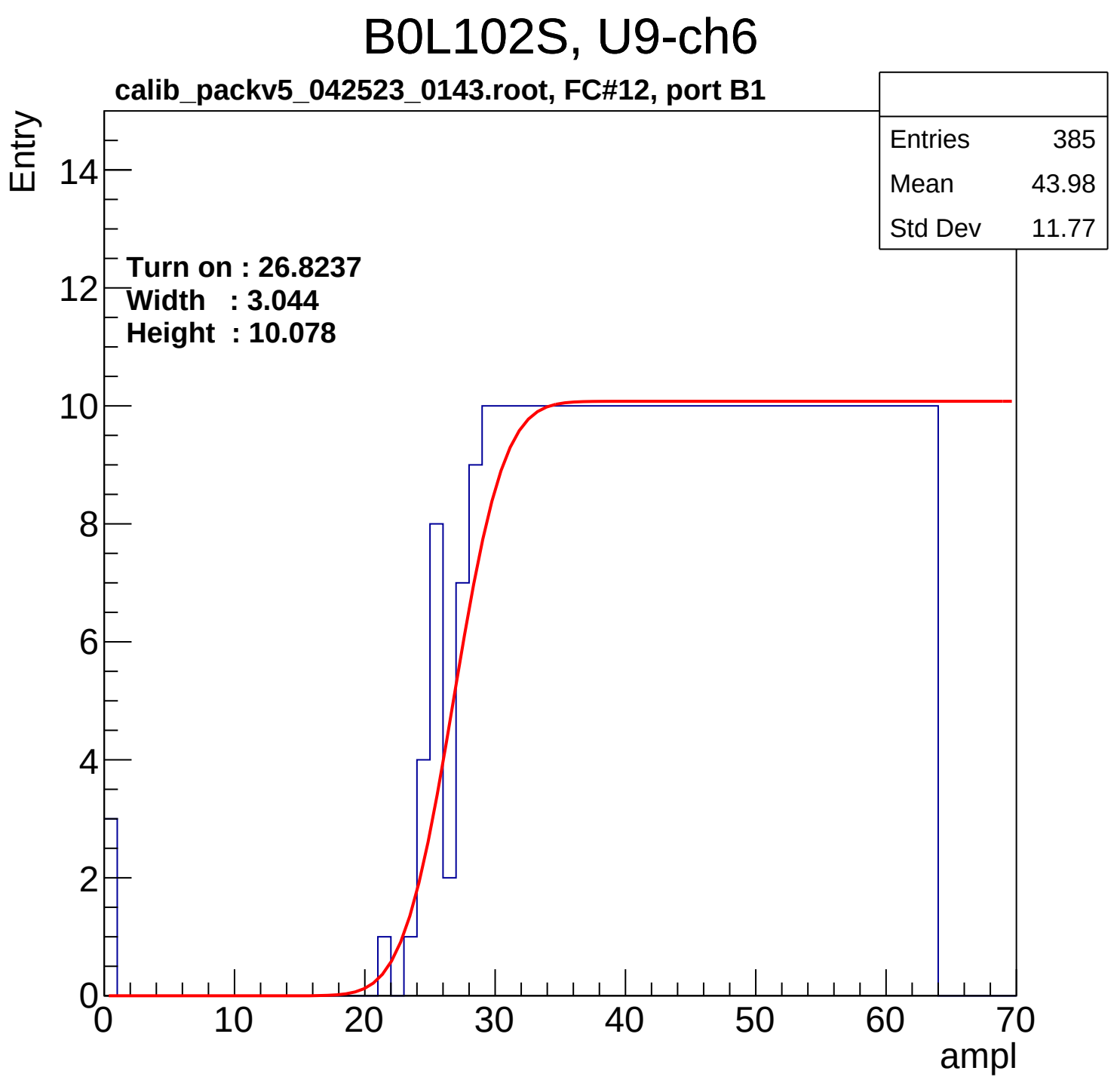

B0L102S, U9-ch1
calib_packv5_042523_0143.root, FC#12, port B1
Entries 377
Mean 44.46
Std Dev 11.27
Turn on : 26.0485
Width : 4.133
Height : 10.043
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

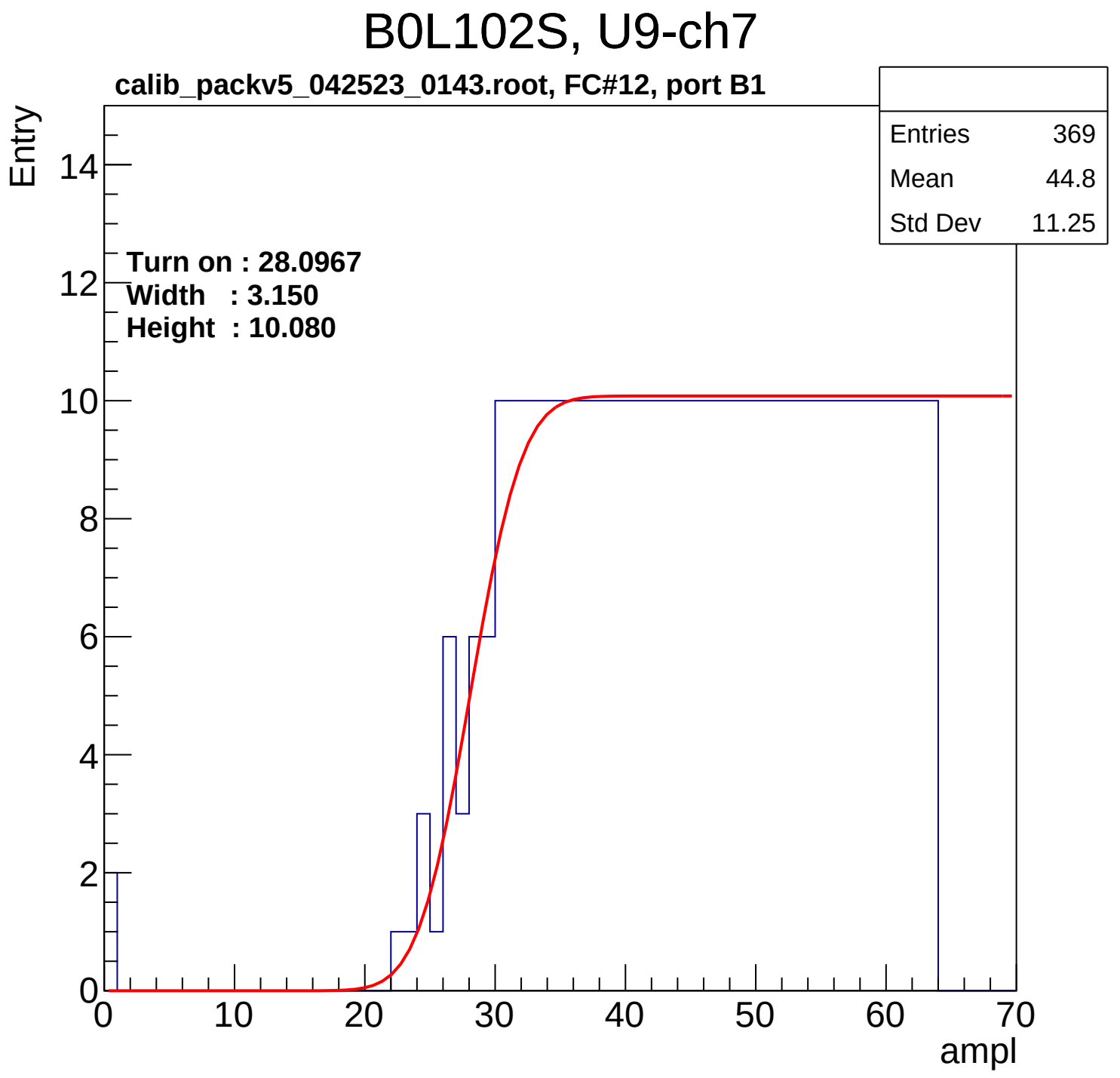

B0L102S, U9-ch2
calib_packv5_042523_0143.root, FC#12, port B1
Entries 400
Mean 43.24
Std Dev 12.08
Turn on : 23.8156
Width : 4.029
Height : 10.001
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

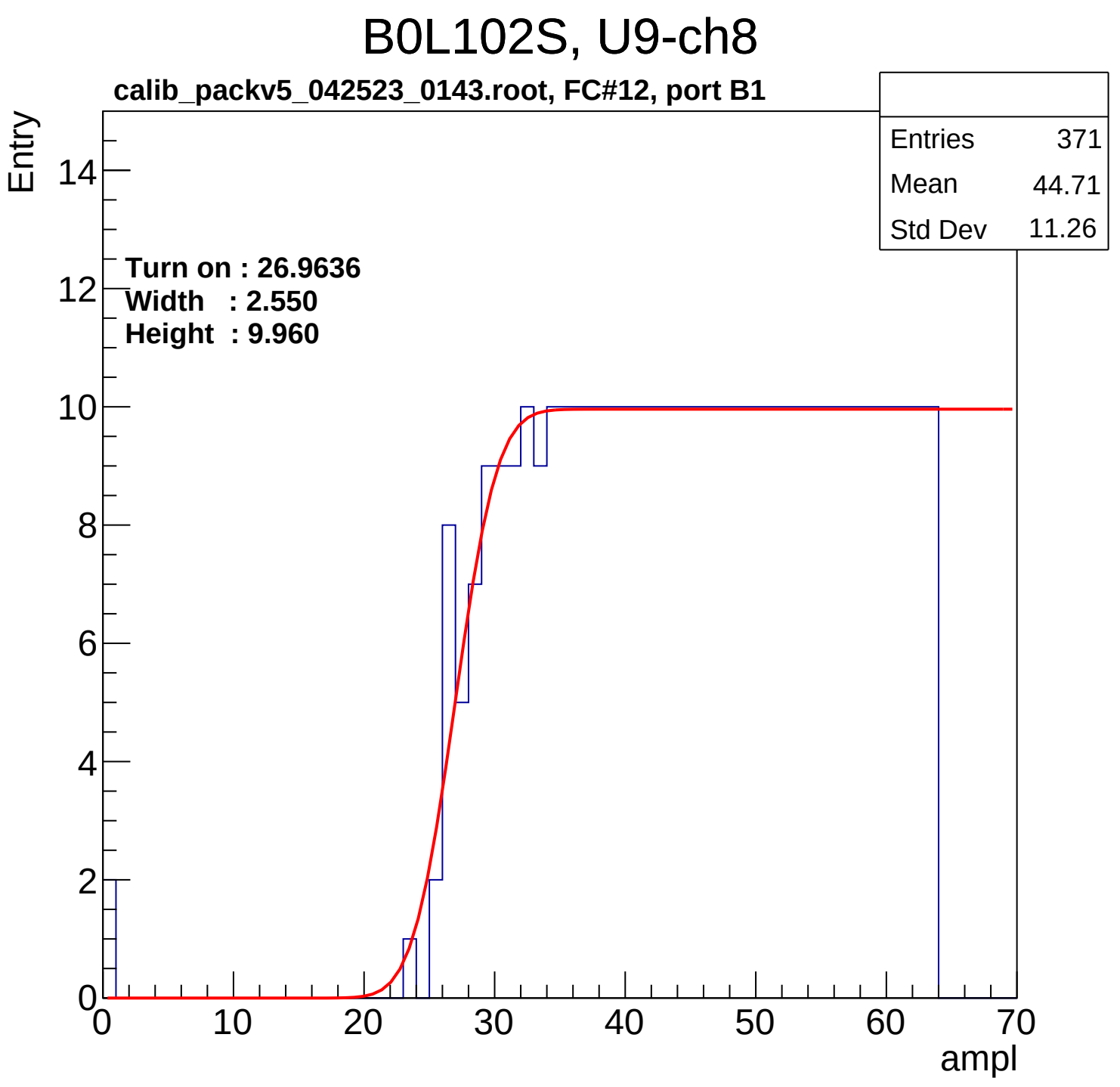

B0L102S, U9-ch3
calib_packv5_042523_0143.root, FC#12, port B1
Entries 386
Mean 44.03
Std Dev 11.5
Turn on : 25.8503
Width : 2.518
Height : 10.009
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

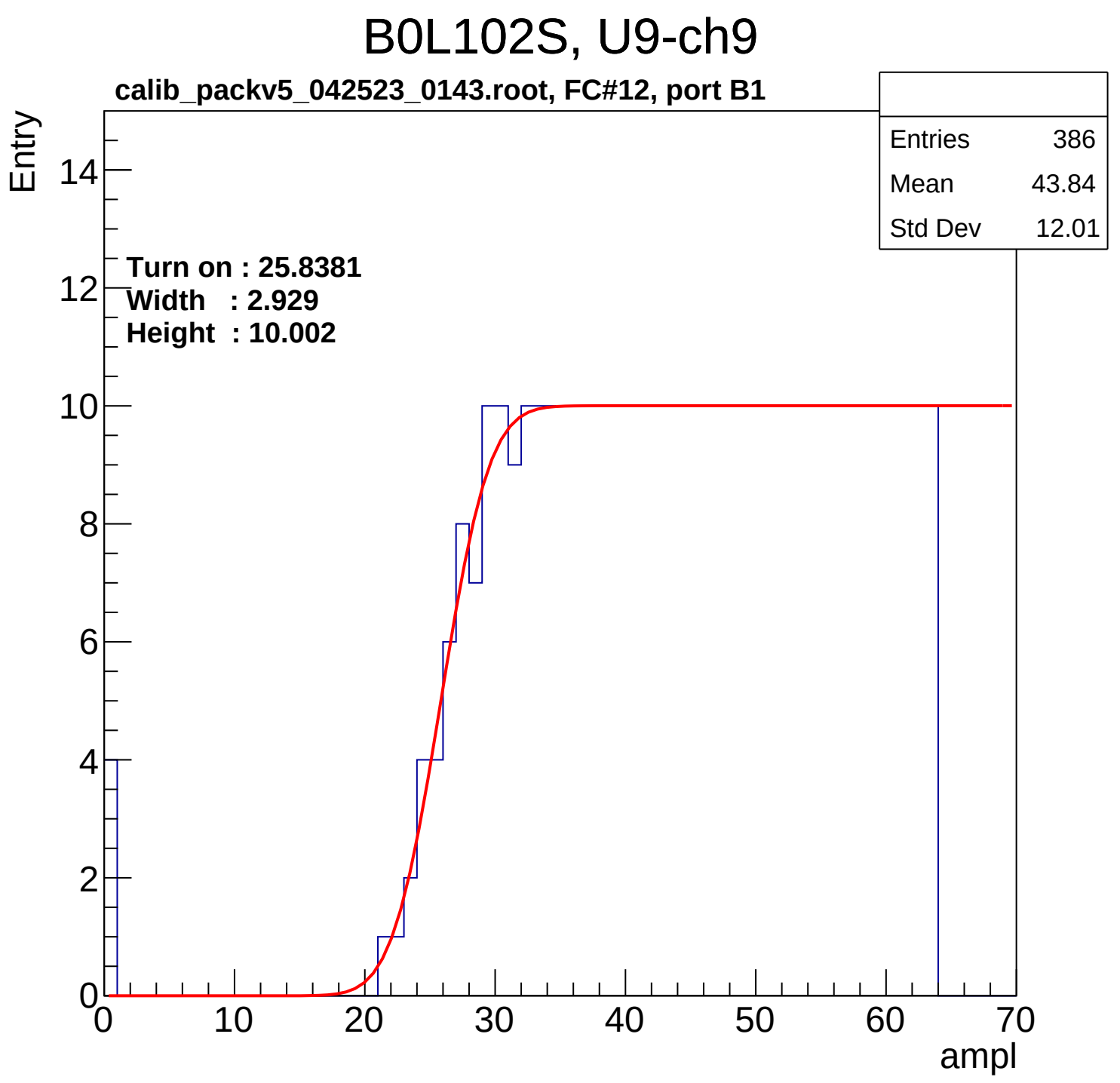

B0L102S, U9-ch4
calib_packv5_042523_0143.root, FC#12, port B1
Entries 383
Mean 44.16
Std Dev 11.45
Turn on : 25.8847
Width : 3.842
Height : 10.039
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

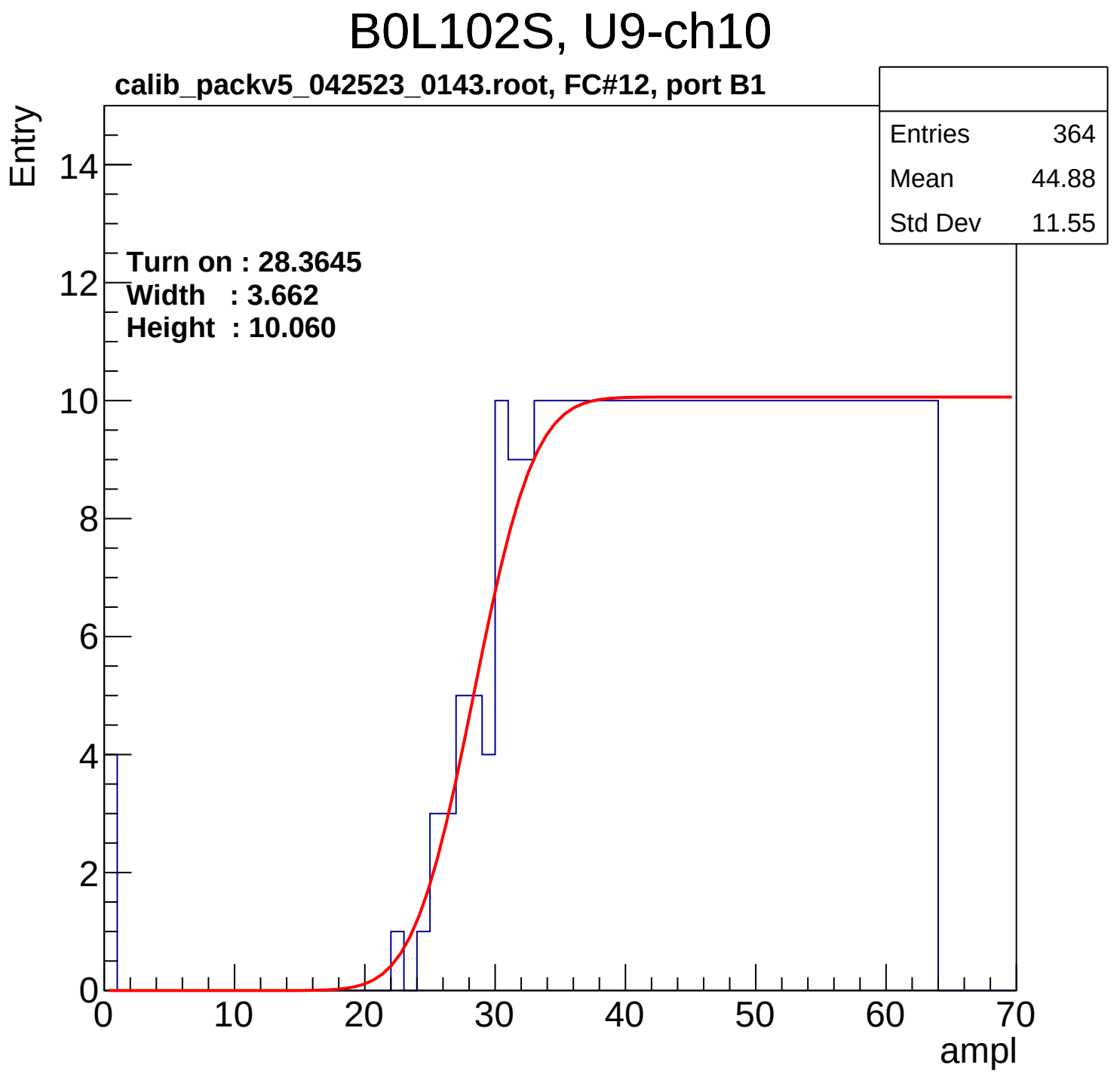

B0L102S, U9-ch5
calib_packv5_042523_0143.root, FC#12, port B1
Entries 366
Mean 44.88
Std Dev 11.36
Turn on : 27.5996
Width : 2.976
Height : 9.999
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

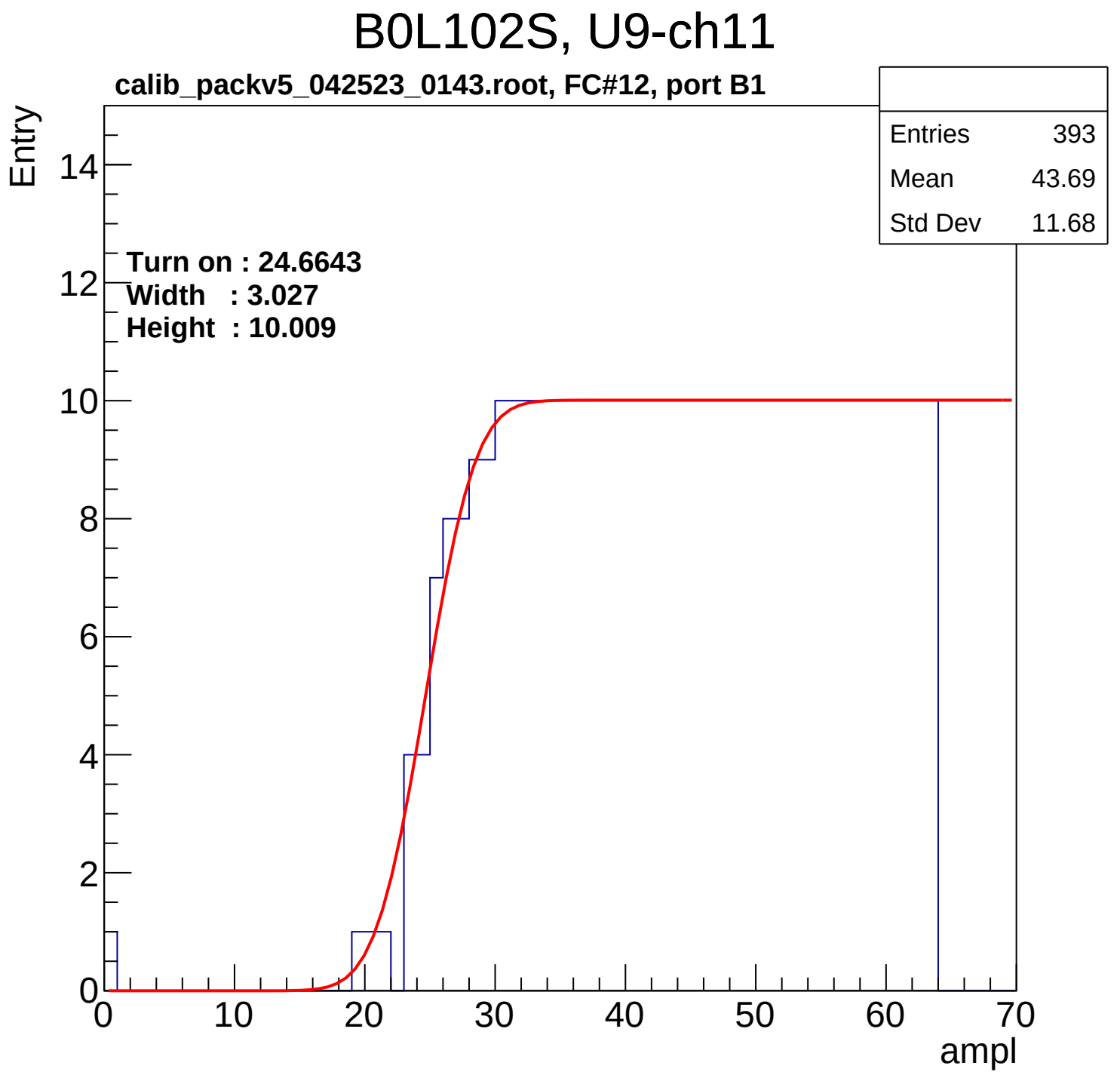

B0L102S, U9-ch6
calib_packv5_042523_0143.root, FC#12, port B1
Entries 385
Mean 43.98
Std Dev 11.77
Turn on : 26.8237
Width : 3.044
Height : 10.078
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

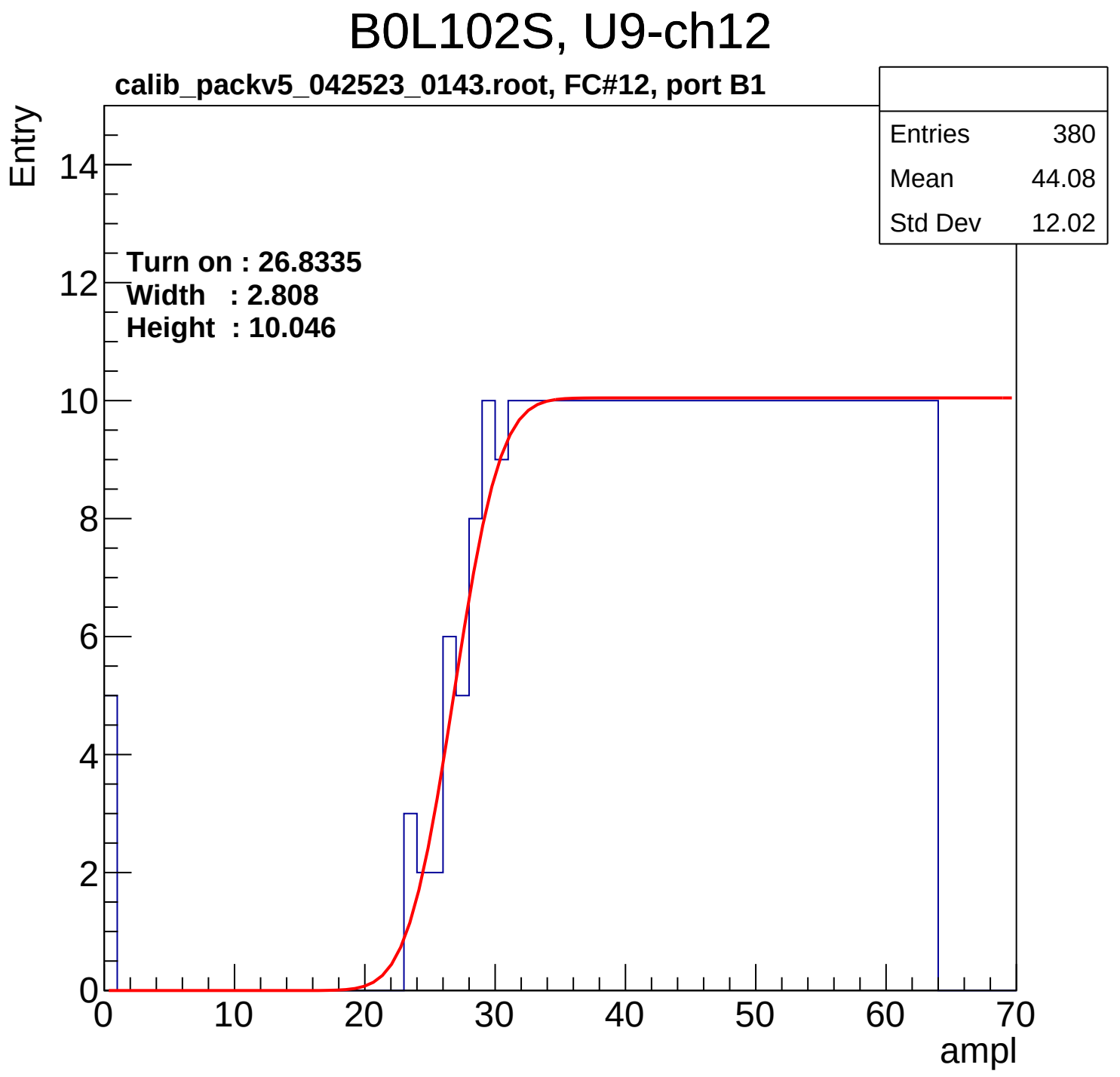

B0L102S, U9-ch7
calib_packv5_042523_0143.root, FC#12, port B1
Entries 369
Mean 44.8
Std Dev 11.25
Turn on : 28.0967
Width : 3.150
Height : 10.080
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

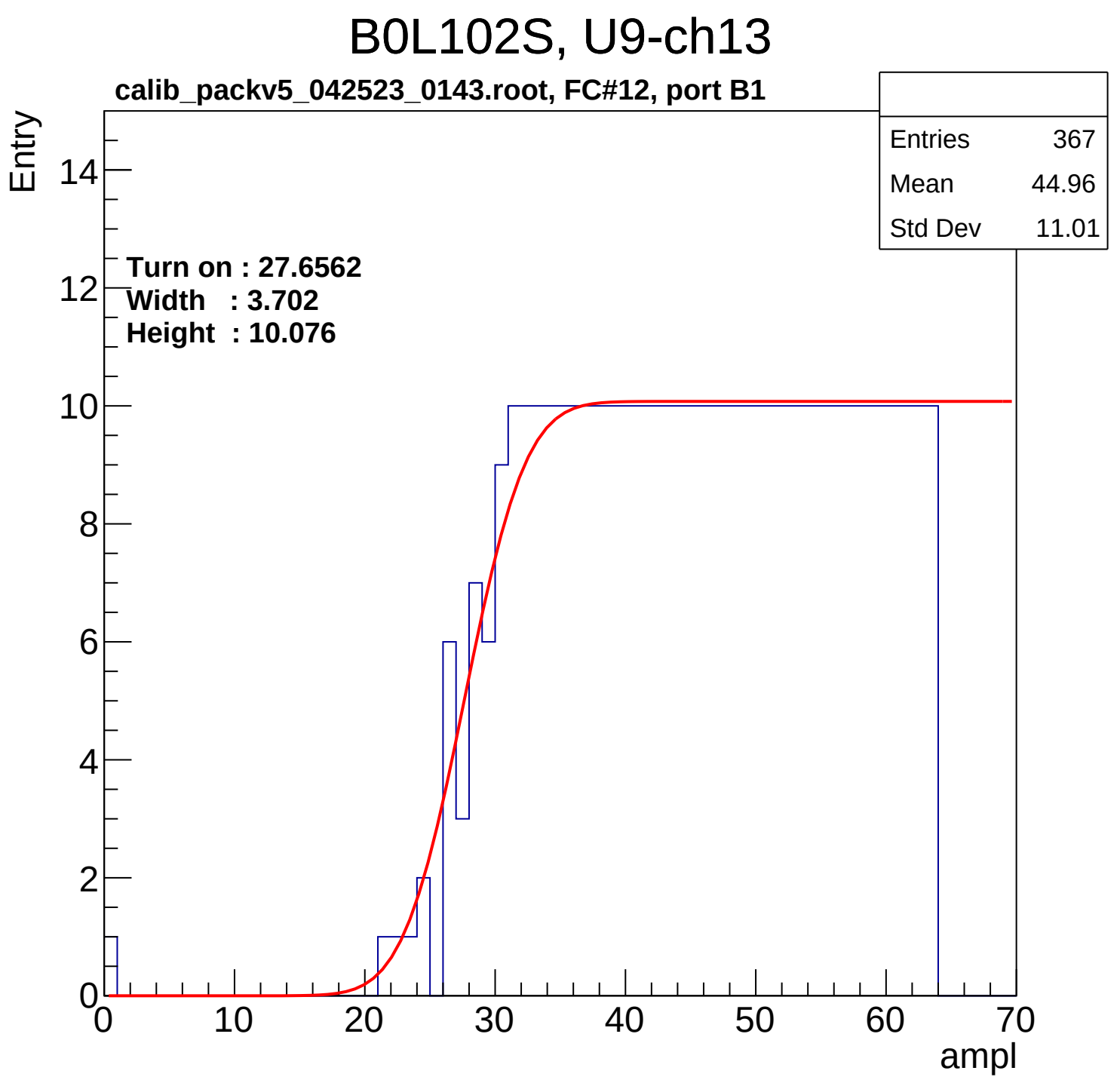

B0L102S, U9-ch8
calib_packv5_042523_0143.root, FC#12, port B1
Entries 371
Mean 44.71
Std Dev 11.26
Turn on : 26.9636
Width : 2.550
Height : 9.960
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

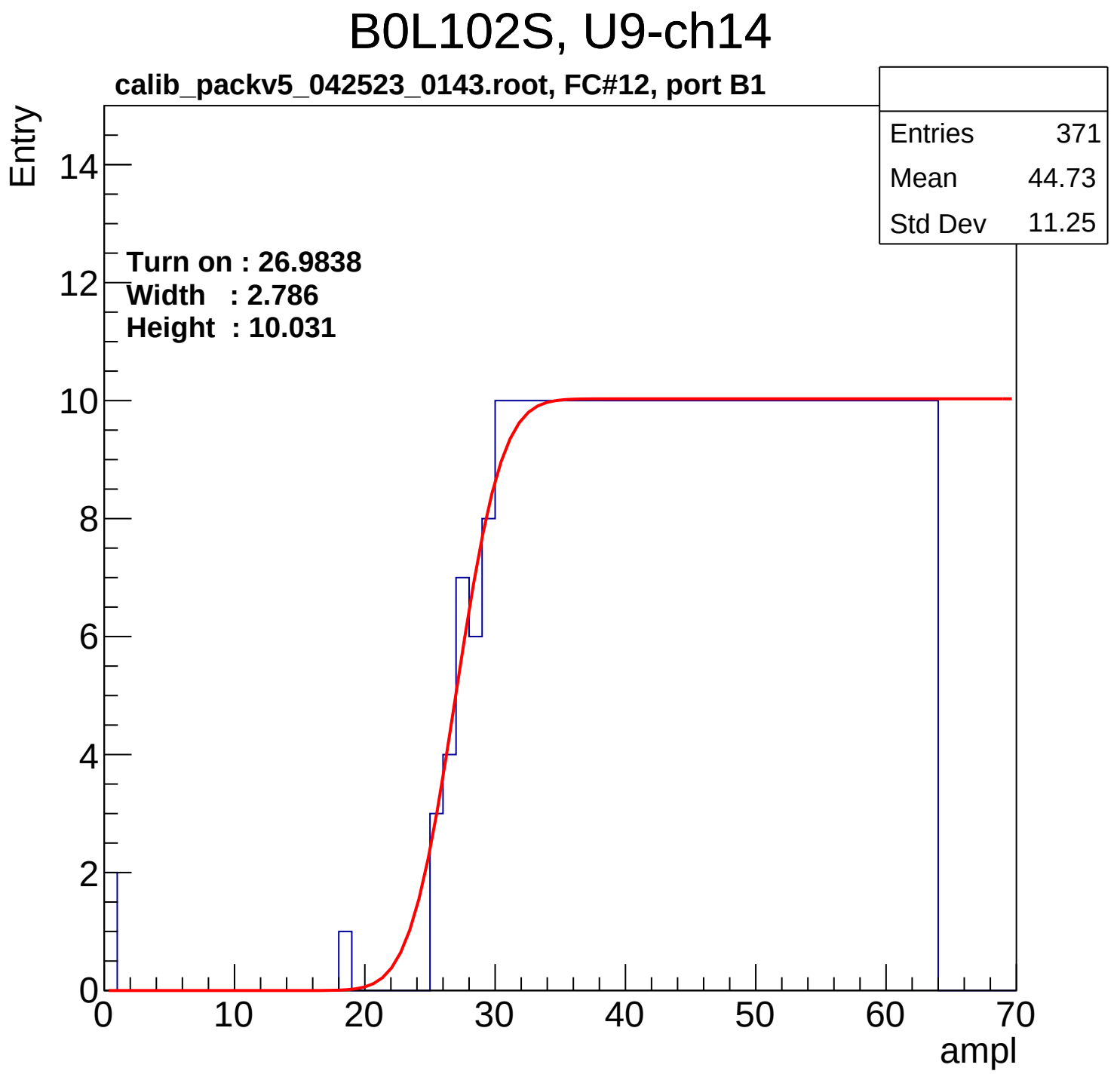

B0L102S, U9-ch9
calib_packv5_042523_0143.root, FC#12, port B1
Entries 386
Mean 43.84
Std Dev 12.01
Turn on : 25.8381
Width : 2.929
Height : 10.002
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

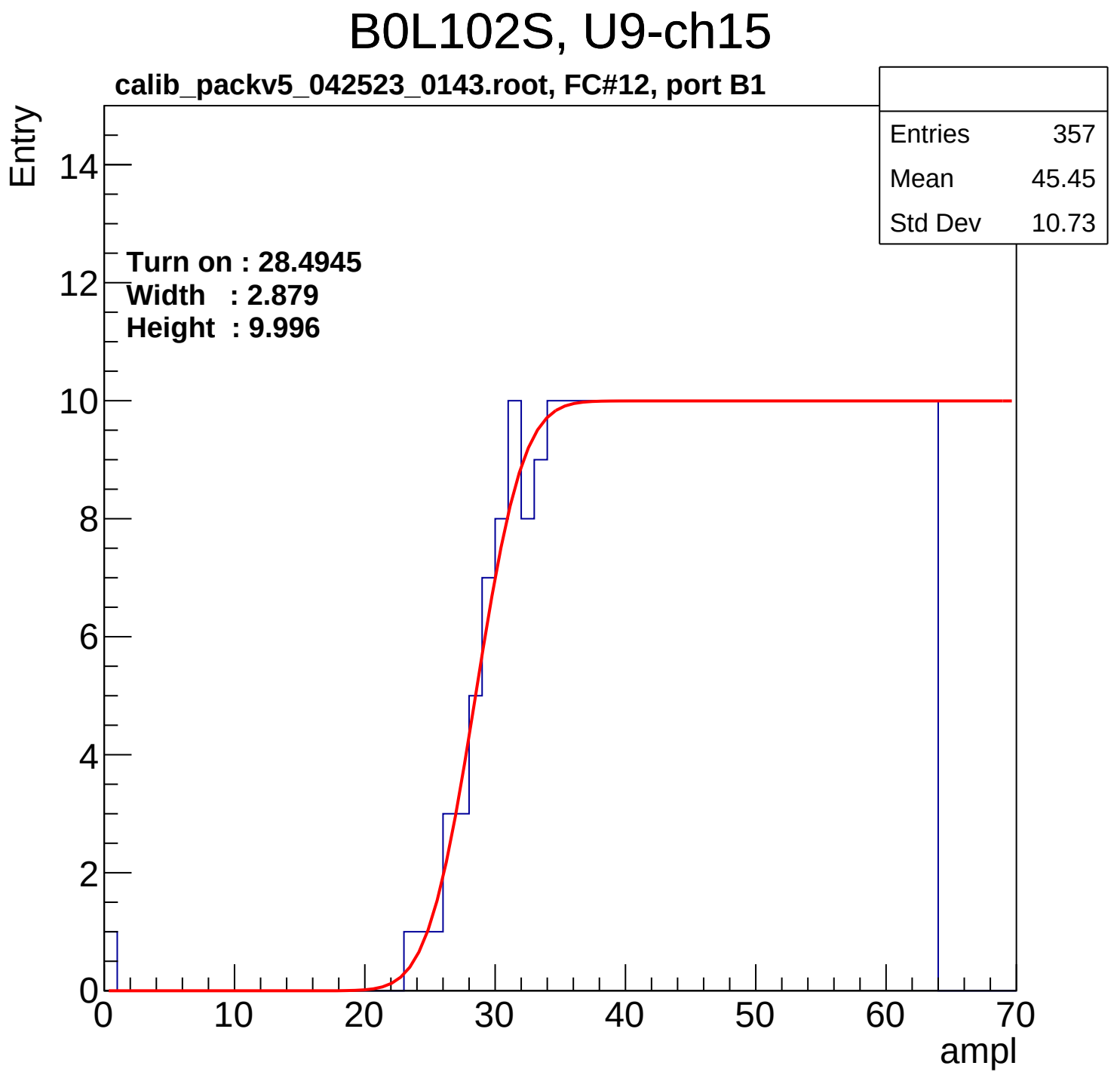

B0L102S, U9-ch10
calib_packv5_042523_0143.root, FC#12, port B1
Entries 364
Mean 44.88
Std Dev 11.55
Turn on : 28.3645
Width : 3.662
Height : 10.060
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

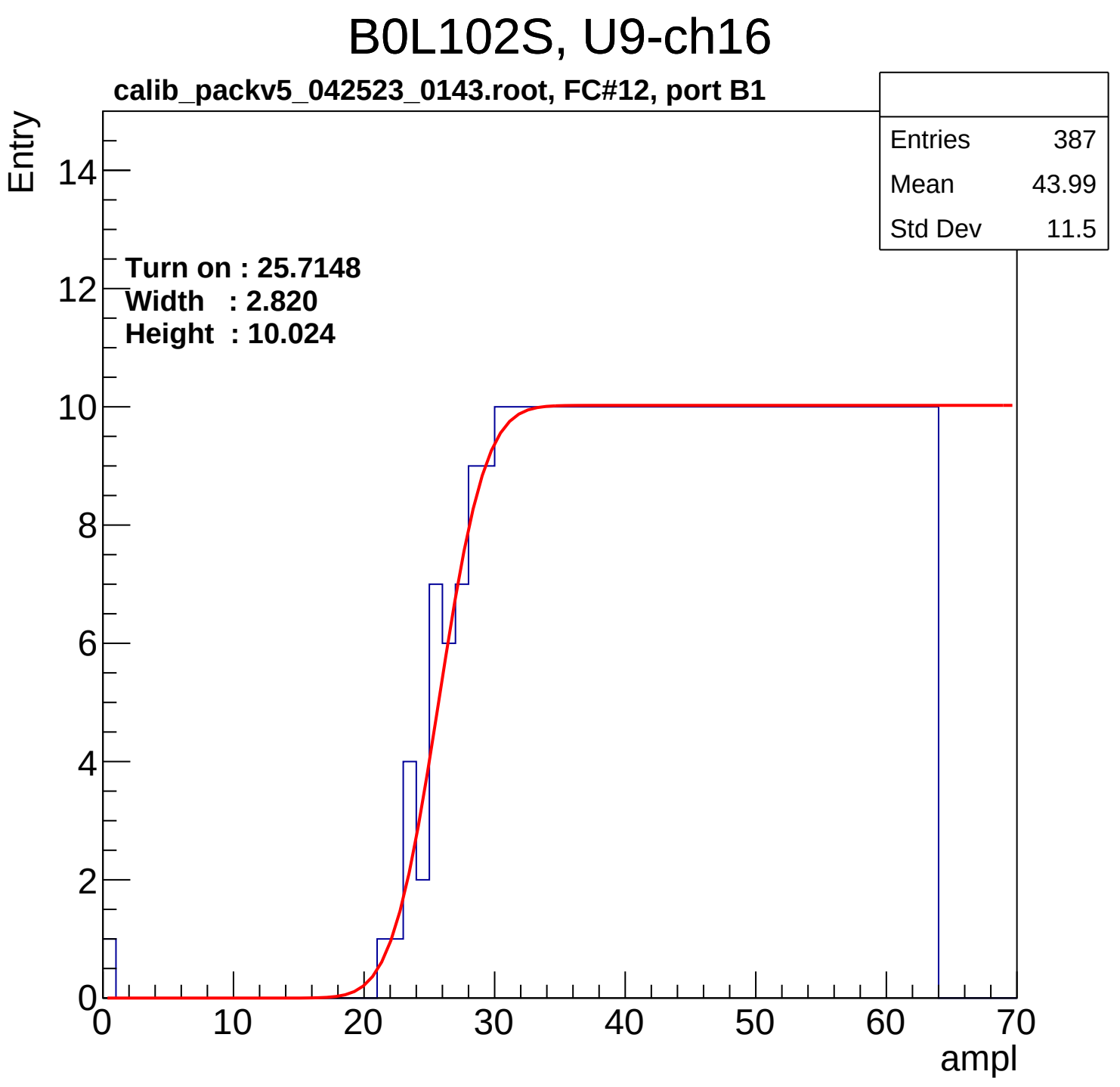

B0L102S, U9-ch11
calib_packv5_042523_0143.root, FC#12, port B1
Entries 393
Mean 43.69
Std Dev 11.68
Turn on : 24.6643
Width : 3.027
Height : 10.009
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

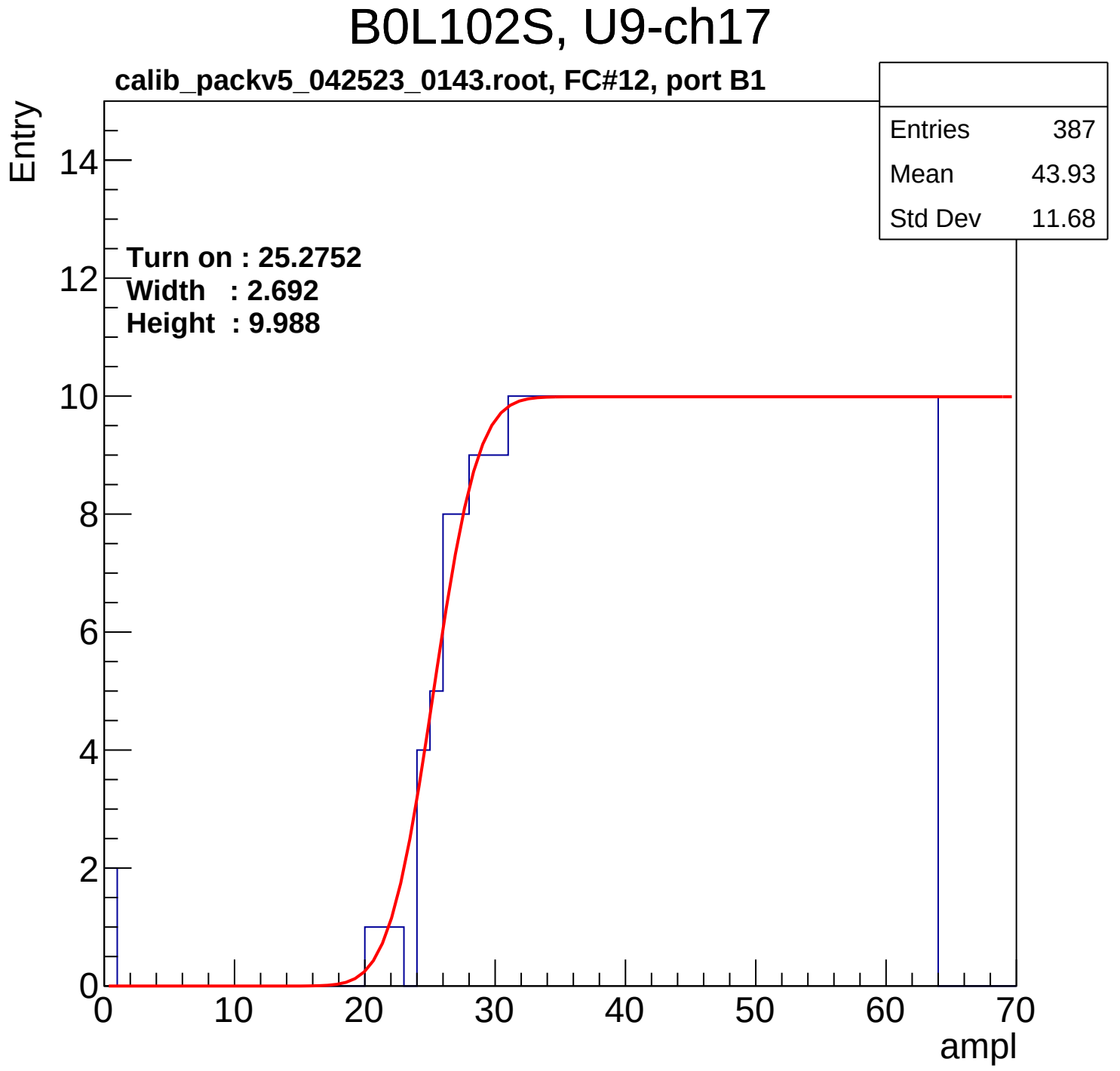

B0L102S, U9-ch12
calib_packv5_042523_0143.root, FC#12, port B1
Entries 380
Mean 44.08
Std Dev 12.02
Turn on : 26.8335
Width : 2.808
Height : 10.046
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

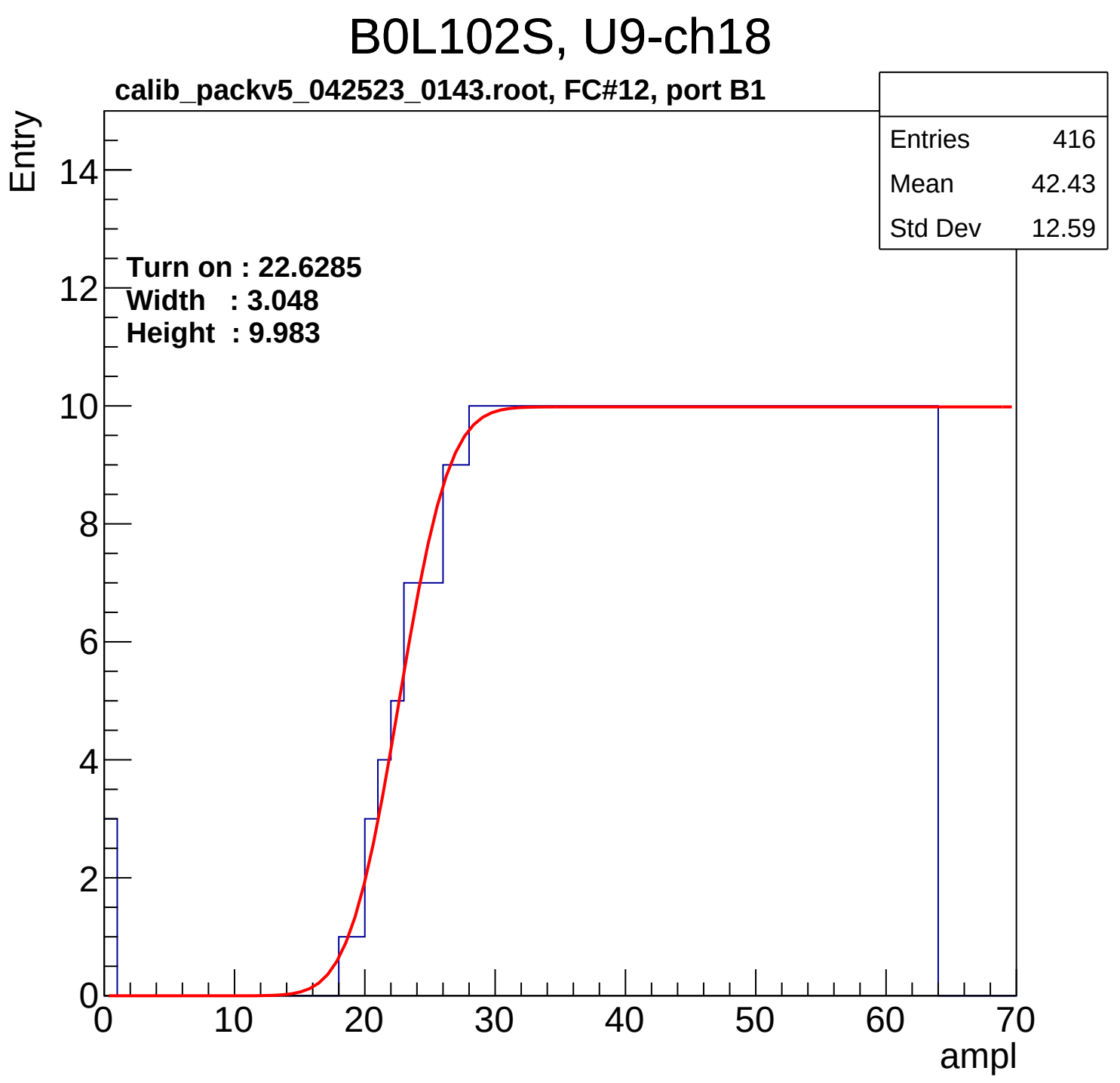

B0L102S, U9-ch13
calib_packv5_042523_0143.root, FC#12, port B1
Entries 367
Mean 44.96
Std Dev 11.01
Turn on : 27.6562
Width : 3.702
Height : 10.076
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

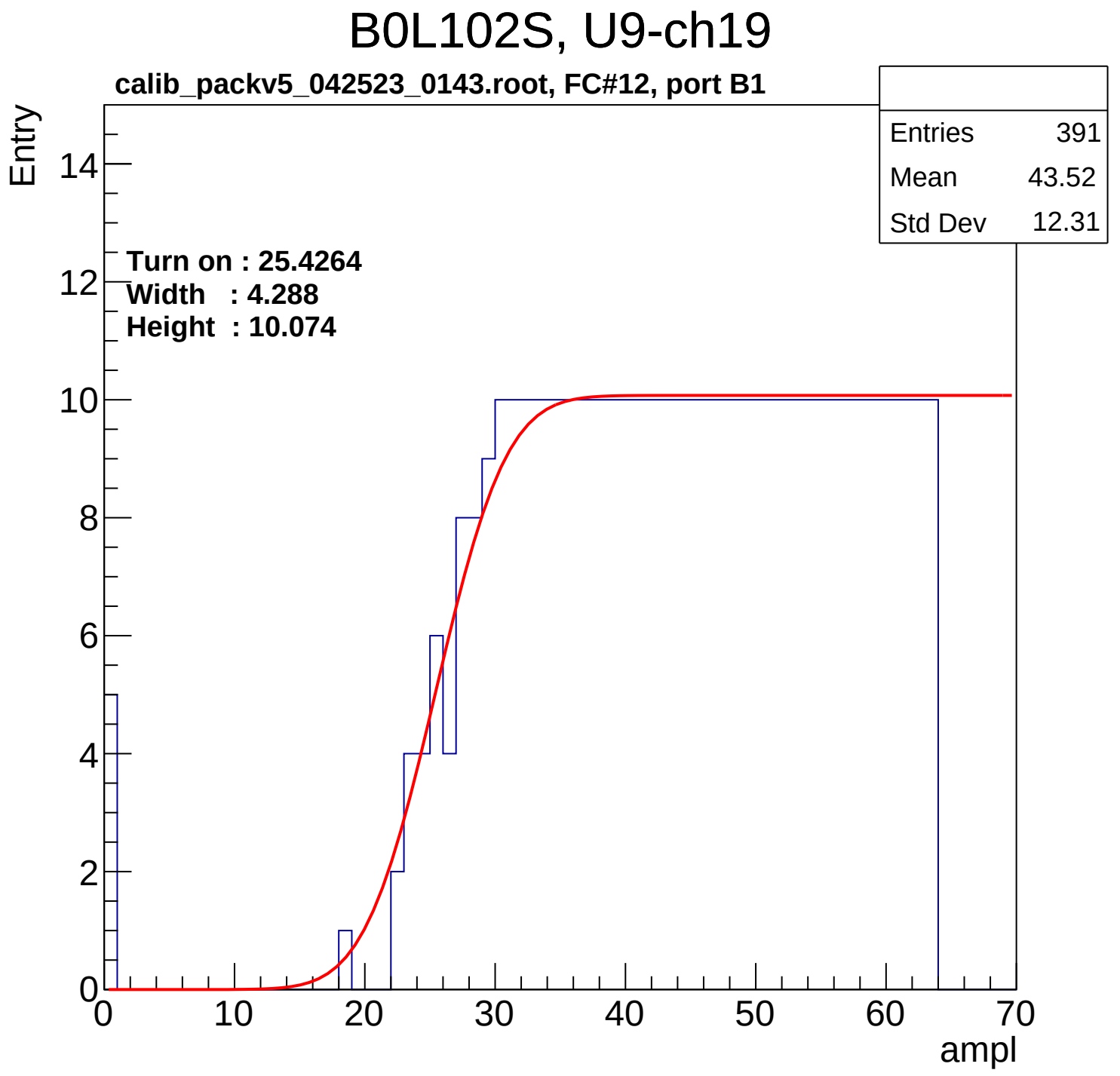

B0L102S, U9-ch14
calib_packv5_042523_0143.root, FC#12, port B1
Entries 371
Mean 44.73
Std Dev 11.25
Turn on : 26.9838
Width : 2.786
Height : 10.031
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

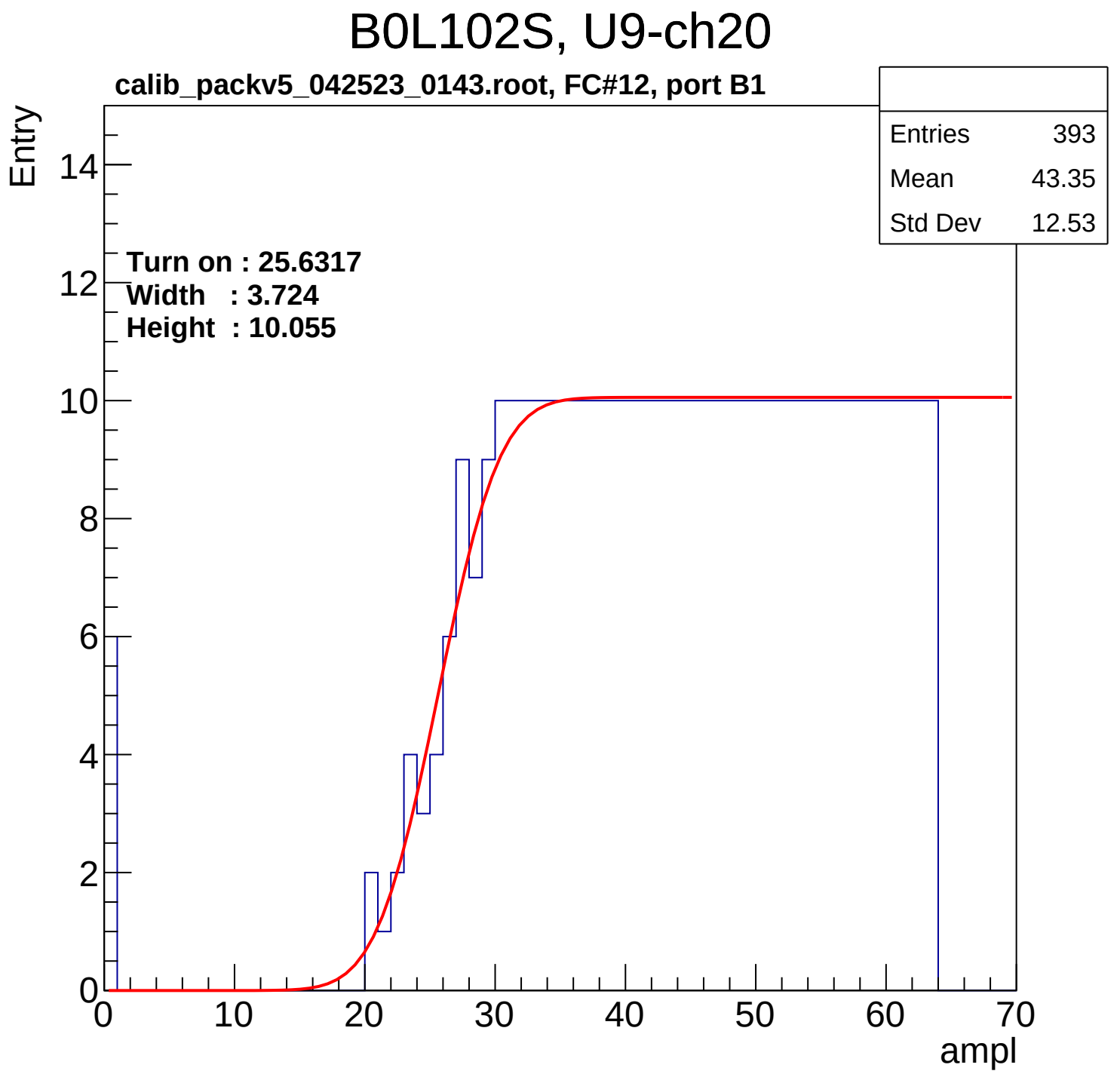

B0L102S, U9-ch15
calib_packv5_042523_0143.root, FC#12, port B1
Entries 357
Mean 45.45
Std Dev 10.73
Turn on : 28.4945
Width : 2.879
Height : 9.996
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

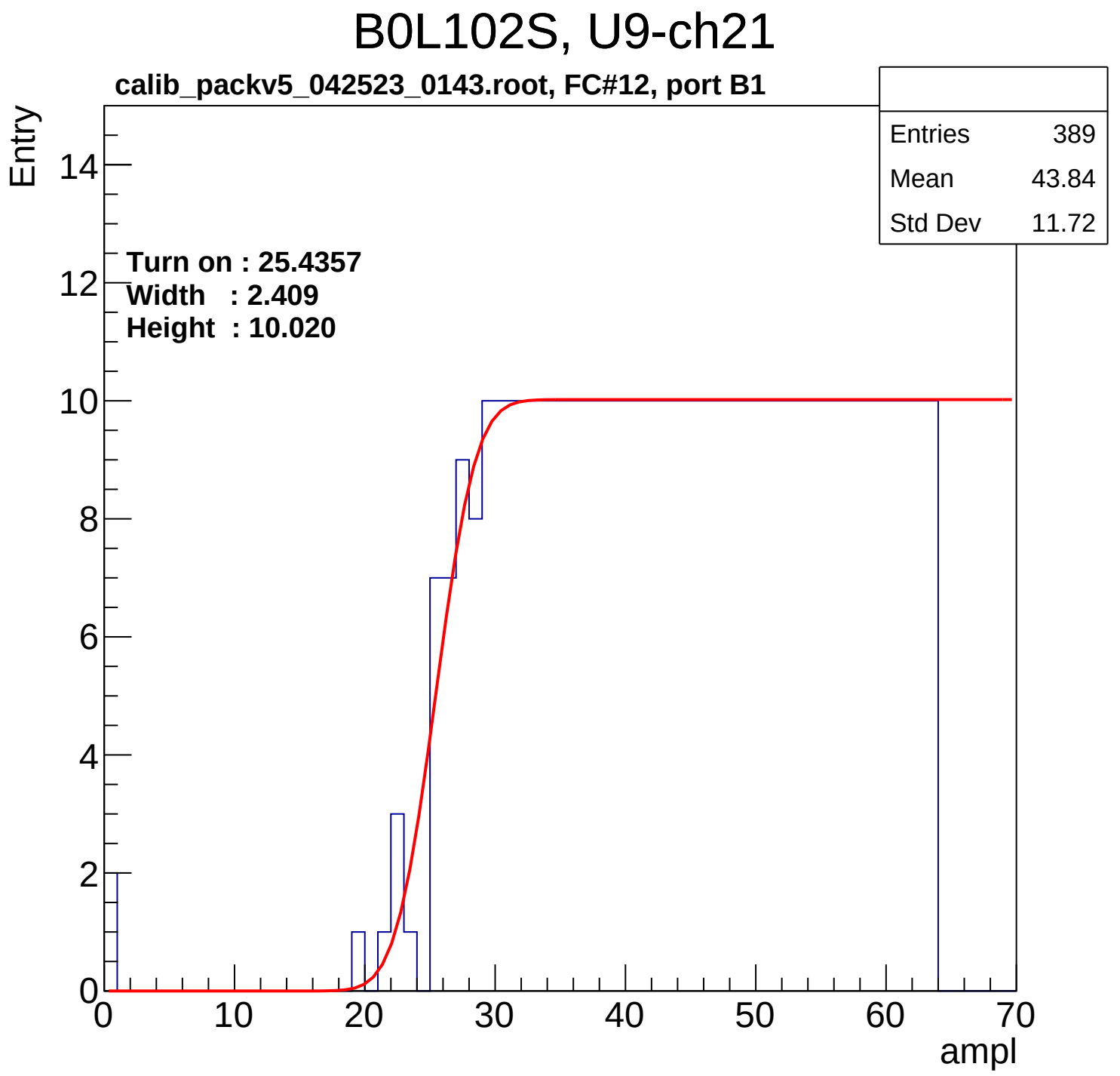

B0L102S, U9-ch16
calib_packv5_042523_0143.root, FC#12, port B1
Entries 387
Mean 43.99
Std Dev 11.5
Turn on : 25.7148
Width : 2.820
Height : 10.024
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

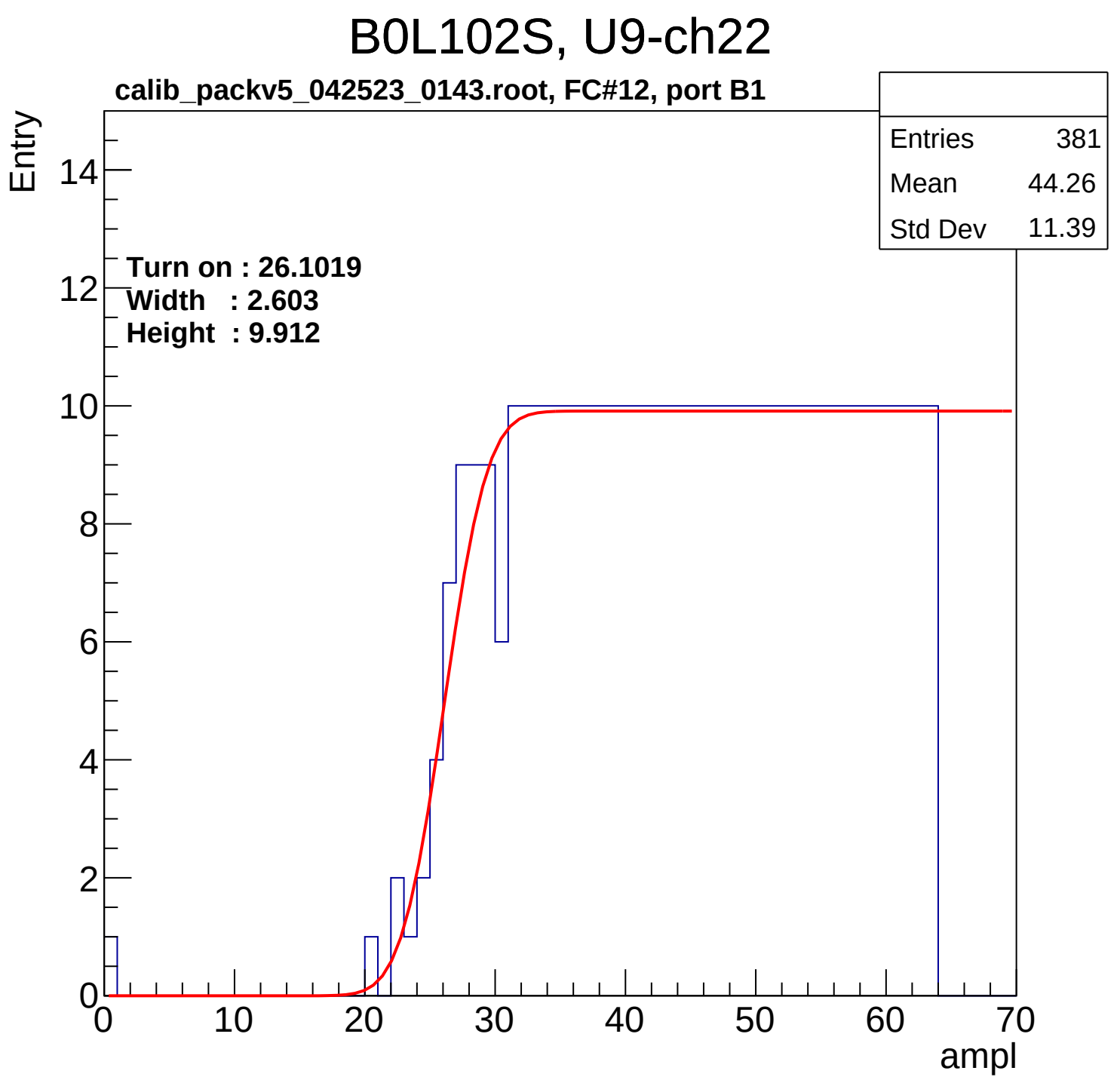

B0L102S, U9-ch17
calib_packv5_042523_0143.root, FC#12, port B1
Entries 387
Mean 43.93
Std Dev 11.68
Turn on : 25.2752
Width : 2.692
Height : 9.988
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

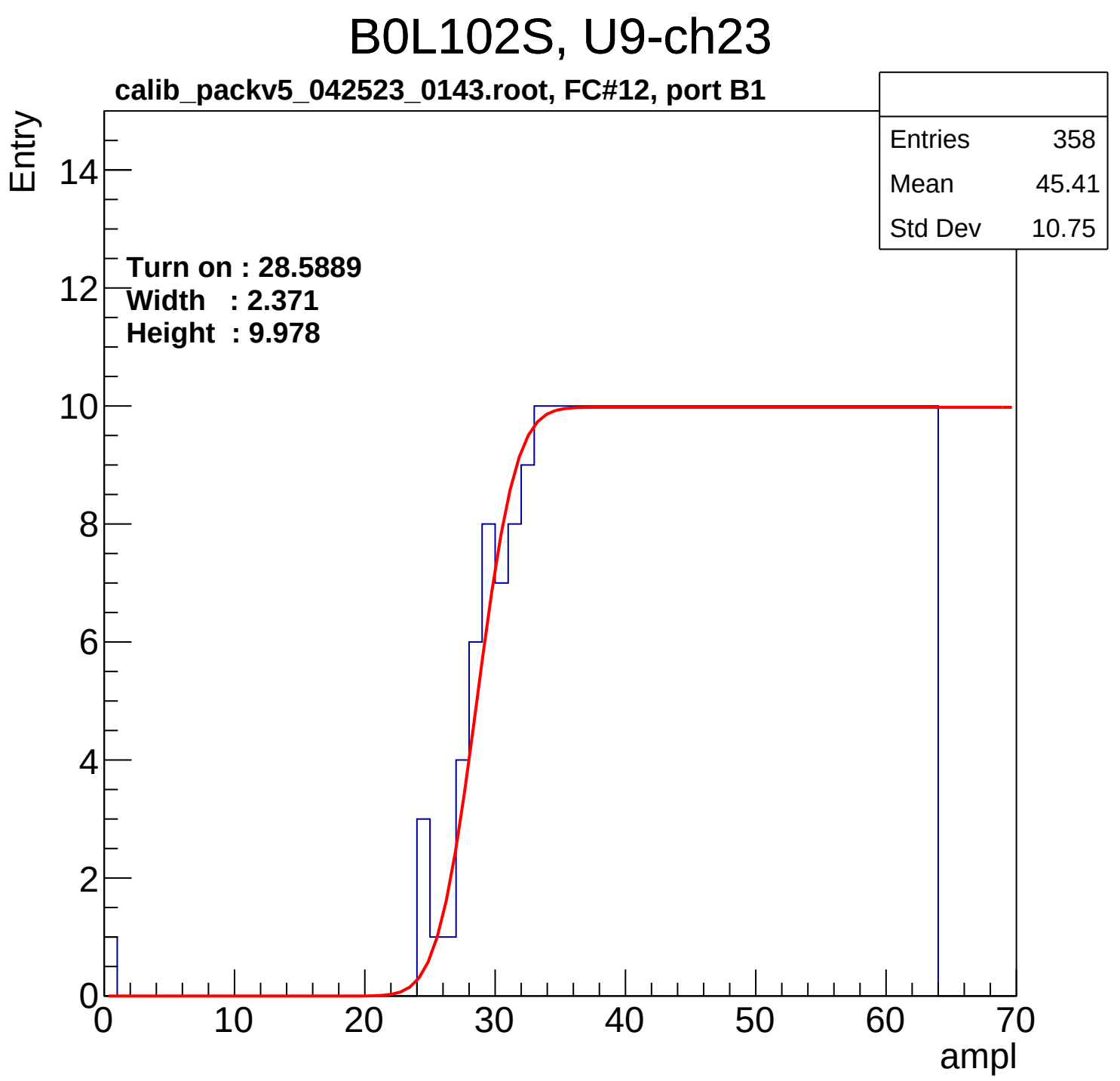

B0L102S, U9-ch18
calib_packv5_042523_0143.root, FC#12, port B1
Entries 416
Mean 42.43
Std Dev 12.59
Turn on : 22.6285
Width : 3.048
Height : 9.983
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

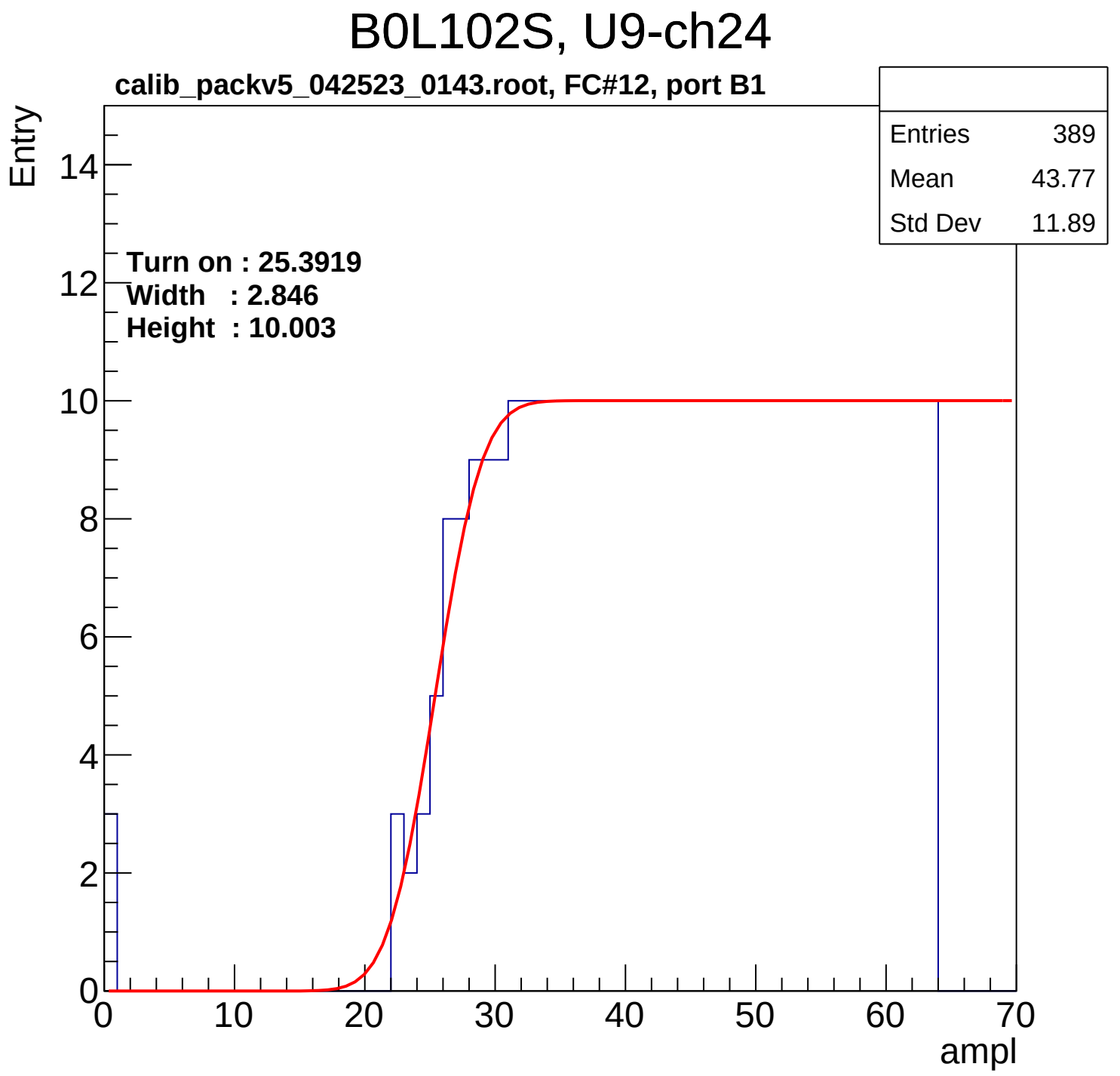

B0L102S, U9-ch19
calib_packv5_042523_0143.root, FC#12, port B1
Entries 391
Mean 43.52
Std Dev 12.31
Turn on : 25.4264
Width : 4.288
Height : 10.074
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

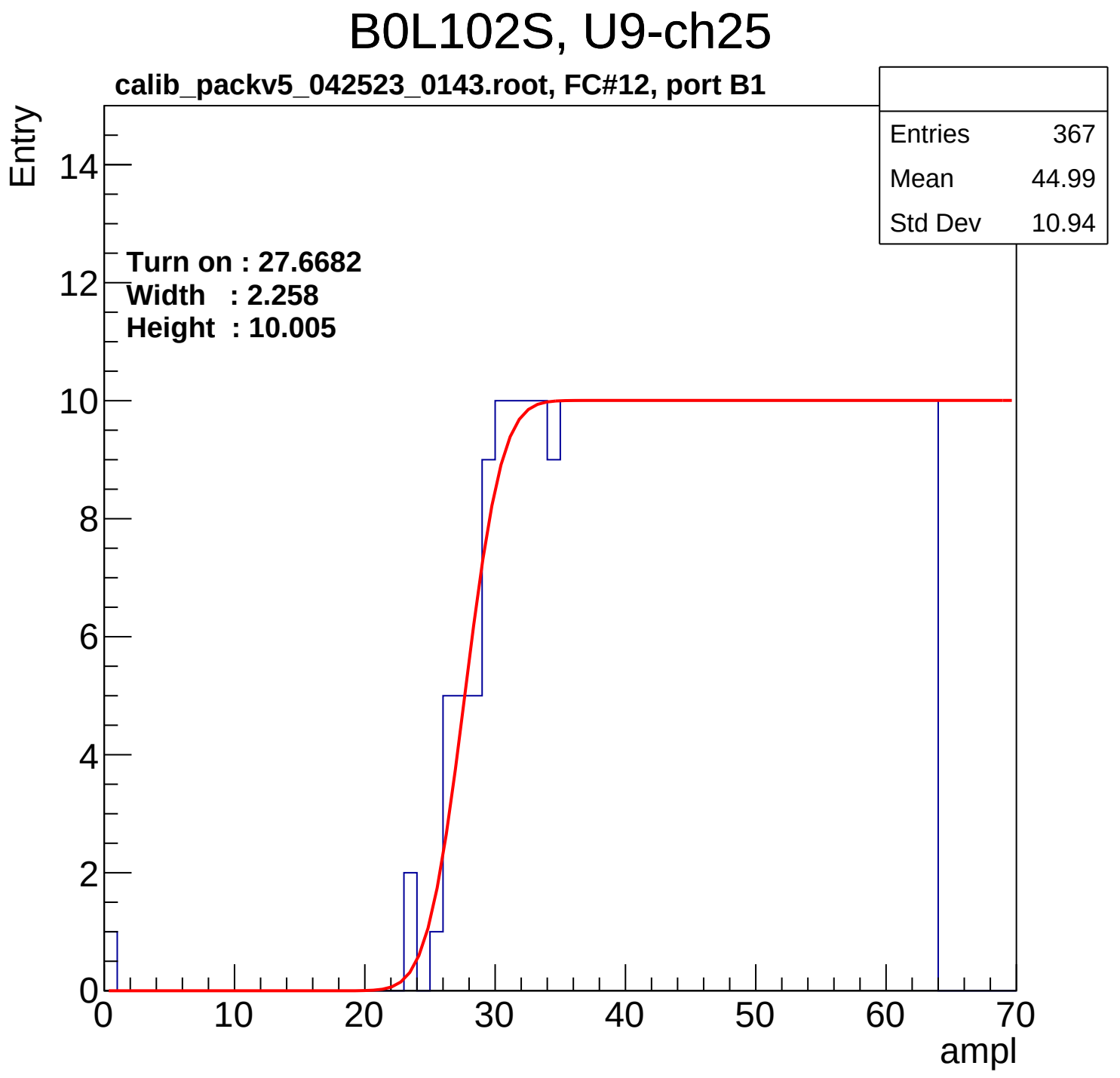

B0L102S, U9-ch20
calib_packv5_042523_0143.root, FC#12, port B1
Entries 393
Mean 43.35
Std Dev 12.53
Turn on : 25.6317
Width : 3.724
Height : 10.055
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

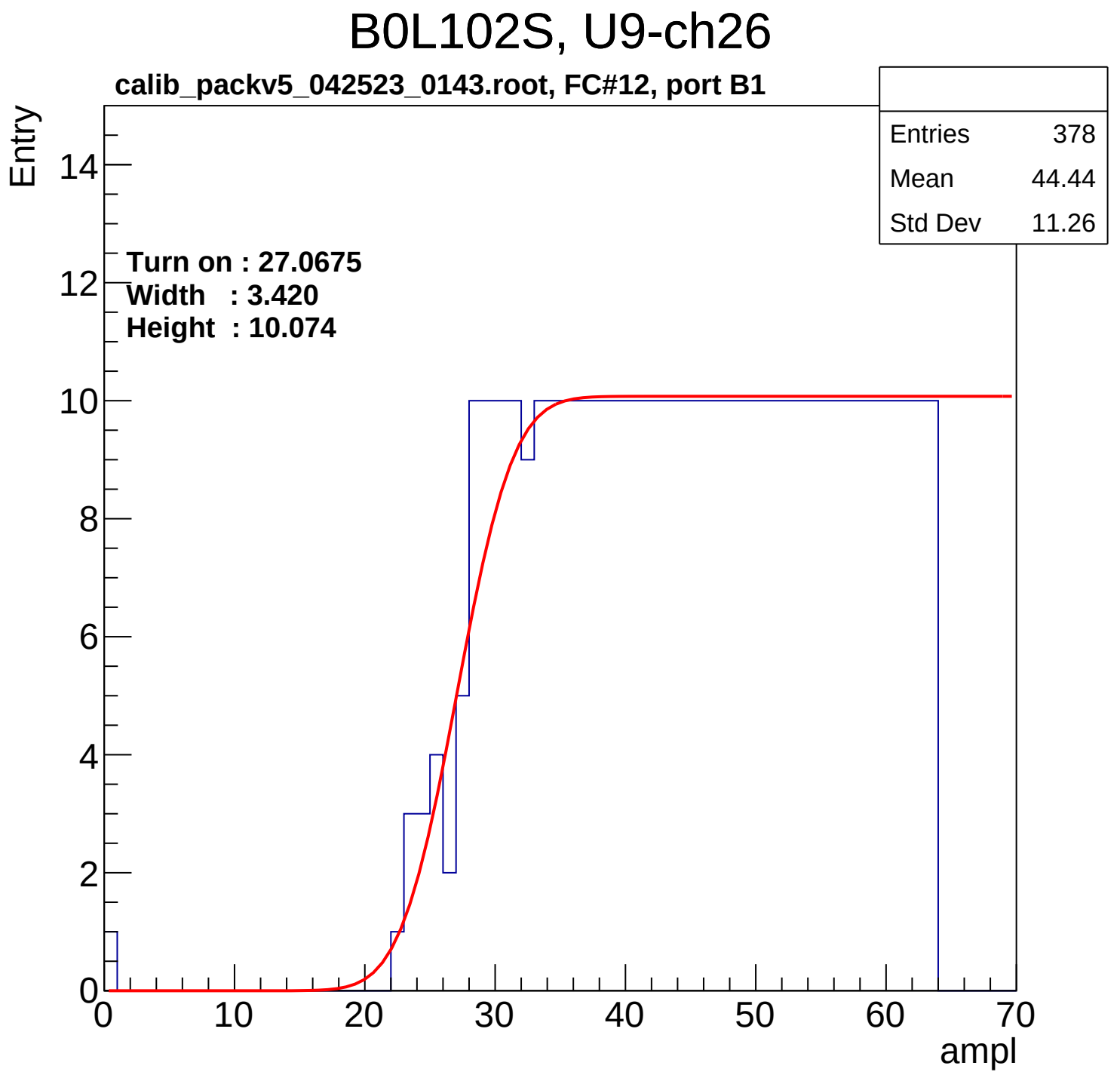

B0L102S, U9-ch21
calib_packv5_042523_0143.root, FC#12, port B1
Entries 389
Mean 43.84
Std Dev 11.72
Turn on : 25.4357
Width : 2.409
Height : 10.020
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

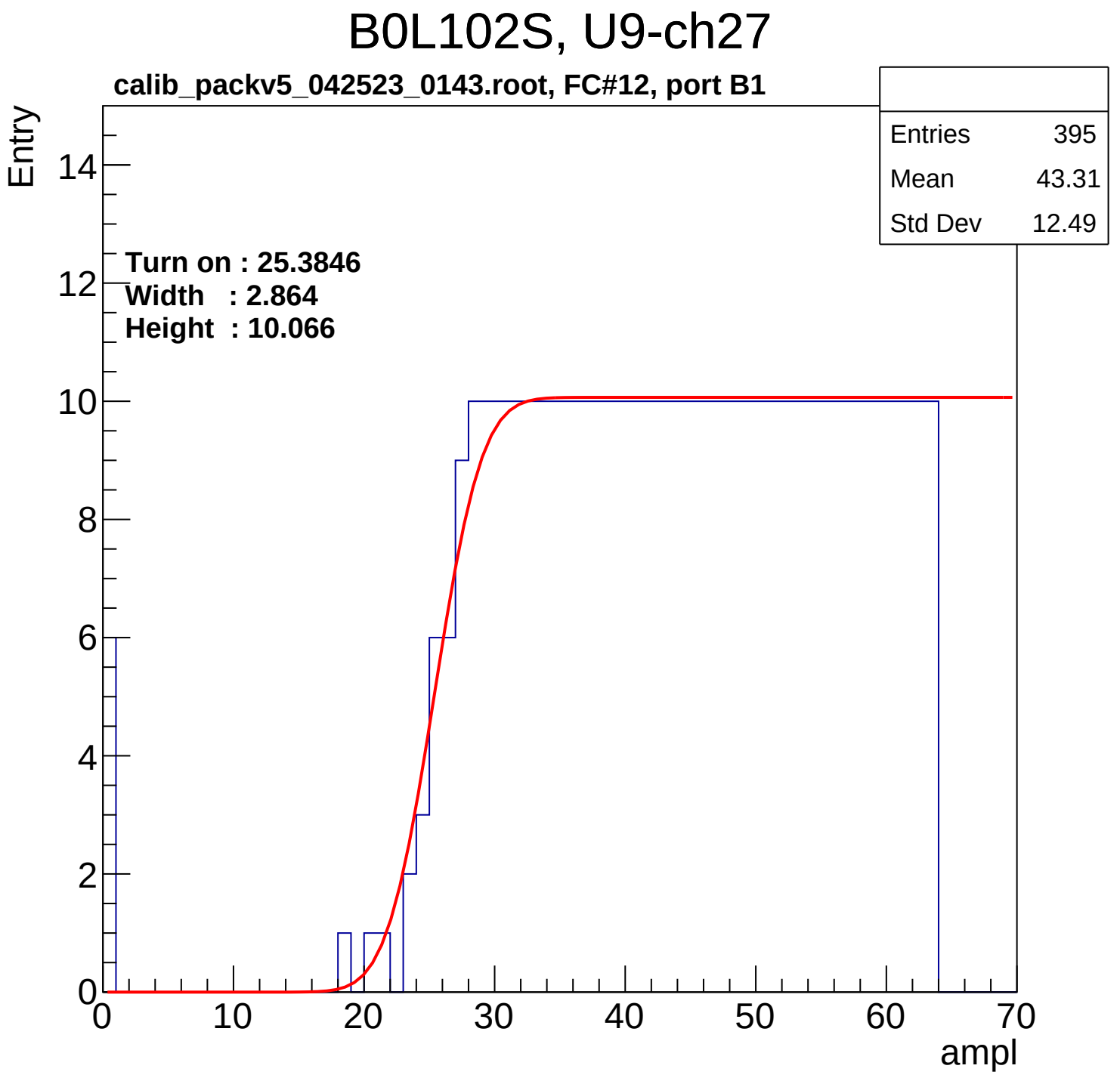

B0L102S, U9-ch22
calib_packv5_042523_0143.root, FC#12, port B1
Entries 381
Mean 44.26
Std Dev 11.39
Turn on : 26.1019
Width : 2.603
Height : 9.912
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

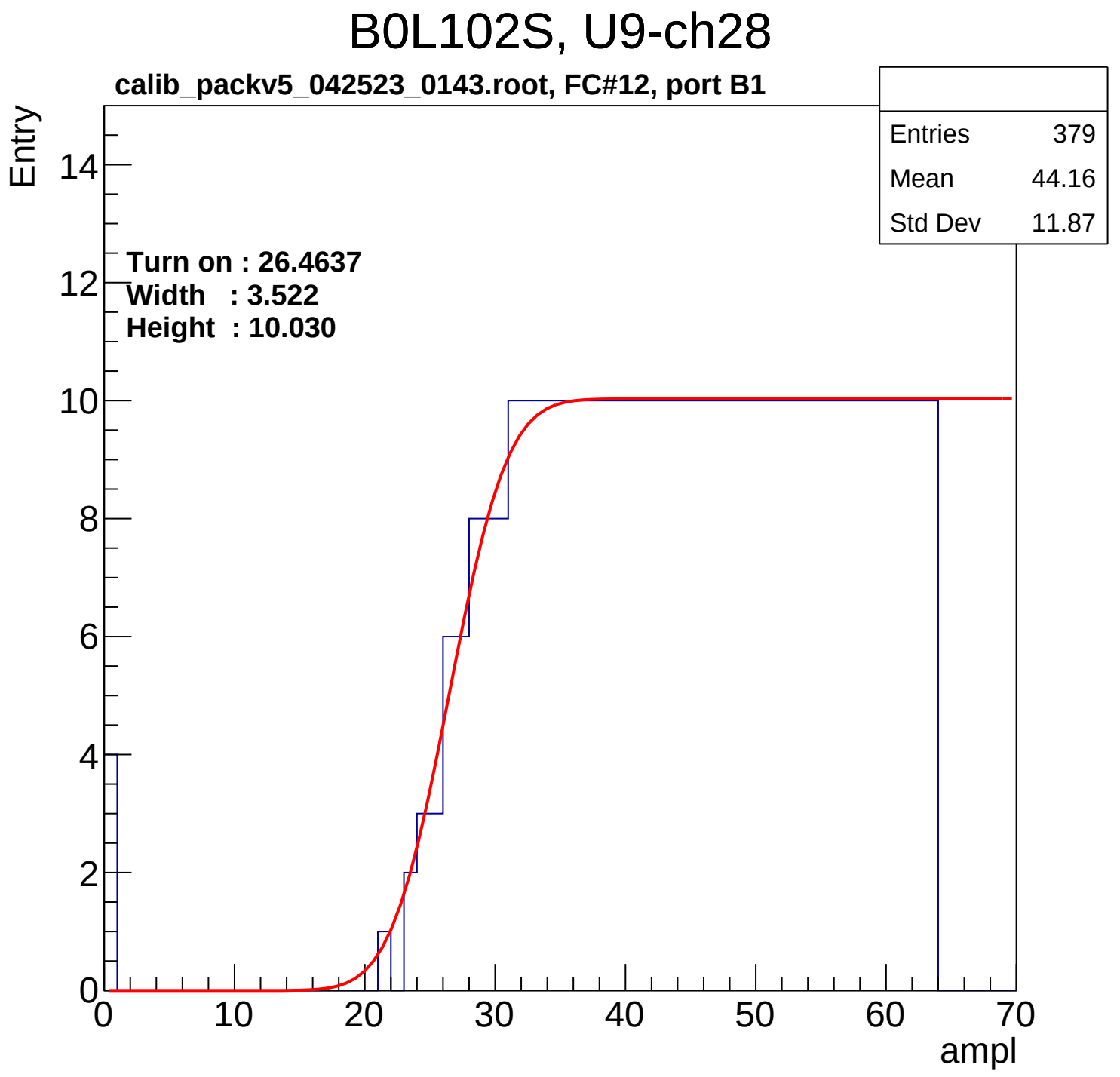

B0L102S, U9-ch23
calib_packv5_042523_0143.root, FC#12, port B1
Entries 358
Mean 45.41
Std Dev 10.75
Turn on : 28.5889
Width : 2.371
Height : 9.978
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

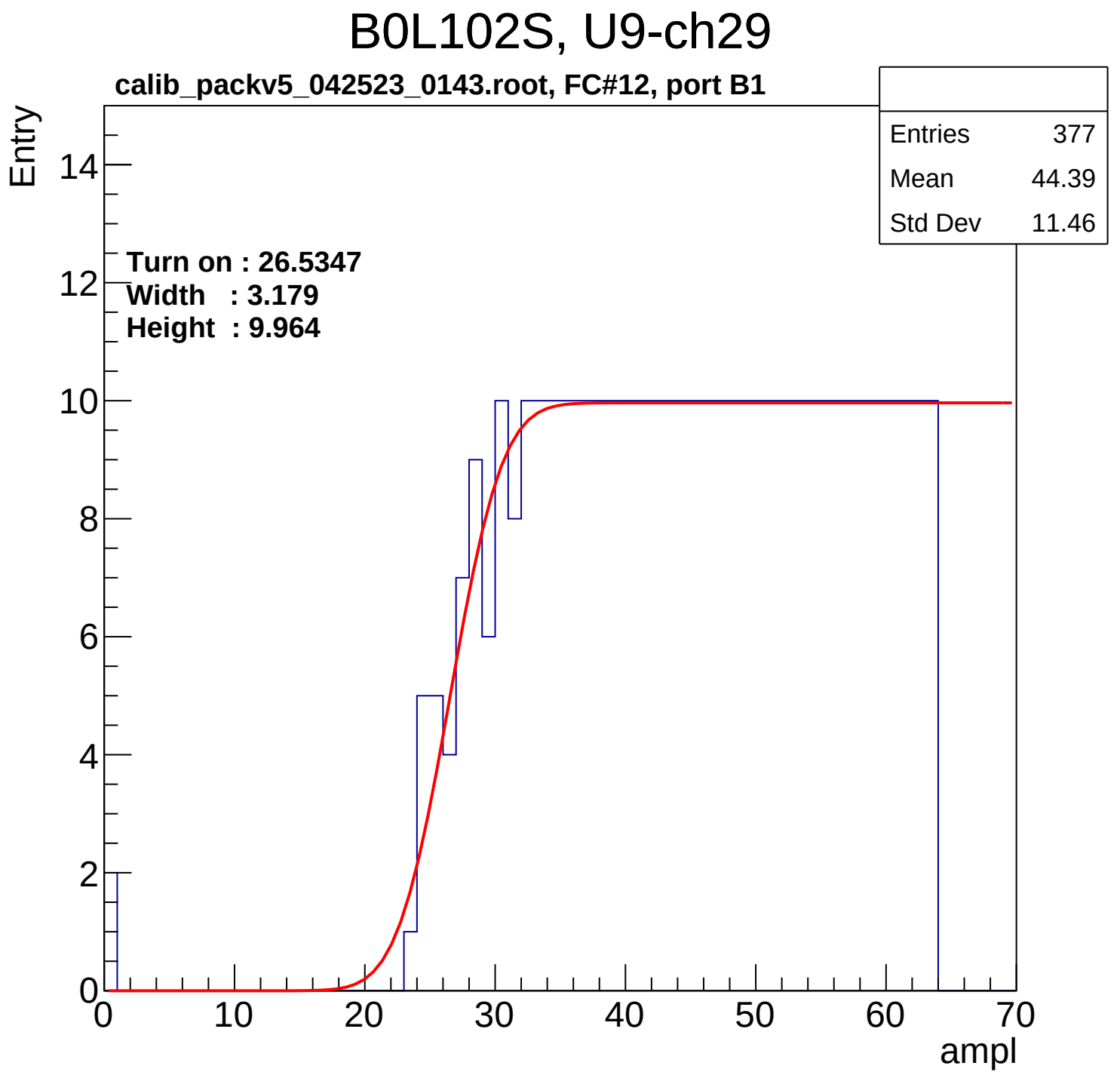

B0L102S, U9-ch24
calib_packv5_042523_0143.root, FC#12, port B1
Entries 389
Mean 43.77
Std Dev 11.89
Turn on : 25.3919
Width : 2.846
Height : 10.003
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

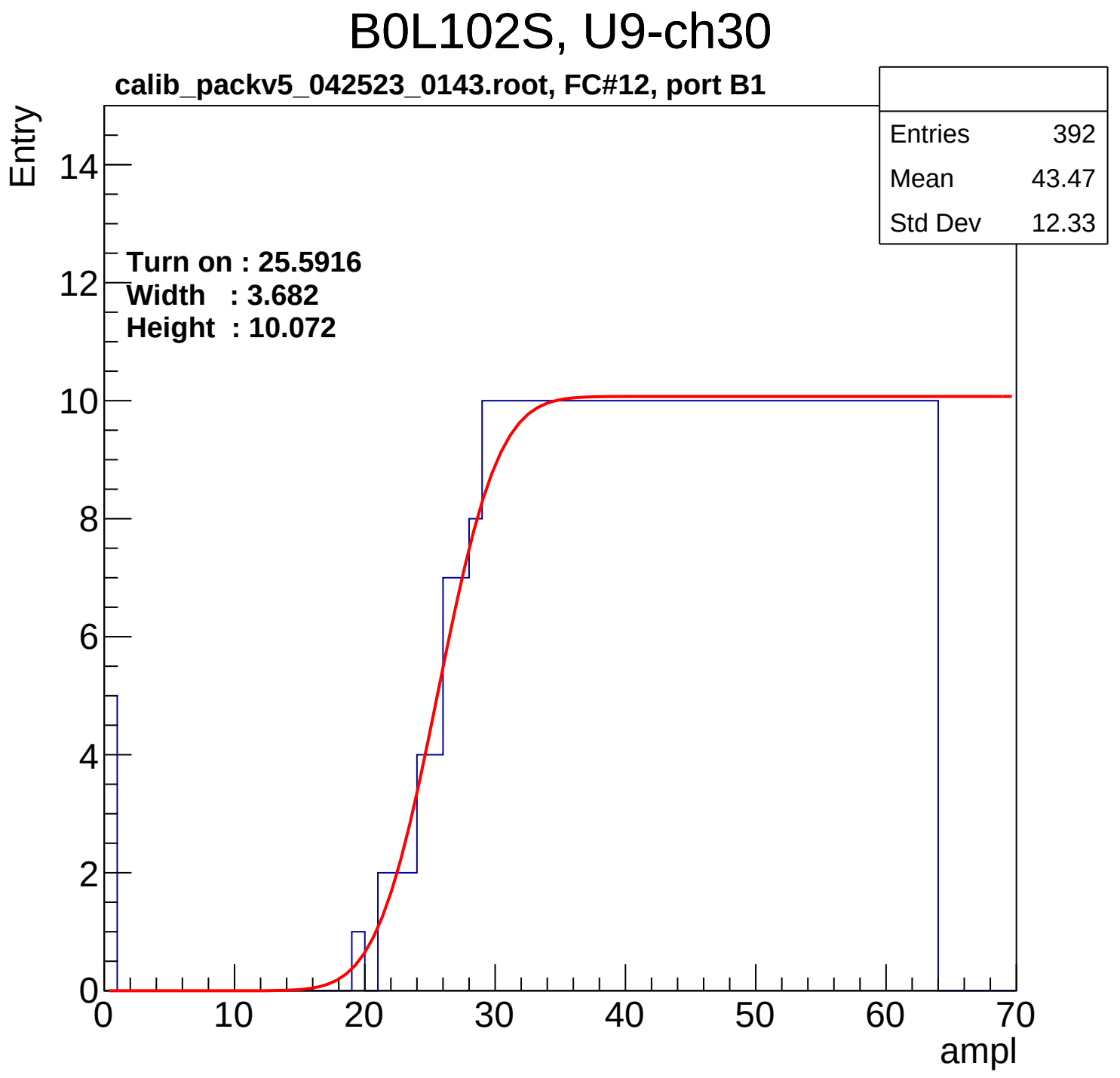

B0L102S, U9-ch25
calib_packv5_042523_0143.root, FC#12, port B1
Entries 367
Mean 44.99
Std Dev 10.94
Turn on : 27.6682
Width : 2.258
Height : 10.005
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

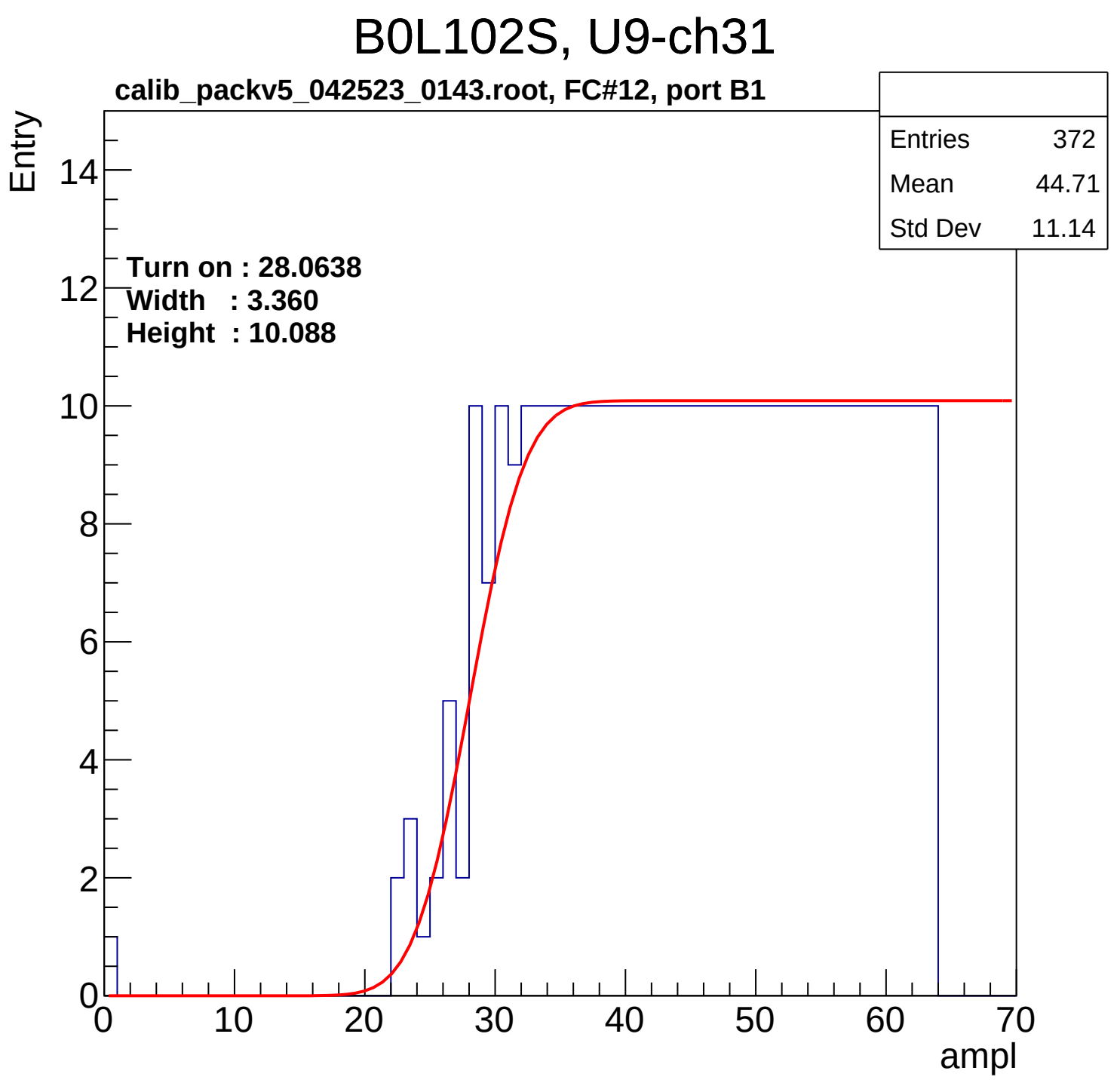

B0L102S, U9-ch26
calib_packv5_042523_0143.root, FC#12, port B1
Entries 378
Mean 44.44
Std Dev 11.26
Turn on : 27.0675
Width : 3.420
Height : 10.074
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

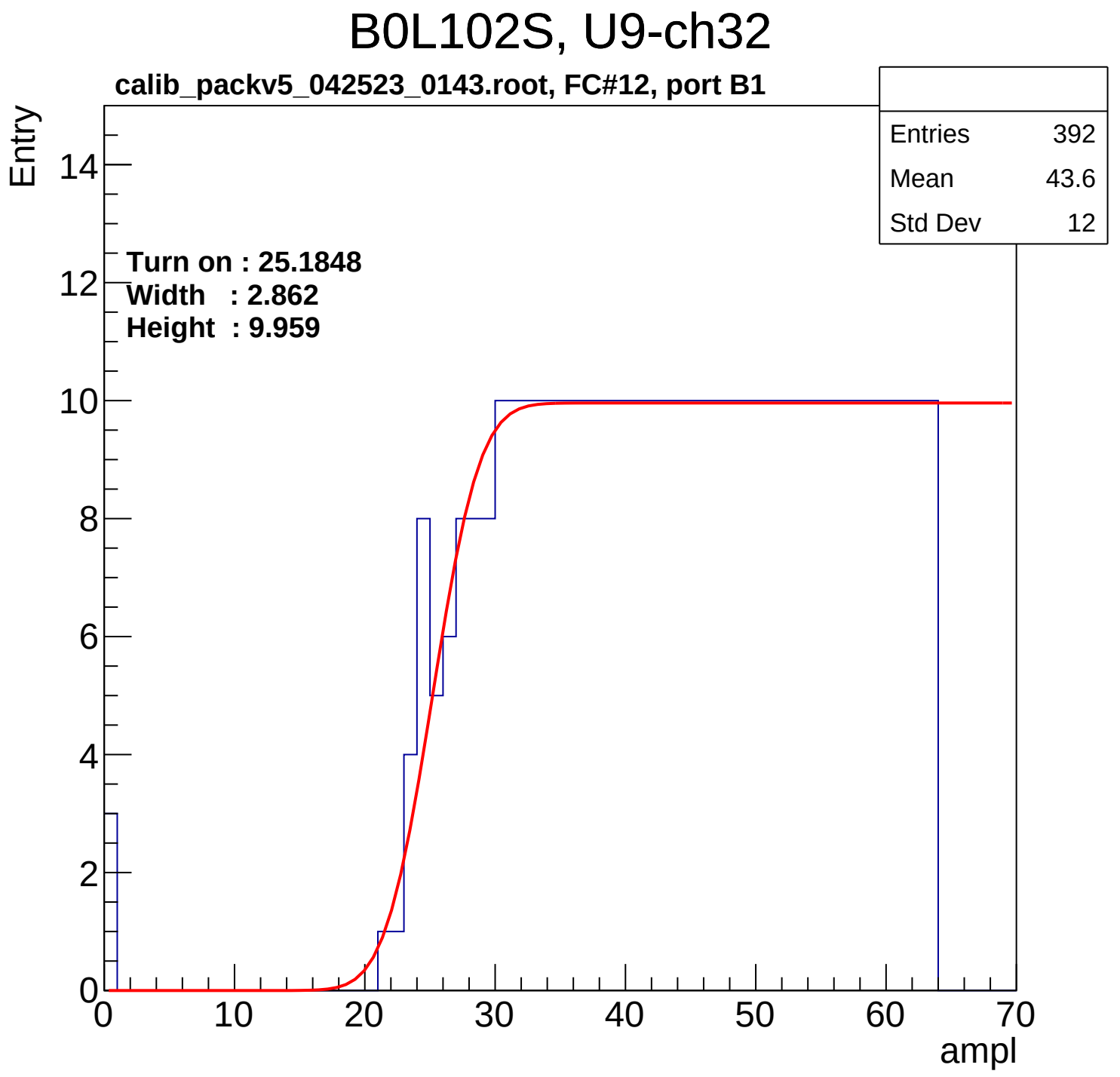

B0L102S, U9-ch27
calib_packv5_042523_0143.root, FC#12, port B1
Entries 395
Mean 43.31
Std Dev 12.49
Turn on : 25.3846
Width : 2.864
Height : 10.066
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

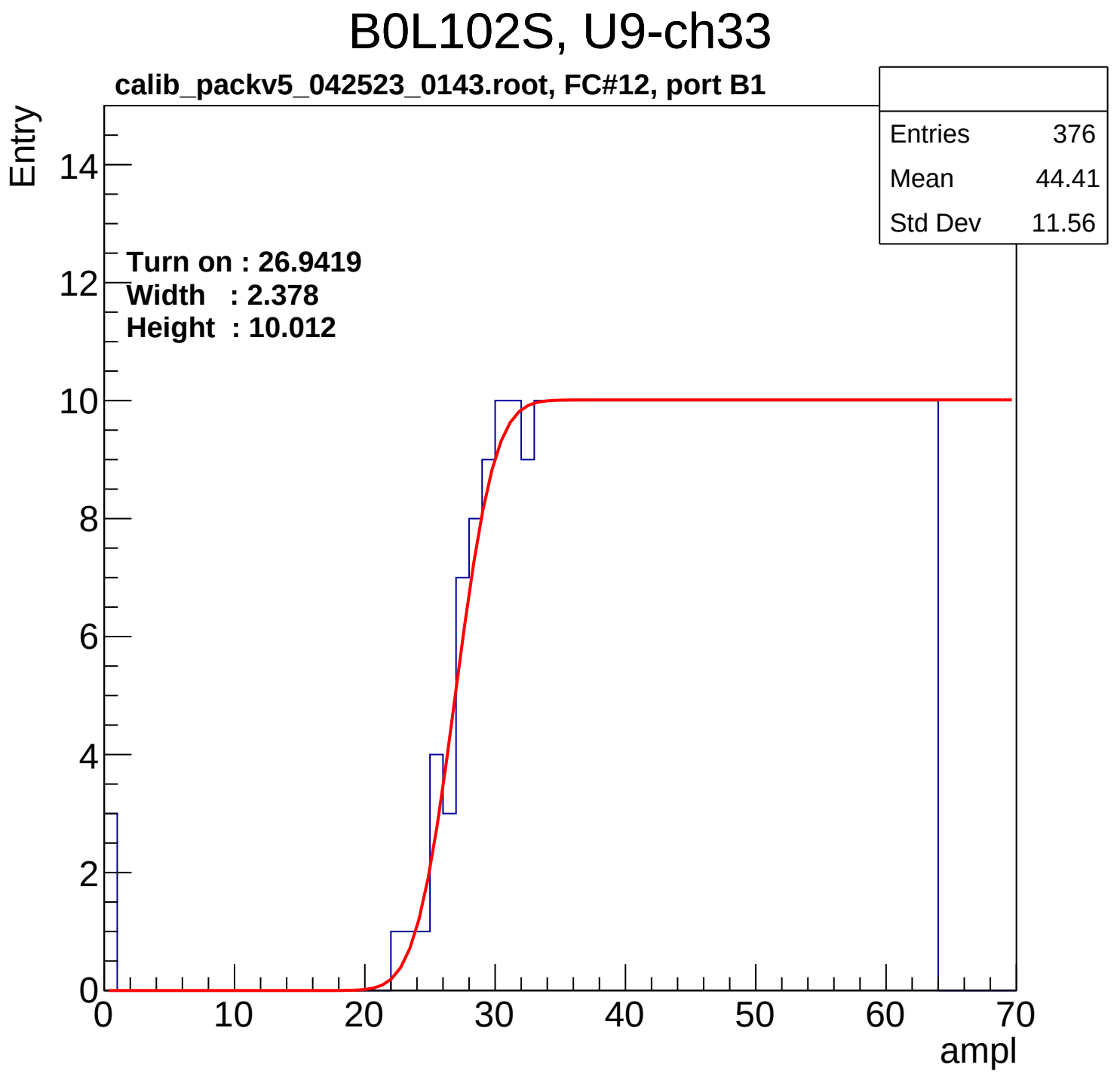

B0L102S, U9-ch28
calib_packv5_042523_0143.root, FC#12, port B1
Entries 379
Mean 44.16
Std Dev 11.87
Turn on : 26.4637
Width : 3.522
Height : 10.030
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

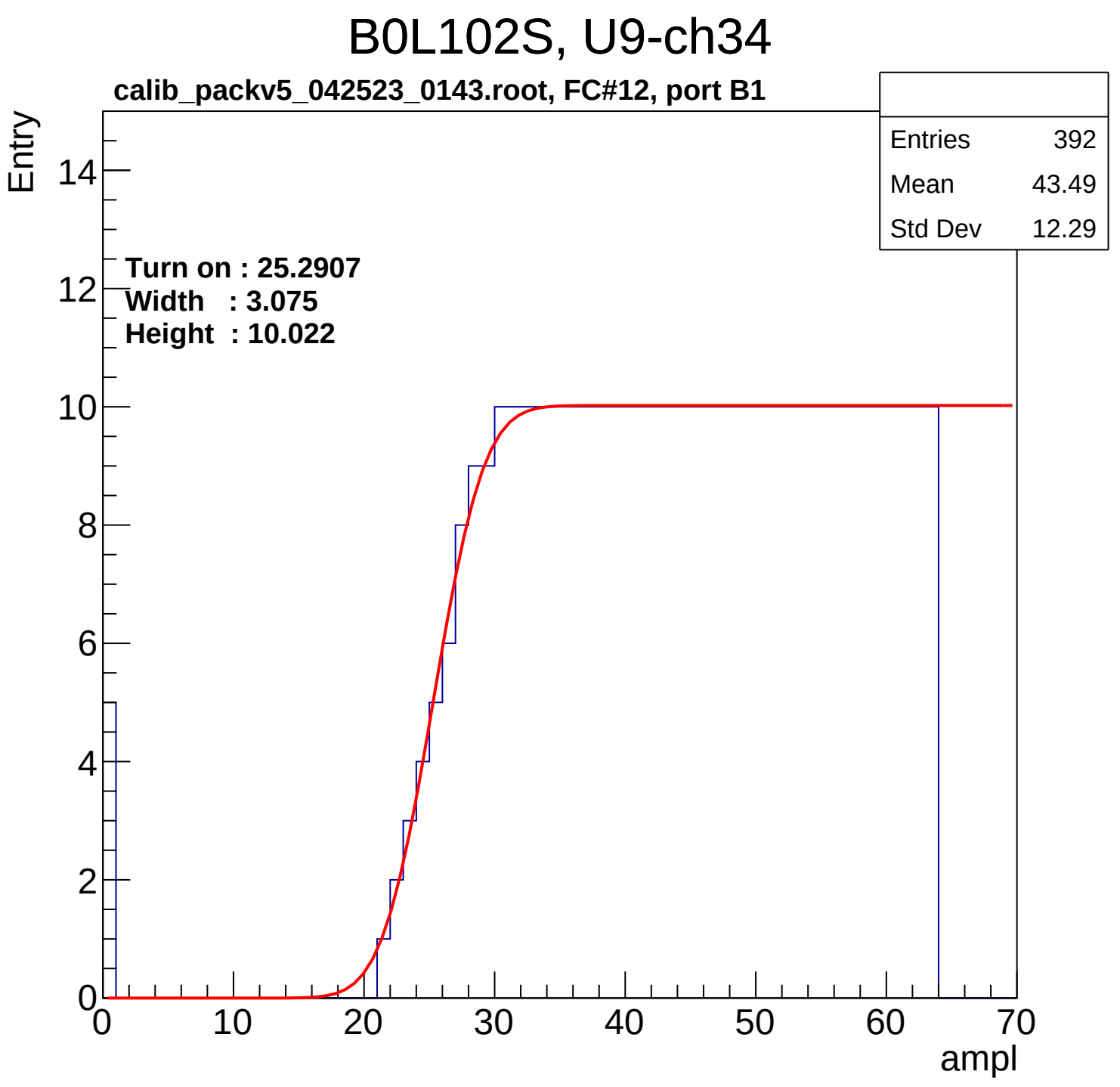

B0L102S, U9-ch29
calib_packv5_042523_0143.root, FC#12, port B1
Entries 377
Mean 44.39
Std Dev 11.46
Turn on : 26.5347
Width : 3.179
Height : 9.964
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

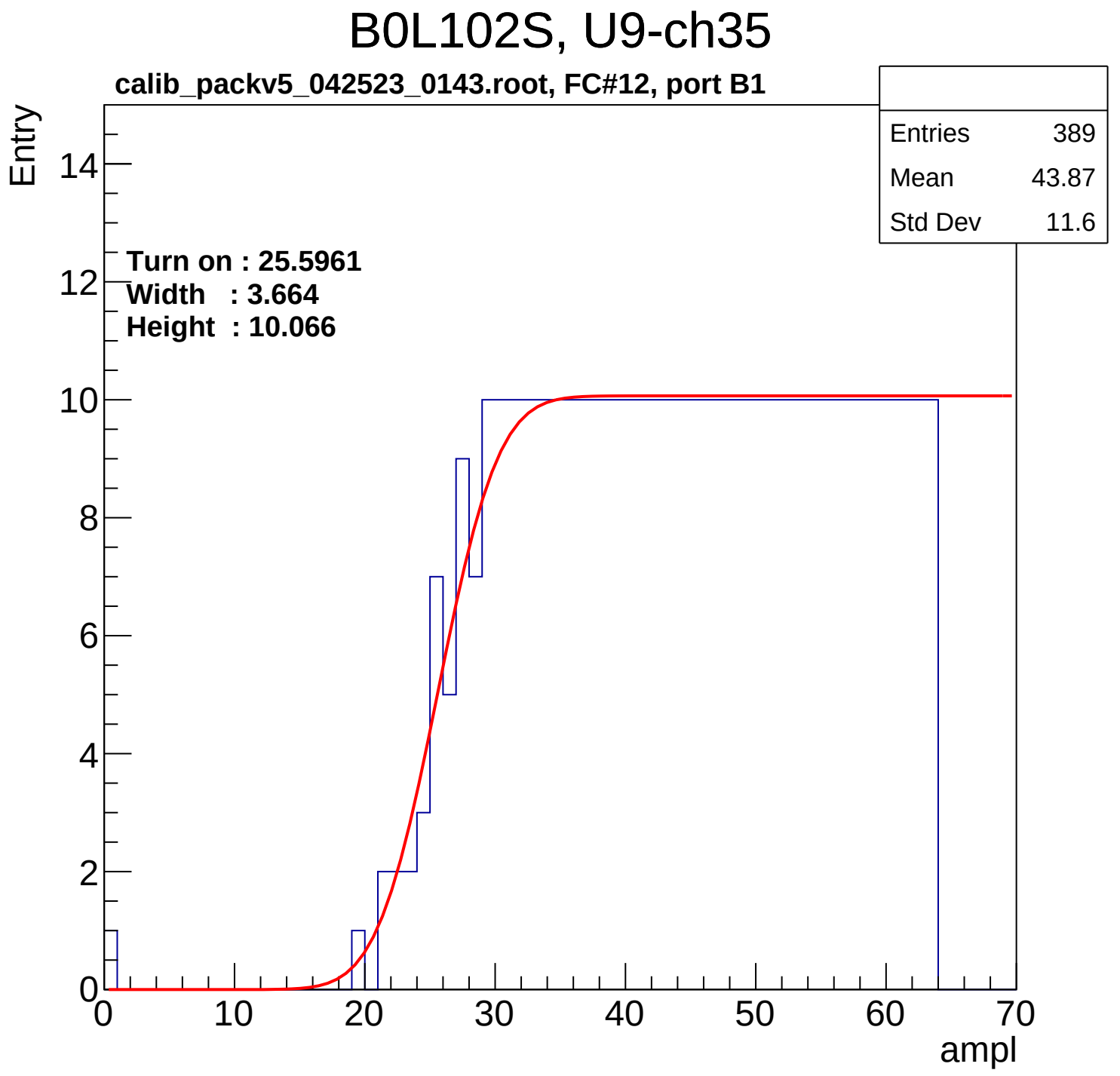

B0L102S, U9-ch30
calib_packv5_042523_0143.root, FC#12, port B1
Entries 392
Mean 43.47
Std Dev 12.33
Turn on : 25.5916
Width : 3.682
Height : 10.072
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

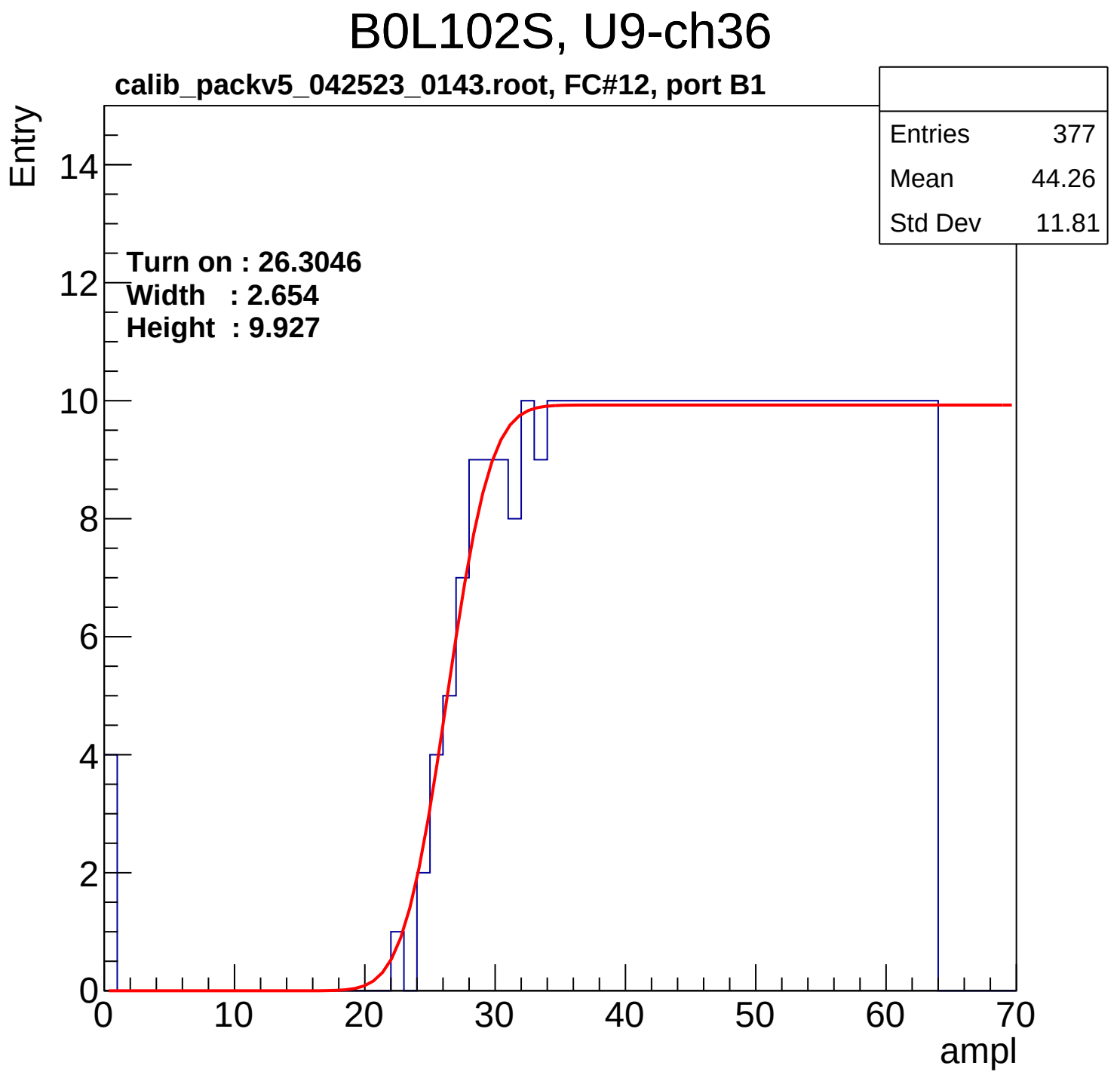

B0L102S, U9-ch31
calib_packv5_042523_0143.root, FC#12, port B1
Entries 372
Mean 44.71
Std Dev 11.14
Turn on : 28.0638
Width : 3.360
Height : 10.088
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

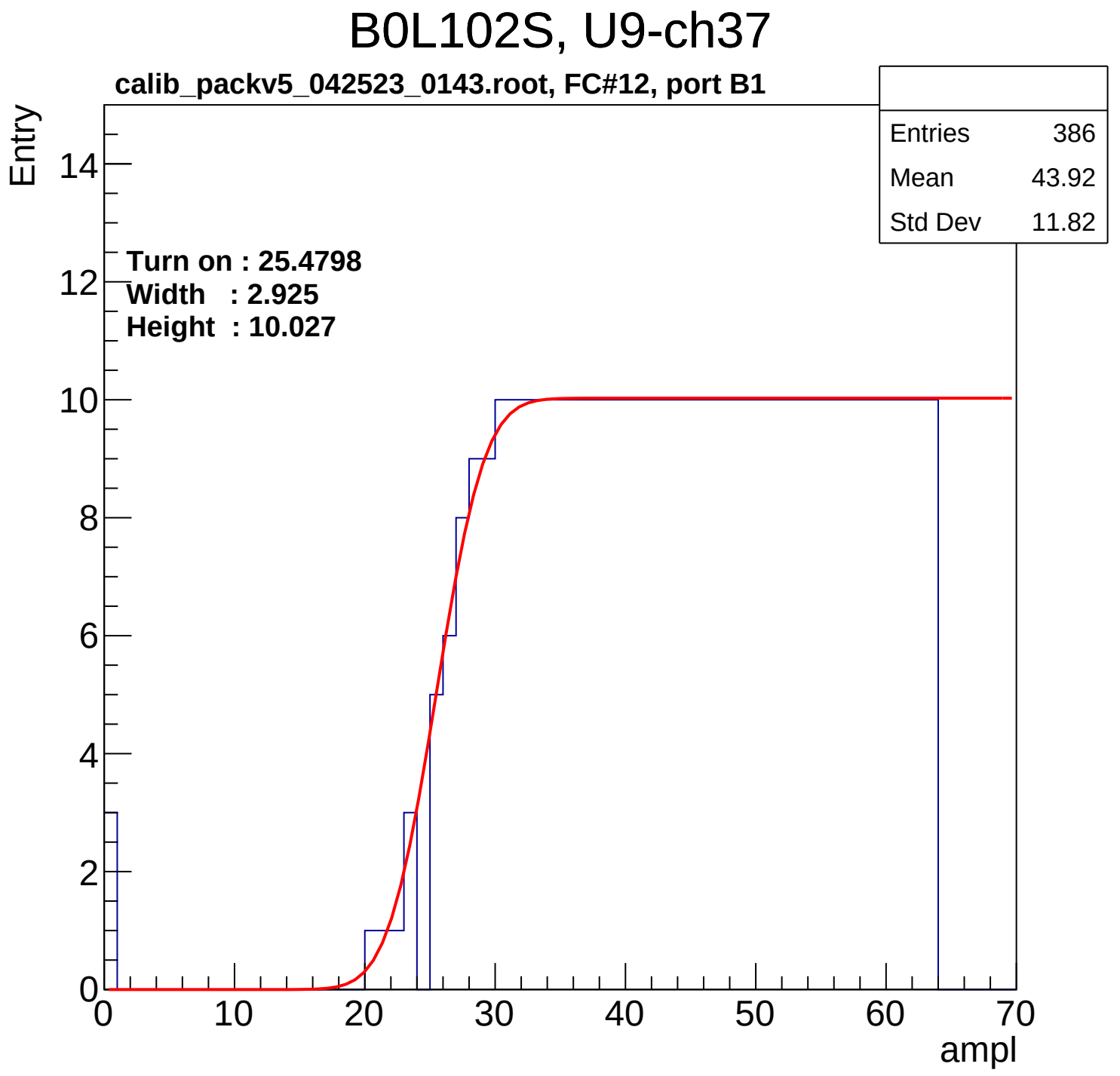

B0L102S, U9-ch32
calib_packv5_042523_0143.root, FC#12, port B1
Entries 392
Mean 43.6
Std Dev 12
Turn on : 25.1848
Width : 2.862
Height : 9.959
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

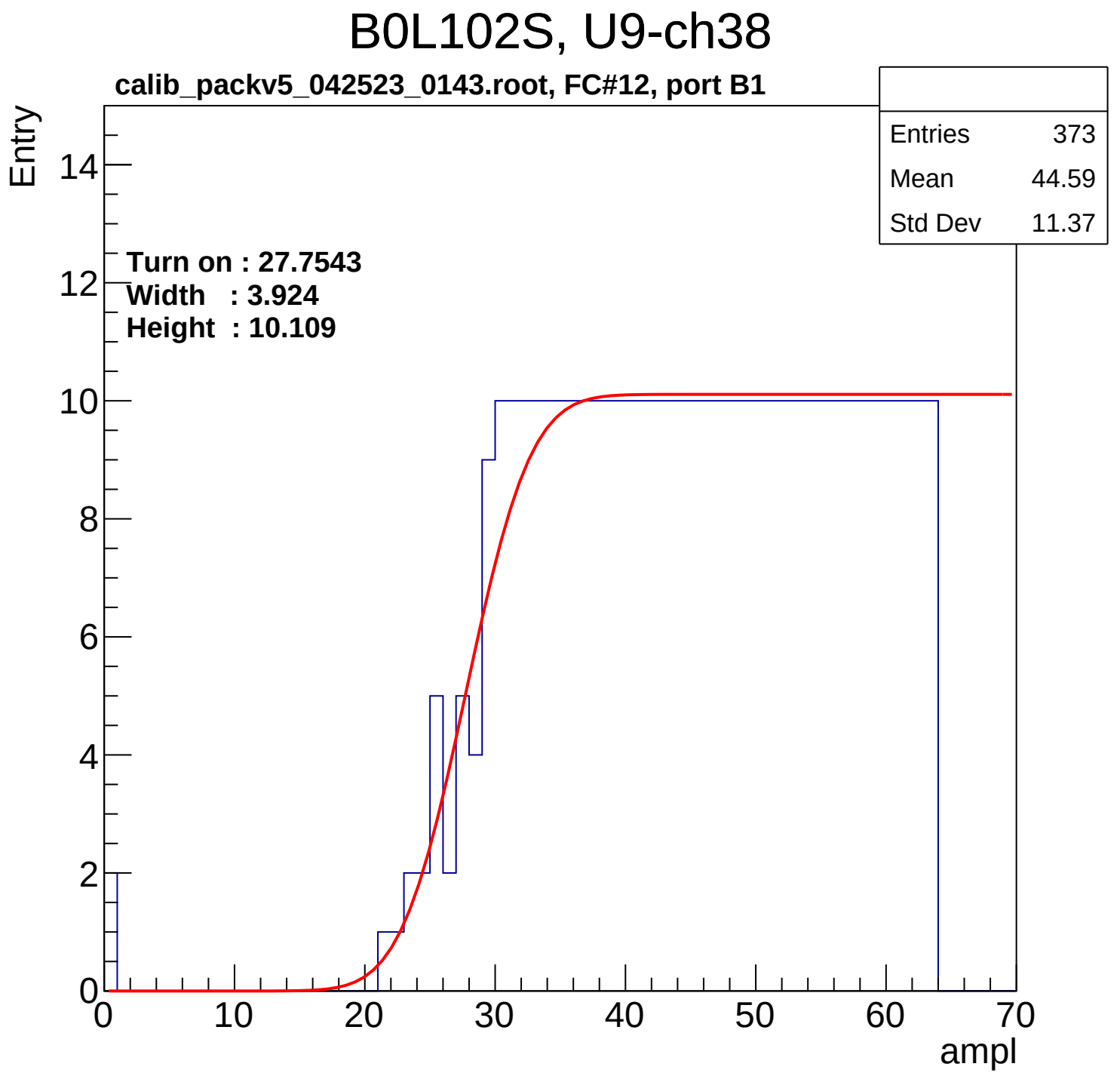

B0L102S, U9-ch33
calib_packv5_042523_0143.root, FC#12, port B1
Entries 376
Mean 44.41
Std Dev 11.56
Turn on : 26.9419
Width : 2.378
Height : 10.012
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

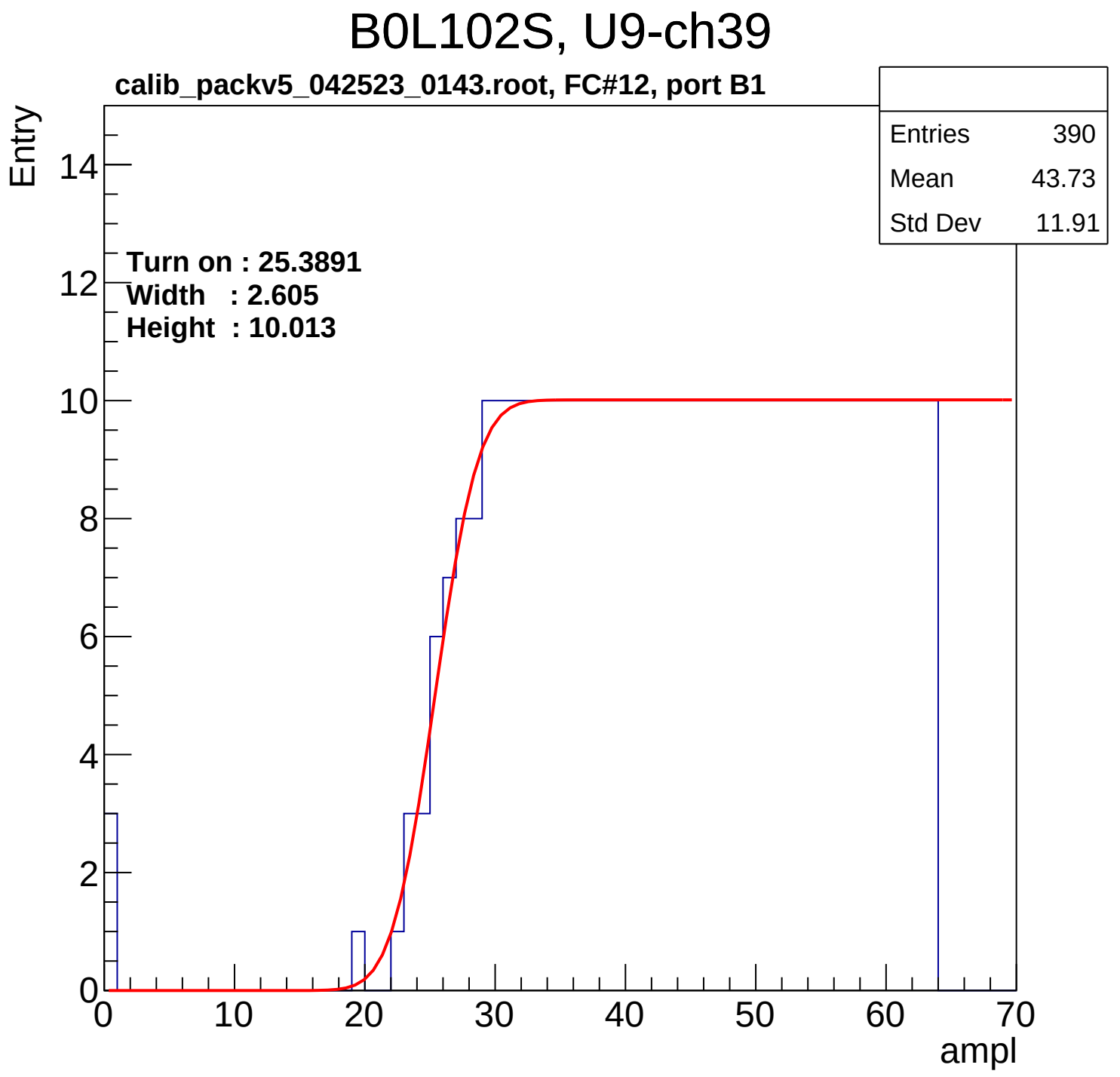

B0L102S, U9-ch34
calib_packv5_042523_0143.root, FC#12, port B1
Entries 392
Mean 43.49
Std Dev 12.29
Turn on : 25.2907
Width : 3.075
Height : 10.022
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

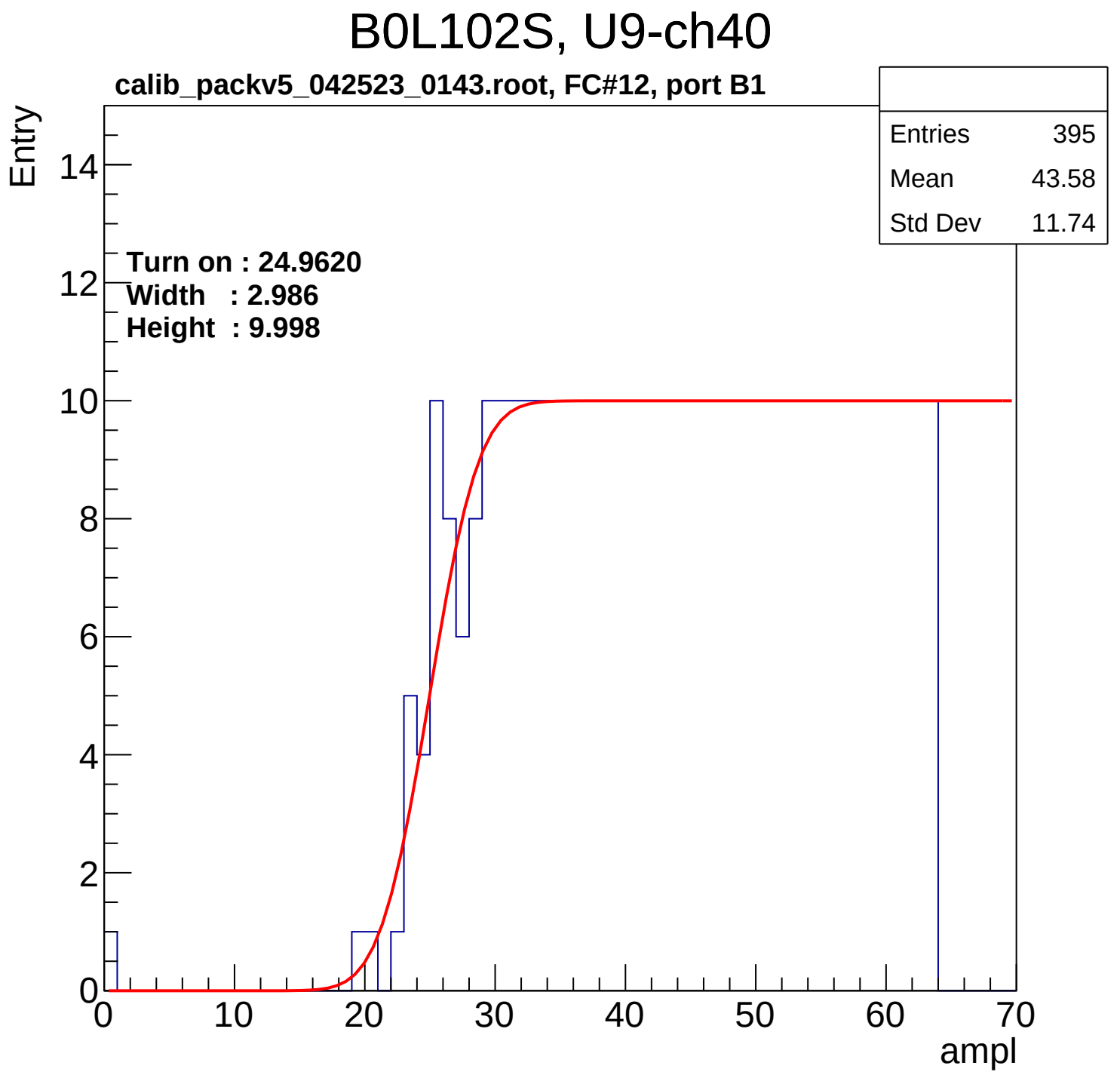

B0L102S, U9-ch35
calib_packv5_042523_0143.root, FC#12, port B1
Entries 389
Mean 43.87
Std Dev 11.6
Turn on : 25.5961
Width : 3.664
Height : 10.066
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

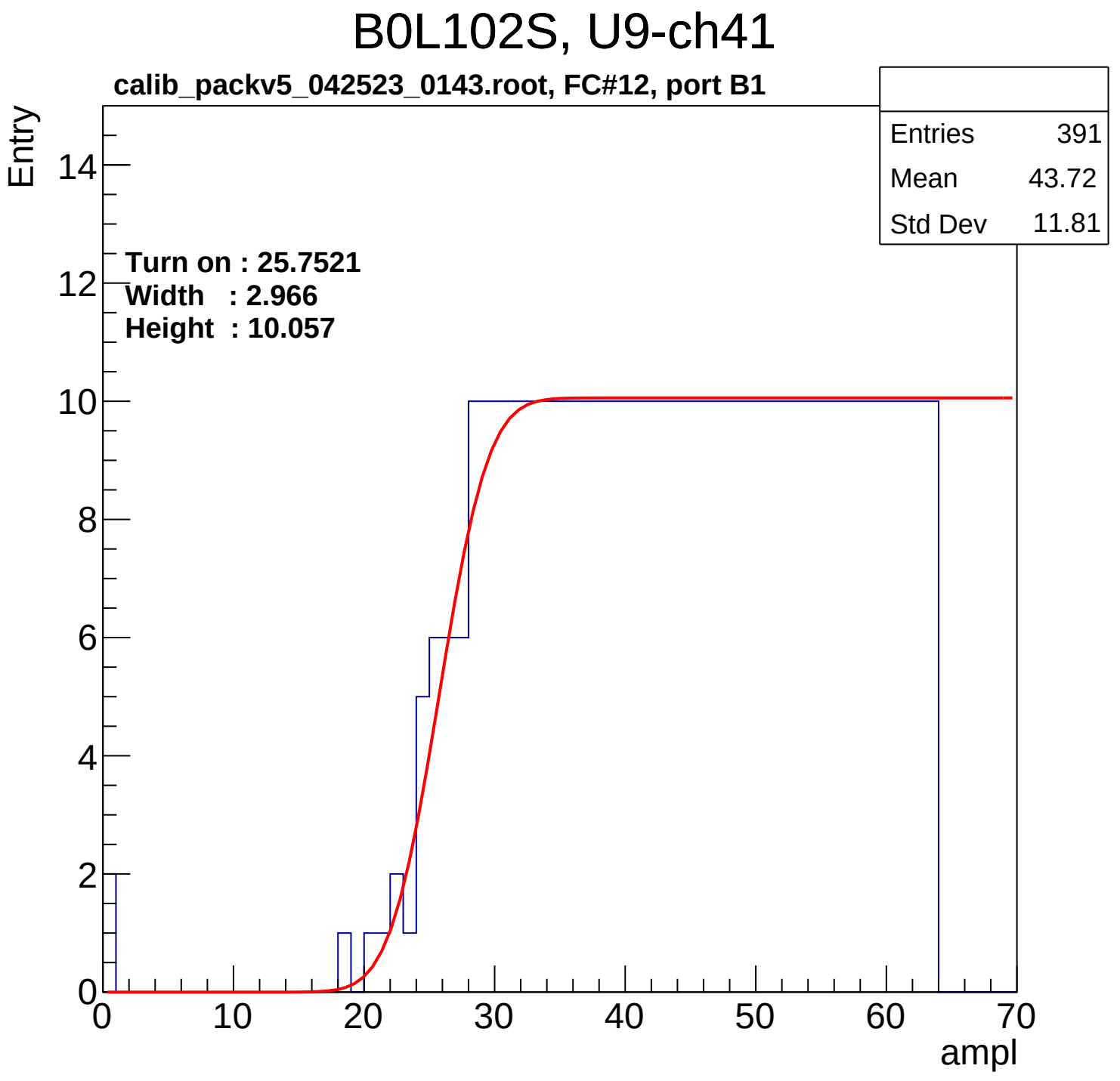

B0L102S, U9-ch36
calib_packv5_042523_0143.root, FC#12, port B1
Entries 377
Mean 44.26
Std Dev 11.81
Turn on : 26.3046
Width : 2.654
Height : 9.927
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

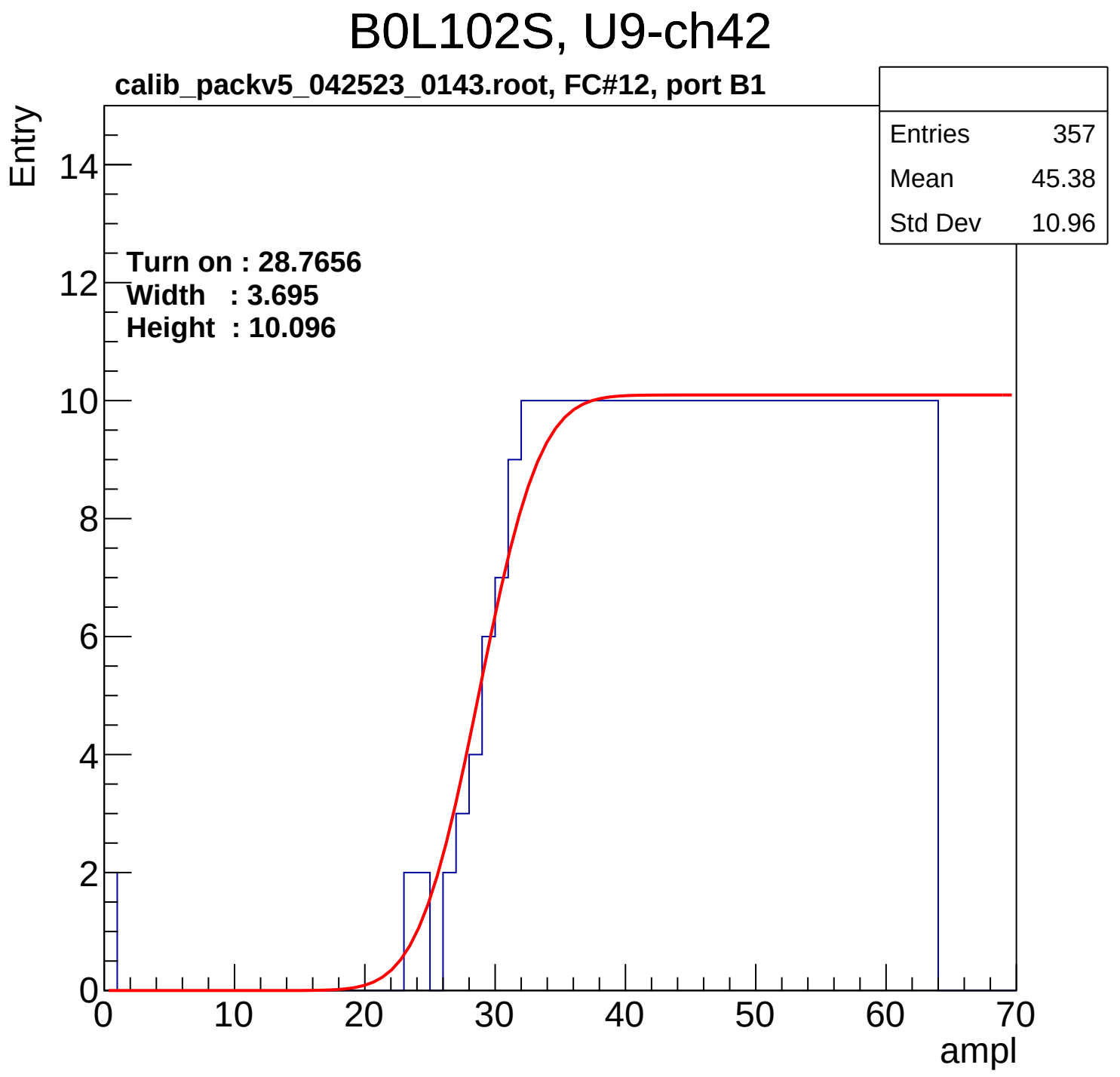

B0L102S, U9-ch37
calib_packv5_042523_0143.root, FC#12, port B1
Entries 386
Mean 43.92
Std Dev 11.82
Turn on : 25.4798
Width : 2.925
Height : 10.027
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

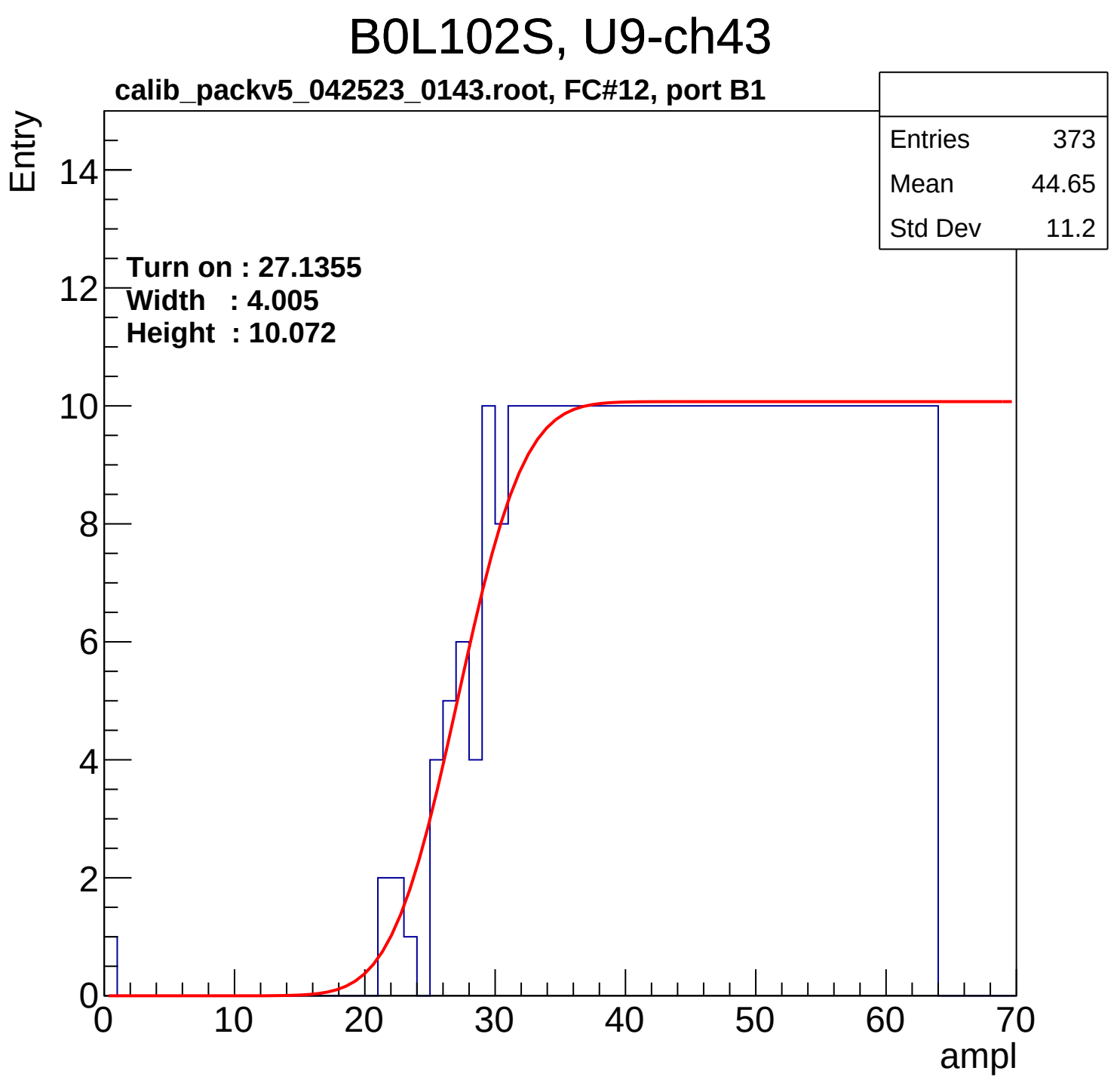

B0L102S, U9-ch38
calib_packv5_042523_0143.root, FC#12, port B1
Entries 373
Mean 44.59
Std Dev 11.37
Turn on : 27.7543
Width : 3.924
Height : 10.109
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

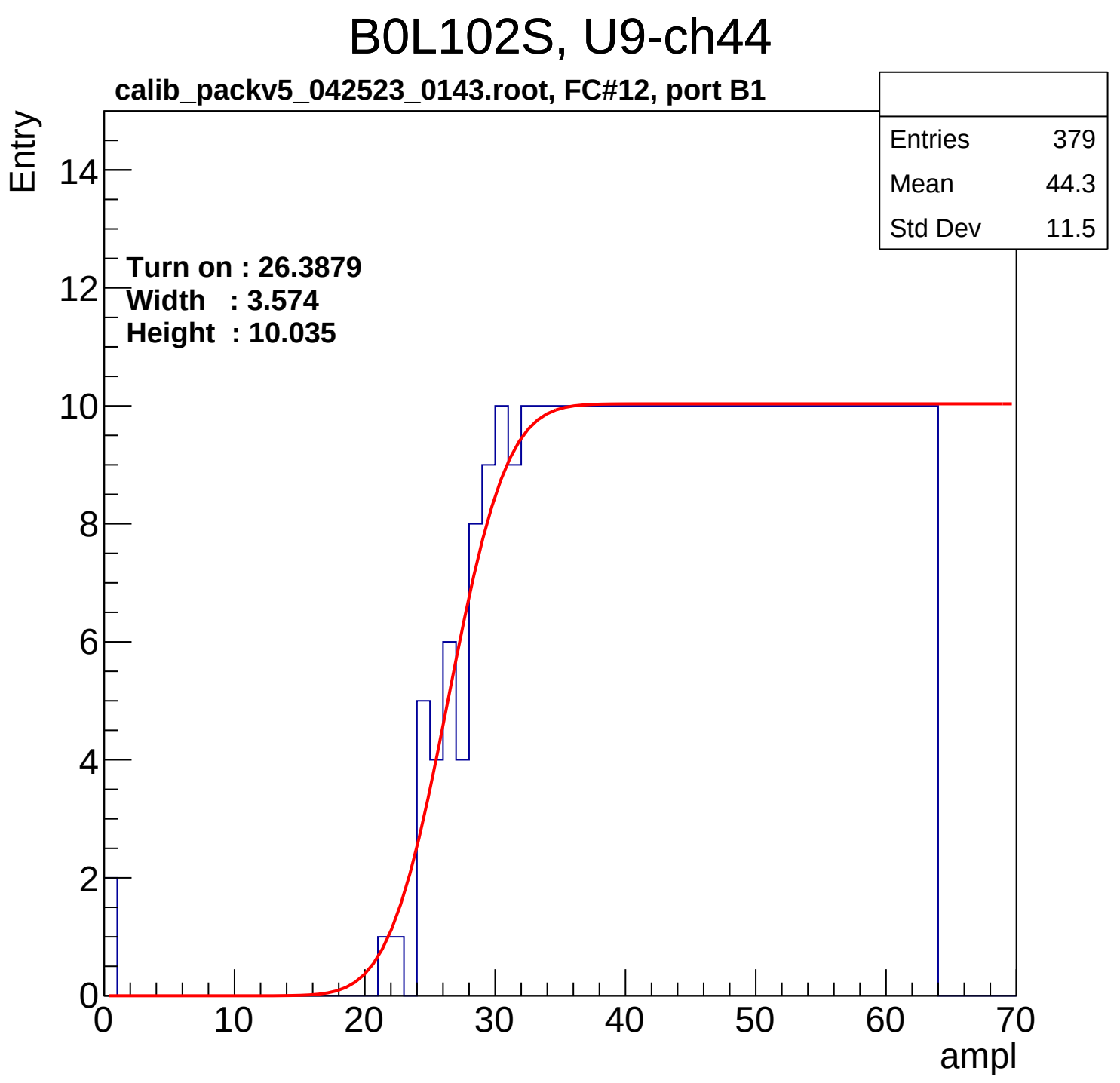

B0L102S, U9-ch39
calib_packv5_042523_0143.root, FC#12, port B1
Entries 390
Mean 43.73
Std Dev 11.91
Turn on : 25.3891
Width : 2.605
Height : 10.013
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

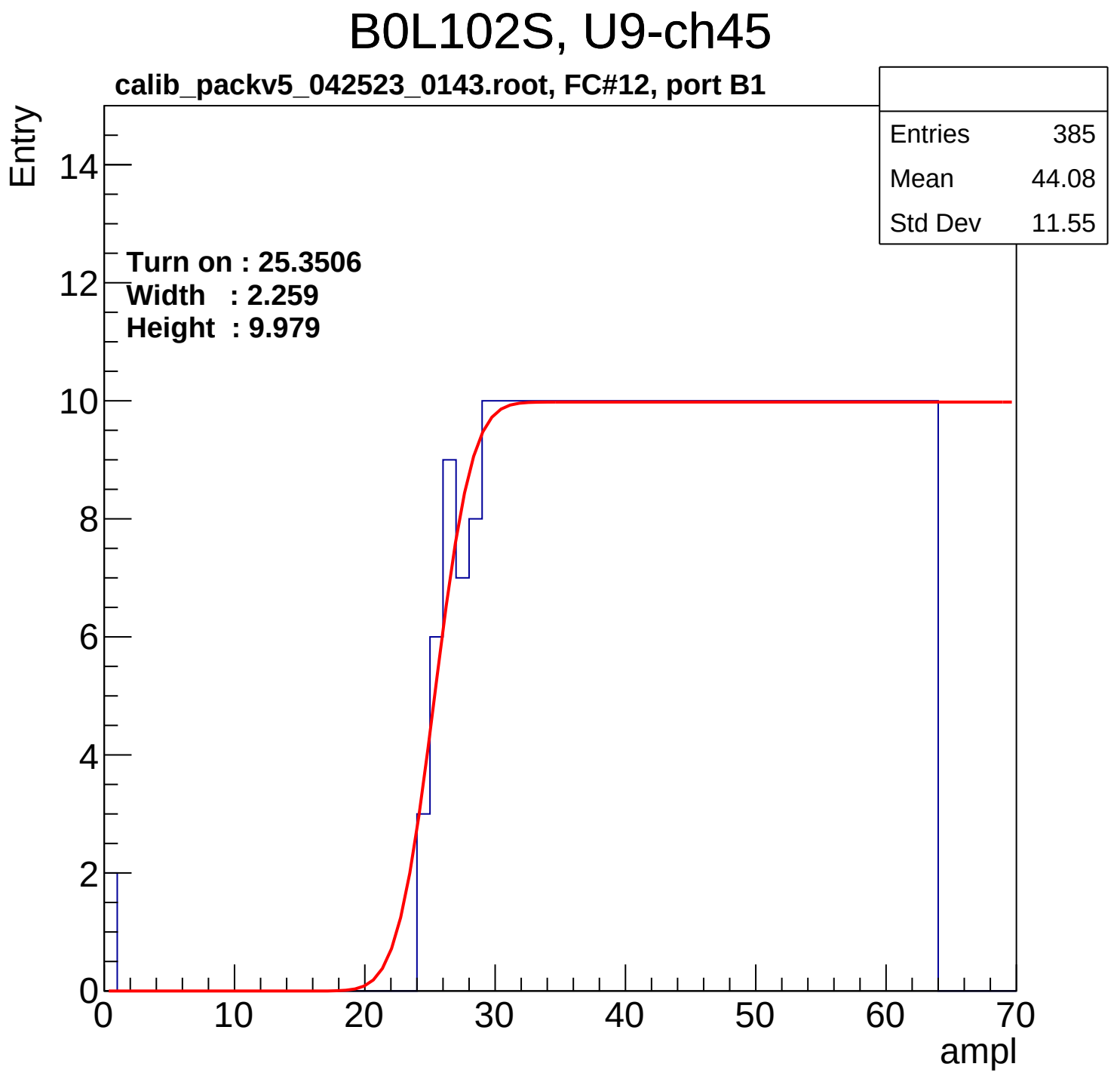

B0L102S, U9-ch40
calib_packv5_042523_0143.root, FC#12, port B1
Entries 395
Mean 43.58
Std Dev 11.74
Turn on : 24.9620
Width : 2.986
Height : 9.998
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

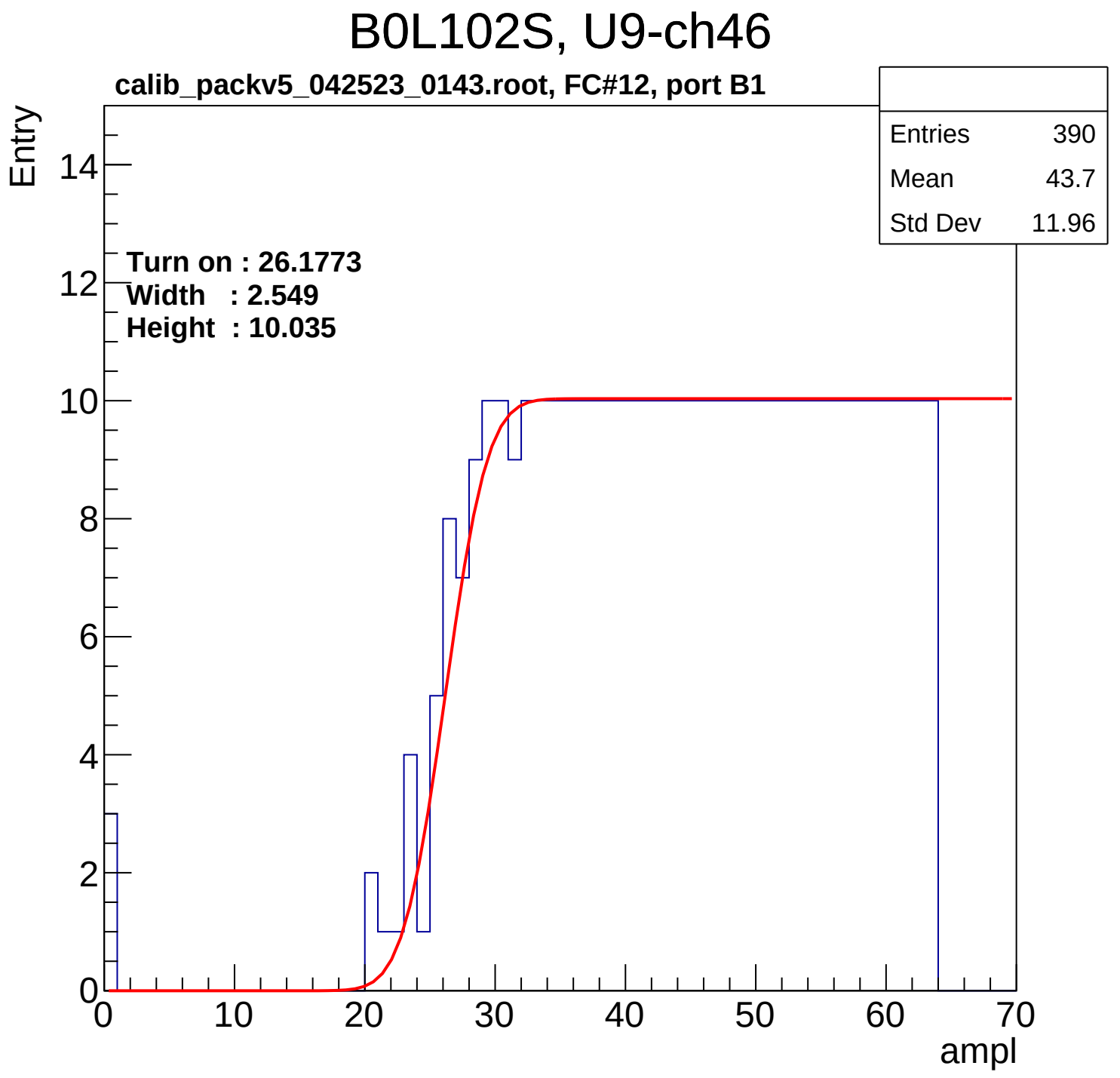

B0L102S, U9-ch41
calib_packv5_042523_0143.root, FC#12, port B1
Entries 391
Mean 43.72
Std Dev 11.81
Turn on : 25.7521
Width : 2.966
Height : 10.057
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

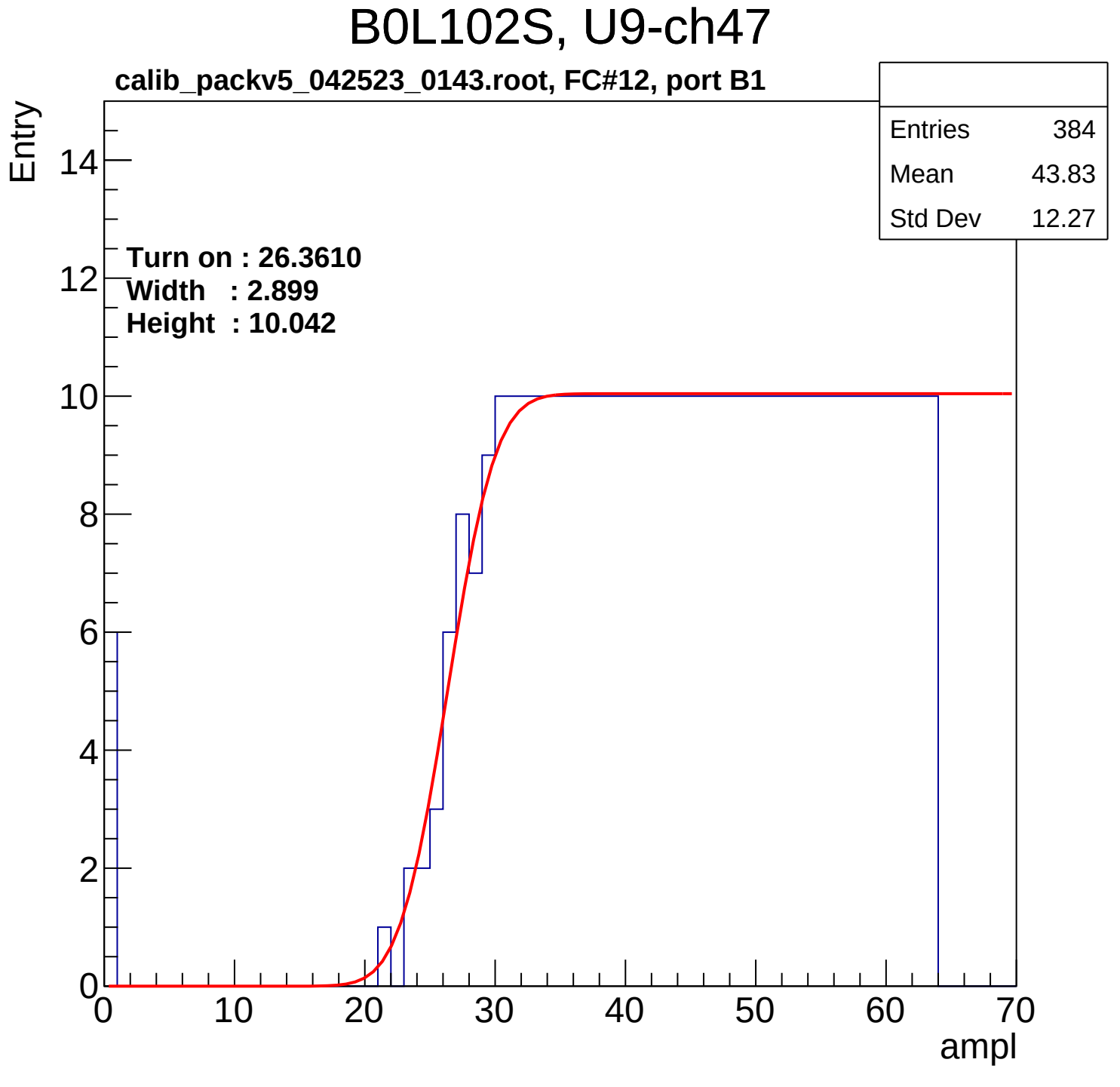

B0L102S, U9-ch42
calib_packv5_042523_0143.root, FC#12, port B1
Entries 357
Mean 45.38
Std Dev 10.96
Turn on : 28.7656
Width : 3.695
Height : 10.096
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

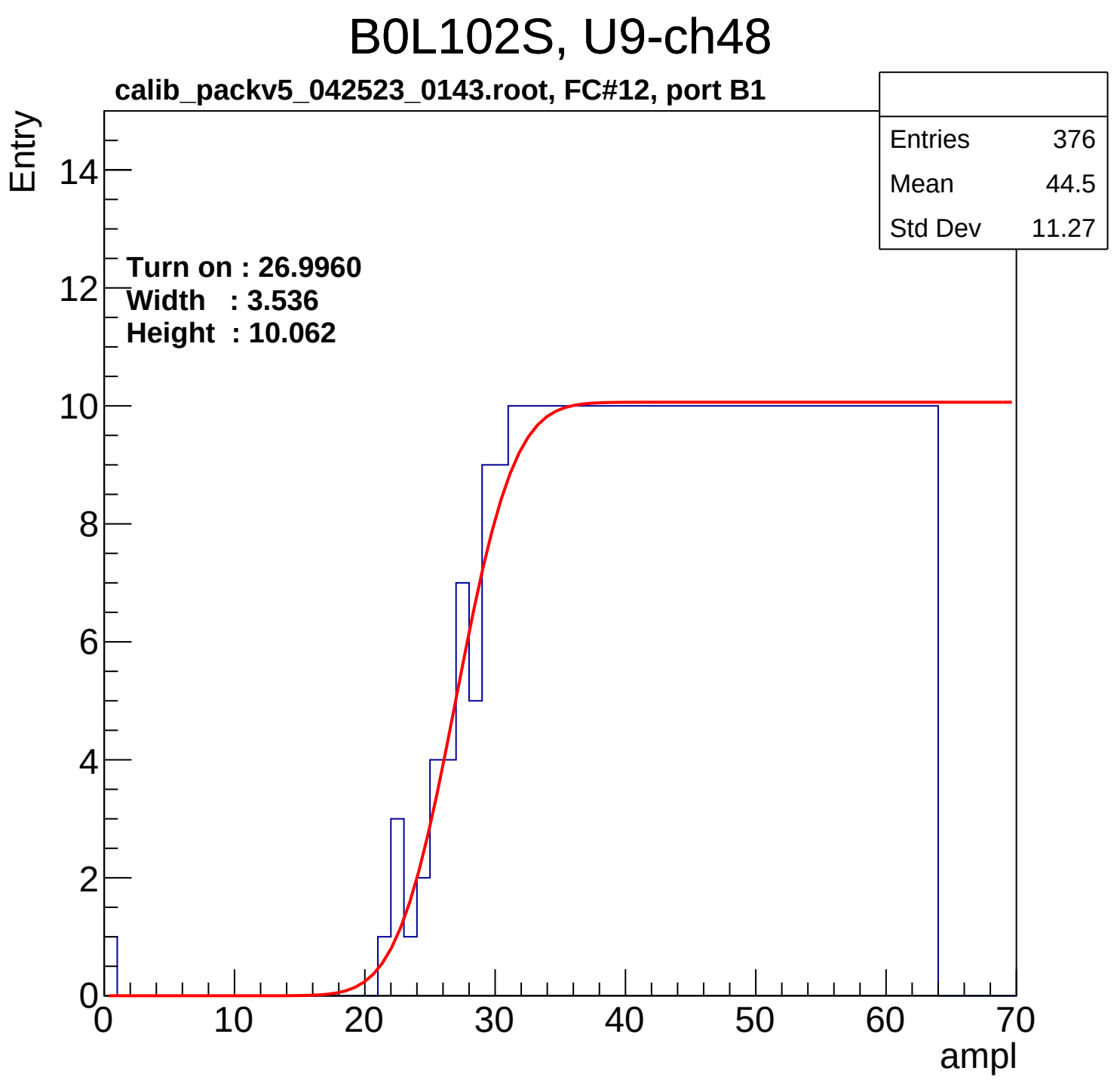

B0L102S, U9-ch43
calib_packv5_042523_0143.root, FC#12, port B1
Entries 373
Mean 44.65
Std Dev 11.2
Turn on : 27.1355
Width : 4.005
Height : 10.072
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

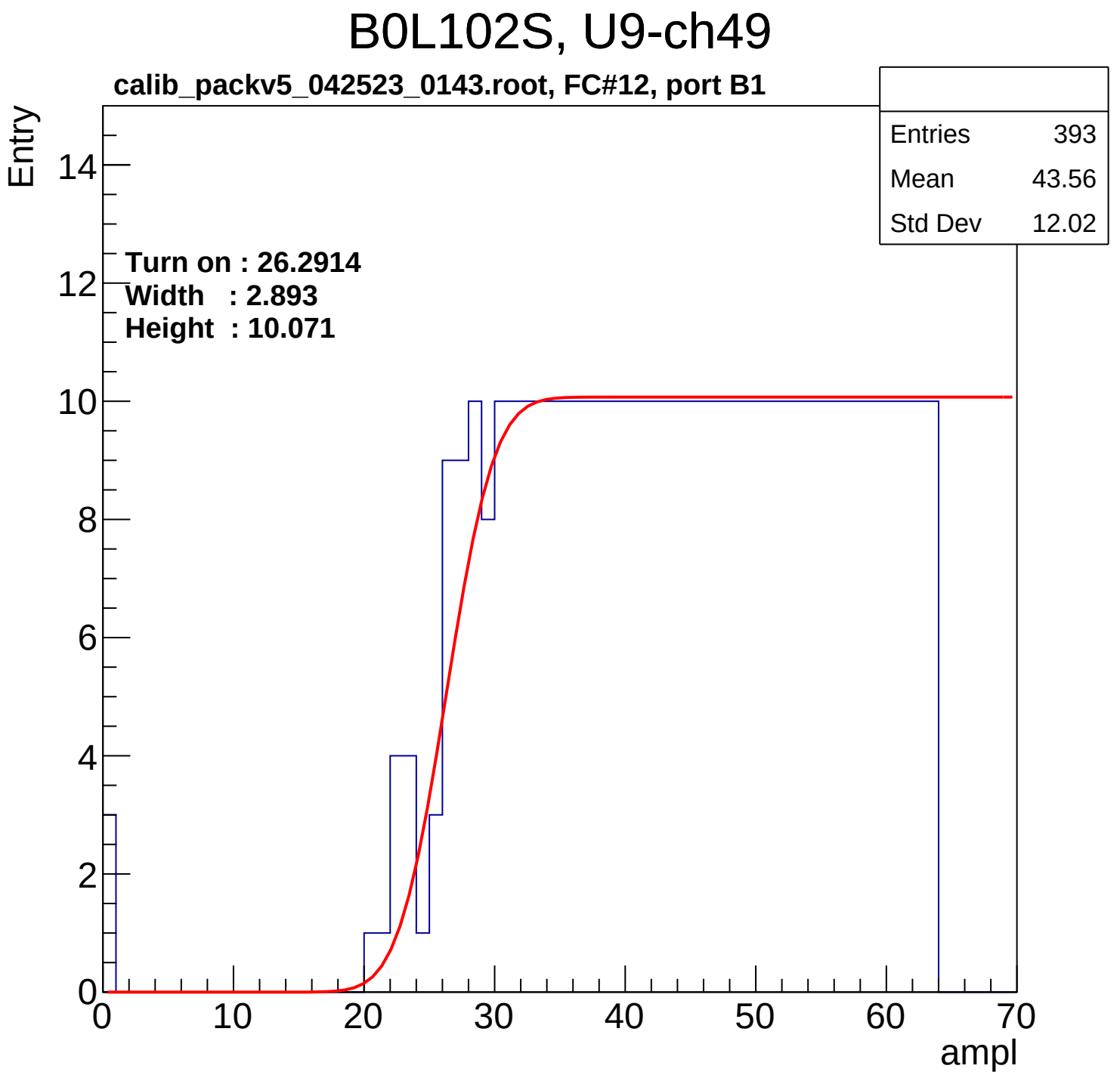

B0L102S, U9-ch44
calib_packv5_042523_0143.root, FC#12, port B1
Entries 379
Mean 44.3
Std Dev 11.5
Turn on : 26.3879
Width : 3.574
Height : 10.035
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

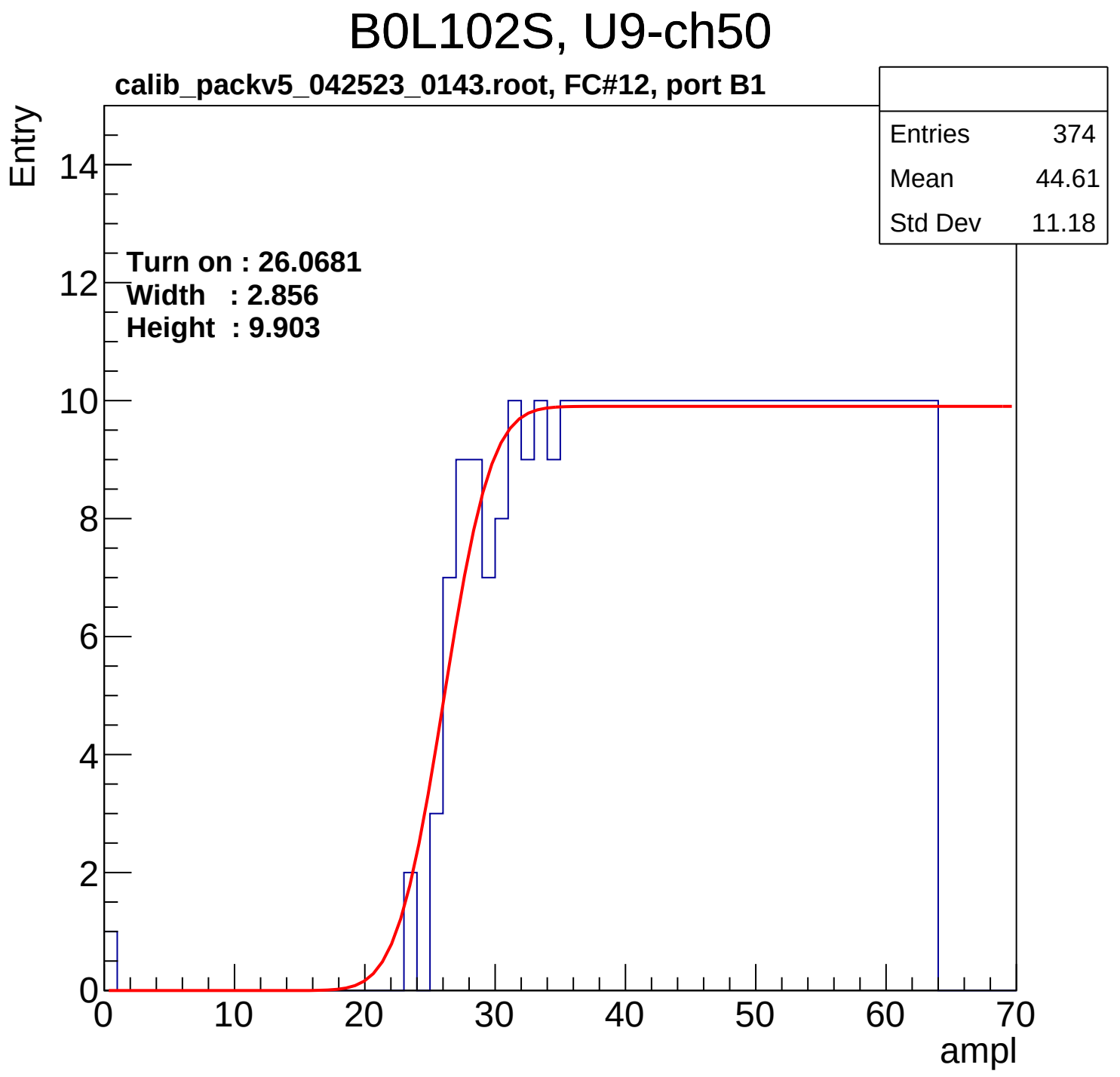

B0L102S, U9-ch45
calib_packv5_042523_0143.root, FC#12, port B1
Entries 385
Mean 44.08
Std Dev 11.55
Turn on : 25.3506
Width : 2.259
Height : 9.979
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

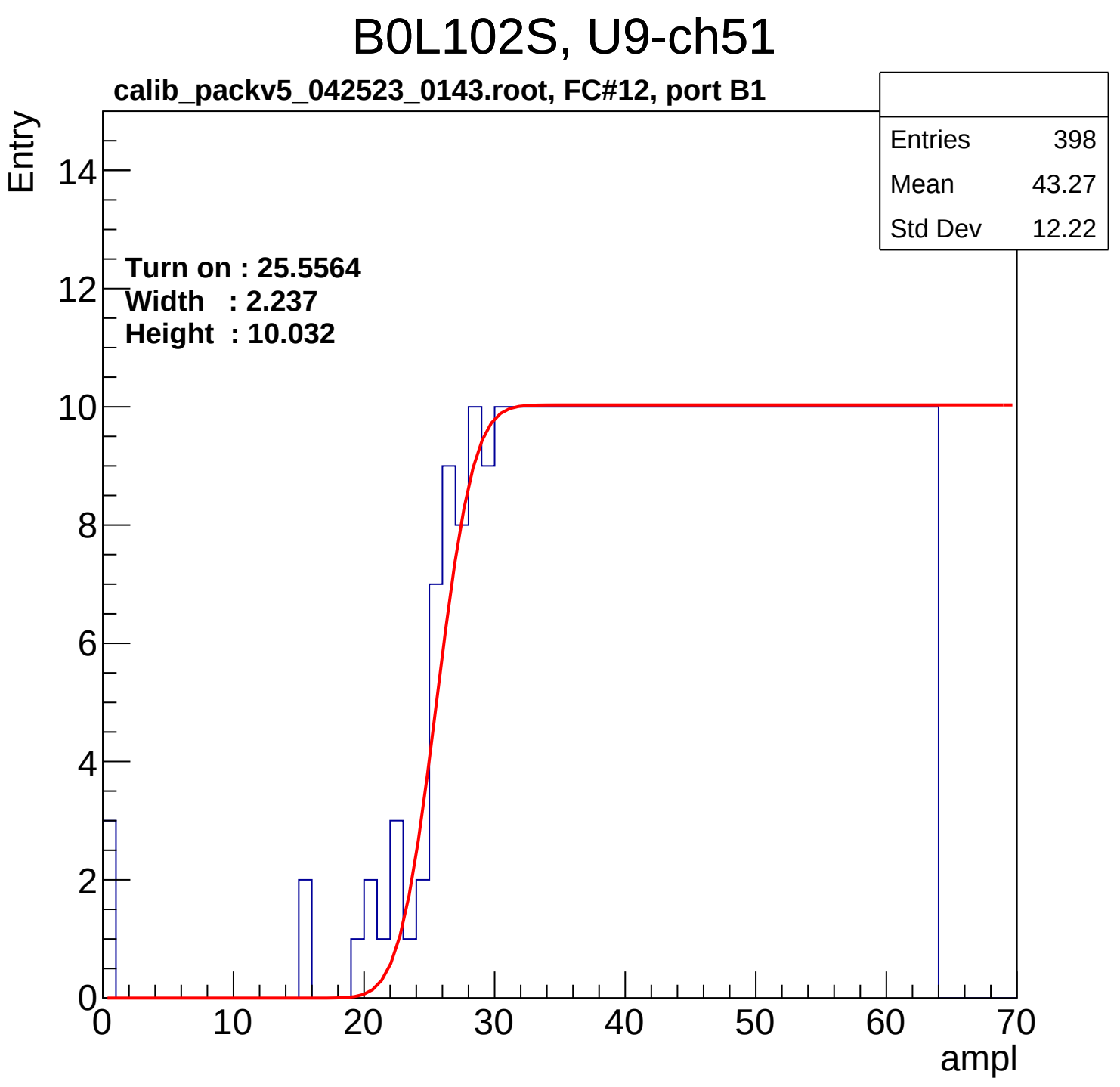

B0L102S, U9-ch46
calib_packv5_042523_0143.root, FC#12, port B1
Entries 390
Mean 43.7
Std Dev 11.96
Turn on : 26.1773
Width : 2.549
Height : 10.035
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

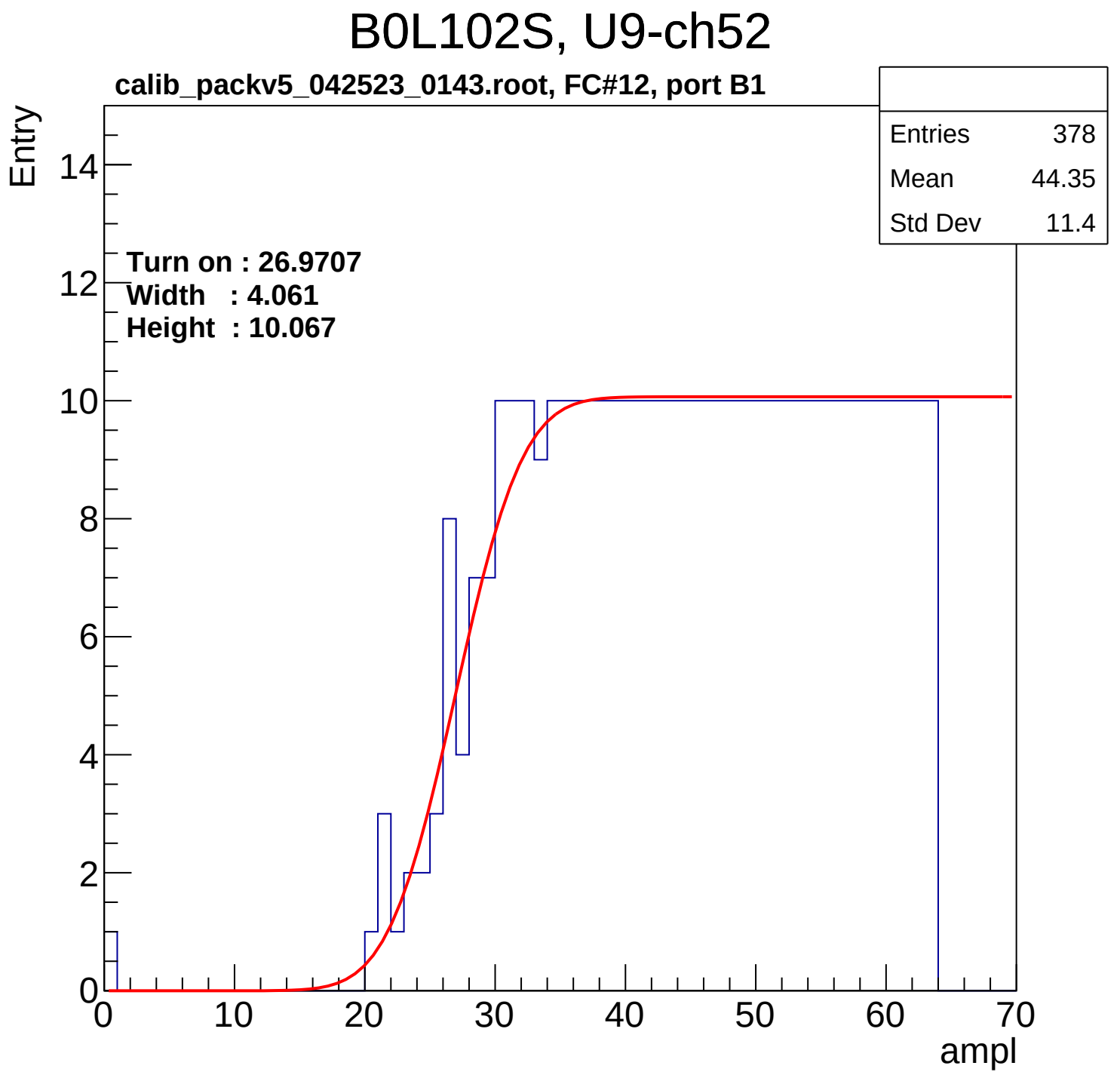

B0L102S, U9-ch47
calib_packv5_042523_0143.root, FC#12, port B1
Entries 384
Mean 43.83
Std Dev 12.27
Turn on : 26.3610
Width : 2.899
Height : 10.042
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

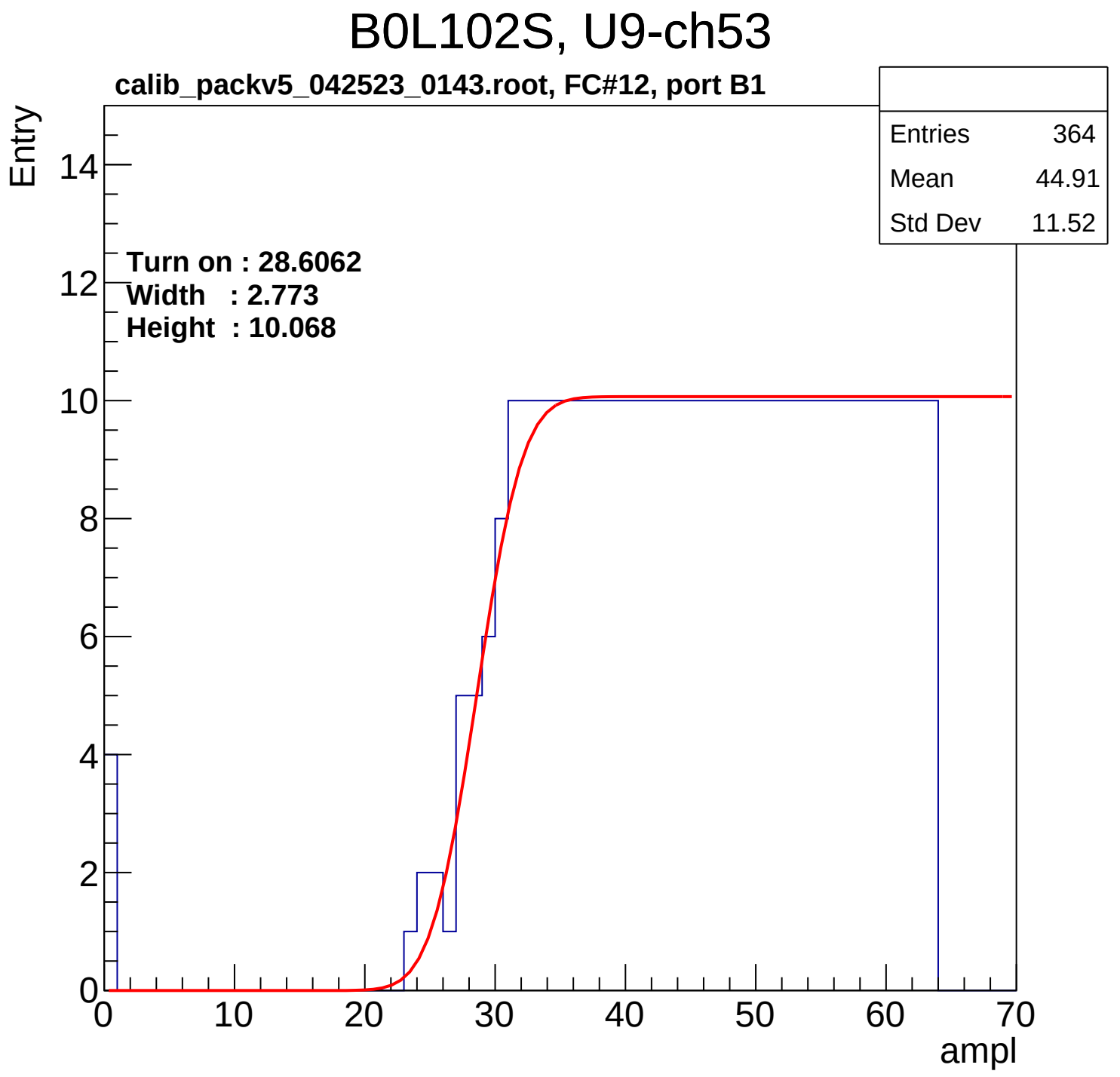

B0L102S, U9-ch48
calib_packv5_042523_0143.root, FC#12, port B1
Entries 376
Mean 44.5
Std Dev 11.27
Turn on : 26.9960
Width : 3.536
Height : 10.062
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

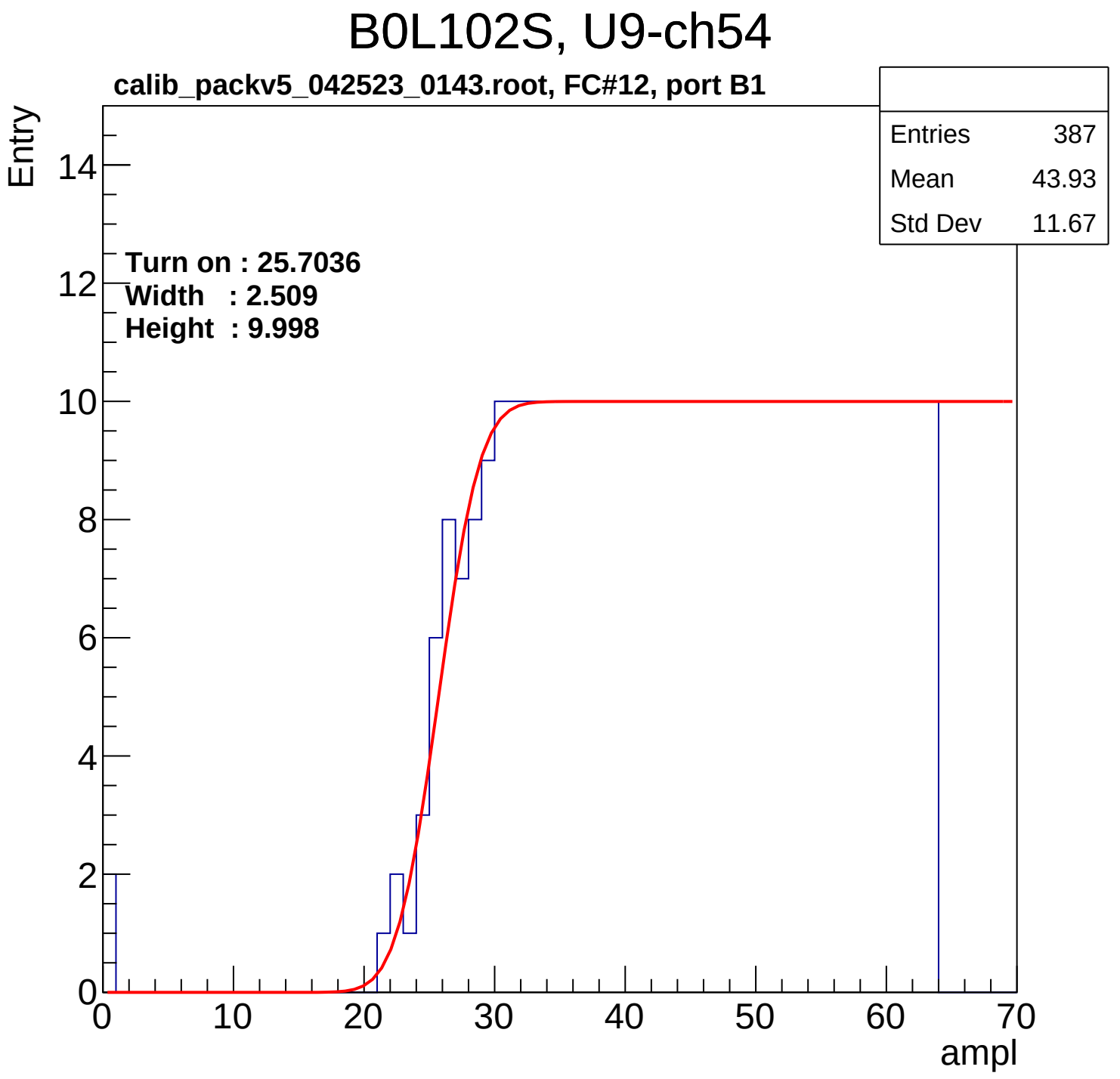

B0L102S, U9-ch49
calib_packv5_042523_0143.root, FC#12, port B1
Entries 393
Mean 43.56
Std Dev 12.02
Turn on : 26.2914
Width : 2.893
Height : 10.071
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

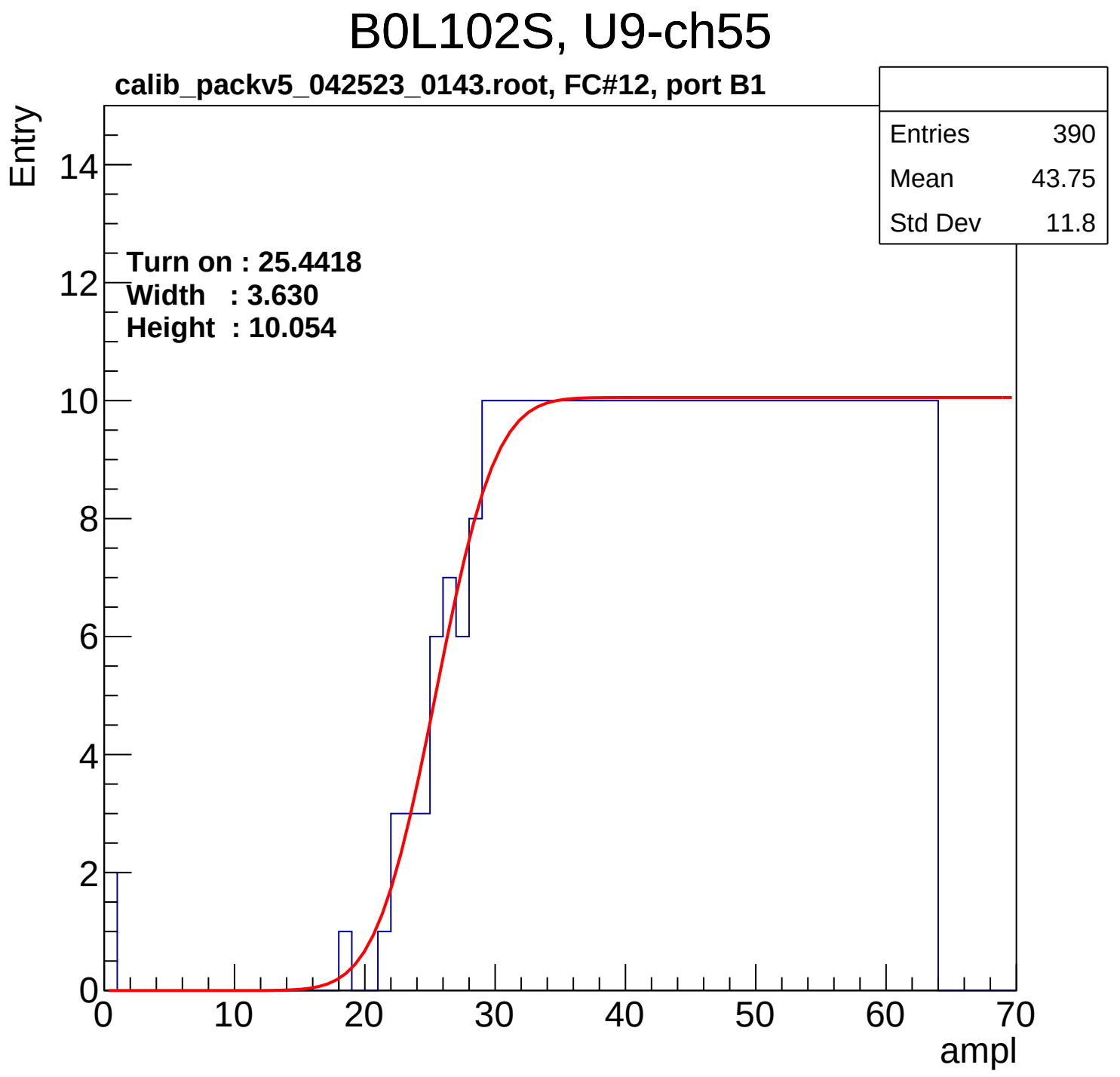

B0L102S, U9-ch50
calib_packv5_042523_0143.root, FC#12, port B1
Entries 374
Mean 44.61
Std Dev 11.18
Turn on : 26.0681
Width : 2.856
Height : 9.903
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

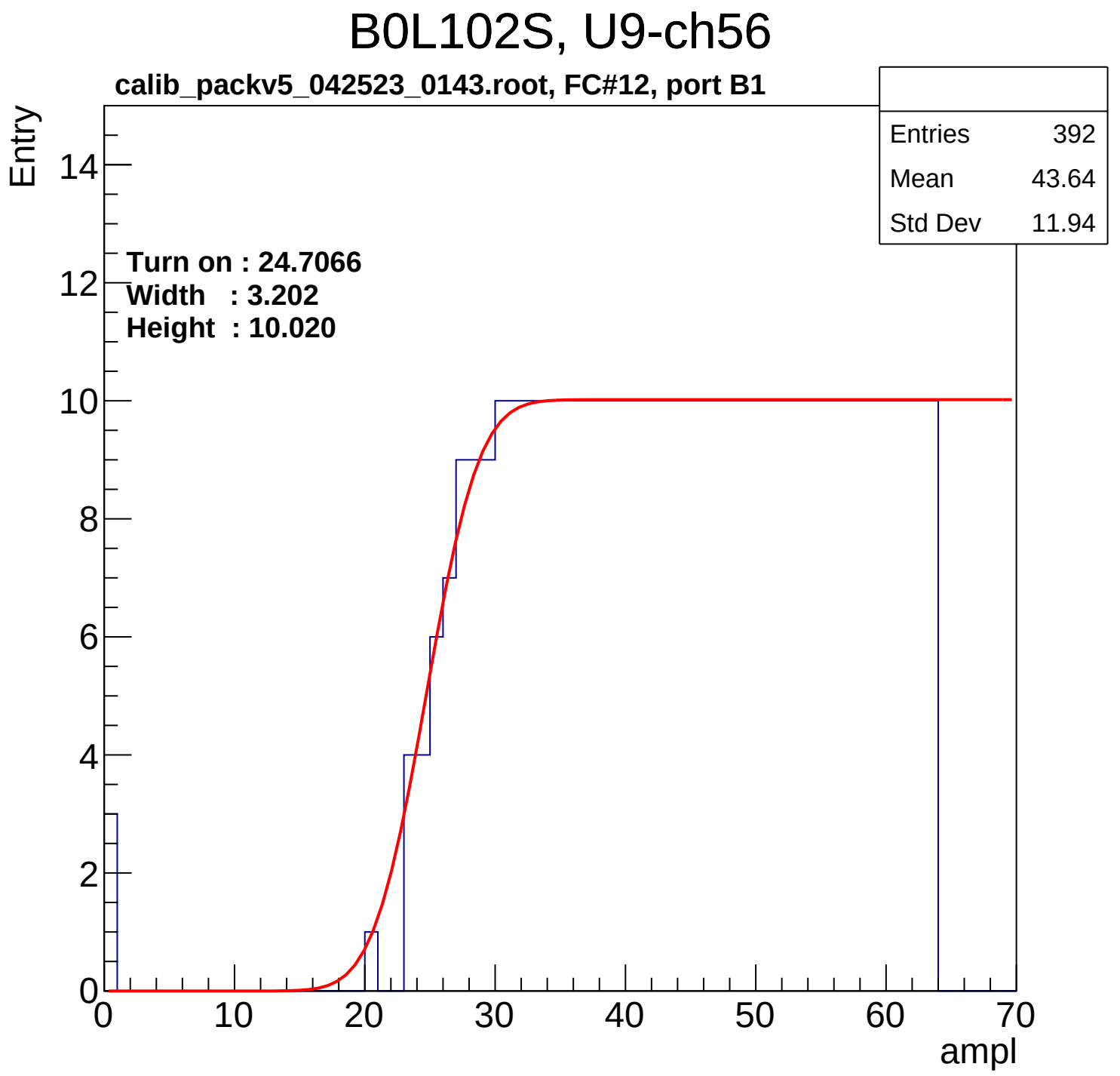

B0L102S, U9-ch51
calib_packv5_042523_0143.root, FC#12, port B1
Entries 398
Mean 43.27
Std Dev 12.22
Turn on : 25.5564
Width : 2.237
Height : 10.032
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

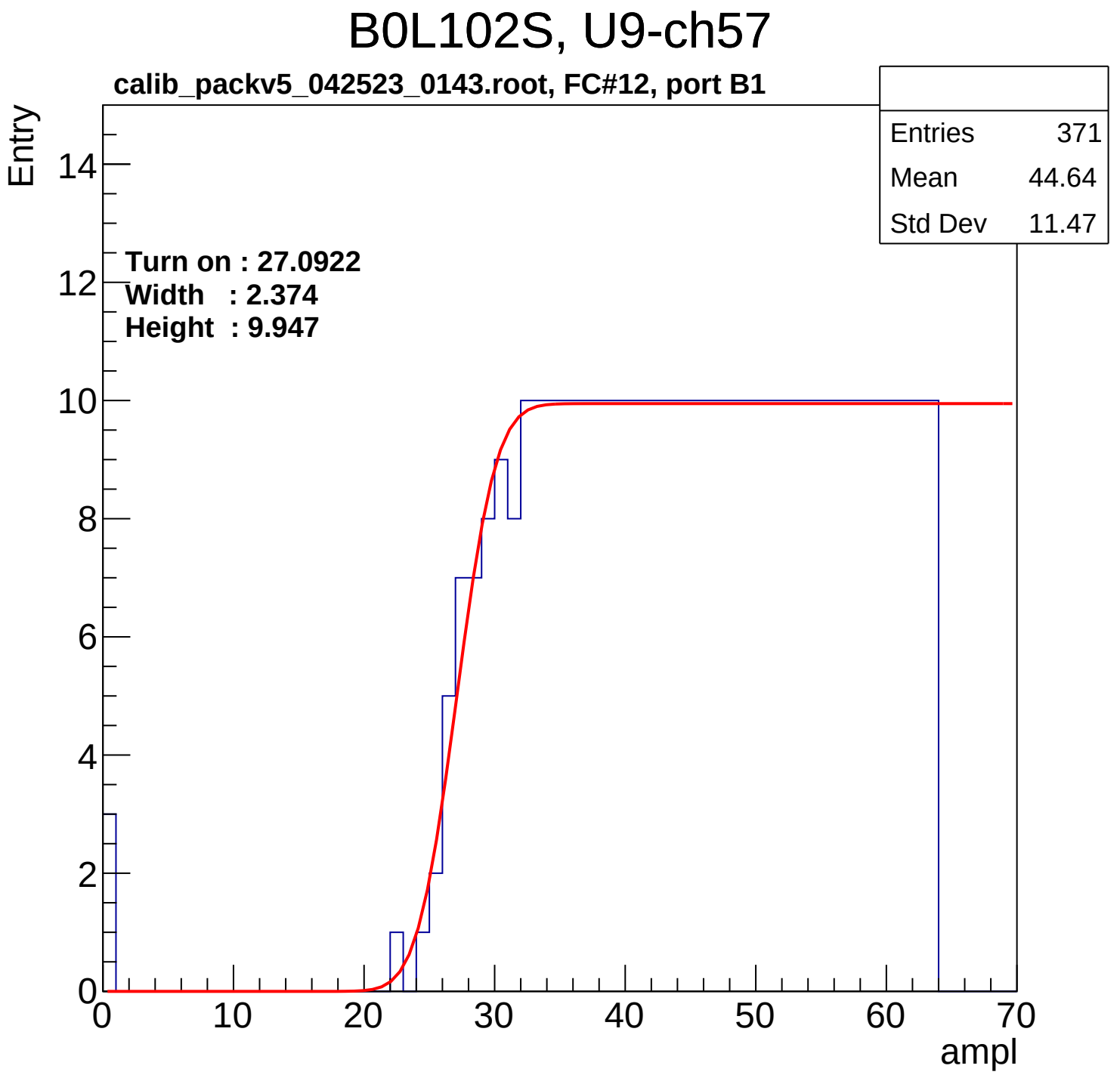

B0L102S, U9-ch52
calib_packv5_042523_0143.root, FC#12, port B1
Entries 378
Mean 44.35
Std Dev 11.4
Turn on : 26.9707
Width : 4.061
Height : 10.067
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

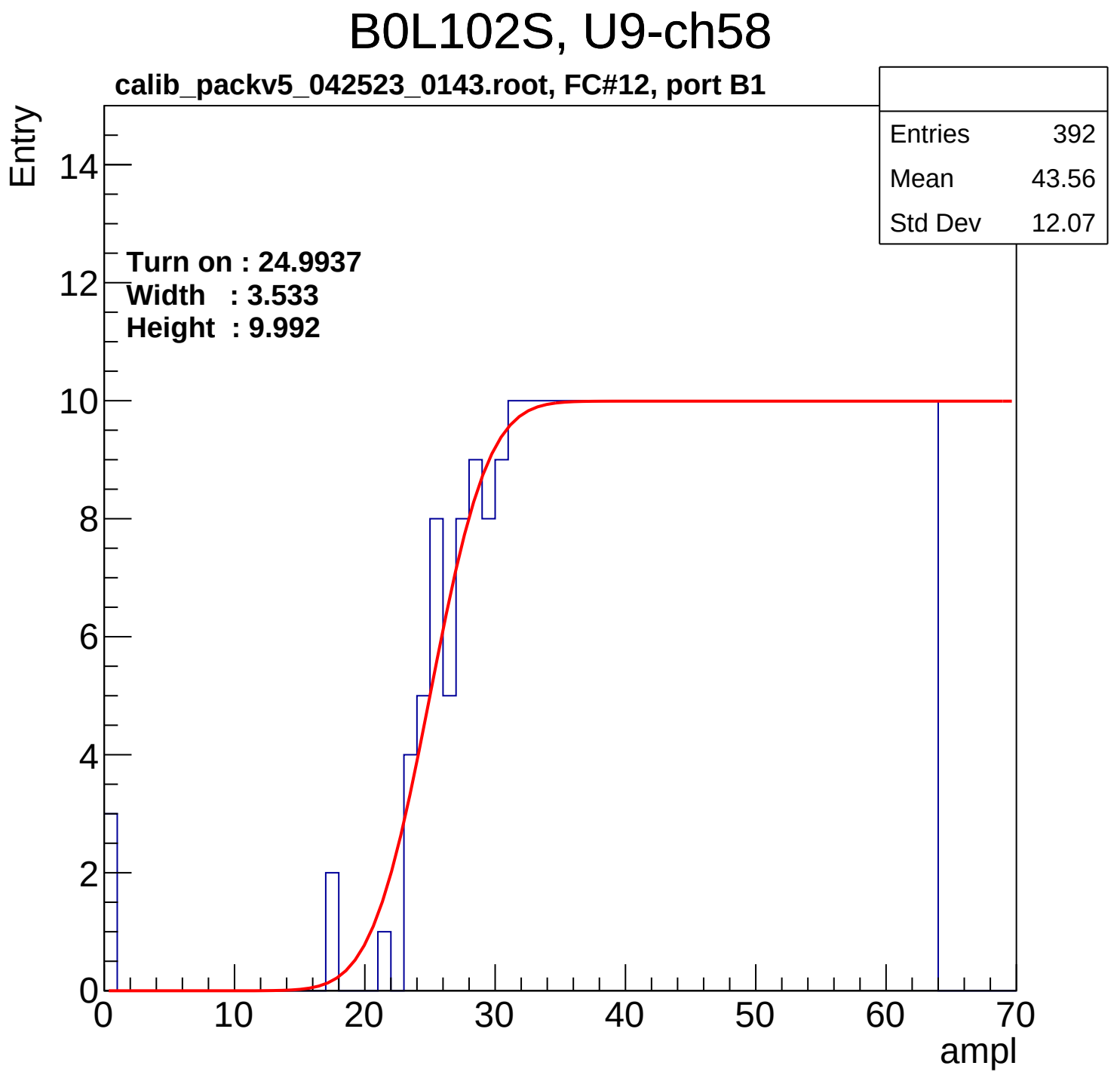

B0L102S, U9-ch53
calib_packv5_042523_0143.root, FC#12, port B1
Entries 364
Mean 44.91
Std Dev 11.52
Turn on : 28.6062
Width : 2.773
Height : 10.068
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

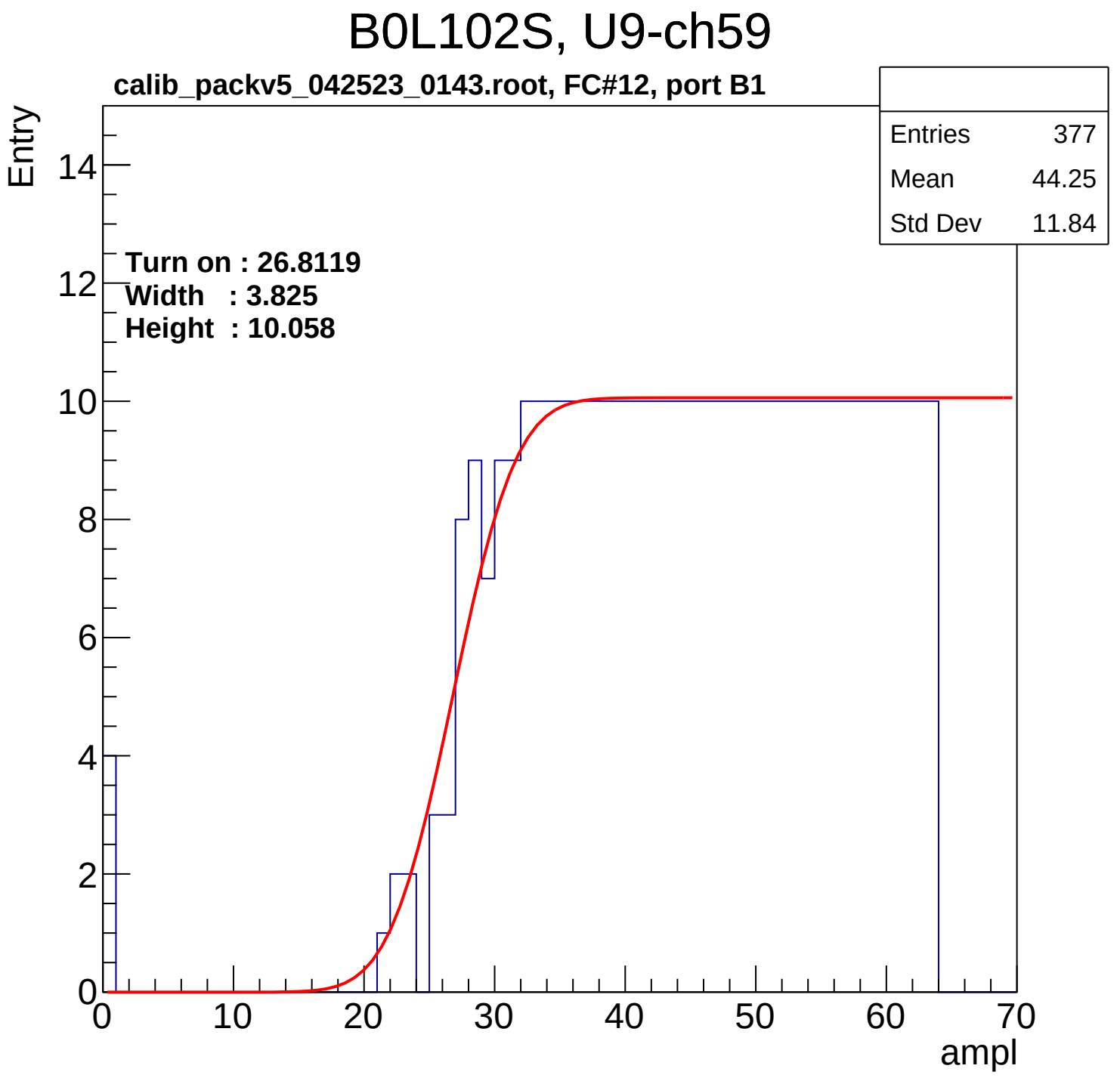

B0L102S, U9-ch54
calib_packv5_042523_0143.root, FC#12, port B1
Entries 387
Mean 43.93
Std Dev 11.67
Turn on : 25.7036
Width : 2.509
Height : 9.998
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

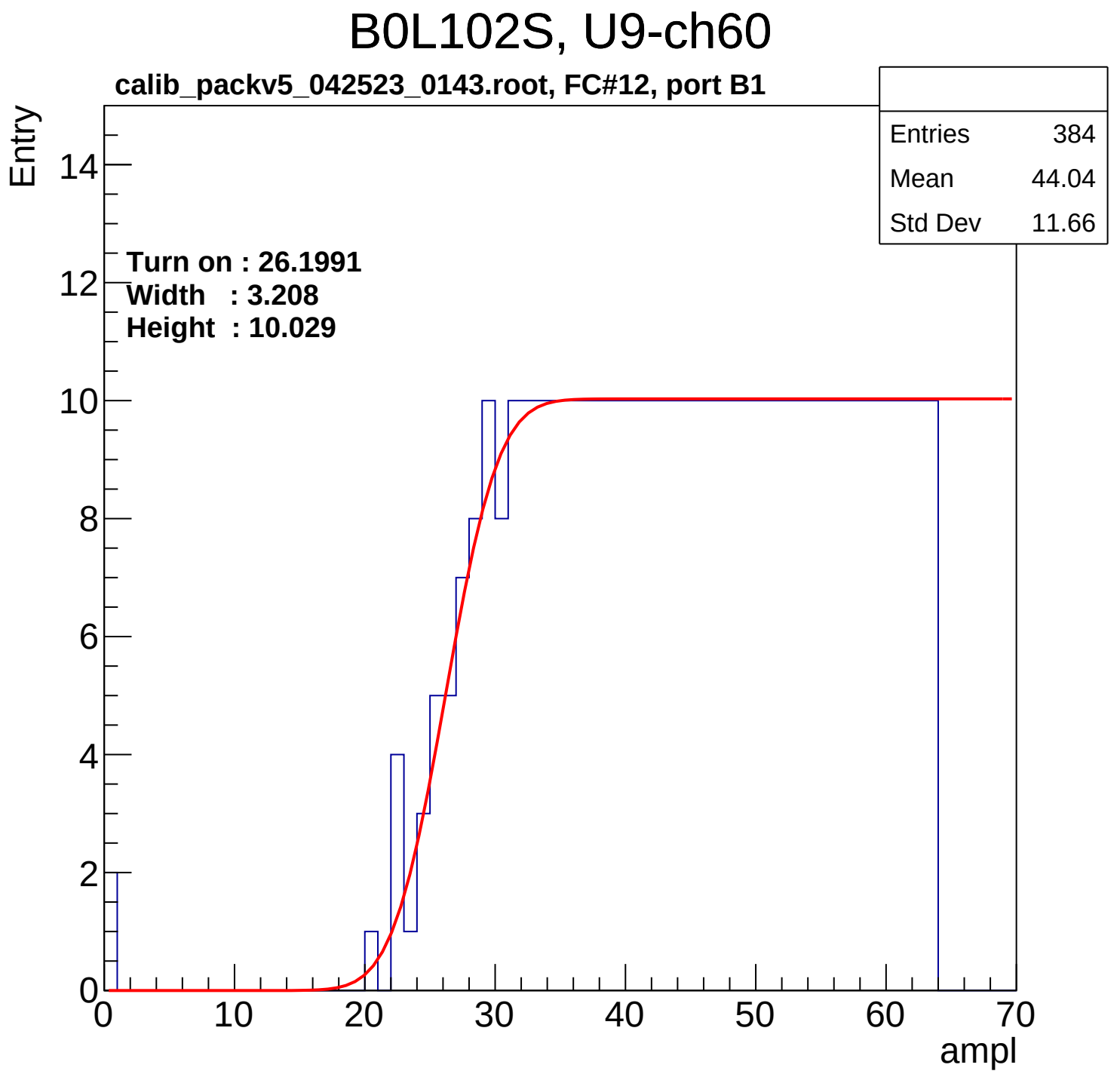

B0L102S, U9-ch55
calib_packv5_042523_0143.root, FC#12, port B1
Entries 390
Mean 43.75
Std Dev 11.8
Turn on : 25.4418
Width : 3.630
Height : 10.054
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

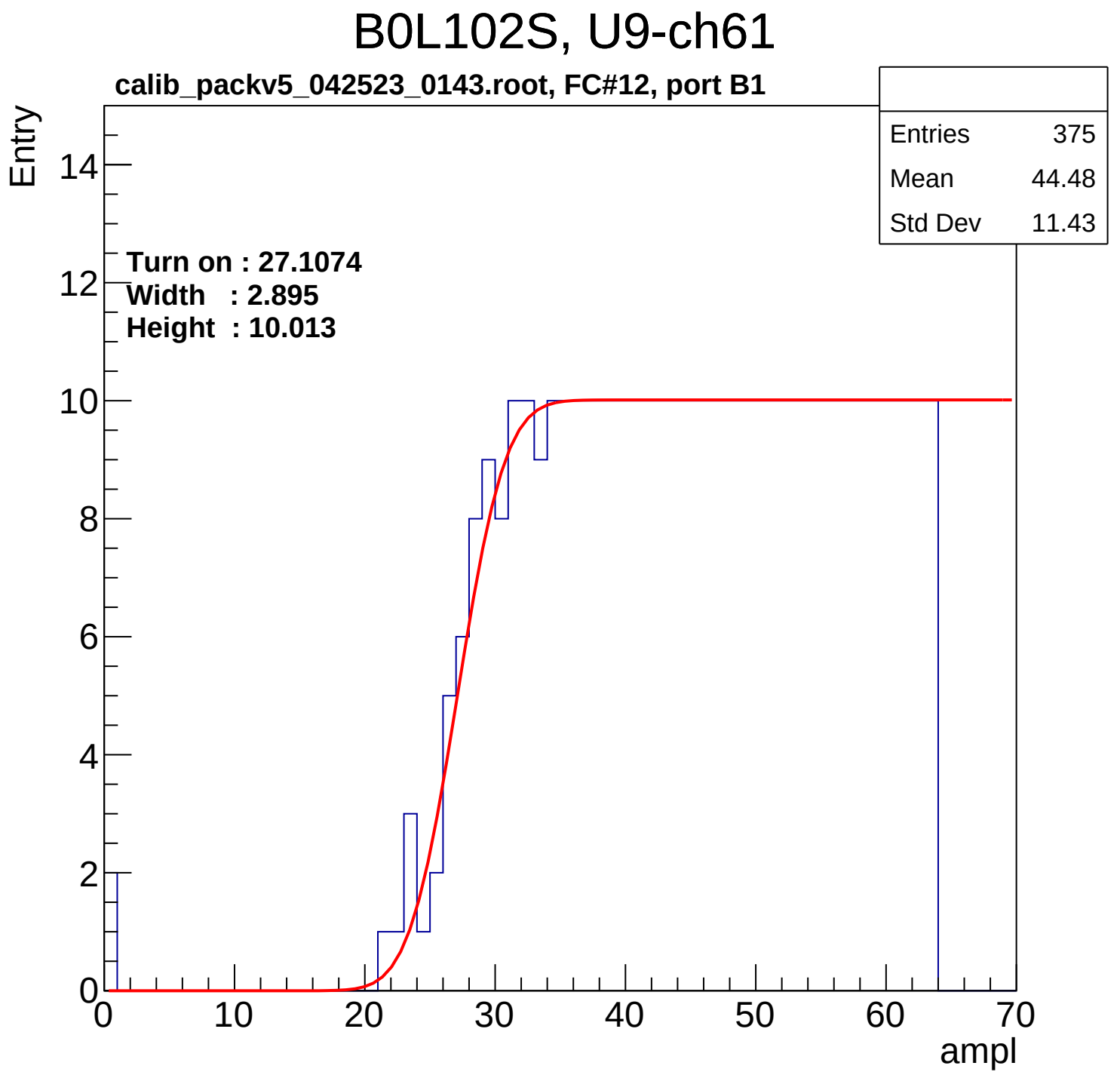

B0L102S, U9-ch56
calib_packv5_042523_0143.root, FC#12, port B1
Entries 392
Mean 43.64
Std Dev 11.94
Turn on : 24.7066
Width : 3.202
Height : 10.020
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

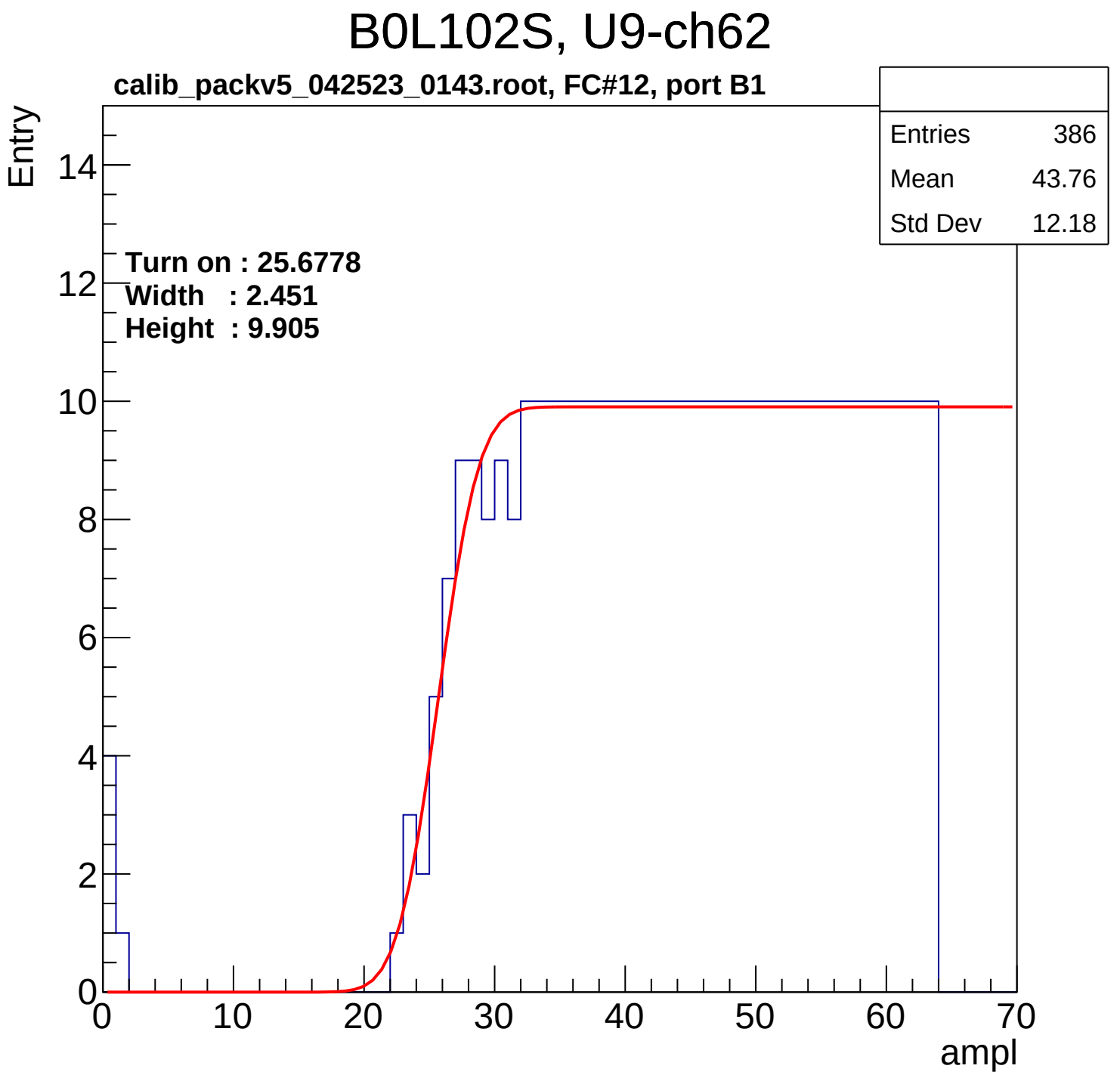

B0L102S, U9-ch57
calib_packv5_042523_0143.root, FC#12, port B1
Entries 371
Mean 44.64
Std Dev 11.47
Turn on : 27.0922
Width : 2.374
Height : 9.947
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

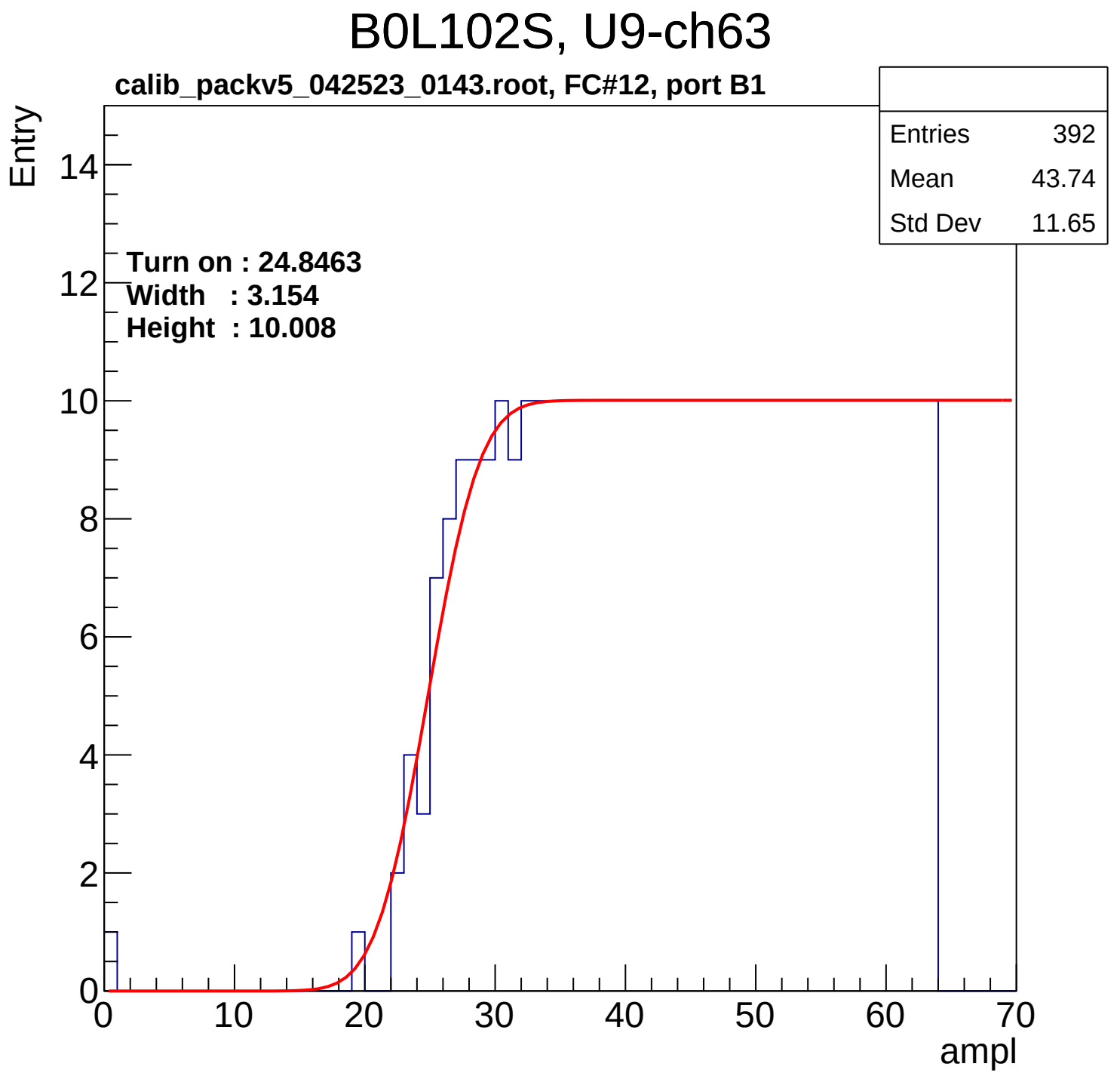

B0L102S, U9-ch58
calib_packv5_042523_0143.root, FC#12, port B1
Entries 392
Mean 43.56
Std Dev 12.07
Turn on : 24.9937
Width : 3.533
Height : 9.992
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

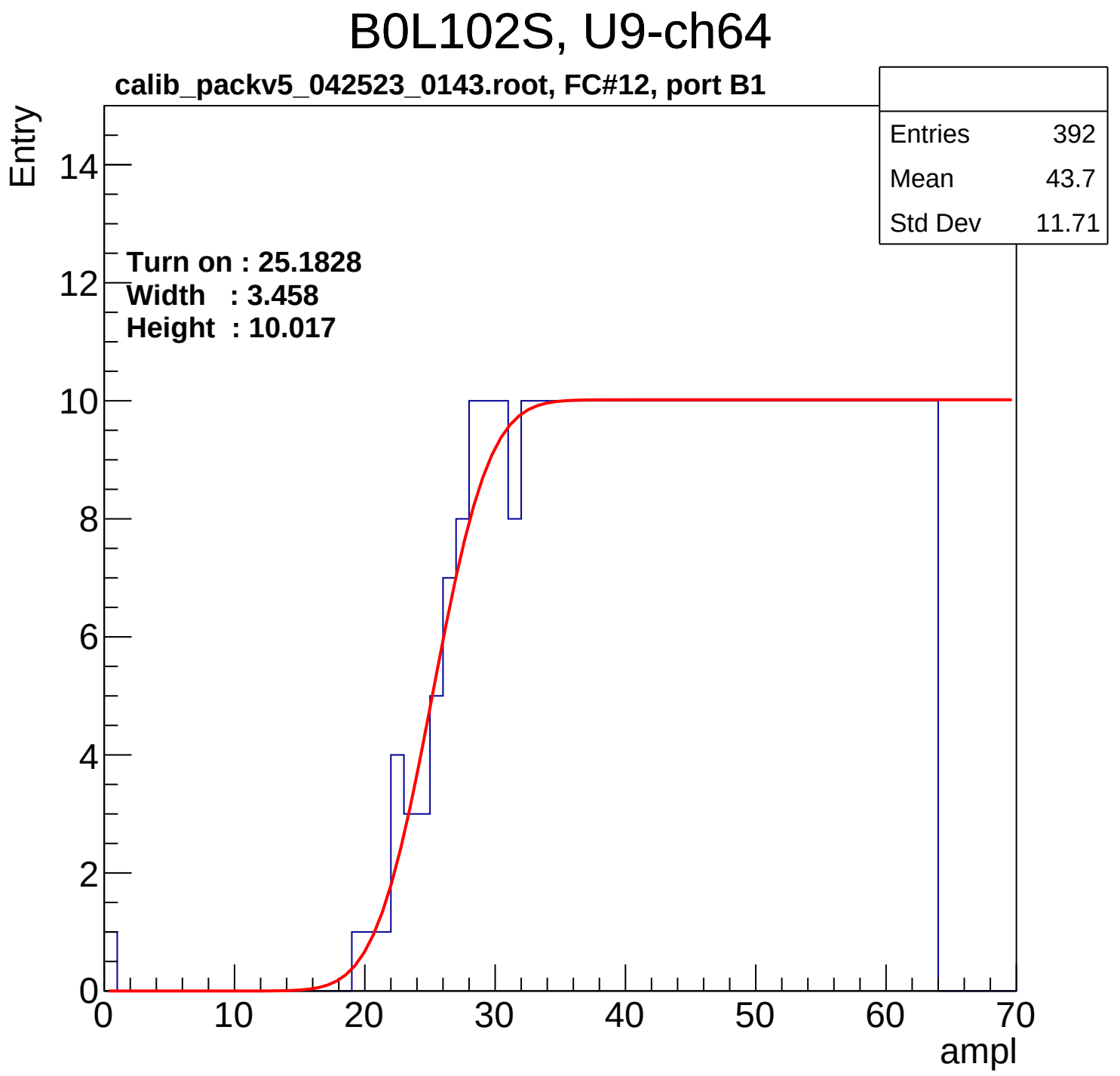

B0L102S, U9-ch59
calib_packv5_042523_0143.root, FC#12, port B1
Entries 377
Mean 44.25
Std Dev 11.84
Turn on : 26.8119
Width : 3.825
Height : 10.058
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

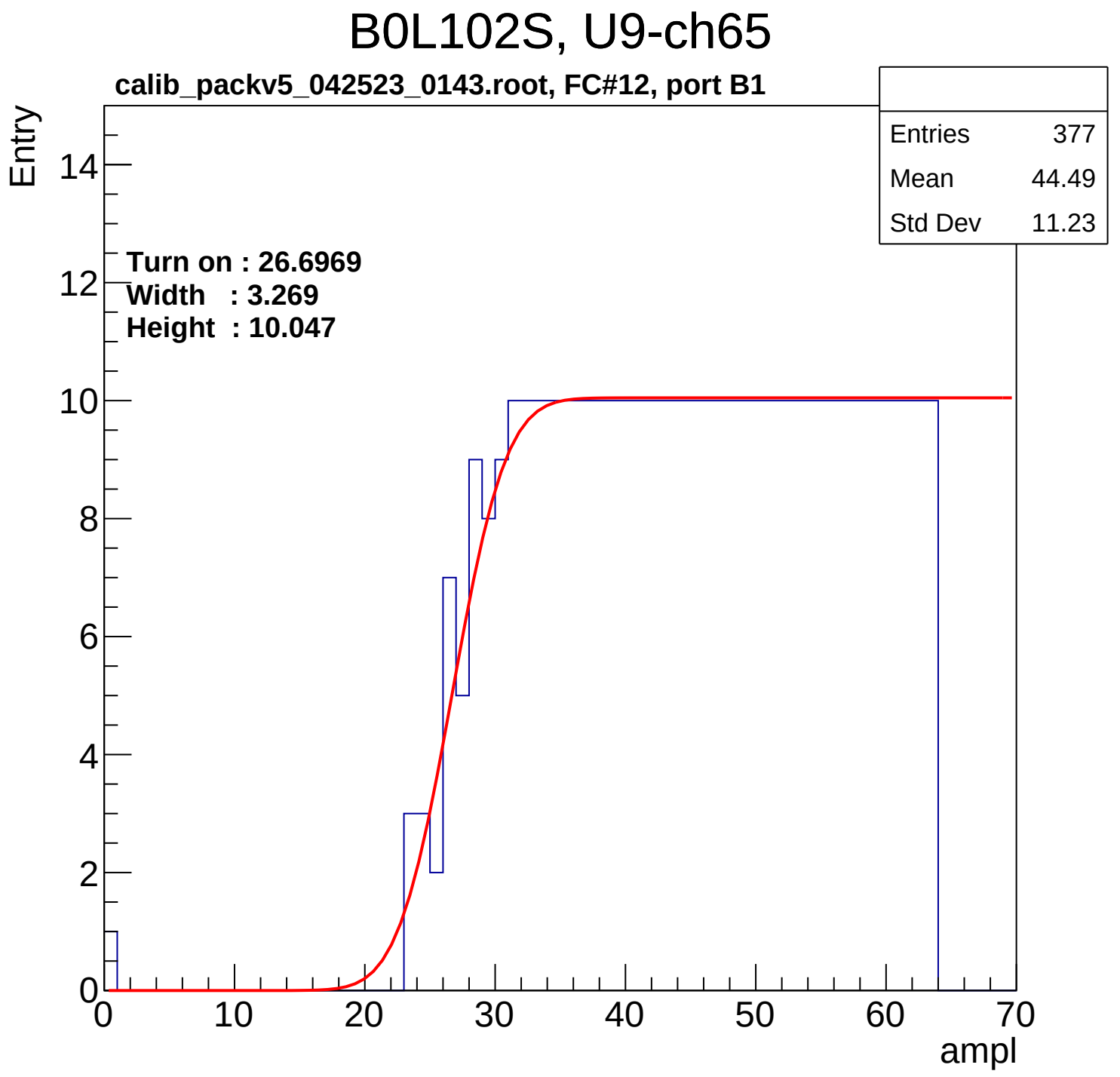

B0L102S, U9-ch60
calib_packv5_042523_0143.root, FC#12, port B1
Entries 384
Mean 44.04
Std Dev 11.66
Turn on : 26.1991
Width : 3.208
Height : 10.029
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

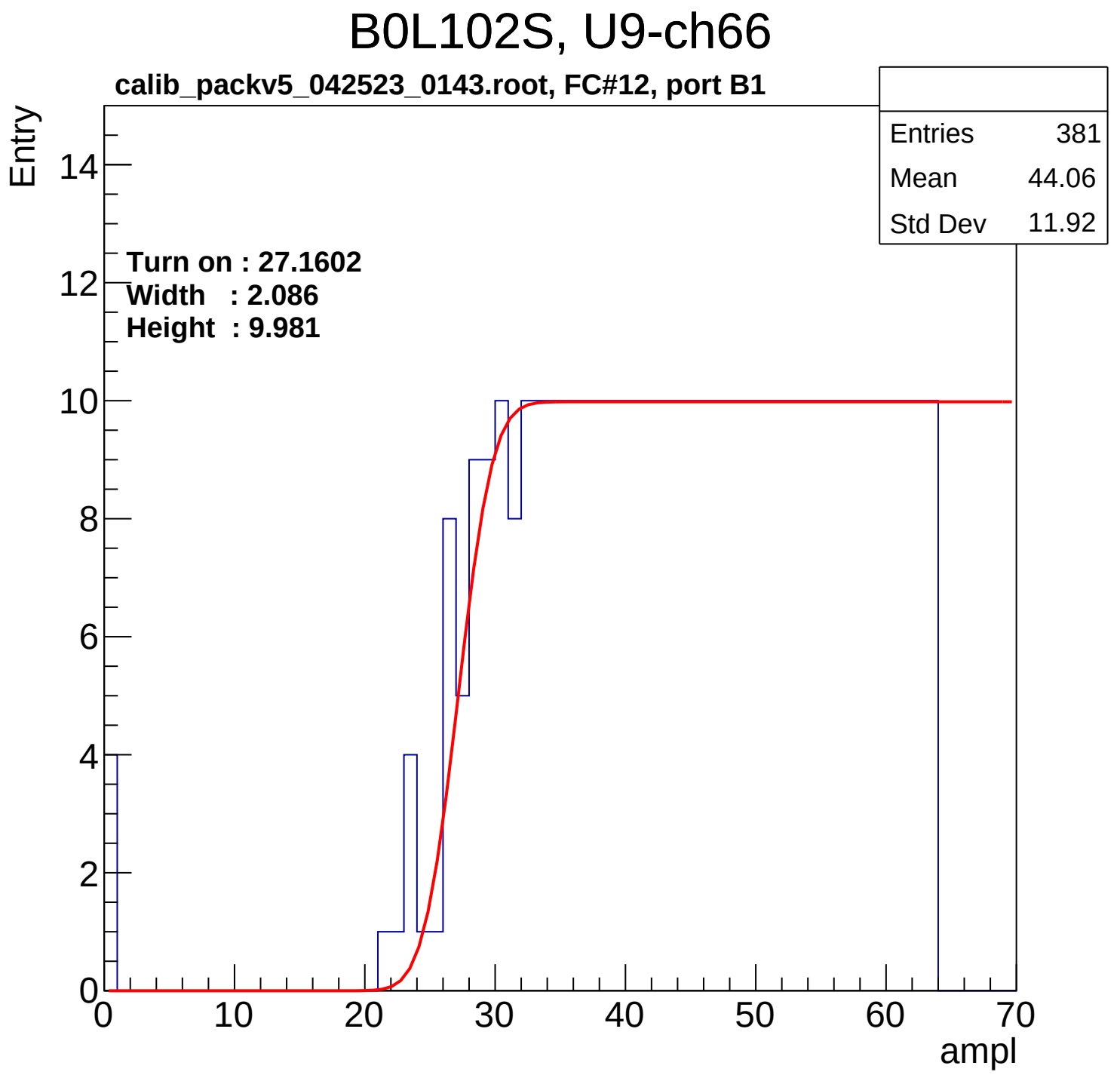

B0L102S, U9-ch61
calib_packv5_042523_0143.root, FC#12, port B1
Entries 375
Mean 44.48
Std Dev 11.43
Turn on : 27.1074
Width : 2.895
Height : 10.013
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

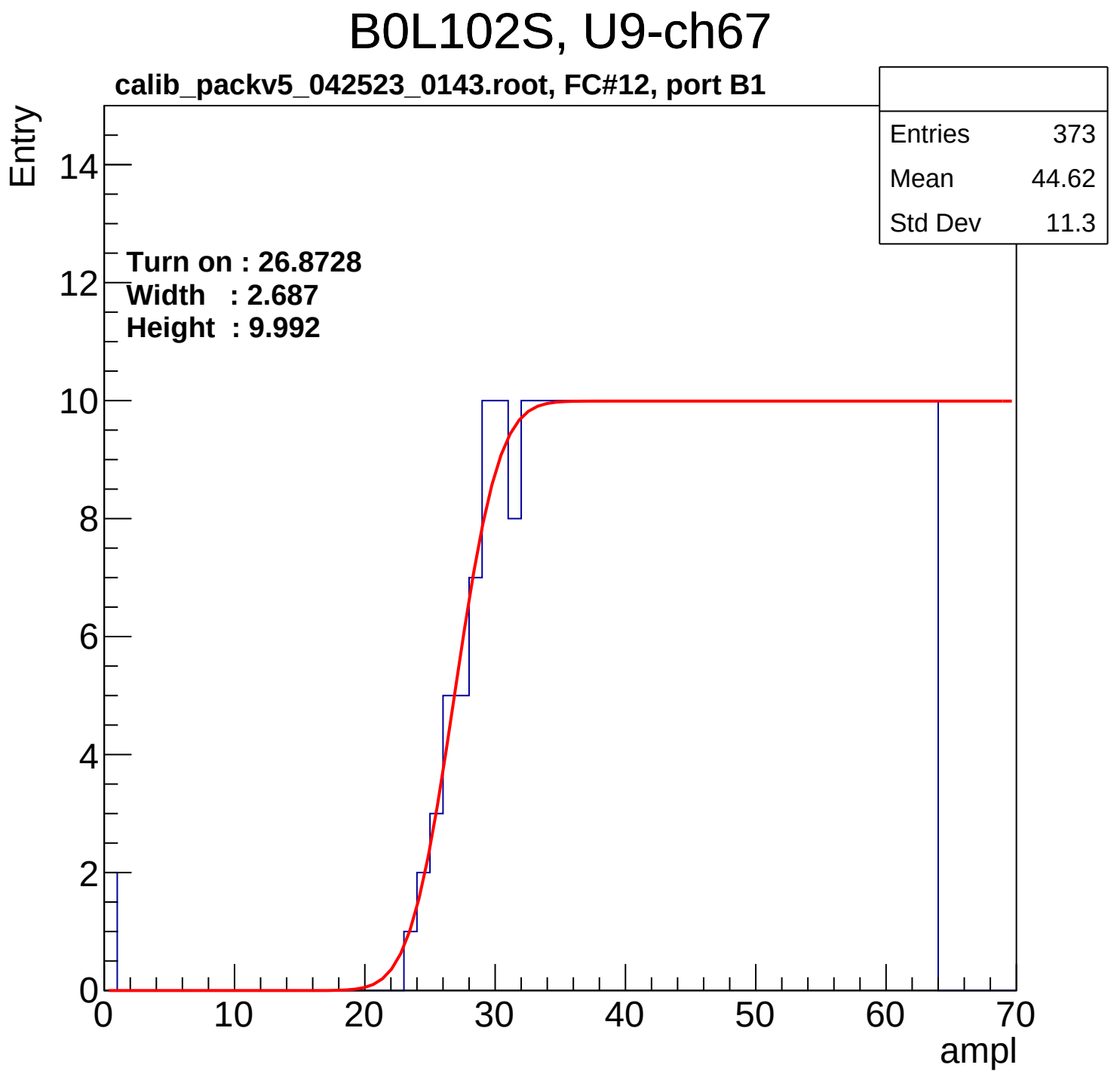

B0L102S, U9-ch62
calib_packv5_042523_0143.root, FC#12, port B1
Entries 386
Mean 43.76
Std Dev 12.18
Turn on : 25.6778
Width : 2.451
Height : 9.905
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

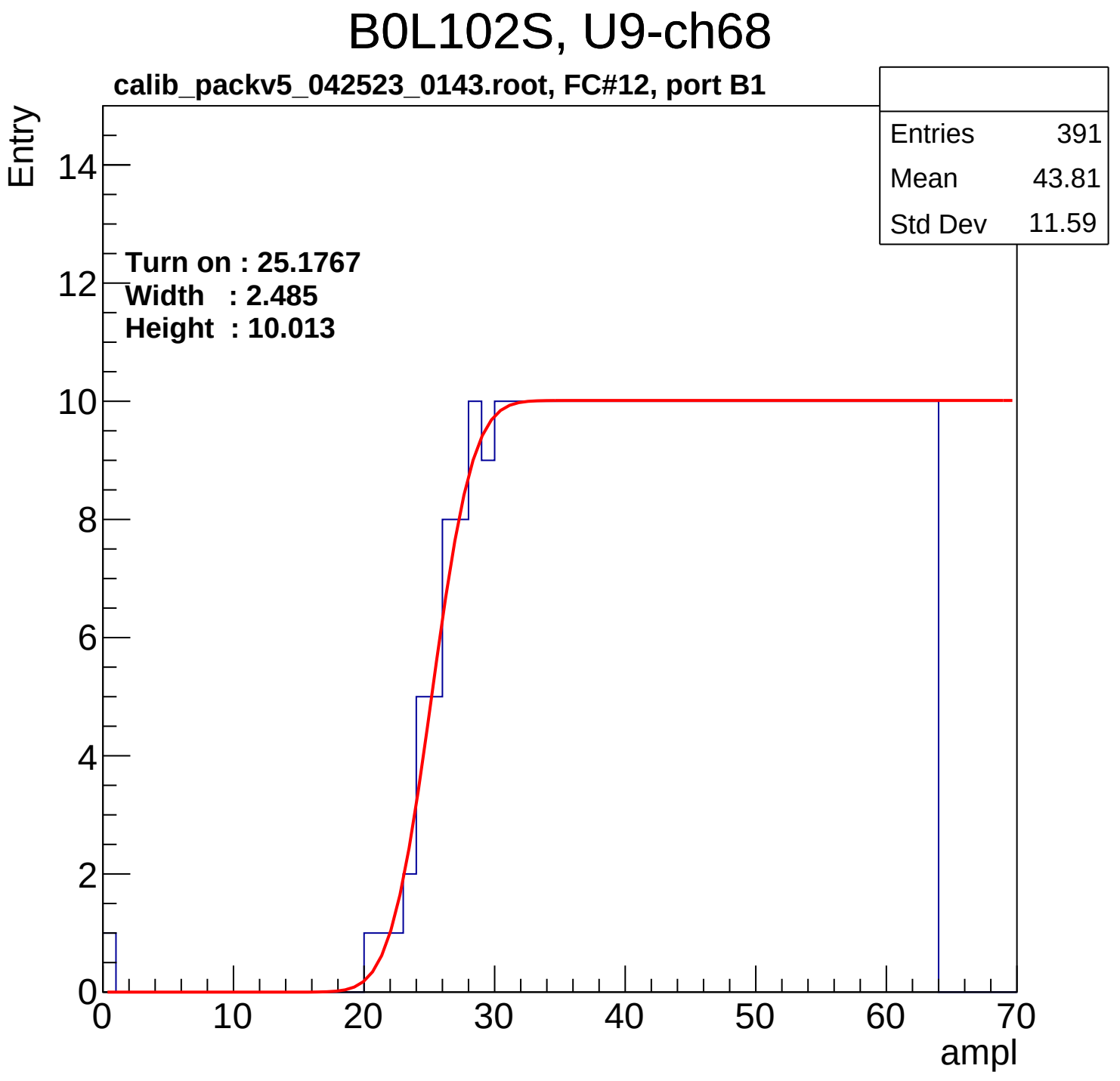

B0L102S, U9-ch63
calib_packv5_042523_0143.root, FC#12, port B1
Entries 392
Mean 43.74
Std Dev 11.65
Turn on : 24.8463
Width : 3.154
Height : 10.008
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

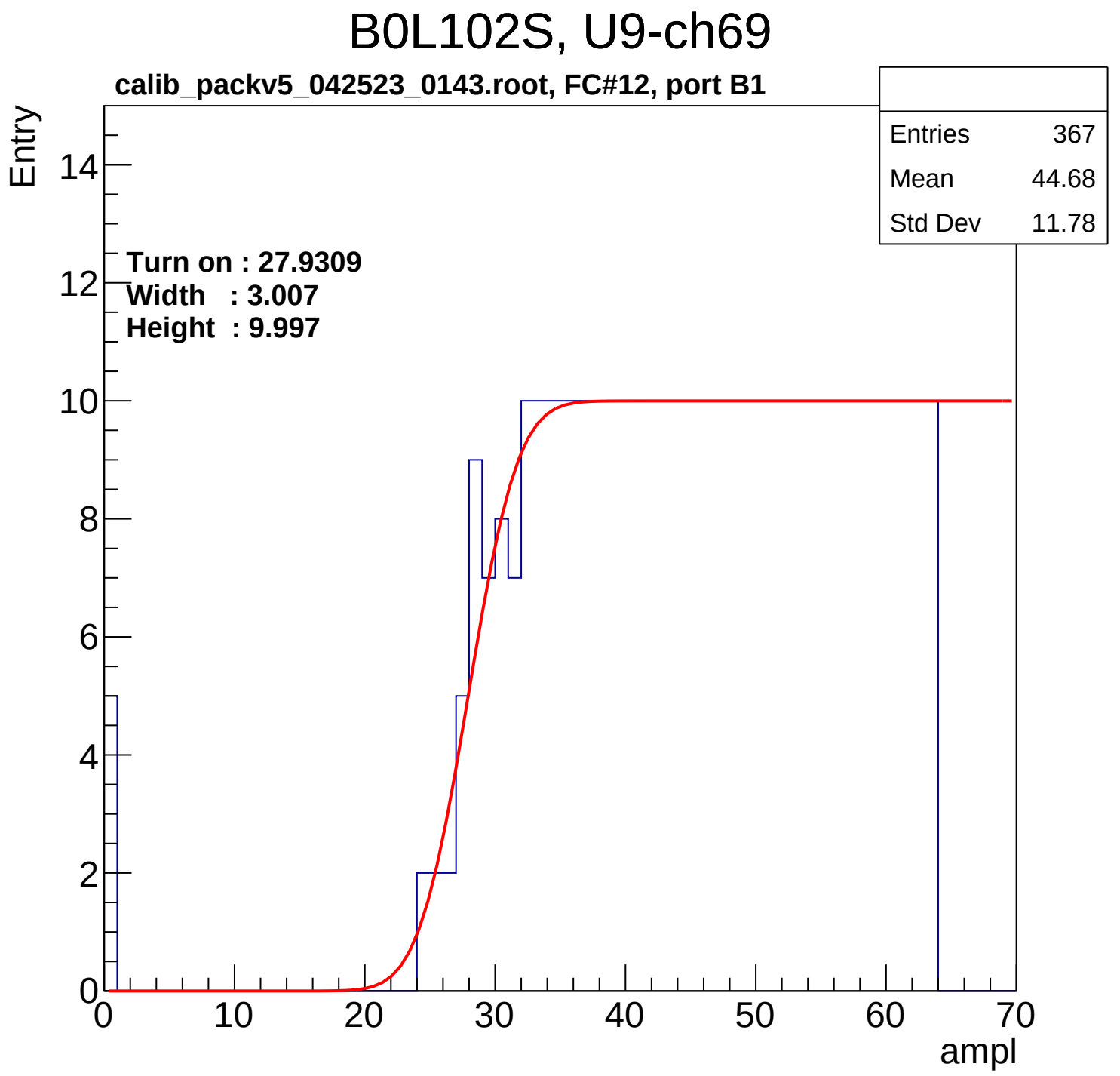

B0L102S, U9-ch64
calib_packv5_042523_0143.root, FC#12, port B1
Entries 392
Mean 43.7
Std Dev 11.71
Turn on : 25.1828
Width : 3.458
Height : 10.017
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

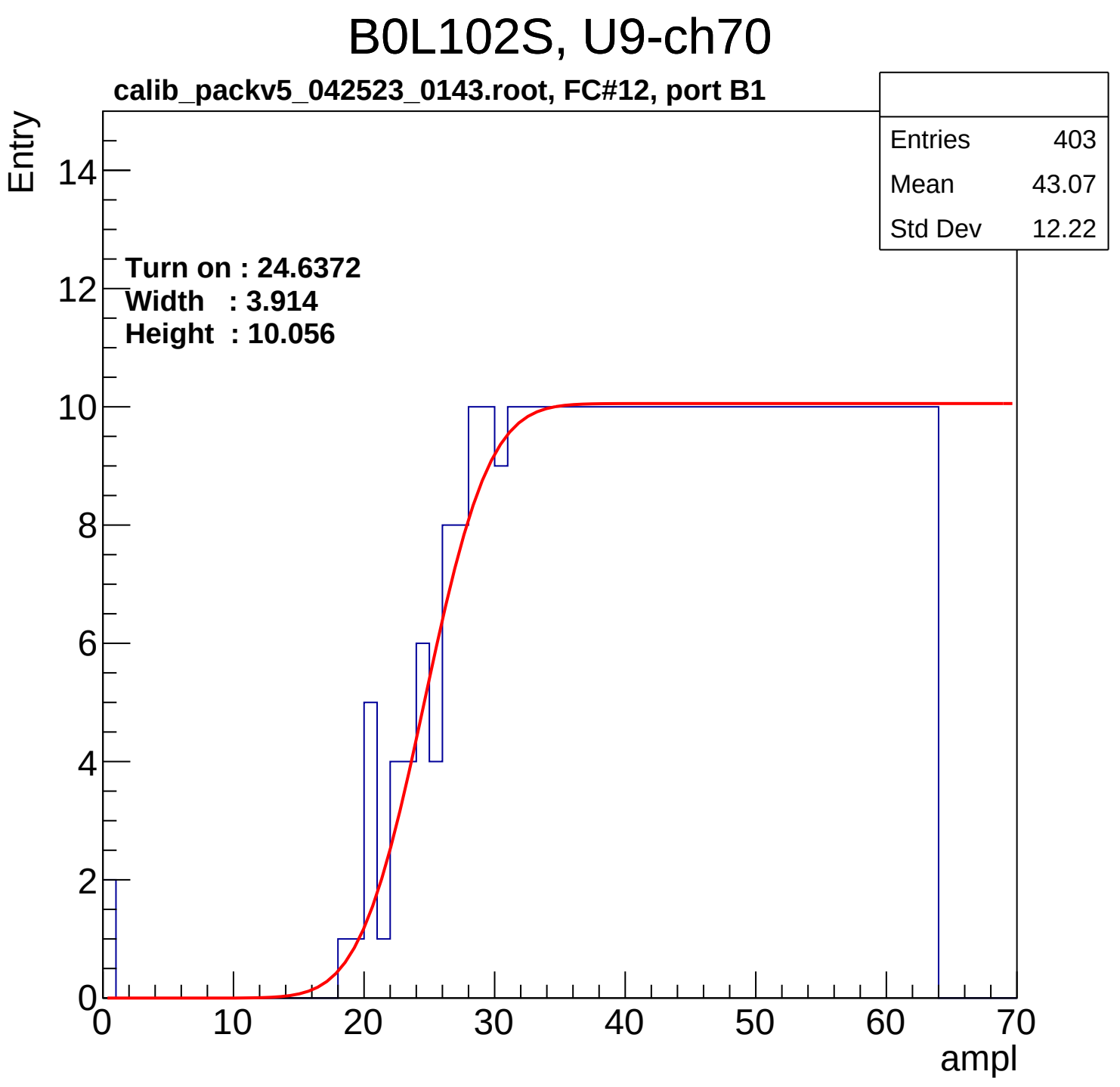

B0L102S, U9-ch65
calib_packv5_042523_0143.root, FC#12, port B1
Entries 377
Mean 44.49
Std Dev 11.23
Turn on : 26.6969
Width : 3.269
Height : 10.047
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

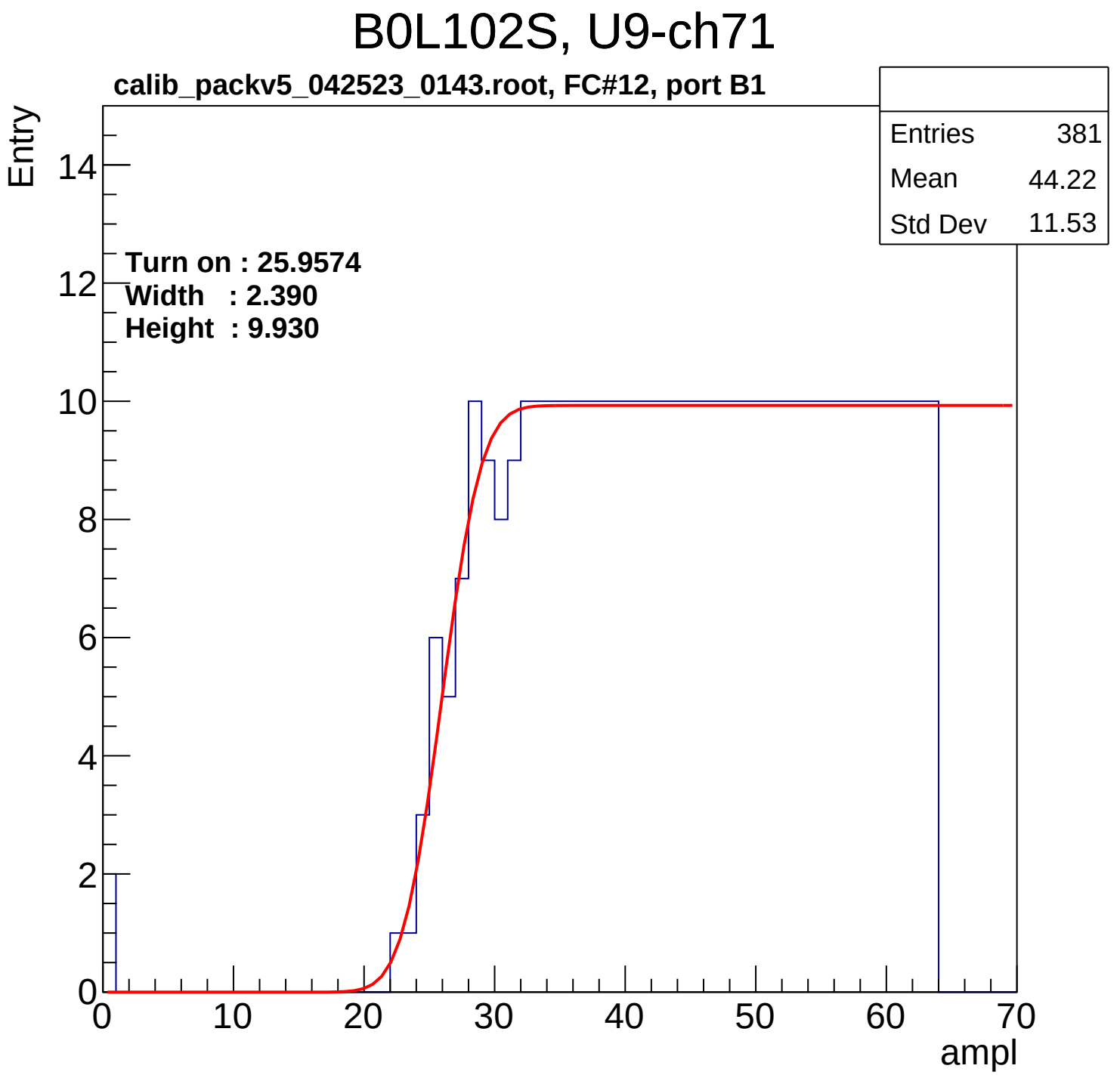

B0L102S, U9-ch66
calib_packv5_042523_0143.root, FC#12, port B1
Entries 381
Mean 44.06
Std Dev 11.92
Turn on : 27.1602
Width : 2.086
Height : 9.981
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

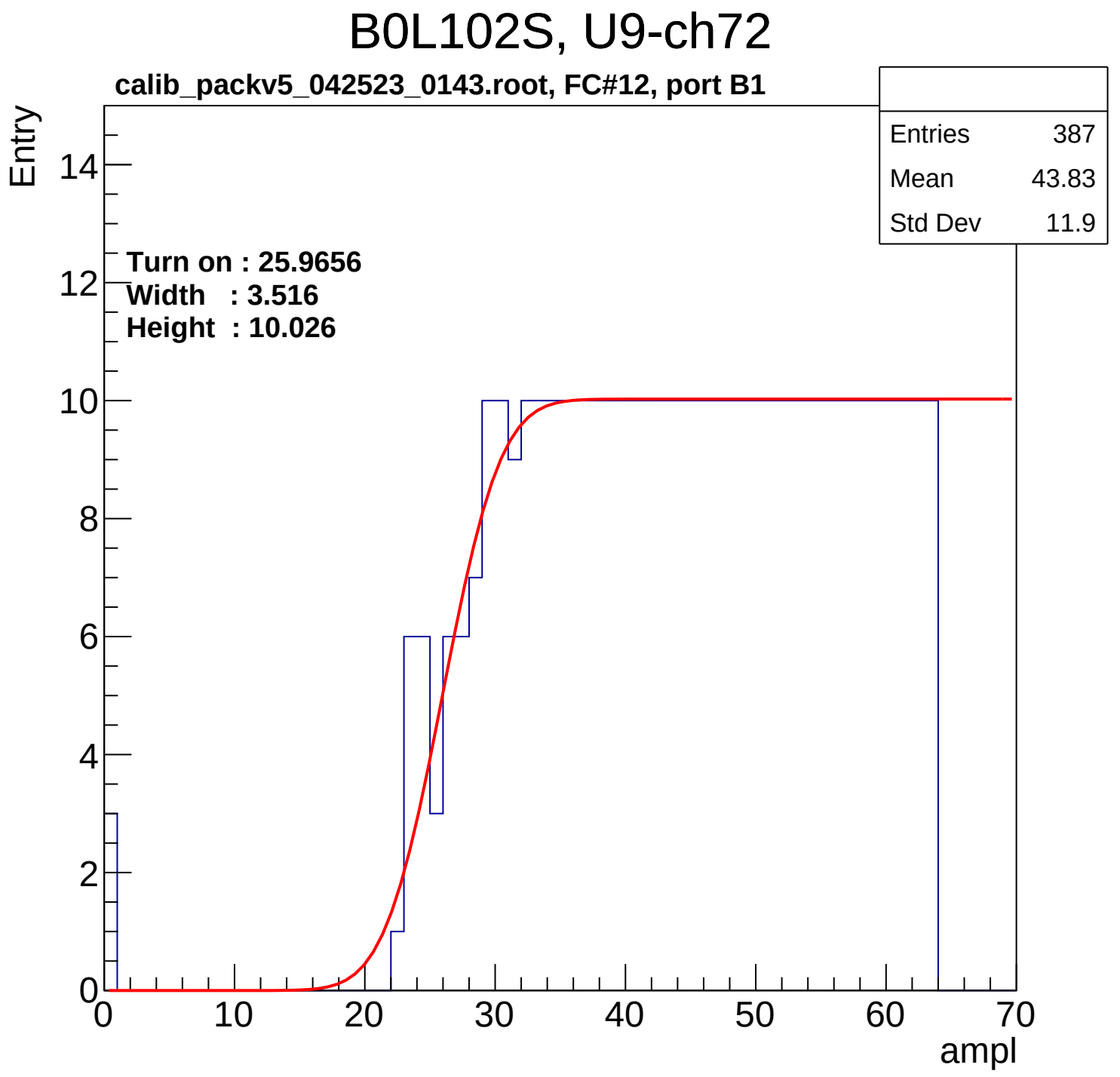

B0L102S, U9-ch67
calib_packv5_042523_0143.root, FC#12, port B1
Entries 373
Mean 44.62
Std Dev 11.3
Turn on : 26.8728
Width : 2.687
Height : 9.992
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

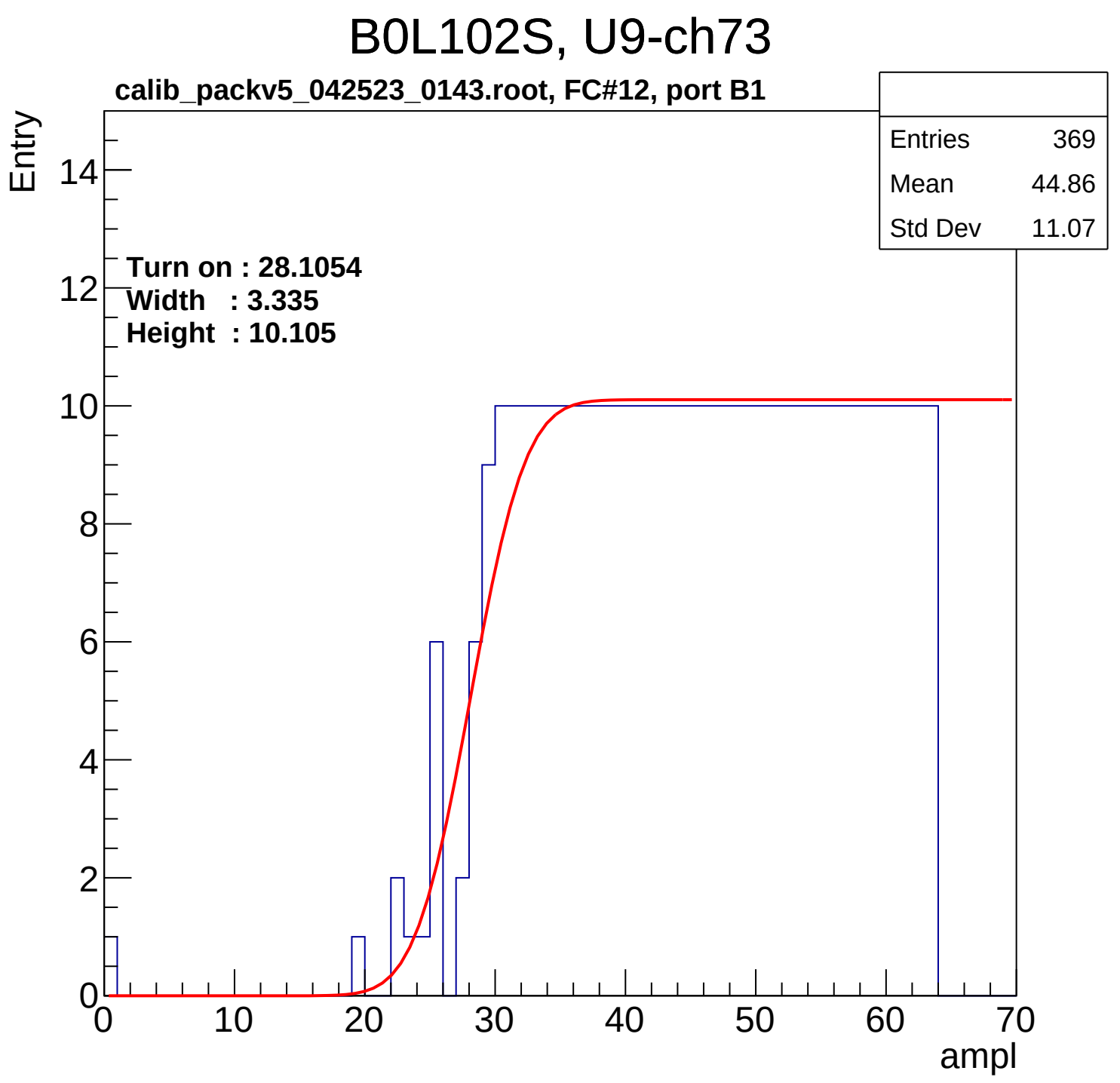

B0L102S, U9-ch68
calib_packv5_042523_0143.root, FC#12, port B1
Entries 391
Mean 43.81
Std Dev 11.59
Turn on : 25.1767
Width : 2.485
Height : 10.013
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

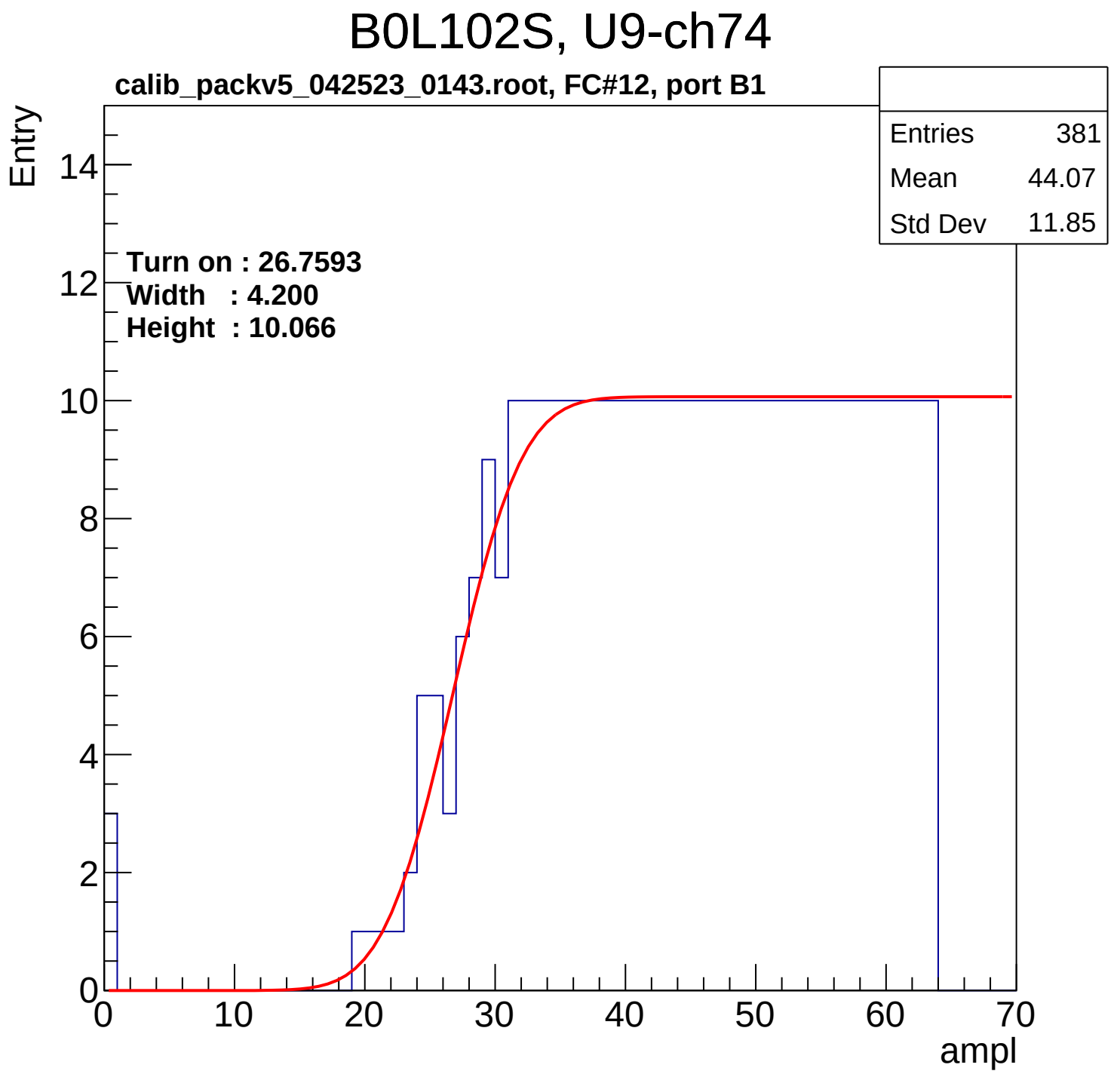

B0L102S, U9-ch69
calib_packv5_042523_0143.root, FC#12, port B1
Entries 367
Mean 44.68
Std Dev 11.78
Turn on : 27.9309
Width : 3.007
Height : 9.997
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

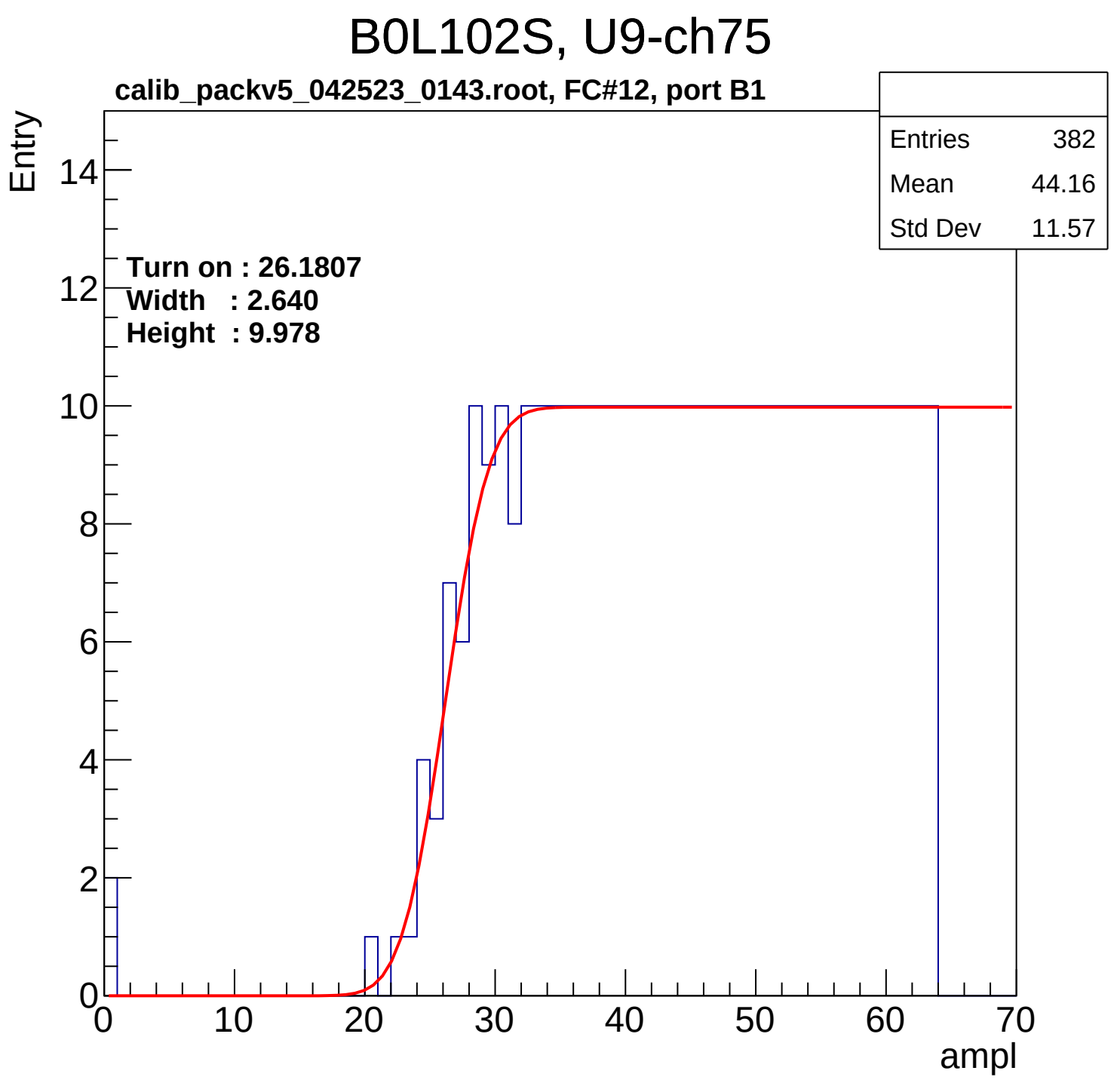

B0L102S, U9-ch70
calib_packv5_042523_0143.root, FC#12, port B1
Entries 403
Mean 43.07
Std Dev 12.22
Turn on : 24.6372
Width : 3.914
Height : 10.056
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

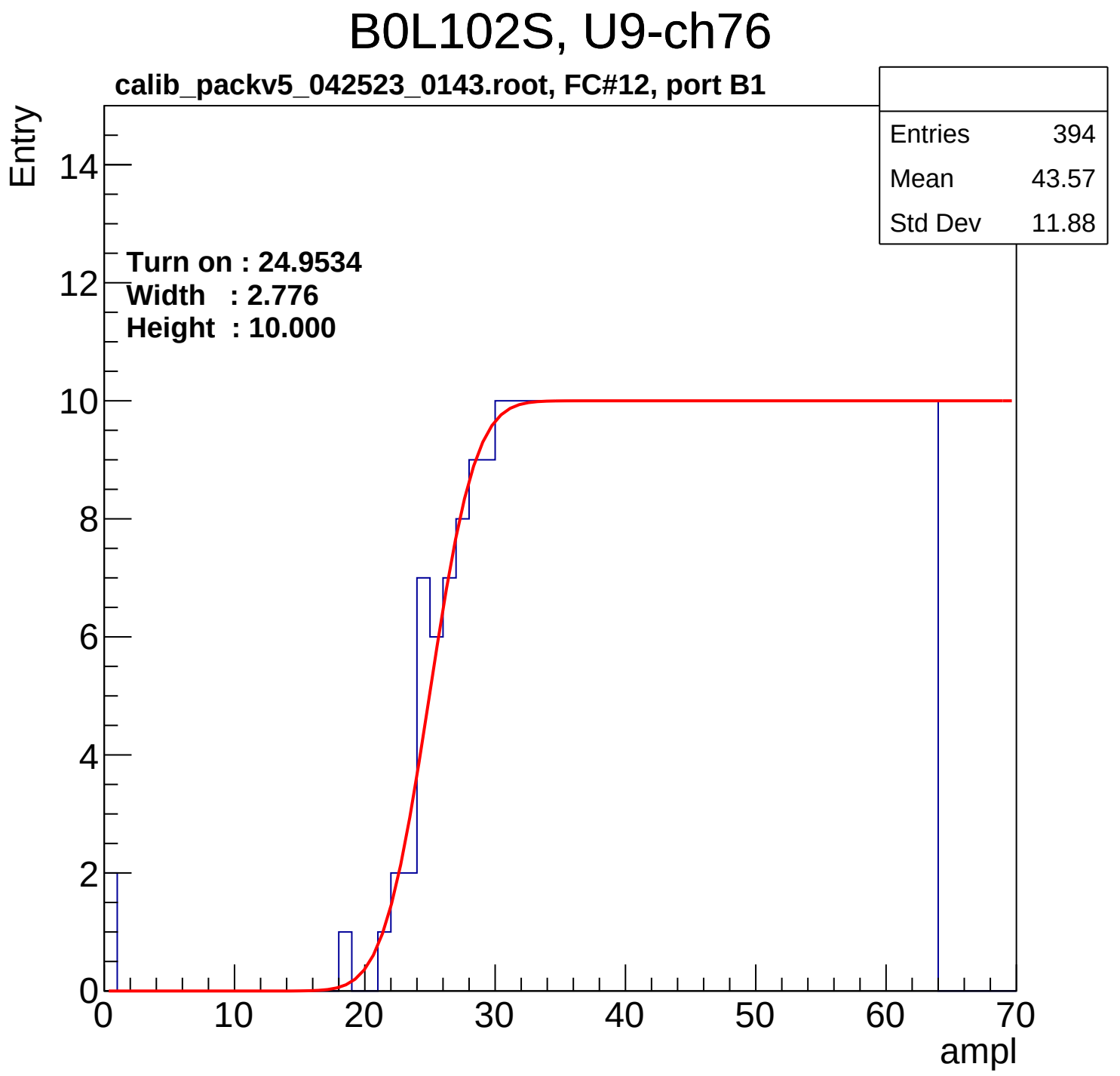

B0L102S, U9-ch71
calib_packv5_042523_0143.root, FC#12, port B1
Entries 381
Mean 44.22
Std Dev 11.53
Turn on : 25.9574
Width : 2.390
Height : 9.930
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

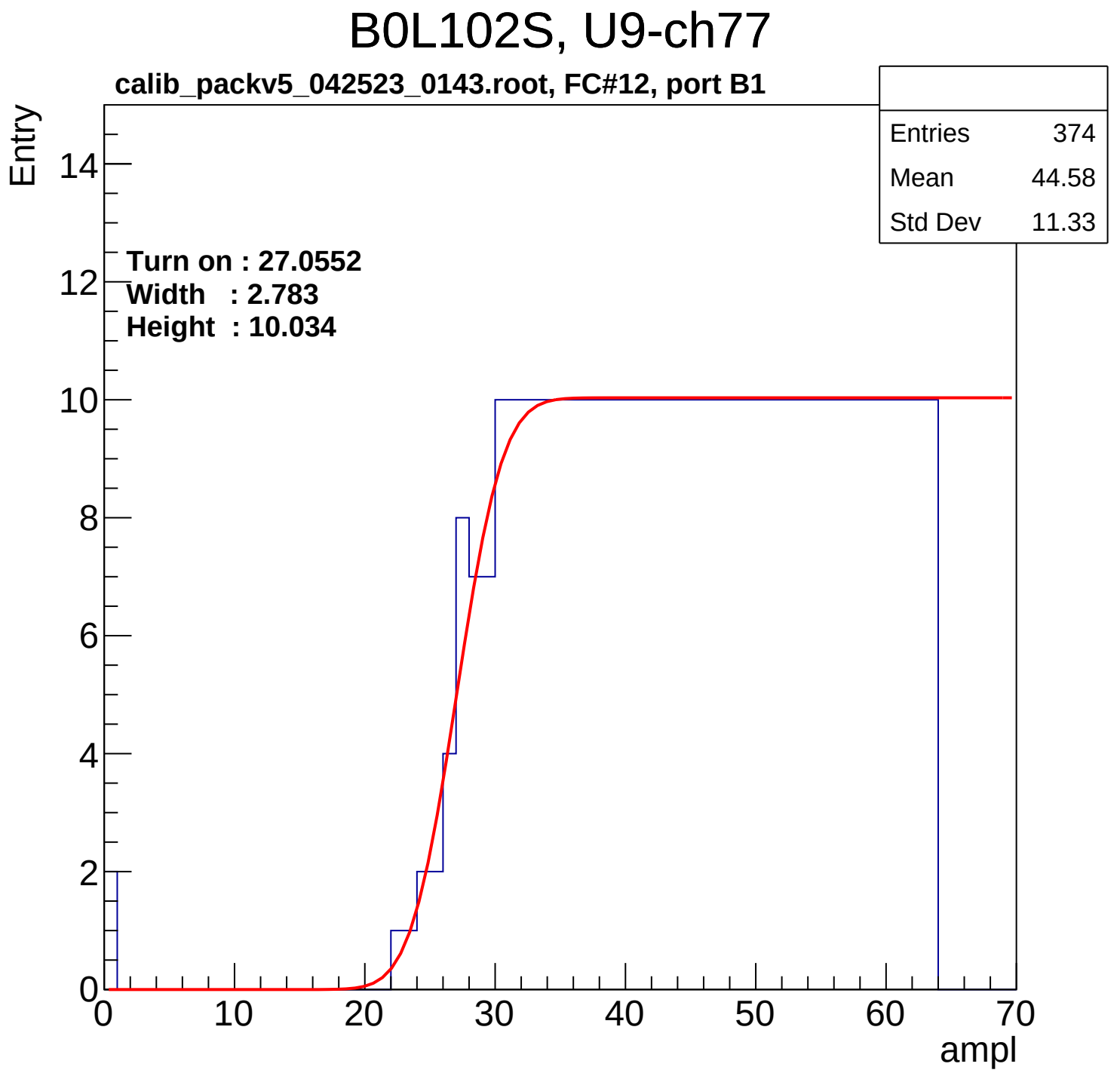

B0L102S, U9-ch72
calib_packv5_042523_0143.root, FC#12, port B1
Entries 387
Mean 43.83
Std Dev 11.9
Turn on : 25.9656
Width : 3.516
Height : 10.026
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

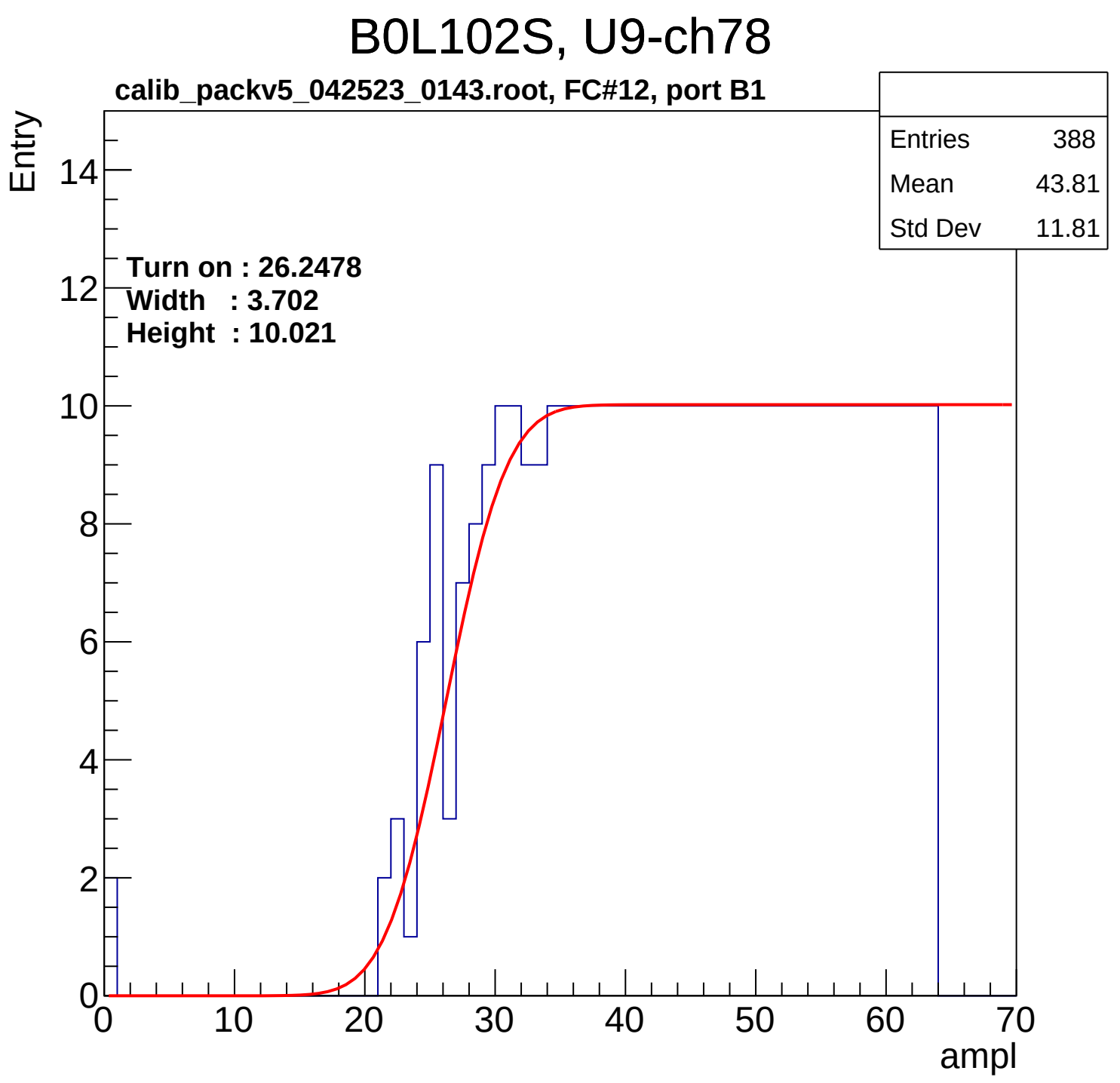

B0L102S, U9-ch73
calib_packv5_042523_0143.root, FC#12, port B1
Entries 369
Mean 44.86
Std Dev 11.07
Turn on : 28.1054
Width : 3.335
Height : 10.105
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

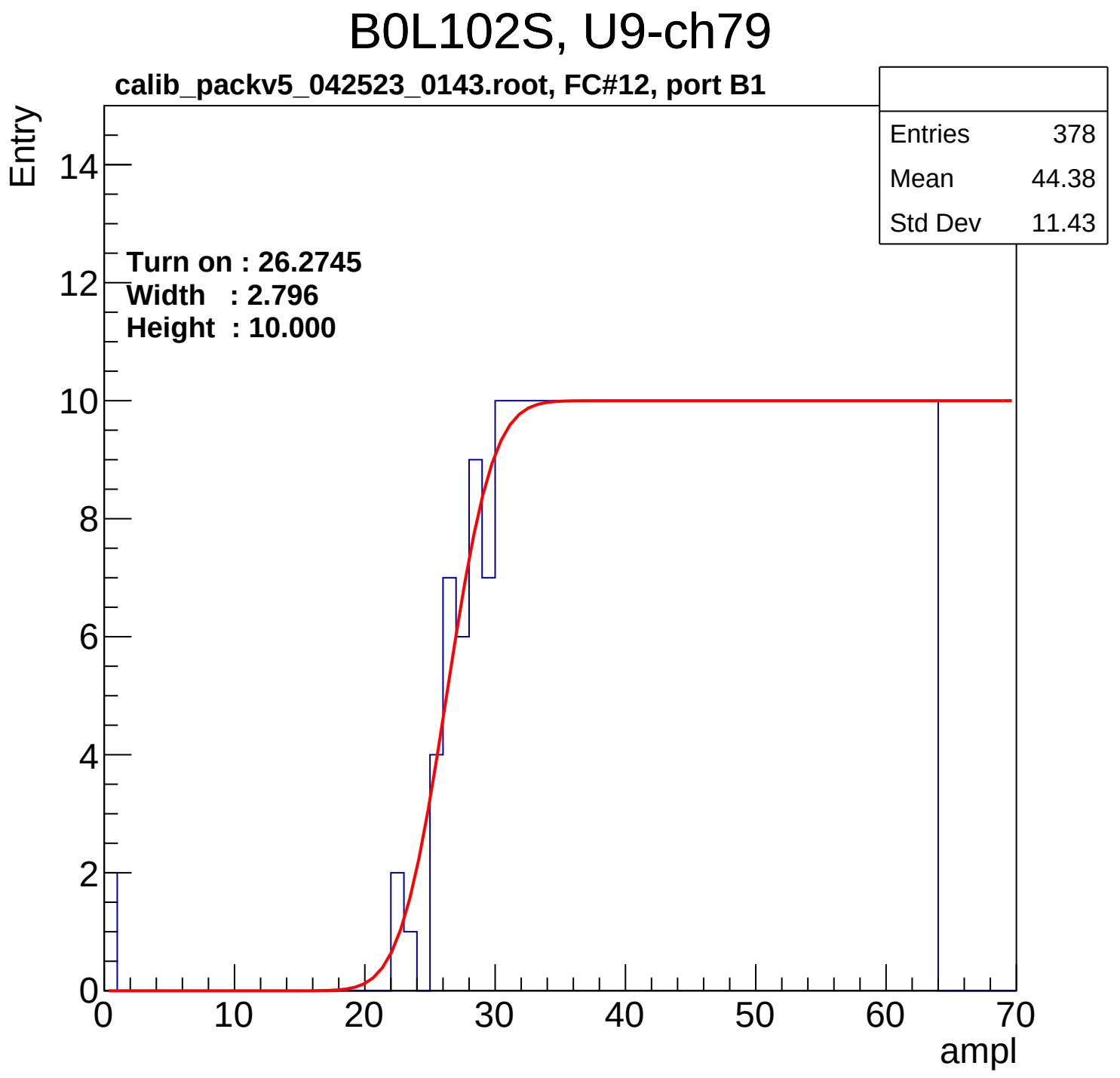

B0L102S, U9-ch74
calib_packv5_042523_0143.root, FC#12, port B1
Entries 381
Mean 44.07
Std Dev 11.85
Turn on : 26.7593
Width : 4.200
Height : 10.066
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

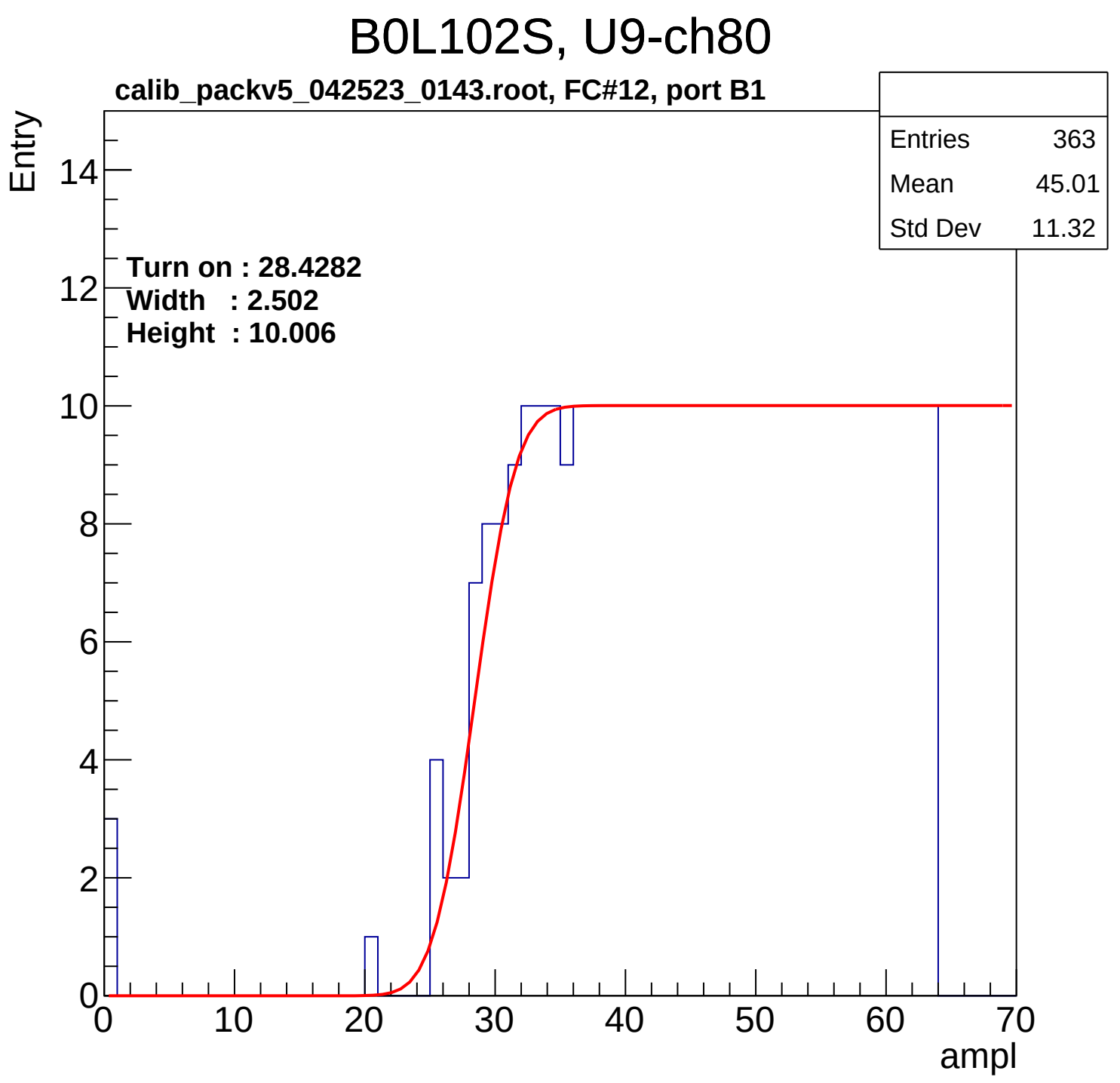

B0L102S, U9-ch75
calib_packv5_042523_0143.root, FC#12, port B1
Entries 382
Mean 44.16
Std Dev 11.57
Turn on : 26.1807
Width : 2.640
Height : 9.978
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

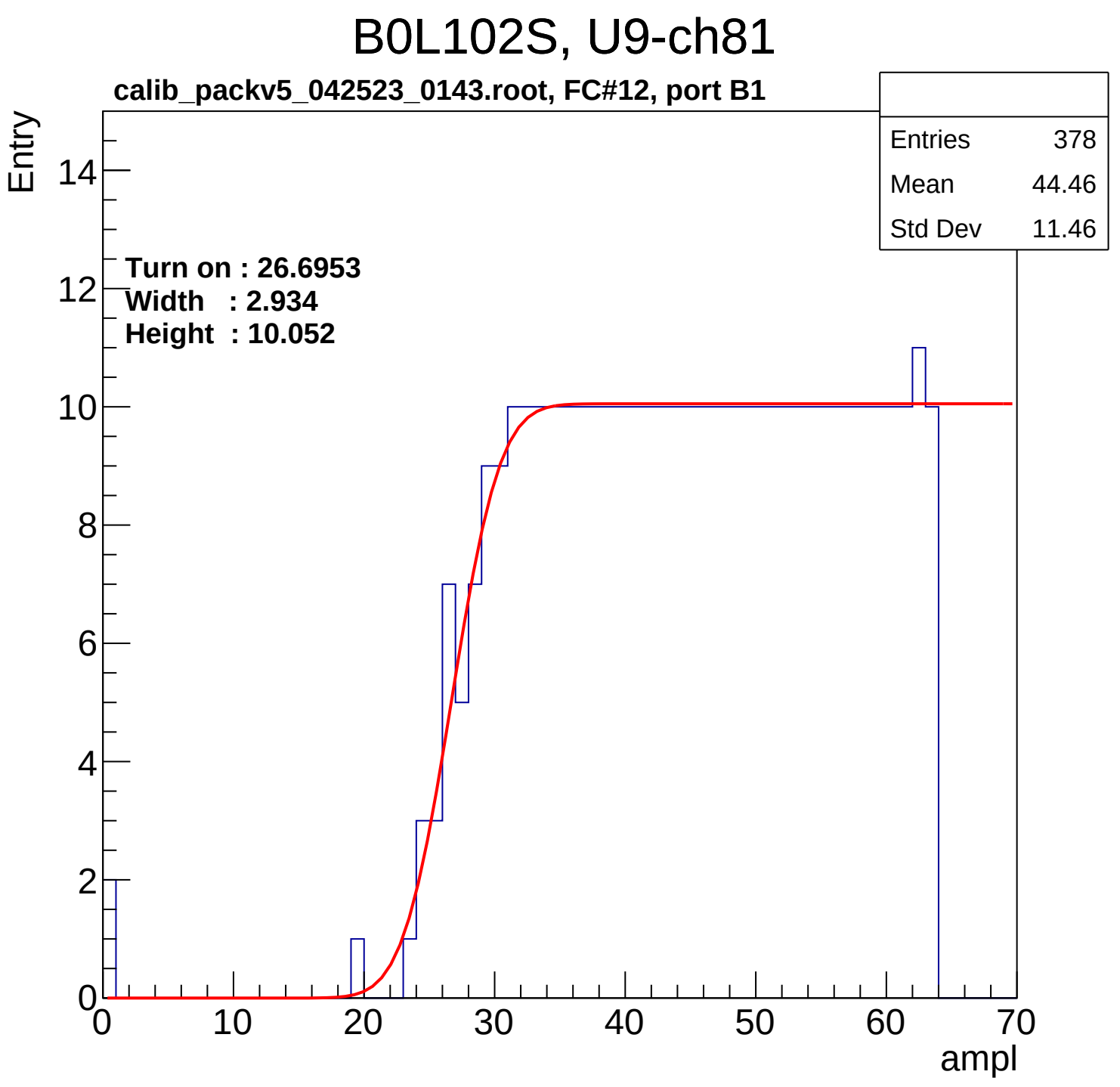

B0L102S, U9-ch76
calib_packv5_042523_0143.root, FC#12, port B1
Entries 394
Mean 43.57
Std Dev 11.88
Turn on : 24.9534
Width : 2.776
Height : 10.000
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

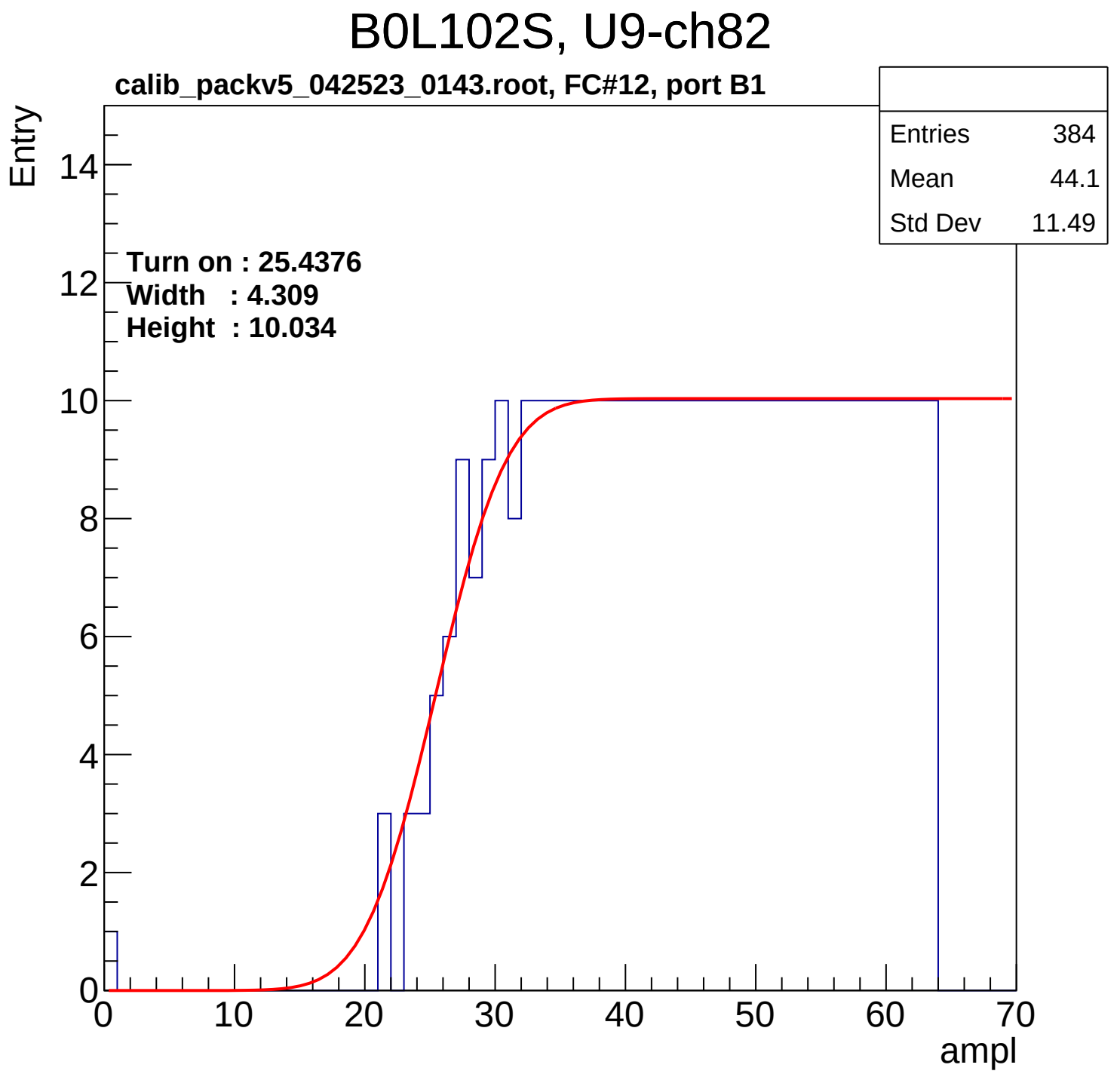

B0L102S, U9-ch77
calib_packv5_042523_0143.root, FC#12, port B1
Entries 374
Mean 44.58
Std Dev 11.33
Turn on : 27.0552
Width : 2.783
Height : 10.034
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

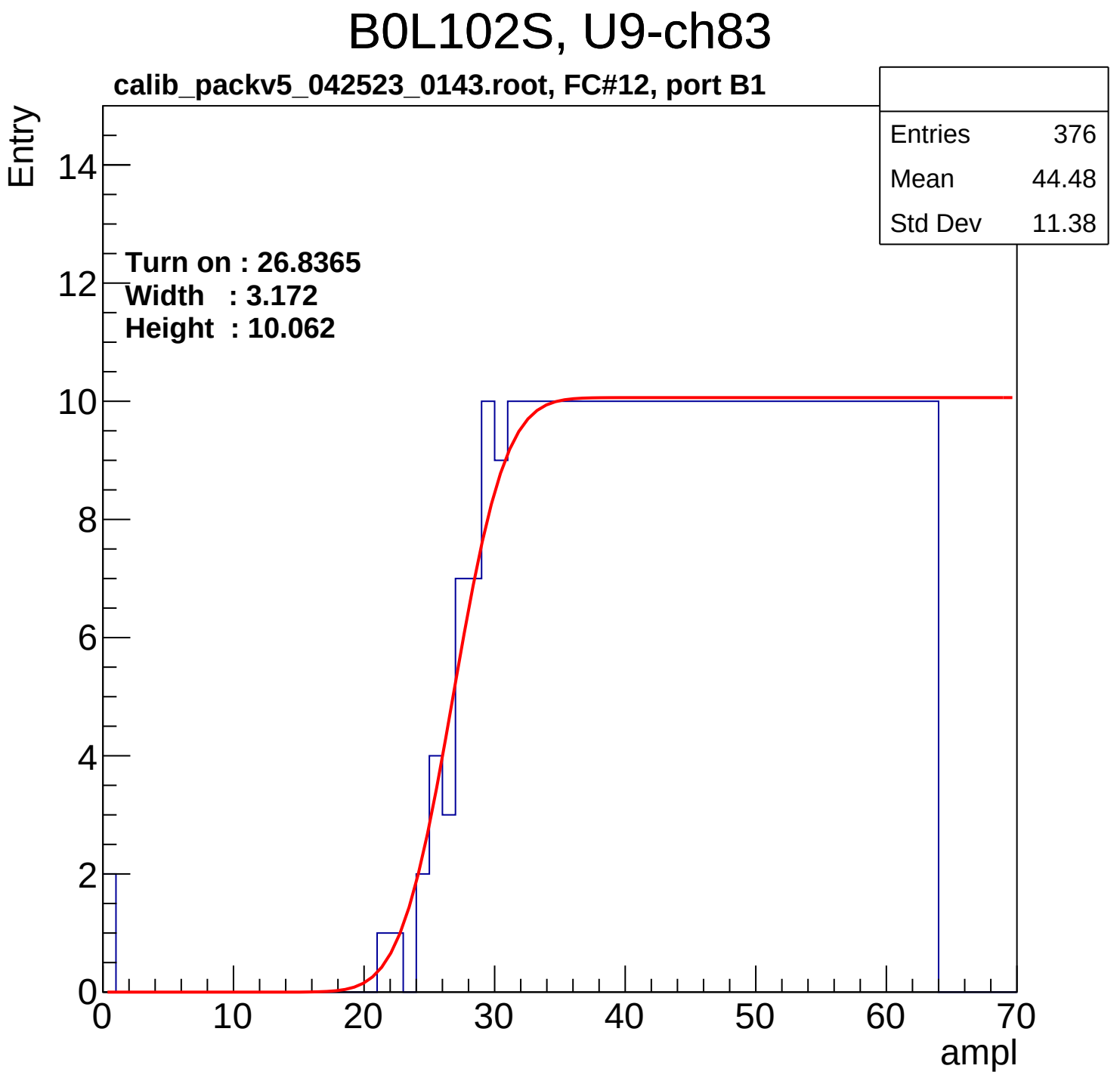

B0L102S, U9-ch78
calib_packv5_042523_0143.root, FC#12, port B1
Entries 388
Mean 43.81
Std Dev 11.81
Turn on : 26.2478
Width : 3.702
Height : 10.021
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

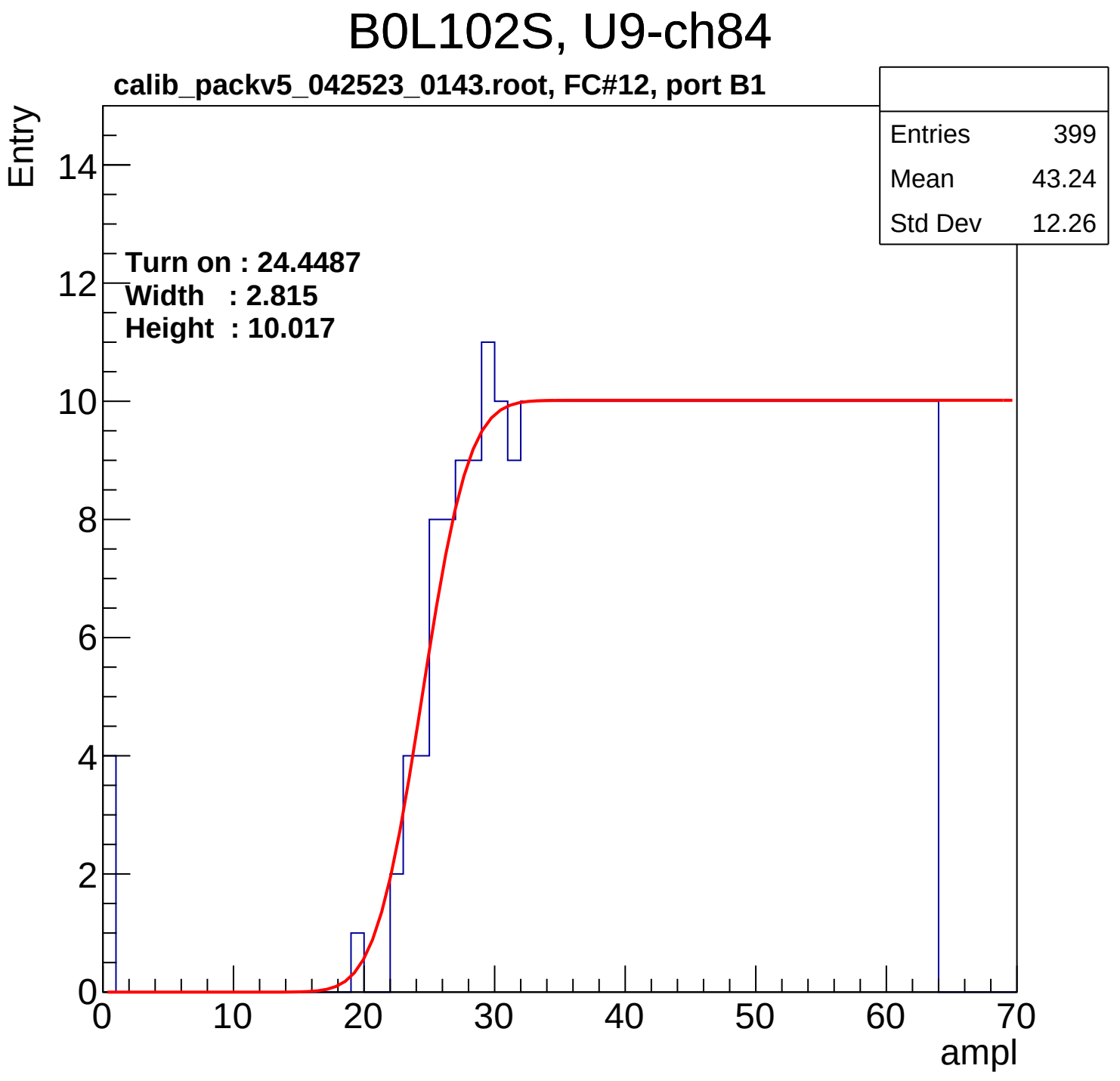

B0L102S, U9-ch79
calib_packv5_042523_0143.root, FC#12, port B1
Entries 378
Mean 44.38
Std Dev 11.43
Turn on : 26.2745
Width : 2.796
Height : 10.000
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

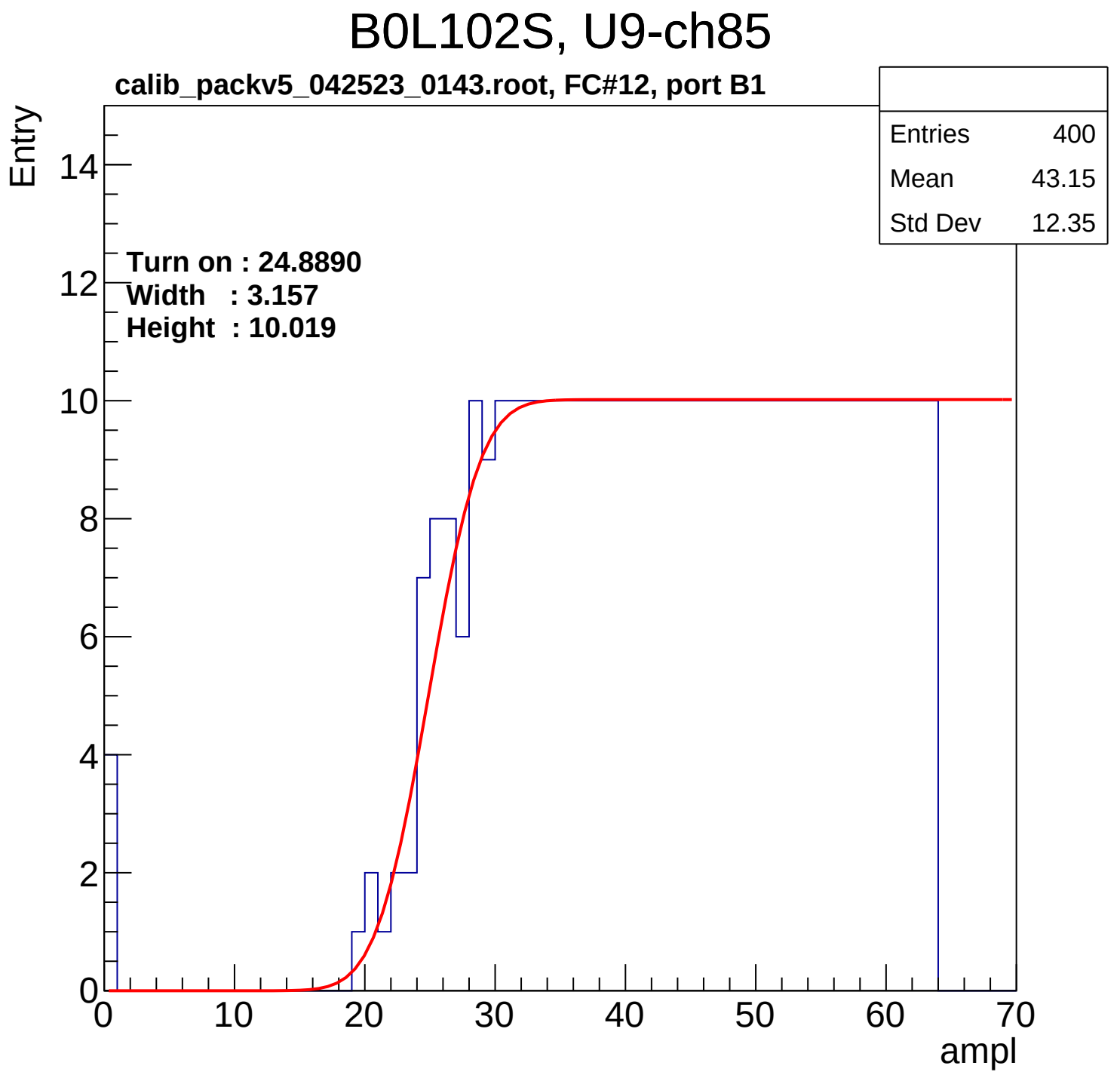

B0L102S, U9-ch80
calib_packv5_042523_0143.root, FC#12, port B1
Entries 363
Mean 45.01
Std Dev 11.32
Turn on : 28.4282
Width : 2.502
Height : 10.006
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

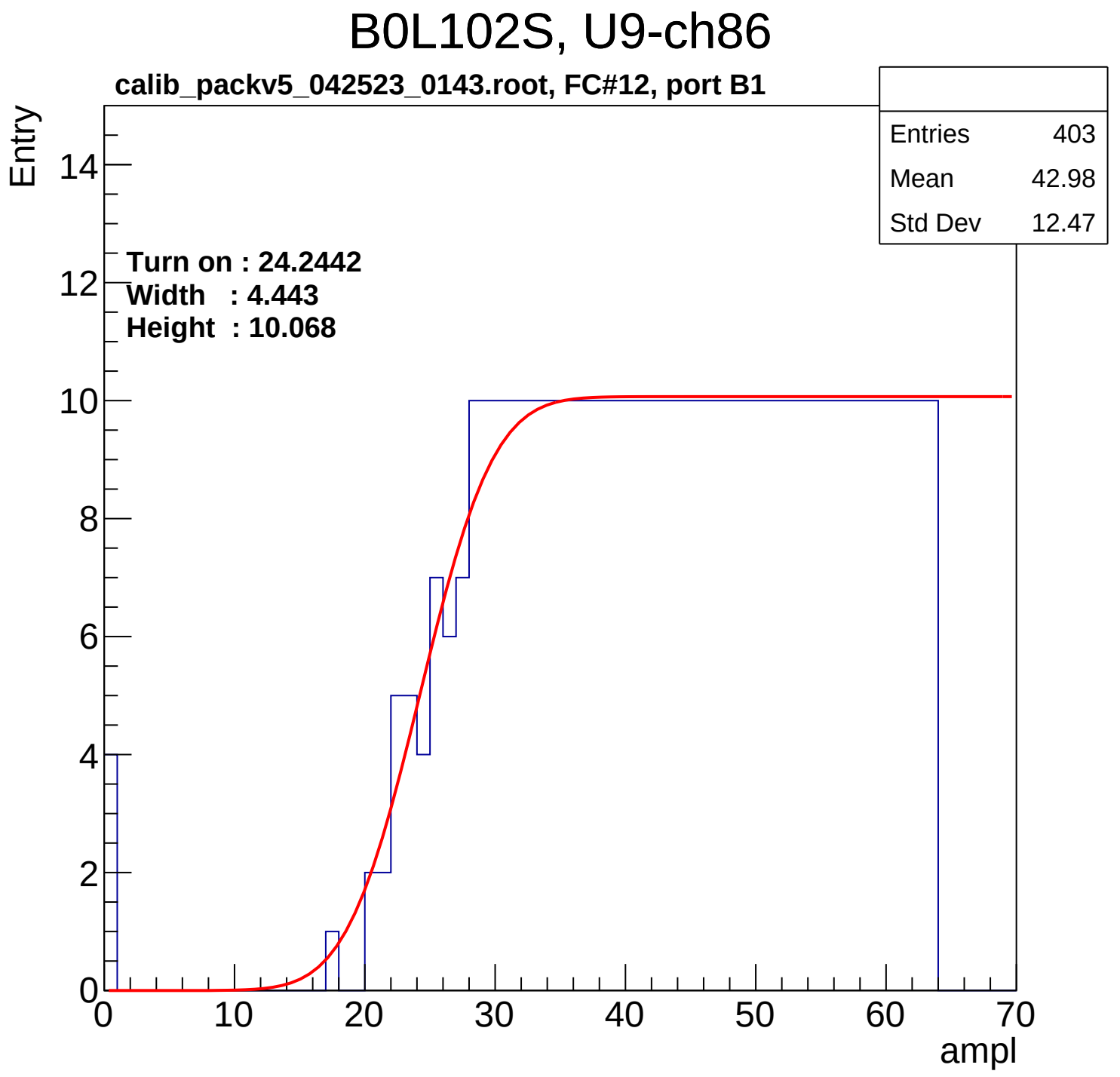

B0L102S, U9-ch81
calib_packv5_042523_0143.root, FC#12, port B1
Entries 378
Mean 44.46
Std Dev 11.46
Turn on : 26.6953
Width : 2.934
Height : 10.052
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

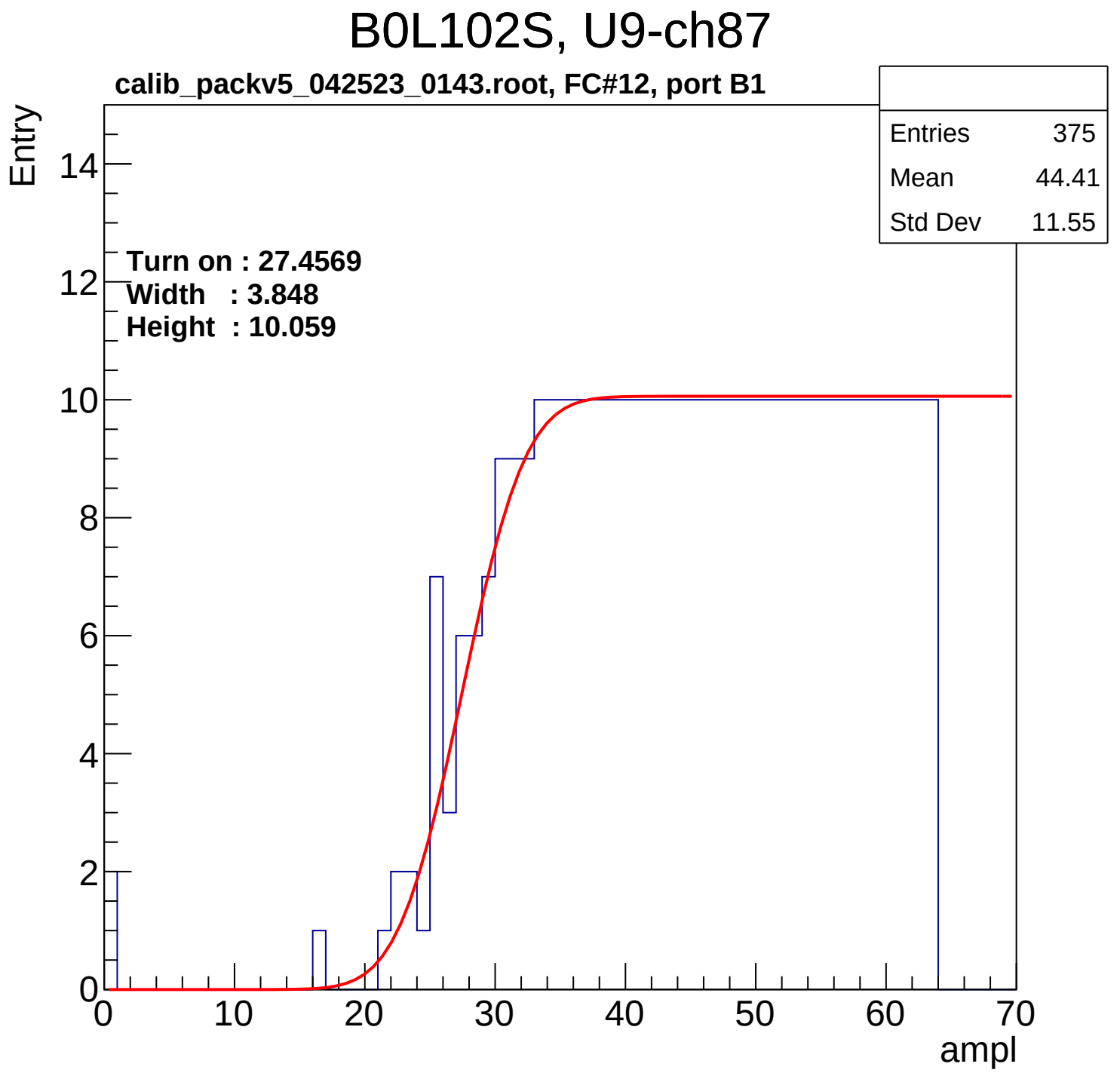

B0L102S, U9-ch82
calib_packv5_042523_0143.root, FC#12, port B1
Entries 384
Mean 44.1
Std Dev 11.49
Turn on : 25.4376
Width : 4.309
Height : 10.034
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

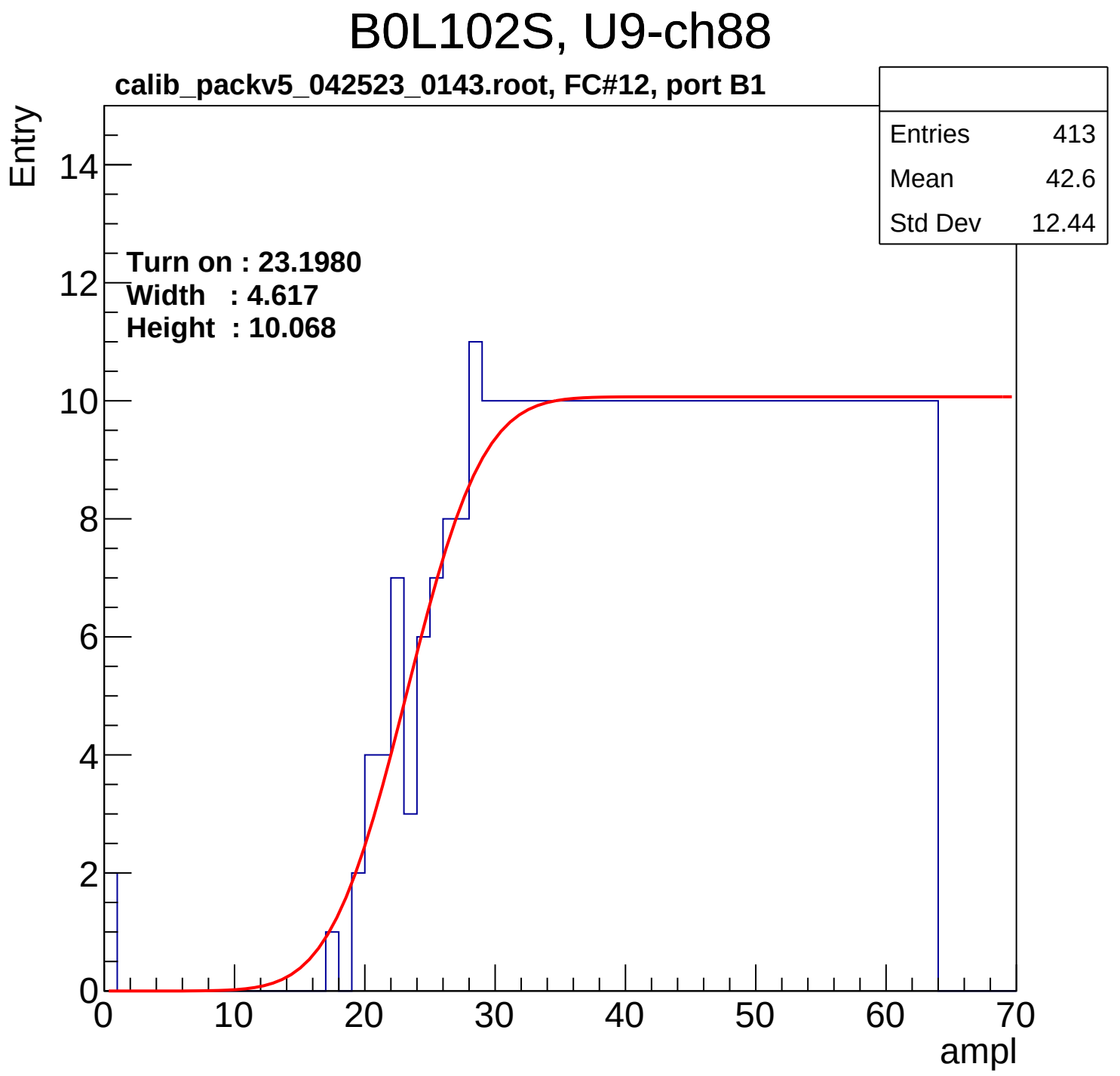

B0L102S, U9-ch83
calib_packv5_042523_0143.root, FC#12, port B1
Entries 376
Mean 44.48
Std Dev 11.38
Turn on : 26.8365
Width : 3.172
Height : 10.062
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

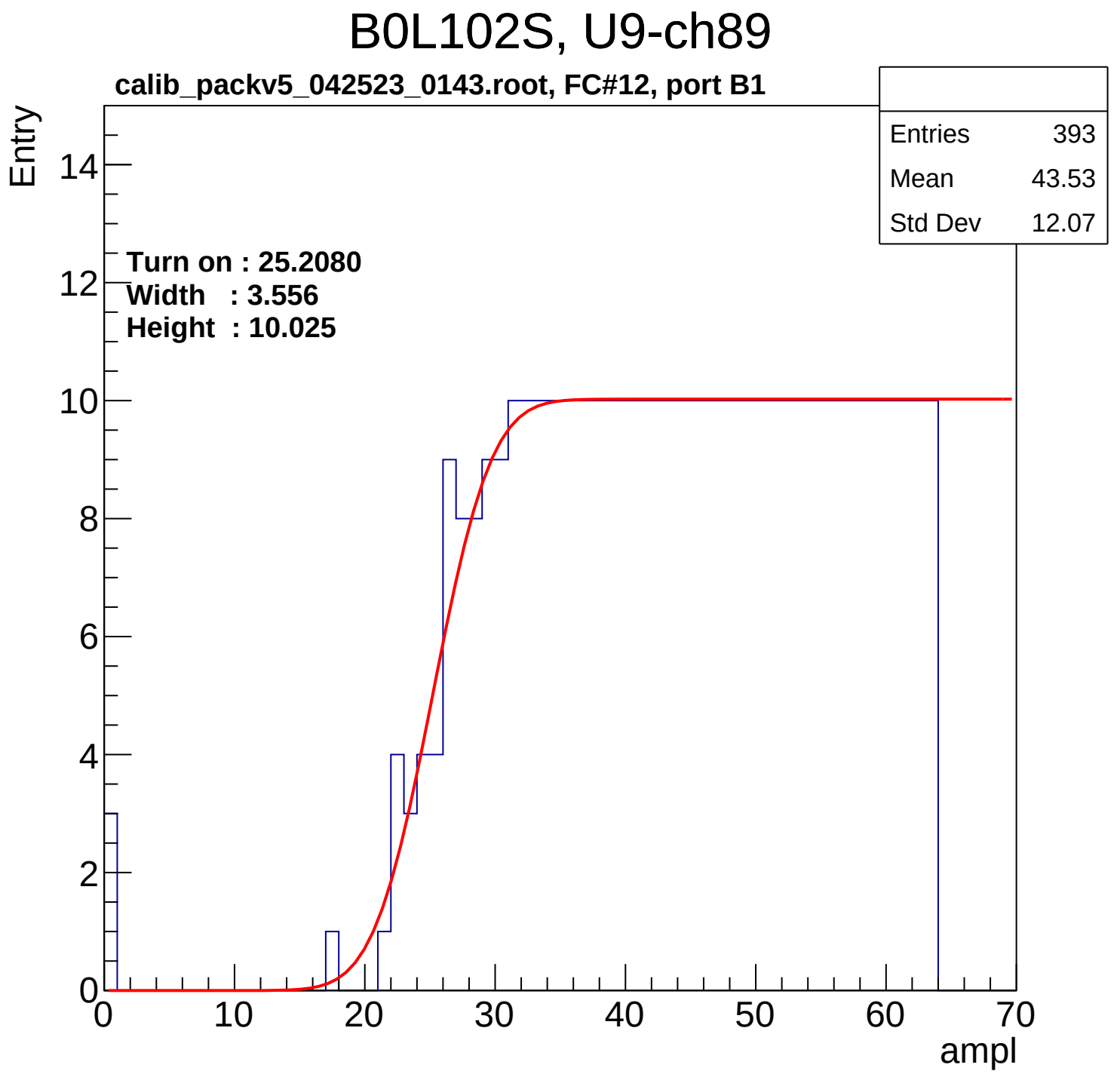

B0L102S, U9-ch84
calib_packv5_042523_0143.root, FC#12, port B1
Entries 399
Mean 43.24
Std Dev 12.26
Turn on : 24.4487
Width : 2.815
Height : 10.017
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

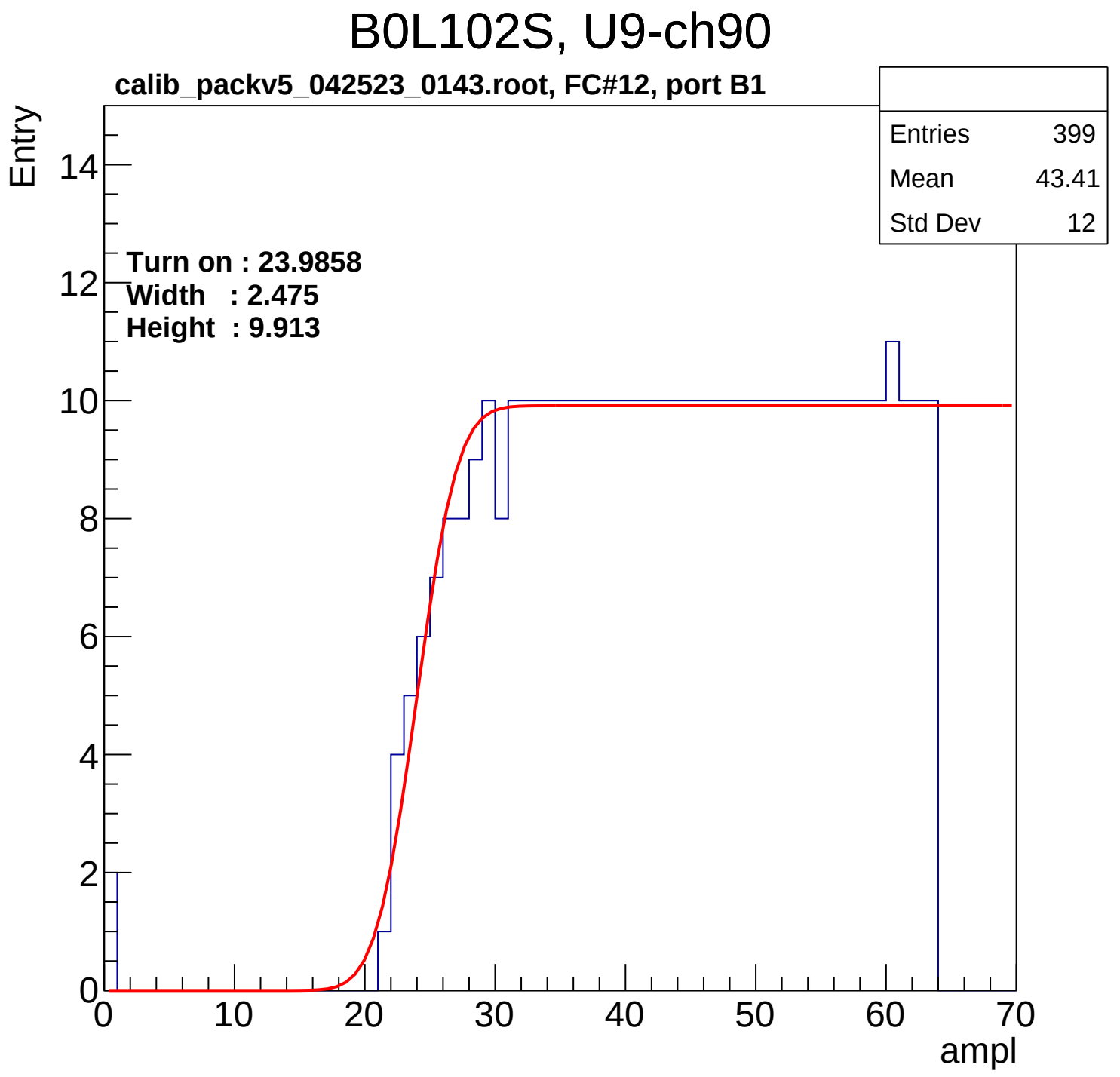

B0L102S, U9-ch85
calib_packv5_042523_0143.root, FC#12, port B1
Entries 400
Mean 43.15
Std Dev 12.35
Turn on : 24.8890
Width : 3.157
Height : 10.019
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

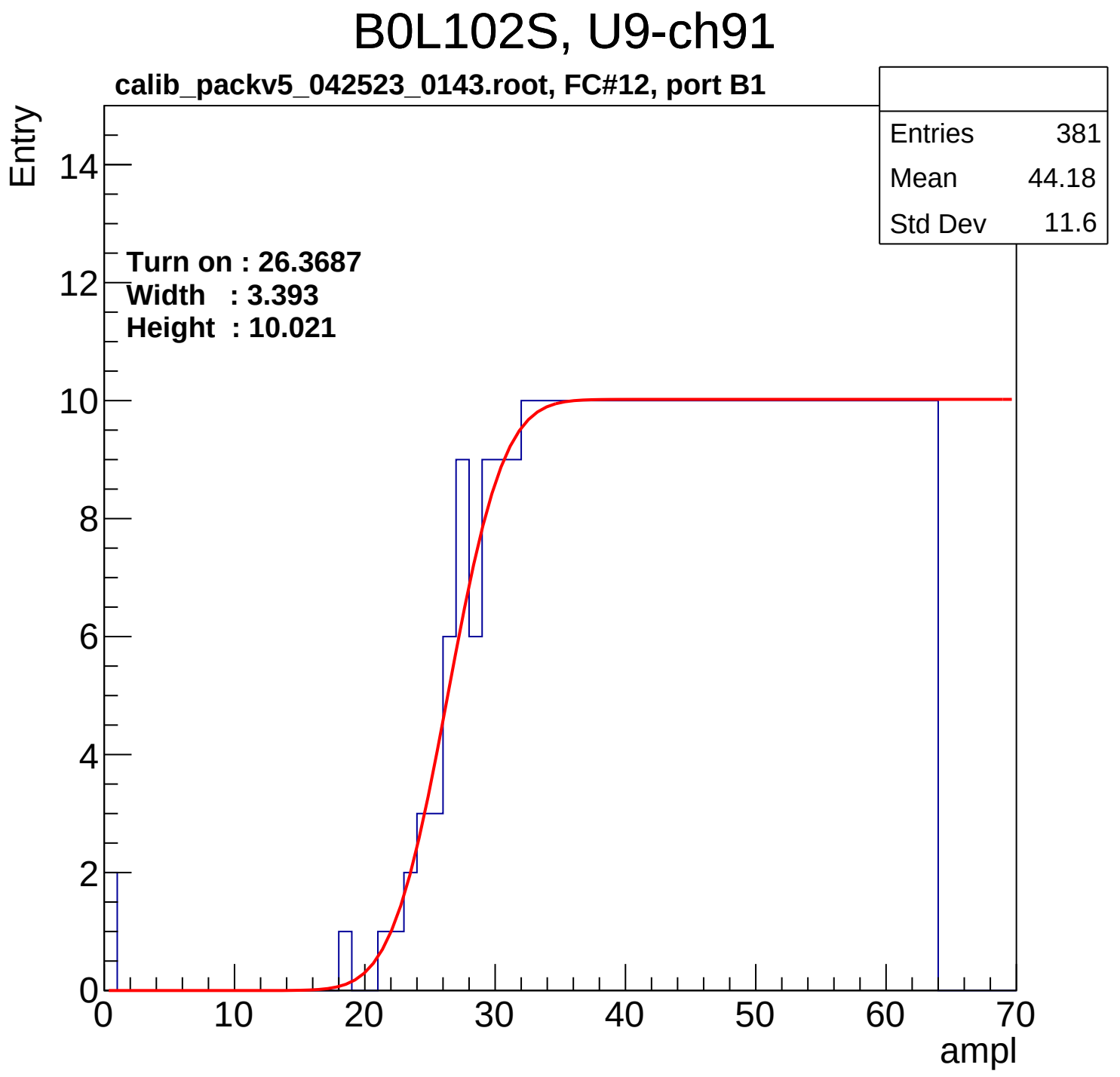

B0L102S, U9-ch86
calib_packv5_042523_0143.root, FC#12, port B1
Entries 403
Mean 42.98
Std Dev 12.47
Turn on : 24.2442
Width : 4.443
Height : 10.068
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

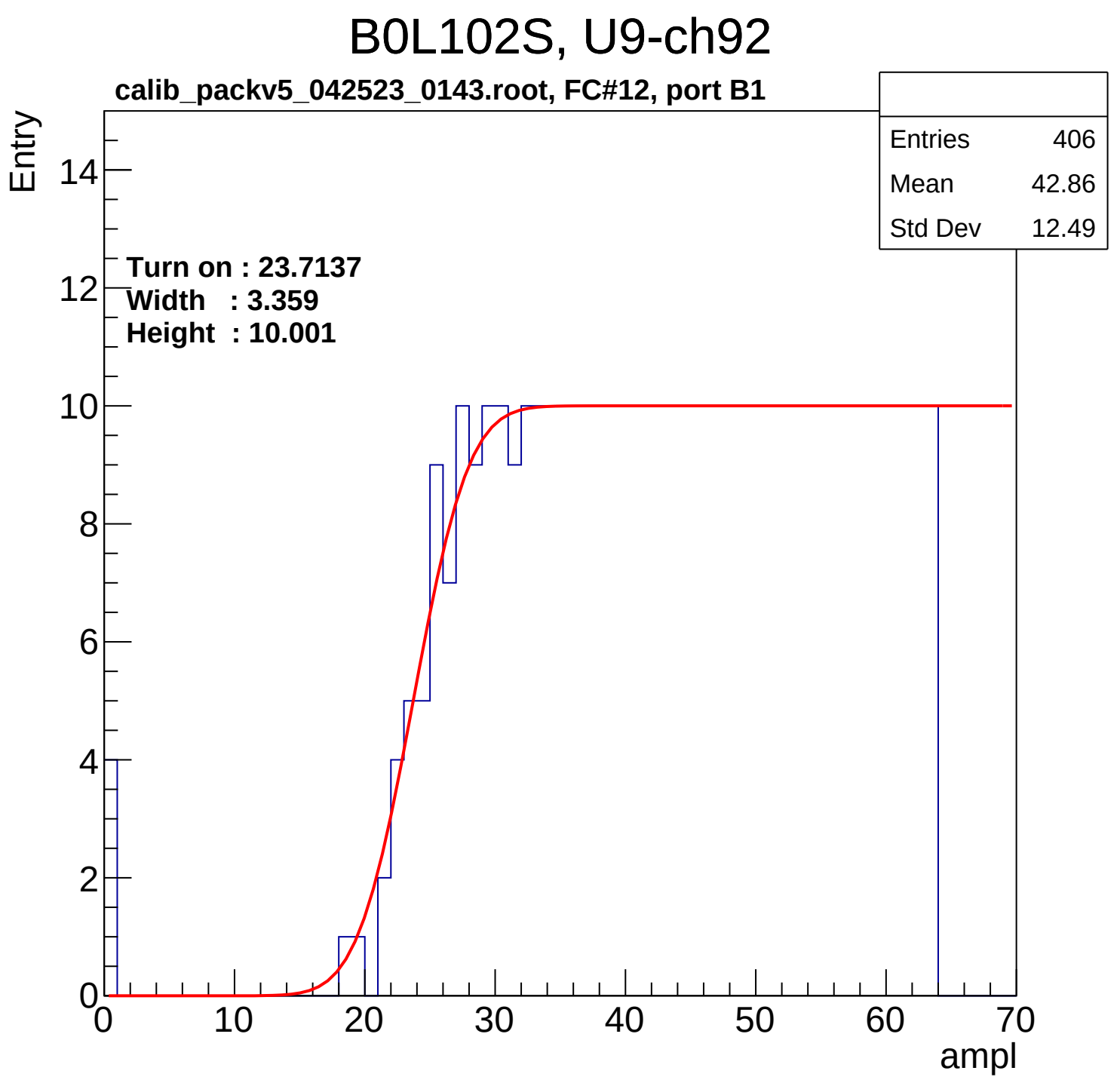

B0L102S, U9-ch87
calib_packv5_042523_0143.root, FC#12, port B1
Entries 375
Mean 44.41
Std Dev 11.55
Turn on : 27.4569
Width : 3.848
Height : 10.059
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

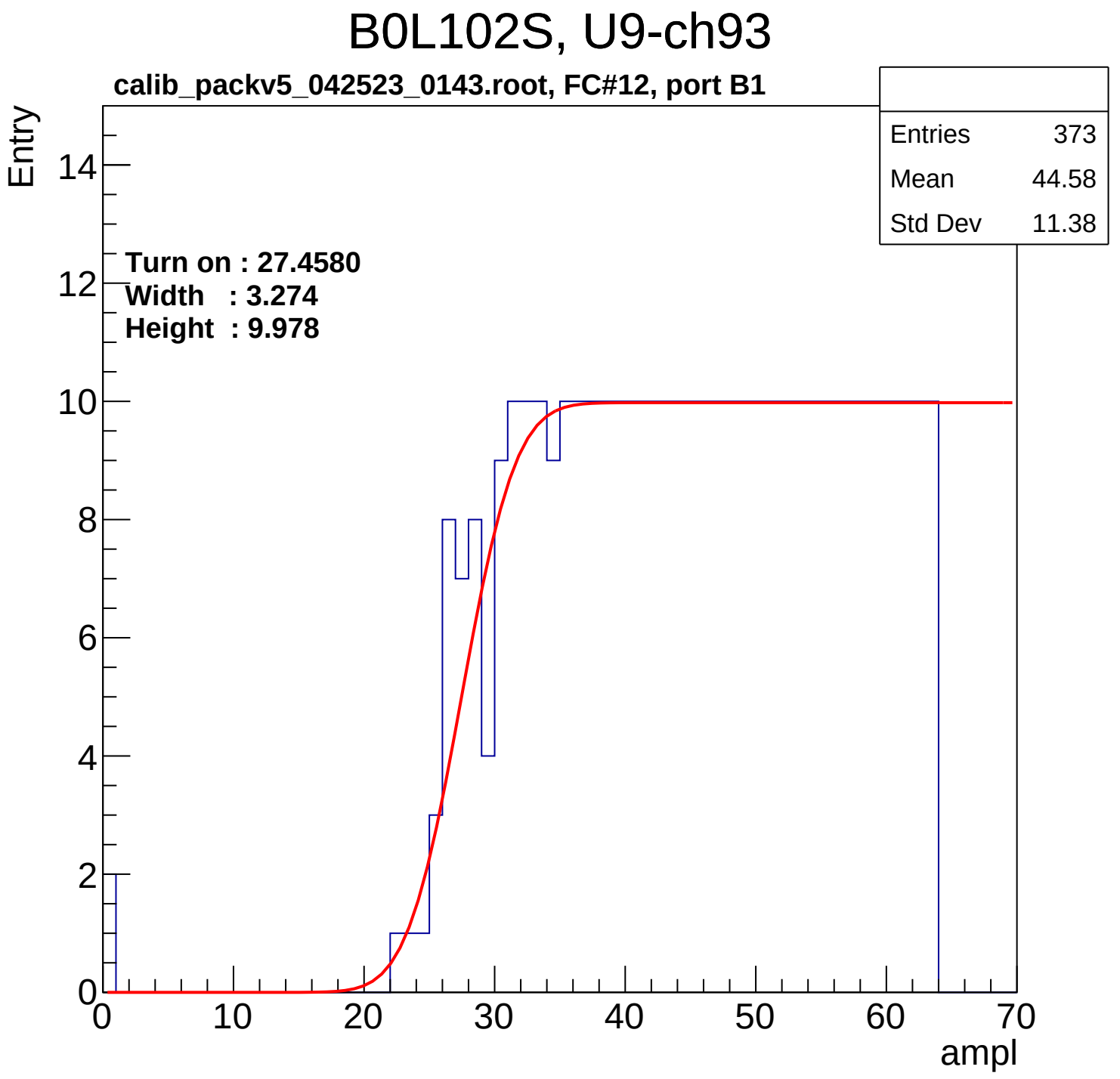

B0L102S, U9-ch88
calib_packv5_042523_0143.root, FC#12, port B1
Entries 413
Mean 42.6
Std Dev 12.44
Turn on : 23.1980
Width : 4.617
Height : 10.068
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

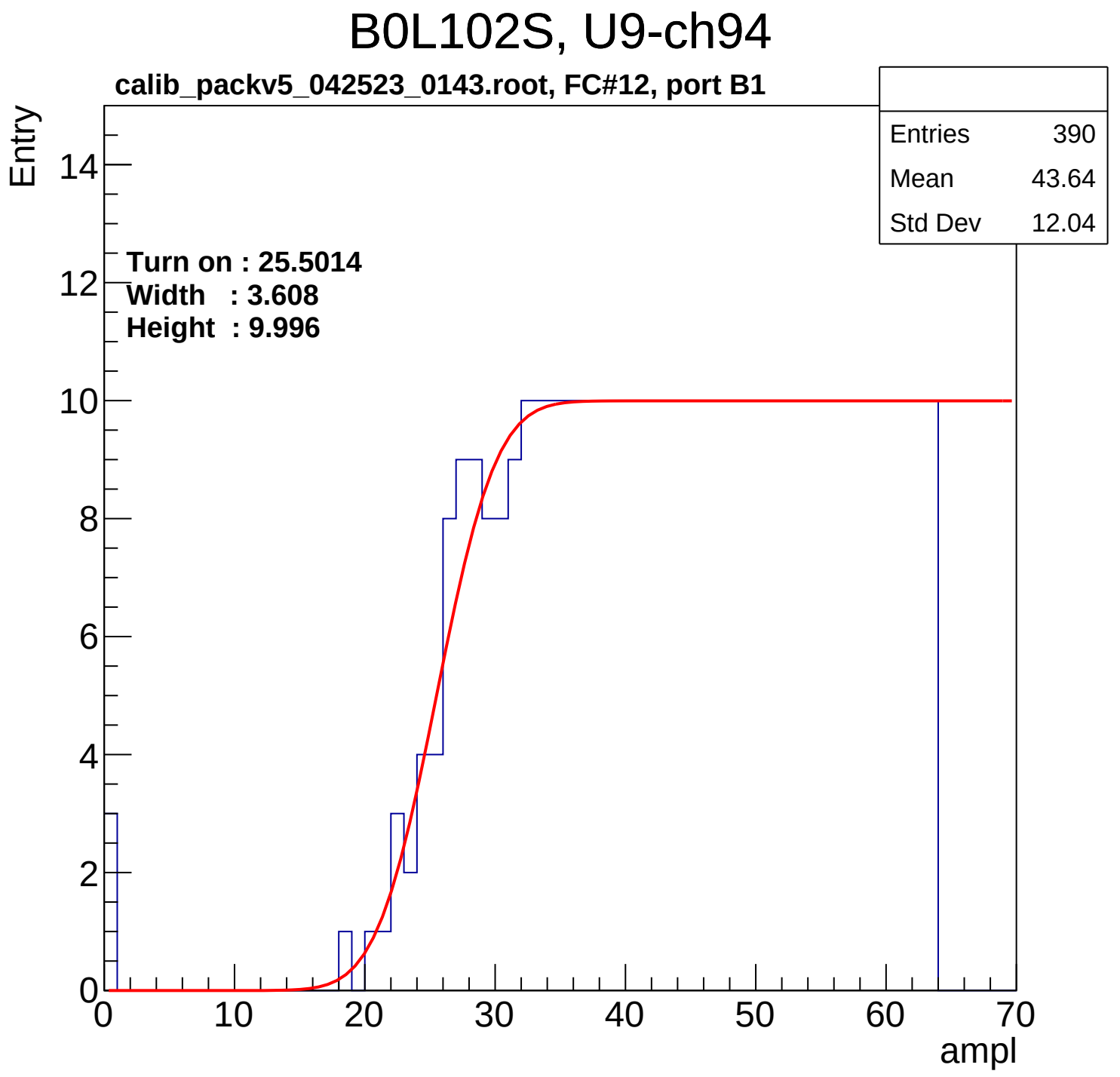

B0L102S, U9-ch89
calib_packv5_042523_0143.root, FC#12, port B1
Entries 393
Mean 43.53
Std Dev 12.07
Turn on : 25.2080
Width : 3.556
Height : 10.025
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

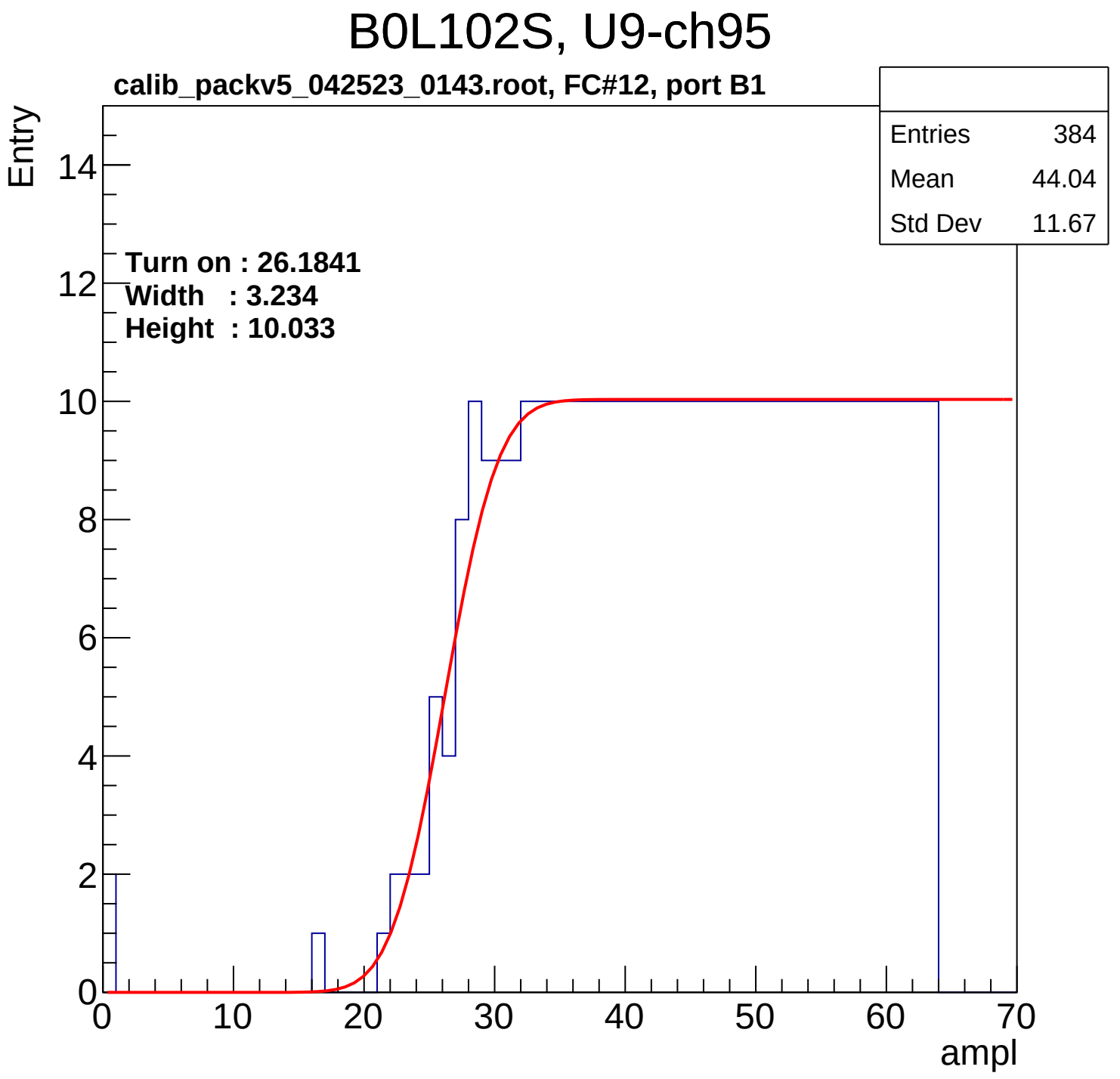

B0L102S, U9-ch90
calib_packv5_042523_0143.root, FC#12, port B1
Entries 399
Mean 43.41
Std Dev 12
Turn on : 23.9858
Width : 2.475
Height : 9.913
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

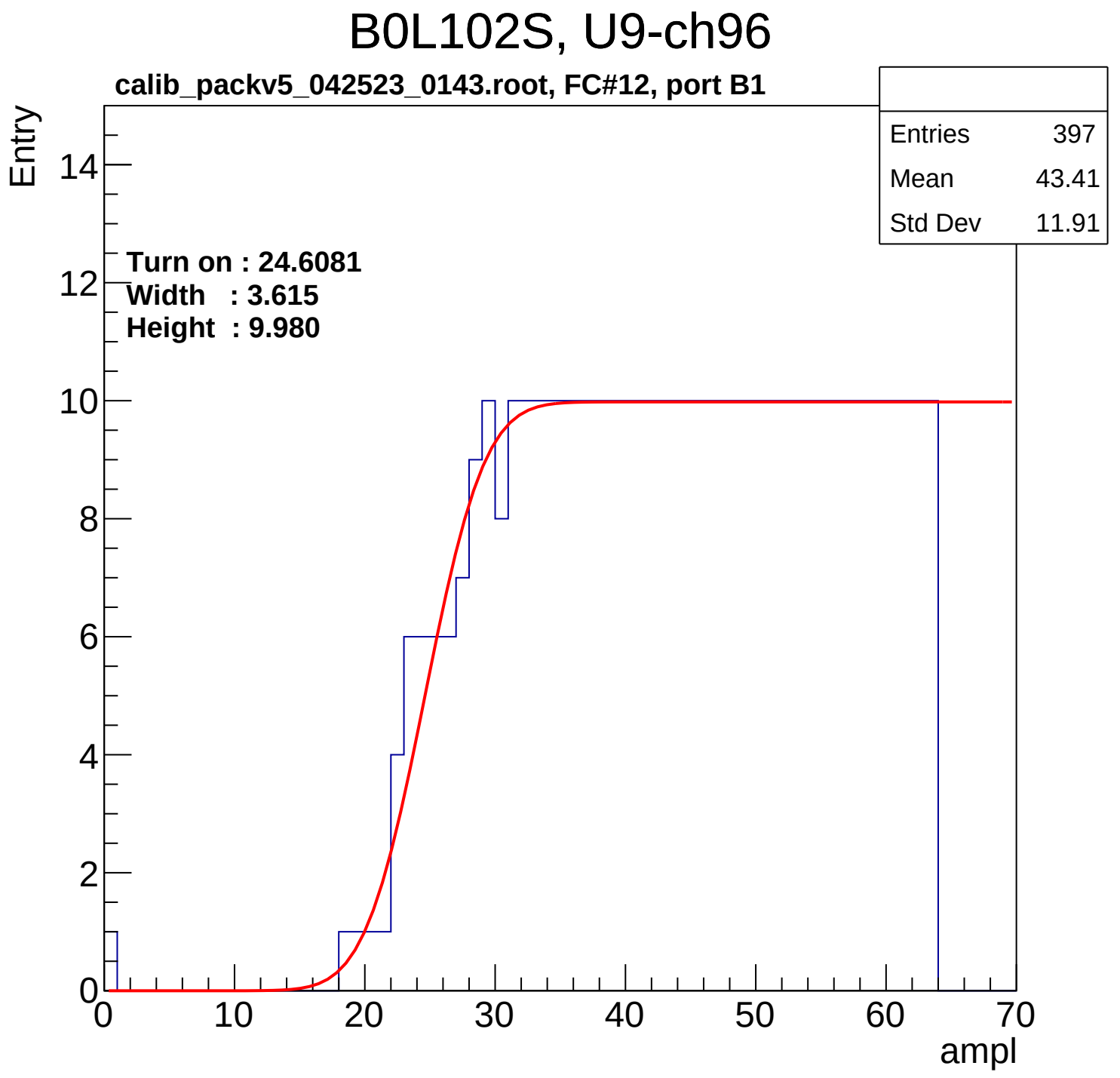

B0L102S, U9-ch91
calib_packv5_042523_0143.root, FC#12, port B1
Entries 381
Mean 44.18
Std Dev 11.6
Turn on : 26.3687
Width : 3.393
Height : 10.021
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

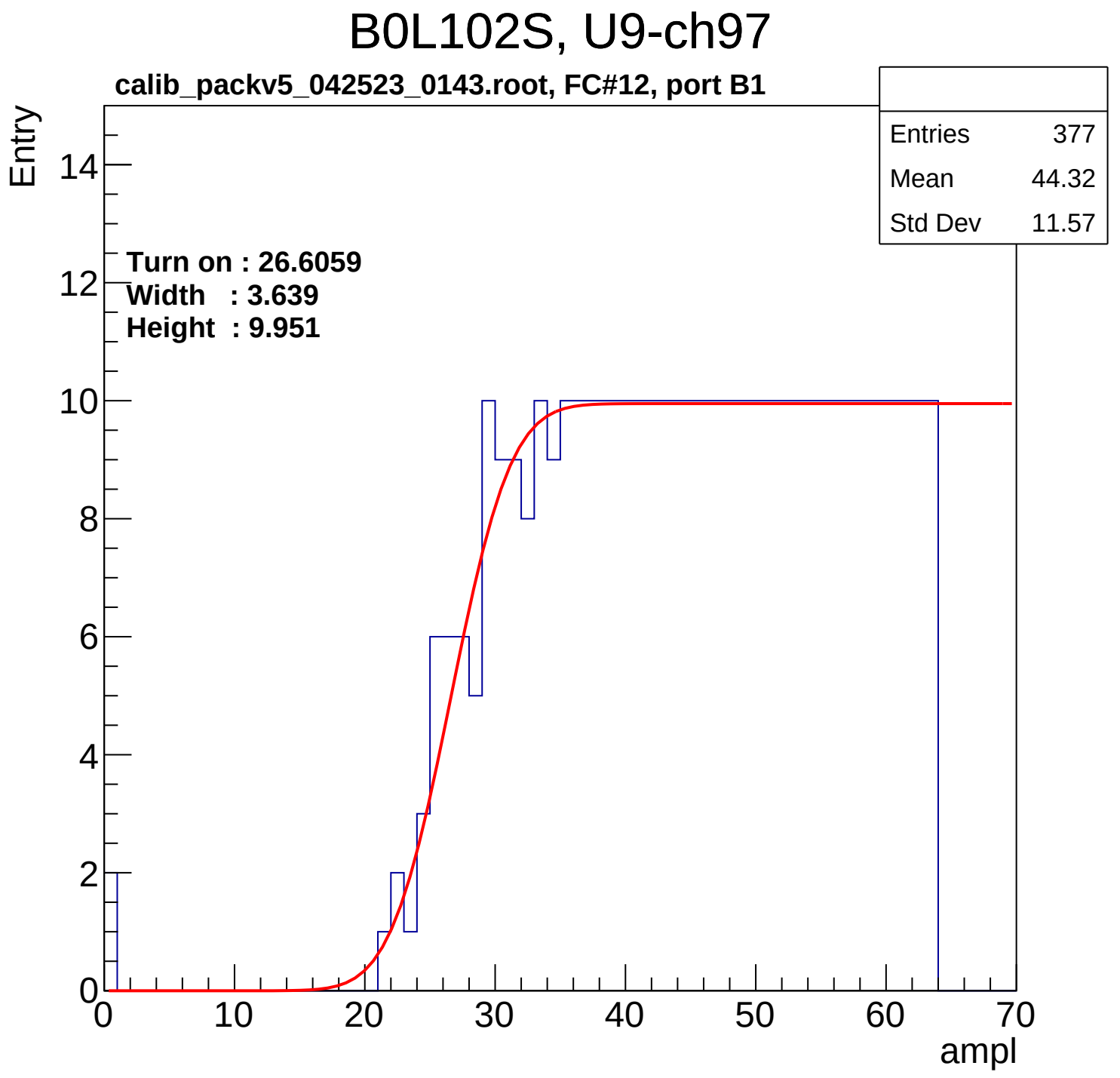

B0L102S, U9-ch92
calib_packv5_042523_0143.root, FC#12, port B1
Entries 406
Mean 42.86
Std Dev 12.49
Turn on : 23.7137
Width : 3.359
Height : 10.001
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

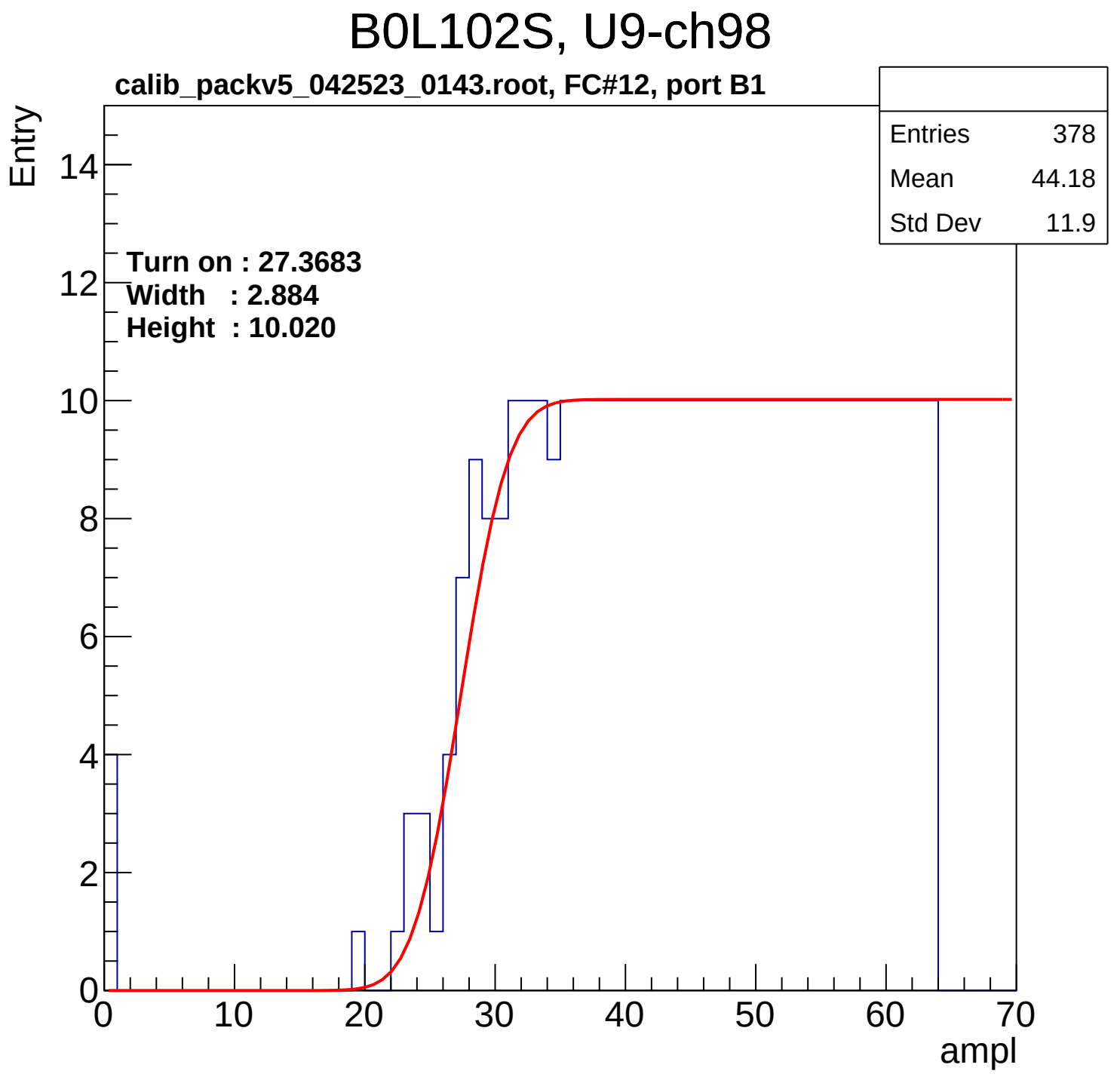

B0L102S, U9-ch93
calib_packv5_042523_0143.root, FC#12, port B1
Entries 373
Mean 44.58
Std Dev 11.38
Turn on : 27.4580
Width : 3.274
Height : 9.978
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

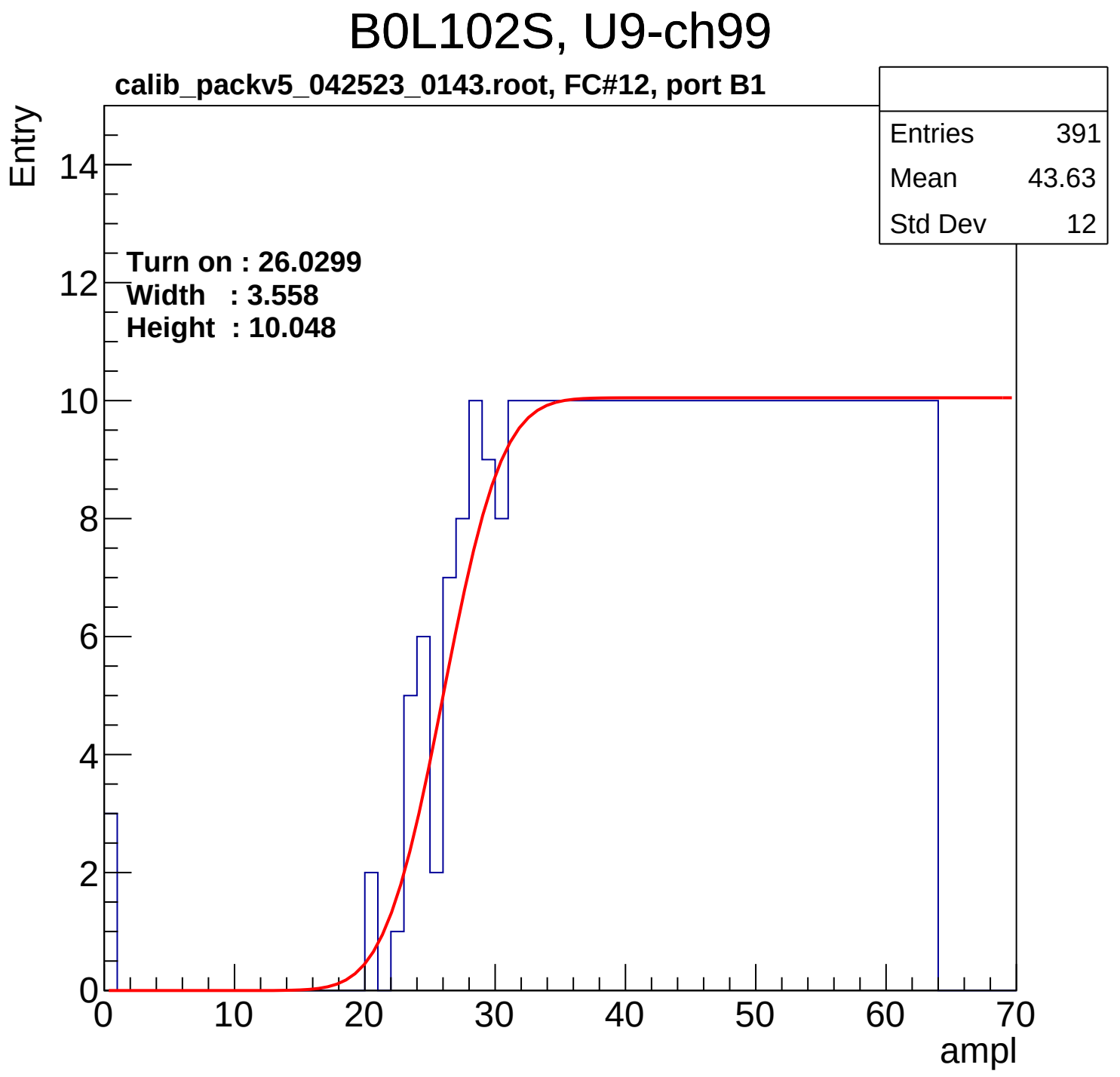

B0L102S, U9-ch94
calib_packv5_042523_0143.root, FC#12, port B1
Entries 390
Mean 43.64
Std Dev 12.04
Turn on : 25.5014
Width : 3.608
Height : 9.996
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

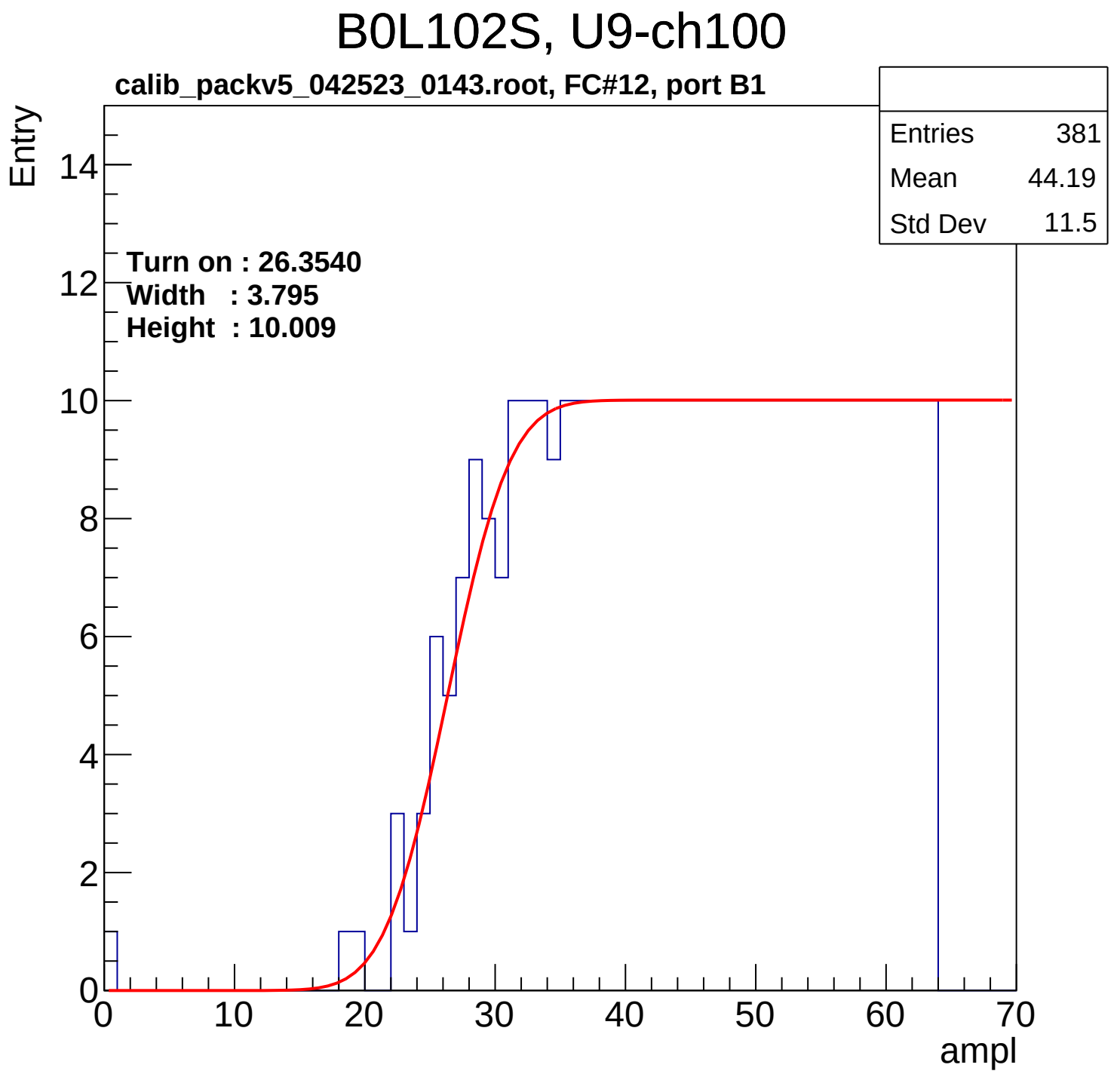

B0L102S, U9-ch95
calib_packv5_042523_0143.root, FC#12, port B1
Entries 384
Mean 44.04
Std Dev 11.67
Turn on : 26.1841
Width : 3.234
Height : 10.033
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

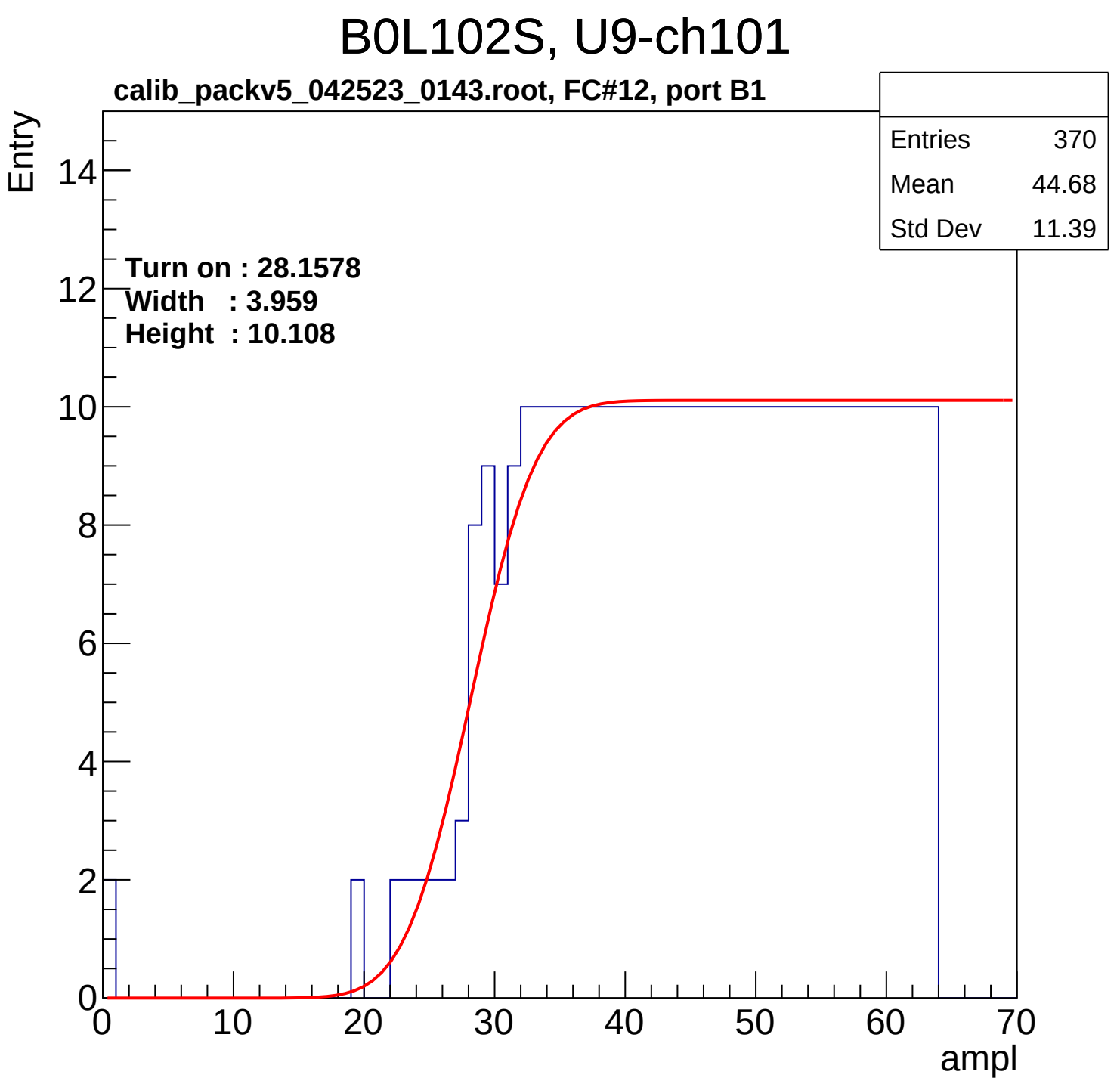

B0L102S, U9-ch96
calib_packv5_042523_0143.root, FC#12, port B1
Entries 397
Mean 43.41
Std Dev 11.91
Turn on : 24.6081
Width : 3.615
Height : 9.980
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

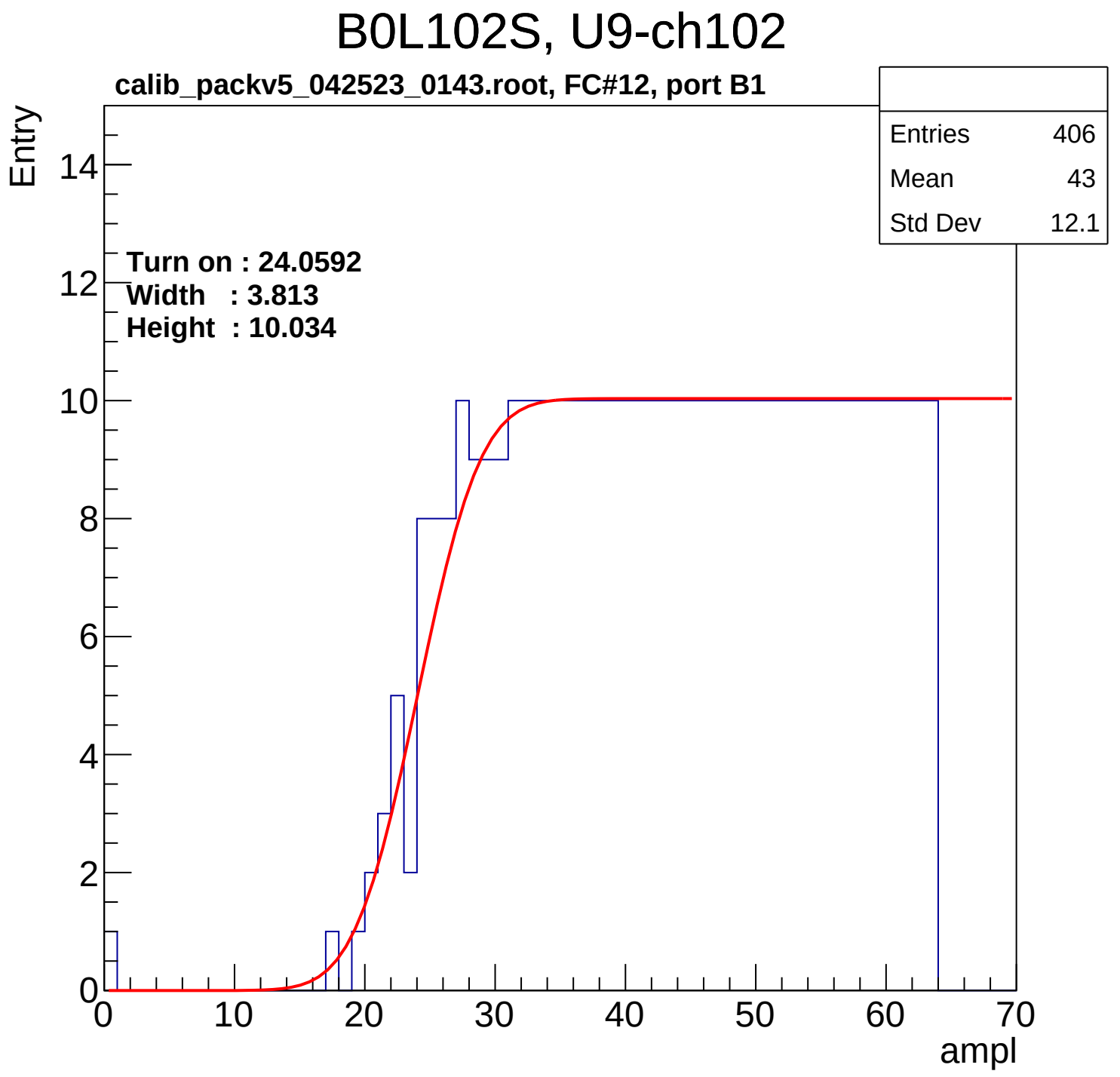

B0L102S, U9-ch97
calib_packv5_042523_0143.root, FC#12, port B1
Entries 377
Mean 44.32
Std Dev 11.57
Turn on : 26.6059
Width : 3.639
Height : 9.951
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

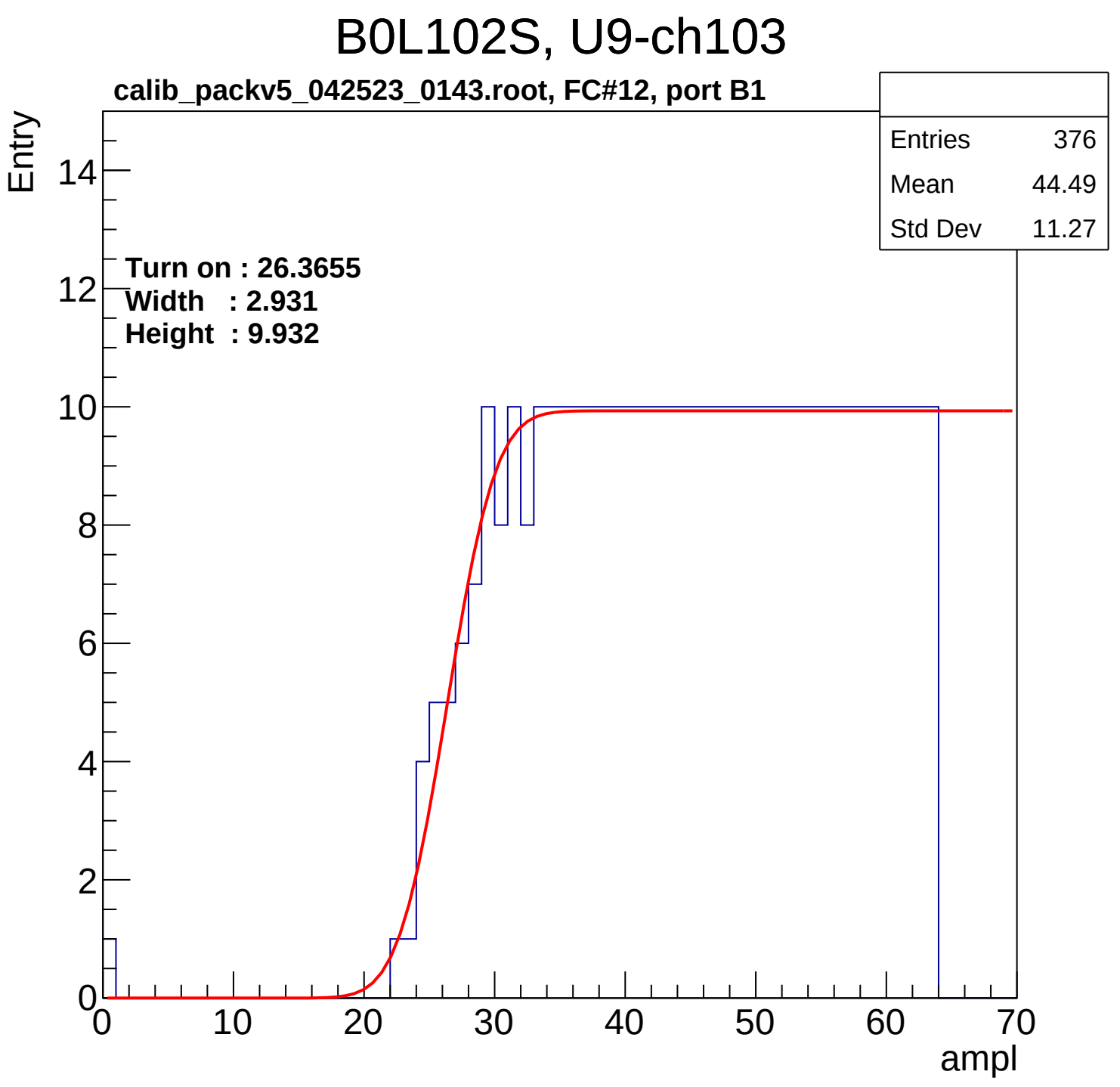

B0L102S, U9-ch98
calib_packv5_042523_0143.root, FC#12, port B1
Entries 378
Mean 44.18
Std Dev 11.9
Turn on : 27.3683
Width : 2.884
Height : 10.020
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

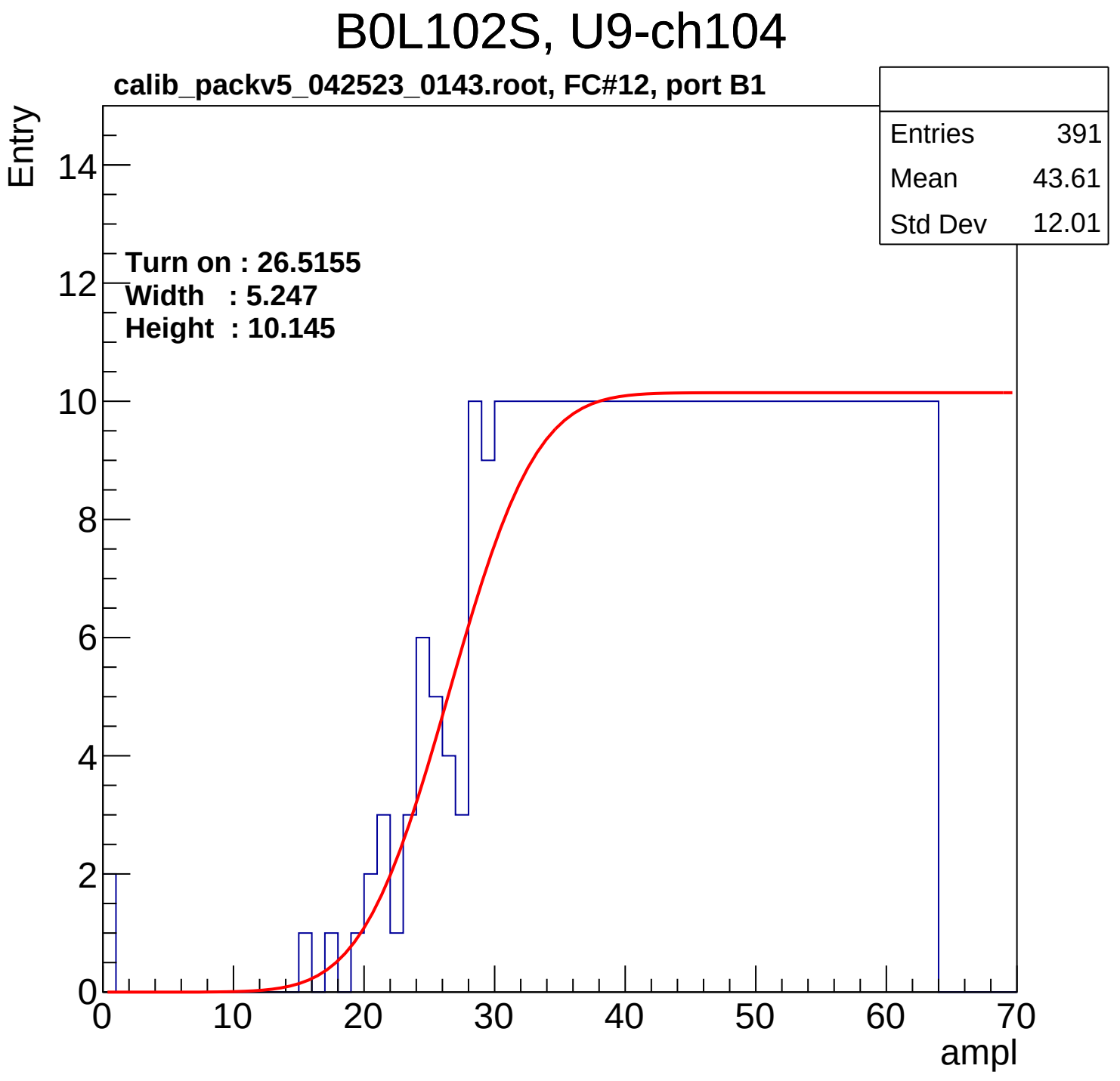

B0L102S, U9-ch99
calib_packv5_042523_0143.root, FC#12, port B1
Entries 391
Mean 43.63
Std Dev 12
Turn on : 26.0299
Width : 3.558
Height : 10.048
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

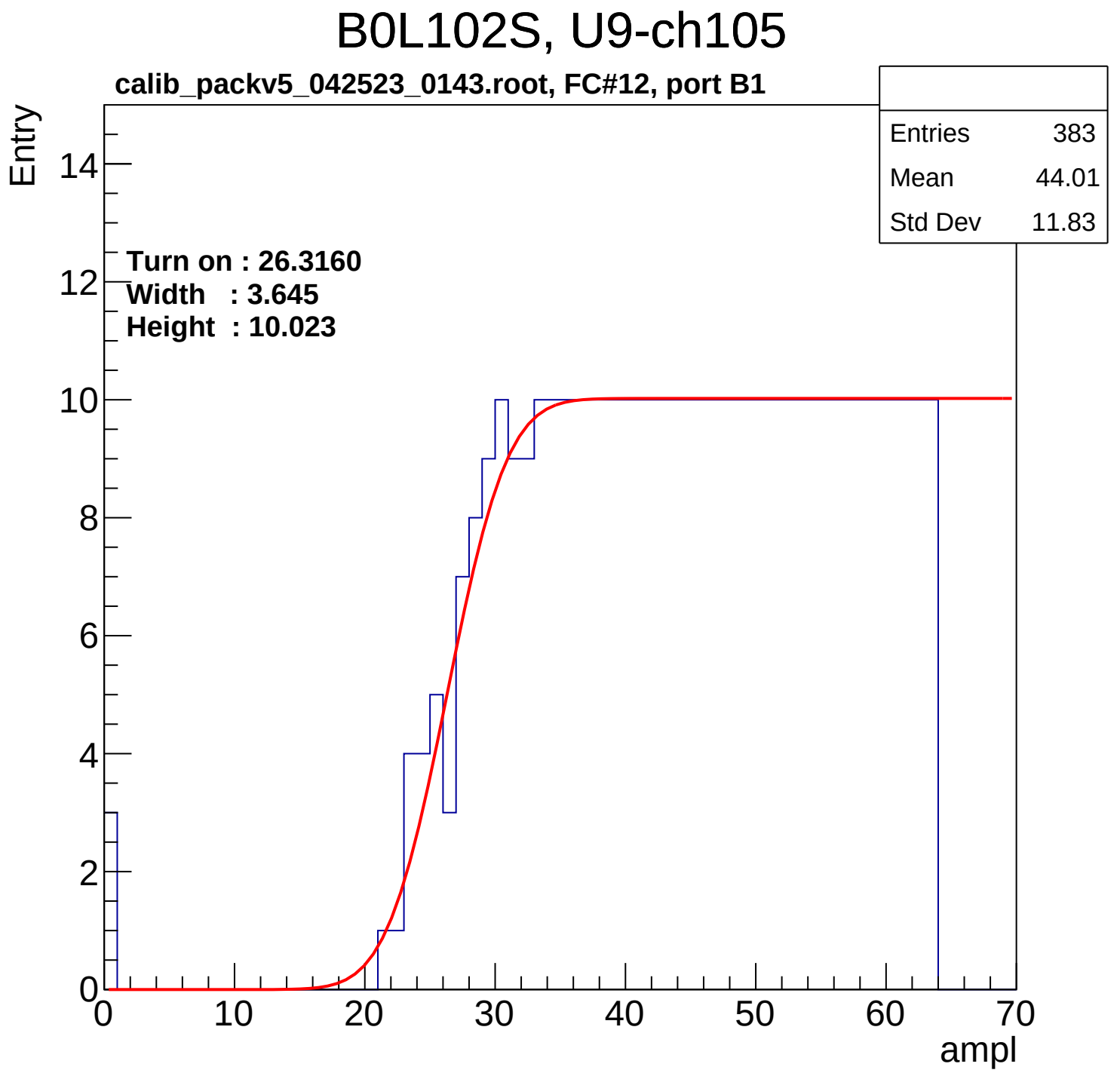

B0L102S, U9-ch100
calib_packv5_042523_0143.root, FC#12, port B1
Entries 381
Mean 44.19
Std Dev 11.5
Turn on : 26.3540
Width : 3.795
Height : 10.009
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

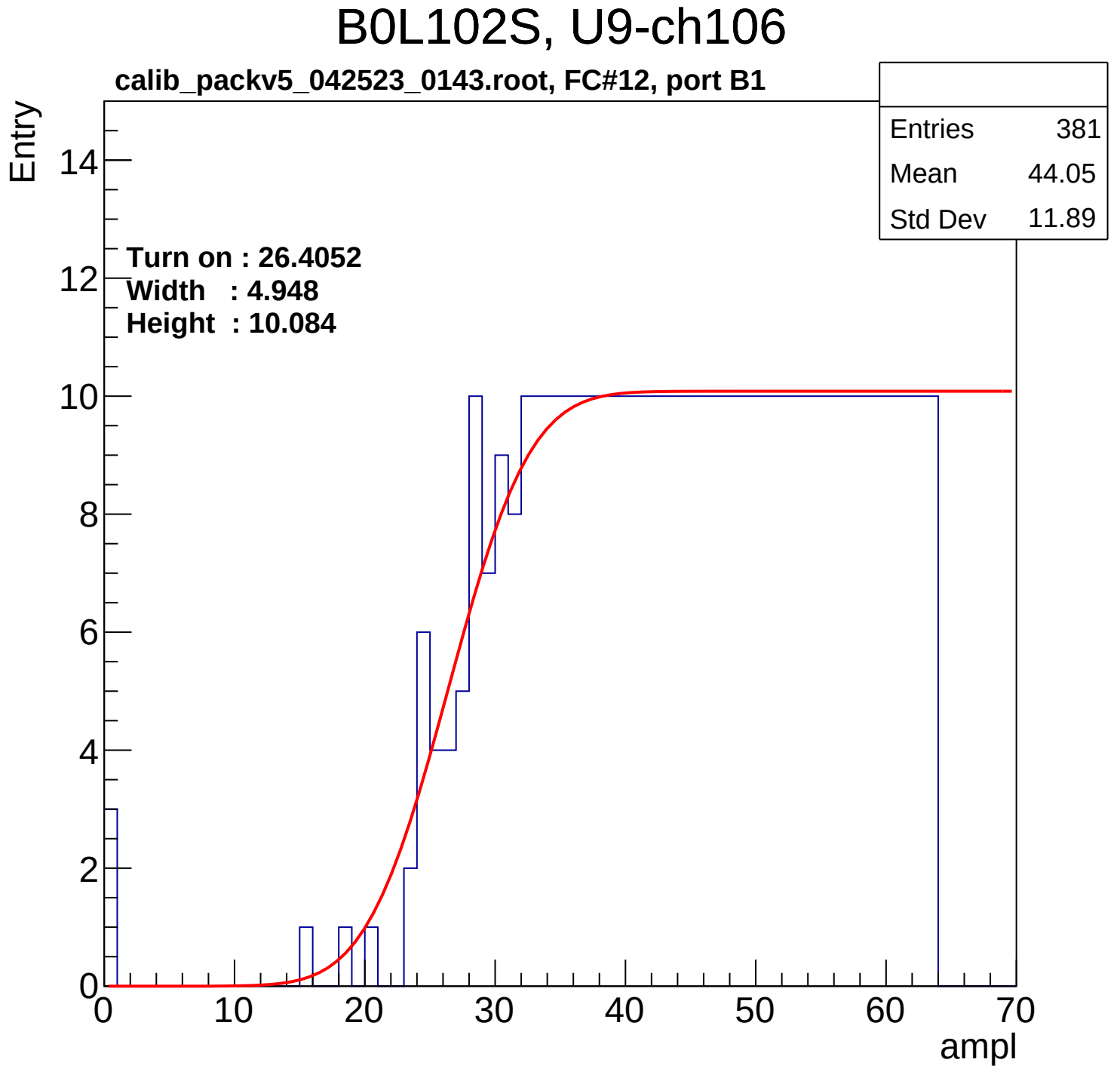

B0L102S, U9-ch101
calib_packv5_042523_0143.root, FC#12, port B1
Entries 370
Mean 44.68
Std Dev 11.39
Turn on : 28.1578
Width : 3.959
Height : 10.108
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

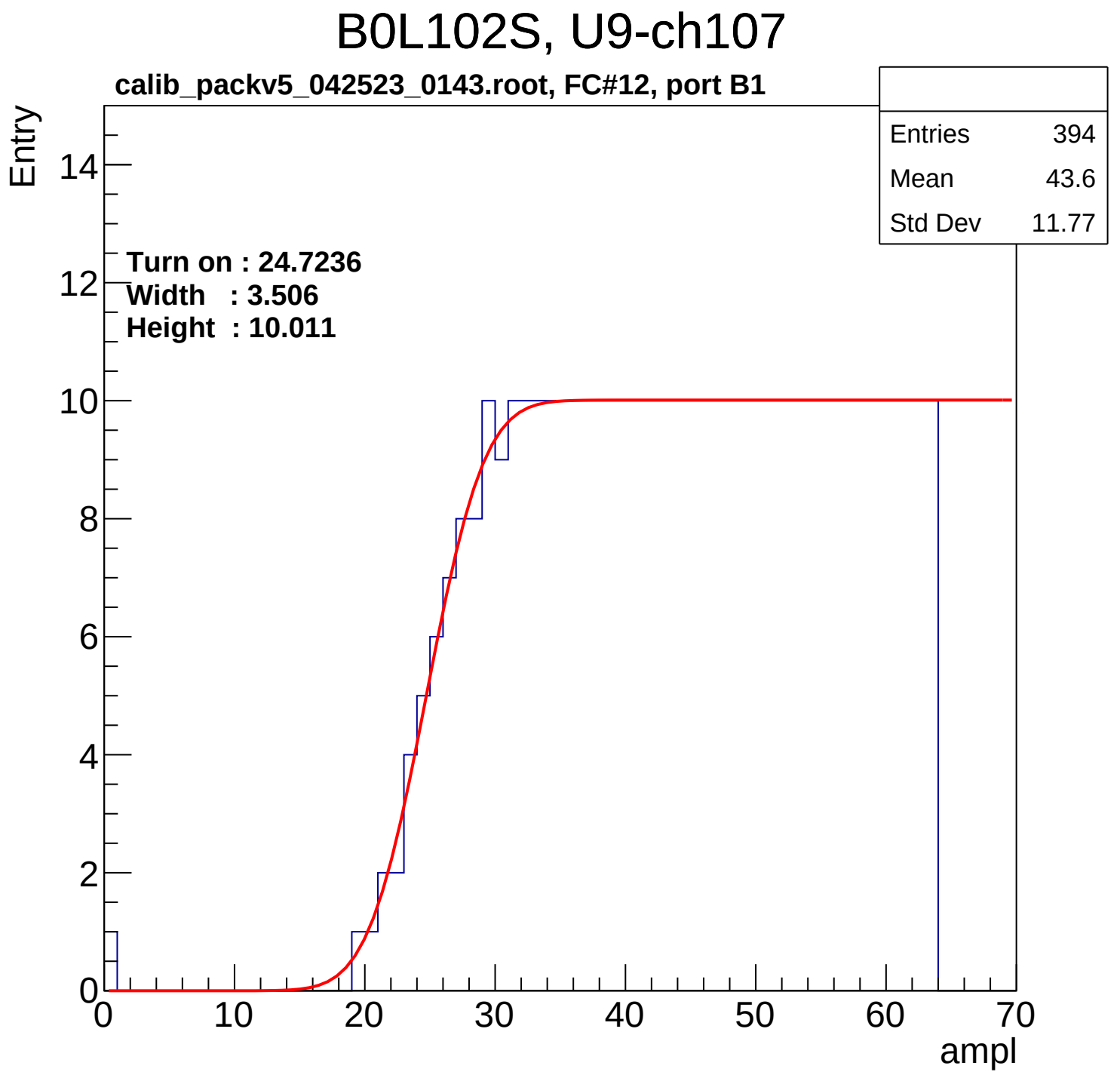

B0L102S, U9-ch102
calib_packv5_042523_0143.root, FC#12, port B1
Entries 406
Mean 43
Std Dev 12.1
Turn on : 24.0592
Width : 3.813
Height : 10.034
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

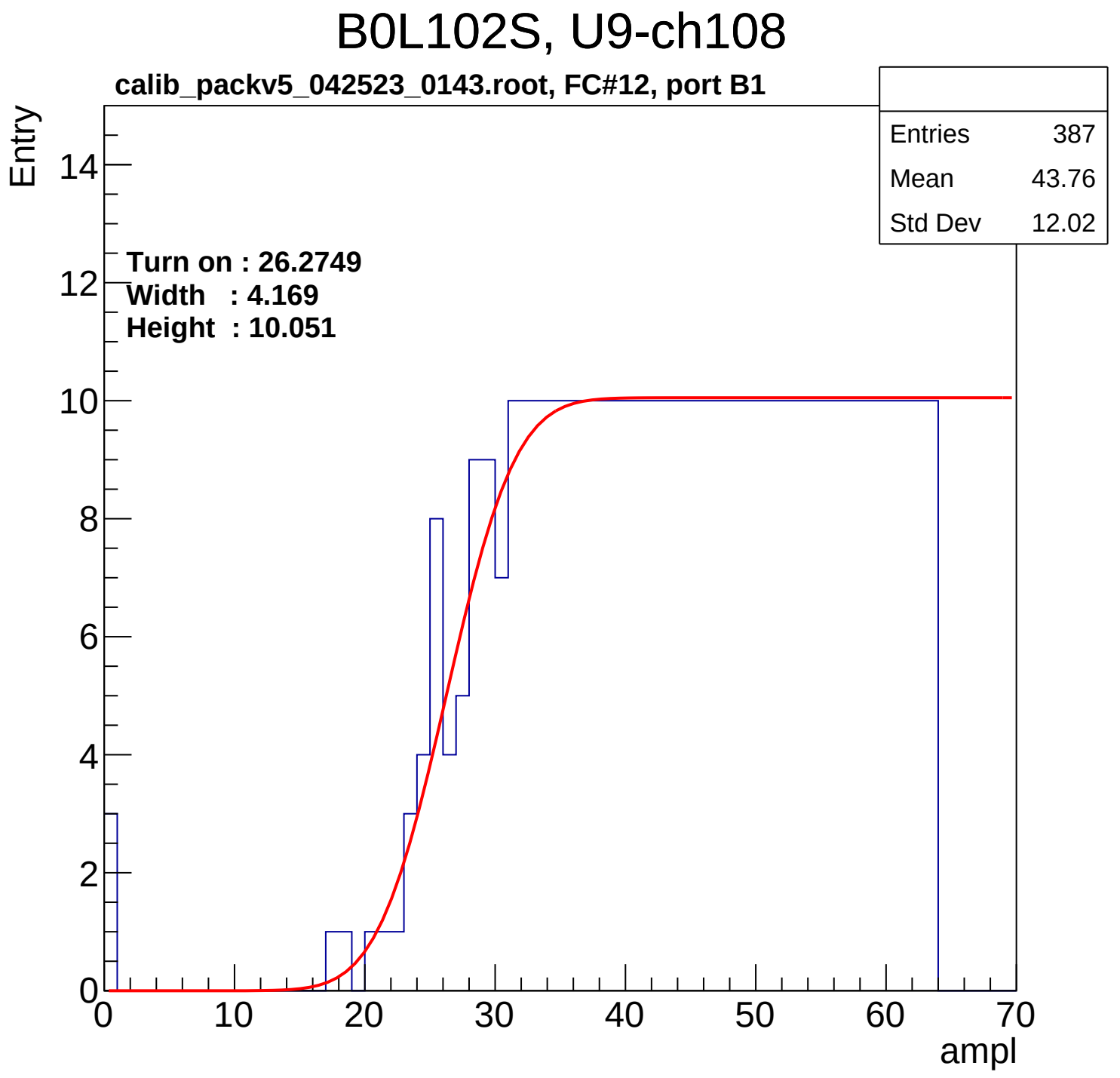

B0L102S, U9-ch103
calib_packv5_042523_0143.root, FC#12, port B1
Entries 376
Mean 44.49
Std Dev 11.27
Turn on : 26.3655
Width : 2.931
Height : 9.932
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

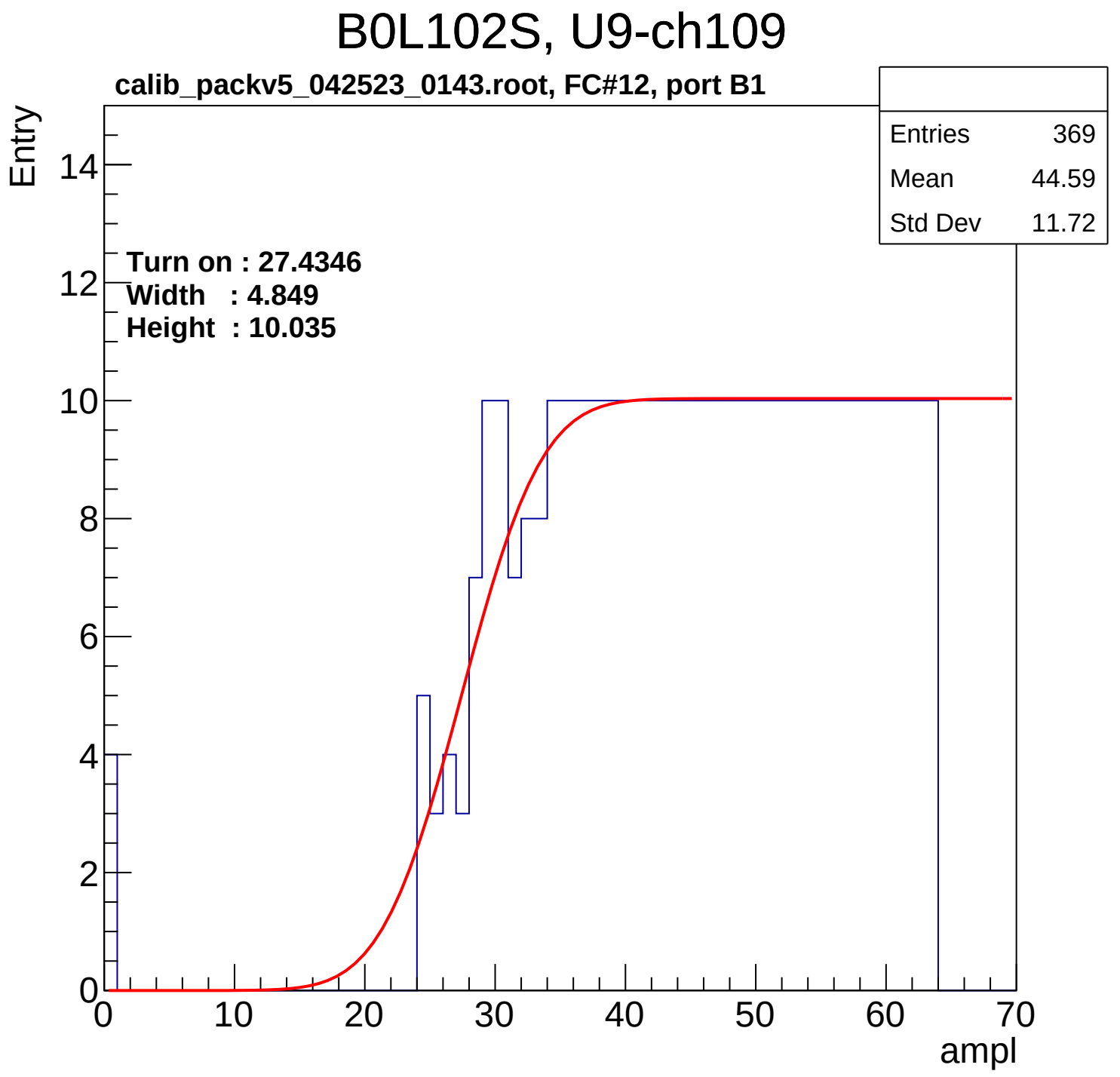

B0L102S, U9-ch104
calib_packv5_042523_0143.root, FC#12, port B1
Entries 391
Mean 43.61
Std Dev 12.01
Turn on : 26.5155
Width : 5.247
Height : 10.145
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

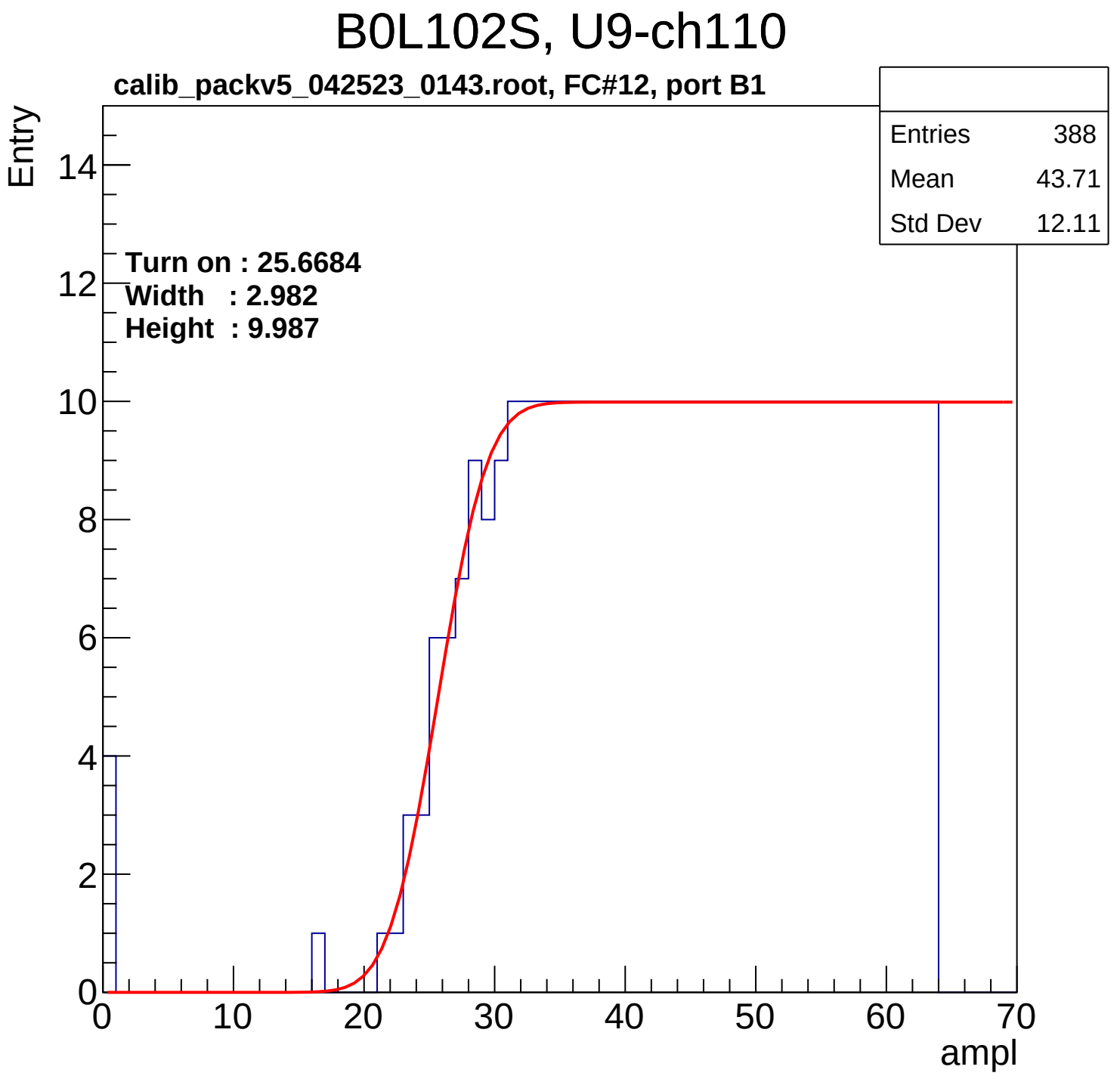

B0L102S, U9-ch105
calib_packv5_042523_0143.root, FC#12, port B1
Entries 383
Mean 44.01
Std Dev 11.83
Turn on : 26.3160
Width : 3.645
Height : 10.023
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

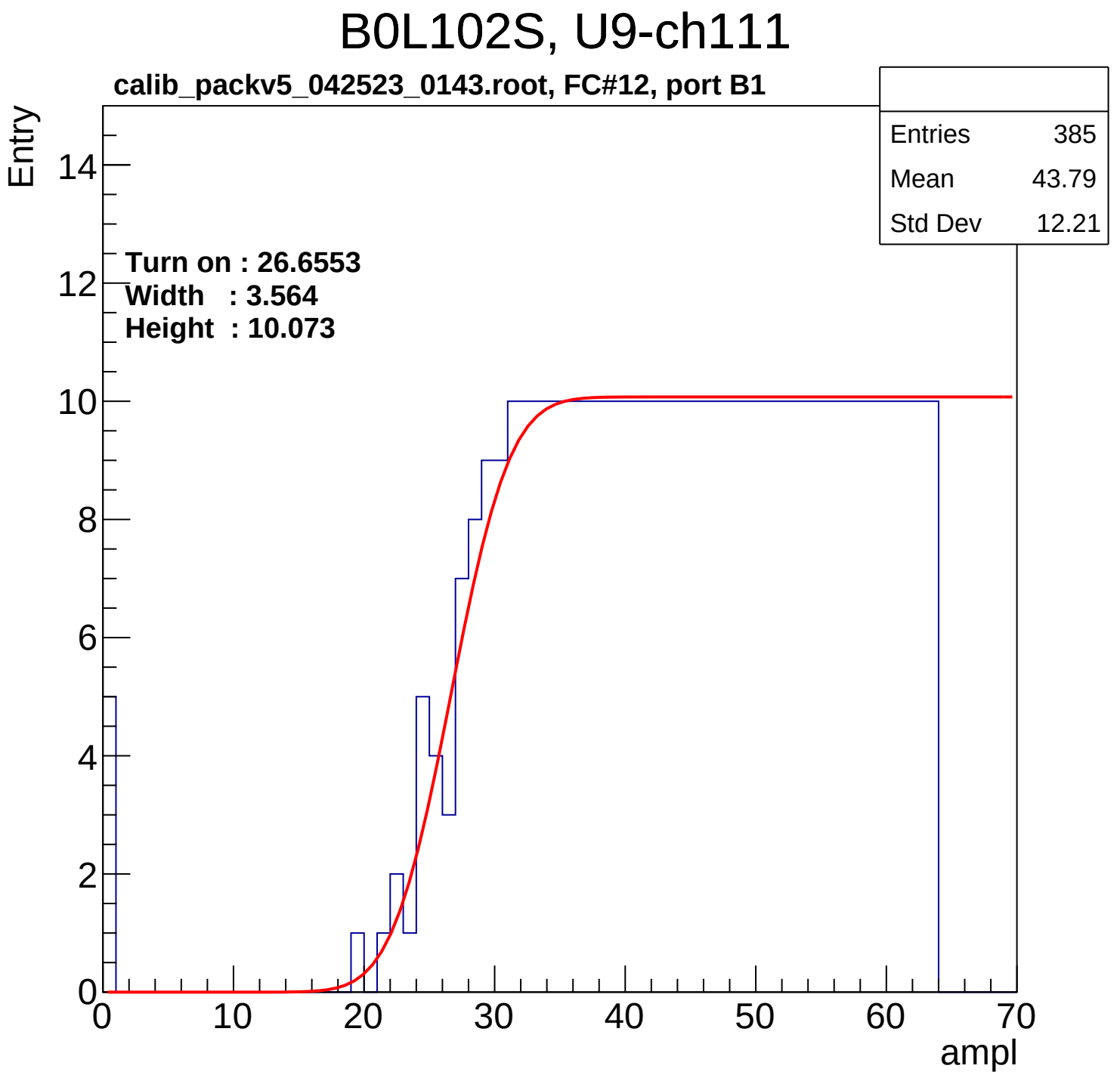

B0L102S, U9-ch106
calib_packv5_042523_0143.root, FC#12, port B1
Entries 381
Mean 44.05
Std Dev 11.89
Turn on : 26.4052
Width : 4.948
Height : 10.084
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

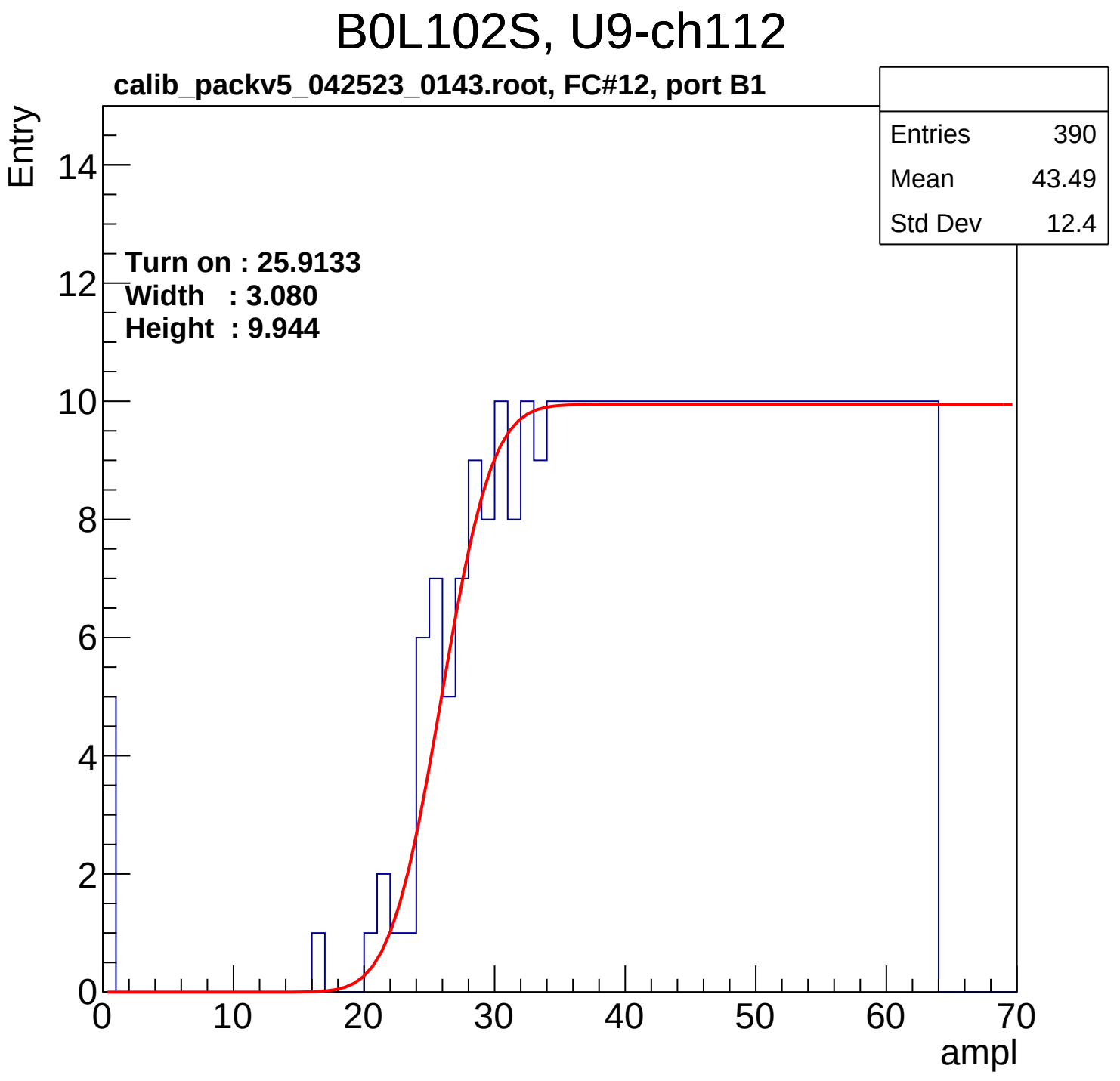

B0L102S, U9-ch107
calib_packv5_042523_0143.root, FC#12, port B1
Entries 394
Mean 43.6
Std Dev 11.77
Turn on : 24.7236
Width : 3.506
Height : 10.011
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

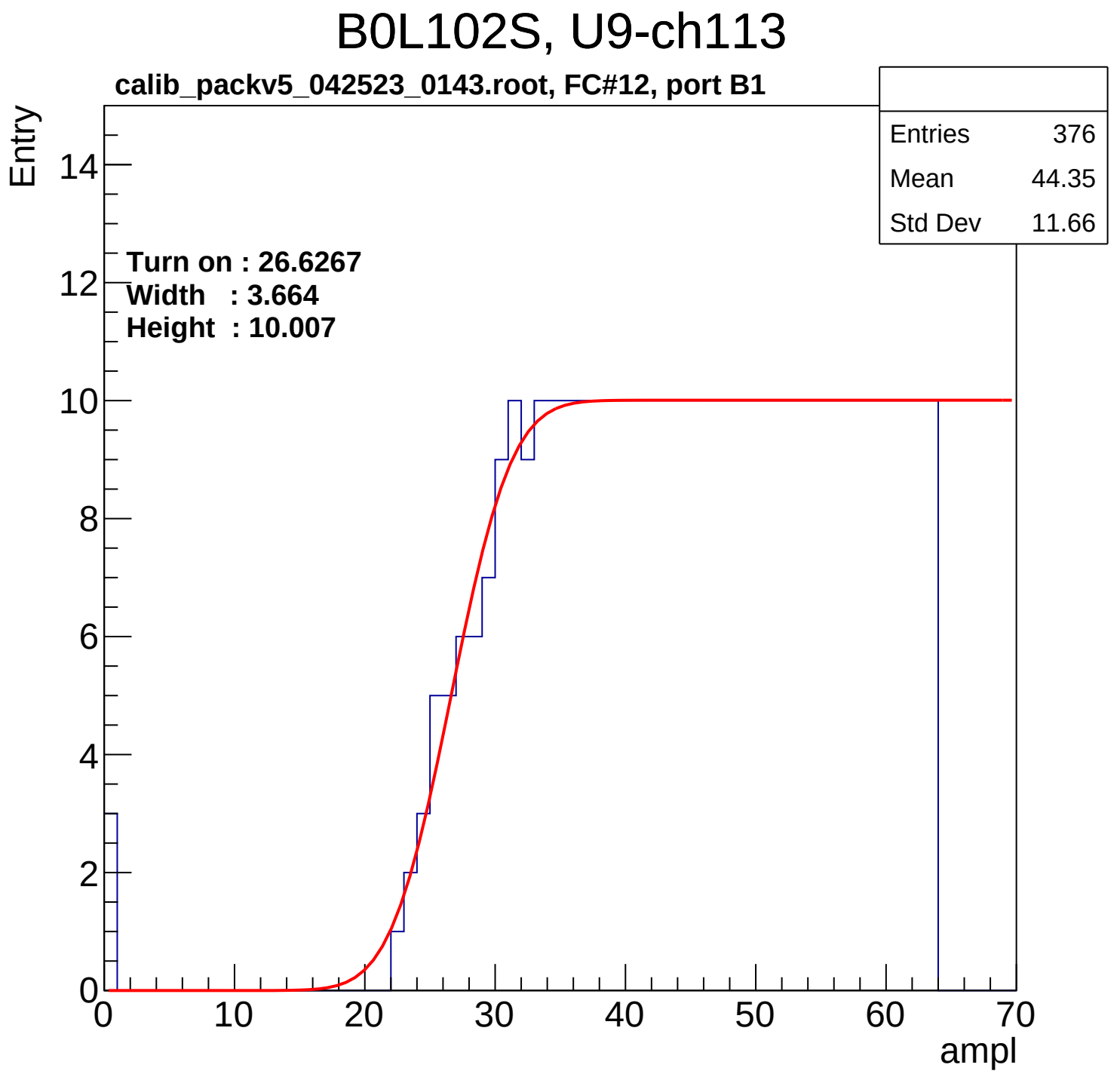

B0L102S, U9-ch108
calib_packv5_042523_0143.root, FC#12, port B1
Entries 387
Mean 43.76
Std Dev 12.02
Turn on : 26.2749
Width : 4.169
Height : 10.051
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

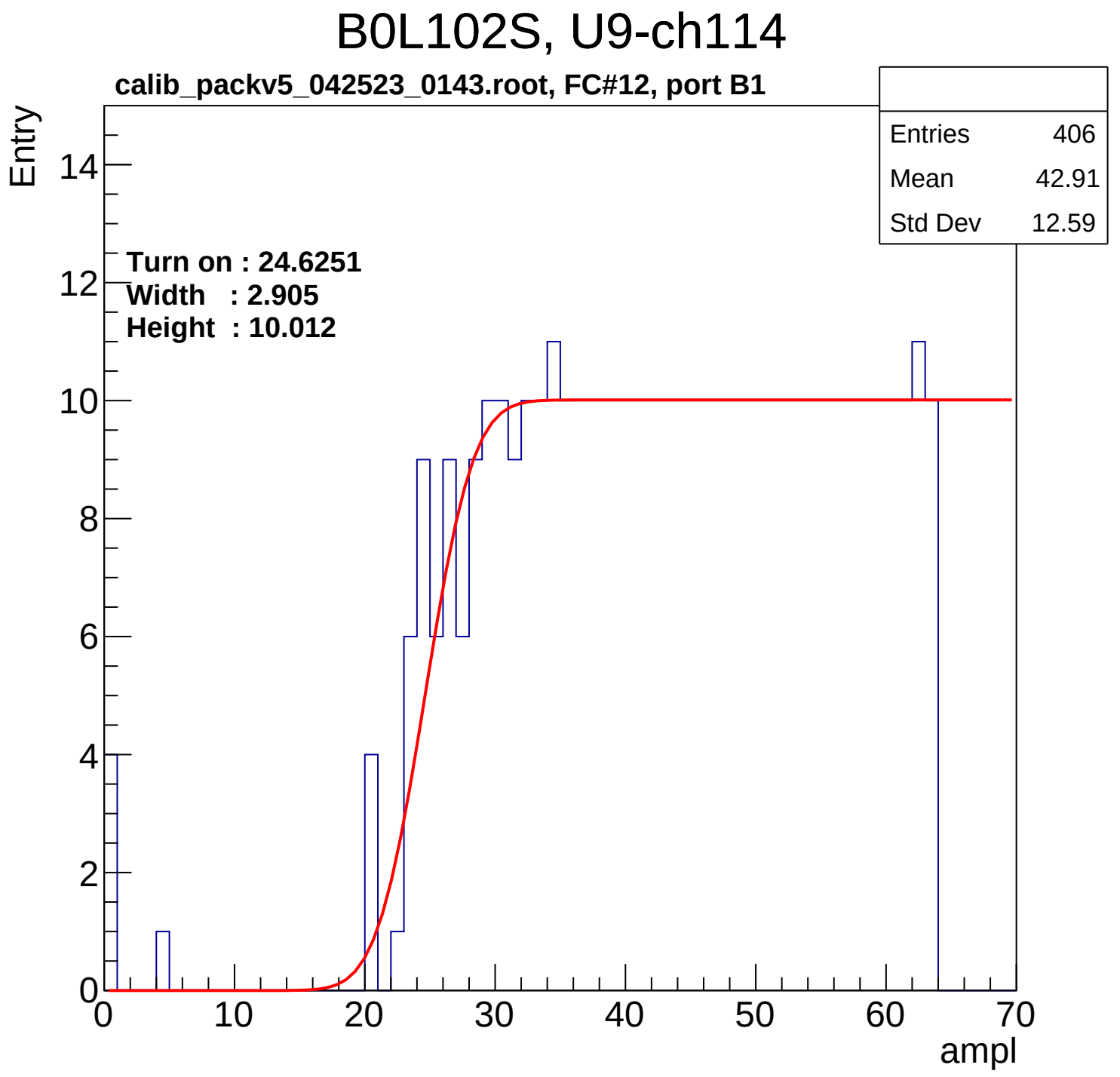

B0L102S, U9-ch109
calib_packv5_042523_0143.root, FC#12, port B1
Entries 369
Mean 44.59
Std Dev 11.72
Turn on : 27.4346
Width : 4.849
Height : 10.035
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

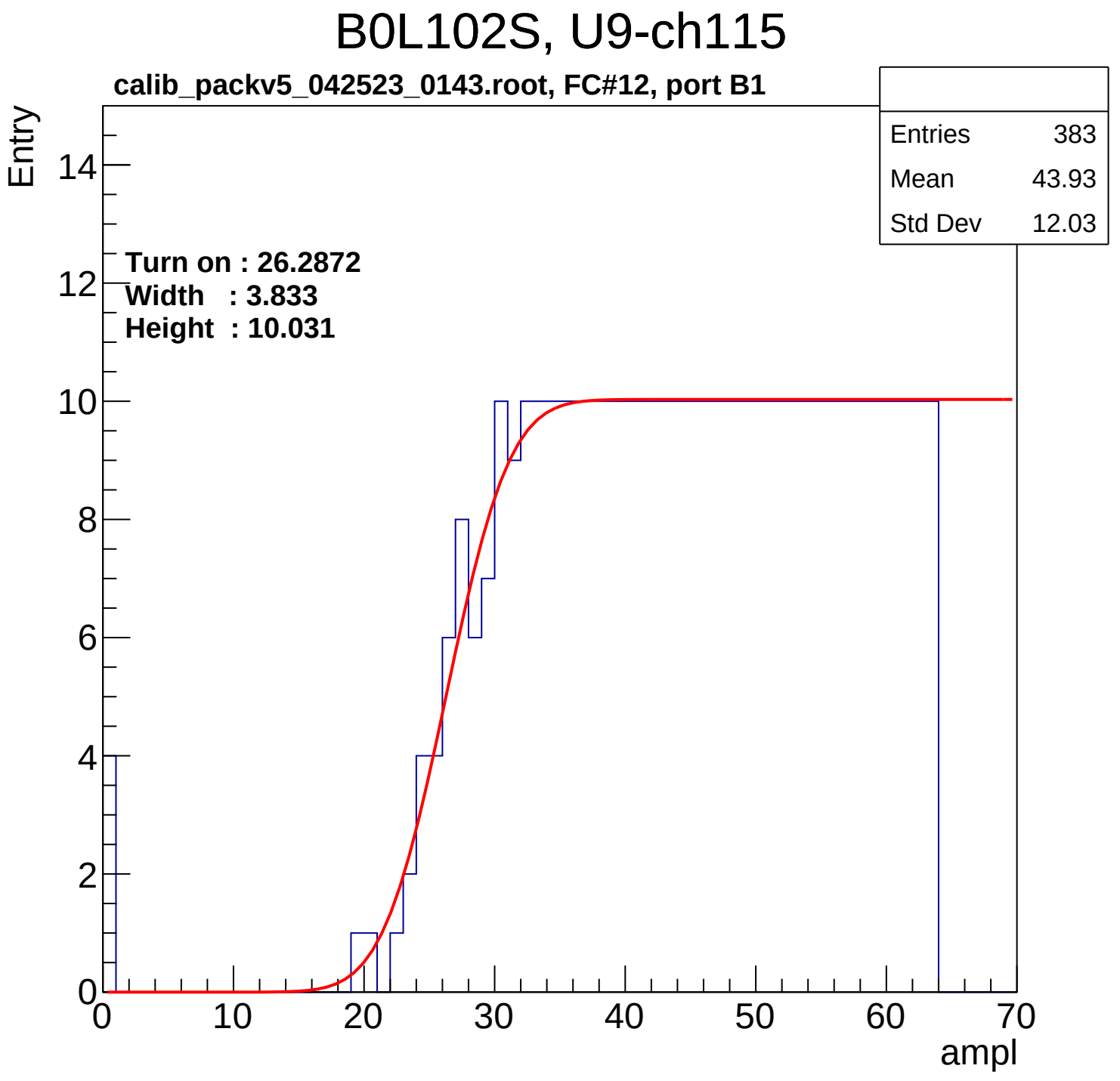

B0L102S, U9-ch110
calib_packv5_042523_0143.root, FC#12, port B1
Entries 388
Mean 43.71
Std Dev 12.11
Turn on : 25.6684
Width : 2.982
Height : 9.987
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

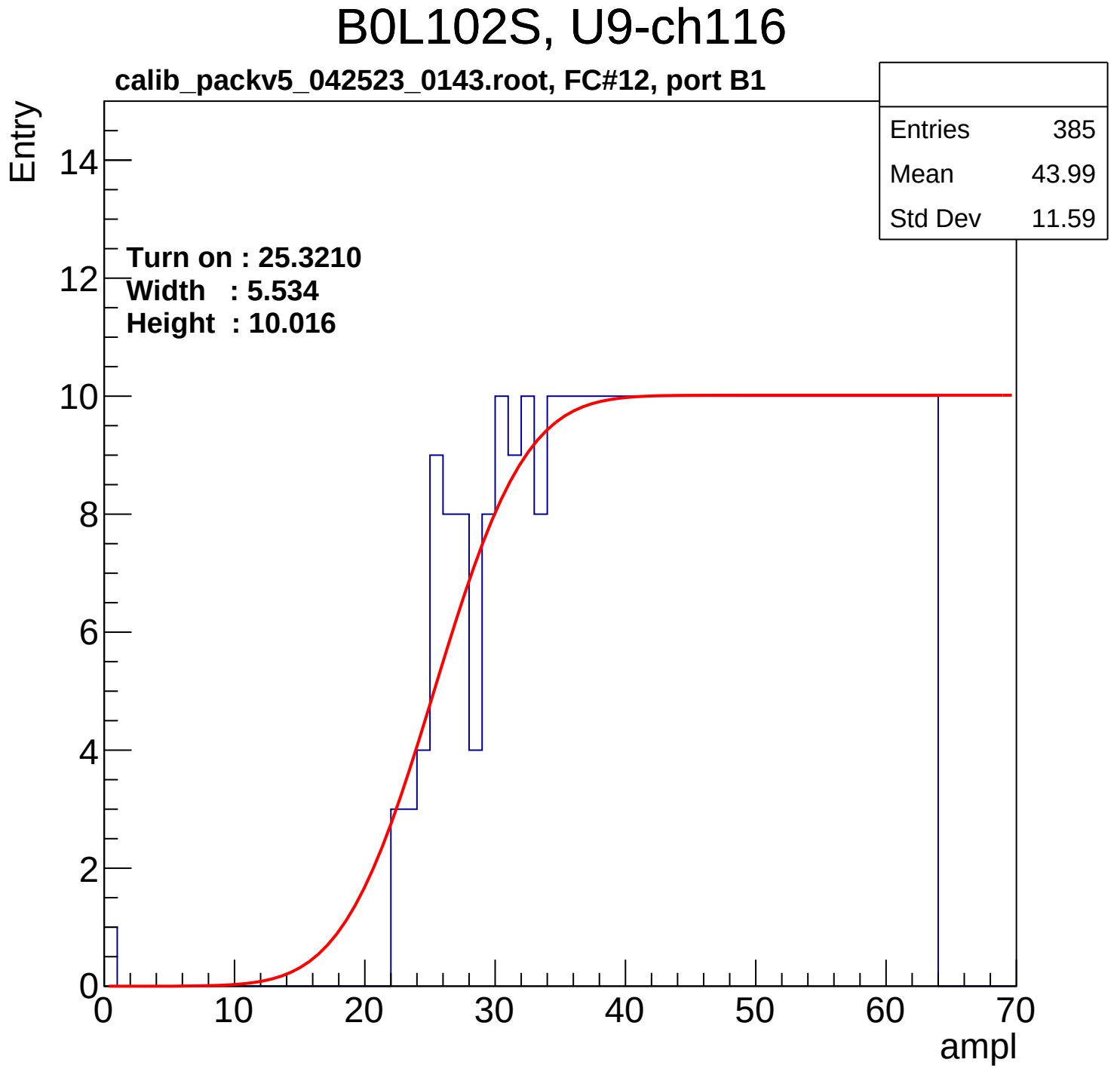

B0L102S, U9-ch111
calib_packv5_042523_0143.root, FC#12, port B1
Entries 385
Mean 43.79
Std Dev 12.21
Turn on : 26.6553
Width : 3.564
Height : 10.073
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

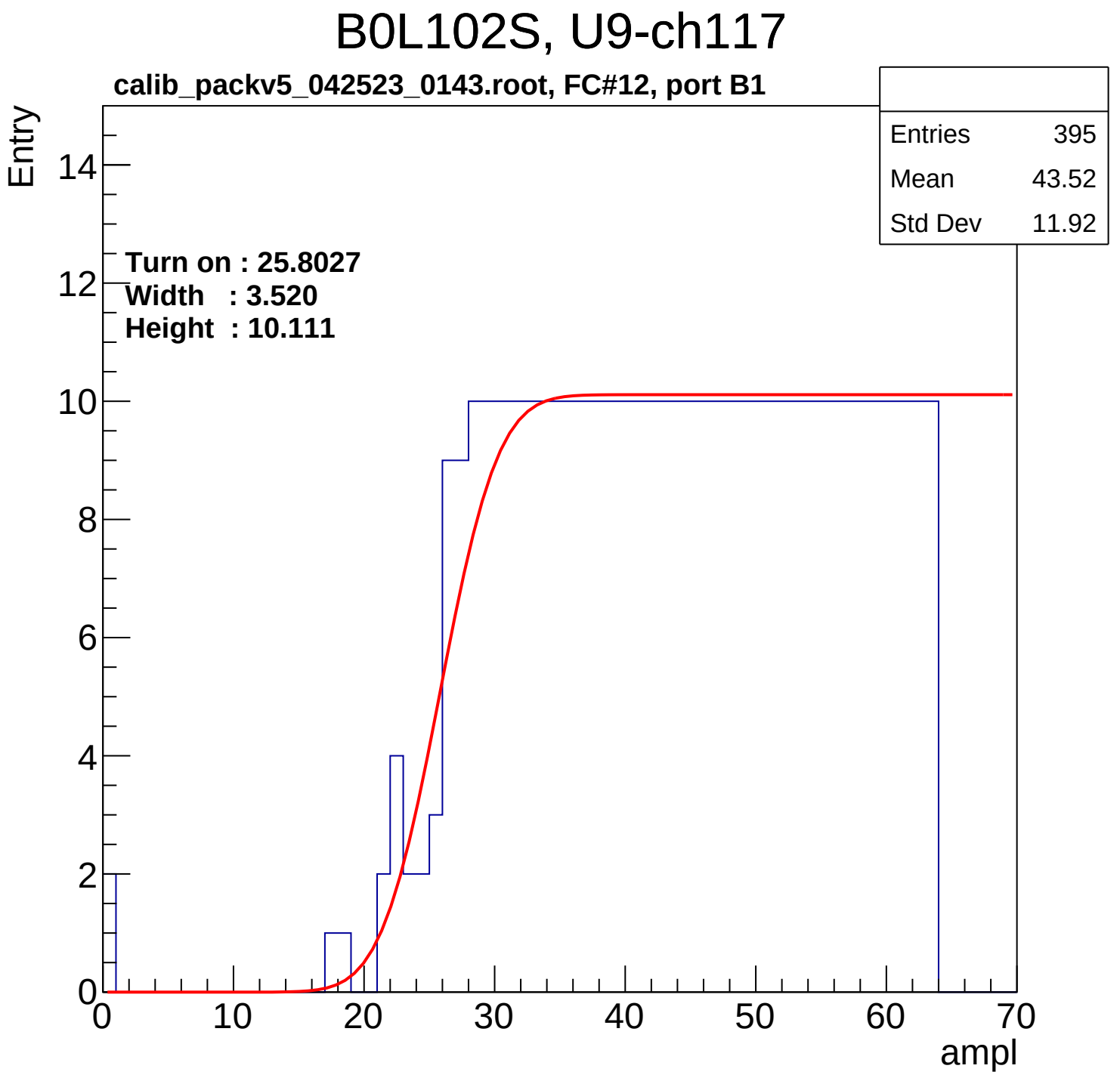

B0L102S, U9-ch112
calib_packv5_042523_0143.root, FC#12, port B1
Entries 390
Mean 43.49
Std Dev 12.4
Turn on : 25.9133
Width : 3.080
Height : 9.944
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

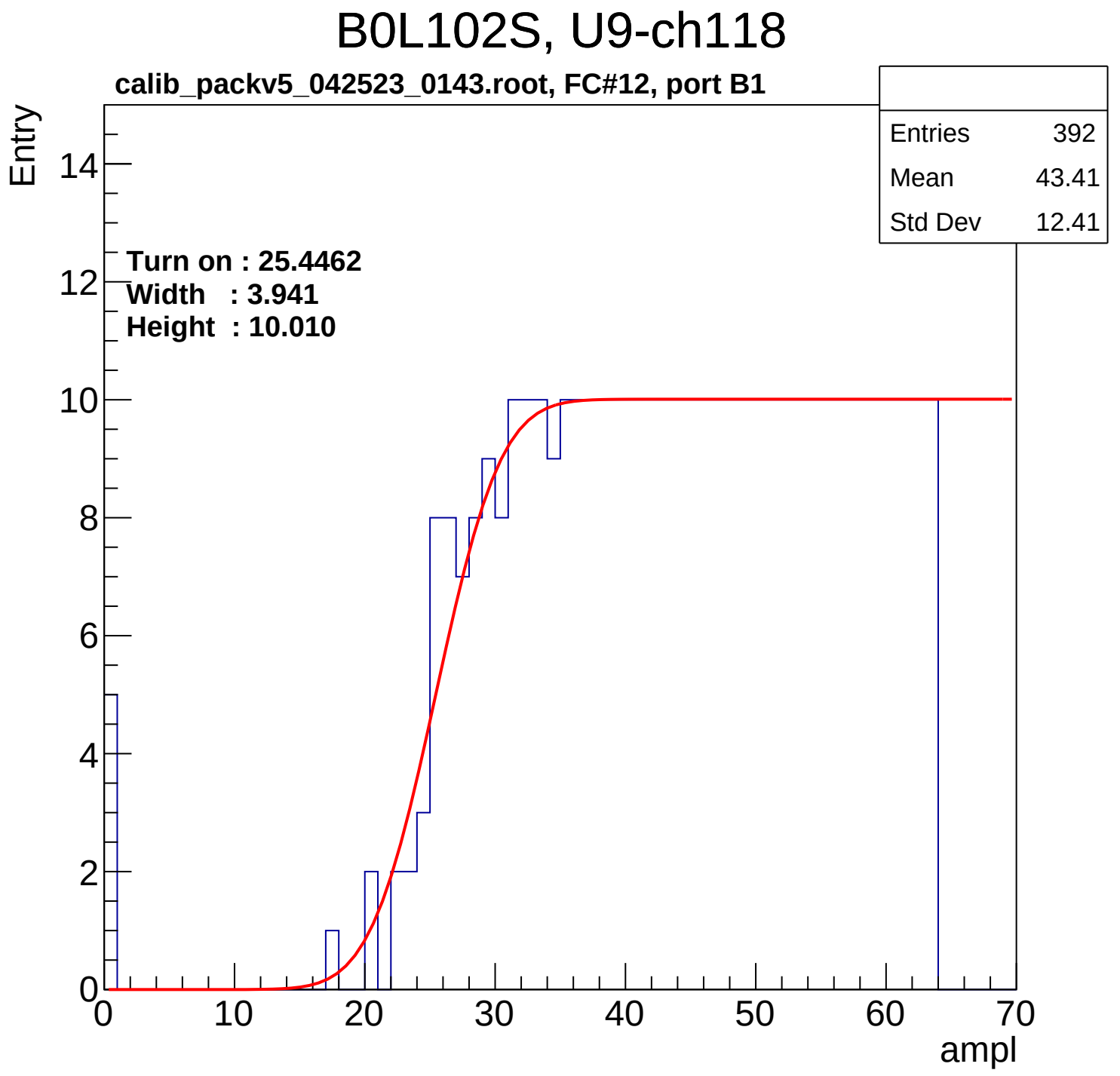

B0L102S, U9-ch113
calib_packv5_042523_0143.root, FC#12, port B1
Entries 376
Mean 44.35
Std Dev 11.66
Turn on : 26.6267
Width : 3.664
Height : 10.007
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

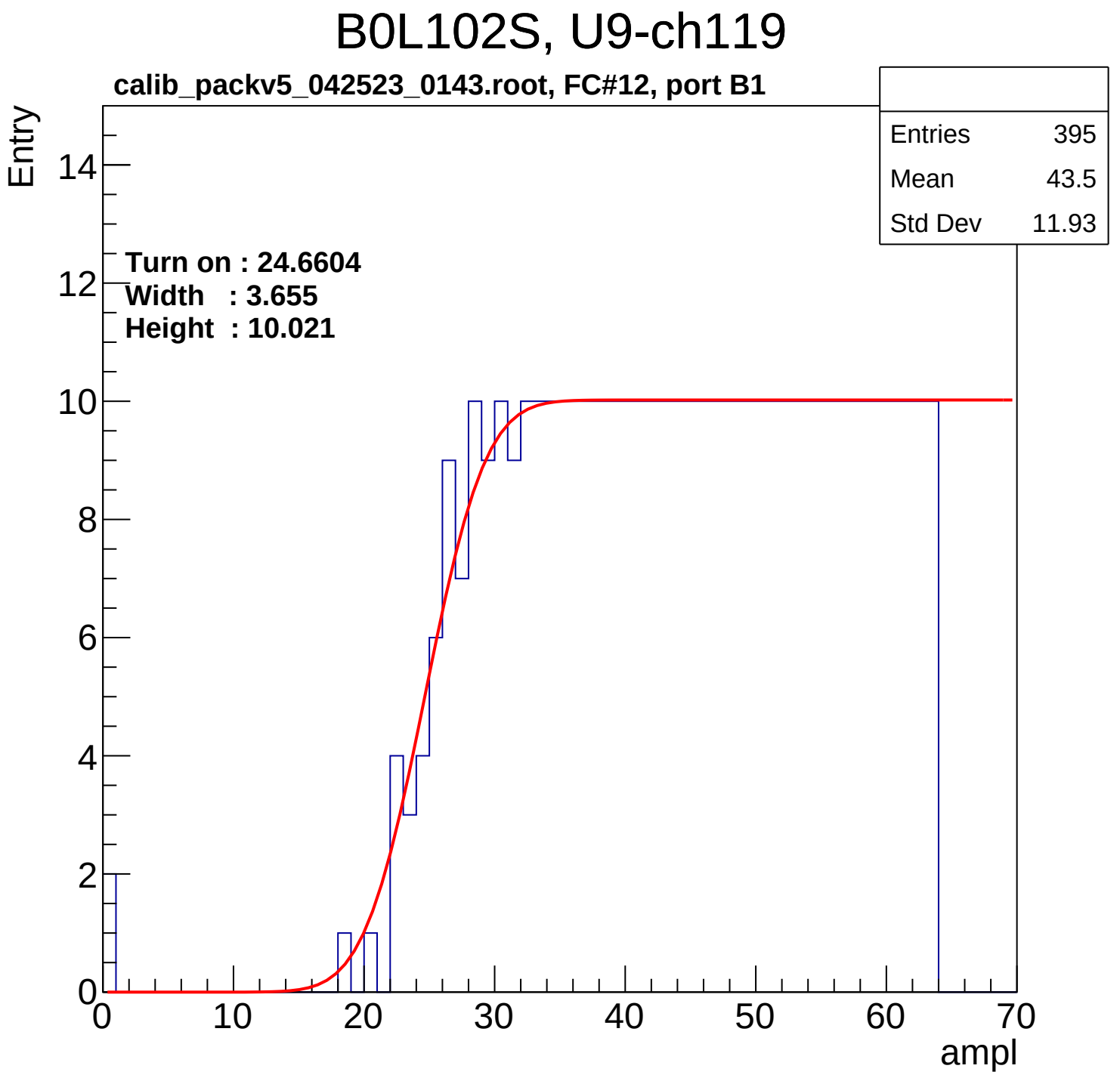

B0L102S, U9-ch114
calib_packv5_042523_0143.root, FC#12, port B1
Entries 406
Mean 42.91
Std Dev 12.59
Turn on : 24.6251
Width : 2.905
Height : 10.012
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

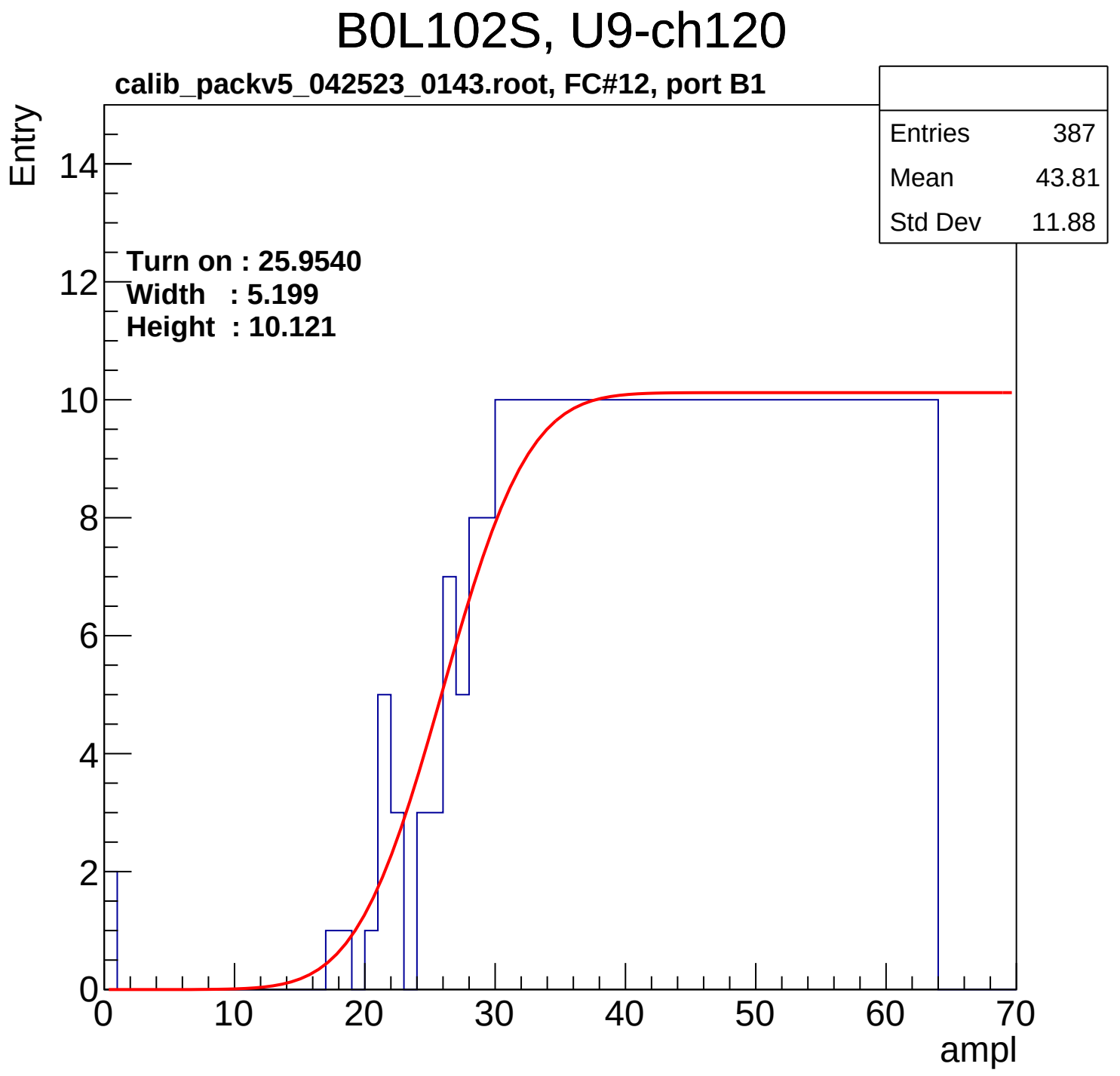

B0L102S, U9-ch115
calib_packv5_042523_0143.root, FC#12, port B1
Entries 383
Mean 43.93
Std Dev 12.03
Turn on : 26.2872
Width : 3.833
Height : 10.031
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

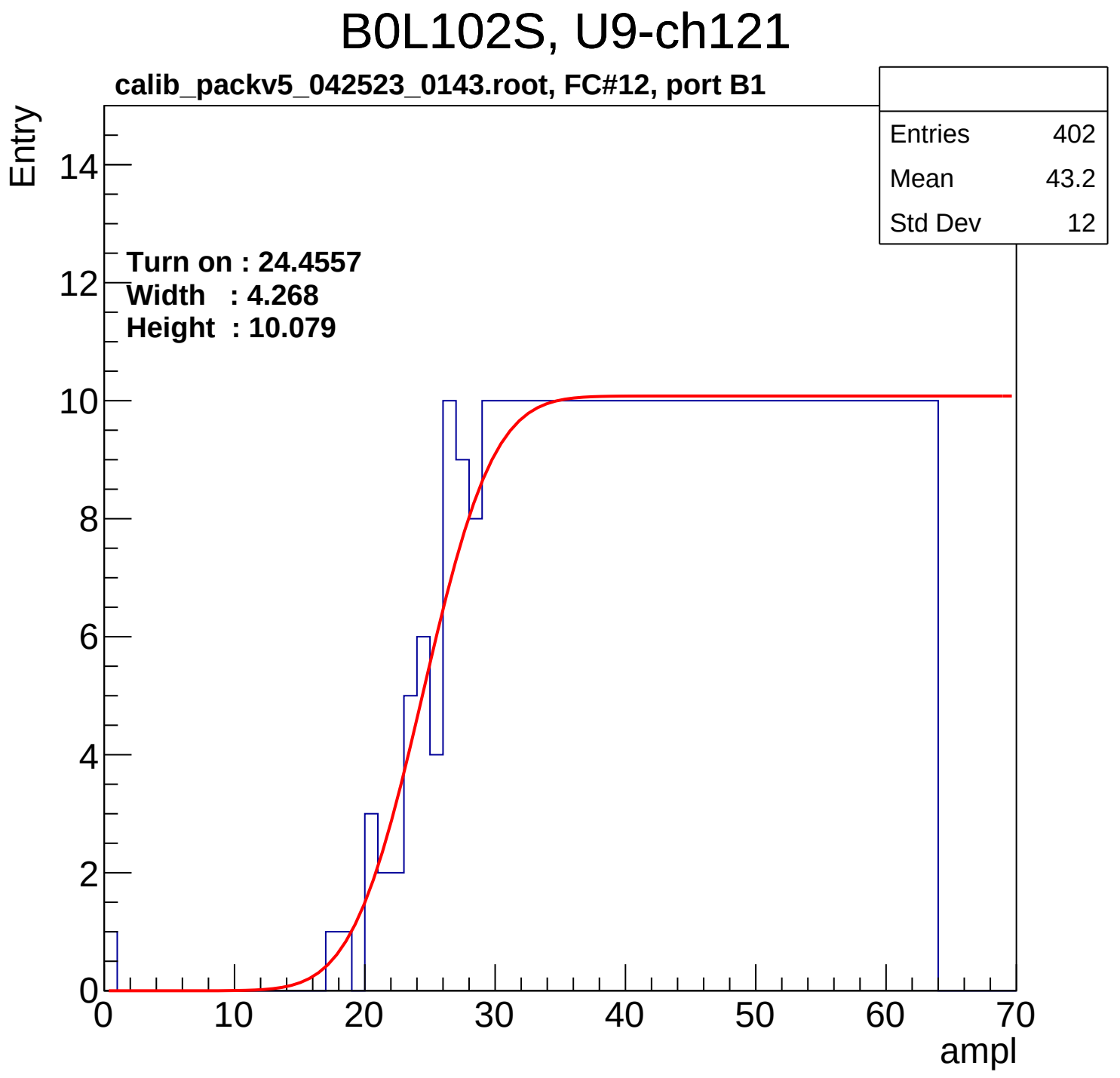

B0L102S, U9-ch116
calib_packv5_042523_0143.root, FC#12, port B1
Entries 385
Mean 43.99
Std Dev 11.59
Turn on : 25.3210
Width : 5.534
Height : 10.016
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

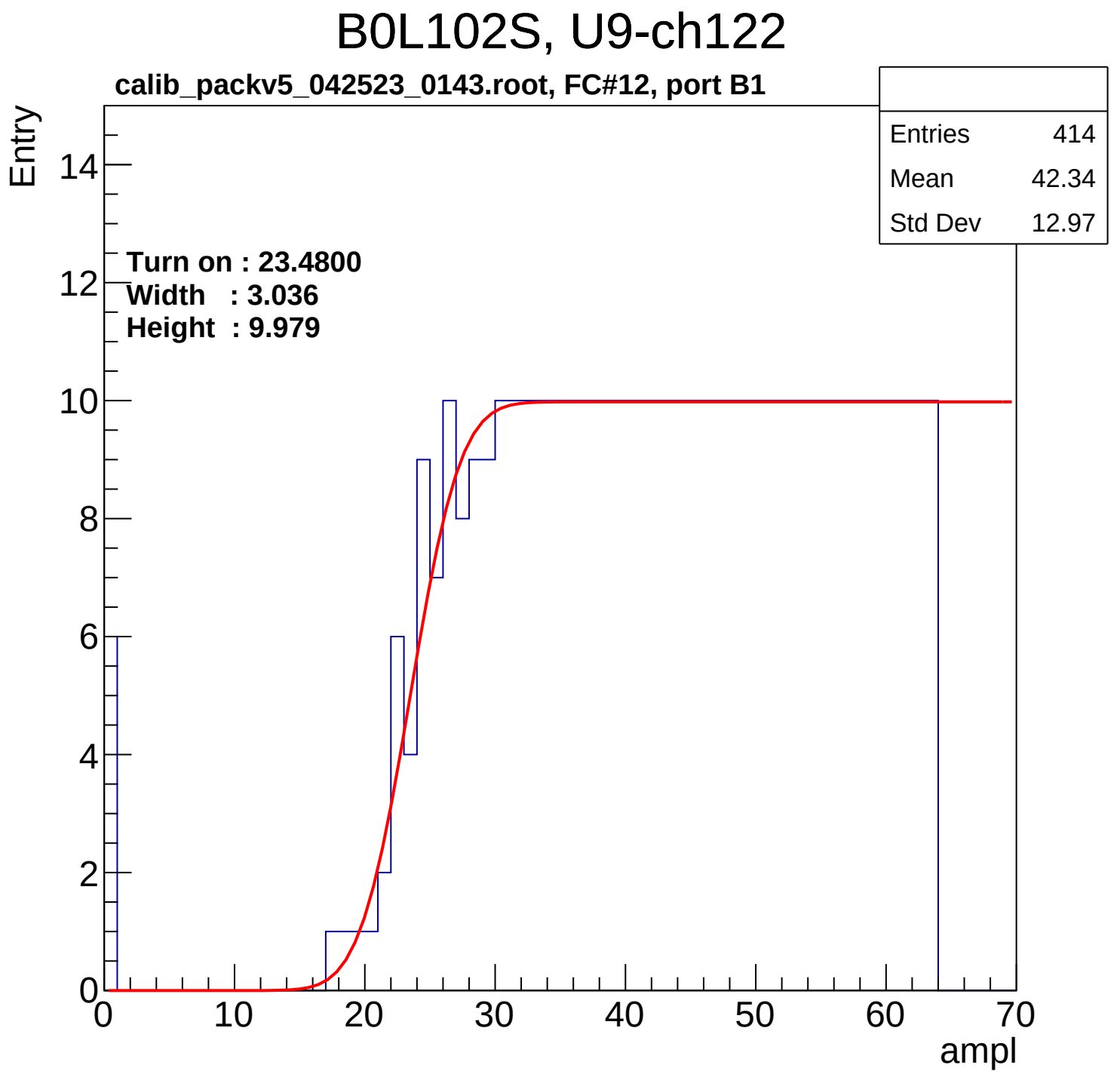

B0L102S, U9-ch117
calib_packv5_042523_0143.root, FC#12, port B1
Entries 395
Mean 43.52
Std Dev 11.92
Turn on : 25.8027
Width : 3.520
Height : 10.111
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

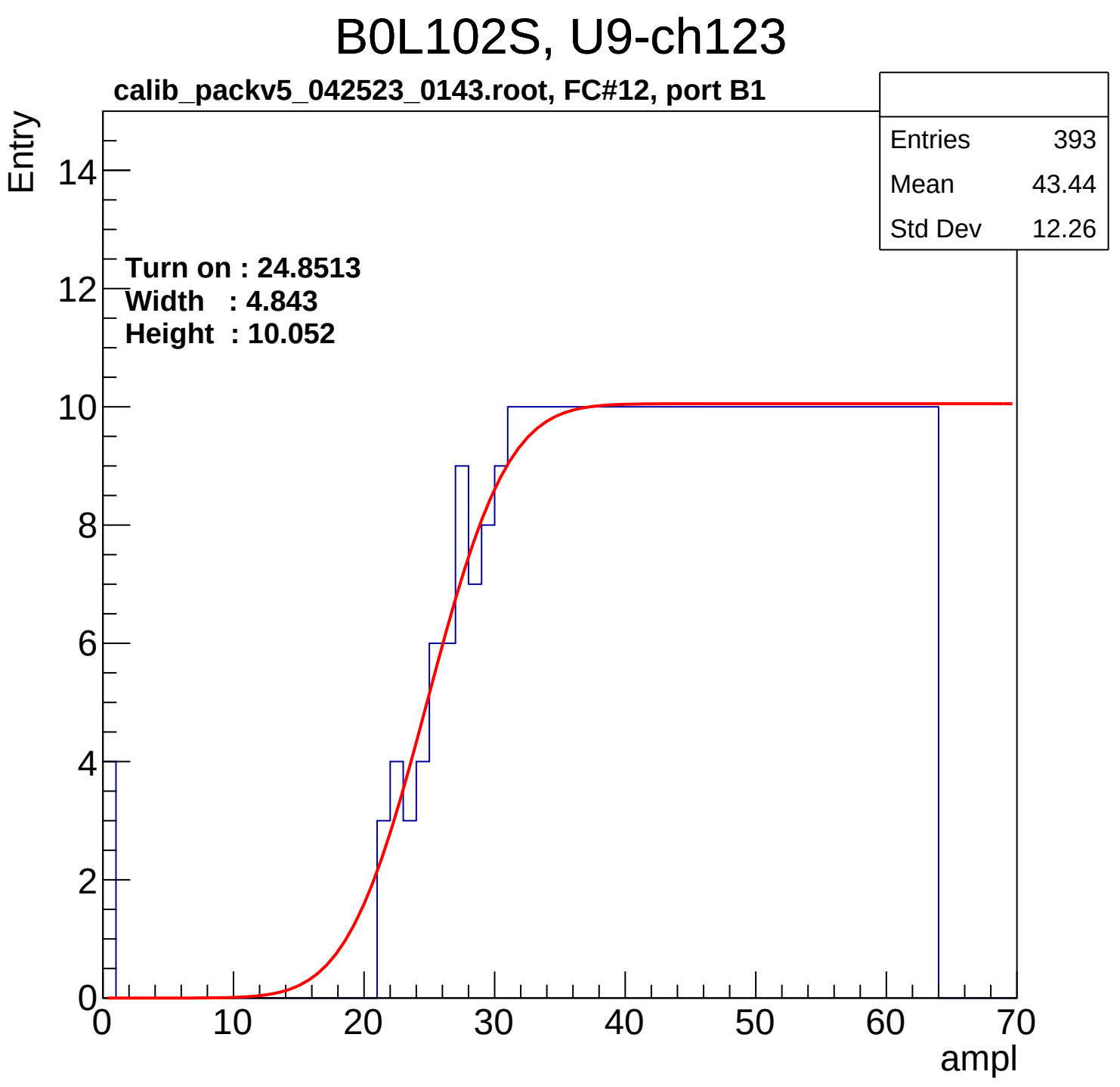

B0L102S, U9-ch118
calib_packv5_042523_0143.root, FC#12, port B1
Entries 392
Mean 43.41
Std Dev 12.41
Turn on : 25.4462
Width : 3.941
Height : 10.010
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

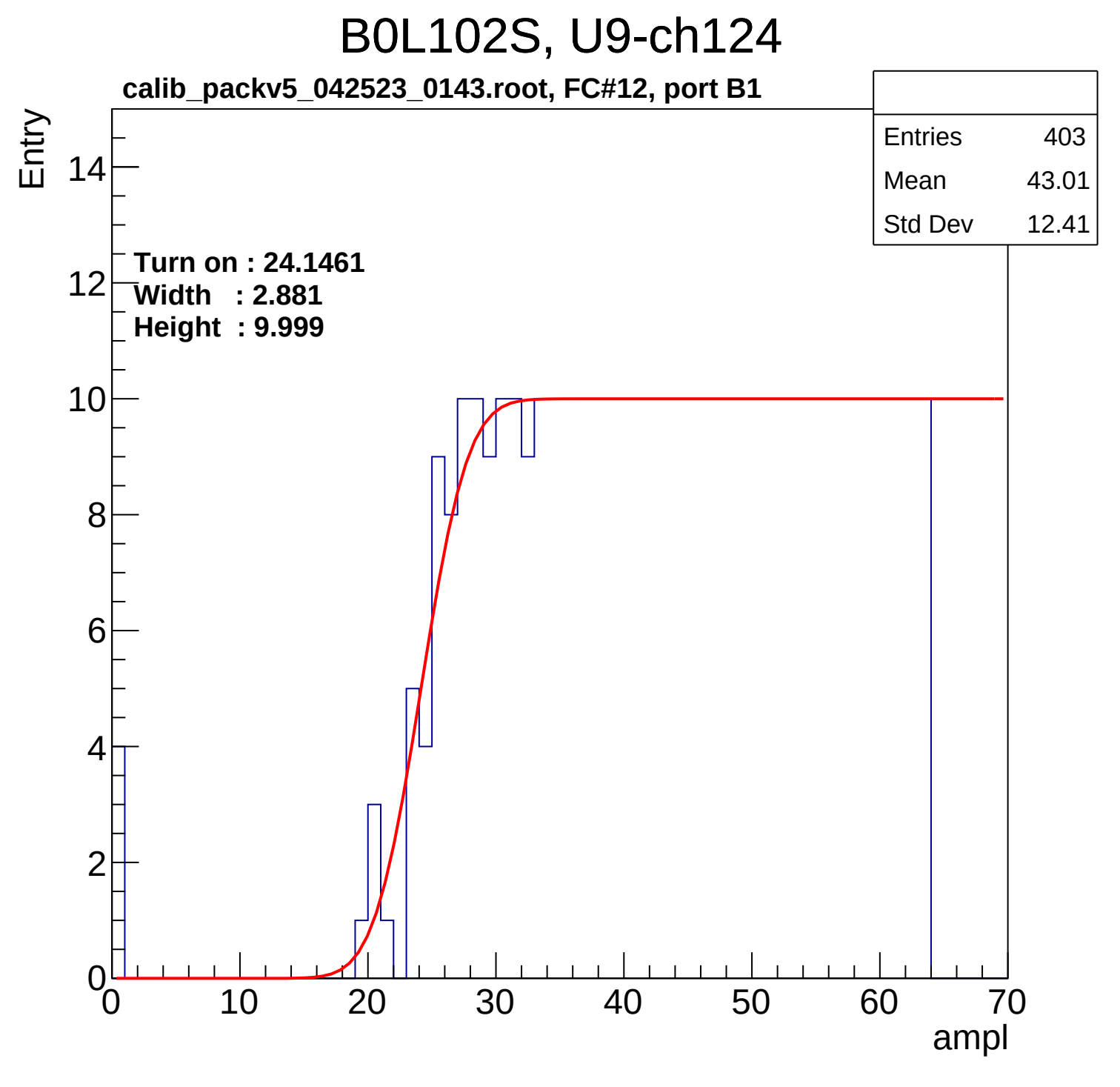

B0L102S, U9-ch119
calib_packv5_042523_0143.root, FC#12, port B1
Entries 395
Mean 43.5
Std Dev 11.93
Turn on : 24.6604
Width : 3.655
Height : 10.021
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

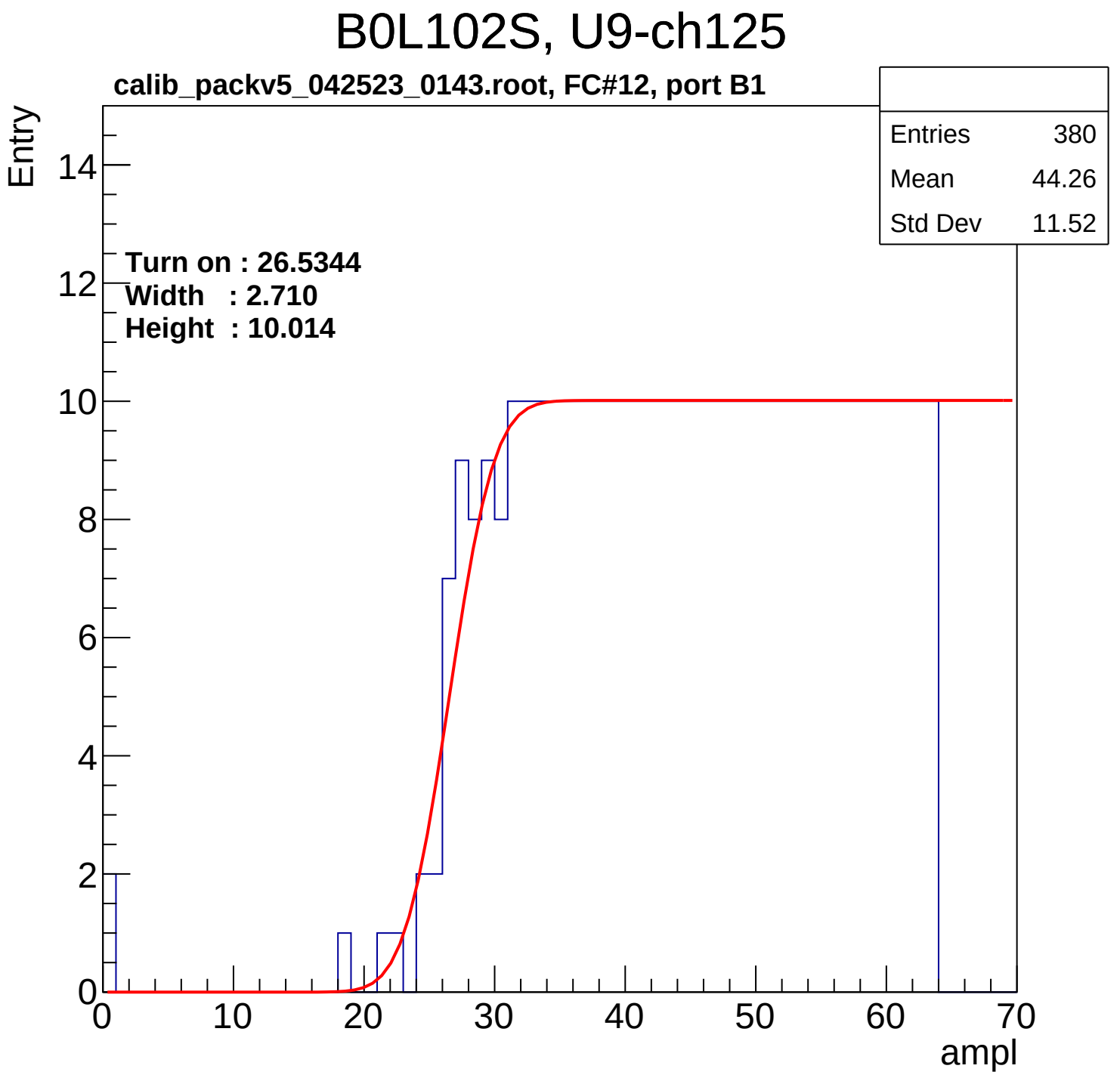

B0L102S, U9-ch120
calib_packv5_042523_0143.root, FC#12, port B1
Entries 387
Mean 43.81
Std Dev 11.88
Turn on : 25.9540
Width : 5.199
Height : 10.121
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

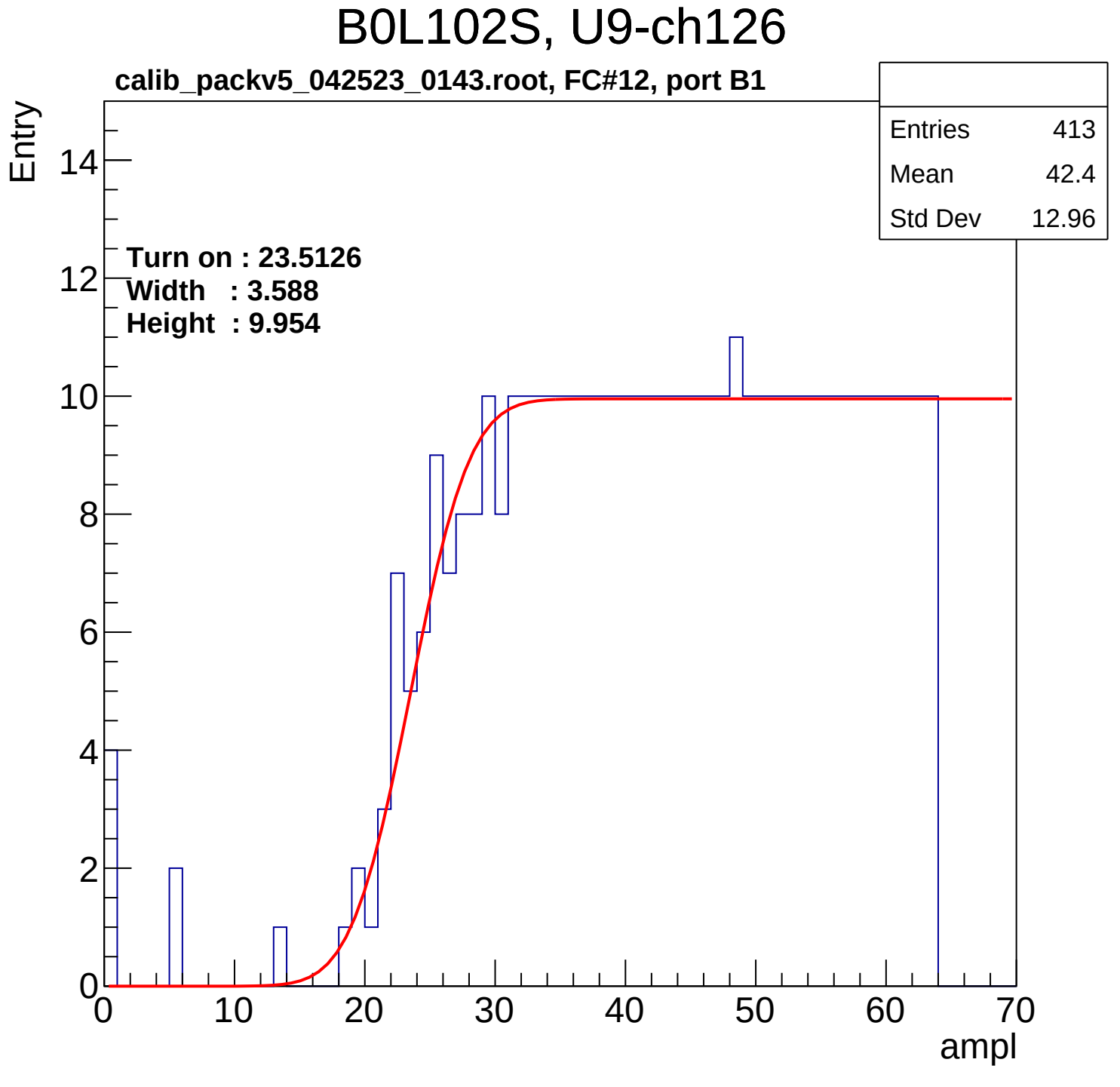

B0L102S, U9-ch121
calib_packv5_042523_0143.root, FC#12, port B1
Entries 402
Mean 43.2
Std Dev 12
Turn on : 24.4557
Width : 4.268
Height : 10.079
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

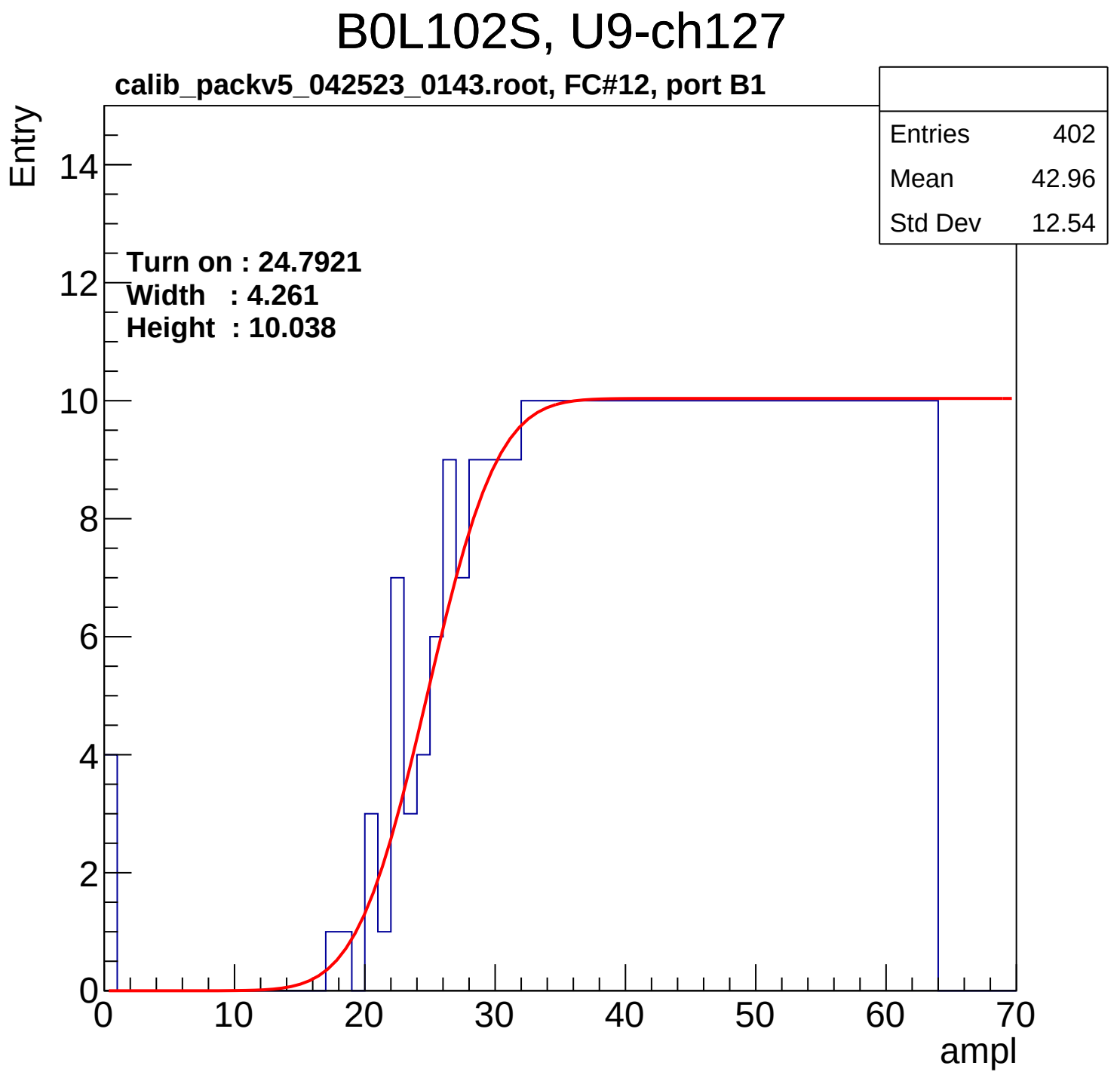

B0L102S, U9-ch122
calib_packv5_042523_0143.root, FC#12, port B1
Entries 414
Mean 42.34
Std Dev 12.97
Turn on : 23.4800
Width : 3.036
Height : 9.979
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

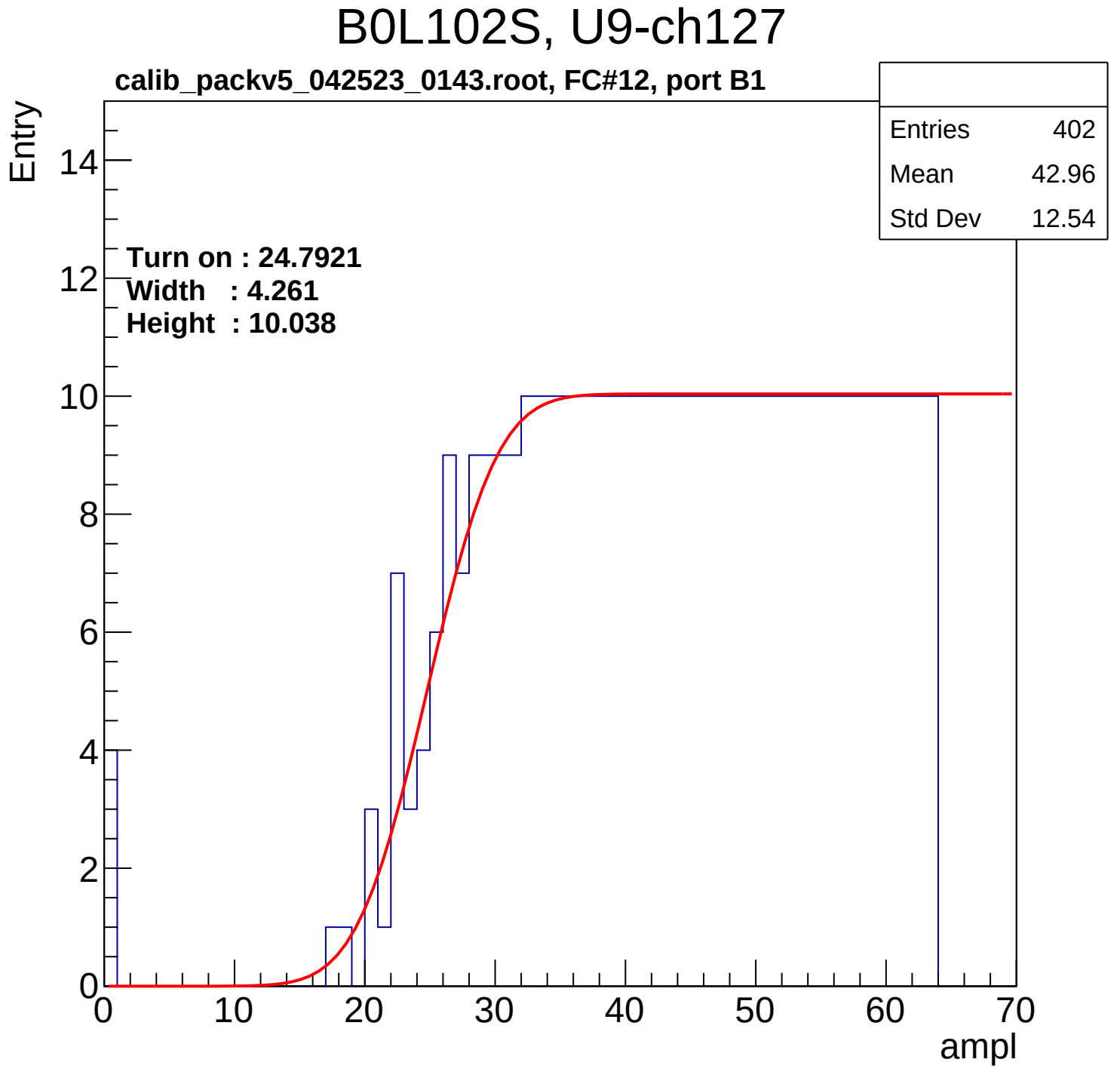

B0L102S, U9-ch123
calib_packv5_042523_0143.root, FC#12, port B1
Entries 393
Mean 43.44
Std Dev 12.26
Turn on : 24.8513
Width : 4.843
Height : 10.052
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L102S, U9-ch124
calib_packv5_042523_0143.root, FC#12, port B1
Entries 403
Mean 43.01
Std Dev 12.41
Turn on : 24.1461
Width : 2.881
Height : 9.999
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L102S, U9-ch125
calib_packv5_042523_0143.root, FC#12, port B1
Entries 380
Mean 44.26
Std Dev 11.52
Turn on : 26.5344
Width : 2.710
Height : 10.014
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L102S, U9-ch126
calib_packv5_042523_0143.root, FC#12, port B1
Entries 413
Mean 42.4
Std Dev 12.96
Turn on : 23.5126
Width : 3.588
Height : 9.954
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L102S, U9-ch127
calib_packv5_042523_0143.root, FC#12, port B1
Entries 402
Mean 42.96
Std Dev 12.54
Turn on : 24.7921
Width : 4.261
Height : 10.038
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L102S, U9-ch127
calib_packv5_042523_0143.root, FC#12, port B1
Entries 402
Mean 42.96
Std Dev 12.54
Turn on : 24.7921
Width : 4.261
Height : 10.038
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70