



# B0L001S, U10-ch0, adc0

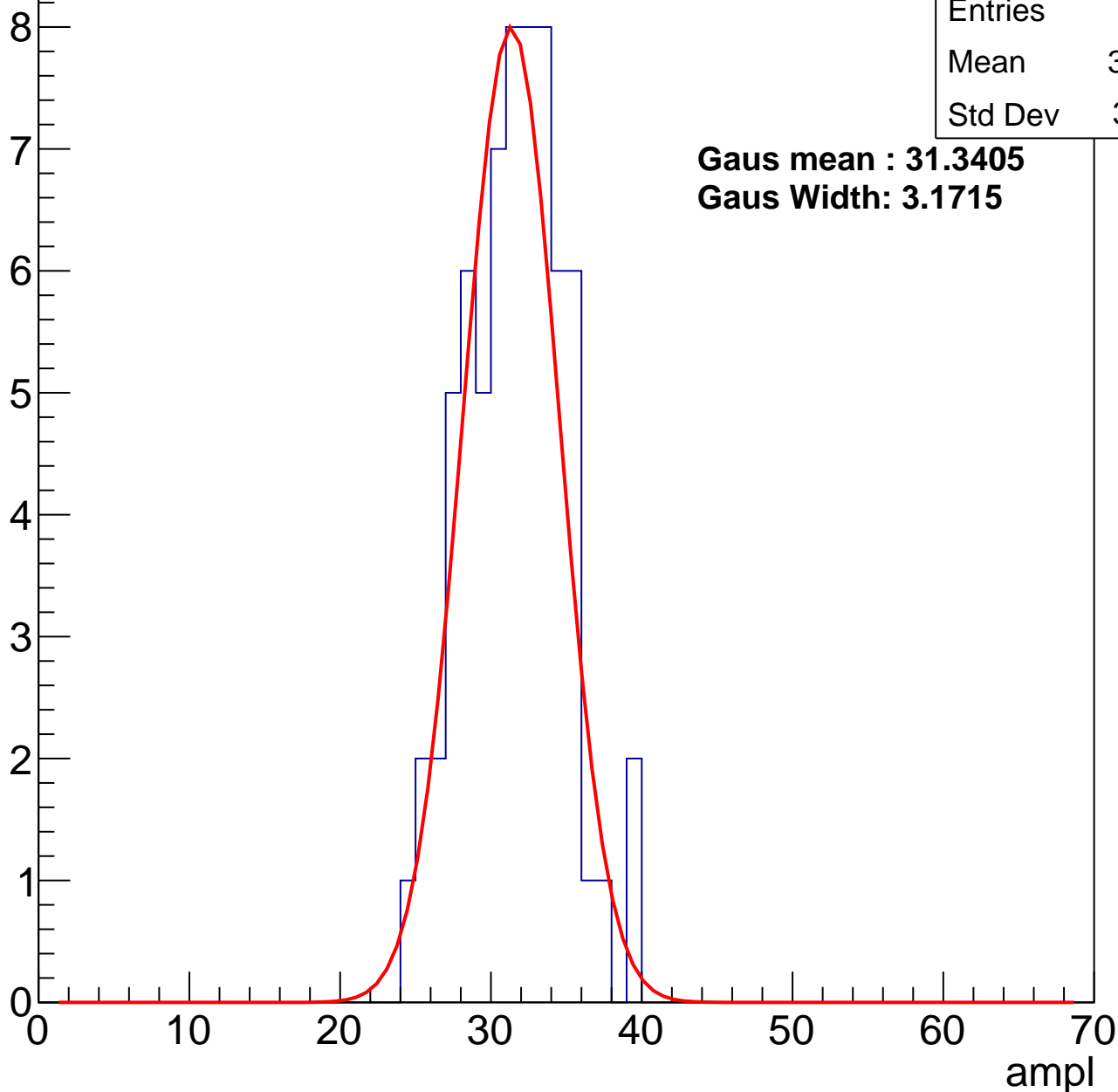
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	31.13
Std Dev	3.231

**Gaus mean : 31.3405**

**Gaus Width: 3.1715**



# B0L001S, U10-ch0, adc1

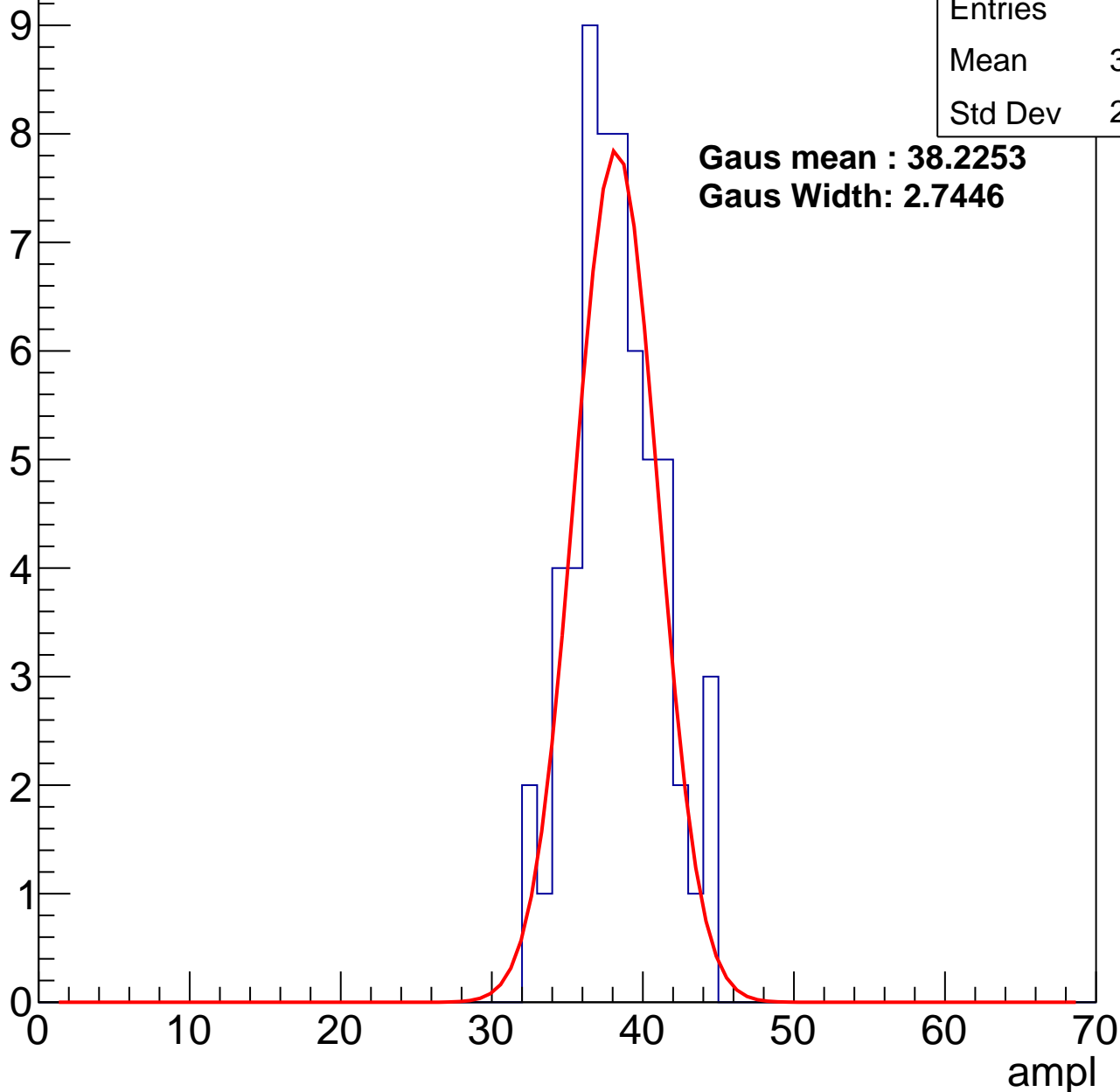
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	37.84
Std Dev	2.864

**Gaus mean : 38.2253**

**Gaus Width: 2.7446**



# B0L001S, U10-ch0, adc2

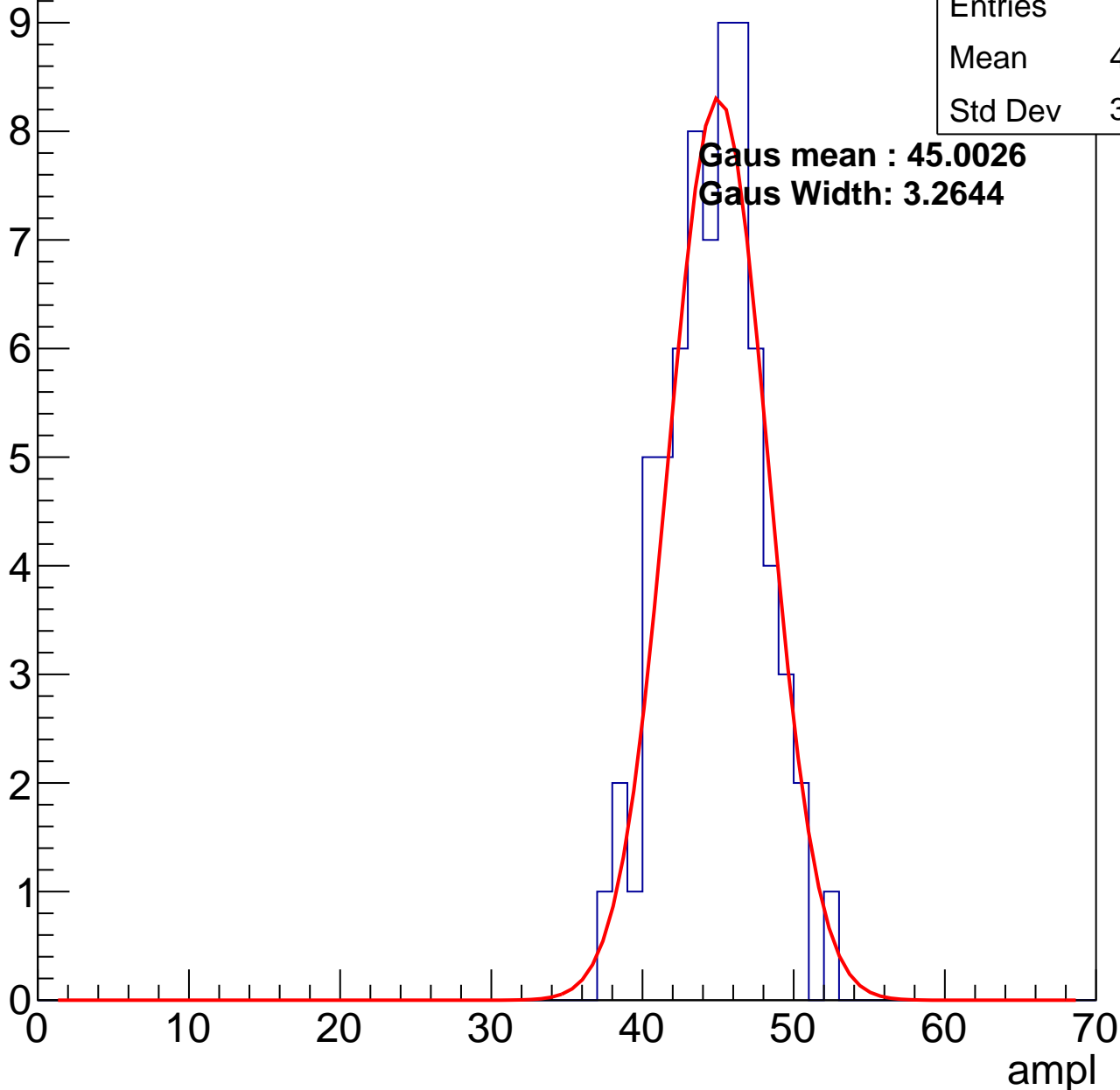
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	44.25
Std Dev	3.123

**Gaus mean : 45.0026**

**Gaus Width: 3.2644**



# B0L001S, U10-ch0, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

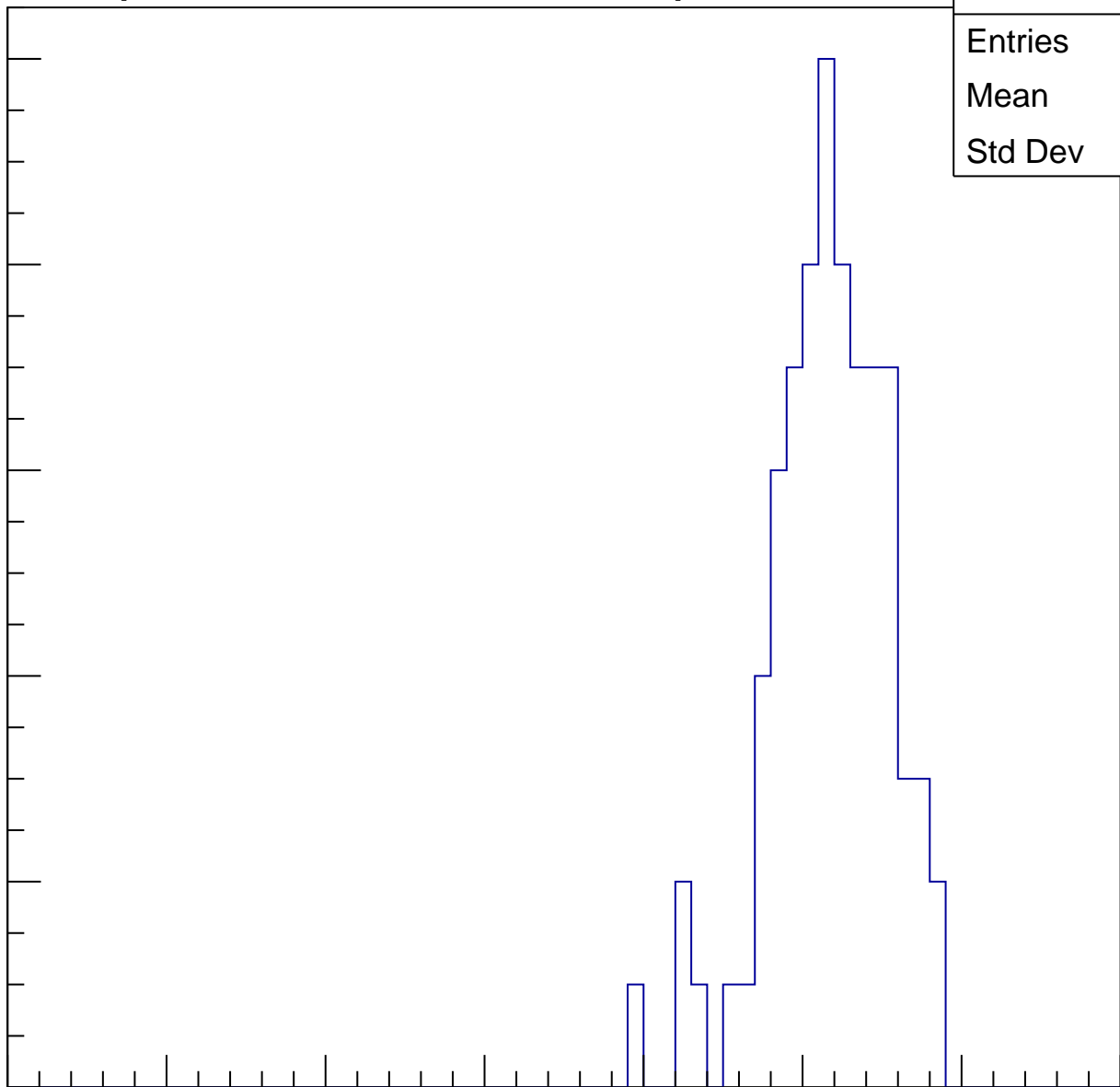
Entries	78
Mean	51.17
Std Dev	3.712

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

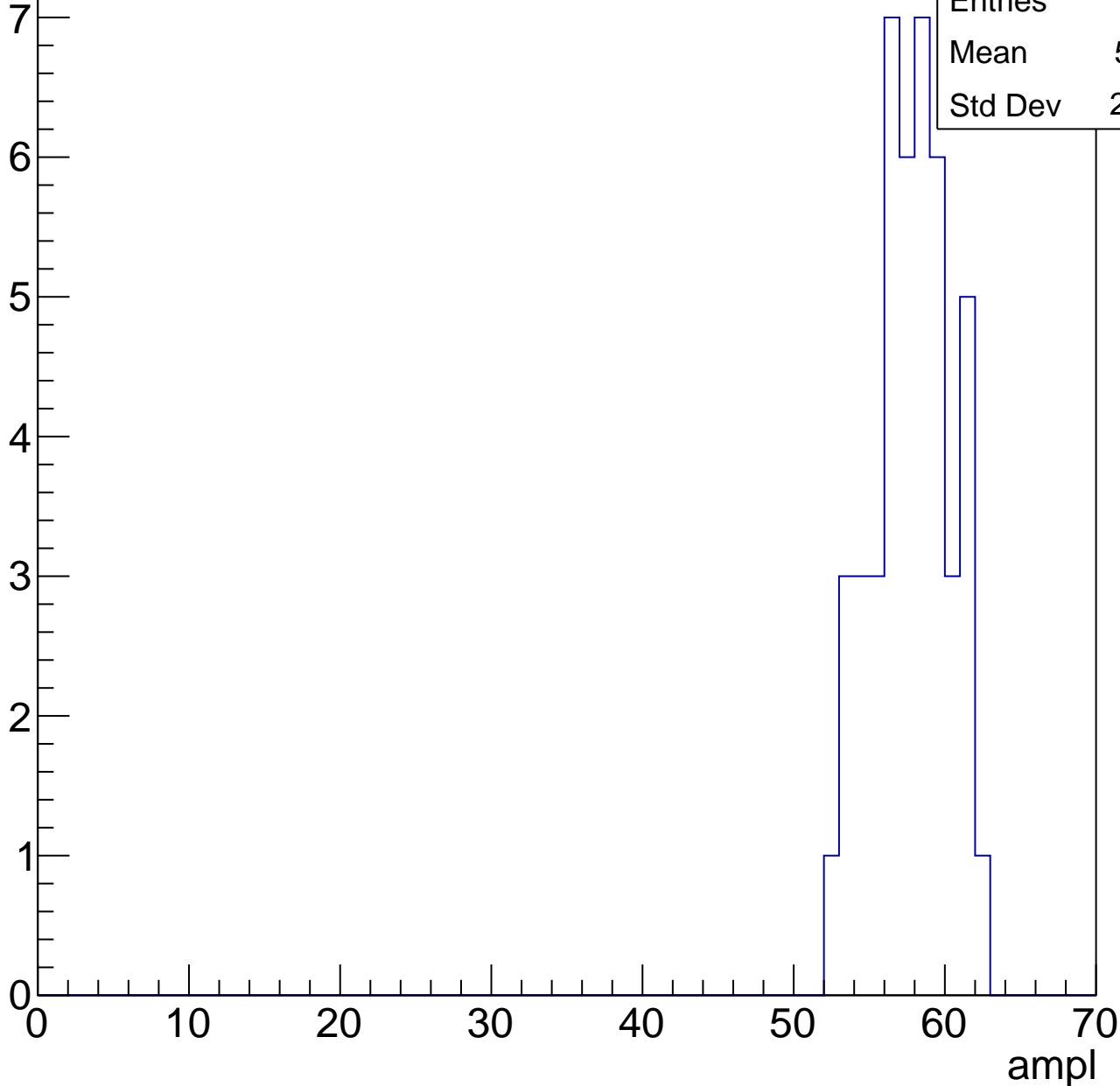


# B0L001S, U10-ch0, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	45
Mean	57.31
Std Dev	2.484



# B0L001S, U10-ch0, adc5

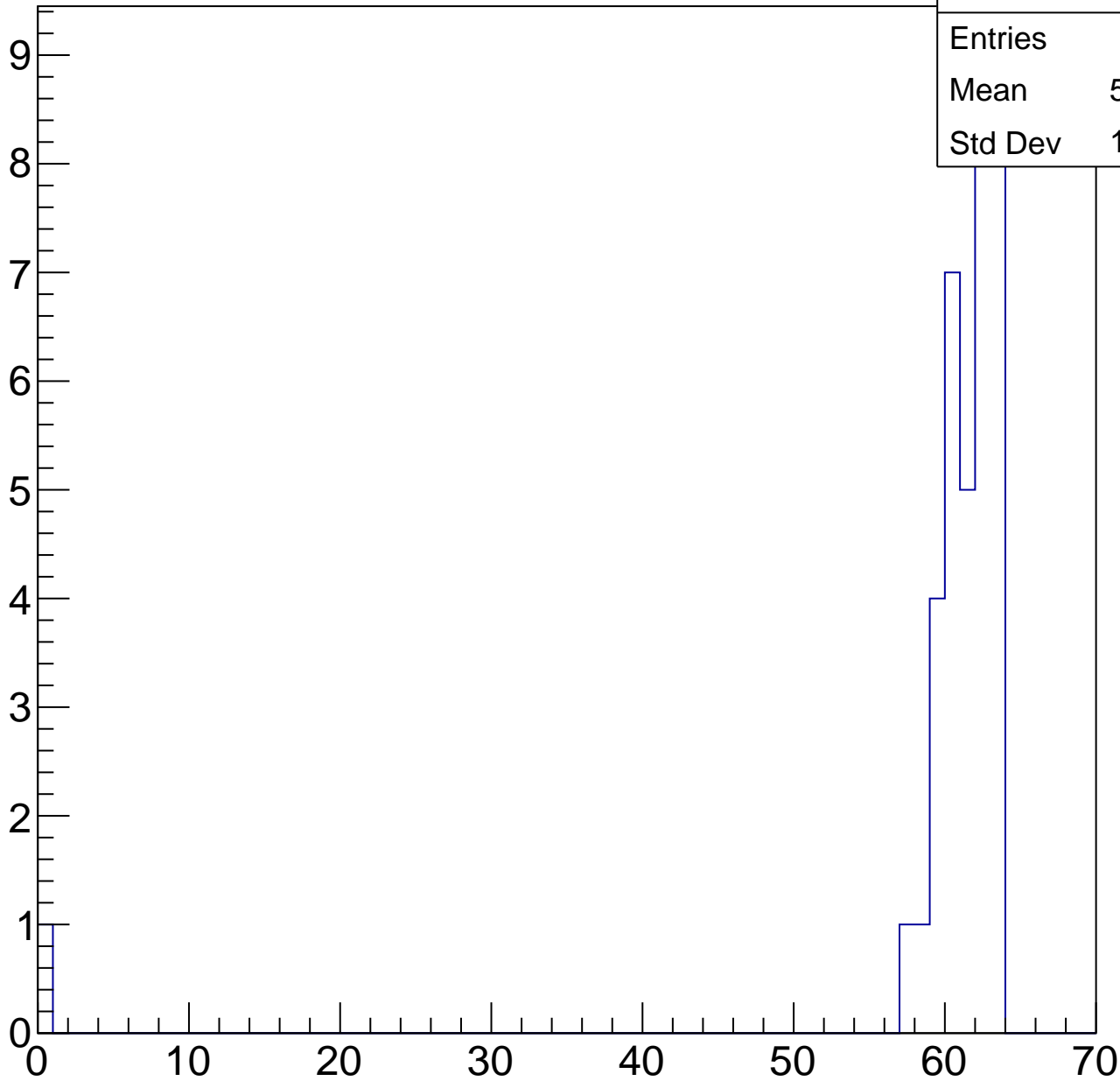
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	36
Mean	59.42
Std Dev	10.17

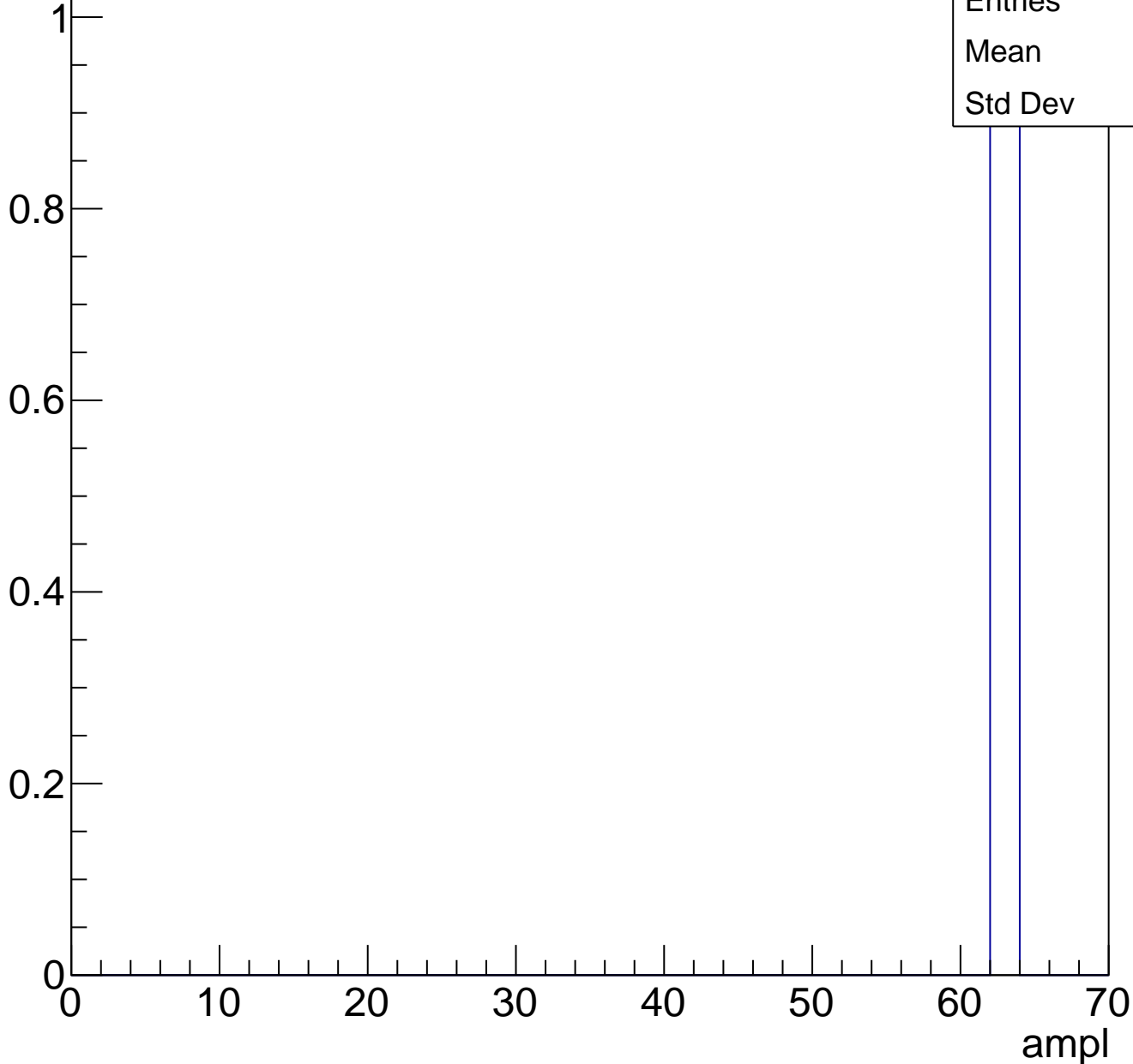
ampl



# B0L001S, U10-ch0, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch0, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U10-ch1, adc0

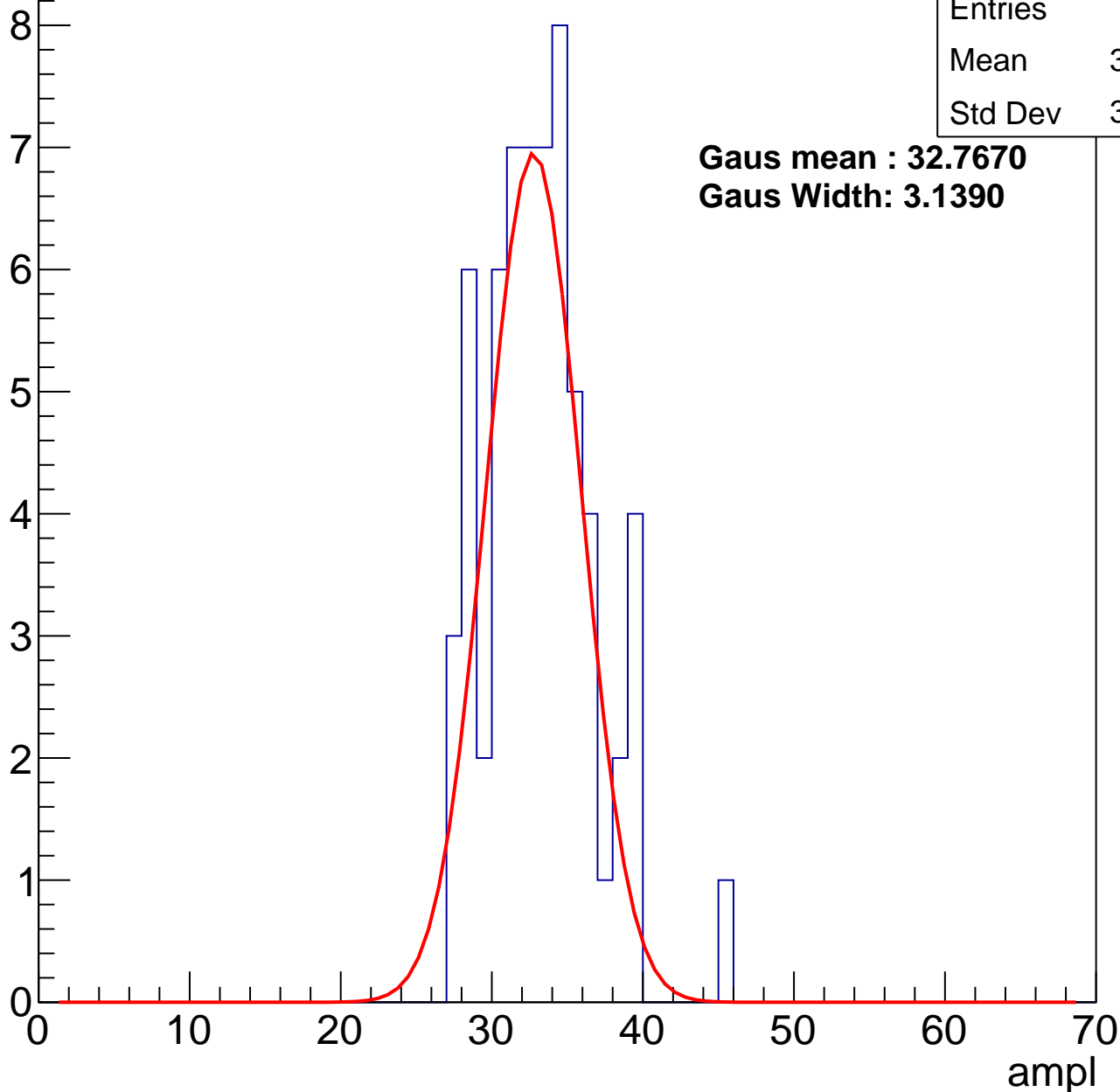
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	32.76
Std Dev	3.549

**Gaus mean : 32.7670**

**Gaus Width: 3.1390**



# B0L001S, U10-ch1, adc1

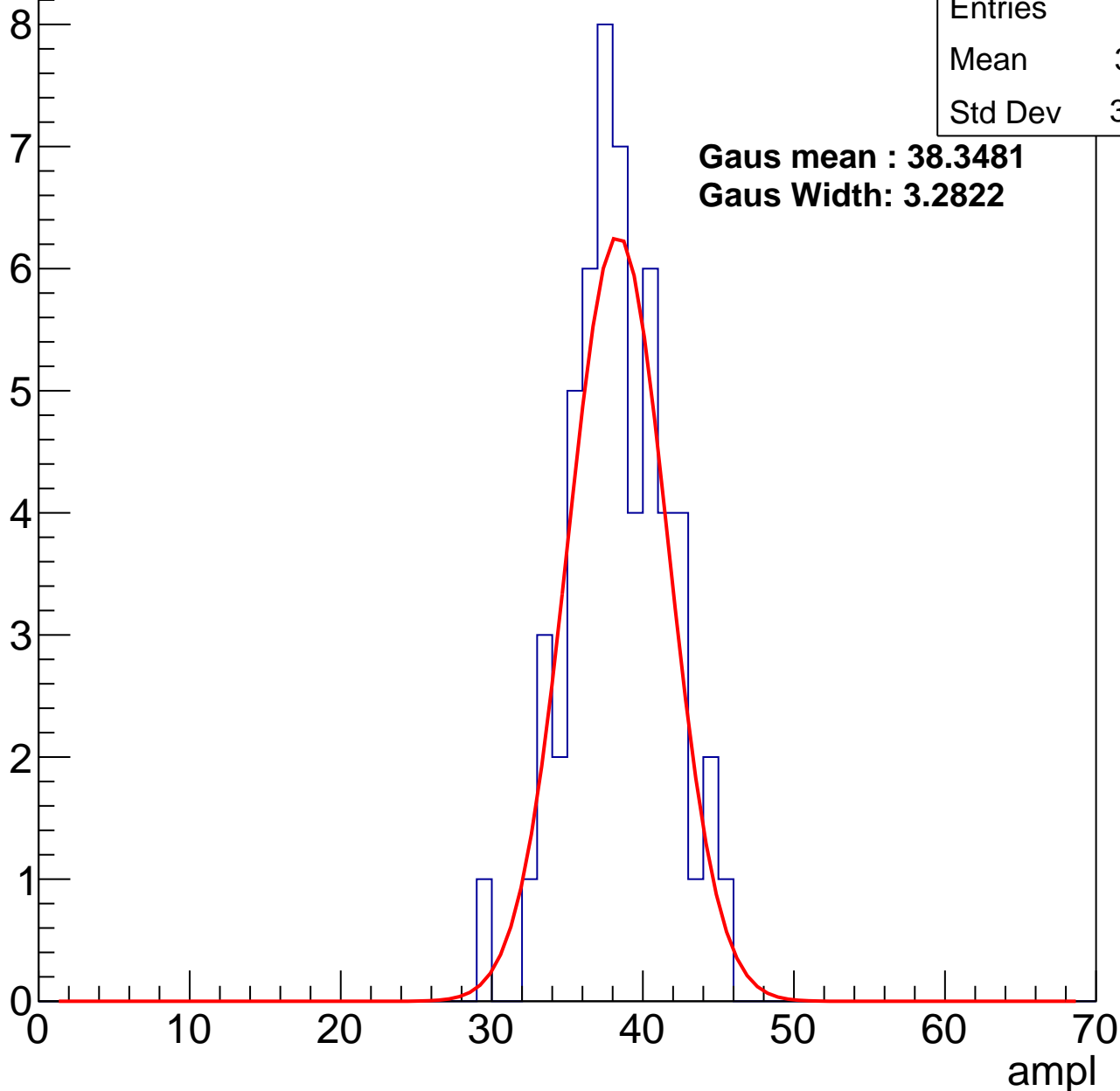
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	37.91
Std Dev	3.232

**Gaus mean : 38.3481**

**Gaus Width: 3.2822**



# B0L001S, U10-ch1, adc2

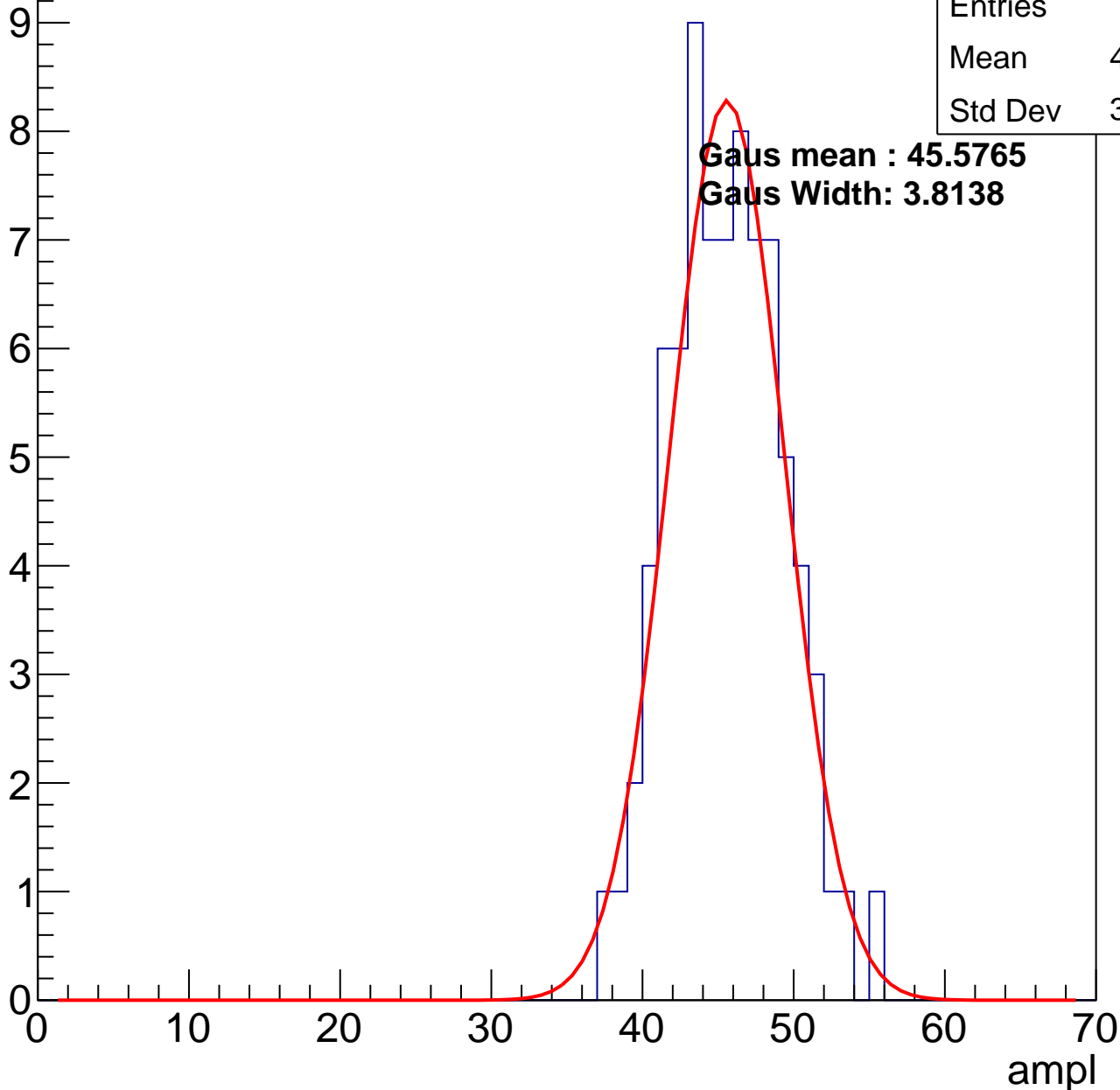
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	80
Mean	45.15
Std Dev	3.668

**Gaus mean : 45.5765**

**Gaus Width: 3.8138**

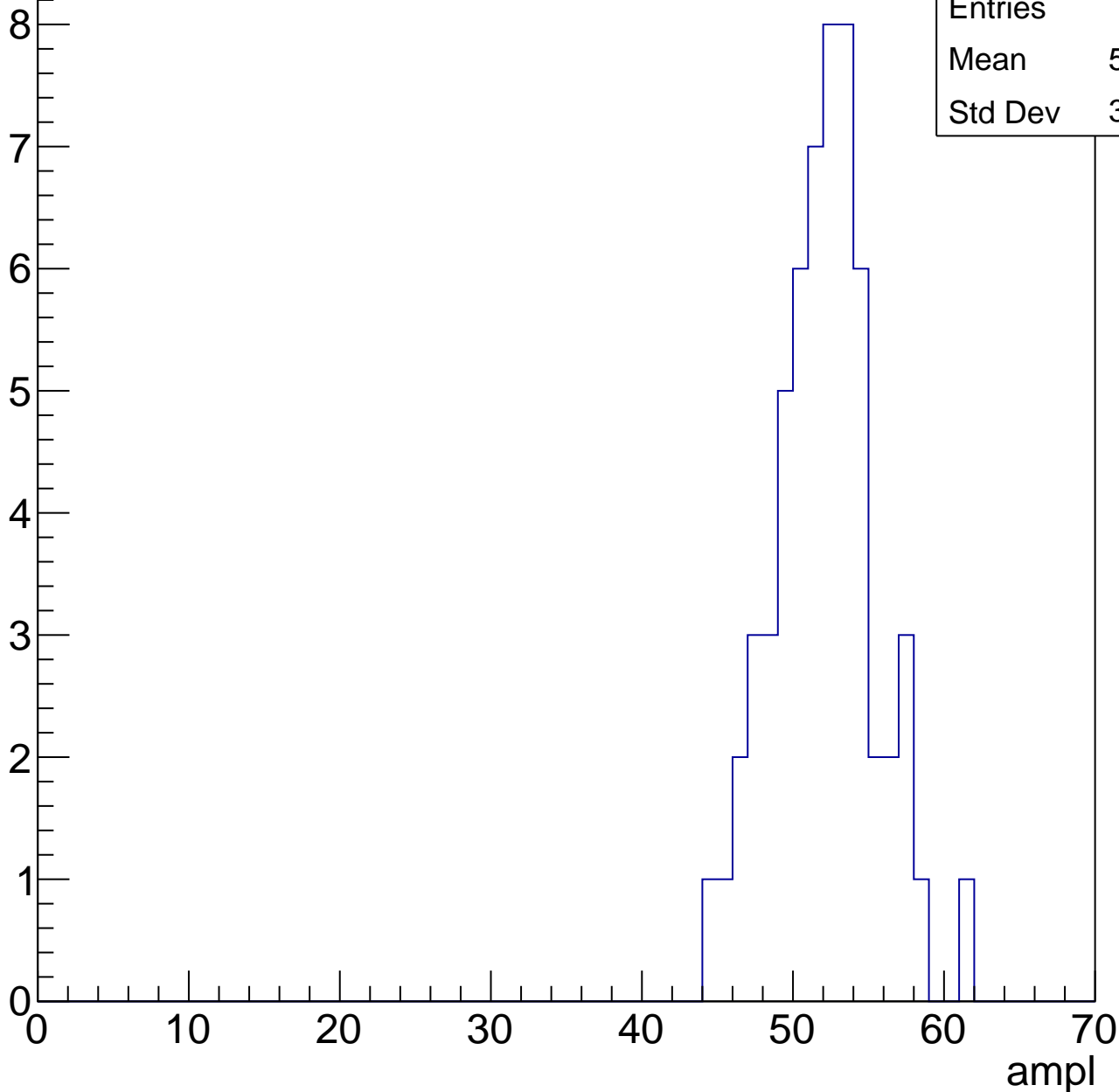


# B0L001S, U10-ch1, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

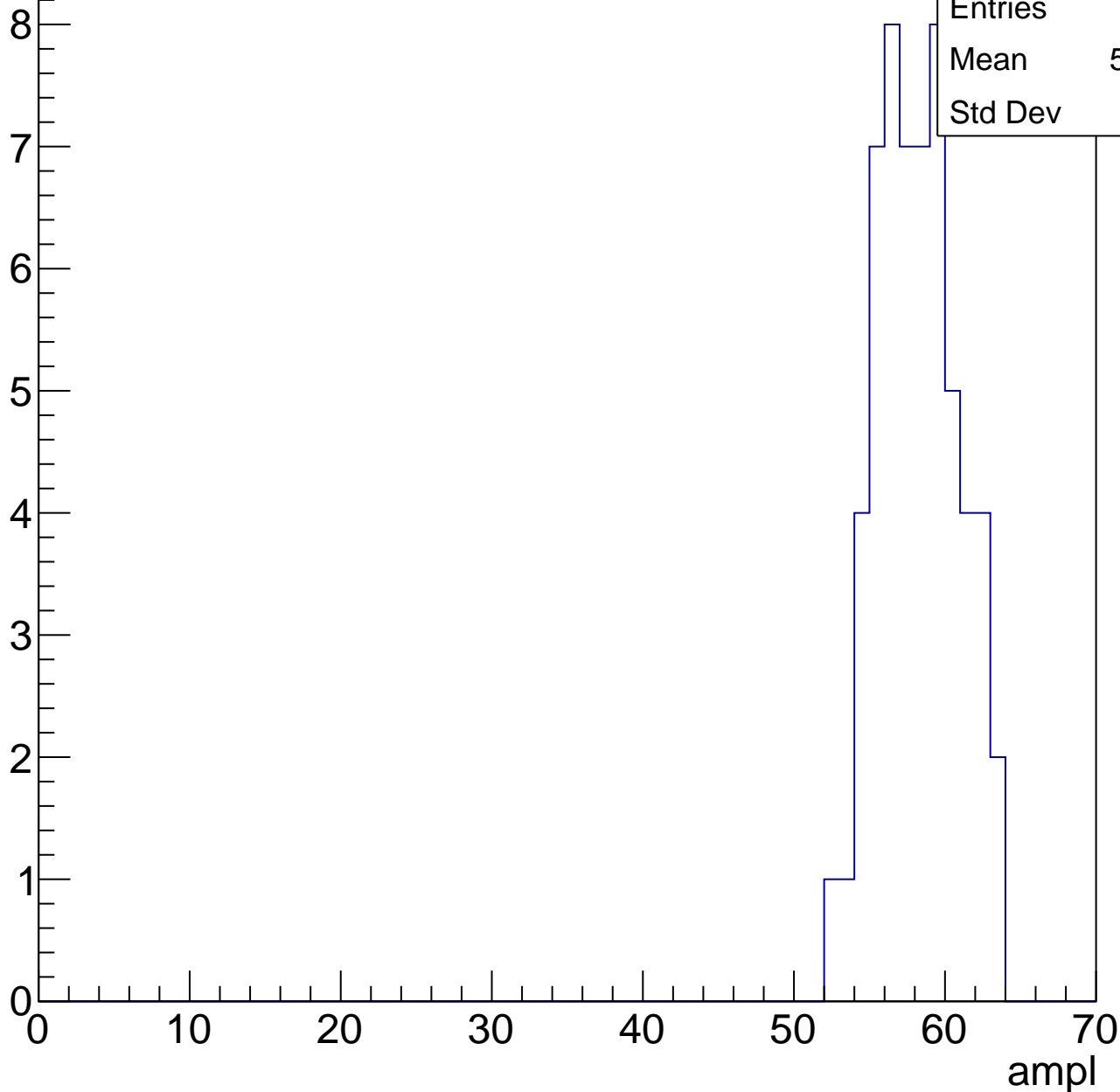
Entries	59
Mean	51.59
Std Dev	3.315



# B0L001S, U10-ch1, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



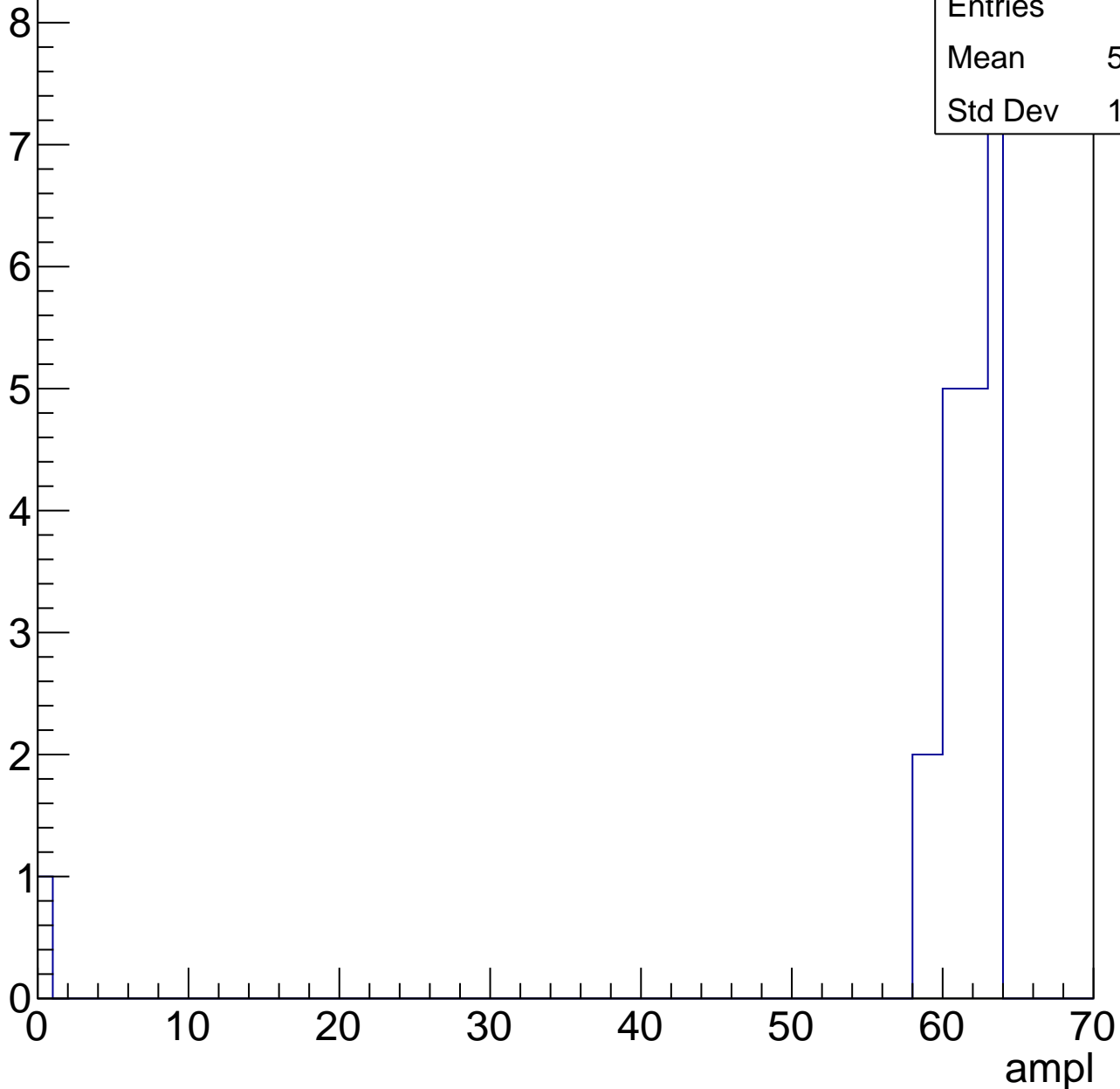
Entries	58
Mean	57.74
Std Dev	2.63

# B0L001S, U10-ch1, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	28
Mean	59.04
Std Dev	11.47



# B0L001S, U10-ch1, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch1, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U10-ch2, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	79
Mean	32.25
Std Dev	3.407

**Gaus mean : 32.6329**

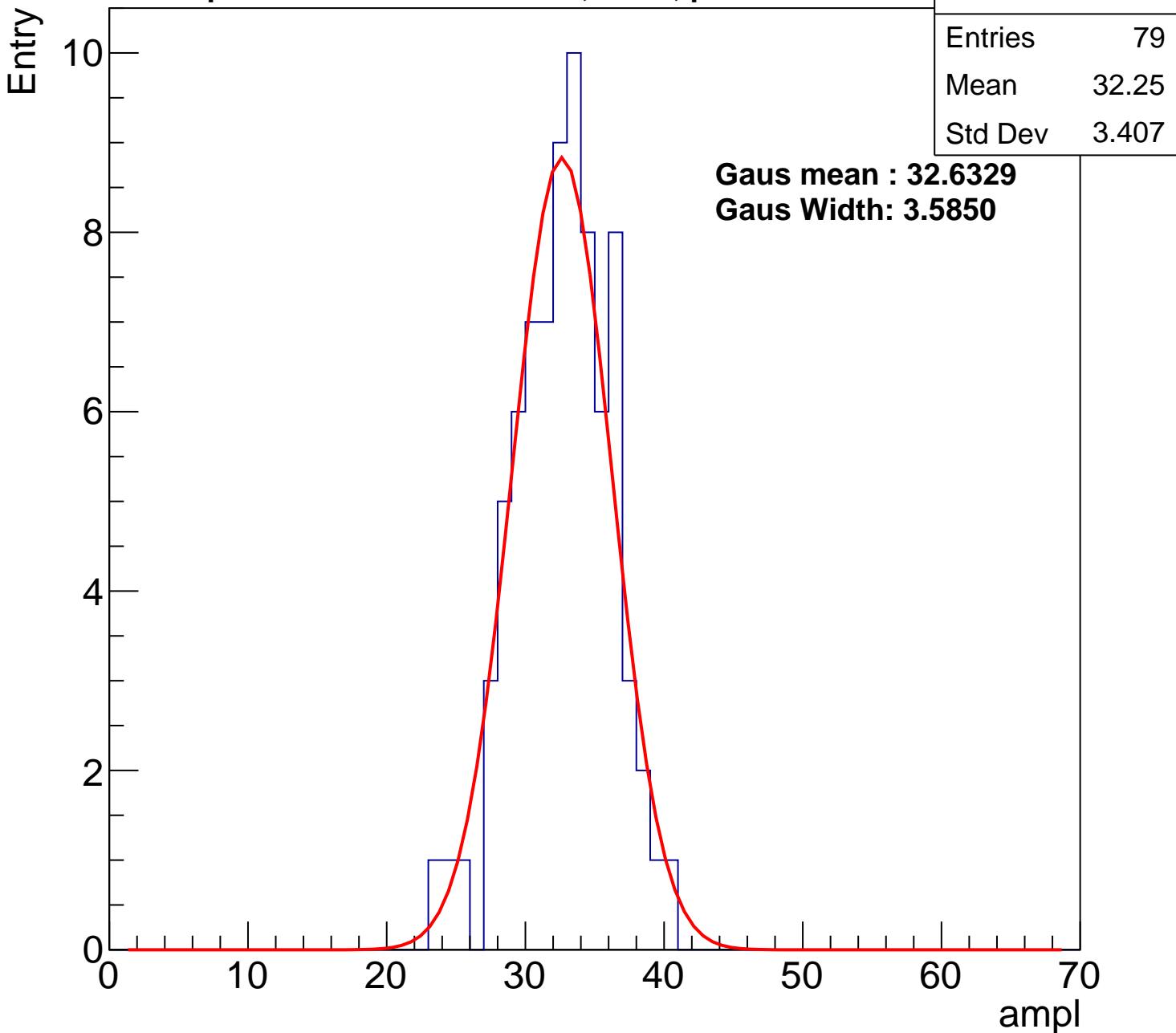
**Gaus Width: 3.5850**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U10-ch2, adc1

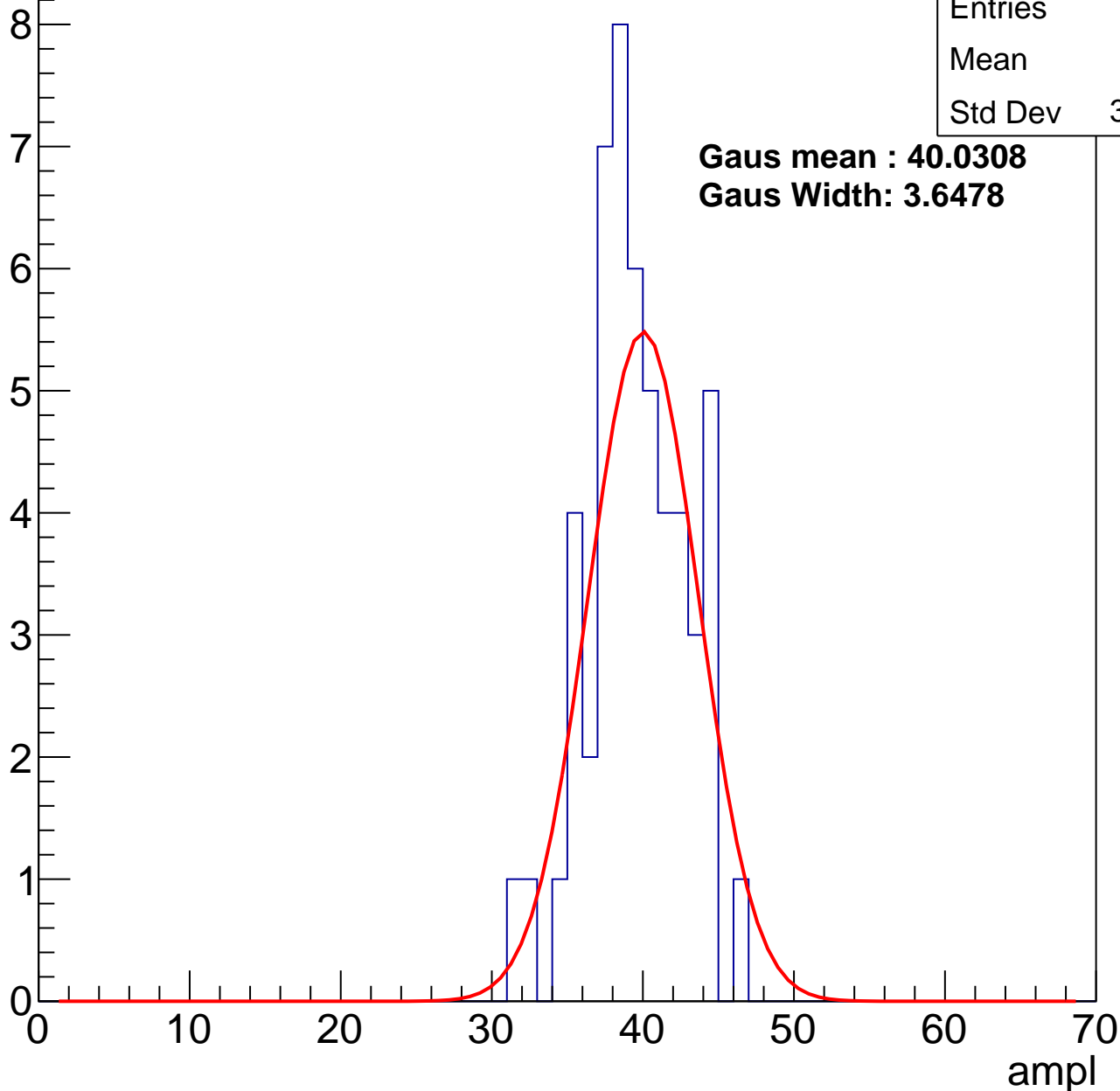
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	39.1
Std Dev	3.206

**Gaus mean : 40.0308**

**Gaus Width: 3.6478**



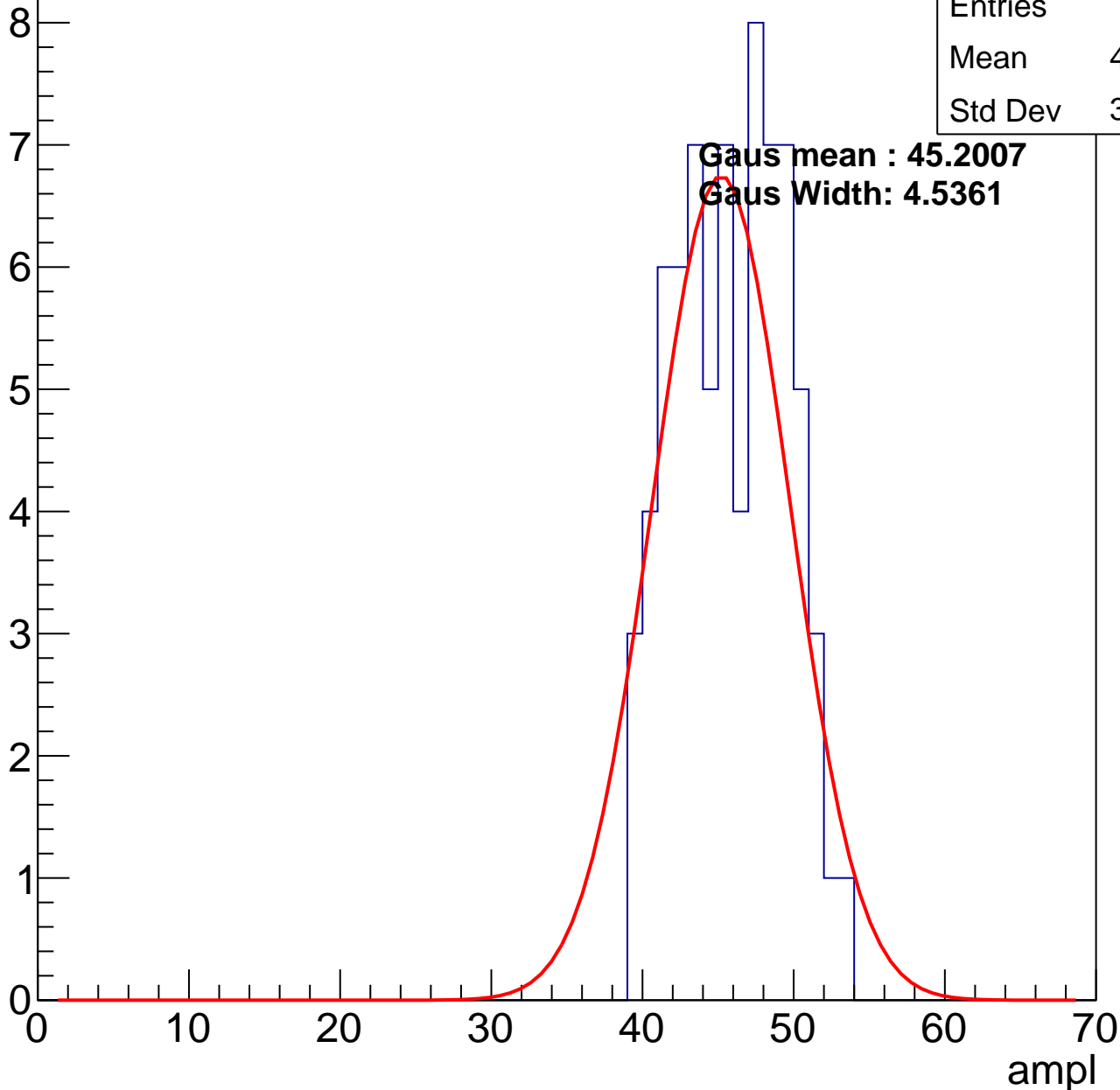
# B0L001S, U10-ch2, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	45.38
Std Dev	3.559

**Gaus mean : 45.2007**  
**Gaus Width: 4.5361**

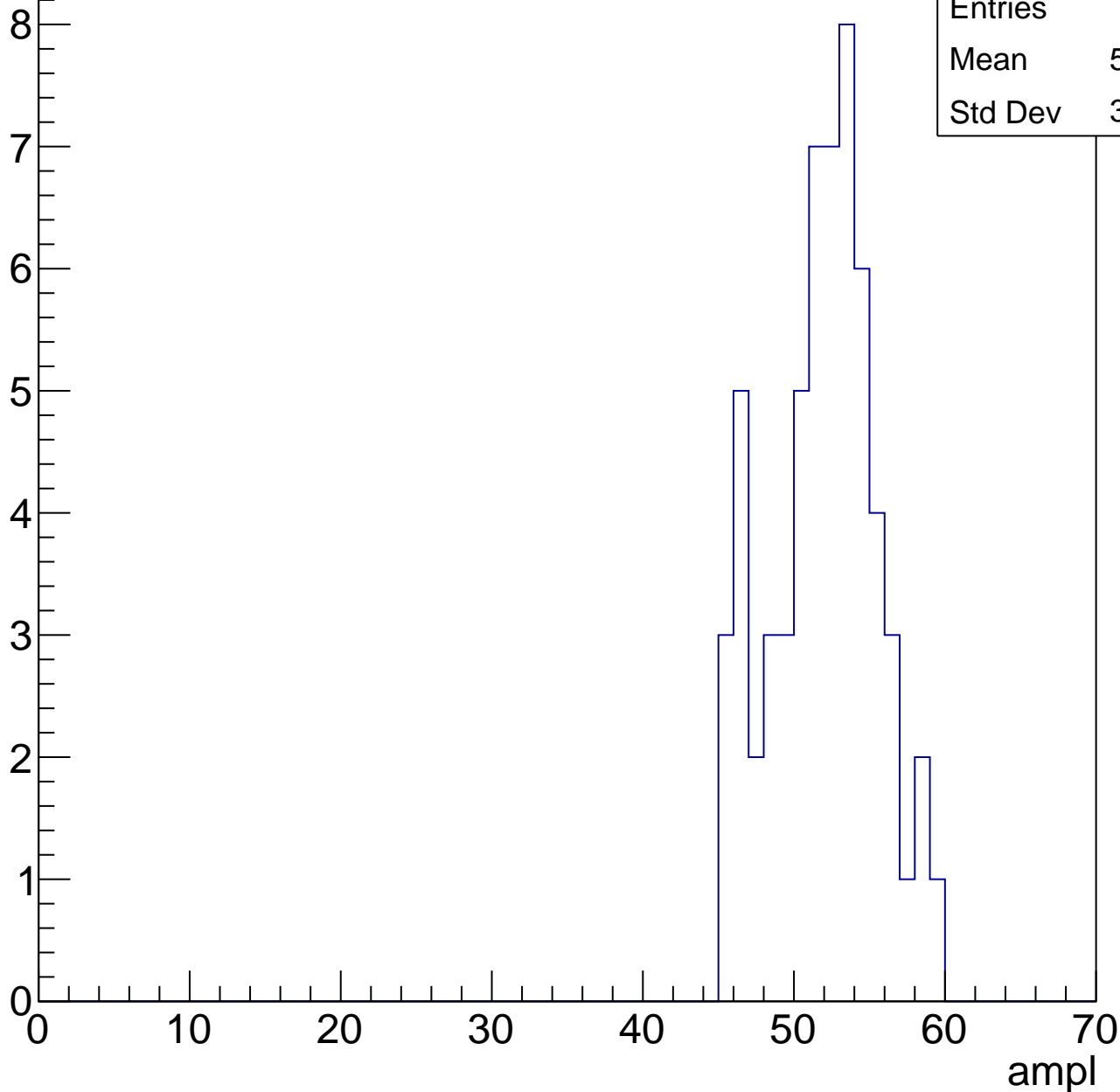


# B0L001S, U10-ch2, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

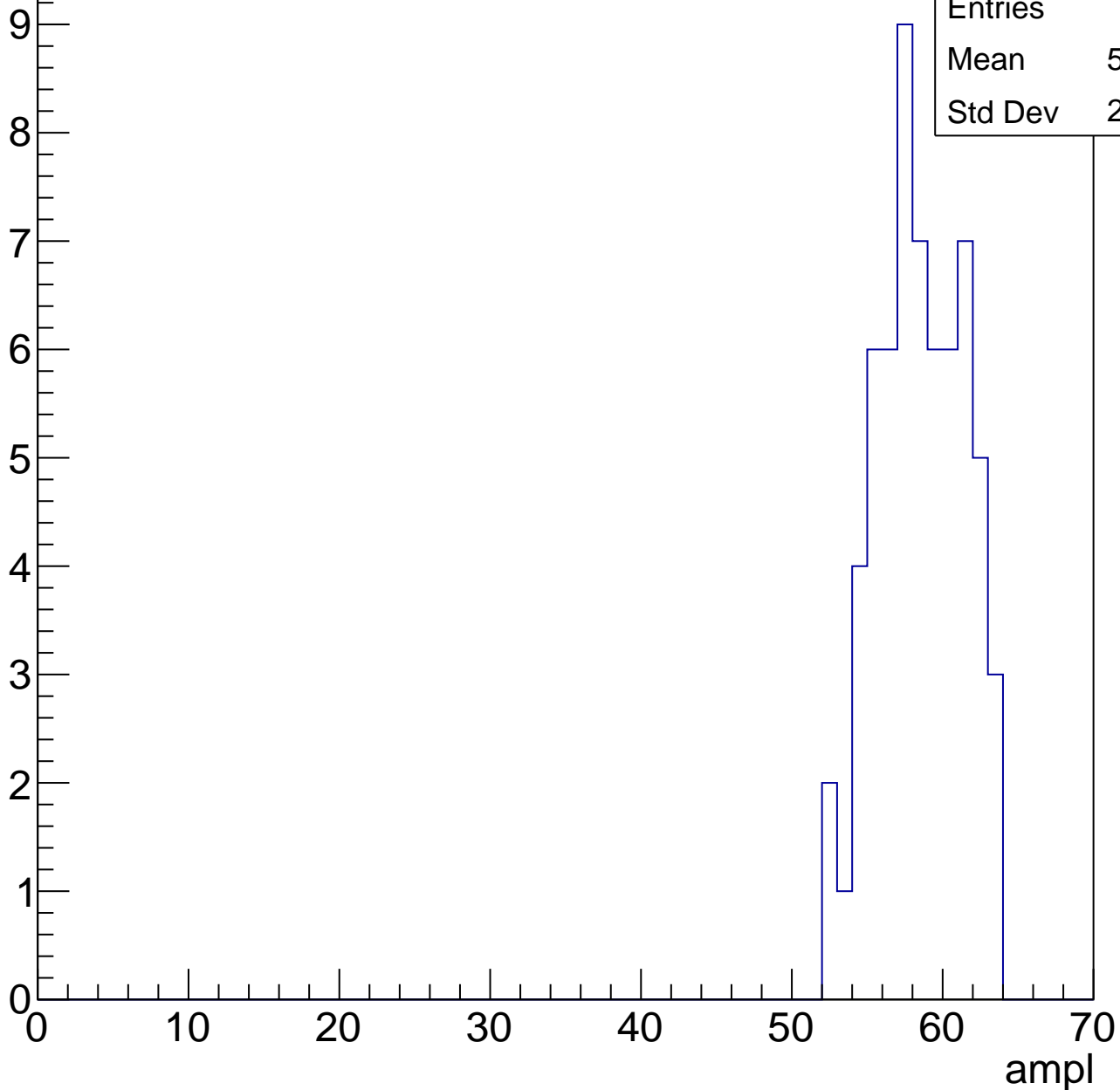
Entries	60
Mean	51.48
Std Dev	3.476



# B0L001S, U10-ch2, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



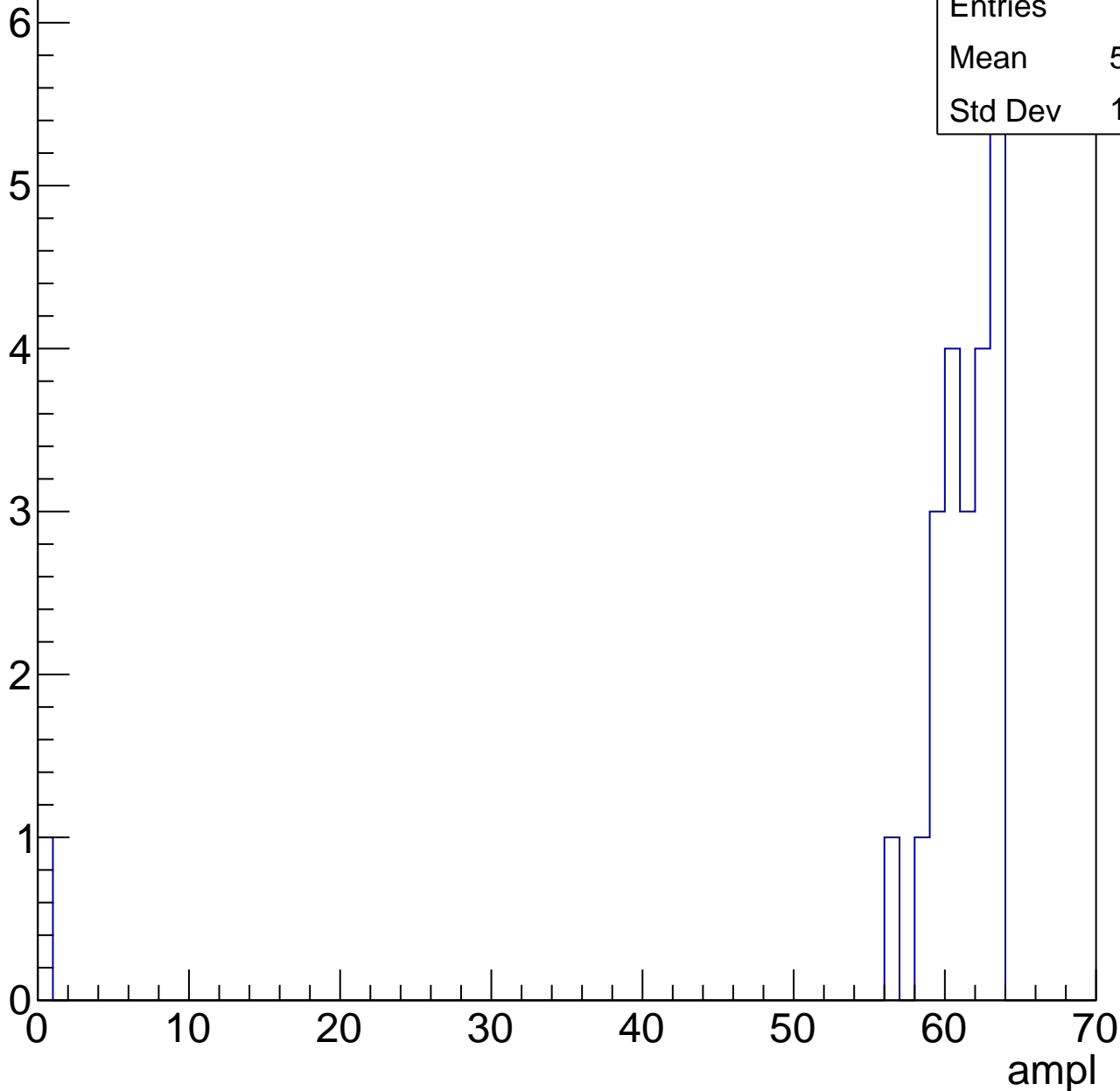
Entries	62
Mean	58.03
Std Dev	2.828

# B0L001S, U10-ch2, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

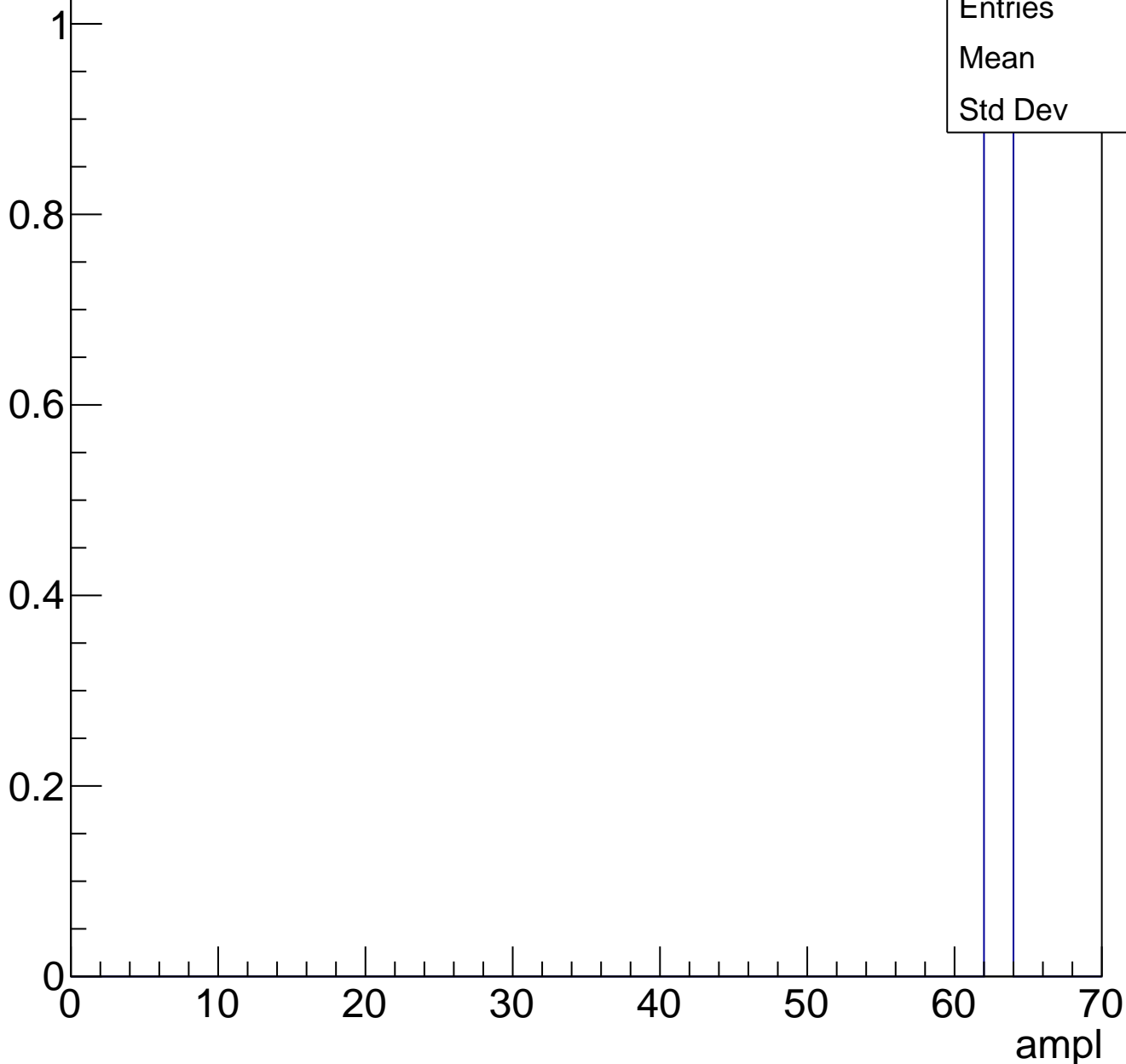
Entries	23
Mean	58.26
Std Dev	12.56



# B0L001S, U10-ch2, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch2, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U10-ch3, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	74
Mean	30.45
Std Dev	3.441

**Gaus mean : 30.9000**

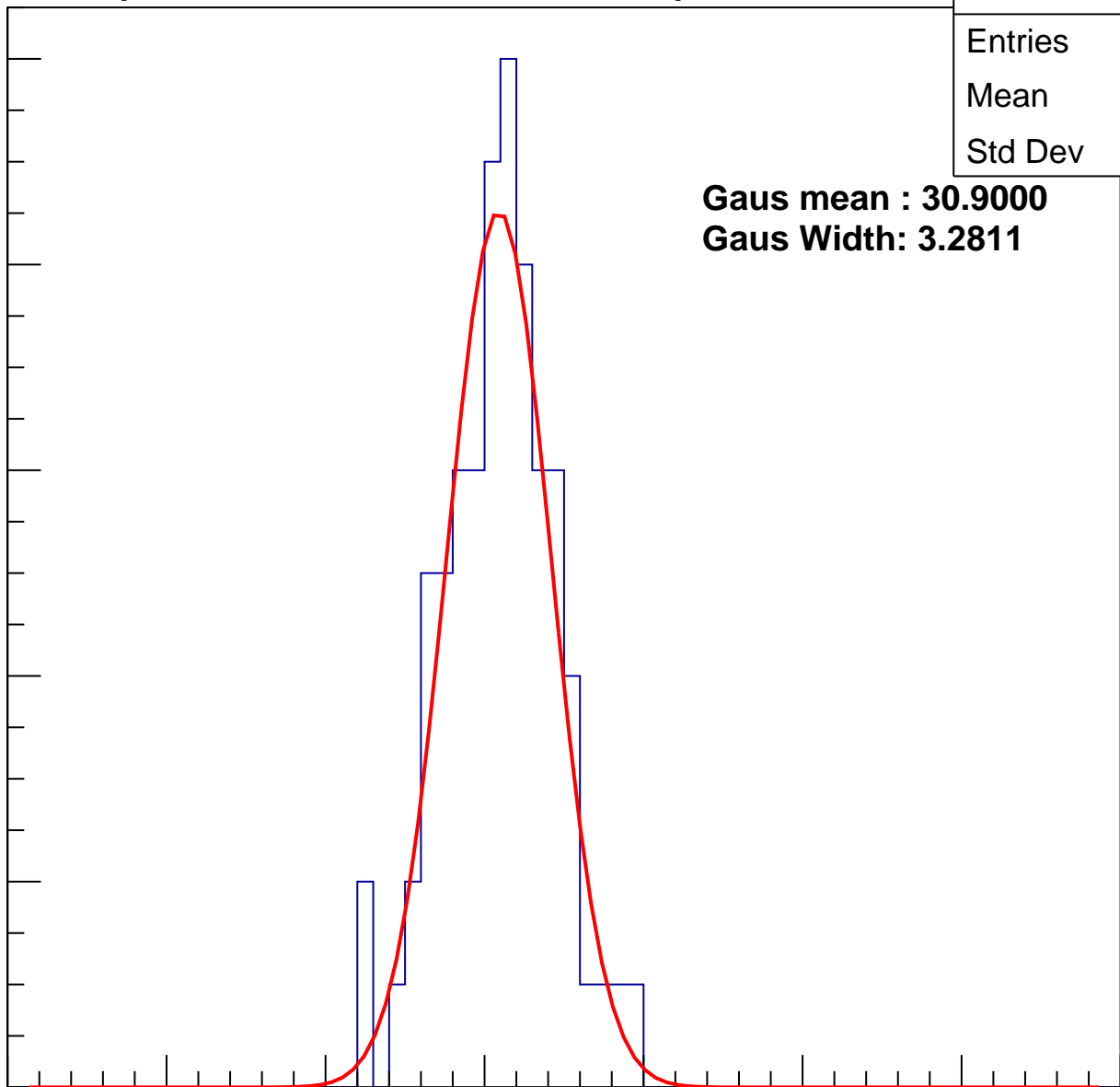
**Gaus Width: 3.2811**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U10-ch3, adc1

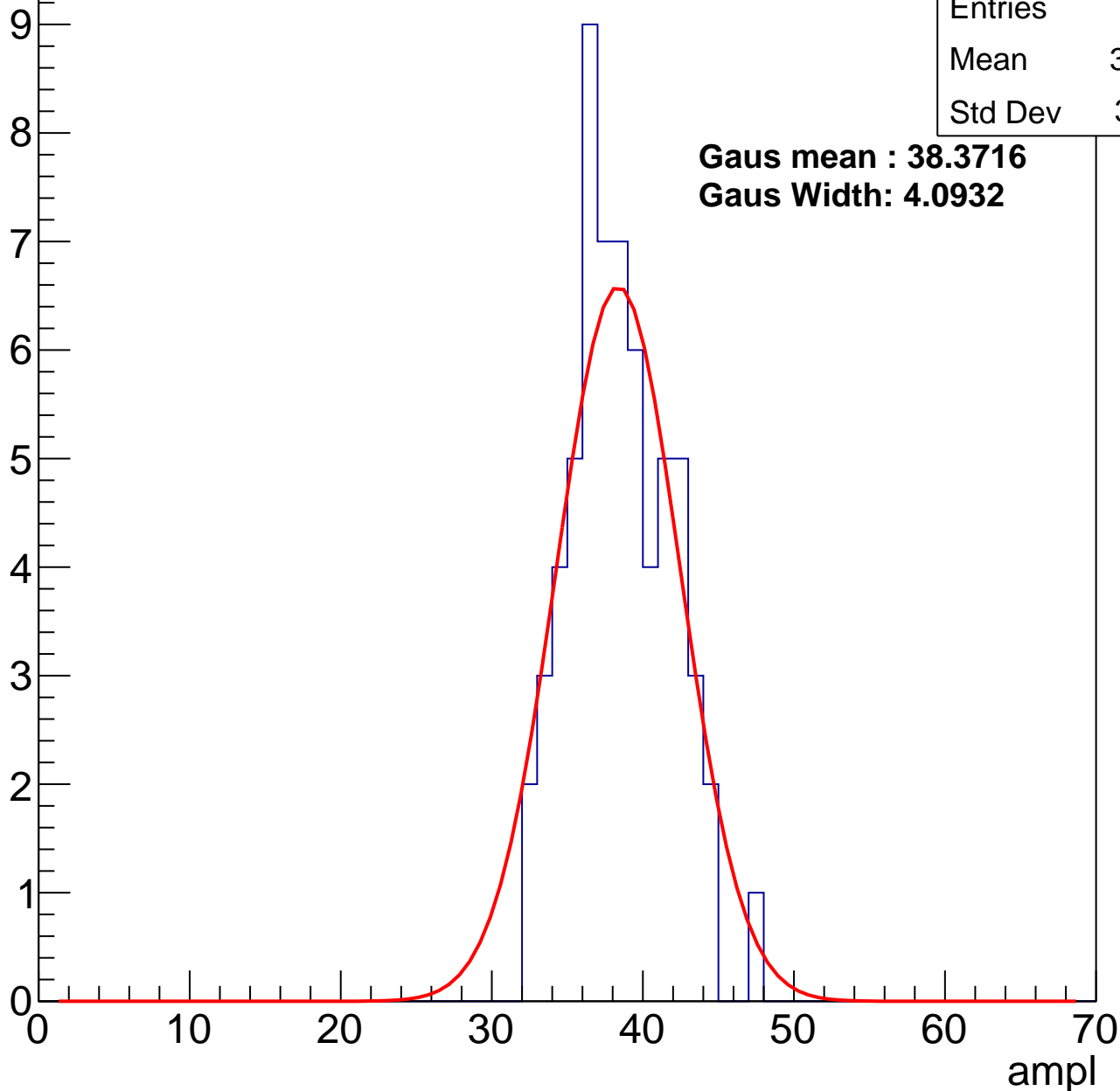
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	38.03
Std Dev	3.271

**Gaus mean : 38.3716**

**Gaus Width: 4.0932**



# B0L001S, U10-ch3, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	80
Mean	44.56
Std Dev	3.911

**Gaus mean : 44.9451**

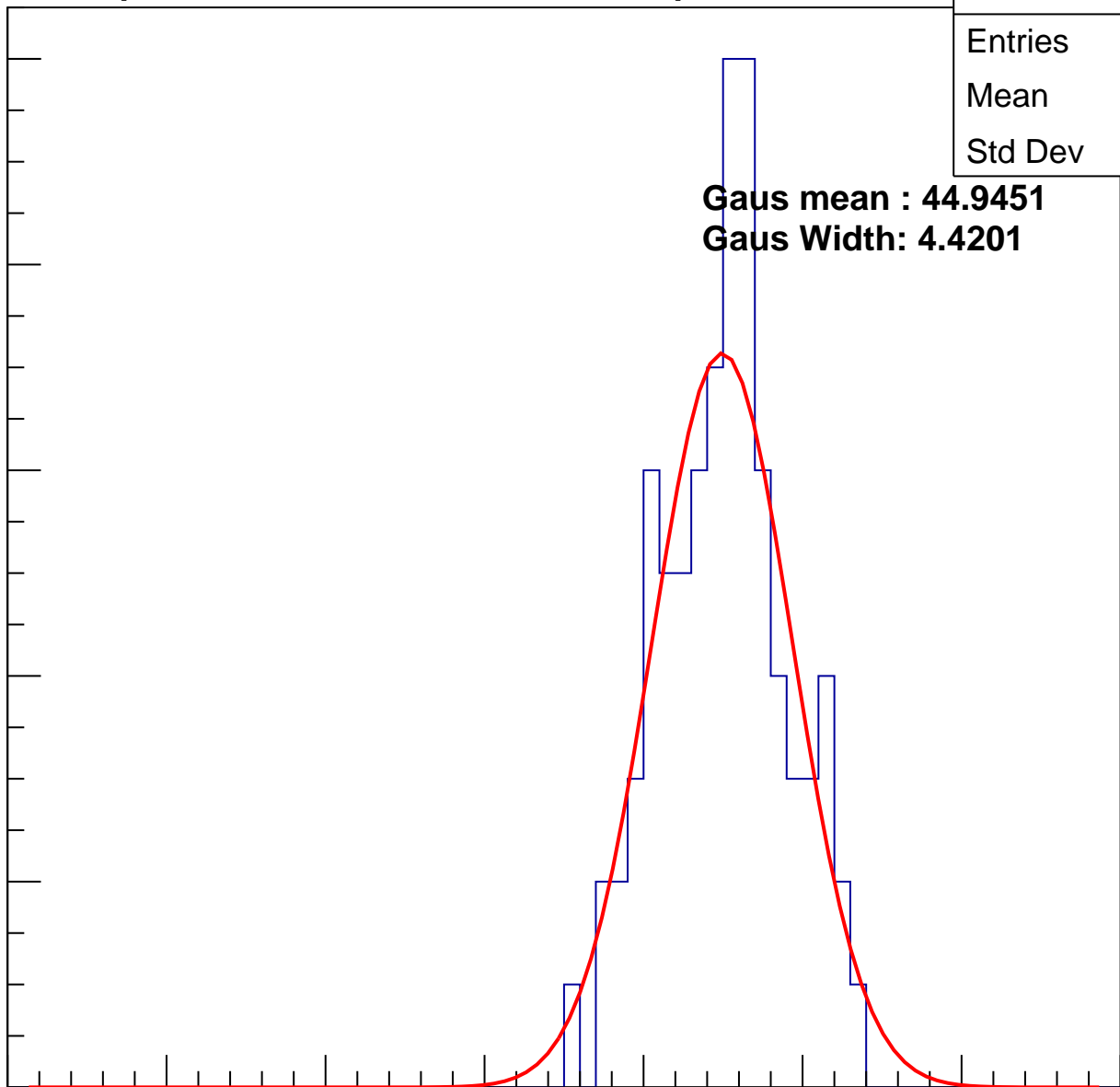
**Gaus Width: 4.4201**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

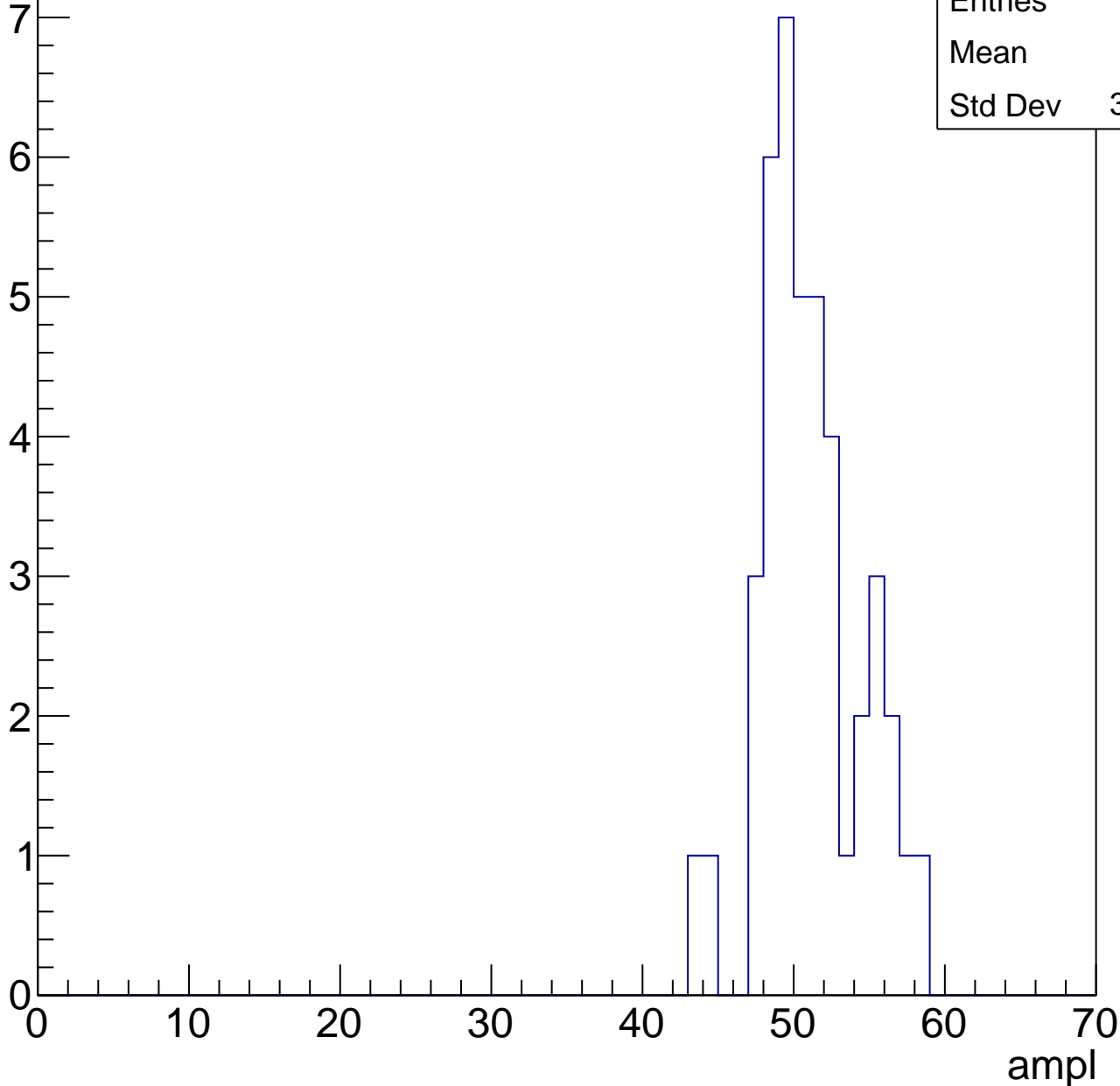


# B0L001S, U10-ch3, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	42
Mean	50.6
Std Dev	3.274

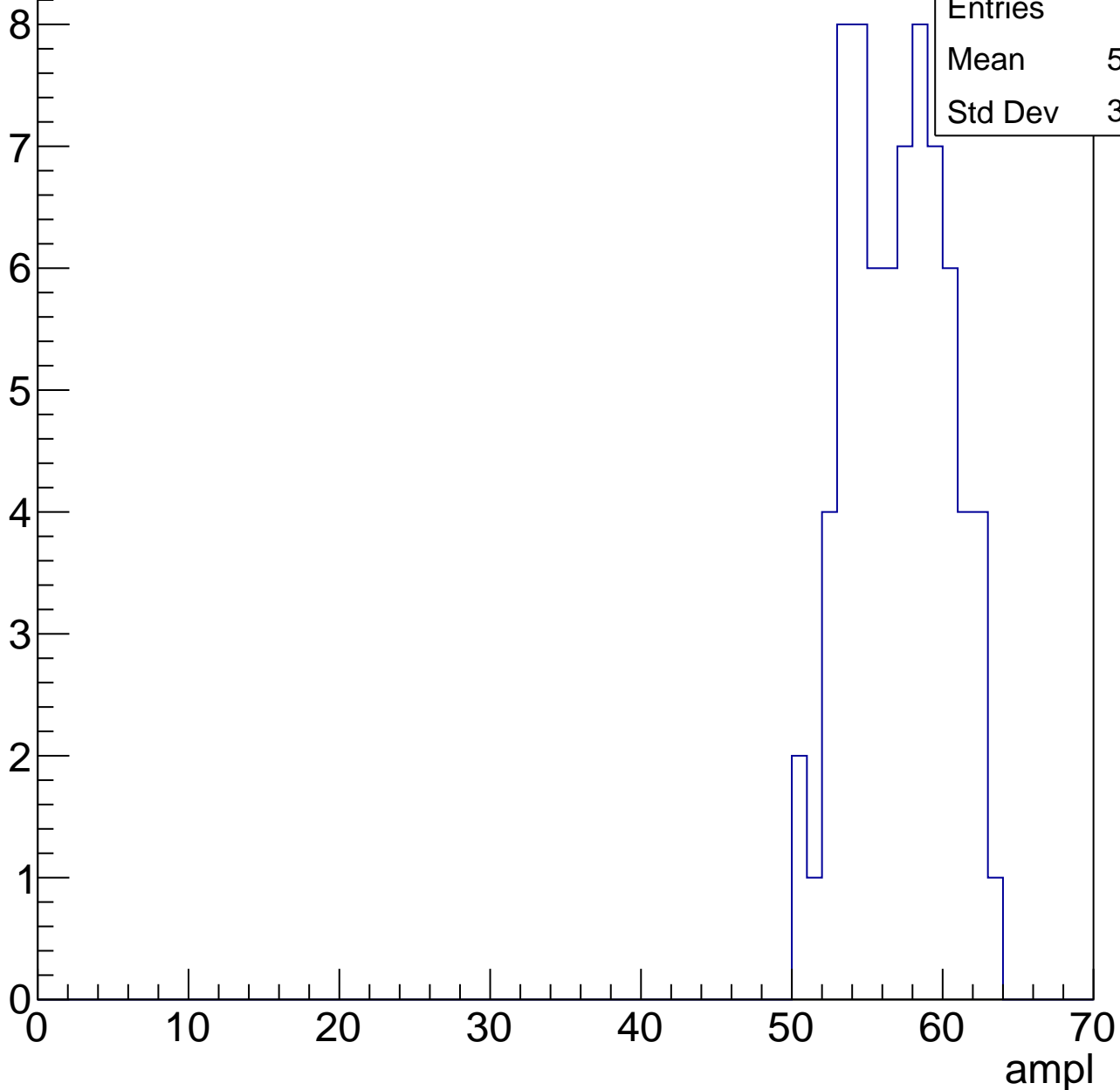


# B0L001S, U10-ch3, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	56.56
Std Dev	3.205

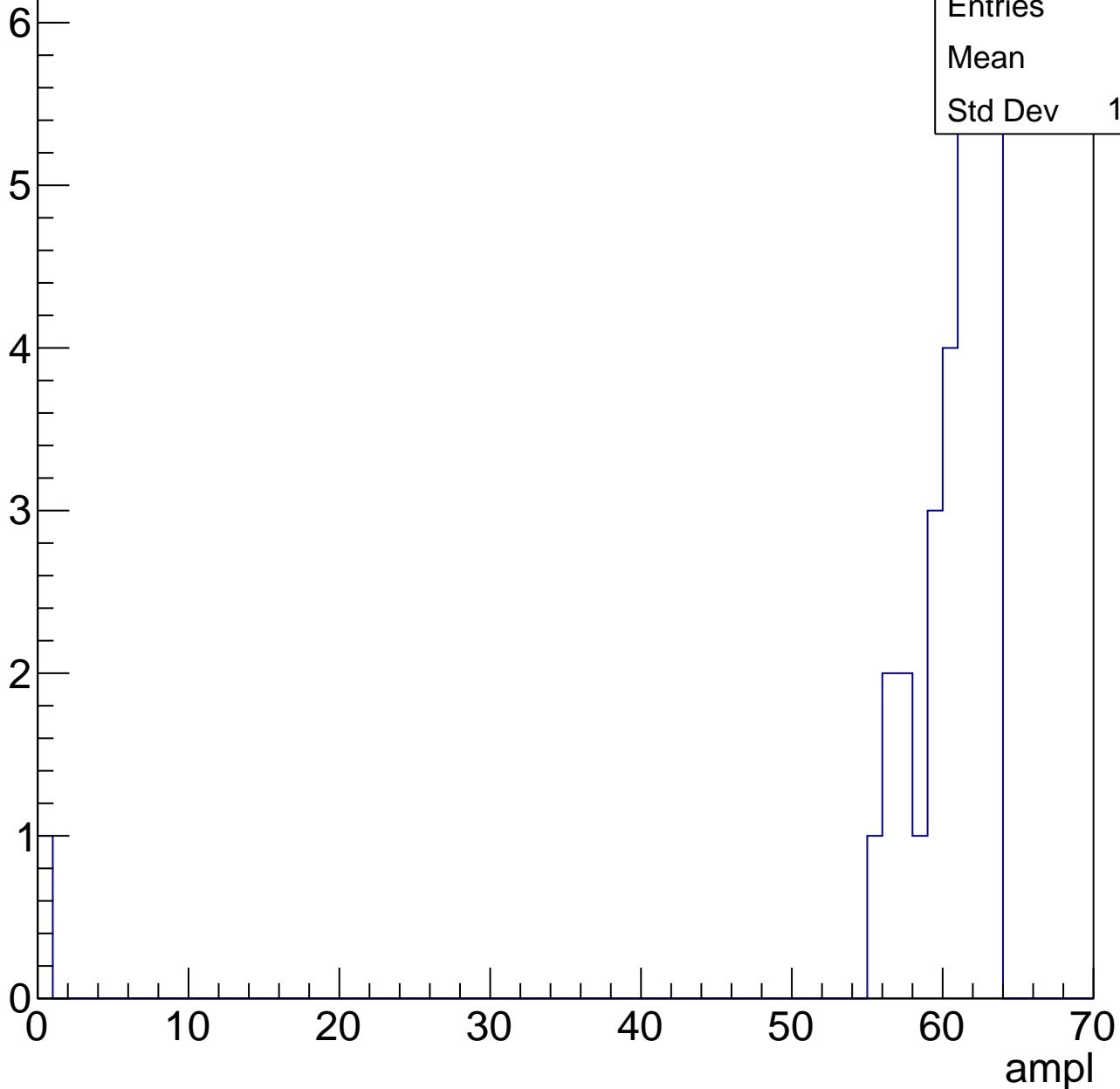


# B0L001S, U10-ch3, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	32
Mean	58.5
Std Dev	10.74



# B0L001S, U10-ch3, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch3, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L001S, U10-ch4, adc0

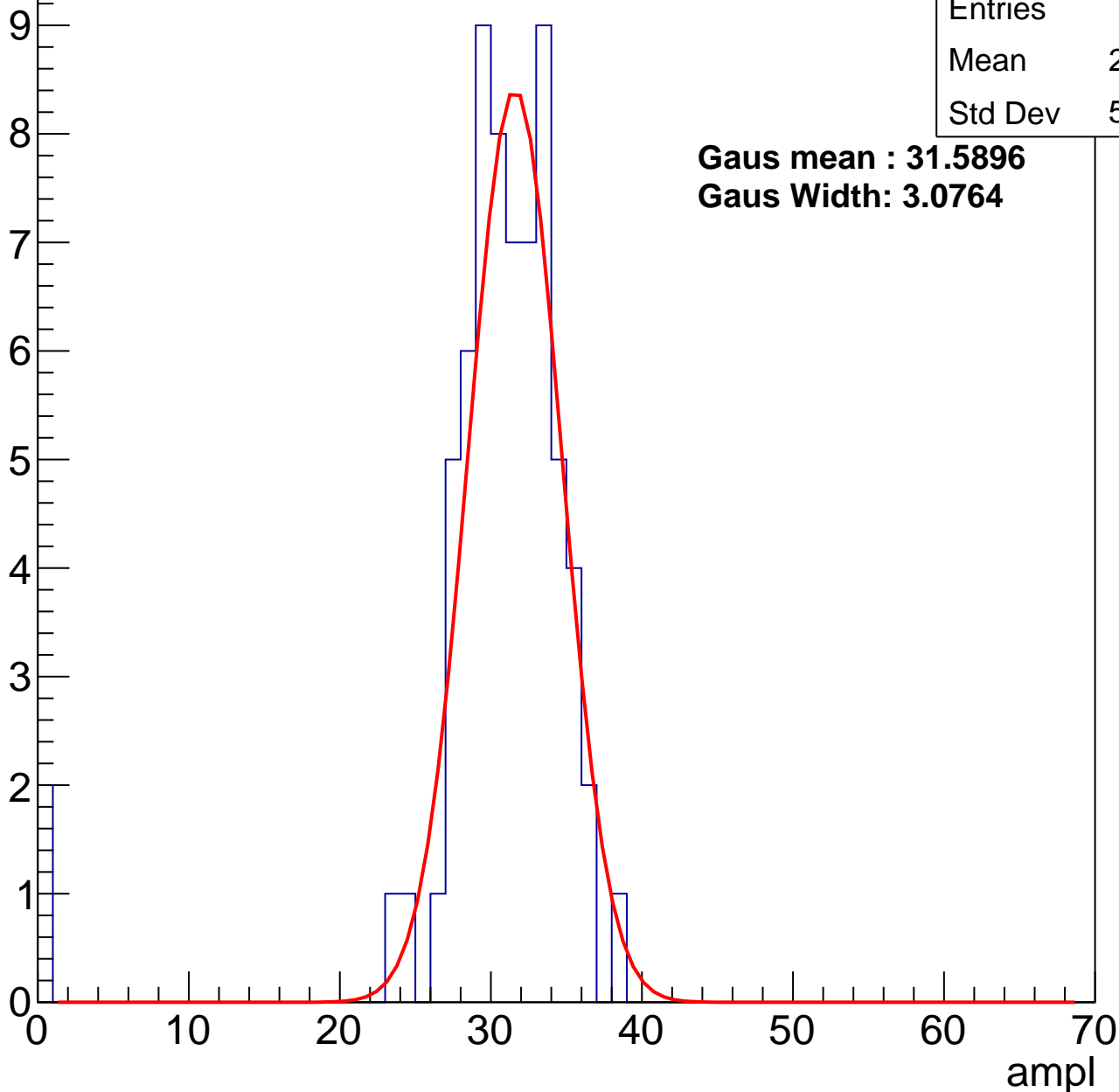
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	29.93
Std Dev	5.954

**Gaus mean : 31.5896**

**Gaus Width: 3.0764**



# B0L001S, U10-ch4, adc1

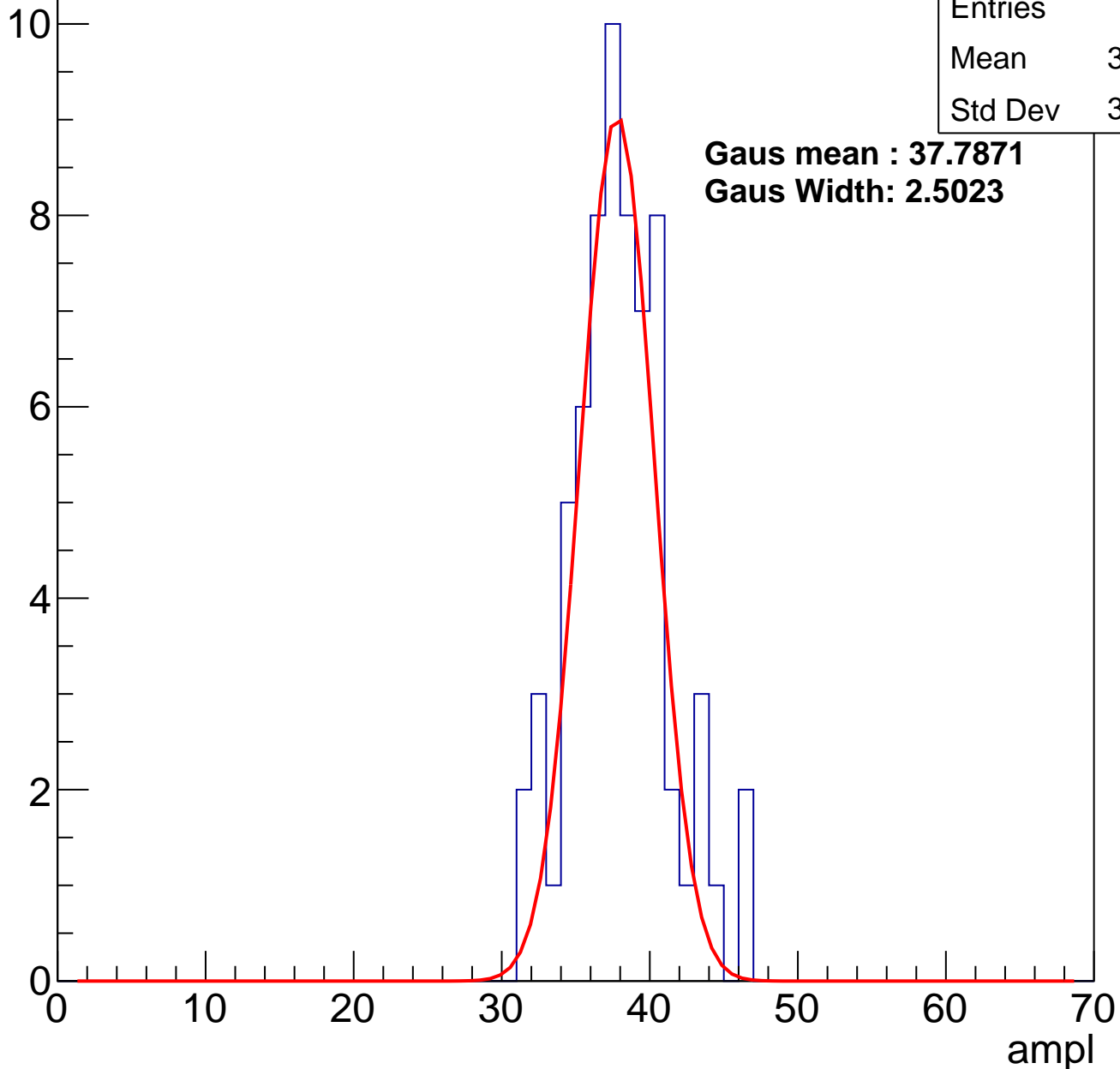
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	67
Mean	37.54
Std Dev	3.243

**Gaus mean : 37.7871**

**Gaus Width: 2.5023**

Entry



# B0L001S, U10-ch4, adc2

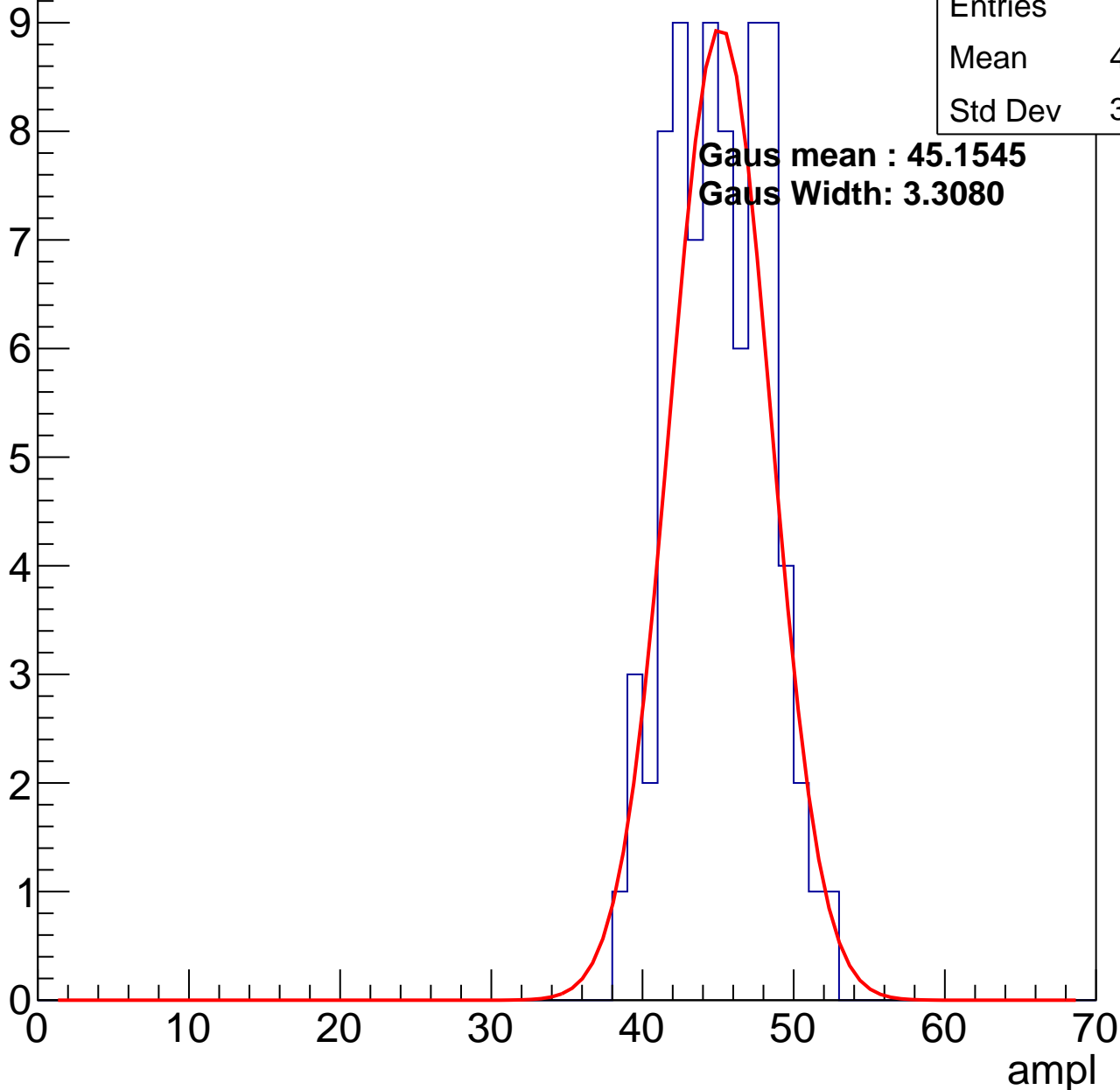
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	79
Mean	44.66
Std Dev	3.113

**Gaus mean : 45.1545**

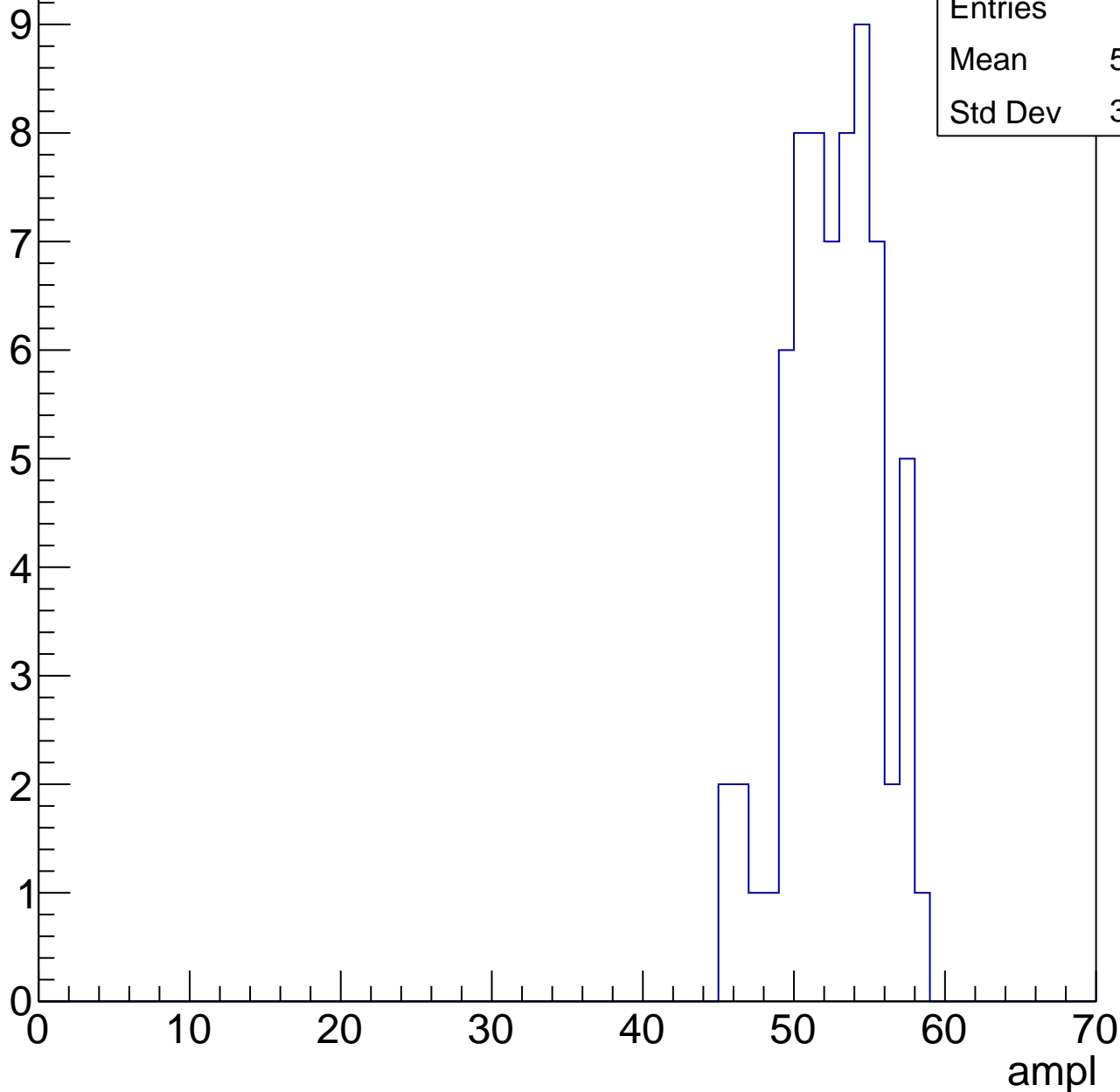
**Gaus Width: 3.3080**



# B0L001S, U10-ch4, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



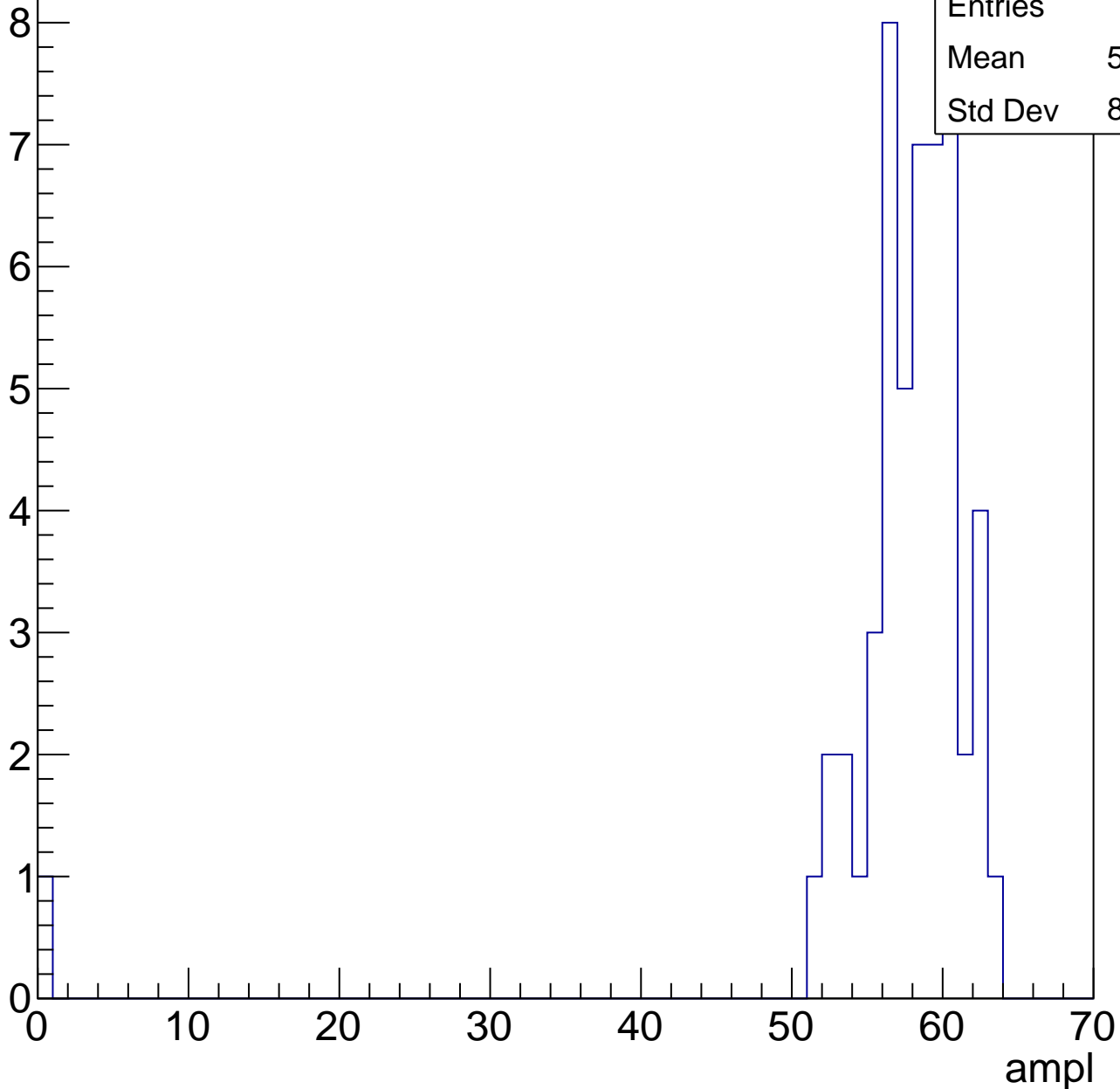
Entries	67
Mean	52.13
Std Dev	3.002

# B0L001S, U10-ch4, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	56.63
Std Dev	8.394



# B0L001S, U10-ch4, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

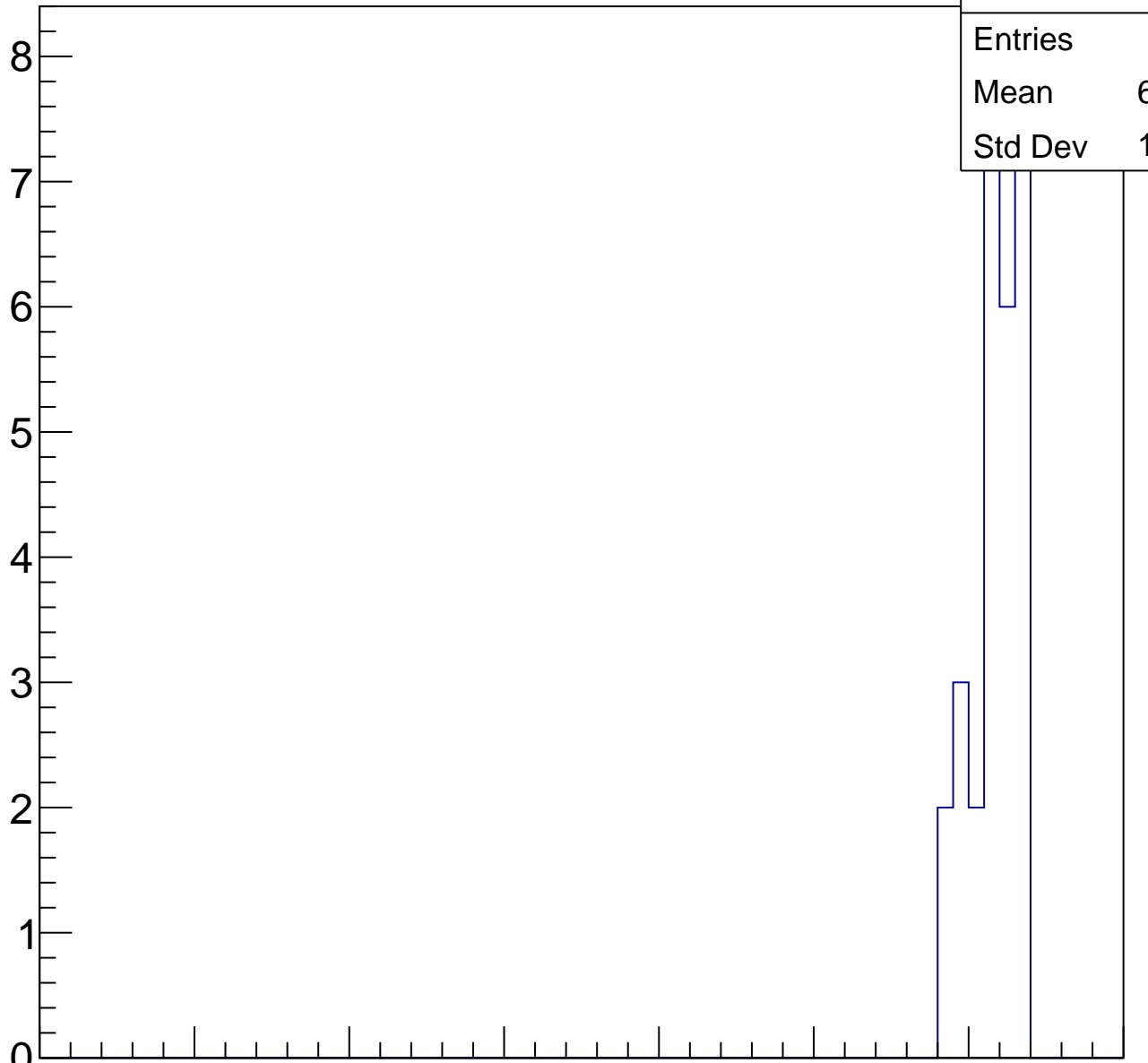
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	29
Mean	61.28
Std Dev	1.529

ampl

0 10 20 30 40 50 60 70



# B0L001S, U10-ch4, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch4, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U10-ch5, adc0

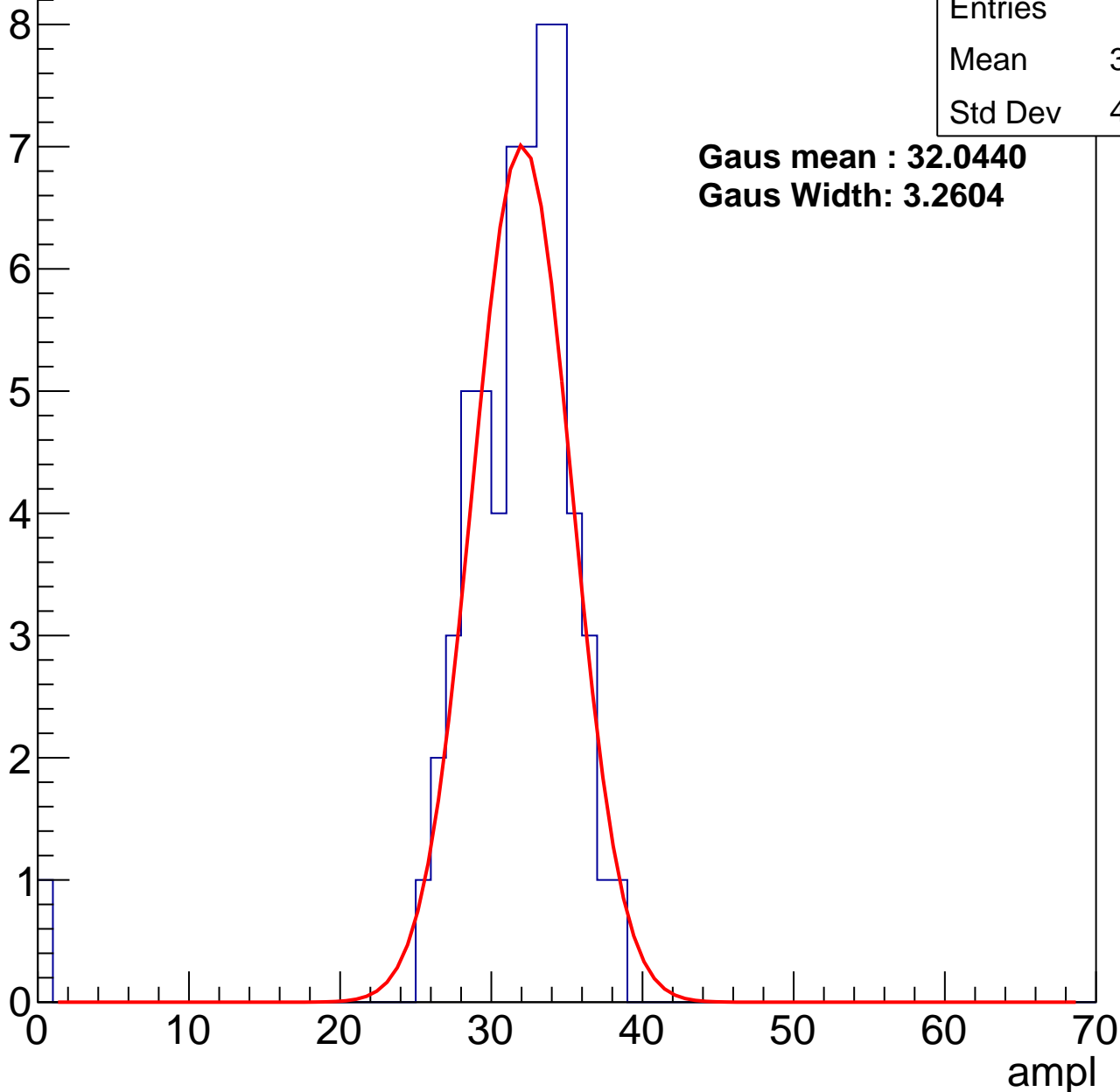
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	31.05
Std Dev	4.998

**Gaus mean : 32.0440**

**Gaus Width: 3.2604**



# B0L001S, U10-ch5, adc1

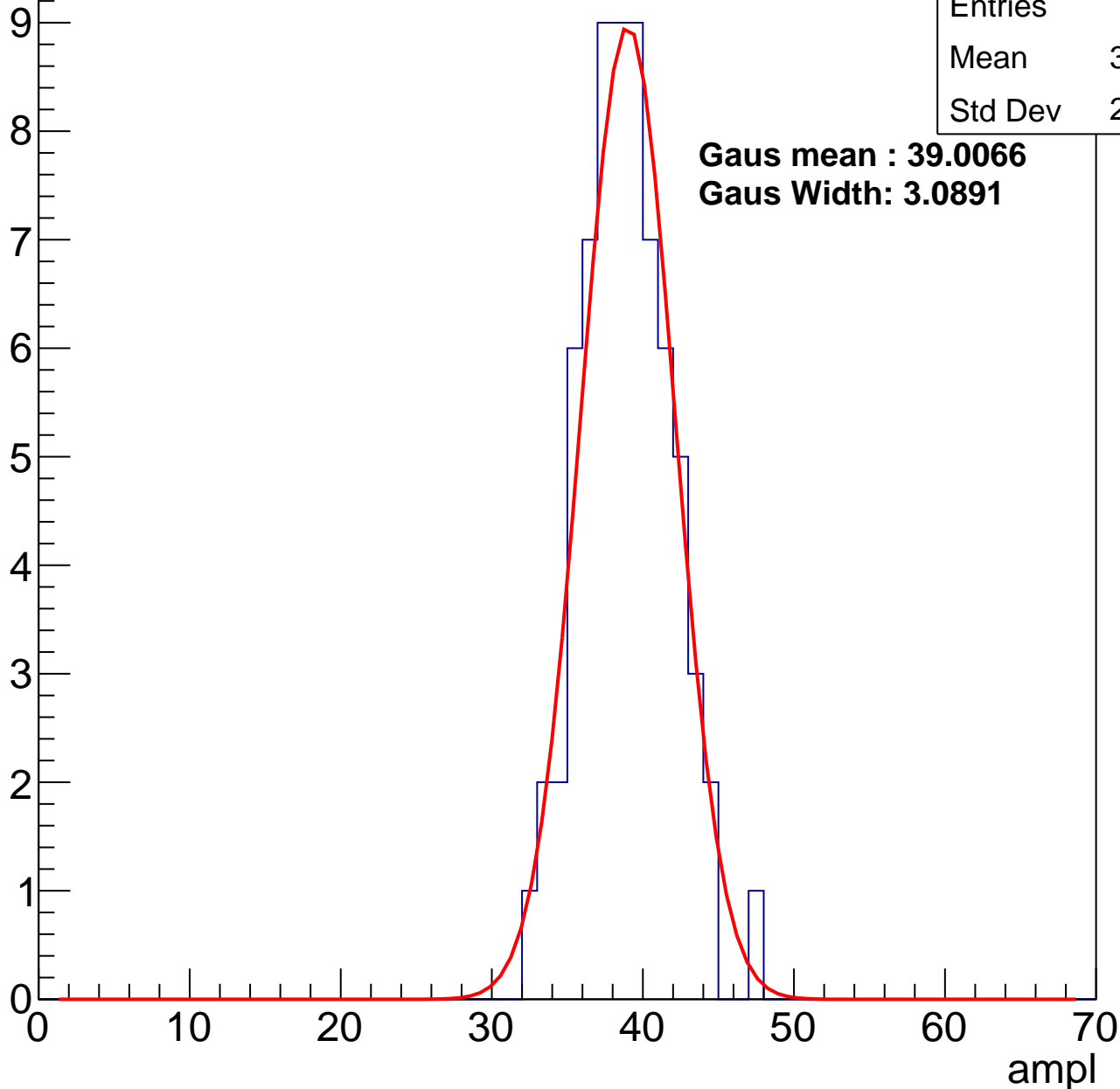
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	38.46
Std Dev	2.932

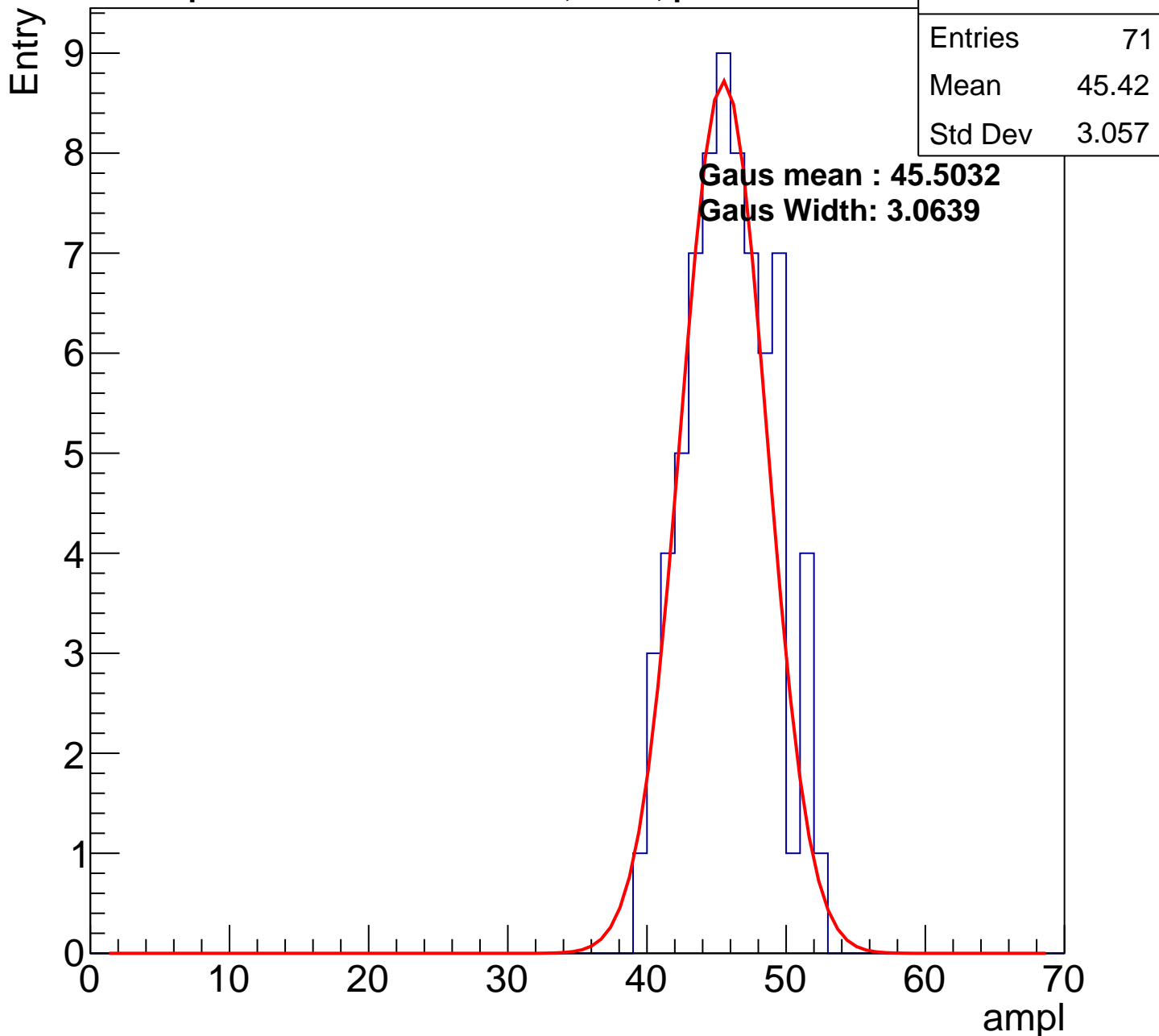
**Gaus mean : 39.0066**

**Gaus Width: 3.0891**



# B0L001S, U10-ch5, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

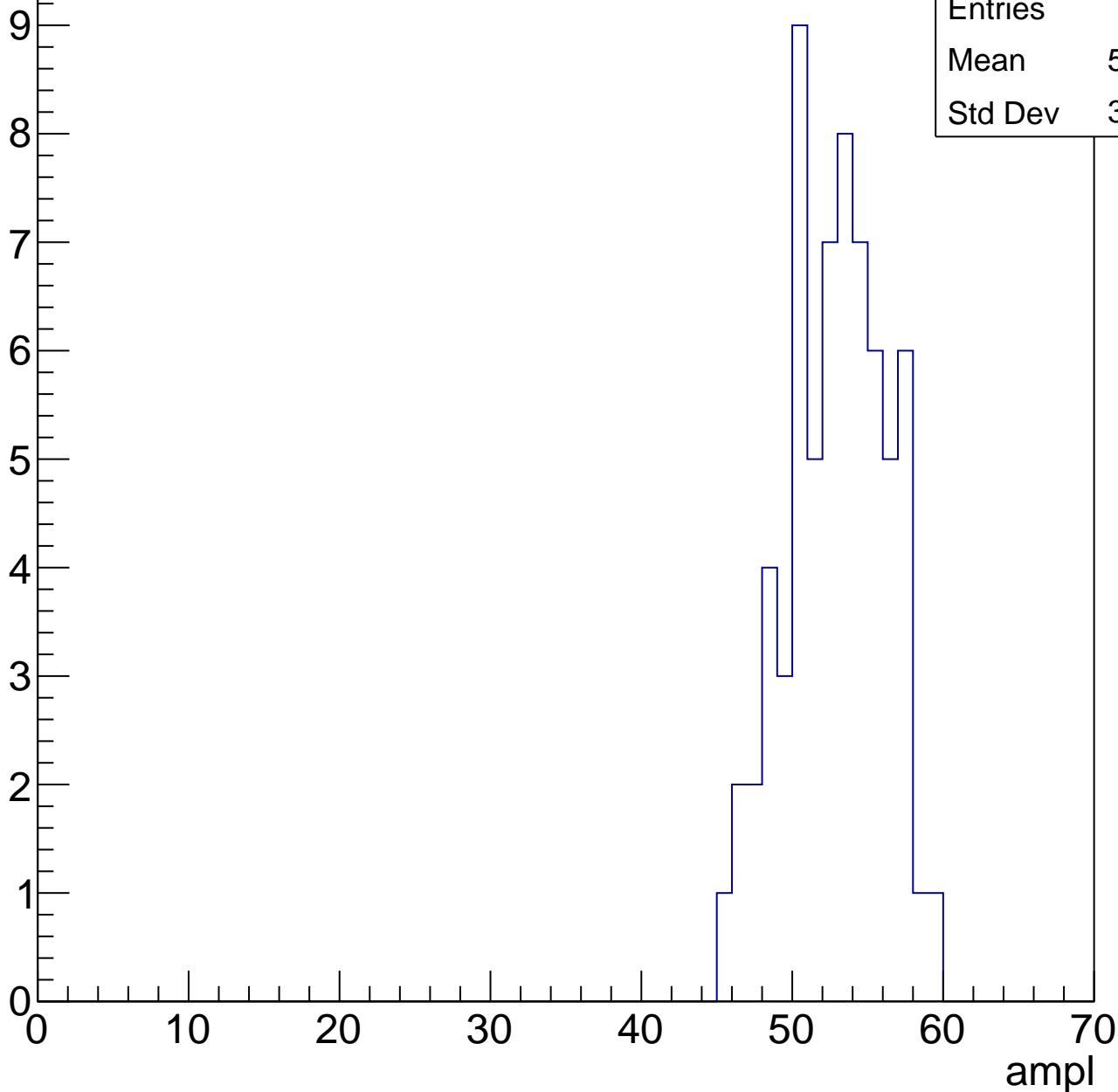


# B0L001S, U10-ch5, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	52.39
Std Dev	3.227

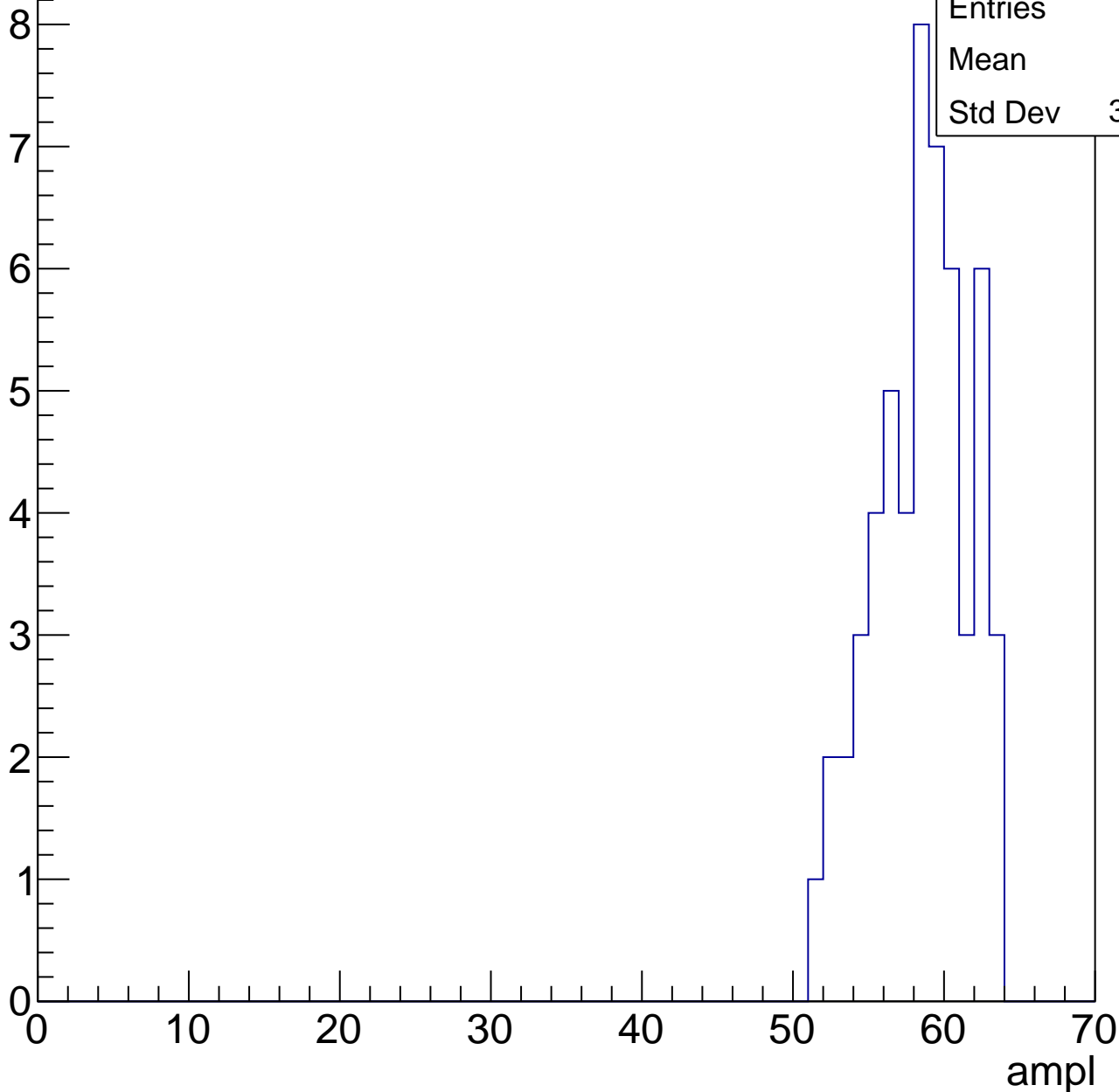


# B0L001S, U10-ch5, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	58
Std Dev	3.067

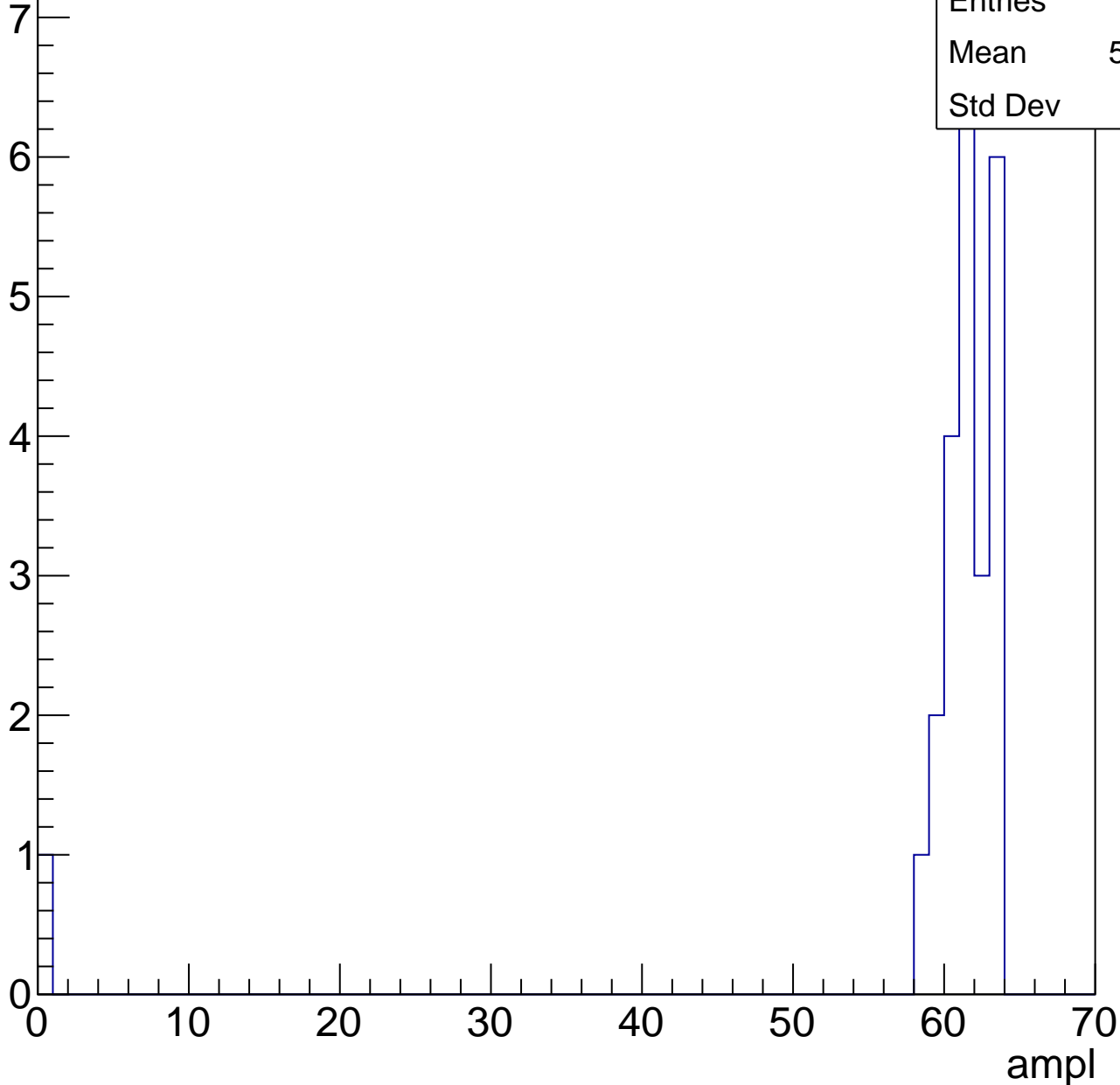


# B0L001S, U10-ch5, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	24
Mean	58.62
Std Dev	12.3



# B0L001S, U10-ch5, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch5, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U10-ch6, adc0

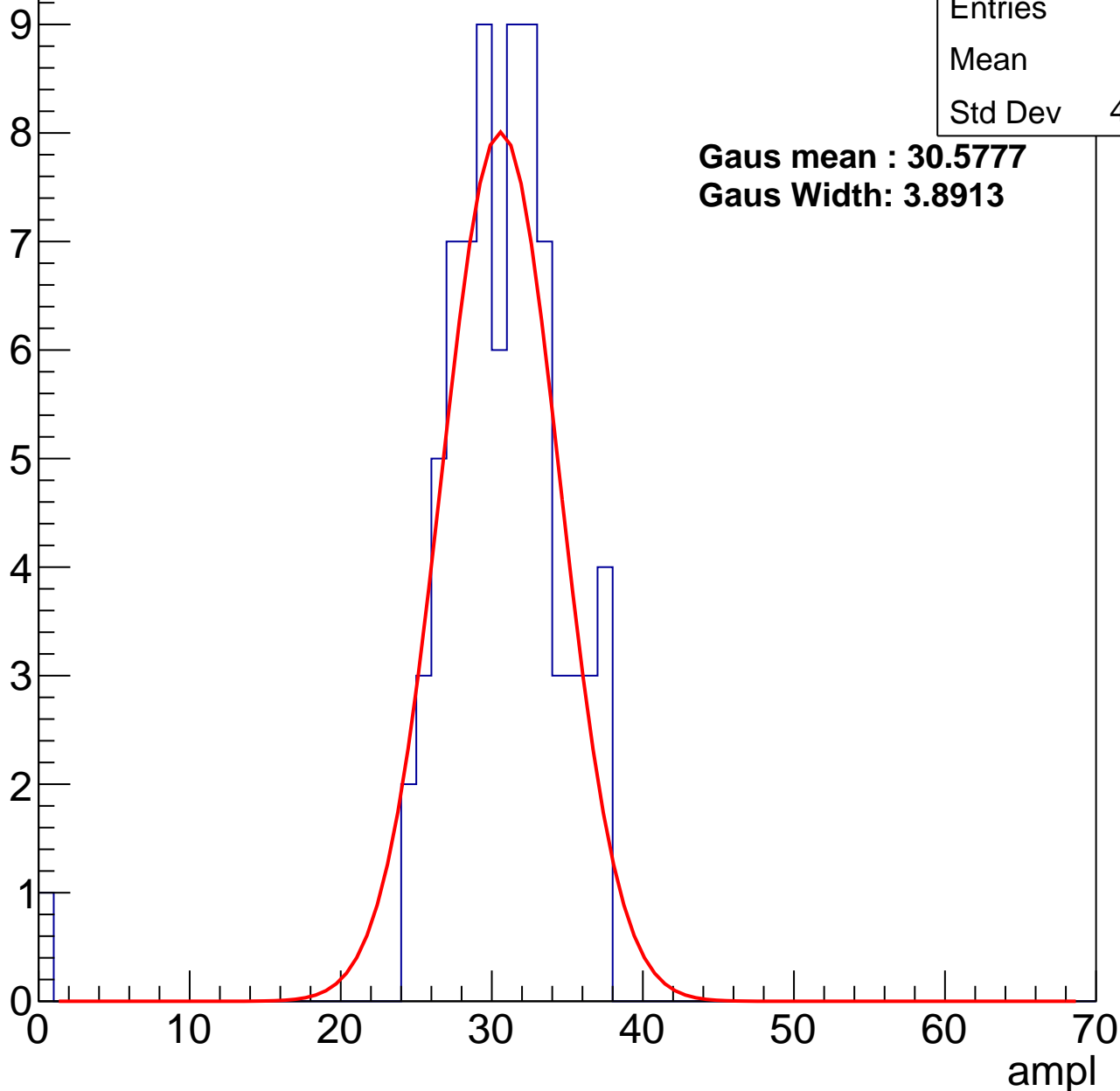
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	78
Mean	30
Std Dev	4.753

**Gaus mean : 30.5777**

**Gaus Width: 3.8913**



# B0L001S, U10-ch6, adc1

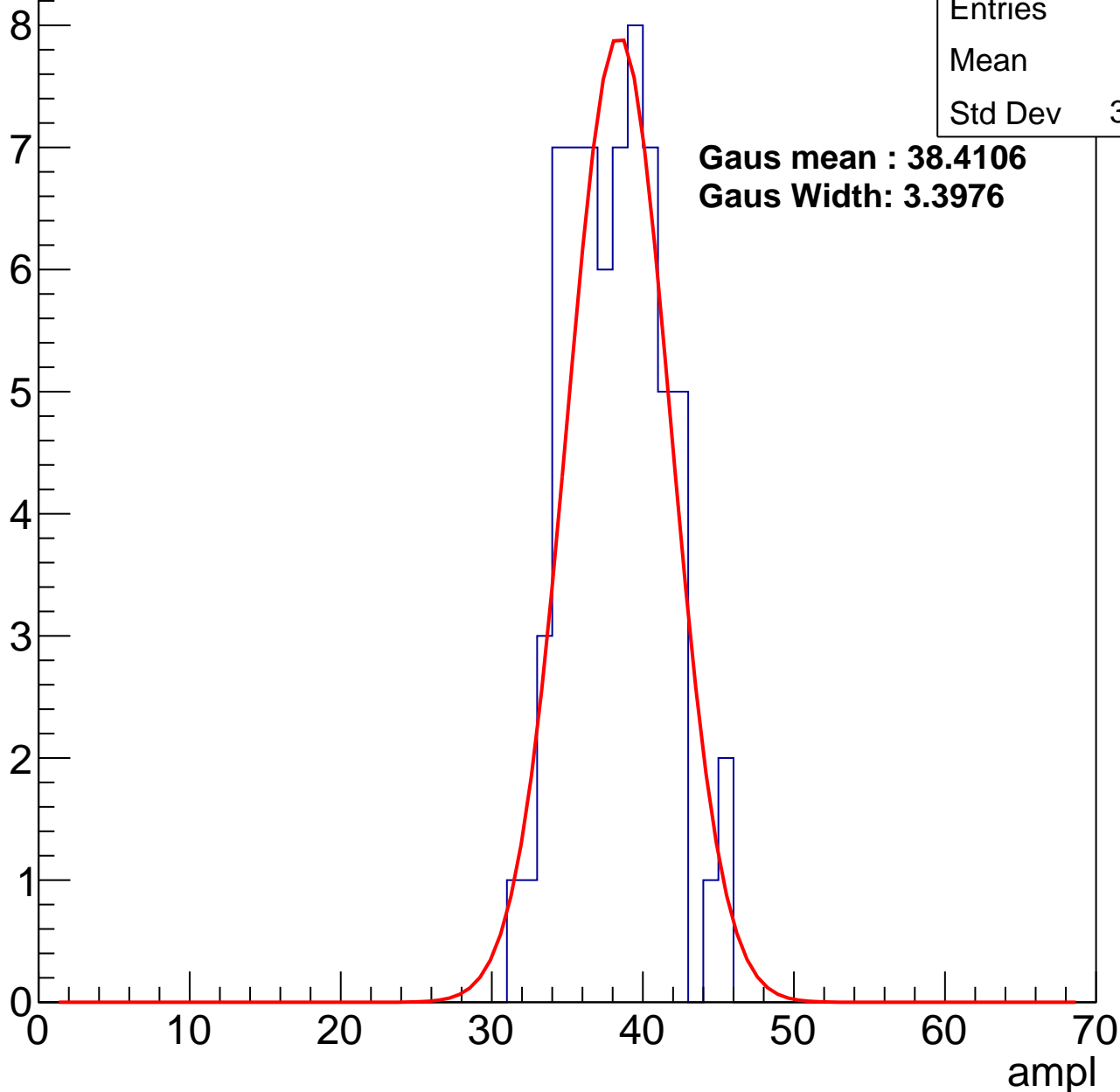
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	37.7
Std Dev	3.134

**Gaus mean : 38.4106**

**Gaus Width: 3.3976**



# B0L001S, U10-ch6, adc2

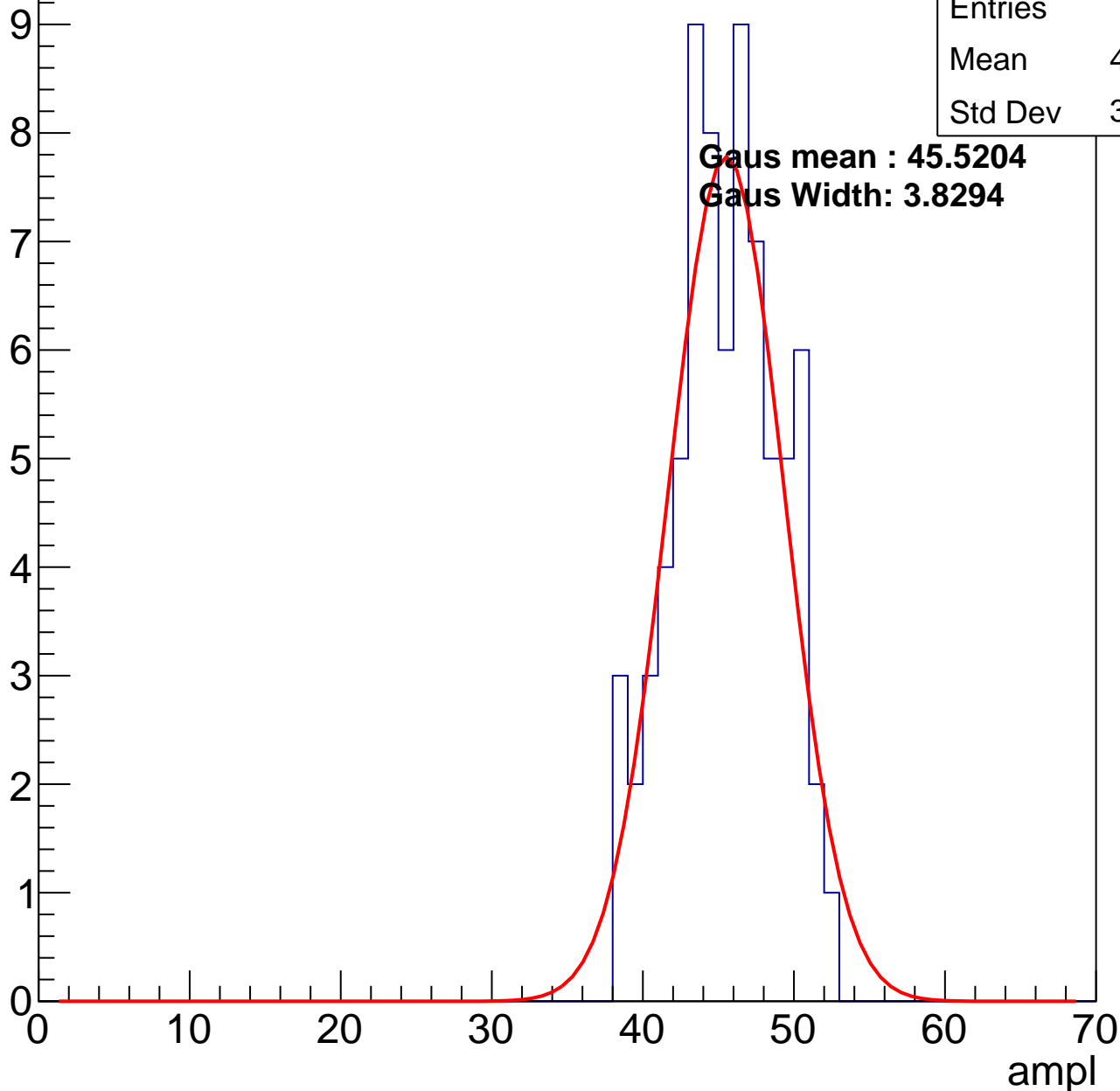
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	75
Mean	45.03
Std Dev	3.425

**Gaus mean : 45.5204**

**Gaus Width: 3.8294**

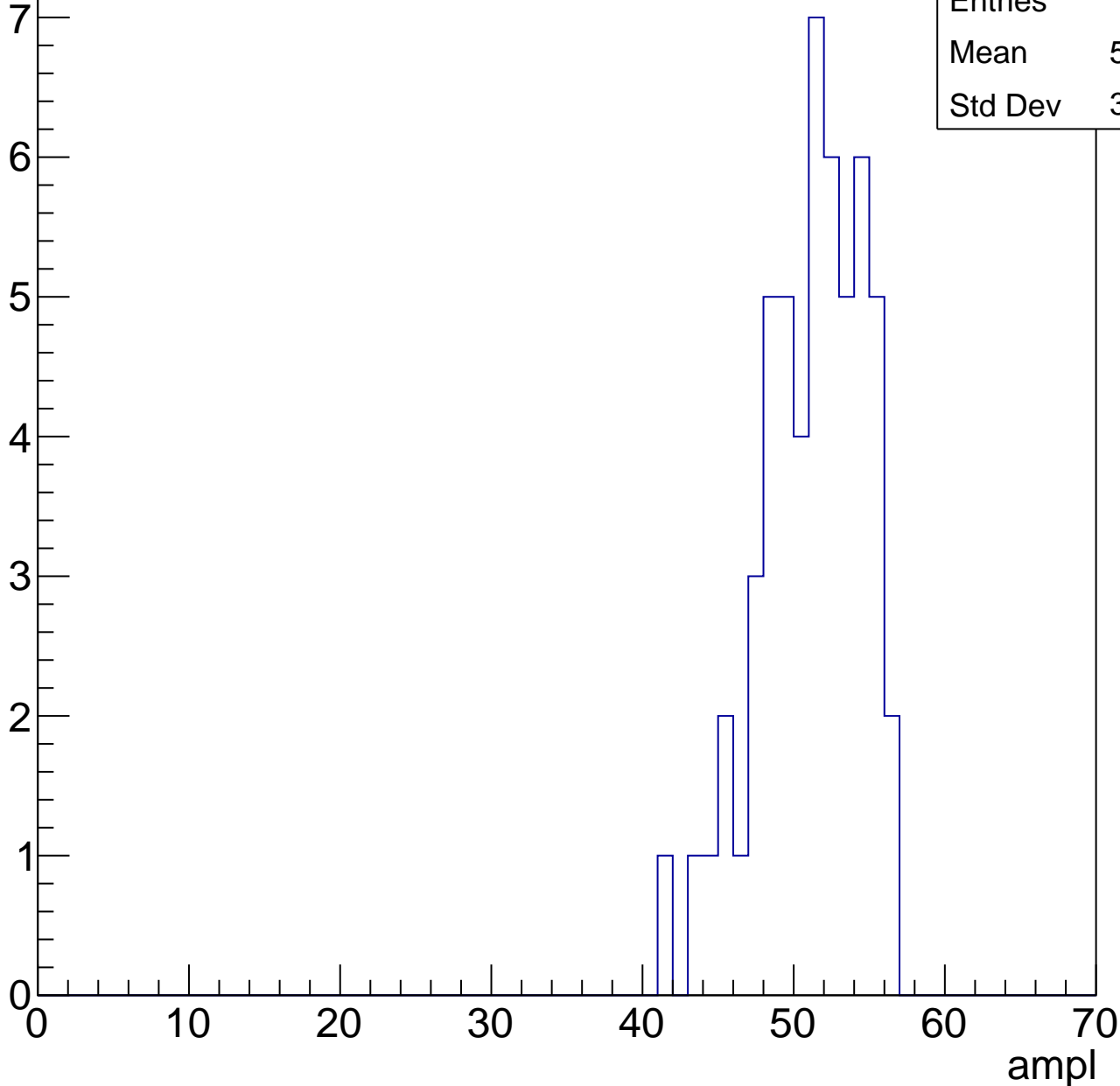


# B0L001S, U10-ch6, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	50.65
Std Dev	3.417

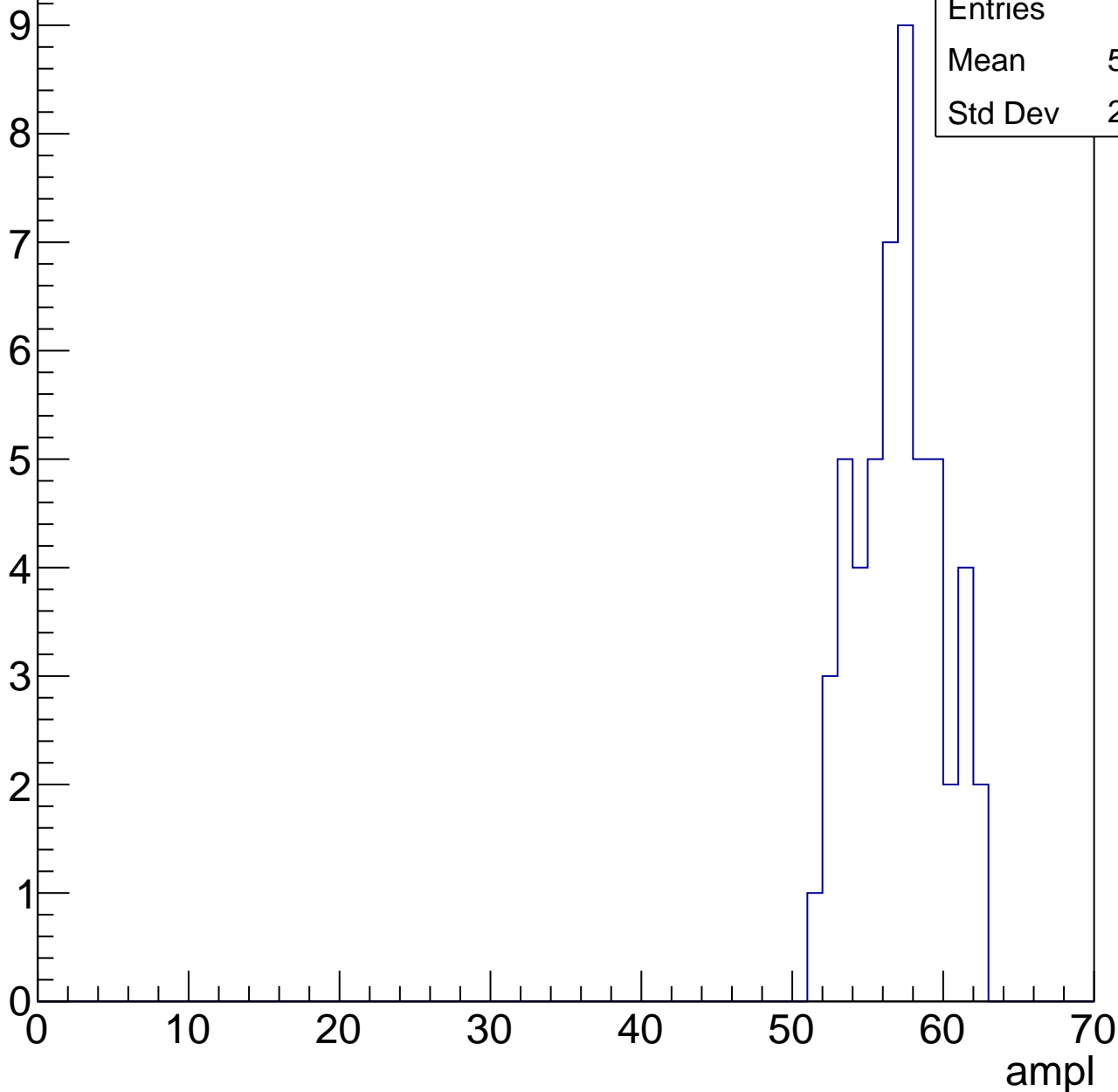


# B0L001S, U10-ch6, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	56.56
Std Dev	2.776



# B0L001S, U10-ch6, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

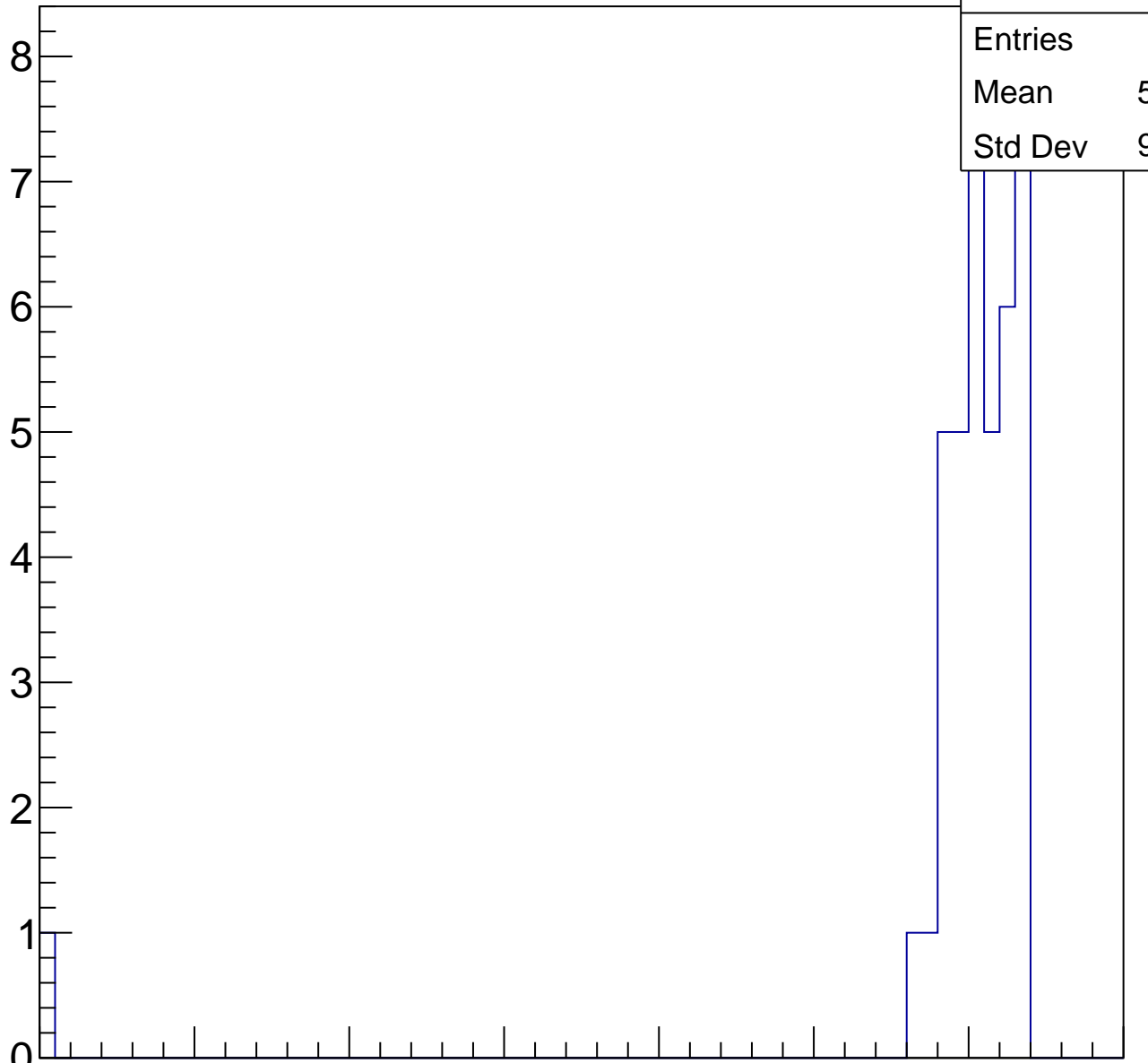
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	40
Mean	58.98
Std Dev	9.629

ampl

0 10 20 30 40 50 60 70



# B0L001S, U10-ch6, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch6, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U10-ch7, adc0

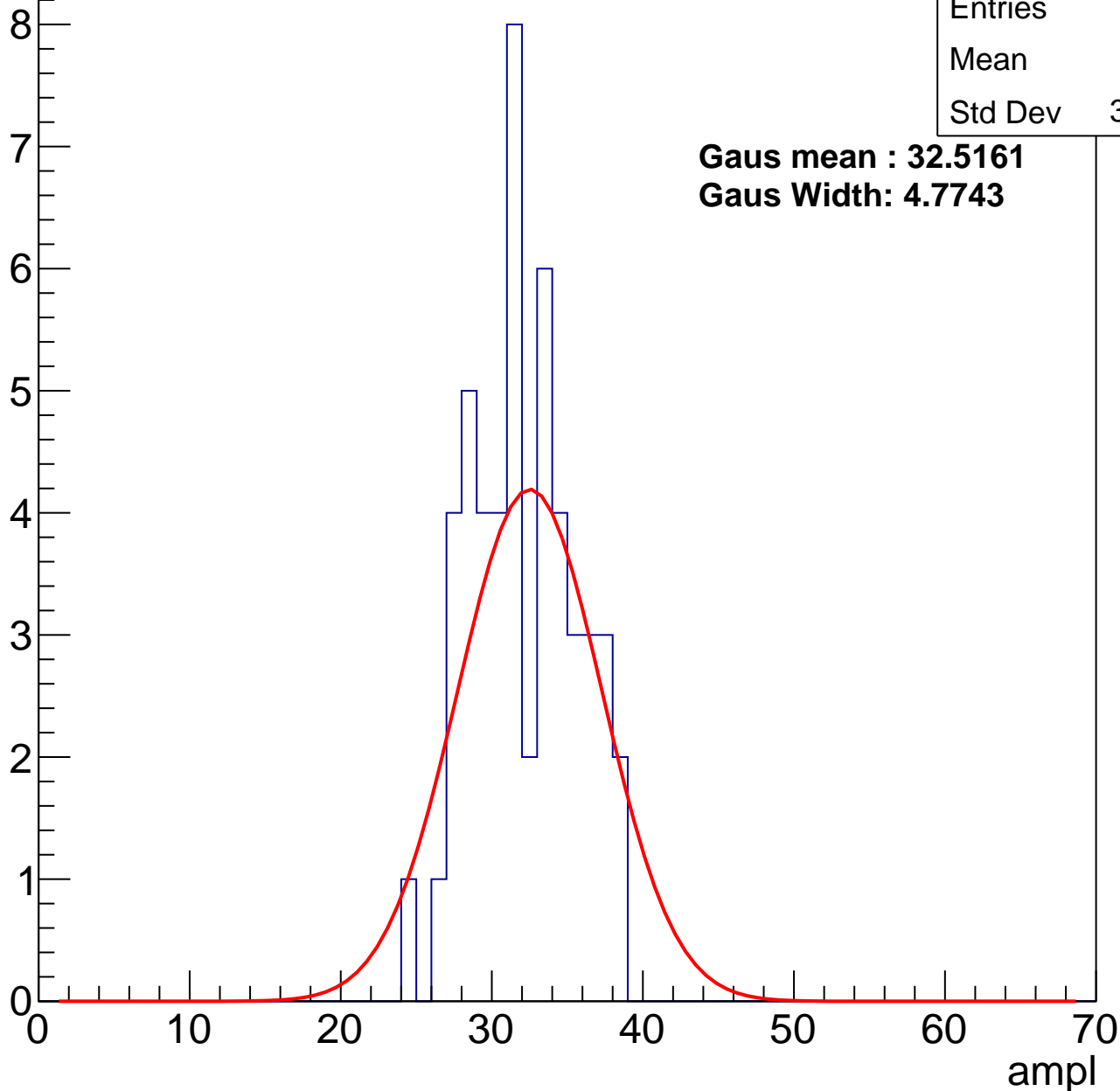
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	50
Mean	31.6
Std Dev	3.394

**Gaus mean : 32.5161**

**Gaus Width: 4.7743**



# B0L001S, U10-ch7, adc1

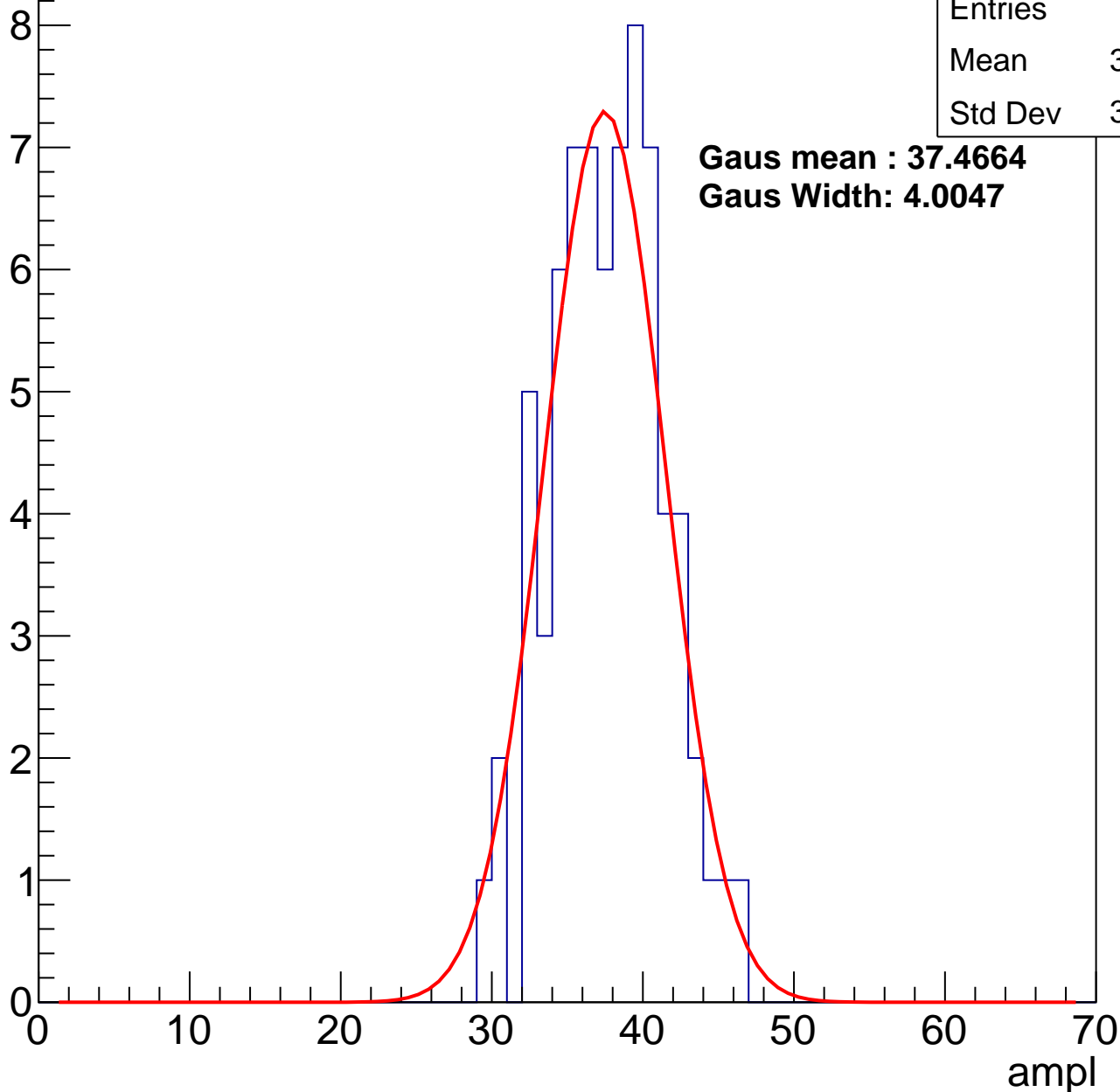
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	37.25
Std Dev	3.635

**Gaus mean : 37.4664**

**Gaus Width: 4.0047**



# B0L001S, U10-ch7, adc2

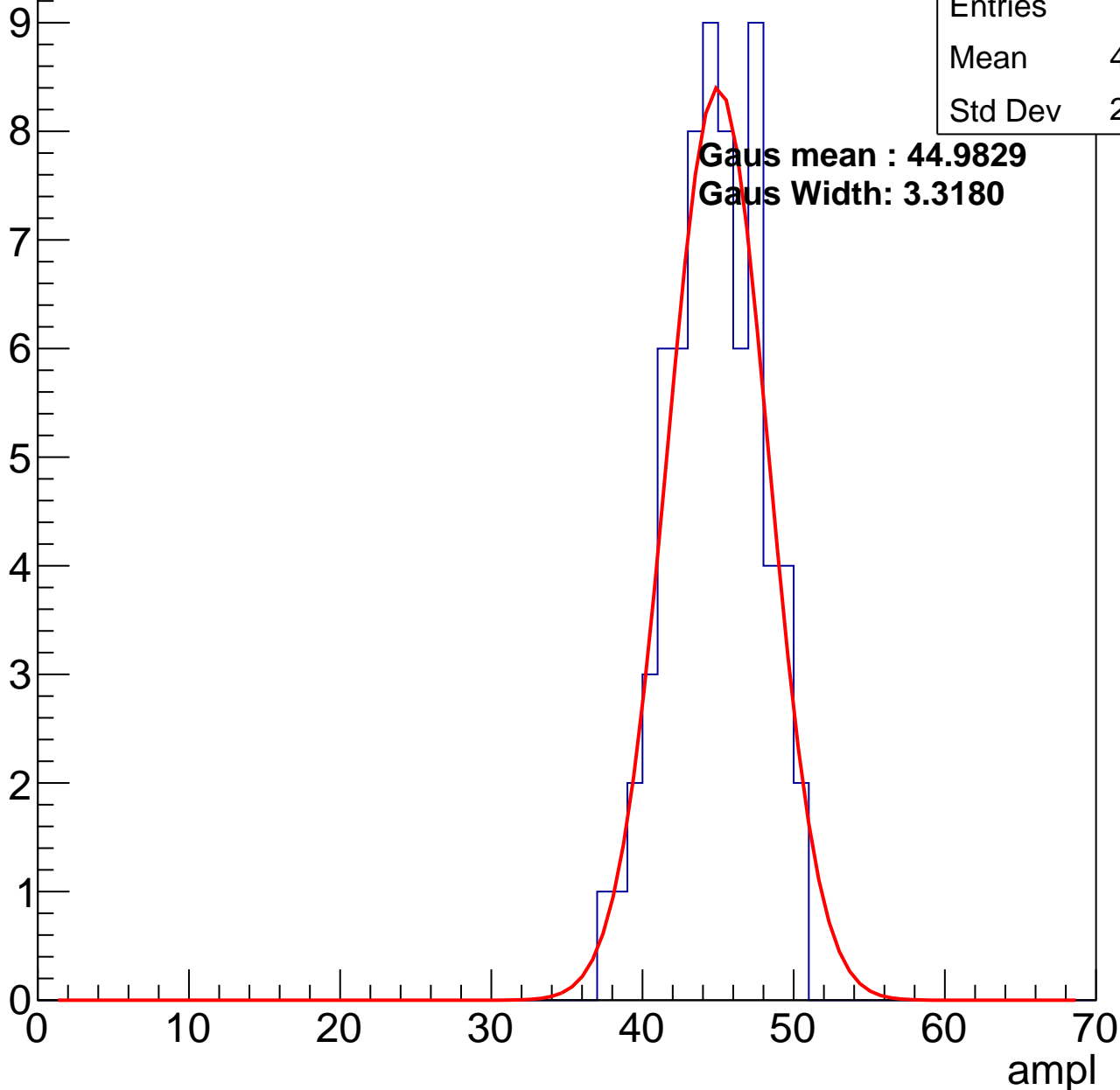
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	44.32
Std Dev	2.976

**Gaus mean : 44.9829**

**Gaus Width: 3.3180**

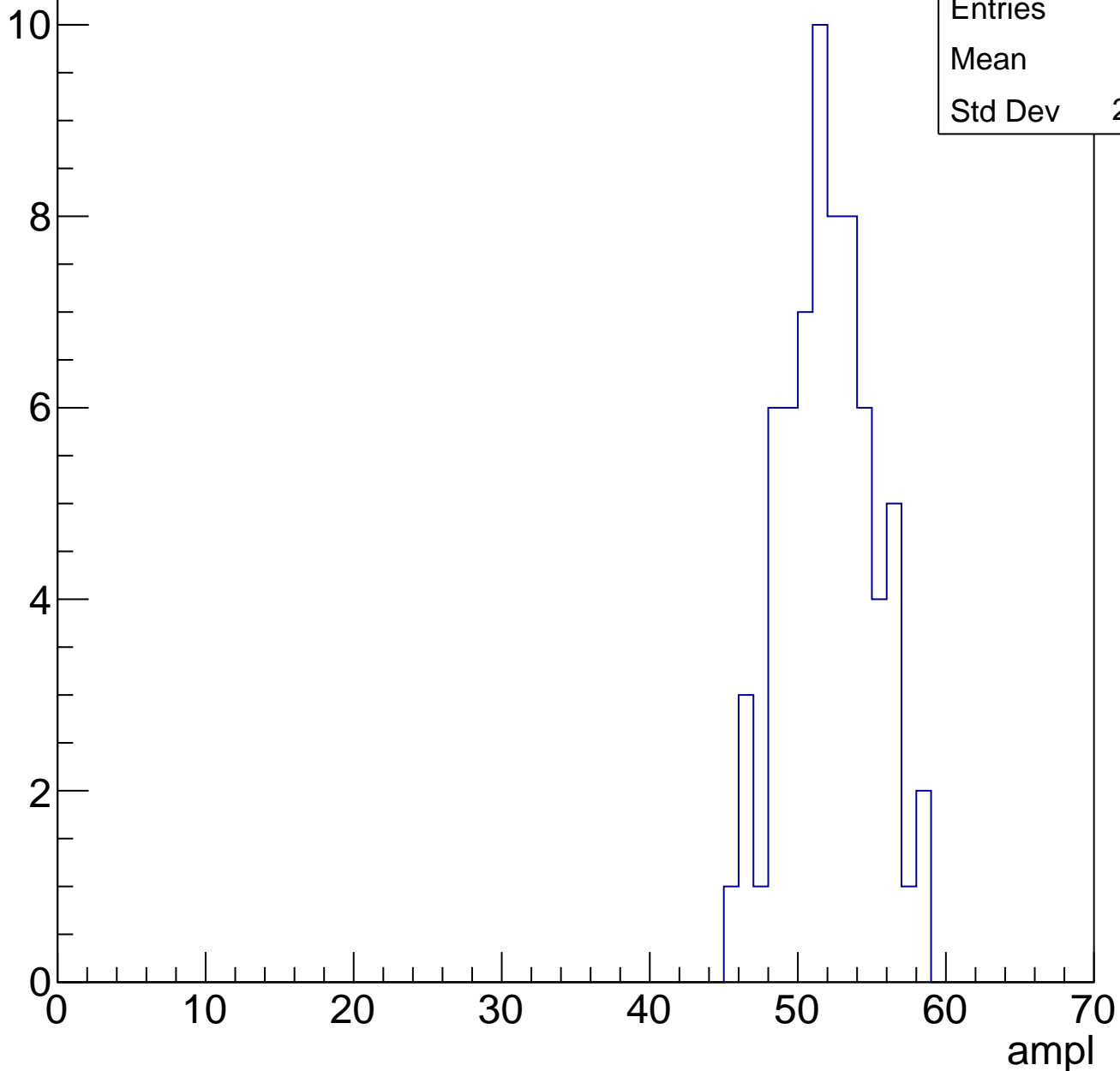


# B0L001S, U10-ch7, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	68
Mean	51.6
Std Dev	2.981

Entry

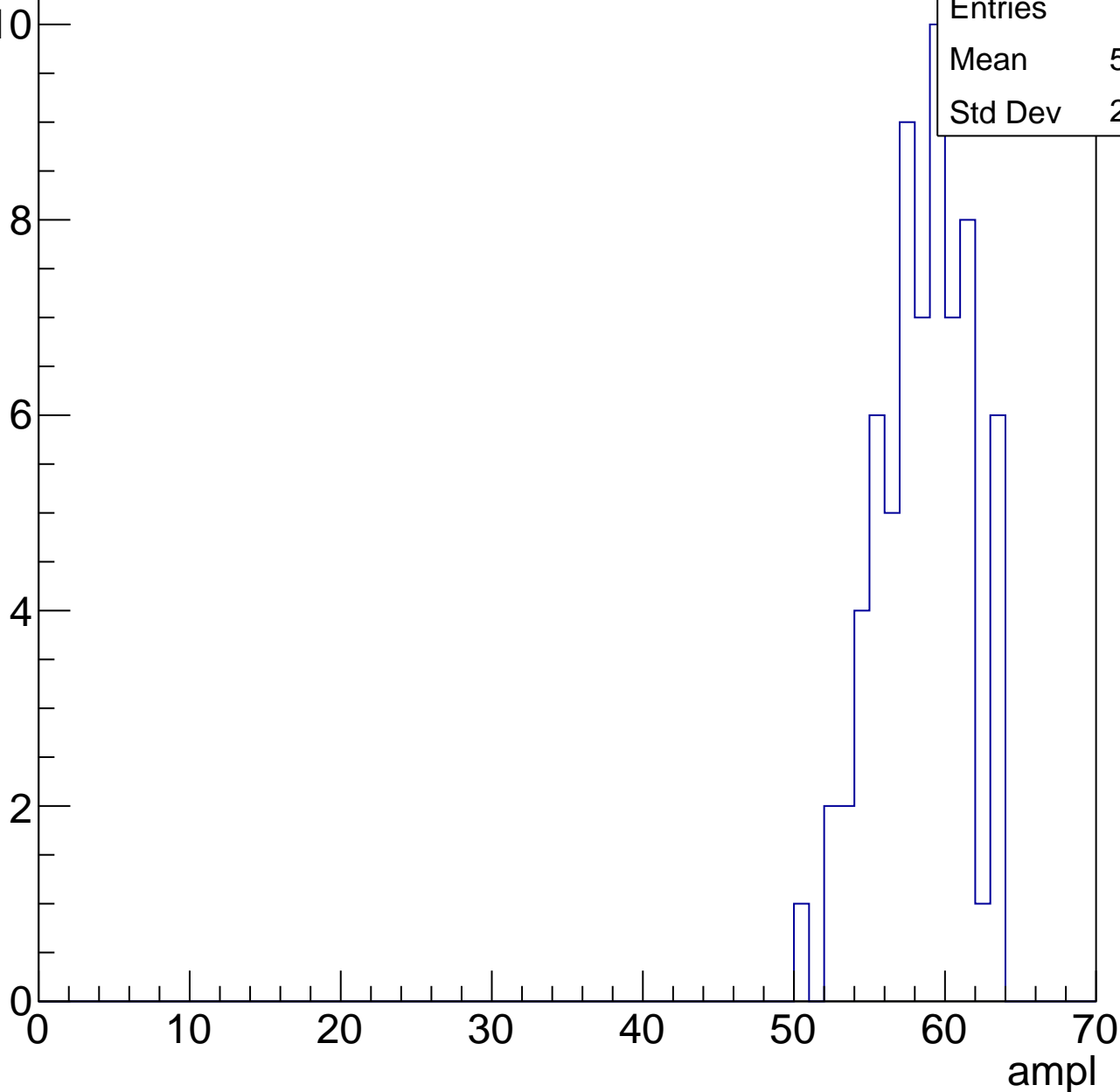


# B0L001S, U10-ch7, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	57.99
Std Dev	2.993

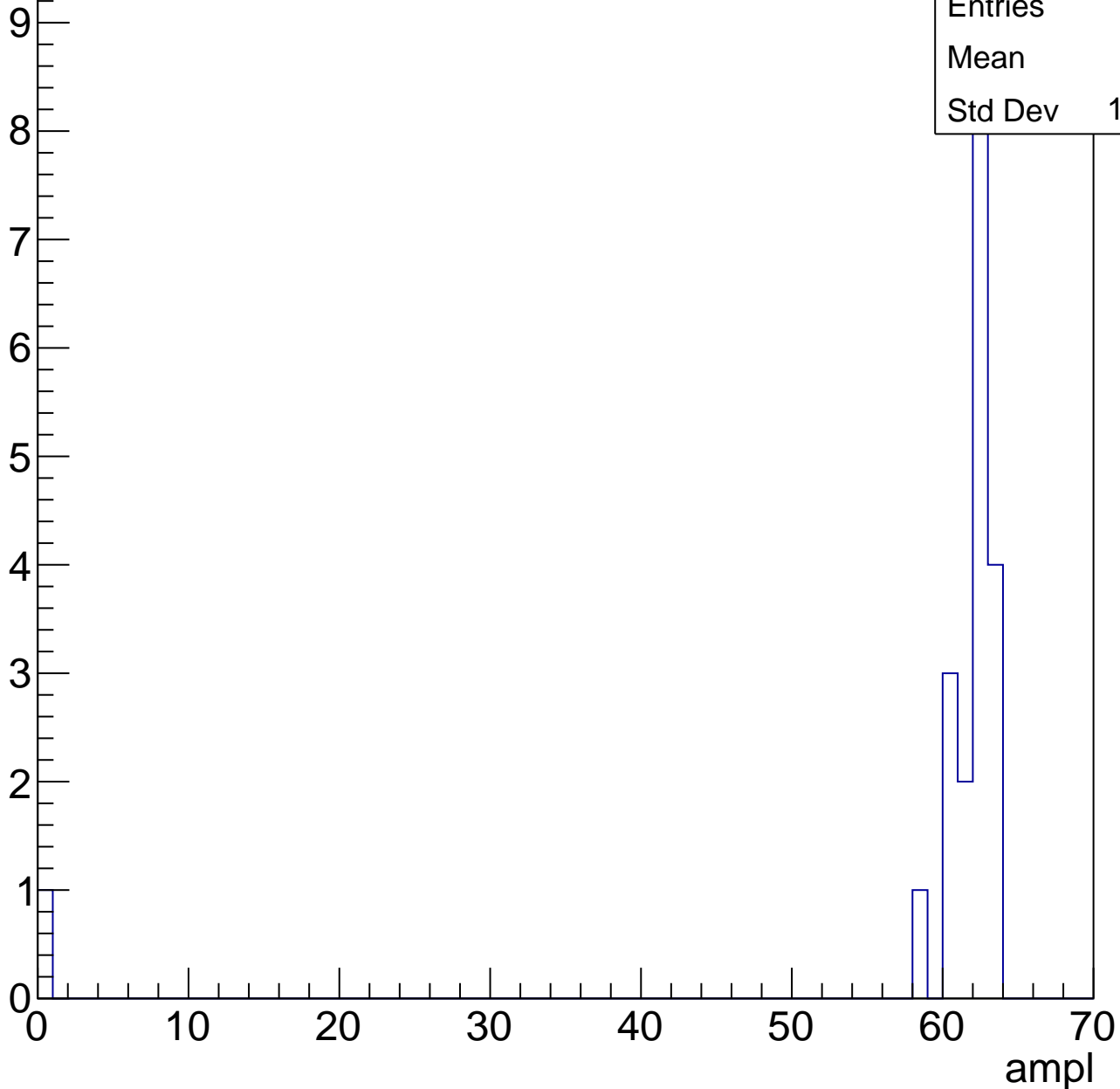


# B0L001S, U10-ch7, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	20
Mean	58.5
Std Dev	13.48



# B0L001S, U10-ch7, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U10-ch7, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U10-ch8, adc0

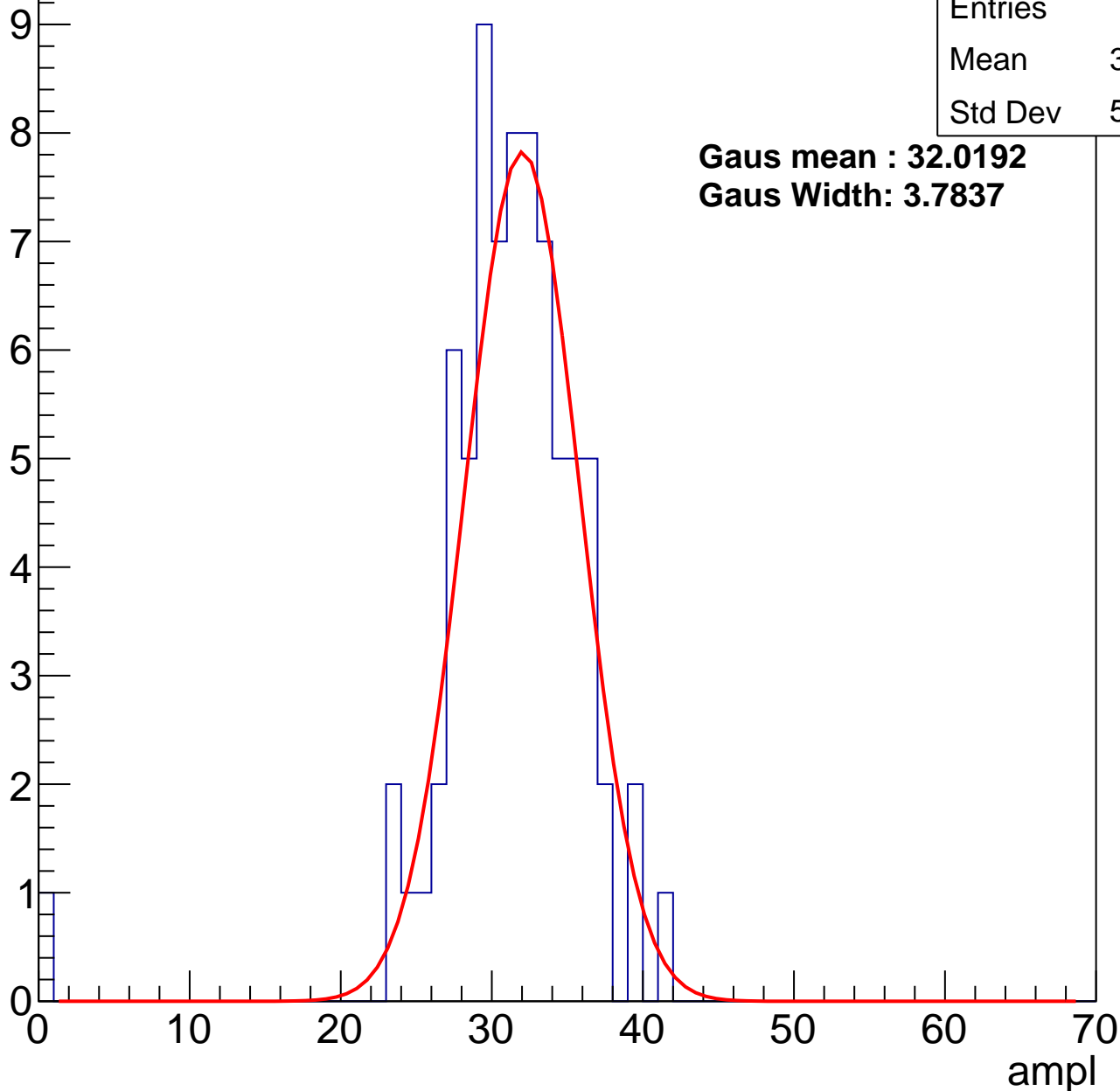
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	77
Mean	30.82
Std Dev	5.086

**Gaus mean : 32.0192**

**Gaus Width: 3.7837**



# B0L001S, U10-ch8, adc1

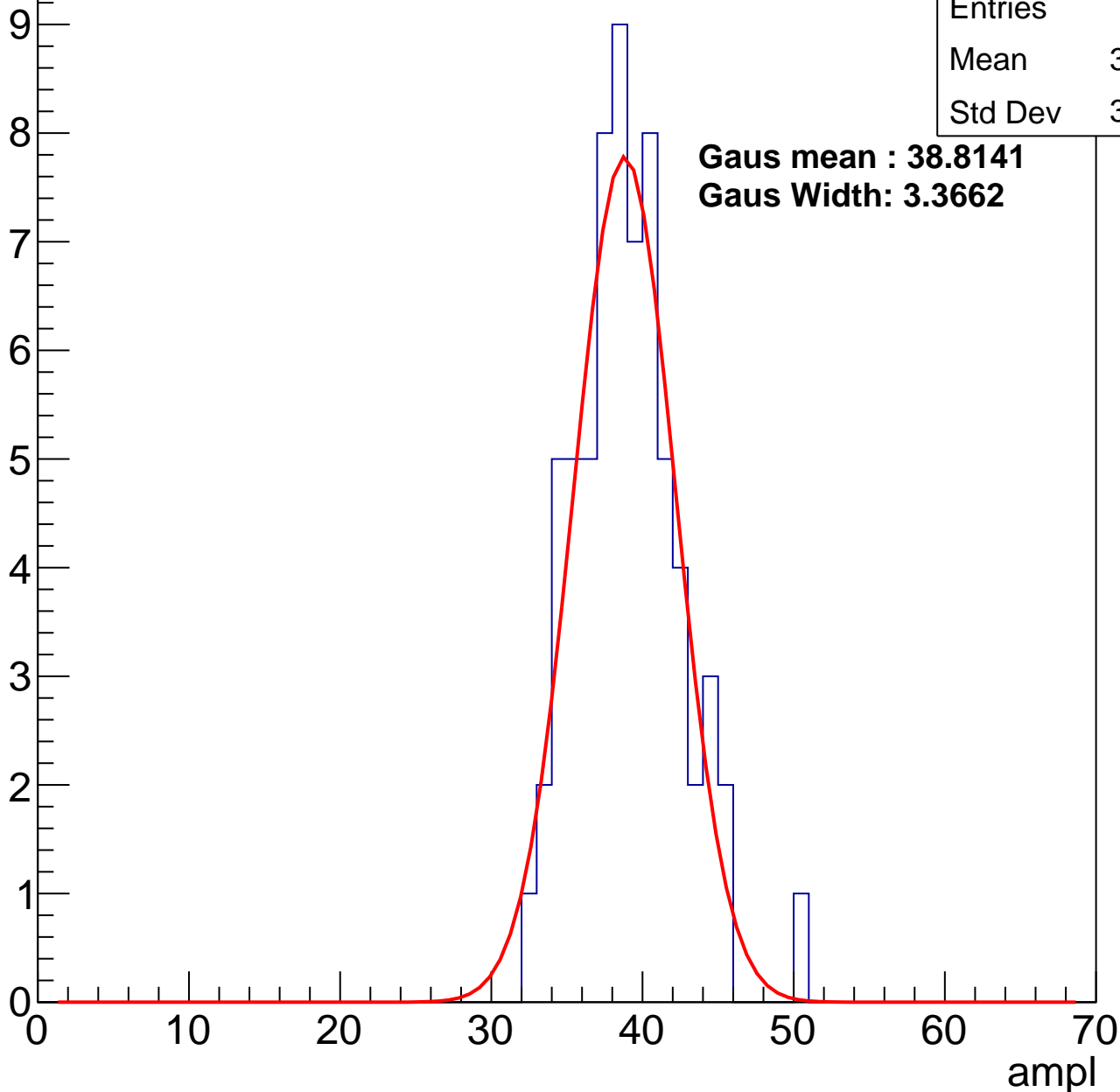
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	38.58
Std Dev	3.377

**Gaus mean : 38.8141**

**Gaus Width: 3.3662**



# B0L001S, U10-ch8, adc2

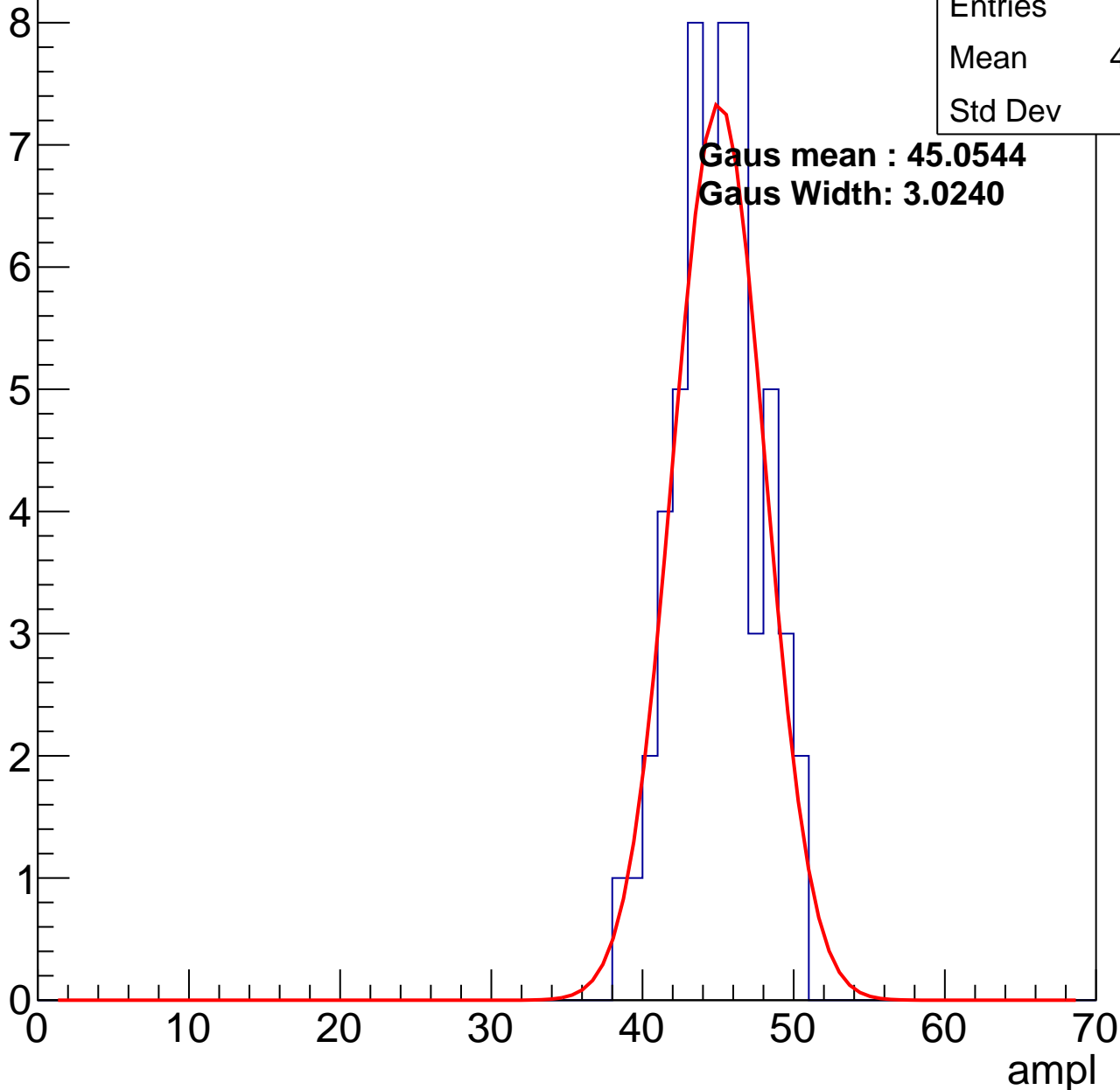
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	44.54
Std Dev	2.76

**Gaus mean : 45.0544**

**Gaus Width: 3.0240**

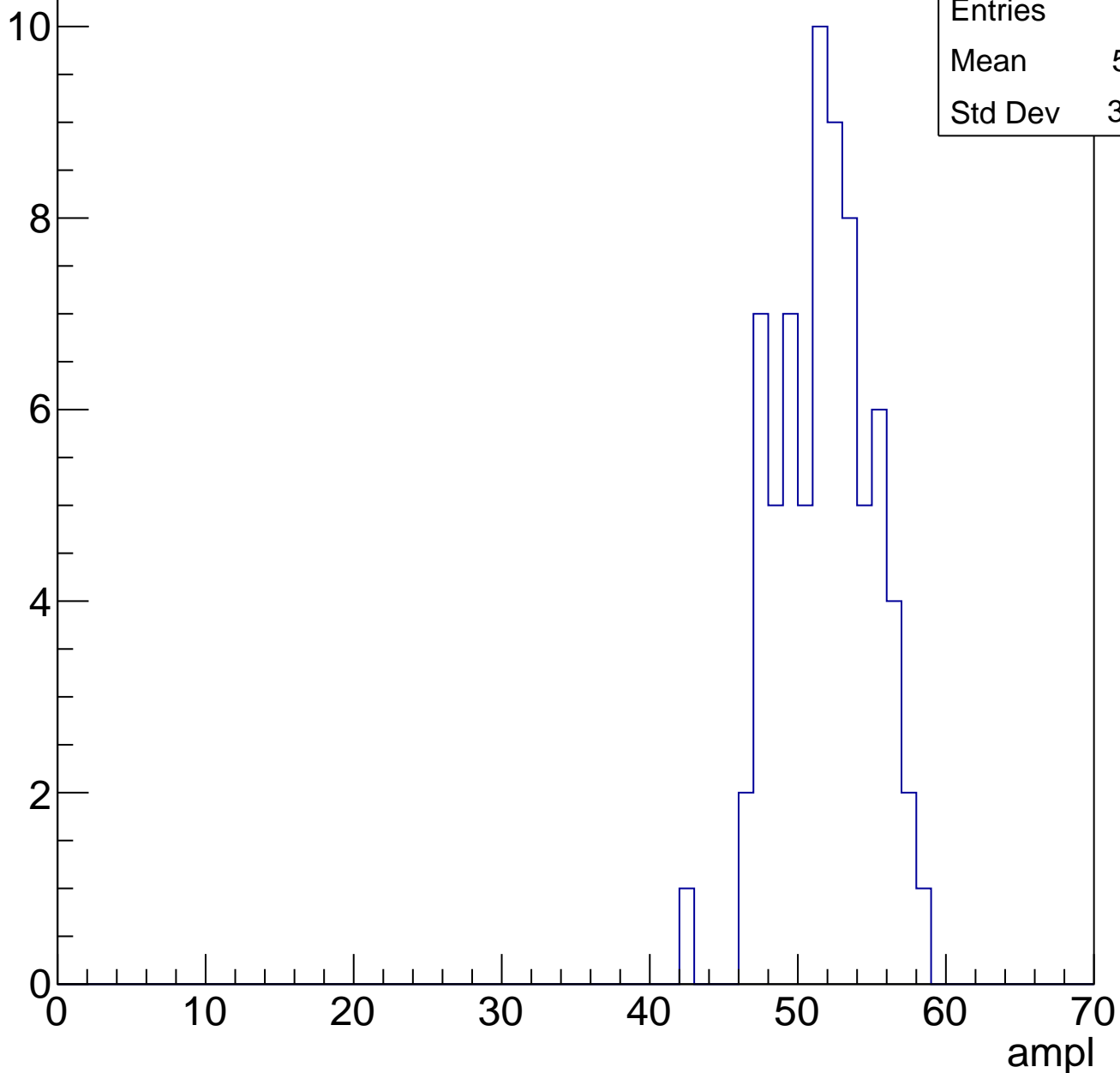


# B0L001S, U10-ch8, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

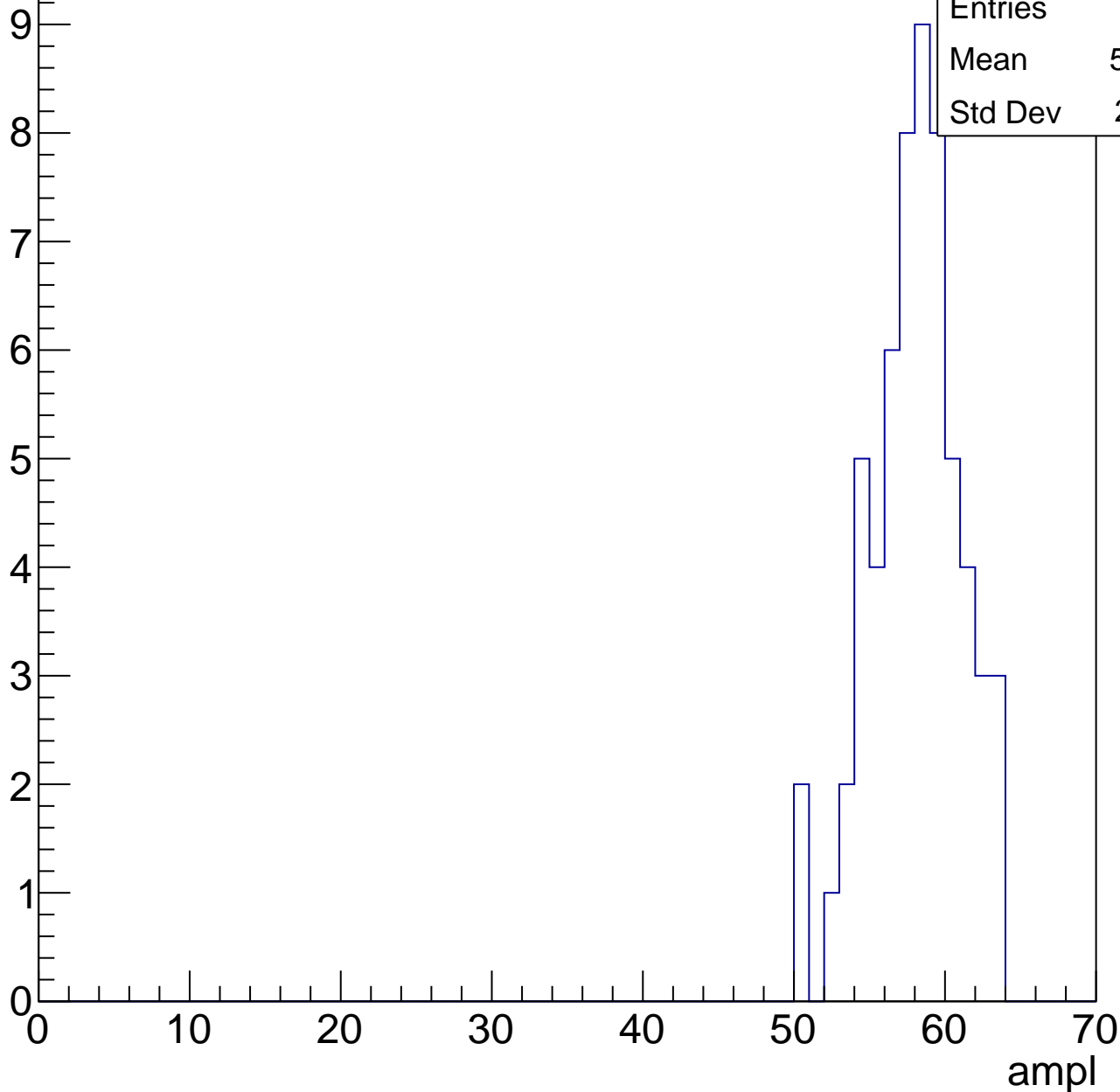
Entries	72
Mean	51.31
Std Dev	3.156



# B0L001S, U10-ch8, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



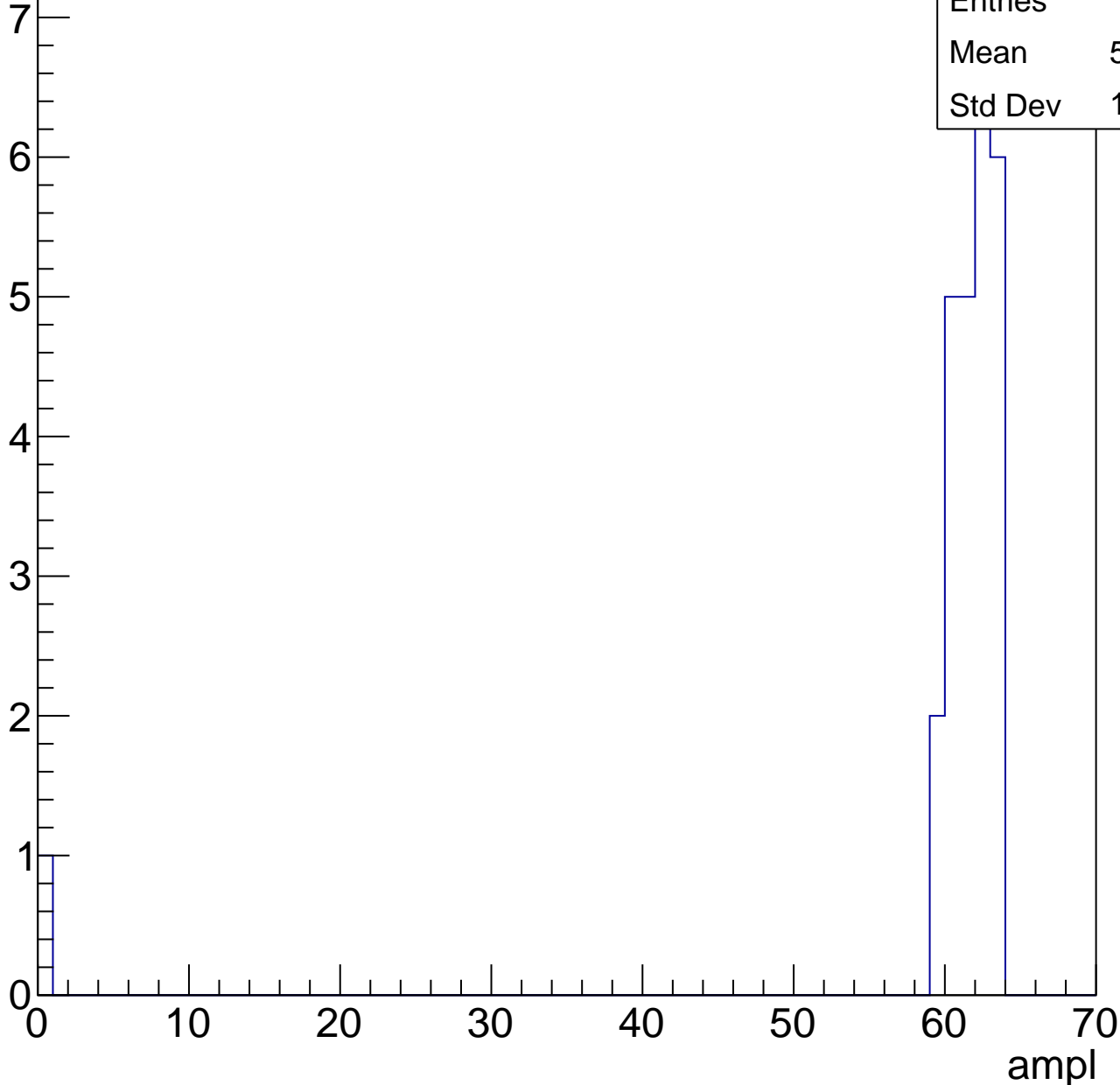
Entries	60
Mean	57.55
Std Dev	2.991

# B0L001S, U10-ch8, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	26
Mean	59.04
Std Dev	11.87



# B0L001S, U10-ch8, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch8, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U10-ch9, adc0

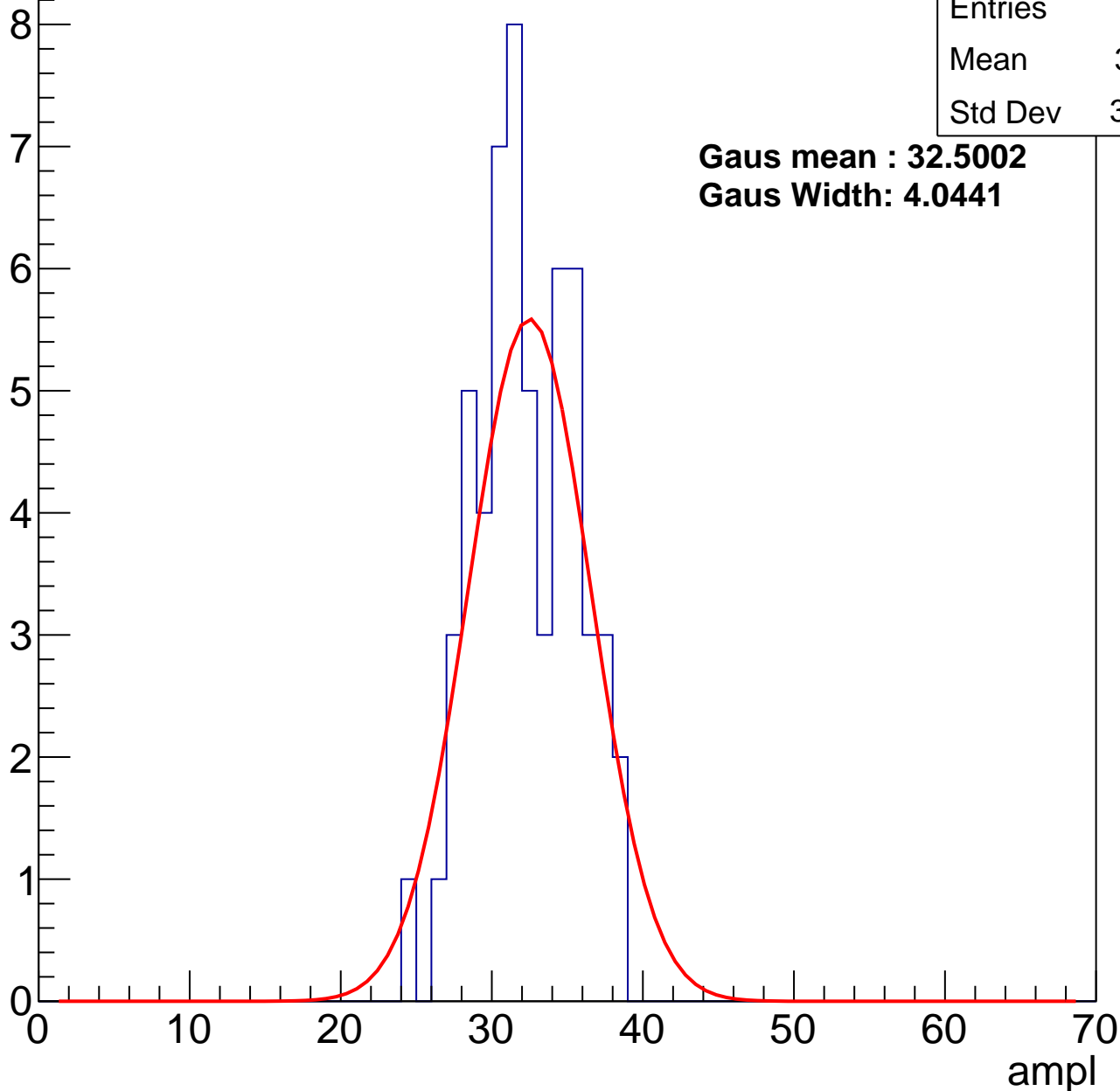
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	31.81
Std Dev	3.247

**Gaus mean : 32.5002**

**Gaus Width: 4.0441**



# B0L001S, U10-ch9, adc1

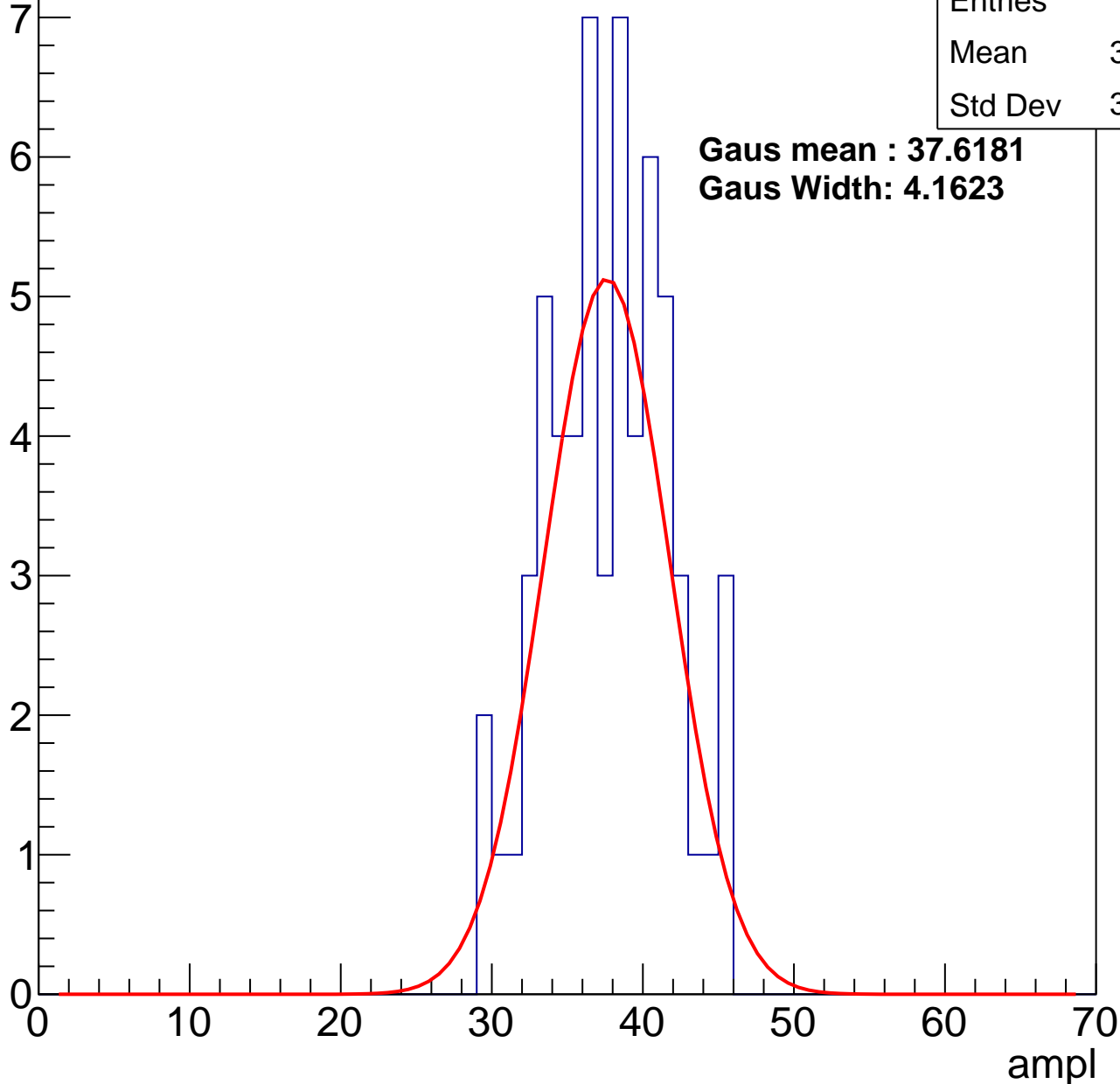
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	37.23
Std Dev	3.943

**Gaus mean : 37.6181**

**Gaus Width: 4.1623**



# B0L001S, U10-ch9, adc2

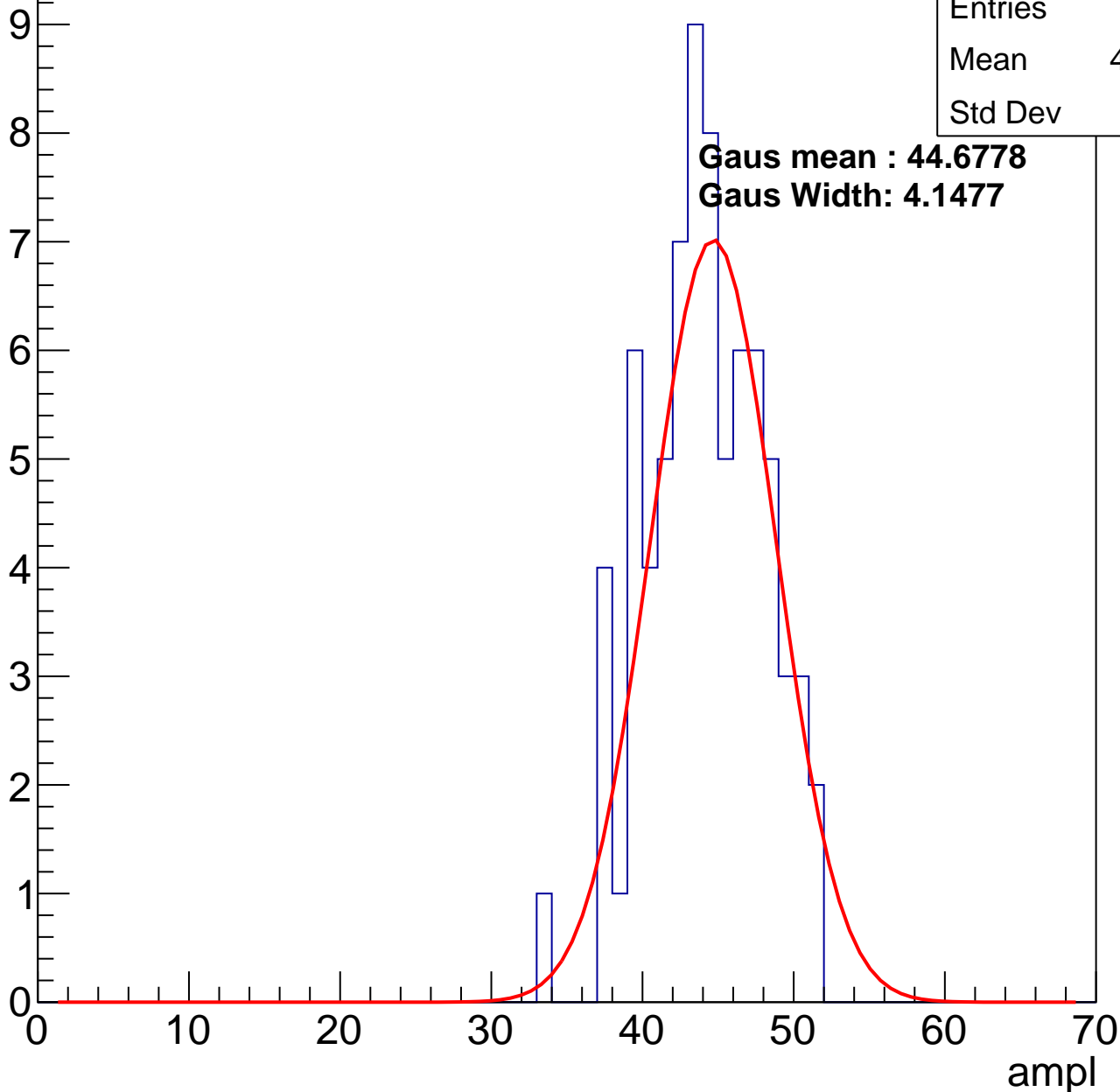
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	75
Mean	43.64
Std Dev	3.8

**Gaus mean : 44.6778**

**Gaus Width: 4.1477**

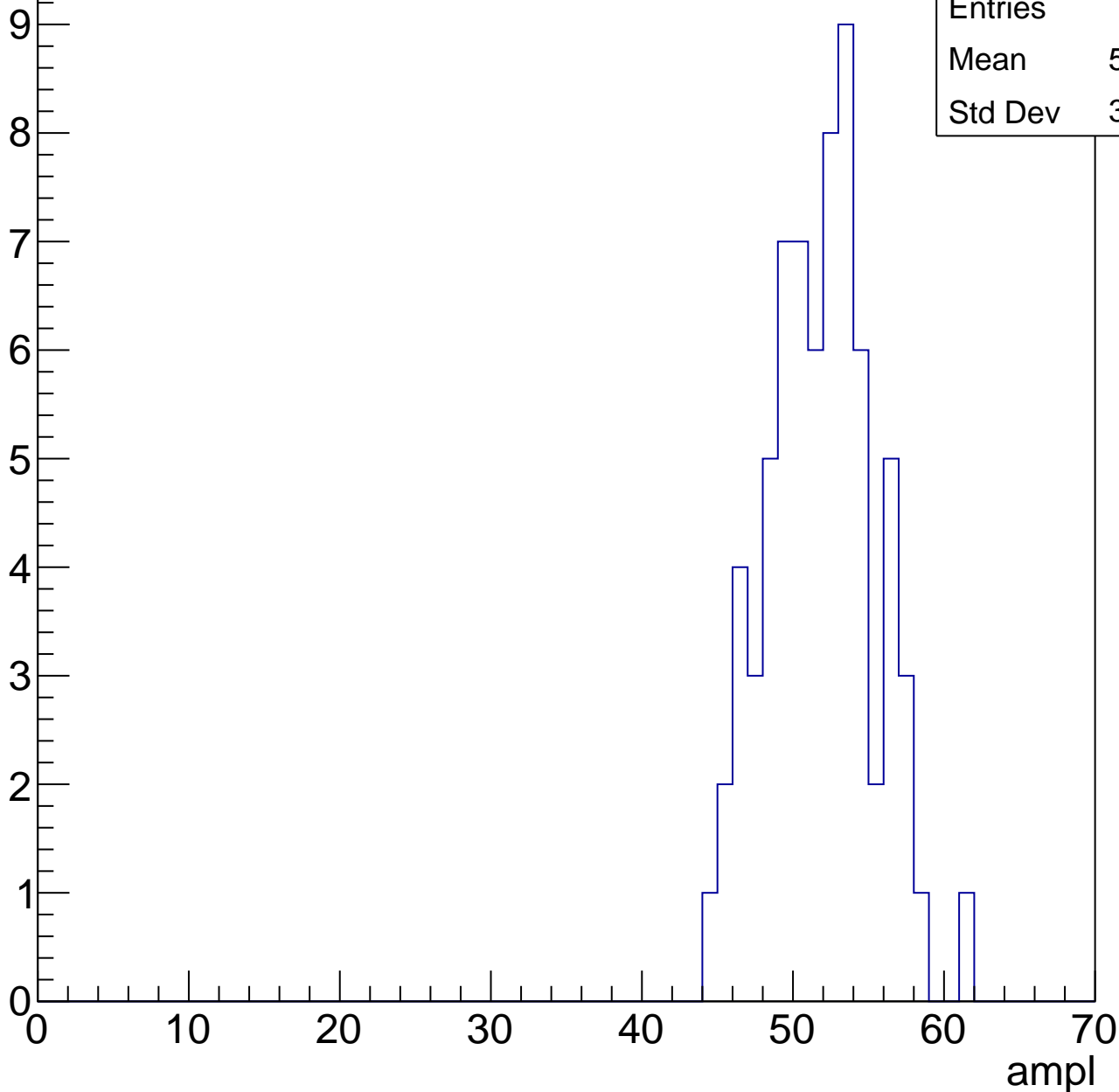


# B0L001S, U10-ch9, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	51.36
Std Dev	3.489

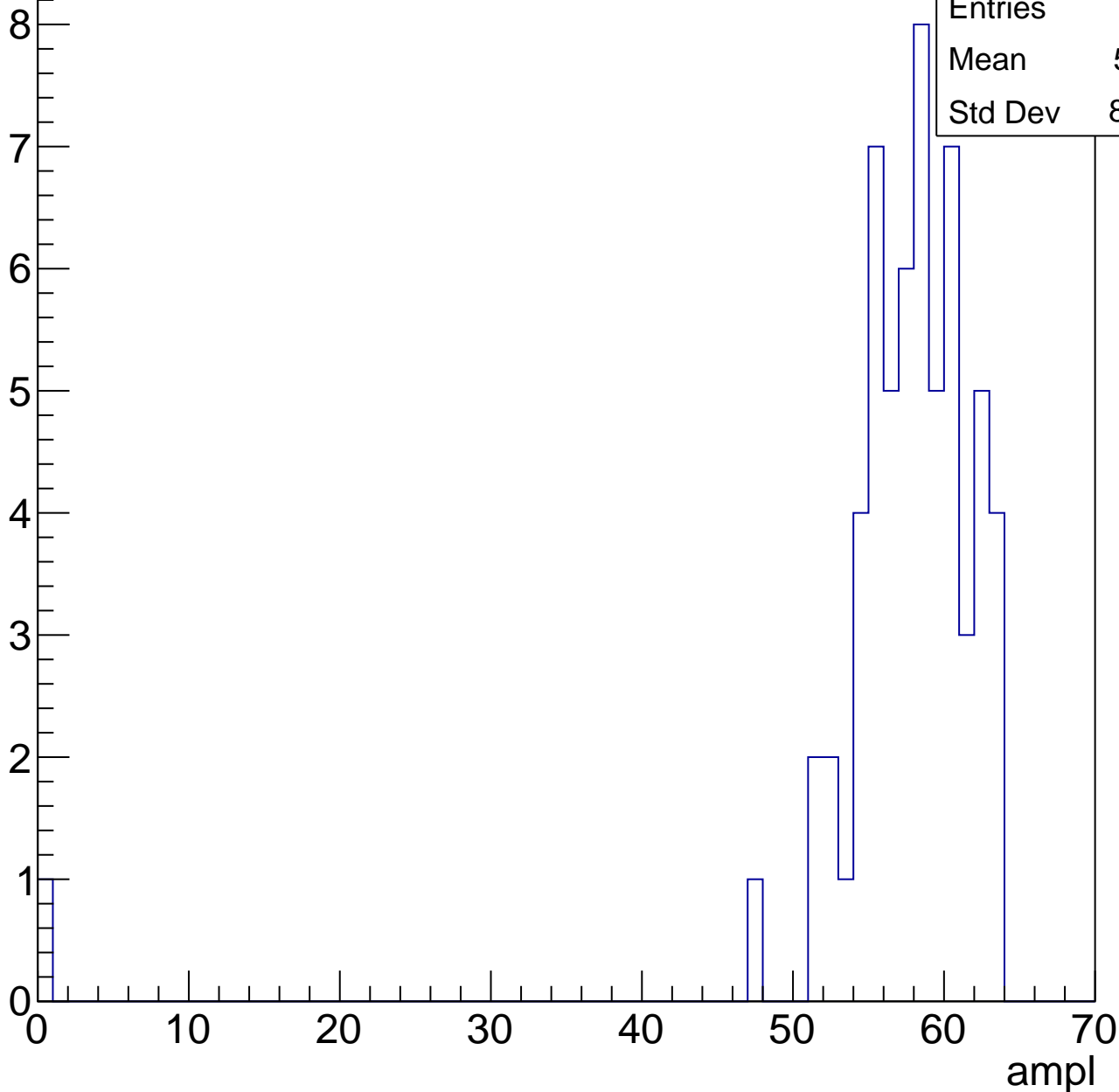


# B0L001S, U10-ch9, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	56.61
Std Dev	8.052

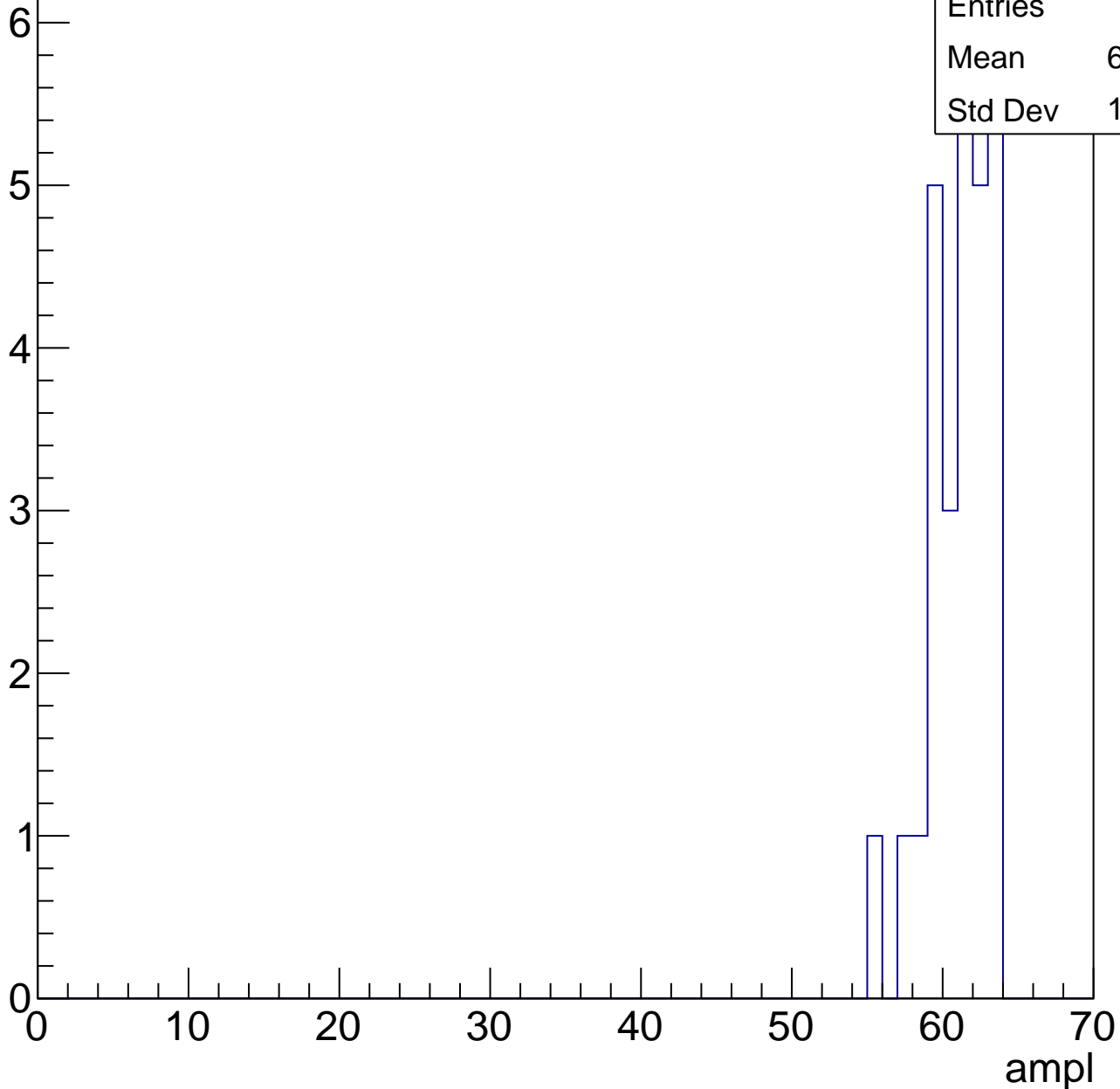


# B0L001S, U10-ch9, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	28
Mean	60.68
Std Dev	1.983



# B0L001S, U10-ch9, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U10-ch9, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U10-ch10, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	65
Mean	30.89
Std Dev	3.104

**Gaus mean : 31.4900**

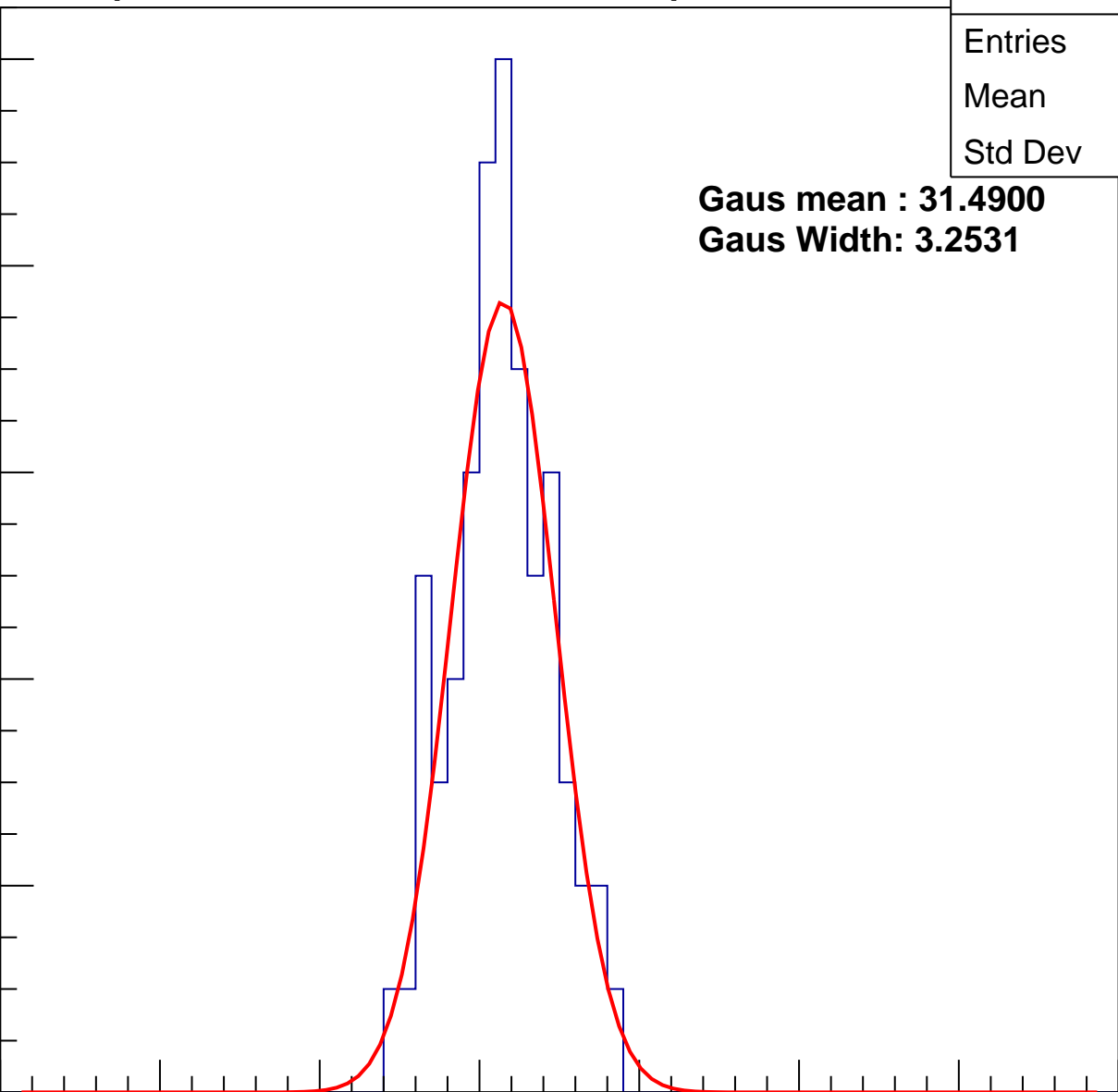
**Gaus Width: 3.2531**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U10-ch10, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	76
Mean	37.75
Std Dev	3.495

**Gaus mean : 38.1714**

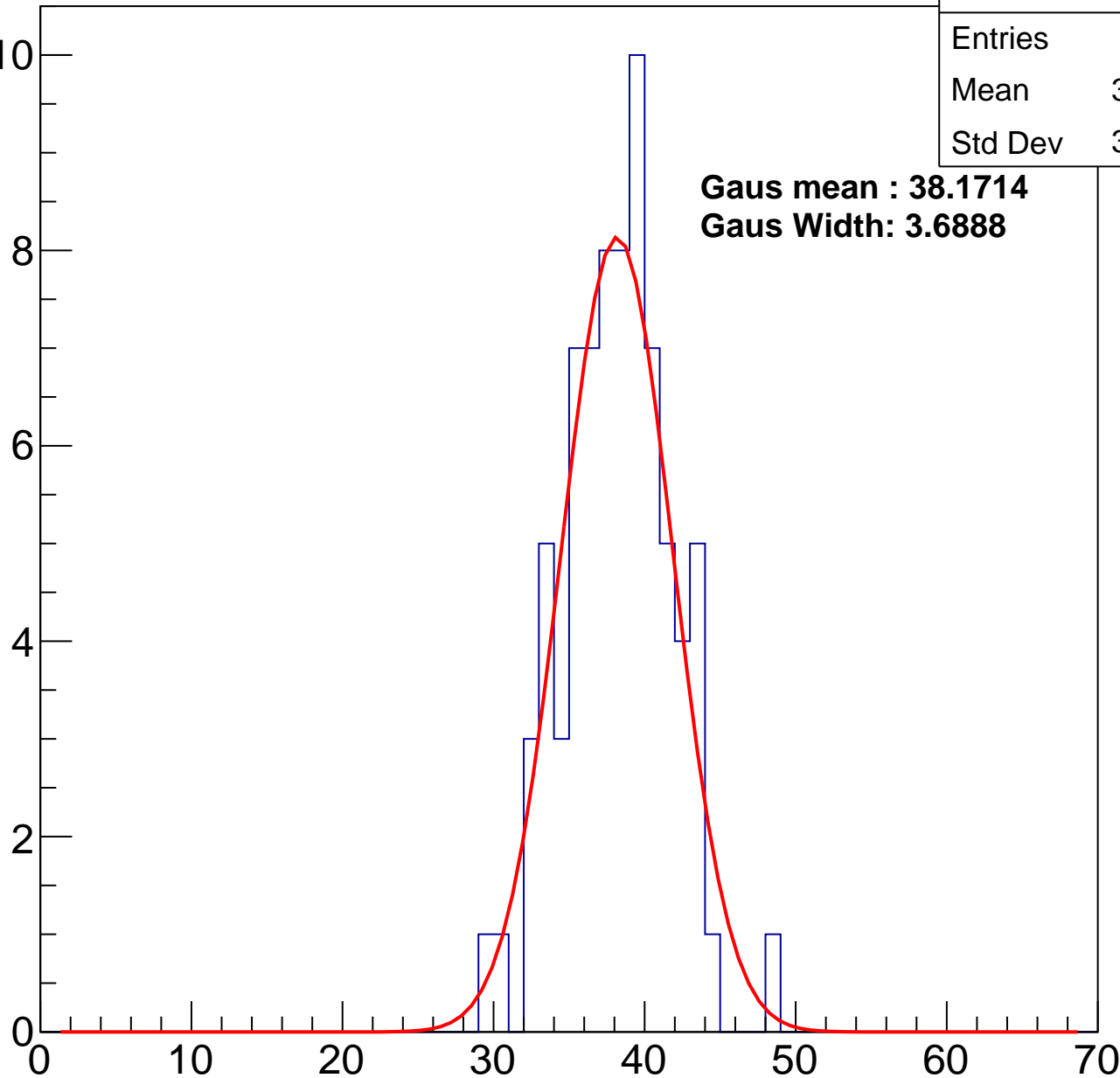
**Gaus Width: 3.6888**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B0L001S, U10-ch10, adc2

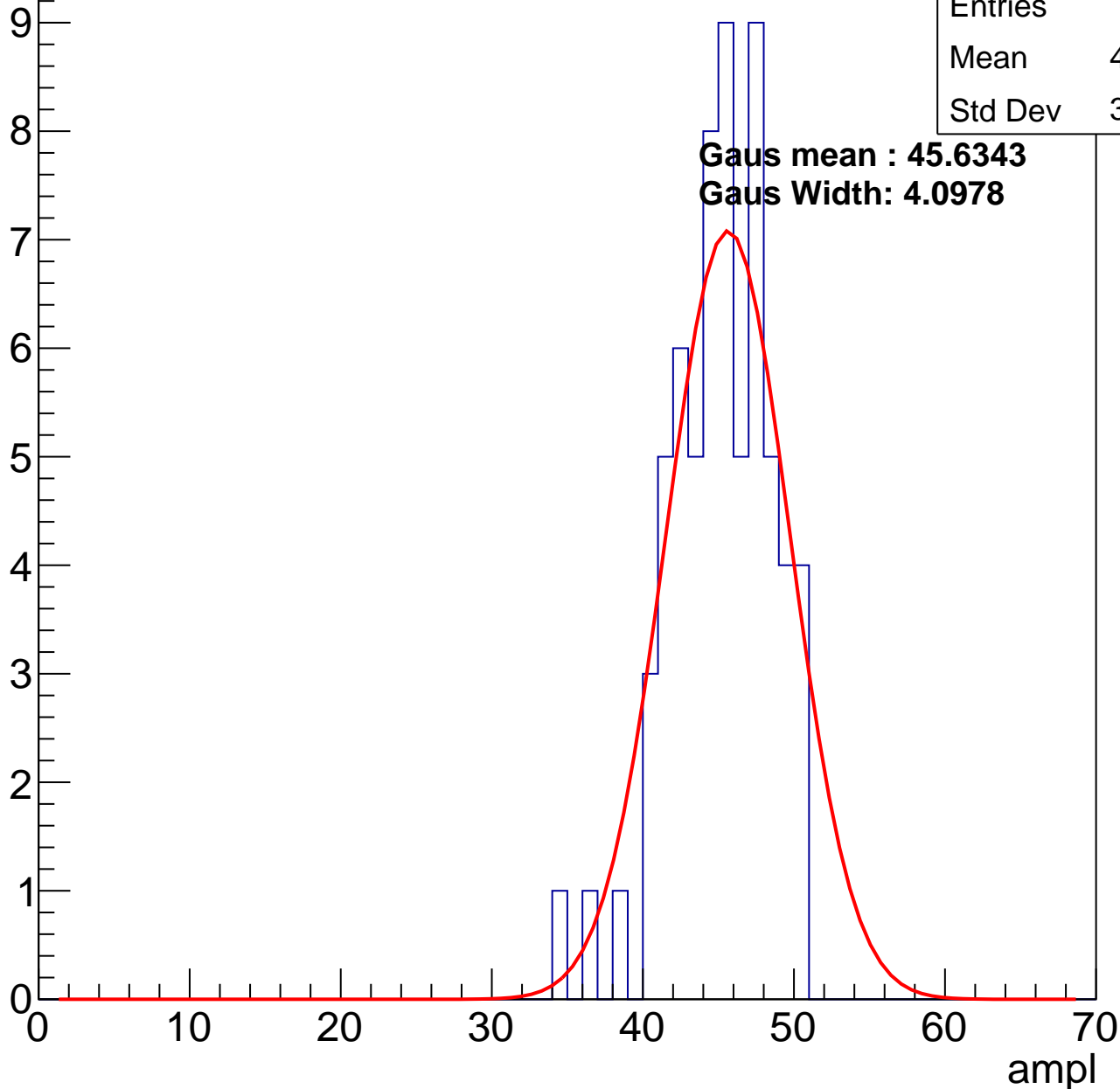
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	44.64
Std Dev	3.324

**Gaus mean : 45.6343**

**Gaus Width: 4.0978**

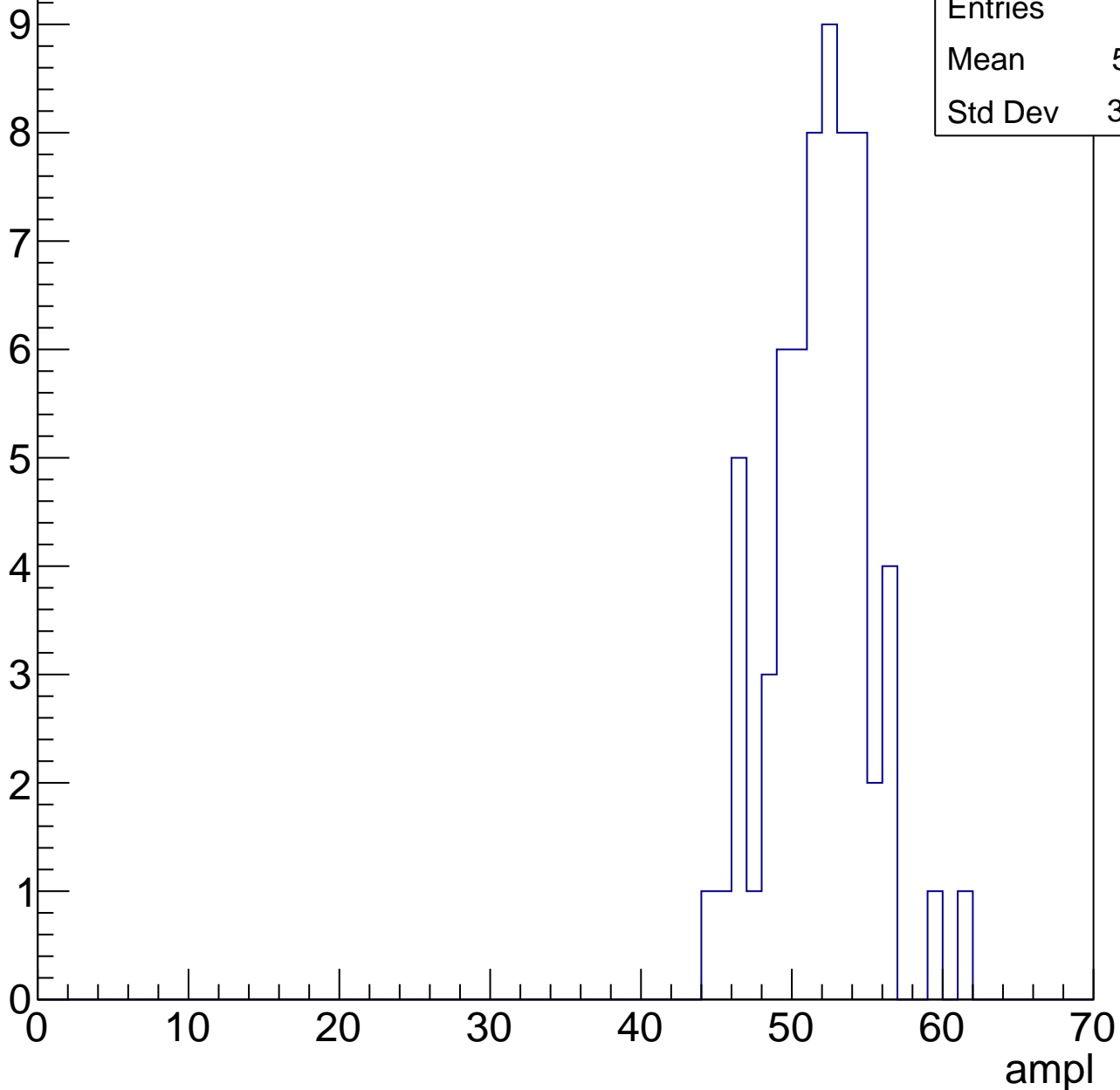


# B0L001S, U10-ch10, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

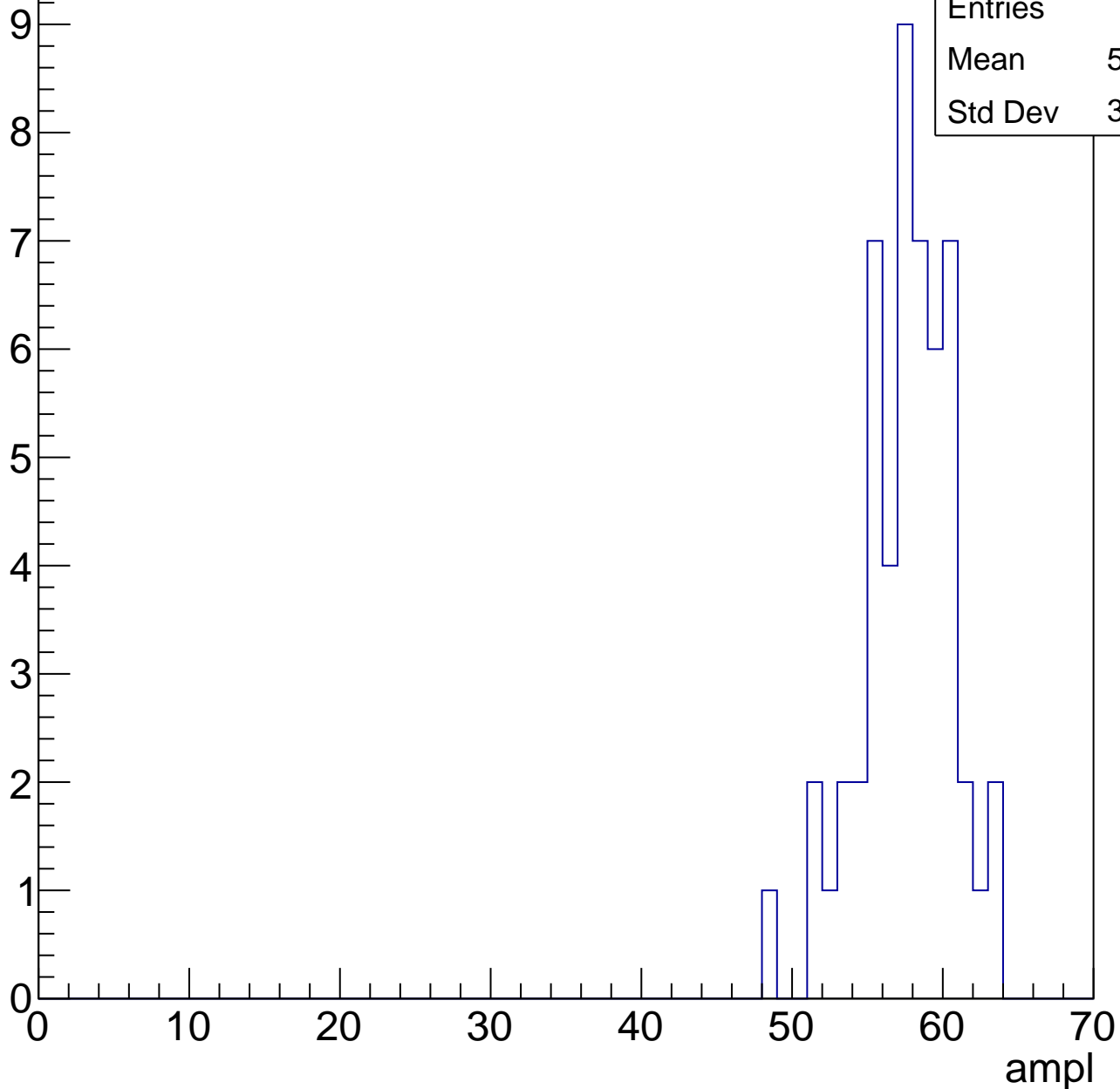
Entries	64
Mean	51.41
Std Dev	3.263



# B0L001S, U10-ch10, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

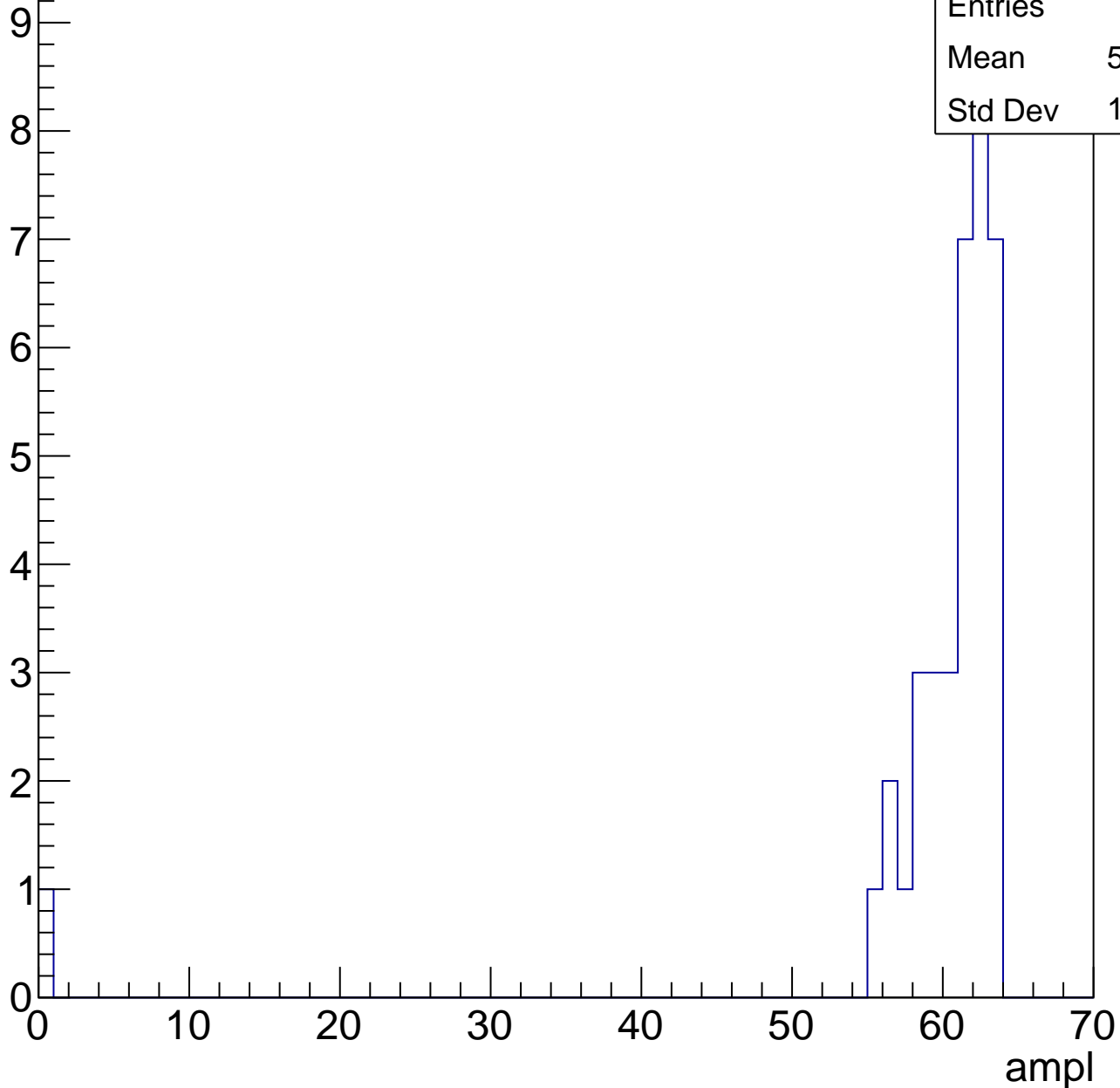
Entry



# B0L001S, U10-ch10, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U10-ch10, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch10, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U10-ch11, adc0

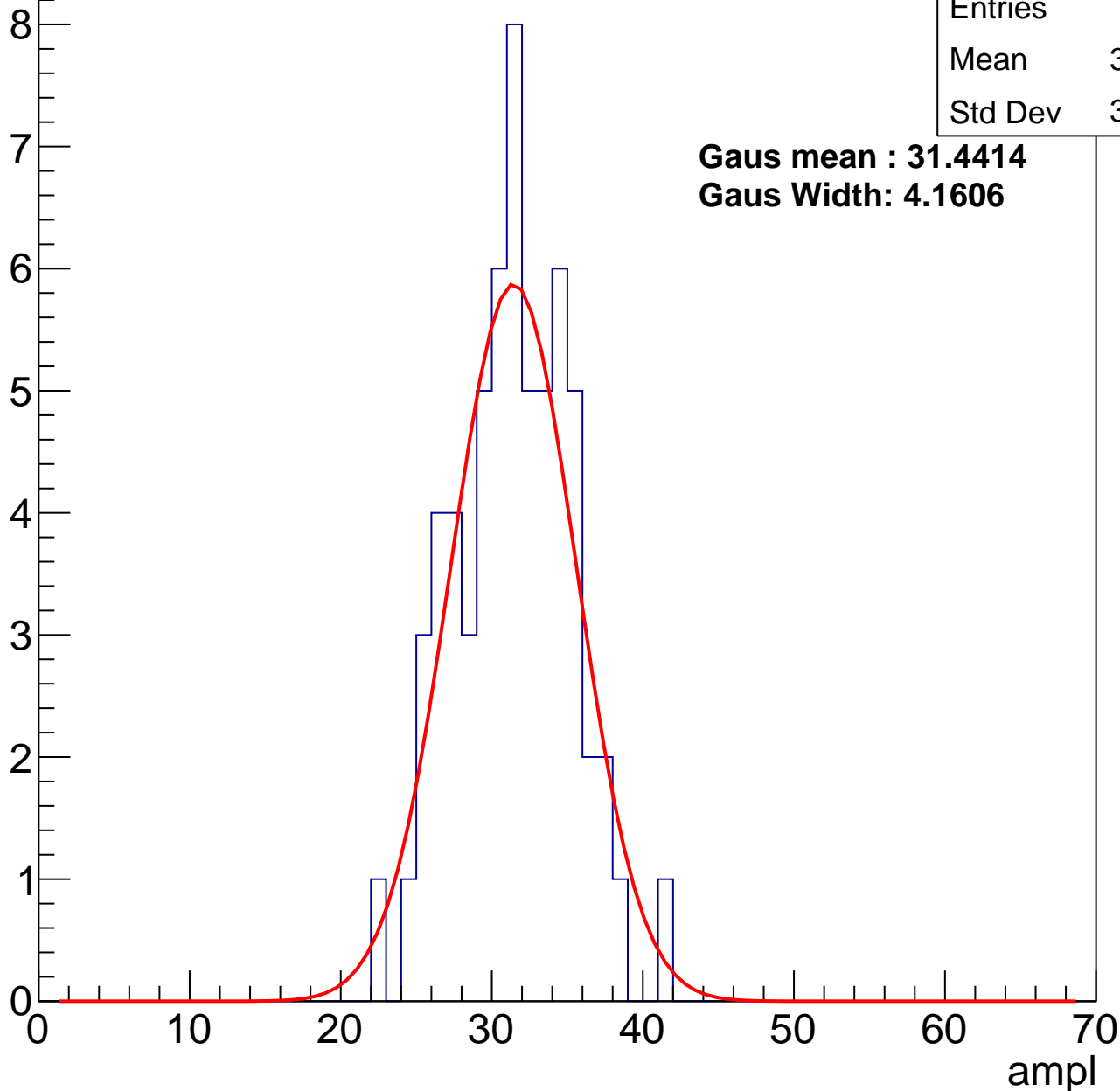
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	30.95
Std Dev	3.778

**Gaus mean : 31.4414**

**Gaus Width: 4.1606**



# B0L001S, U10-ch11, adc1

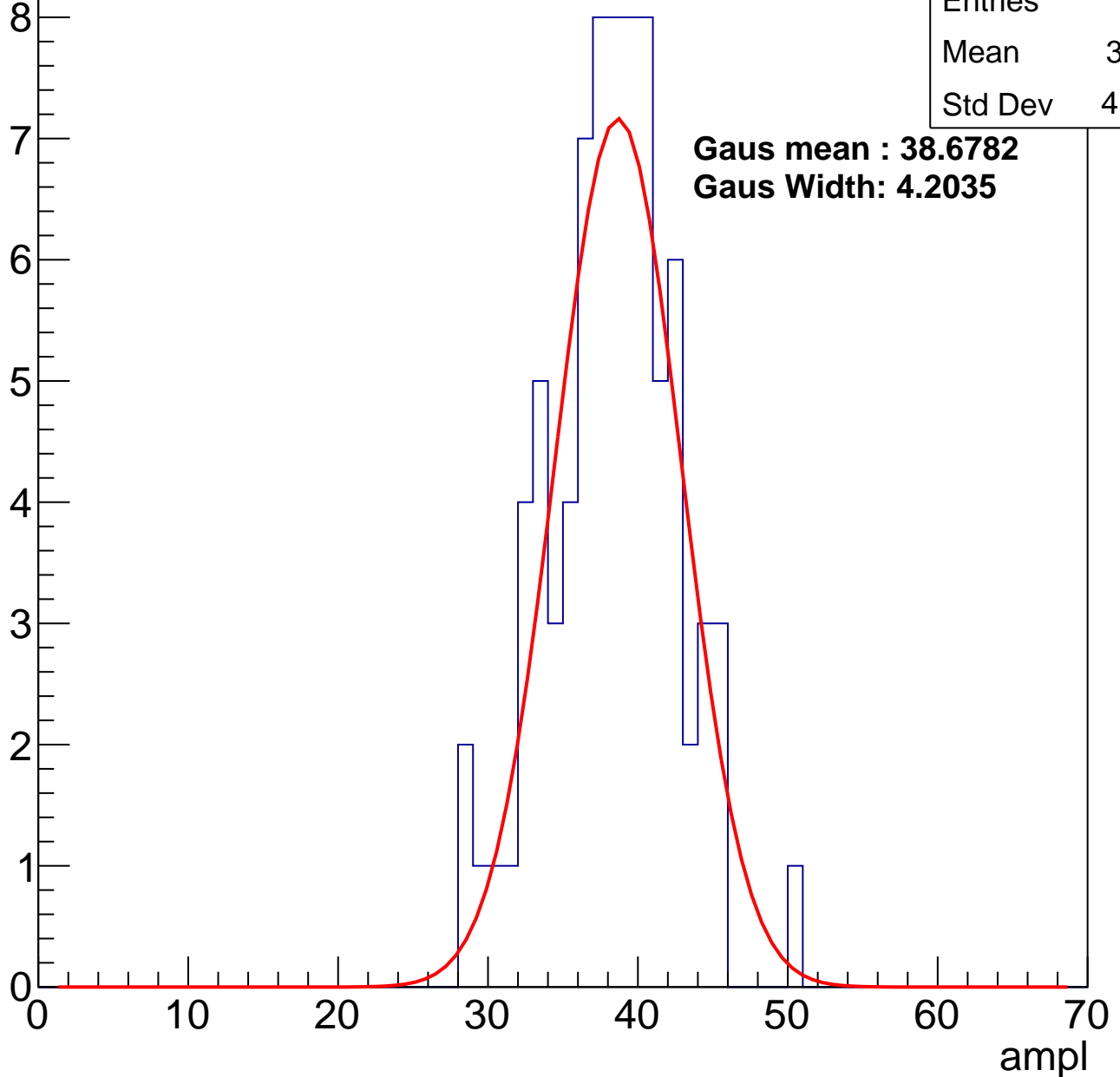
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	80
Mean	37.81
Std Dev	4.198

**Gaus mean : 38.6782**

**Gaus Width: 4.2035**



# B0L001S, U10-ch11, adc2

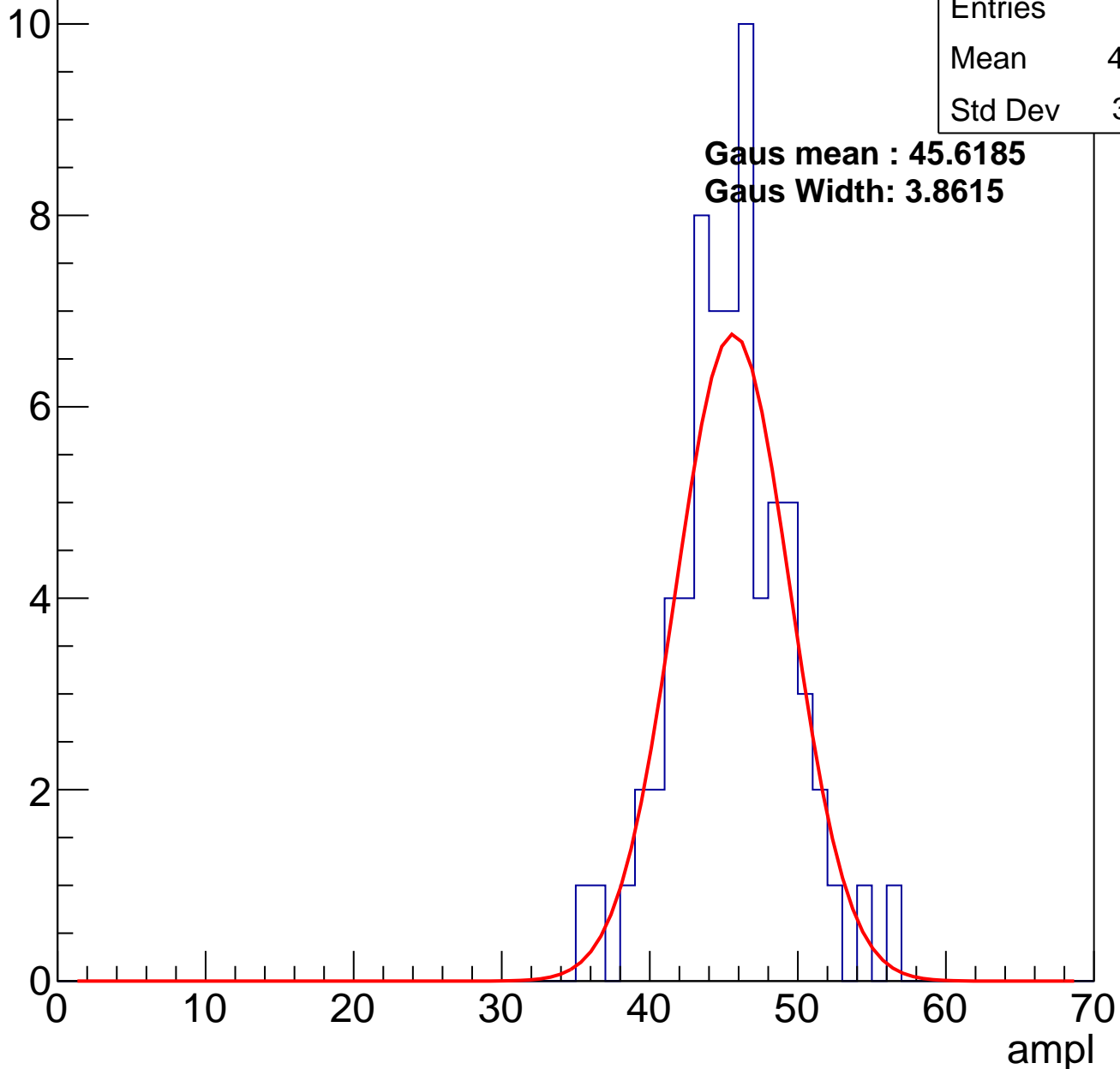
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	69
Mean	45.12
Std Dev	3.881

**Gaus mean : 45.6185**

**Gaus Width: 3.8615**

Entry

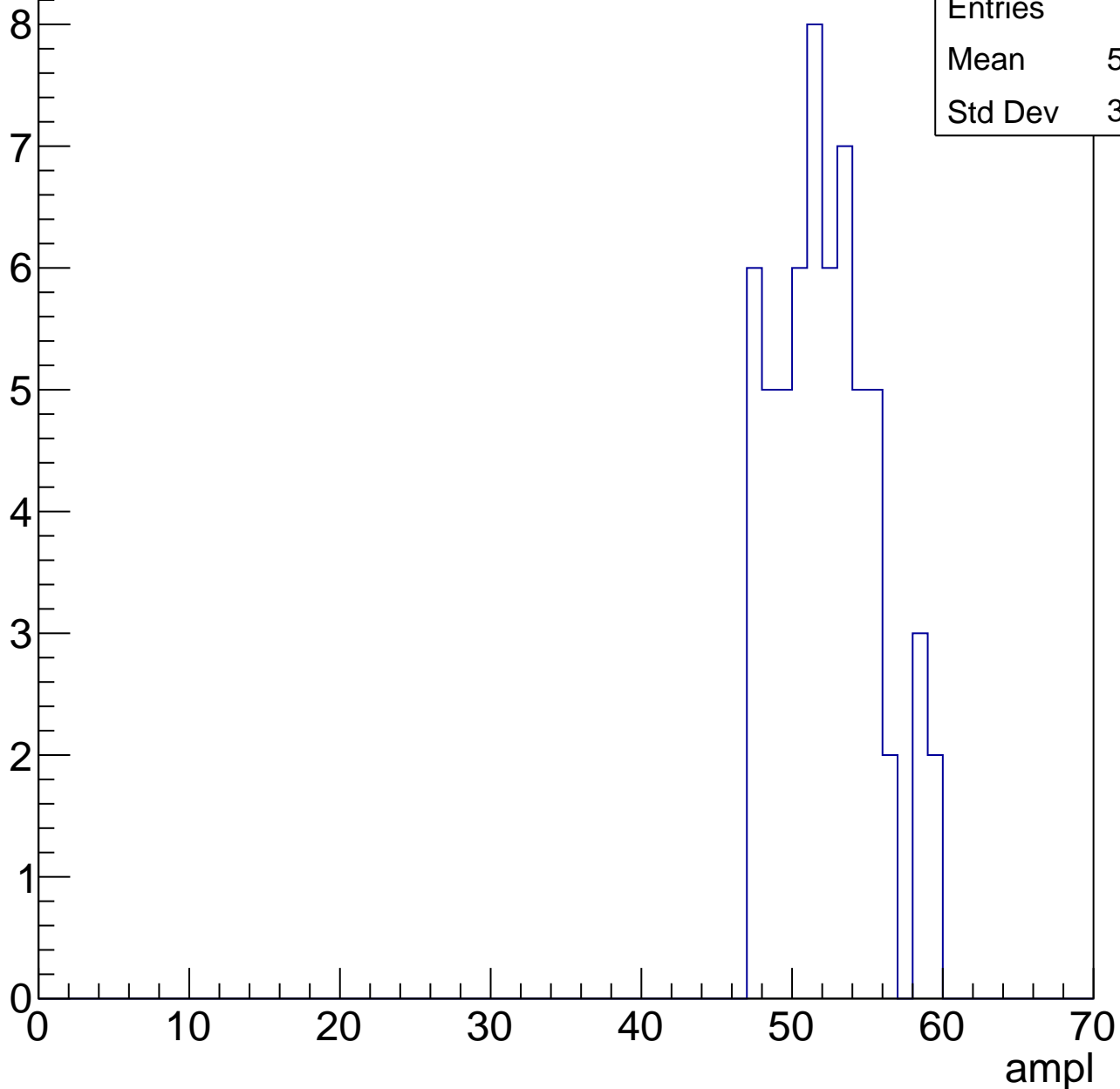


# B0L001S, U10-ch11, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	51.78
Std Dev	3.199

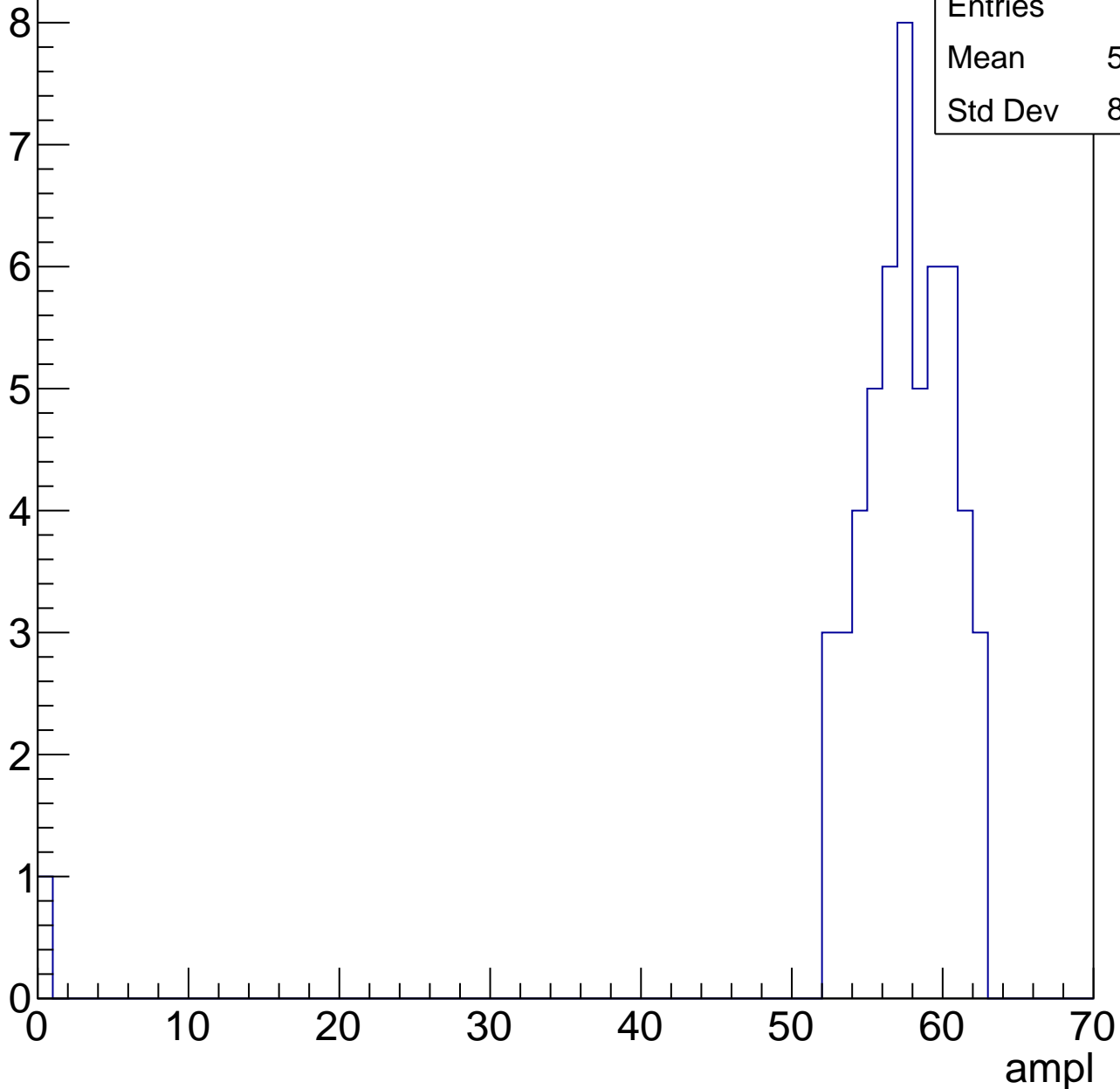


# B0L001S, U10-ch11, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	56.15
Std Dev	8.184

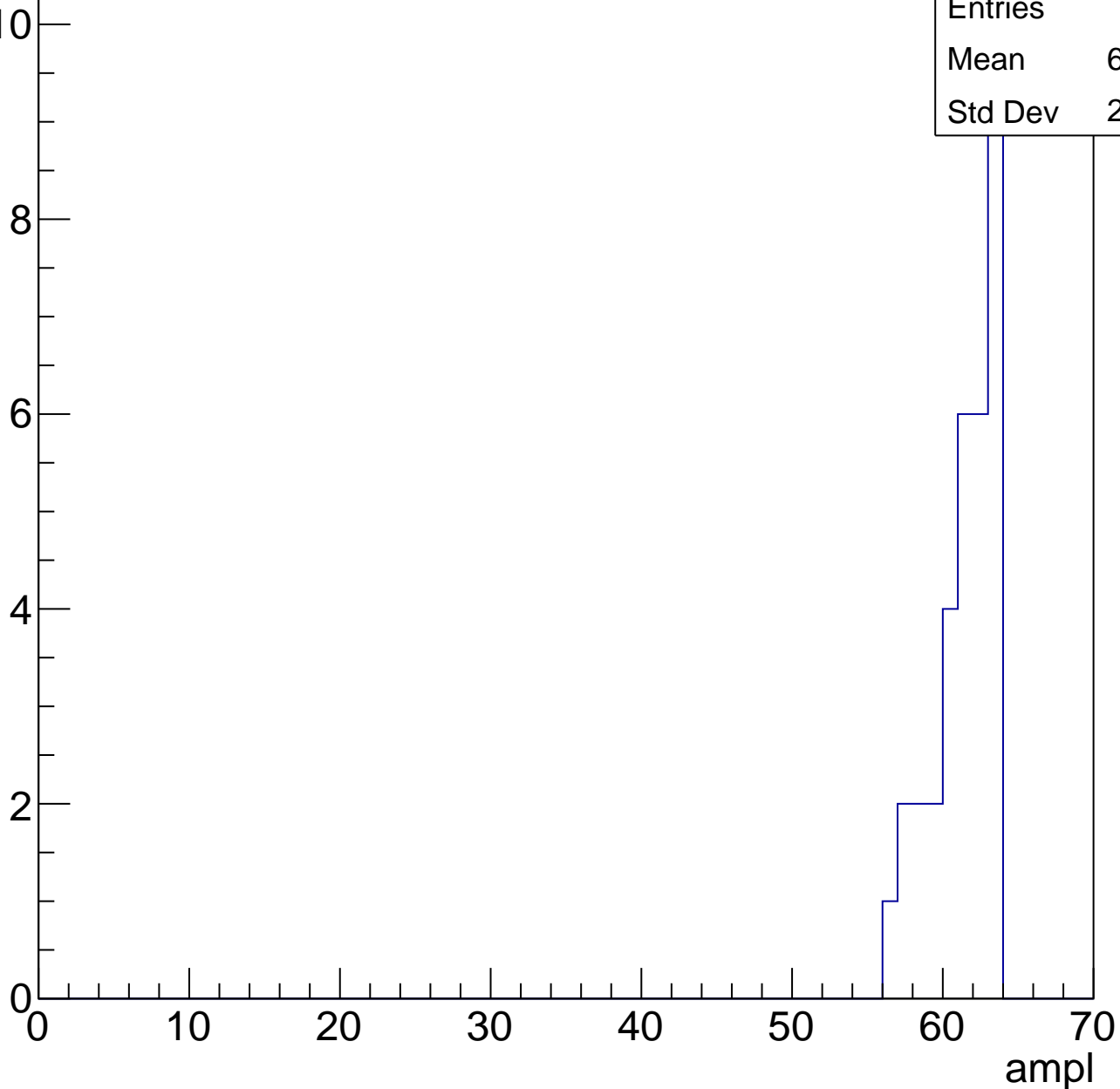


# B0L001S, U10-ch11, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	33
Mean	60.97
Std Dev	2.007



# B0L001S, U10-ch11, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch11, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U10-ch12, adc0

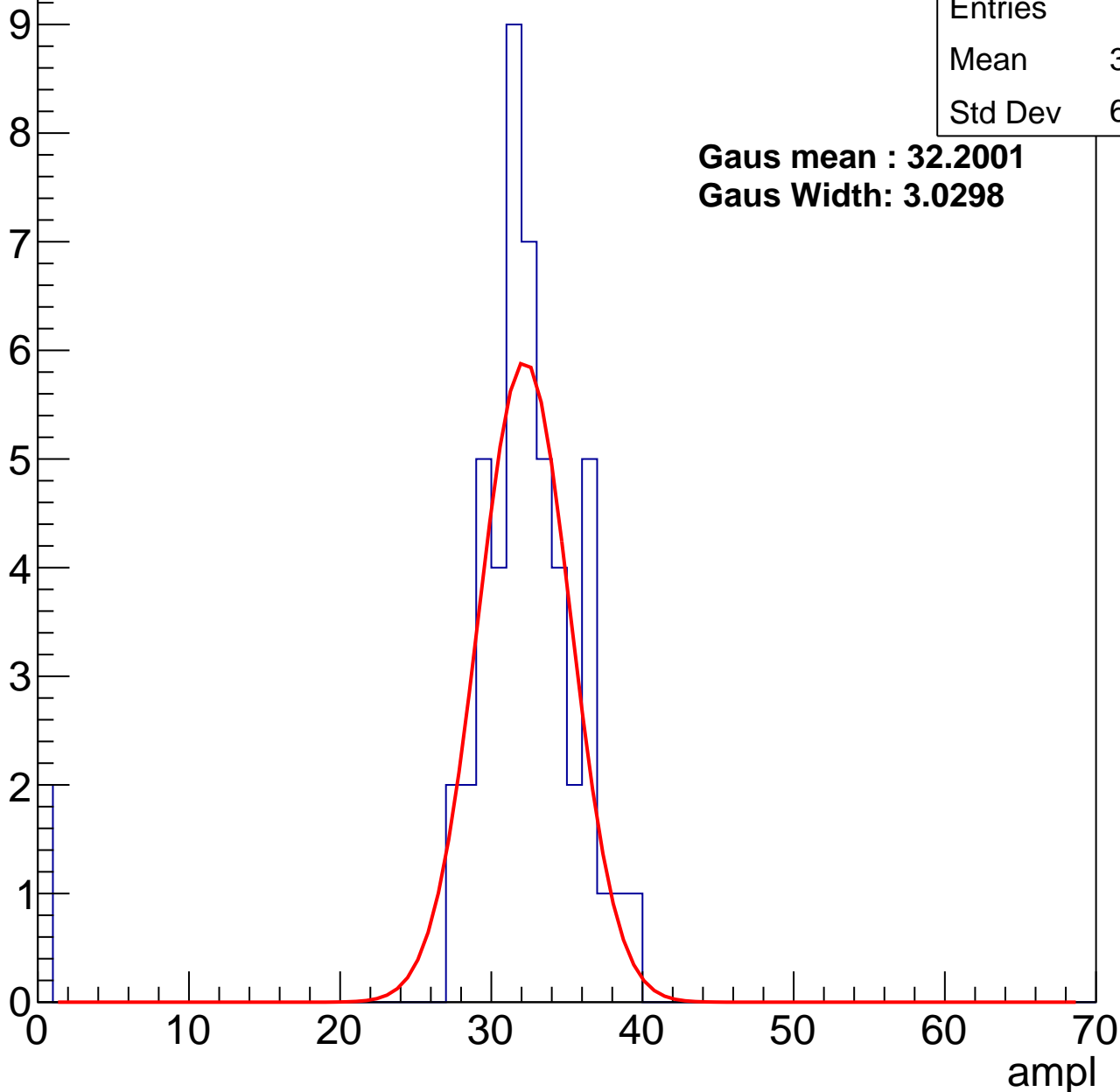
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	50
Mean	30.86
Std Dev	6.876

**Gaus mean : 32.2001**

**Gaus Width: 3.0298**



# B0L001S, U10-ch12, adc1

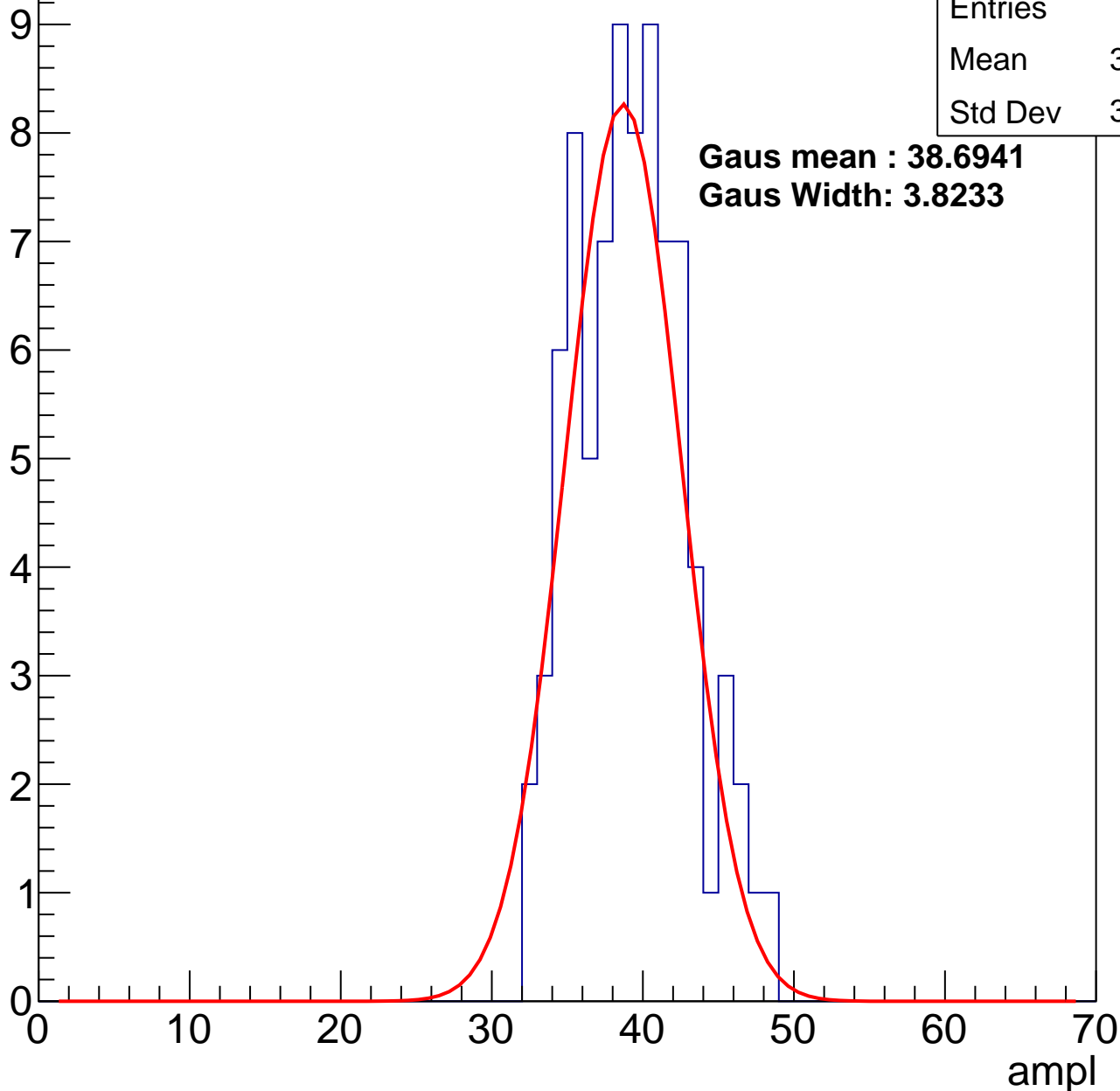
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	83
Mean	38.78
Std Dev	3.644

**Gaus mean : 38.6941**

**Gaus Width: 3.8233**



# B0L001S, U10-ch12, adc2

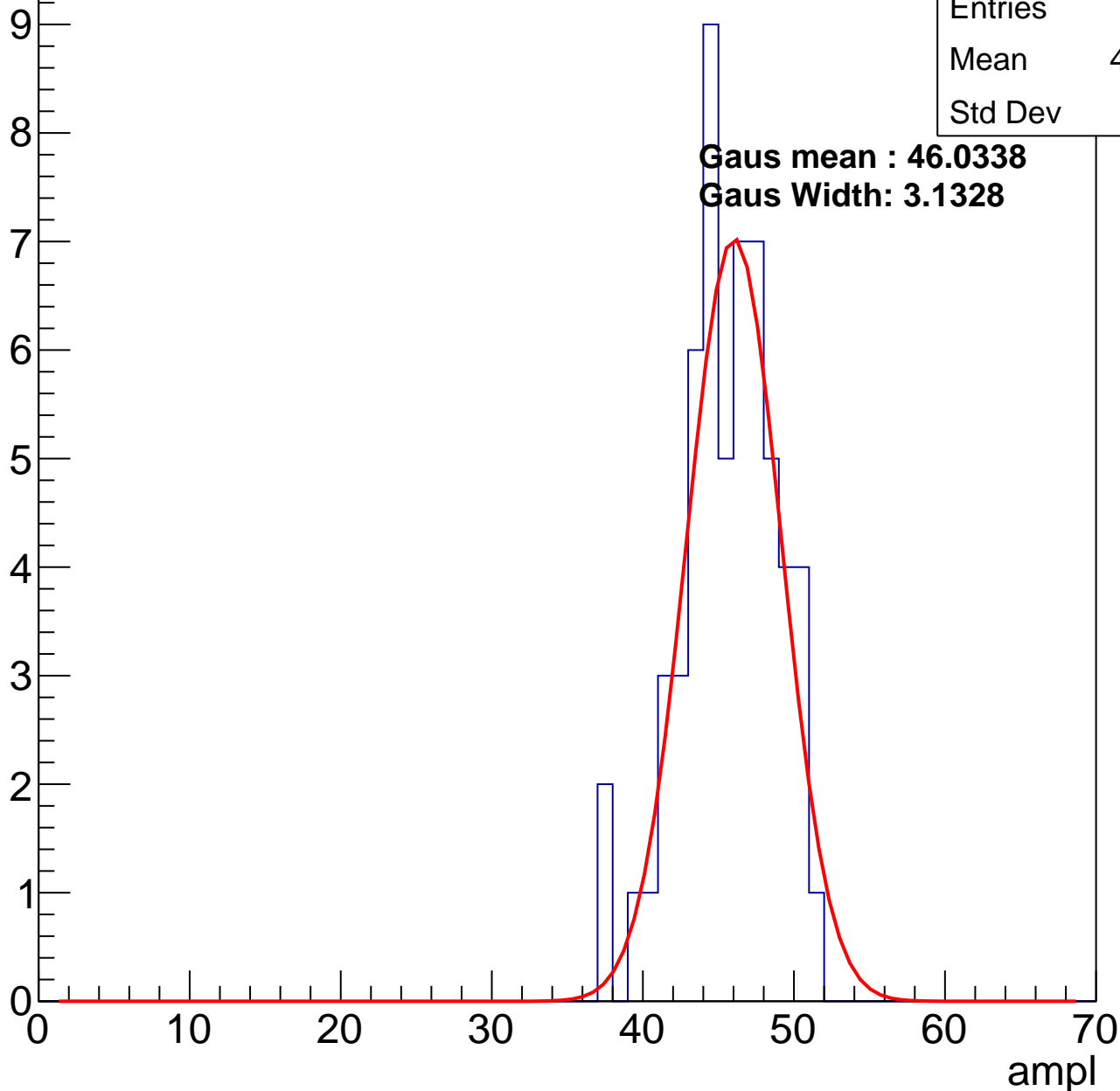
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	45.16
Std Dev	3.15

**Gaus mean : 46.0338**

**Gaus Width: 3.1328**



# B0L001S, U10-ch12, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	62
Mean	51.81
Std Dev	3.136

Entry

10

8

6

4

2

0

0

10

20

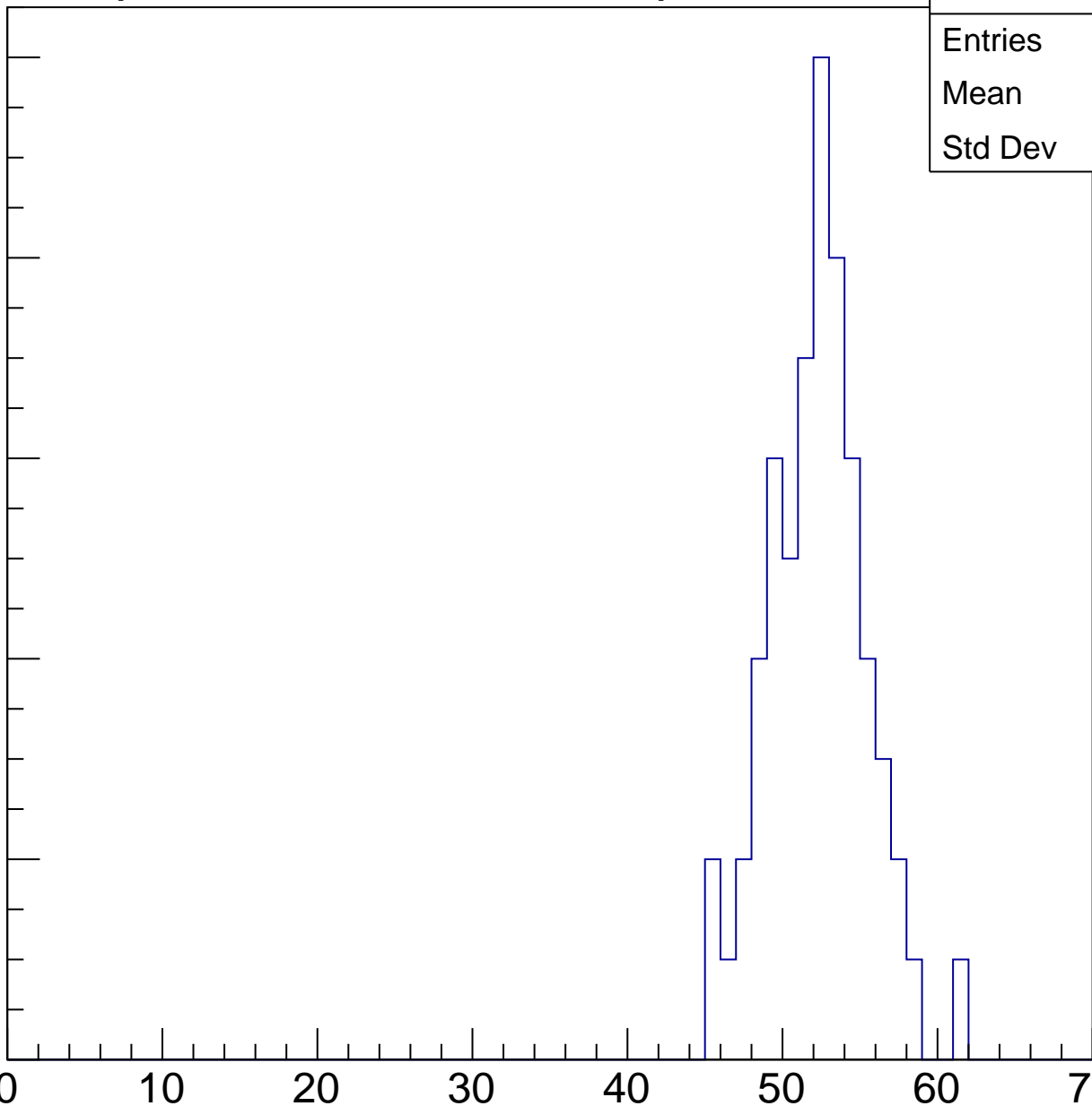
30

40

50

60

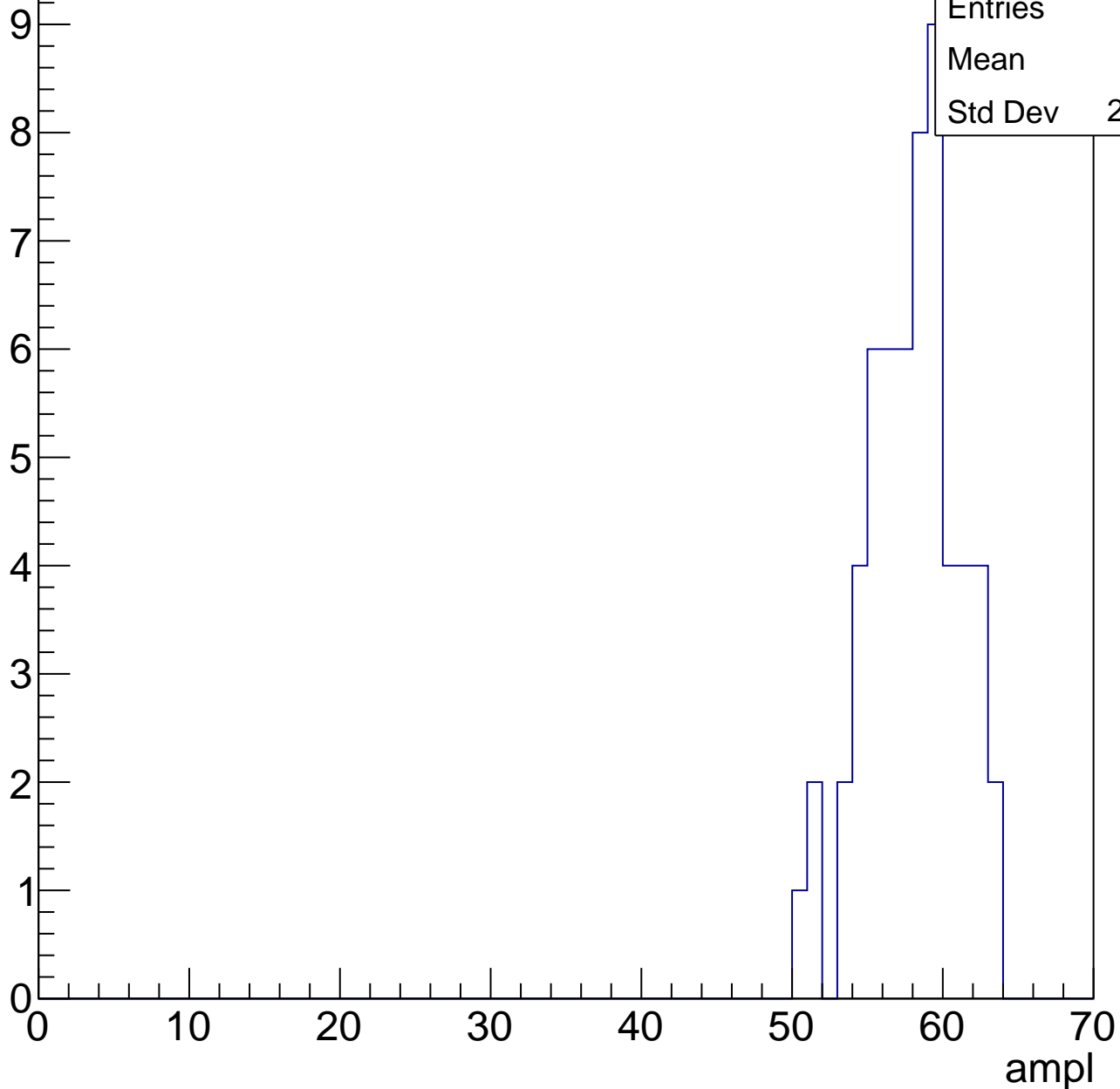
ampl



# B0L001S, U10-ch12, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



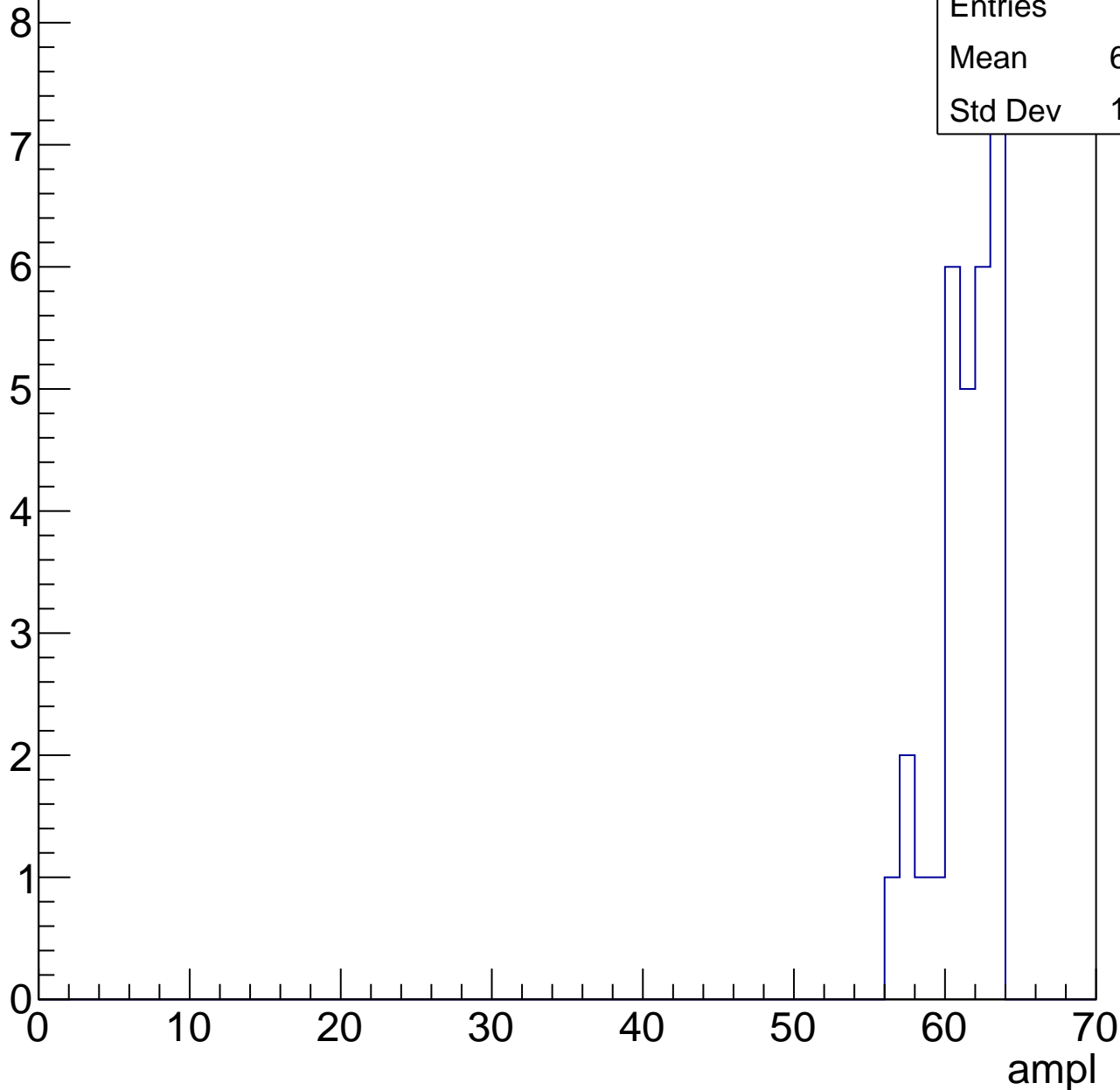
Entries	58
Mean	57.5
Std Dev	2.996

# B0L001S, U10-ch12, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	30
Mean	60.93
Std Dev	1.948



# B0L001S, U10-ch12, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch12, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U10-ch13, adc0

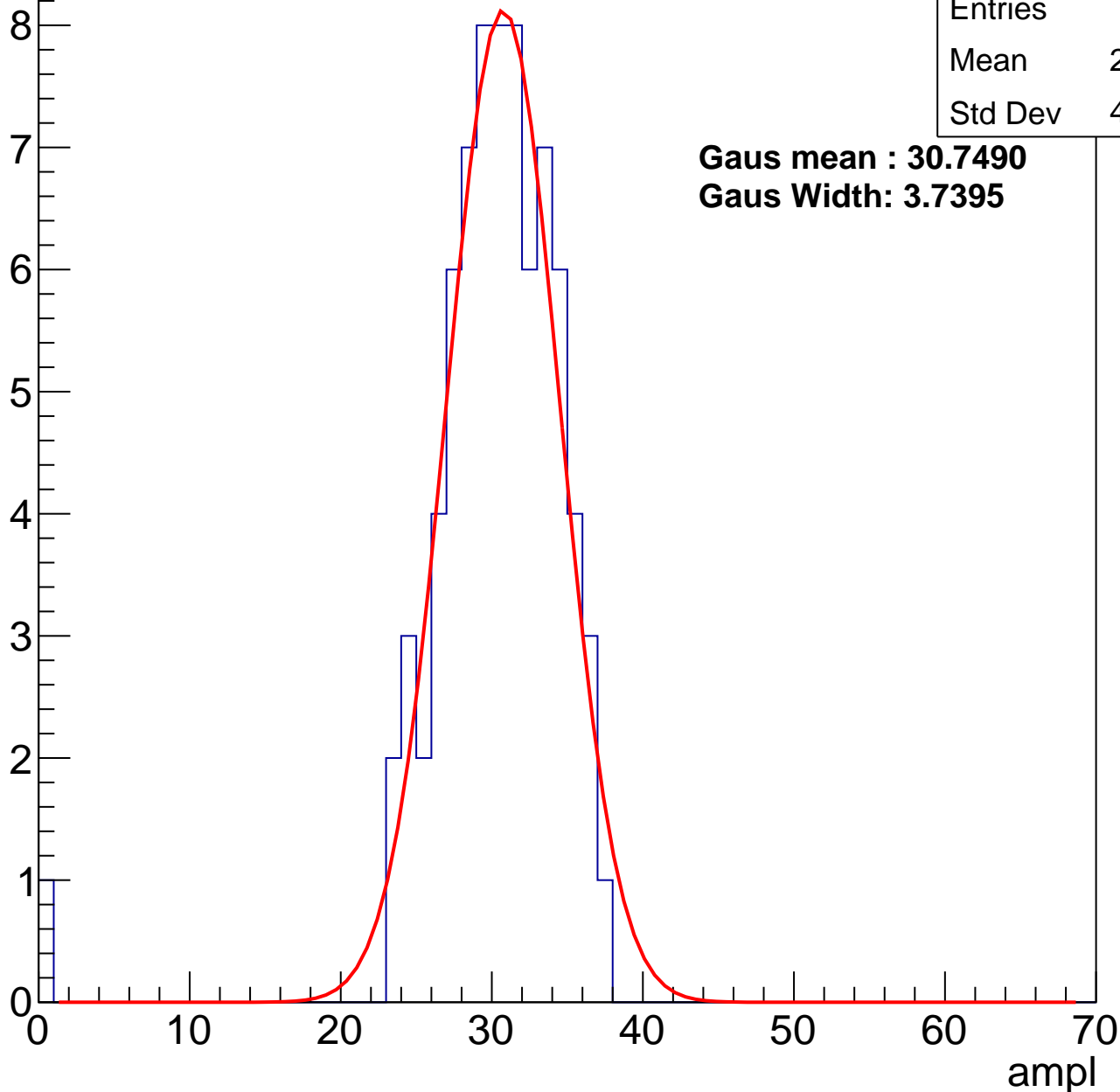
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	76
Mean	29.76
Std Dev	4.804

**Gaus mean : 30.7490**

**Gaus Width: 3.7395**



# B0L001S, U10-ch13, adc1

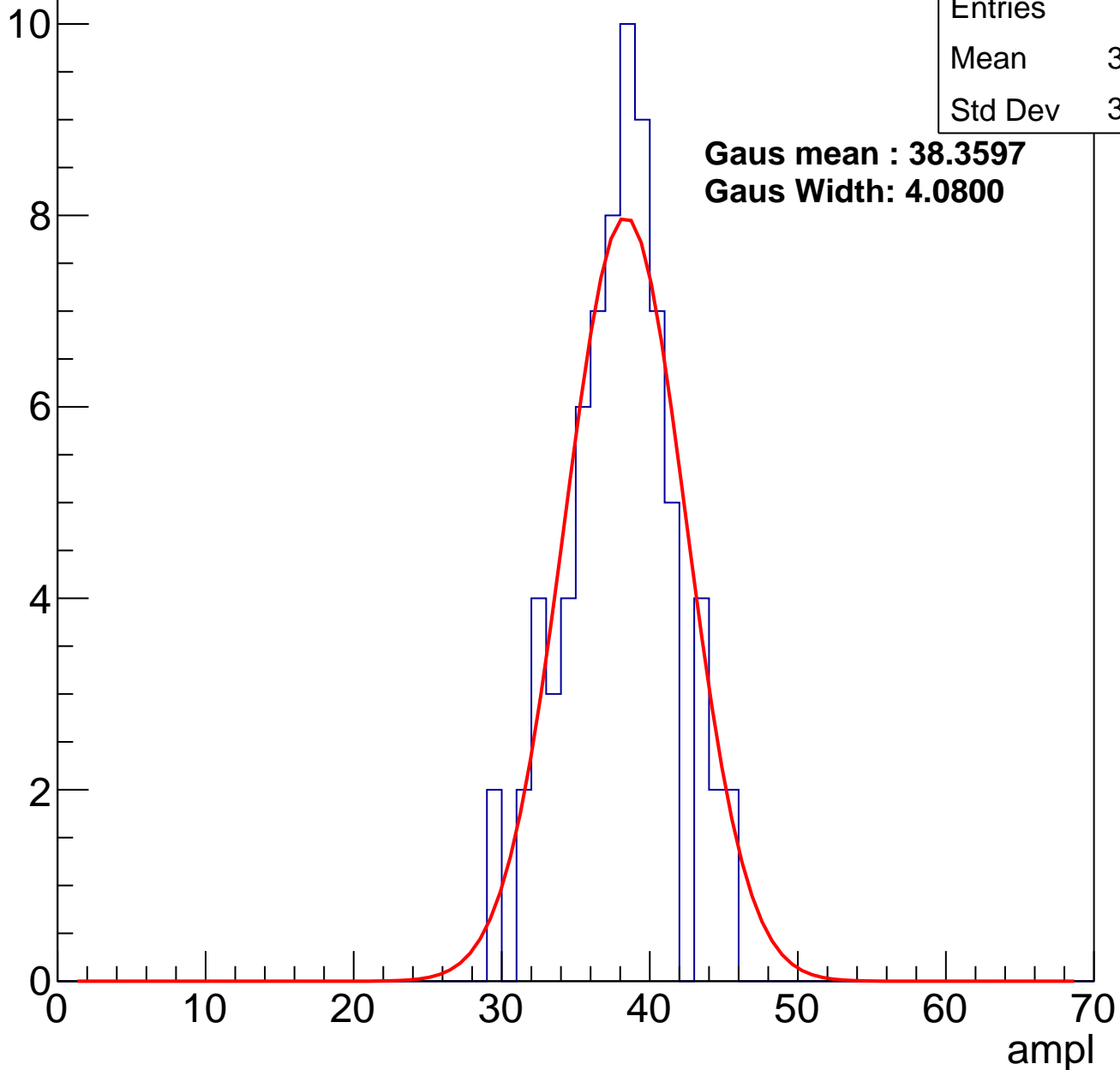
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	75
Mean	37.43
Std Dev	3.578

**Gaus mean : 38.3597**

**Gaus Width: 4.0800**

Entry



# B0L001S, U10-ch13, adc2

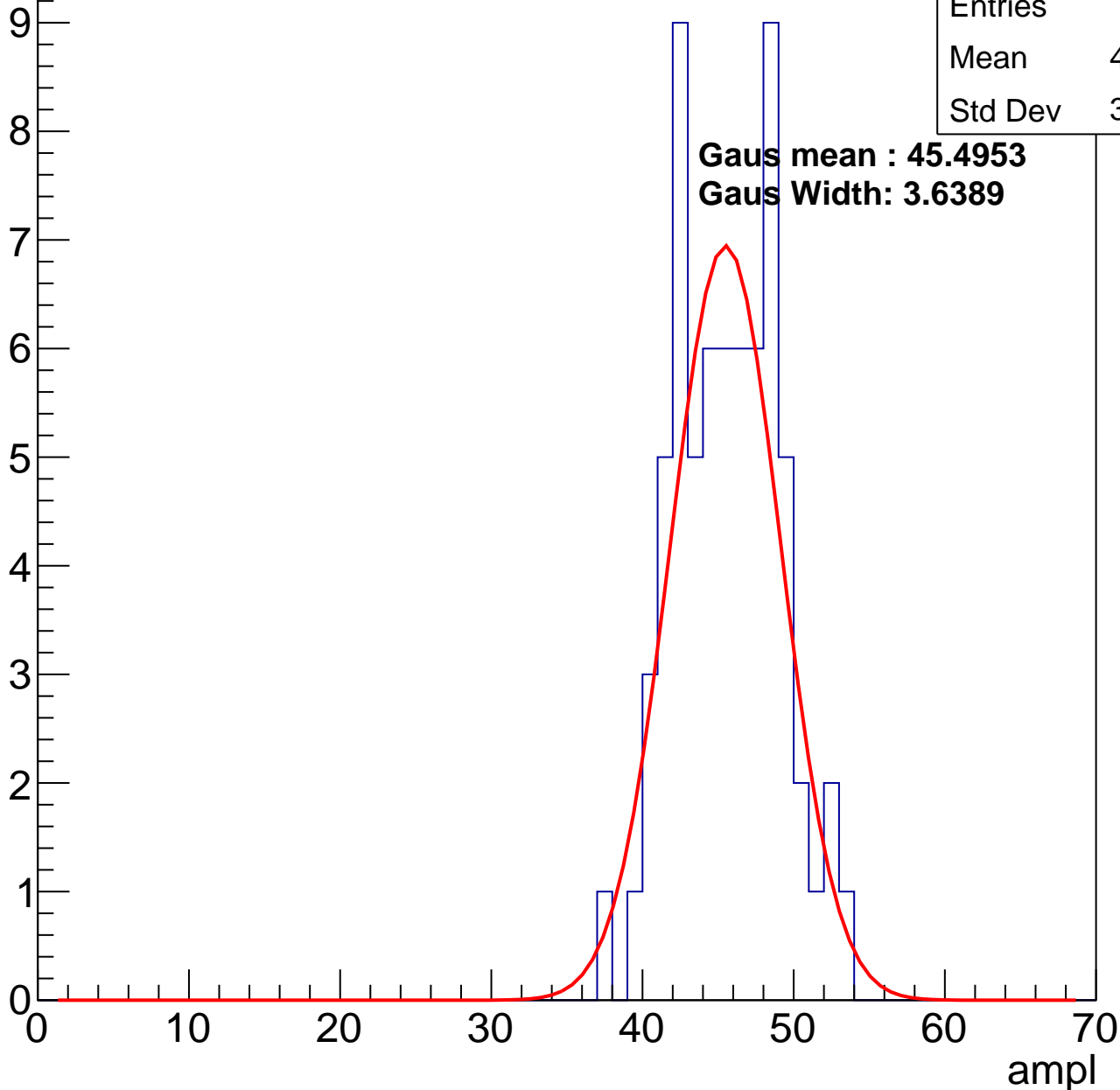
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	45.16
Std Dev	3.428

**Gaus mean : 45.4953**

**Gaus Width: 3.6389**

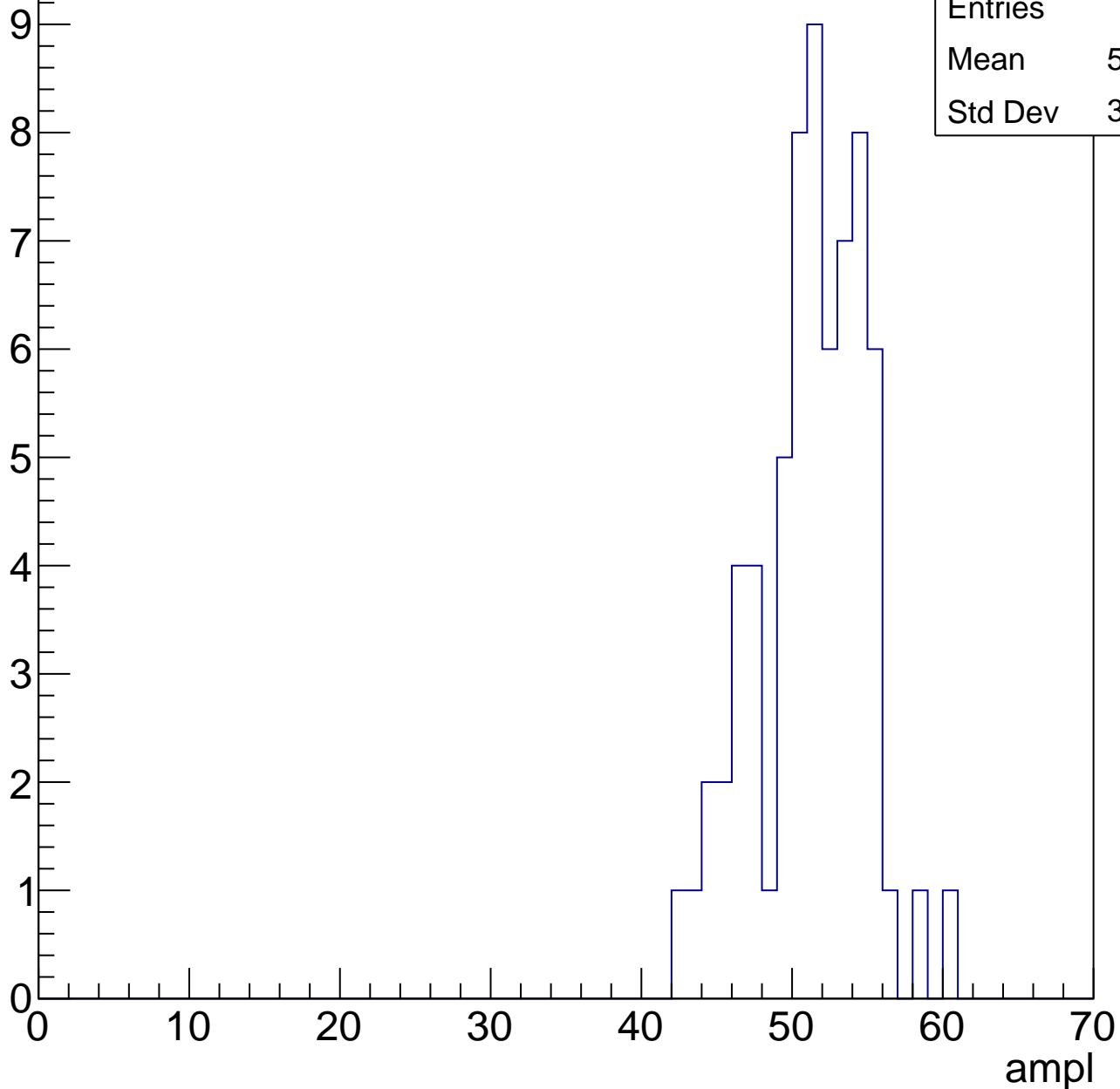


# B0L001S, U10-ch13, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	50.84
Std Dev	3.606

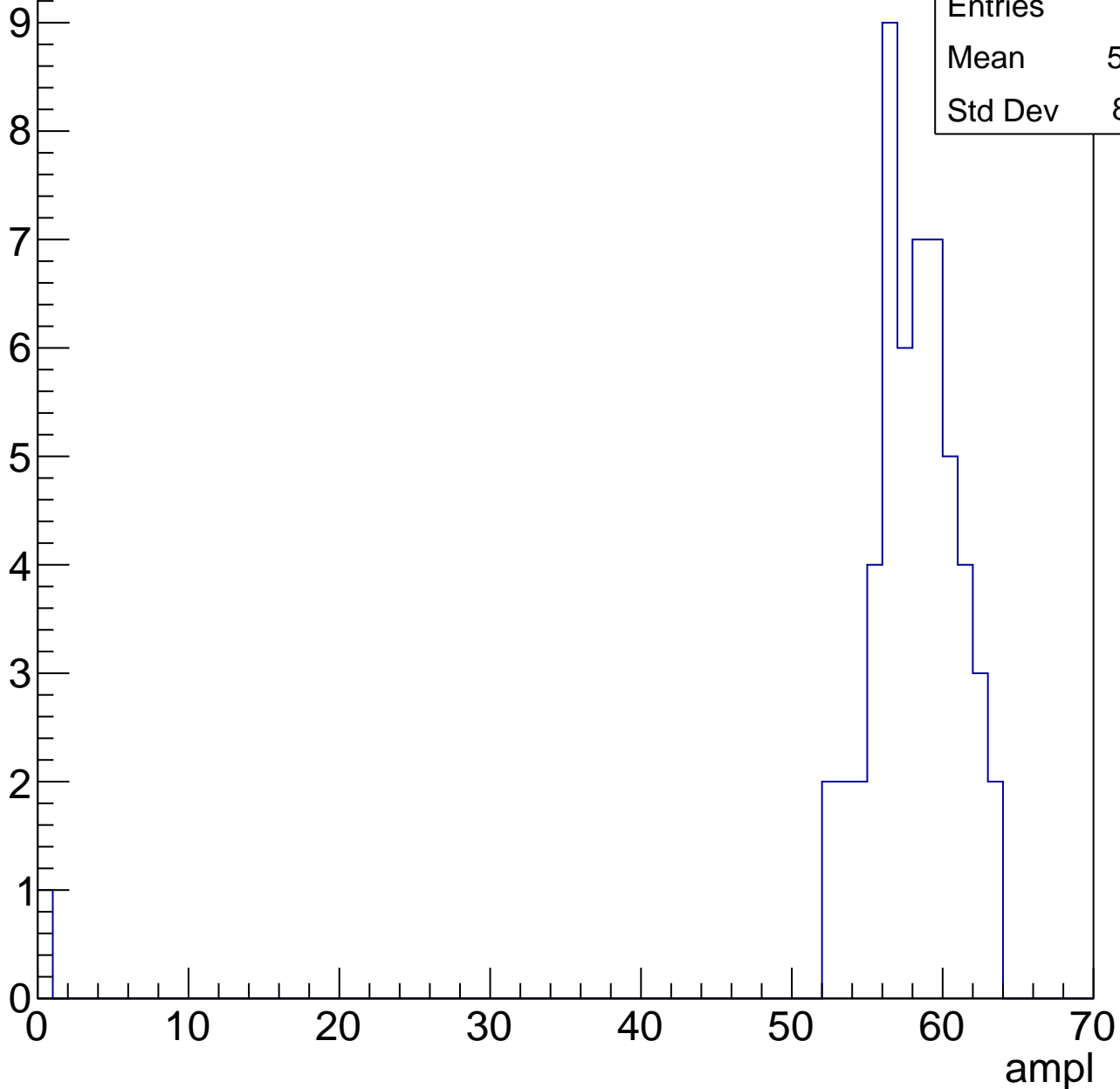


# B0L001S, U10-ch13, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	56.65
Std Dev	8.231

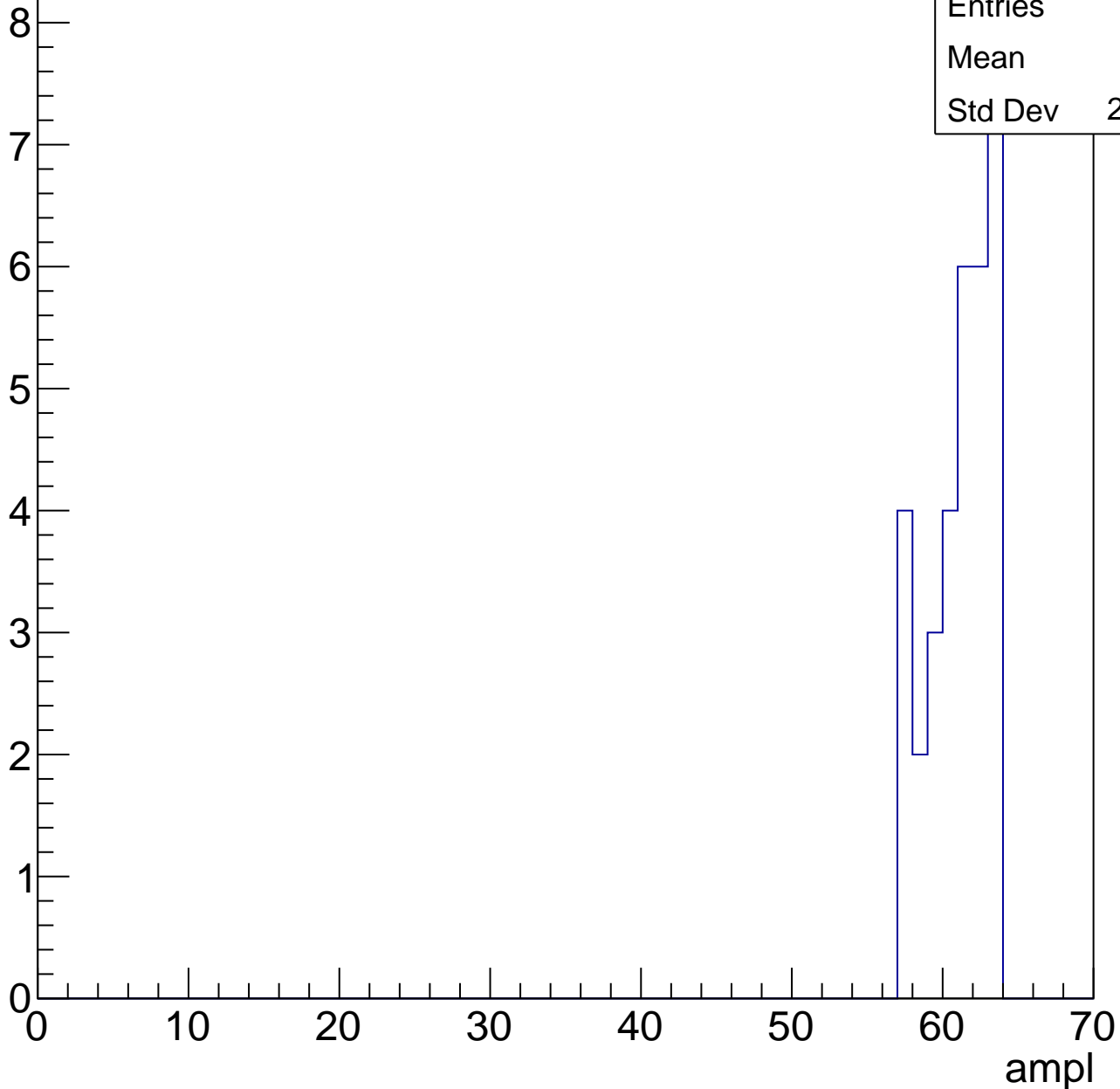


# B0L001S, U10-ch13, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	33
Mean	60.7
Std Dev	2.007



# B0L001S, U10-ch13, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch13, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U10-ch14, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	63
Mean	29.97
Std Dev	6.233

**Gaus mean : 31.4921**

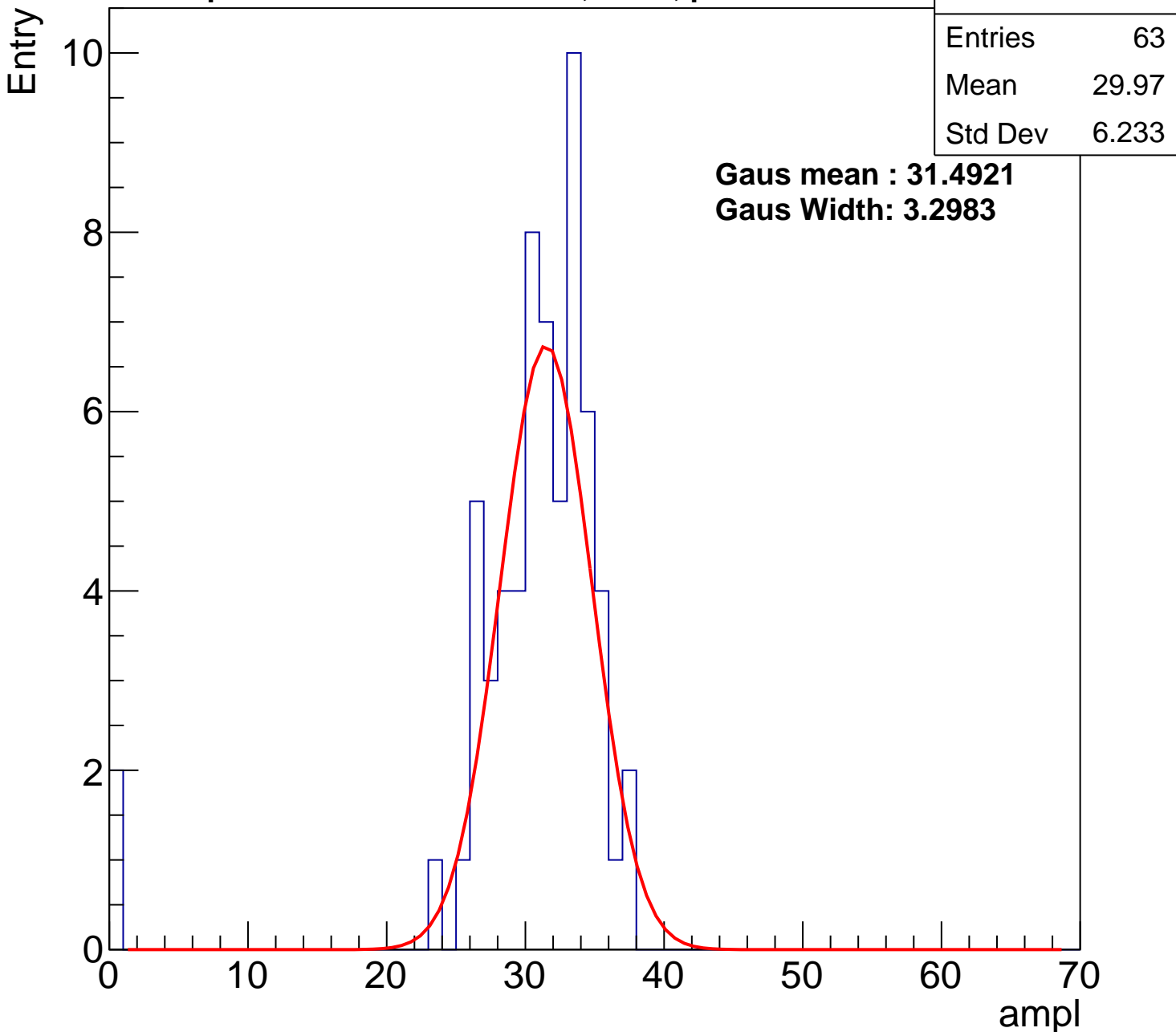
**Gaus Width: 3.2983**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



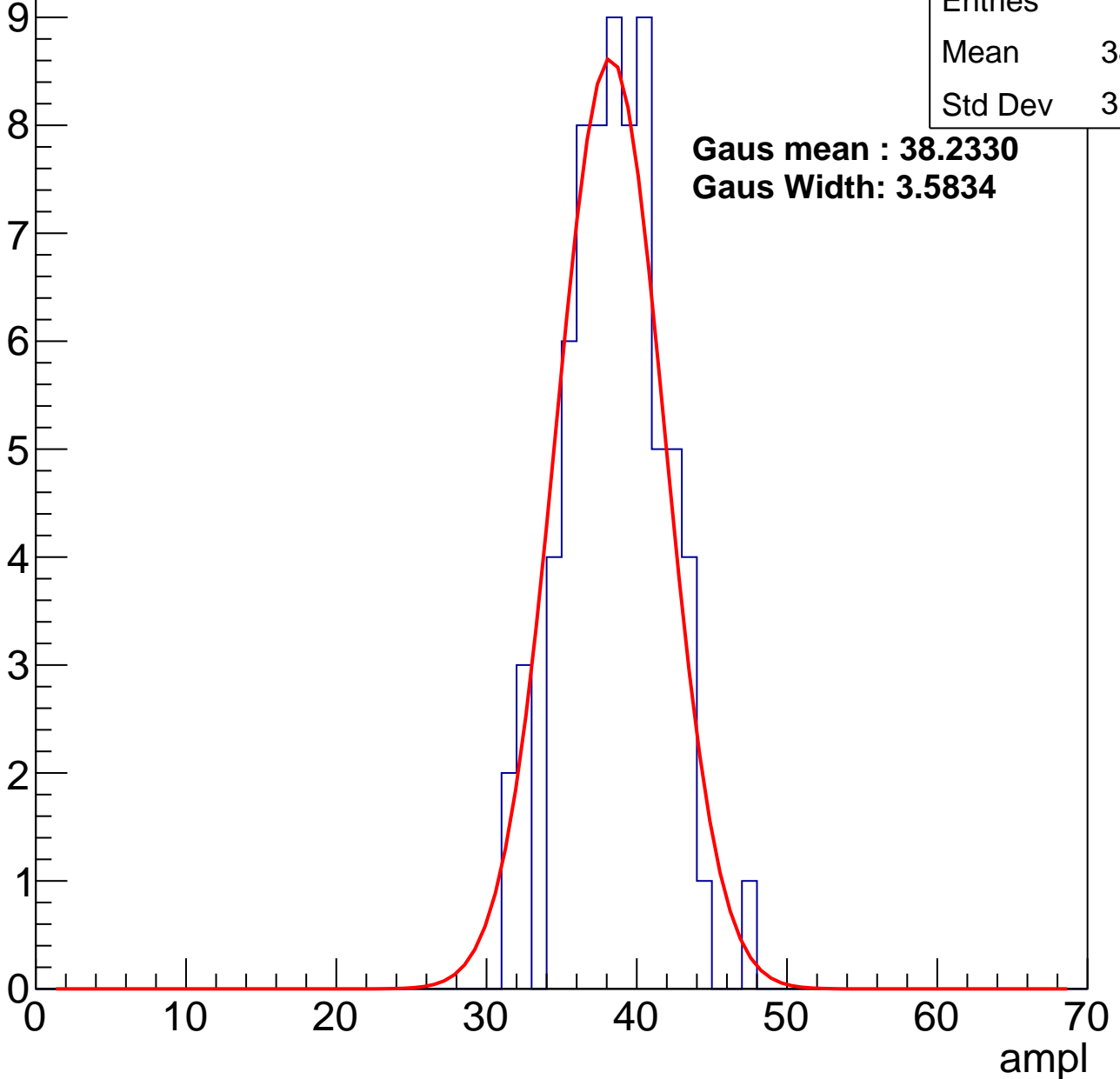
# B0L001S, U10-ch14, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	38.08
Std Dev	3.204

**Gaus mean : 38.2330**  
**Gaus Width: 3.5834**



# B0L001S, U10-ch14, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	81
Mean	45.65
Std Dev	3.563

**Gaus mean : 46.5595**

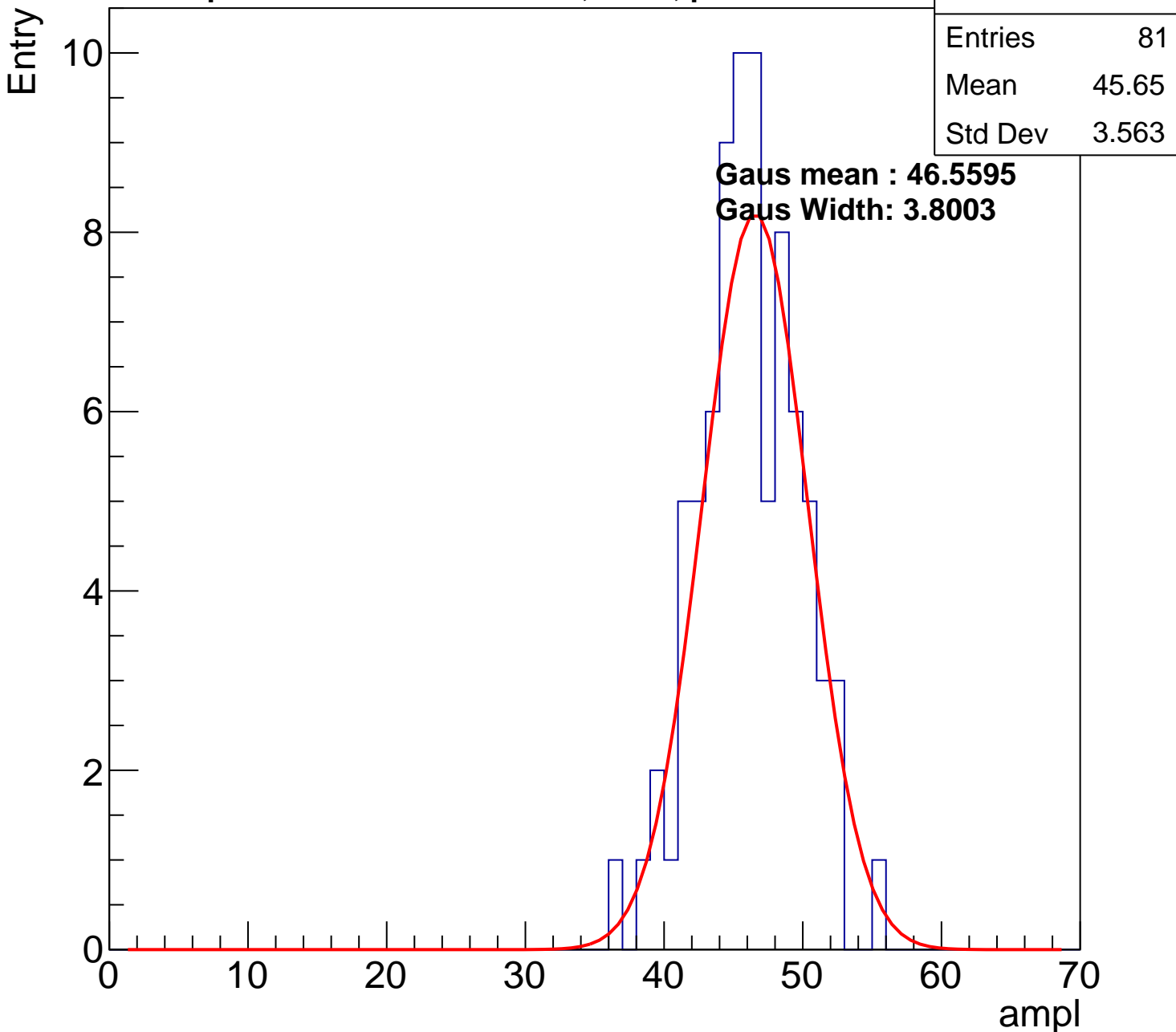
**Gaus Width: 3.8003**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

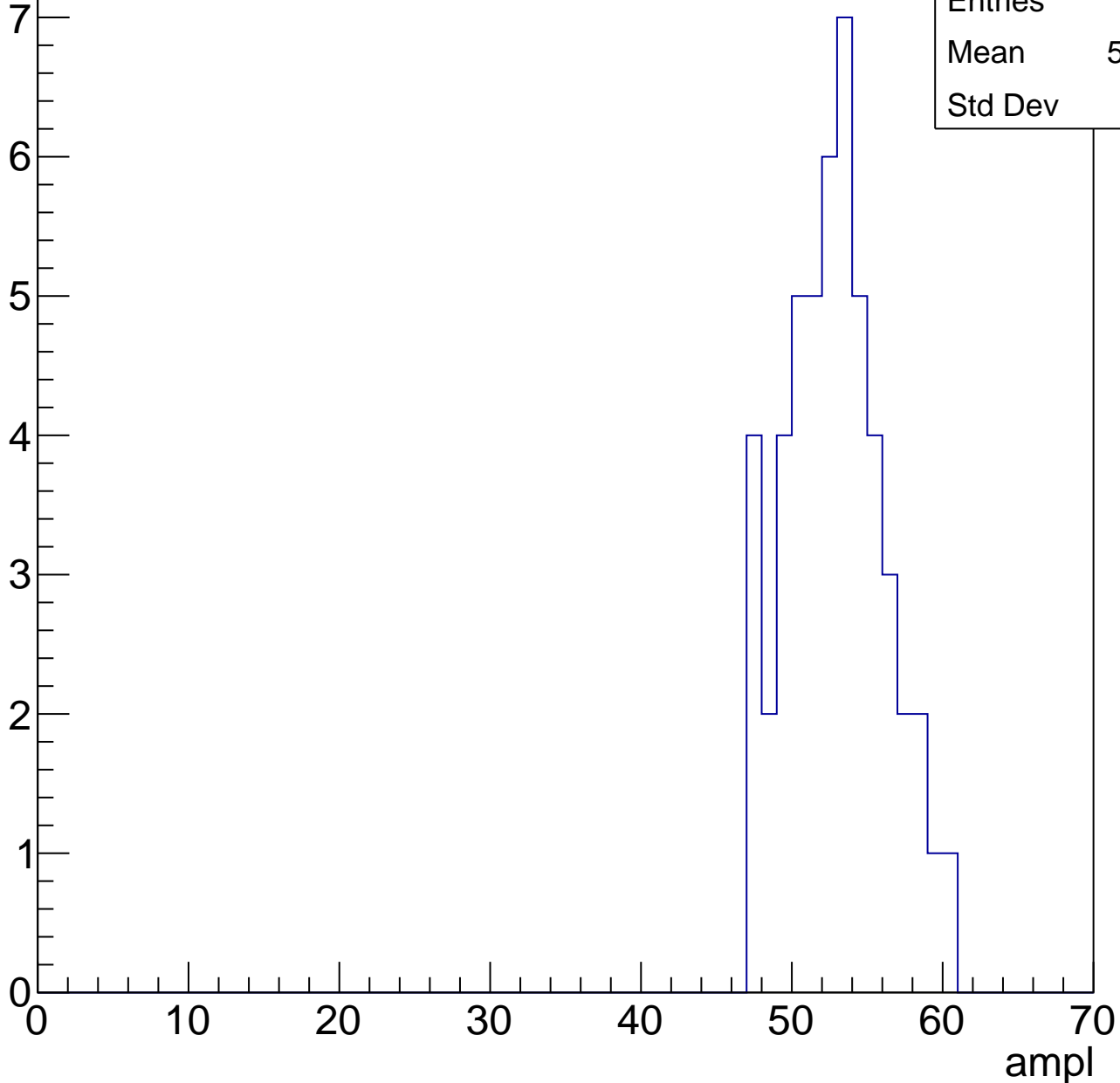


# B0L001S, U10-ch14, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

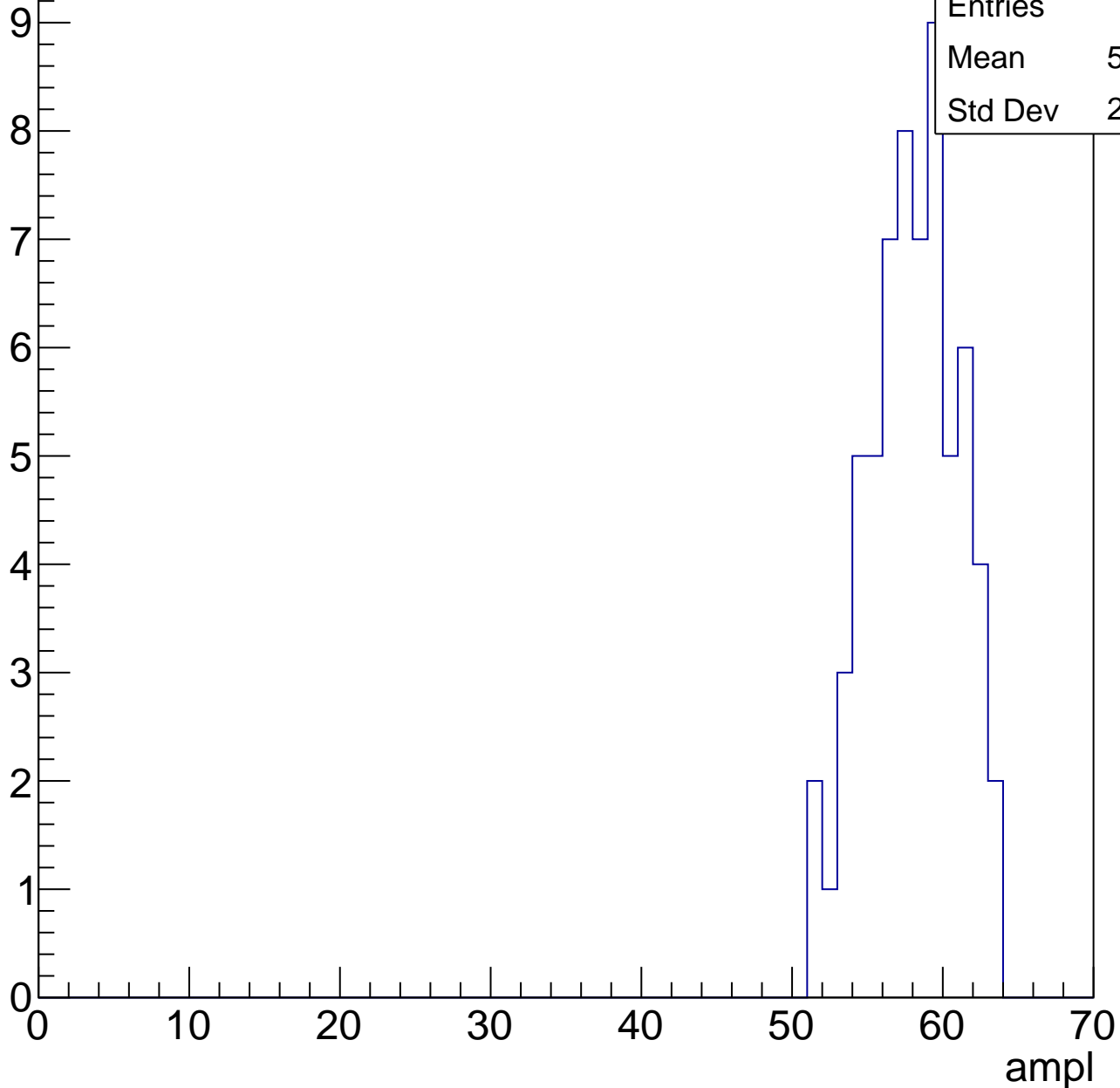
Entries	51
Mean	52.45
Std Dev	3.22



# B0L001S, U10-ch14, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

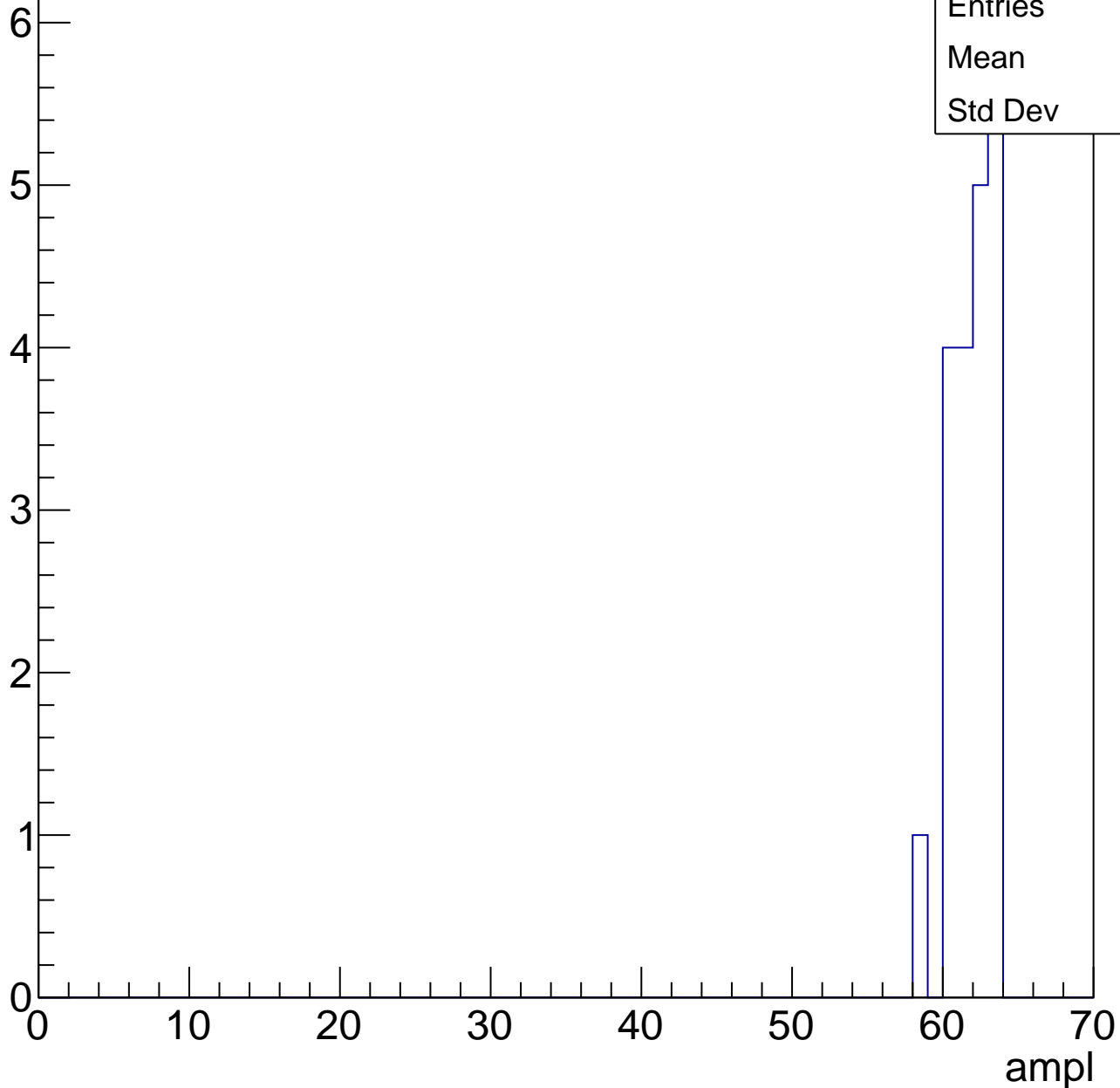


# B0L001S, U10-ch14, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	20
Mean	61.5
Std Dev	1.36



# B0L001S, U10-ch14, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch14, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U10-ch15, adc0

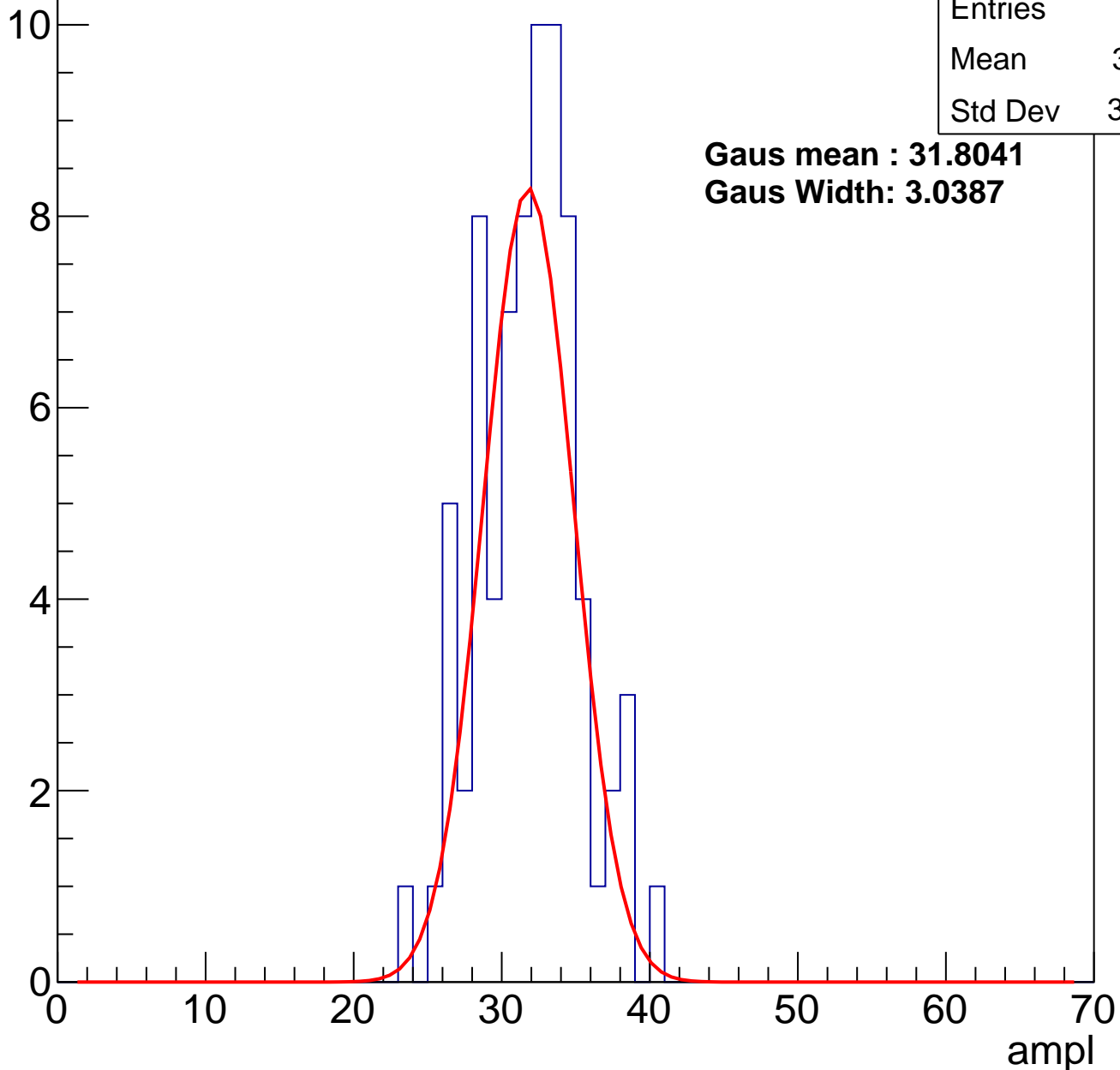
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	75
Mean	31.41
Std Dev	3.367

**Gaus mean : 31.8041**

**Gaus Width: 3.0387**

Entry



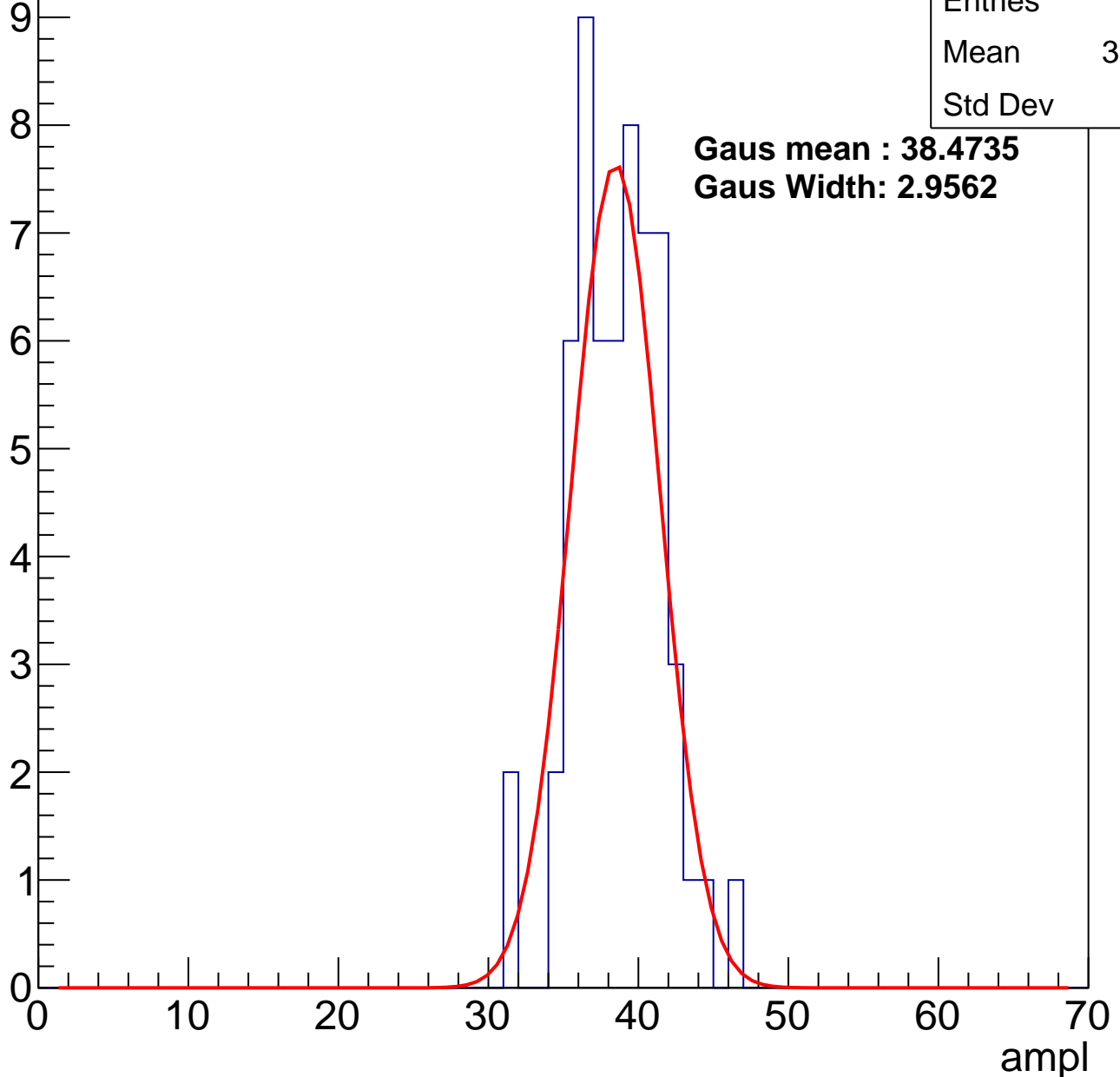
# B0L001S, U10-ch15, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	38.17
Std Dev	2.9

**Gaus mean : 38.4735**  
**Gaus Width: 2.9562**



# B0L001S, U10-ch15, adc2

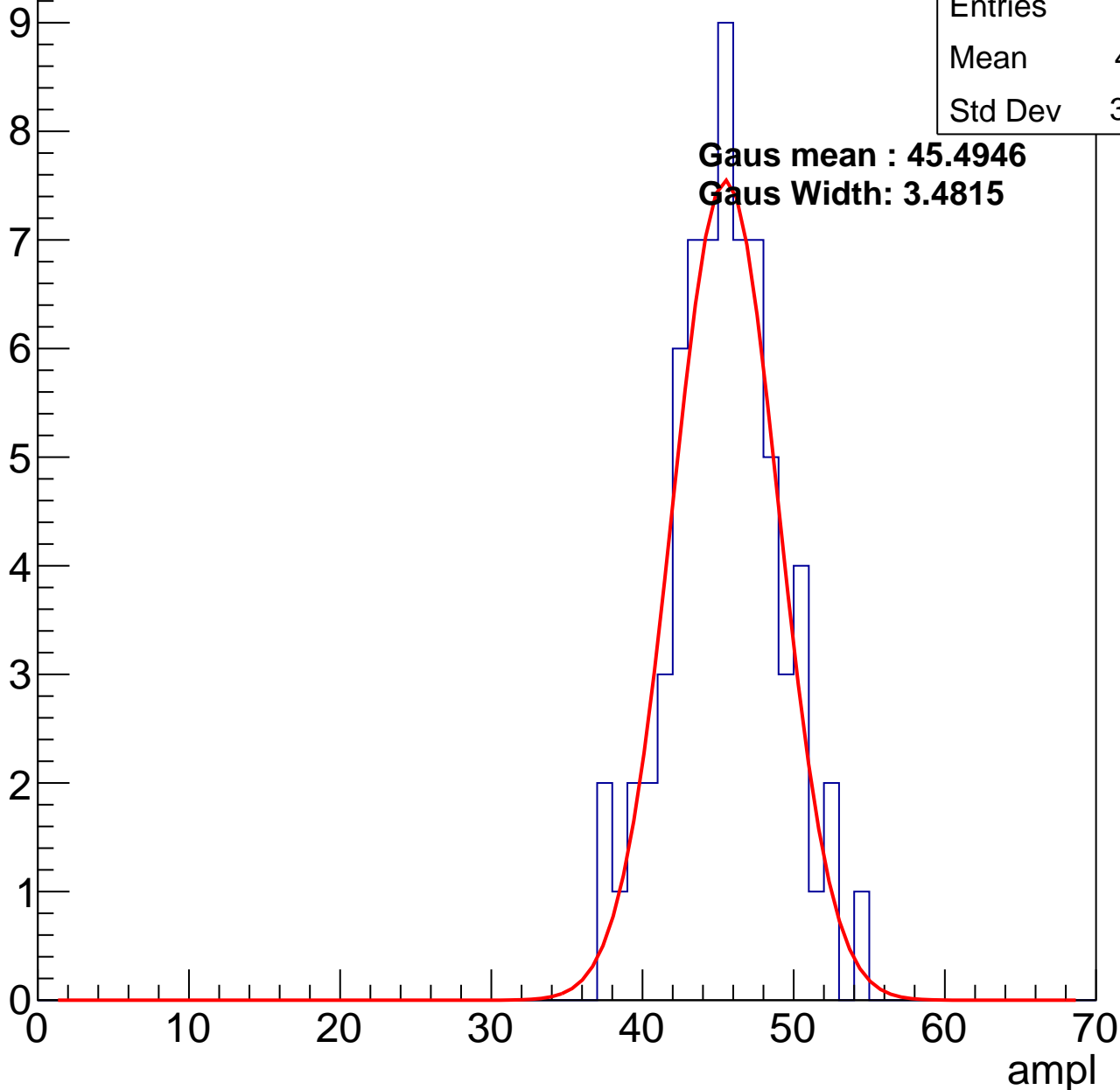
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	45.01
Std Dev	3.569

Gaus mean : 45.4946

Gaus Width: 3.4815

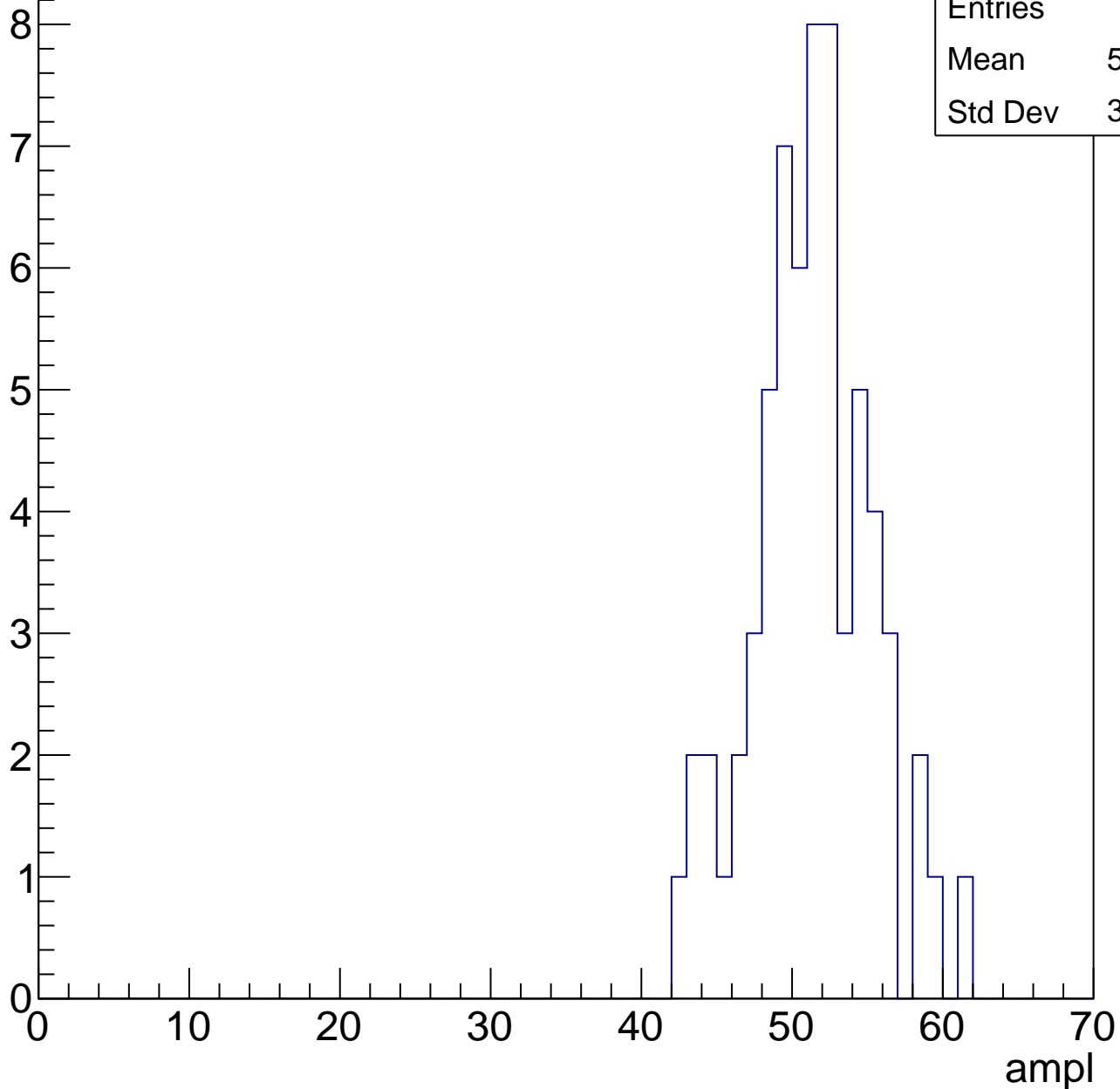


# B0L001S, U10-ch15, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

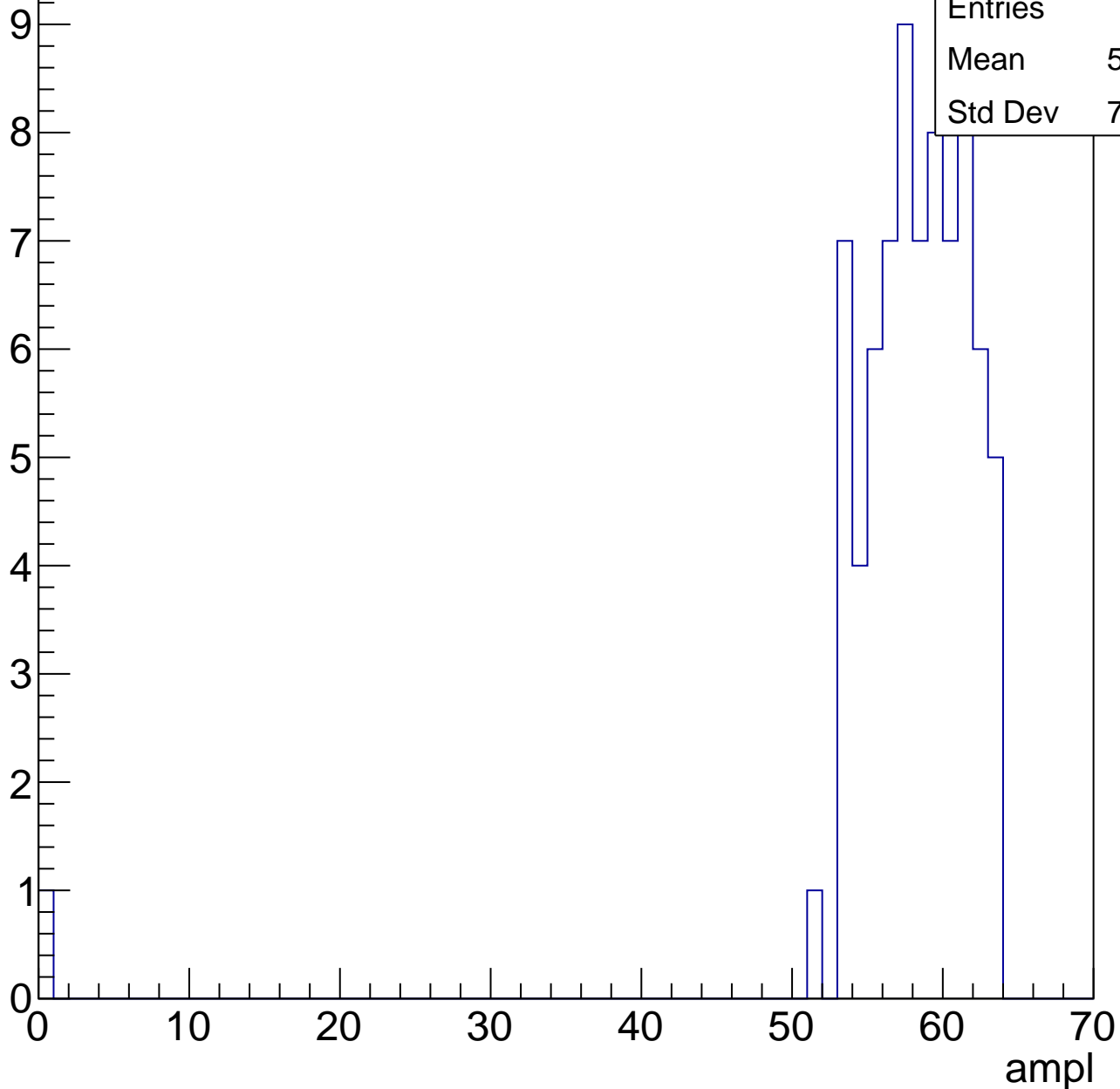
Entries	64
Mean	50.84
Std Dev	3.922



# B0L001S, U10-ch15, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

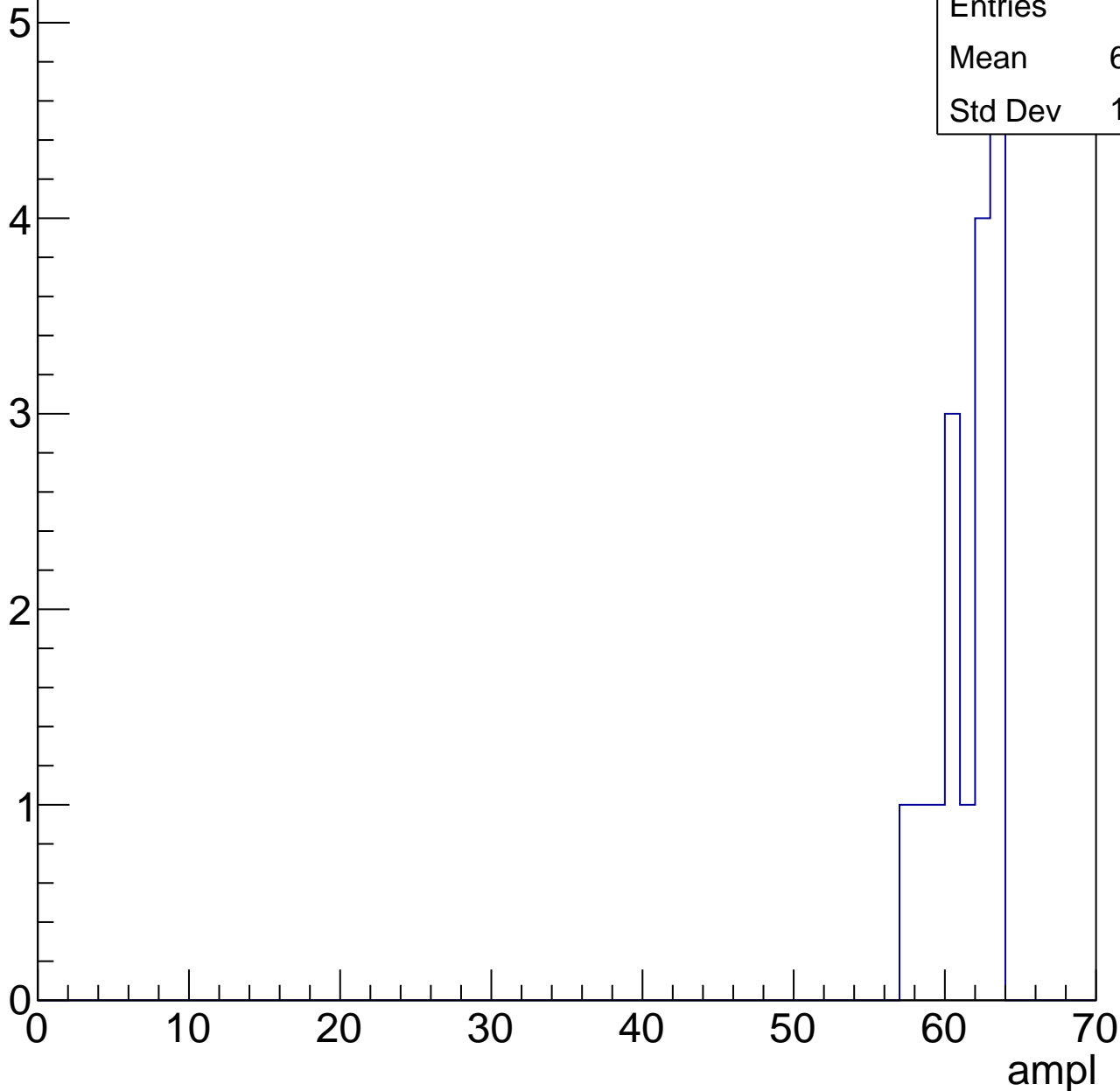


# B0L001S, U10-ch15, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	16
Mean	61.12
Std Dev	1.867



# B0L001S, U10-ch15, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U10-ch15, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U10-ch16, adc0

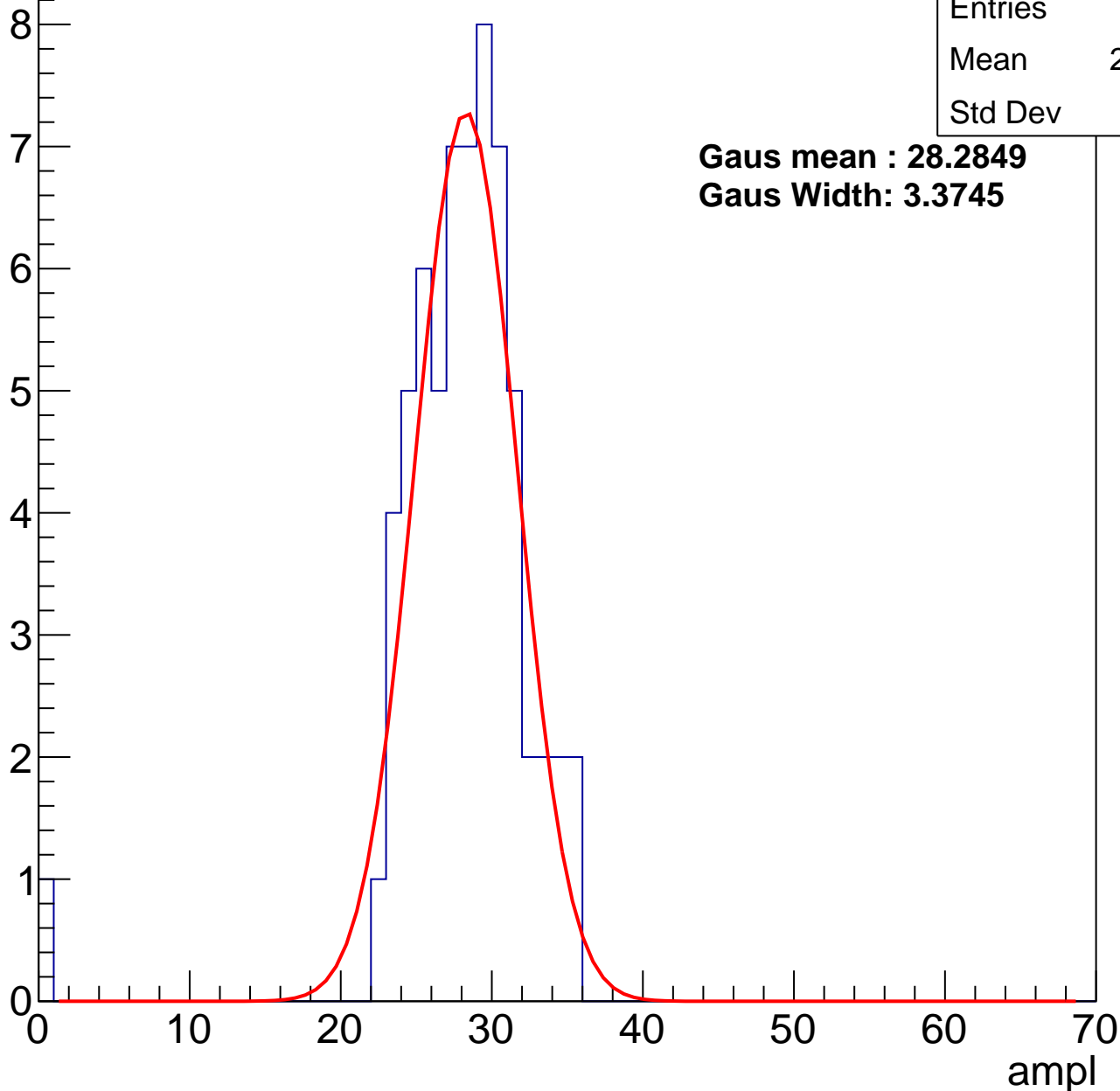
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	27.56
Std Dev	4.68

**Gaus mean : 28.2849**

**Gaus Width: 3.3745**



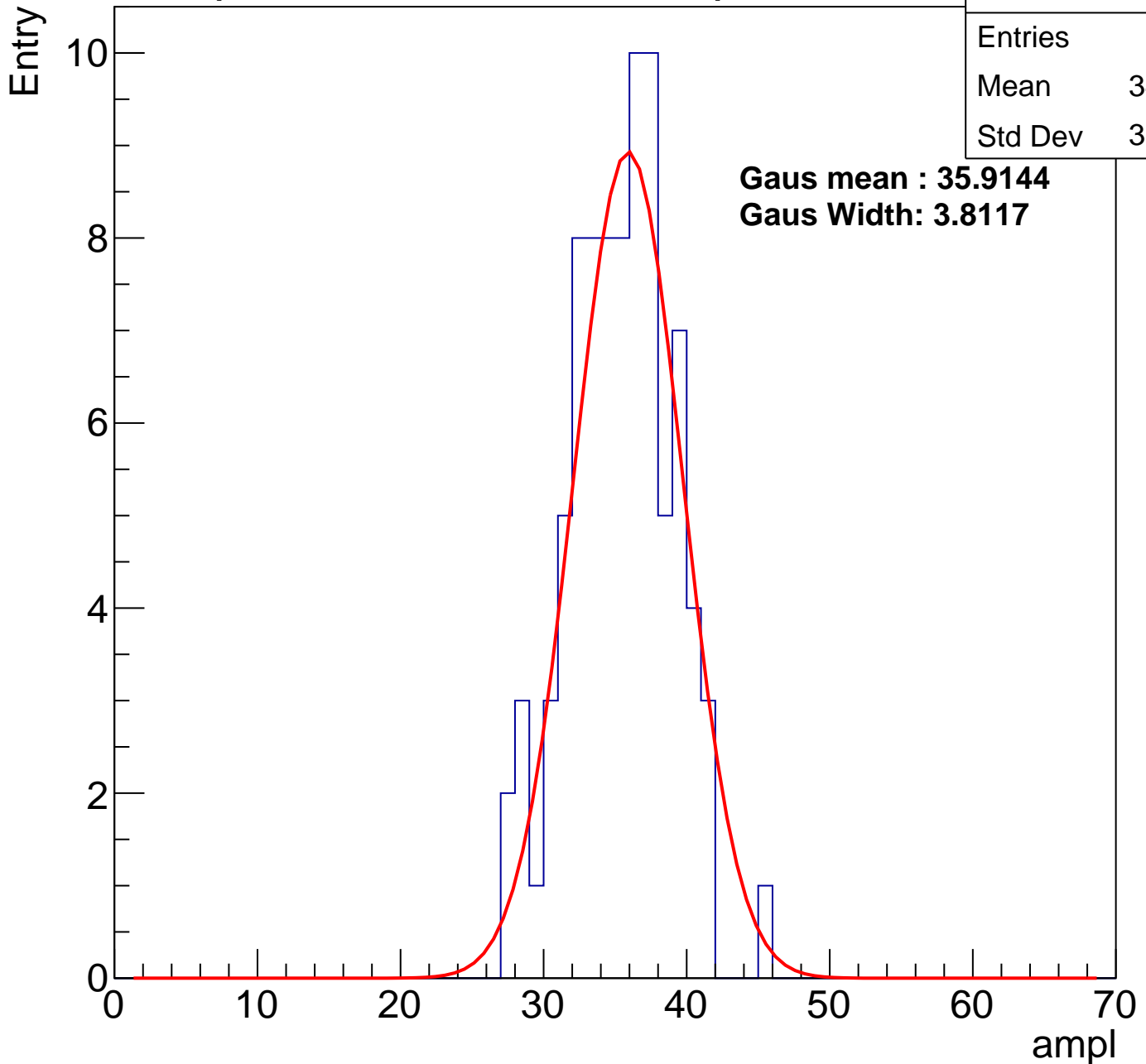
# B0L001S, U10-ch16, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	86
Mean	34.94
Std Dev	3.565

**Gaus mean : 35.9144**

**Gaus Width: 3.8117**



# B0L001S, U10-ch16, adc2

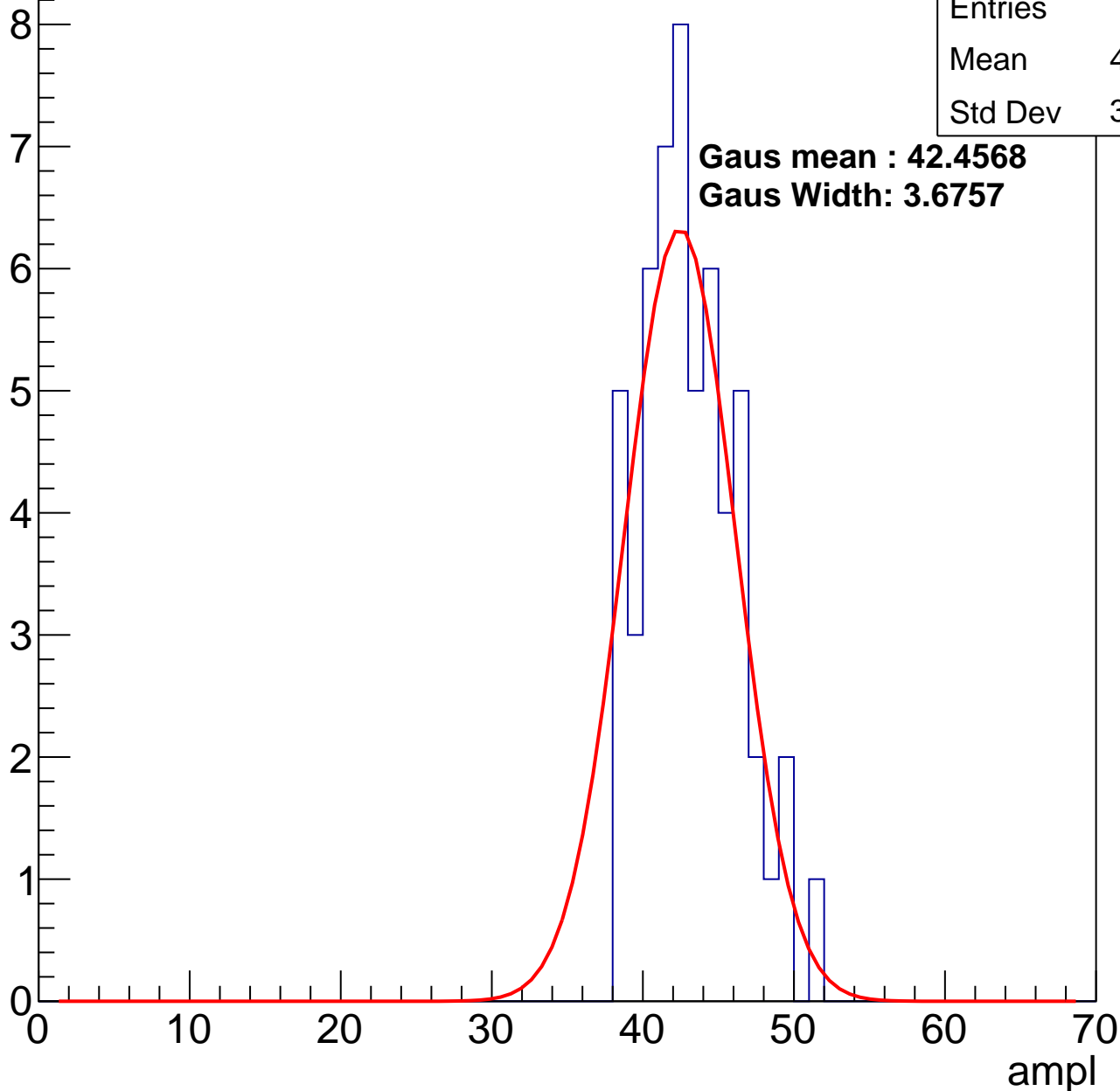
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	42.73
Std Dev	3.072

**Gaus mean : 42.4568**

**Gaus Width: 3.6757**



# B0L001S, U10-ch16, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	80
Mean	49
Std Dev	3.715

Entry

10

8

6

4

2

0

0

10

20

30

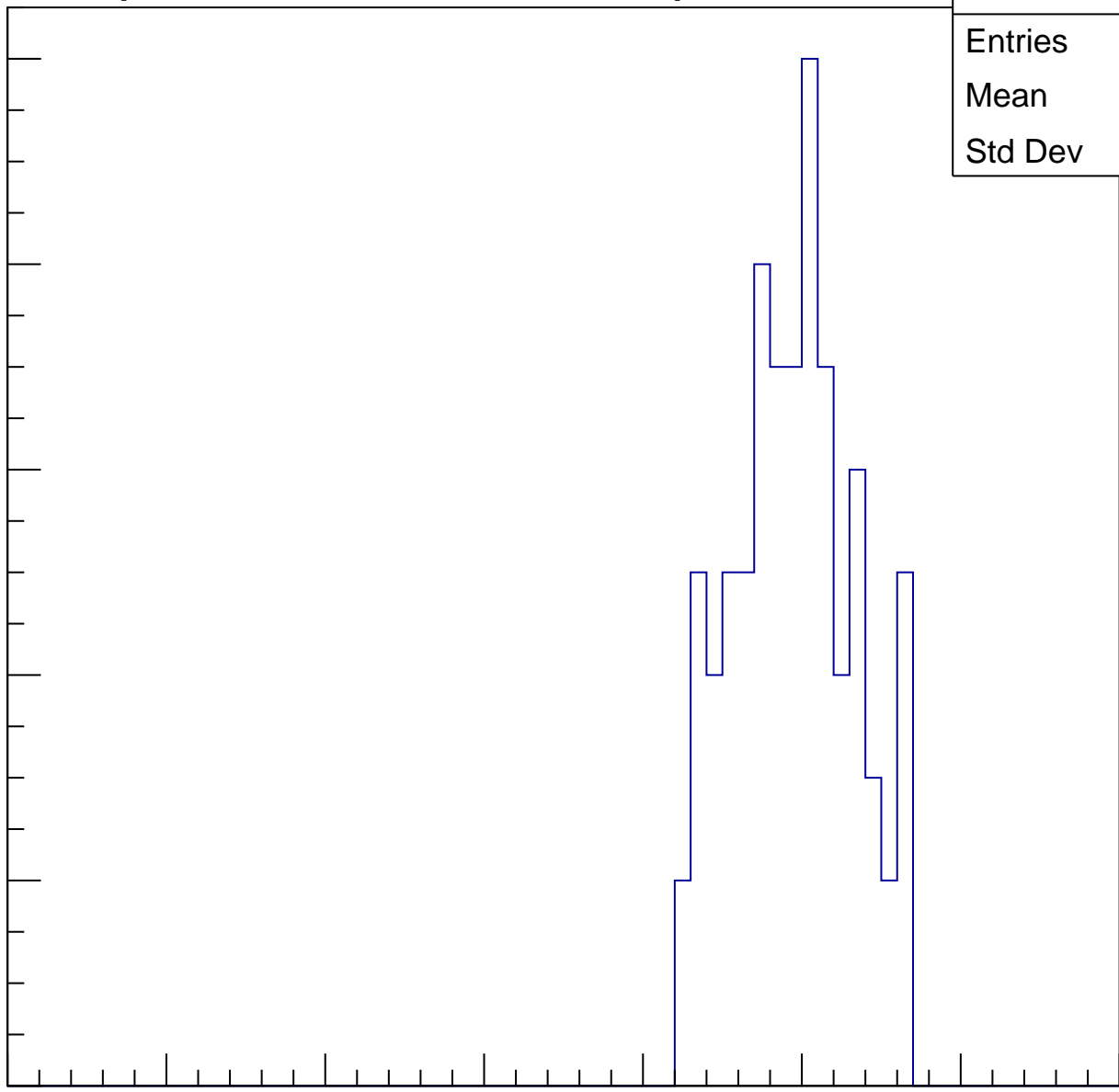
40

50

60

70

ampl

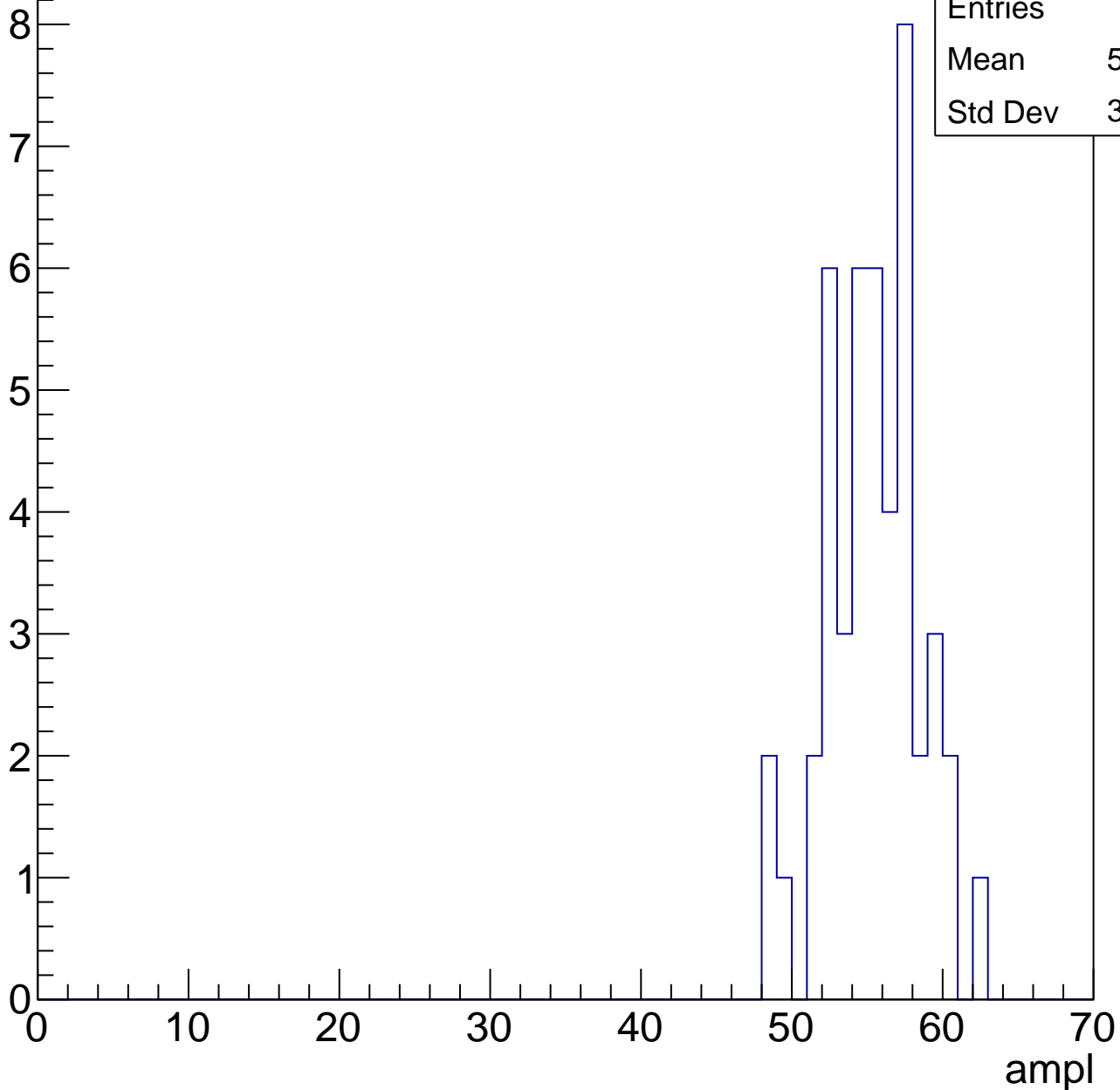


# B0L001S, U10-ch16, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	46
Mean	54.93
Std Dev	3.089

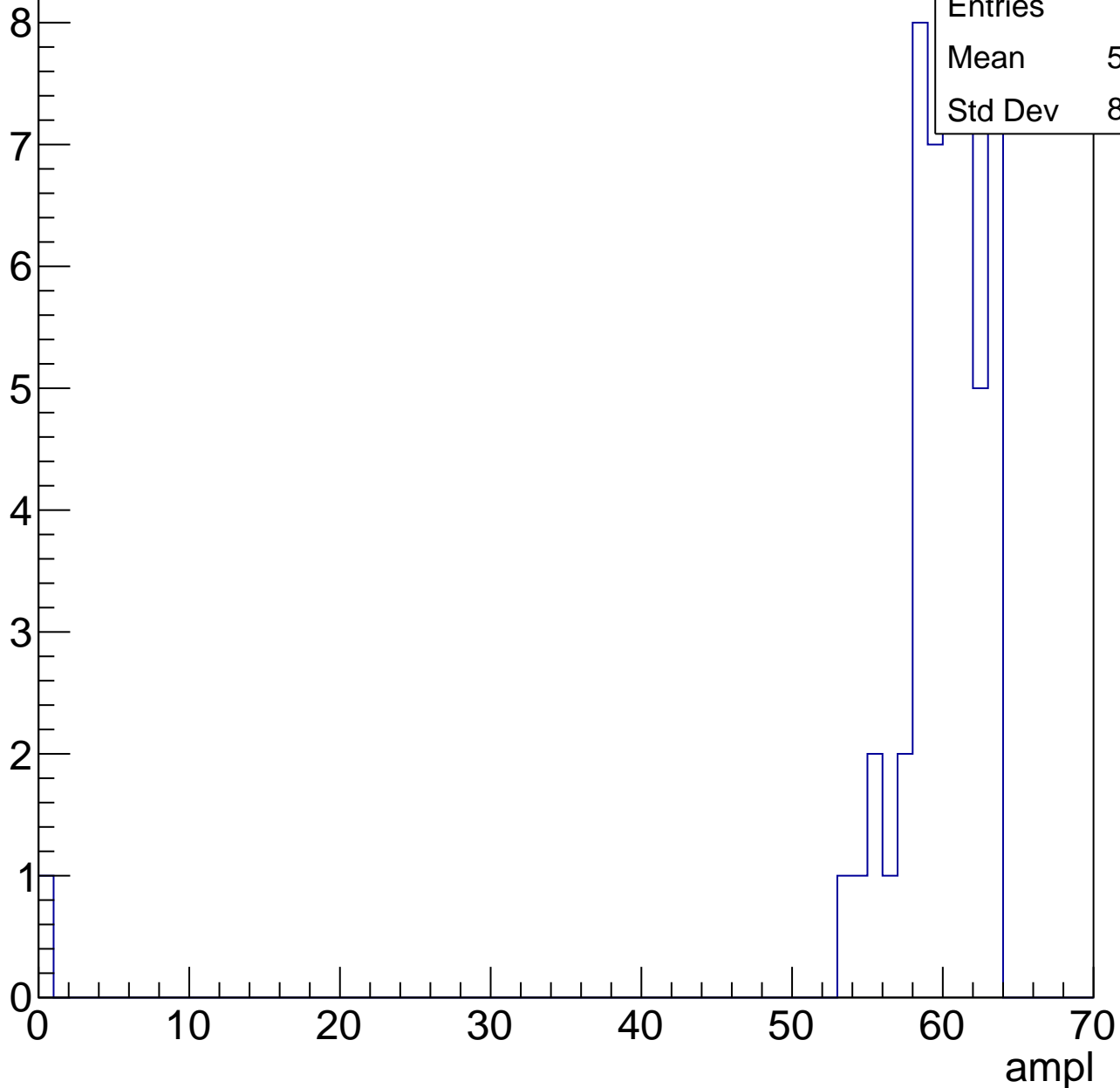


# B0L001S, U10-ch16, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

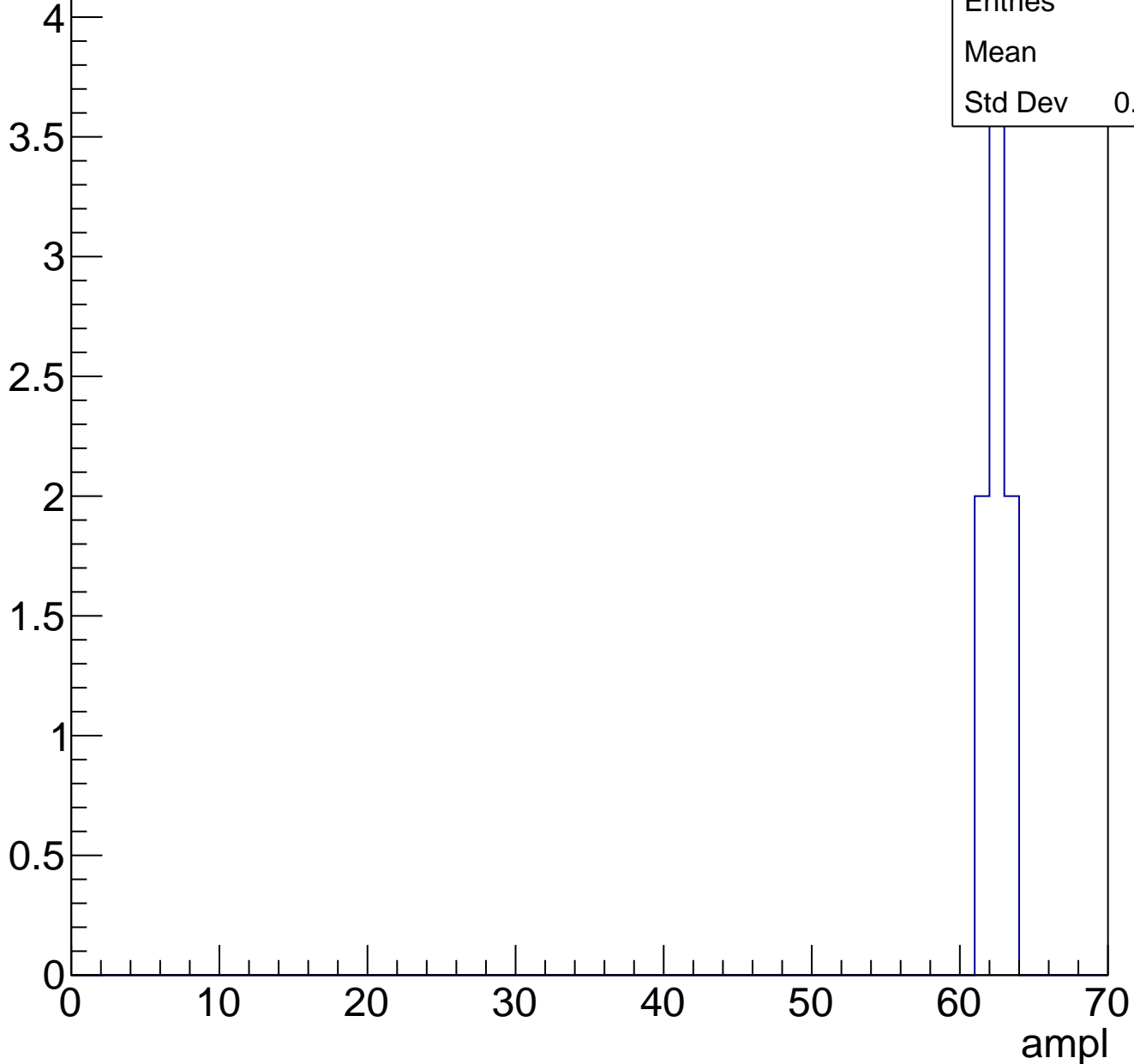
Entries	52
Mean	58.58
Std Dev	8.552



# B0L001S, U10-ch16, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch16, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U10-ch17, adc0

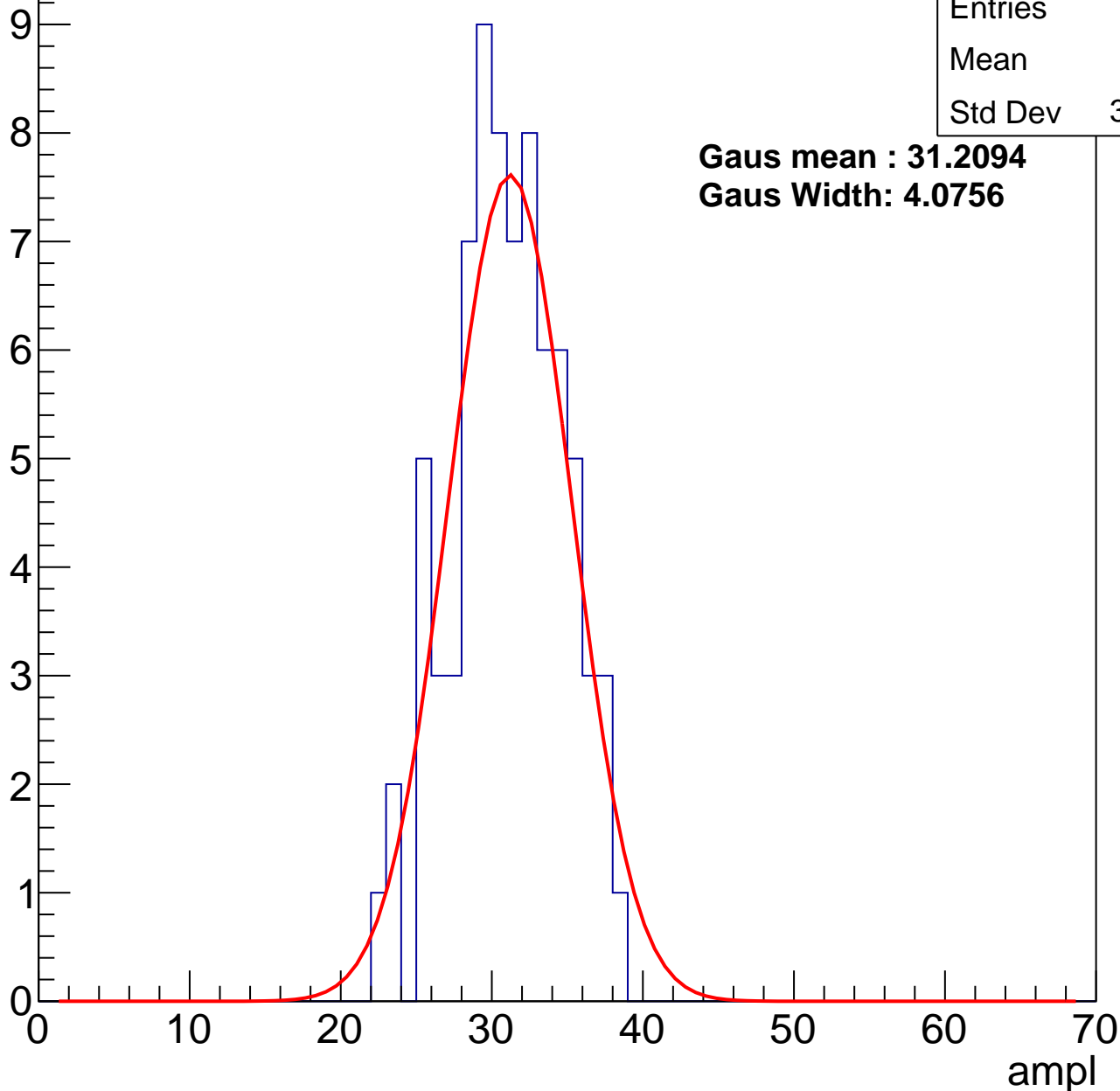
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	77
Mean	30.6
Std Dev	3.612

**Gaus mean : 31.2094**

**Gaus Width: 4.0756**



# B0L001S, U10-ch17, adc1

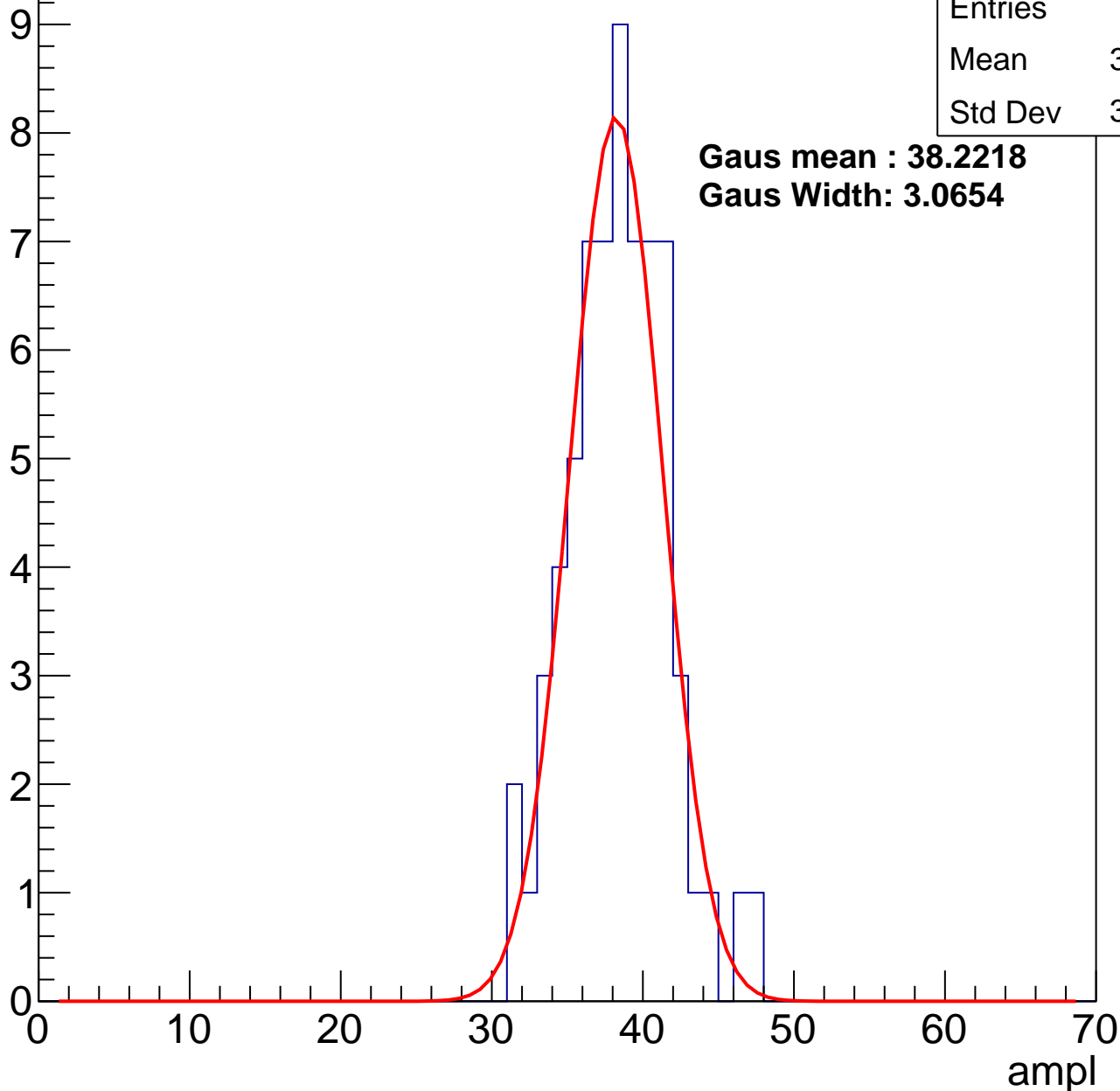
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	37.92
Std Dev	3.267

**Gaus mean : 38.2218**

**Gaus Width: 3.0654**



# B0L001S, U10-ch17, adc2

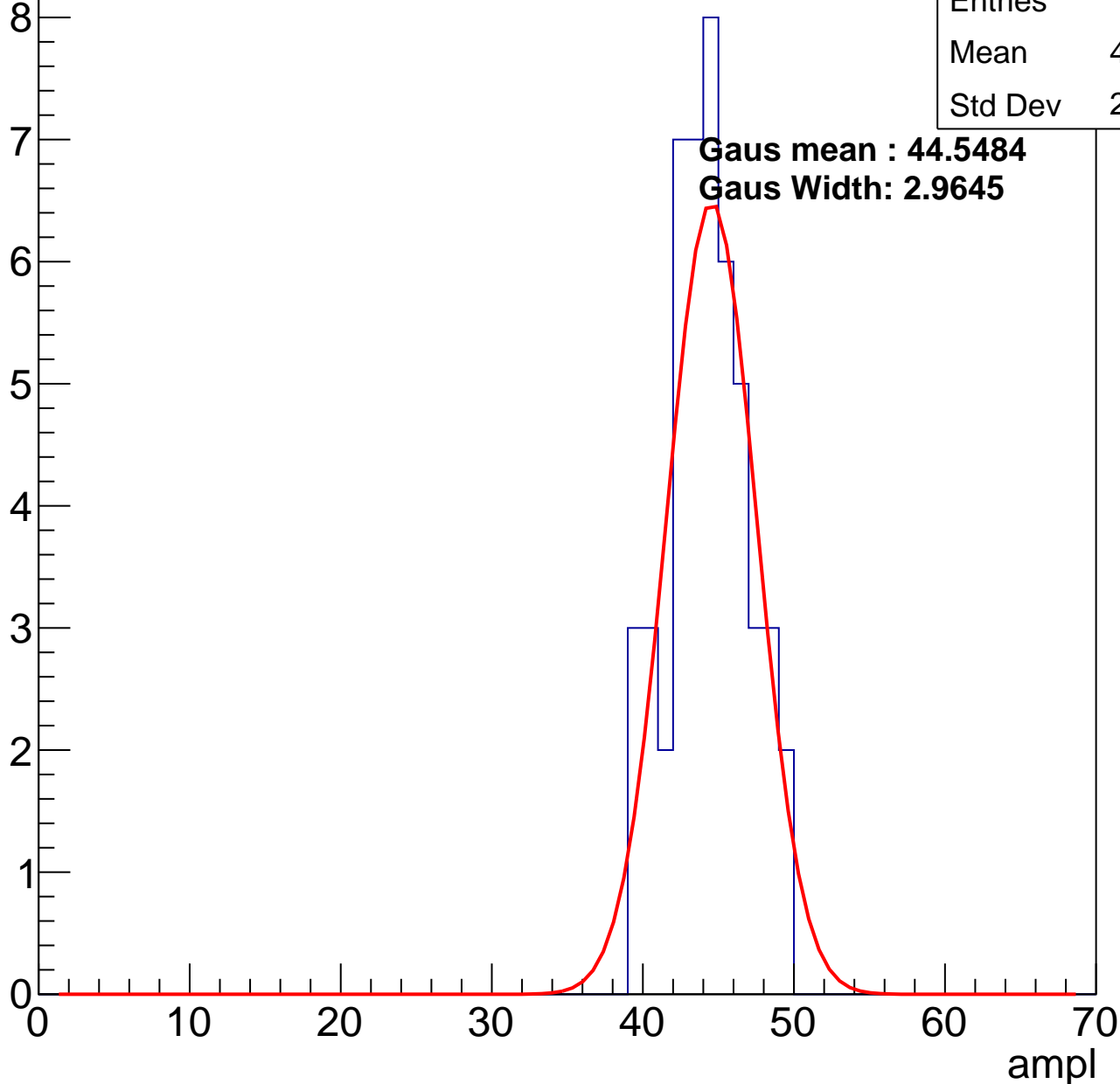
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	49
Mean	43.86
Std Dev	2.579

**Gaus mean : 44.5484**

**Gaus Width: 2.9645**



# B0L001S, U10-ch17, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	77
Mean	50.23
Std Dev	3.664

Entry

10

8

6

4

2

0

0

10

20

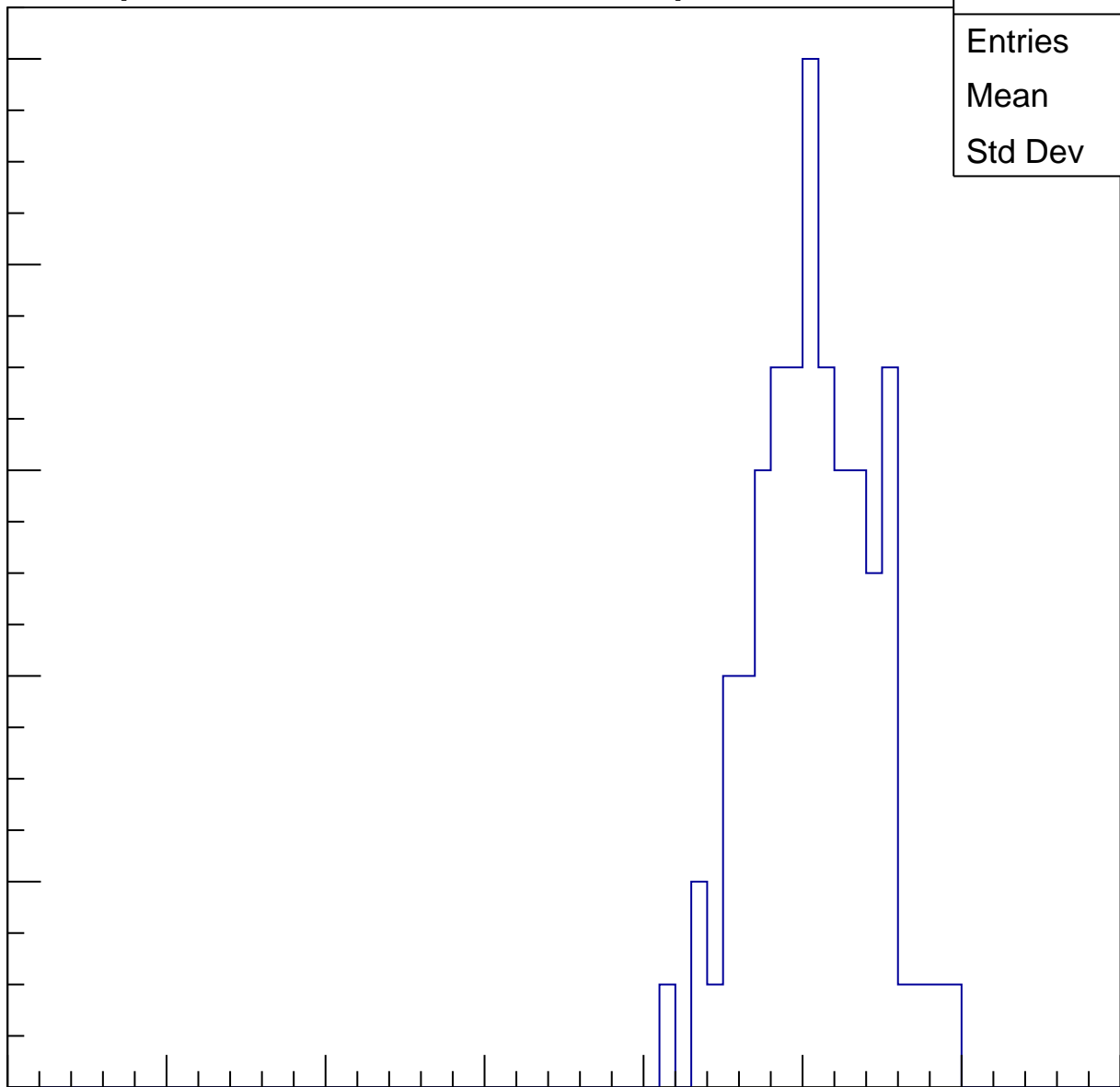
30

40

50

60

ampl

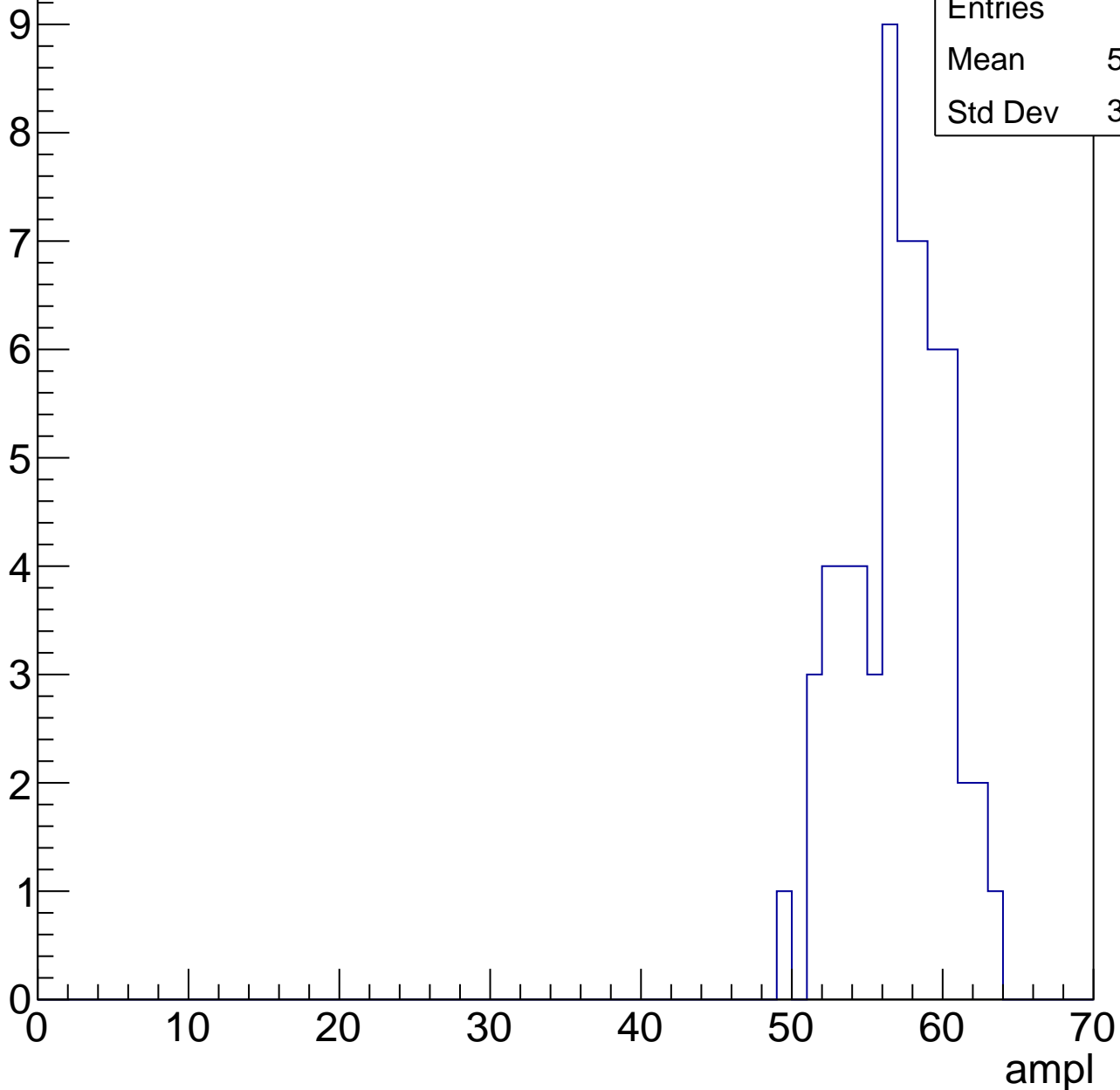


# B0L001S, U10-ch17, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	56.53
Std Dev	3.143

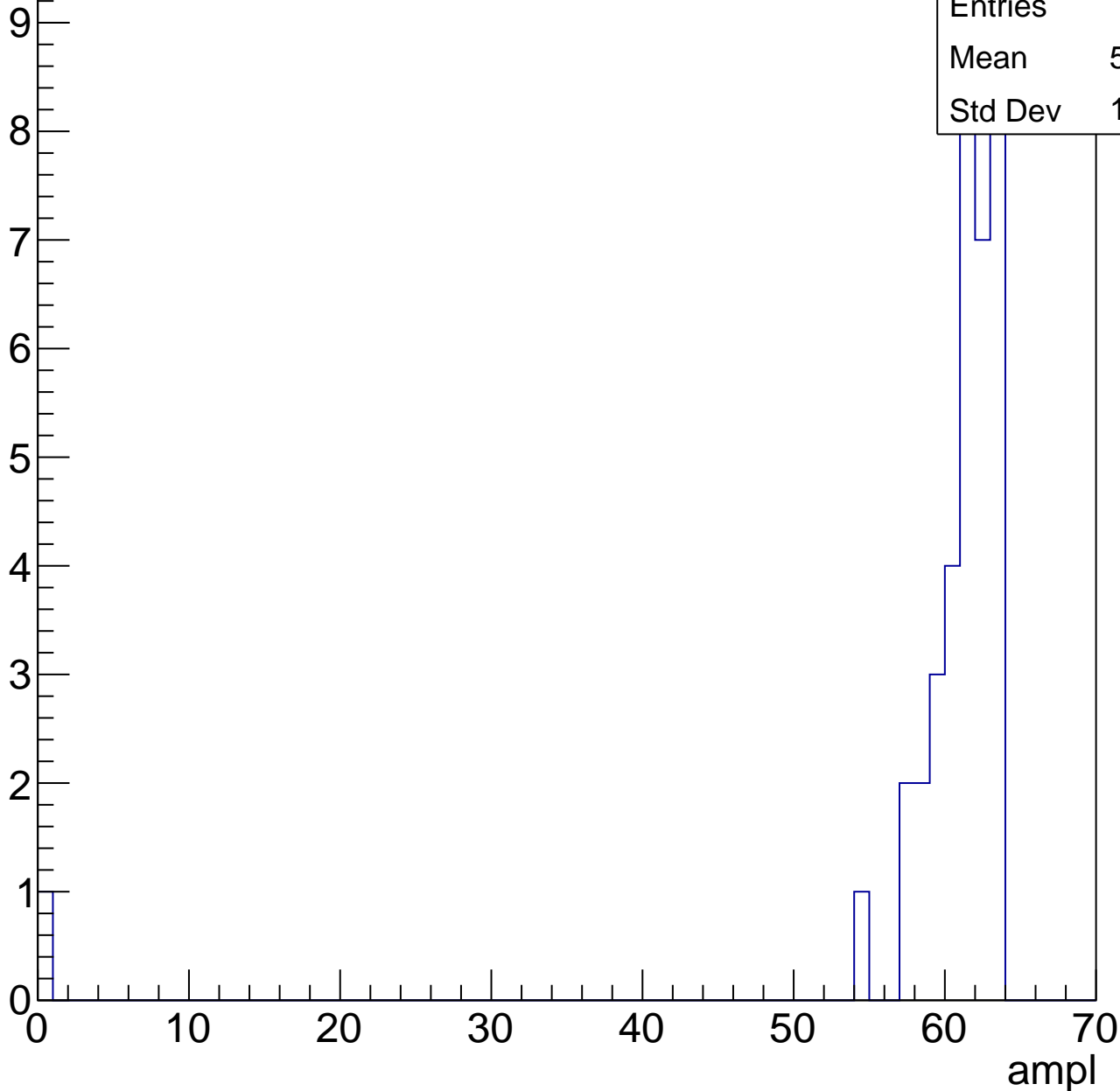


# B0L001S, U10-ch17, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	37
Mean	59.19
Std Dev	10.08



# B0L001S, U10-ch17, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch17, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U10-ch18, adc0

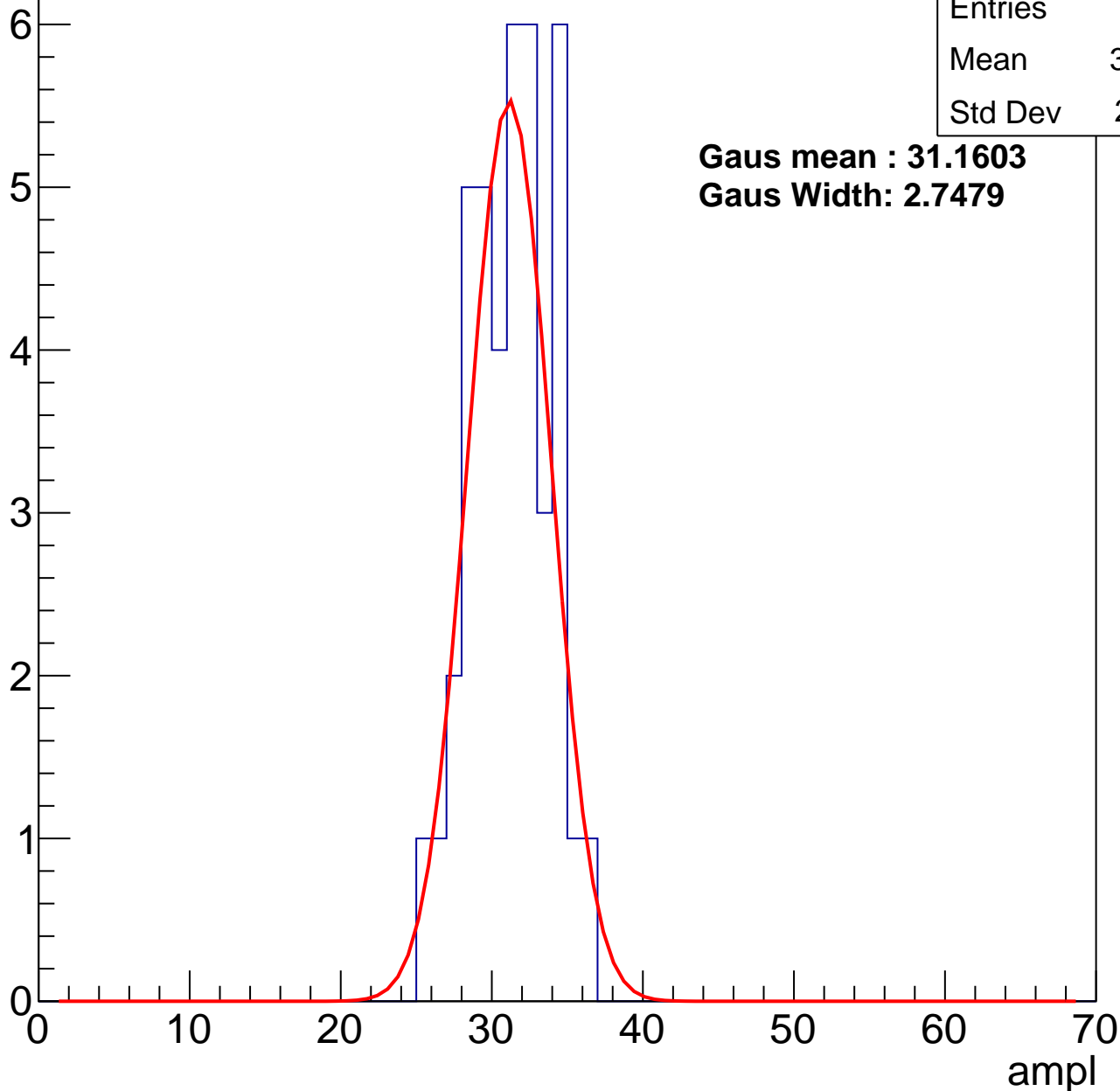
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	41
Mean	30.78
Std Dev	2.581

**Gaus mean : 31.1603**

**Gaus Width: 2.7479**



# B0L001S, U10-ch18, adc1

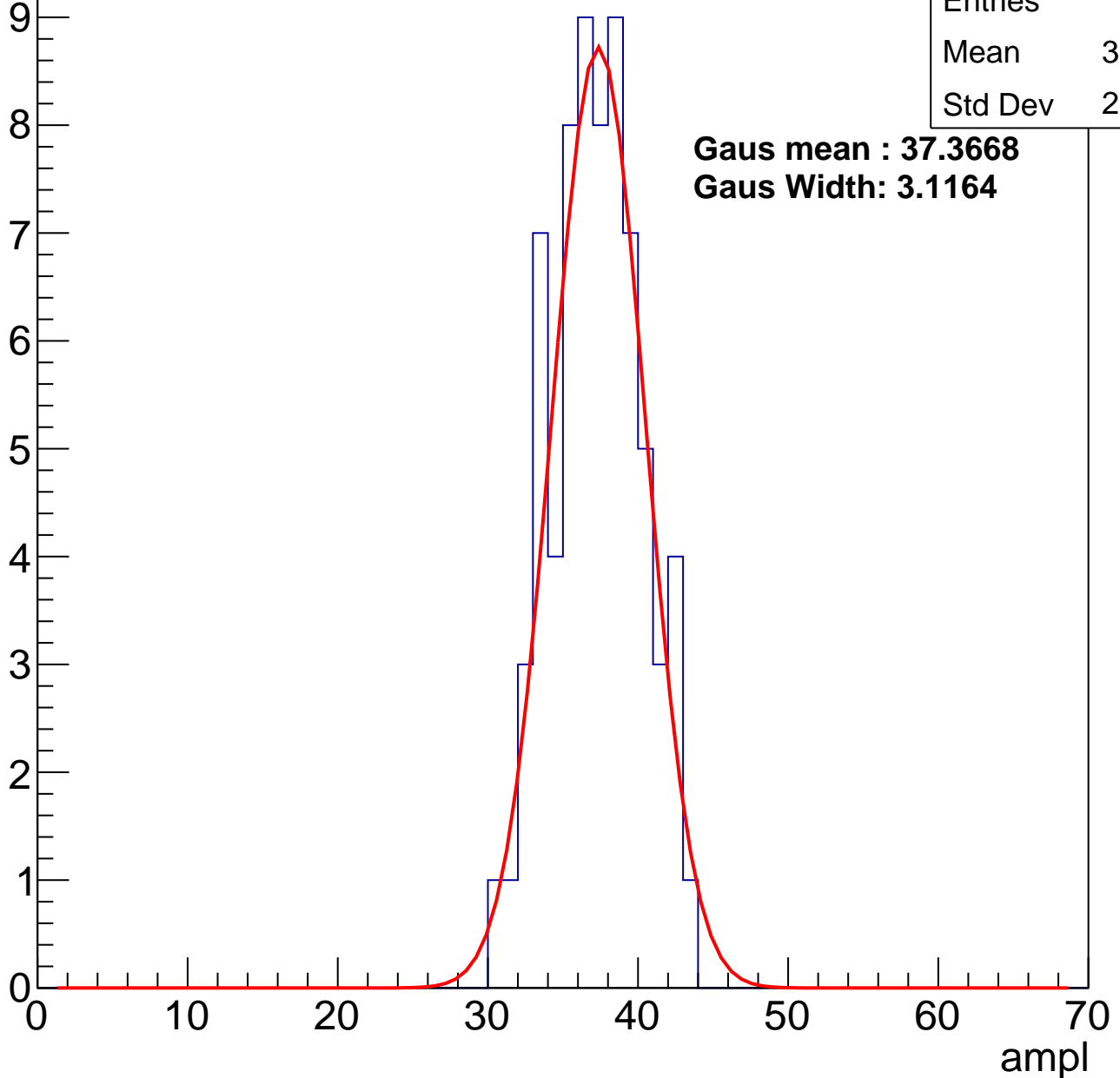
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	36.76
Std Dev	2.954

**Gaus mean : 37.3668**

**Gaus Width: 3.1164**



# B0L001S, U10-ch18, adc2

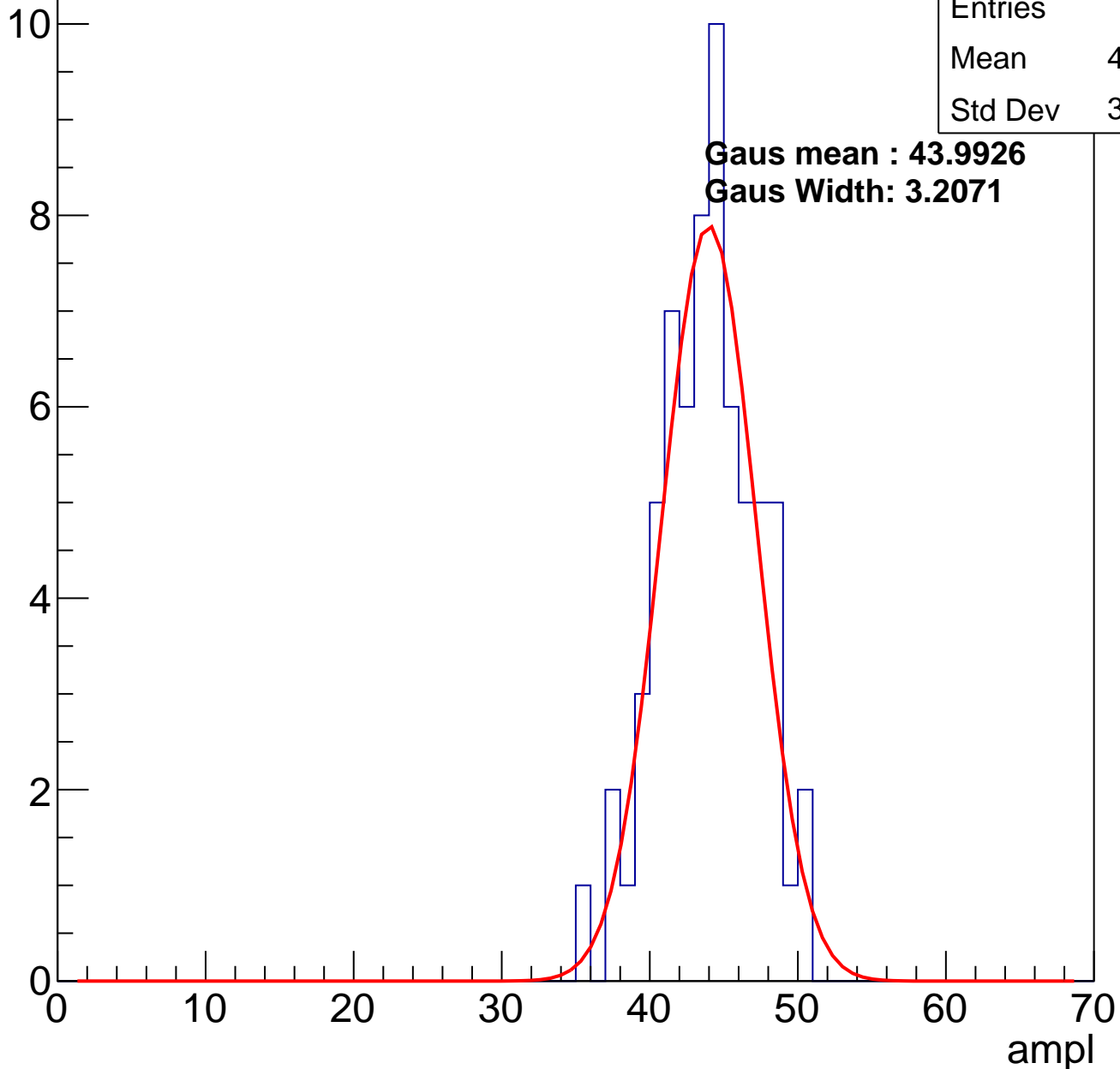
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	67
Mean	43.45
Std Dev	3.215

**Gaus mean : 43.9926**

**Gaus Width: 3.2071**

Entry



# B0L001S, U10-ch18, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	77
Mean	50.75
Std Dev	3.546

Entry

10

8

6

4

2

0

0

10

20

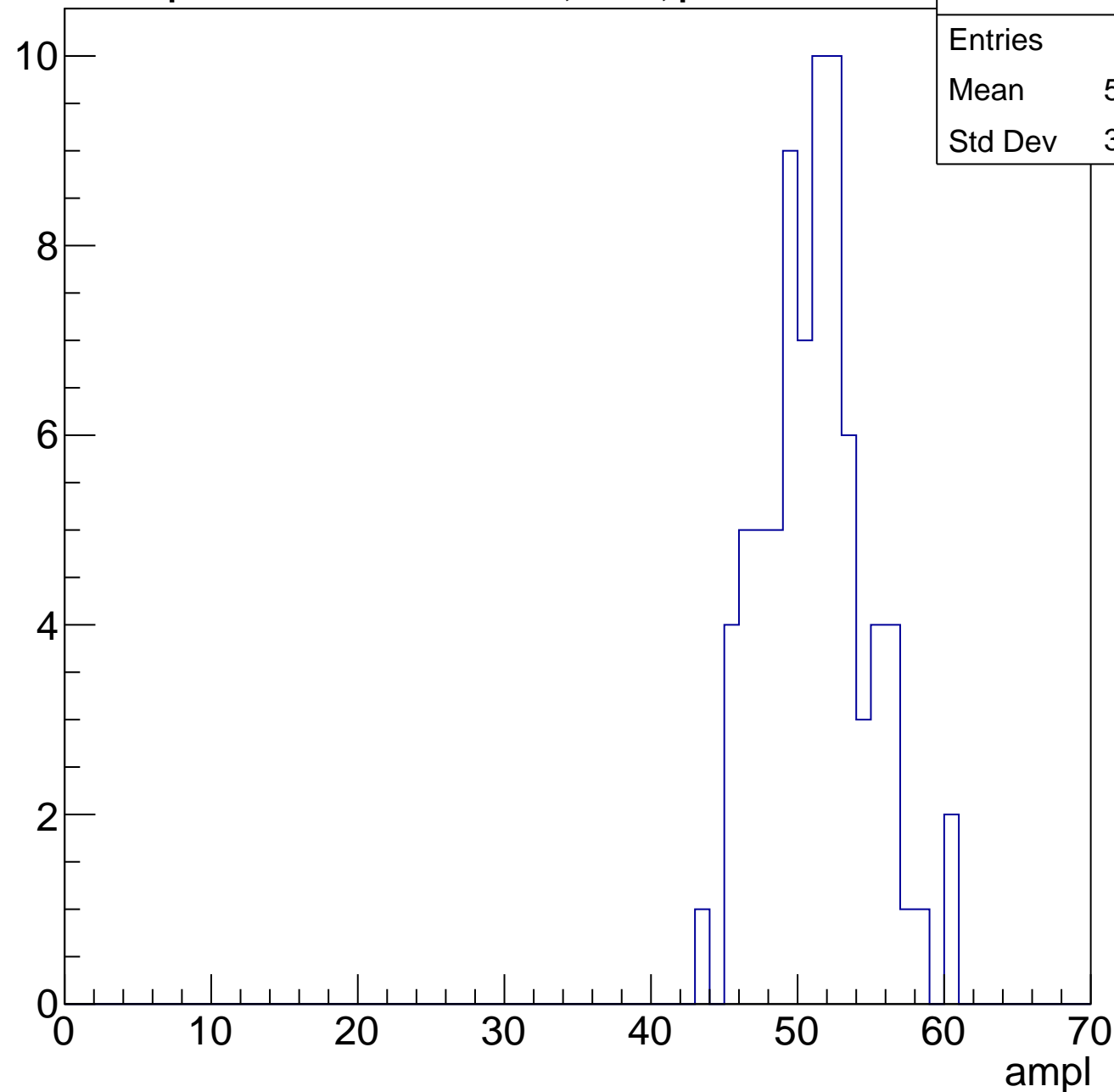
30

40

50

60

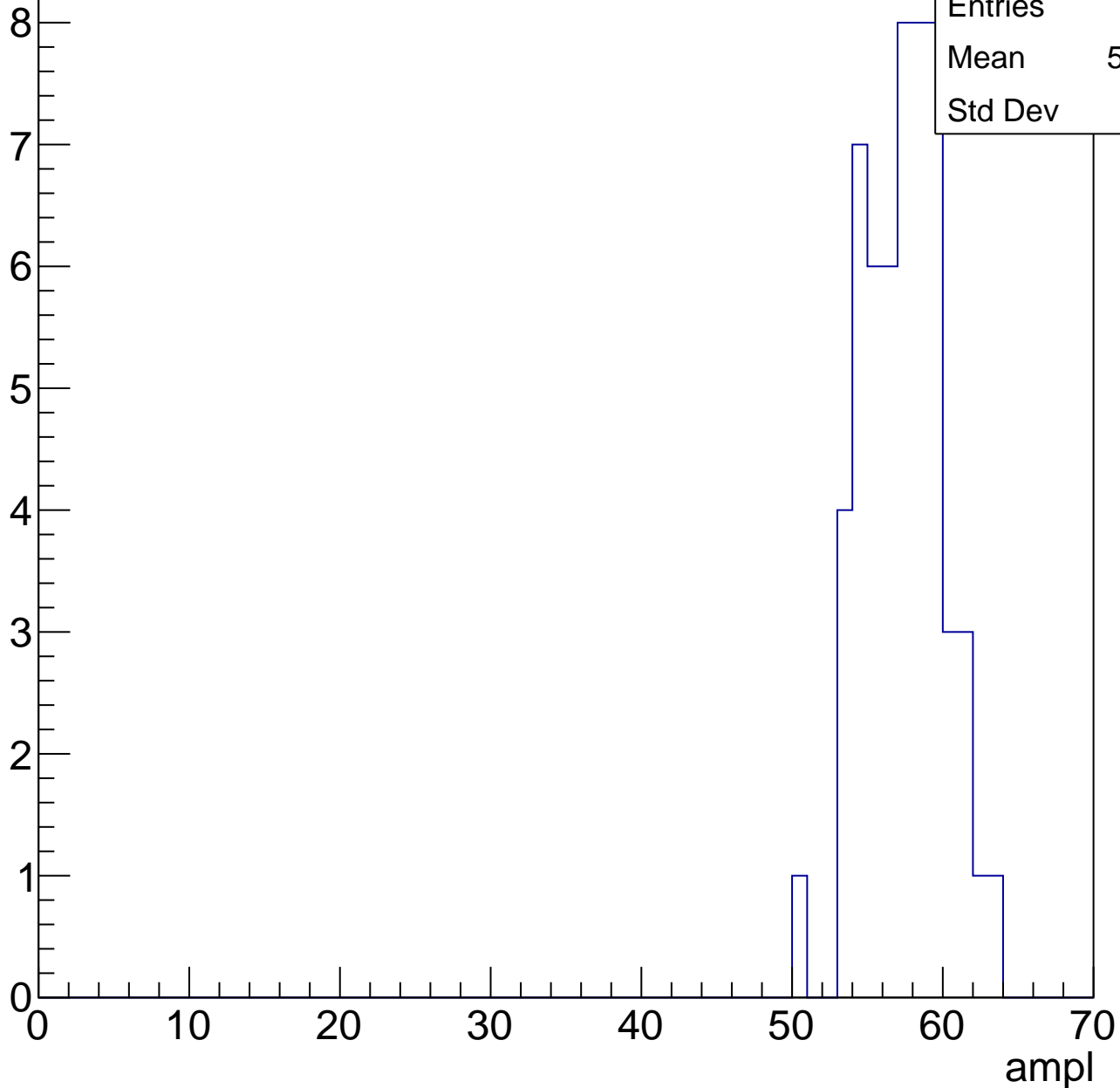
ampl



# B0L001S, U10-ch18, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



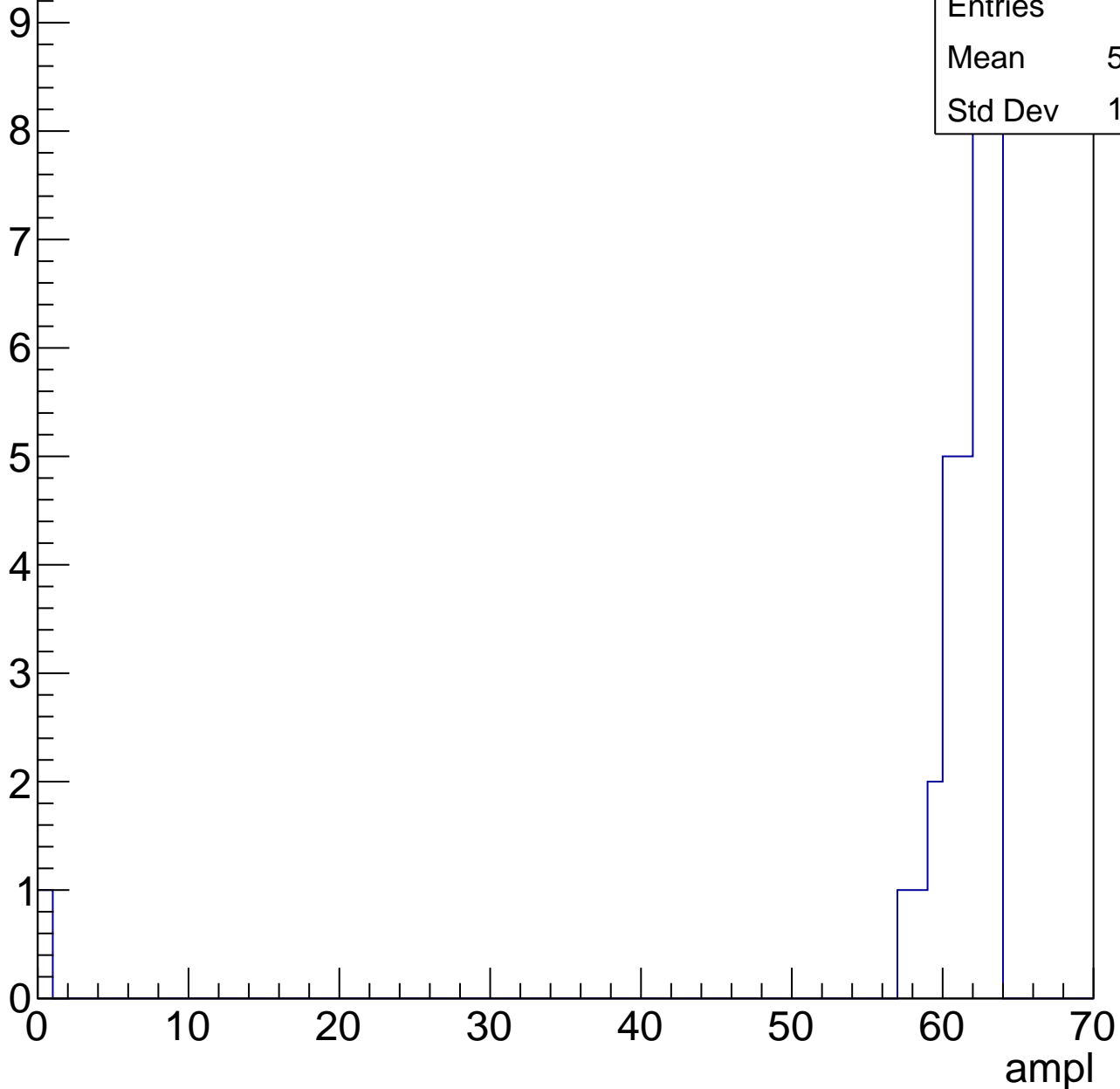
Entries	56
Mean	56.89
Std Dev	2.61

# B0L001S, U10-ch18, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	33
Mean	59.48
Std Dev	10.63



# B0L001S, U10-ch18, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	61
Std Dev	0

ampl



# B0L001S, U10-ch18, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U10-ch19, adc0

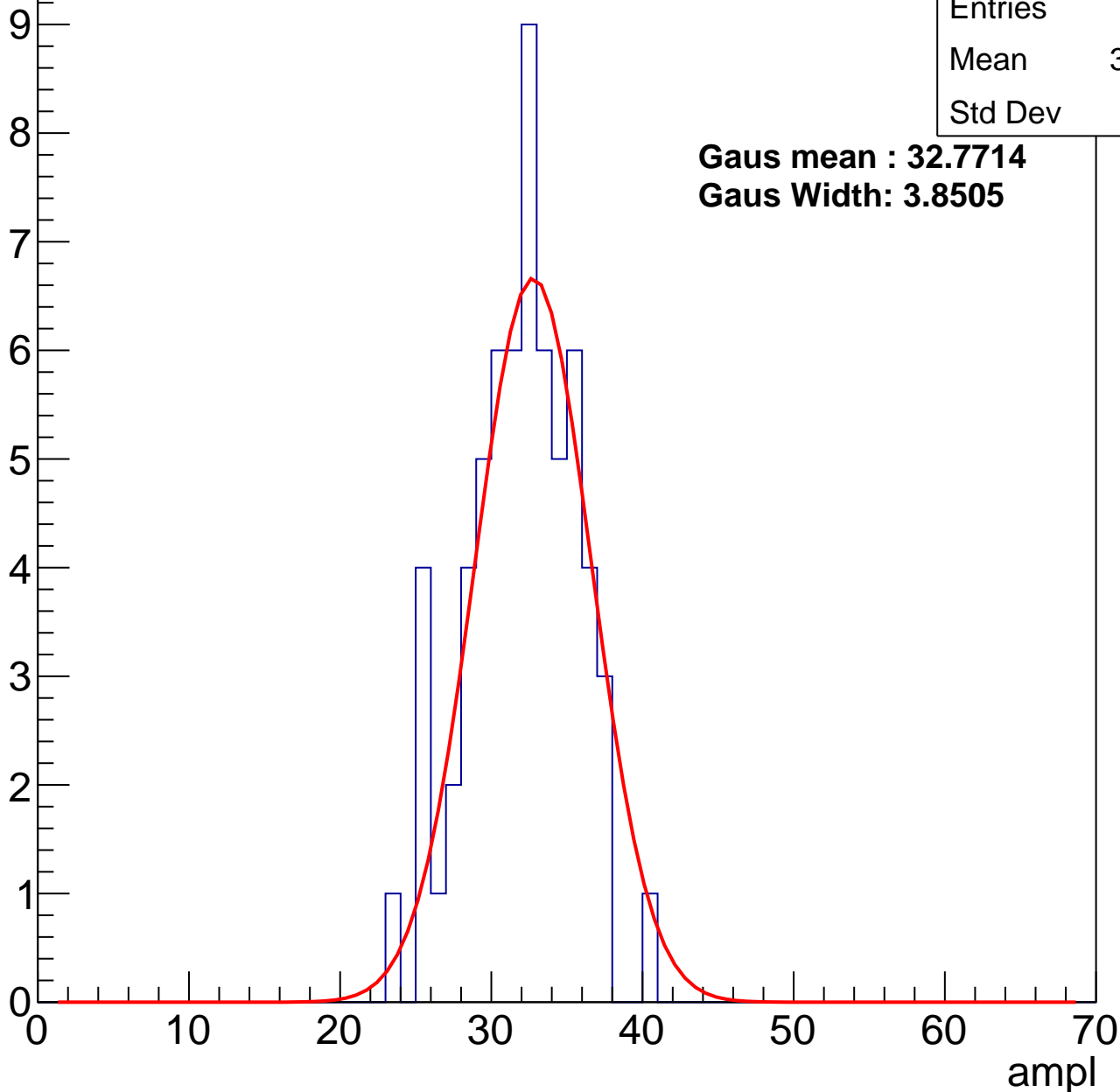
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	31.54
Std Dev	3.5

**Gaus mean : 32.7714**

**Gaus Width: 3.8505**



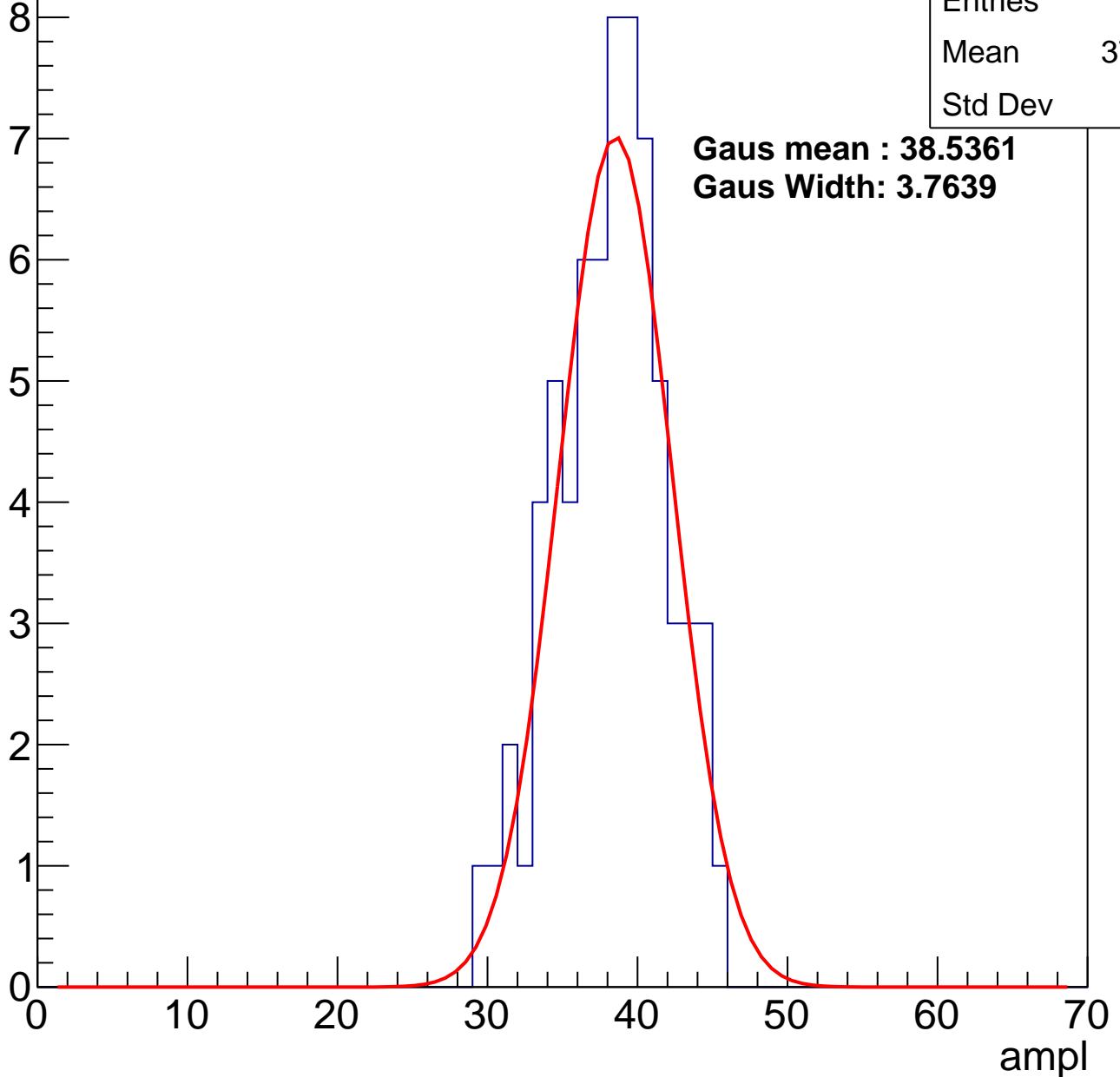
# B0L001S, U10-ch19, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	37.74
Std Dev	3.6

**Gaus mean : 38.5361**  
**Gaus Width: 3.7639**



# B0L001S, U10-ch19, adc2

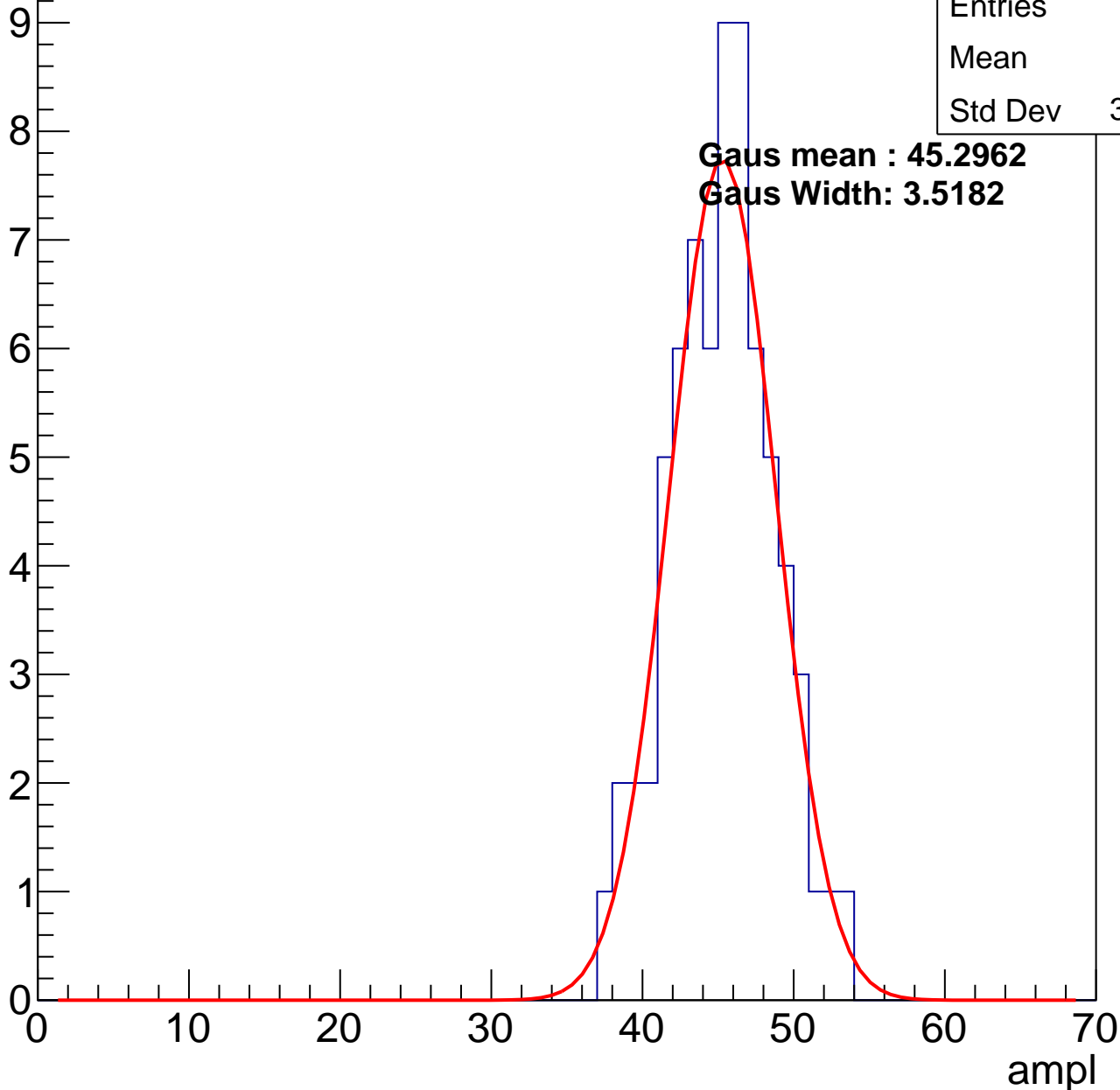
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	44.8
Std Dev	3.413

**Gaus mean : 45.2962**

**Gaus Width: 3.5182**

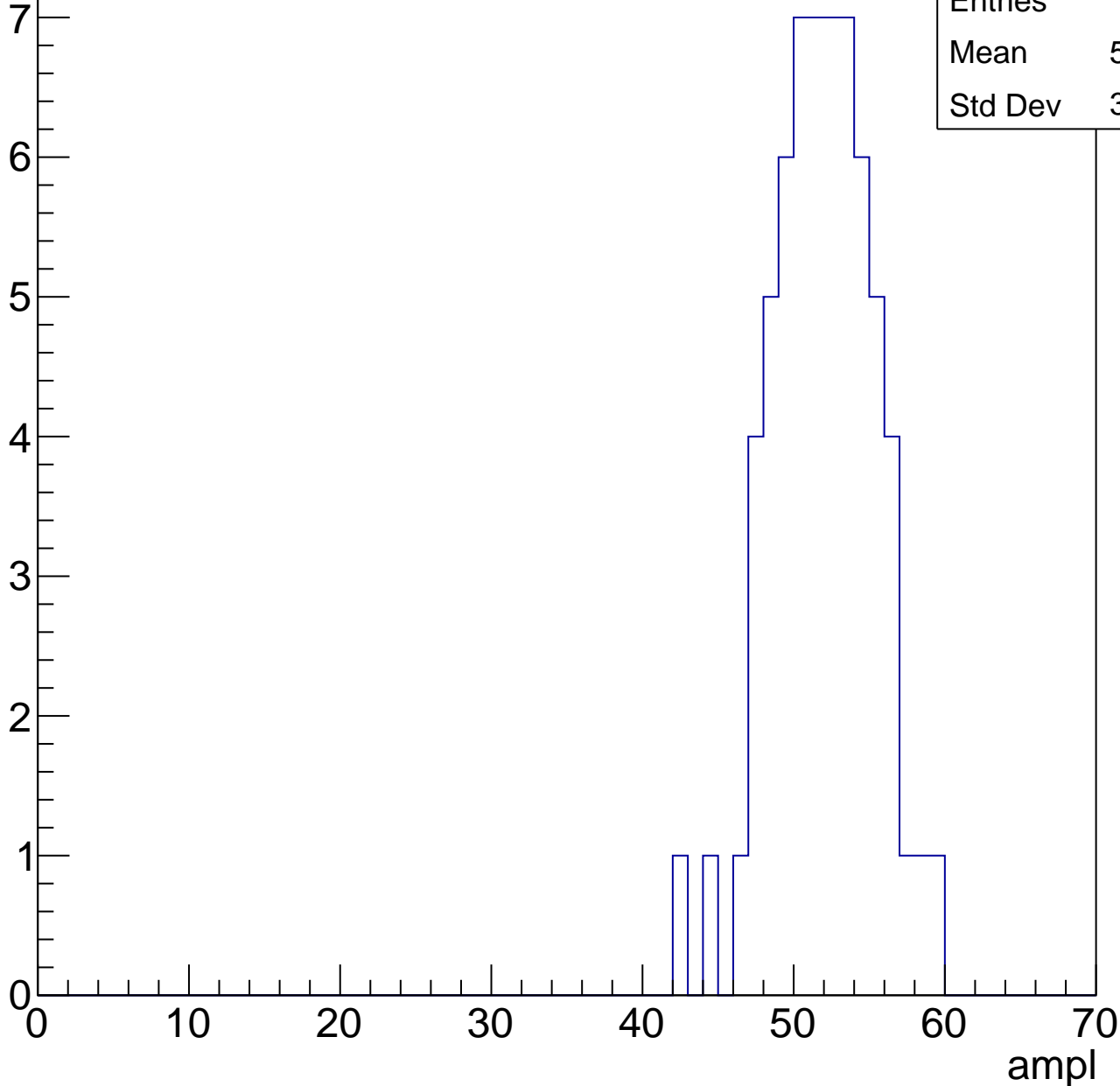


# B0L001S, U10-ch19, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	51.45
Std Dev	3.307



# B0L001S, U10-ch19, adc4

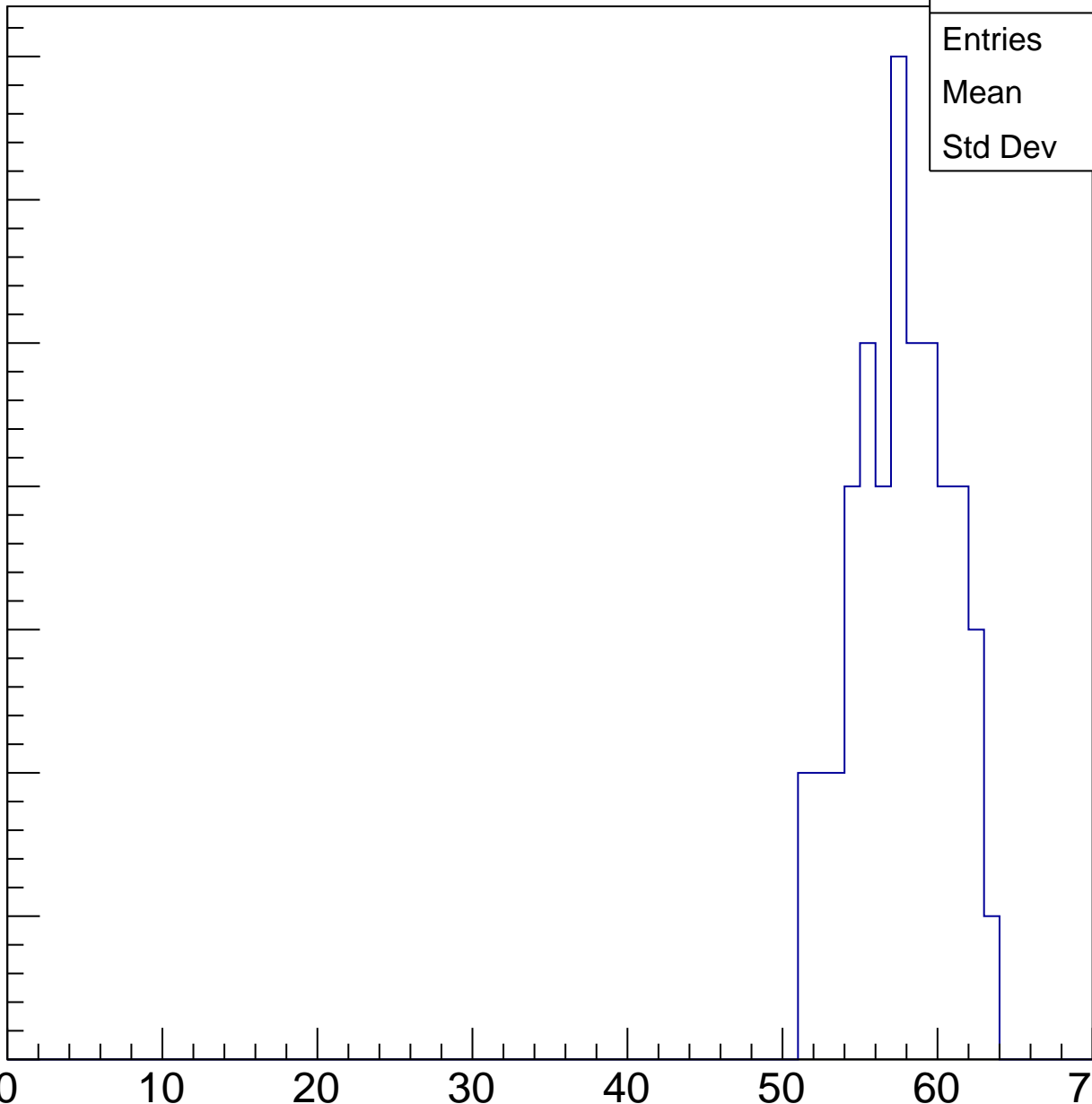
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

7  
6  
5  
4  
3  
2  
1  
0

Entries	48
Mean	57.17
Std Dev	3.057

ampl

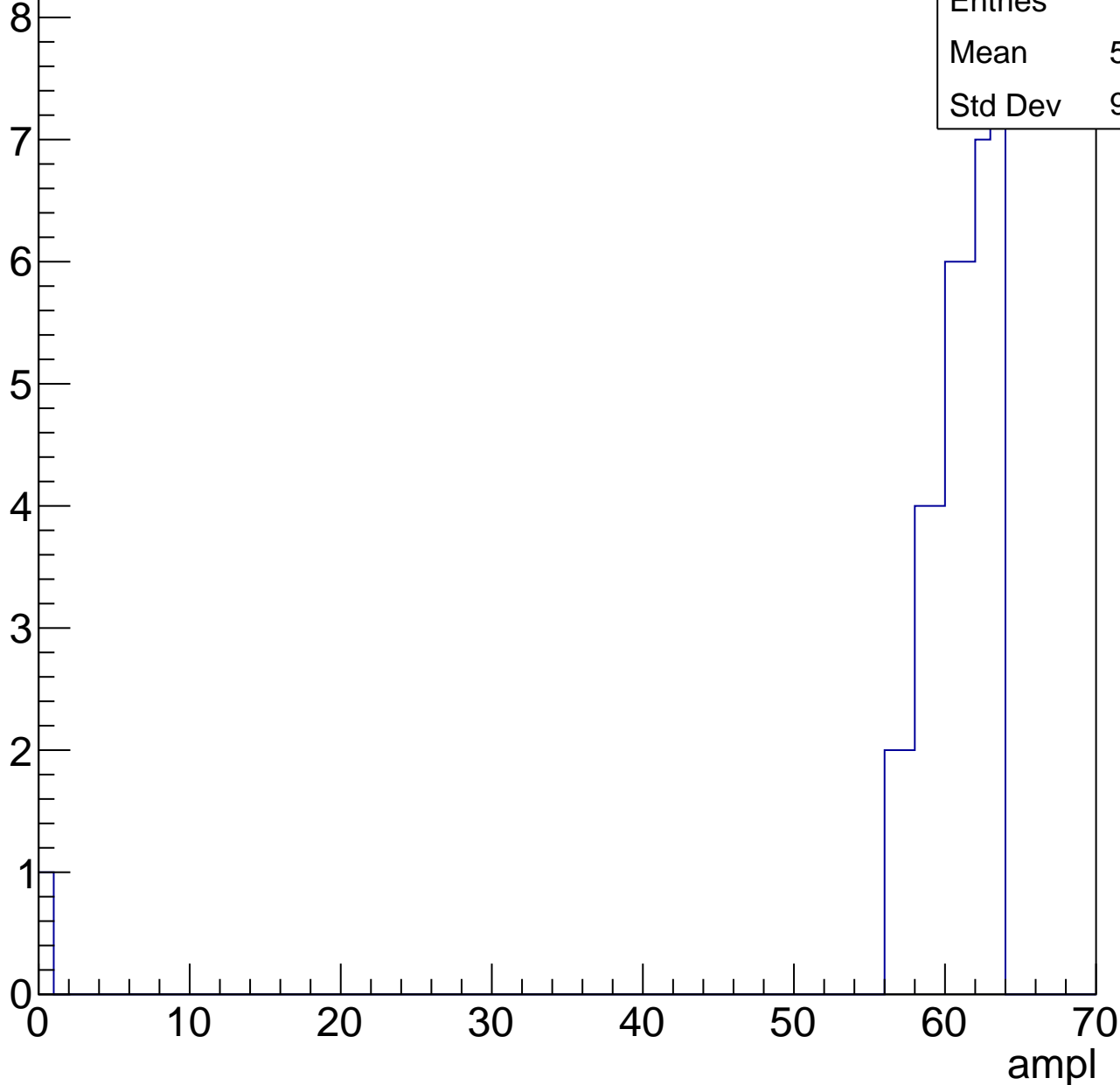


# B0L001S, U10-ch19, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	40
Mean	58.95
Std Dev	9.659



# B0L001S, U10-ch19, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch19, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U10-ch20, adc0

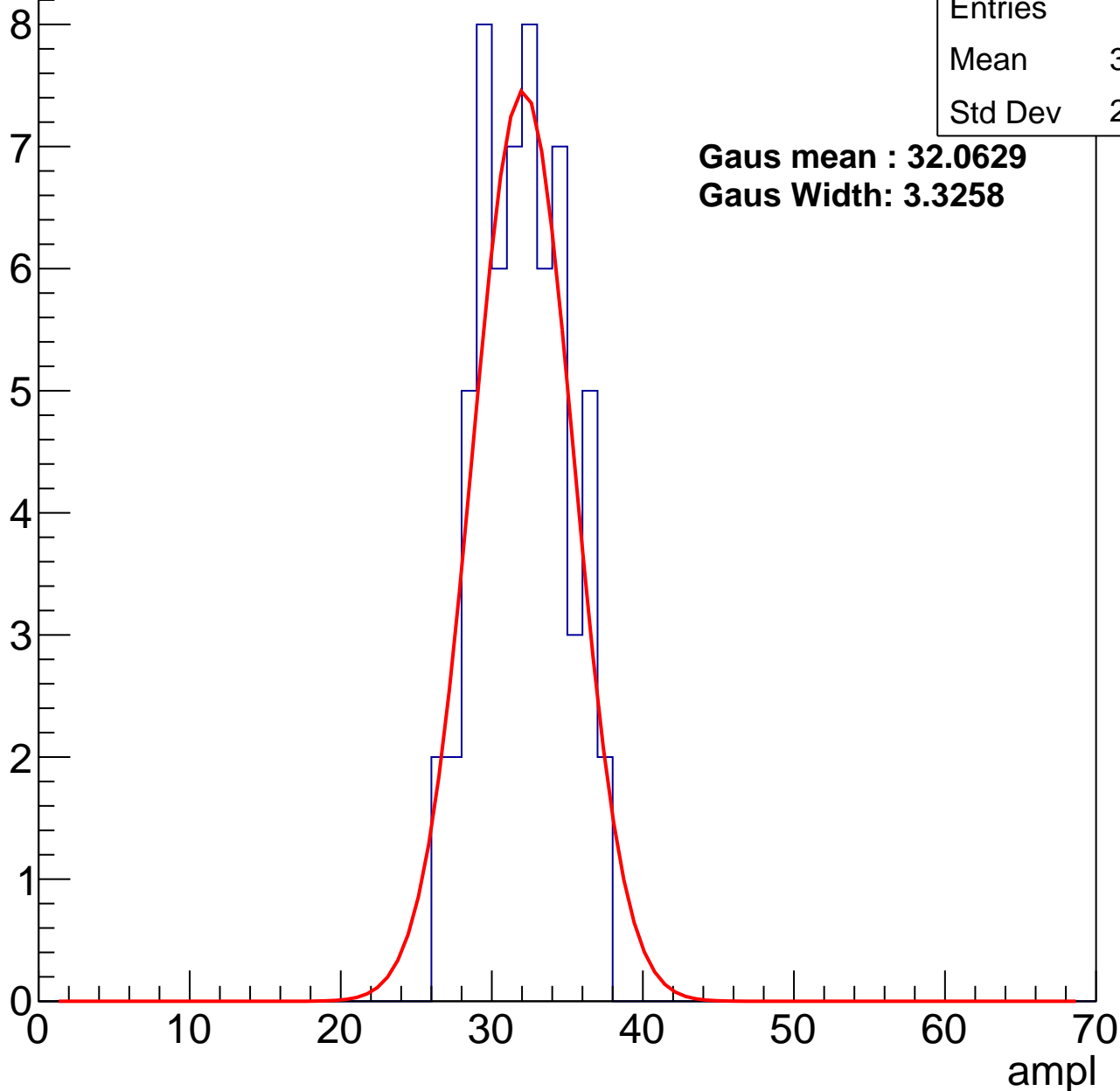
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	31.57
Std Dev	2.819

**Gaus mean : 32.0629**

**Gaus Width: 3.3258**



# B0L001S, U10-ch20, adc1

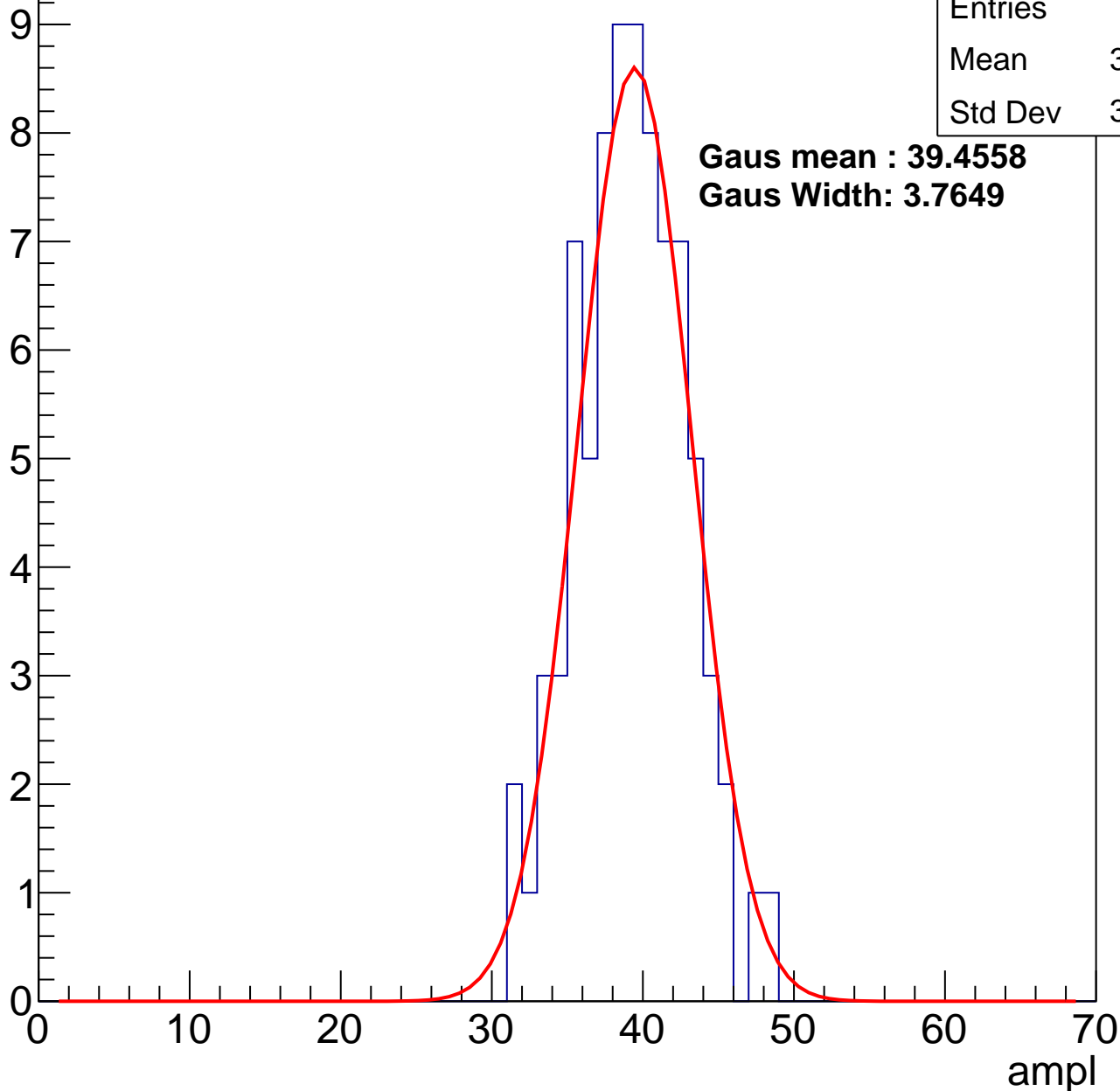
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	81
Mean	38.79
Std Dev	3.558

**Gaus mean : 39.4558**

**Gaus Width: 3.7649**



# B0L001S, U10-ch20, adc2

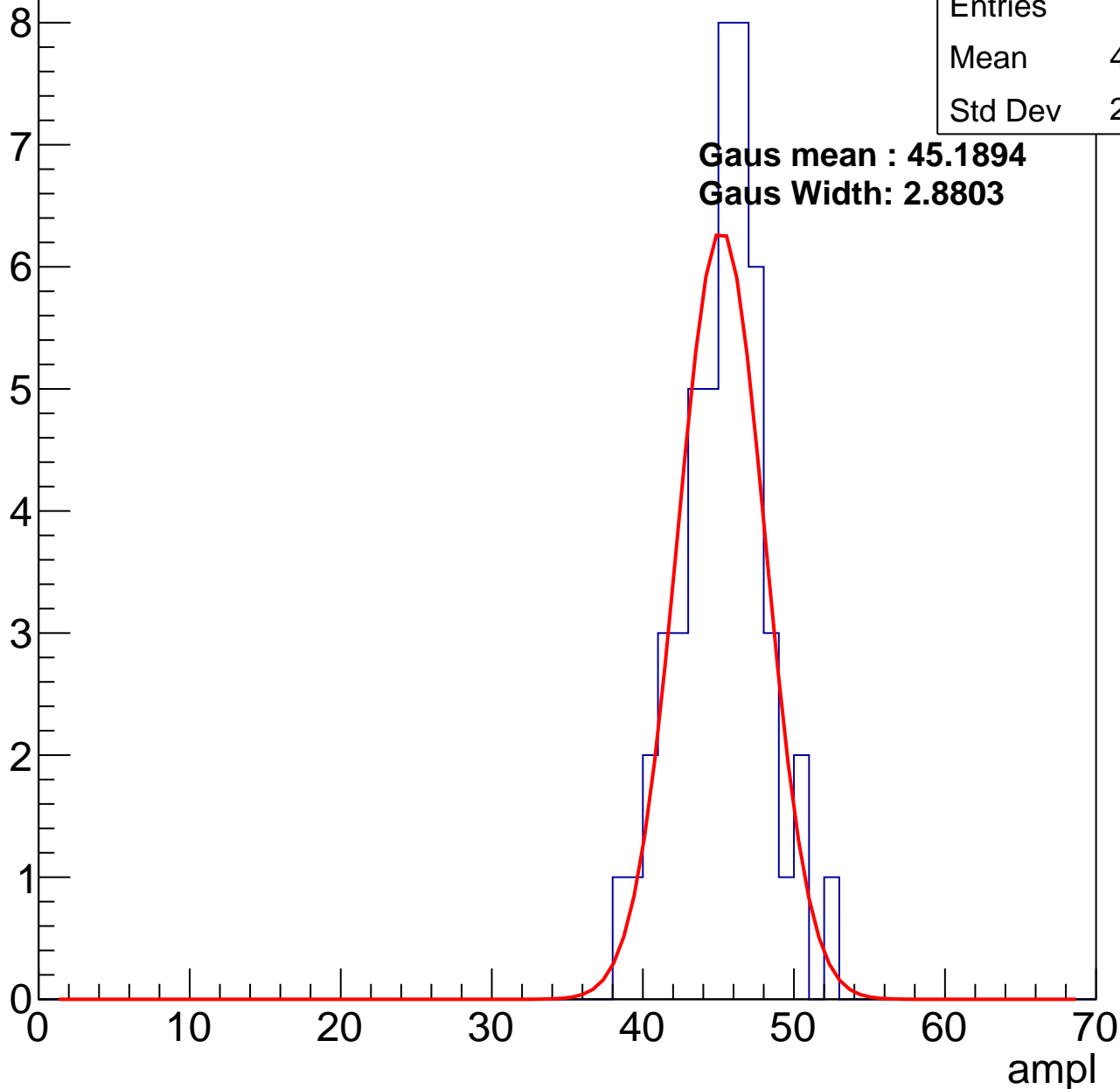
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	49
Mean	44.82
Std Dev	2.883

**Gaus mean : 45.1894**

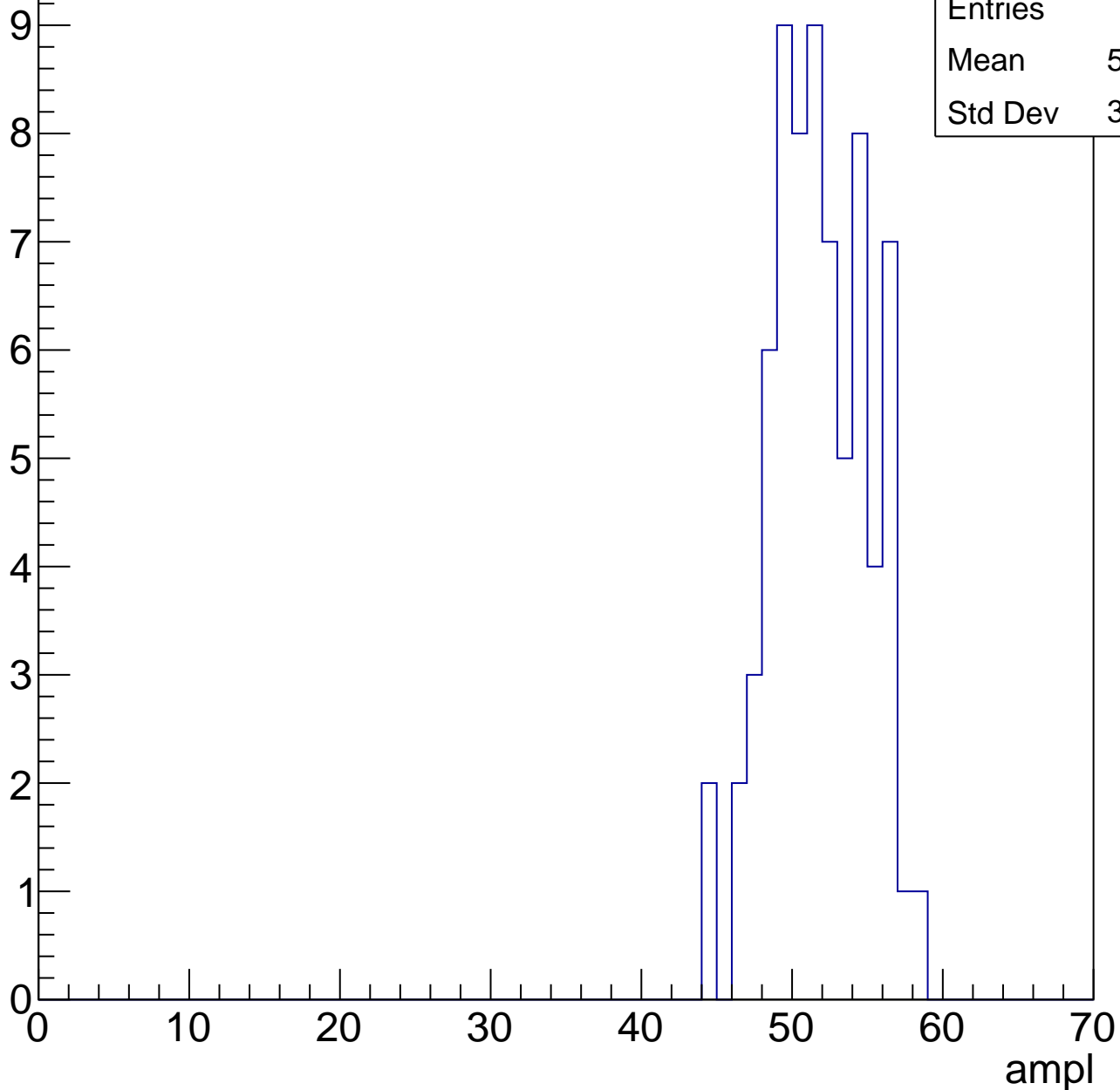
**Gaus Width: 2.8803**



# B0L001S, U10-ch20, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



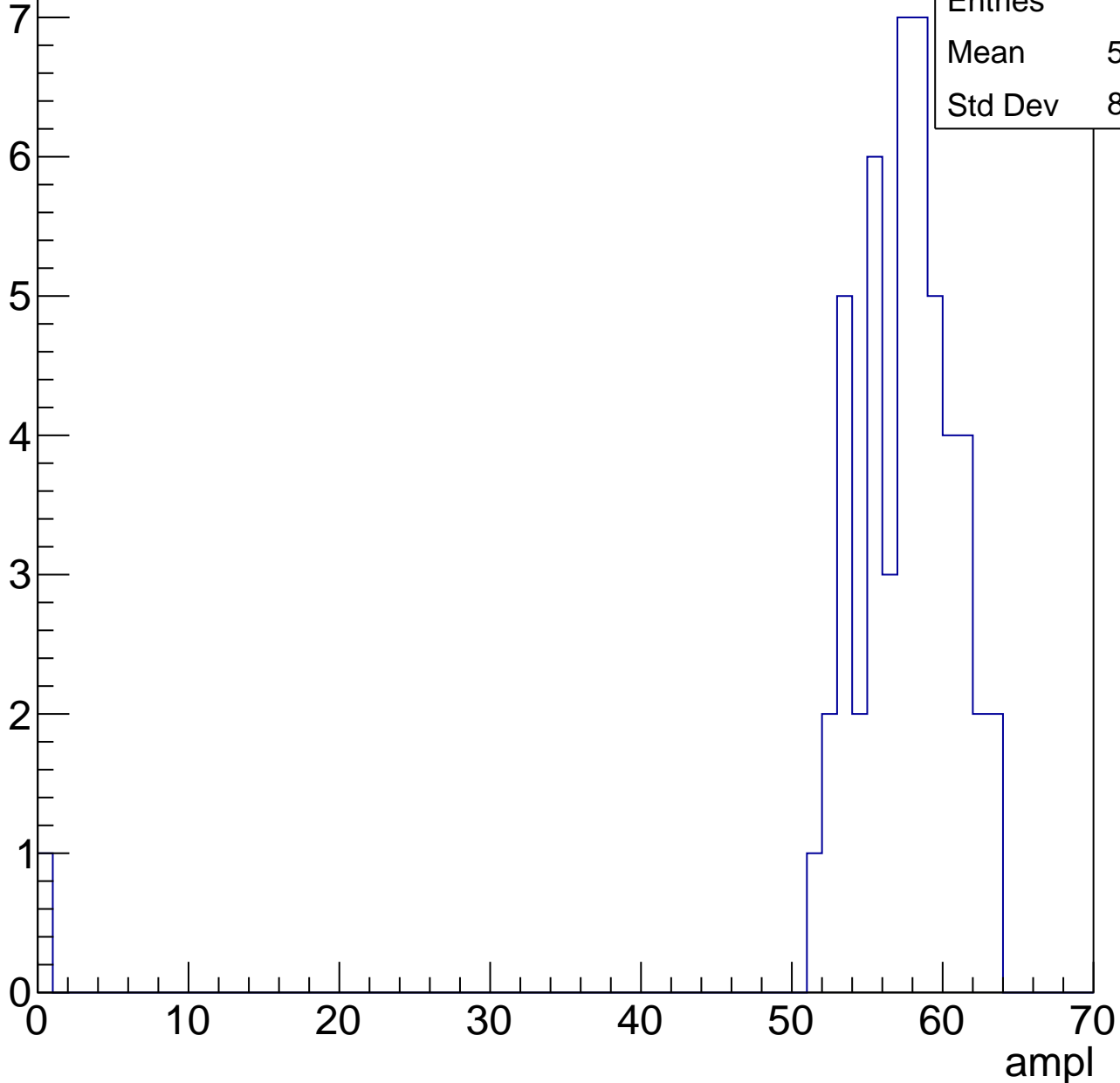
Entries	72
Mean	51.35
Std Dev	3.137

# B0L001S, U10-ch20, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	51
Mean	56.08
Std Dev	8.478

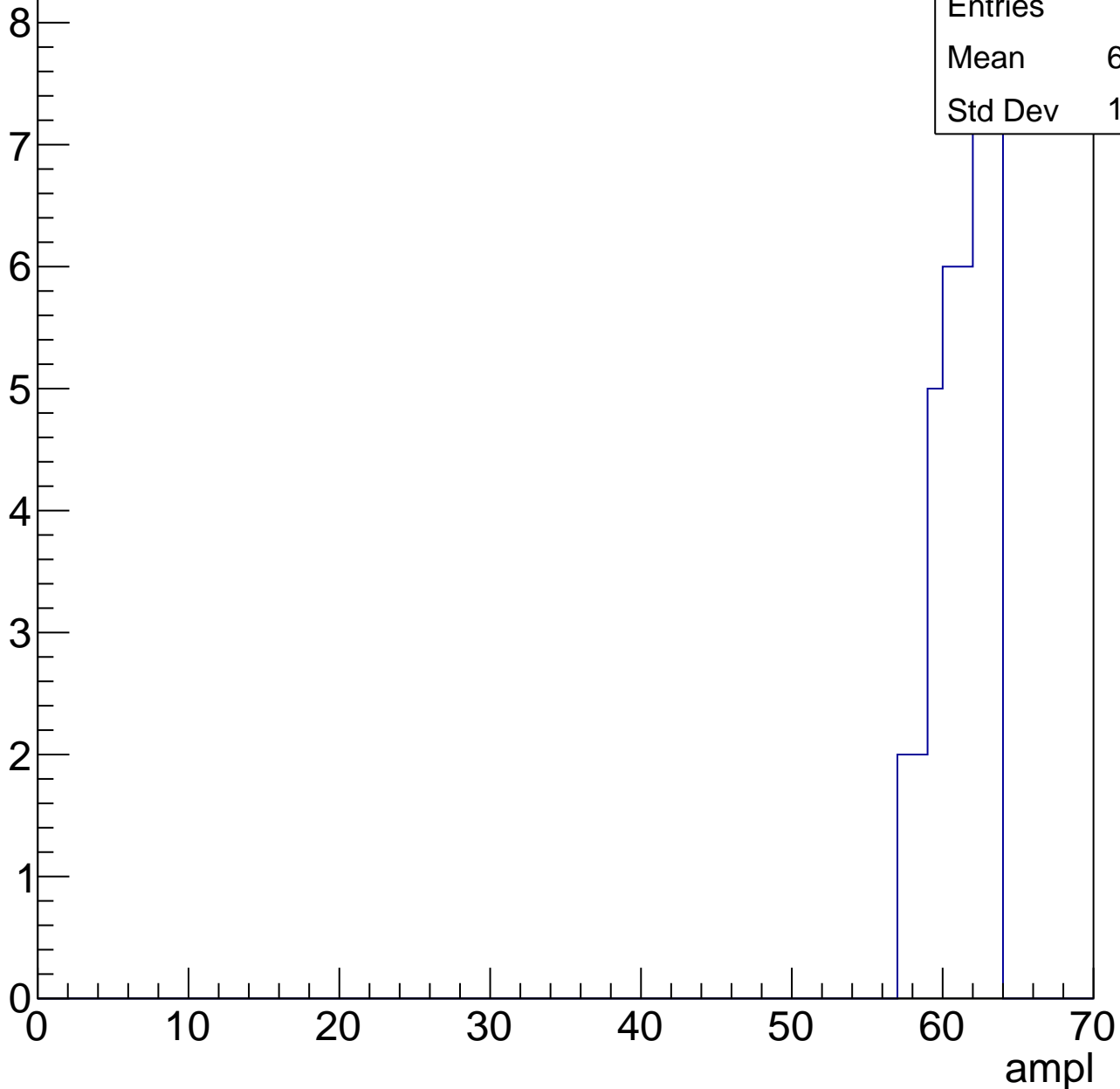


# B0L001S, U10-ch20, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	37
Mean	60.84
Std Dev	1.763



# B0L001S, U10-ch20, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

0

Mean

0

Std Dev

0



# B0L001S, U10-ch20, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	12.5
Std Dev	12.5

# B0L001S, U10-ch21, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	68
Mean	30.57
Std Dev	3.117

**Gaus mean : 31.0697**

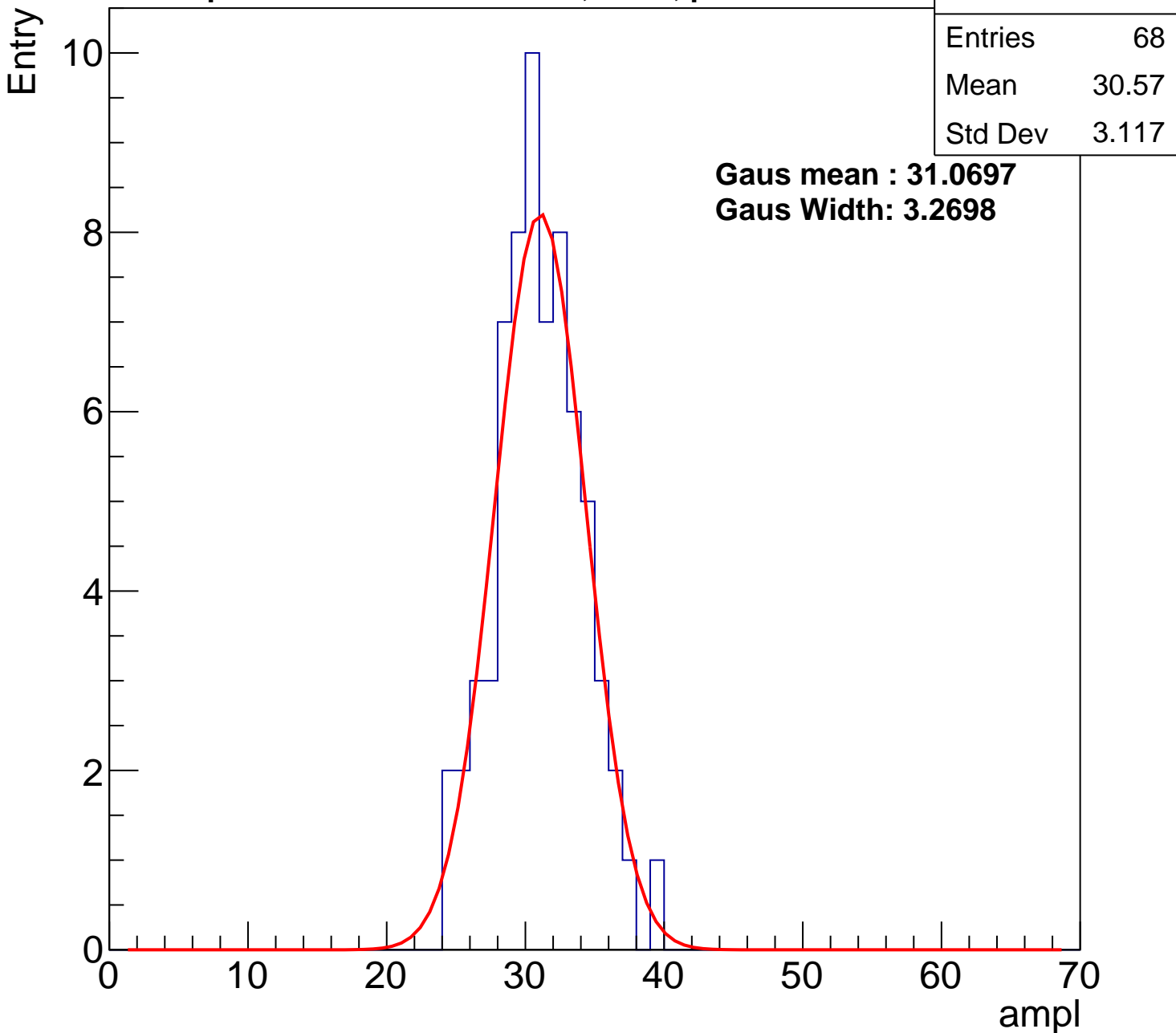
**Gaus Width: 3.2698**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



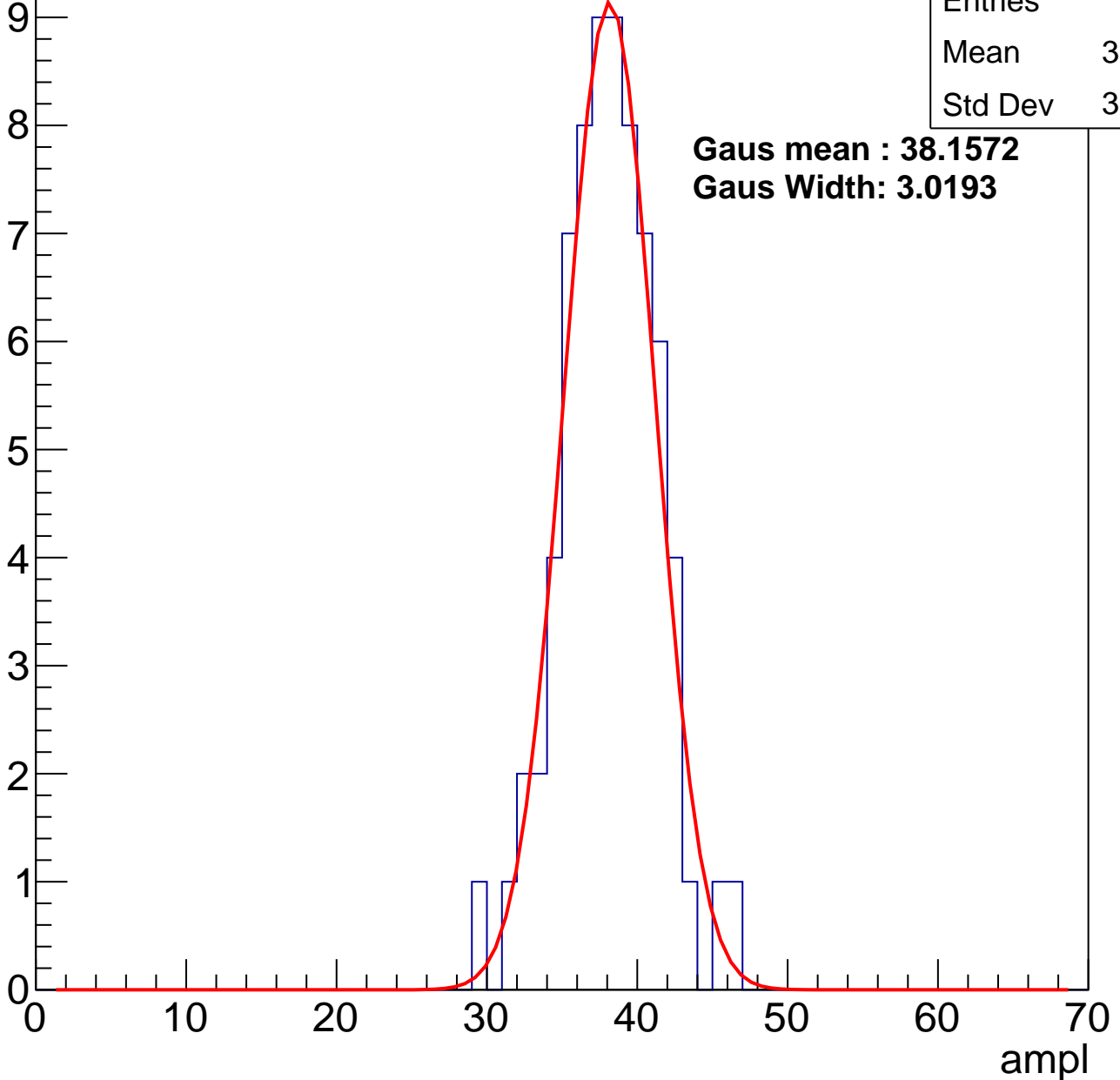
# B0L001S, U10-ch21, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	37.66
Std Dev	3.149

**Gaus mean : 38.1572**  
**Gaus Width: 3.0193**



# B0L001S, U10-ch21, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	69
Mean	44.87
Std Dev	3.426

**Gaus mean : 45.3584**

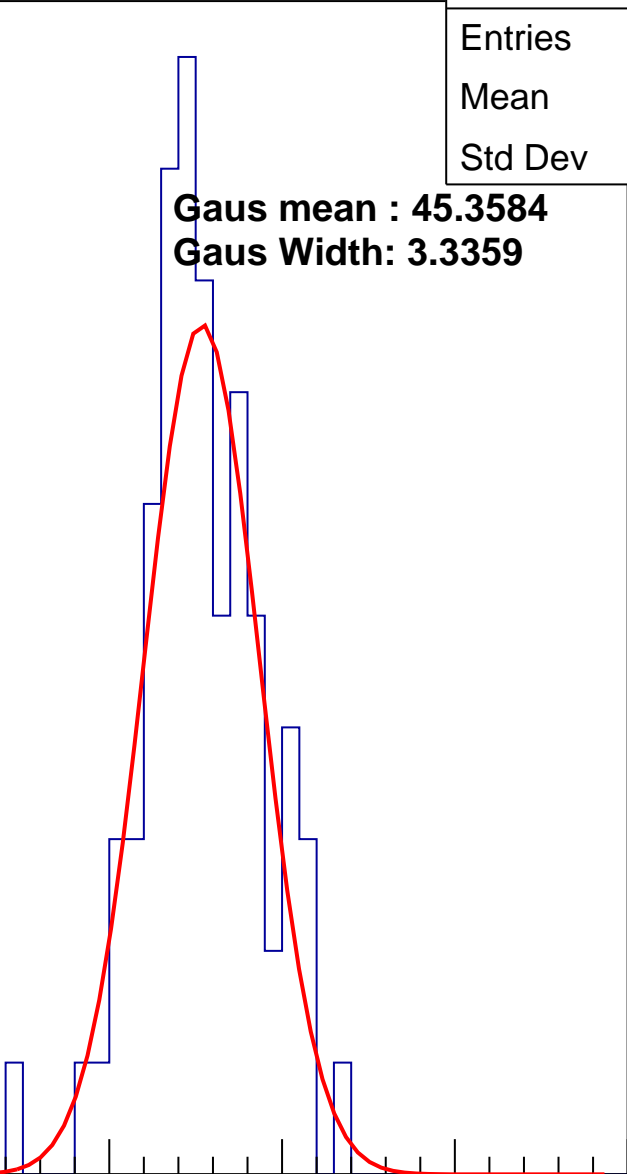
**Gaus Width: 3.3359**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

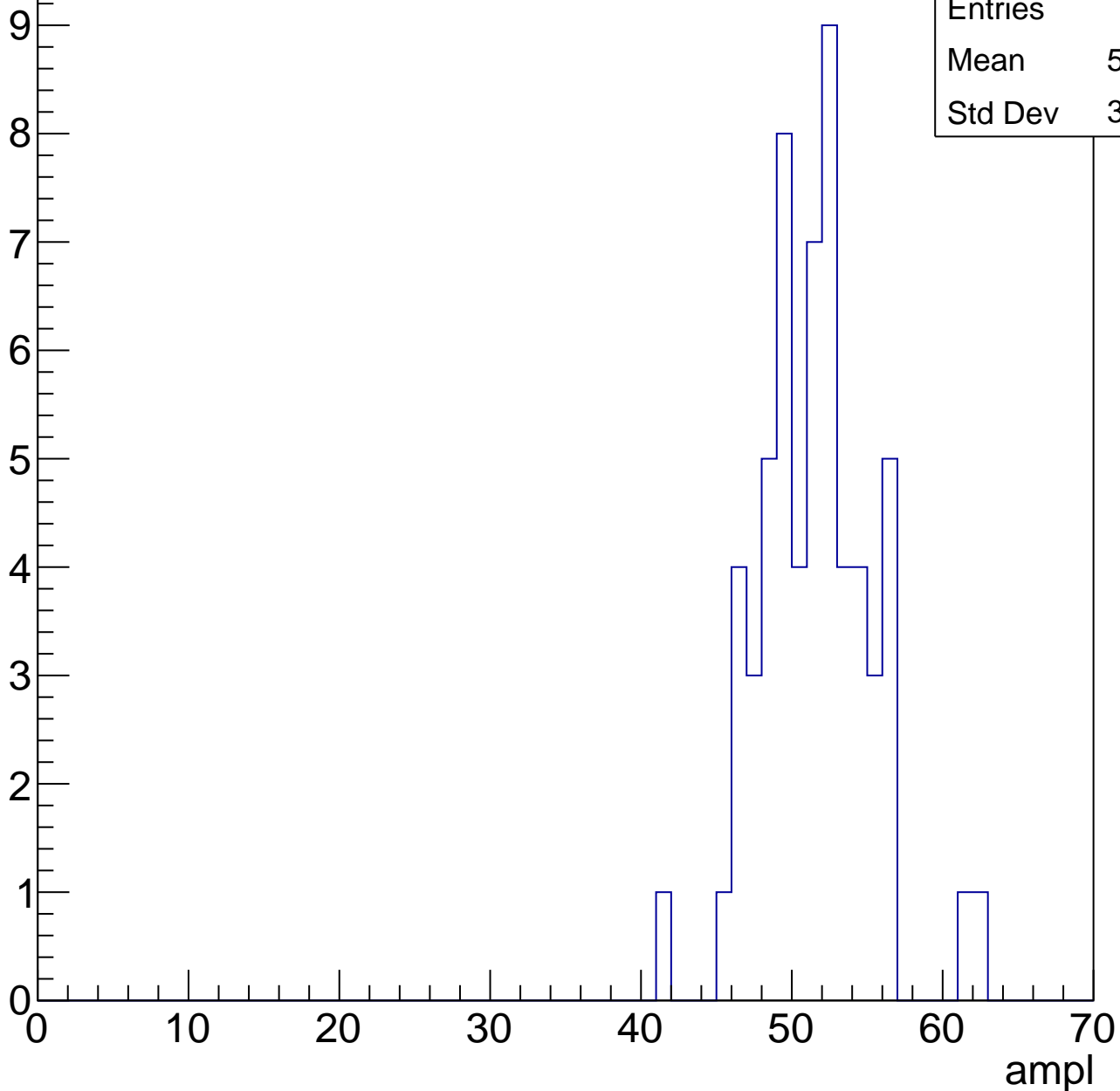


# B0L001S, U10-ch21, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	51.07
Std Dev	3.696



# B0L001S, U10-ch21, adc4

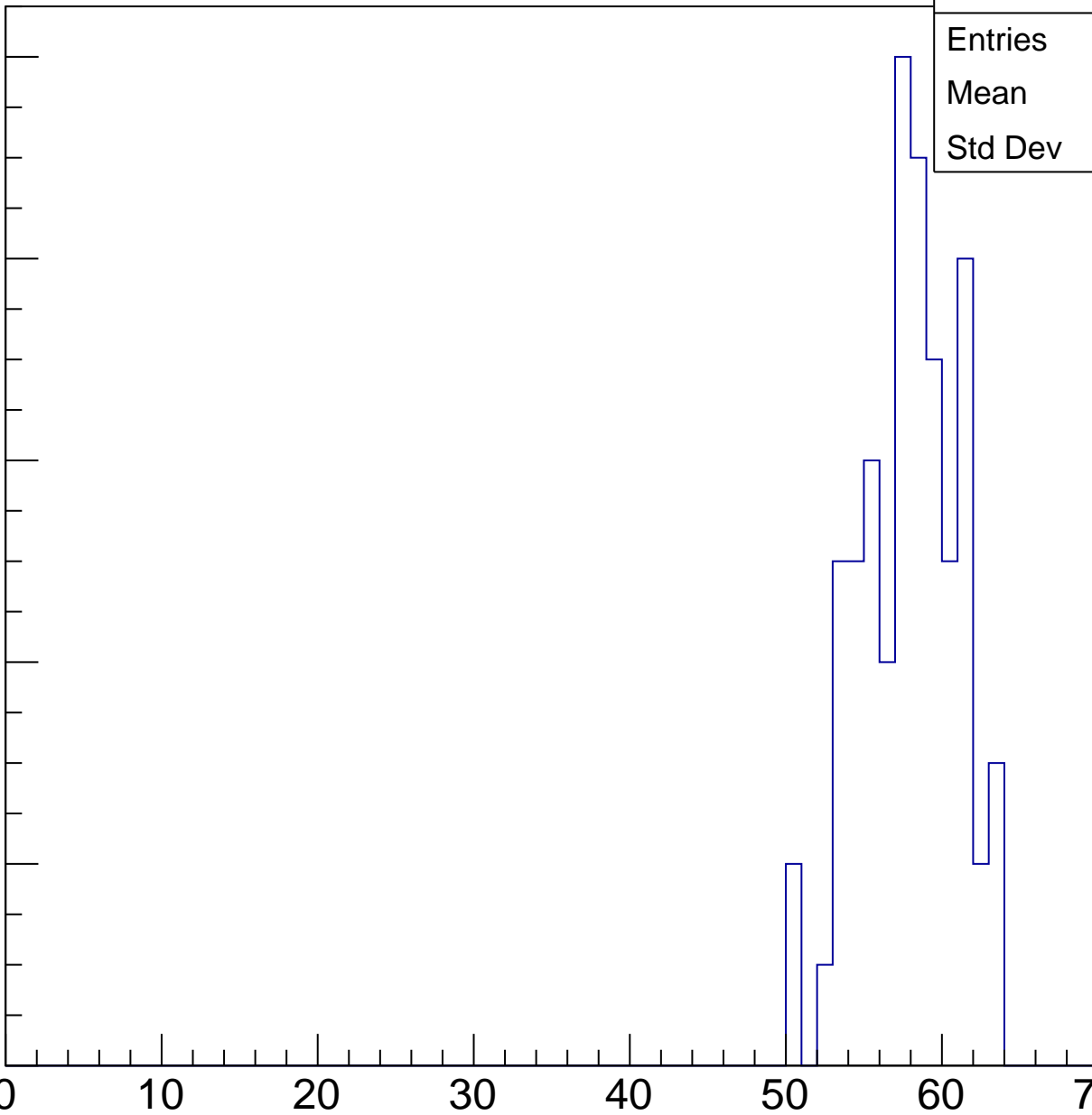
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	67
Mean	57.42
Std Dev	3.072

Entry

10  
8  
6  
4  
2  
0

ampl

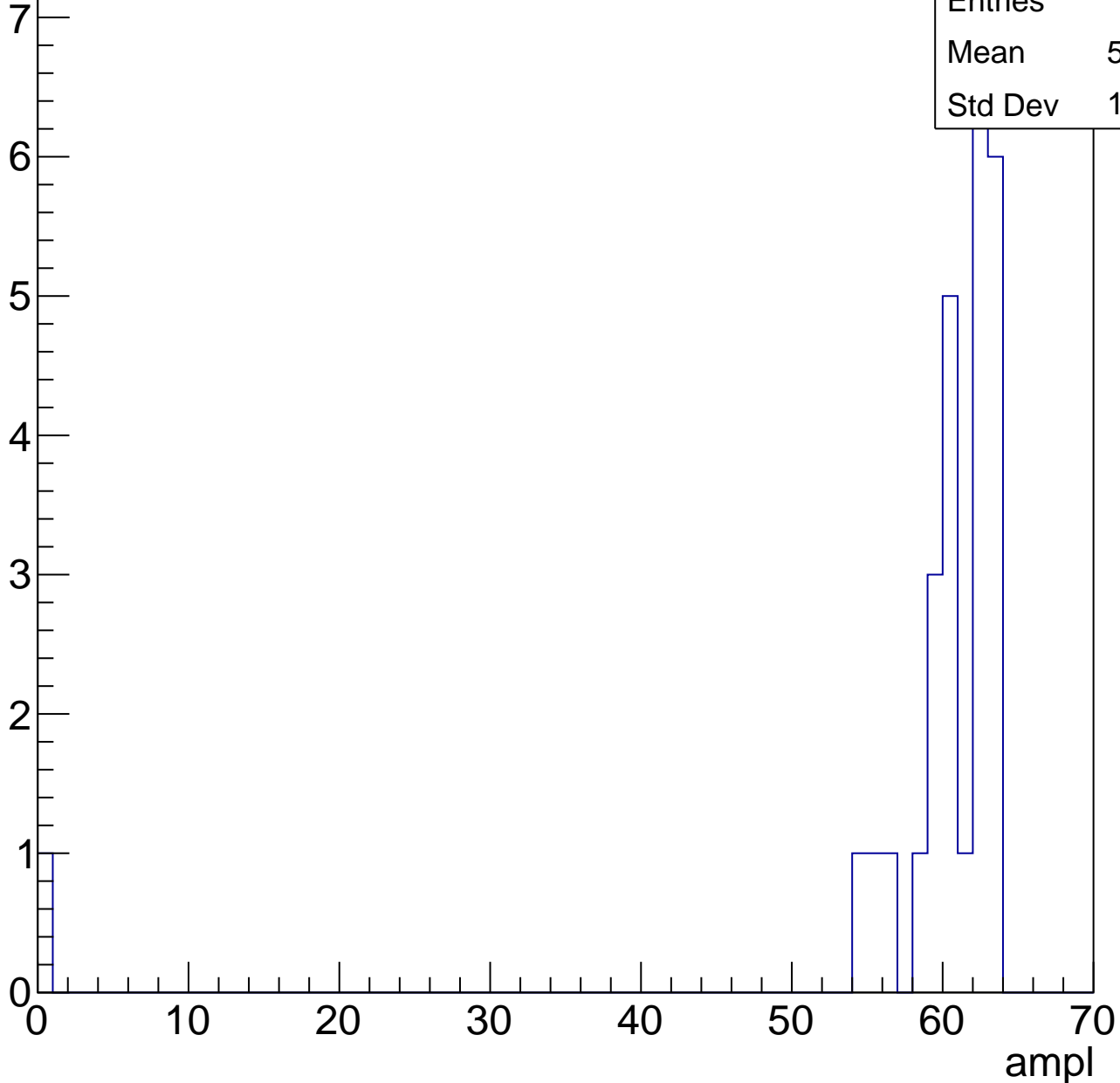


# B0L001S, U10-ch21, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	27
Mean	58.26
Std Dev	11.68



# B0L001S, U10-ch21, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch21, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U10-ch22, adc0

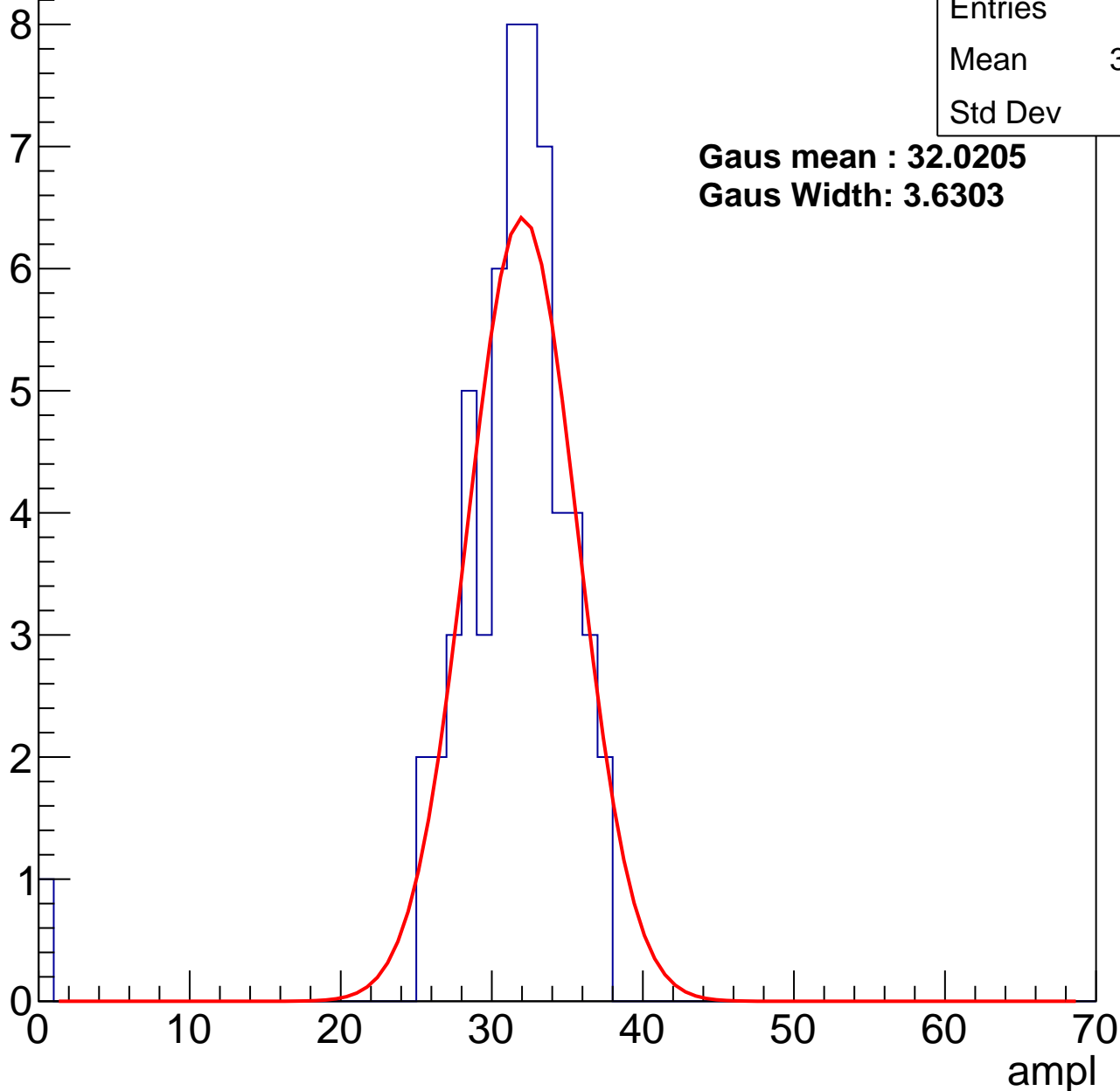
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	30.74
Std Dev	5.04

**Gaus mean : 32.0205**

**Gaus Width: 3.6303**



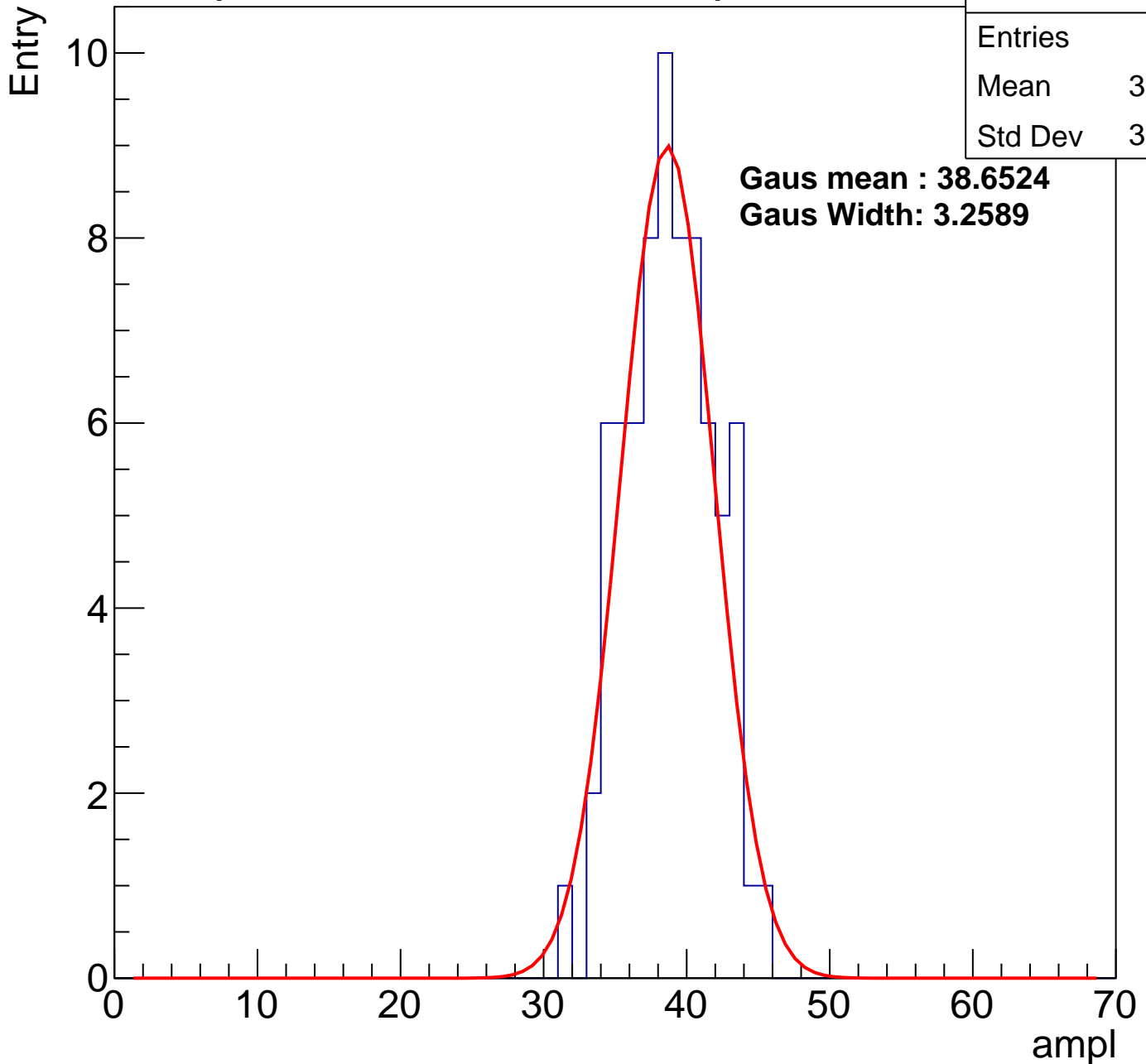
# B0L001S, U10-ch22, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	74
Mean	38.35
Std Dev	3.033

**Gaus mean : 38.6524**

**Gaus Width: 3.2589**



# B0L001S, U10-ch22, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	73
Mean	45.36
Std Dev	3.16

**Gaus mean : 45.9075**

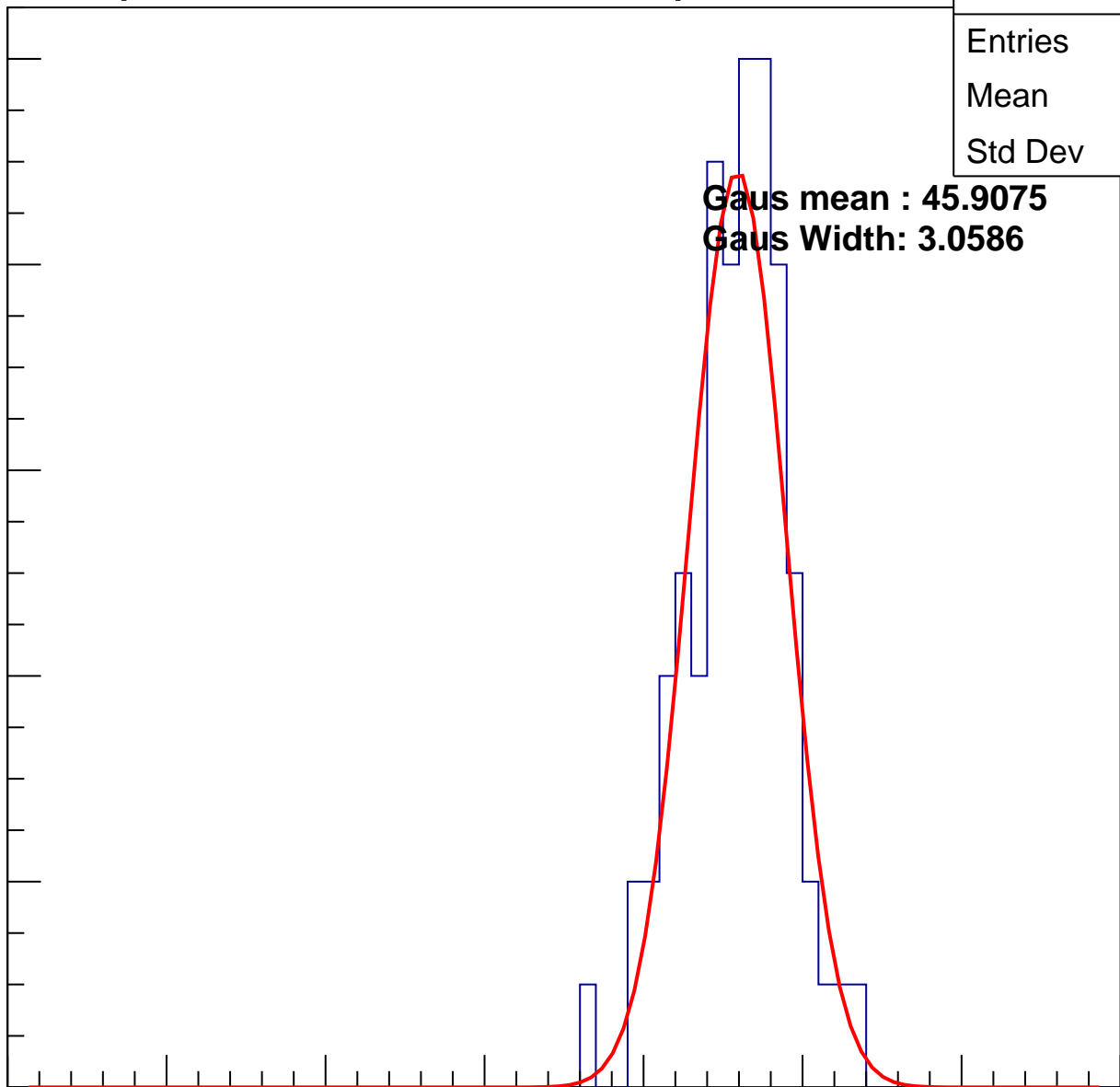
**Gaus Width: 3.0586**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

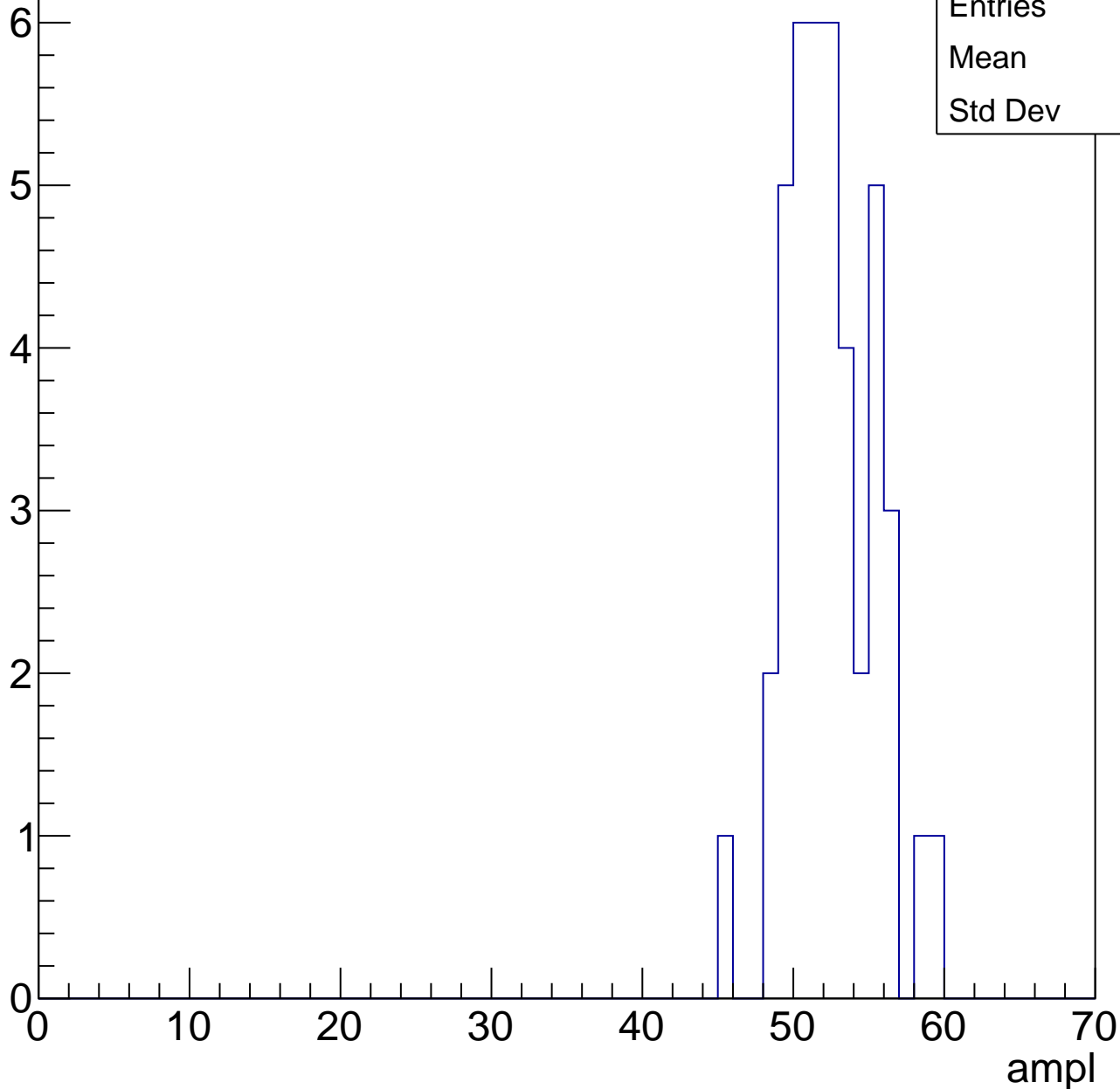


# B0L001S, U10-ch22, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	42
Mean	52
Std Dev	2.87

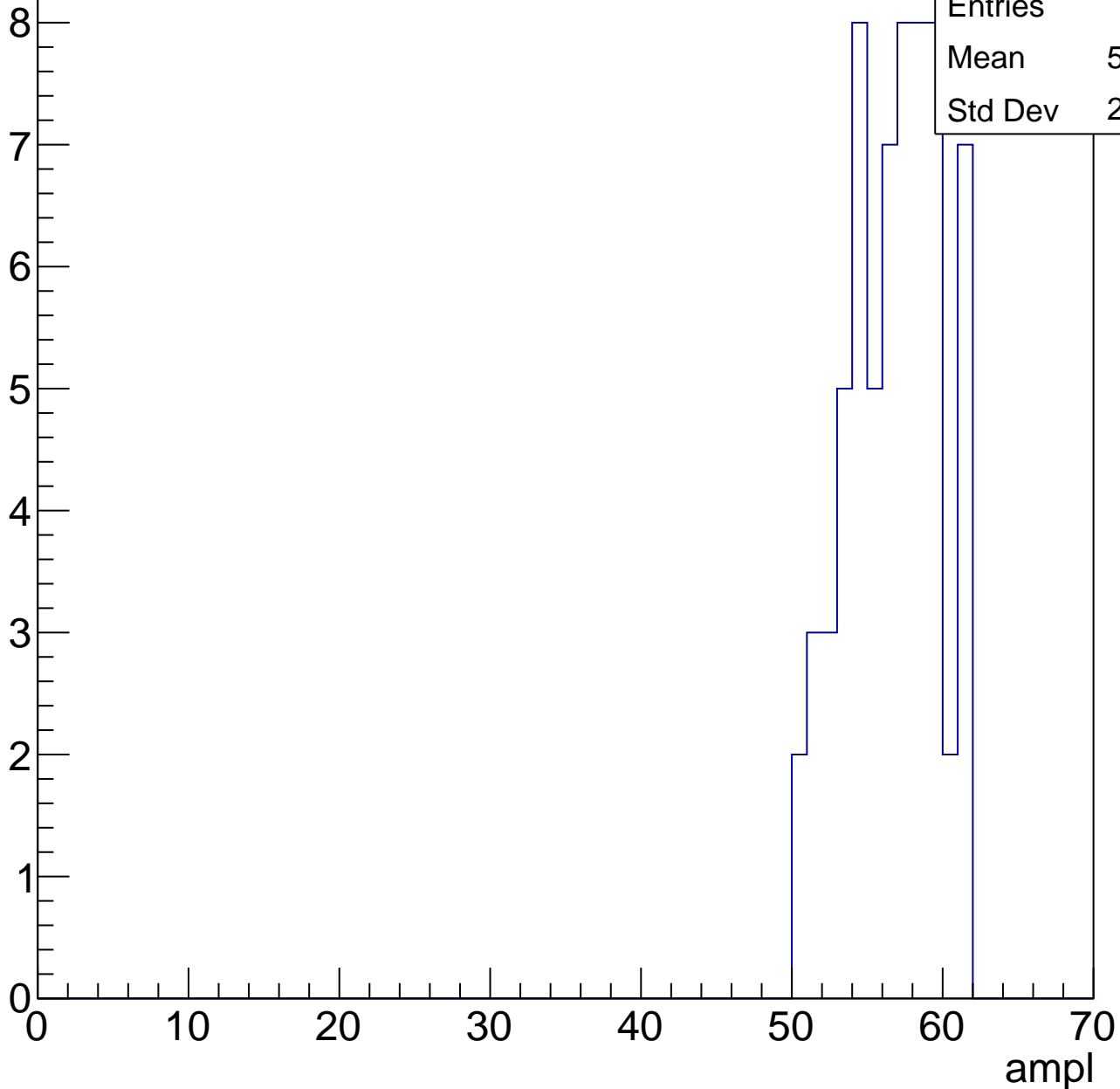


# B0L001S, U10-ch22, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

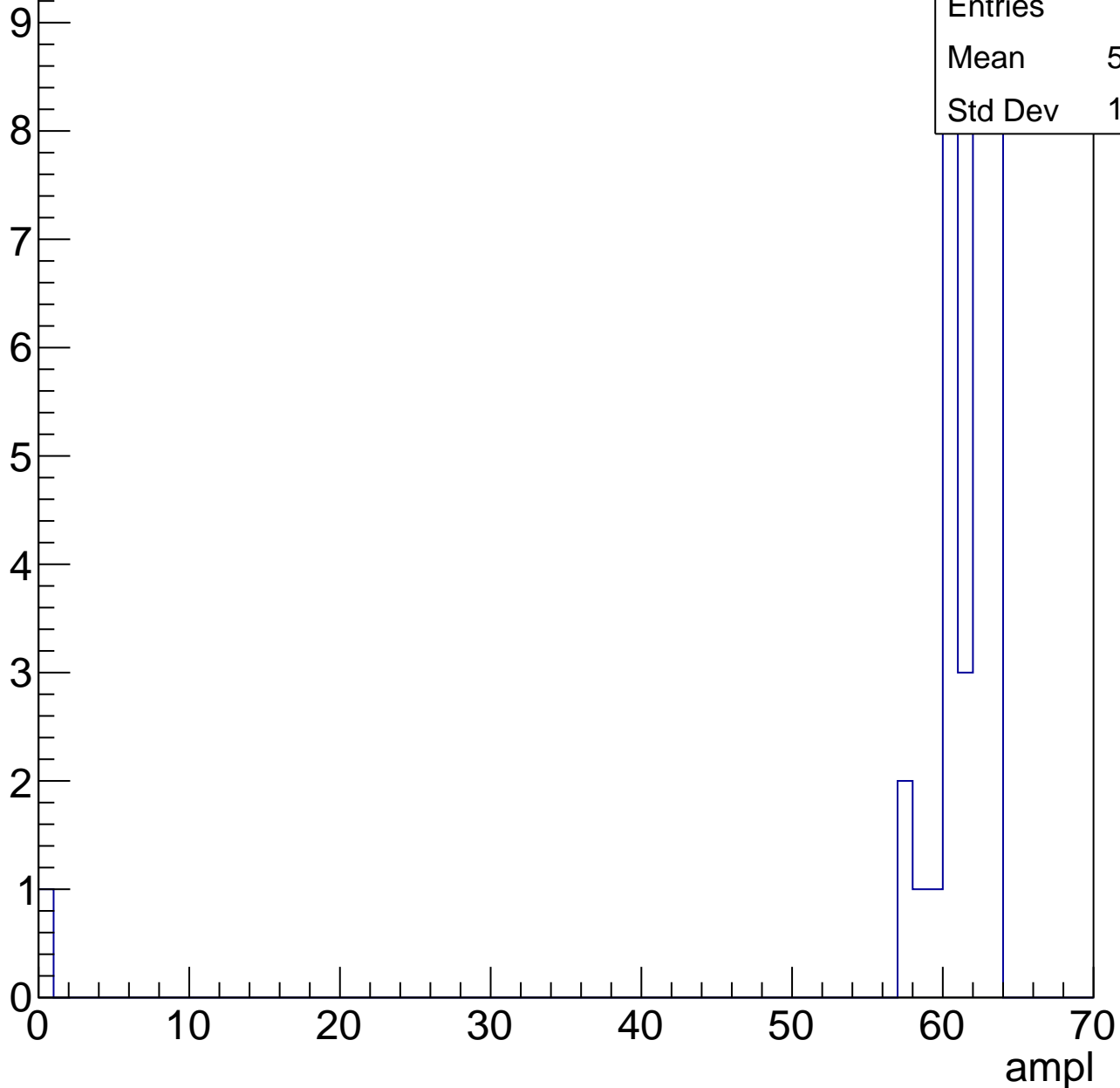
Entries	66
Mean	56.24
Std Dev	2.995



# B0L001S, U10-ch22, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U10-ch22, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch22, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	12.5
Std Dev	12.5

# B0L001S, U10-ch23, adc0

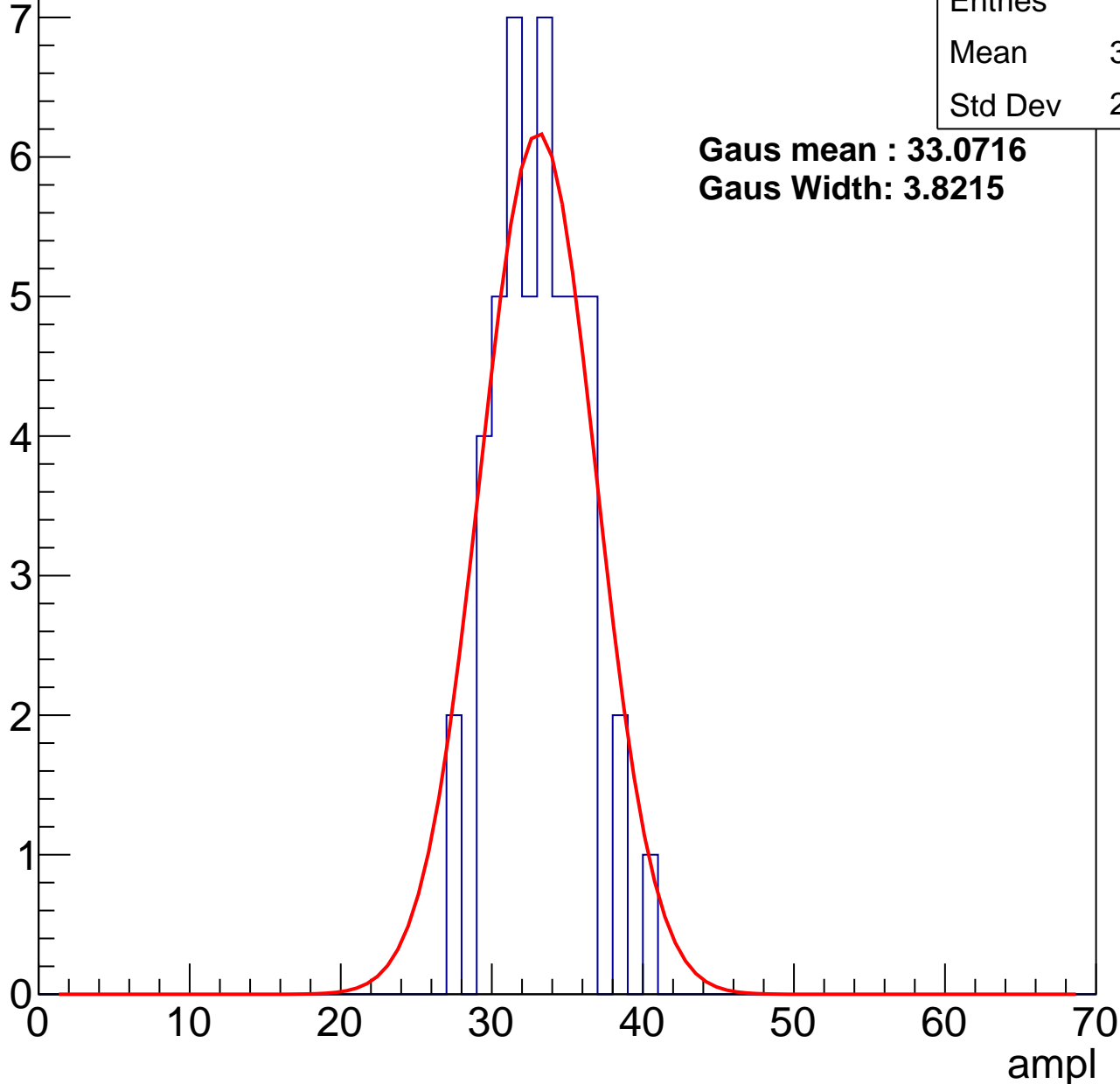
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	48
Mean	32.69
Std Dev	2.807

**Gaus mean : 33.0716**

**Gaus Width: 3.8215**



# B0L001S, U10-ch23, adc1

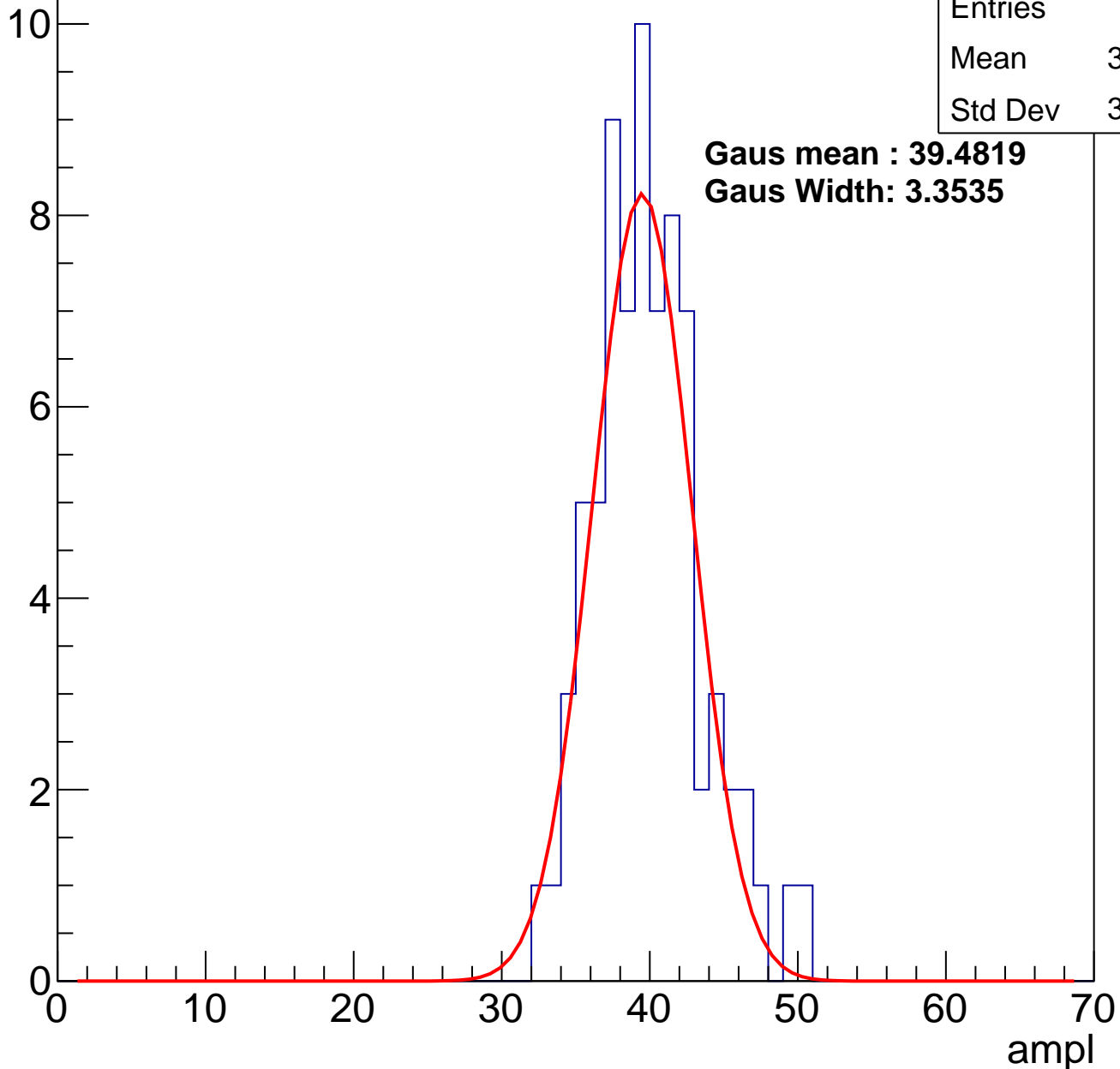
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	75
Mean	39.45
Std Dev	3.608

**Gaus mean : 39.4819**

**Gaus Width: 3.3535**

Entry



# B0L001S, U10-ch23, adc2

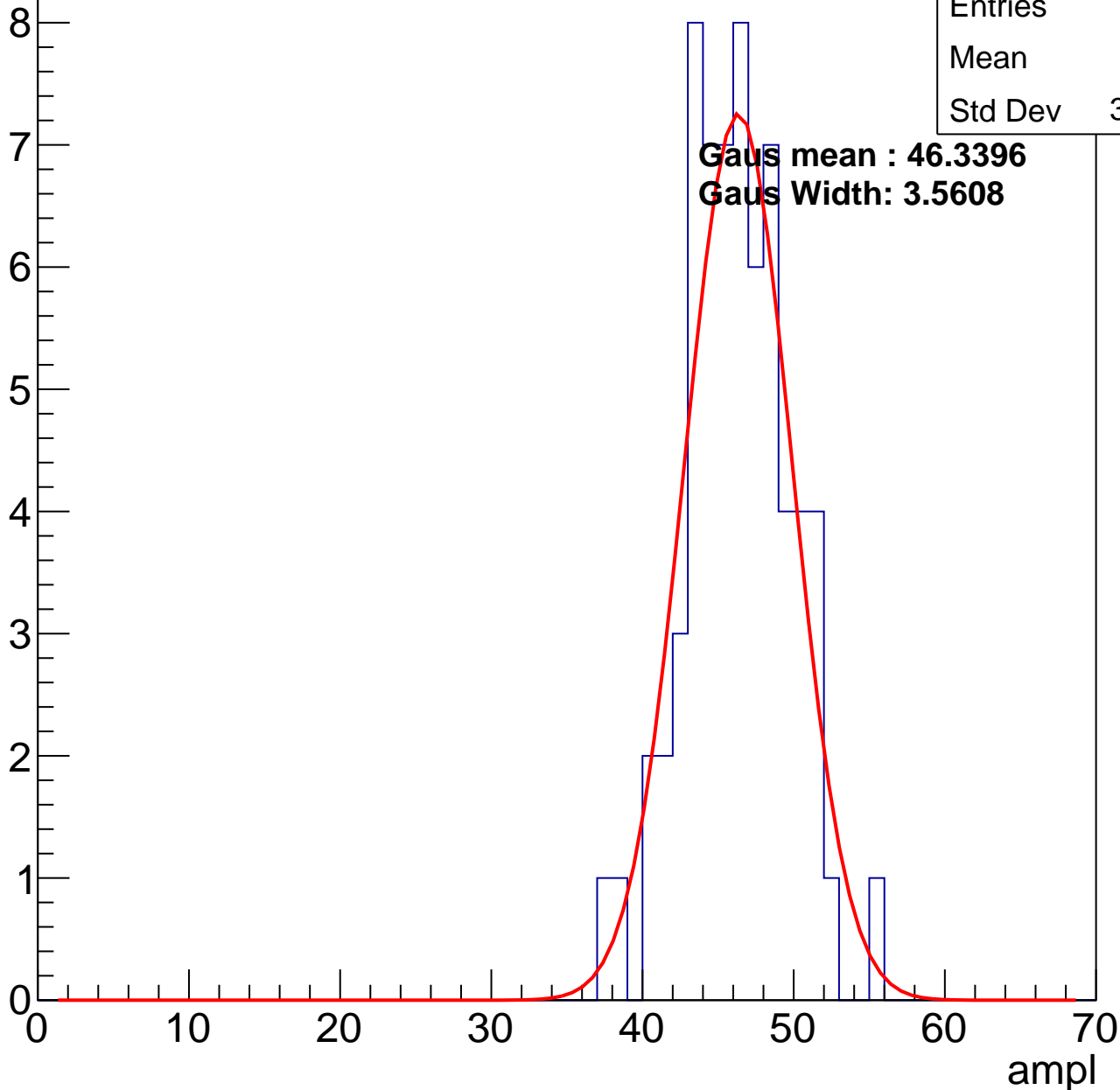
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	45.8
Std Dev	3.417

**Gaus mean : 46.3396**

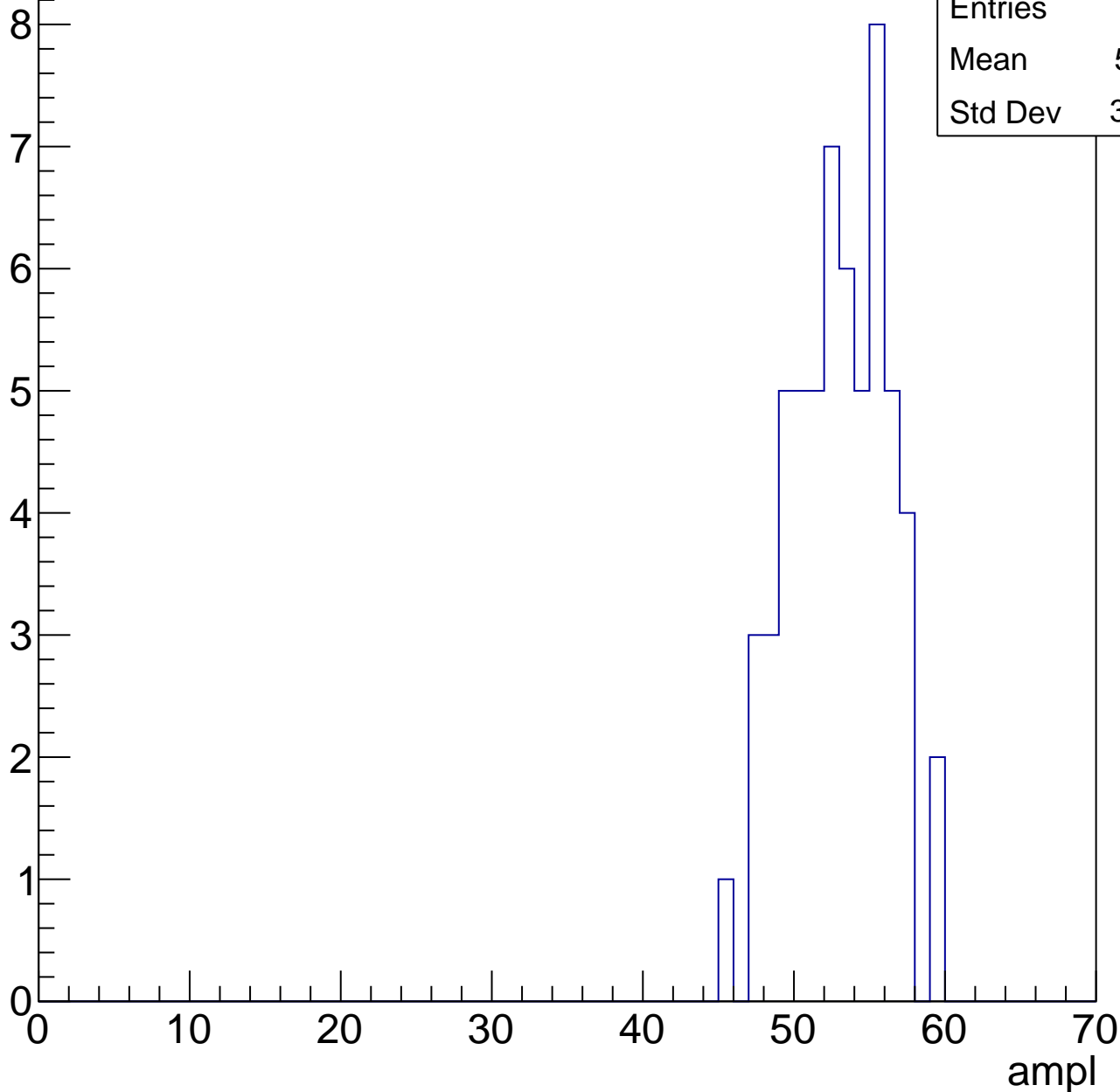
**Gaus Width: 3.5608**



# B0L001S, U10-ch23, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

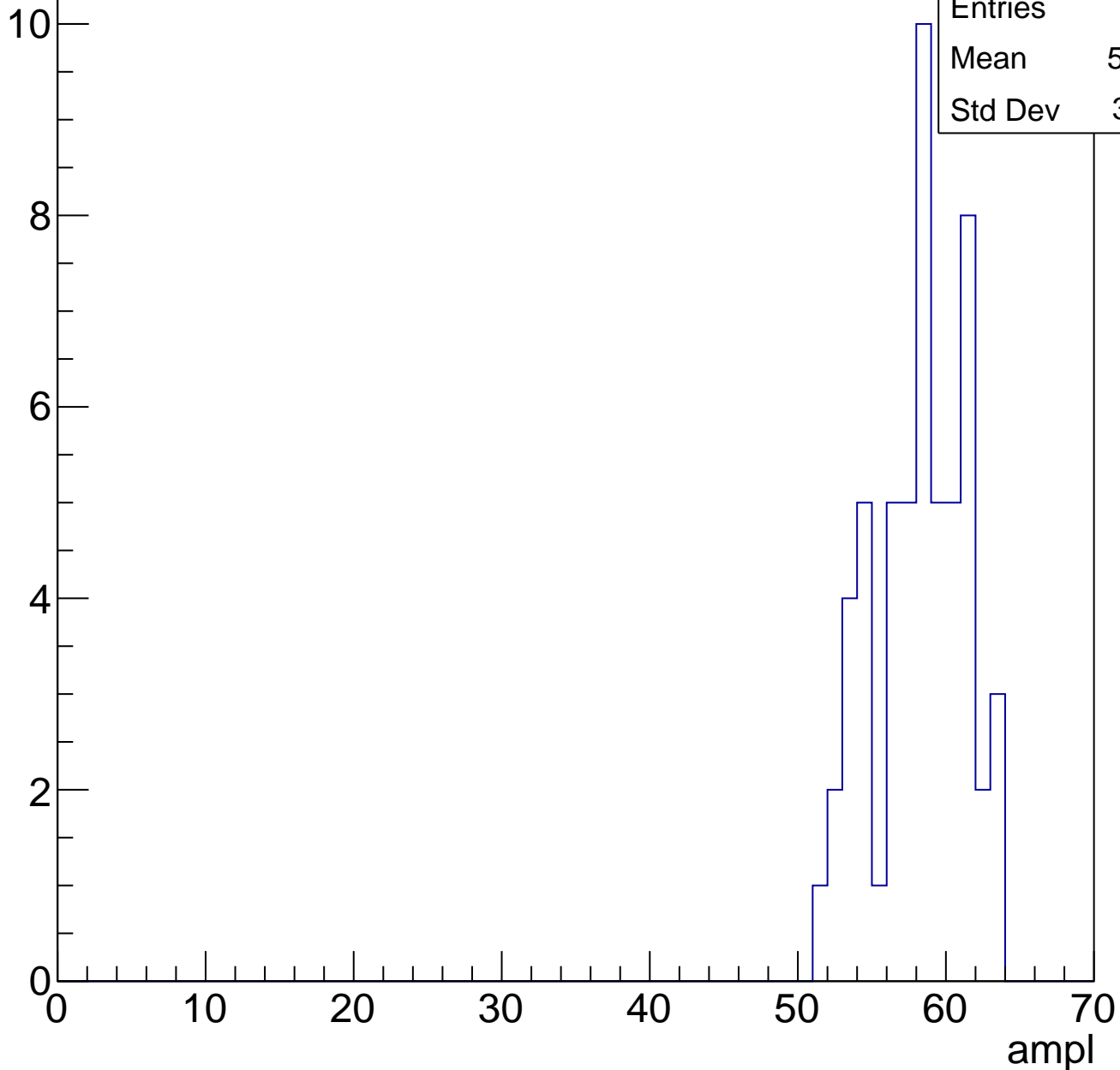


# B0L001S, U10-ch23, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	56
Mean	57.73
Std Dev	3.091

Entry

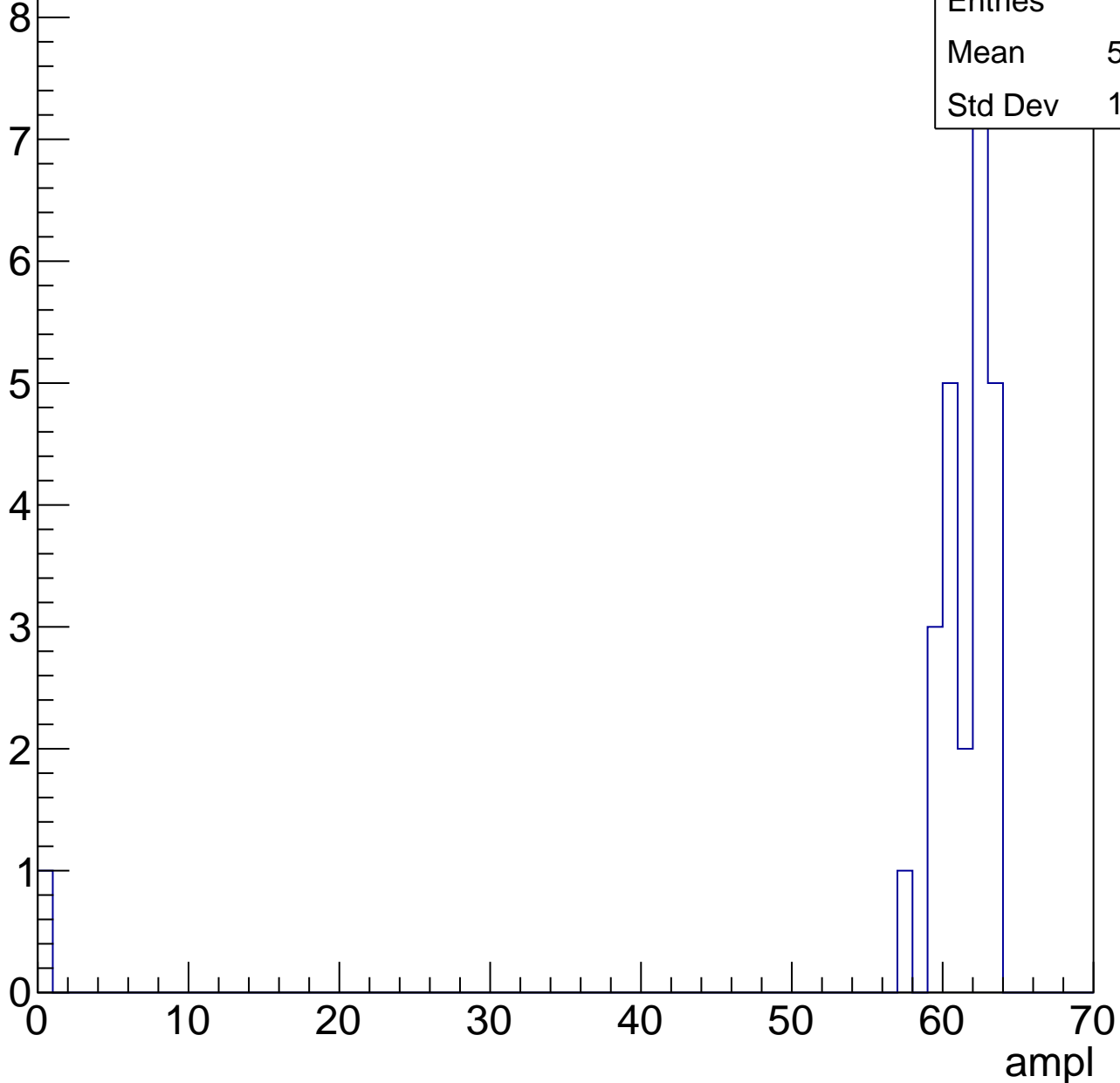


# B0L001S, U10-ch23, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	25
Mean	58.68
Std Dev	12.08



# B0L001S, U10-ch23, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

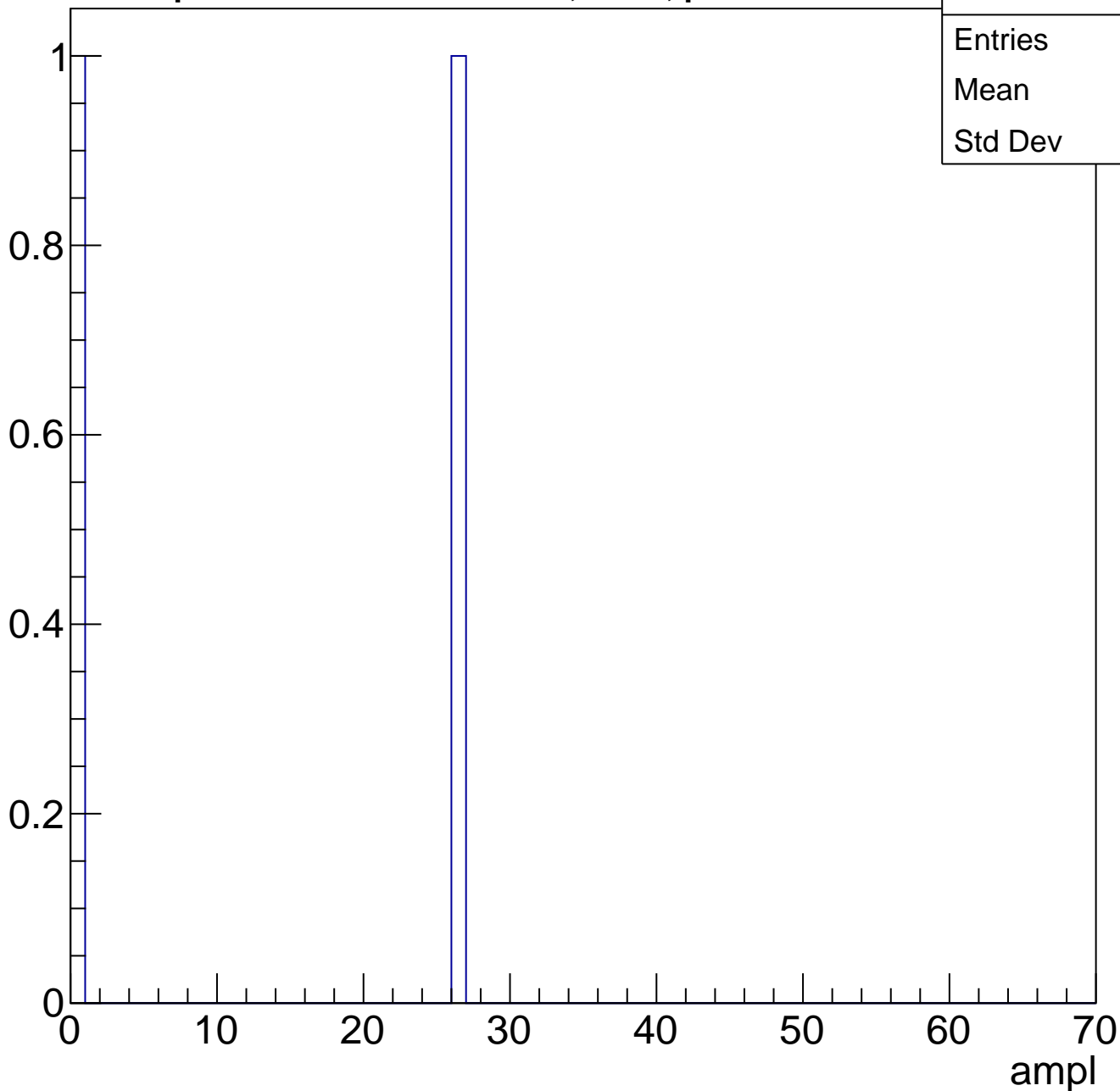




# B0L001S, U10-ch23, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	13
Std Dev	13

# B0L001S, U10-ch24, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	59
Mean	30.68
Std Dev	3.165

**Gaus mean : 31.1642**

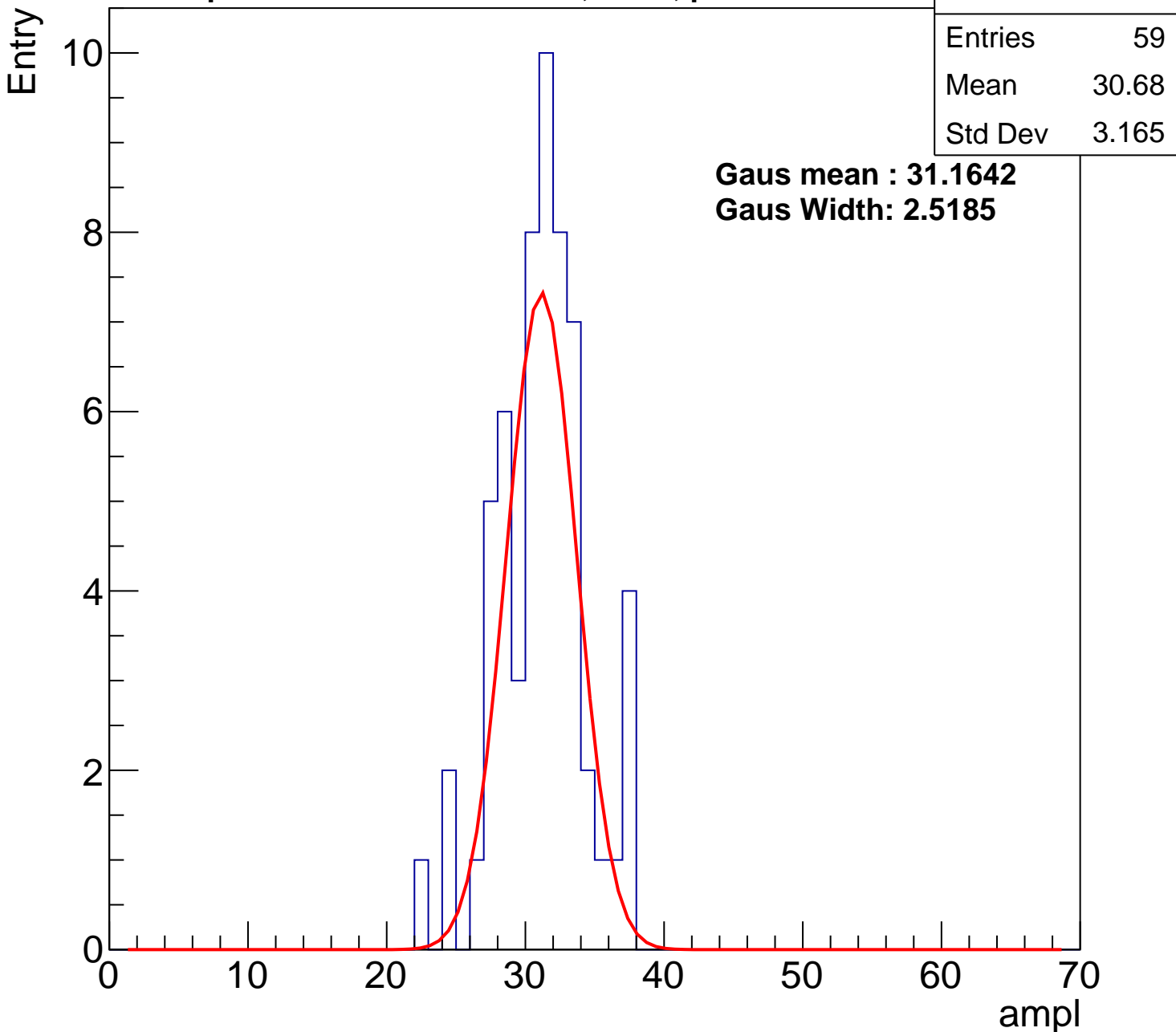
**Gaus Width: 2.5185**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U10-ch24, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	69
Mean	37.3
Std Dev	3.145

**Gaus mean : 38.2143**

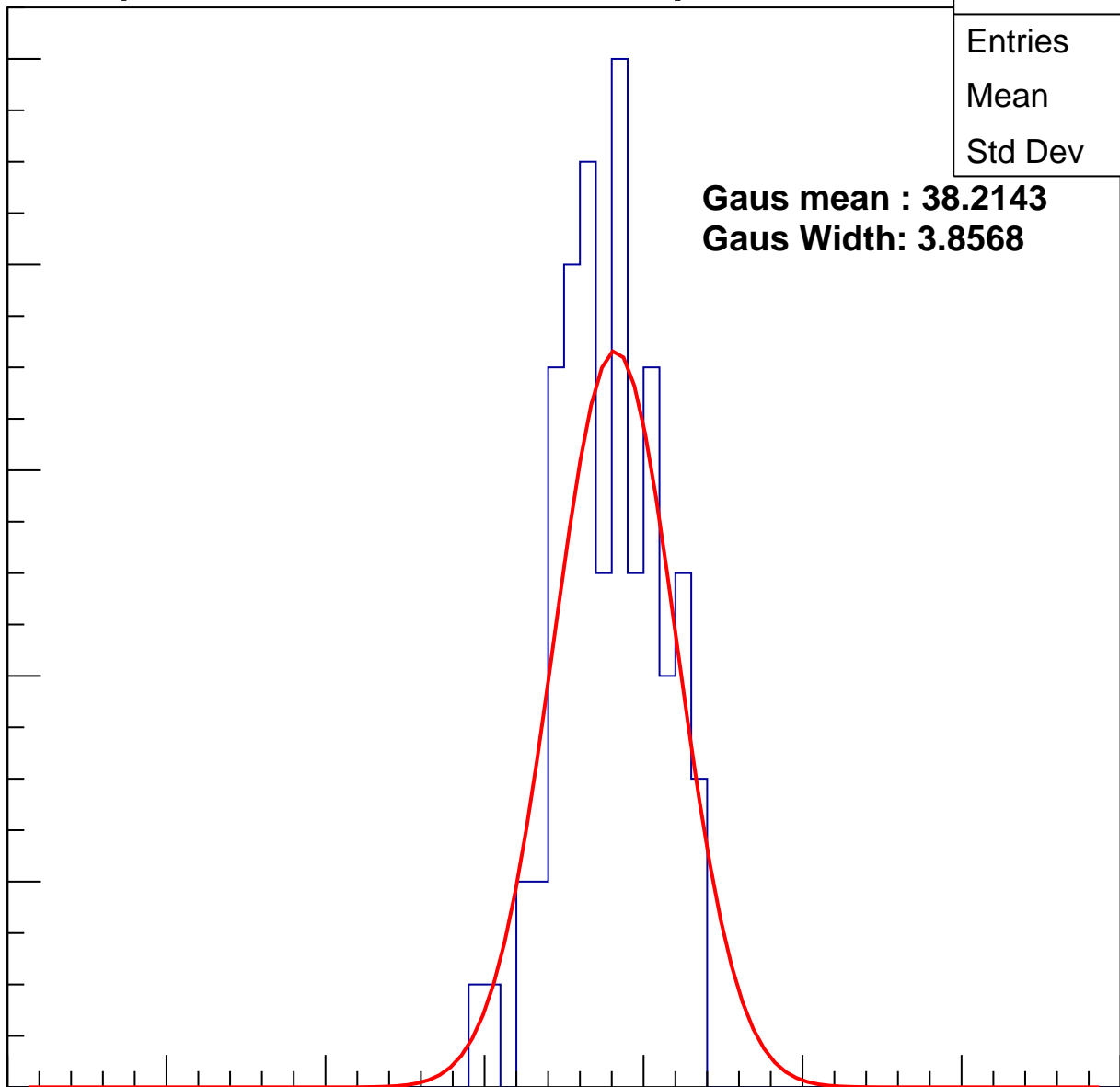
**Gaus Width: 3.8568**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B0L001S, U10-ch24, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	78
Mean	44.26
Std Dev	3.966

**Gaus mean : 45.0502**

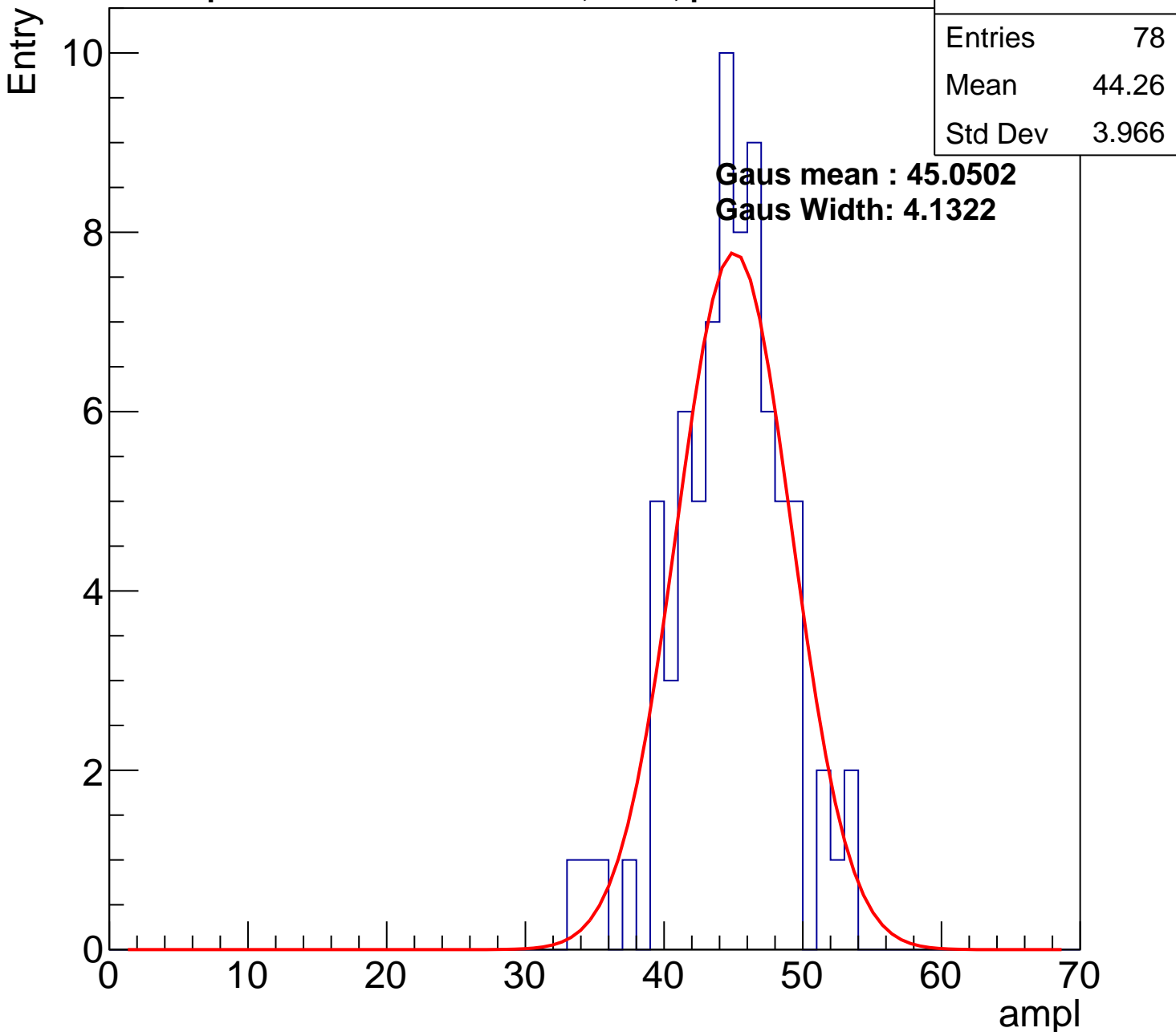
**Gaus Width: 4.1322**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

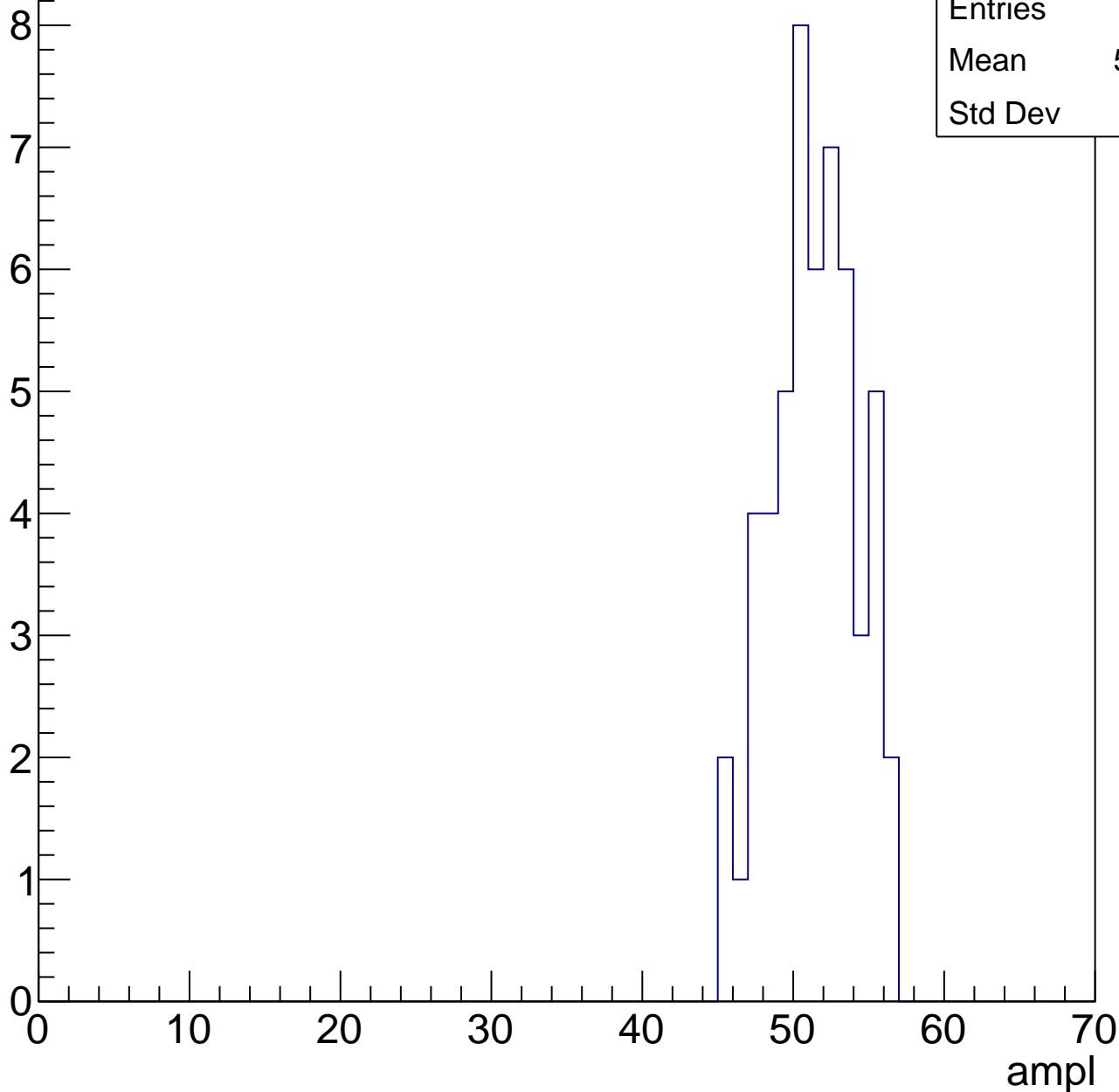


# B0L001S, U10-ch24, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	50.91
Std Dev	2.79



# B0L001S, U10-ch24, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

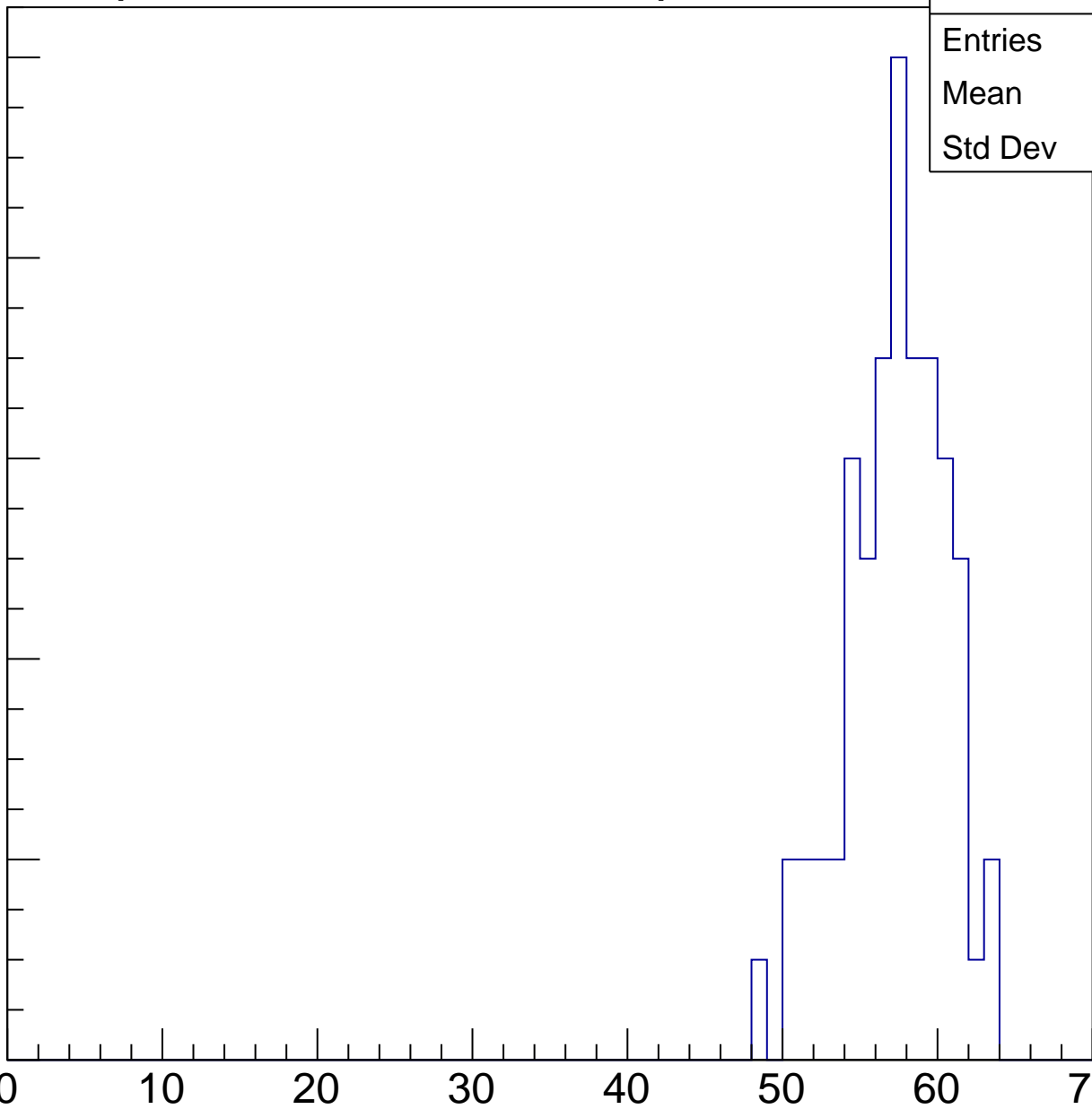
Entries	65
Mean	56.82
Std Dev	3.229

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

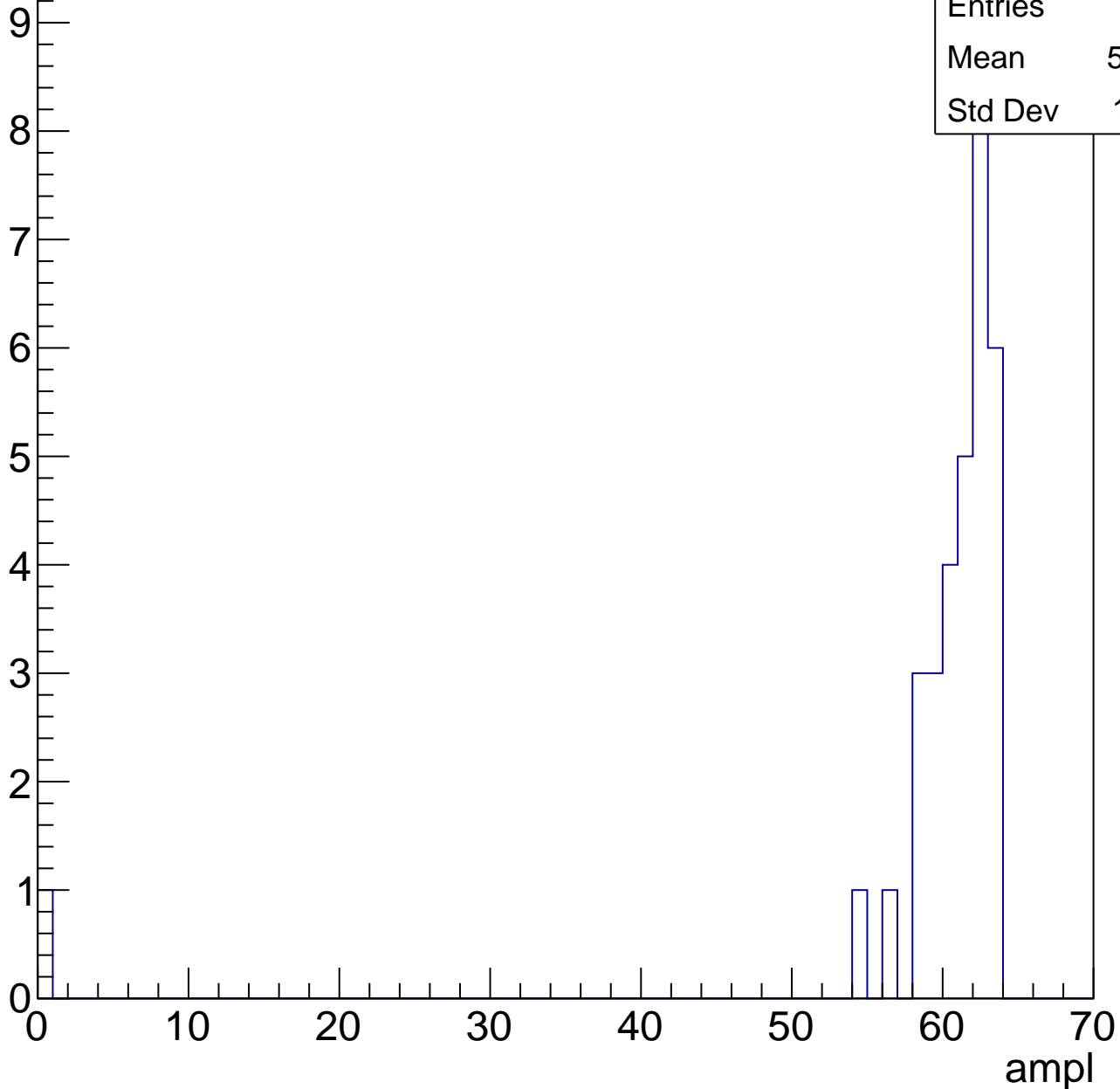


# B0L001S, U10-ch24, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	33
Mean	58.85
Std Dev	10.61



# B0L001S, U10-ch24, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch24, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	3
Mean	0
Std Dev	0

# B0L001S, U10-ch25, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	75
Mean	29.37
Std Dev	3.063

**Gaus mean : 30.1354**

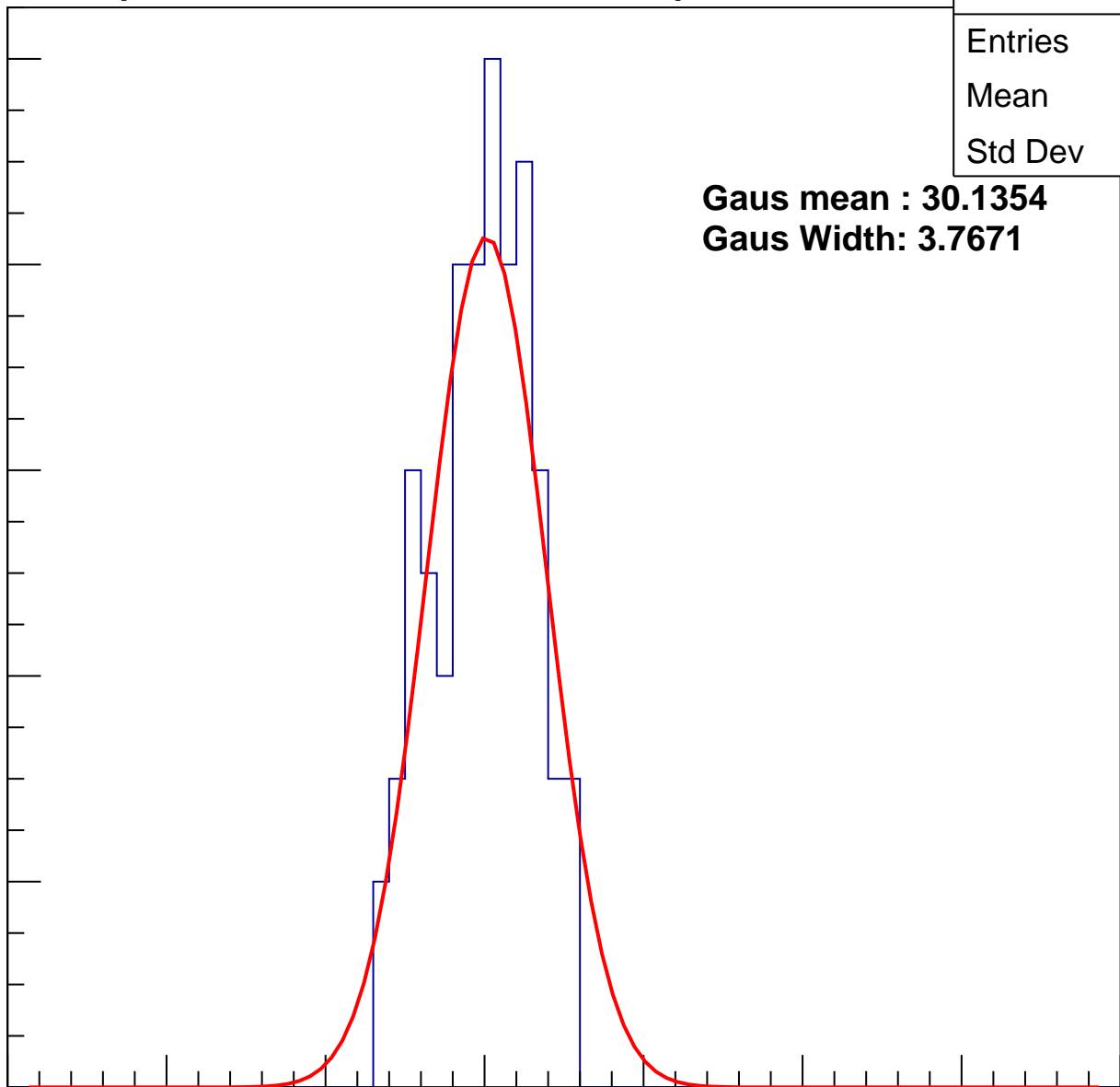
**Gaus Width: 3.7671**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U10-ch25, adc1

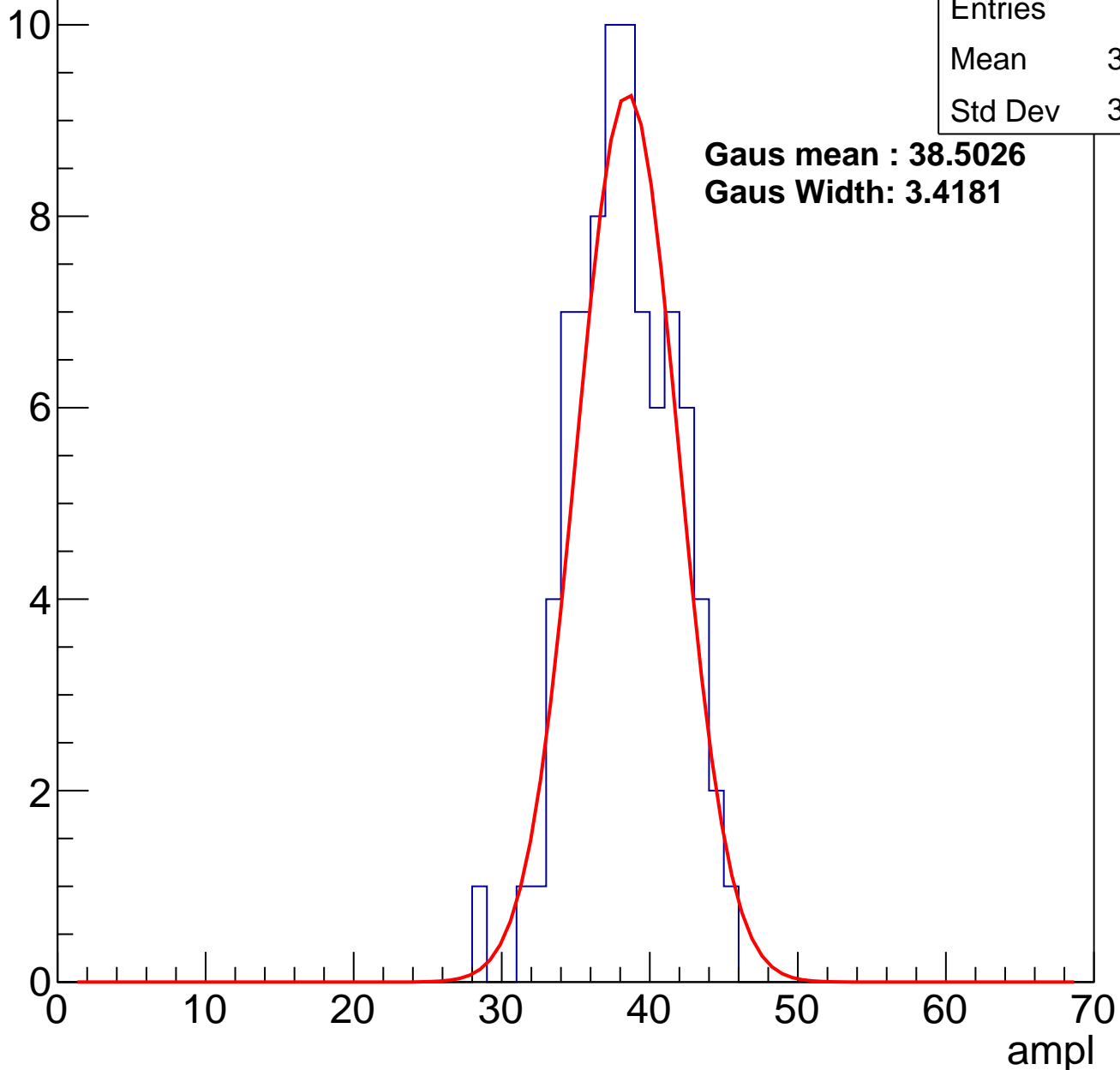
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	82
Mean	37.82
Std Dev	3.332

**Gaus mean : 38.5026**

**Gaus Width: 3.4181**

Entry



# B0L001S, U10-ch25, adc2

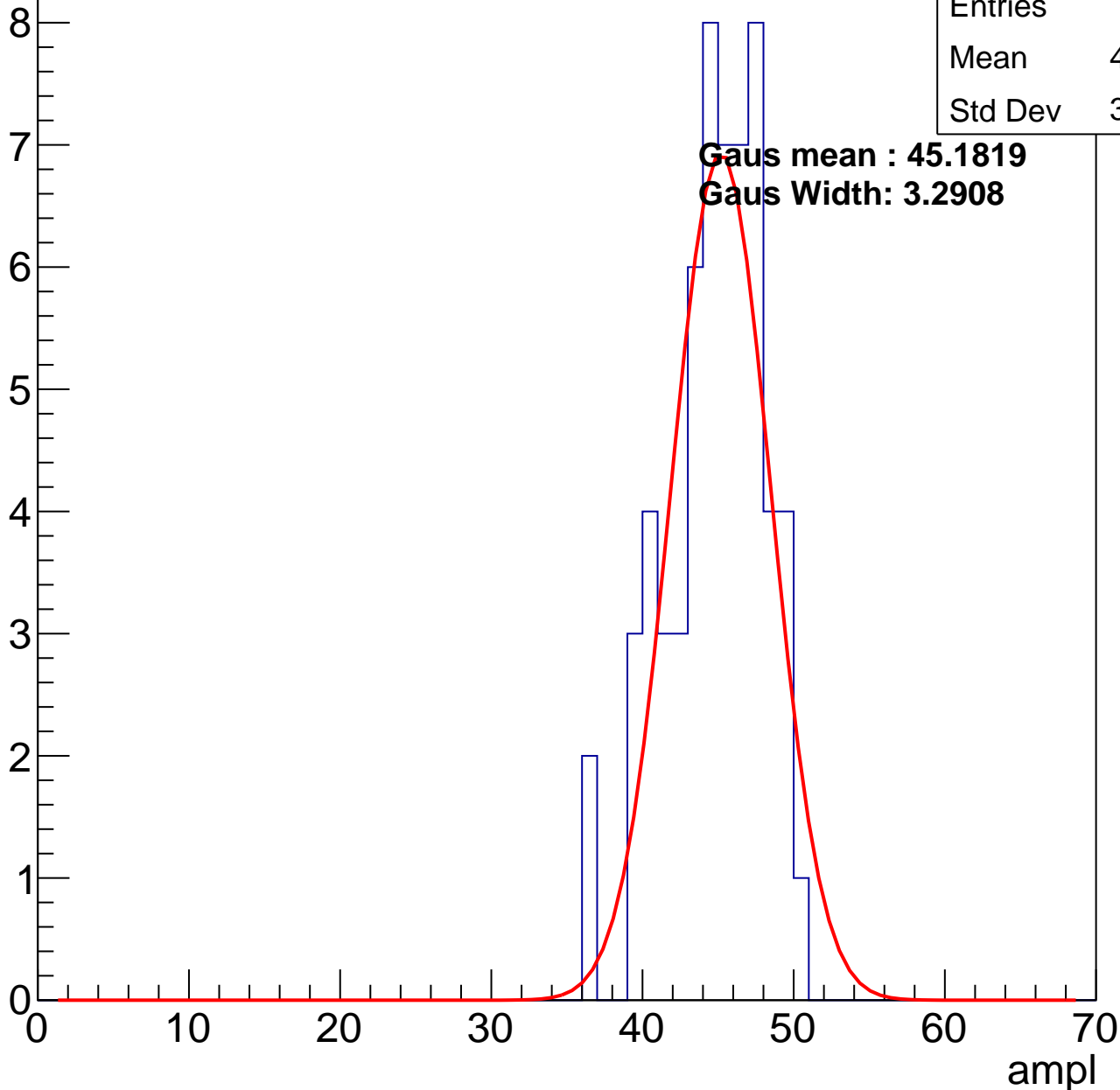
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	44.32
Std Dev	3.196

**Gaus mean : 45.1819**

**Gaus Width: 3.2908**



# B0L001S, U10-ch25, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	68
Mean	51.1
Std Dev	3.268

Entry

10

8

6

4

2

0

0

10

20

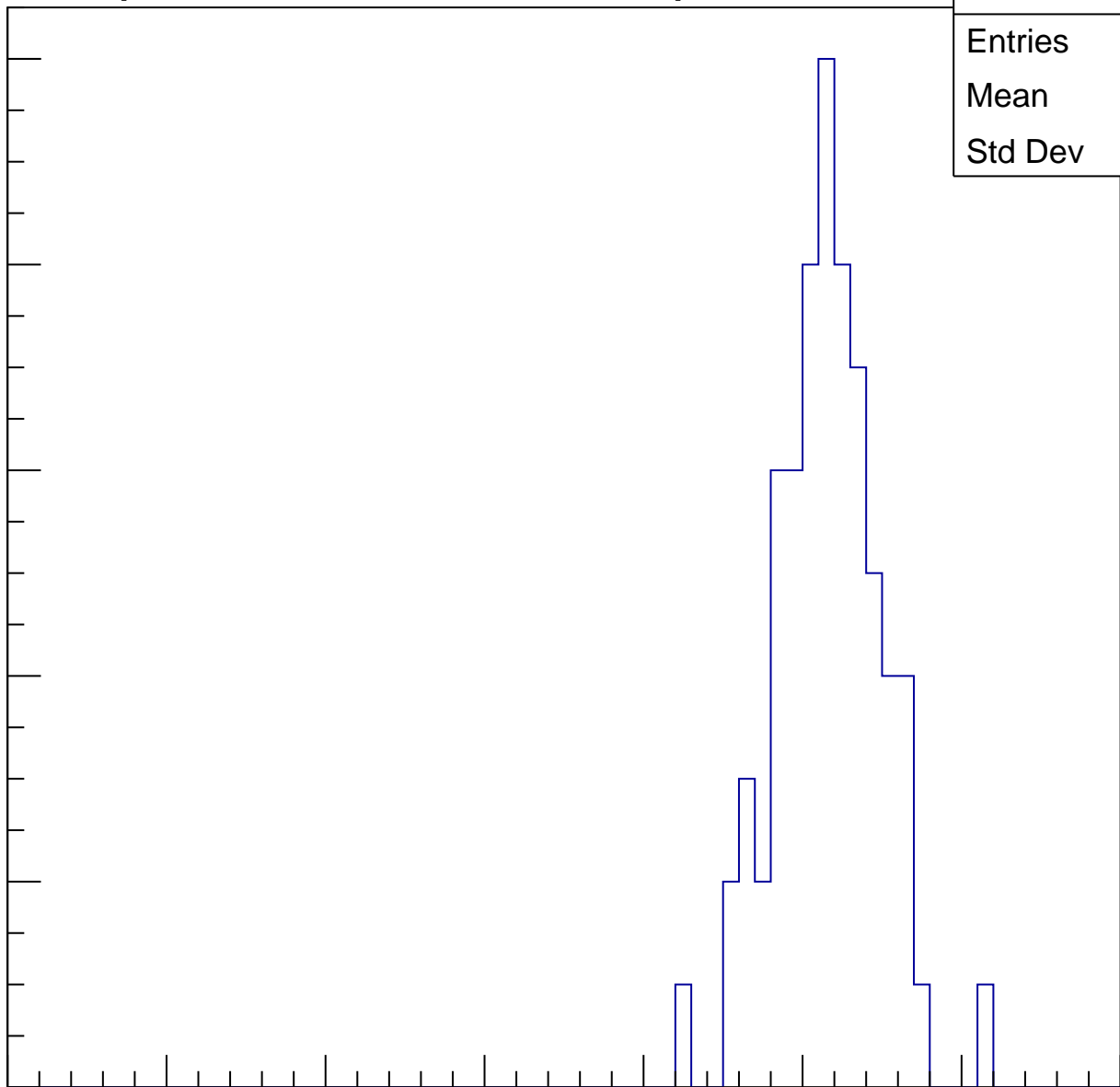
30

40

50

60

ampl

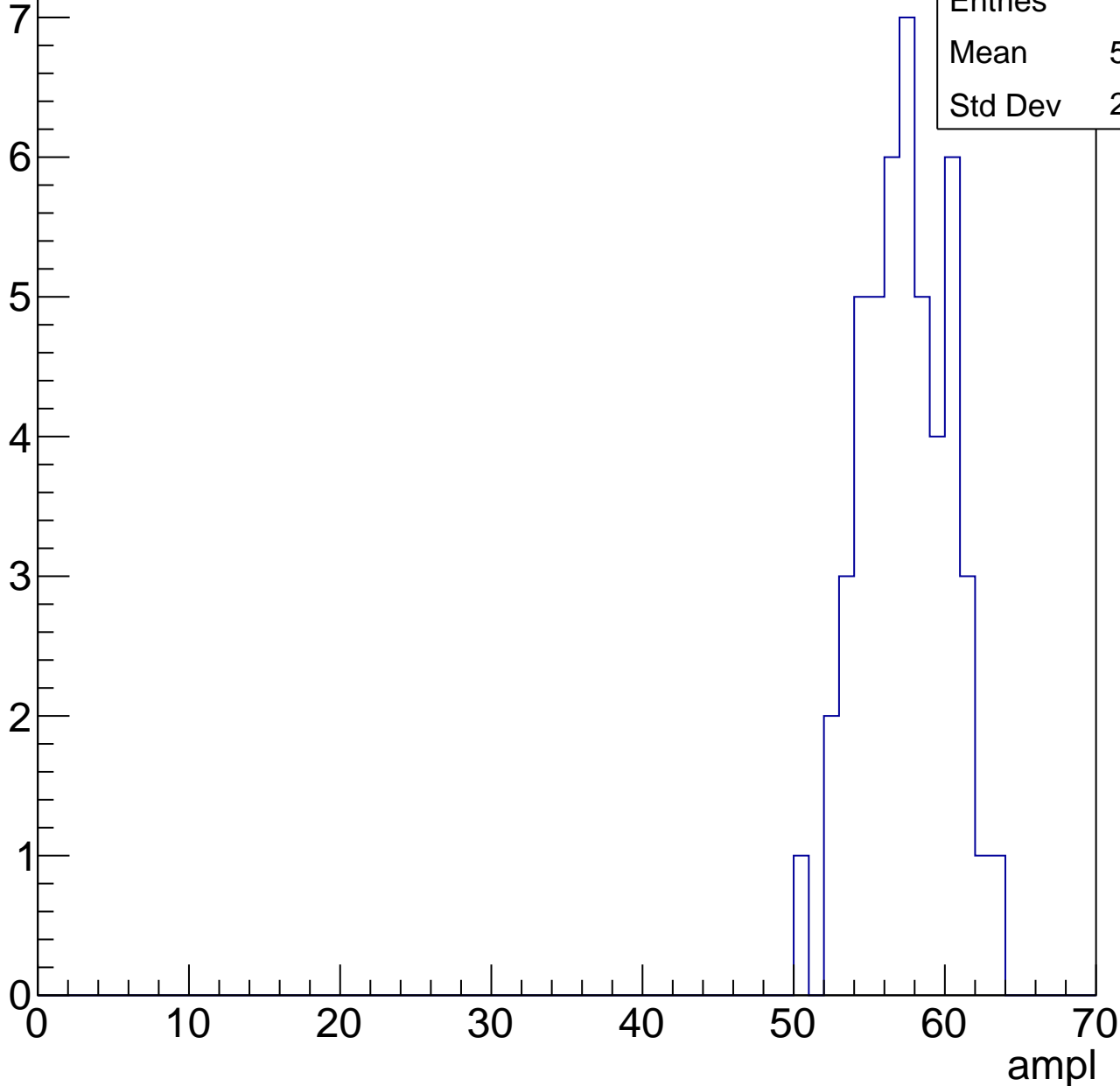


# B0L001S, U10-ch25, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	49
Mean	56.88
Std Dev	2.862

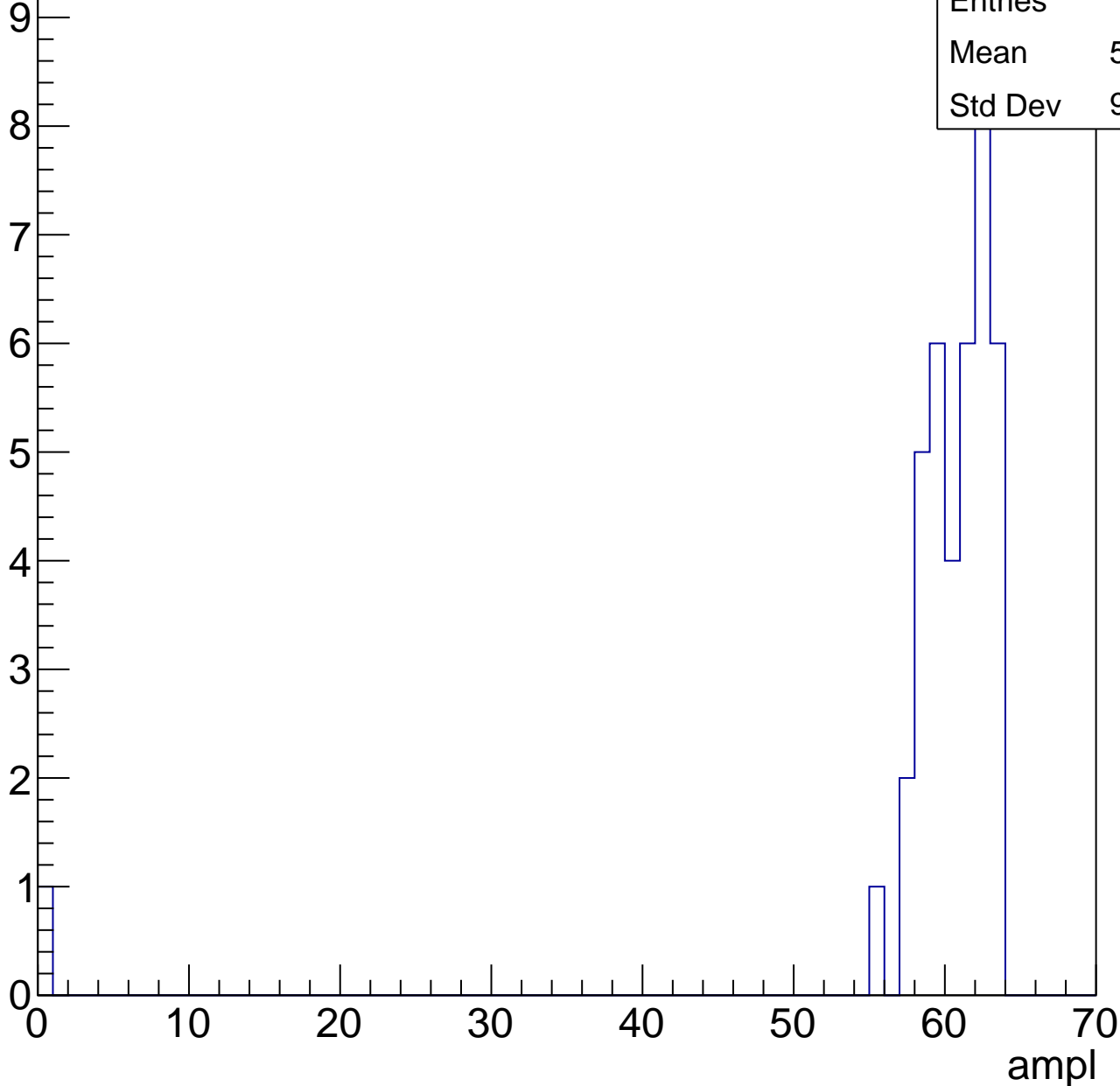


# B0L001S, U10-ch25, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	40
Mean	58.88
Std Dev	9.636



# B0L001S, U10-ch25, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch25, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U10-ch26, adc0

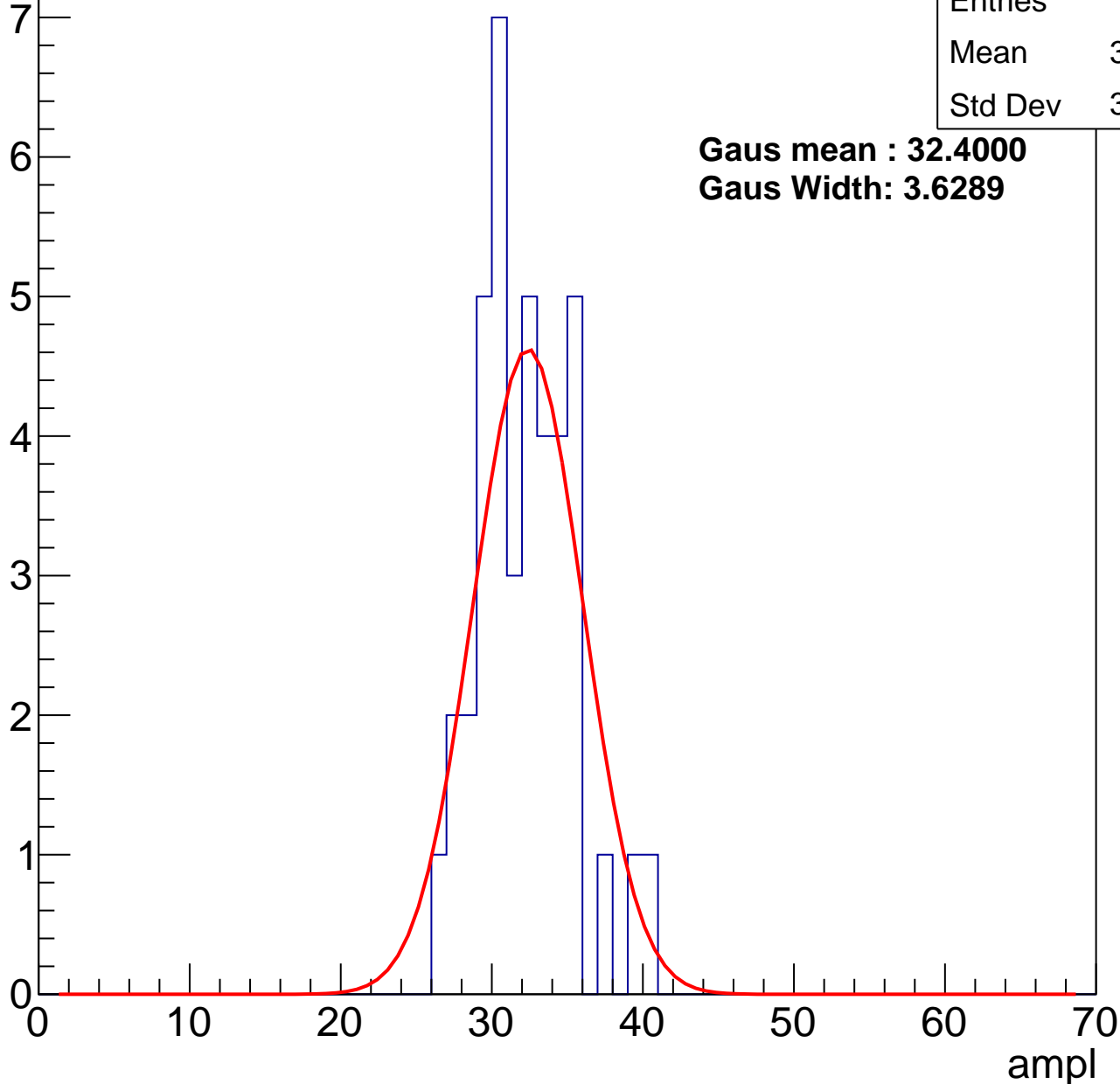
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	41
Mean	31.78
Std Dev	3.104

**Gaus mean : 32.4000**

**Gaus Width: 3.6289**



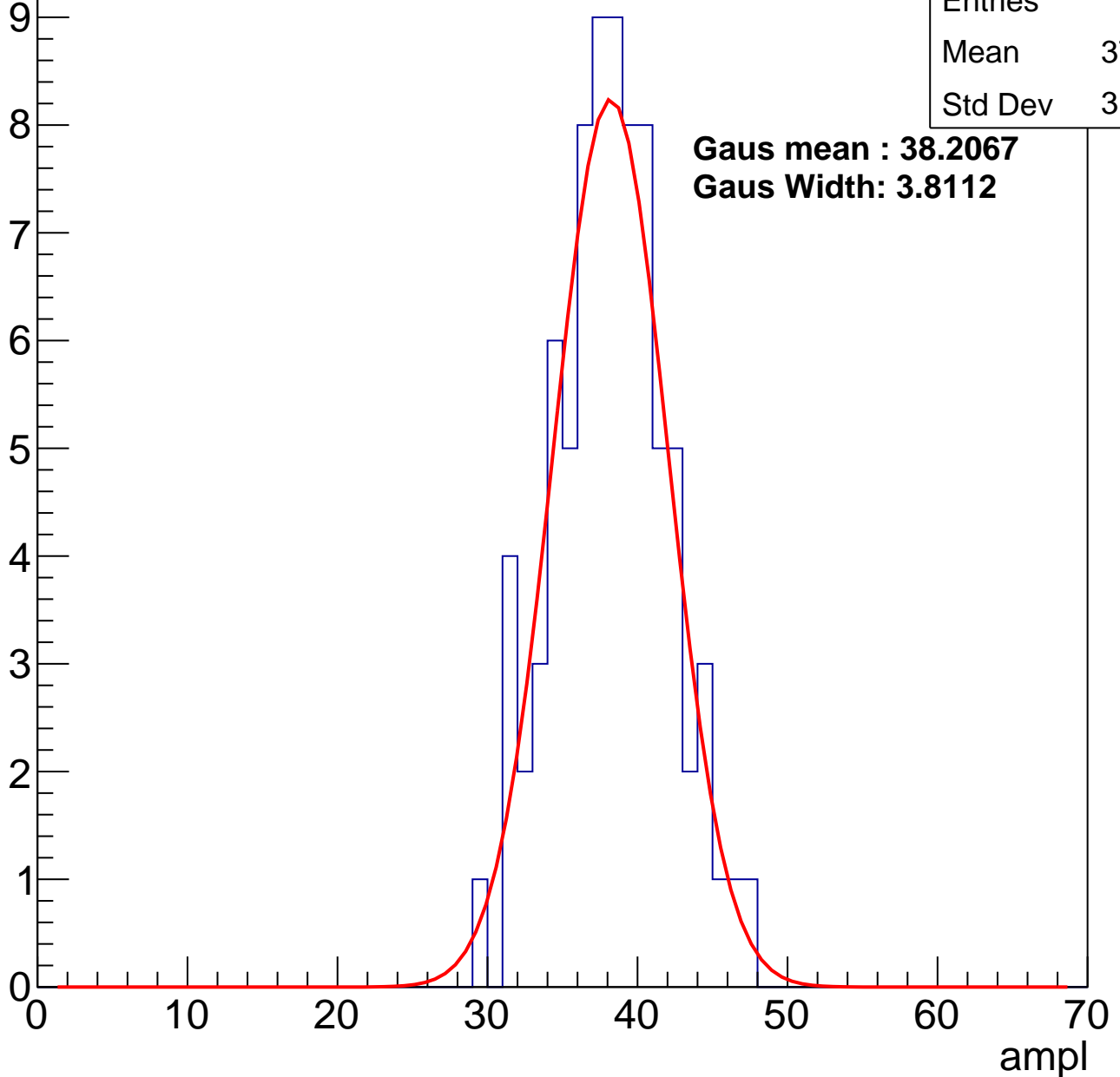
# B0L001S, U10-ch26, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	81
Mean	37.79
Std Dev	3.718

**Gaus mean : 38.2067**  
**Gaus Width: 3.8112**



# B0L001S, U10-ch26, adc2

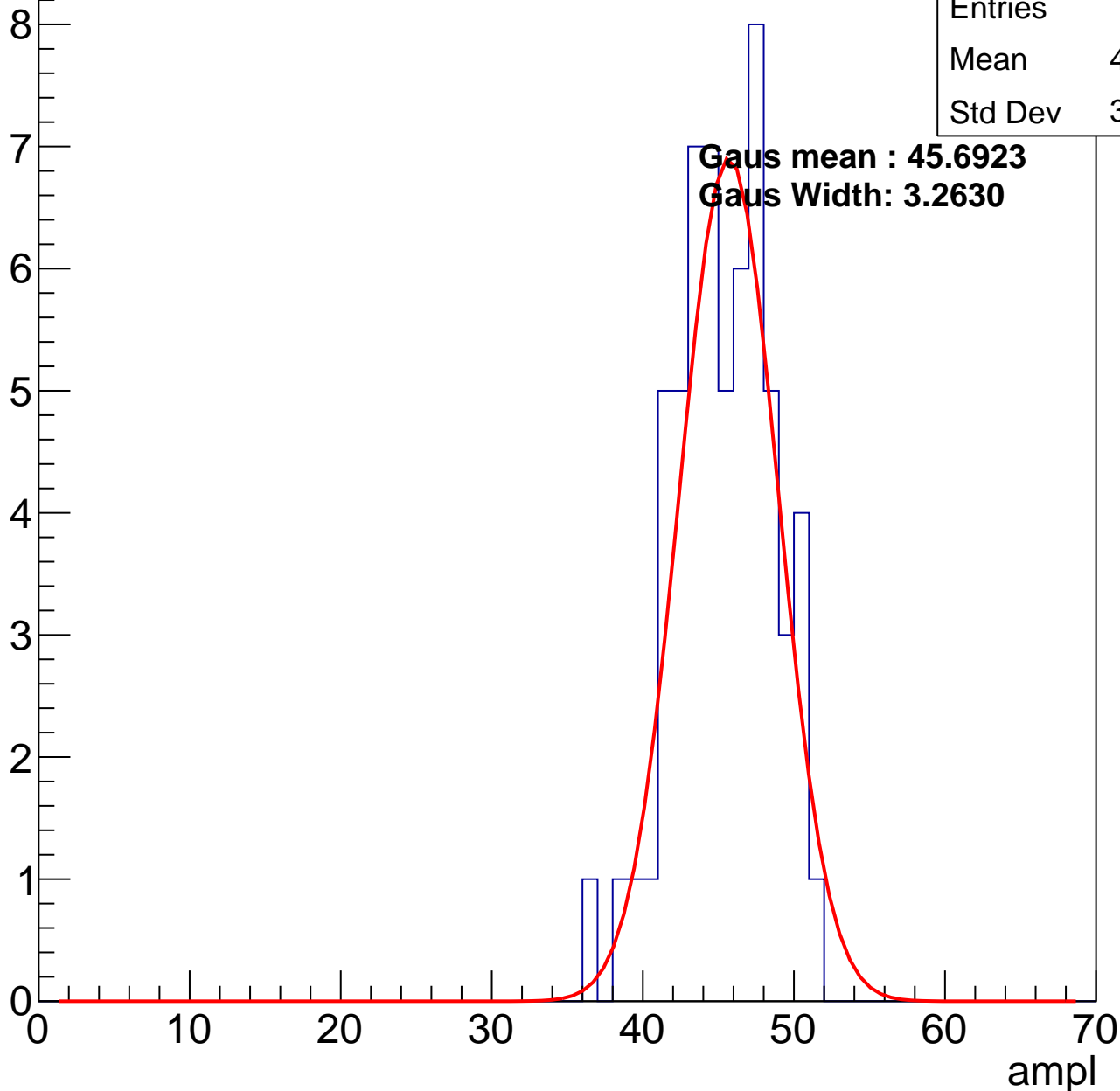
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	44.87
Std Dev	3.207

**Gaus mean : 45.6923**

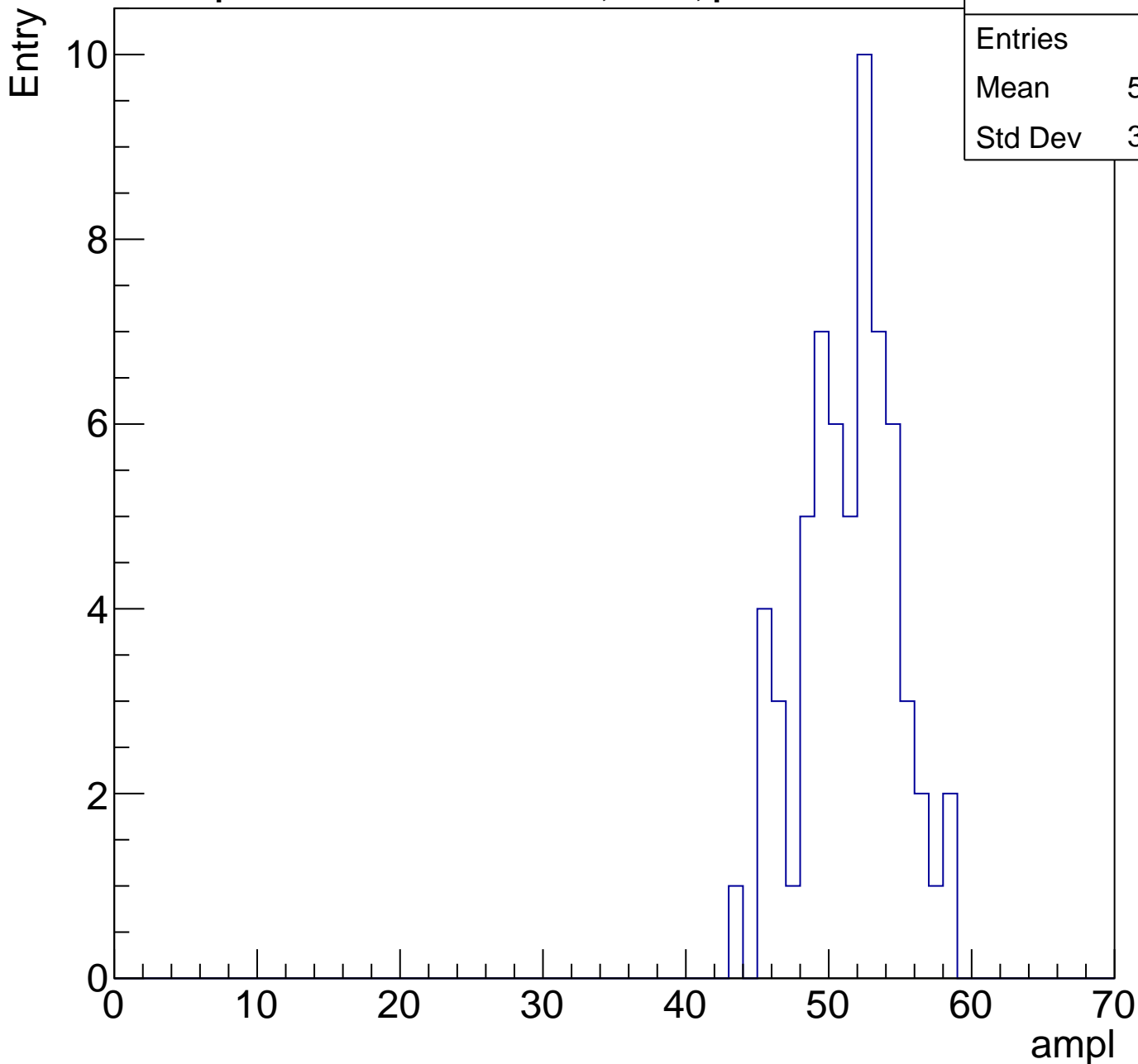
**Gaus Width: 3.2630**



# B0L001S, U10-ch26, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

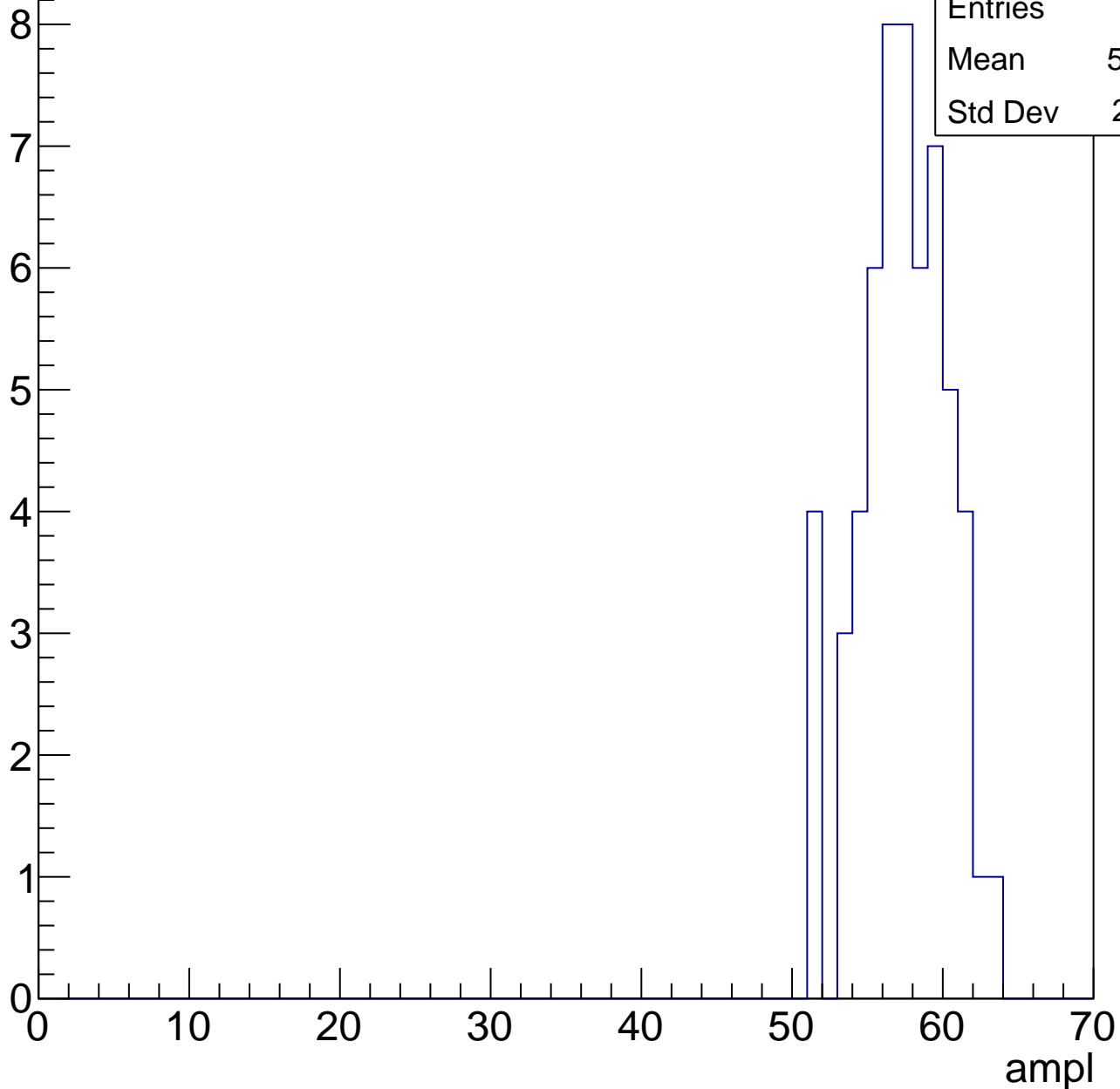
Entries	63
Mean	50.97
Std Dev	3.338



# B0L001S, U10-ch26, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

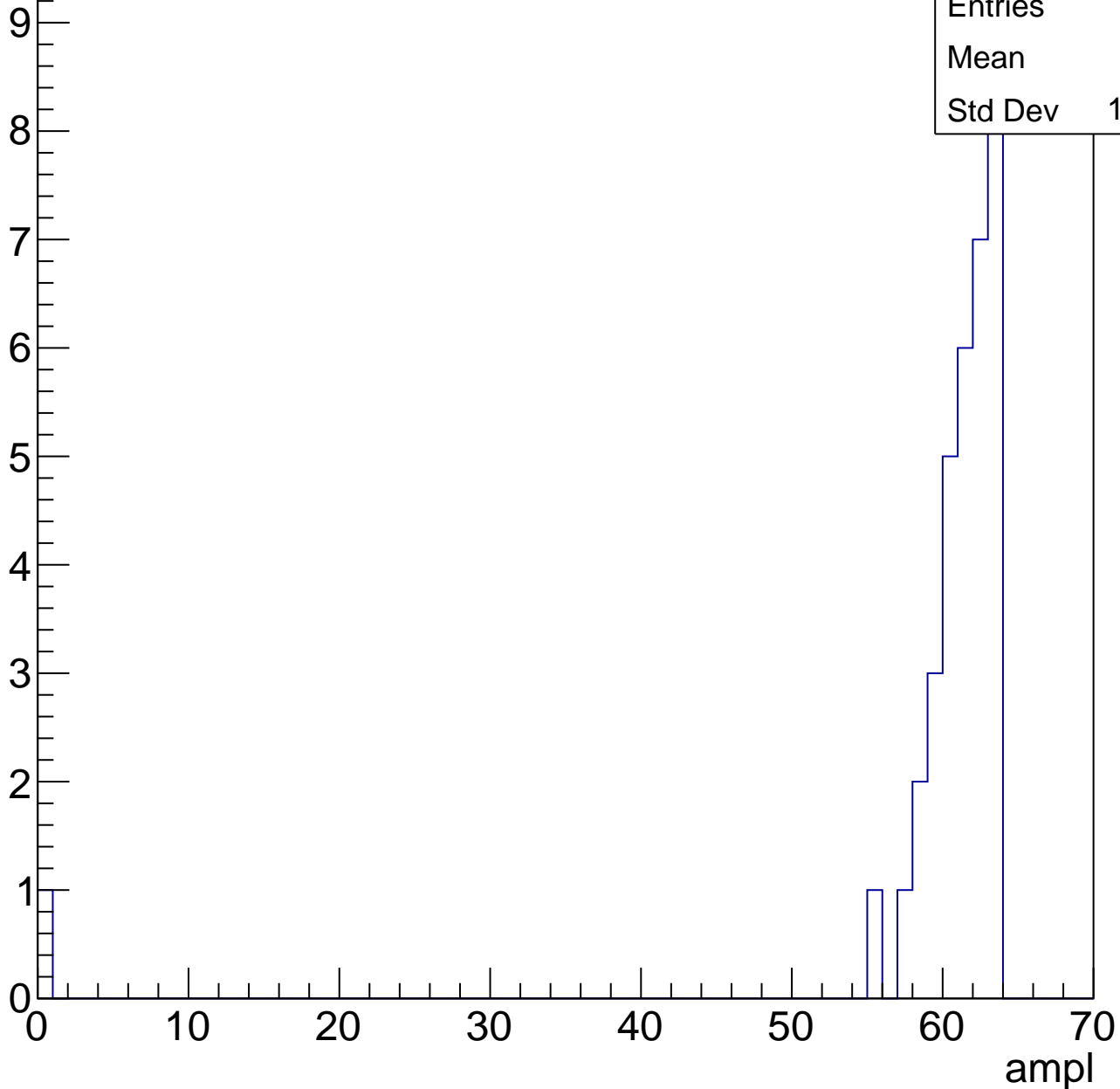


# B0L001S, U10-ch26, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	35
Mean	59.2
Std Dev	10.33



# B0L001S, U10-ch26, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	62
Std Dev	0

ampl



# B0L001S, U10-ch26, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L001S, U10-ch27, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	89
Mean	28.13
Std Dev	5.713

**Gaus mean : 30.4911**

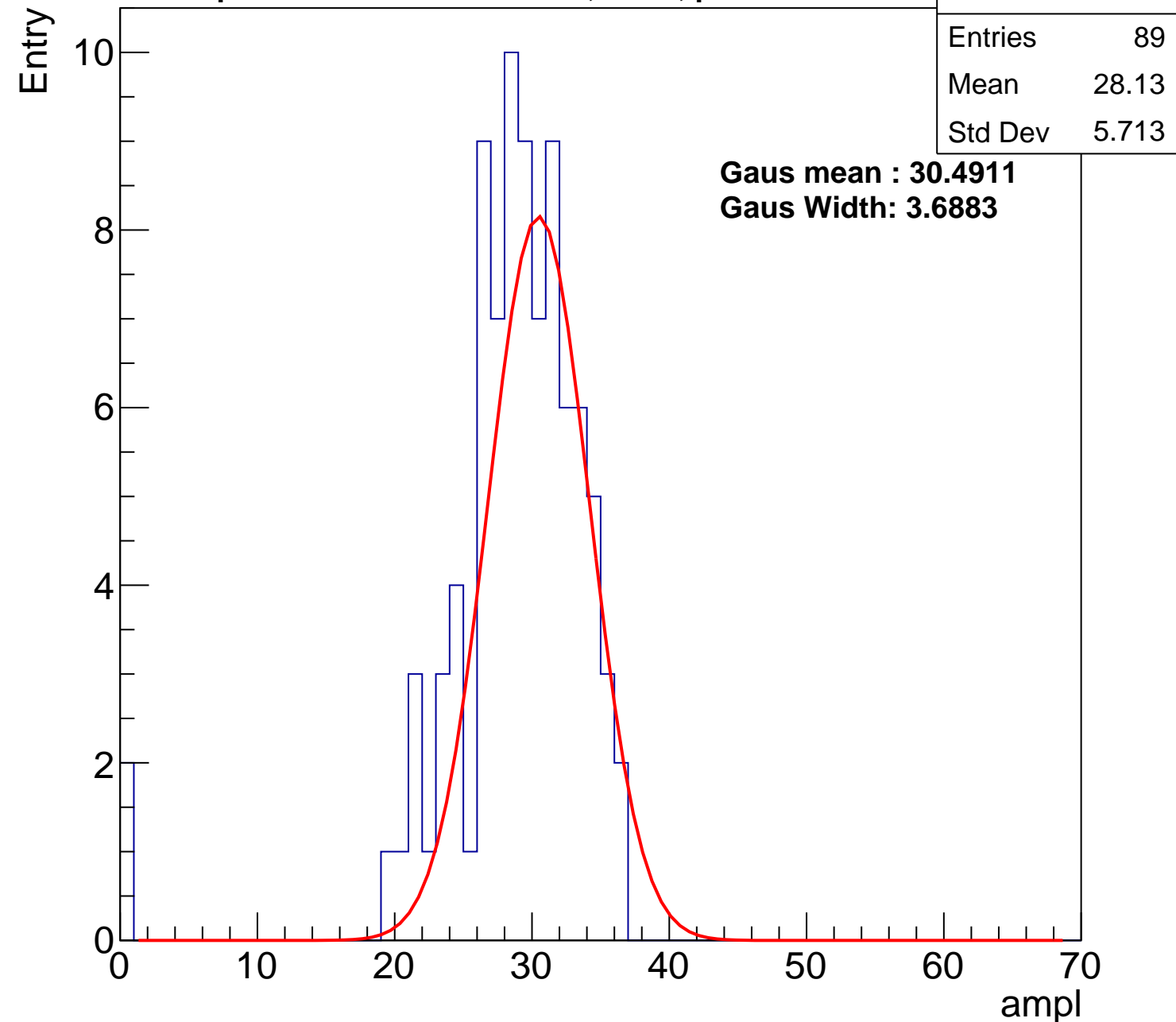
**Gaus Width: 3.6883**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U10-ch27, adc1

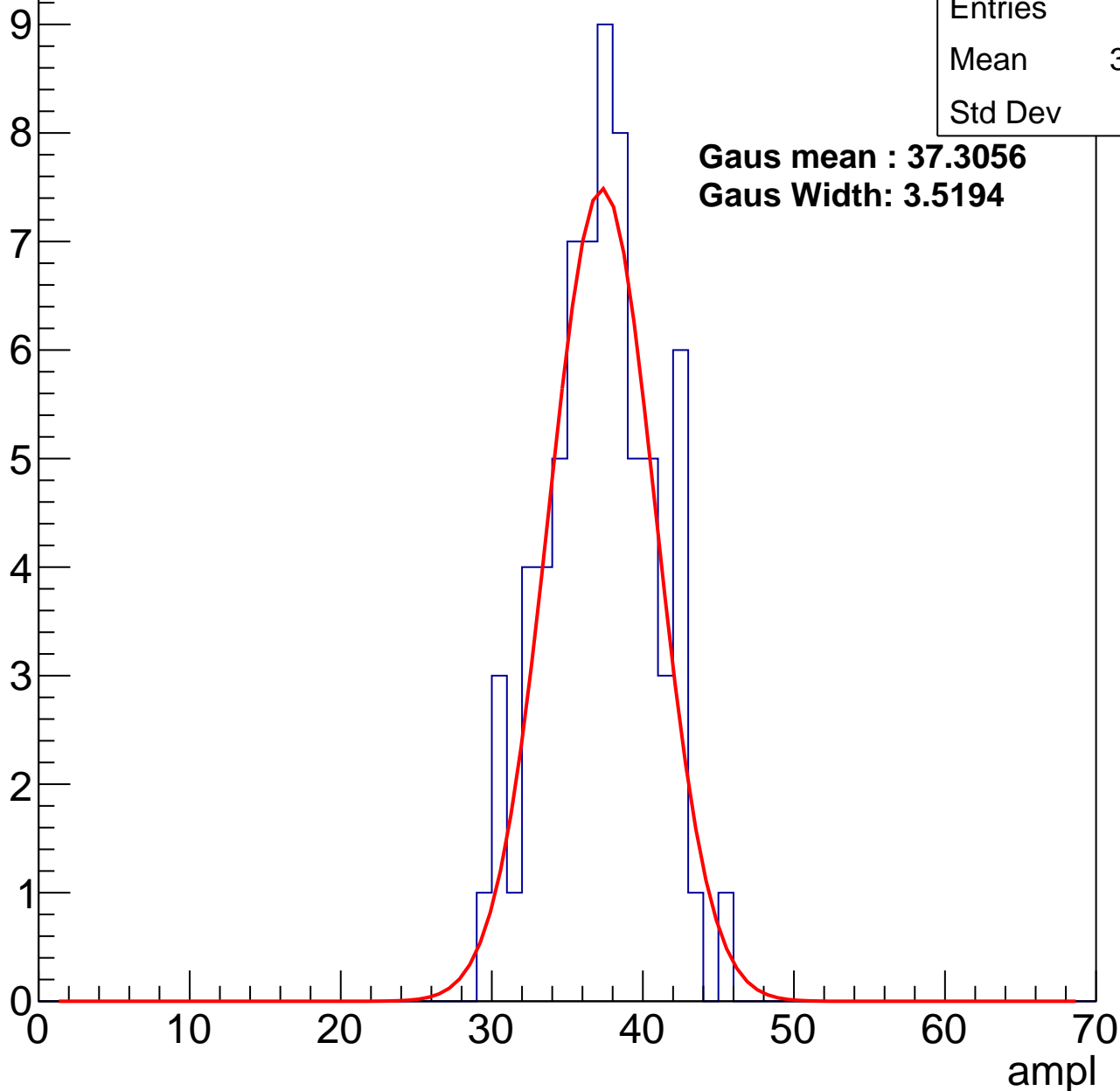
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	36.74
Std Dev	3.5

**Gaus mean : 37.3056**

**Gaus Width: 3.5194**



# B0L001S, U10-ch27, adc2

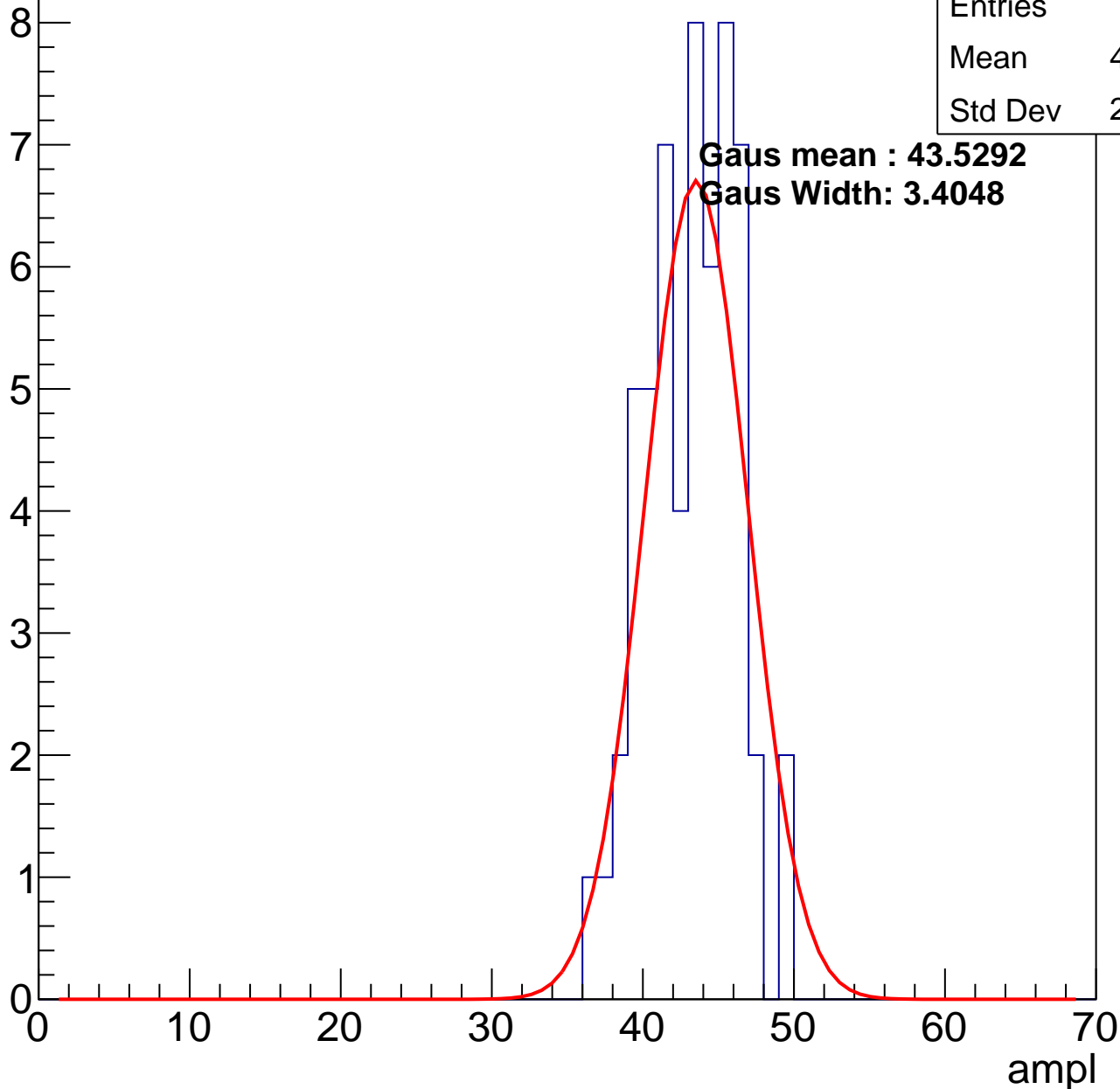
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	42.78
Std Dev	2.919

**Gaus mean : 43.5292**

**Gaus Width: 3.4048**



# B0L001S, U10-ch27, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	69
Mean	49.33
Std Dev	2.759

Entry

10

8

6

4

2

0

0

10

20

30

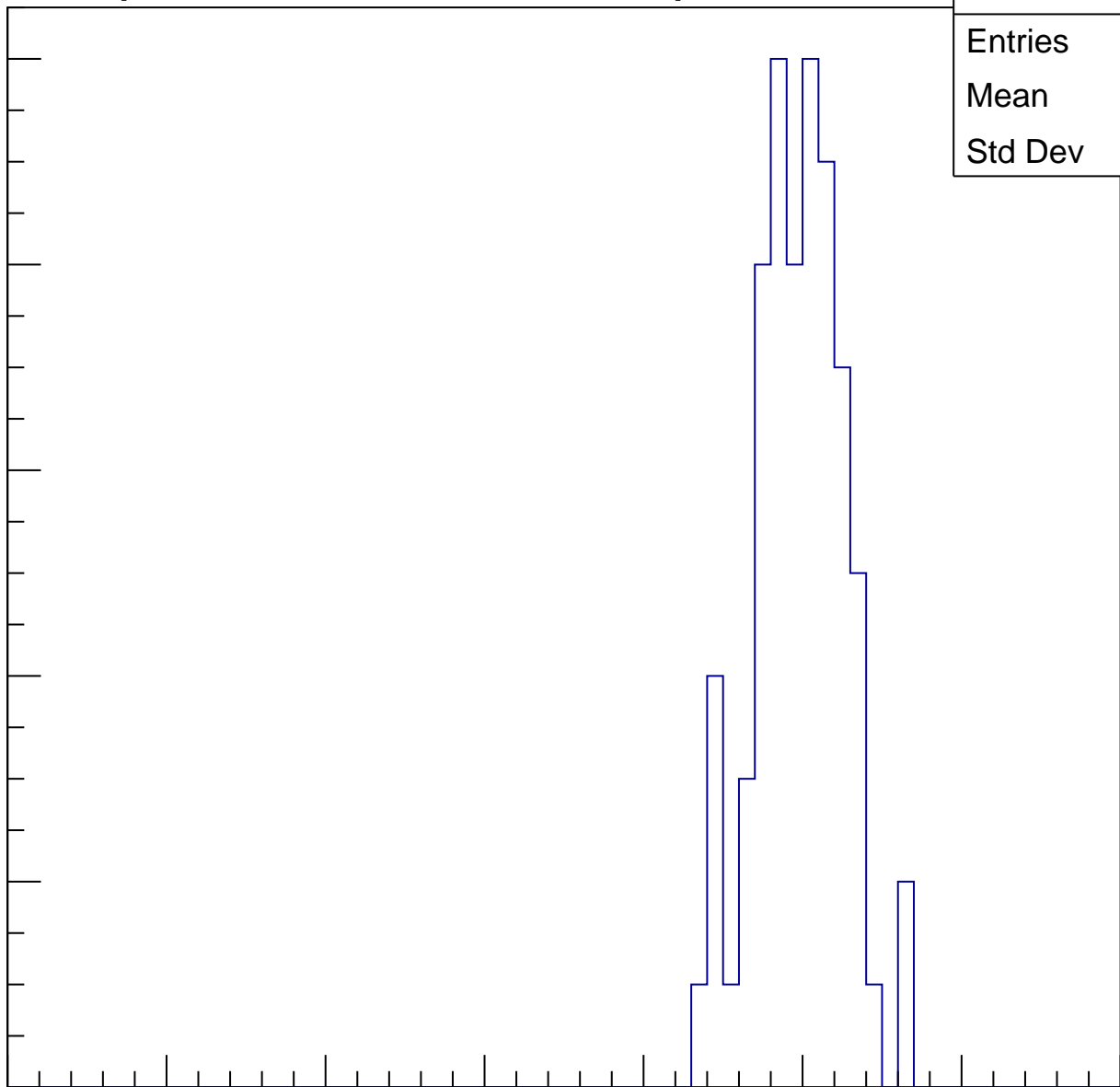
40

50

60

70

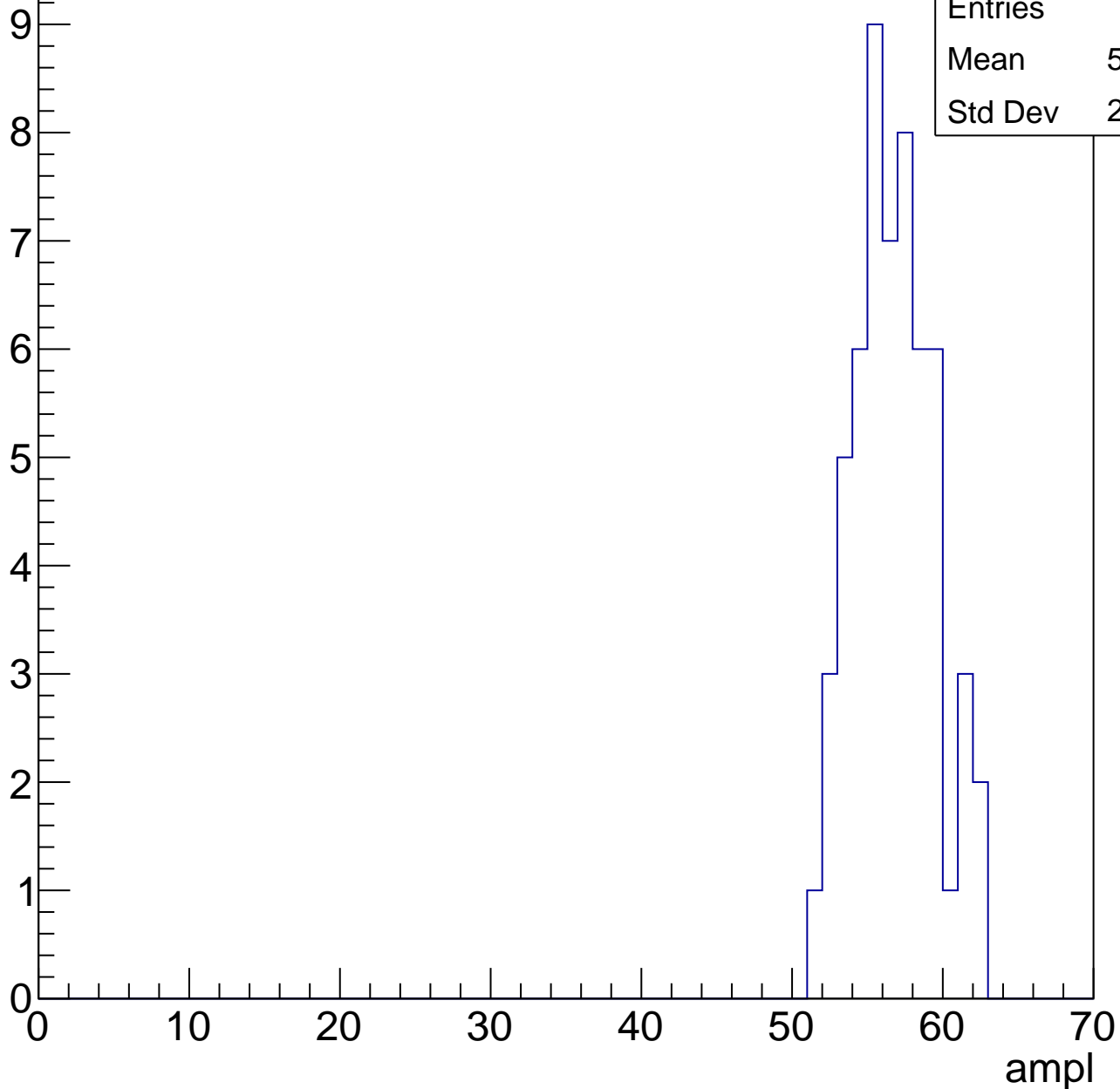
ampl



# B0L001S, U10-ch27, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

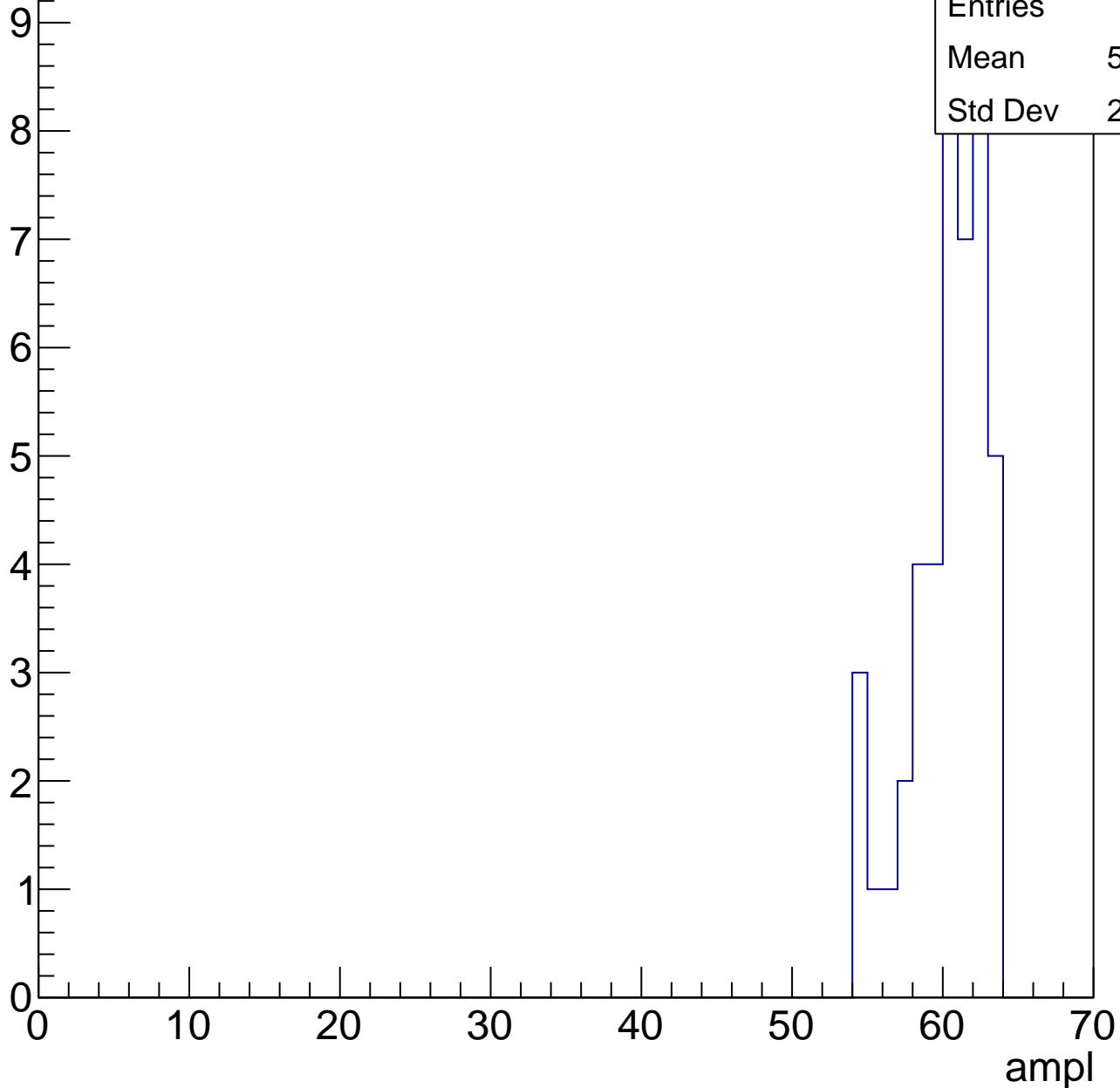


Entries	57
Mean	56.28
Std Dev	2.634

# B0L001S, U10-ch27, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

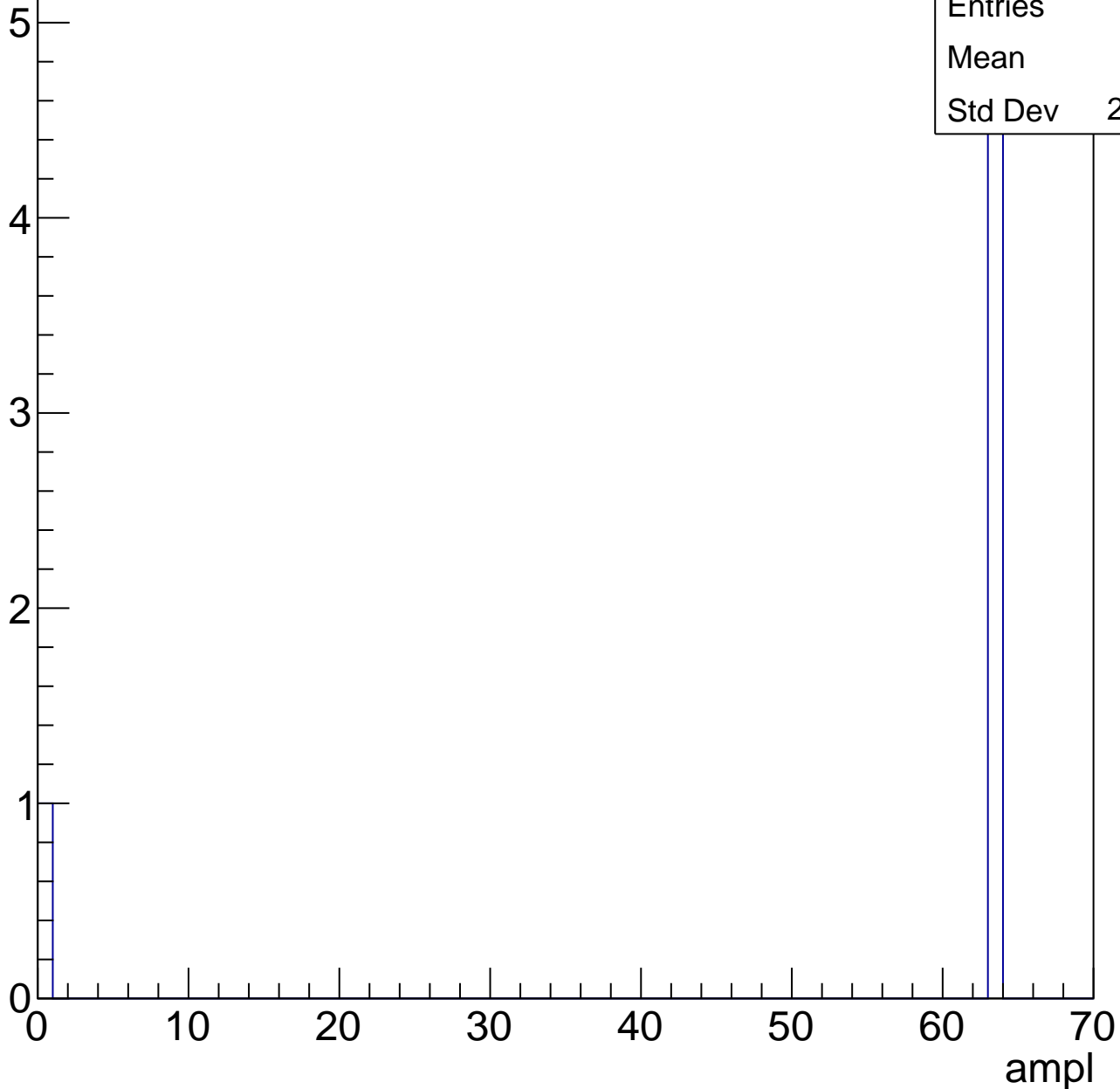


# B0L001S, U10-ch27, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	6
Mean	52.5
Std Dev	23.48





# B0L001S, U10-ch27, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U10-ch28, adc0

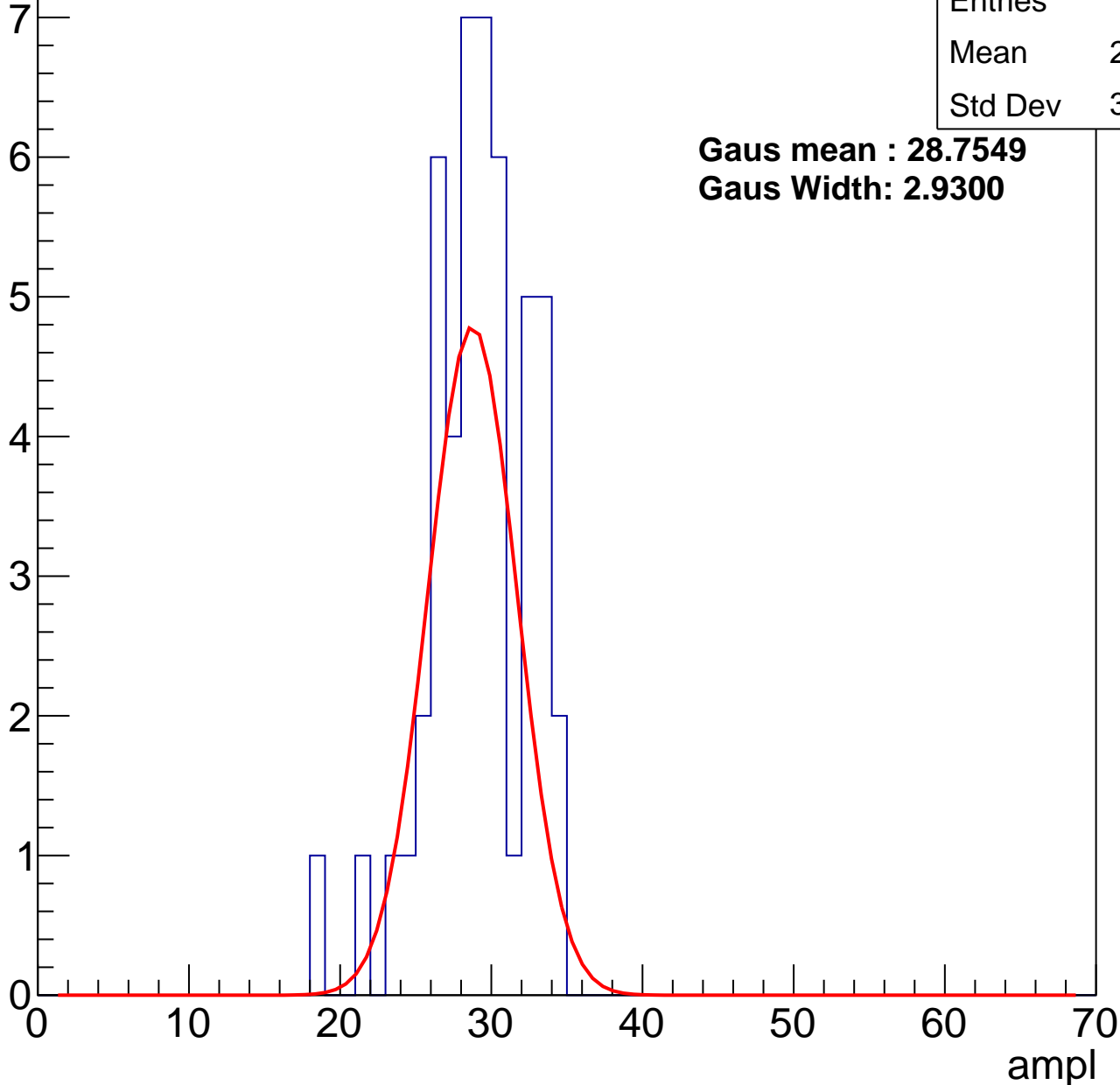
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	49
Mean	28.63
Std Dev	3.299

**Gaus mean : 28.7549**

**Gaus Width: 2.9300**



# B0L001S, U10-ch28, adc1

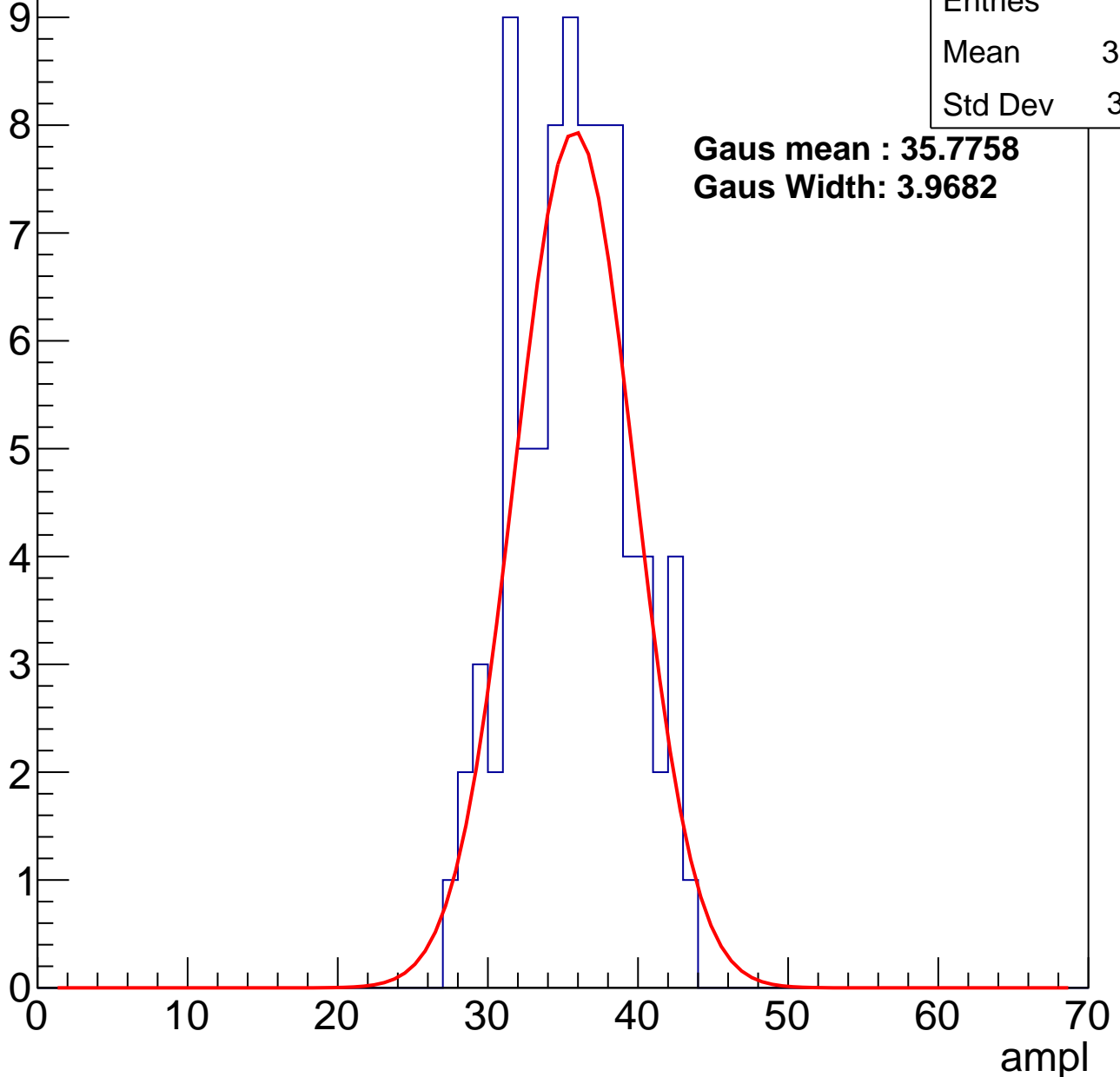
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	83
Mean	35.16
Std Dev	3.711

**Gaus mean : 35.7758**

**Gaus Width: 3.9682**



# B0L001S, U10-ch28, adc2

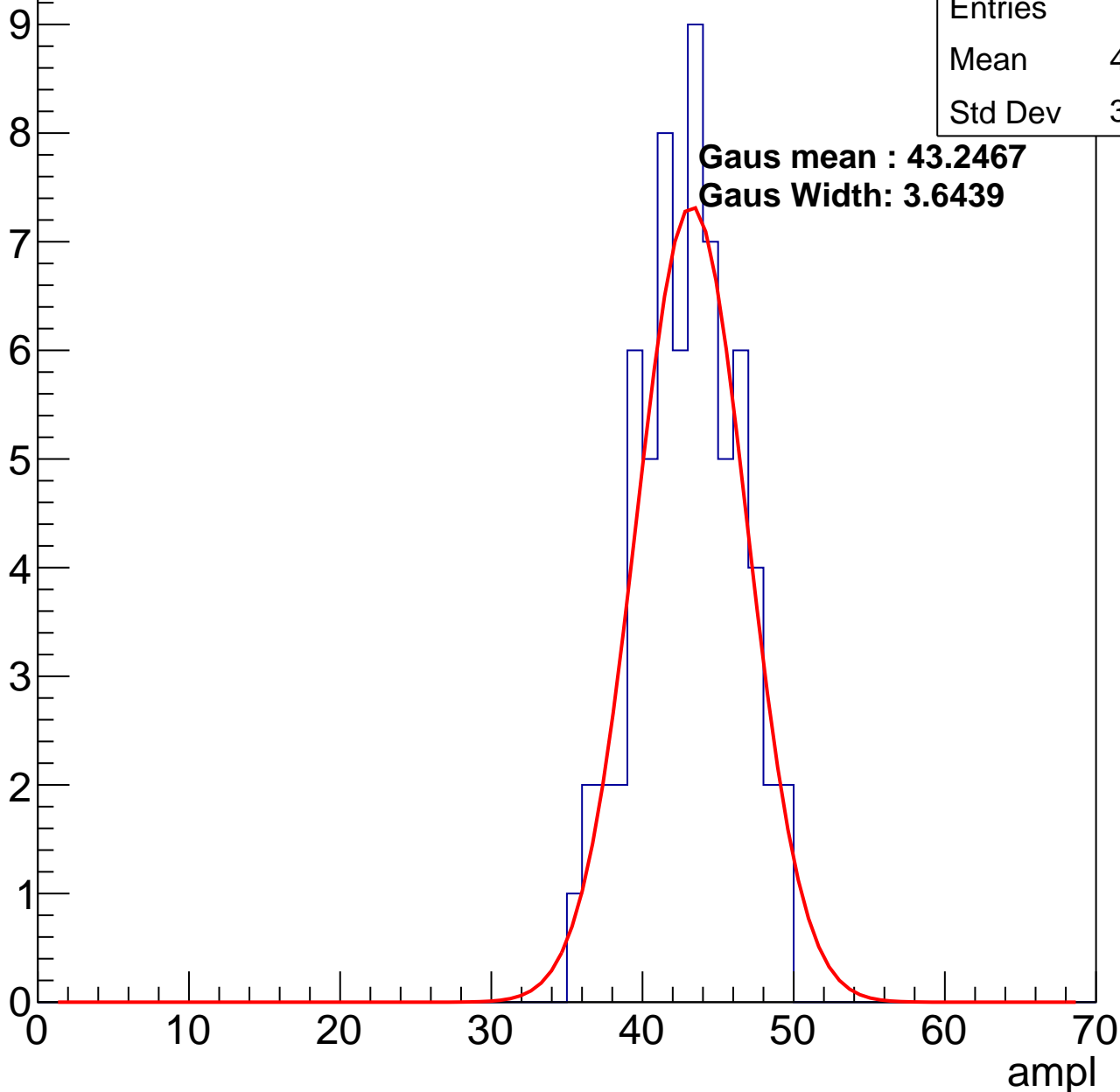
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	42.52
Std Dev	3.266

**Gaus mean : 43.2467**

**Gaus Width: 3.6439**

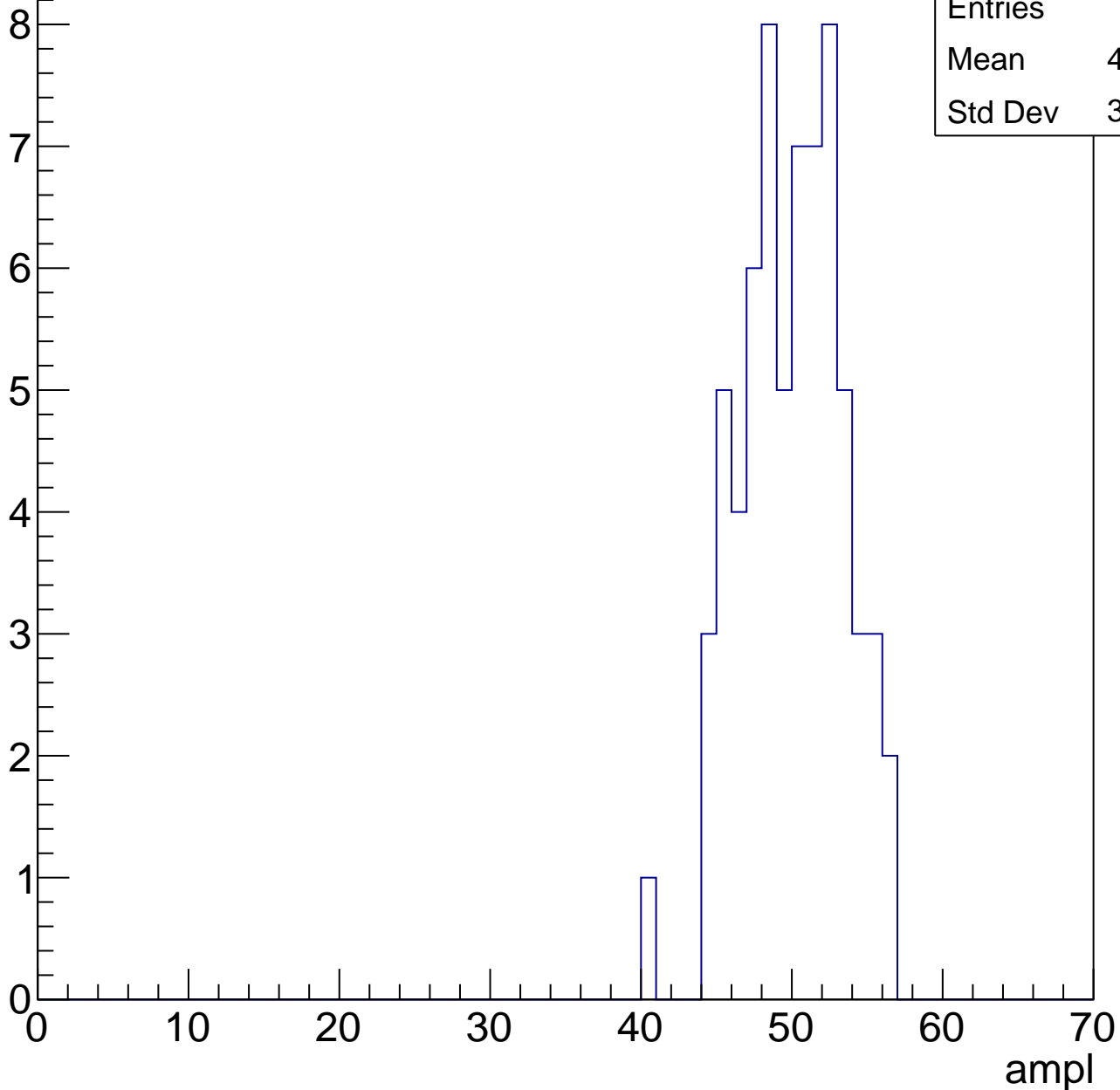


# B0L001S, U10-ch28, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

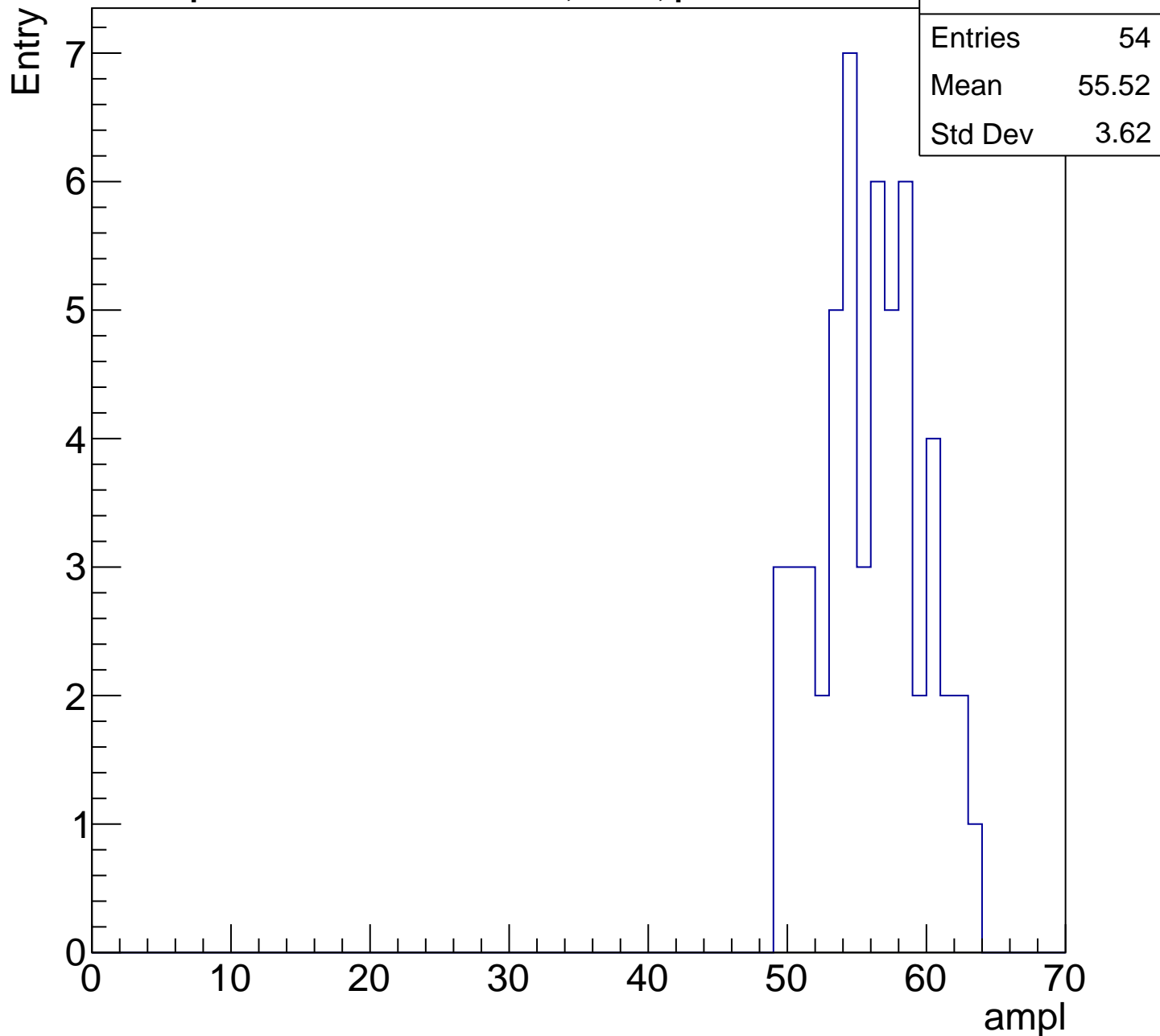
Entry

Entries	67
Mean	49.54
Std Dev	3.352



# B0L001S, U10-ch28, adc4

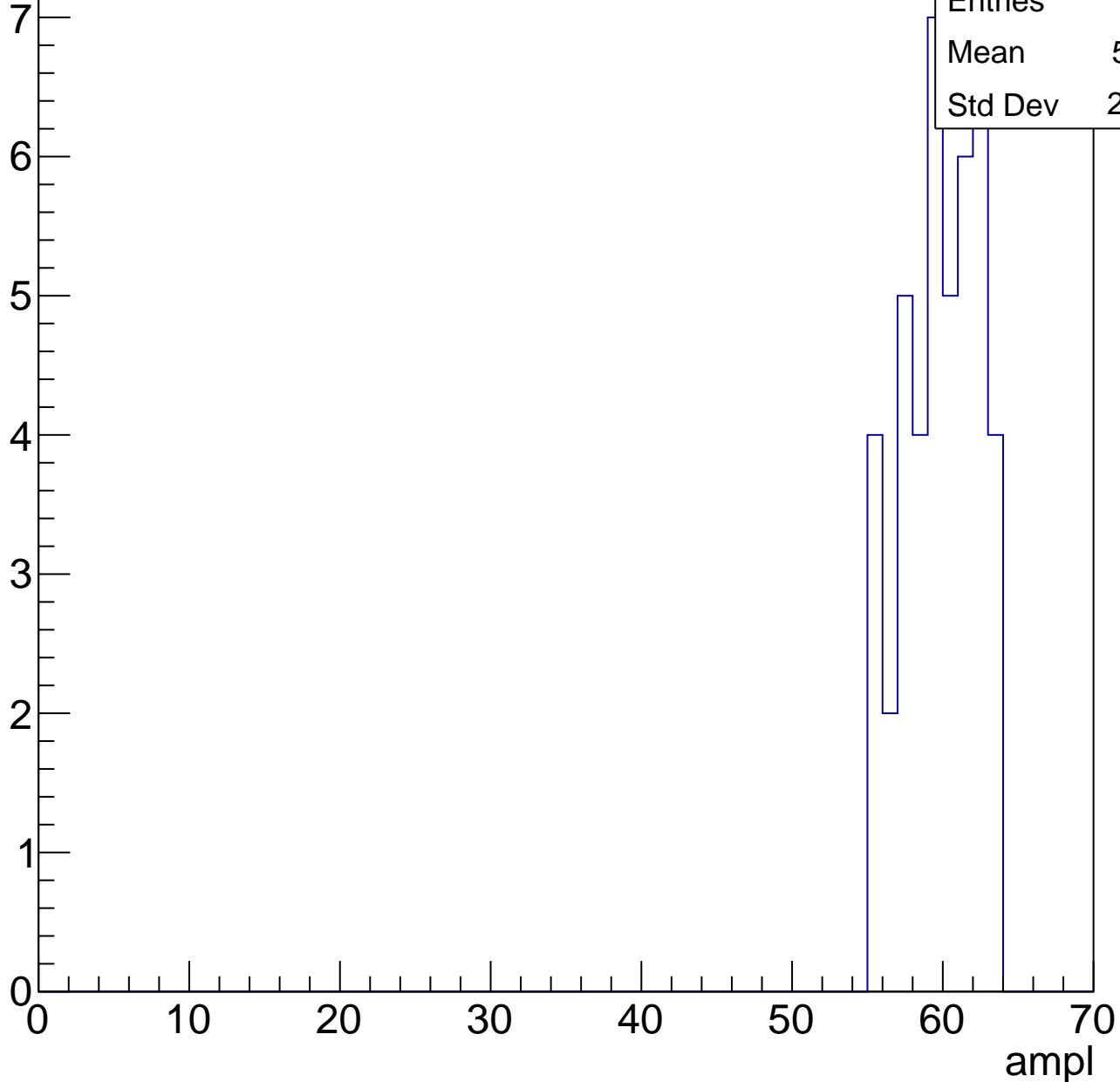
calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U10-ch28, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

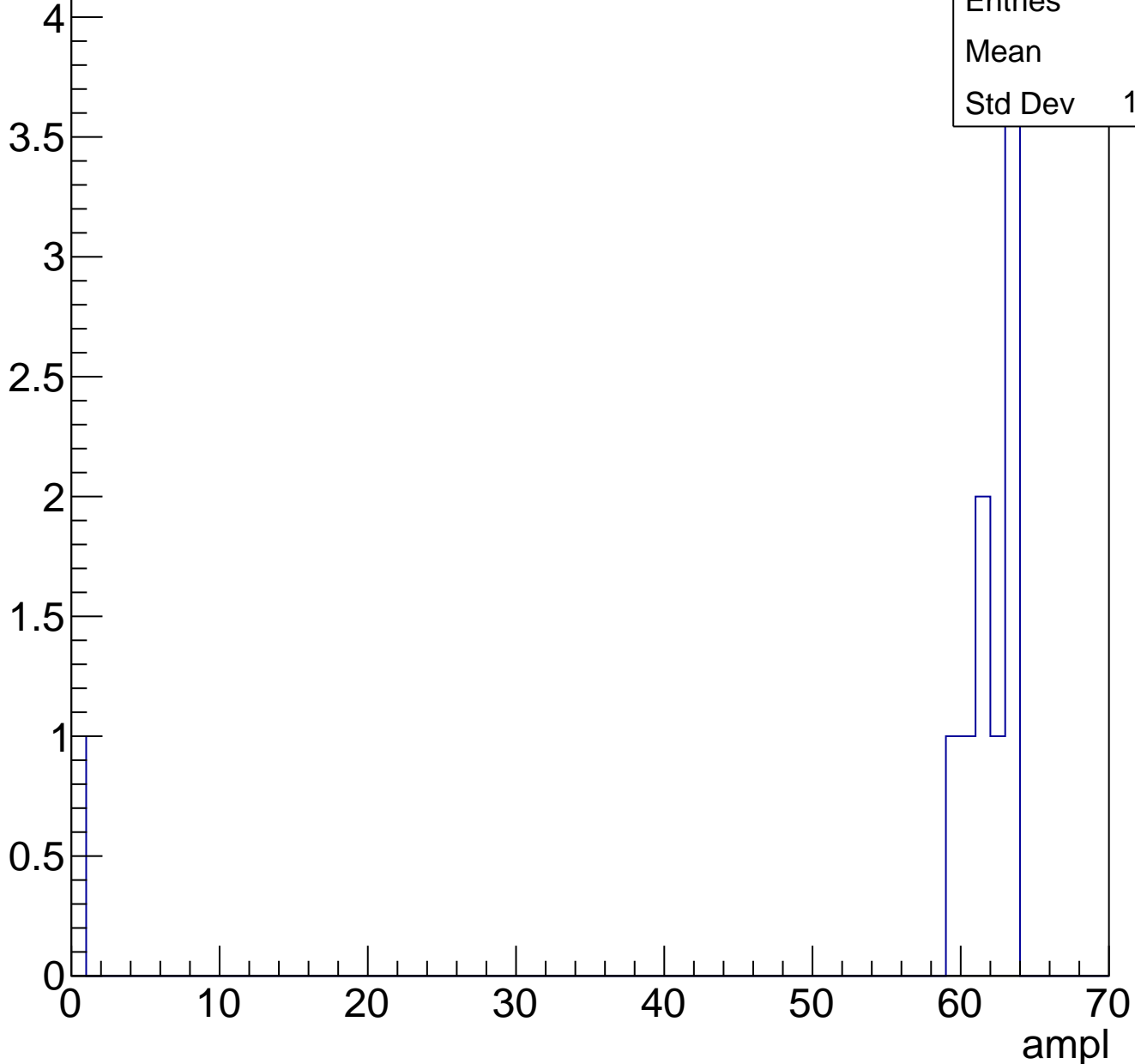
Entry



# B0L001S, U10-ch28, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	10
Mean	55.5
Std Dev	18.55



# B0L001S, U10-ch28, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U10-ch29, adc0

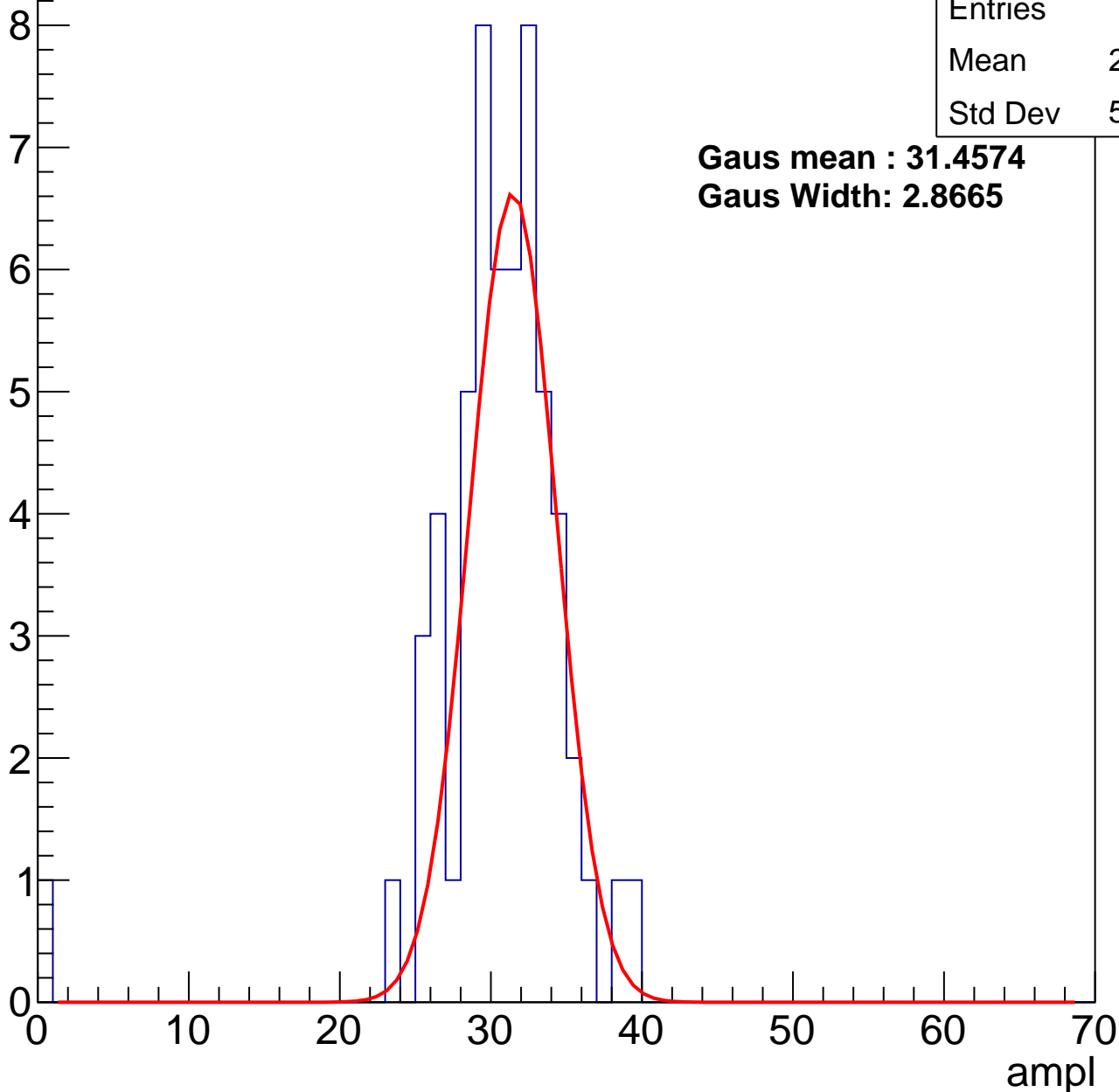
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	29.95
Std Dev	5.135

**Gaus mean : 31.4574**

**Gaus Width: 2.8665**



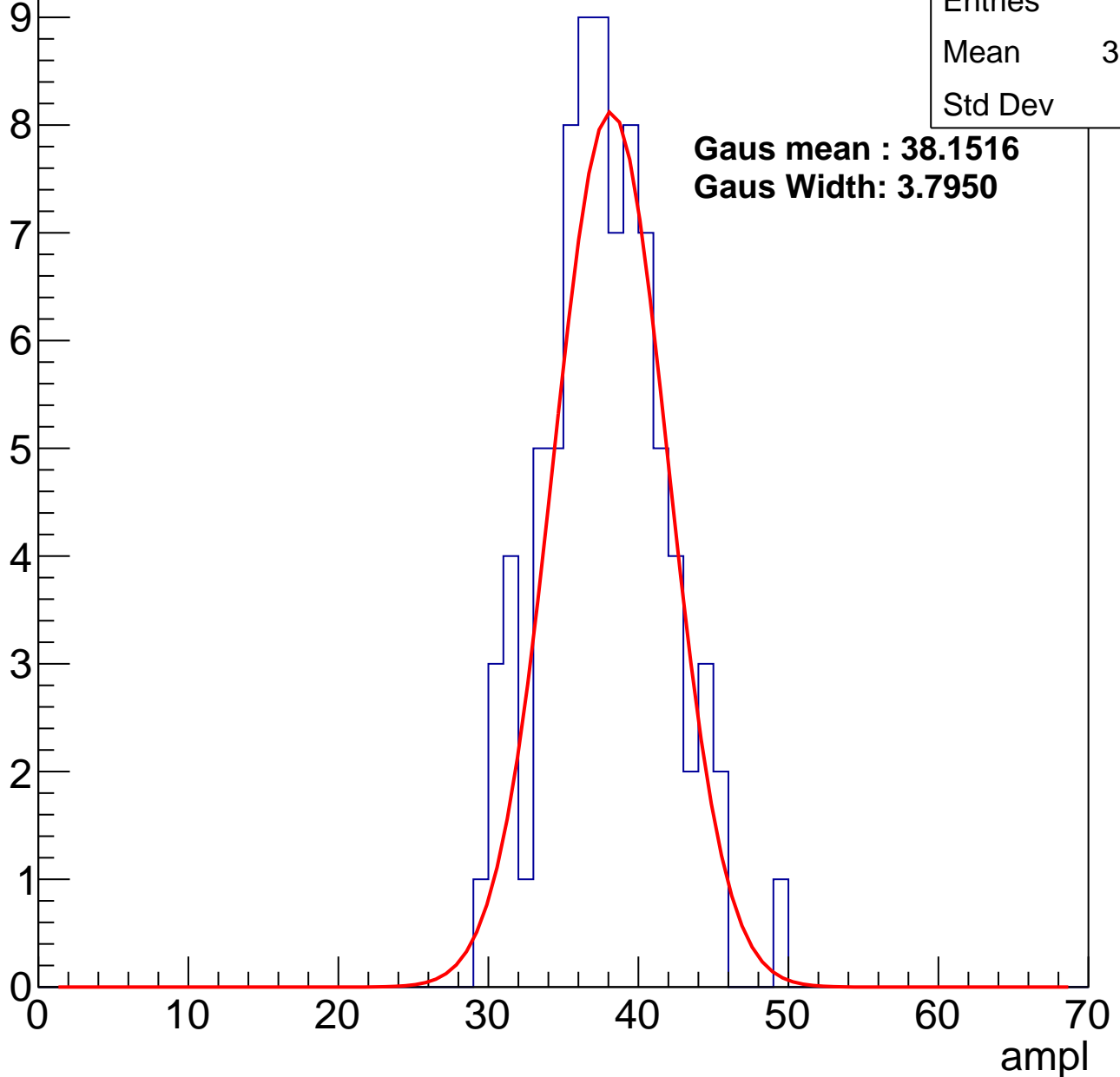
# B0L001S, U10-ch29, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	84
Mean	37.32
Std Dev	3.95

**Gaus mean : 38.1516**  
**Gaus Width: 3.7950**



# B0L001S, U10-ch29, adc2

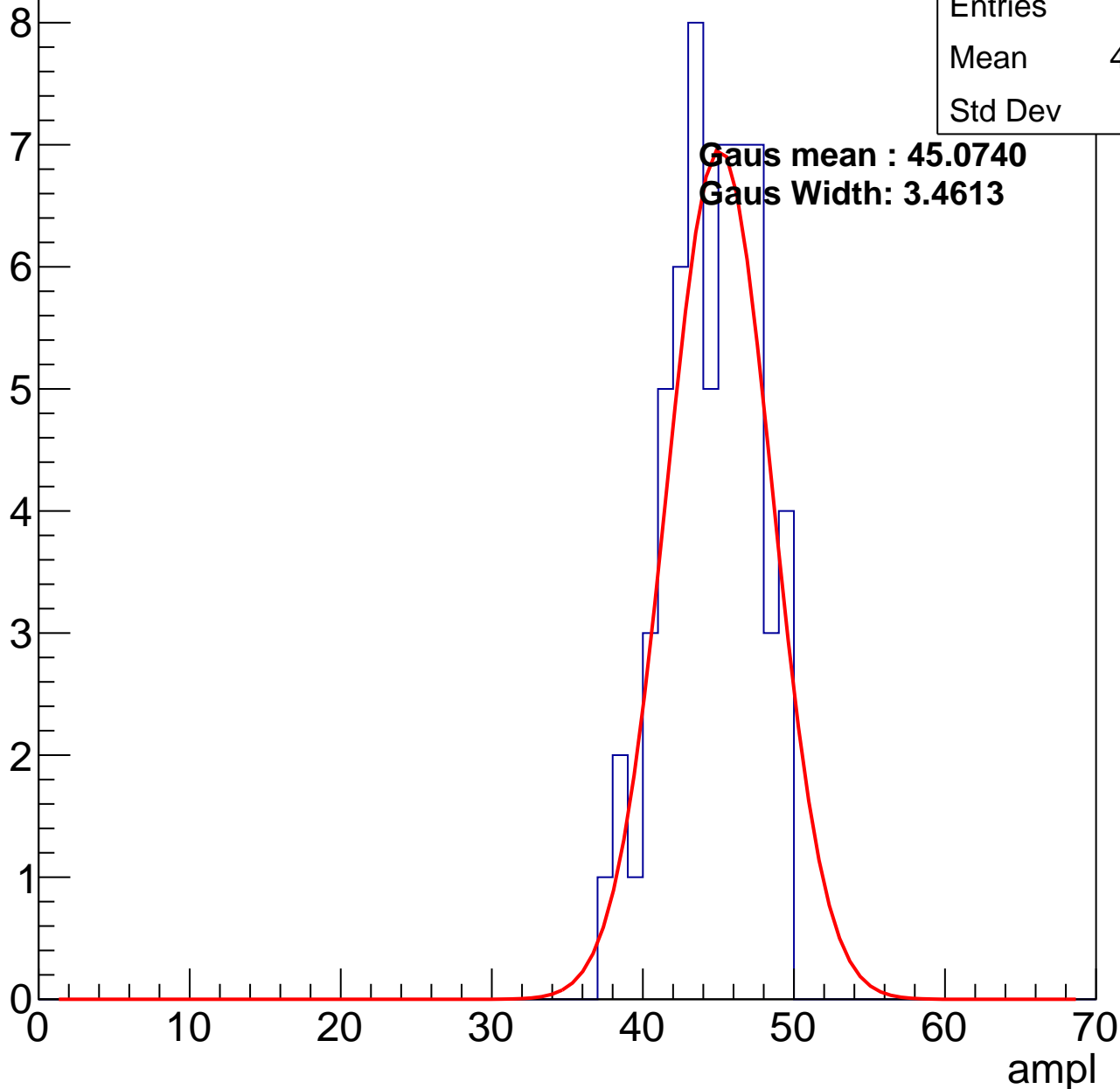
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	44.05
Std Dev	2.96

**Gaus mean : 45.0740**

**Gaus Width: 3.4613**

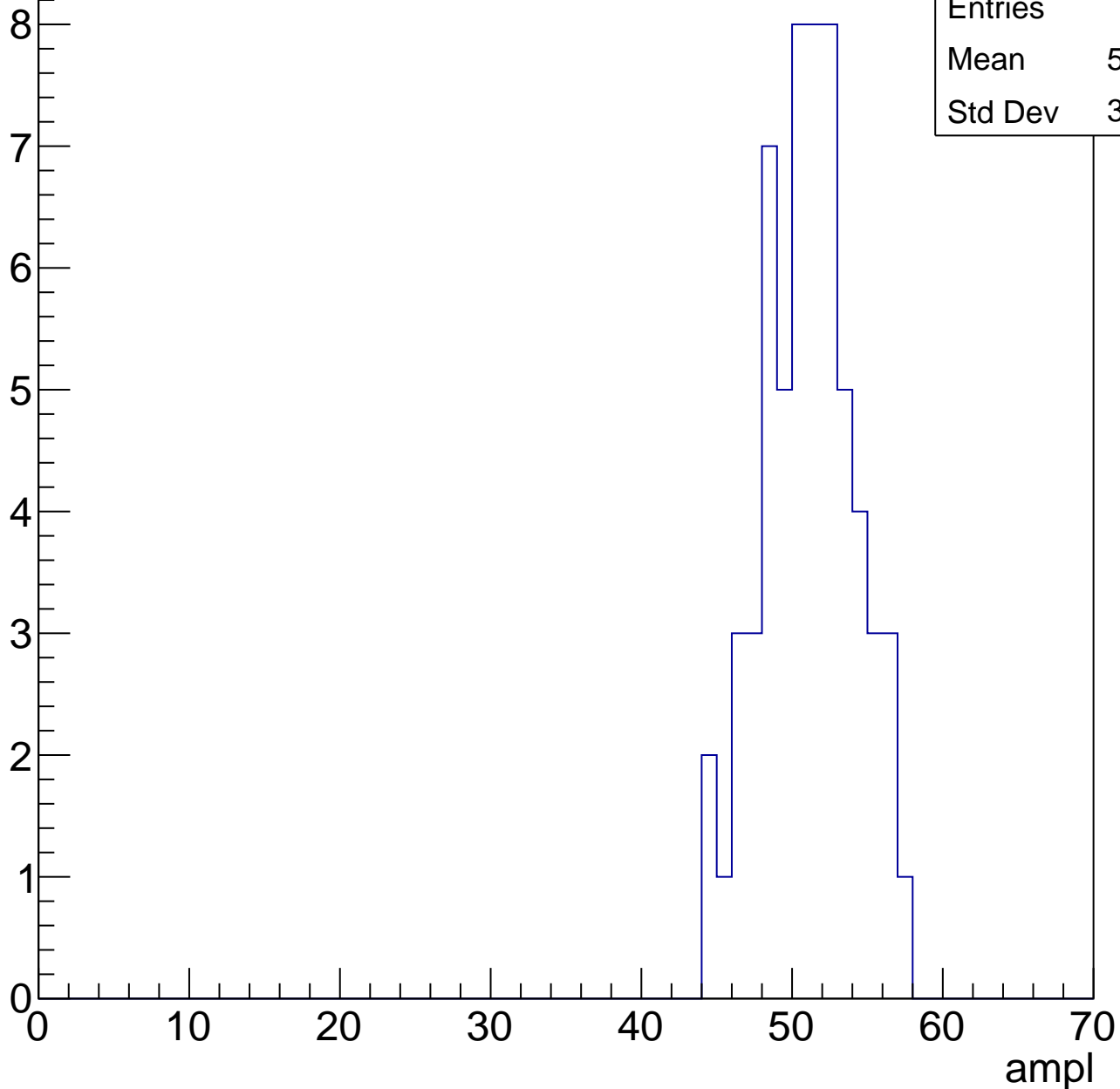


# B0L001S, U10-ch29, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

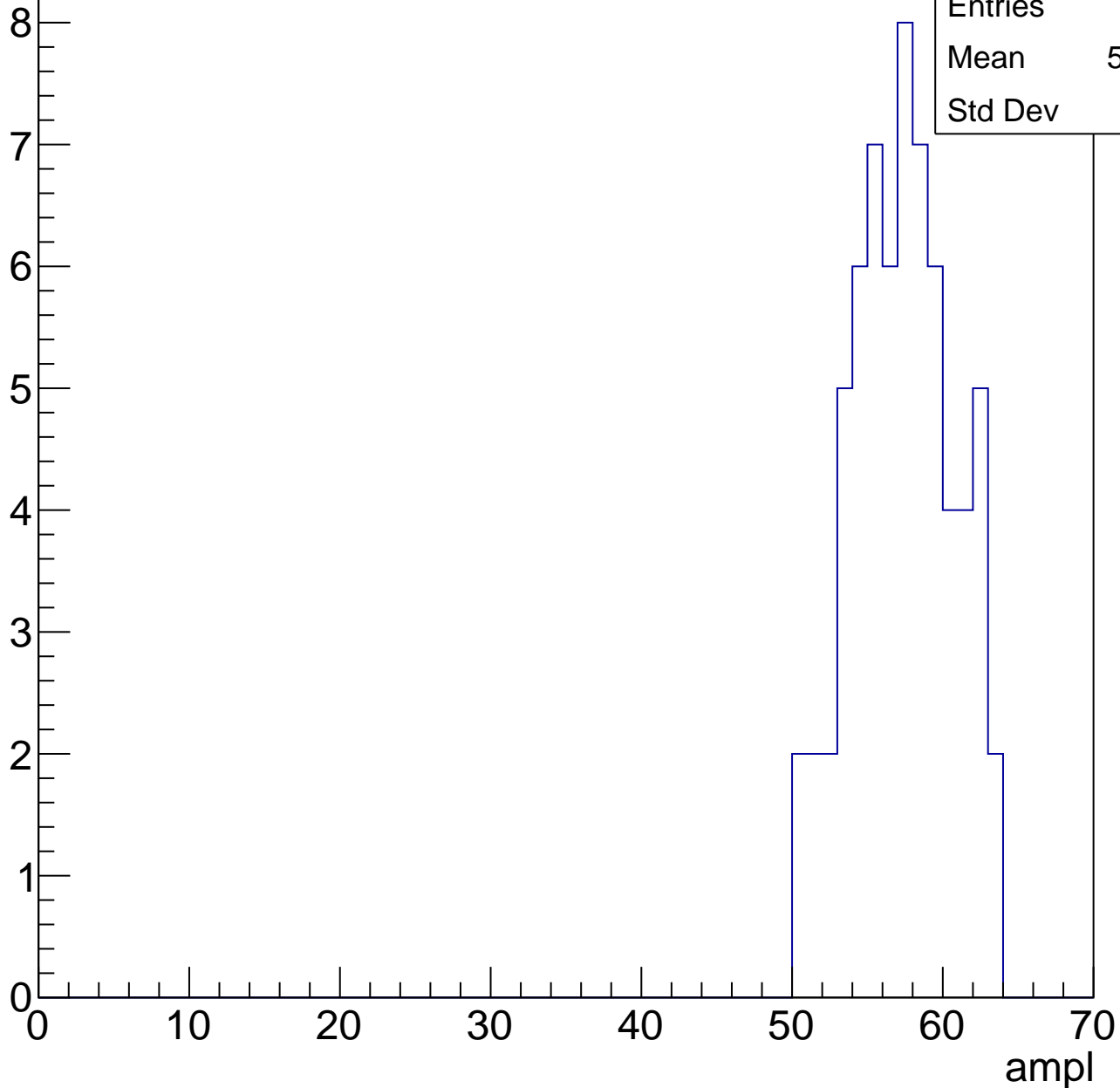
Entries	61
Mean	50.62
Std Dev	3.036



# B0L001S, U10-ch29, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

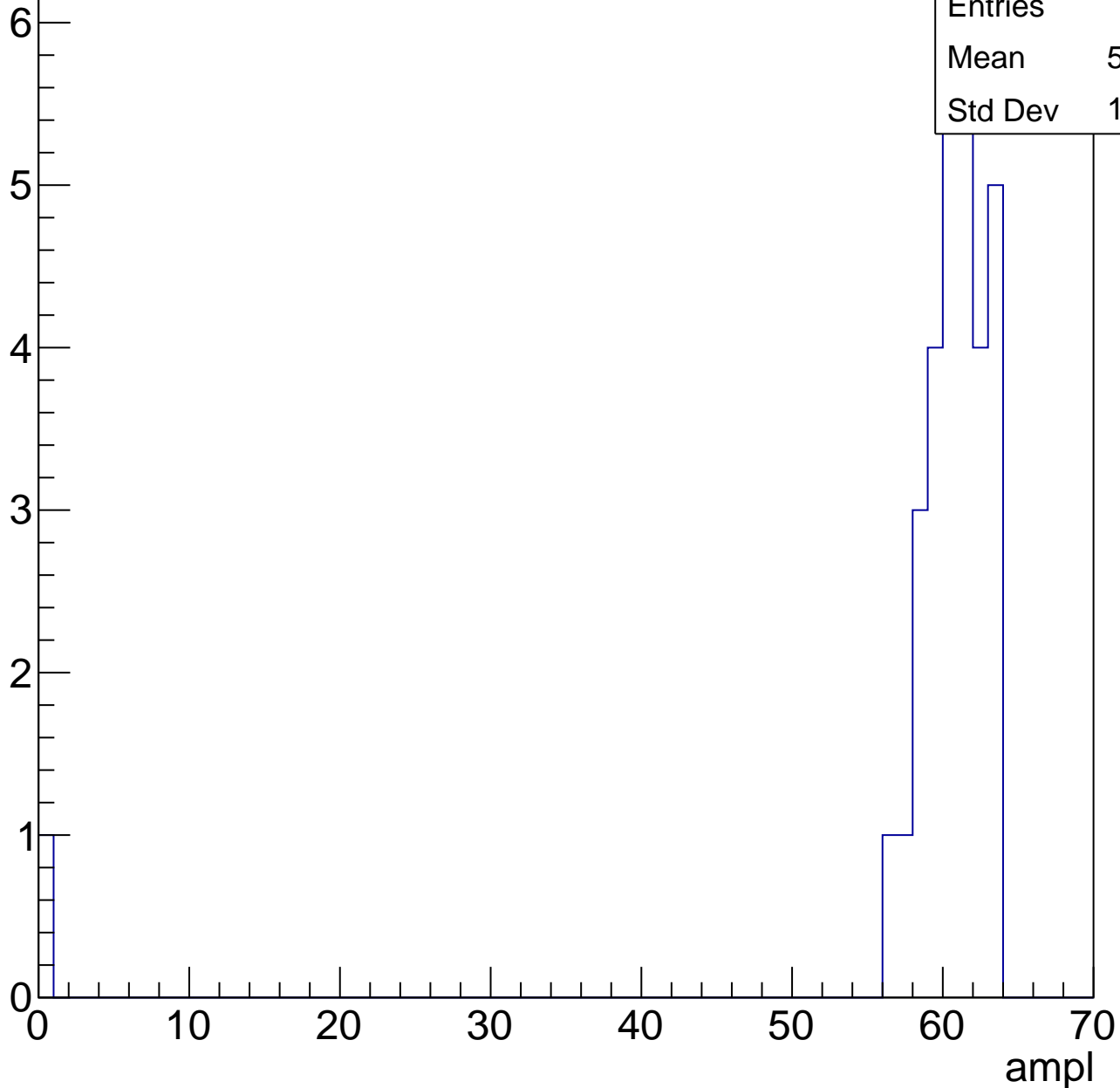
Entry



# B0L001S, U10-ch29, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U10-ch29, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch29, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	3
Mean	7
Std Dev	9.899

# B0L001S, U10-ch30, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	81
Mean	31.6
Std Dev	6.154

**Gaus mean : 32.6458**

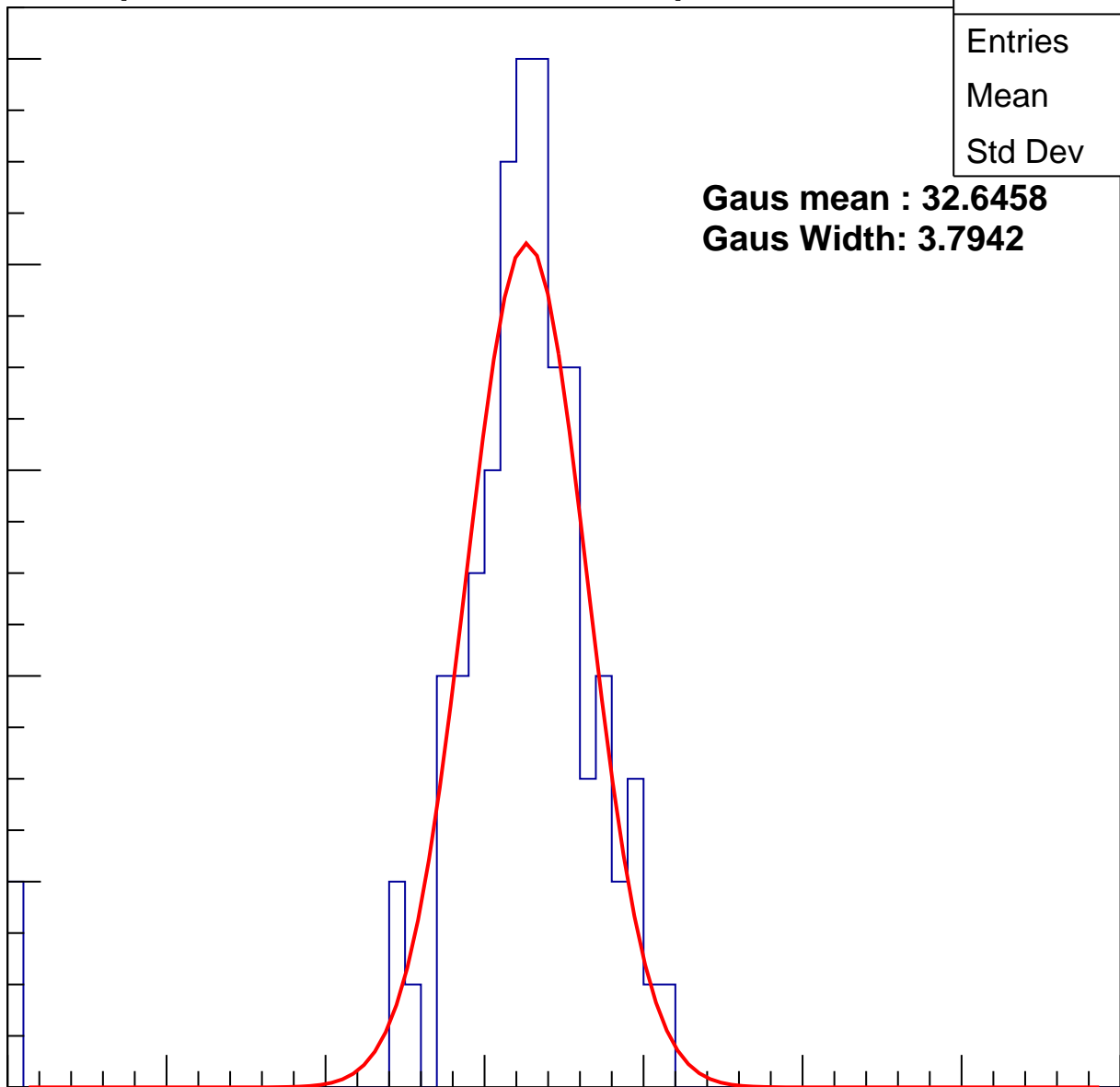
**Gaus Width: 3.7942**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U10-ch30, adc1

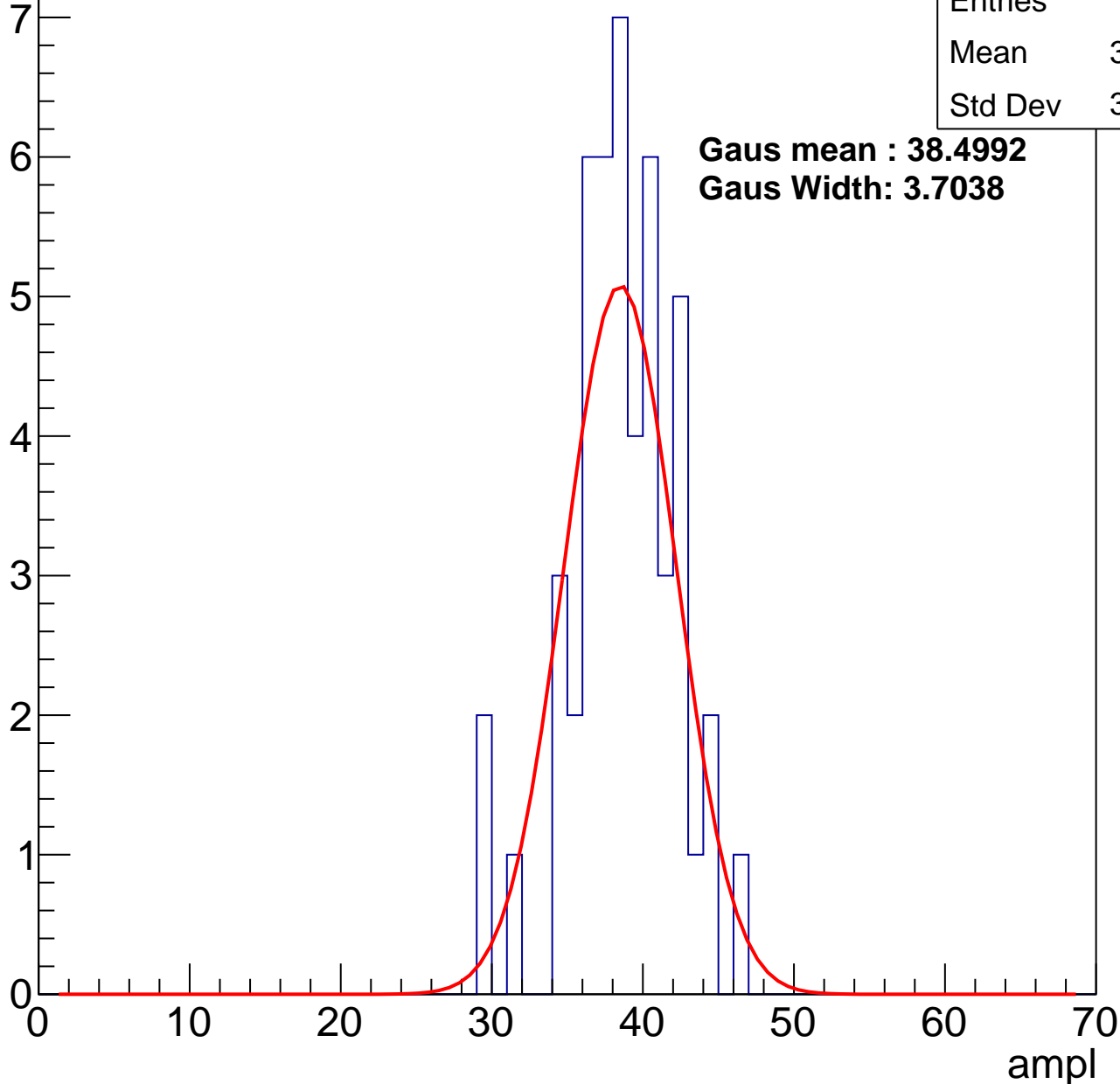
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	49
Mean	38.18
Std Dev	3.503

**Gaus mean : 38.4992**

**Gaus Width: 3.7038**



# B0L001S, U10-ch30, adc2

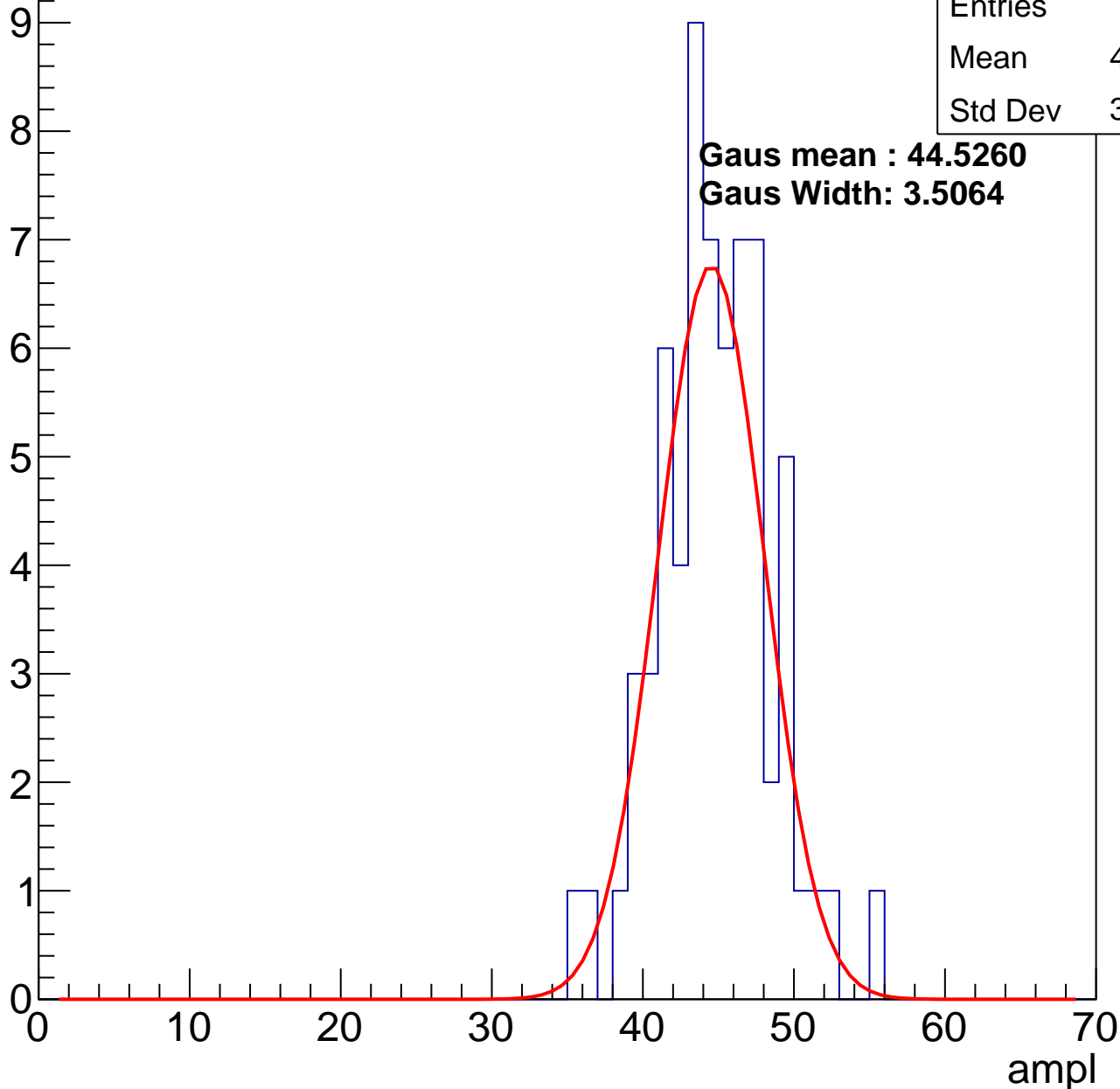
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	44.32
Std Dev	3.693

**Gaus mean : 44.5260**

**Gaus Width: 3.5064**

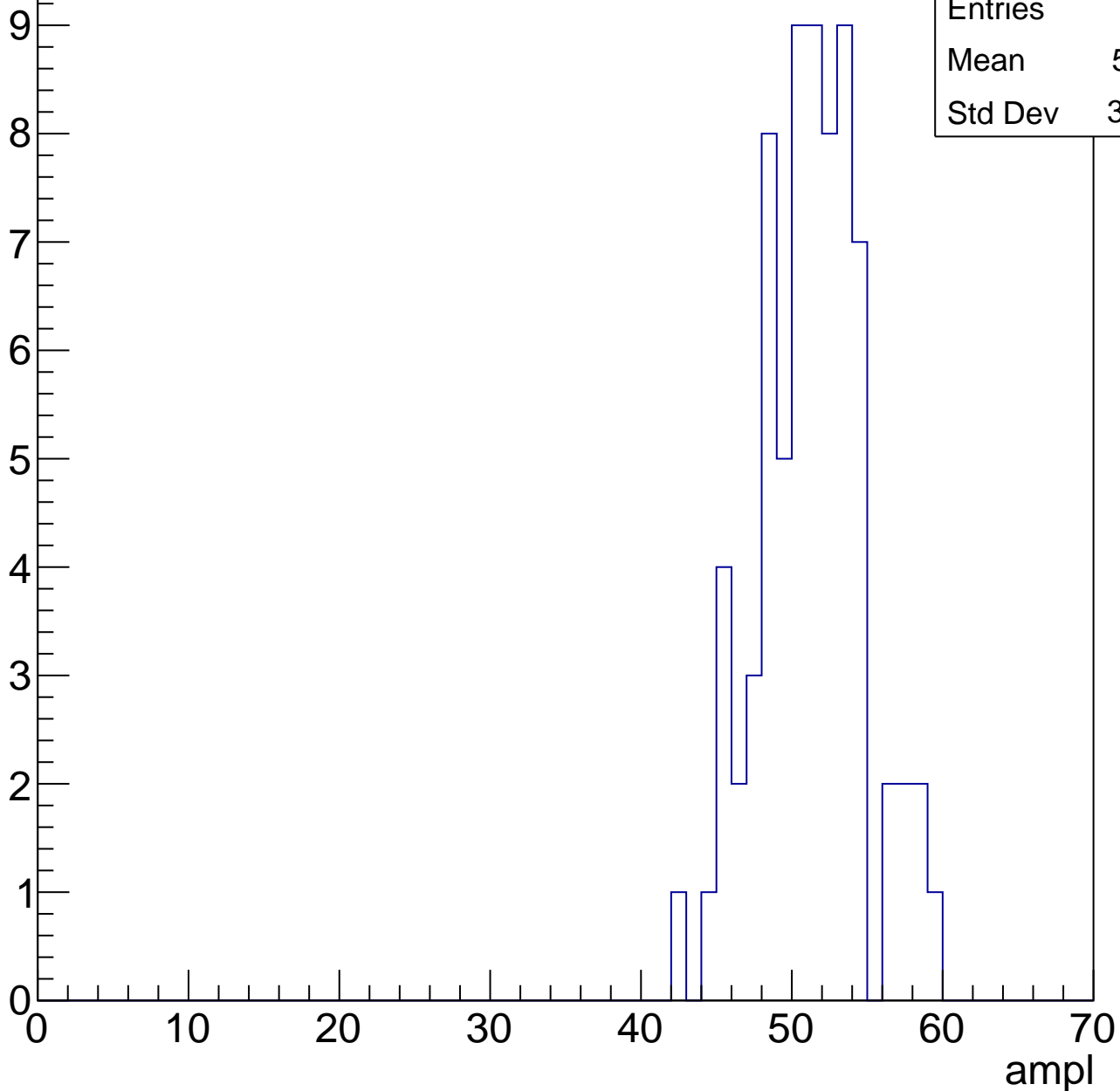


# B0L001S, U10-ch30, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	50.81
Std Dev	3.435

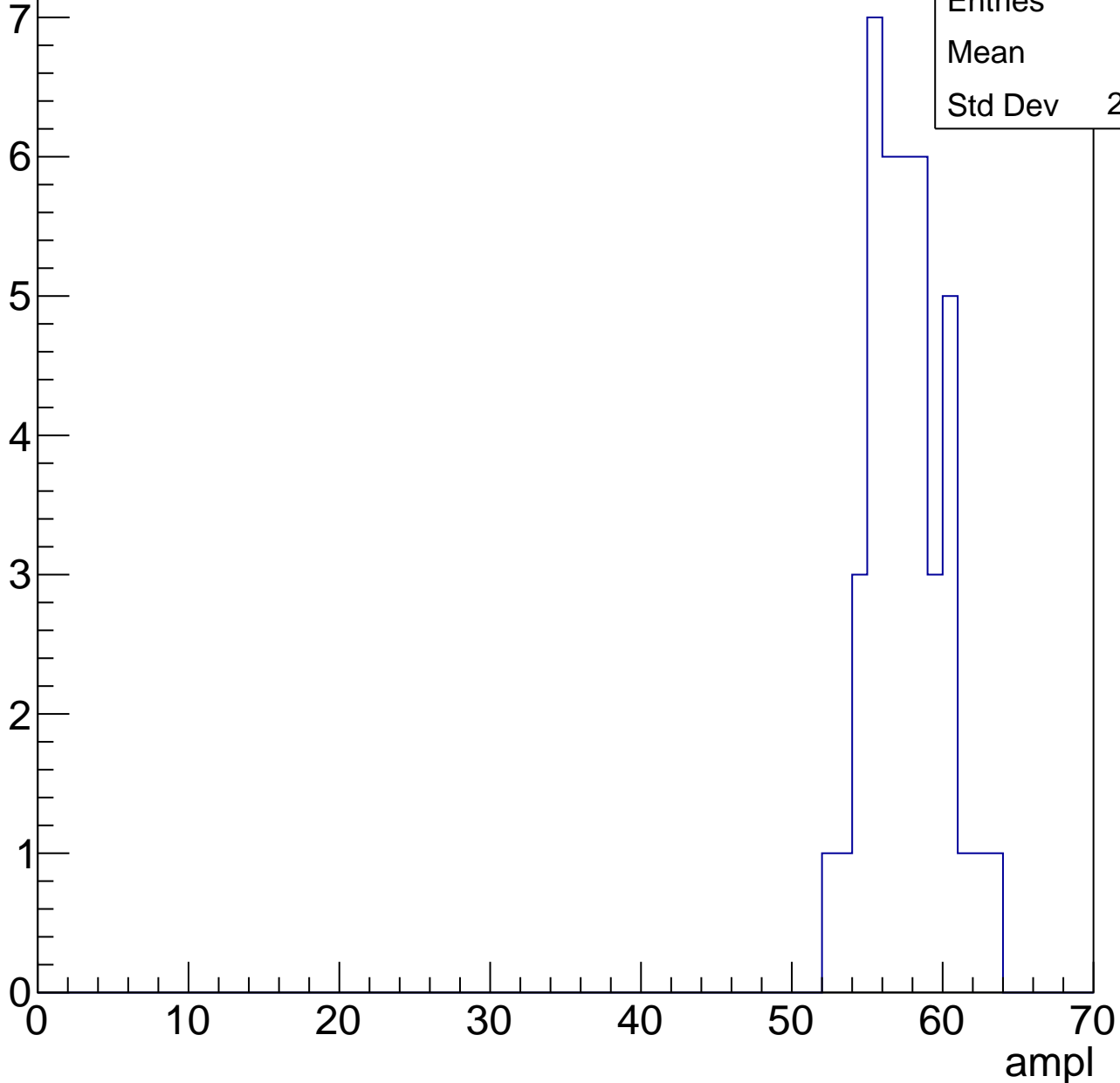


# B0L001S, U10-ch30, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

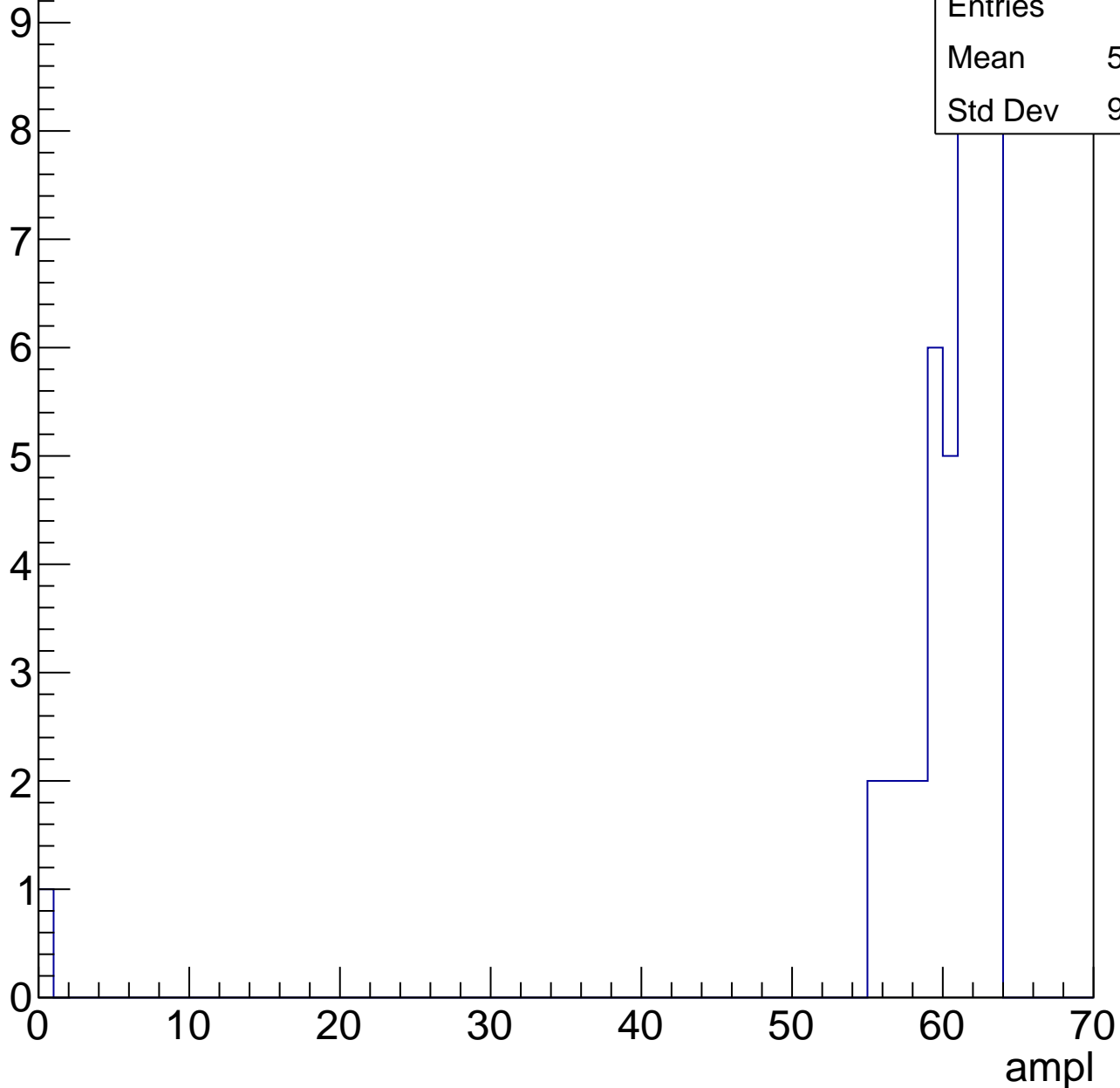
Entries	41
Mean	57.1
Std Dev	2.428



# B0L001S, U10-ch30, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U10-ch30, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch30, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	11
Std Dev	11

# B0L001S, U10-ch31, adc0

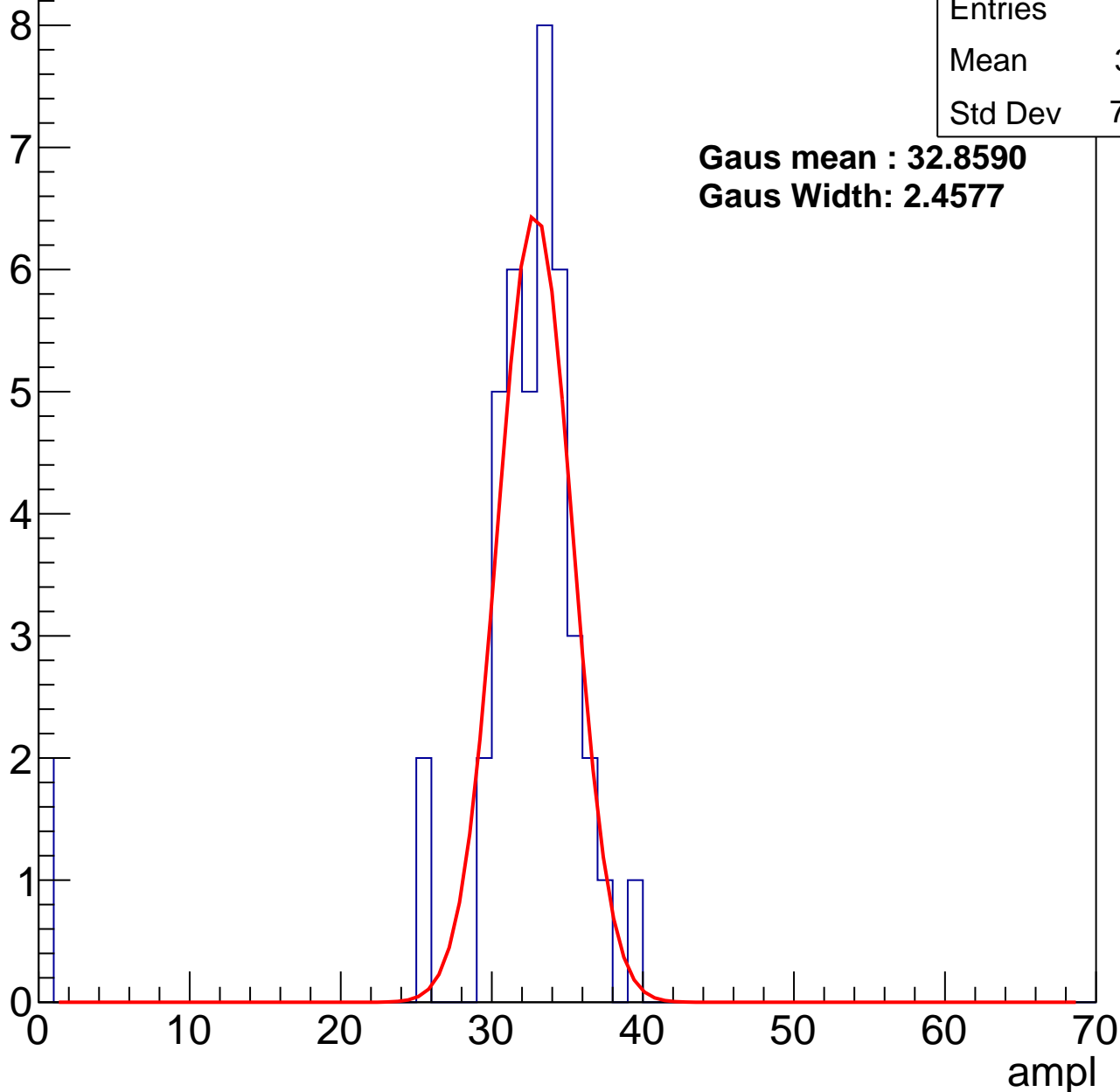
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	43
Mean	30.81
Std Dev	7.305

**Gaus mean : 32.8590**

**Gaus Width: 2.4577**



# B0L001S, U10-ch31, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	78
Mean	38.87
Std Dev	3.176

**Gaus mean : 38.6730**

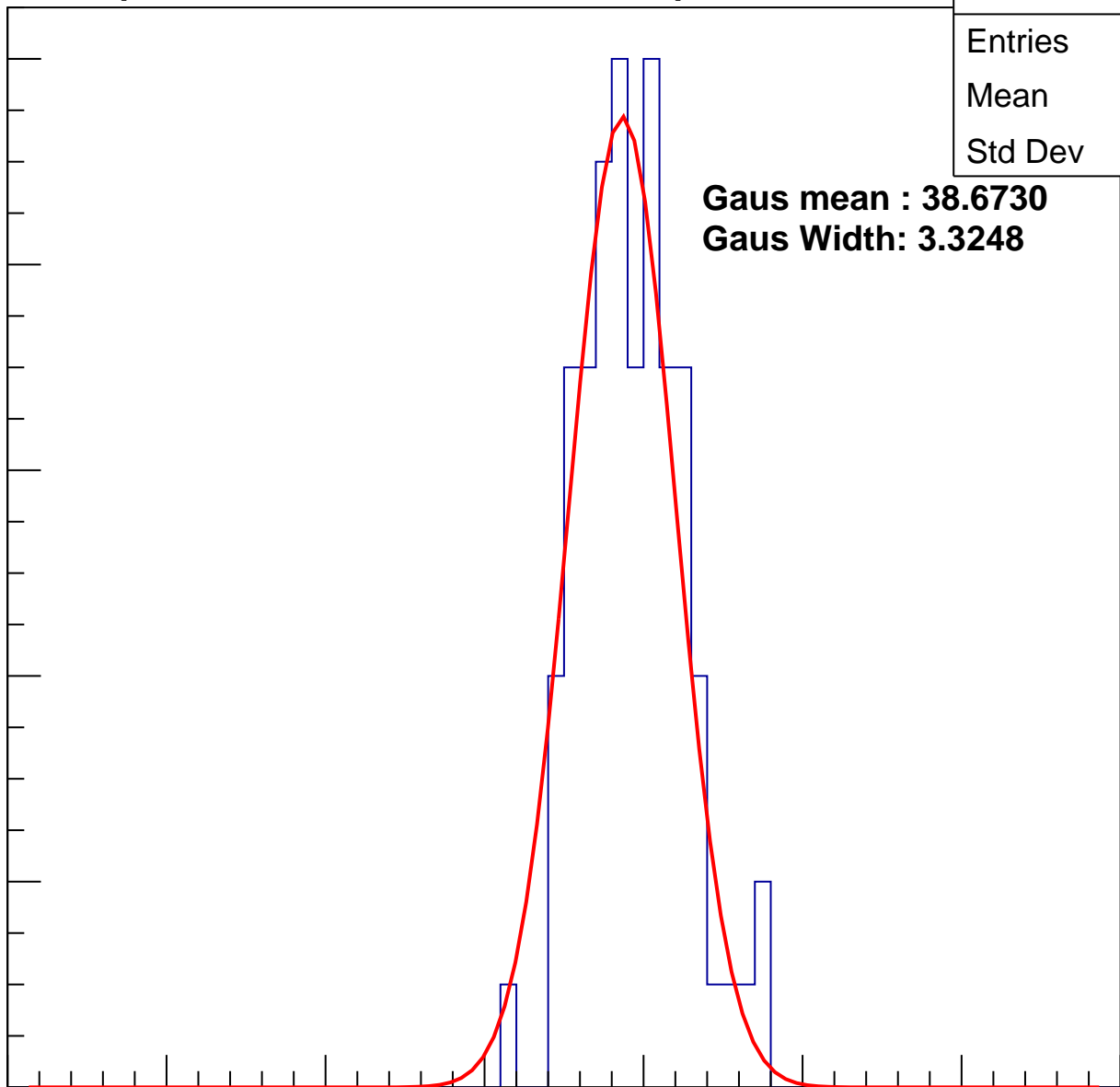
**Gaus Width: 3.3248**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B0L001S, U10-ch31, adc2

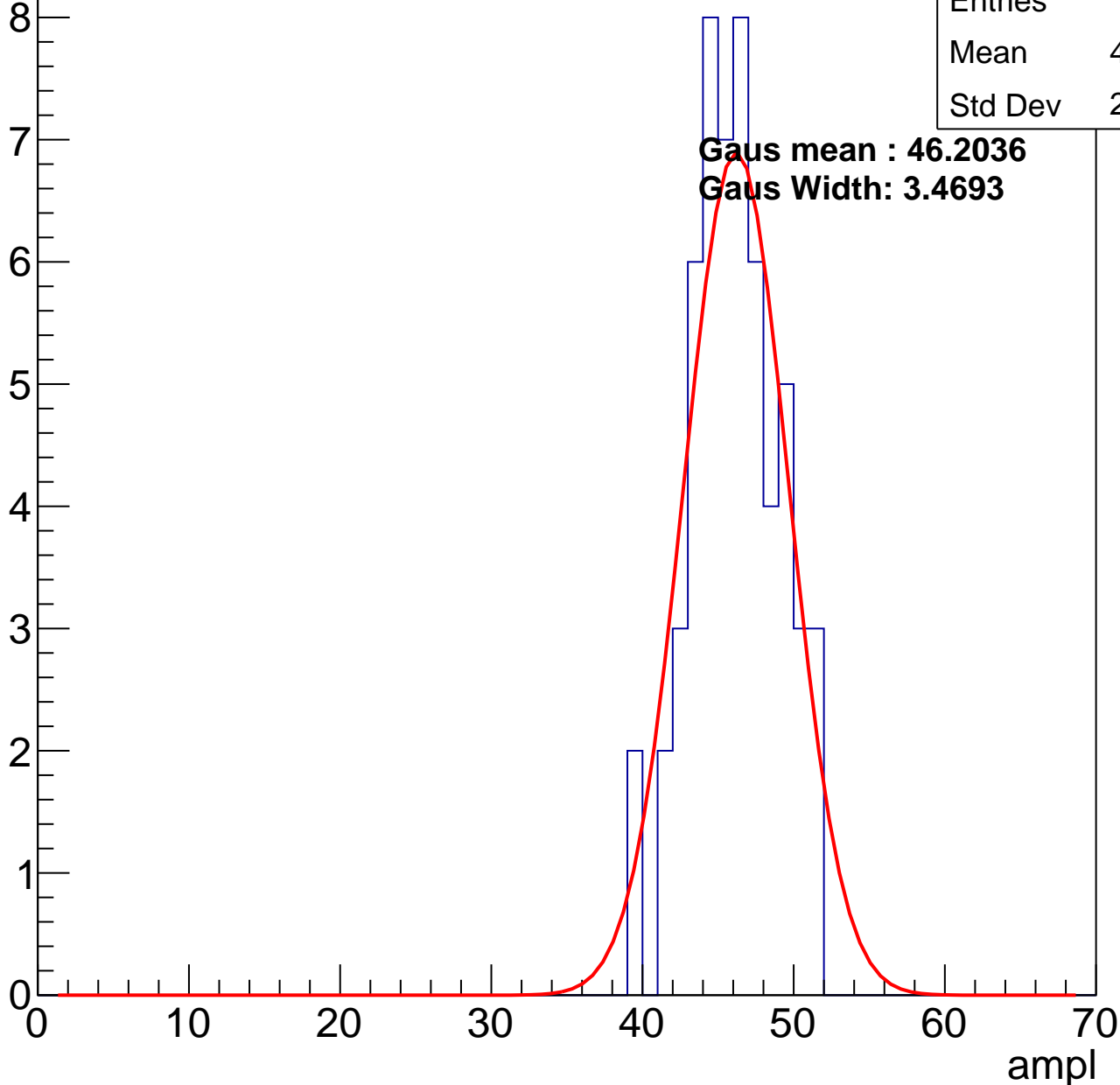
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	45.63
Std Dev	2.875

**Gaus mean : 46.2036**

**Gaus Width: 3.4693**

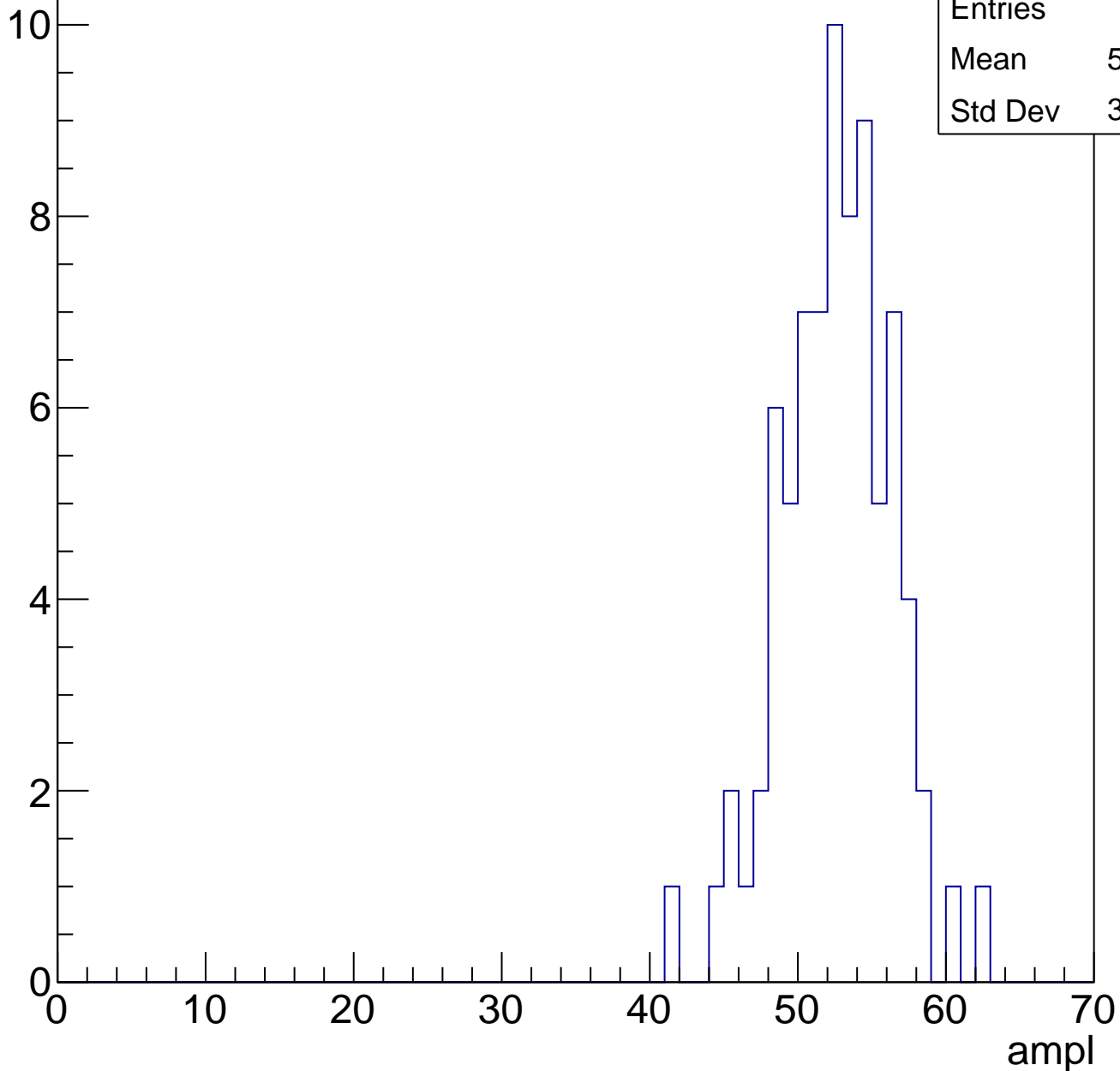


# B0L001S, U10-ch31, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	79
Mean	52.13
Std Dev	3.699

Entry

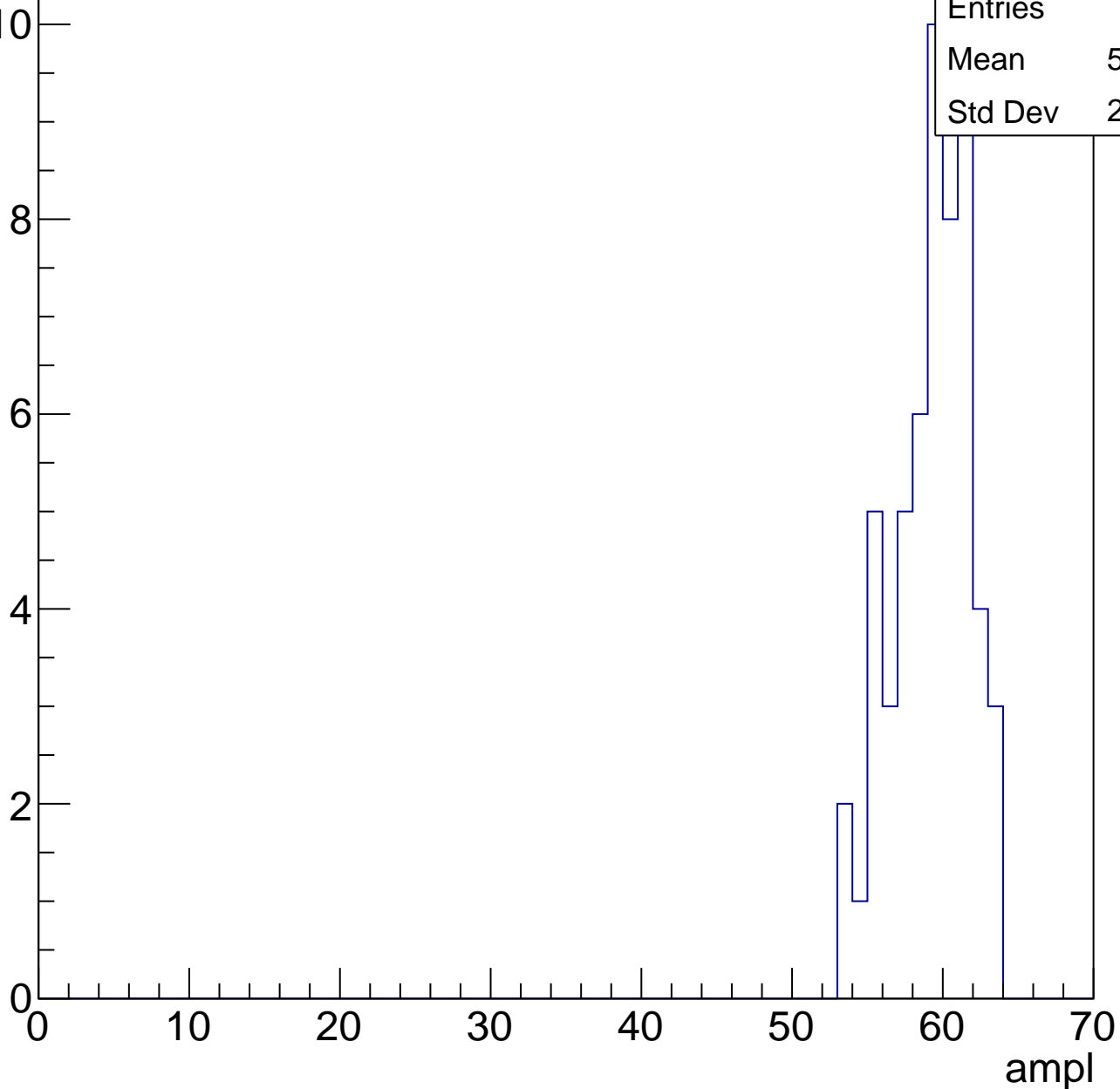


# B0L001S, U10-ch31, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	58.79
Std Dev	2.519

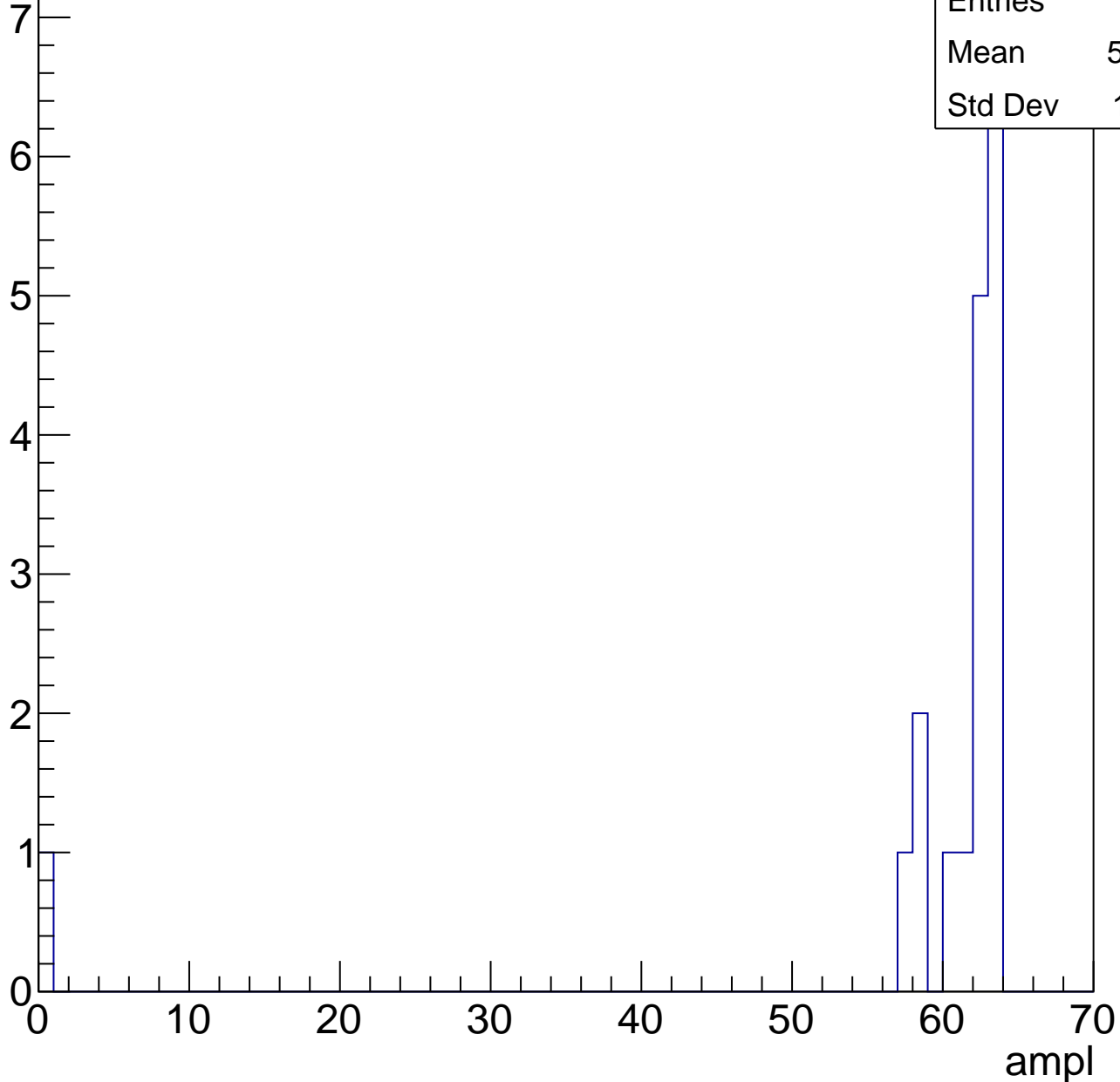


# B0L001S, U10-ch31, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	18
Mean	58.06
Std Dev	14.21



# B0L001S, U10-ch31, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch31, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

0

Mean

0

Std Dev

0

# B0L001S, U10-ch32, adc0

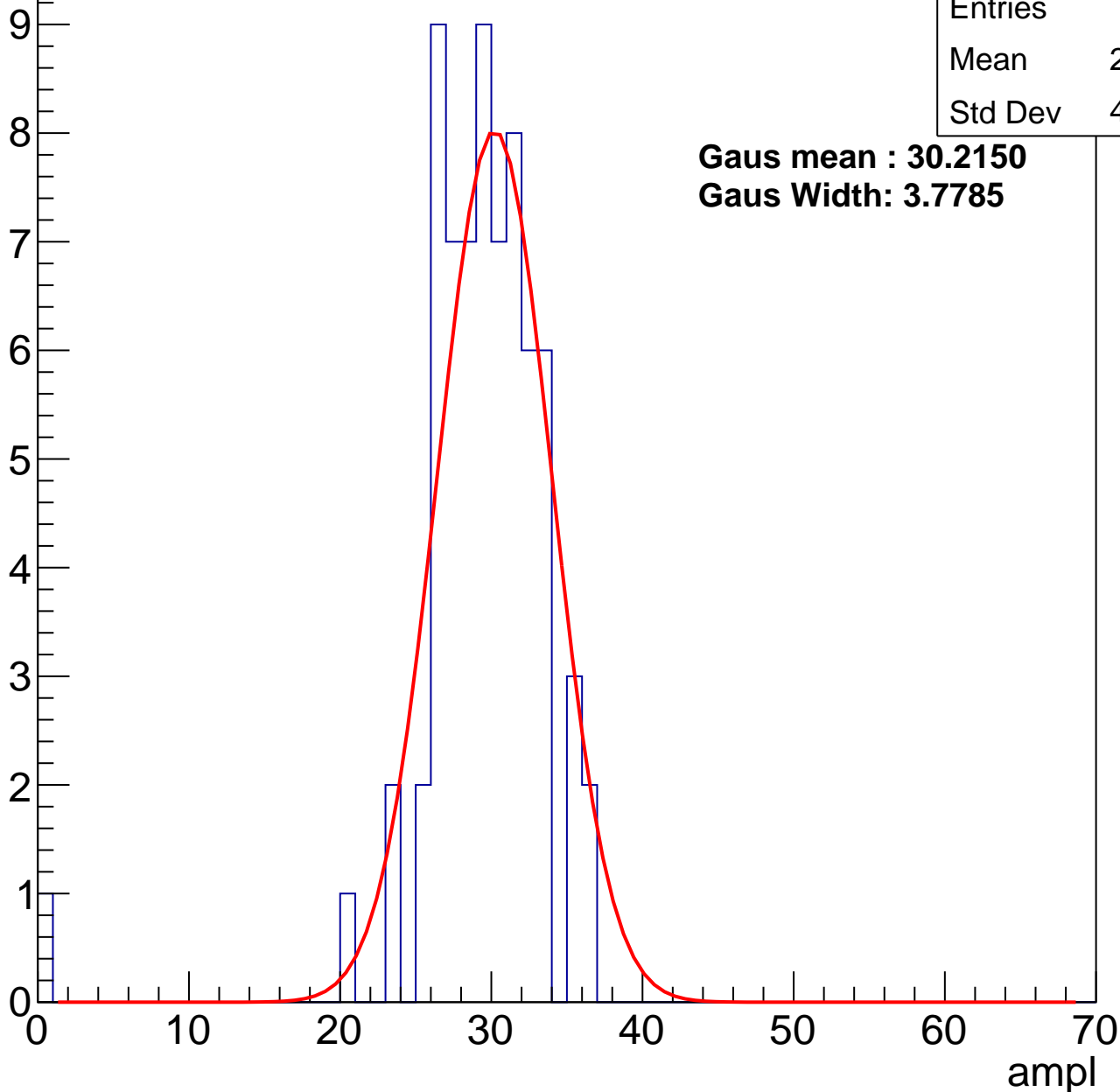
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	28.87
Std Dev	4.684

**Gaus mean : 30.2150**

**Gaus Width: 3.7785**

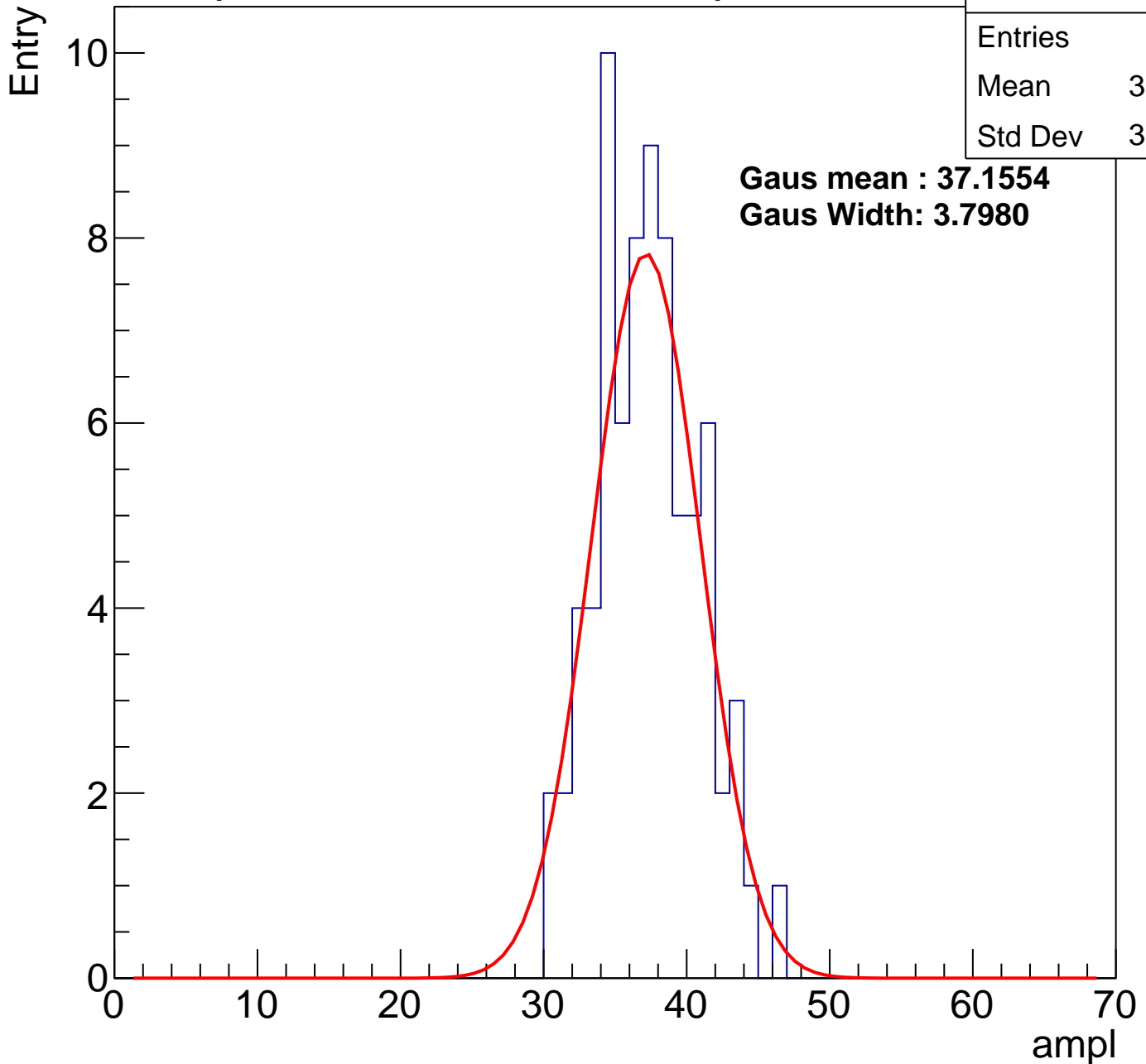


# B0L001S, U10-ch32, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	76
Mean	36.86
Std Dev	3.463

**Gaus mean : 37.1554**  
**Gaus Width: 3.7980**



# B0L001S, U10-ch32, adc2

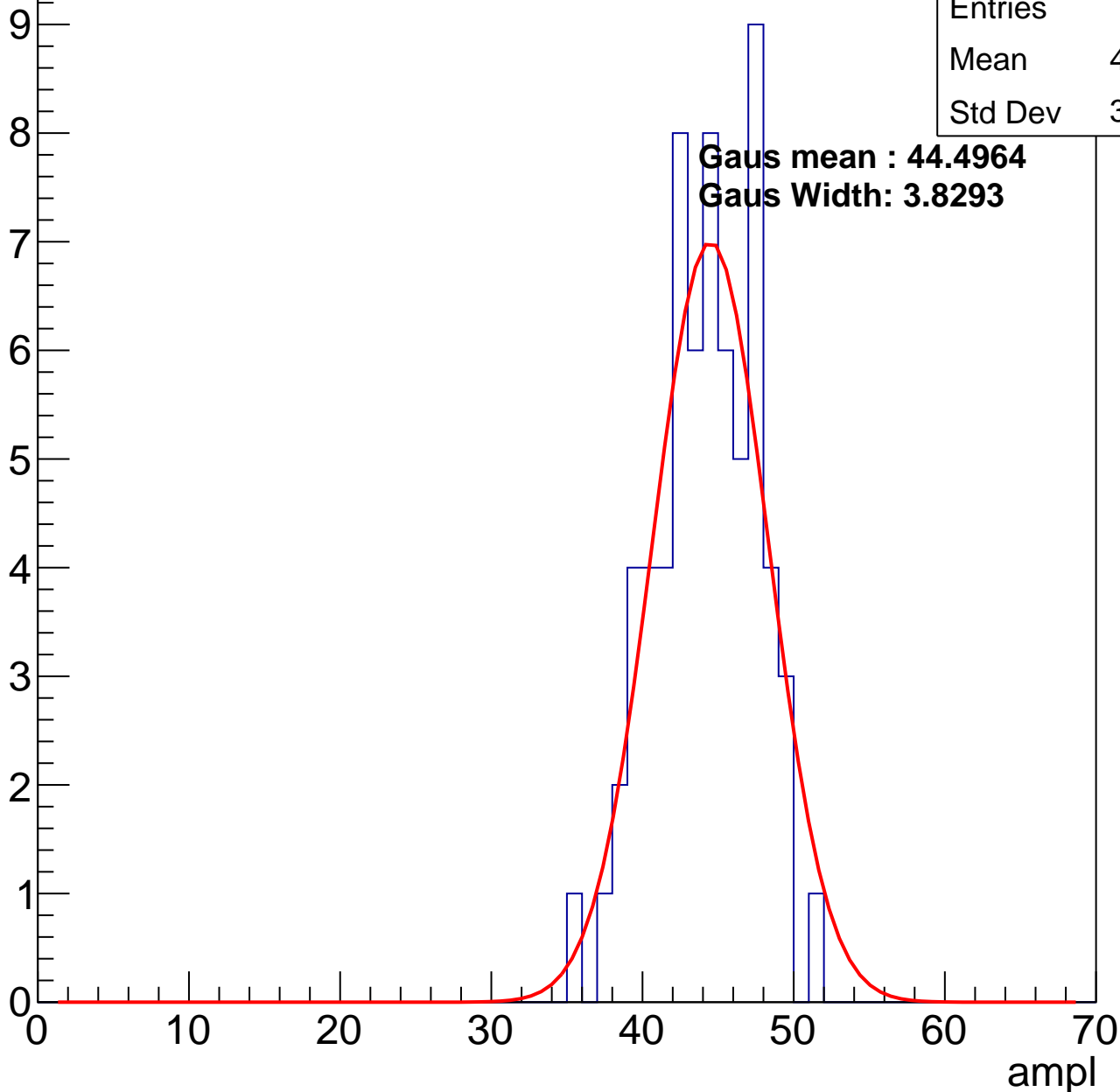
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	43.74
Std Dev	3.327

**Gaus mean : 44.4964**

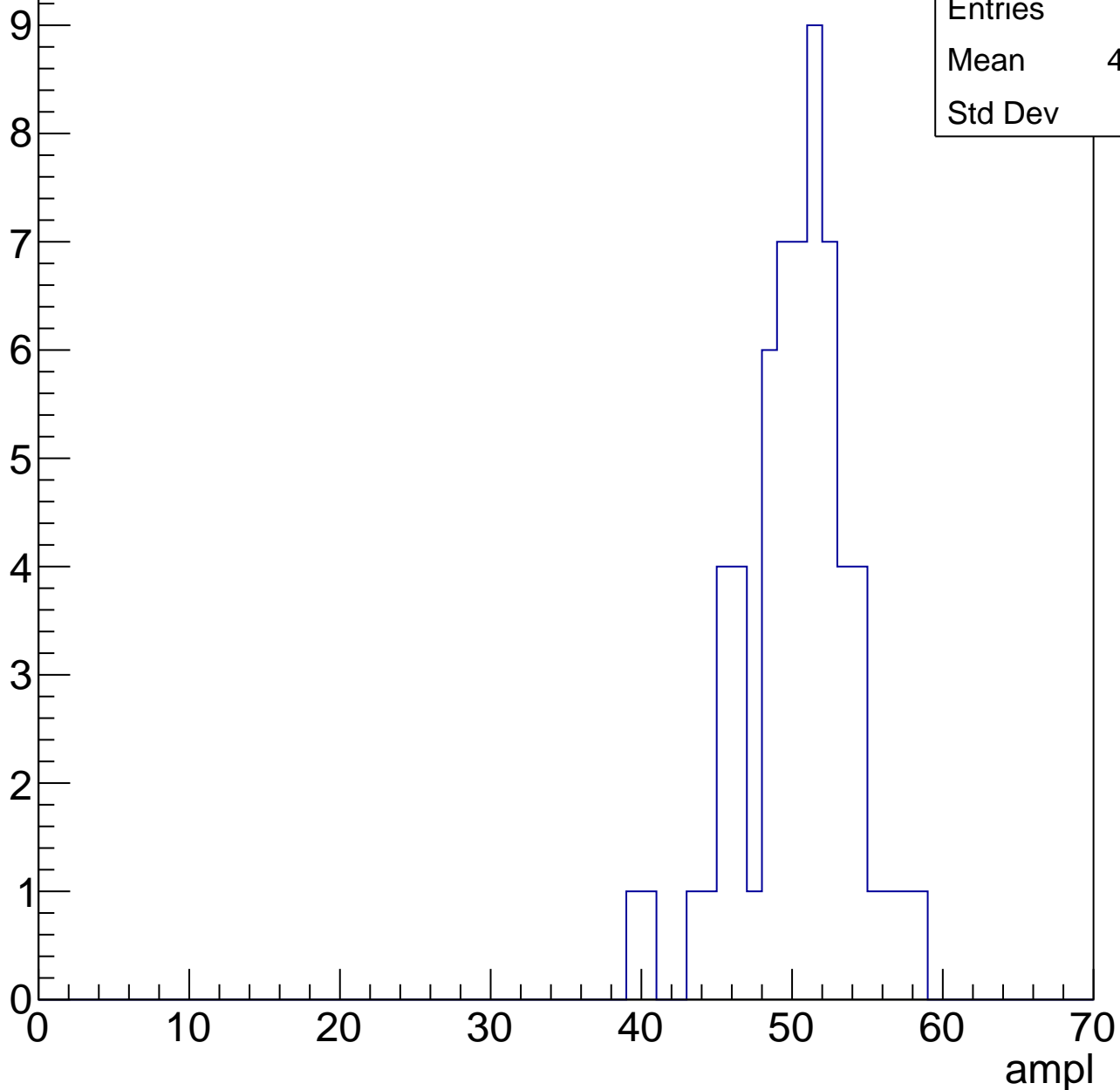
**Gaus Width: 3.8293**



# B0L001S, U10-ch32, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

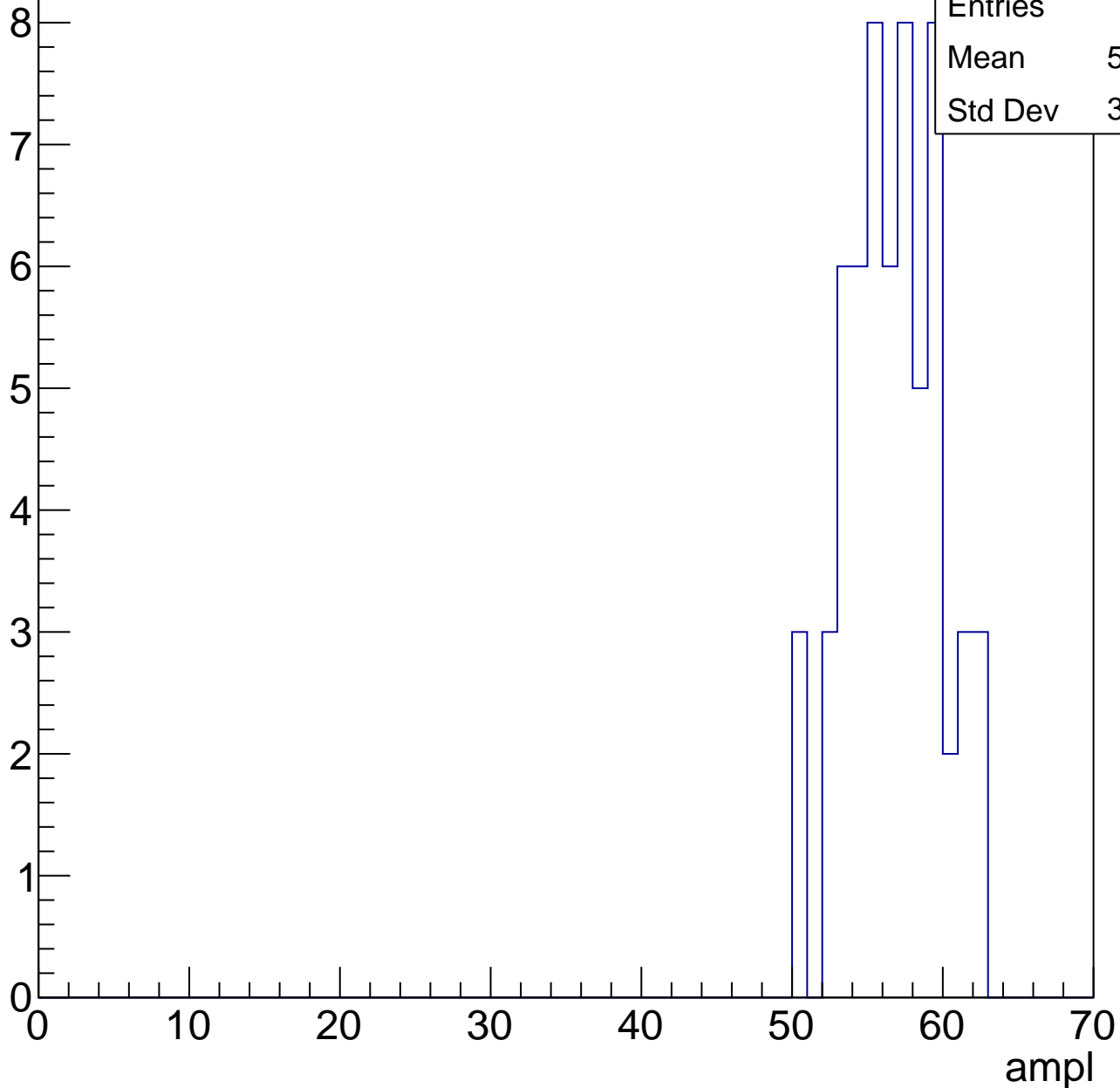


Entries	61
Mean	49.75
Std Dev	3.66

# B0L001S, U10-ch32, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	61
Mean	56.25
Std Dev	3.012

# B0L001S, U10-ch32, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

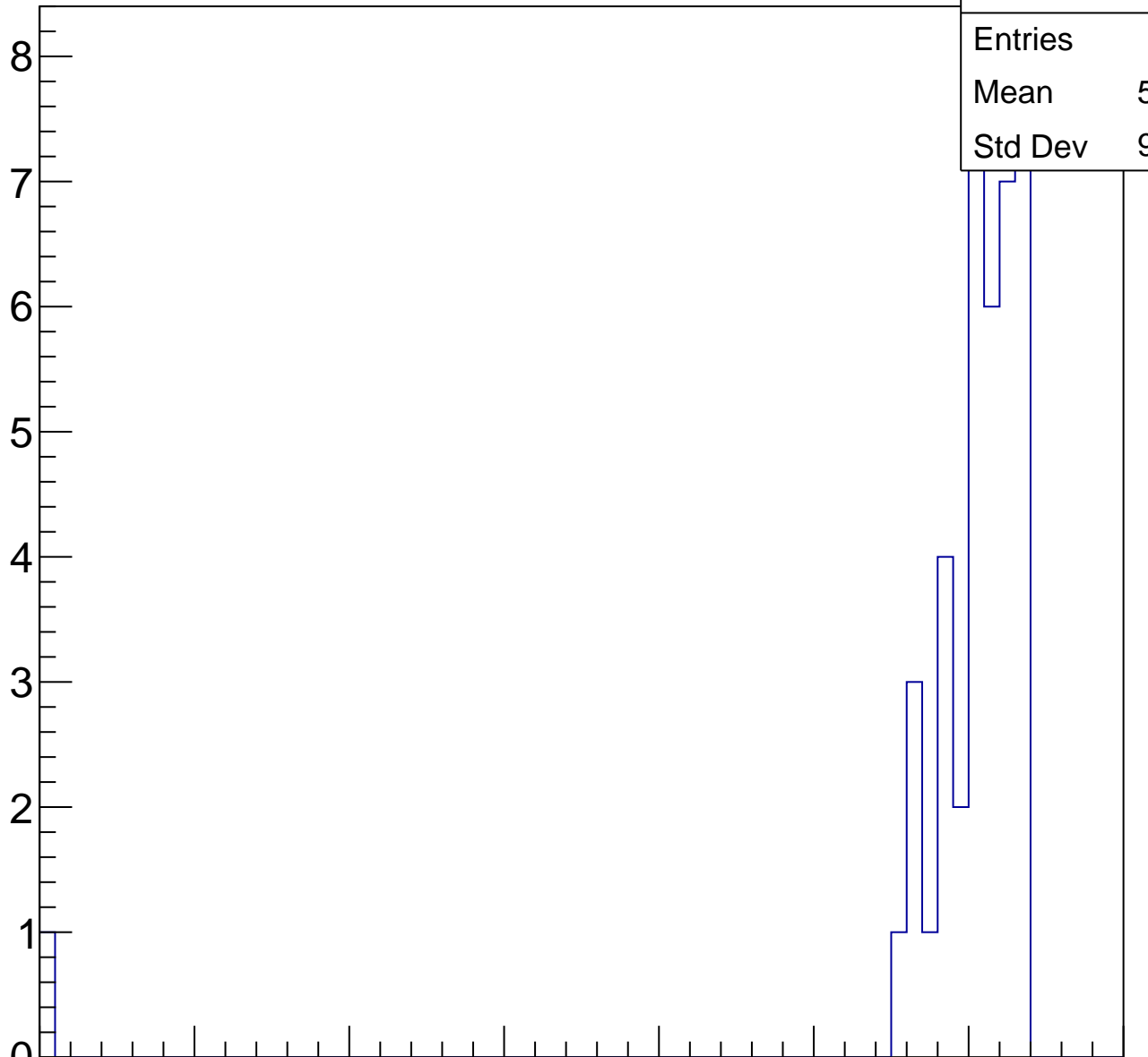
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	41
Mean	58.88
Std Dev	9.569

ampl

0 10 20 30 40 50 60 70



# B0L001S, U10-ch32, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch32, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U10-ch33, adc0

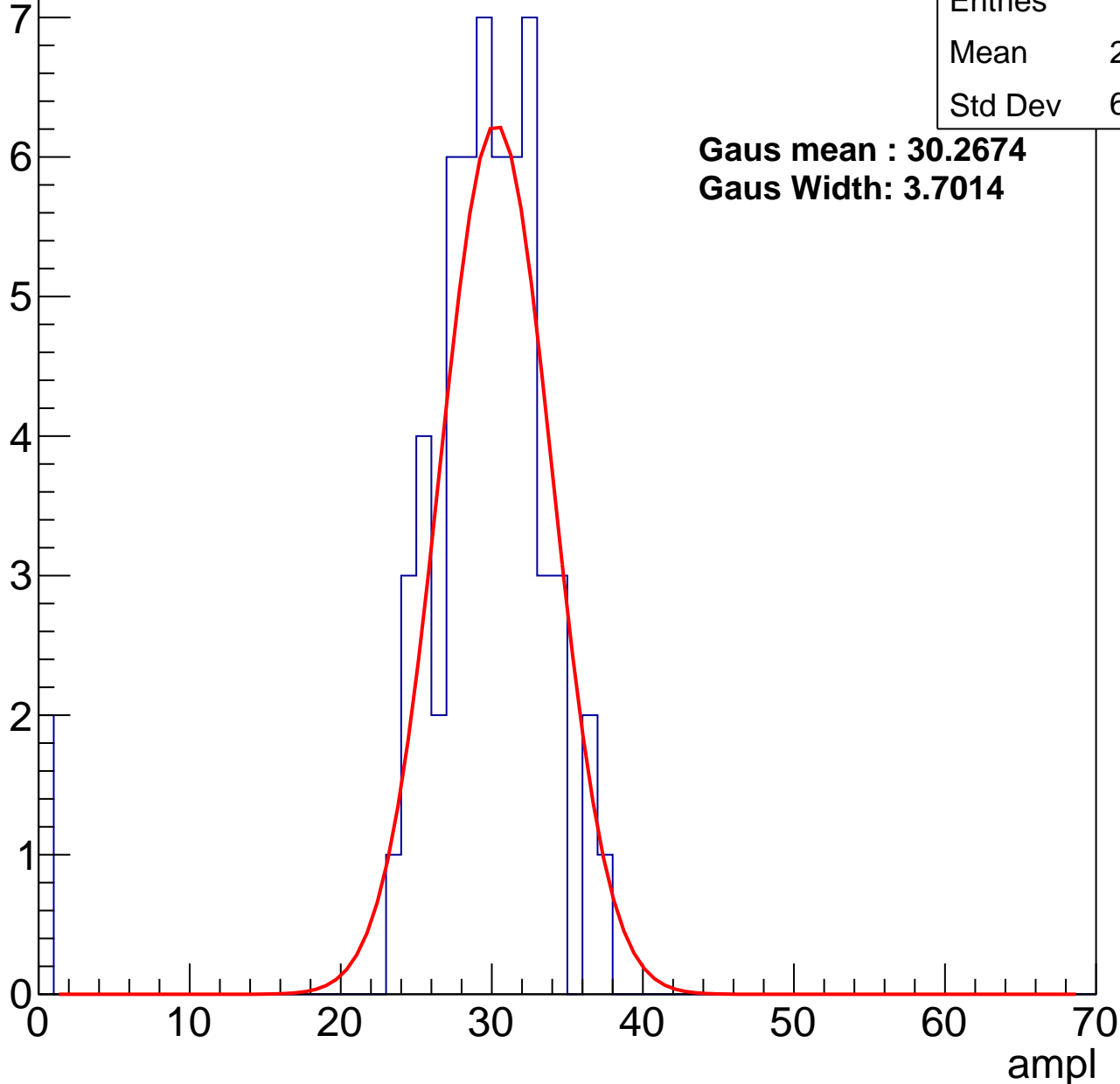
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	28.47
Std Dev	6.198

**Gaus mean : 30.2674**

**Gaus Width: 3.7014**



# B0L001S, U10-ch33, adc1

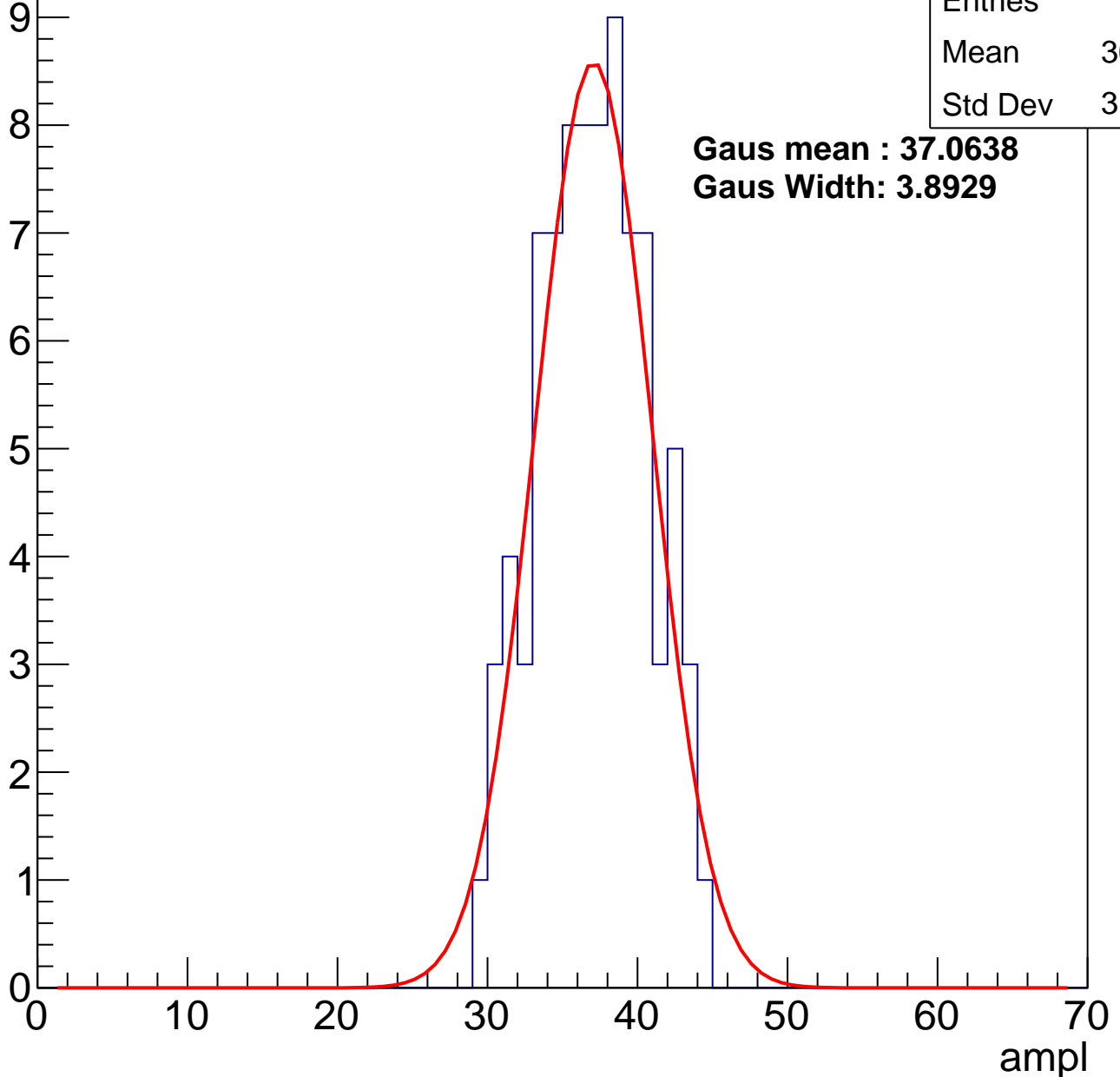
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	84
Mean	36.58
Std Dev	3.553

**Gaus mean : 37.0638**

**Gaus Width: 3.8929**



# B0L001S, U10-ch33, adc2

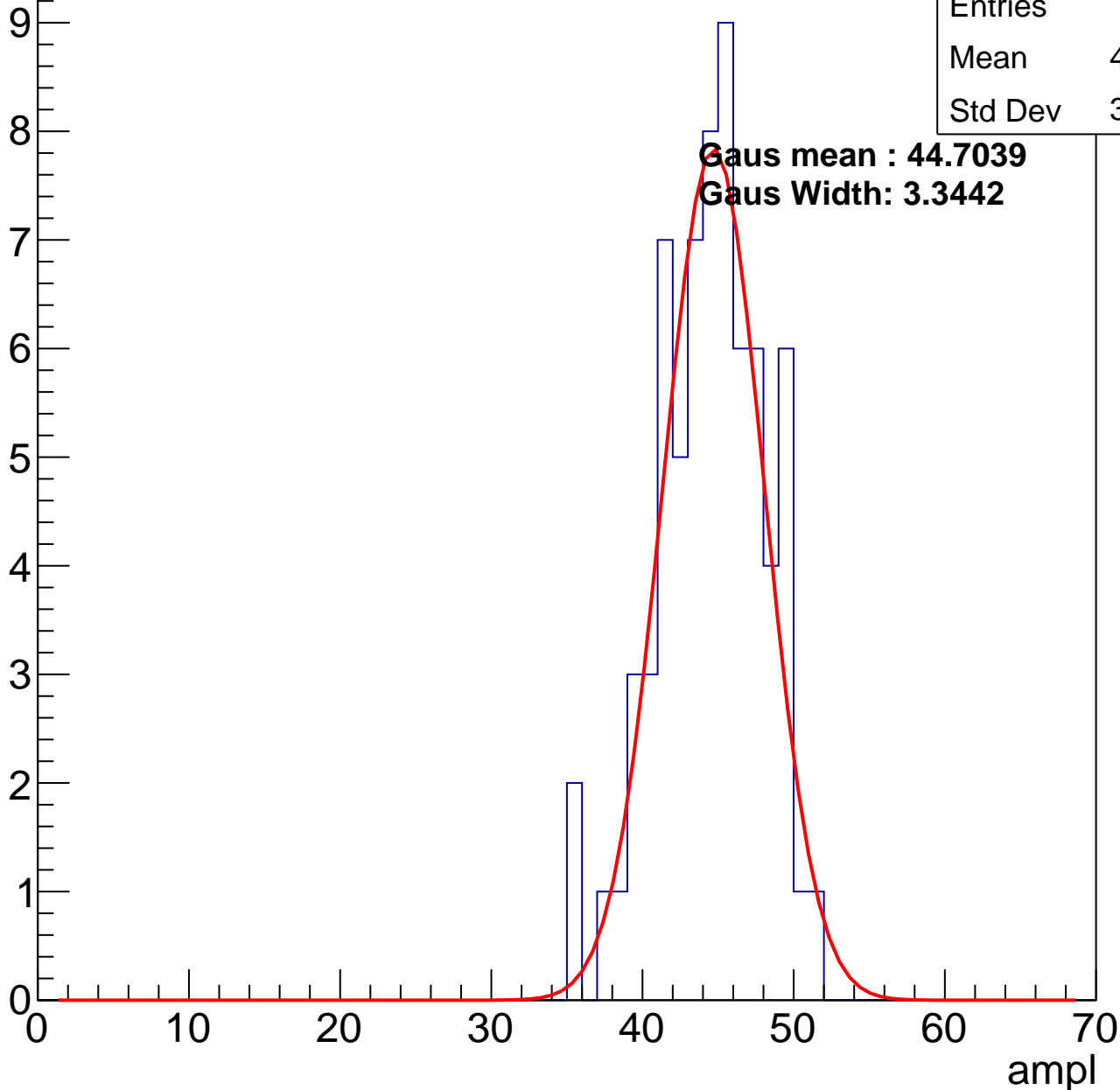
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	44.03
Std Dev	3.476

Gaus mean : 44.7039

Gaus Width: 3.3442

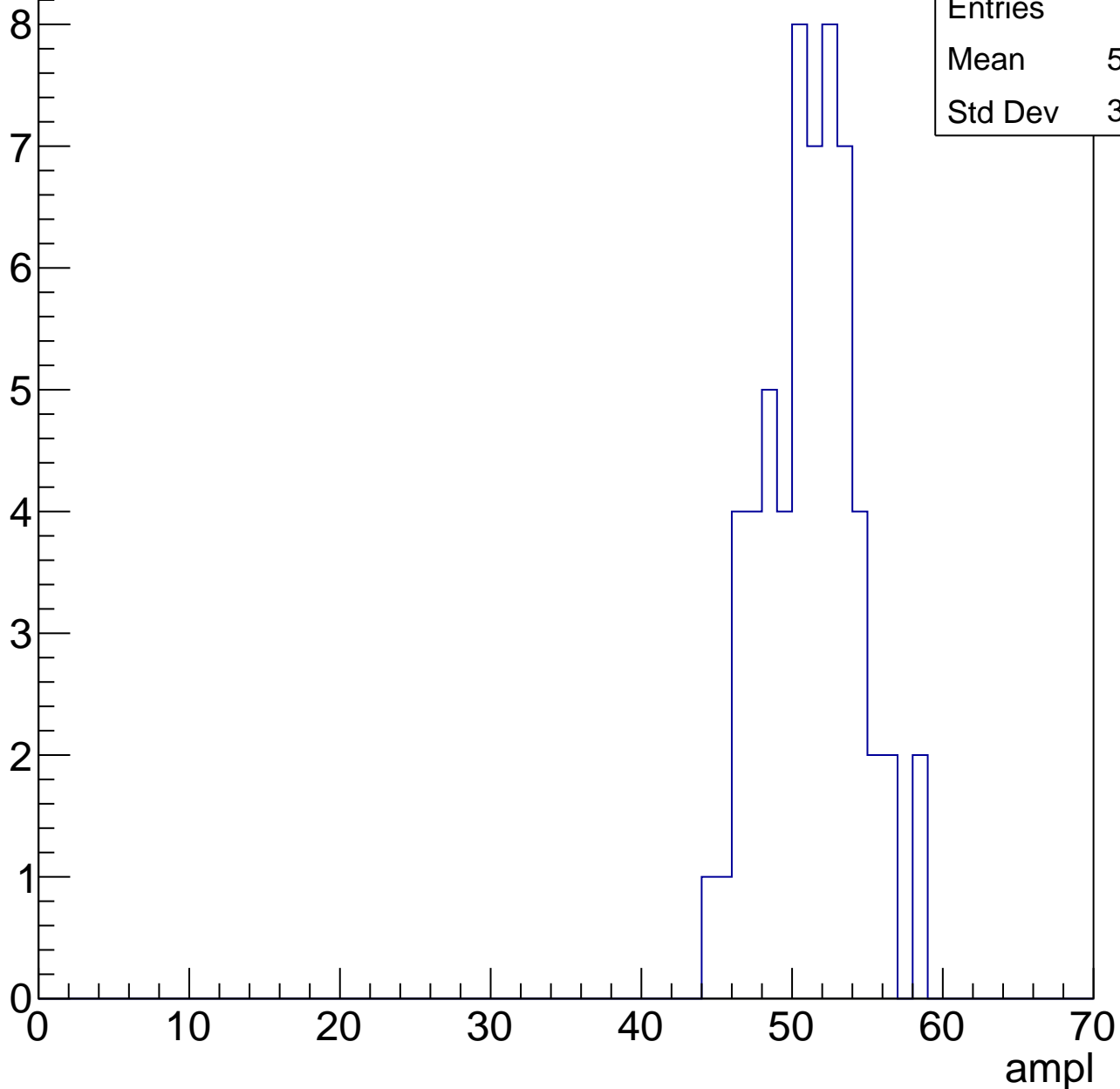


# B0L001S, U10-ch33, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	50.76
Std Dev	3.099



# B0L001S, U10-ch33, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

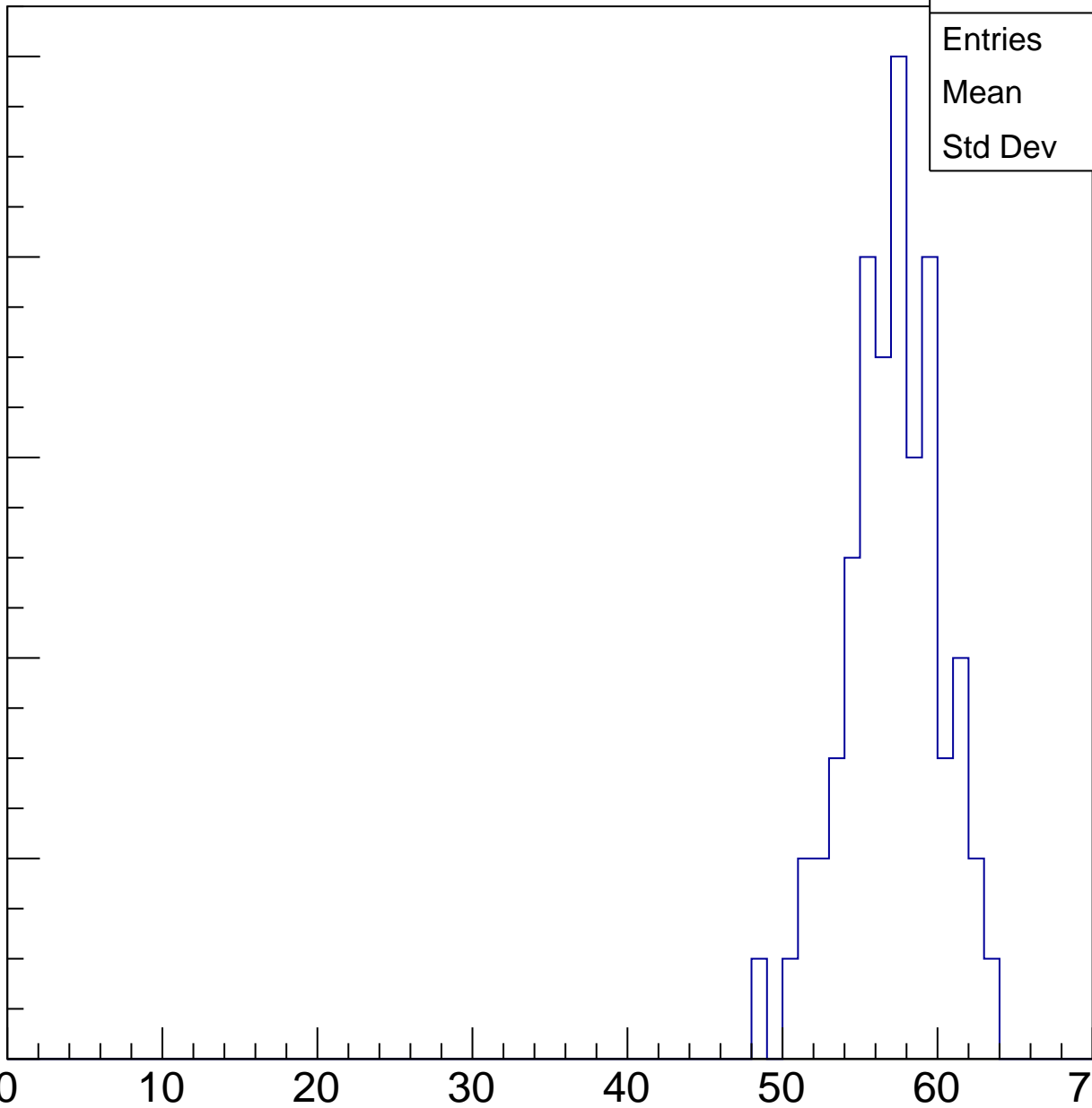
Entries	63
Mean	56.6
Std Dev	3.058

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

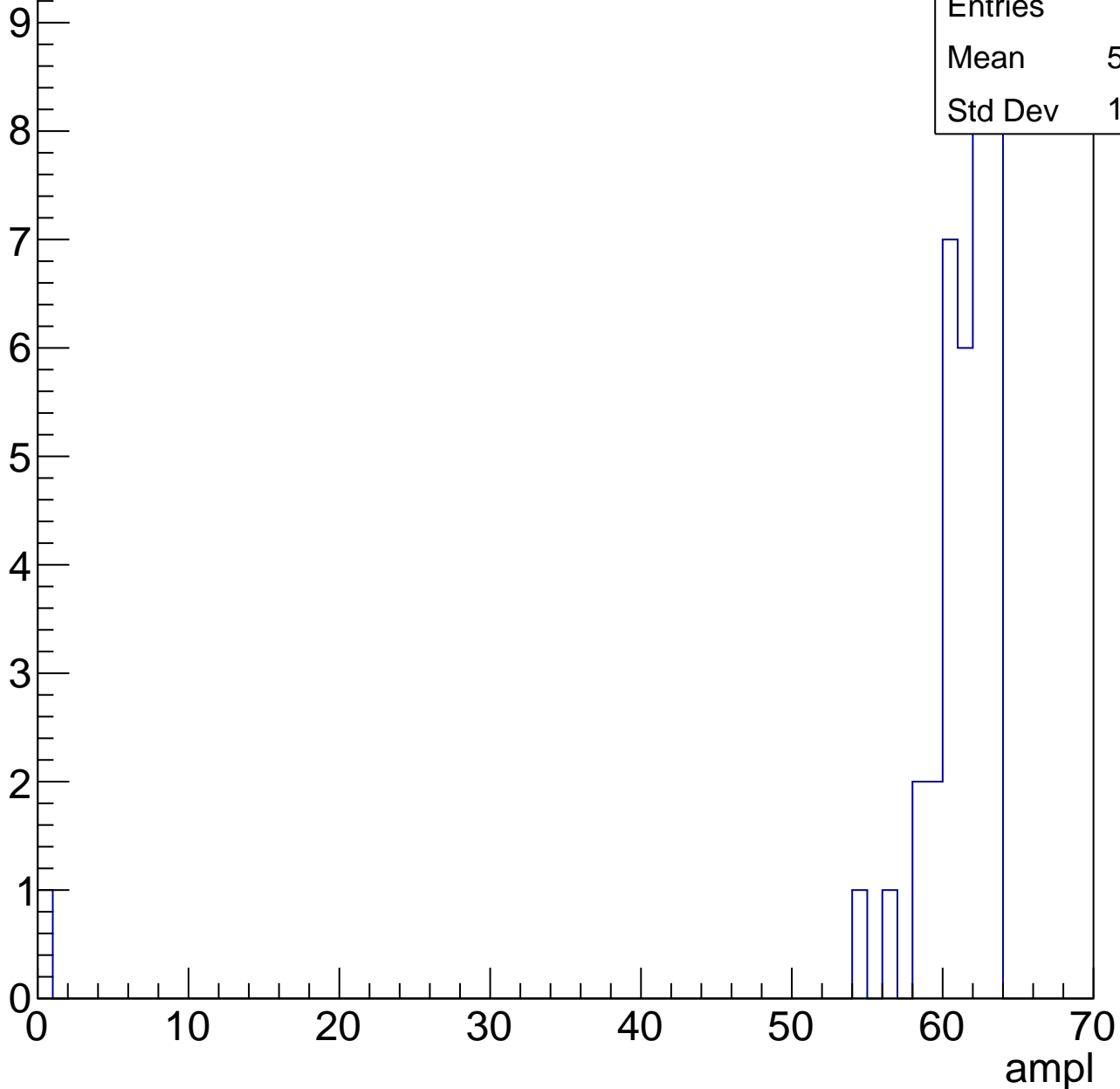


# B0L001S, U10-ch33, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	37
Mean	59.27
Std Dev	10.08



# B0L001S, U10-ch33, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U10-ch33, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U10-ch34, adc0

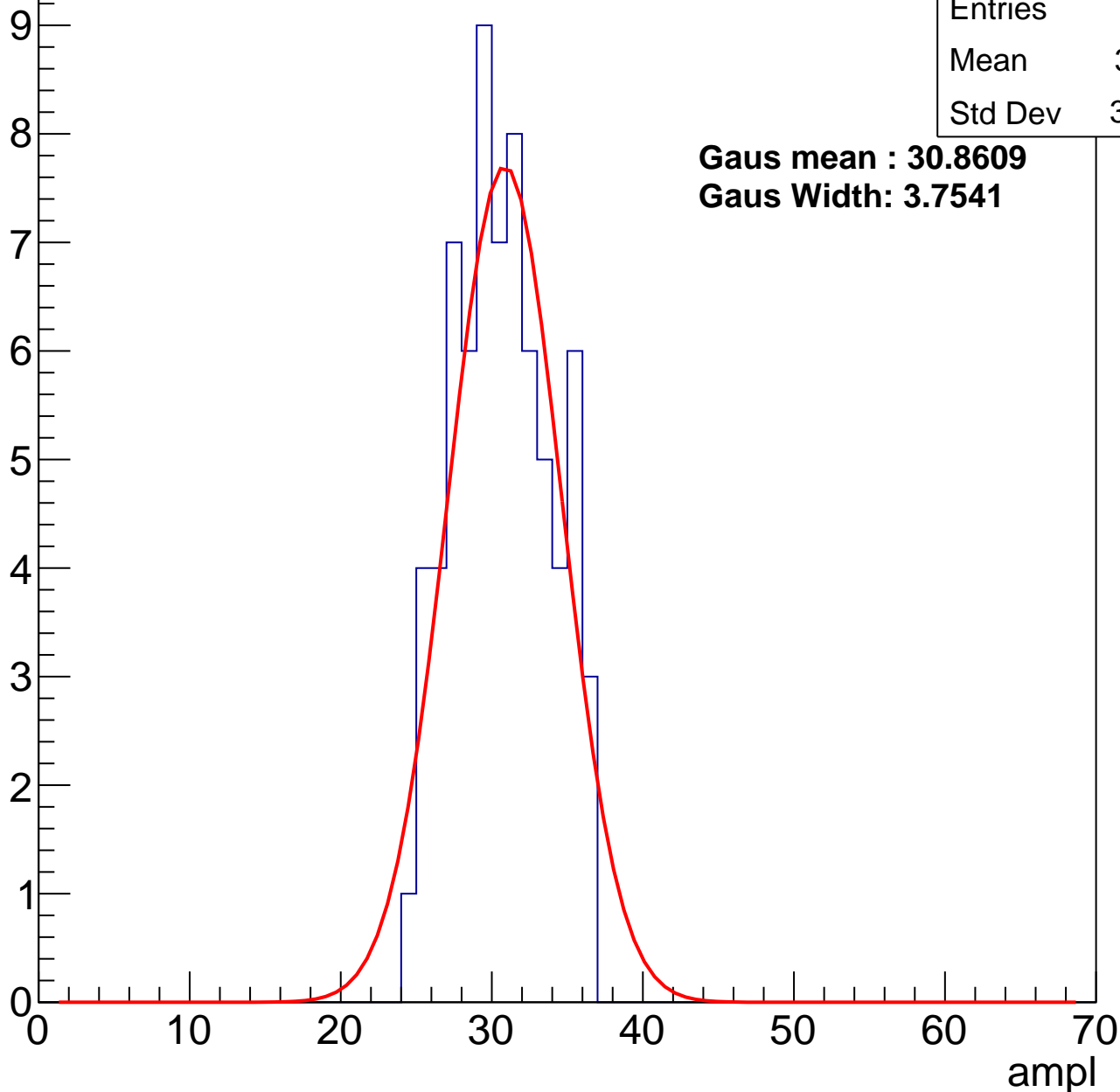
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	30.21
Std Dev	3.144

**Gaus mean : 30.8609**

**Gaus Width: 3.7541**



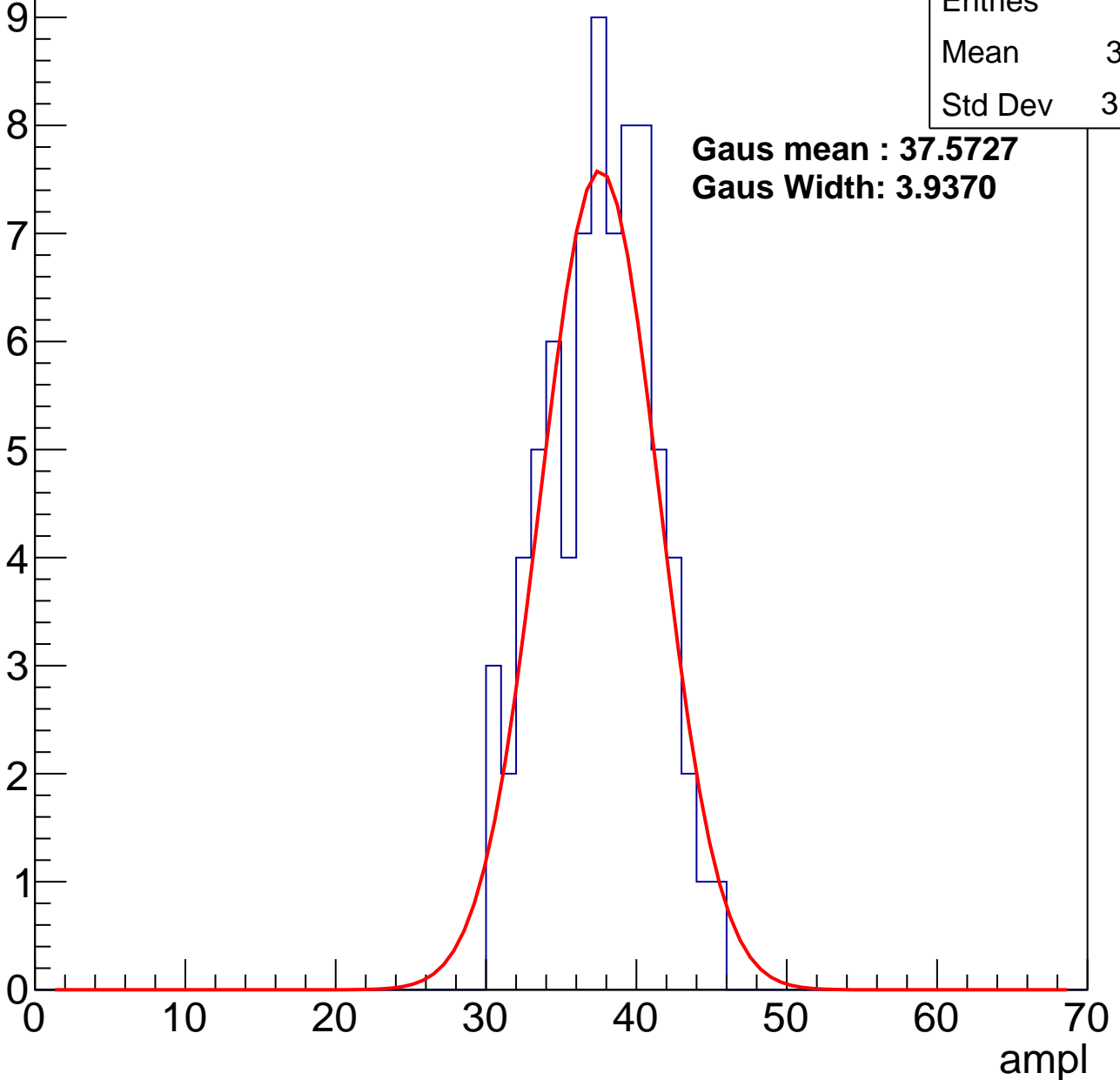
# B0L001S, U10-ch34, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	76
Mean	37.11
Std Dev	3.538

**Gaus mean : 37.5727**  
**Gaus Width: 3.9370**



# B0L001S, U10-ch34, adc2

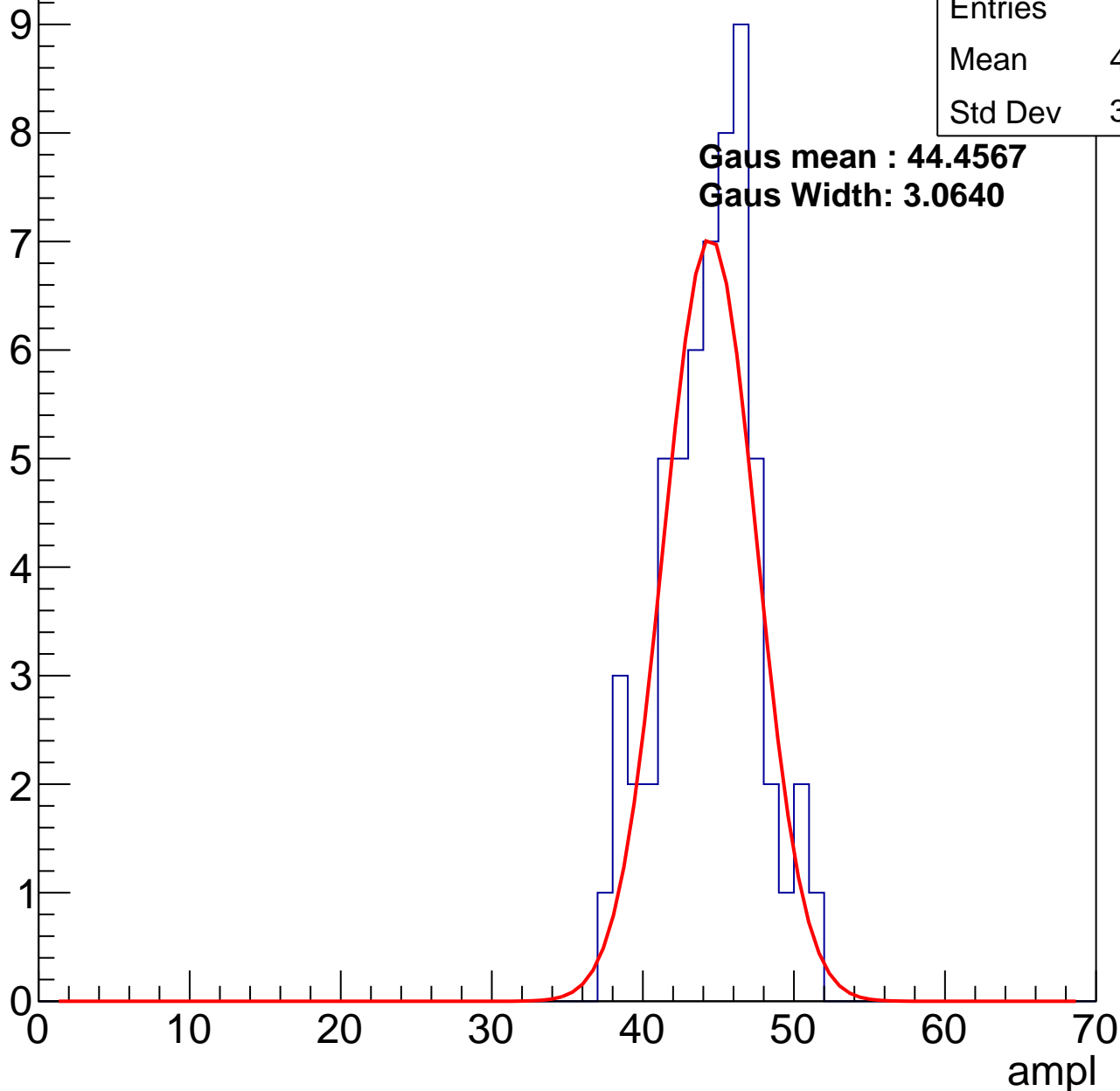
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	43.98
Std Dev	3.127

**Gaus mean : 44.4567**

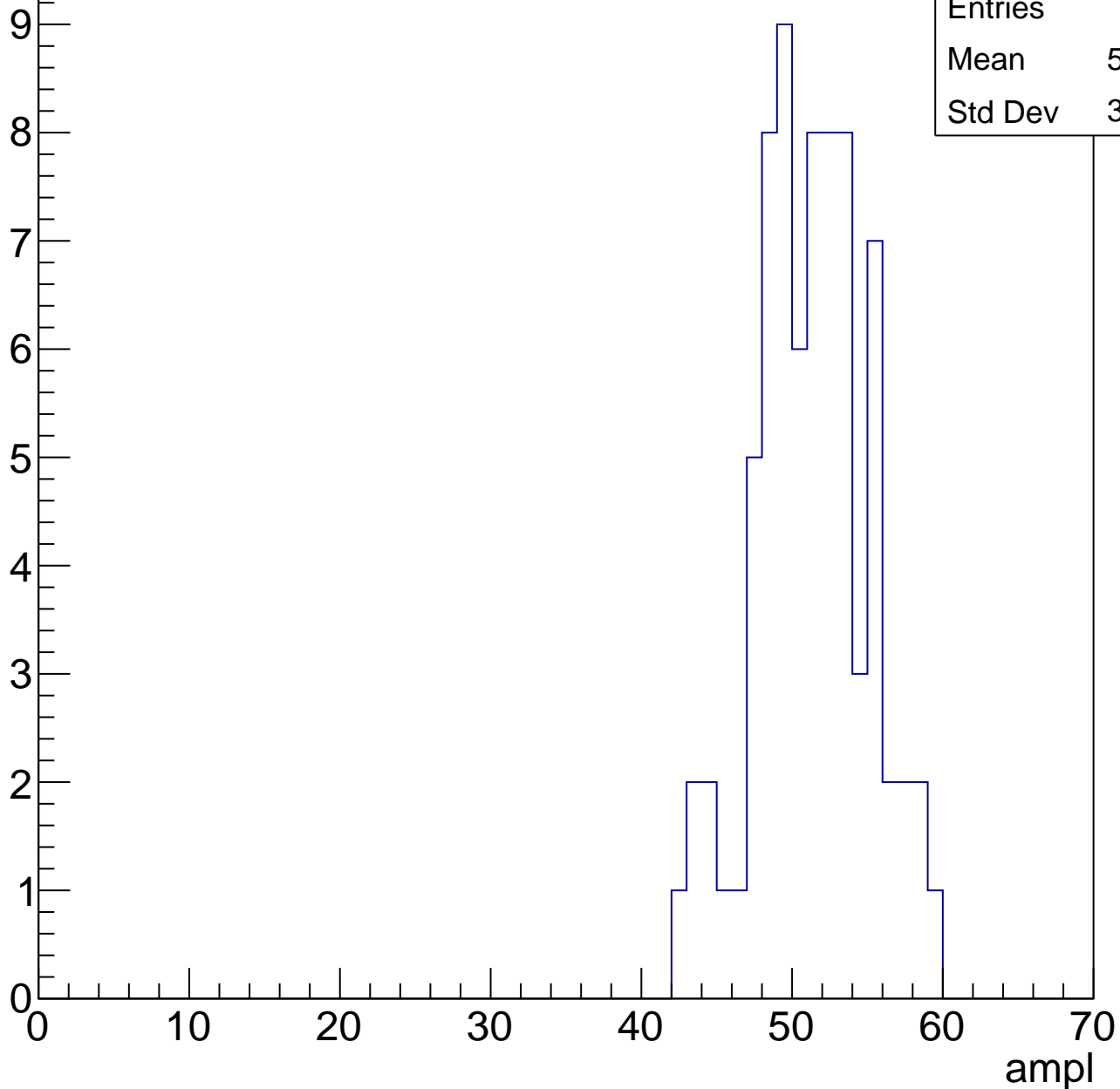
**Gaus Width: 3.0640**



# B0L001S, U10-ch34, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	76
Mean	50.83
Std Dev	3.668

# B0L001S, U10-ch34, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

6

5

4

3

2

1

0

Entries	41
Mean	56.39
Std Dev	3.027

0

1

2

3

4

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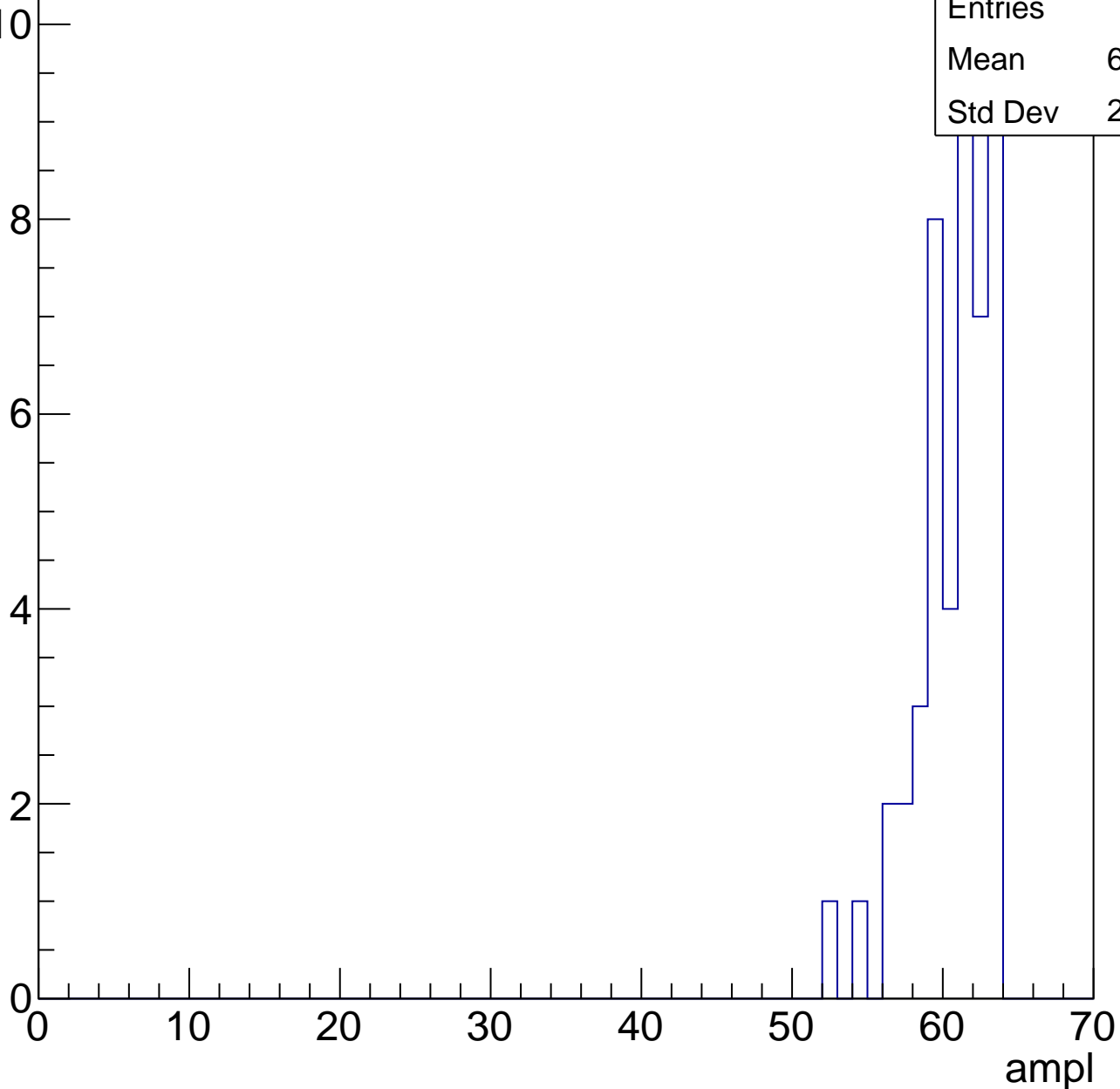
323

# B0L001S, U10-ch34, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

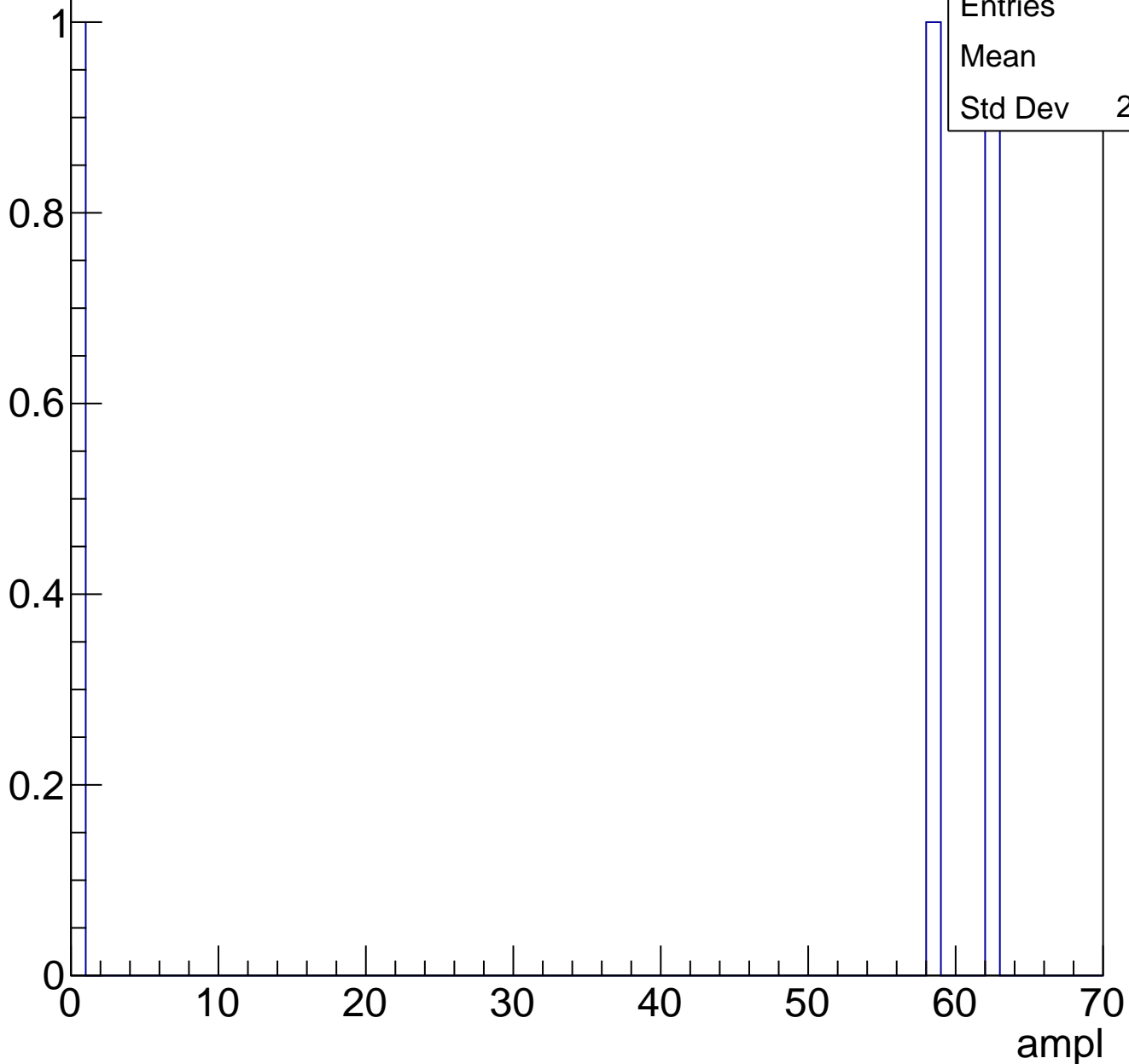
Entries	47
Mean	60.23
Std Dev	2.503



# B0L001S, U10-ch34, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch34, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	11
Std Dev	11

# B0L001S, U10-ch35, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	70
Mean	30.77
Std Dev	6.114

**Gaus mean : 31.8868**

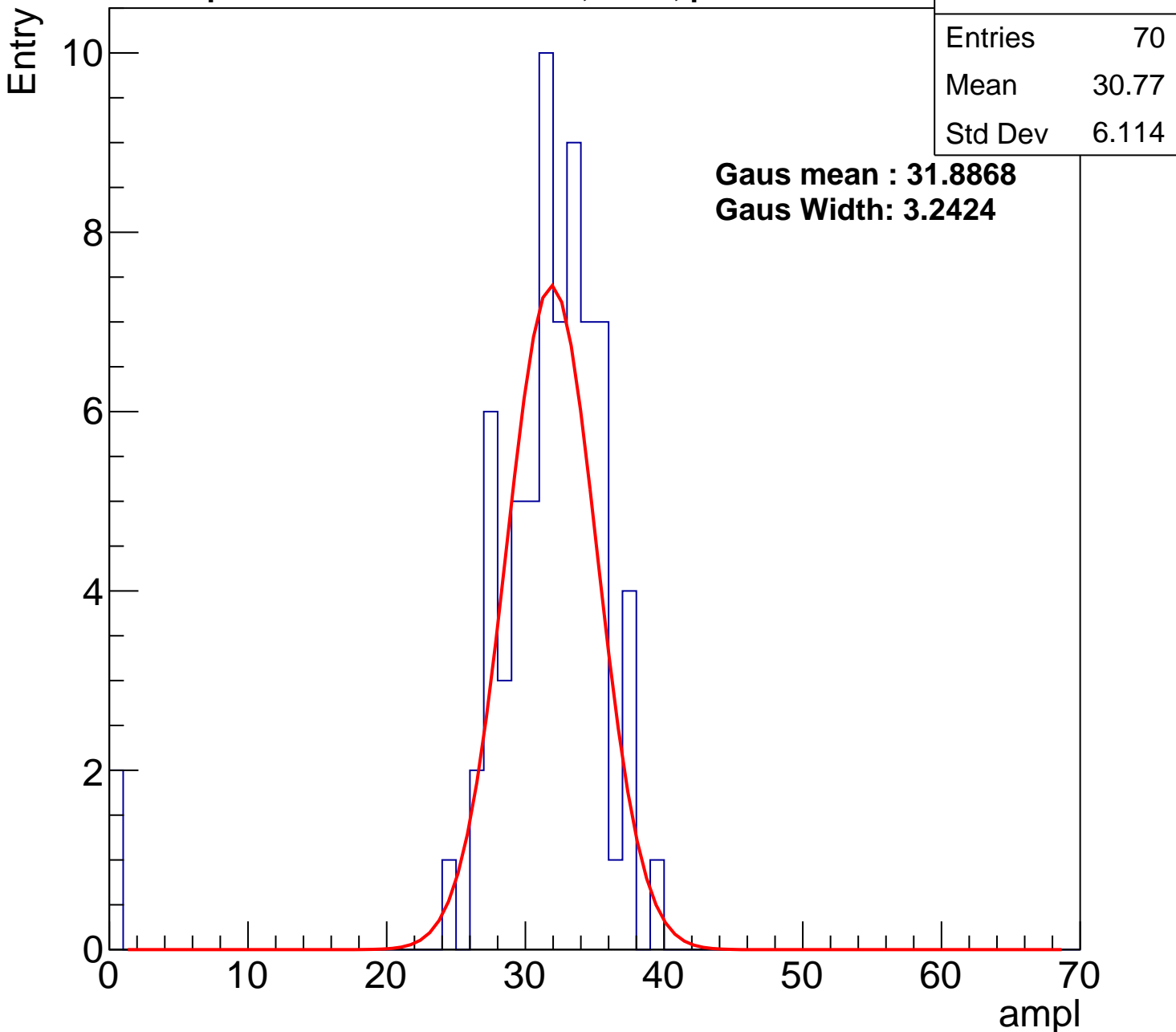
**Gaus Width: 3.2424**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U10-ch35, adc1

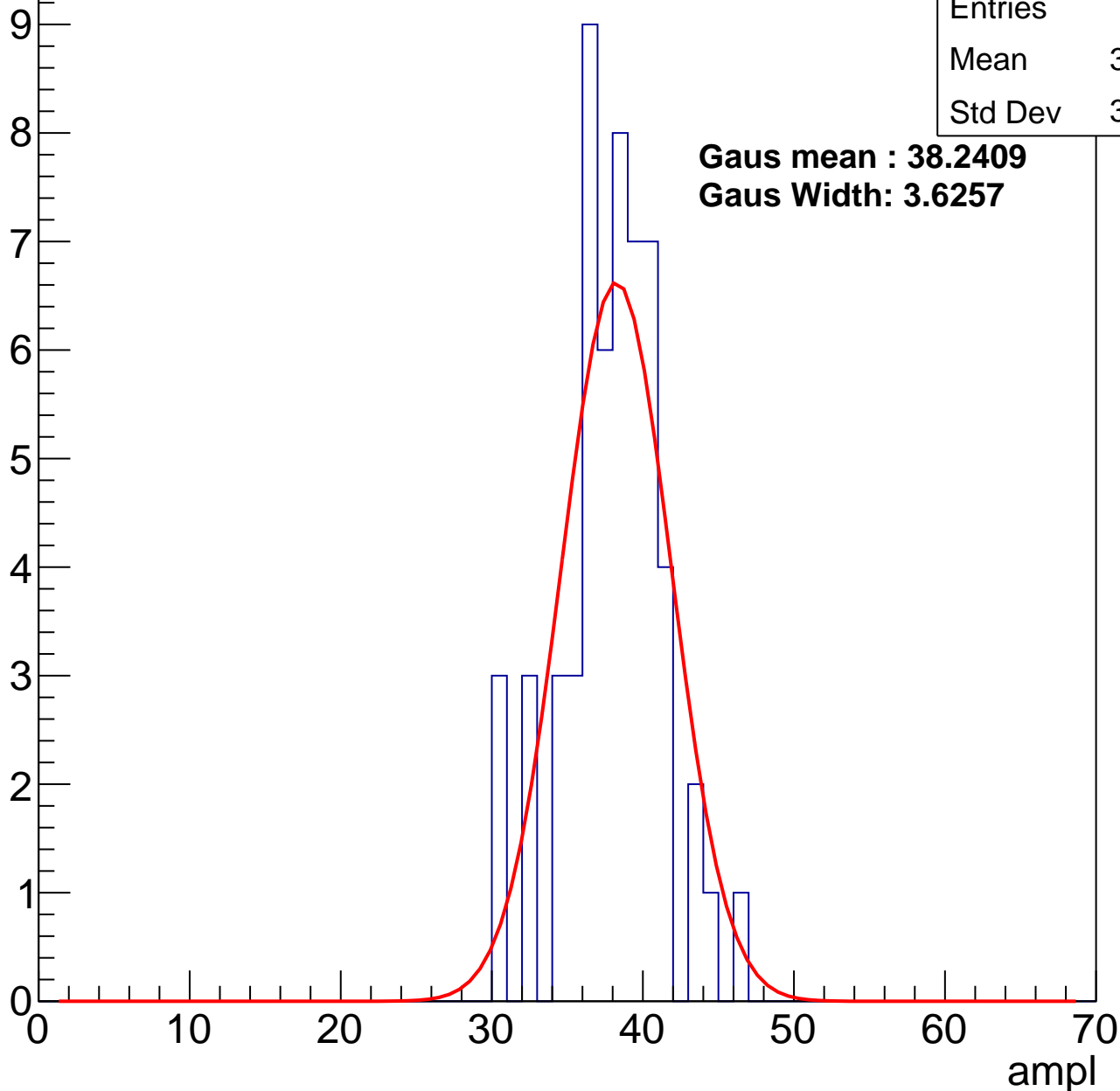
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	37.47
Std Dev	3.304

**Gaus mean : 38.2409**

**Gaus Width: 3.6257**



# B0L001S, U10-ch35, adc2

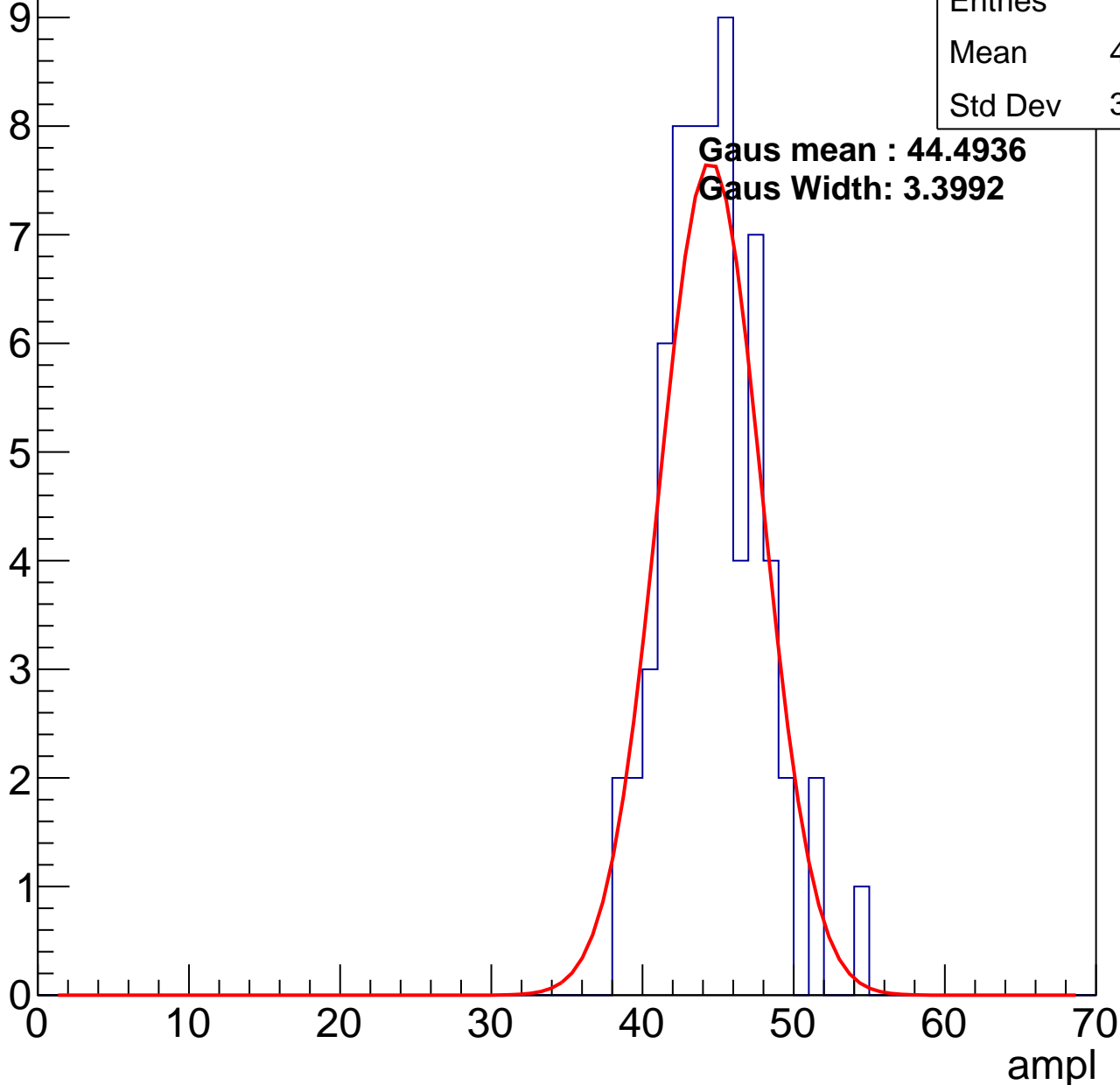
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	44.18
Std Dev	3.167

**Gaus mean : 44.4936**

**Gaus Width: 3.3992**



# B0L001S, U10-ch35, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	66
Mean	50.67
Std Dev	3.59

Entry

10

8

6

4

2

0

0

10

20

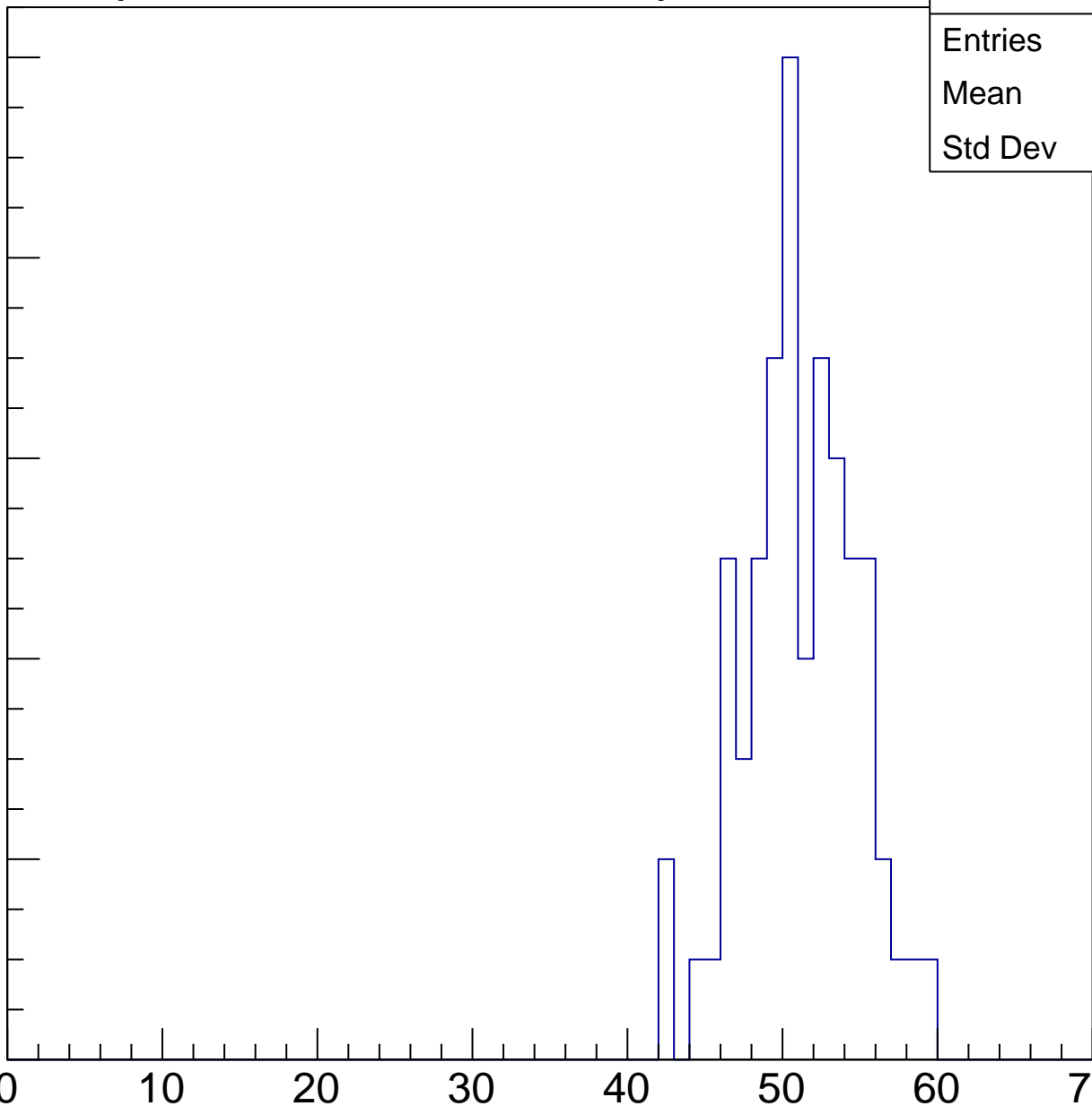
30

40

50

60

ampl

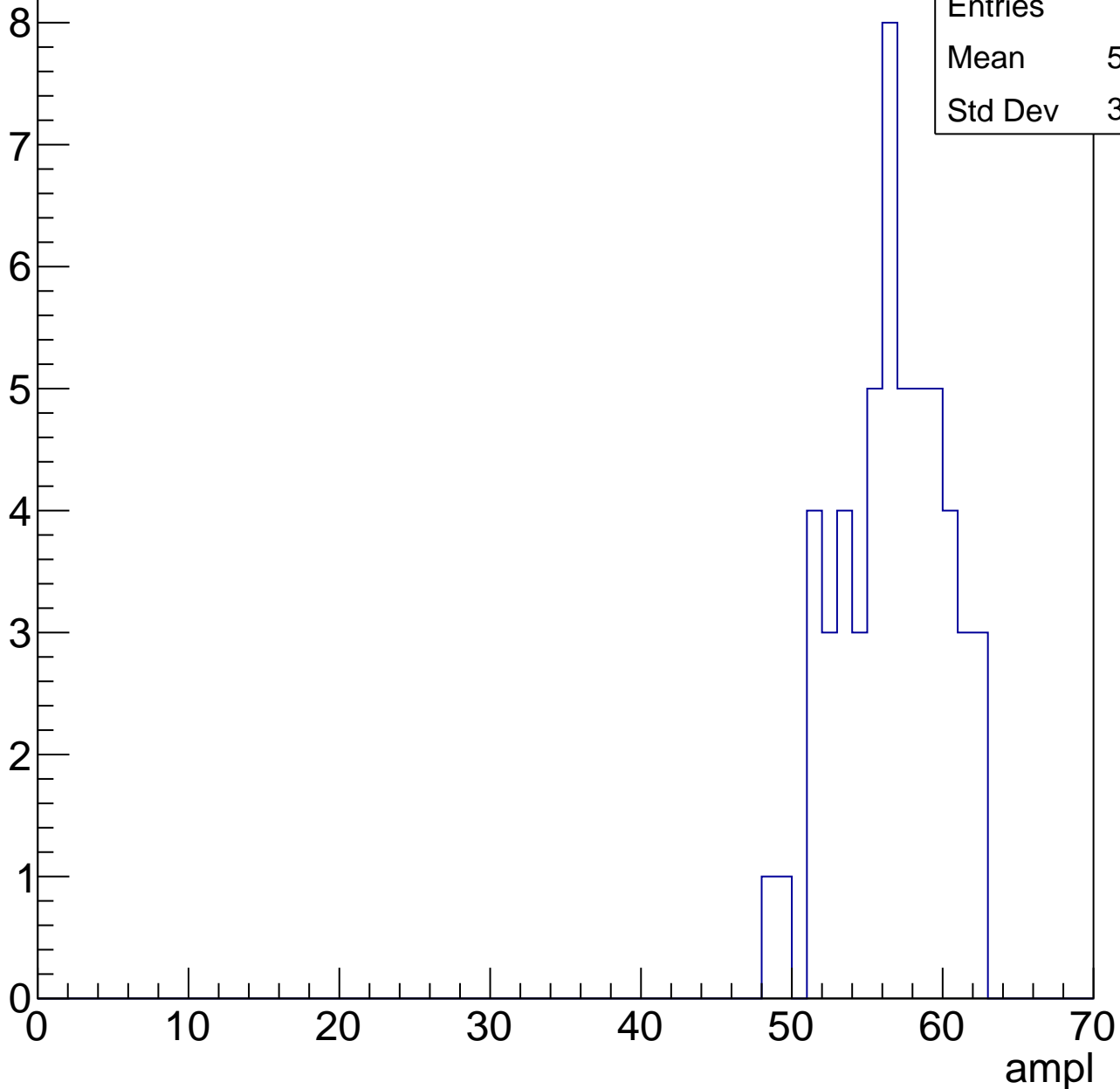


# B0L001S, U10-ch35, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	56.17
Std Dev	3.414

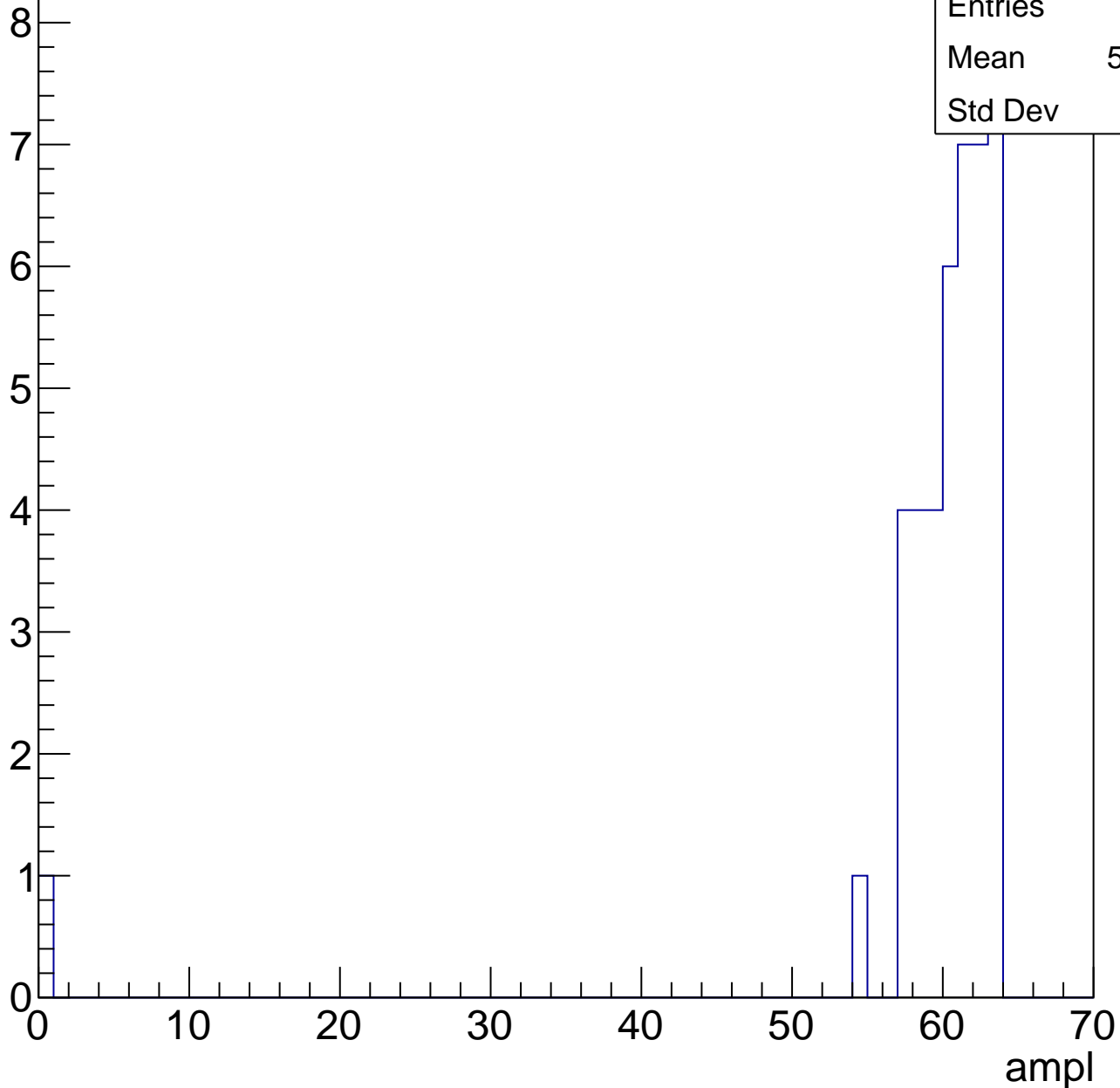


# B0L001S, U10-ch35, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	42
Mean	58.93
Std Dev	9.45



# B0L001S, U10-ch35, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch35, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U10-ch36, adc0

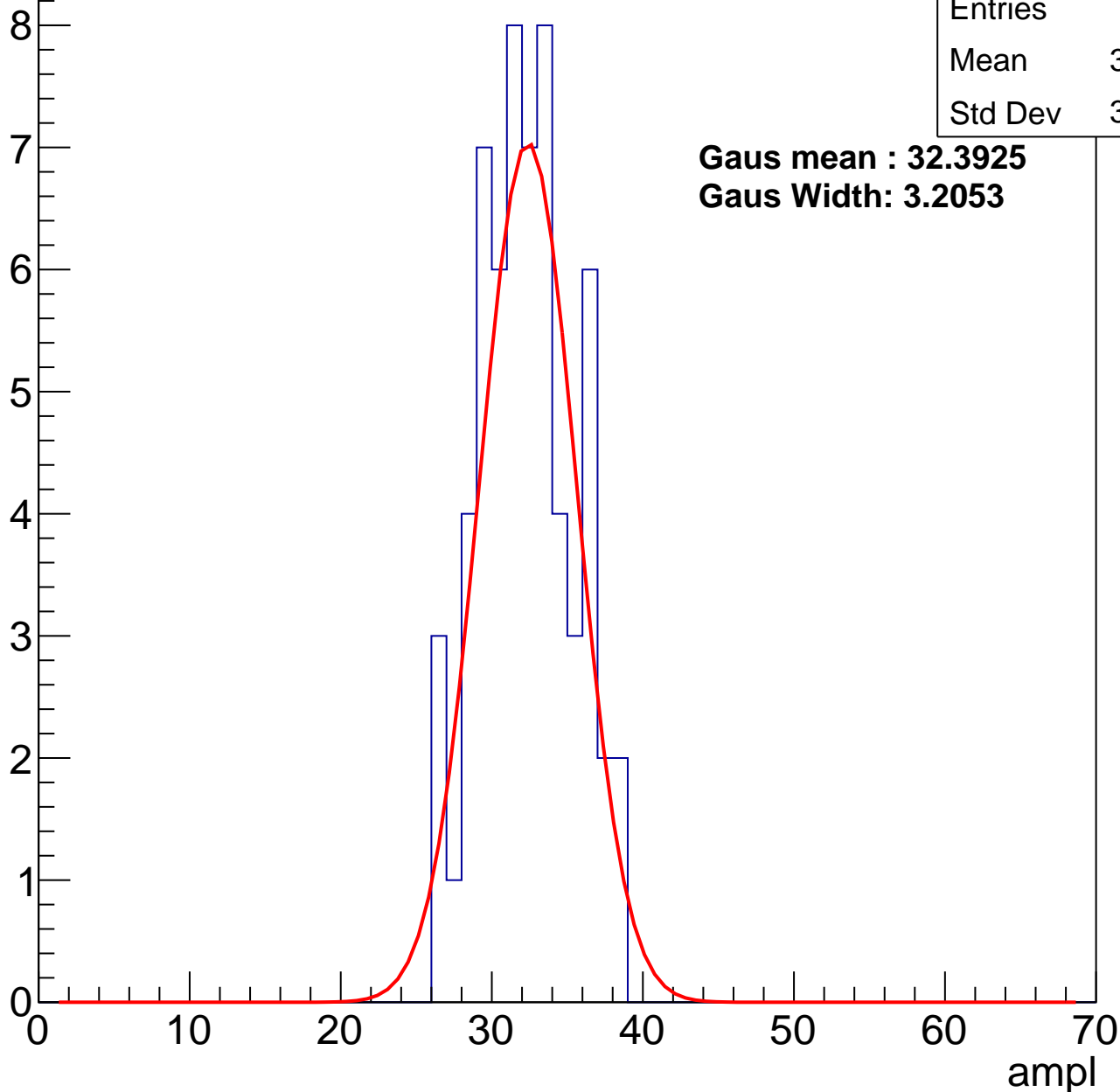
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	31.85
Std Dev	3.029

**Gaus mean : 32.3925**

**Gaus Width: 3.2053**



# B0L001S, U10-ch36, adc1

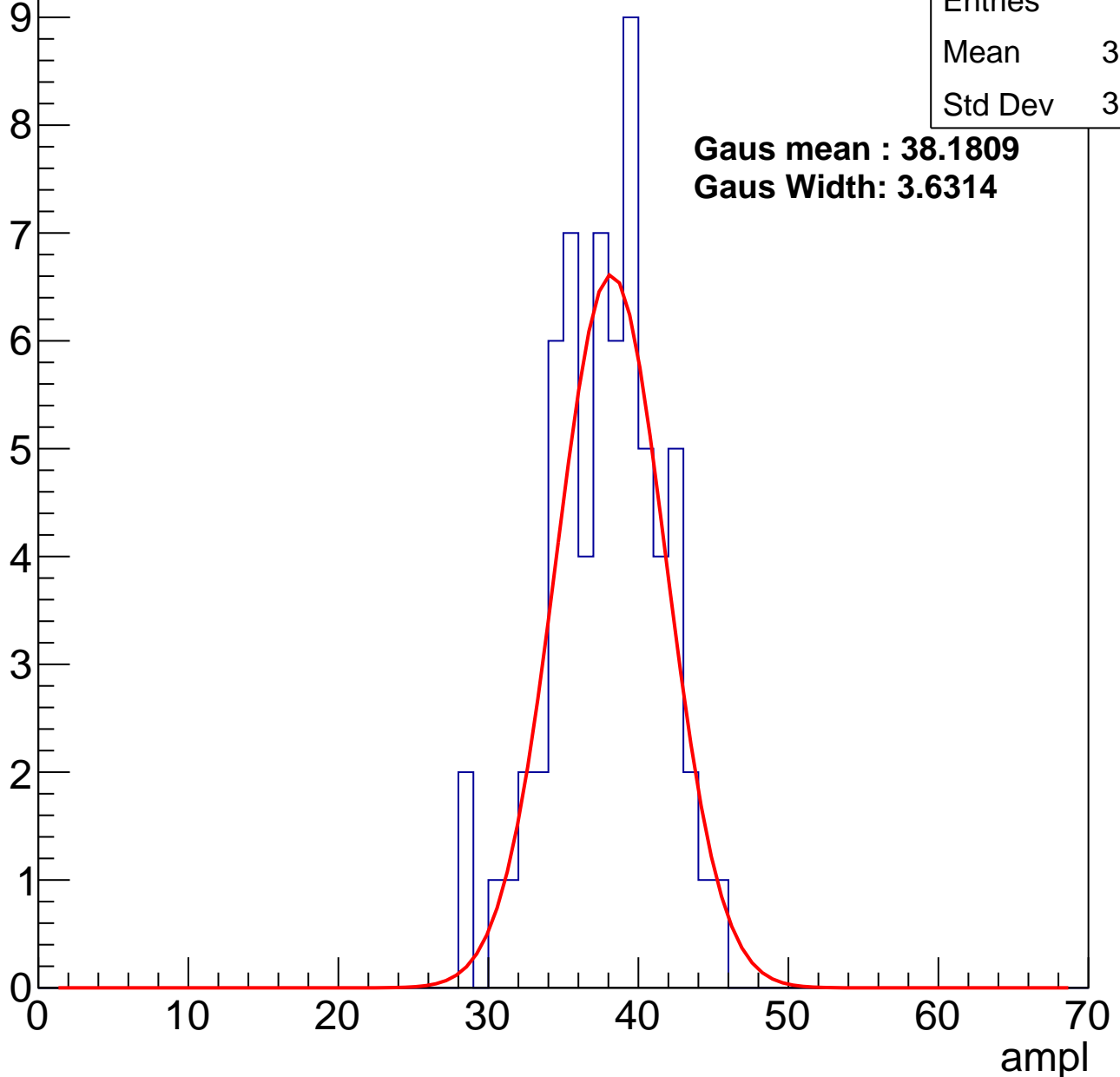
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	37.34
Std Dev	3.655

**Gaus mean : 38.1809**

**Gaus Width: 3.6314**



# B0L001S, U10-ch36, adc2

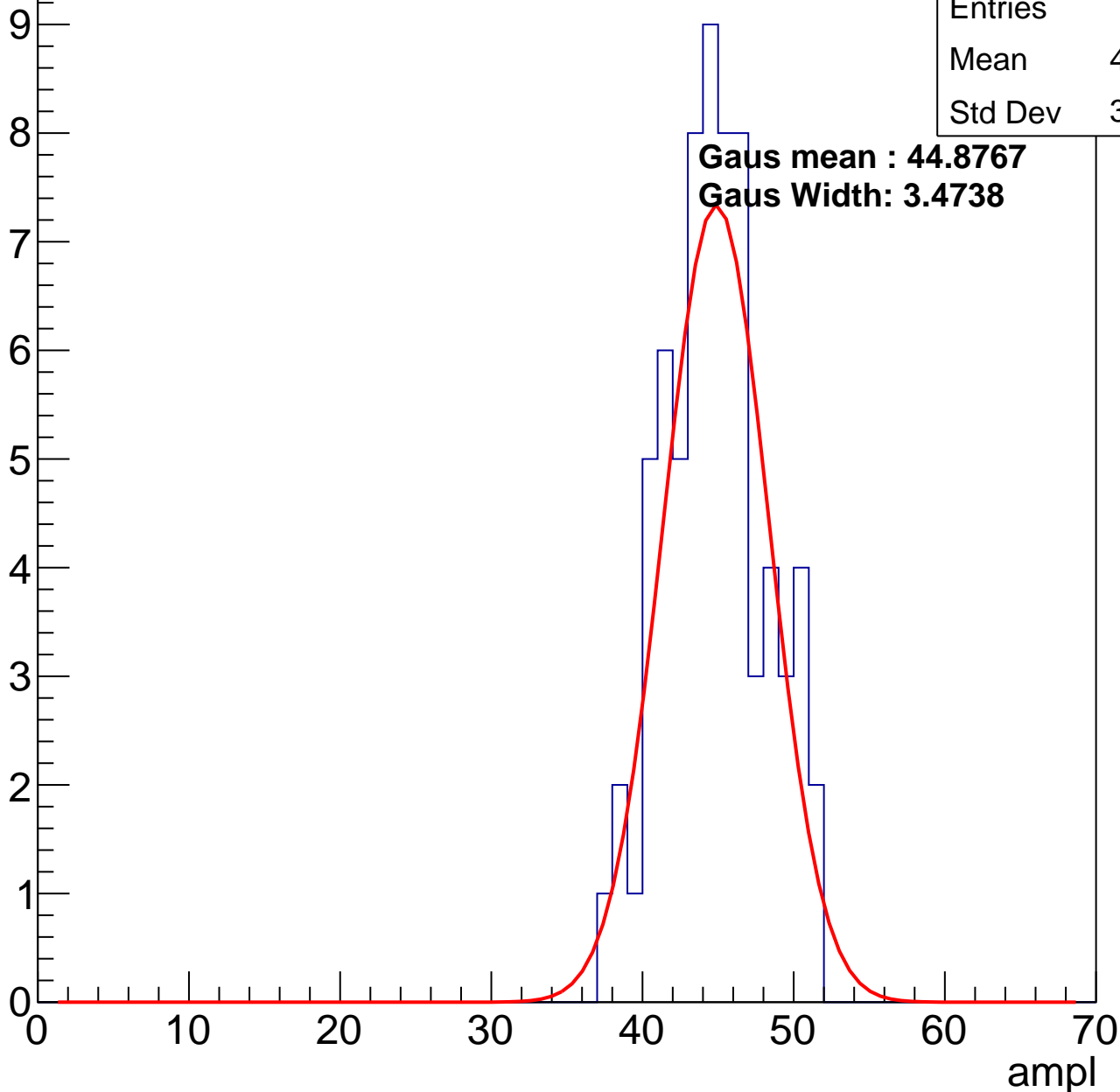
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	44.32
Std Dev	3.295

**Gaus mean : 44.8767**

**Gaus Width: 3.4738**

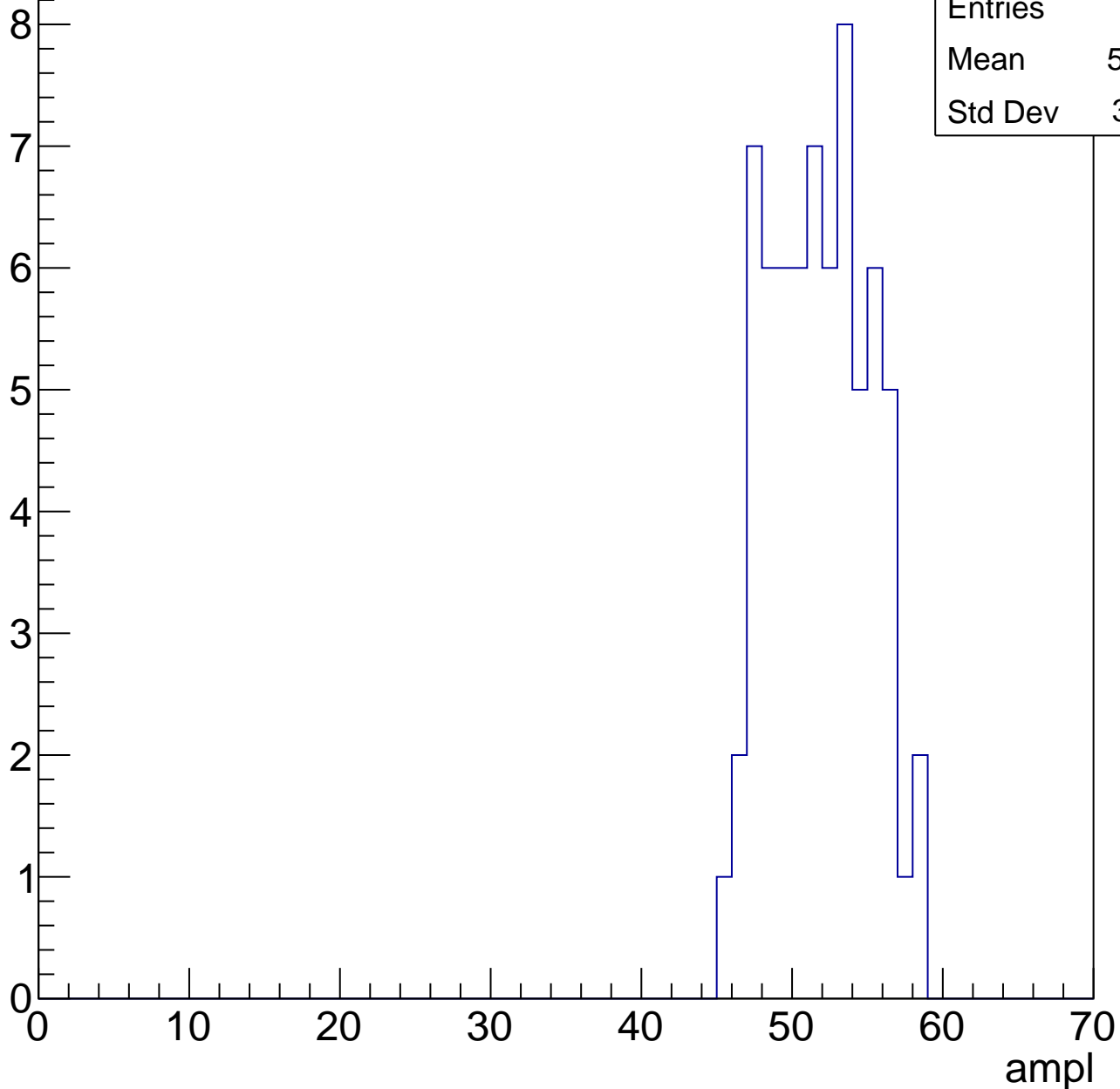


# B0L001S, U10-ch36, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	51.38
Std Dev	3.231

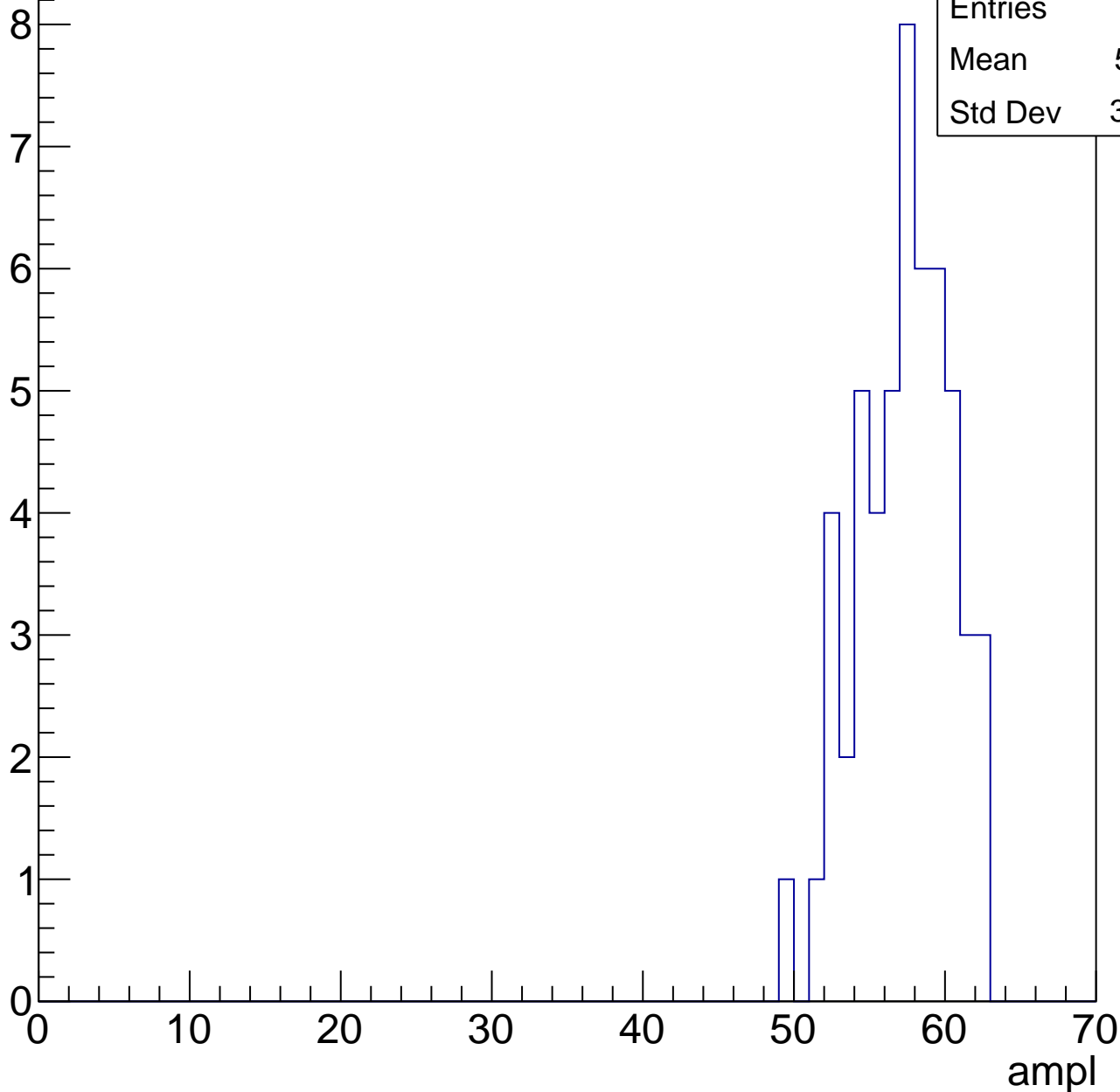


# B0L001S, U10-ch36, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	56.81
Std Dev	3.053

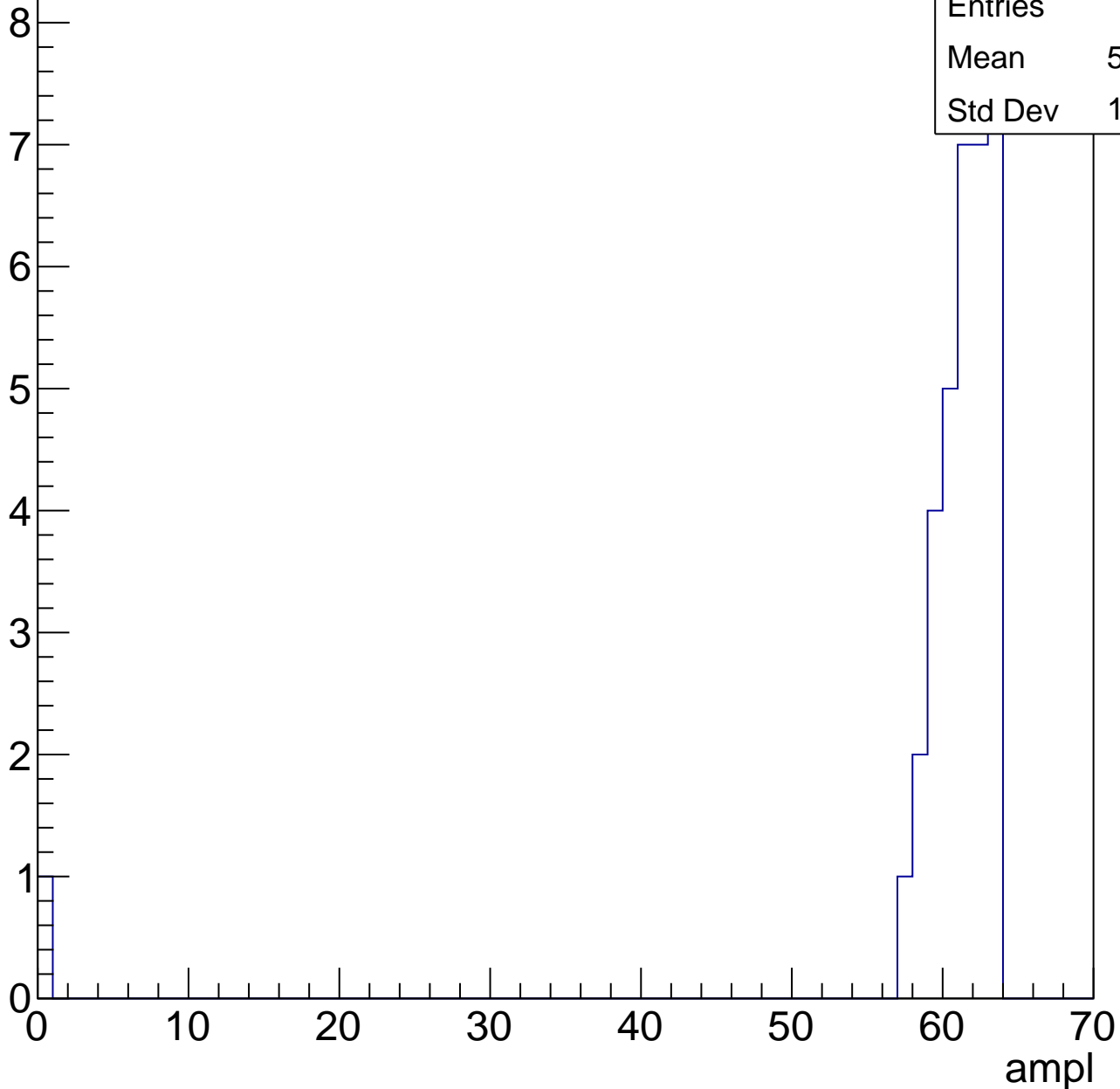


# B0L001S, U10-ch36, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	35
Mean	59.26
Std Dev	10.29



# B0L001S, U10-ch36, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch36, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U10-ch37, adc0

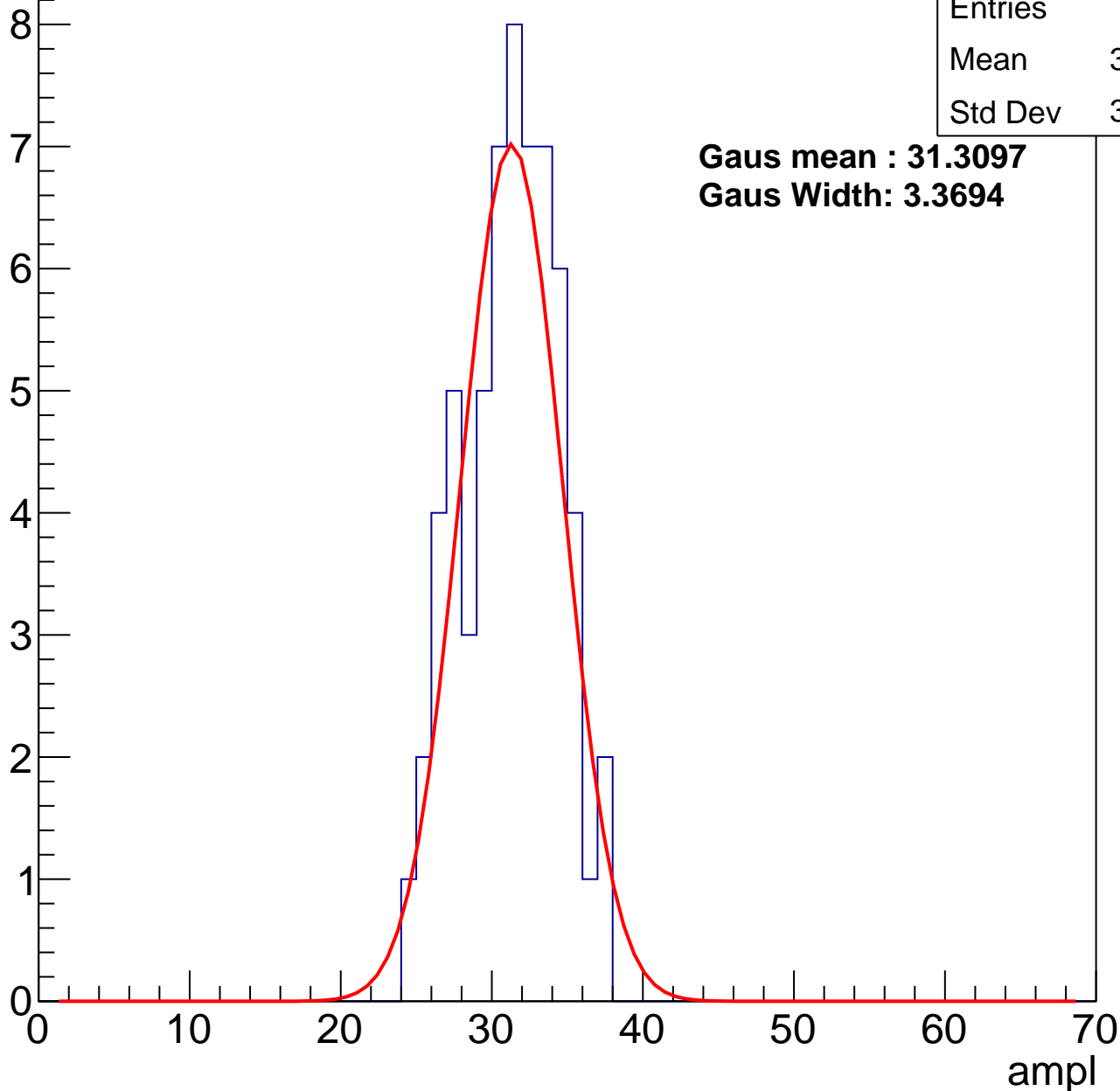
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	30.79
Std Dev	3.117

**Gaus mean : 31.3097**

**Gaus Width: 3.3694**



# B0L001S, U10-ch37, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	80
Mean	37.85
Std Dev	3.966

**Gaus mean : 38.6952**

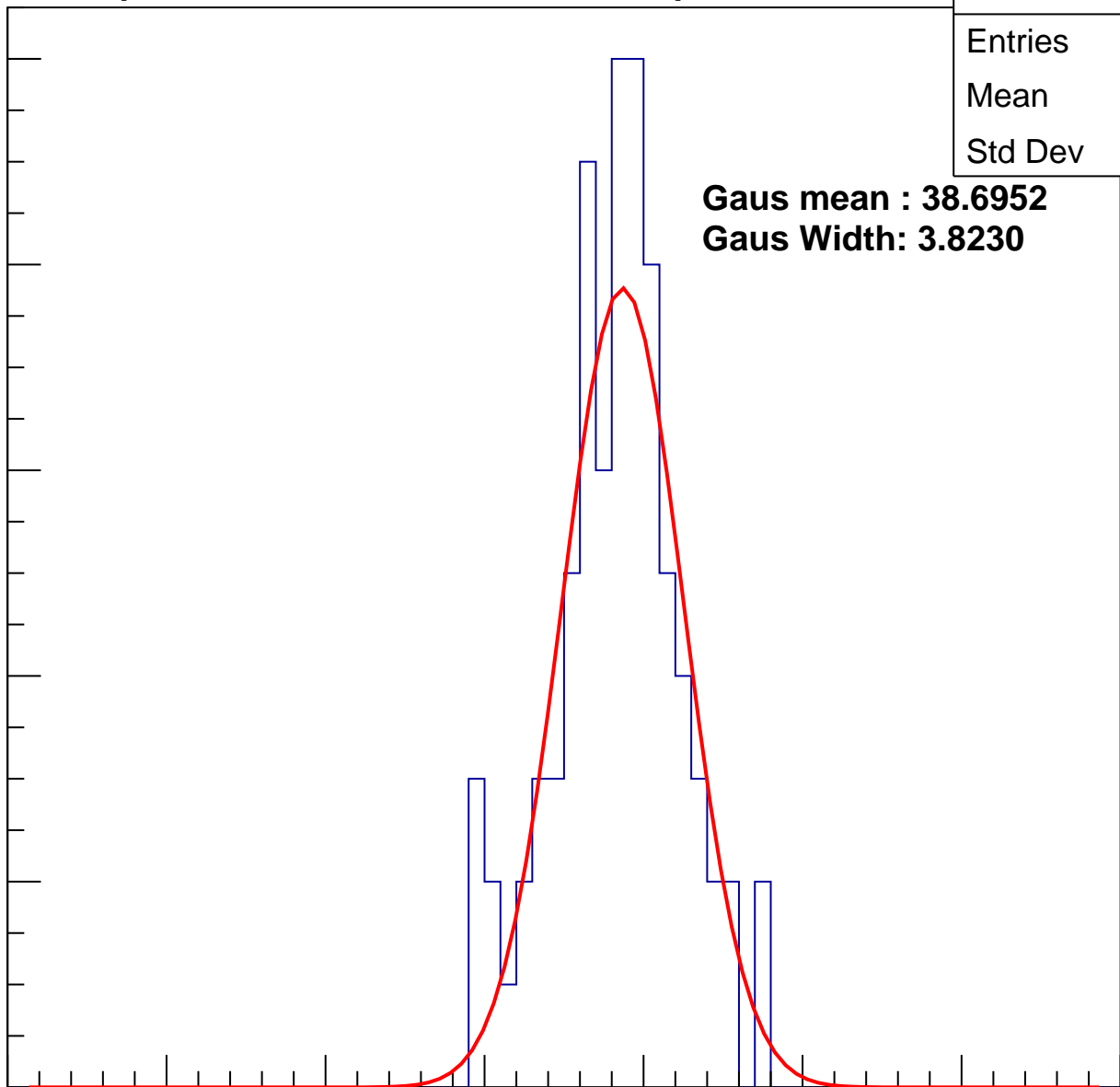
**Gaus Width: 3.8230**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U10-ch37, adc2

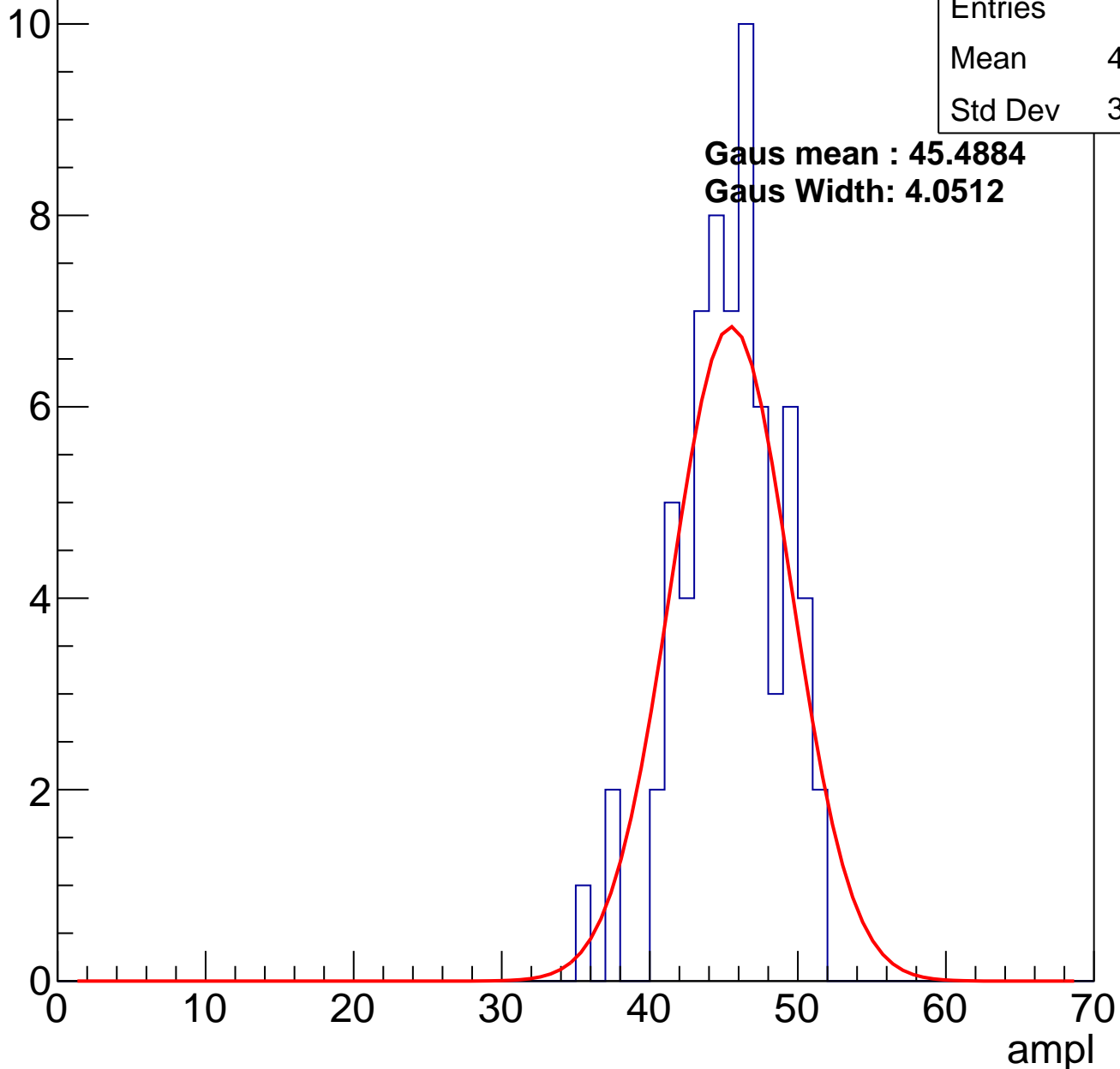
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	67
Mean	44.96
Std Dev	3.365

**Gaus mean : 45.4884**

**Gaus Width: 4.0512**

Entry

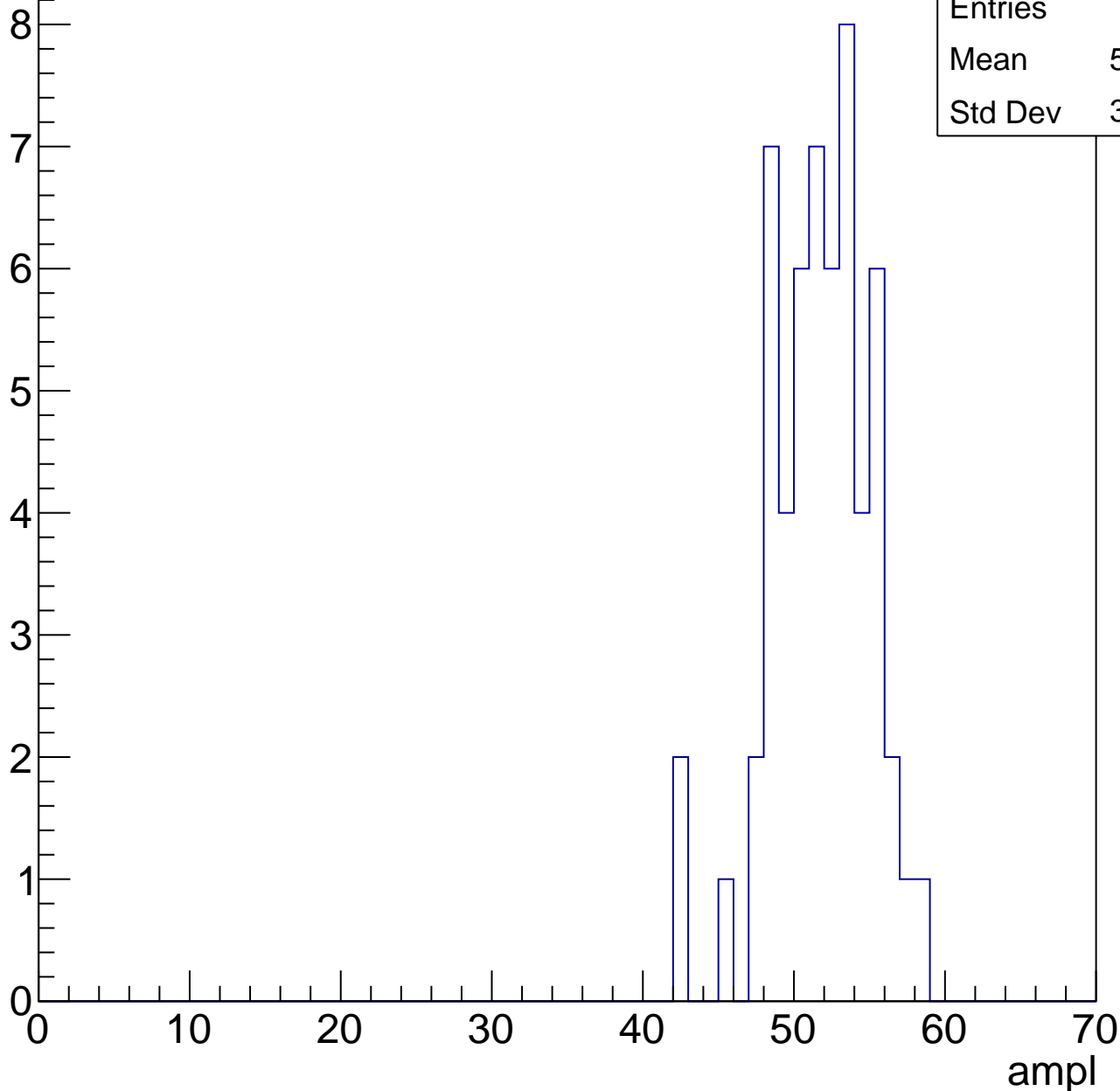


# B0L001S, U10-ch37, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	51.25
Std Dev	3.289



# B0L001S, U10-ch37, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	79
Mean	57.94
Std Dev	3.066

Entry

10

8

6

4

2

0

0

10

20

30

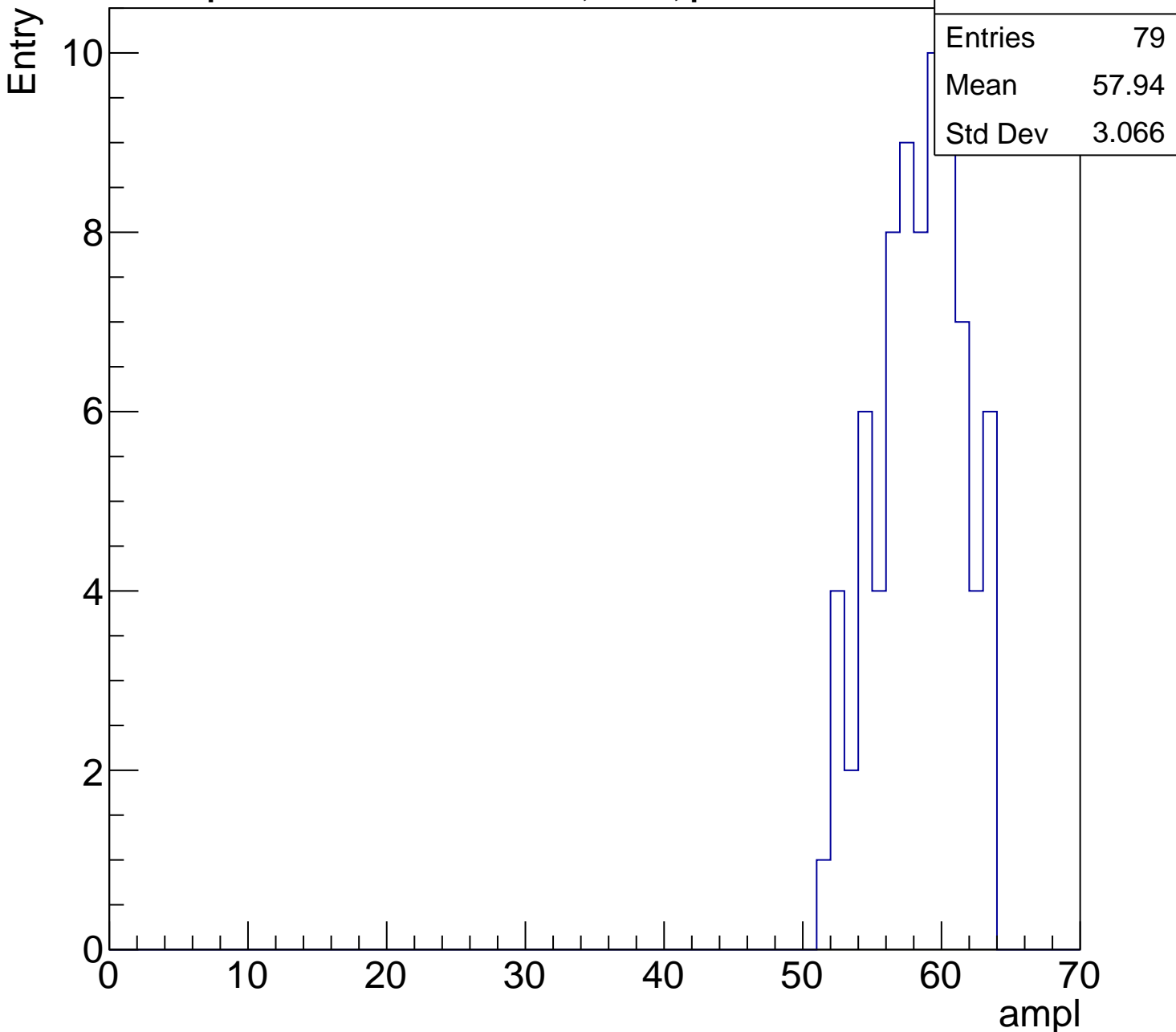
40

50

60

ampl

70

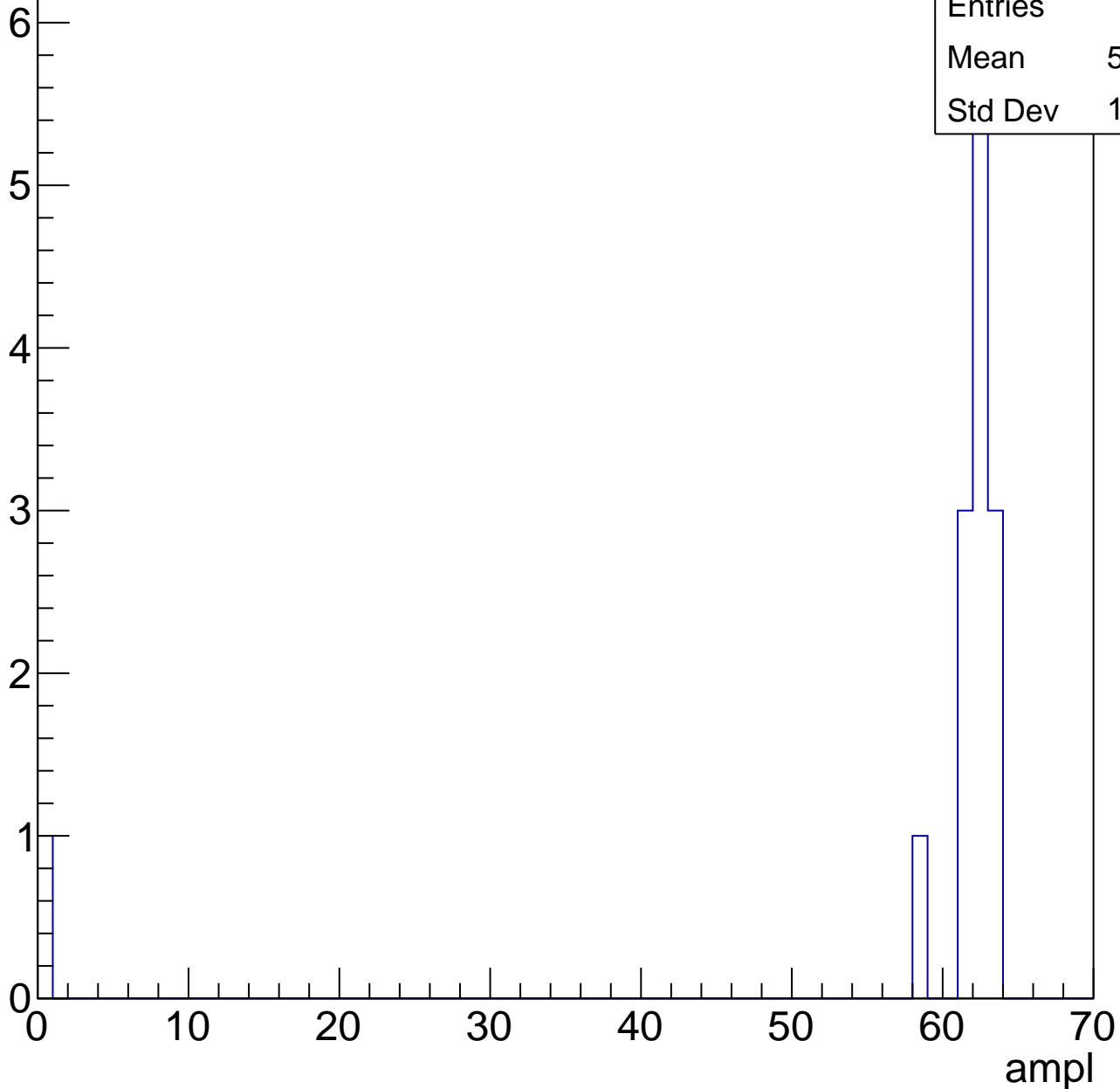


# B0L001S, U10-ch37, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	14
Mean	57.29
Std Dev	15.93



# B0L001S, U10-ch37, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch37, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U10-ch38, adc0

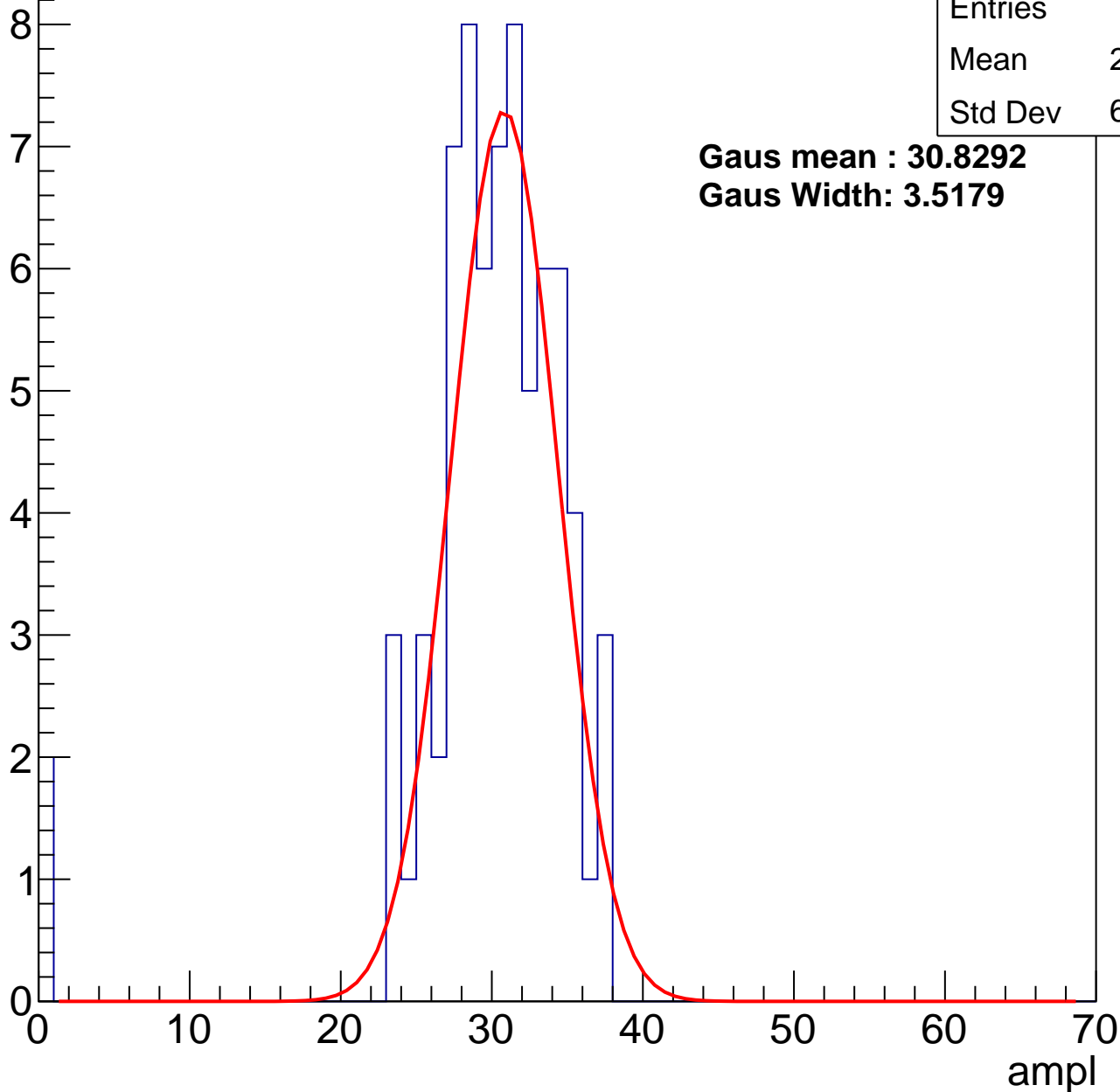
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	29.36
Std Dev	6.035

**Gaus mean : 30.8292**

**Gaus Width: 3.5179**



# B0L001S, U10-ch38, adc1

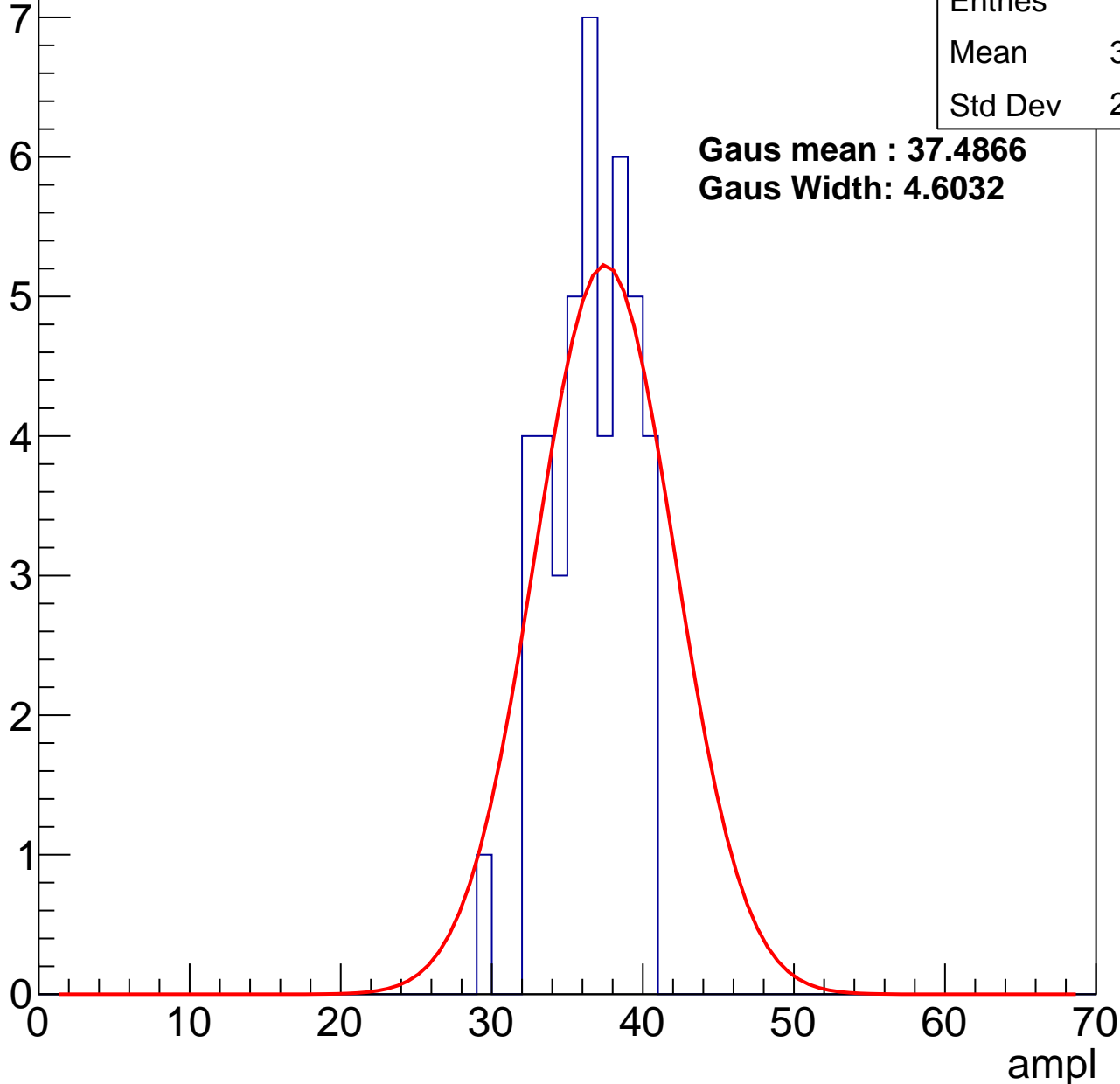
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	43
Mean	36.02
Std Dev	2.654

**Gaus mean : 37.4866**

**Gaus Width: 4.6032**



# B0L001S, U10-ch38, adc2

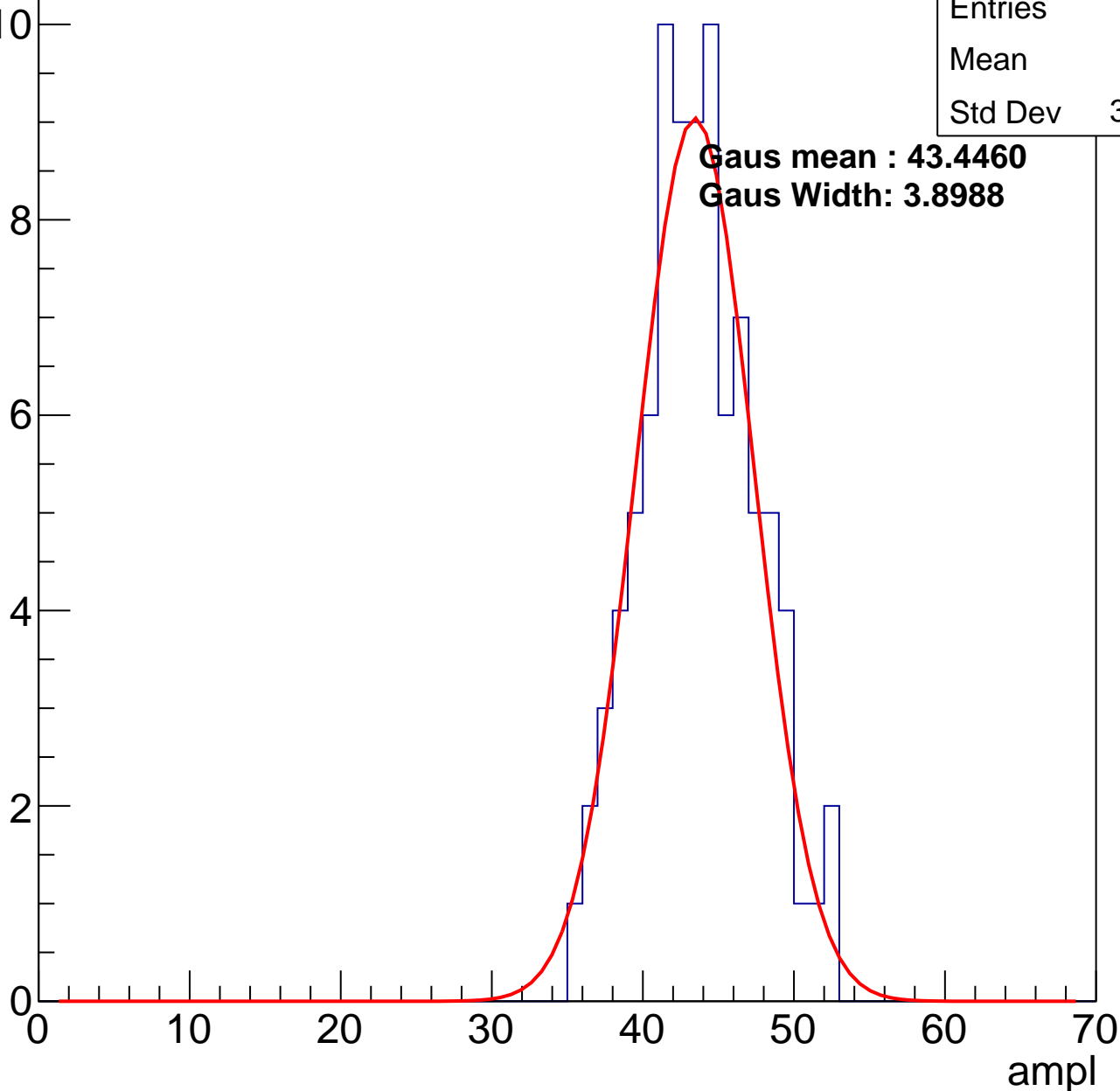
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	90
Mean	43.2
Std Dev	3.757

**Gaus mean : 43.4460**

**Gaus Width: 3.8988**

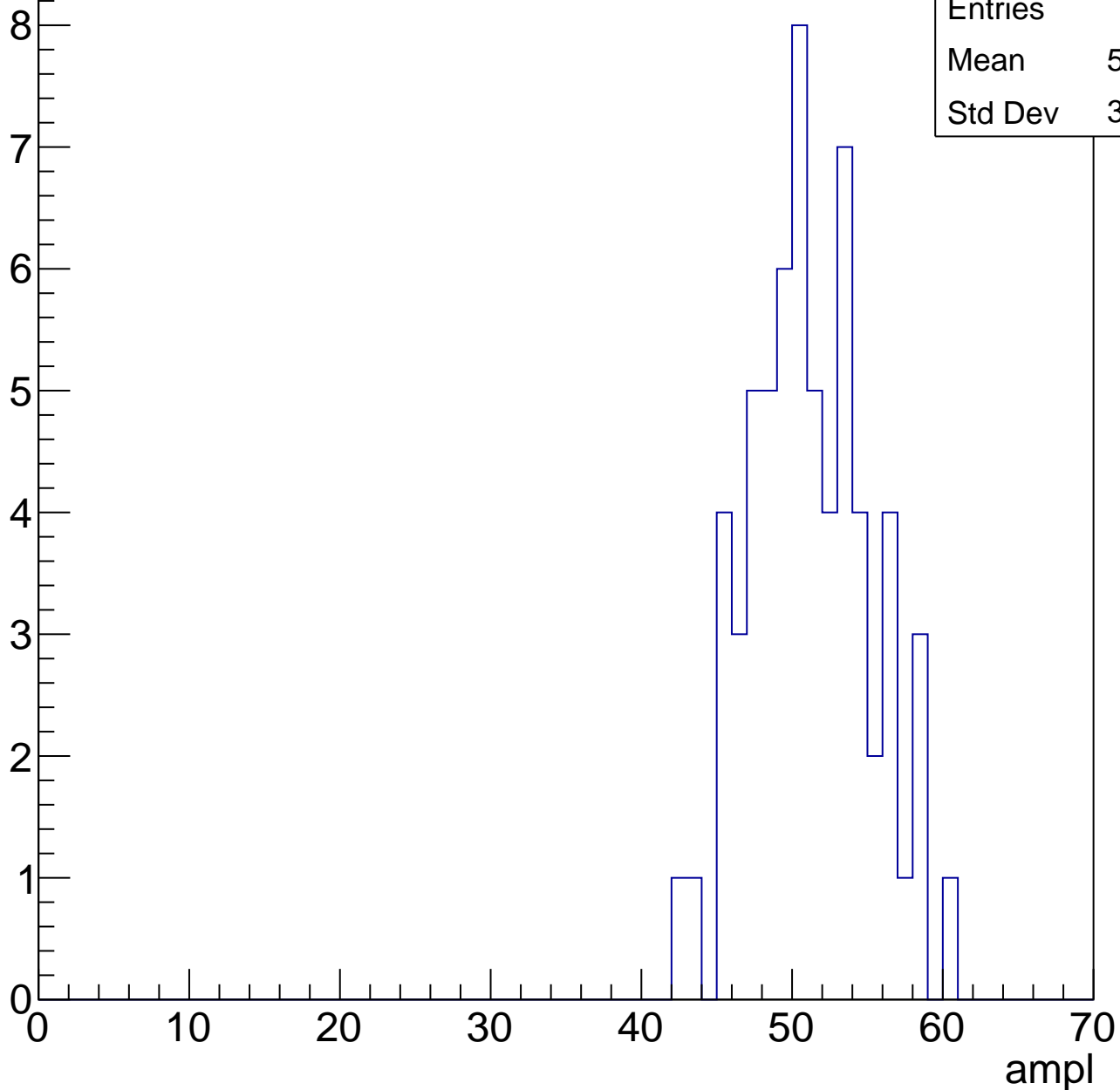


# B0L001S, U10-ch38, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	50.73
Std Dev	3.914

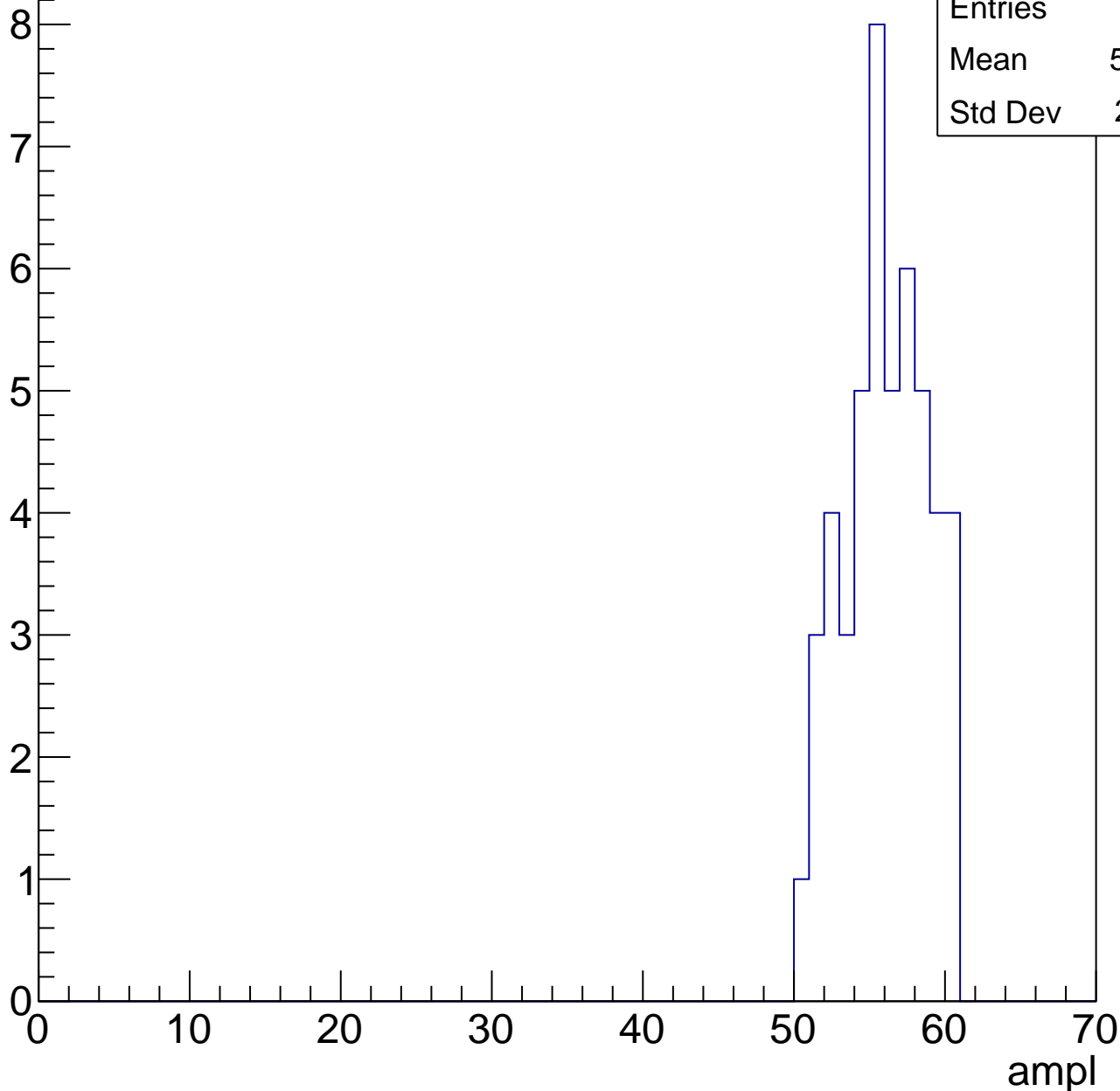


# B0L001S, U10-ch38, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	48
Mean	55.58
Std Dev	2.691

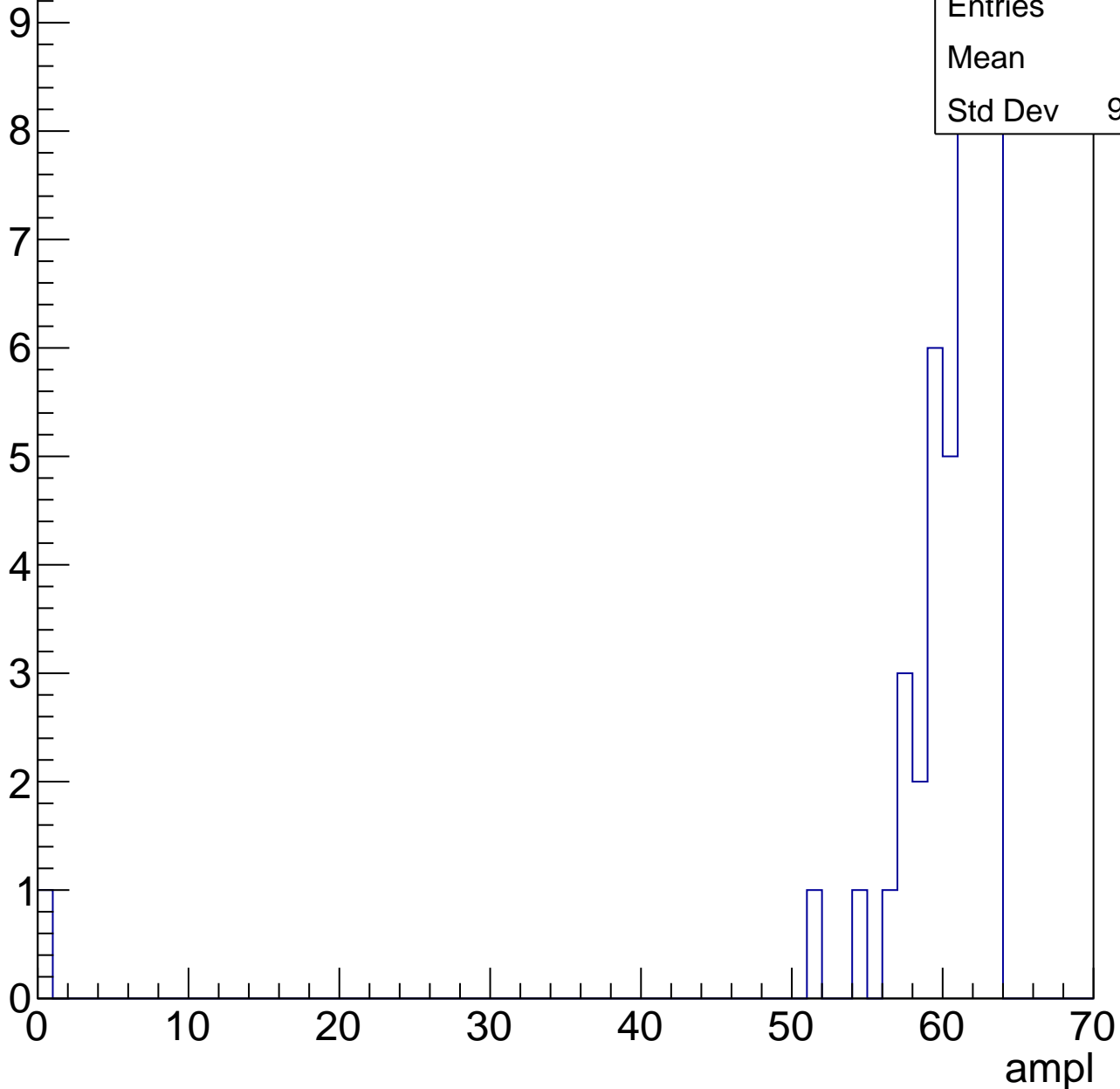


# B0L001S, U10-ch38, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	46
Mean	59
Std Dev	9.149



# B0L001S, U10-ch38, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch38, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U10-ch39, adc0

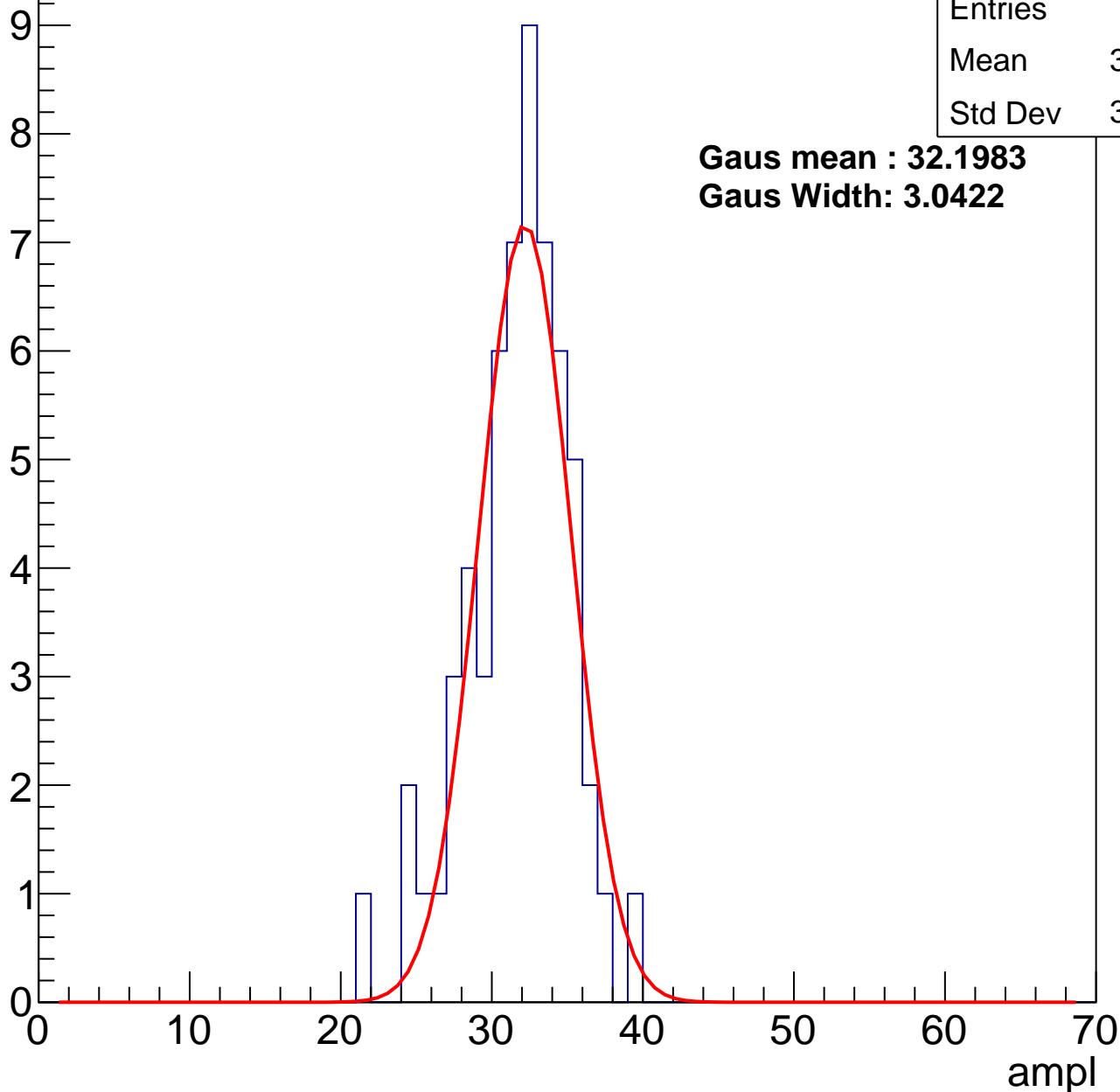
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	31.24
Std Dev	3.392

**Gaus mean : 32.1983**

**Gaus Width: 3.0422**

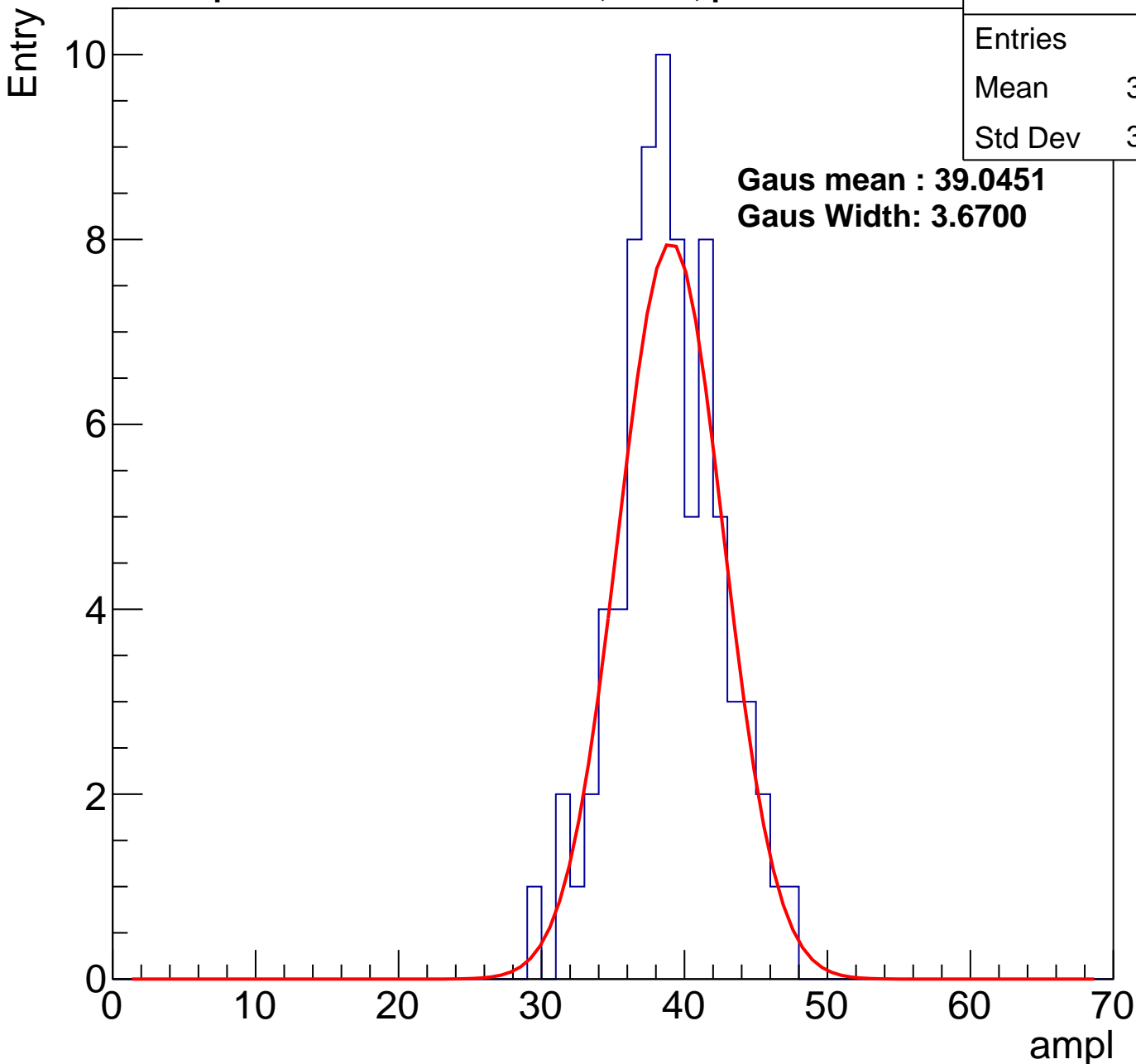


# B0L001S, U10-ch39, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	77
Mean	38.44
Std Dev	3.598

**Gaus mean : 39.0451**  
**Gaus Width: 3.6700**



# B0L001S, U10-ch39, adc2

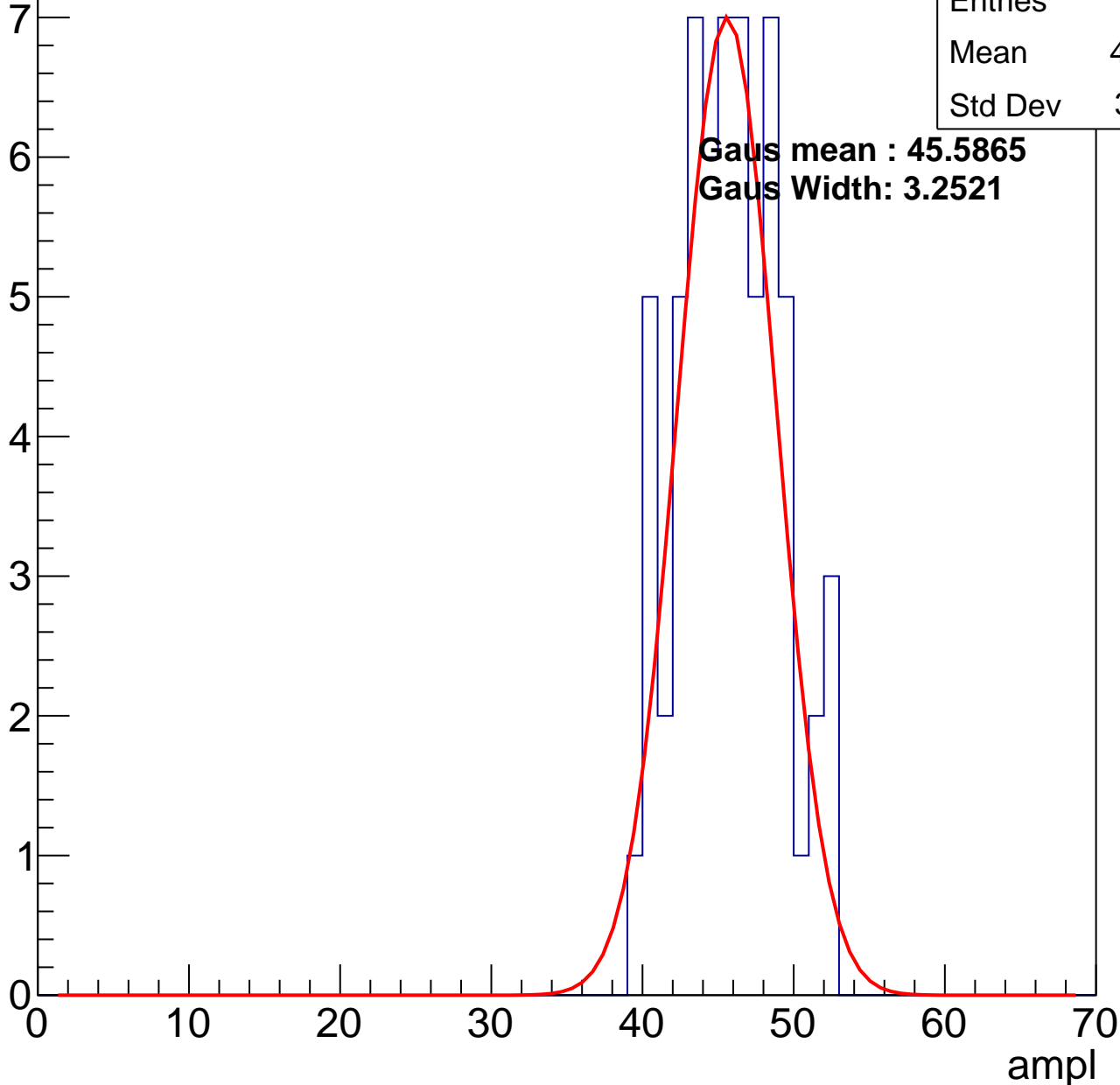
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	45.35
Std Dev	3.281

**Gaus mean : 45.5865**

**Gaus Width: 3.2521**

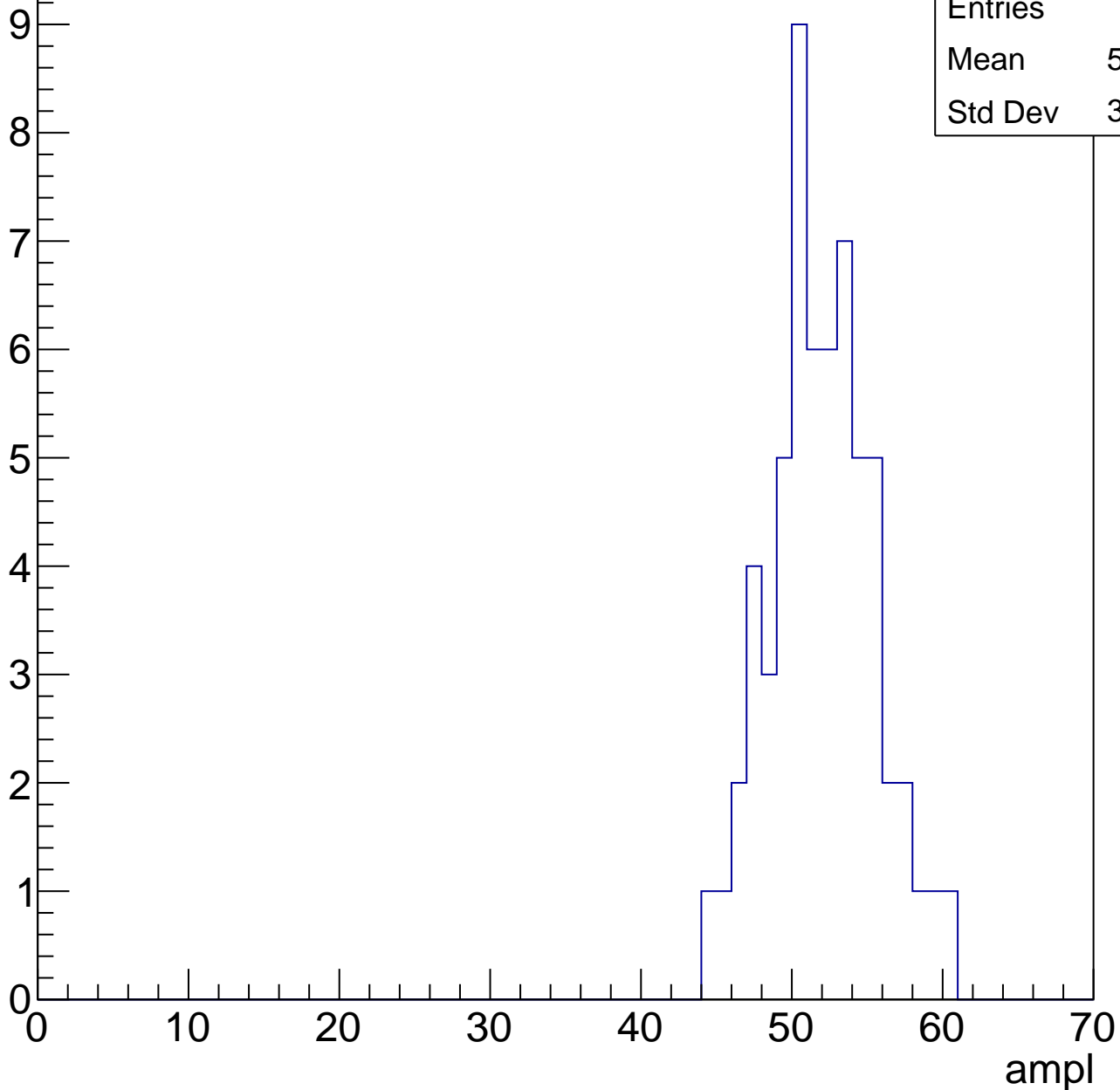


# B0L001S, U10-ch39, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	51.56
Std Dev	3.414

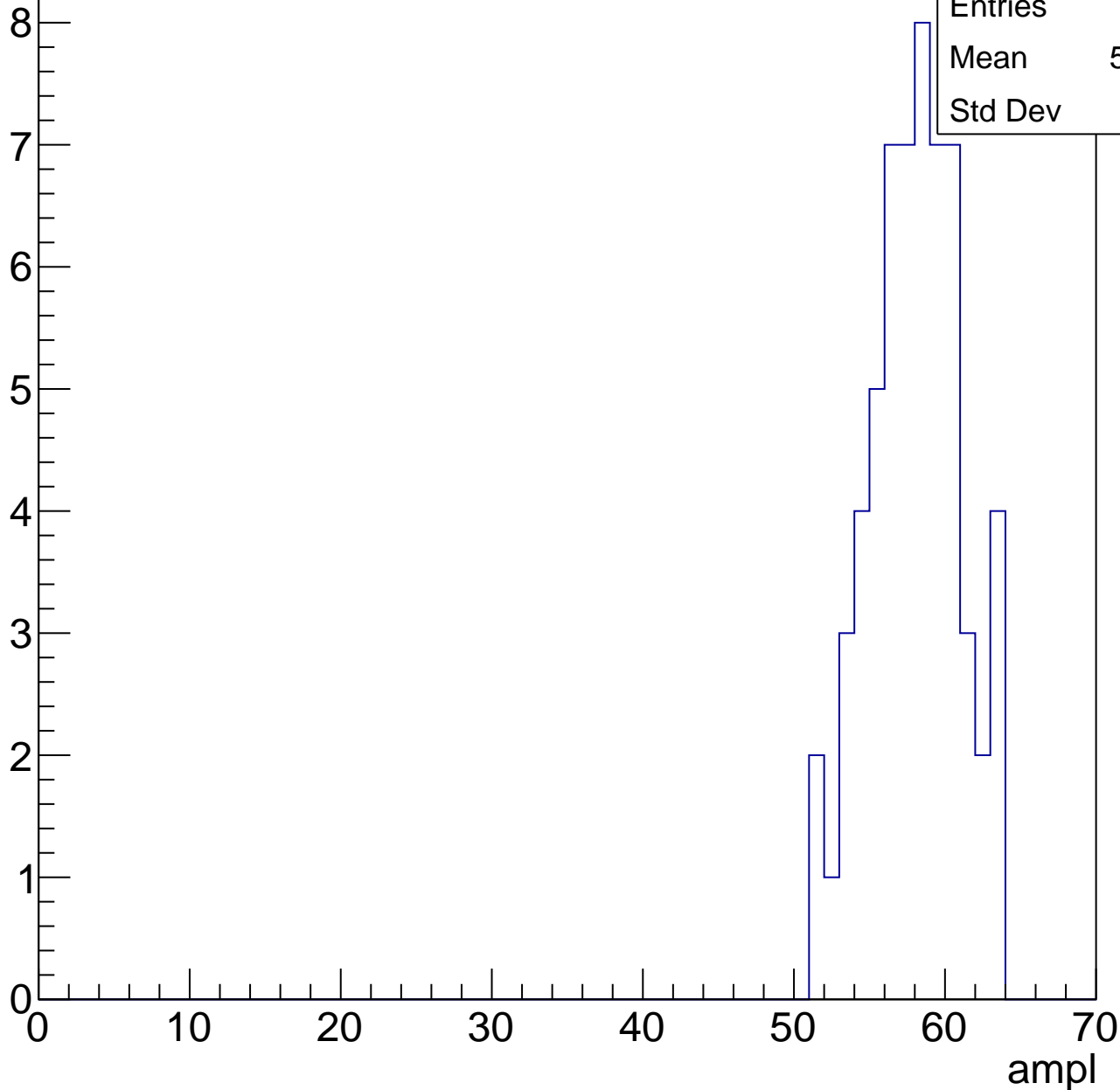


# B0L001S, U10-ch39, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	57.52
Std Dev	2.98

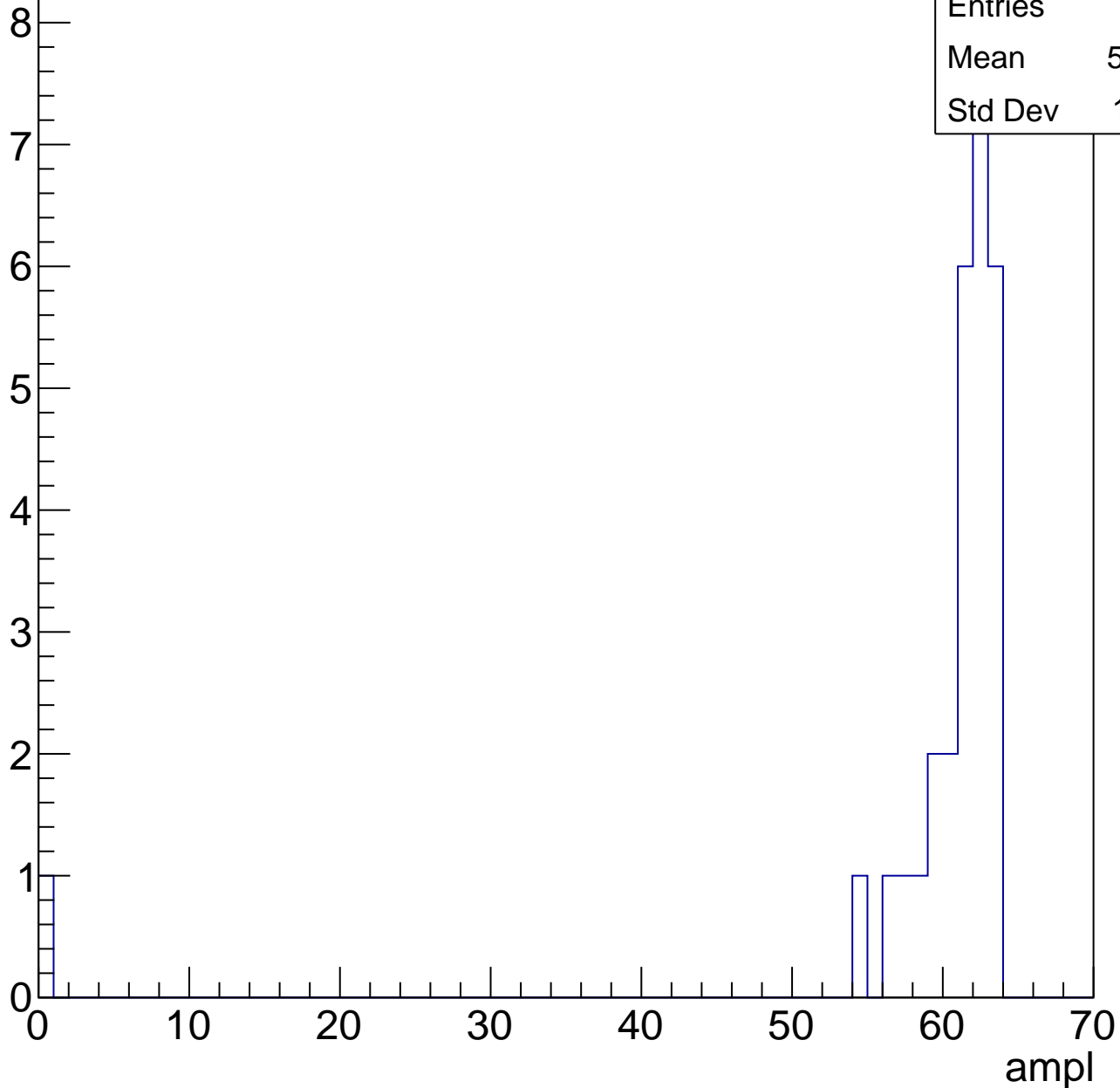


# B0L001S, U10-ch39, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	29
Mean	58.72
Std Dev	11.31



# B0L001S, U10-ch39, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch39, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U10-ch40, adc0

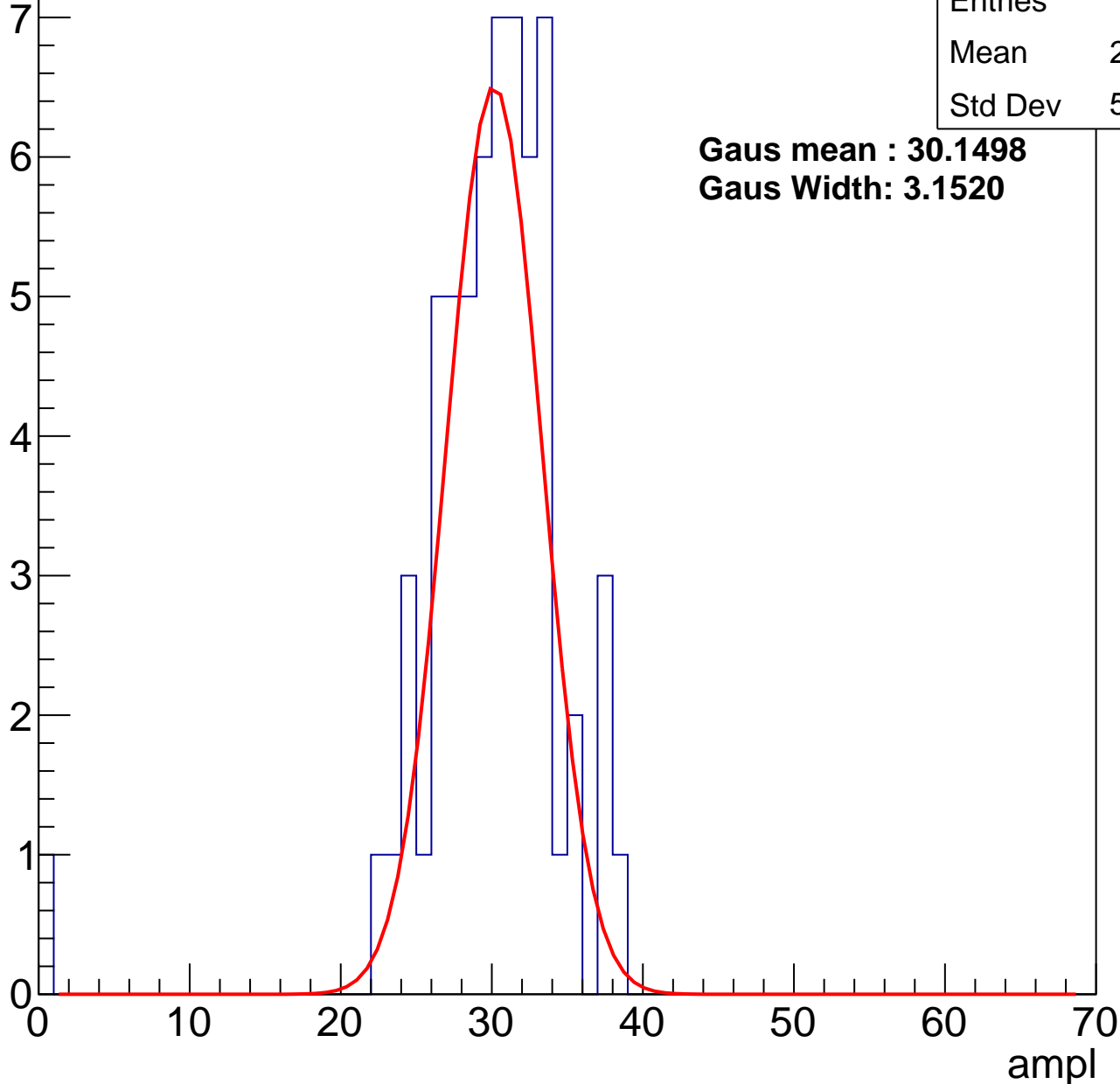
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	29.42
Std Dev	5.154

**Gaus mean : 30.1498**

**Gaus Width: 3.1520**



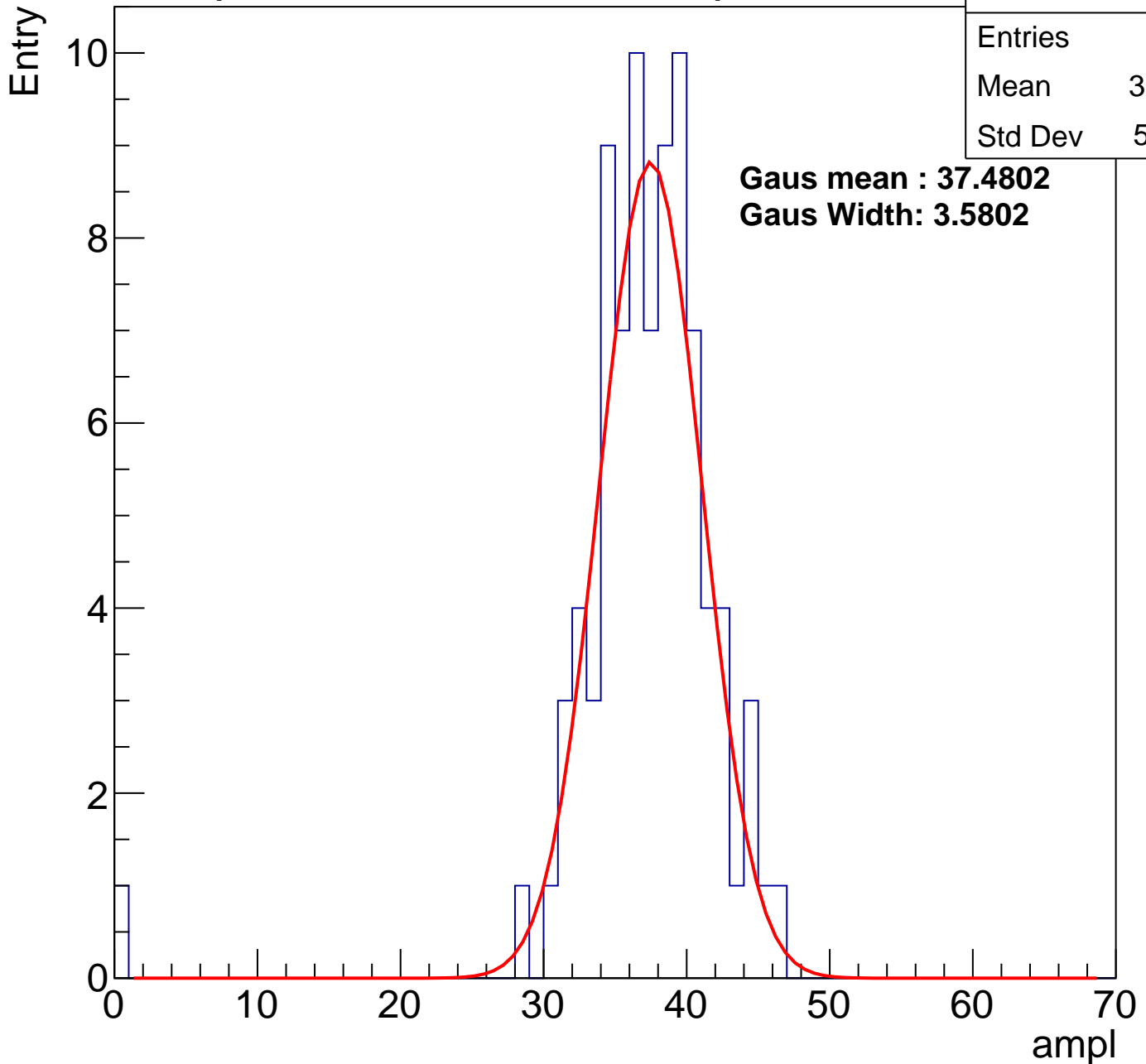
# B0L001S, U10-ch40, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	86
Mean	36.72
Std Dev	5.361

**Gaus mean : 37.4802**

**Gaus Width: 3.5802**



# B0L001S, U10-ch40, adc2

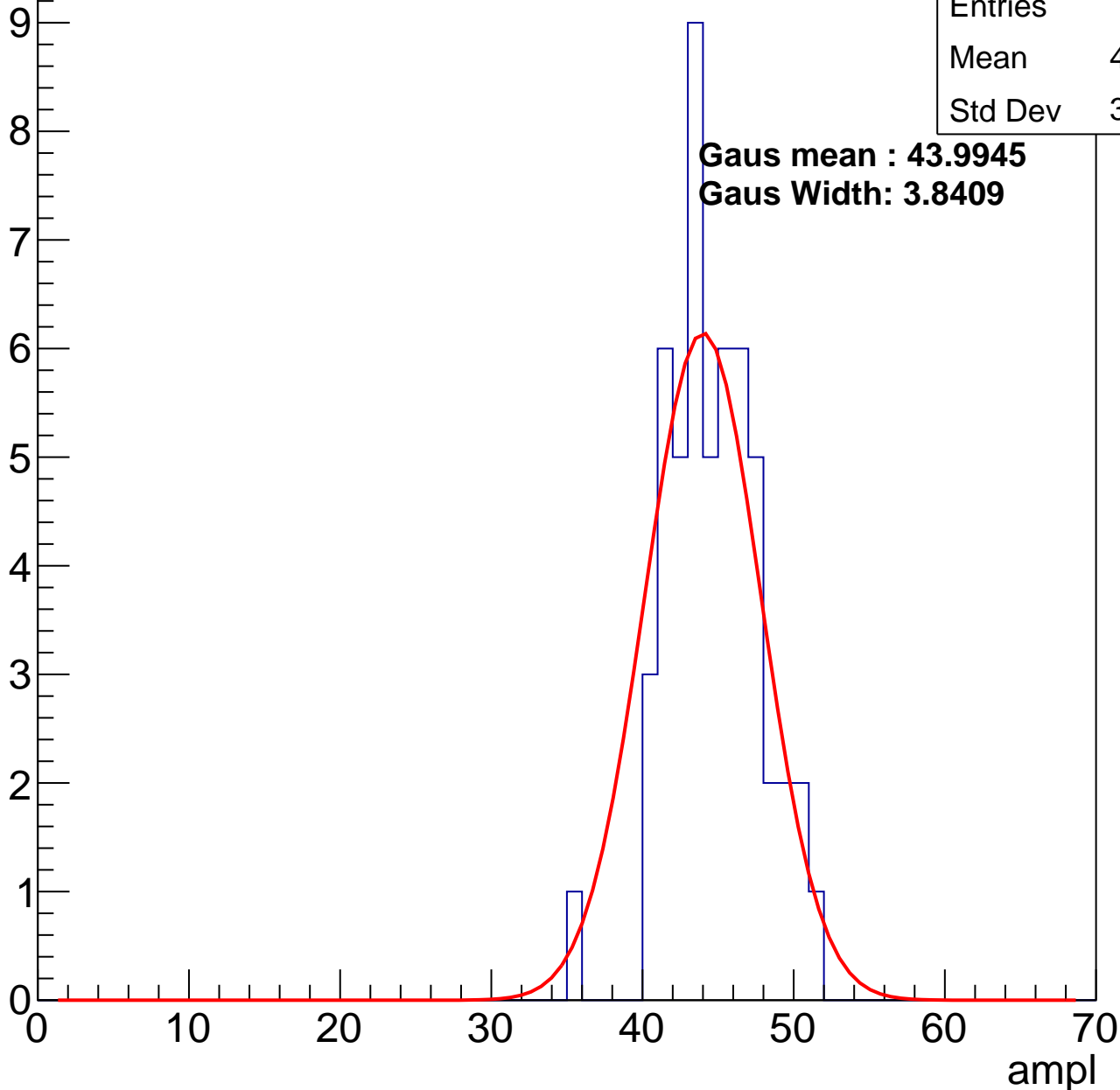
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	44.23
Std Dev	3.032

**Gaus mean : 43.9945**

**Gaus Width: 3.8409**

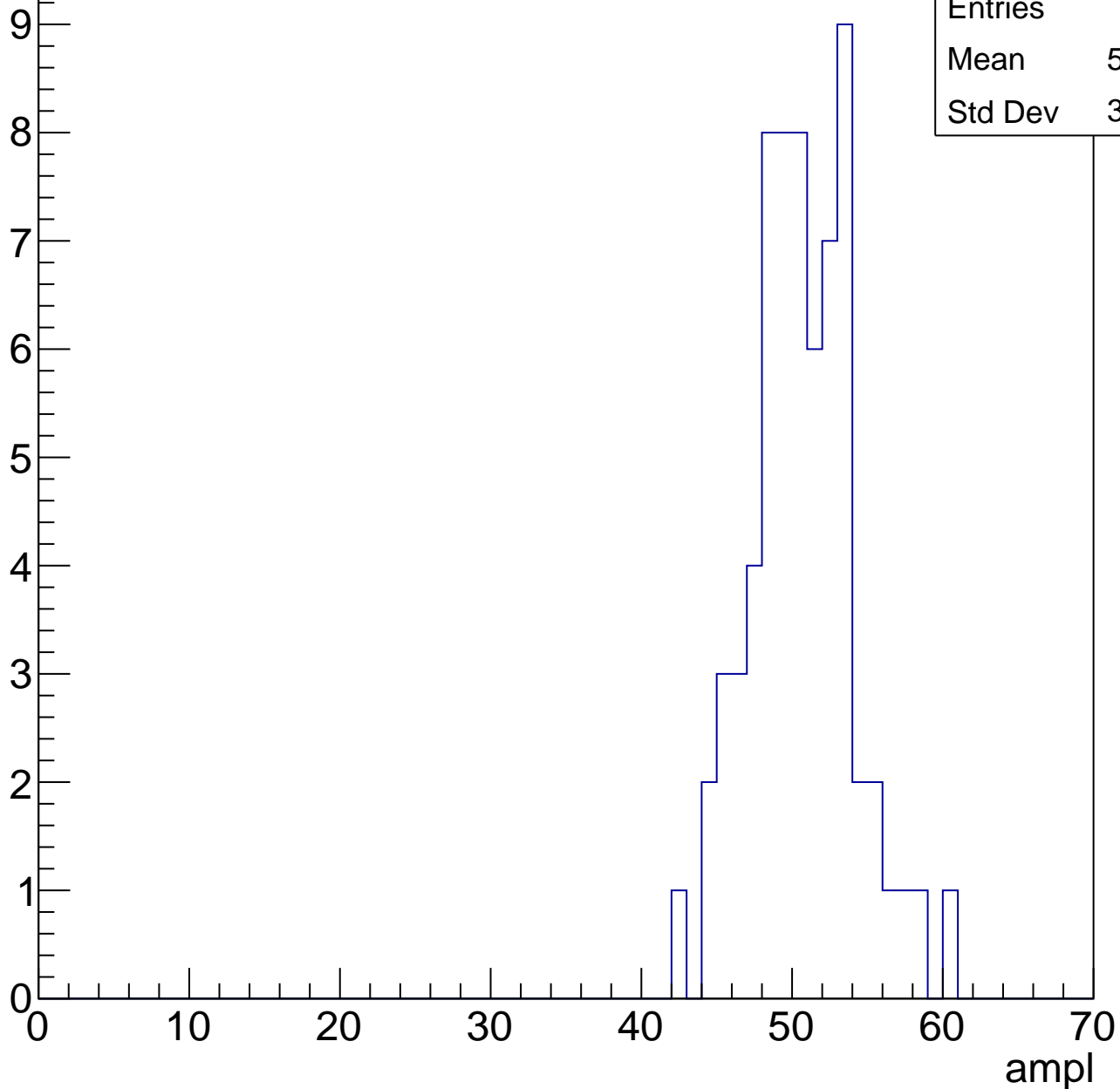


# B0L001S, U10-ch40, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	50.19
Std Dev	3.409

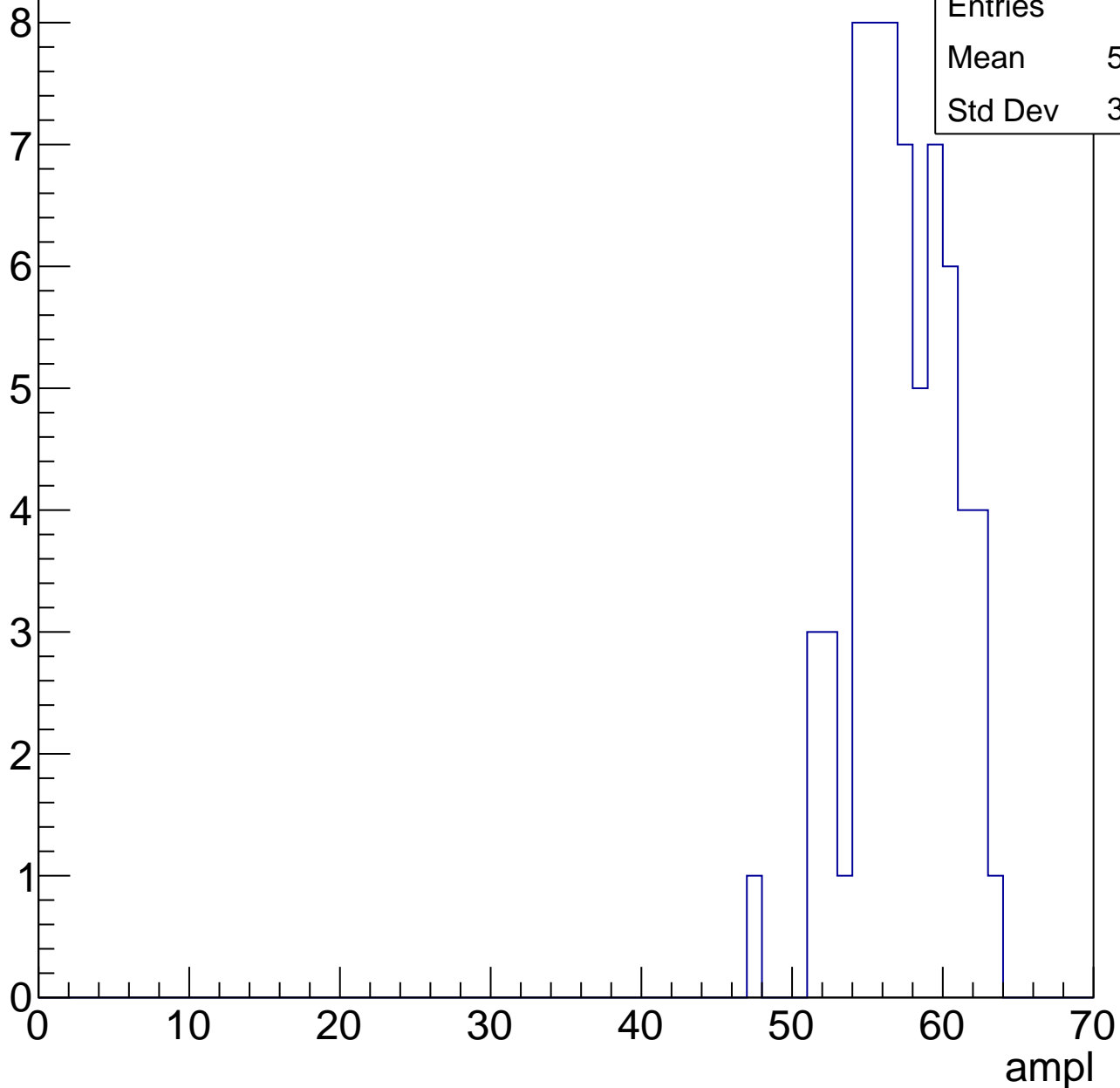


# B0L001S, U10-ch40, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	56.76
Std Dev	3.243

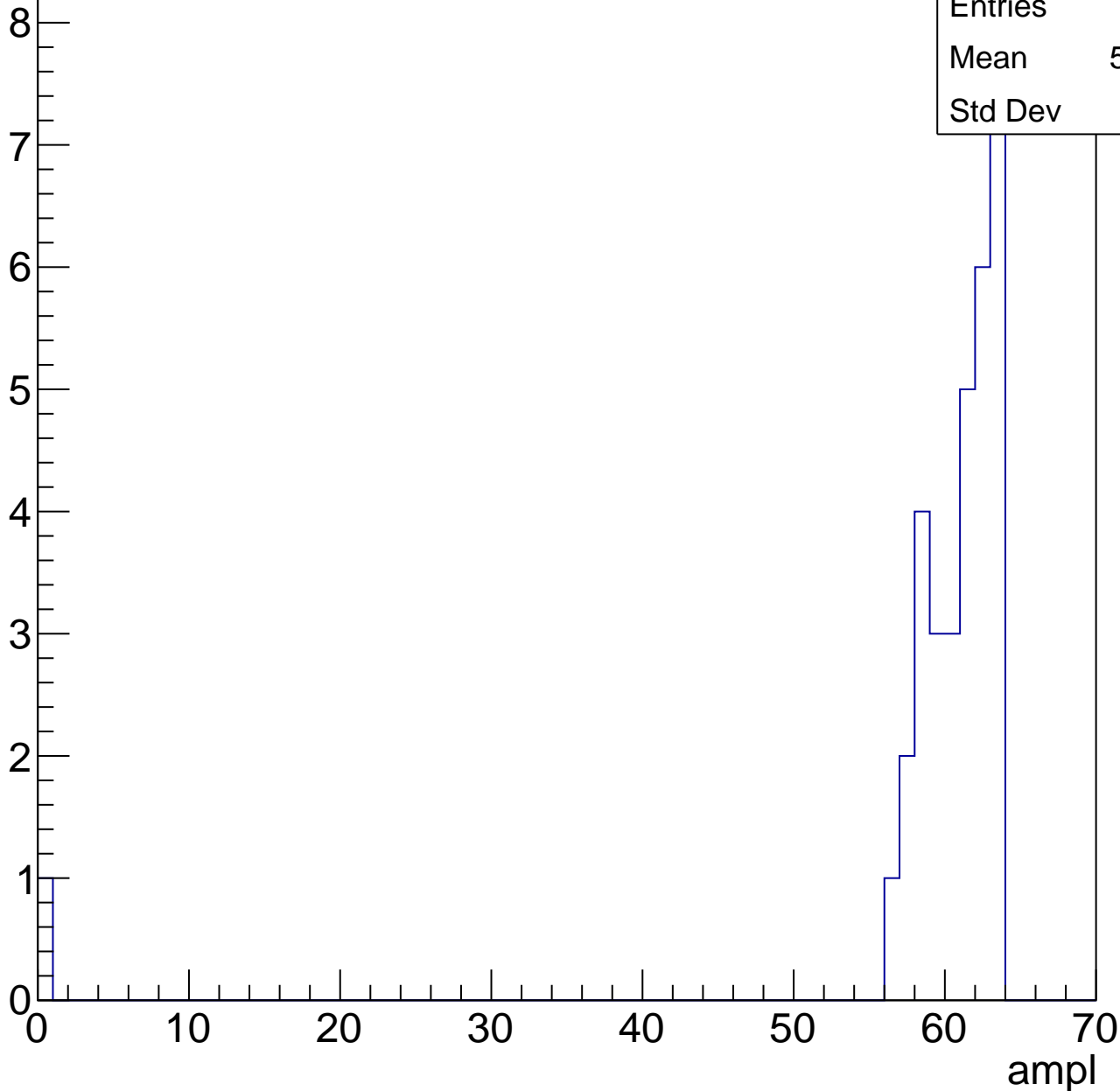


# B0L001S, U10-ch40, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	33
Mean	58.79
Std Dev	10.6



# B0L001S, U10-ch40, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch40, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U10-ch41, adc0

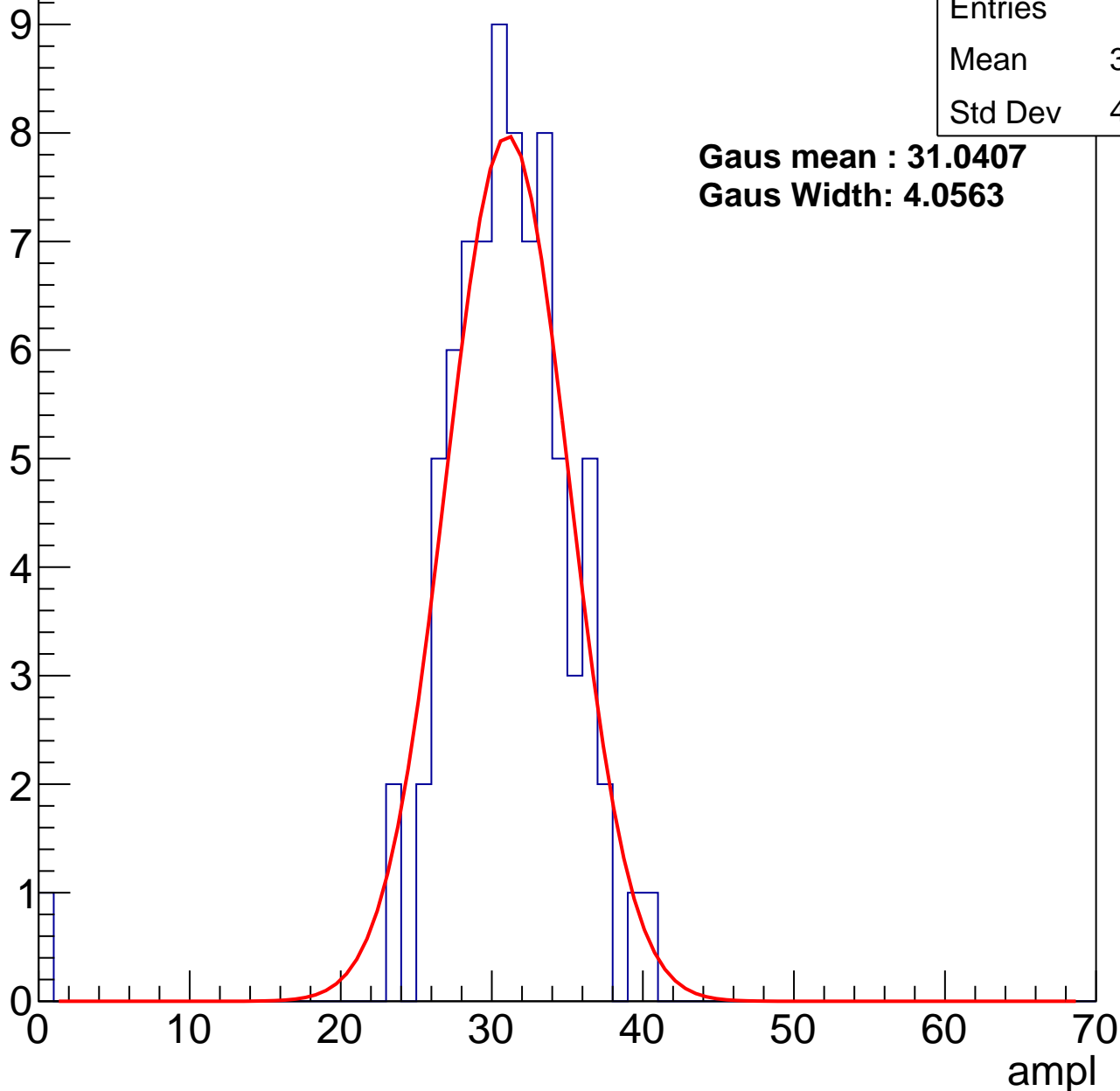
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	79
Mean	30.39
Std Dev	4.939

**Gaus mean : 31.0407**

**Gaus Width: 4.0563**



# B0L001S, U10-ch41, adc1

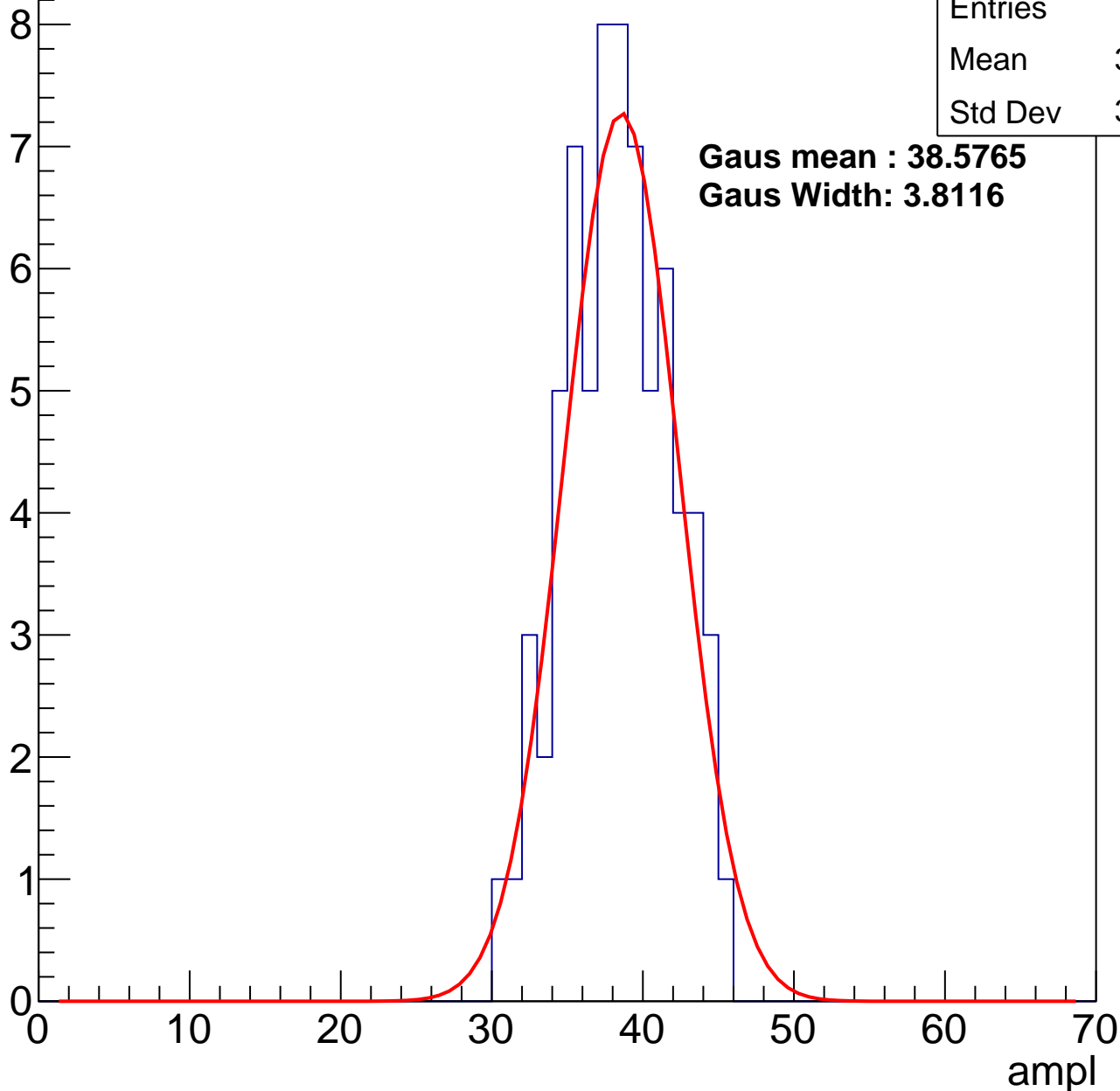
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	37.91
Std Dev	3.471

**Gaus mean : 38.5765**

**Gaus Width: 3.8116**



# B0L001S, U10-ch41, adc2

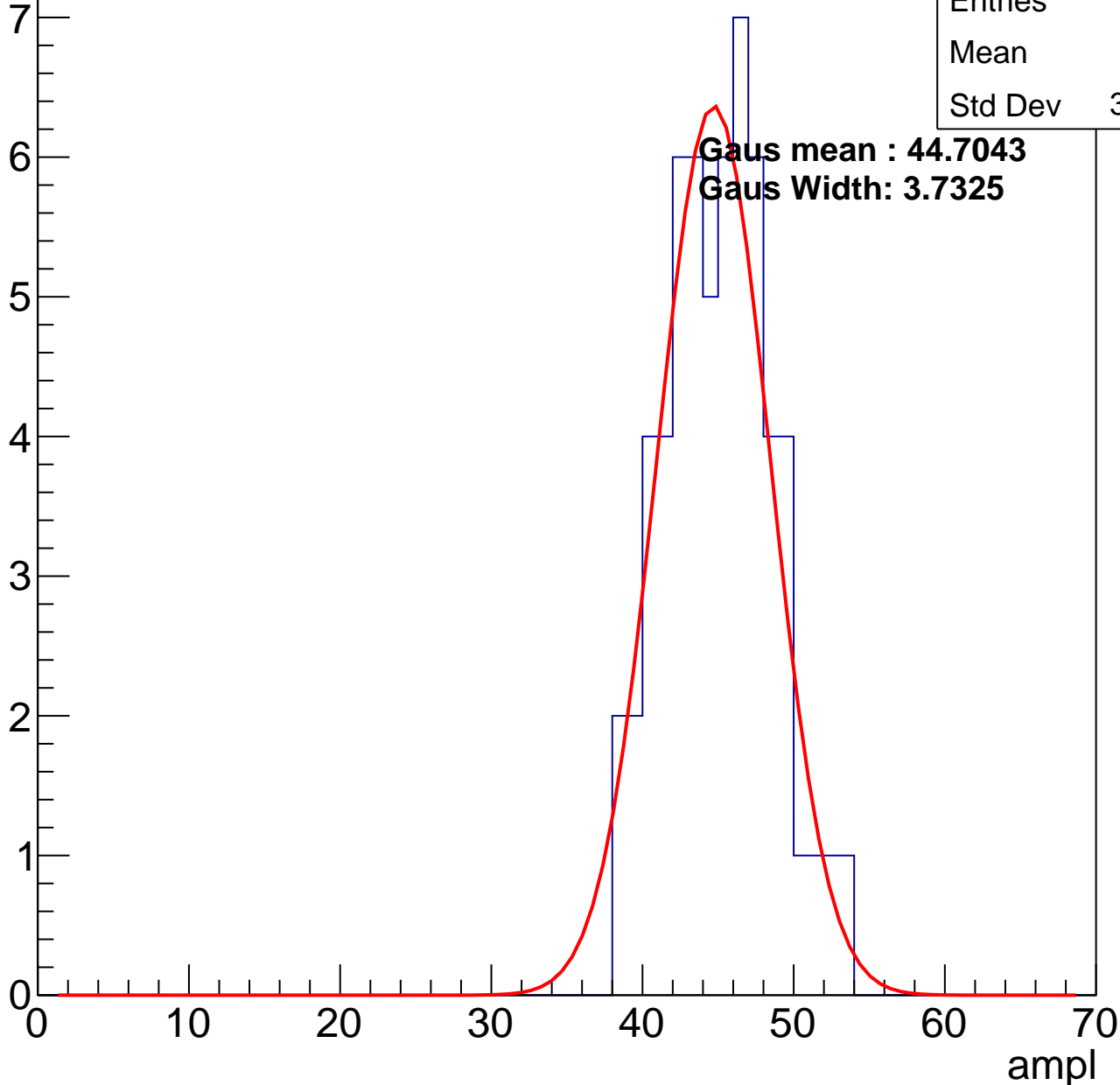
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	44.6
Std Dev	3.446

**Gaus mean : 44.7043**

**Gaus Width: 3.7325**

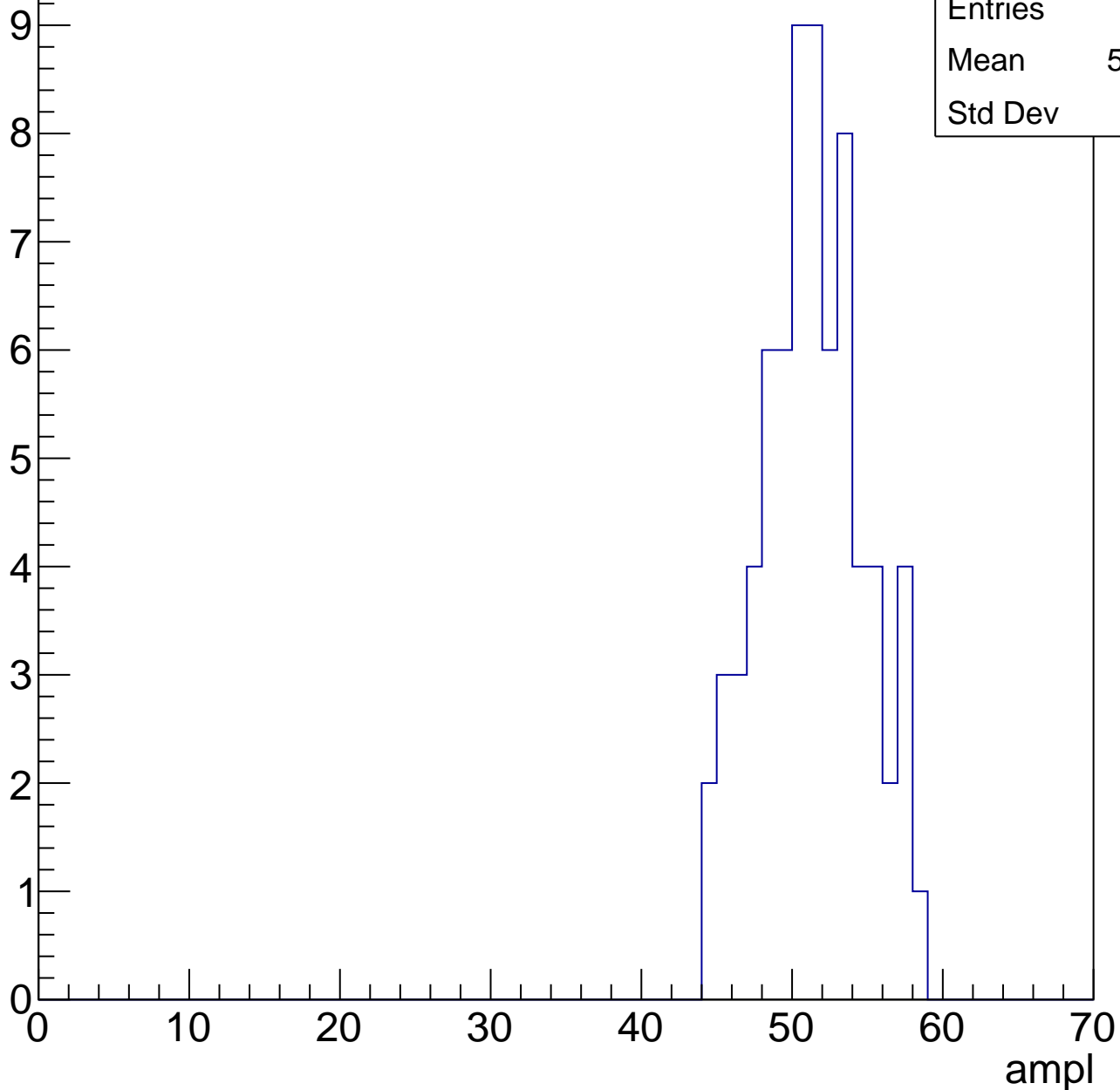


# B0L001S, U10-ch41, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	50.85
Std Dev	3.38

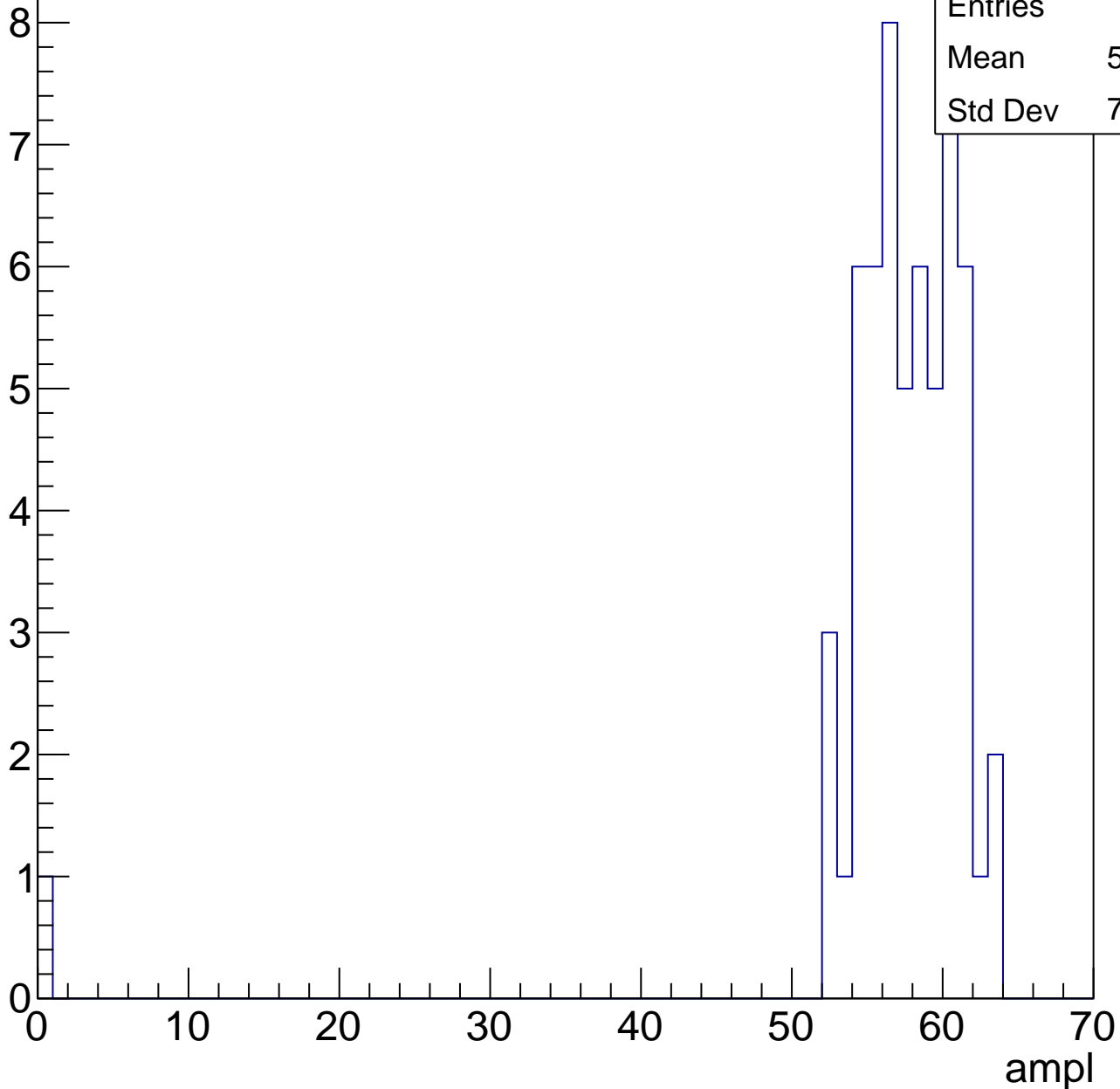


# B0L001S, U10-ch41, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	56.43
Std Dev	7.985

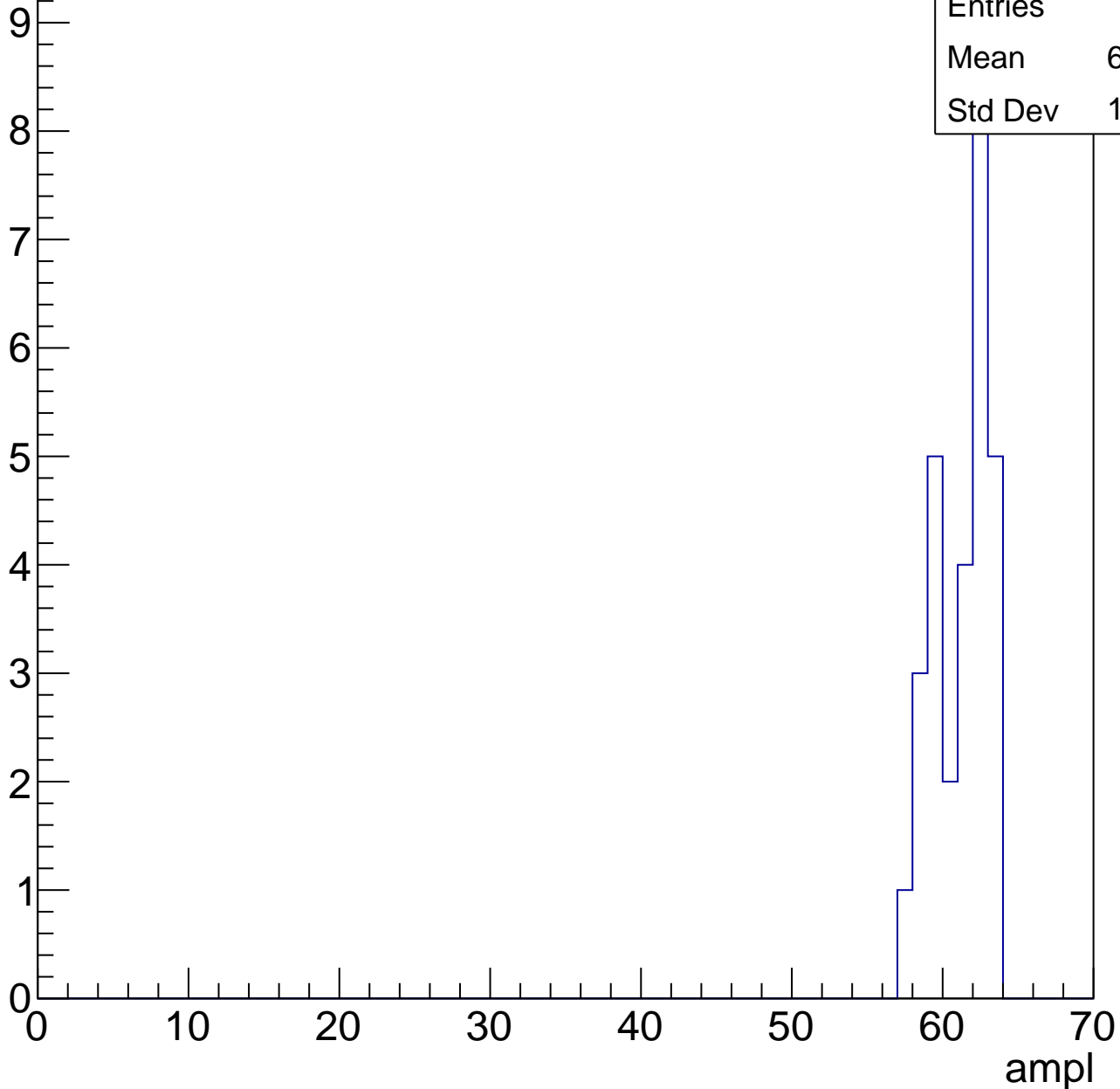


# B0L001S, U10-ch41, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	29
Mean	60.79
Std Dev	1.788



# B0L001S, U10-ch41, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch41, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U10-ch42, adc0

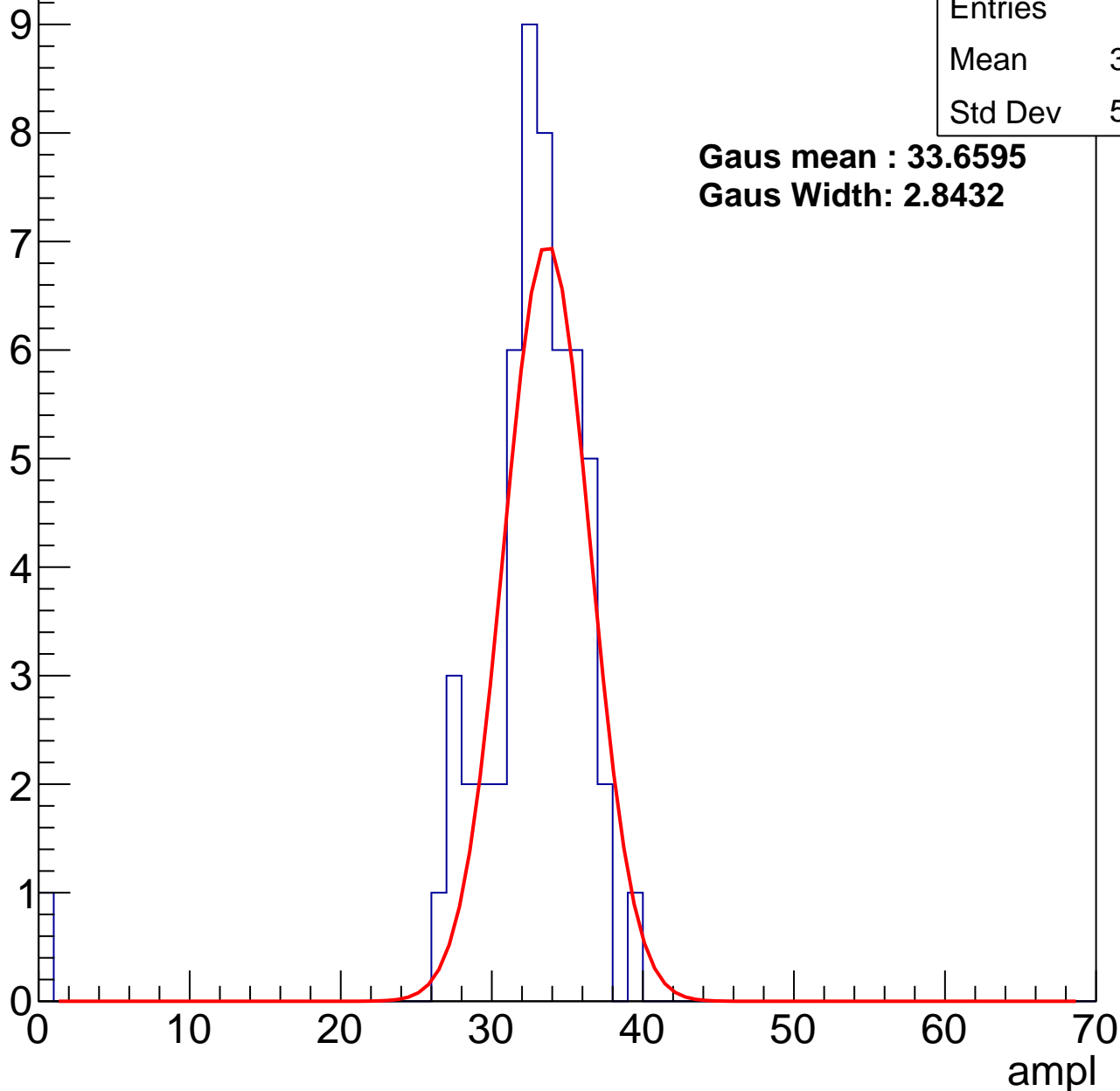
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	31.96
Std Dev	5.207

**Gaus mean : 33.6595**

**Gaus Width: 2.8432**



# B0L001S, U10-ch42, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	64
Mean	38.7
Std Dev	3.239

**Gaus mean : 38.6630**

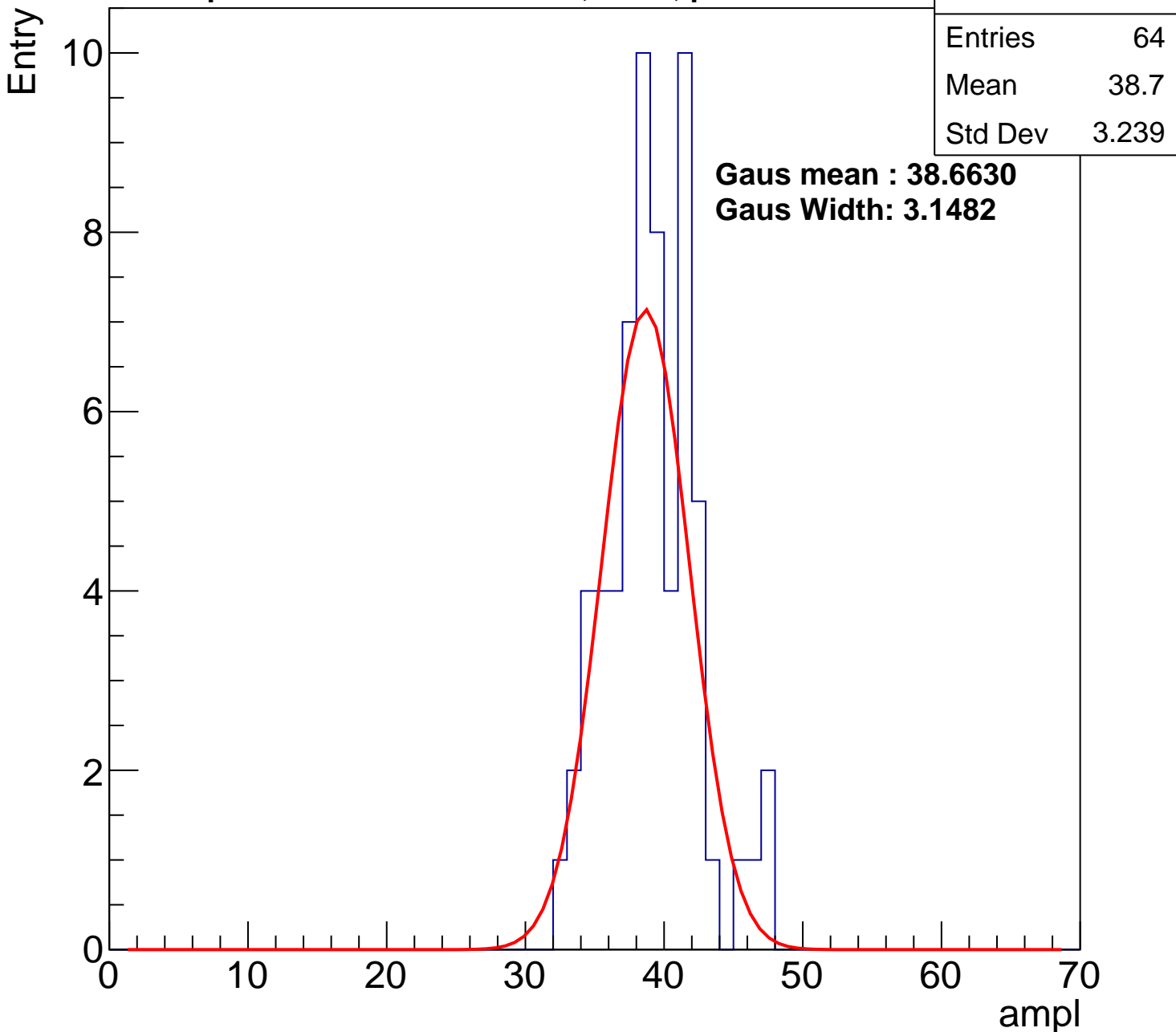
**Gaus Width: 3.1482**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U10-ch42, adc2

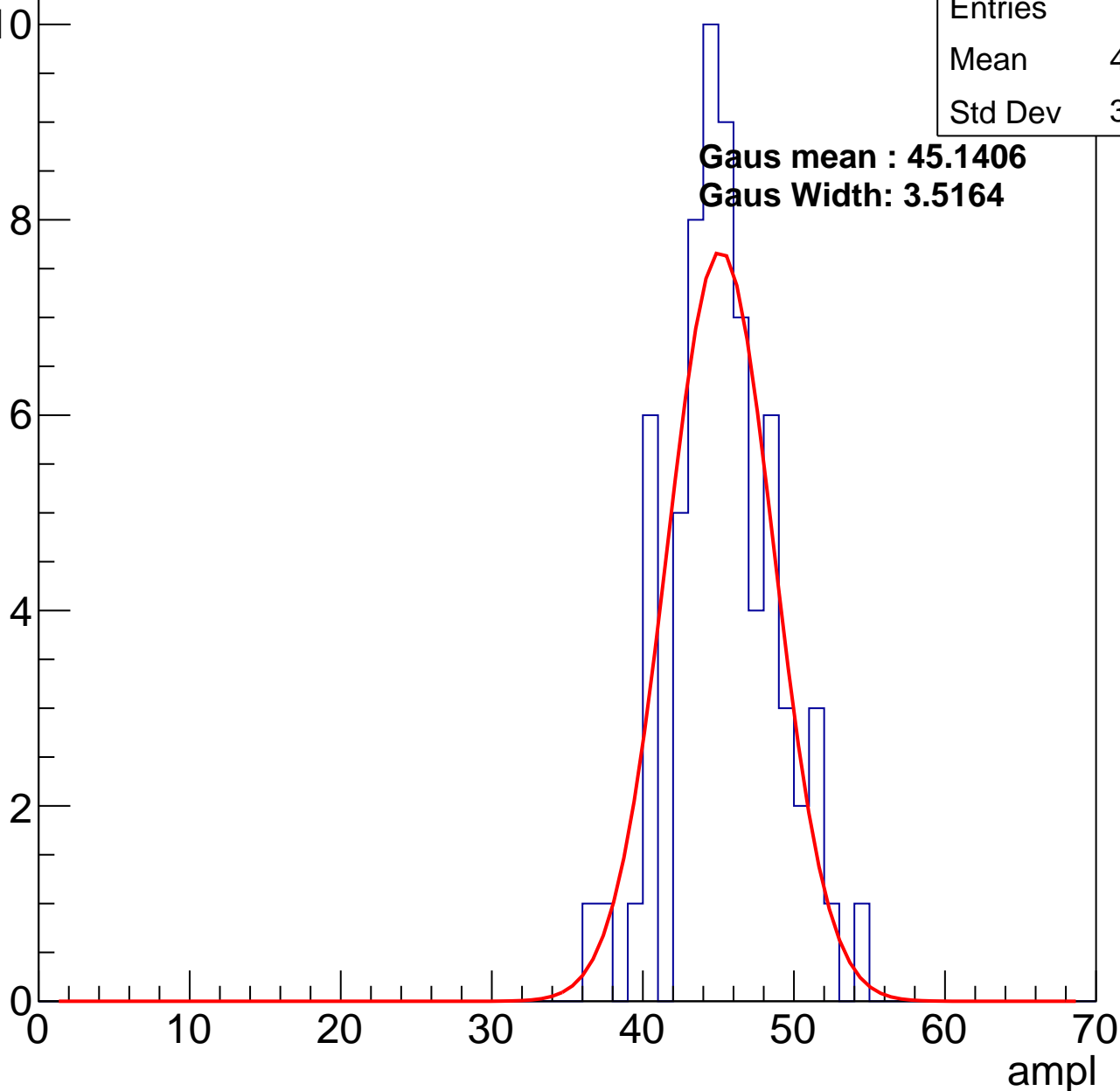
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	44.93
Std Dev	3.495

**Gaus mean : 45.1406**

**Gaus Width: 3.5164**

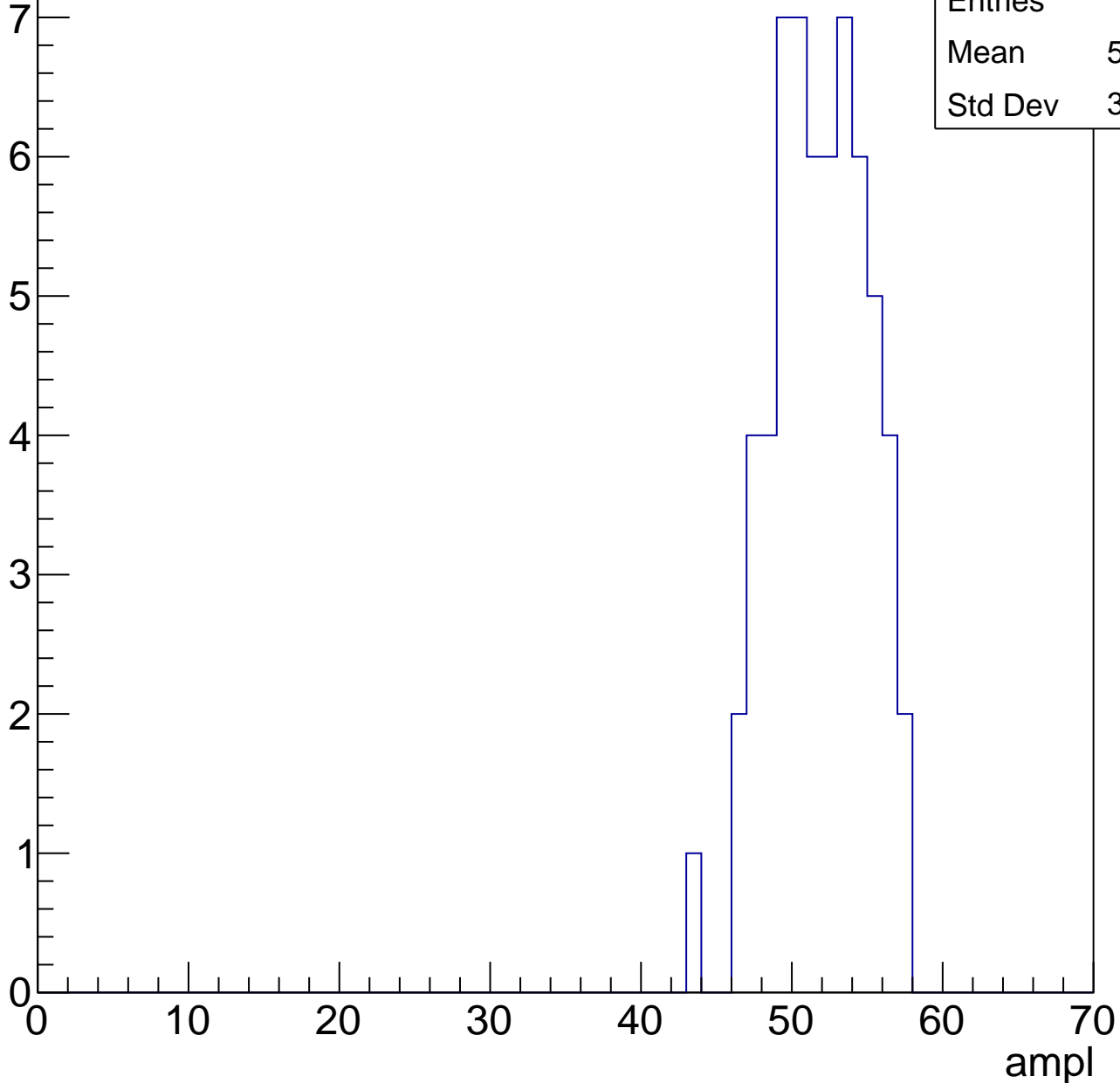


# B0L001S, U10-ch42, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	51.38
Std Dev	3.084

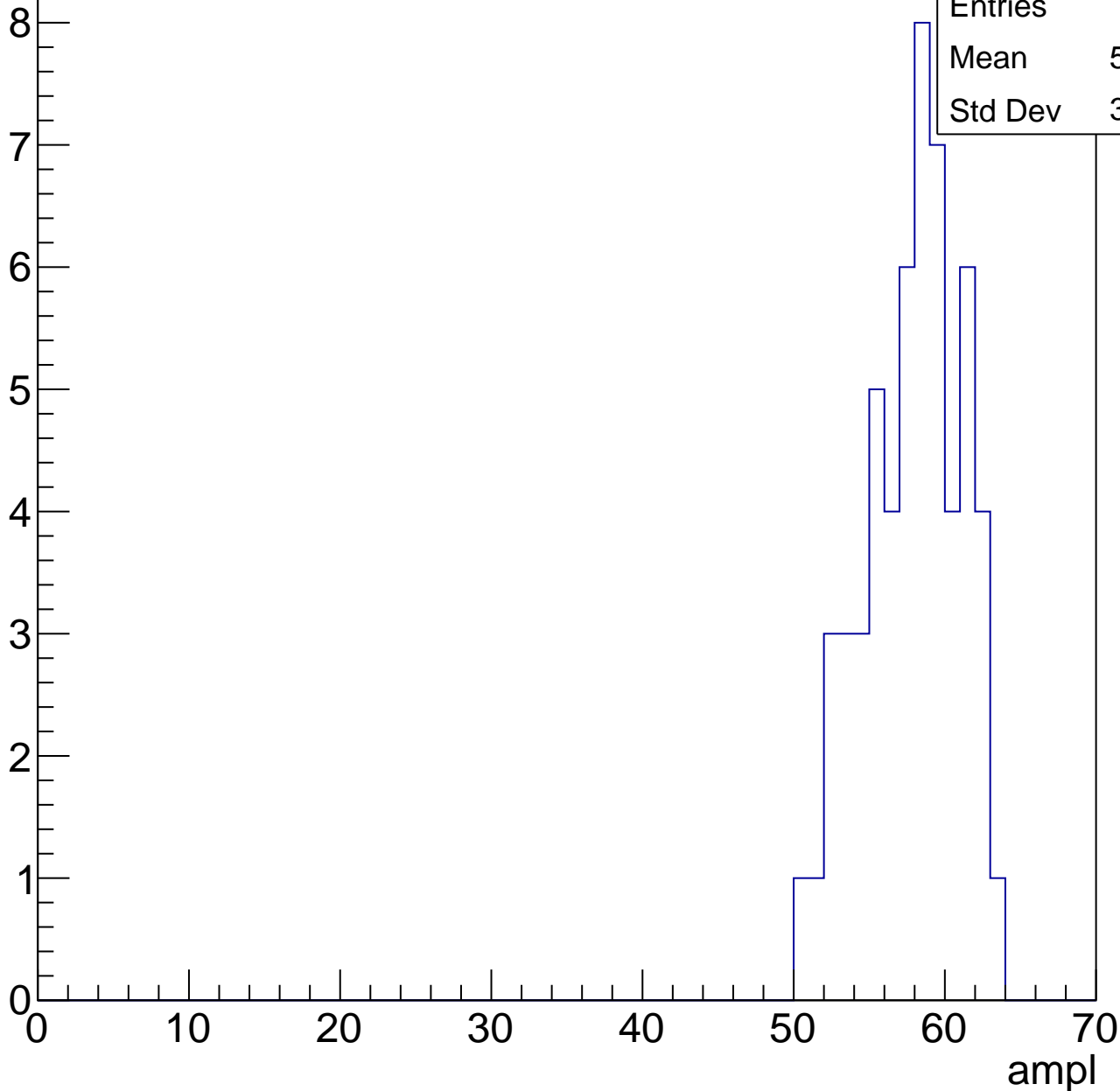


# B0L001S, U10-ch42, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	57.38
Std Dev	3.148

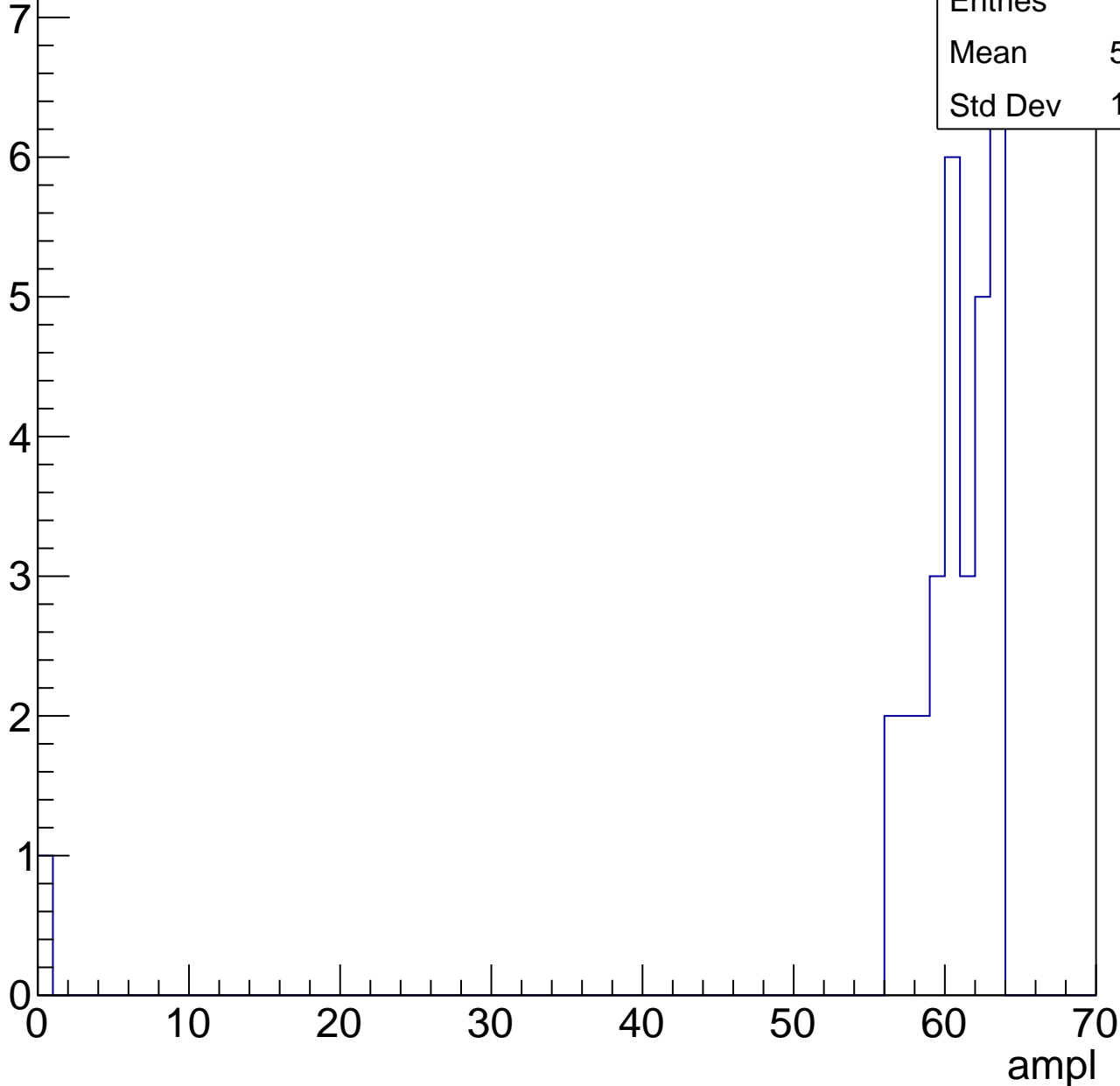


# B0L001S, U10-ch42, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	31
Mean	58.48
Std Dev	10.89



# B0L001S, U10-ch42, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch42, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L001S, U10-ch43, adc0

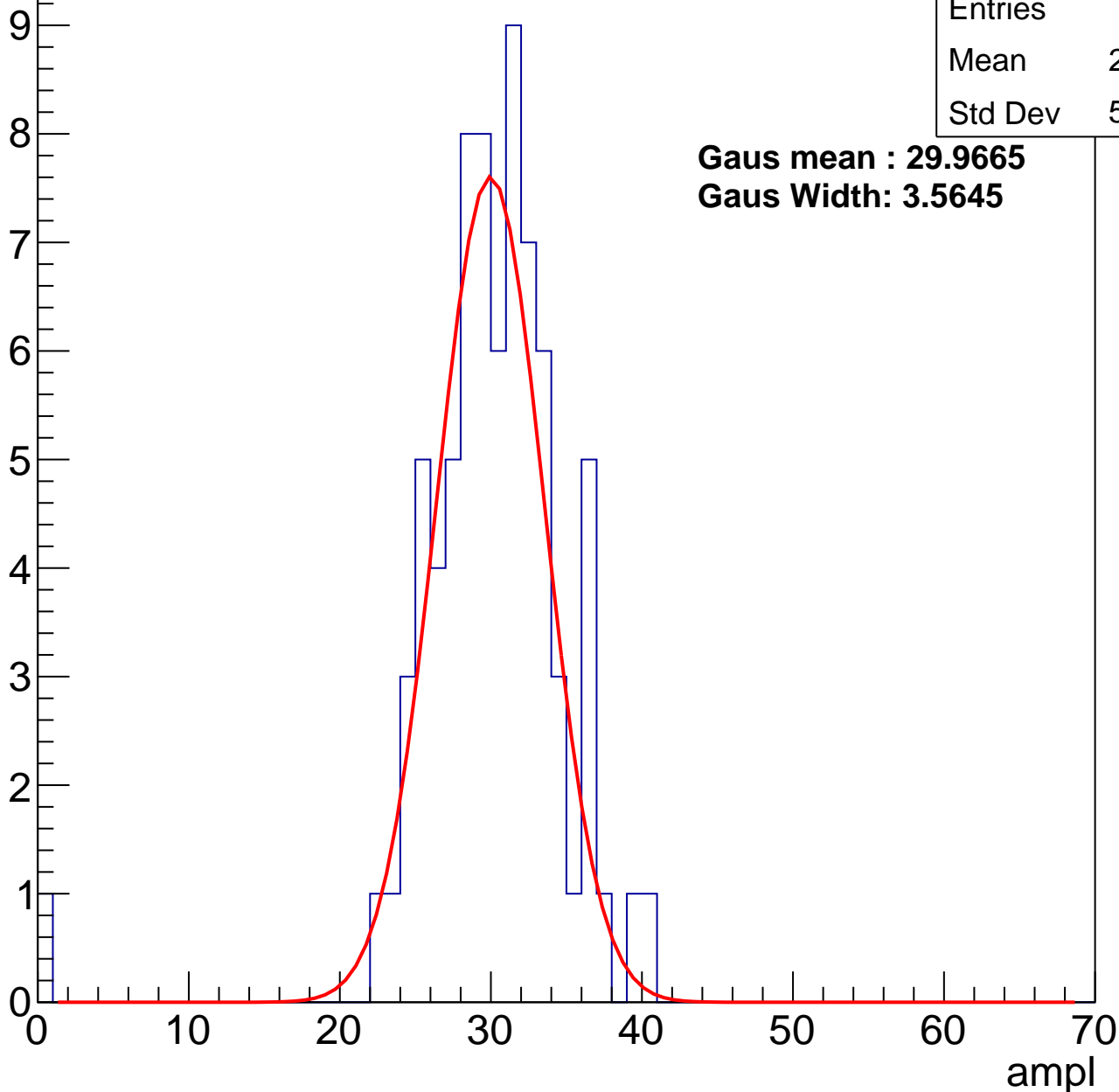
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	76
Mean	29.62
Std Dev	5.076

**Gaus mean : 29.9665**

**Gaus Width: 3.5645**



# B0L001S, U10-ch43, adc1

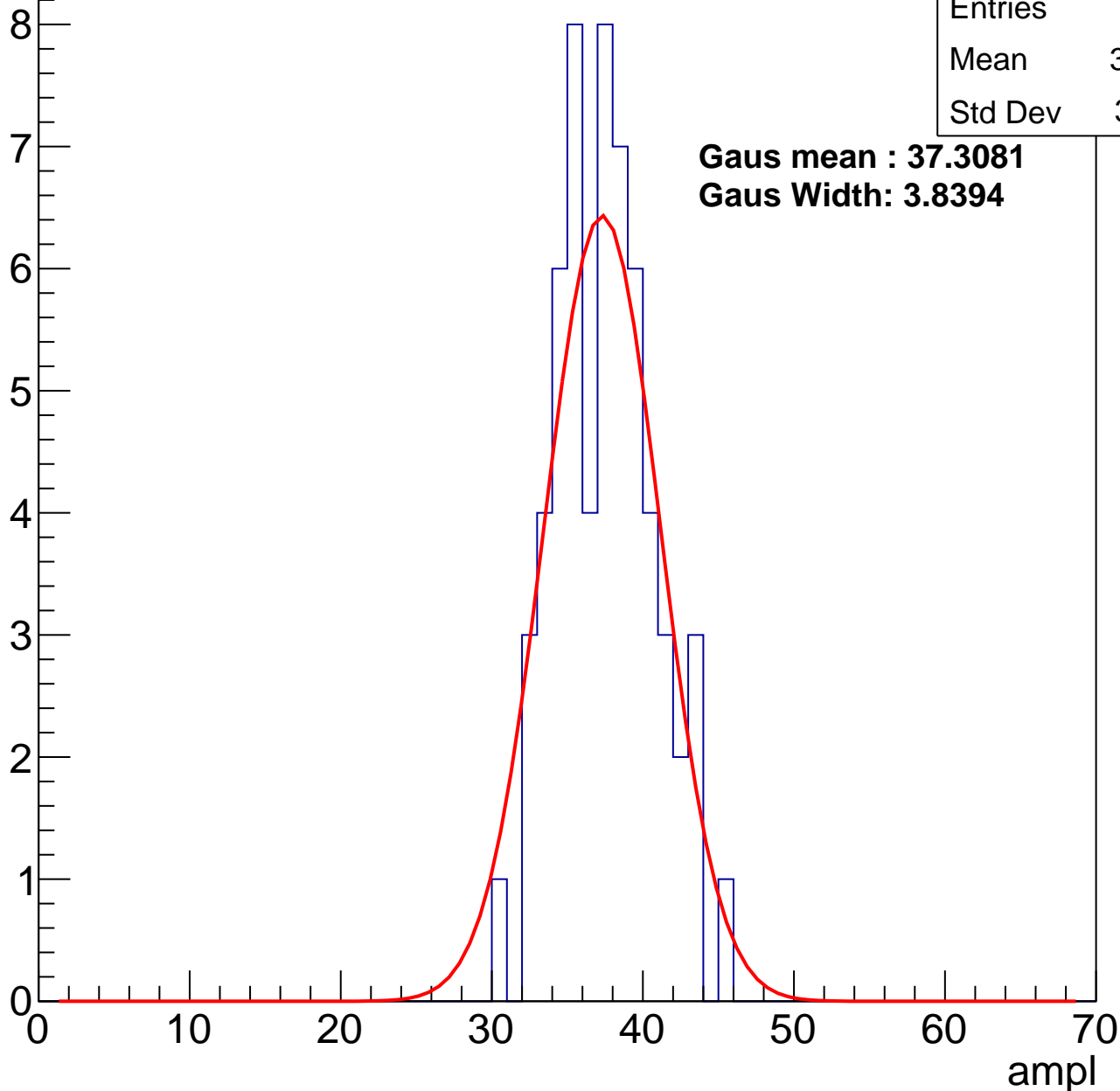
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	37.05
Std Dev	3.201

**Gaus mean : 37.3081**

**Gaus Width: 3.8394**



# B0L001S, U10-ch43, adc2

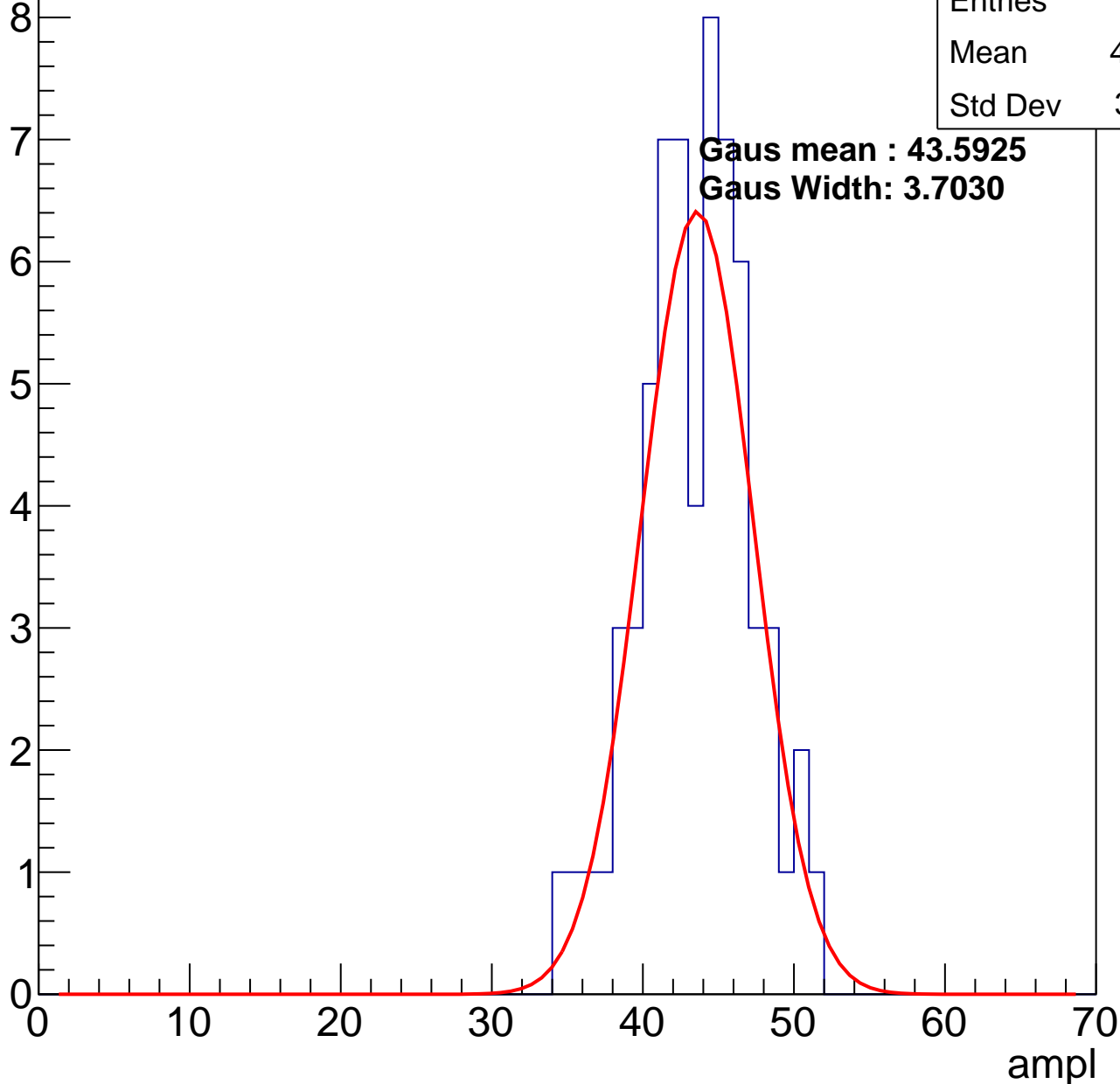
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	43.03
Std Dev	3.631

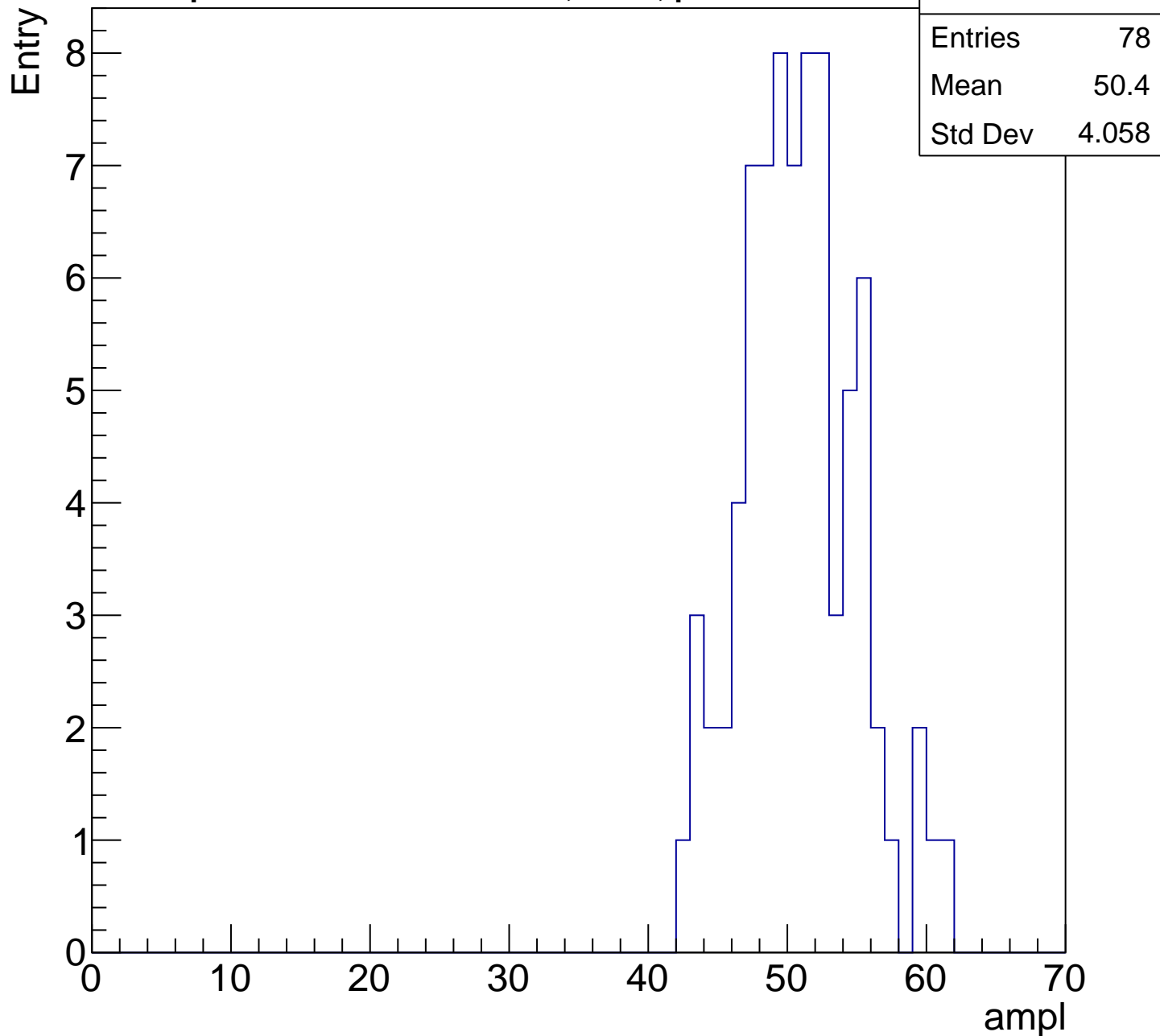
**Gaus mean : 43.5925**

**Gaus Width: 3.7030**



# B0L001S, U10-ch43, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

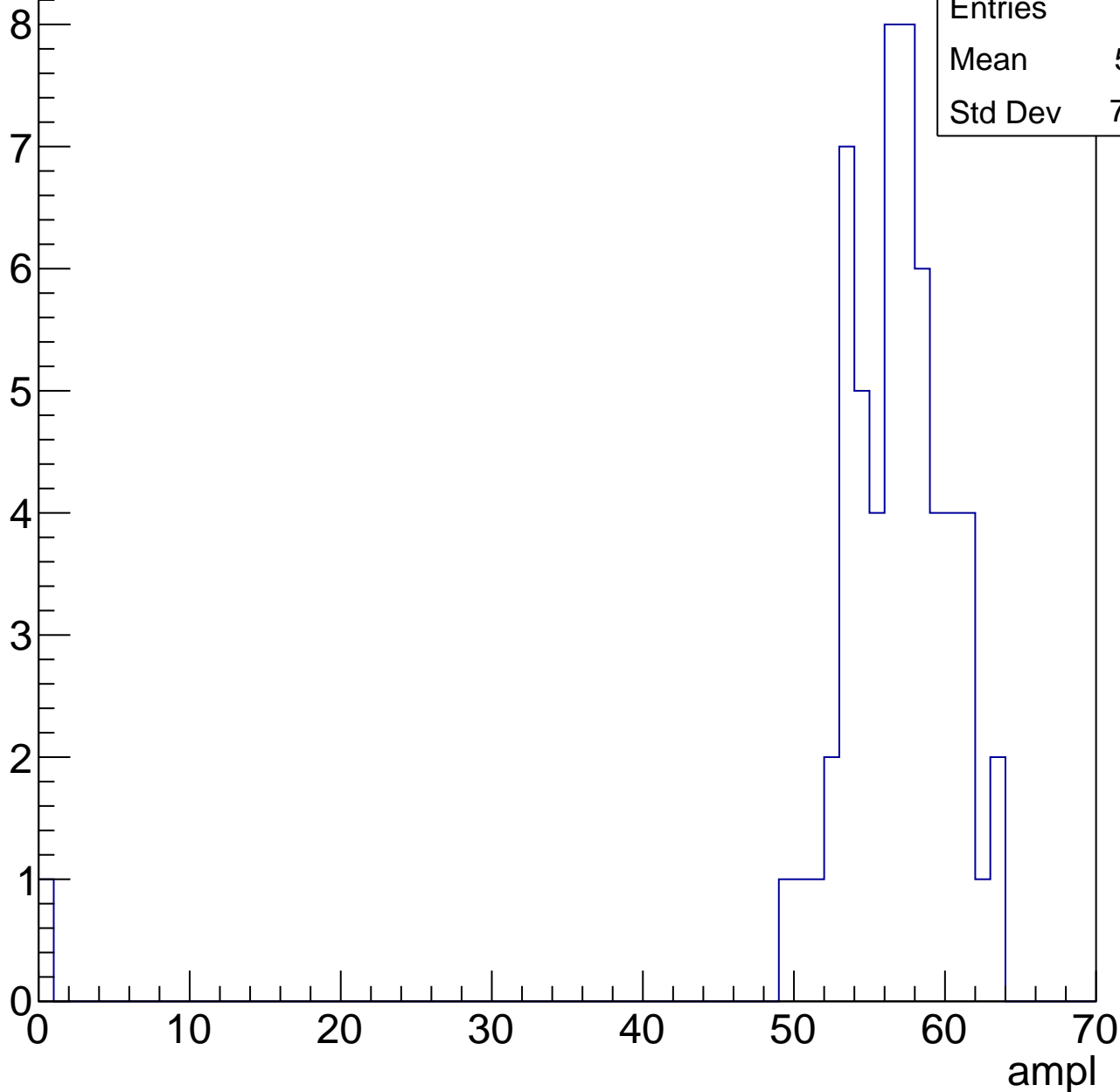


# B0L001S, U10-ch43, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	55.51
Std Dev	7.937



# B0L001S, U10-ch43, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

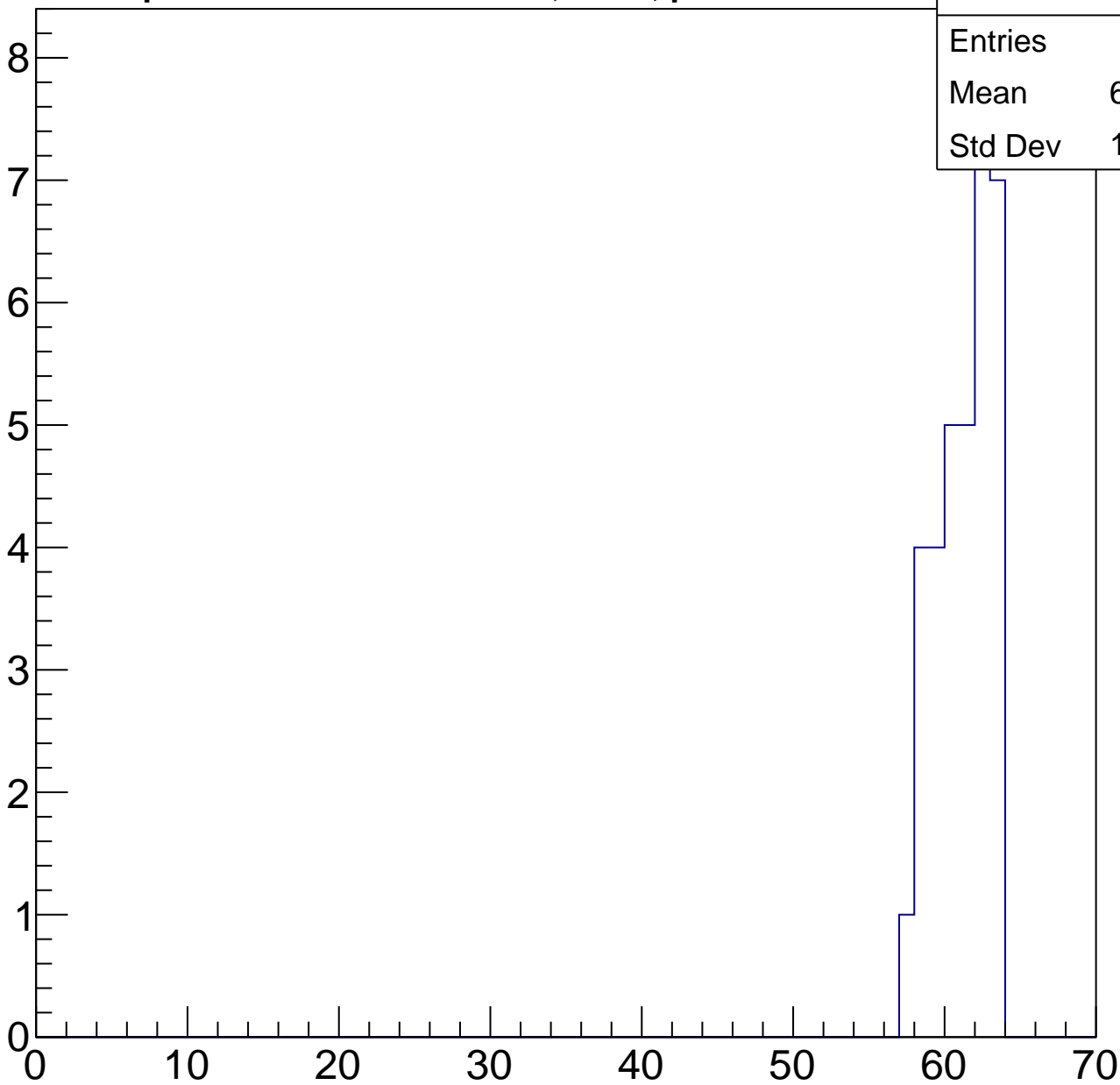
Entry

Entries	34
Mean	60.79
Std Dev	1.779

8  
7  
6  
5  
4  
3  
2  
1  
0

0 10 20 30 40 50 60 70

ampl



# B0L001S, U10-ch43, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch43, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U10-ch44, adc0

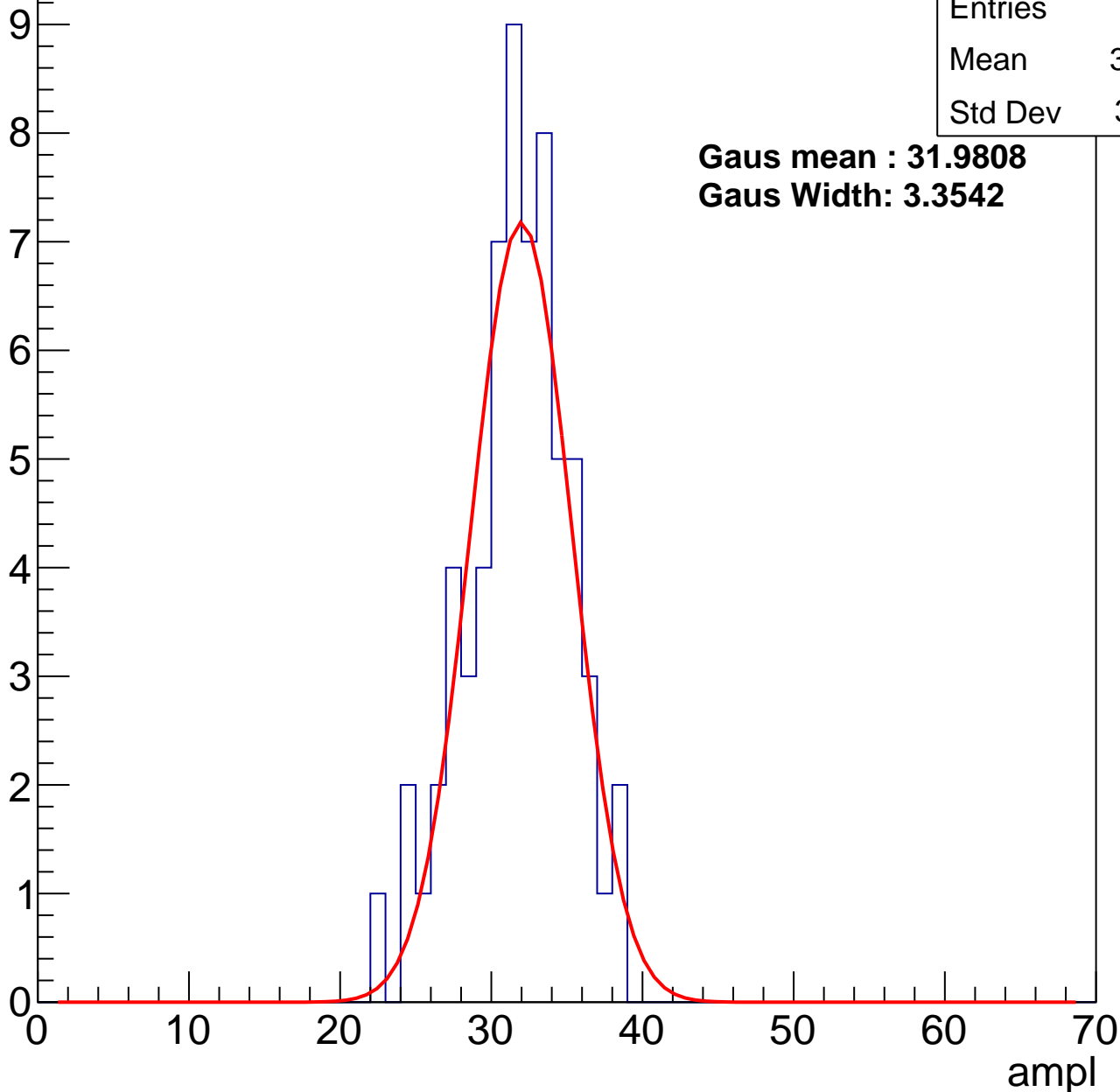
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	31.22
Std Dev	3.421

**Gaus mean : 31.9808**

**Gaus Width: 3.3542**



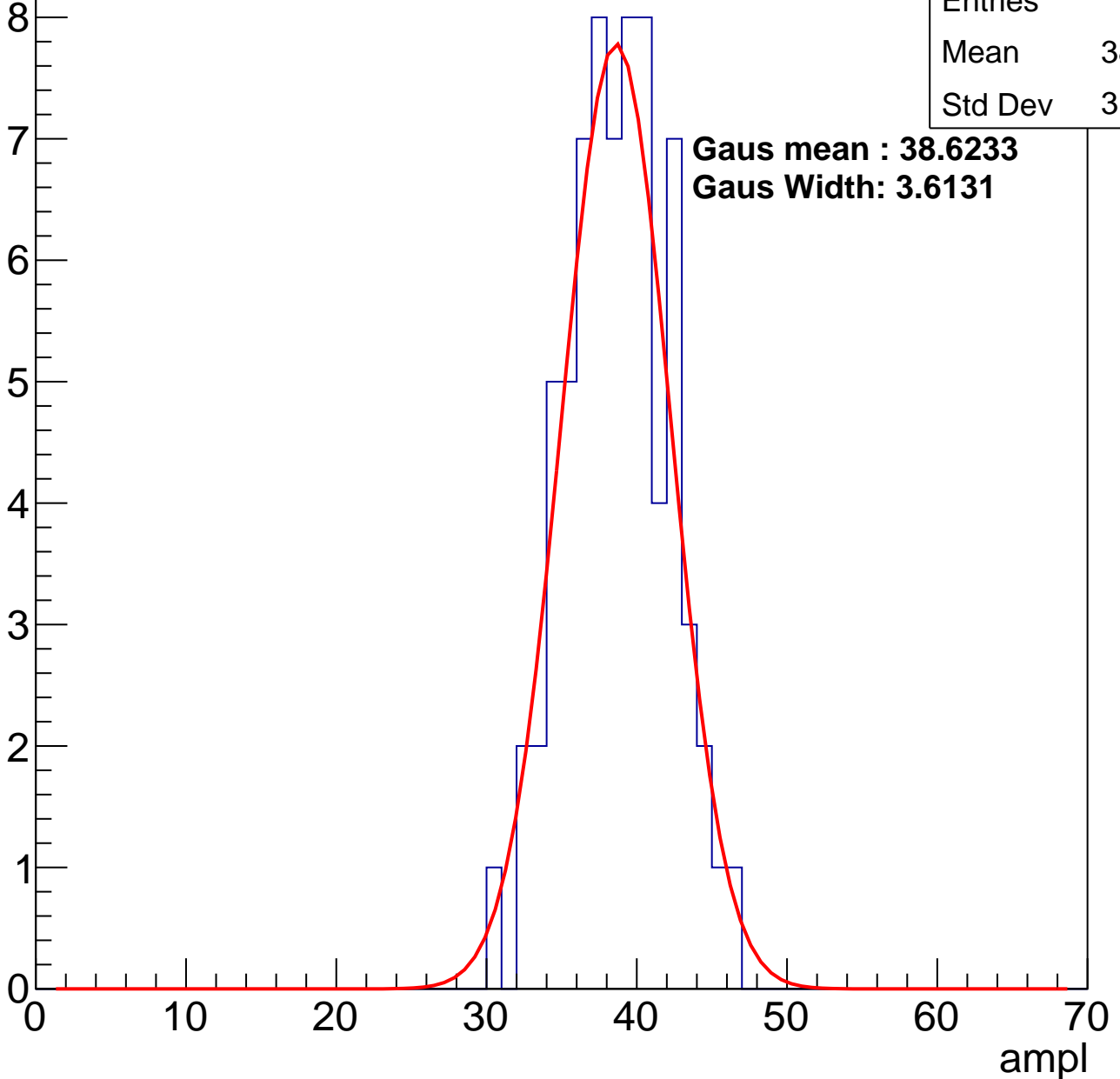
# B0L001S, U10-ch44, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	38.27
Std Dev	3.336

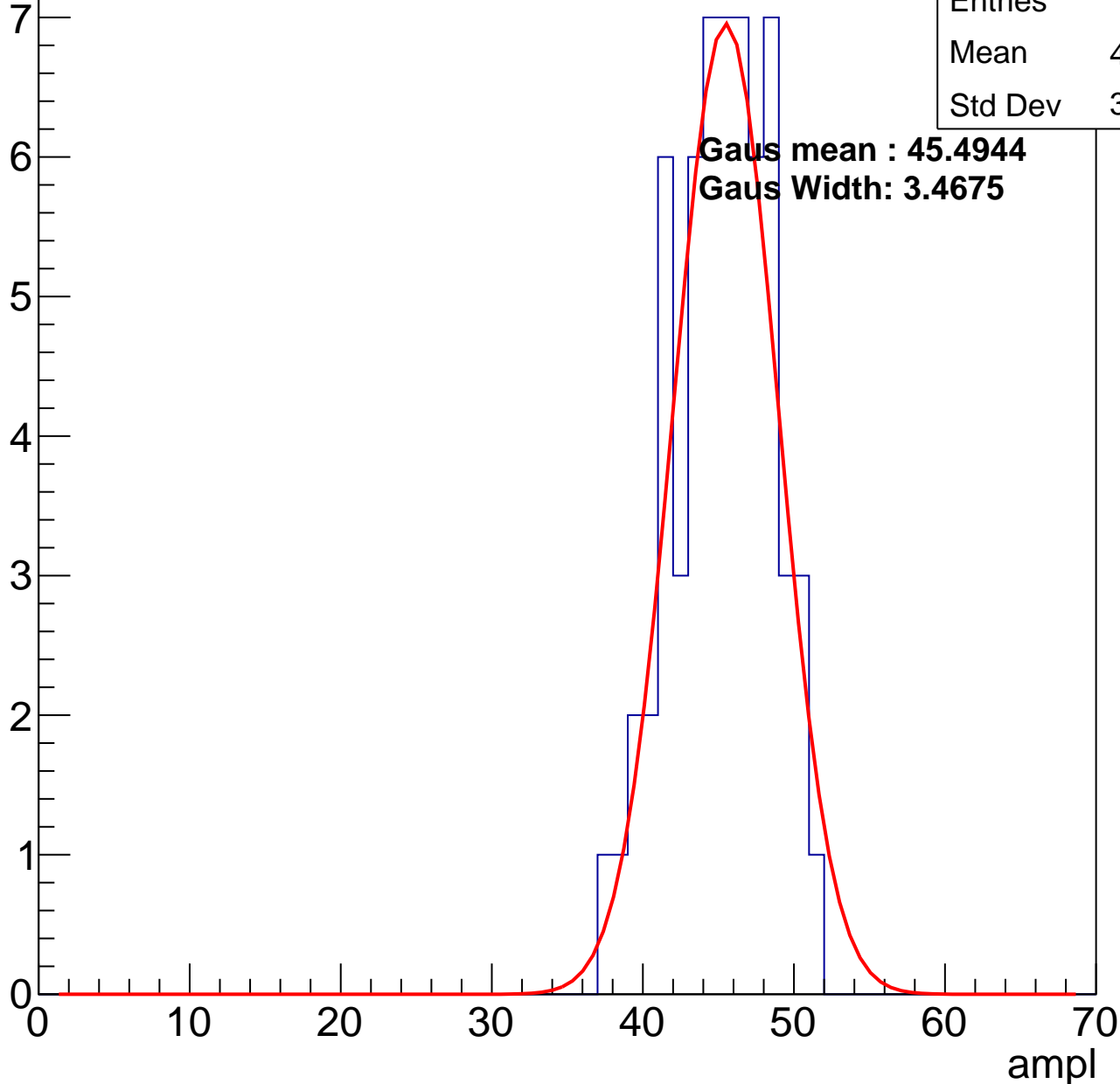
**Gaus mean : 38.6233**  
**Gaus Width: 3.6131**



# B0L001S, U10-ch44, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



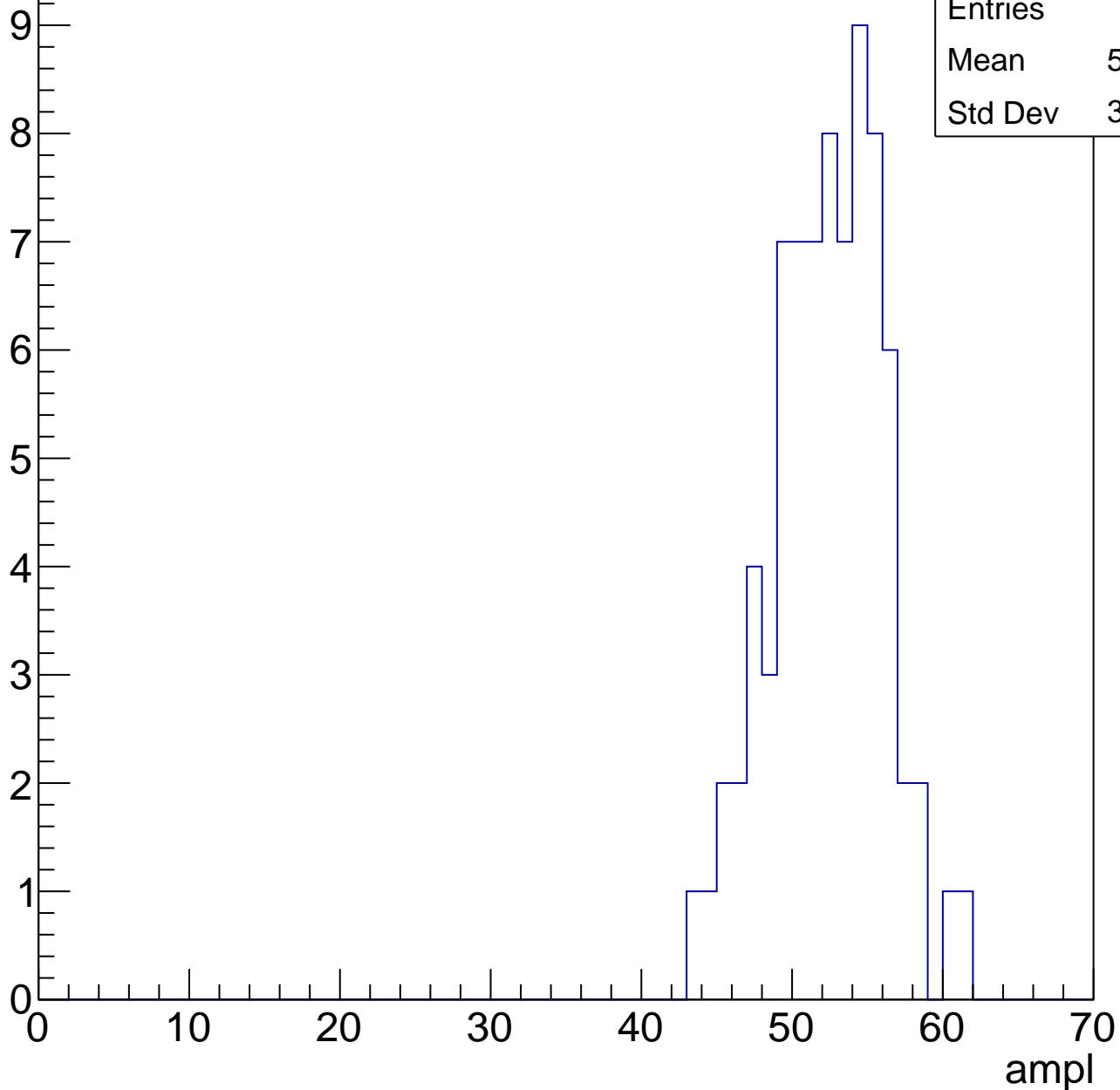
Entries	62
Mean	44.74
Std Dev	3.208

# B0L001S, U10-ch44, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

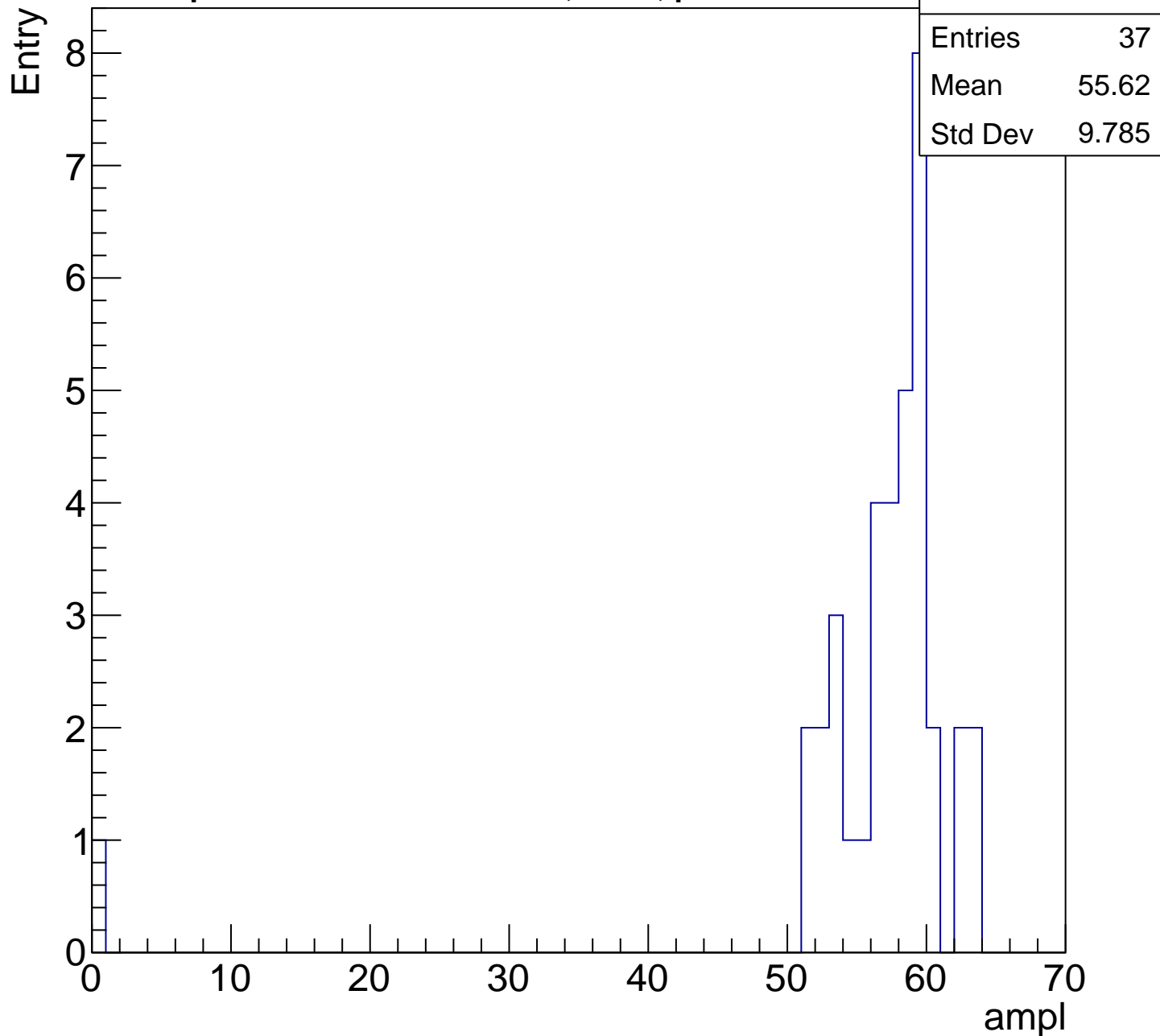
Entry

Entries	78
Mean	51.94
Std Dev	3.649



# B0L001S, U10-ch44, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

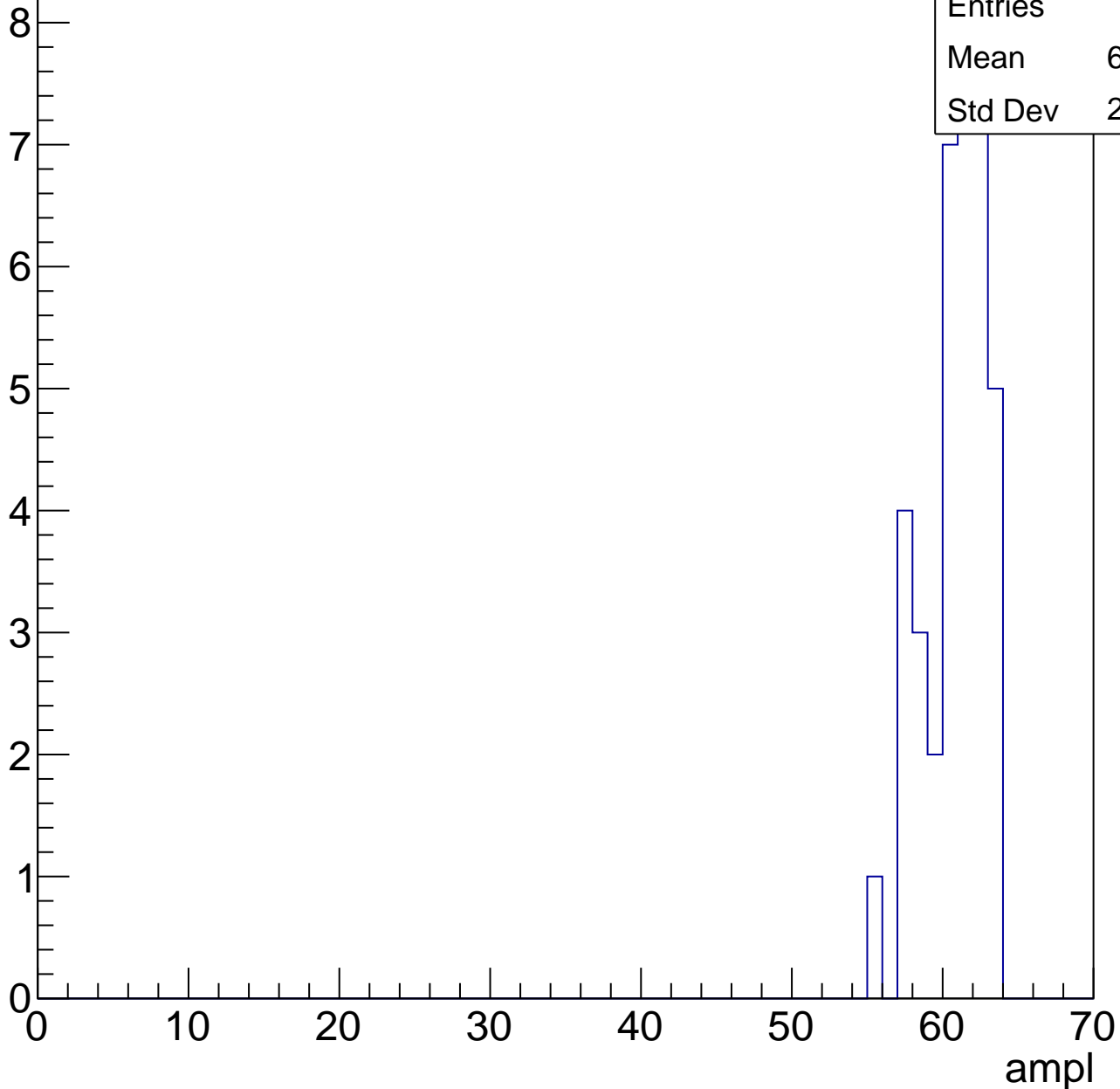


# B0L001S, U10-ch44, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	38
Mean	60.37
Std Dev	2.019



# B0L001S, U10-ch44, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch44, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U10-ch45, adc0

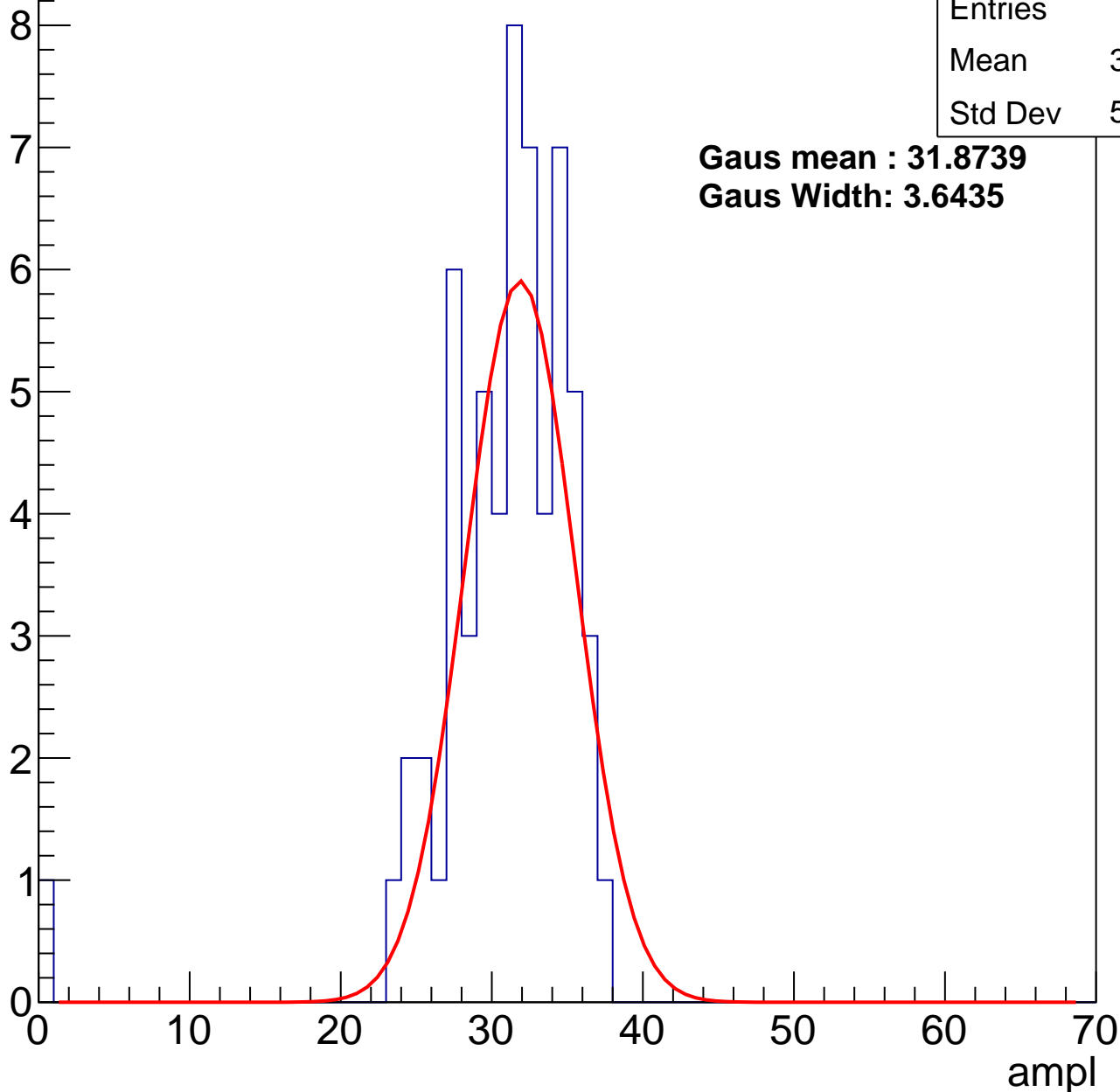
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	30.33
Std Dev	5.192

**Gaus mean : 31.8739**

**Gaus Width: 3.6435**



# B0L001S, U10-ch45, adc1

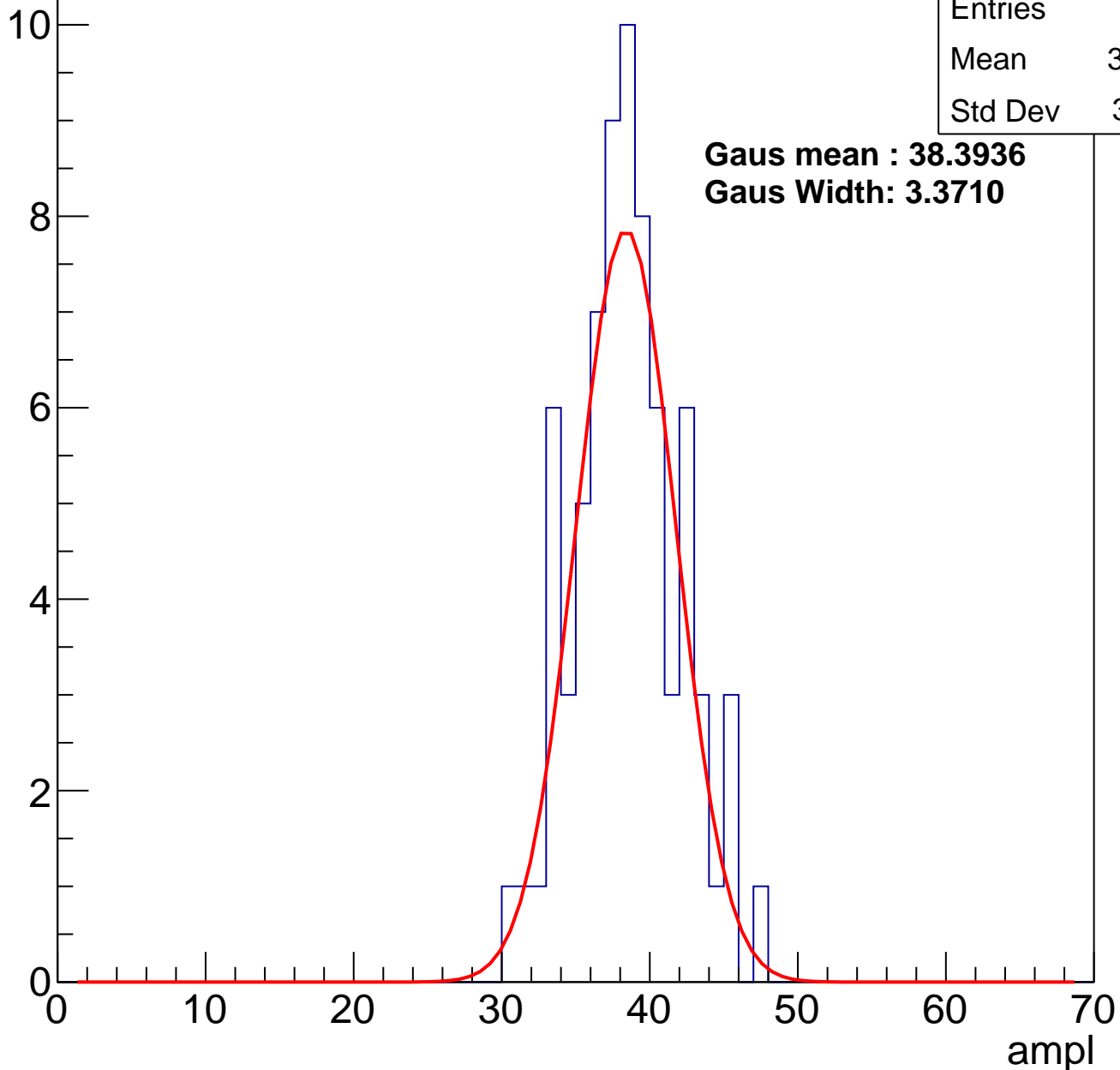
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	74
Mean	38.04
Std Dev	3.531

**Gaus mean : 38.3936**

**Gaus Width: 3.3710**

Entry



# B0L001S, U10-ch45, adc2

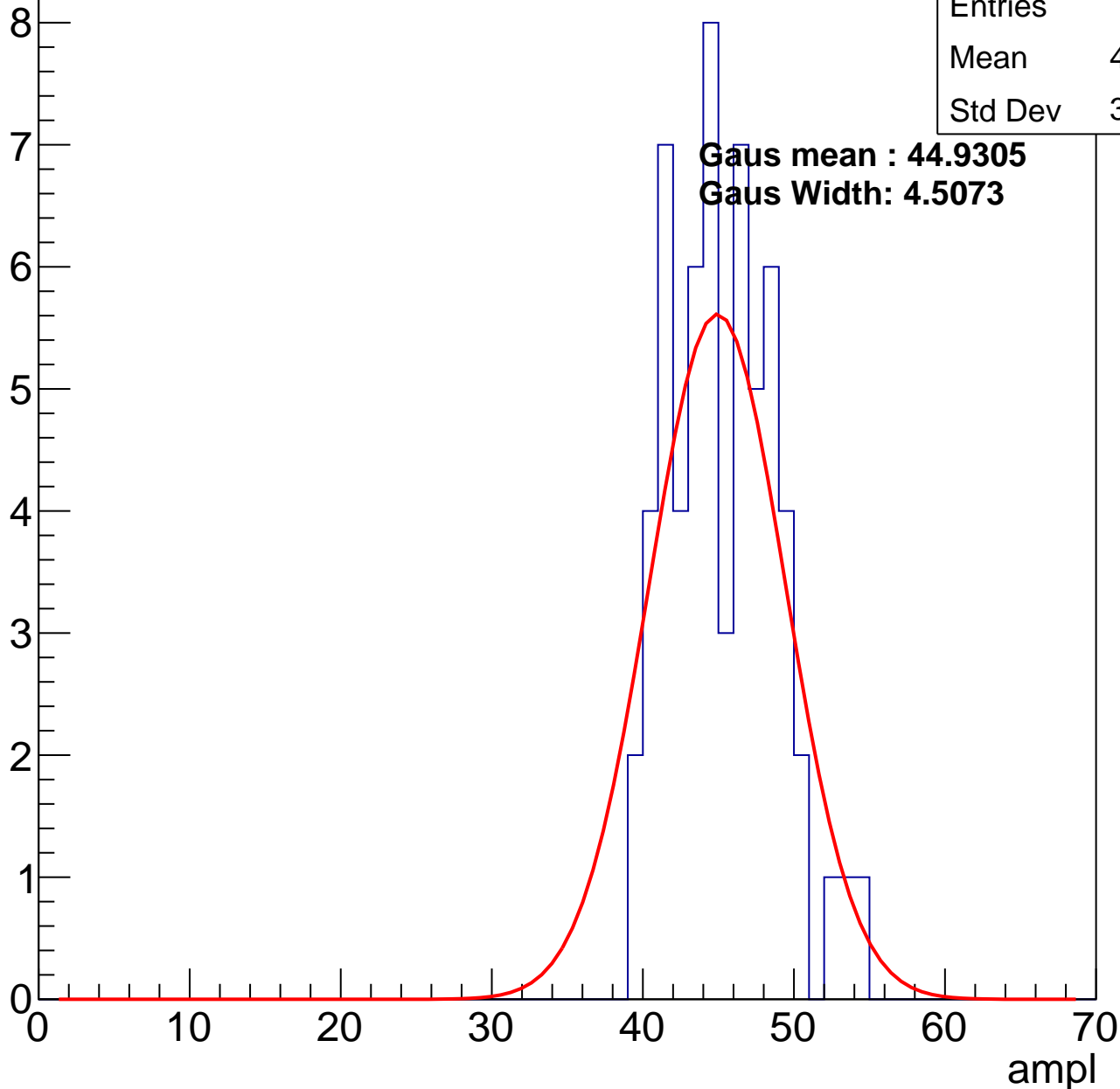
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	44.89
Std Dev	3.483

**Gaus mean : 44.9305**

**Gaus Width: 4.5073**



# B0L001S, U10-ch45, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

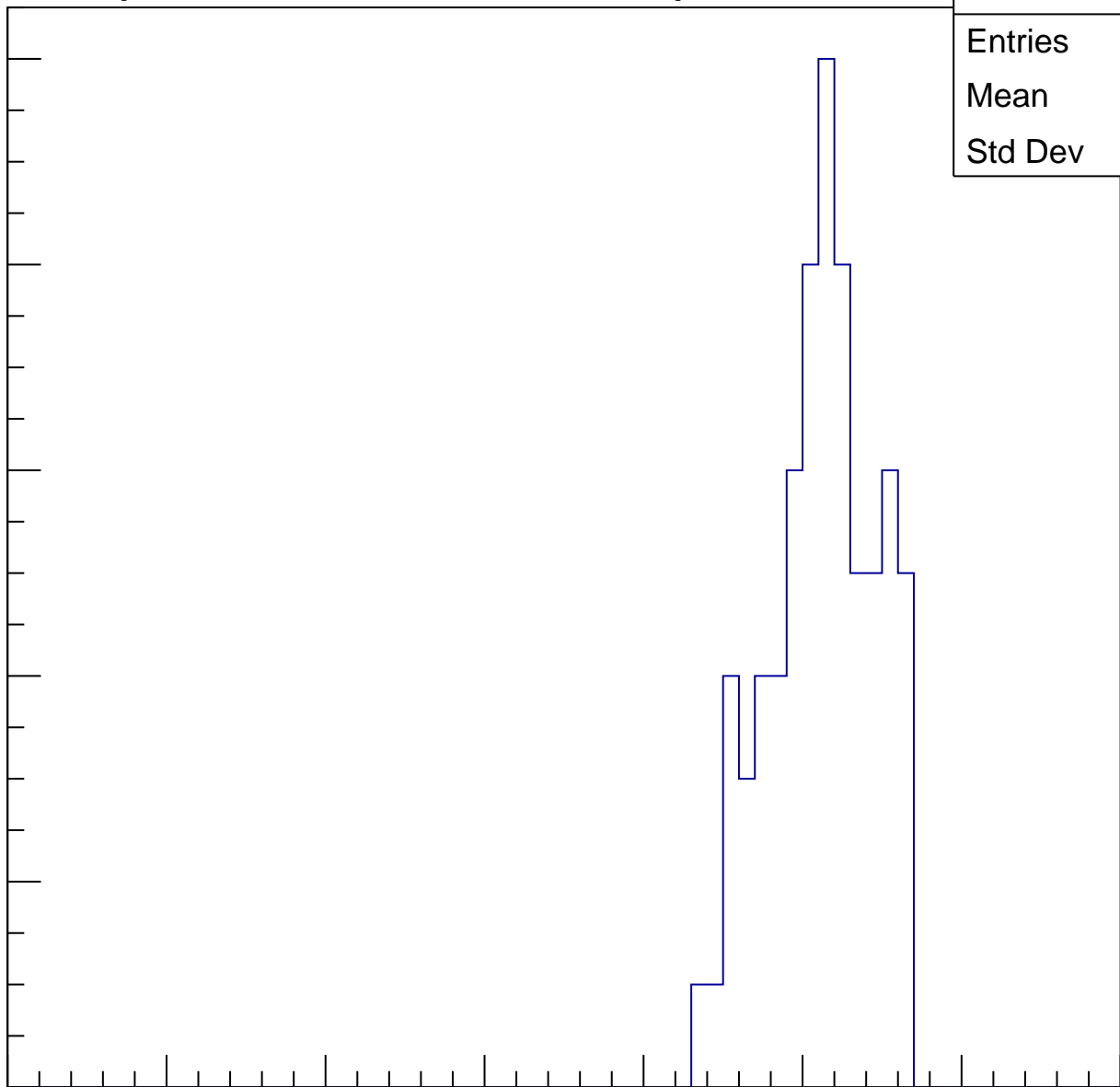
Entries	70
Mean	50.71
Std Dev	3.278

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B0L001S, U10-ch45, adc4

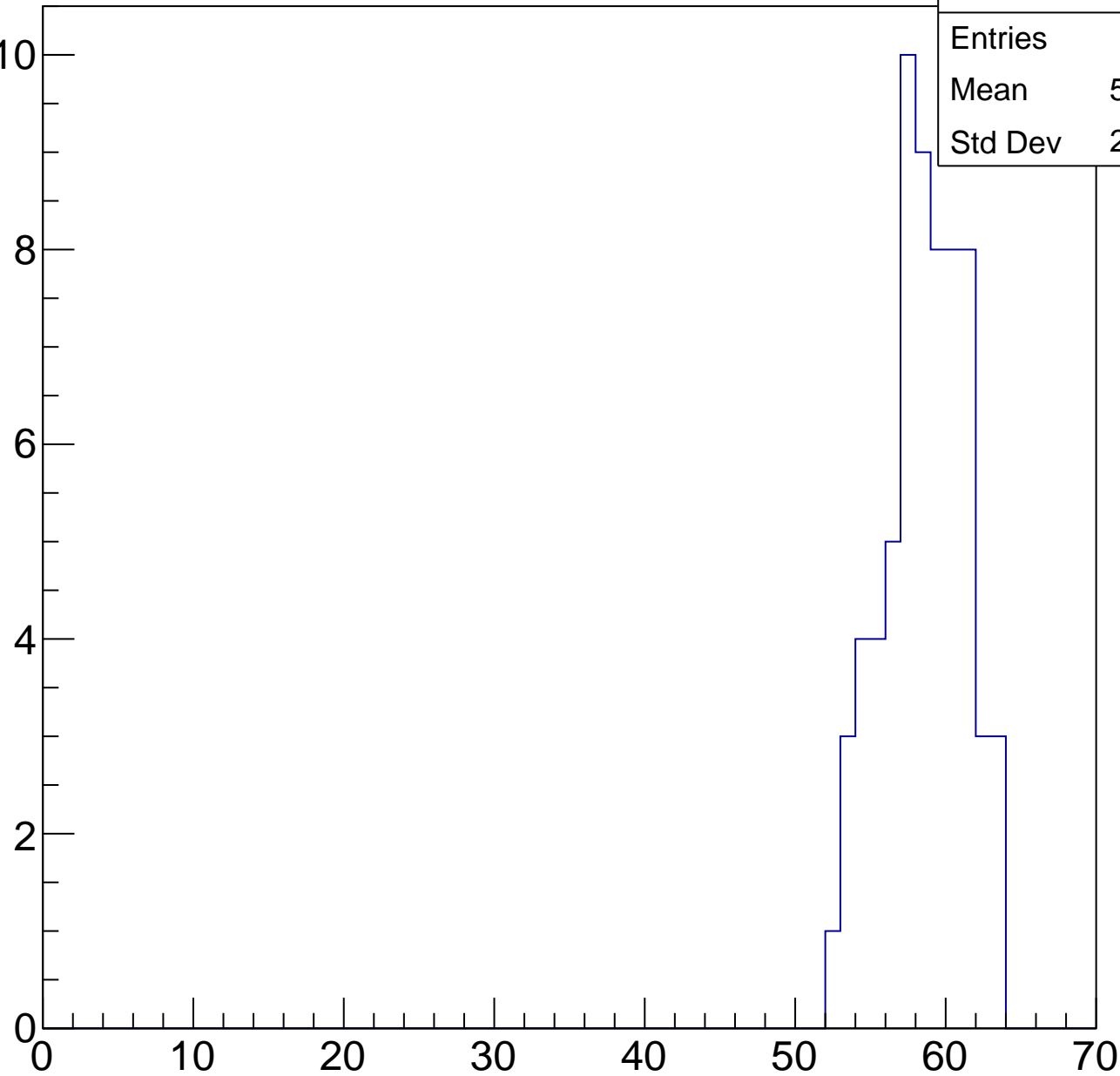
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

10  
8  
6  
4  
2  
0

Entries	66
Mean	58.09
Std Dev	2.684

ampl

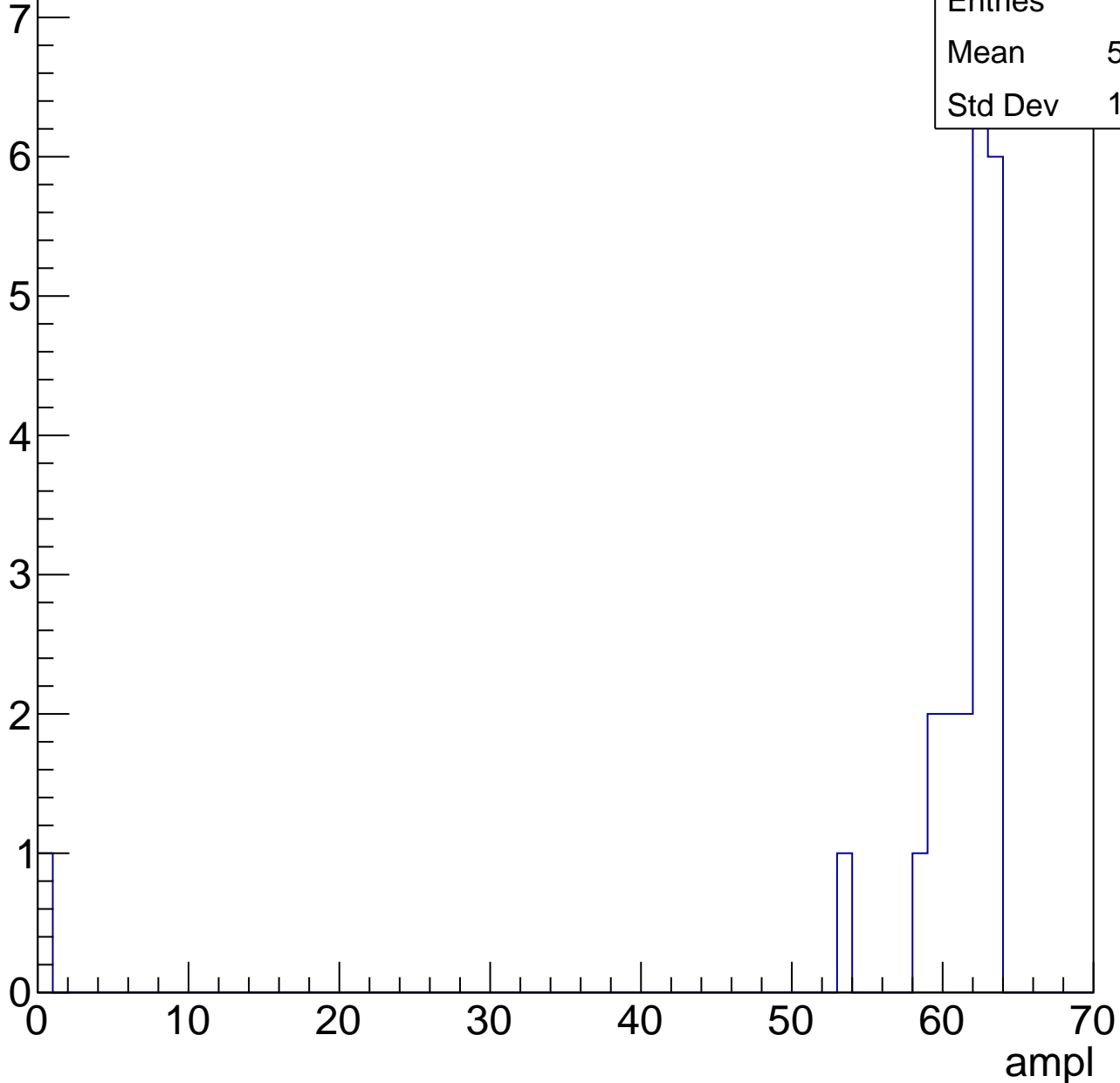


# B0L001S, U10-ch45, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	22
Mean	58.32
Std Dev	12.93



# B0L001S, U10-ch45, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch45, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U10-ch46, adc0

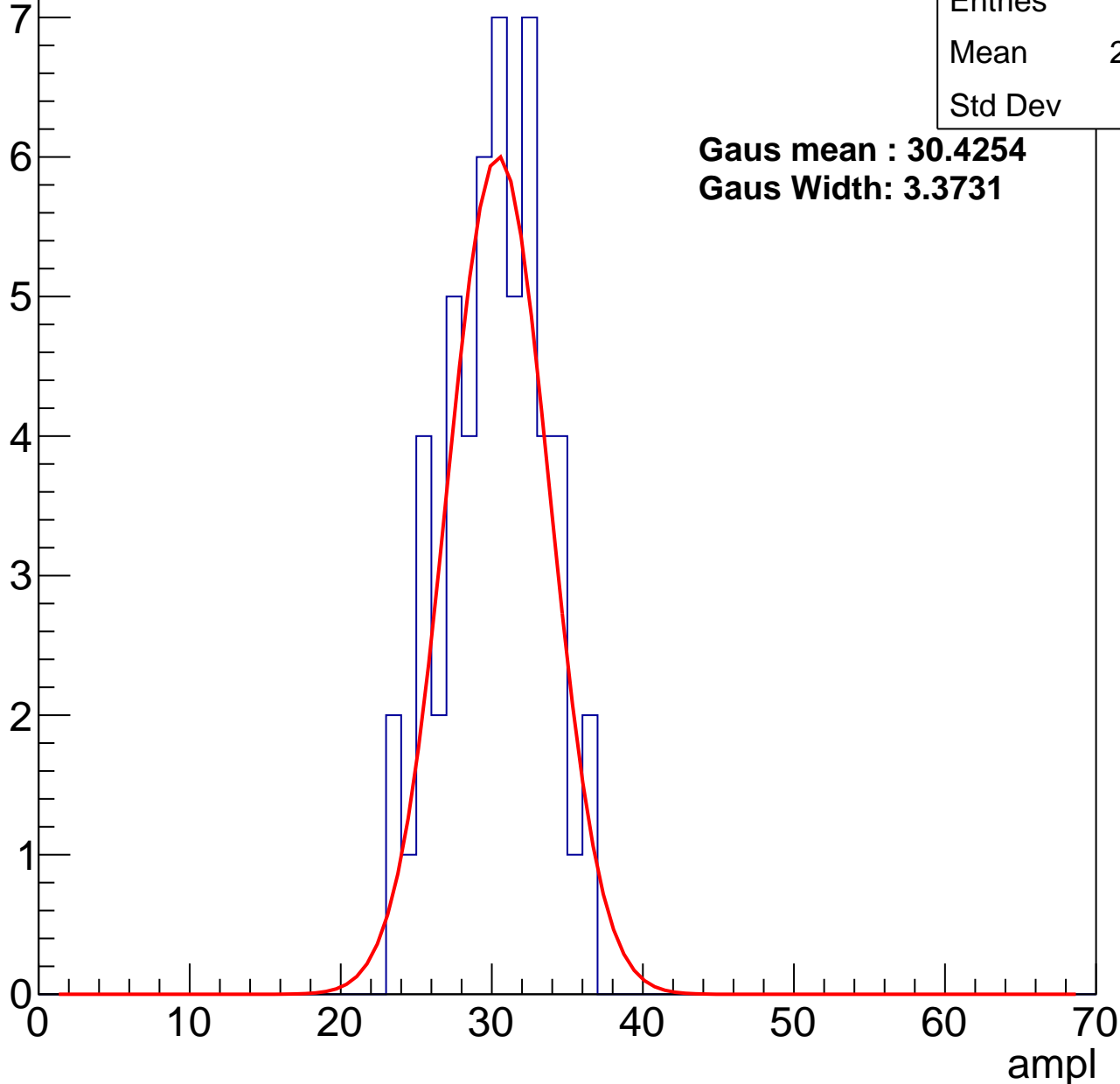
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	29.76
Std Dev	3.22

**Gaus mean : 30.4254**

**Gaus Width: 3.3731**



# B0L001S, U10-ch46, adc1

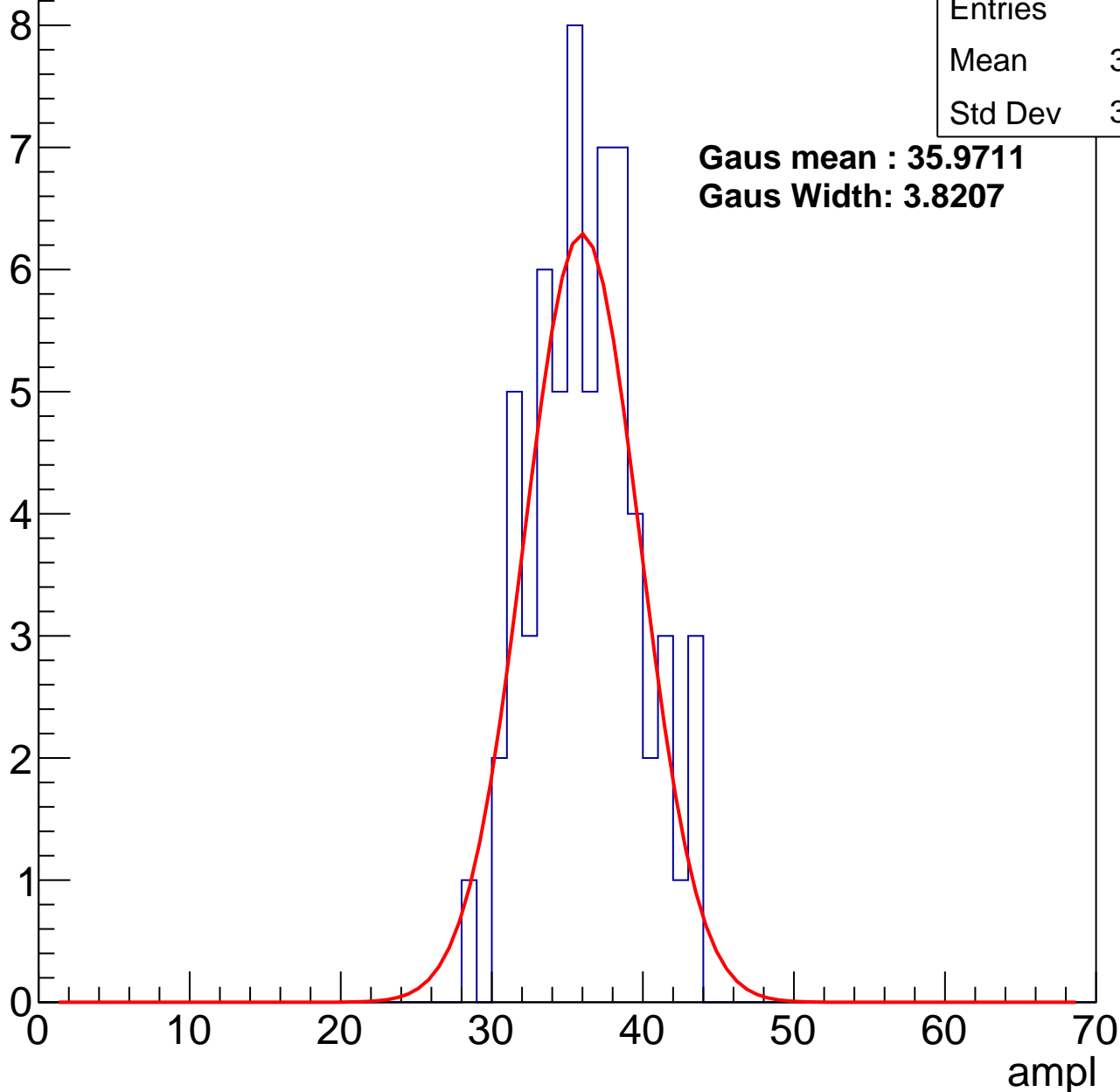
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	35.84
Std Dev	3.479

**Gaus mean : 35.9711**

**Gaus Width: 3.8207**



# B0L001S, U10-ch46, adc2

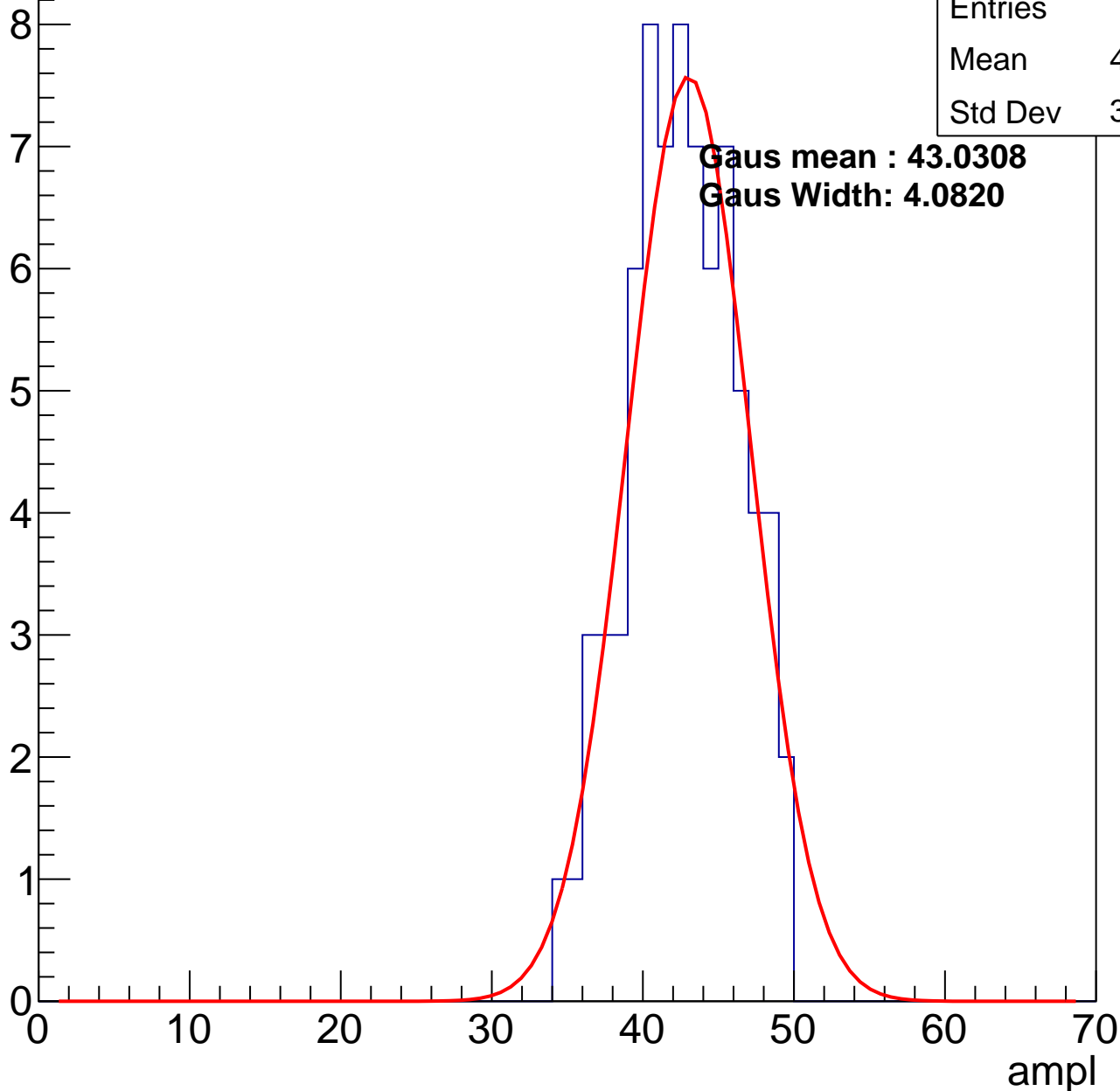
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	75
Mean	42.23
Std Dev	3.557

**Gaus mean : 43.0308**

**Gaus Width: 4.0820**

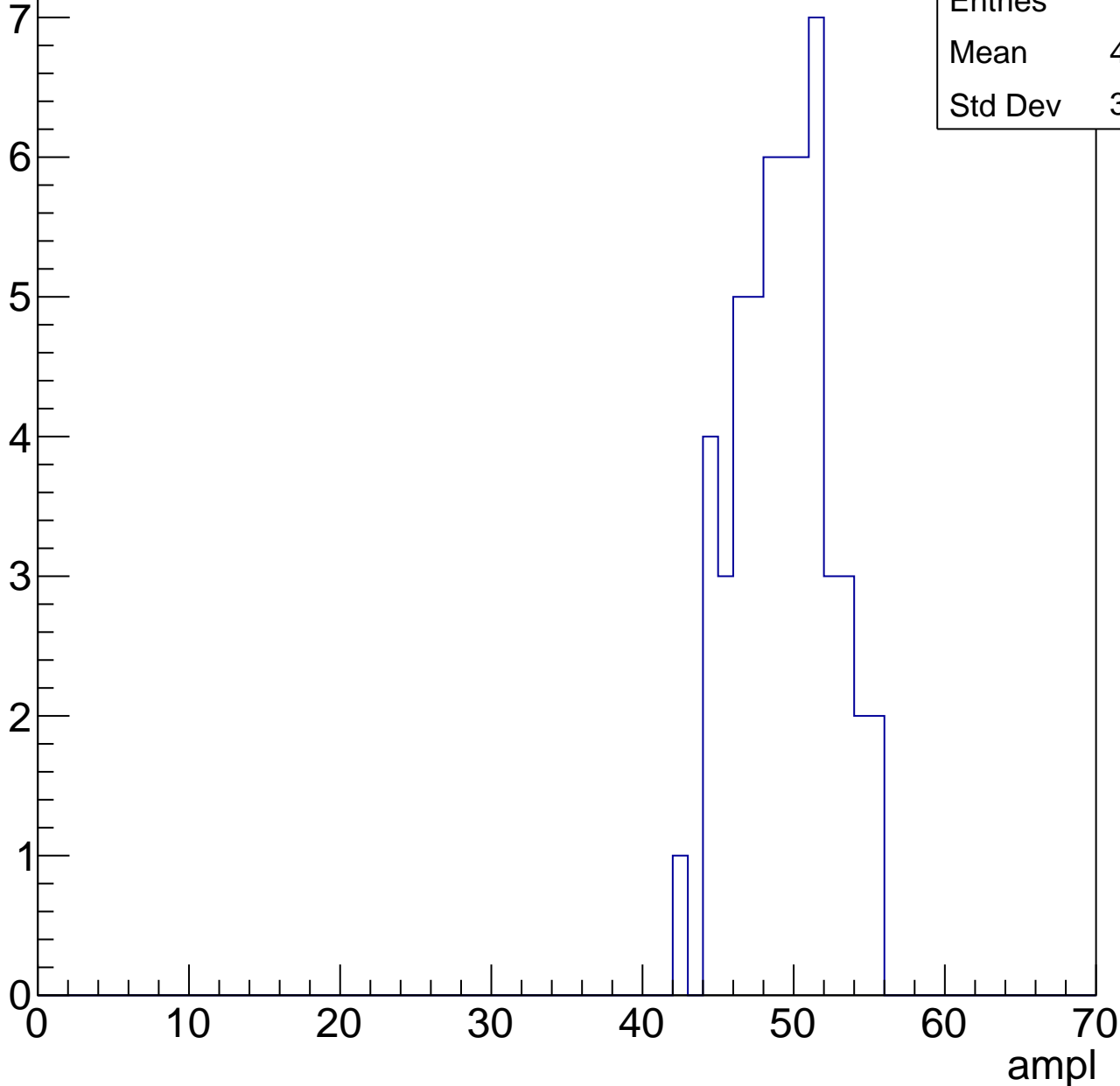


# B0L001S, U10-ch46, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	48.87
Std Dev	3.066

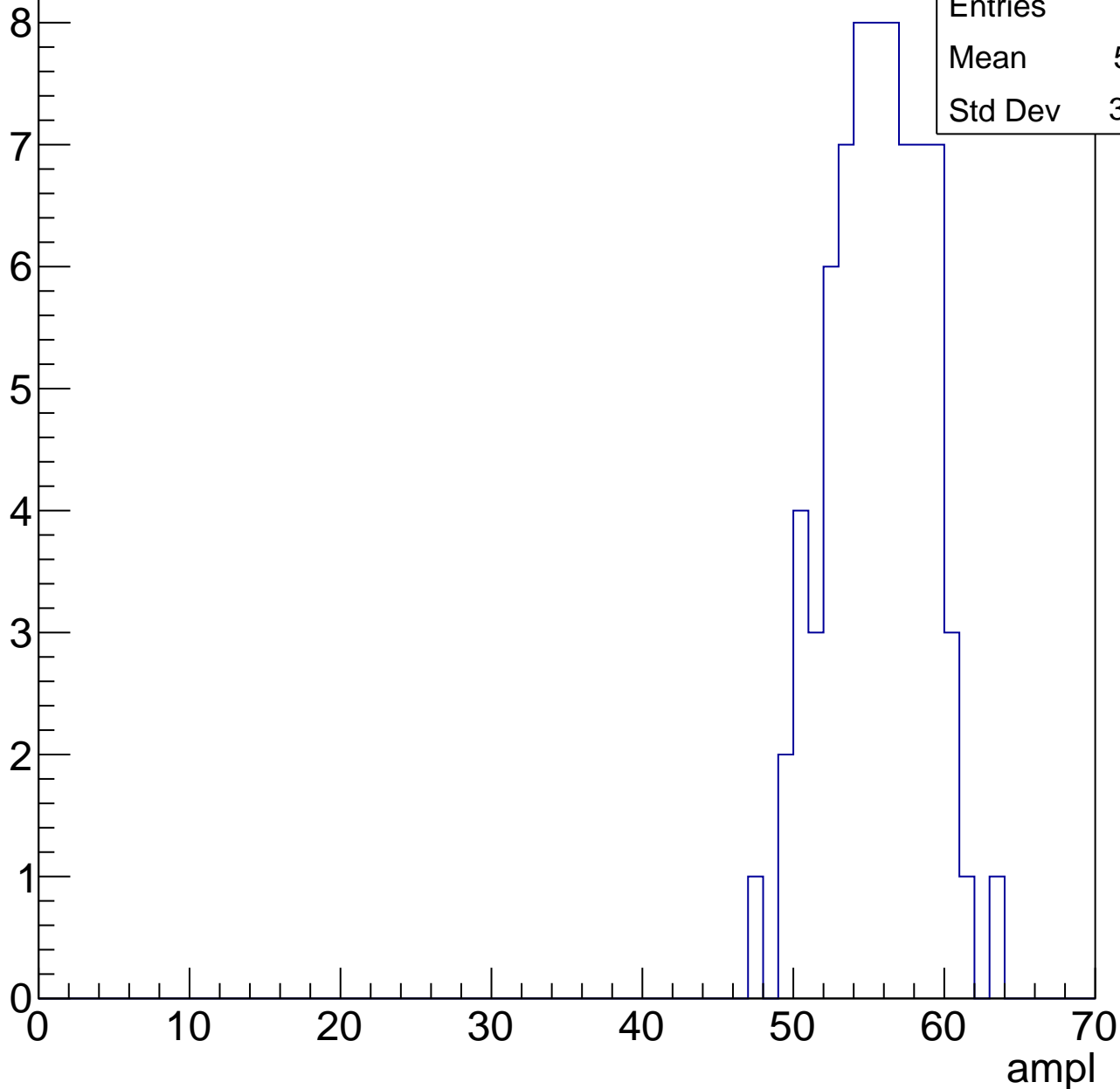


# B0L001S, U10-ch46, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	55.11
Std Dev	3.225

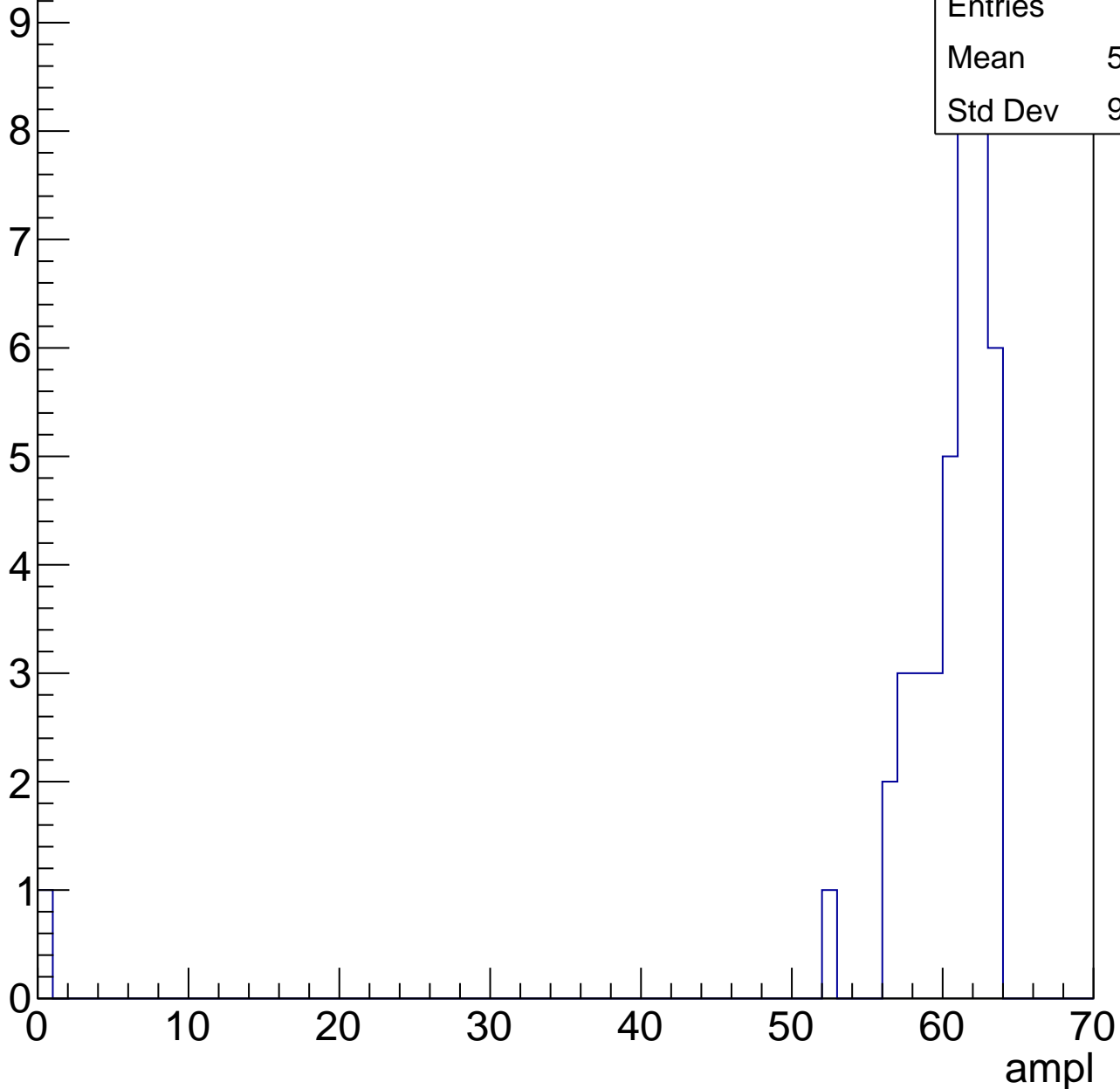


# B0L001S, U10-ch46, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

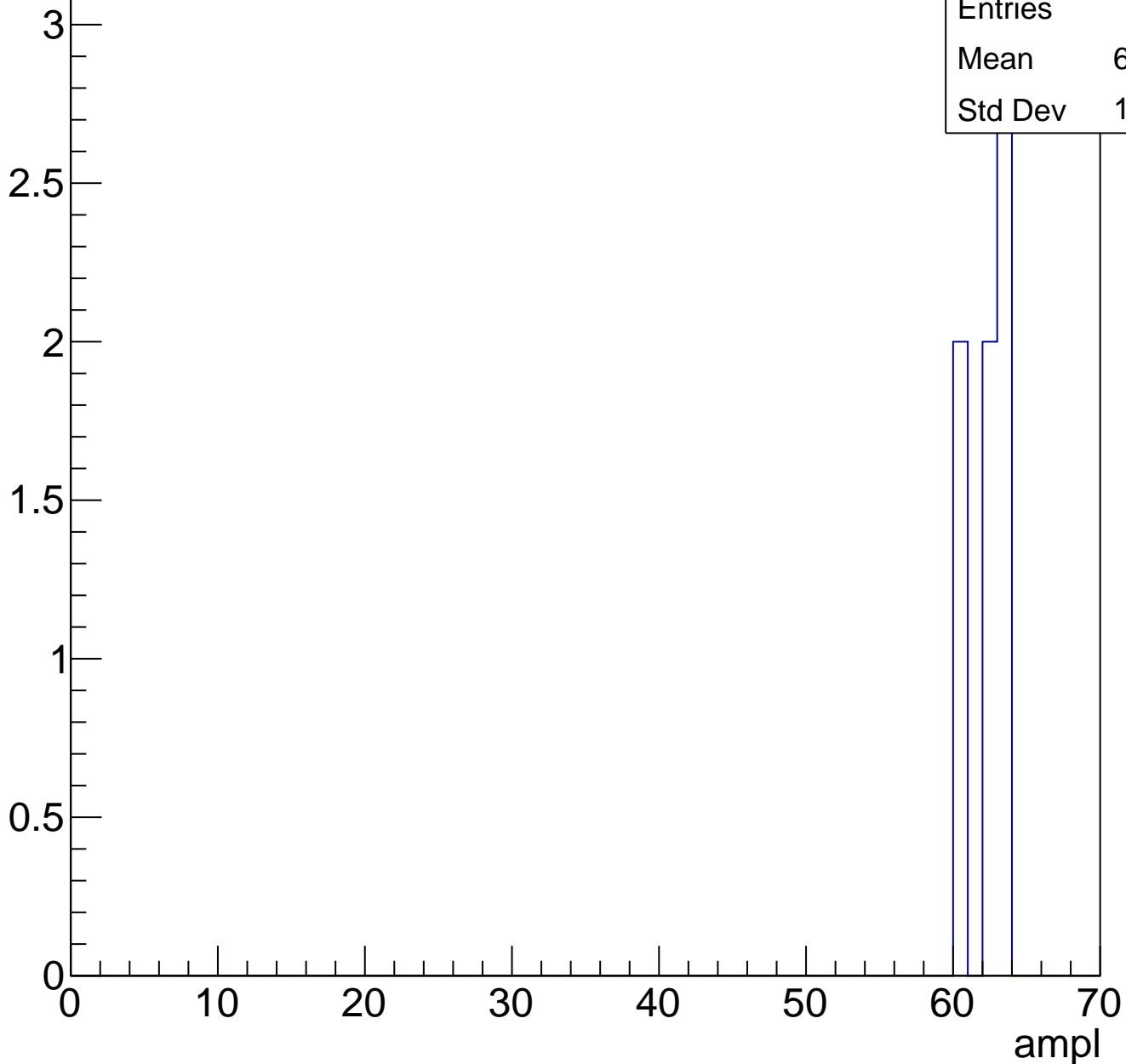
Entries	41
Mean	58.76
Std Dev	9.589



# B0L001S, U10-ch46, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch46, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L001S, U10-ch47, adc0

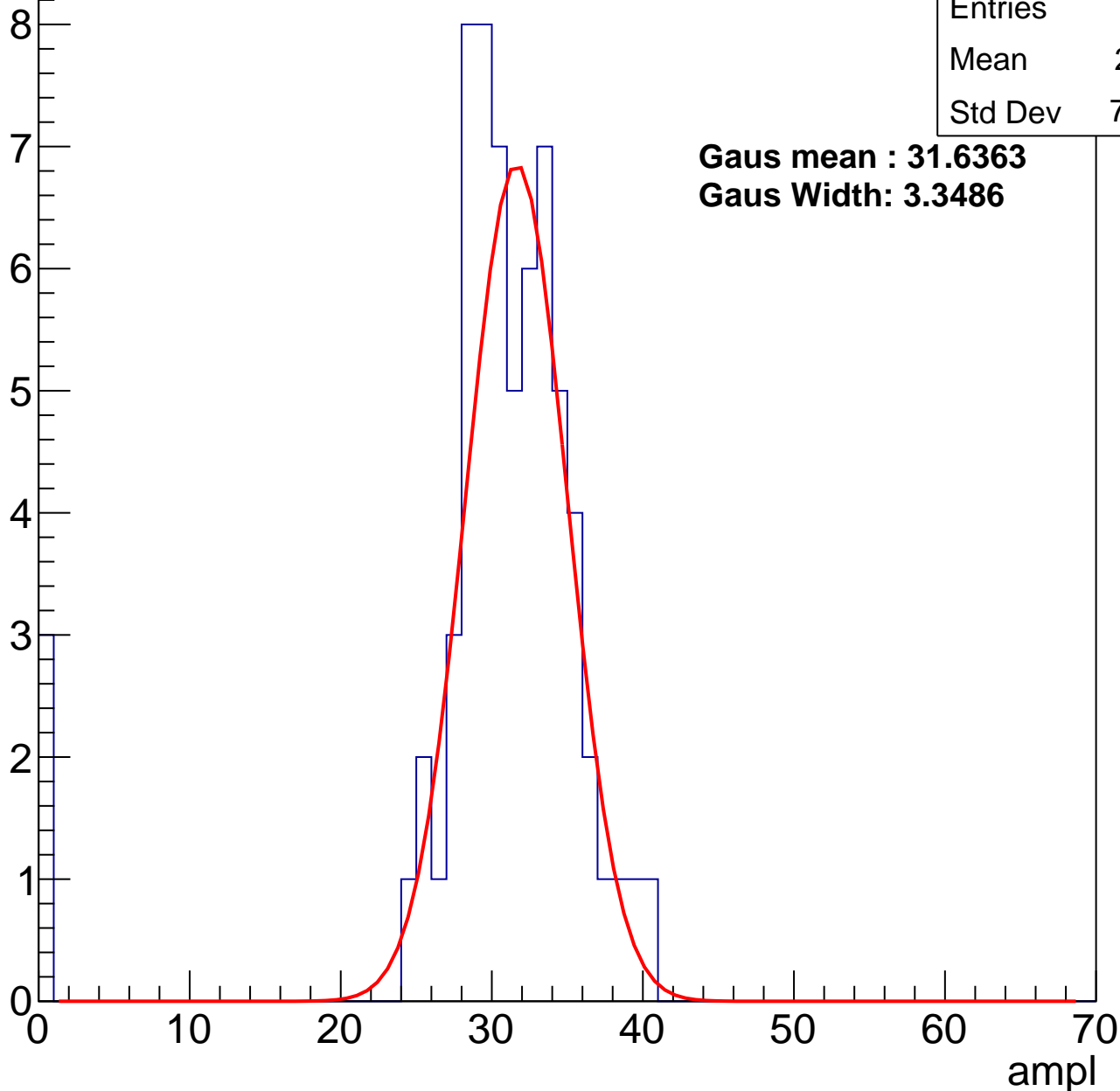
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	29.71
Std Dev	7.284

**Gaus mean : 31.6363**

**Gaus Width: 3.3486**



# B0L001S, U10-ch47, adc1

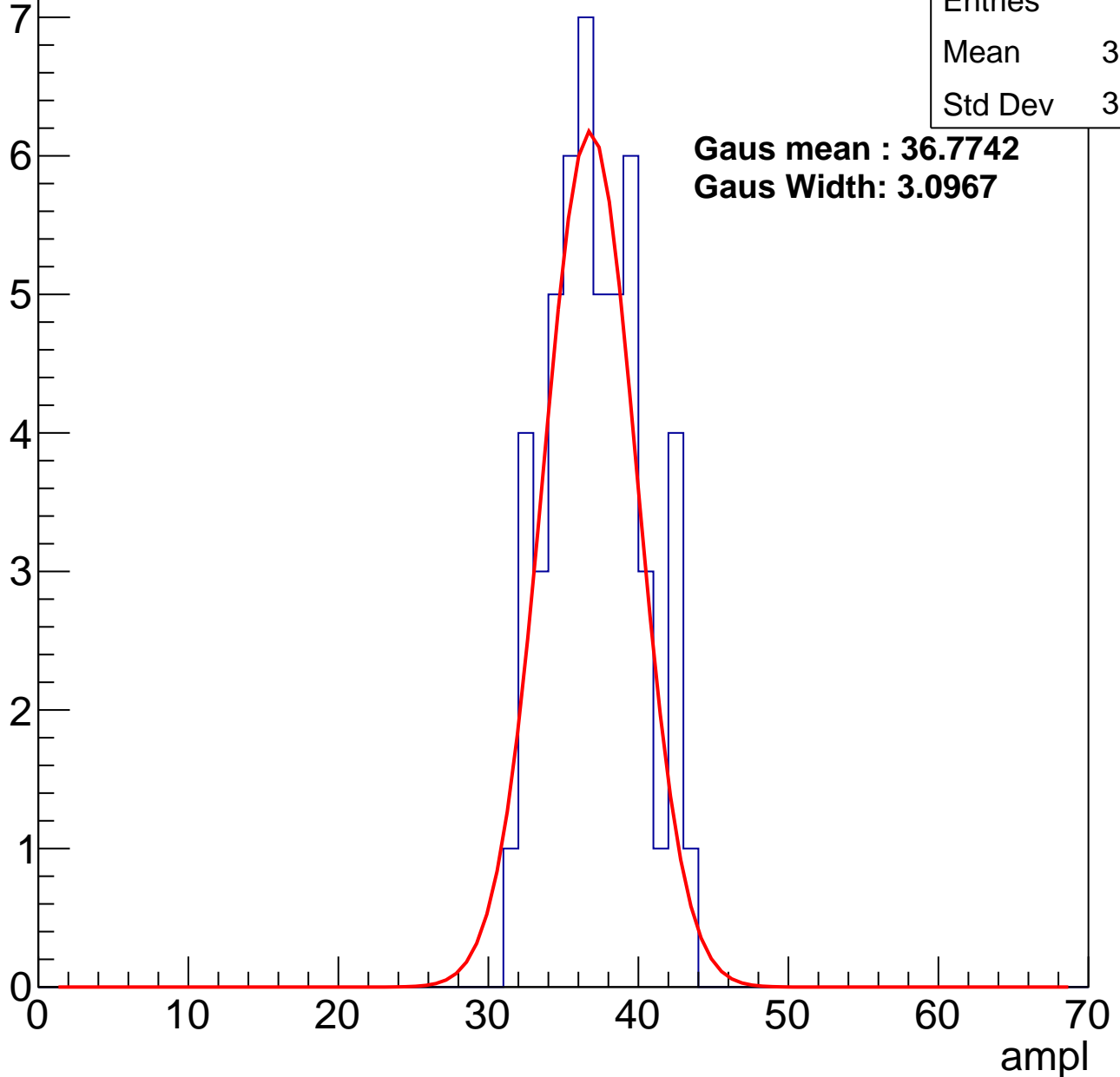
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	51
Mean	36.69
Std Dev	3.013

**Gaus mean : 36.7742**

**Gaus Width: 3.0967**



# B0L001S, U10-ch47, adc2

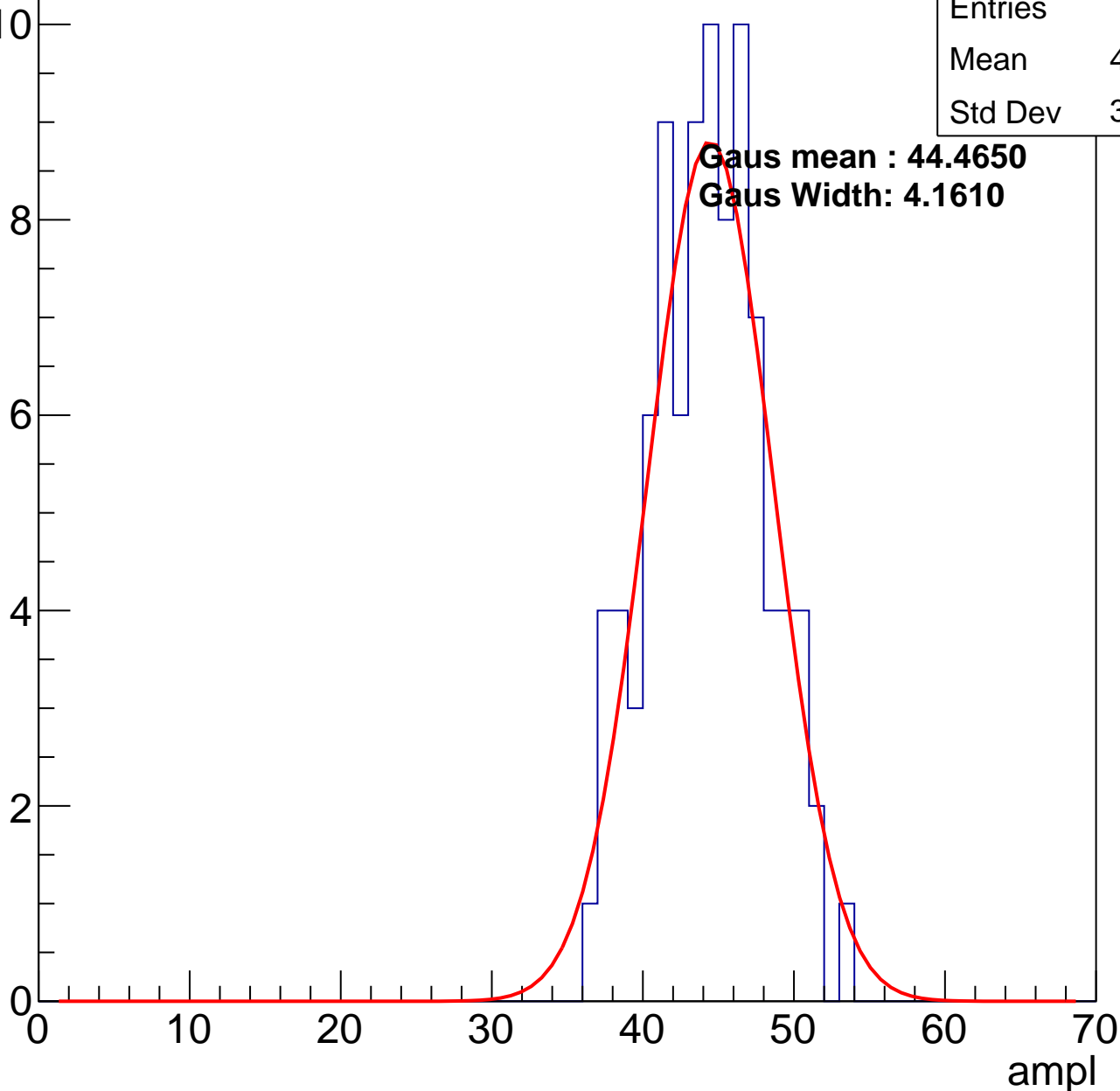
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	92
Mean	43.84
Std Dev	3.737

**Gaus mean : 44.4650**

**Gaus Width: 4.1610**

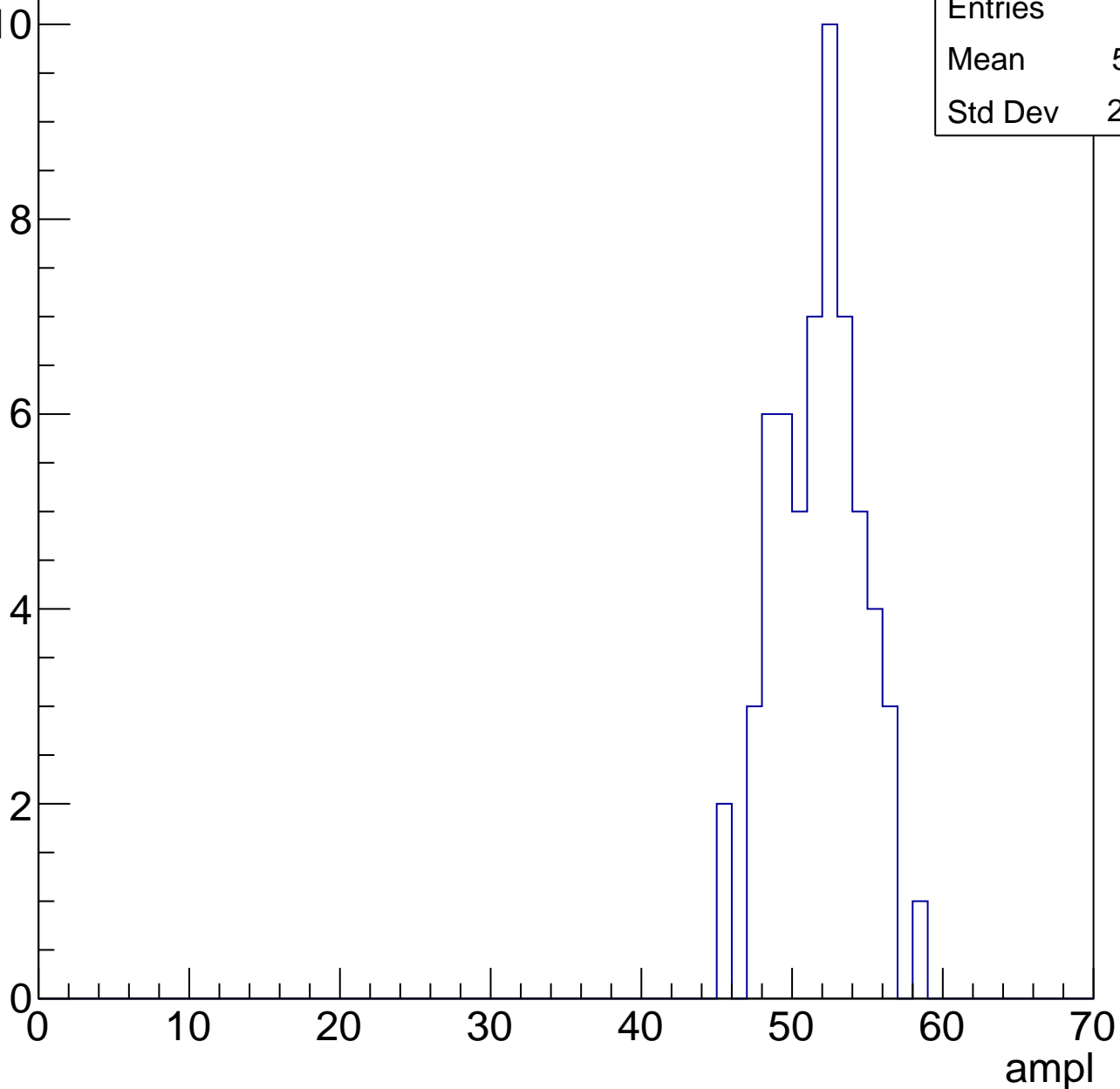


# B0L001S, U10-ch47, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

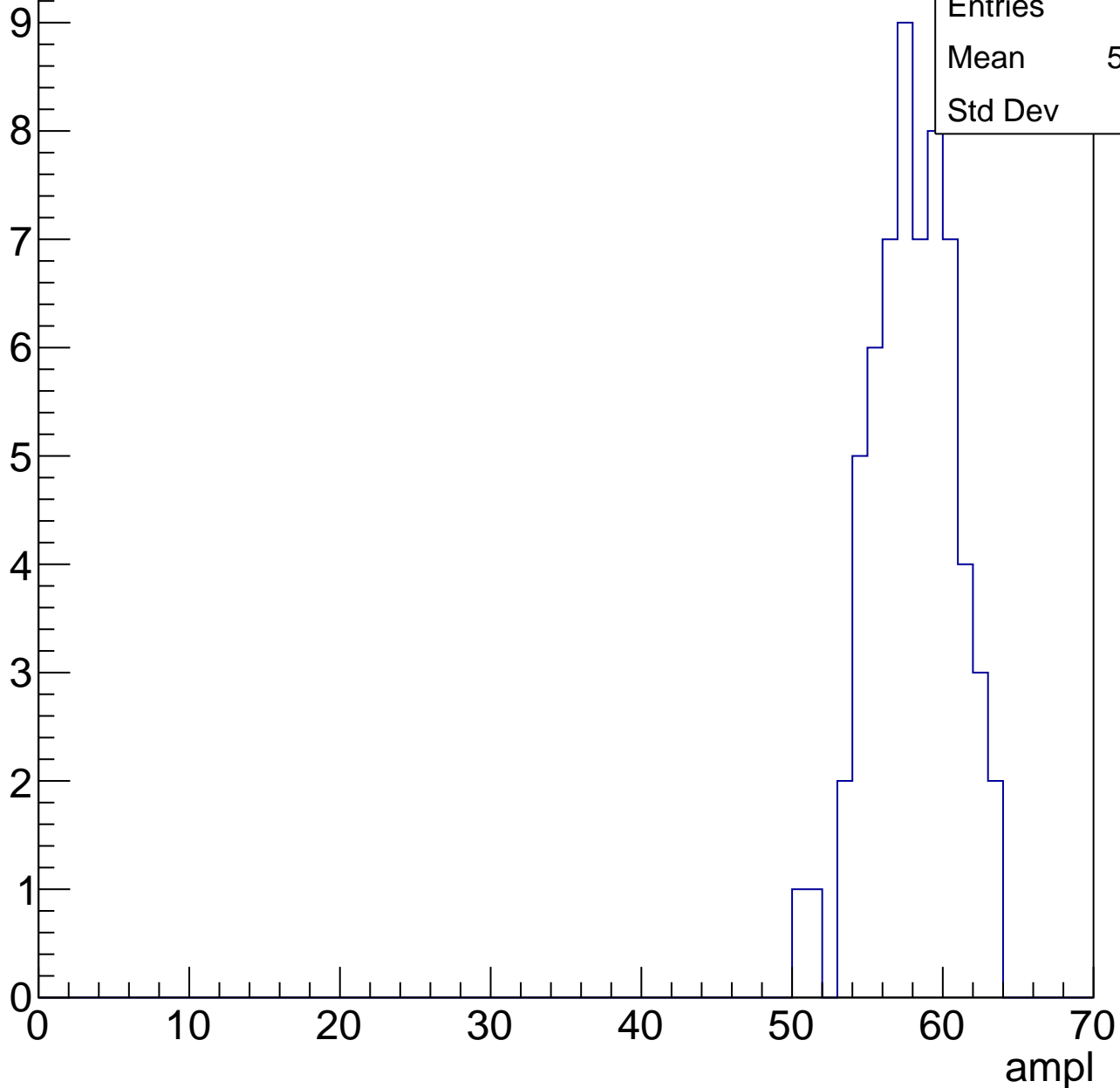
Entries	59
Mean	51.31
Std Dev	2.818



# B0L001S, U10-ch47, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



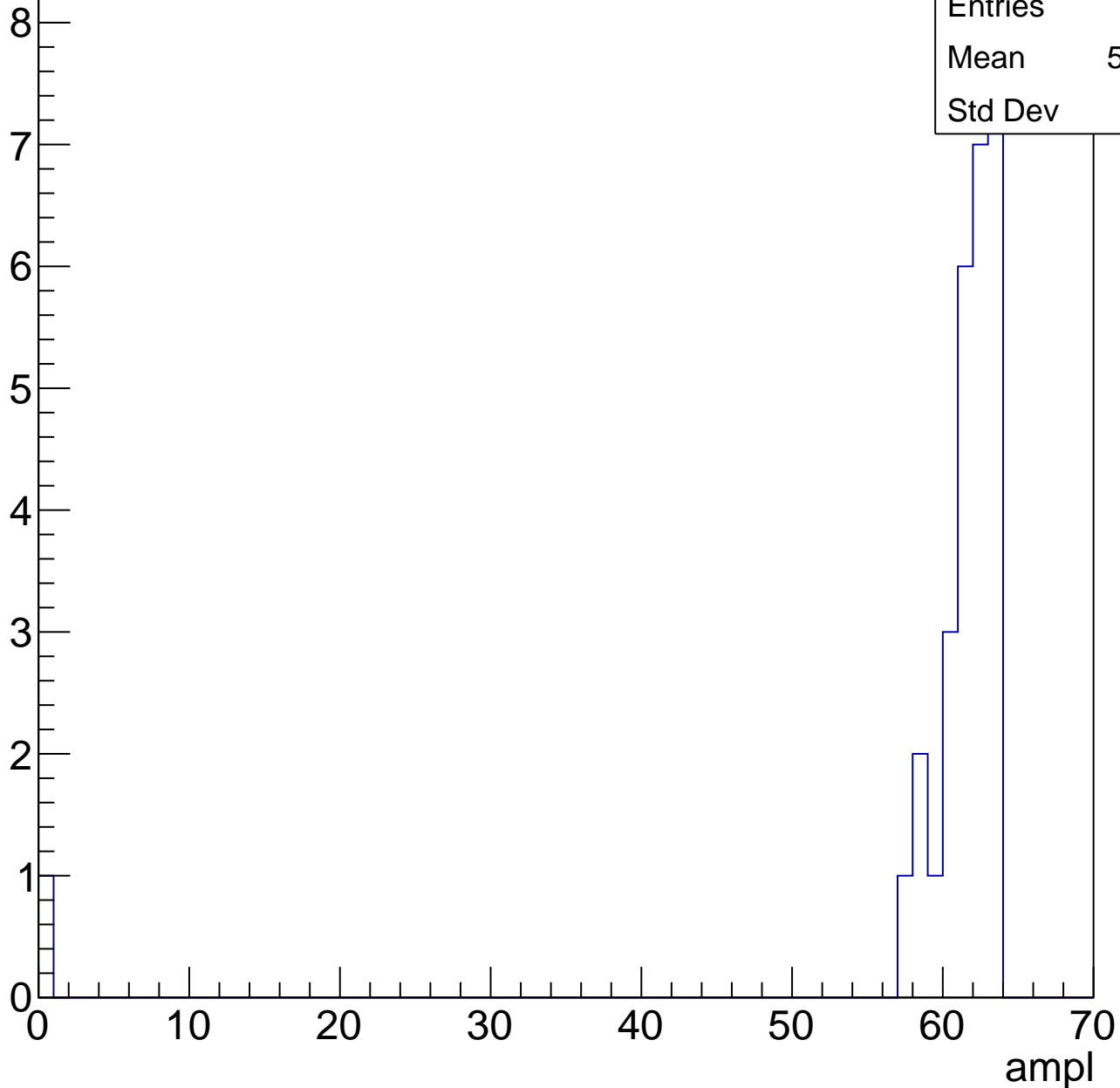
Entries	62
Mean	57.52
Std Dev	2.81

# B0L001S, U10-ch47, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	29
Mean	59.17
Std Dev	11.3



# B0L001S, U10-ch47, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

0 10 20 30 40 50 60 70

ampl

Entries	1
Mean	59
Std Dev	0



# B0L001S, U10-ch47, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U10-ch48, adc0

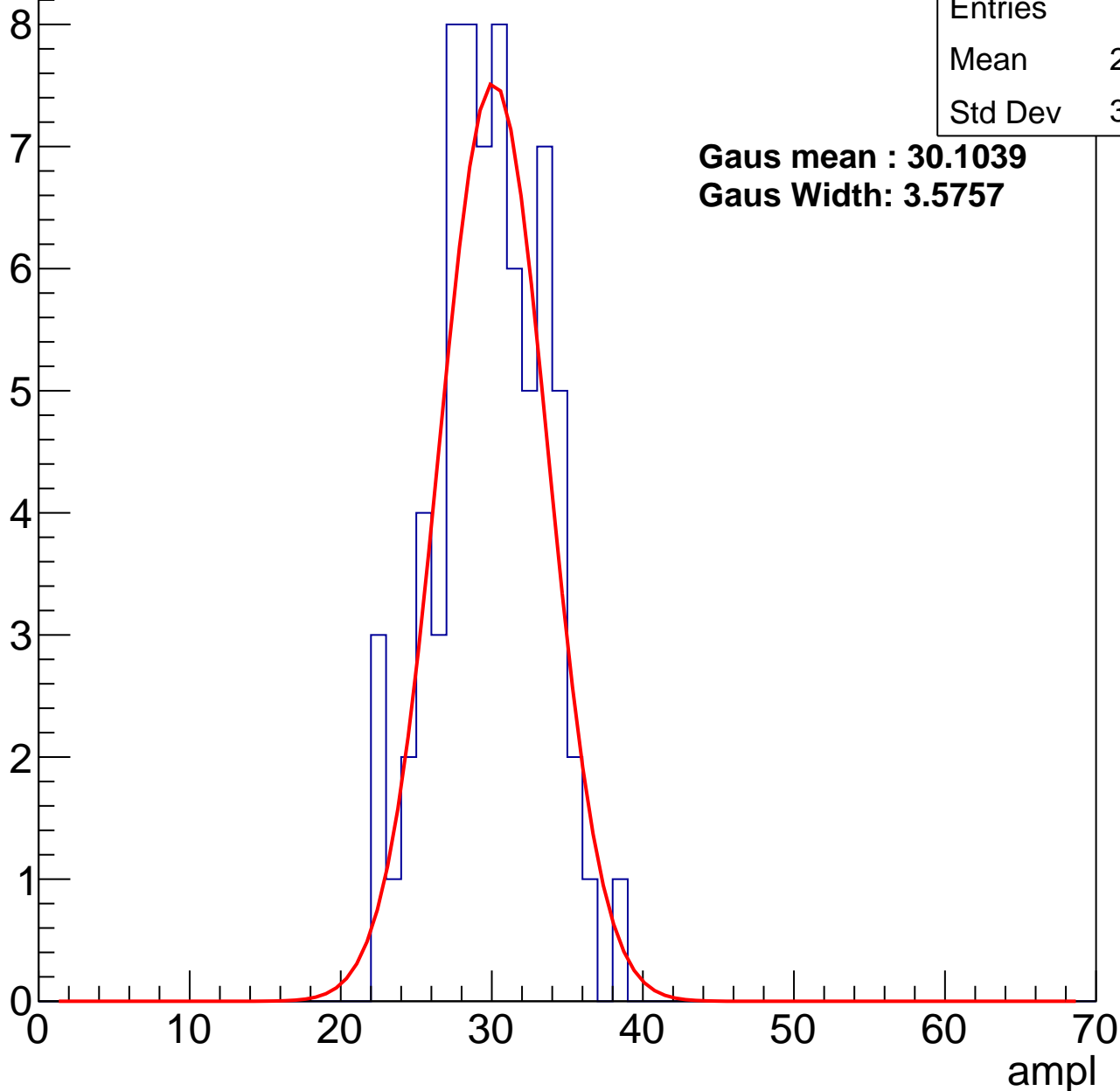
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	29.42
Std Dev	3.495

**Gaus mean : 30.1039**

**Gaus Width: 3.5757**



# B0L001S, U10-ch48, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	74
Mean	36.14
Std Dev	4.114

**Gaus mean : 36.4982**

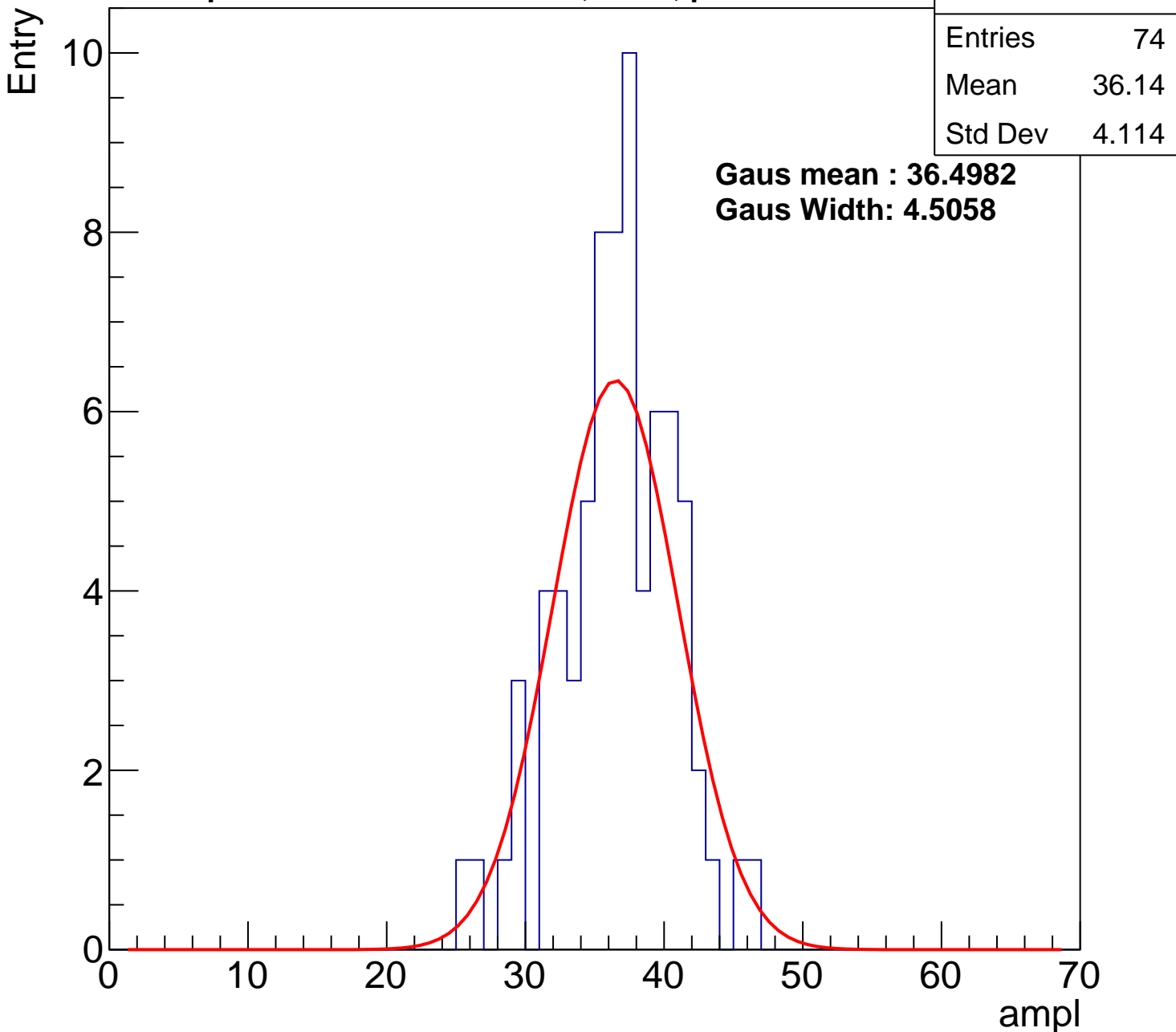
**Gaus Width: 4.5058**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U10-ch48, adc2

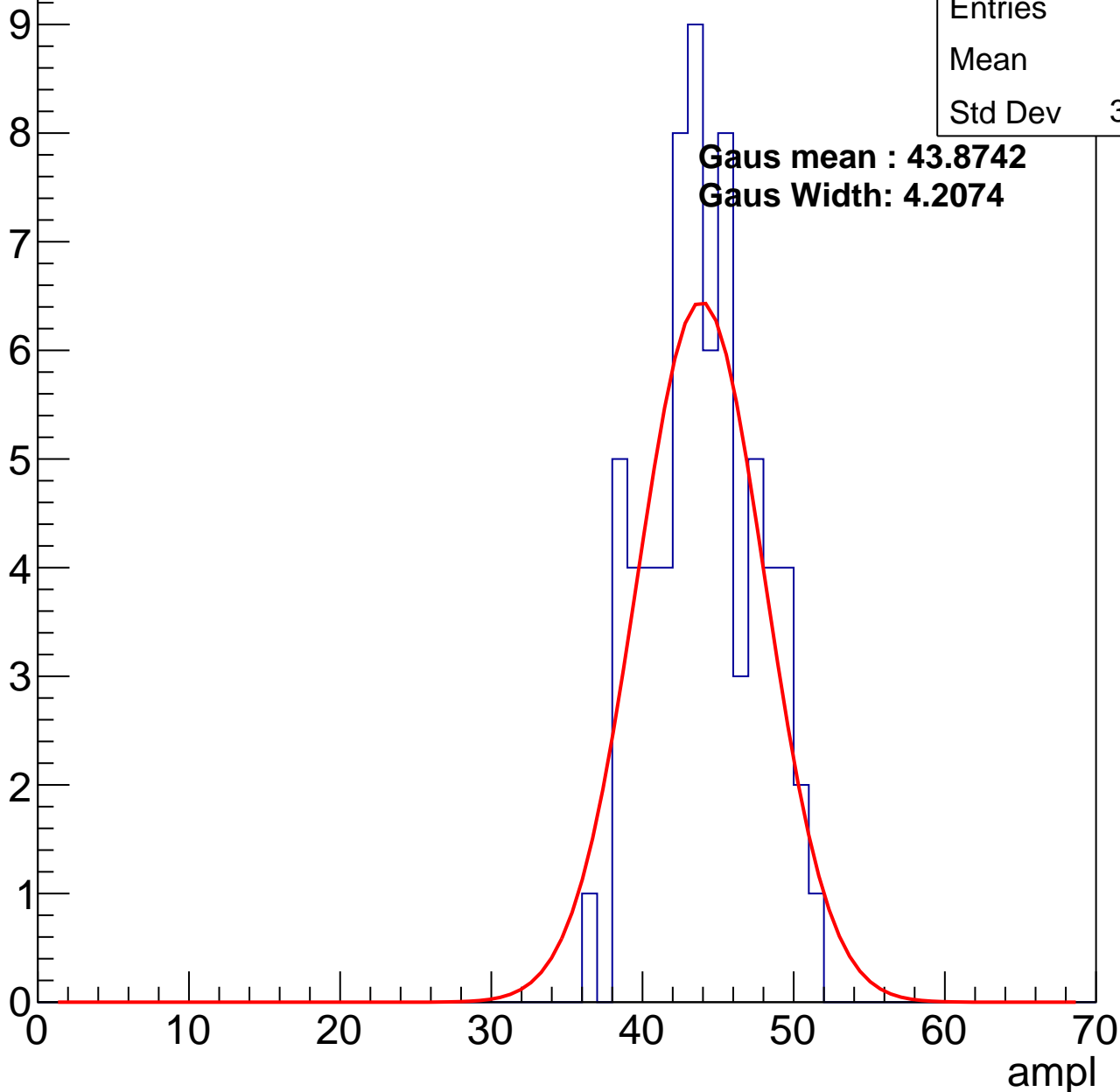
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	43.6
Std Dev	3.482

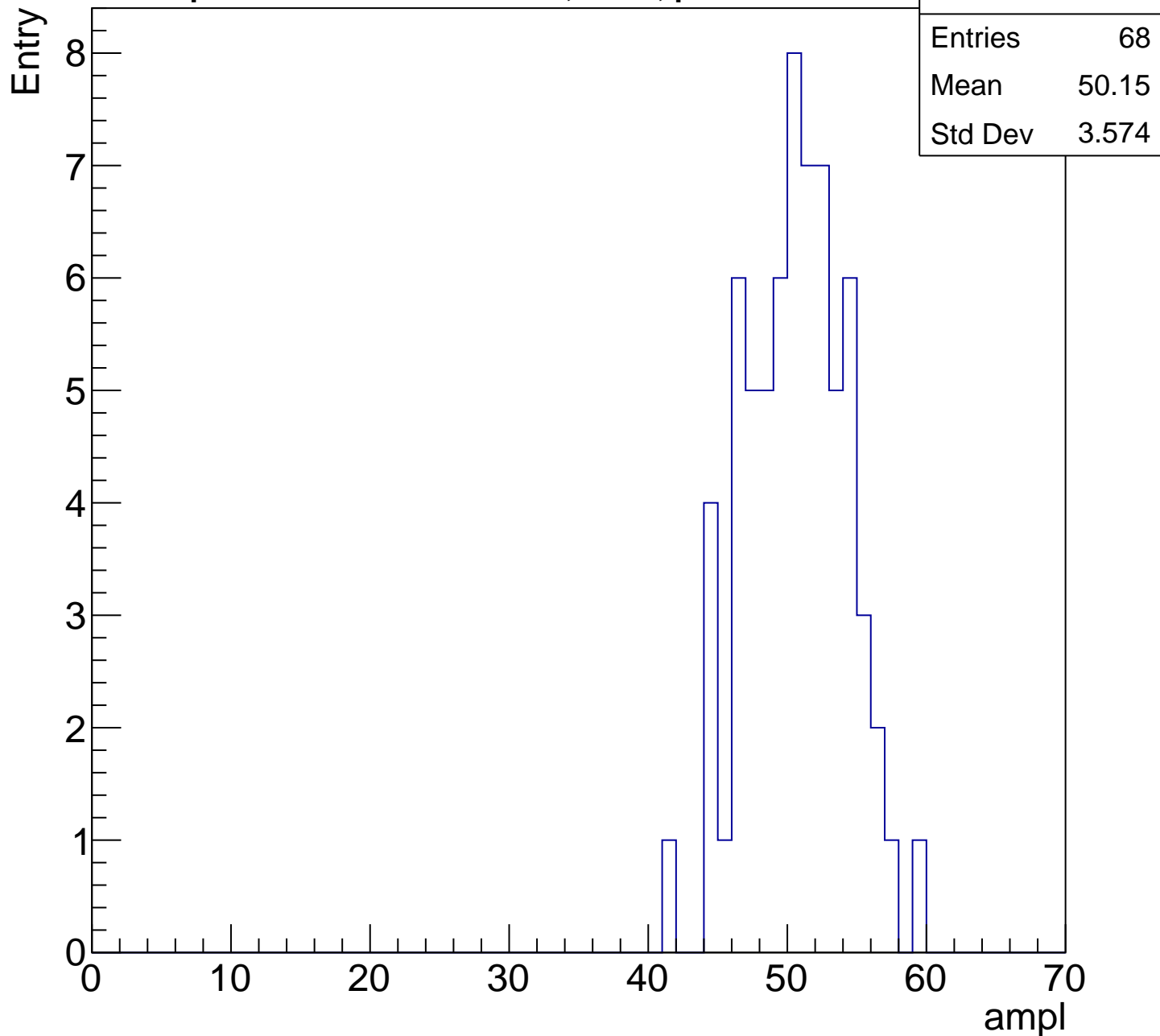
**Gaus mean : 43.8742**

**Gaus Width: 4.2074**



# B0L001S, U10-ch48, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

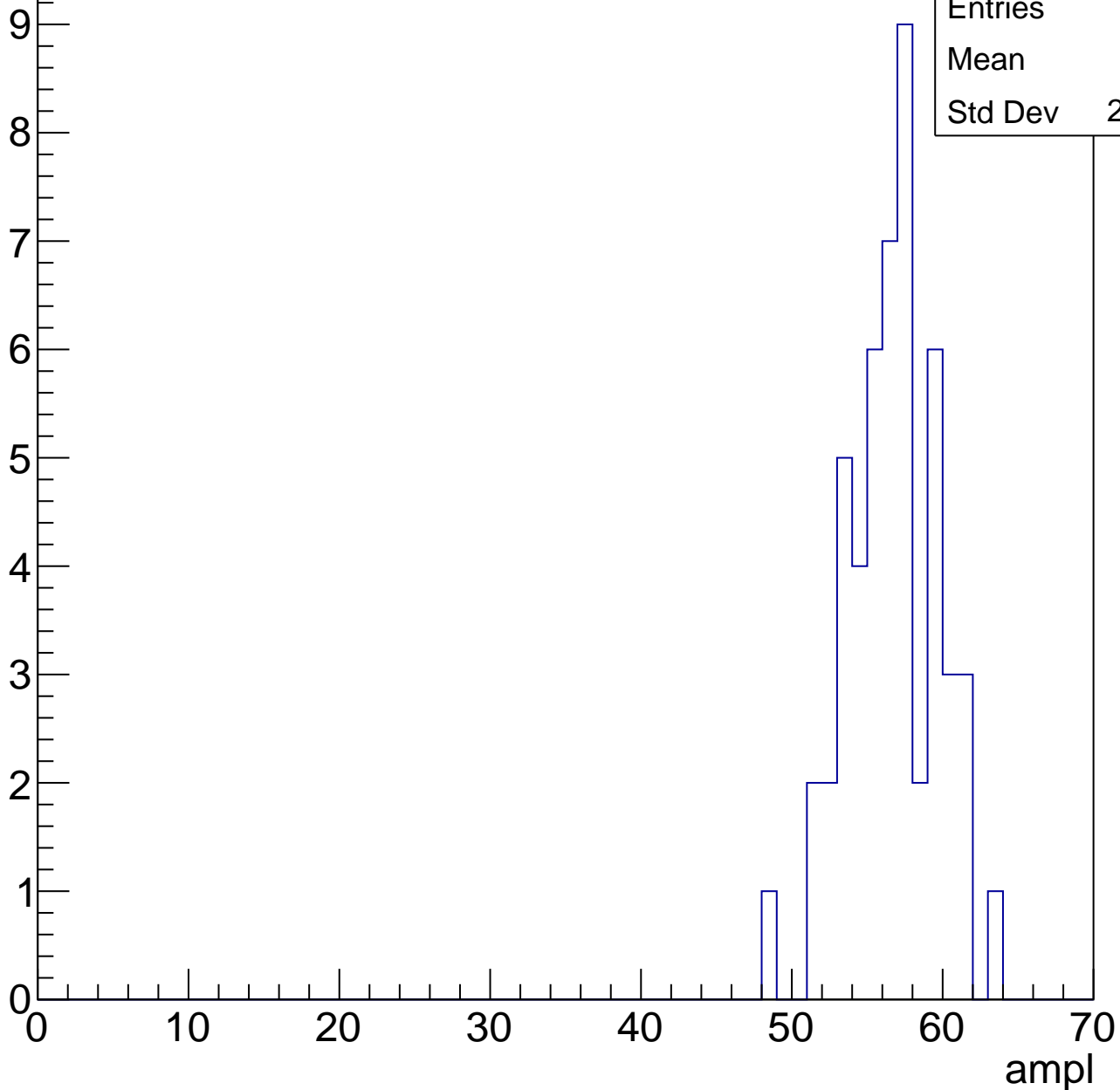


# B0L001S, U10-ch48, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	51
Mean	56.2
Std Dev	2.984

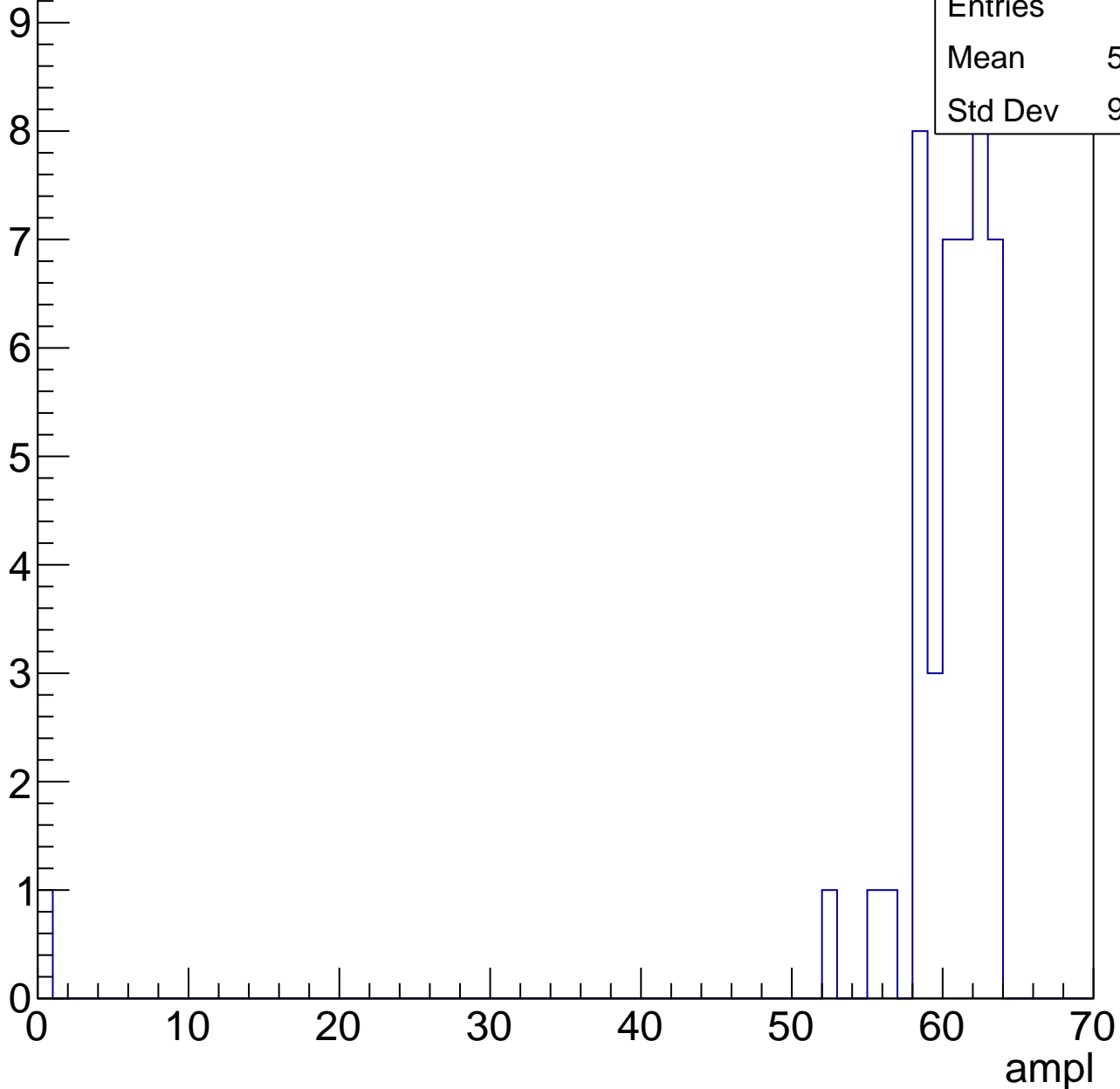


# B0L001S, U10-ch48, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	45
Mean	58.89
Std Dev	9.178



# B0L001S, U10-ch48, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.67
Std Dev	0.4714

ampl

0 10 20 30 40 50 60 70



# B0L001S, U10-ch48, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U10-ch49, adc0

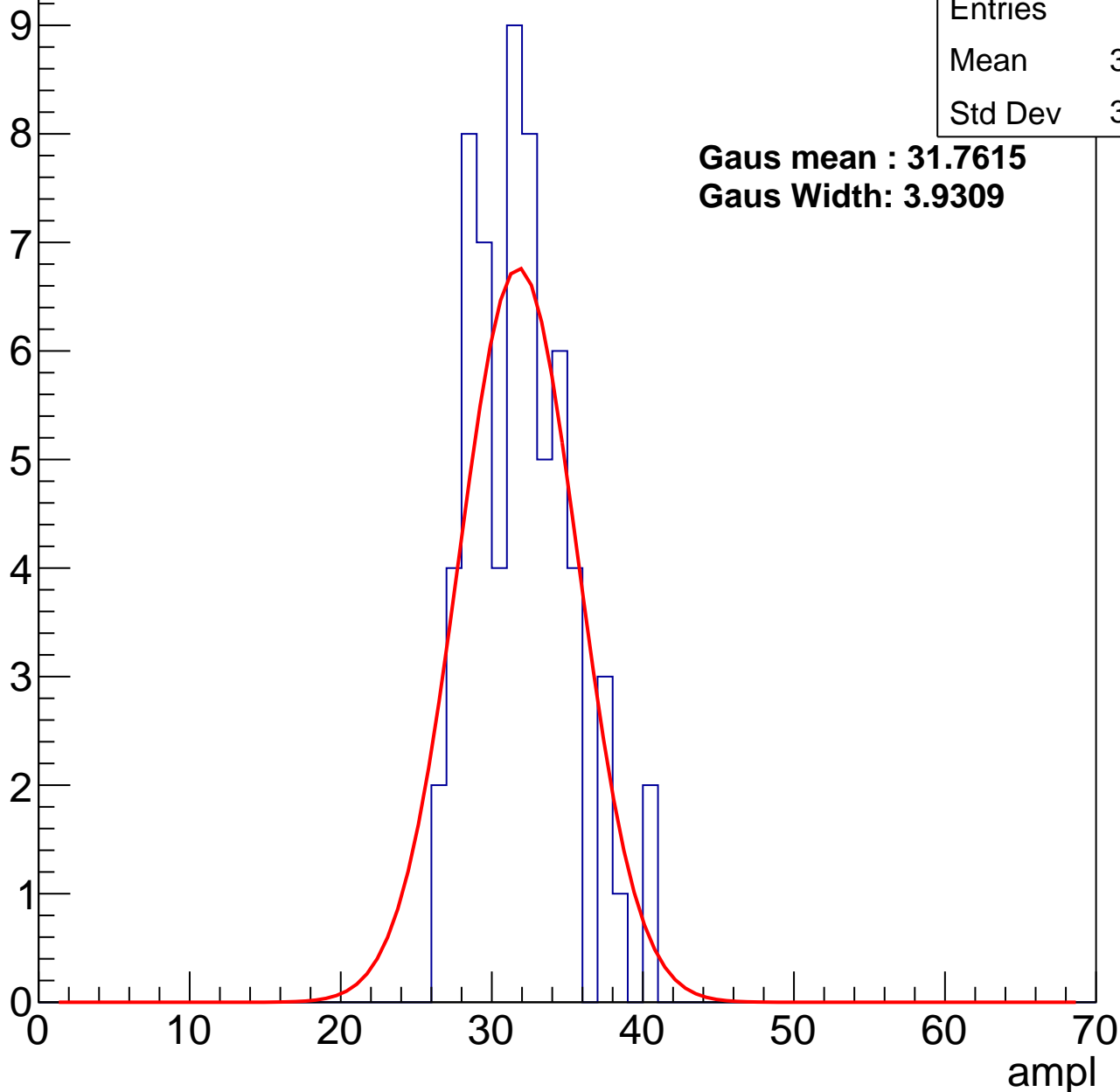
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	31.43
Std Dev	3.265

**Gaus mean : 31.7615**

**Gaus Width: 3.9309**



# B0L001S, U10-ch49, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	72
Mean	38.15
Std Dev	3.623

**Gaus mean : 38.3520**

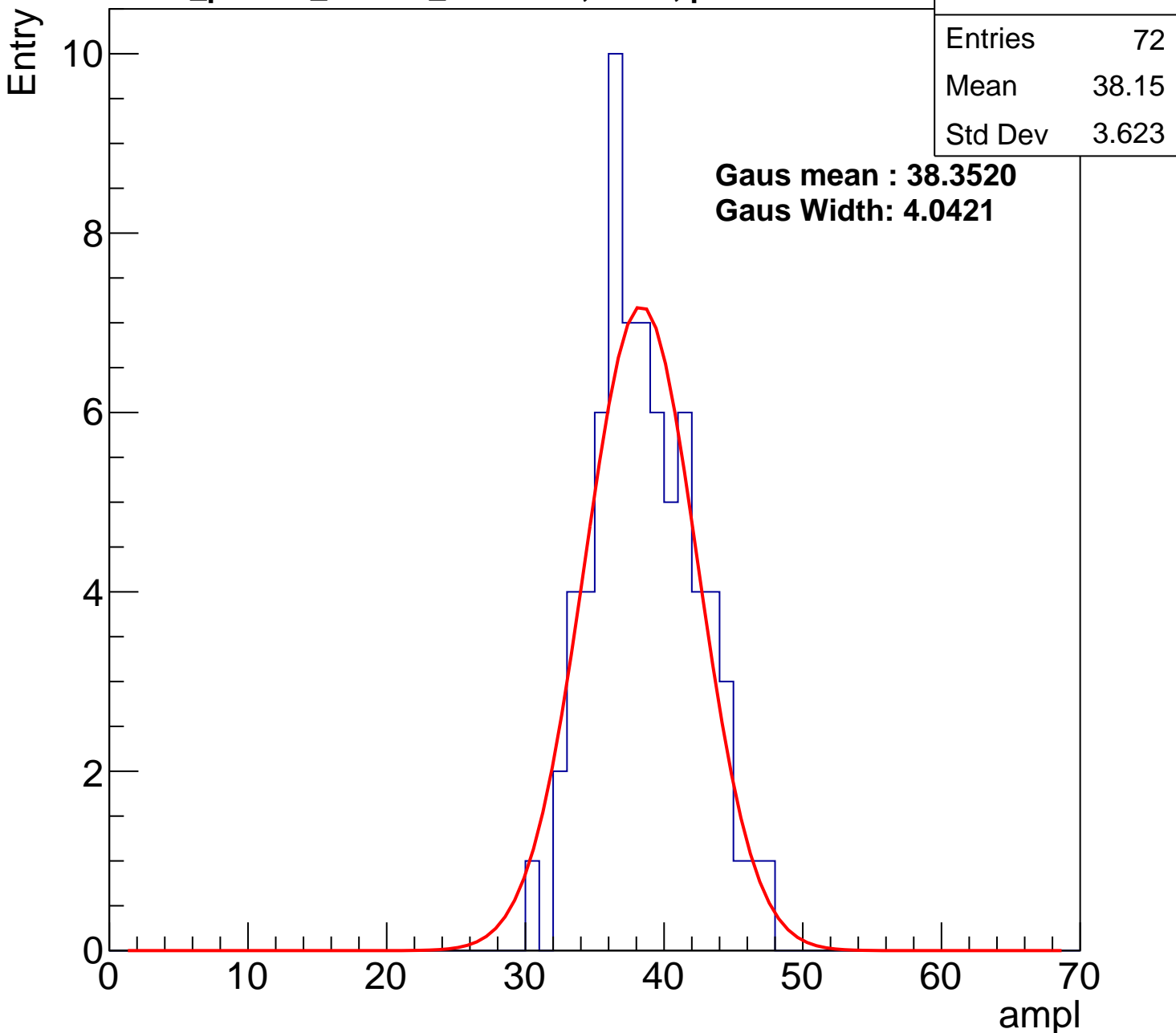
**Gaus Width: 4.0421**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U10-ch49, adc2

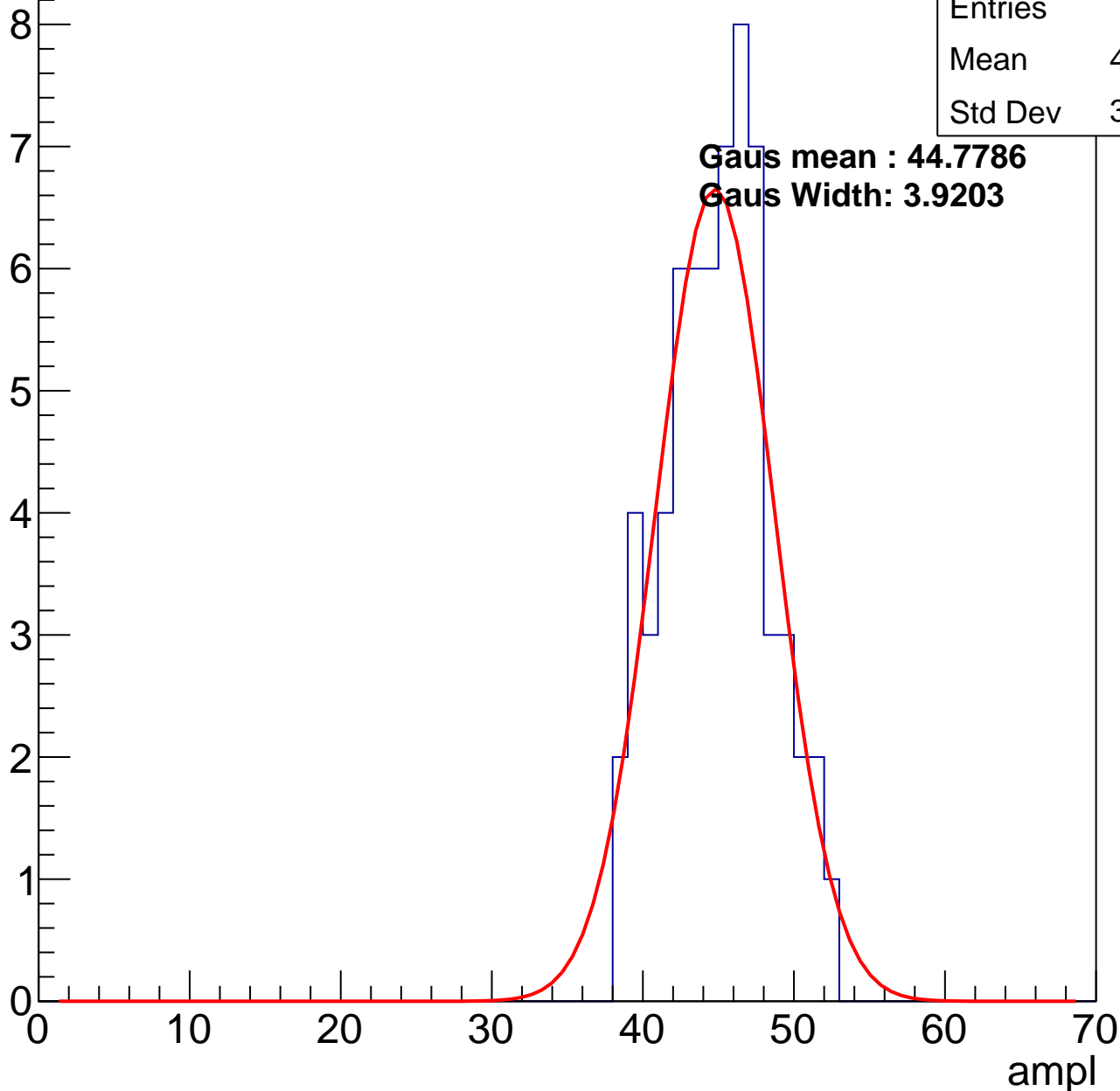
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	44.48
Std Dev	3.377

Gaus mean : 44.7786

Gaus Width: 3.9203

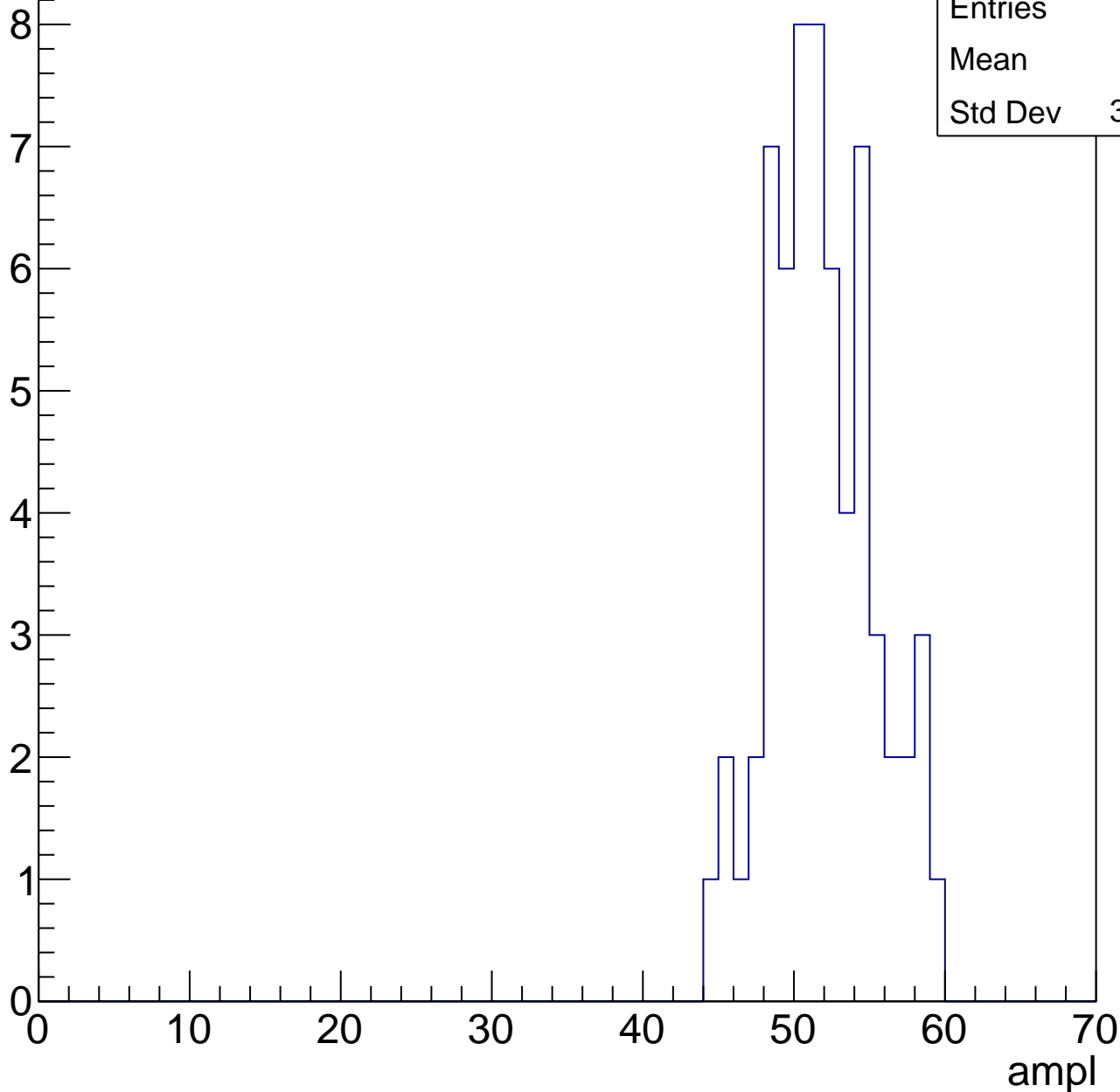


# B0L001S, U10-ch49, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

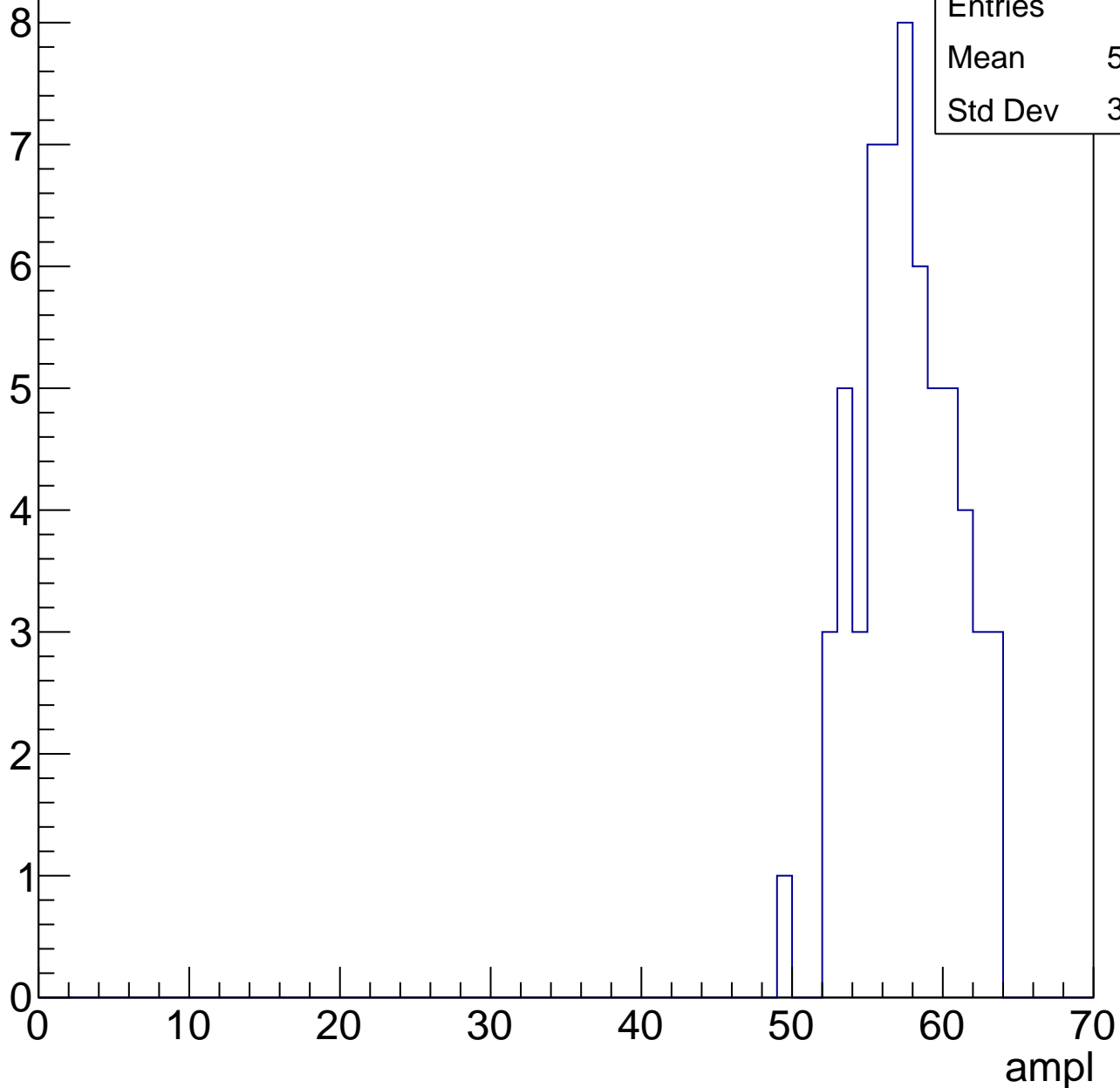
Entries	63
Mean	51.4
Std Dev	3.402



# B0L001S, U10-ch49, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

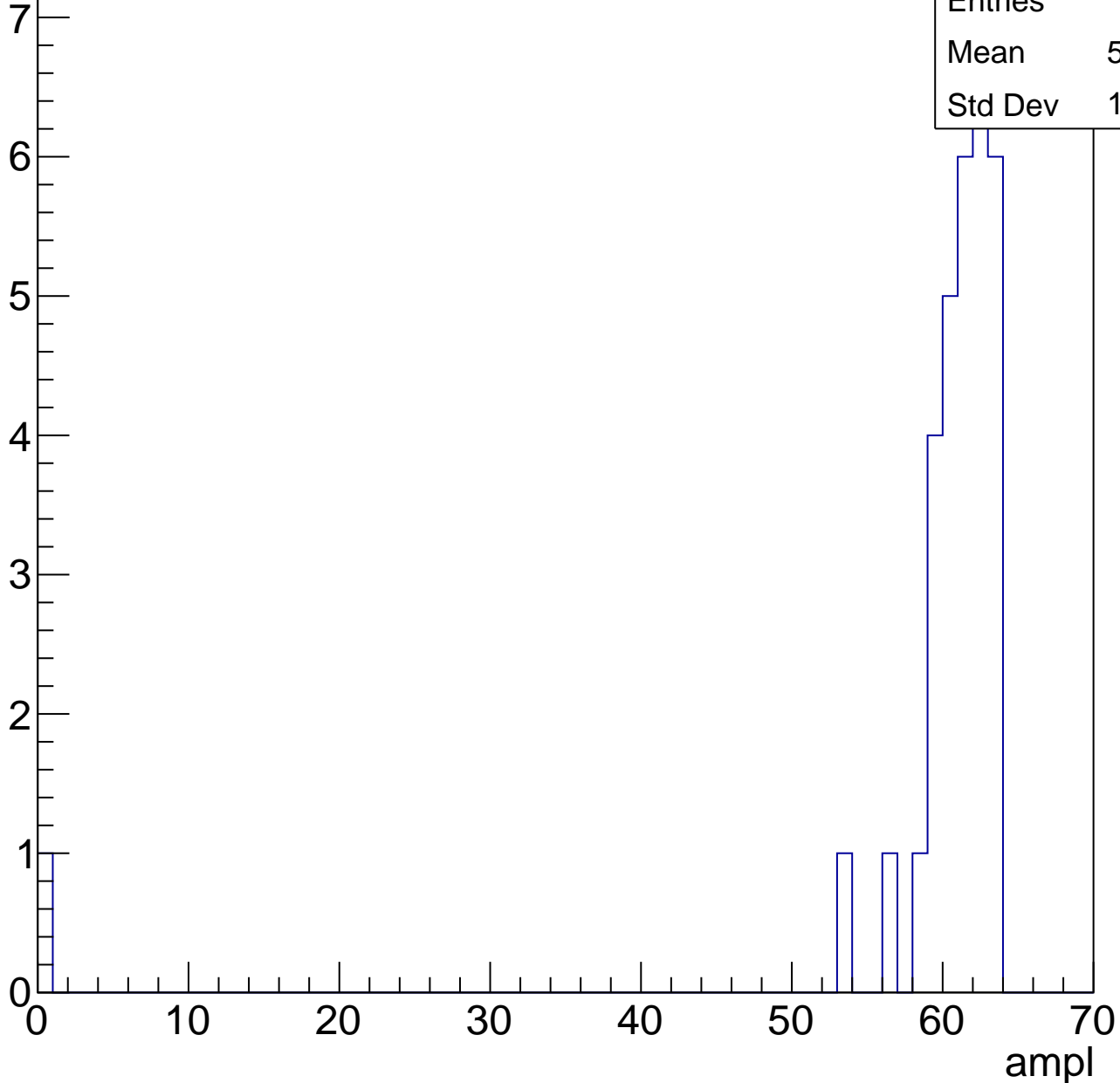


# B0L001S, U10-ch49, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	32
Mean	58.78
Std Dev	10.77



# B0L001S, U10-ch49, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

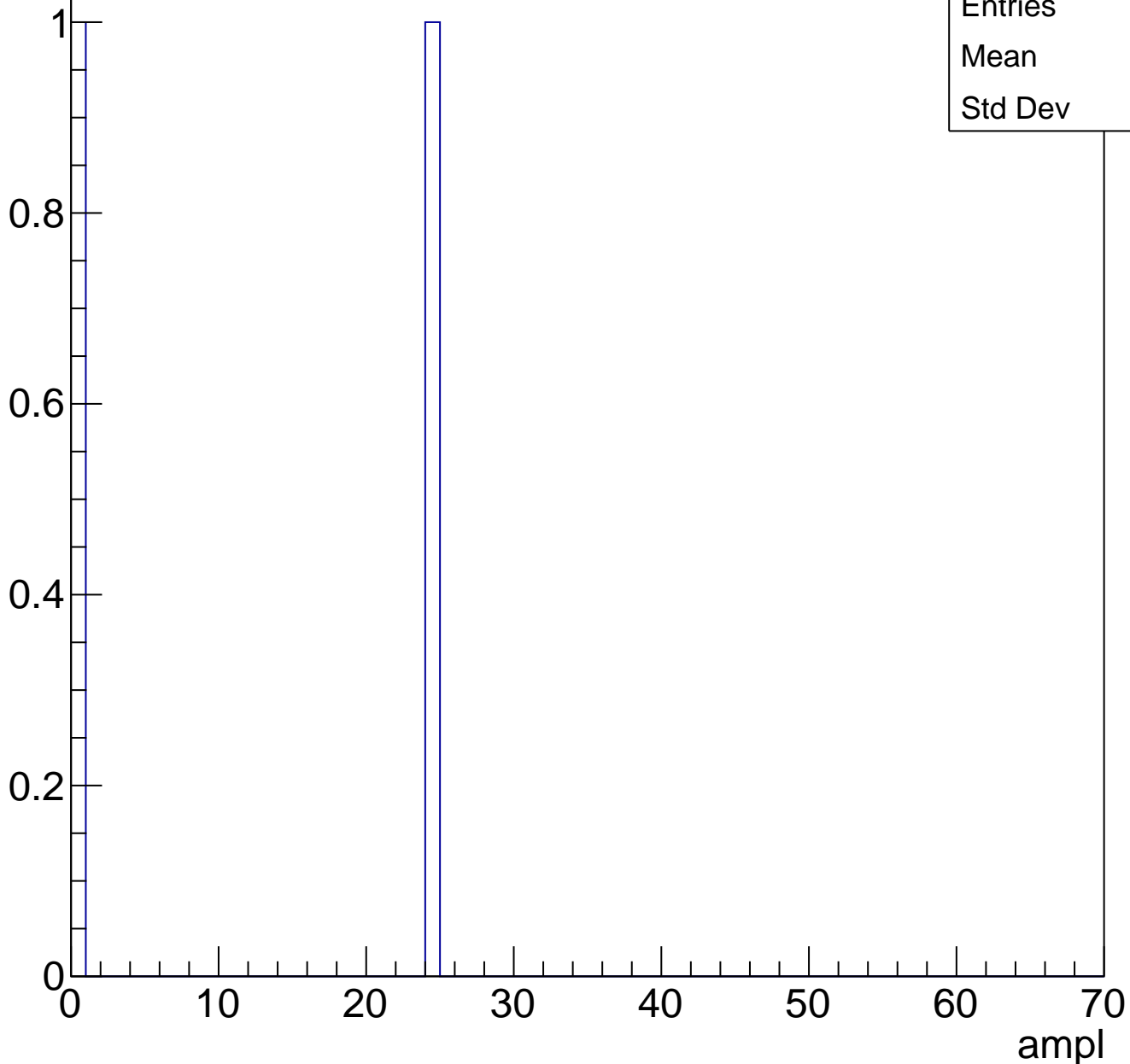




# B0L001S, U10-ch49, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U10-ch50, adc0

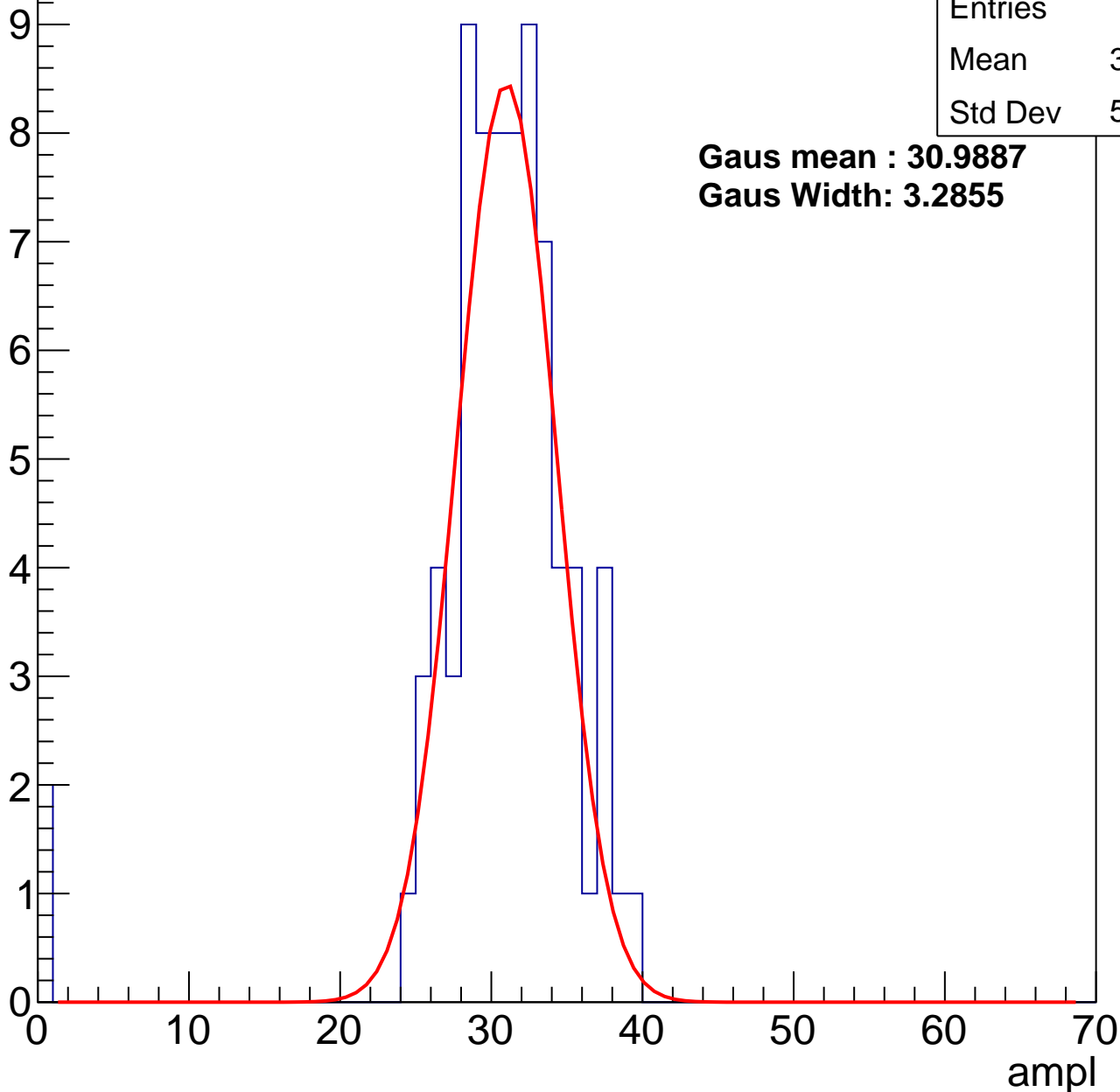
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	77
Mean	30.03
Std Dev	5.915

**Gaus mean : 30.9887**

**Gaus Width: 3.2855**



# B0L001S, U10-ch50, adc1

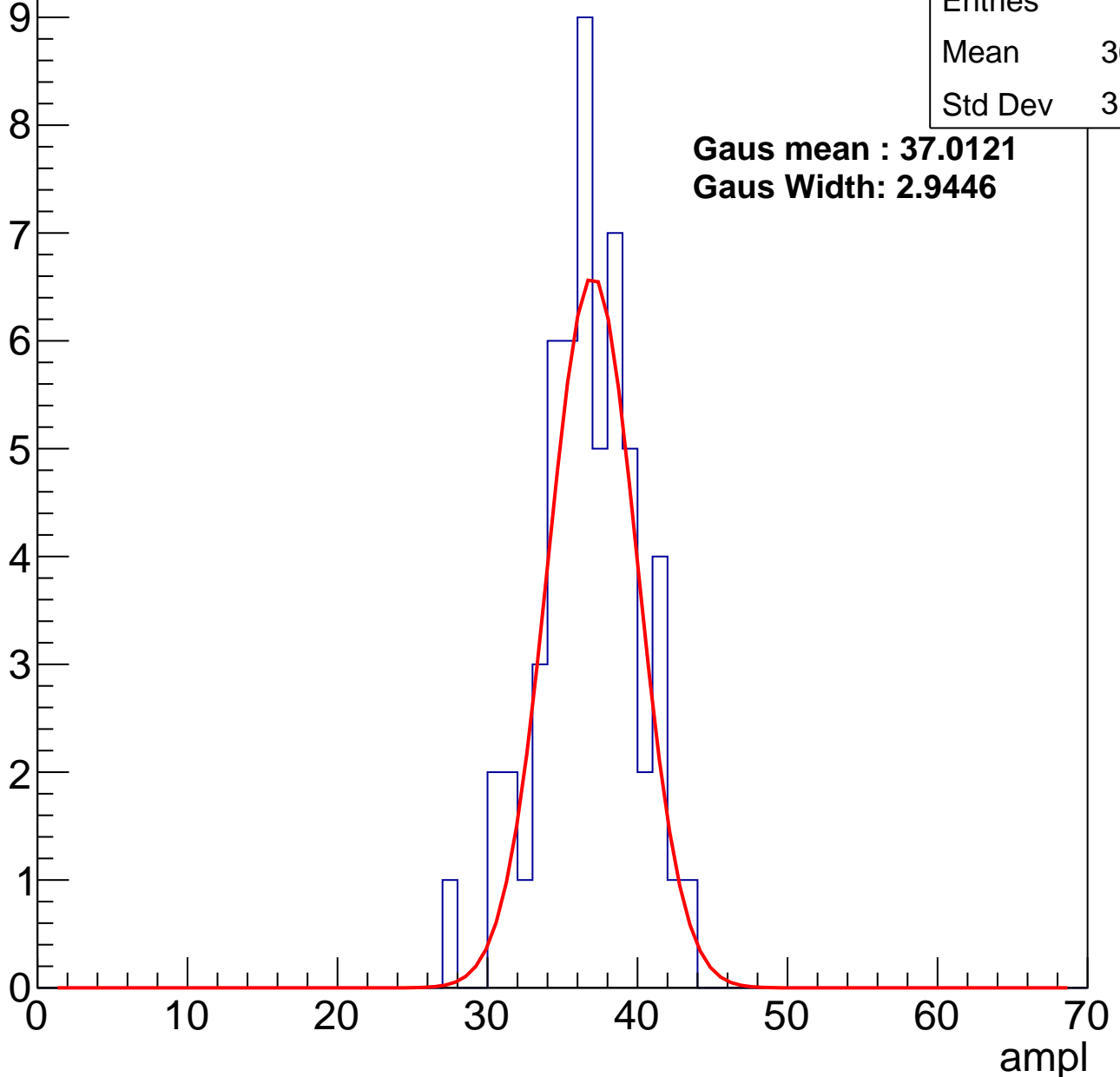
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	36.24
Std Dev	3.213

**Gaus mean : 37.0121**

**Gaus Width: 2.9446**



# B0L001S, U10-ch50, adc2

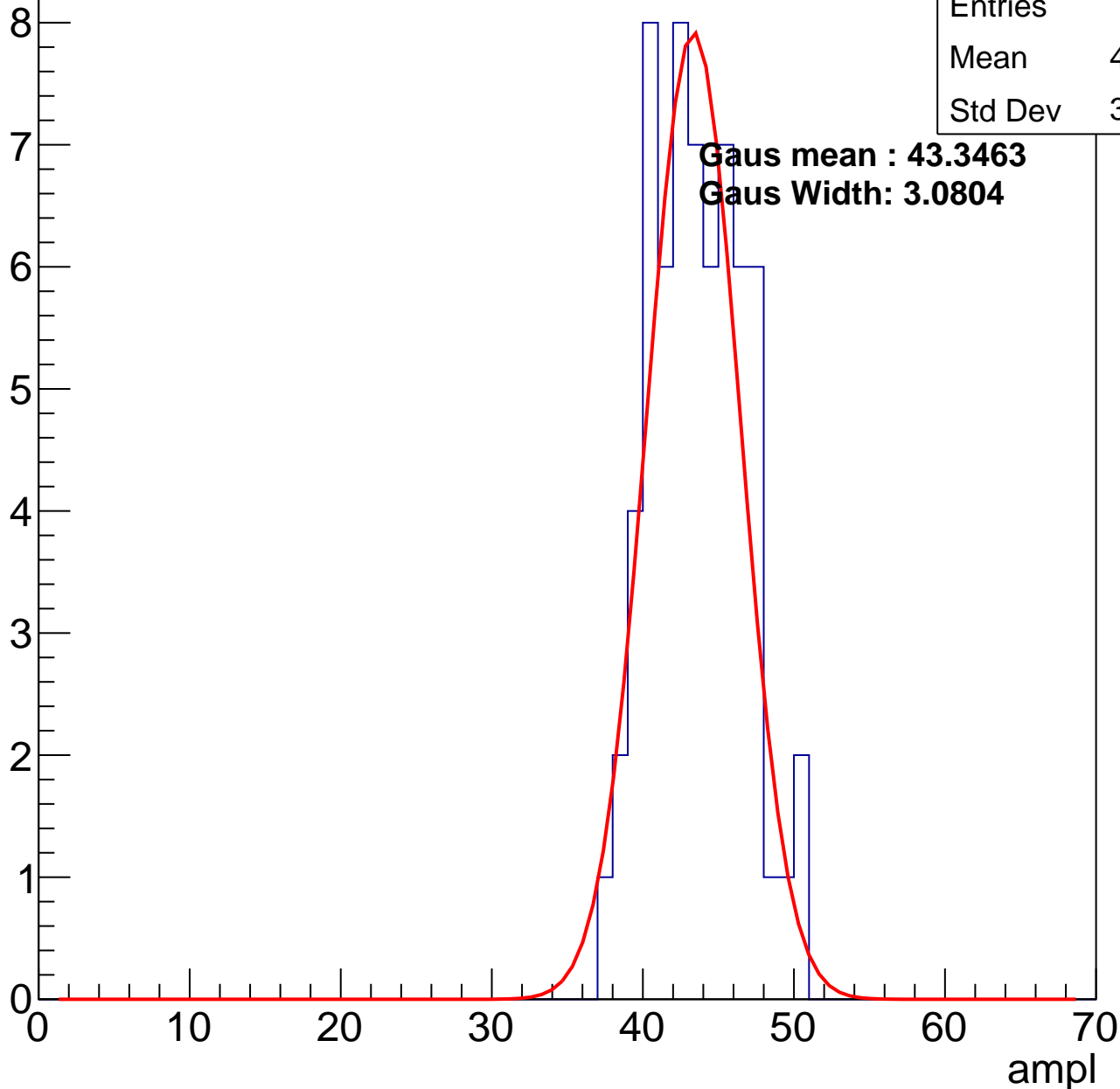
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	43.17
Std Dev	3.026

**Gaus mean : 43.3463**

**Gaus Width: 3.0804**

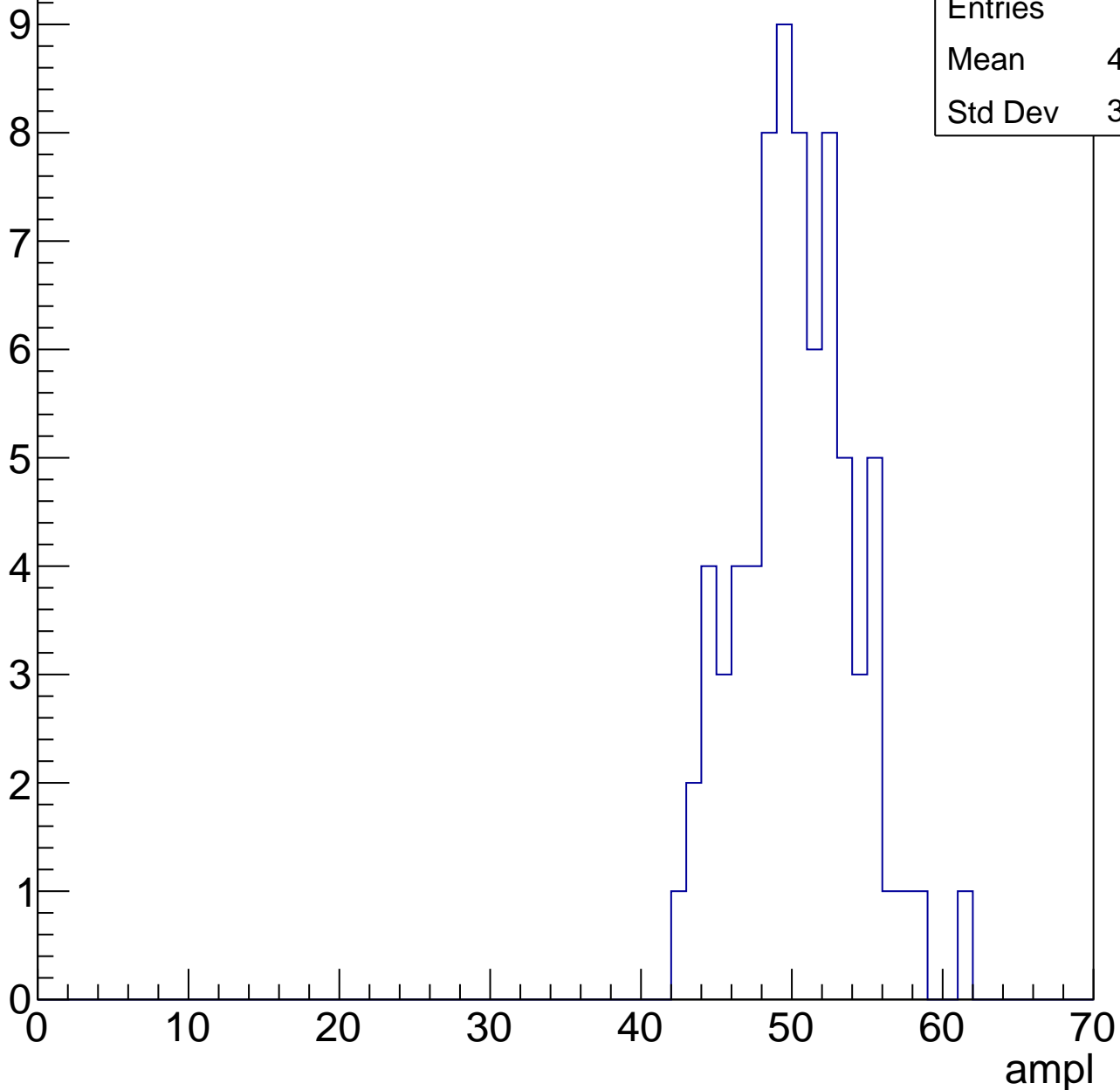


# B0L001S, U10-ch50, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

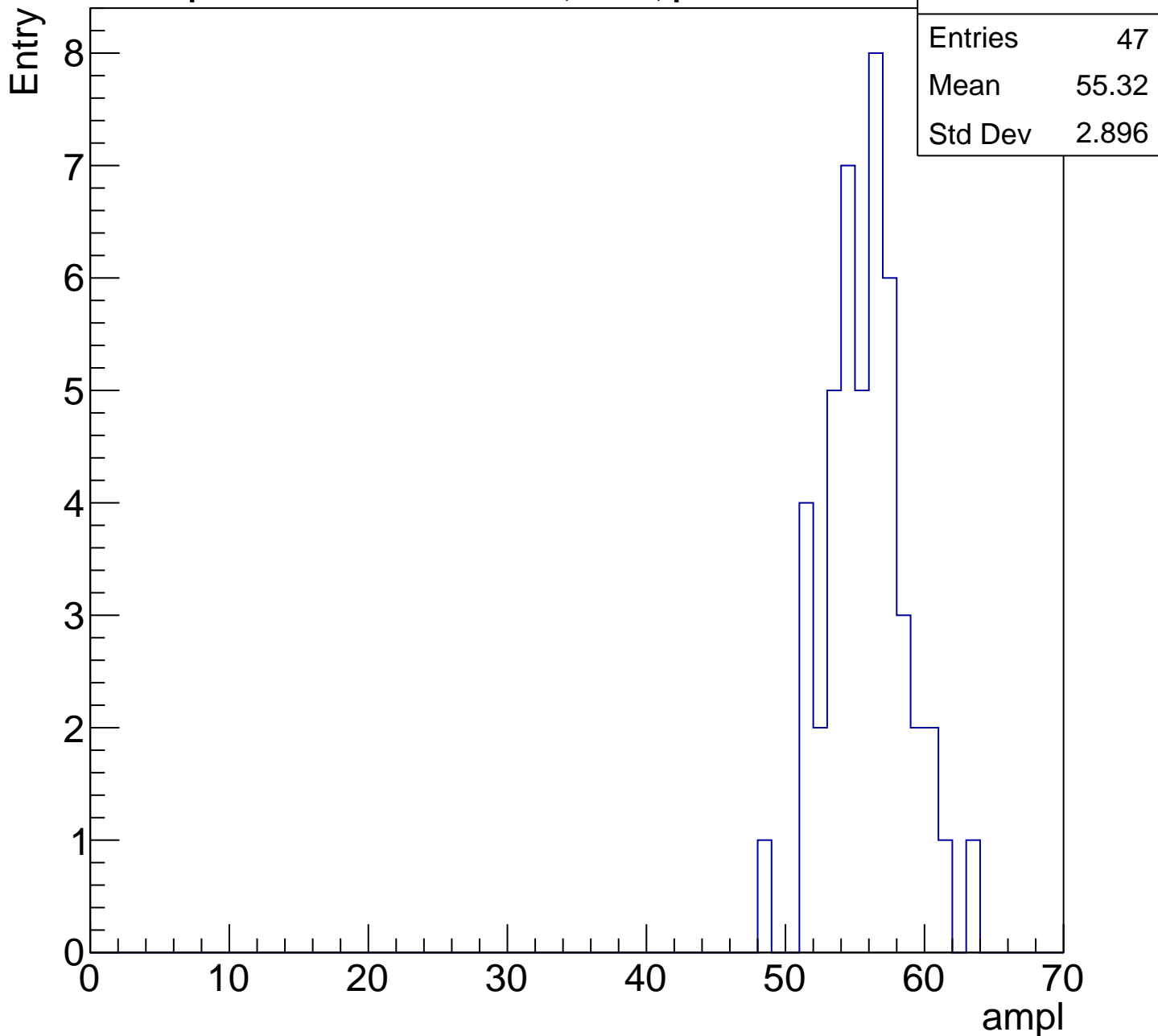
Entry

Entries	74
Mean	49.89
Std Dev	3.762



# B0L001S, U10-ch50, adc4

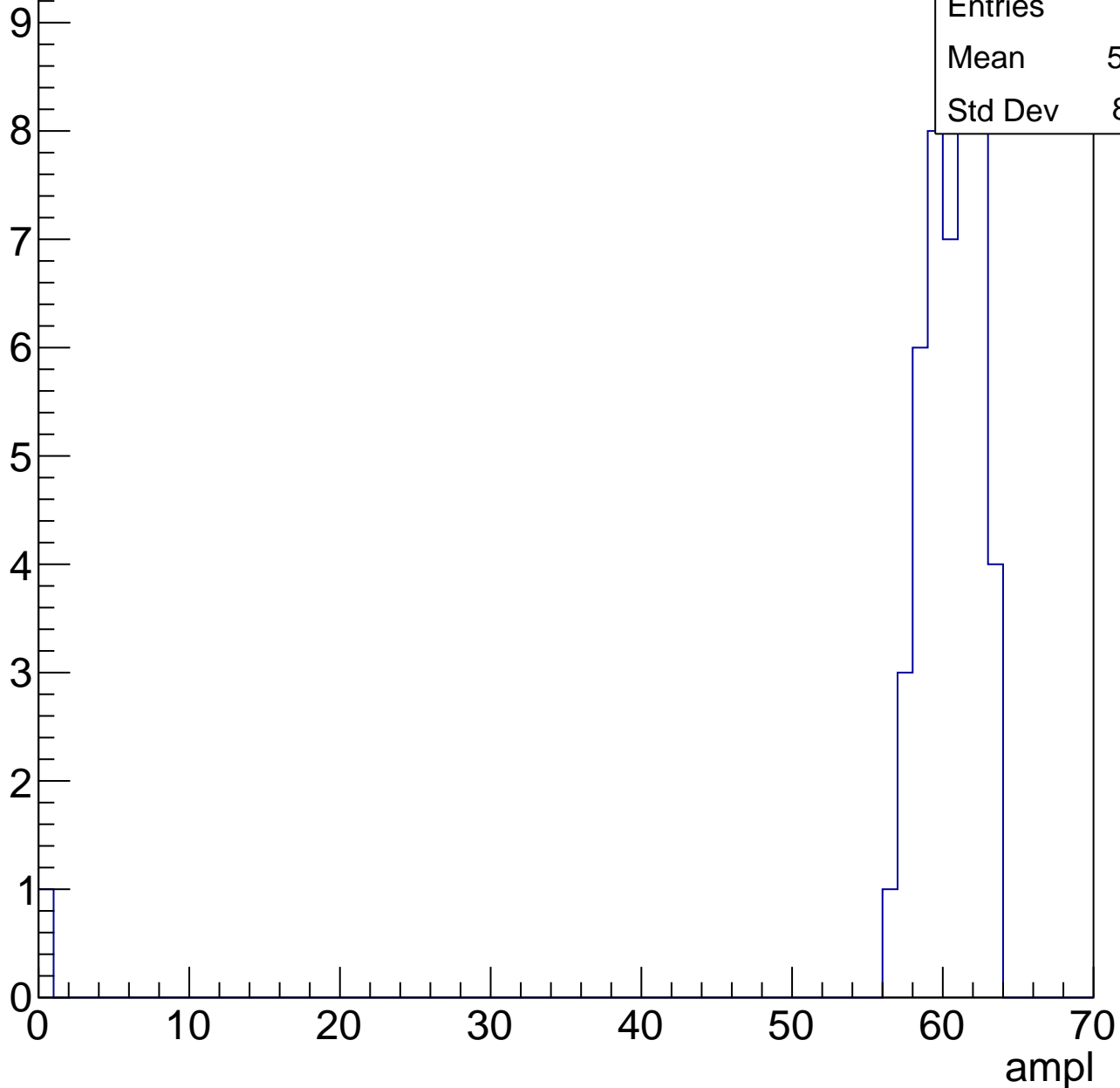
calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U10-ch50, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

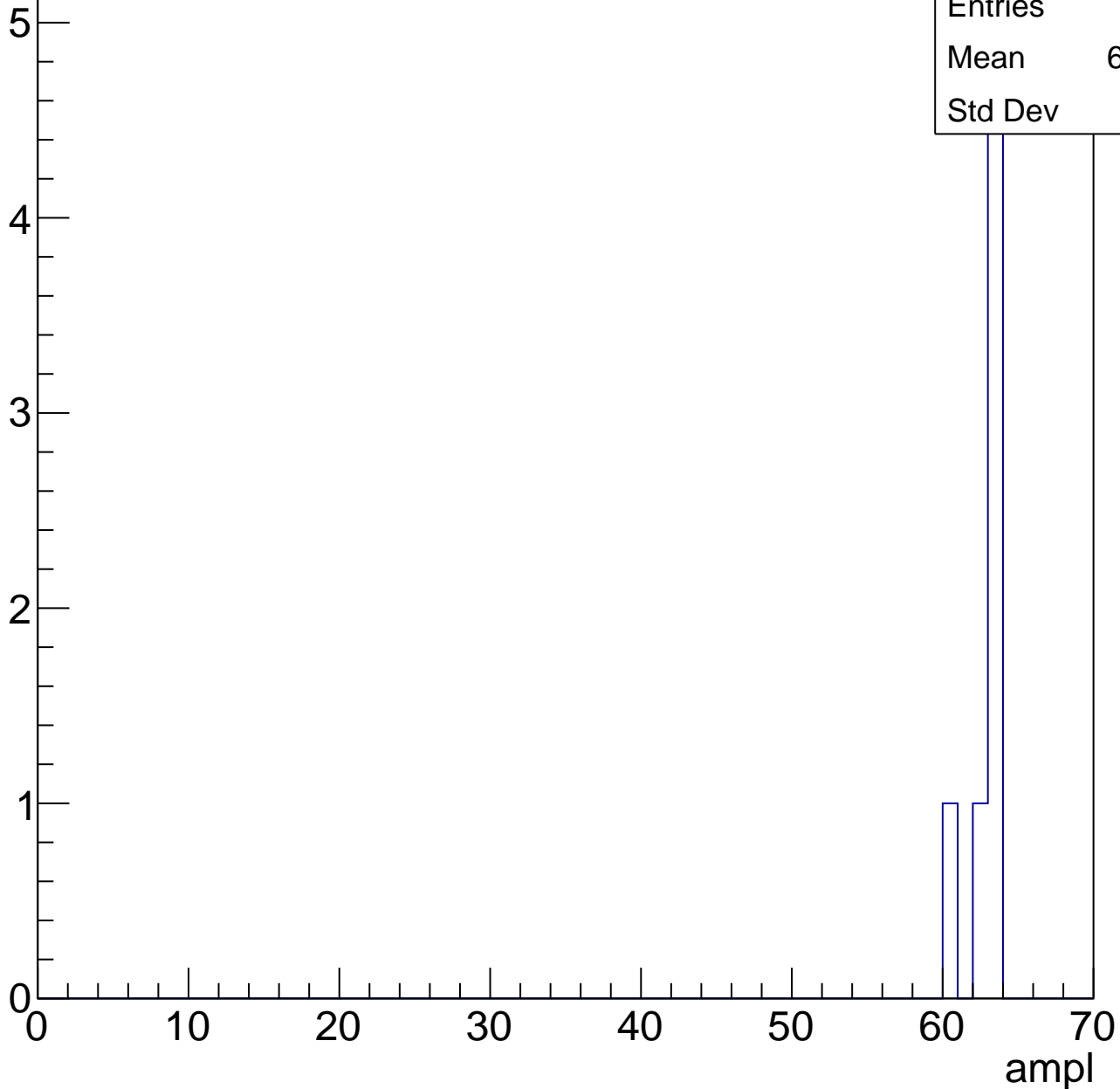


# B0L001S, U10-ch50, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	7
Mean	62.43
Std Dev	1.05





# B0L001S, U10-ch50, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	3
Mean	7.333
Std Dev	10.37

# B0L001S, U10-ch51, adc0

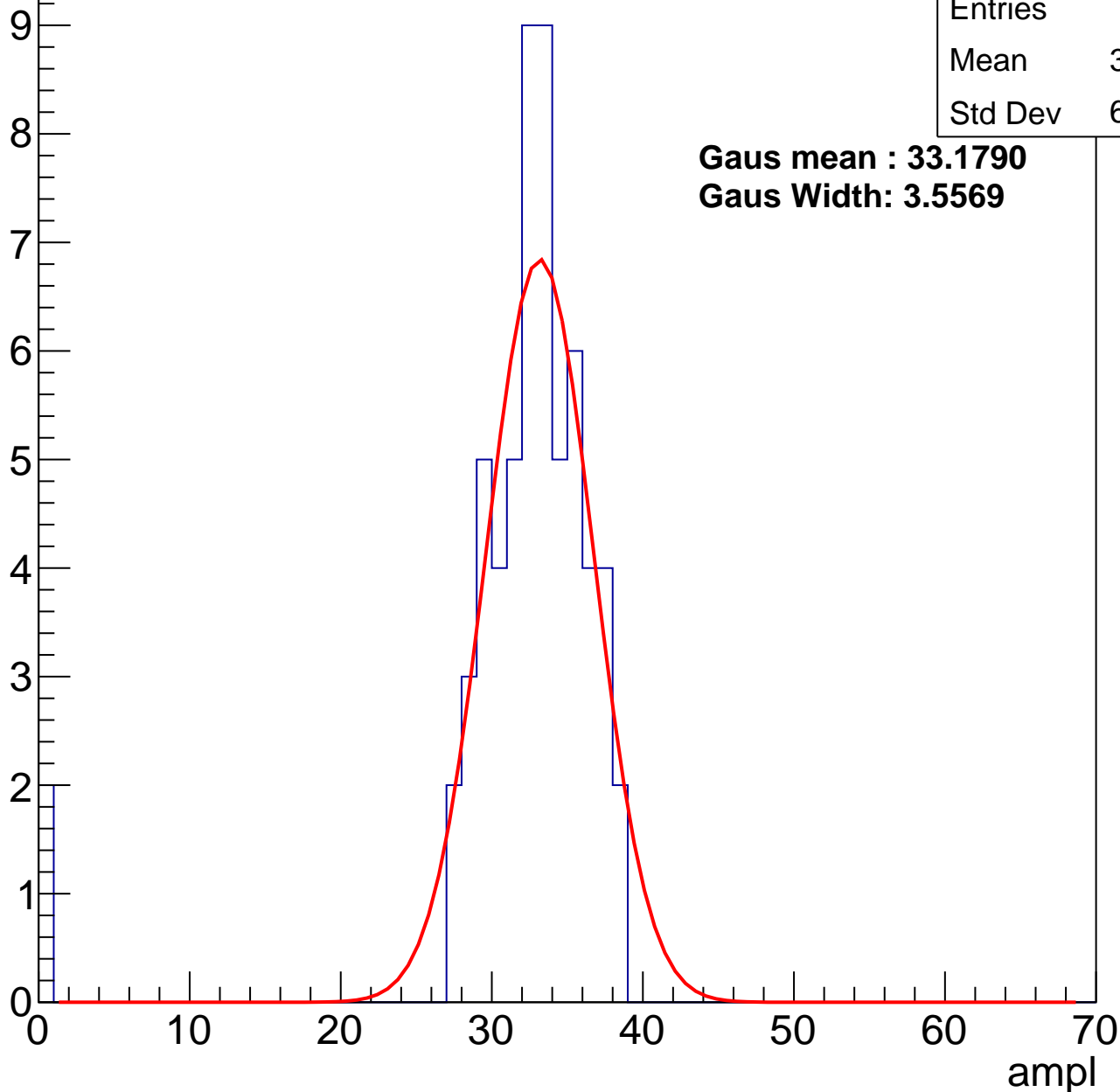
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	31.52
Std Dev	6.477

**Gaus mean : 33.1790**

**Gaus Width: 3.5569**



# B0L001S, U10-ch51, adc1

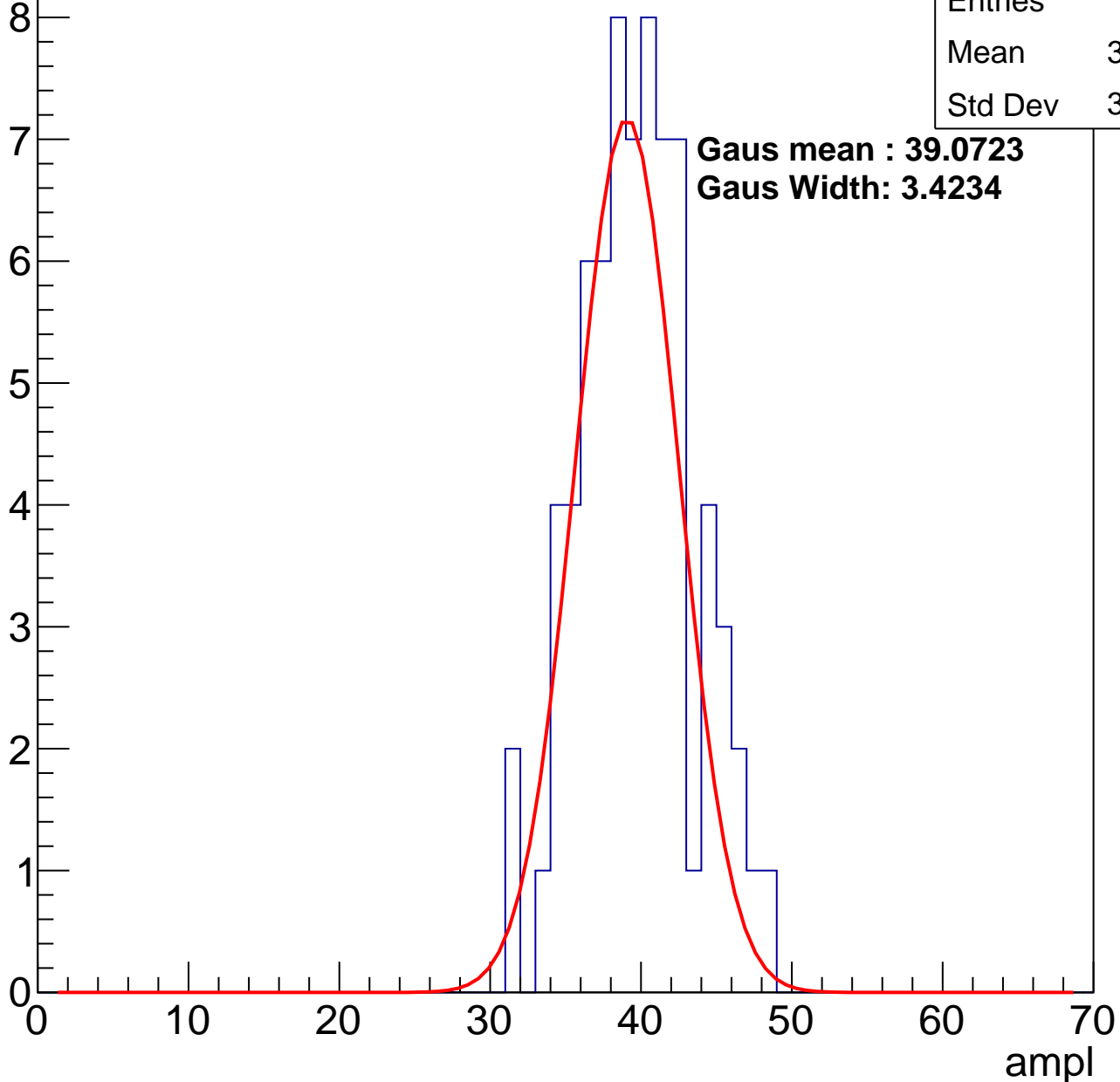
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	39.28
Std Dev	3.679

**Gaus mean : 39.0723**

**Gaus Width: 3.4234**



# B0L001S, U10-ch51, adc2

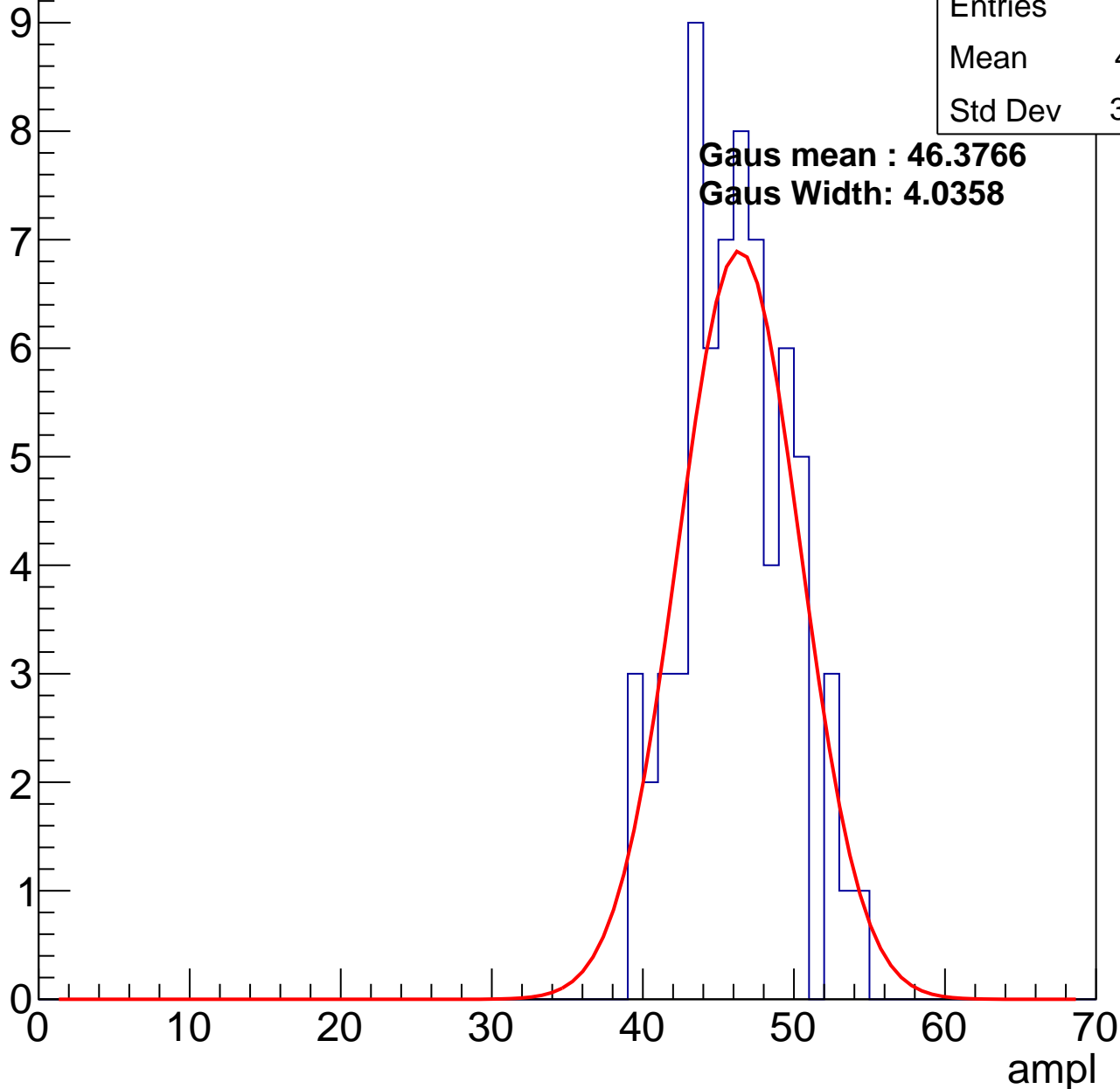
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	45.71
Std Dev	3.486

**Gaus mean : 46.3766**

**Gaus Width: 4.0358**



# B0L001S, U10-ch51, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	75
Mean	53.09
Std Dev	3.18

Entry

10

8

6

4

2

0

0

10

20

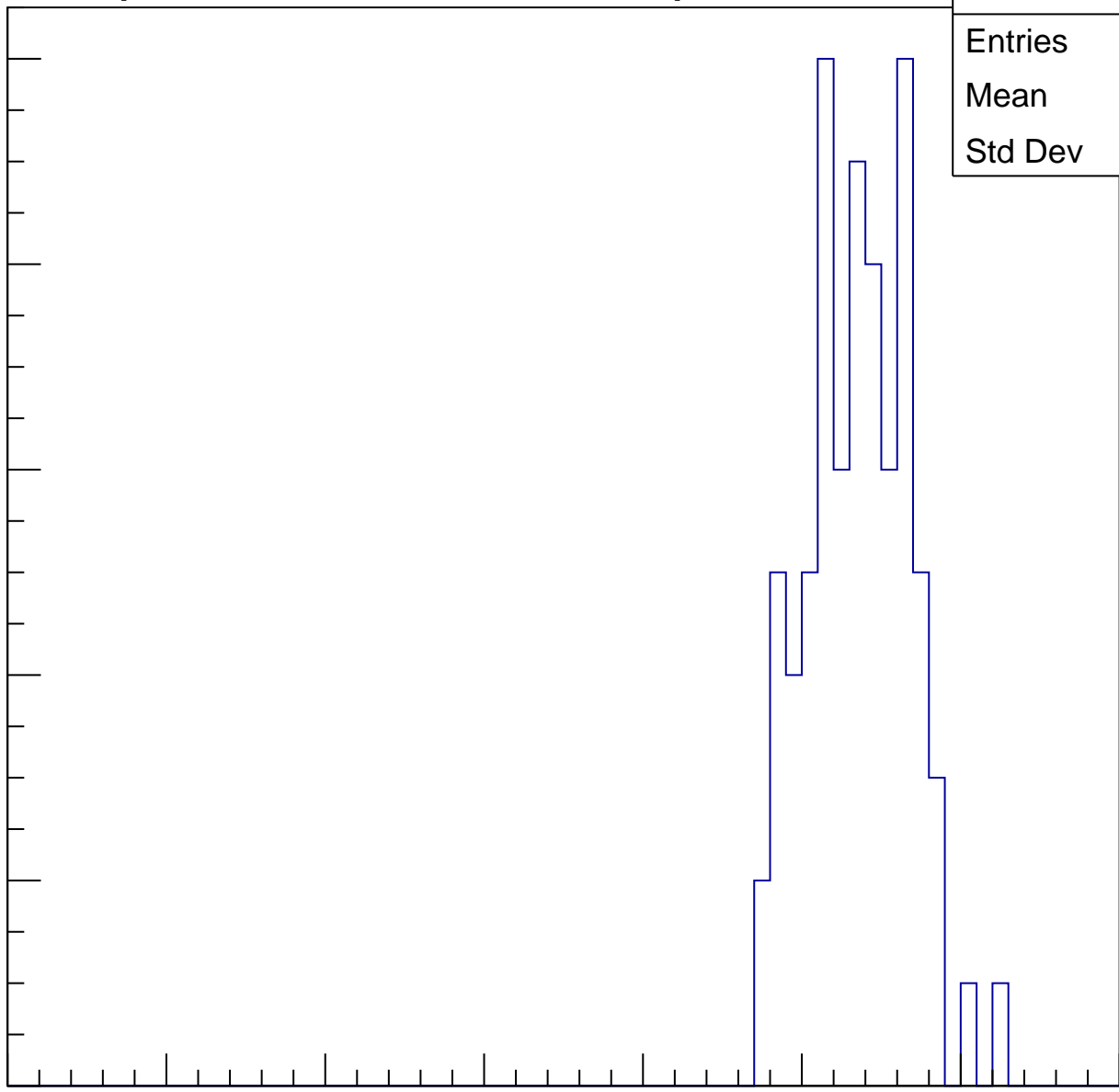
30

40

50

60

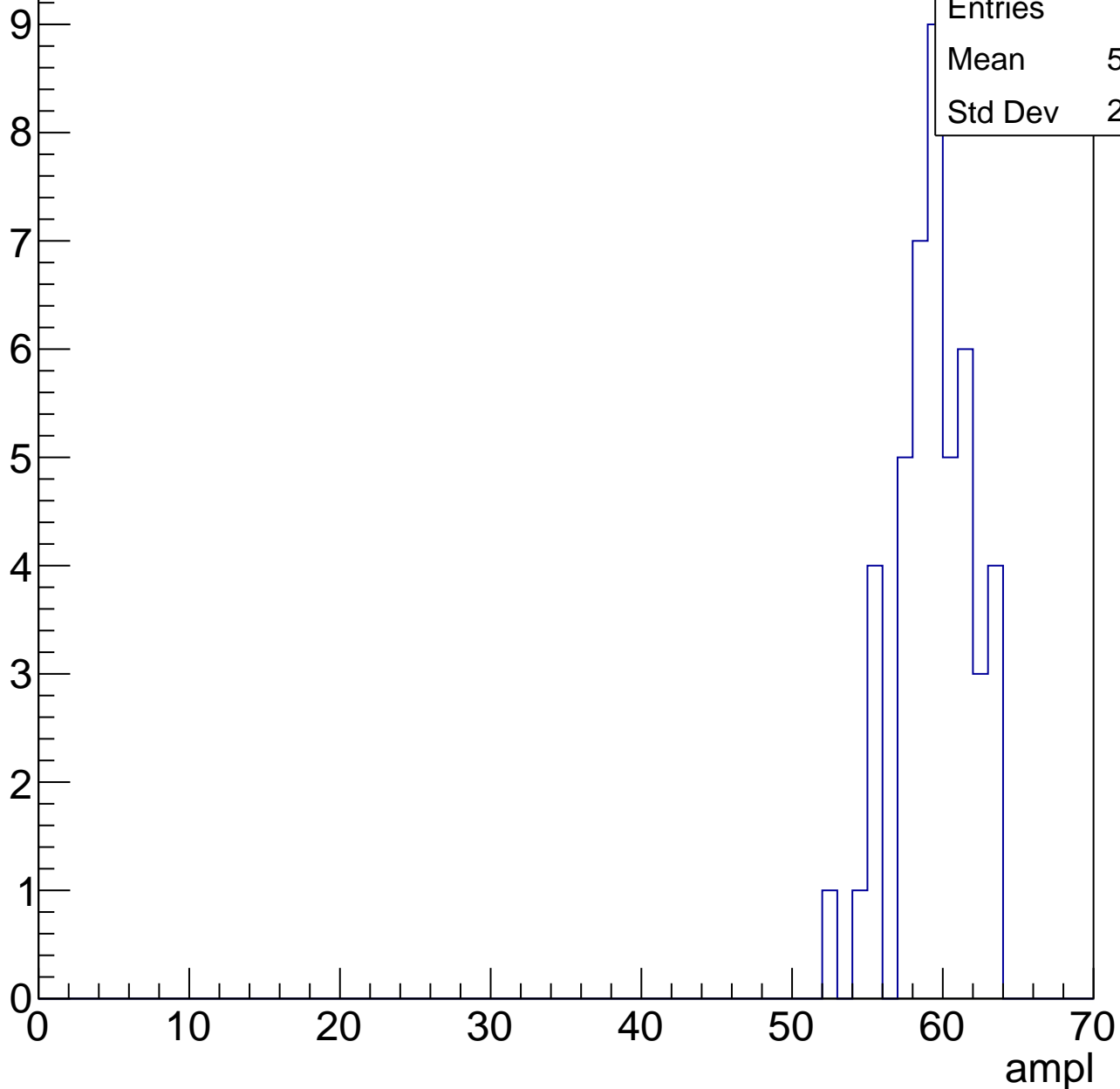
ampl



# B0L001S, U10-ch51, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

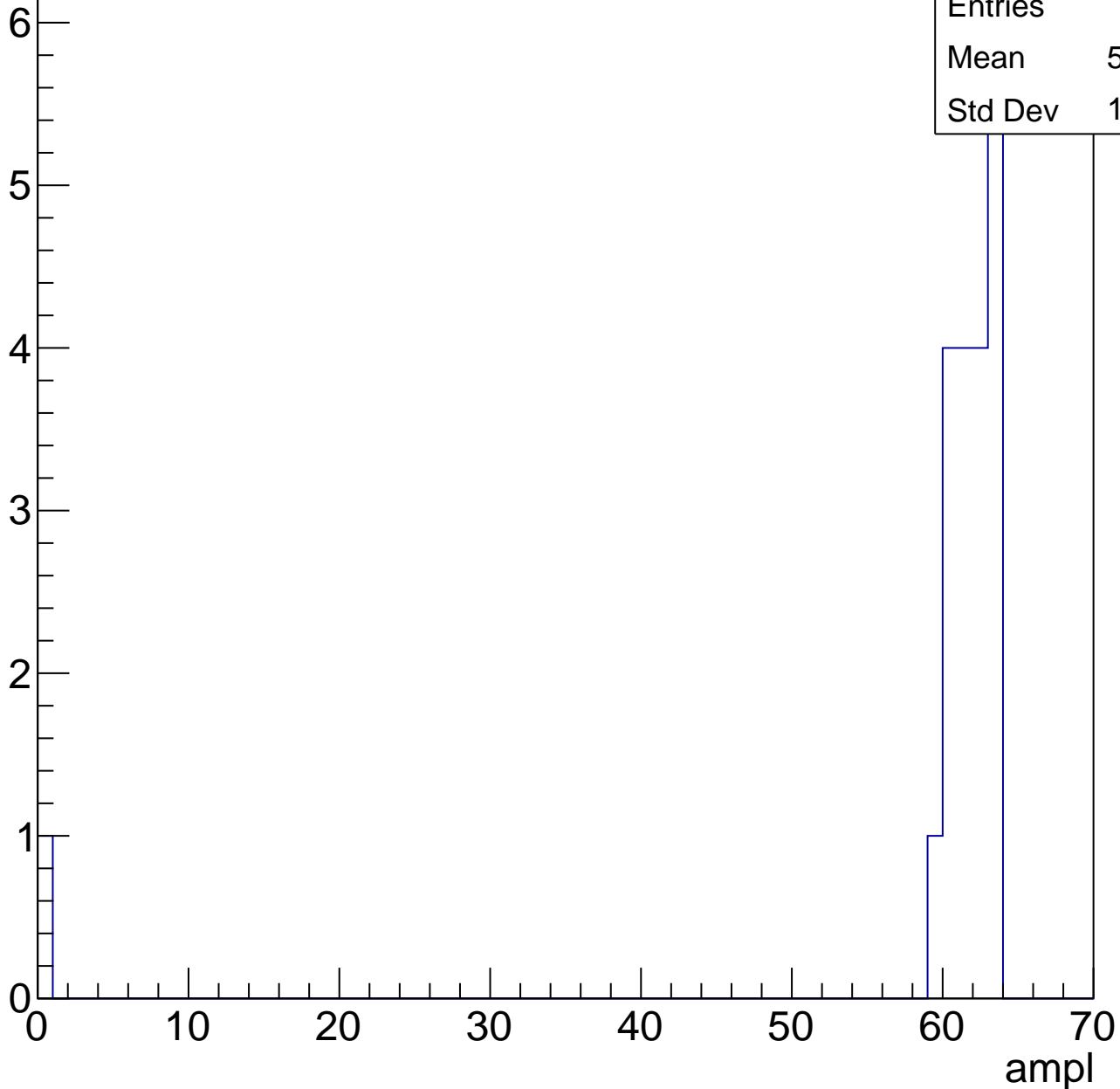


# B0L001S, U10-ch51, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	20
Mean	58.45
Std Dev	13.47



# B0L001S, U10-ch51, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch51, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U10-ch52, adc0

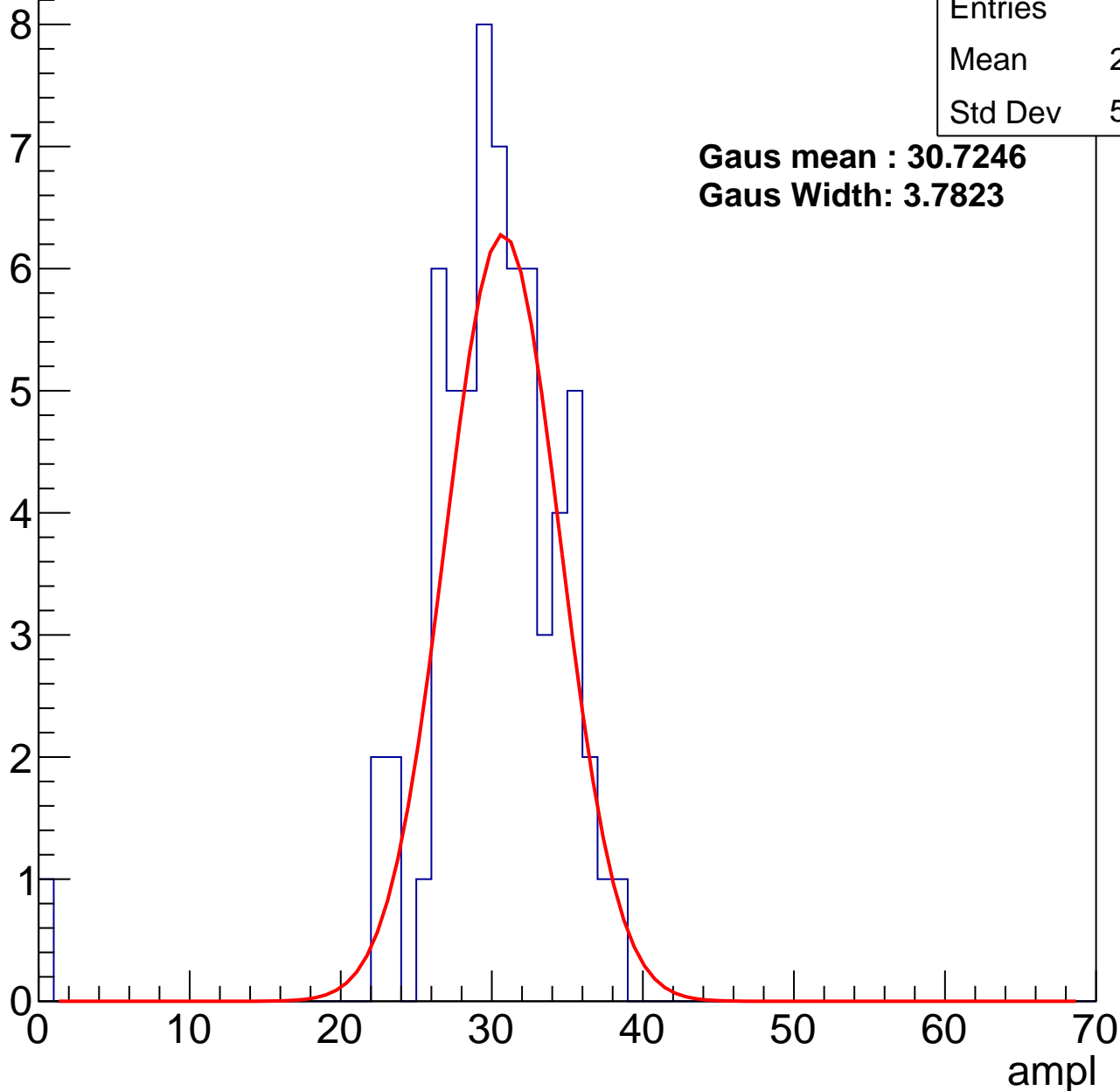
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	29.58
Std Dev	5.174

**Gaus mean : 30.7246**

**Gaus Width: 3.7823**



# B0L001S, U10-ch52, adc1

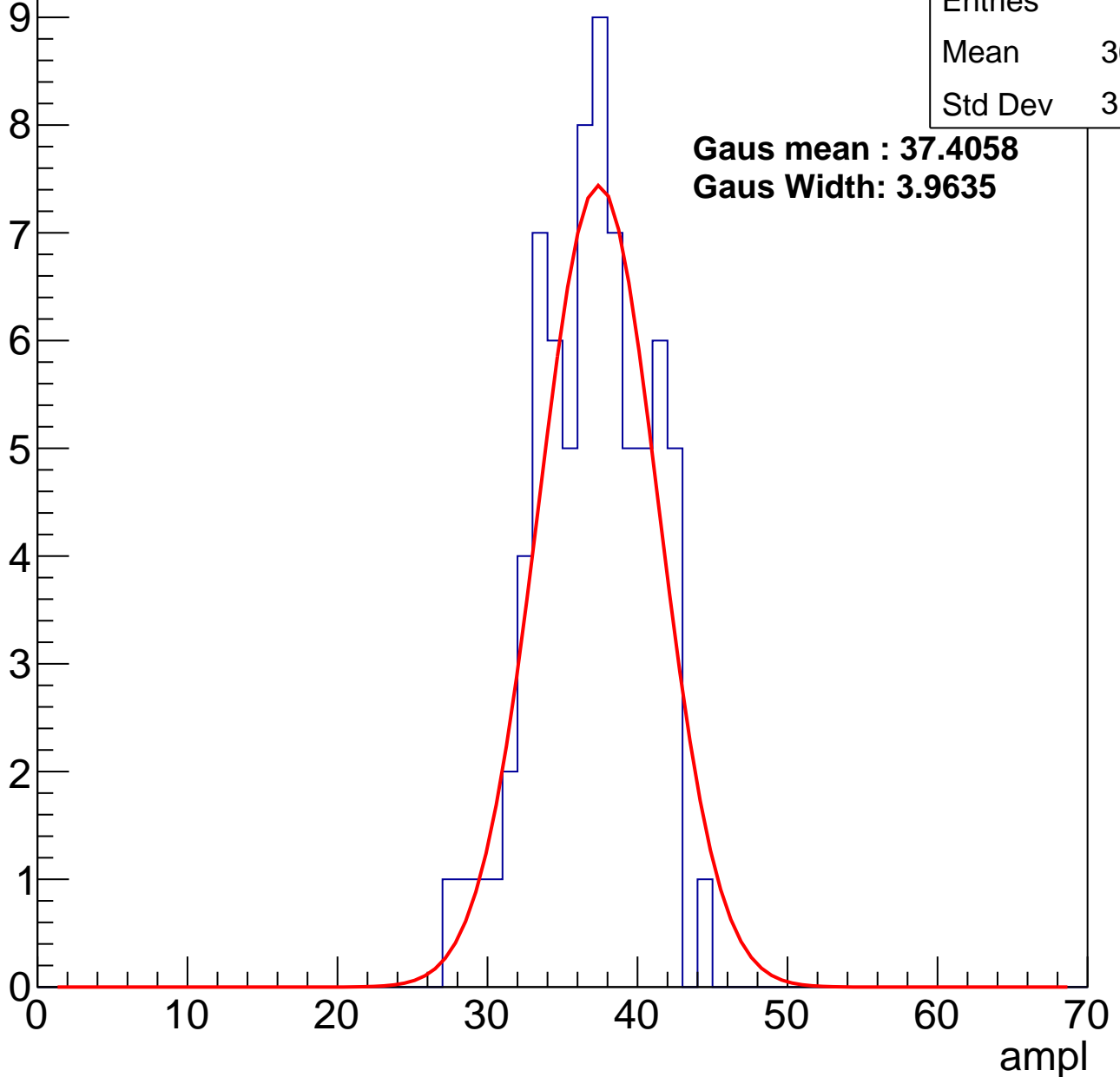
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	36.43
Std Dev	3.636

**Gaus mean : 37.4058**

**Gaus Width: 3.9635**



# B0L001S, U10-ch52, adc2

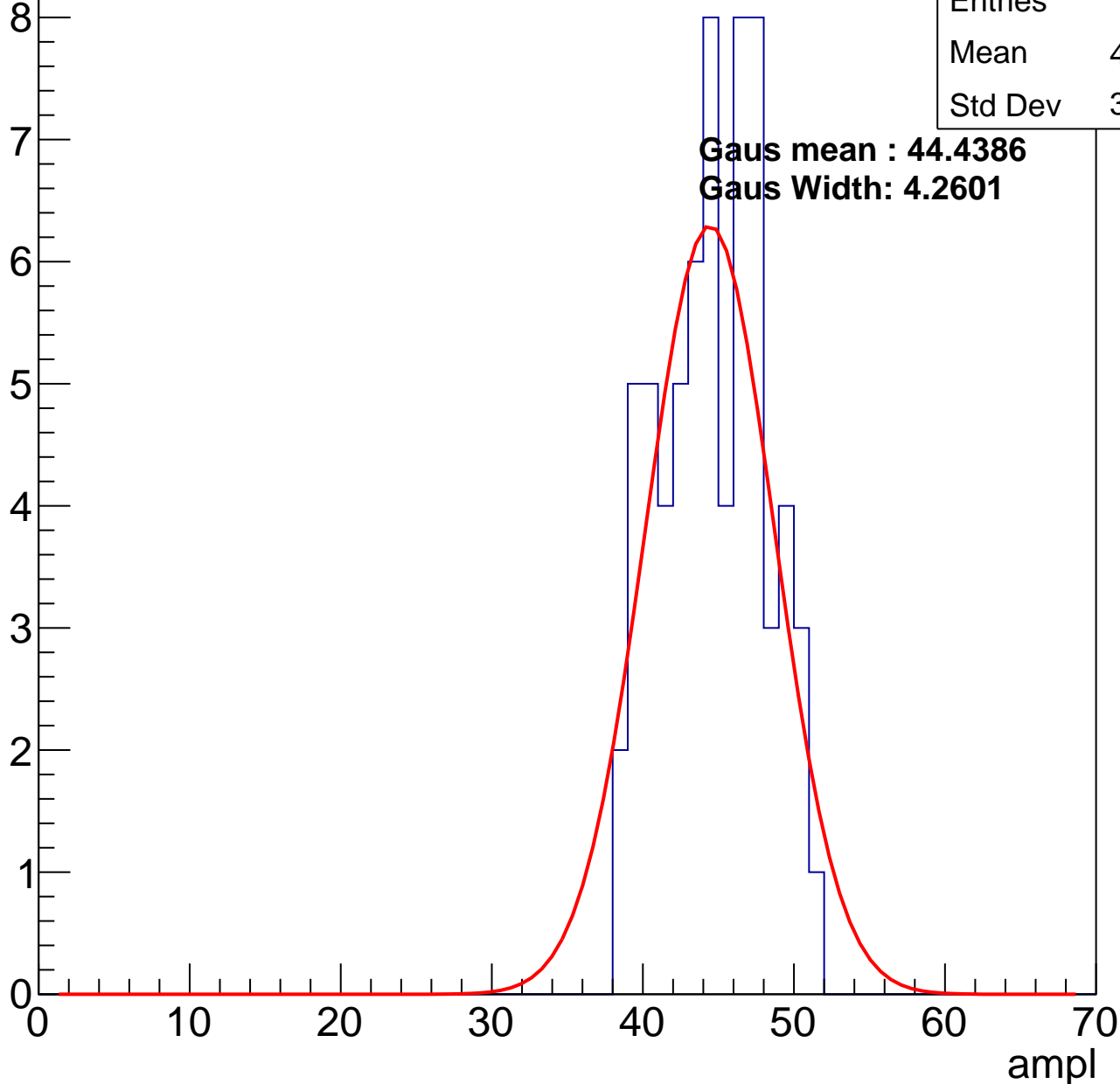
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	44.24
Std Dev	3.367

**Gaus mean : 44.4386**

**Gaus Width: 4.2601**



# B0L001S, U10-ch52, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	68
Mean	50.01
Std Dev	3.521

Entry

10

8

6

4

2

0

0

10

20

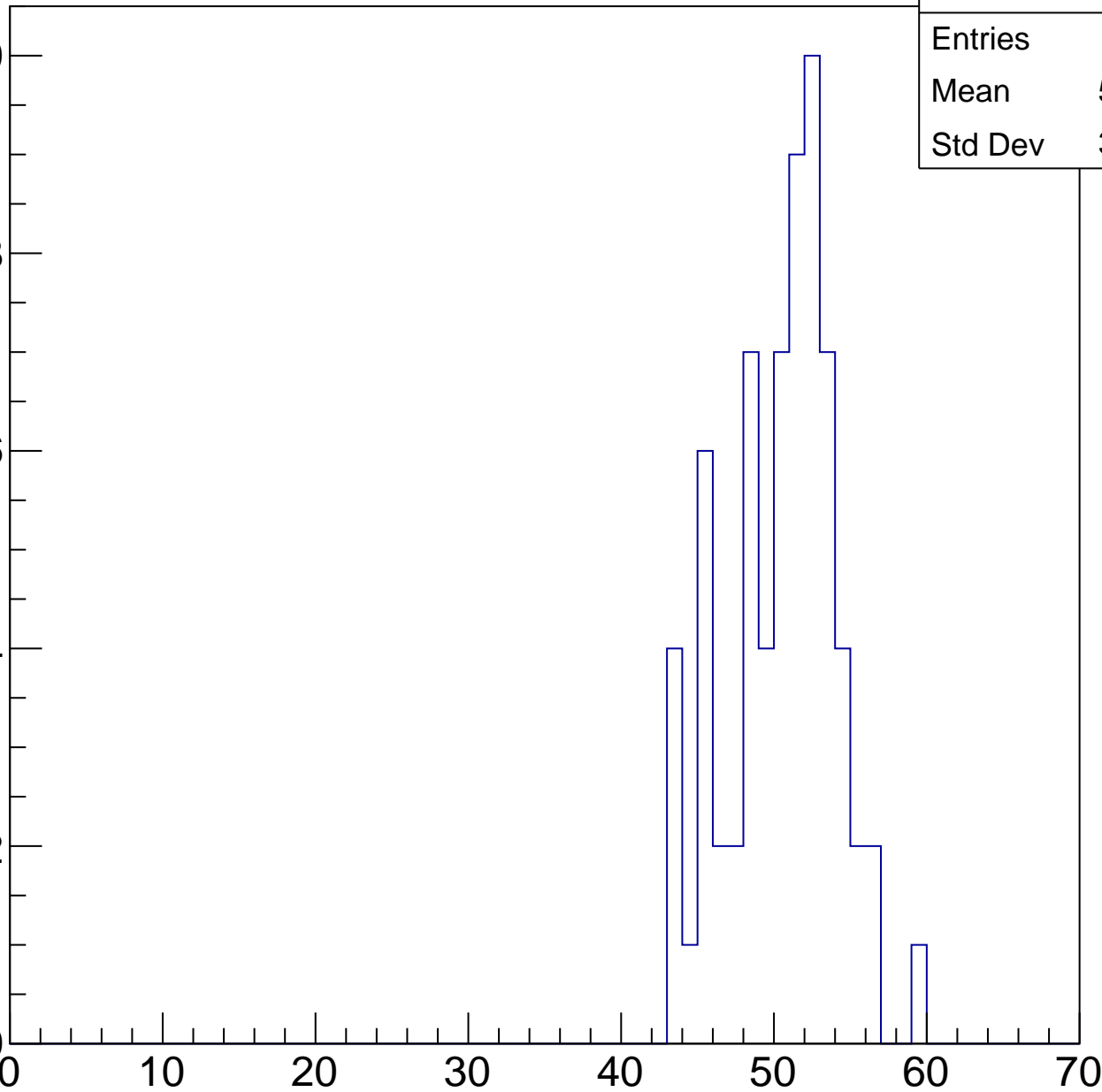
30

40

50

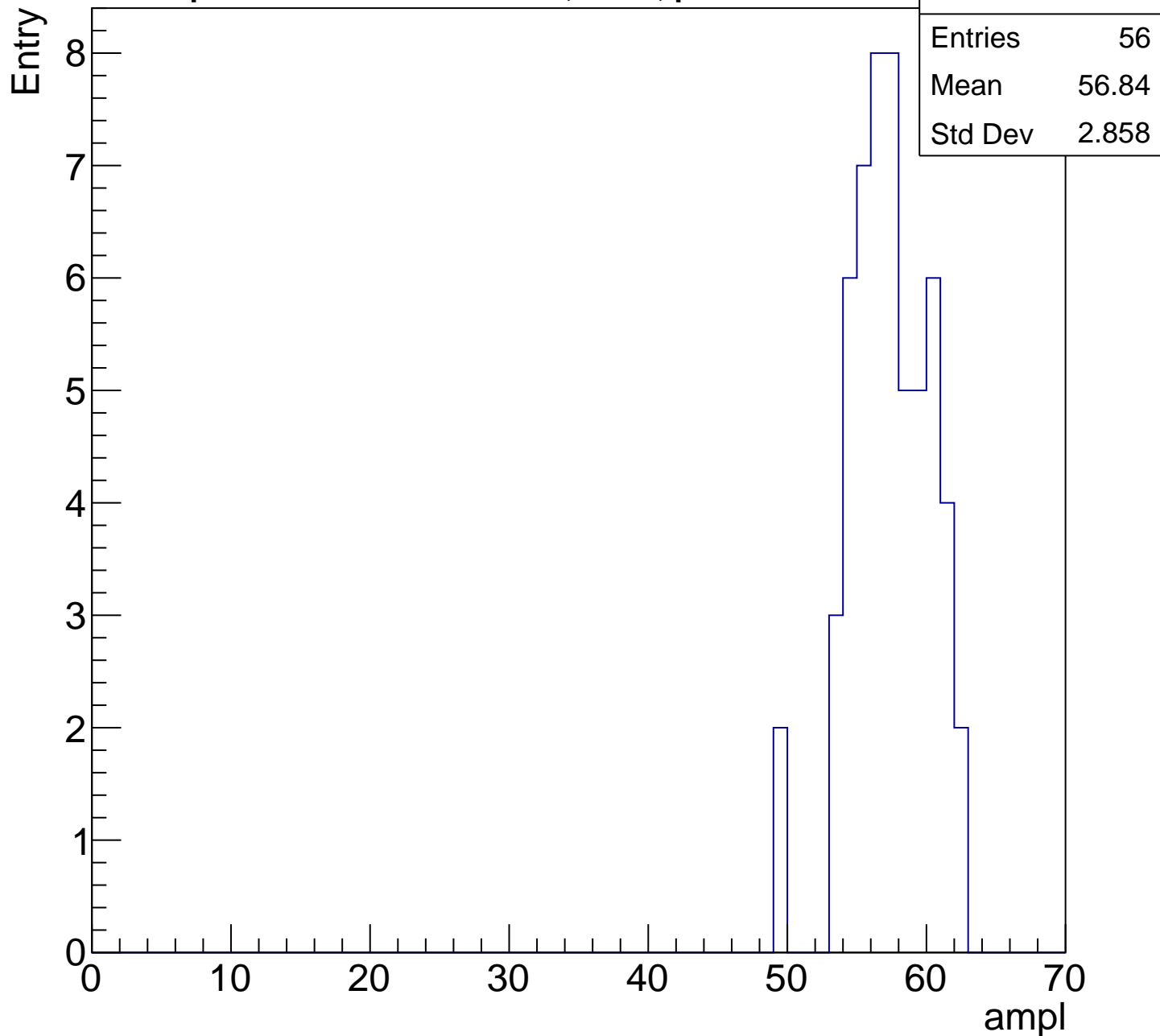
60

ampl



# B0L001S, U10-ch52, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

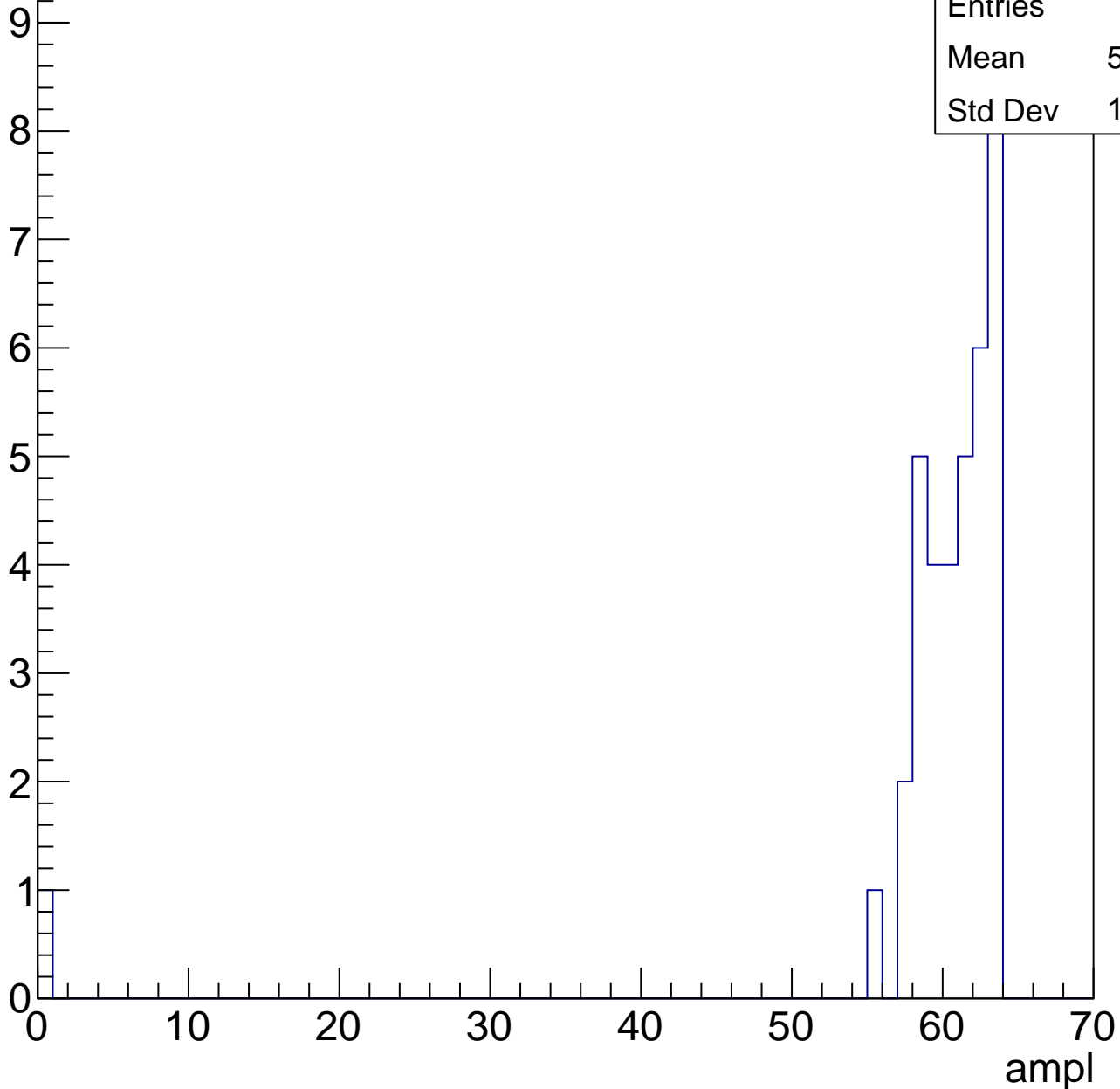


# B0L001S, U10-ch52, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	37
Mean	58.89
Std Dev	10.04



# B0L001S, U10-ch52, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	61.67
Std Dev	0.4714

ampl

0 10 20 30 40 50 60 70



# B0L001S, U10-ch52, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	3
Mean	21
Std Dev	29.7

# B0L001S, U10-ch53, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	90
Mean	31.56
Std Dev	3.97

**Gaus mean : 31.8254**

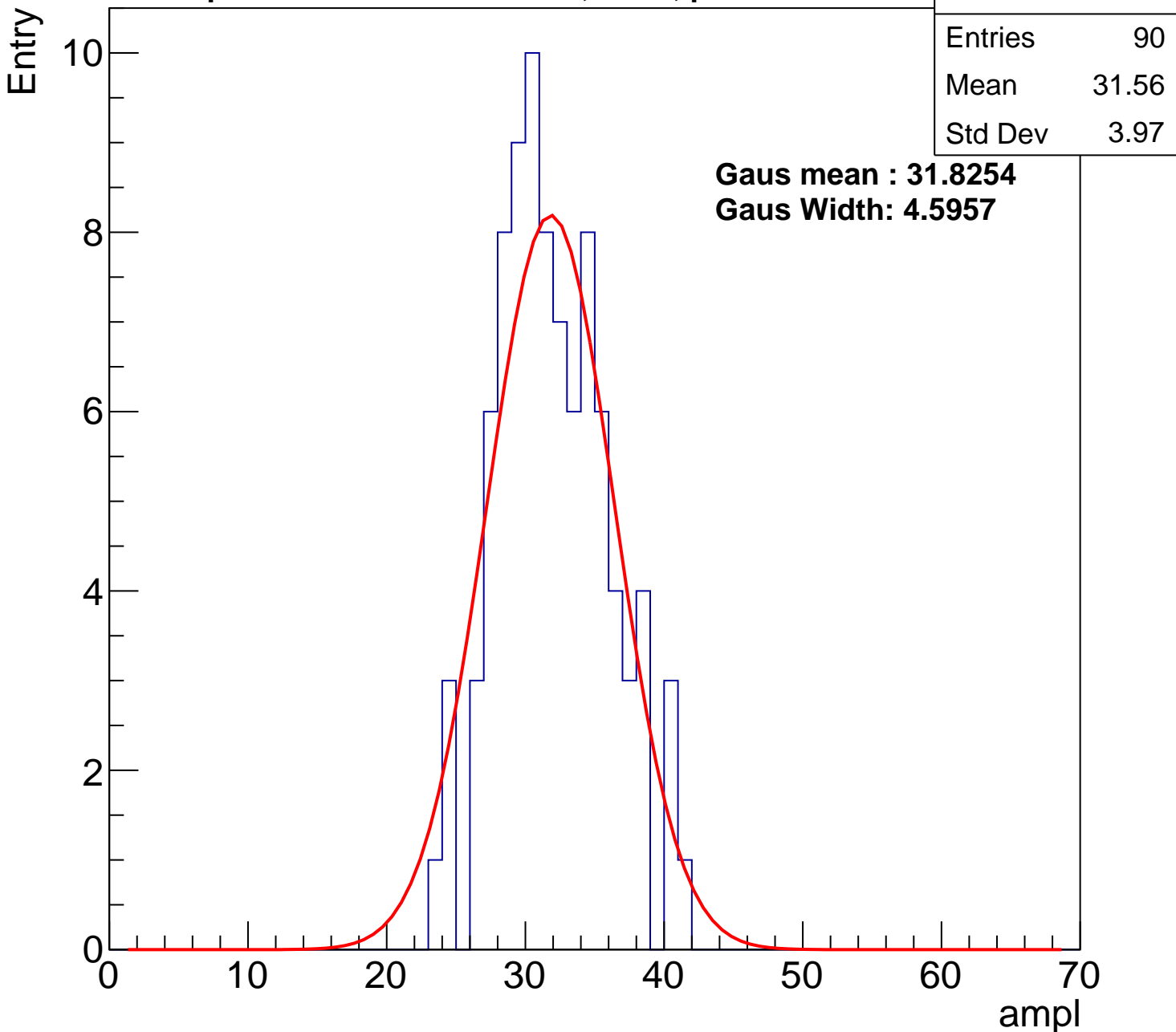
**Gaus Width: 4.5957**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U10-ch53, adc1

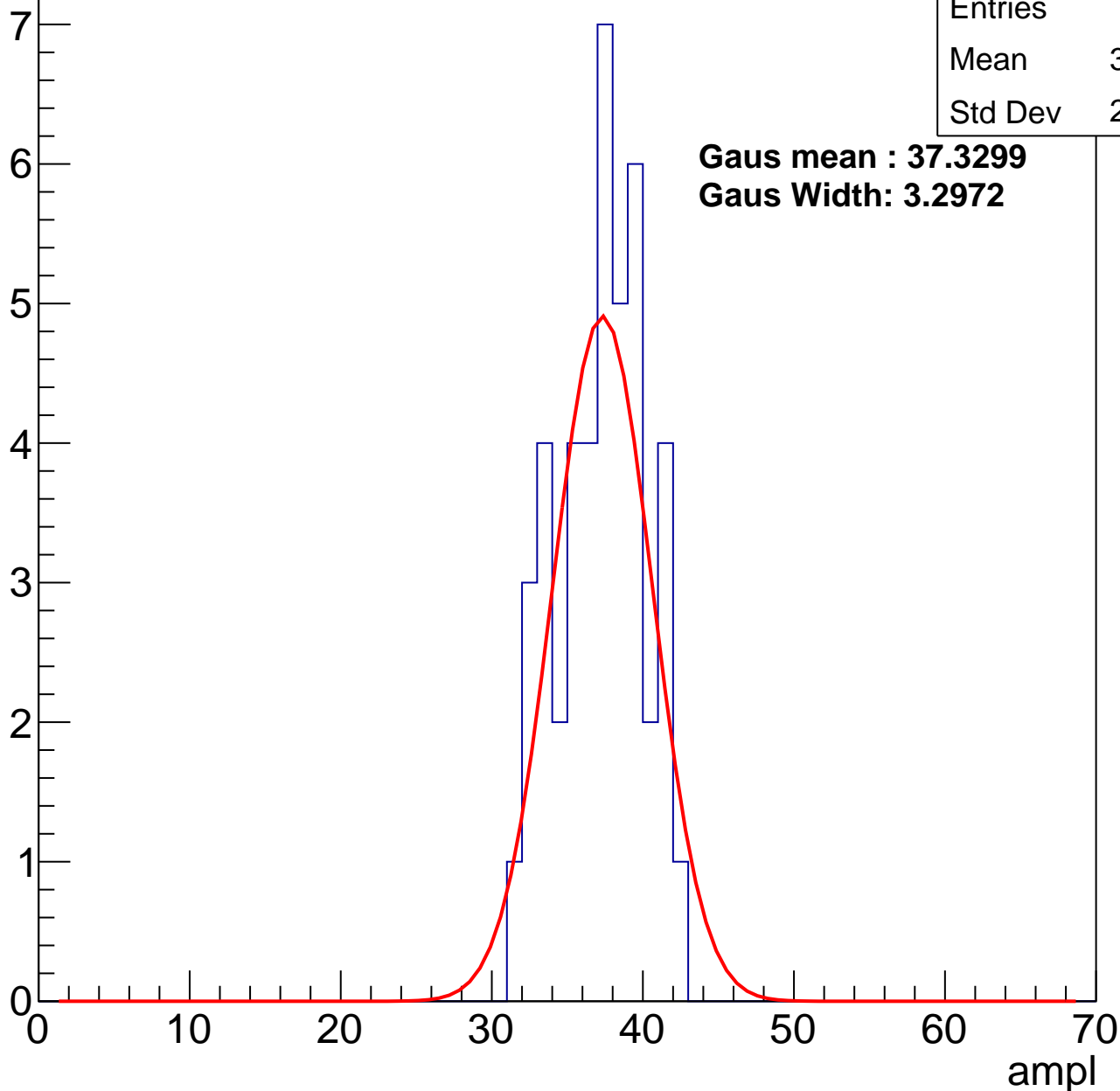
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	43
Mean	36.74
Std Dev	2.837

**Gaus mean : 37.3299**

**Gaus Width: 3.2972**



# B0L001S, U10-ch53, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	78
Mean	44.1
Std Dev	3.51

**Gaus mean : 43.8116**

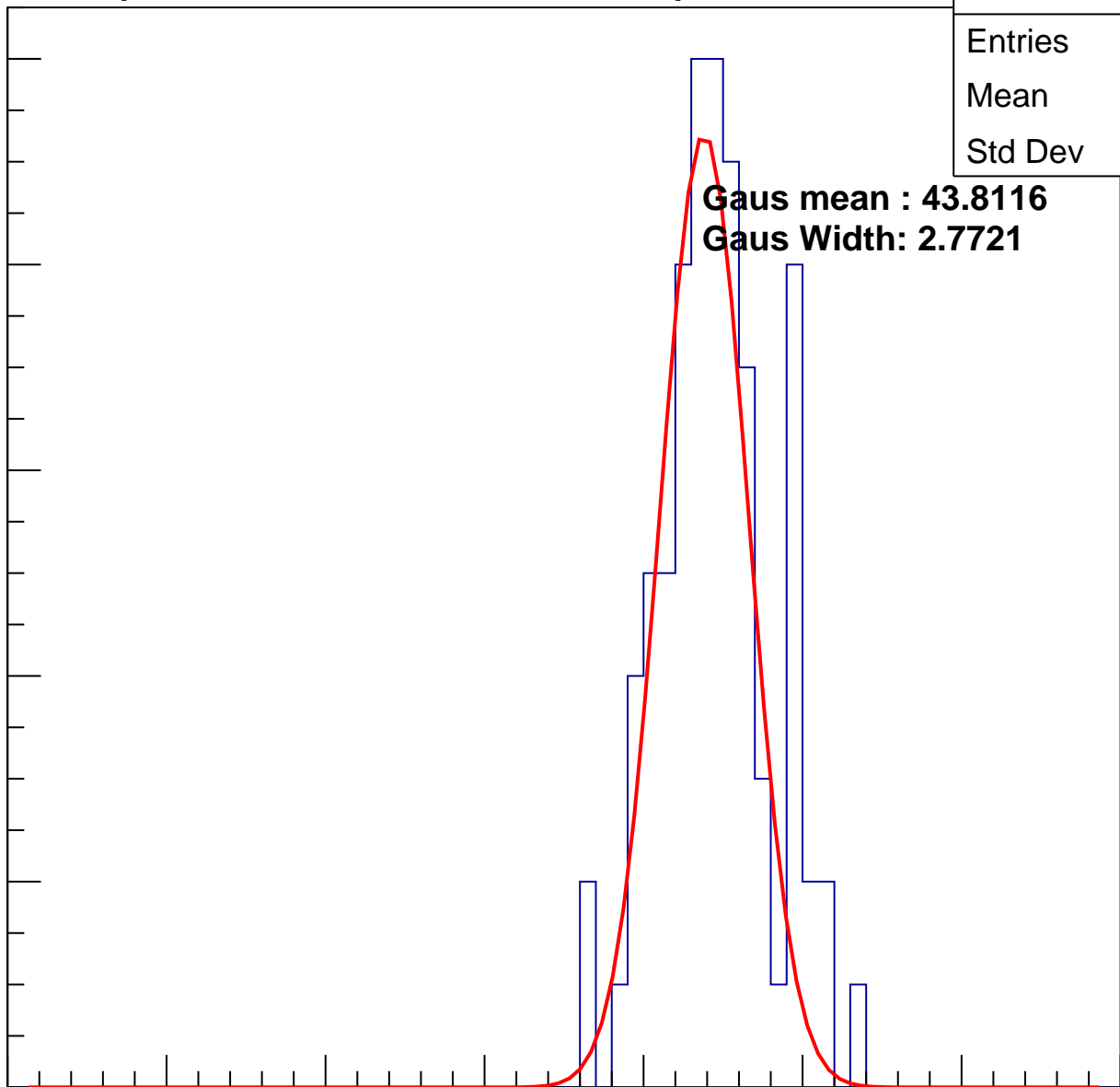
**Gaus Width: 2.7721**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

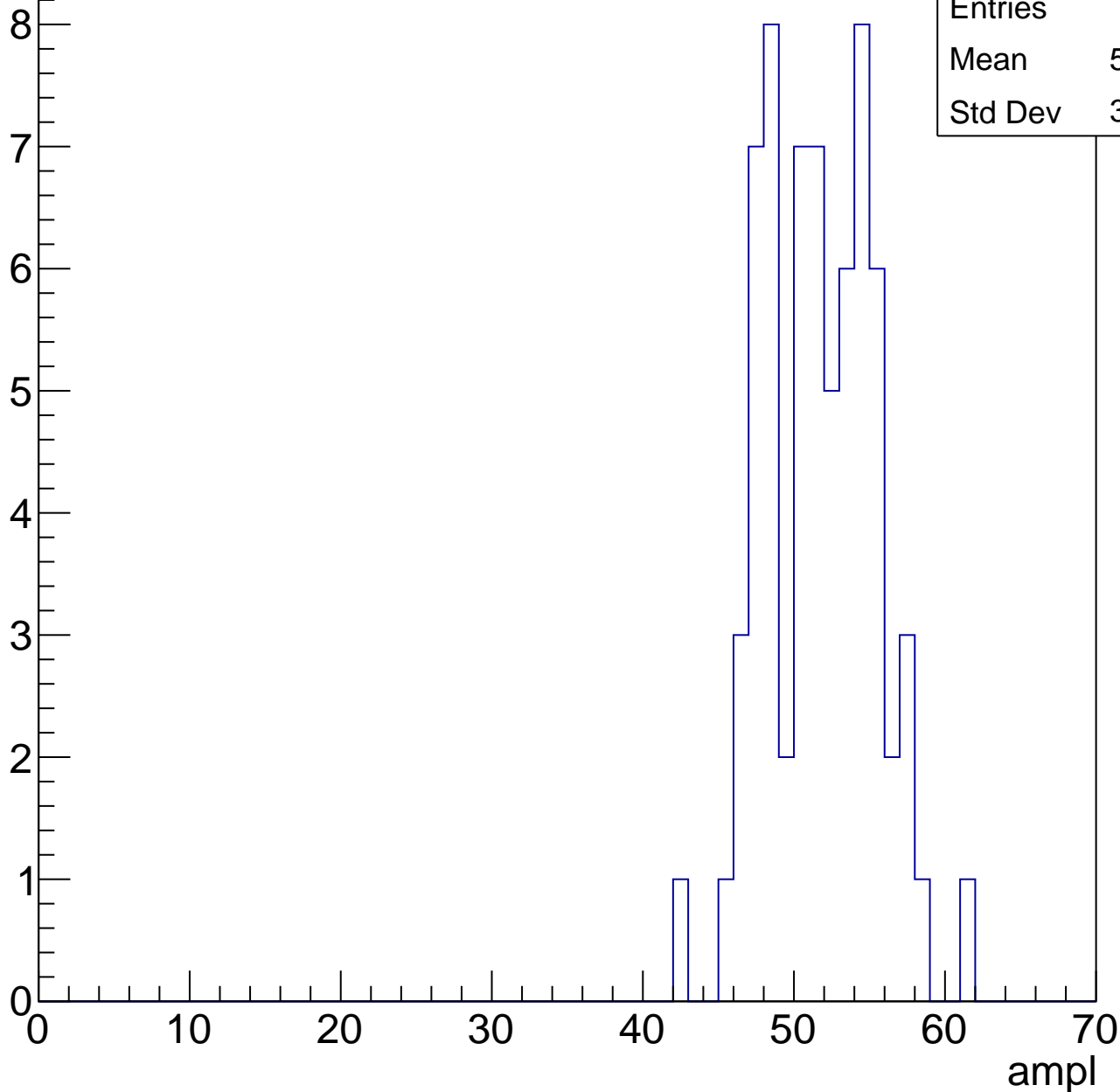


# B0L001S, U10-ch53, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	51.25
Std Dev	3.619

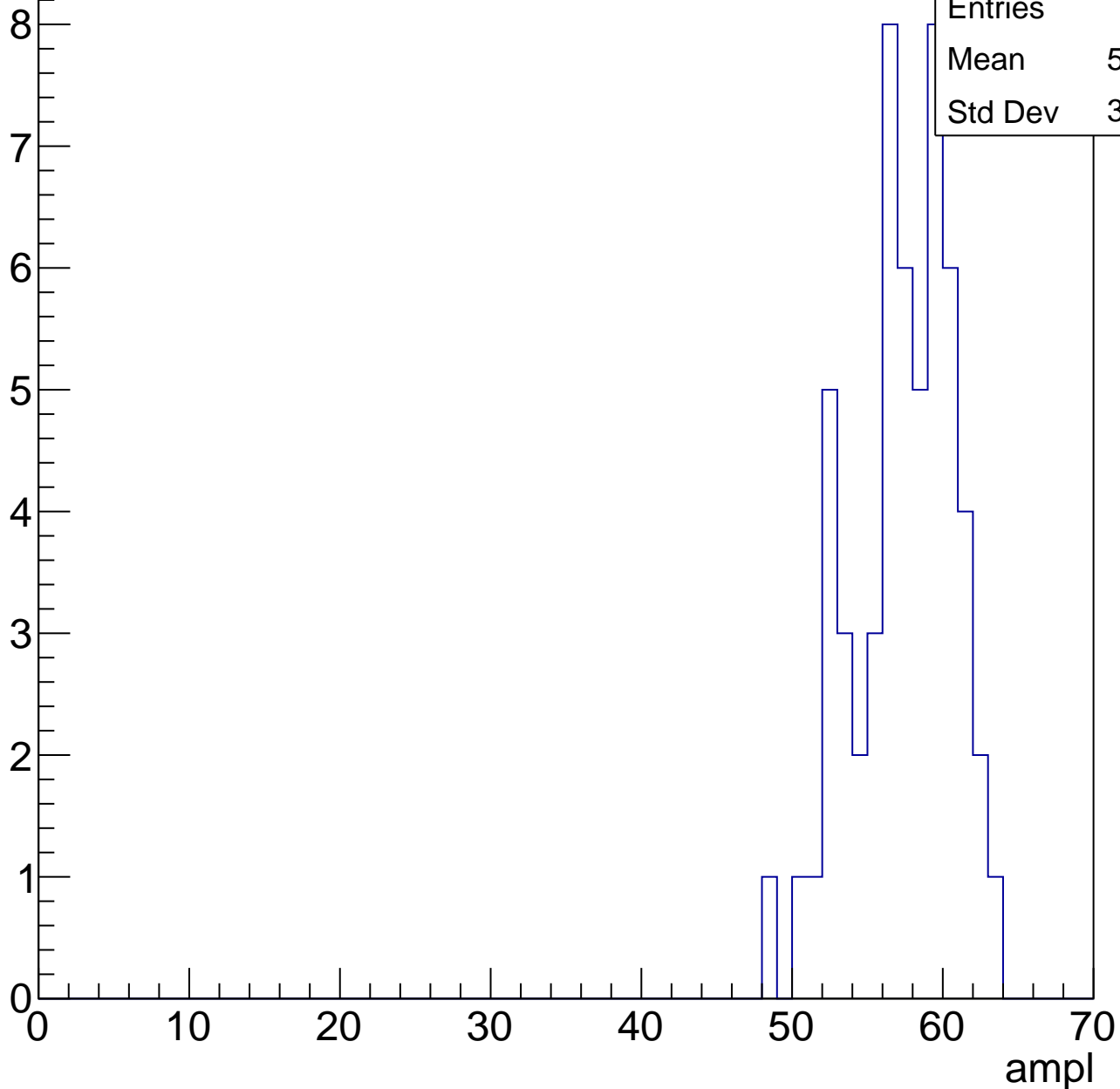


# B0L001S, U10-ch53, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	56.86
Std Dev	3.319

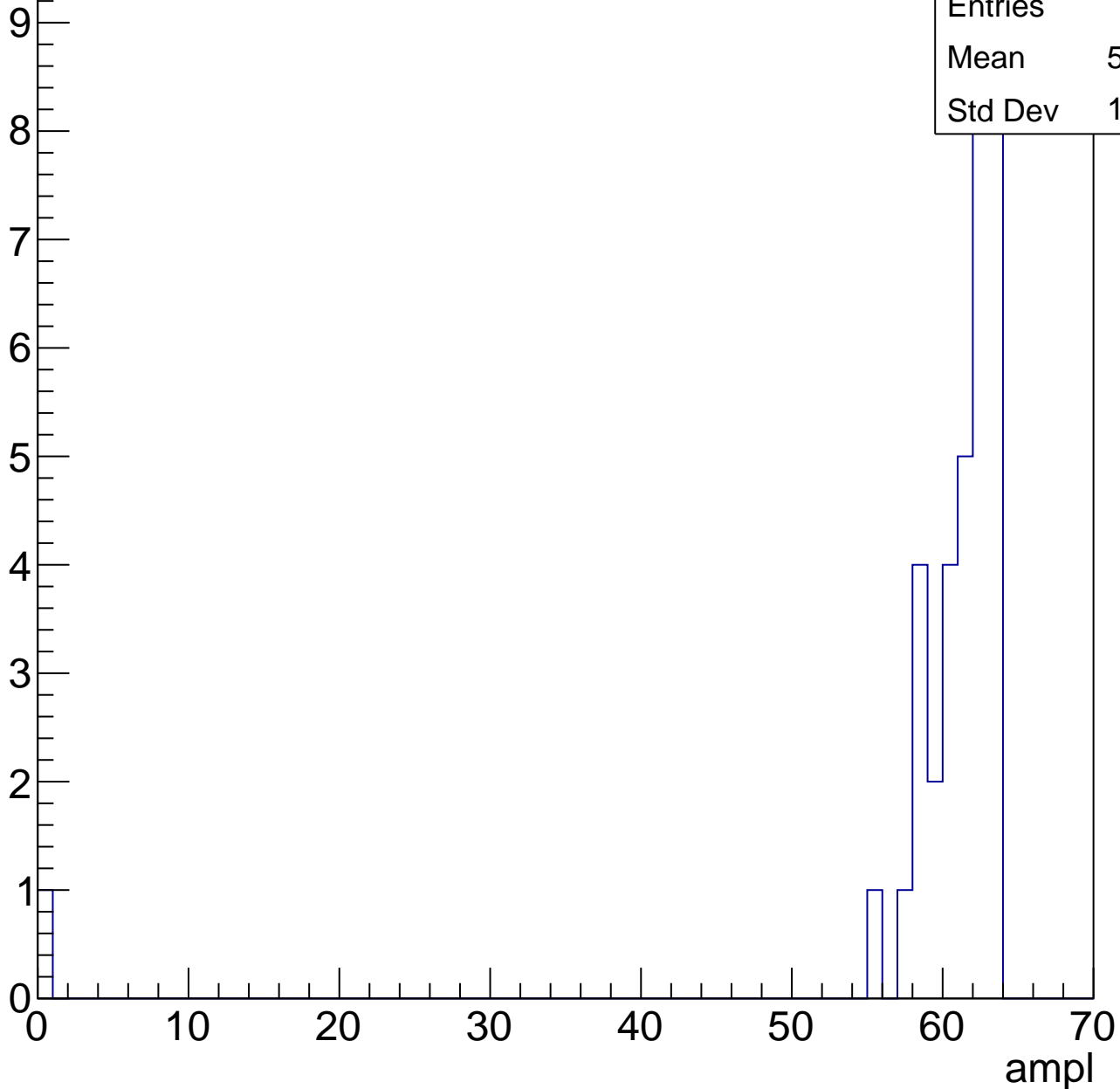


# B0L001S, U10-ch53, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	35
Mean	59.14
Std Dev	10.34



# B0L001S, U10-ch53, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U10-ch53, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U10-ch54, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	79
Mean	30.65
Std Dev	4.889

**Gaus mean : 31.1153**

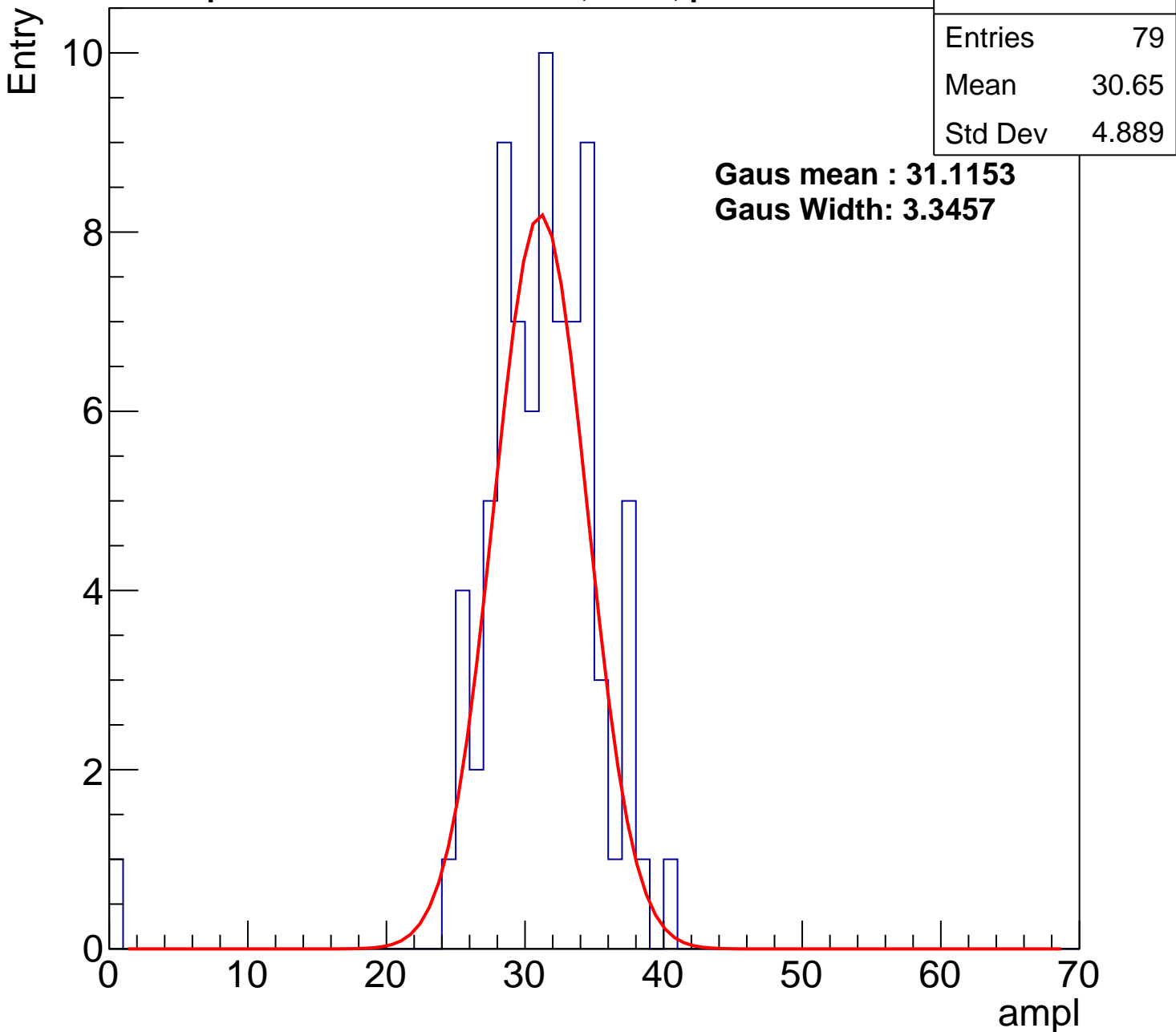
**Gaus Width: 3.3457**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U10-ch54, adc1

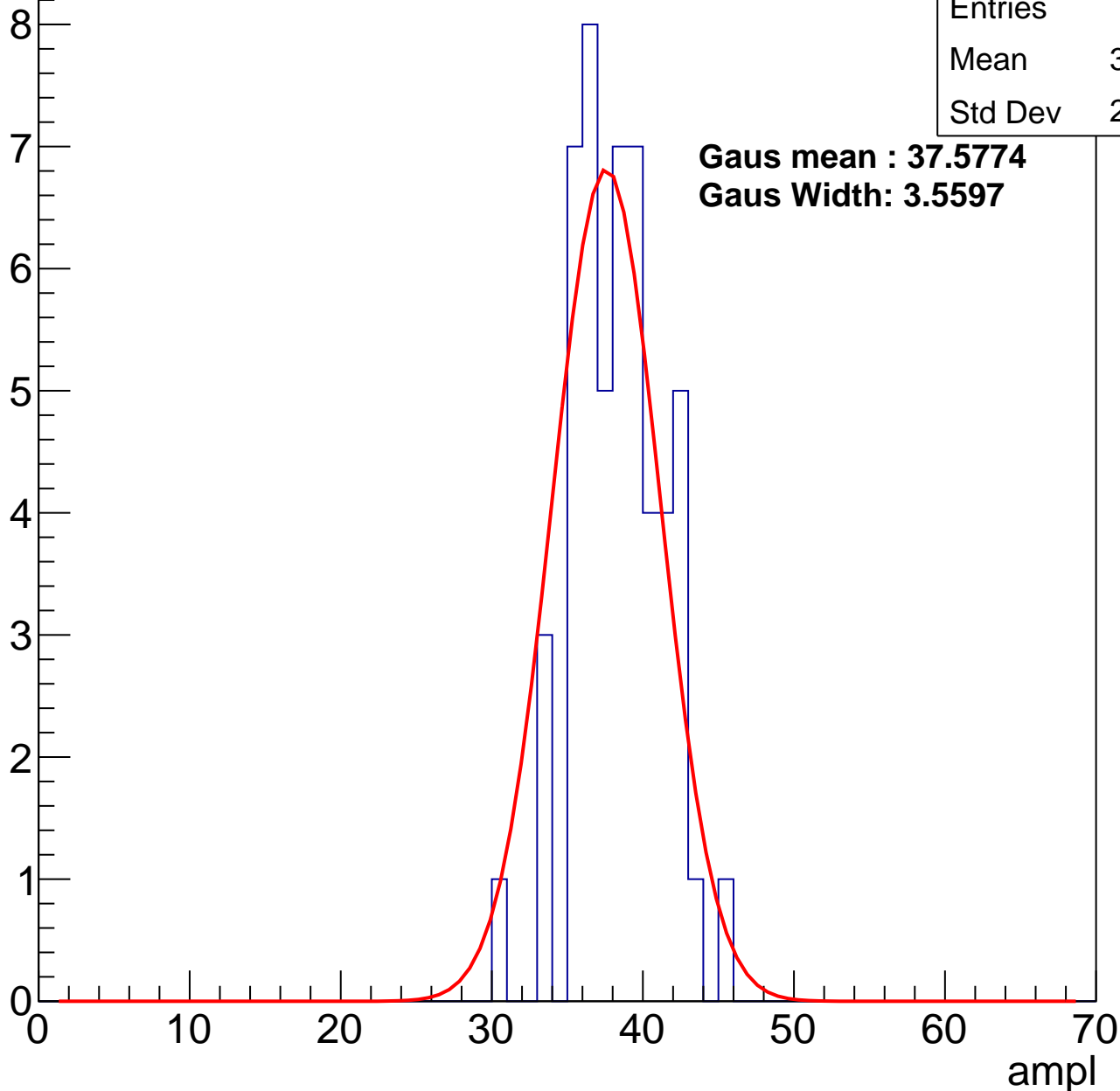
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	37.89
Std Dev	2.918

**Gaus mean : 37.5774**

**Gaus Width: 3.5597**



# B0L001S, U10-ch54, adc2

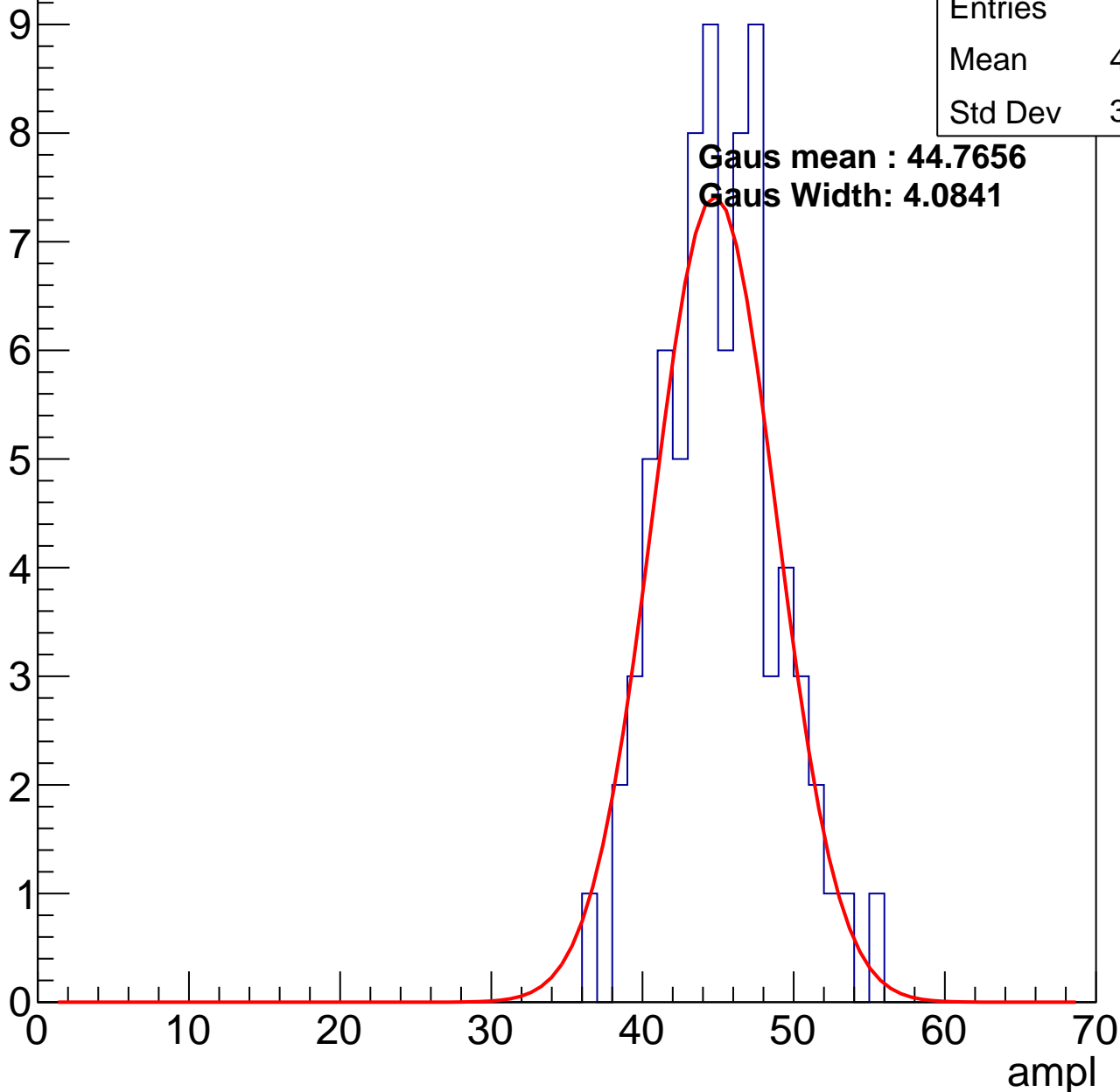
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	77
Mean	44.65
Std Dev	3.744

**Gaus mean : 44.7656**

**Gaus Width: 4.0841**

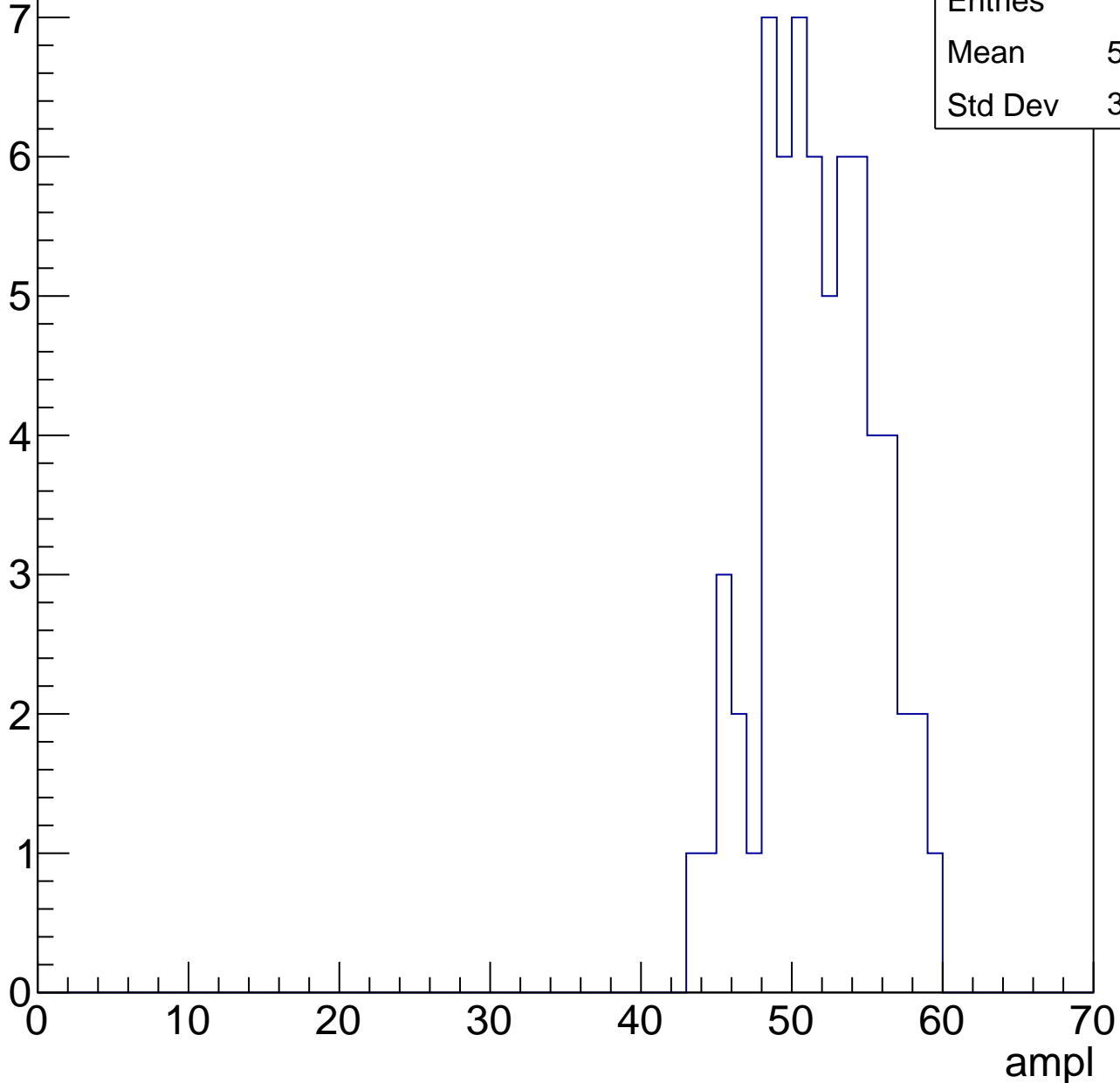


# B0L001S, U10-ch54, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

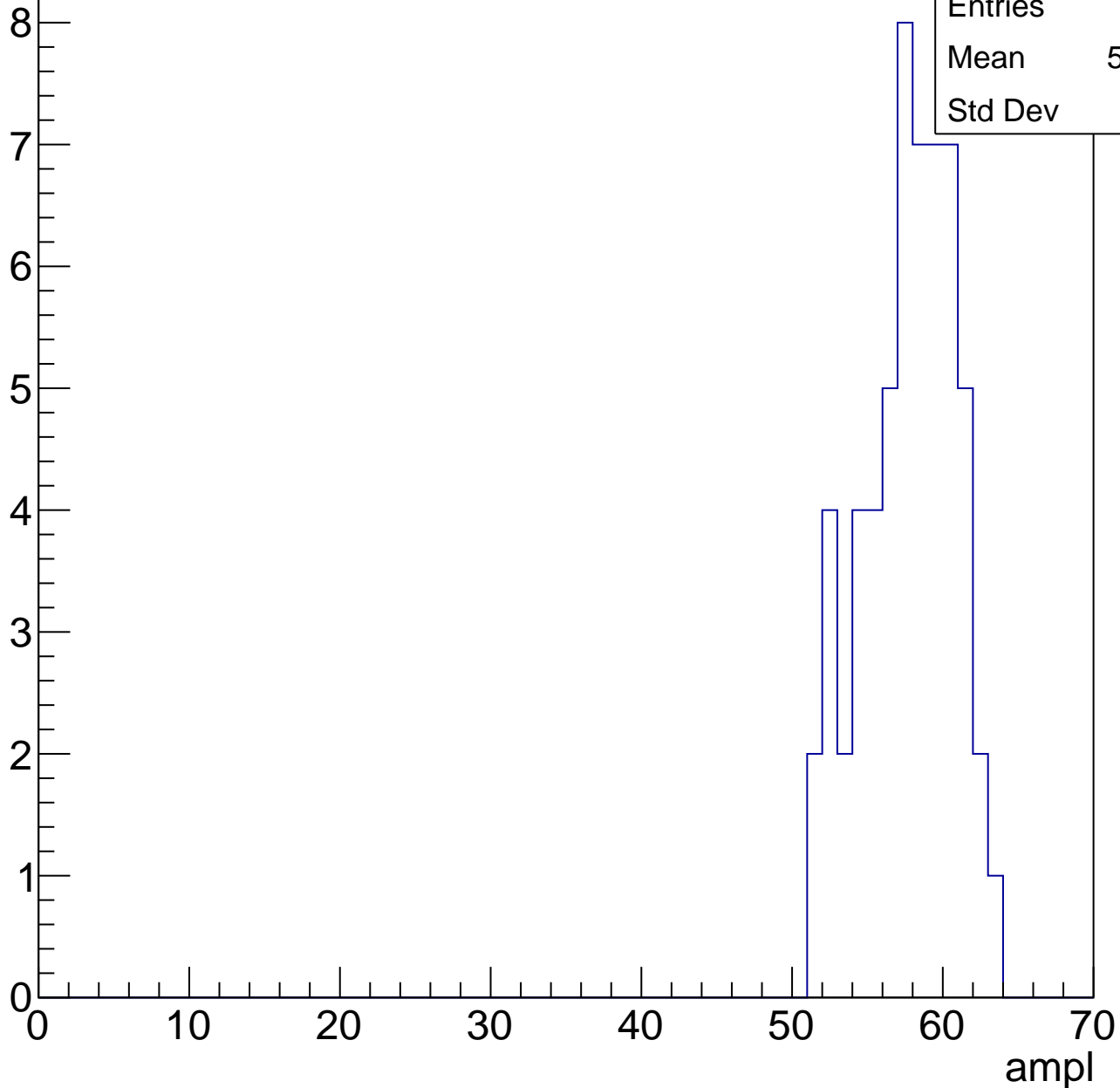
Entries	64
Mean	51.28
Std Dev	3.659



# B0L001S, U10-ch54, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



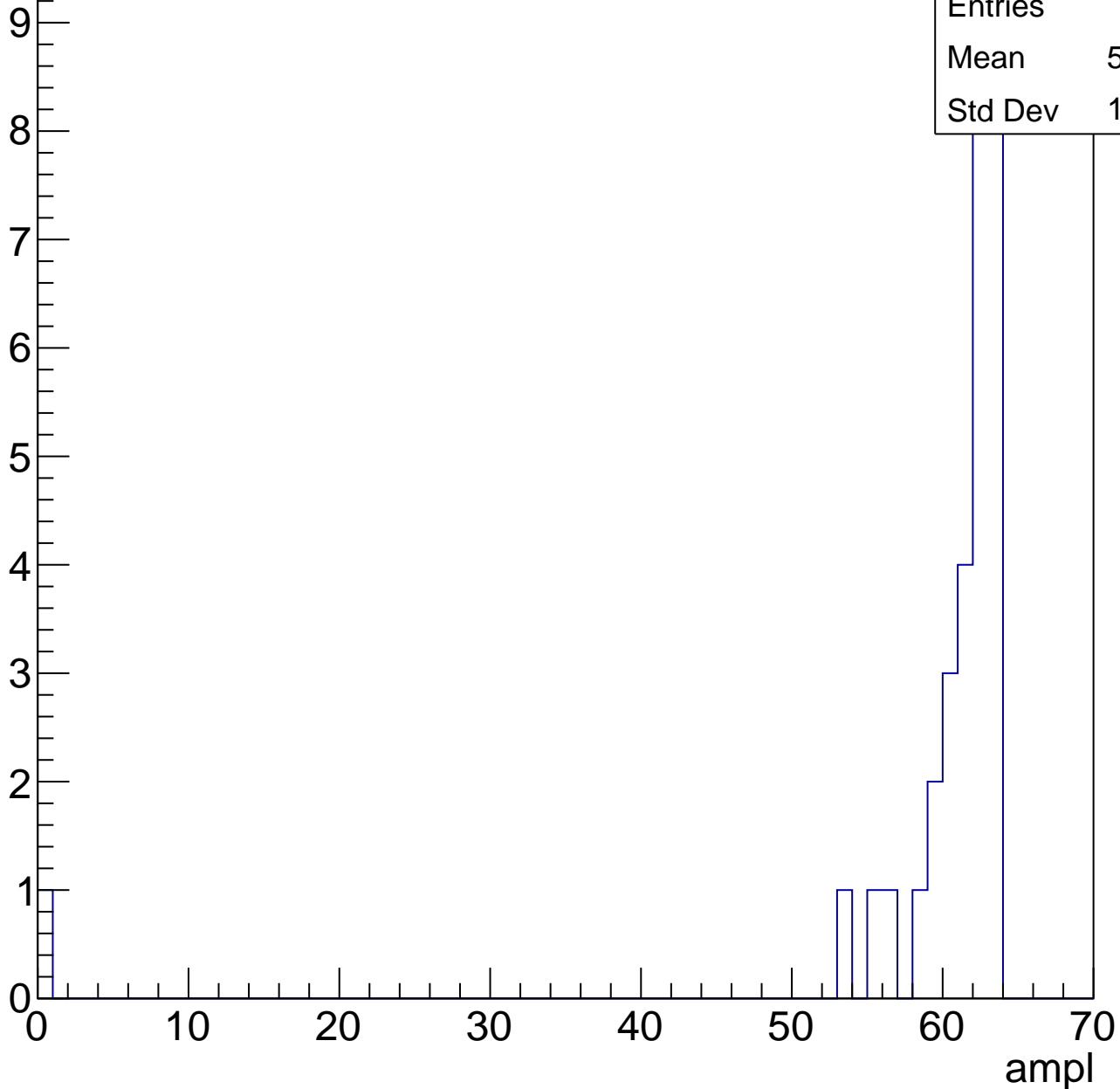
Entries	58
Mean	57.22
Std Dev	3

# B0L001S, U10-ch54, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	31
Mean	58.94
Std Dev	11.04



# B0L001S, U10-ch54, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch54, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U10-ch55, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	82
Mean	33.17
Std Dev	3.352

**Gaus mean : 33.8224**

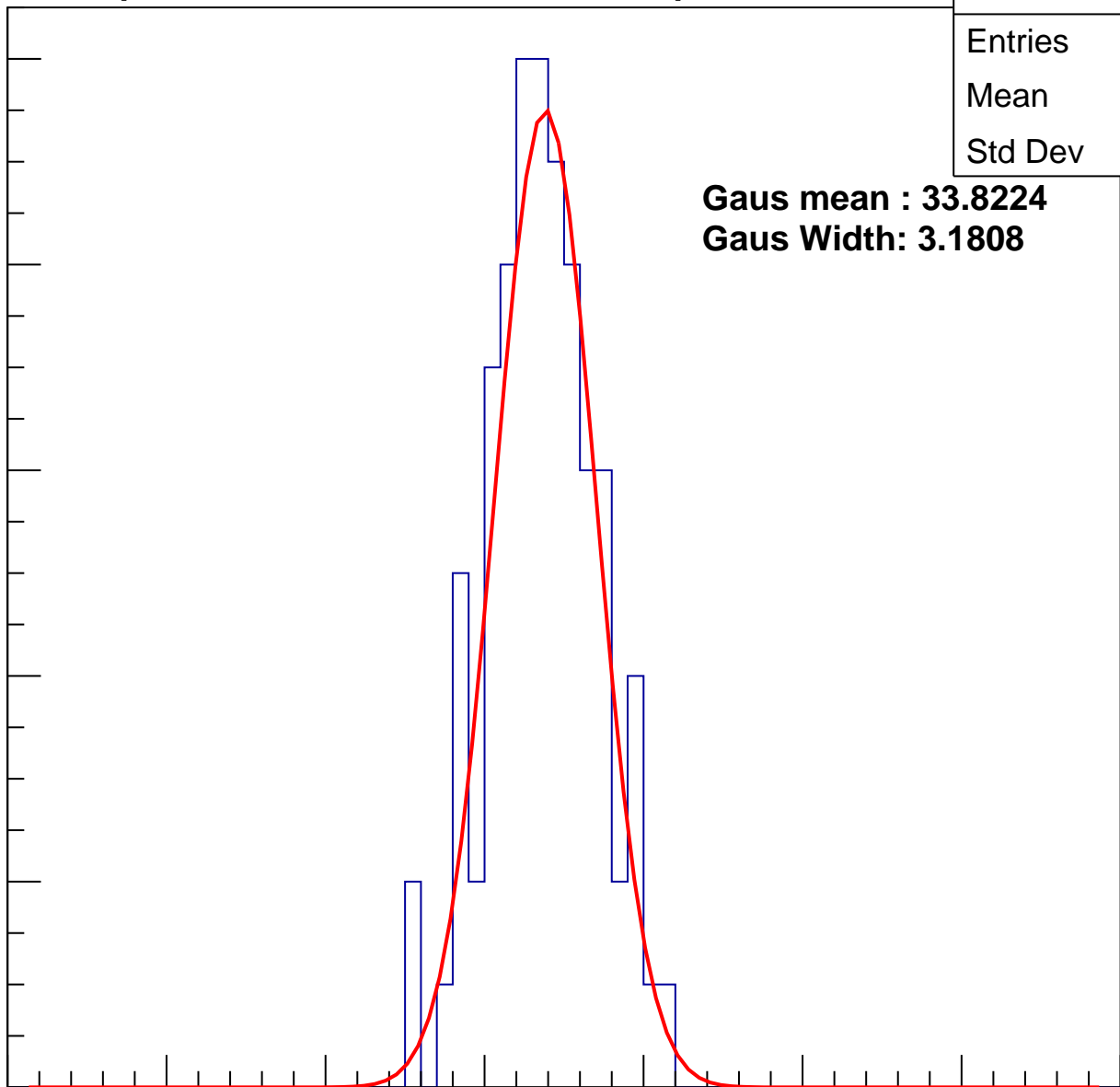
**Gaus Width: 3.1808**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U10-ch55, adc1

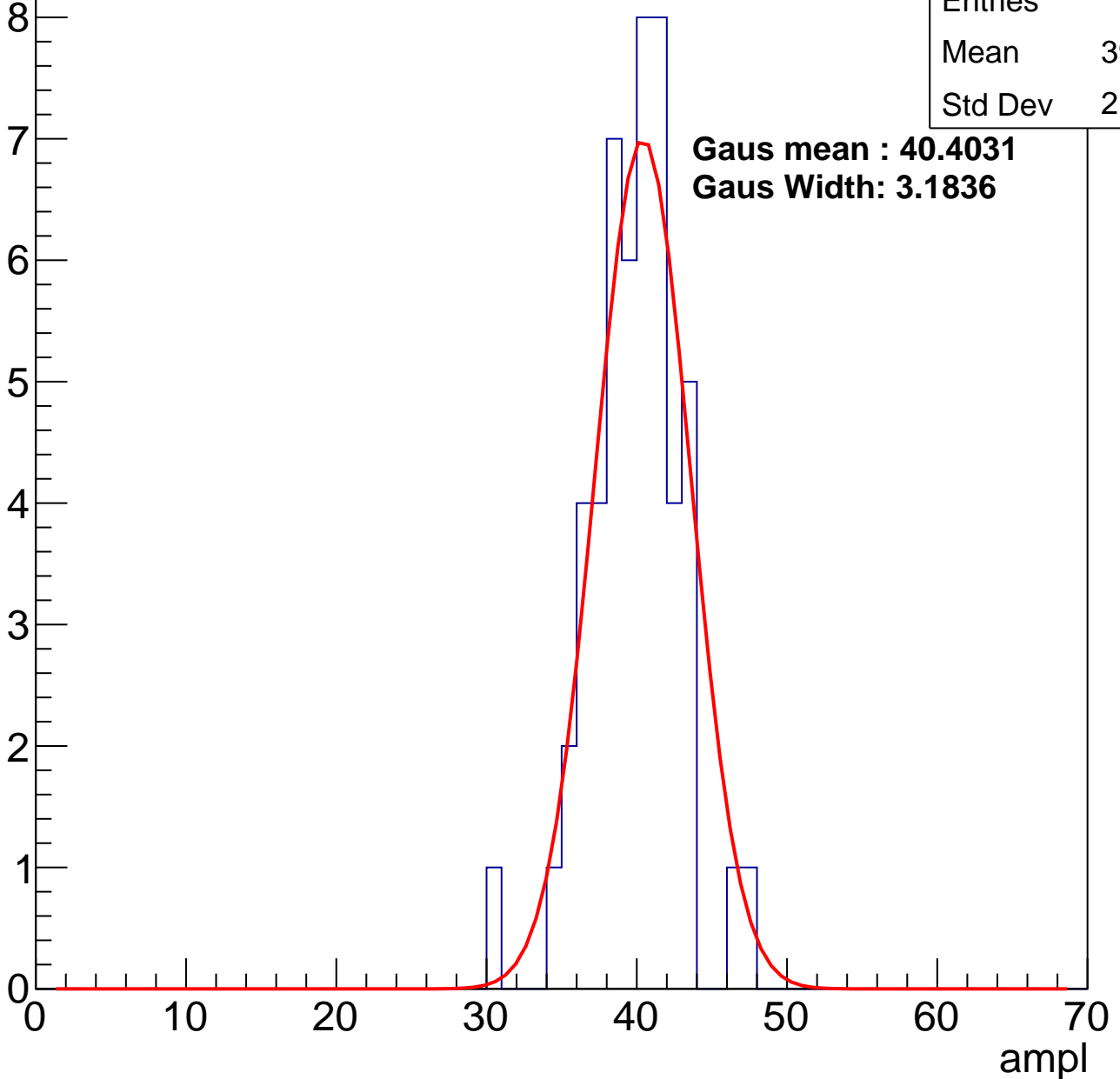
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	39.42
Std Dev	2.964

**Gaus mean : 40.4031**

**Gaus Width: 3.1836**



# B0L001S, U10-ch55, adc2

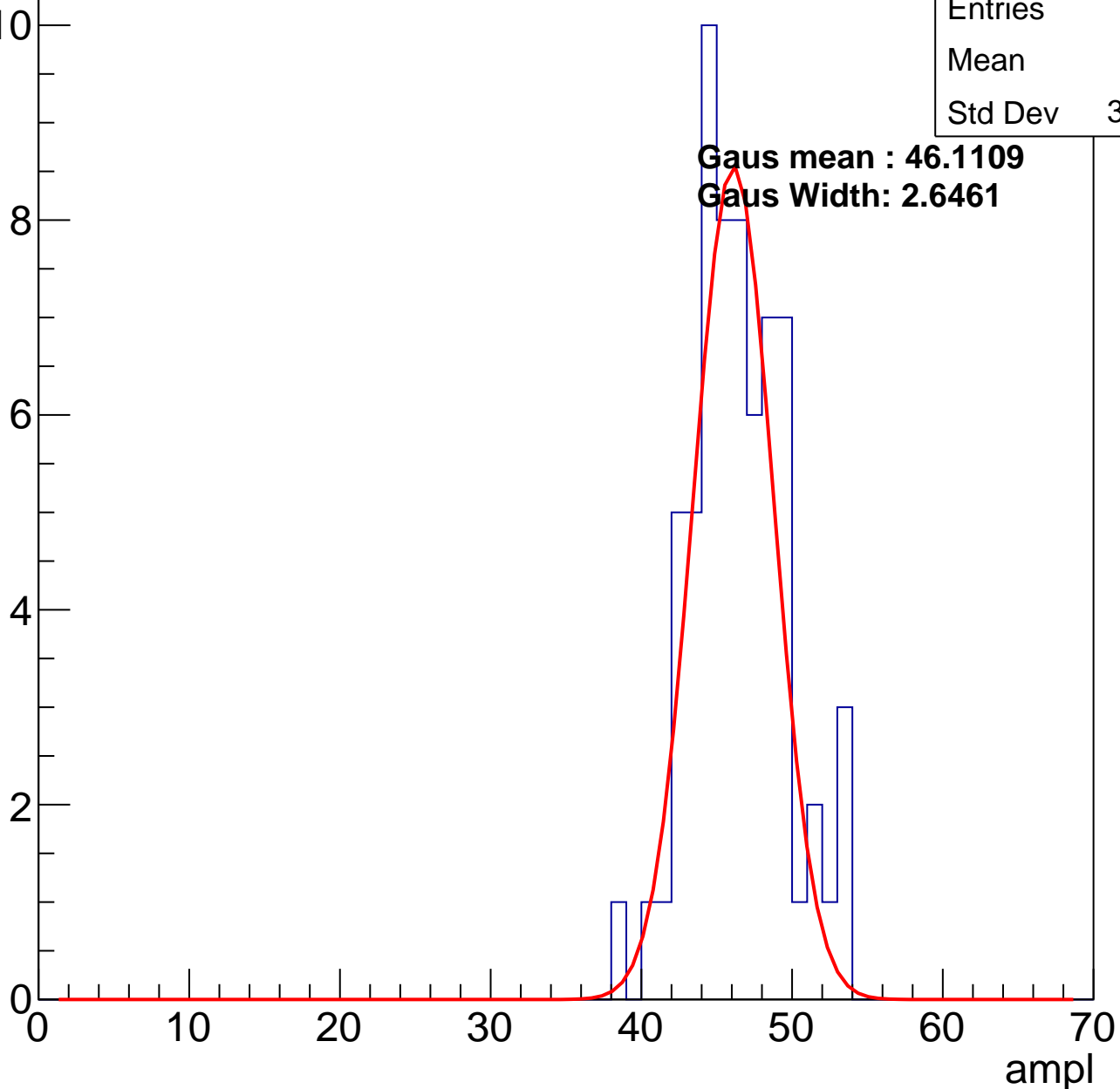
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	46
Std Dev	3.124

**Gaus mean : 46.1109**

**Gaus Width: 2.6461**

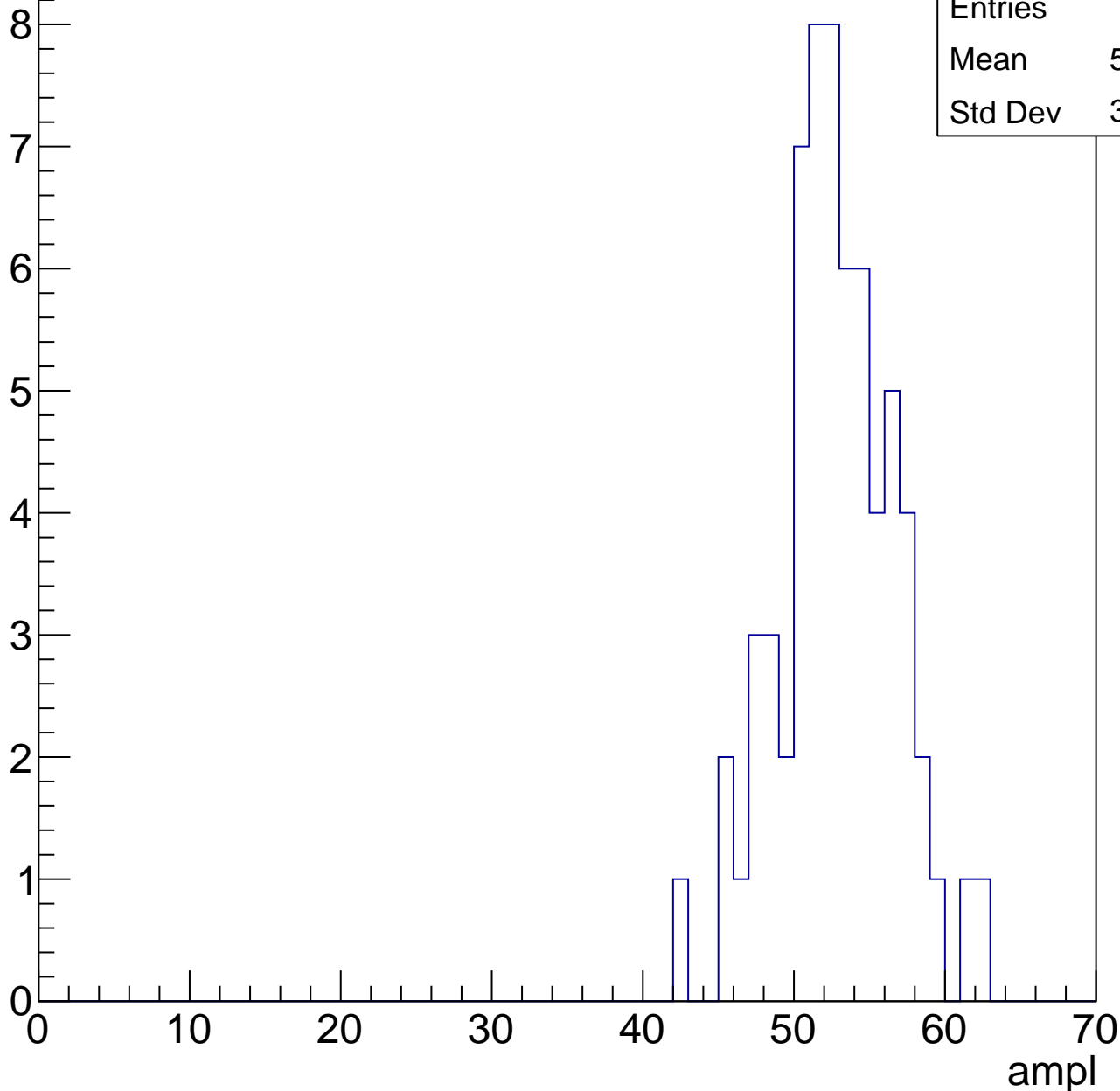


# B0L001S, U10-ch55, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	52.35
Std Dev	3.825

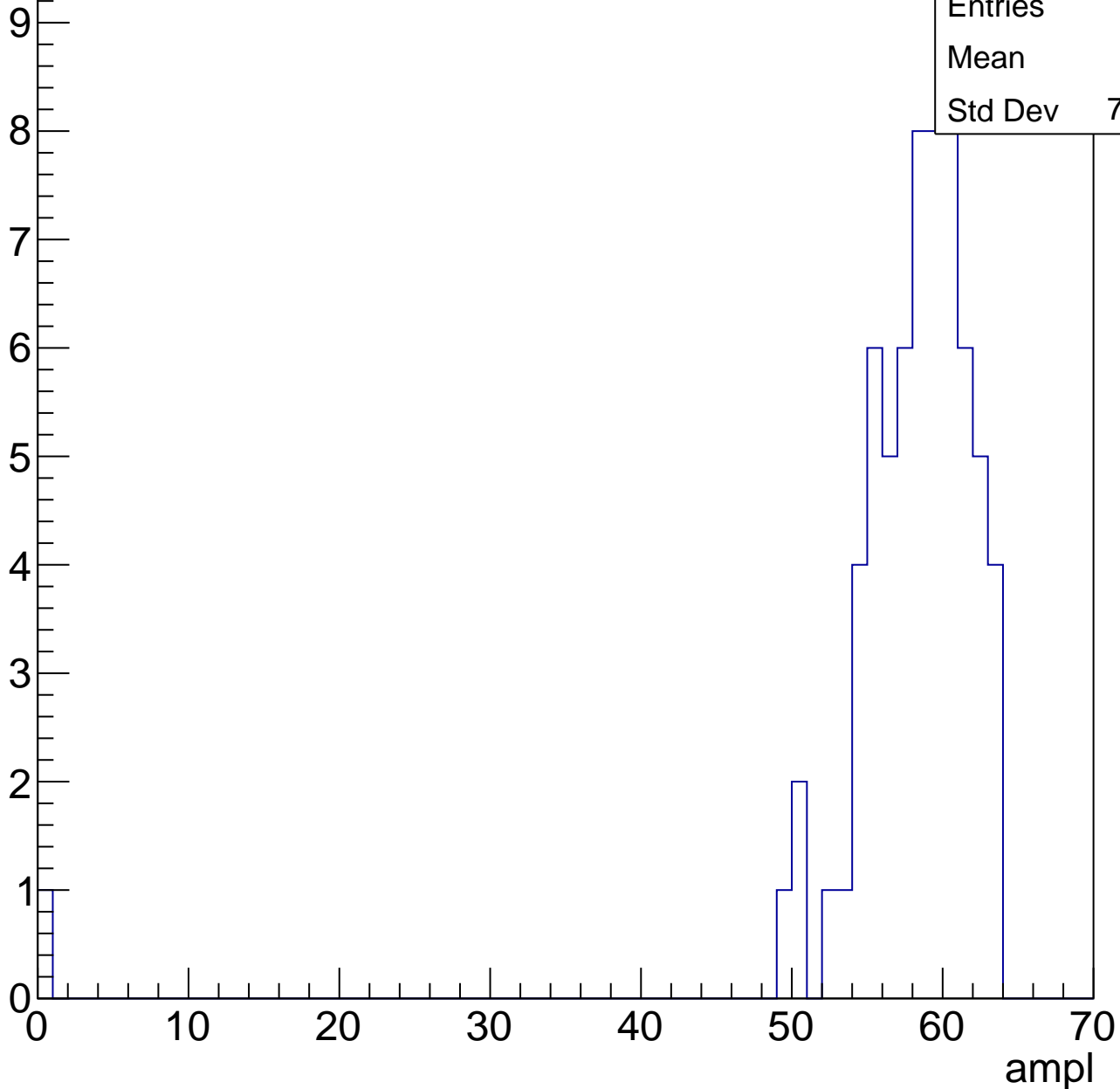


# B0L001S, U10-ch55, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	57.1
Std Dev	7.729

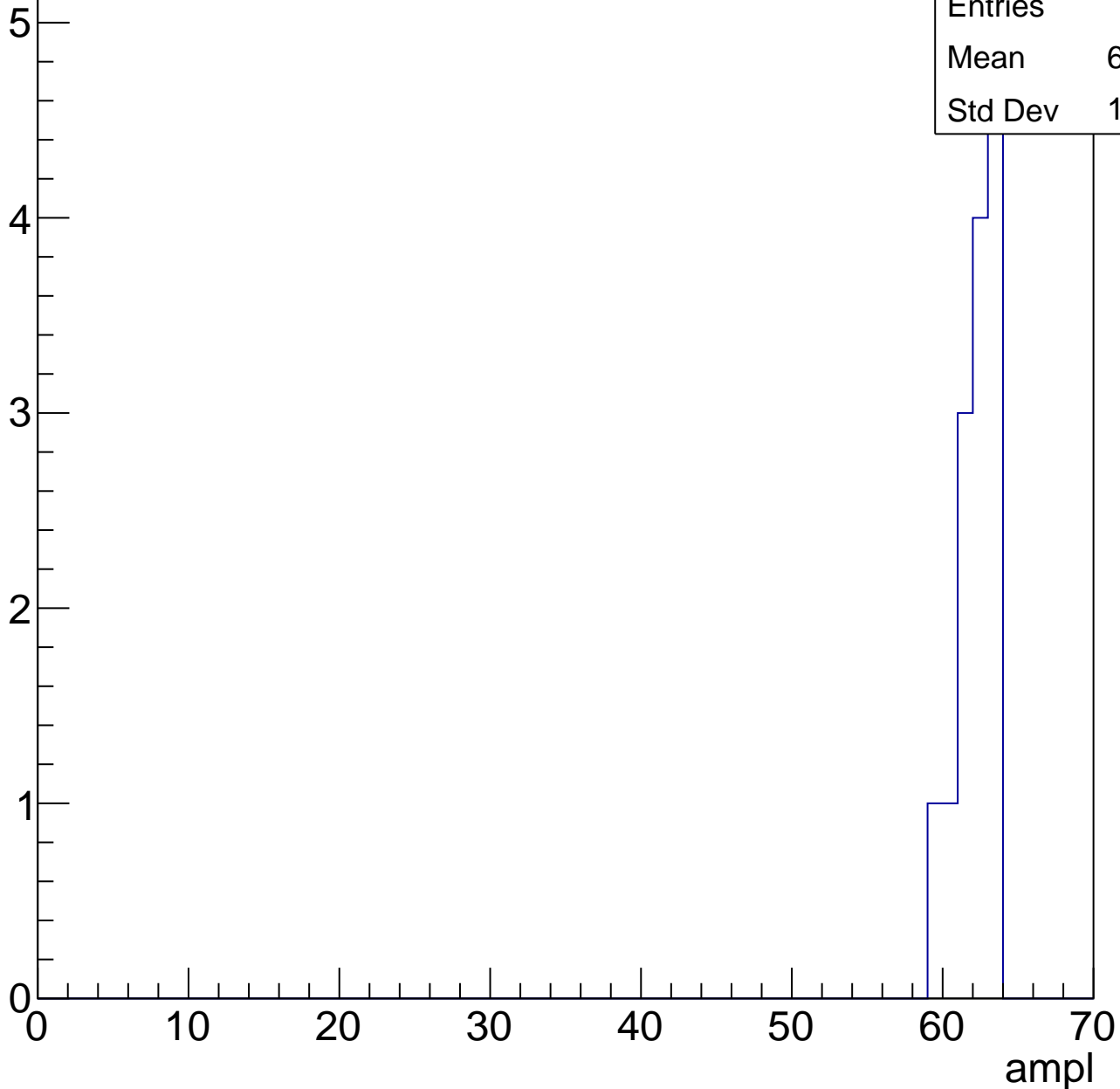


# B0L001S, U10-ch55, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	14
Mean	61.79
Std Dev	1.206



# B0L001S, U10-ch55, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch55, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U10-ch56, adc0

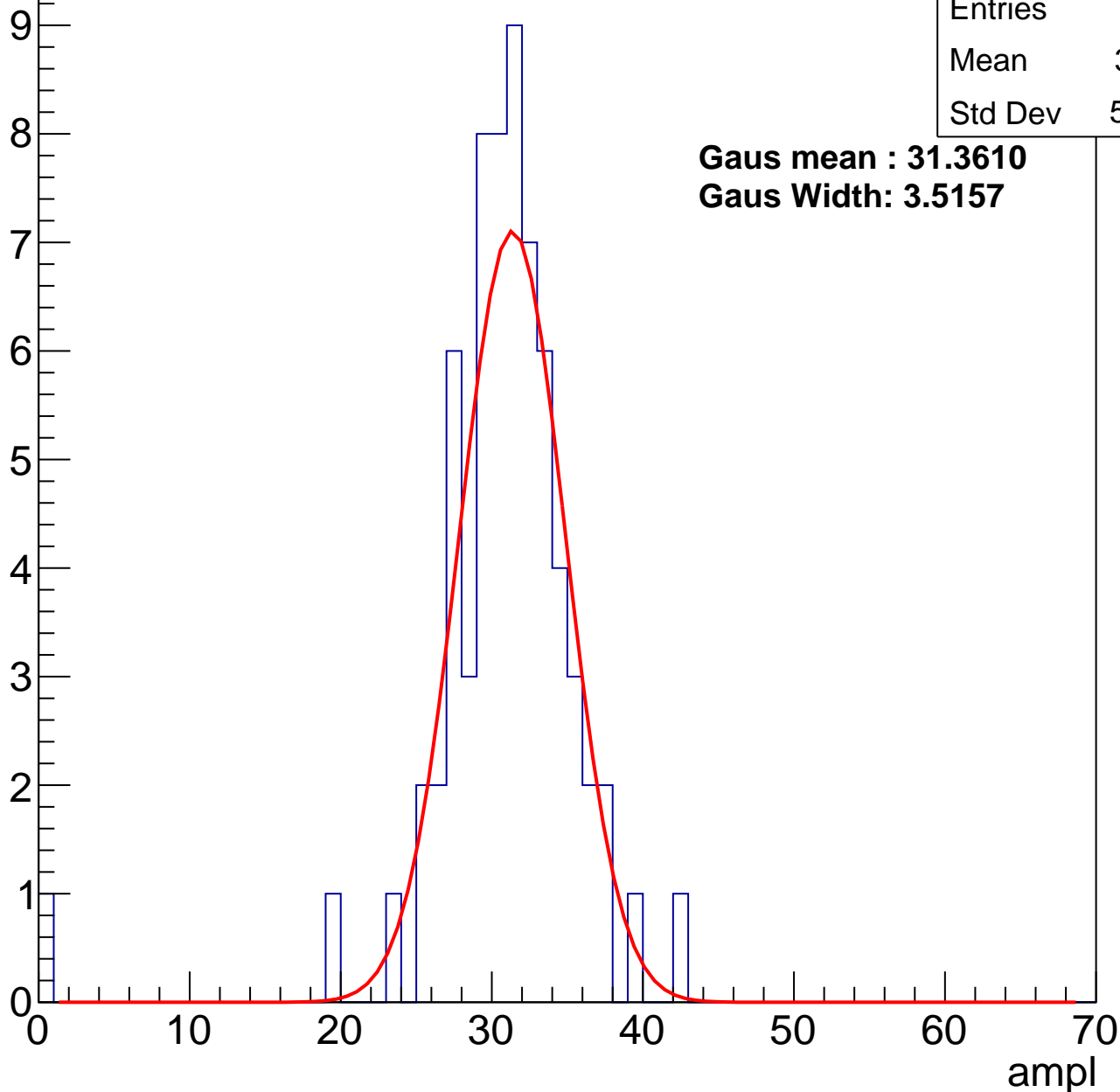
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	30.31
Std Dev	5.247

**Gaus mean : 31.3610**

**Gaus Width: 3.5157**



# B0L001S, U10-ch56, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	76
Mean	37.74
Std Dev	3.326

**Gaus mean : 37.8067**

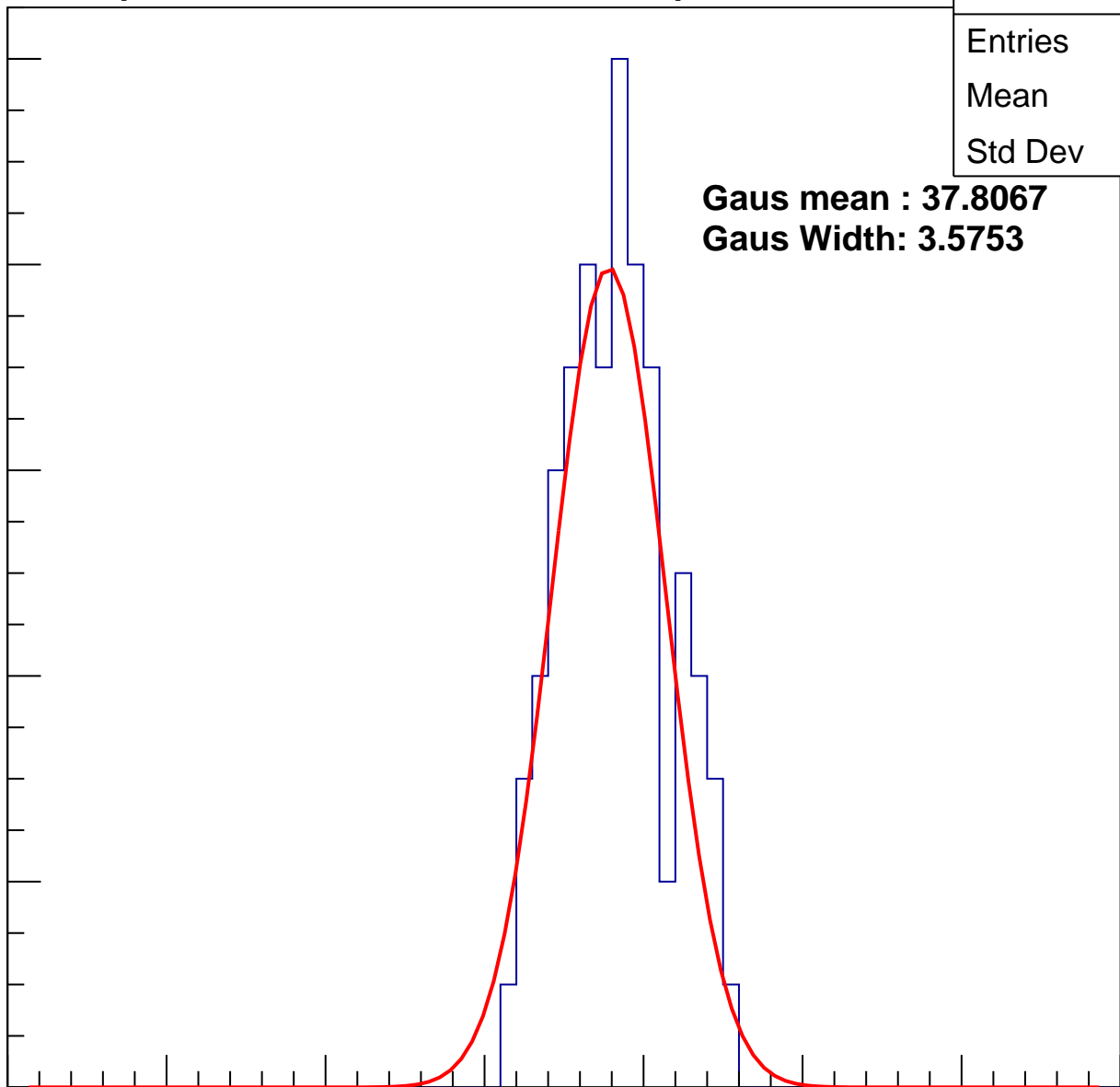
**Gaus Width: 3.5753**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



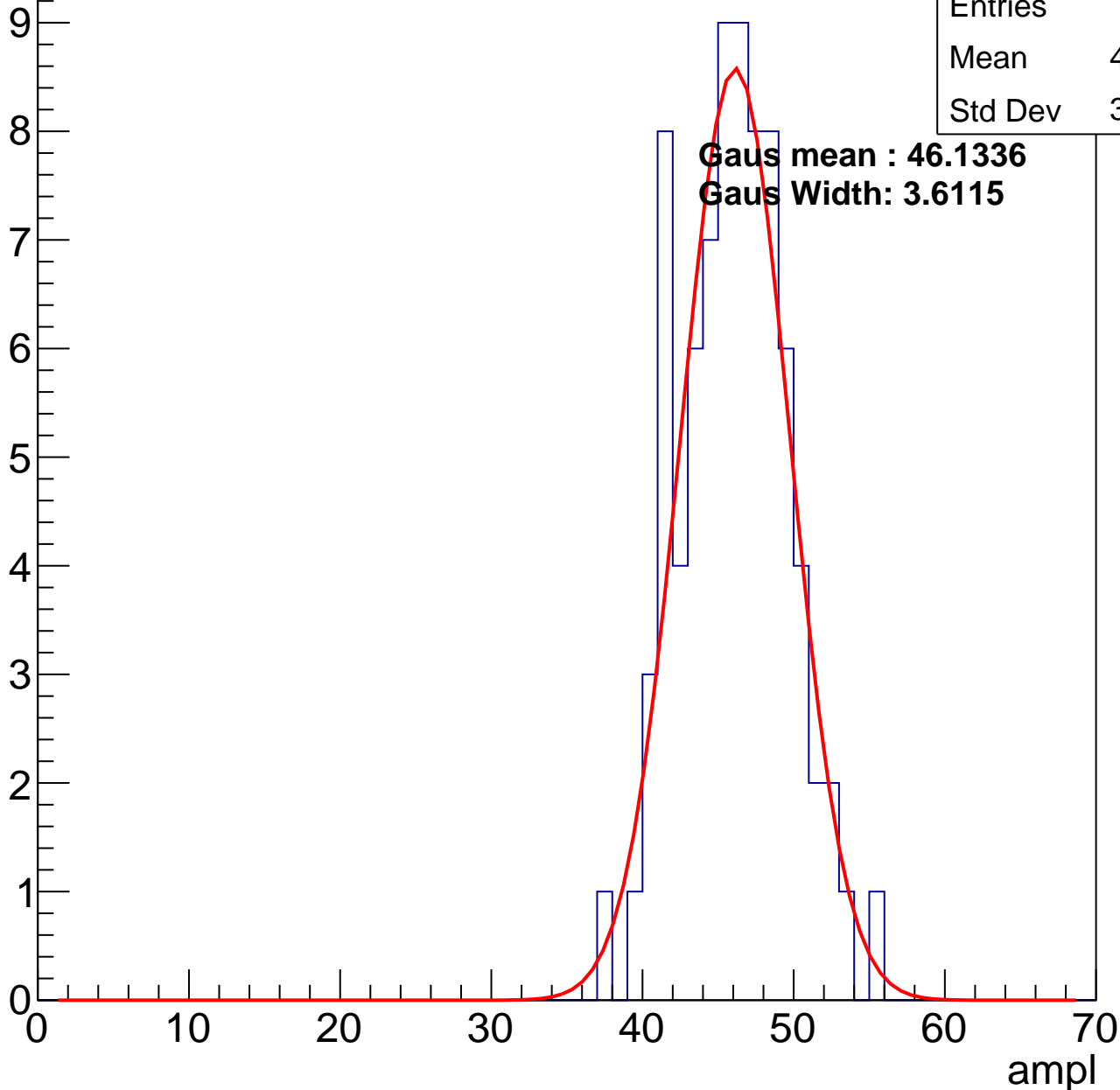
# B0L001S, U10-ch56, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	80
Mean	45.56
Std Dev	3.514

**Gaus mean : 46.1336**  
**Gaus Width: 3.6115**

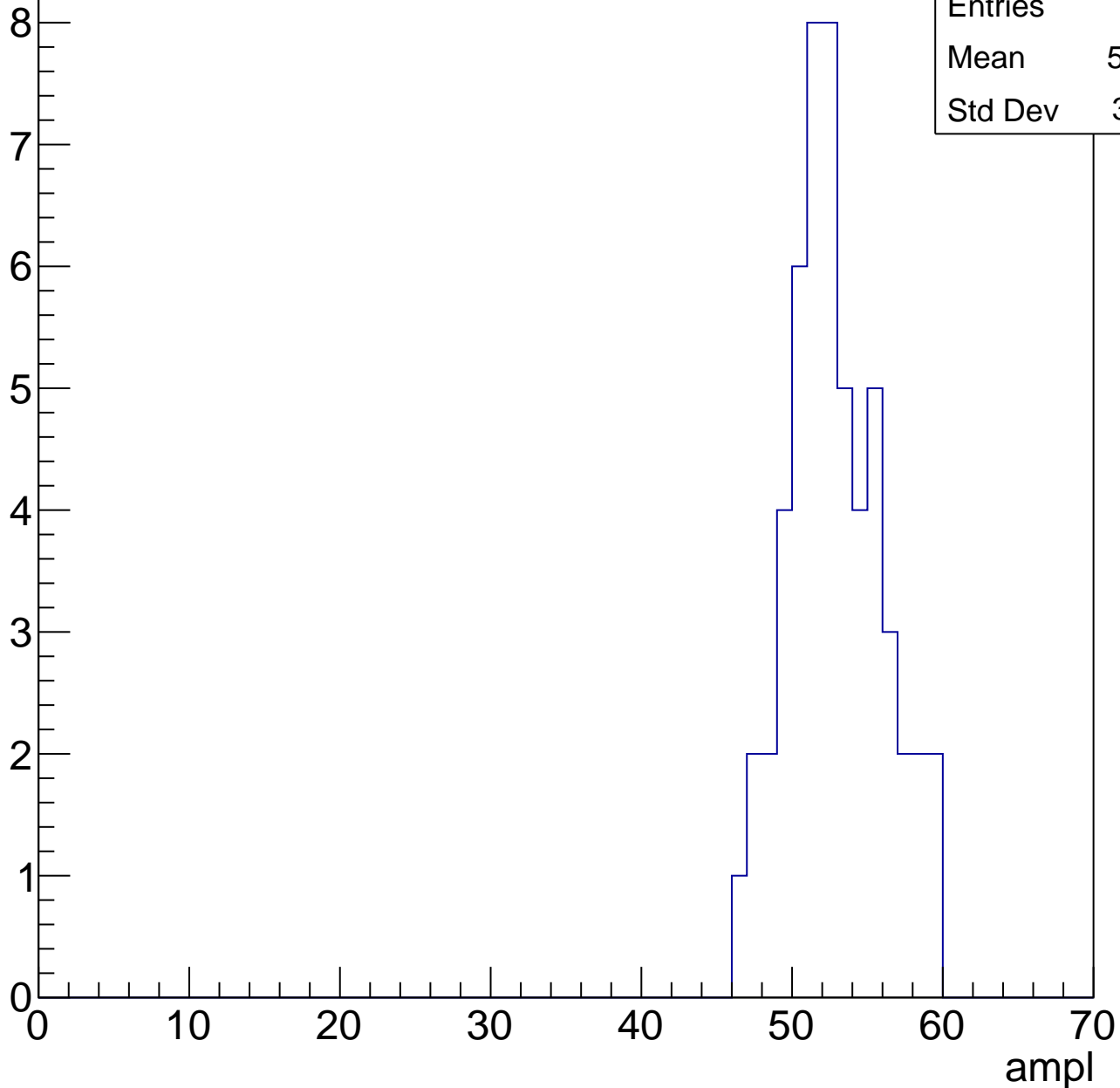


# B0L001S, U10-ch56, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	52.37
Std Dev	3.081

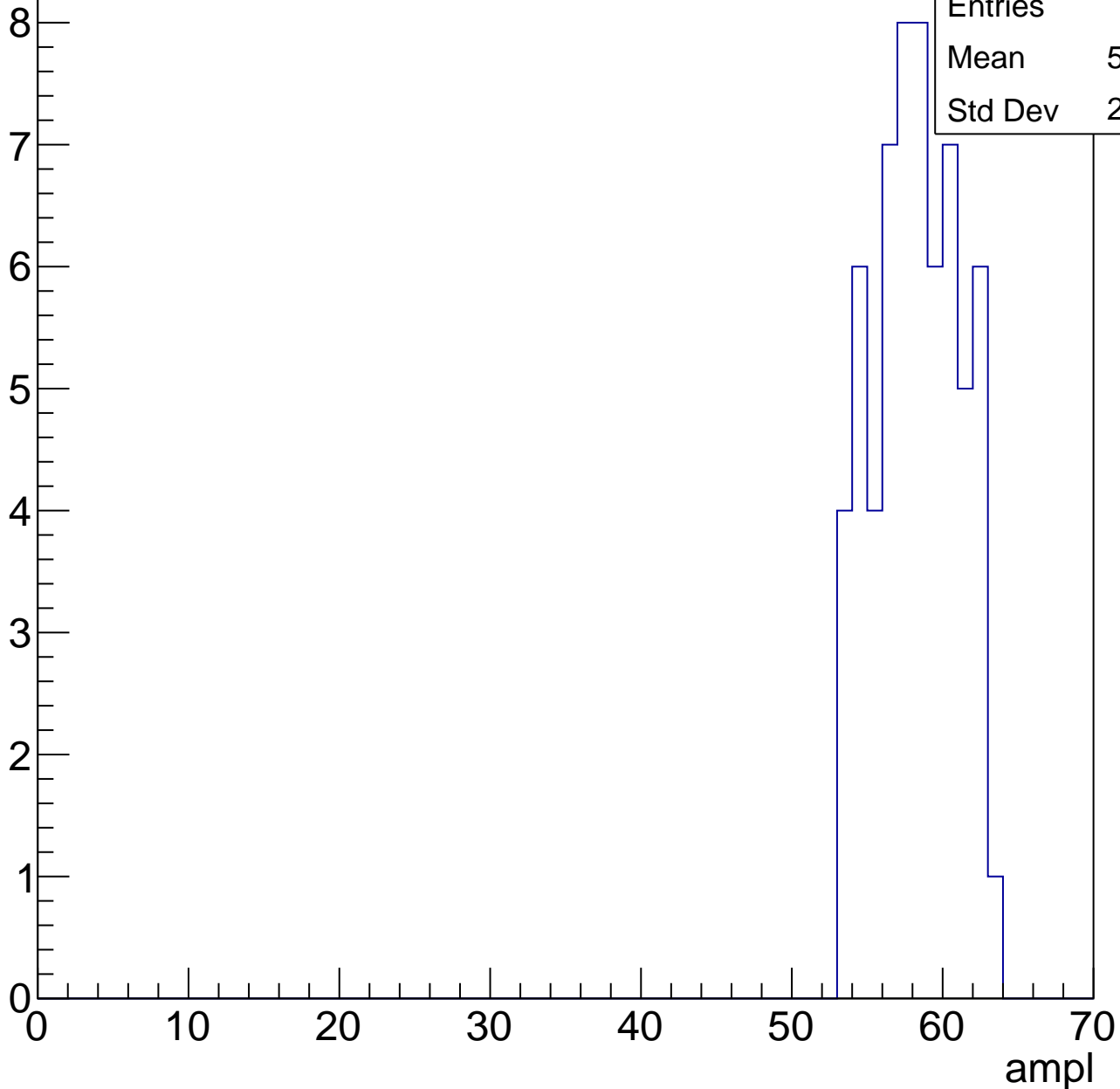


# B0L001S, U10-ch56, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	57.77
Std Dev	2.738

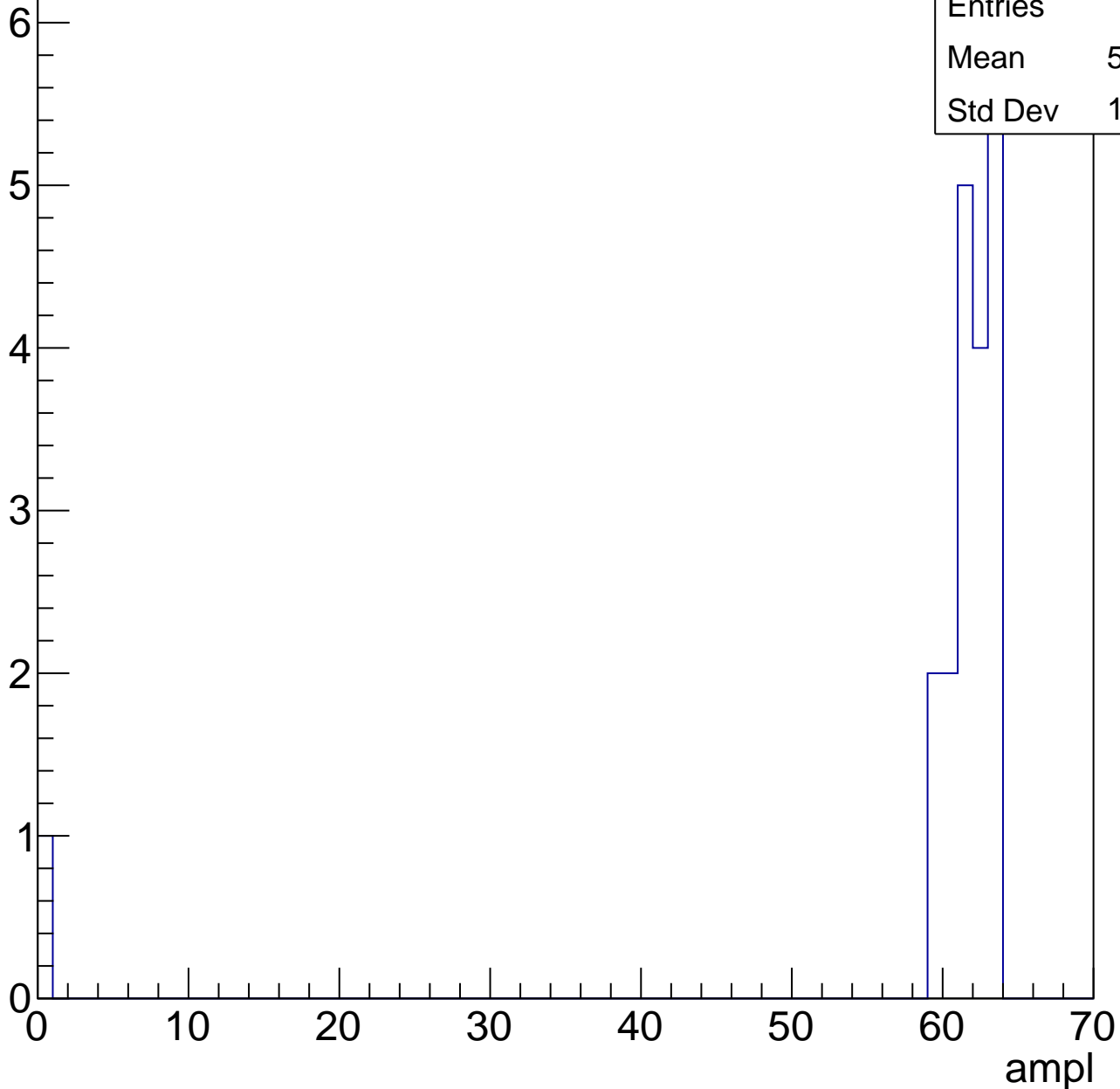


# B0L001S, U10-ch56, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	20
Mean	58.45
Std Dev	13.47



# B0L001S, U10-ch56, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch56, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U10-ch57, adc0

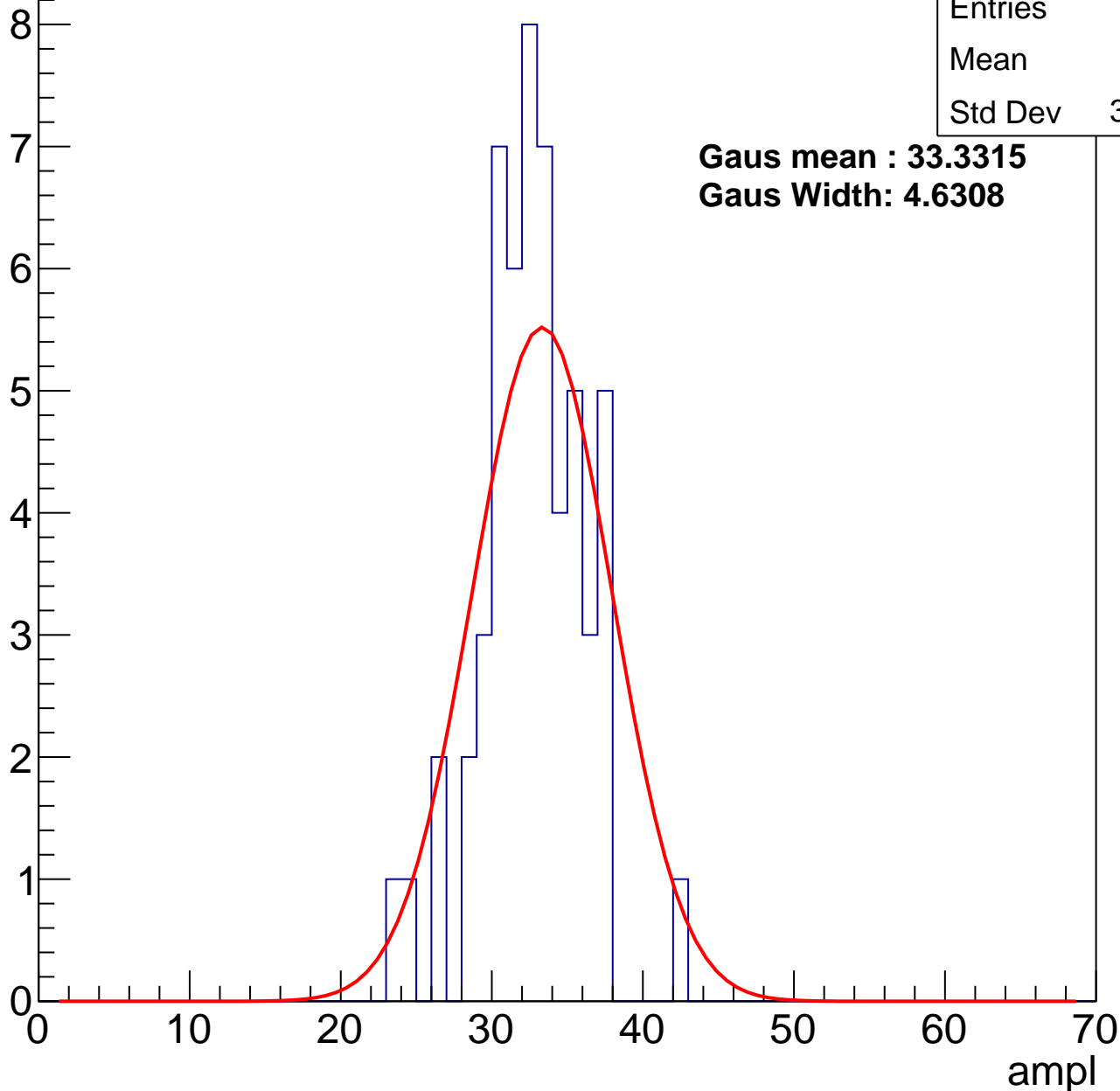
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	32.2
Std Dev	3.435

**Gaus mean : 33.3315**

**Gaus Width: 4.6308**



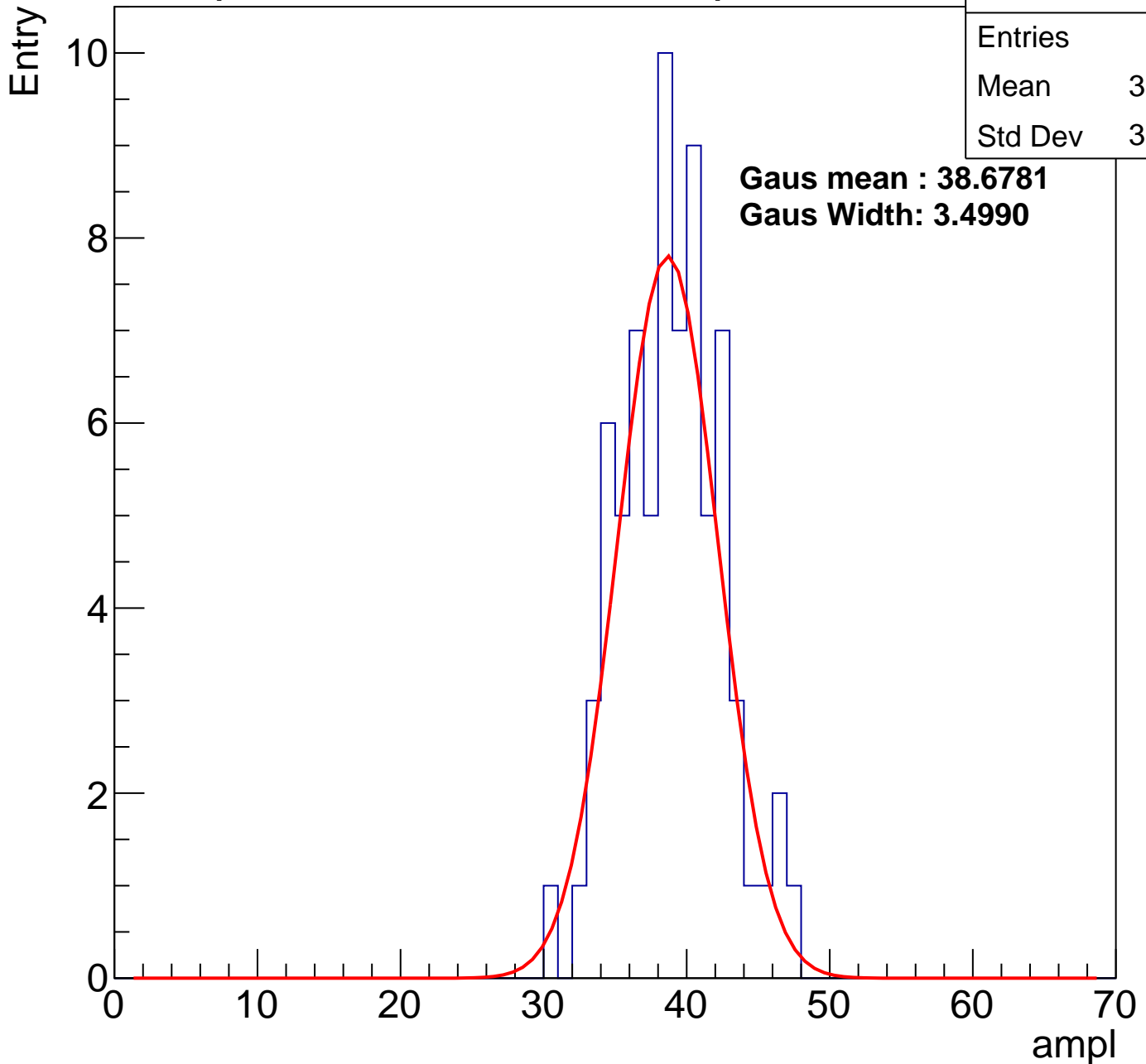
# B0L001S, U10-ch57, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	74
Mean	38.46
Std Dev	3.492

**Gaus mean : 38.6781**

**Gaus Width: 3.4990**



# B0L001S, U10-ch57, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	71
Mean	45.87
Std Dev	3.39

**Gaus mean : 46.7440**

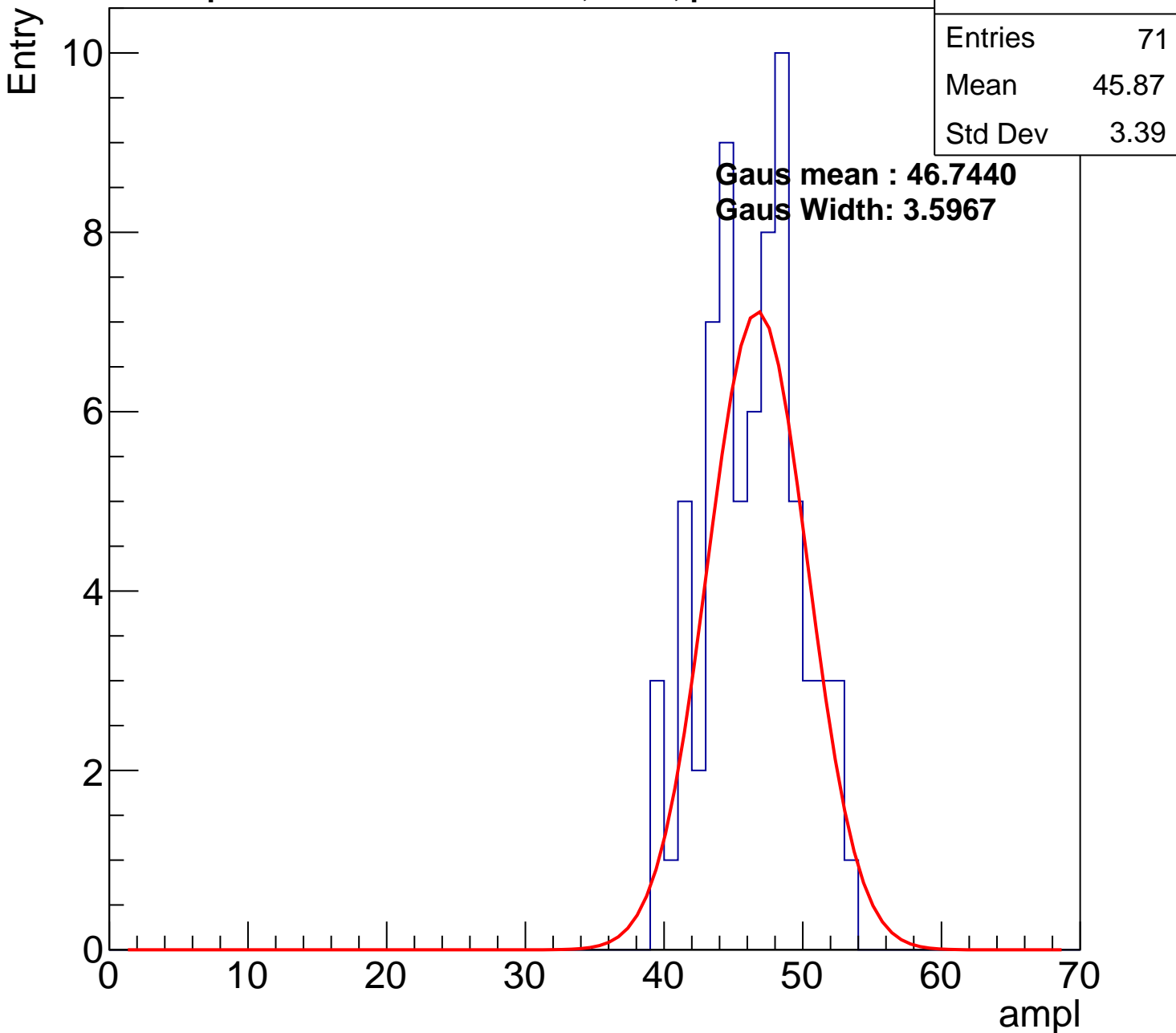
**Gaus Width: 3.5967**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

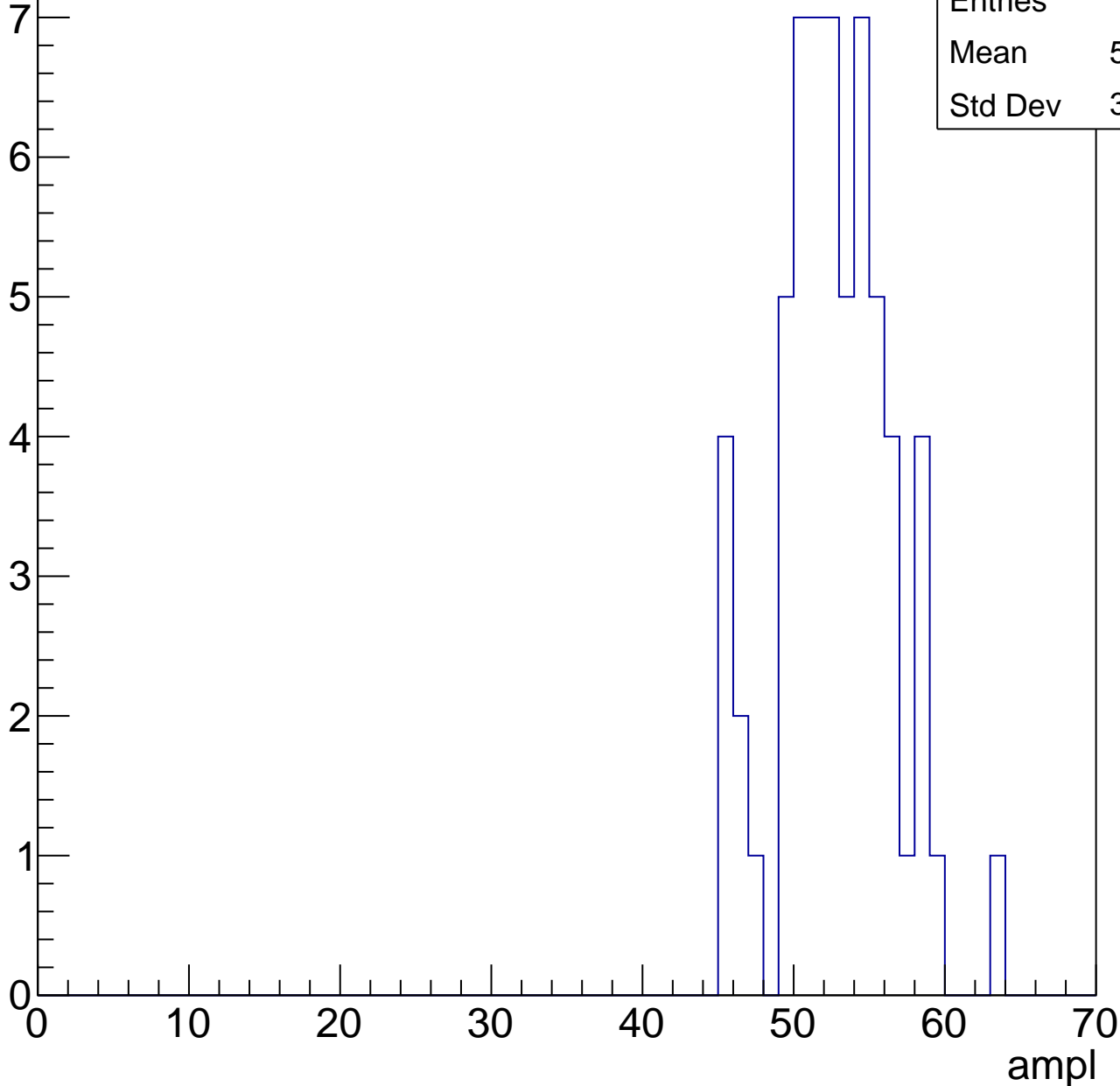


# B0L001S, U10-ch57, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

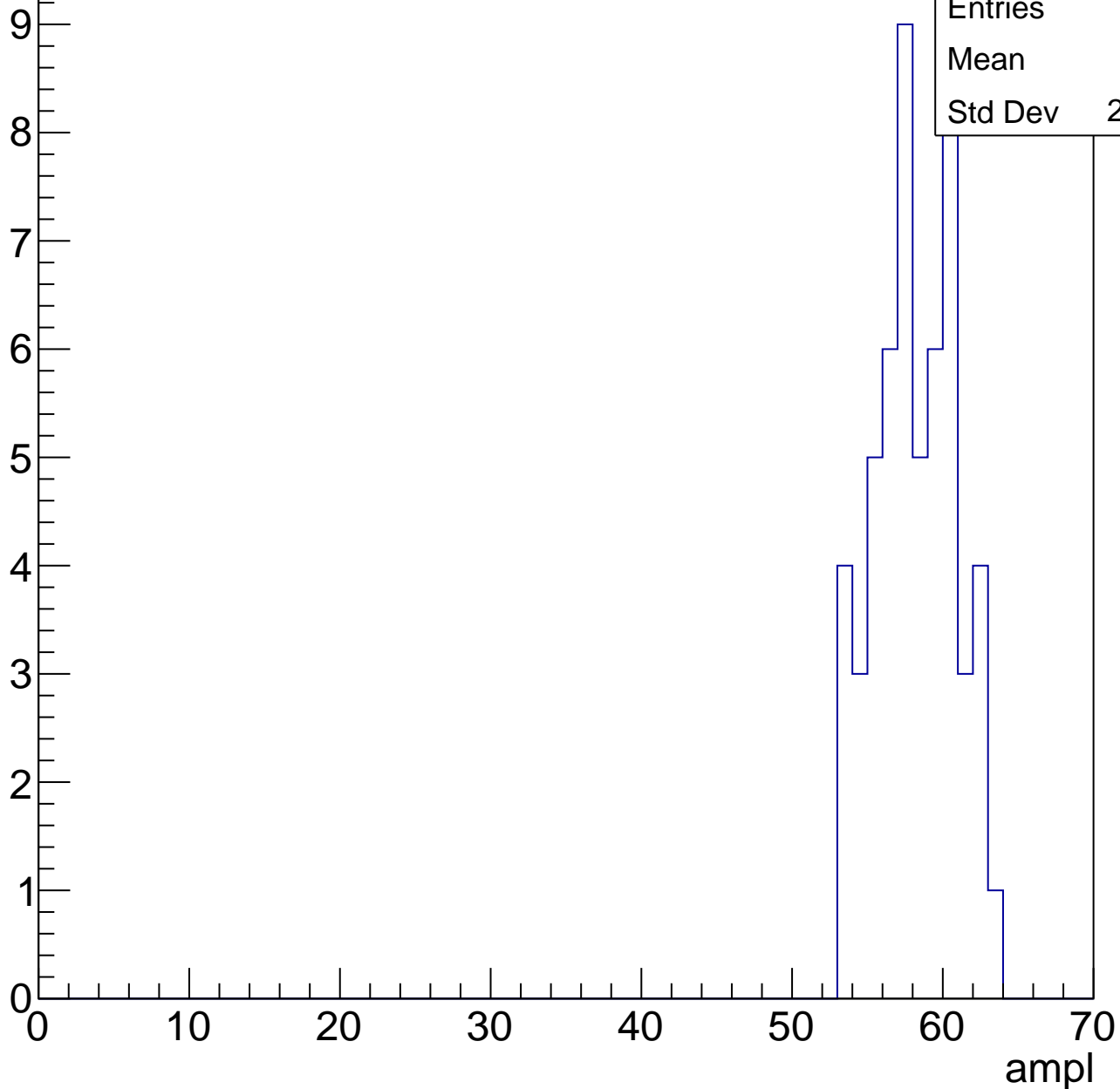
Entries	61
Mean	52.26
Std Dev	3.732



# B0L001S, U10-ch57, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

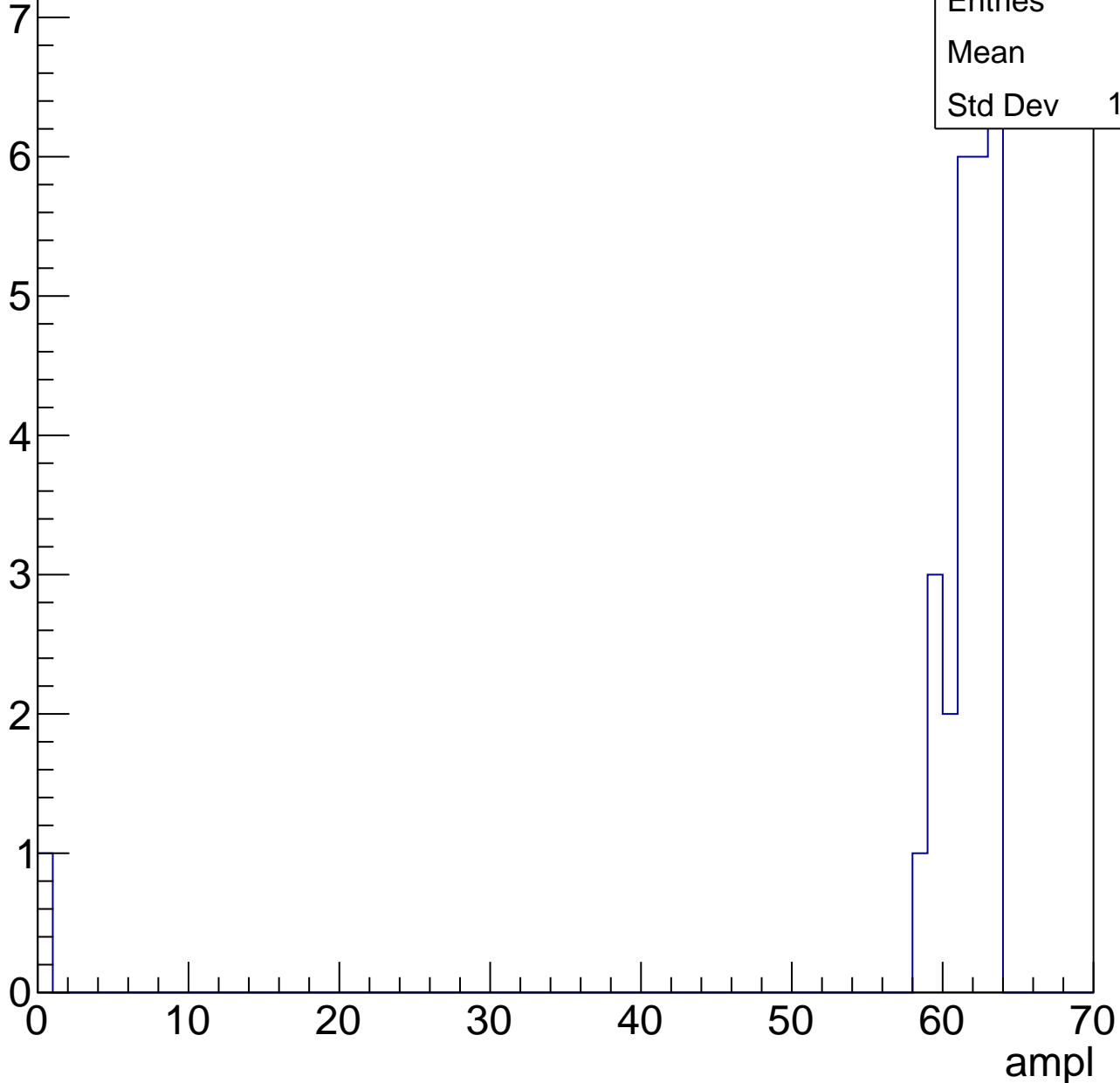


# B0L001S, U10-ch57, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	26
Mean	59
Std Dev	11.89



# B0L001S, U10-ch57, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch57, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U10-ch58, adc0

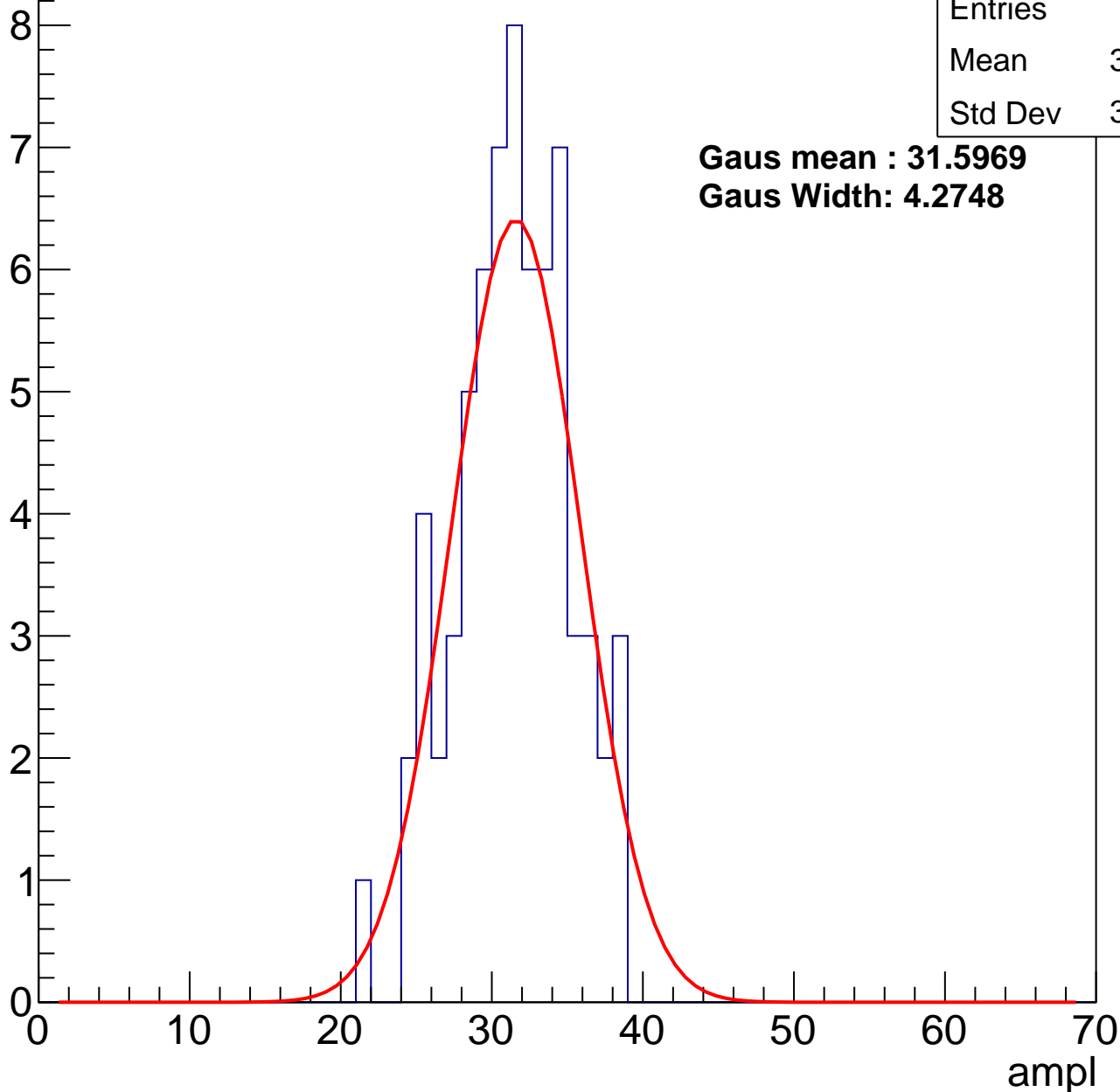
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	30.93
Std Dev	3.739

**Gaus mean : 31.5969**

**Gaus Width: 4.2748**



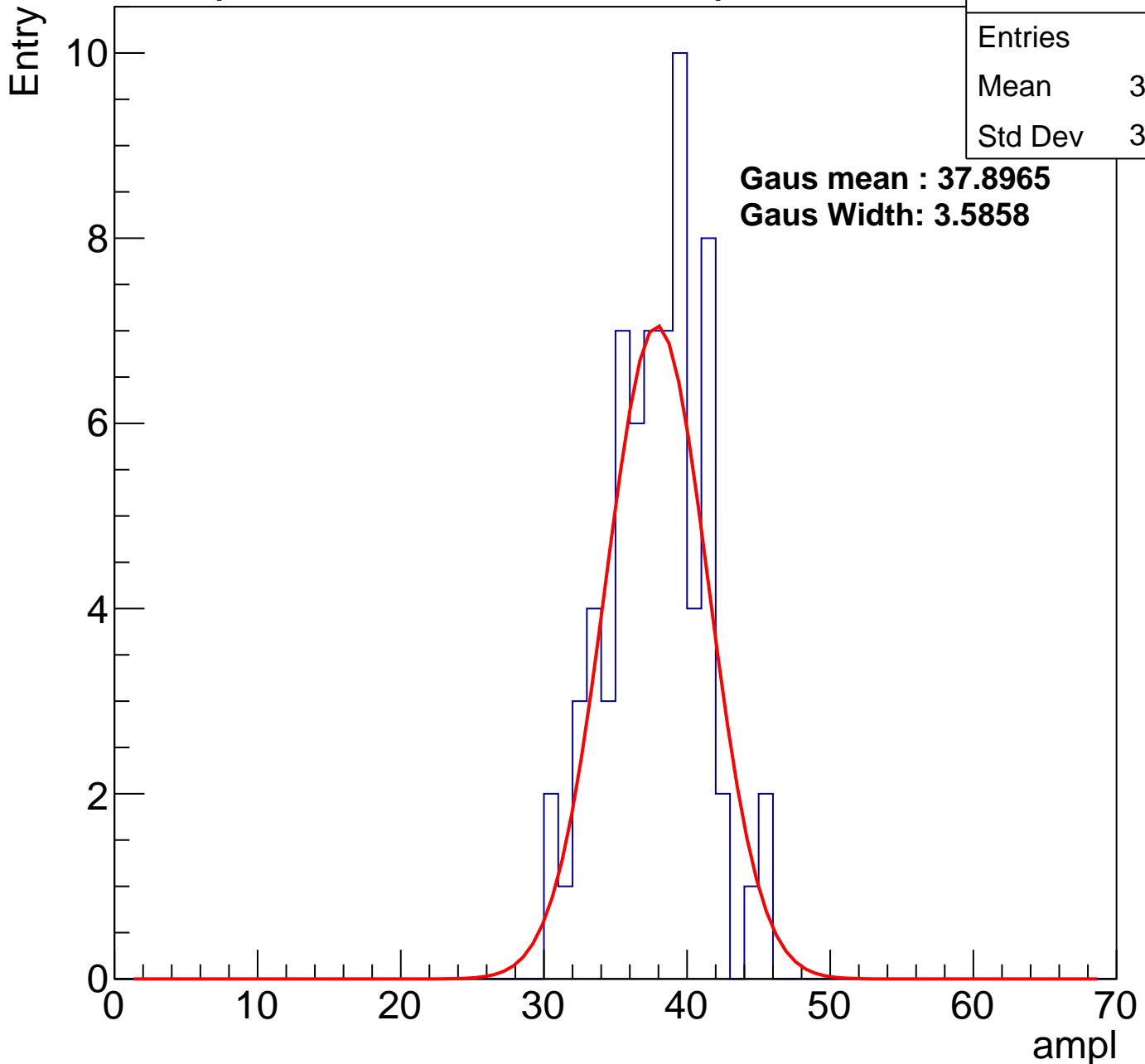
# B0L001S, U10-ch58, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	67
Mean	37.36
Std Dev	3.376

**Gaus mean : 37.8965**

**Gaus Width: 3.5858**



# B0L001S, U10-ch58, adc2

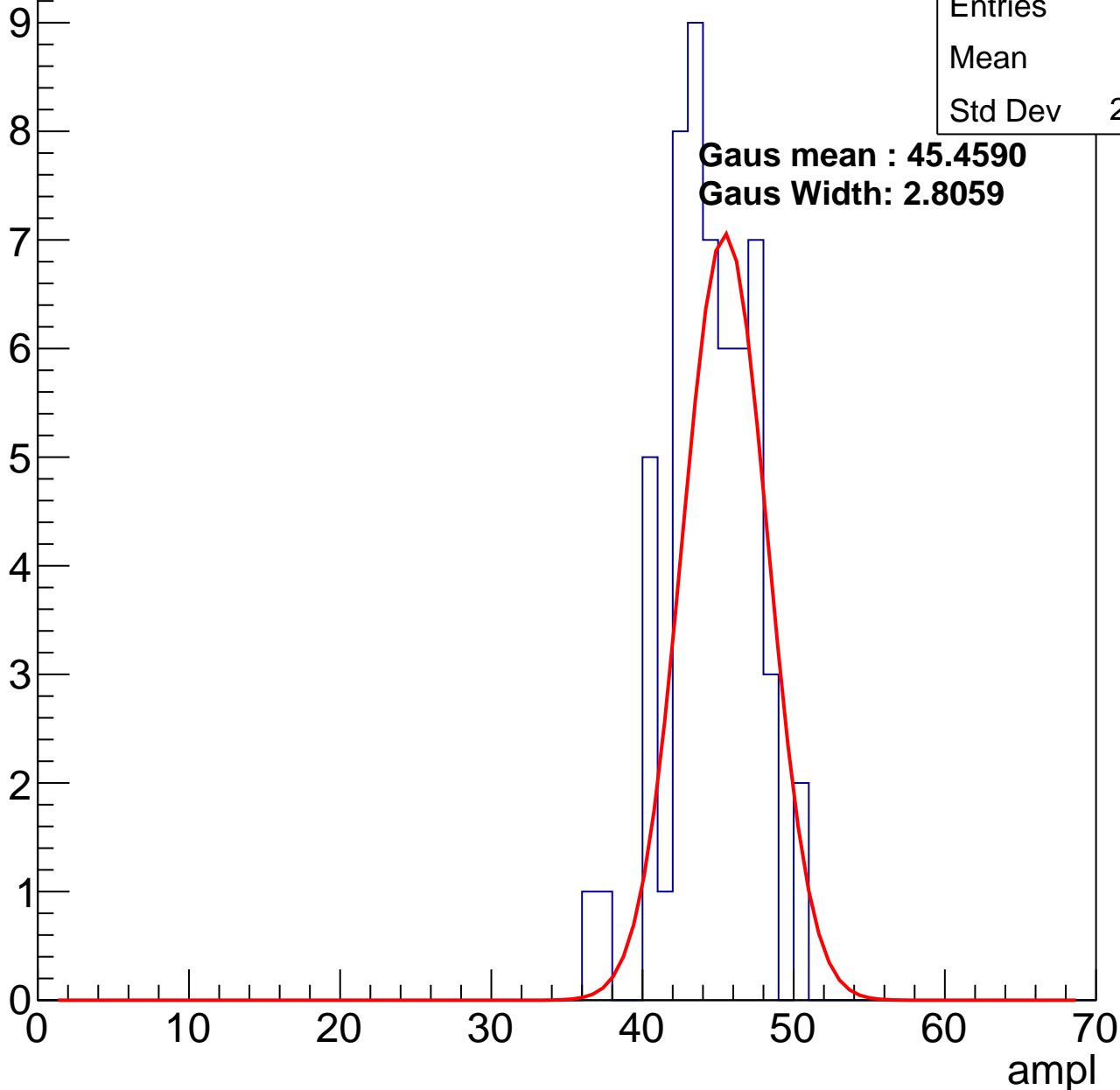
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	44
Std Dev	2.854

**Gaus mean : 45.4590**

**Gaus Width: 2.8059**

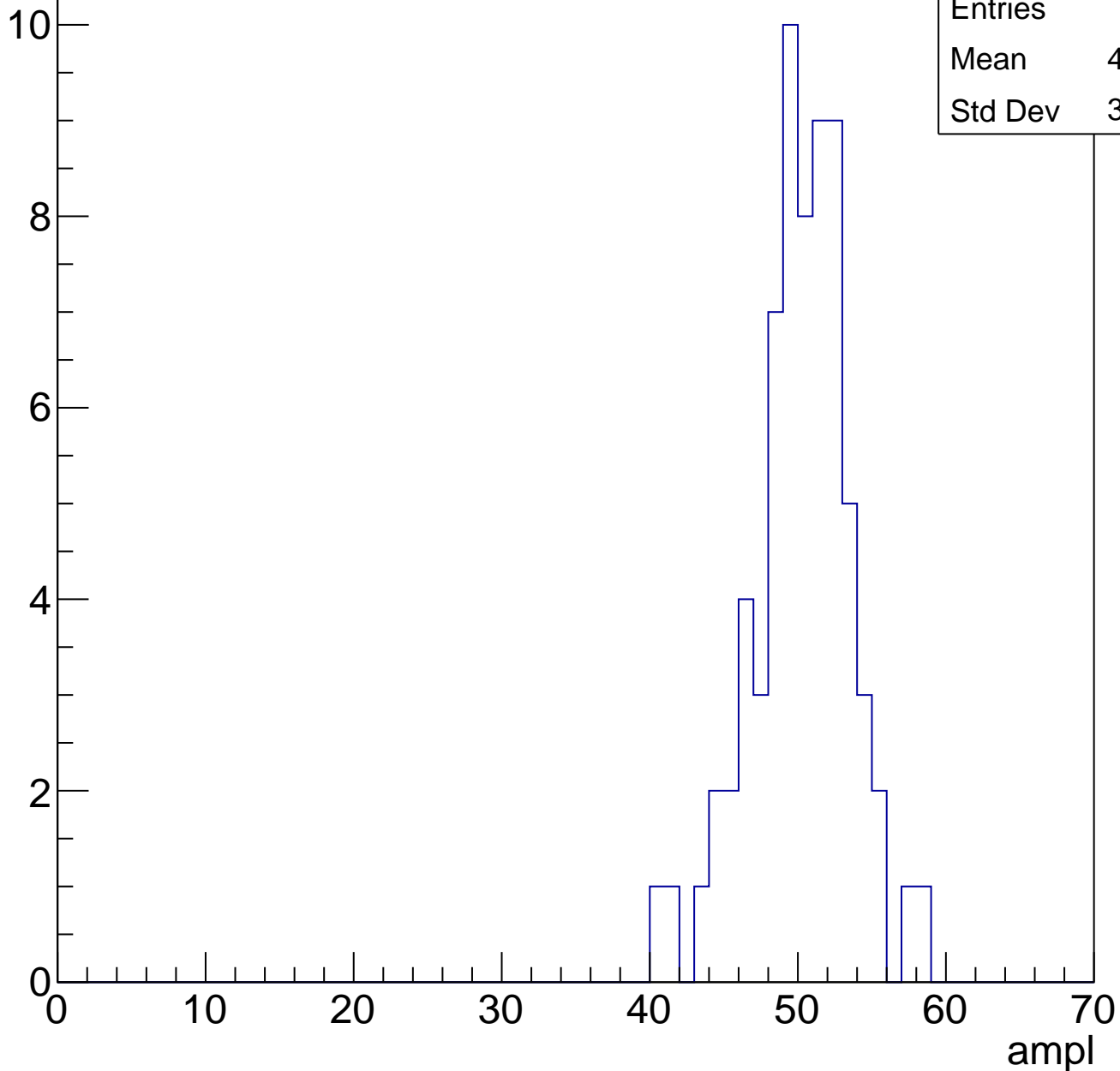


# B0L001S, U10-ch58, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	69
Mean	49.74
Std Dev	3.356

Entry

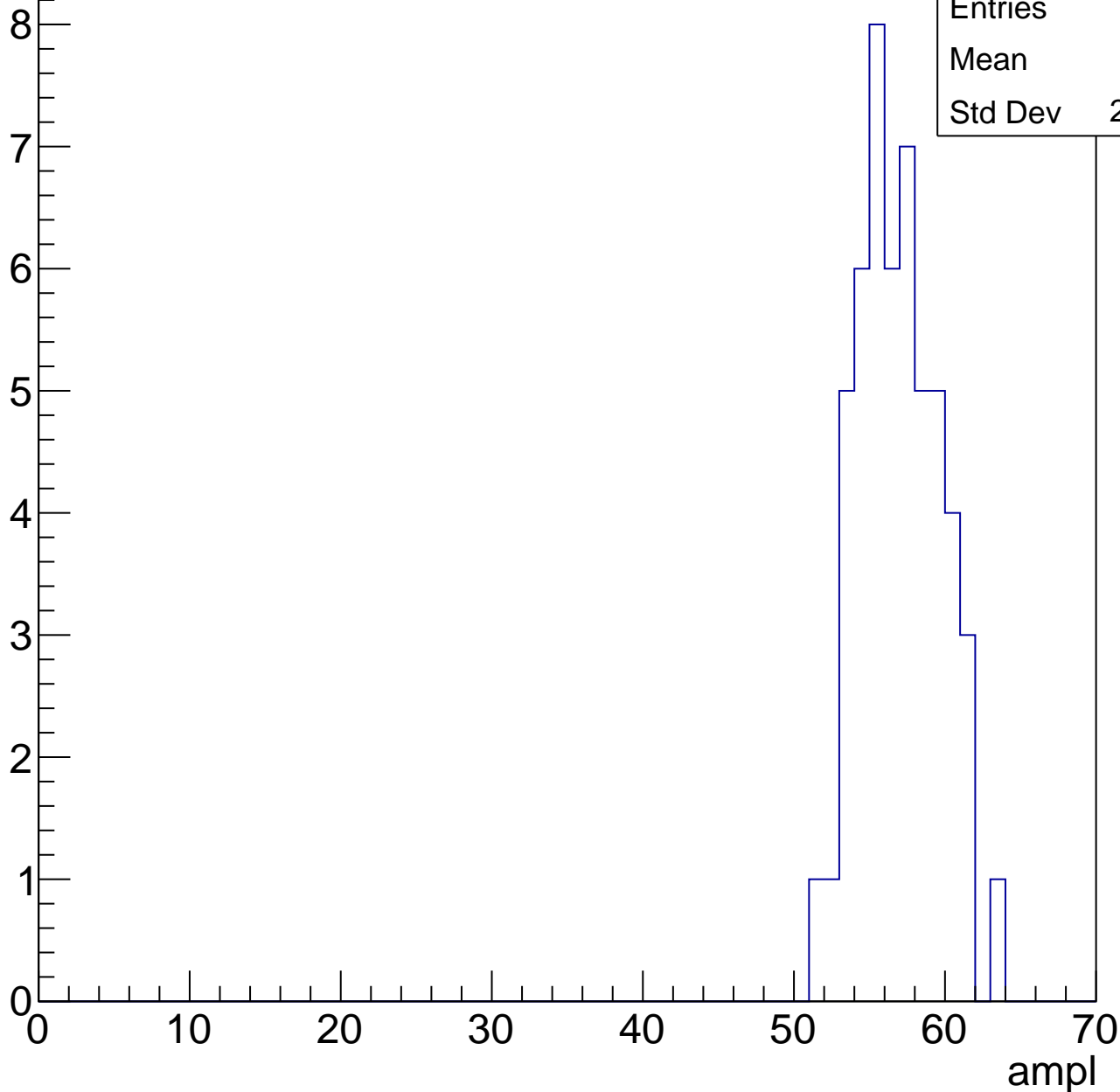


# B0L001S, U10-ch58, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	56.5
Std Dev	2.649

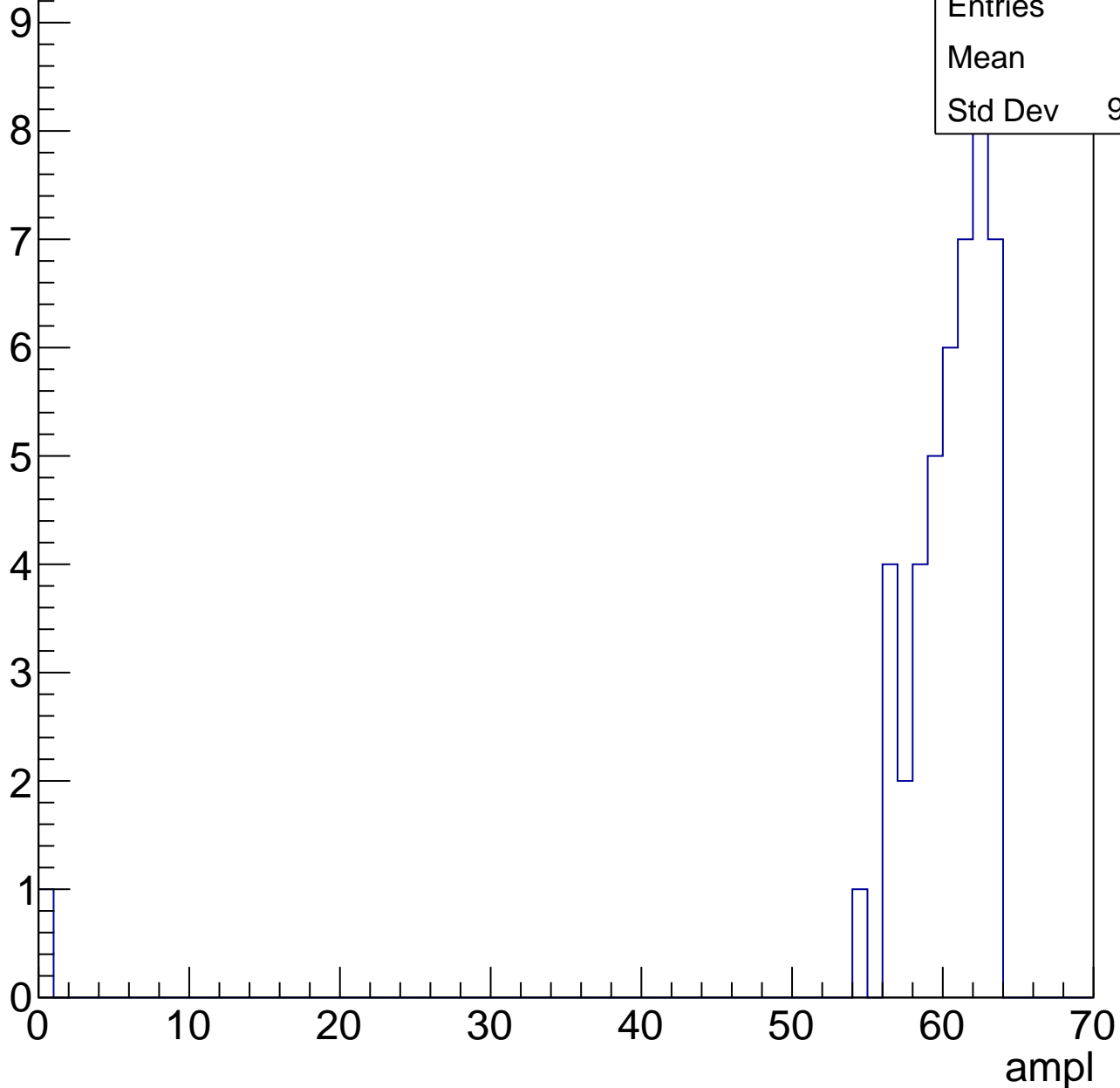


# B0L001S, U10-ch58, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	46
Mean	58.8
Std Dev	9.064



# B0L001S, U10-ch58, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.67
Std Dev	0.4714

ampl

0 10 20 30 40 50 60 70



# B0L001S, U10-ch58, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U10-ch59, adc0

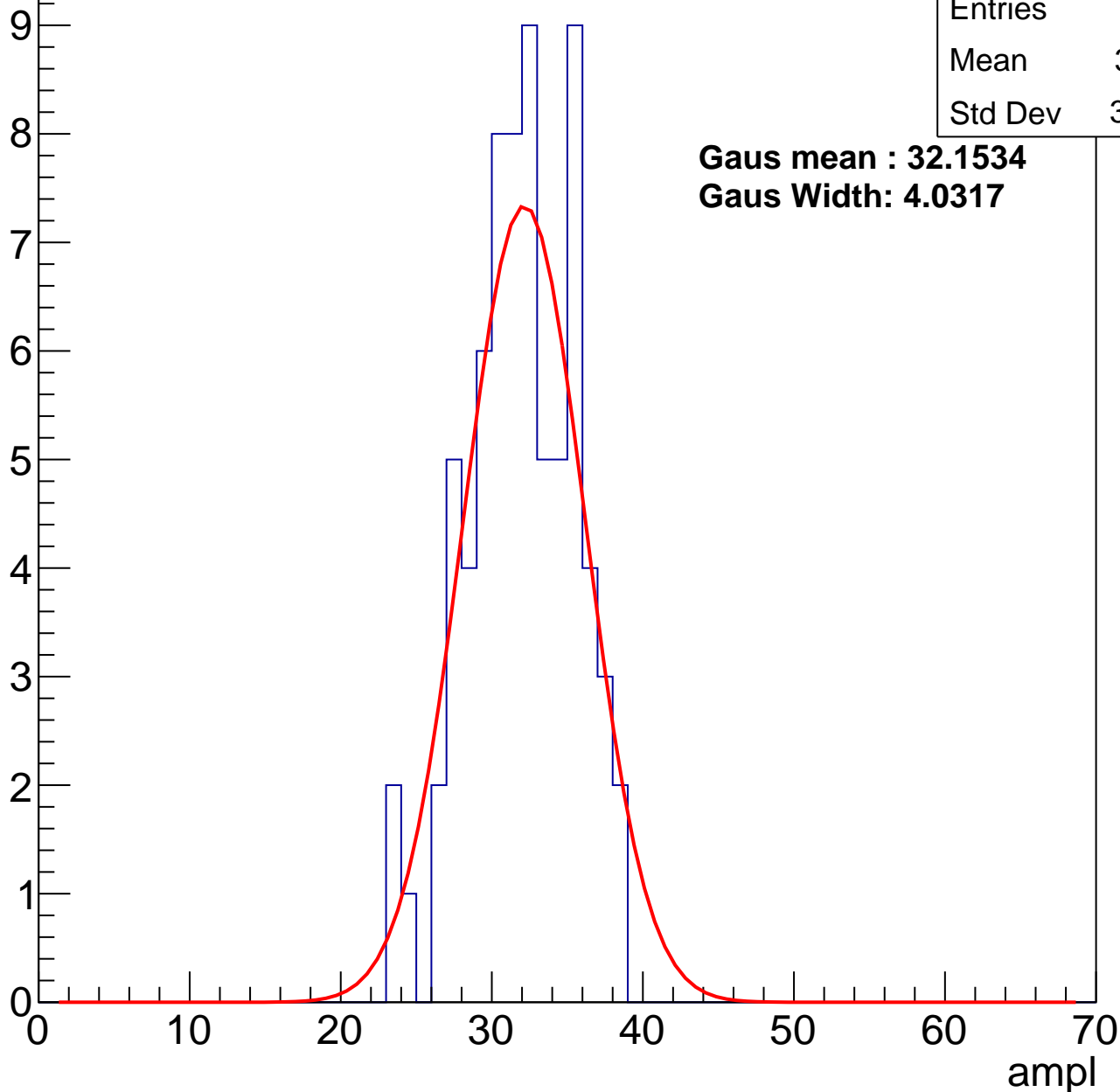
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	31.51
Std Dev	3.472

**Gaus mean : 32.1534**

**Gaus Width: 4.0317**



# B0L001S, U10-ch59, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	67
Mean	38.16
Std Dev	3.335

**Gaus mean : 39.4544**

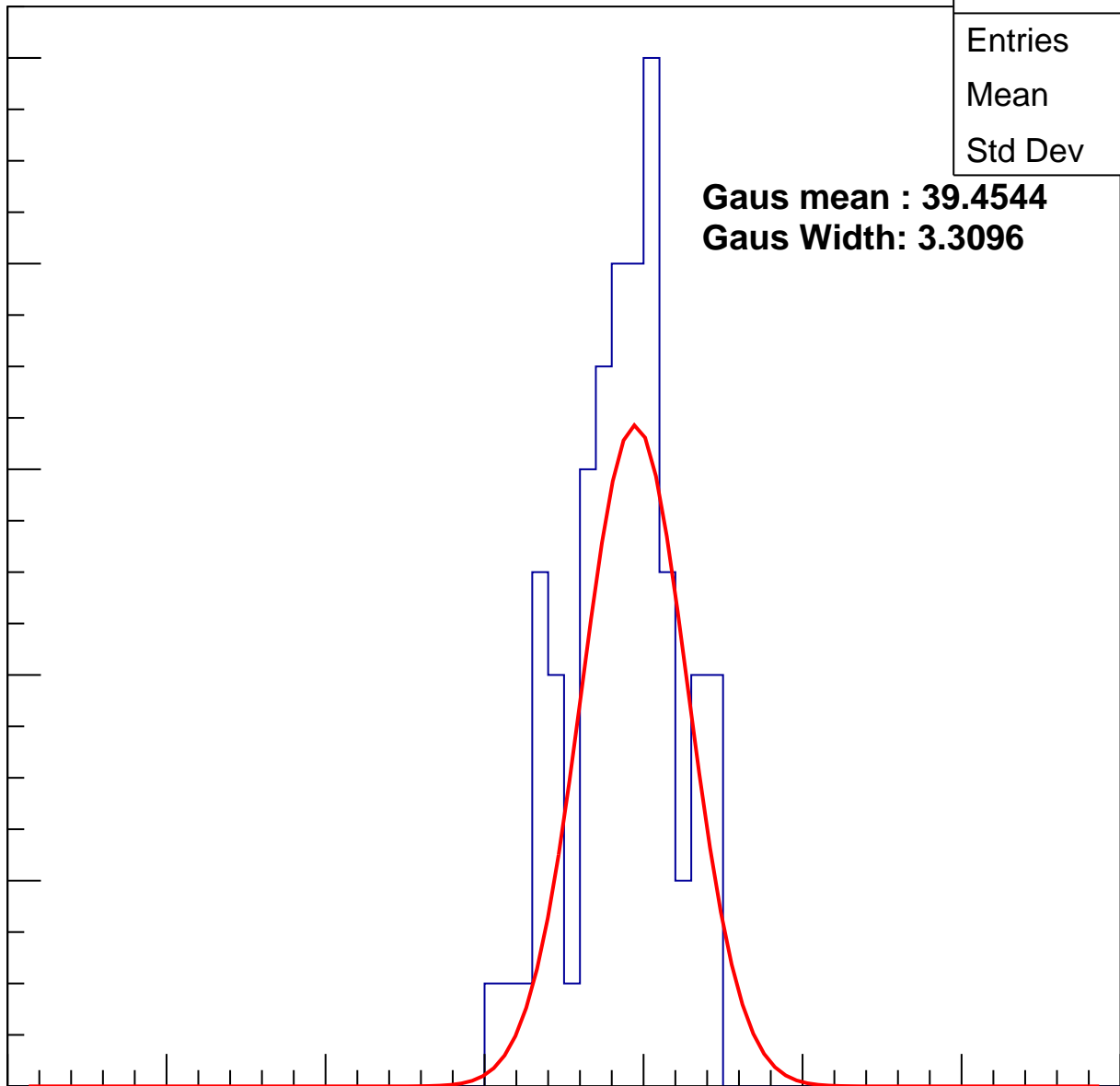
**Gaus Width: 3.3096**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U10-ch59, adc2

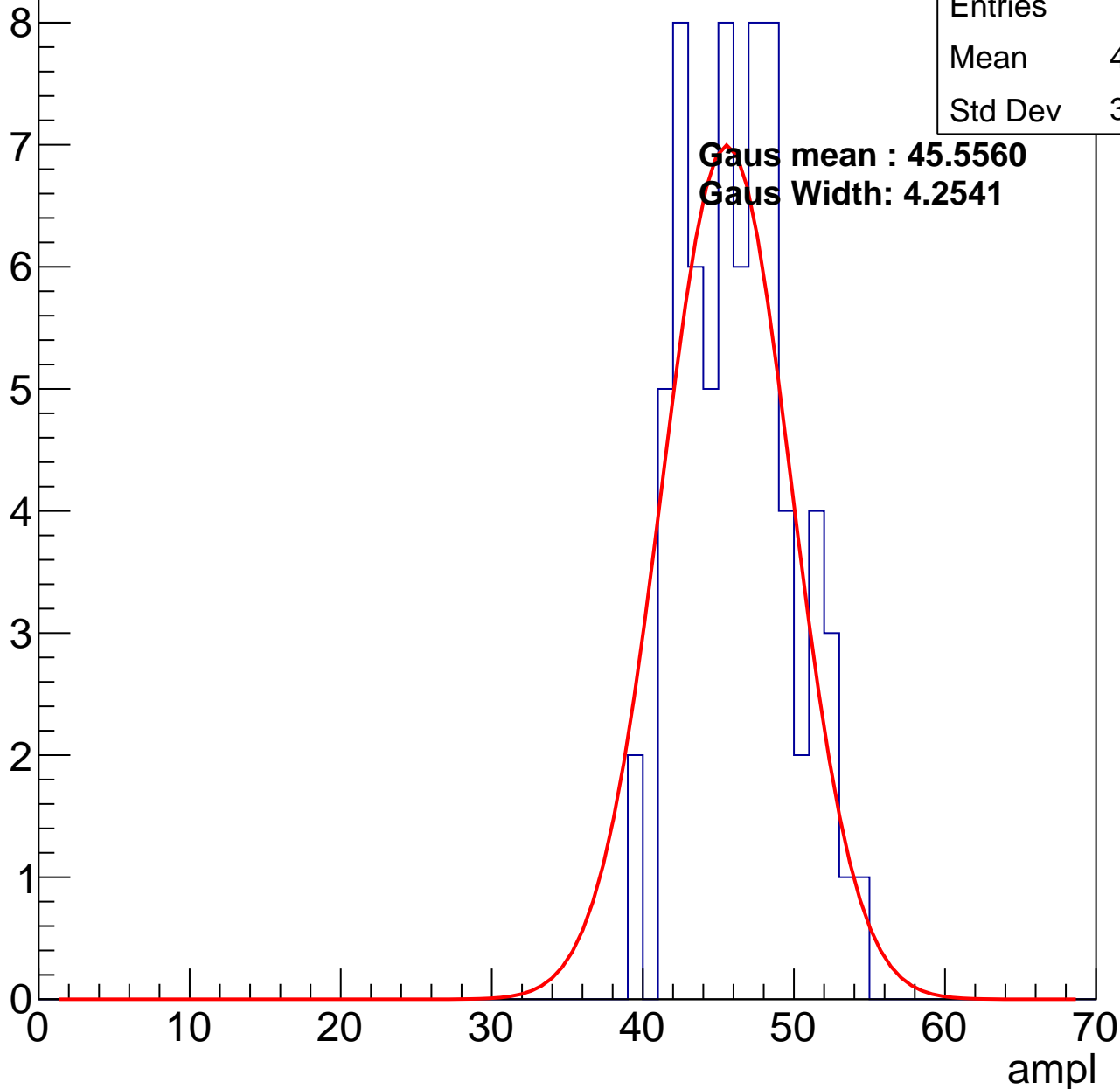
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	45.86
Std Dev	3.482

Gaus mean : 45.5560

Gaus Width: 4.2541

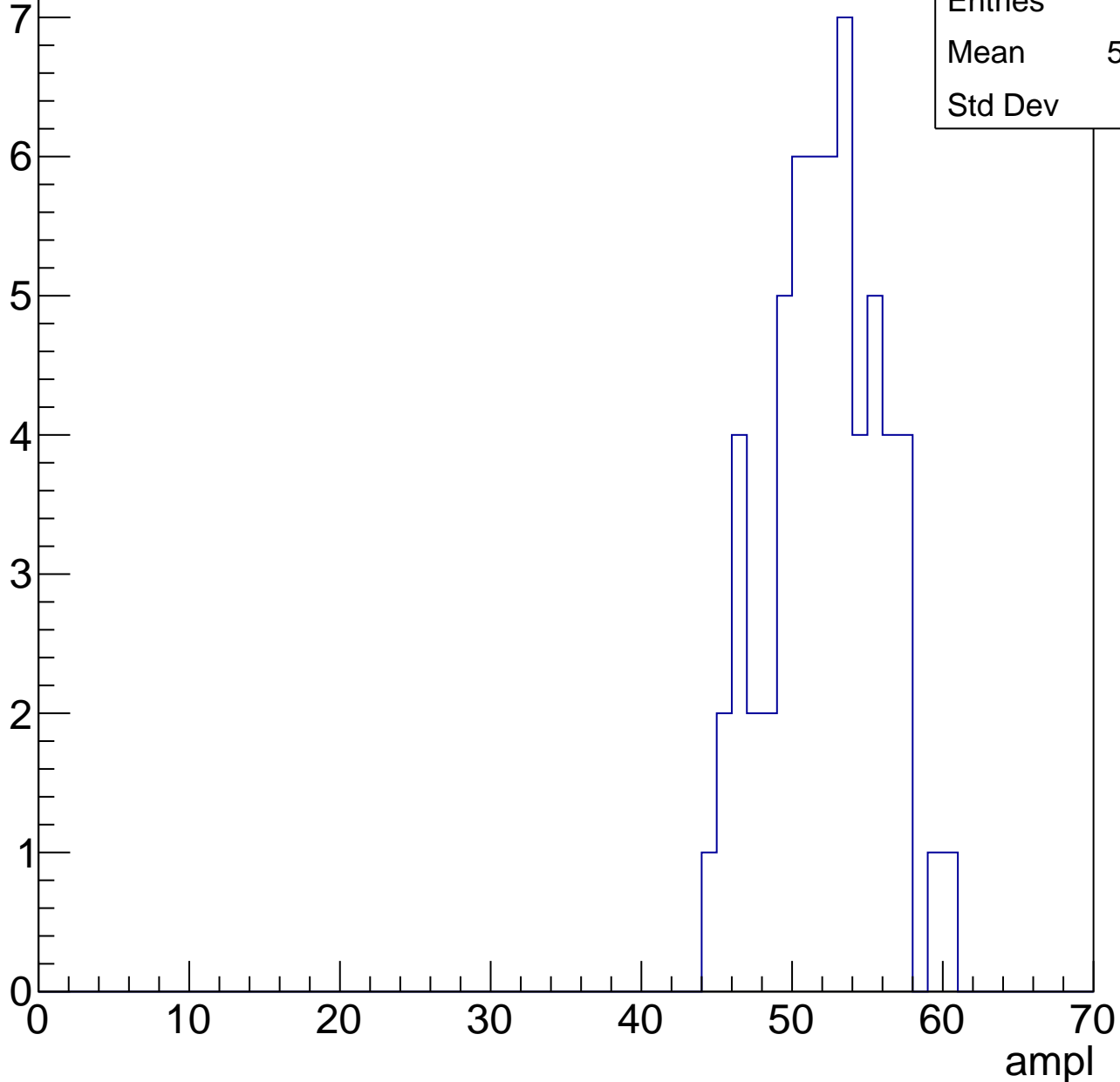


# B0L001S, U10-ch59, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	51.73
Std Dev	3.66



# B0L001S, U10-ch59, adc4

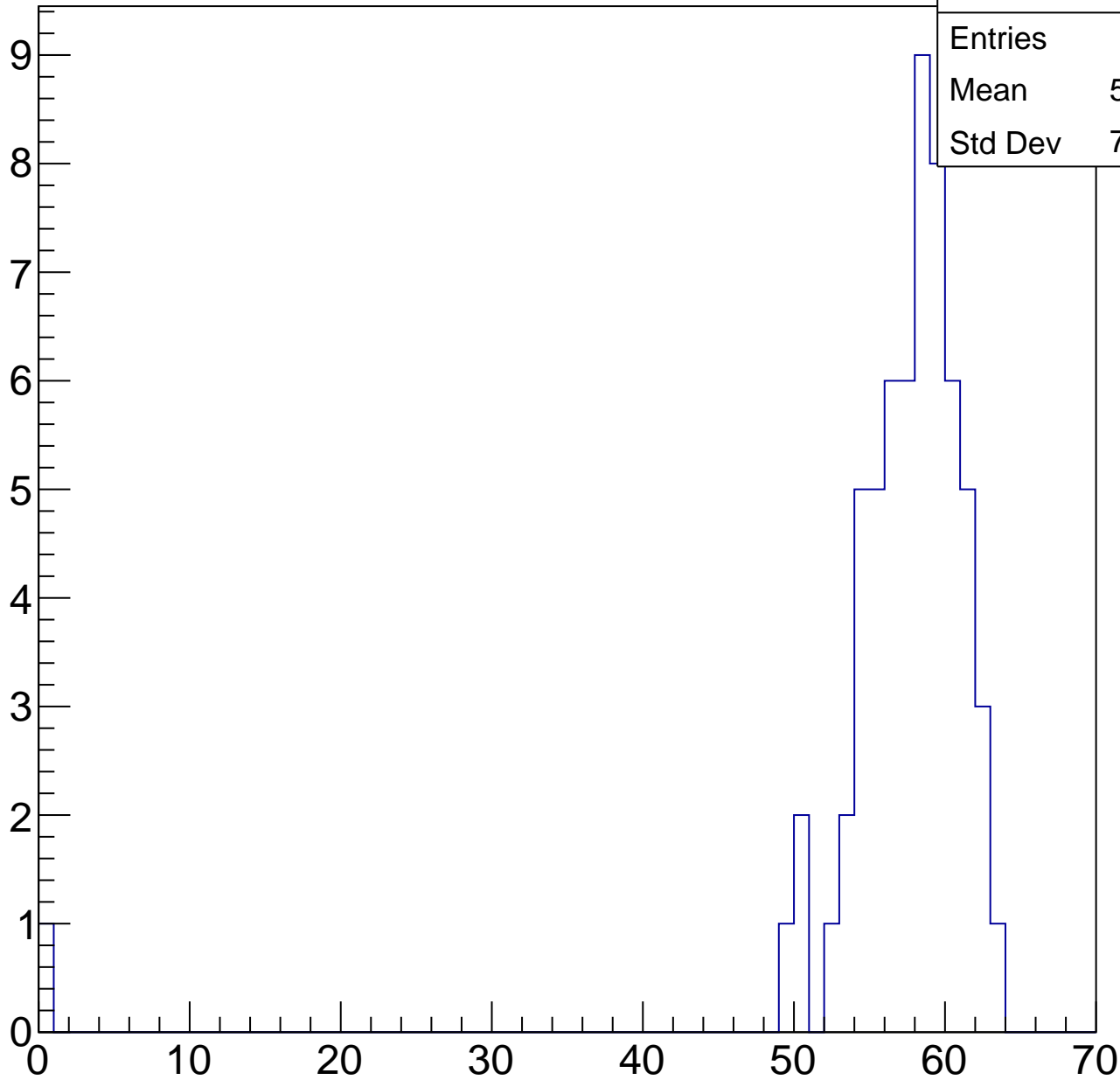
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	61
Mean	56.36
Std Dev	7.893

ampl

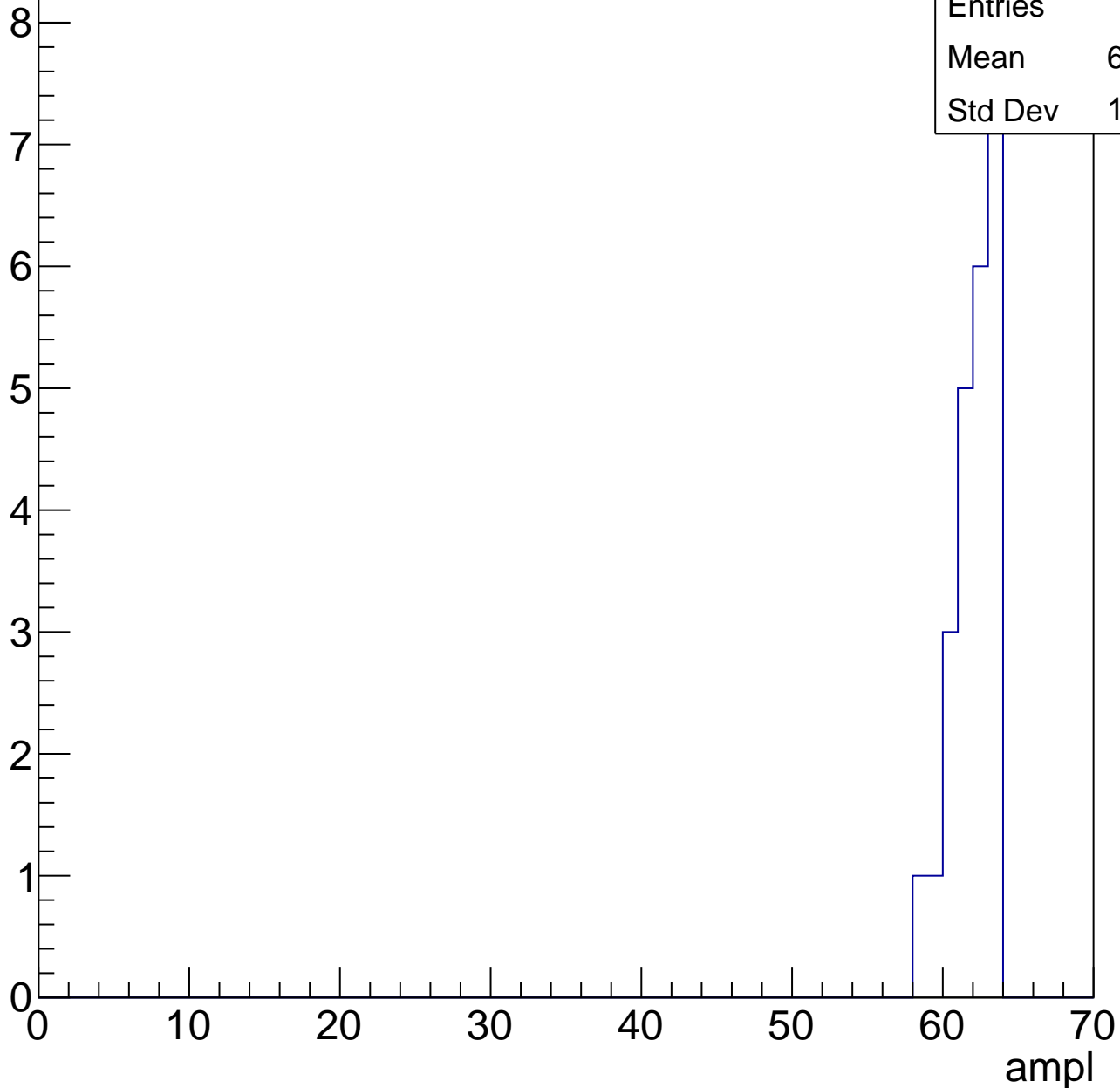


# B0L001S, U10-ch59, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	24
Mean	61.58
Std Dev	1.382



# B0L001S, U10-ch59, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch59, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U10-ch60, adc0

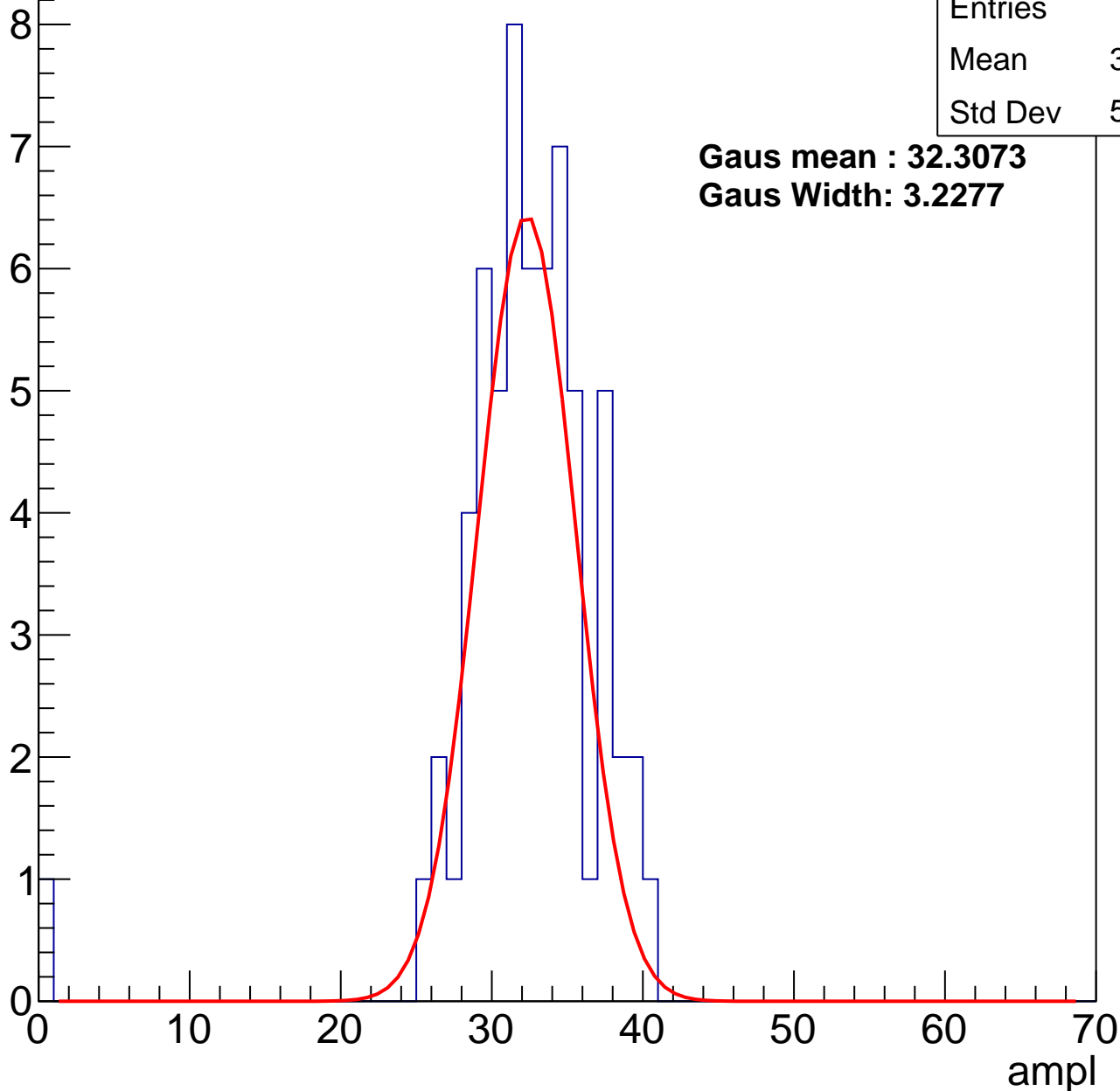
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	31.84
Std Dev	5.298

**Gaus mean : 32.3073**

**Gaus Width: 3.2277**



# B0L001S, U10-ch60, adc1

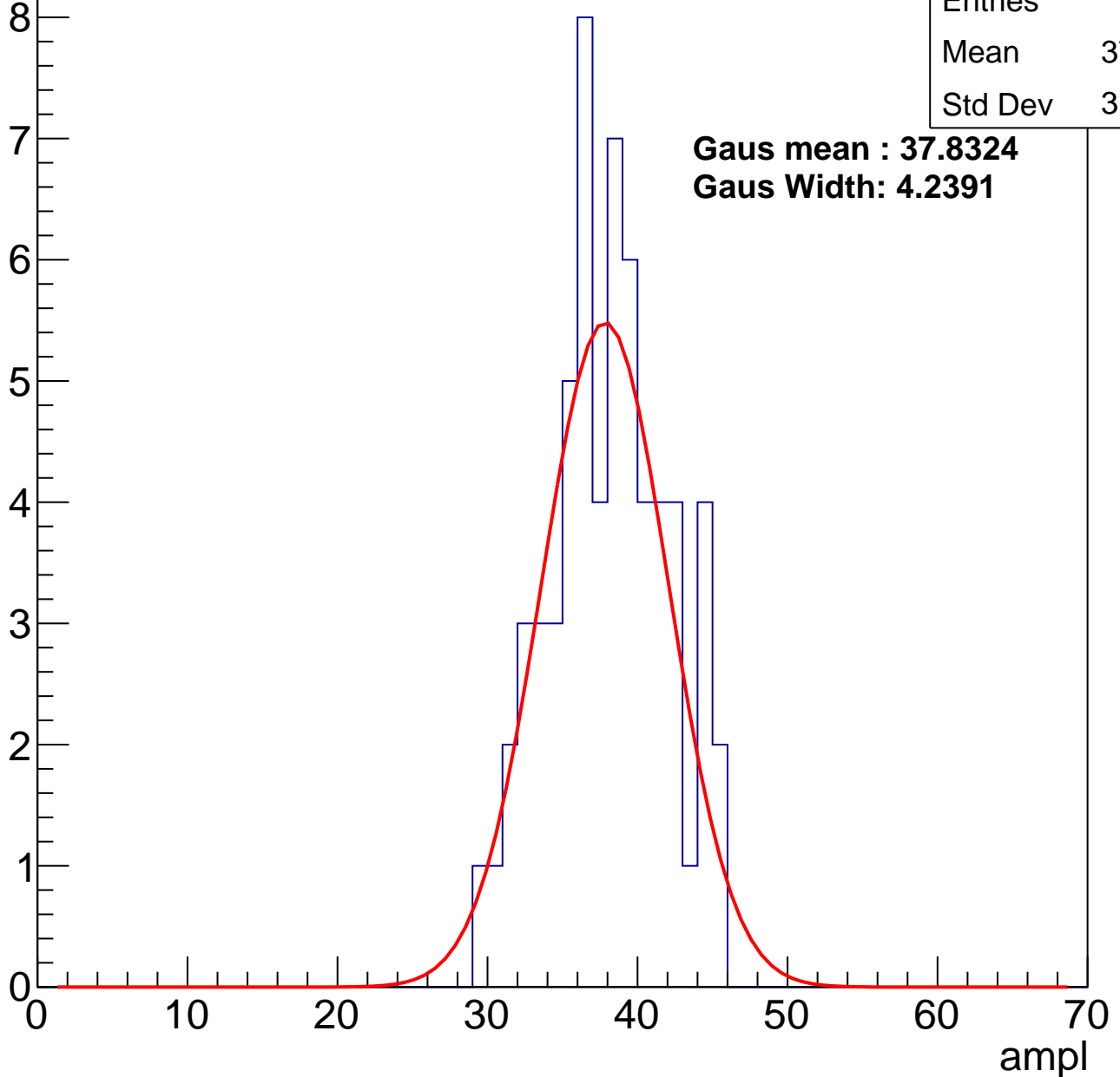
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	37.58
Std Dev	3.879

**Gaus mean : 37.8324**

**Gaus Width: 4.2391**



# B0L001S, U10-ch60, adc2

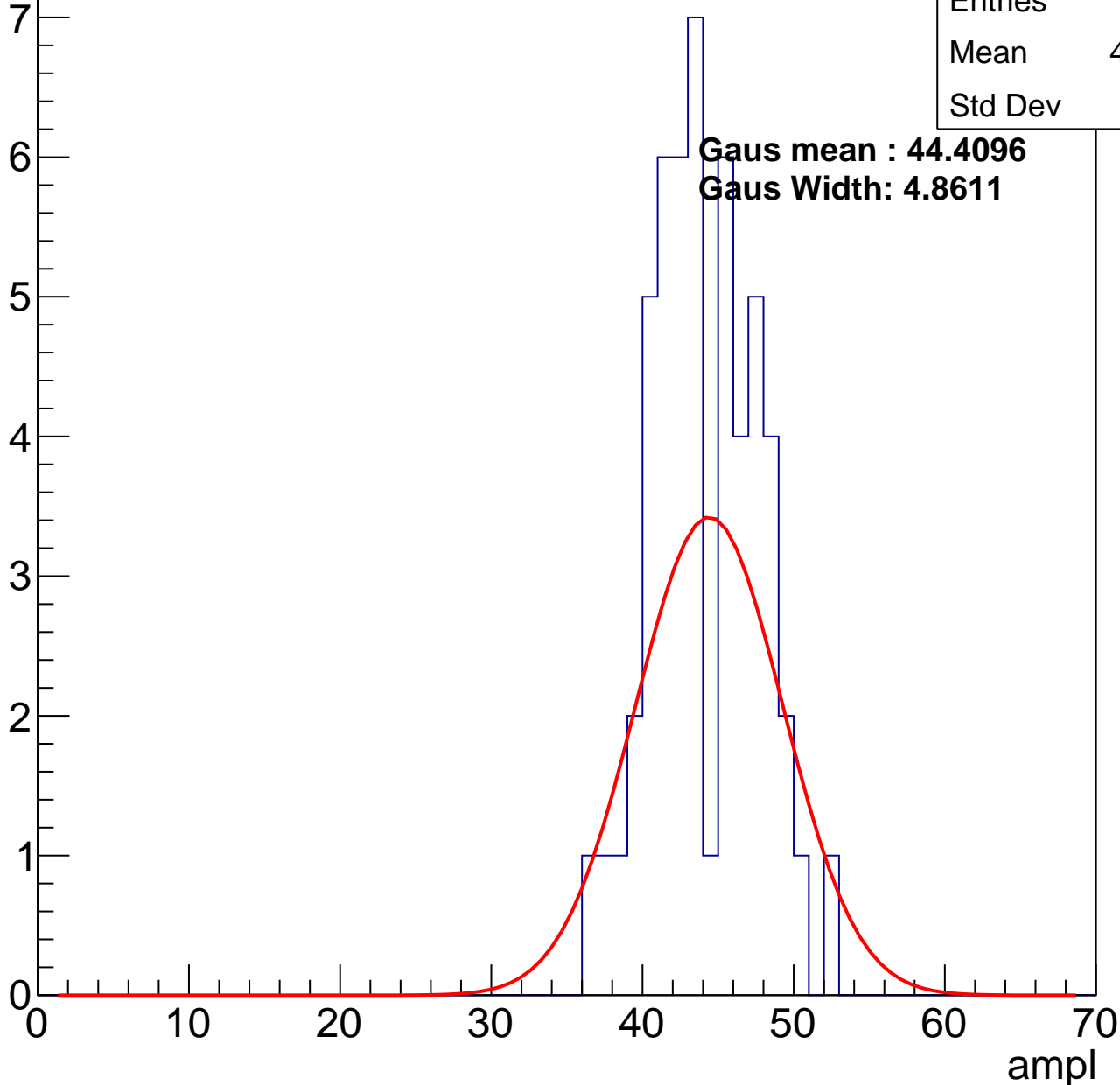
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	43.64
Std Dev	3.47

**Gaus mean : 44.4096**

**Gaus Width: 4.8611**

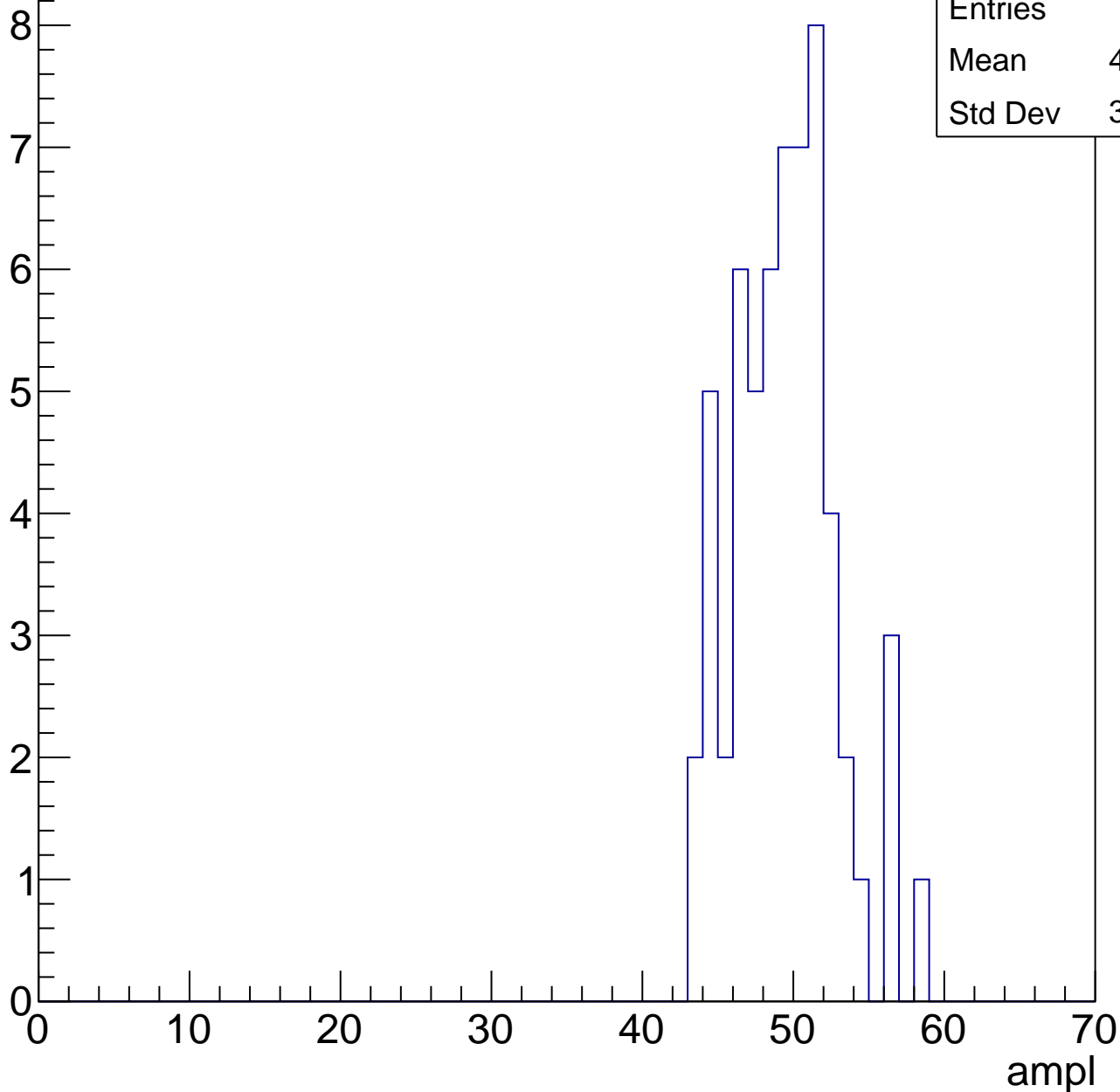


# B0L001S, U10-ch60, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	48.98
Std Dev	3.367



# B0L001S, U10-ch60, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

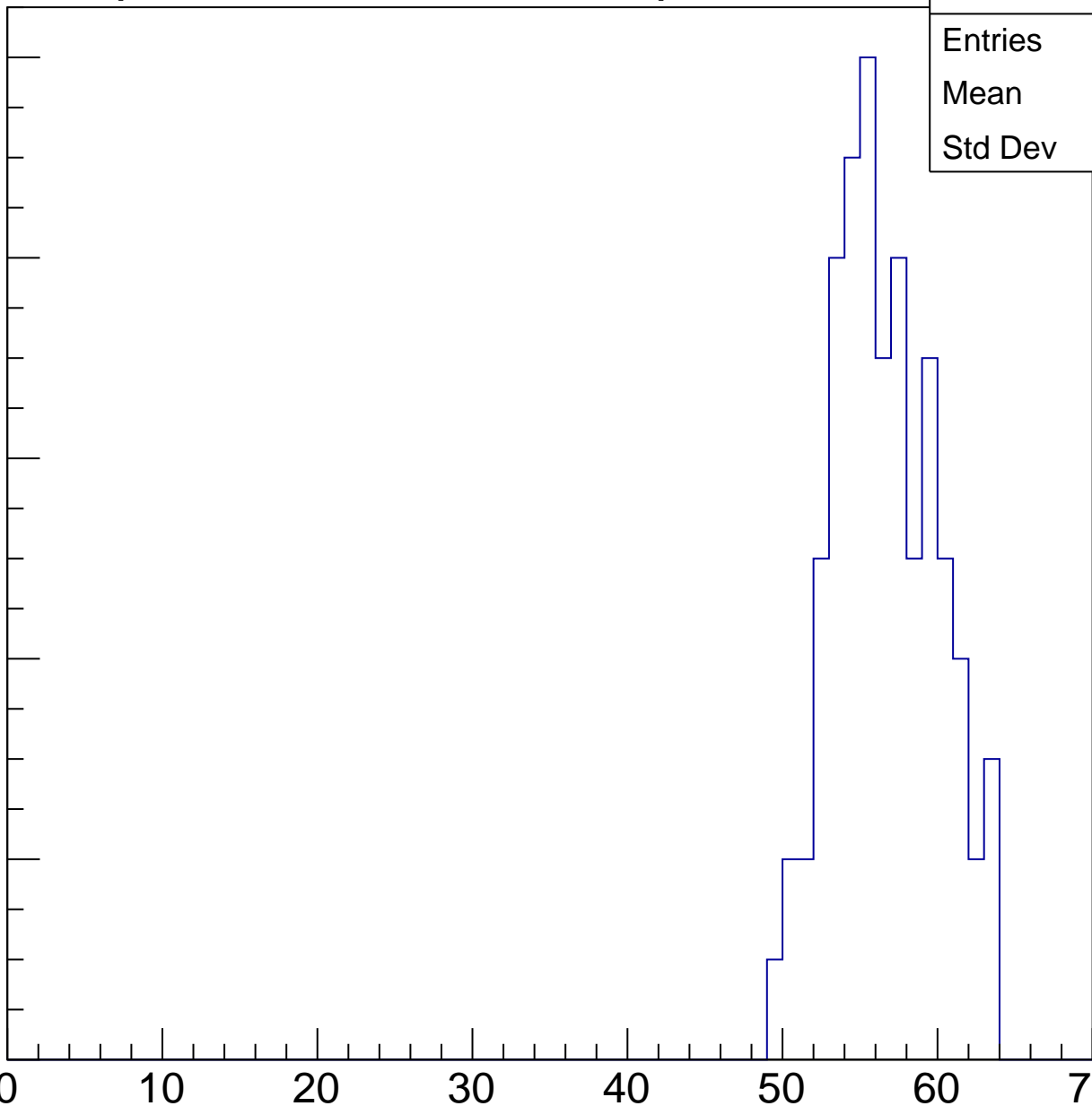
Entries	78
Mean	56.14
Std Dev	3.316

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

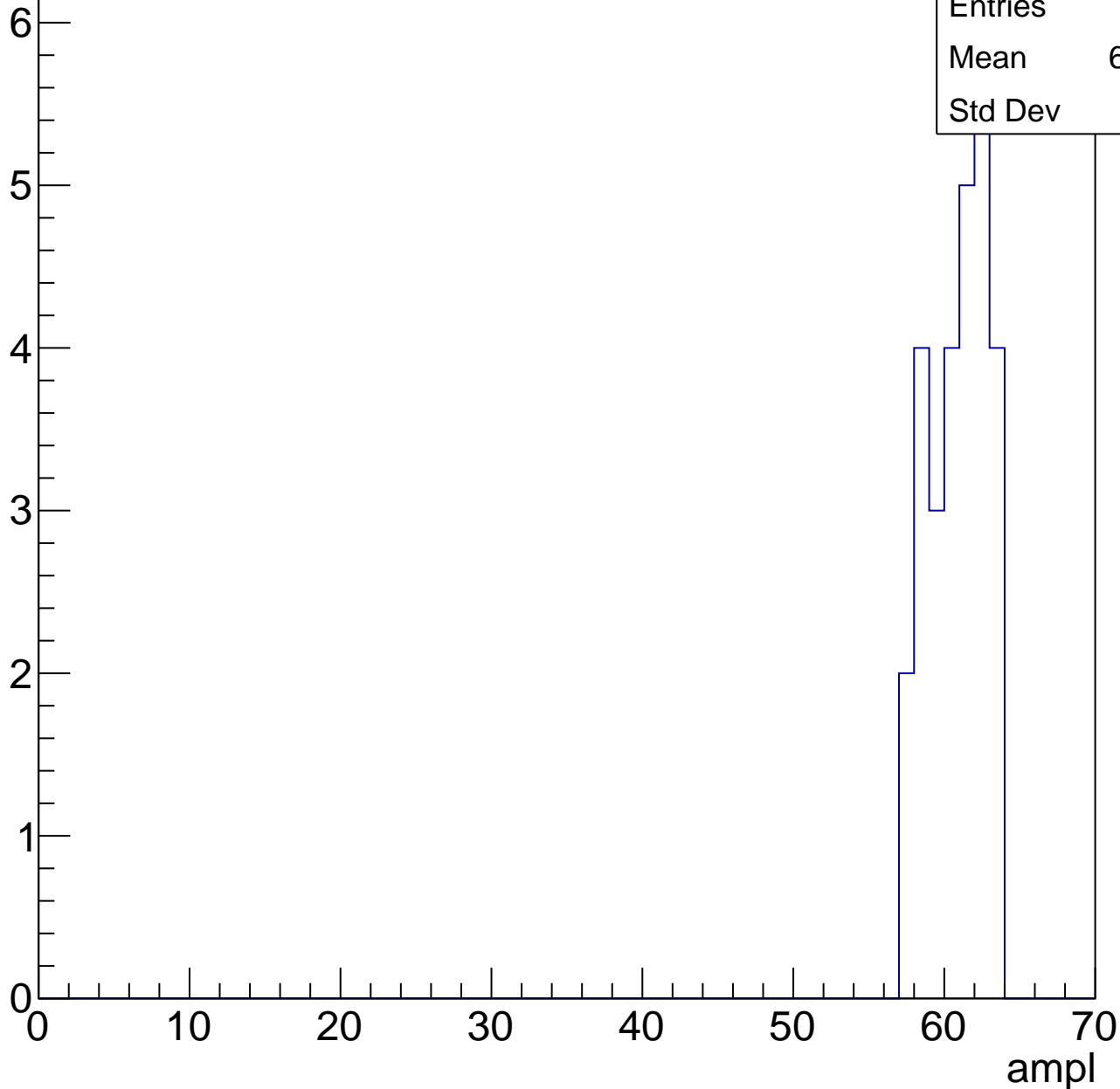


# B0L001S, U10-ch60, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

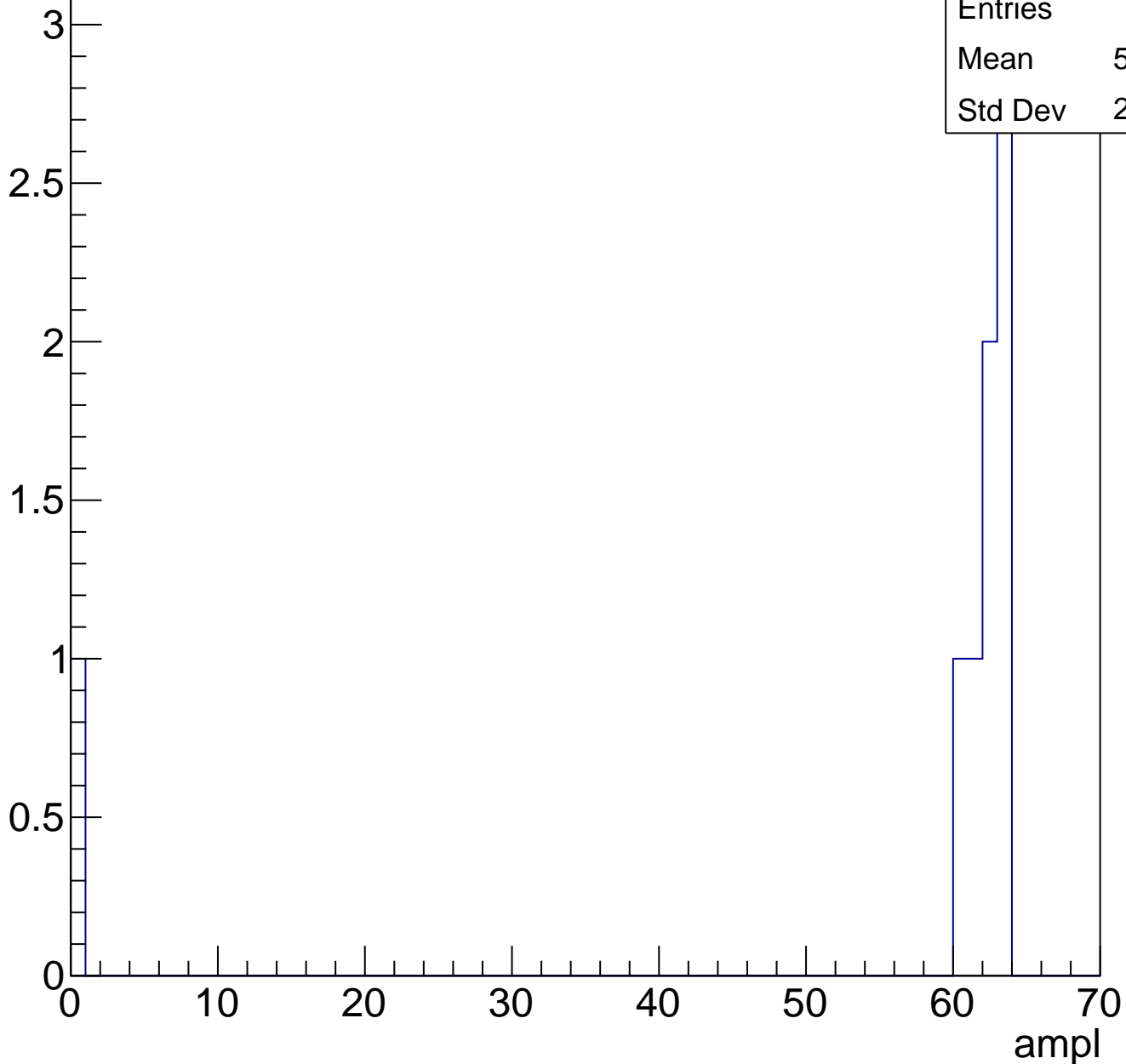
Entries	28
Mean	60.43
Std Dev	1.86



# B0L001S, U10-ch60, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch60, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U10-ch61, adc0

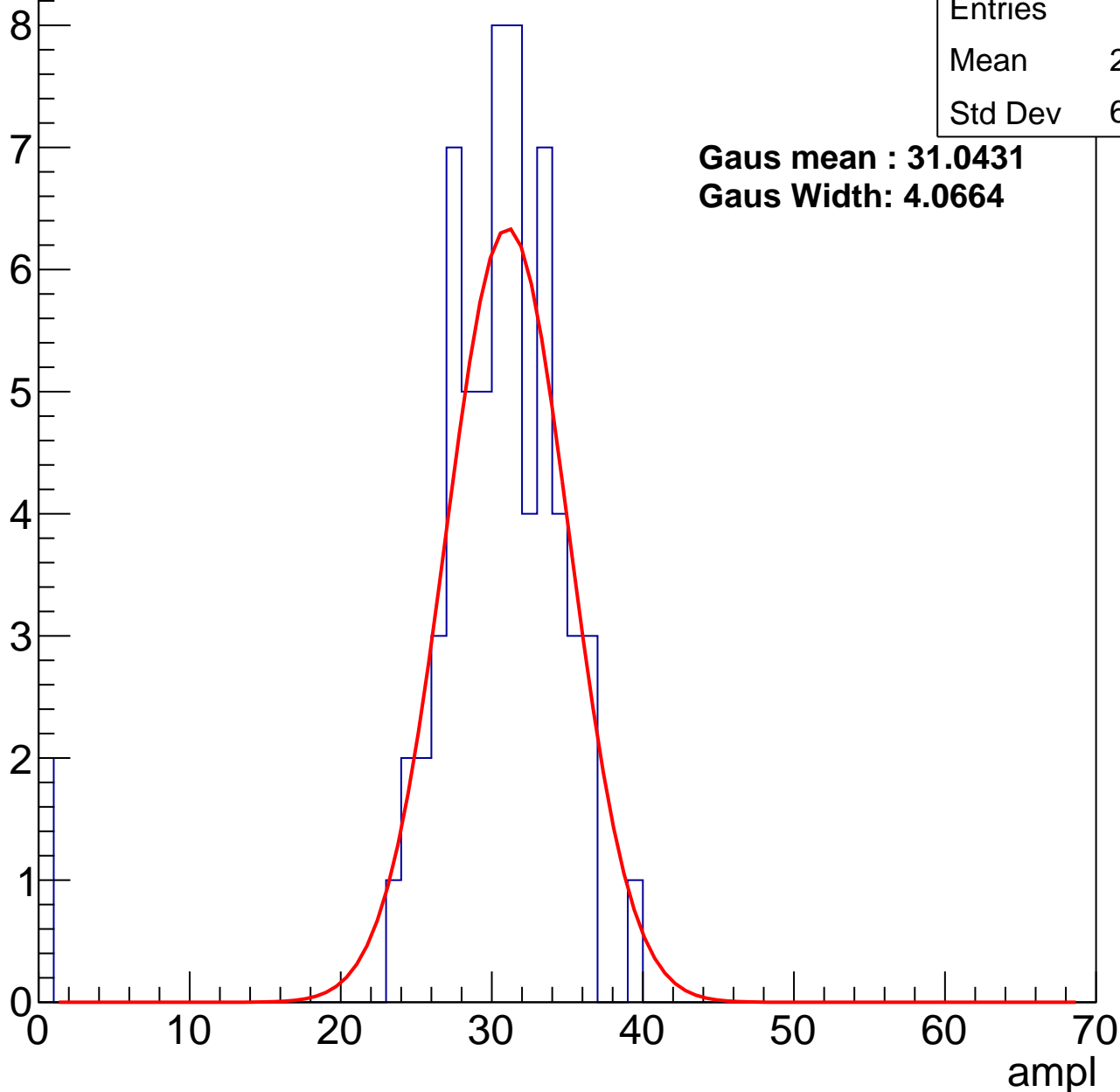
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	29.35
Std Dev	6.195

**Gaus mean : 31.0431**

**Gaus Width: 4.0664**



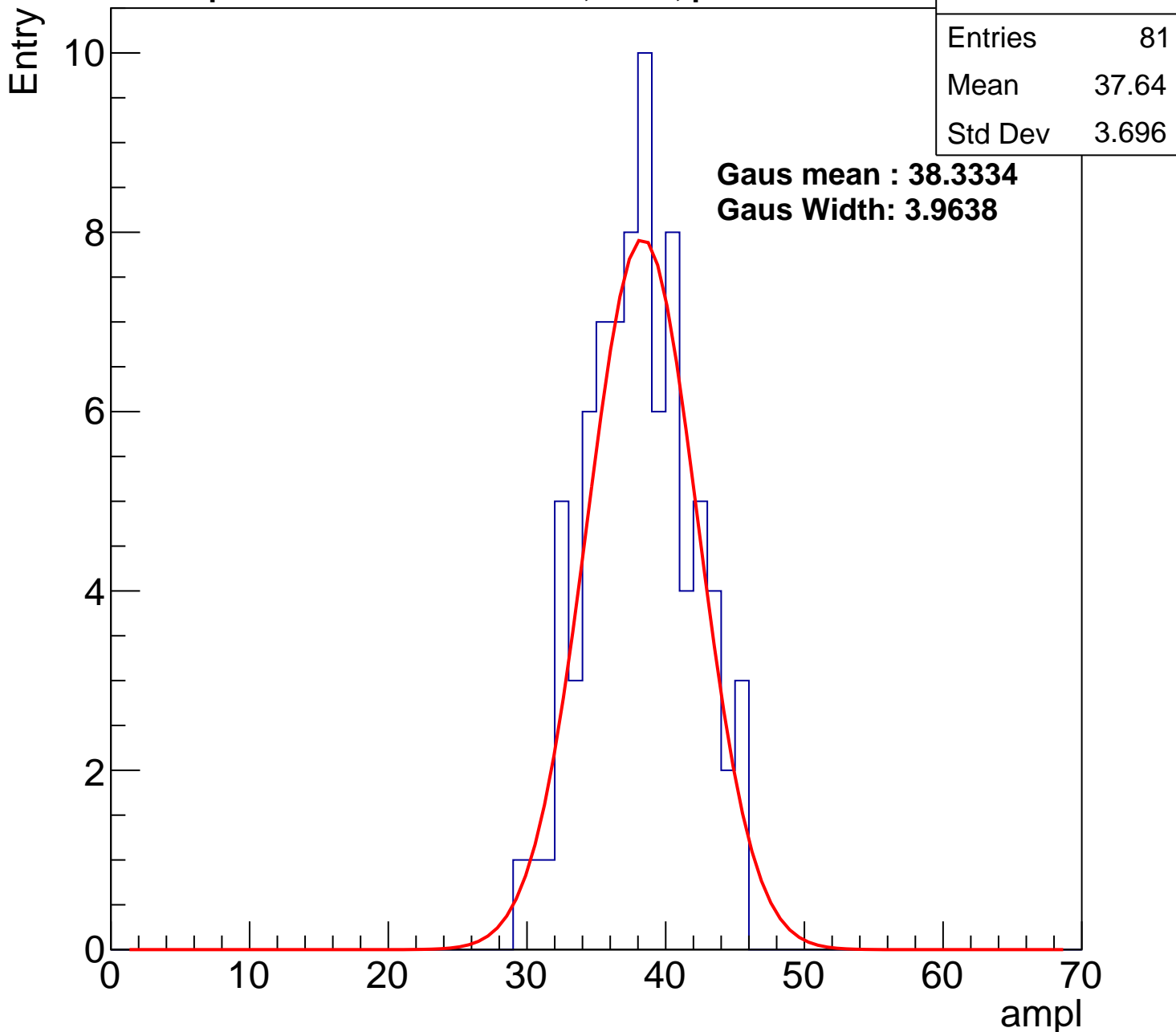
# B0L001S, U10-ch61, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	81
Mean	37.64
Std Dev	3.696

**Gaus mean : 38.3334**

**Gaus Width: 3.9638**



# B0L001S, U10-ch61, adc2

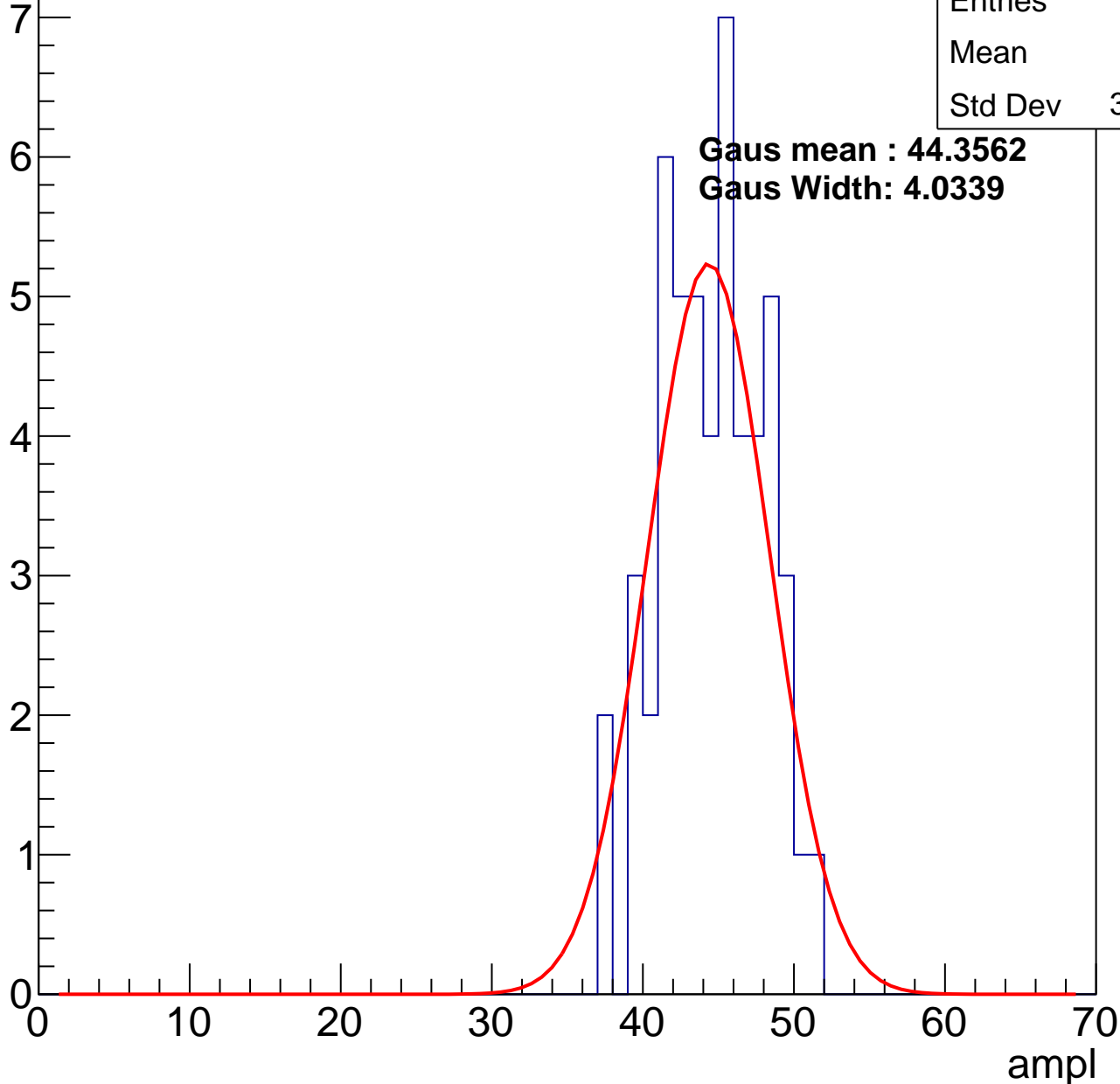
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	44.1
Std Dev	3.347

**Gaus mean : 44.3562**

**Gaus Width: 4.0339**

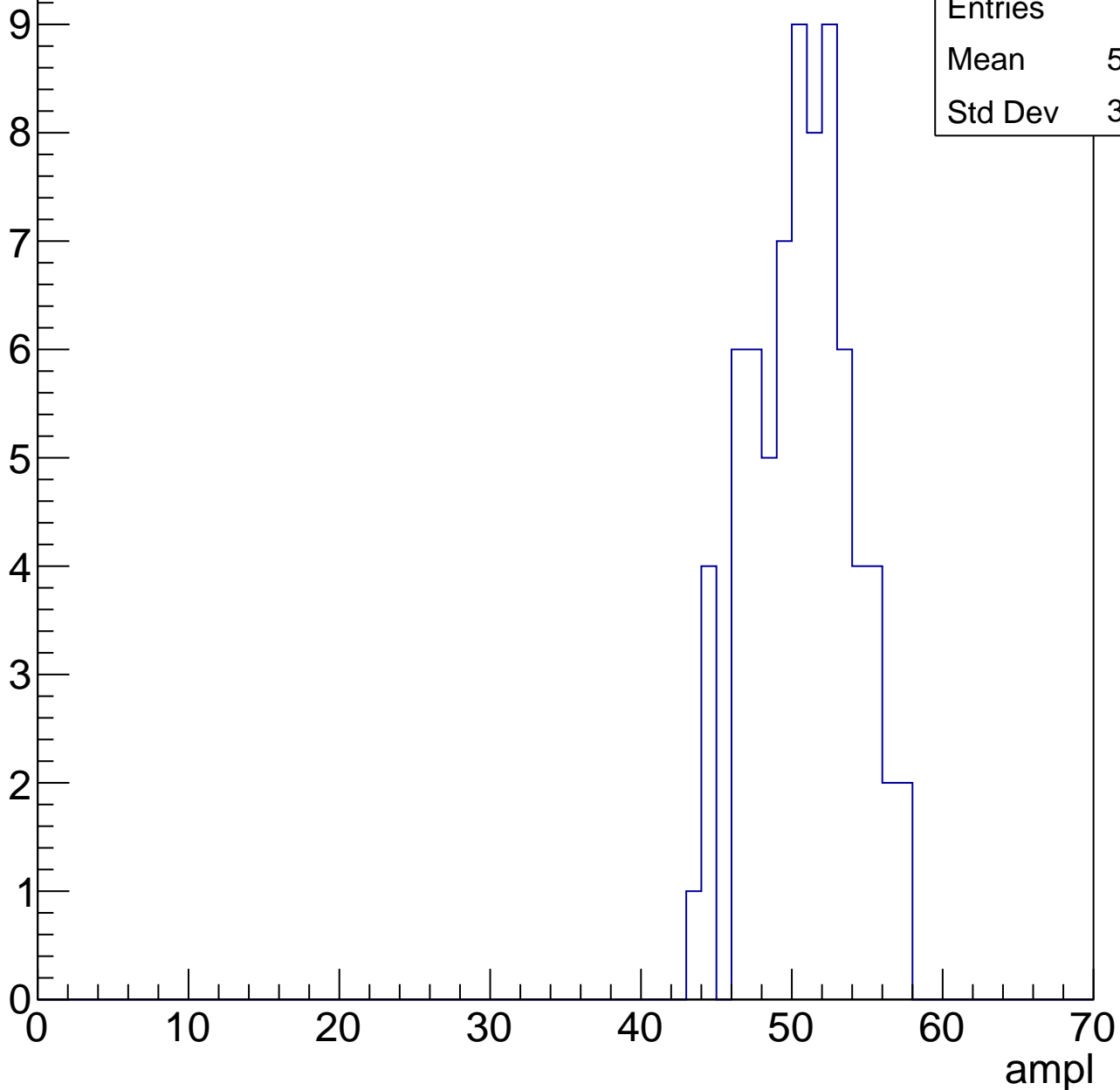


# B0L001S, U10-ch61, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	50.22
Std Dev	3.307

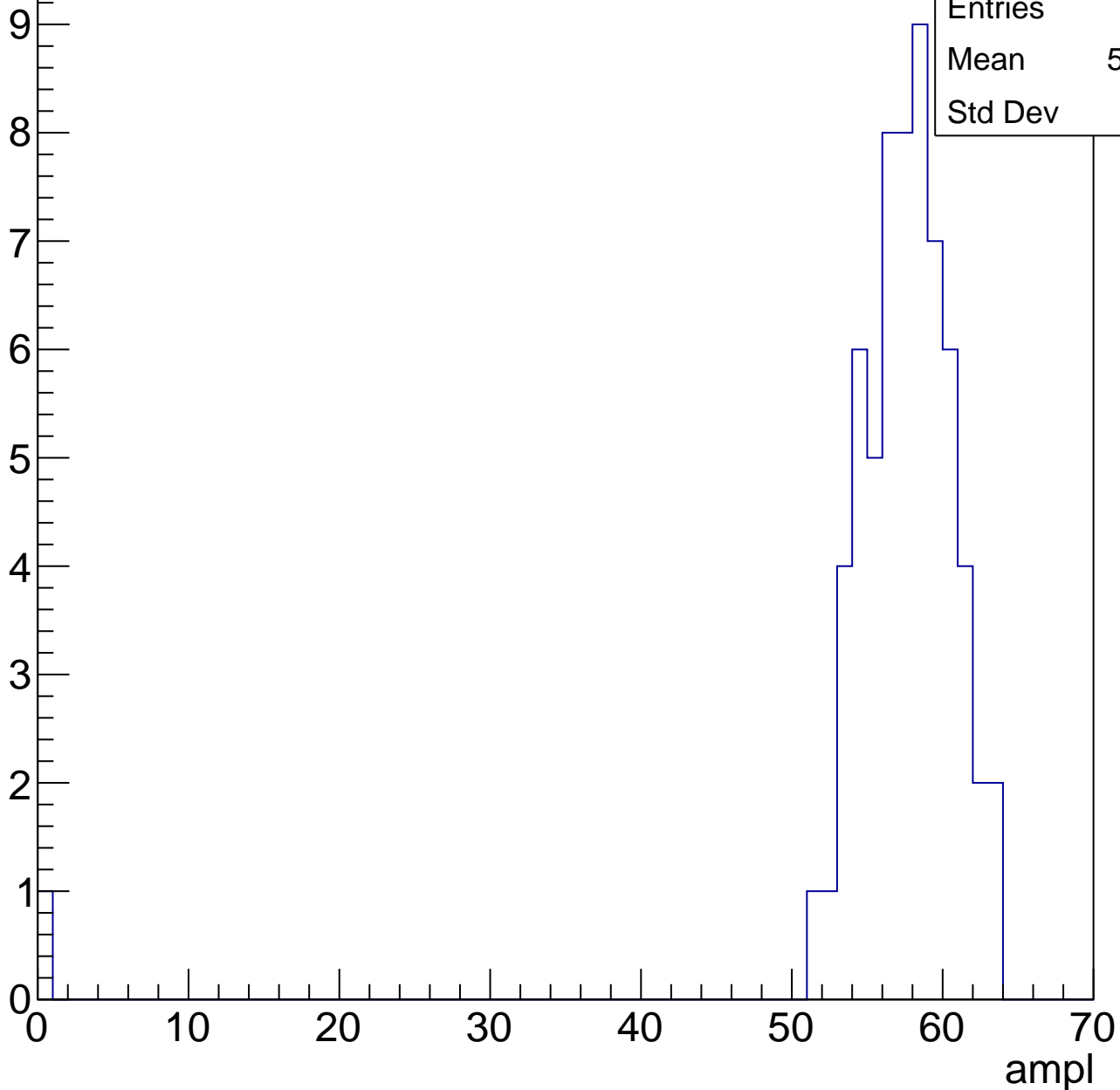


# B0L001S, U10-ch61, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	56.36
Std Dev	7.61

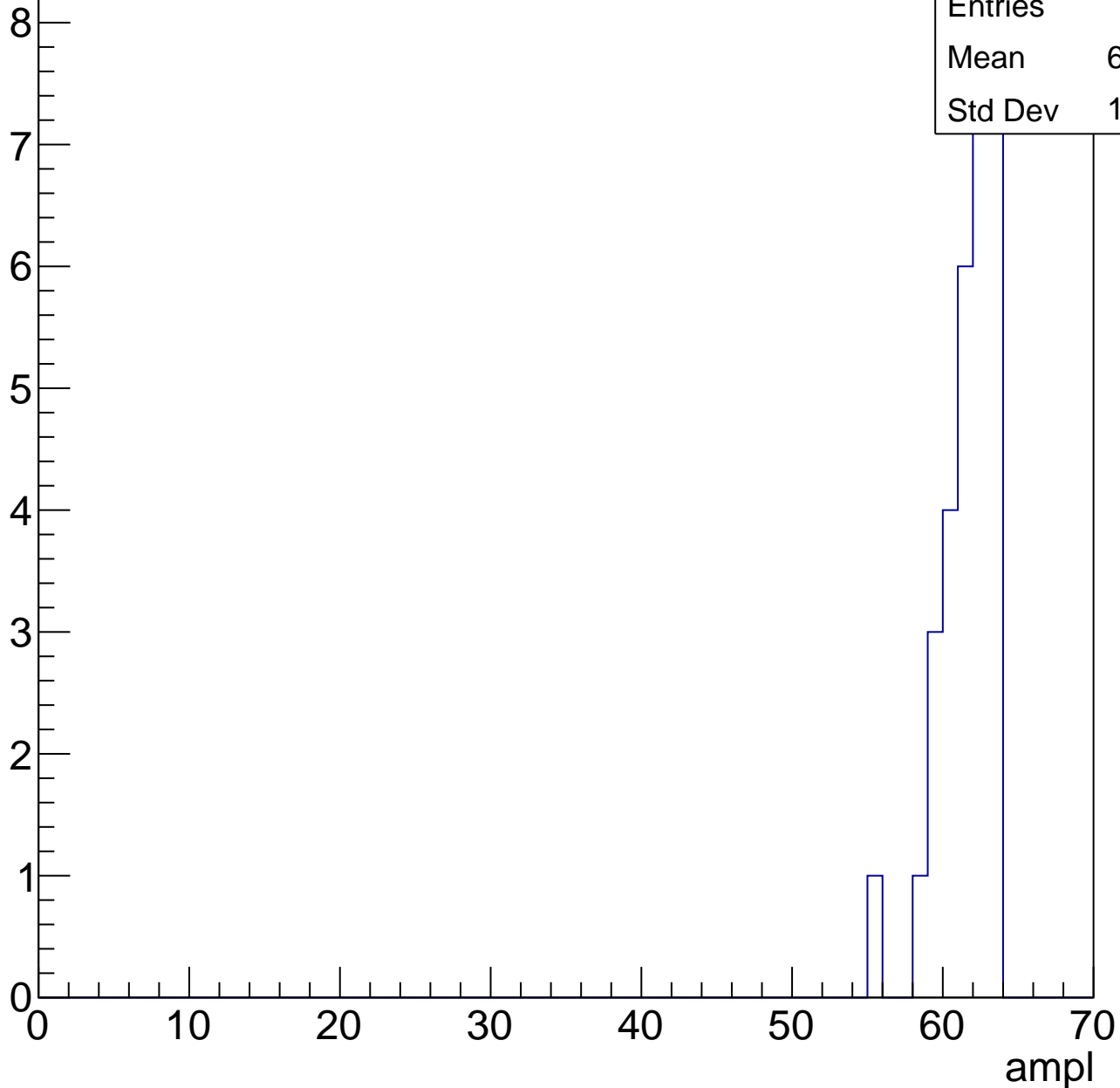


# B0L001S, U10-ch61, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	31
Mean	61.16
Std Dev	1.798



# B0L001S, U10-ch61, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U10-ch61, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U10-ch62, adc0

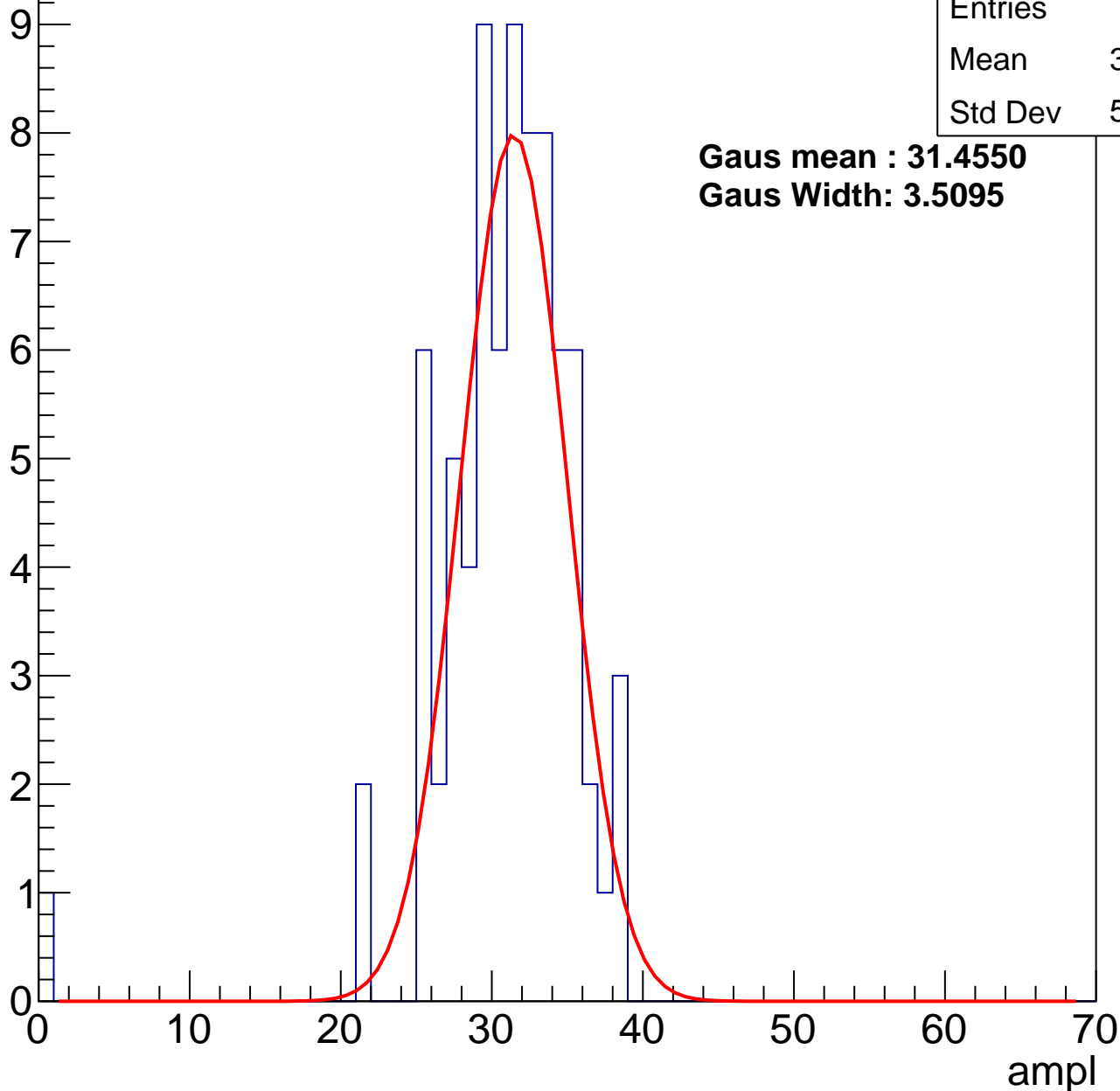
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	78
Mean	30.36
Std Dev	5.033

**Gaus mean : 31.4550**

**Gaus Width: 3.5095**



# B0L001S, U10-ch62, adc1

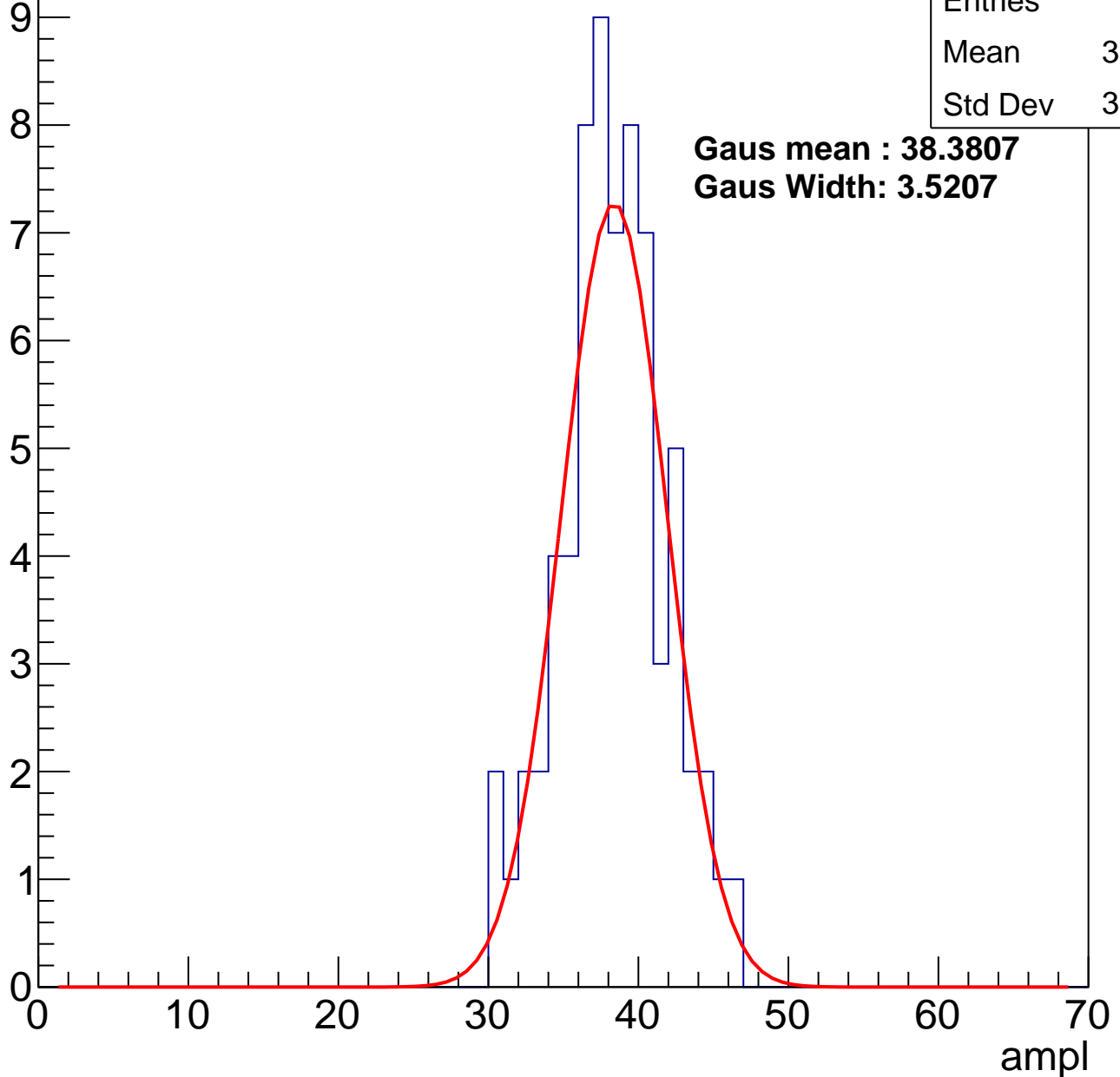
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	37.85
Std Dev	3.465

**Gaus mean : 38.3807**

**Gaus Width: 3.5207**



# B0L001S, U10-ch62, adc2

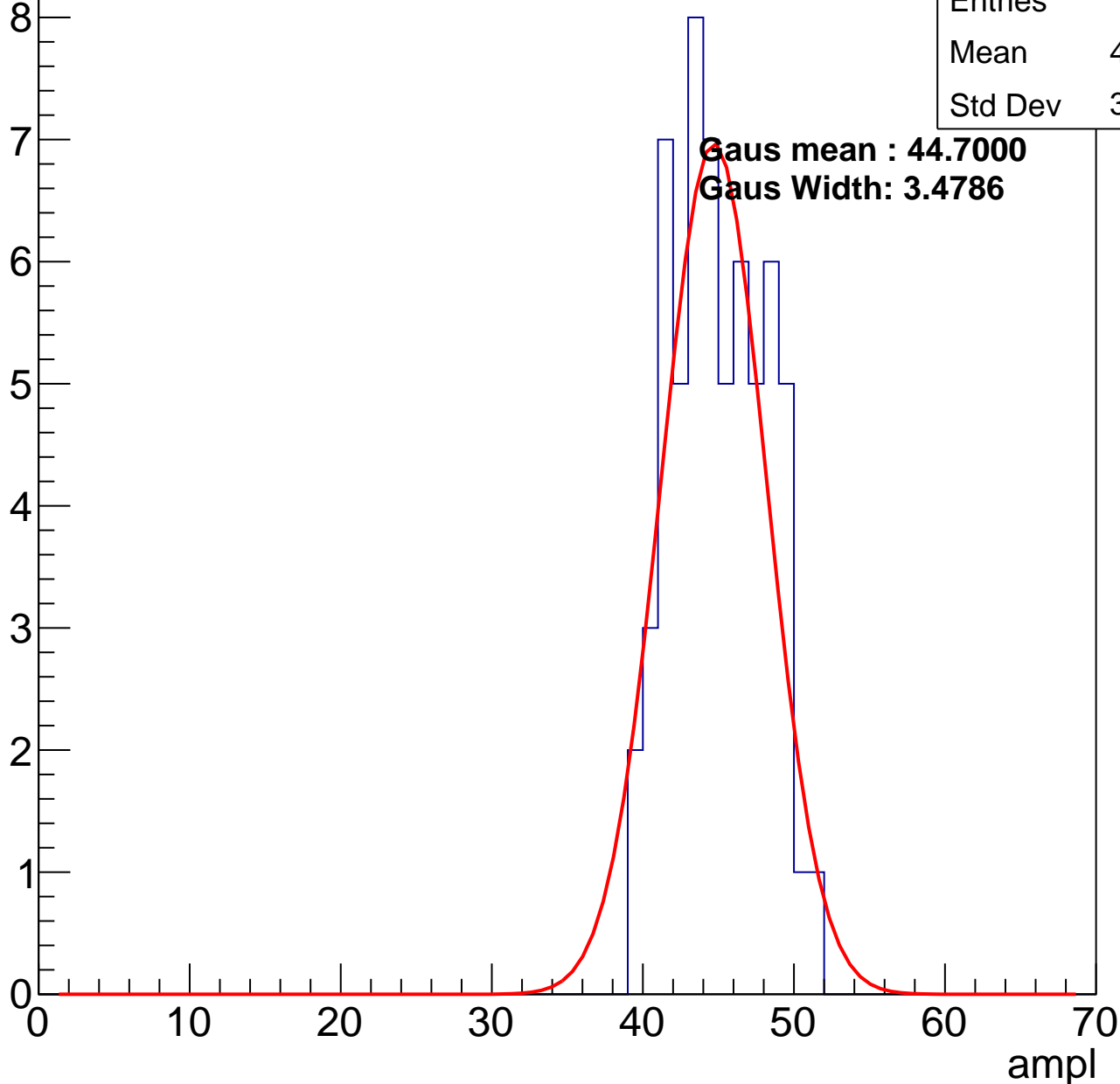
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	44.54
Std Dev	3.006

**Gaus mean : 44.7000**

**Gaus Width: 3.4786**

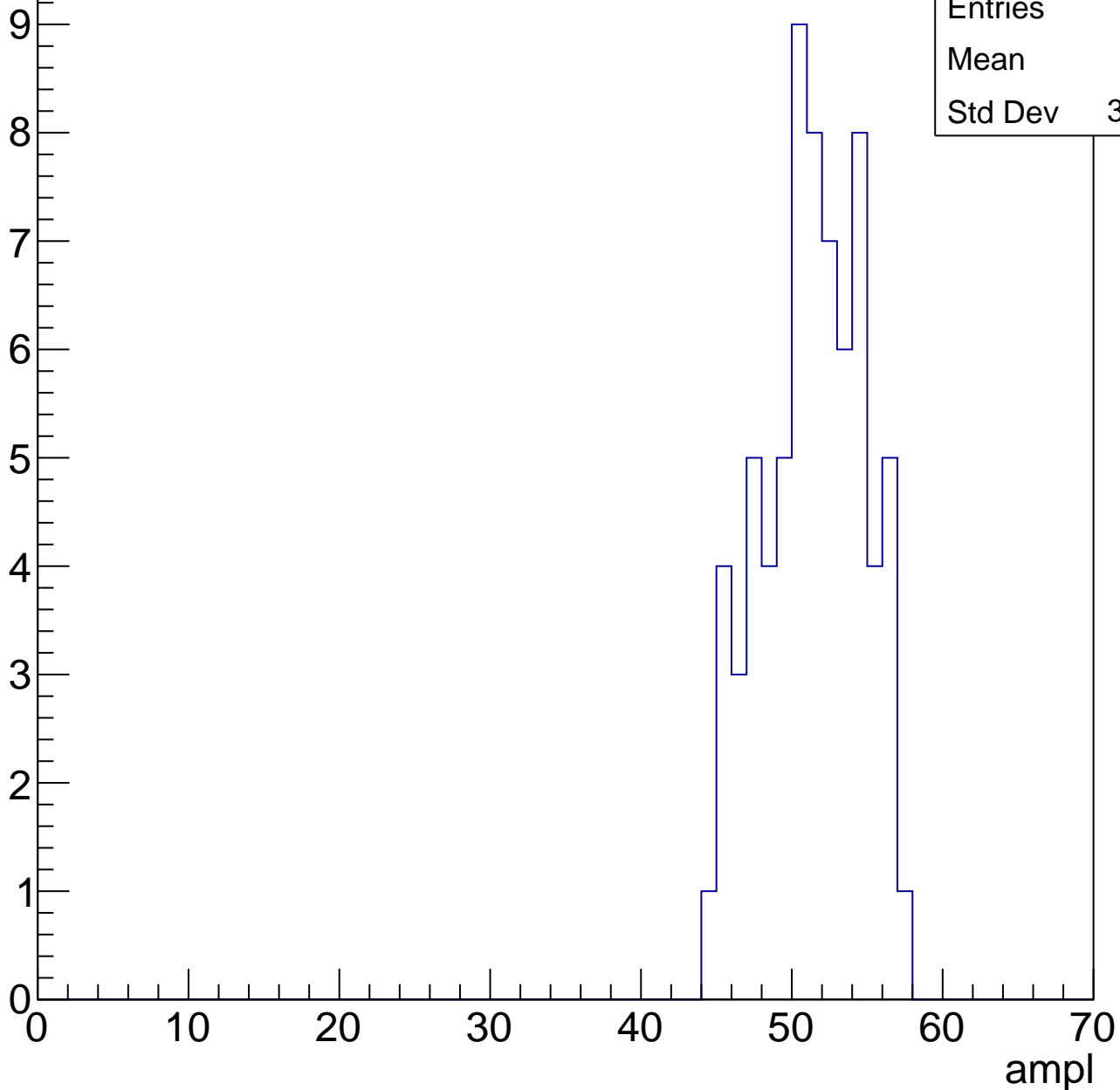


# B0L001S, U10-ch62, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	50.9
Std Dev	3.252

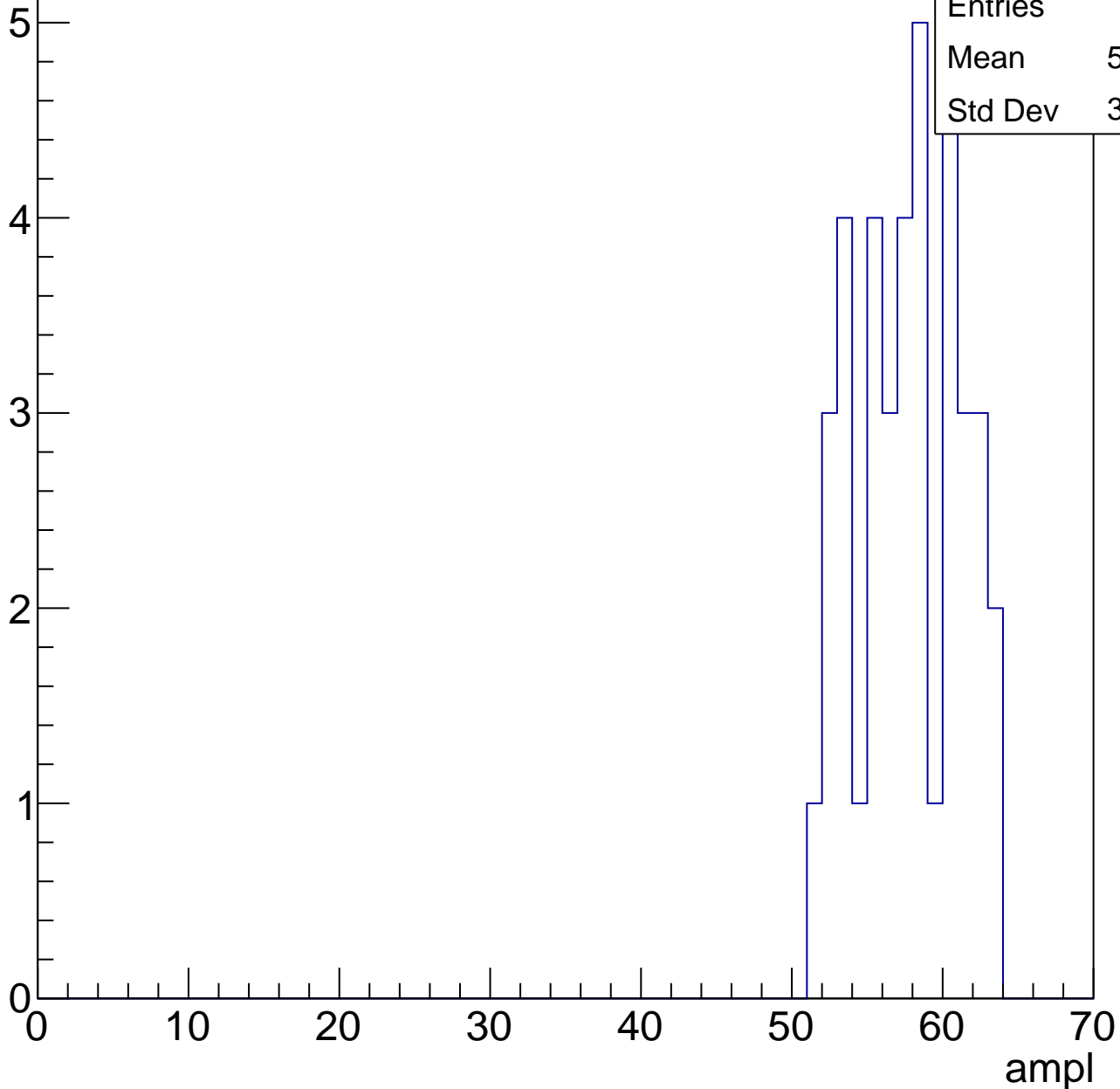


# B0L001S, U10-ch62, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

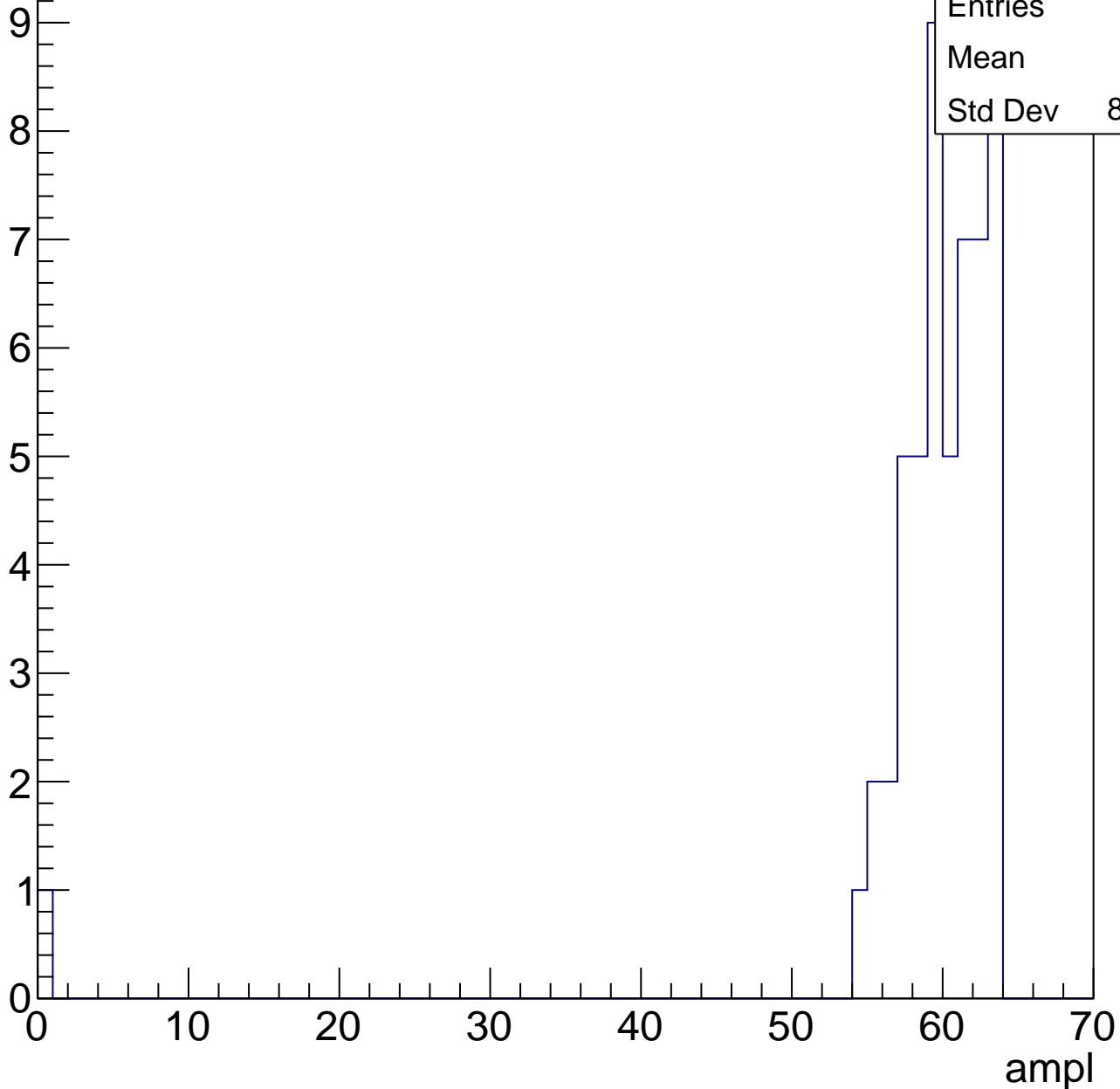
Entries	39
Mean	57.26
Std Dev	3.395



# B0L001S, U10-ch62, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U10-ch62, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U10-ch62, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U10-ch63, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	72
Mean	30.39
Std Dev	6.248

**Gaus mean : 32.1279**

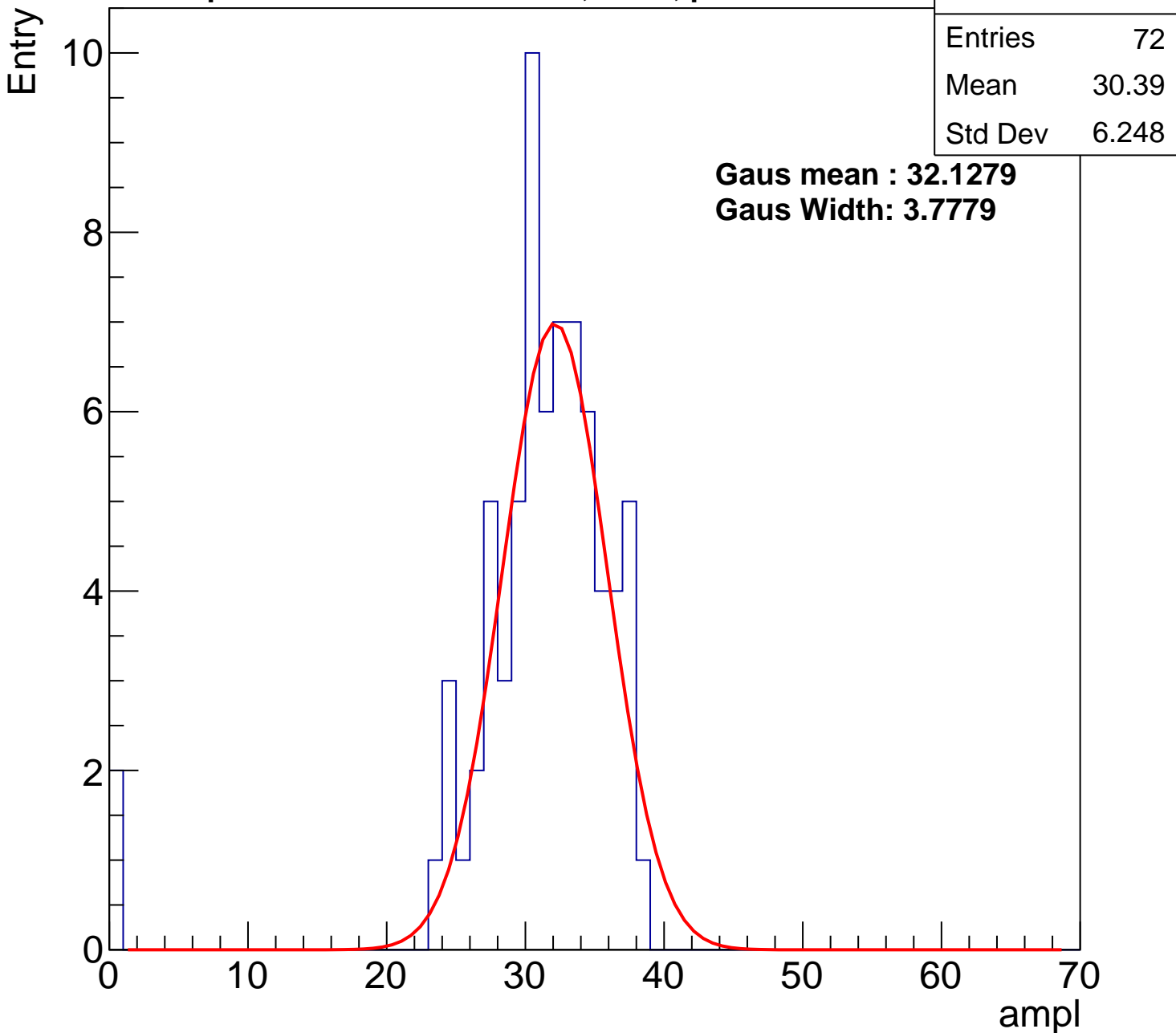
**Gaus Width: 3.7779**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U10-ch63, adc1

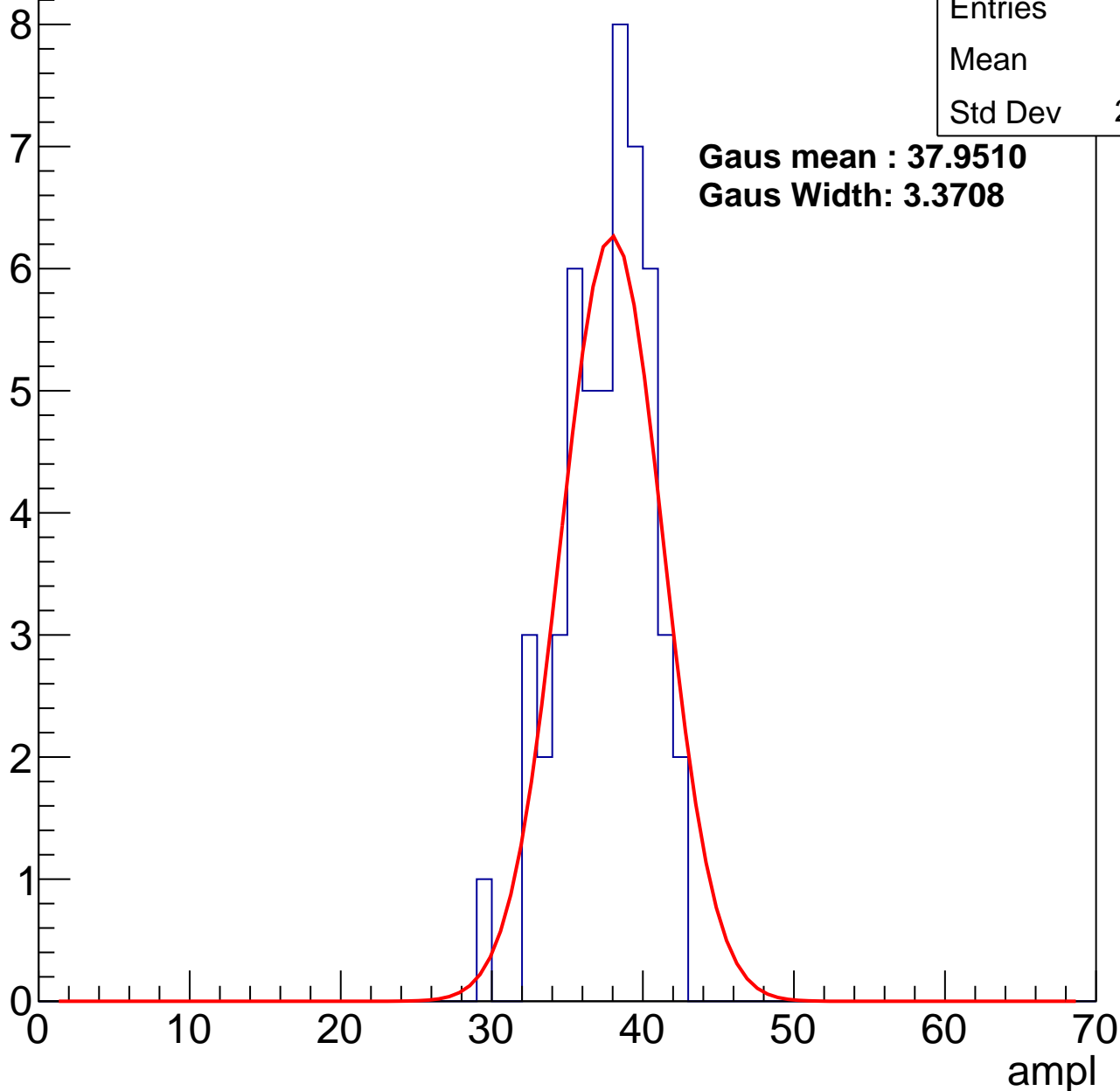
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	51
Mean	37.1
Std Dev	2.851

**Gaus mean : 37.9510**

**Gaus Width: 3.3708**



# B0L001S, U10-ch63, adc2

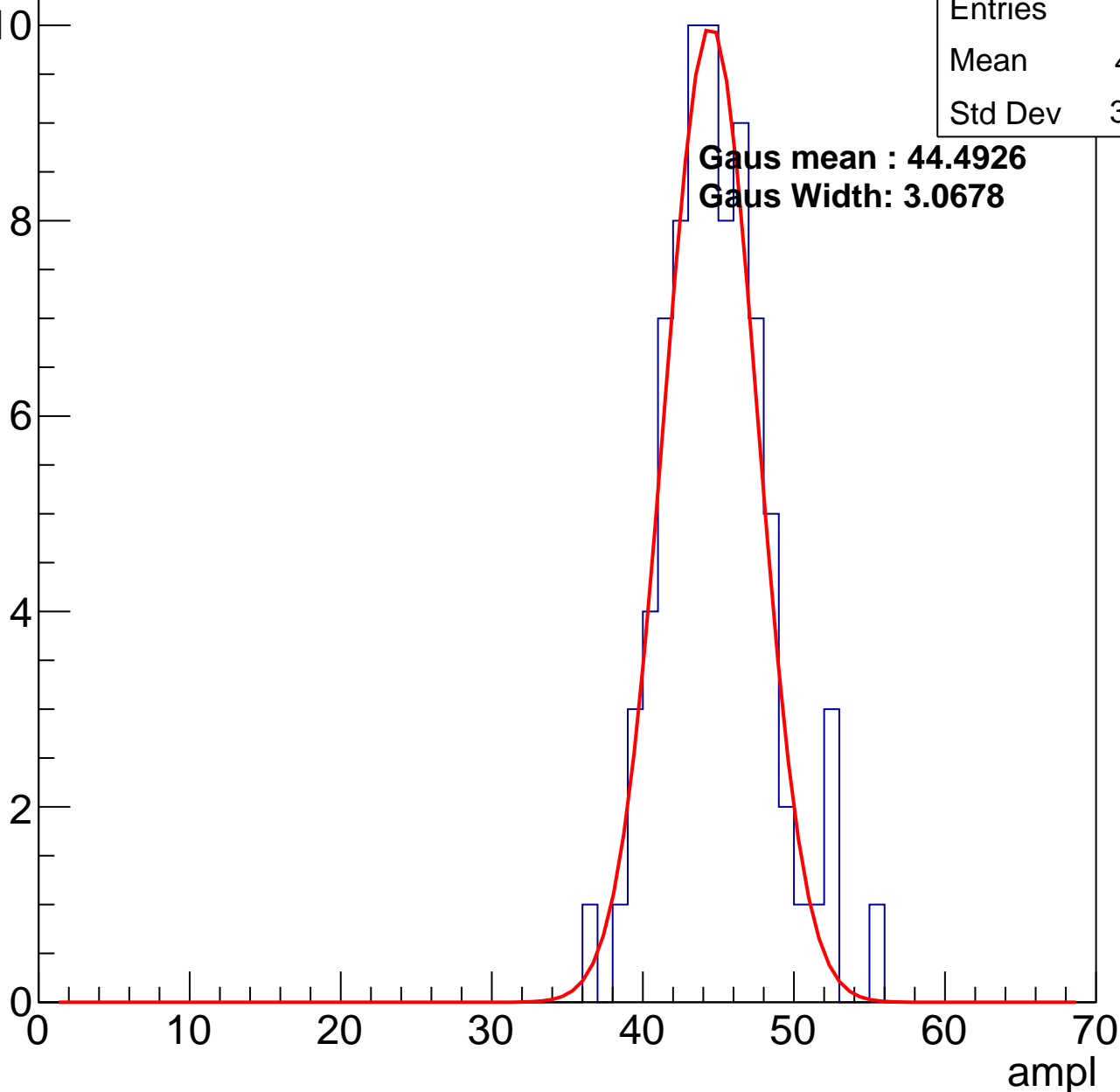
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	81
Mean	44.41
Std Dev	3.453

**Gaus mean : 44.4926**

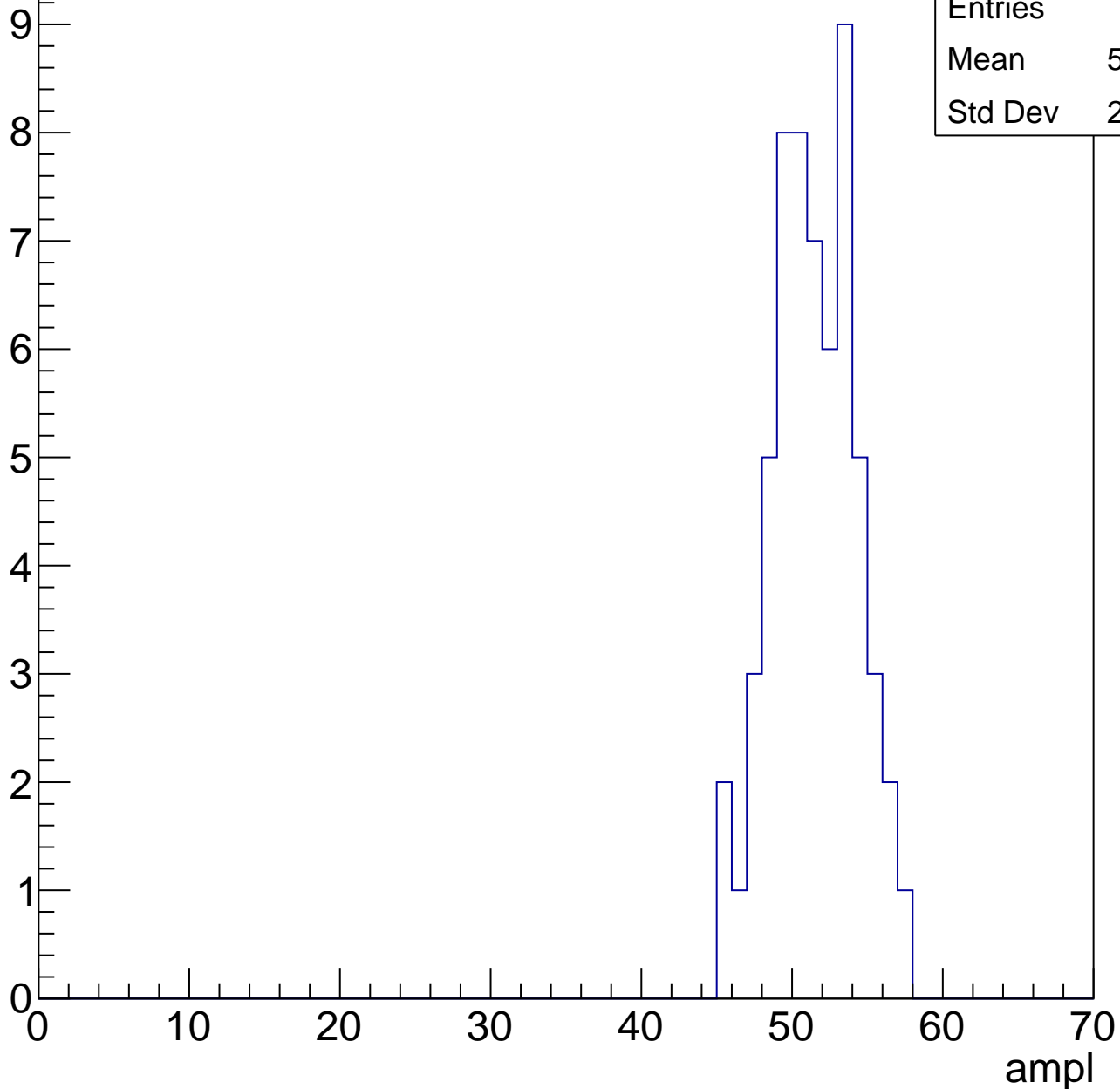
**Gaus Width: 3.0678**



# B0L001S, U10-ch63, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

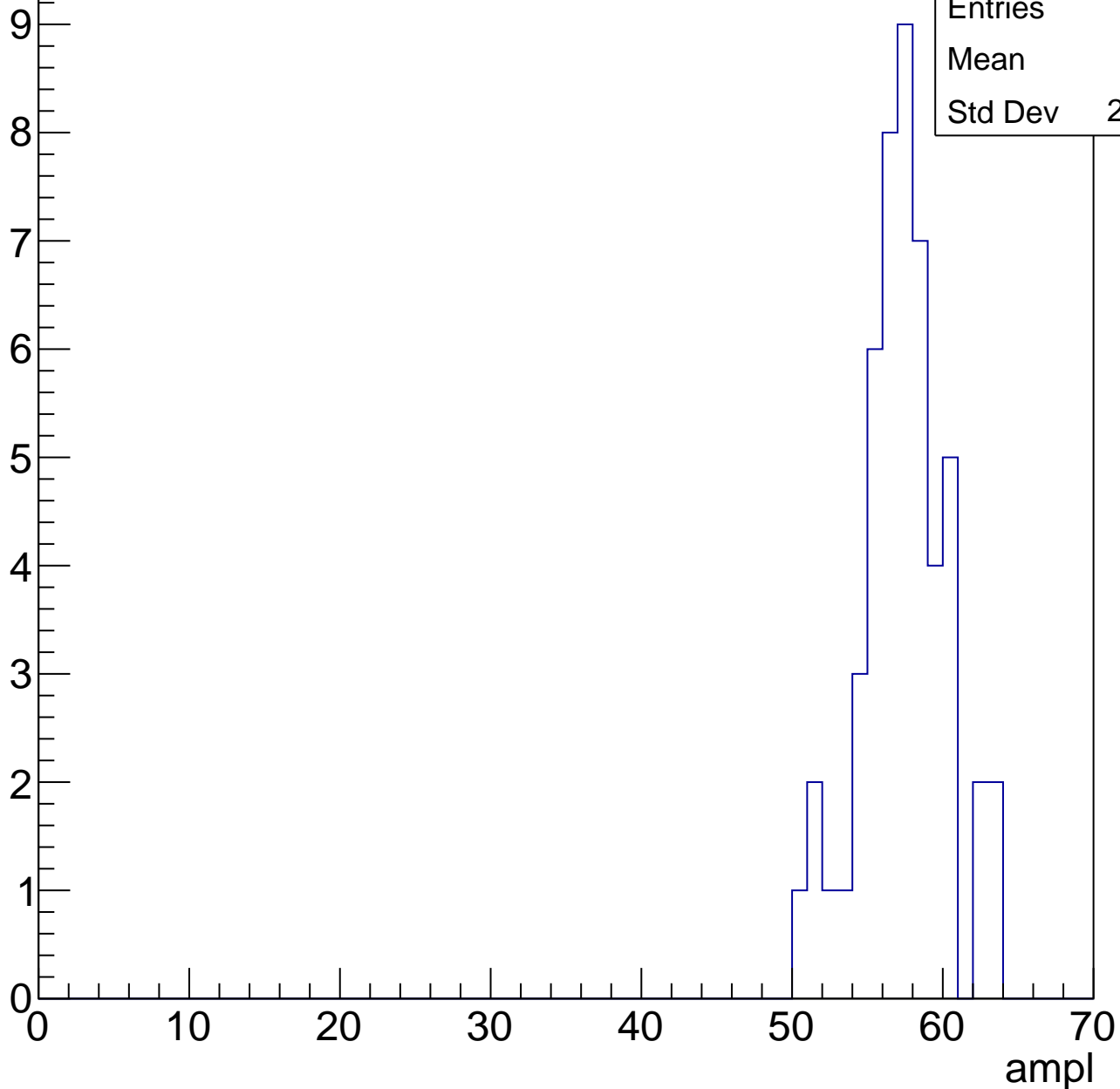


Entries	60
Mean	50.98
Std Dev	2.742

# B0L001S, U10-ch63, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U10-ch63, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	43
Mean	59.21
Std Dev	9.372

Entry

10

8

6

4

2

0

0

10

20

30

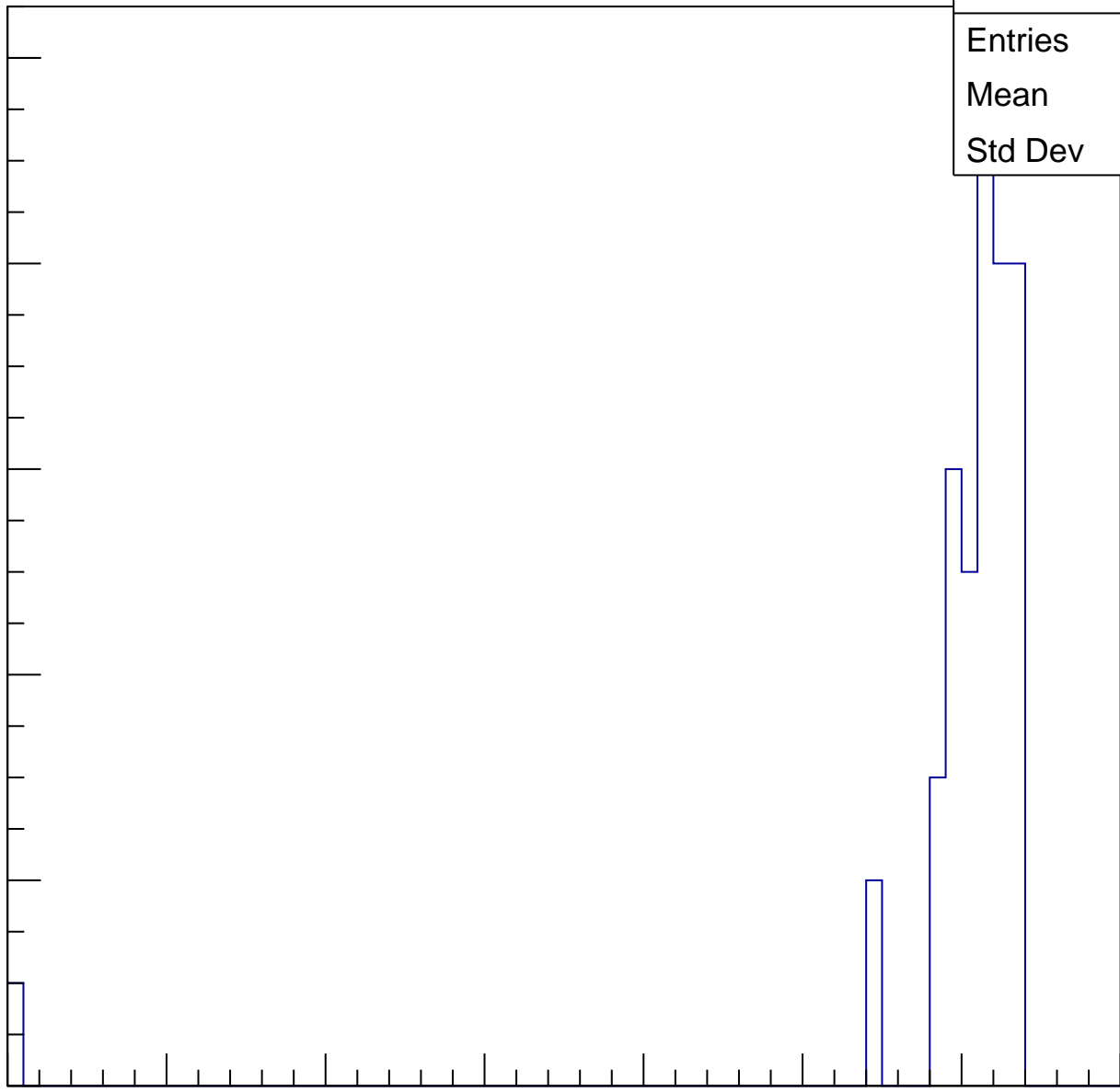
40

50

60

70

ampl



# B0L001S, U10-ch63, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U10-ch63, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U10-ch64, adc0

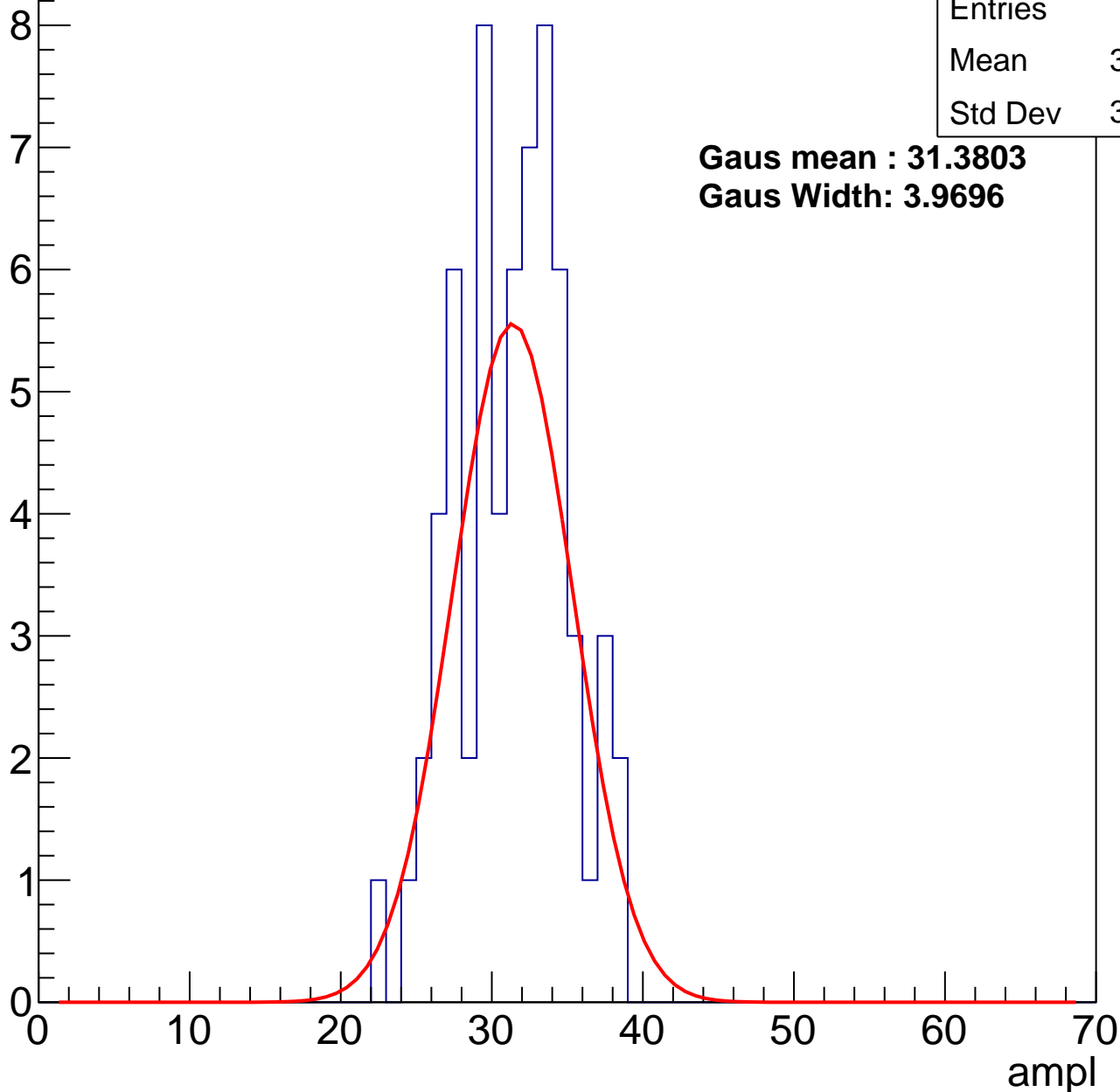
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	30.88
Std Dev	3.586

**Gaus mean : 31.3803**

**Gaus Width: 3.9696**



# B0L001S, U10-ch64, adc1

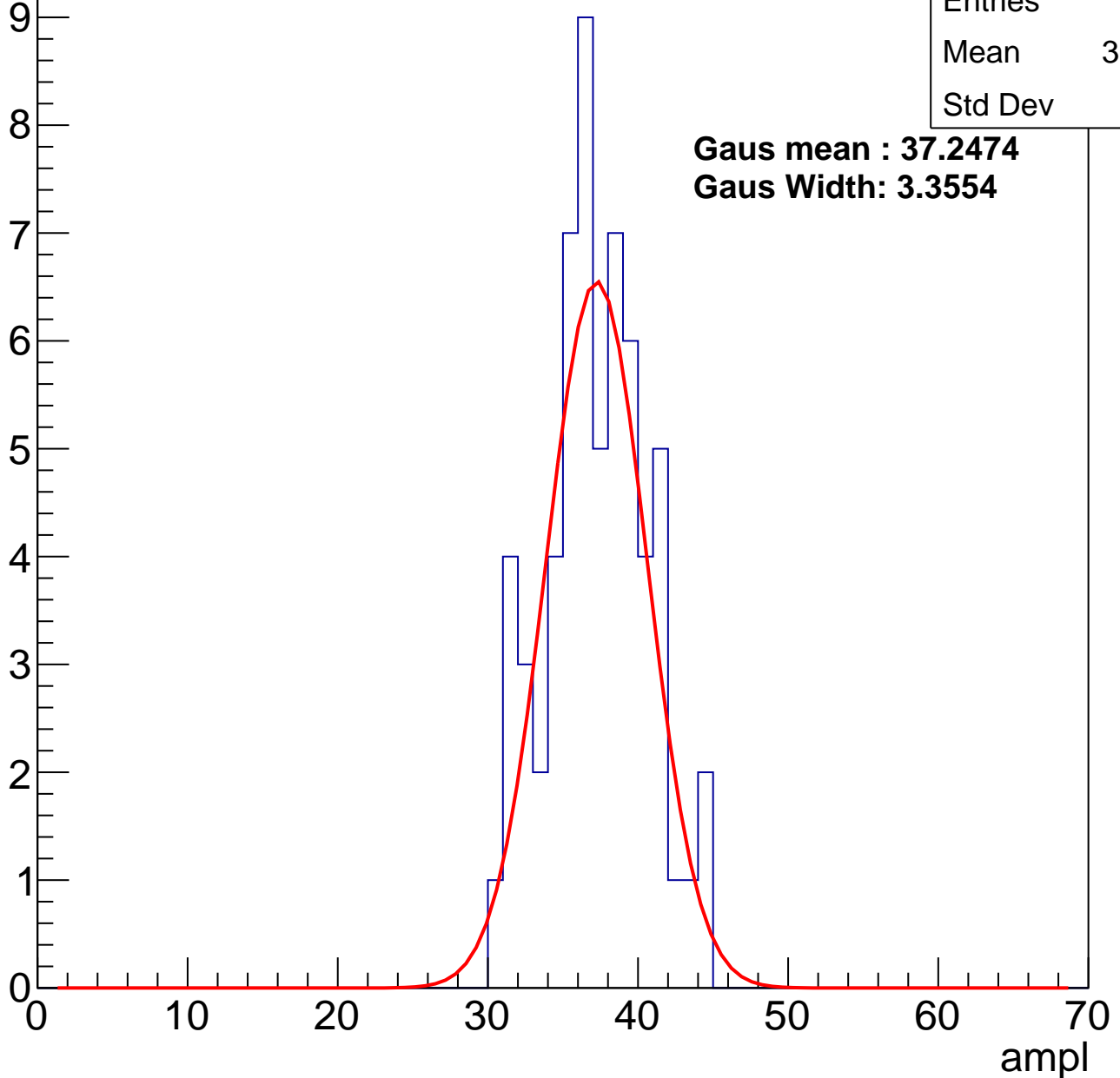
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	36.79
Std Dev	3.33

**Gaus mean : 37.2474**

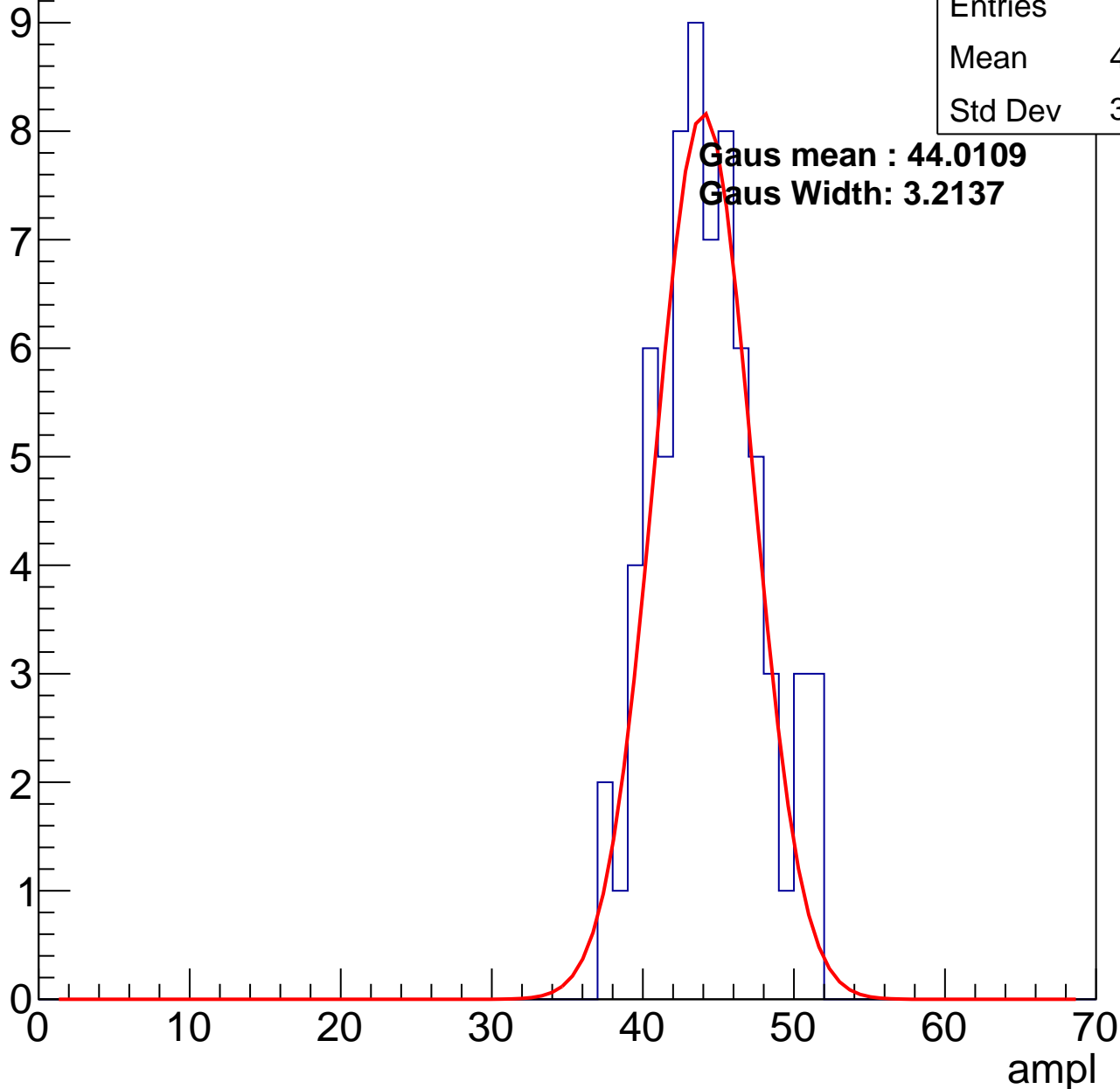
**Gaus Width: 3.3554**



# B0L001S, U10-ch64, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

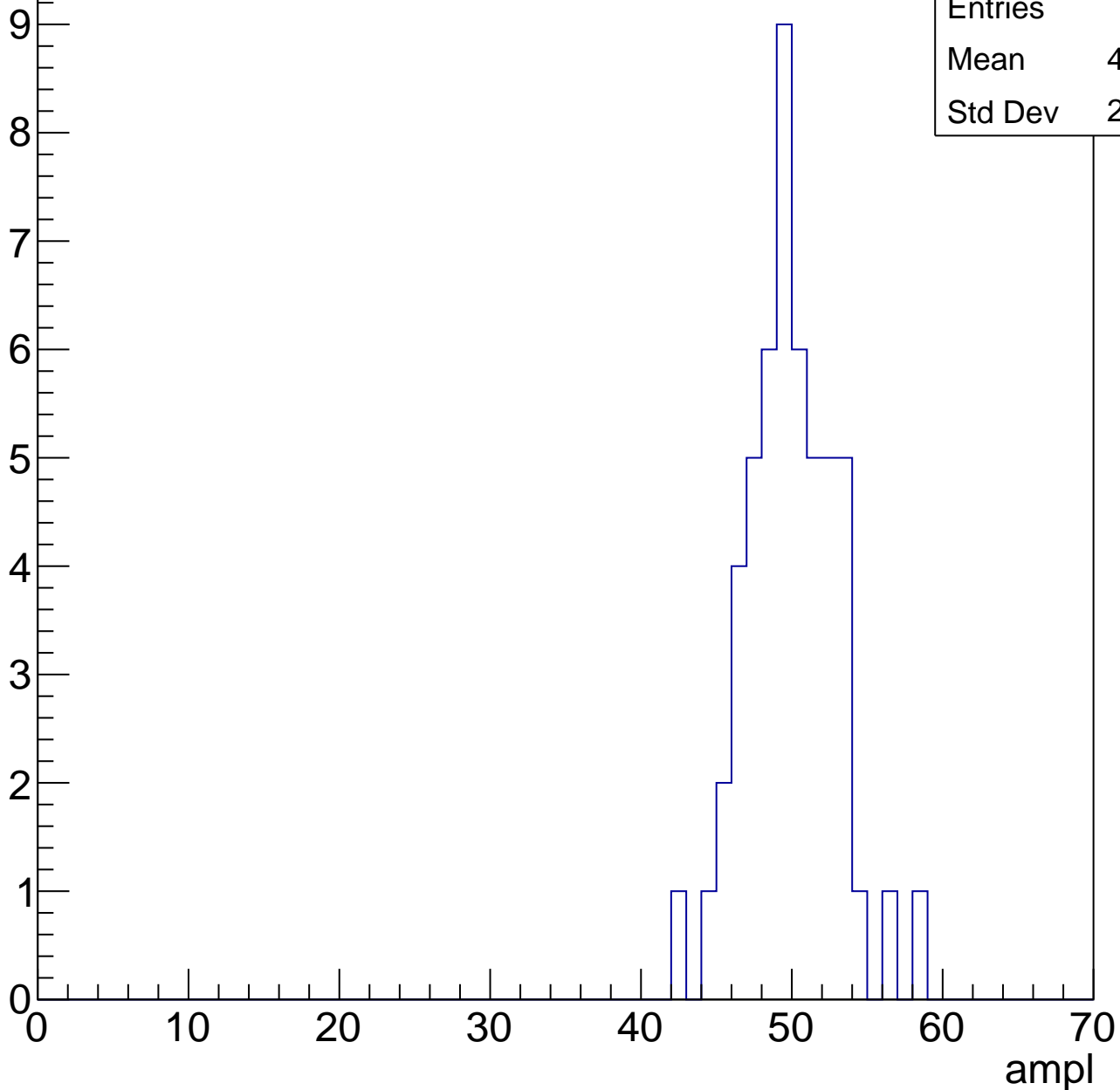


# B0L001S, U10-ch64, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	49.46
Std Dev	2.984



# B0L001S, U10-ch64, adc4

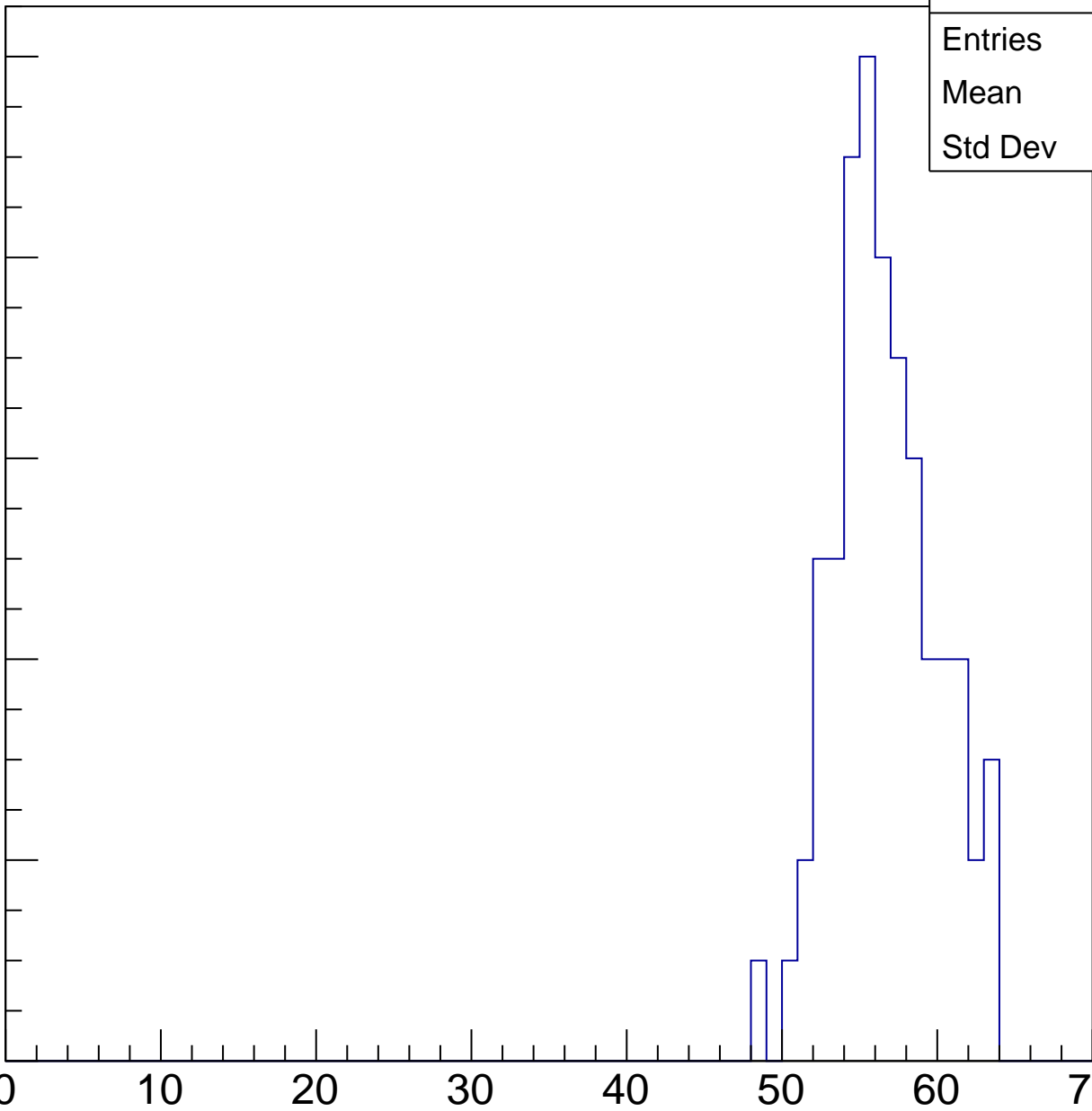
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	71
Mean	56.18
Std Dev	3.29

Entry

10  
8  
6  
4  
2  
0

ampl

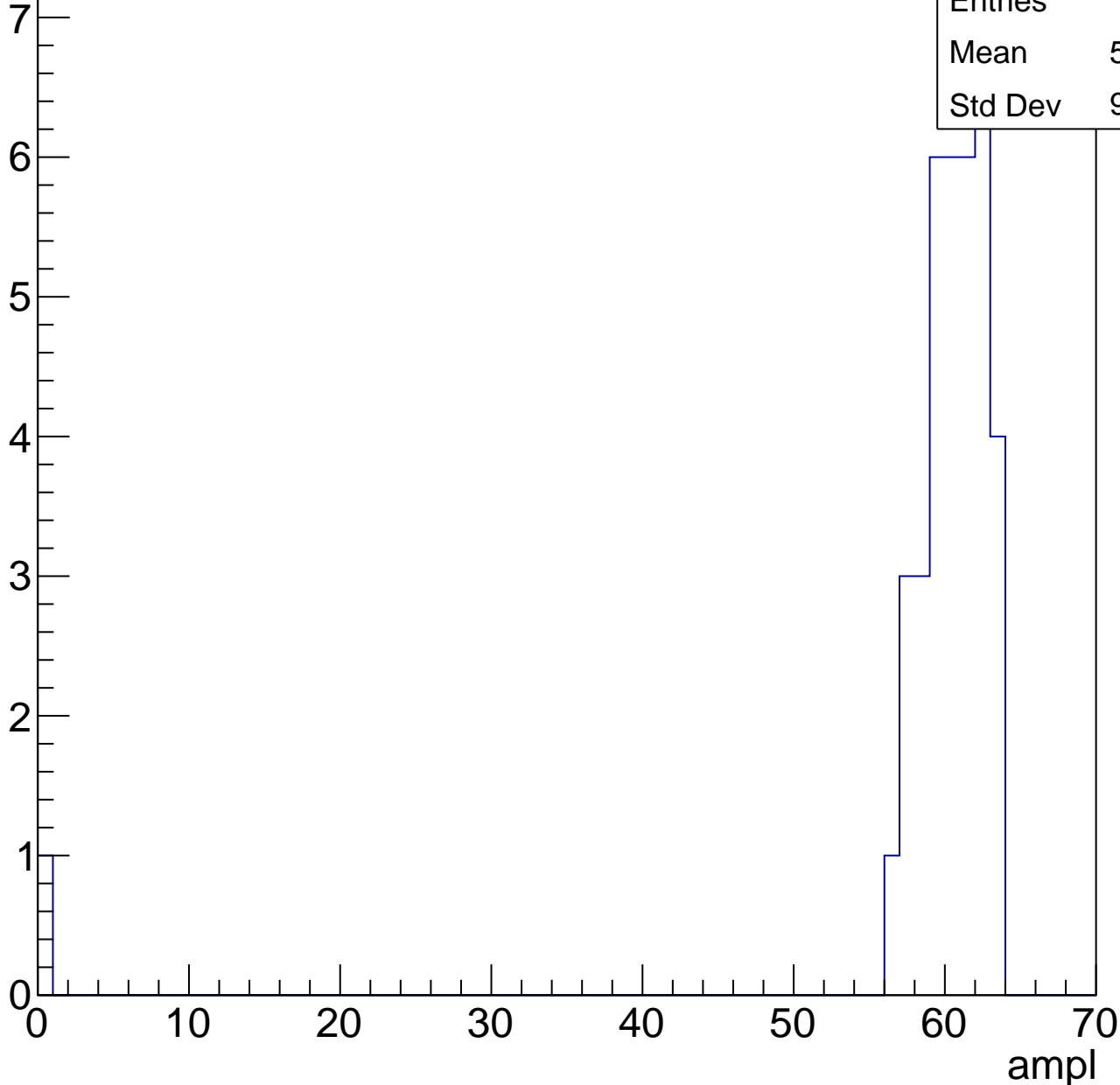


# B0L001S, U10-ch64, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	37
Mean	58.57
Std Dev	9.939



# B0L001S, U10-ch64, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch64, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U10-ch65, adc0

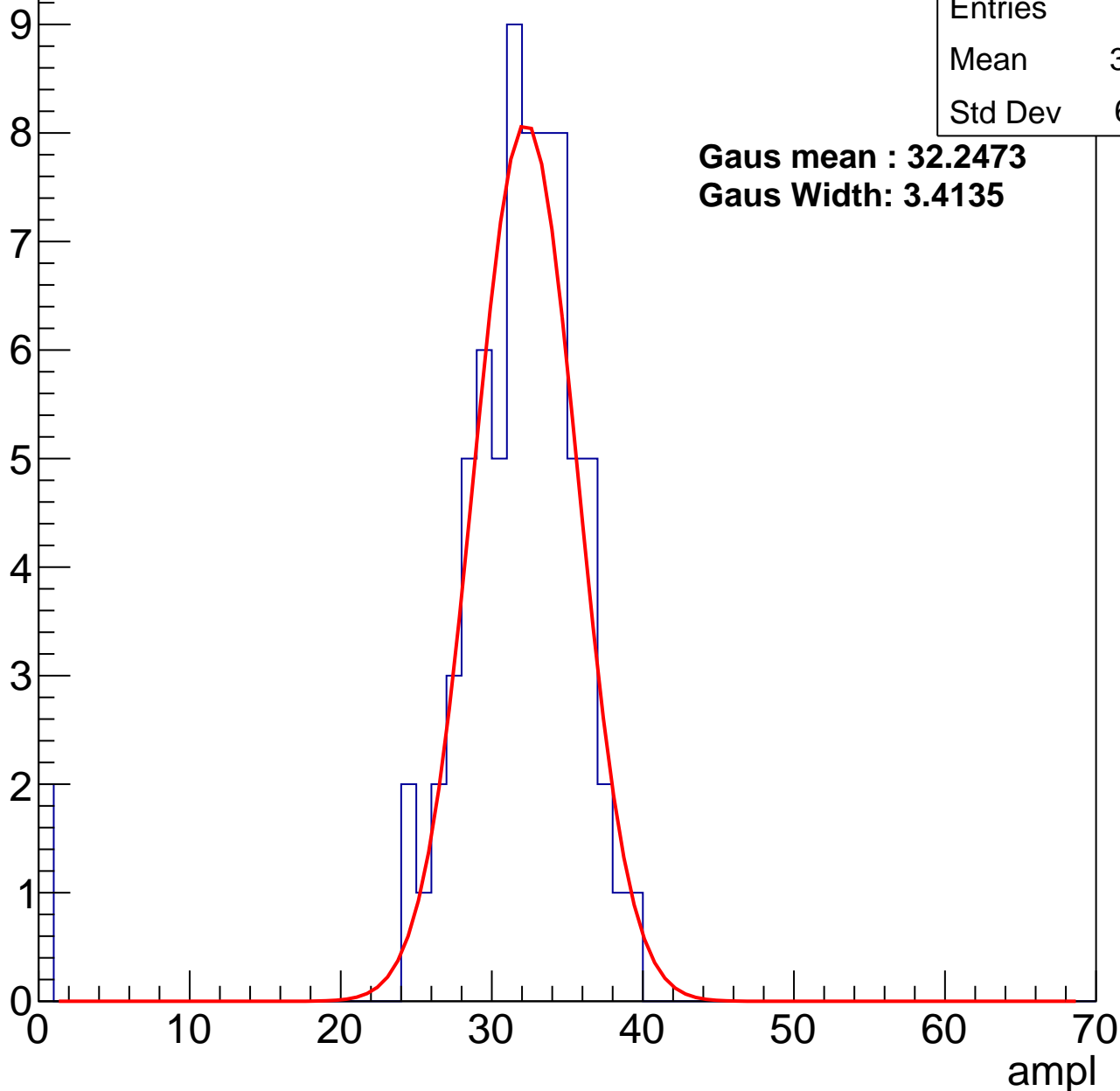
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	30.78
Std Dev	6.111

**Gaus mean : 32.2473**

**Gaus Width: 3.4135**



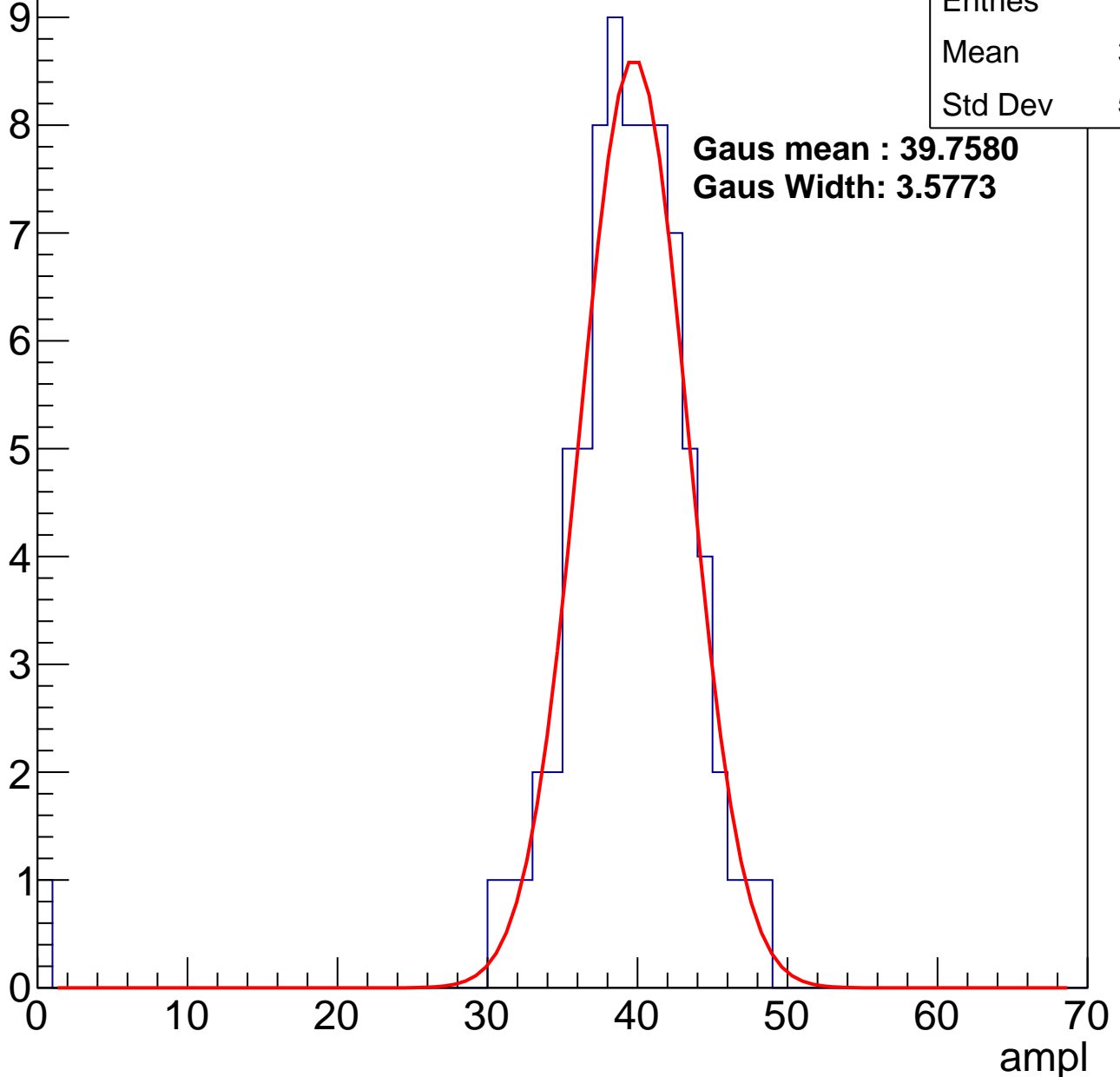
# B0L001S, U10-ch65, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	80
Mean	38.7
Std Dev	5.64

**Gaus mean : 39.7580**  
**Gaus Width: 3.5773**



# B0L001S, U10-ch65, adc2

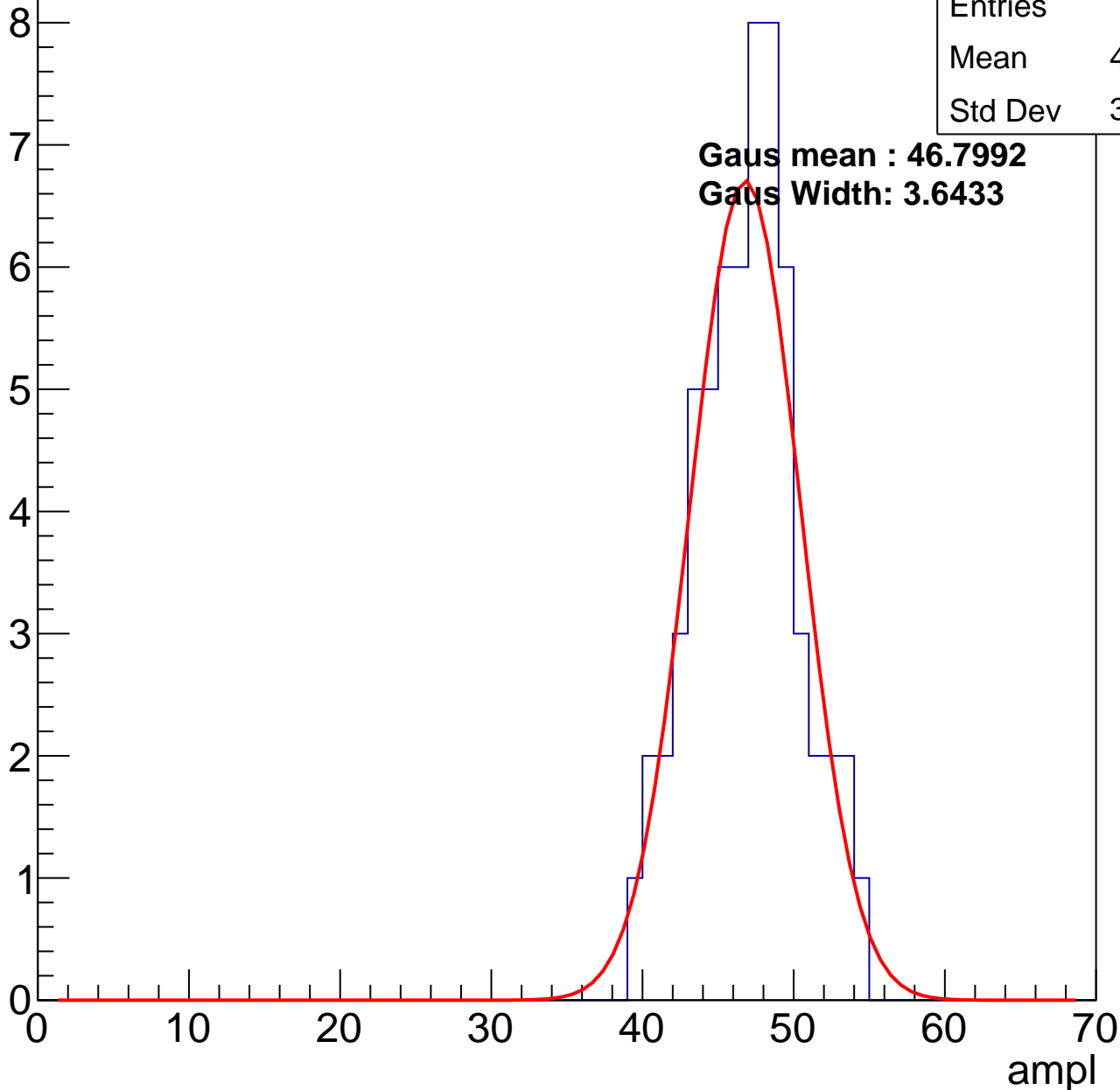
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	46.42
Std Dev	3.372

**Gaus mean : 46.7992**

**Gaus Width: 3.6433**

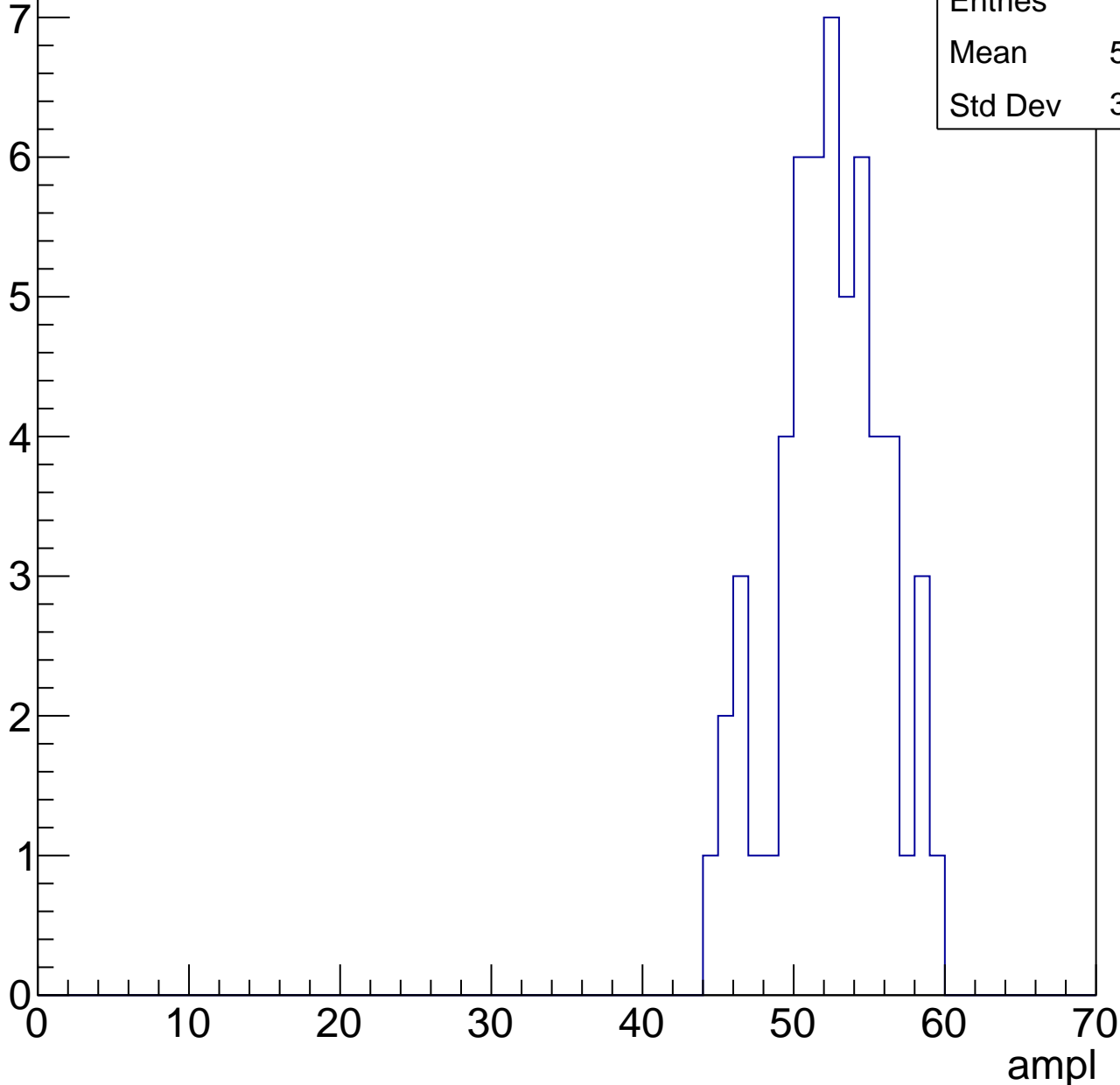


# B0L001S, U10-ch65, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	51.93
Std Dev	3.536

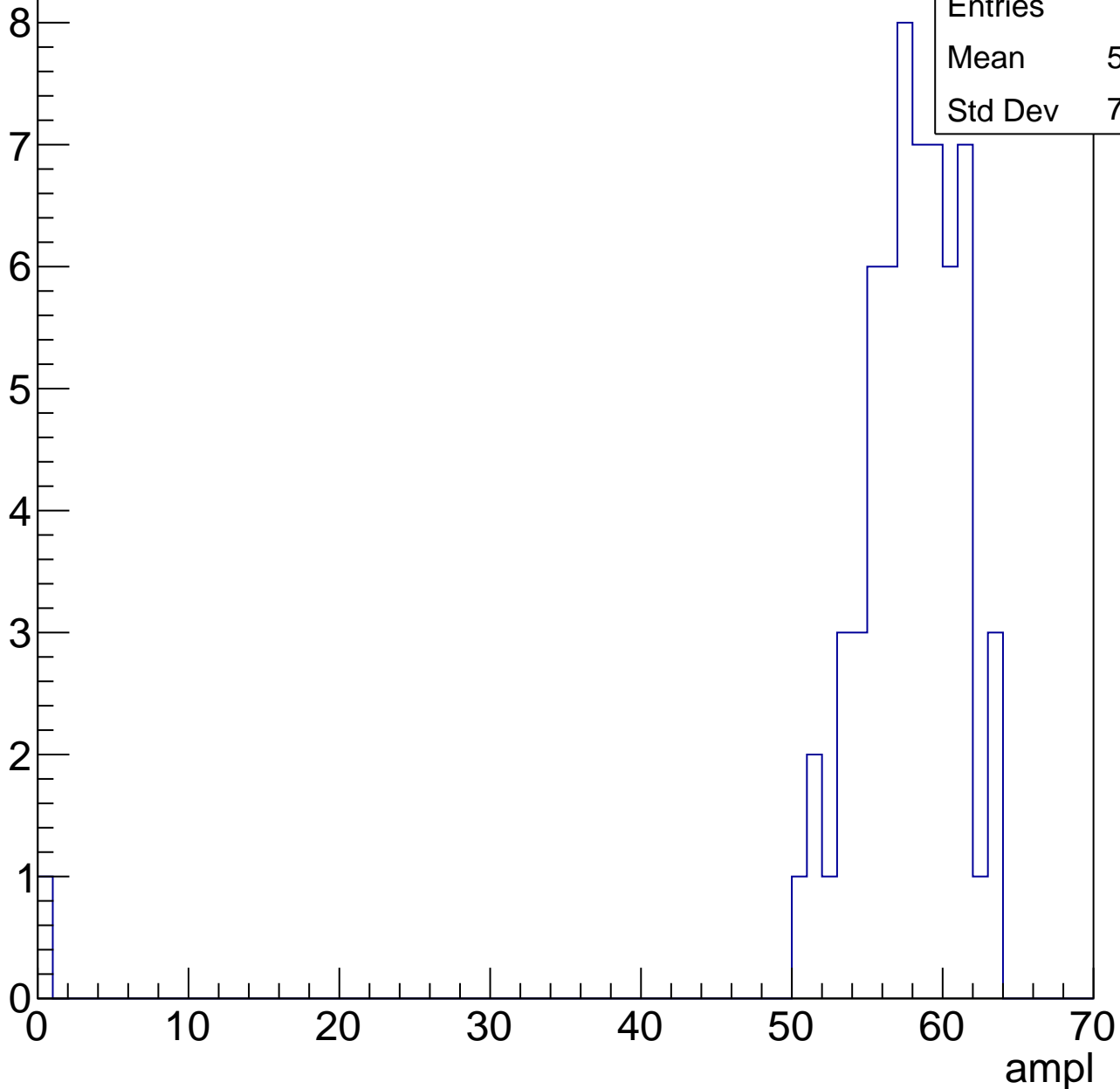


# B0L001S, U10-ch65, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	56.52
Std Dev	7.849

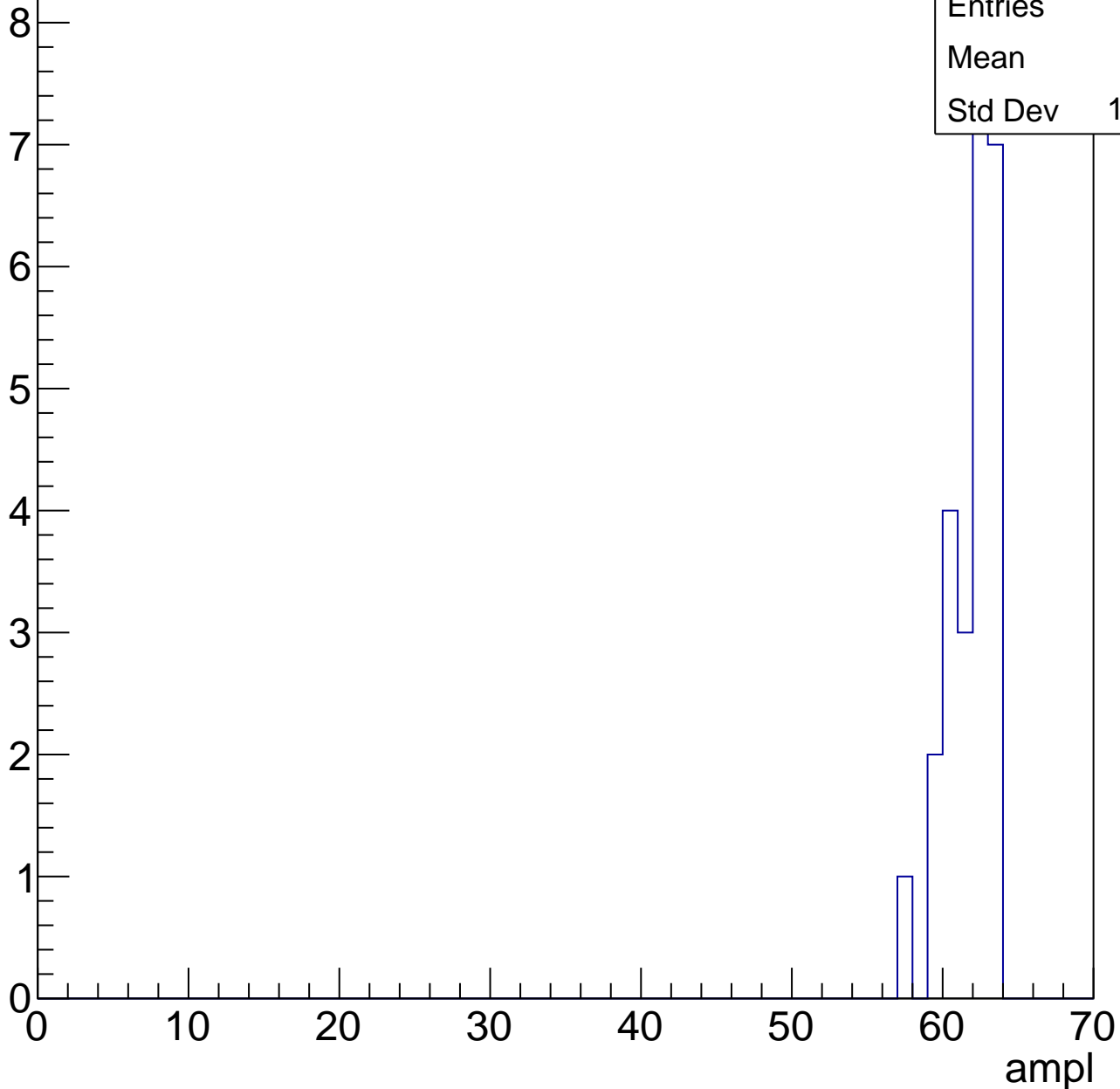


# B0L001S, U10-ch65, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	25
Mean	61.4
Std Dev	1.549



# B0L001S, U10-ch65, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	62
Std Dev	0



# B0L001S, U10-ch65, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U10-ch66, adc0

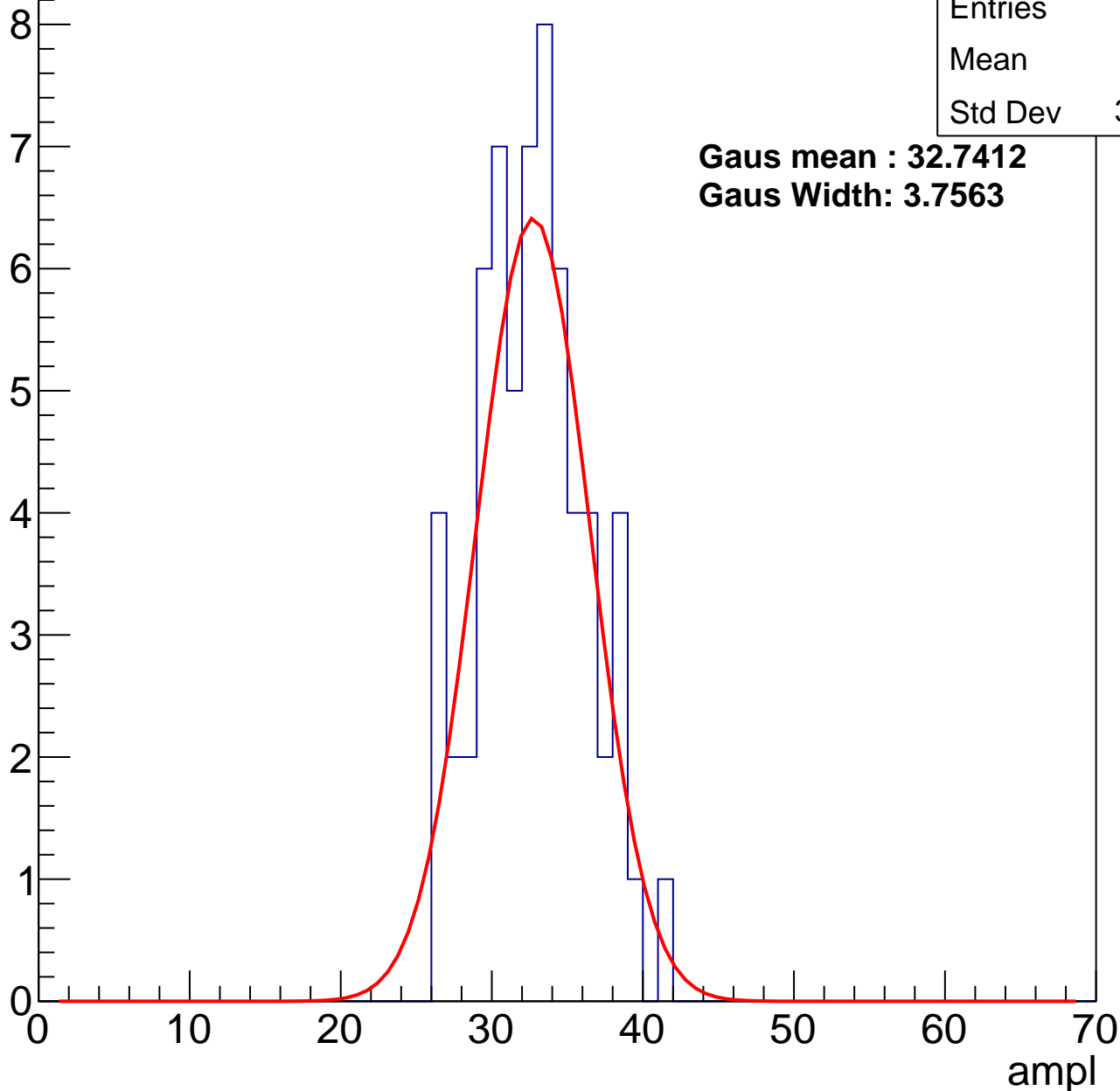
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	32.3
Std Dev	3.481

**Gaus mean : 32.7412**

**Gaus Width: 3.7563**



# B0L001S, U10-ch66, adc1

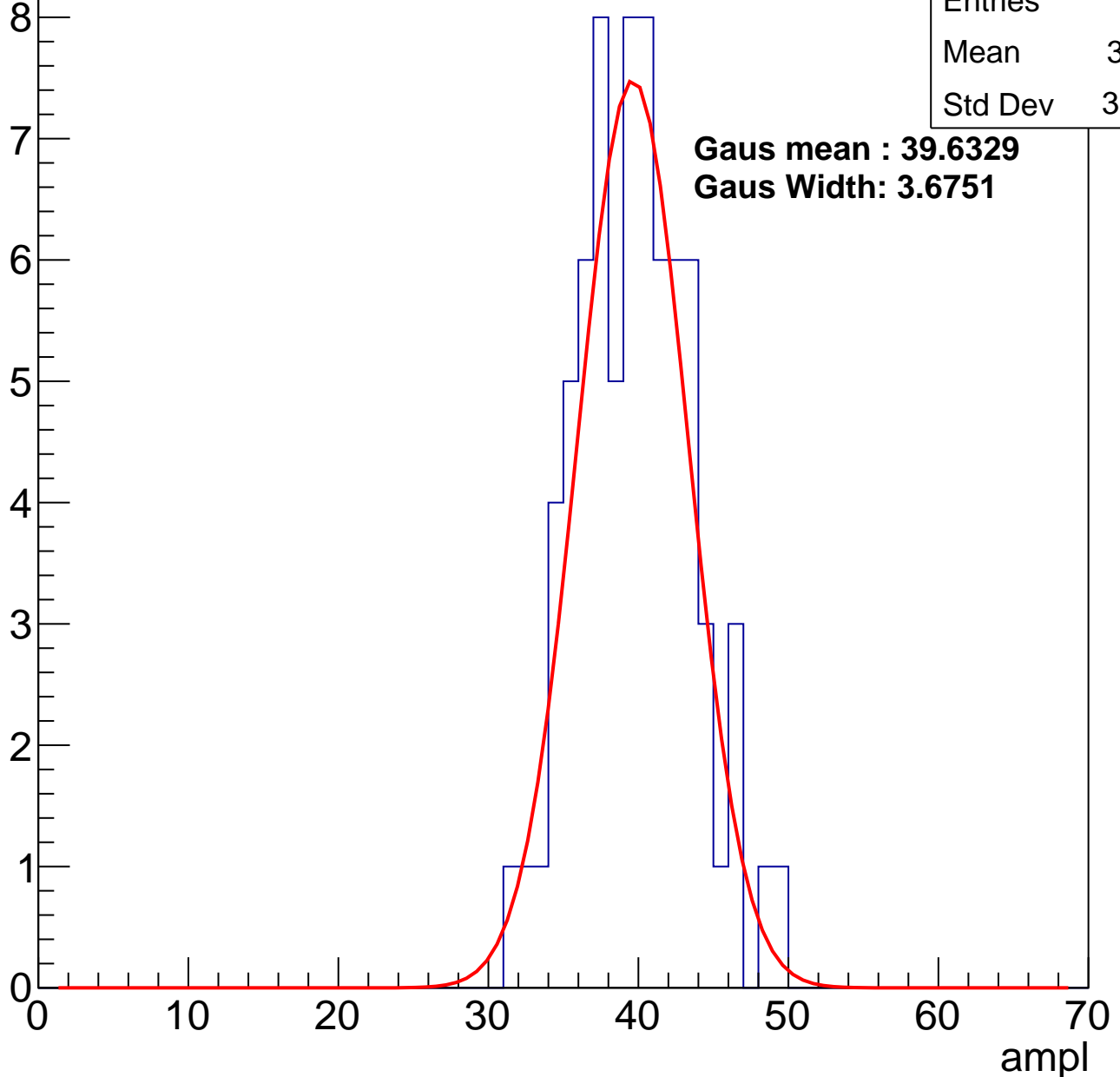
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	39.31
Std Dev	3.738

**Gaus mean : 39.6329**

**Gaus Width: 3.6751**



# B0L001S, U10-ch66, adc2

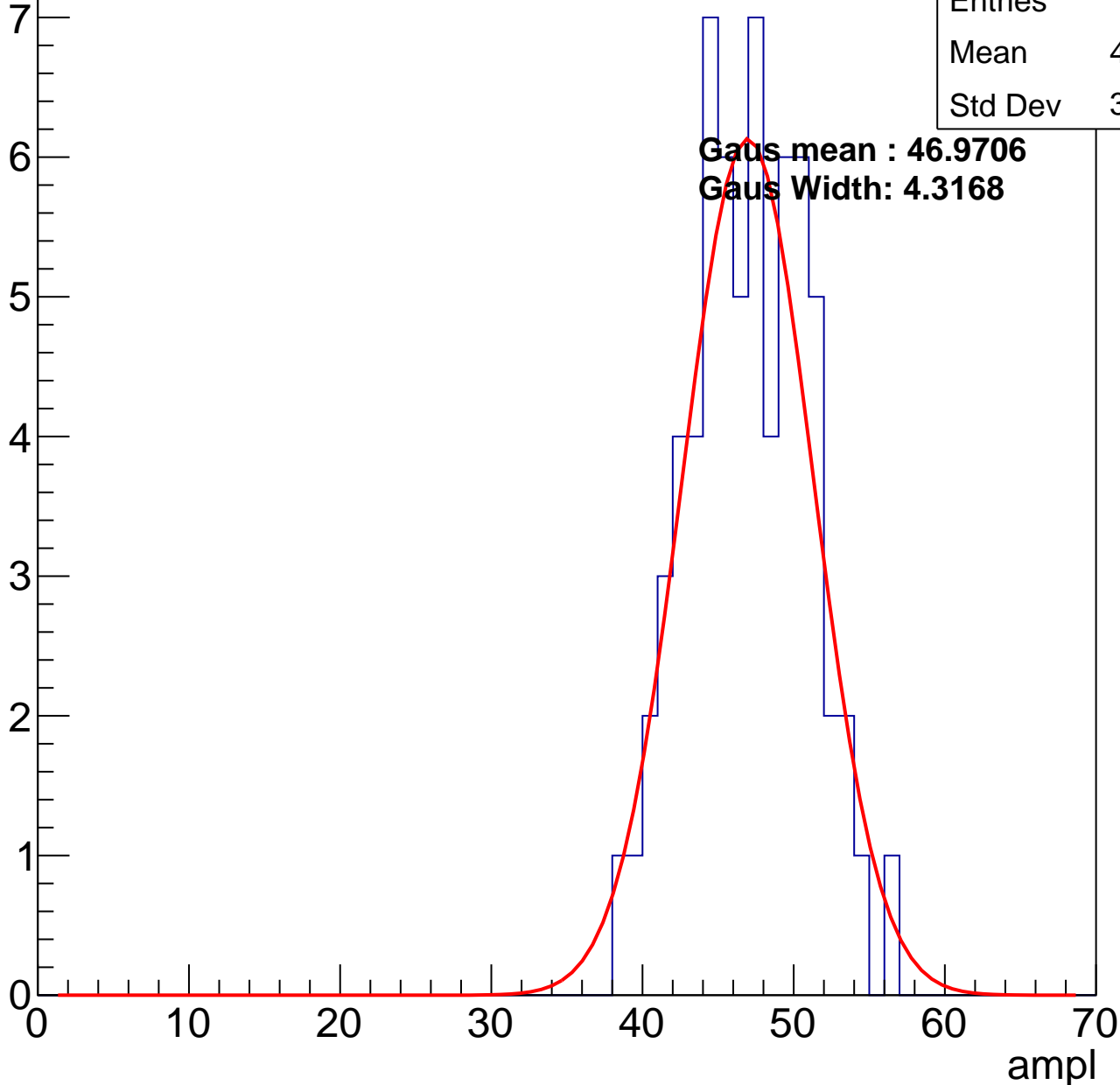
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	46.54
Std Dev	3.876

**Gaus mean : 46.9706**

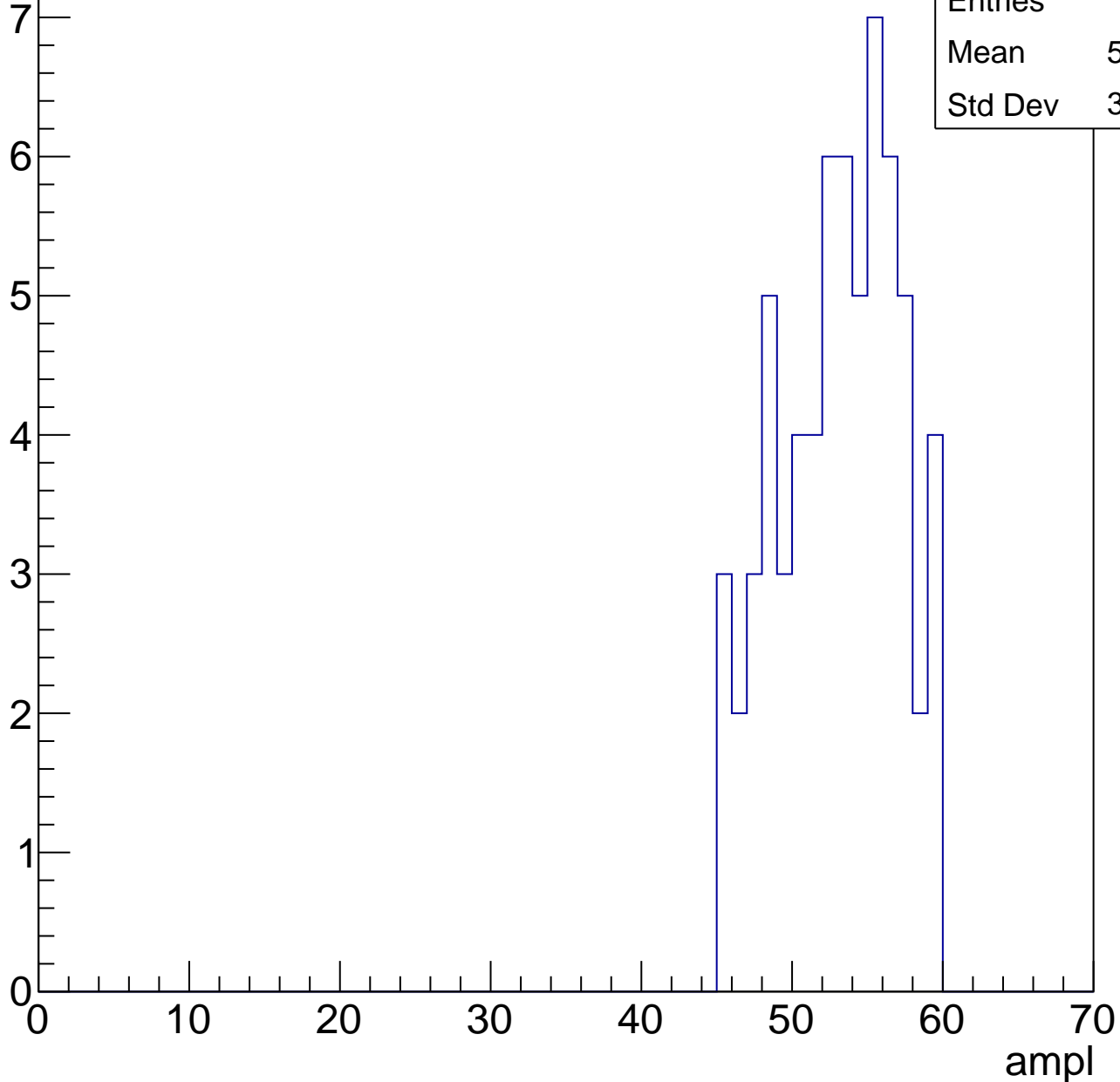
**Gaus Width: 4.3168**



# B0L001S, U10-ch66, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

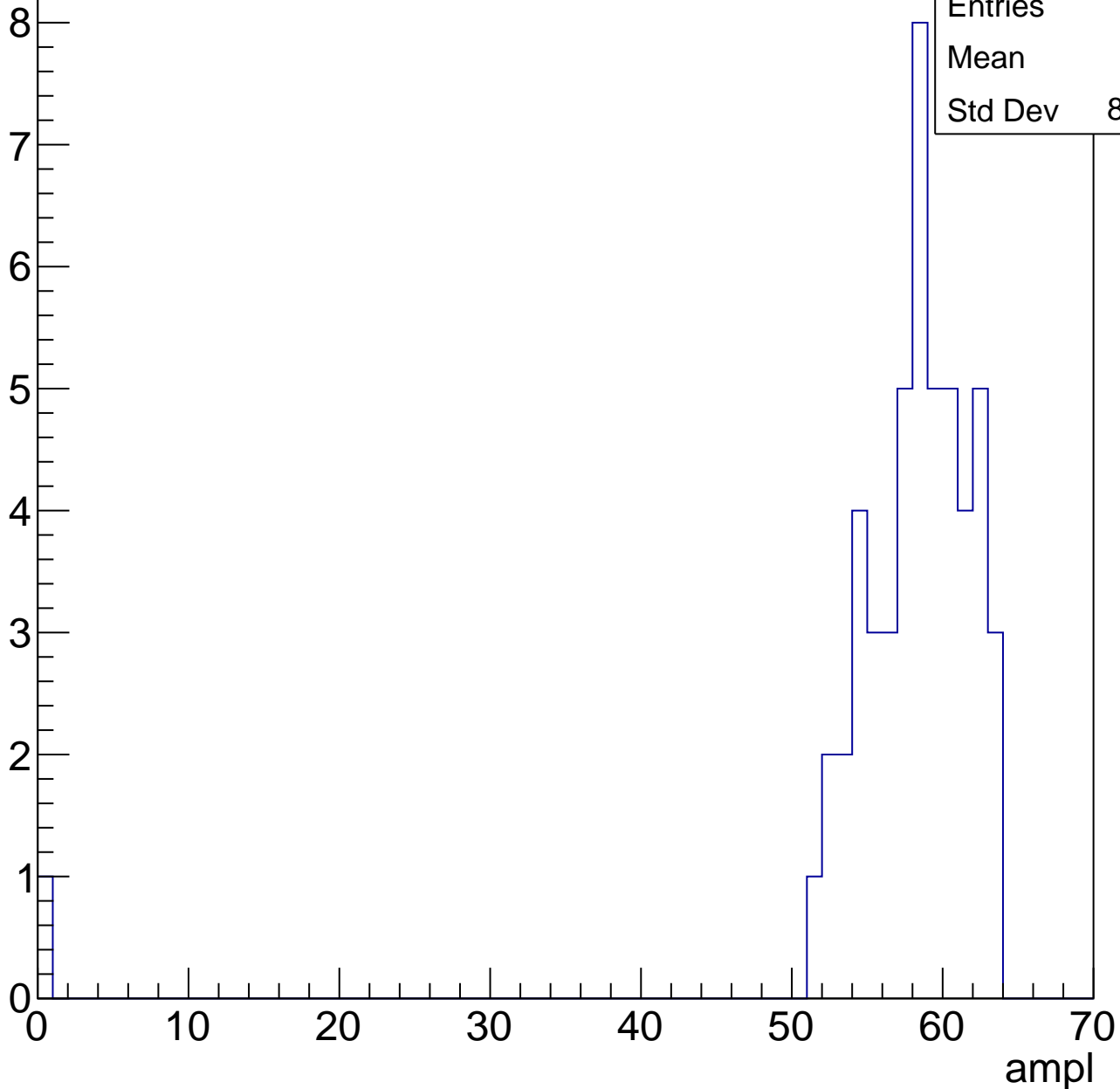


# B0L001S, U10-ch66, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

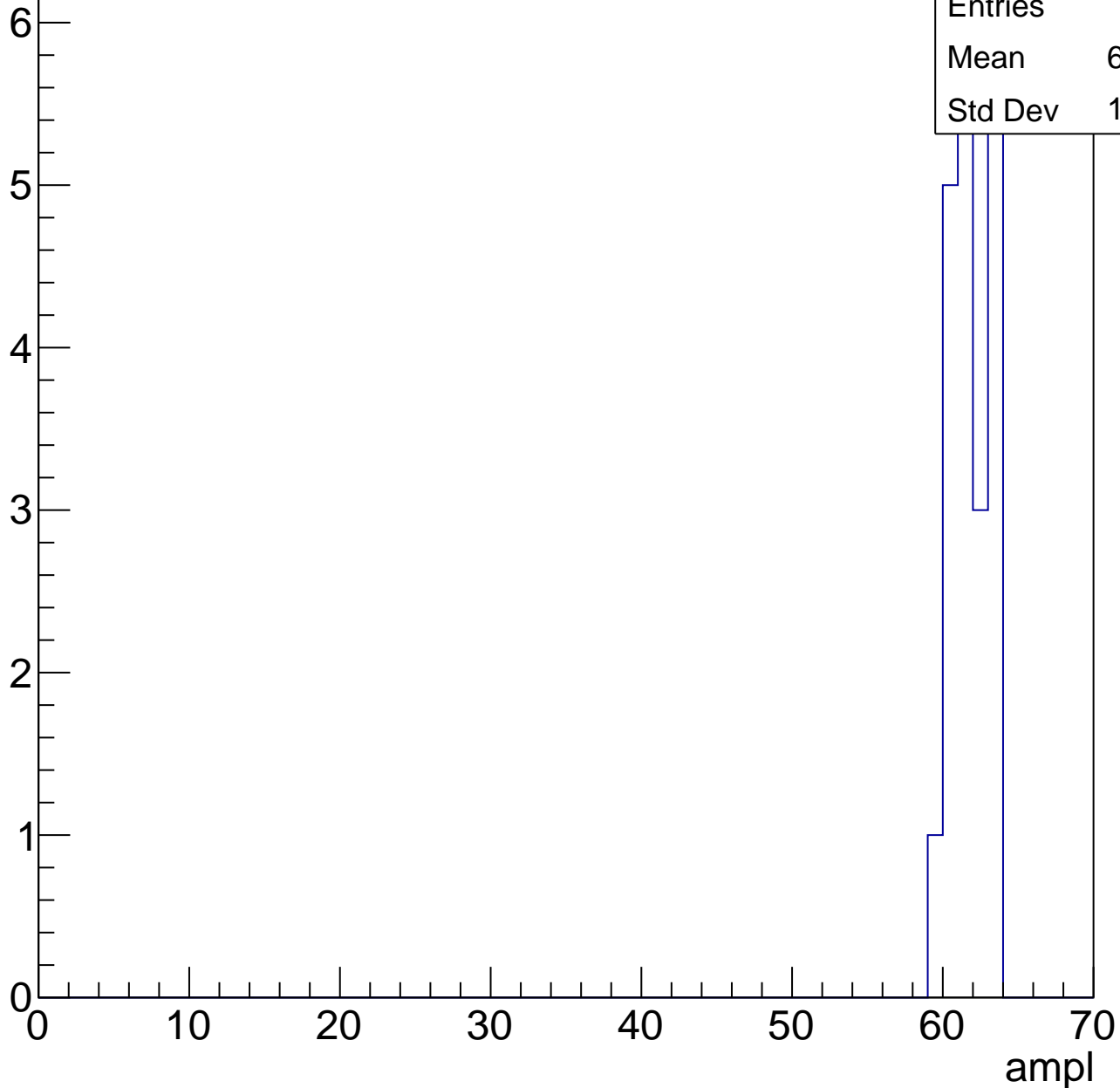
Entries	51
Mean	56.8
Std Dev	8.616



# B0L001S, U10-ch66, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U10-ch66, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.33
Std Dev	0.4714

ampl





# B0L001S, U10-ch66, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	3
Mean	8.333
Std Dev	11.79

# B0L001S, U10-ch67, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	65
Mean	29.8
Std Dev	3.306

**Gaus mean : 30.6169**

**Gaus Width: 3.0491**

Entry

10  
8  
6  
4  
2  
0

ampl

0

10

20

30

40

50

60

70

# B0L001S, U10-ch67, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	86
Mean	37.45
Std Dev	3.422

**Gaus mean : 37.8977**

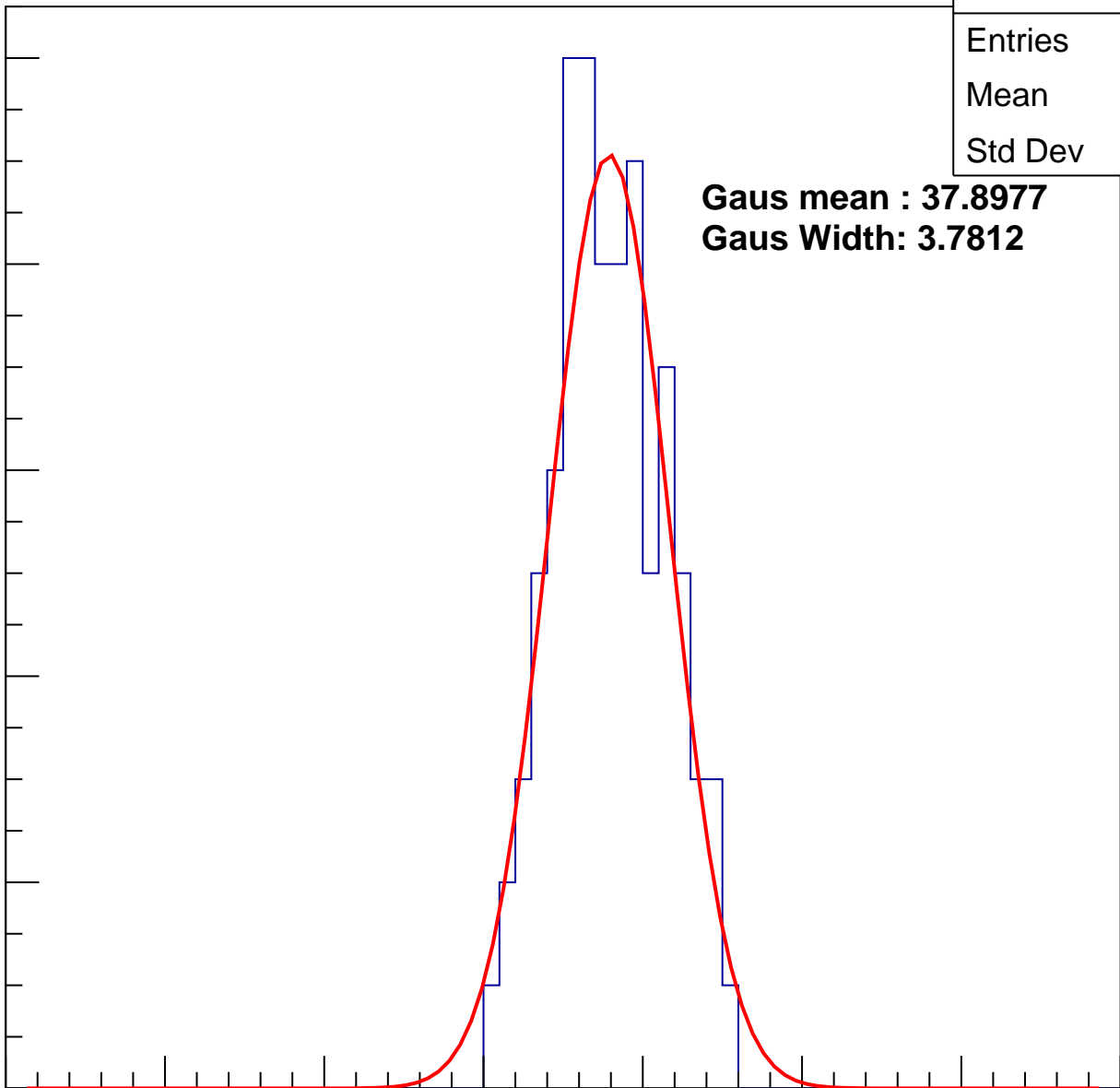
**Gaus Width: 3.7812**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U10-ch67, adc2

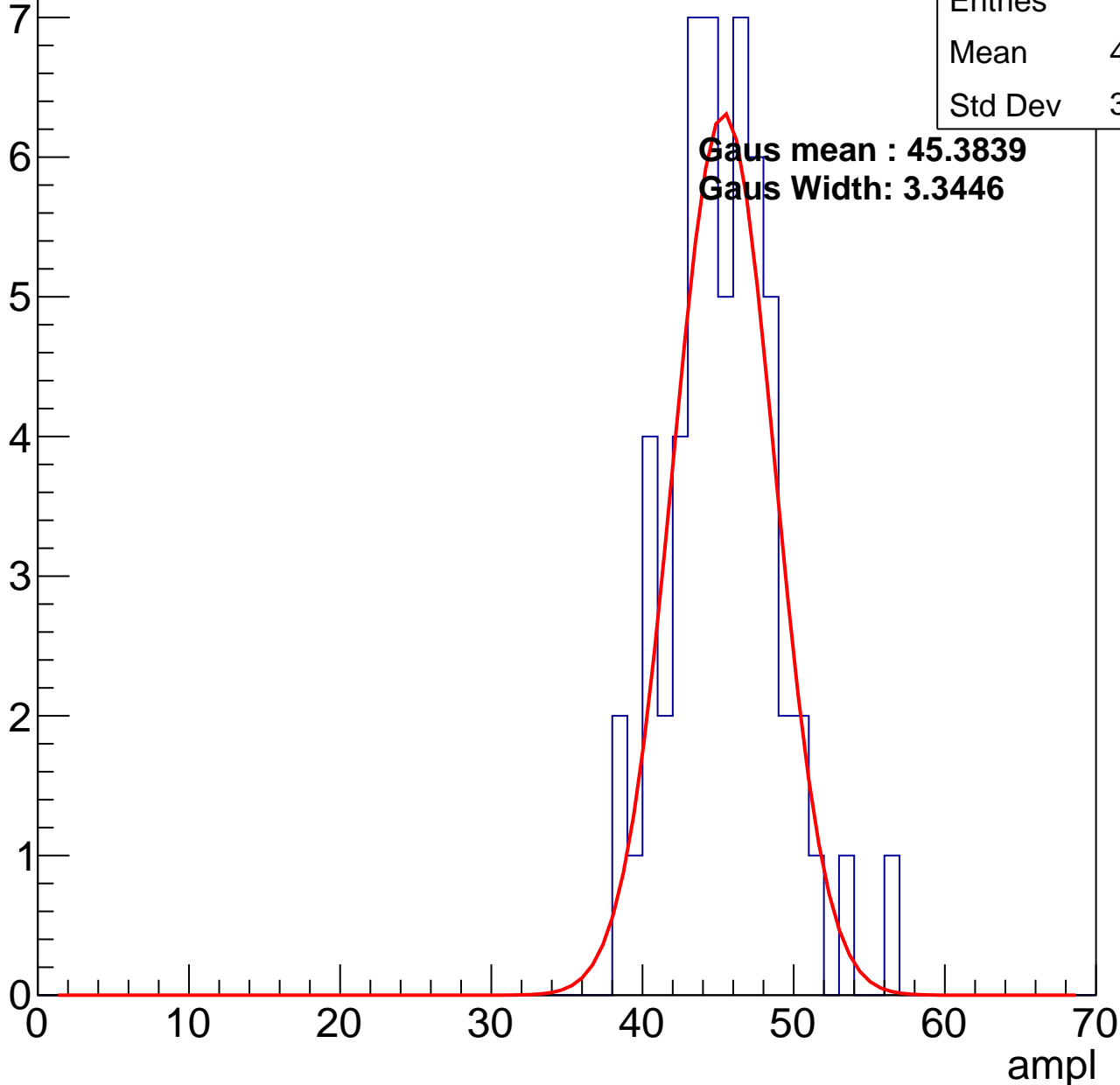
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	44.93
Std Dev	3.544

**Gaus mean : 45.3839**

**Gaus Width: 3.3446**

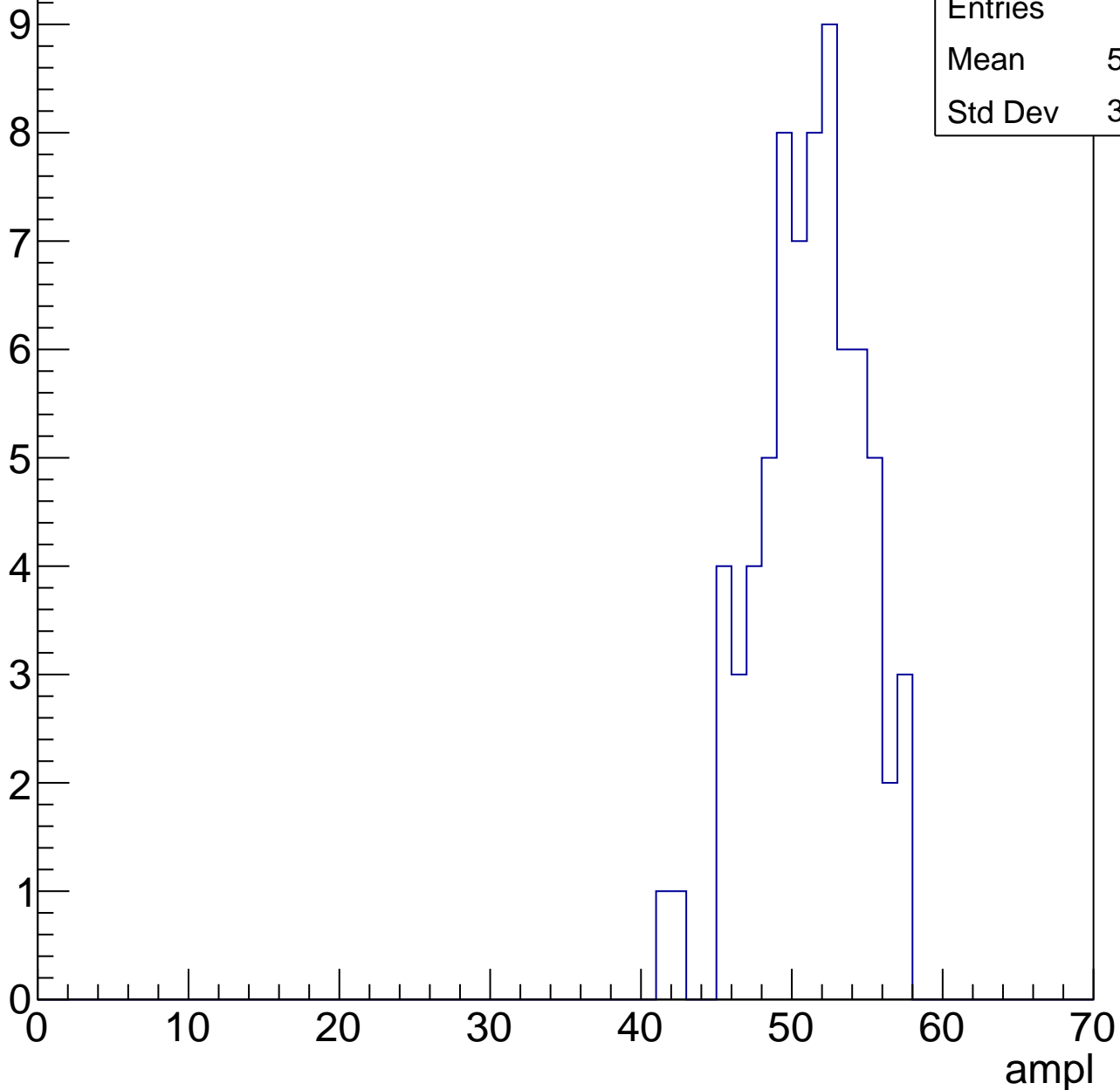


# B0L001S, U10-ch67, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	50.65
Std Dev	3.465



# B0L001S, U10-ch67, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

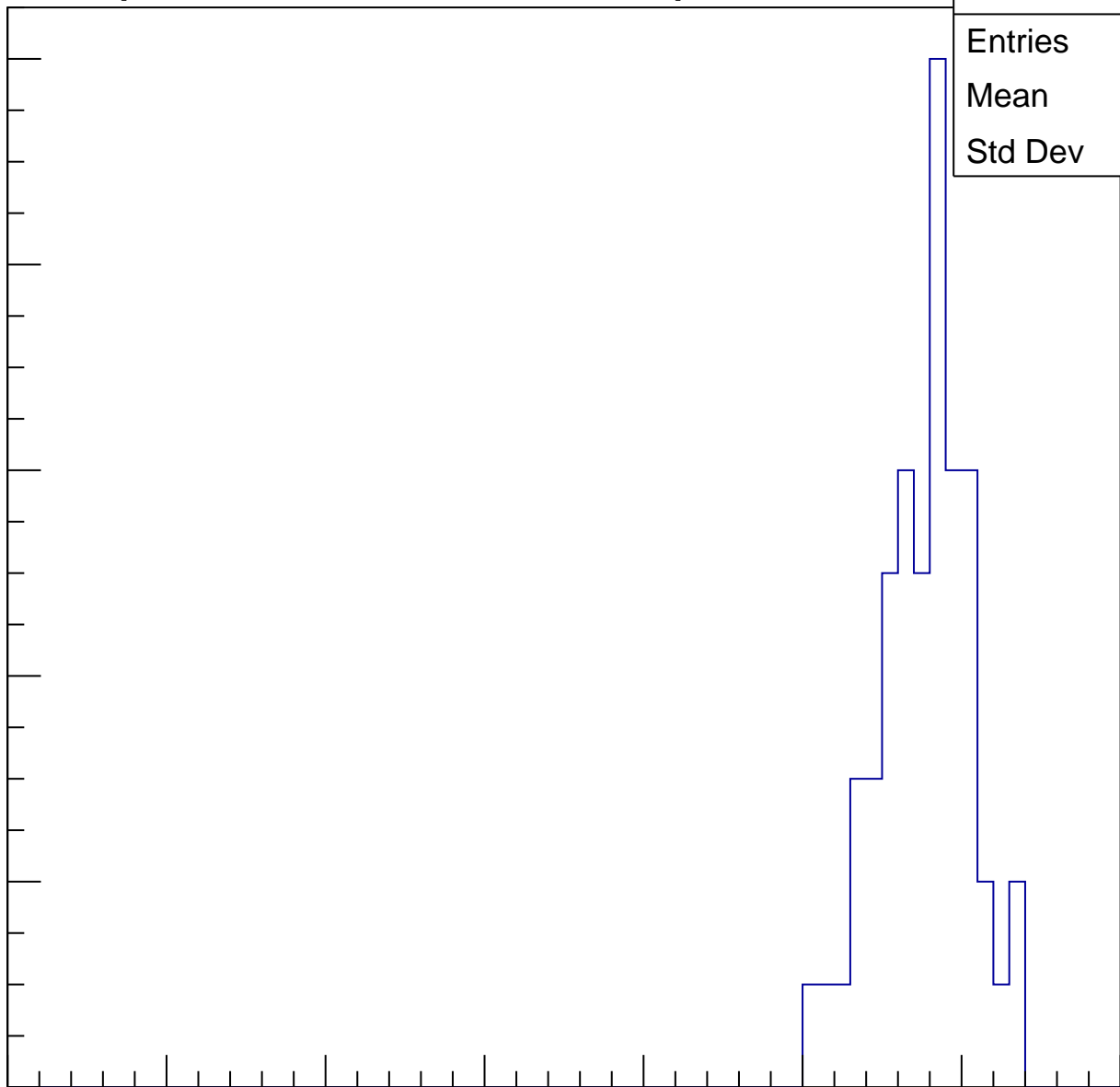
Entries	52
Mean	57.19
Std Dev	2.862

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

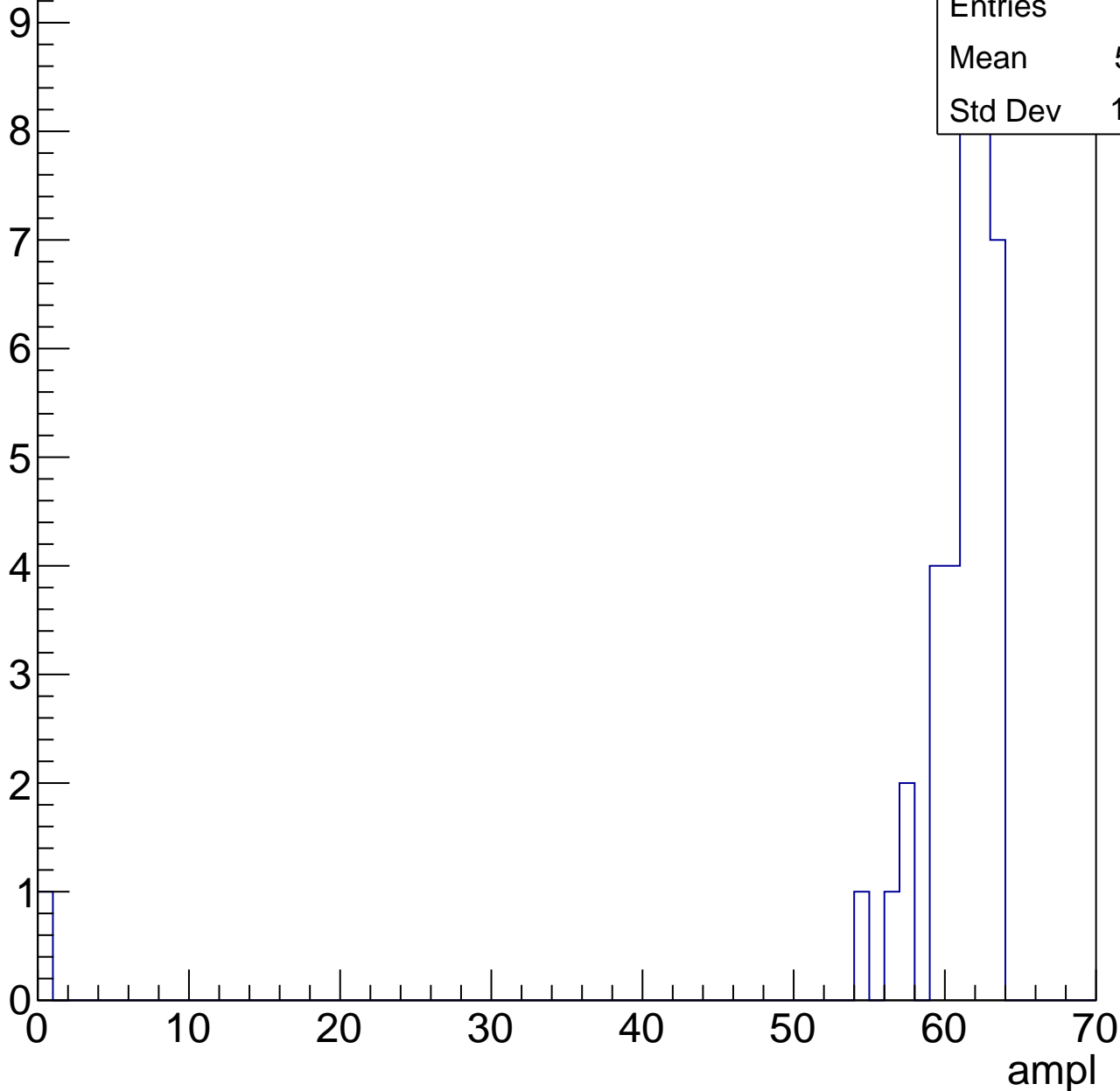


# B0L001S, U10-ch67, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	37
Mean	59.11
Std Dev	10.07



# B0L001S, U10-ch67, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

1

Mean

63

Std Dev

0



# B0L001S, U10-ch67, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U10-ch68, adc0

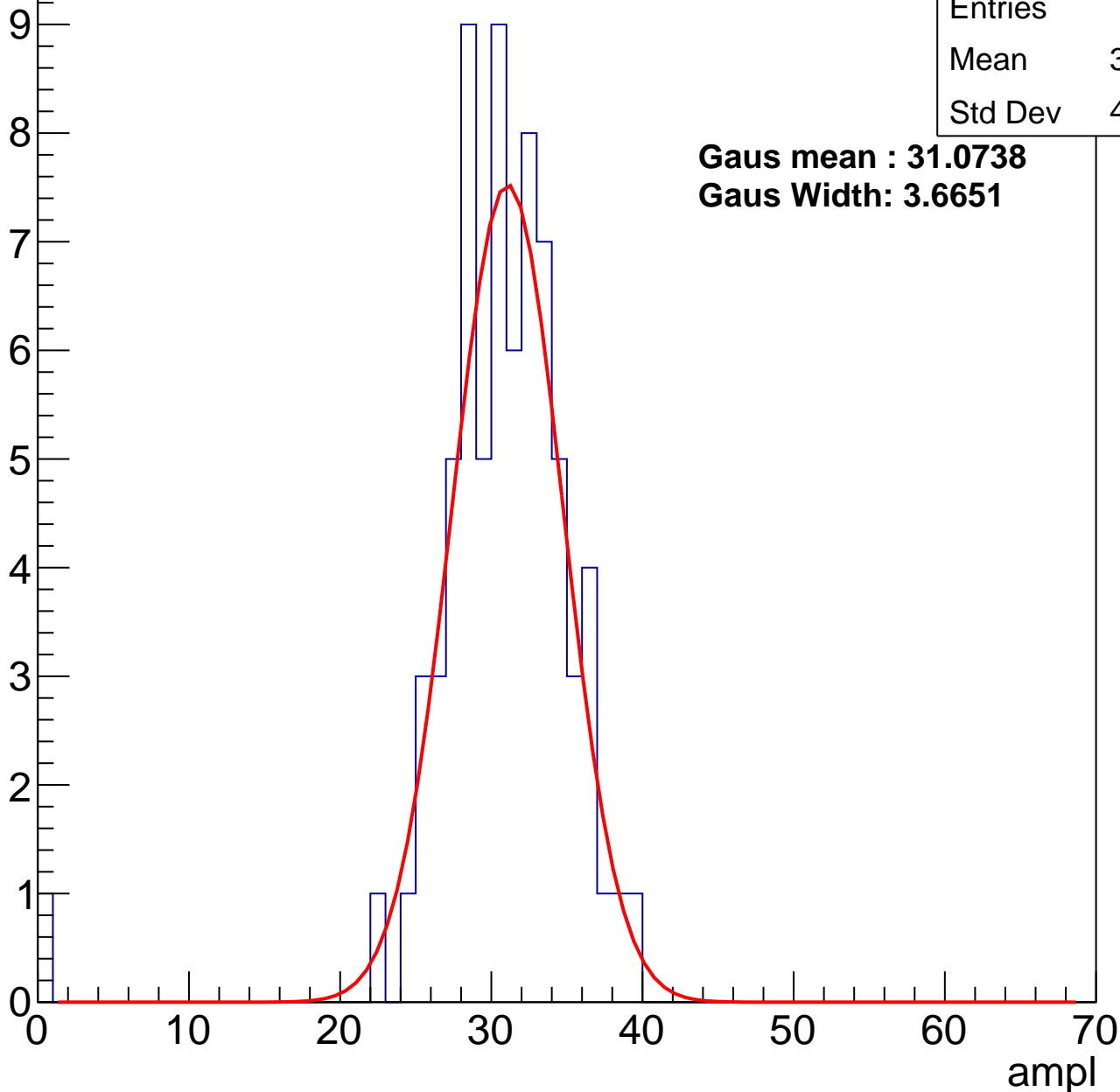
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	30.23
Std Dev	4.964

**Gaus mean : 31.0738**

**Gaus Width: 3.6651**



# B0L001S, U10-ch68, adc1

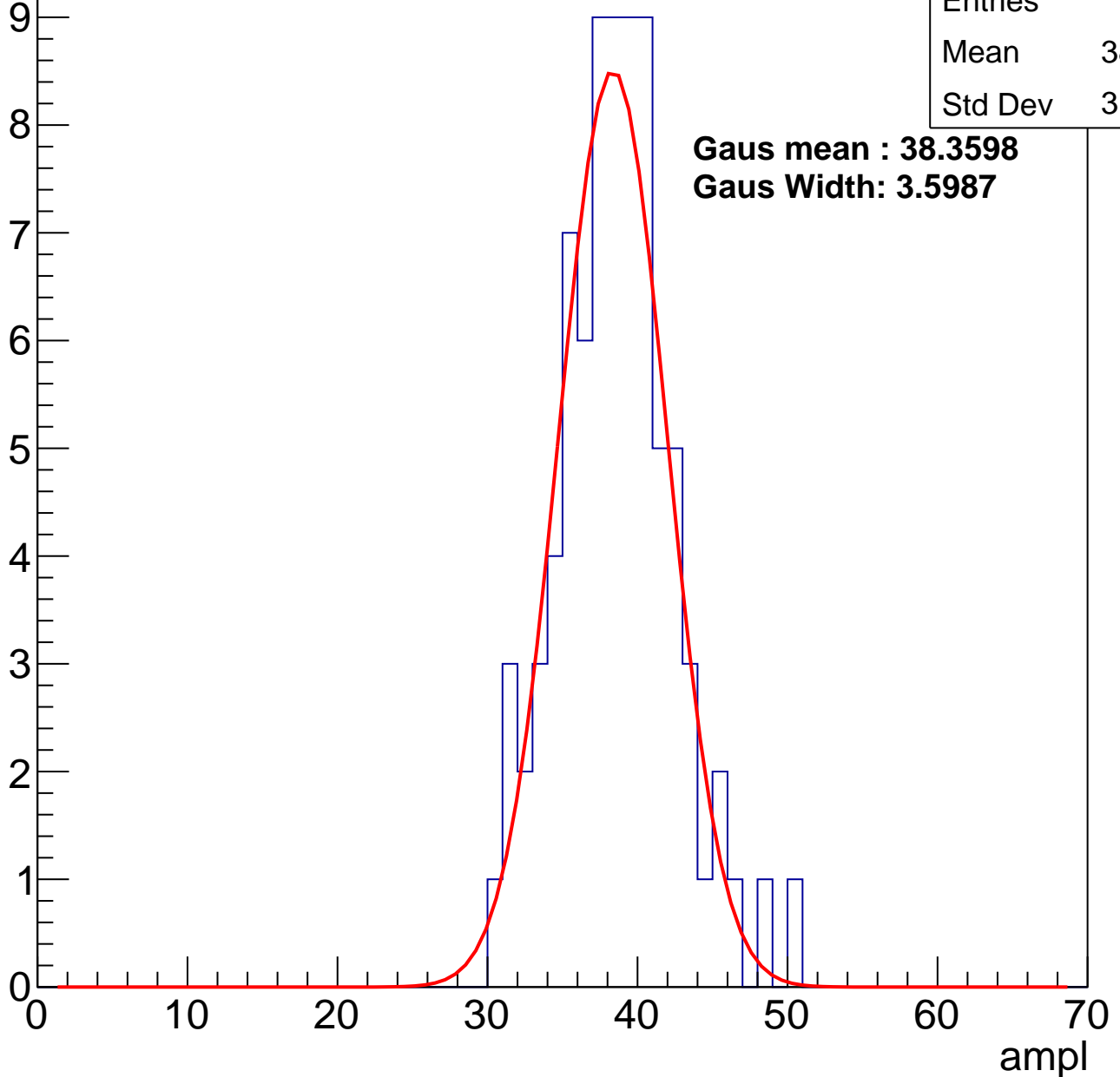
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	81
Mean	38.16
Std Dev	3.854

**Gaus mean : 38.3598**

**Gaus Width: 3.5987**



# B0L001S, U10-ch68, adc2

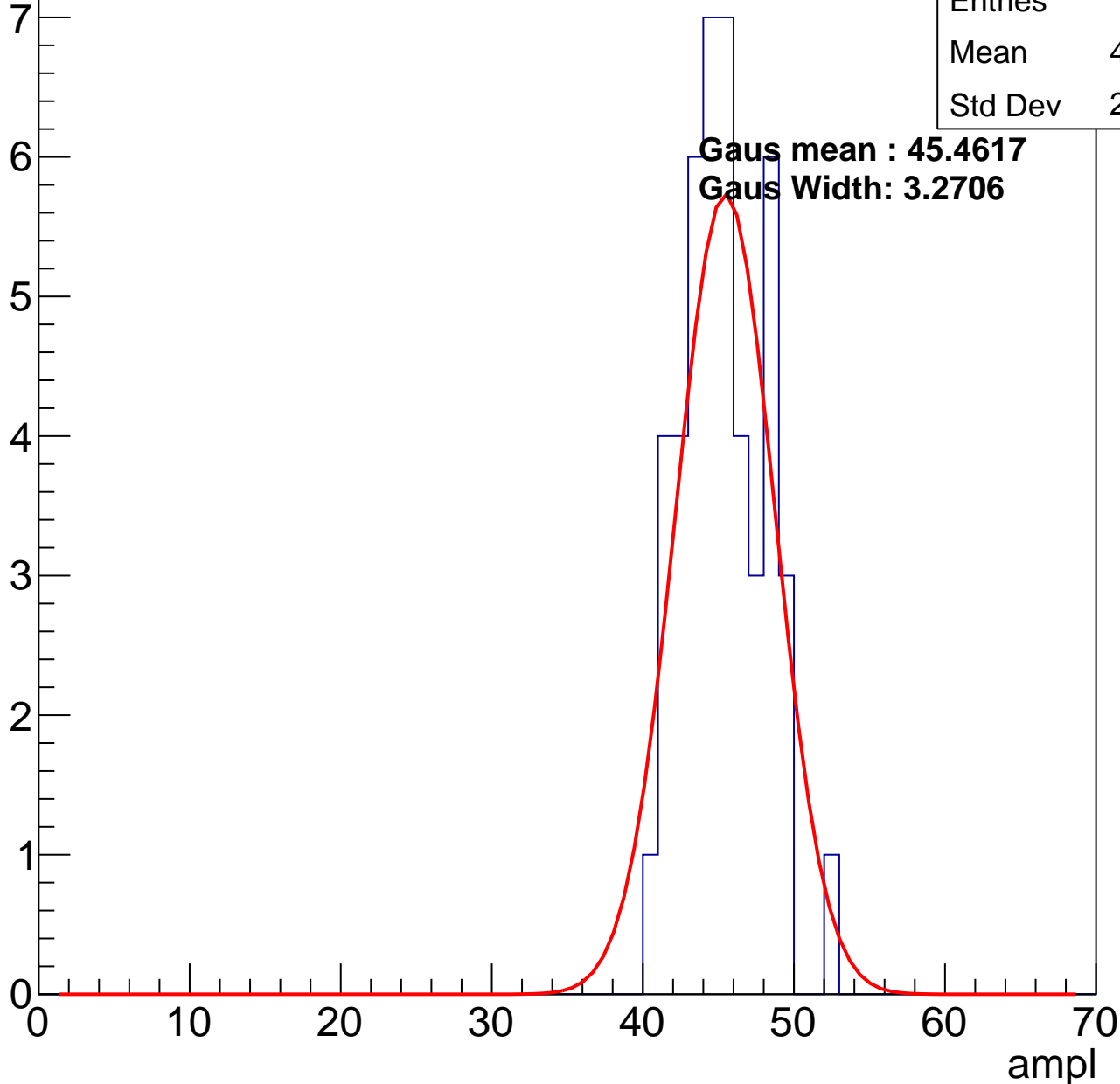
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	46
Mean	44.89
Std Dev	2.648

**Gaus mean : 45.4617**

**Gaus Width: 3.2706**

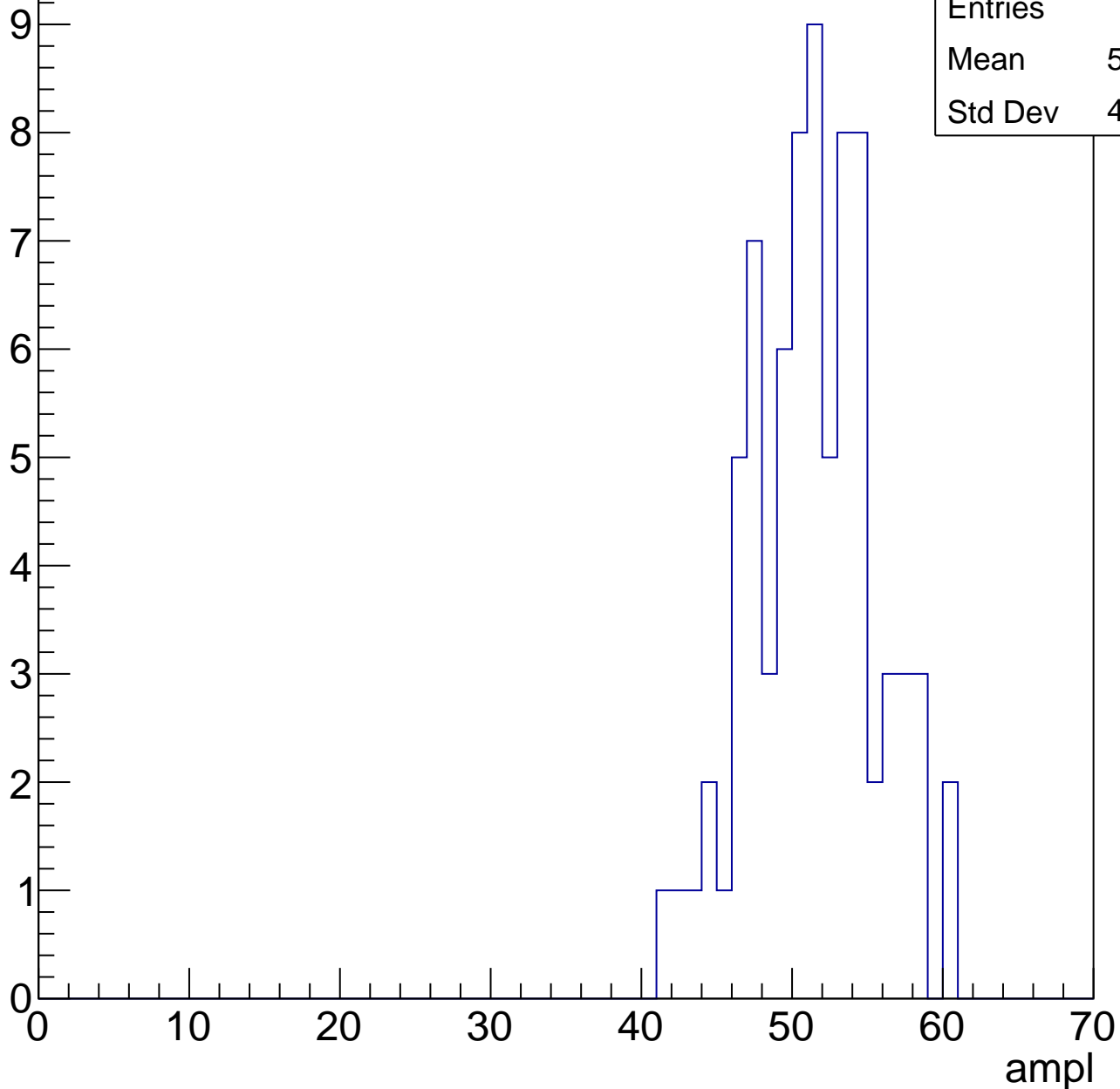


# B0L001S, U10-ch68, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

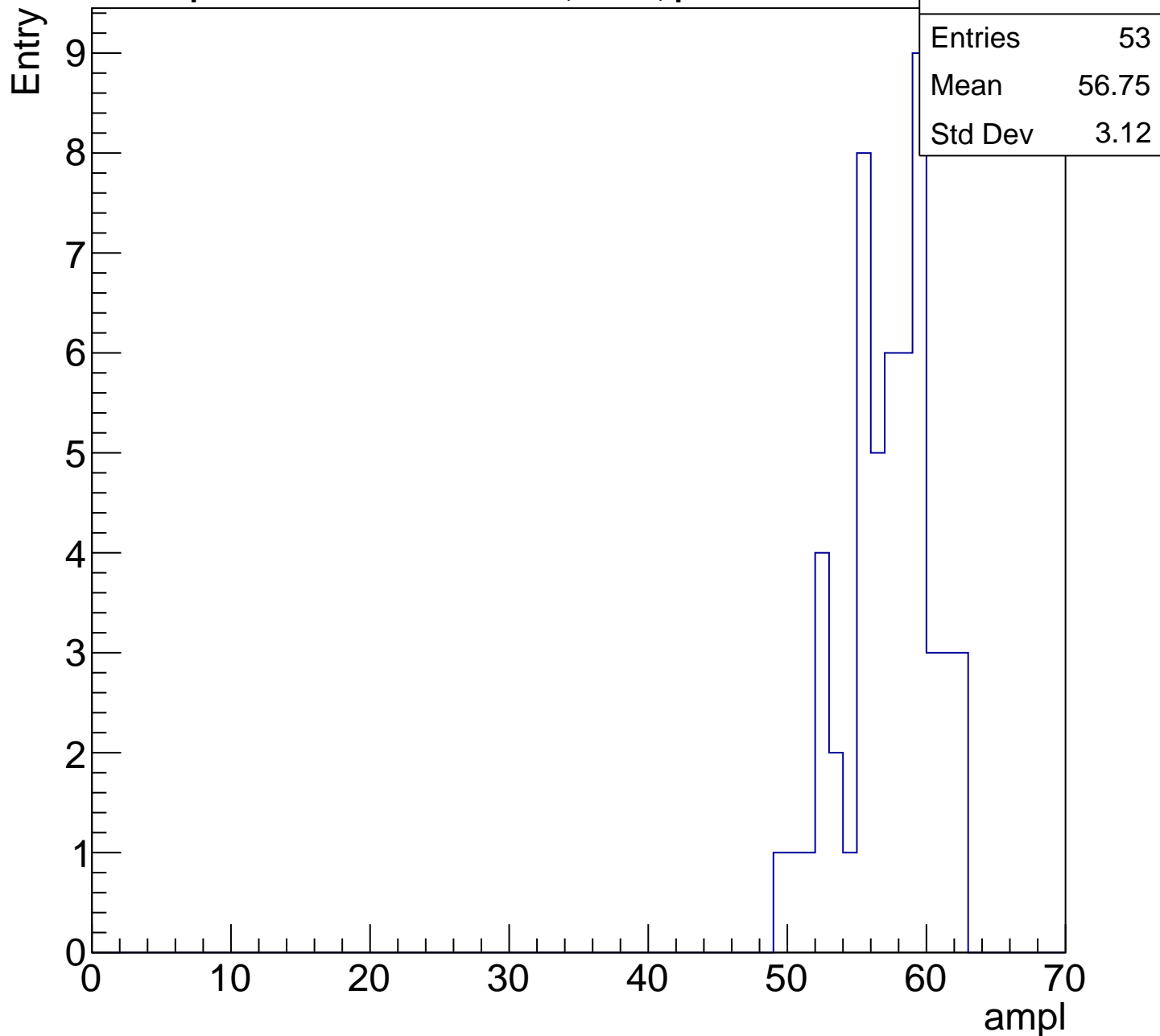
Entry

Entries	78
Mean	50.95
Std Dev	4.095



# B0L001S, U10-ch68, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

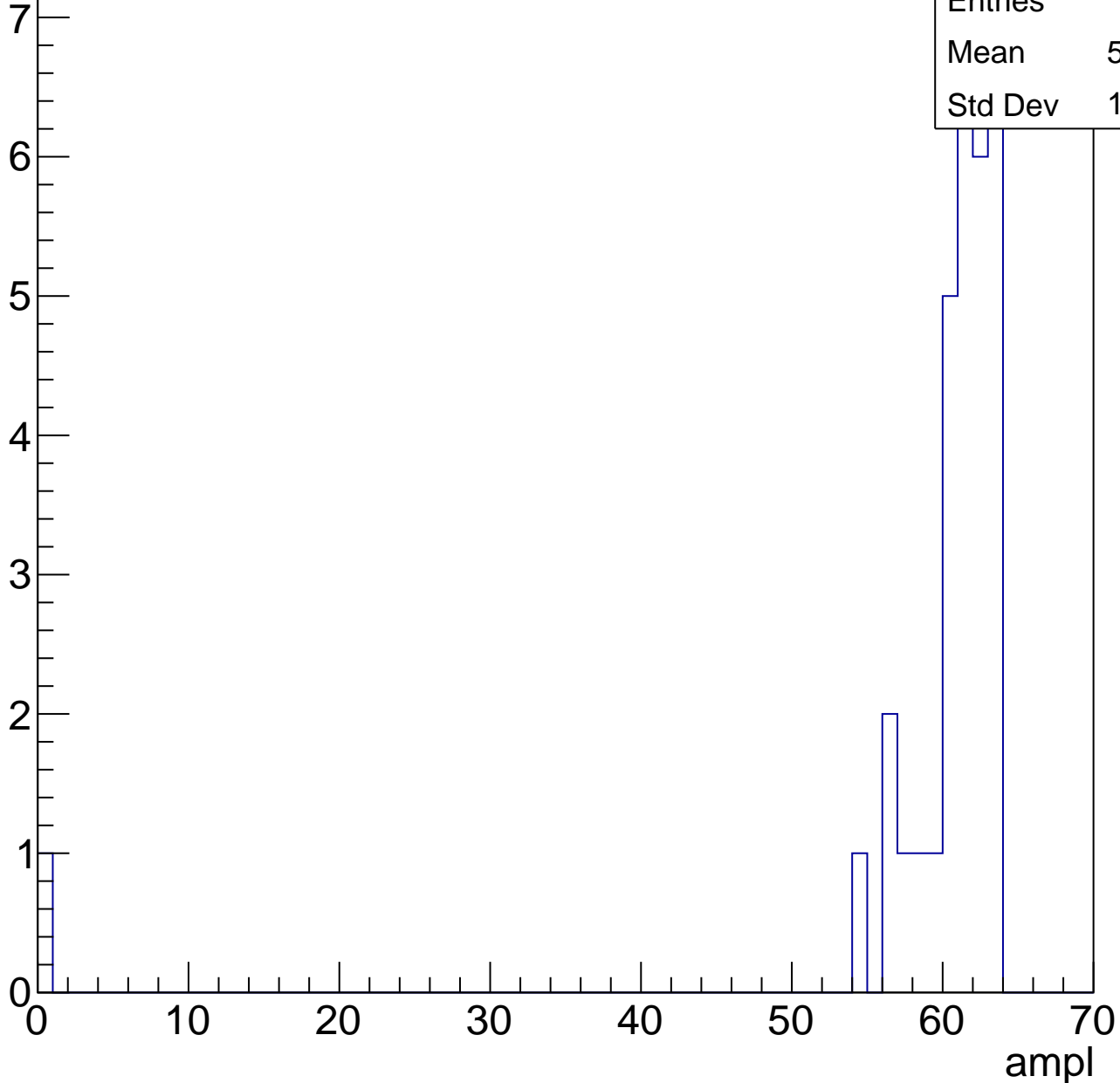


# B0L001S, U10-ch68, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	32
Mean	58.75
Std Dev	10.79



# B0L001S, U10-ch68, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	4
Mean	62.75
Std Dev	0.433



# B0L001S, U10-ch68, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U10-ch69, adc0

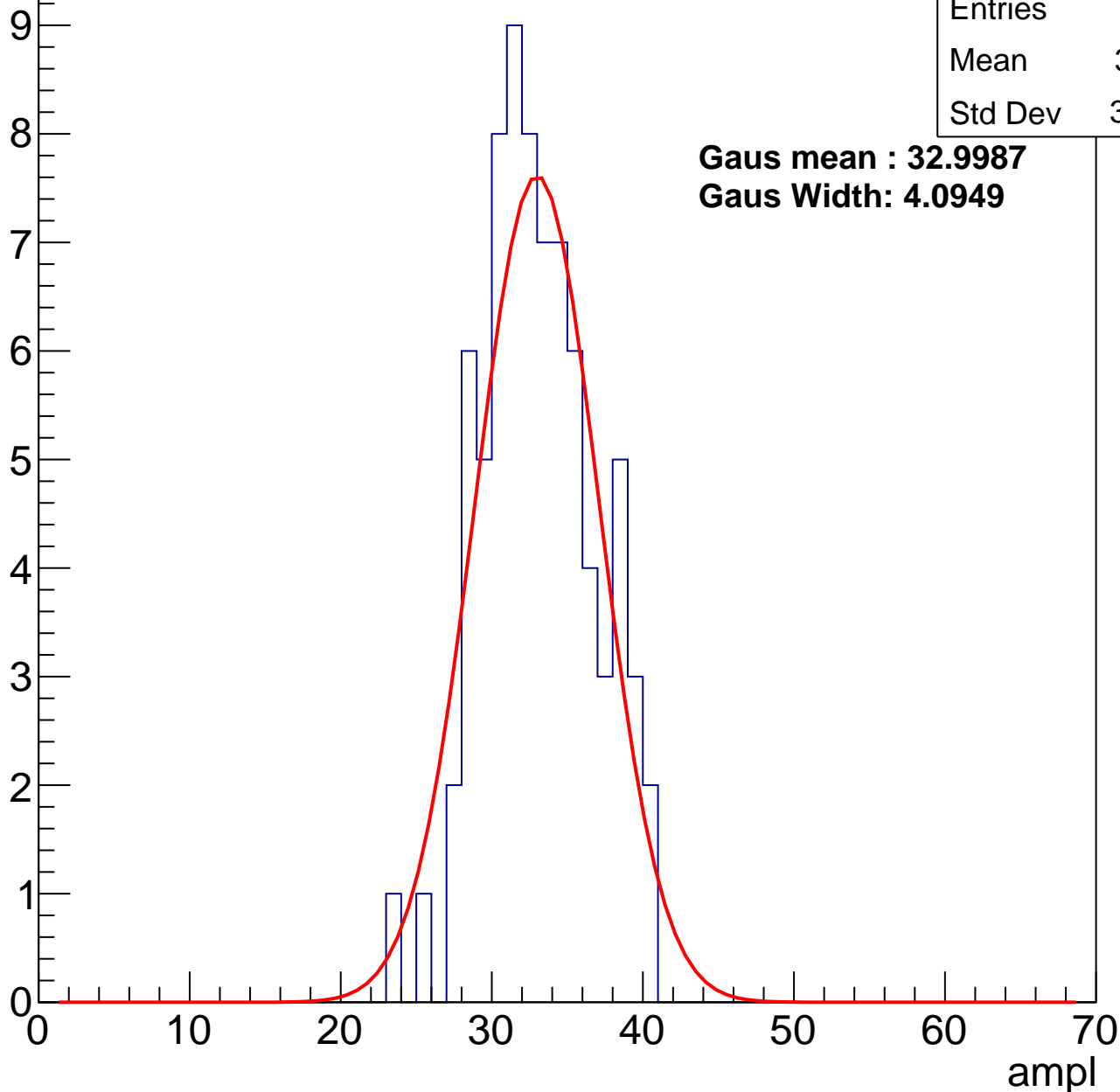
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	77
Mean	32.61
Std Dev	3.633

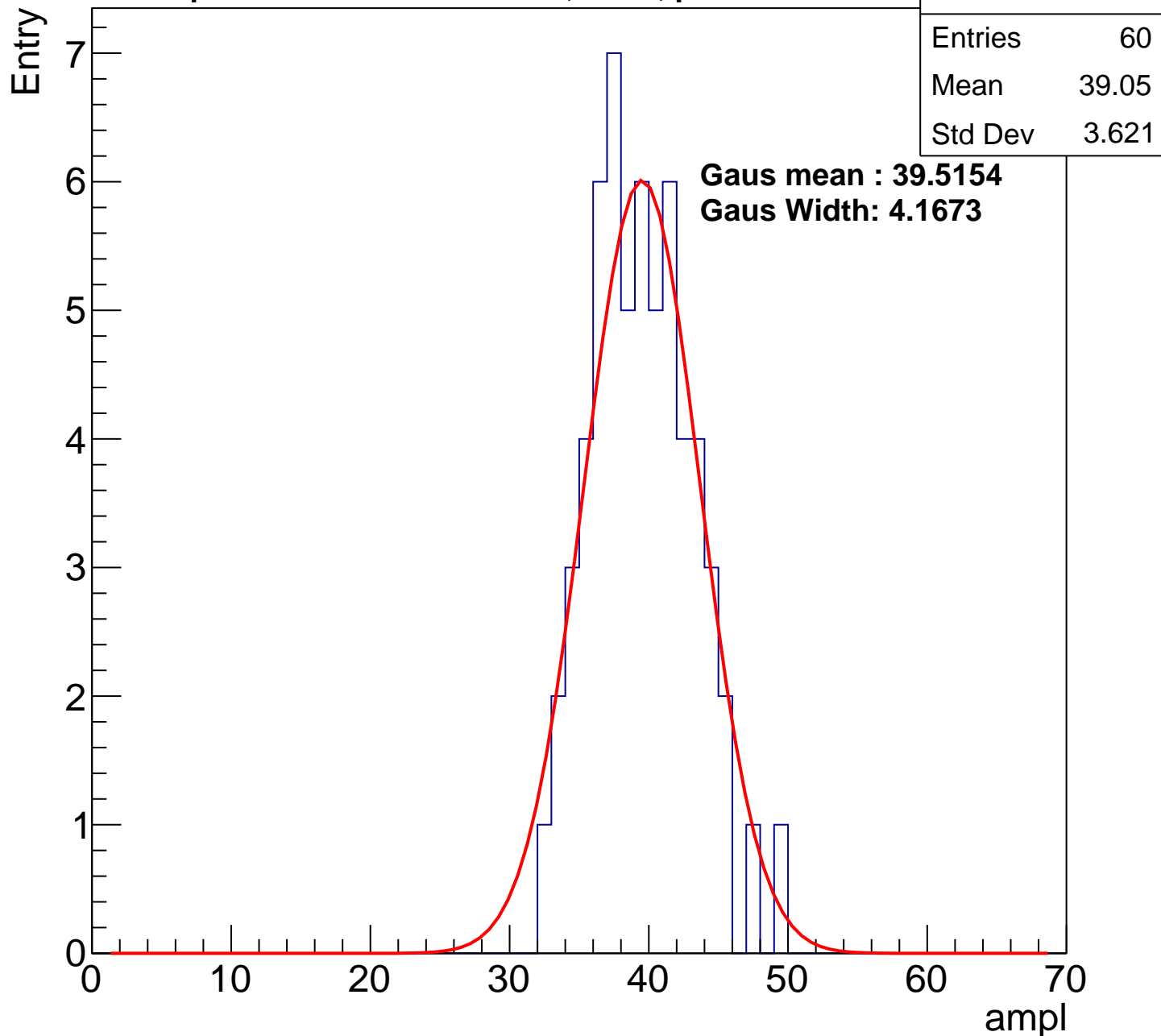
**Gaus mean : 32.9987**

**Gaus Width: 4.0949**



# B0L001S, U10-ch69, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U10-ch69, adc2

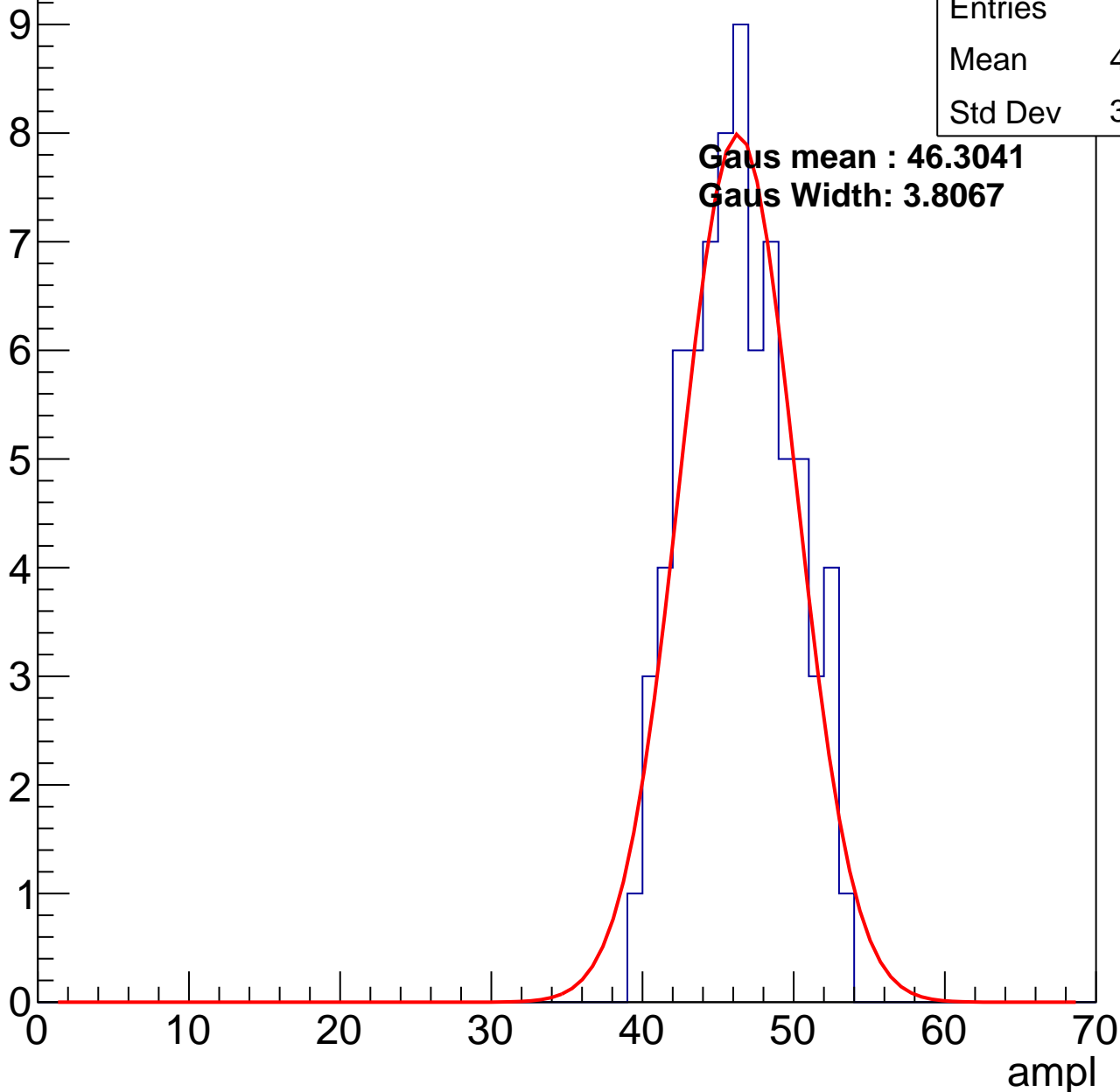
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	75
Mean	45.89
Std Dev	3.404

**Gaus mean : 46.3041**

**Gaus Width: 3.8067**

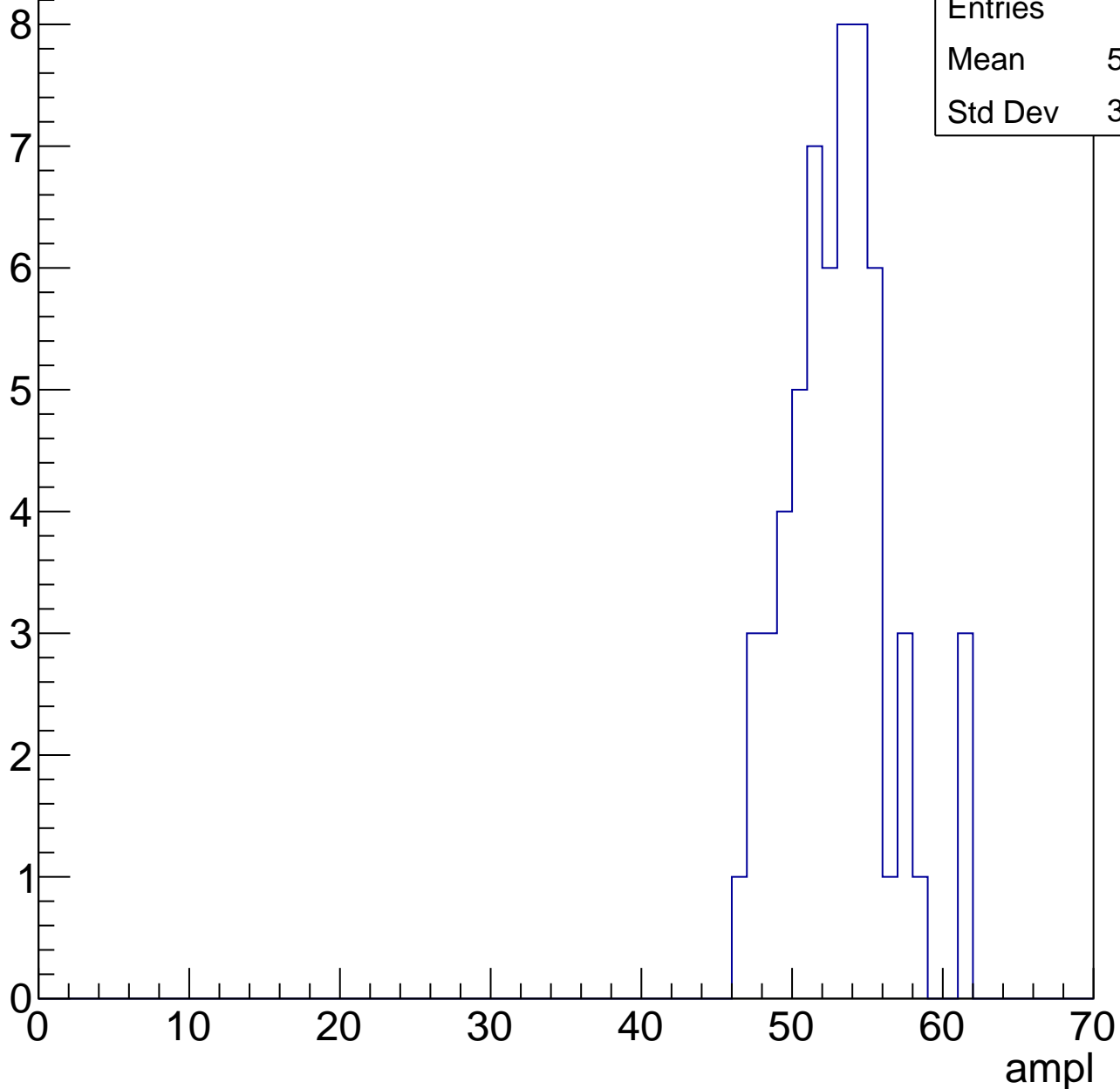


# B0L001S, U10-ch69, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

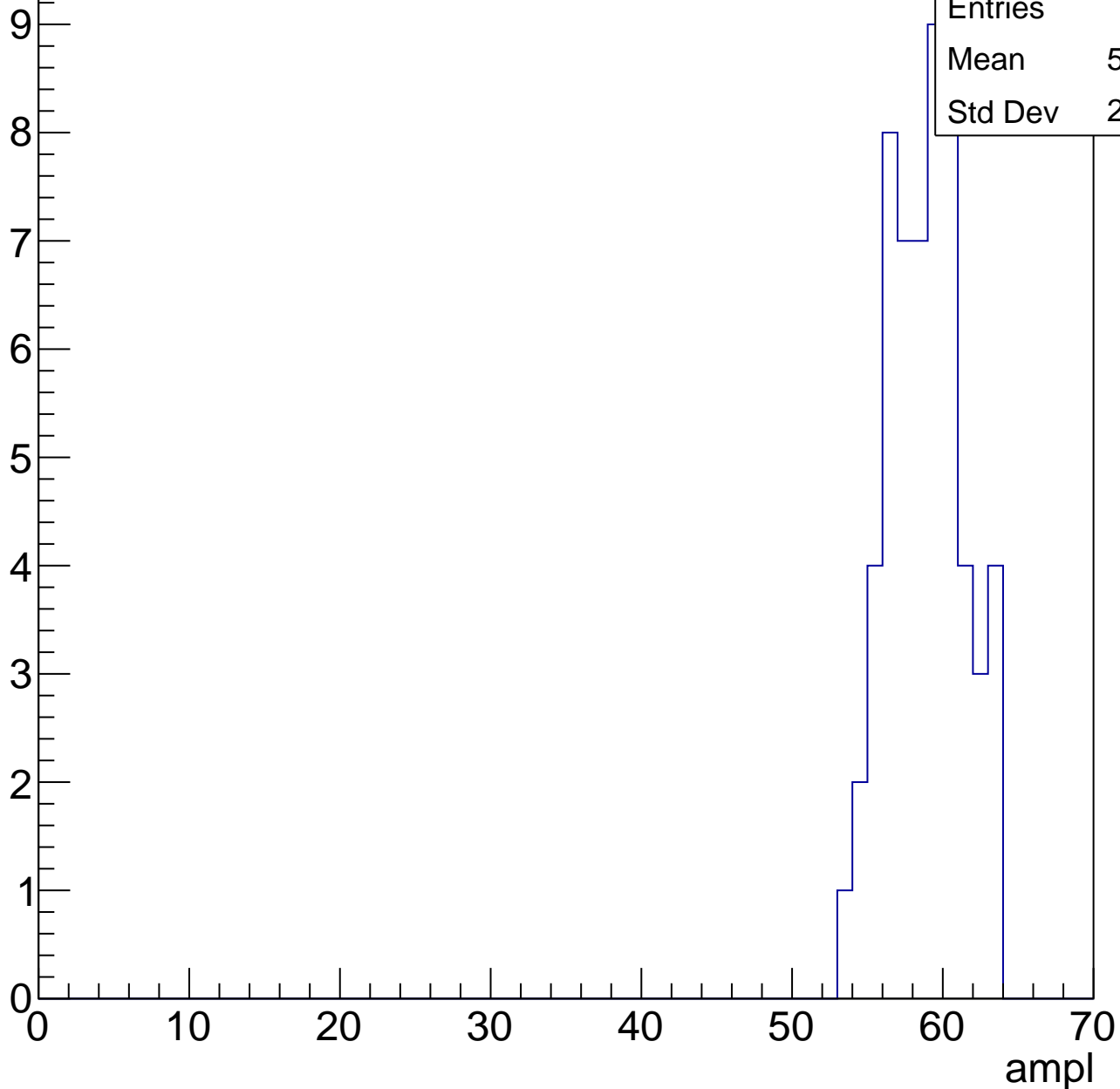
Entries	59
Mean	52.54
Std Dev	3.366



# B0L001S, U10-ch69, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

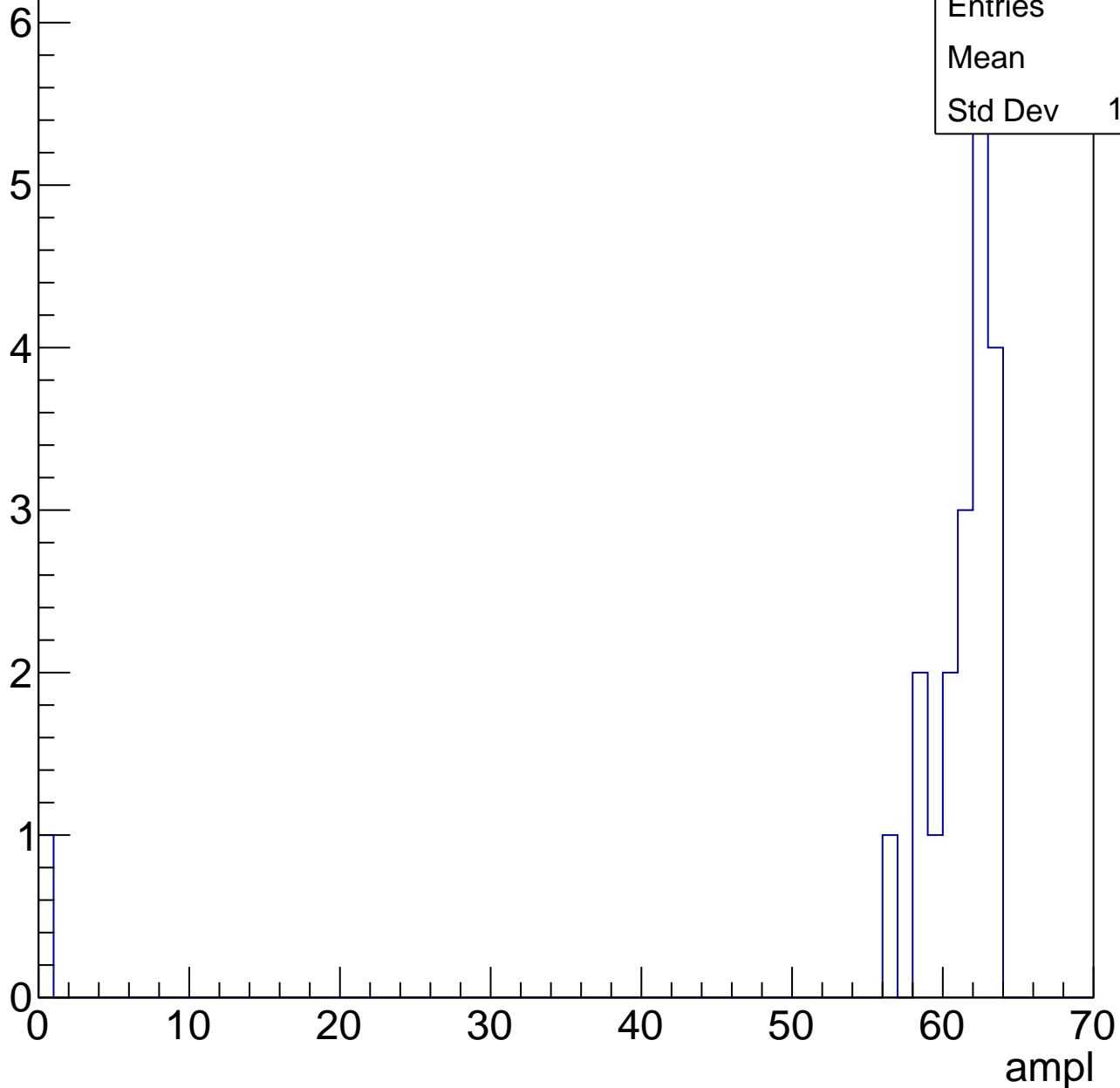


# B0L001S, U10-ch69, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	20
Mean	57.9
Std Dev	13.42



# B0L001S, U10-ch69, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch69, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U10-ch70, adc0

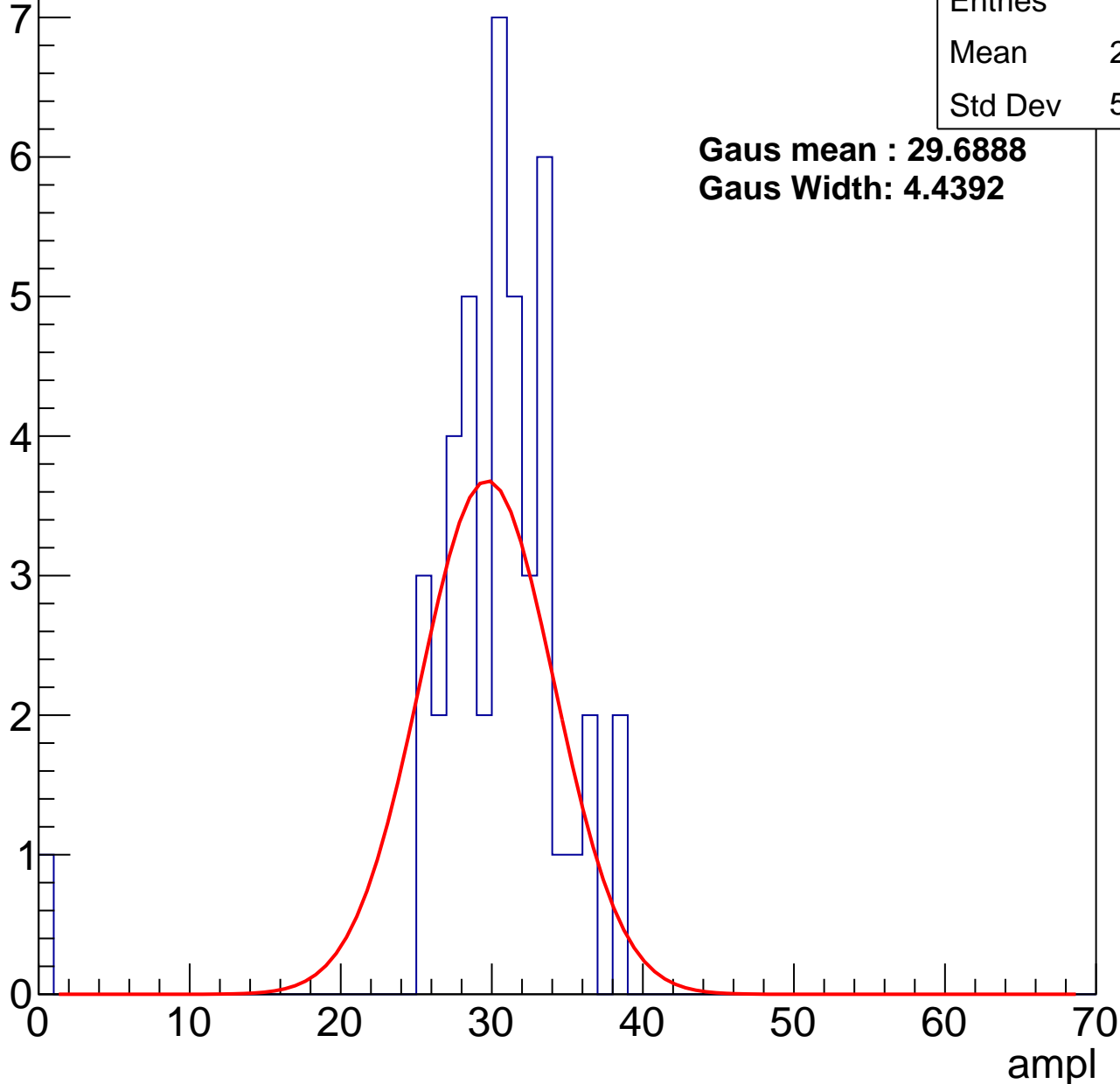
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	44
Mean	29.75
Std Dev	5.589

**Gaus mean : 29.6888**

**Gaus Width: 4.4392**



# B0L001S, U10-ch70, adc1

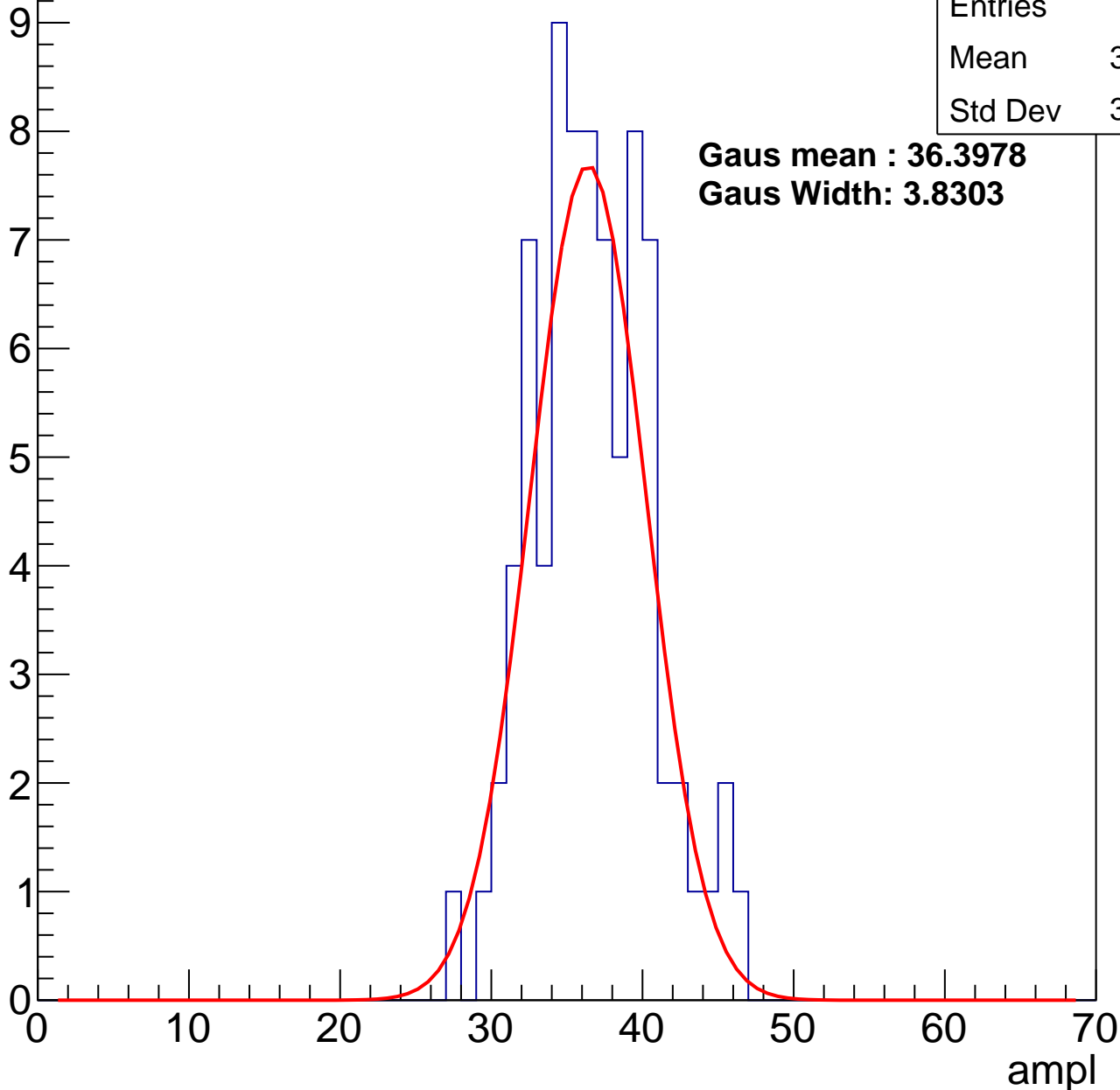
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	80
Mean	36.25
Std Dev	3.868

**Gaus mean : 36.3978**

**Gaus Width: 3.8303**



# B0L001S, U10-ch70, adc2

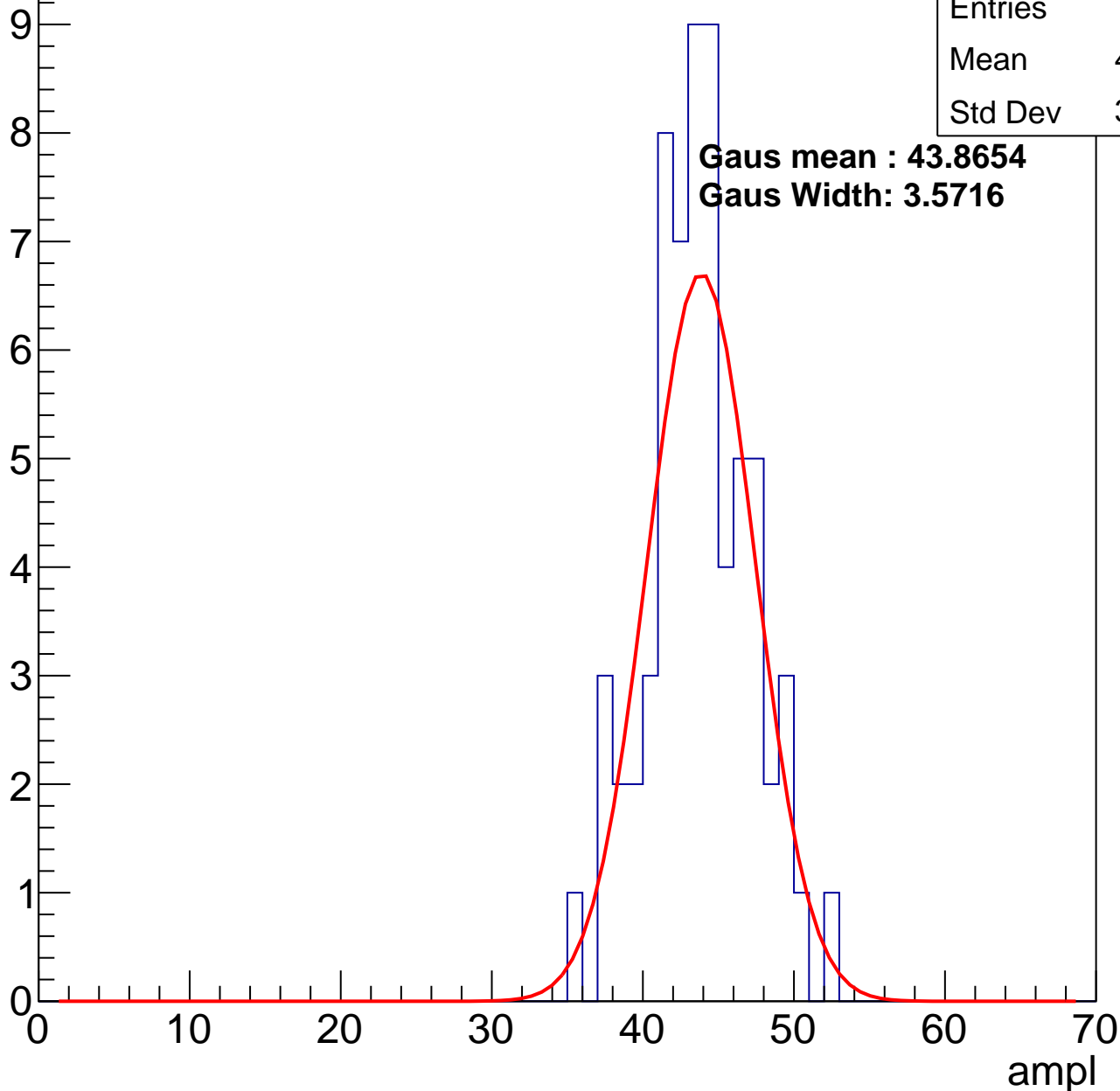
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	43.31
Std Dev	3.401

**Gaus mean : 43.8654**

**Gaus Width: 3.5716**

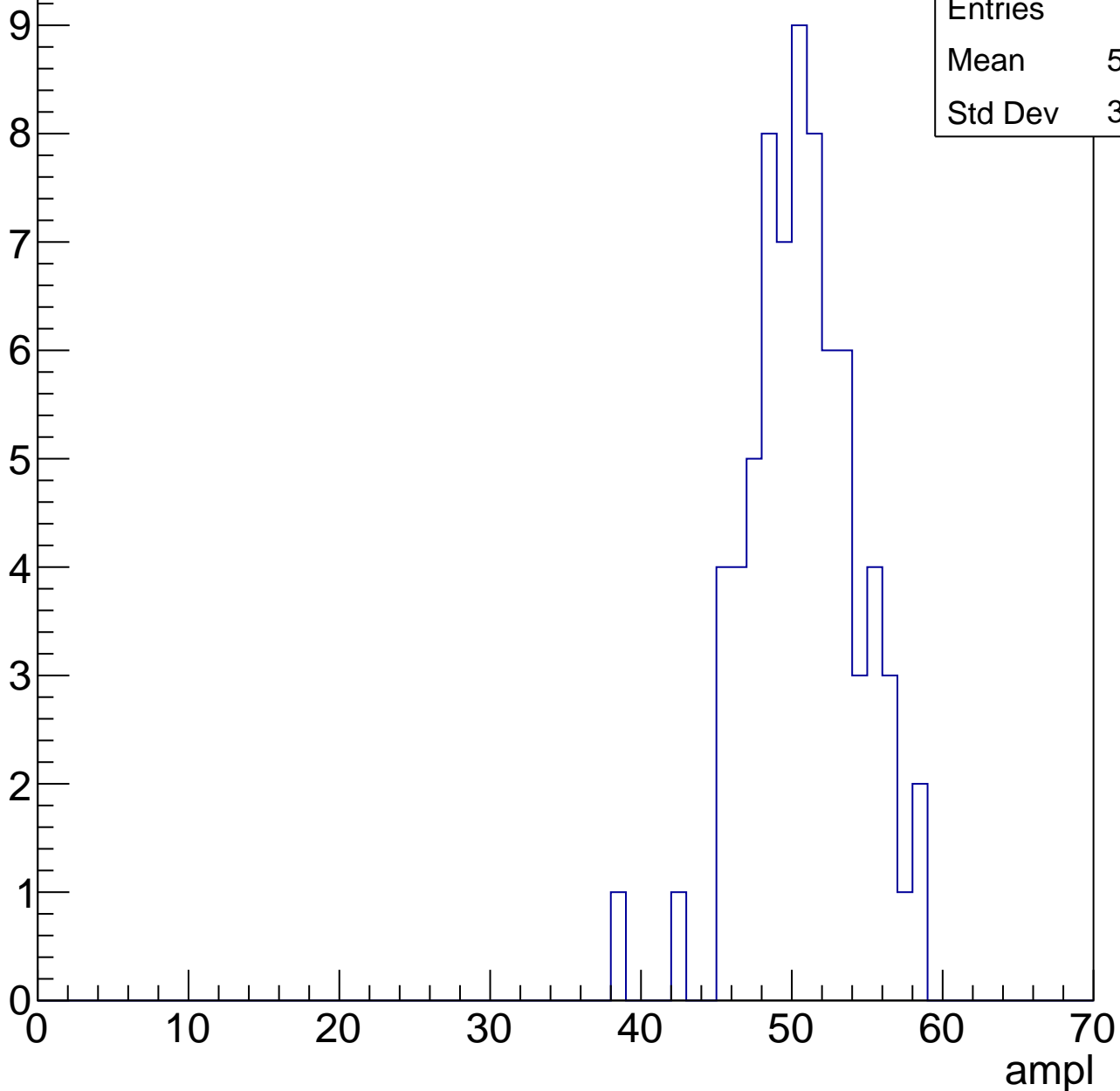


# B0L001S, U10-ch70, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	50.24
Std Dev	3.672



# B0L001S, U10-ch70, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

6

5

4

3

2

1

0

Entries 54

Mean 56.69

Std Dev 3.072

0

10

20

30

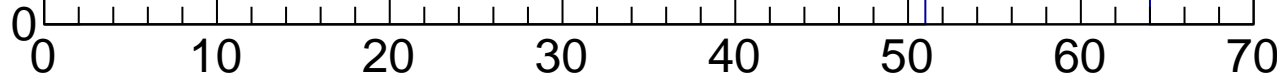
40

50

60

70

ampl

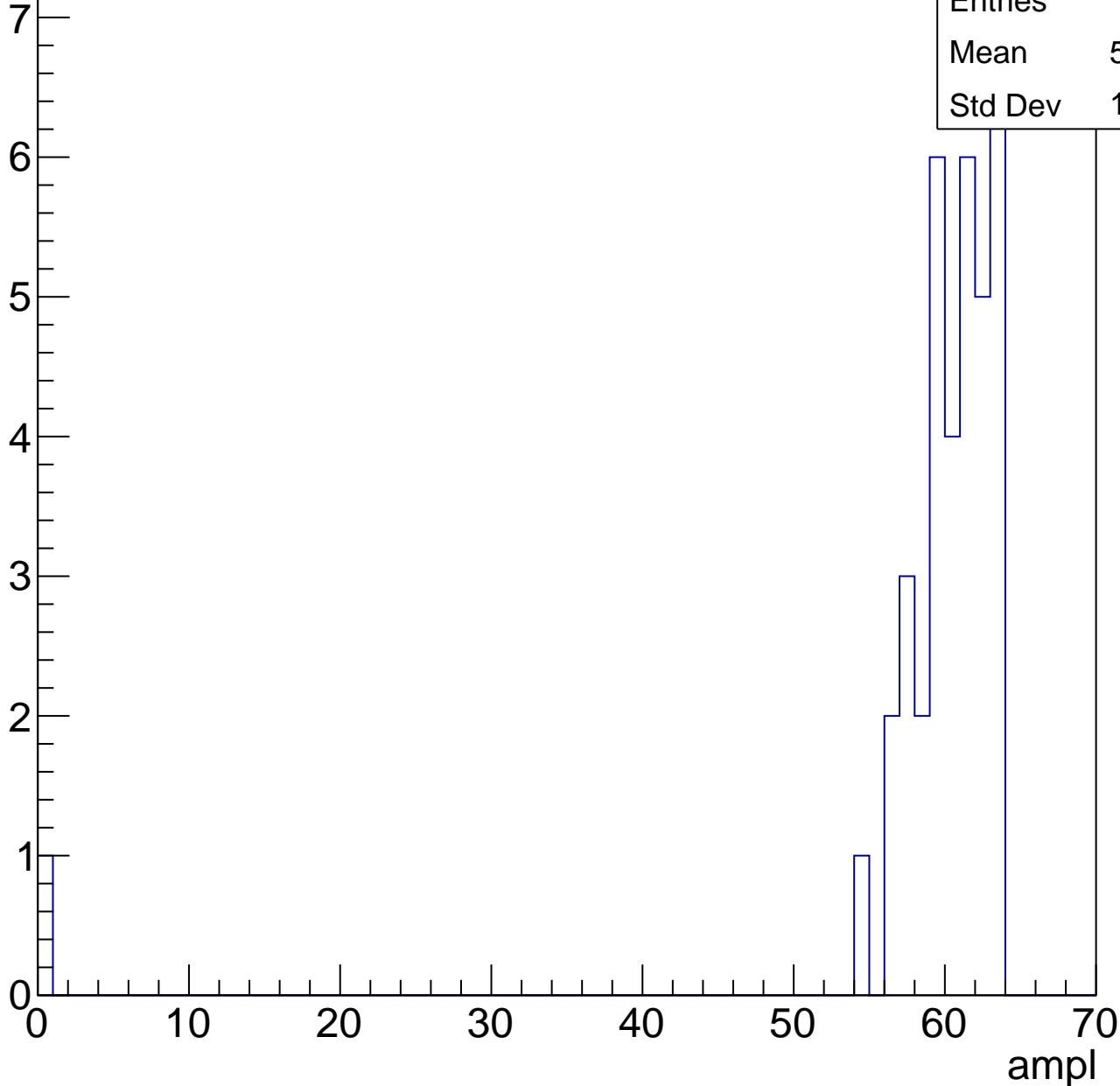


# B0L001S, U10-ch70, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

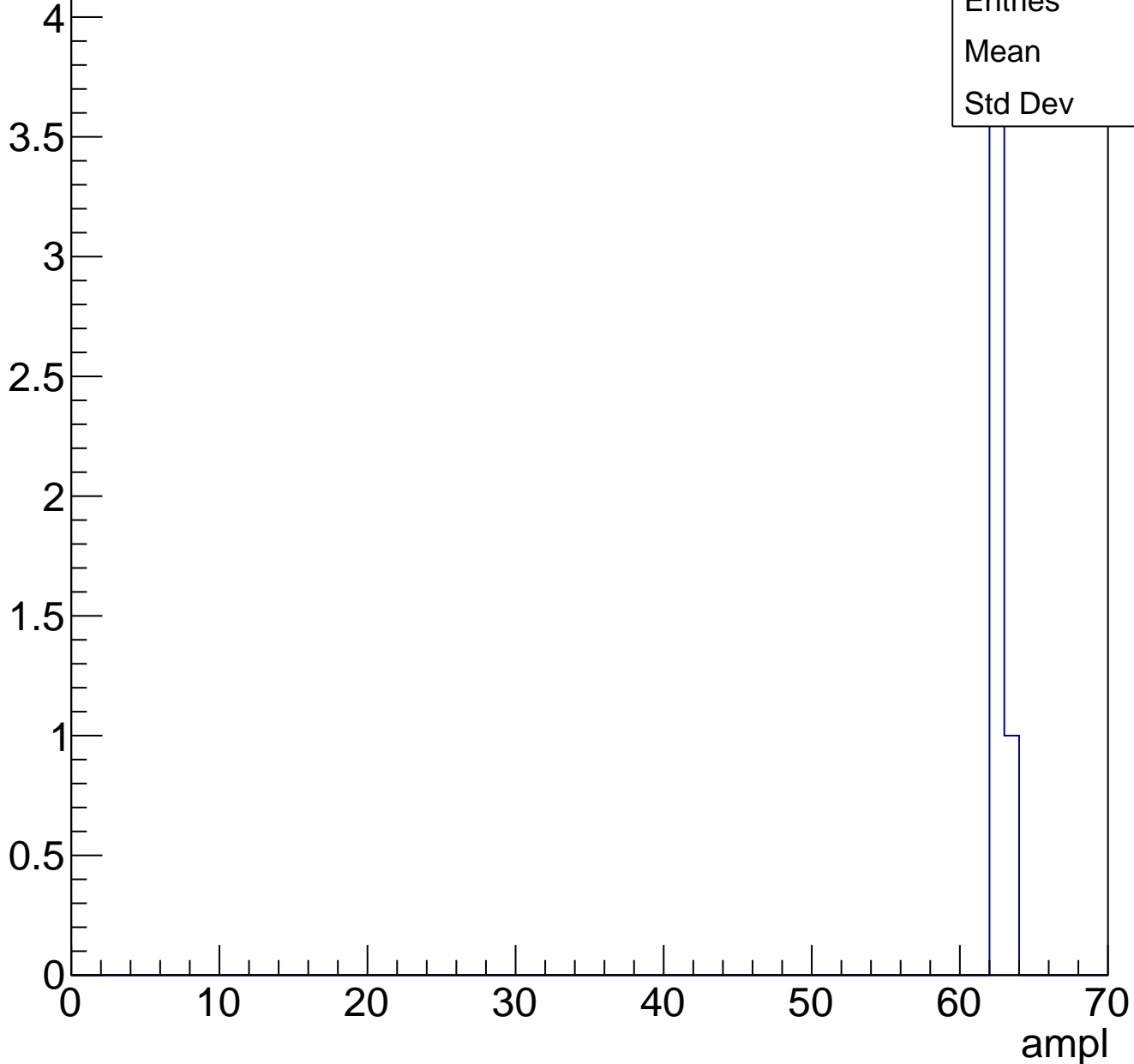
Entries	37
Mean	58.49
Std Dev	10.02



# B0L001S, U10-ch70, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

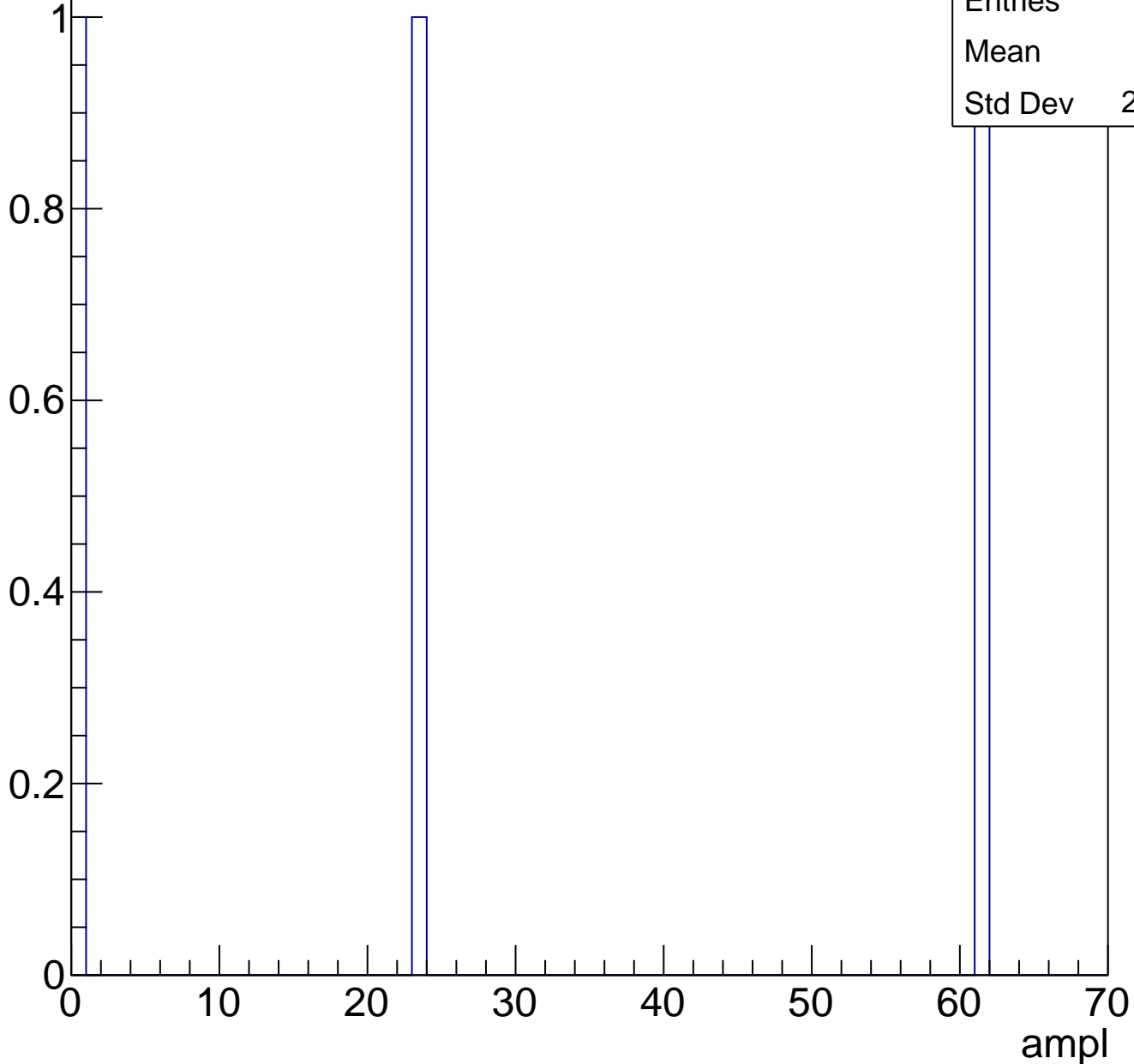




# B0L001S, U10-ch70, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	3
Mean	28
Std Dev	25.15

# B0L001S, U10-ch71, adc0

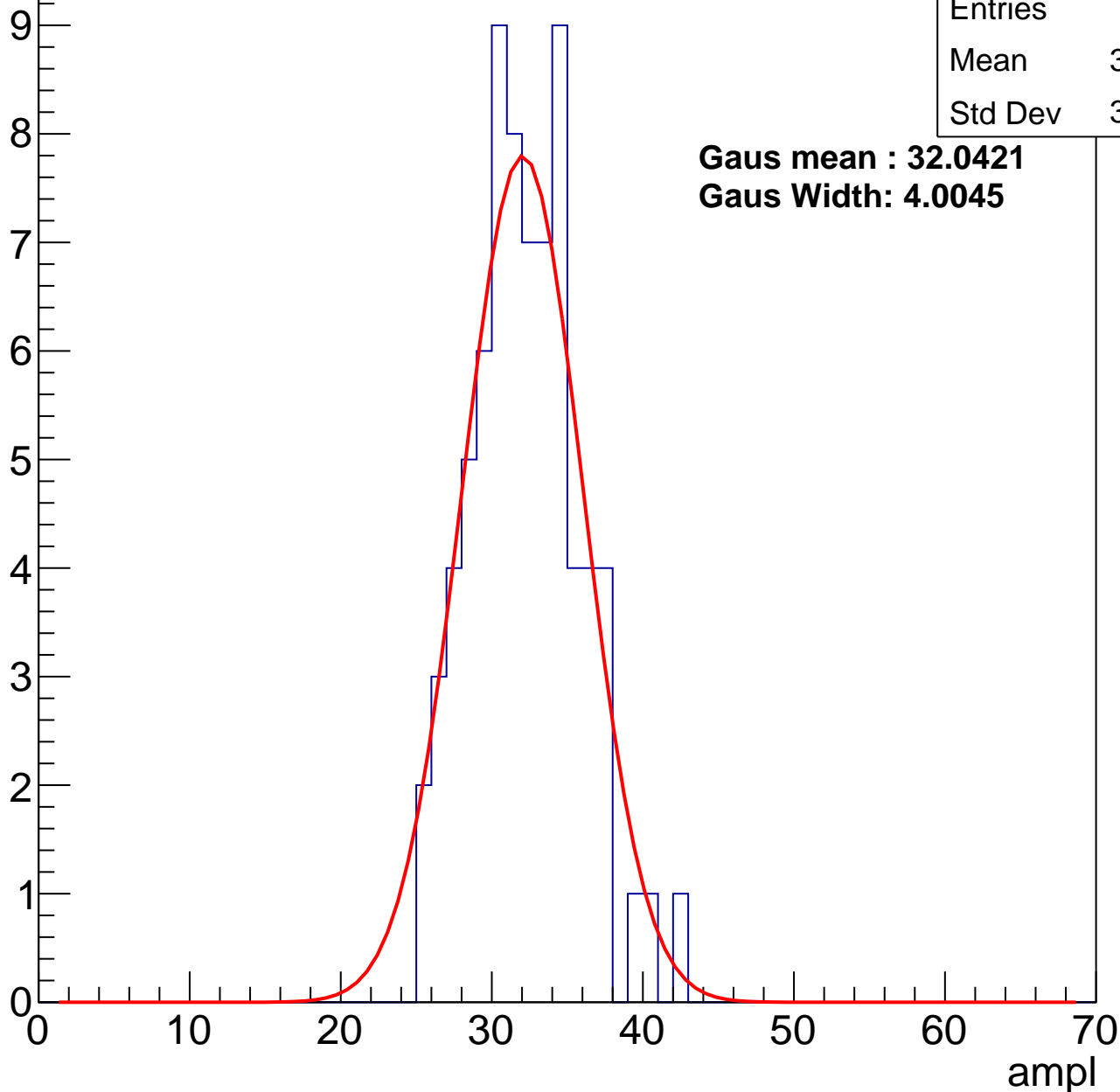
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	75
Mean	31.76
Std Dev	3.532

**Gaus mean : 32.0421**

**Gaus Width: 4.0045**



# B0L001S, U10-ch71, adc1

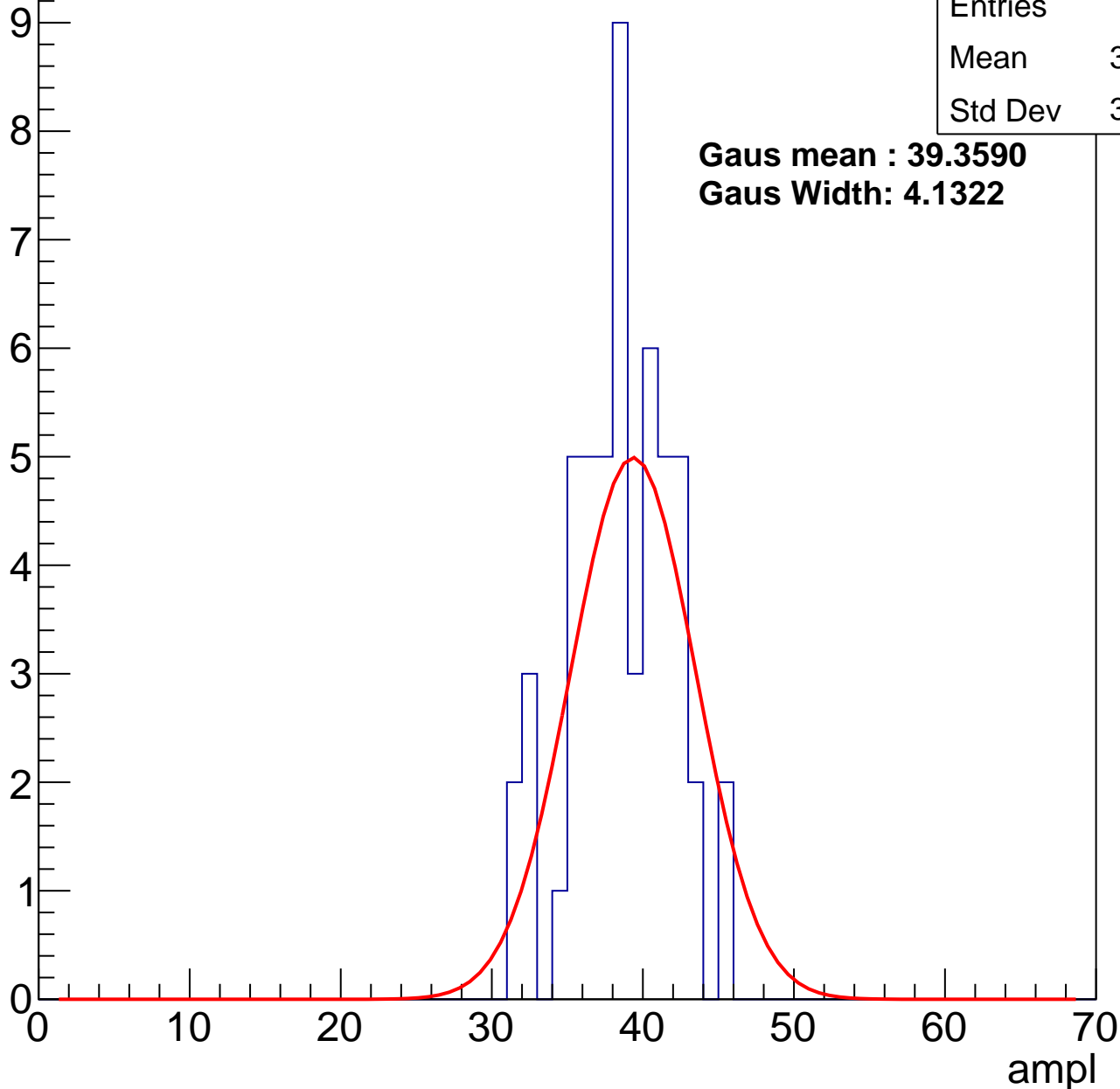
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	38.15
Std Dev	3.339

**Gaus mean : 39.3590**

**Gaus Width: 4.1322**



# B0L001S, U10-ch71, adc2

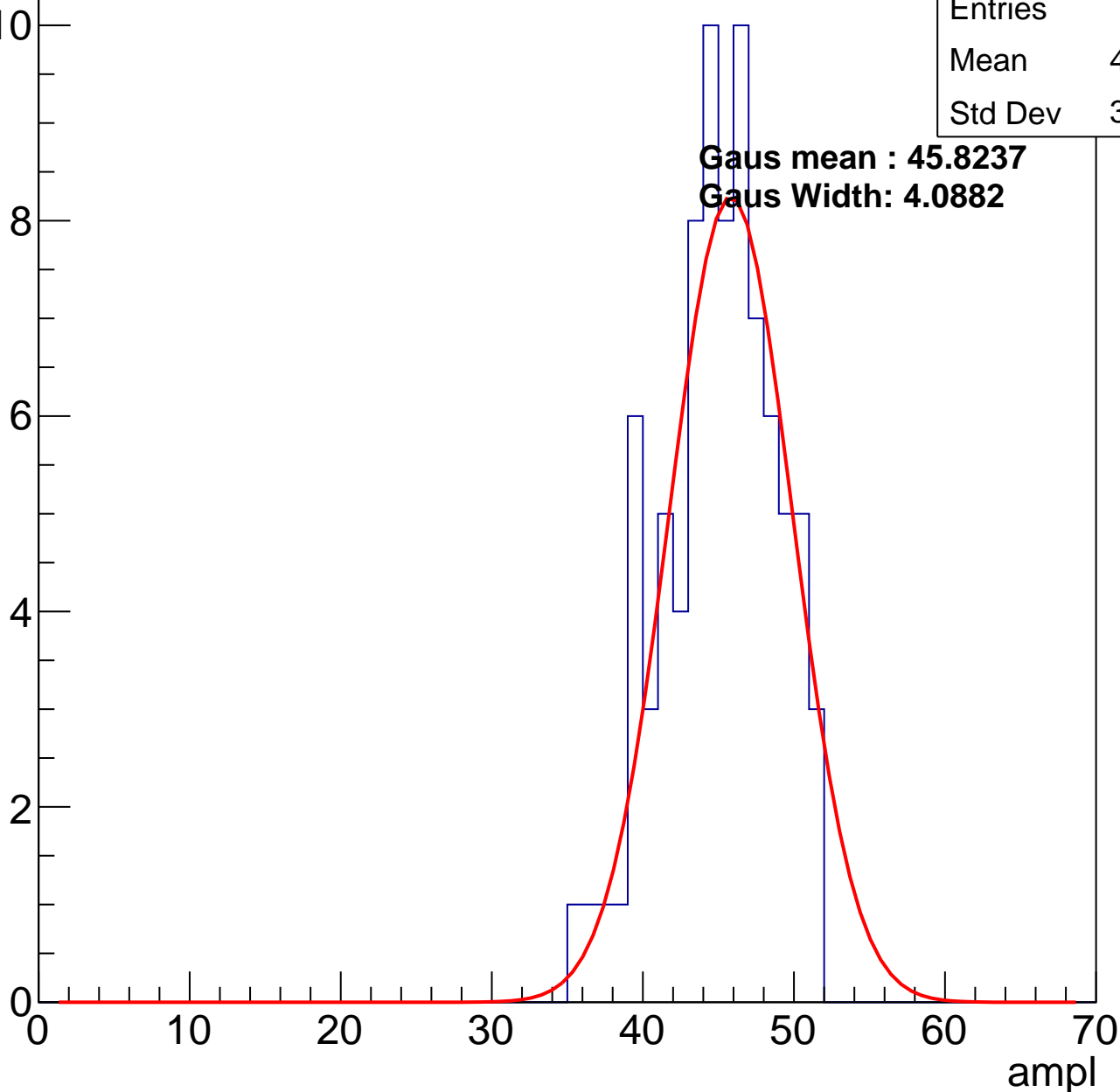
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	84
Mean	44.55
Std Dev	3.669

**Gaus mean : 45.8237**

**Gaus Width: 4.0882**

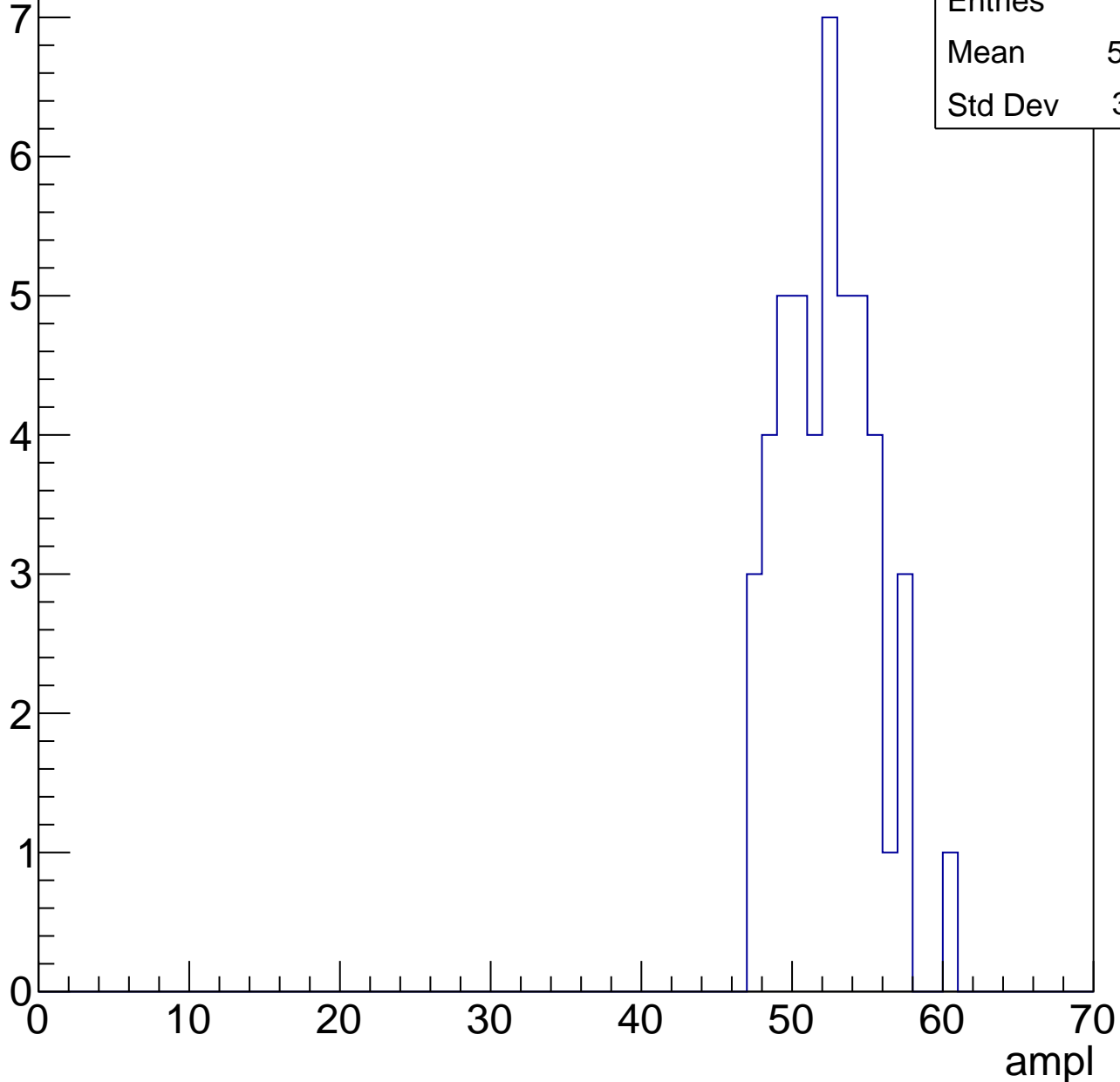


# B0L001S, U10-ch71, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

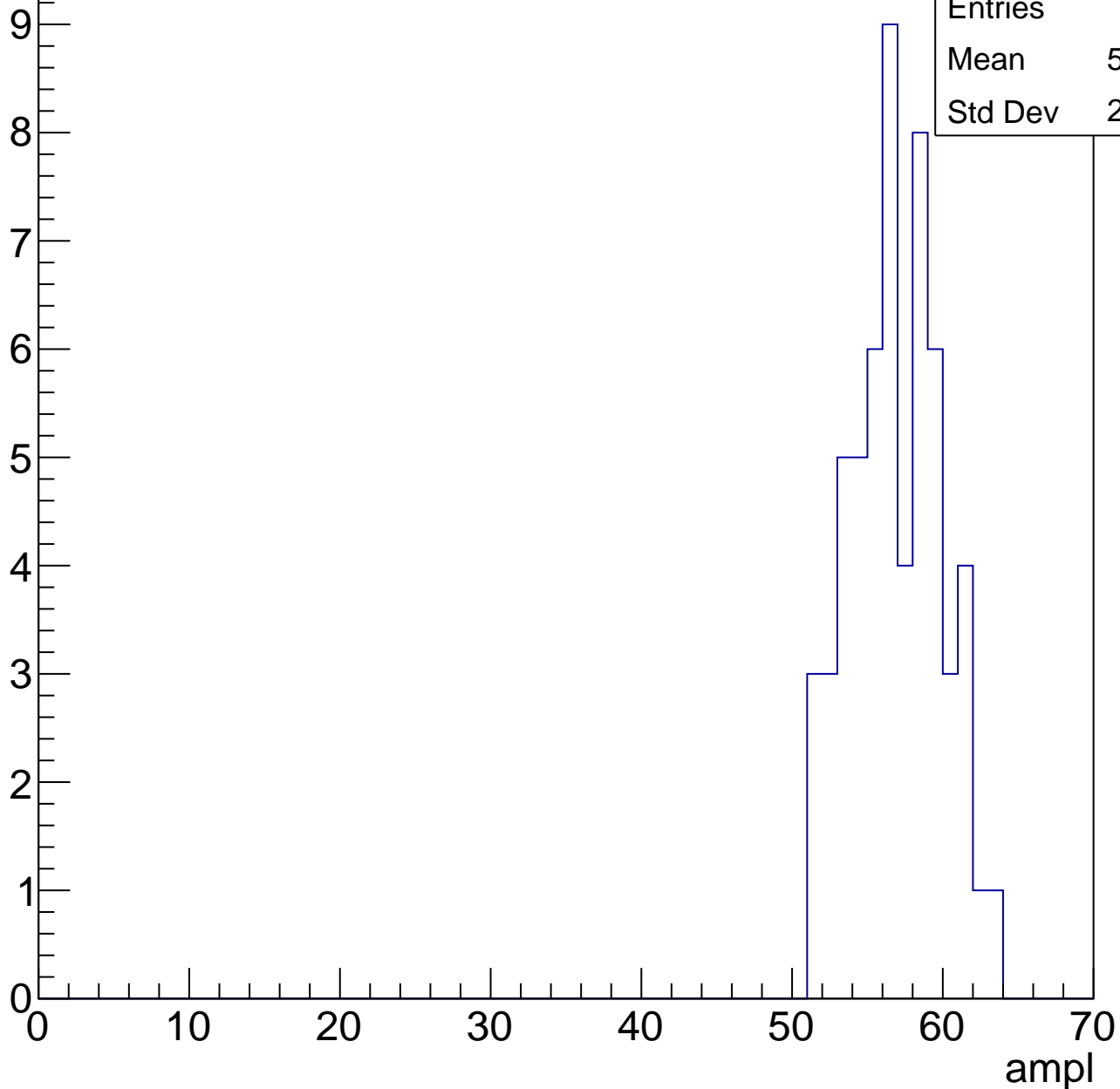
Entries	47
Mean	51.87
Std Dev	3.001



# B0L001S, U10-ch71, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

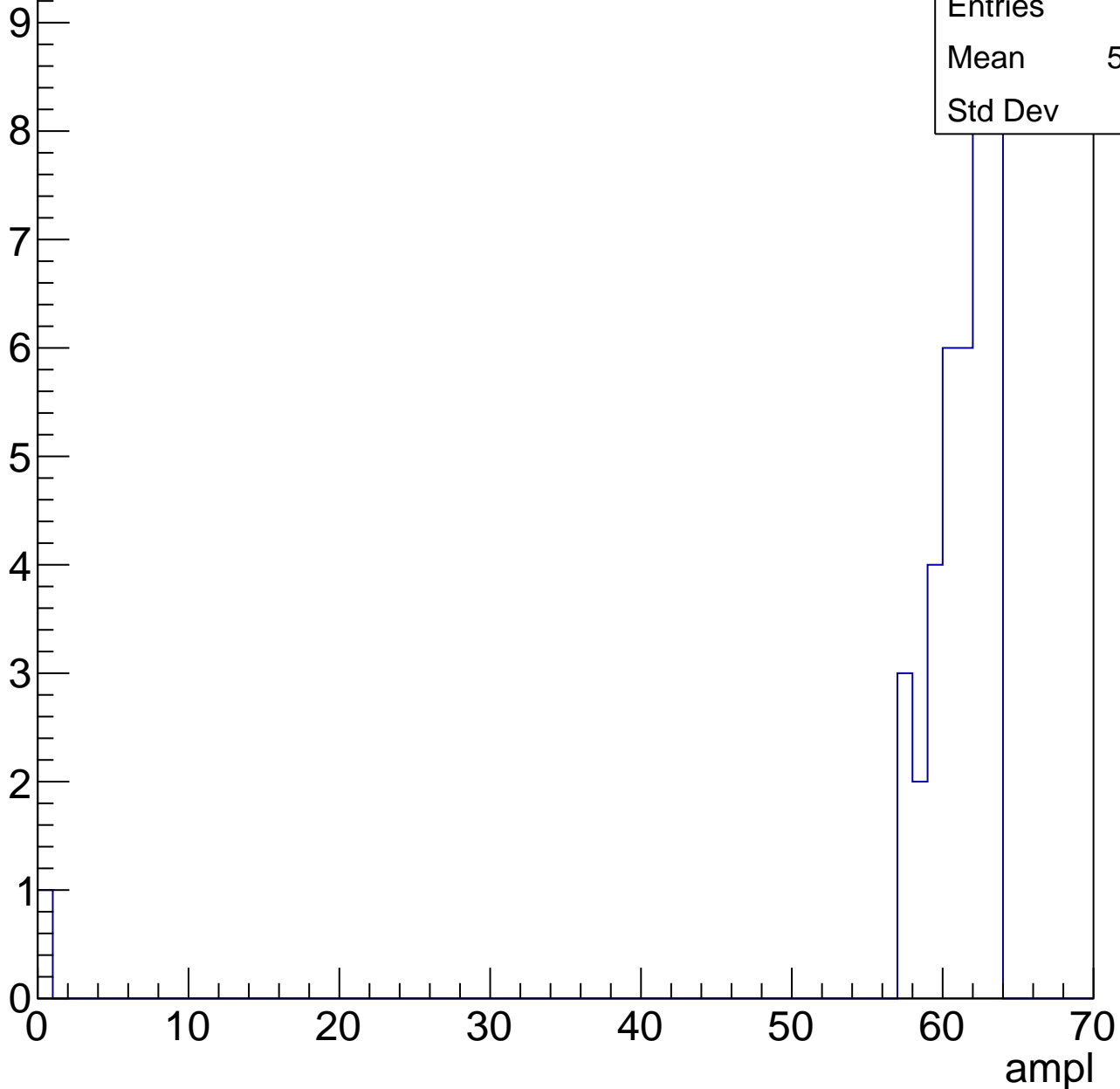


# B0L001S, U10-ch71, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	39
Mean	59.28
Std Dev	9.79



# B0L001S, U10-ch71, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	62
Std Dev	0



# B0L001S, U10-ch71, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	3
Mean	0
Std Dev	0

# B0L001S, U10-ch72, adc0

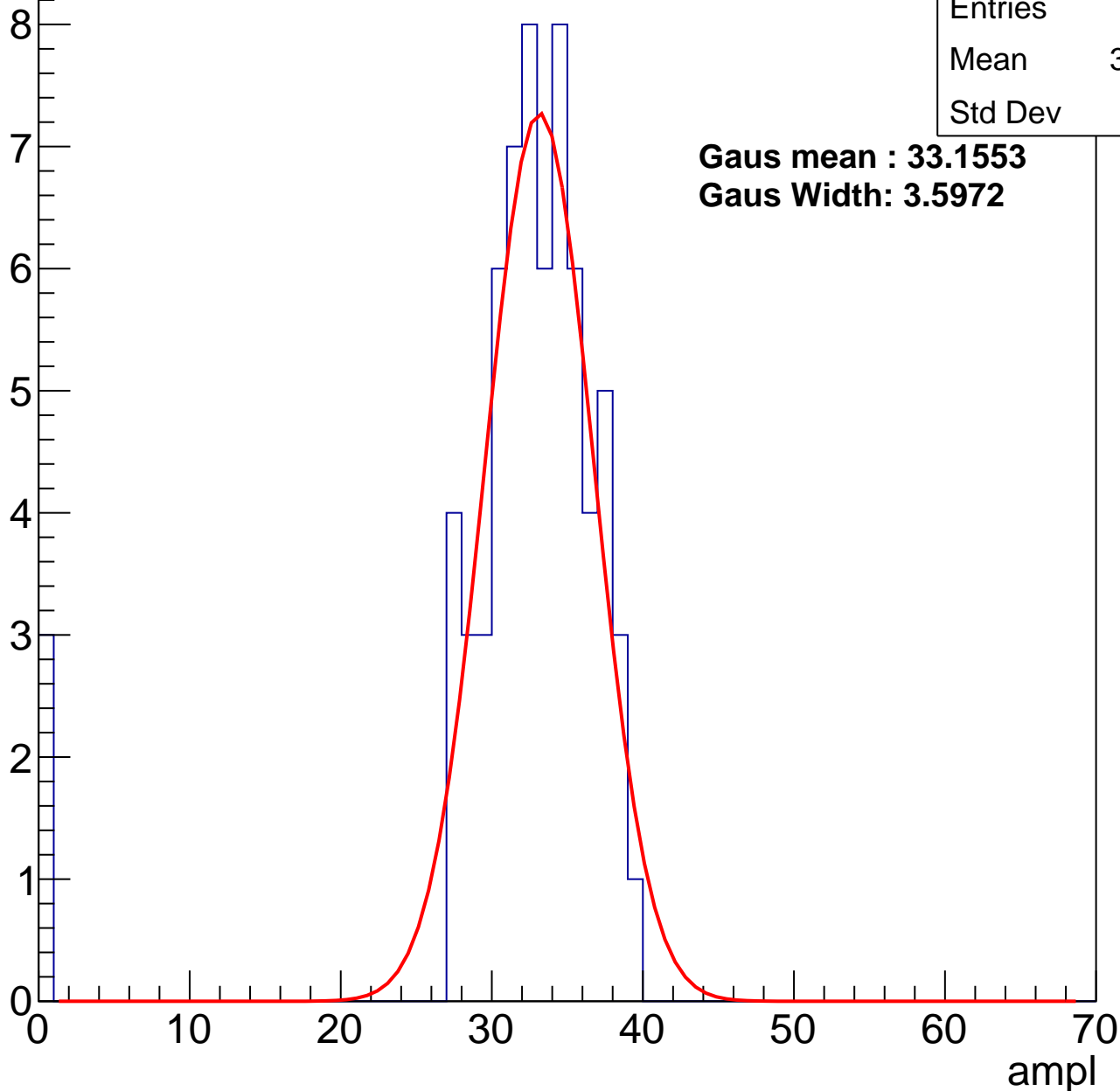
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	31.25
Std Dev	7.41

**Gaus mean : 33.1553**

**Gaus Width: 3.5972**



# B0L001S, U10-ch72, adc1

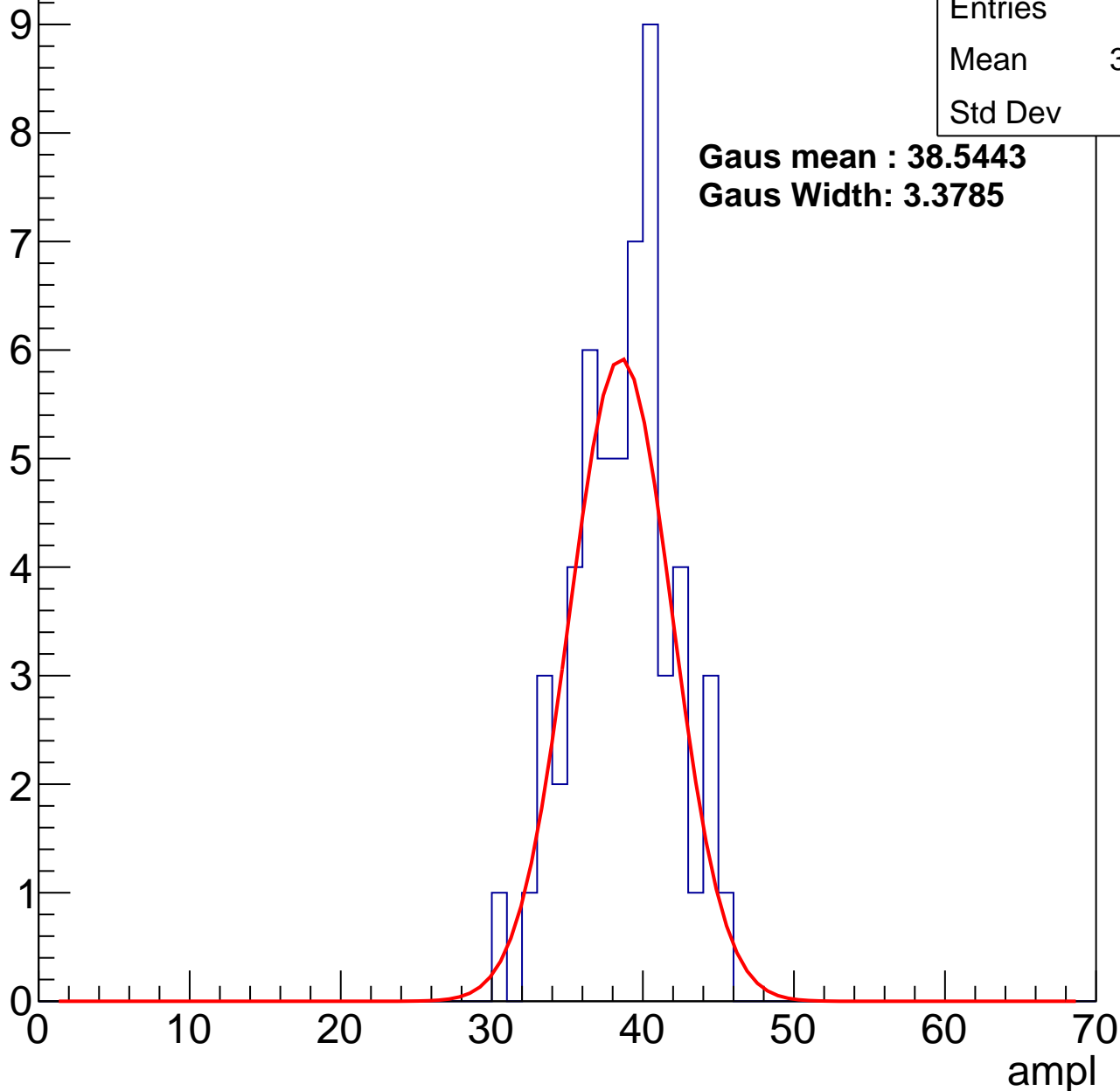
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	38.25
Std Dev	3.26

**Gaus mean : 38.5443**

**Gaus Width: 3.3785**



# B0L001S, U10-ch72, adc2

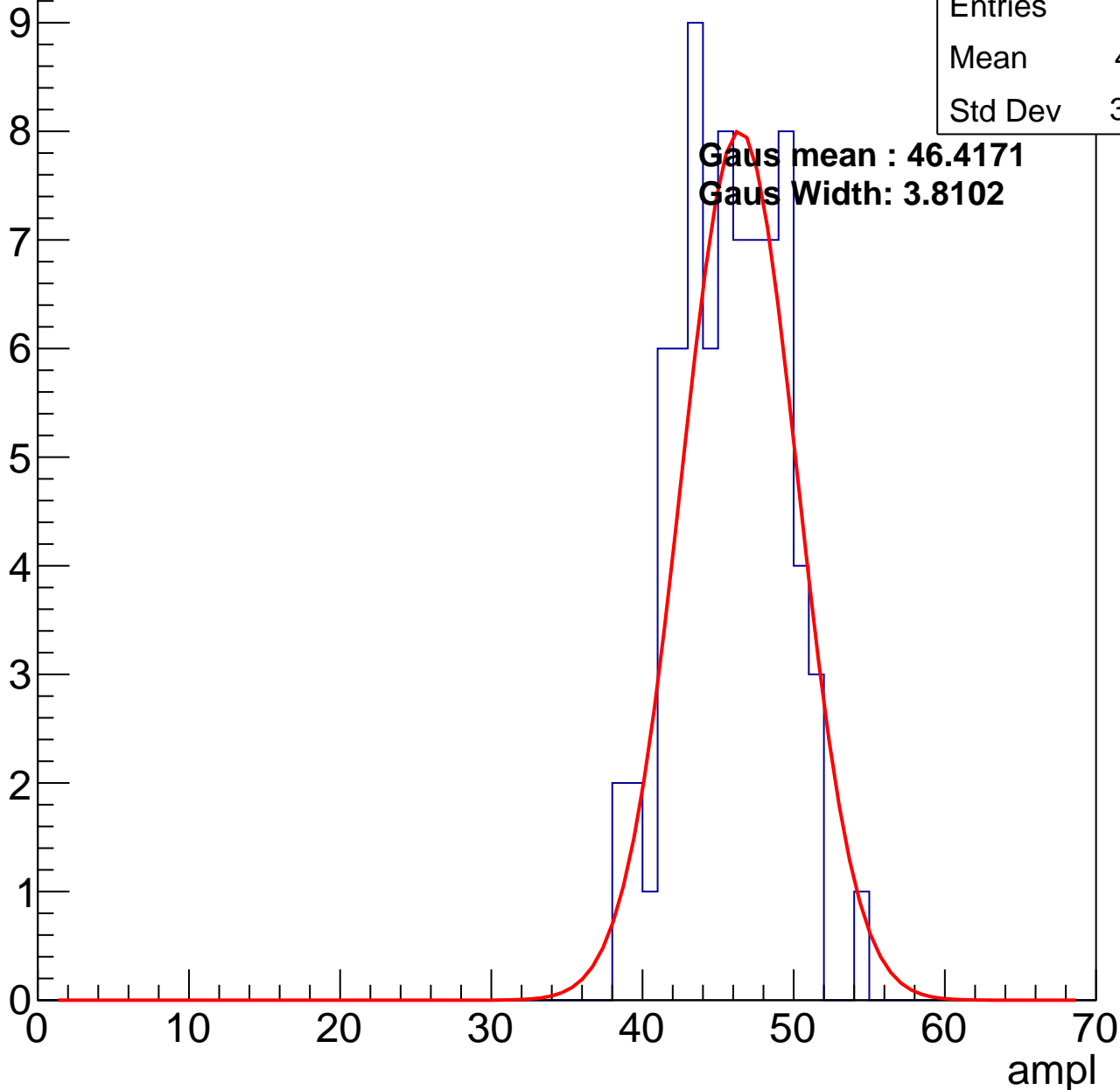
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	77
Mean	45.31
Std Dev	3.408

Gaus mean : 46.4171

Gaus Width: 3.8102

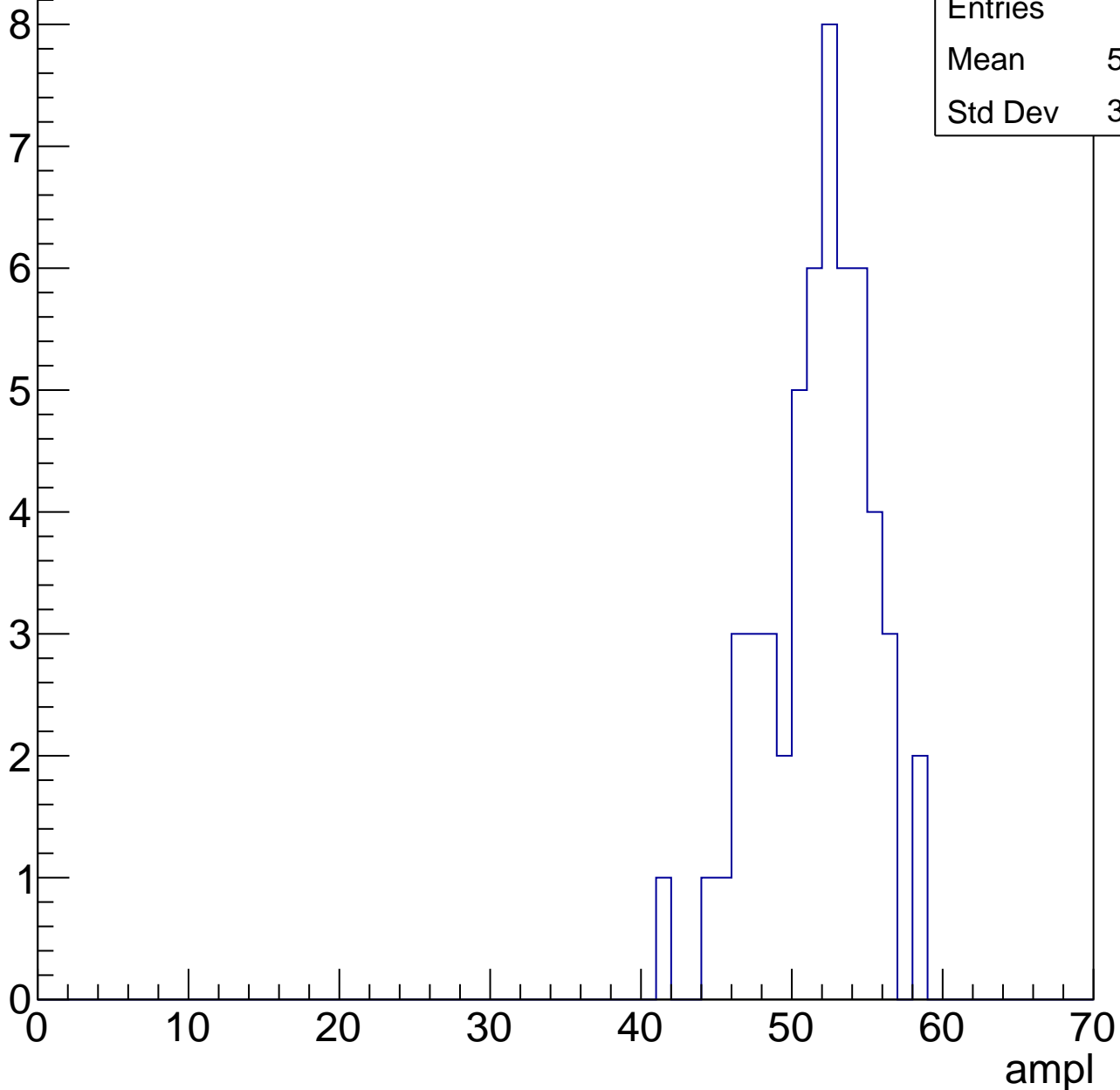


# B0L001S, U10-ch72, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	51.28
Std Dev	3.514

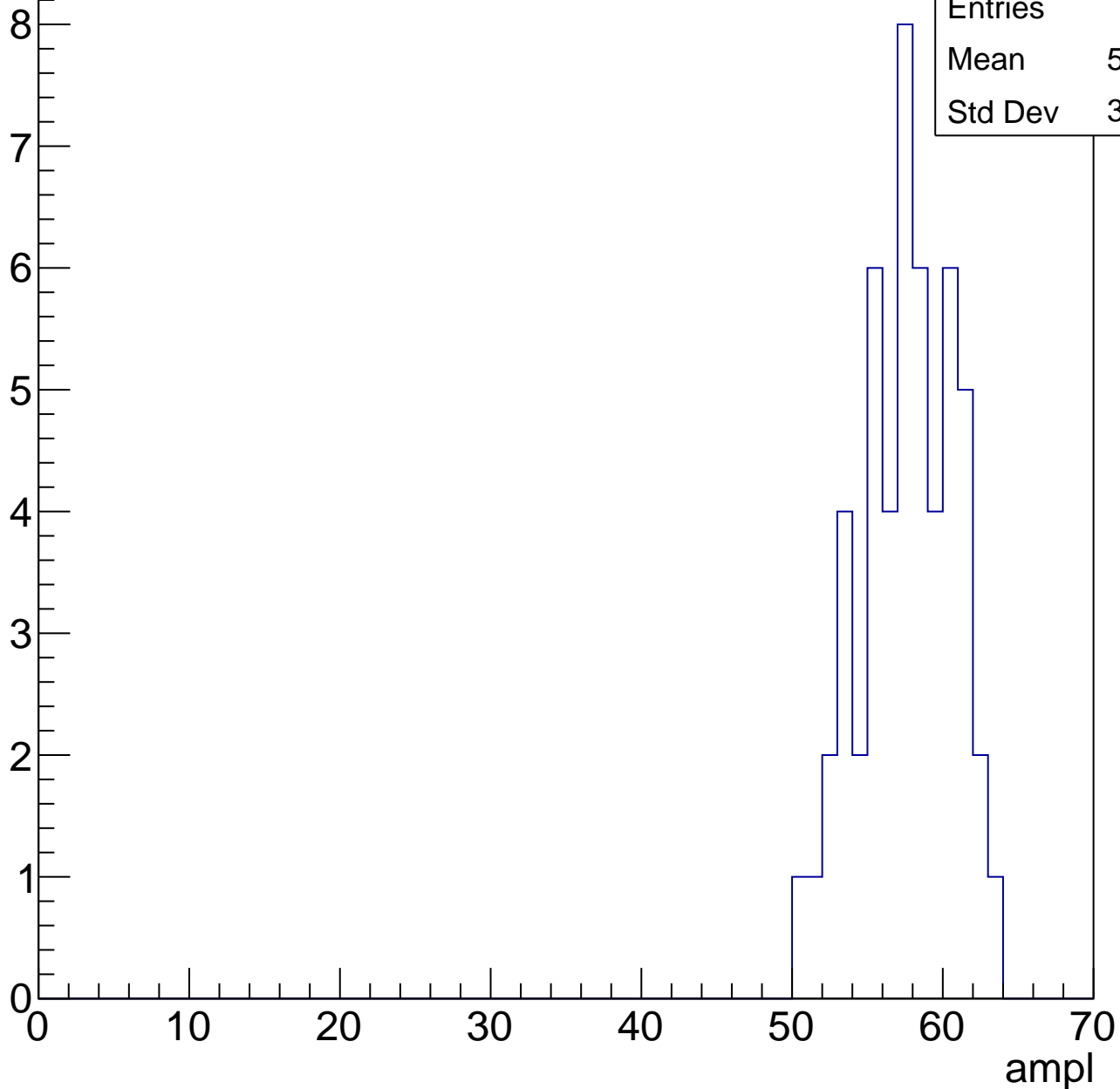


# B0L001S, U10-ch72, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	57.13
Std Dev	3.057

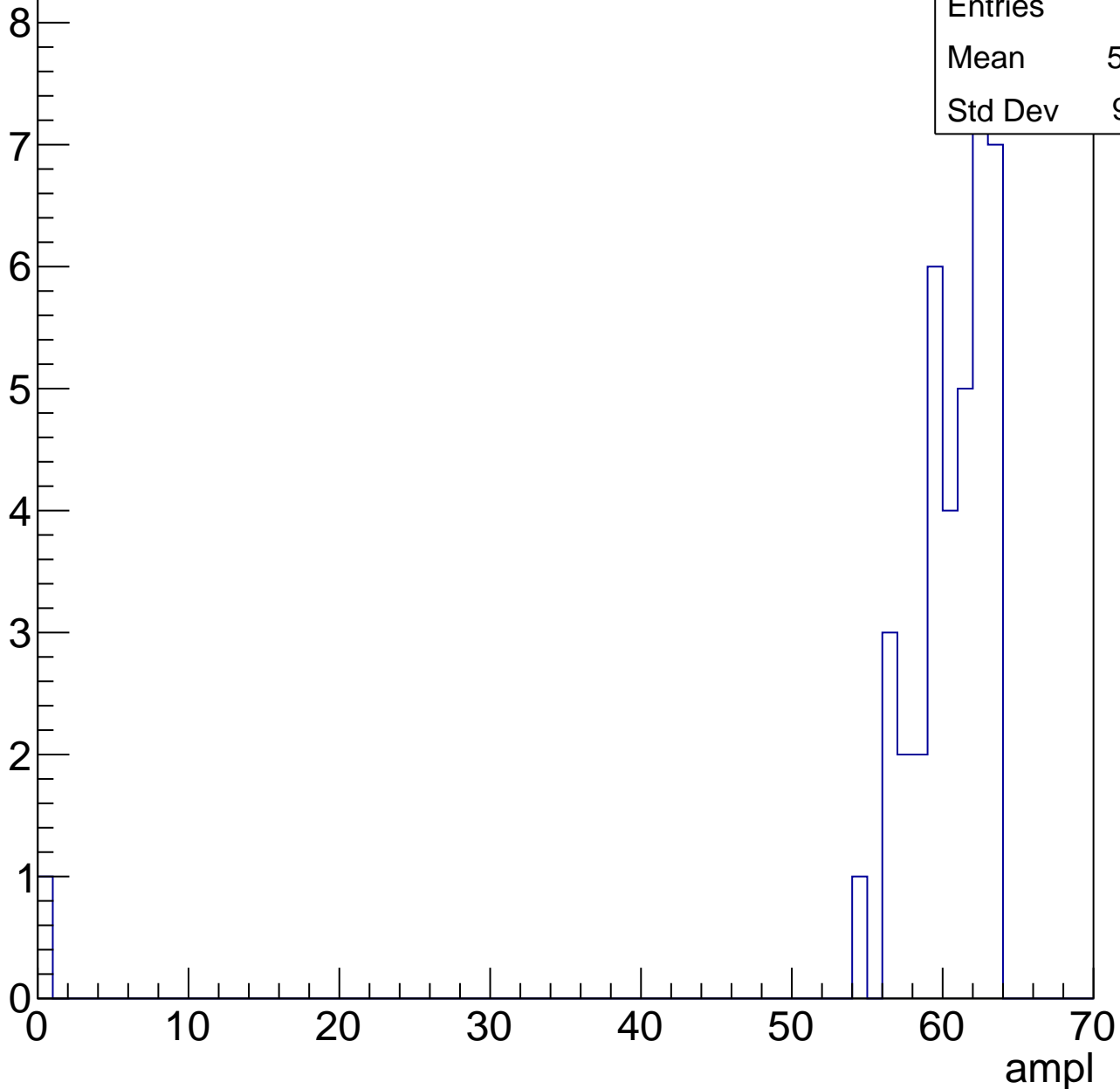


# B0L001S, U10-ch72, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	39
Mean	58.67
Std Dev	9.801



# B0L001S, U10-ch72, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	63
Std Dev	0

0 10 20 30 40 50 60 70

ampl



# B0L001S, U10-ch72, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U10-ch73, adc0

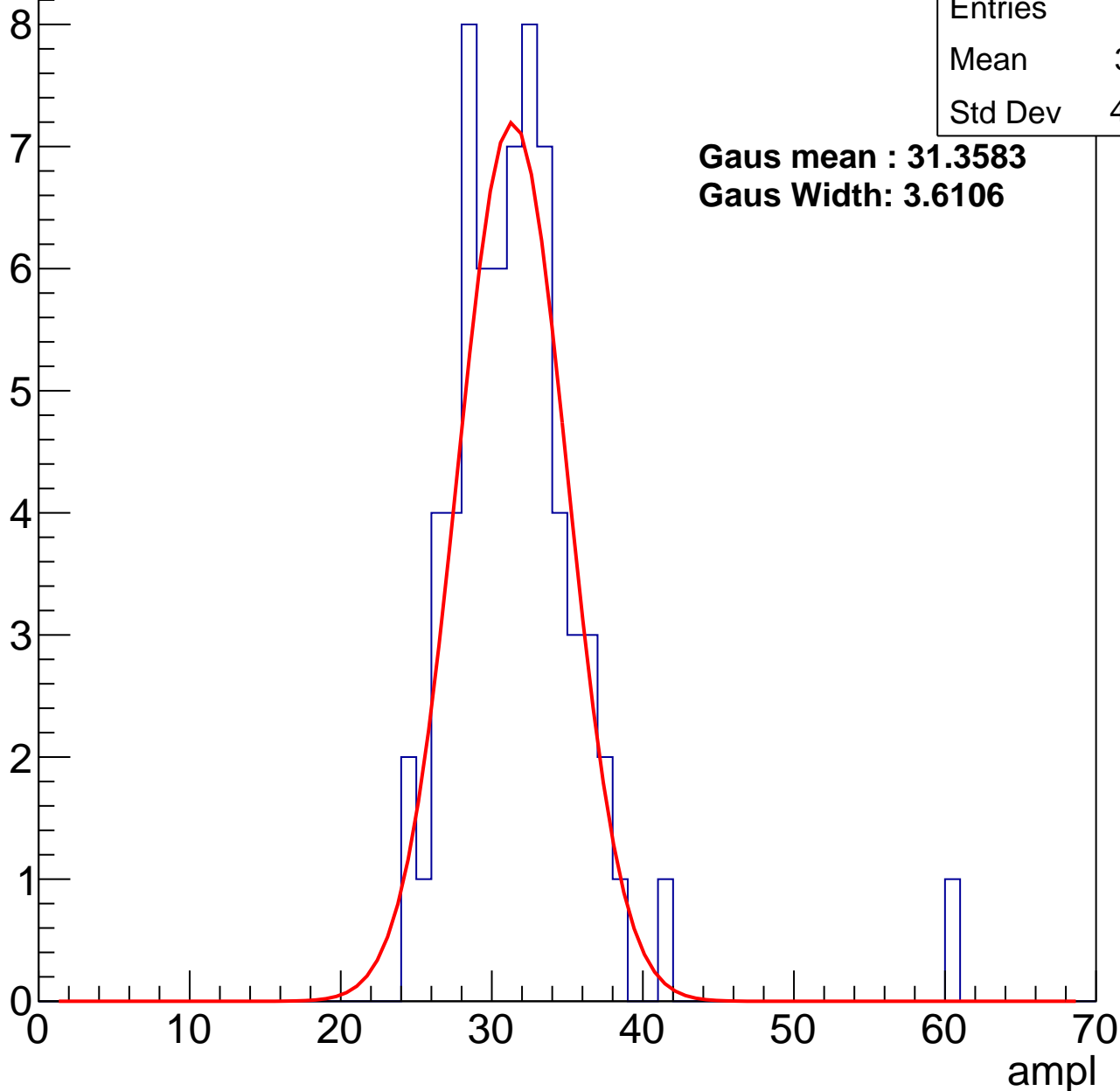
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	31.31
Std Dev	4.927

**Gaus mean : 31.3583**

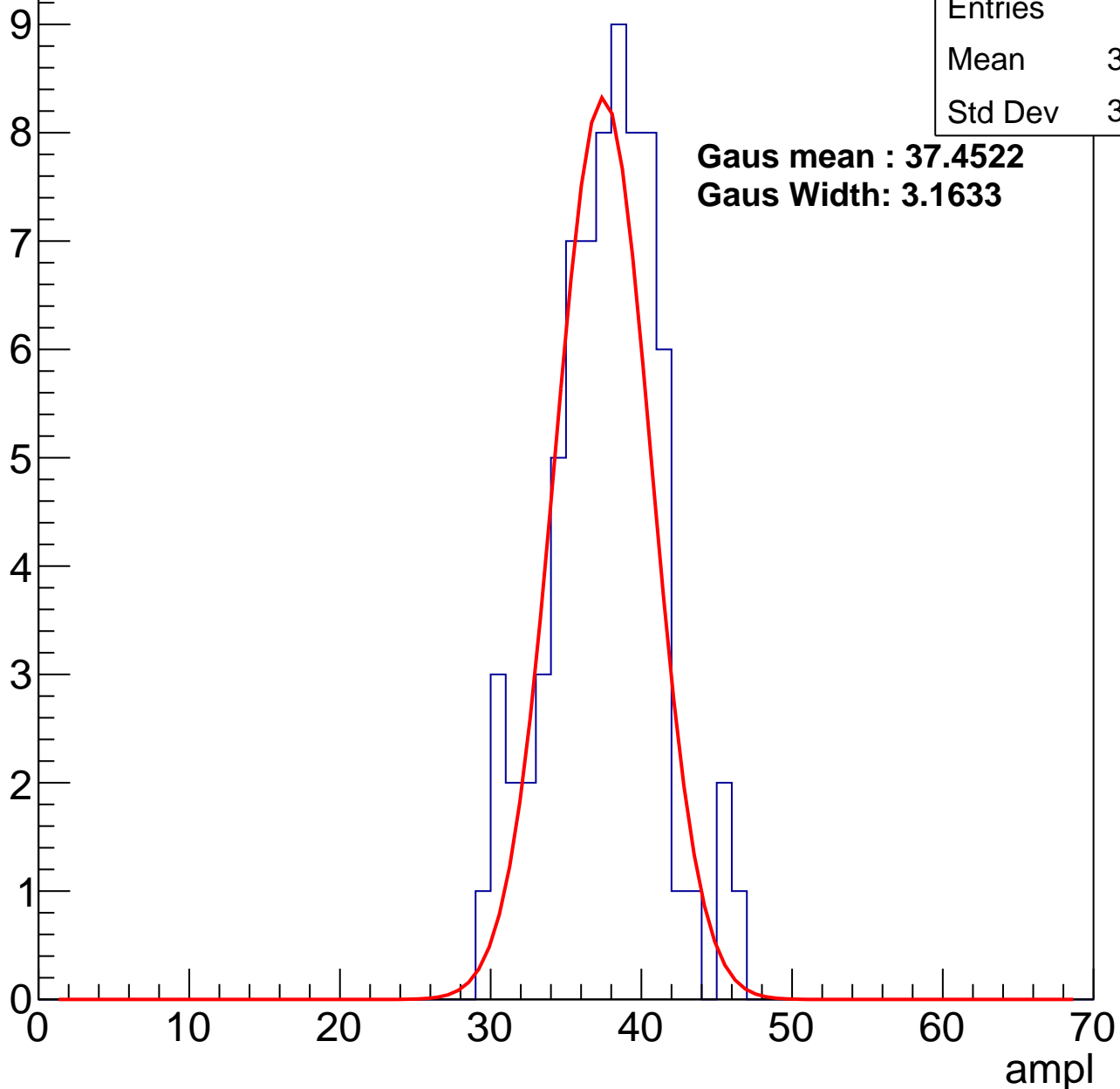
**Gaus Width: 3.6106**



# B0L001S, U10-ch73, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U10-ch73, adc2

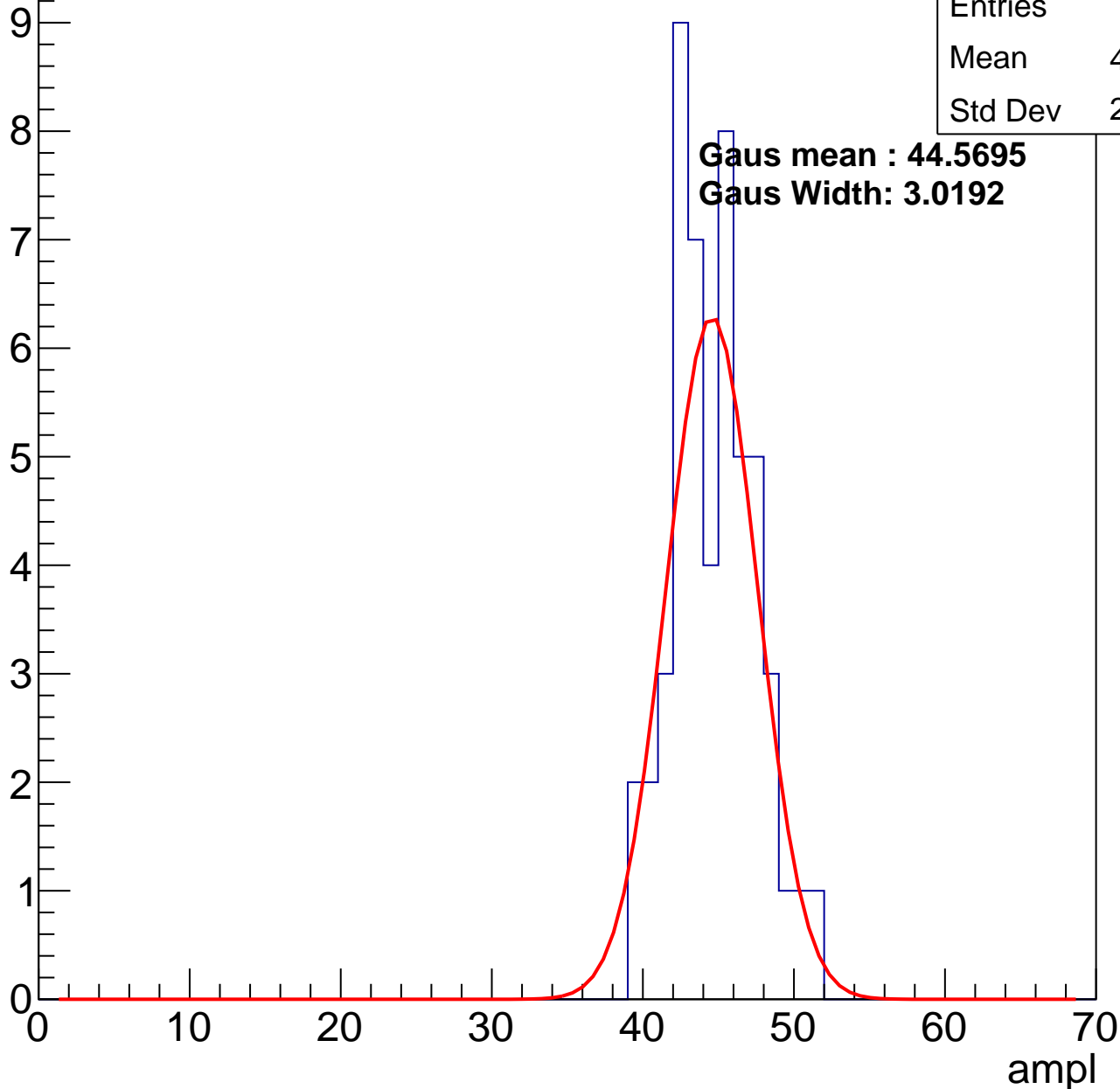
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	51
Mean	44.22
Std Dev	2.732

**Gaus mean : 44.5695**

**Gaus Width: 3.0192**

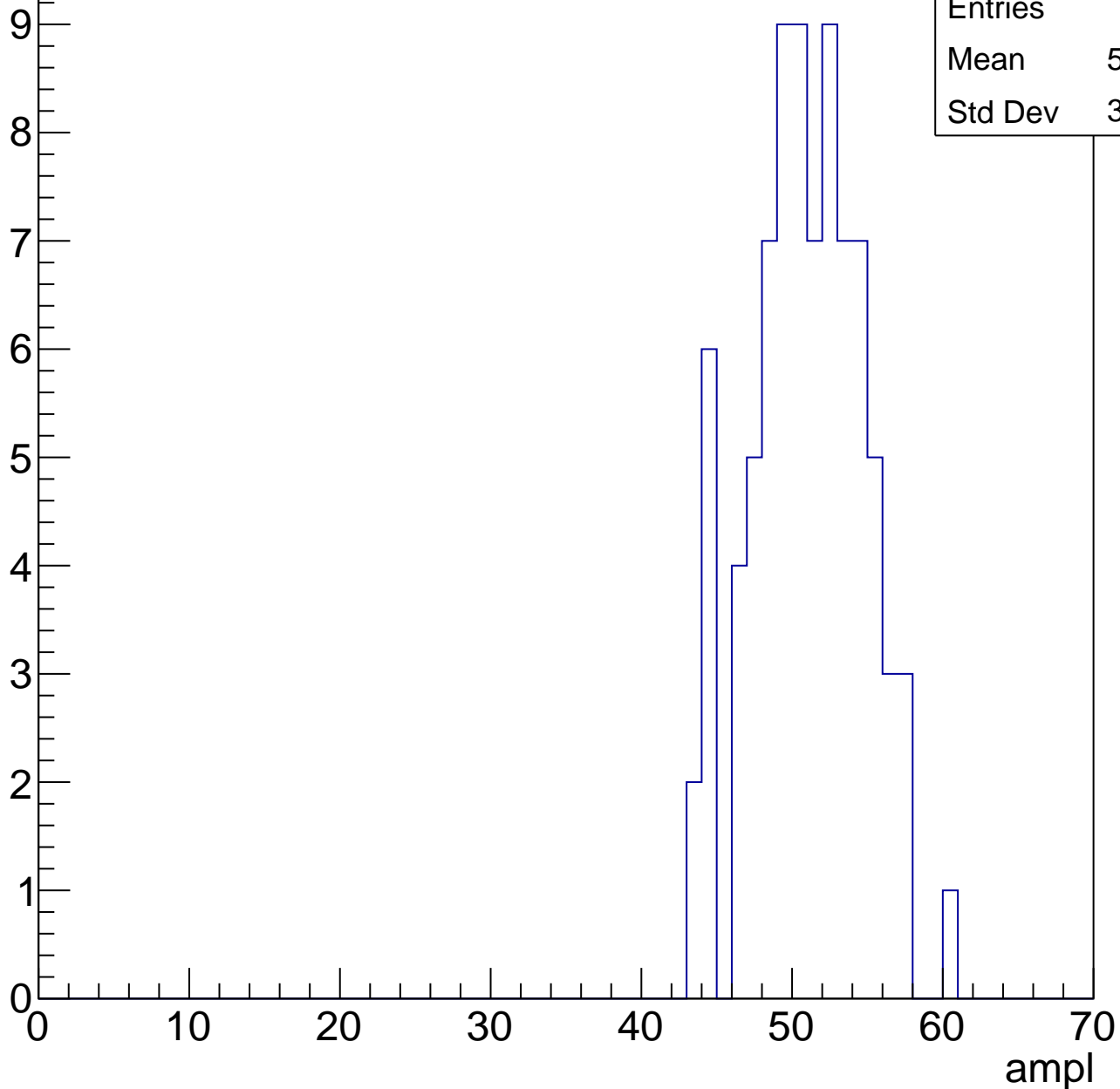


# B0L001S, U10-ch73, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	84
Mean	50.52
Std Dev	3.676

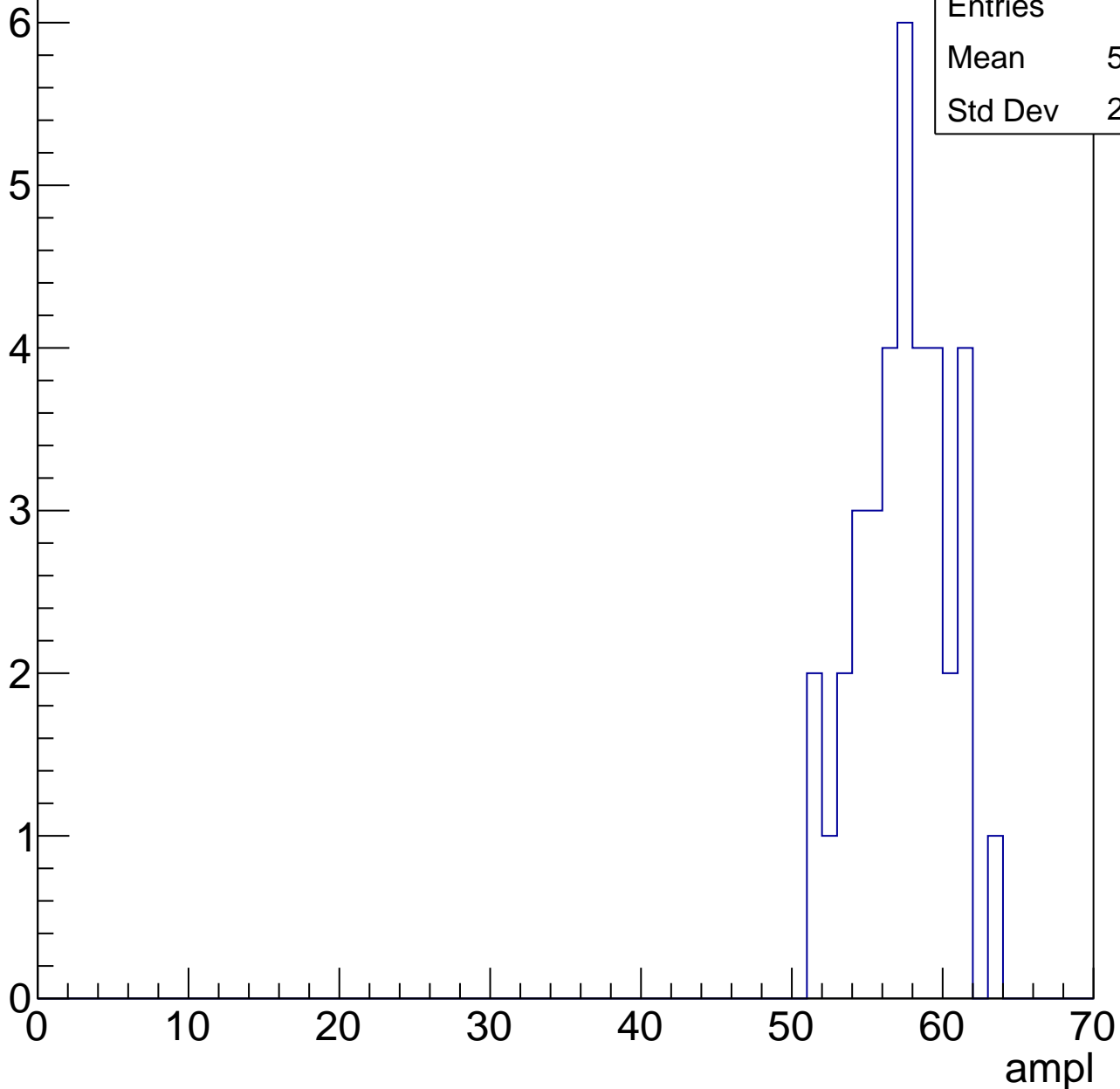


# B0L001S, U10-ch73, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	36
Mean	56.89
Std Dev	2.932



# B0L001S, U10-ch73, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	49
Mean	58.78
Std Dev	8.842

Entry

10

8

6

4

2

0

0

10

20

30

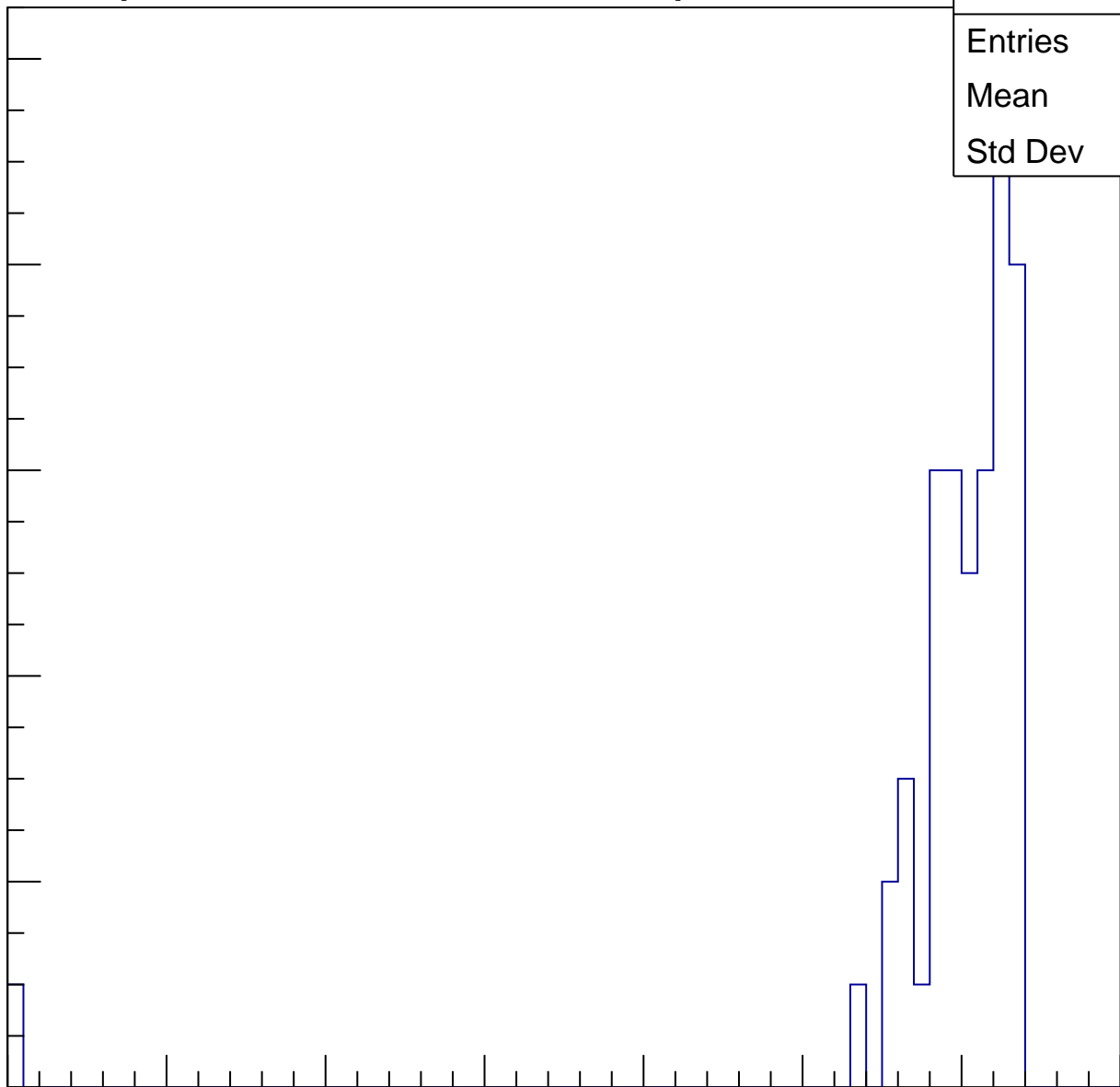
40

50

60

70

ampl



# B0L001S, U10-ch73, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch73, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U10-ch74, adc0

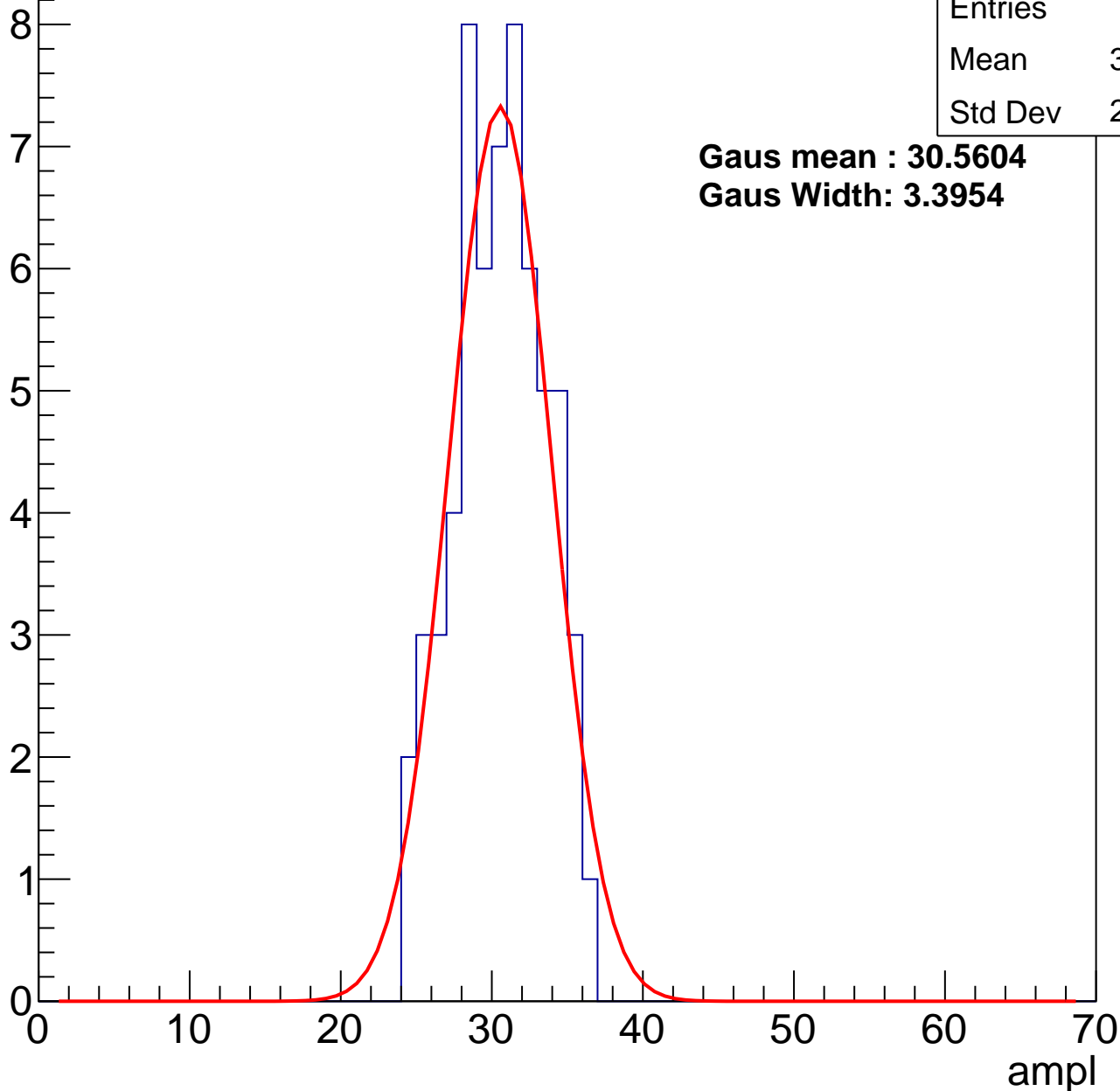
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	30.05
Std Dev	2.967

**Gaus mean : 30.5604**

**Gaus Width: 3.3954**



# B0L001S, U10-ch74, adc1

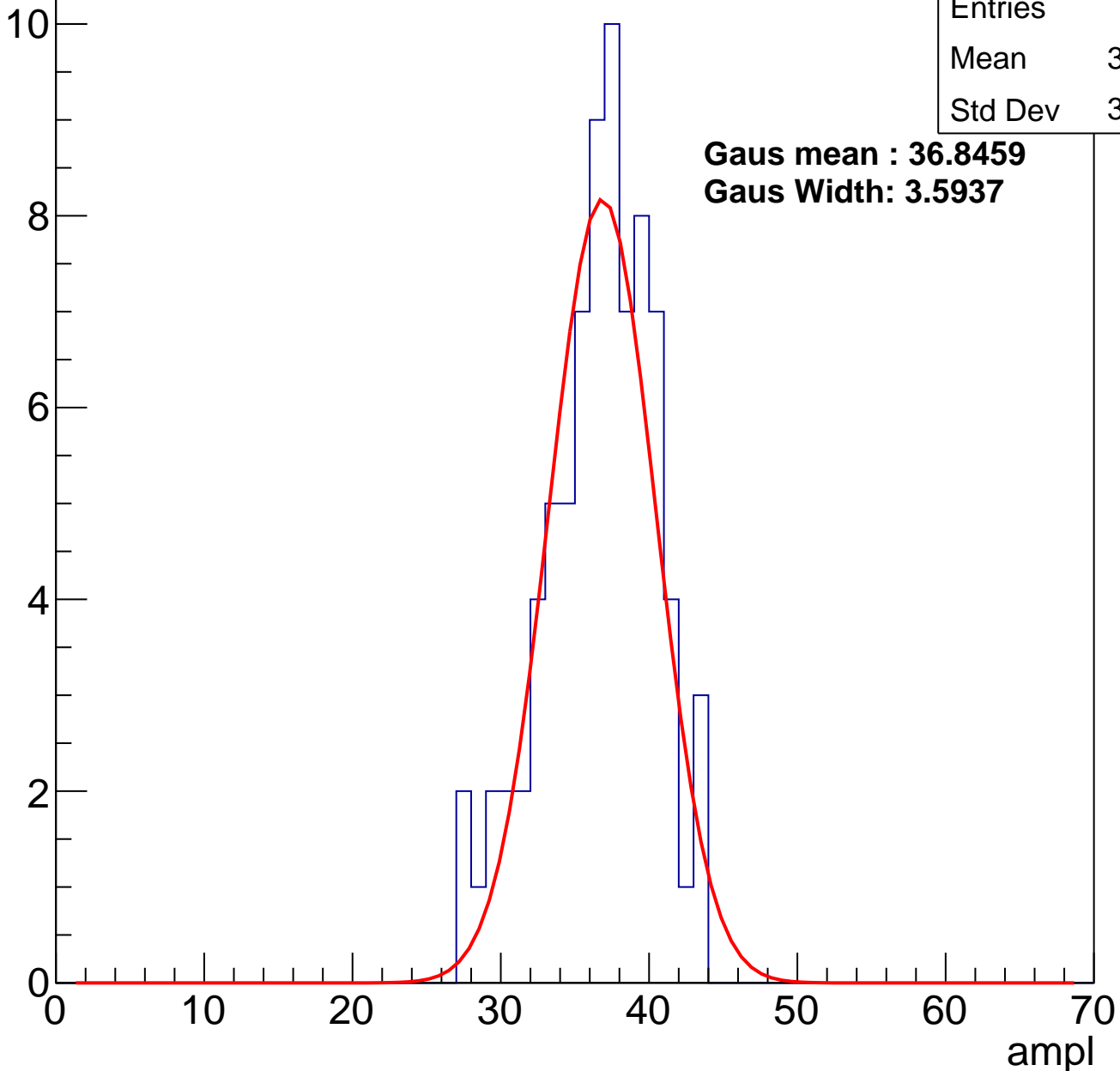
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	79
Mean	36.16
Std Dev	3.706

**Gaus mean : 36.8459**

**Gaus Width: 3.5937**

Entry



# B0L001S, U10-ch74, adc2

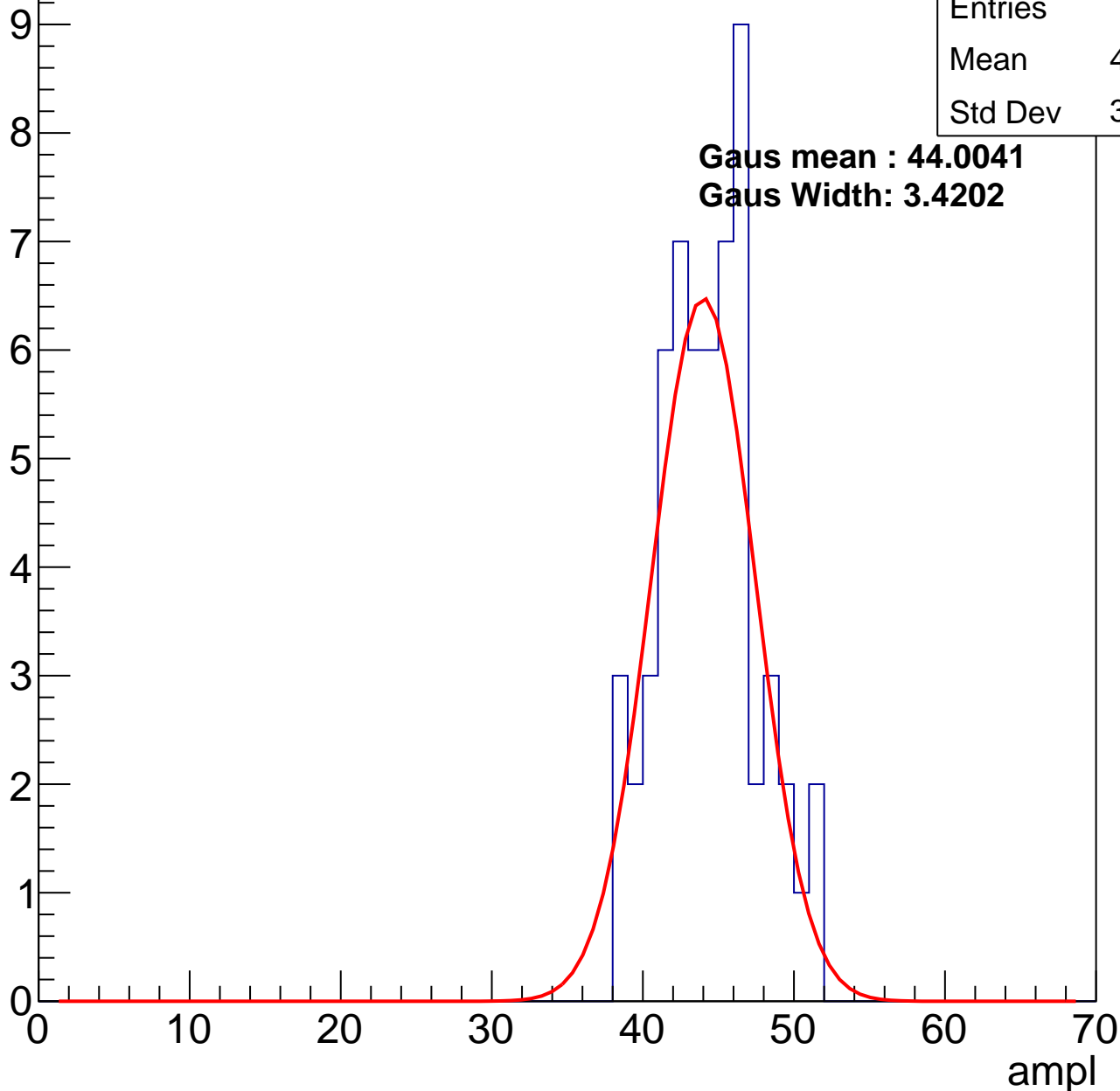
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	43.92
Std Dev	3.153

**Gaus mean : 44.0041**

**Gaus Width: 3.4202**

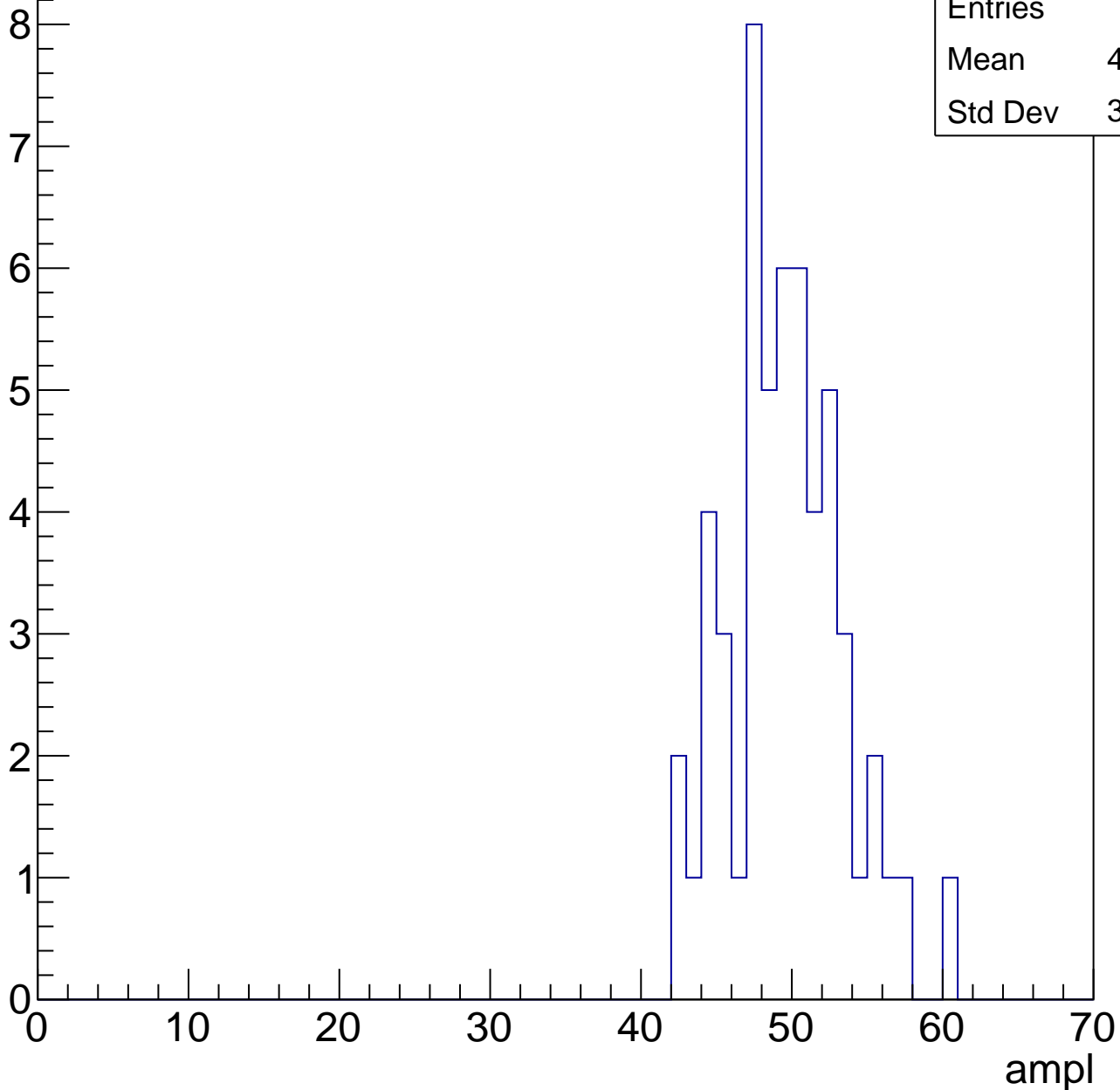


# B0L001S, U10-ch74, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	49.15
Std Dev	3.783

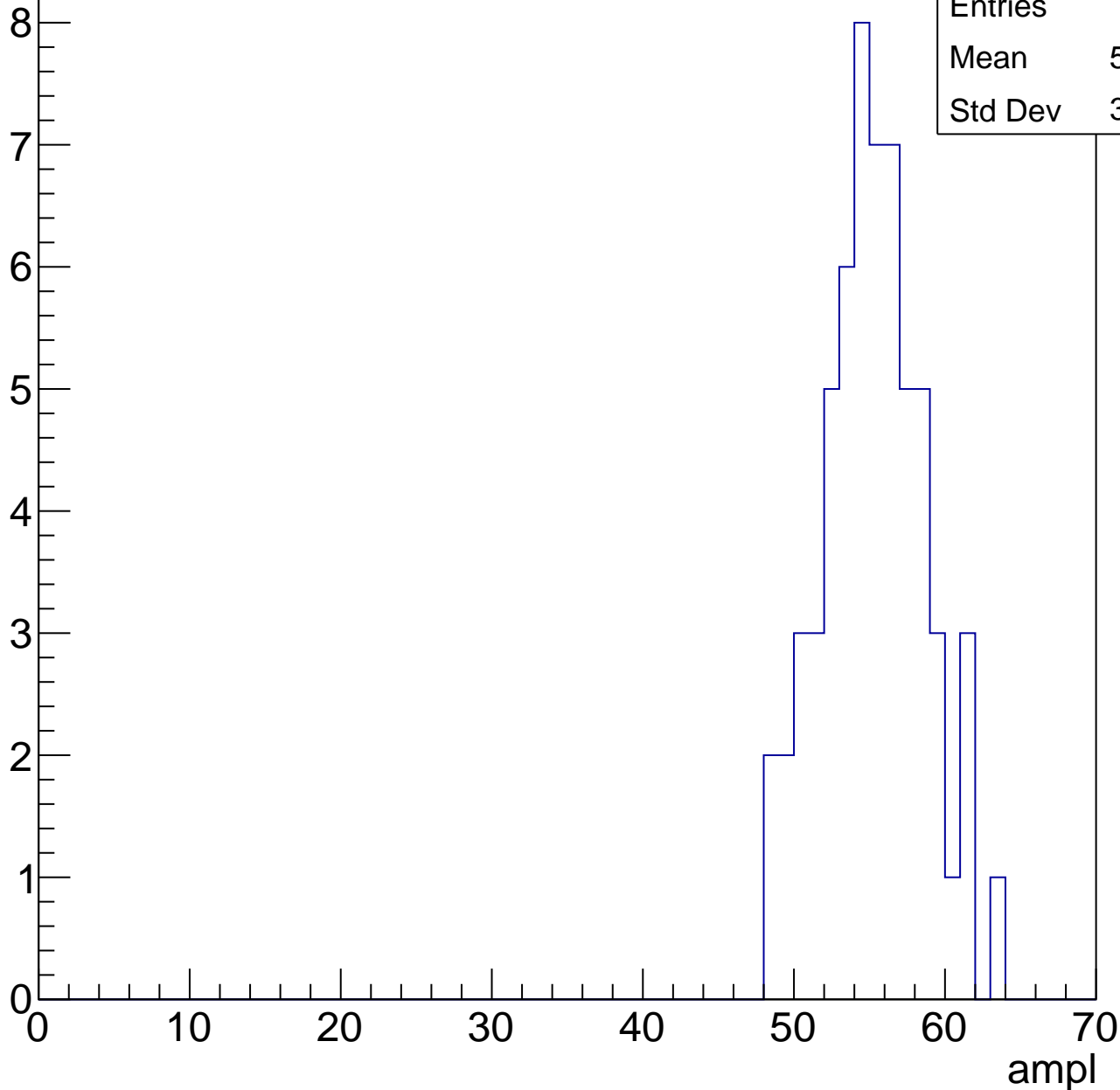


# B0L001S, U10-ch74, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	54.79
Std Dev	3.349

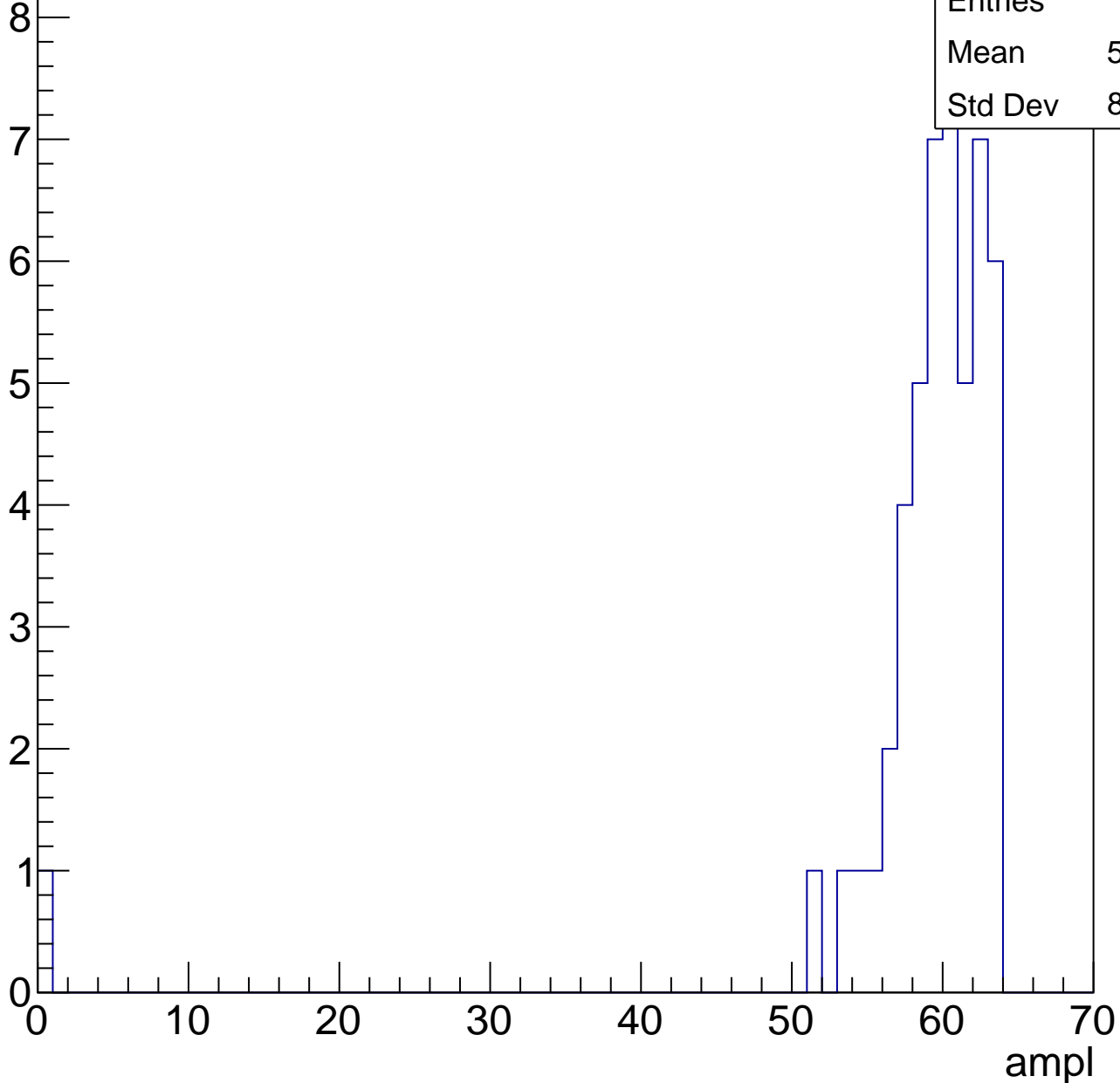


# B0L001S, U10-ch74, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	49
Mean	58.22
Std Dev	8.828



# B0L001S, U10-ch74, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries

8

Mean

62.12

Std Dev

0.7806



# B0L001S, U10-ch74, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	3
Mean	7.667
Std Dev	10.84

# B0L001S, U10-ch75, adc0

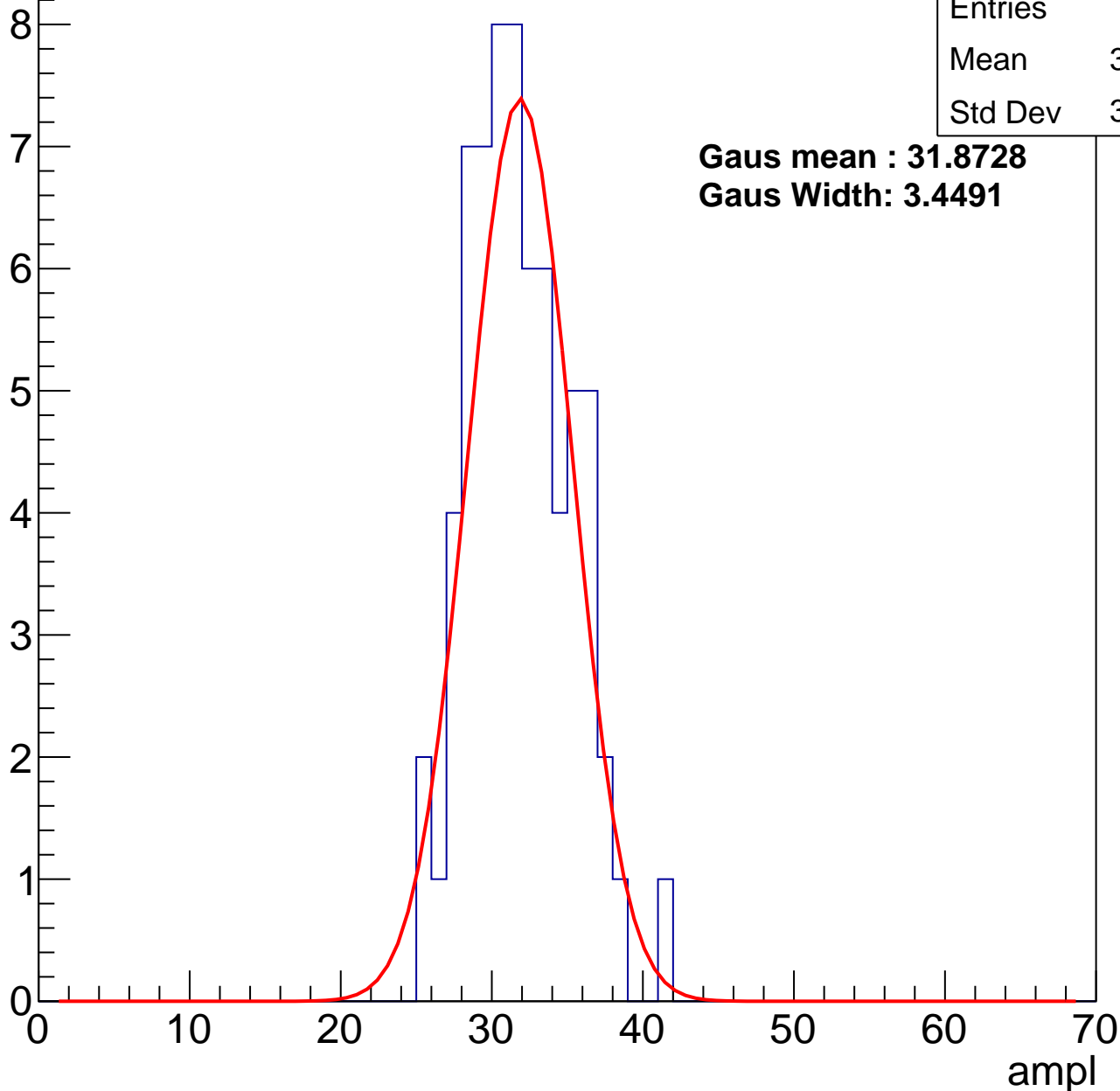
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	31.42
Std Dev	3.324

**Gaus mean : 31.8728**

**Gaus Width: 3.4491**



# B0L001S, U10-ch75, adc1

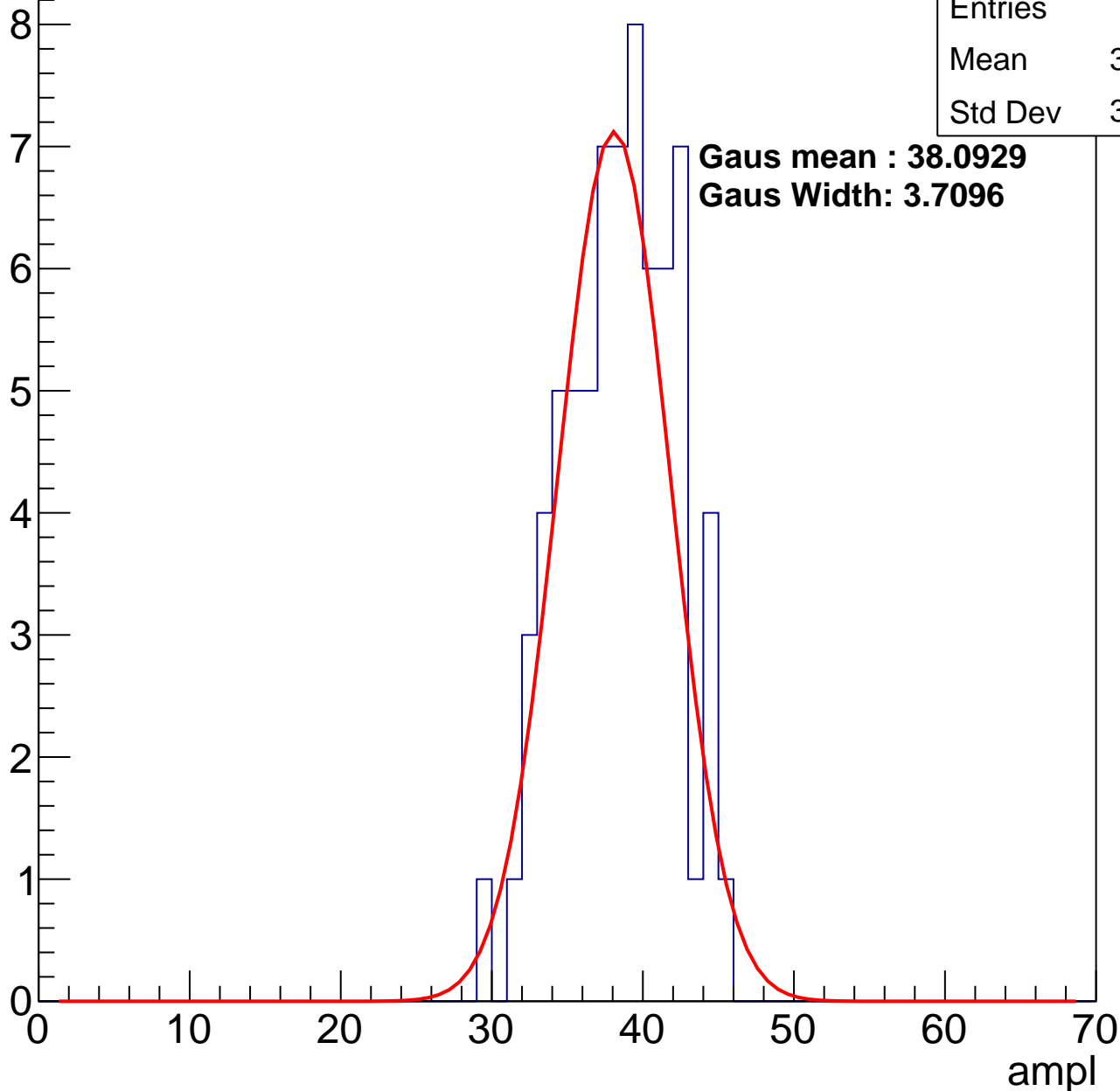
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	37.94
Std Dev	3.572

**Gaus mean : 38.0929**

**Gaus Width: 3.7096**



# B0L001S, U10-ch75, adc2

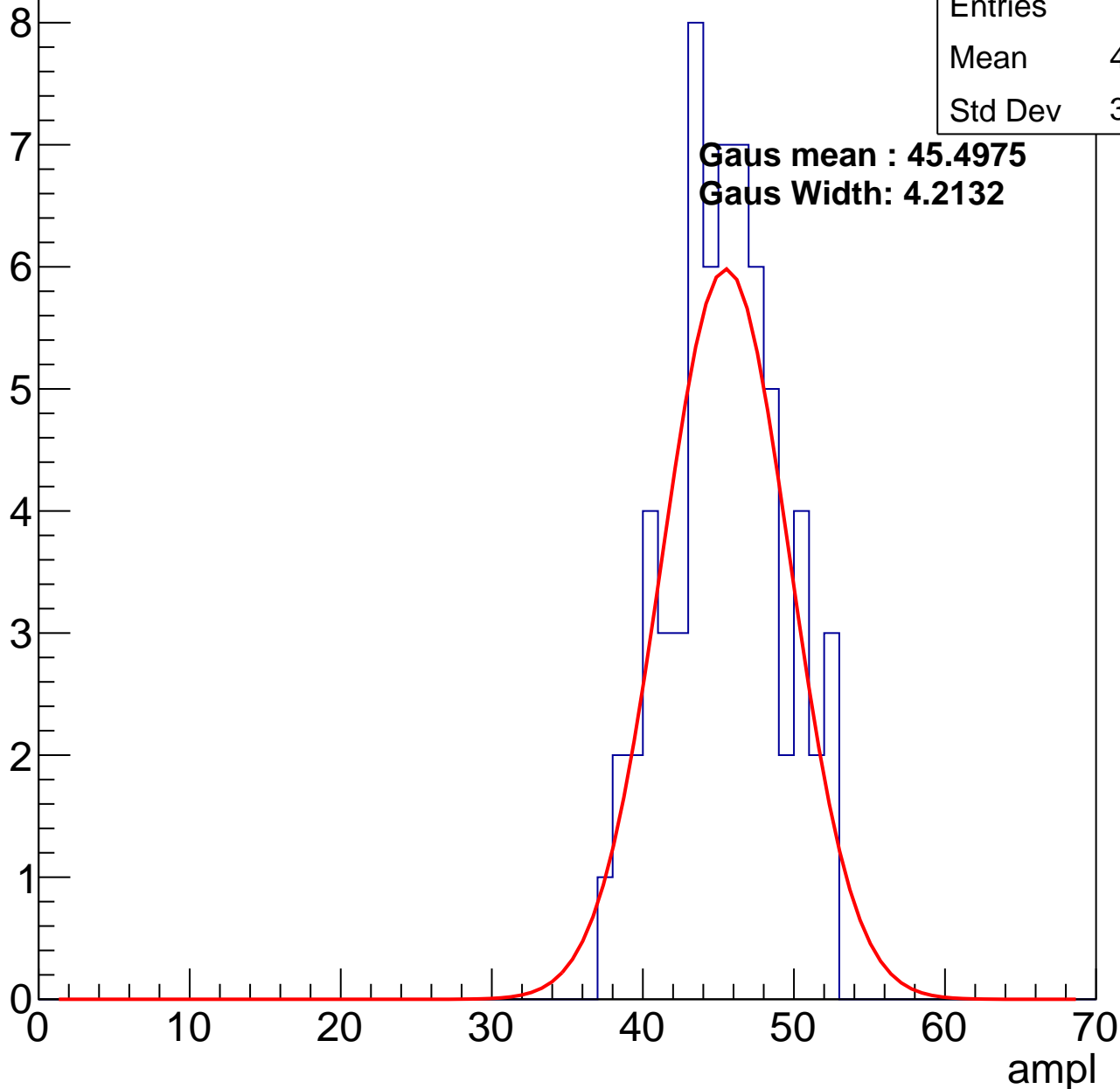
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	44.97
Std Dev	3.667

**Gaus mean : 45.4975**

**Gaus Width: 4.2132**

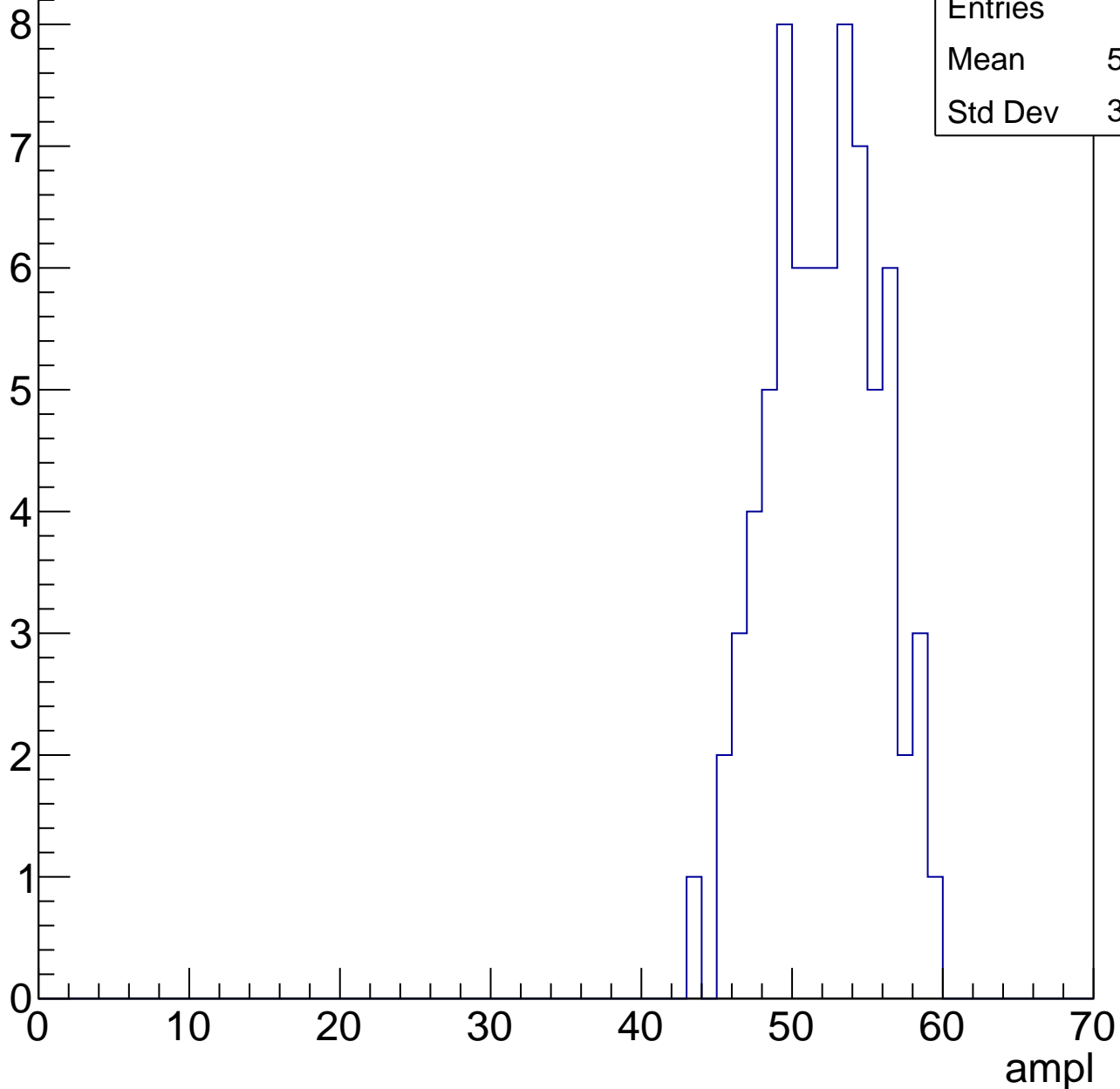


# B0L001S, U10-ch75, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	51.63
Std Dev	3.594

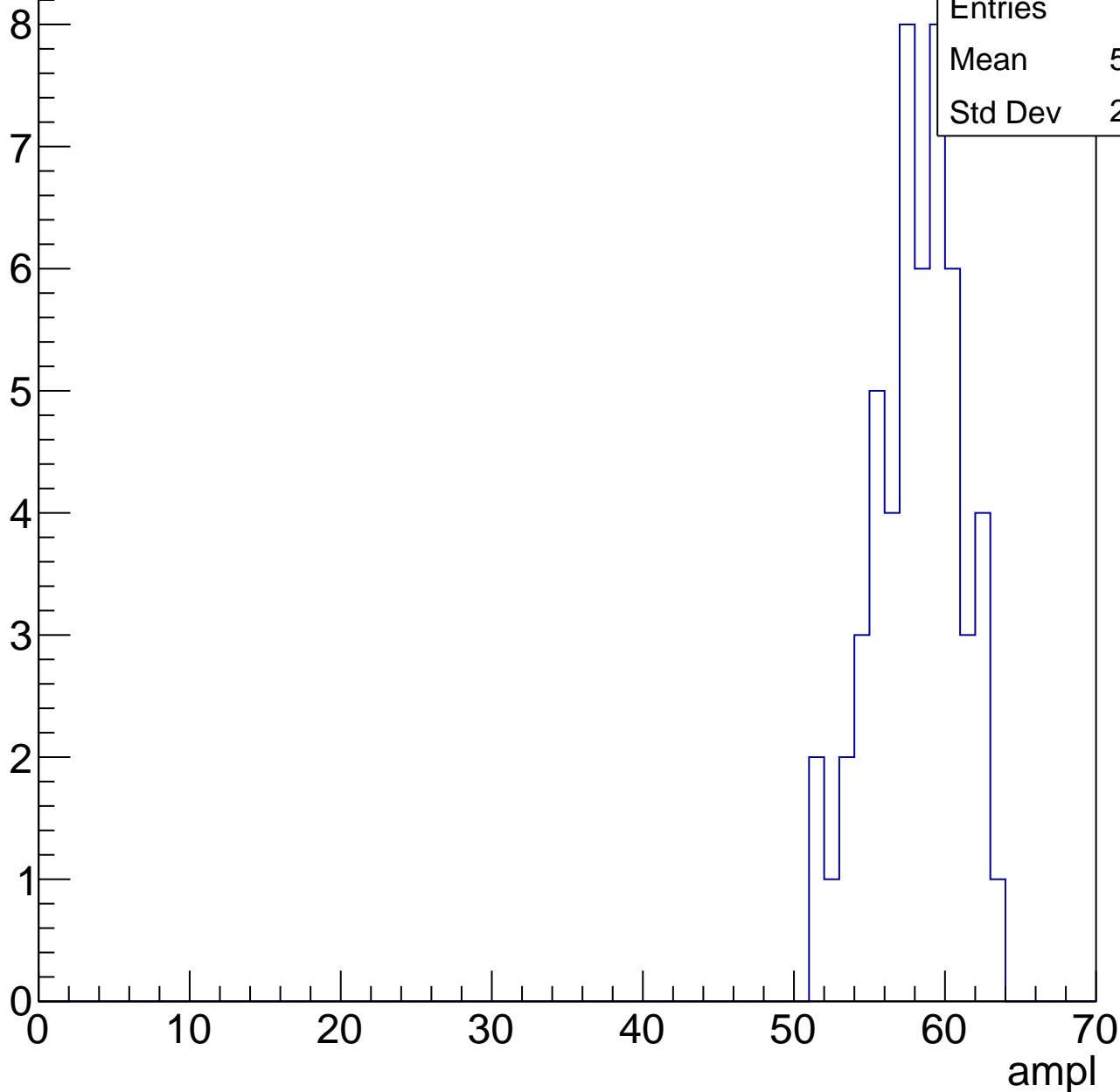


# B0L001S, U10-ch75, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	57.57
Std Dev	2.878

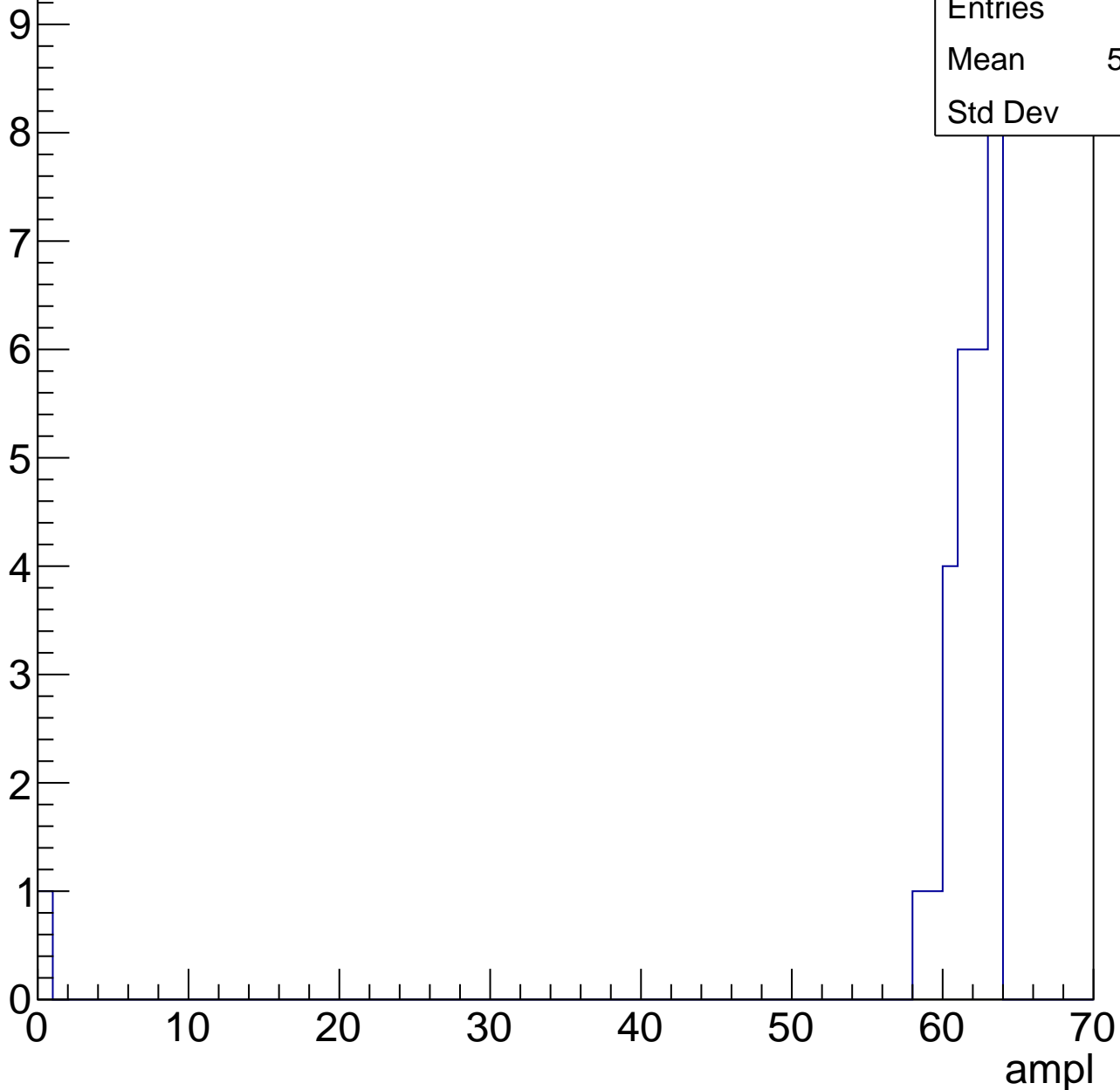


# B0L001S, U10-ch75, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	28
Mean	59.36
Std Dev	11.5



# B0L001S, U10-ch75, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch75, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	3
Mean	8
Std Dev	11.31

# B0L001S, U10-ch76, adc0

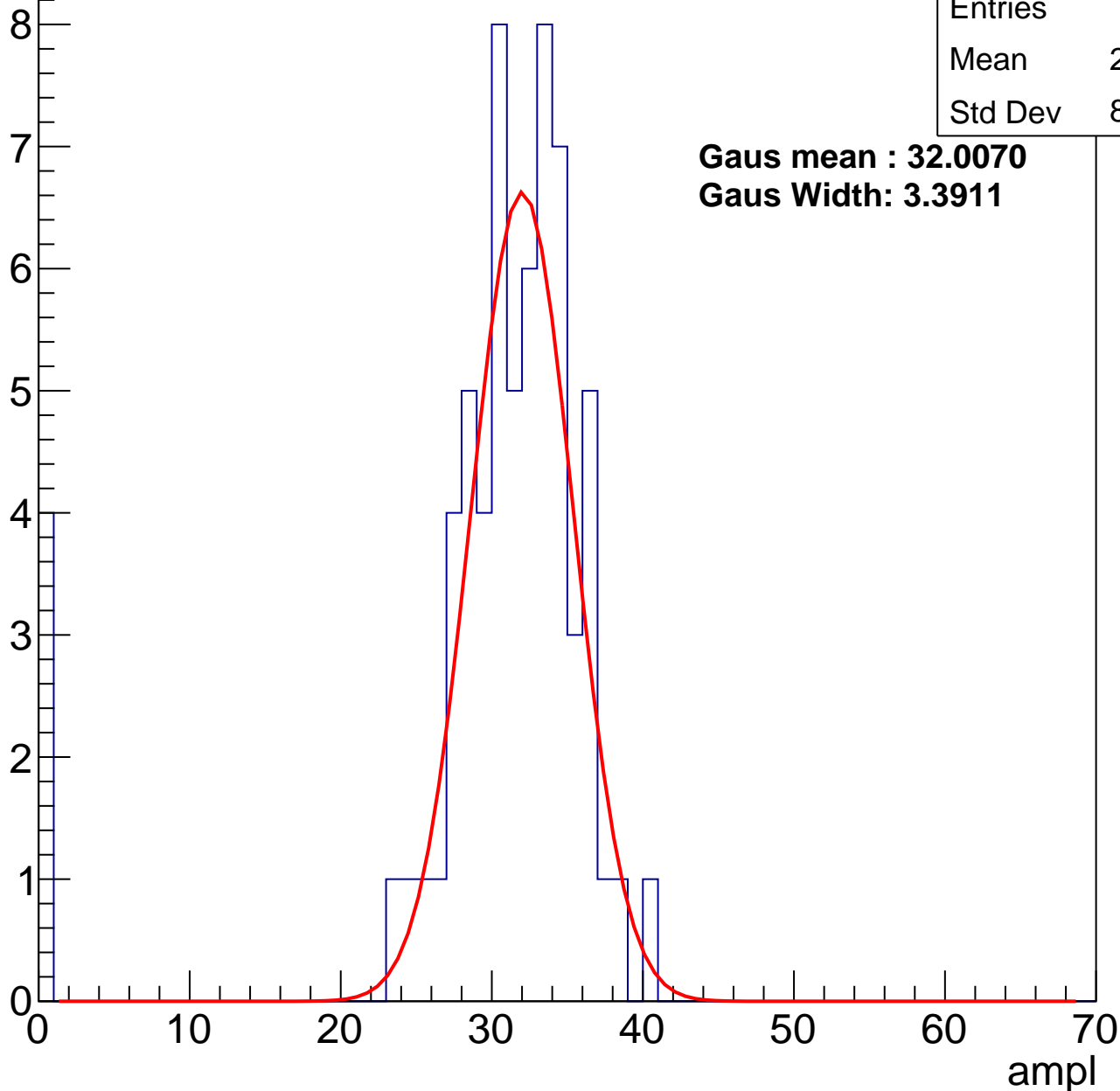
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	29.56
Std Dev	8.215

**Gaus mean : 32.0070**

**Gaus Width: 3.3911**



# B0L001S, U10-ch76, adc1

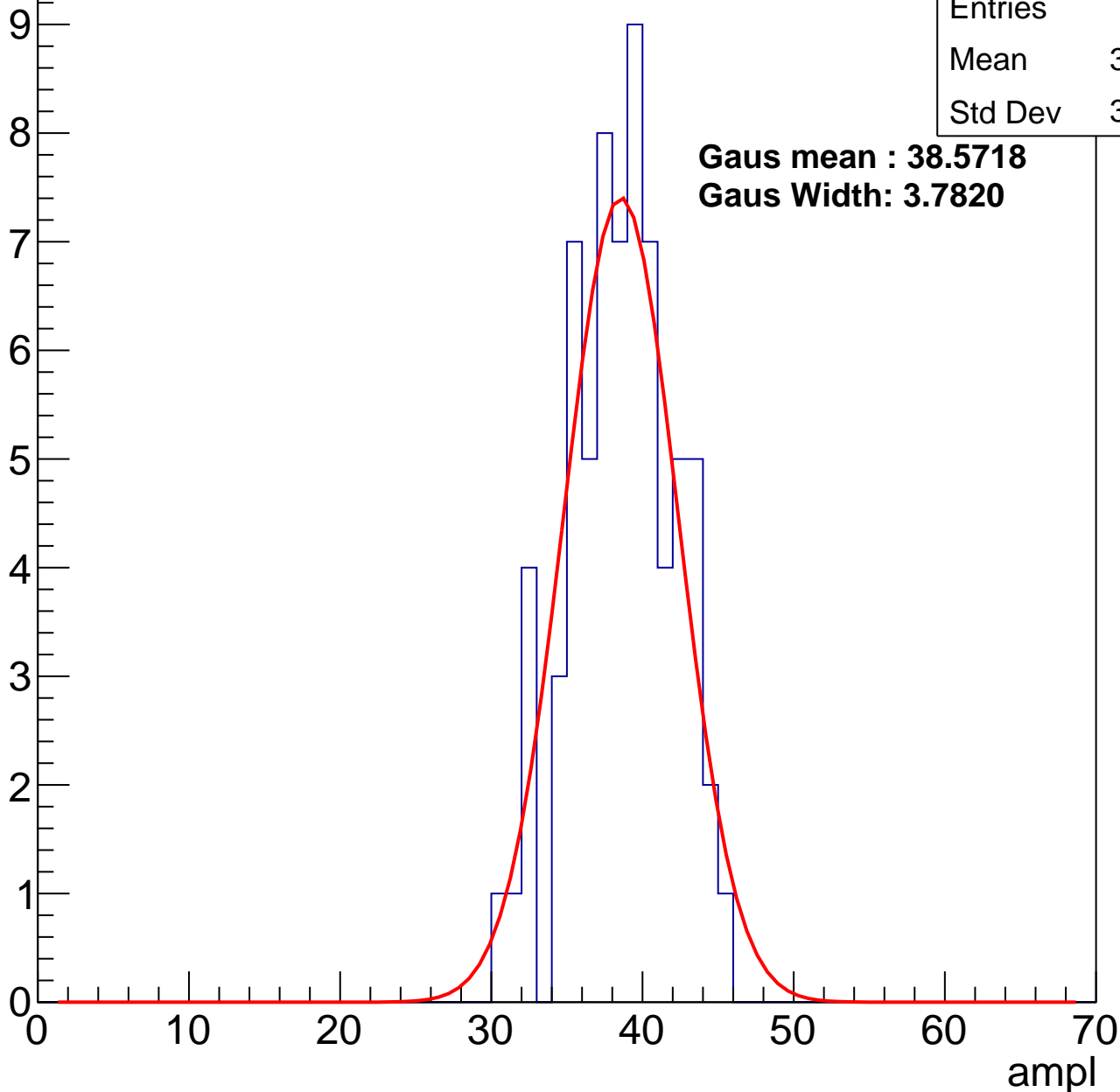
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	38.13
Std Dev	3.392

**Gaus mean : 38.5718**

**Gaus Width: 3.7820**



# B0L001S, U10-ch76, adc2

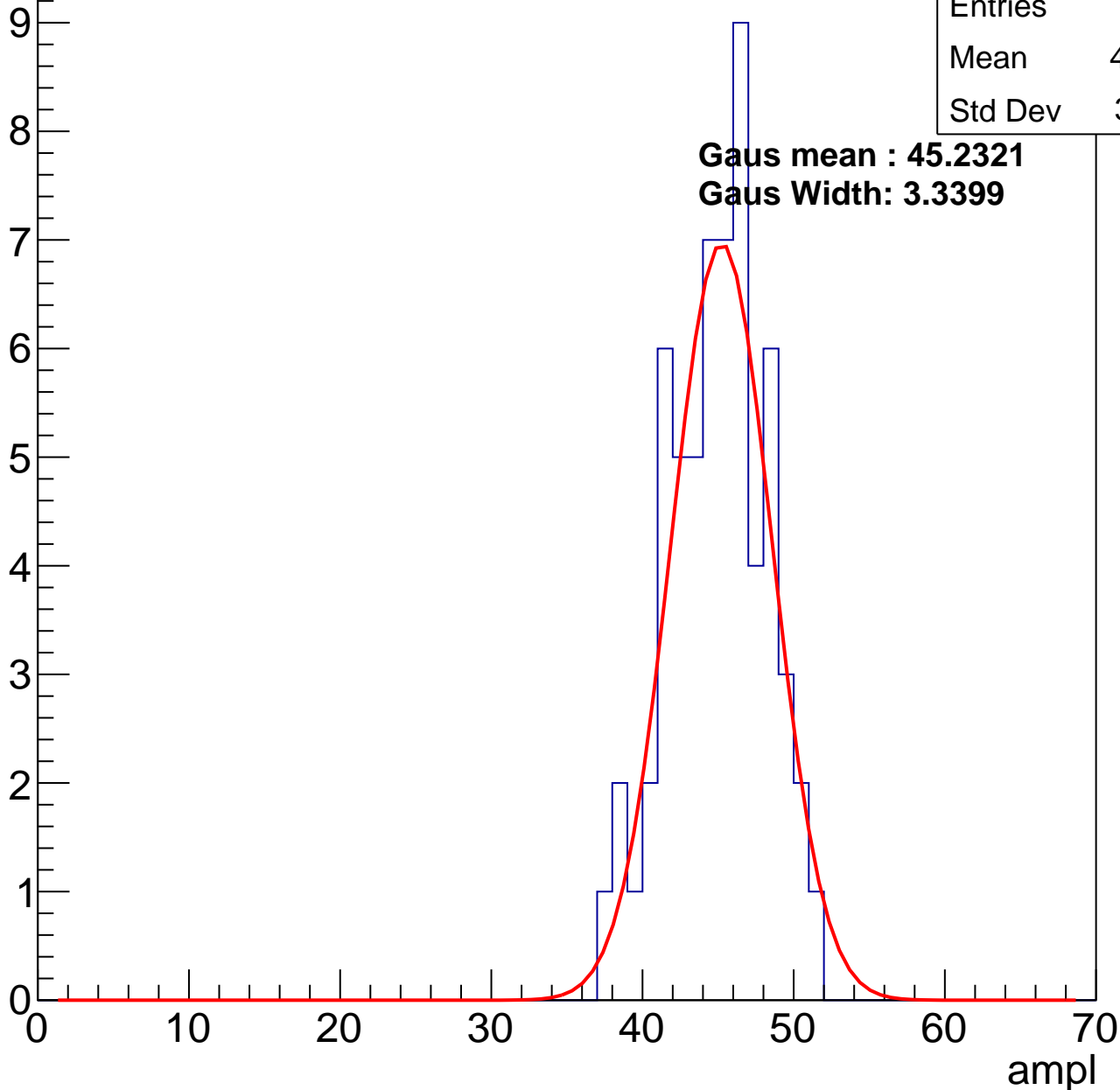
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	44.49
Std Dev	3.171

**Gaus mean : 45.2321**

**Gaus Width: 3.3399**

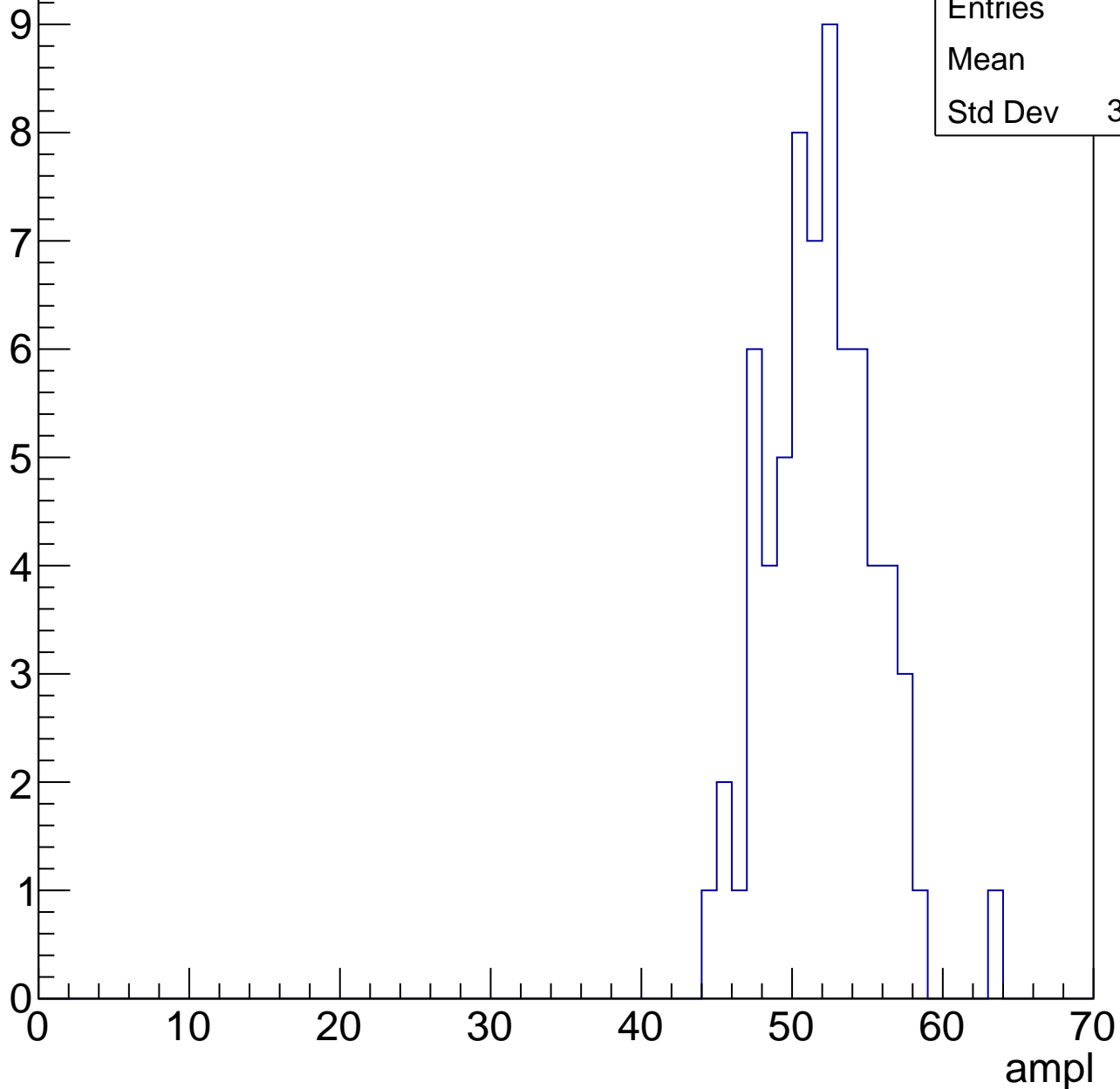


# B0L001S, U10-ch76, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	51.5
Std Dev	3.517



# B0L001S, U10-ch76, adc4

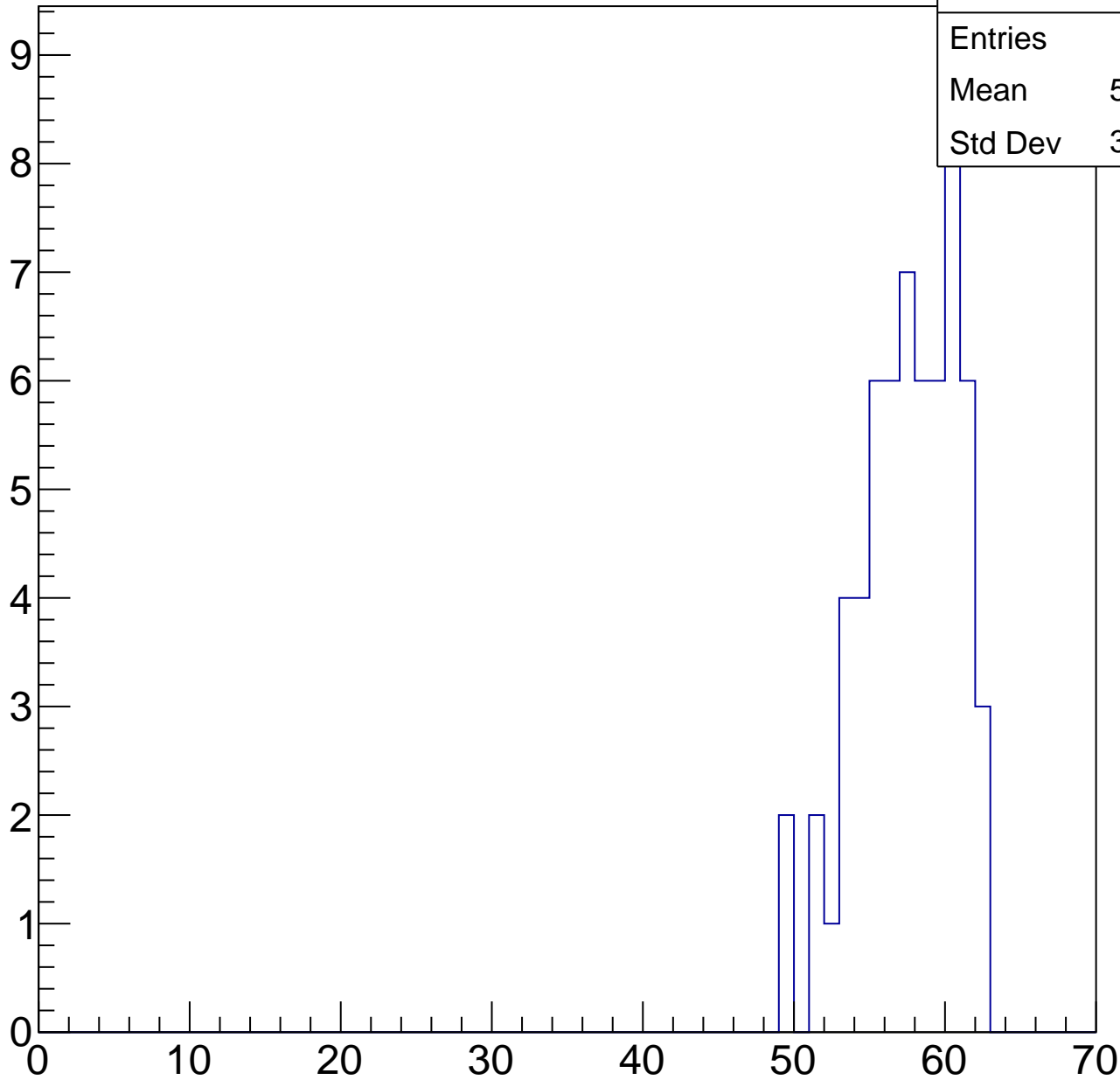
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	62
Mean	57.08
Std Dev	3.204

ampl

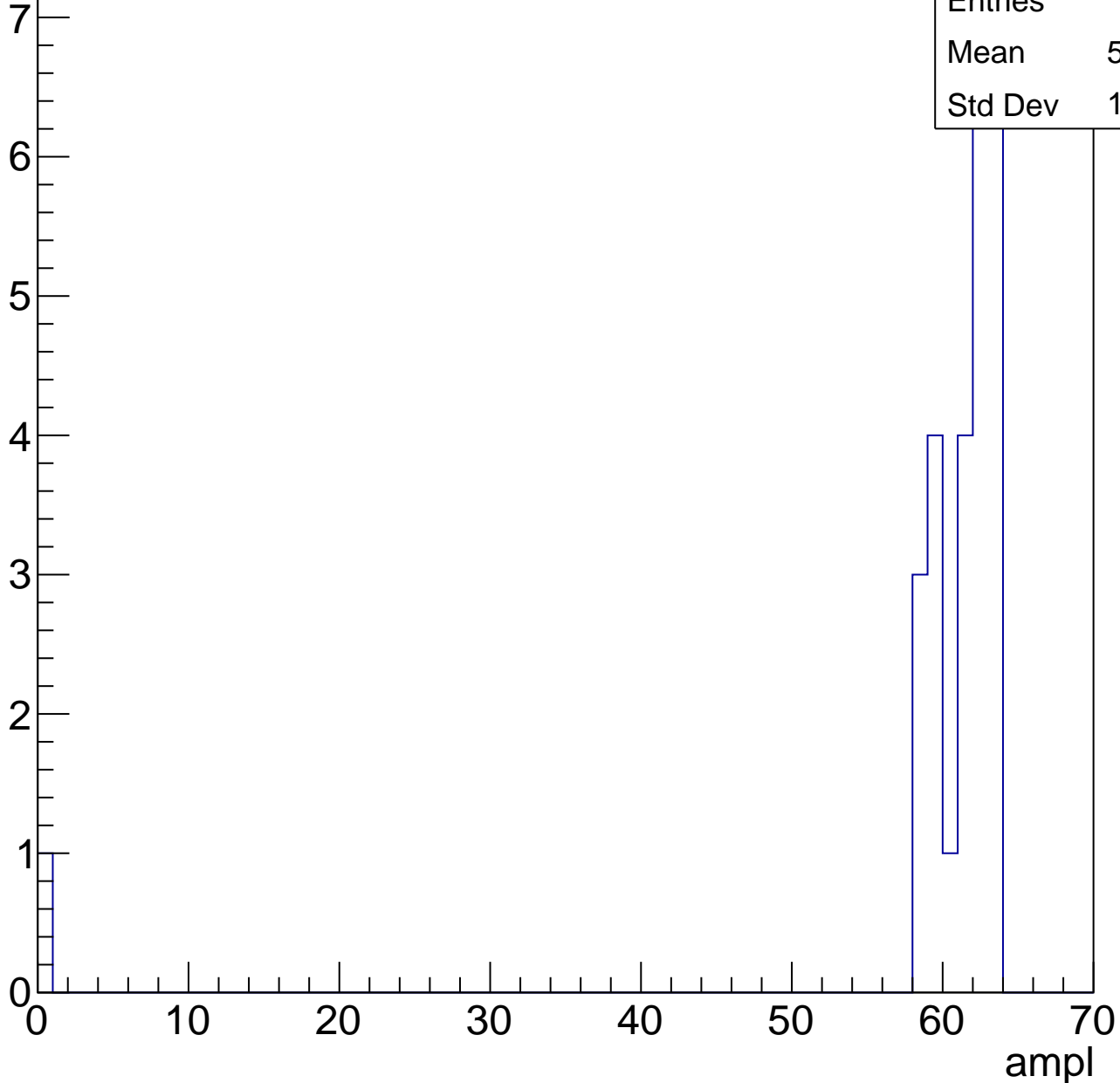


# B0L001S, U10-ch76, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	27
Mean	58.85
Std Dev	11.67



# B0L001S, U10-ch76, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	63
Std Dev	0

ampl



# B0L001S, U10-ch76, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U10-ch77, adc0

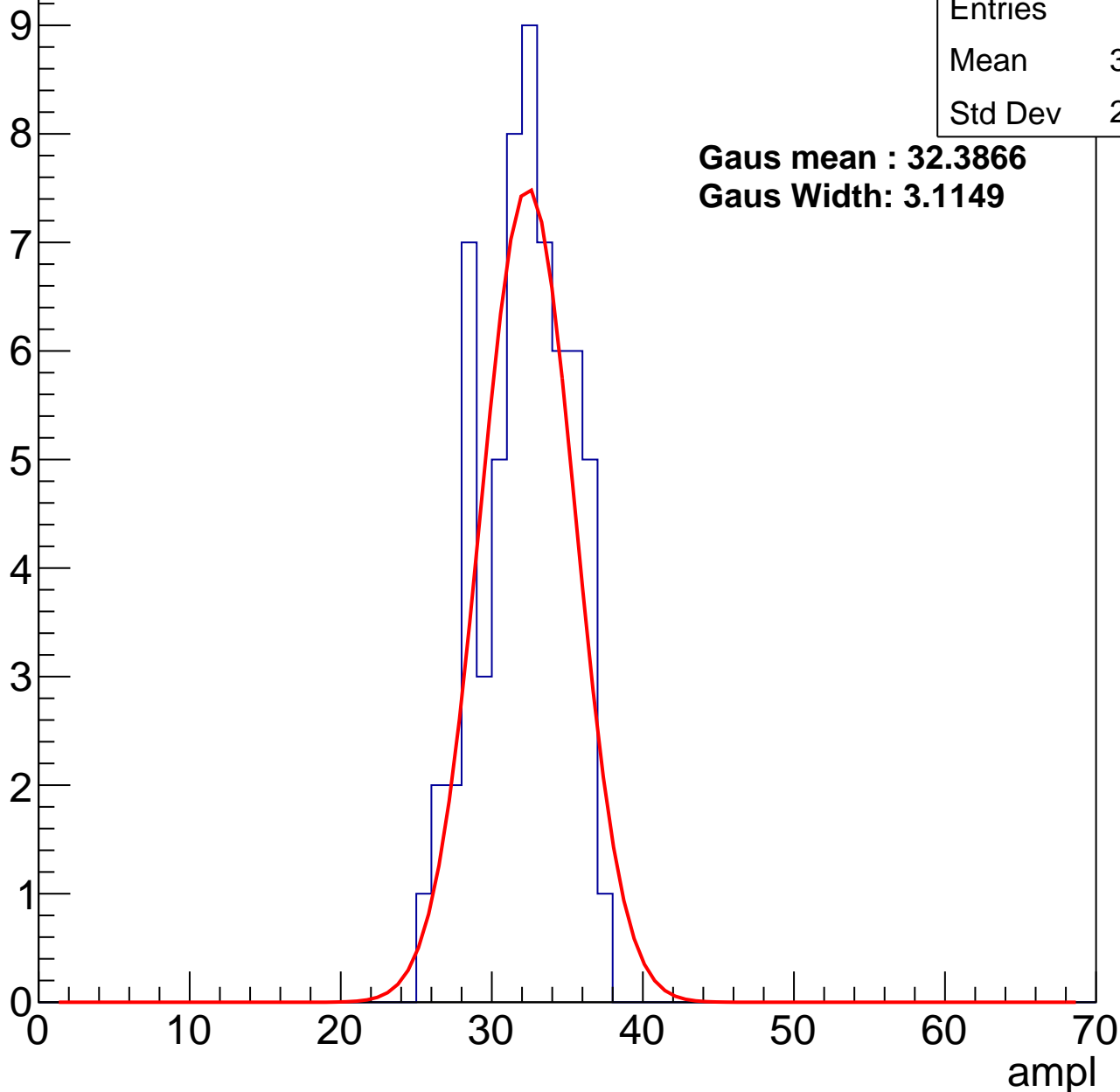
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	31.65
Std Dev	2.897

**Gaus mean : 32.3866**

**Gaus Width: 3.1149**



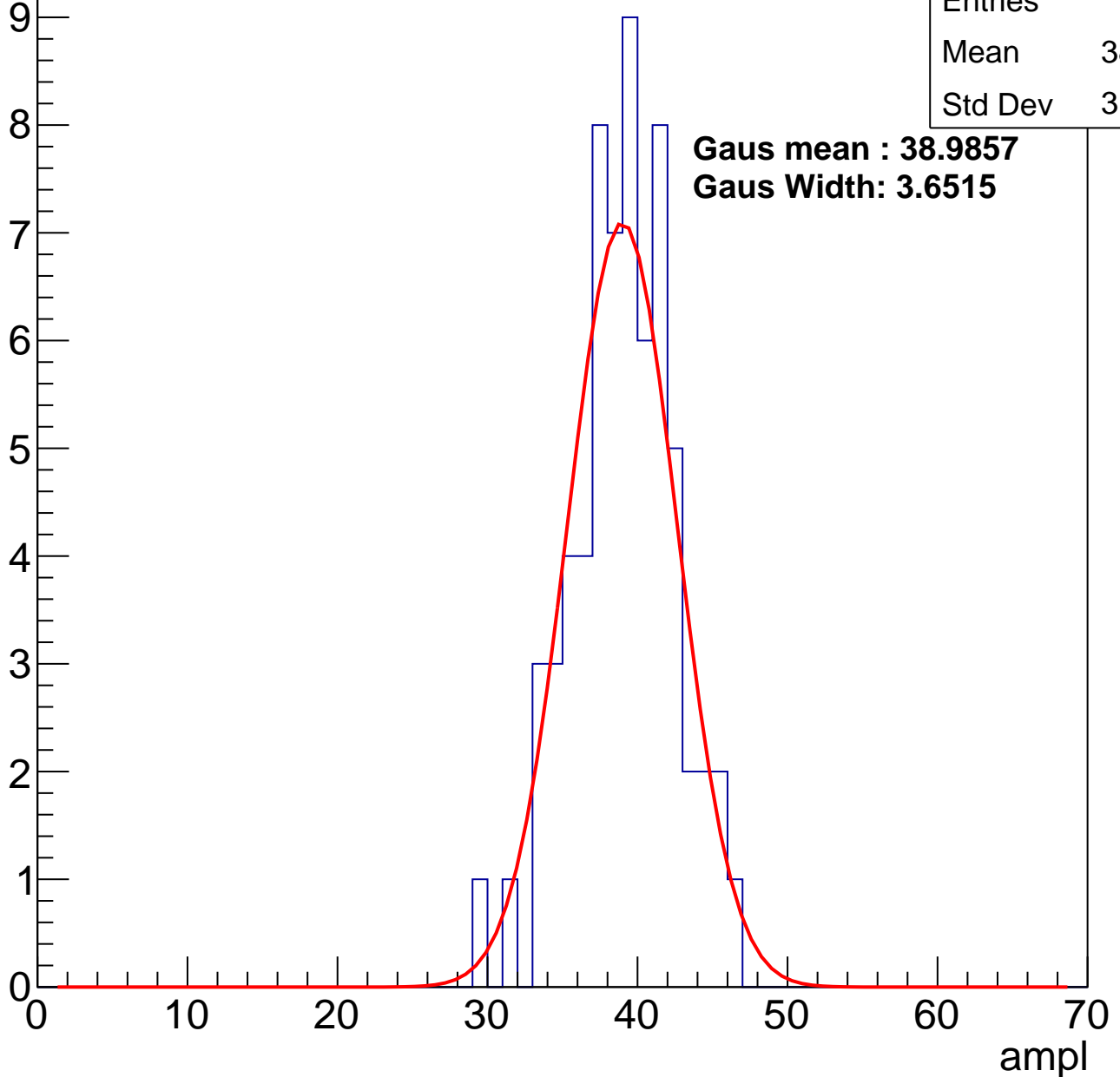
# B0L001S, U10-ch77, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	38.58
Std Dev	3.394

**Gaus mean : 38.9857**  
**Gaus Width: 3.6515**



# B0L001S, U10-ch77, adc2

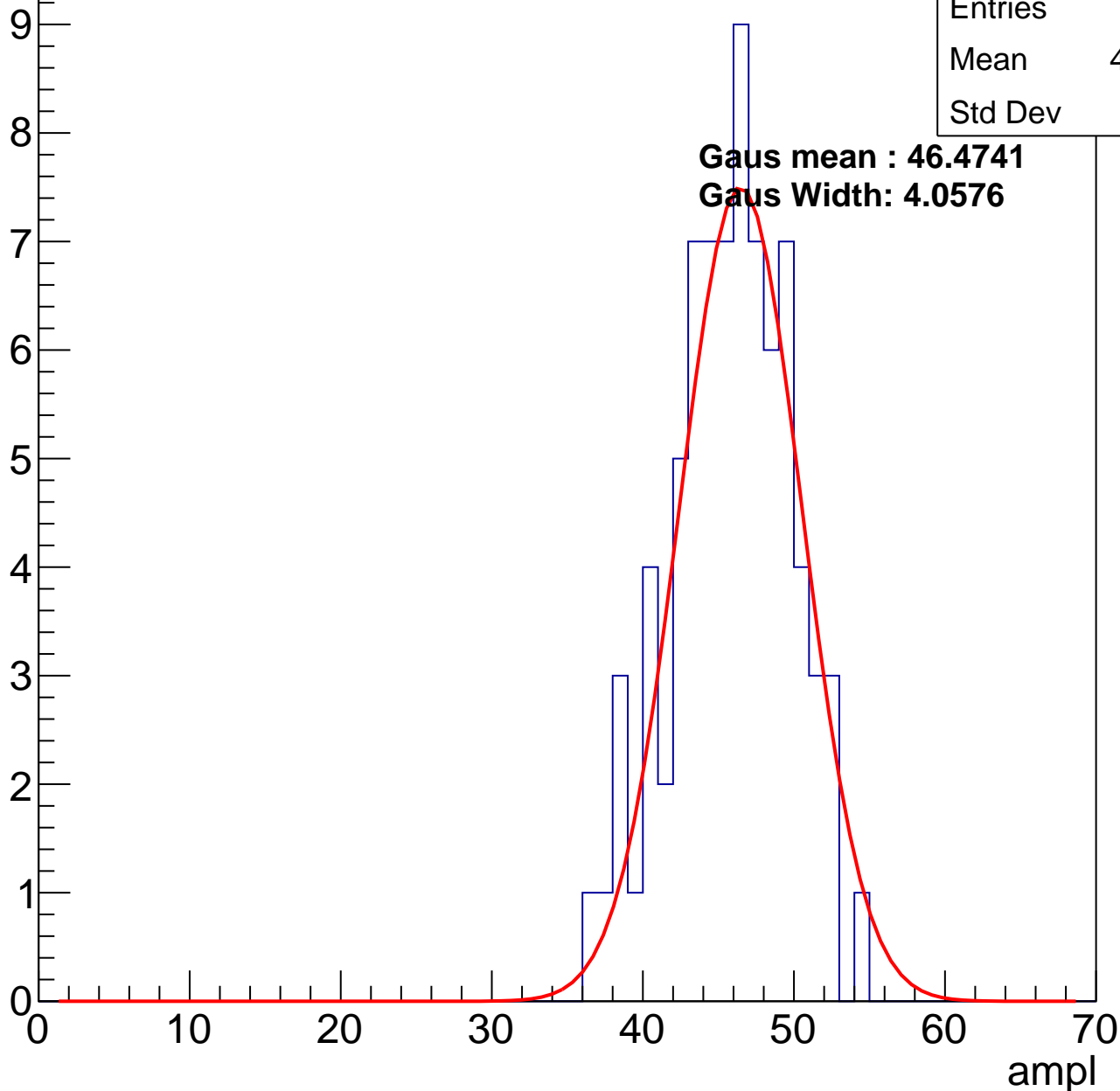
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	78
Mean	45.37
Std Dev	3.87

**Gaus mean : 46.4741**

**Gaus Width: 4.0576**

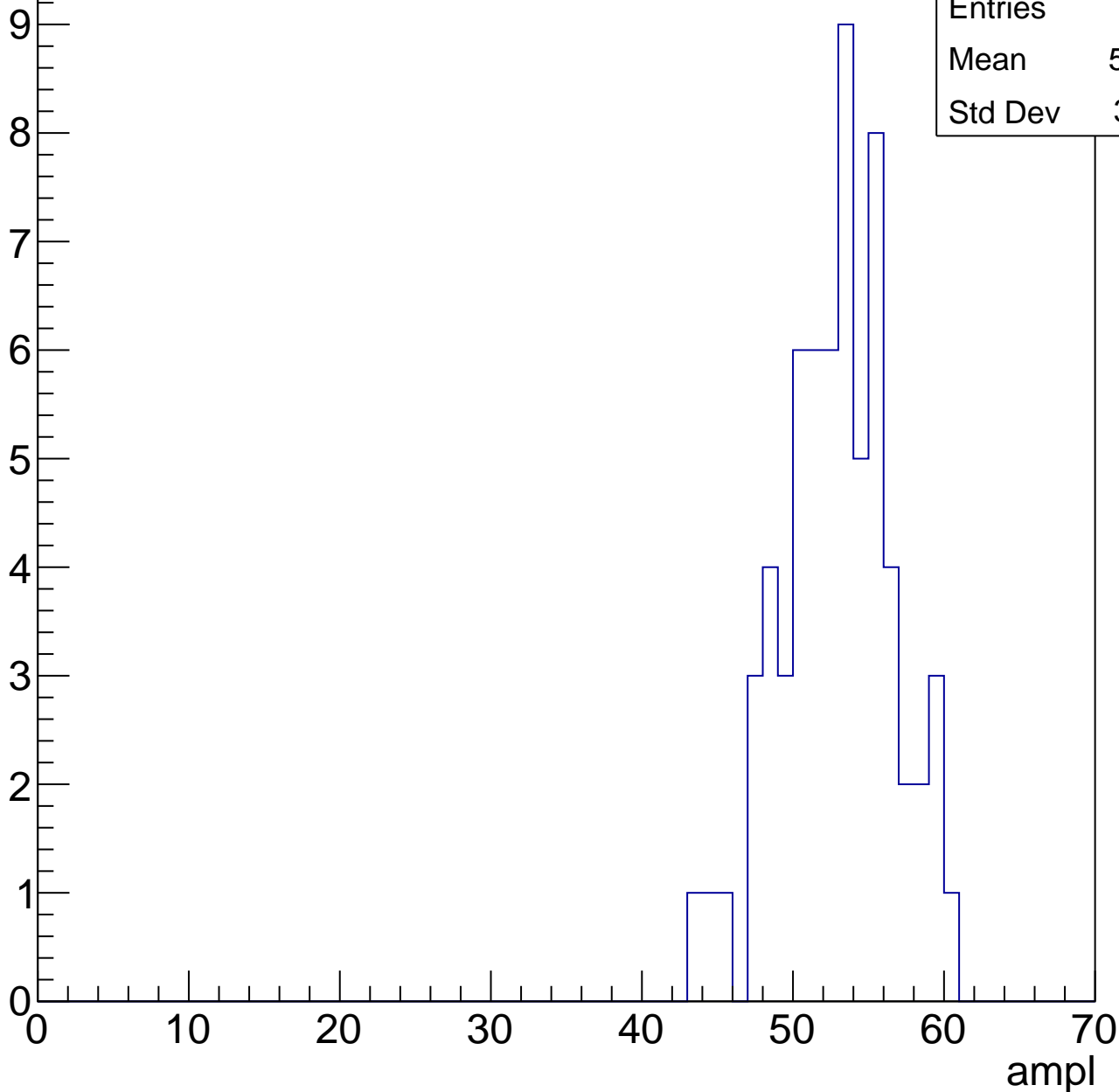


# B0L001S, U10-ch77, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	52.43
Std Dev	3.671

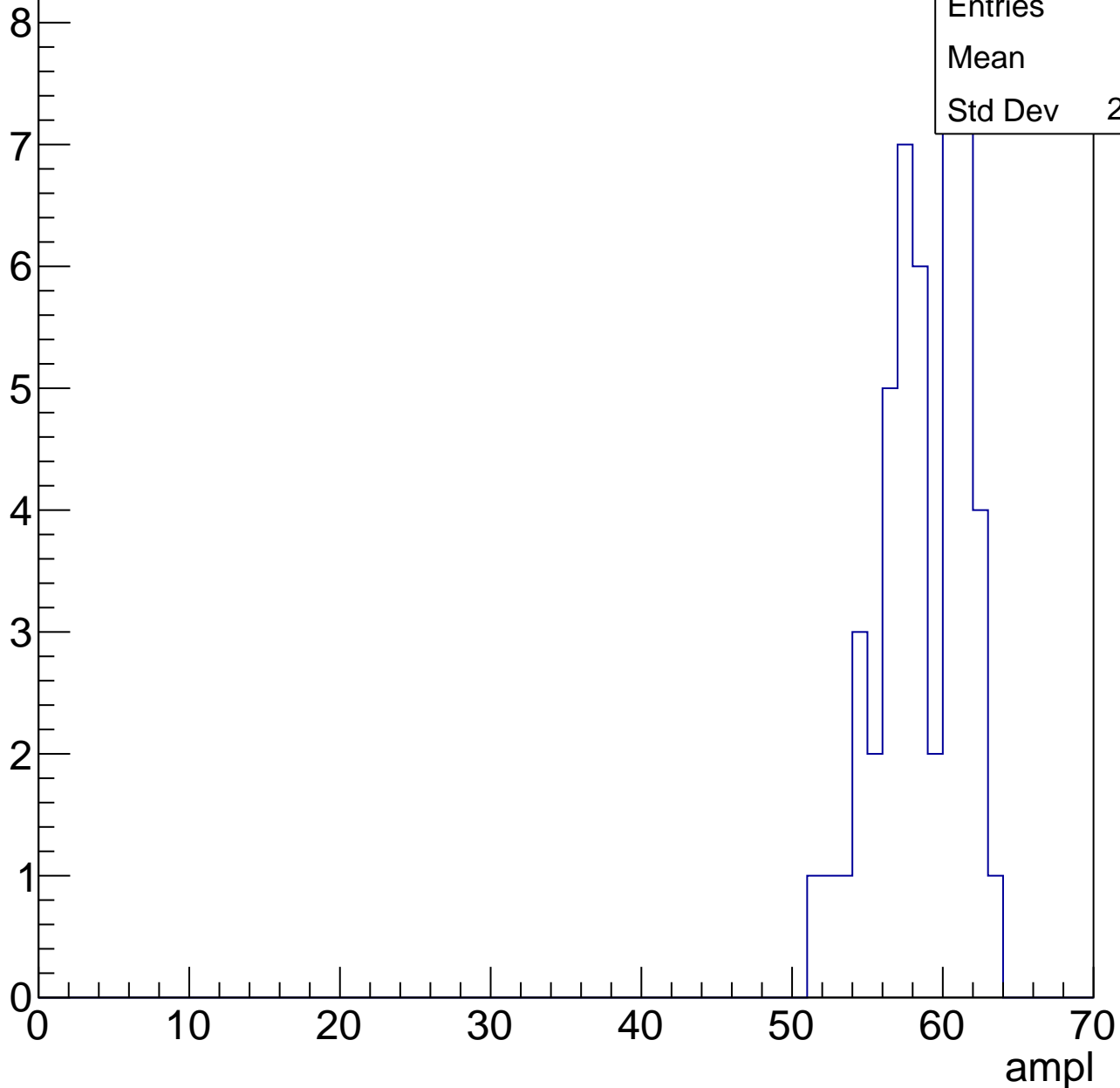


# B0L001S, U10-ch77, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	49
Mean	58.2
Std Dev	2.843

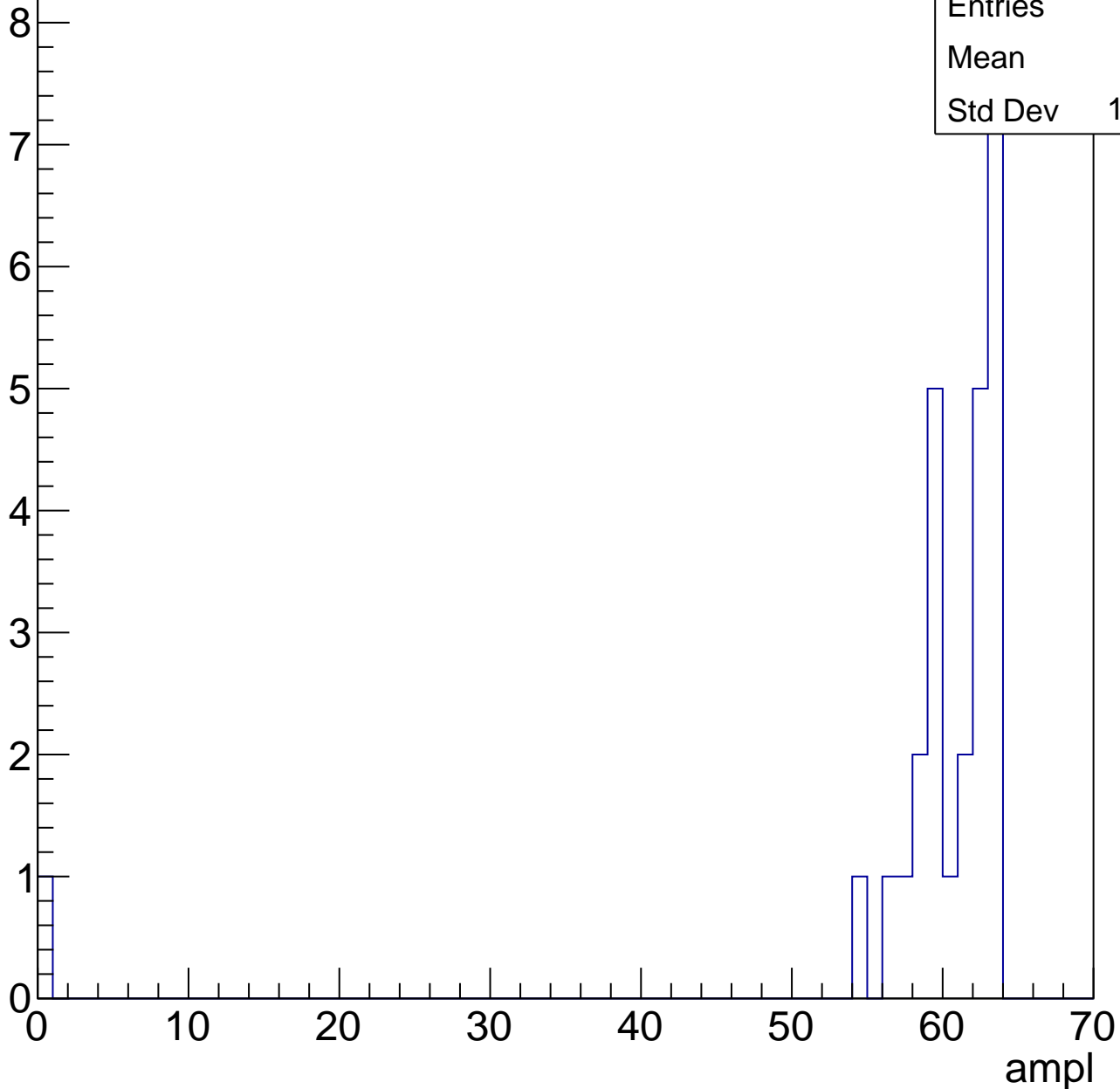


# B0L001S, U10-ch77, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	27
Mean	58.3
Std Dev	11.69



# B0L001S, U10-ch77, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch77, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U10-ch78, adc0

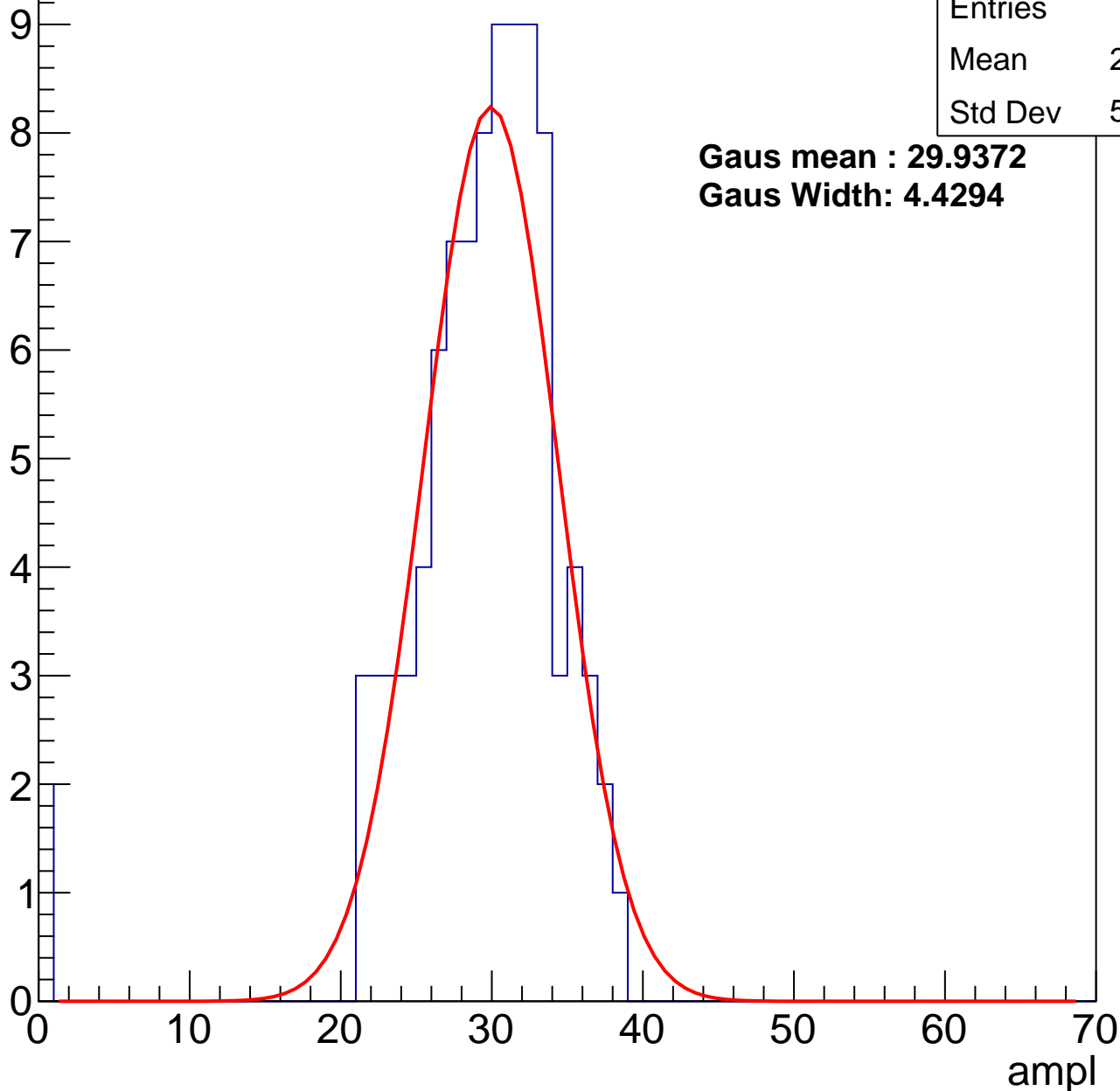
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	94
Mean	28.79
Std Dev	5.818

**Gaus mean : 29.9372**

**Gaus Width: 4.4294**



# B0L001S, U10-ch78, adc1

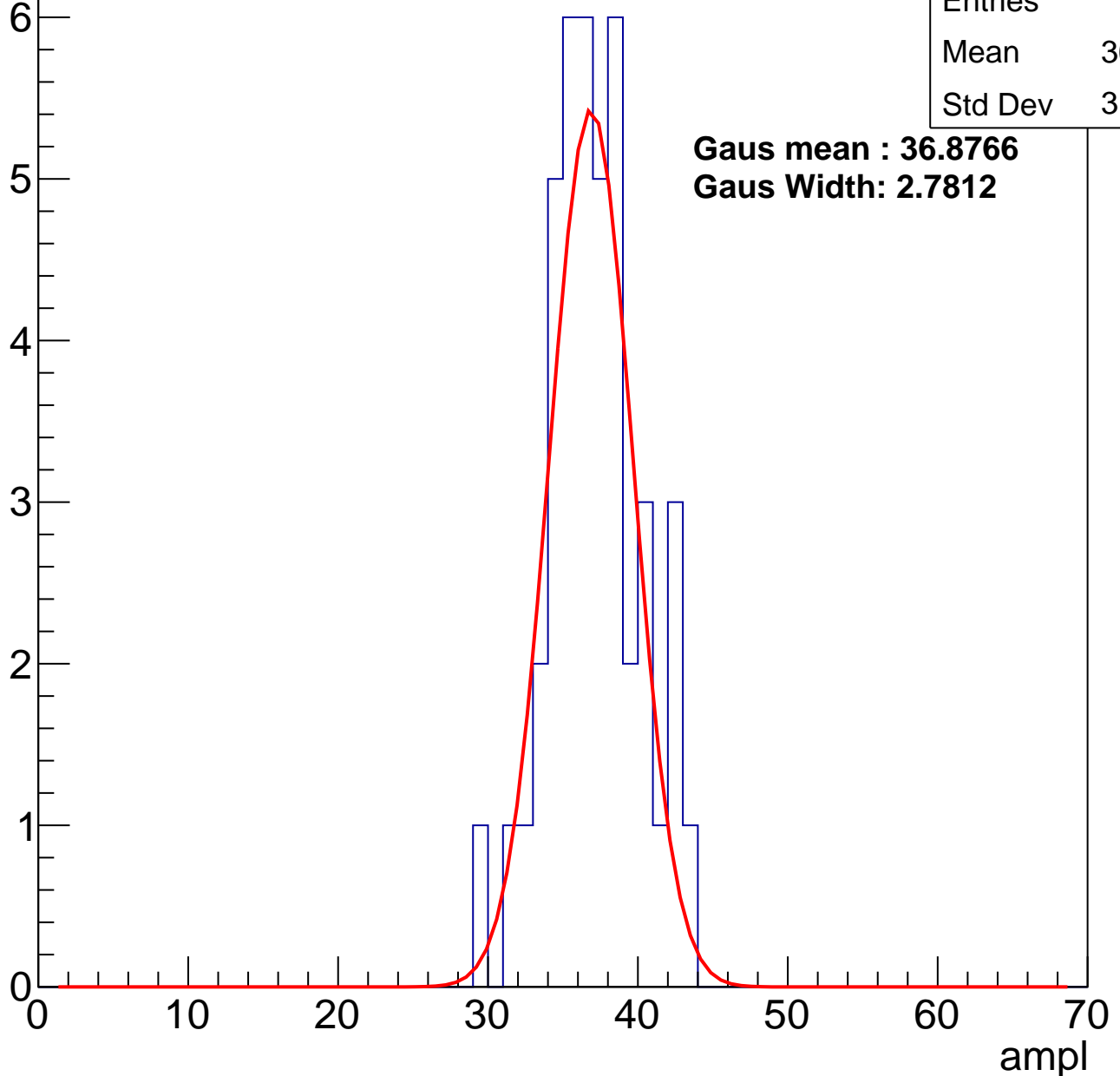
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	43
Mean	36.63
Std Dev	3.027

**Gaus mean : 36.8766**

**Gaus Width: 2.7812**



# B0L001S, U10-ch78, adc2

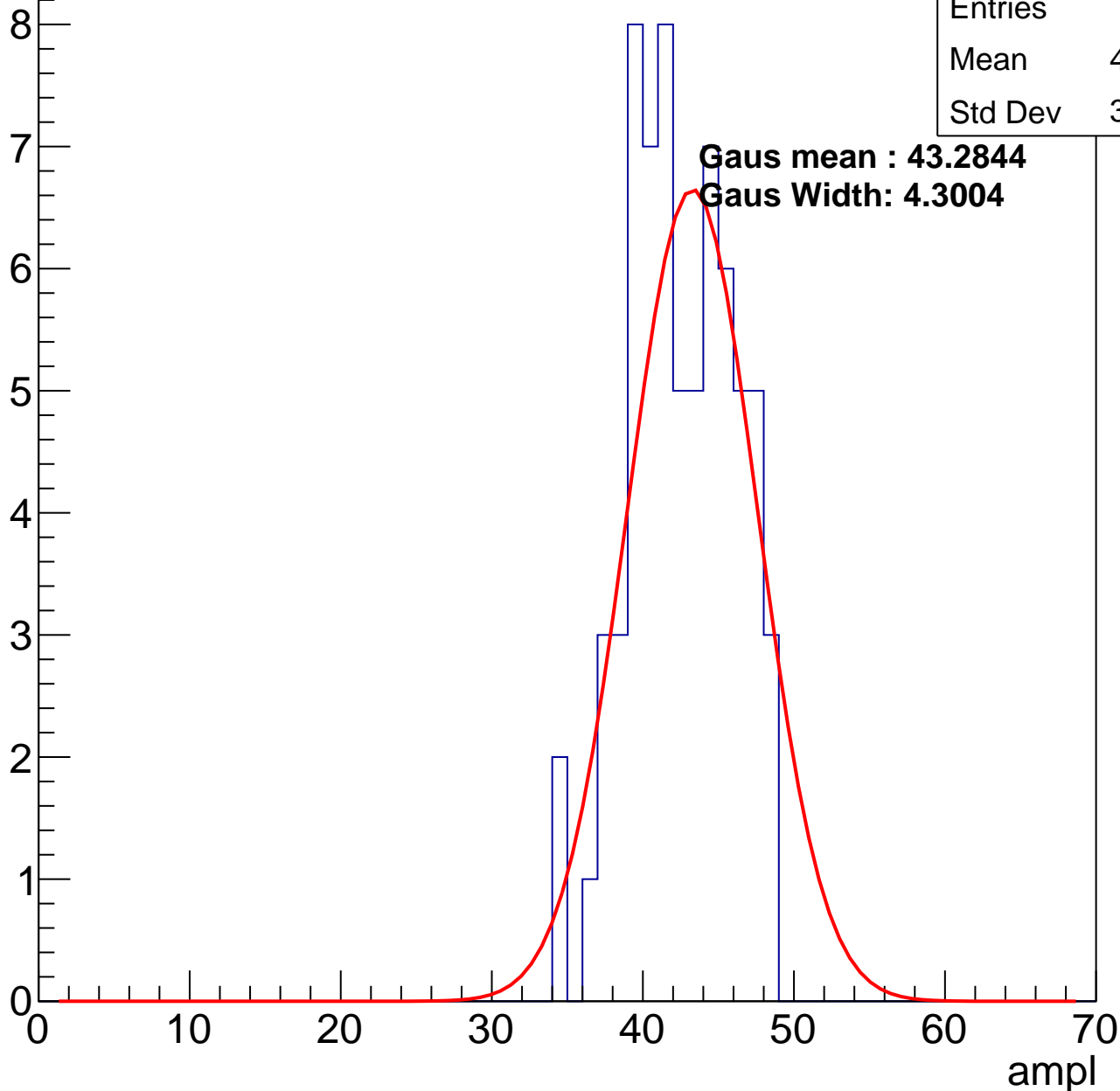
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	42.07
Std Dev	3.418

**Gaus mean : 43.2844**

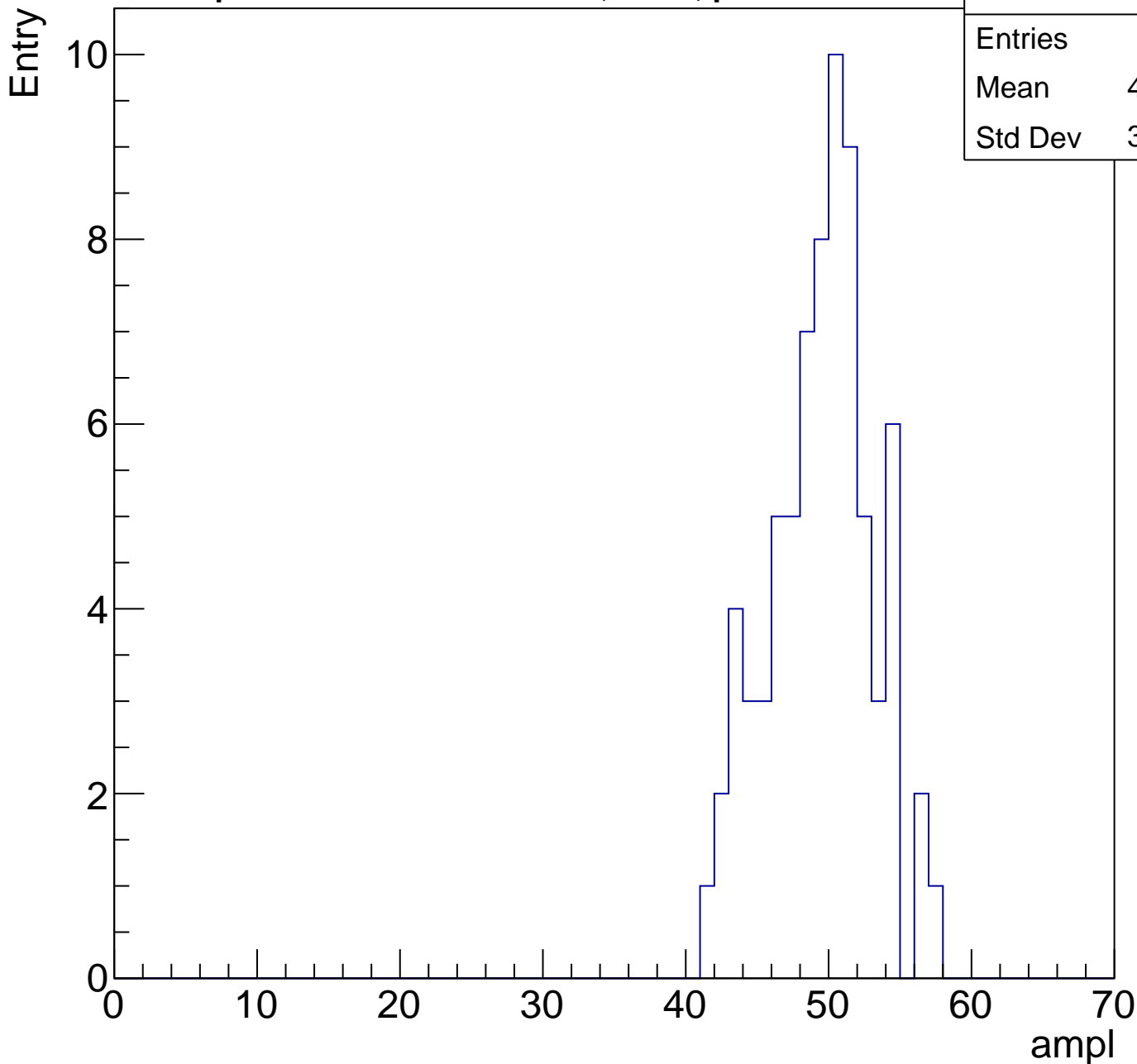
**Gaus Width: 4.3004**



# B0L001S, U10-ch78, adc3

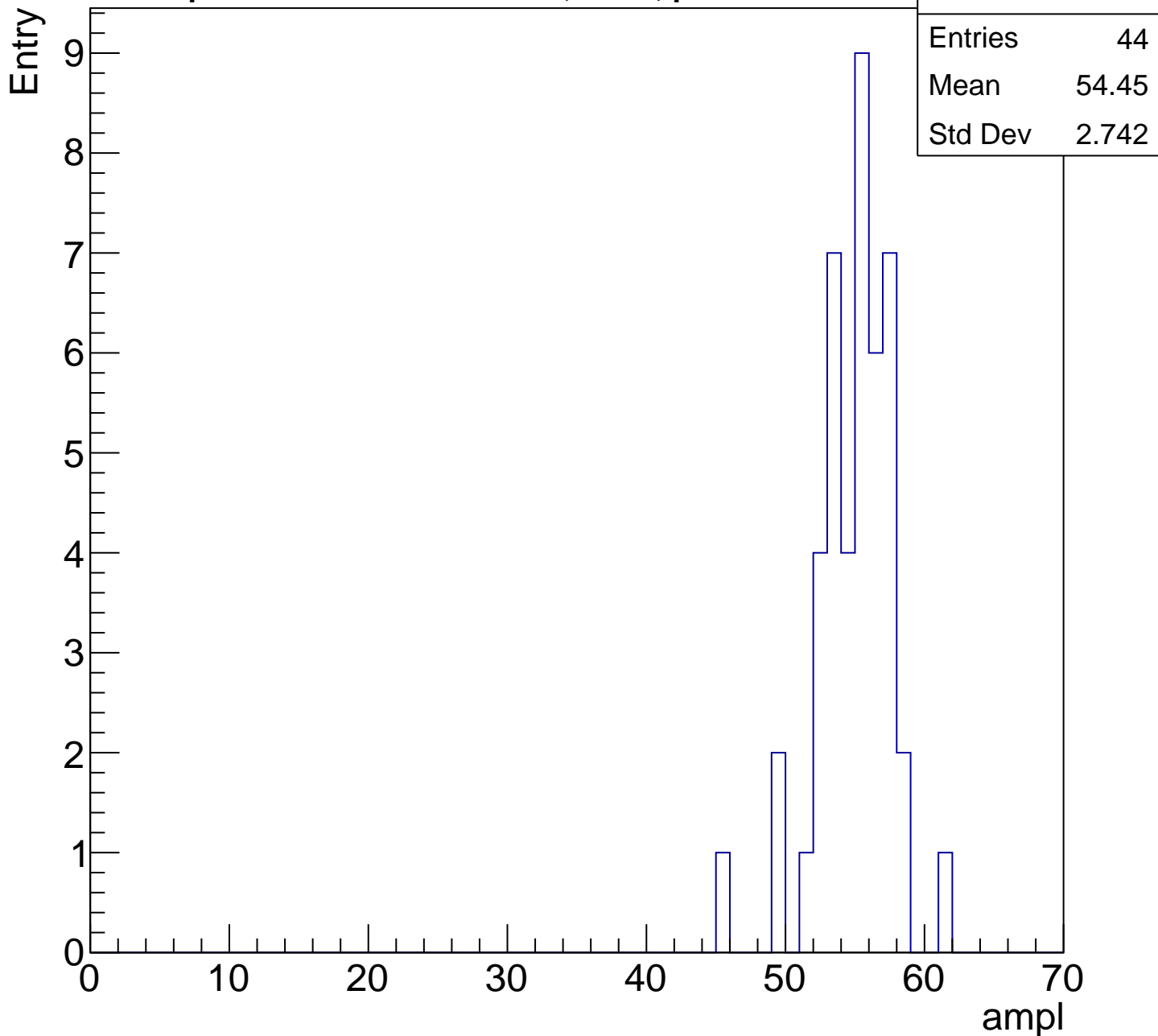
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	74
Mean	49.03
Std Dev	3.587



# B0L001S, U10-ch78, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

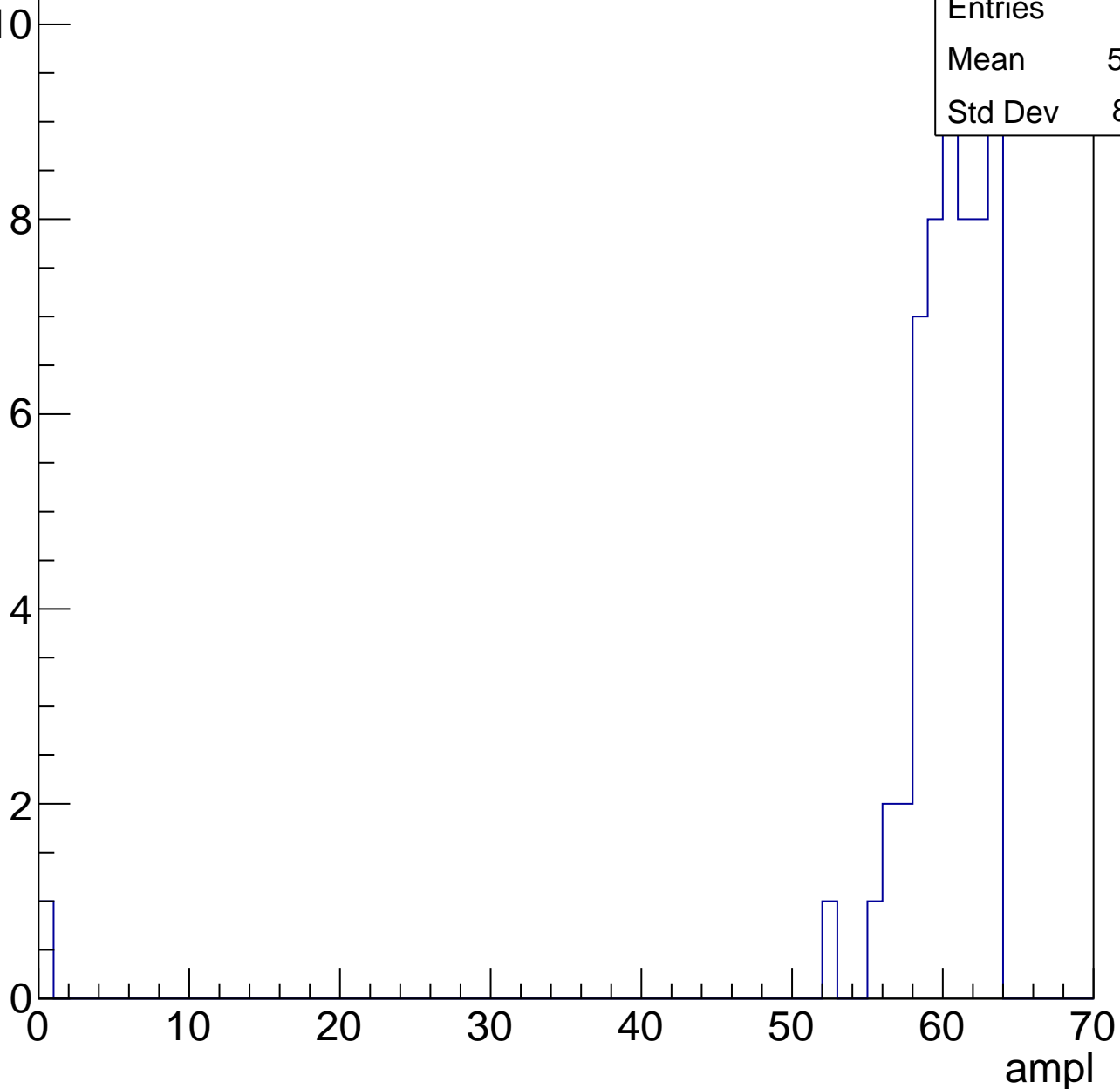


# B0L001S, U10-ch78, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	59.04
Std Dev	8.221



# B0L001S, U10-ch78, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	7
Mean	60.14
Std Dev	1.457

ampl

0 10 20 30 40 50 60 70



# B0L001S, U10-ch78, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U10-ch79, adc0

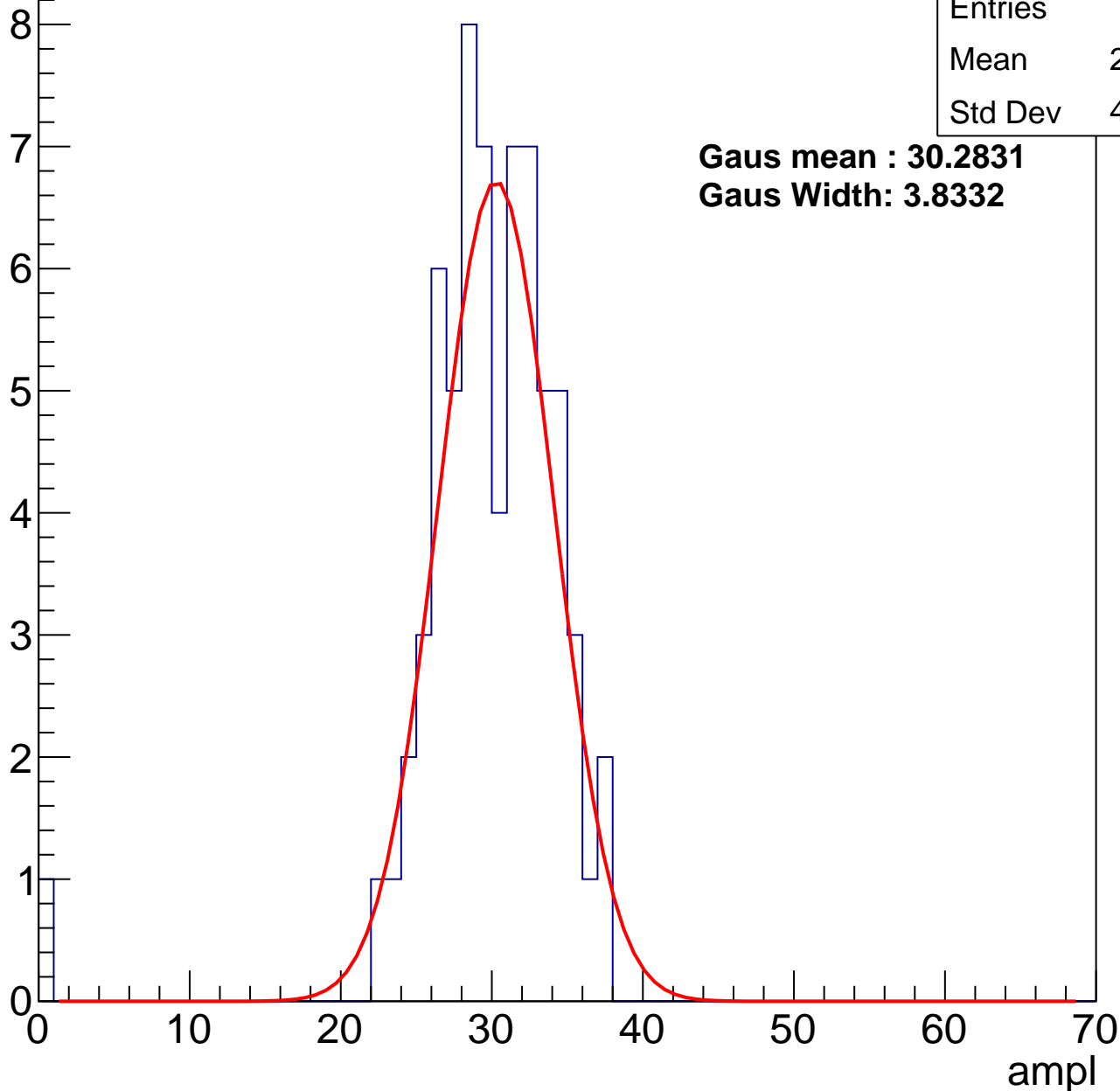
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	29.37
Std Dev	4.973

**Gaus mean : 30.2831**

**Gaus Width: 3.8332**



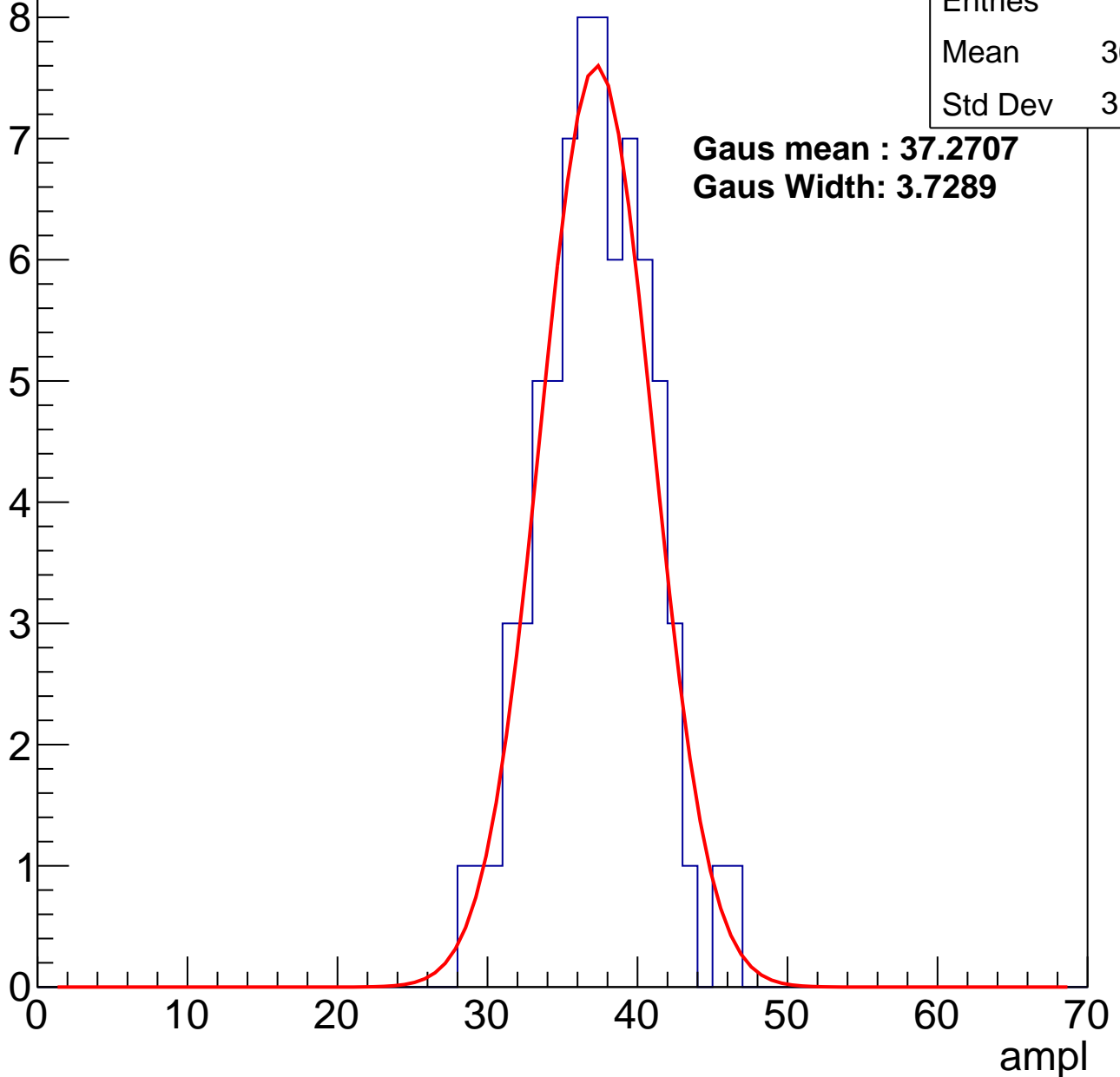
# B0L001S, U10-ch79, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	36.75
Std Dev	3.647

**Gaus mean : 37.2707**  
**Gaus Width: 3.7289**



# B0L001S, U10-ch79, adc2

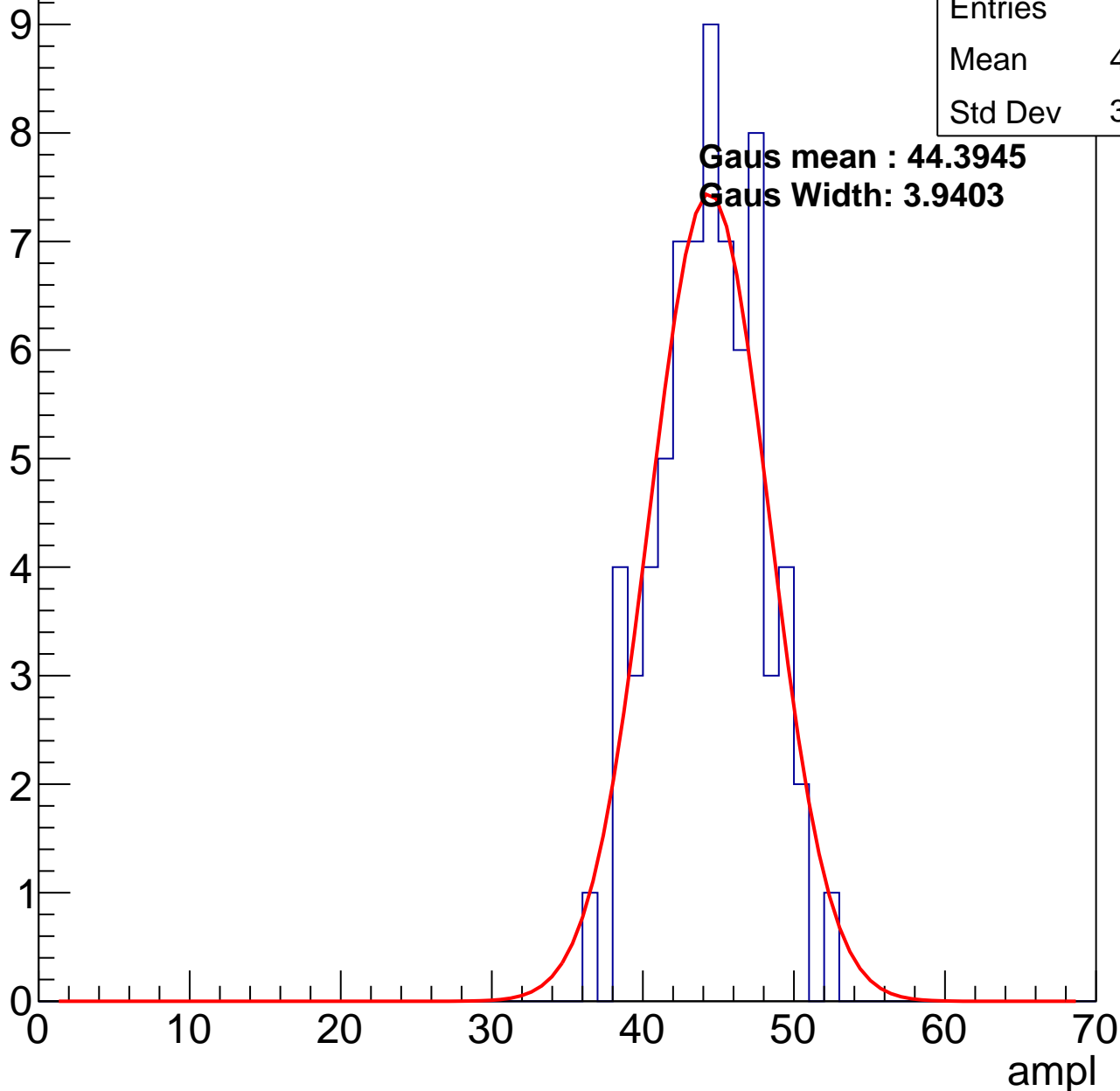
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	43.94
Std Dev	3.386

**Gaus mean : 44.3945**

**Gaus Width: 3.9403**

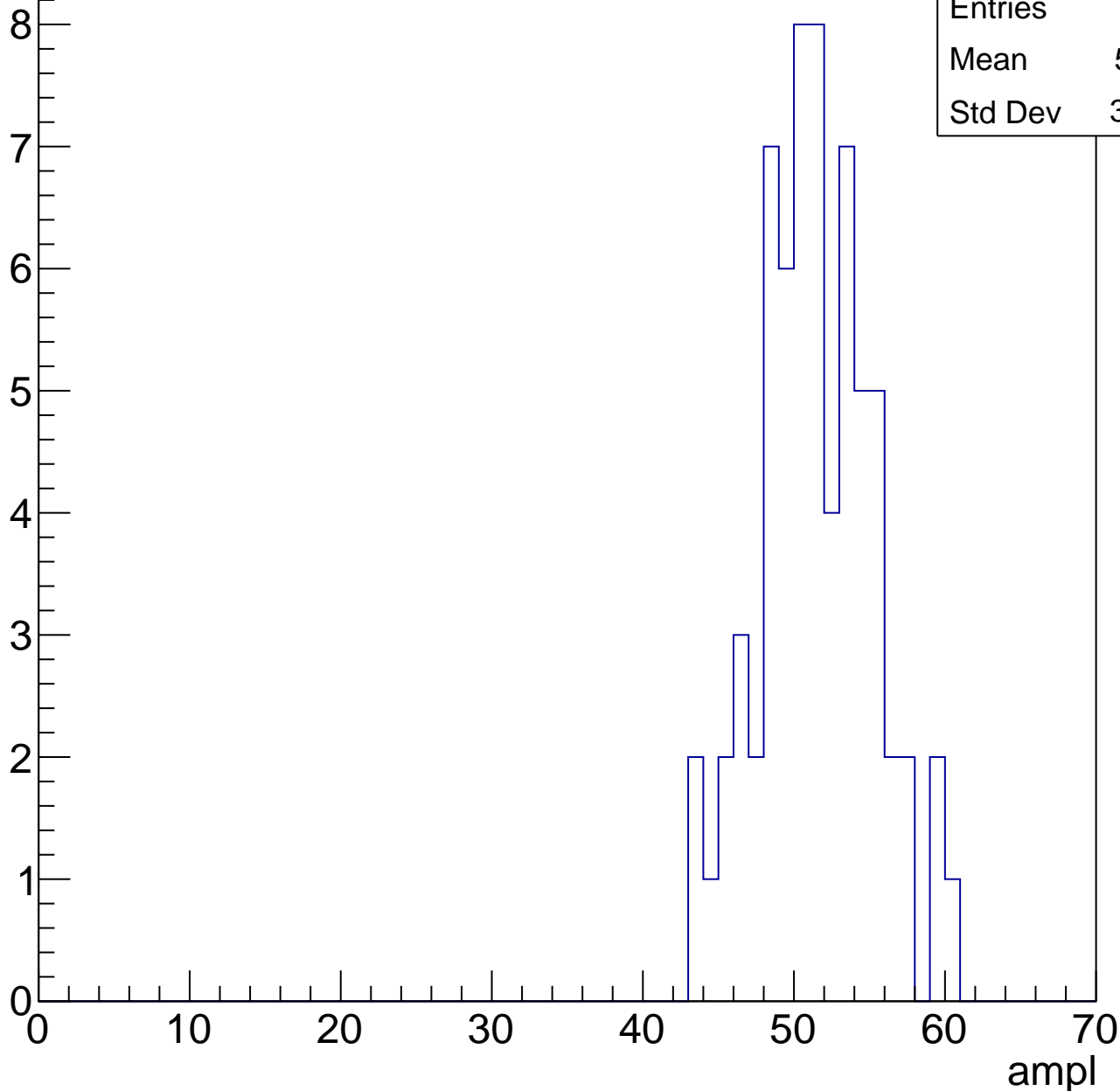


# B0L001S, U10-ch79, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	51.01
Std Dev	3.744

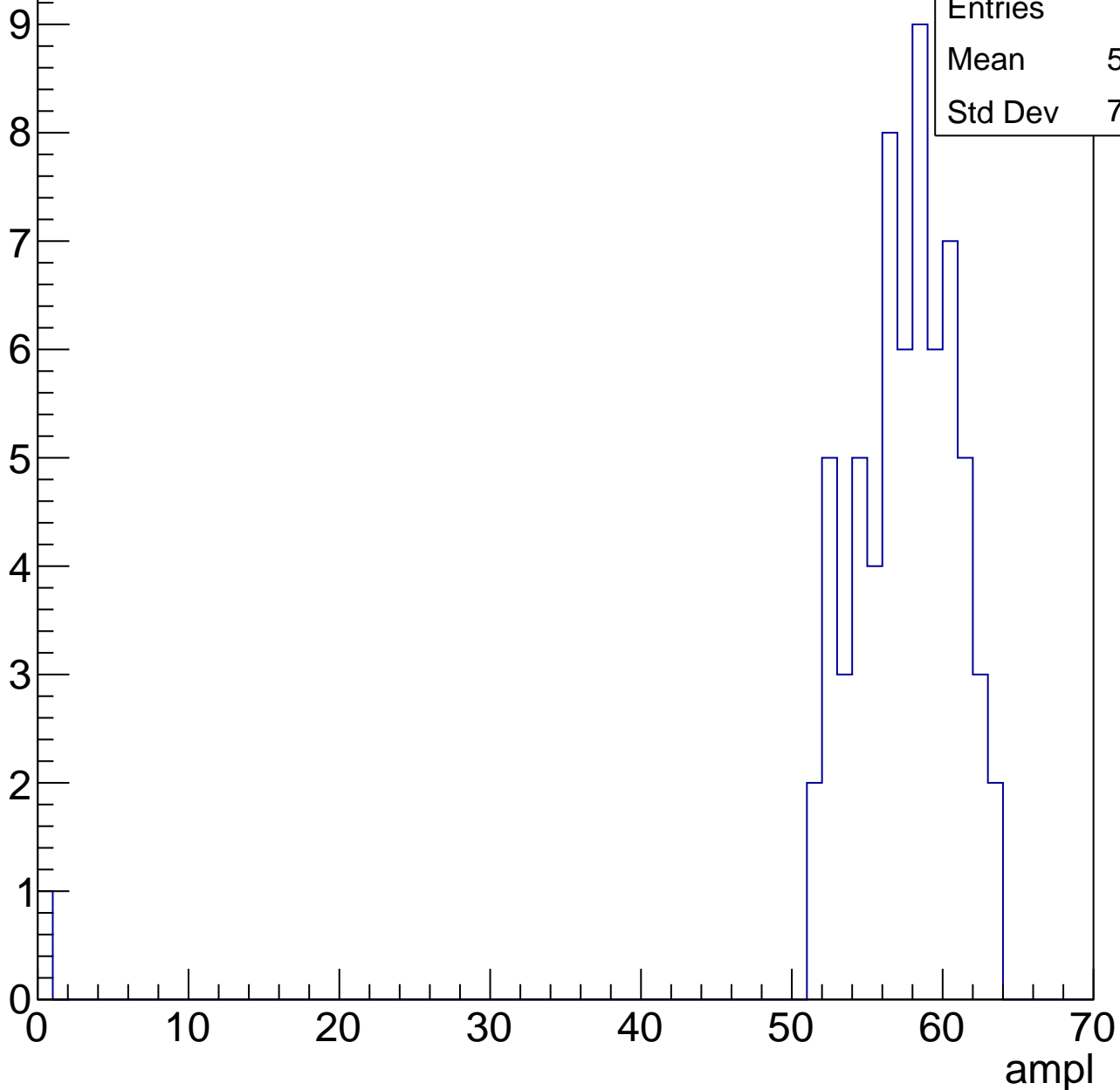


# B0L001S, U10-ch79, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	56.27
Std Dev	7.639

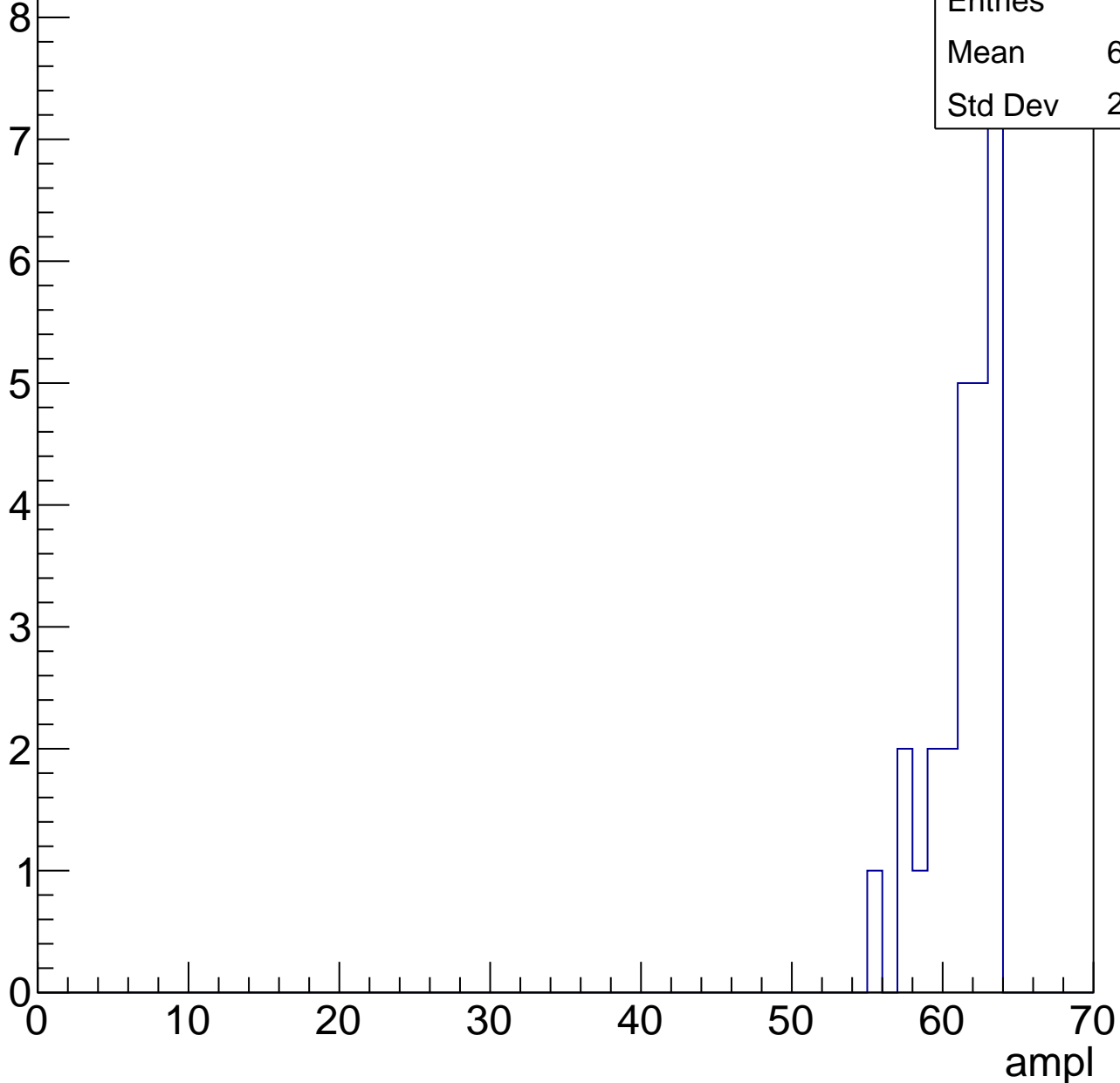


# B0L001S, U10-ch79, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	26
Mean	60.92
Std Dev	2.183



# B0L001S, U10-ch79, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	62
Std Dev	0

ampl



# B0L001S, U10-ch79, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L001S, U10-ch80, adc0

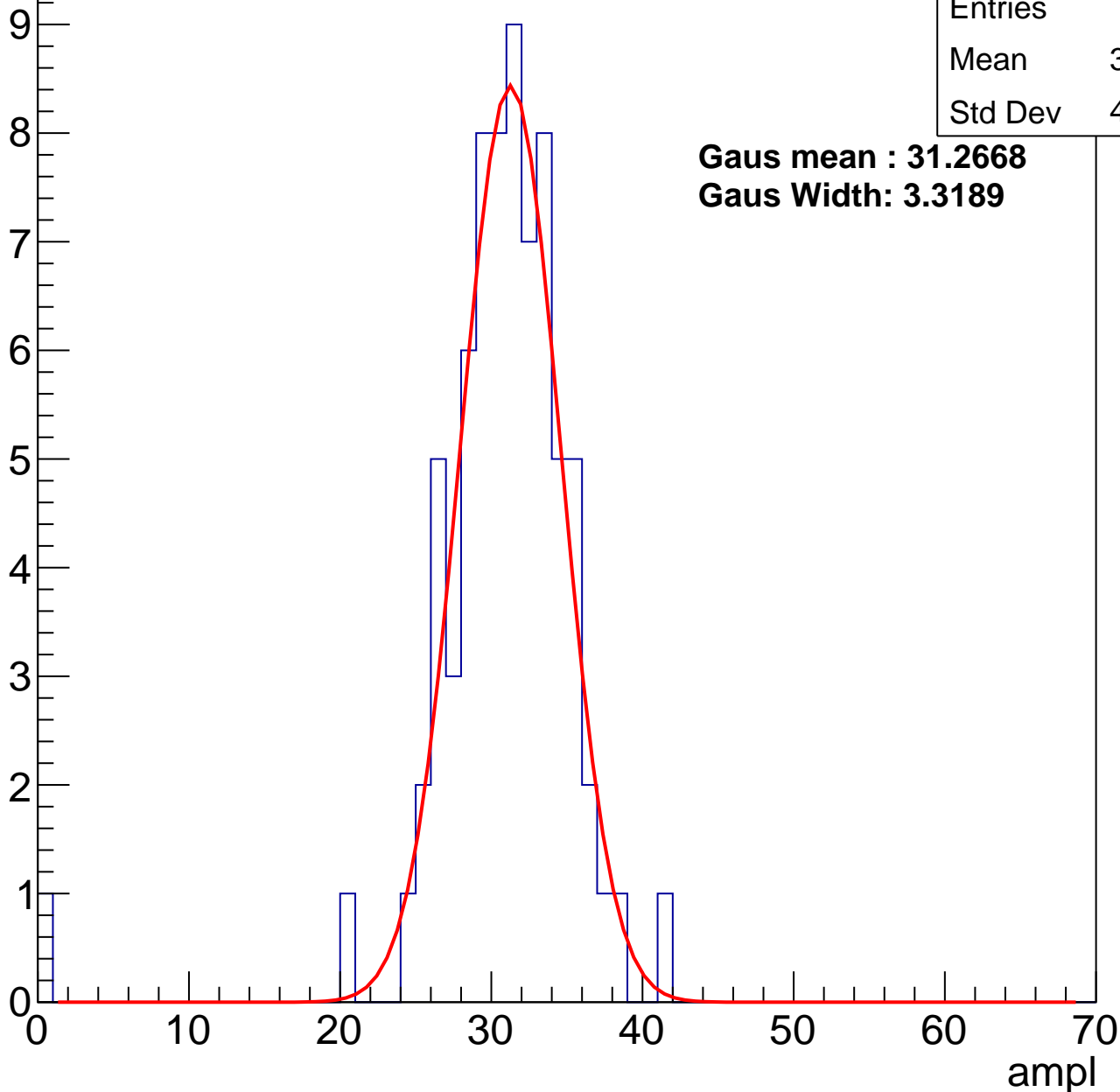
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	30.34
Std Dev	4.982

**Gaus mean : 31.2668**

**Gaus Width: 3.3189**

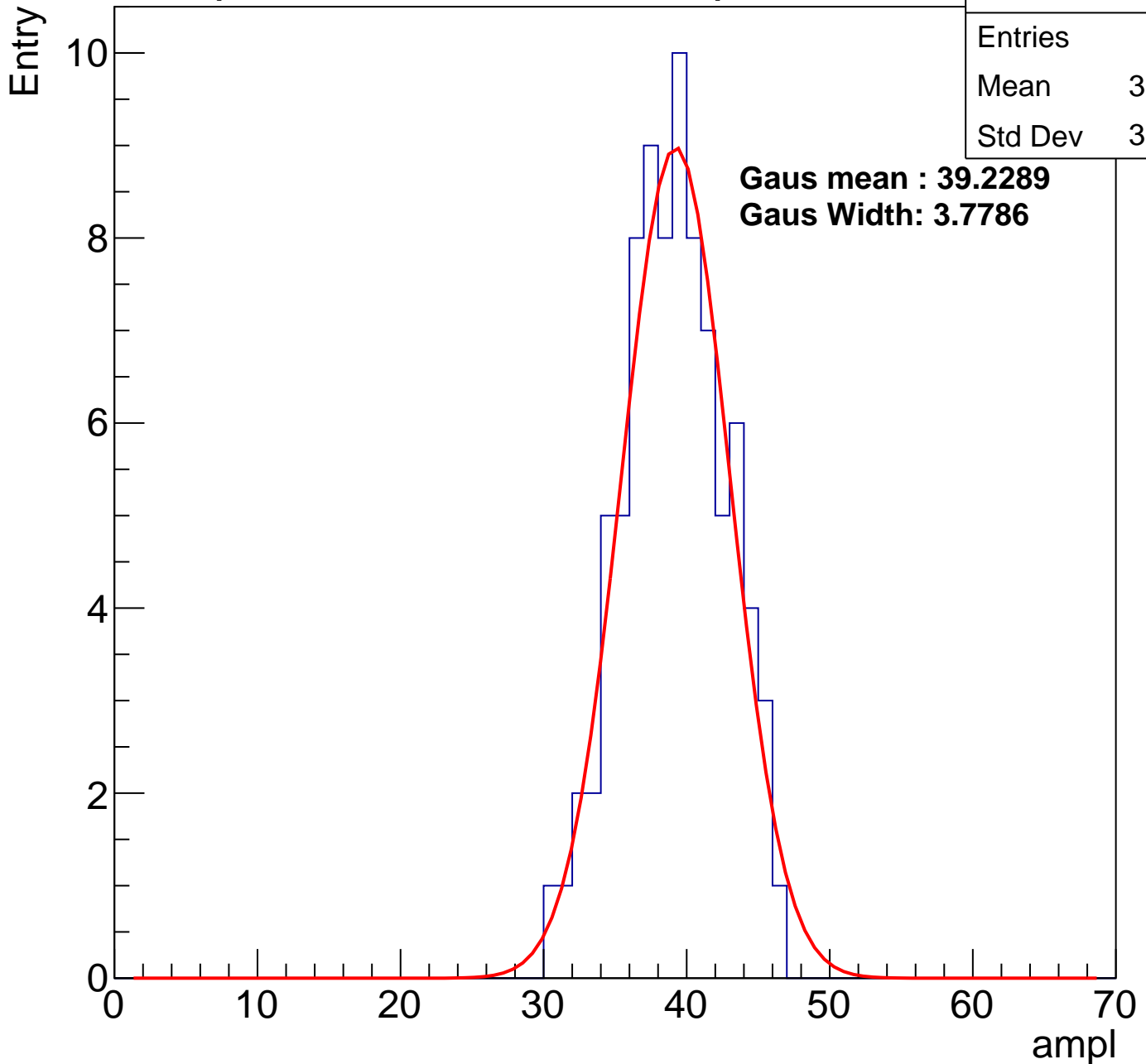


# B0L001S, U10-ch80, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	85
Mean	38.62
Std Dev	3.528

**Gaus mean : 39.2289**  
**Gaus Width: 3.7786**



# B0L001S, U10-ch80, adc2

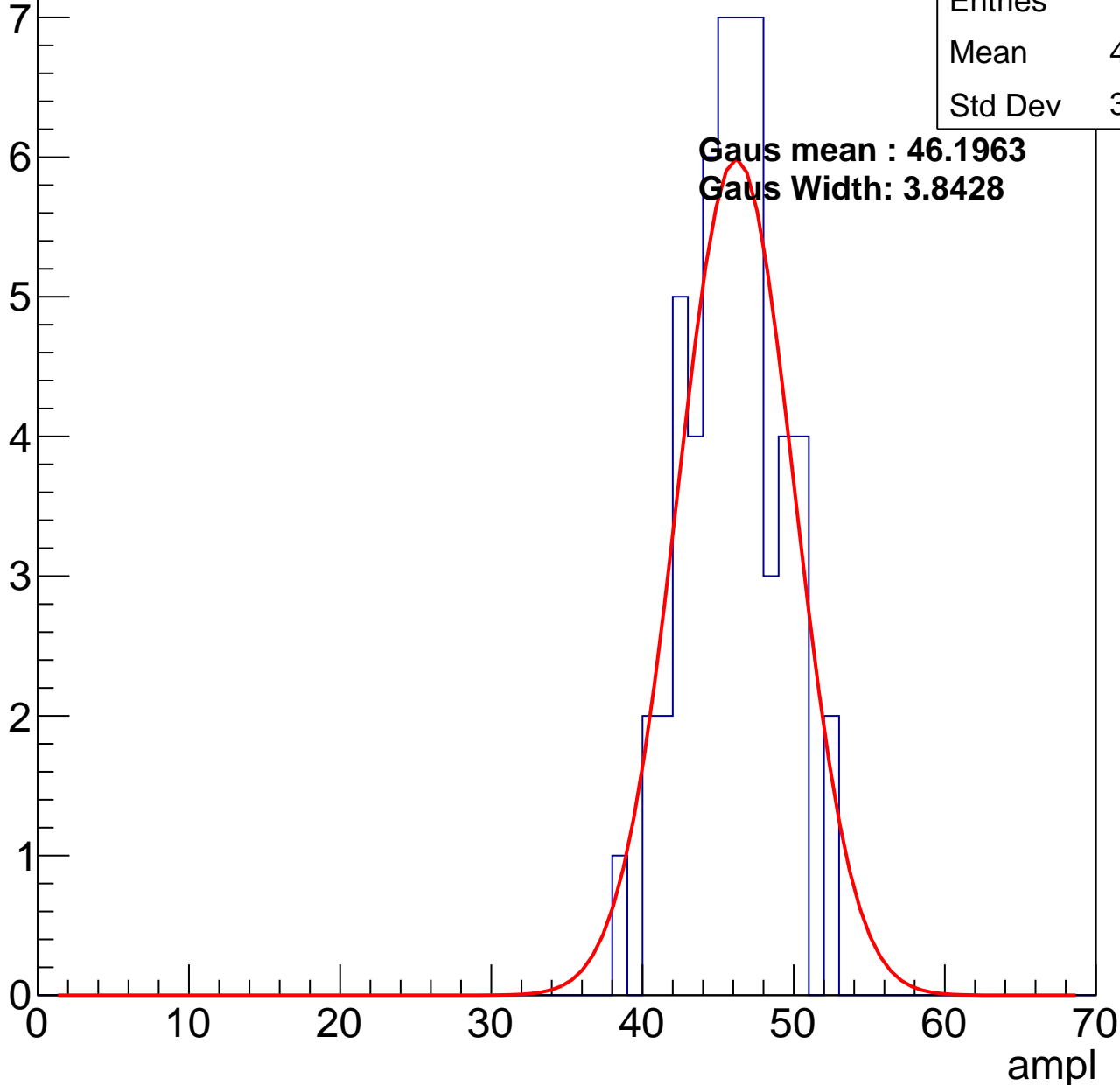
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	45.48
Std Dev	3.072

**Gaus mean : 46.1963**

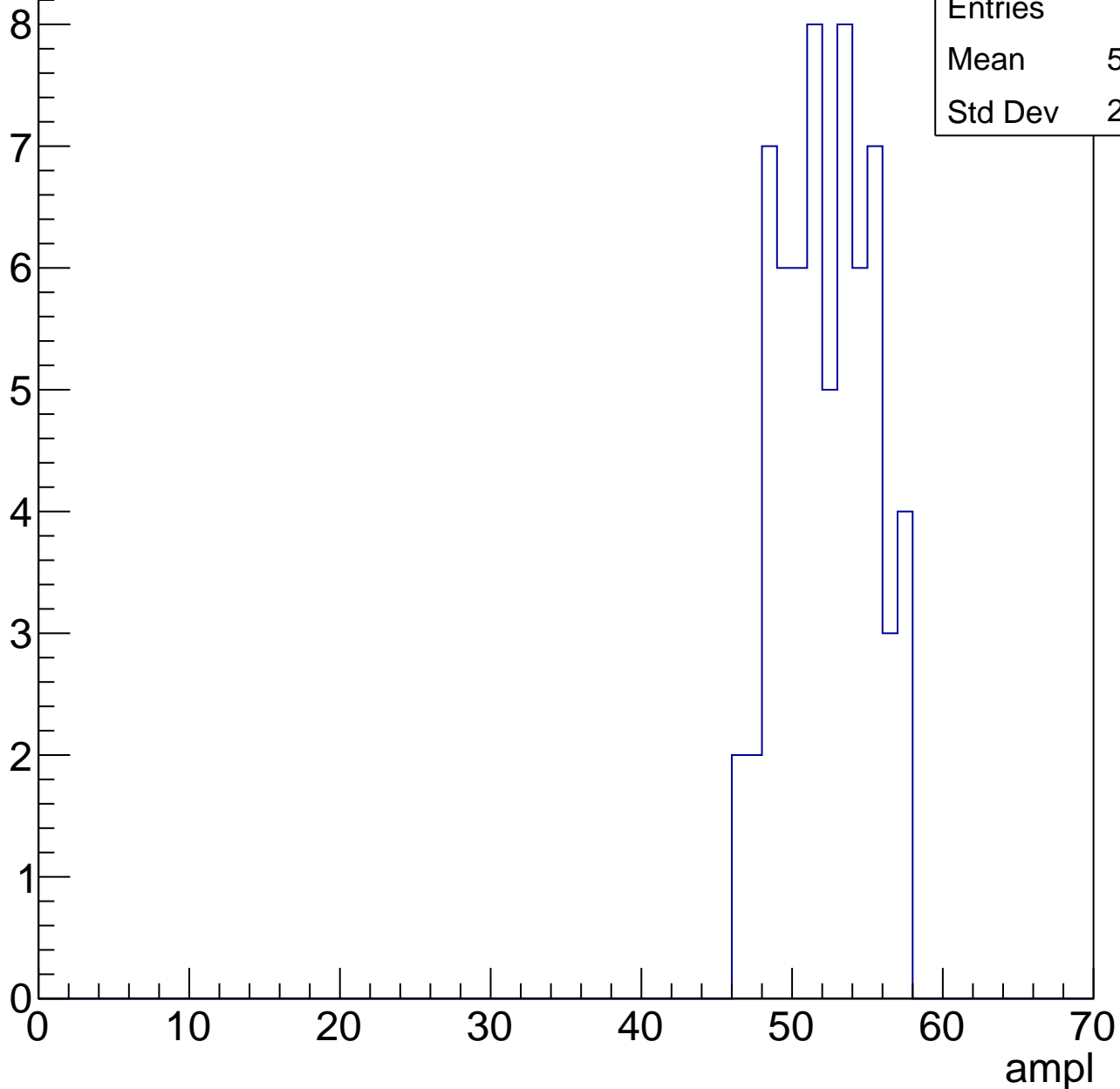
**Gaus Width: 3.8428**



# B0L001S, U10-ch80, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

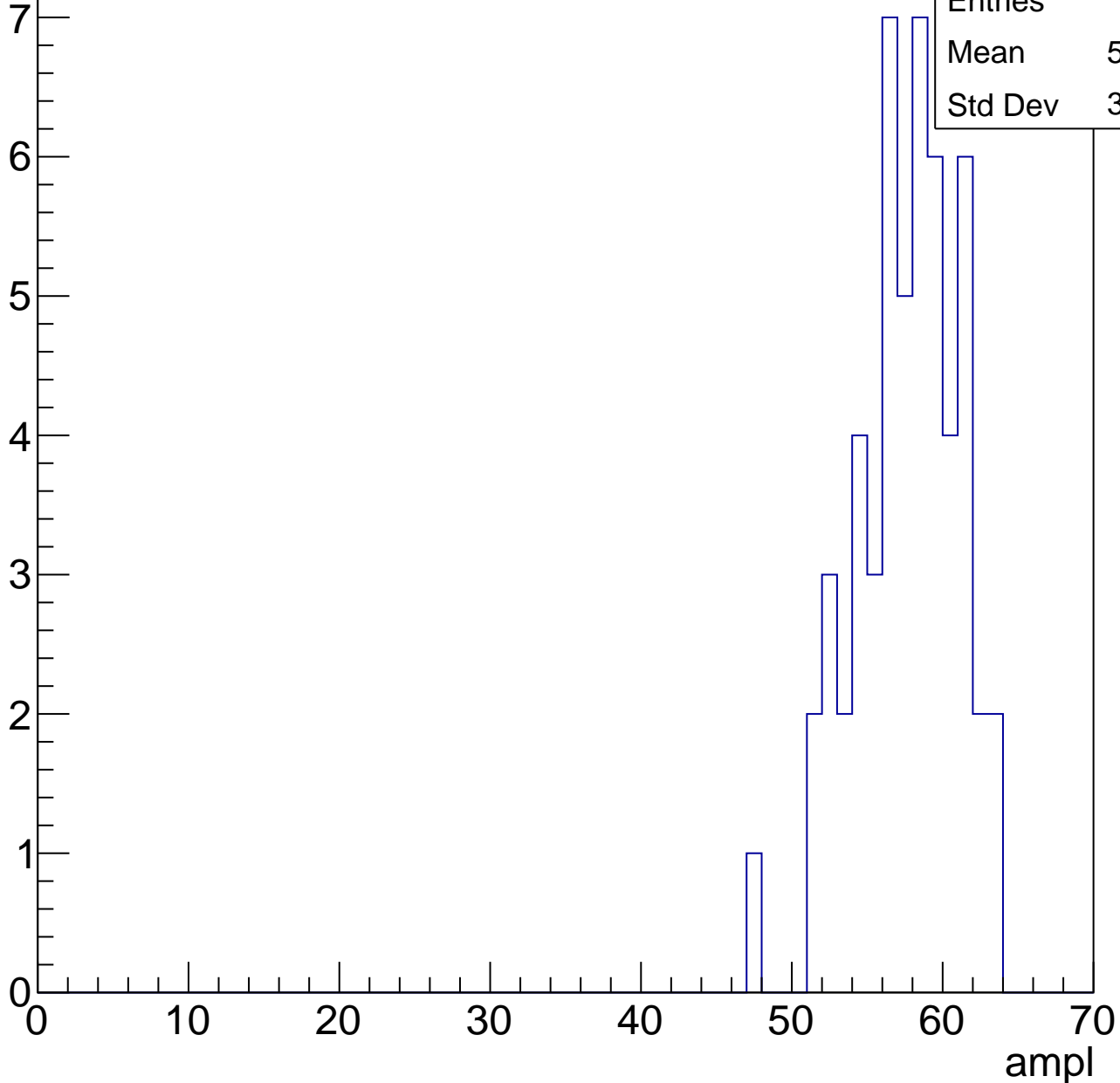


# B0L001S, U10-ch80, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	57.13
Std Dev	3.383

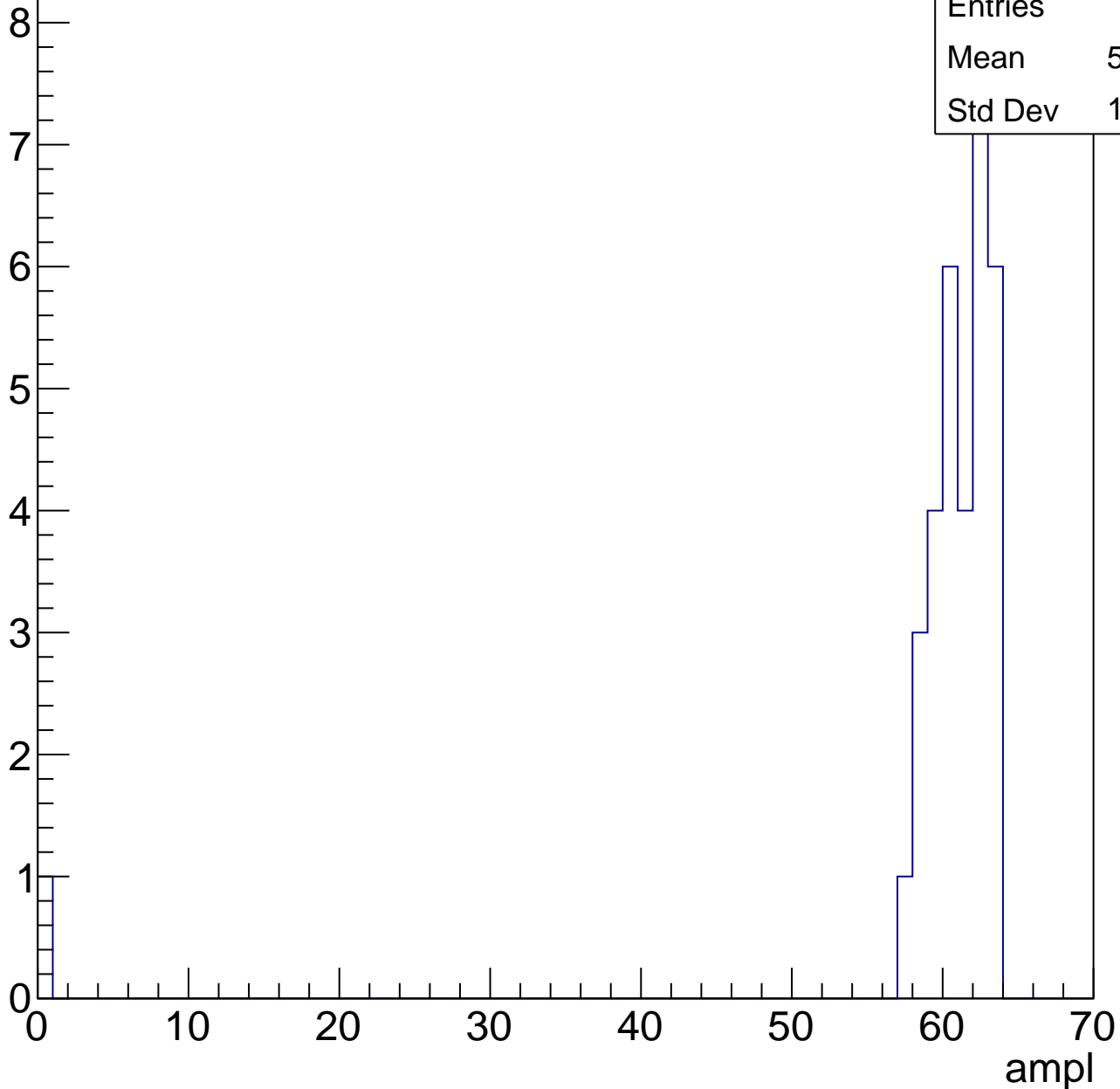


# B0L001S, U10-ch80, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	33
Mean	58.94
Std Dev	10.56



# B0L001S, U10-ch80, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	63
Std Dev	0

0 10 20 30 40 50 60 70

ampl



# B0L001S, U10-ch80, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U10-ch81, adc0

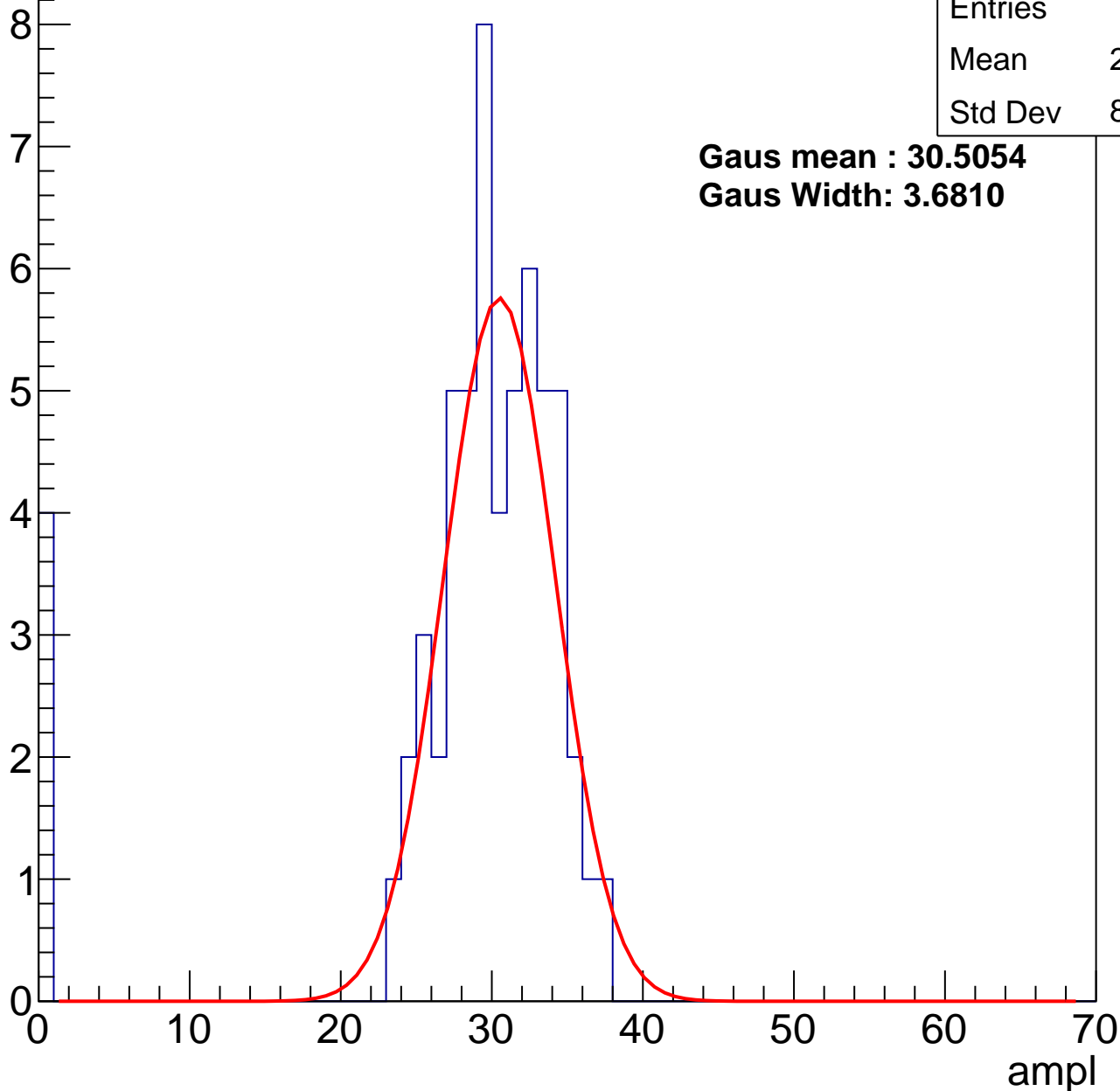
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	27.97
Std Dev	8.178

**Gaus mean : 30.5054**

**Gaus Width: 3.6810**



# B0L001S, U10-ch81, adc1

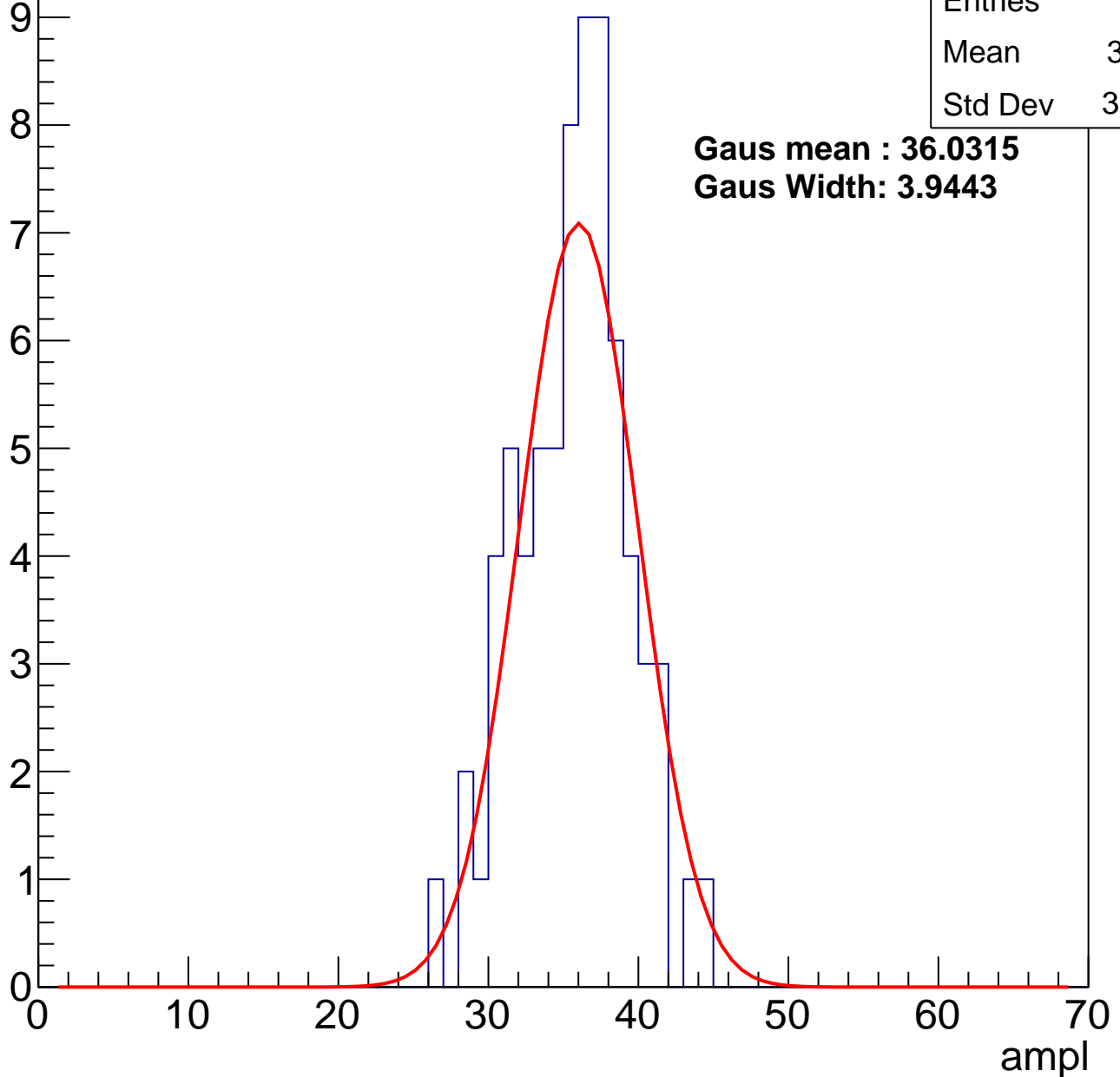
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	35.21
Std Dev	3.646

**Gaus mean : 36.0315**

**Gaus Width: 3.9443**



# B0L001S, U10-ch81, adc2

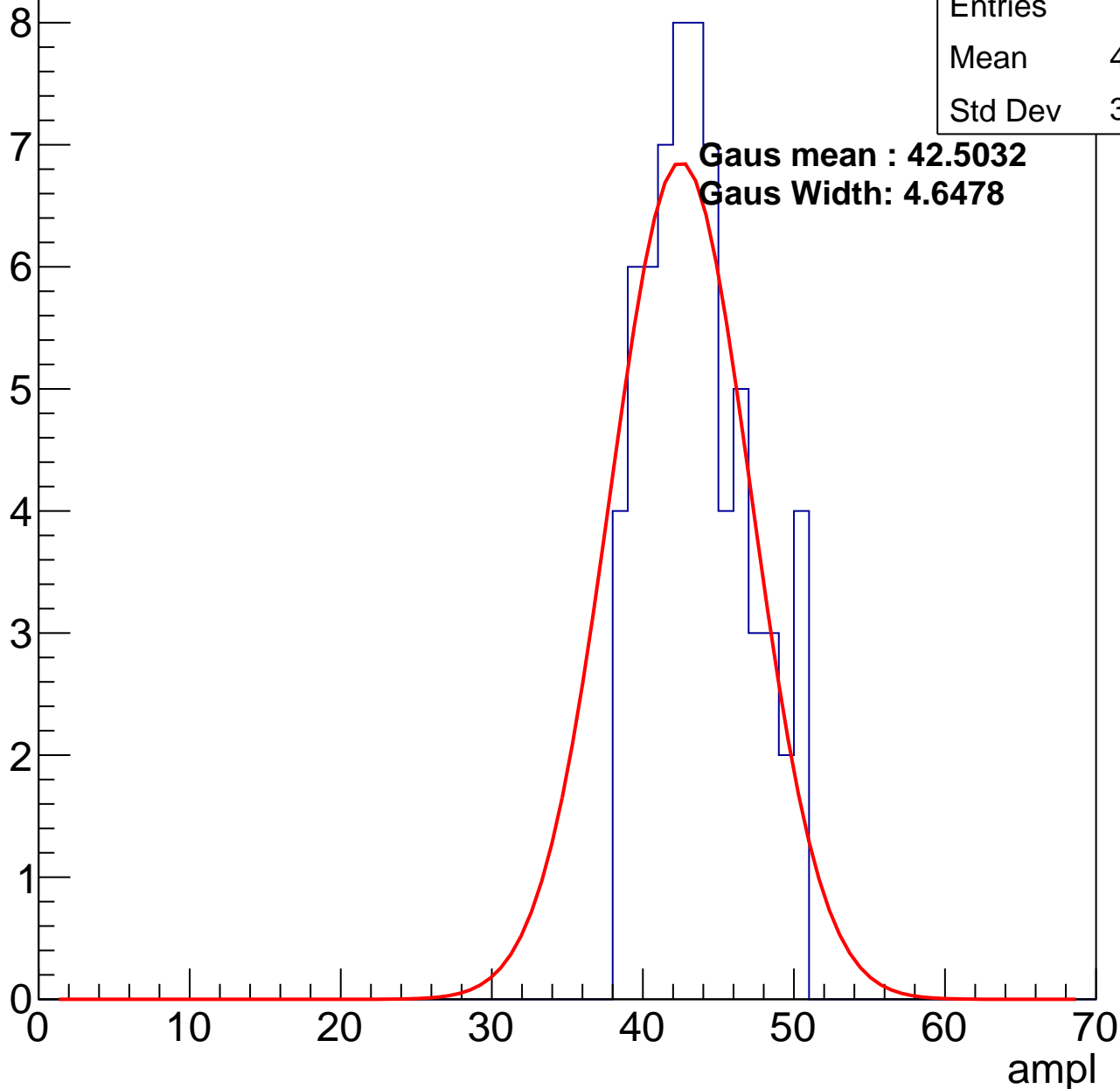
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	43.19
Std Dev	3.329

**Gaus mean : 42.5032**

**Gaus Width: 4.6478**

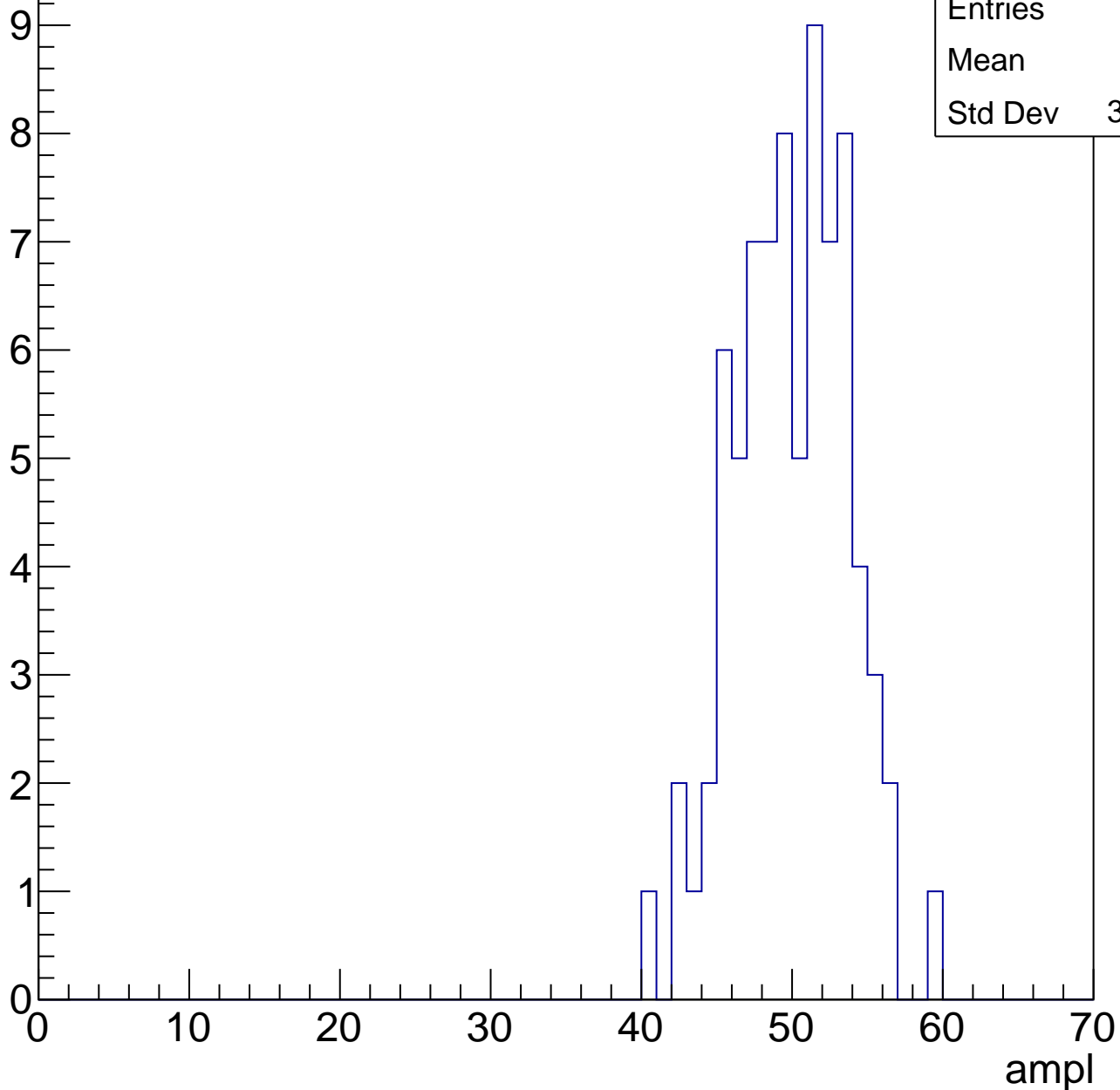


# B0L001S, U10-ch81, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	78
Mean	49.5
Std Dev	3.686

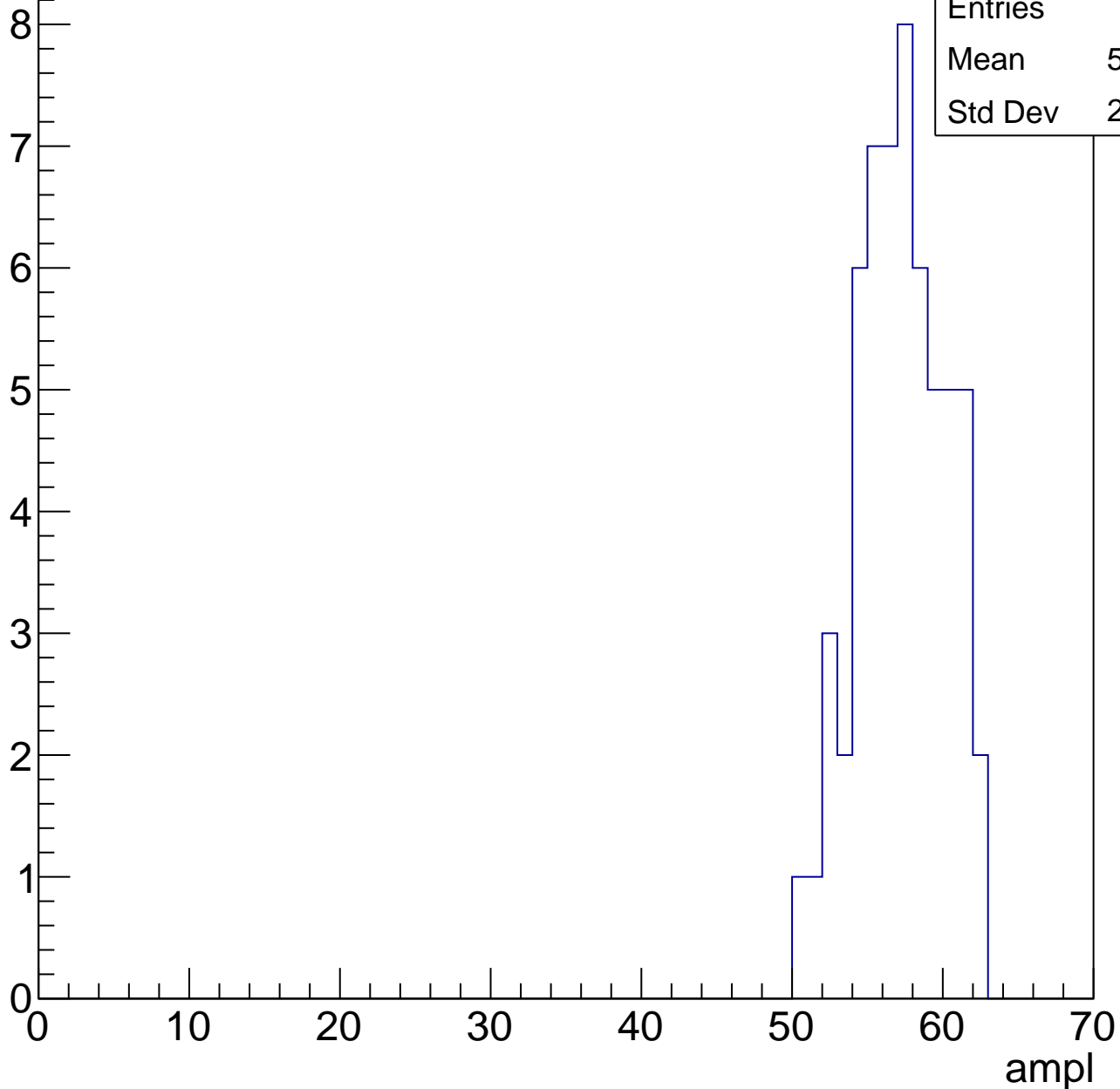


# B0L001S, U10-ch81, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	56.76
Std Dev	2.873

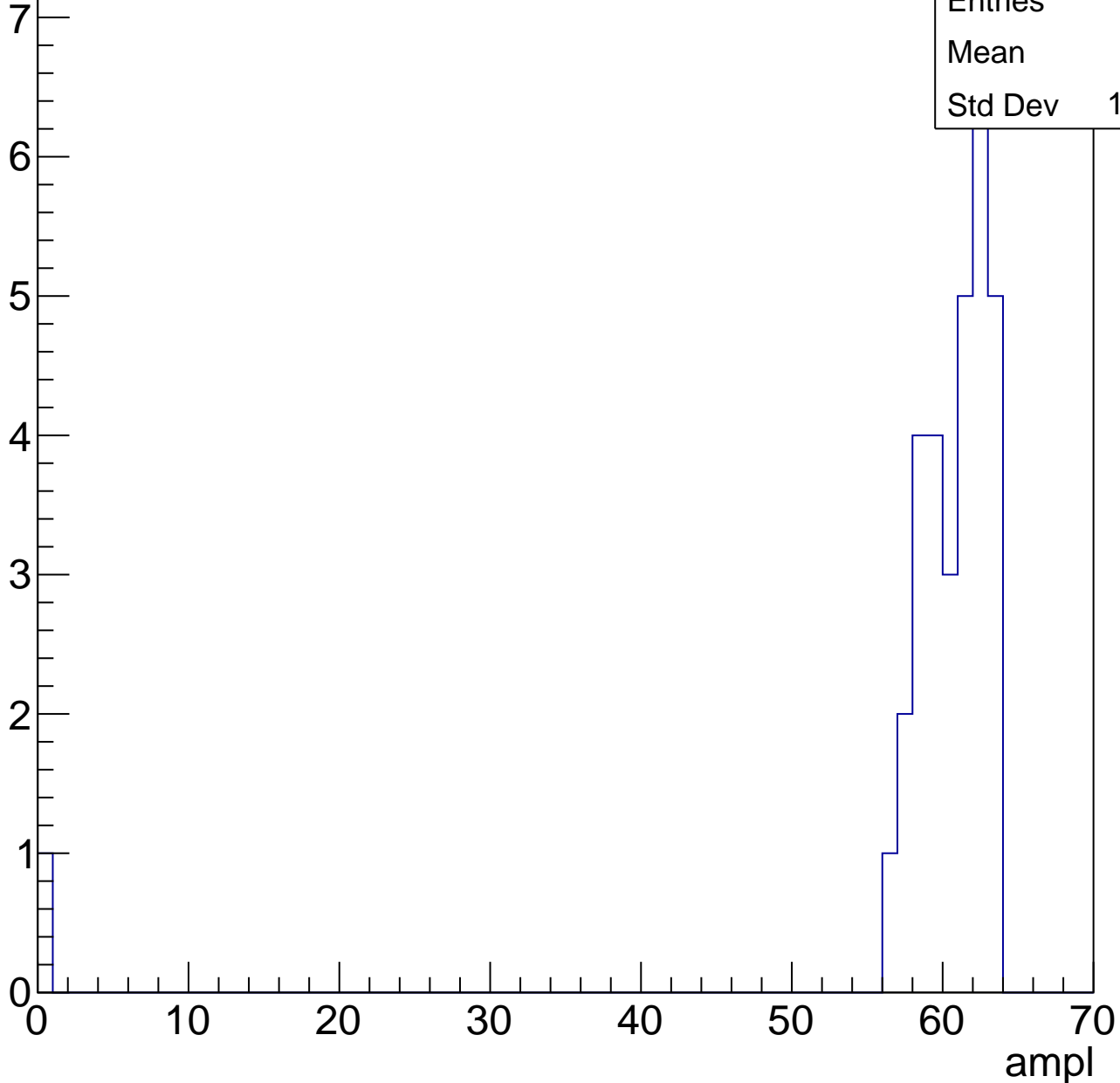


# B0L001S, U10-ch81, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	32
Mean	58.5
Std Dev	10.69

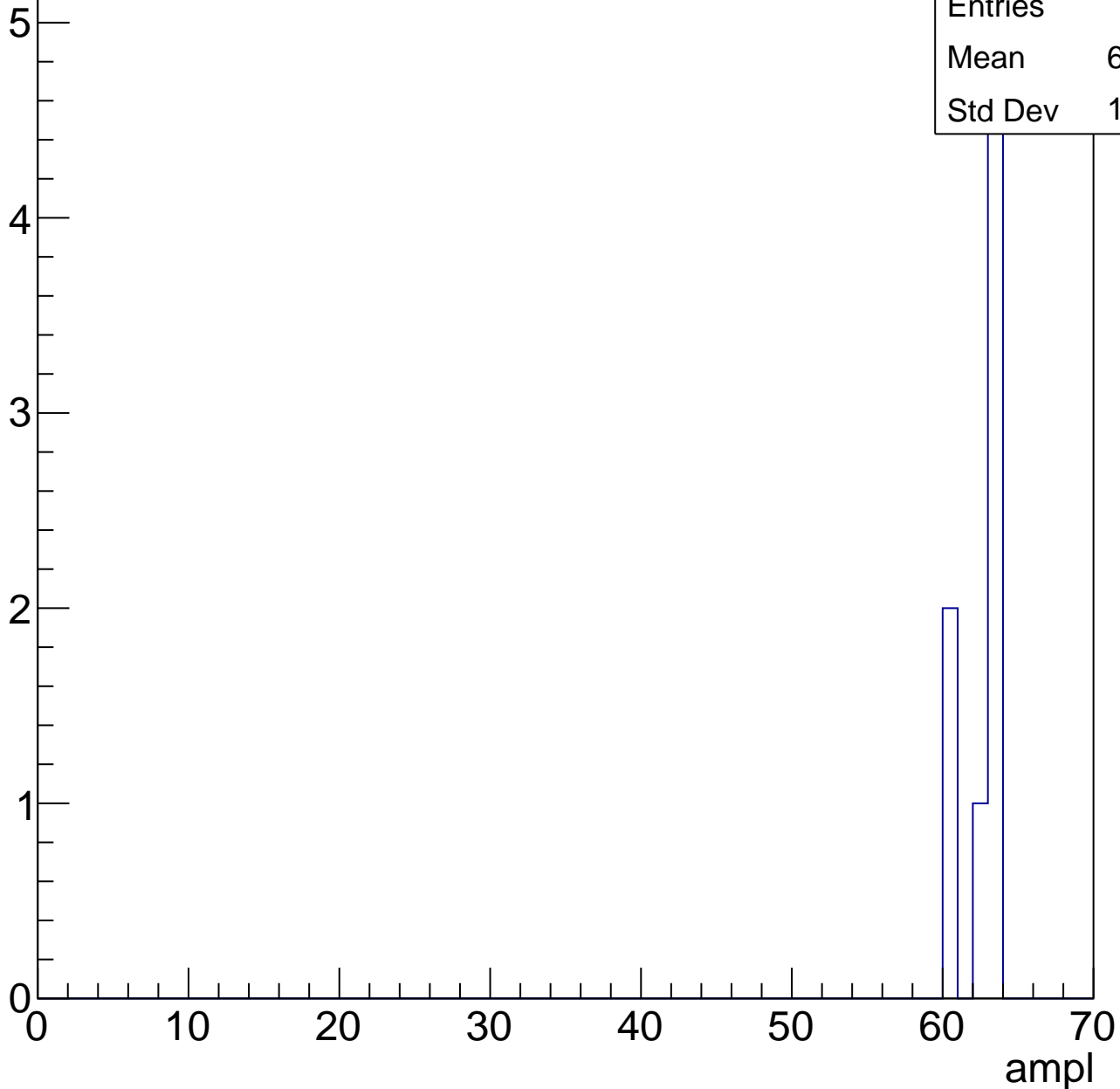


# B0L001S, U10-ch81, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	8
Mean	62.12
Std Dev	1.269





# B0L001S, U10-ch81, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L001S, U10-ch82, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	71
Mean	29.18
Std Dev	4.914

**Gaus mean : 30.1624**

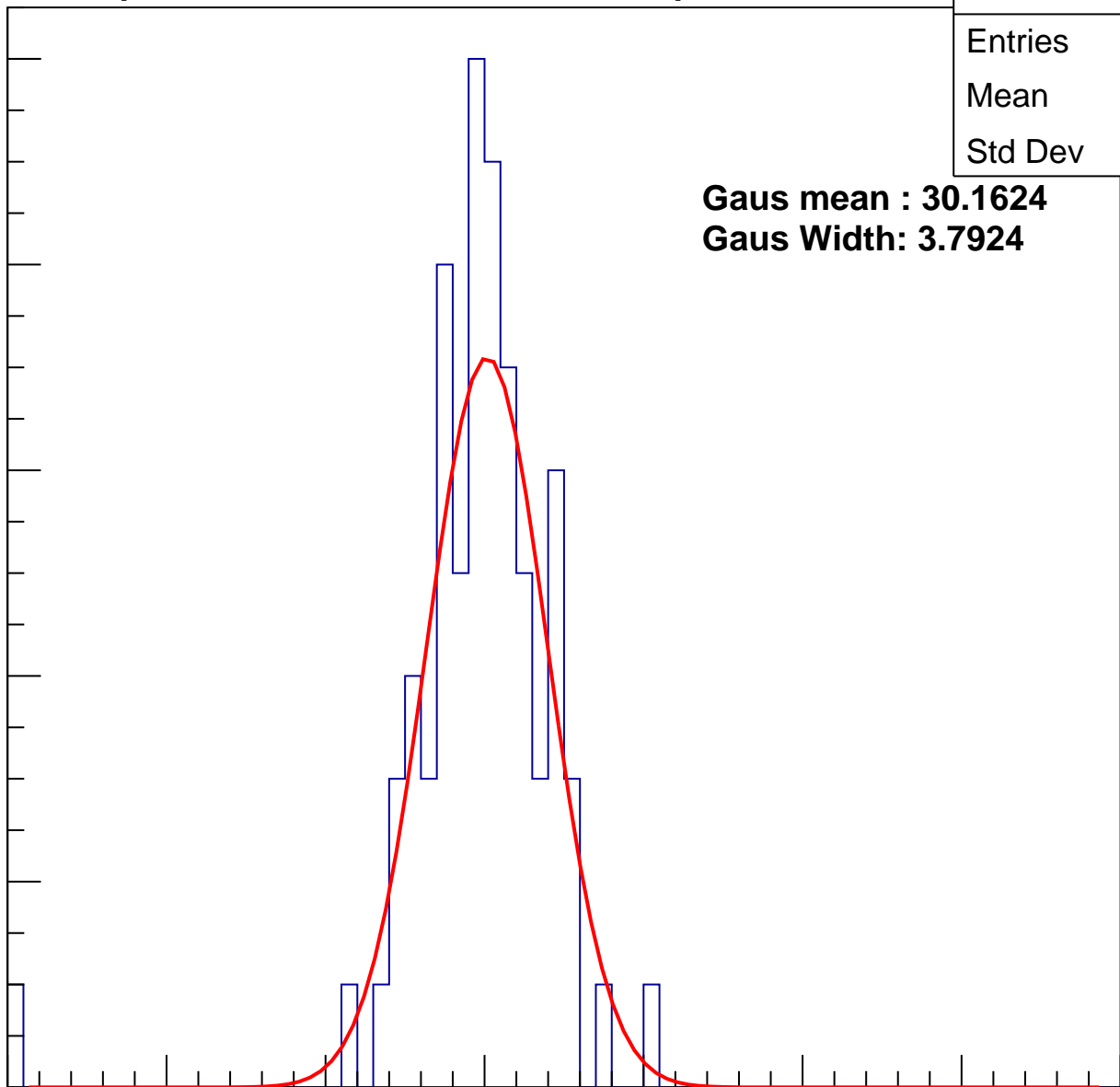
**Gaus Width: 3.7924**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U10-ch82, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	73
Mean	36.85
Std Dev	3.113

**Gaus mean : 37.3903**

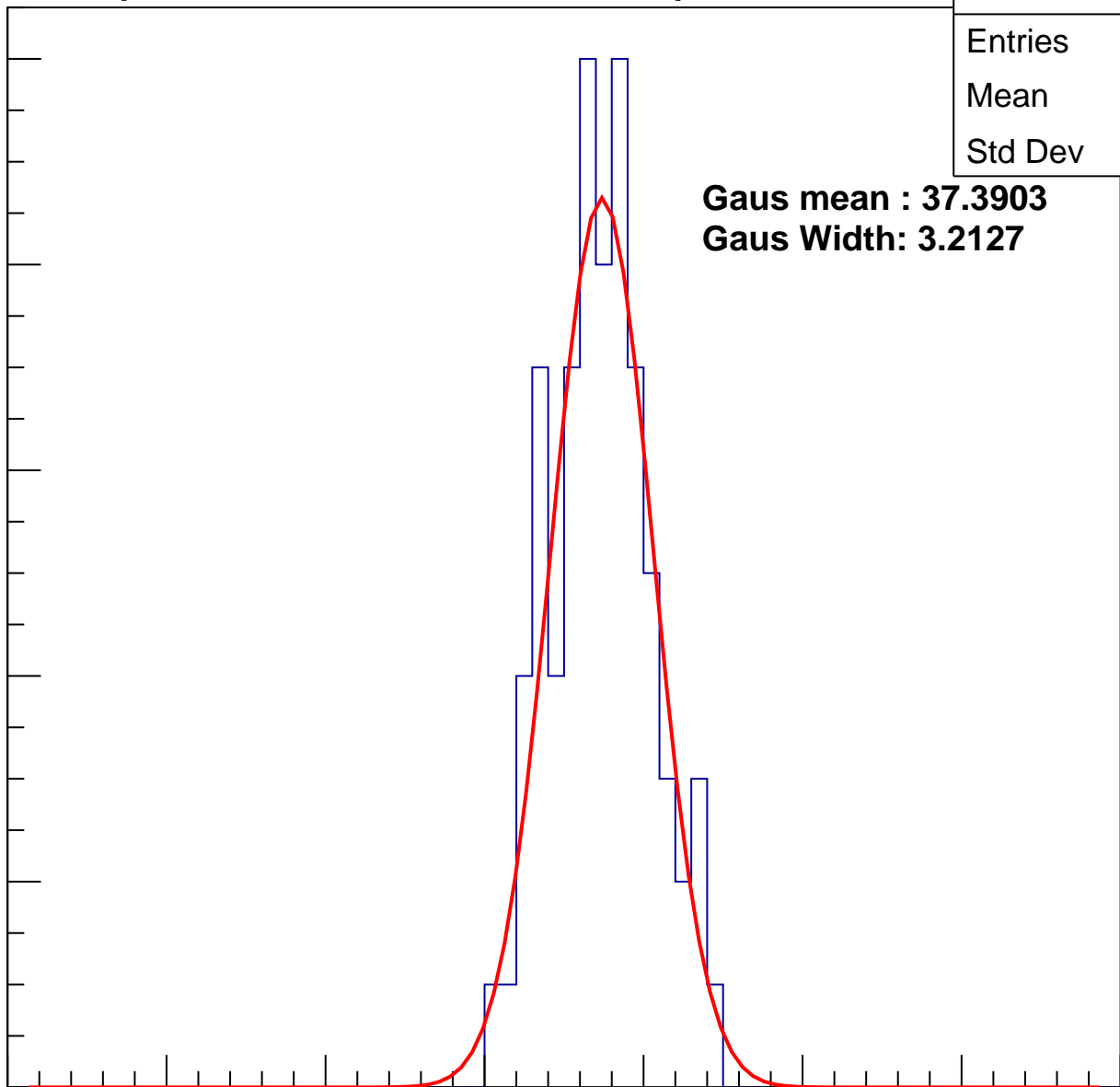
**Gaus Width: 3.2127**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B0L001S, U10-ch82, adc2

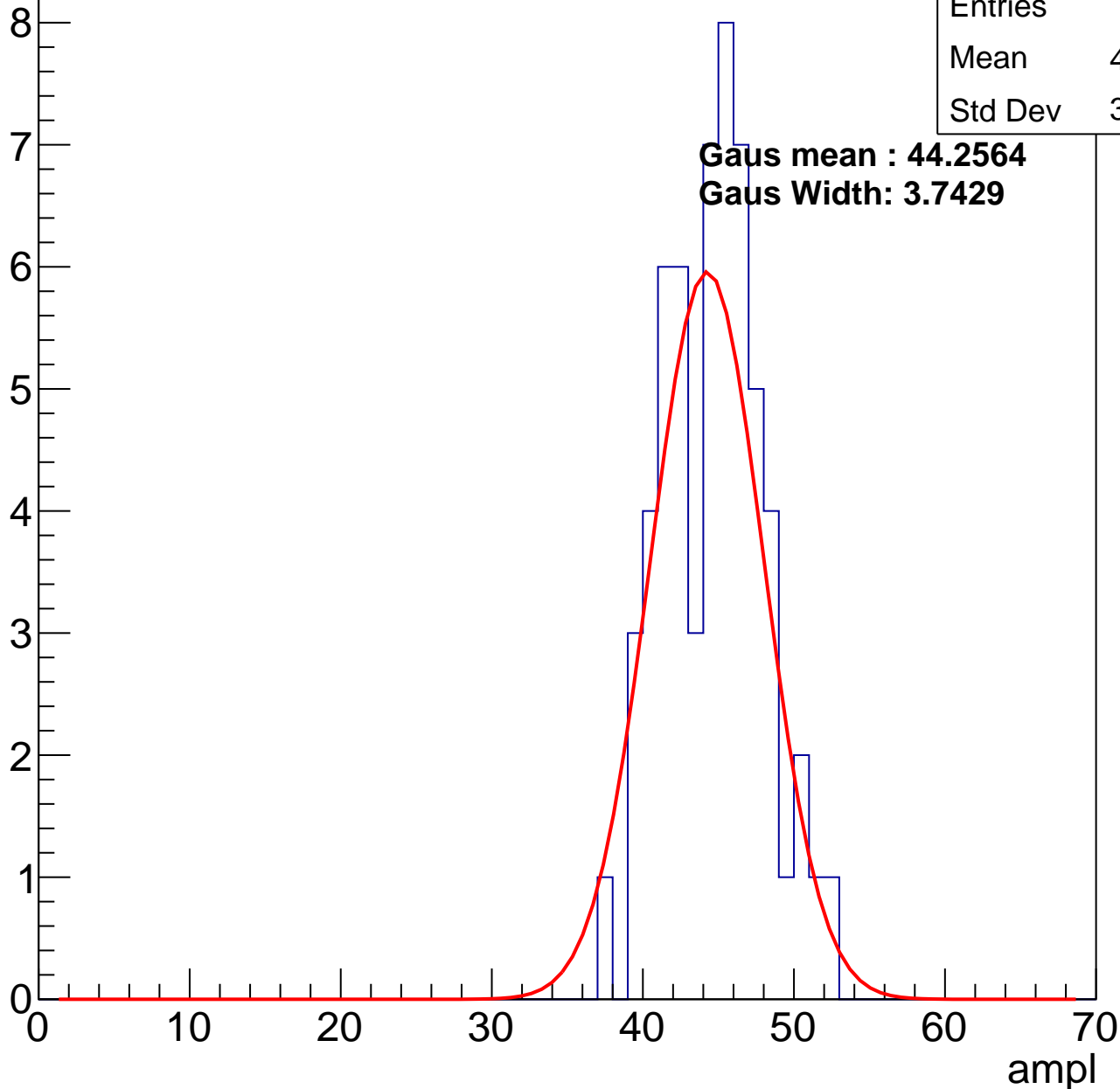
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	44.24
Std Dev	3.243

**Gaus mean : 44.2564**

**Gaus Width: 3.7429**

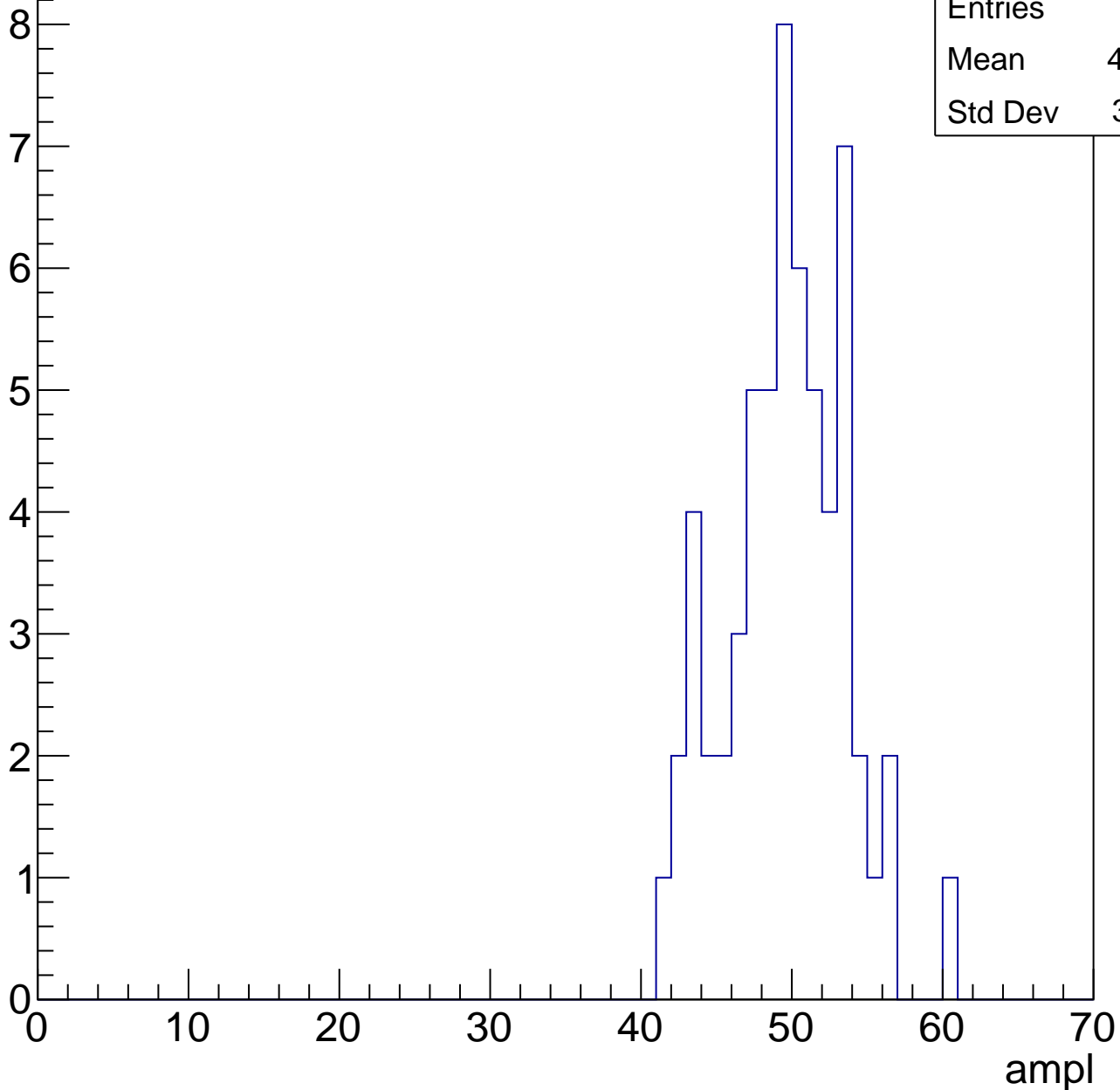


# B0L001S, U10-ch82, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

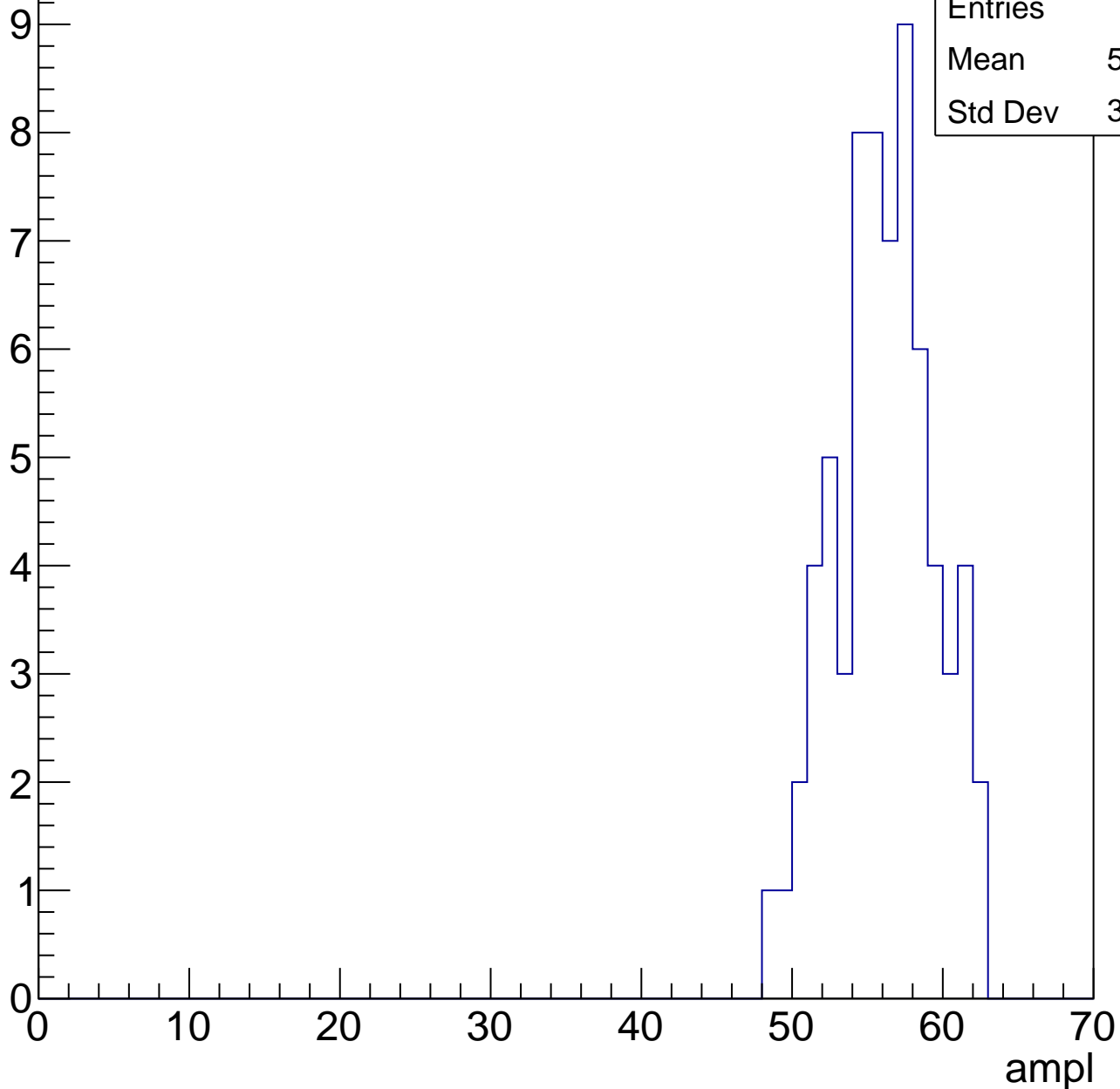
Entries	60
Mean	49.15
Std Dev	3.911



# B0L001S, U10-ch82, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



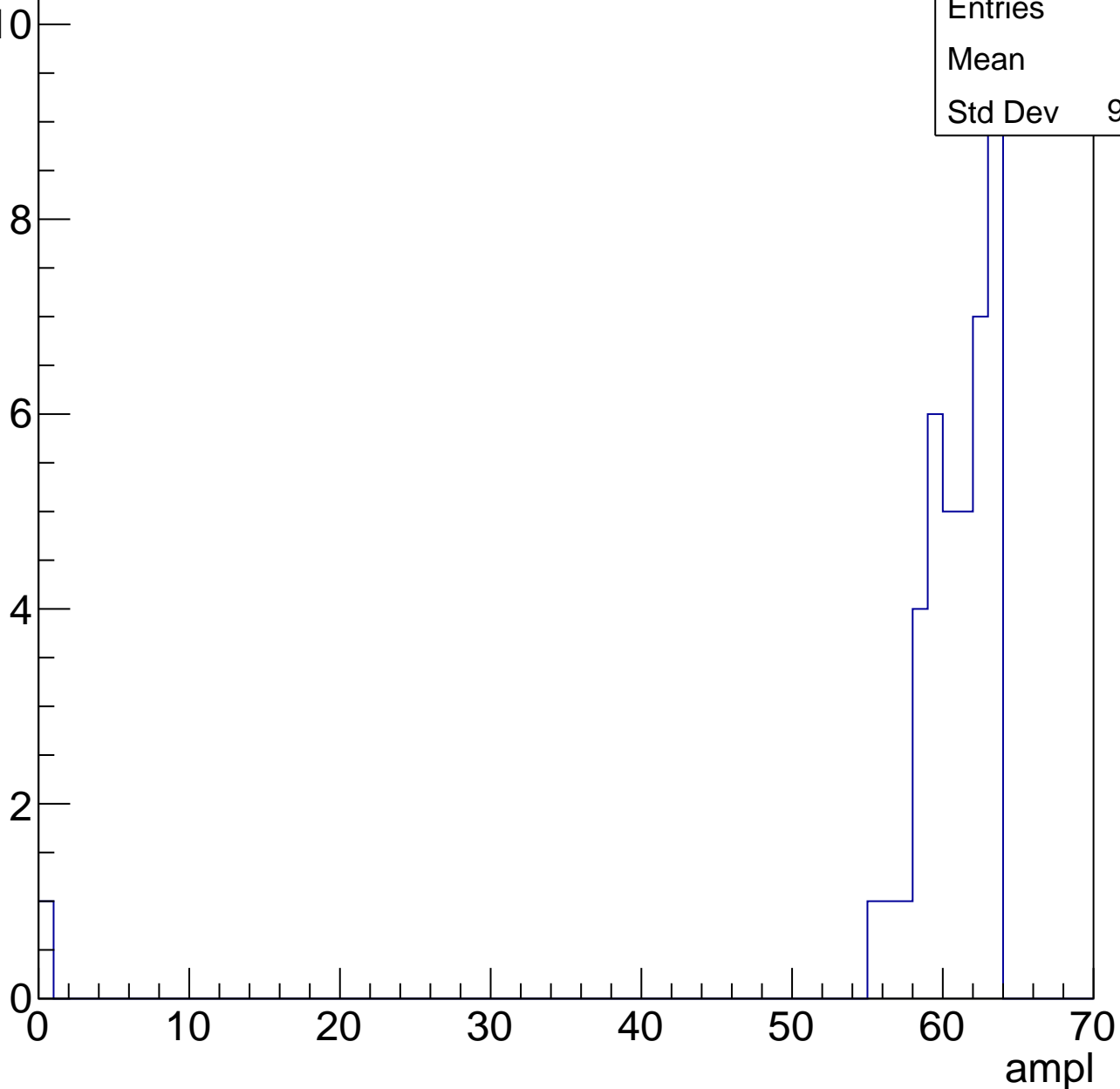
Entries	67
Mean	55.66
Std Dev	3.262

# B0L001S, U10-ch82, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	41
Mean	59.1
Std Dev	9.578



# B0L001S, U10-ch82, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

3

Mean

61

Std Dev

0.8165



# B0L001S, U10-ch82, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U10-ch83, adc0

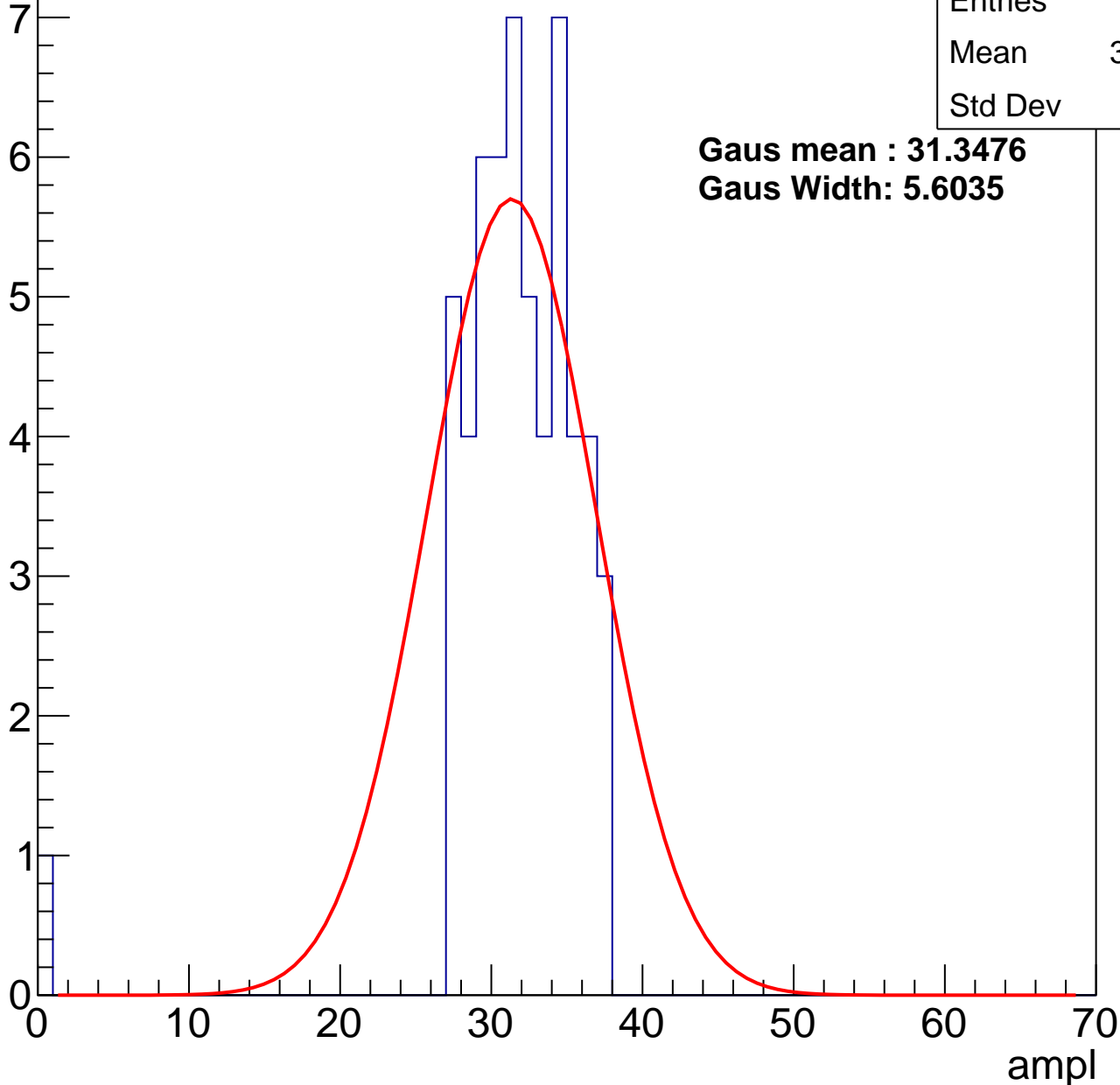
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	31.12
Std Dev	5.11

**Gaus mean : 31.3476**

**Gaus Width: 5.6035**

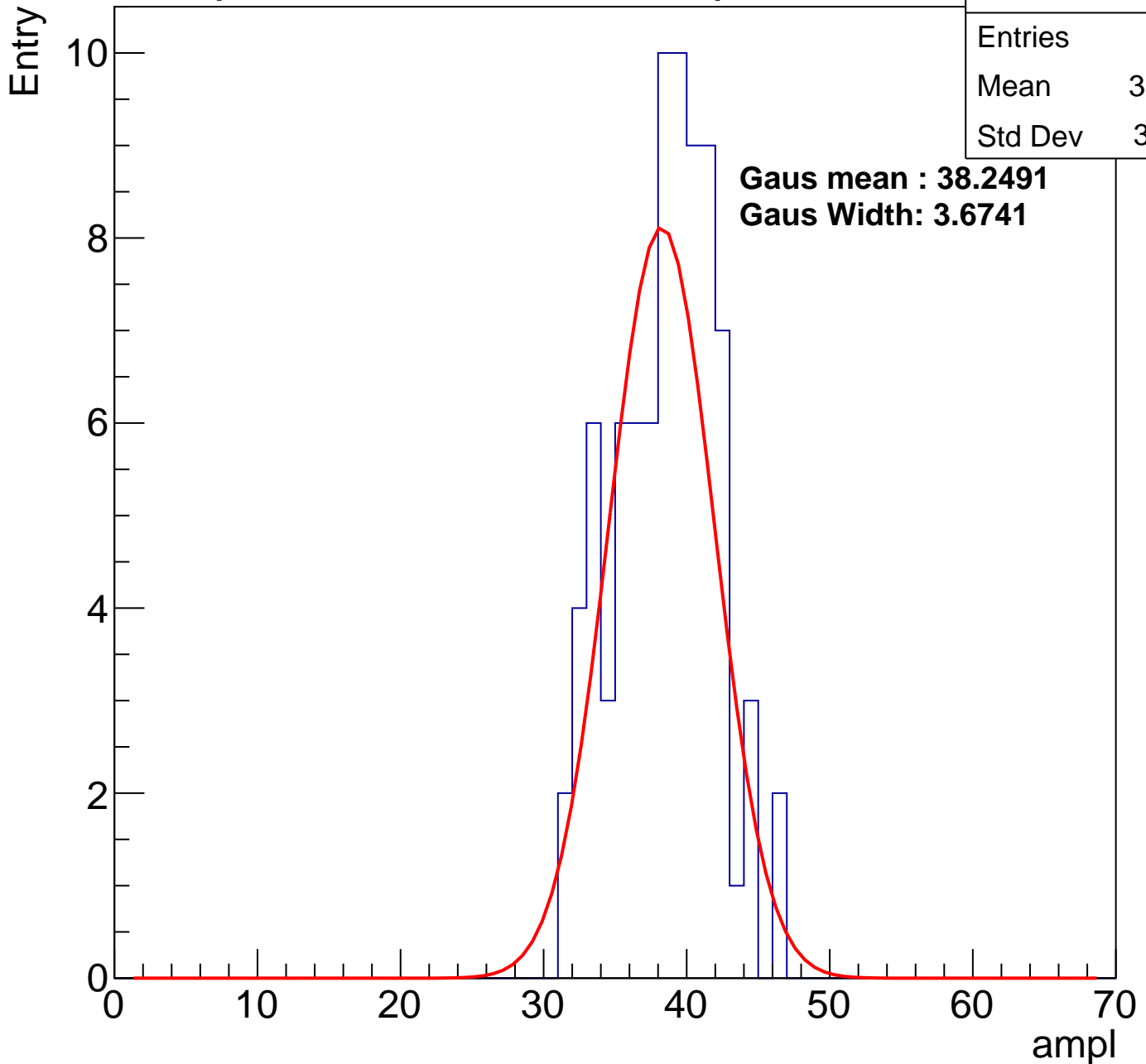


# B0L001S, U10-ch83, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	84
Mean	38.07
Std Dev	3.491

**Gaus mean : 38.2491**  
**Gaus Width: 3.6741**



# B0L001S, U10-ch83, adc2

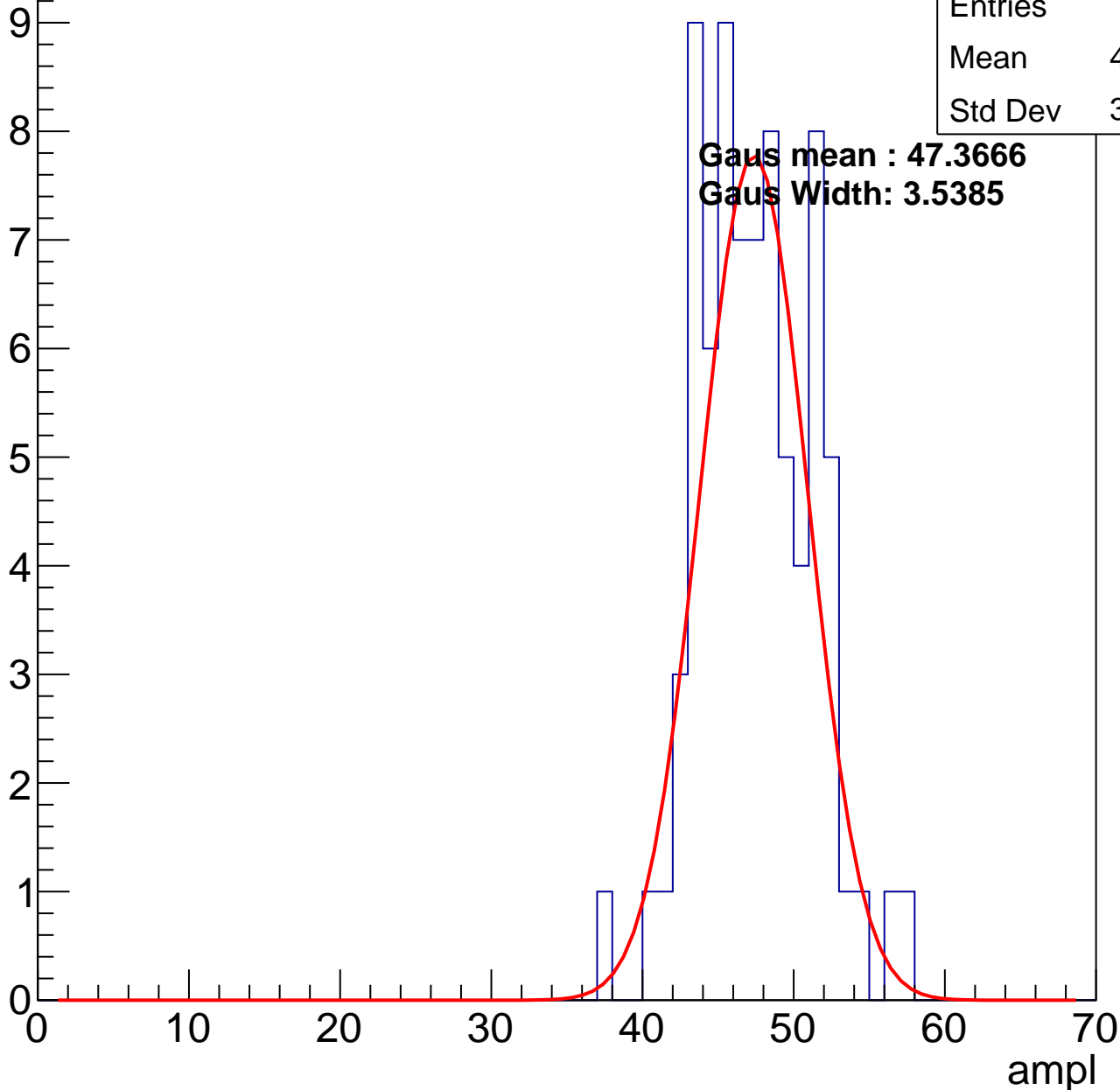
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	78
Mean	47.03
Std Dev	3.728

**Gaus mean : 47.3666**

**Gaus Width: 3.5385**

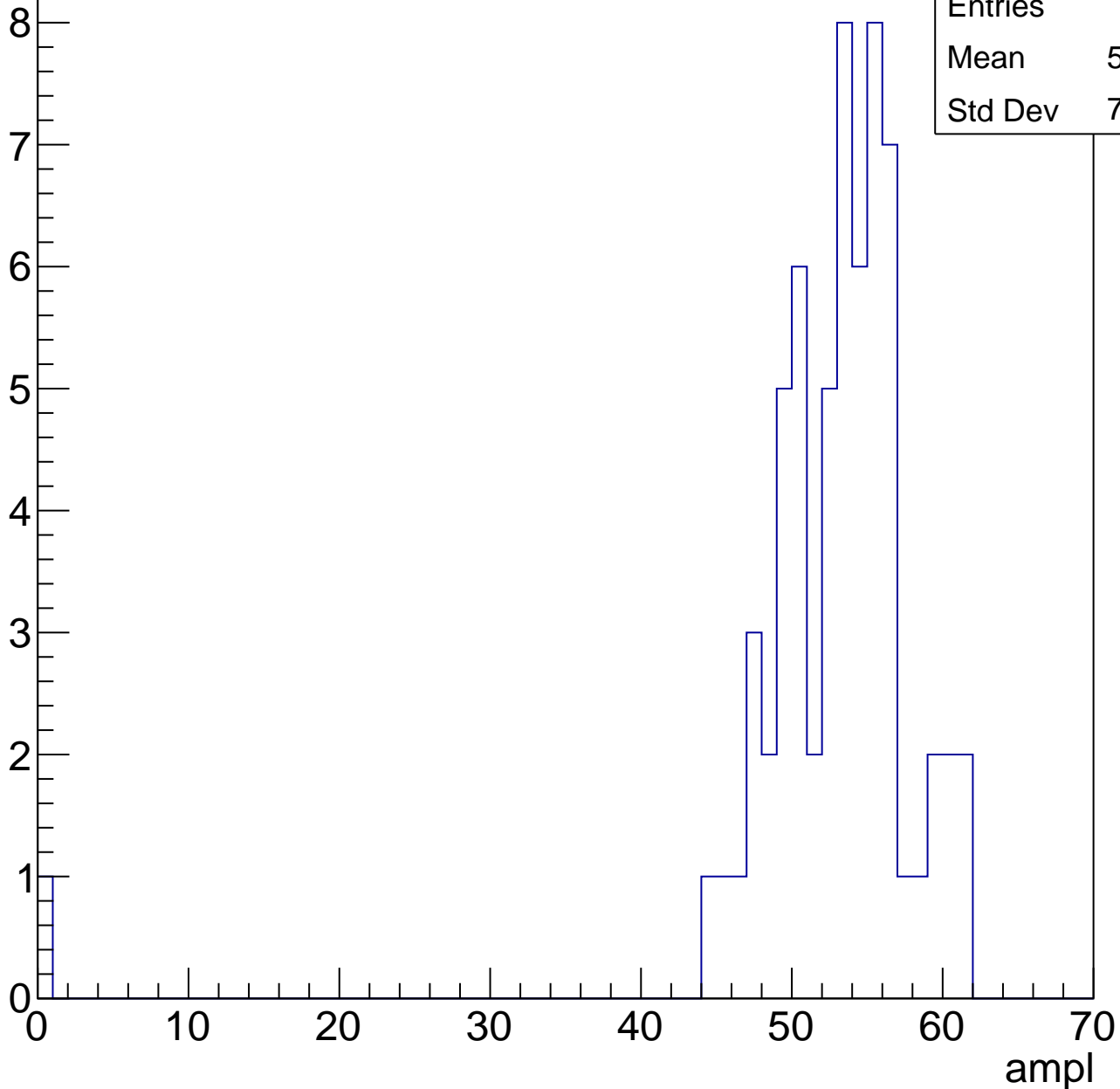


# B0L001S, U10-ch83, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	52.09
Std Dev	7.599

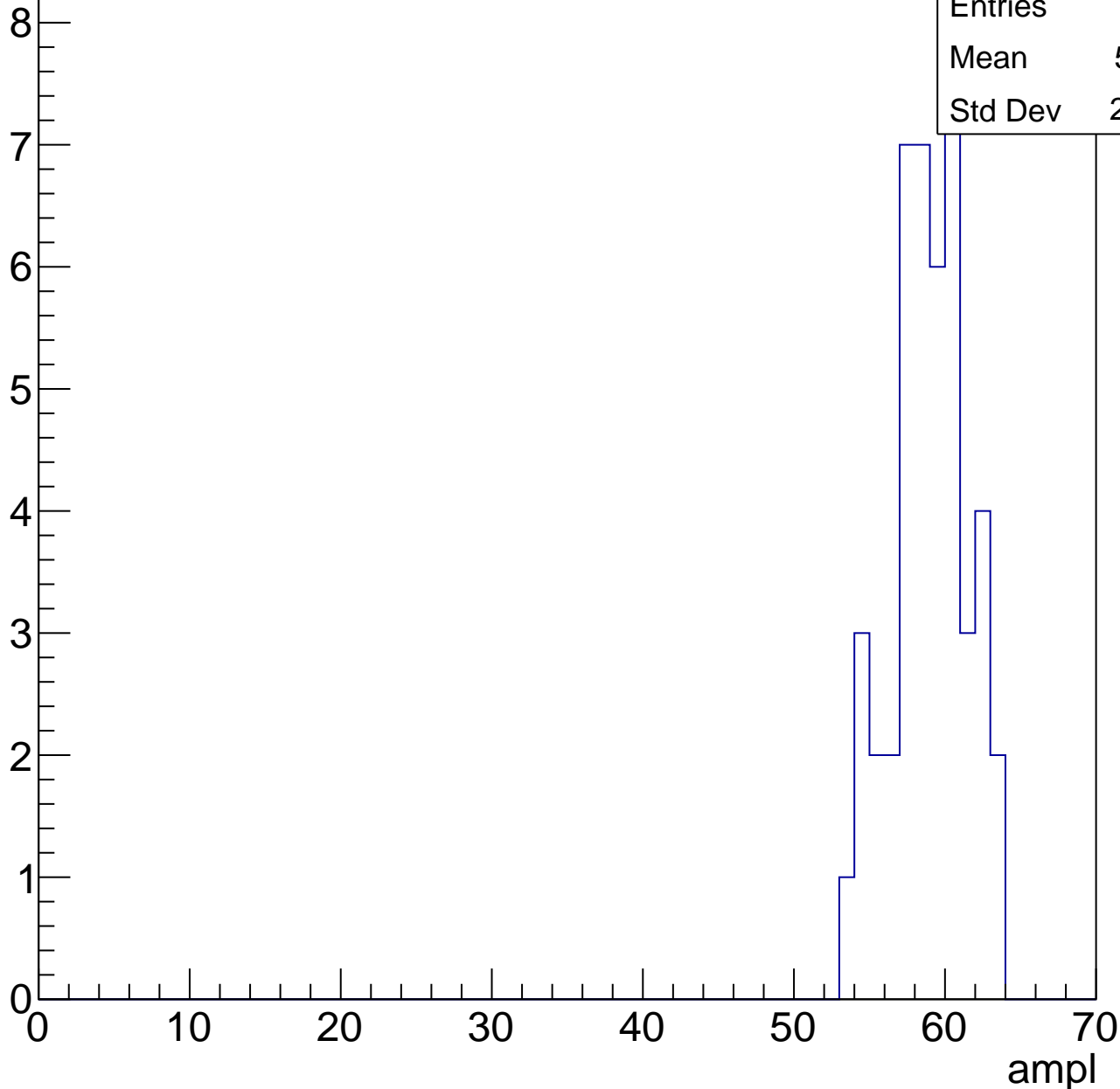


# B0L001S, U10-ch83, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

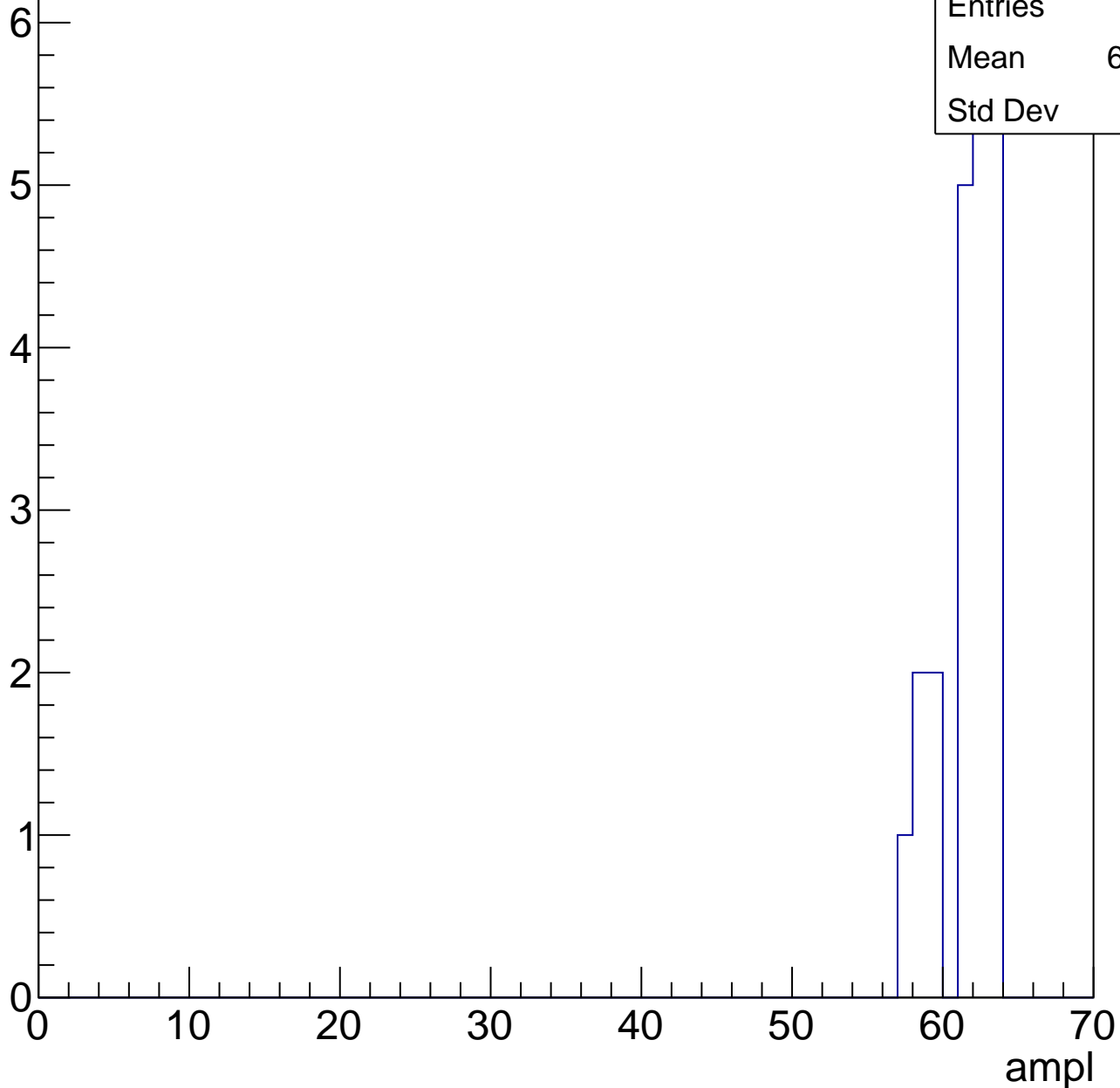
Entries	45
Mean	58.51
Std Dev	2.464



# B0L001S, U10-ch83, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U10-ch83, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch83, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U10-ch84, adc0

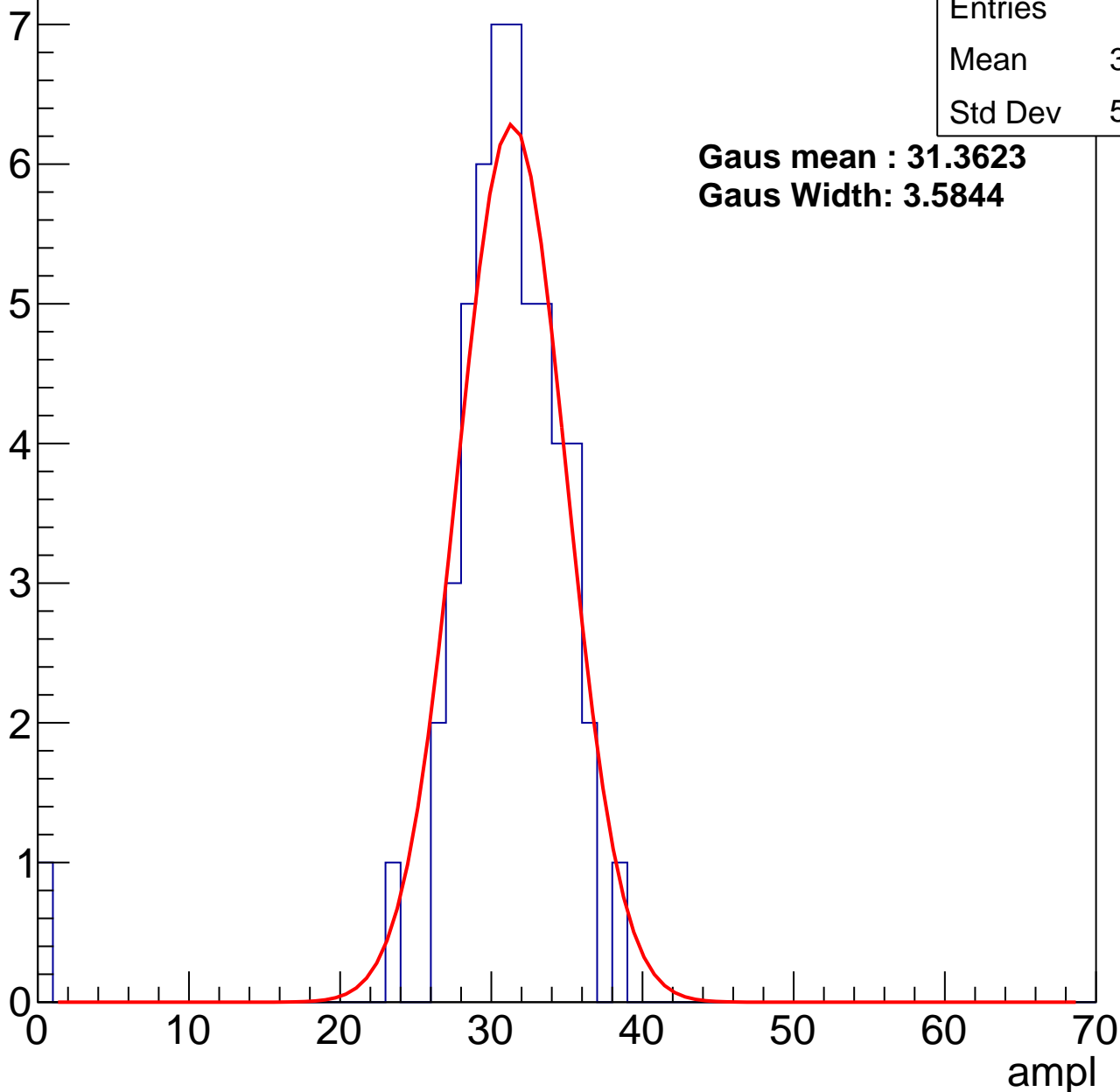
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	30.34
Std Dev	5.139

**Gaus mean : 31.3623**

**Gaus Width: 3.5844**



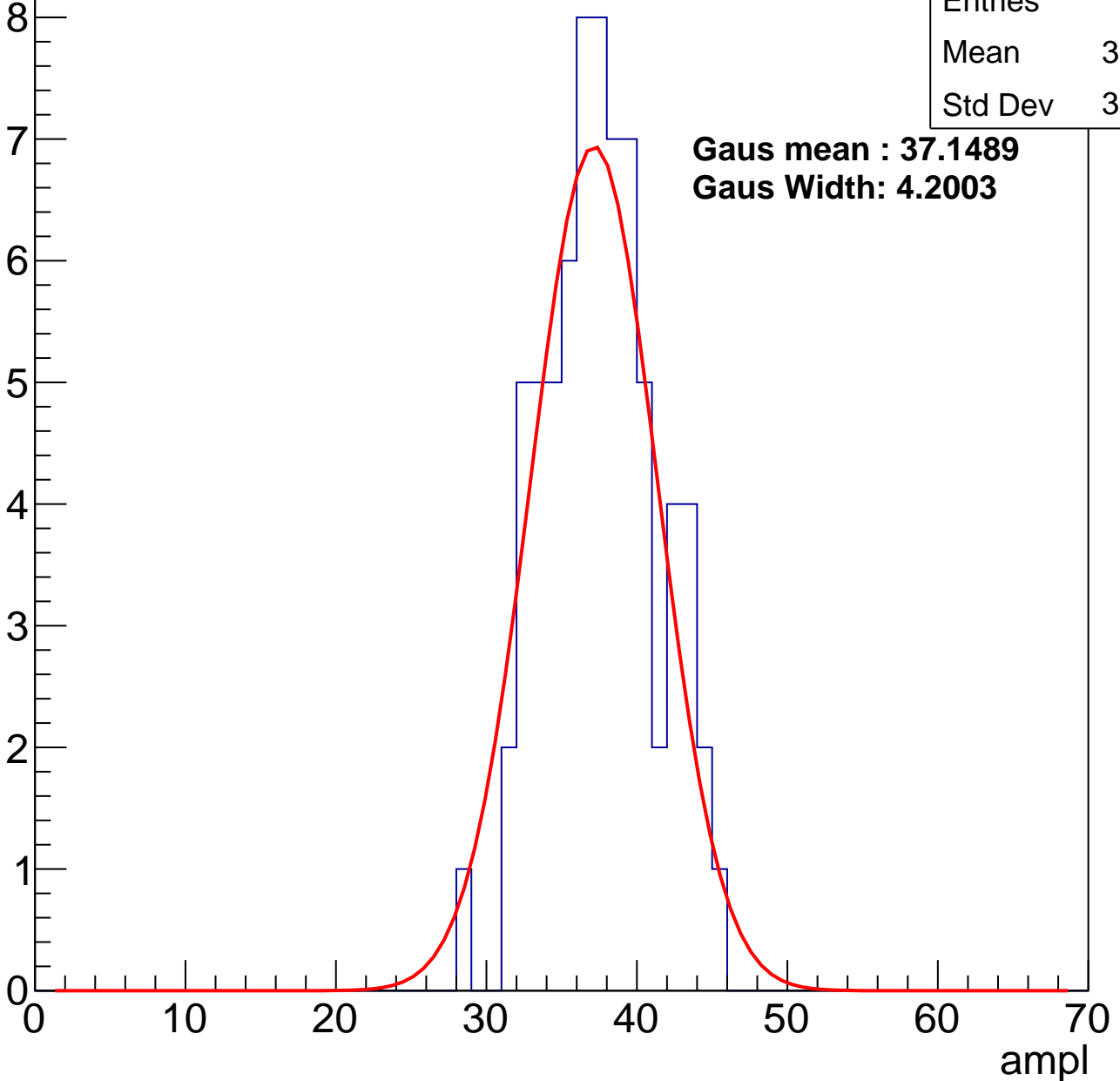
# B0L001S, U10-ch84, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	37.12
Std Dev	3.636

**Gaus mean : 37.1489**  
**Gaus Width: 4.2003**



# B0L001S, U10-ch84, adc2

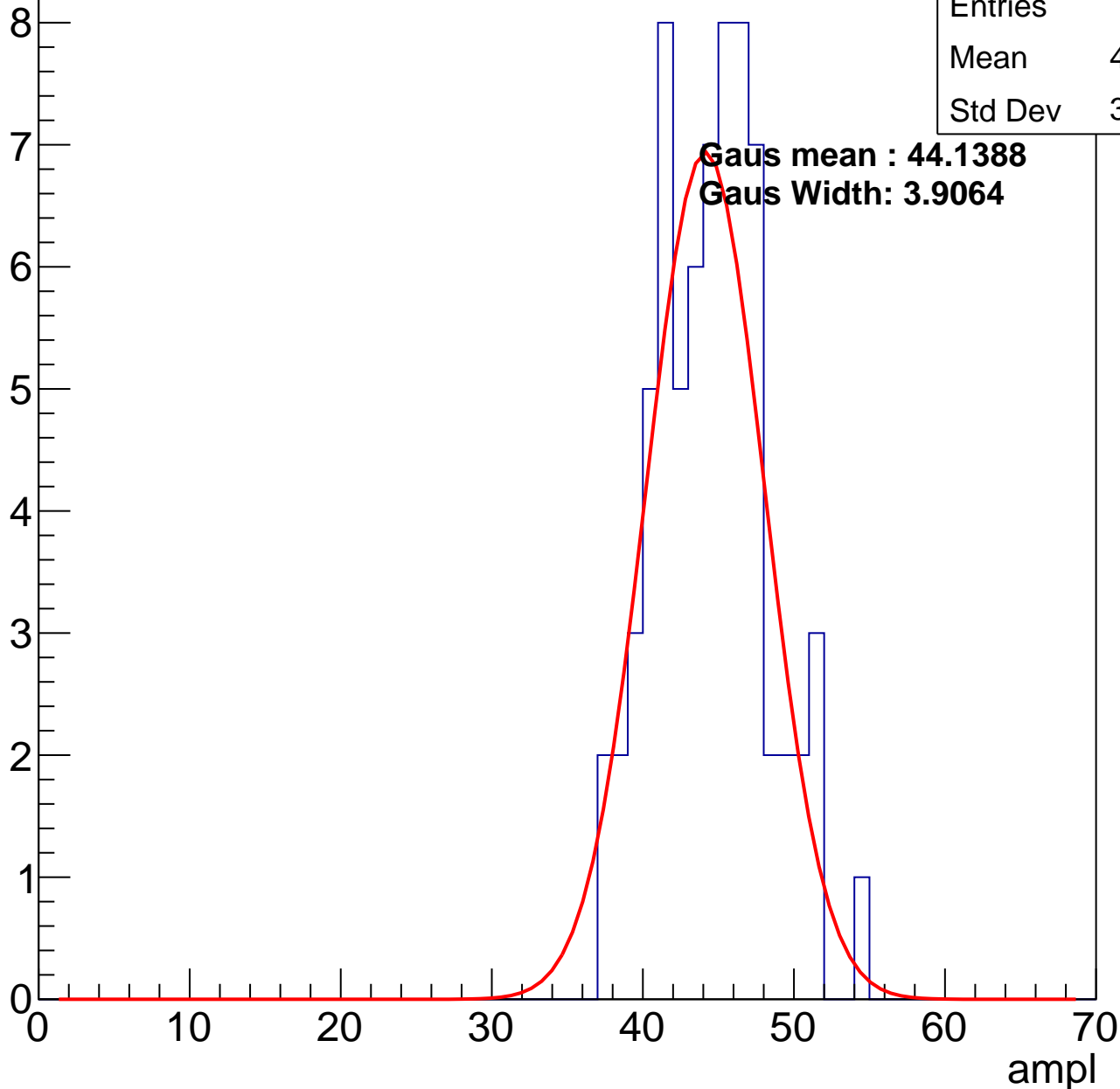
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	44.07
Std Dev	3.613

**Gaus mean : 44.1388**

**Gaus Width: 3.9064**

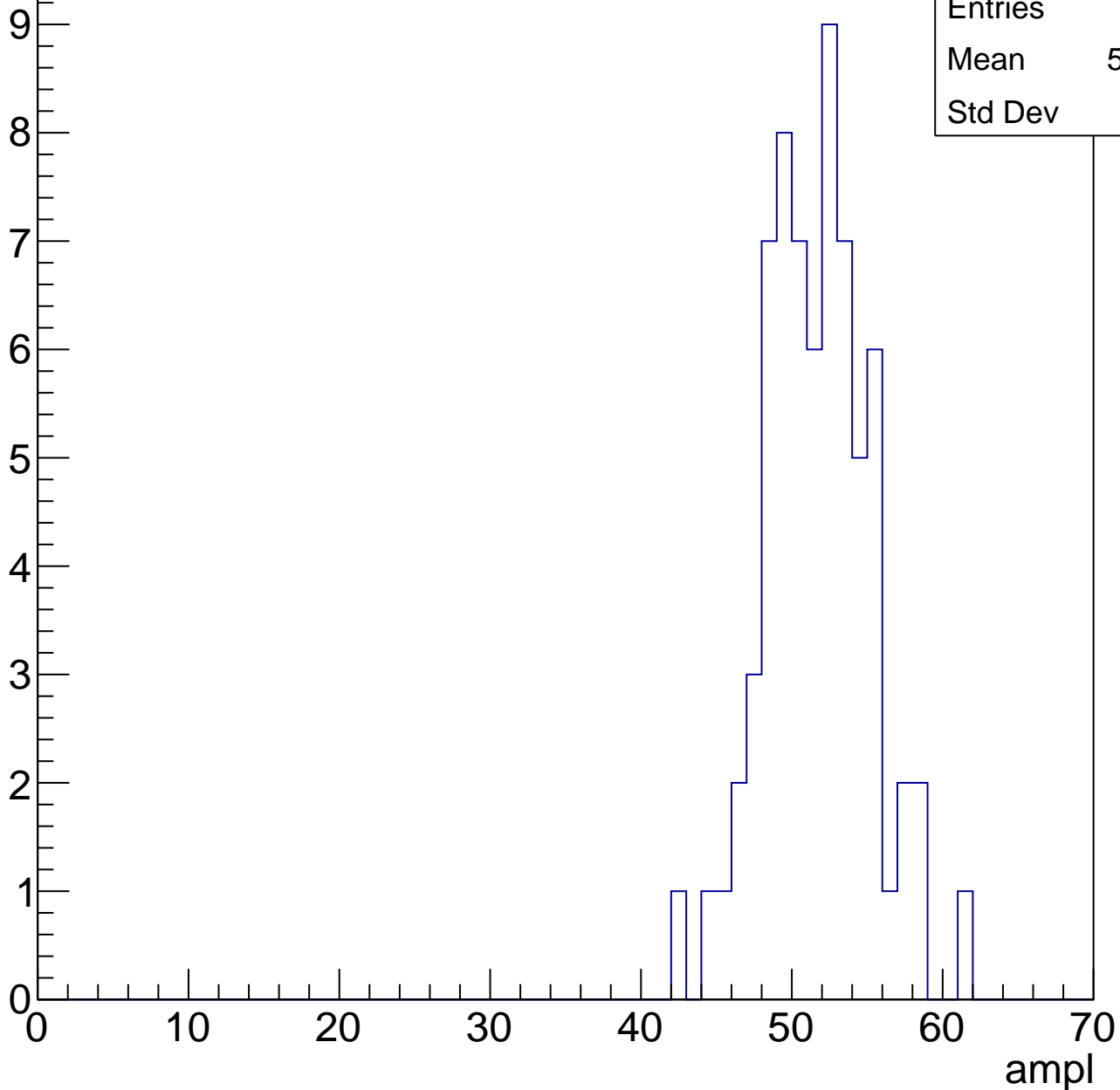


# B0L001S, U10-ch84, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

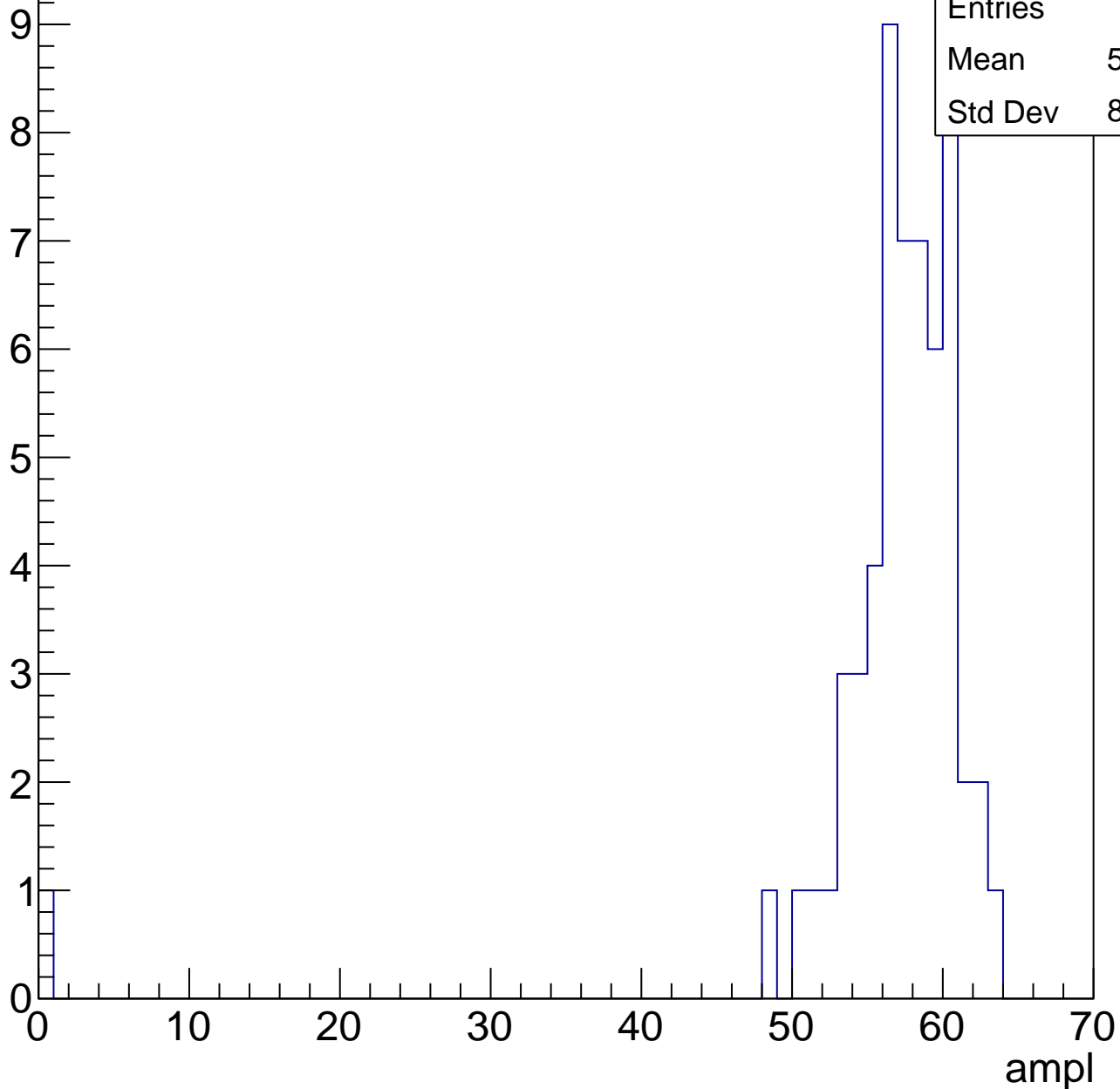
Entries	69
Mean	51.22
Std Dev	3.48



# B0L001S, U10-ch84, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



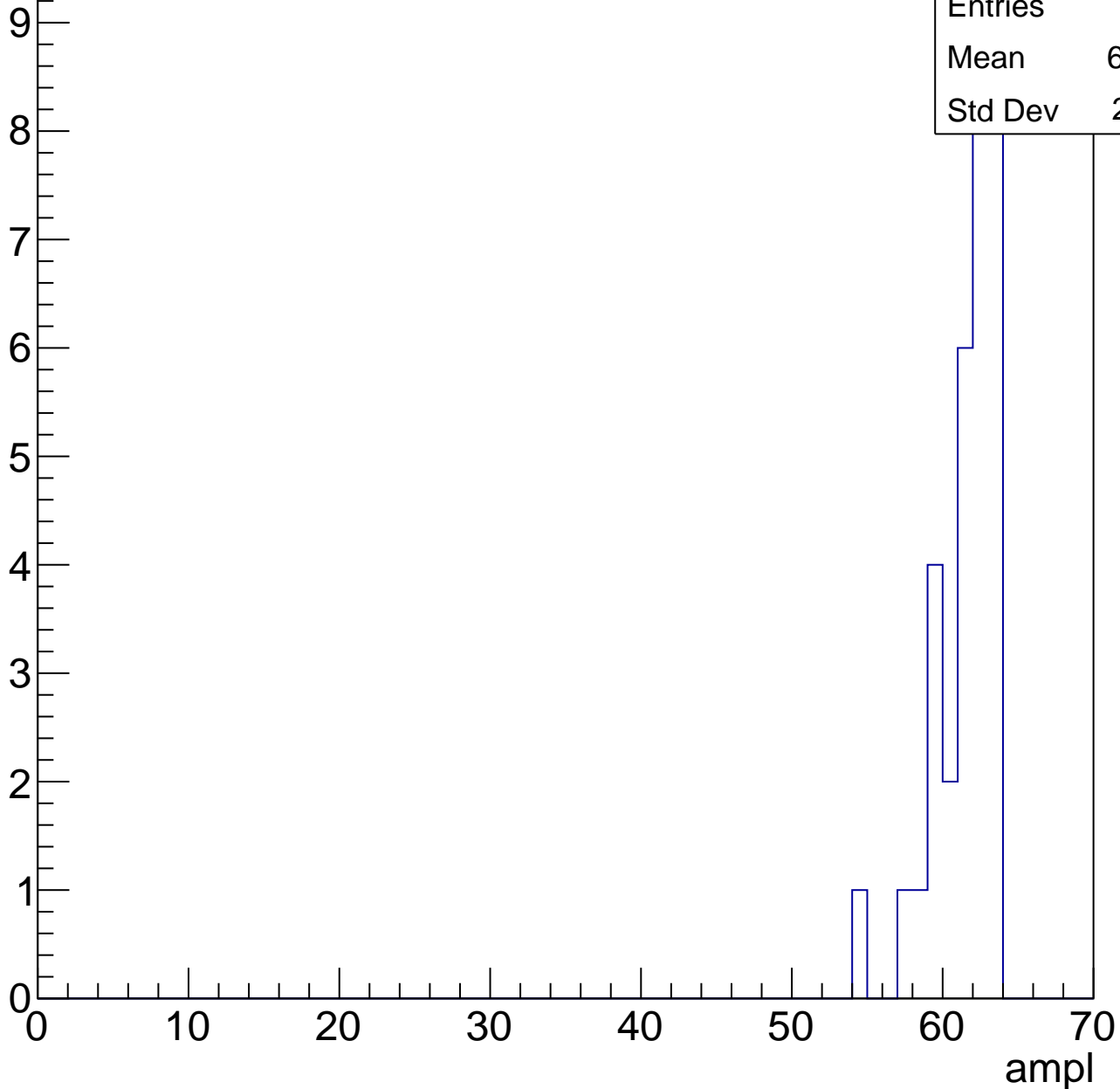
Entries	57
Mean	56.04
Std Dev	8.065

# B0L001S, U10-ch84, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	32
Mean	61.06
Std Dev	2.061



# B0L001S, U10-ch84, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch84, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U10-ch85, adc0

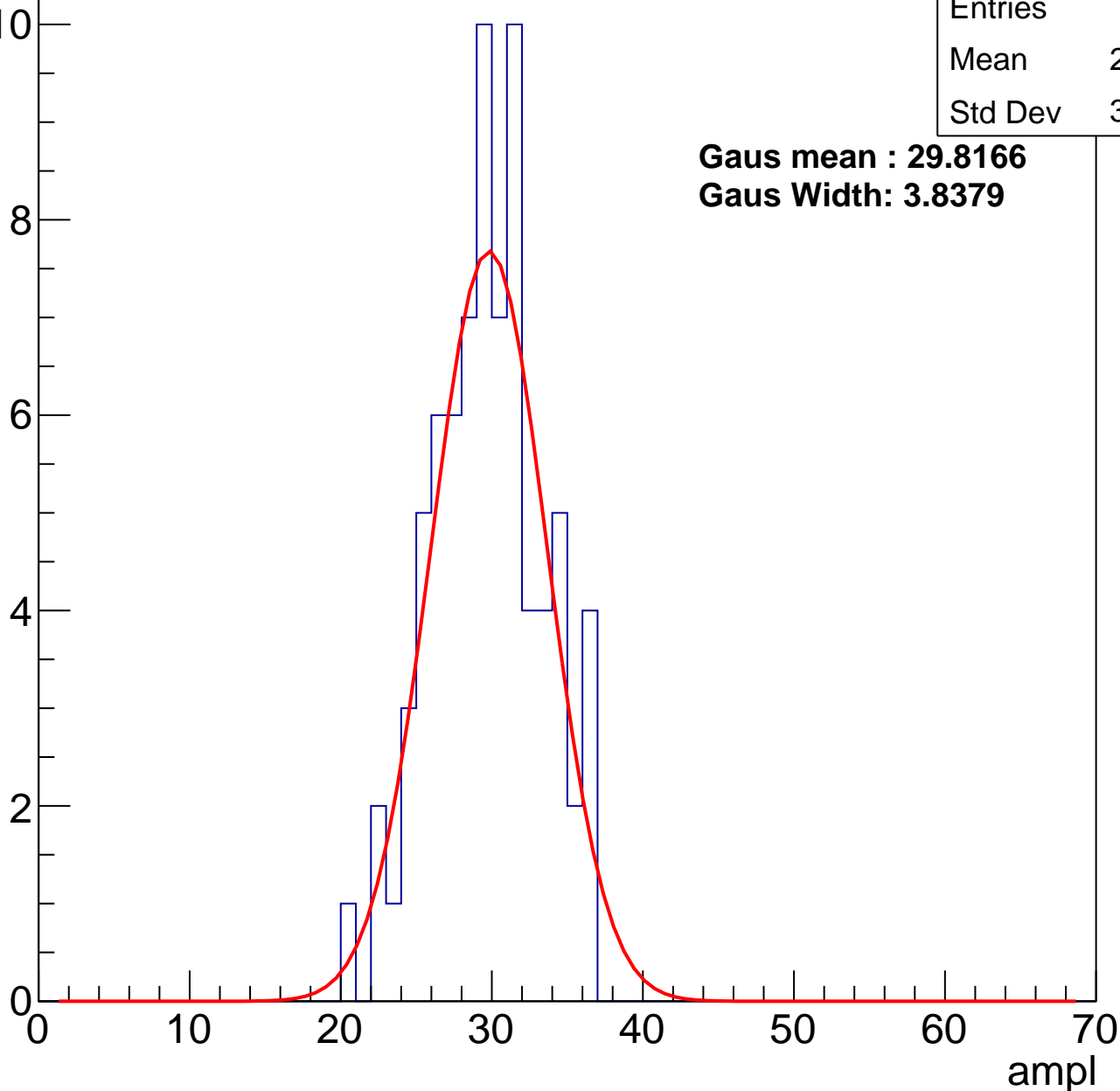
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	77
Mean	29.25
Std Dev	3.586

**Gaus mean : 29.8166**

**Gaus Width: 3.8379**



# B0L001S, U10-ch85, adc1

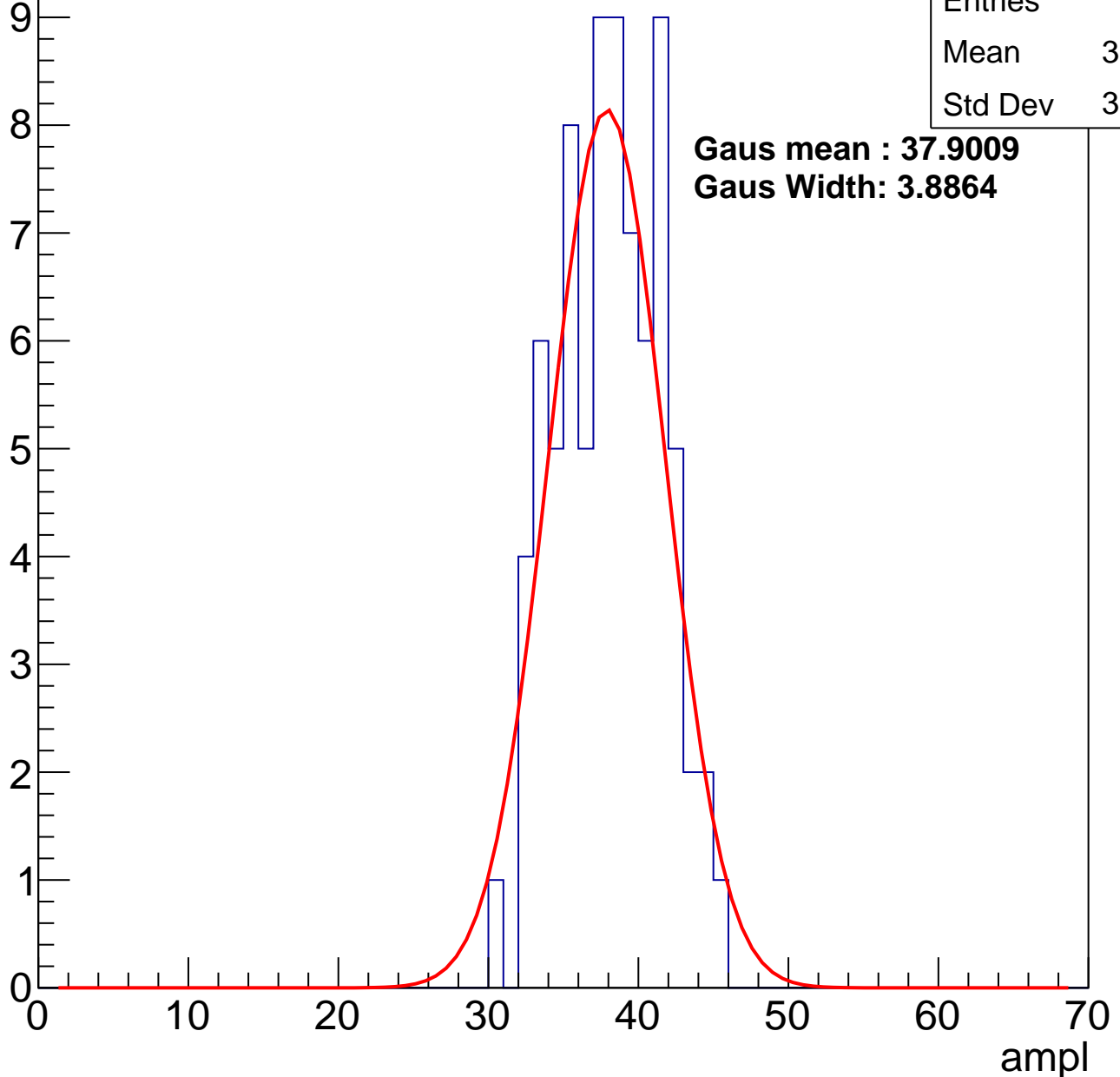
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	79
Mean	37.62
Std Dev	3.358

**Gaus mean : 37.9009**

**Gaus Width: 3.8864**



# B0L001S, U10-ch85, adc2

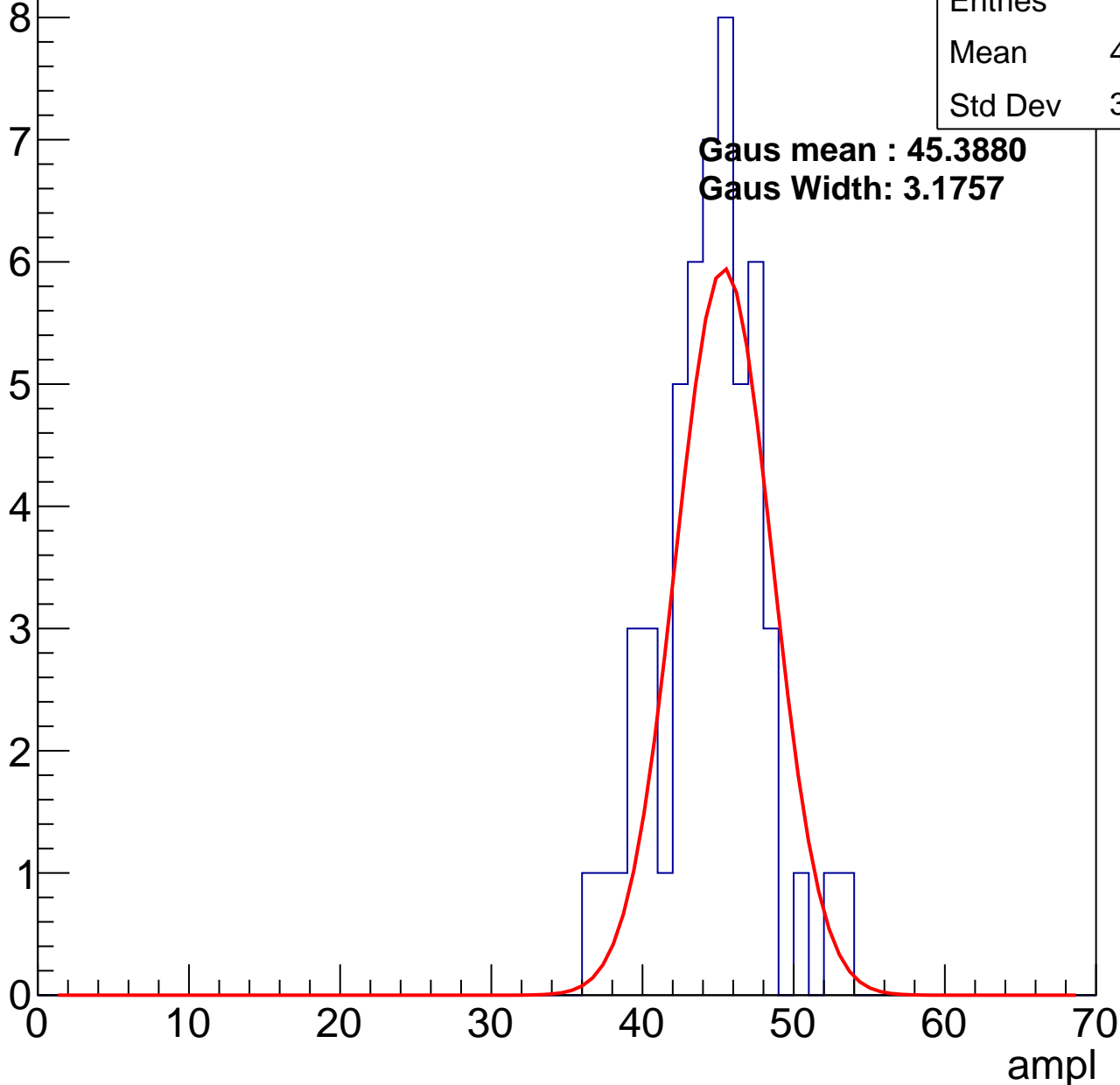
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	44.08
Std Dev	3.414

**Gaus mean : 45.3880**

**Gaus Width: 3.1757**



# B0L001S, U10-ch85, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

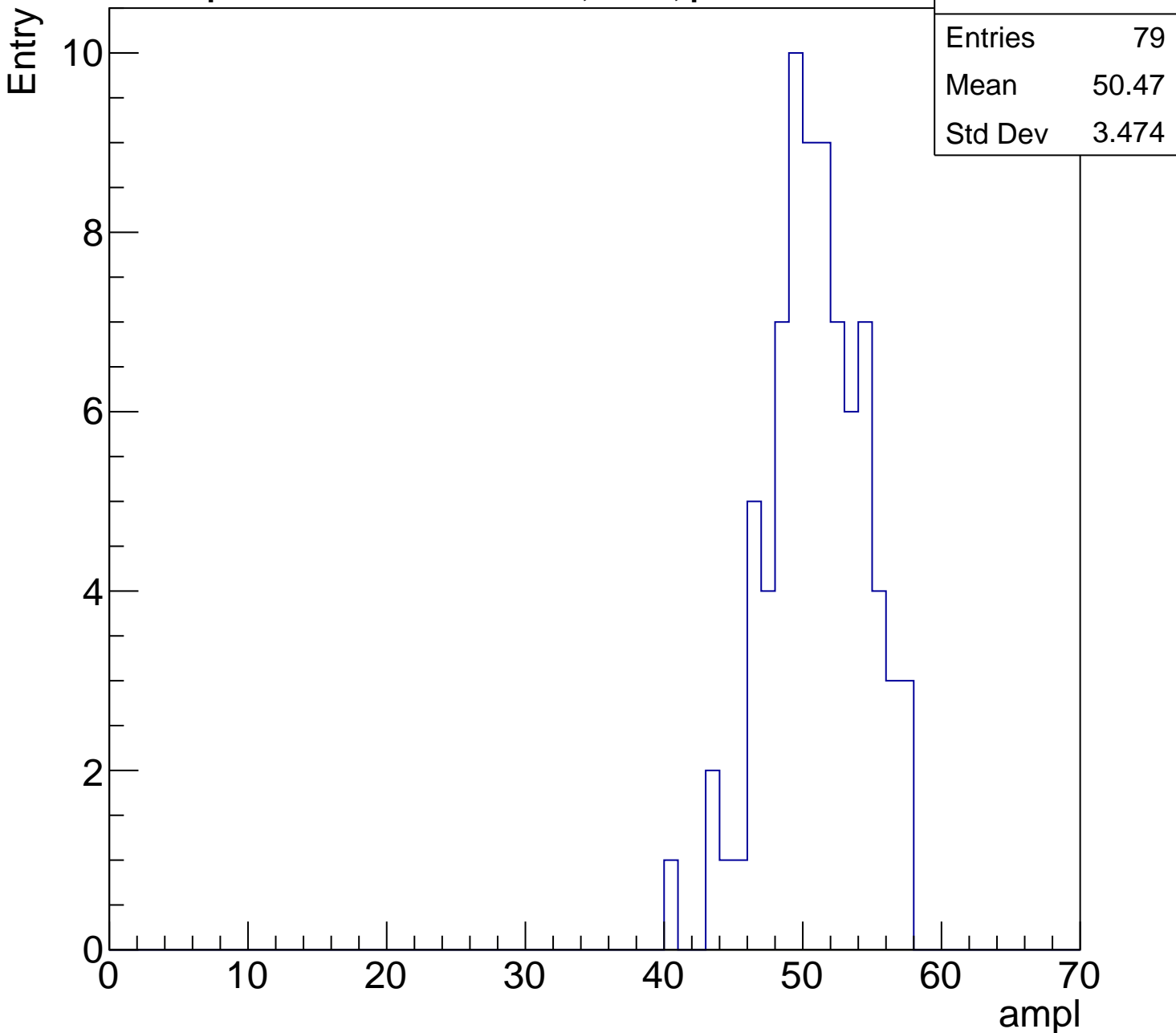
Entries	79
Mean	50.47
Std Dev	3.474

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

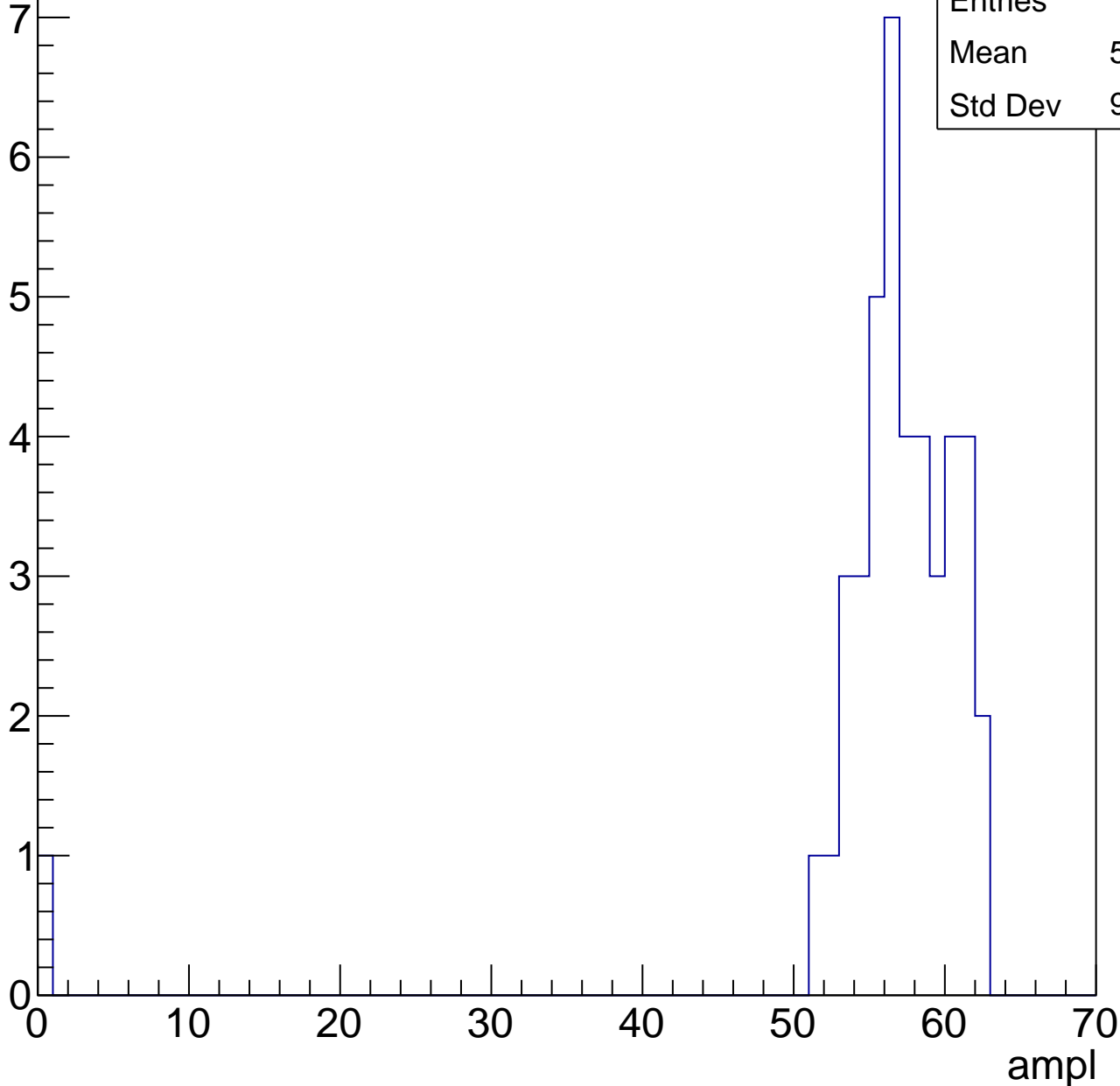


# B0L001S, U10-ch85, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	42
Mean	55.62
Std Dev	9.126



# B0L001S, U10-ch85, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

7

6

5

4

3

2

1

0

Entries	40
Mean	59.88
Std Dev	2.421

ampl

0

10

20

30

40

50

60

70

# B0L001S, U10-ch85, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch85, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U10-ch86, adc0

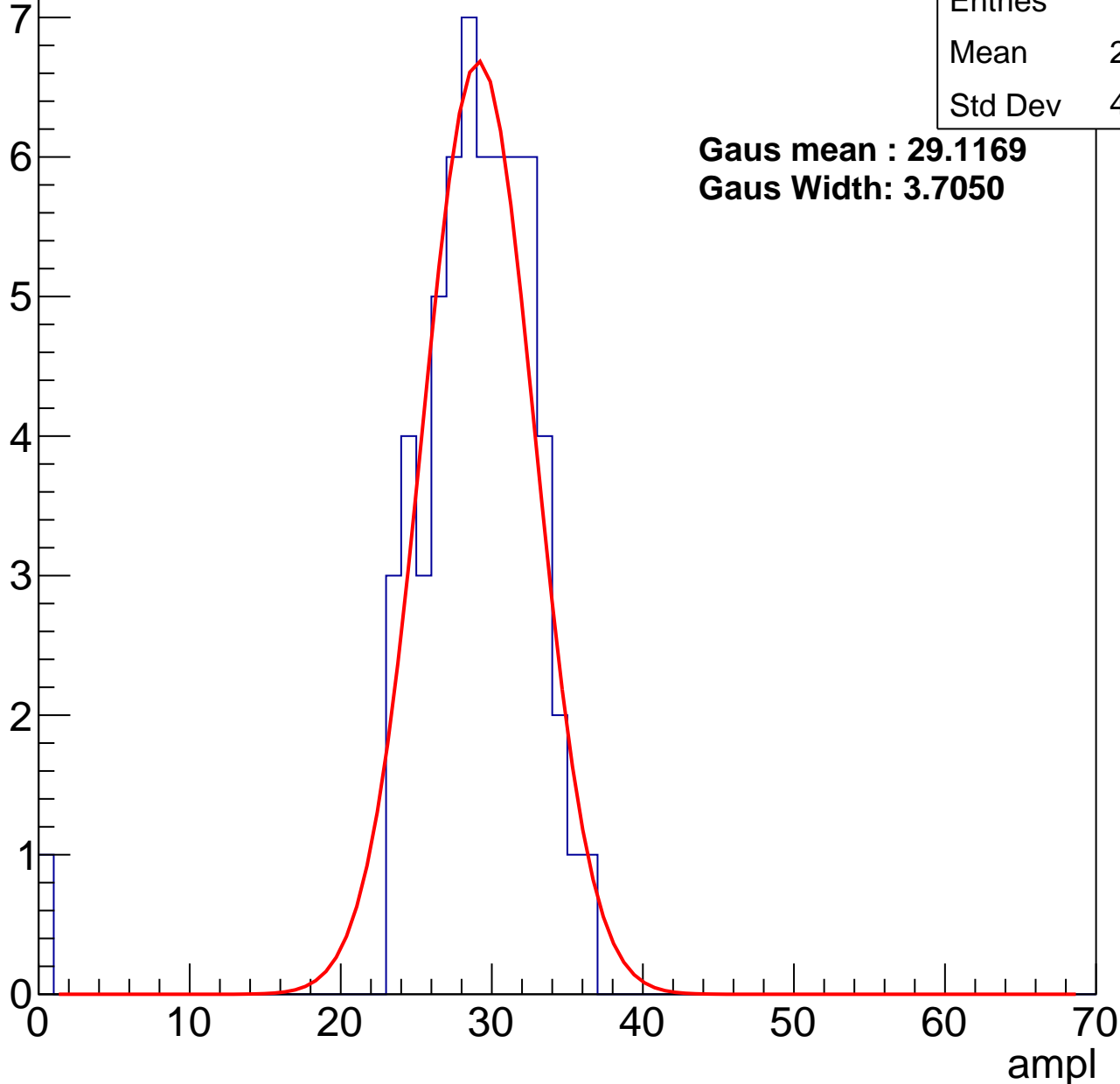
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	28.38
Std Dev	4.846

**Gaus mean : 29.1169**

**Gaus Width: 3.7050**



# B0L001S, U10-ch86, adc1

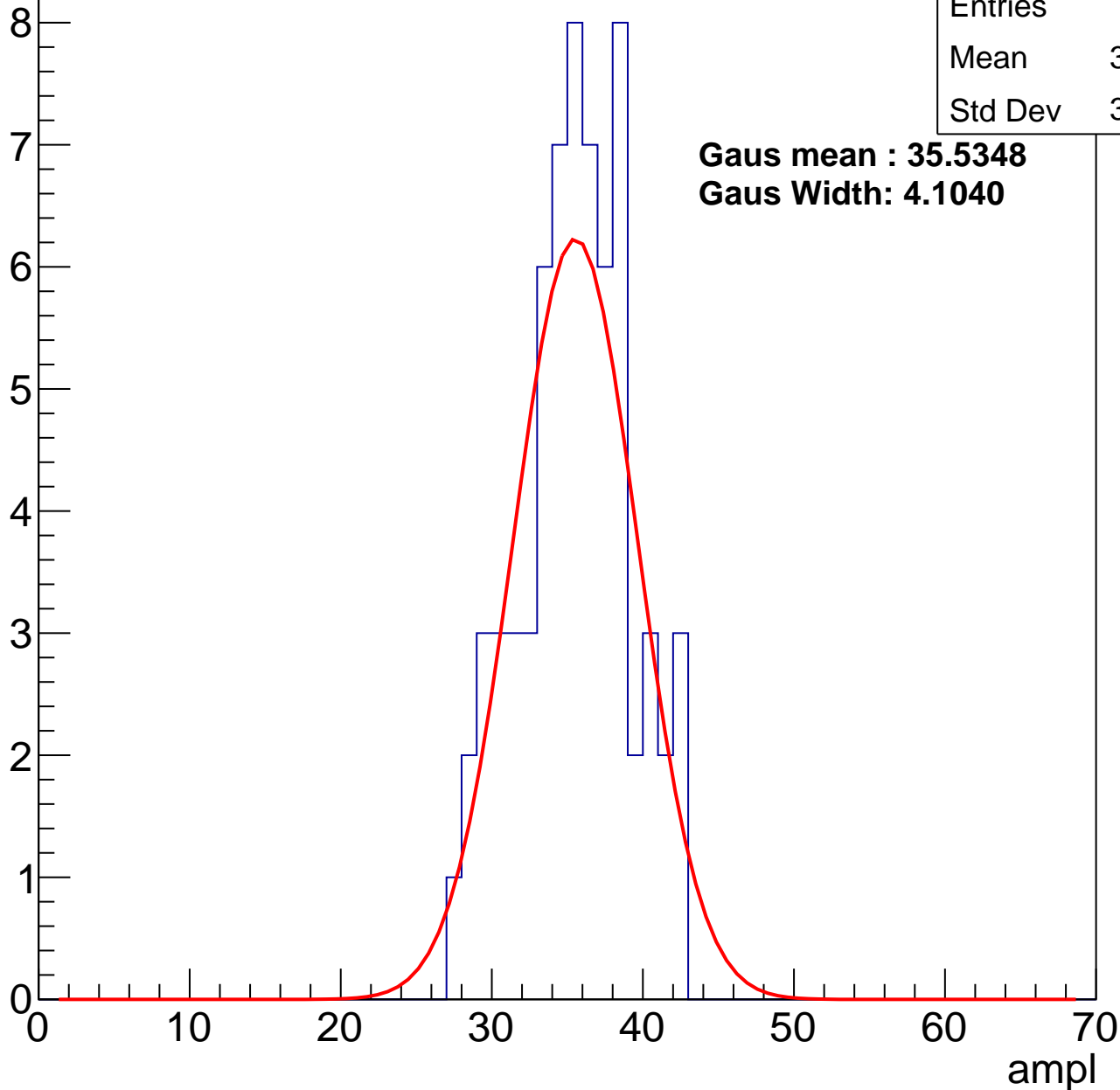
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	35.06
Std Dev	3.624

**Gaus mean : 35.5348**

**Gaus Width: 4.1040**



# B0L001S, U10-ch86, adc2

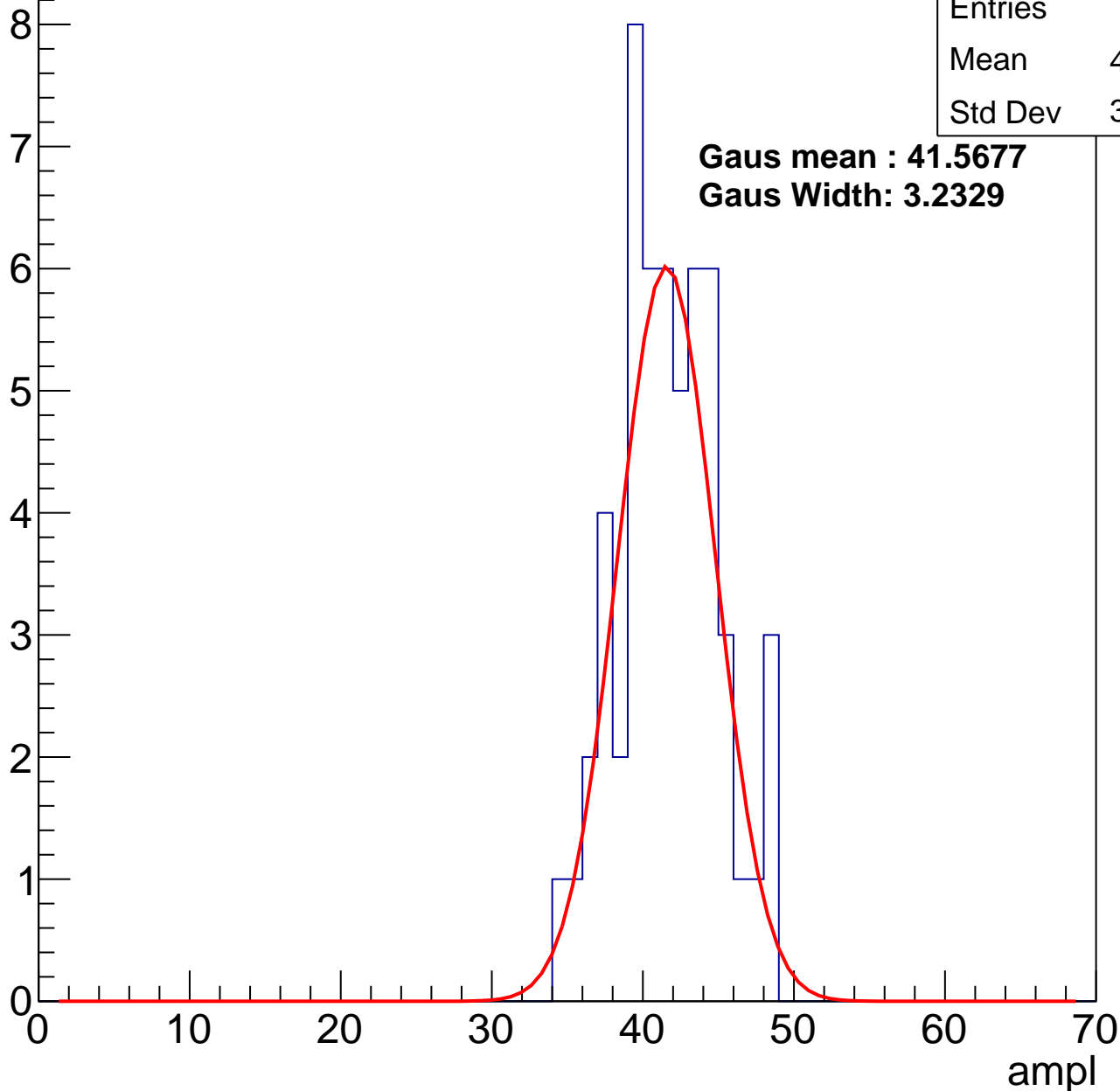
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	41.22
Std Dev	3.279

**Gaus mean : 41.5677**

**Gaus Width: 3.2329**

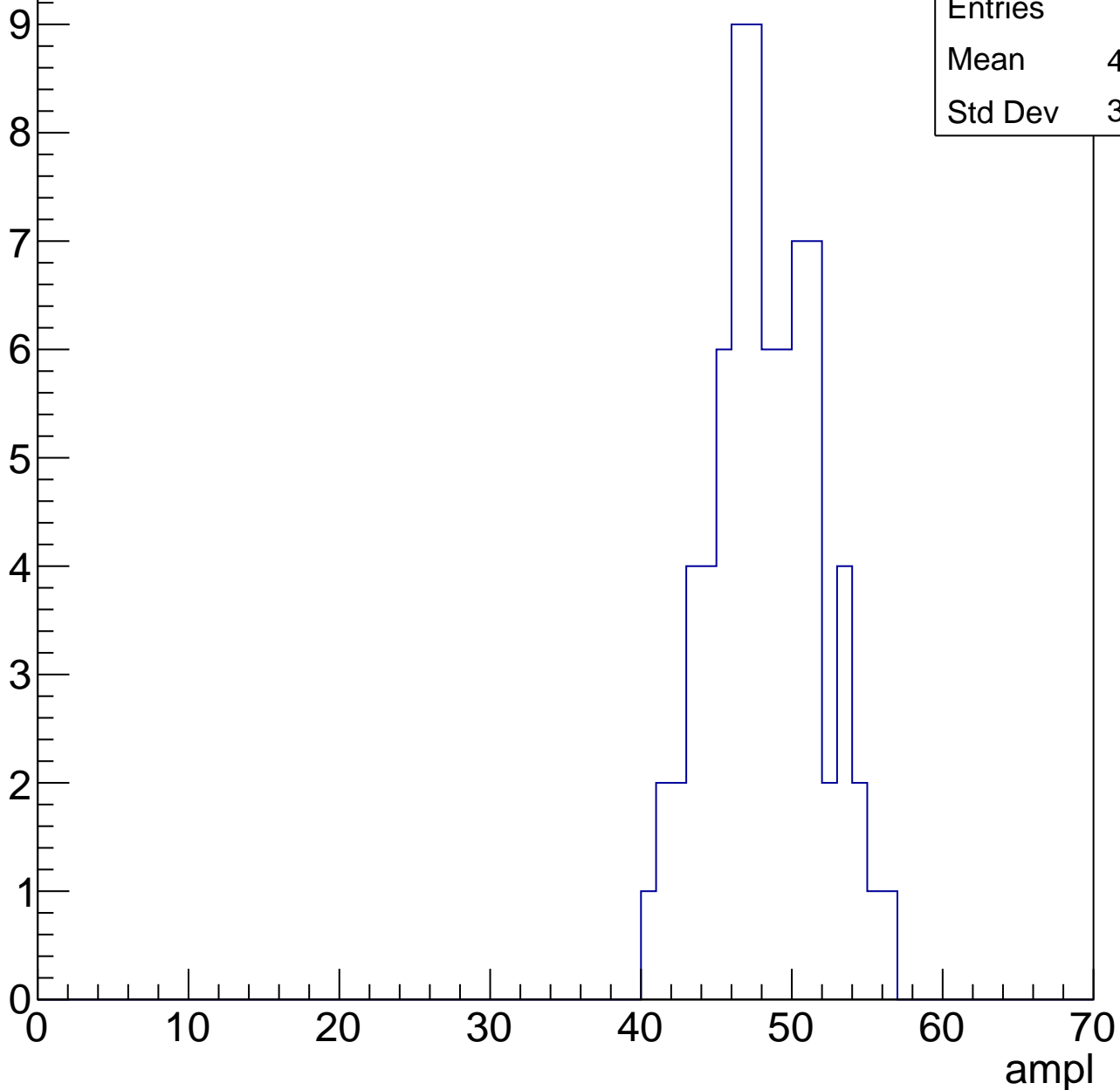


# B0L001S, U10-ch86, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	47.74
Std Dev	3.523

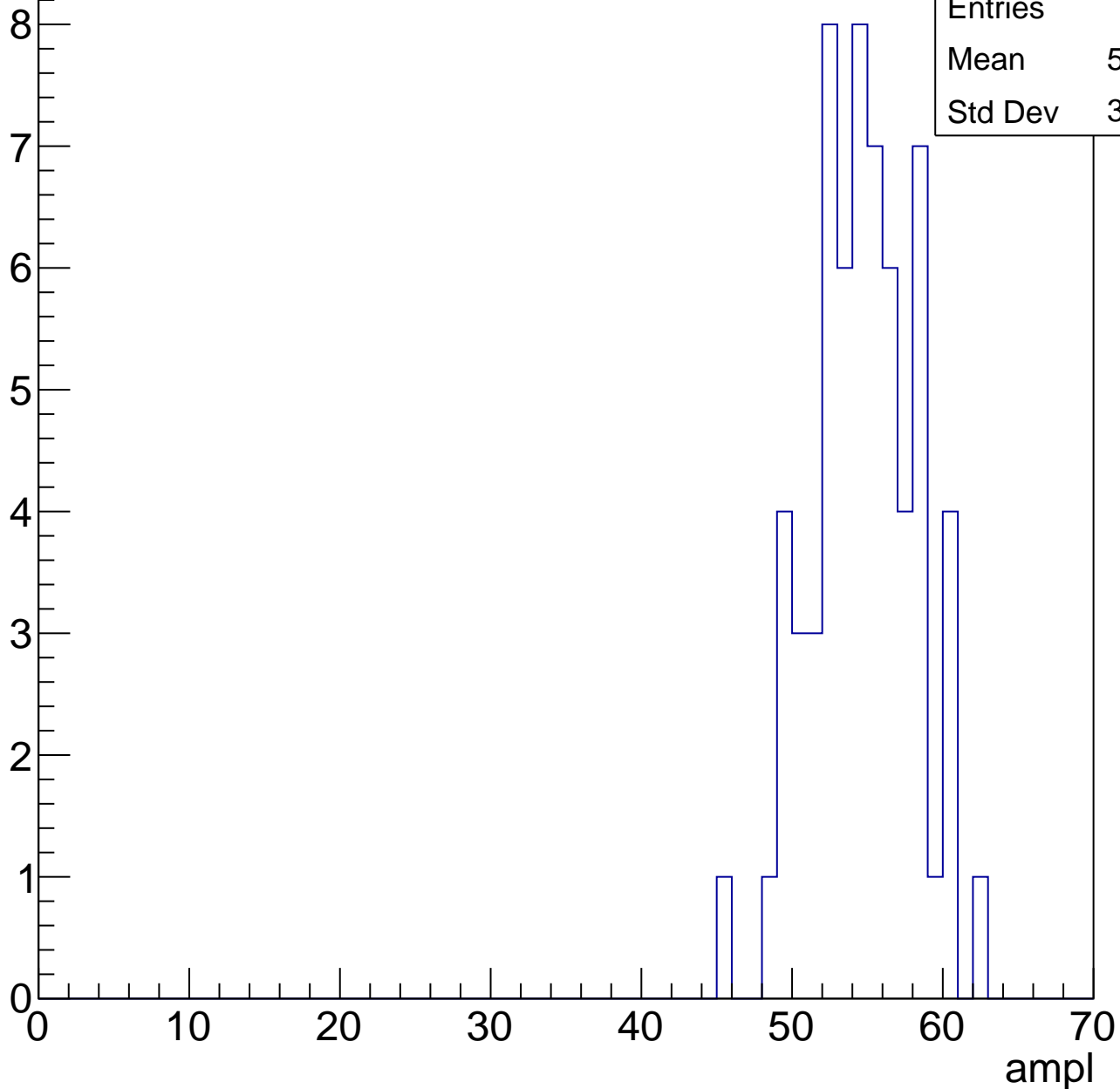


# B0L001S, U10-ch86, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

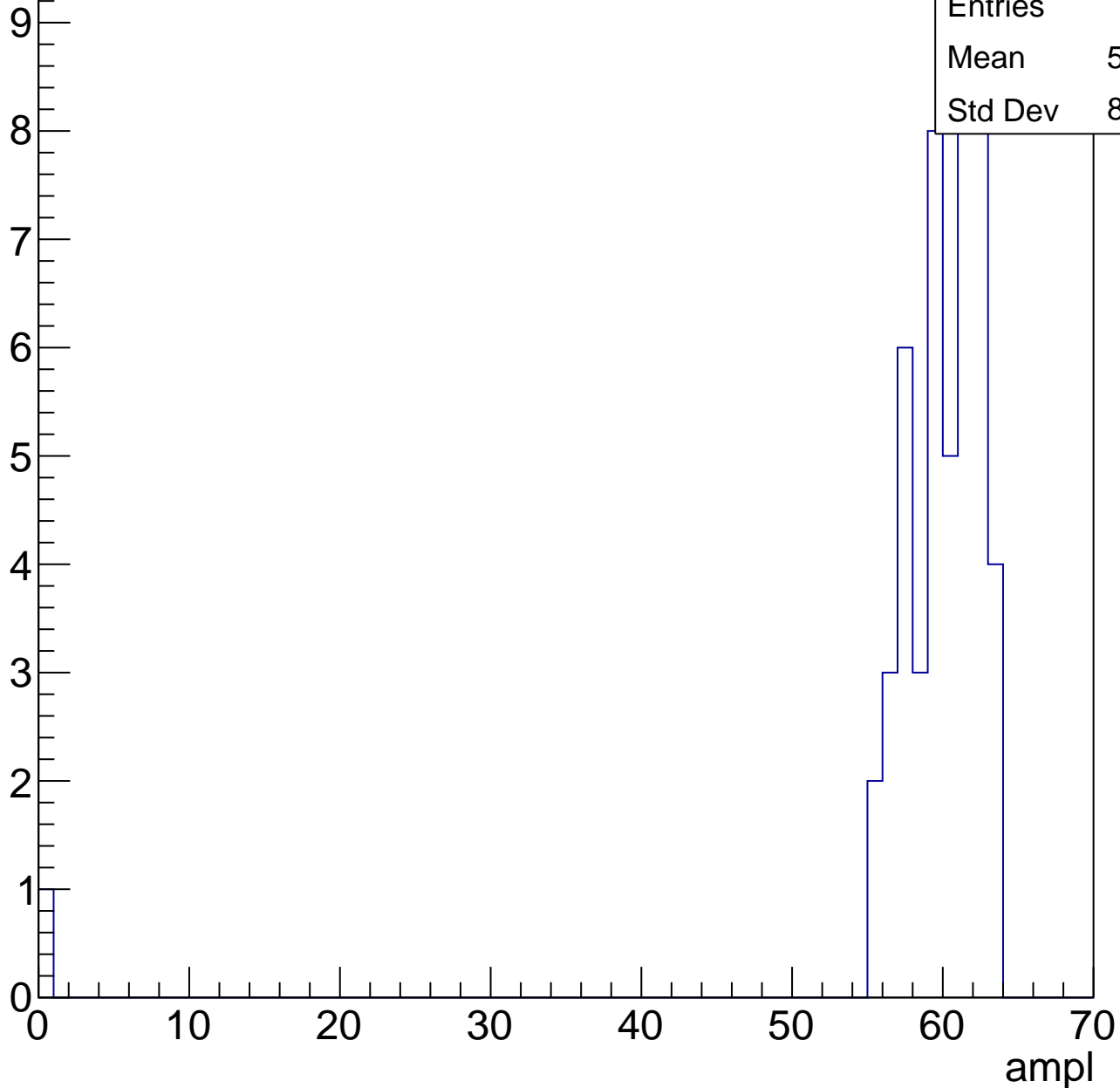
Entries	64
Mean	54.28
Std Dev	3.393



# B0L001S, U10-ch86, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

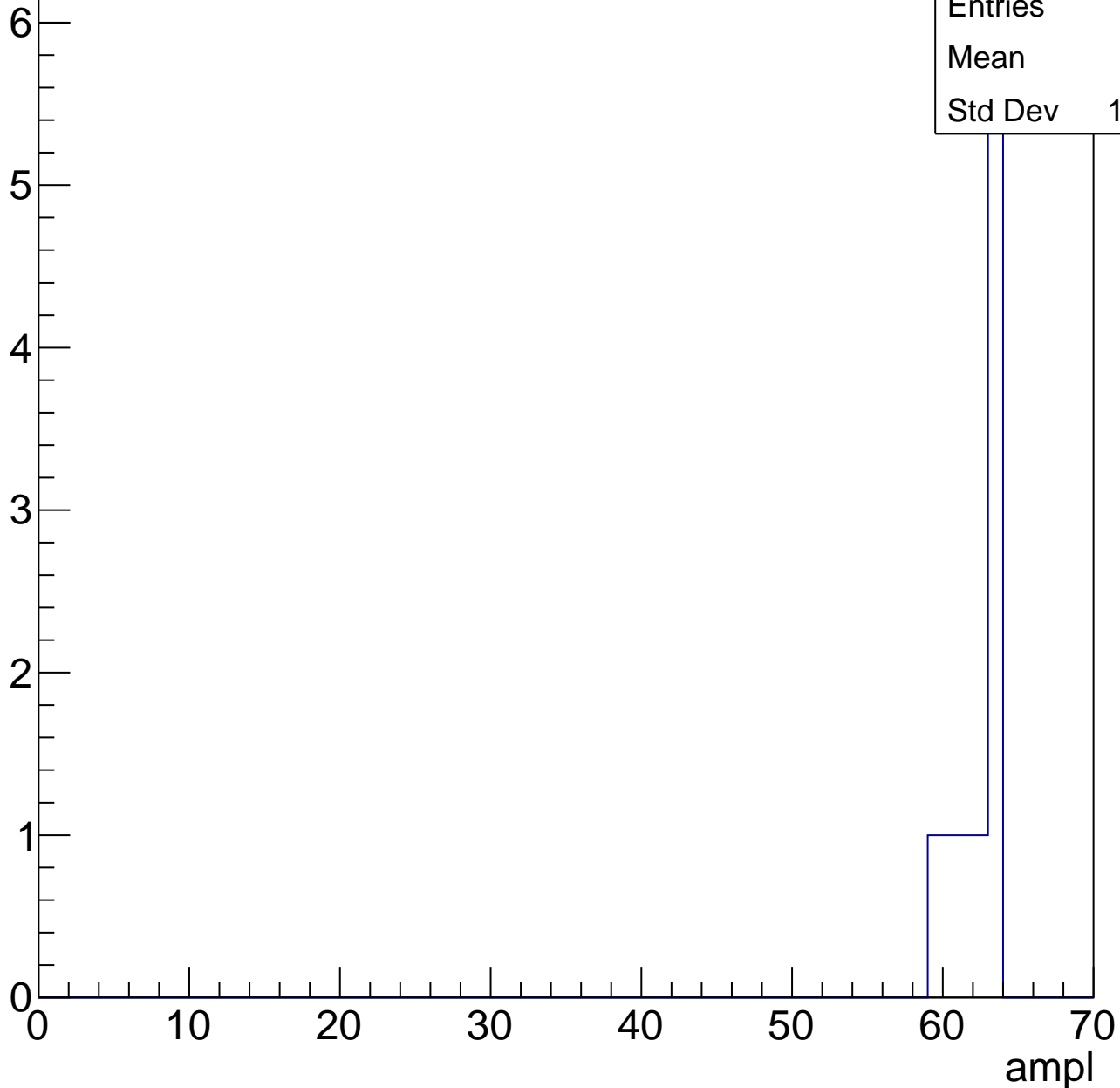


# B0L001S, U10-ch86, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	10
Mean	62
Std Dev	1.414





# B0L001S, U10-ch86, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U10-ch87, adc0

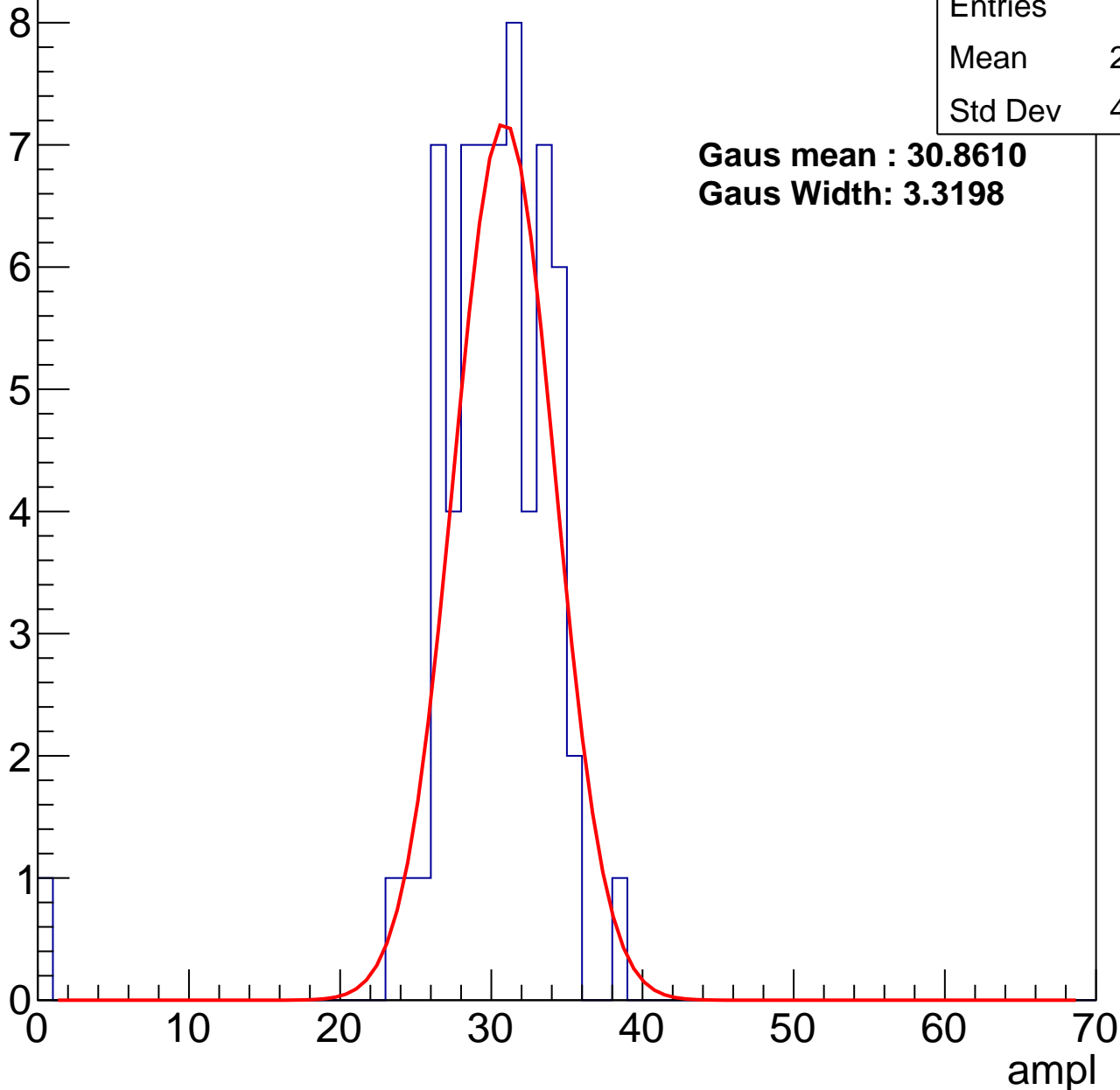
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	29.53
Std Dev	4.802

**Gaus mean : 30.8610**

**Gaus Width: 3.3198**



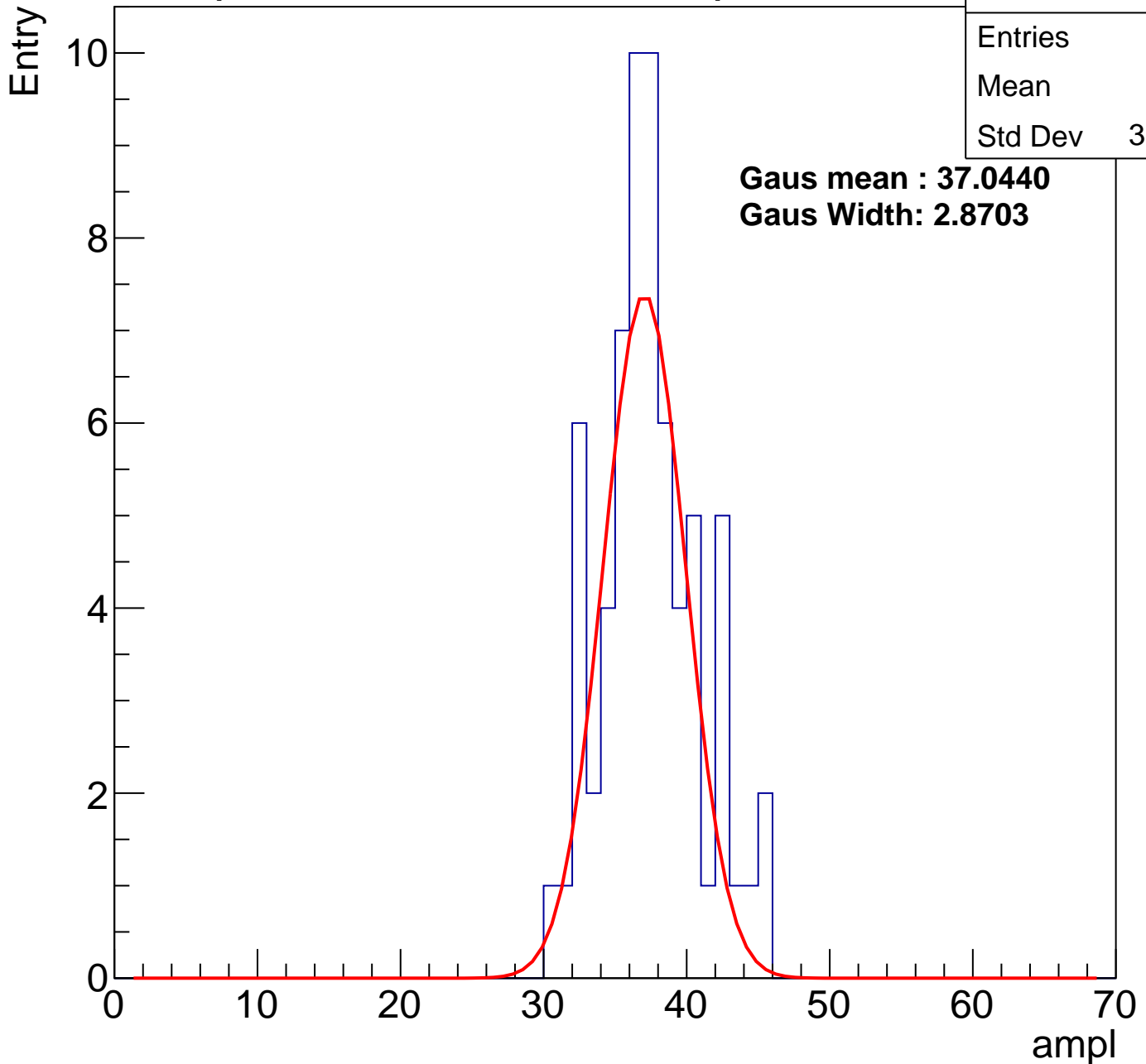
# B0L001S, U10-ch87, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	66
Mean	37
Std Dev	3.398

**Gaus mean : 37.0440**

**Gaus Width: 2.8703**



# B0L001S, U10-ch87, adc2

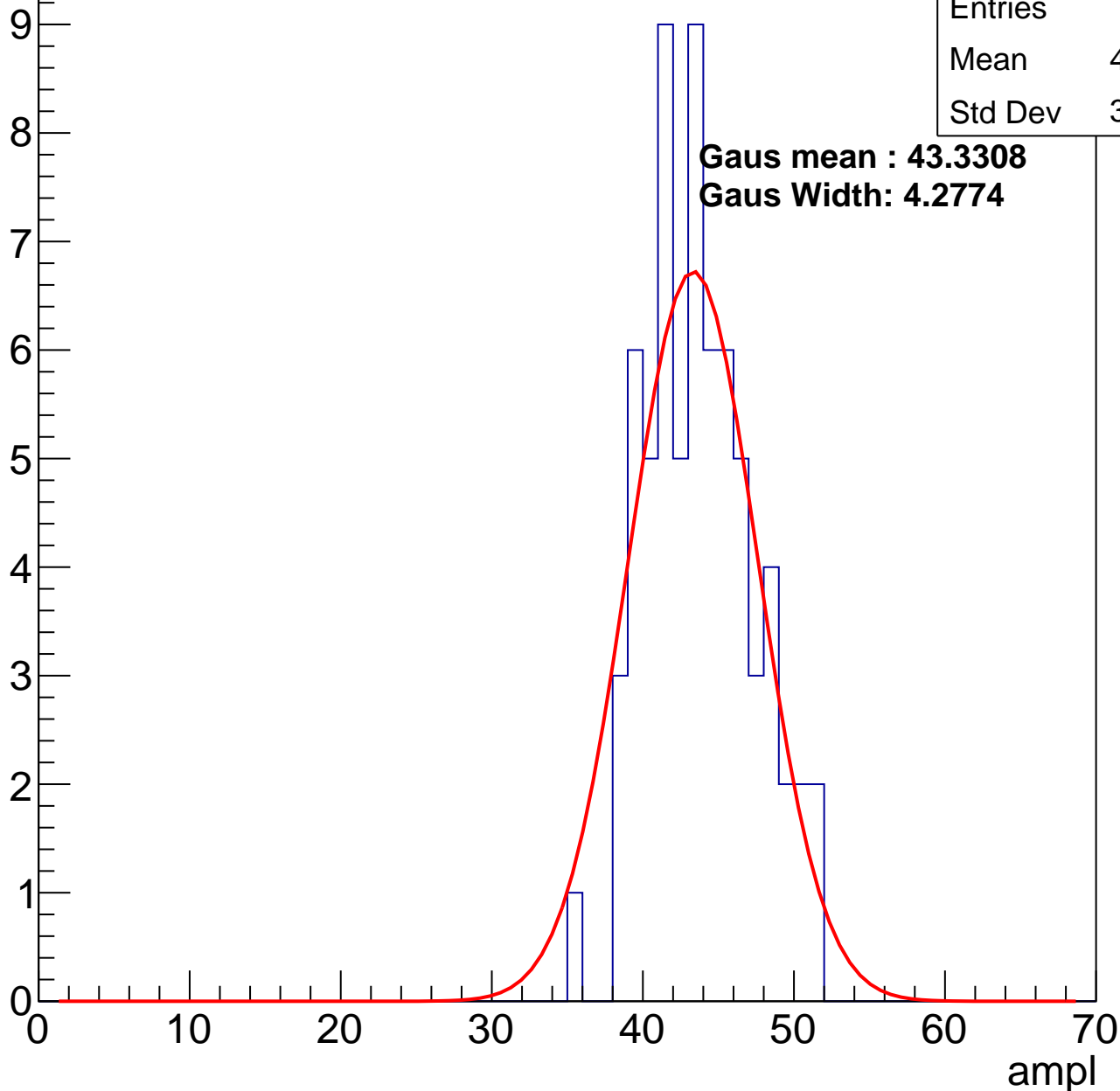
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	43.32
Std Dev	3.504

**Gaus mean : 43.3308**

**Gaus Width: 4.2774**



# B0L001S, U10-ch87, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	81
Mean	50.67
Std Dev	3.348

Entry

10

8

6

4

2

0

0

10

20

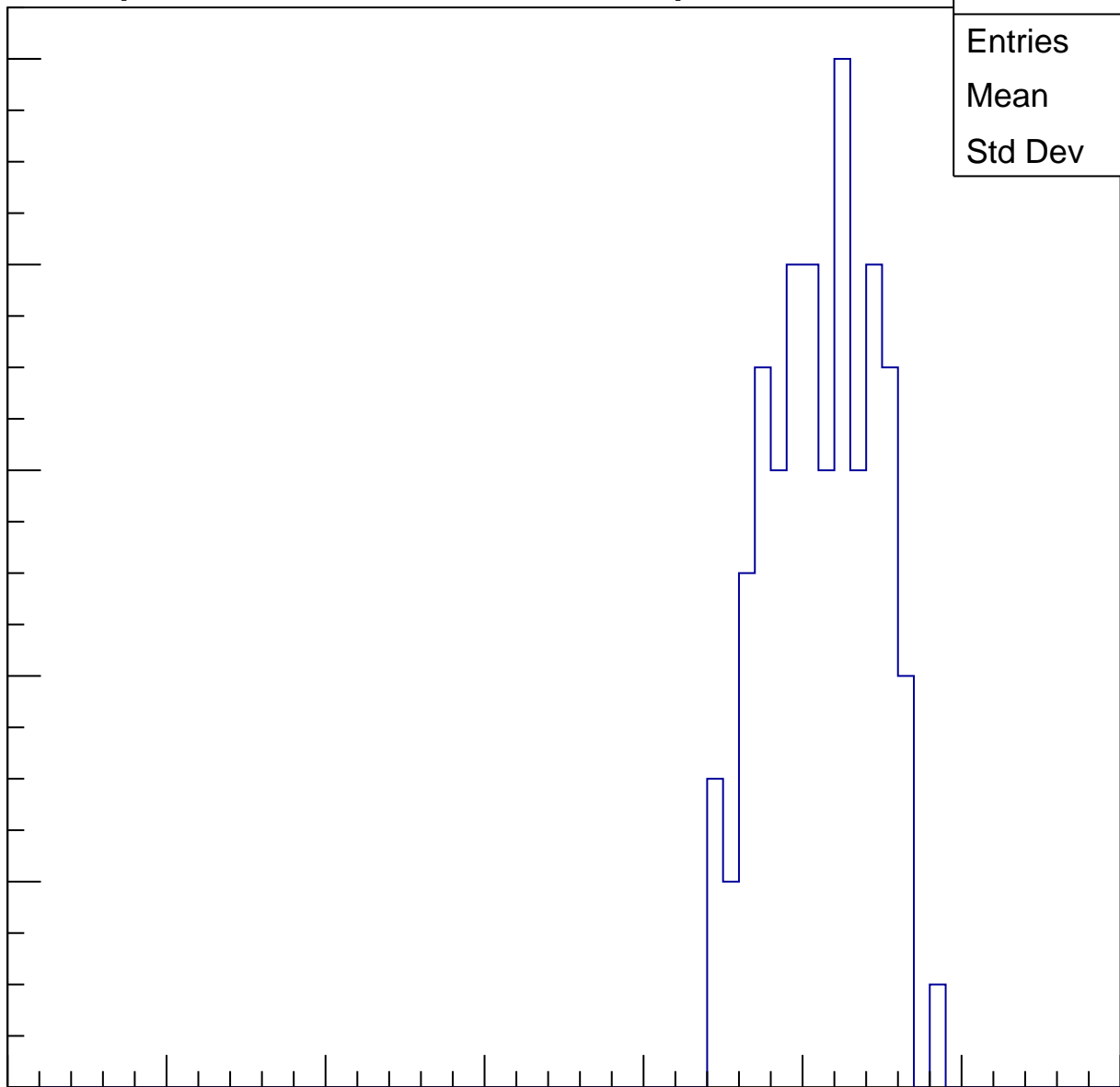
30

40

50

60

ampl

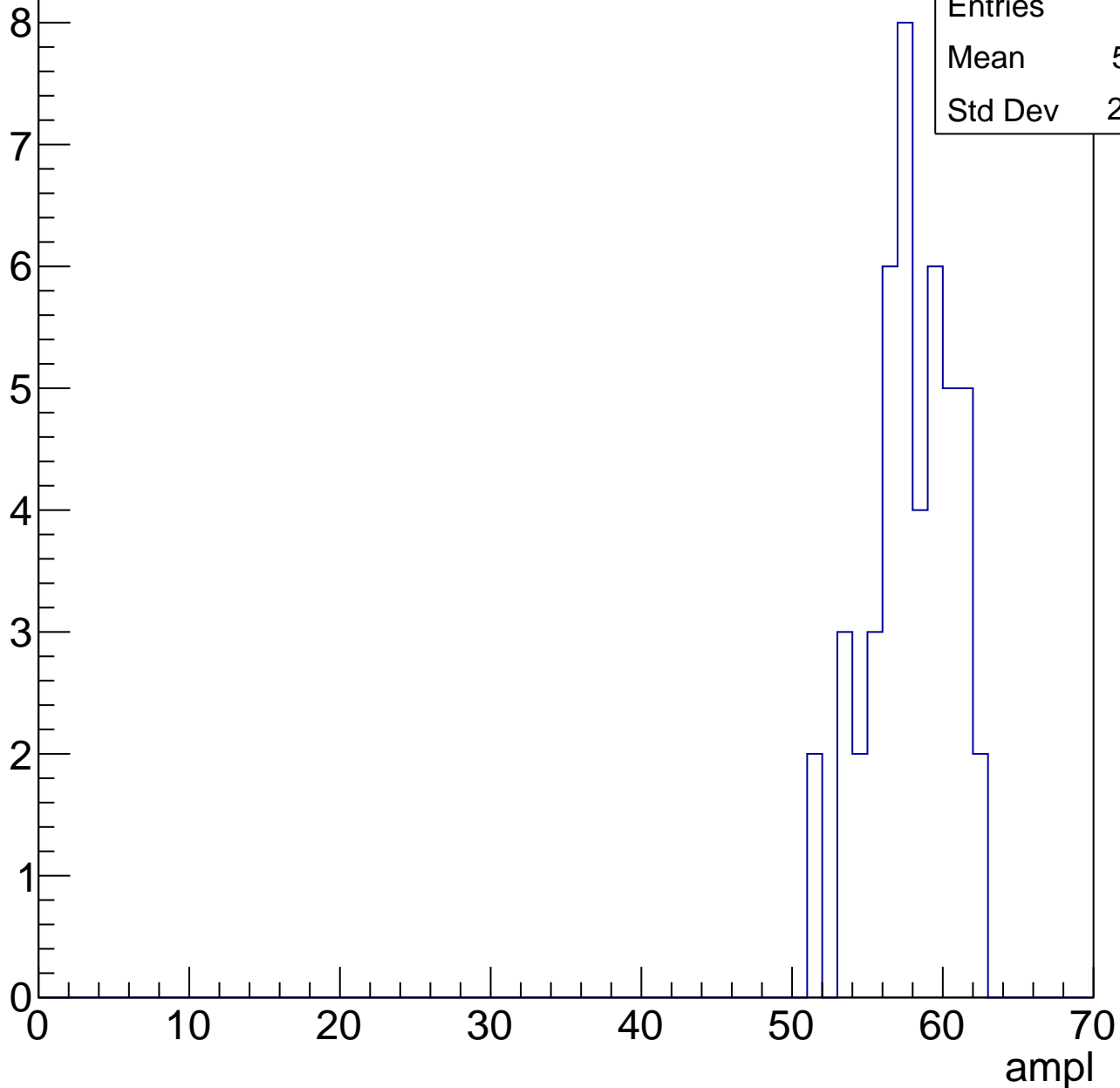


# B0L001S, U10-ch87, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	46
Mean	57.41
Std Dev	2.763

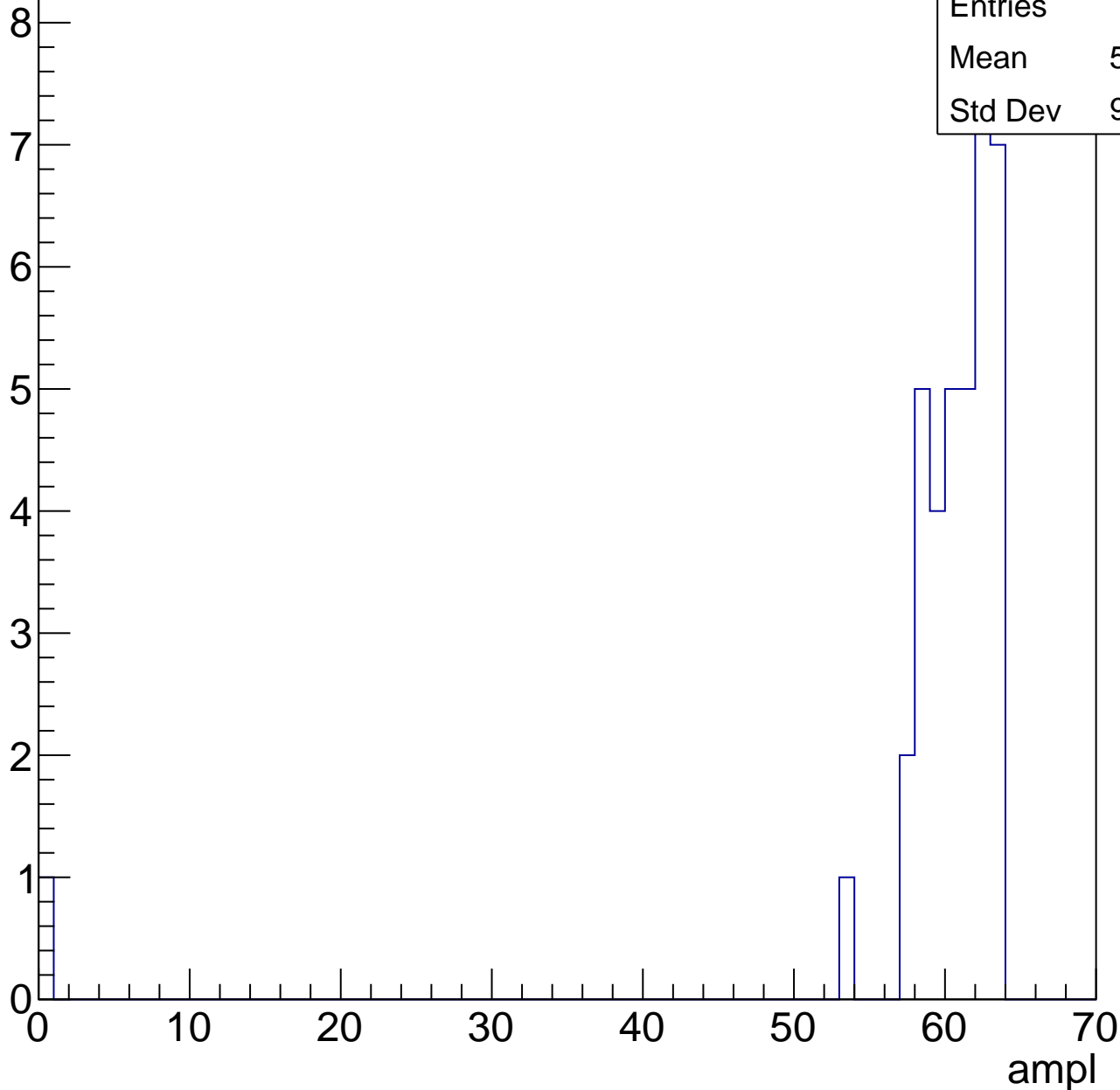


# B0L001S, U10-ch87, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	38
Mean	58.82
Std Dev	9.918



# B0L001S, U10-ch87, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch87, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U10-ch88, adc0

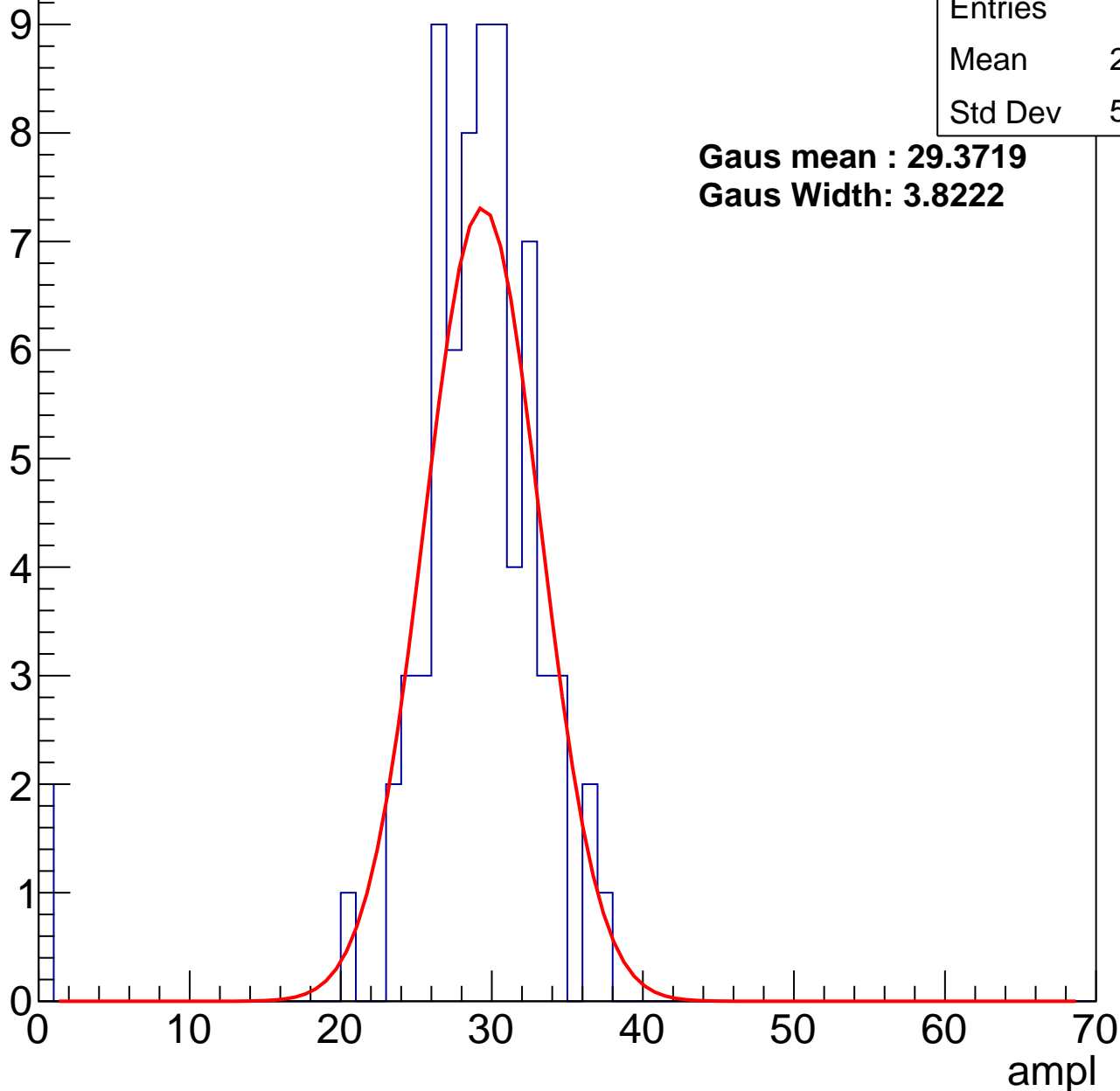
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	28.08
Std Dev	5.754

**Gaus mean : 29.3719**

**Gaus Width: 3.8222**



# B0L001S, U10-ch88, adc1

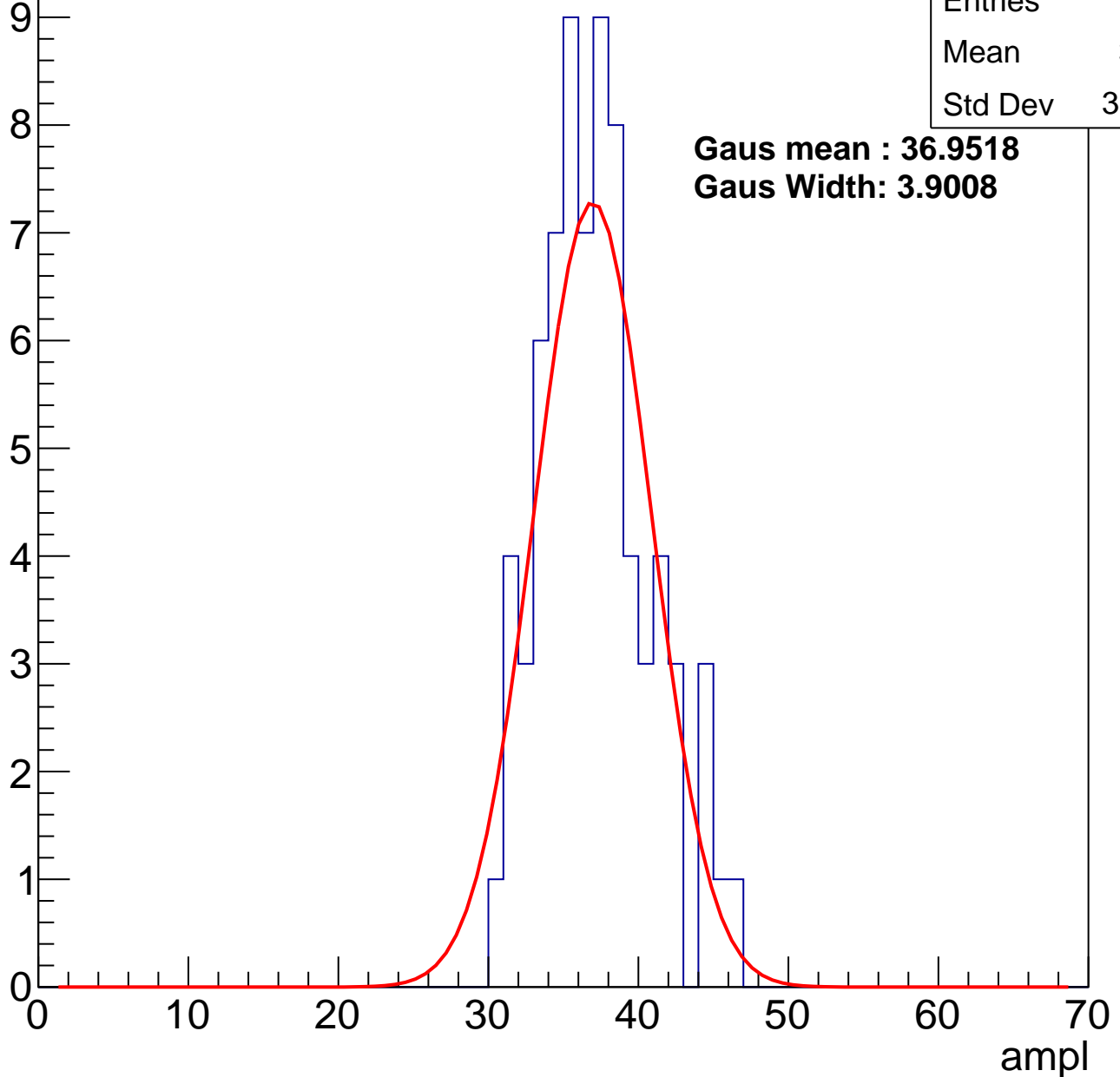
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	36.7
Std Dev	3.599

**Gaus mean : 36.9518**

**Gaus Width: 3.9008**



# B0L001S, U10-ch88, adc2

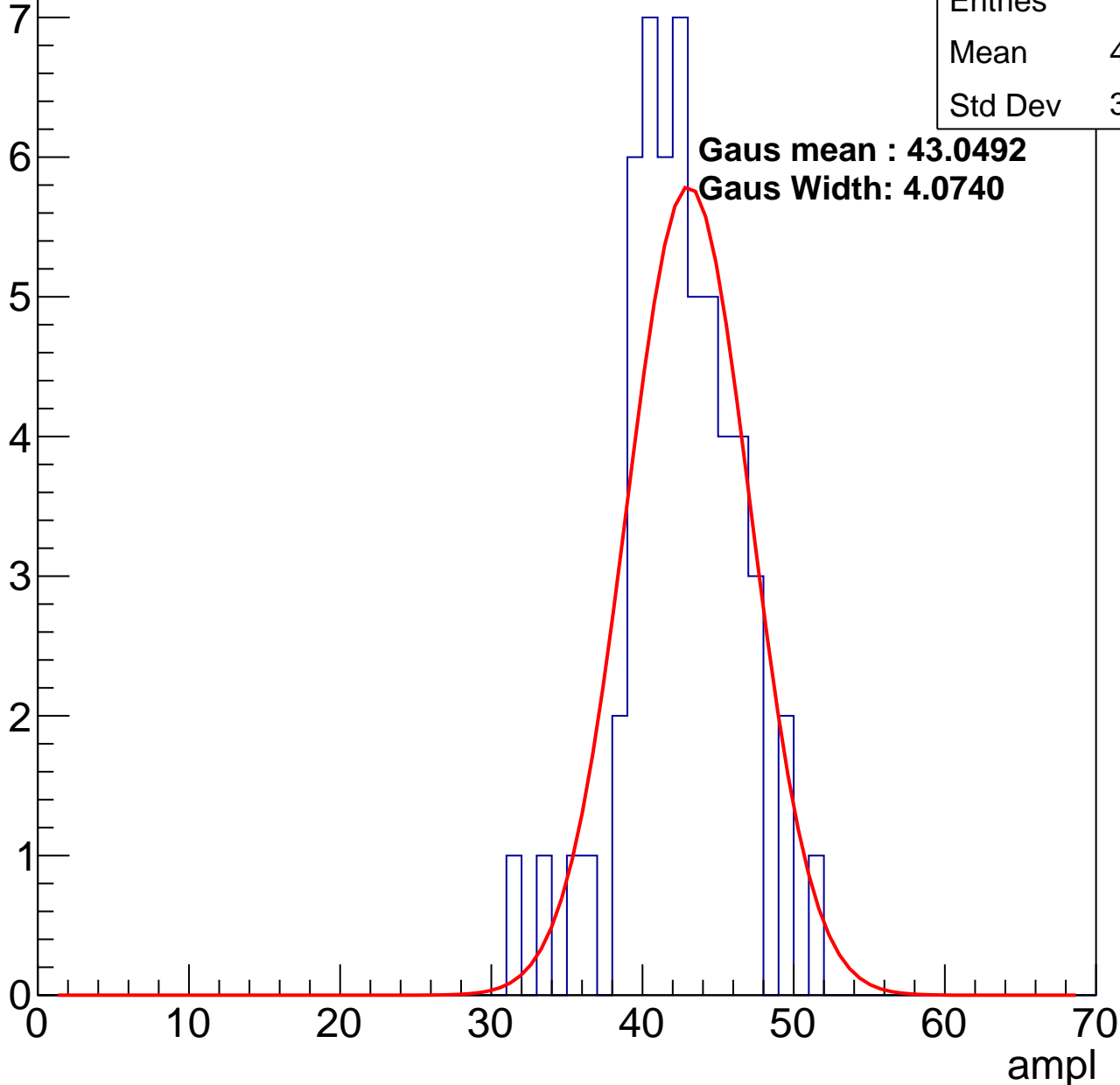
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	42.04
Std Dev	3.746

**Gaus mean : 43.0492**

**Gaus Width: 4.0740**



# B0L001S, U10-ch88, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

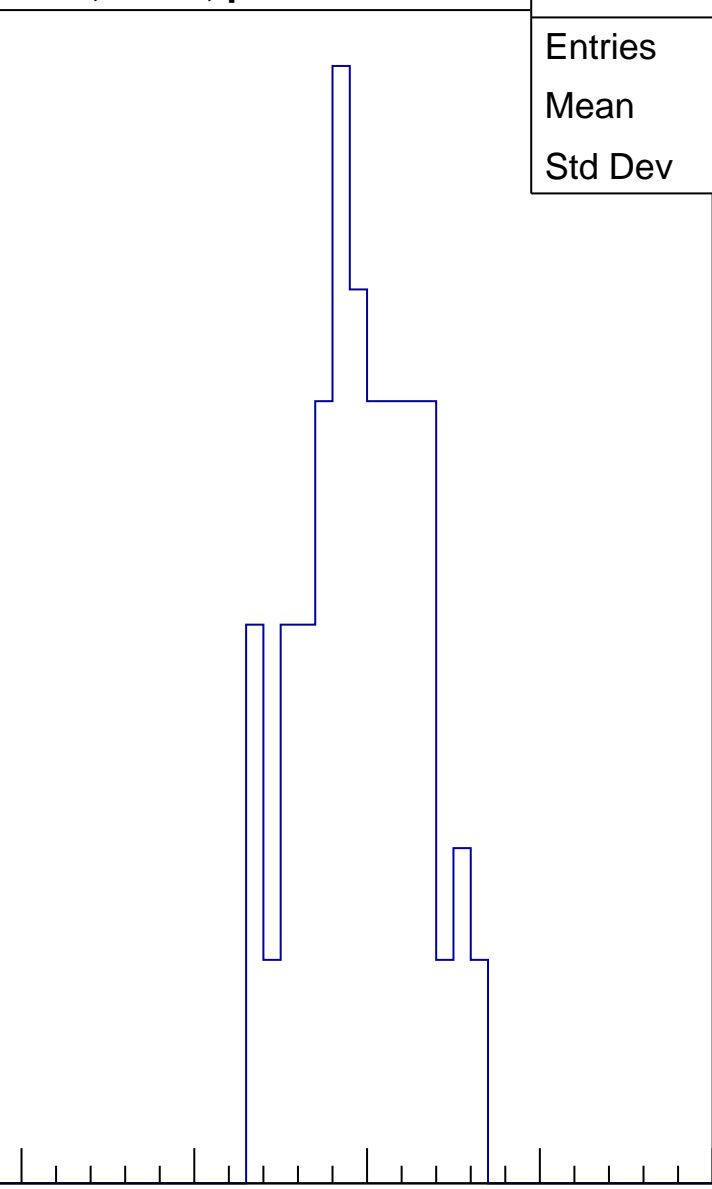
Entries	77
Mean	49.17
Std Dev	3.336

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

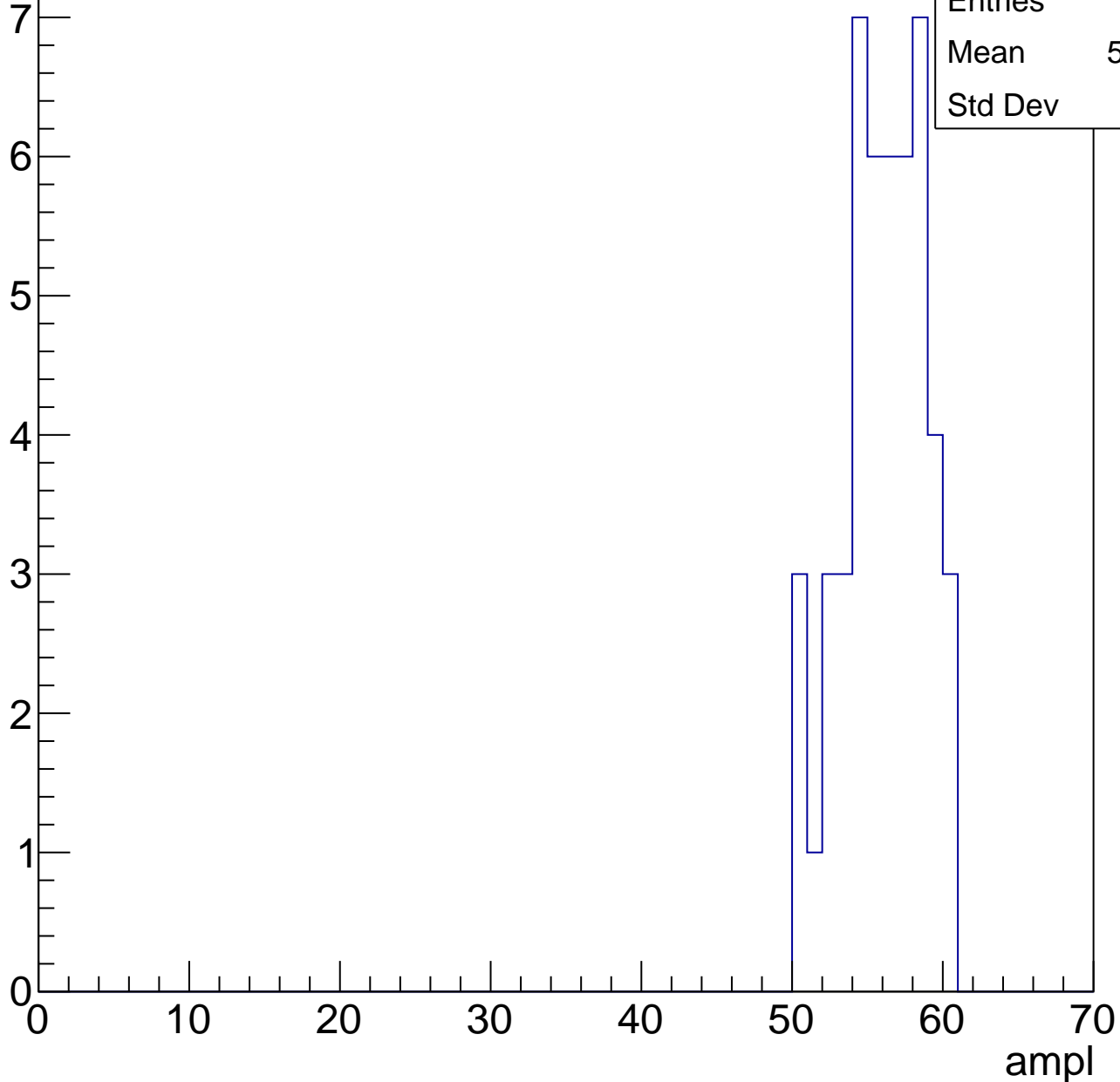
ampl



# B0L001S, U10-ch88, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



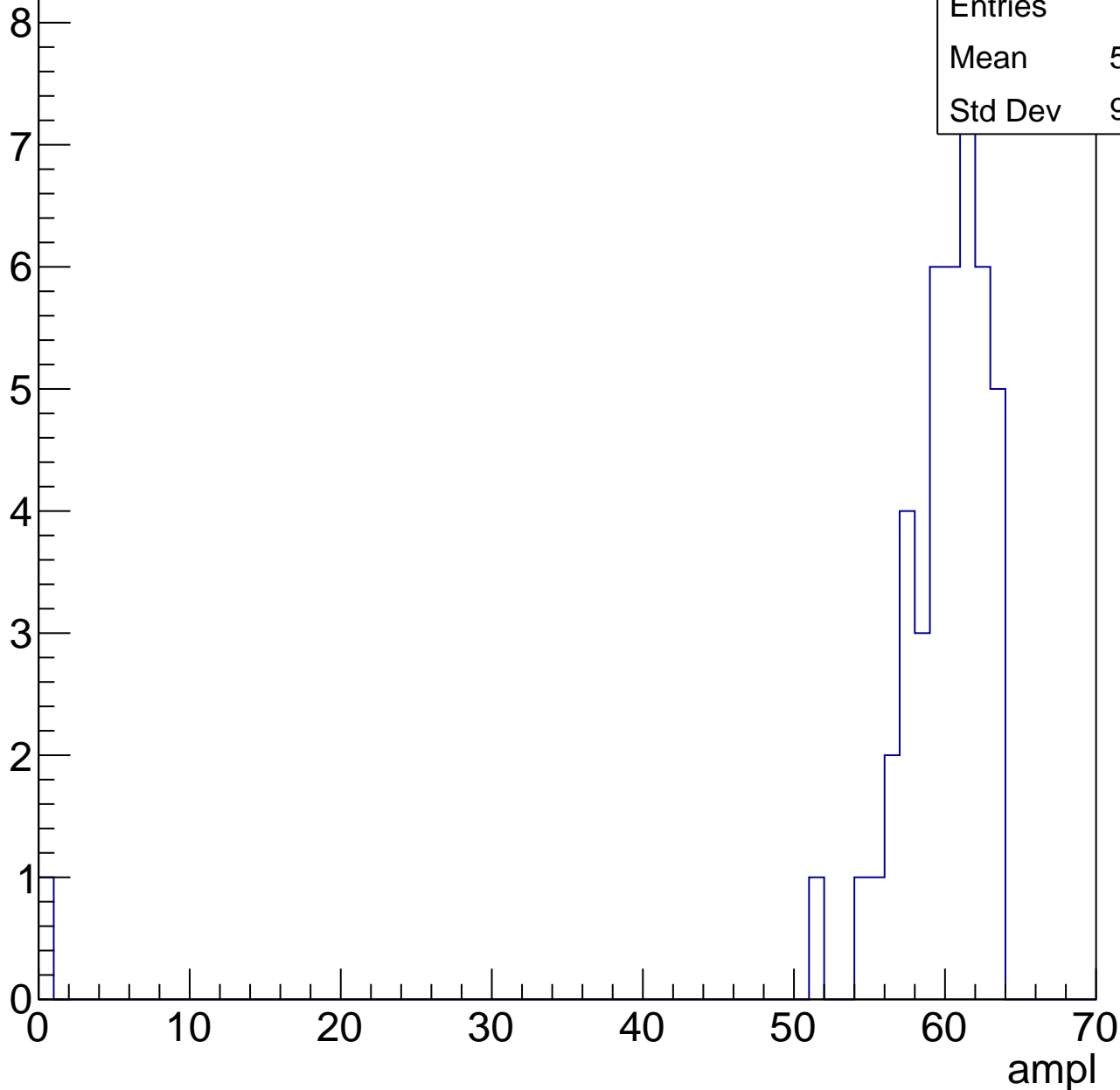
Entries	49
Mean	55.59
Std Dev	2.68

# B0L001S, U10-ch88, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	44
Mean	58.25
Std Dev	9.257

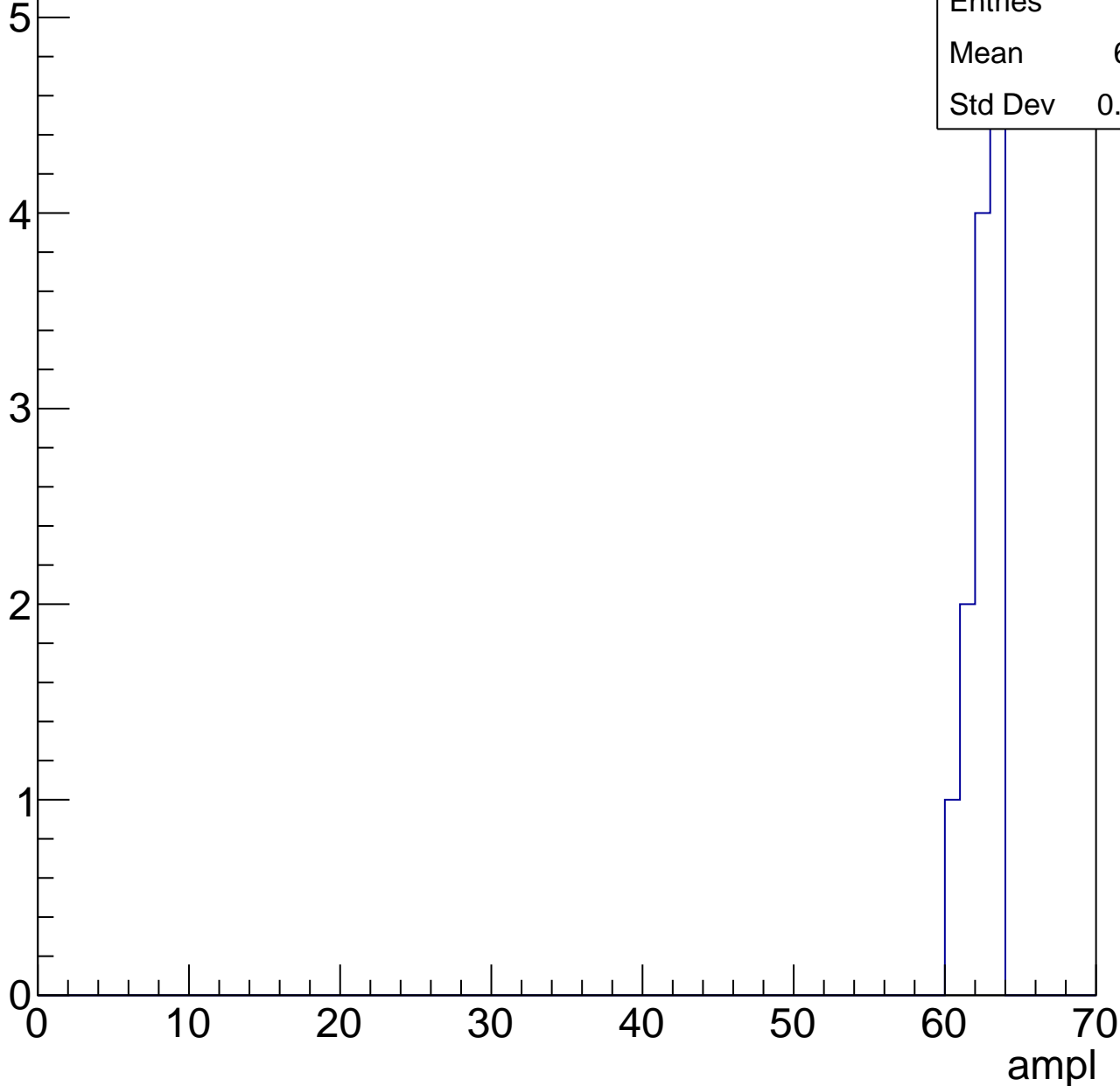


# B0L001S, U10-ch88, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	12
Mean	62.08
Std Dev	0.9538





# B0L001S, U10-ch88, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L001S, U10-ch89, adc0

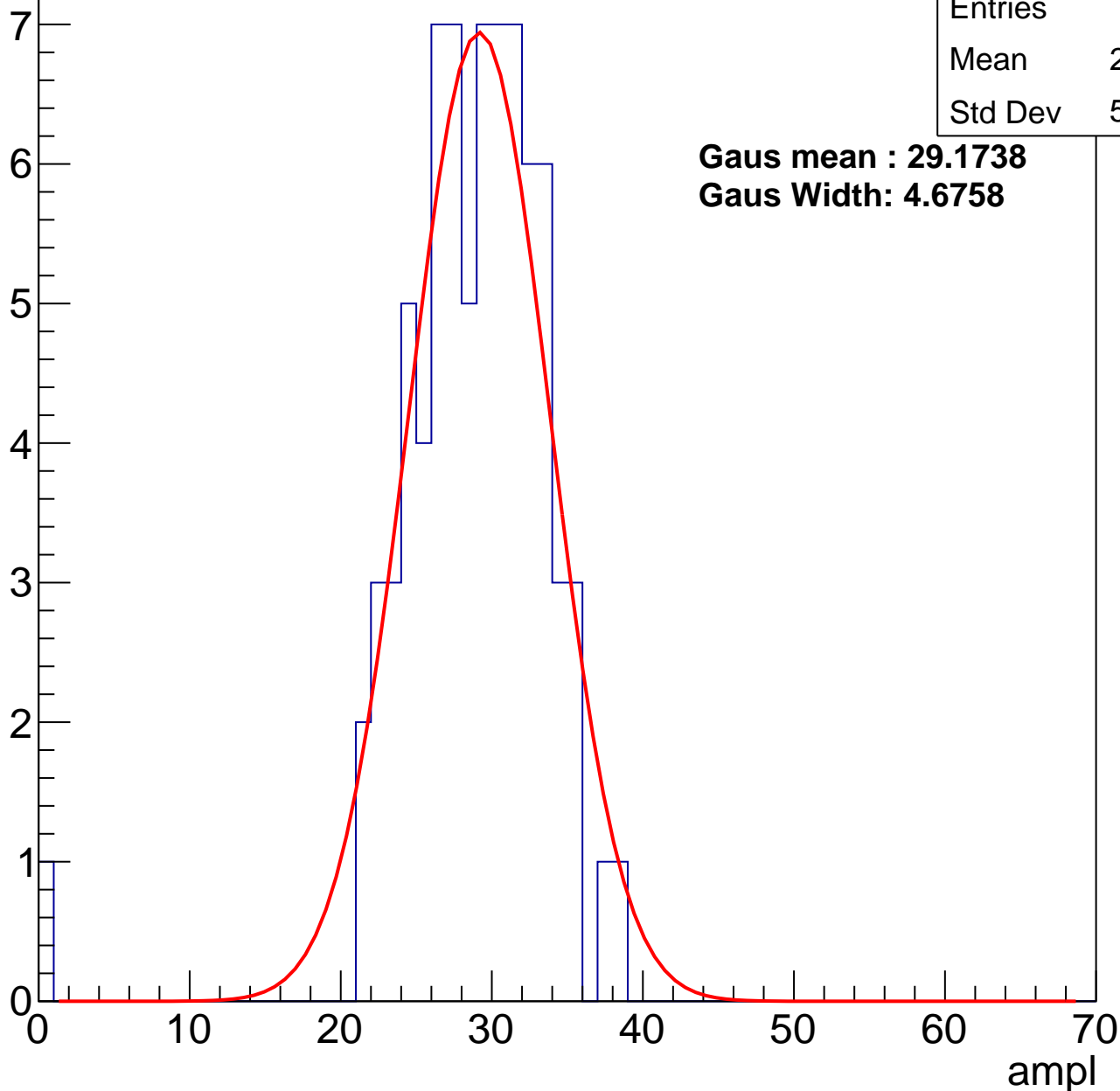
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	78
Mean	28.33
Std Dev	5.048

**Gaus mean : 29.1738**

**Gaus Width: 4.6758**



# B0L001S, U10-ch89, adc1

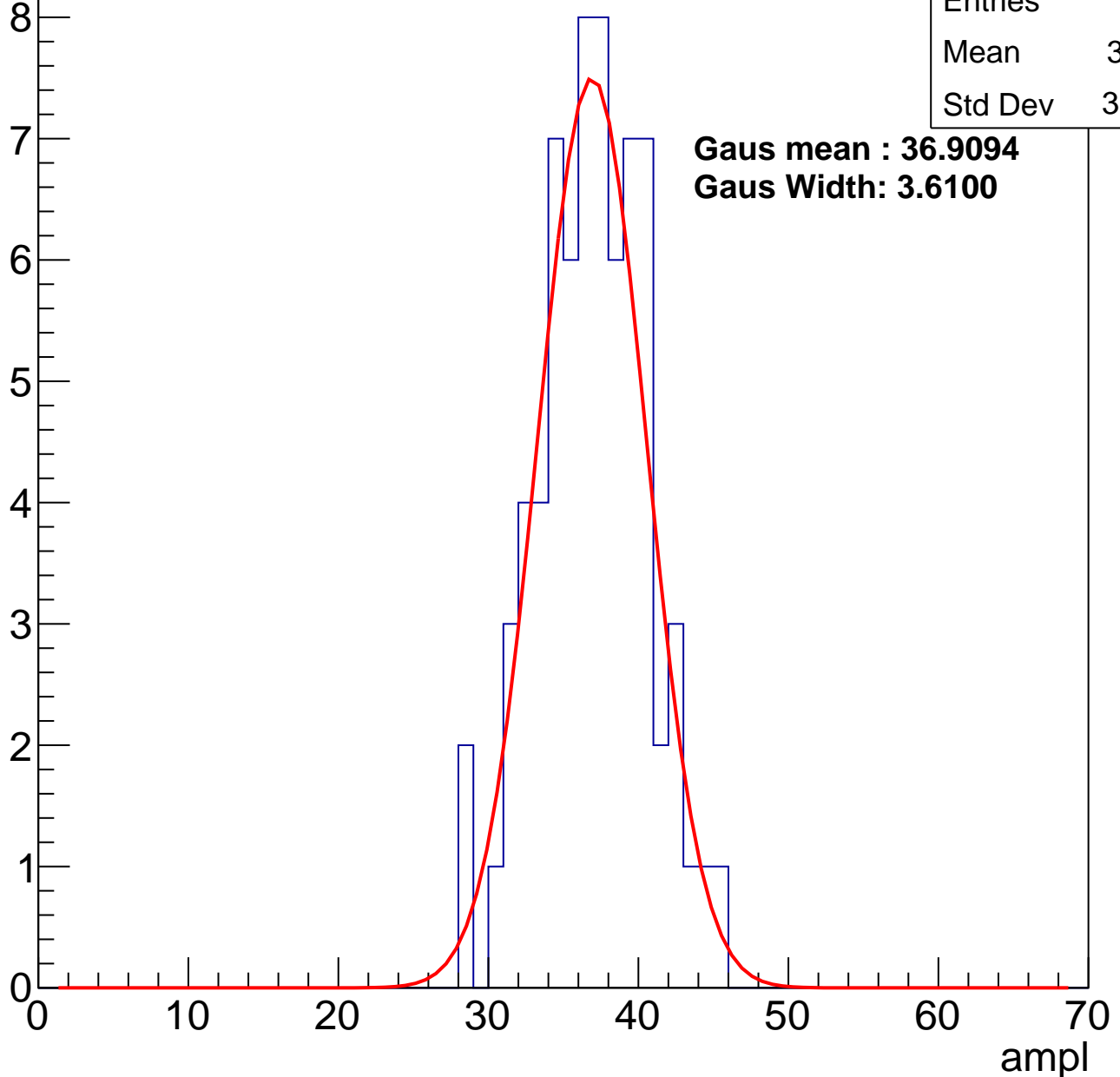
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	36.51
Std Dev	3.587

**Gaus mean : 36.9094**

**Gaus Width: 3.6100**



# B0L001S, U10-ch89, adc2

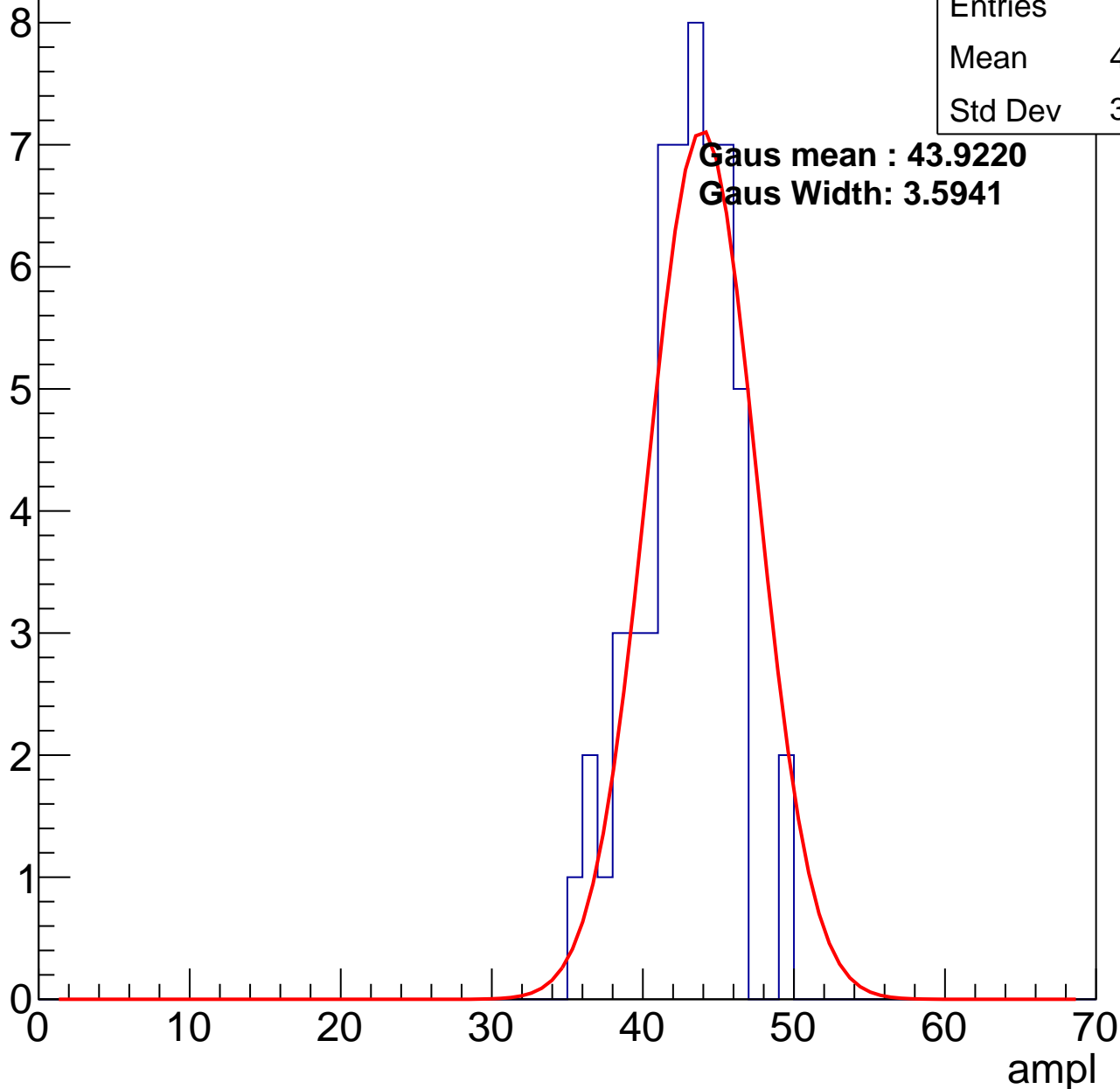
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	42.34
Std Dev	3.019

**Gaus mean : 43.9220**

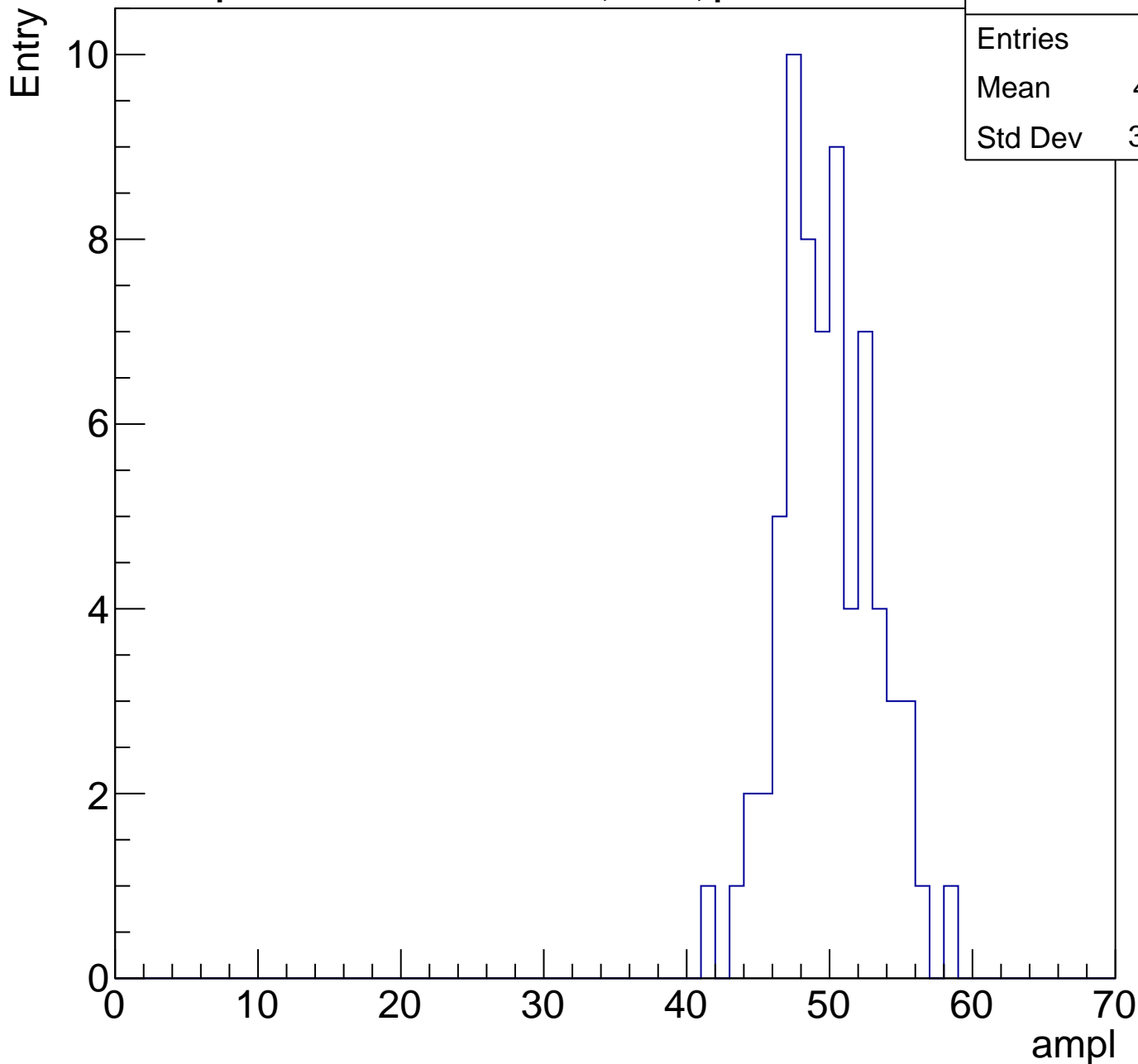
**Gaus Width: 3.5941**



# B0L001S, U10-ch89, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	68
Mean	49.41
Std Dev	3.273

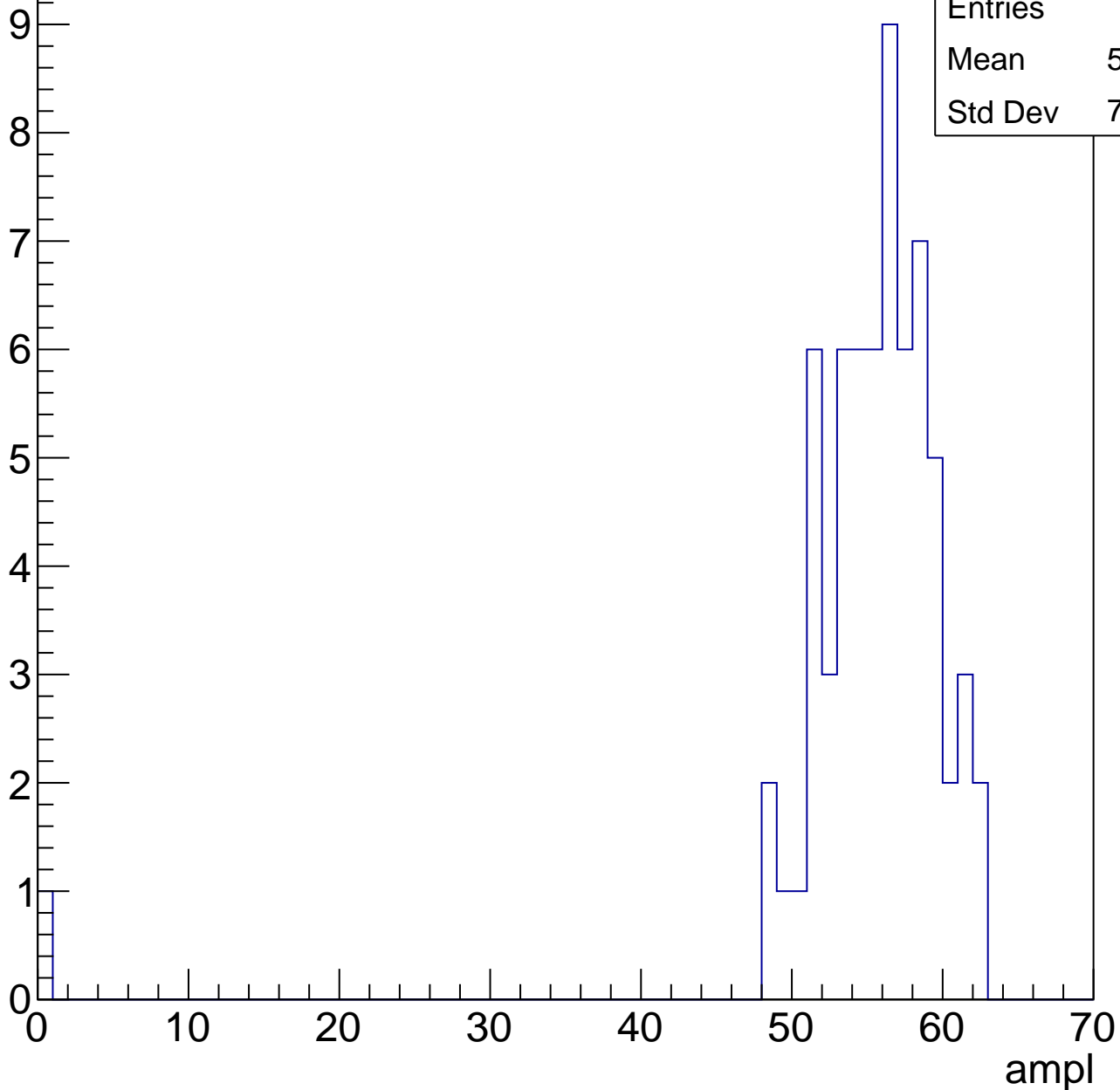


# B0L001S, U10-ch89, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	54.59
Std Dev	7.546

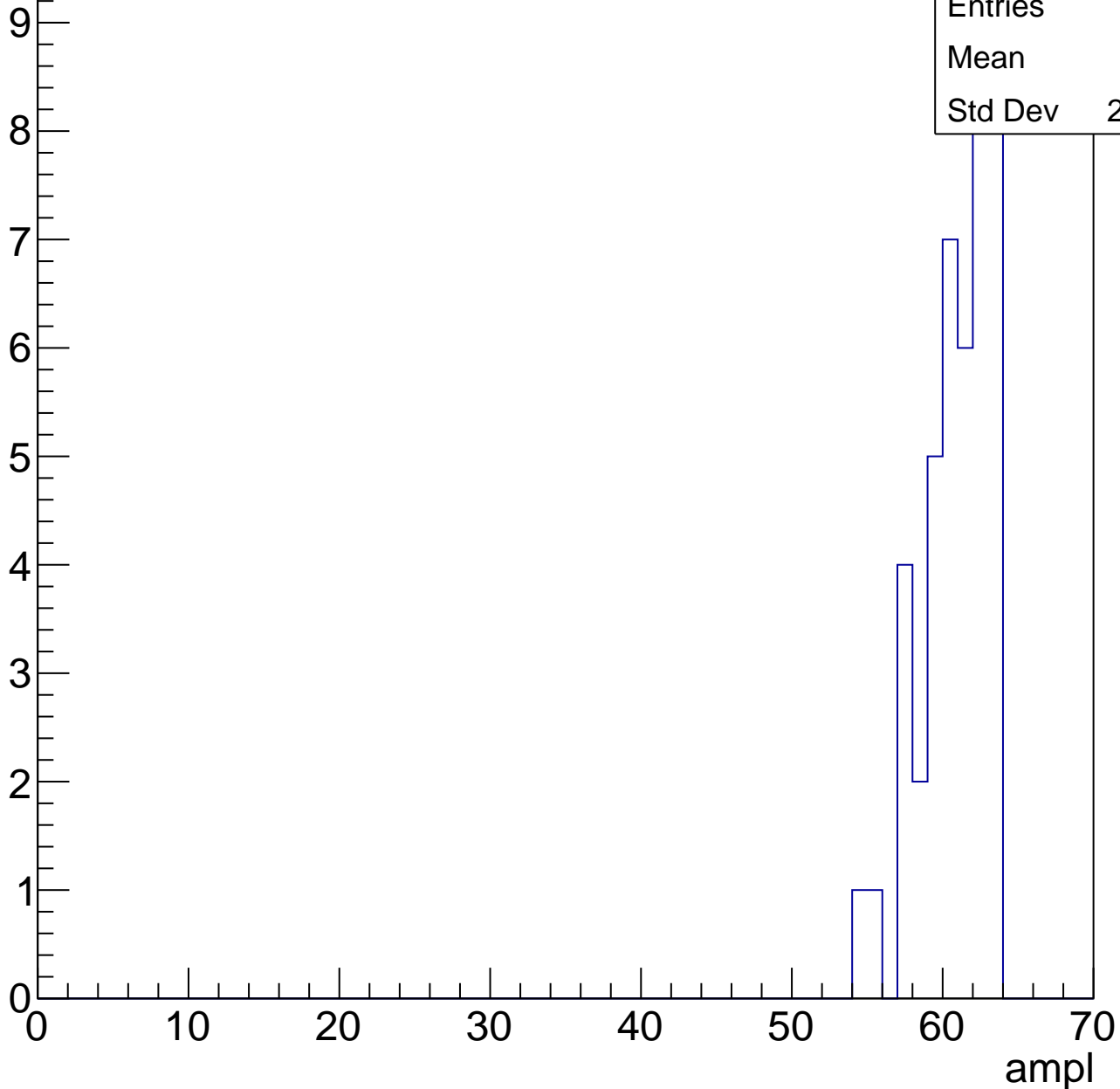


# B0L001S, U10-ch89, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	43
Mean	60.4
Std Dev	2.274



# B0L001S, U10-ch89, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch89, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U10-ch90, adc0

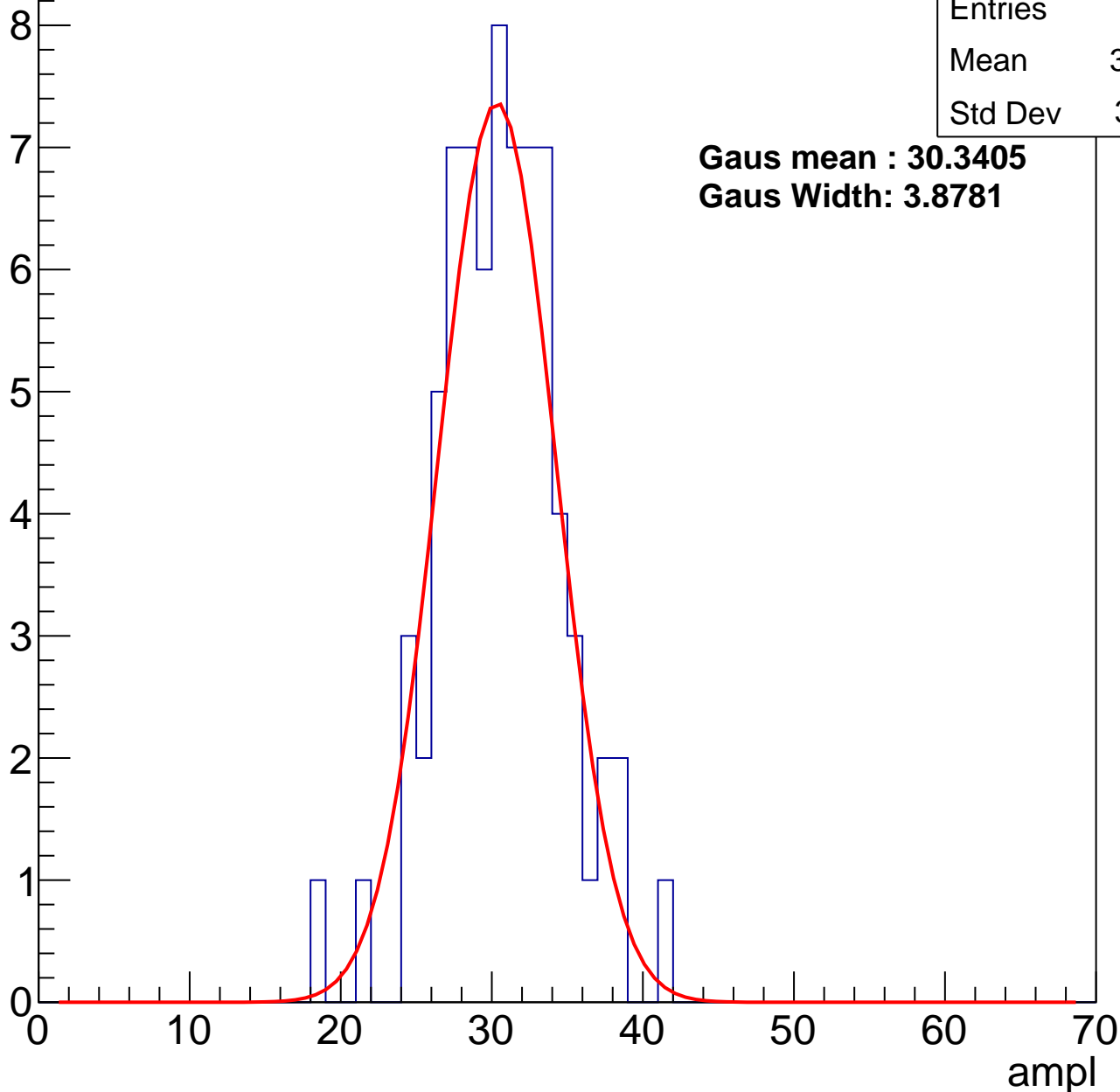
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	30.14
Std Dev	3.991

**Gaus mean : 30.3405**

**Gaus Width: 3.8781**



# B0L001S, U10-ch90, adc1

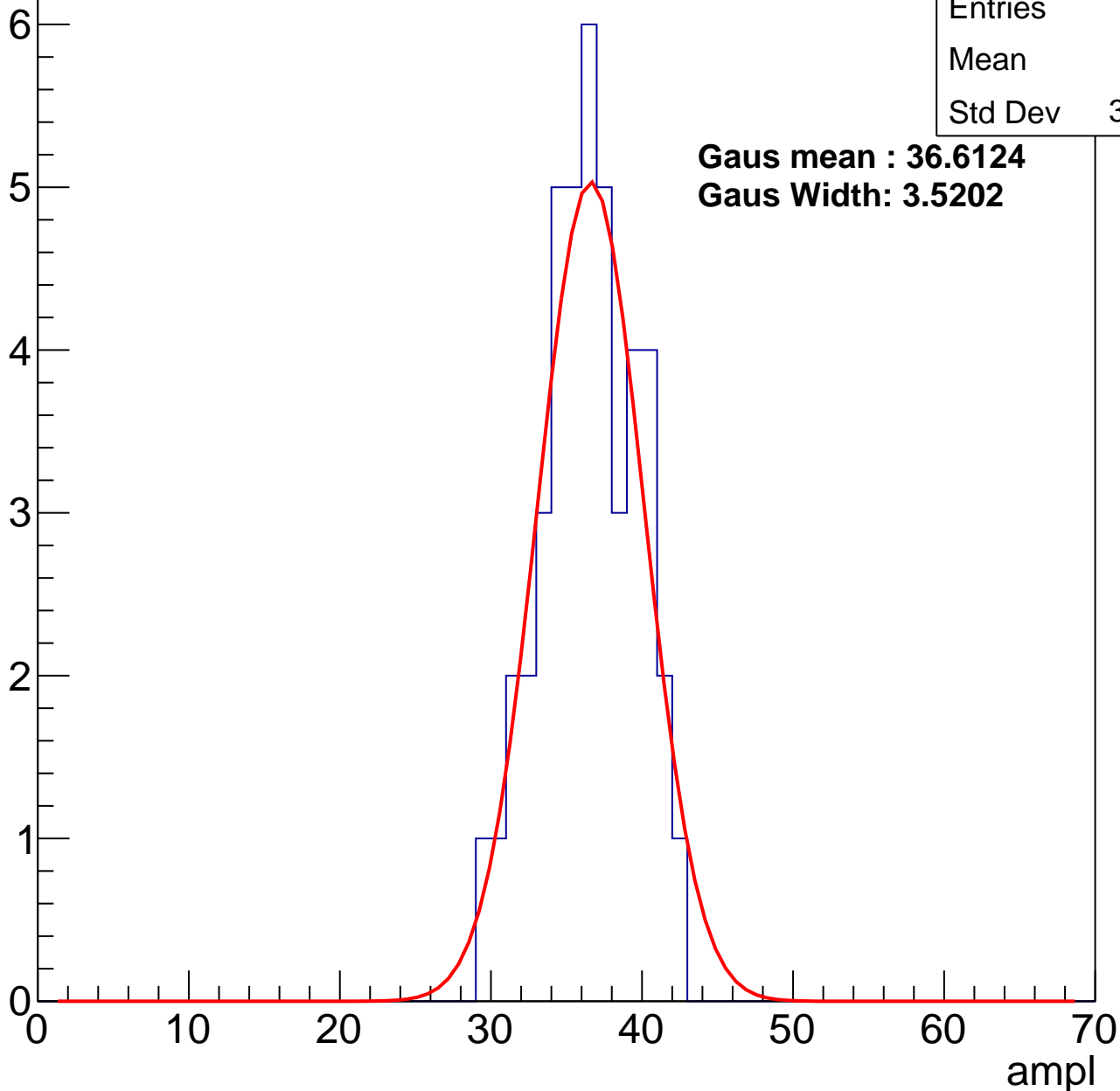
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	44
Mean	36
Std Dev	3.097

**Gaus mean : 36.6124**

**Gaus Width: 3.5202**



# B0L001S, U10-ch90, adc2

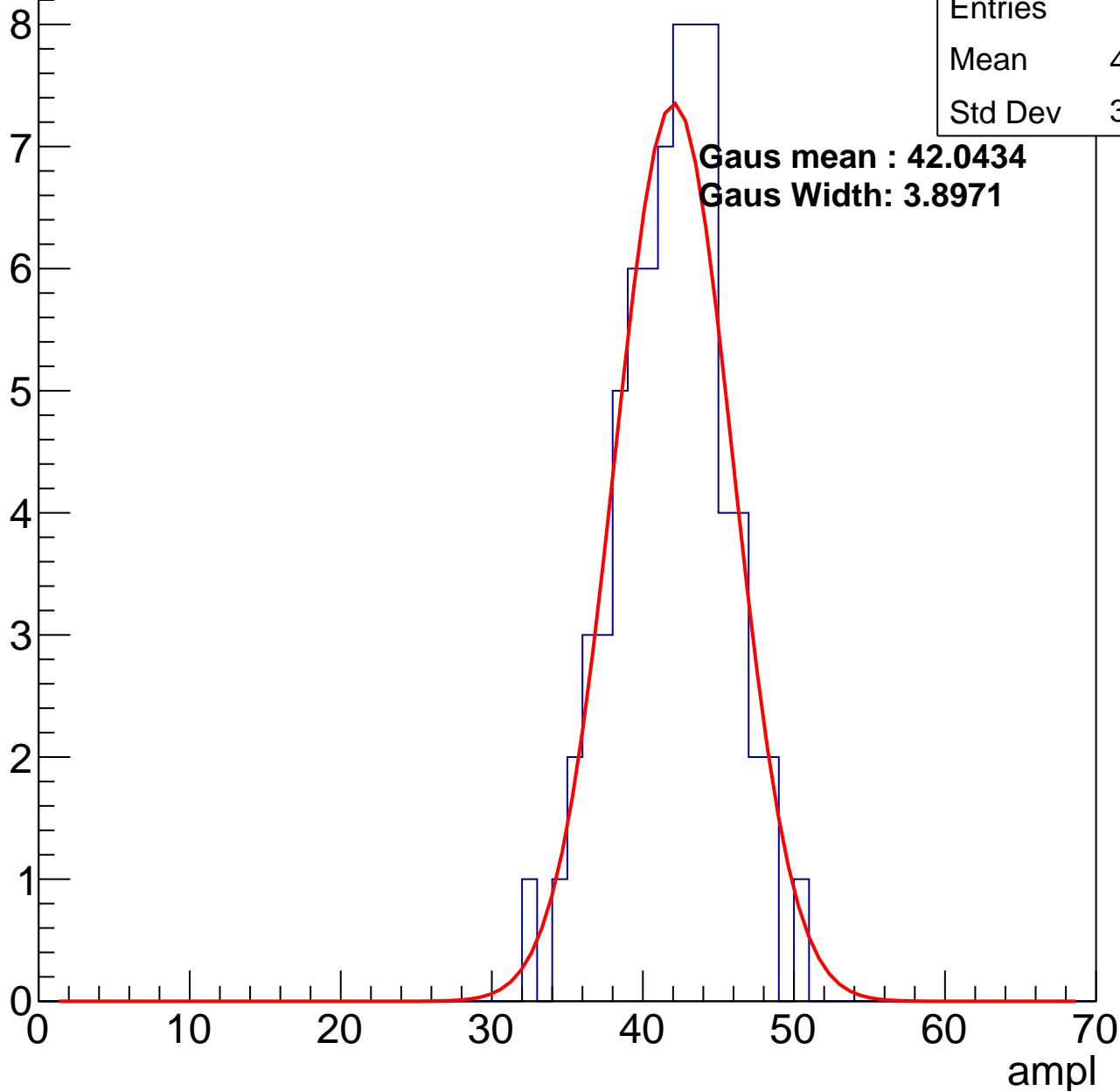
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	41.44
Std Dev	3.587

**Gaus mean : 42.0434**

**Gaus Width: 3.8971**

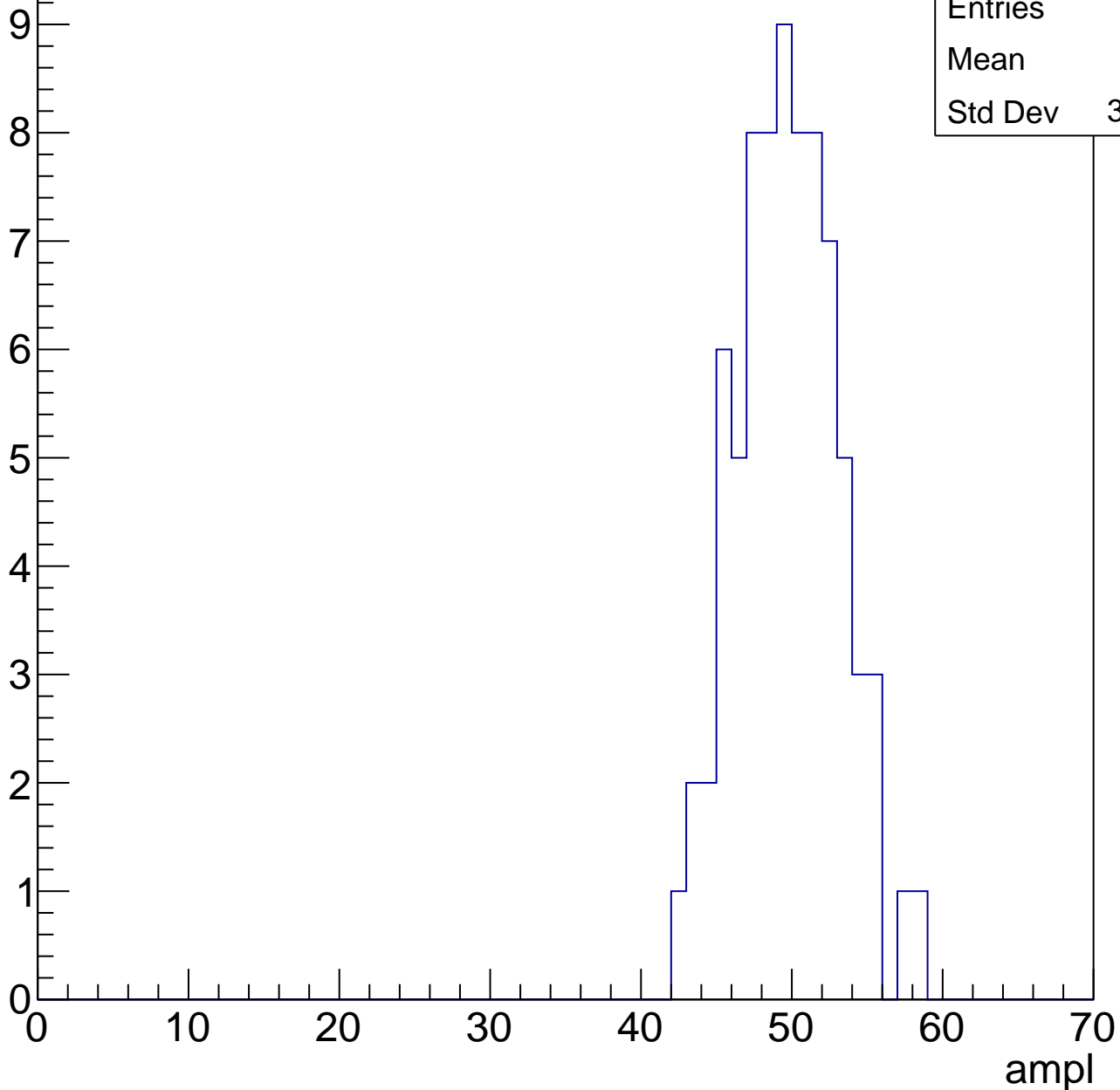


# B0L001S, U10-ch90, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	77
Mean	49.3
Std Dev	3.334

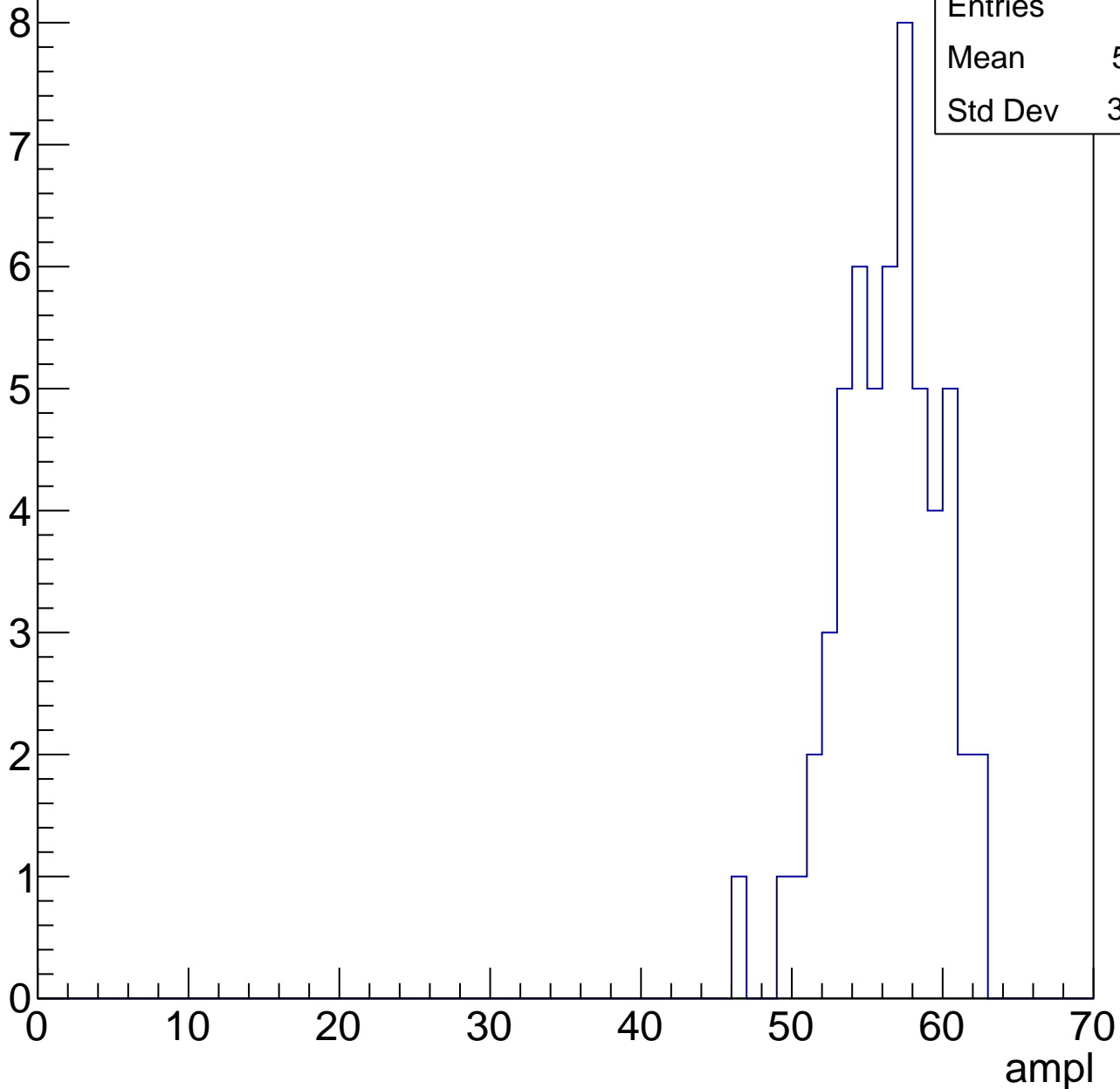


# B0L001S, U10-ch90, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	55.91
Std Dev	3.334

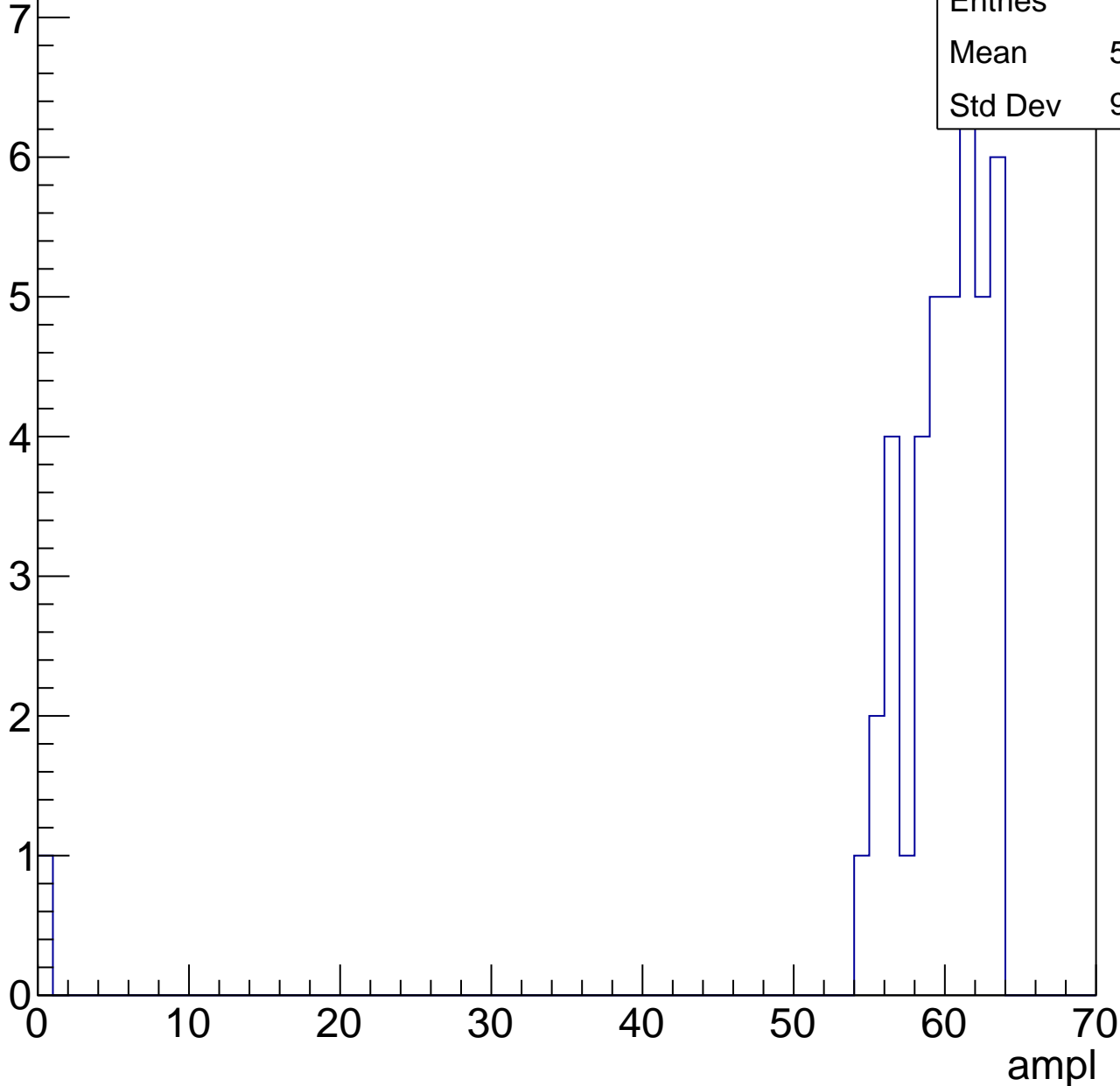


# B0L001S, U10-ch90, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

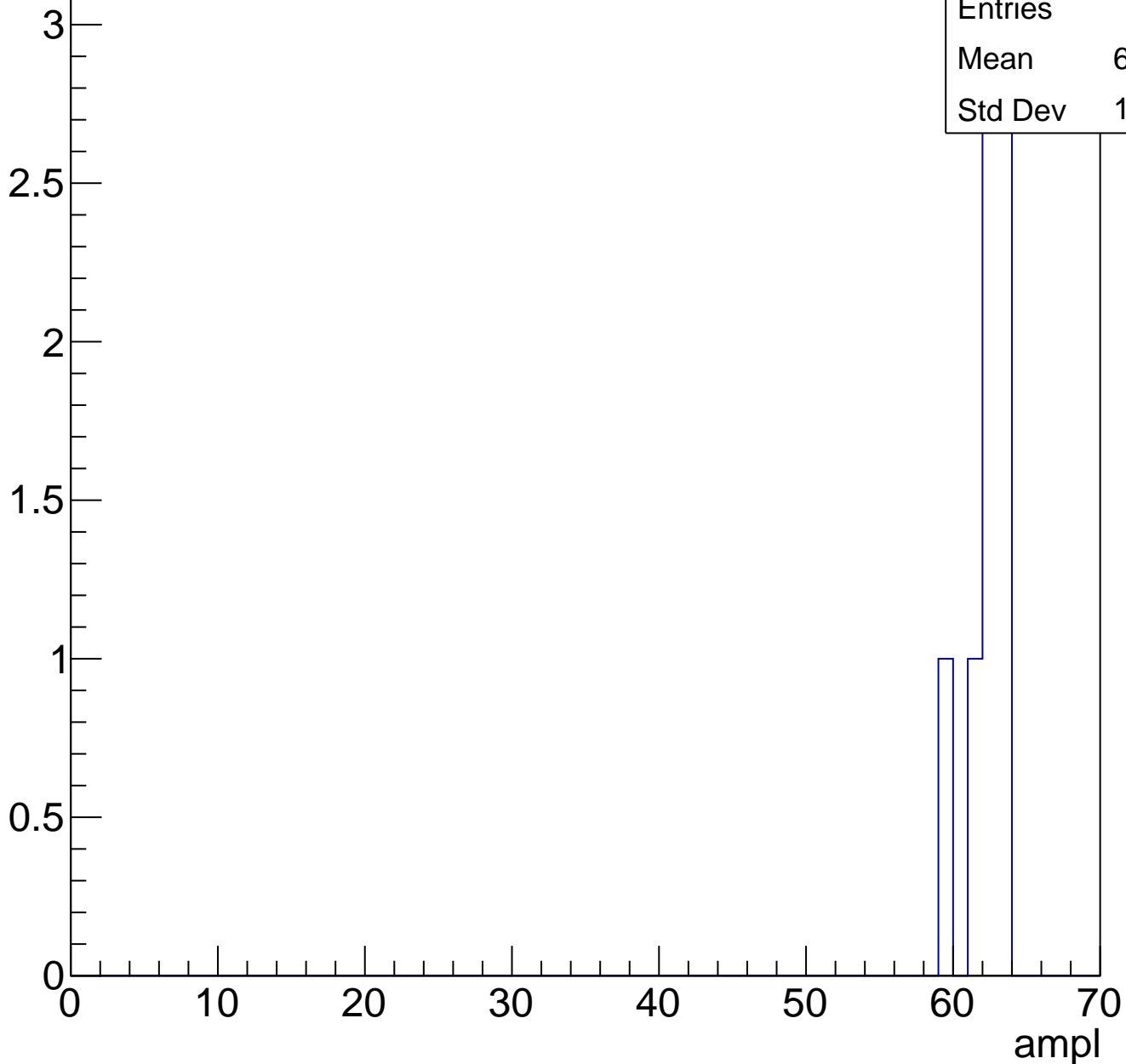
Entries	41
Mean	58.22
Std Dev	9.539



# B0L001S, U10-ch90, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch90, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U10-ch91, adc0

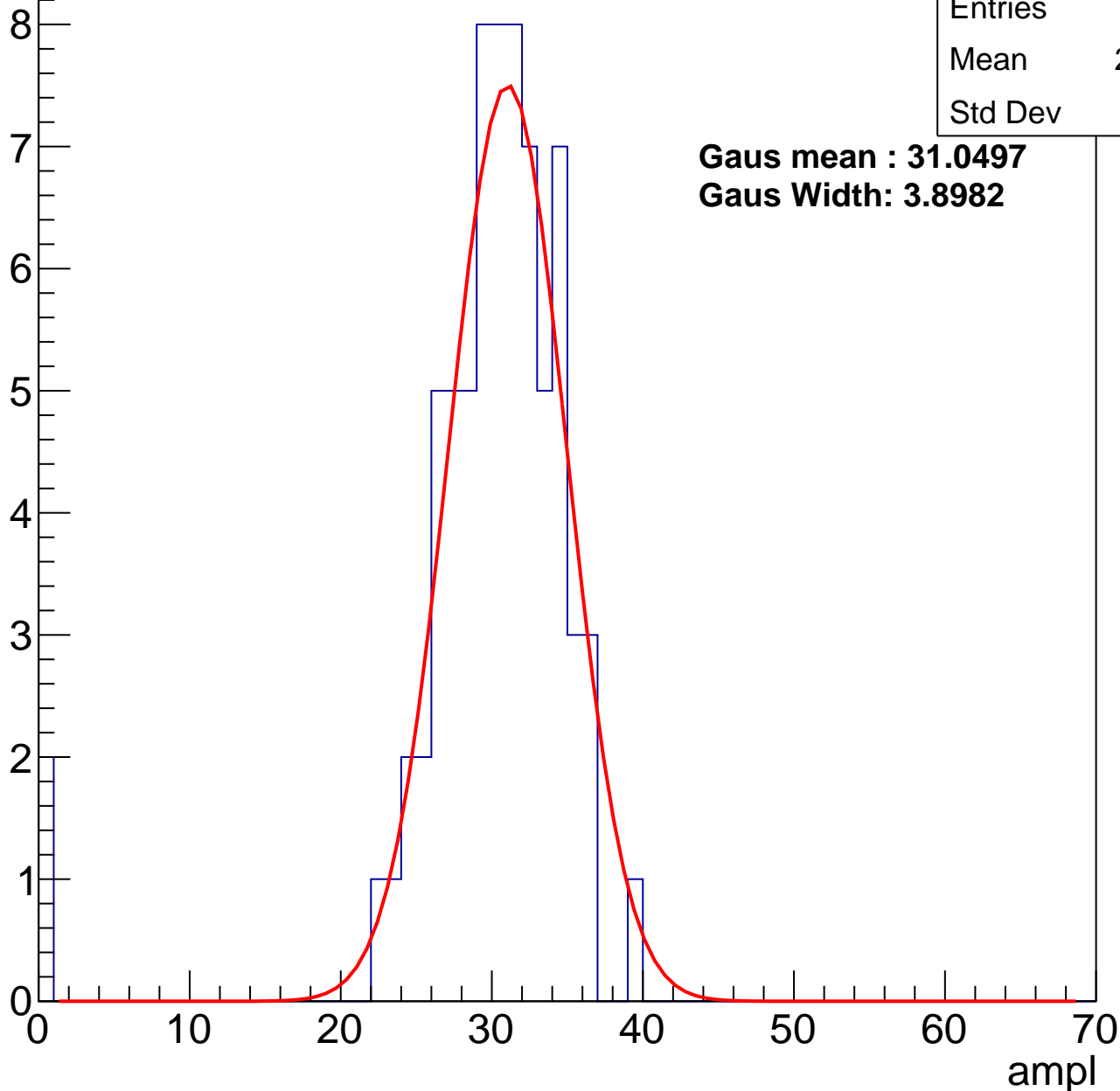
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	29.41
Std Dev	5.99

**Gaus mean : 31.0497**

**Gaus Width: 3.8982**



# B0L001S, U10-ch91, adc1

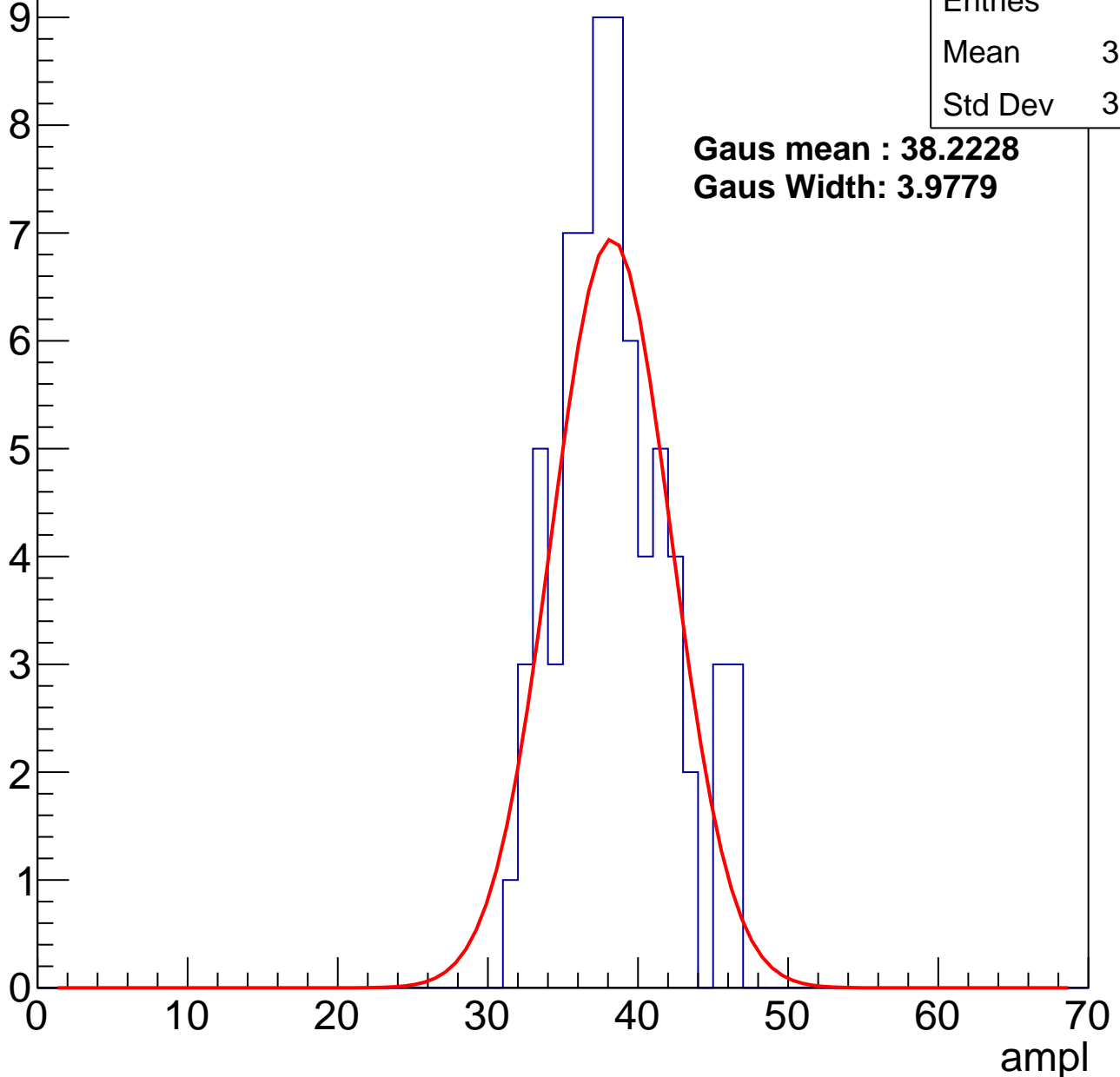
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	37.92
Std Dev	3.657

**Gaus mean : 38.2228**

**Gaus Width: 3.9779**



# B0L001S, U10-ch91, adc2

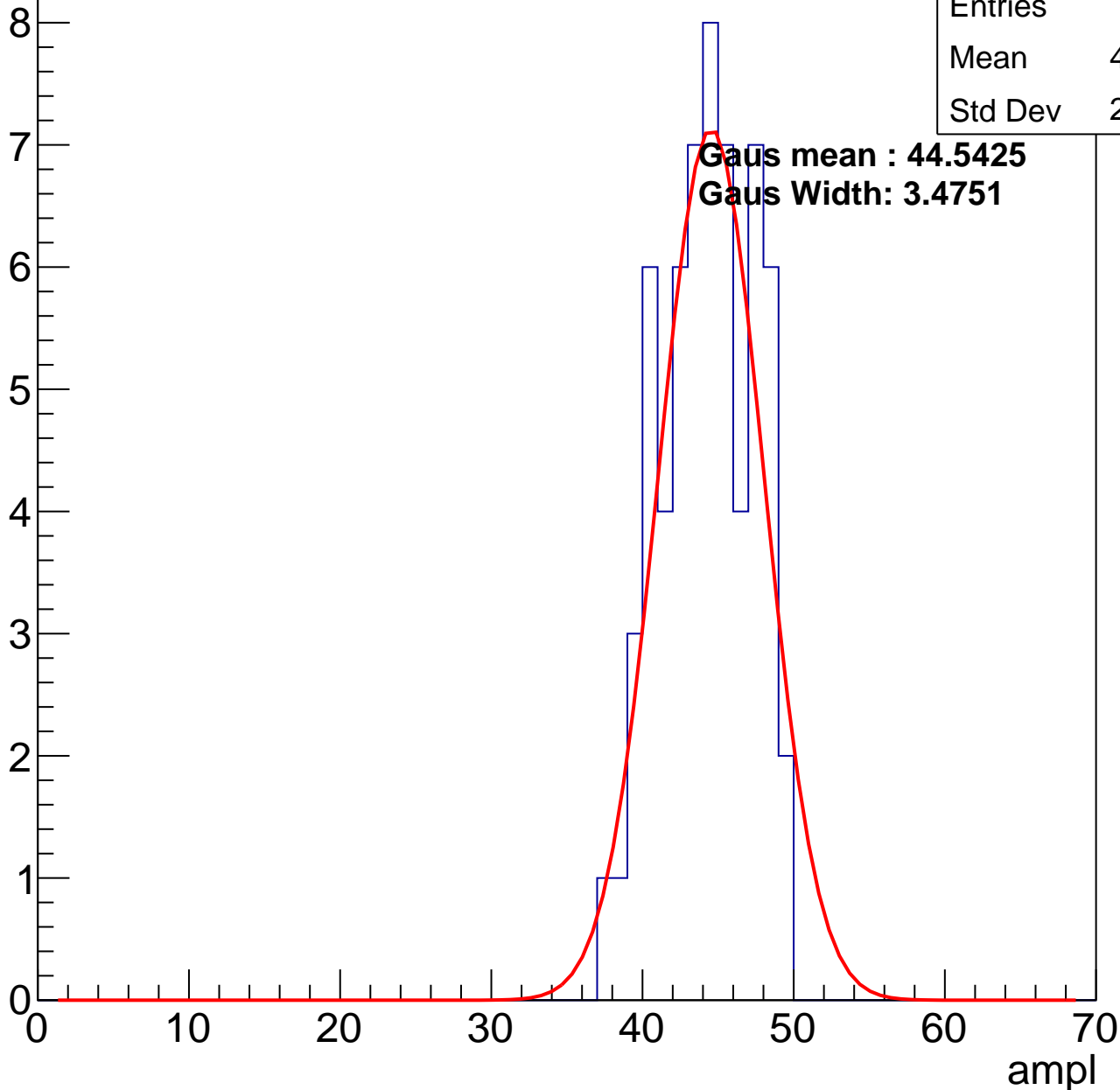
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	43.79
Std Dev	2.985

**Gaus mean : 44.5425**

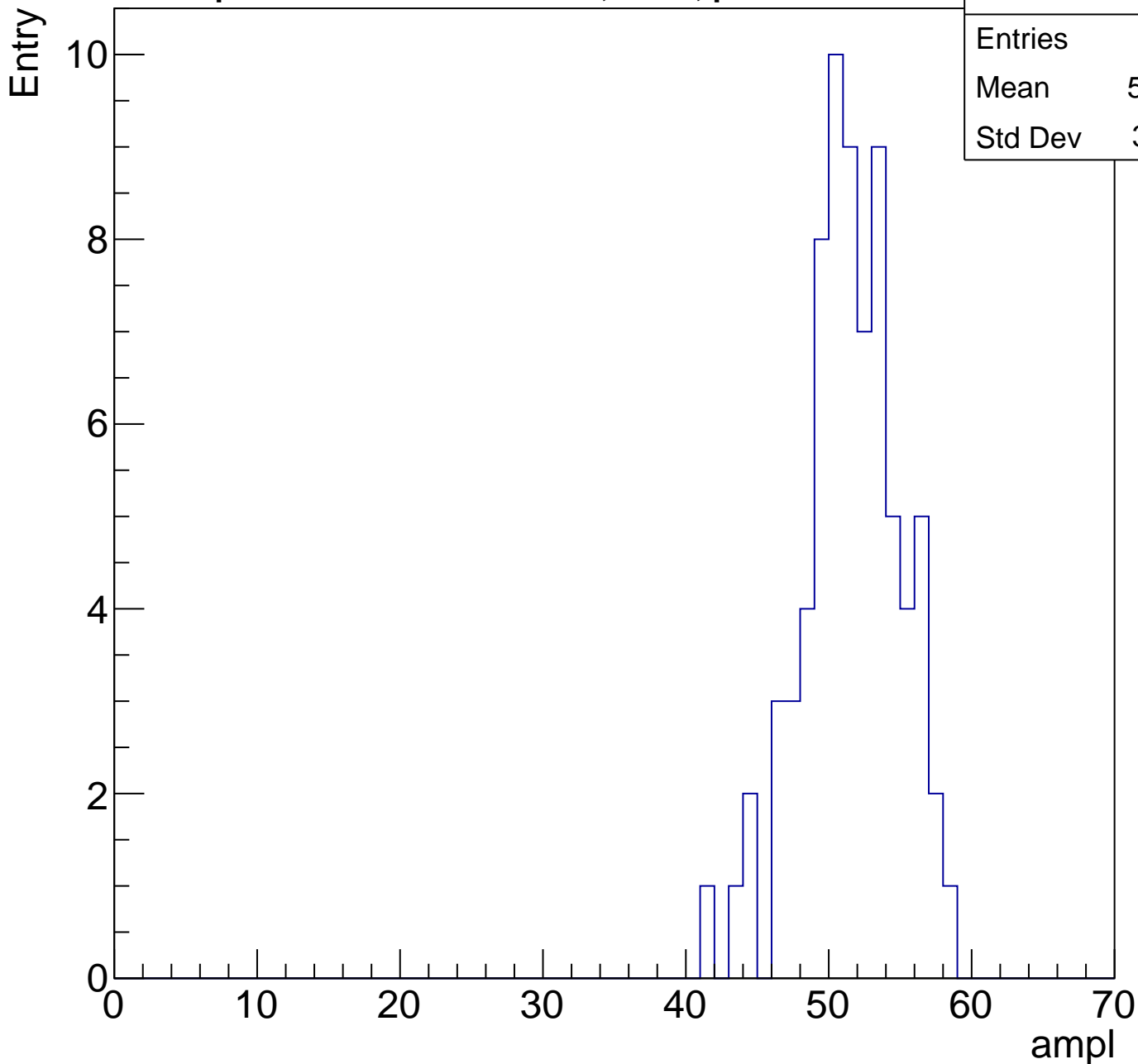
**Gaus Width: 3.4751**



# B0L001S, U10-ch91, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	74
Mean	51.04
Std Dev	3.411

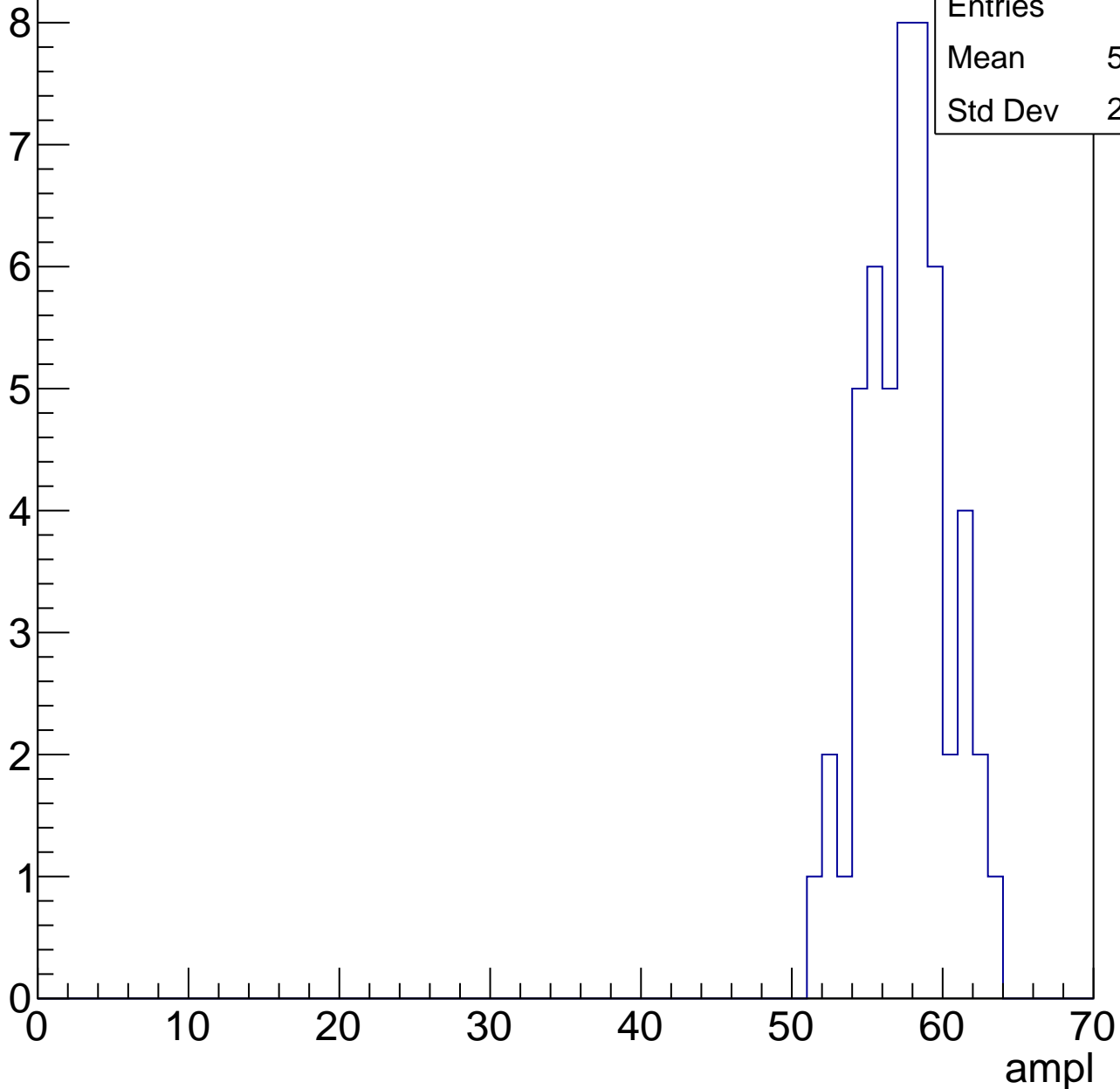


# B0L001S, U10-ch91, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	51
Mean	57.12
Std Dev	2.713

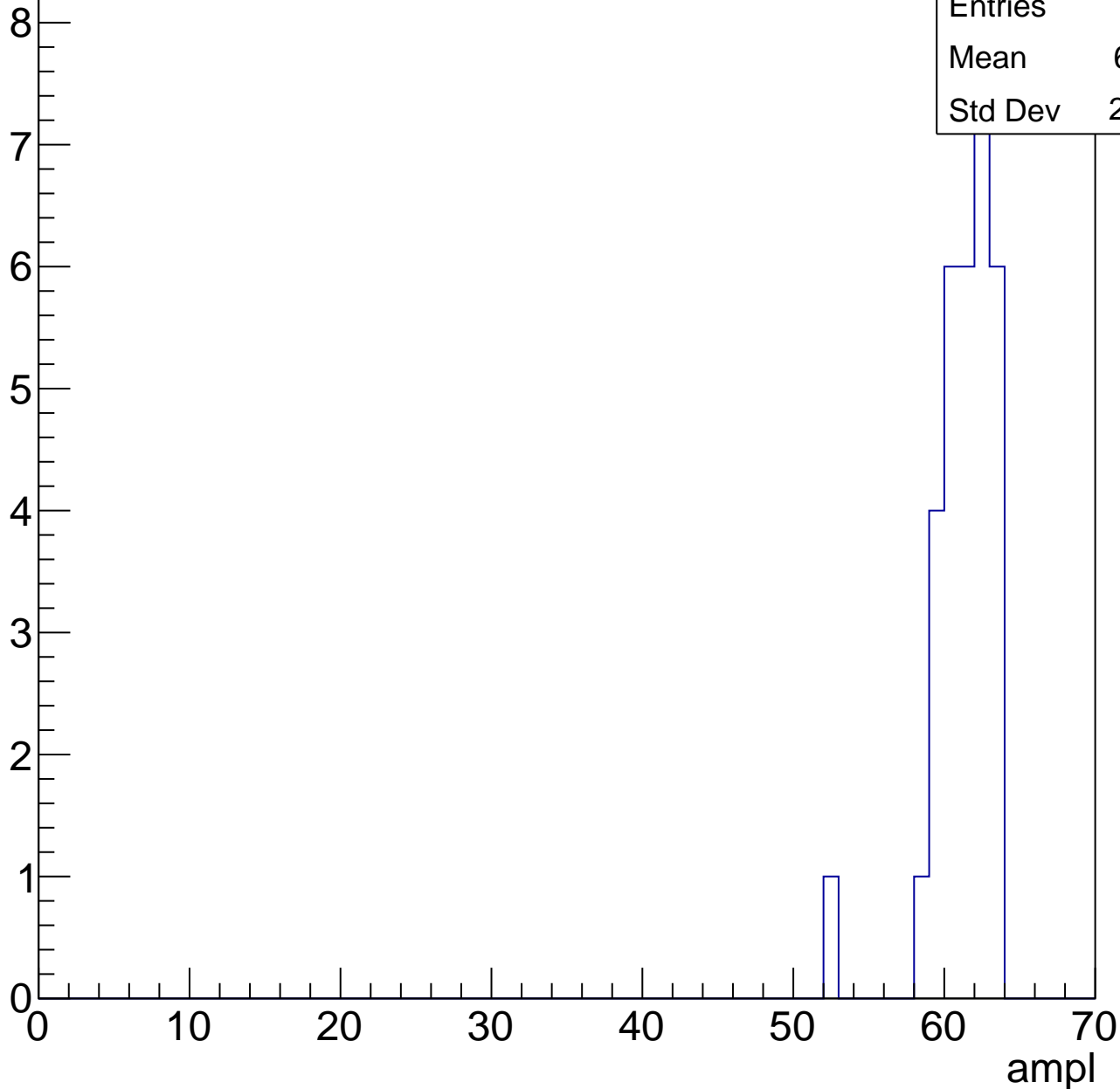


# B0L001S, U10-ch91, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

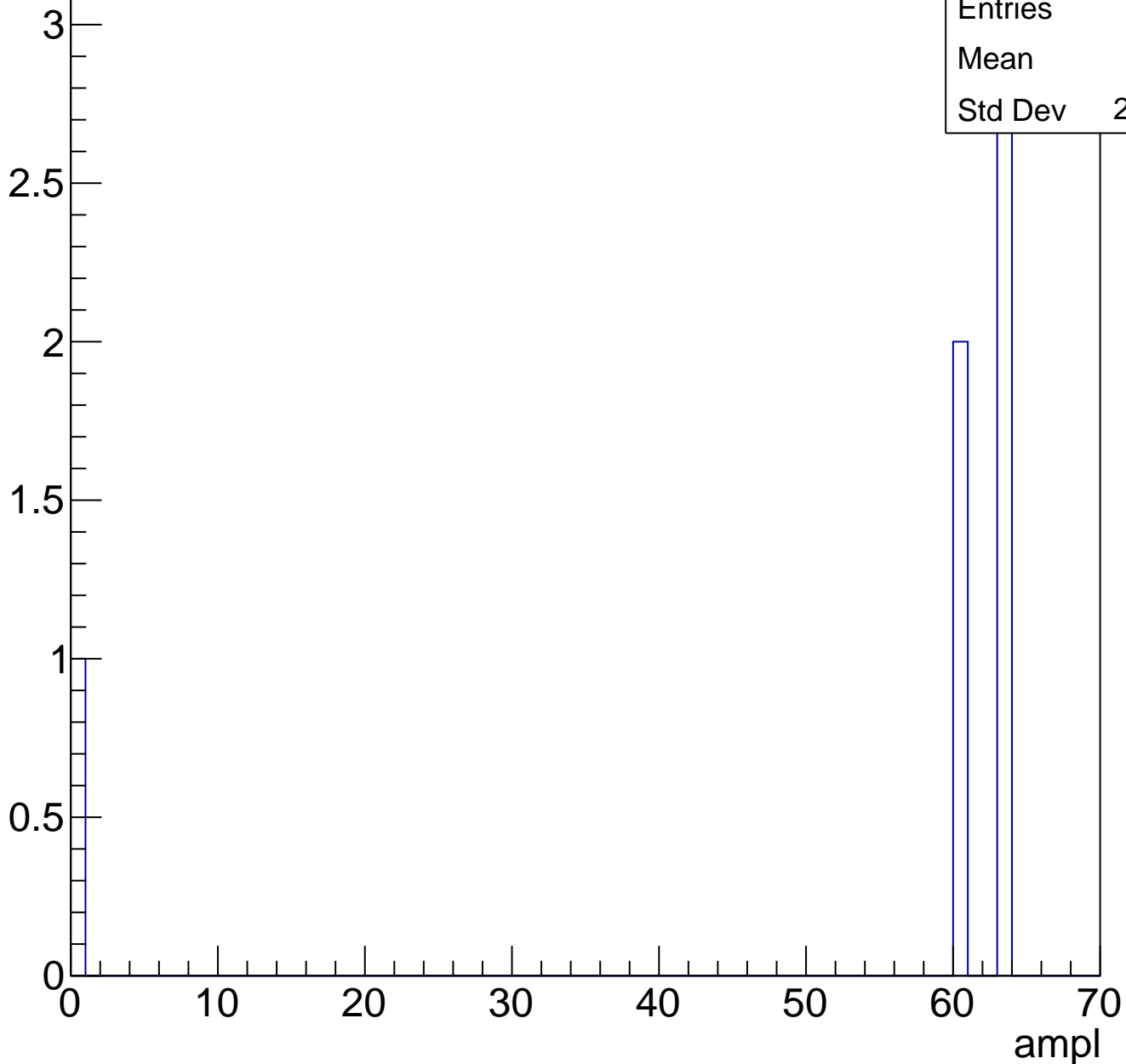
Entries	32
Mean	60.81
Std Dev	2.113



# B0L001S, U10-ch91, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch91, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U10-ch92, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	90
Mean	29.36
Std Dev	5.052

**Gaus mean : 30.1469**

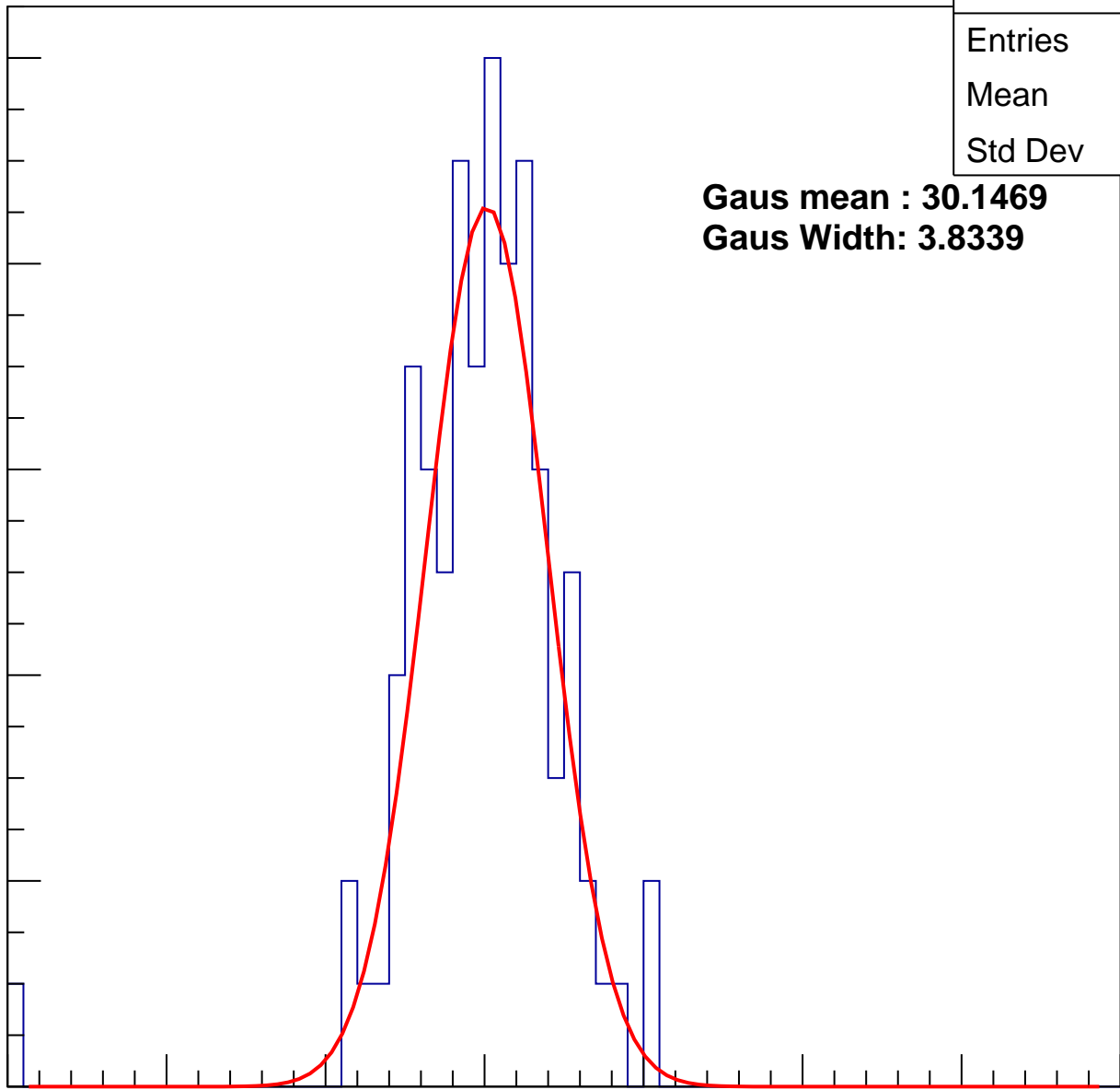
**Gaus Width: 3.8339**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U10-ch92, adc1

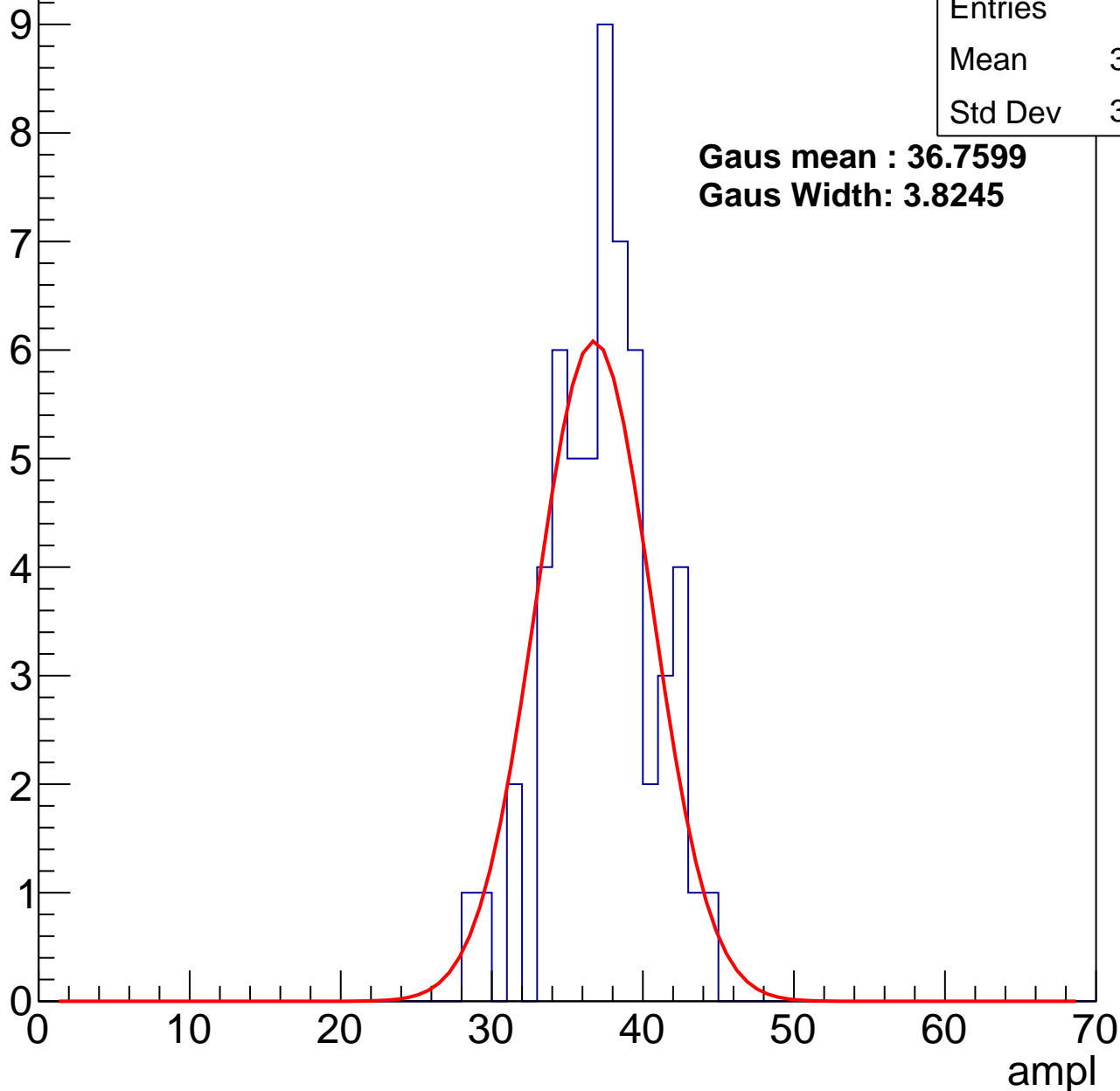
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	36.86
Std Dev	3.353

**Gaus mean : 36.7599**

**Gaus Width: 3.8245**



# B0L001S, U10-ch92, adc2

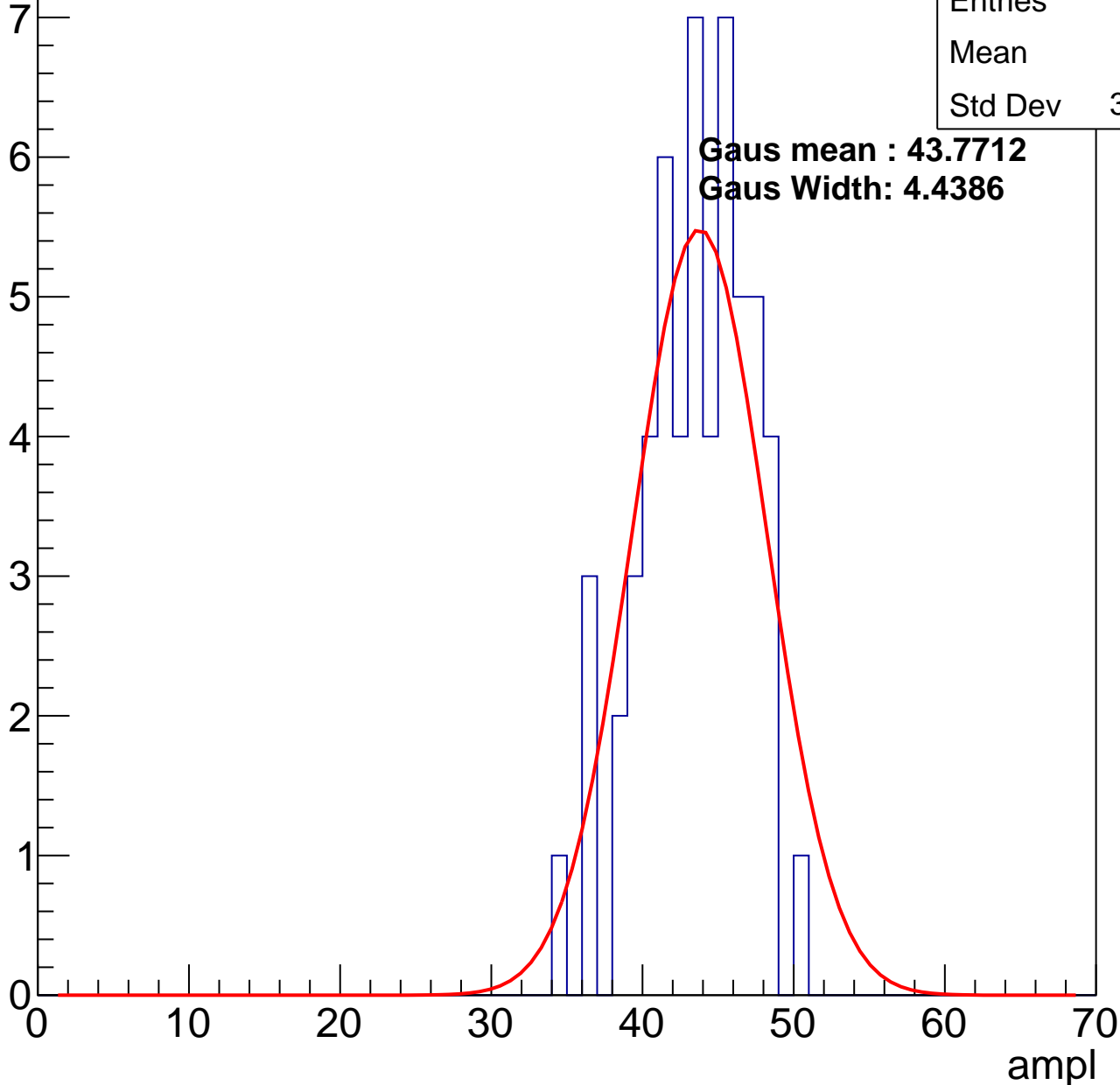
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	43
Std Dev	3.525

**Gaus mean : 43.7712**

**Gaus Width: 4.4386**

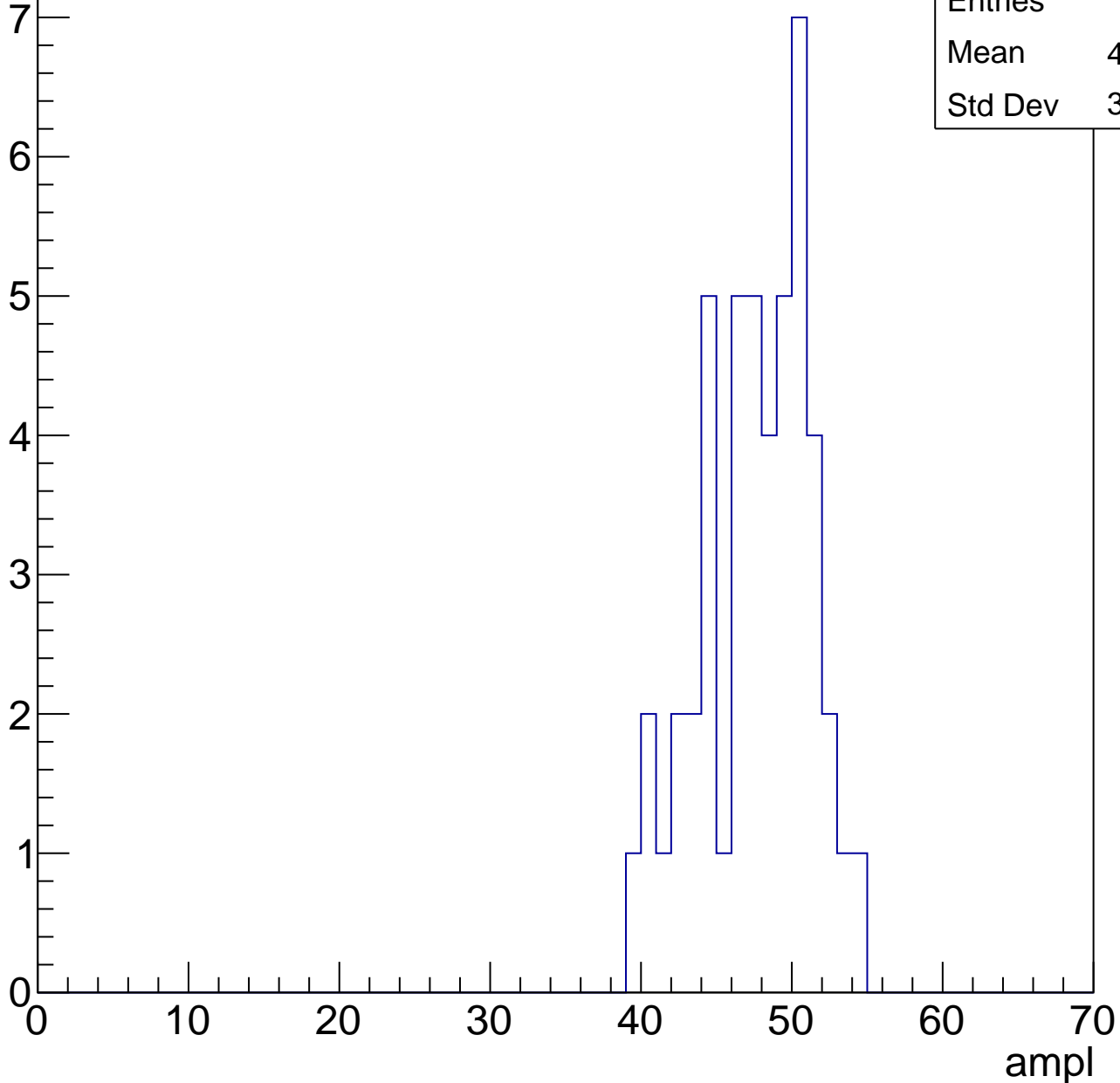


# B0L001S, U10-ch92, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

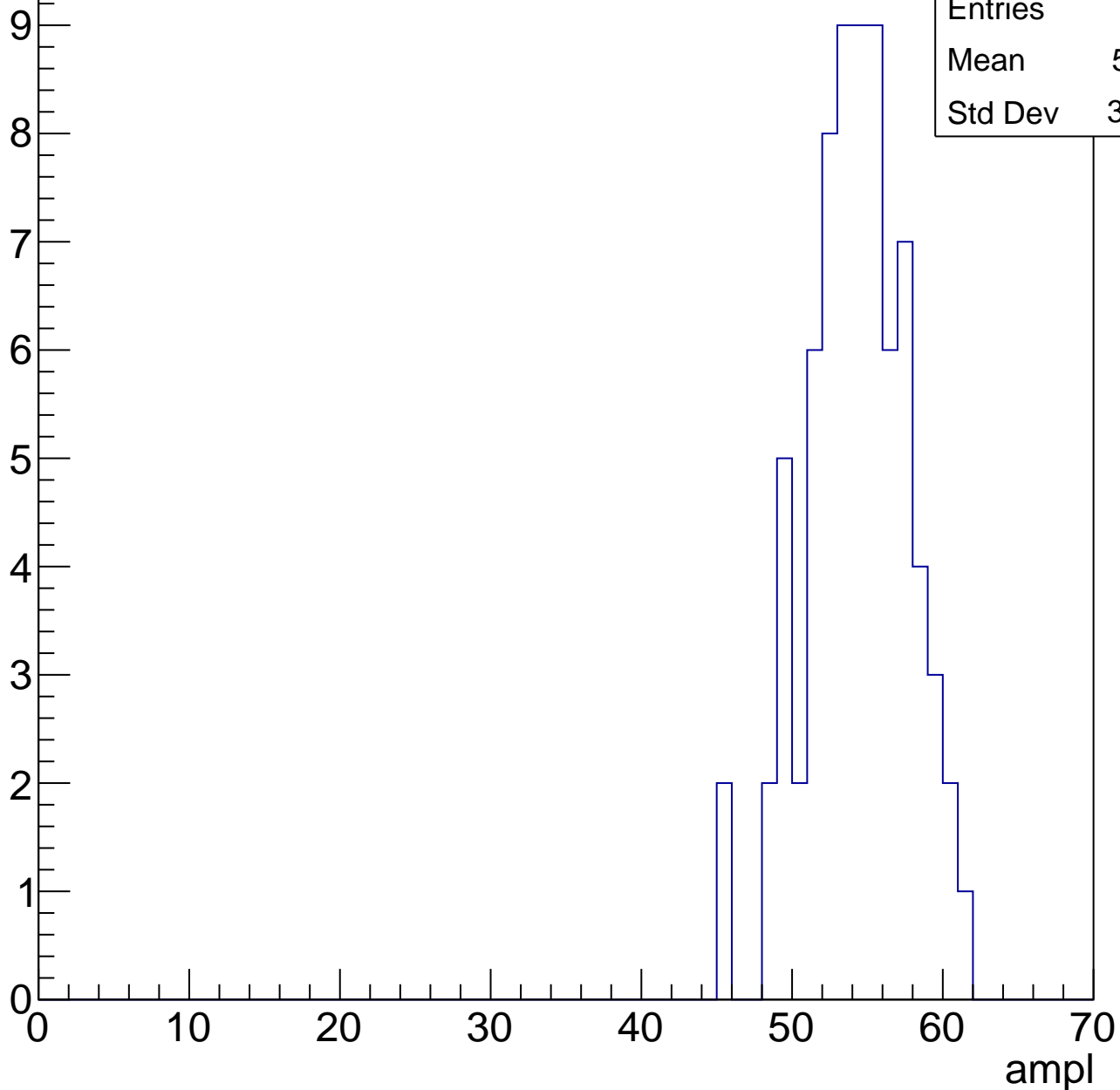
Entries	48
Mean	47.12
Std Dev	3.592



# B0L001S, U10-ch92, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



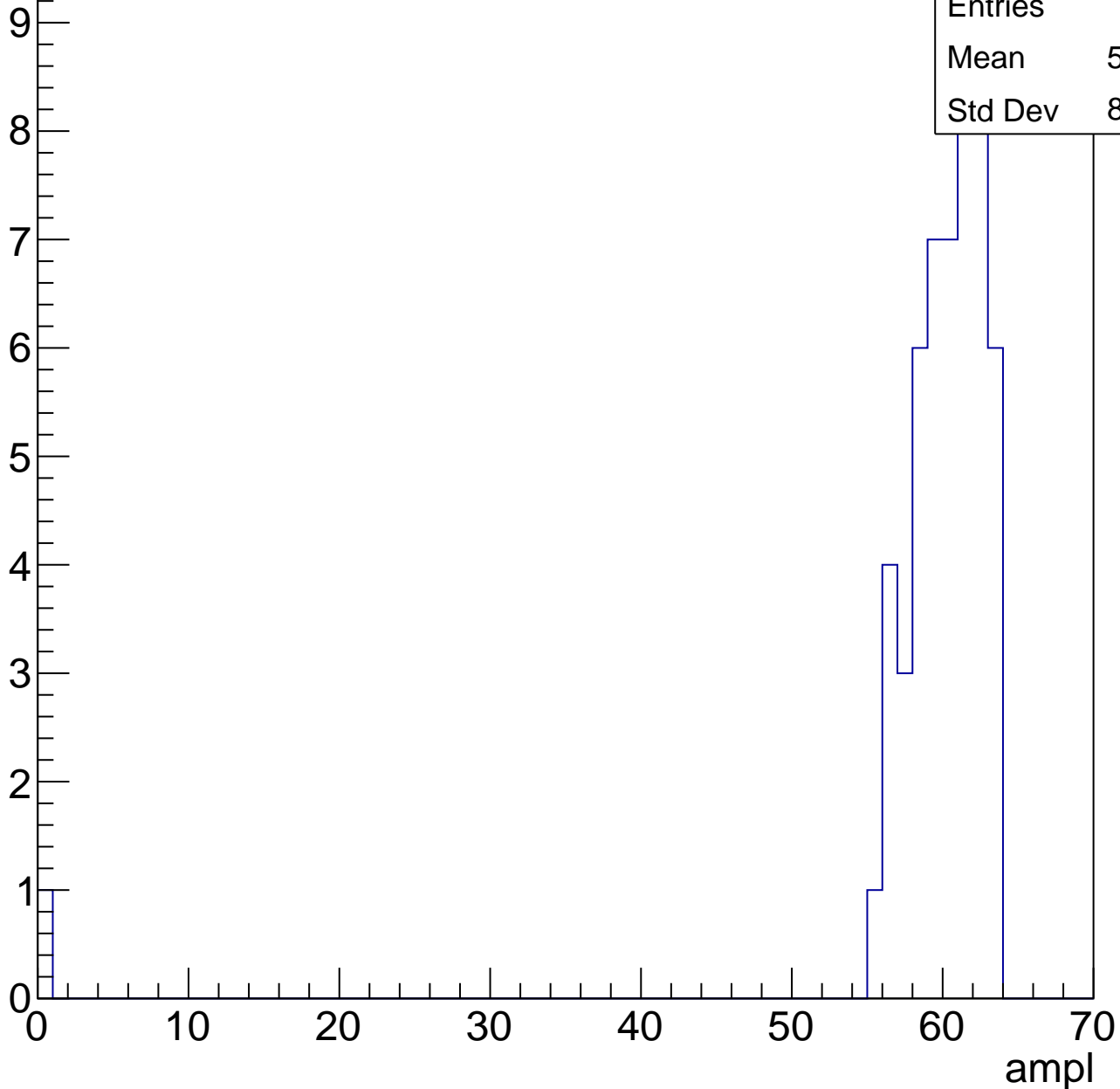
Entries	75
Mean	53.81
Std Dev	3.345

# B0L001S, U10-ch92, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	58.75
Std Dev	8.508



# B0L001S, U10-ch92, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch92, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L001S, U10-ch93, adc0

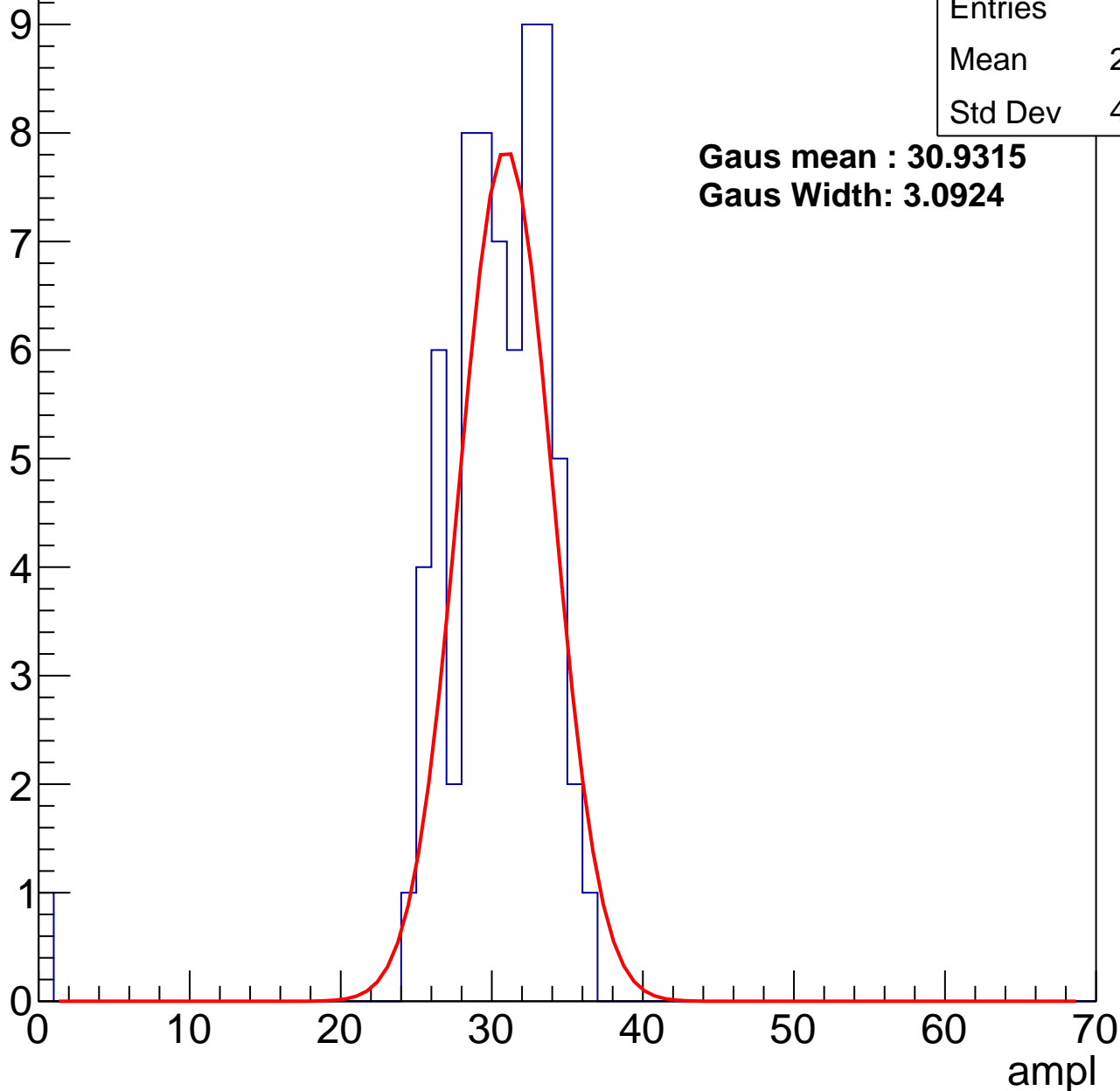
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	29.67
Std Dev	4.618

**Gaus mean : 30.9315**

**Gaus Width: 3.0924**



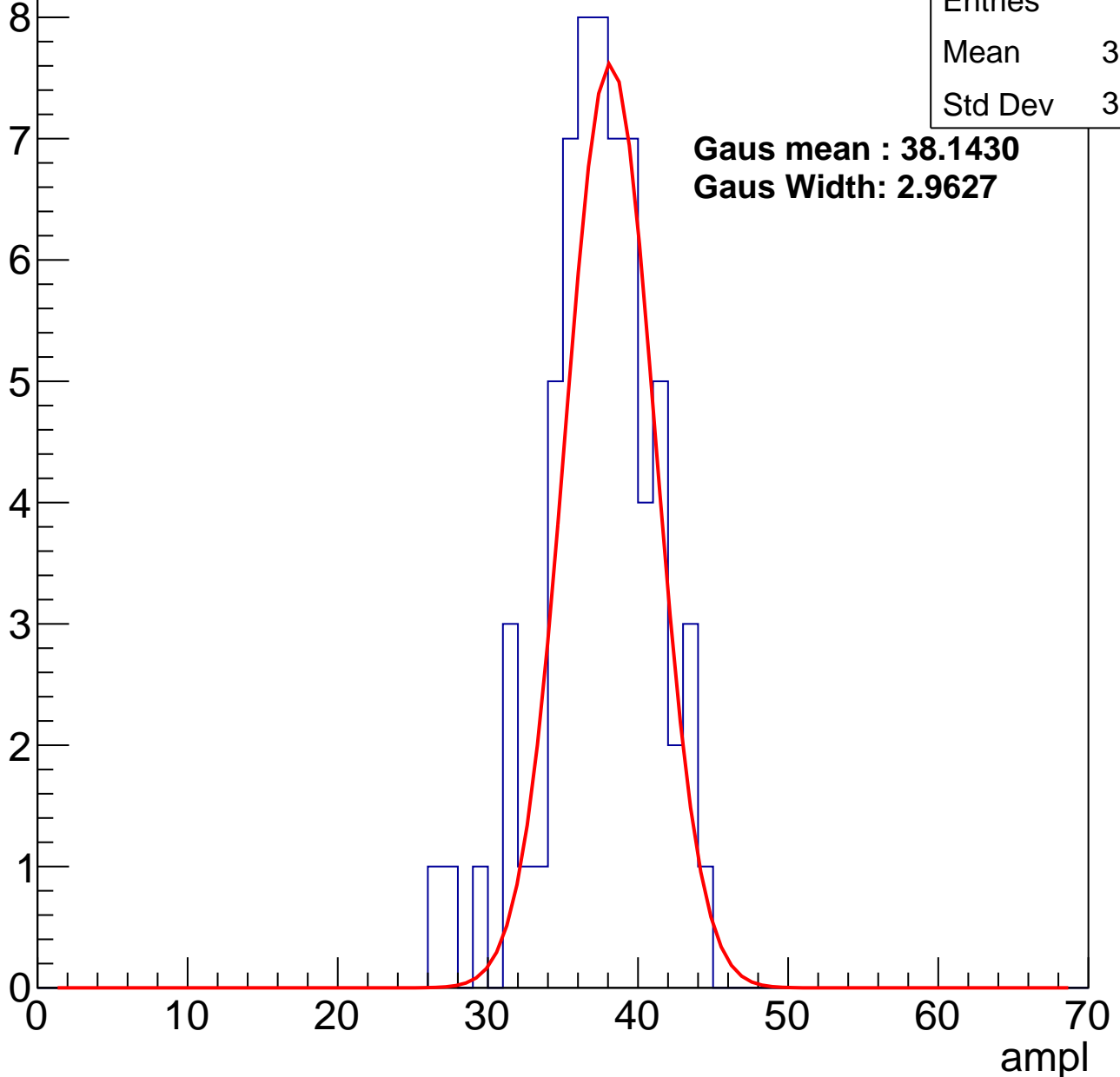
# B0L001S, U10-ch93, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	36.92
Std Dev	3.664

**Gaus mean : 38.1430**  
**Gaus Width: 2.9627**



# B0L001S, U10-ch93, adc2

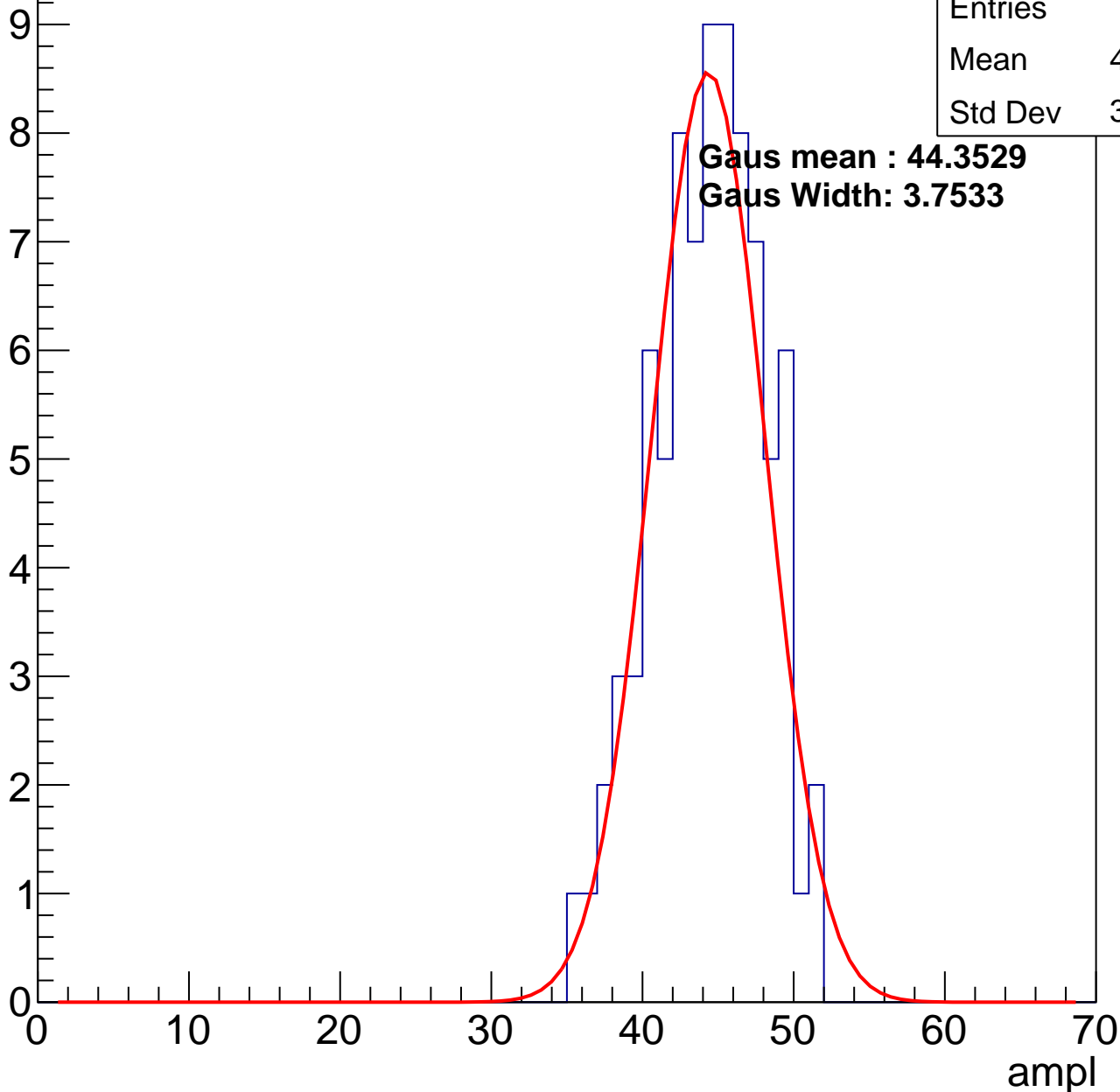
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	83
Mean	43.88
Std Dev	3.595

**Gaus mean : 44.3529**

**Gaus Width: 3.7533**

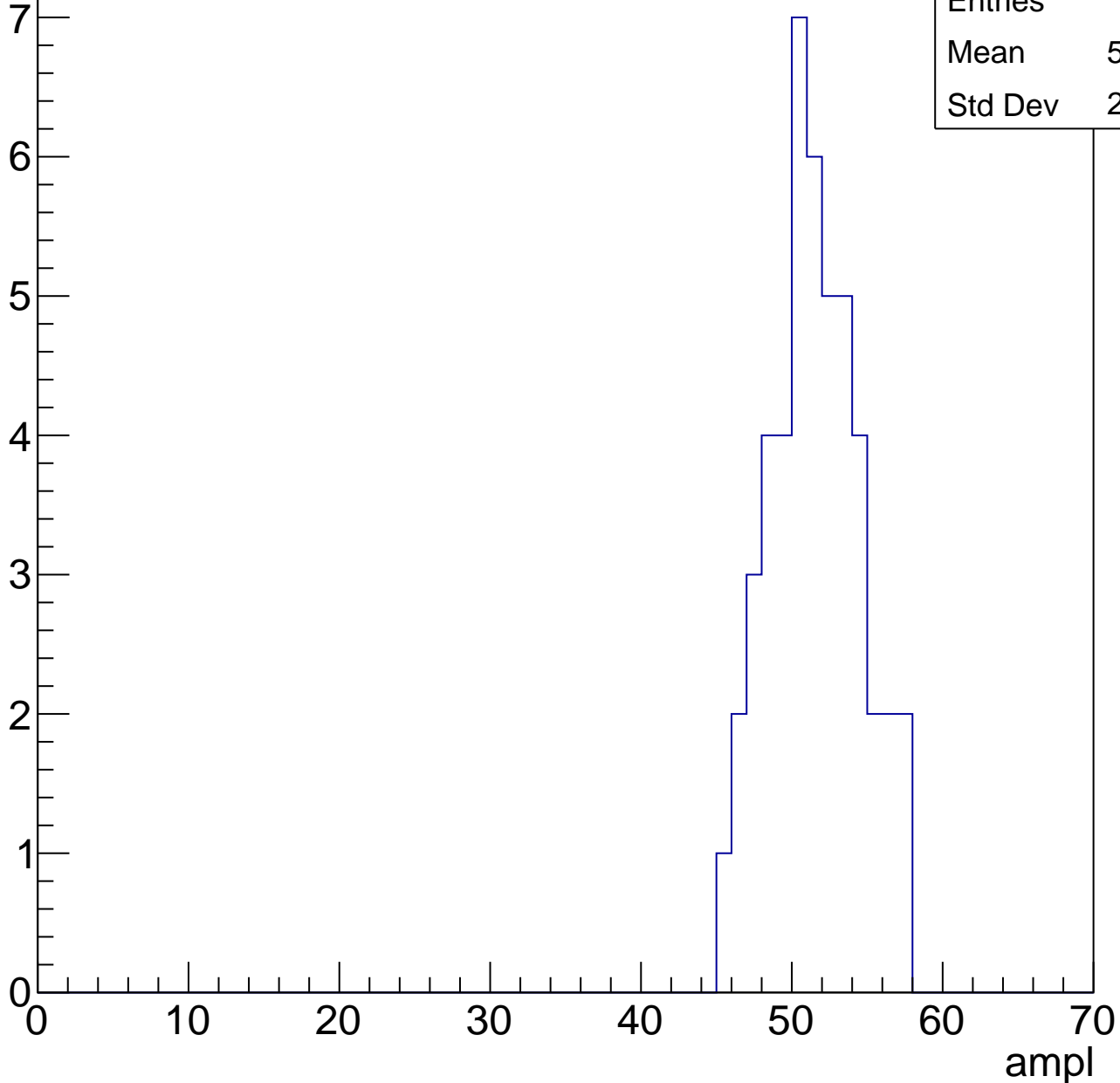


# B0L001S, U10-ch93, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	47
Mean	51.04
Std Dev	2.946



# B0L001S, U10-ch93, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

6

5

4

3

2

1

0

0

10

20

30

40

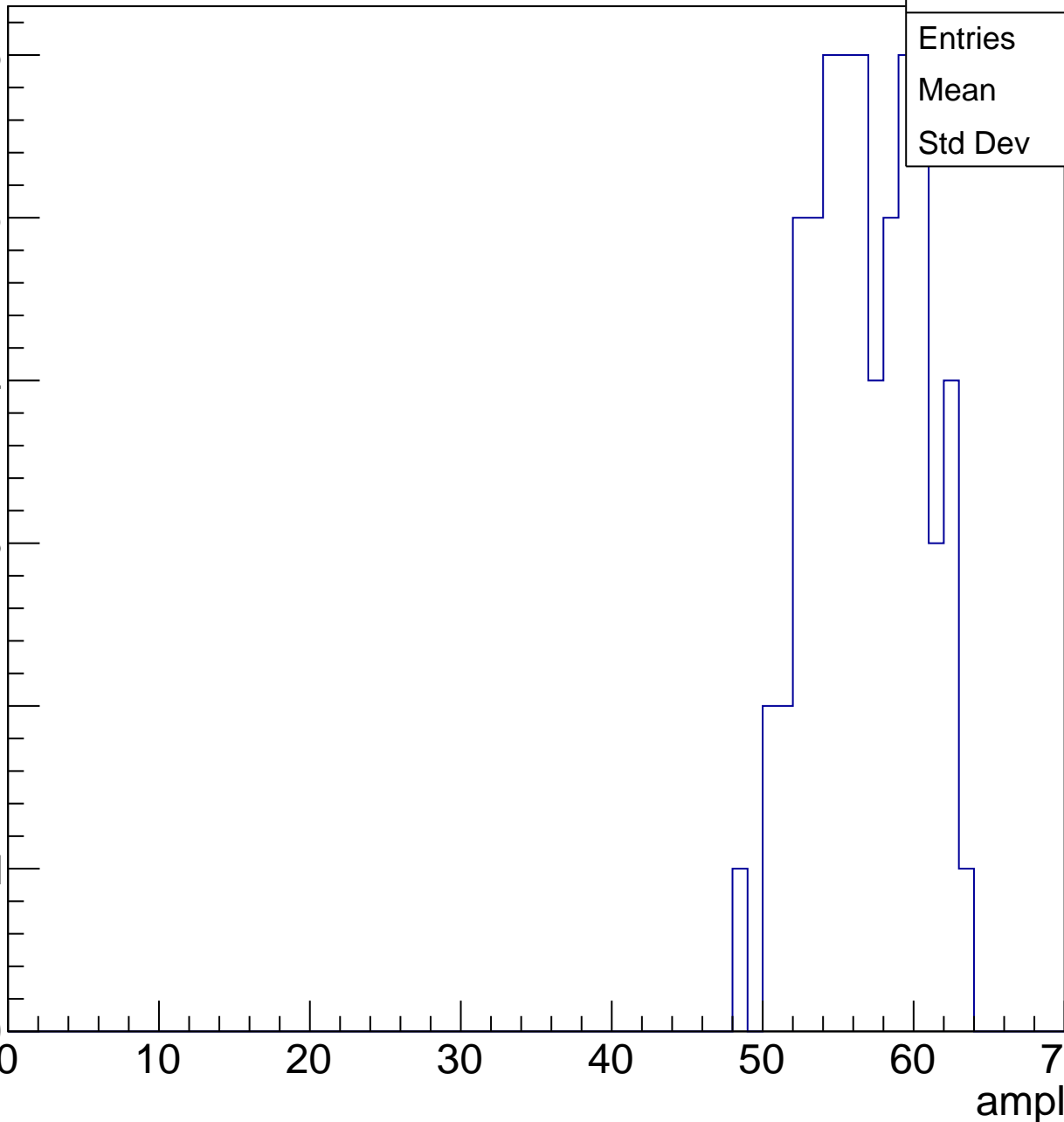
50

60

70

ampl

Entries	62
Mean	56.31
Std Dev	3.54

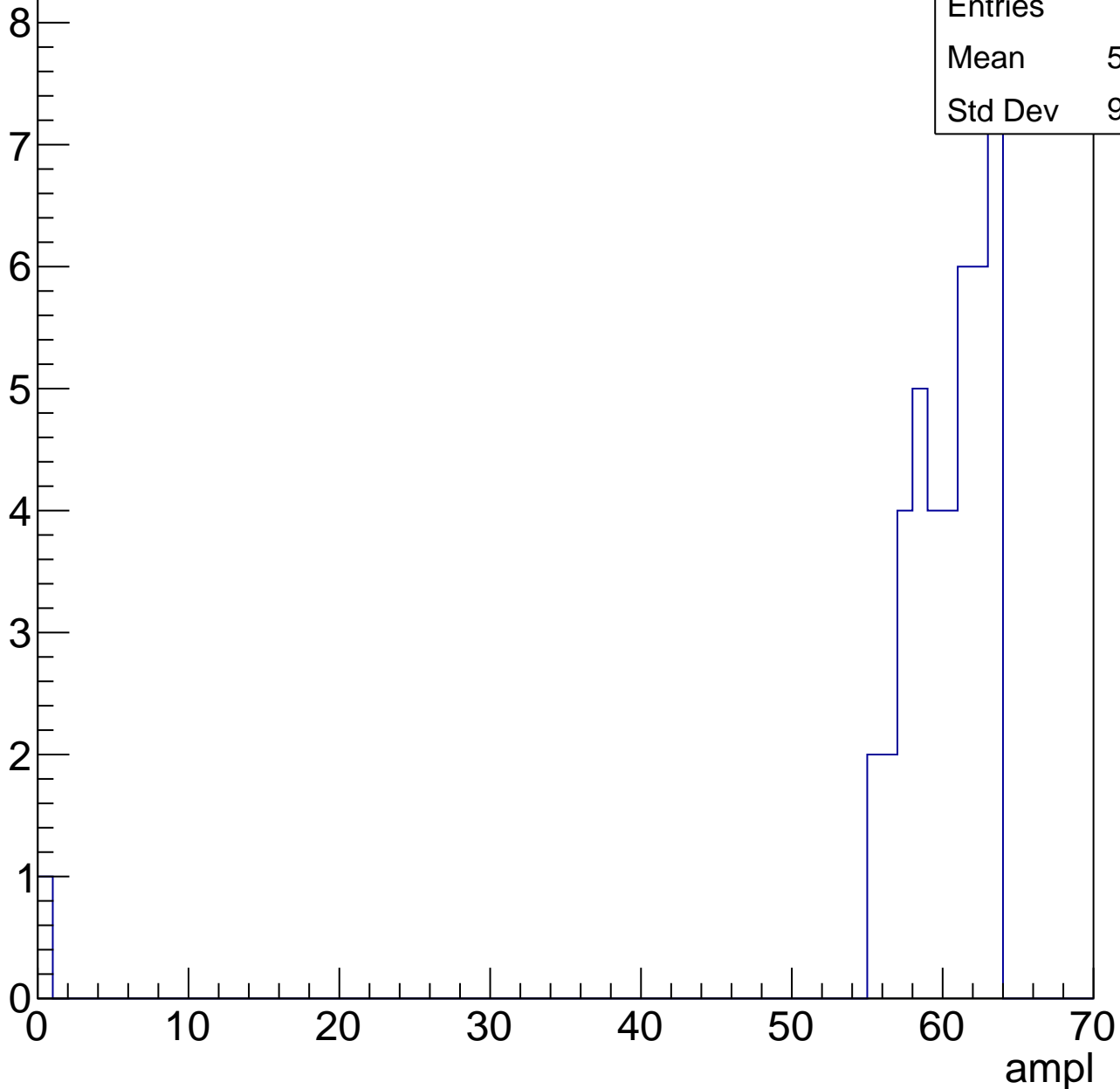


# B0L001S, U10-ch93, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	42
Mean	58.52
Std Dev	9.452



# B0L001S, U10-ch93, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch93, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U10-ch94, adc0

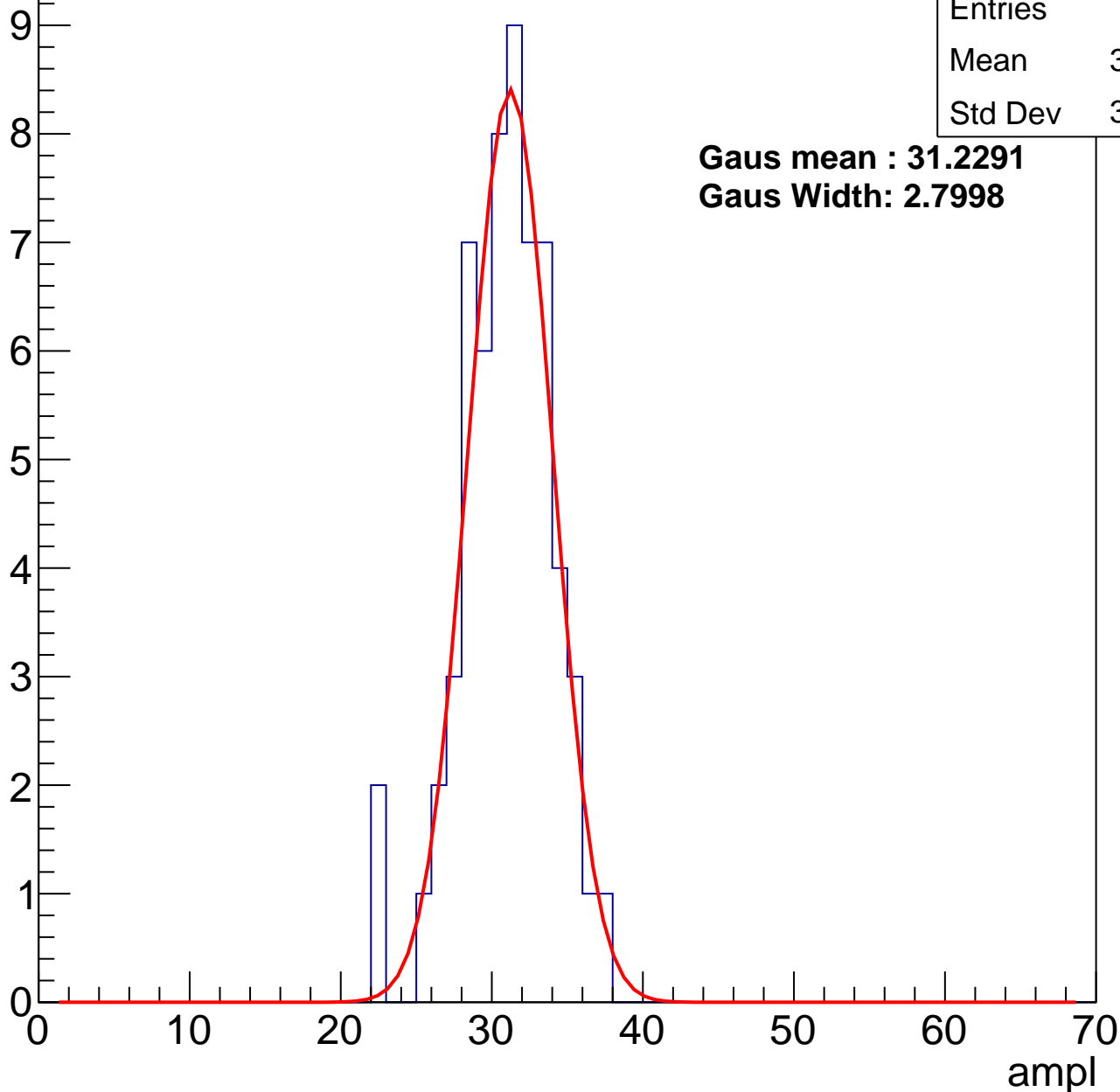
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	30.49
Std Dev	3.017

**Gaus mean : 31.2291**

**Gaus Width: 2.7998**



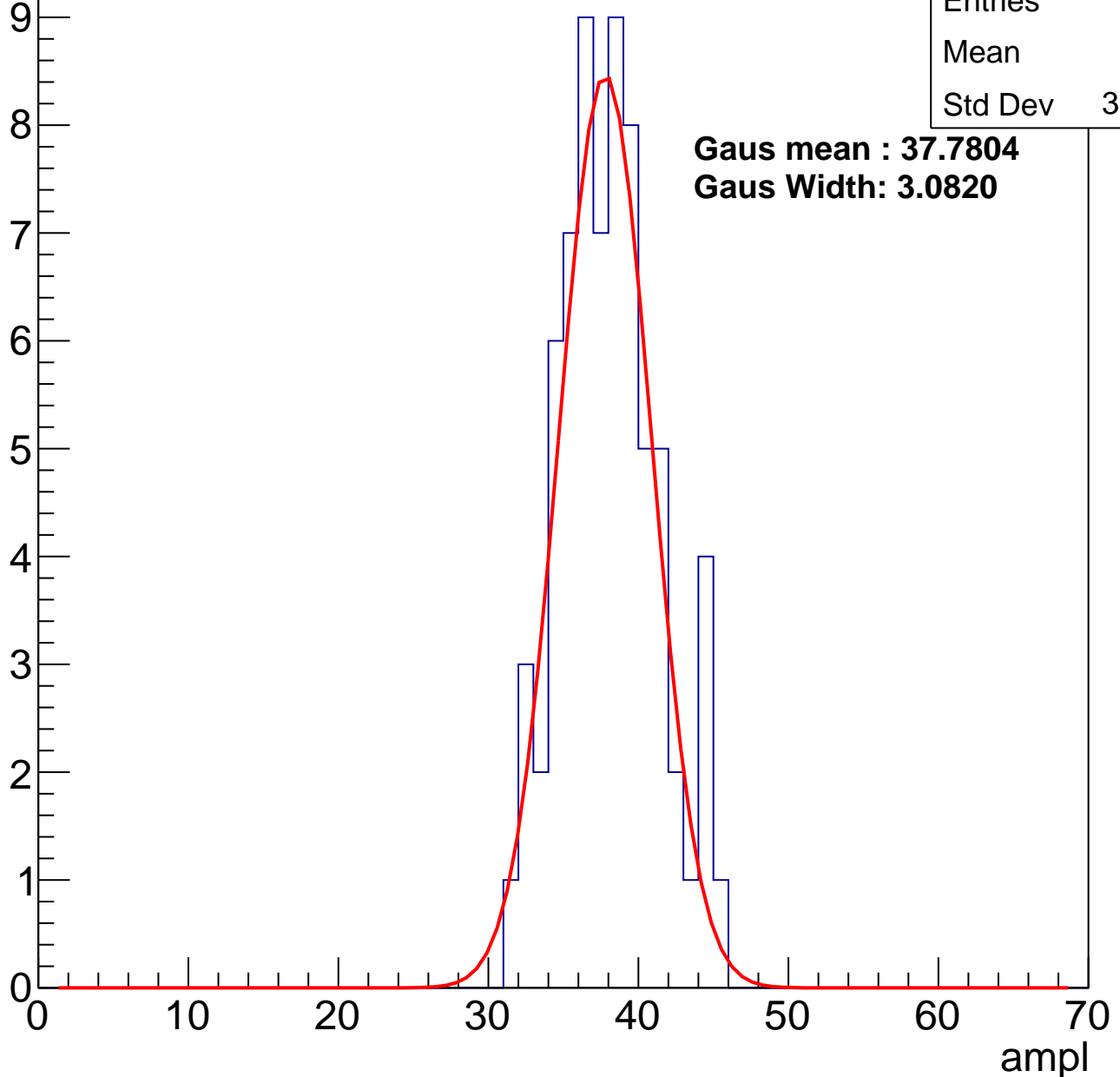
# B0L001S, U10-ch94, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	37.6
Std Dev	3.209

**Gaus mean : 37.7804**  
**Gaus Width: 3.0820**



# B0L001S, U10-ch94, adc2

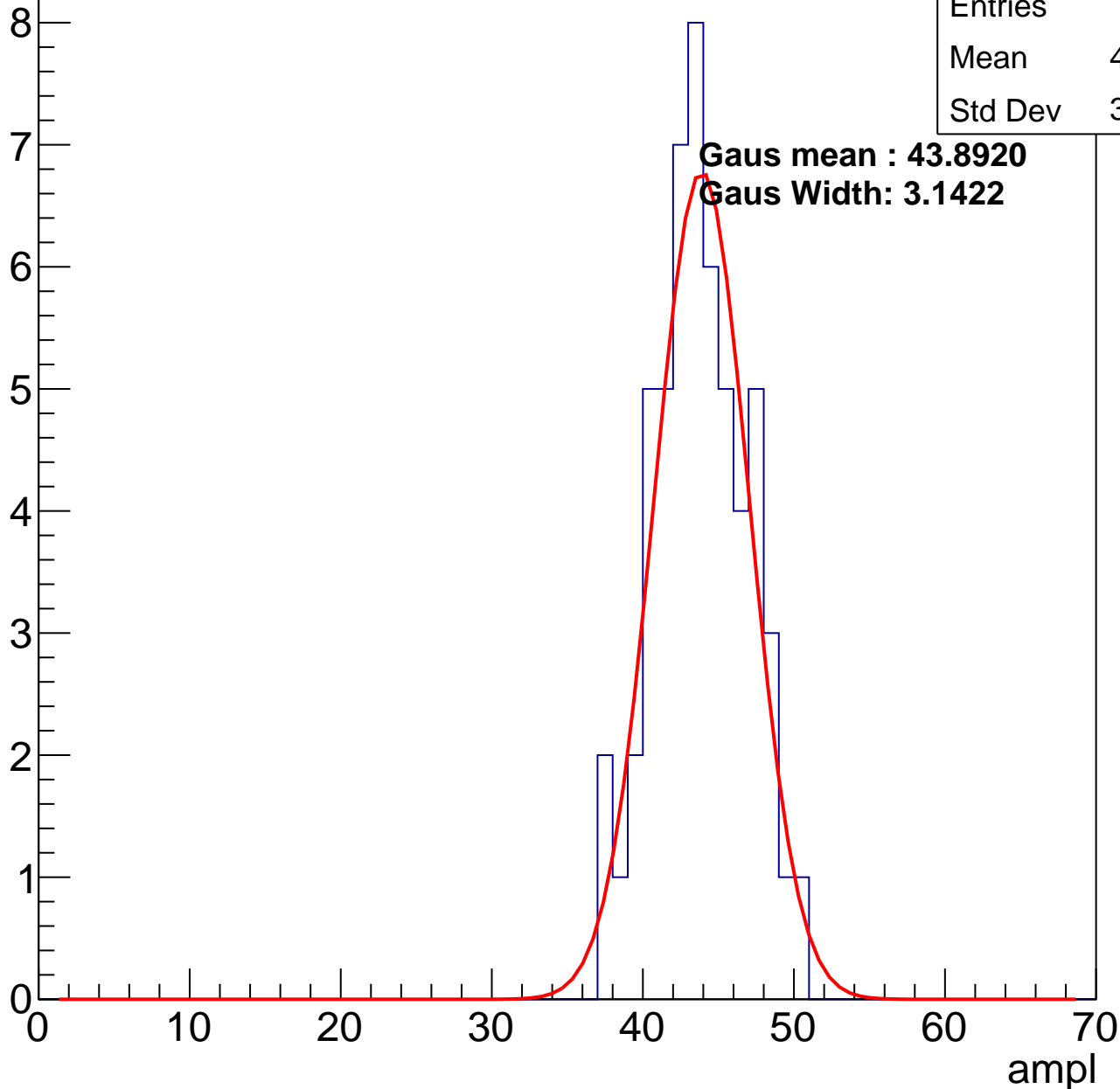
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	43.35
Std Dev	3.004

**Gaus mean : 43.8920**

**Gaus Width: 3.1422**

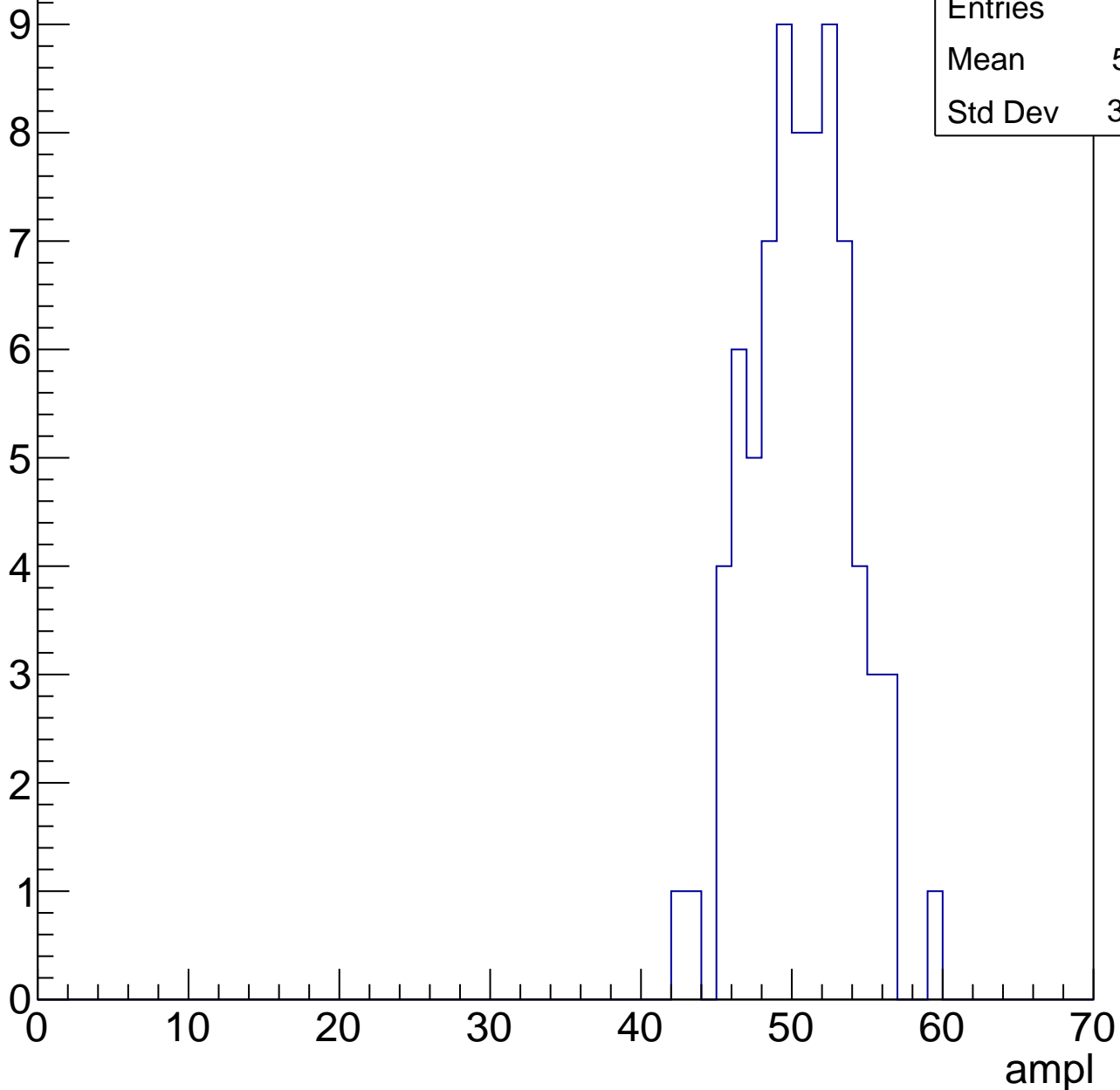


# B0L001S, U10-ch94, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	76
Mean	50.11
Std Dev	3.295

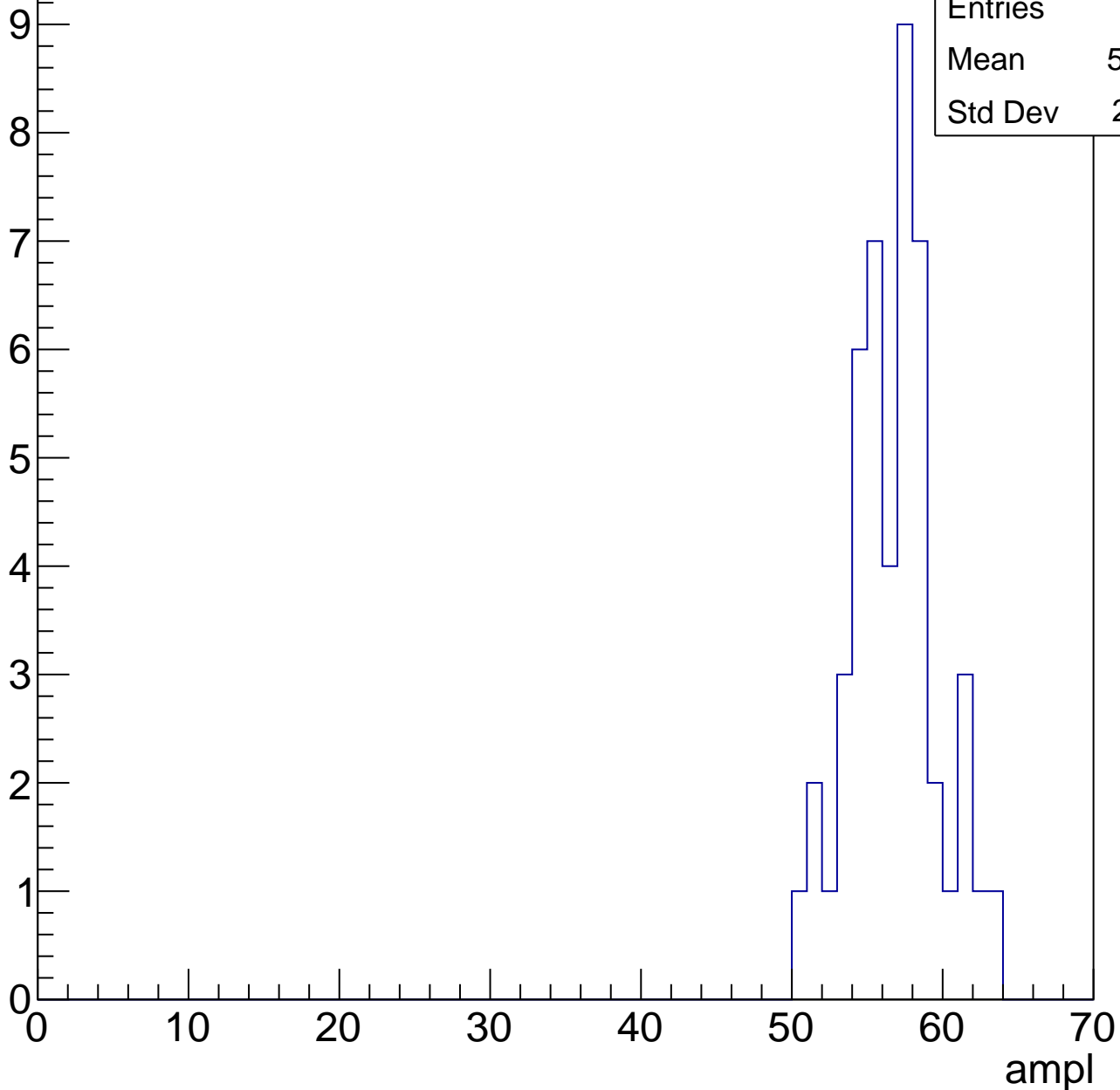


# B0L001S, U10-ch94, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	48
Mean	56.27
Std Dev	2.841

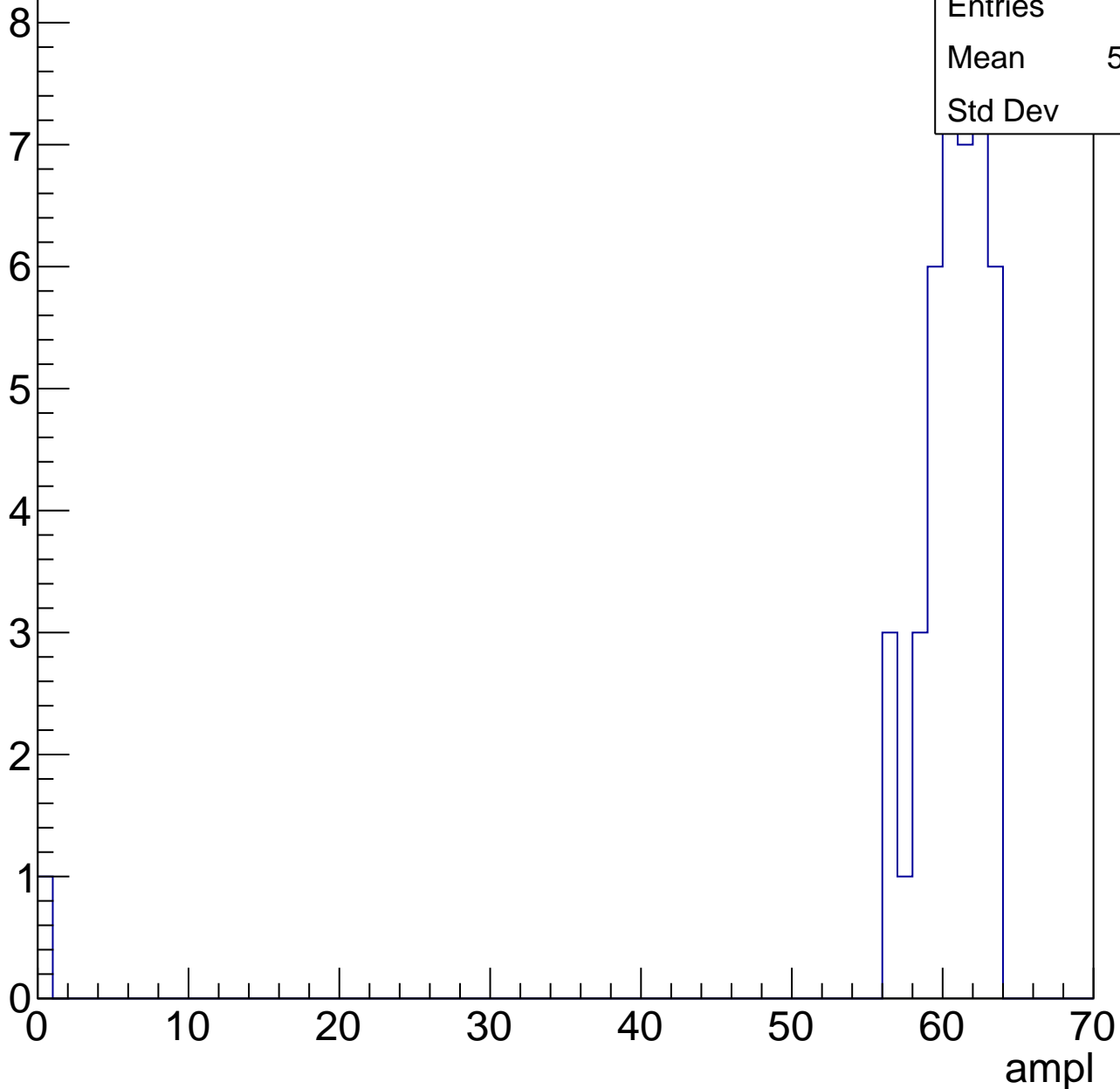


# B0L001S, U10-ch94, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

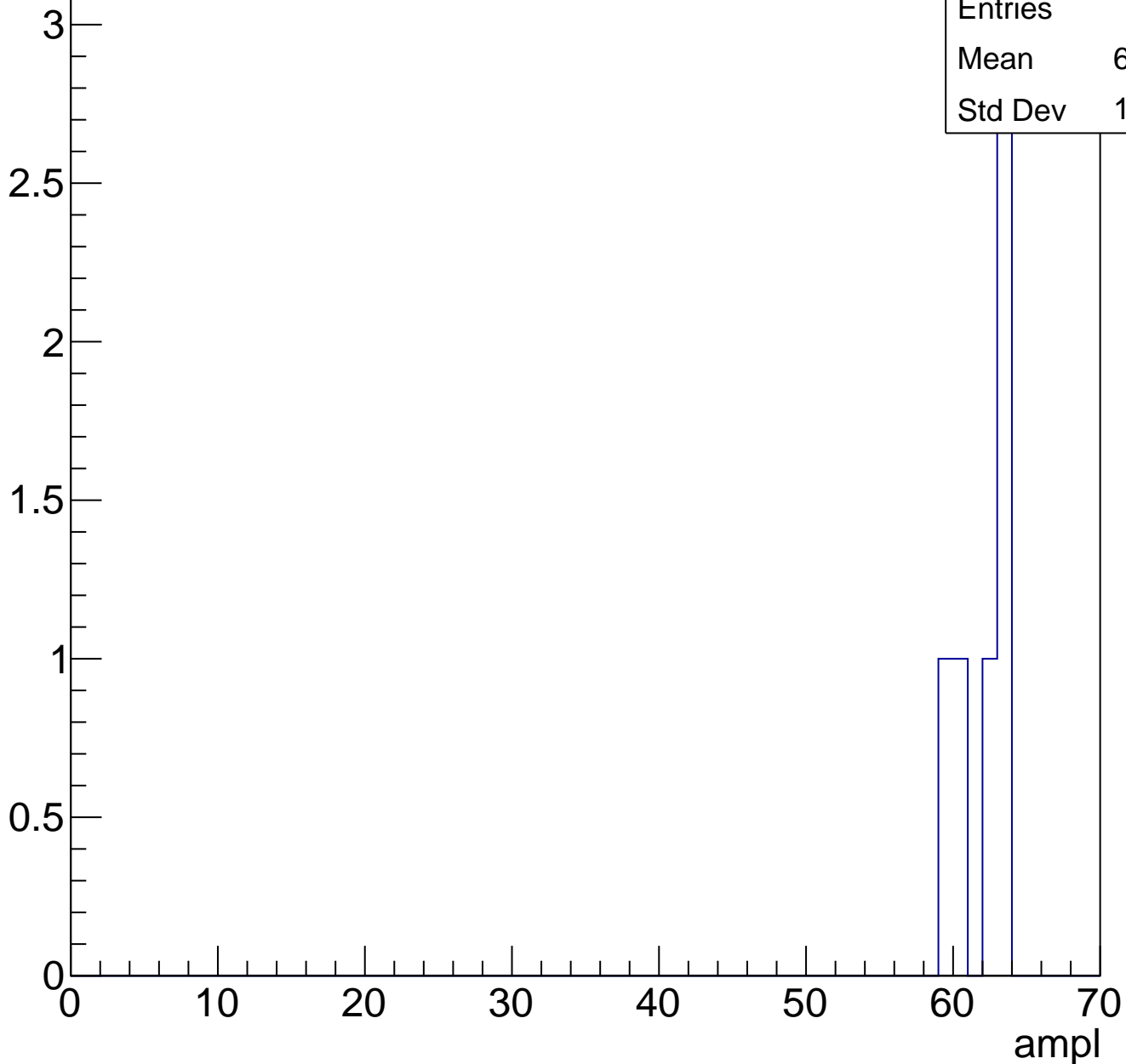
Entries	43
Mean	58.93
Std Dev	9.3



# B0L001S, U10-ch94, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch94, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U10-ch95, adc0

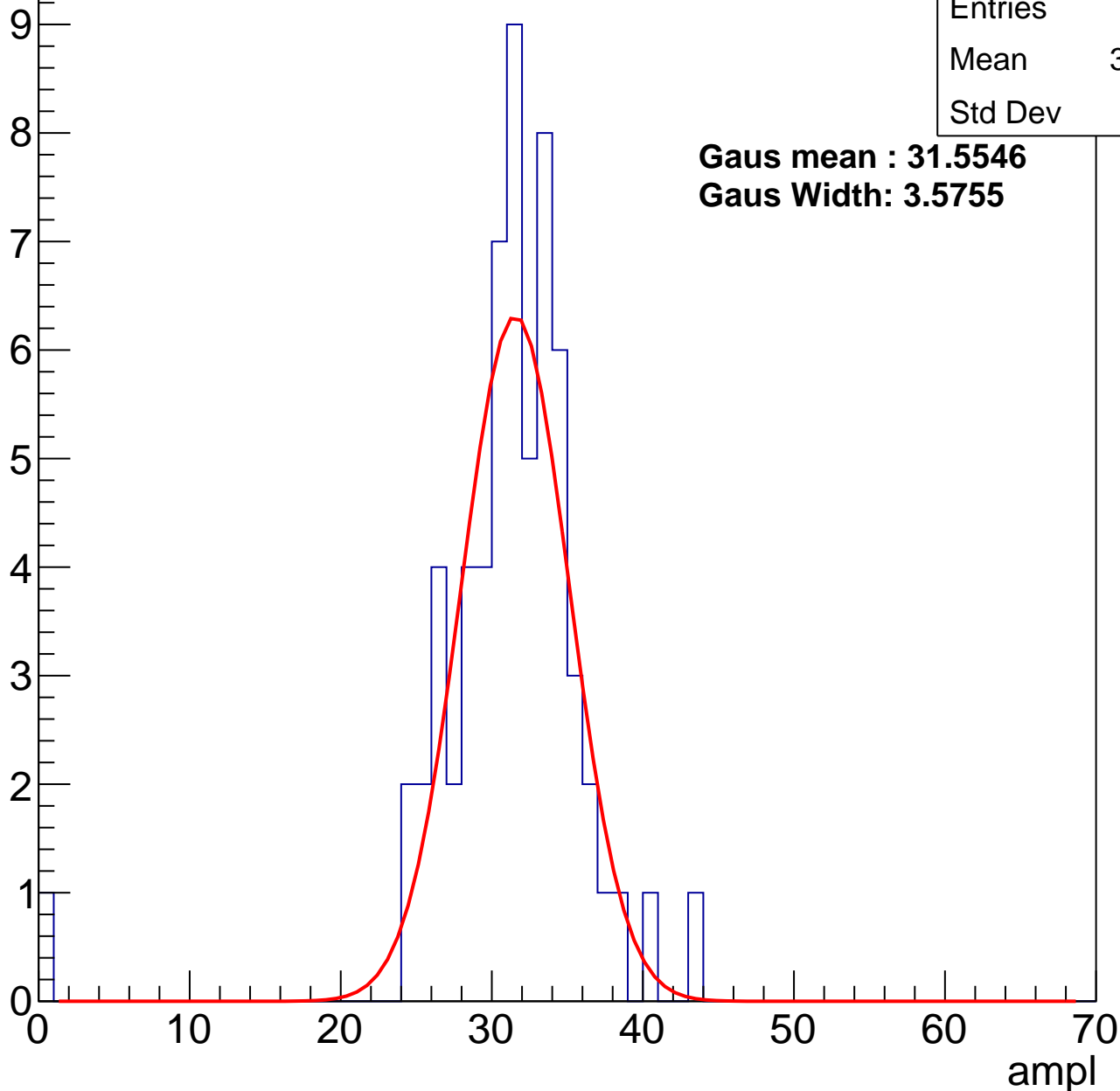
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	30.73
Std Dev	5.37

**Gaus mean : 31.5546**

**Gaus Width: 3.5755**



# B0L001S, U10-ch95, adc1

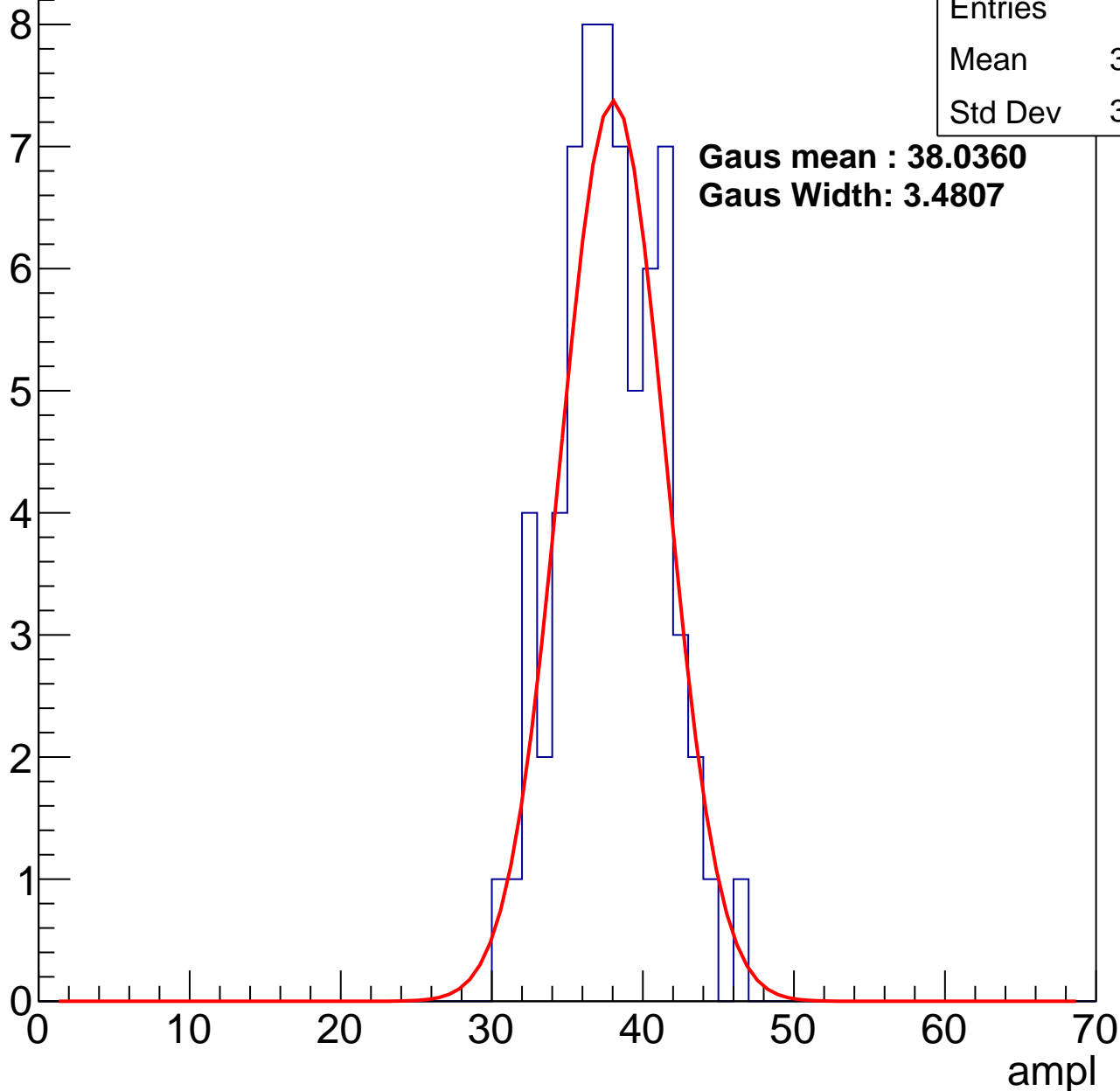
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	37.46
Std Dev	3.334

**Gaus mean : 38.0360**

**Gaus Width: 3.4807**



# B0L001S, U10-ch95, adc2

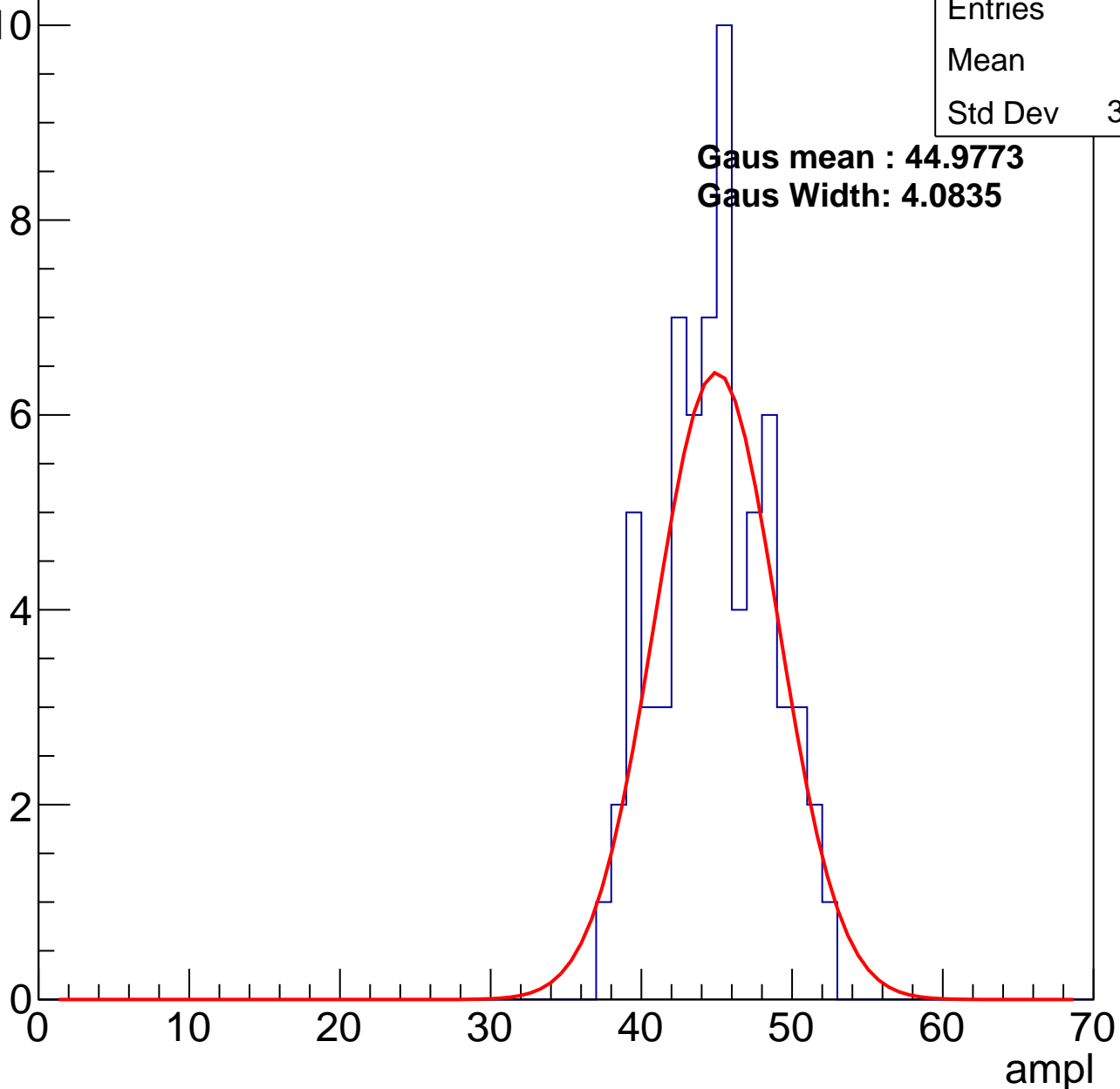
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	44.4
Std Dev	3.549

**Gaus mean : 44.9773**

**Gaus Width: 4.0835**

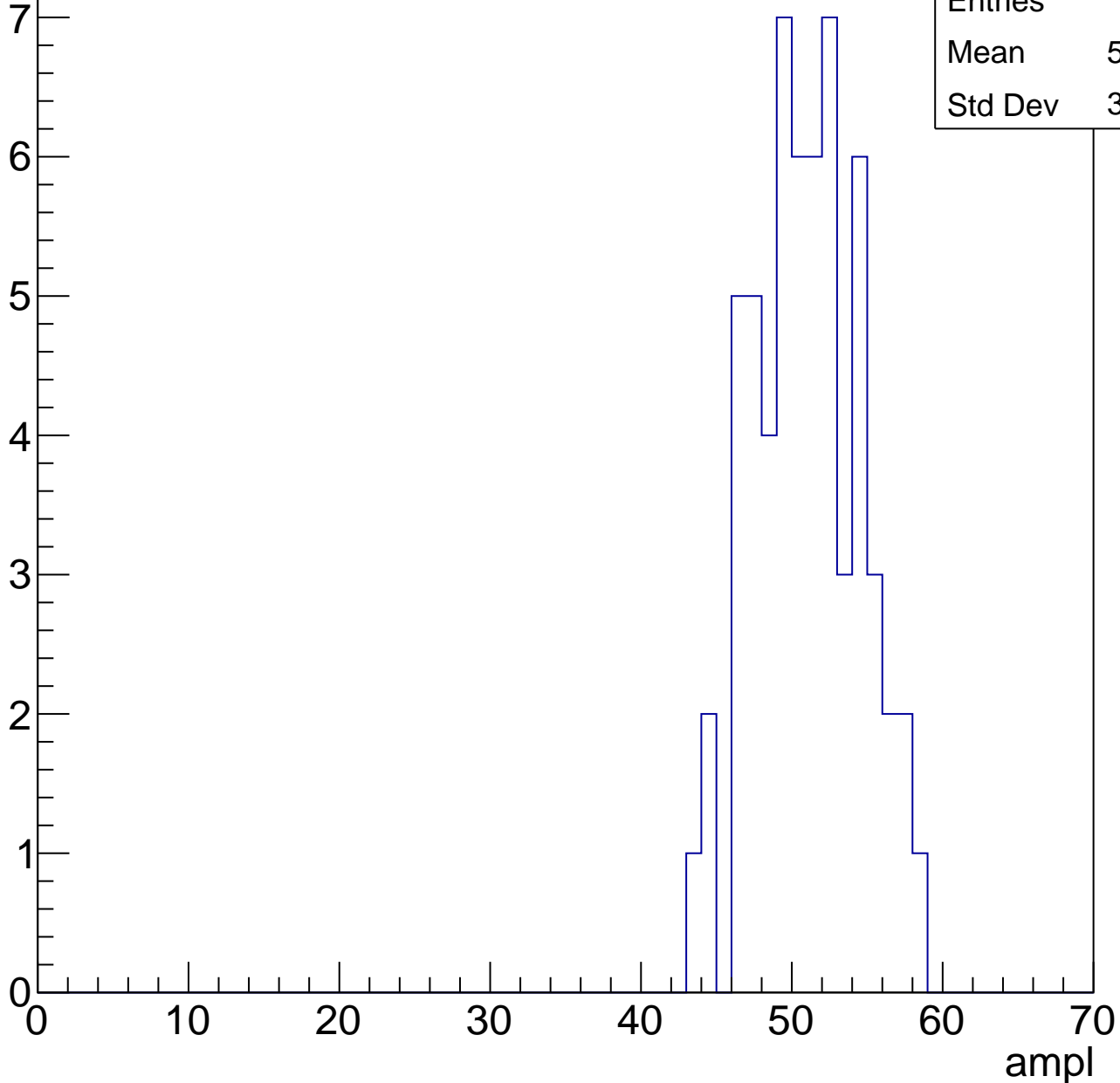


# B0L001S, U10-ch95, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	50.55
Std Dev	3.457

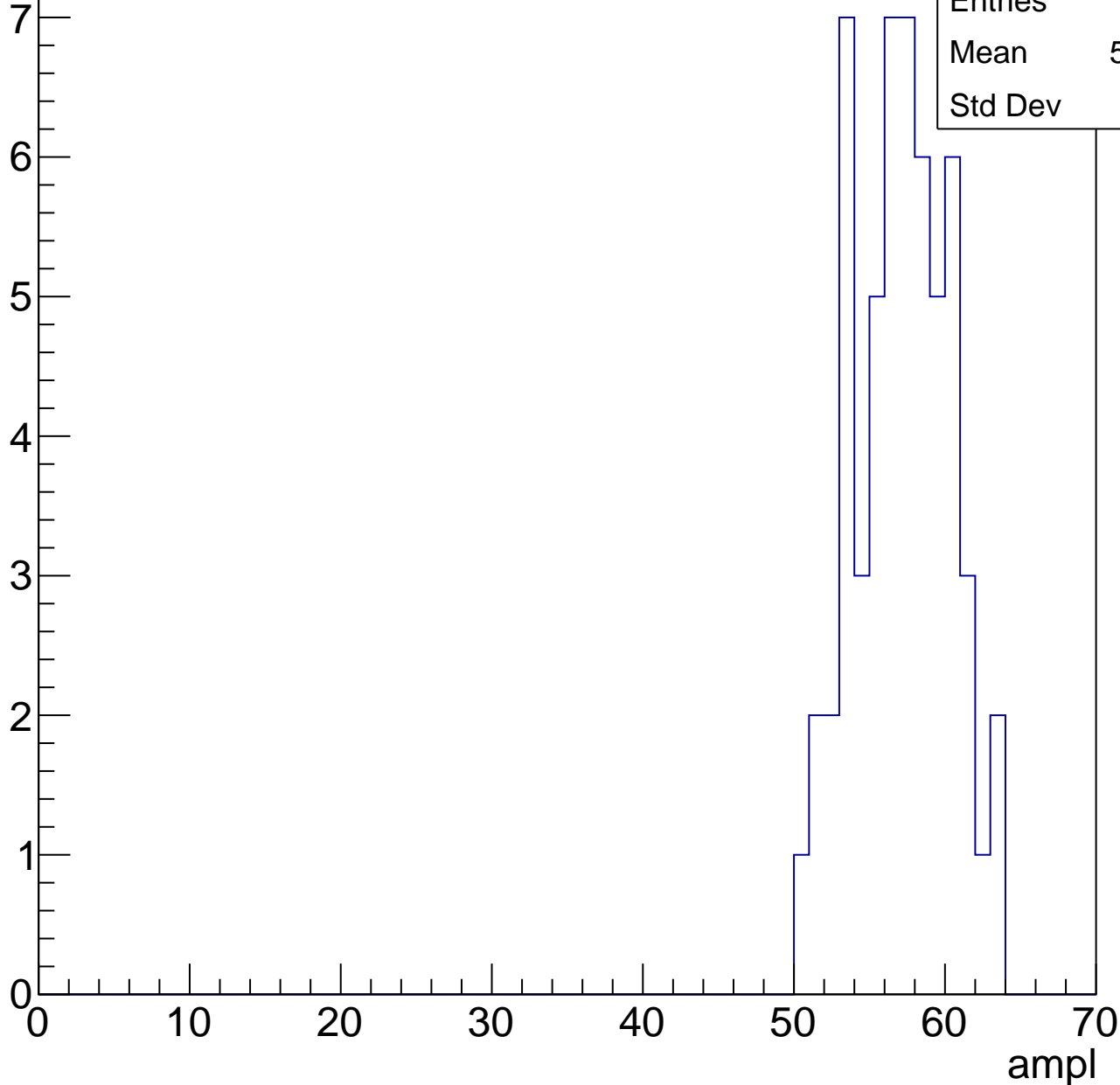


# B0L001S, U10-ch95, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	56.65
Std Dev	3.12

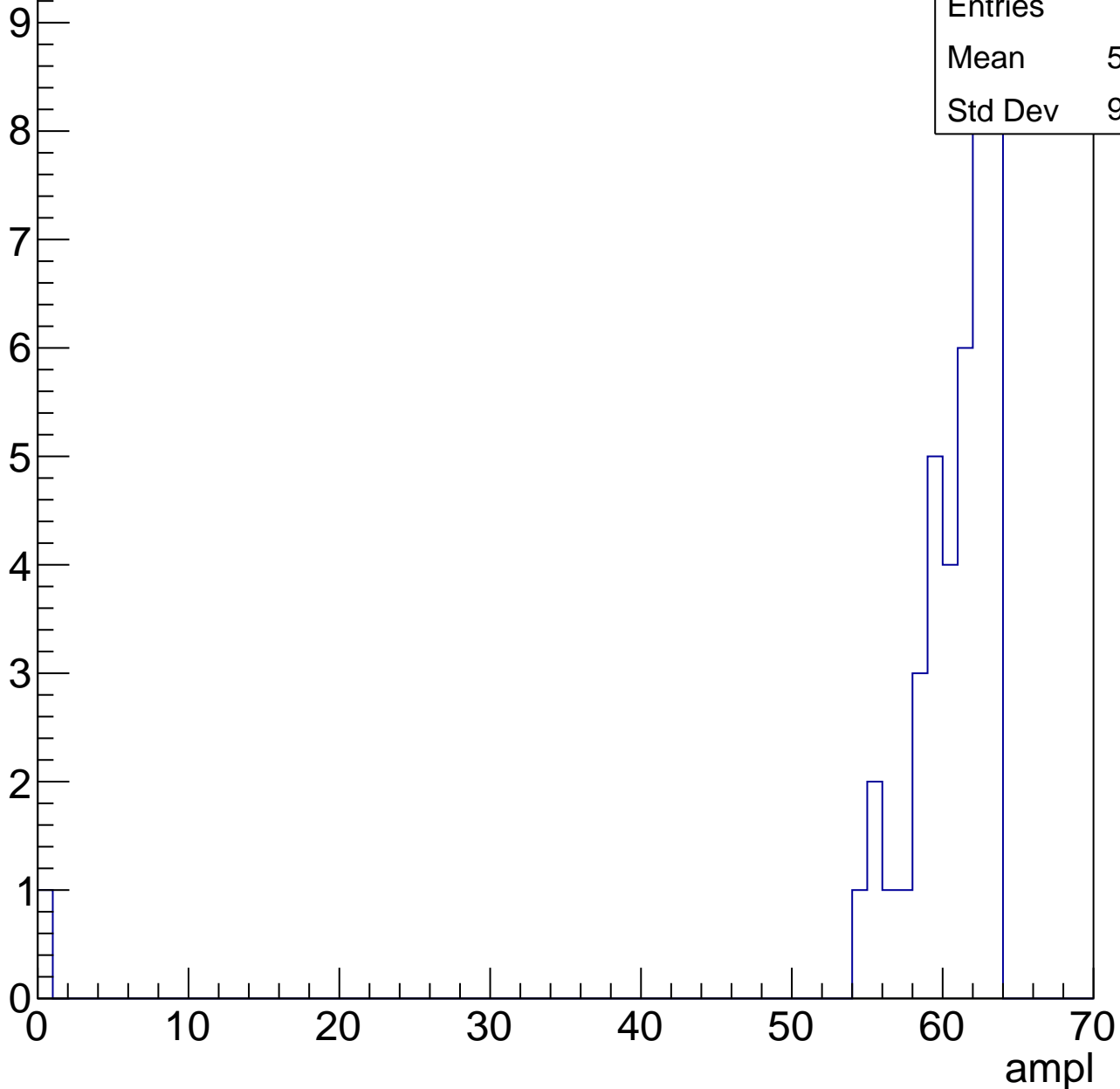


# B0L001S, U10-ch95, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	41
Mean	58.88
Std Dev	9.615



# B0L001S, U10-ch95, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch95, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	23
Std Dev	0

ampl

0 10 20 30 40 50 60 70

# B0L001S, U10-ch96, adc0

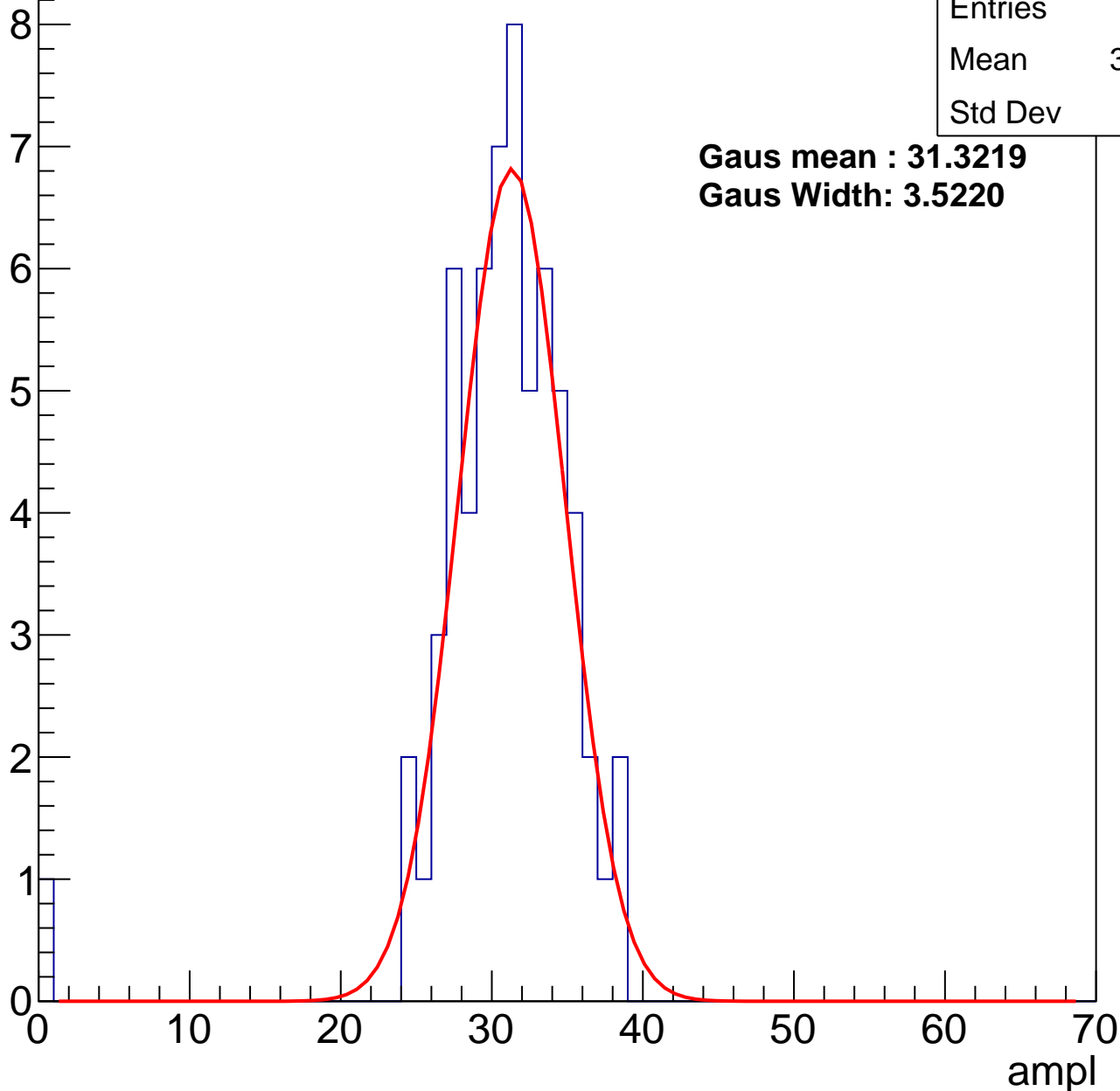
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	30.32
Std Dev	5.08

**Gaus mean : 31.3219**

**Gaus Width: 3.5220**



# B0L001S, U10-ch96, adc1

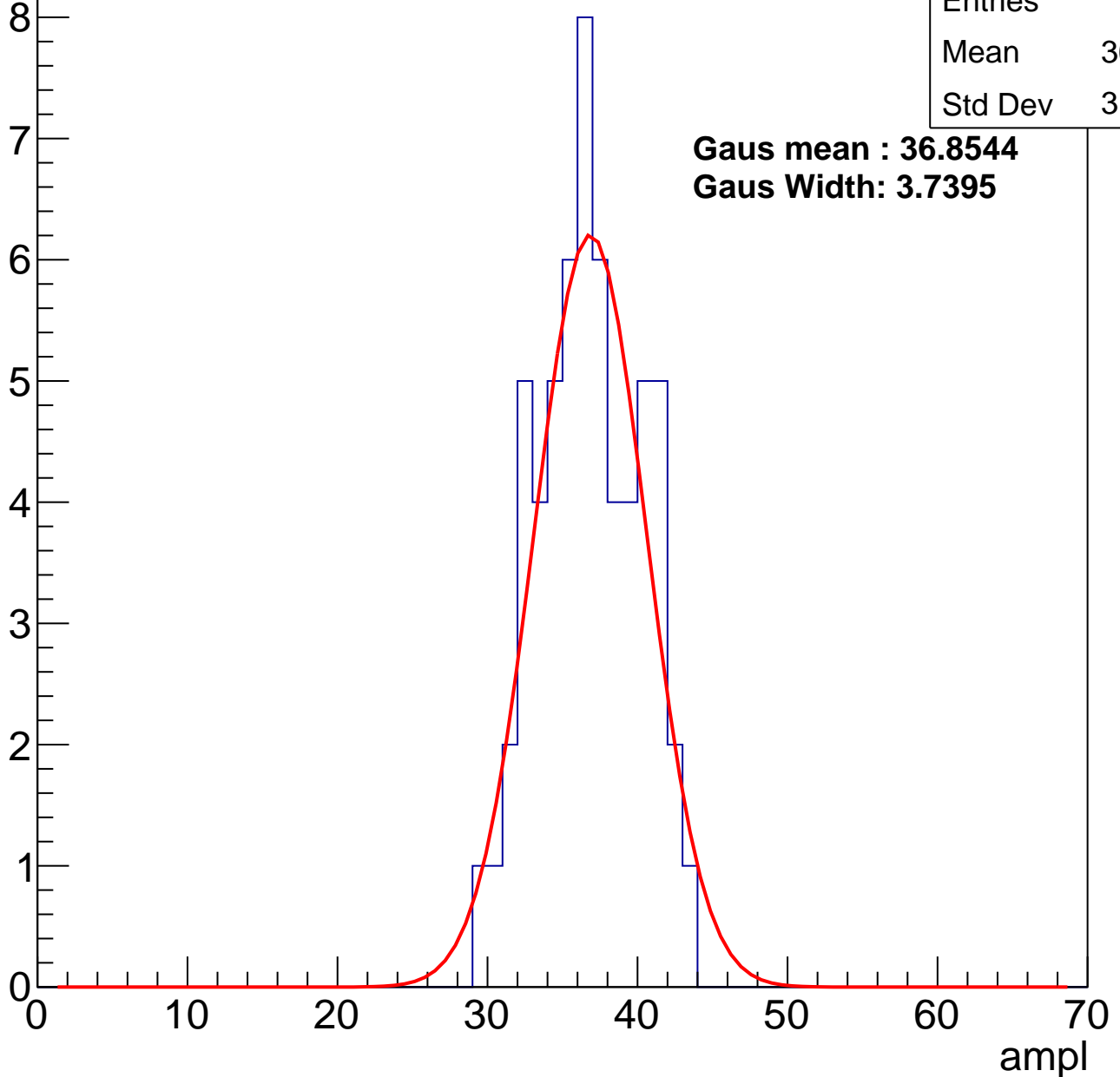
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	36.32
Std Dev	3.332

**Gaus mean : 36.8544**

**Gaus Width: 3.7395**



# B0L001S, U10-ch96, adc2

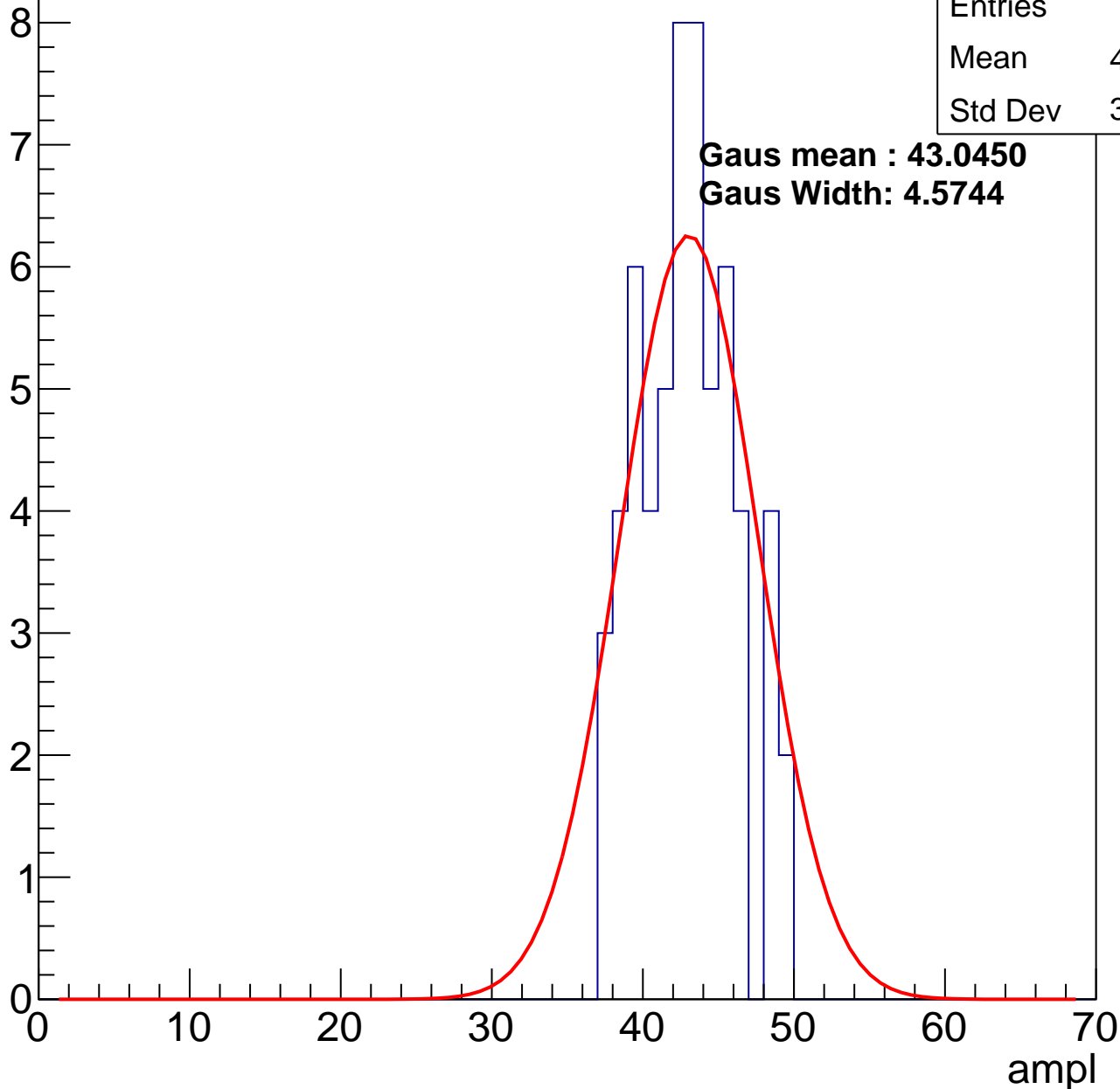
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	42.47
Std Dev	3.159

**Gaus mean : 43.0450**

**Gaus Width: 4.5744**



# B0L001S, U10-ch96, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

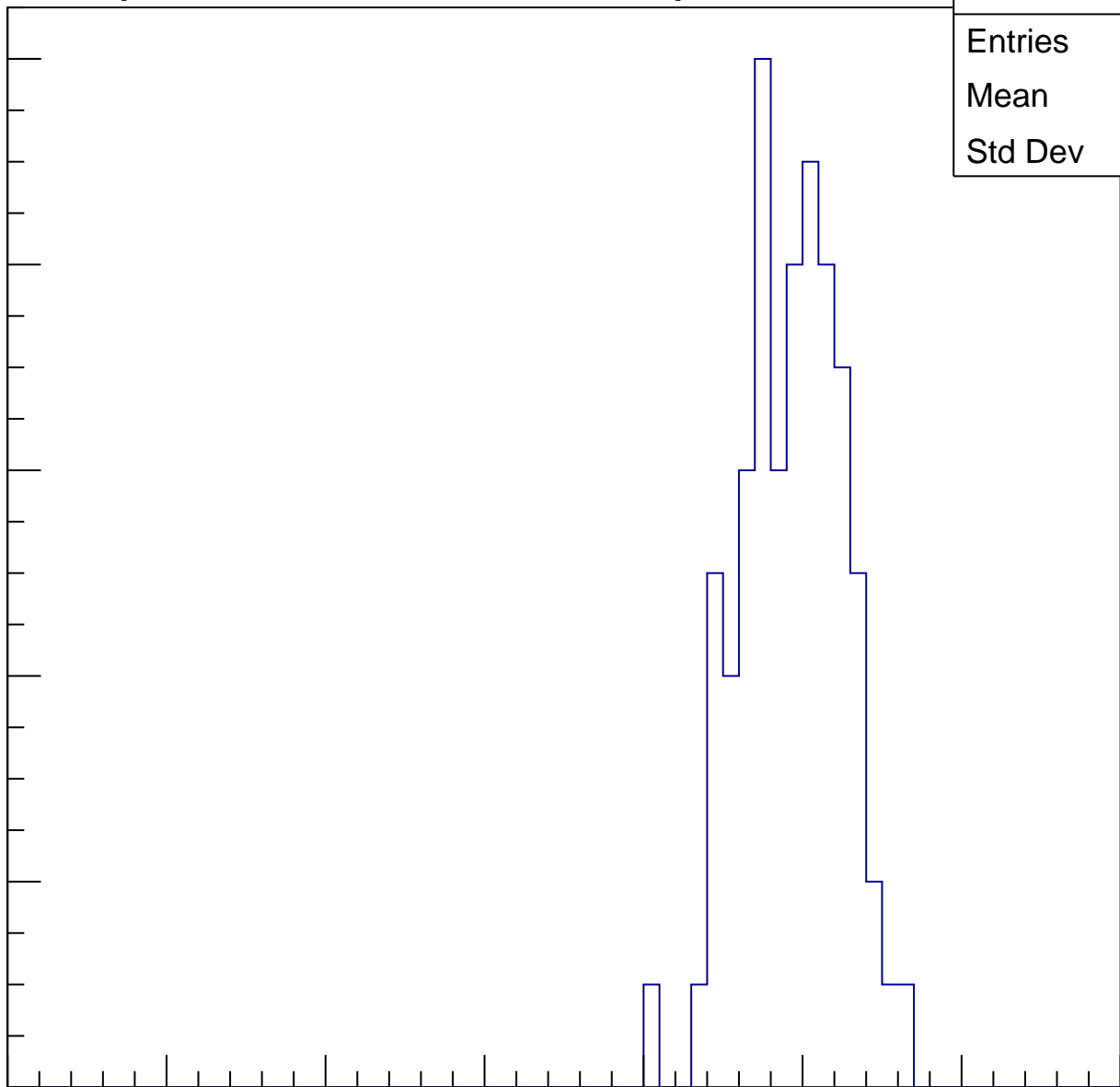
Entries	74
Mean	48.85
Std Dev	3.127

Entry

10  
8  
6  
4  
2  
0

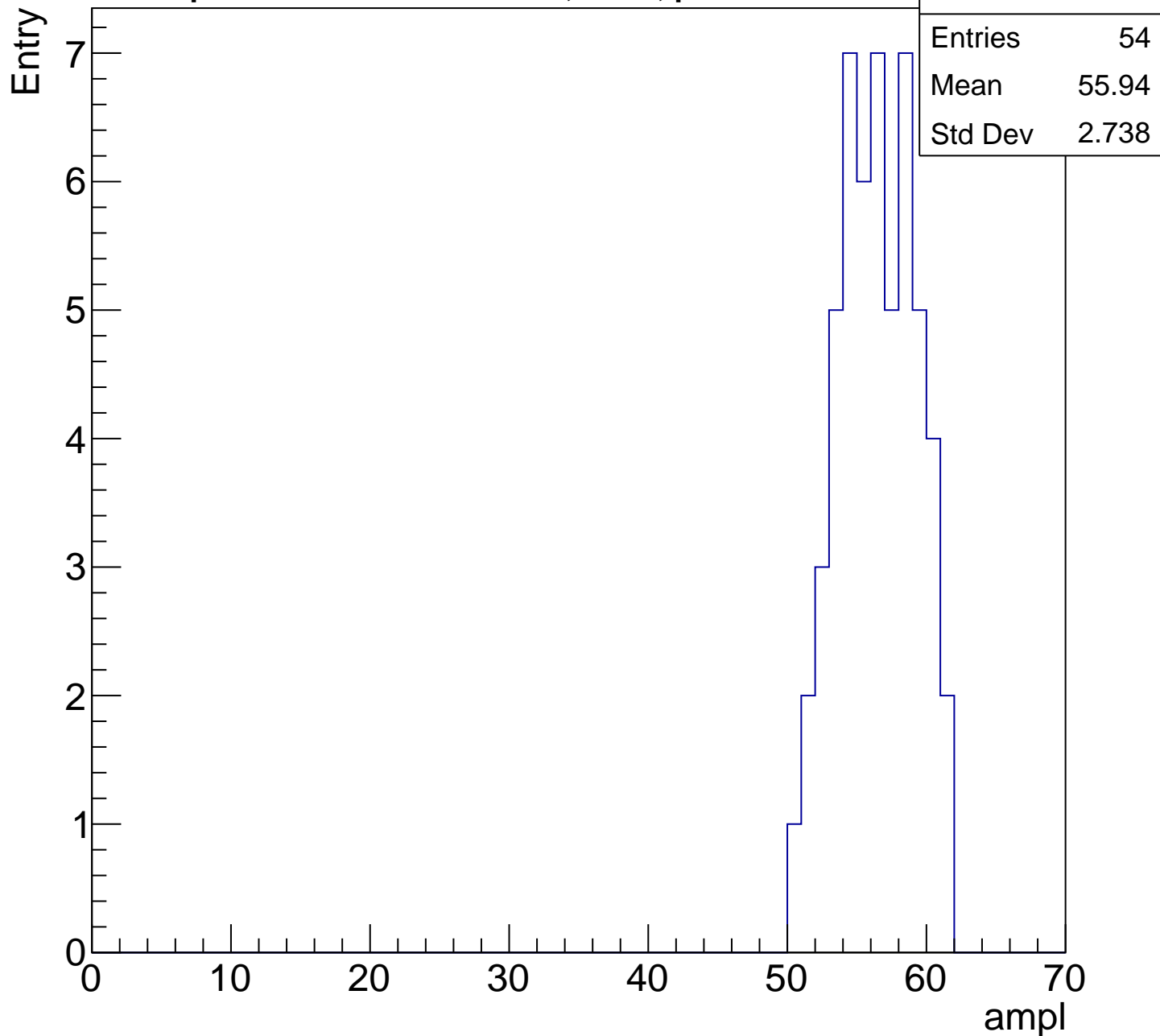
0 10 20 30 40 50 60 70

ampl



# B0L001S, U10-ch96, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

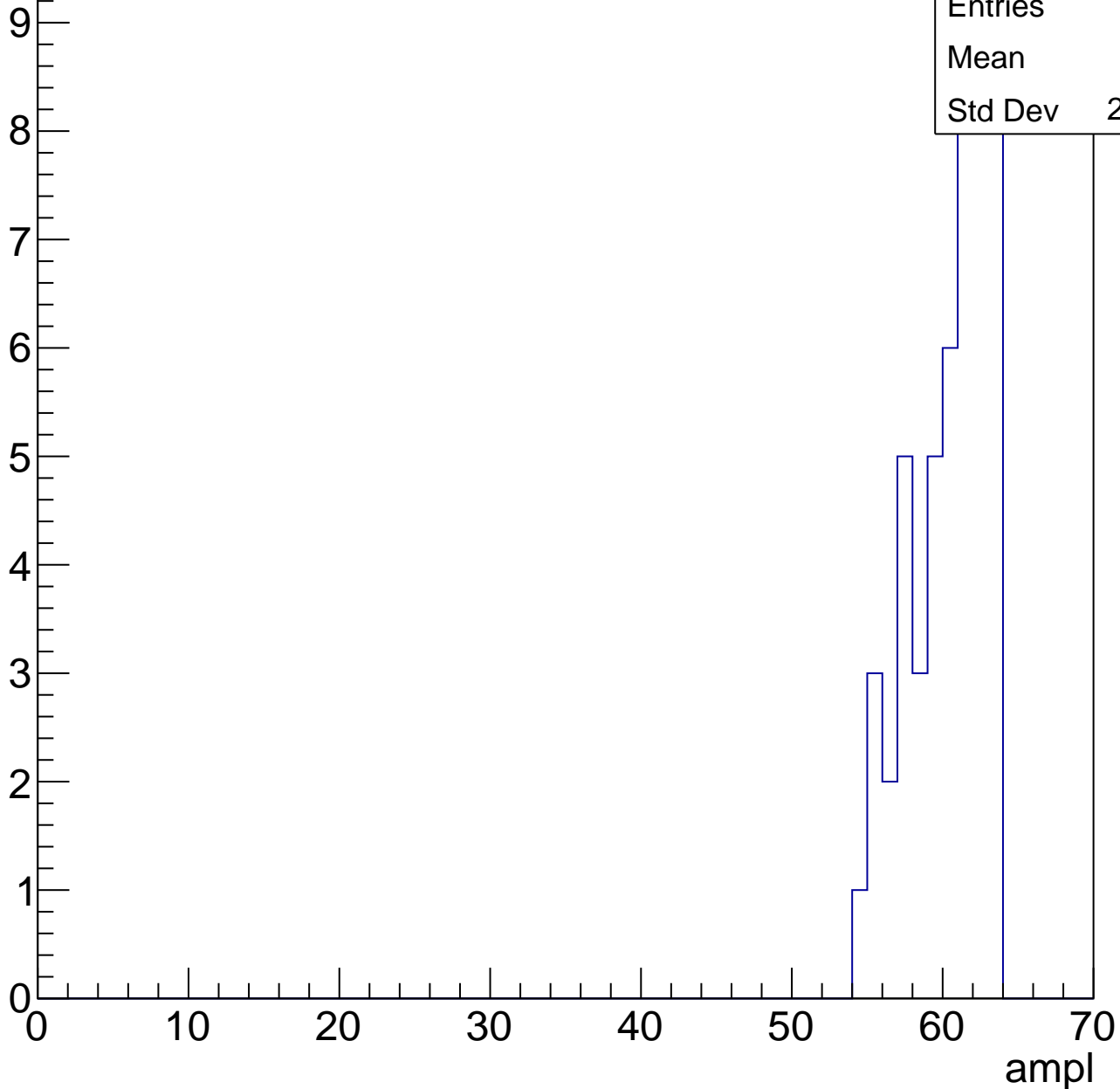


# B0L001S, U10-ch96, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	50
Mean	59.9
Std Dev	2.532



# B0L001S, U10-ch96, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

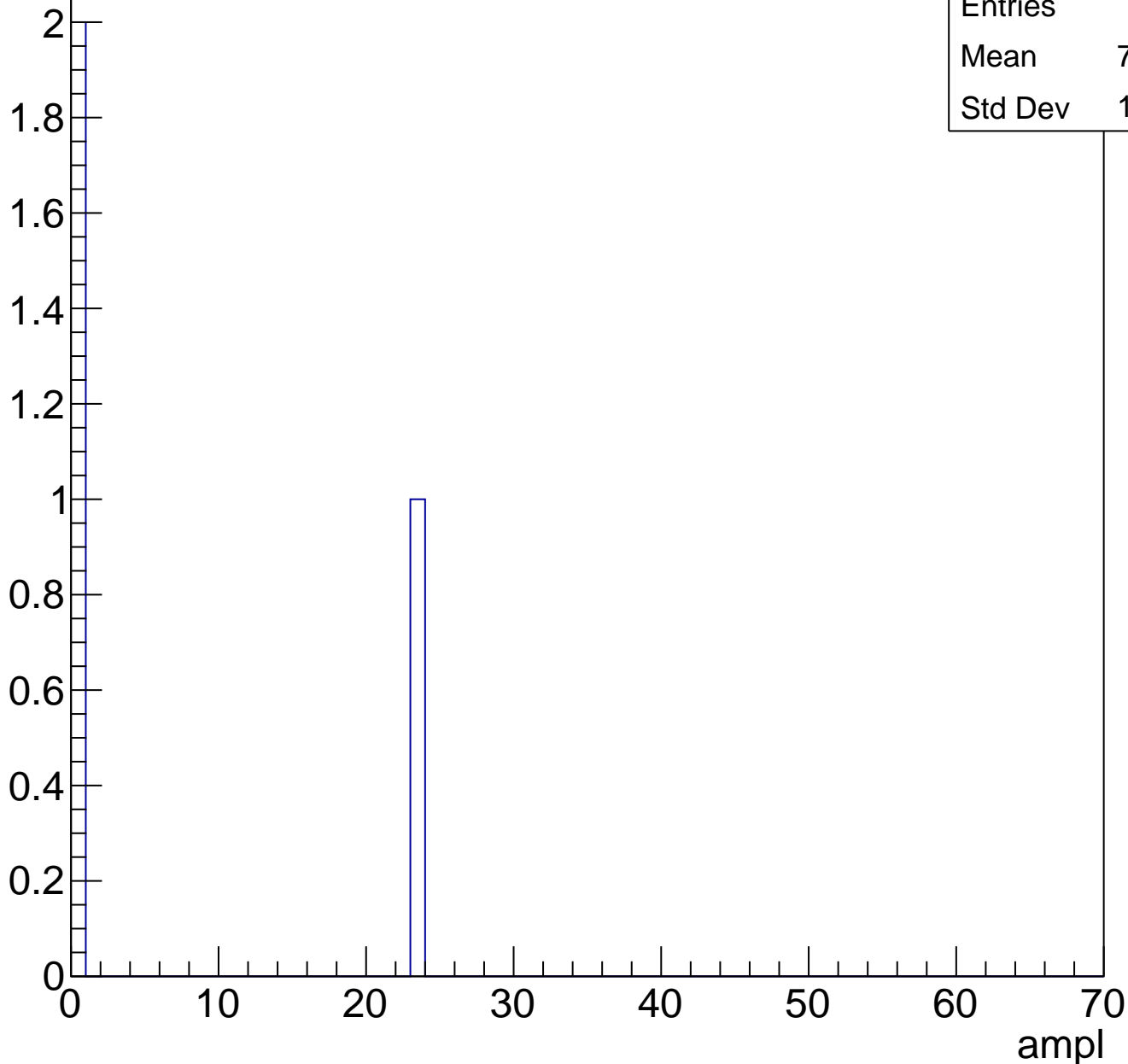




# B0L001S, U10-ch96, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U10-ch97, adc0

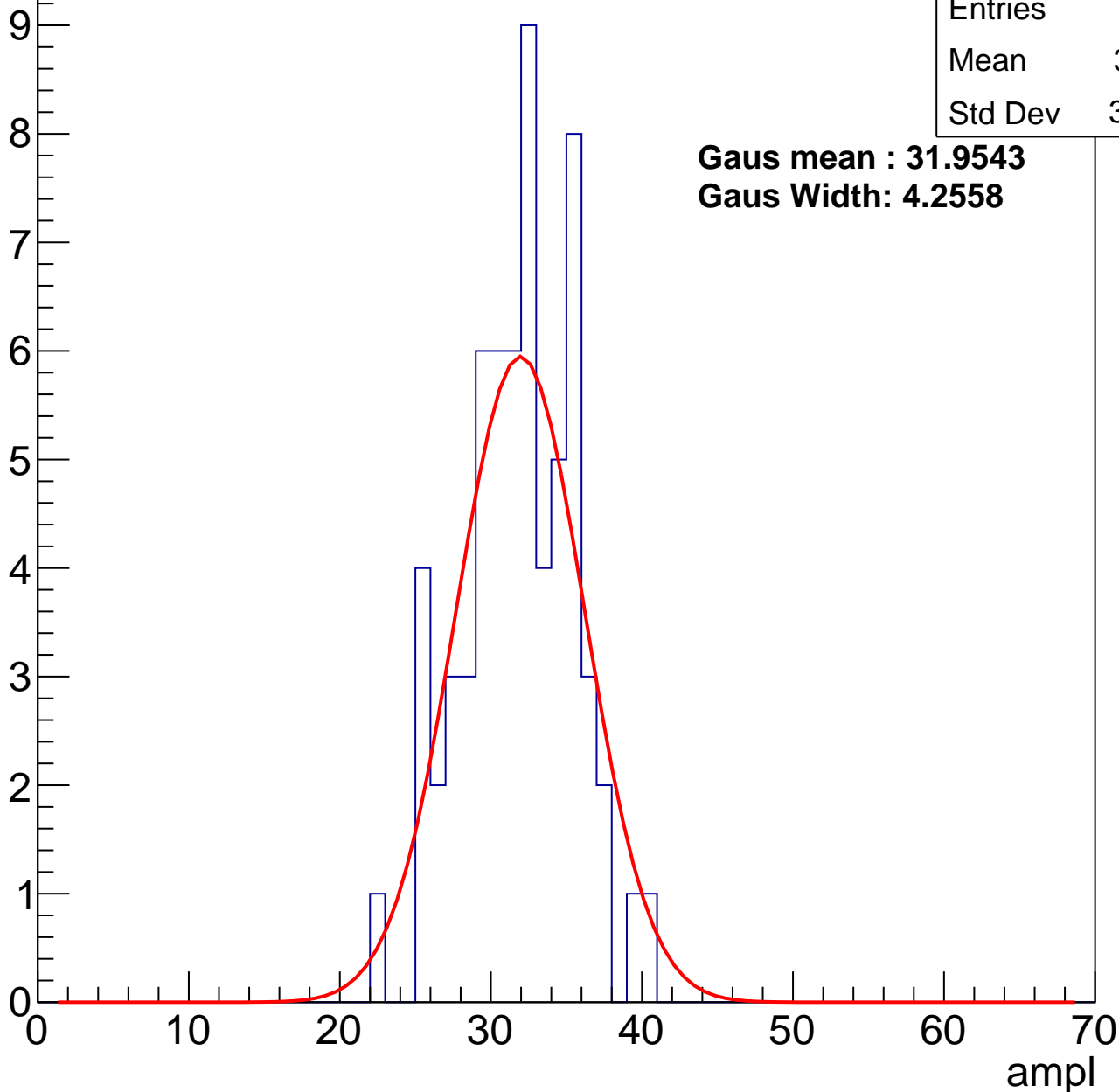
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	31.41
Std Dev	3.665

**Gaus mean : 31.9543**

**Gaus Width: 4.2558**



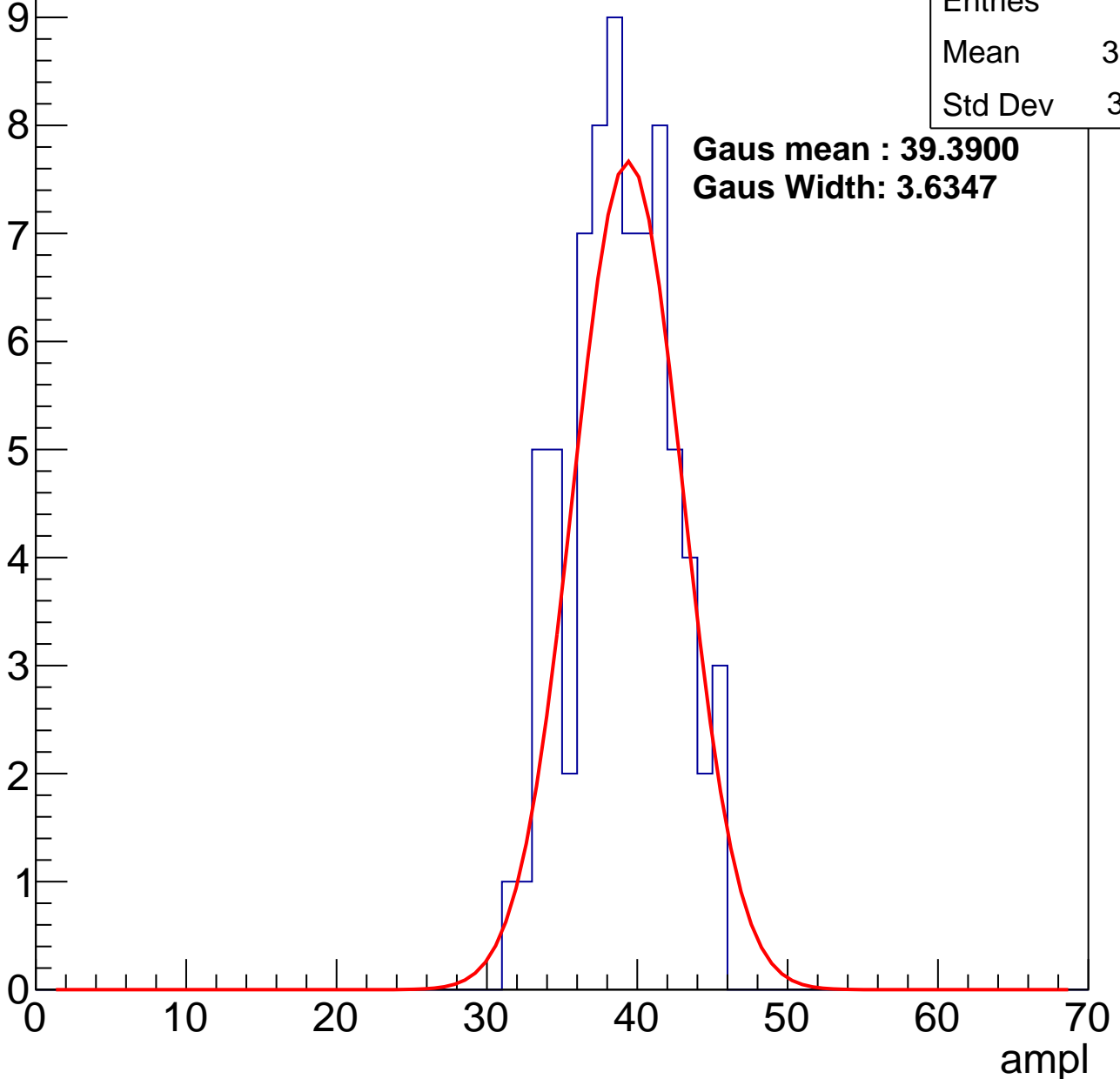
# B0L001S, U10-ch97, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	38.43
Std Dev	3.361

**Gaus mean : 39.3900**  
**Gaus Width: 3.6347**



# B0L001S, U10-ch97, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	60
Mean	45.25
Std Dev	3.118

**Gaus mean : 45.6696**

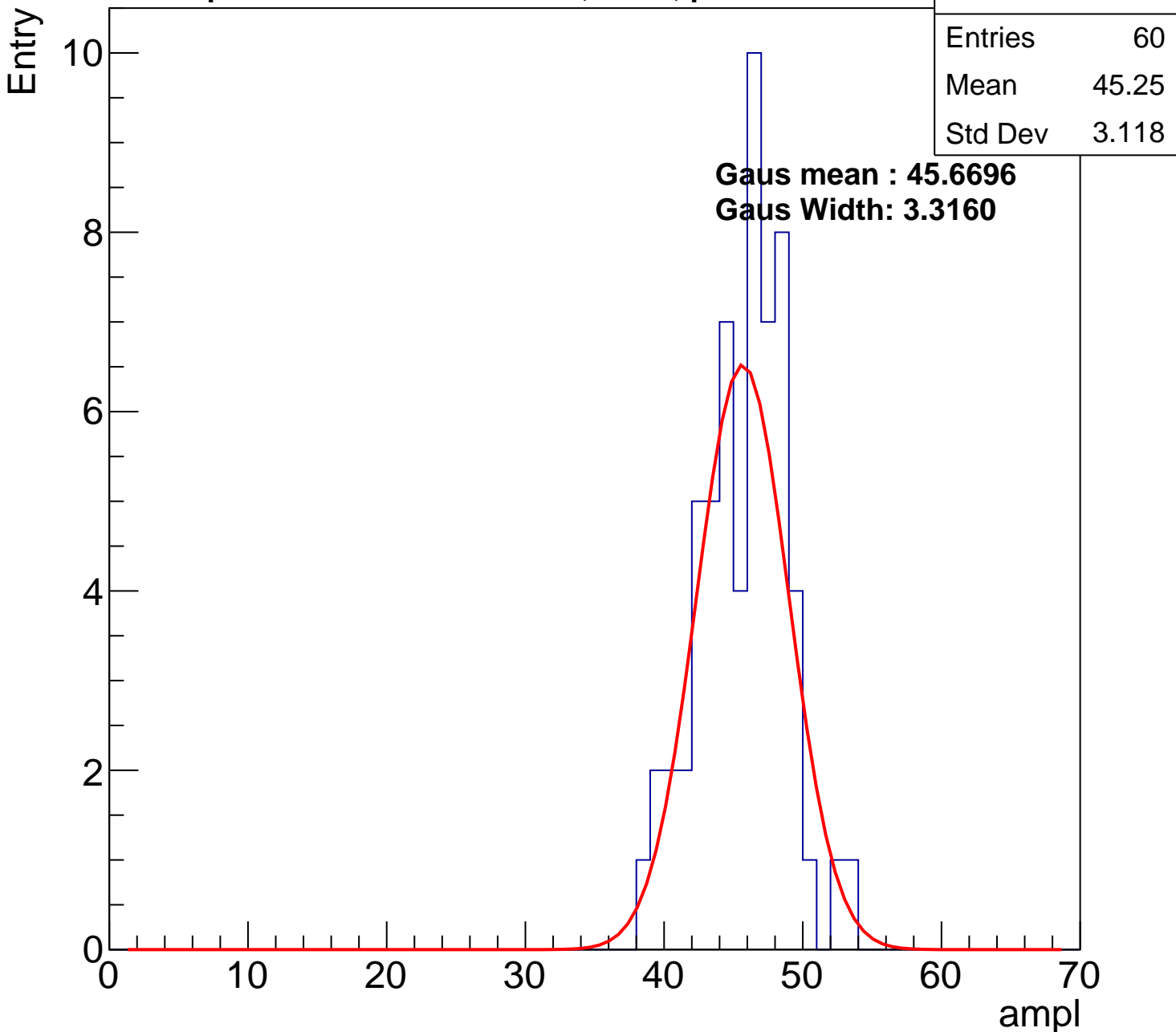
**Gaus Width: 3.3160**

Entry

10  
8  
6  
4  
2  
0

ampl

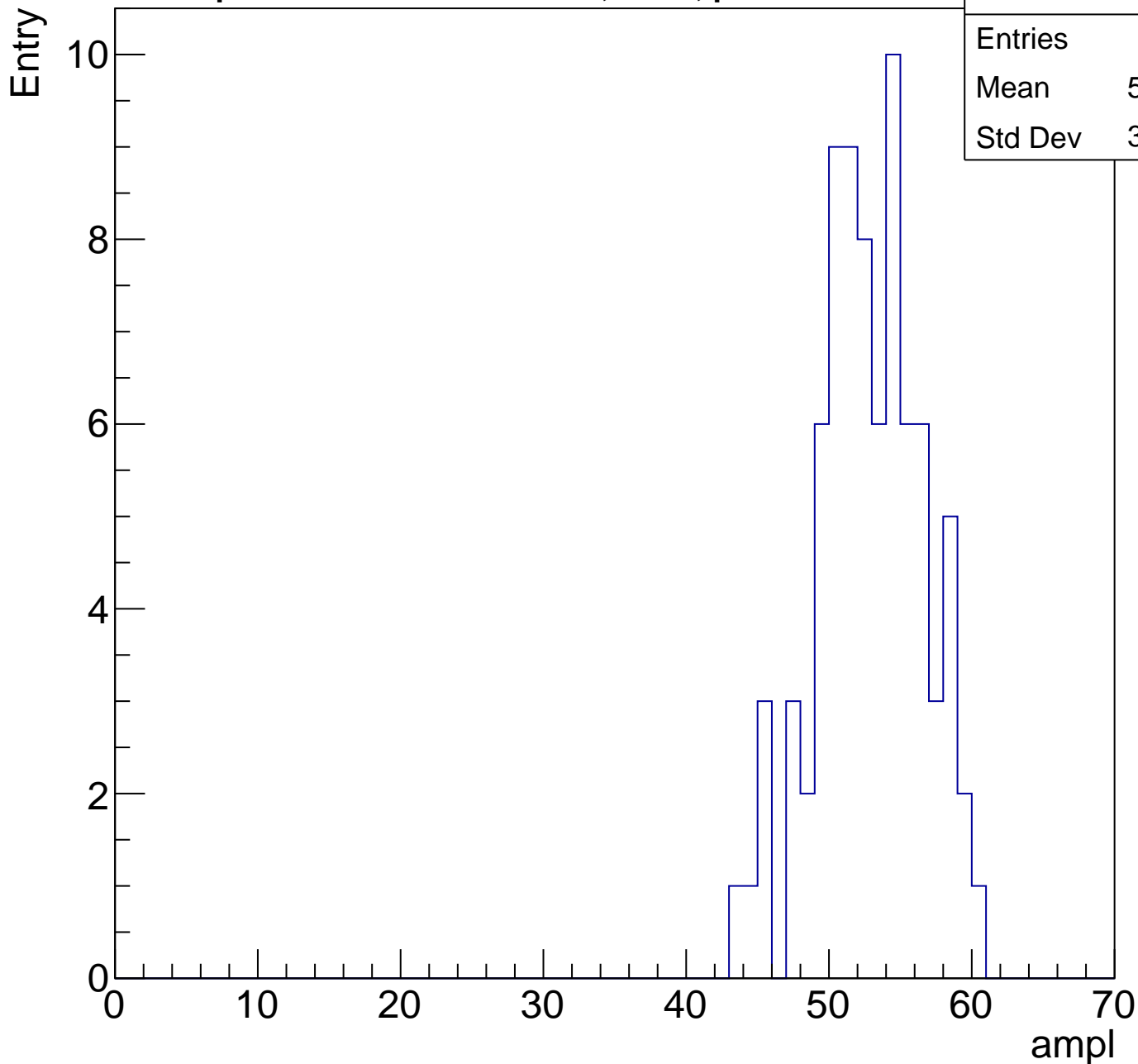
0 10 20 30 40 50 60 70



# B0L001S, U10-ch97, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	81
Mean	52.36
Std Dev	3.686

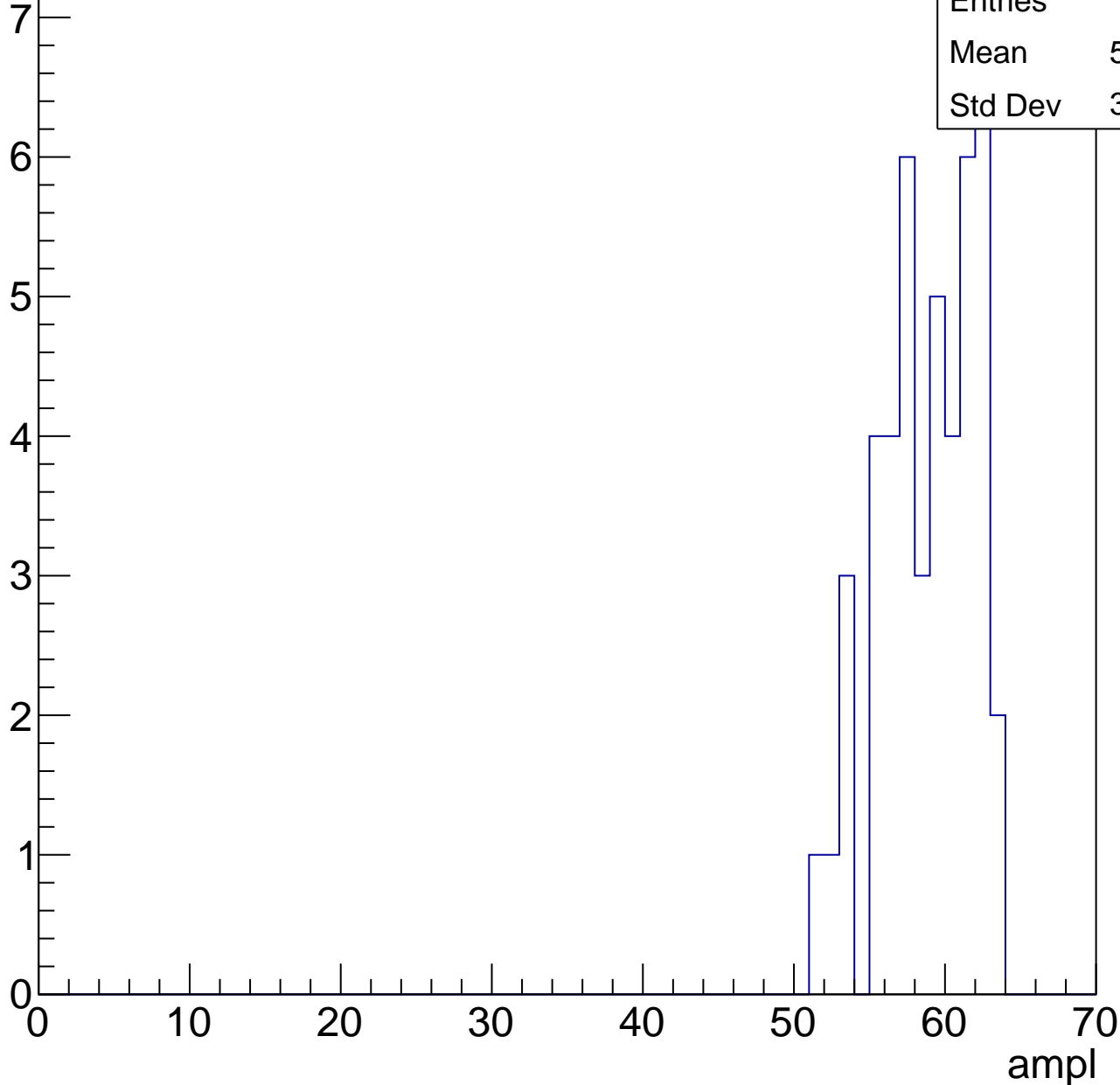


# B0L001S, U10-ch97, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	46
Mean	58.33
Std Dev	3.128

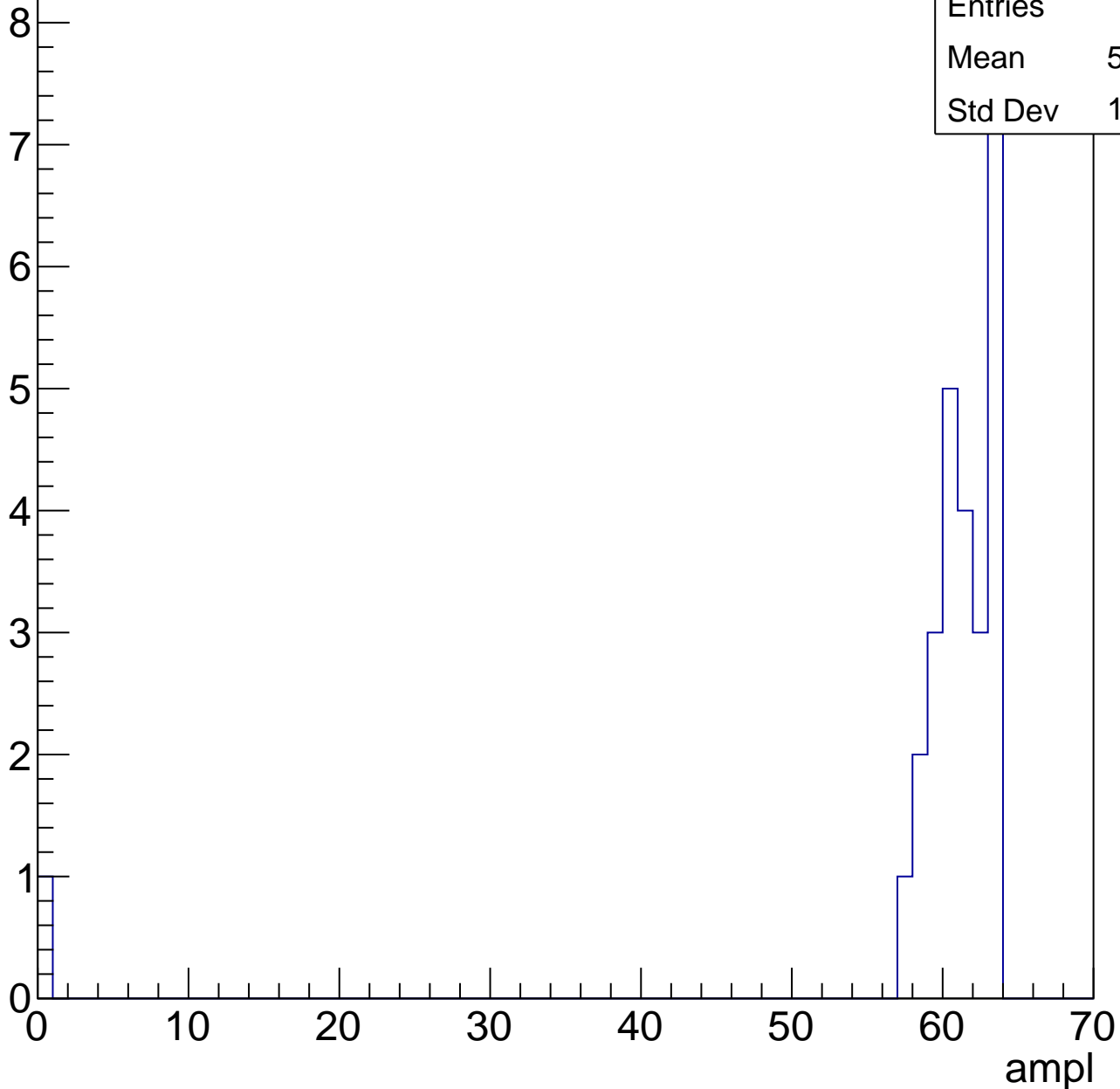


# B0L001S, U10-ch97, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	27
Mean	58.67
Std Dev	11.64



# B0L001S, U10-ch97, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U10-ch97, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U10-ch98, adc0

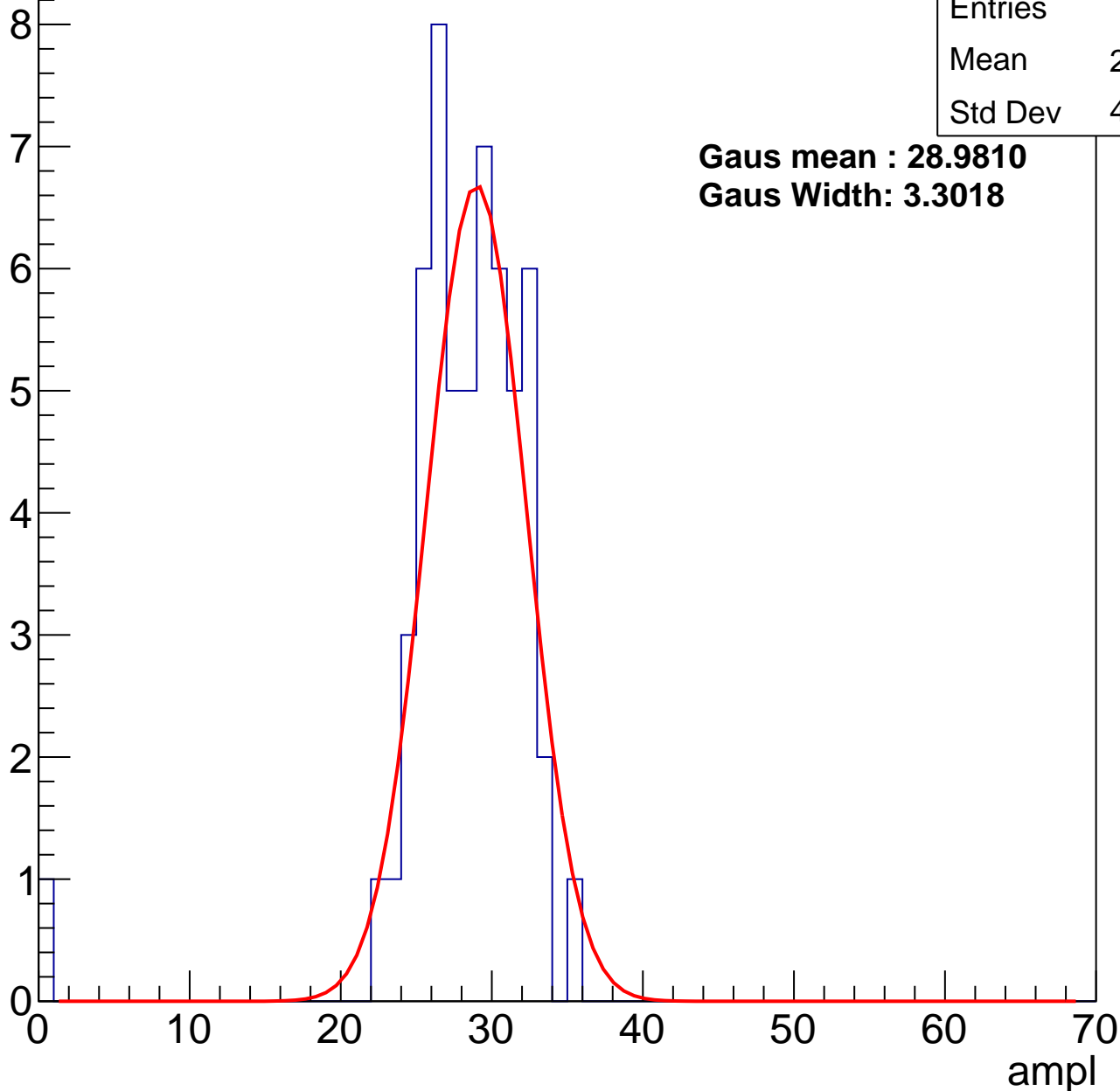
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	27.74
Std Dev	4.685

**Gaus mean : 28.9810**

**Gaus Width: 3.3018**



# B0L001S, U10-ch98, adc1

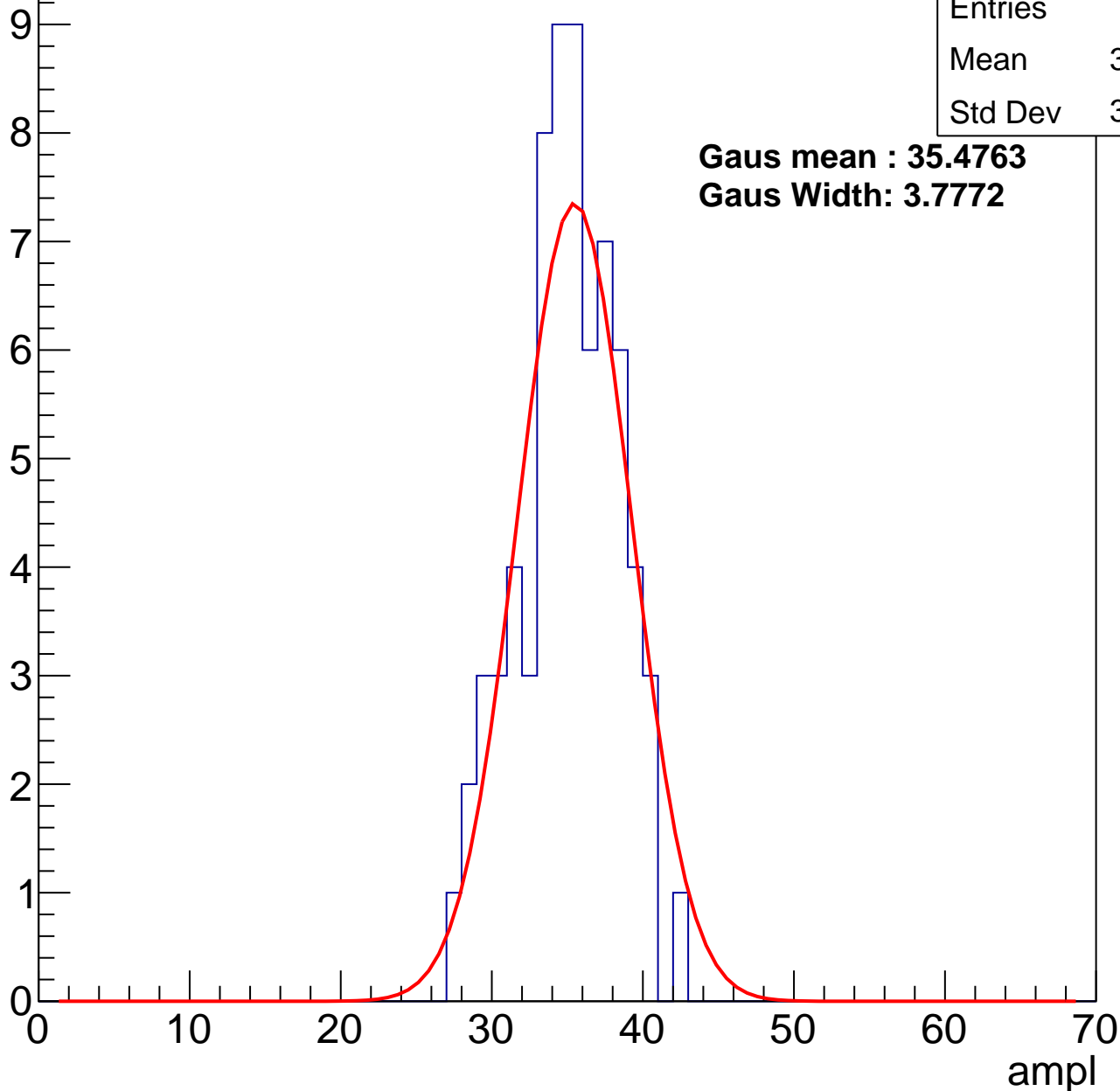
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	34.58
Std Dev	3.277

**Gaus mean : 35.4763**

**Gaus Width: 3.7772**



# B0L001S, U10-ch98, adc2

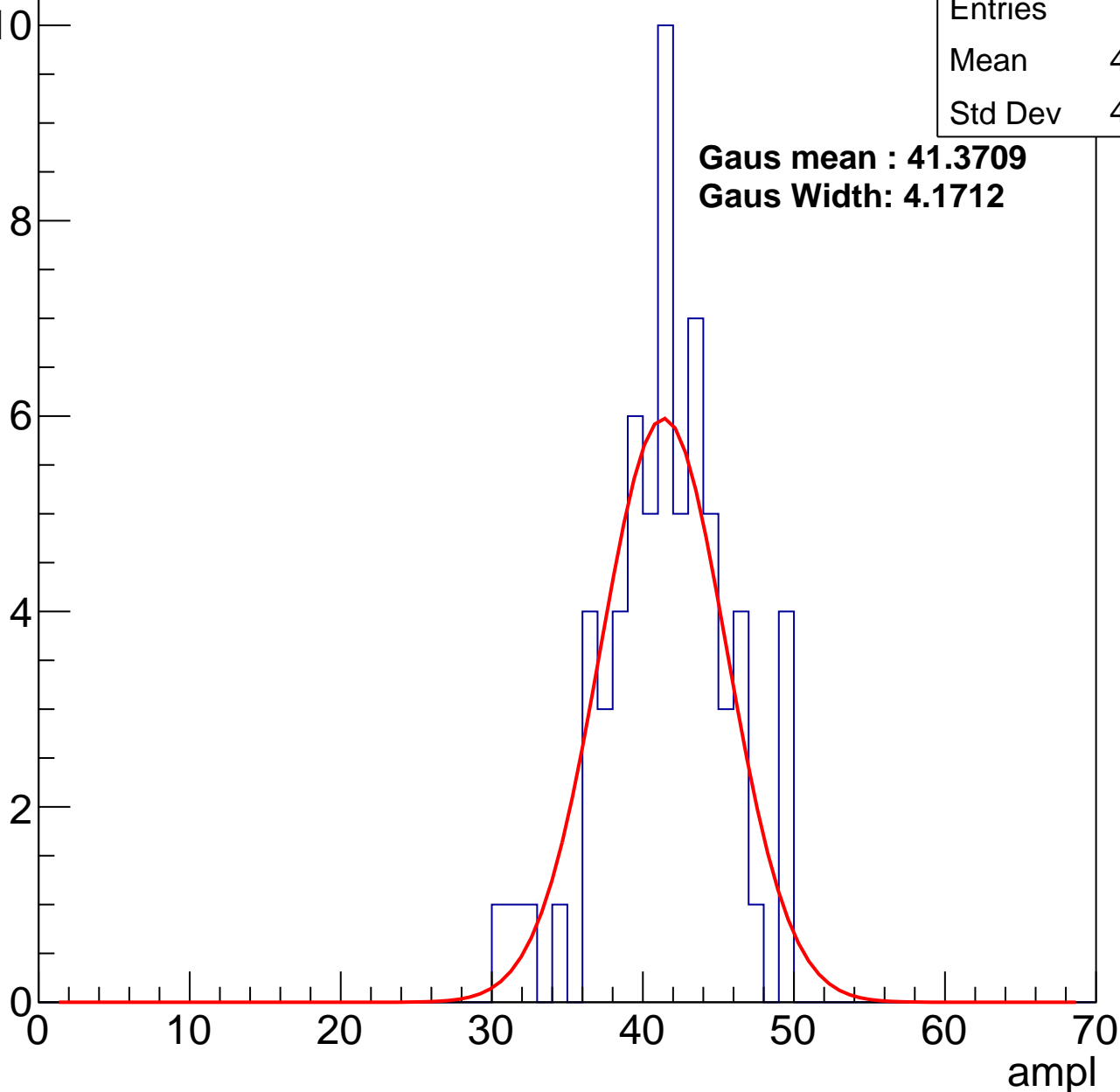
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	41.09
Std Dev	4.079

**Gaus mean : 41.3709**

**Gaus Width: 4.1712**

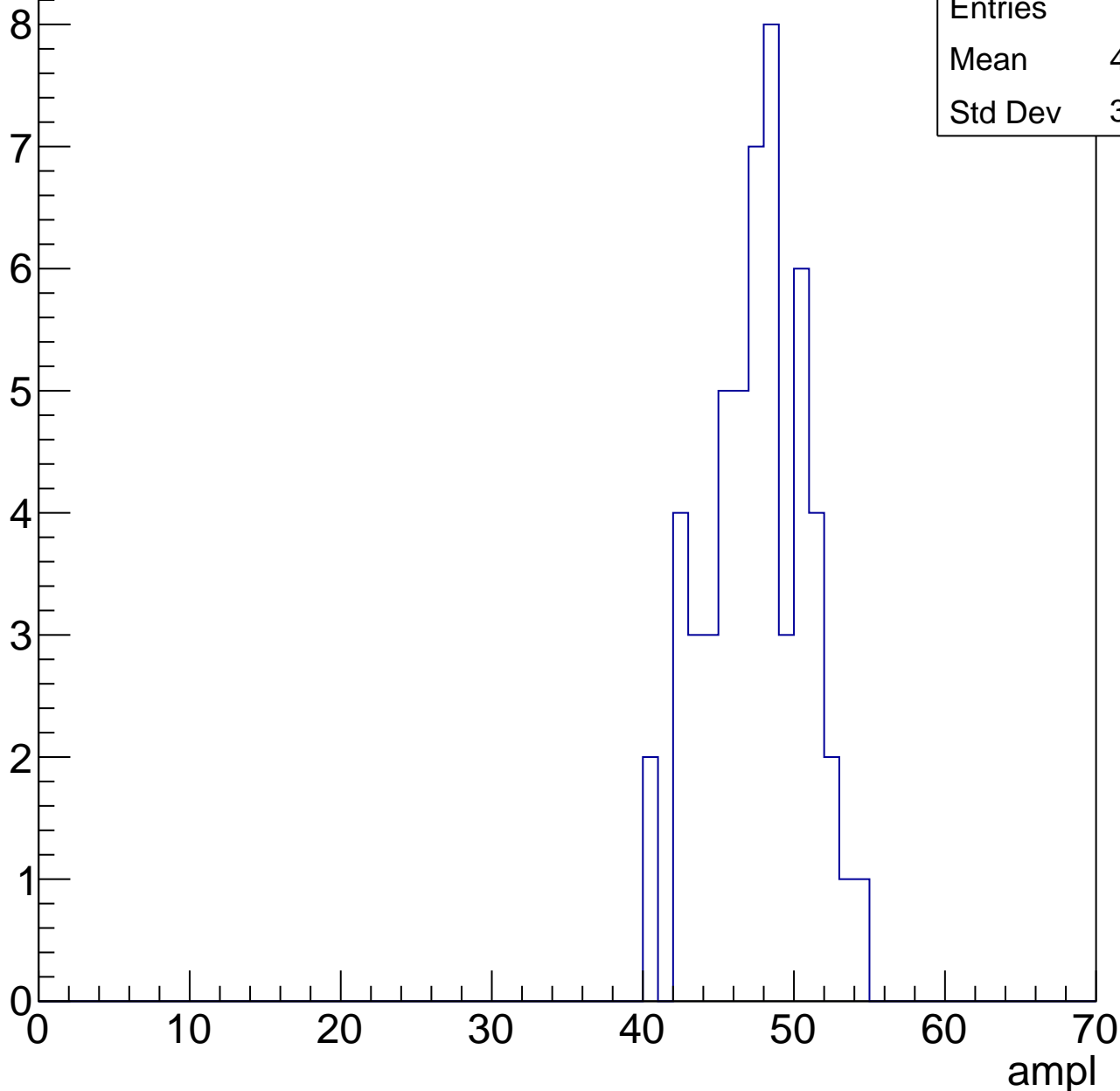


# B0L001S, U10-ch98, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	47.02
Std Dev	3.252

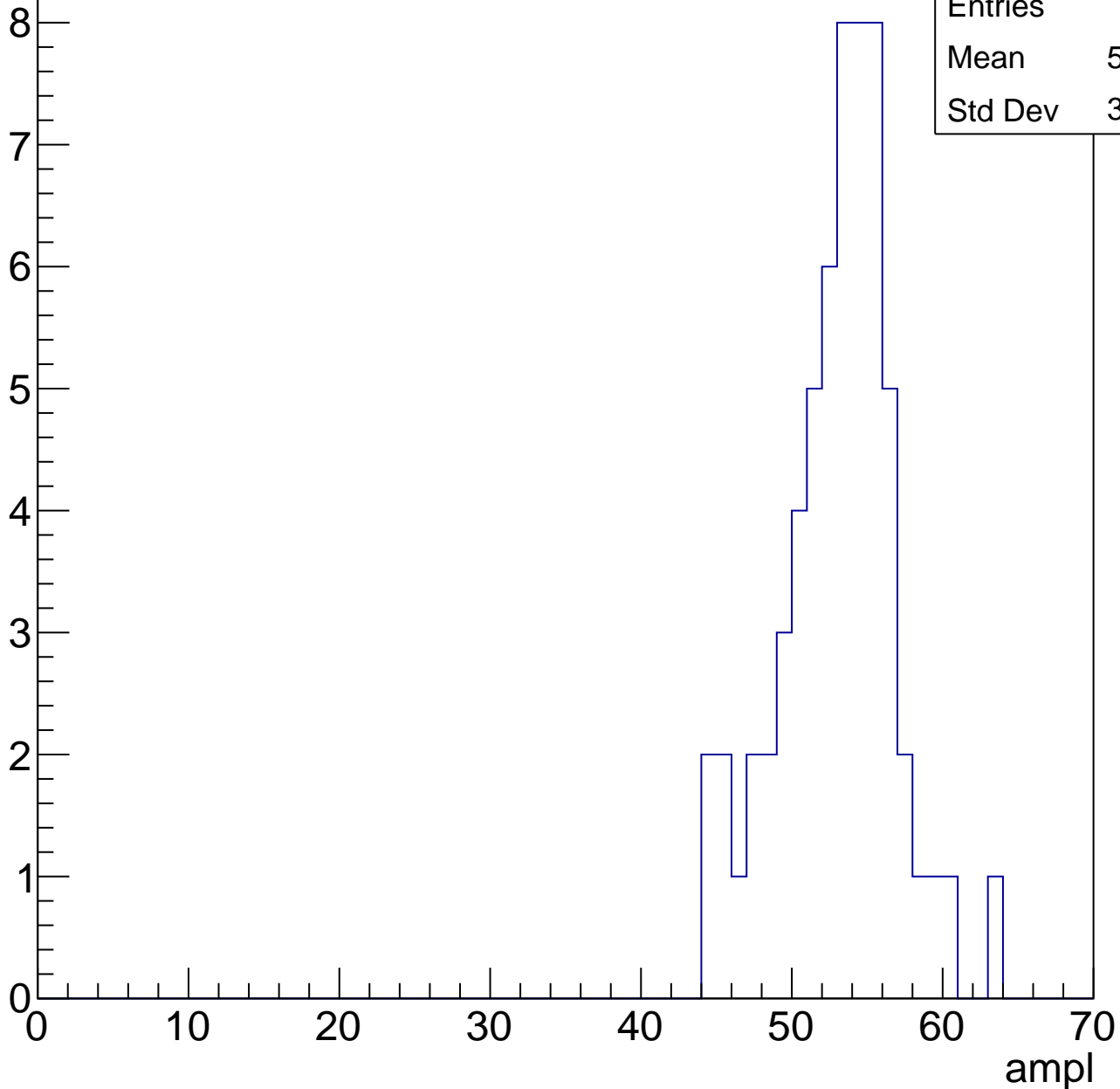


# B0L001S, U10-ch98, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	52.55
Std Dev	3.779



# B0L001S, U10-ch98, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

10

Entries 65

Mean 58.65

Std Dev 2.726

8

6

4

2

0

0

10

20

30

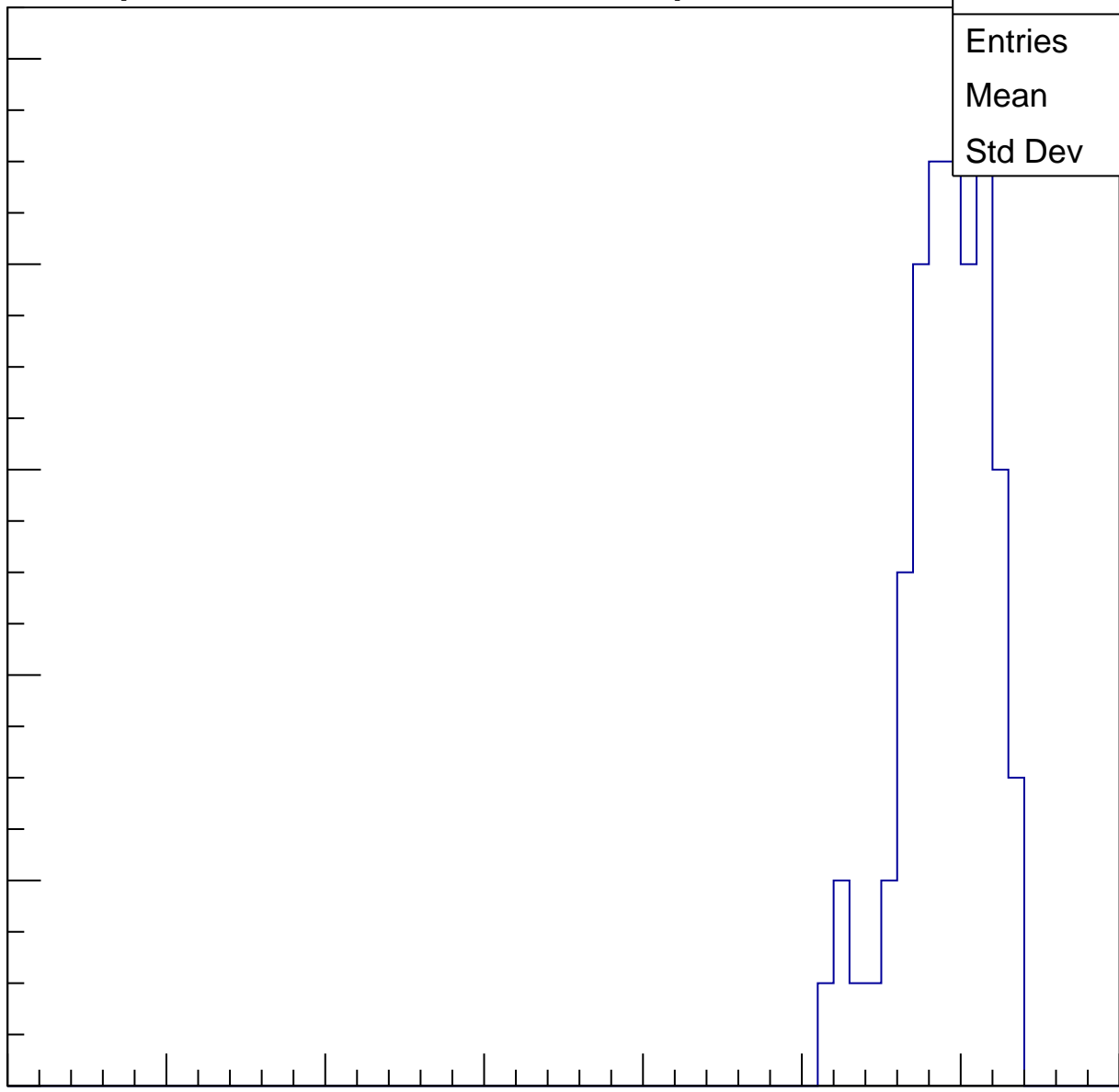
40

50

60

70

ampl

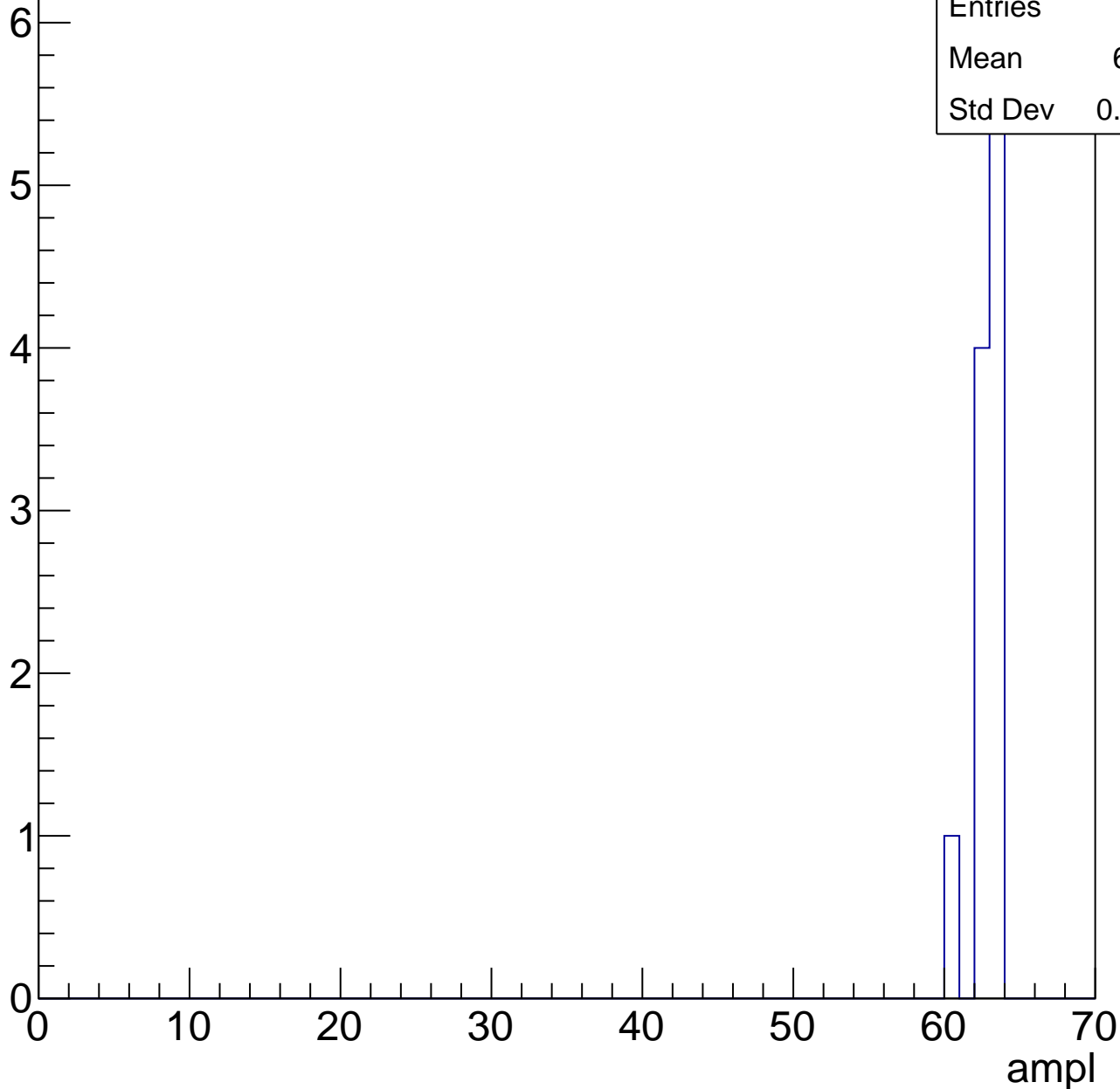


# B0L001S, U10-ch98, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	11
Mean	62.36
Std Dev	0.8814





# B0L001S, U10-ch98, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	10.5
Std Dev	10.5

# B0L001S, U10-ch99, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	90
Mean	28.92
Std Dev	7.103

**Gaus mean : 31.4113**

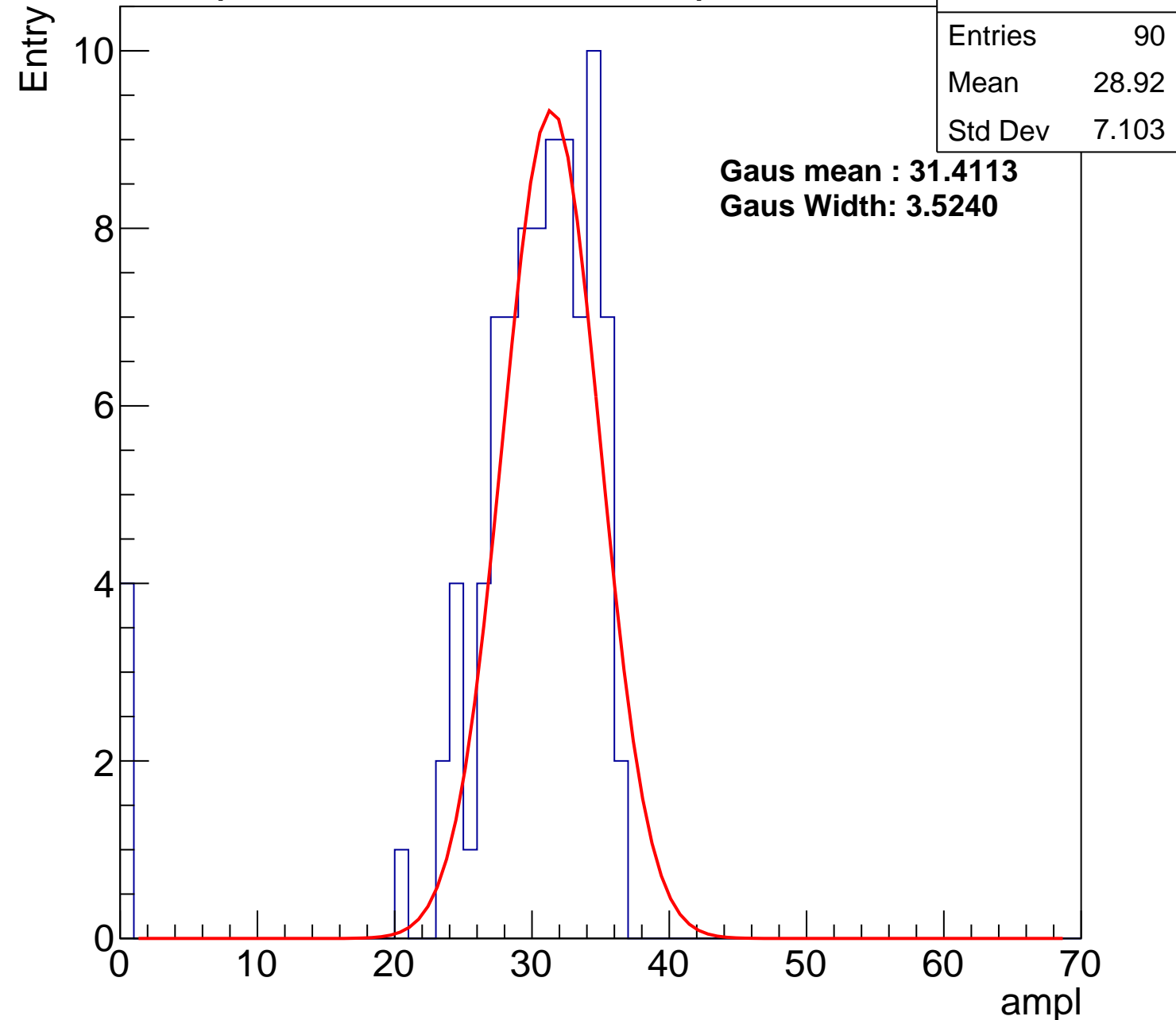
**Gaus Width: 3.5240**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U10-ch99, adc1

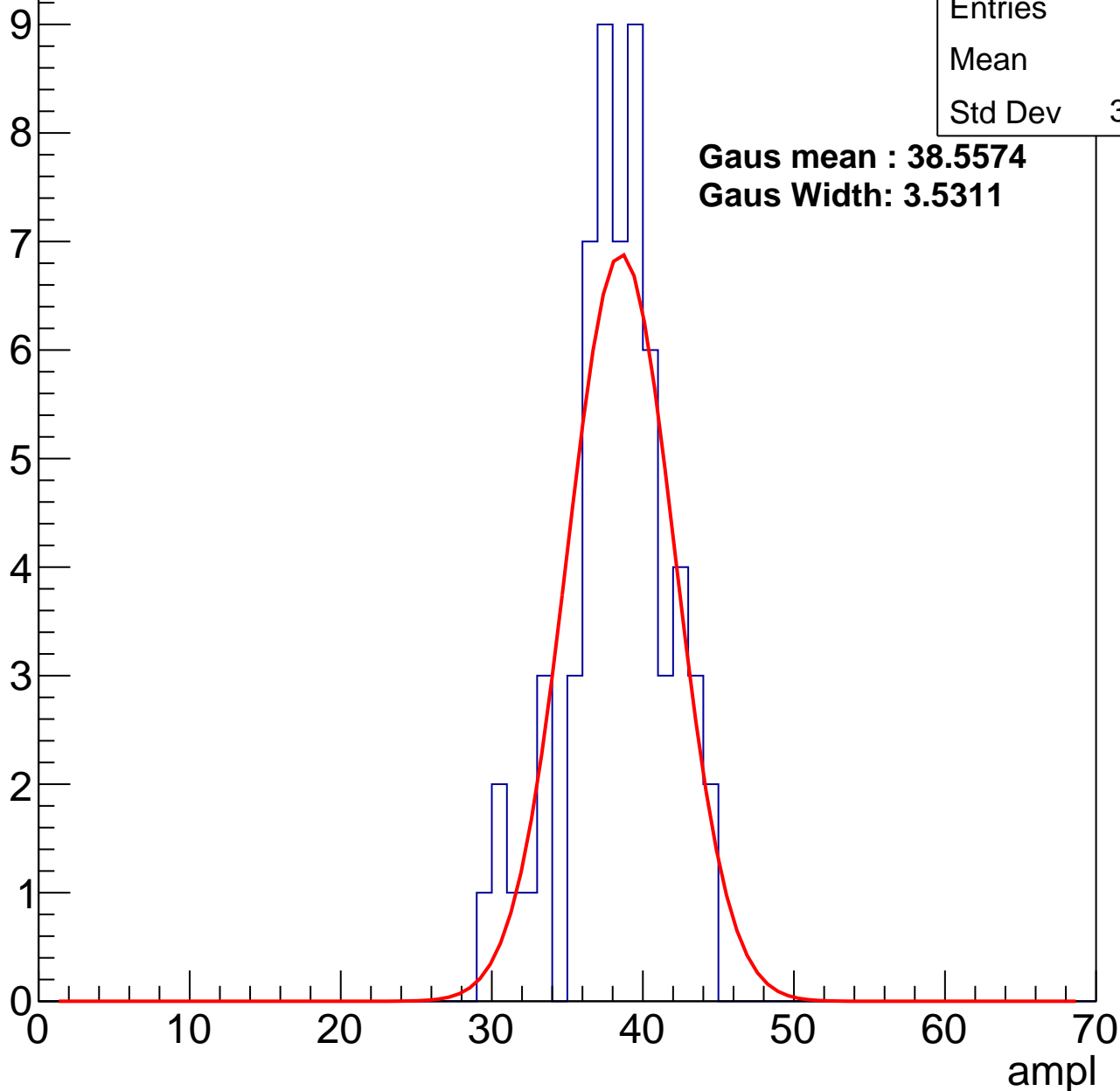
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	37.8
Std Dev	3.392

**Gaus mean : 38.5574**

**Gaus Width: 3.5311**

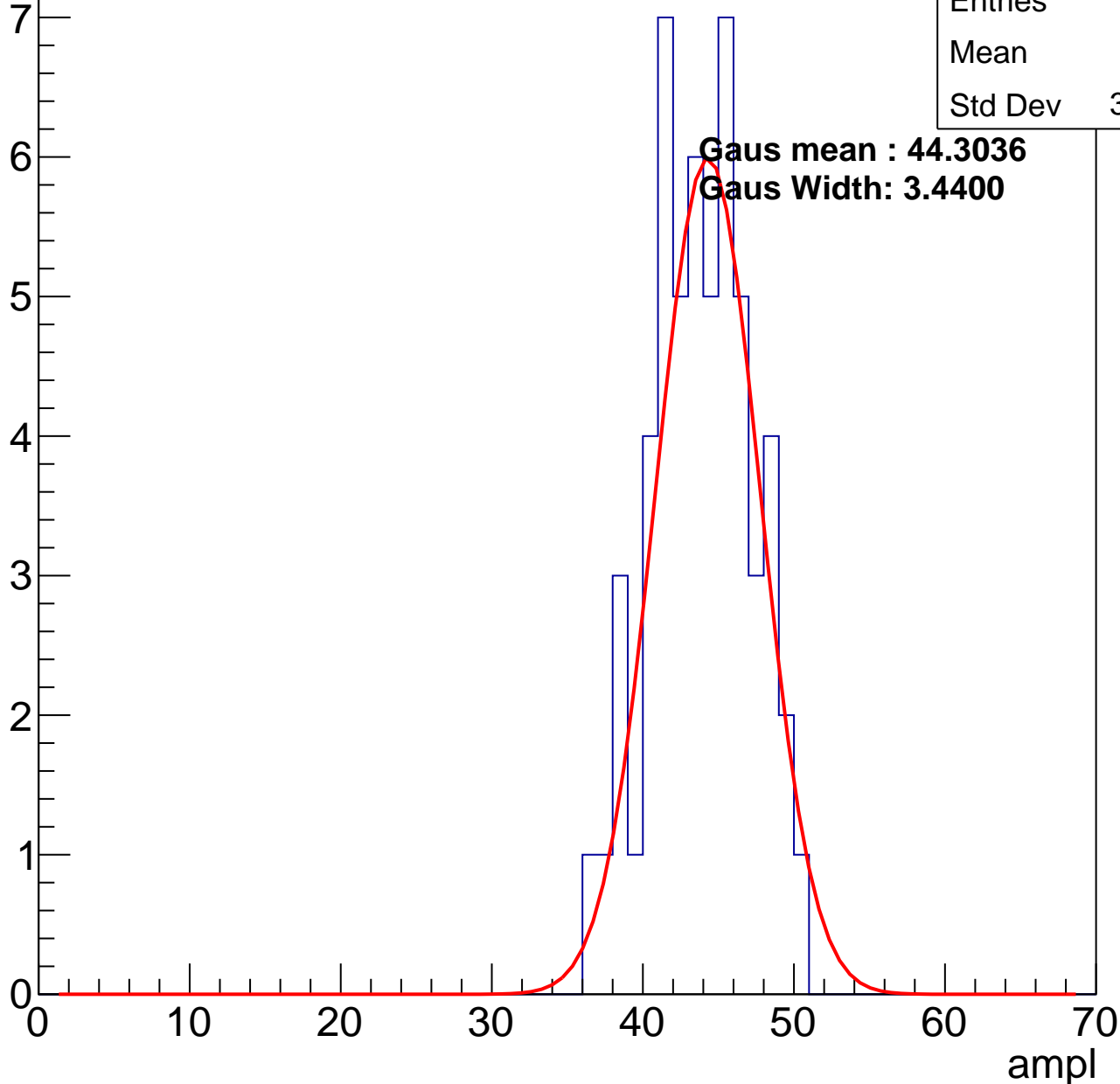


# B0L001S, U10-ch99, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	43.4
Std Dev	3.256

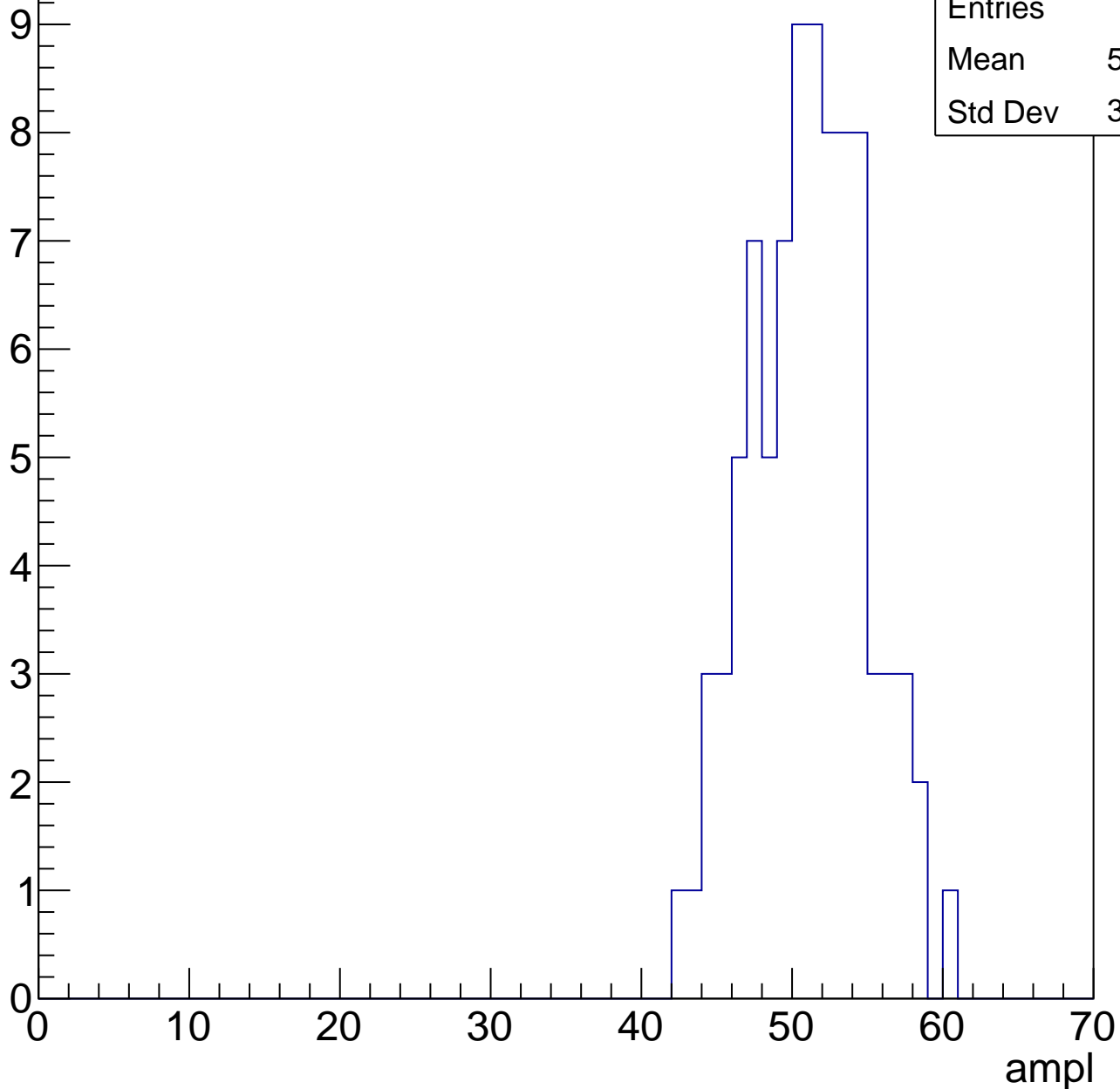


# B0L001S, U10-ch99, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	86
Mean	50.64
Std Dev	3.782

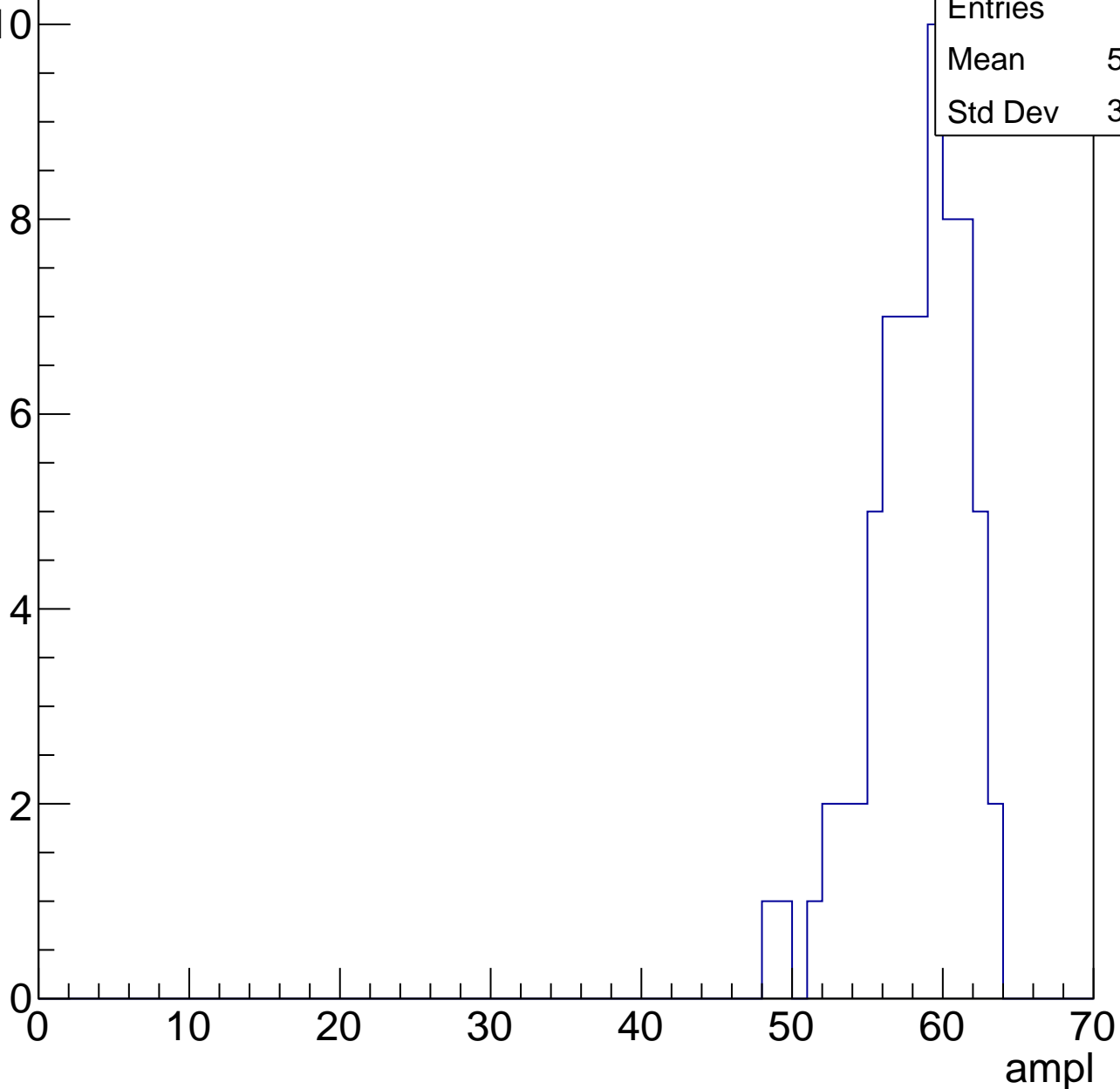


# B0L001S, U10-ch99, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	57.82
Std Dev	3.222

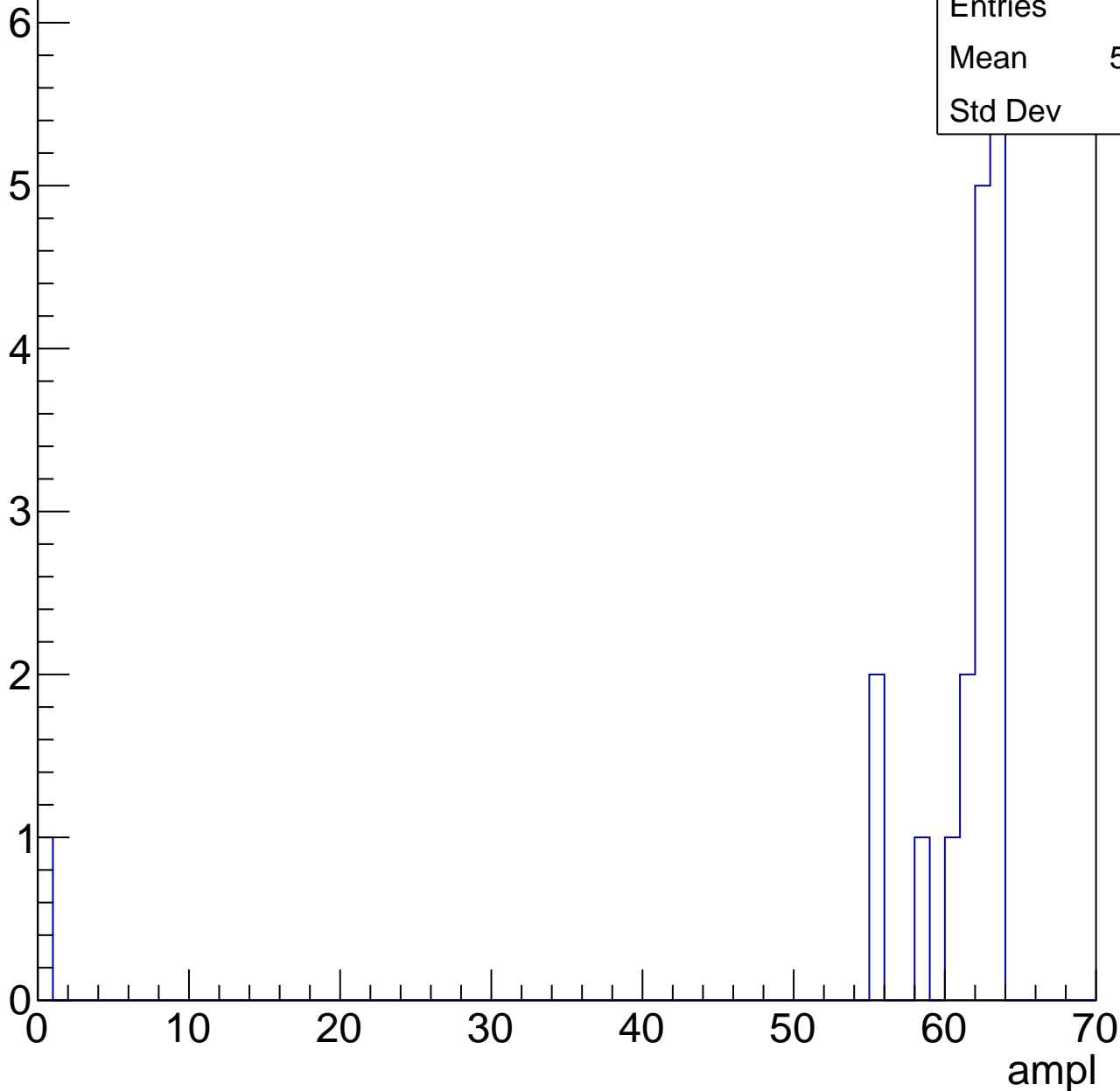


# B0L001S, U10-ch99, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	18
Mean	57.67
Std Dev	14.2



# B0L001S, U10-ch99, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch99, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L001S, U10-ch100, adc0

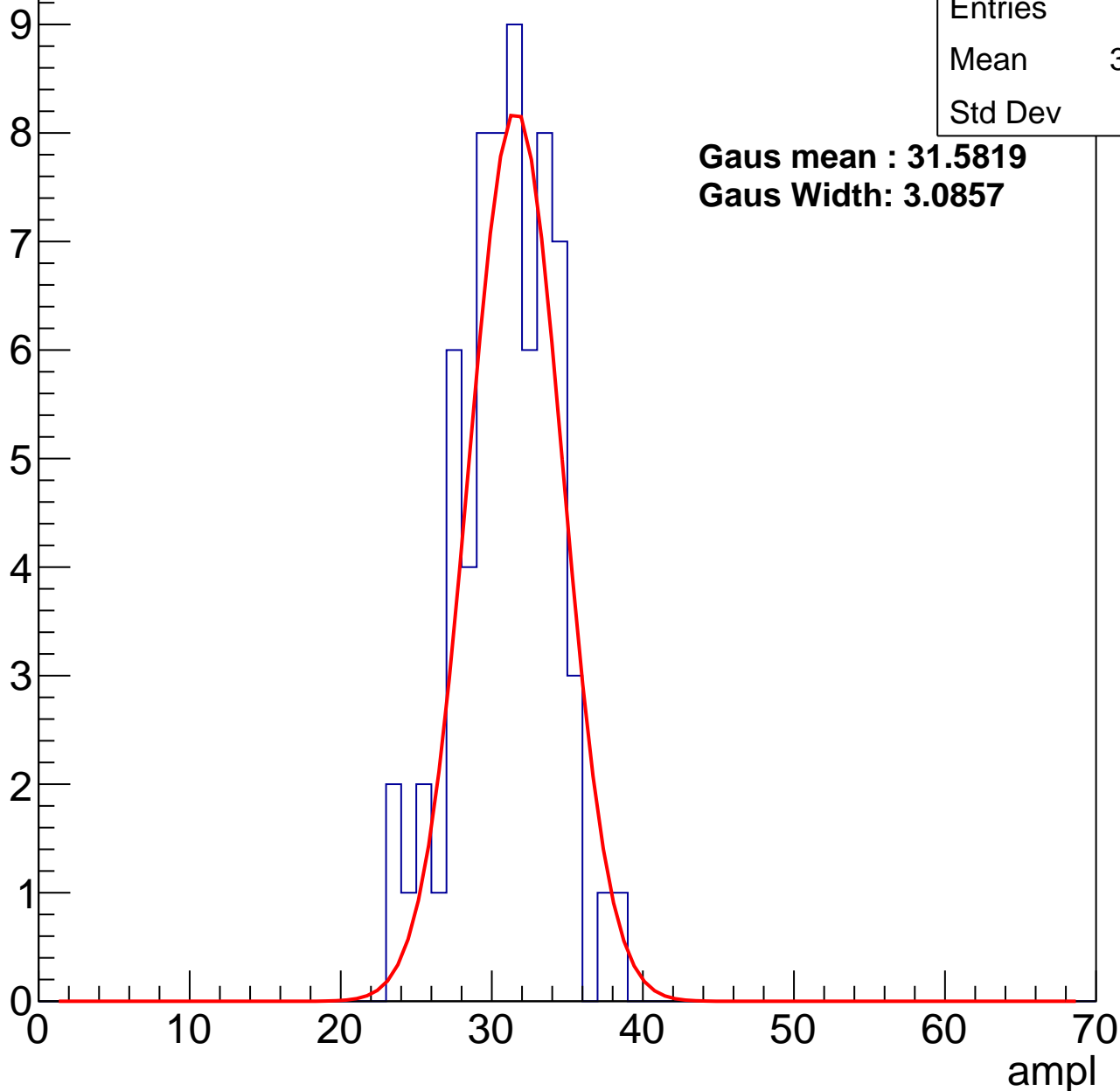
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	30.52
Std Dev	3.15

**Gaus mean : 31.5819**

**Gaus Width: 3.0857**



# B0L001S, U10-ch100, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	65
Mean	37.55
Std Dev	3.31

**Gaus mean : 37.8673**

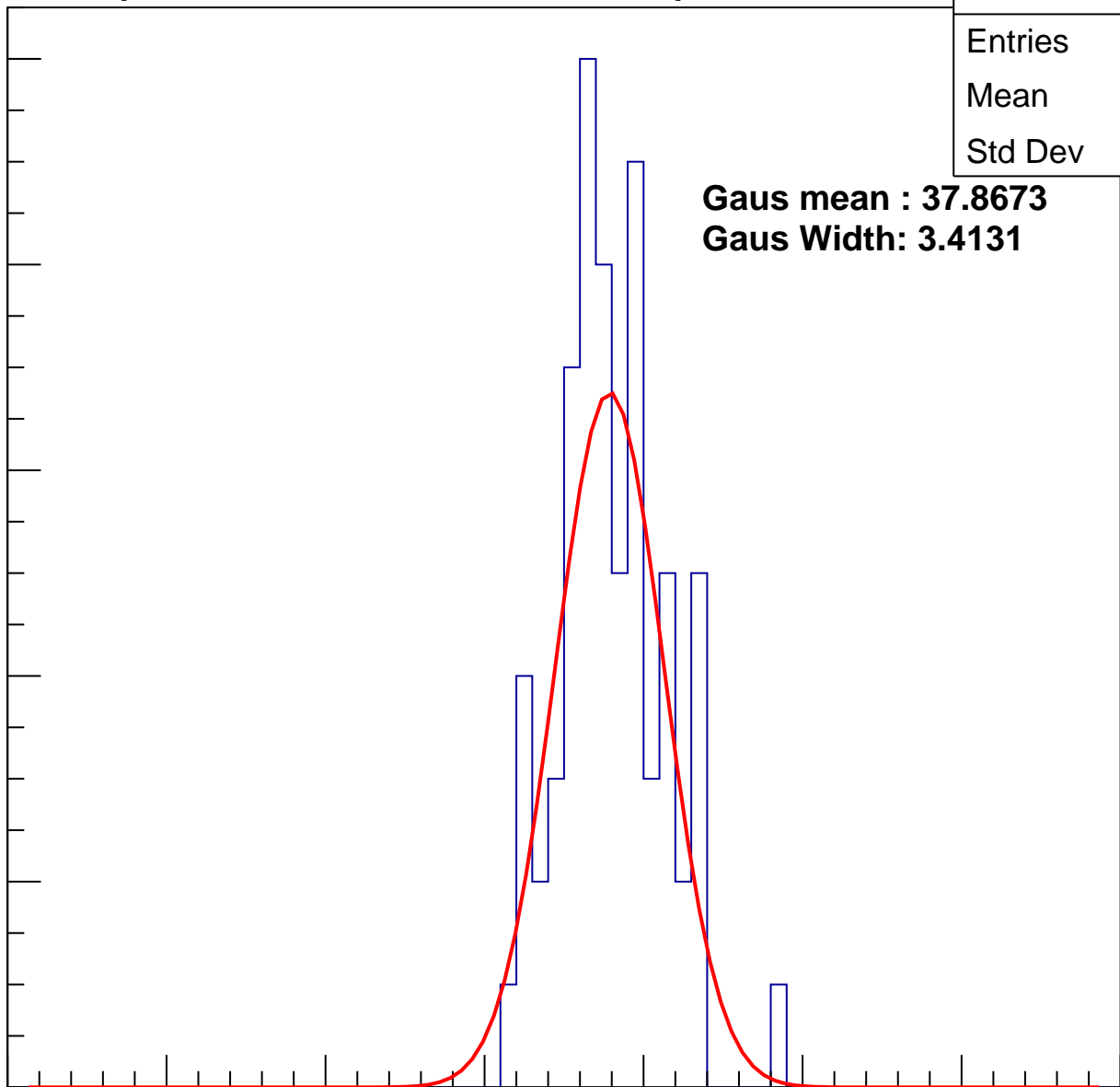
**Gaus Width: 3.4131**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B0L001S, U10-ch100, adc2

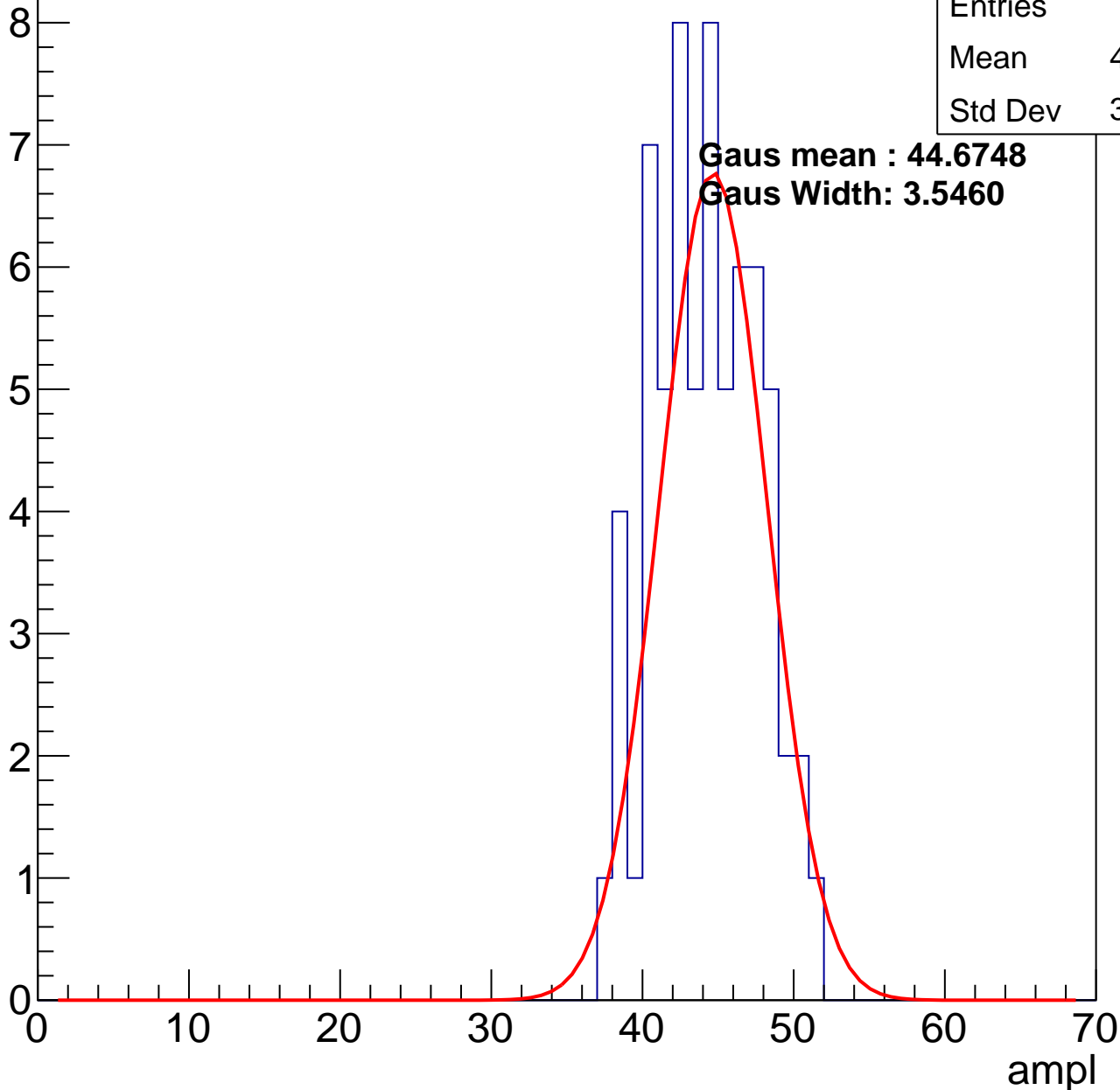
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	43.76
Std Dev	3.353

**Gaus mean : 44.6748**

**Gaus Width: 3.5460**

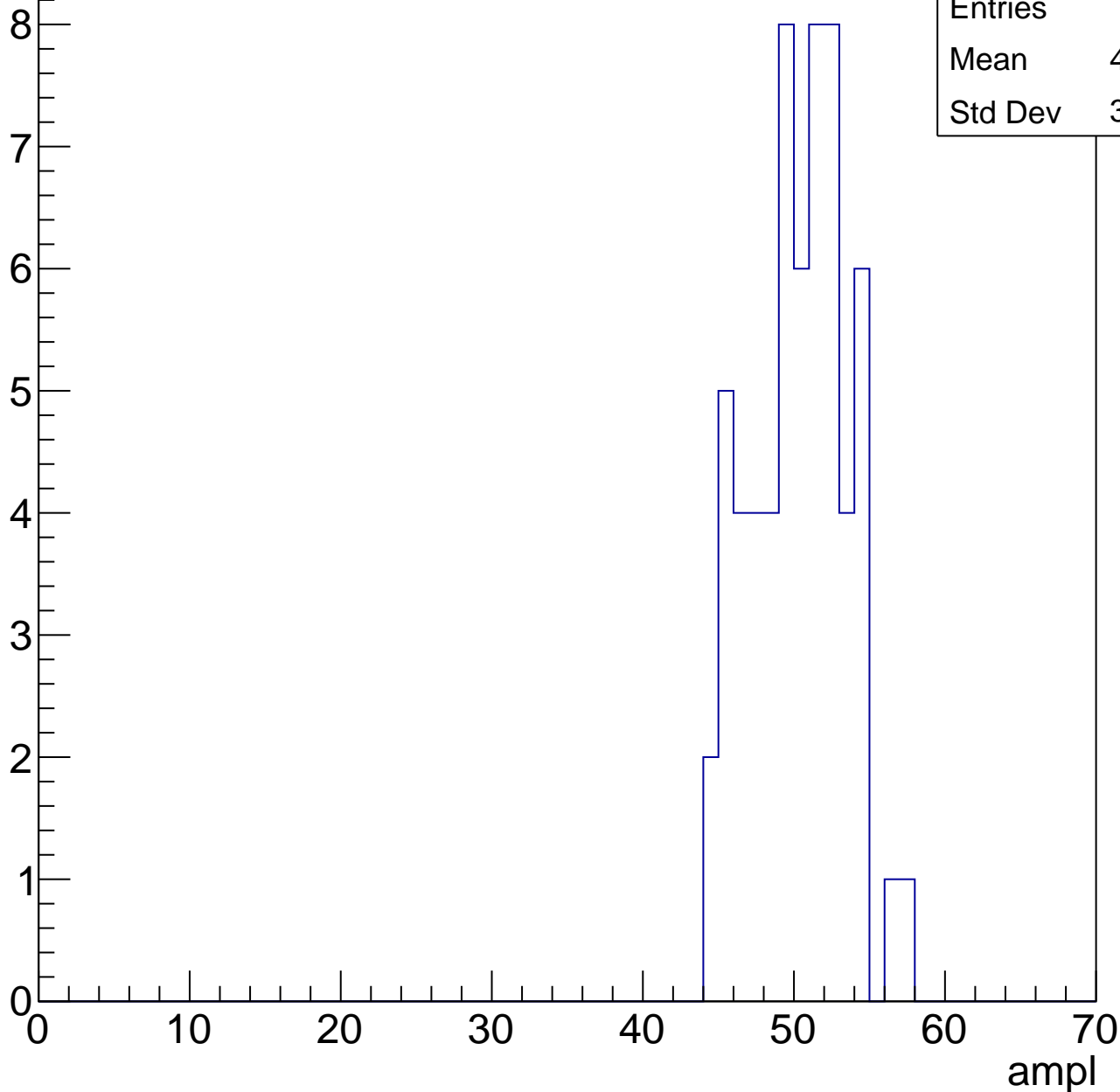


# B0L001S, U10-ch100, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	49.87
Std Dev	3.075

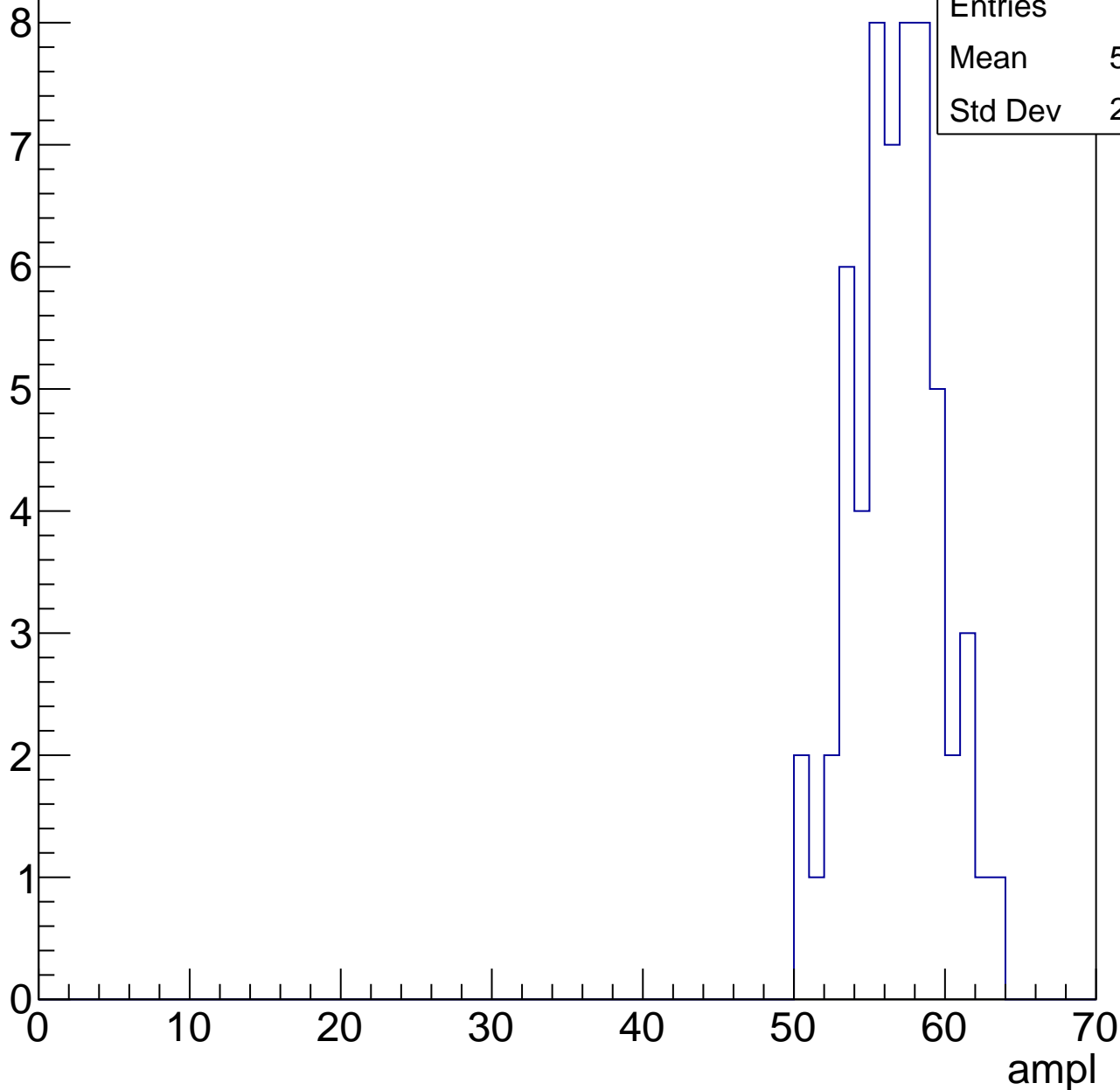


# B0L001S, U10-ch100, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

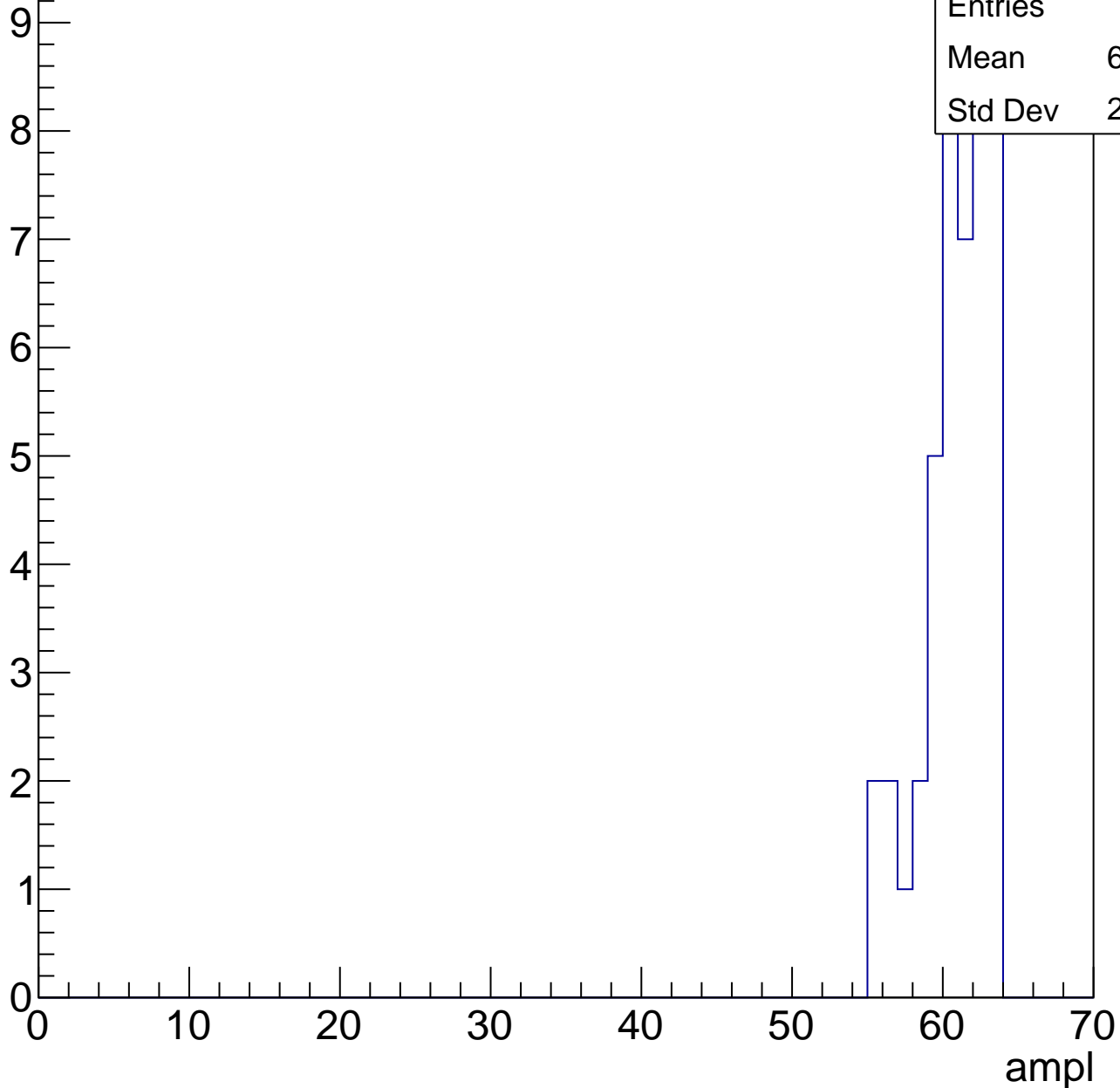
Entries	58
Mean	56.28
Std Dev	2.876



# B0L001S, U10-ch100, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U10-ch100, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch100, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L001S, U10-ch101, adc0

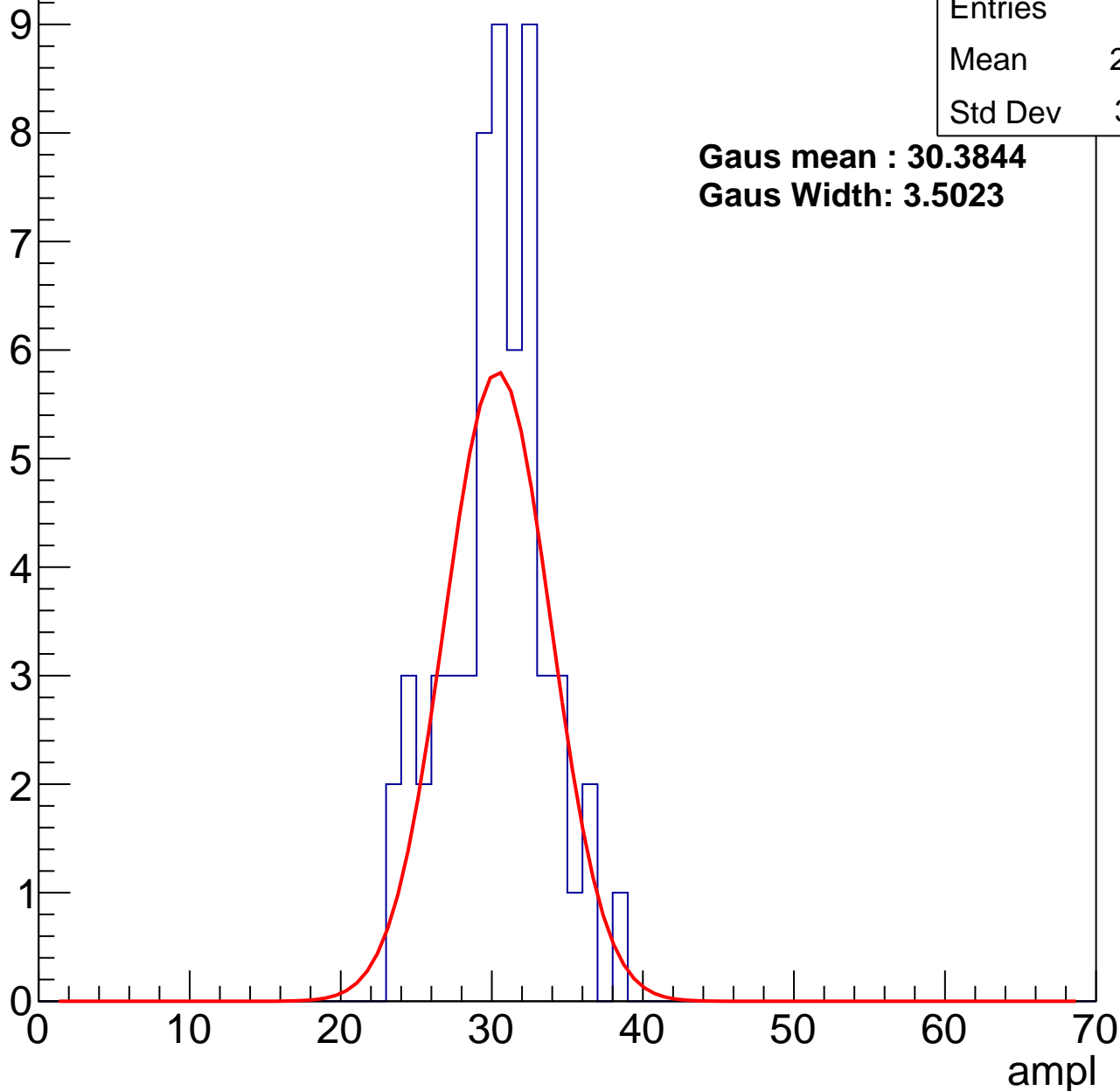
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	29.88
Std Dev	3.291

**Gaus mean : 30.3844**

**Gaus Width: 3.5023**



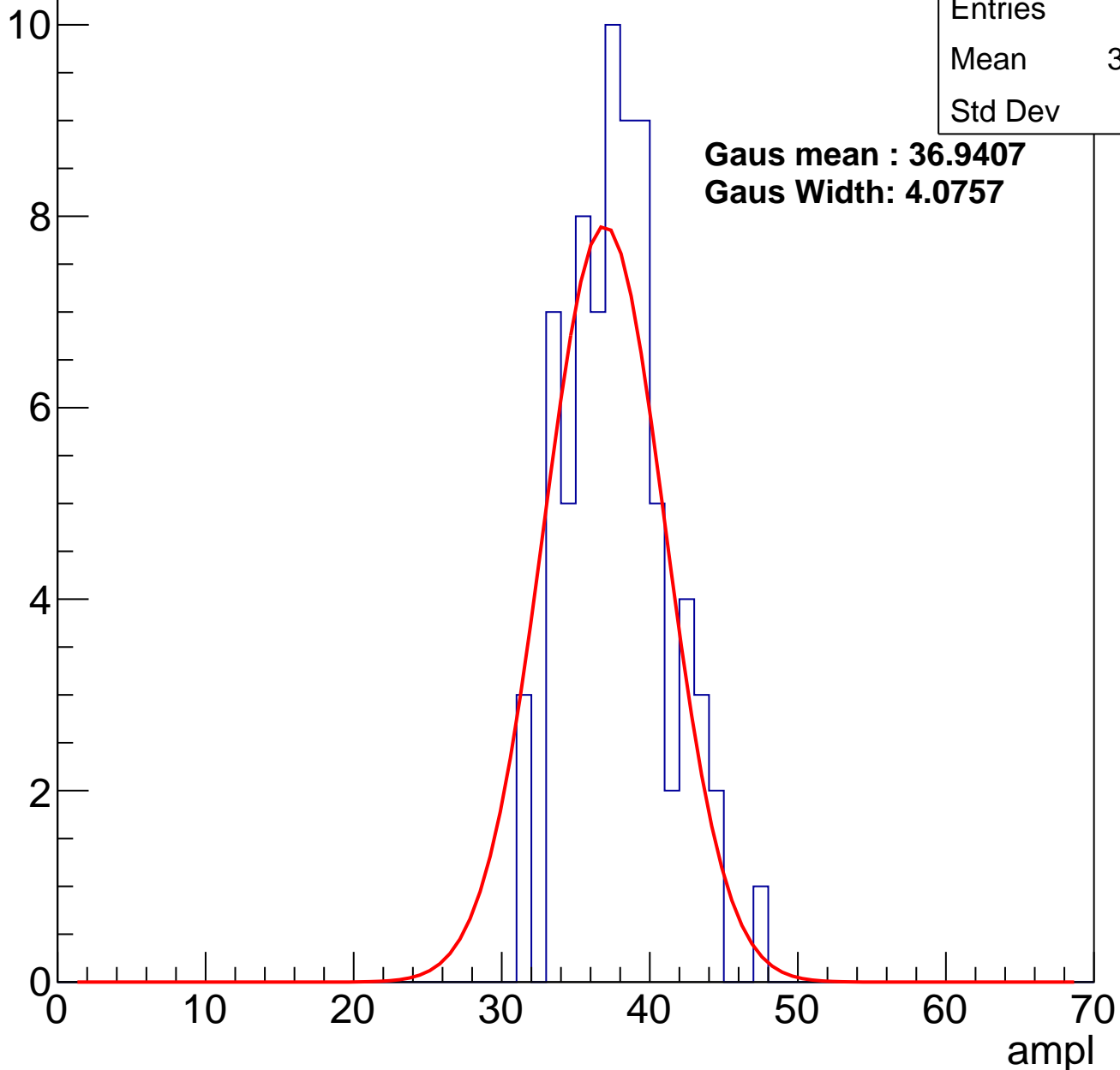
# B0L001S, U10-ch101, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	75
Mean	37.37
Std Dev	3.31

**Gaus mean : 36.9407**  
**Gaus Width: 4.0757**

Entry



# B0L001S, U10-ch101, adc2

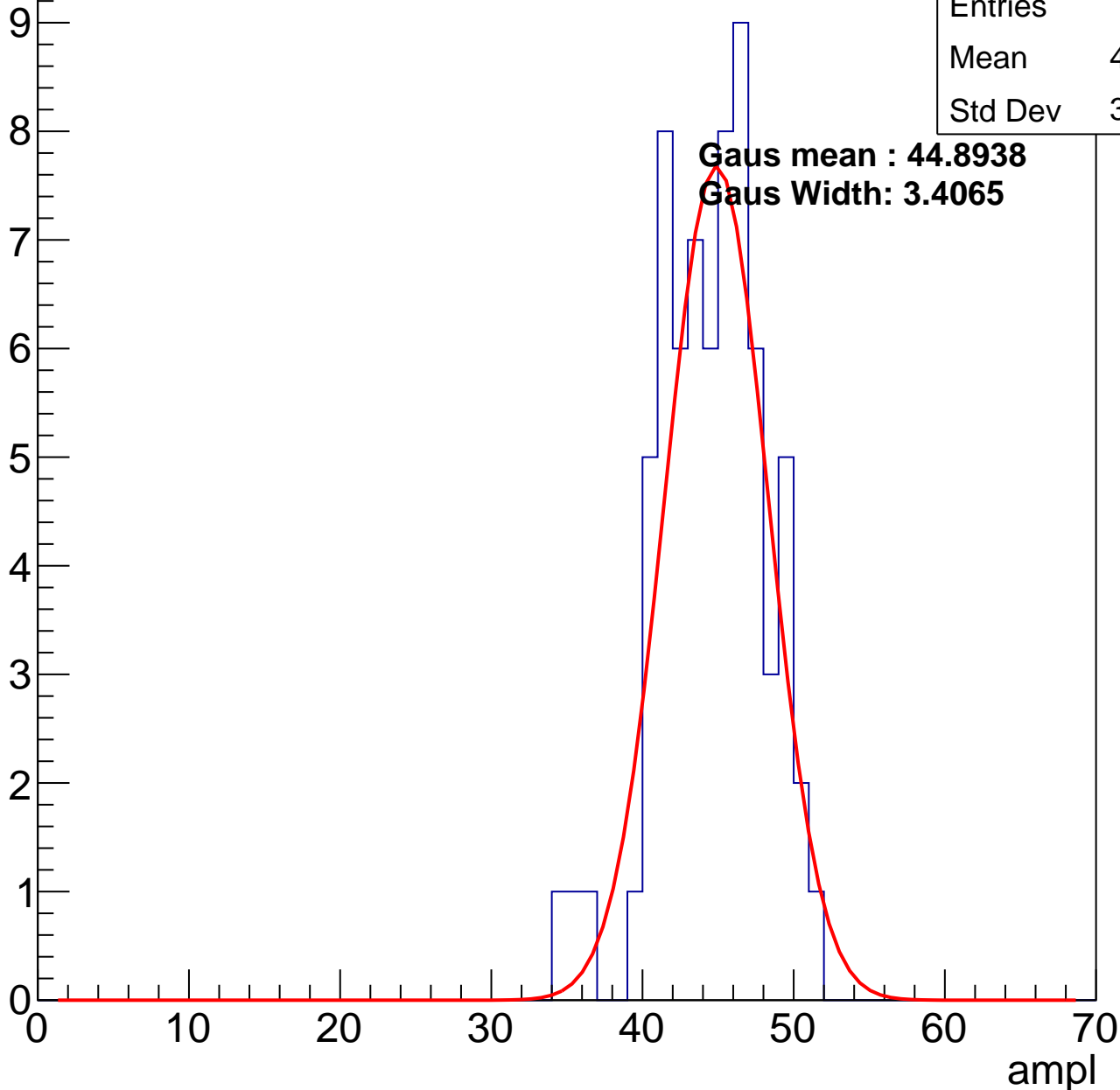
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	44.07
Std Dev	3.474

**Gaus mean : 44.8938**

**Gaus Width: 3.4065**

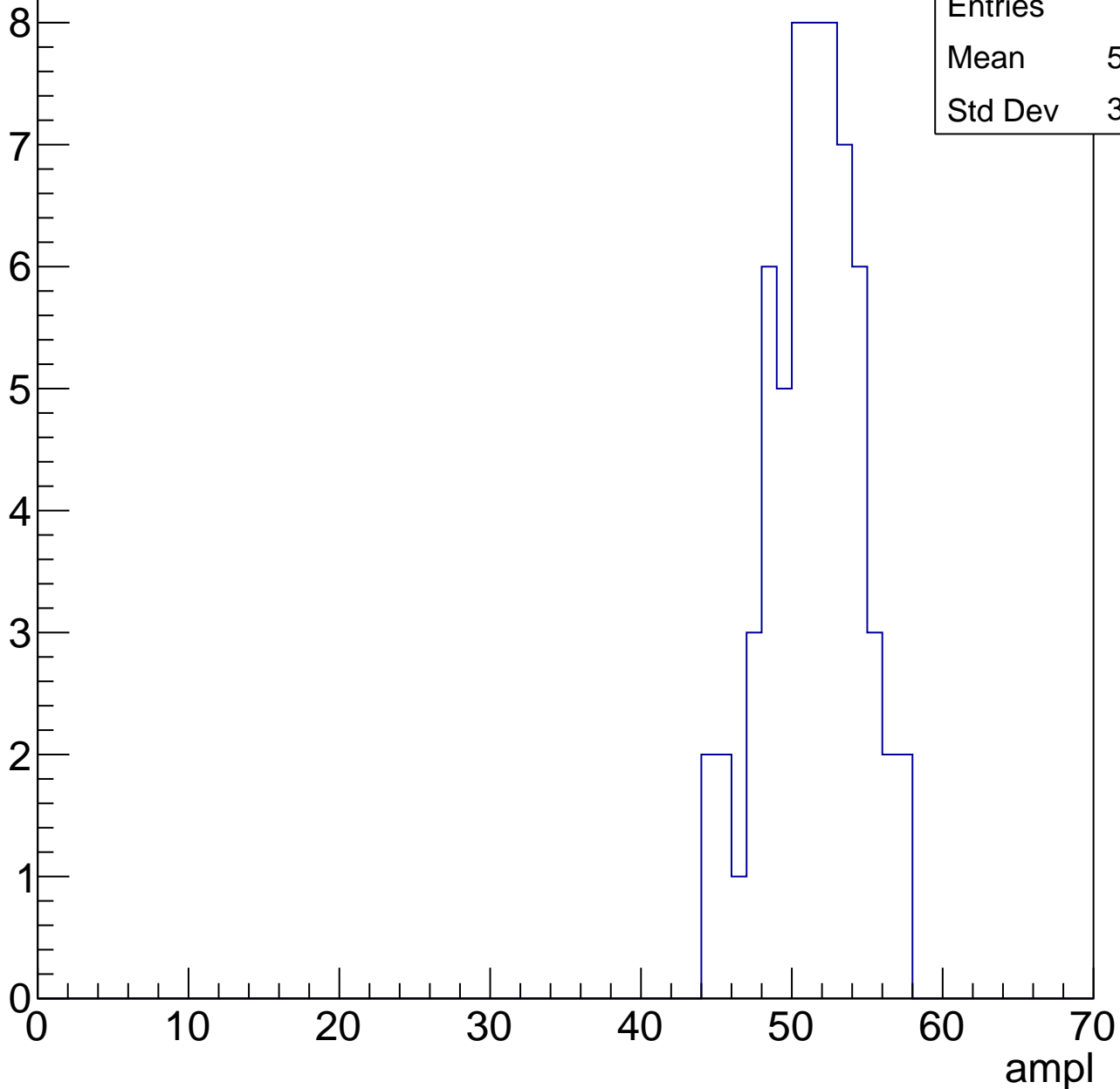


# B0L001S, U10-ch101, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	50.92
Std Dev	3.046

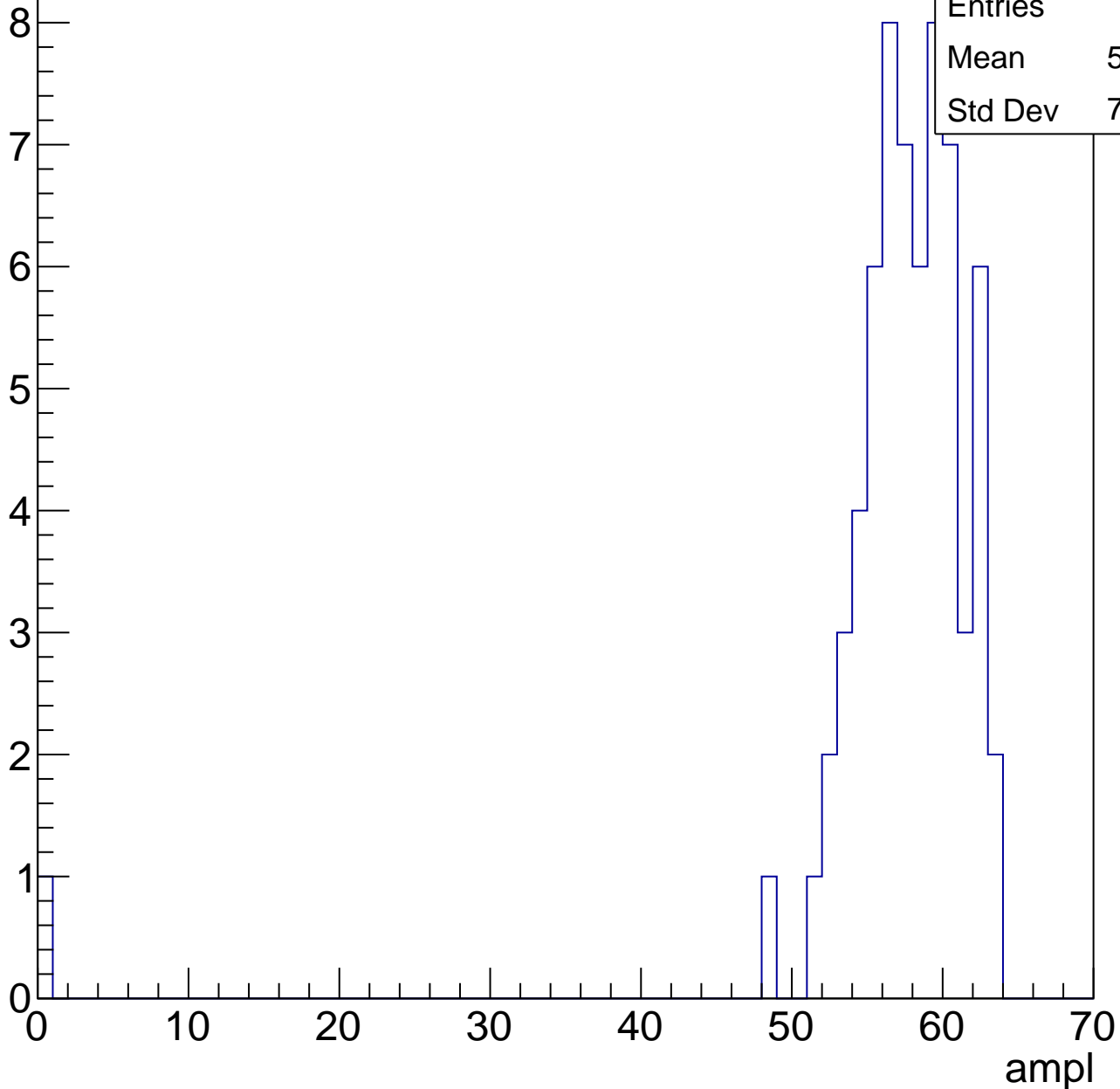


# B0L001S, U10-ch101, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	56.55
Std Dev	7.736

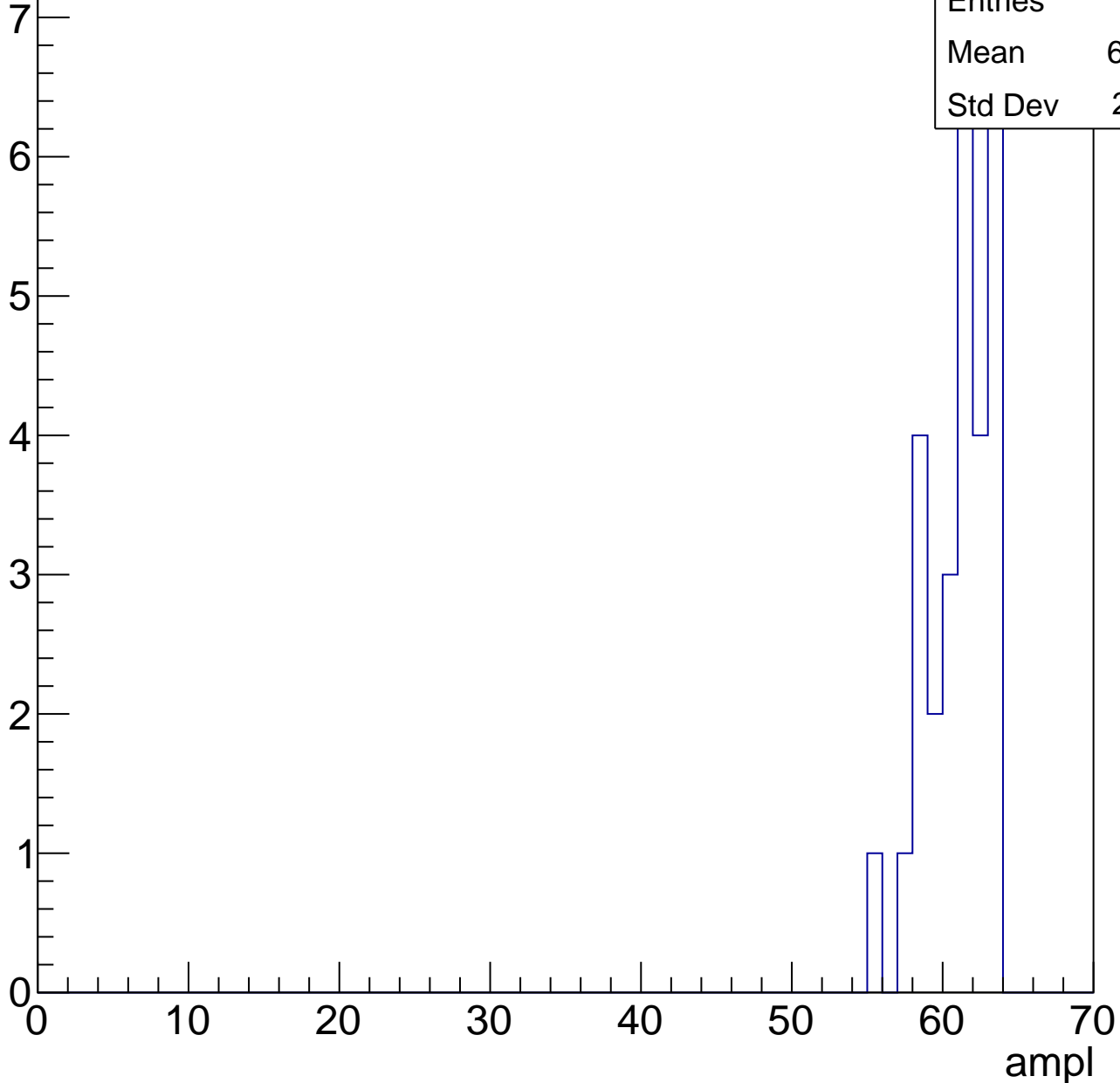


# B0L001S, U10-ch101, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	29
Mean	60.62
Std Dev	2.091



# B0L001S, U10-ch101, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch101, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U10-ch102, adc0

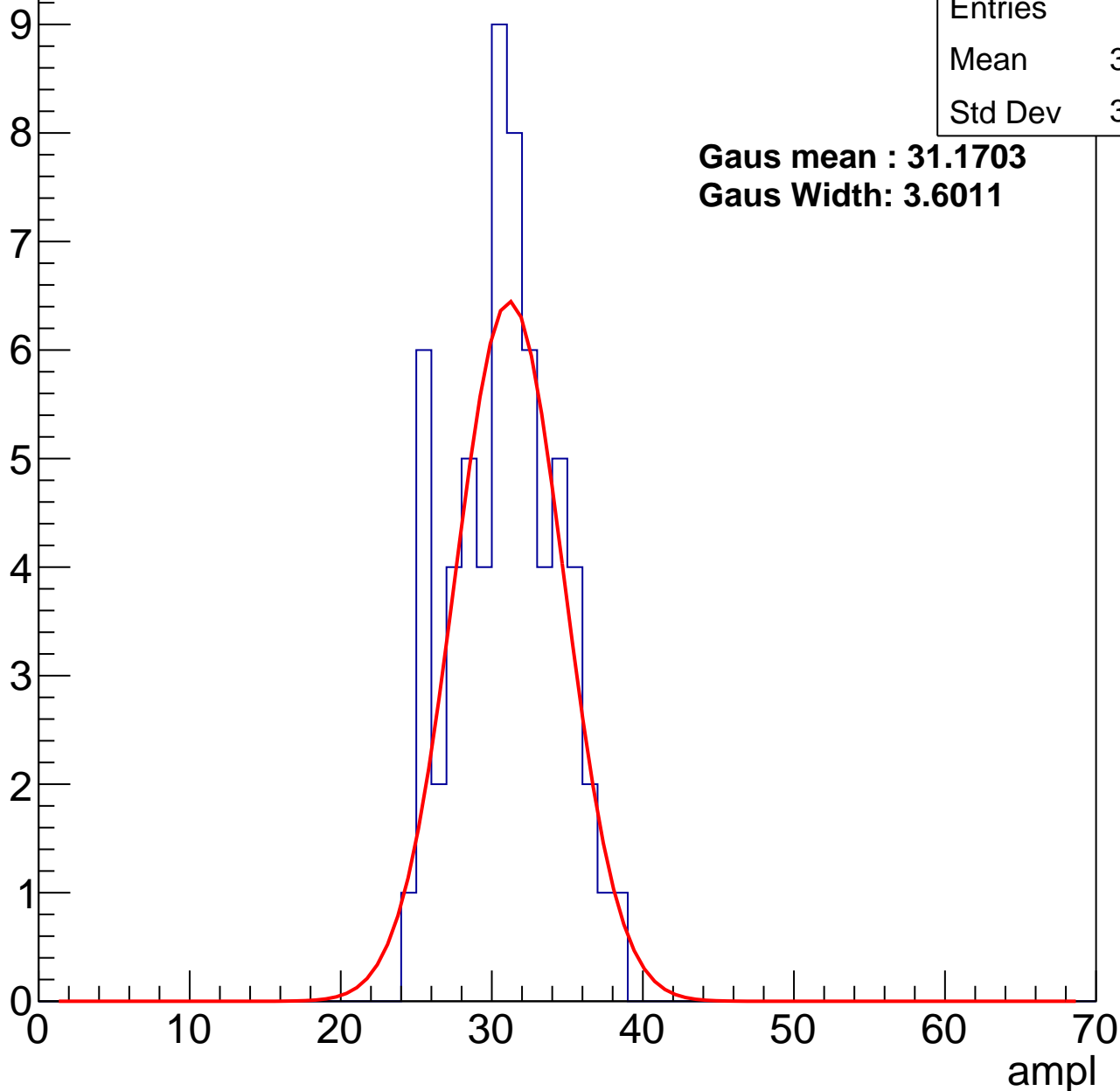
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	30.47
Std Dev	3.354

**Gaus mean : 31.1703**

**Gaus Width: 3.6011**



# B0L001S, U10-ch102, adc1

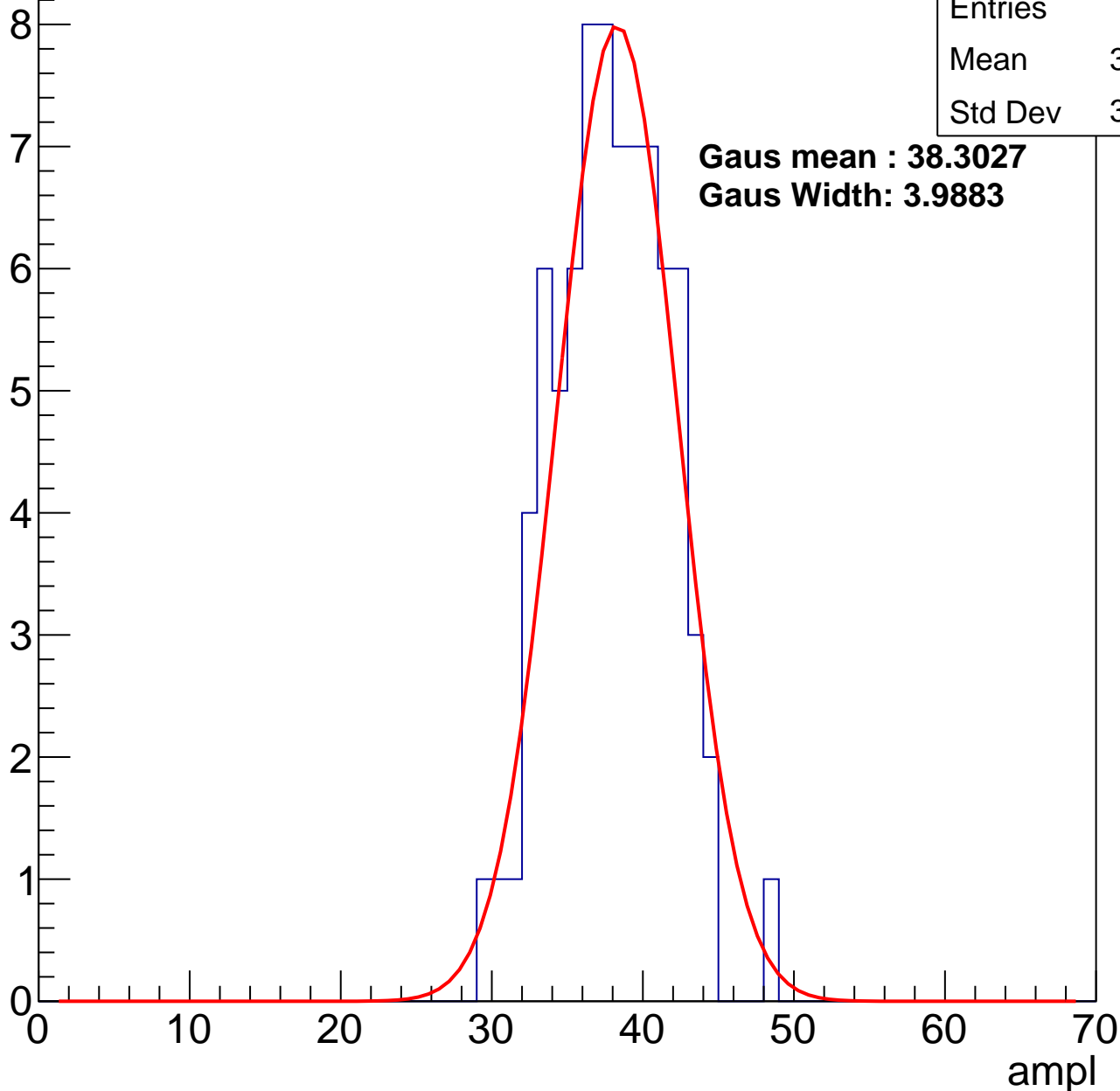
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	79
Mean	37.49
Std Dev	3.687

**Gaus mean : 38.3027**

**Gaus Width: 3.9883**



# B0L001S, U10-ch102, adc2

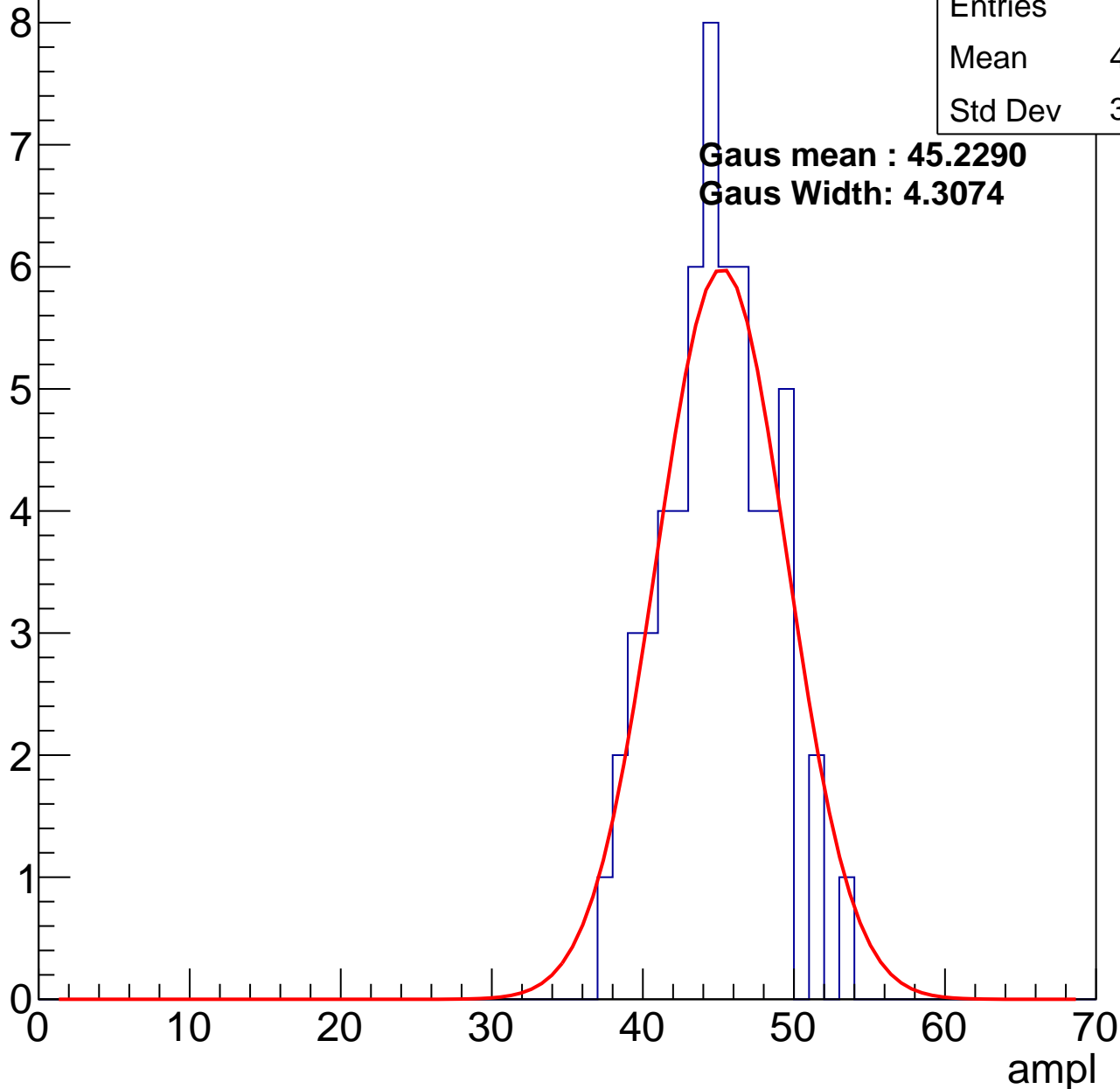
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	44.37
Std Dev	3.512

**Gaus mean : 45.2290**

**Gaus Width: 4.3074**

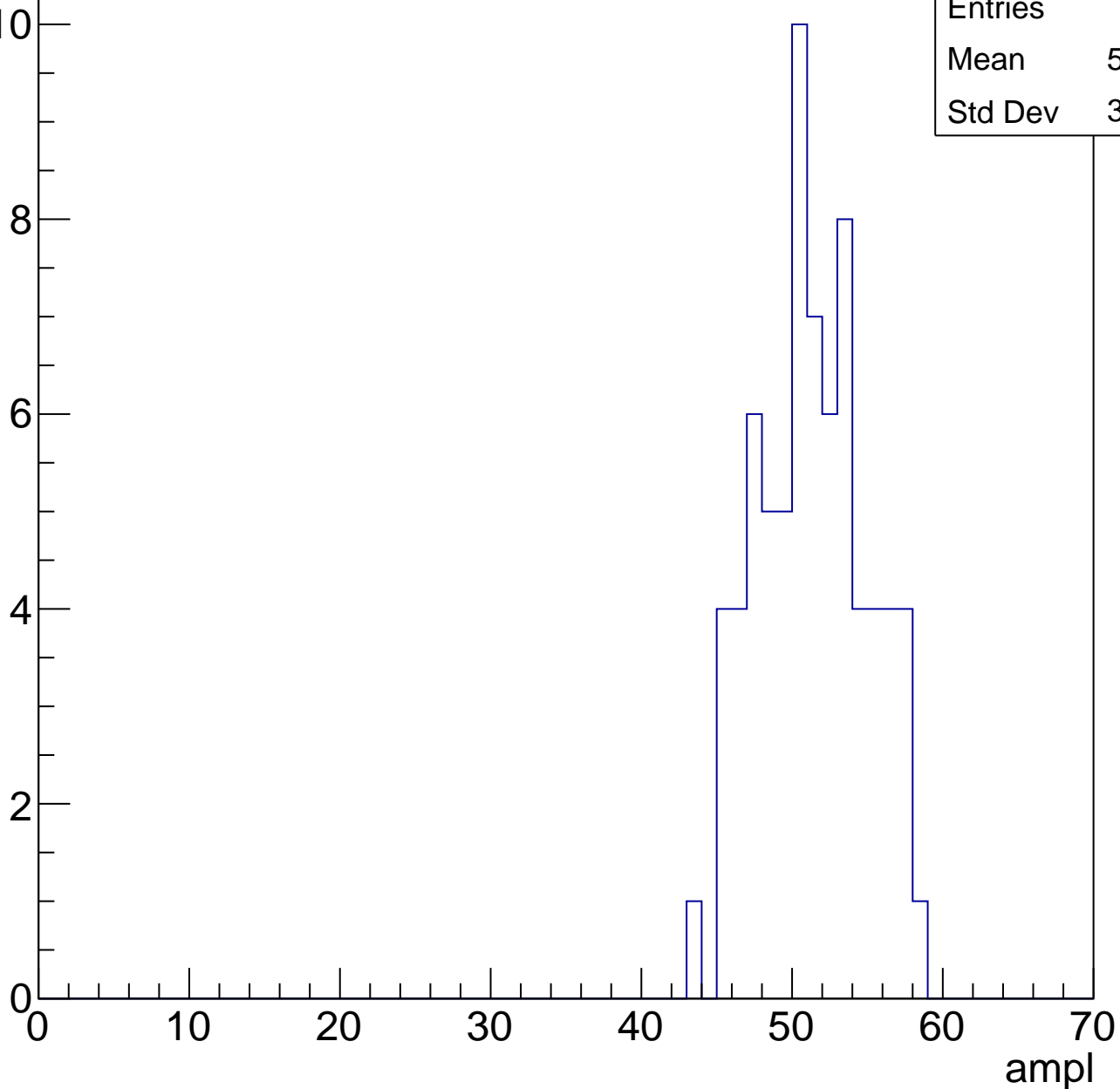


# B0L001S, U10-ch102, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	50.86
Std Dev	3.528

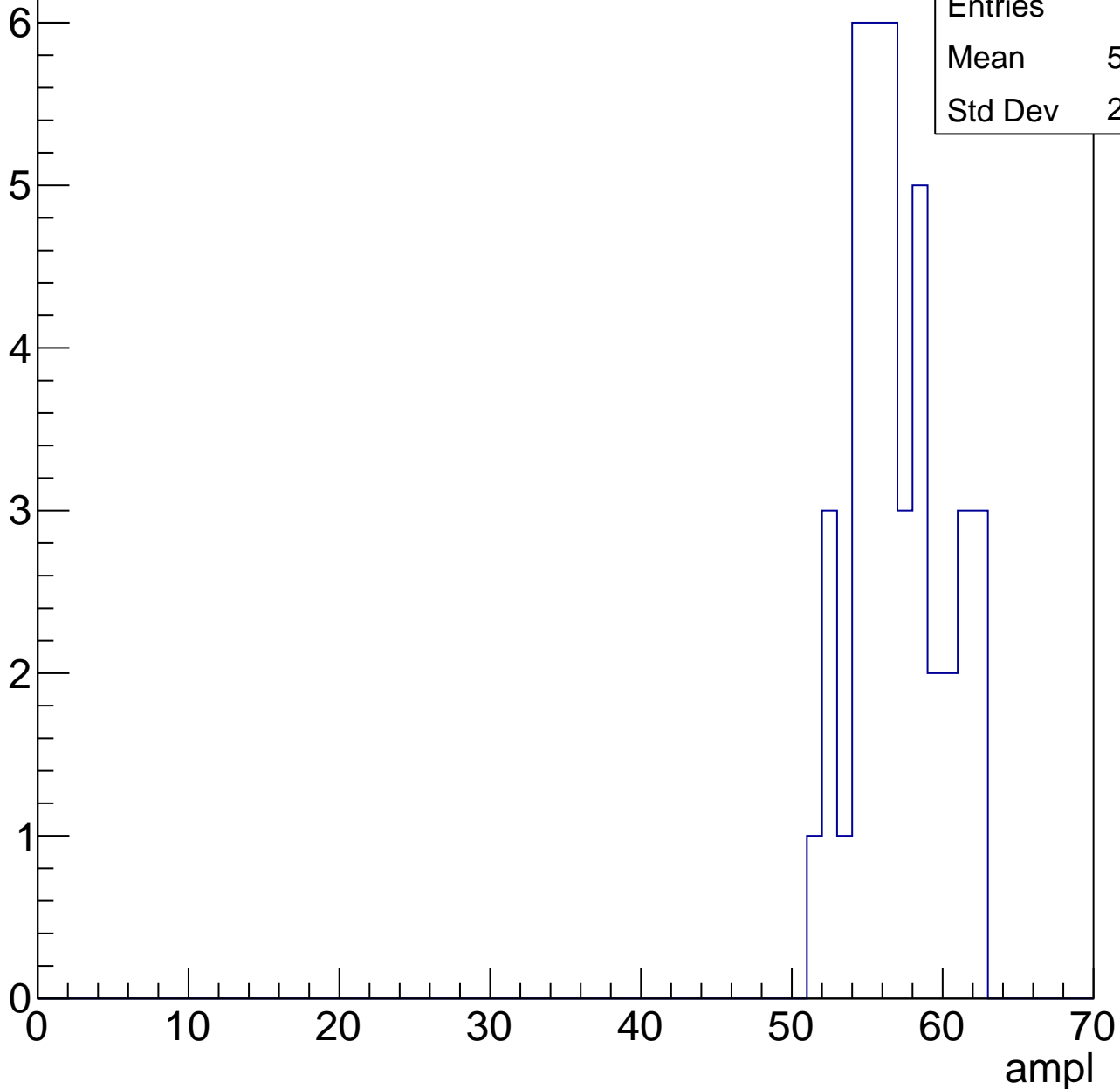


# B0L001S, U10-ch102, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	41
Mean	56.54
Std Dev	2.947

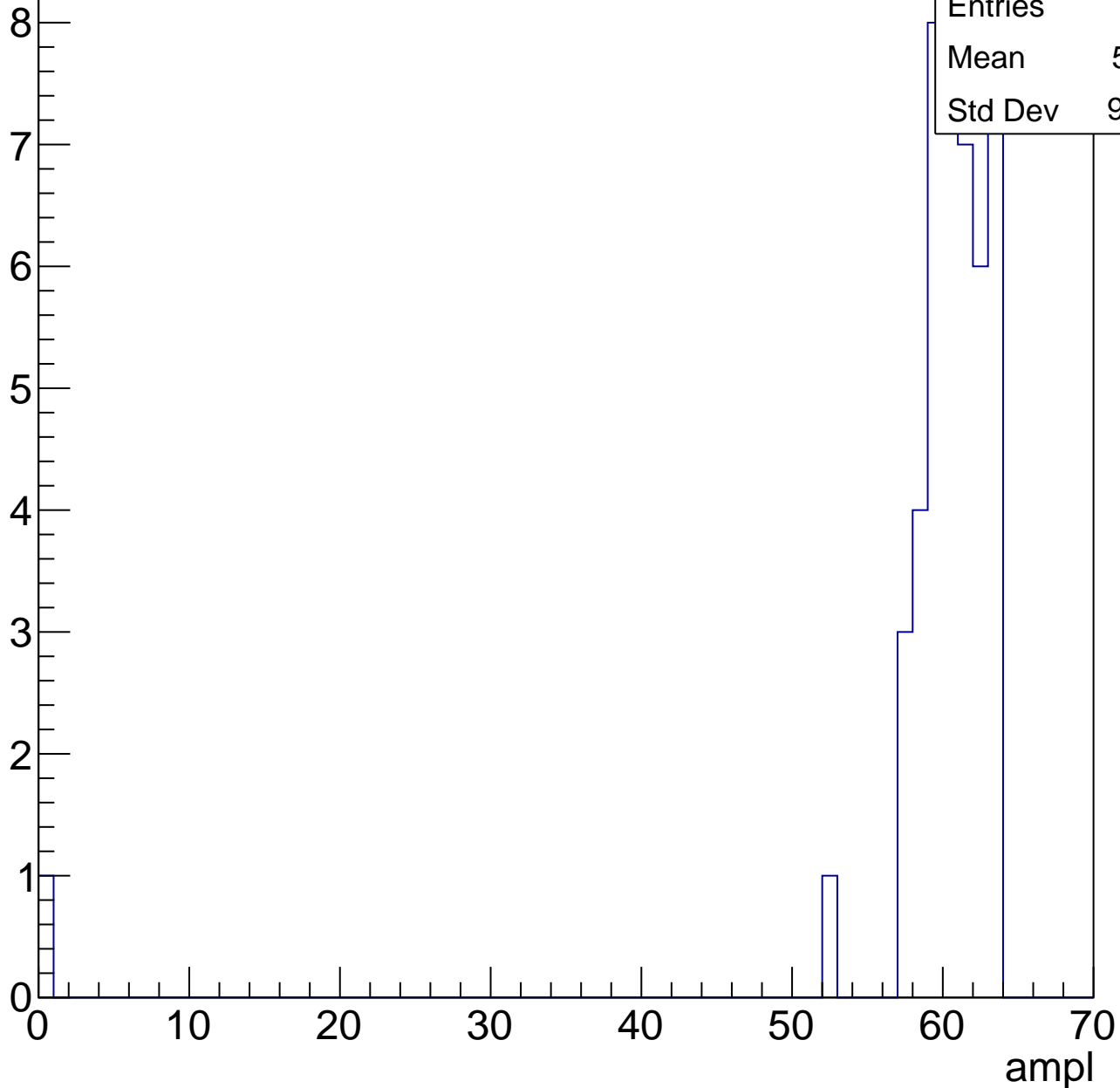


# B0L001S, U10-ch102, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	46
Mean	58.91
Std Dev	9.045



# B0L001S, U10-ch102, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch102, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U10-ch103, adc0

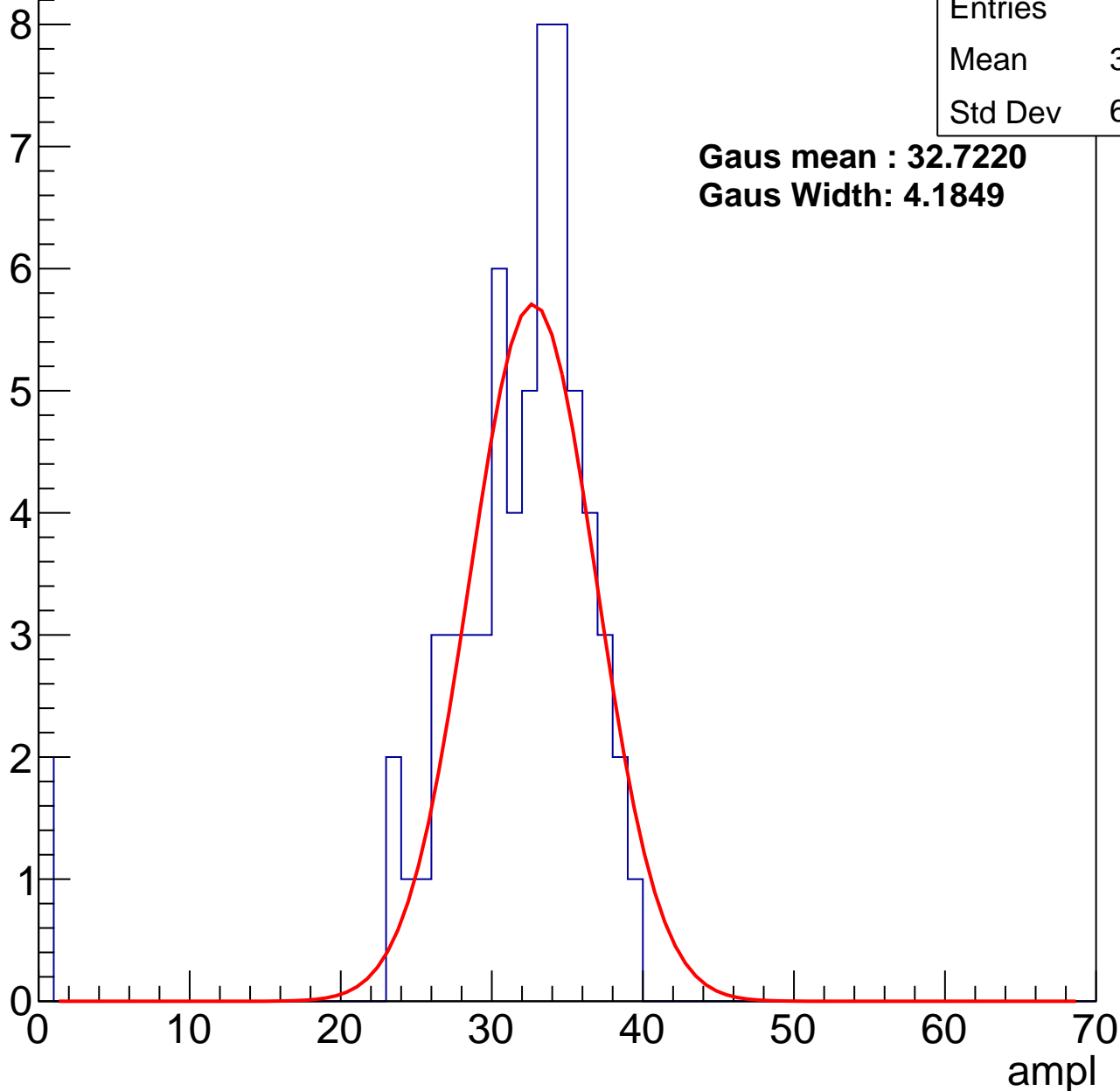
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	30.78
Std Dev	6.684

**Gaus mean : 32.7220**

**Gaus Width: 4.1849**



# B0L001S, U10-ch103, adc1

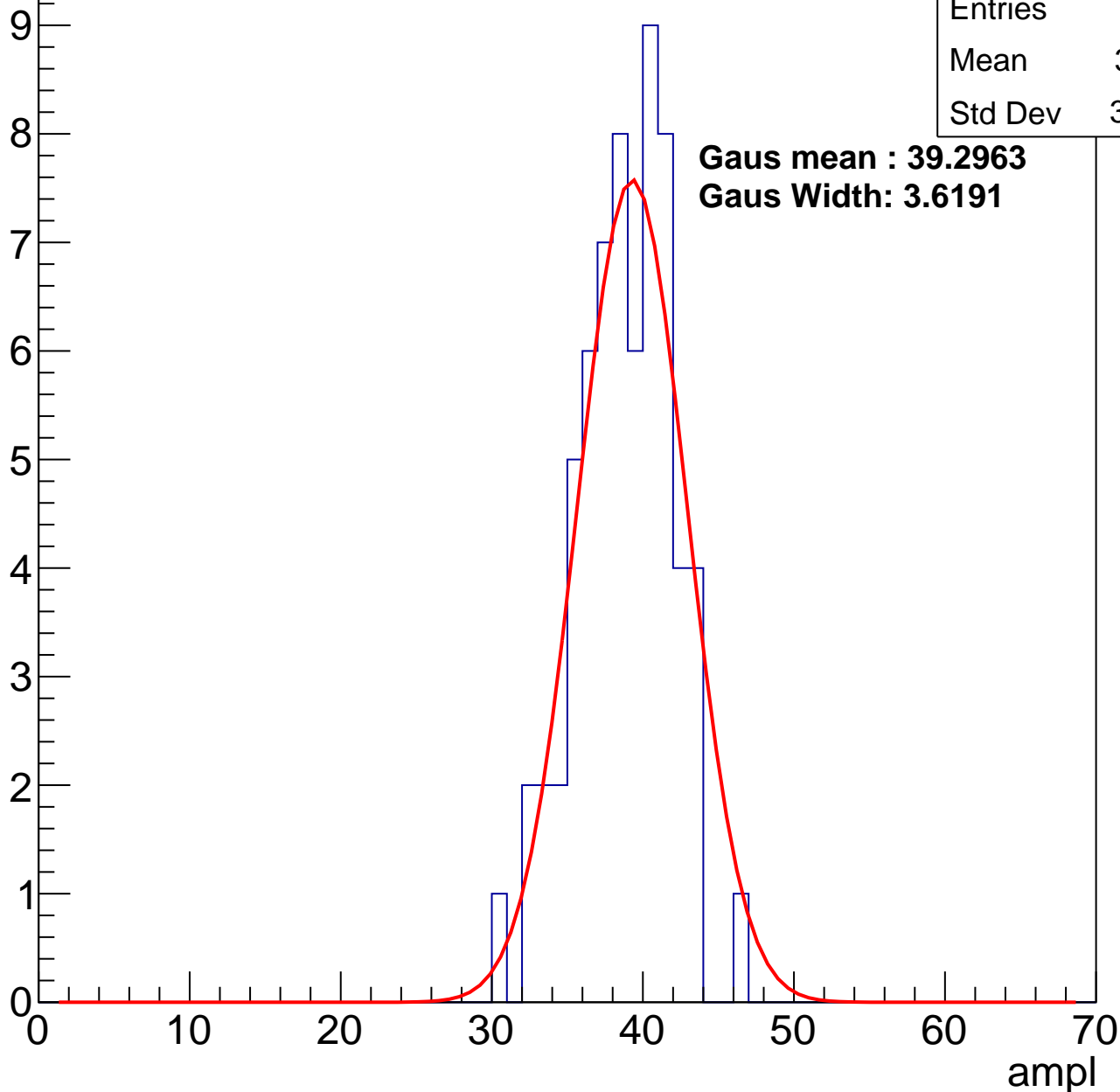
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	38.31
Std Dev	3.113

**Gaus mean : 39.2963**

**Gaus Width: 3.6191**



# B0L001S, U10-ch103, adc2

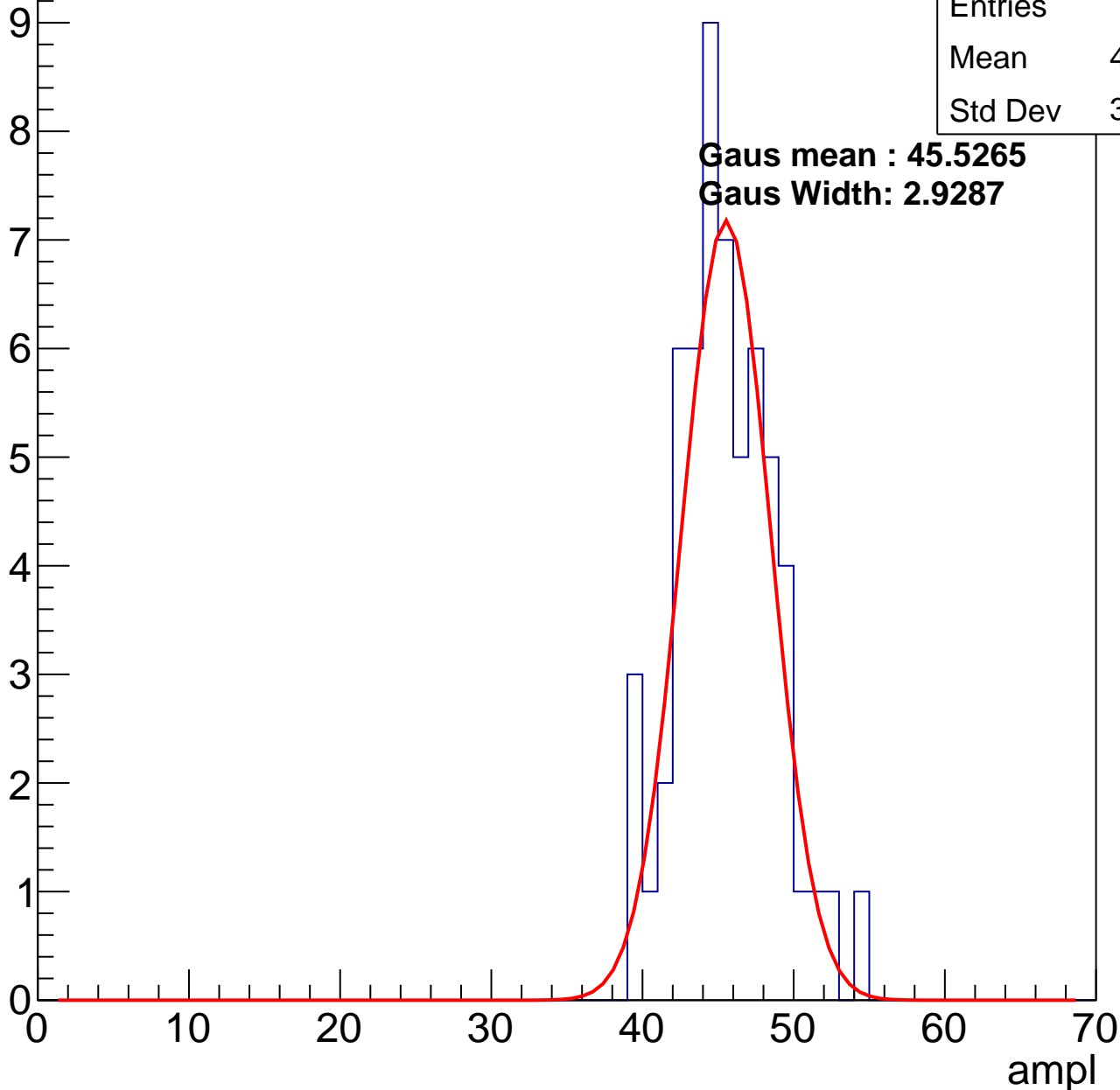
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	45.09
Std Dev	3.164

**Gaus mean : 45.5265**

**Gaus Width: 2.9287**

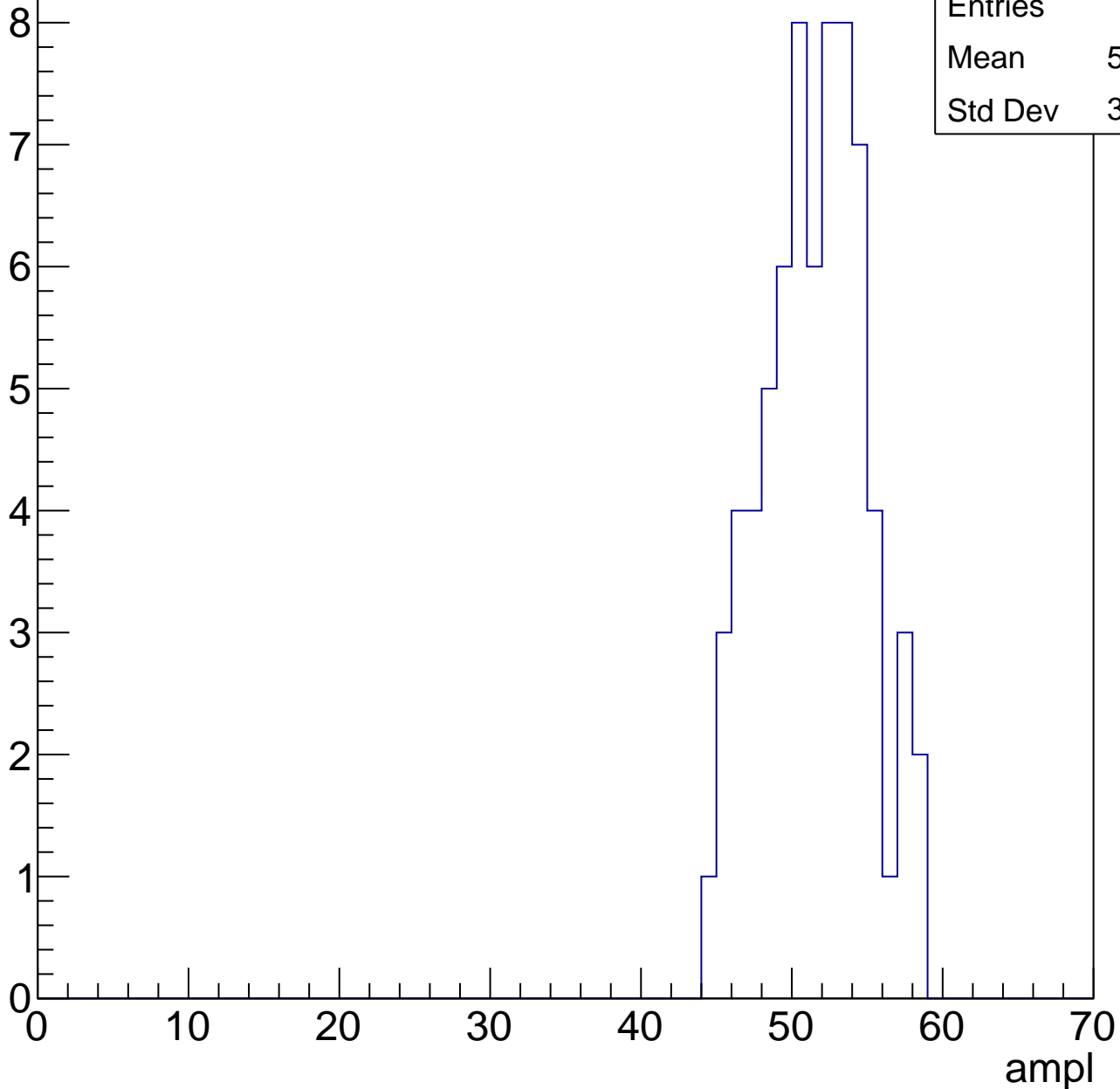


# B0L001S, U10-ch103, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

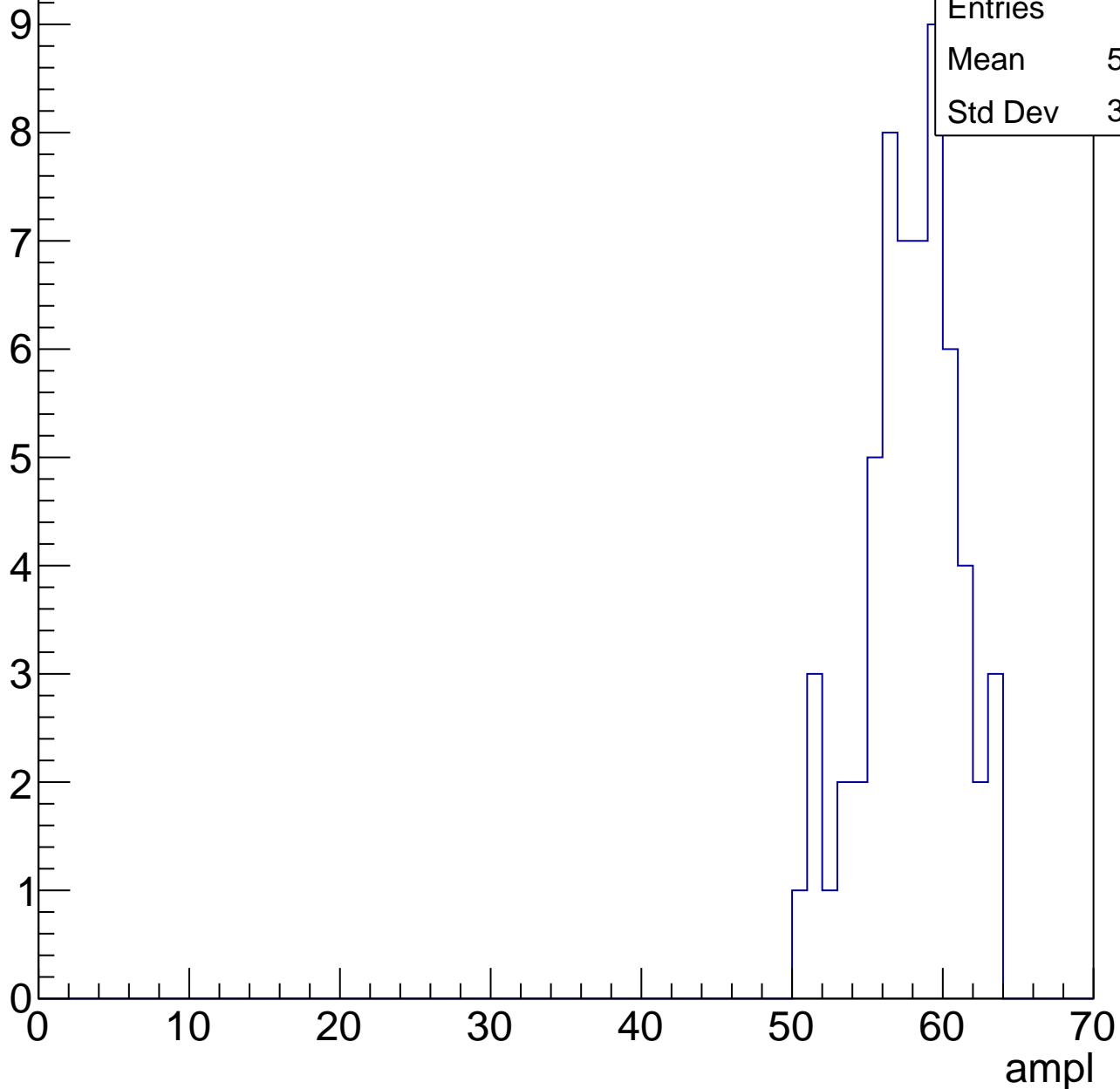
Entries	70
Mean	51.03
Std Dev	3.372



# B0L001S, U10-ch103, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

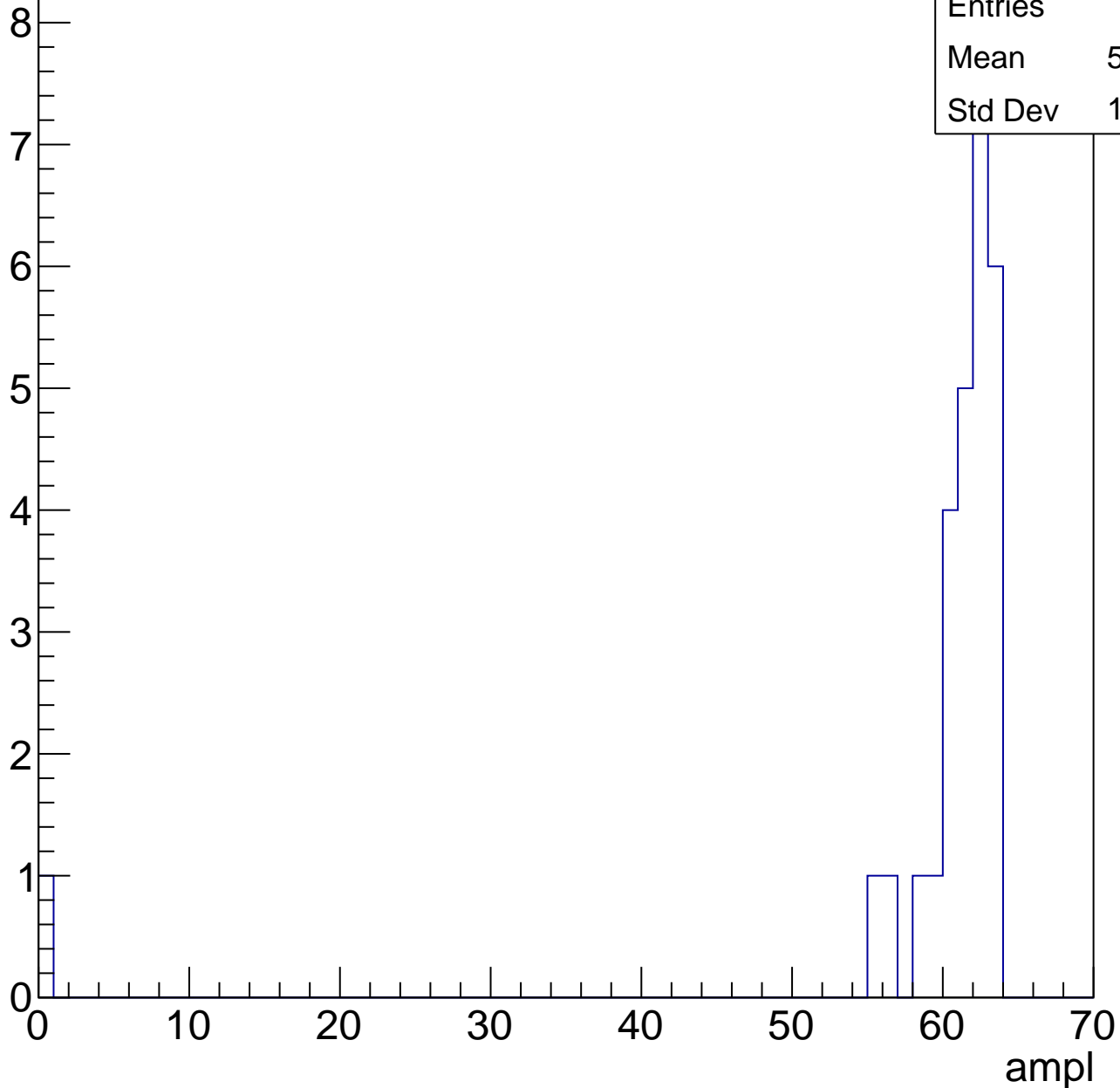


# B0L001S, U10-ch103, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	28
Mean	58.82
Std Dev	11.49



# B0L001S, U10-ch103, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch103, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U10-ch104, adc0

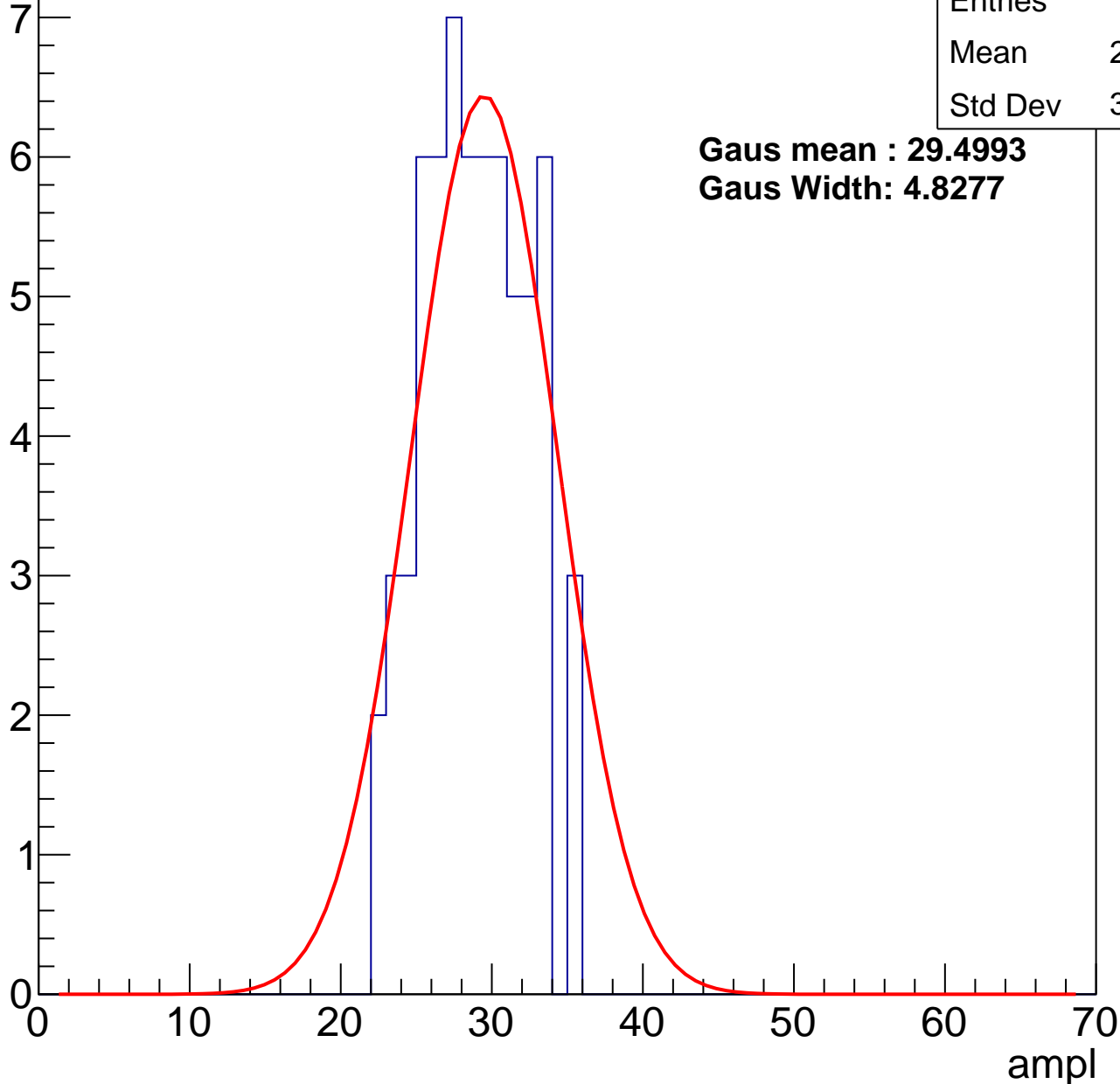
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	28.44
Std Dev	3.354

**Gaus mean : 29.4993**

**Gaus Width: 4.8277**



# B0L001S, U10-ch104, adc1

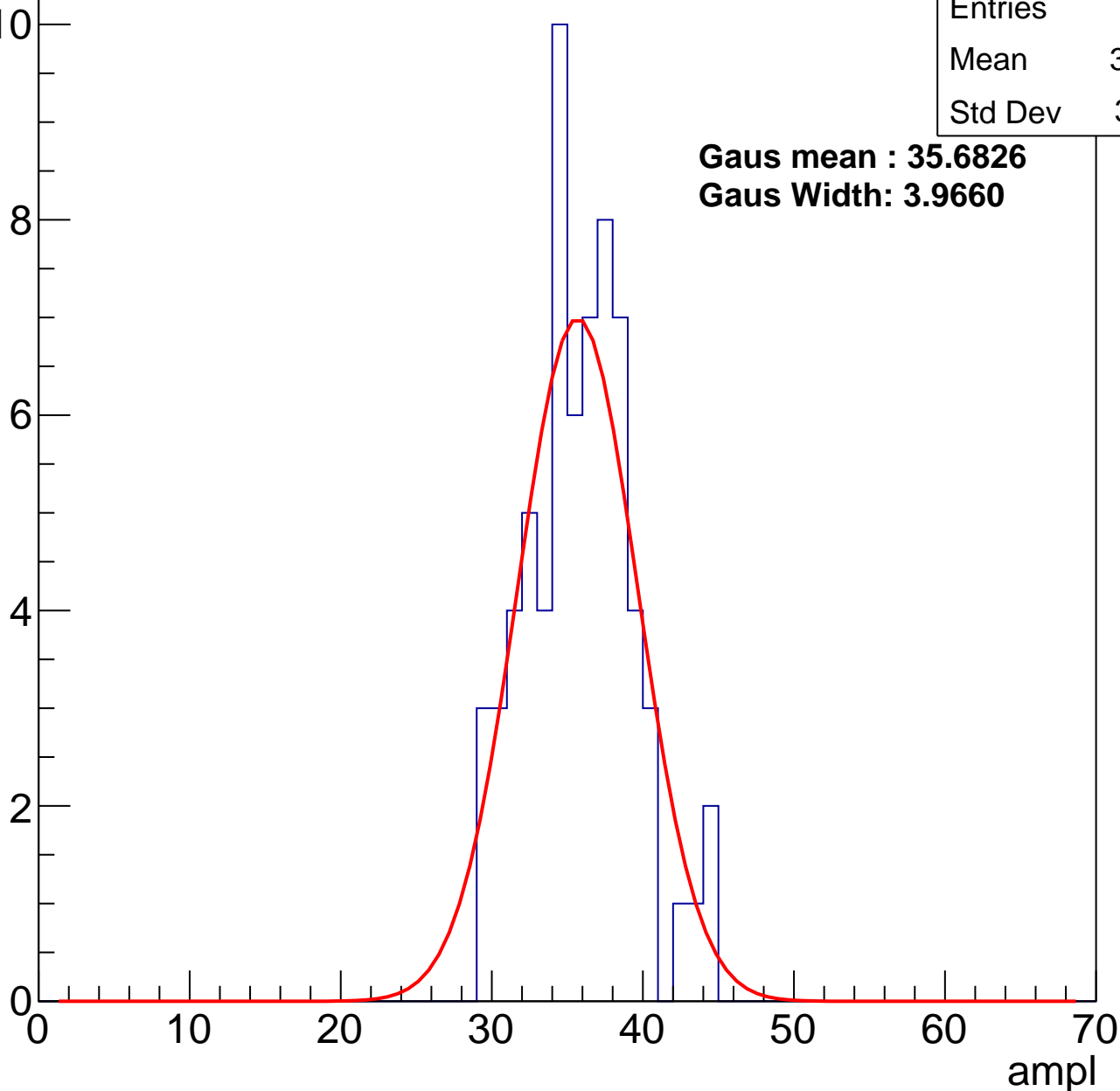
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	35.38
Std Dev	3.481

**Gaus mean : 35.6826**

**Gaus Width: 3.9660**



# B0L001S, U10-ch104, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	72
Mean	42.69
Std Dev	3.703

**Gaus mean : 43.2573**

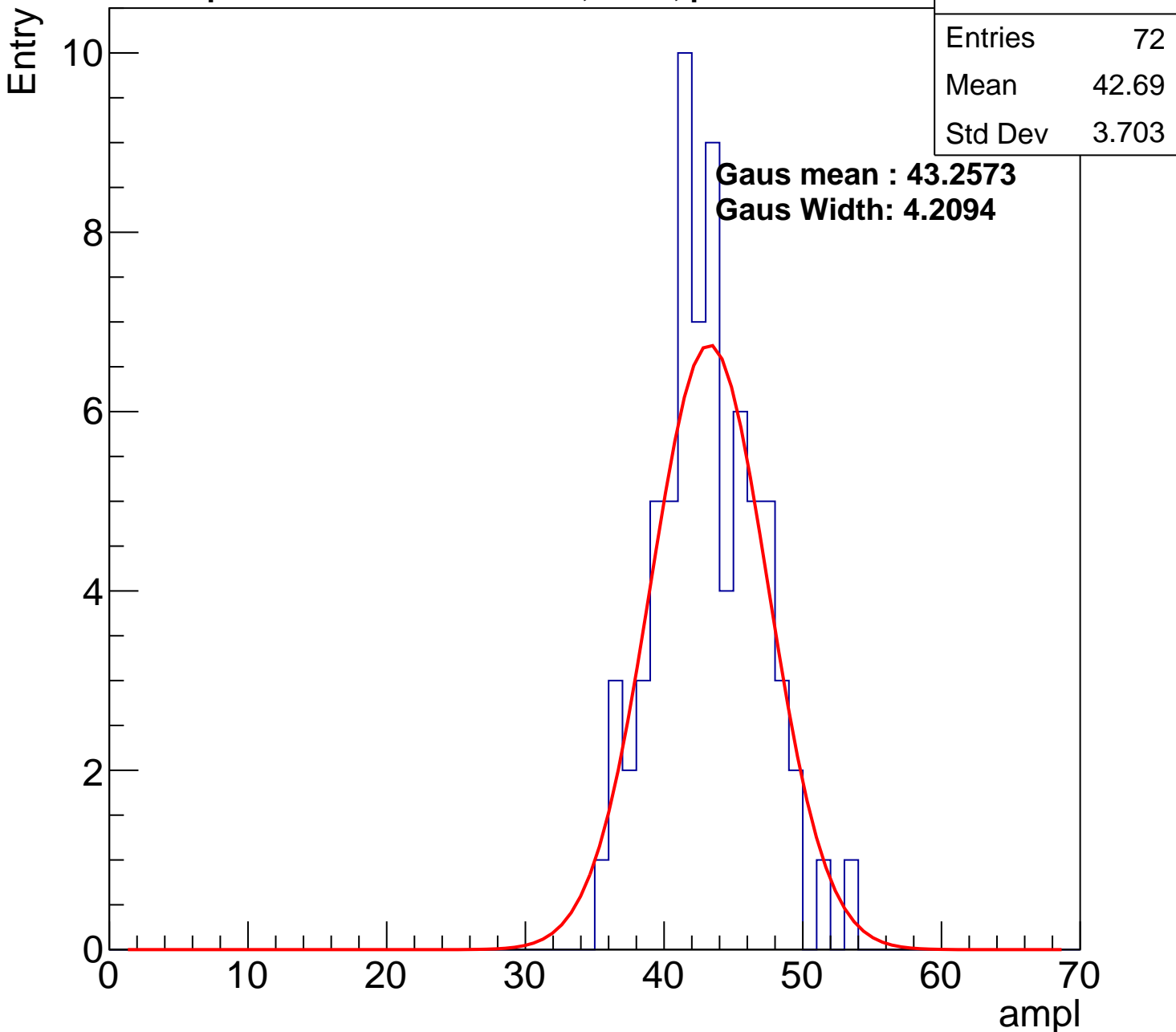
**Gaus Width: 4.2094**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

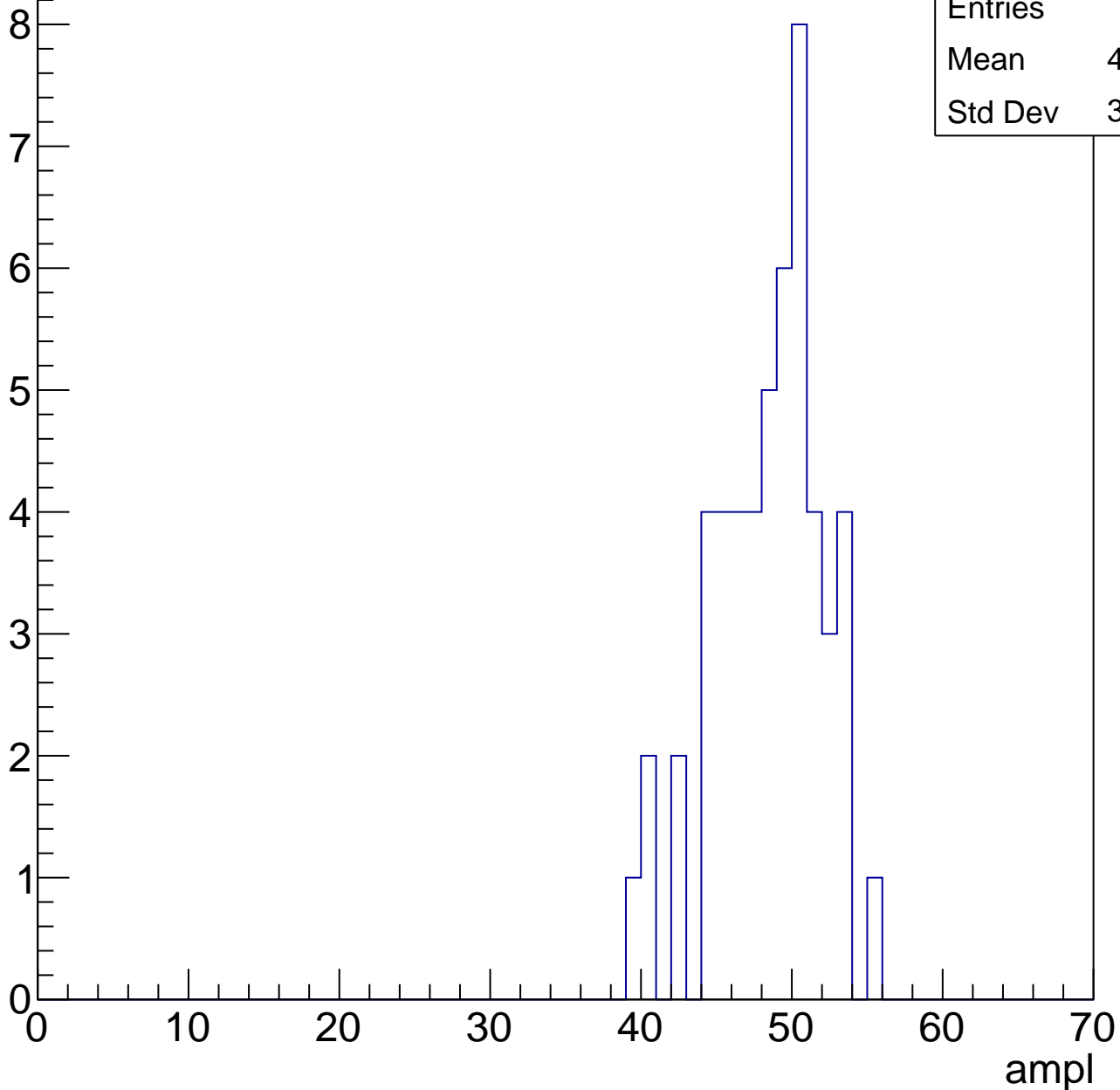


# B0L001S, U10-ch104, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	47.92
Std Dev	3.594

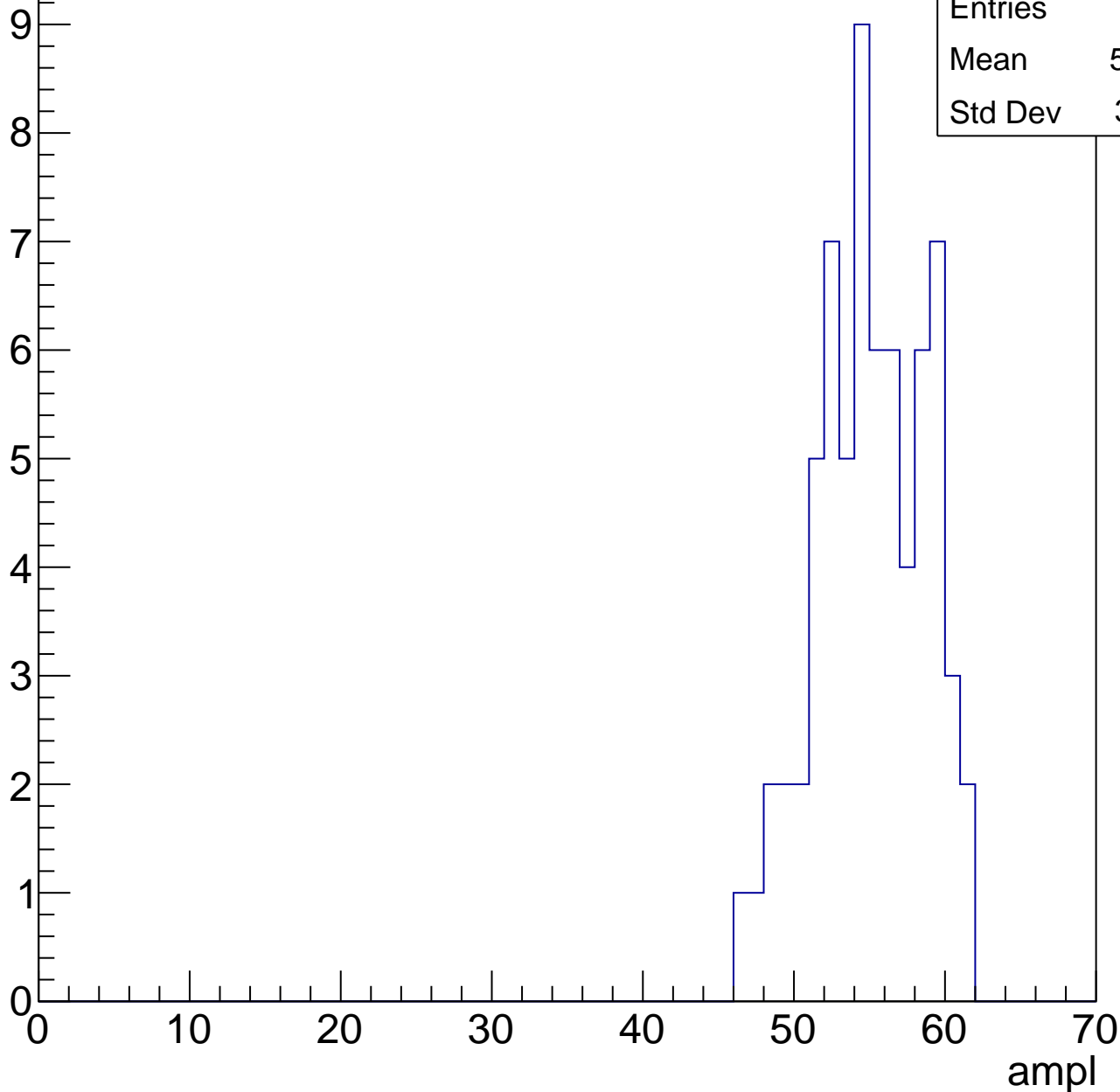


# B0L001S, U10-ch104, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	54.62
Std Dev	3.561

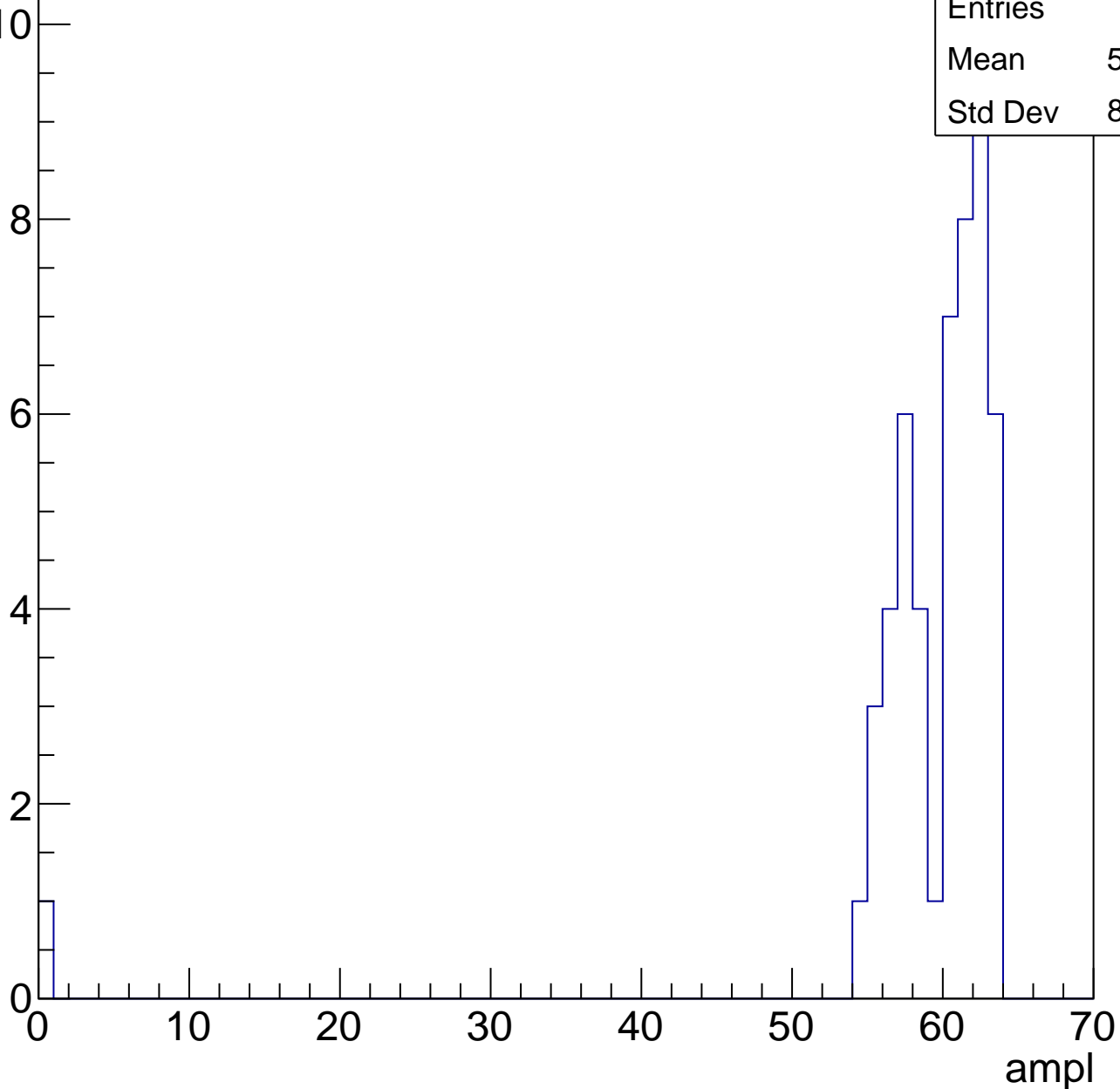


# B0L001S, U10-ch104, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

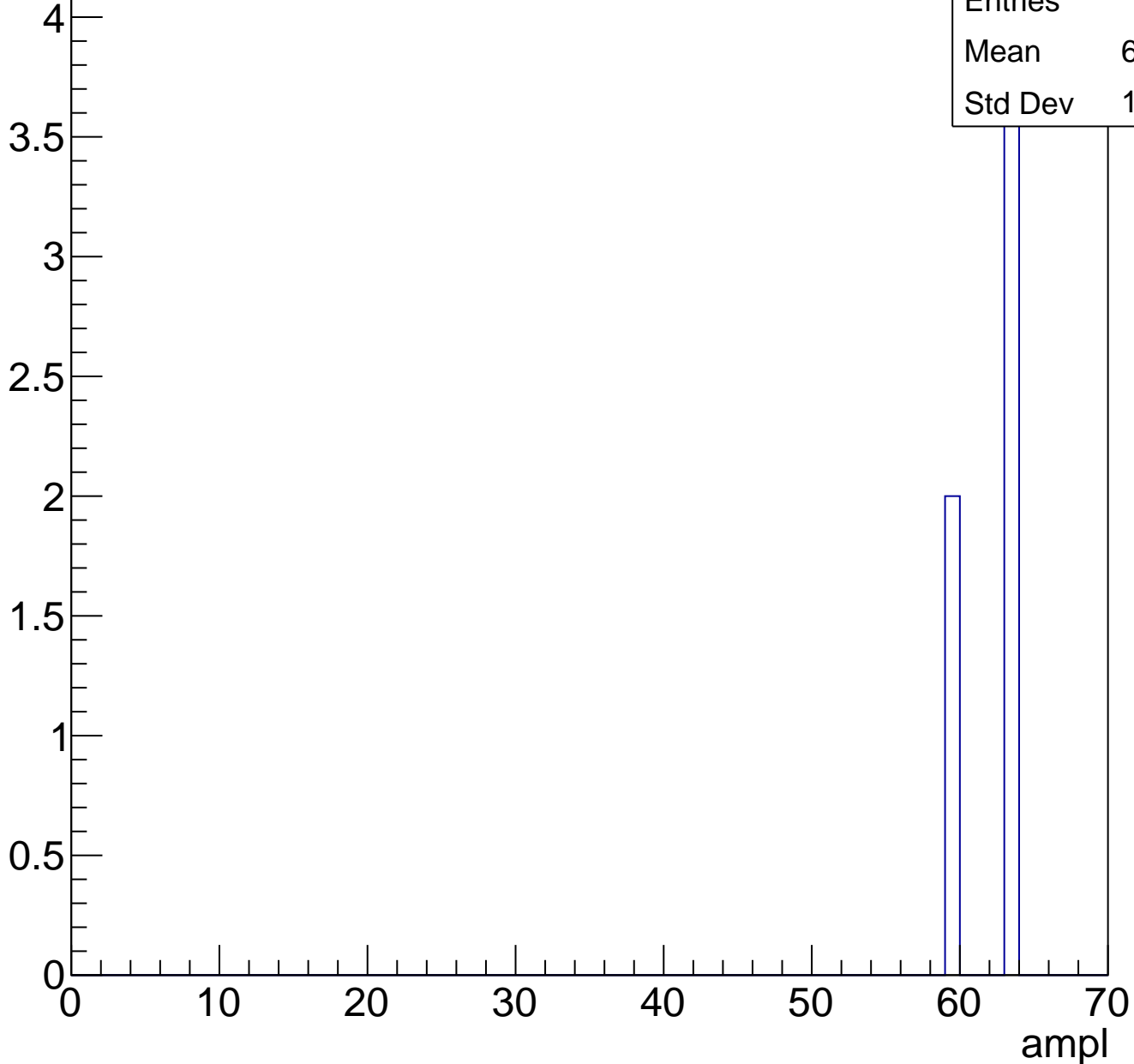
Entries	51
Mean	58.47
Std Dev	8.664



# B0L001S, U10-ch104, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch104, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U10-ch105, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	86
Mean	30.88
Std Dev	4.696

**Gaus mean : 31.4287**

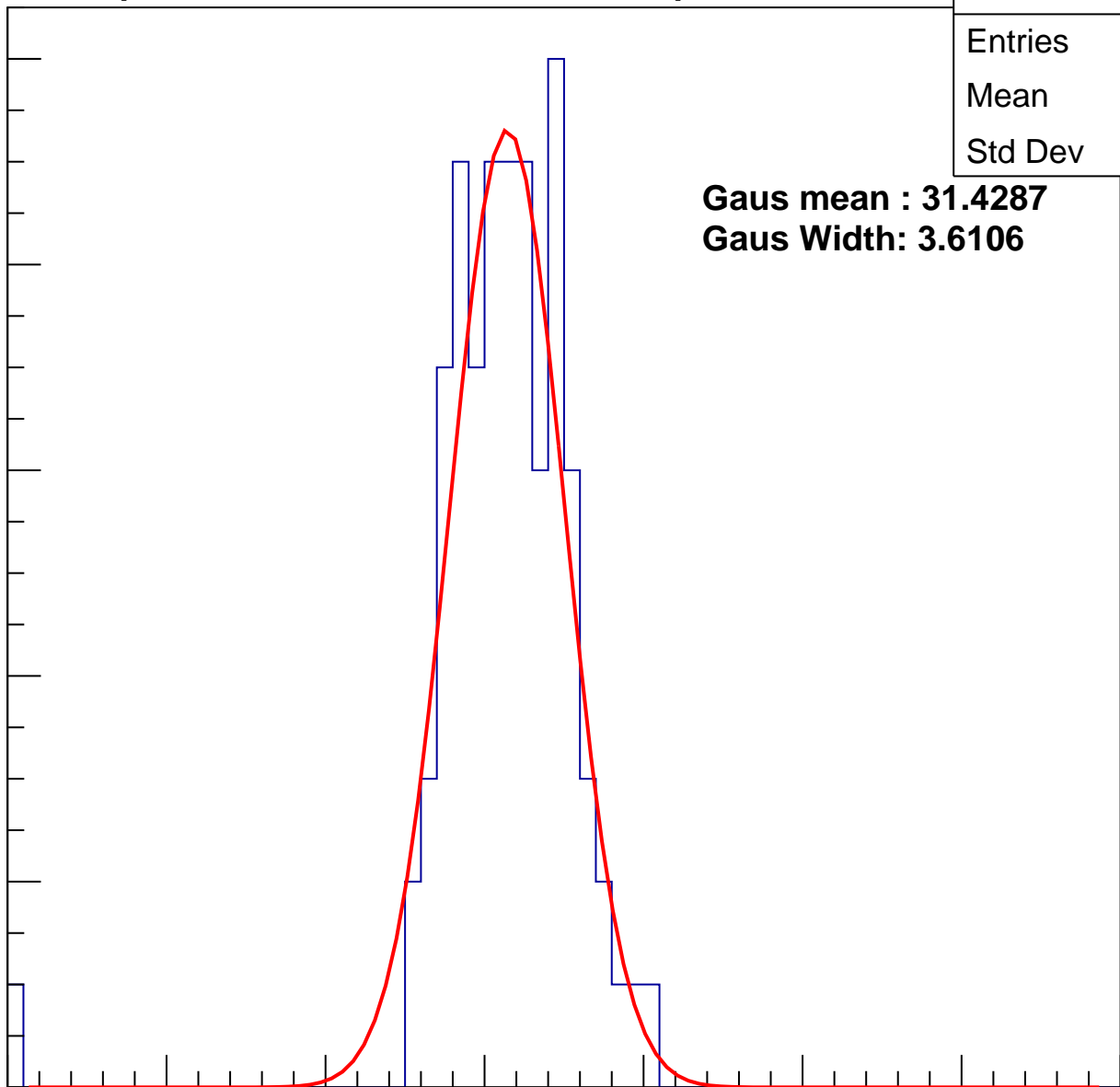
**Gaus Width: 3.6106**

Entry

10  
8  
6  
4  
2  
0

ampl

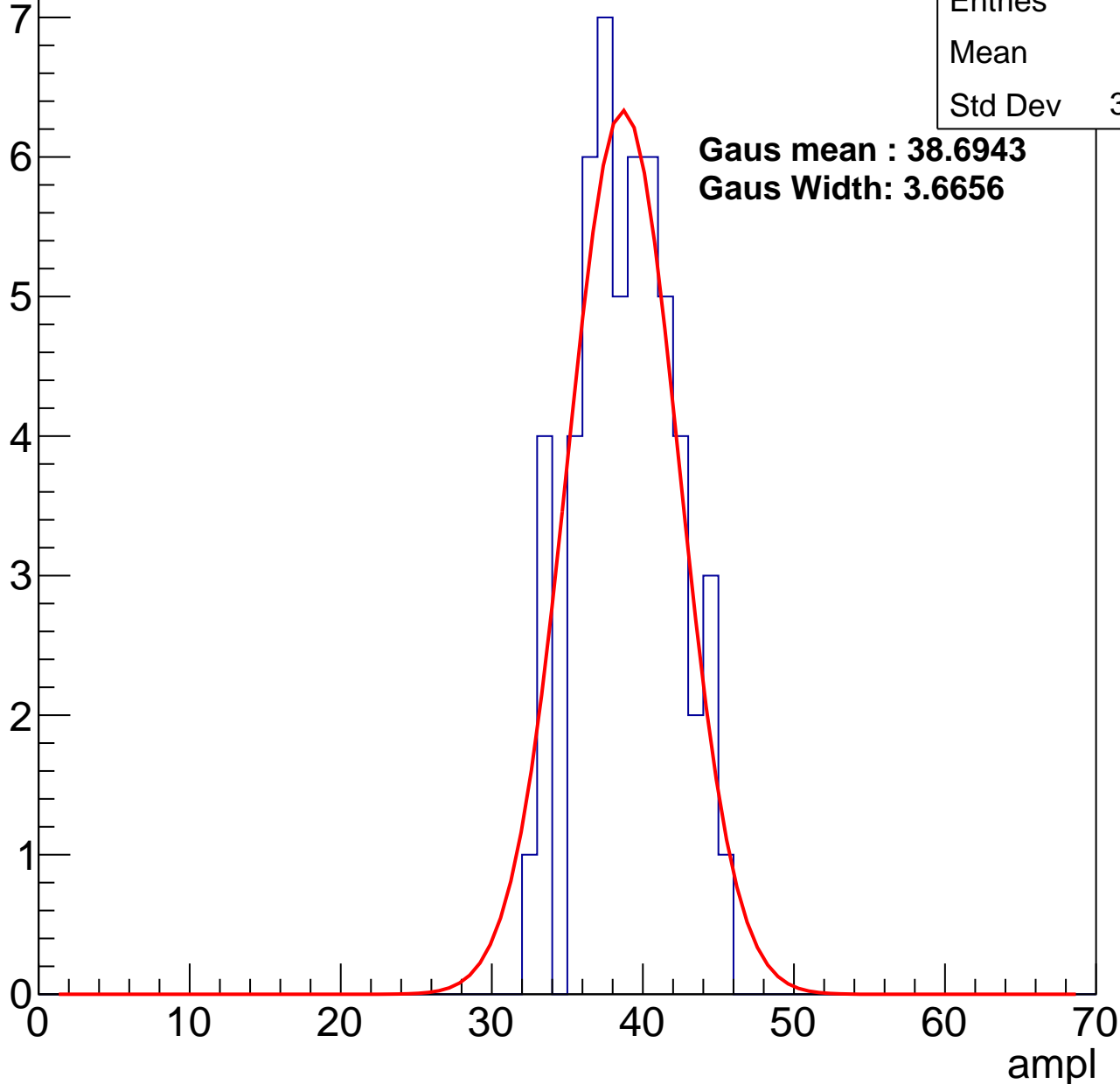
0 10 20 30 40 50 60 70



# B0L001S, U10-ch105, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U10-ch105, adc2

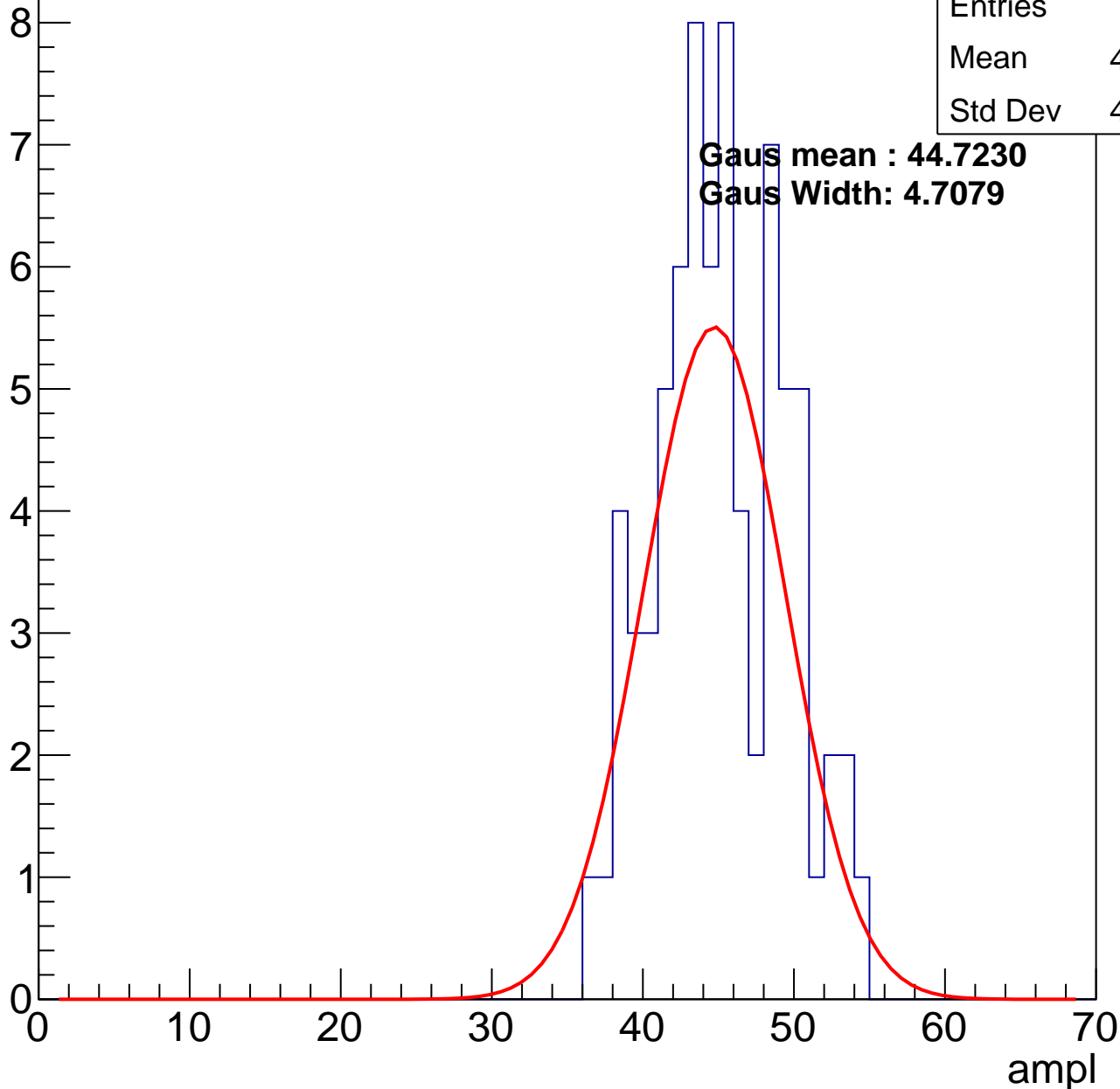
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	44.74
Std Dev	4.214

Gaus mean : 44.7230

Gaus Width: 4.7079

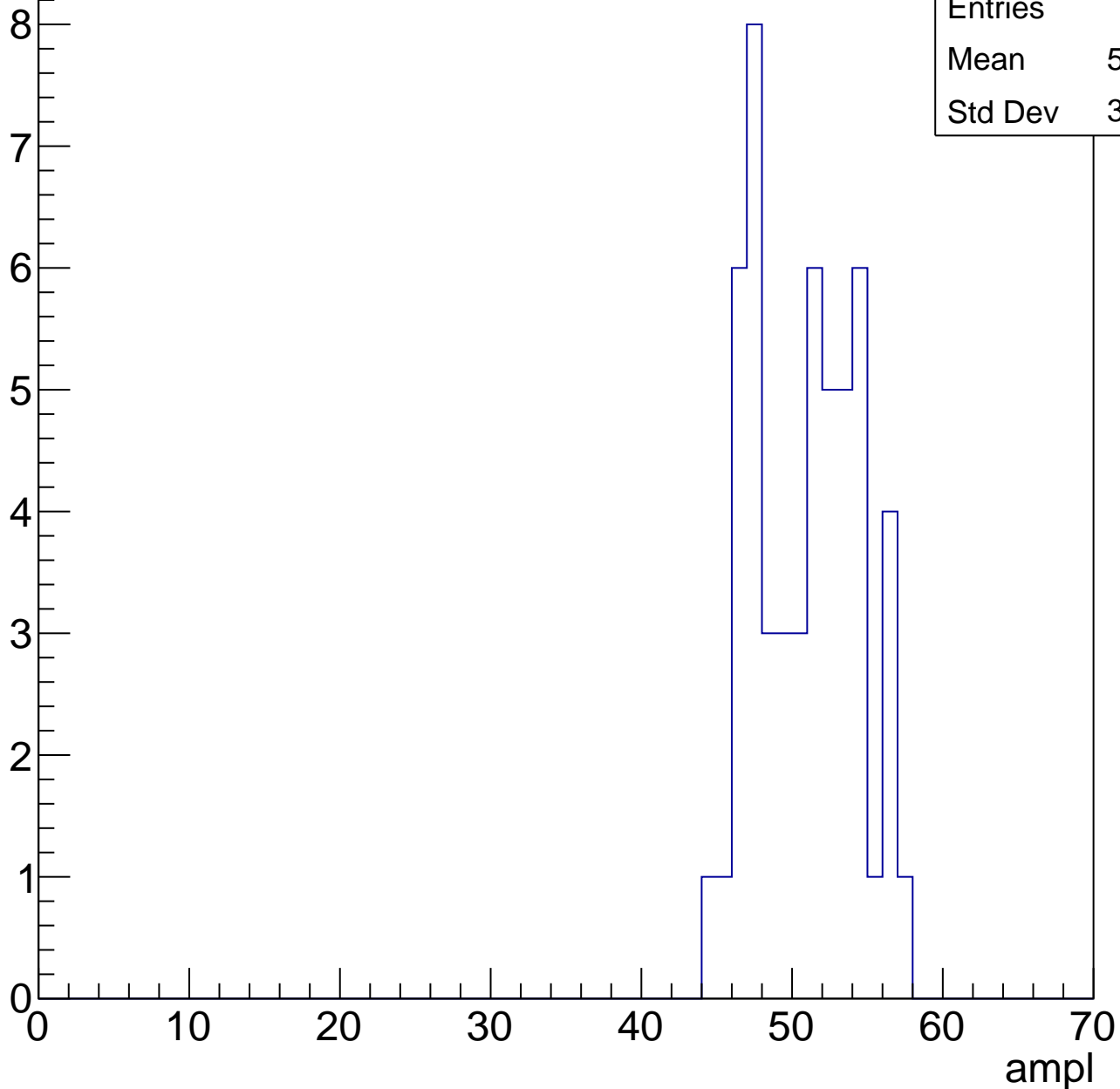


# B0L001S, U10-ch105, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	50.43
Std Dev	3.418



# B0L001S, U10-ch105, adc4

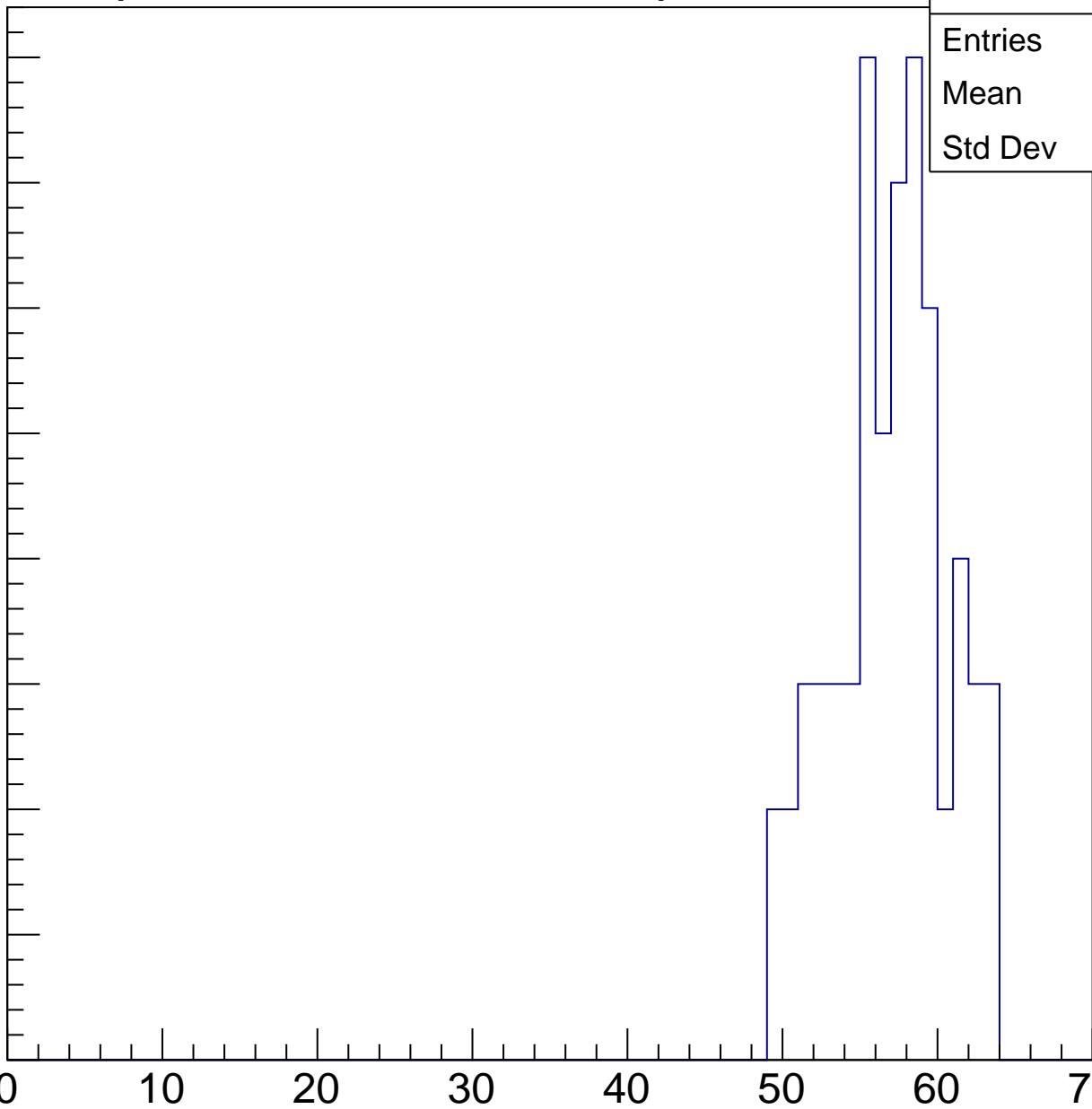
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	62
Mean	56.52
Std Dev	3.6

ampl

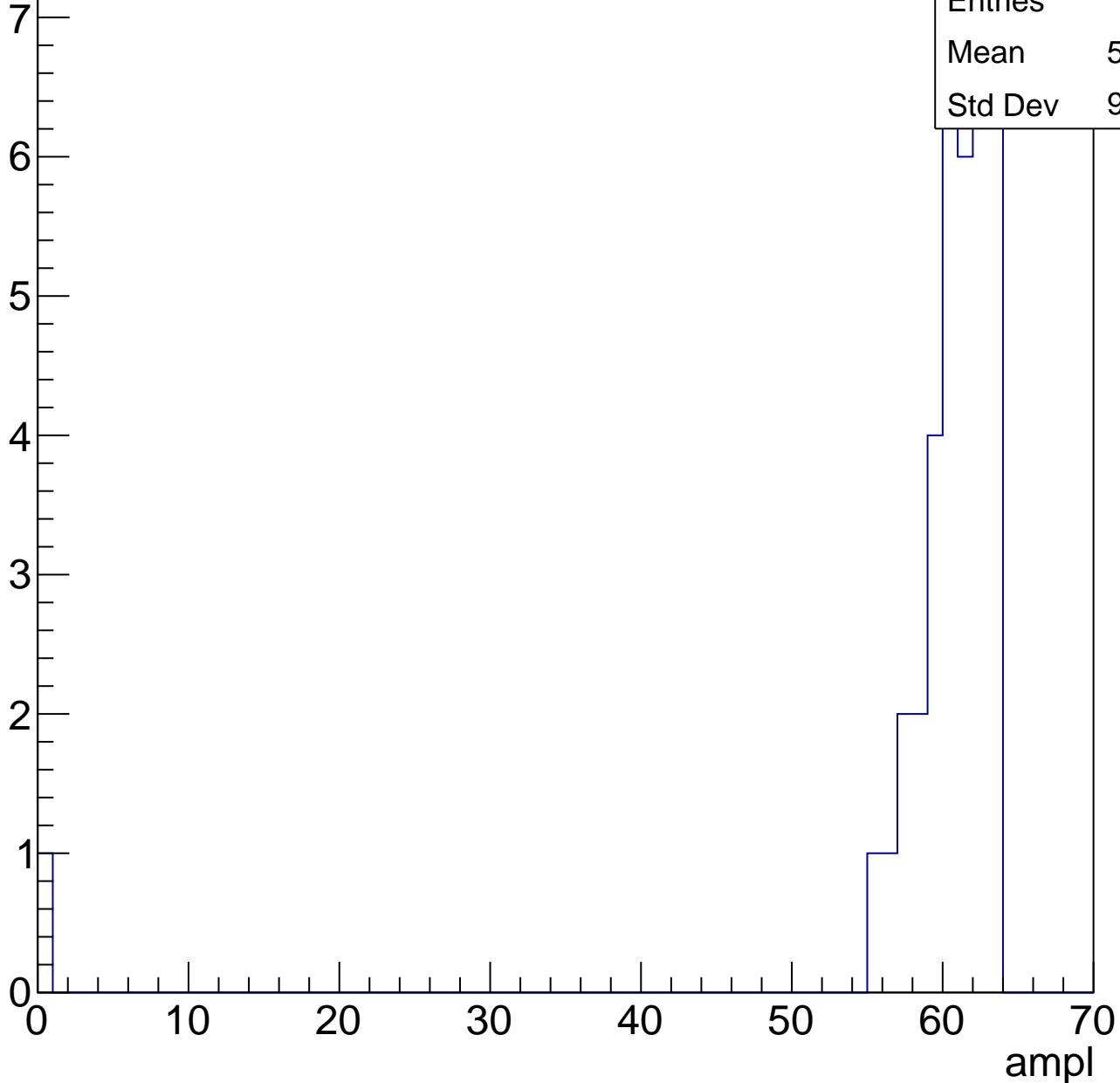


# B0L001S, U10-ch105, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	38
Mean	58.89
Std Dev	9.896



# B0L001S, U10-ch105, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch105, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U10-ch106, adc0

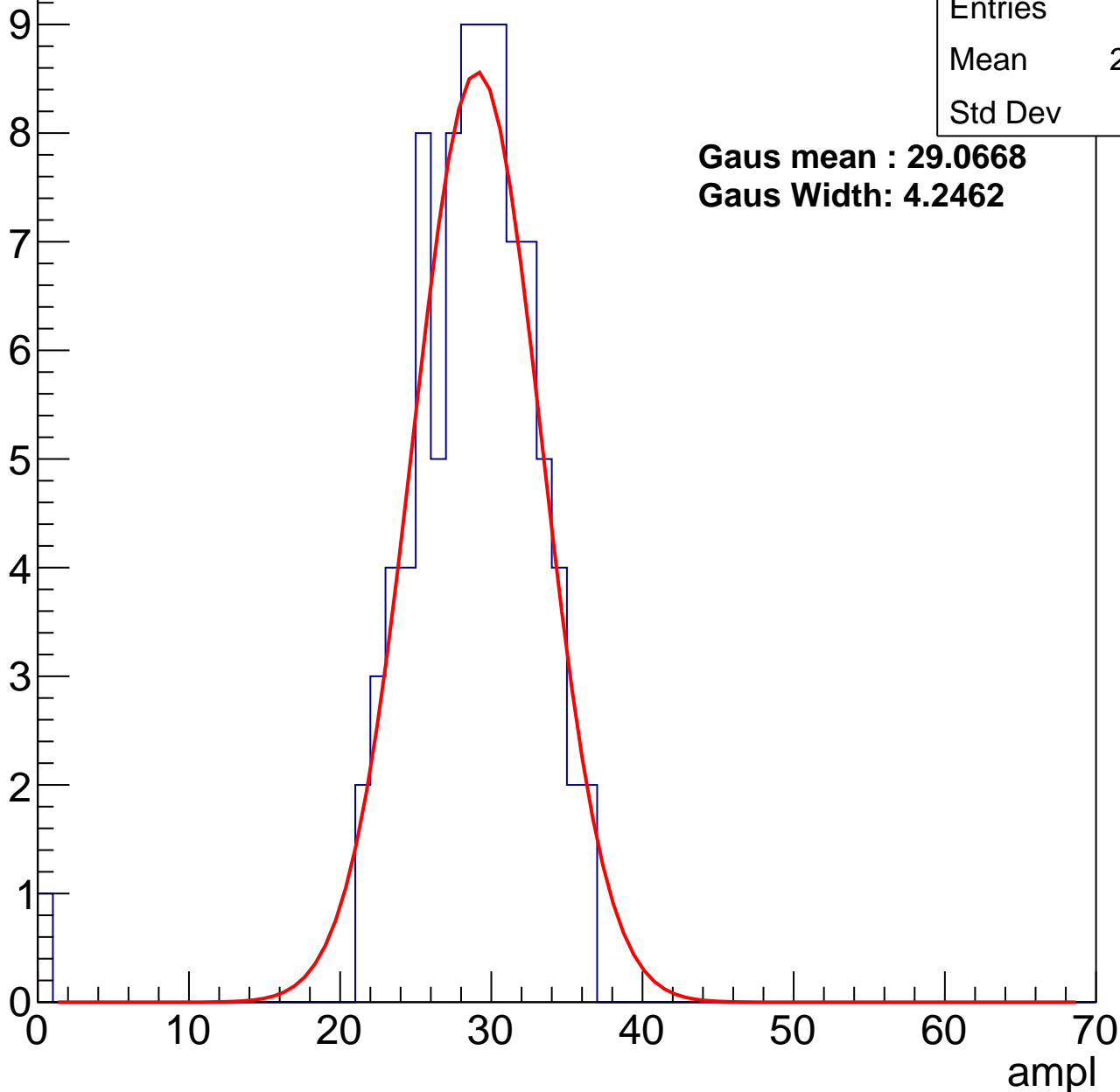
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	89
Mean	28.19
Std Dev	4.7

**Gaus mean : 29.0668**

**Gaus Width: 4.2462**



# B0L001S, U10-ch106, adc1

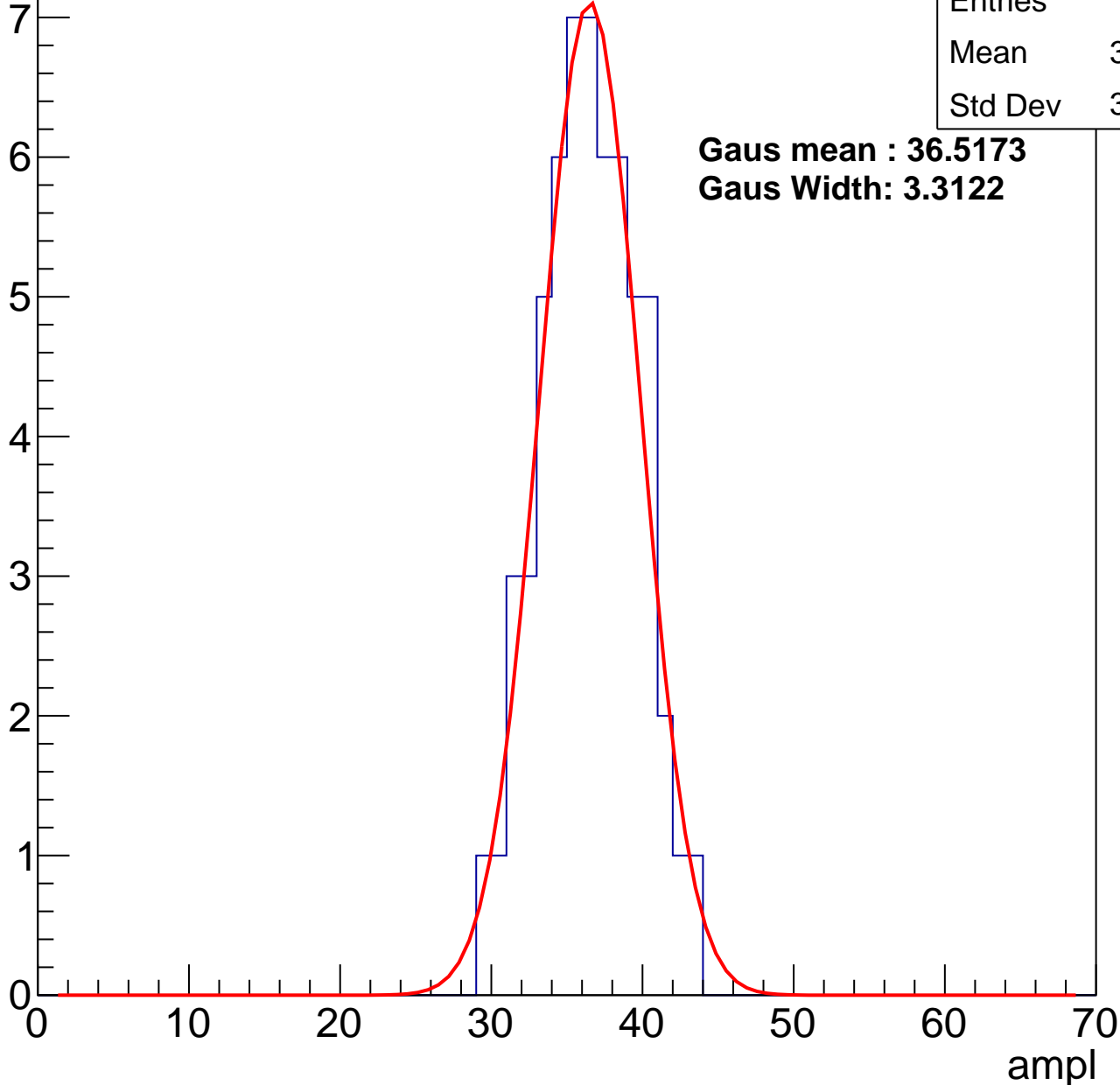
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	36.03
Std Dev	3.119

**Gaus mean : 36.5173**

**Gaus Width: 3.3122**



# B0L001S, U10-ch106, adc2

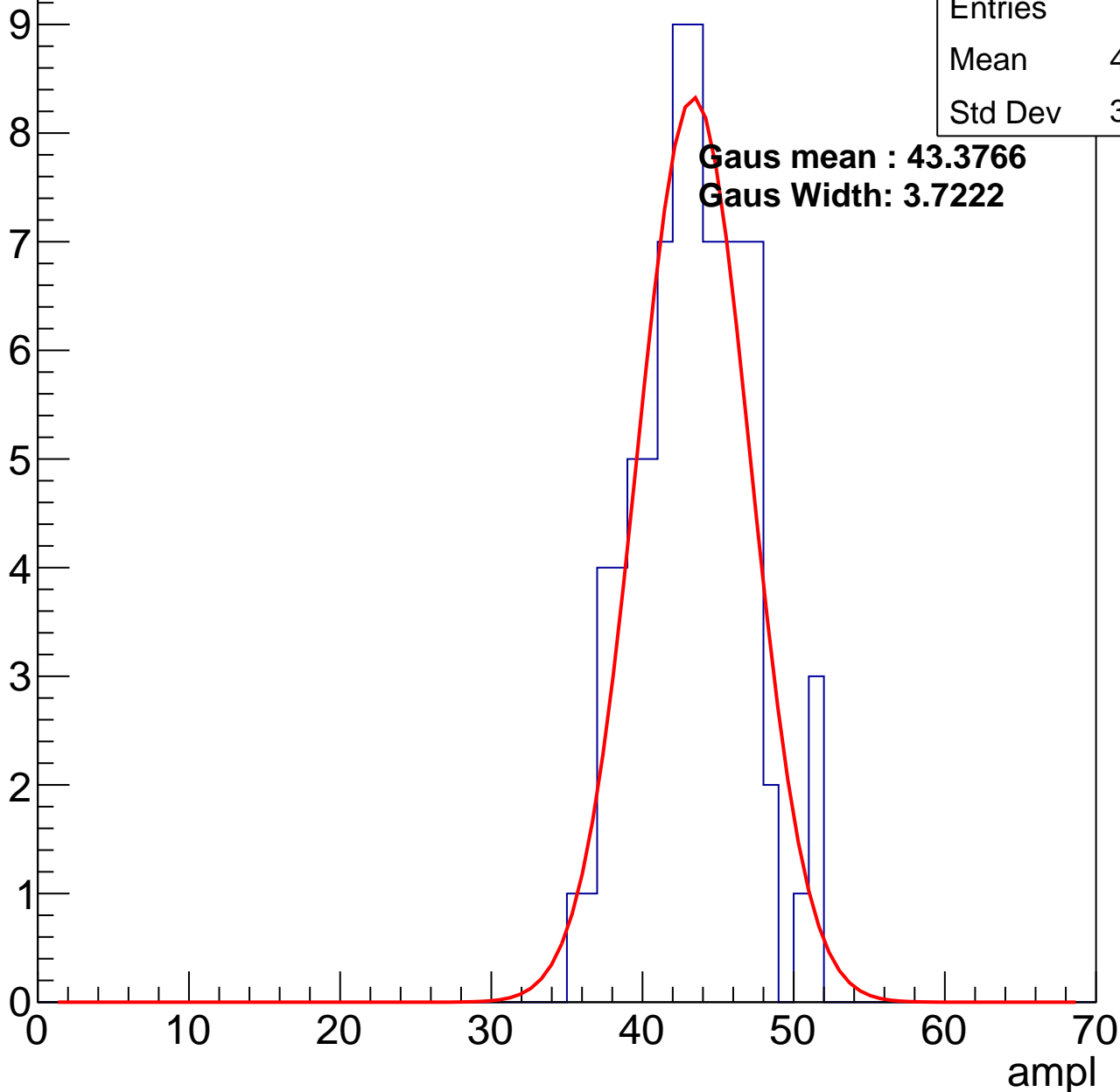
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	79
Mean	42.92
Std Dev	3.592

**Gaus mean : 43.3766**

**Gaus Width: 3.7222**

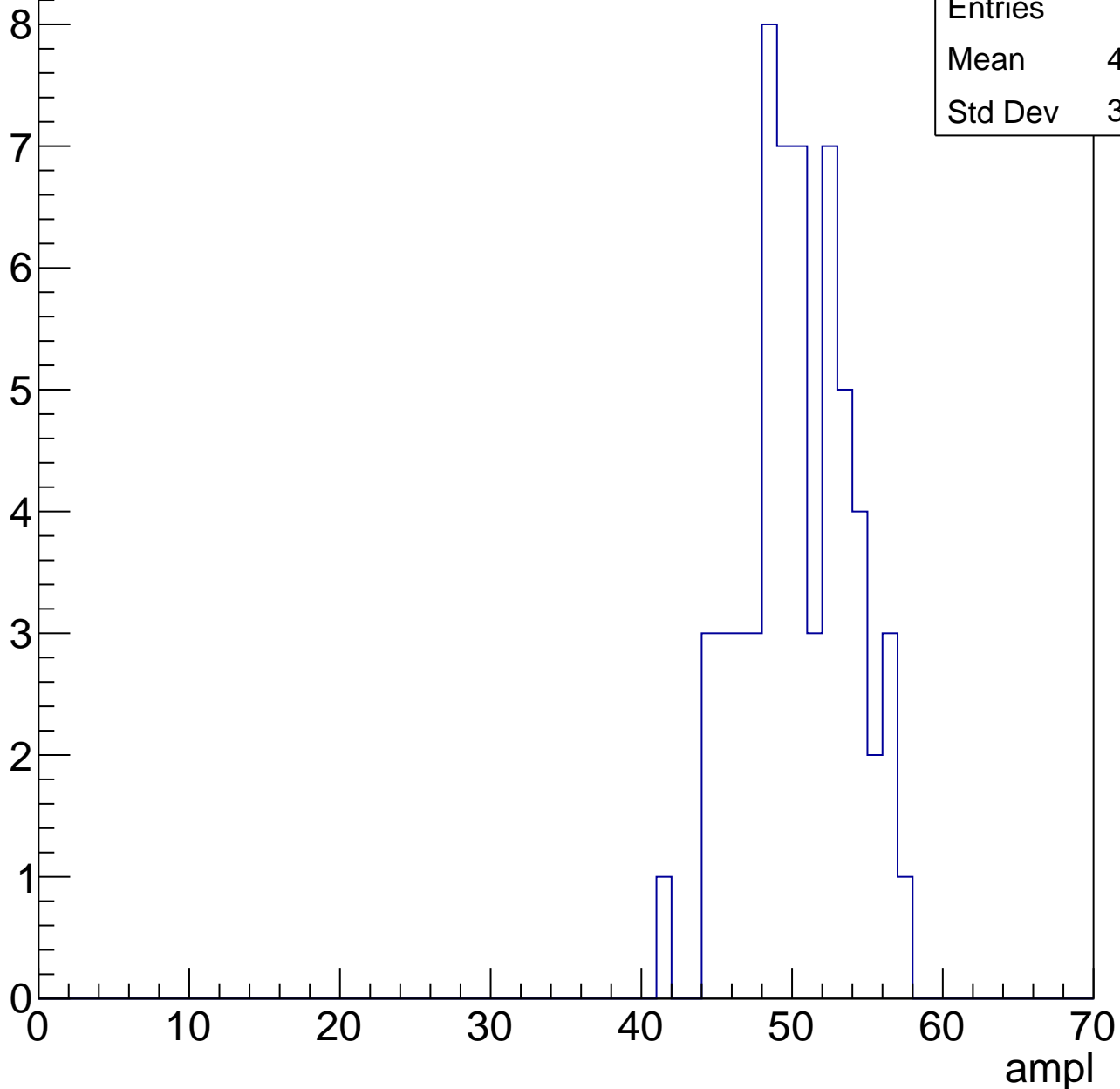


# B0L001S, U10-ch106, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

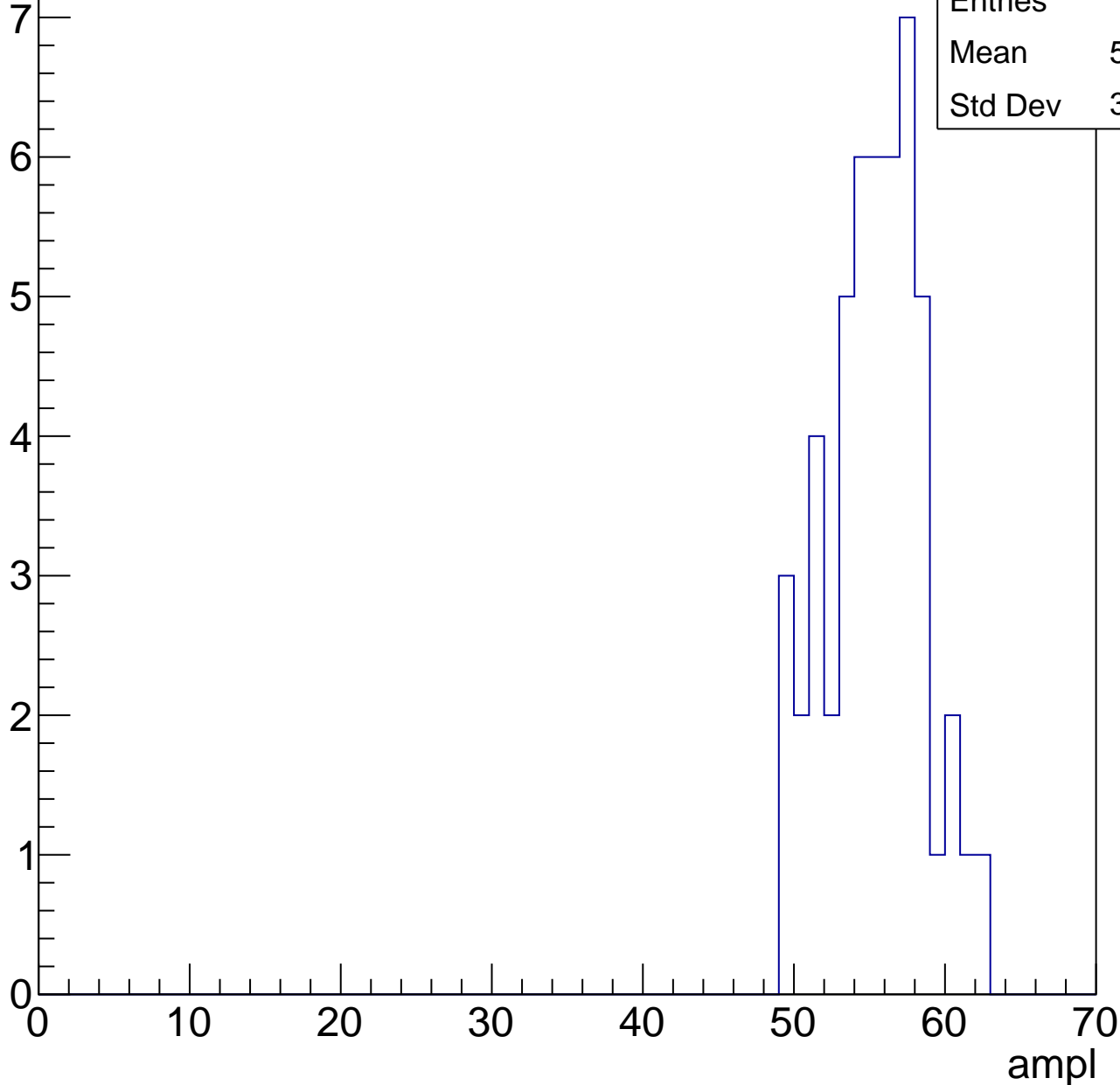
Entries	60
Mean	49.95
Std Dev	3.476



# B0L001S, U10-ch106, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

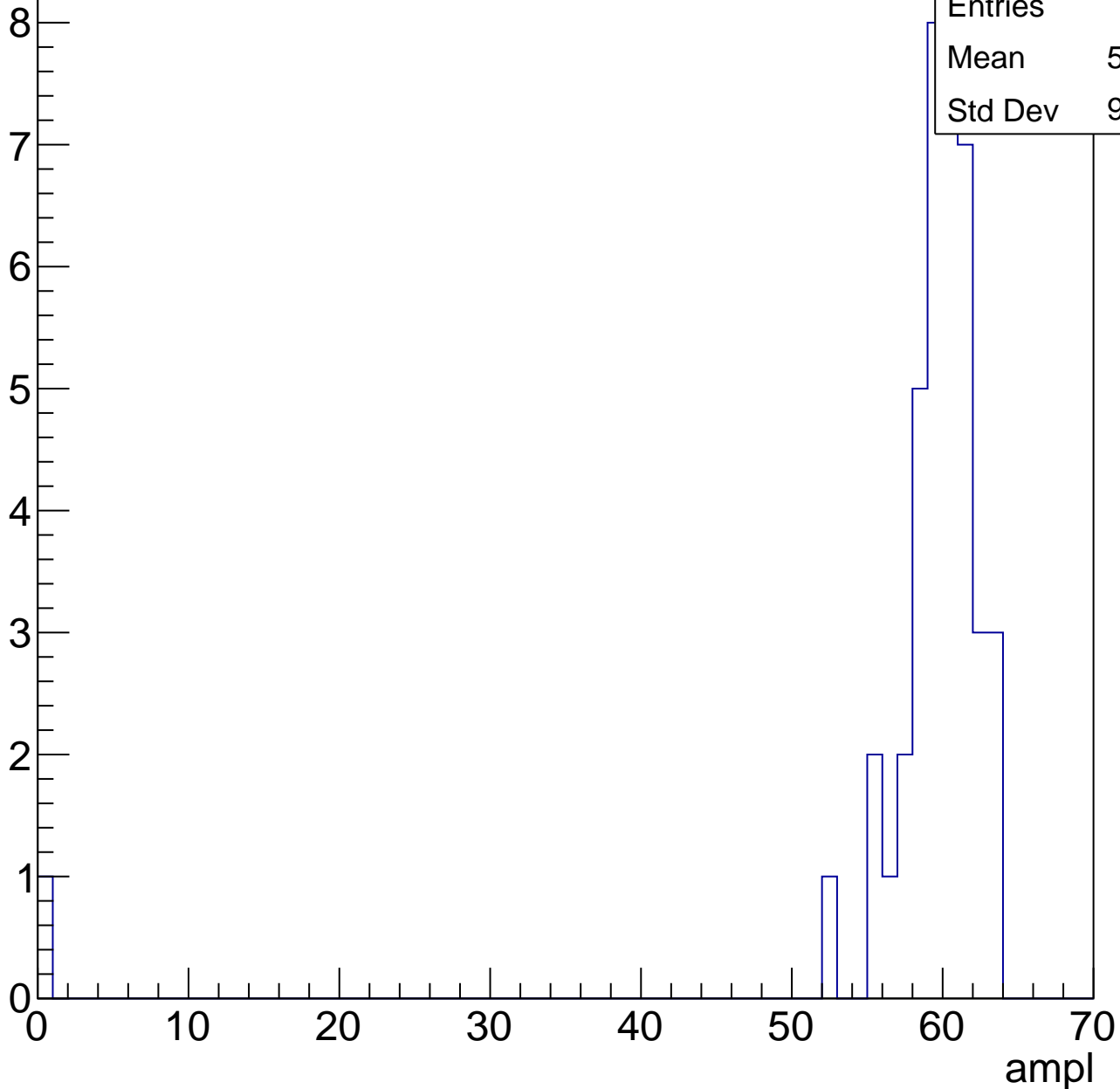


# B0L001S, U10-ch106, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	41
Mean	57.95
Std Dev	9.435

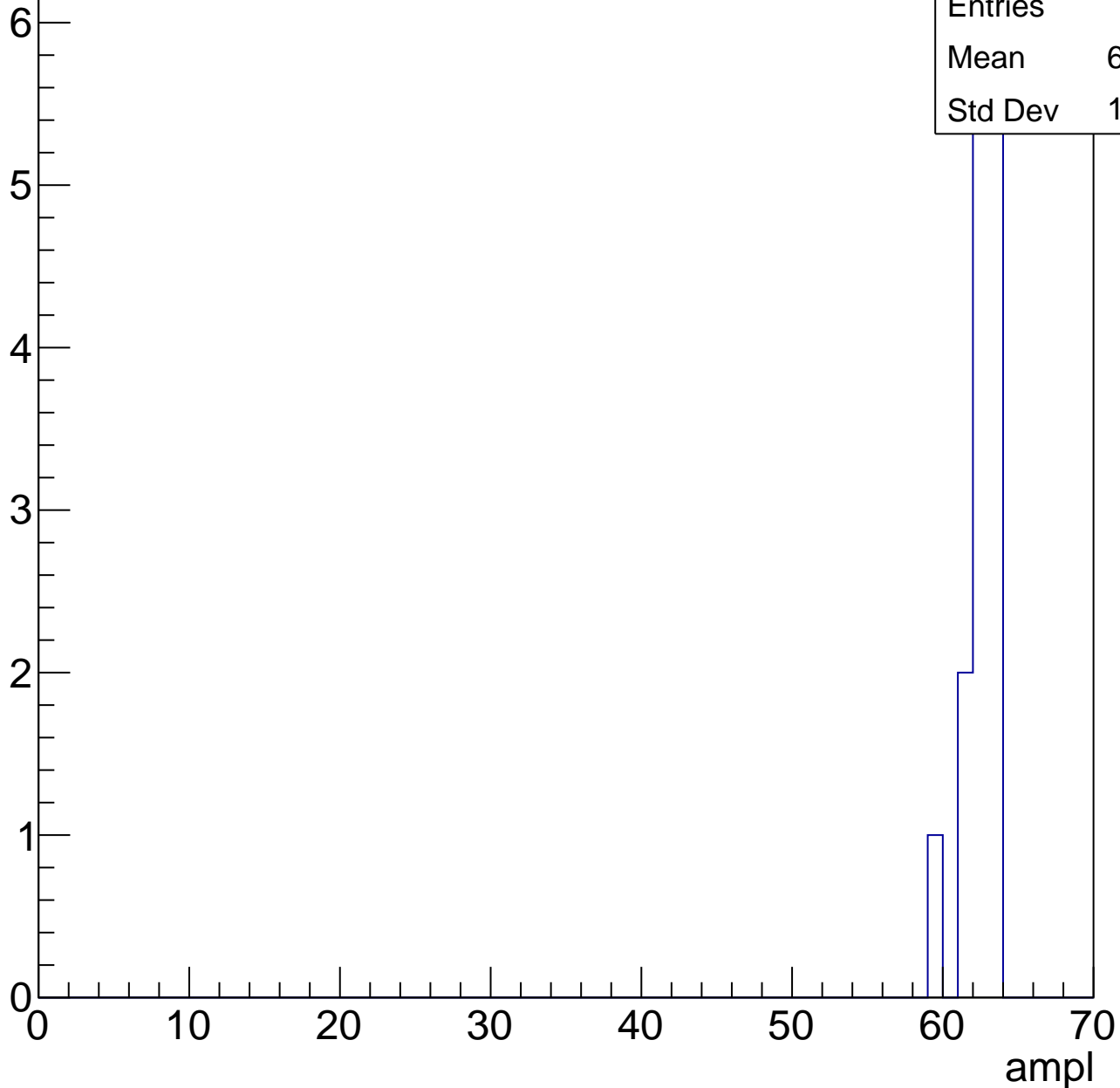


# B0L001S, U10-ch106, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	15
Mean	62.07
Std Dev	1.062





# B0L001S, U10-ch106, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U10-ch107, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	70
Mean	30.36
Std Dev	8.085

**Gaus mean : 32.6442**

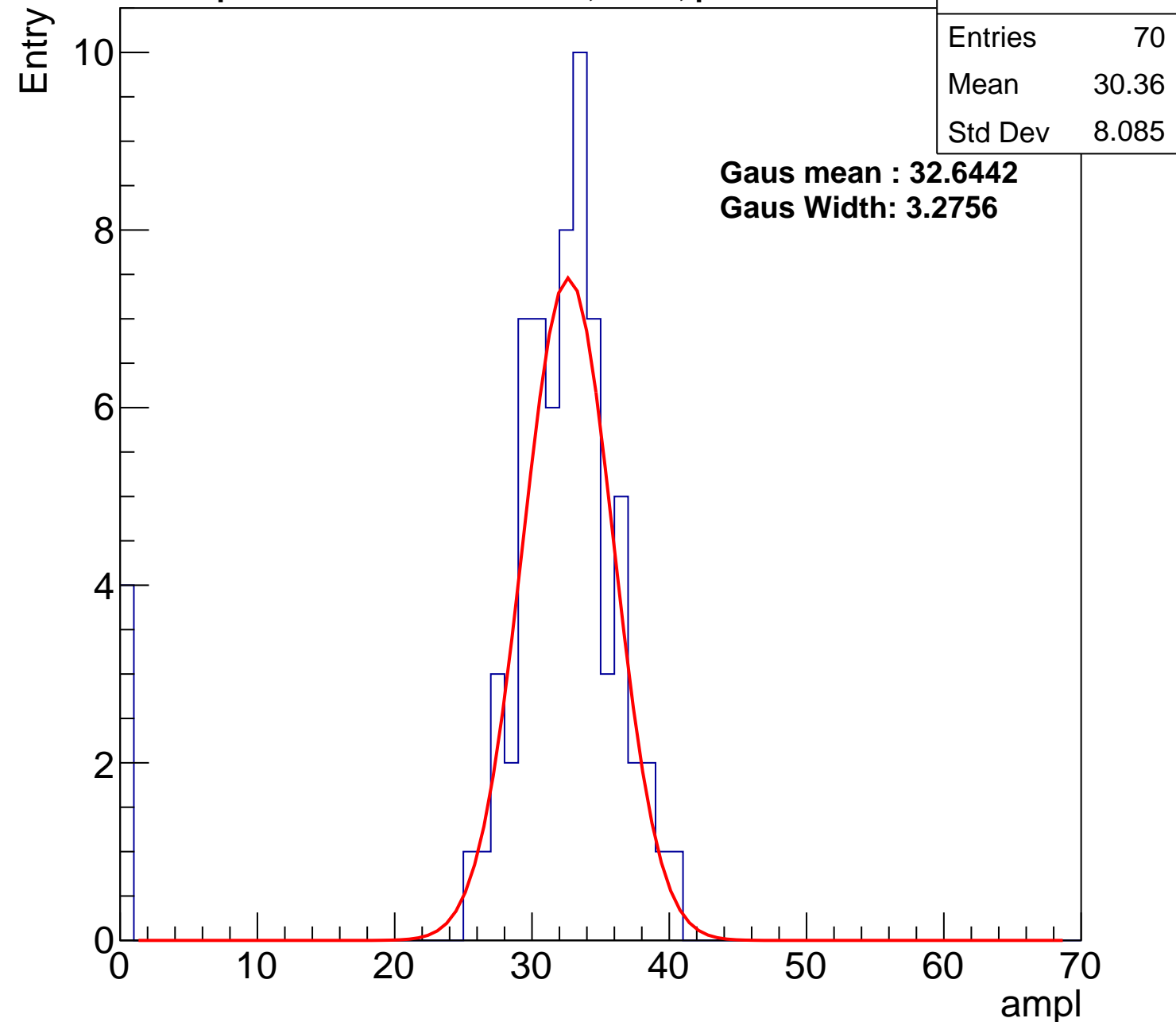
**Gaus Width: 3.2756**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U10-ch107, adc1

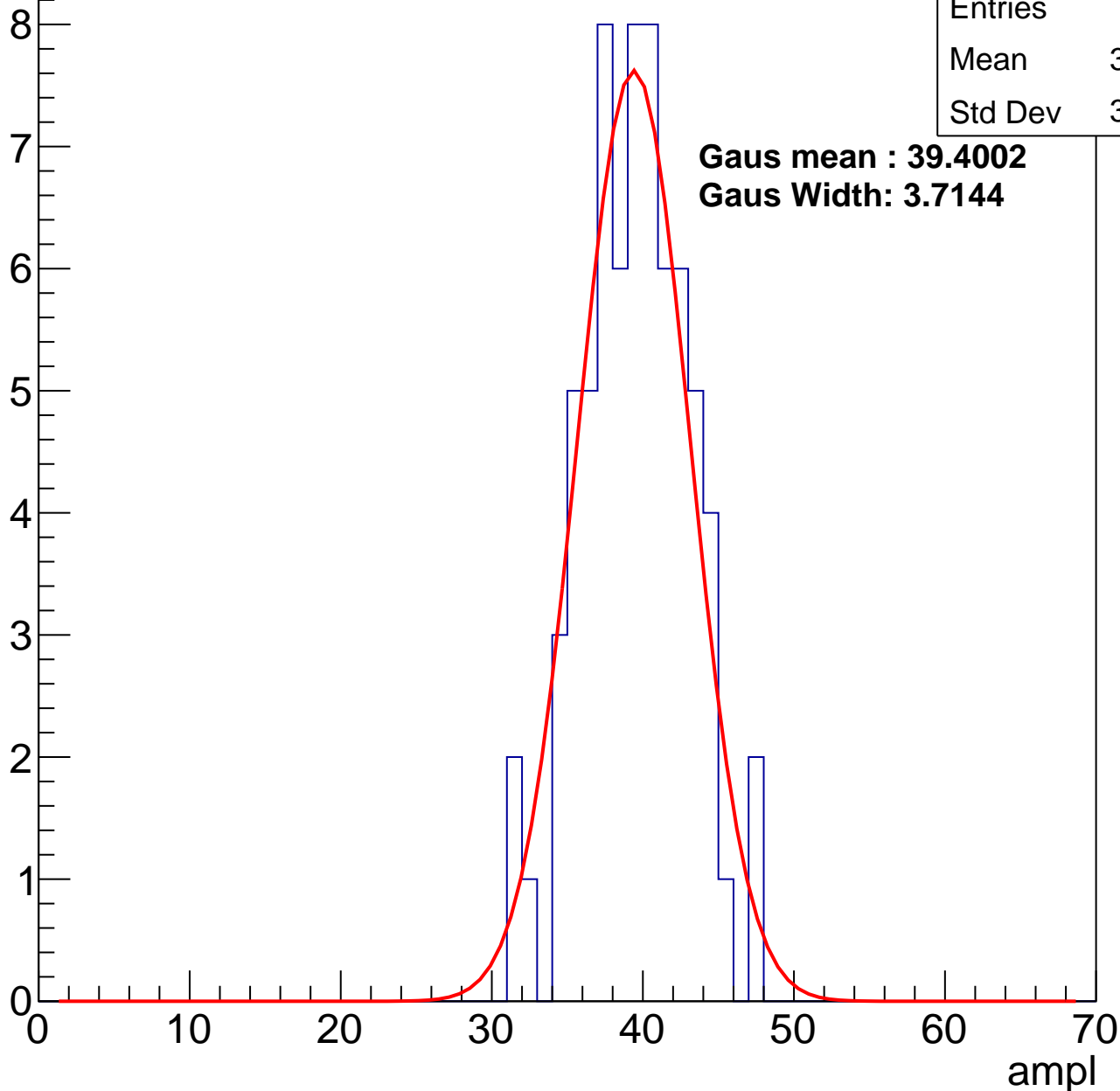
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	39.07
Std Dev	3.474

**Gaus mean : 39.4002**

**Gaus Width: 3.7144**



# B0L001S, U10-ch107, adc2

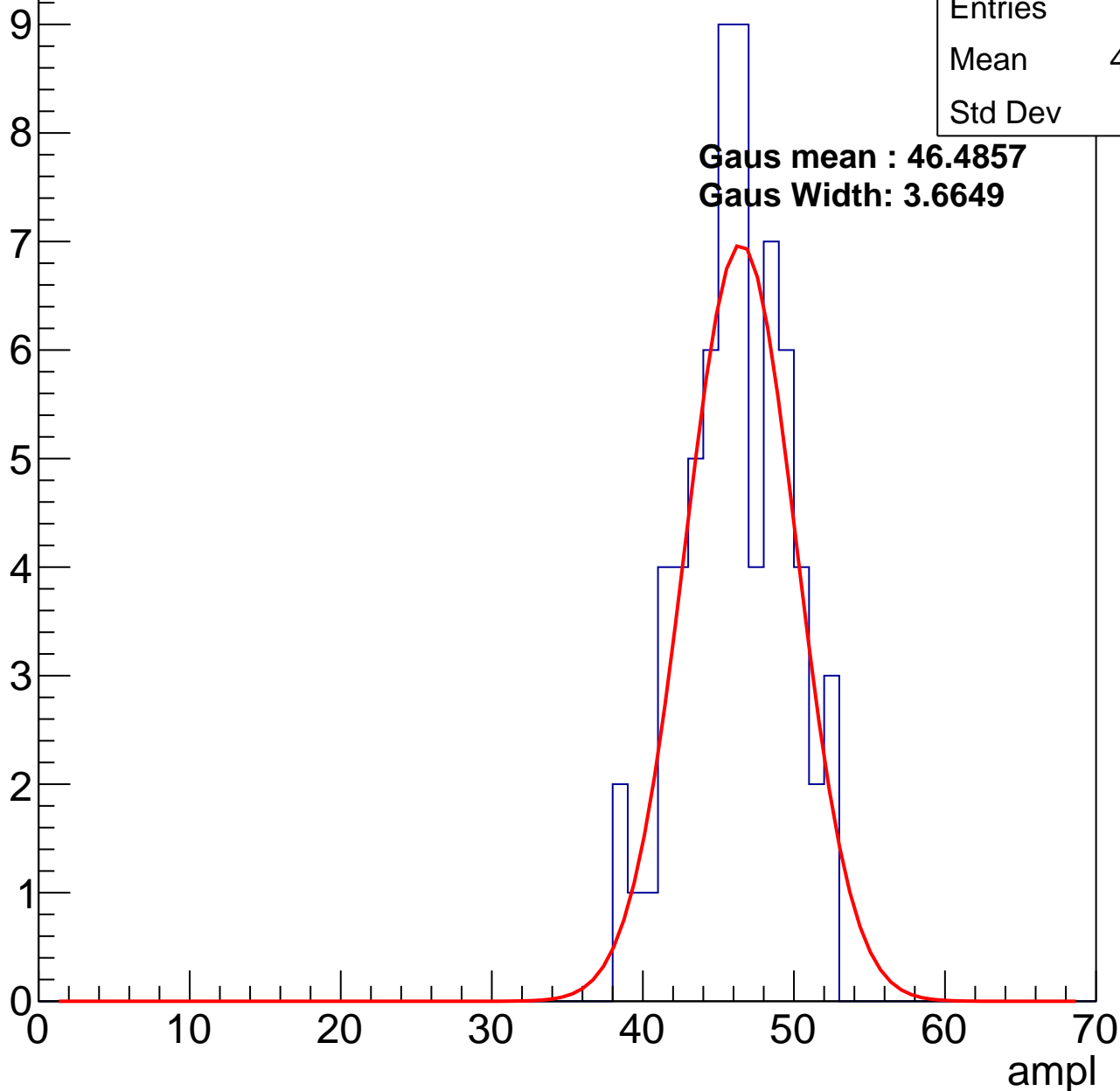
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	45.69
Std Dev	3.36

**Gaus mean : 46.4857**

**Gaus Width: 3.6649**

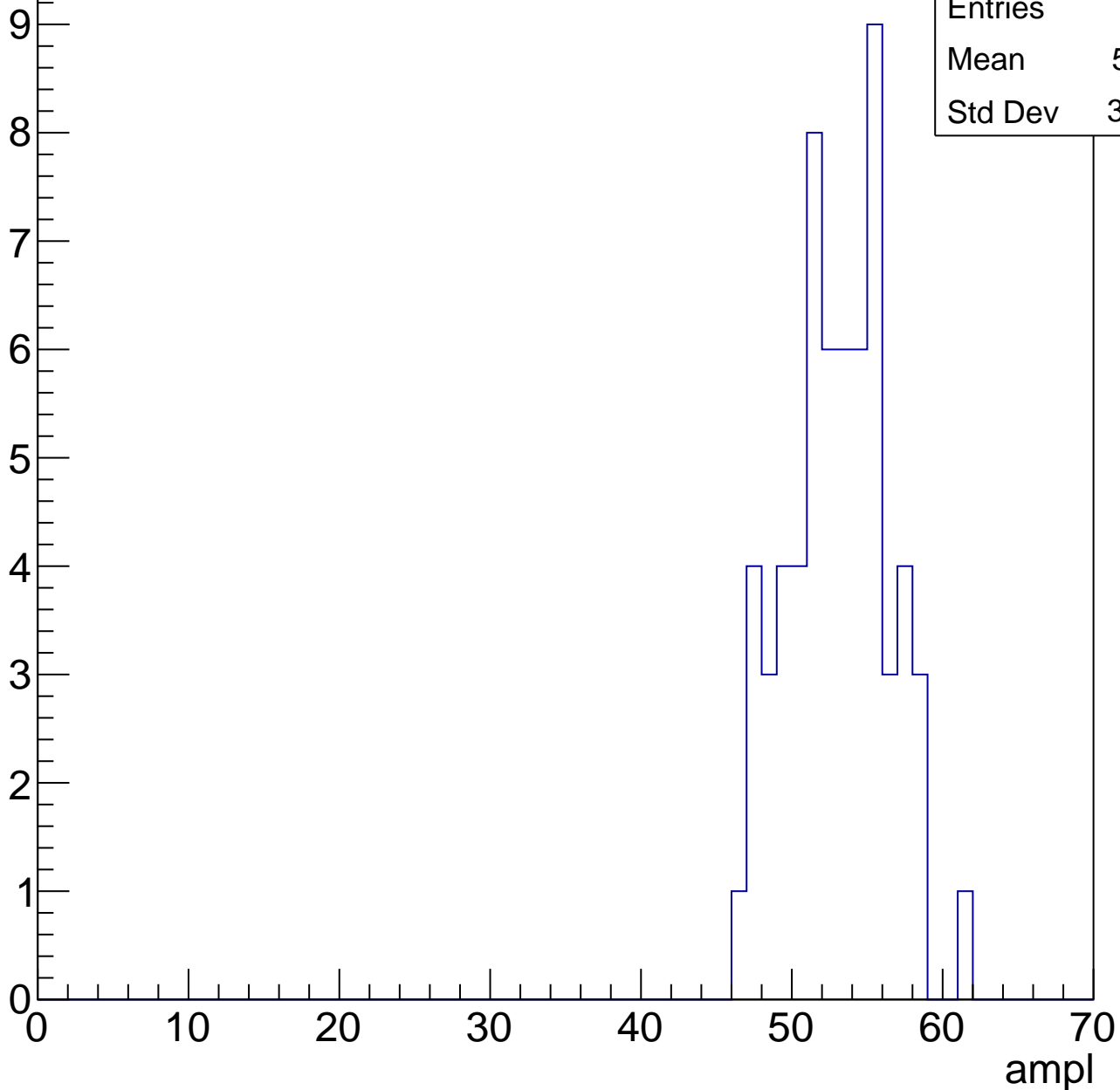


# B0L001S, U10-ch107, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	52.61
Std Dev	3.284

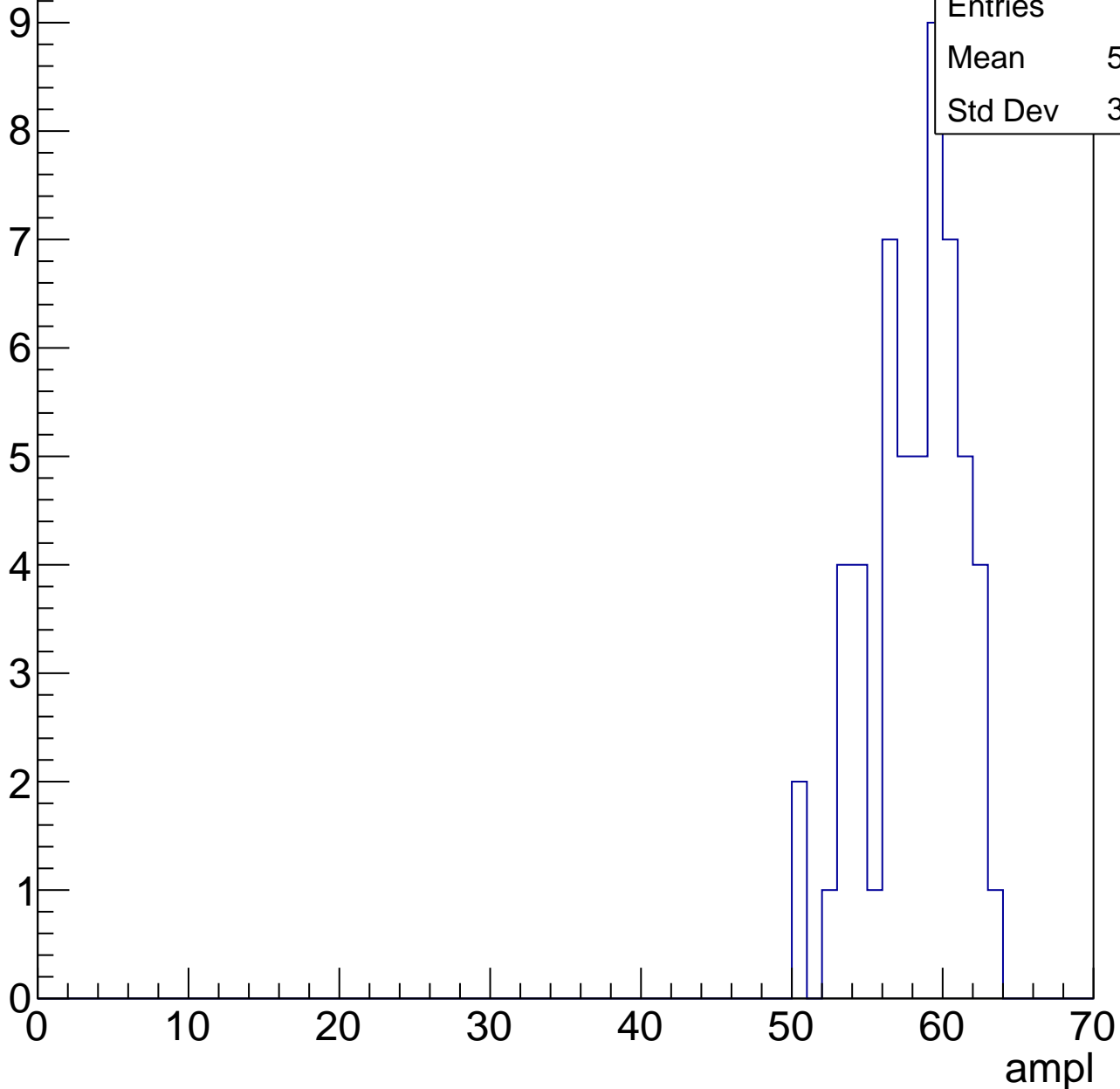


# B0L001S, U10-ch107, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	57.62
Std Dev	3.113

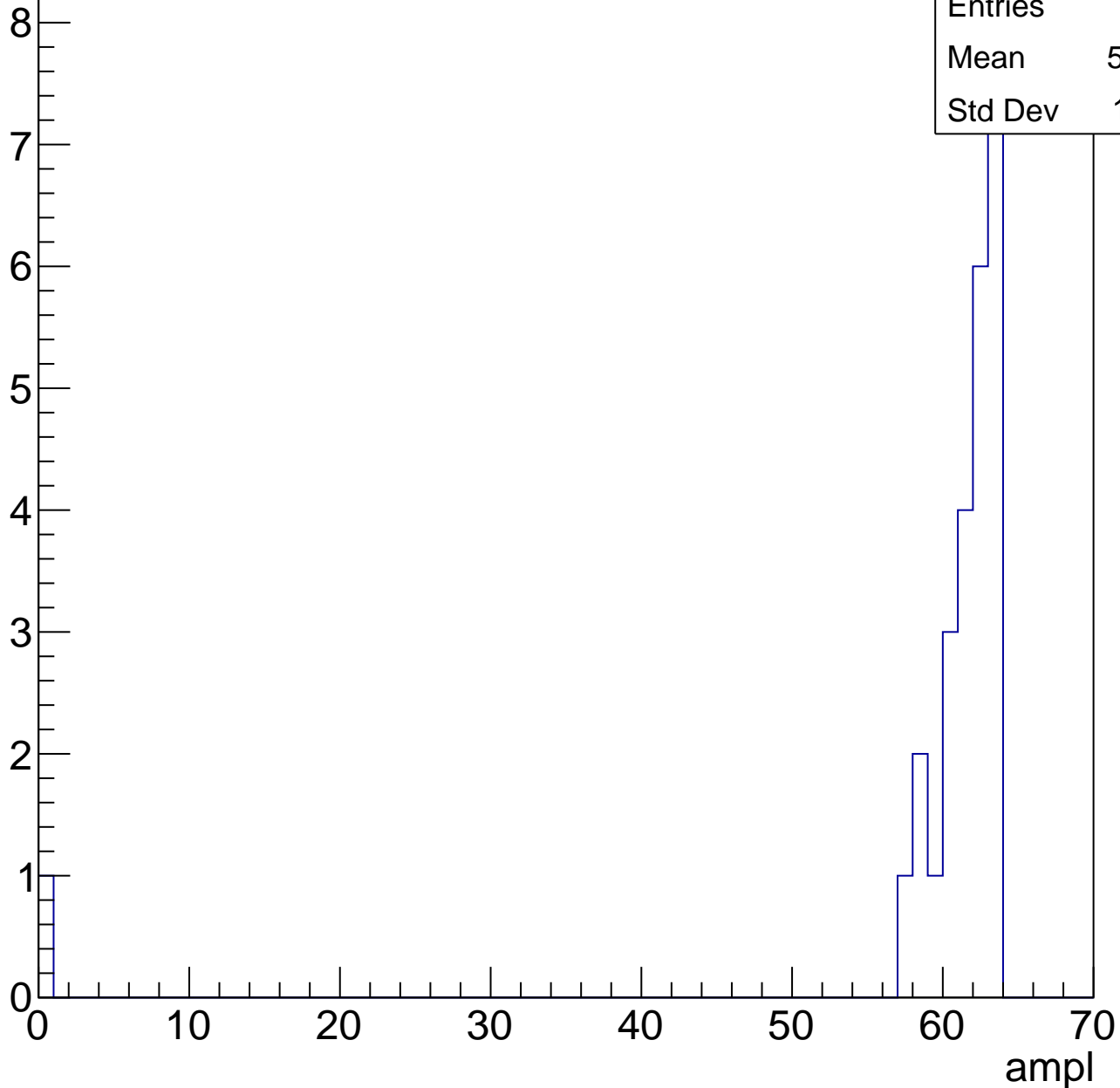


# B0L001S, U10-ch107, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	26
Mean	58.92
Std Dev	11.91



# B0L001S, U10-ch107, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch107, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U10-ch108, adc0

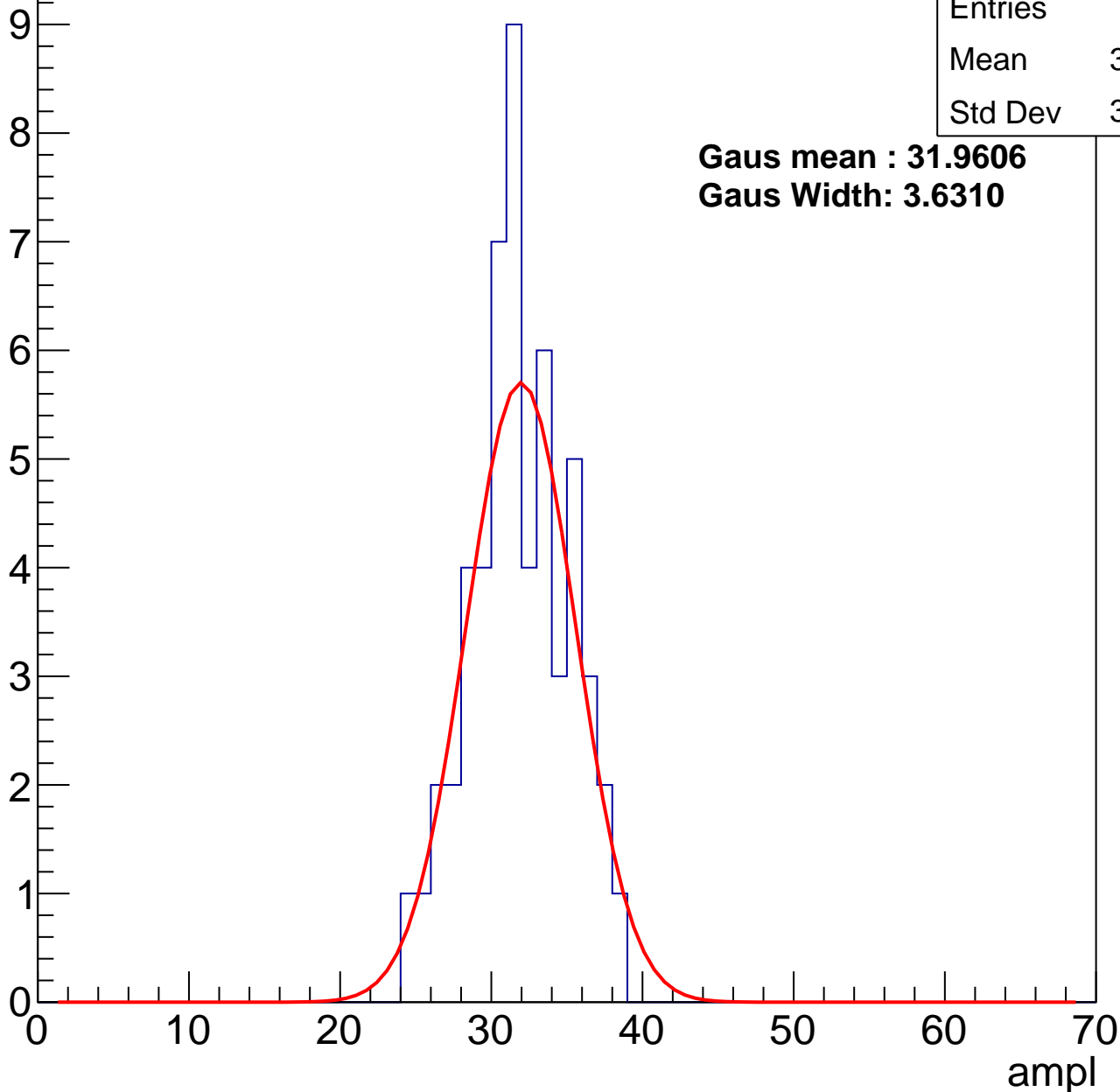
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	31.39
Std Dev	3.188

**Gaus mean : 31.9606**

**Gaus Width: 3.6310**



# B0L001S, U10-ch108, adc1

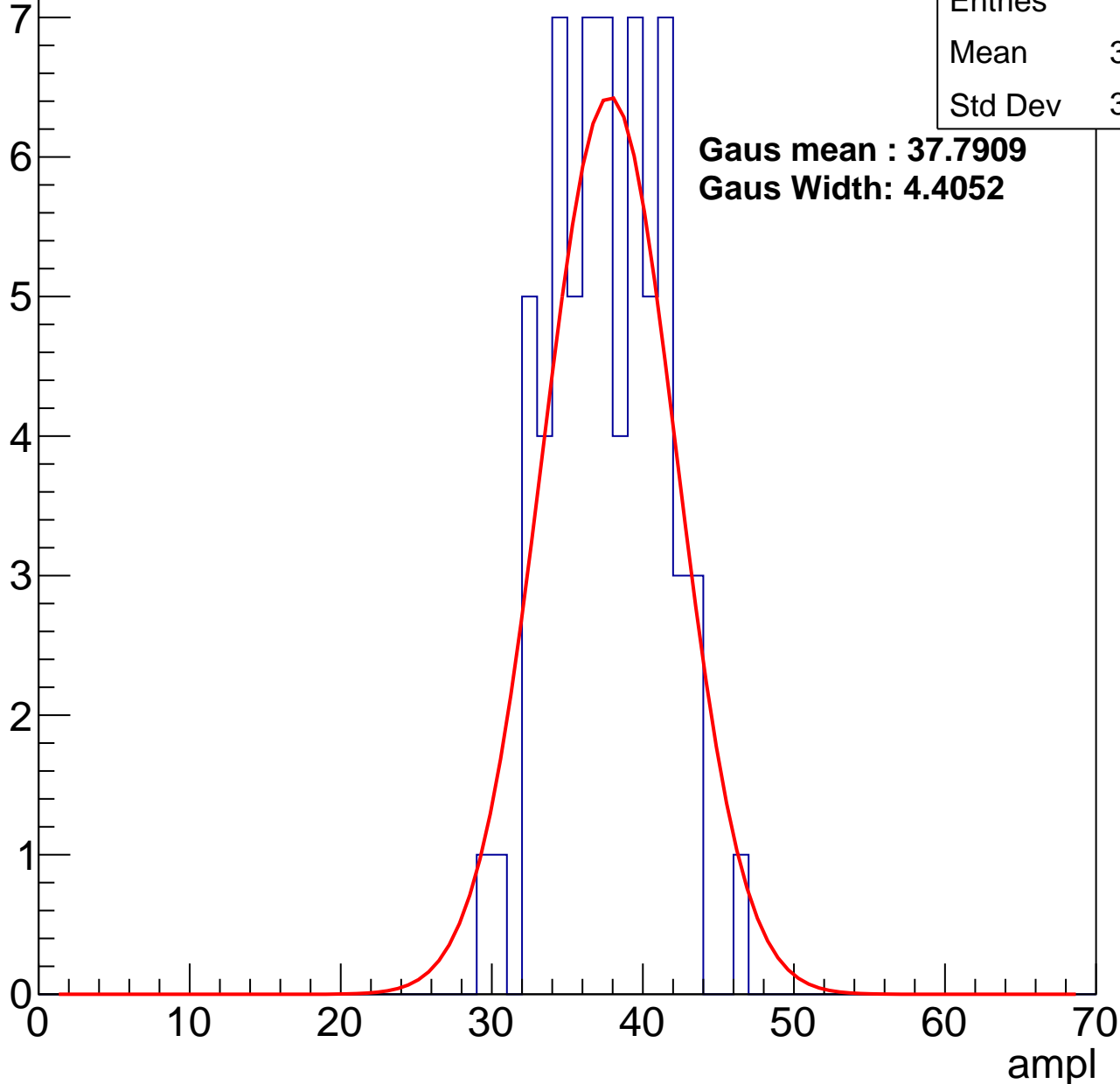
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	37.13
Std Dev	3.549

**Gaus mean : 37.7909**

**Gaus Width: 4.4052**



# B0L001S, U10-ch108, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	68
Mean	43.84
Std Dev	3.534

**Gaus mean : 44.3210**

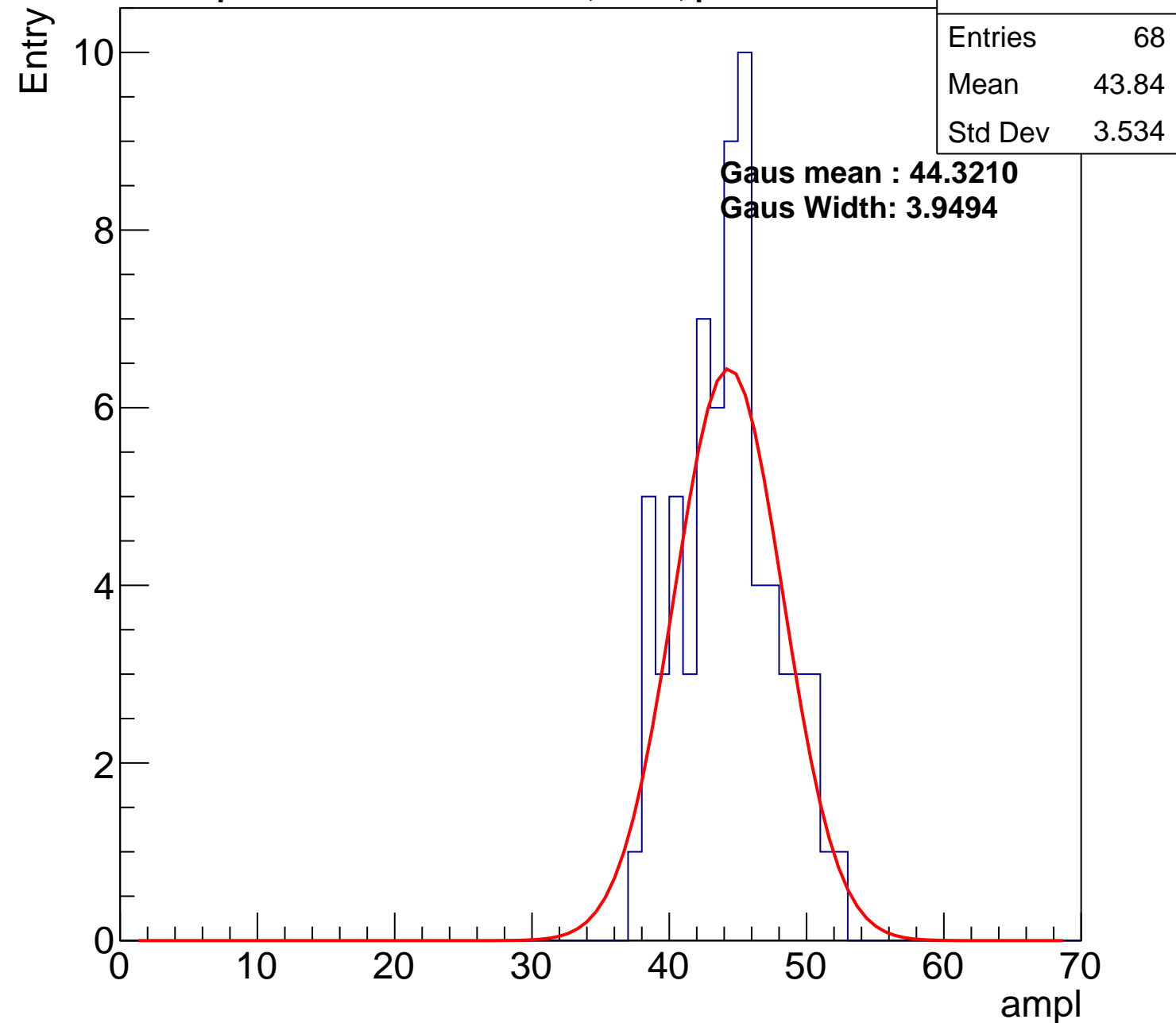
**Gaus Width: 3.9494**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

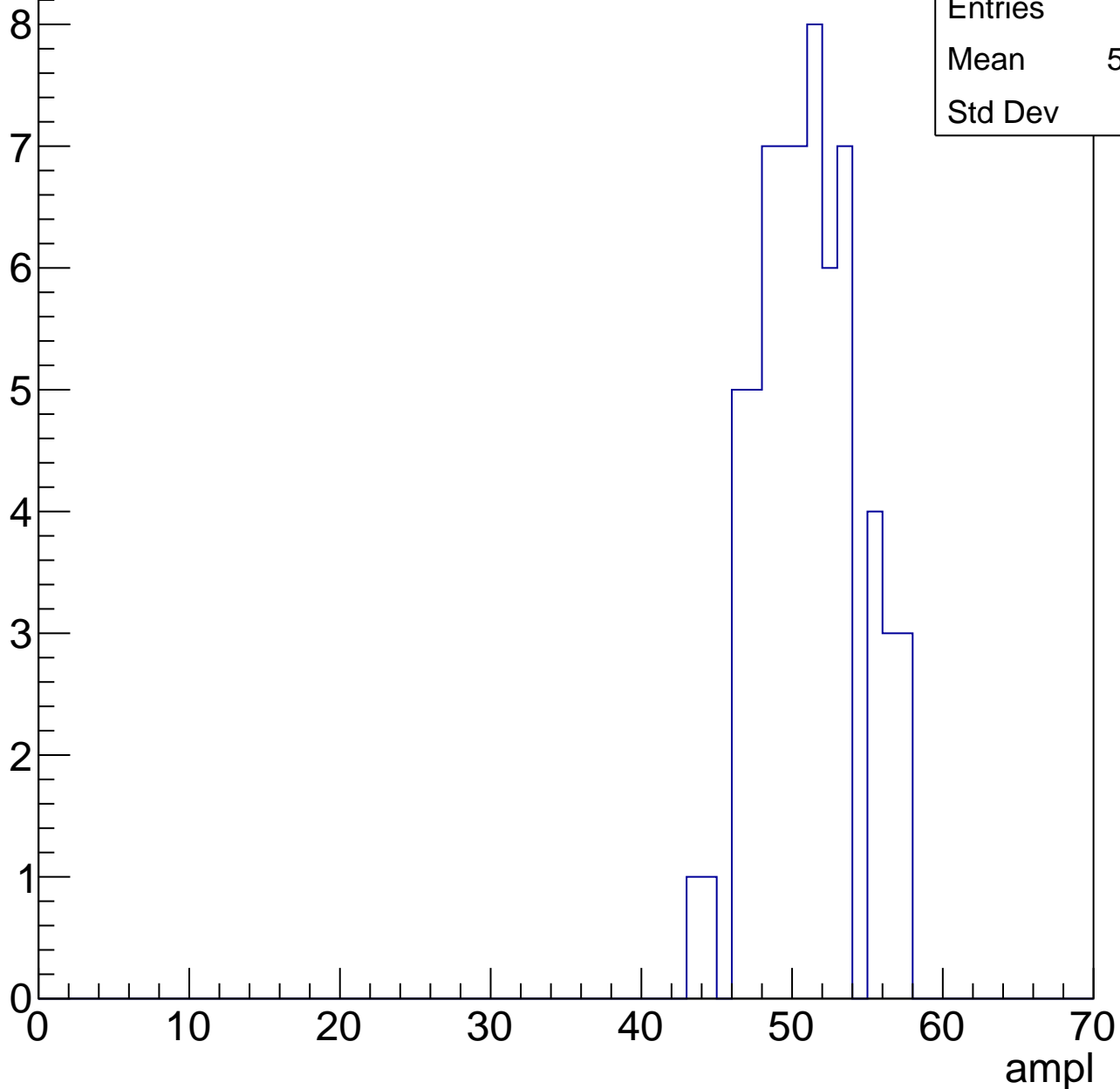


# B0L001S, U10-ch108, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	50.48
Std Dev	3.26

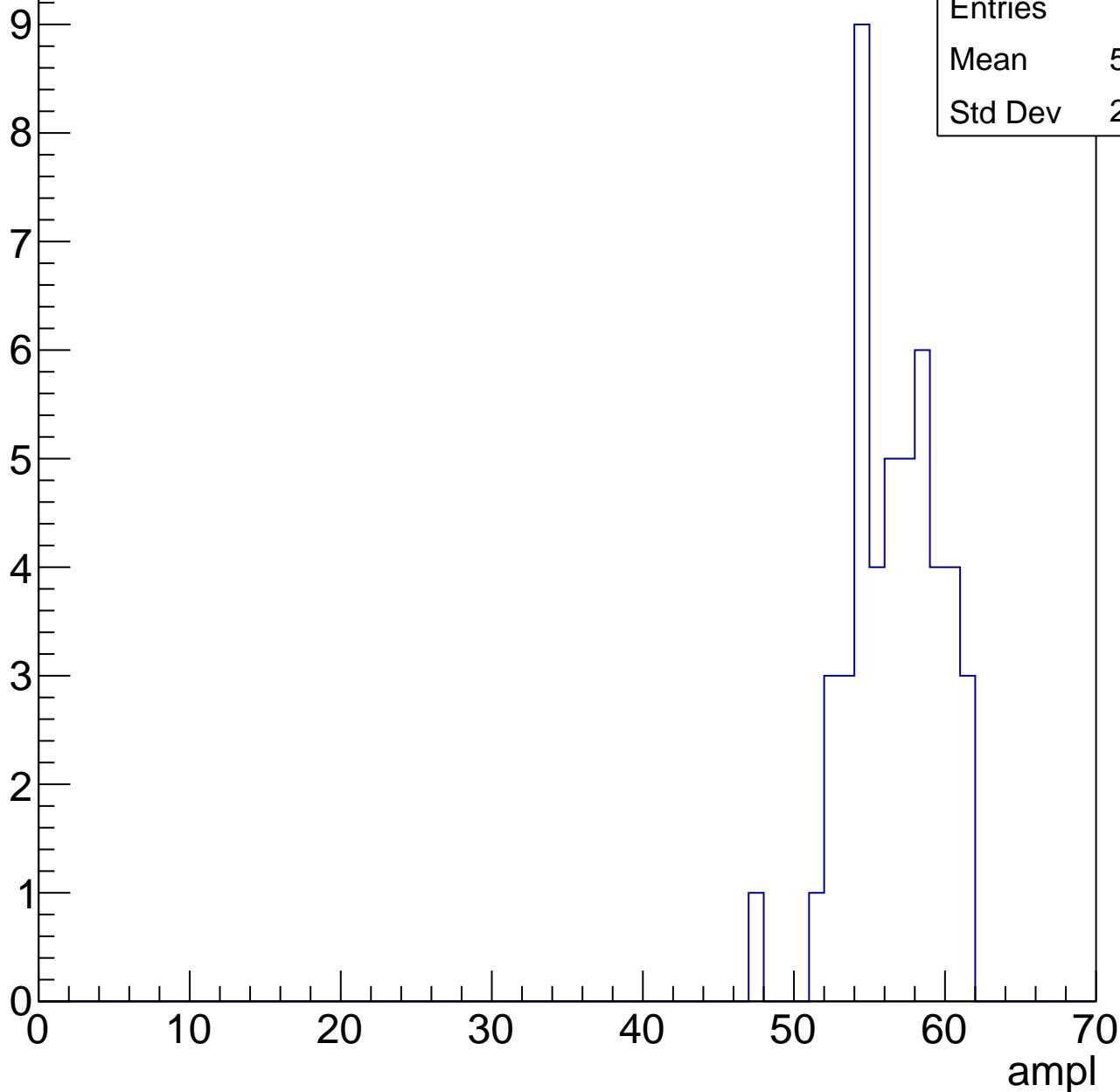


# B0L001S, U10-ch108, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	48
Mean	56.06
Std Dev	2.975

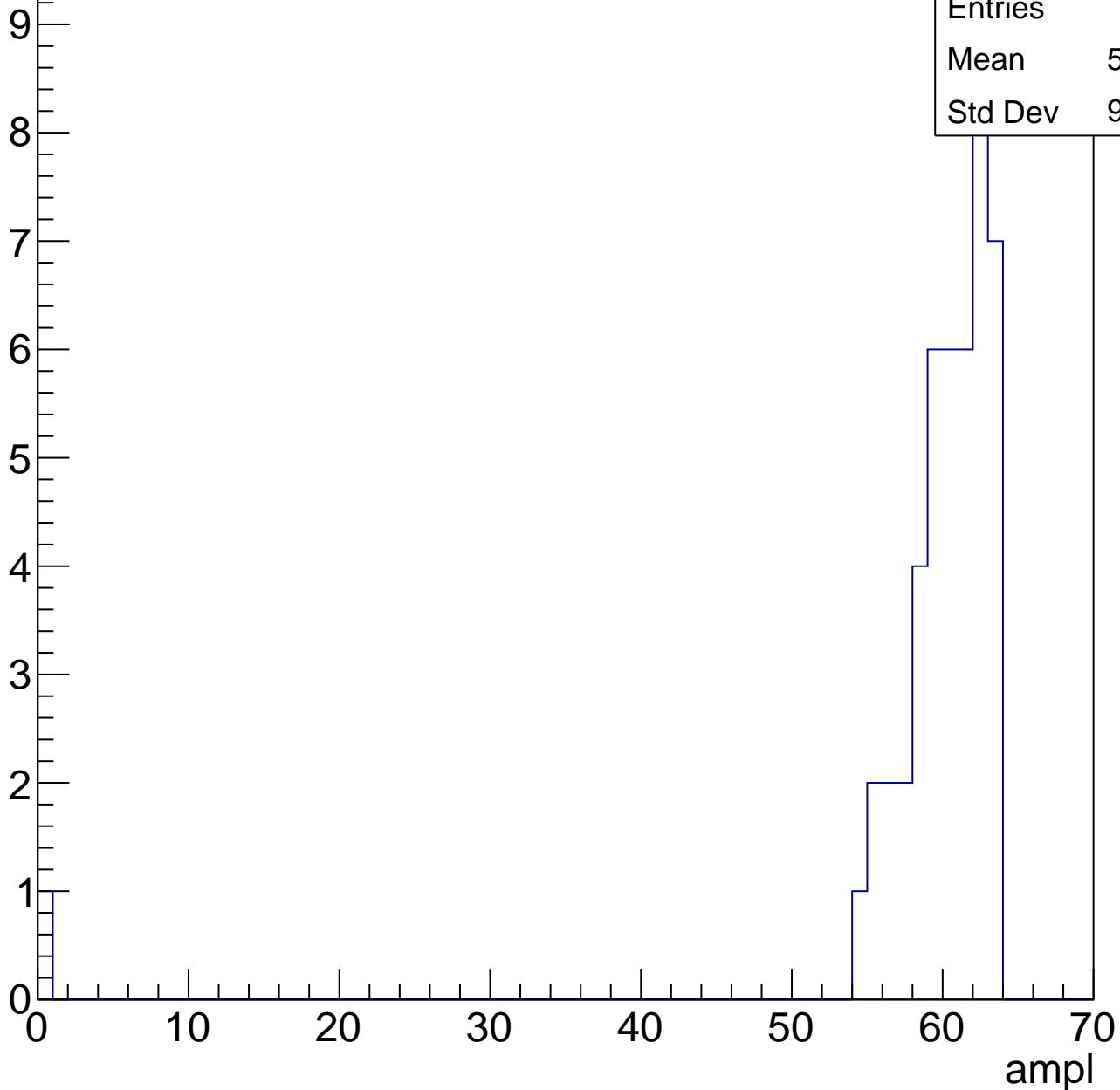


# B0L001S, U10-ch108, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

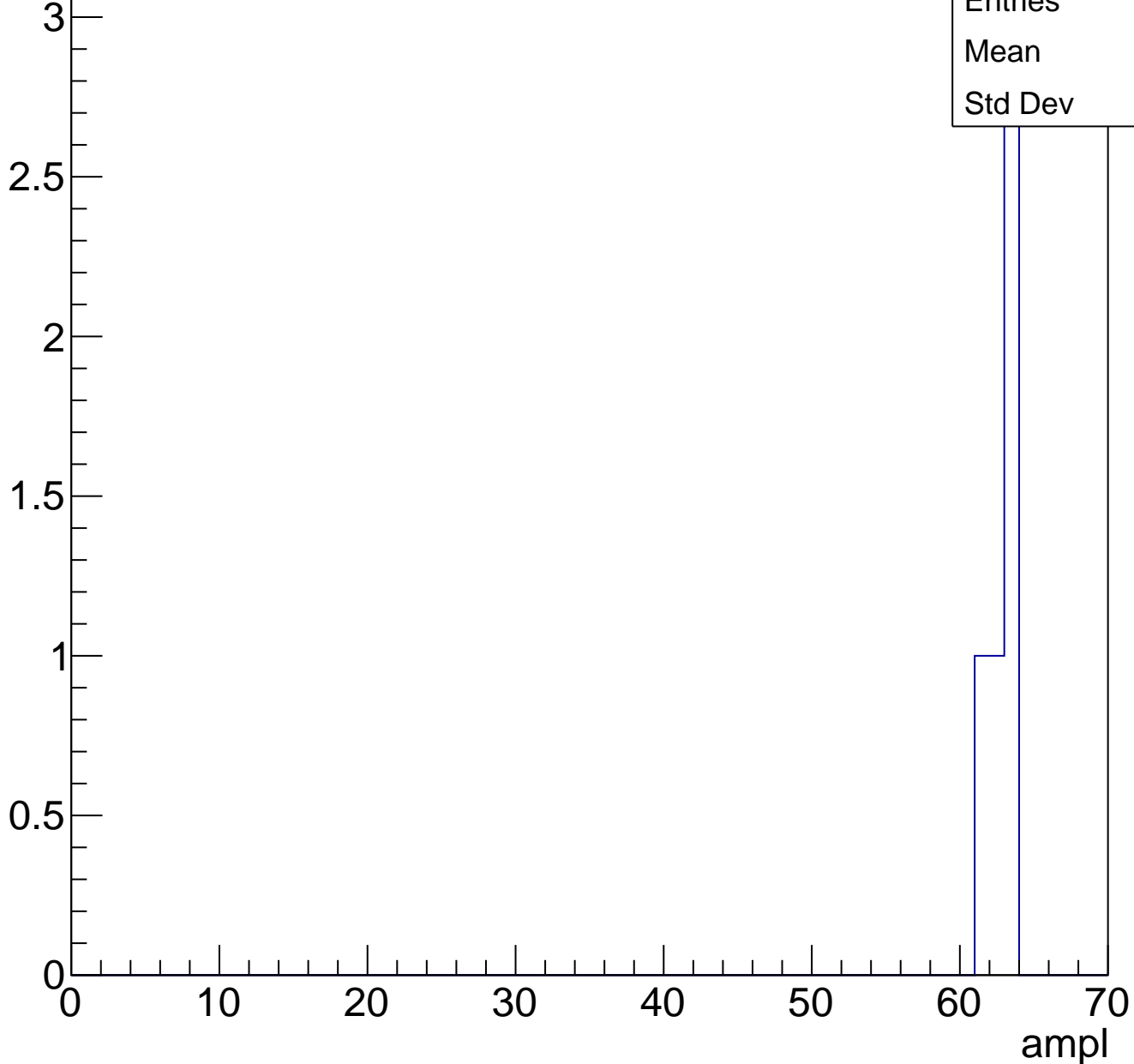
Entries	46
Mean	58.72
Std Dev	9.074



# B0L001S, U10-ch108, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch108, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U10-ch109, adc0

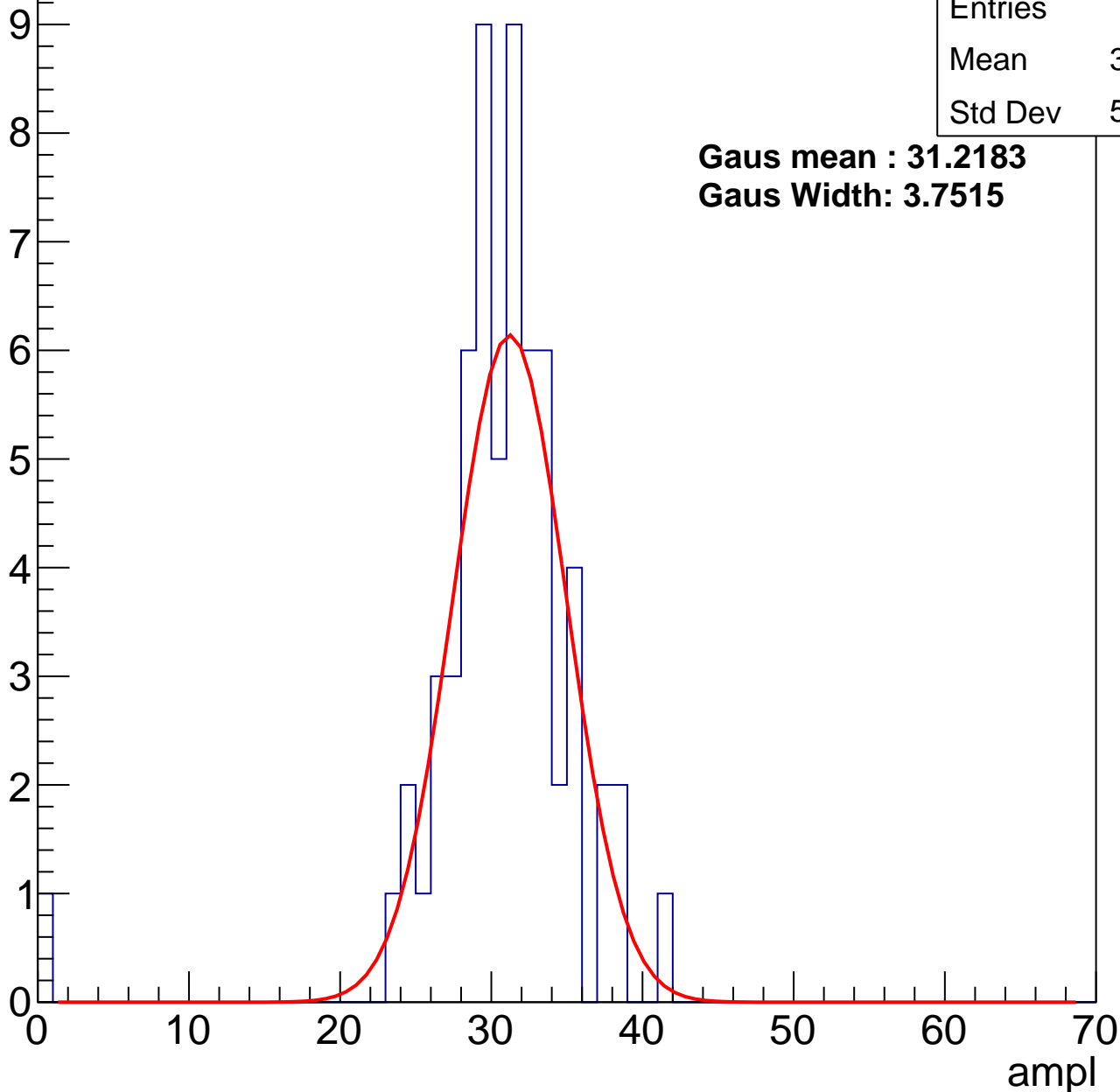
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	30.19
Std Dev	5.222

**Gaus mean : 31.2183**

**Gaus Width: 3.7515**



# B0L001S, U10-ch109, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	73
Mean	37.12
Std Dev	3.38

**Gaus mean : 37.4045**

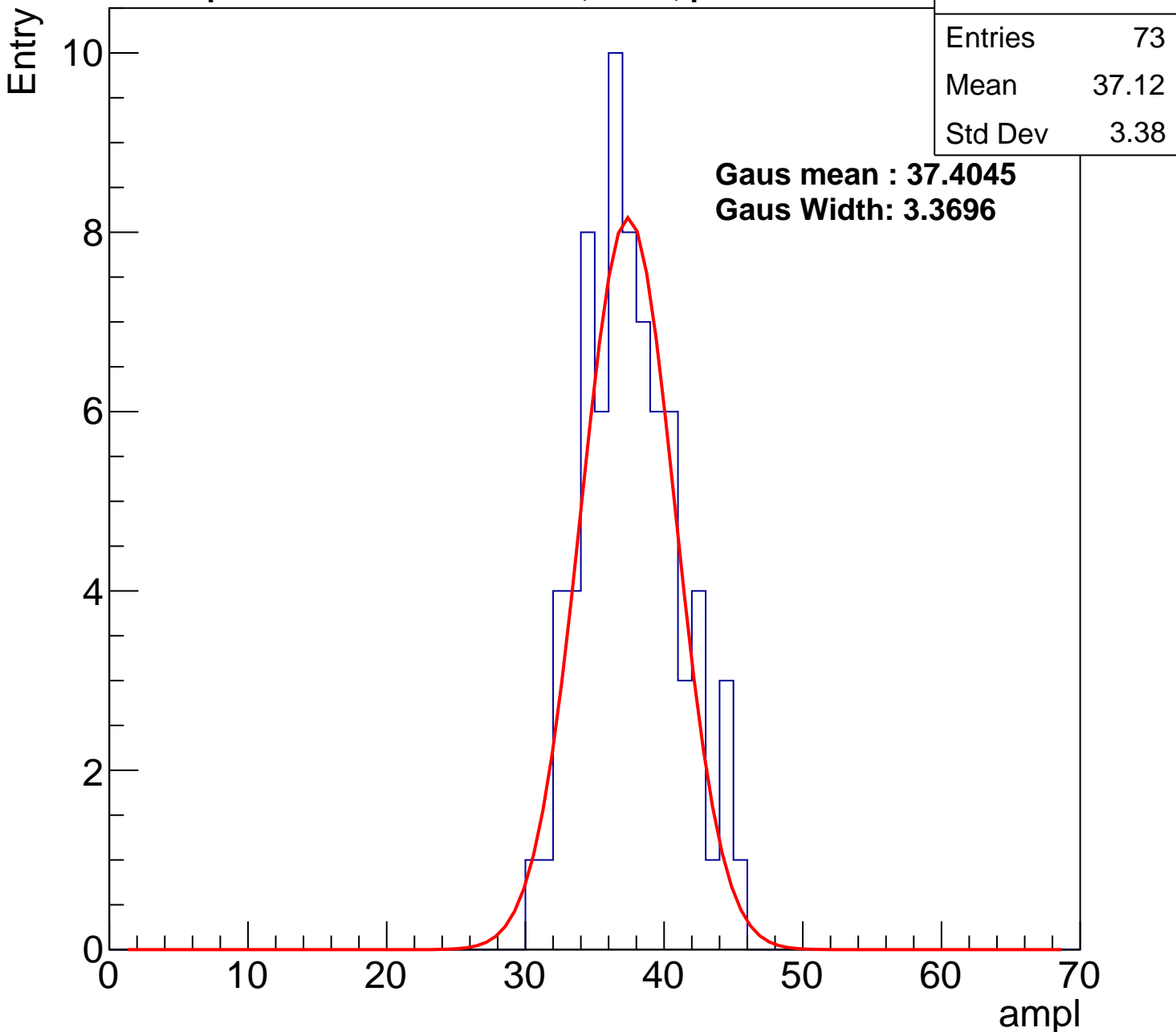
**Gaus Width: 3.3696**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B0L001S, U10-ch109, adc2

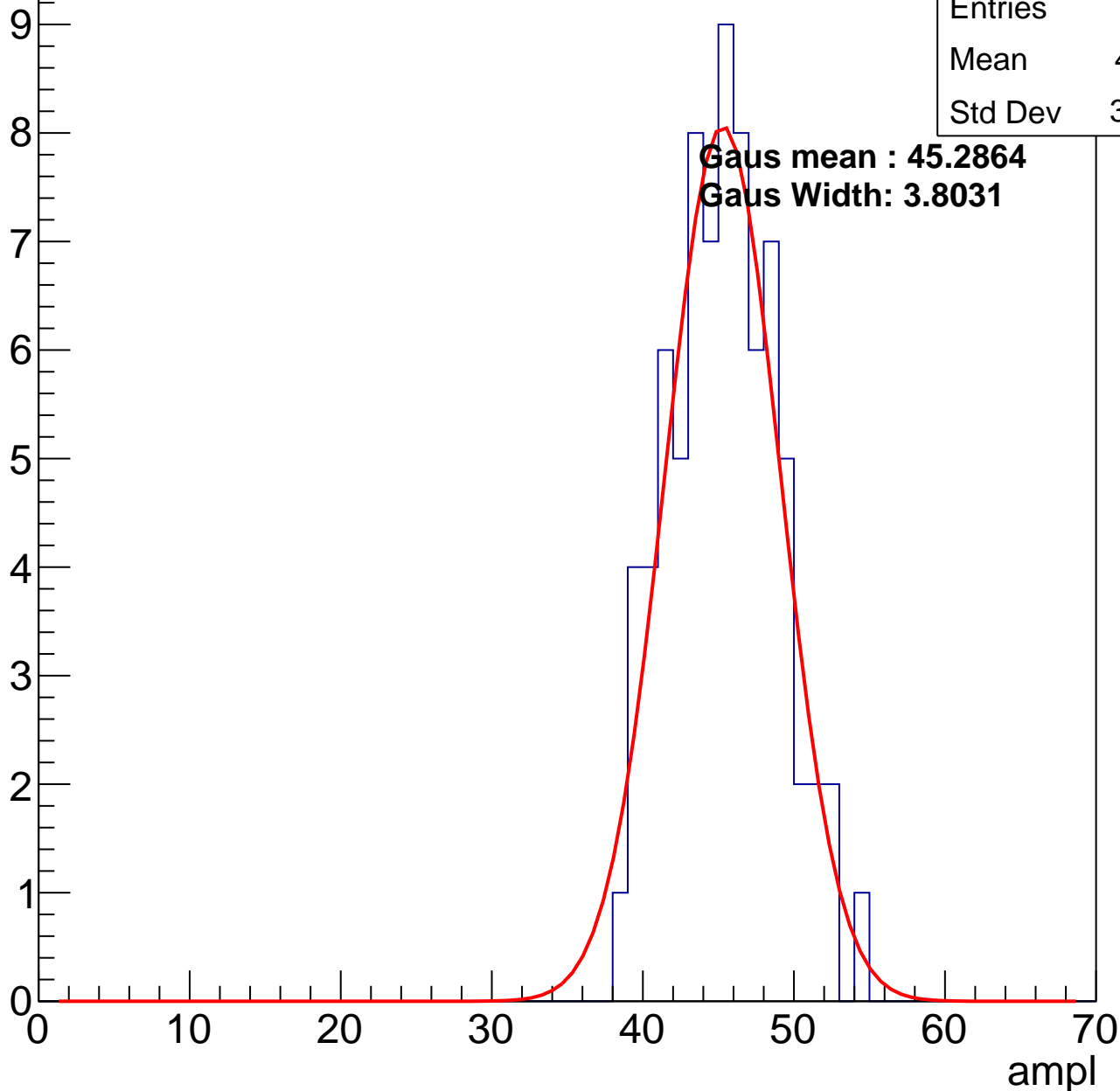
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	77
Mean	44.91
Std Dev	3.509

**Gaus mean : 45.2864**

**Gaus Width: 3.8031**

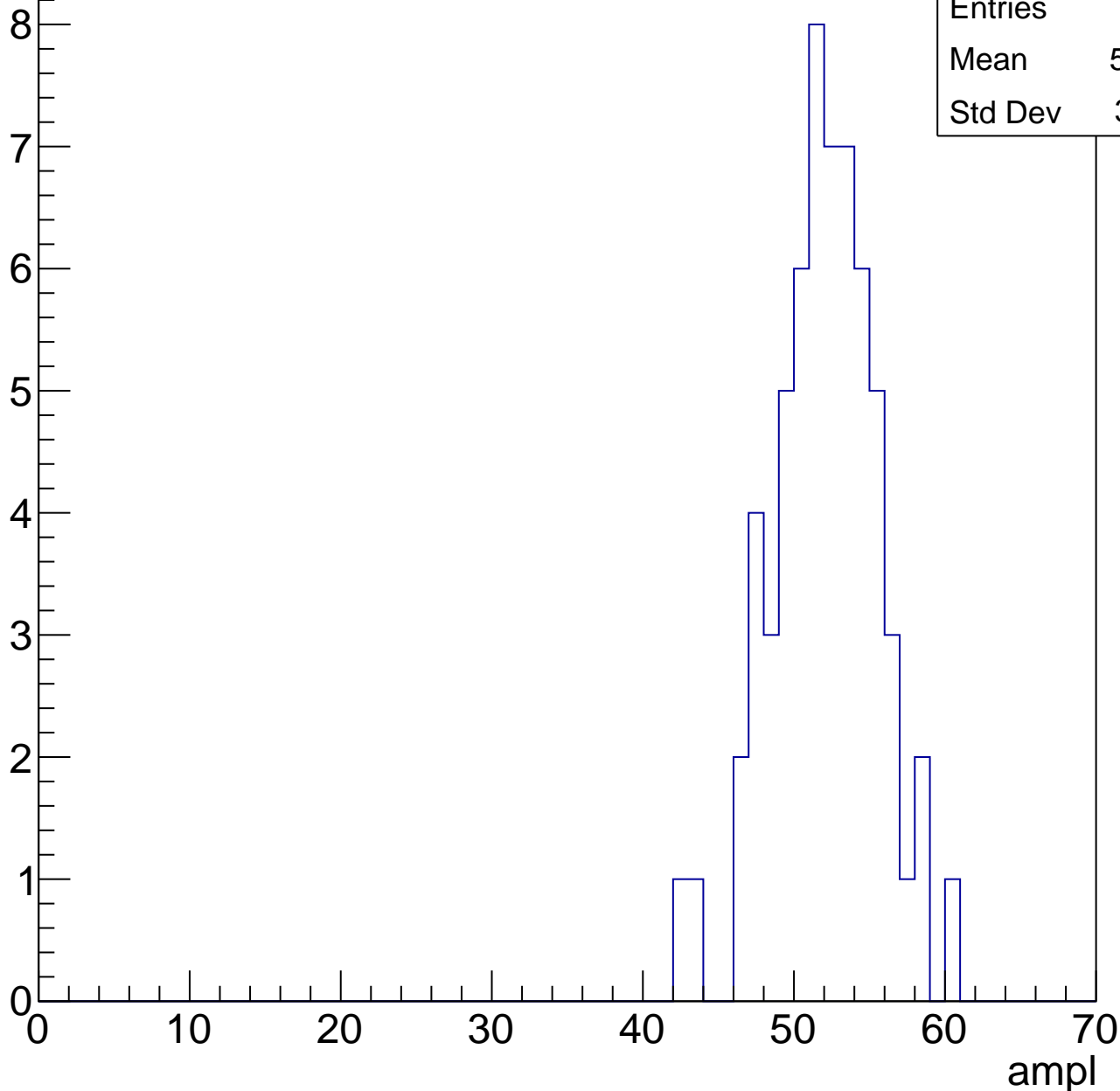


# B0L001S, U10-ch109, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	51.56
Std Dev	3.481

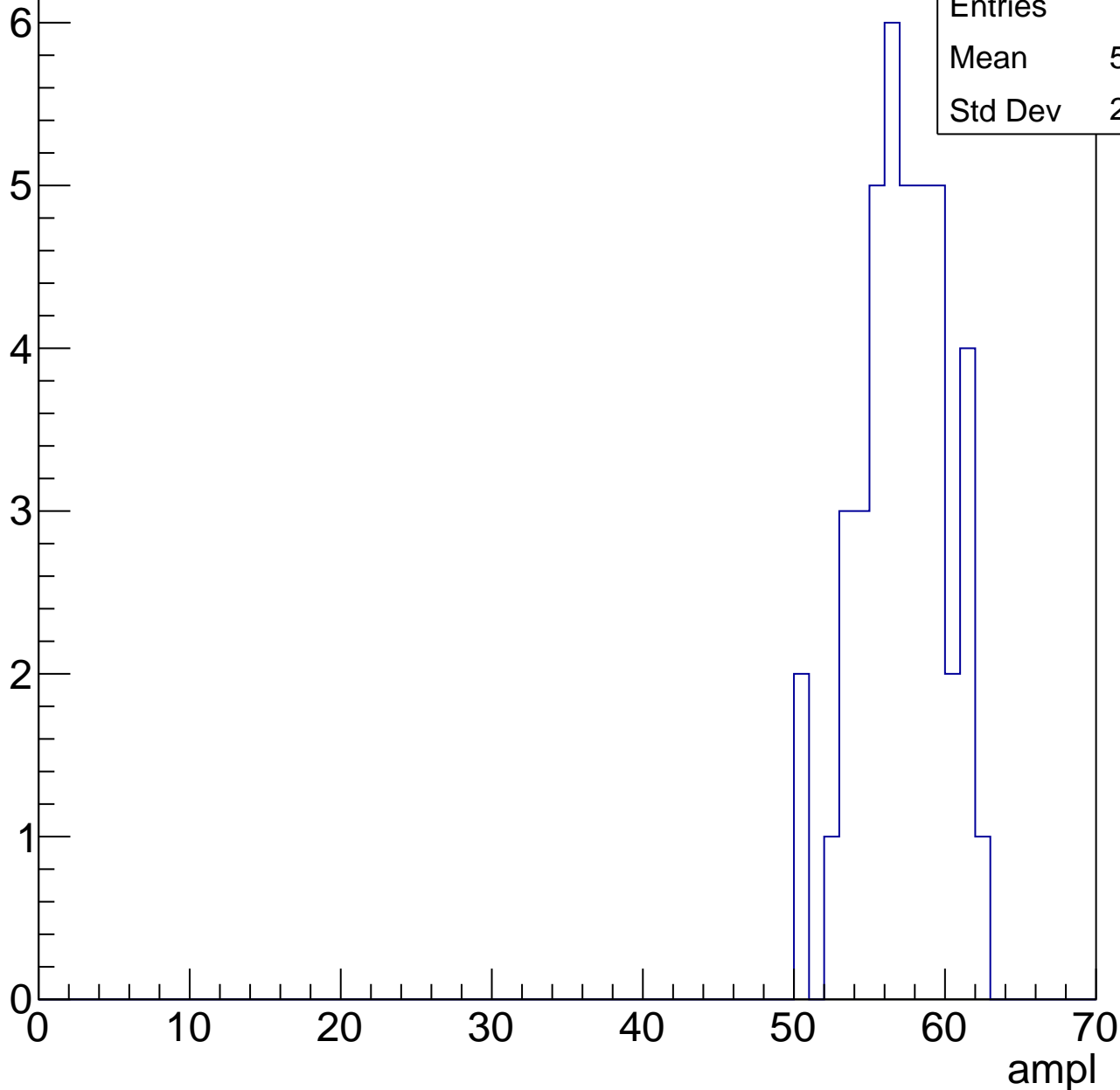


# B0L001S, U10-ch109, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	42
Mean	56.67
Std Dev	2.892

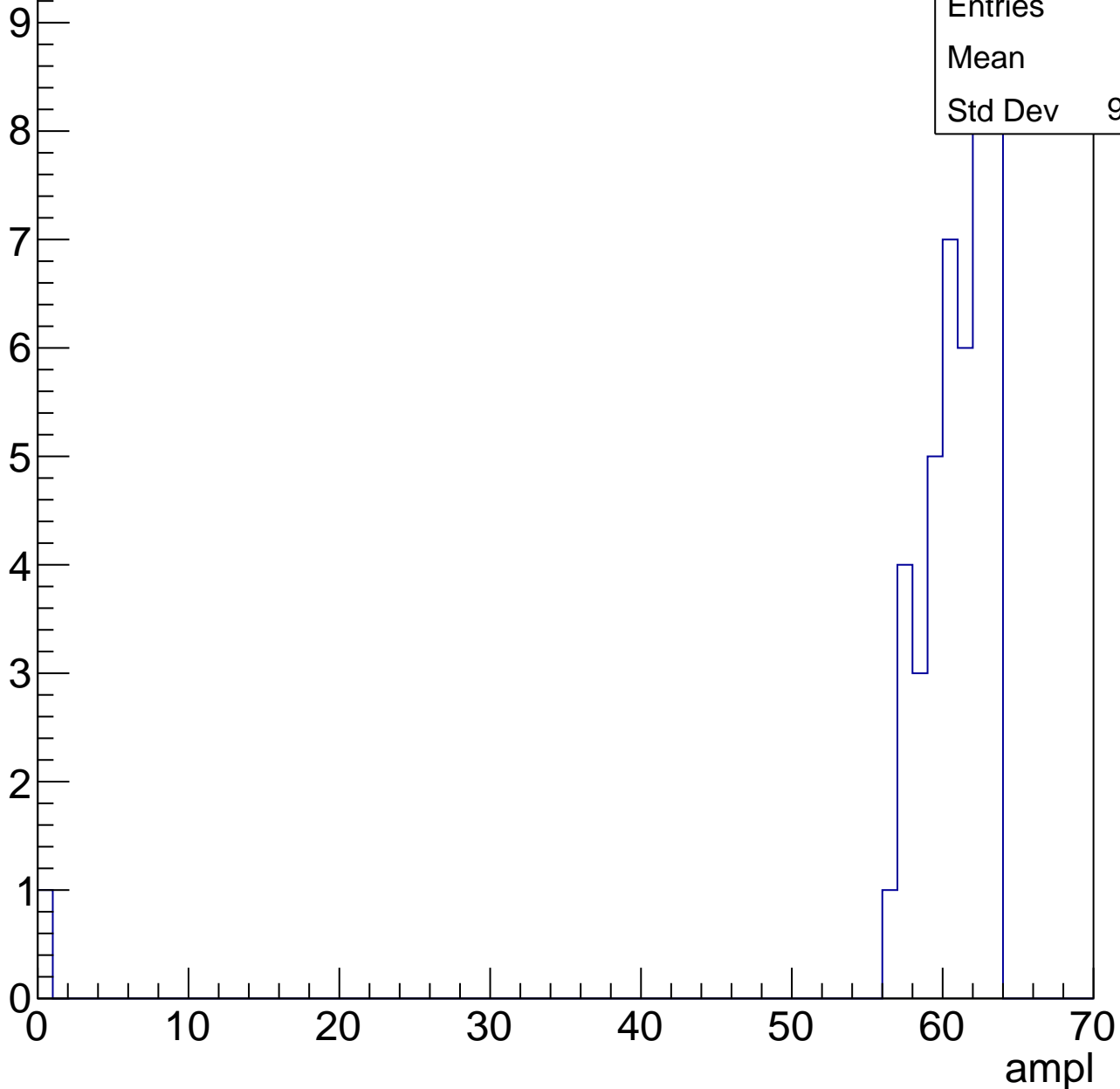


# B0L001S, U10-ch109, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	45
Mean	59.2
Std Dev	9.145



# B0L001S, U10-ch109, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch109, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U10-ch110, adc0

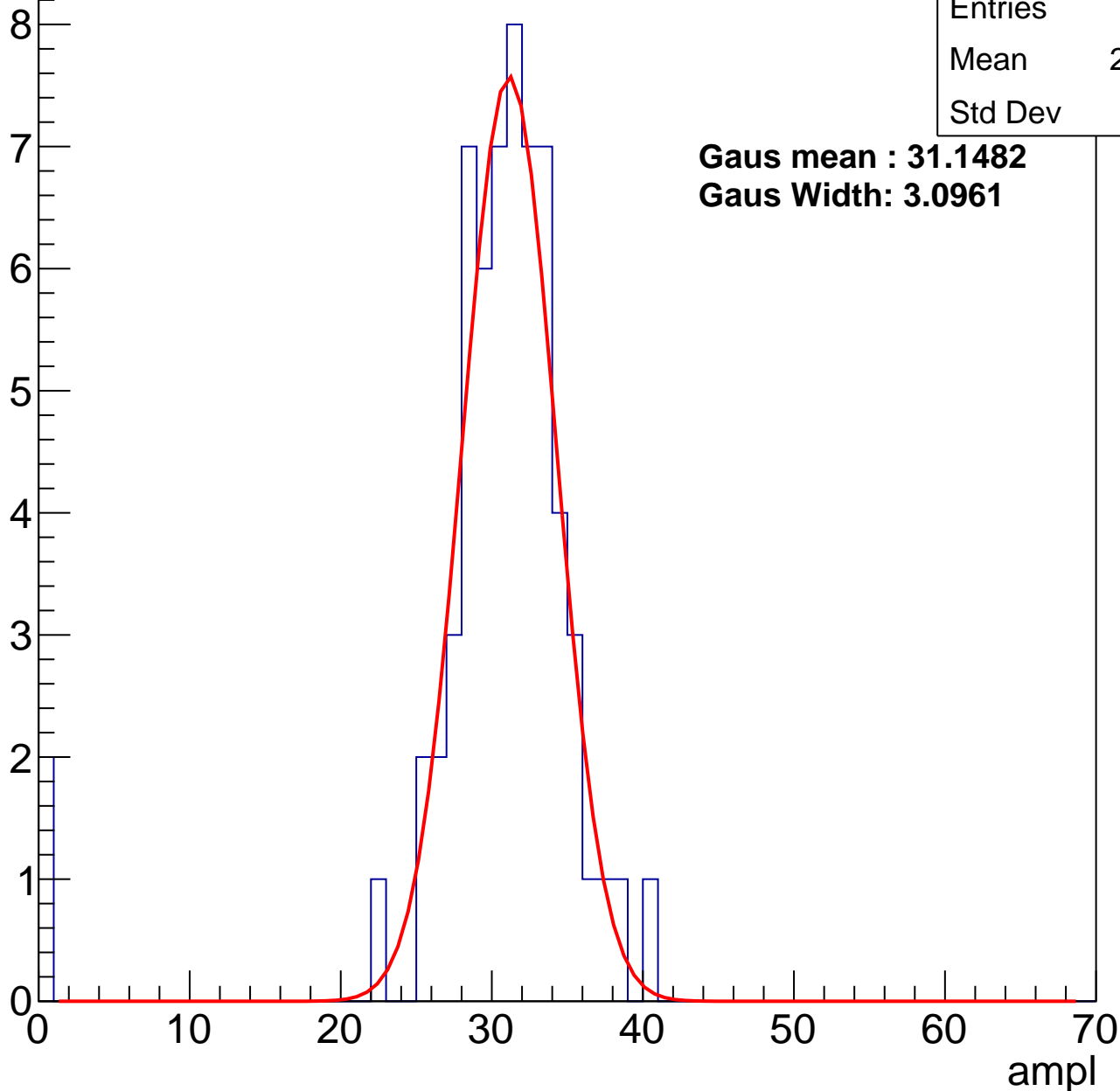
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	29.84
Std Dev	6.29

**Gaus mean : 31.1482**

**Gaus Width: 3.0961**



# B0L001S, U10-ch110, adc1

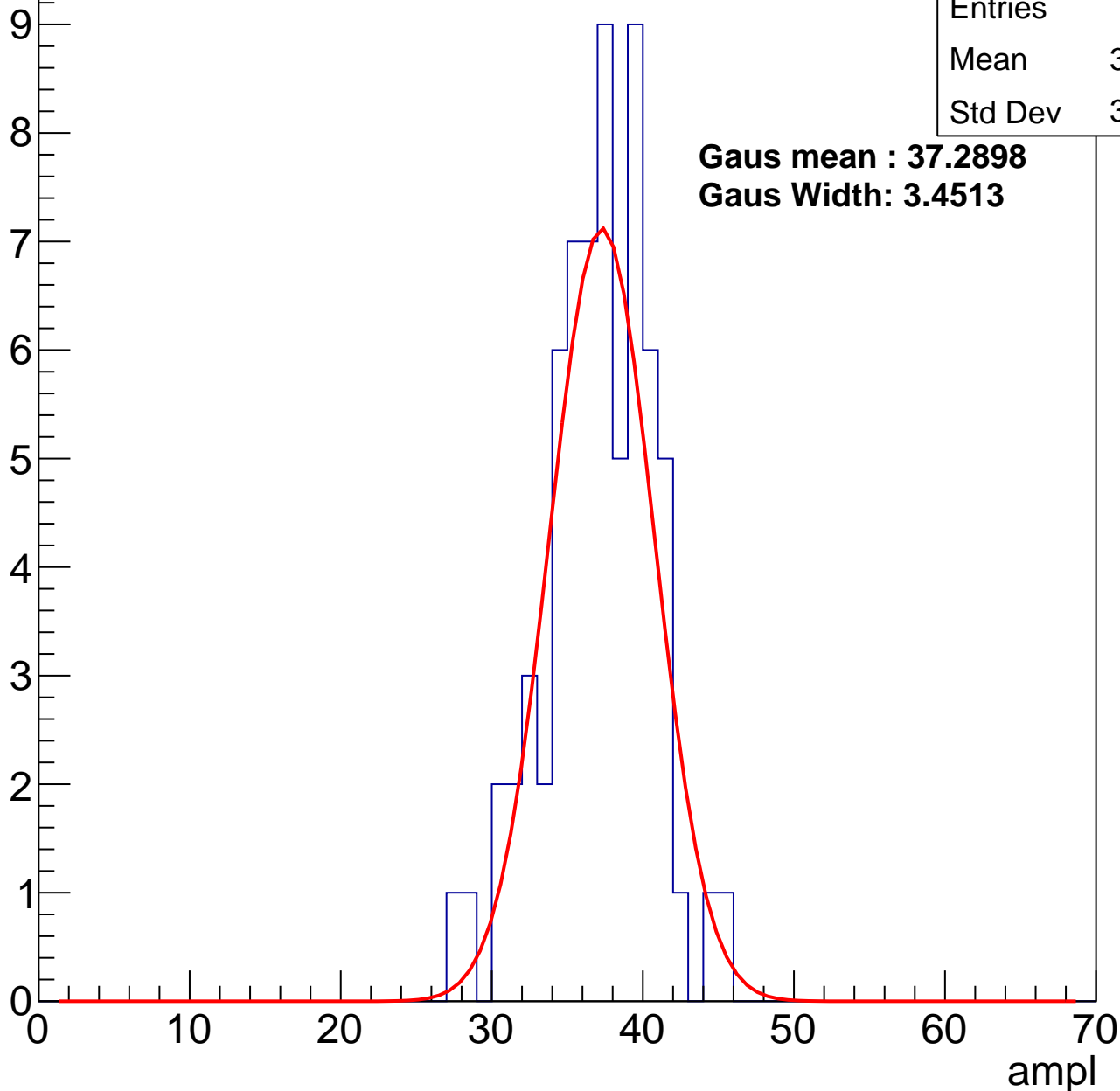
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	36.62
Std Dev	3.536

**Gaus mean : 37.2898**

**Gaus Width: 3.4513**



# B0L001S, U10-ch110, adc2

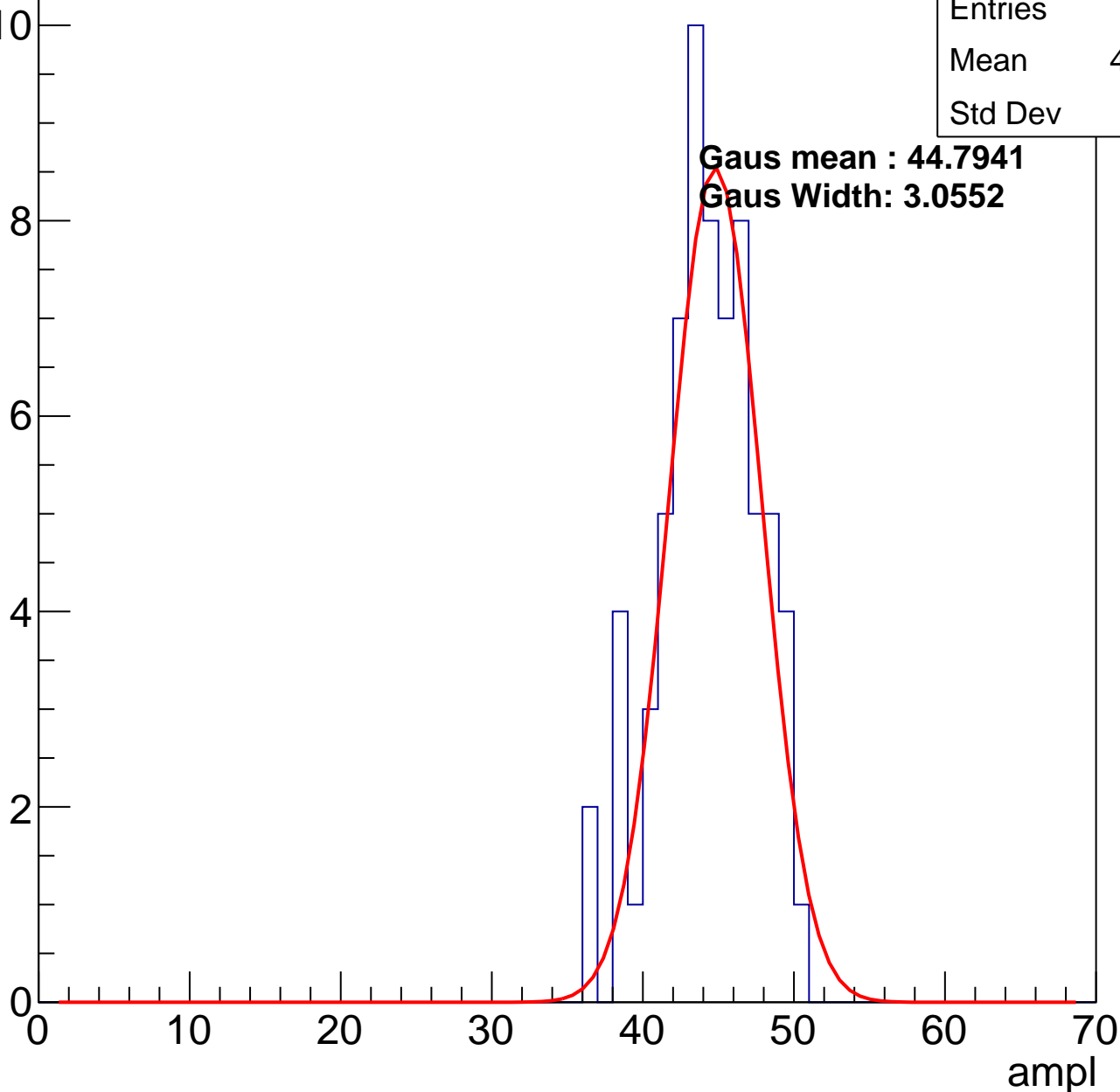
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	43.83
Std Dev	3.22

**Gaus mean : 44.7941**

**Gaus Width: 3.0552**

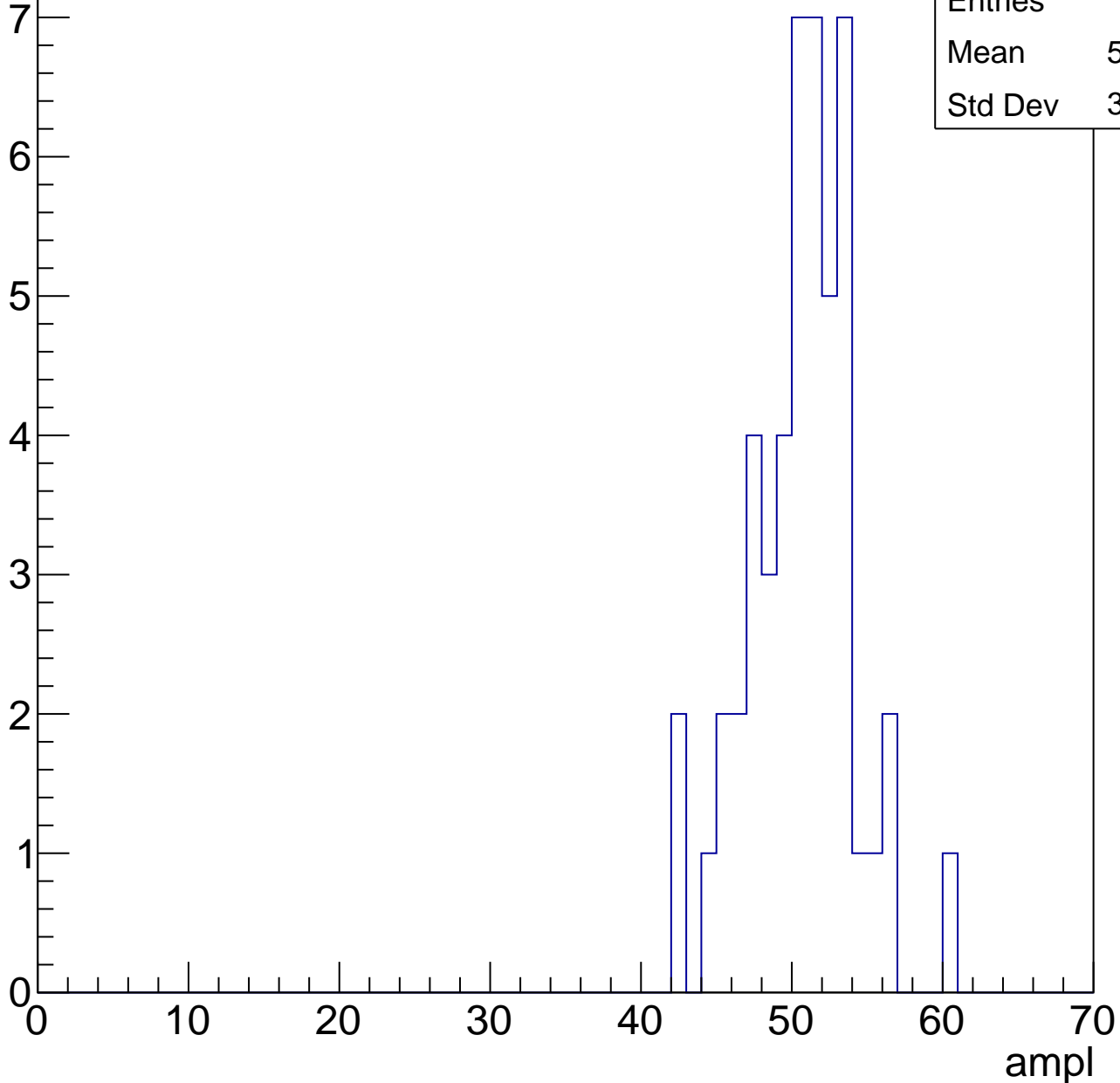


# B0L001S, U10-ch110, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	49
Mean	50.14
Std Dev	3.499

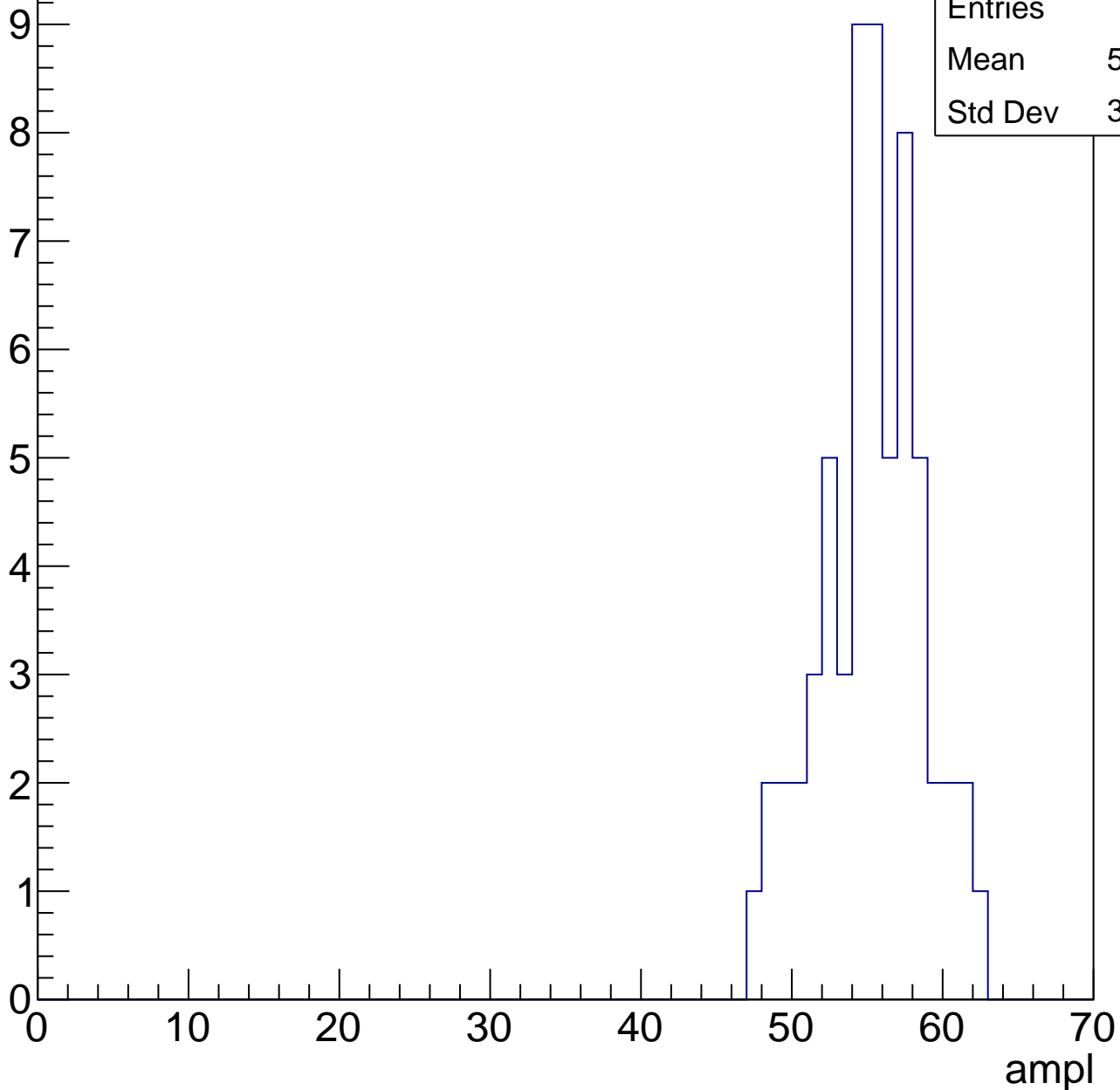


# B0L001S, U10-ch110, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

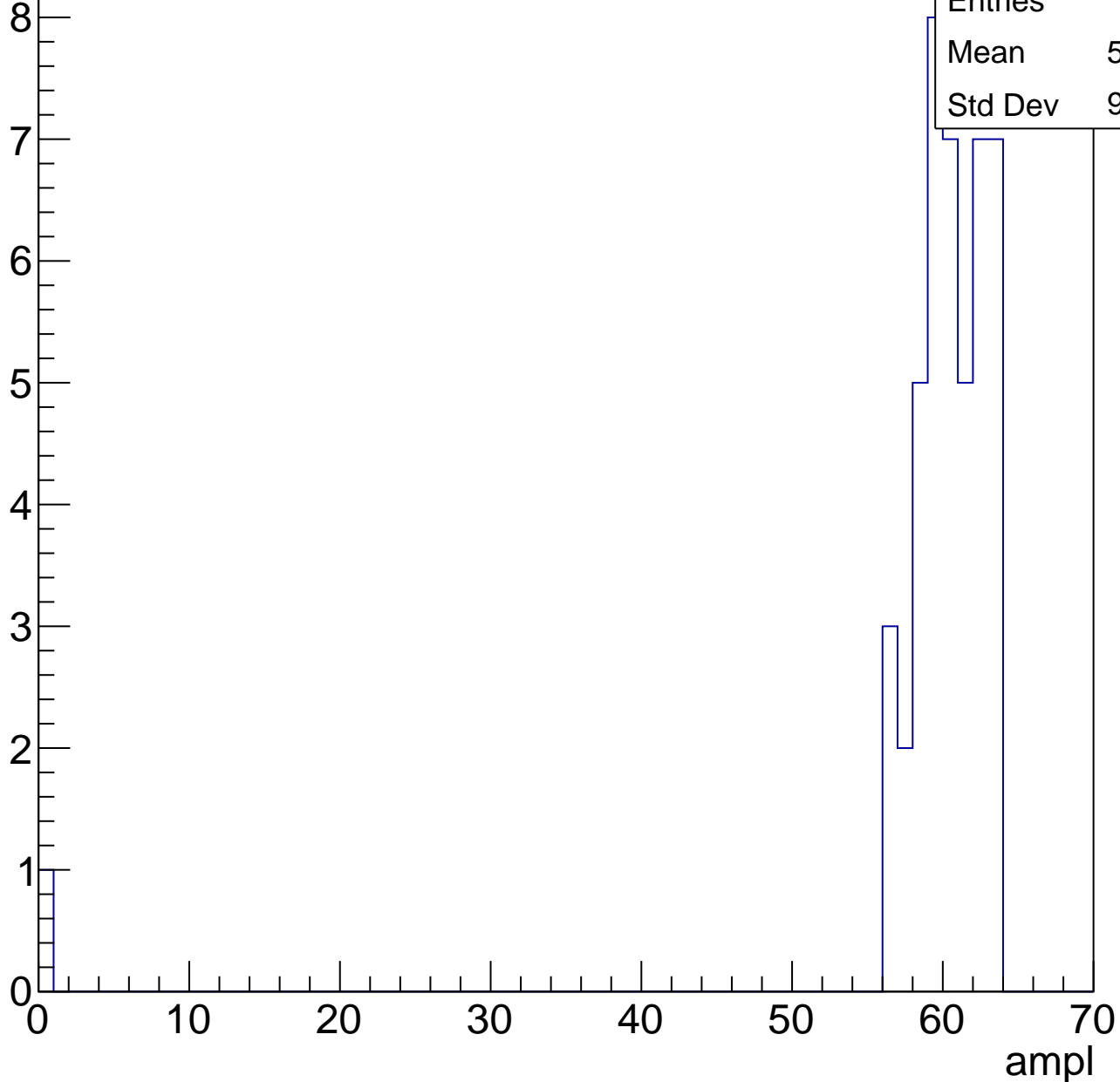
Entries	61
Mean	54.79
Std Dev	3.339



# B0L001S, U10-ch110, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

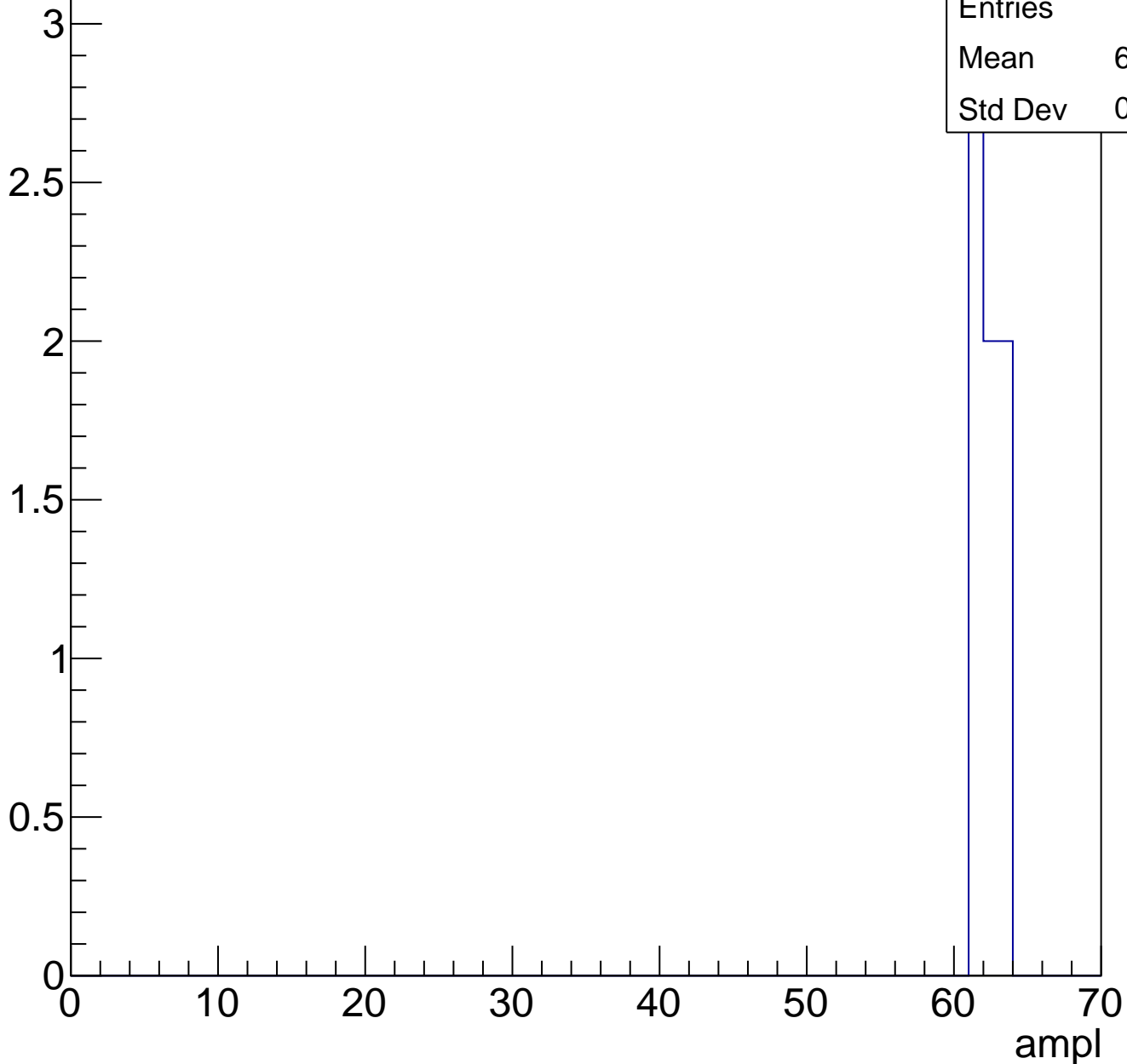
Entry



# B0L001S, U10-ch110, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

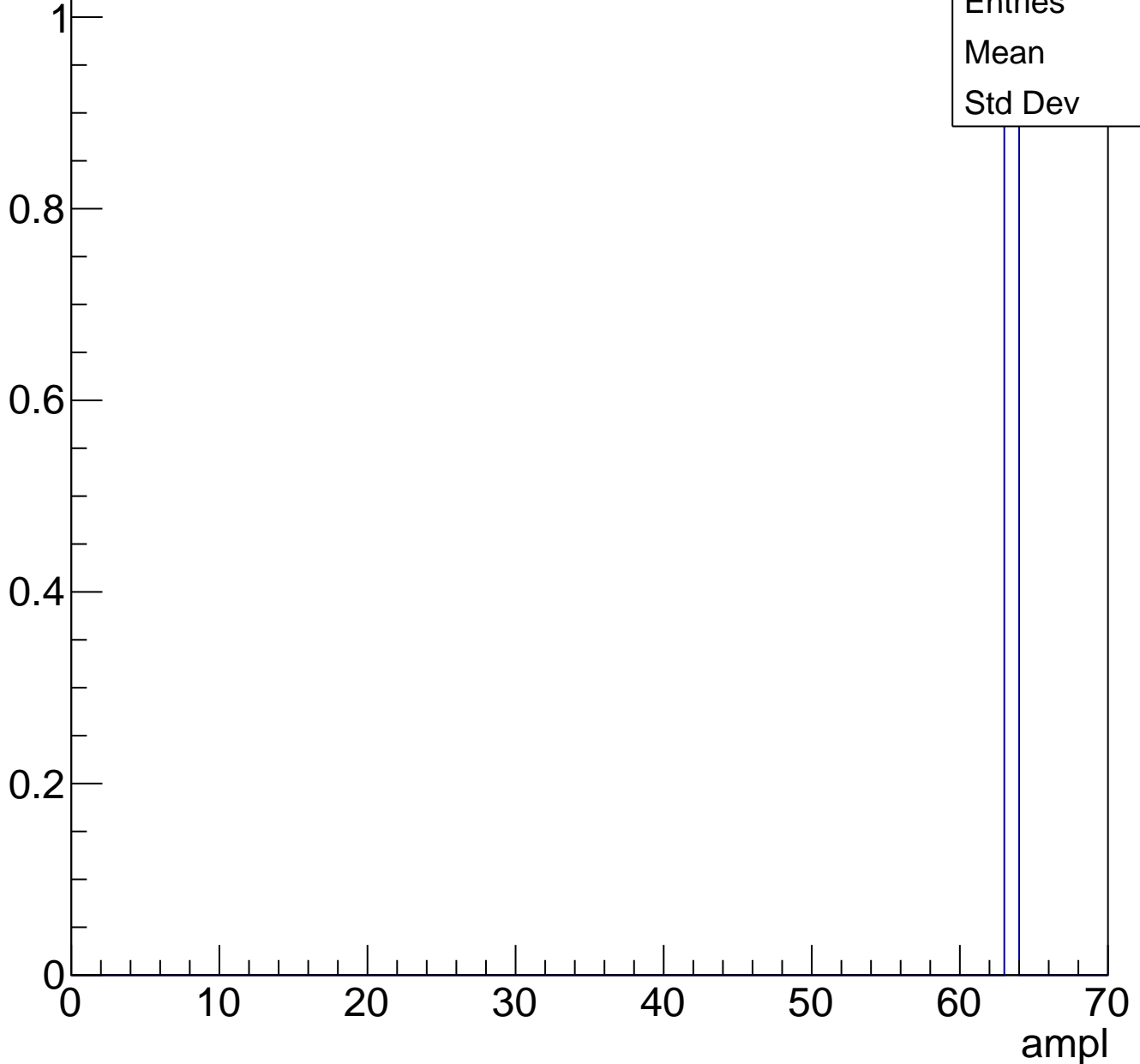




# B0L001S, U10-ch110, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U10-ch111, adc0

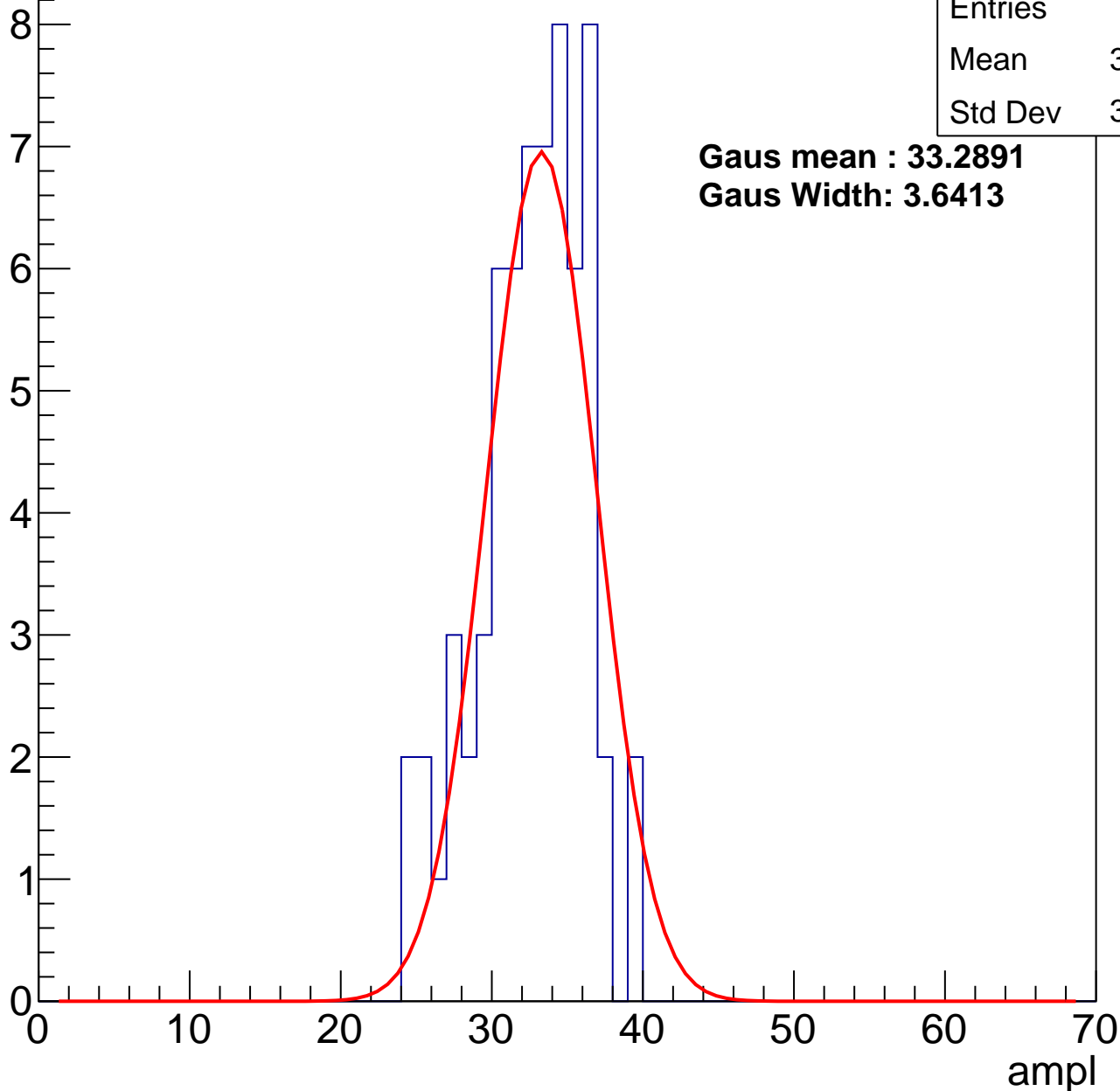
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	32.17
Std Dev	3.493

**Gaus mean : 33.2891**

**Gaus Width: 3.6413**



# B0L001S, U10-ch111, adc1

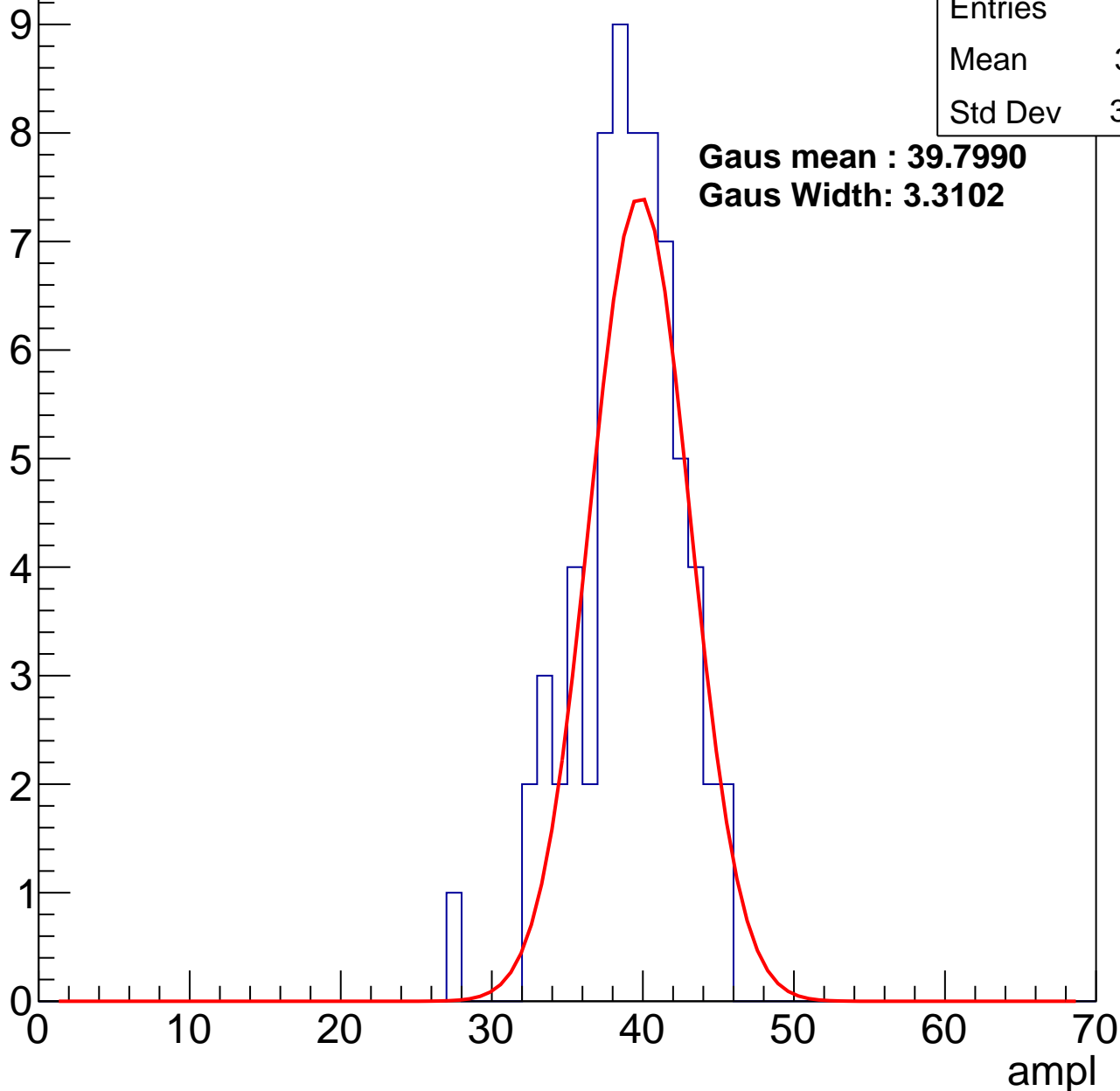
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	38.61
Std Dev	3.412

**Gaus mean : 39.7990**

**Gaus Width: 3.3102**



# B0L001S, U10-ch111, adc2

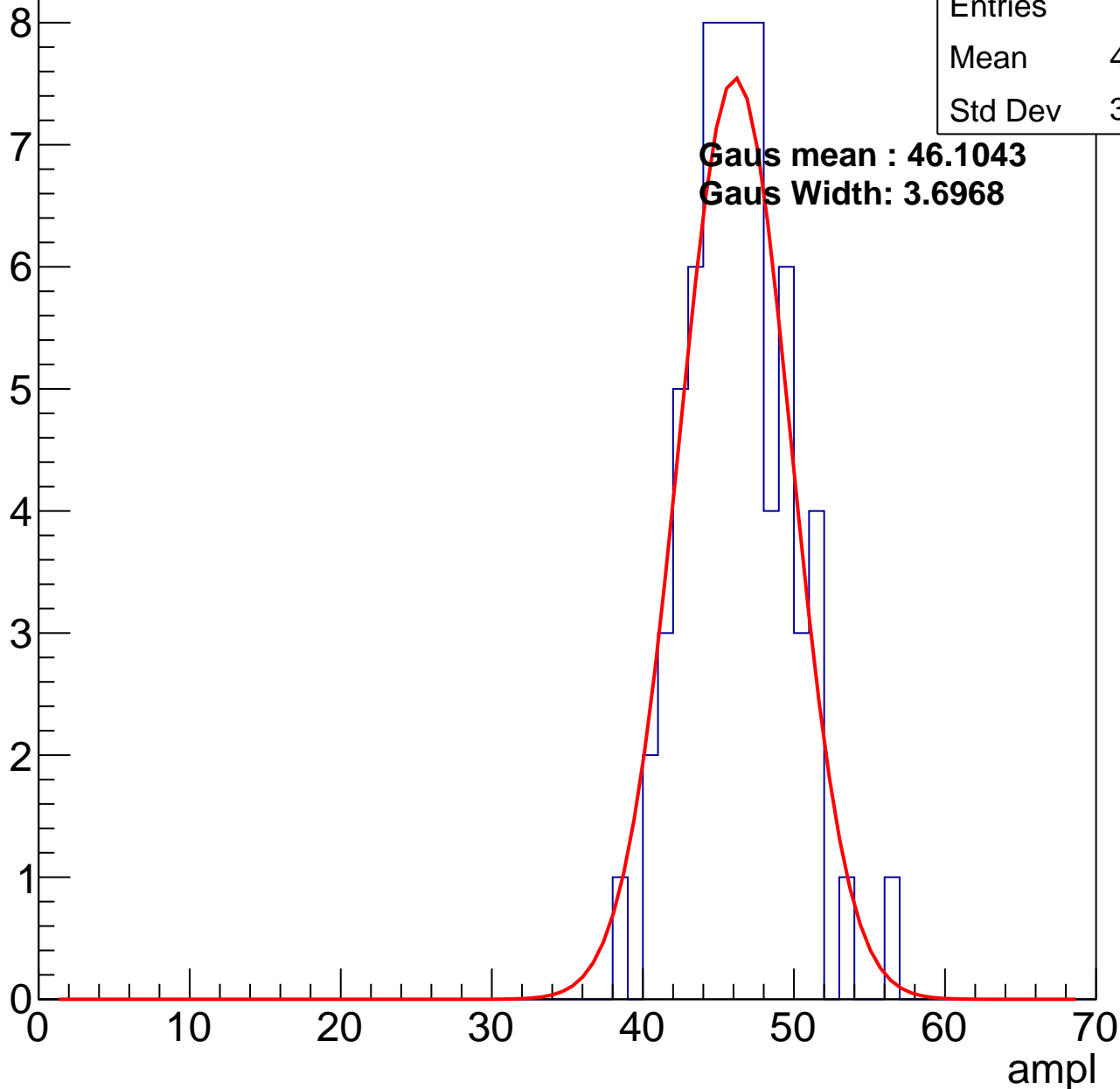
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	45.79
Std Dev	3.337

**Gaus mean : 46.1043**

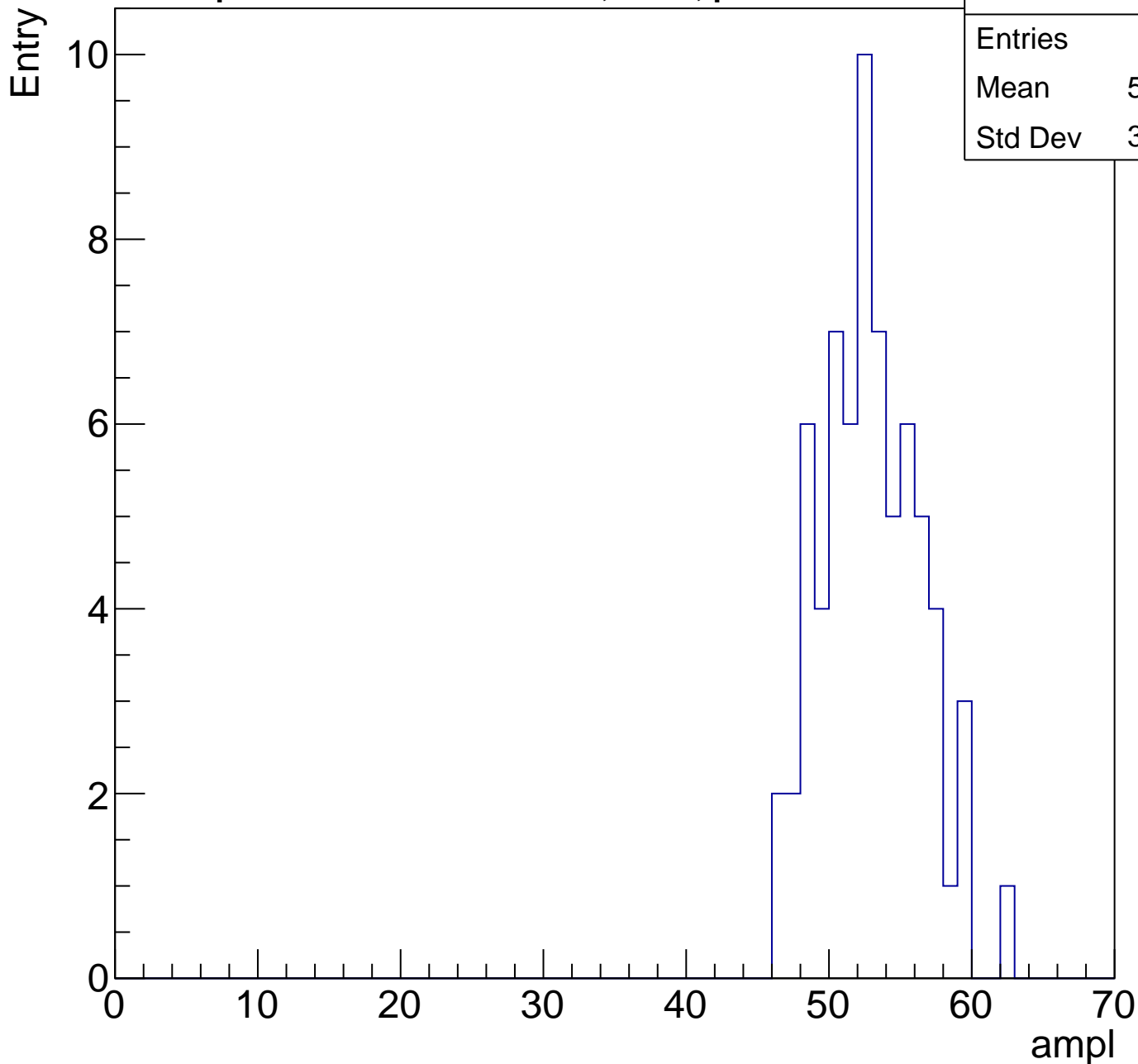
**Gaus Width: 3.6968**



# B0L001S, U10-ch111, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	69
Mean	52.49
Std Dev	3.437

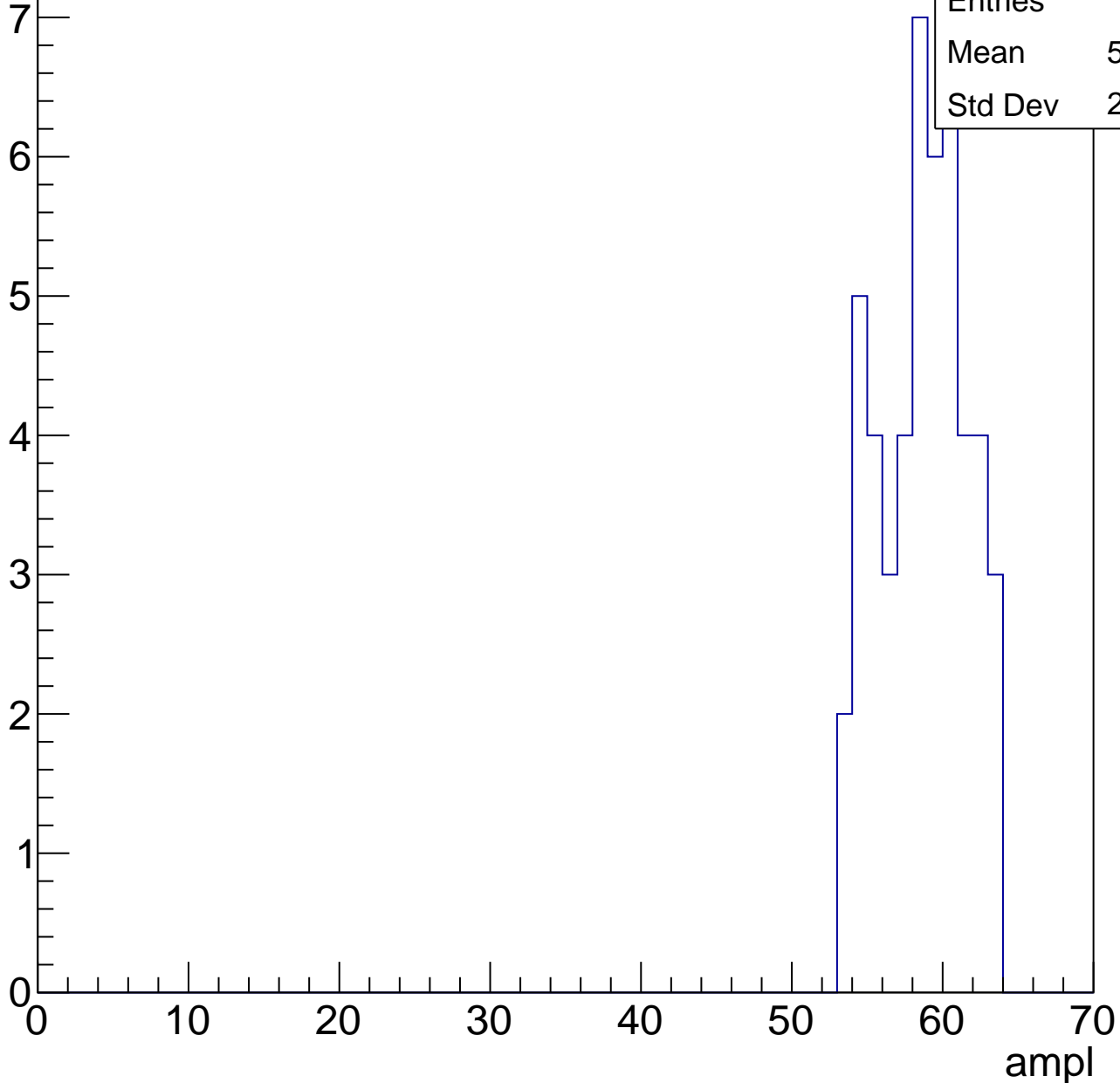


# B0L001S, U10-ch111, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	49
Mean	58.22
Std Dev	2.816

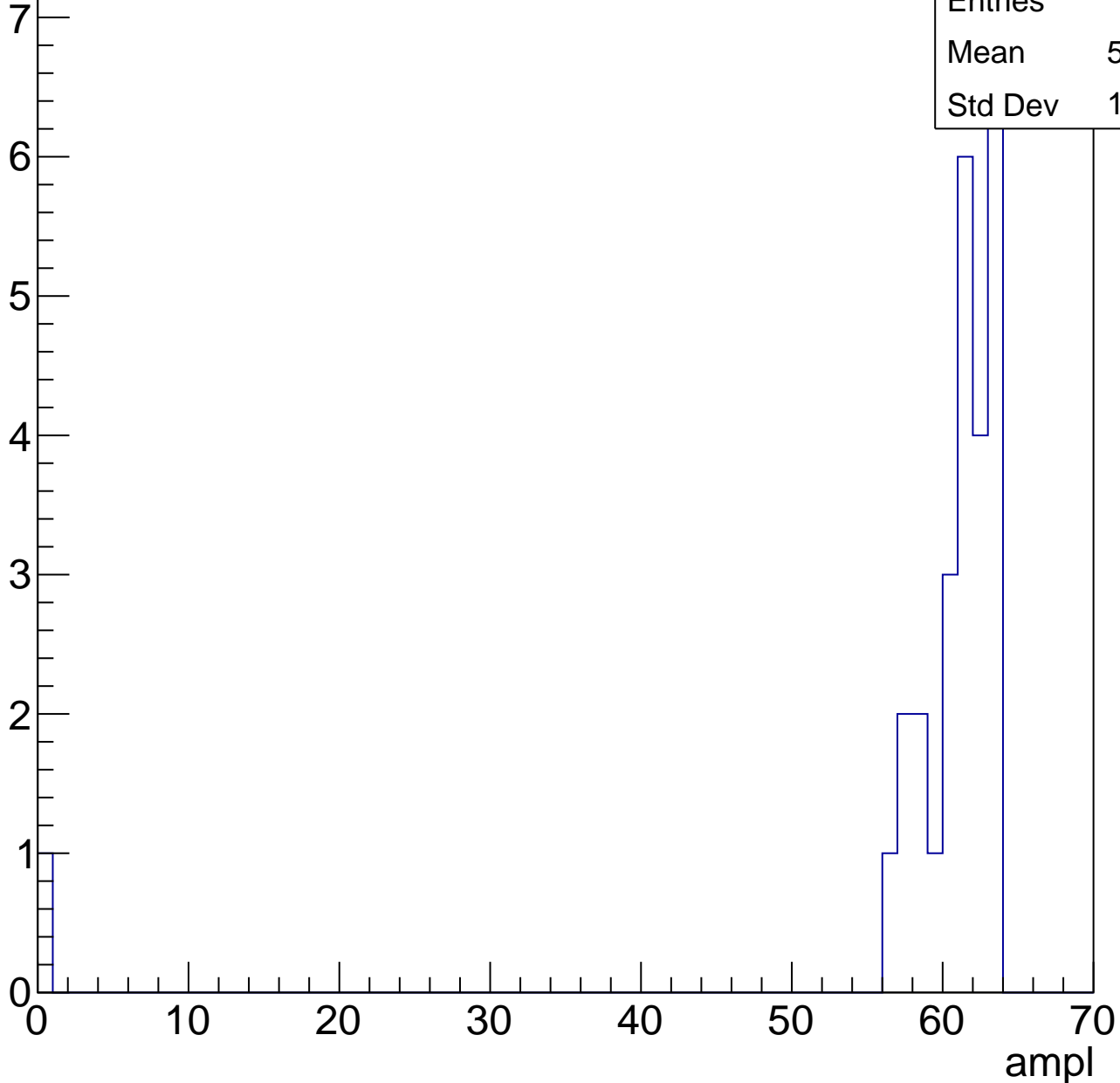


# B0L001S, U10-ch111, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	27
Mean	58.52
Std Dev	11.66



# B0L001S, U10-ch111, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch111, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U10-ch112, adc0

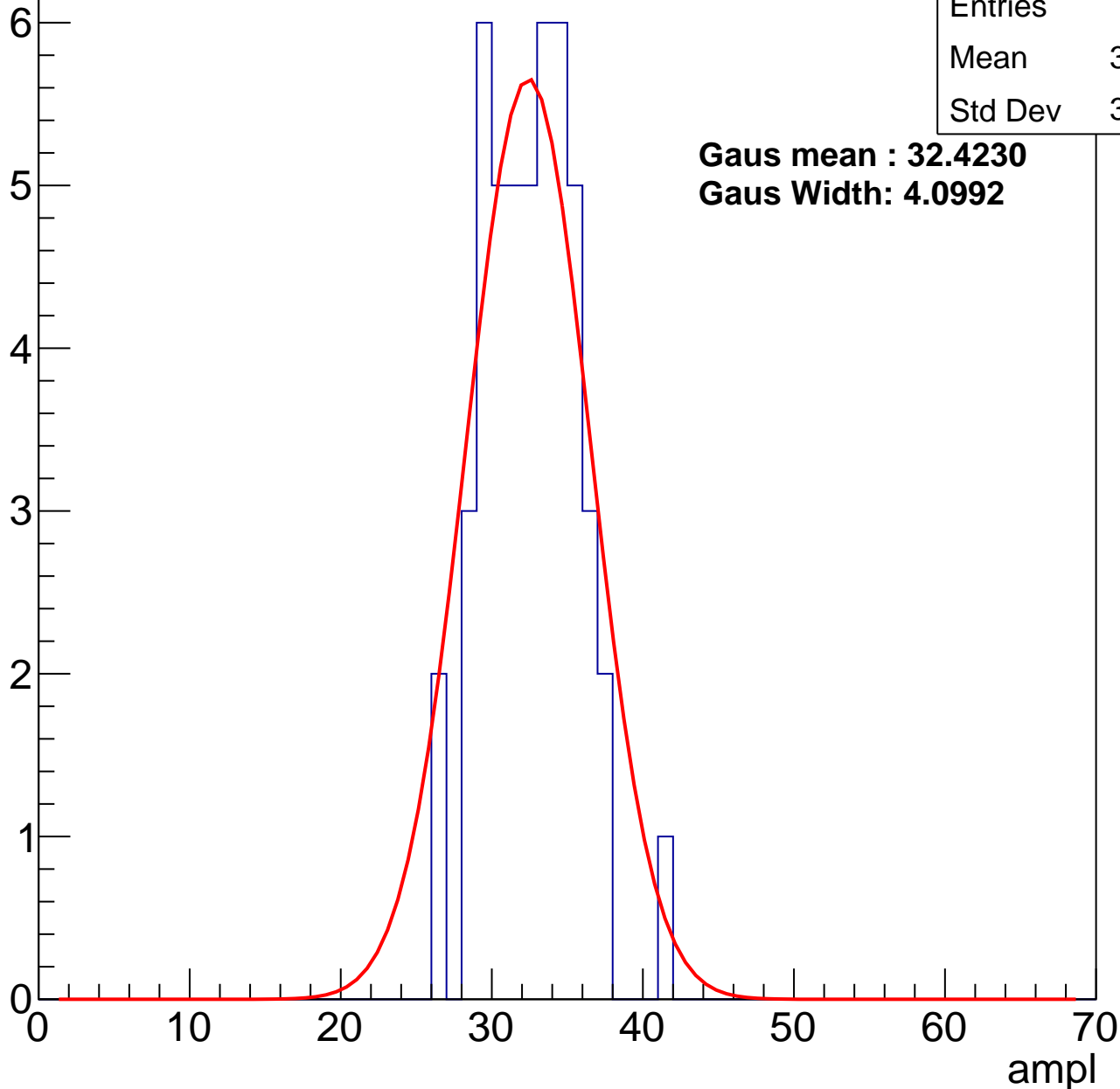
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	49
Mean	32.14
Std Dev	3.037

**Gaus mean : 32.4230**

**Gaus Width: 4.0992**



# B0L001S, U10-ch112, adc1

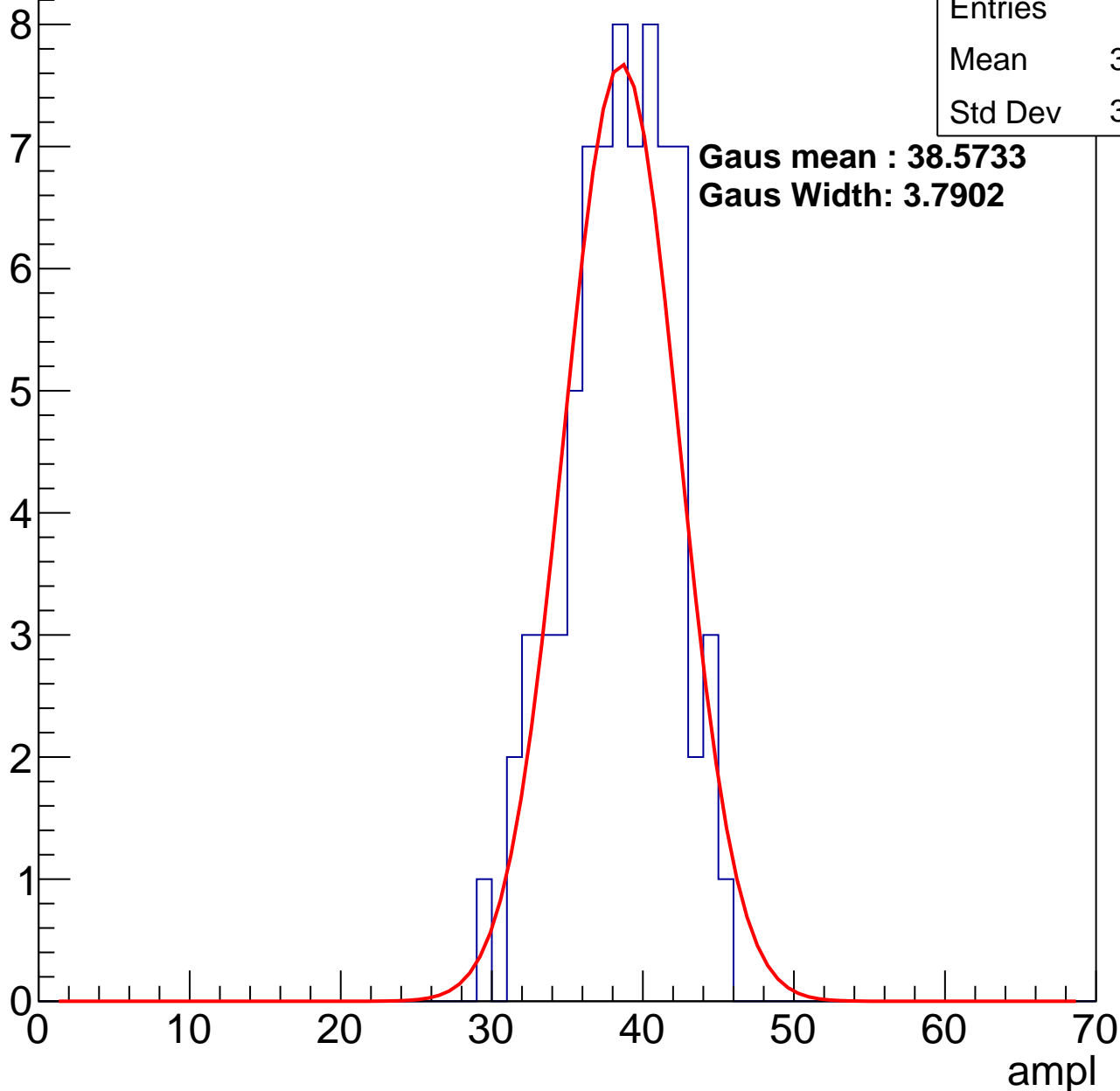
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	38.04
Std Dev	3.508

**Gaus mean : 38.5733**

**Gaus Width: 3.7902**



# B0L001S, U10-ch112, adc2

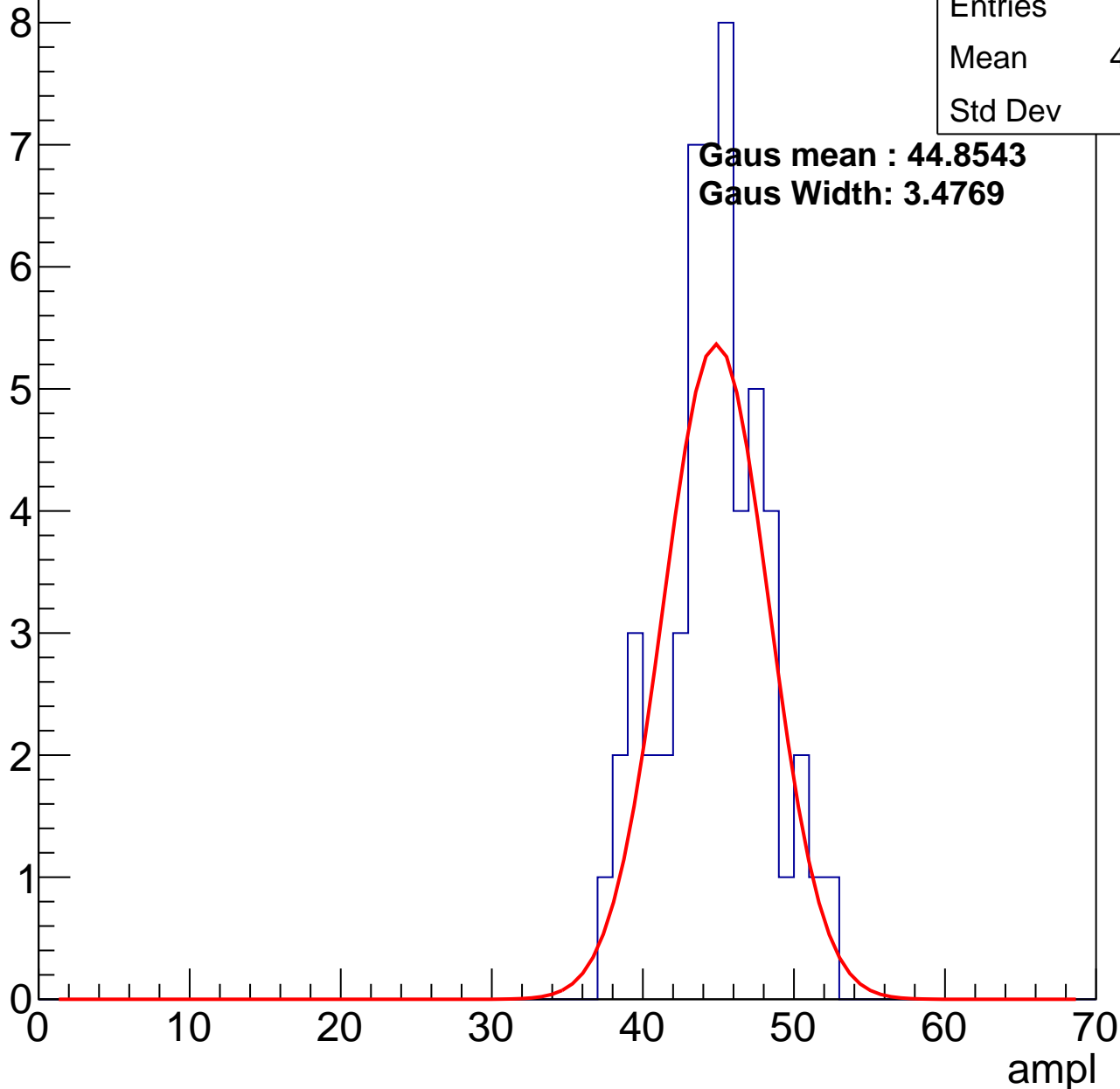
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	44.34
Std Dev	3.37

**Gaus mean : 44.8543**

**Gaus Width: 3.4769**

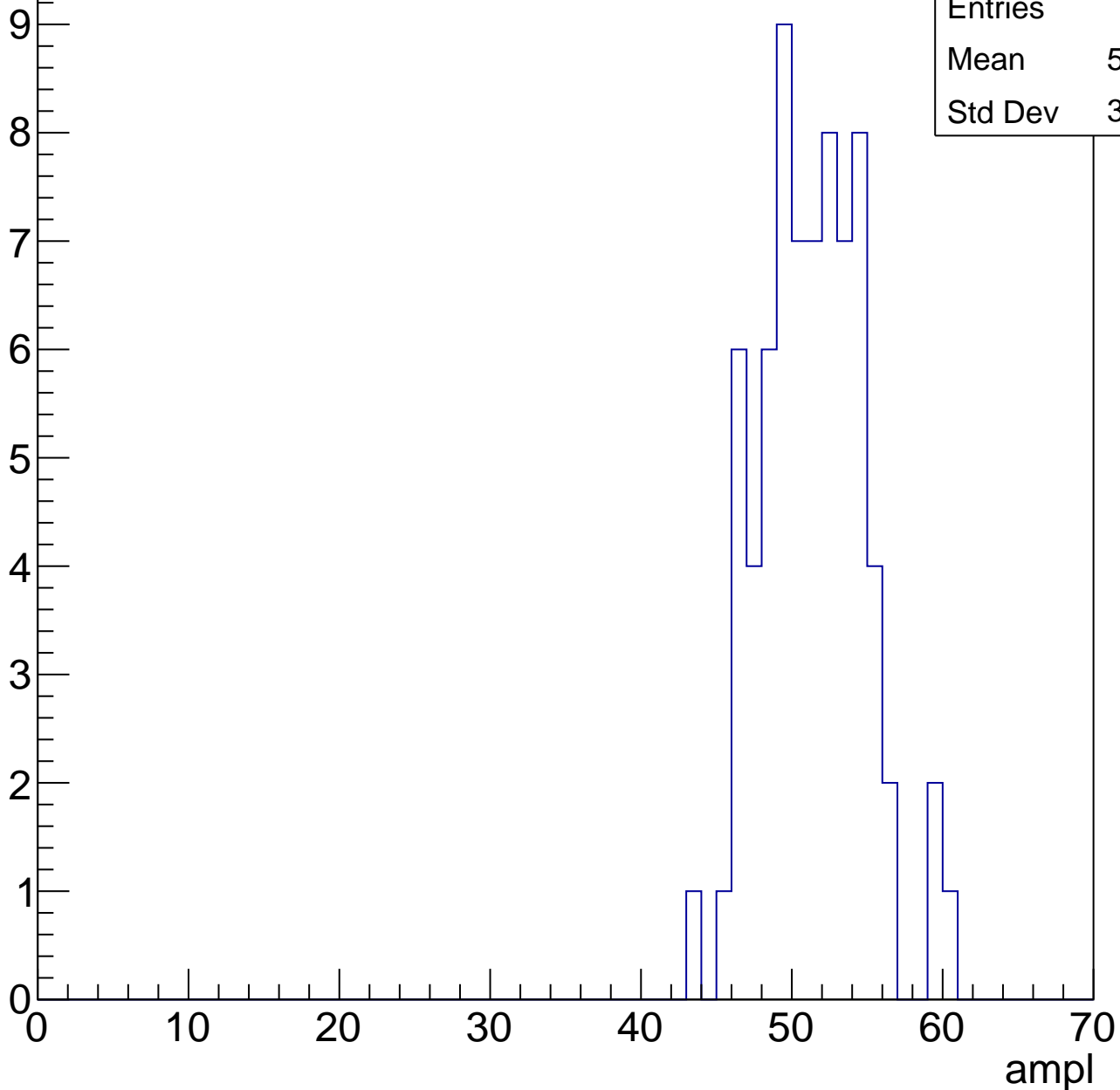


# B0L001S, U10-ch112, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

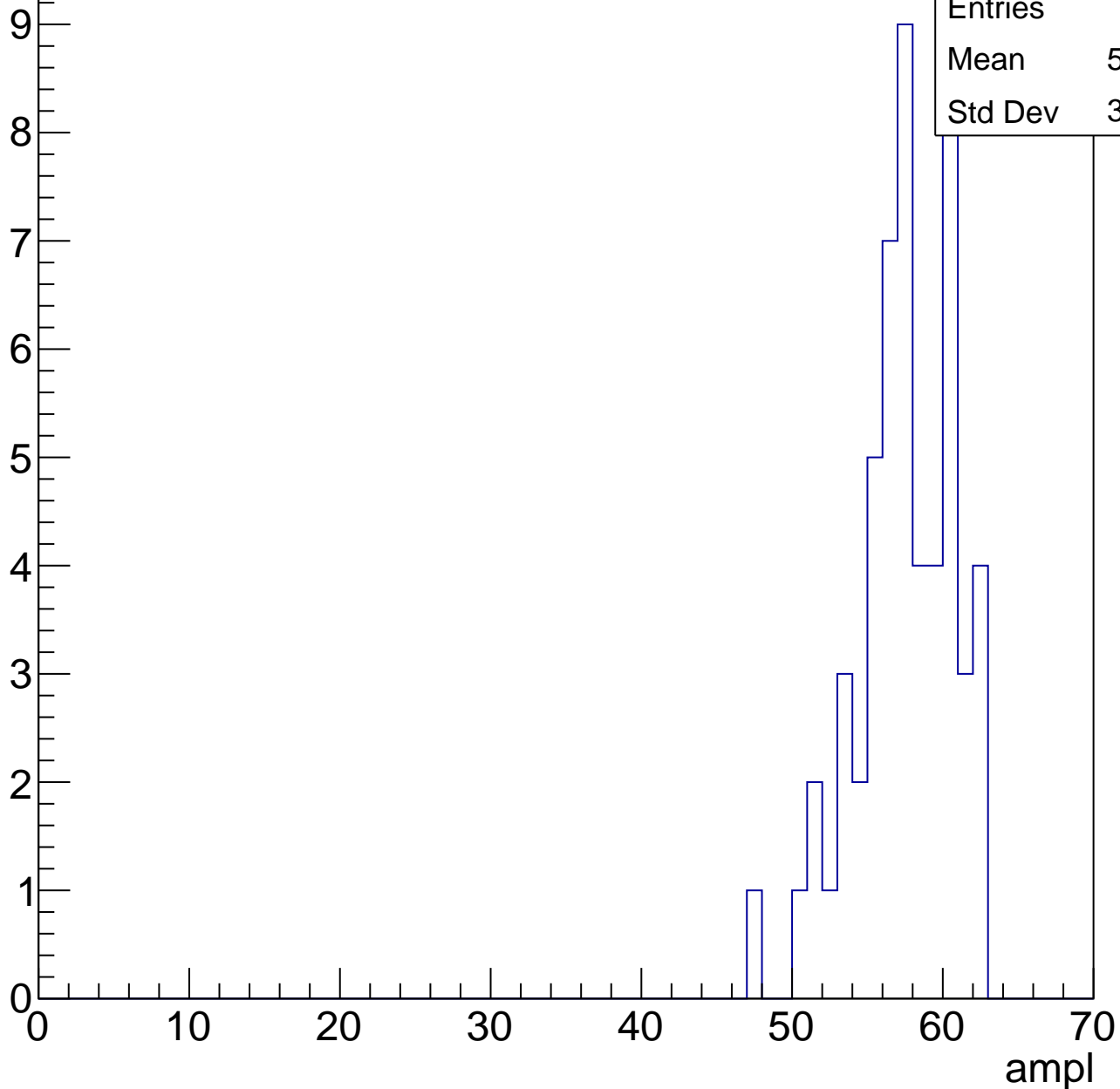
Entries	73
Mean	50.92
Std Dev	3.395



# B0L001S, U10-ch112, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	55
Mean	57.04
Std Dev	3.269

# B0L001S, U10-ch112, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	37
Mean	58.95
Std Dev	10.08

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

ampl

70

# B0L001S, U10-ch112, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U10-ch112, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U10-ch113, adc0

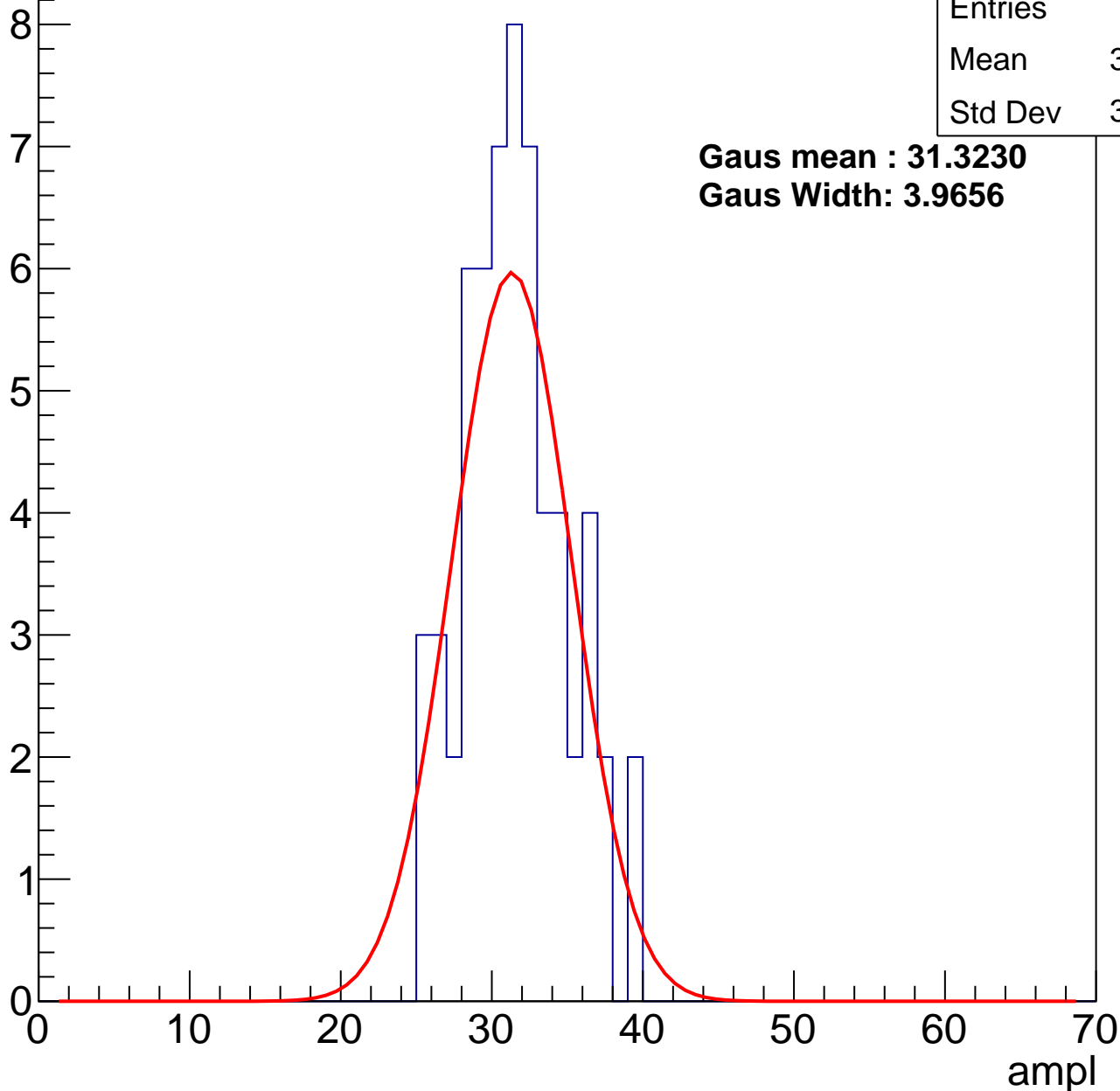
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	31.08
Std Dev	3.393

**Gaus mean : 31.3230**

**Gaus Width: 3.9656**



# B0L001S, U10-ch113, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	66
Mean	37.12
Std Dev	3.557

**Gaus mean : 37.0623**

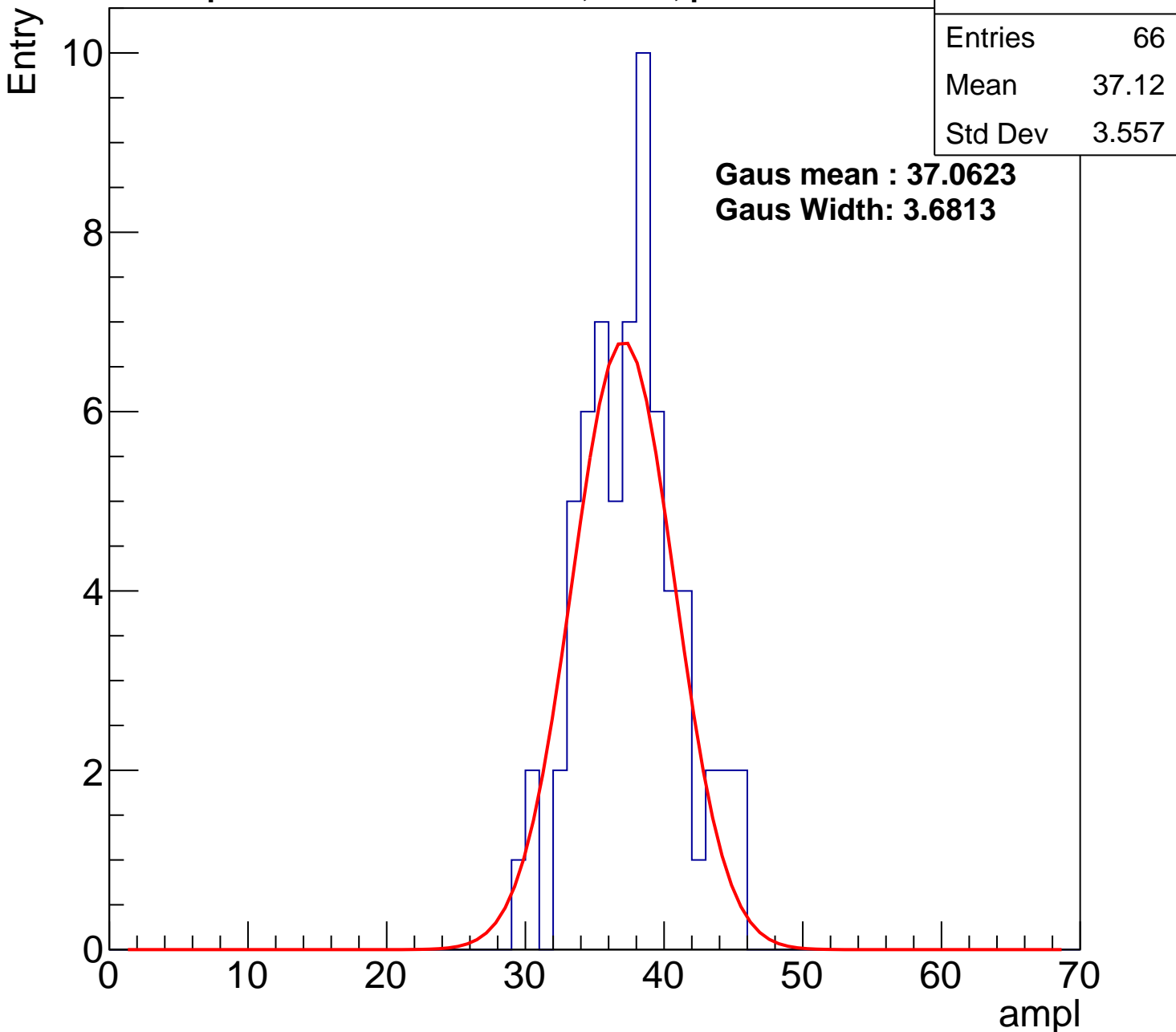
**Gaus Width: 3.6813**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B0L001S, U10-ch113, adc2

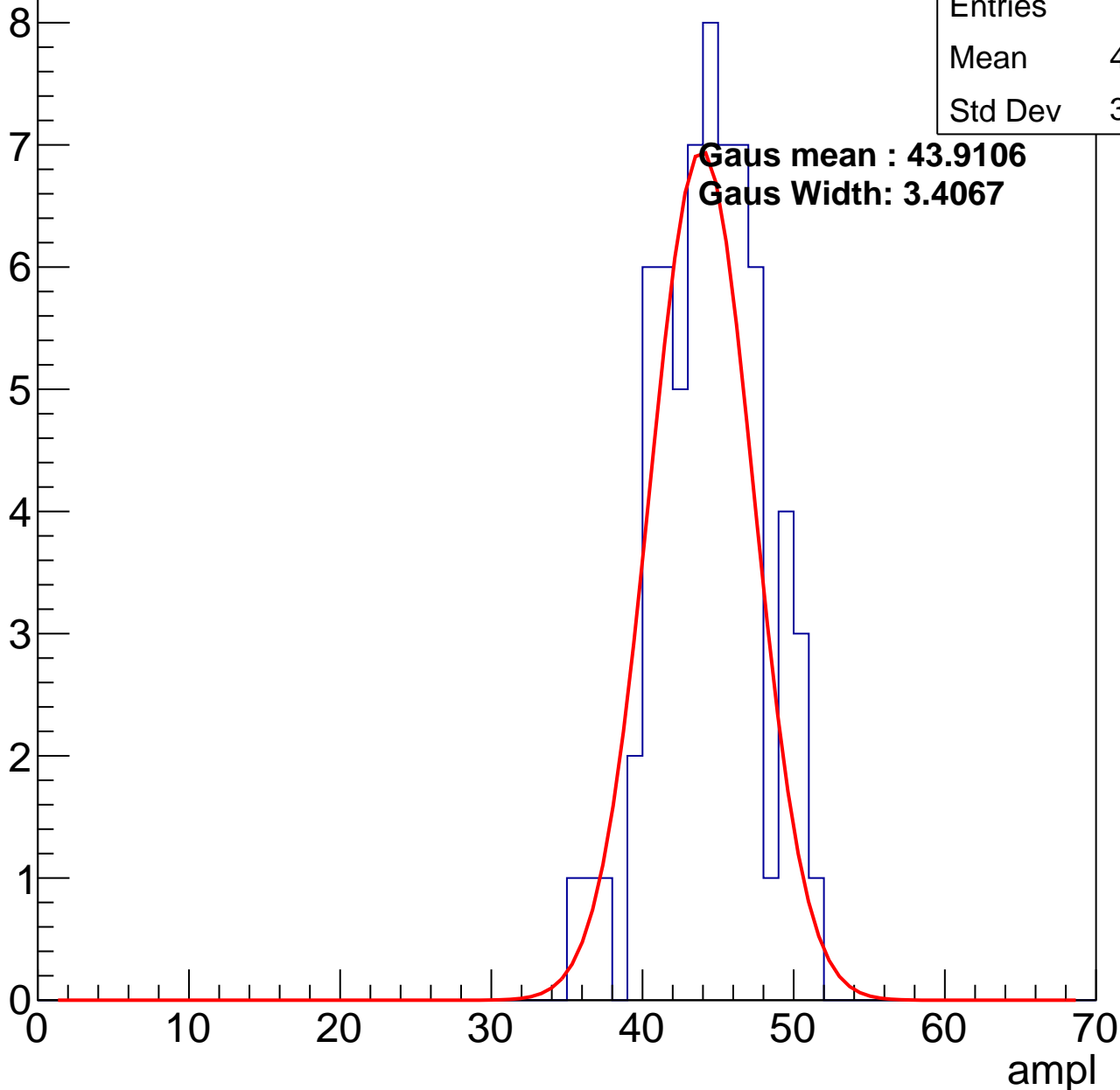
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	43.92
Std Dev	3.444

**Gaus mean : 43.9106**

**Gaus Width: 3.4067**

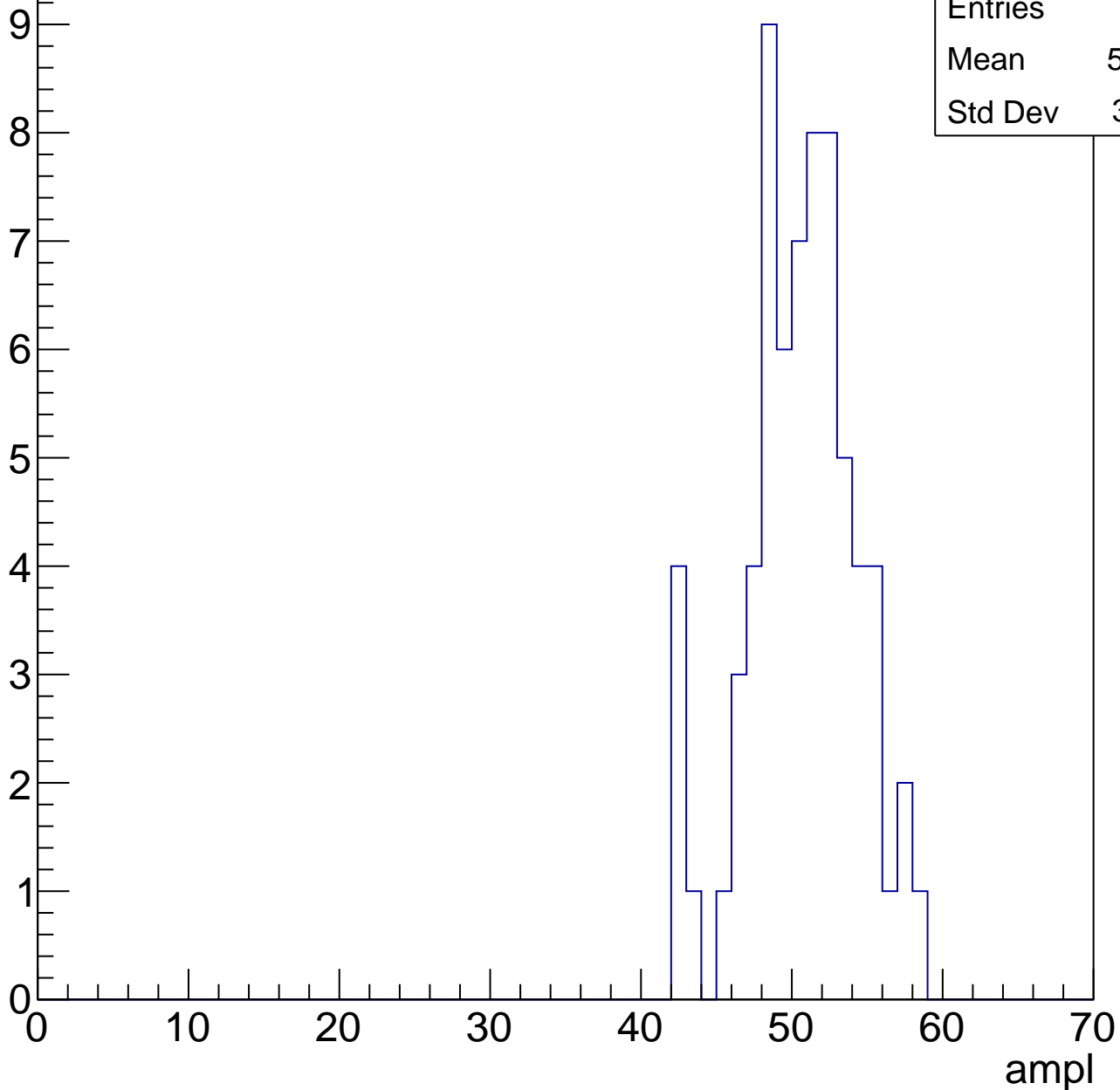


# B0L001S, U10-ch113, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	50.16
Std Dev	3.641

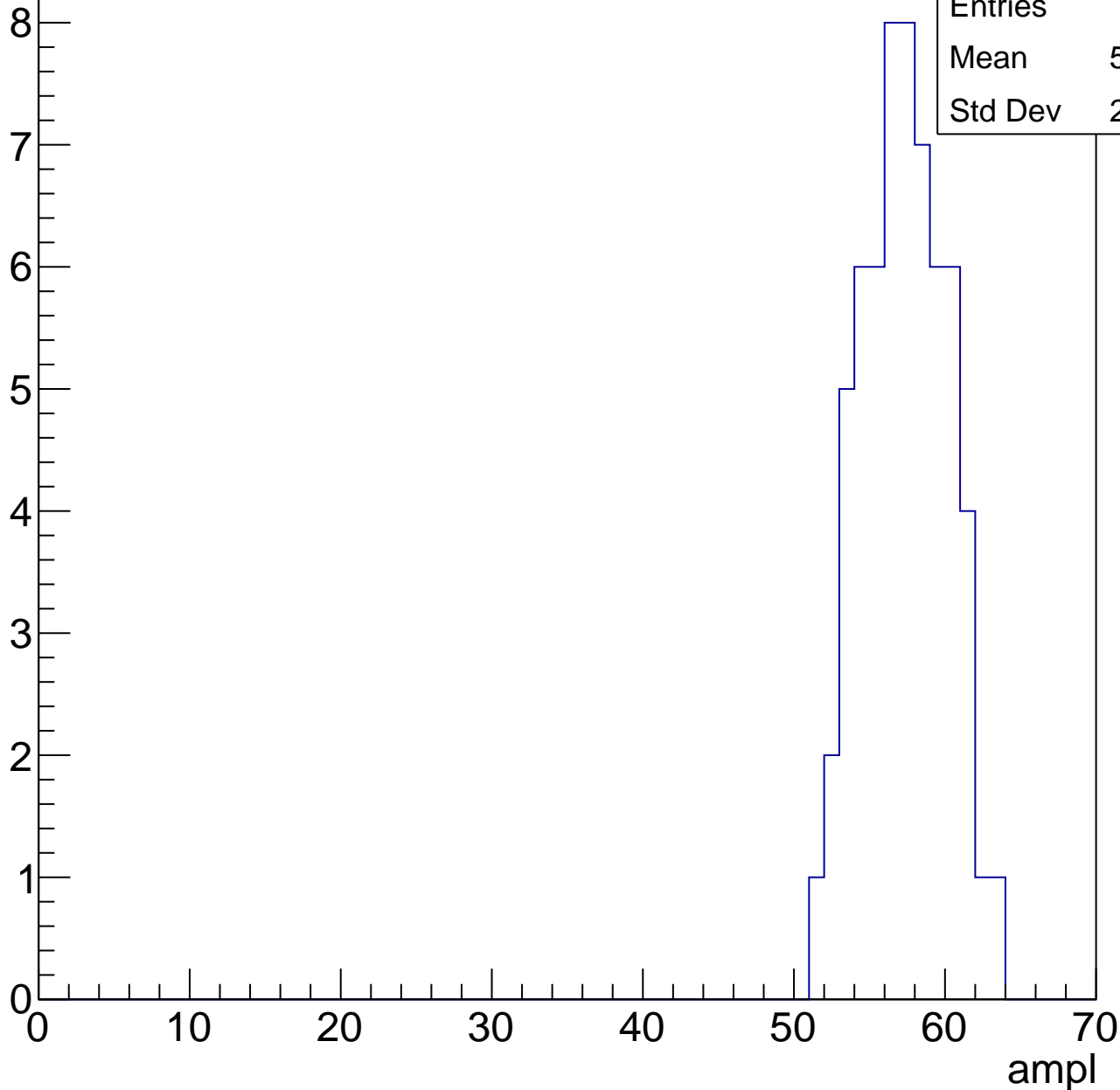


# B0L001S, U10-ch113, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	56.84
Std Dev	2.747

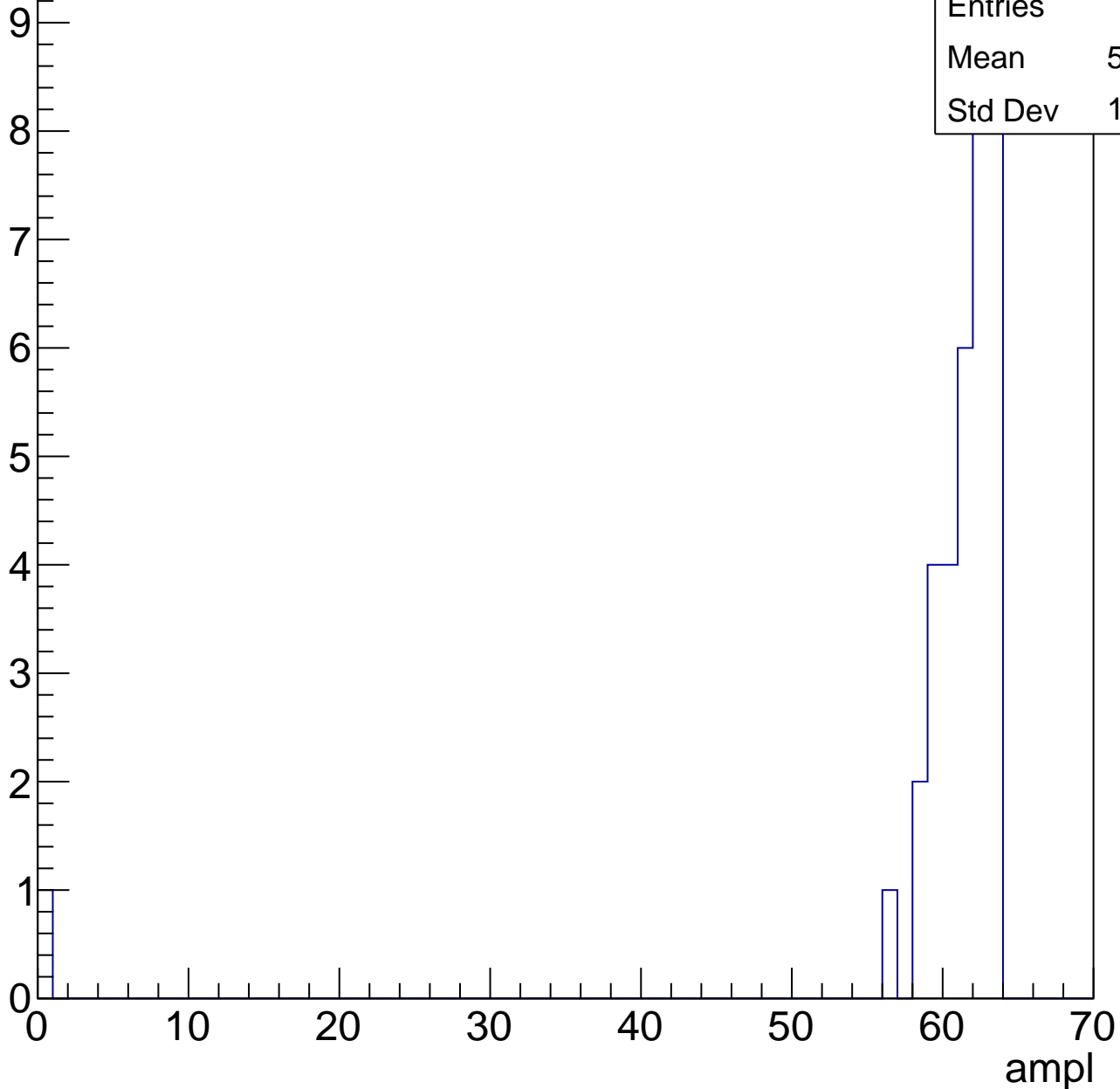


# B0L001S, U10-ch113, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	36
Mean	59.42
Std Dev	10.19



# B0L001S, U10-ch113, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U10-ch113, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	12.5
Std Dev	12.5

# B0L001S, U10-ch114, adc0

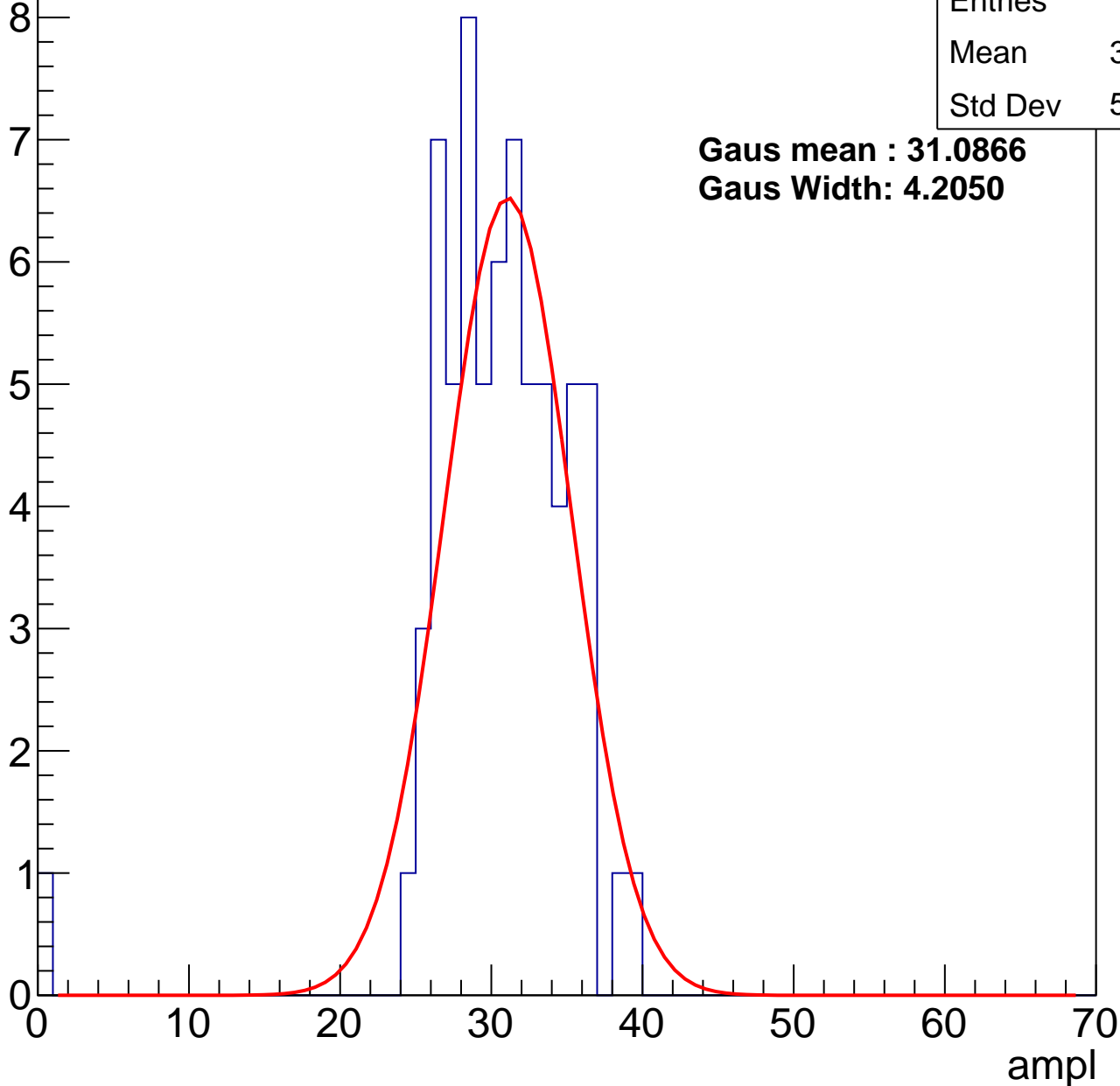
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	30.07
Std Dev	5.094

**Gaus mean : 31.0866**

**Gaus Width: 4.2050**



# B0L001S, U10-ch114, adc1

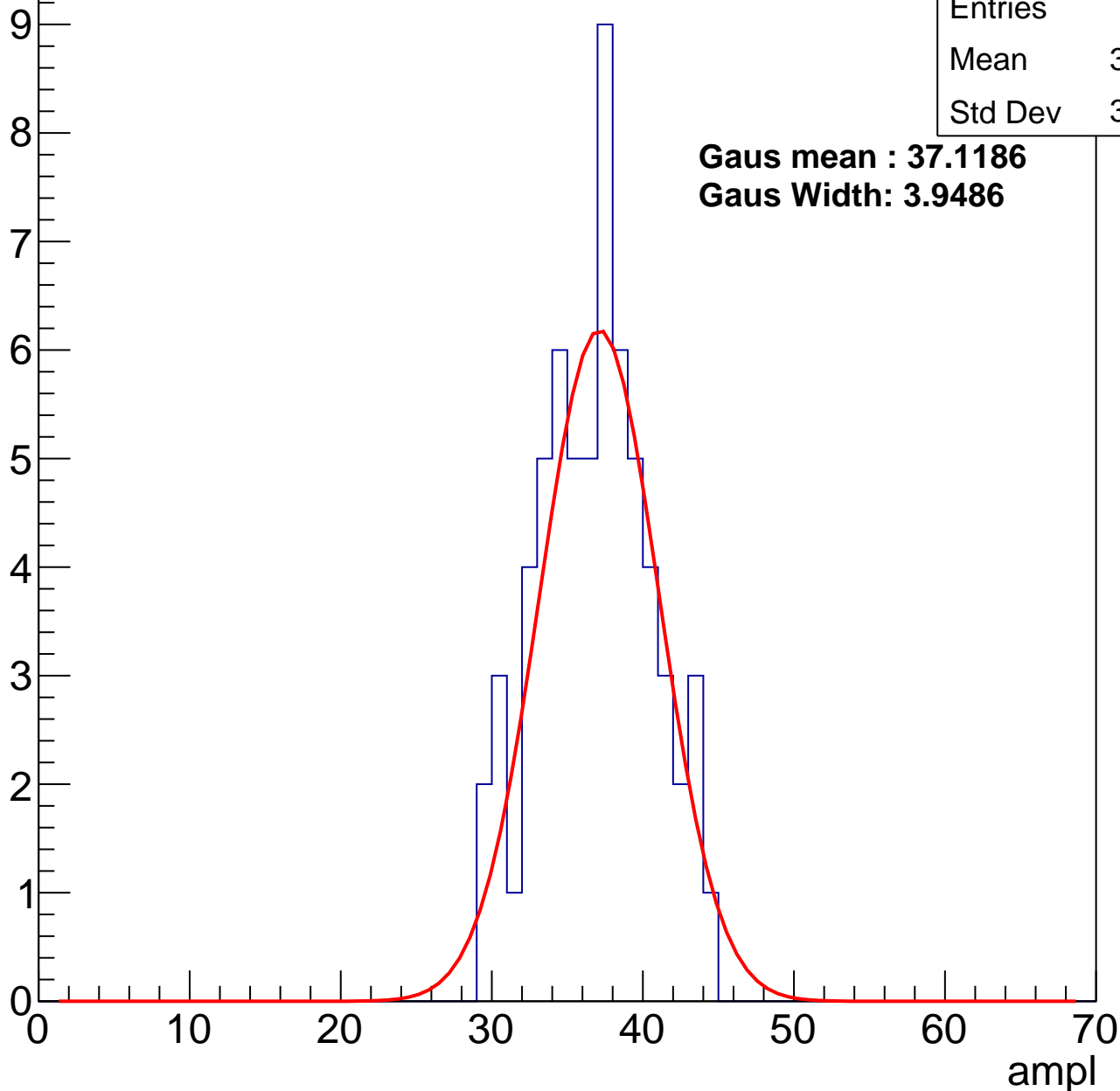
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	36.36
Std Dev	3.667

**Gaus mean : 37.1186**

**Gaus Width: 3.9486**



# B0L001S, U10-ch114, adc2

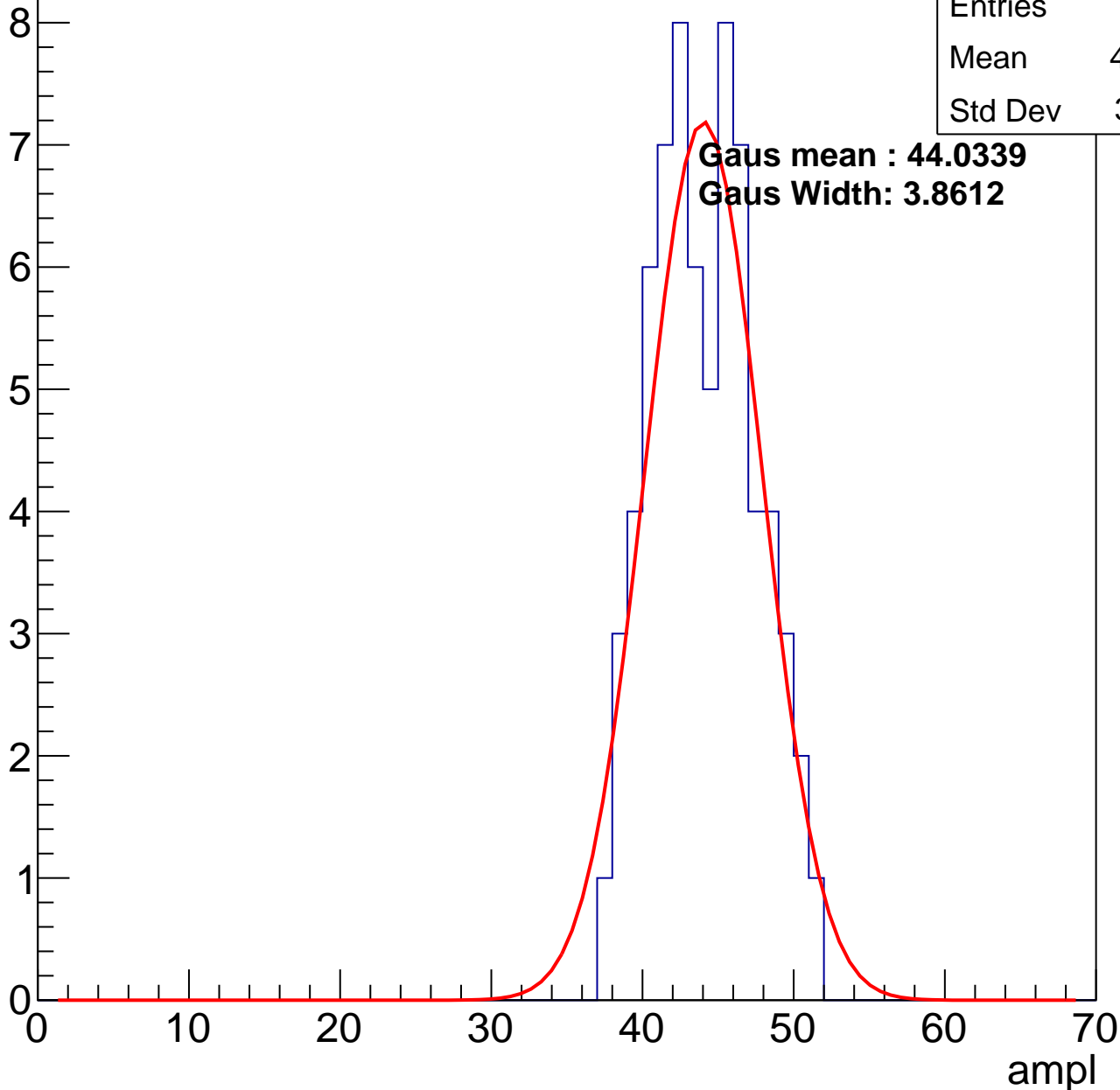
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	43.59
Std Dev	3.351

**Gaus mean : 44.0339**

**Gaus Width: 3.8612**

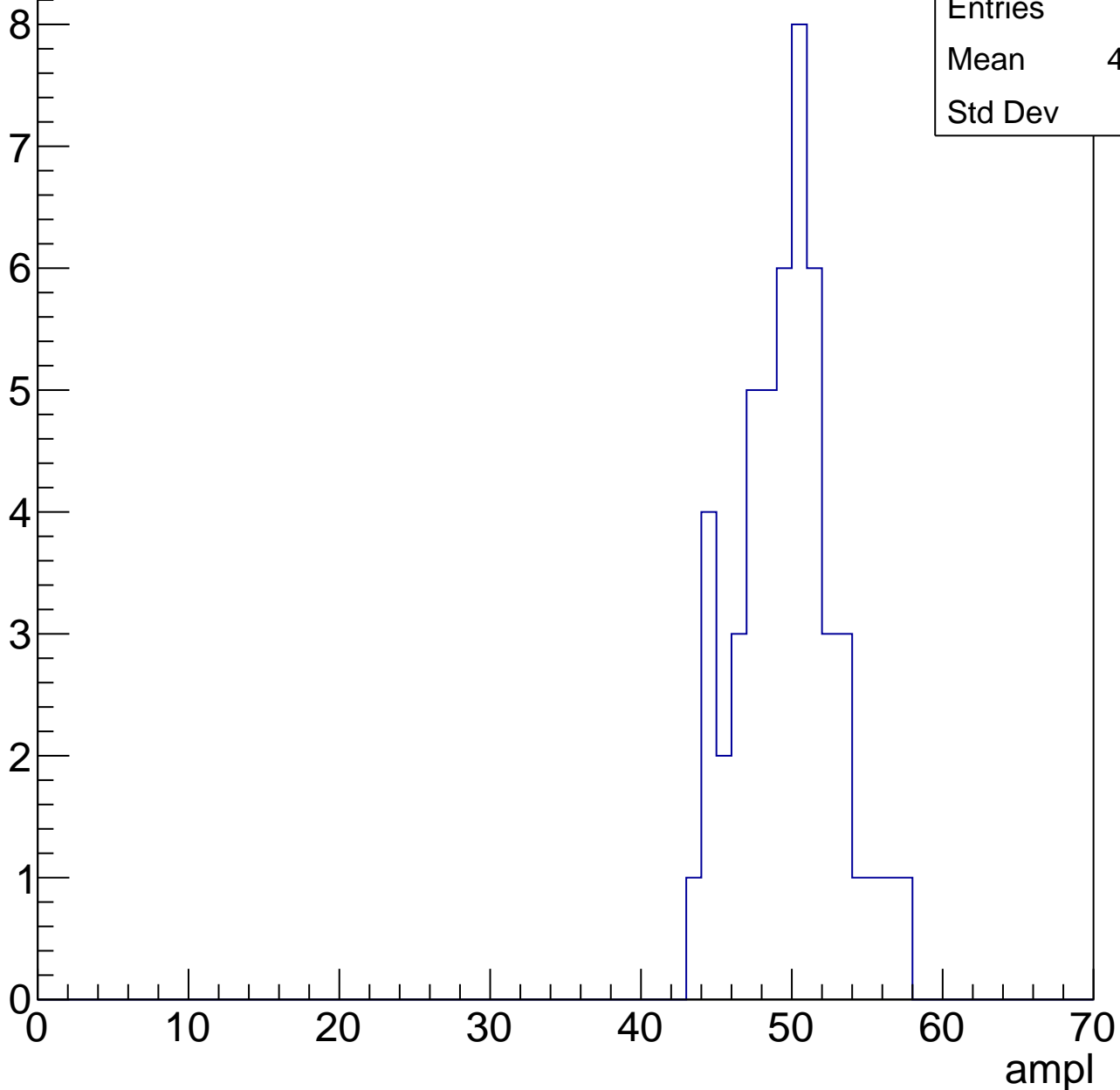


# B0L001S, U10-ch114, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

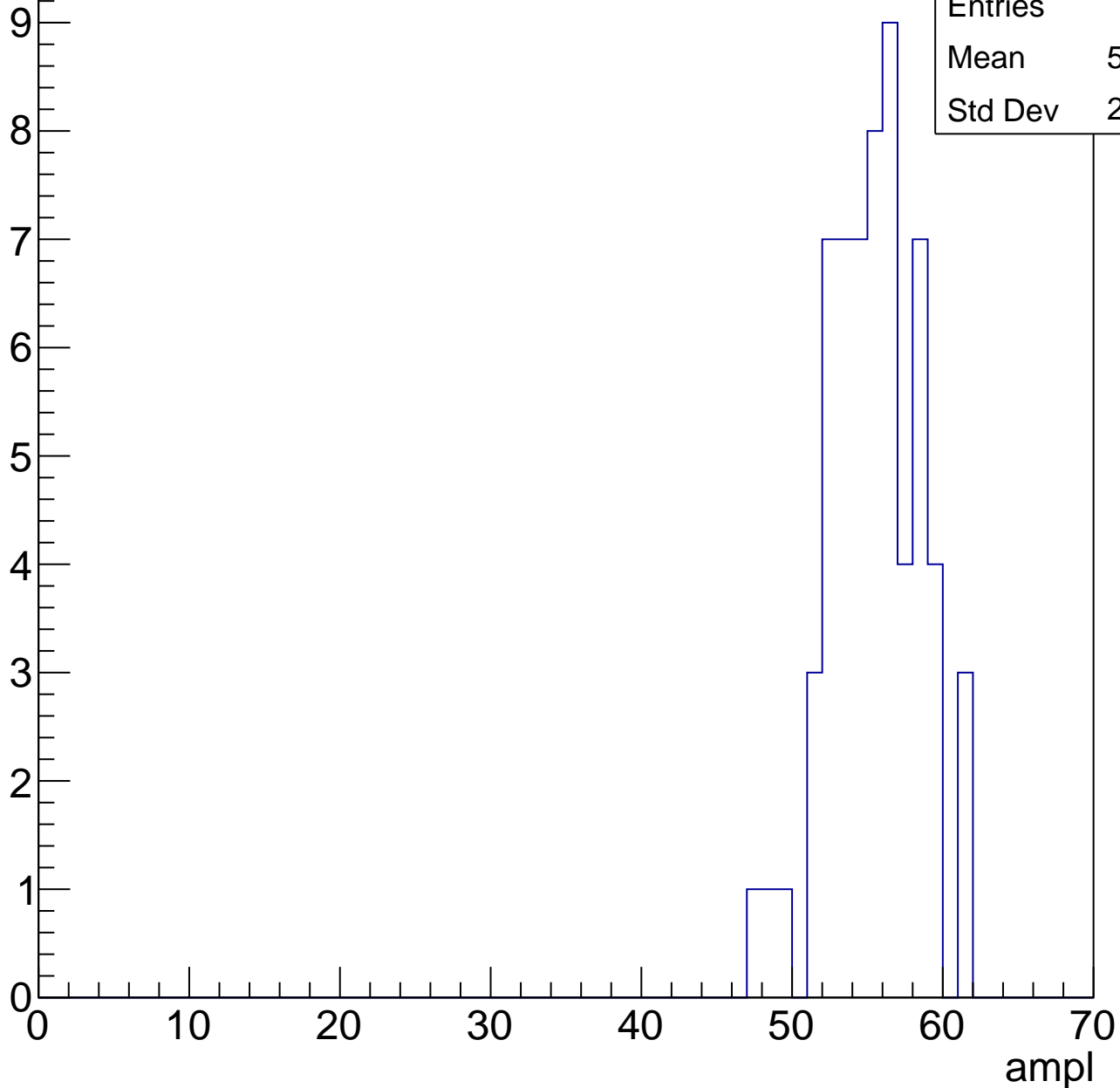
Entries	50
Mean	49.18
Std Dev	3.16



# B0L001S, U10-ch114, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U10-ch114, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

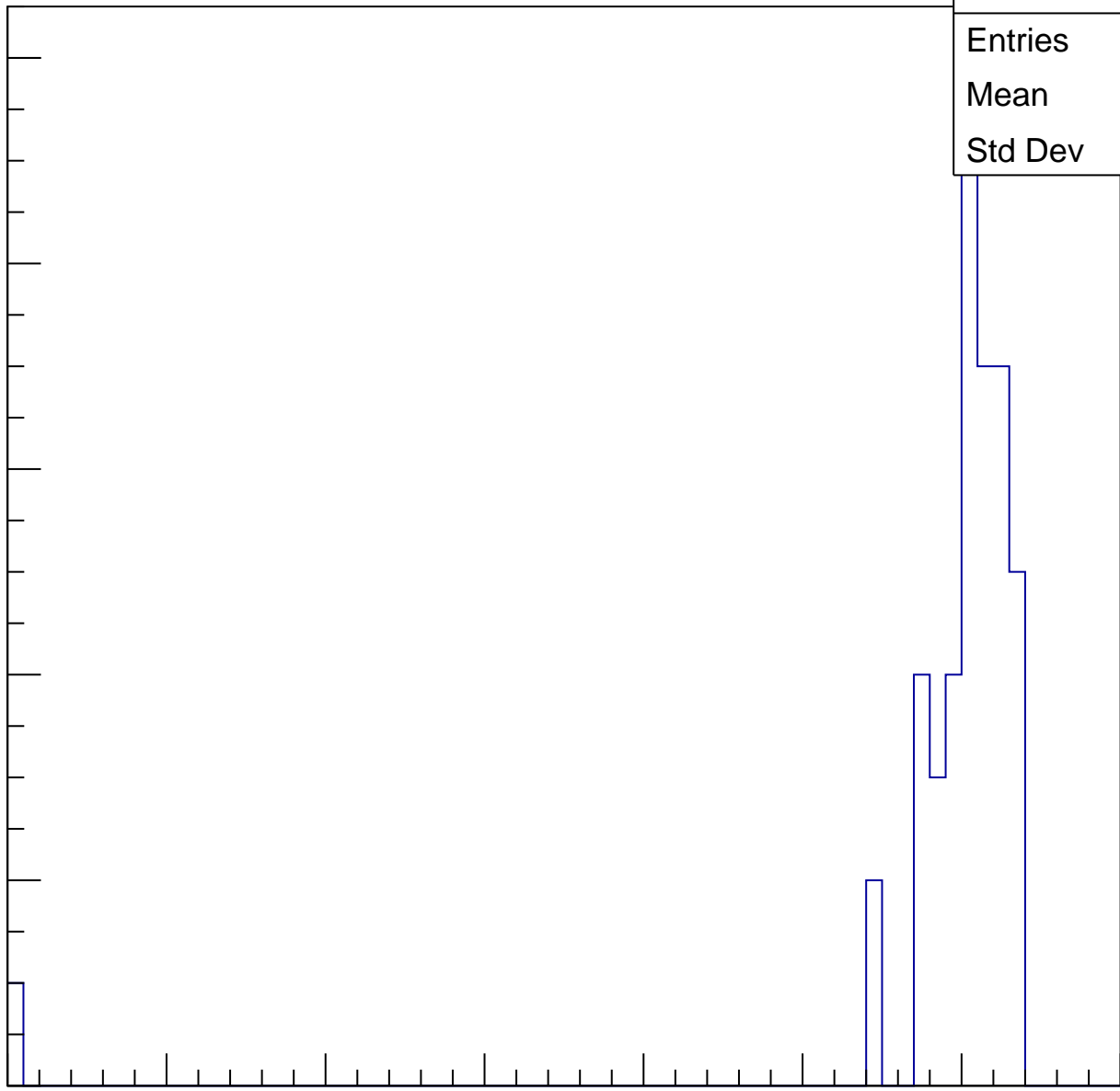
Entries	43
Mean	58.65
Std Dev	9.308

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

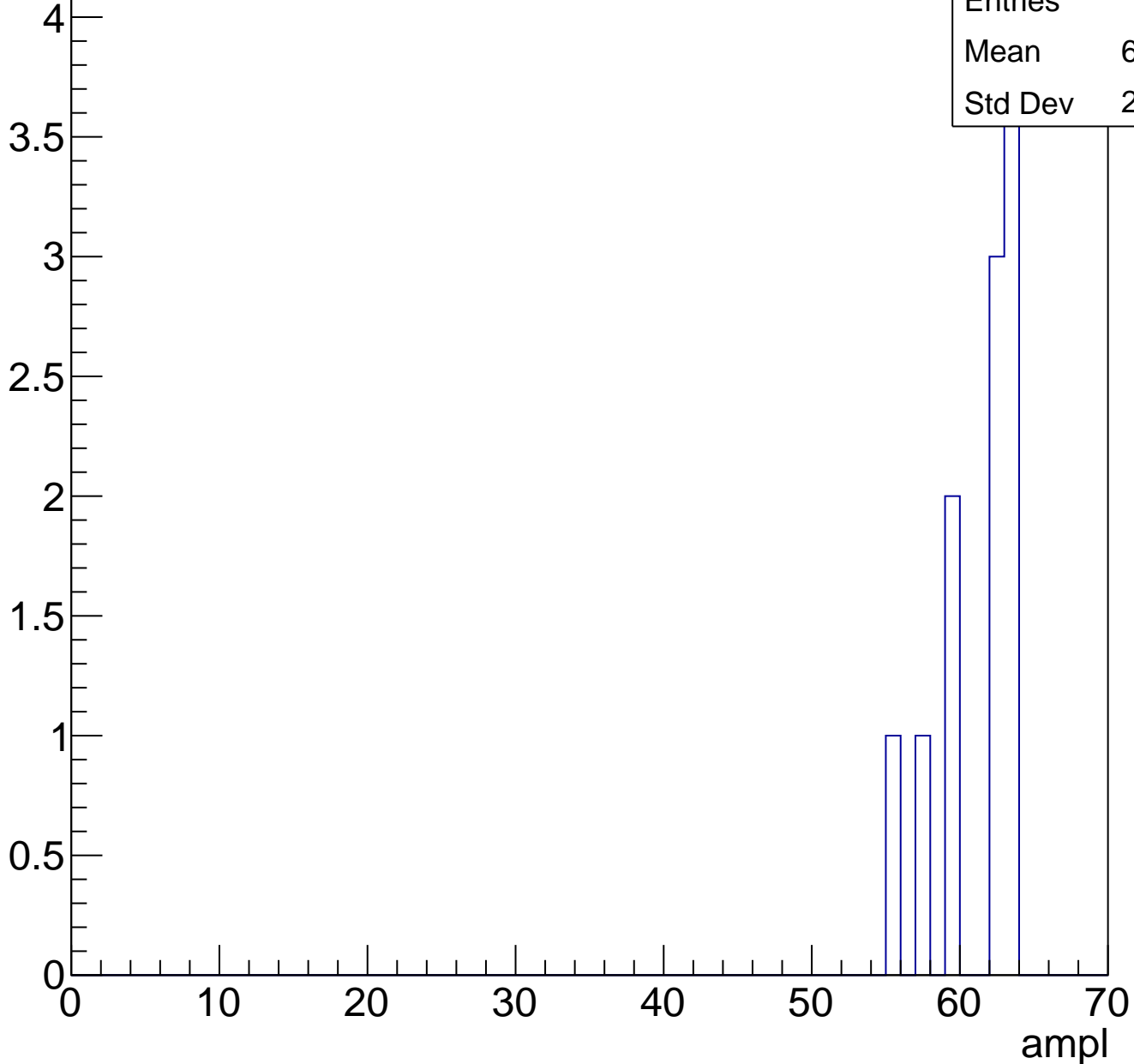
ampl



# B0L001S, U10-ch114, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch114, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U10-ch115, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	77
Mean	32.66
Std Dev	3.66

**Gaus mean : 33.0065**

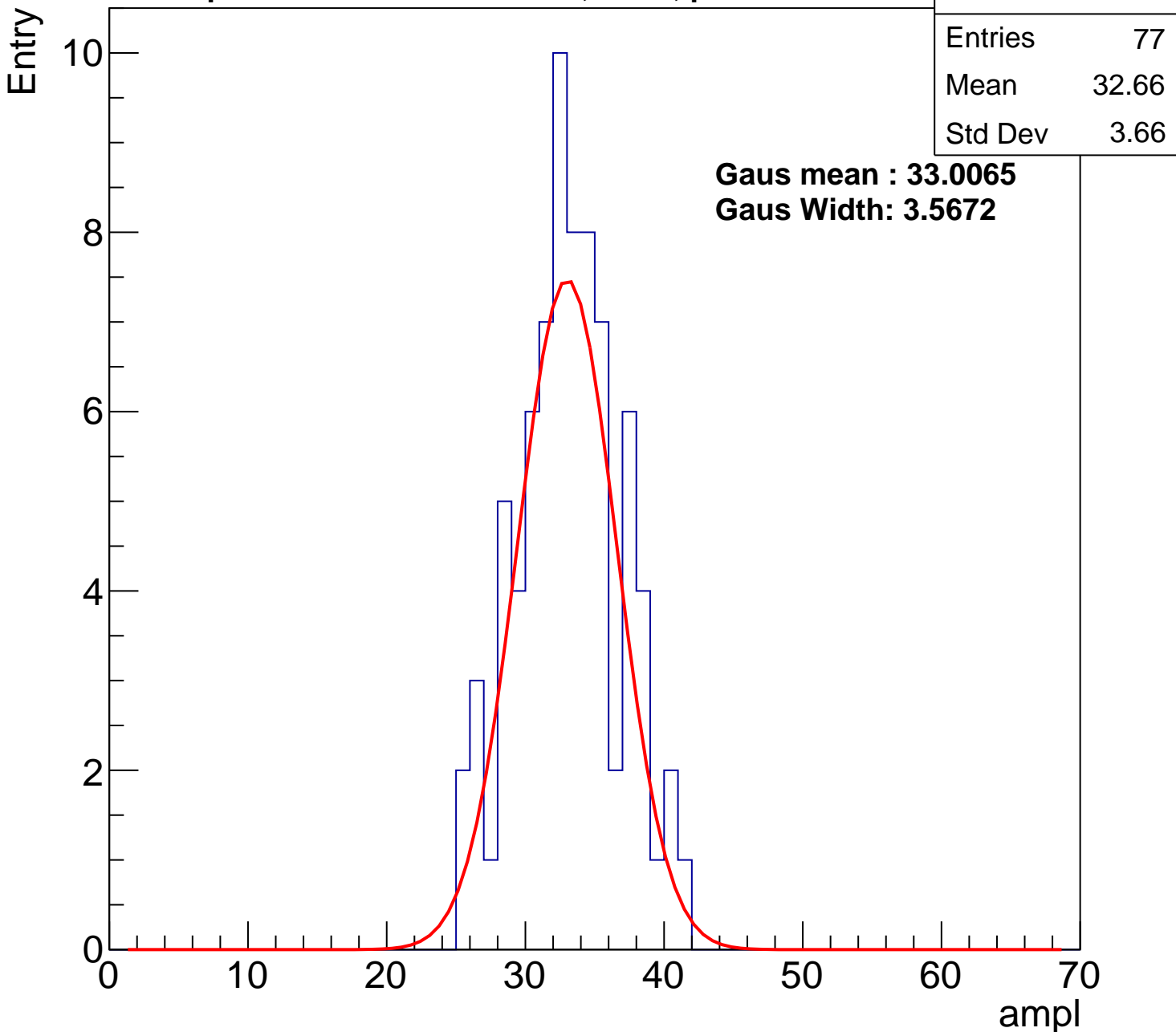
**Gaus Width: 3.5672**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U10-ch115, adc1

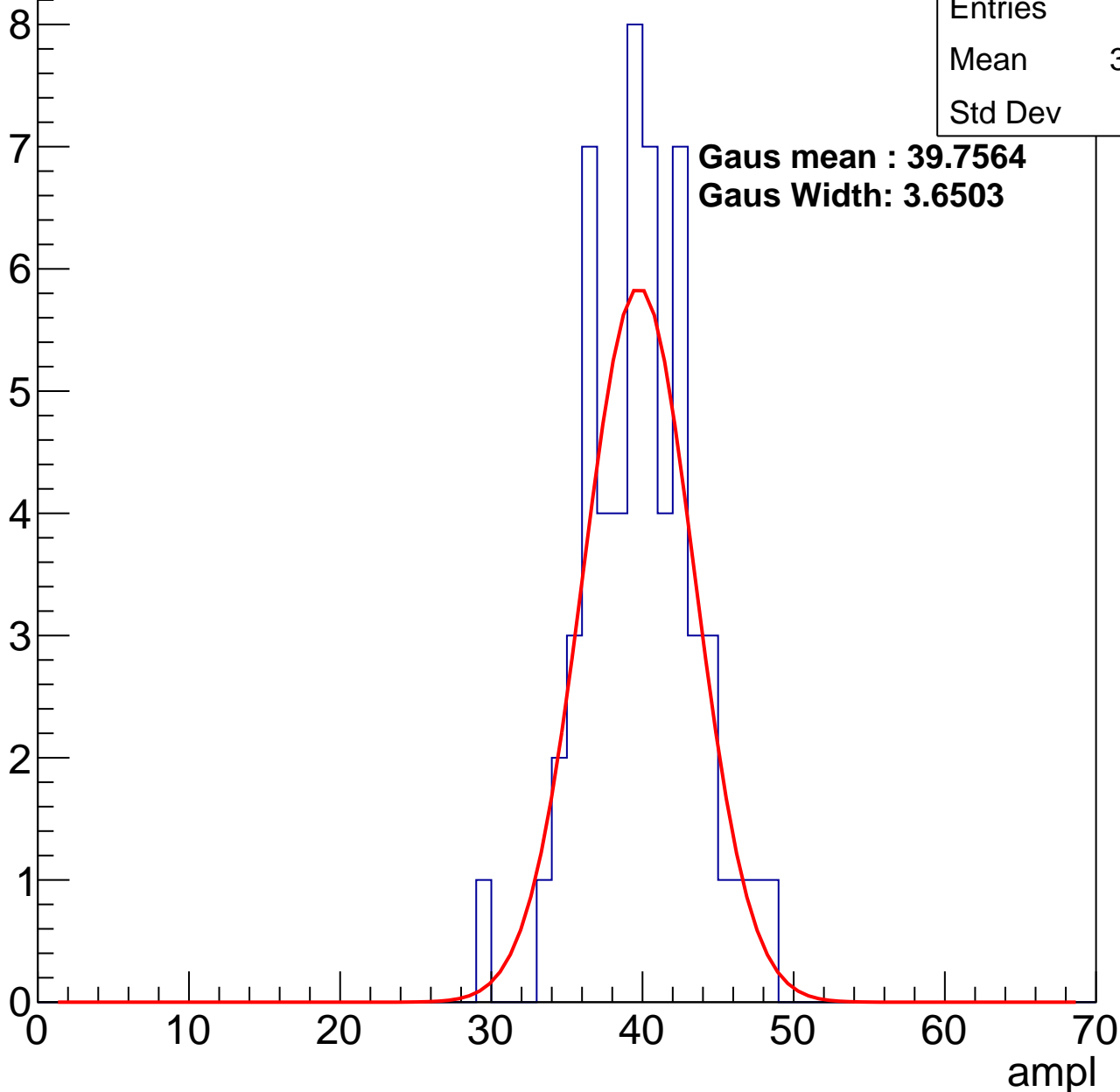
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	39.38
Std Dev	3.59

**Gaus mean : 39.7564**

**Gaus Width: 3.6503**



# B0L001S, U10-ch115, adc2

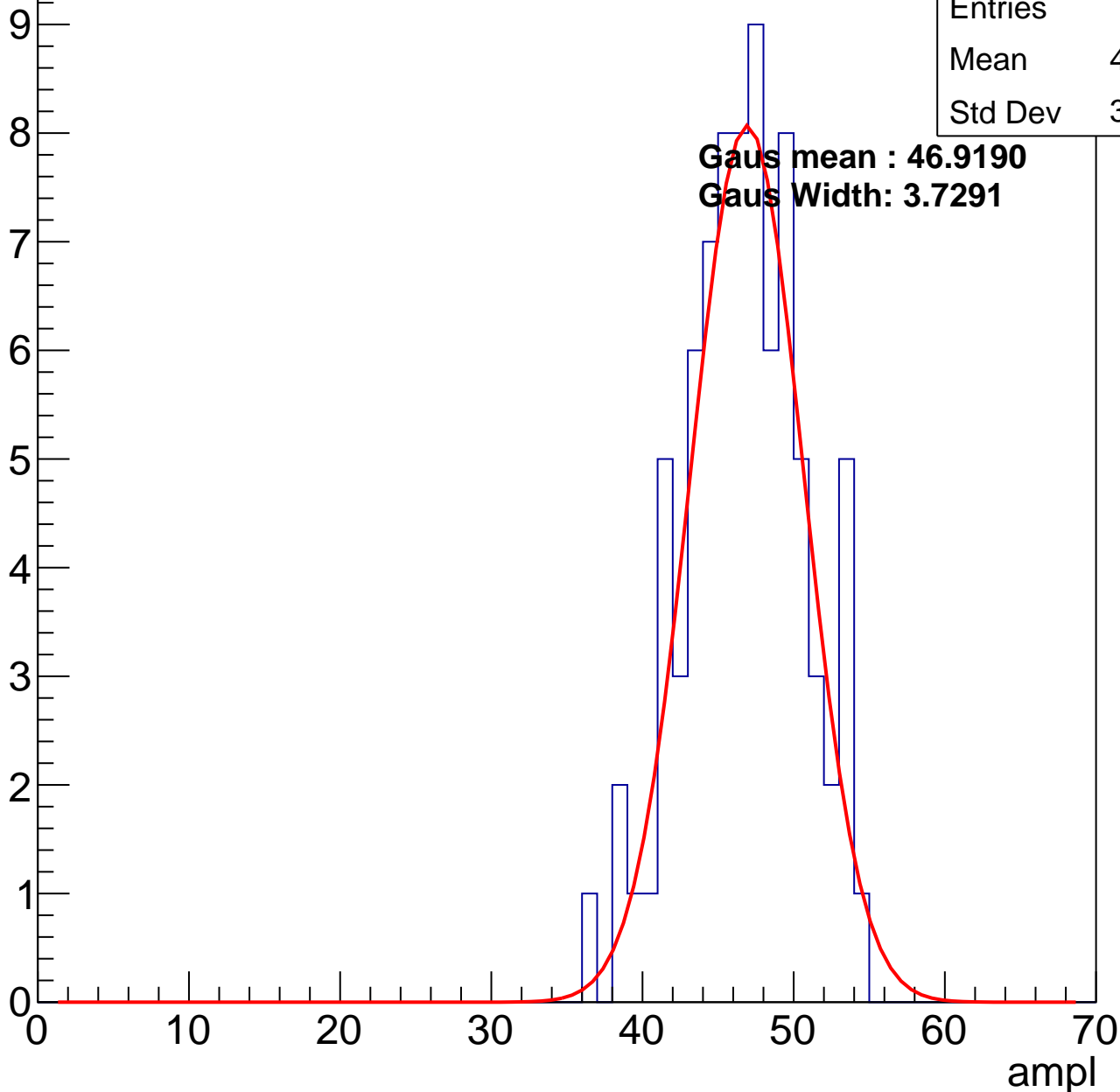
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	81
Mean	46.23
Std Dev	3.869

**Gaus mean : 46.9190**

**Gaus Width: 3.7291**

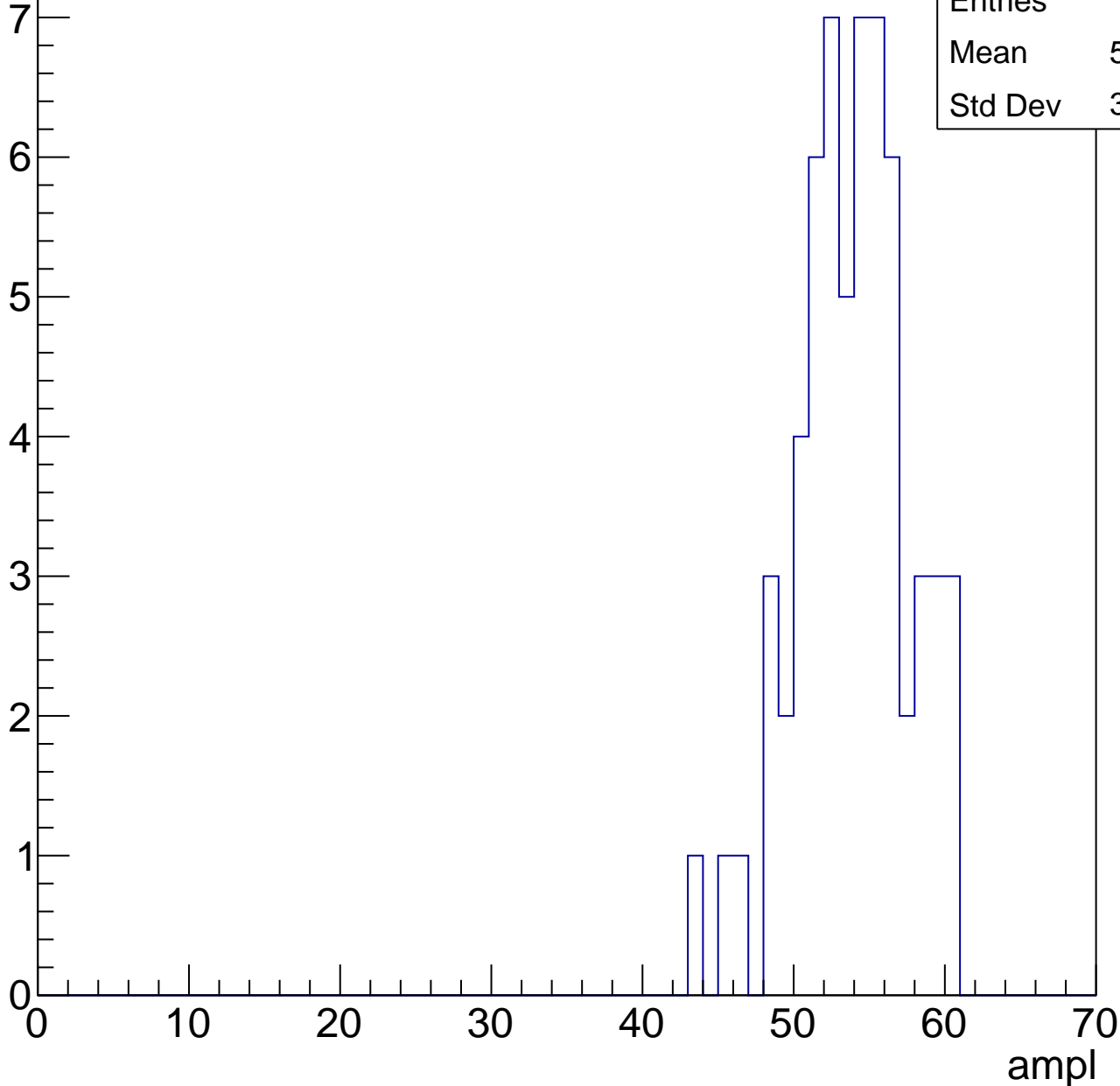


# B0L001S, U10-ch115, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	53.36
Std Dev	3.689

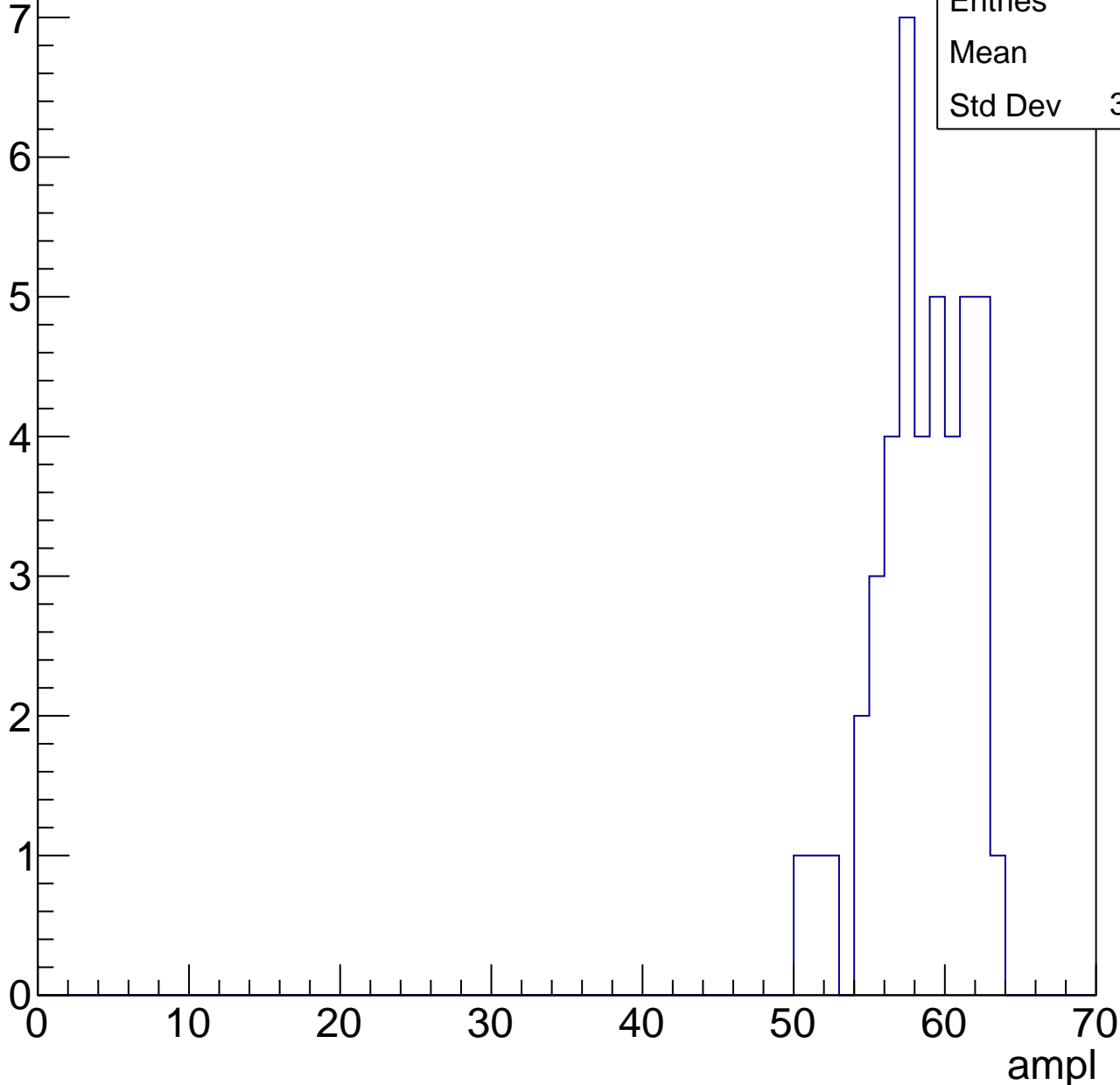


# B0L001S, U10-ch115, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	43
Mean	58
Std Dev	3.058

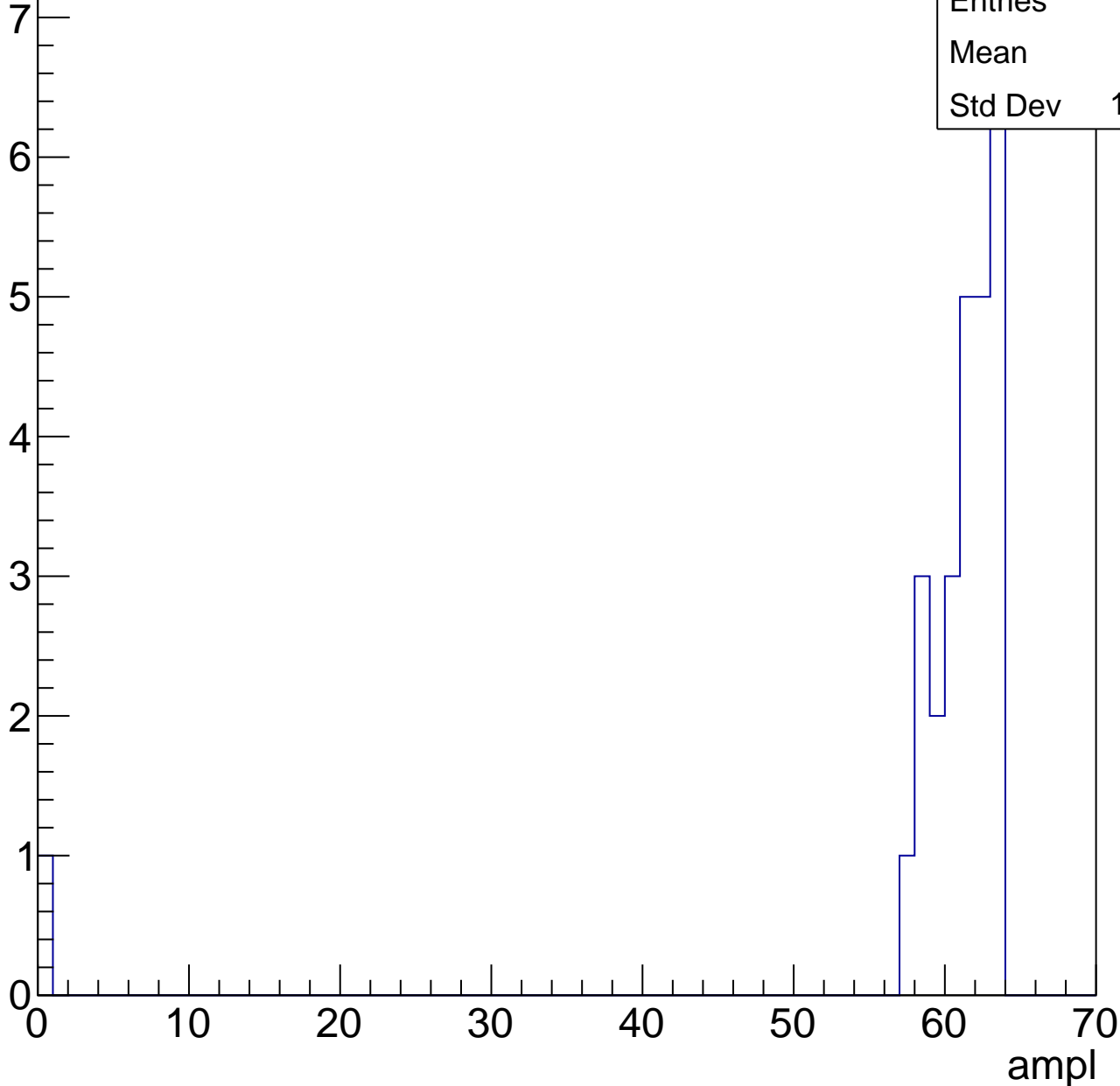


# B0L001S, U10-ch115, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	27
Mean	58.7
Std Dev	11.65



# B0L001S, U10-ch115, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	63
Std Dev	0

ampl



# B0L001S, U10-ch115, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U10-ch116, adc0

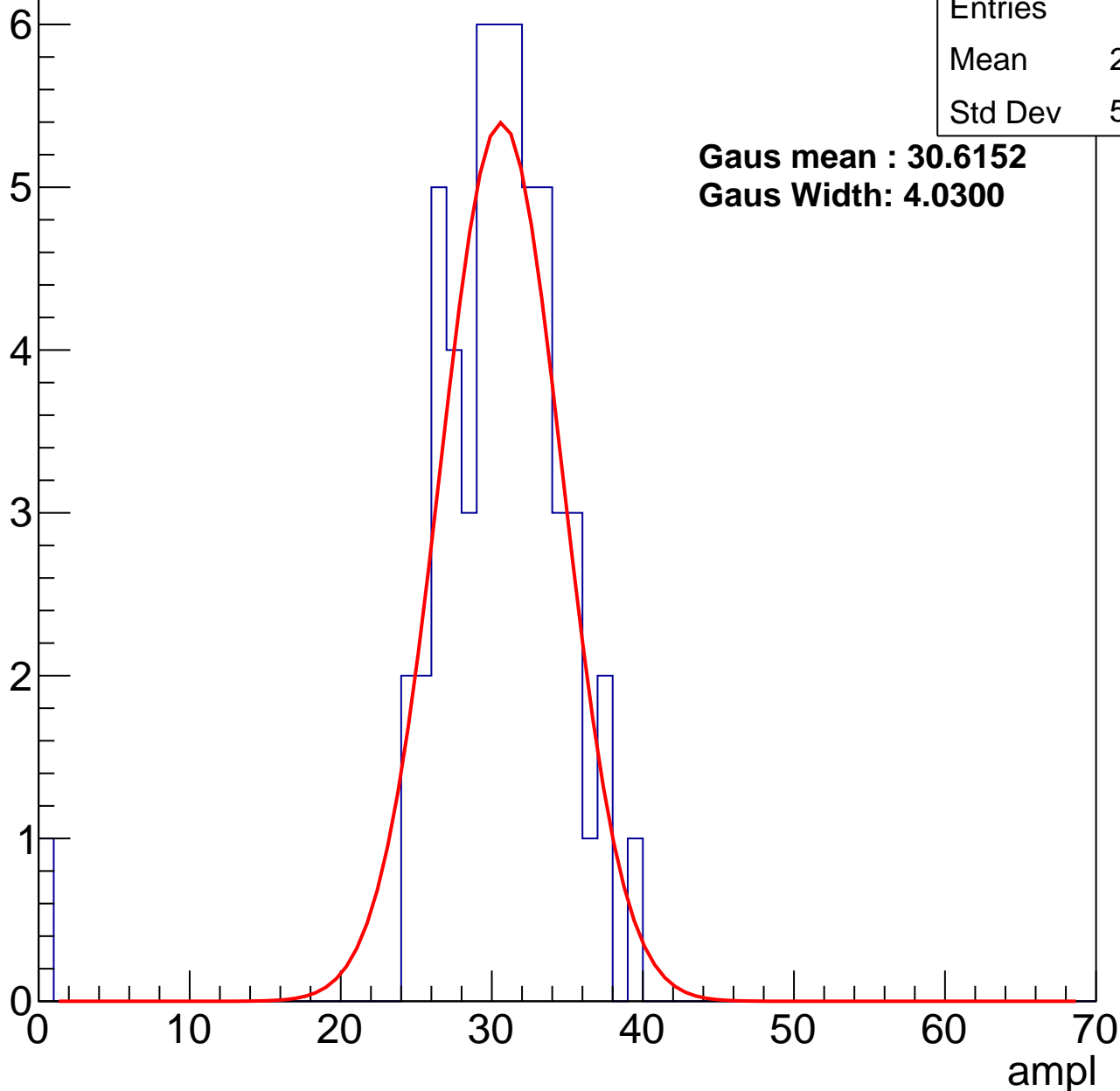
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	29.84
Std Dev	5.332

**Gaus mean : 30.6152**

**Gaus Width: 4.0300**



# B0L001S, U10-ch116, adc1

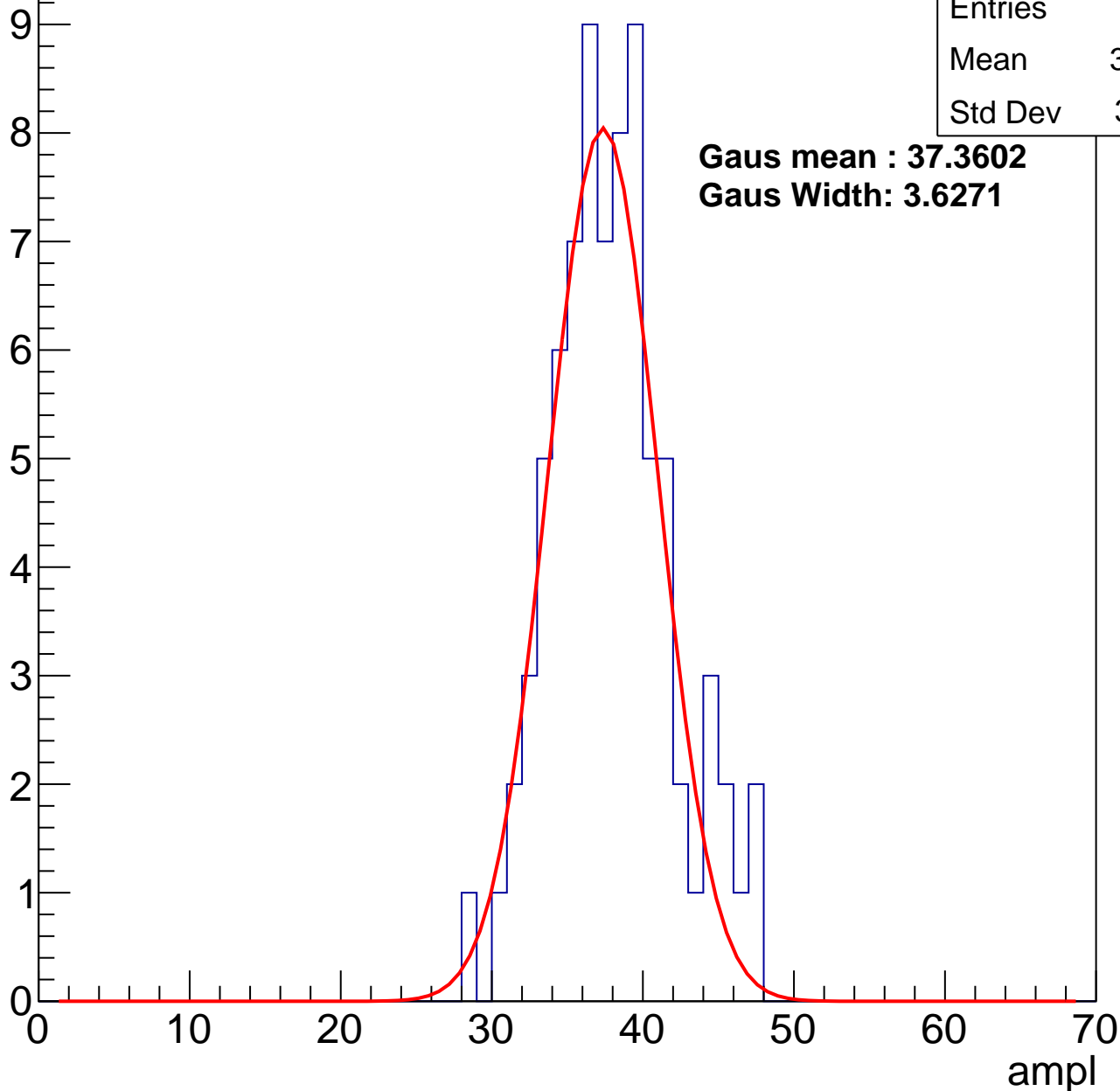
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	79
Mean	37.49
Std Dev	3.961

**Gaus mean : 37.3602**

**Gaus Width: 3.6271**



# B0L001S, U10-ch116, adc2

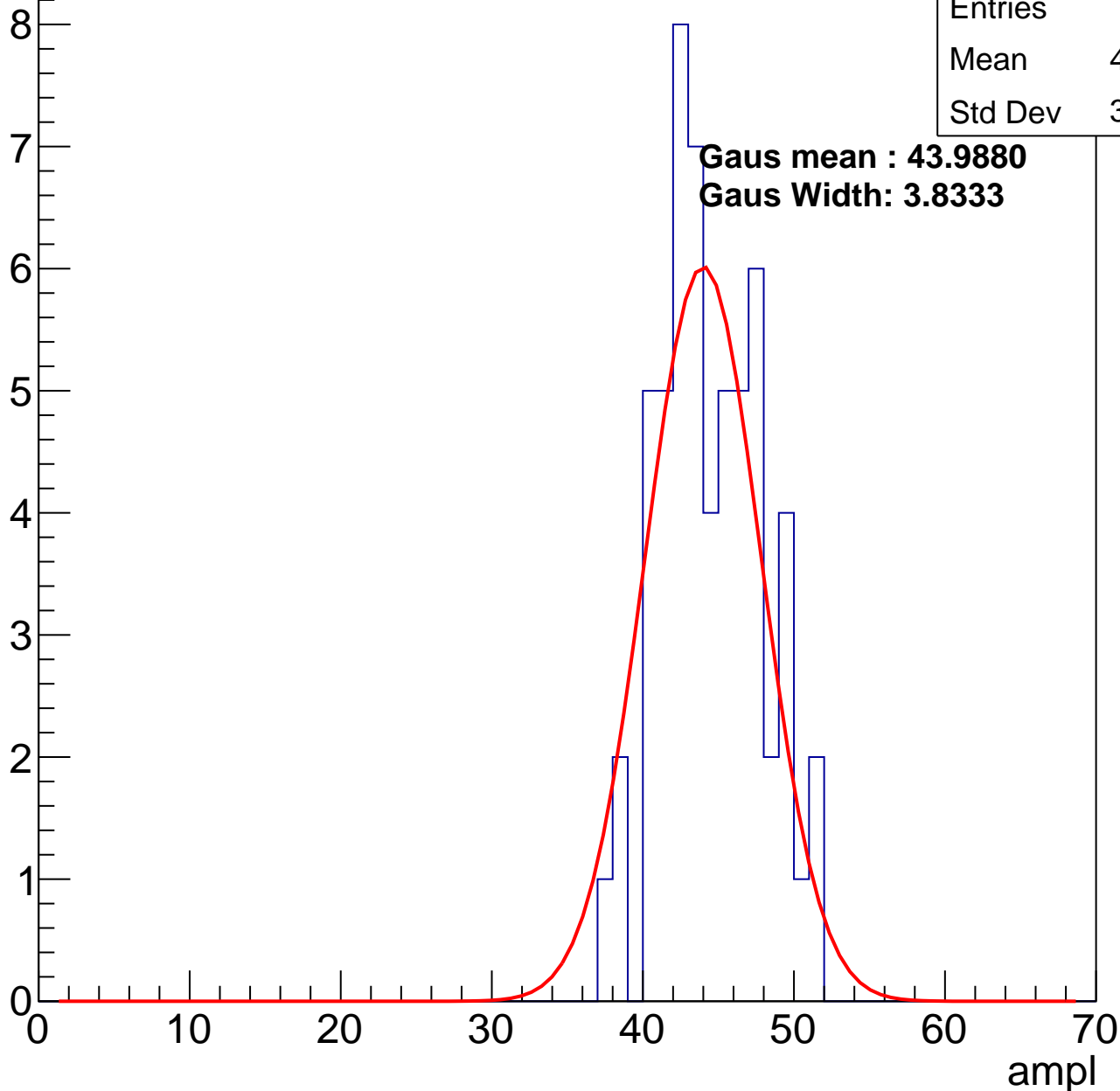
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	44.07
Std Dev	3.324

**Gaus mean : 43.9880**

**Gaus Width: 3.8333**

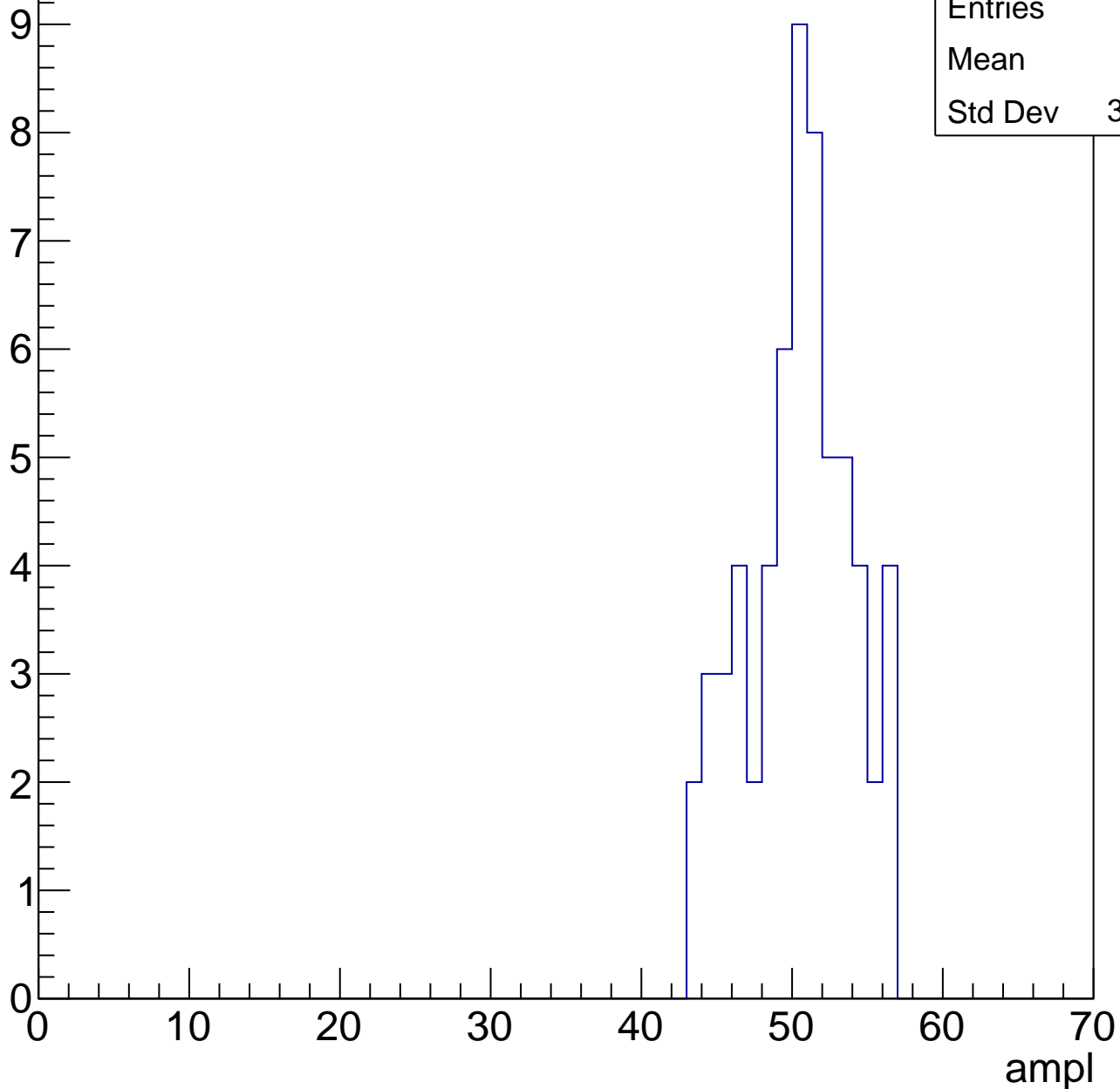


# B0L001S, U10-ch116, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	50
Std Dev	3.426

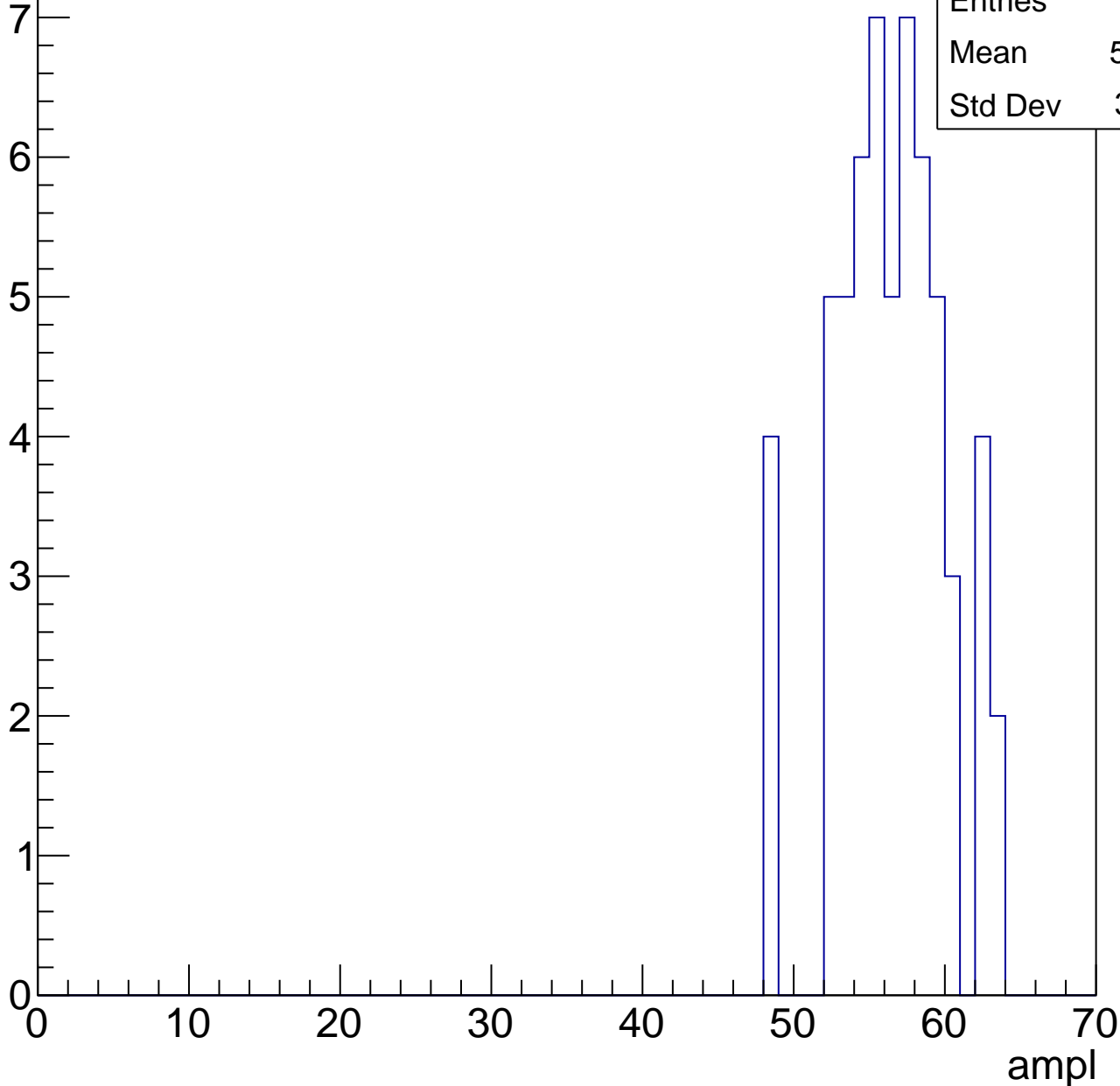


# B0L001S, U10-ch116, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	55.97
Std Dev	3.631

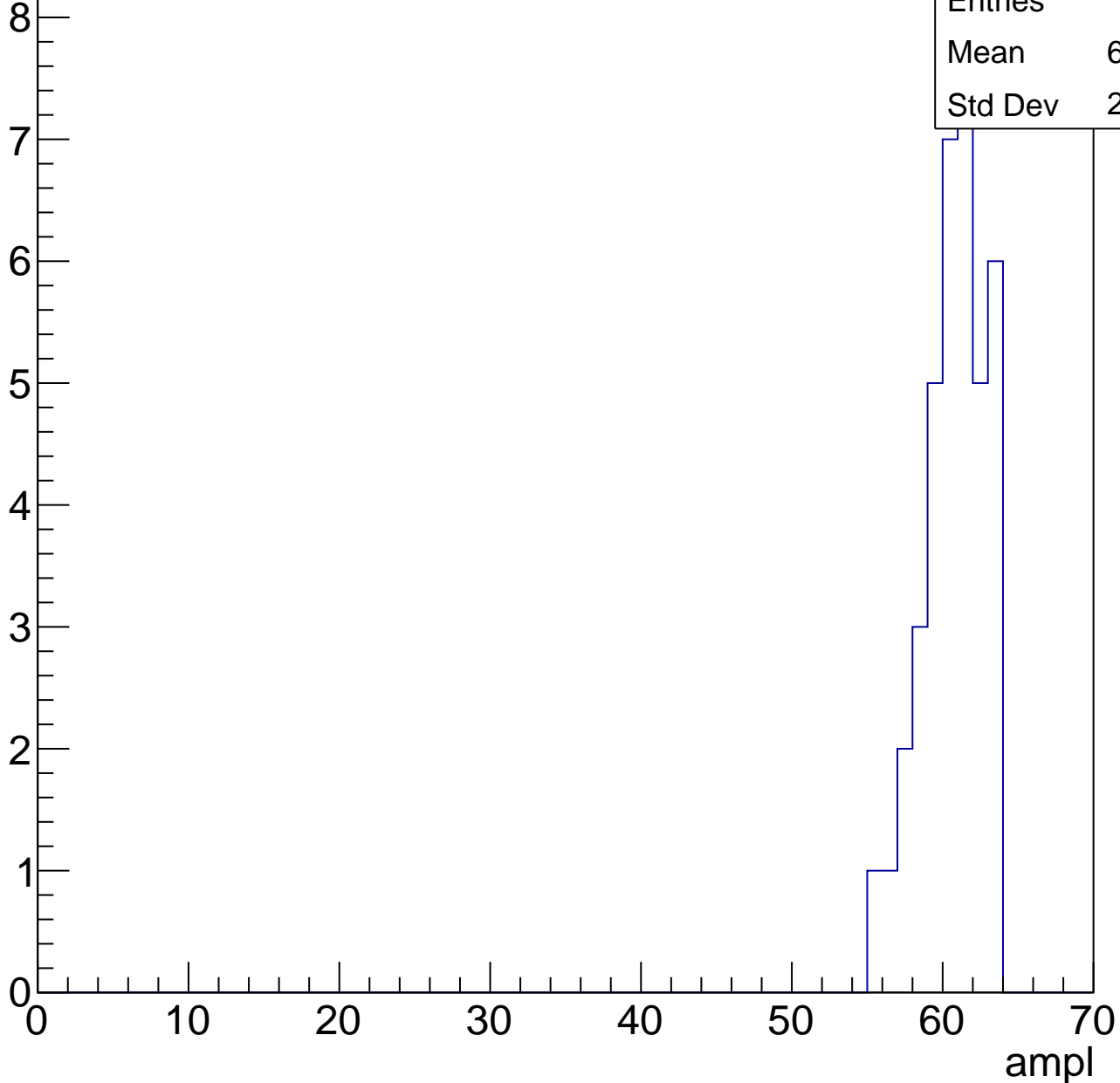


# B0L001S, U10-ch116, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	38
Mean	60.26
Std Dev	2.022



# B0L001S, U10-ch116, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

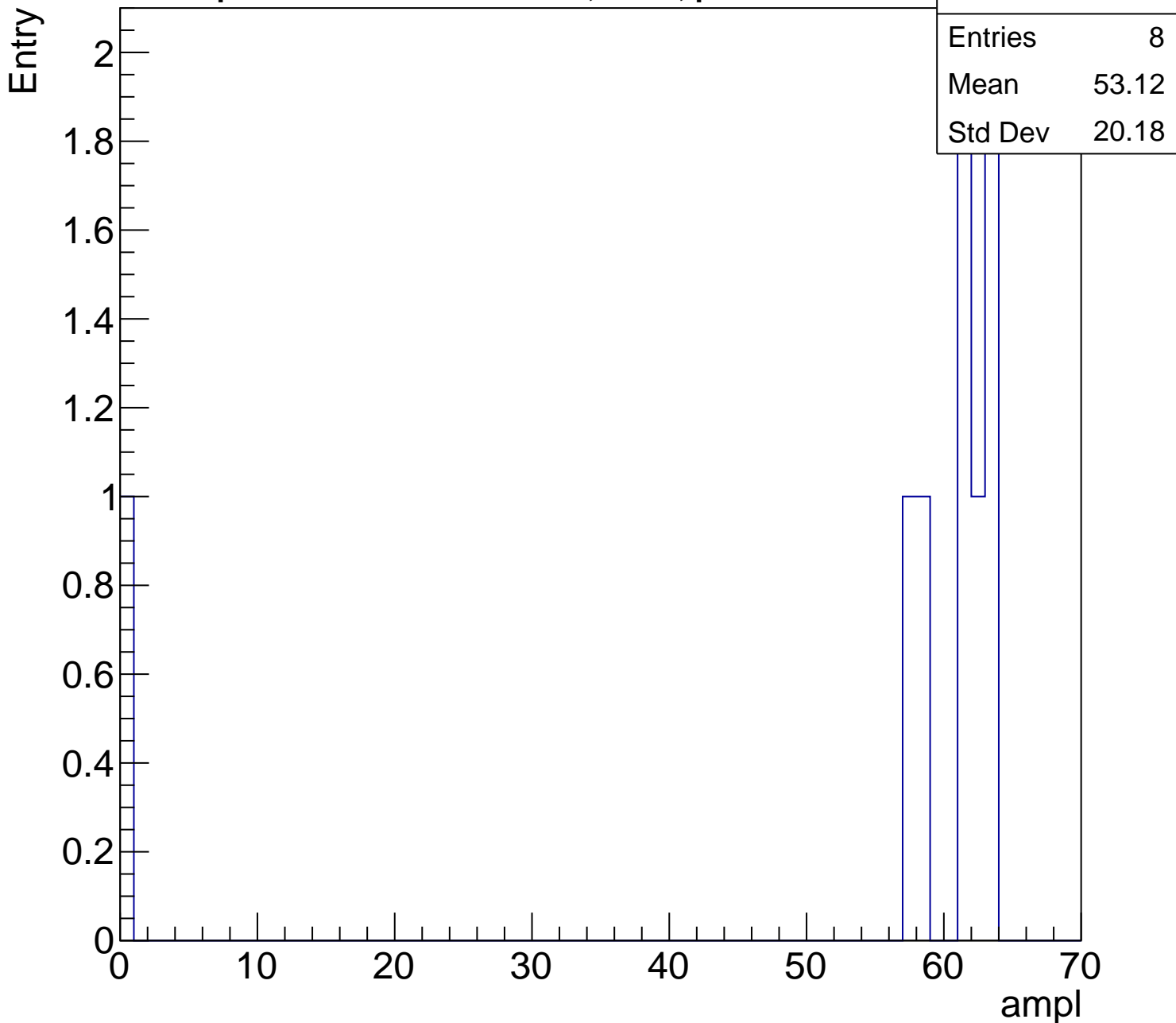
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	8
Mean	53.12
Std Dev	20.18

0 10 20 30 40 50 60 70

ampl





# B0L001S, U10-ch116, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U10-ch117, adc0

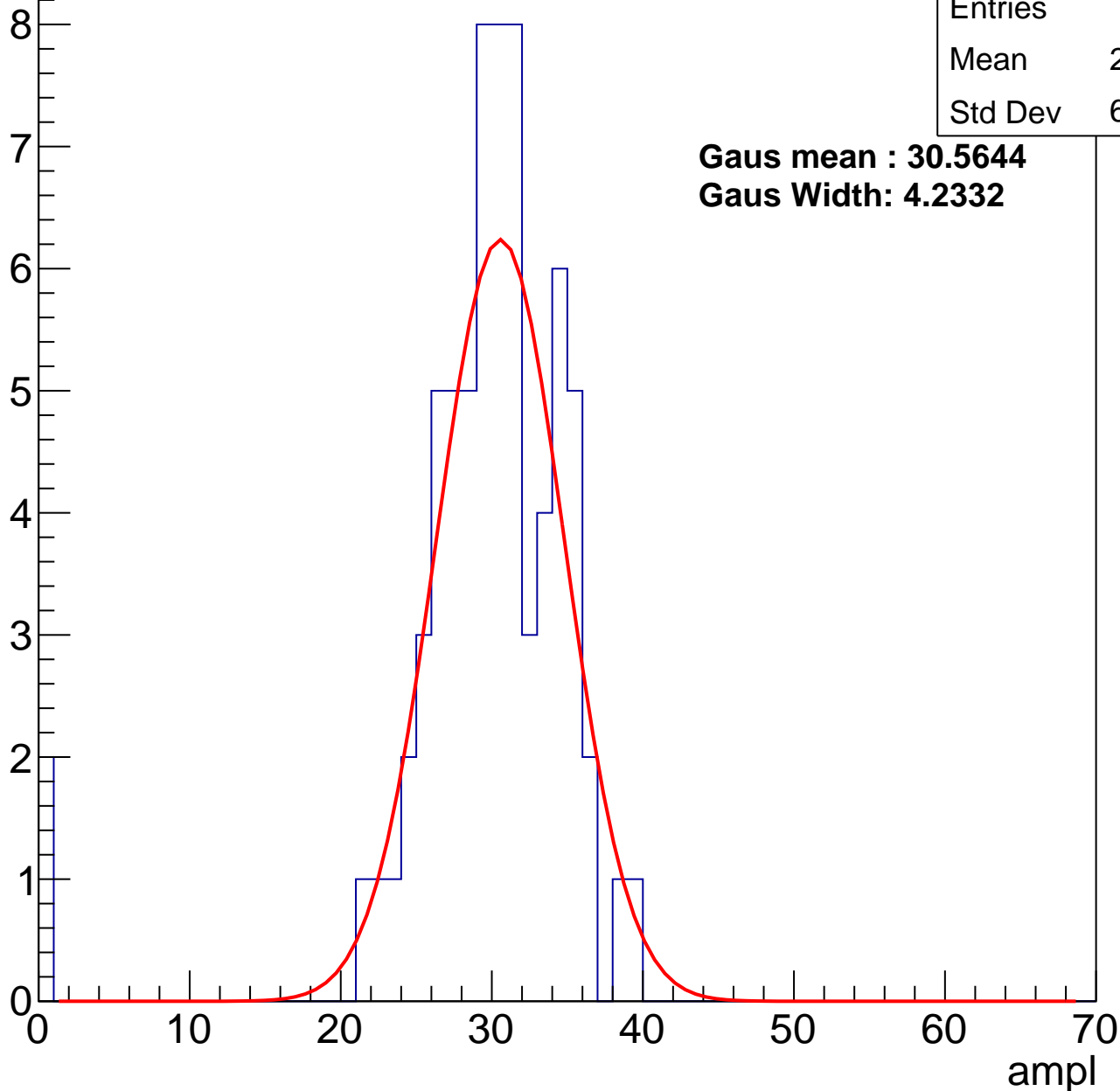
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	29.15
Std Dev	6.209

**Gaus mean : 30.5644**

**Gaus Width: 4.2332**



# B0L001S, U10-ch117, adc1

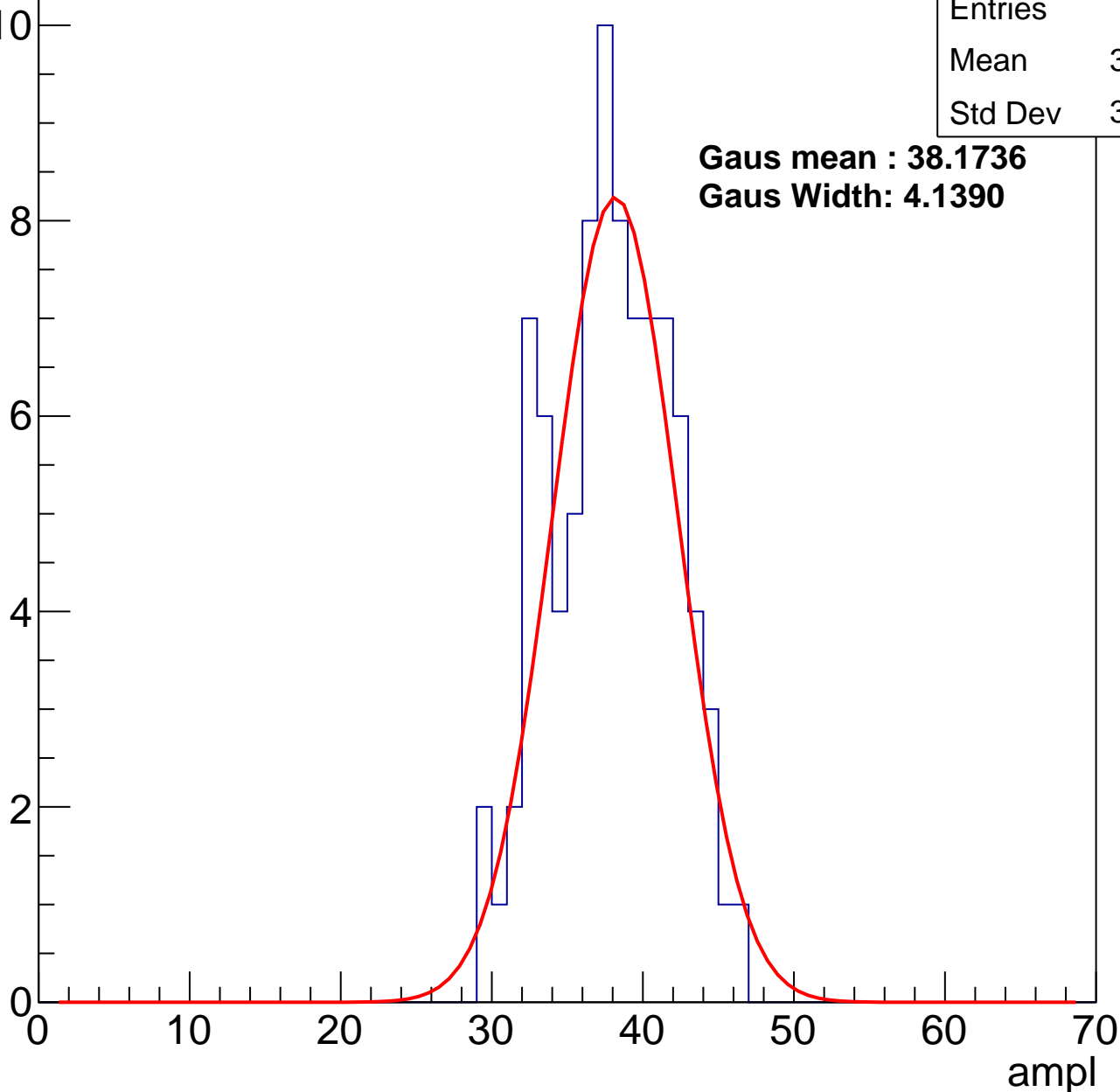
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	89
Mean	37.44
Std Dev	3.915

**Gaus mean : 38.1736**

**Gaus Width: 4.1390**



# B0L001S, U10-ch117, adc2

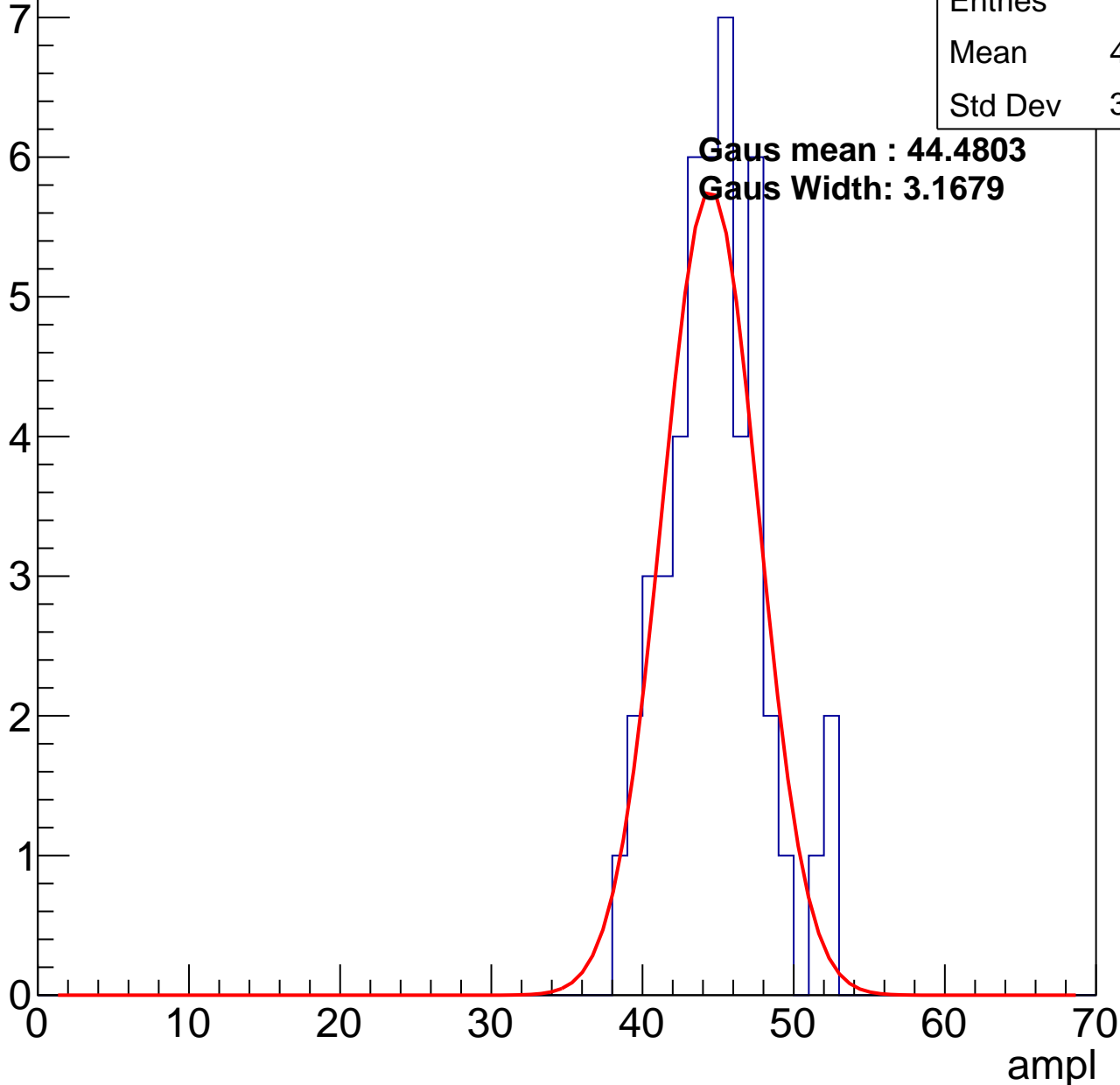
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	48
Mean	44.38
Std Dev	3.186

**Gaus mean : 44.4803**

**Gaus Width: 3.1679**



# B0L001S, U10-ch117, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

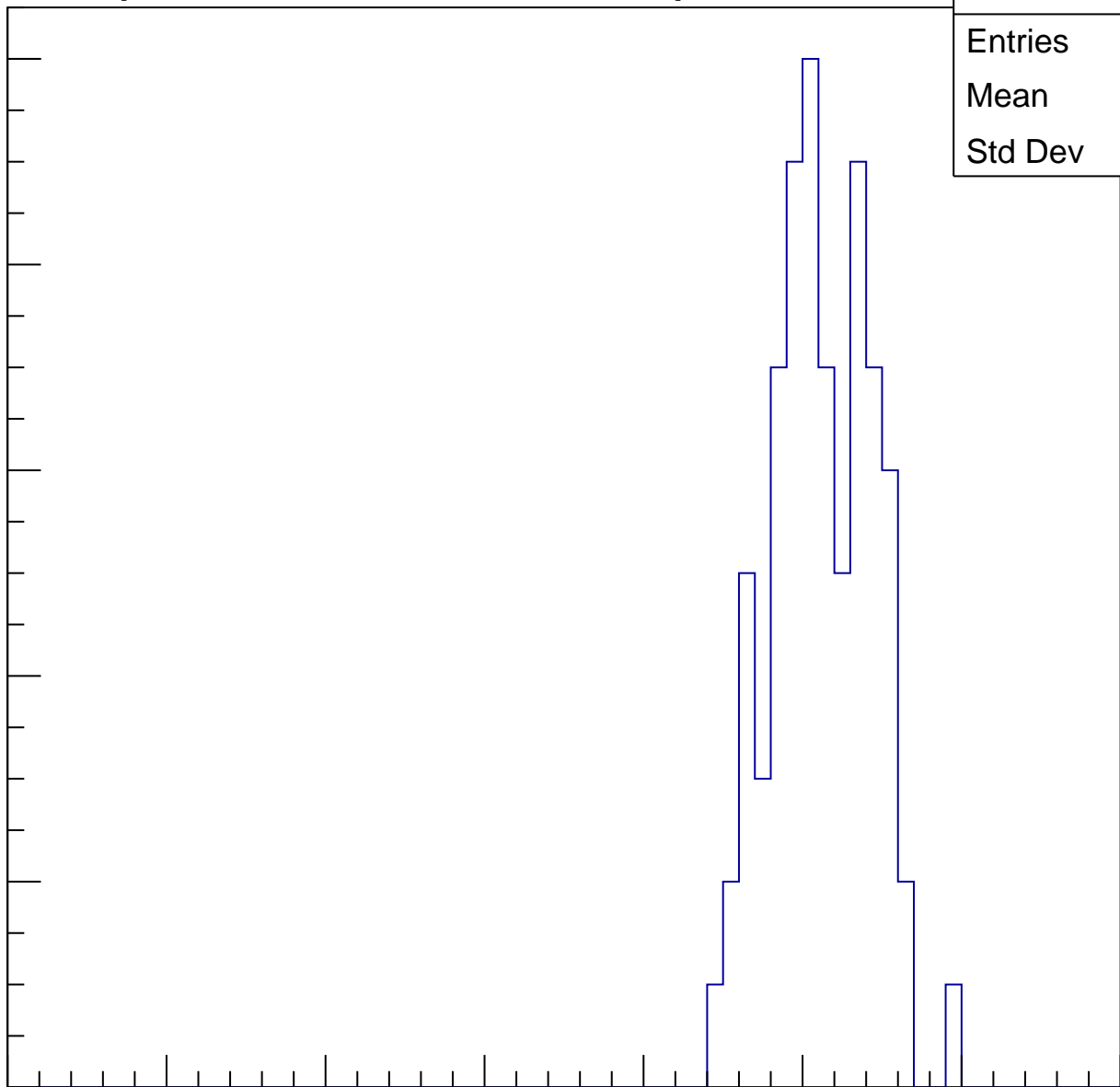
Entries	74
Mean	50.74
Std Dev	3.102

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

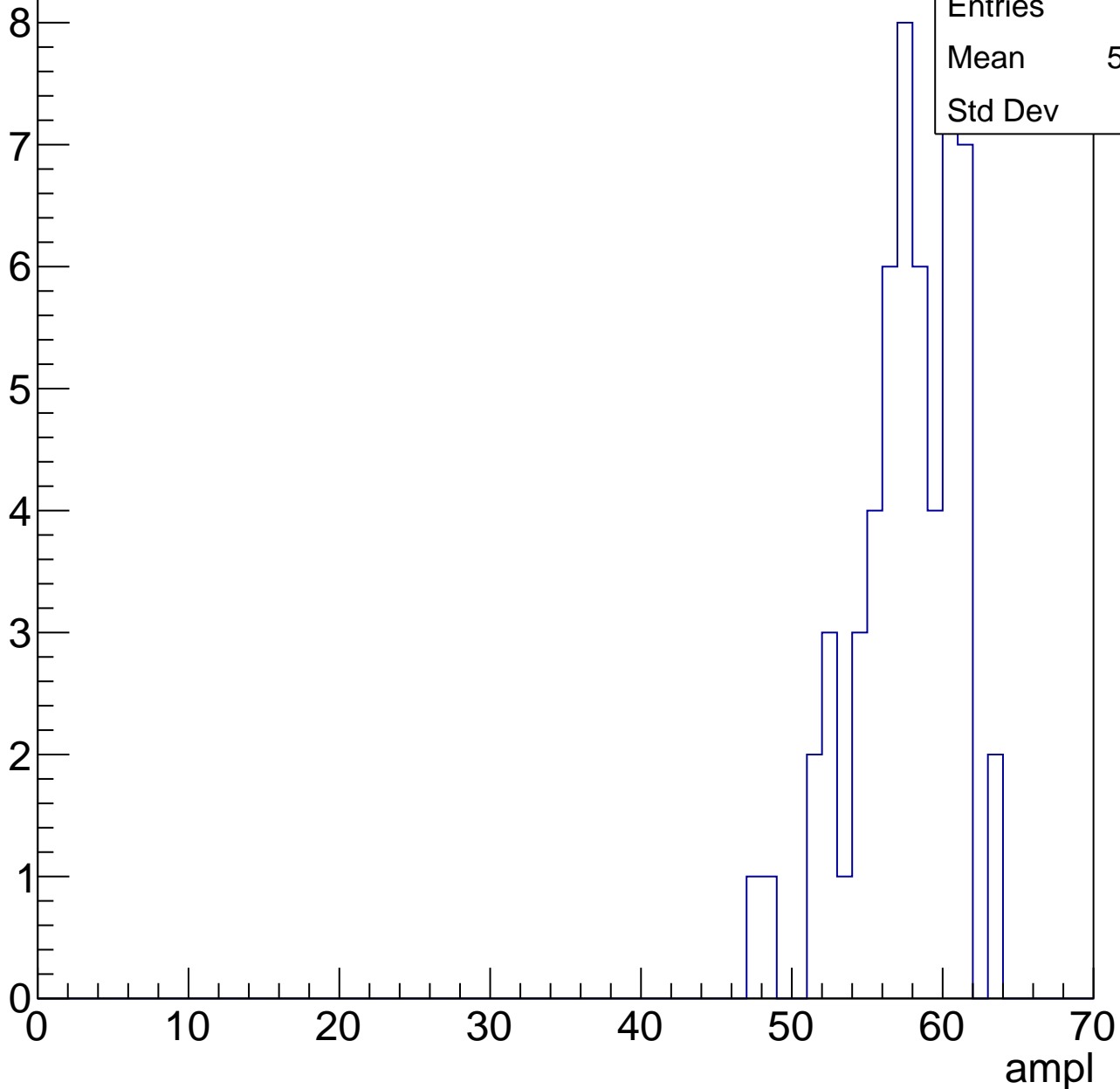


# B0L001S, U10-ch117, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	57.09
Std Dev	3.46

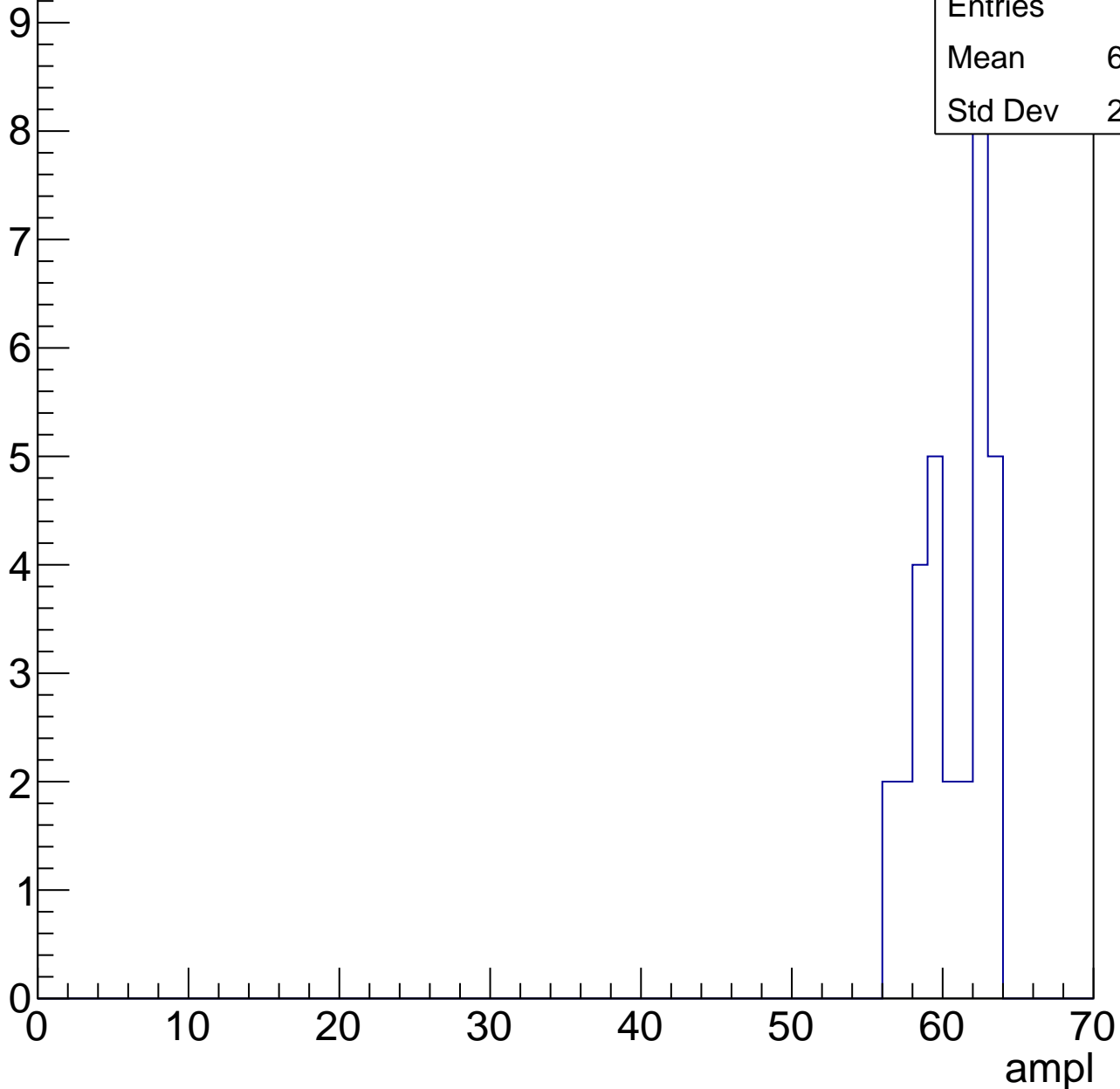


# B0L001S, U10-ch117, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	31
Mean	60.26
Std Dev	2.214



# B0L001S, U10-ch117, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch117, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	3
Mean	0
Std Dev	0

# B0L001S, U10-ch118, adc0

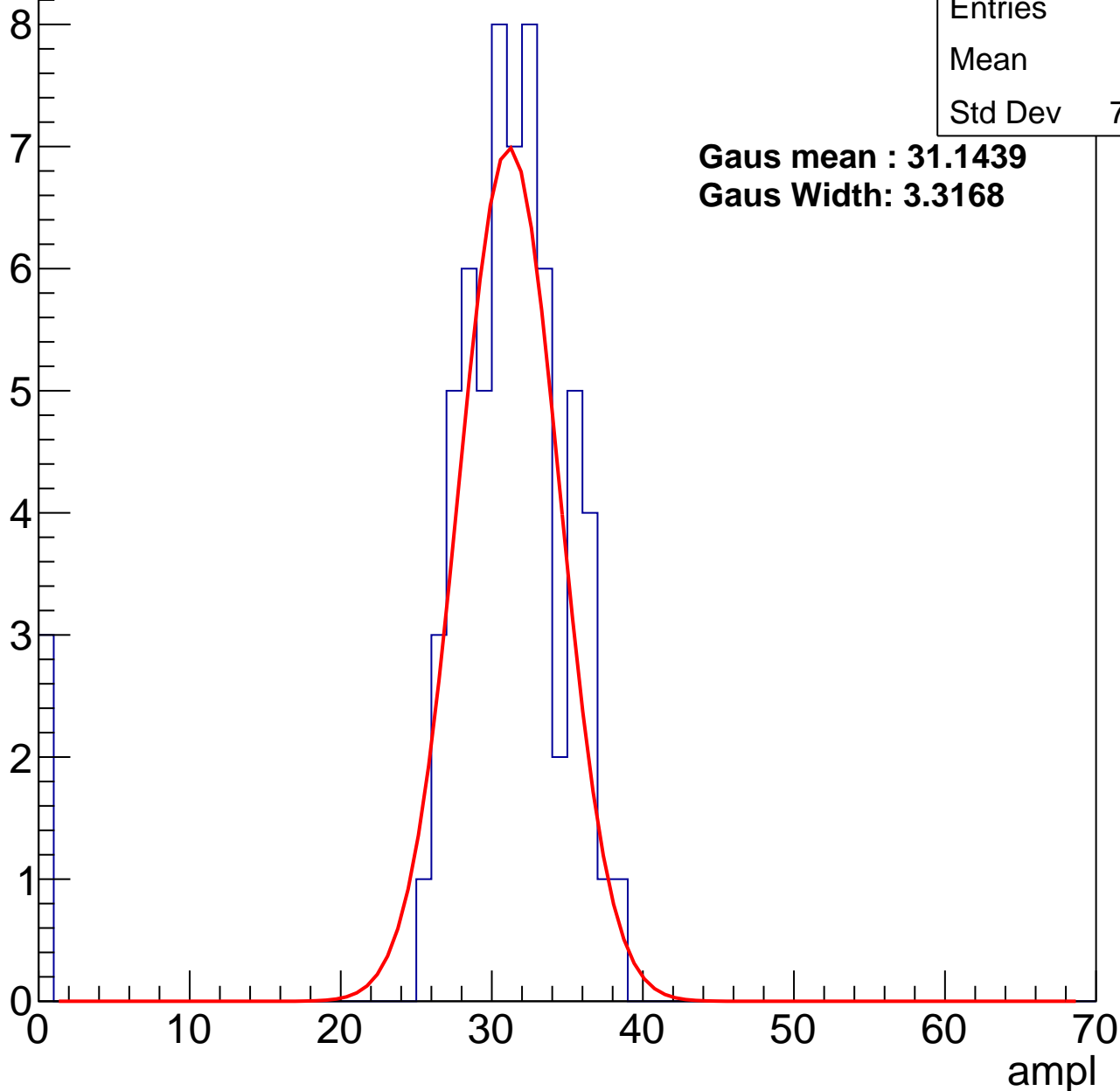
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	29.6
Std Dev	7.172

**Gaus mean : 31.1439**

**Gaus Width: 3.3168**



# B0L001S, U10-ch118, adc1

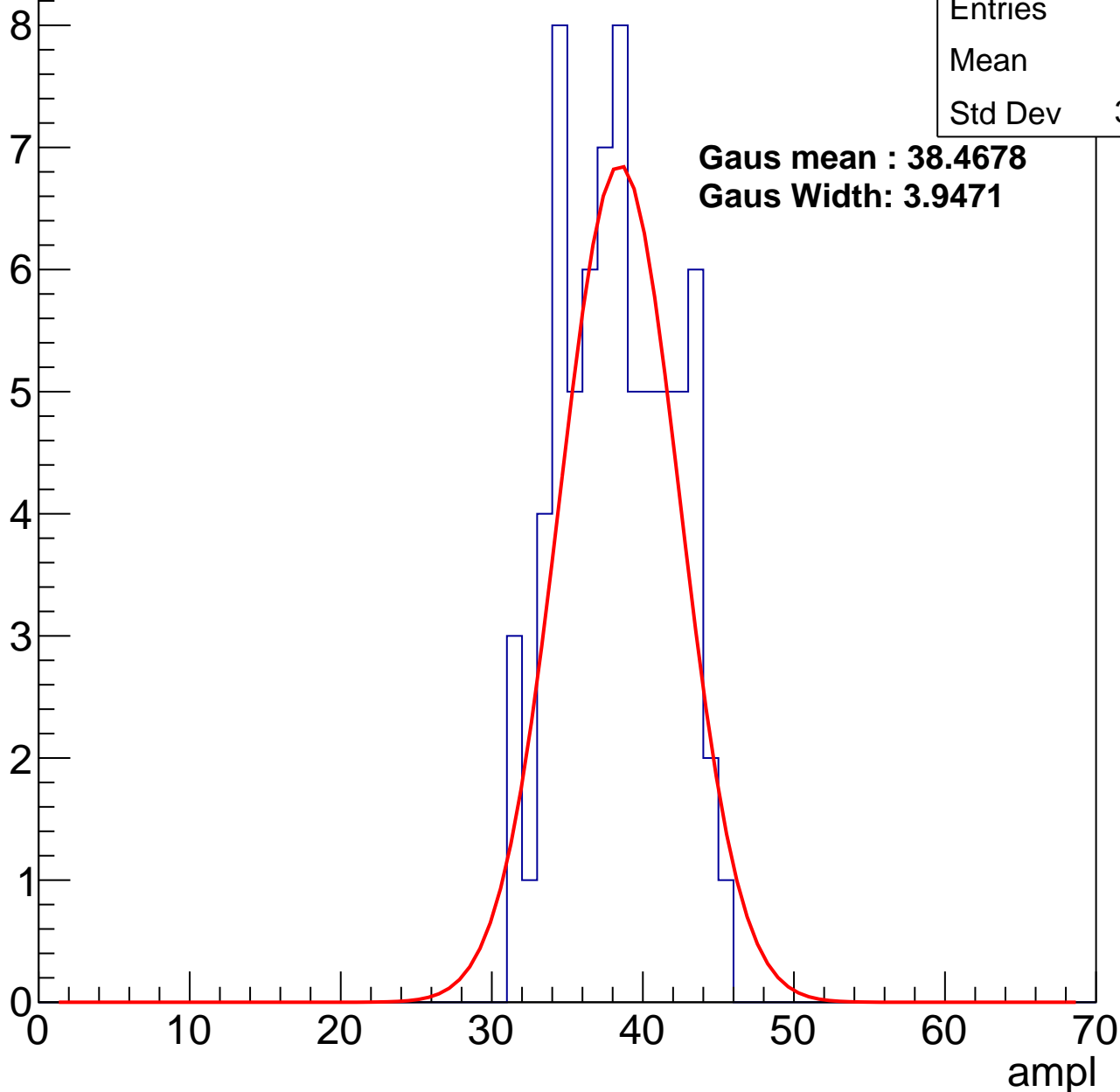
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	37.8
Std Dev	3.571

**Gaus mean : 38.4678**

**Gaus Width: 3.9471**



# B0L001S, U10-ch118, adc2

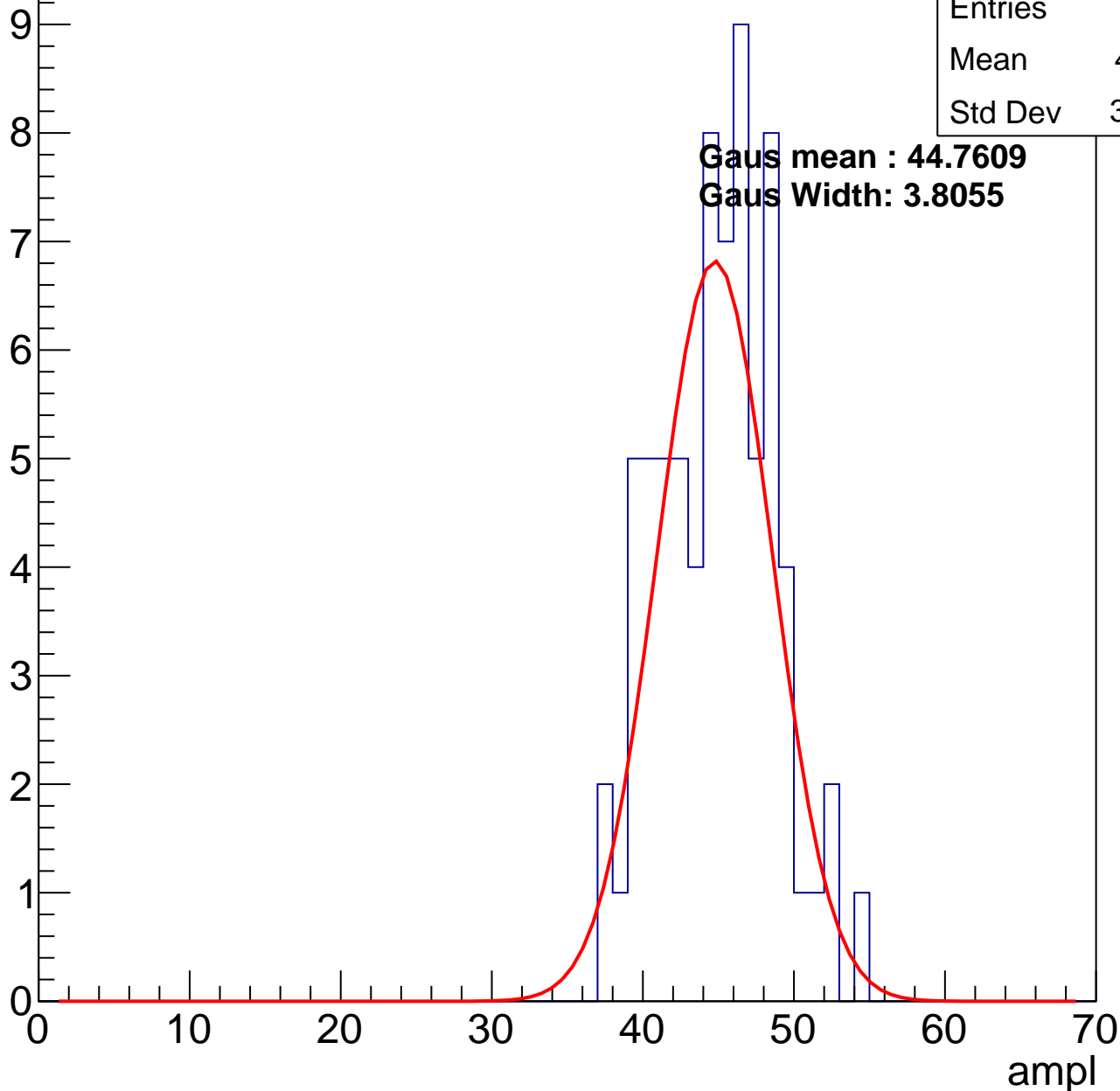
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	44.51
Std Dev	3.735

**Gaus mean : 44.7609**

**Gaus Width: 3.8055**

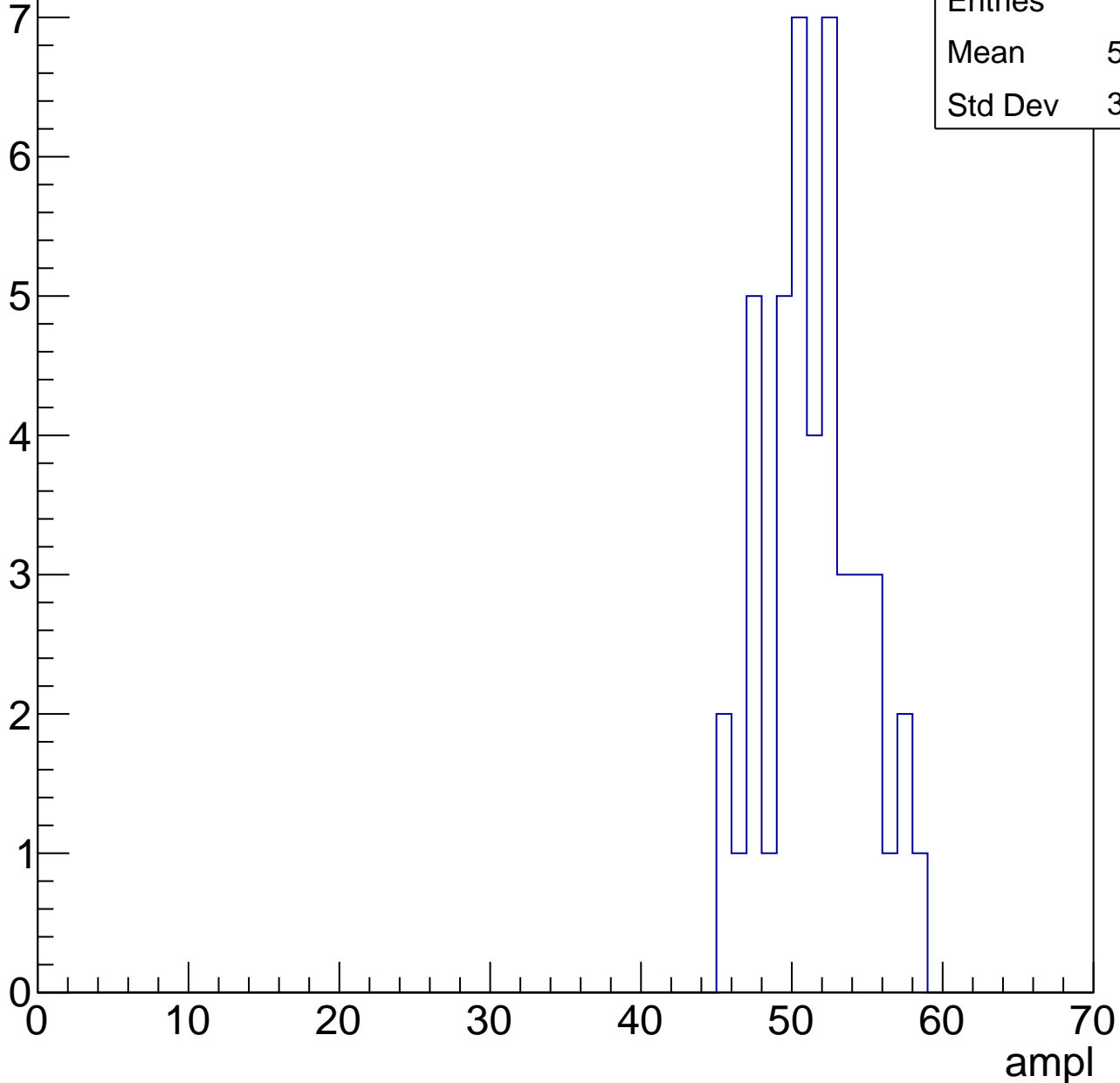


# B0L001S, U10-ch118, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	45
Mean	51.02
Std Dev	3.173

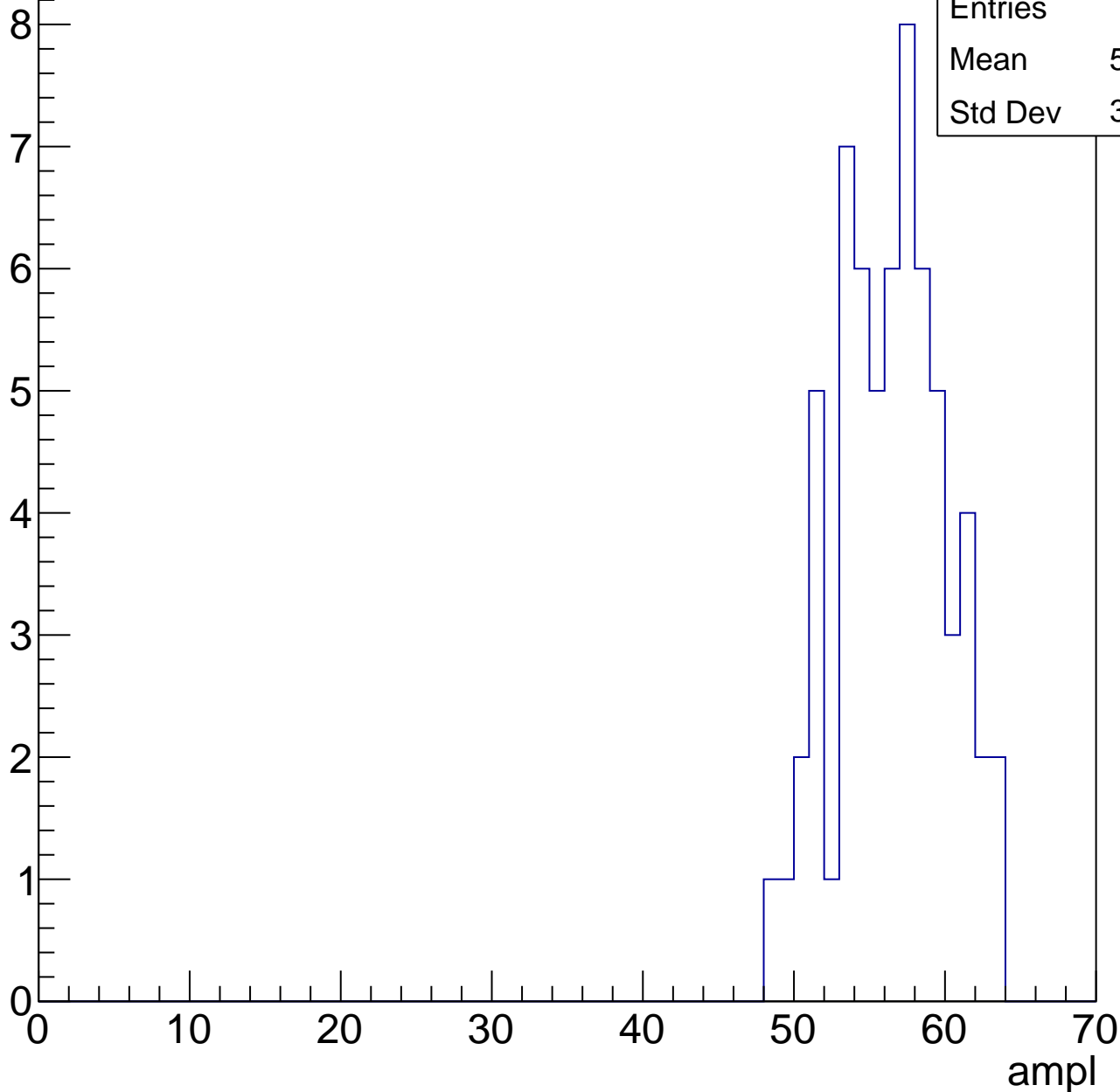


# B0L001S, U10-ch118, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

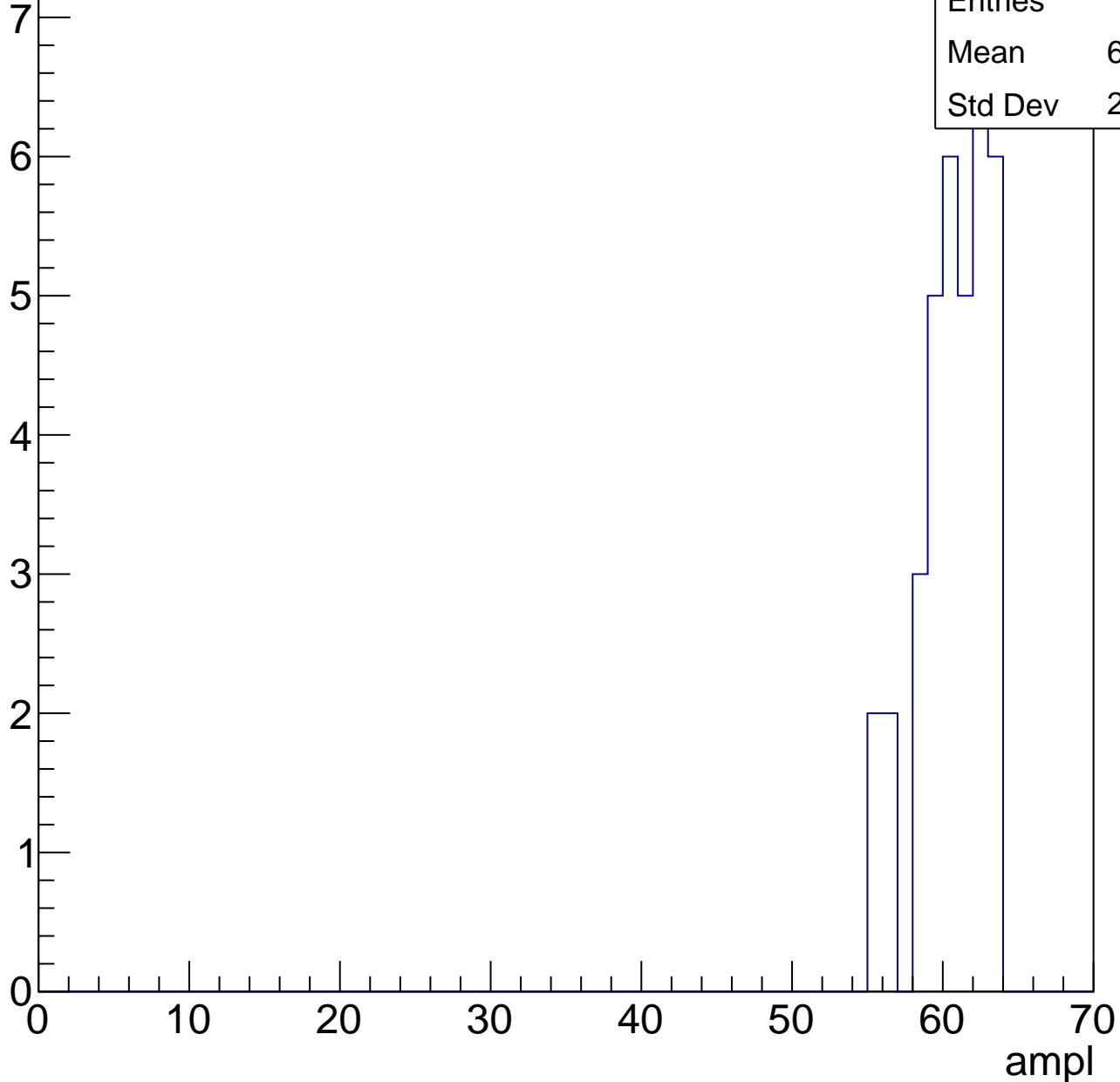
Entries	64
Mean	55.98
Std Dev	3.564



# B0L001S, U10-ch118, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U10-ch118, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

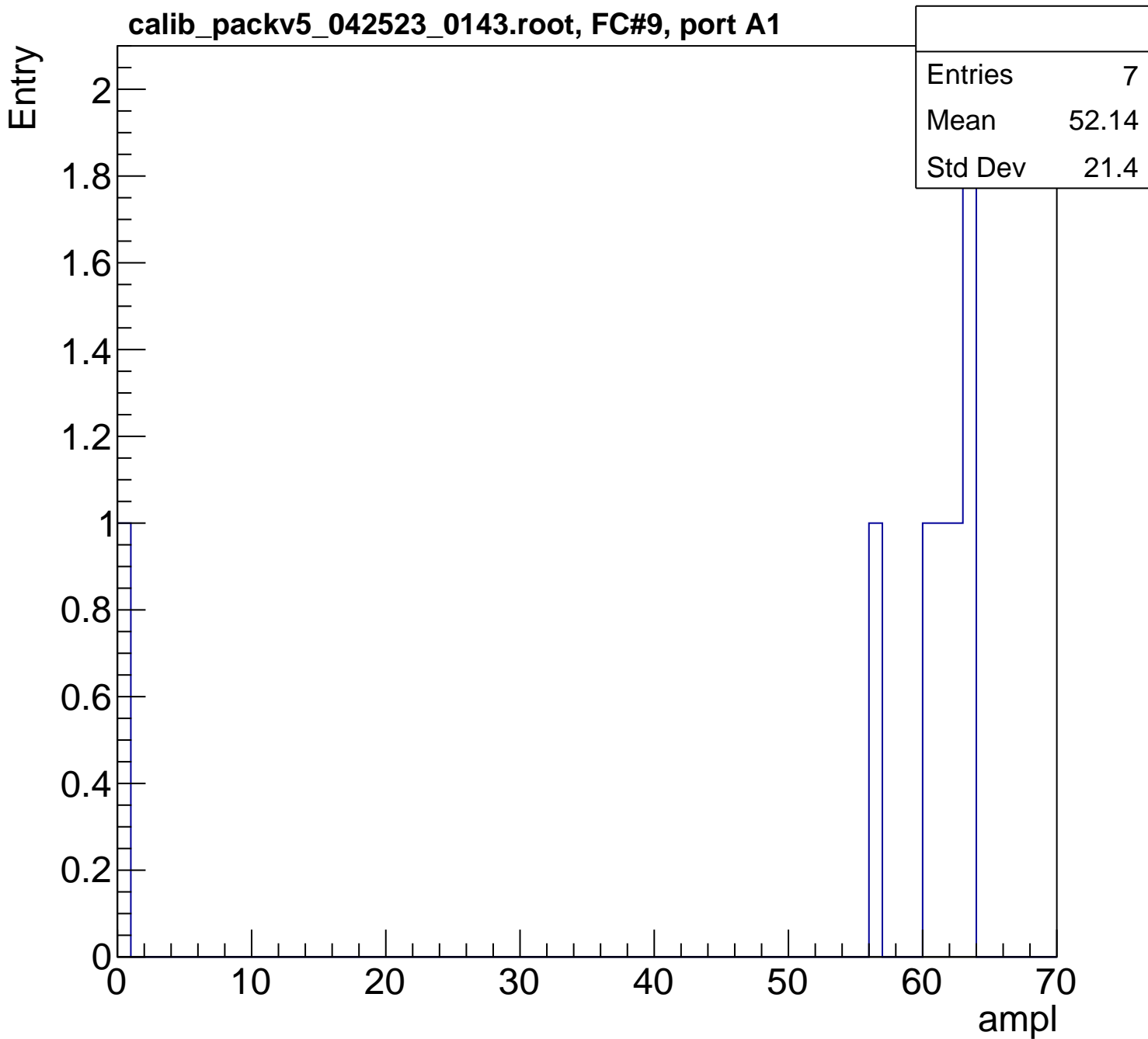
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	7
Mean	52.14
Std Dev	21.4

ampl

0 10 20 30 40 50 60 70





# B0L001S, U10-ch118, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U10-ch119, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	80
Mean	30.18
Std Dev	5.135

**Gaus mean : 30.5237**

**Gaus Width: 4.1307**

Entry

10  
8  
6  
4  
2  
0

ampl

0

10

20

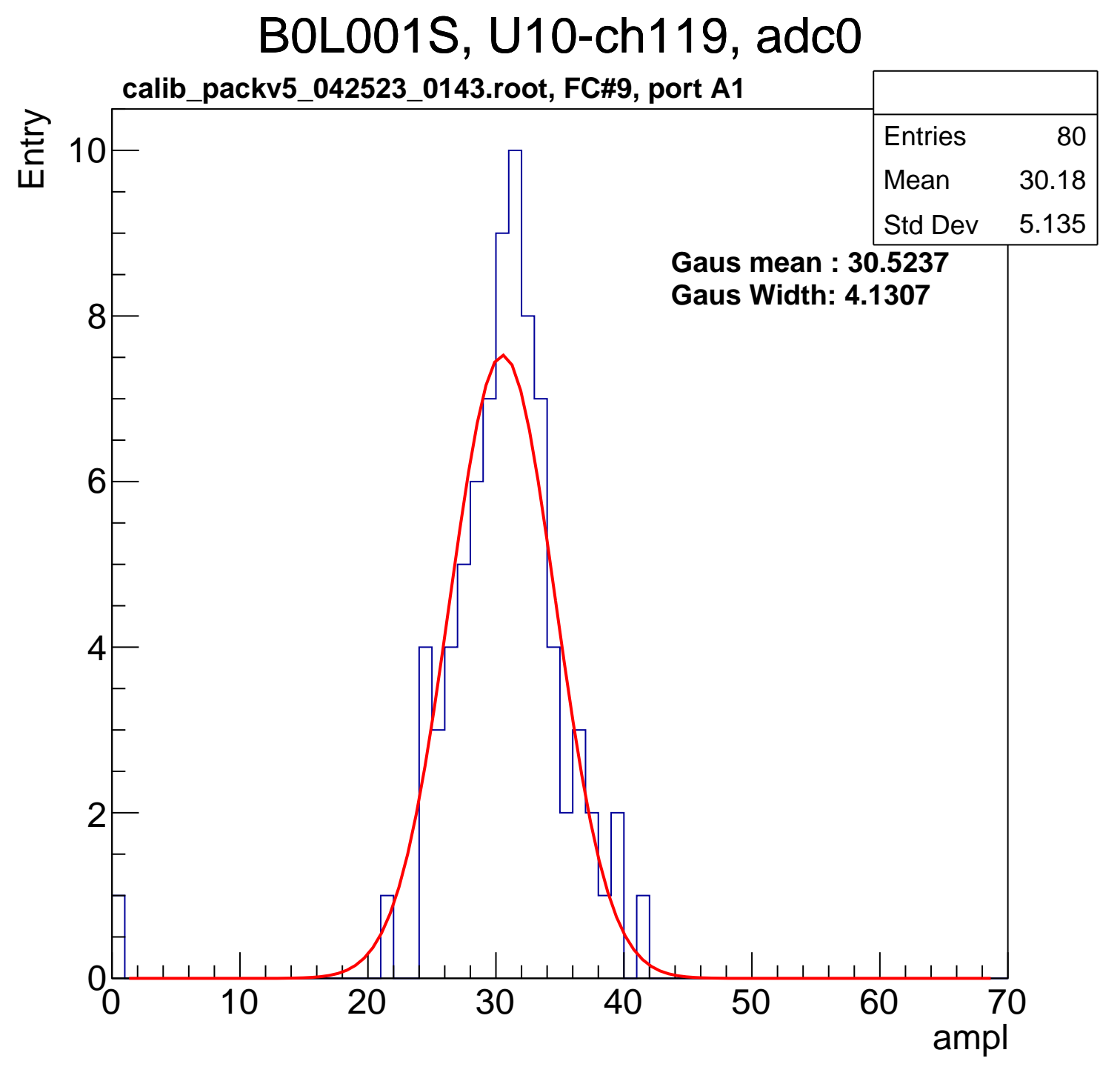
30

40

50

60

70



# B0L001S, U10-ch119, adc1

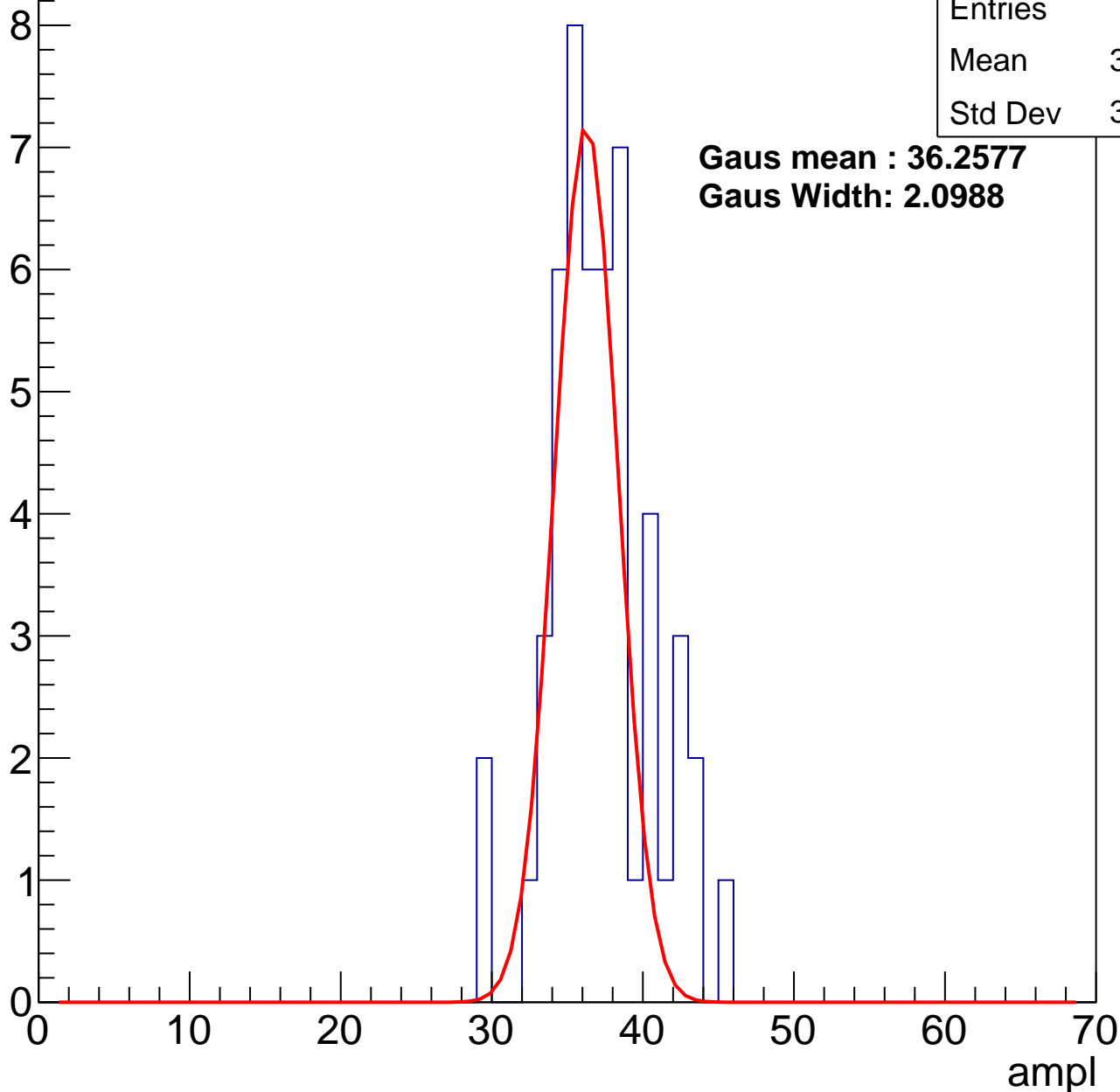
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	51
Mean	36.75
Std Dev	3.325

**Gaus mean : 36.2577**

**Gaus Width: 2.0988**



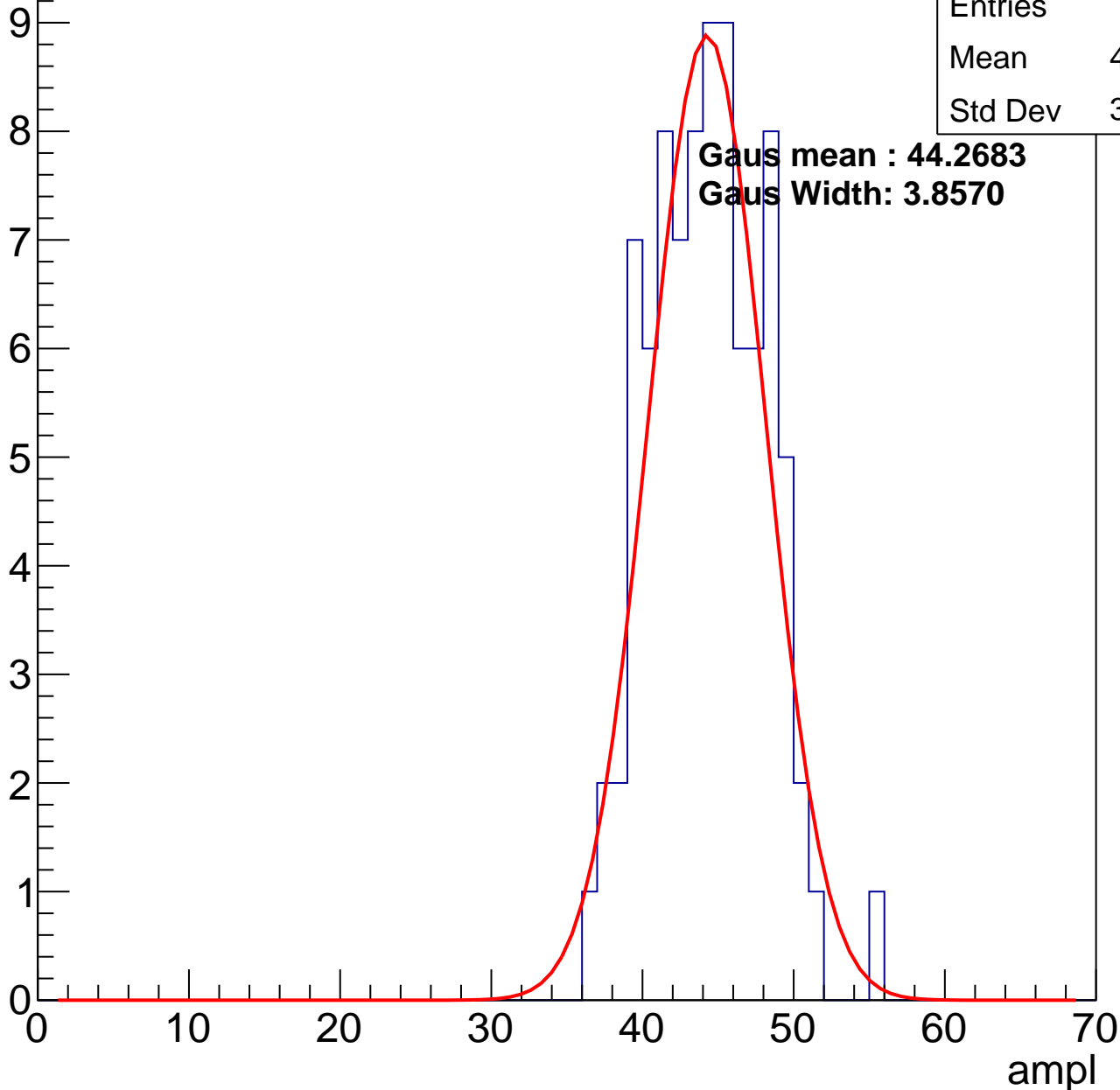
# B0L001S, U10-ch119, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	88
Mean	43.85
Std Dev	3.682

**Gaus mean : 44.2683**  
**Gaus Width: 3.8570**

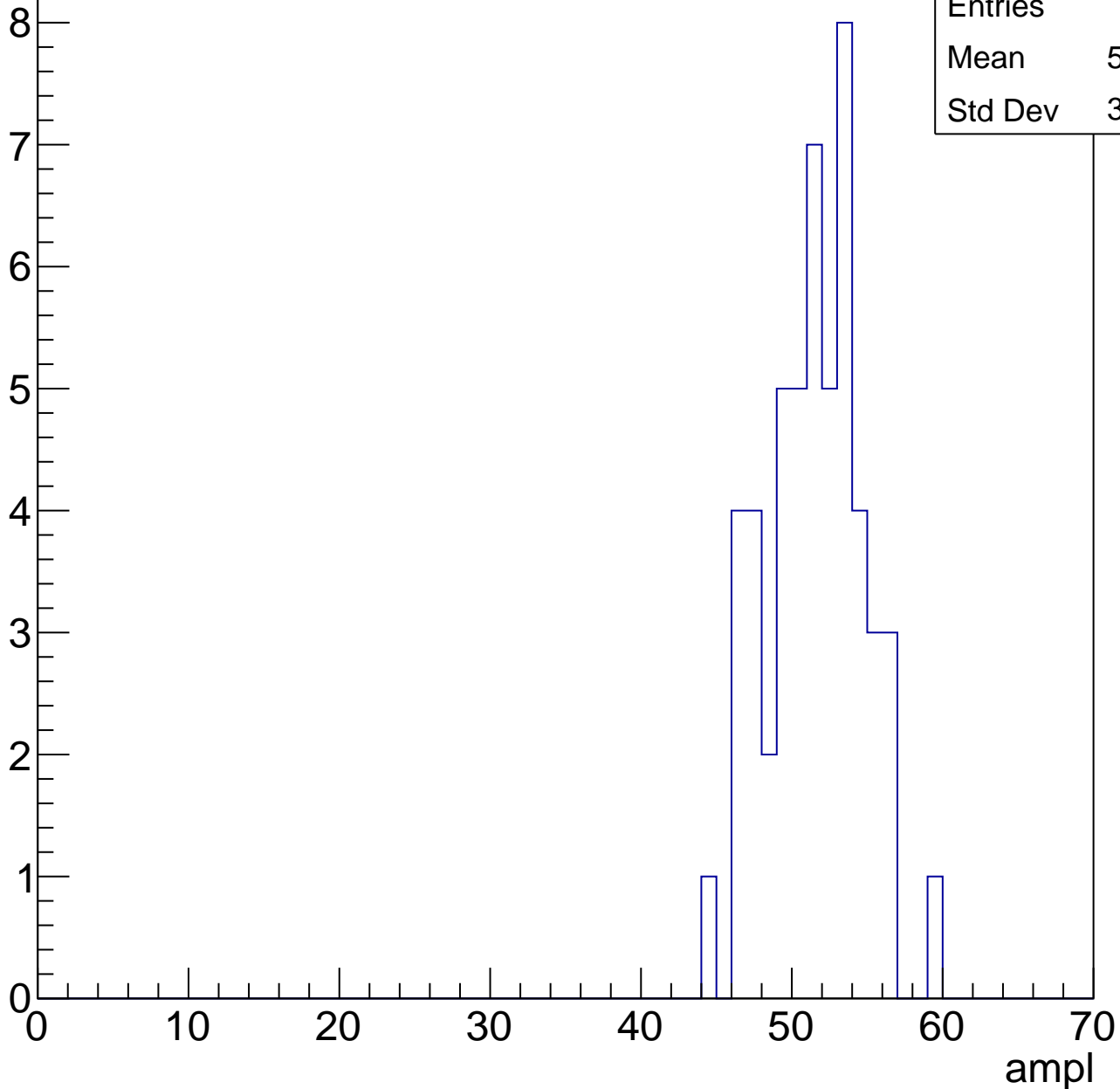


# B0L001S, U10-ch119, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	51.08
Std Dev	3.149

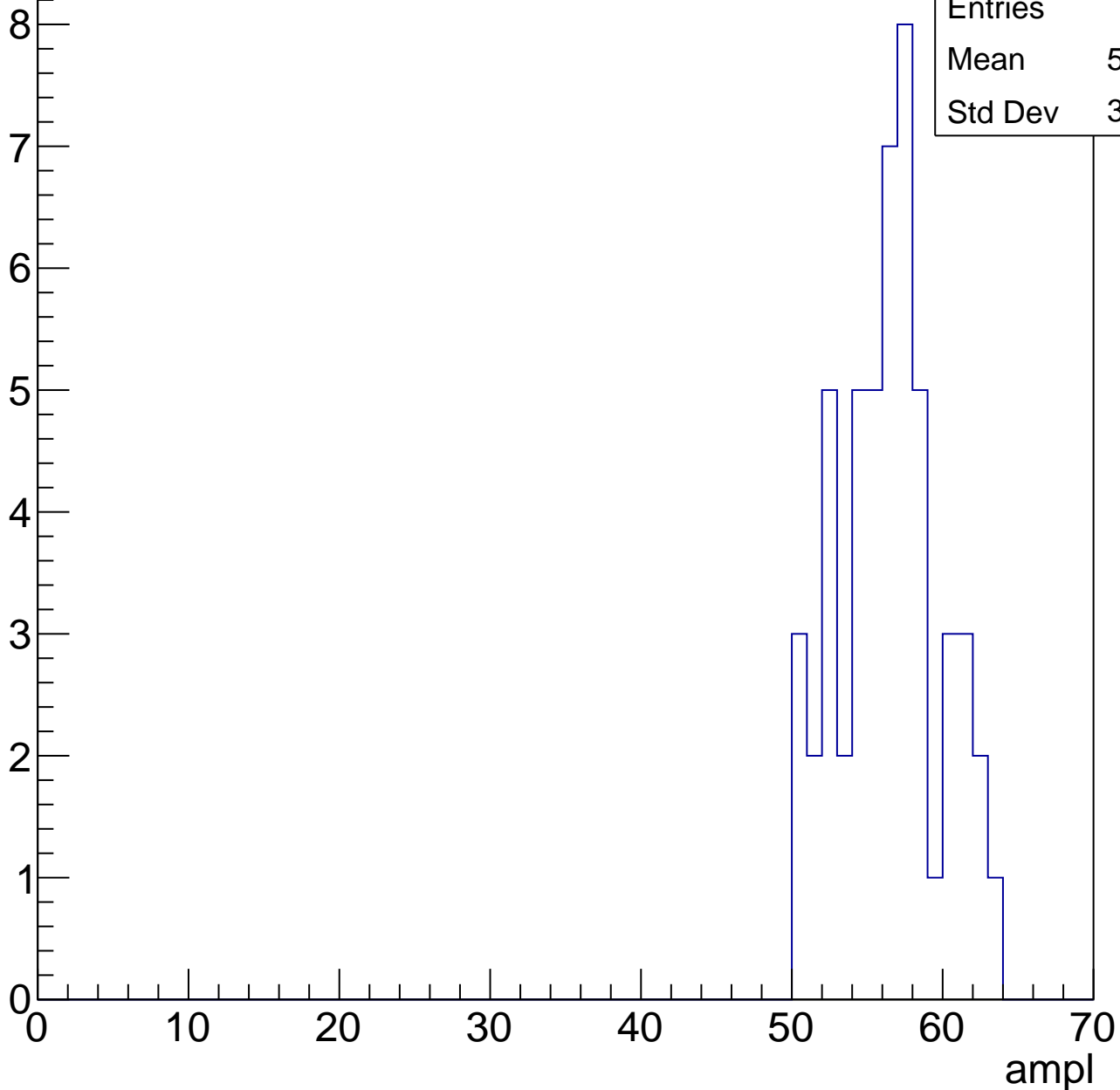


# B0L001S, U10-ch119, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

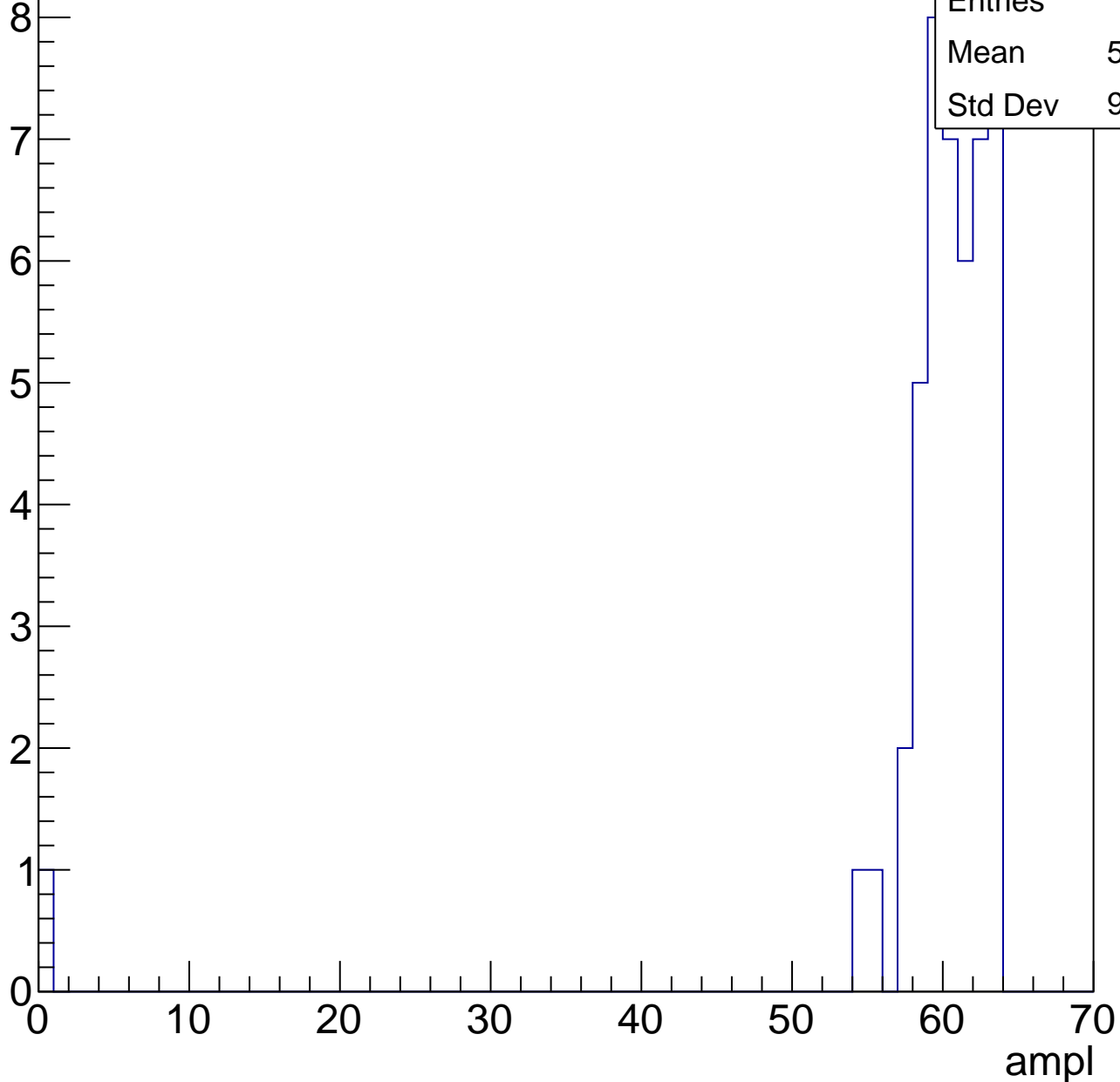
Entries	52
Mean	55.96
Std Dev	3.287



# B0L001S, U10-ch119, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U10-ch119, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch119, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U10-ch120, adc0

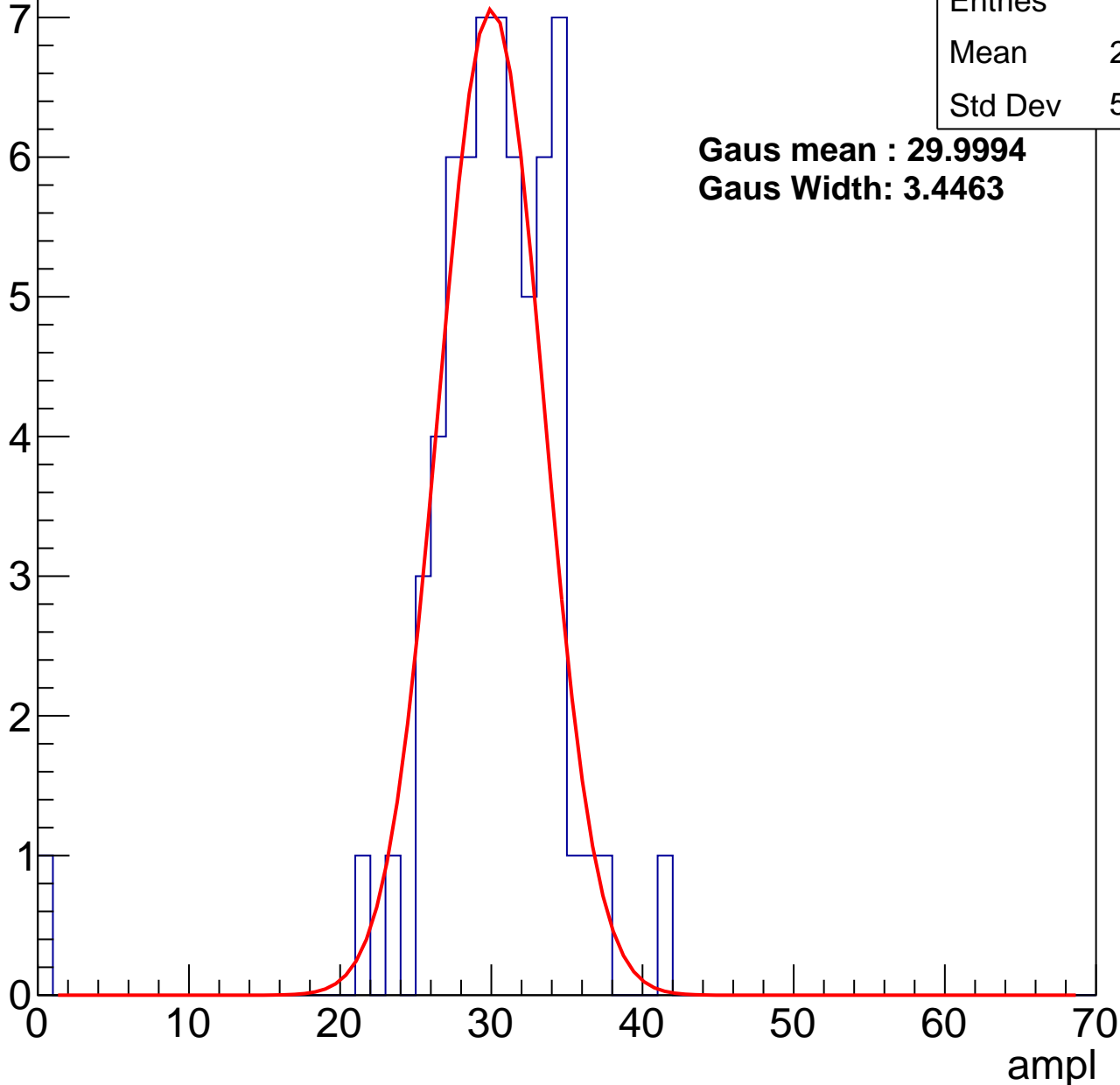
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	29.64
Std Dev	5.106

**Gaus mean : 29.9994**

**Gaus Width: 3.4463**



# B0L001S, U10-ch120, adc1

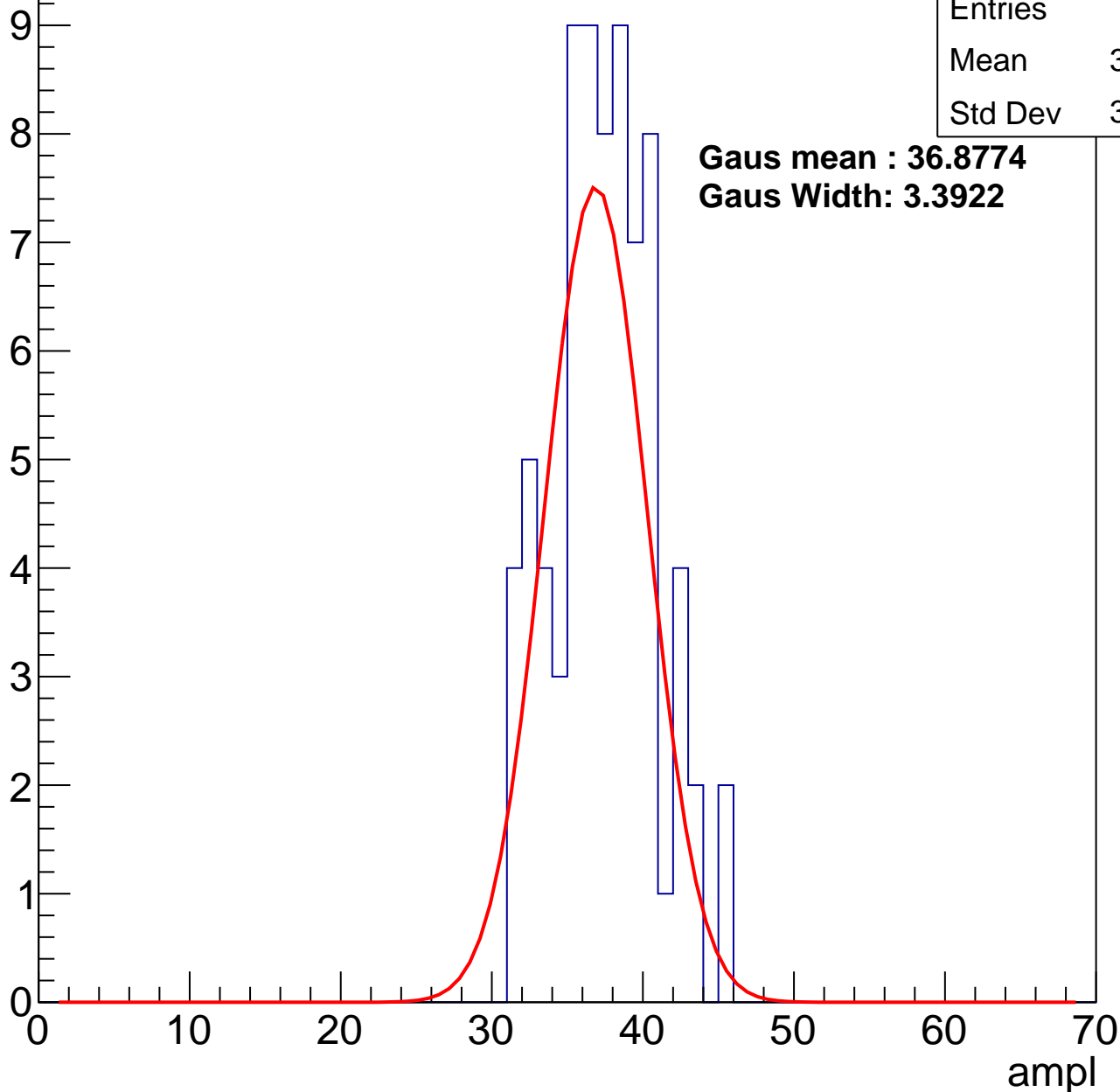
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	75
Mean	36.97
Std Dev	3.327

**Gaus mean : 36.8774**

**Gaus Width: 3.3922**



# B0L001S, U10-ch120, adc2

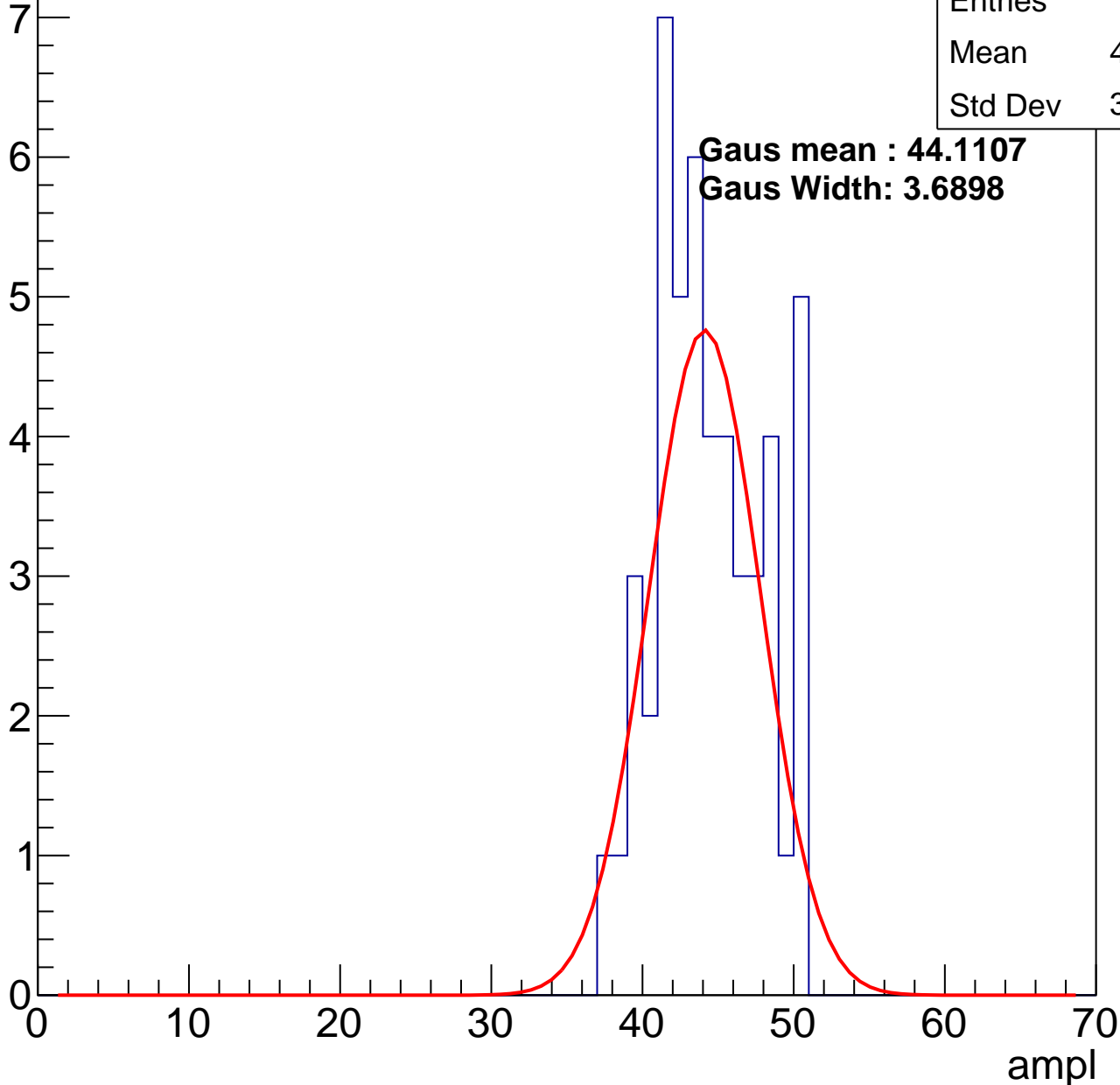
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	49
Mean	43.94
Std Dev	3.478

**Gaus mean : 44.1107**

**Gaus Width: 3.6898**



# B0L001S, U10-ch120, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

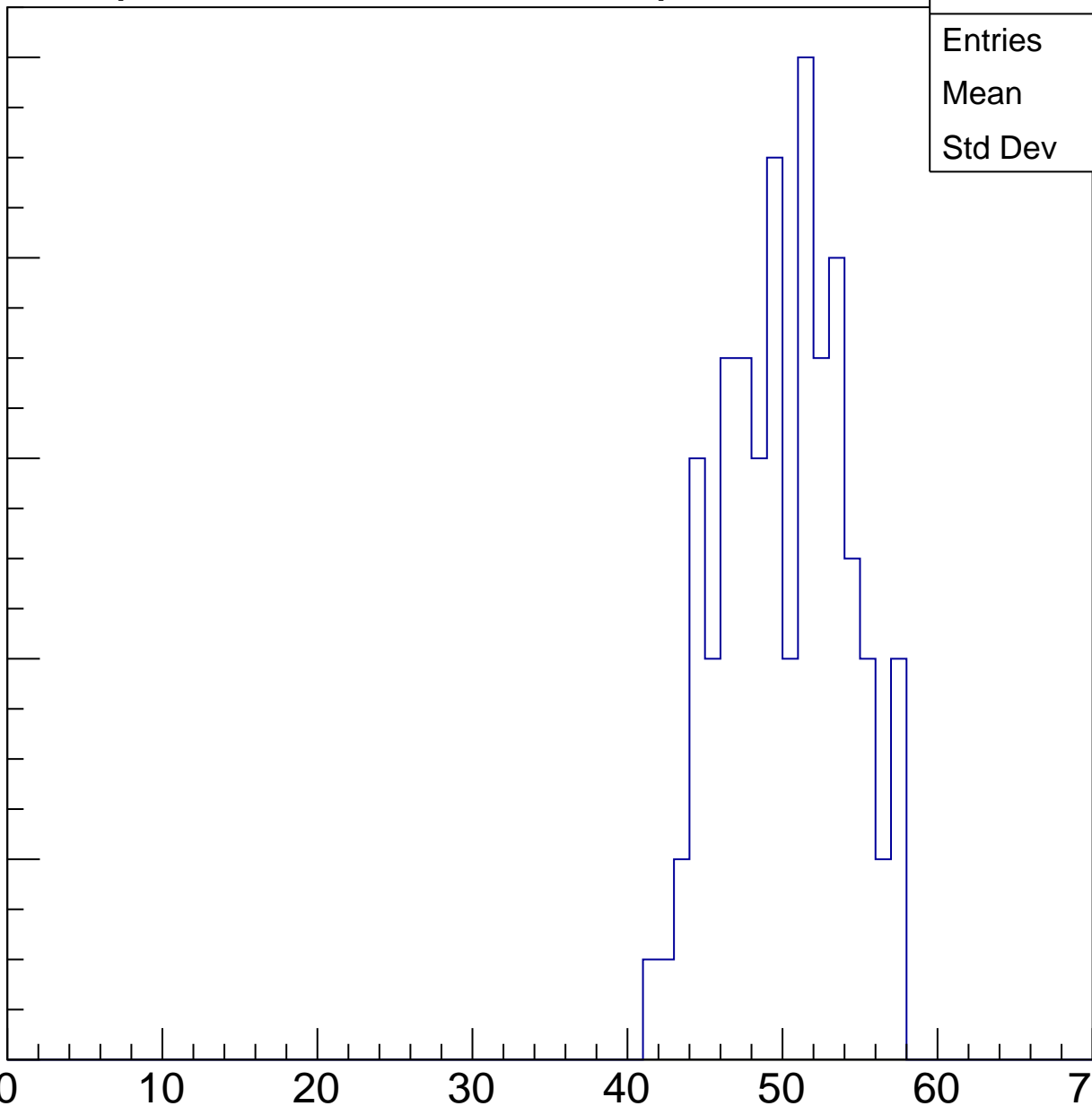
Entries	87
Mean	49.67
Std Dev	3.888

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

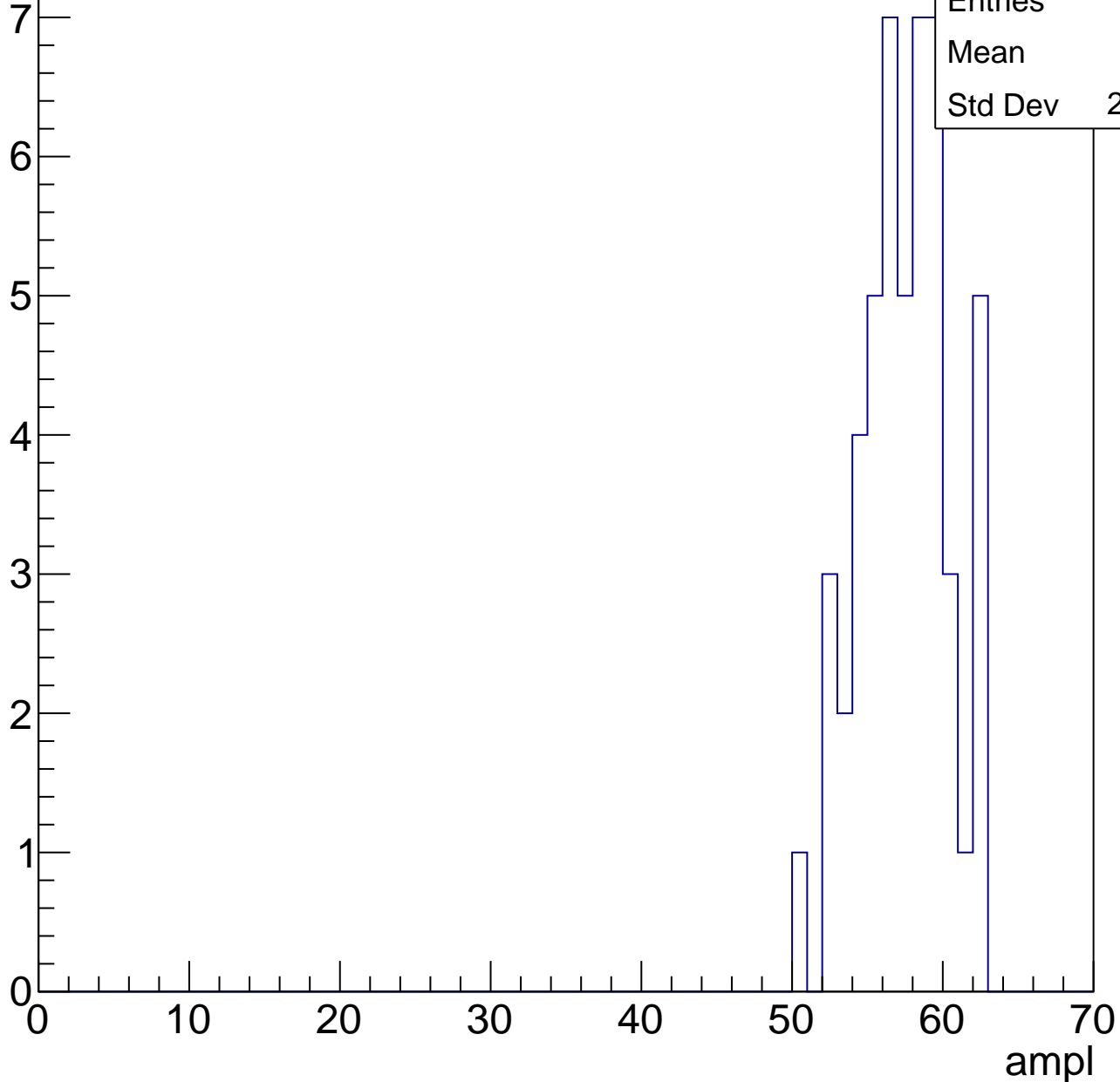
ampl



# B0L001S, U10-ch120, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

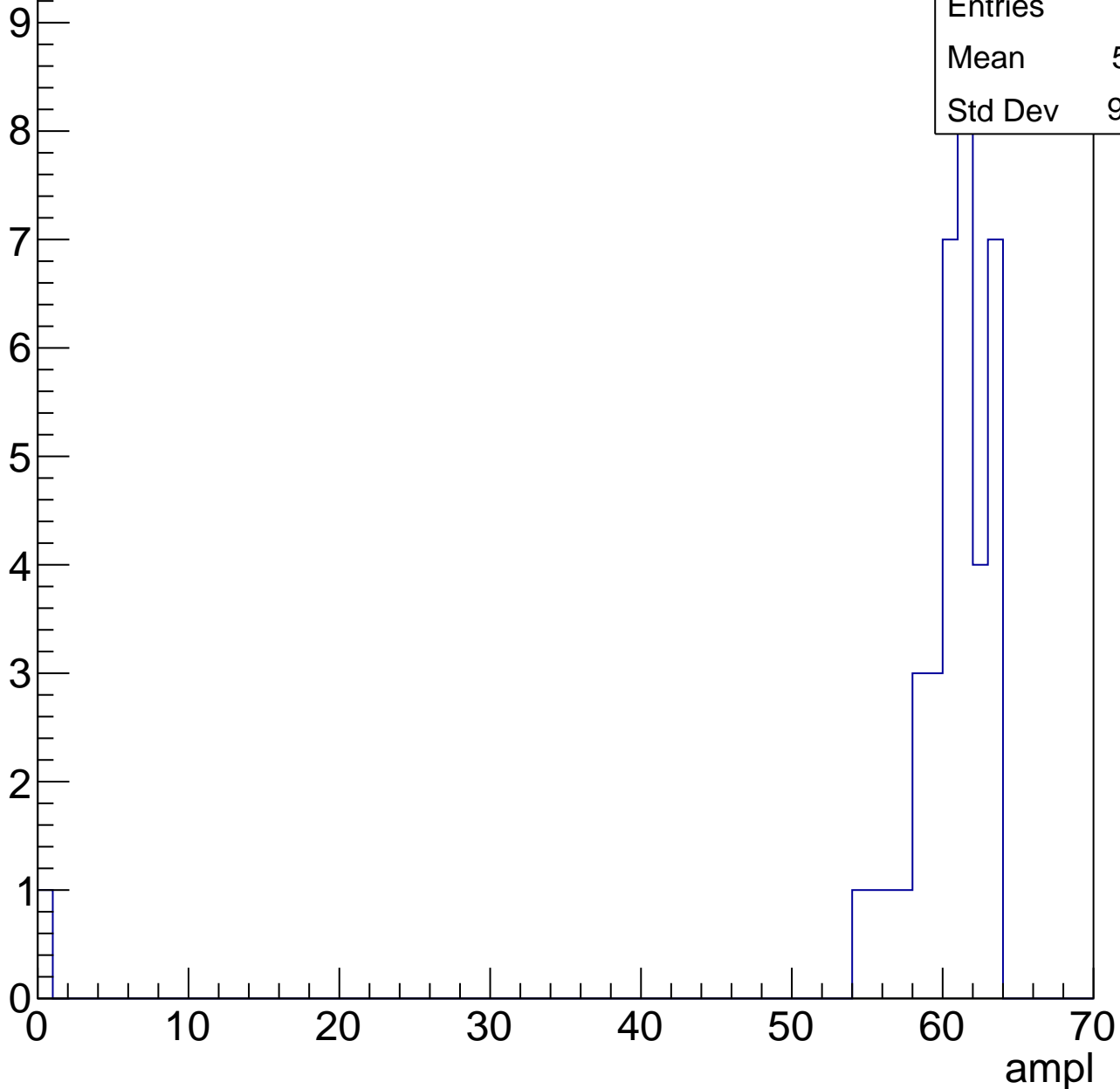


# B0L001S, U10-ch120, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	38
Mean	58.71
Std Dev	9.902



# B0L001S, U10-ch120, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch120, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U10-ch121, adc0

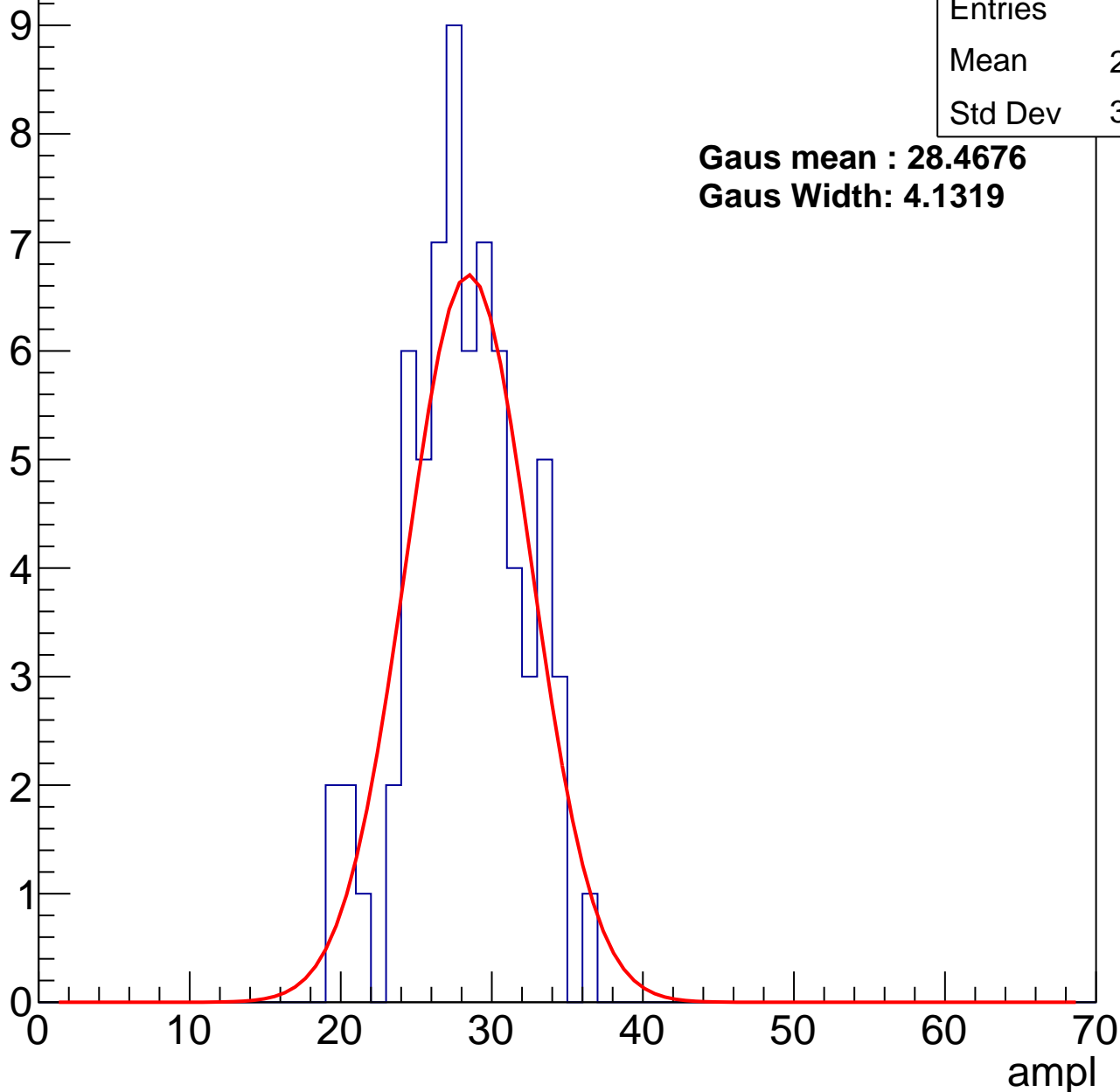
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	27.72
Std Dev	3.757

**Gaus mean : 28.4676**

**Gaus Width: 4.1319**



# B0L001S, U10-ch121, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	87
Mean	35.63
Std Dev	3.579

**Gaus mean : 36.0166**

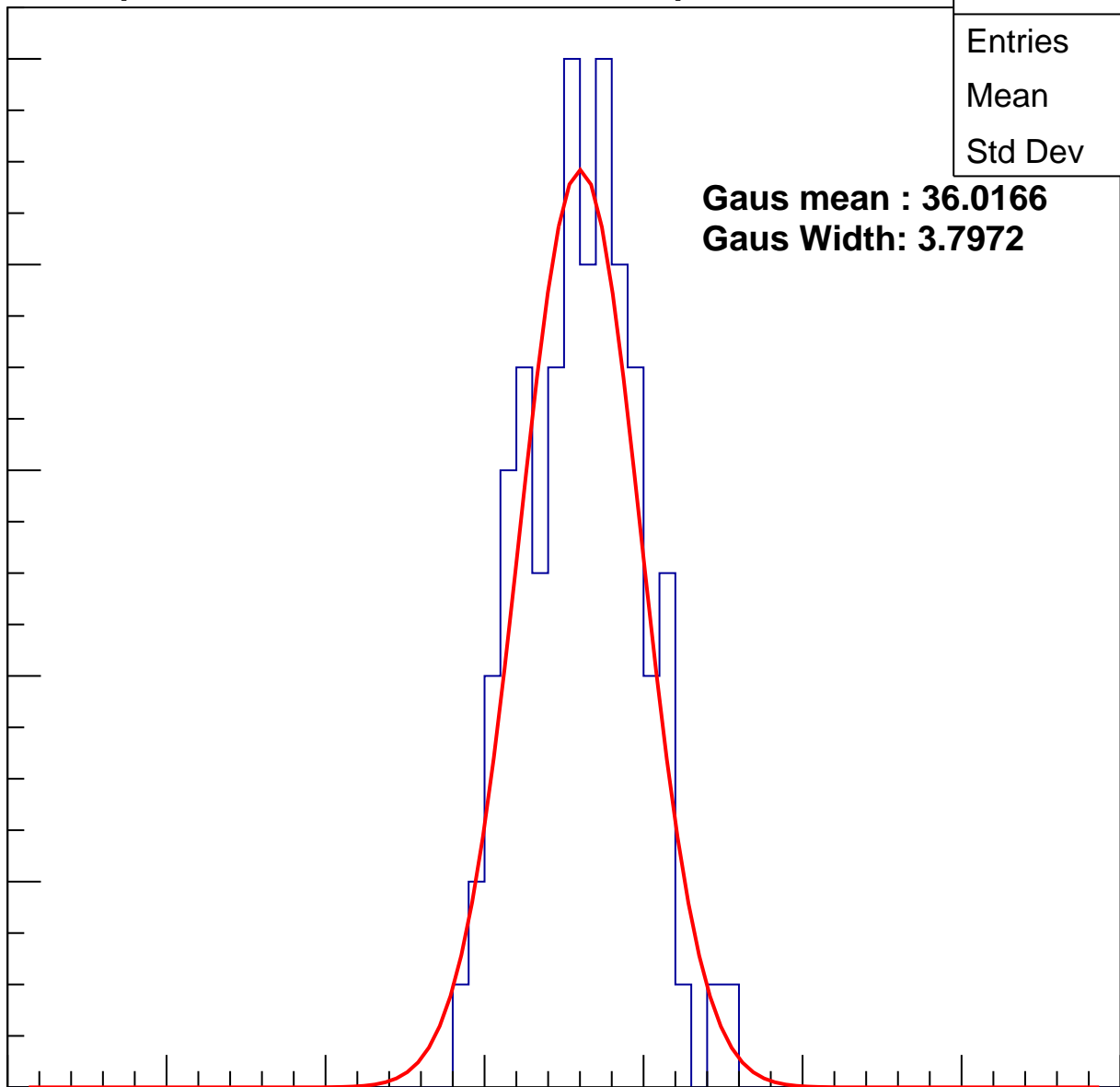
**Gaus Width: 3.7972**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U10-ch121, adc2

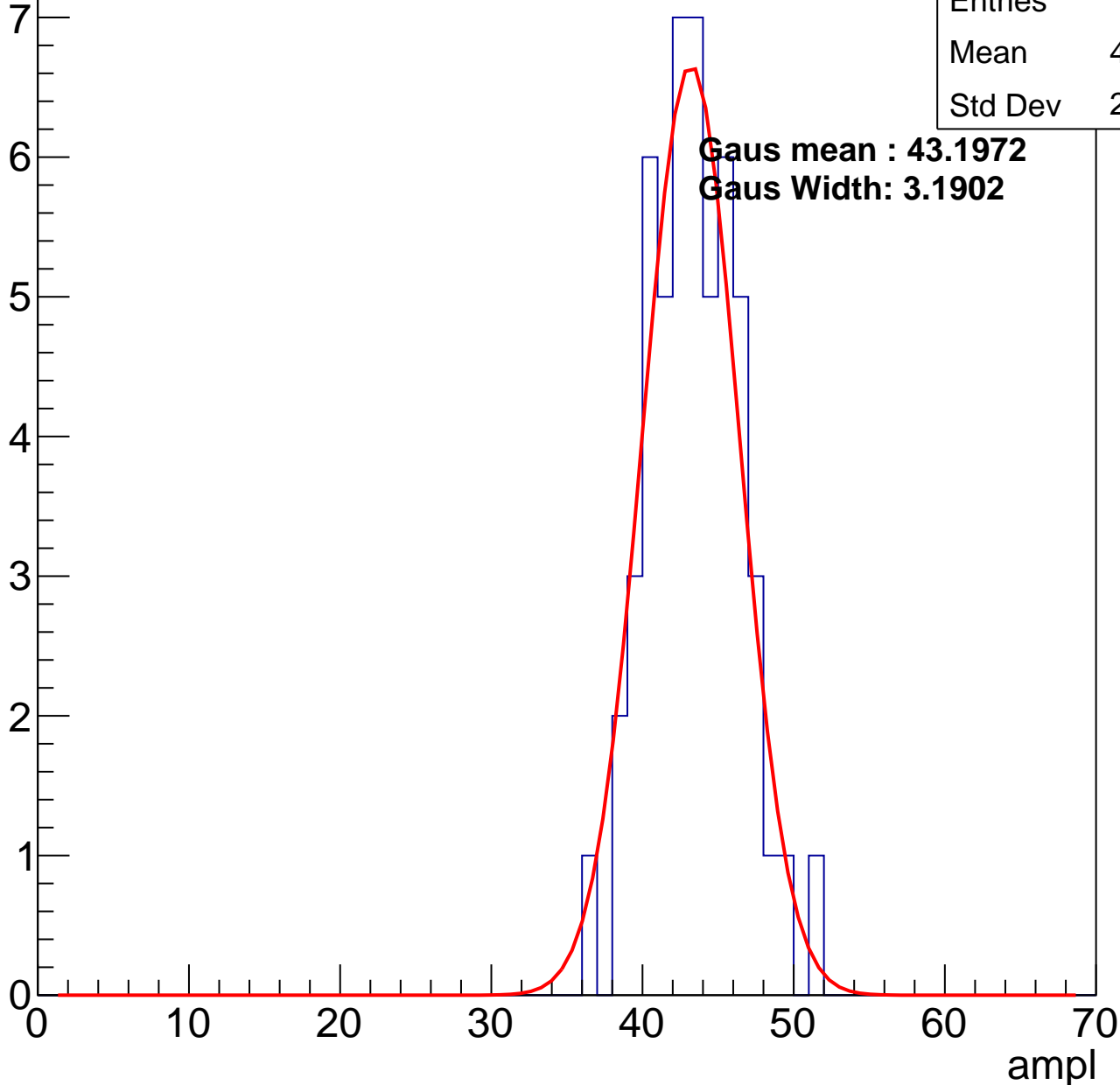
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	42.98
Std Dev	2.994

**Gaus mean : 43.1972**

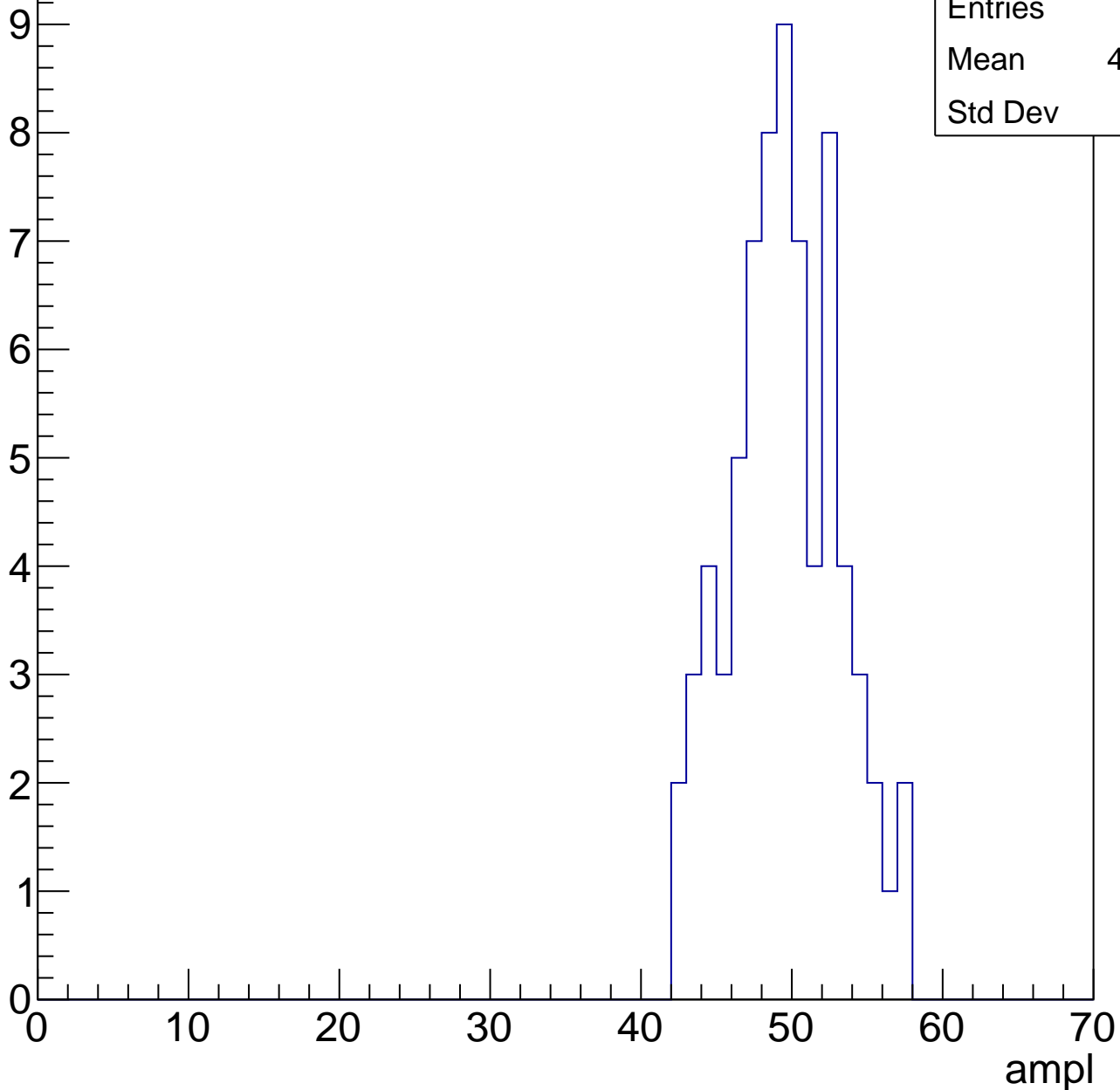
**Gaus Width: 3.1902**



# B0L001S, U10-ch121, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



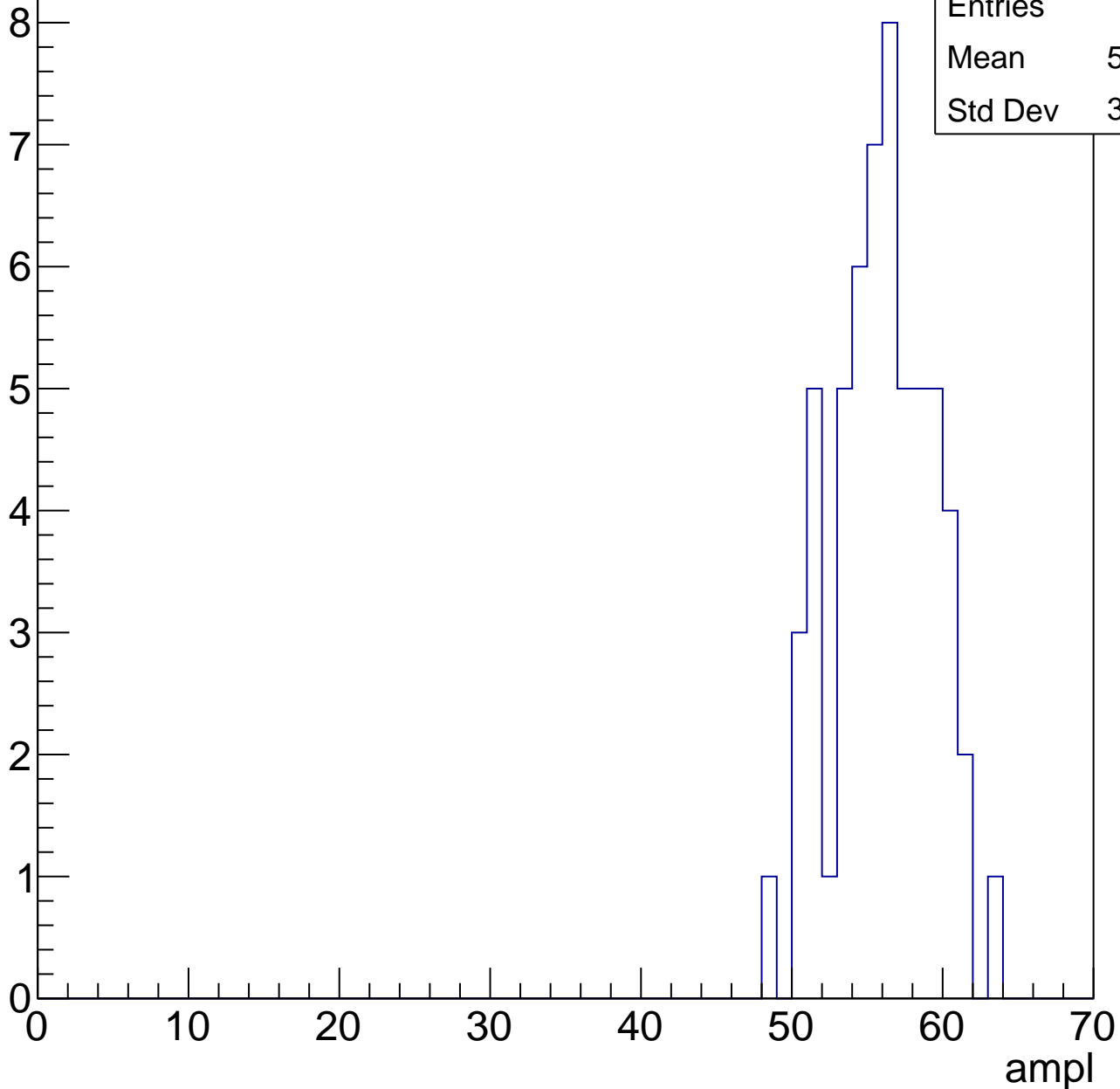
Entries	72
Mean	49.06
Std Dev	3.57

# B0L001S, U10-ch121, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	55.55
Std Dev	3.244

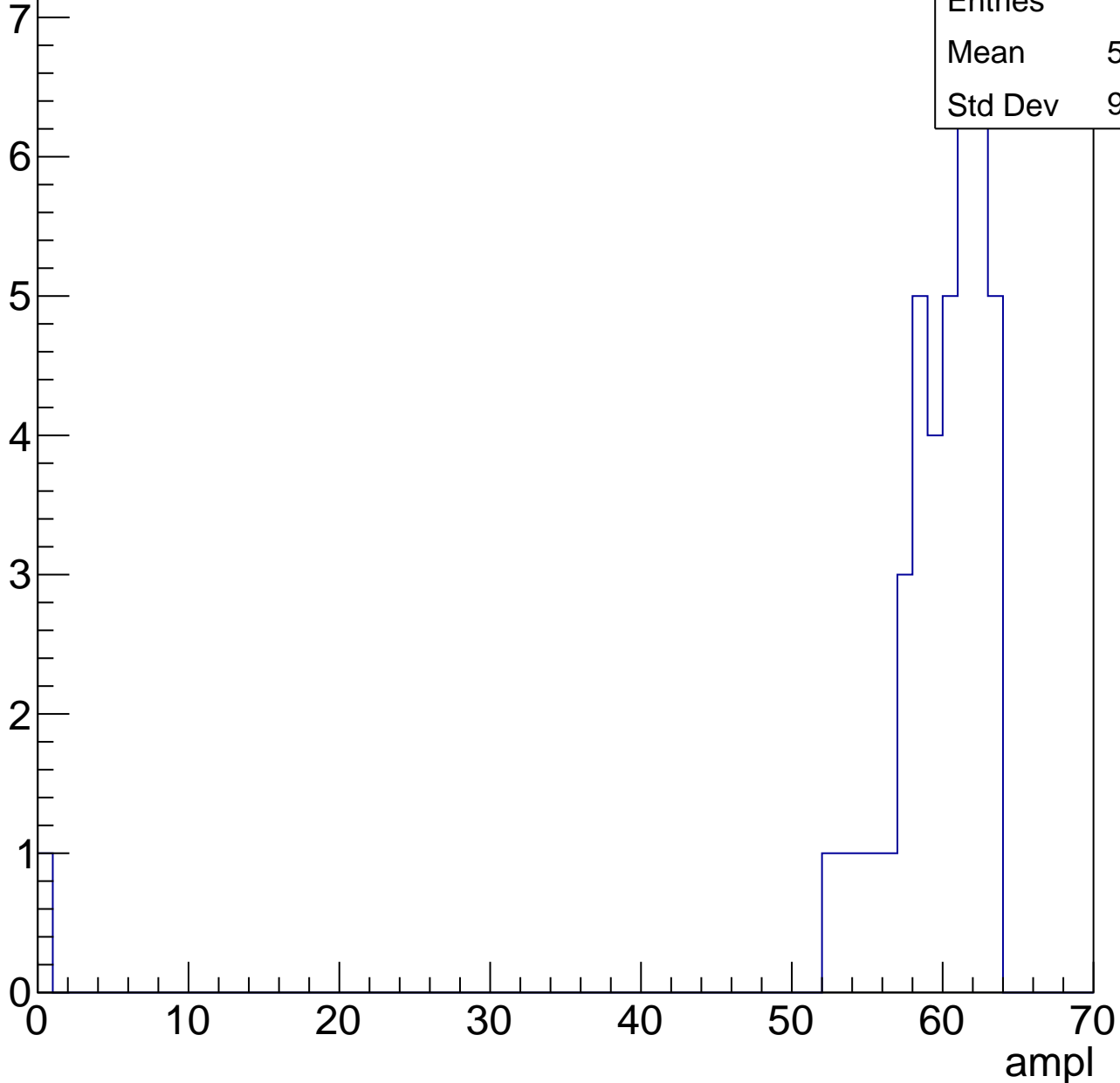


# B0L001S, U10-ch121, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

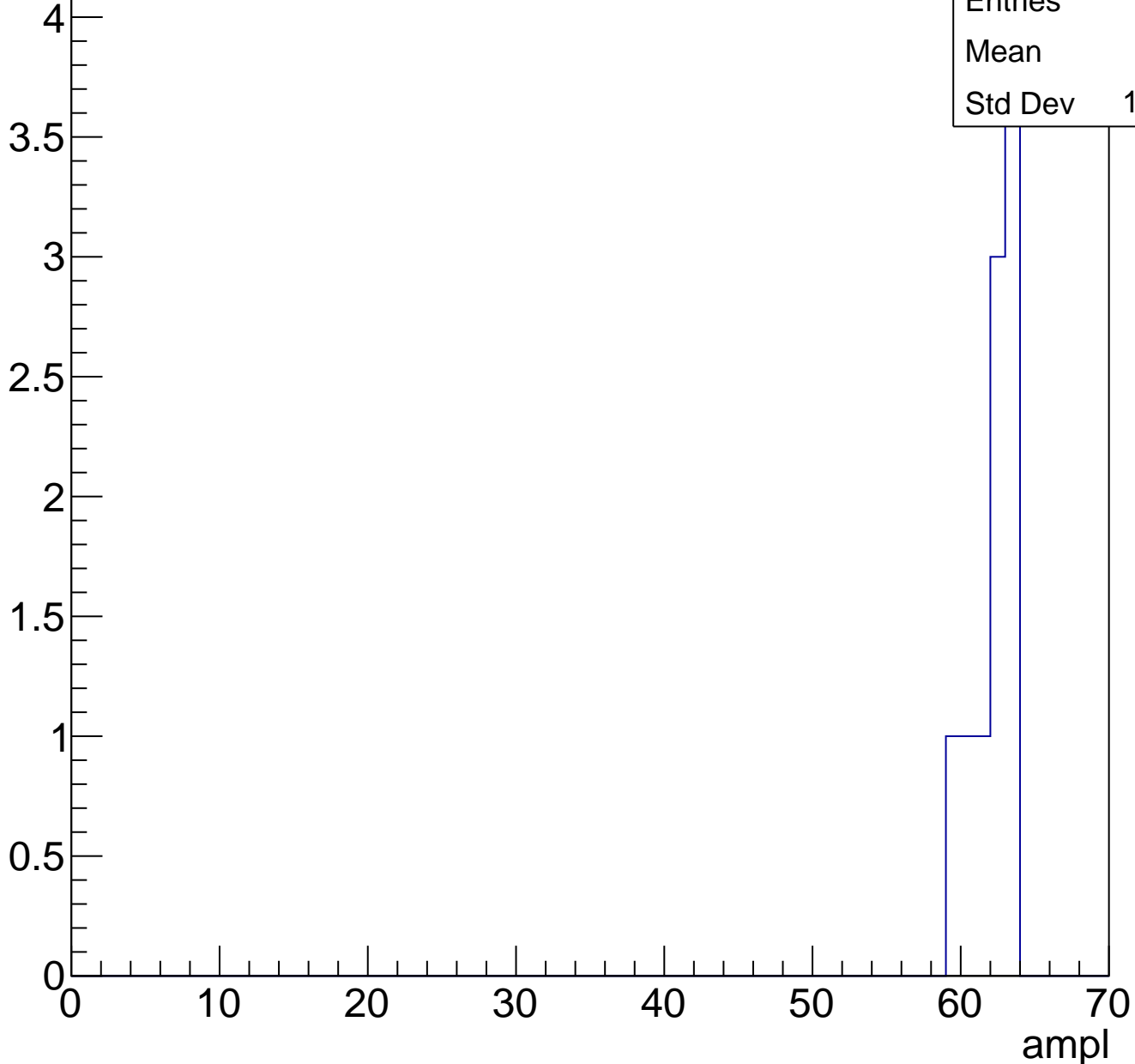
Entries	42
Mean	58.17
Std Dev	9.487



# B0L001S, U10-ch121, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	10
Mean	61.8
Std Dev	1.327



# B0L001S, U10-ch121, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U10-ch122, adc0

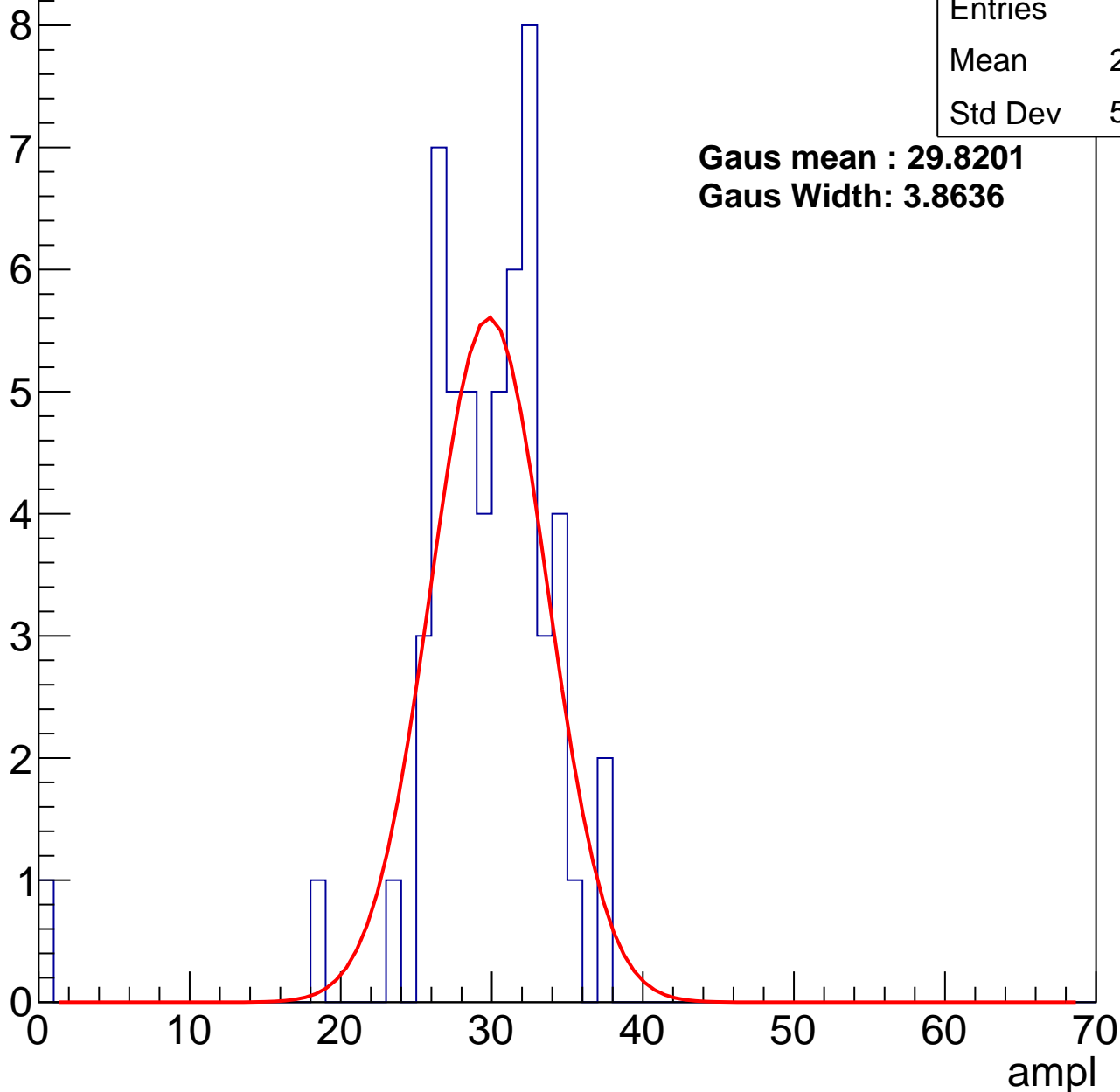
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	29.02
Std Dev	5.256

**Gaus mean : 29.8201**

**Gaus Width: 3.8636**



# B0L001S, U10-ch122, adc1

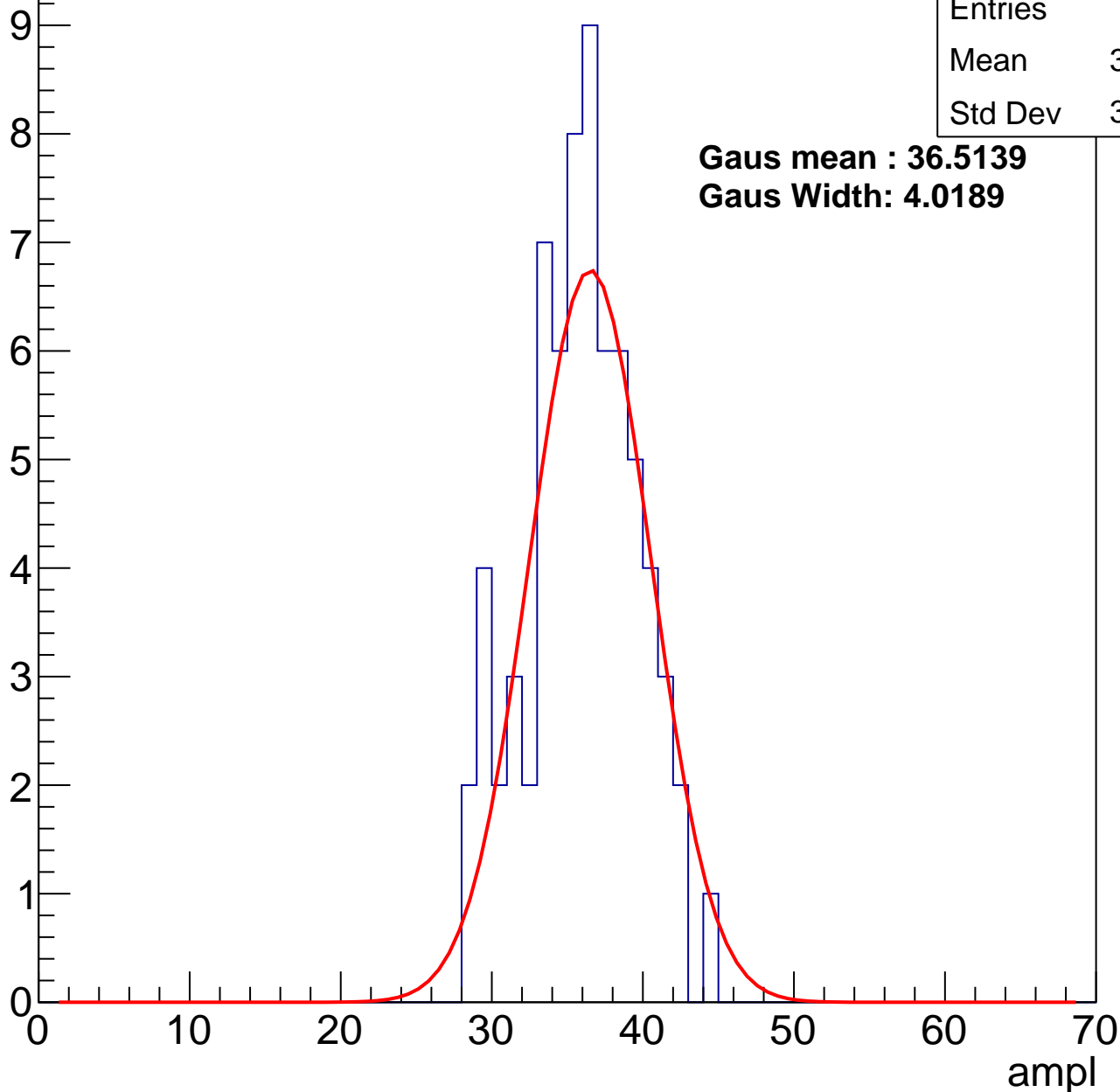
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	35.49
Std Dev	3.644

**Gaus mean : 36.5139**

**Gaus Width: 4.0189**



# B0L001S, U10-ch122, adc2

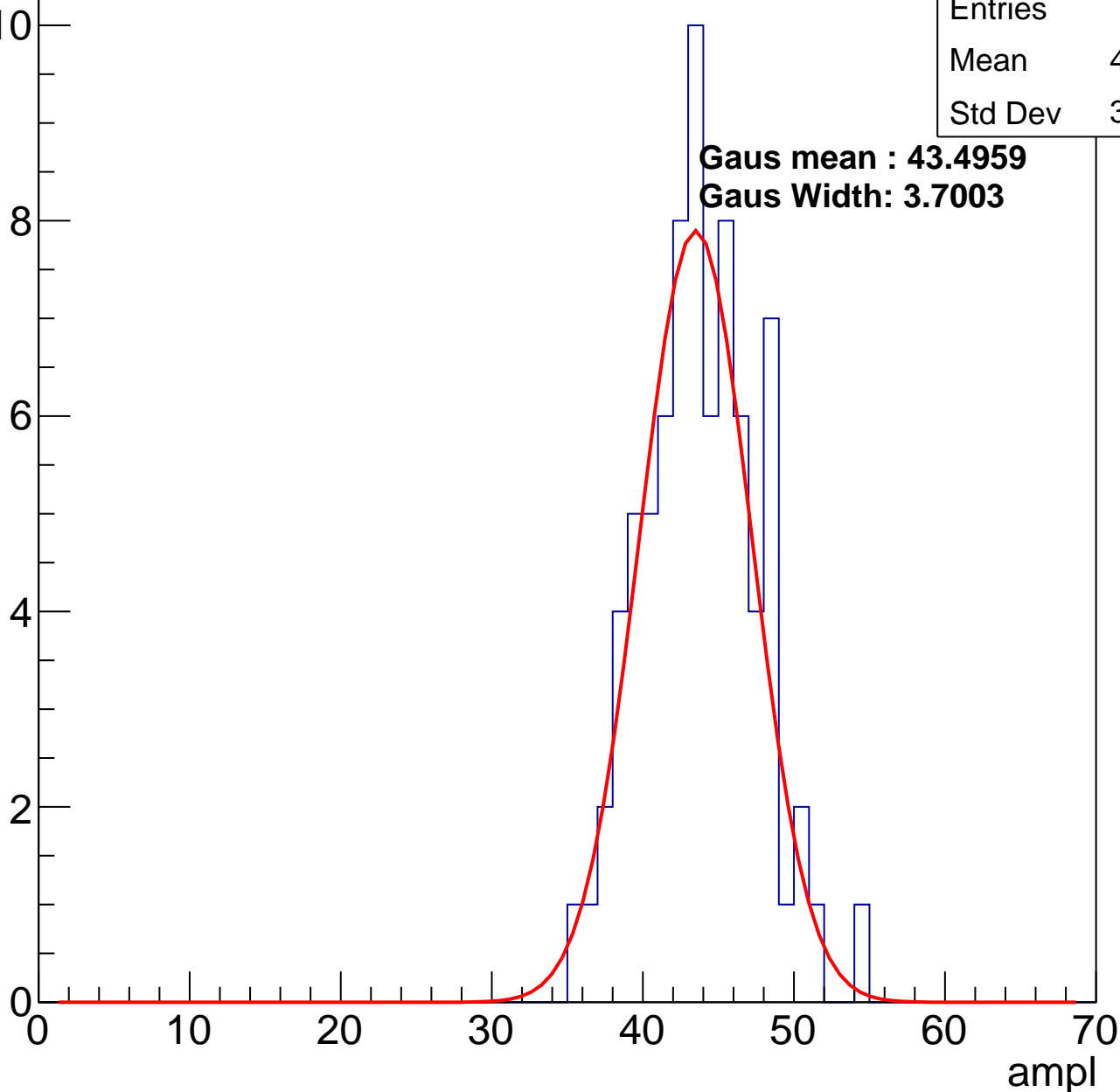
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	78
Mean	43.36
Std Dev	3.724

**Gaus mean : 43.4959**

**Gaus Width: 3.7003**

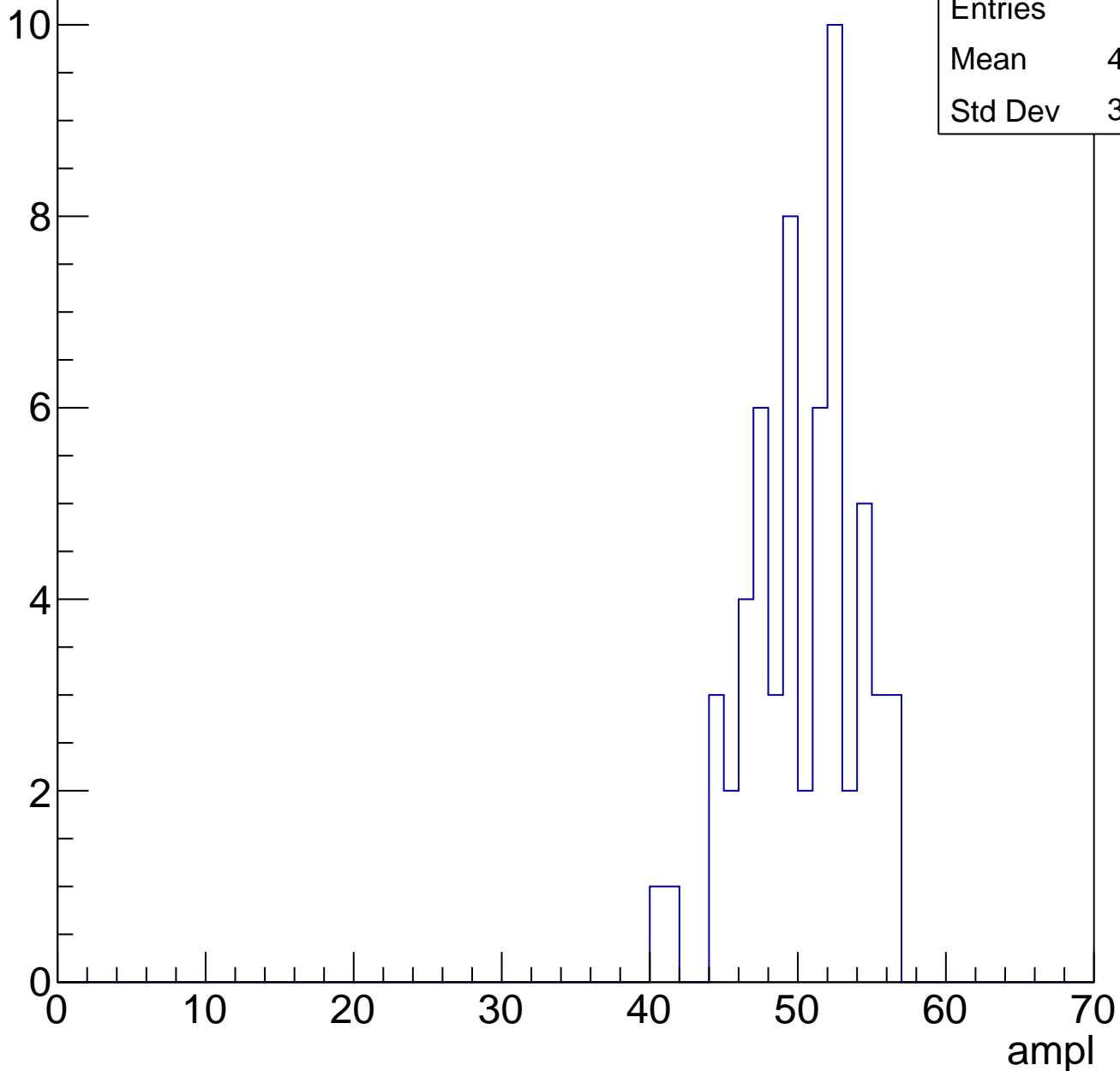


# B0L001S, U10-ch122, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	49.83
Std Dev	3.688



# B0L001S, U10-ch122, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

6

5

4

3

2

1

0

Entries	47
Mean	55.15
Std Dev	3.439

ampl

0

10

20

30

40

50

60

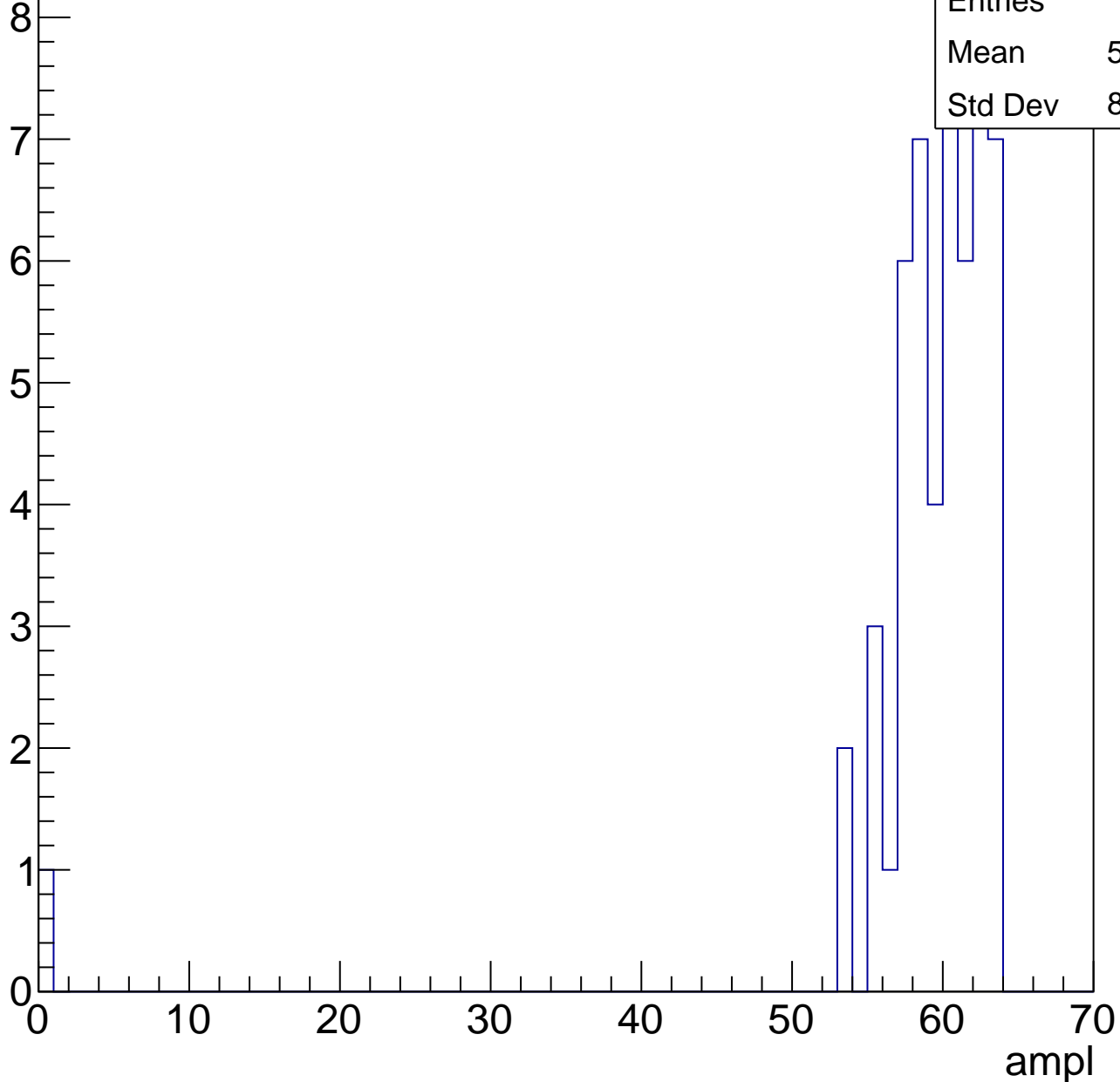
70

# B0L001S, U10-ch122, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	58.38
Std Dev	8.508



# B0L001S, U10-ch122, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch122, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L001S, U10-ch123, adc0

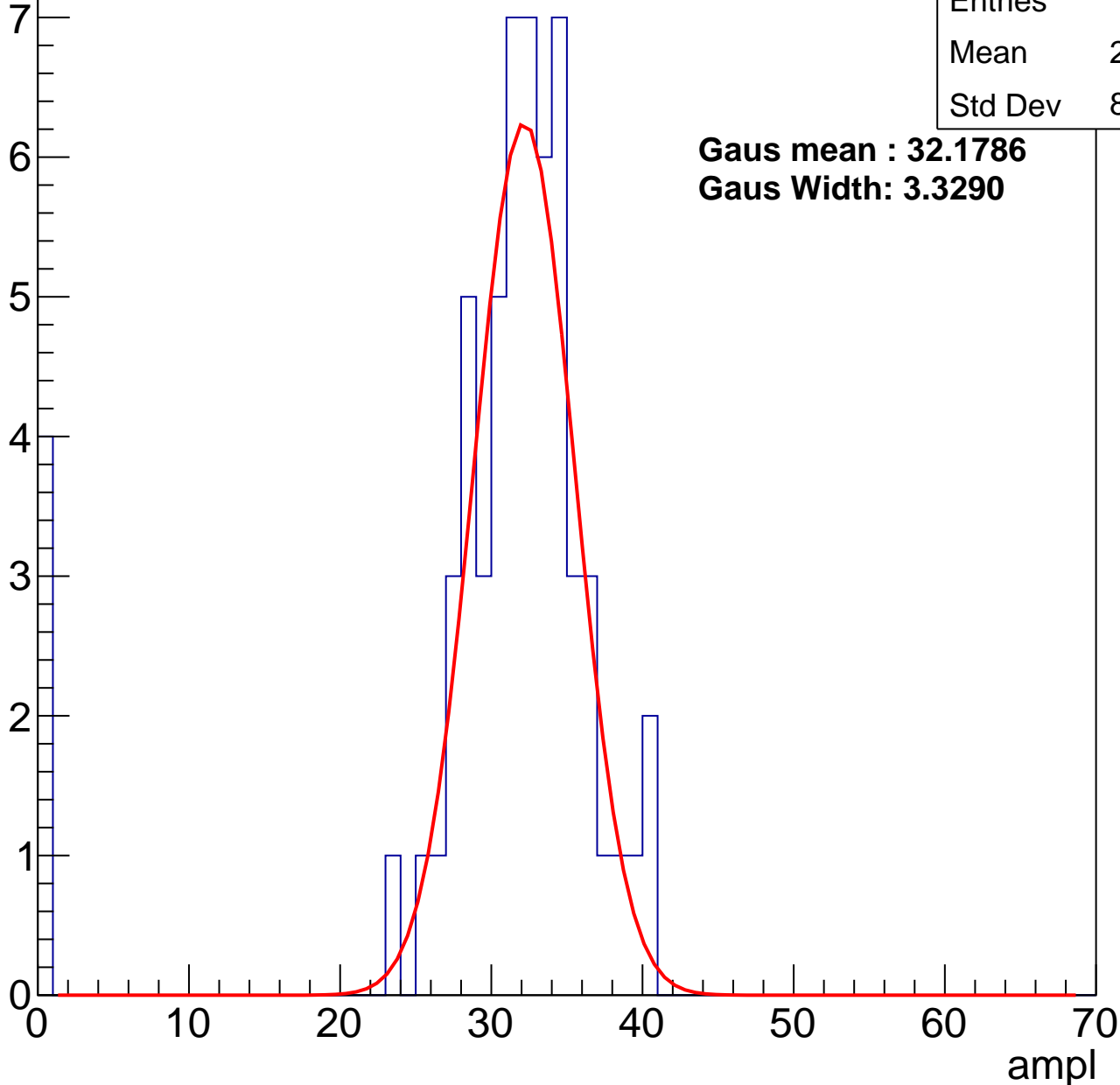
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	29.77
Std Dev	8.603

**Gaus mean : 32.1786**

**Gaus Width: 3.3290**



# B0L001S, U10-ch123, adc1

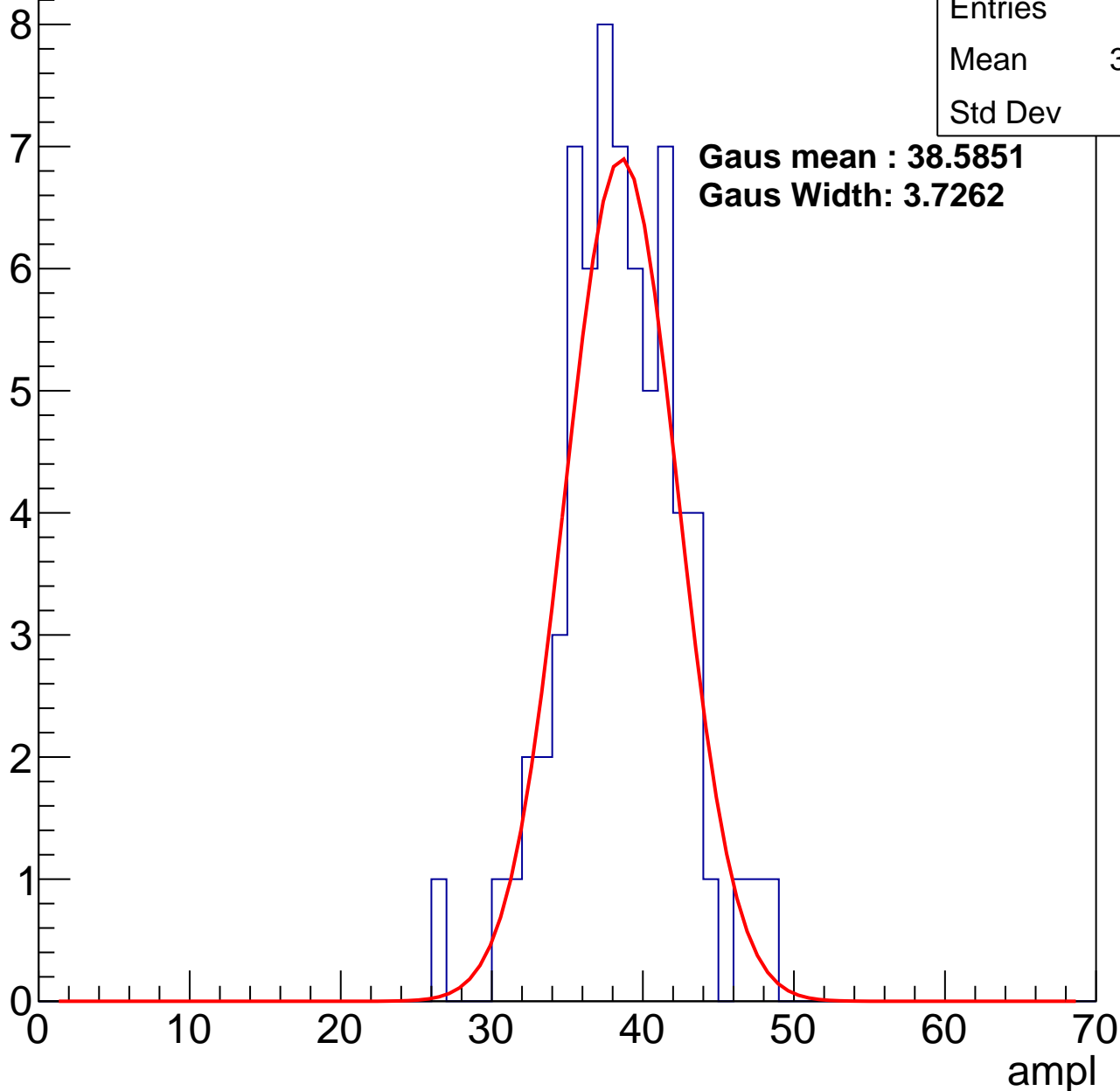
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	38.06
Std Dev	3.94

**Gaus mean : 38.5851**

**Gaus Width: 3.7262**



# B0L001S, U10-ch123, adc2

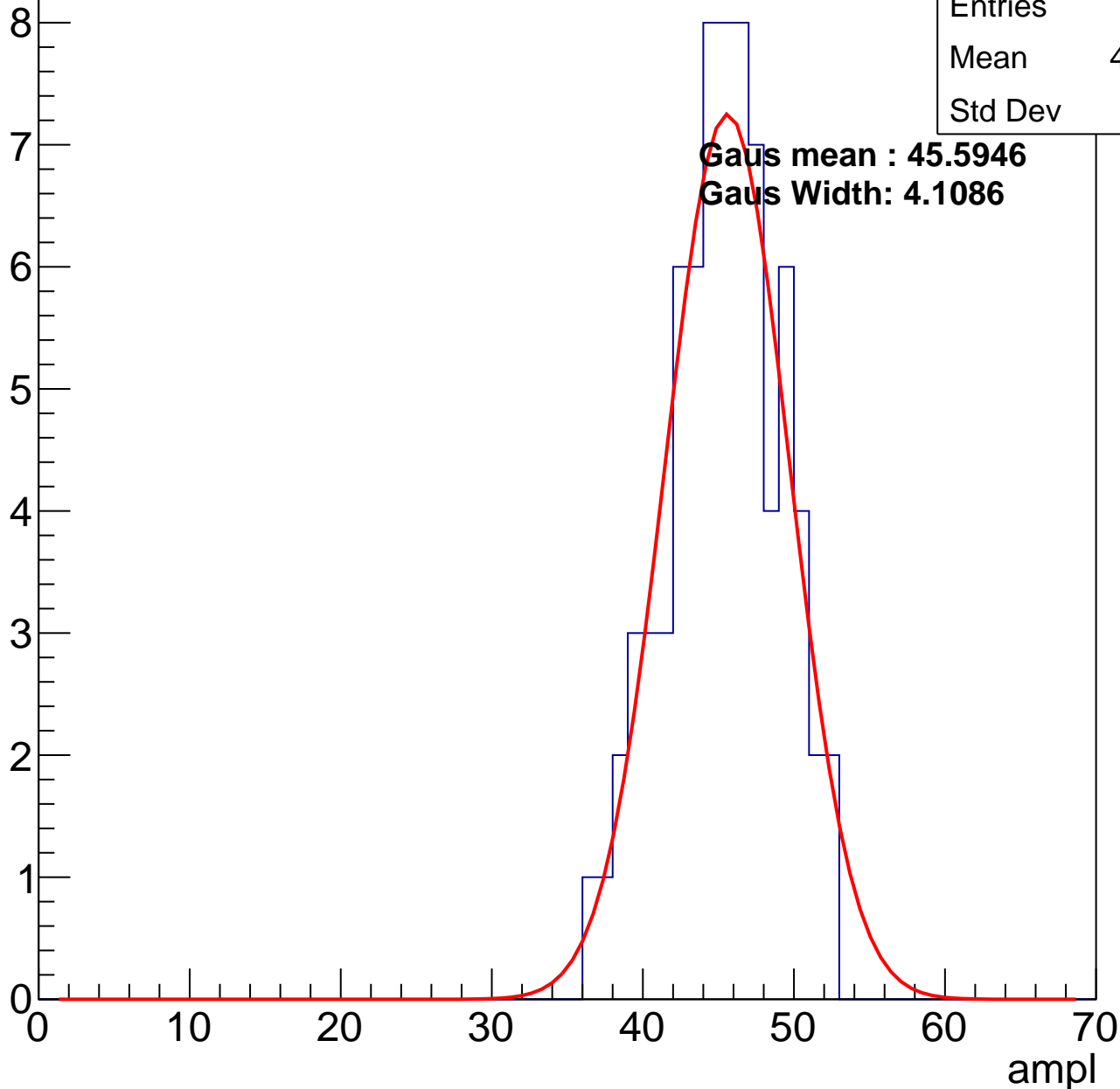
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	44.86
Std Dev	3.67

**Gaus mean : 45.5946**

**Gaus Width: 4.1086**

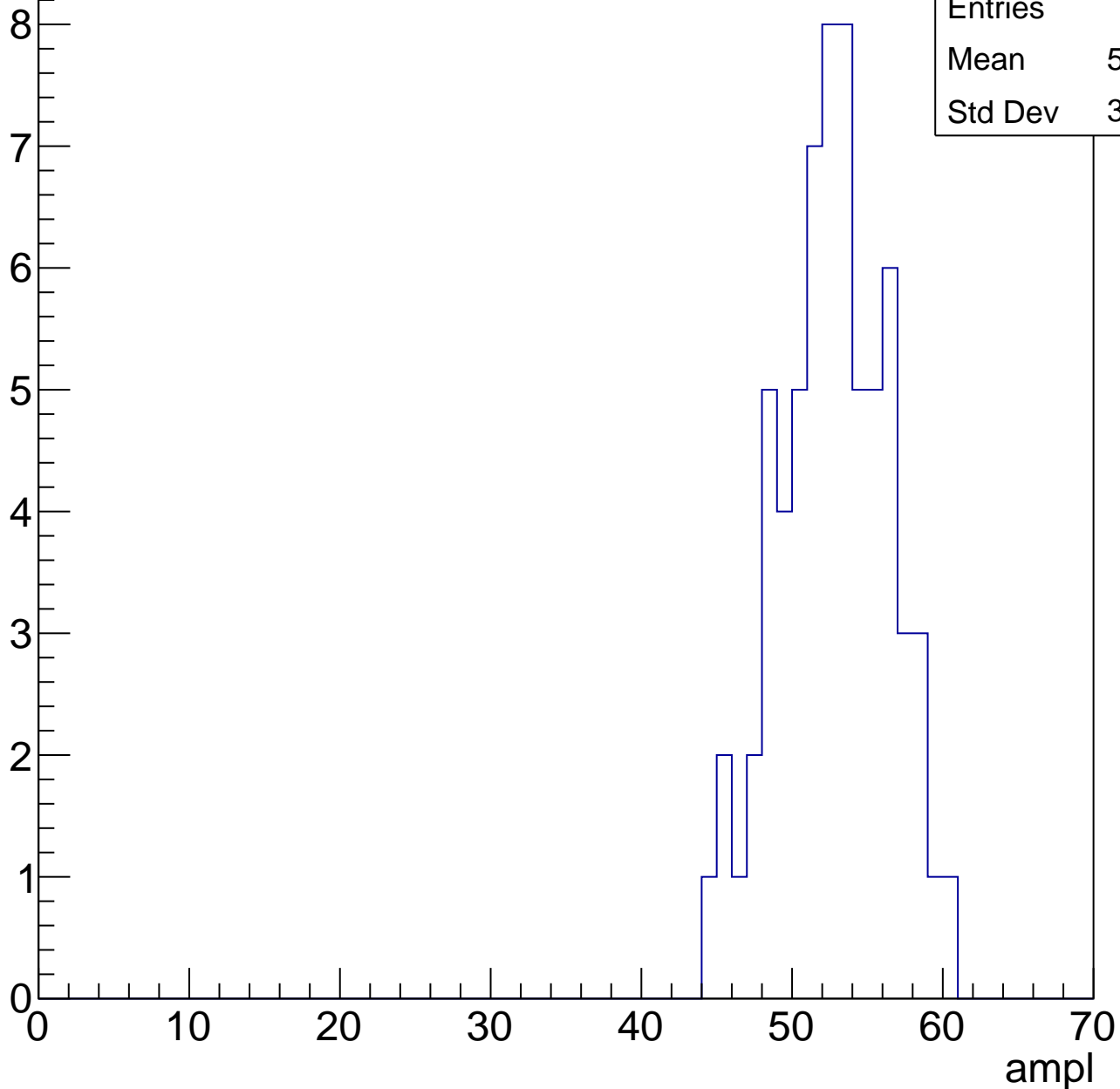


# B0L001S, U10-ch123, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	52.27
Std Dev	3.564

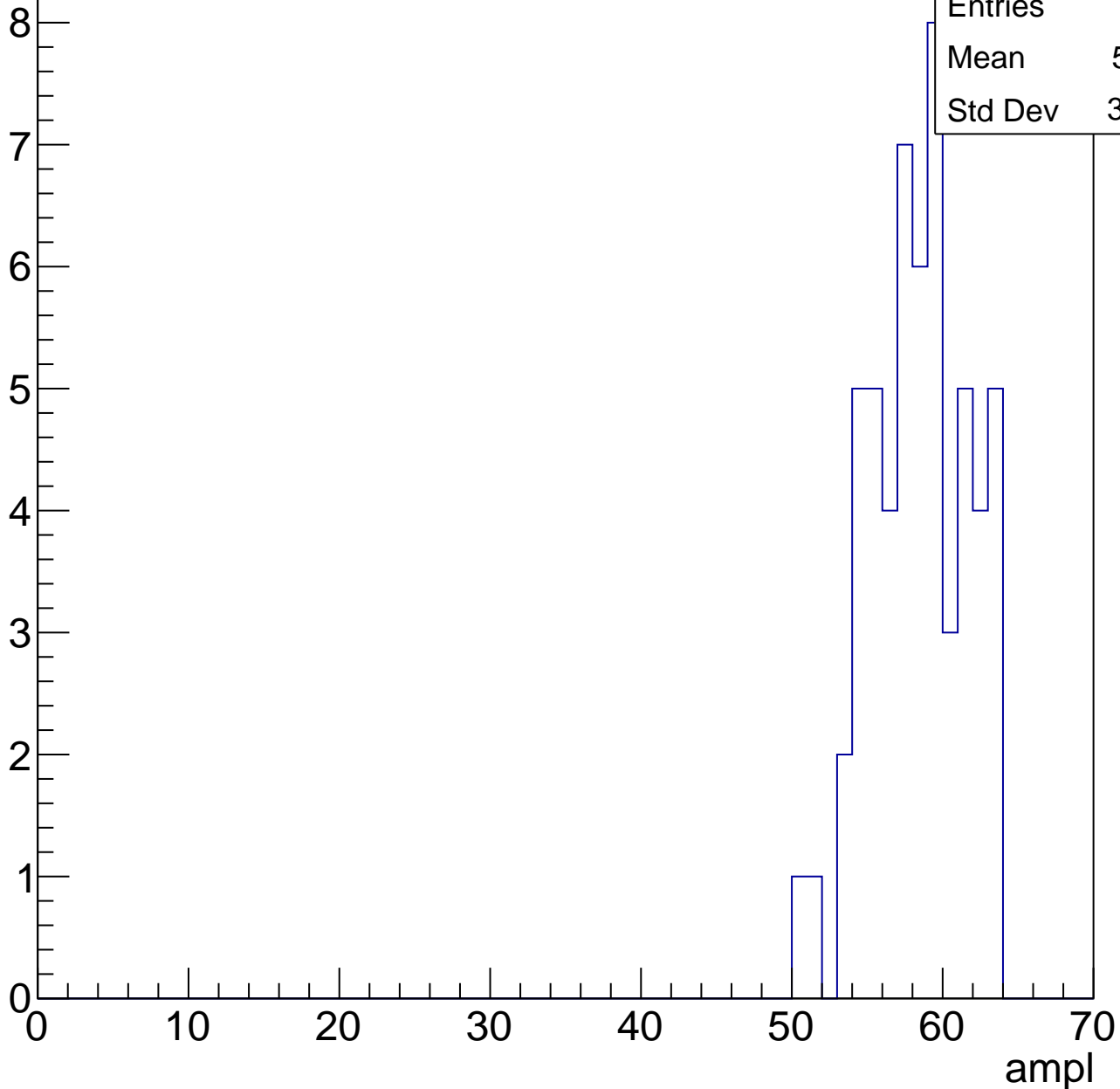


# B0L001S, U10-ch123, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	57.91
Std Dev	3.175

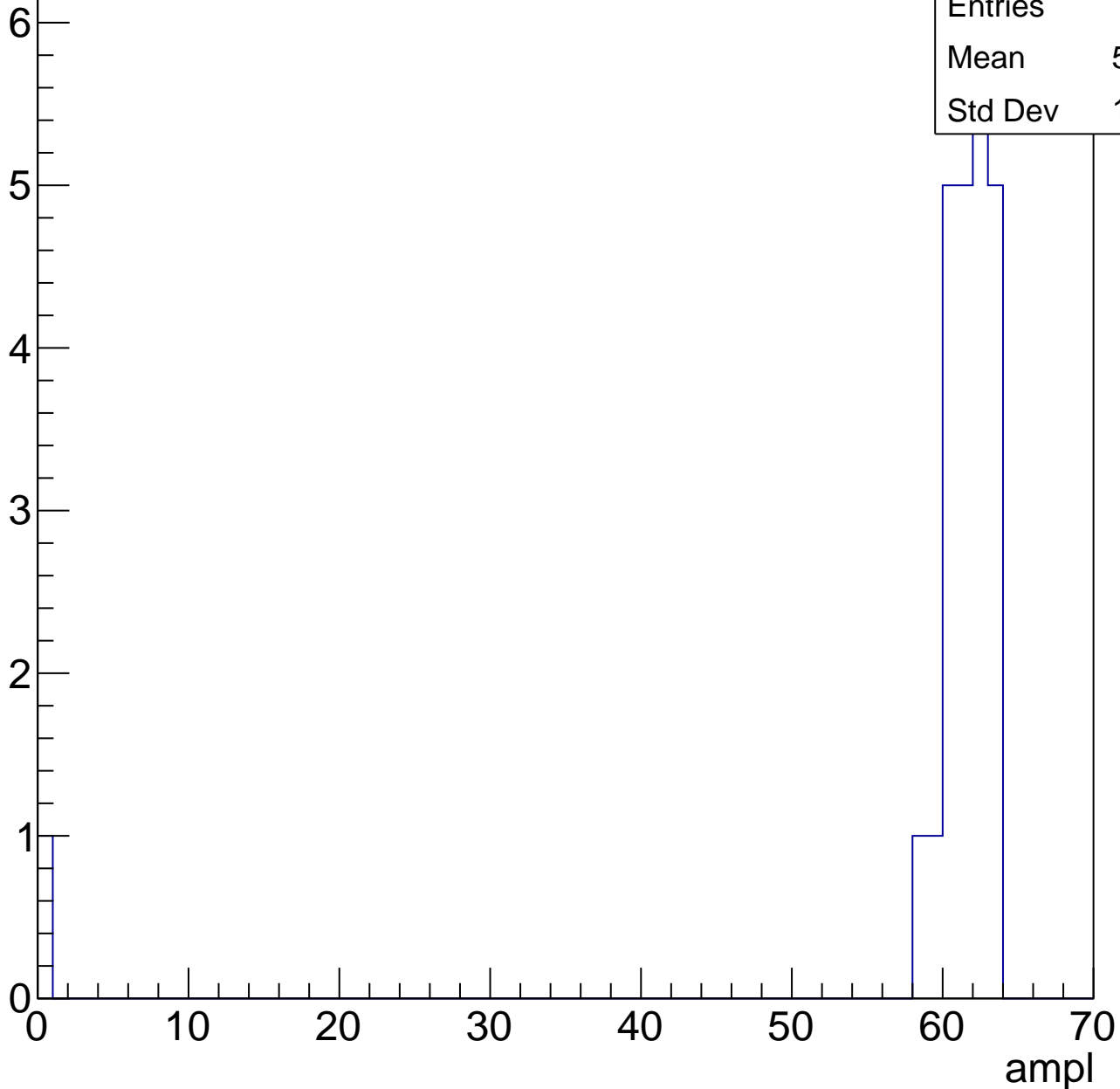


# B0L001S, U10-ch123, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	24
Mean	58.71
Std Dev	12.31



# B0L001S, U10-ch123, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch123, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U10-ch124, adc0

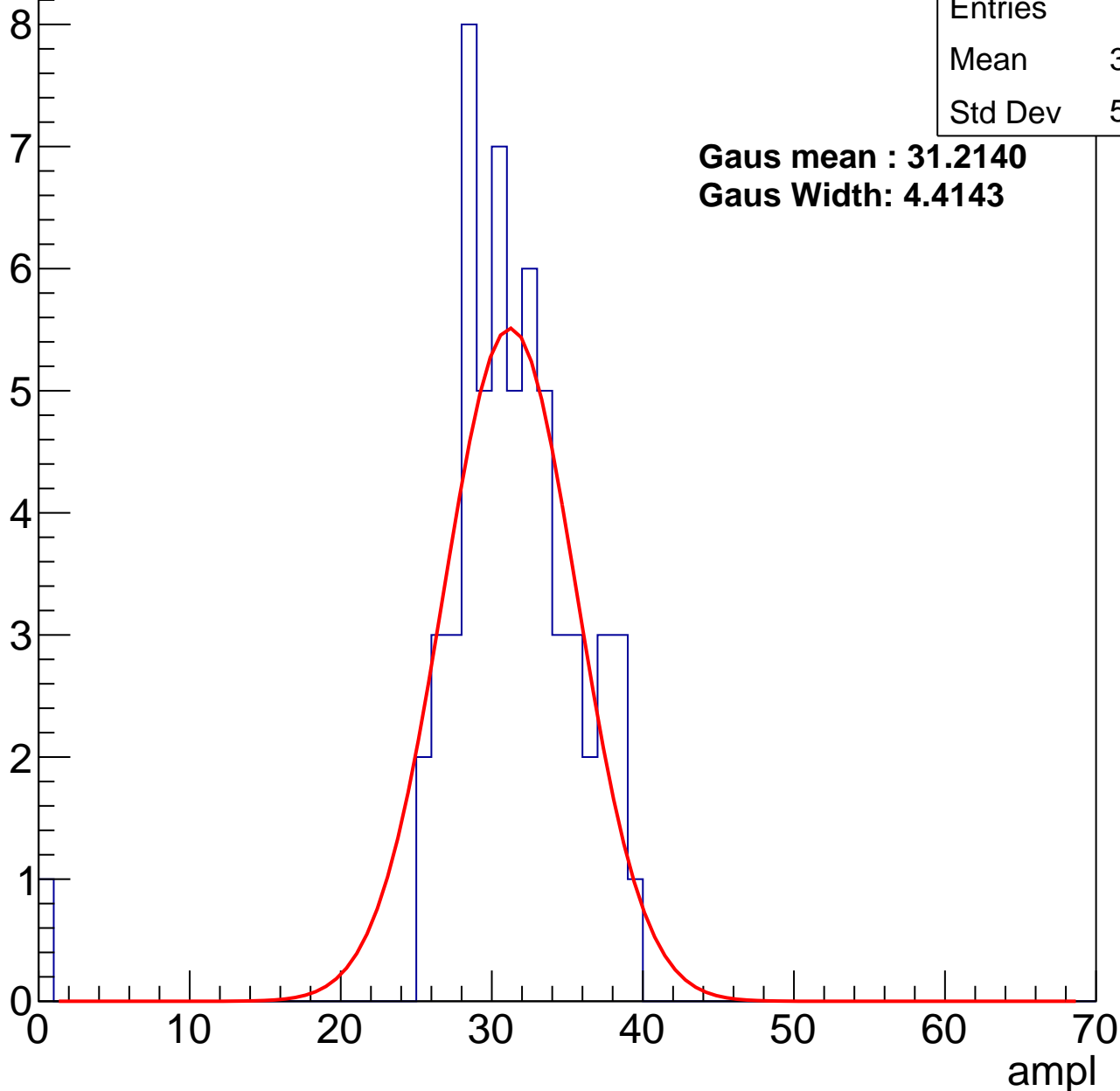
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	30.72
Std Dev	5.354

**Gaus mean : 31.2140**

**Gaus Width: 4.4143**



# B0L001S, U10-ch124, adc1

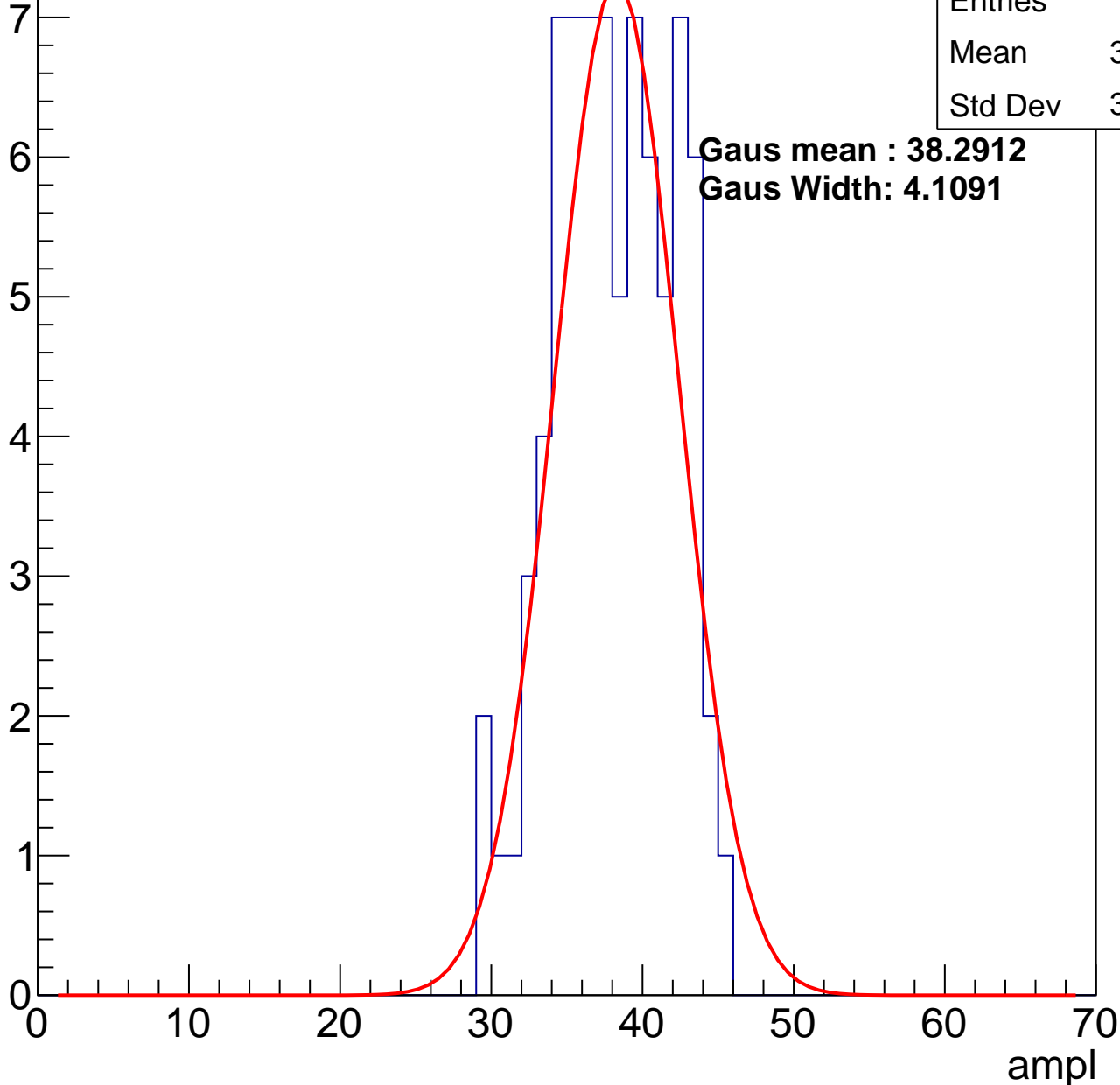
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	78
Mean	37.62
Std Dev	3.824

**Gaus mean : 38.2912**

**Gaus Width: 4.1091**



# B0L001S, U10-ch124, adc2

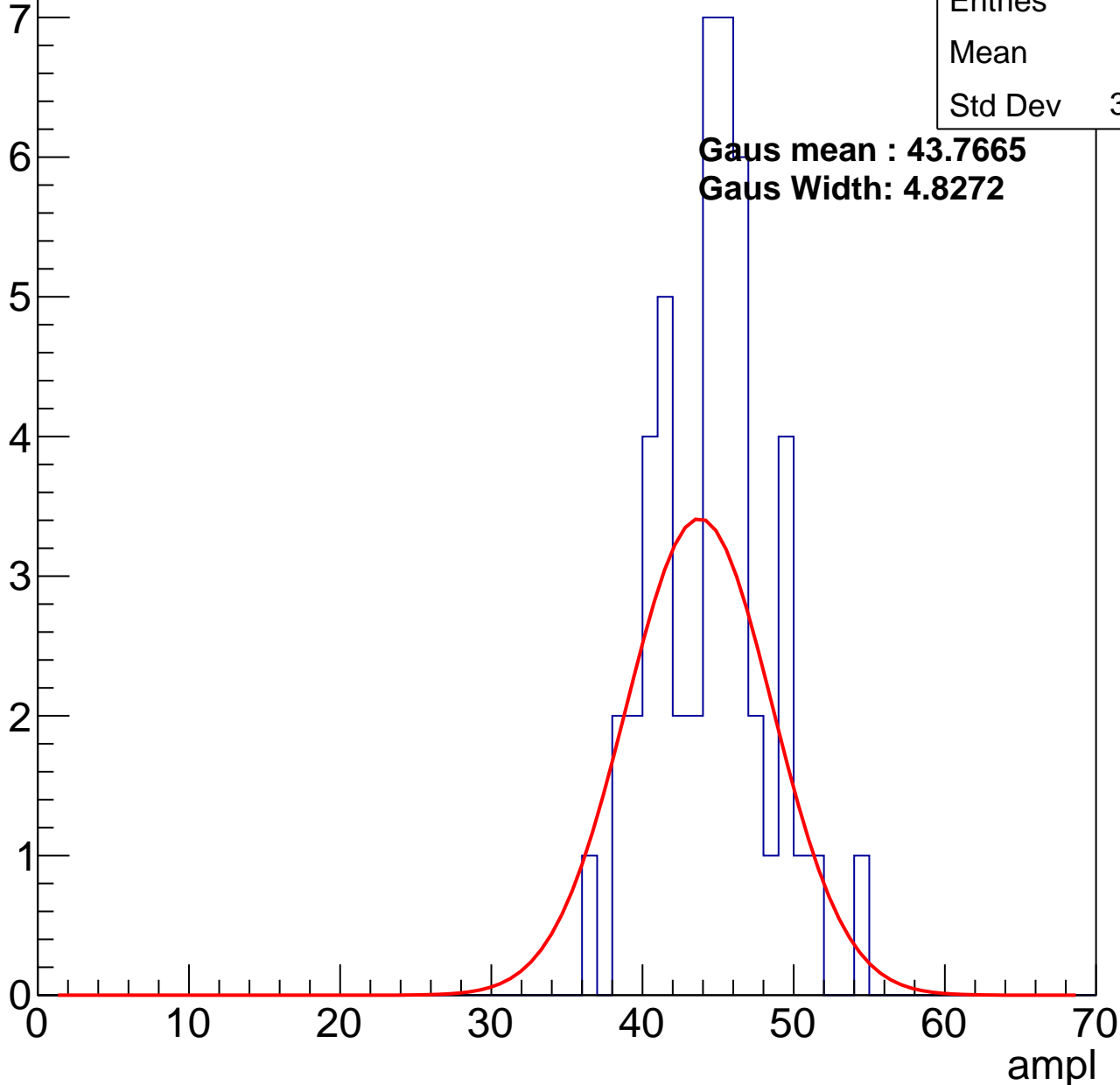
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	48
Mean	44.1
Std Dev	3.693

**Gaus mean : 43.7665**

**Gaus Width: 4.8272**

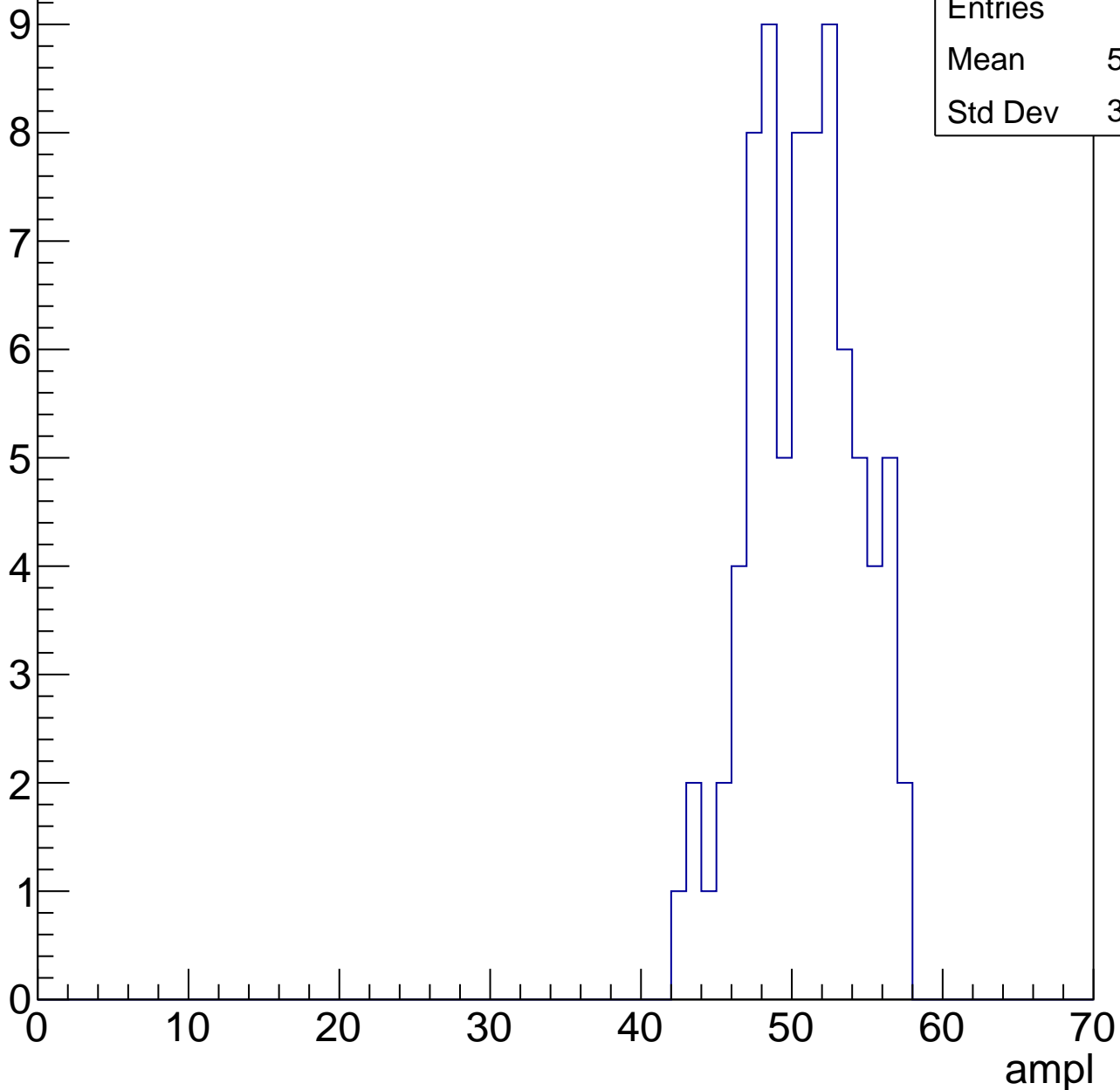


# B0L001S, U10-ch124, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	79
Mean	50.34
Std Dev	3.507

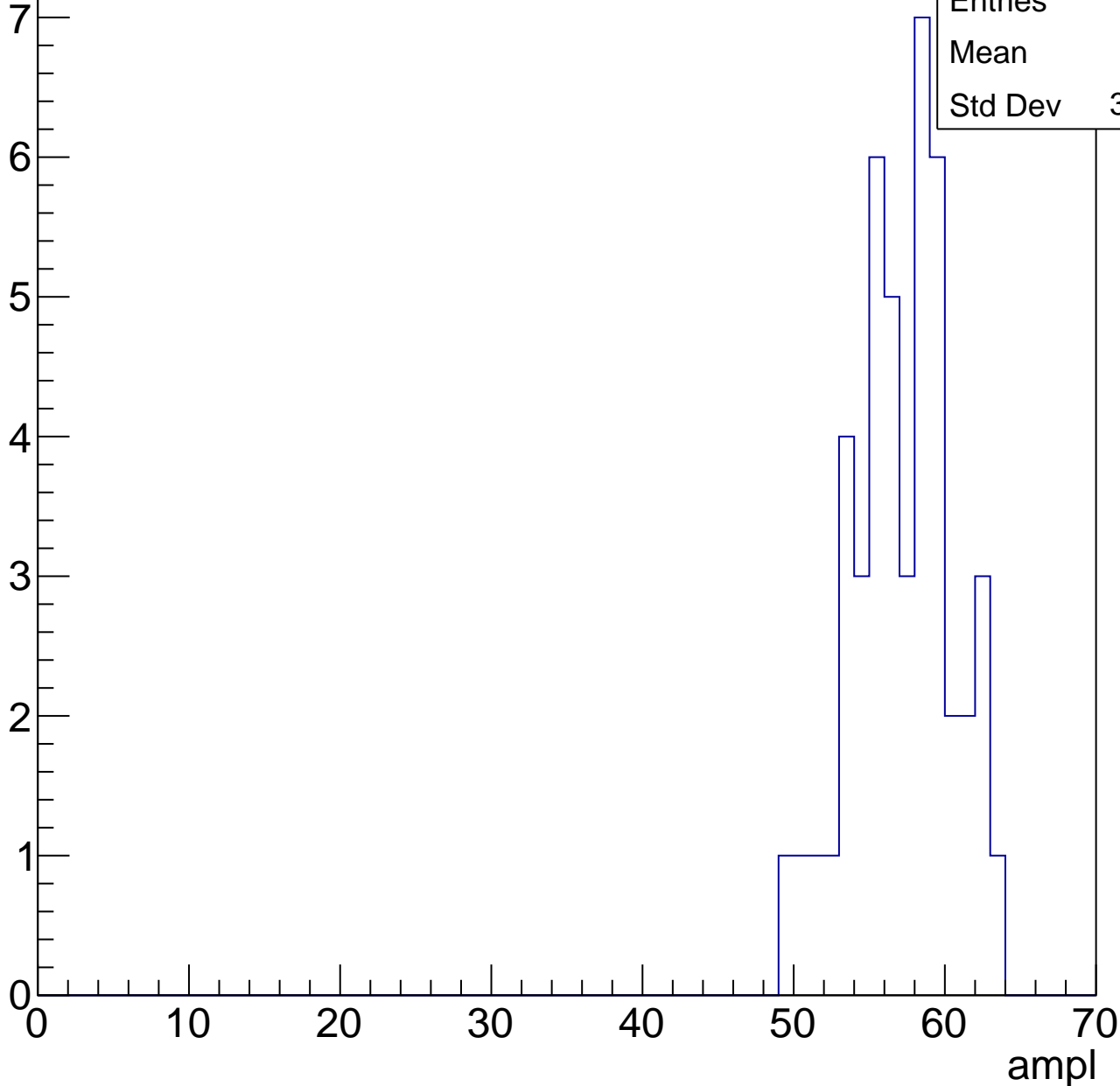


# B0L001S, U10-ch124, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	46
Mean	56.7
Std Dev	3.236

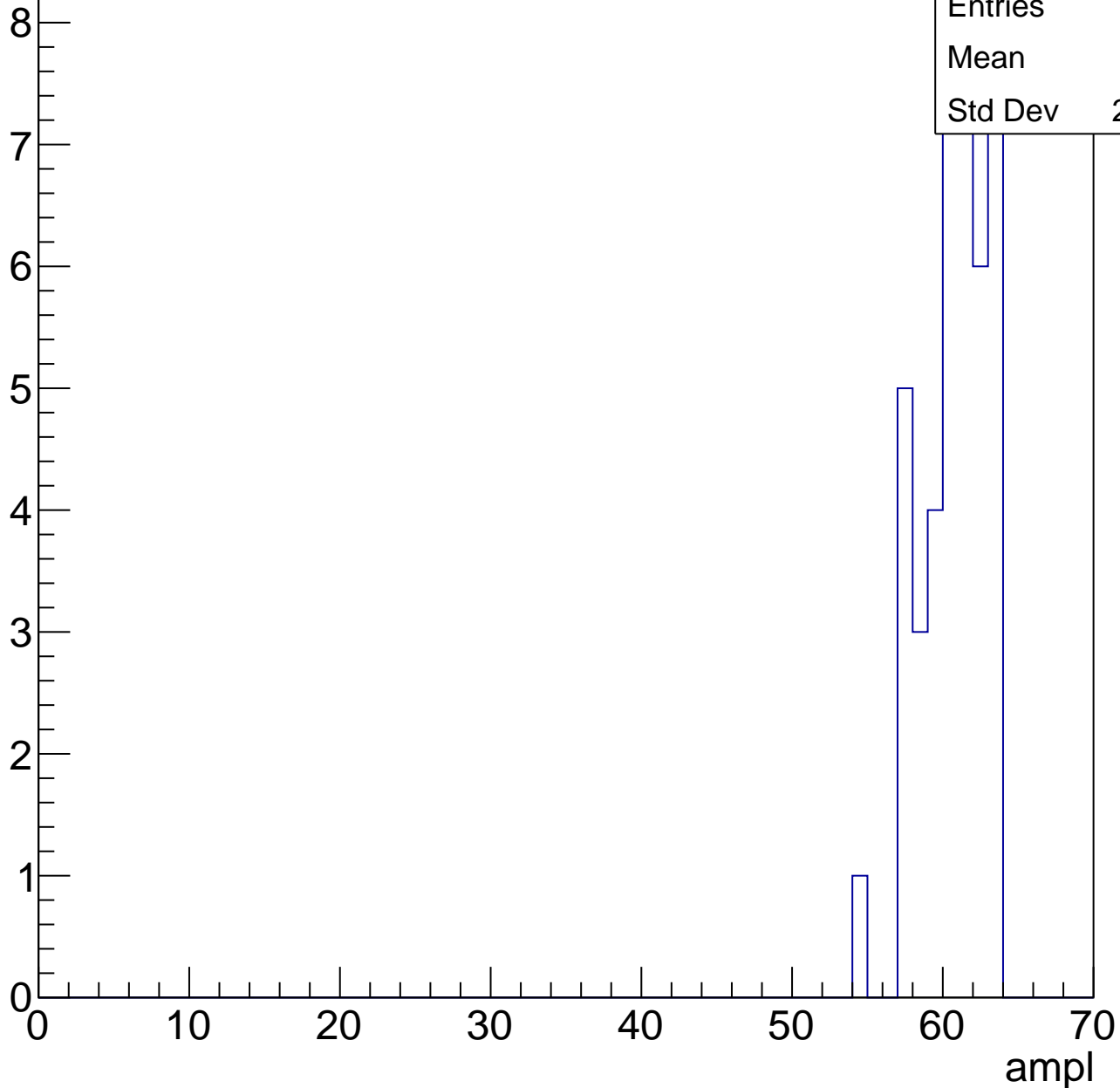


# B0L001S, U10-ch124, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

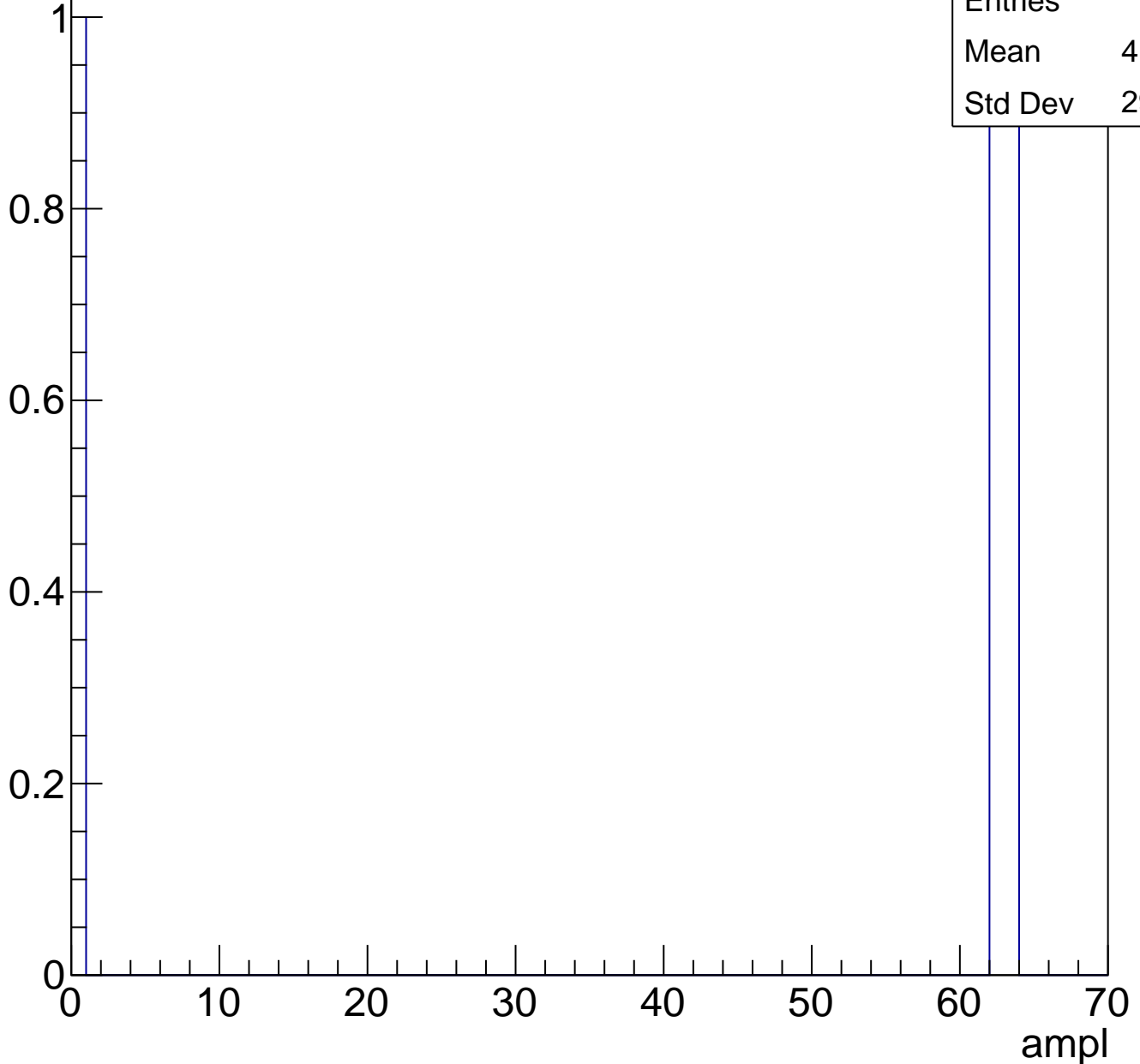
Entries	43
Mean	60.3
Std Dev	2.141



# B0L001S, U10-ch124, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U10-ch124, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	10
Std Dev	10

# B0L001S, U10-ch125, adc0

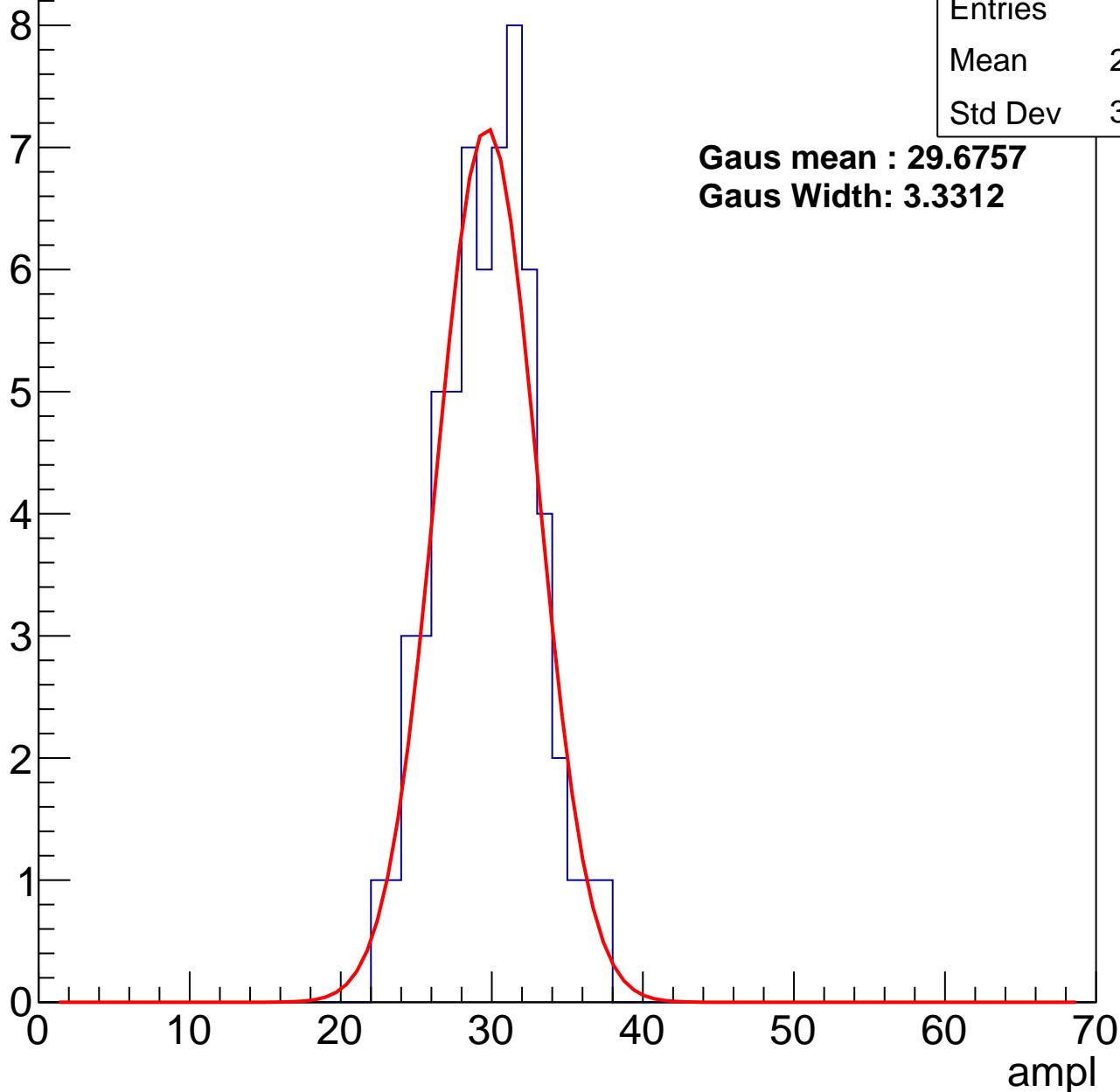
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	29.26
Std Dev	3.218

**Gaus mean : 29.6757**

**Gaus Width: 3.3312**



# B0L001S, U10-ch125, adc1

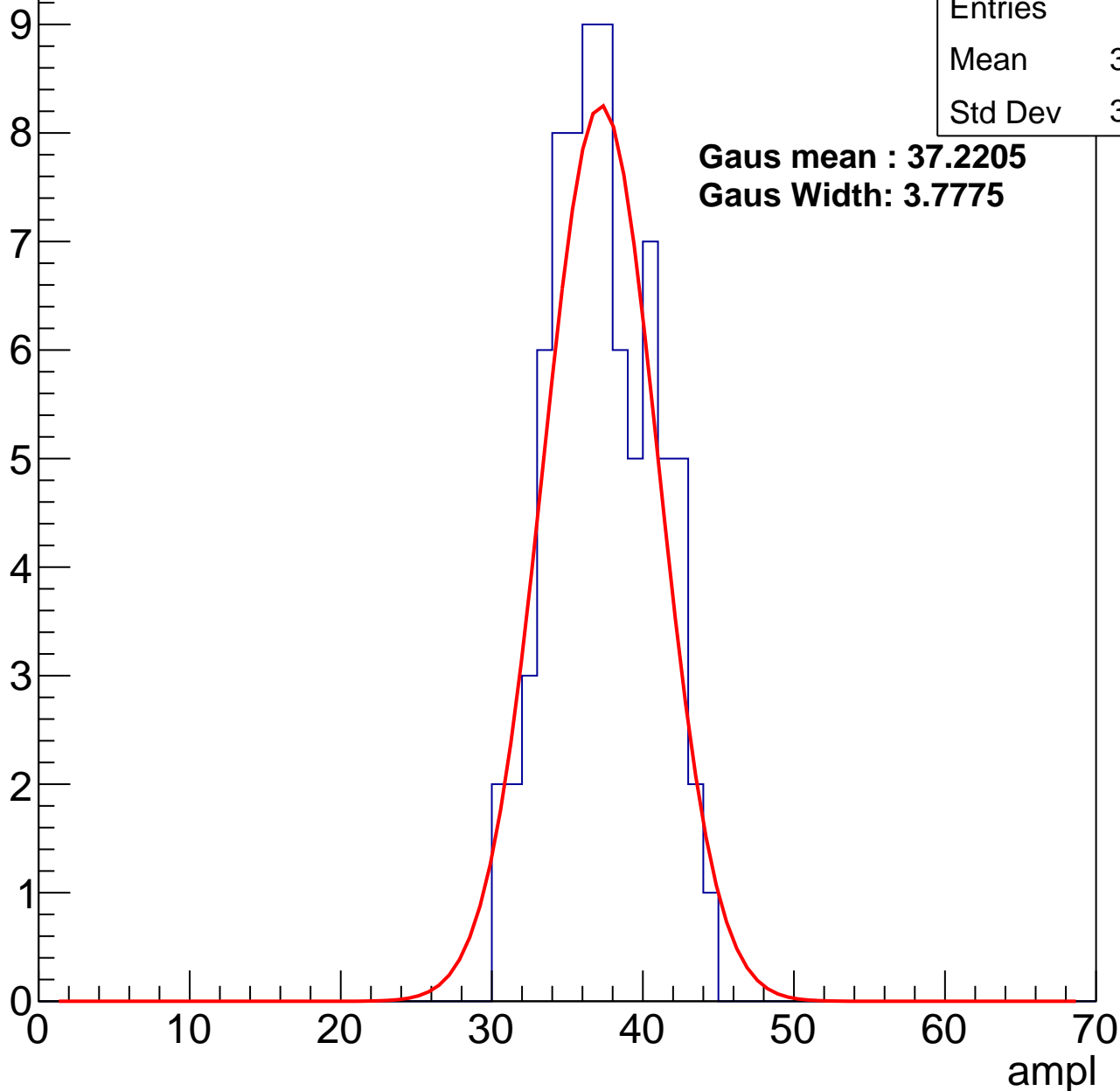
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	78
Mean	36.83
Std Dev	3.334

**Gaus mean : 37.2205**

**Gaus Width: 3.7775**



# B0L001S, U10-ch125, adc2

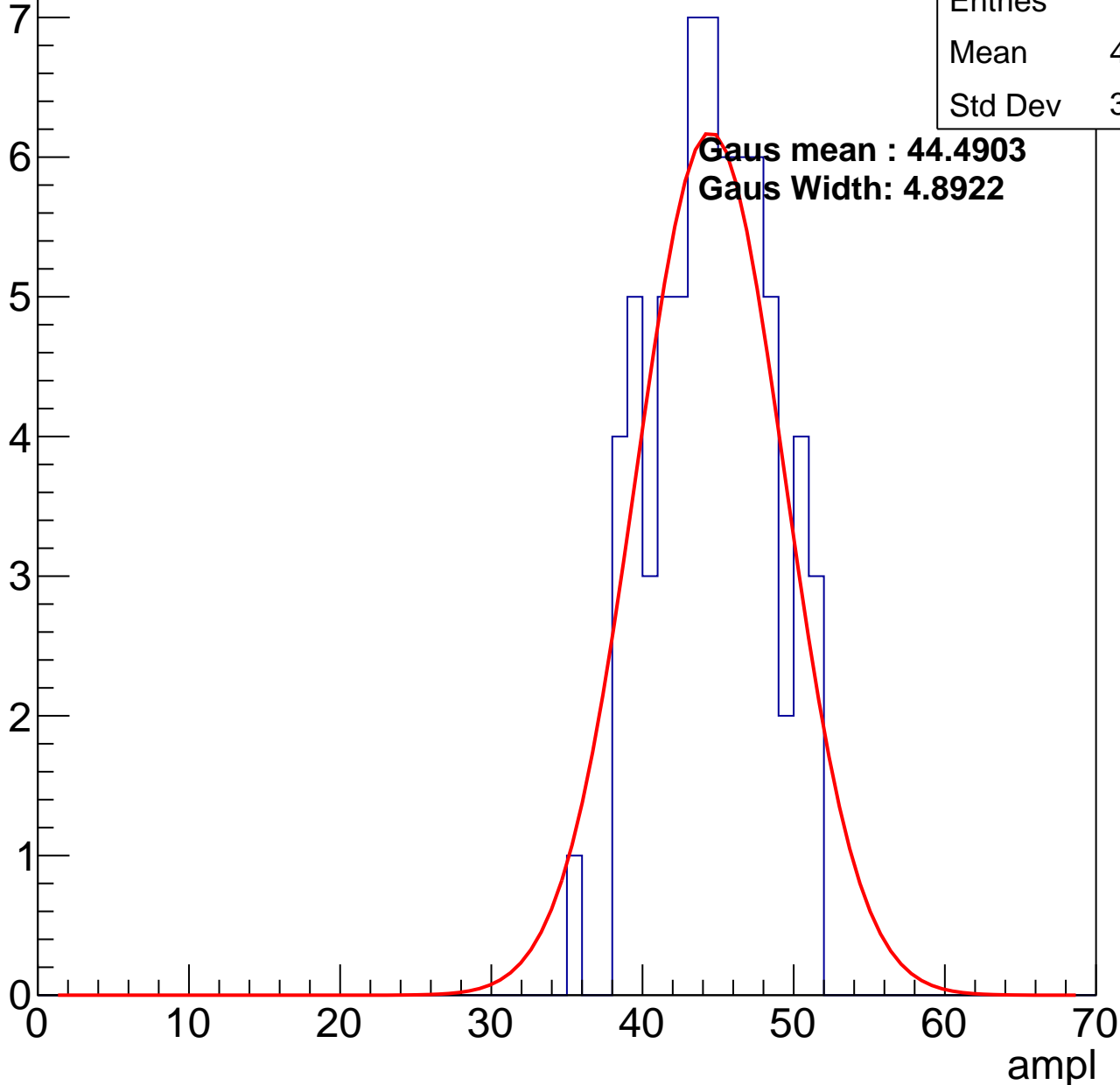
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	44.13
Std Dev	3.757

**Gaus mean : 44.4903**

**Gaus Width: 4.8922**



# B0L001S, U10-ch125, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	65
Mean	50.49
Std Dev	3.565

Entry

10

8

6

4

2

0

0

10

20

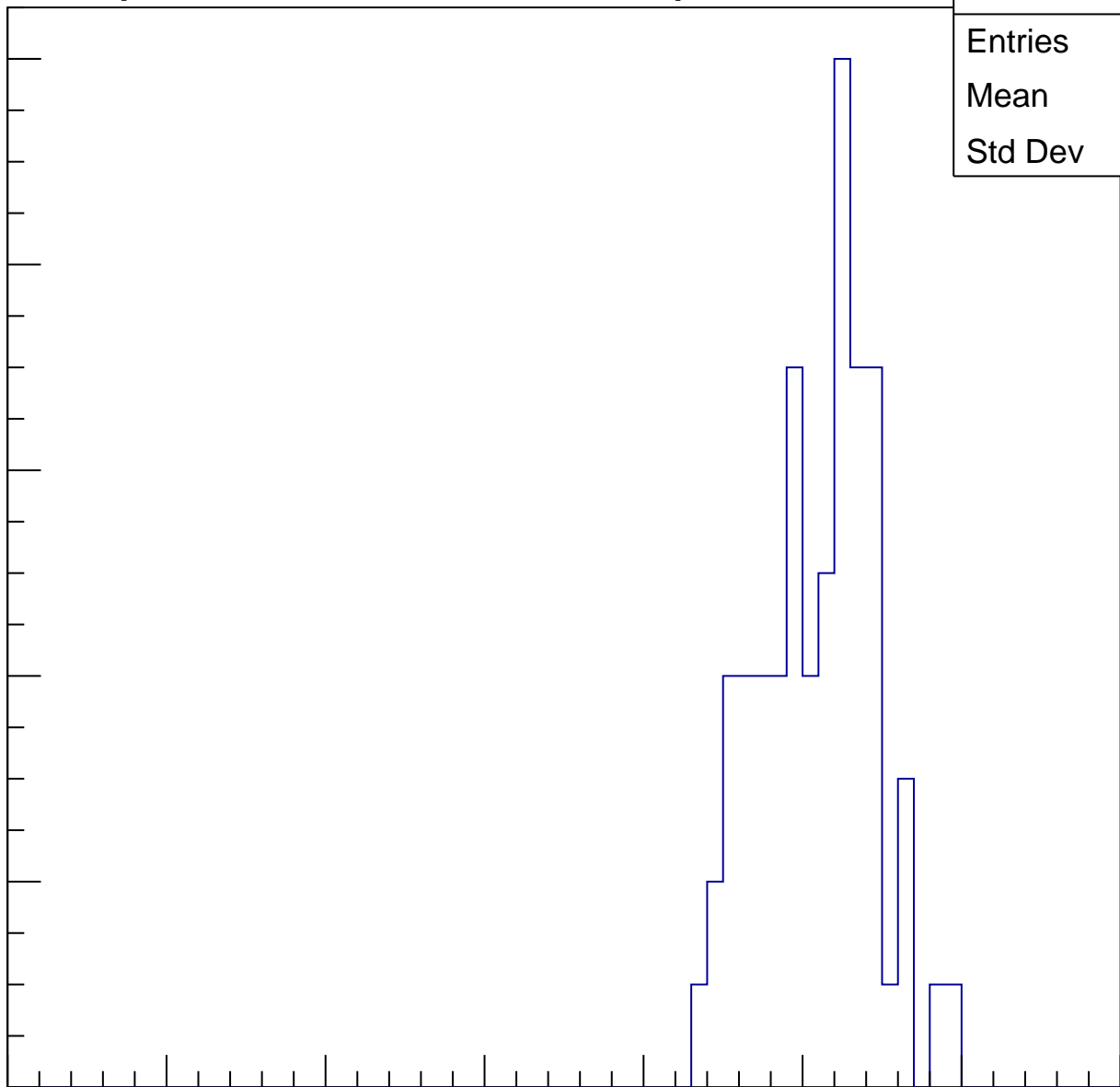
30

40

50

60

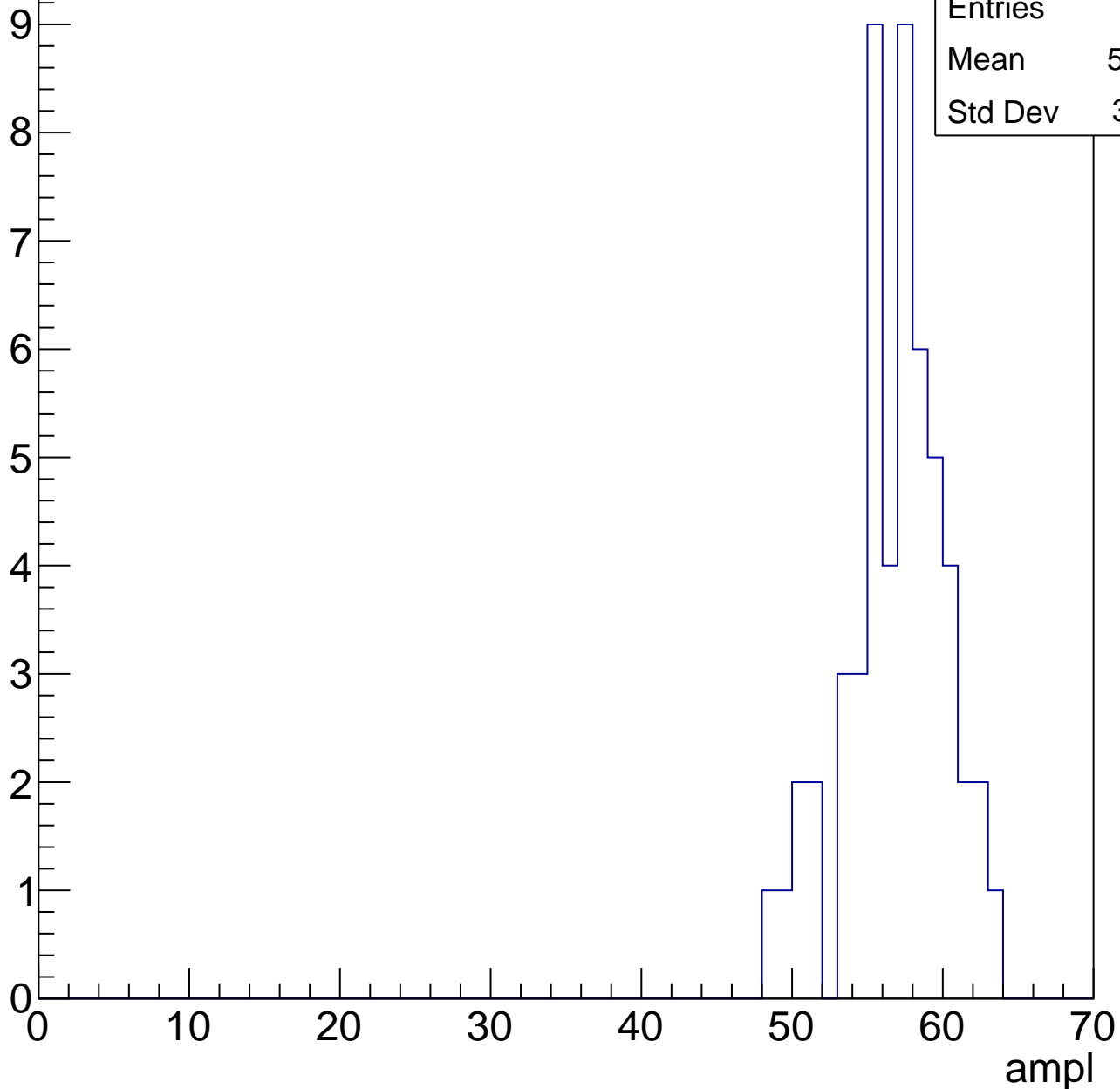
ampl



# B0L001S, U10-ch125, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



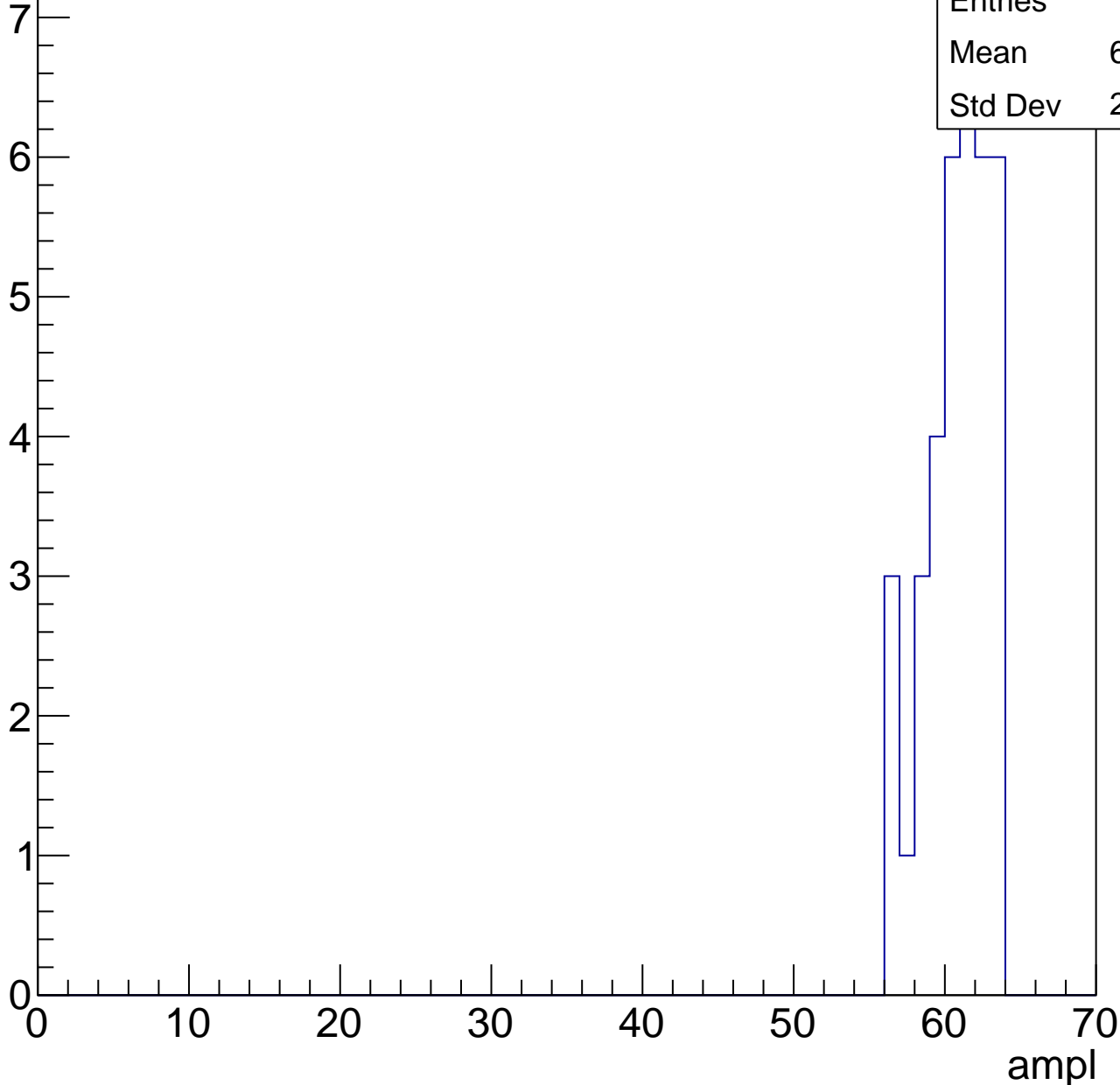
Entries	54
Mean	56.37
Std Dev	3.301

# B0L001S, U10-ch125, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

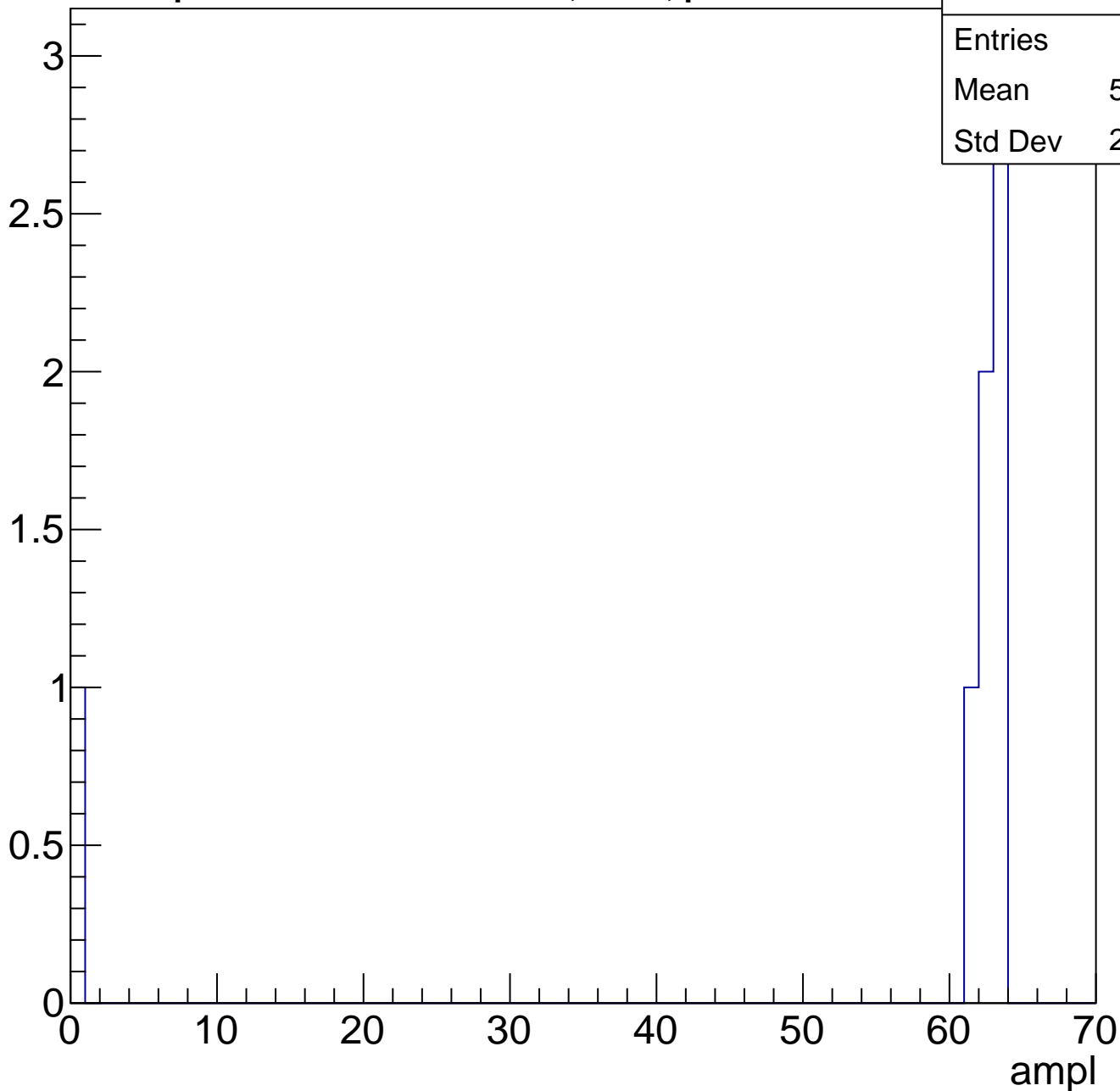
Entries	36
Mean	60.33
Std Dev	2.068



# B0L001S, U10-ch125, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	7
Mean	53.43
Std Dev	21.82



# B0L001S, U10-ch125, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	3
Mean	0
Std Dev	0

# B0L001S, U10-ch126, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	65
Mean	29.98
Std Dev	5.028

**Gaus mean : 30.5130**

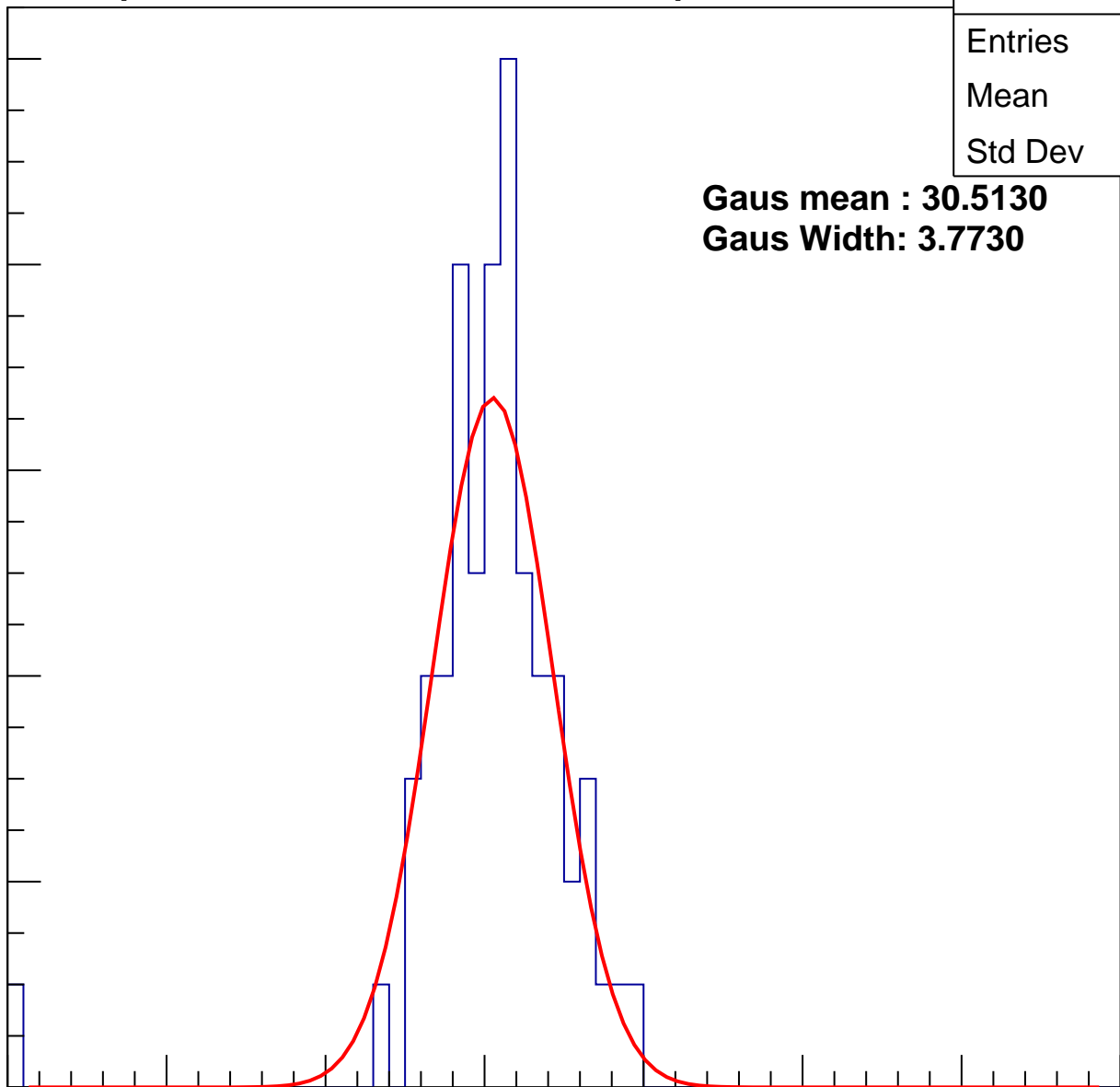
**Gaus Width: 3.7730**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U10-ch126, adc1

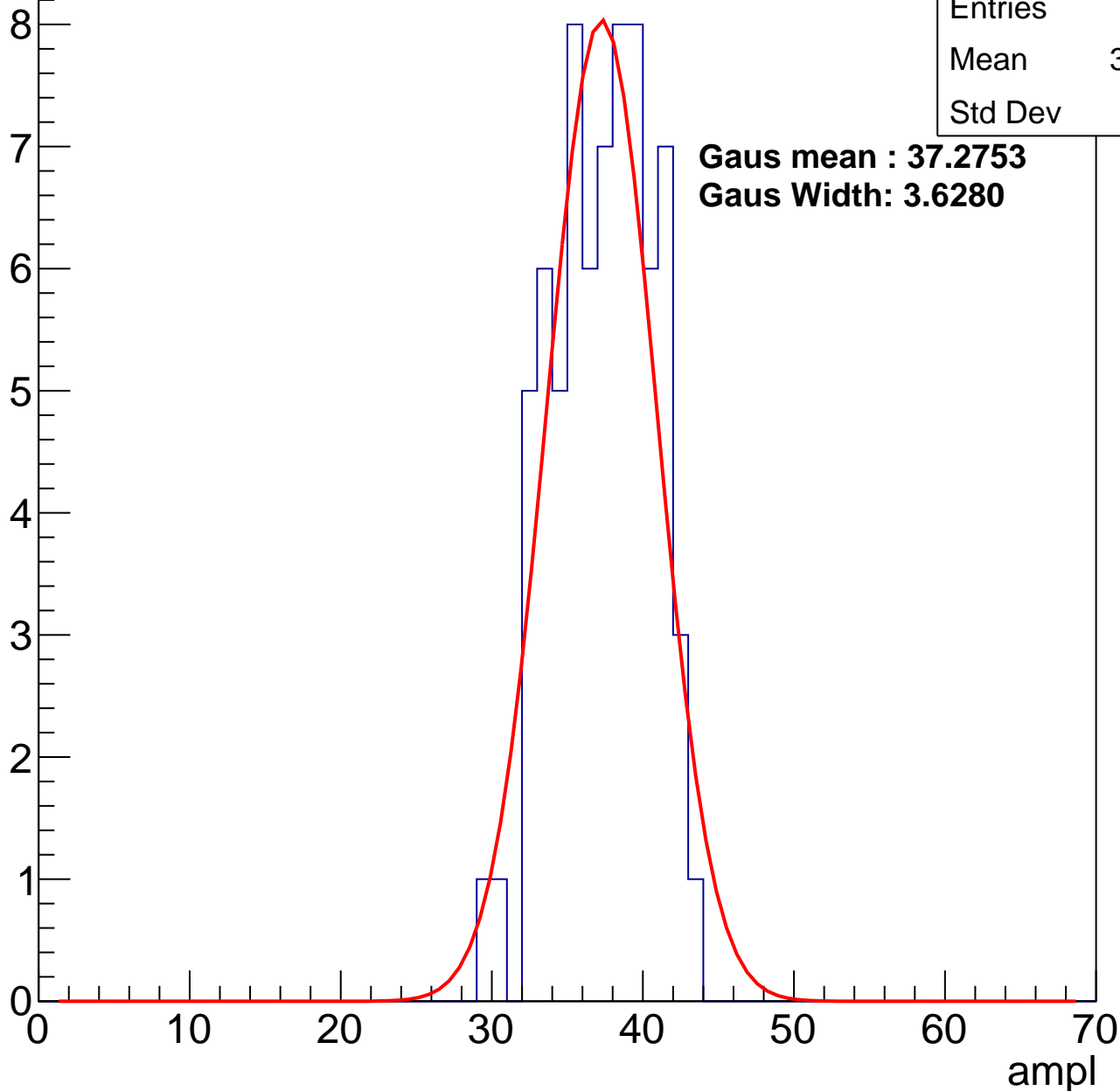
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	36.86
Std Dev	3.19

**Gaus mean : 37.2753**

**Gaus Width: 3.6280**



# B0L001S, U10-ch126, adc2

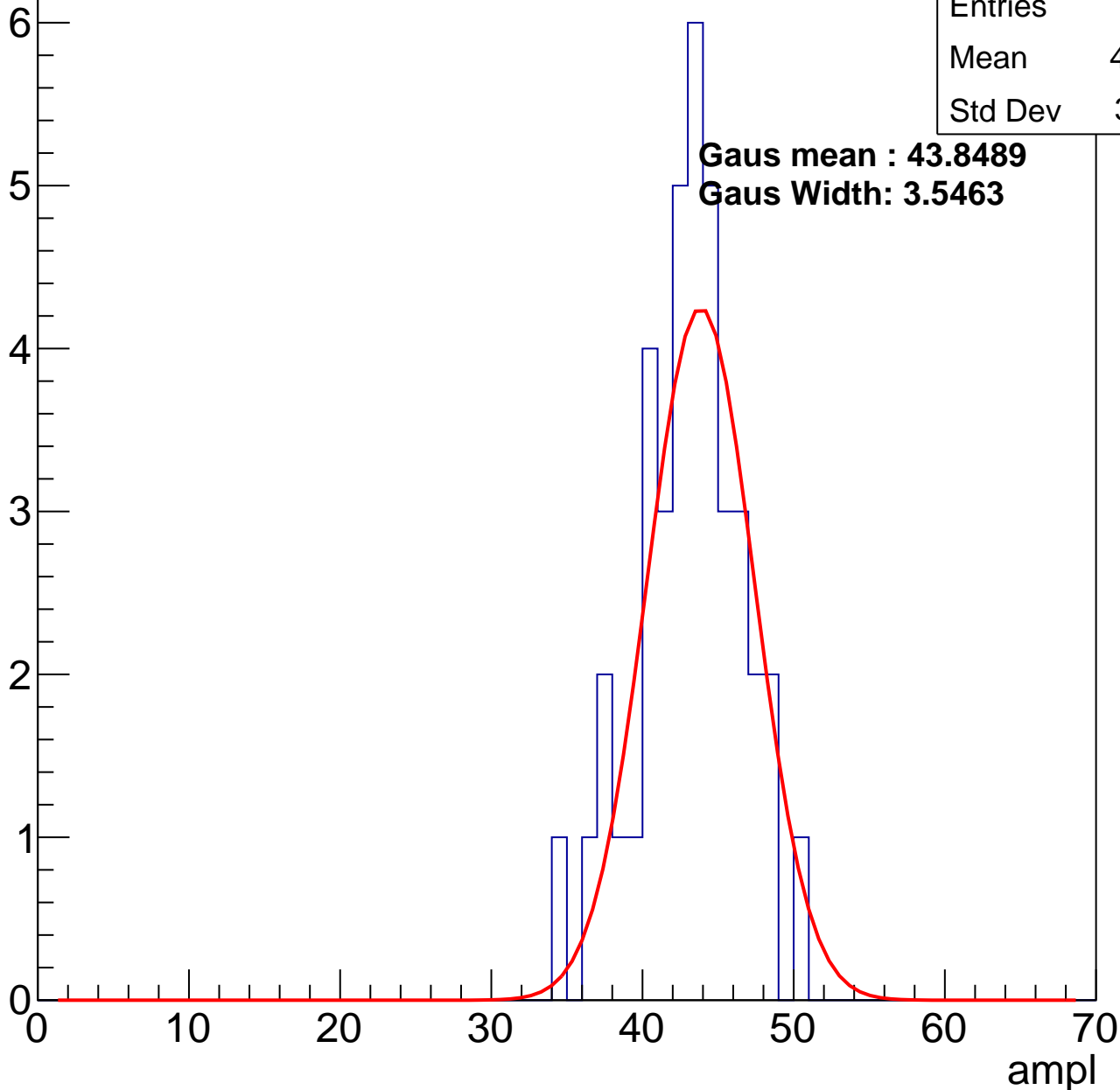
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	40
Mean	42.62
Std Dev	3.411

**Gaus mean : 43.8489**

**Gaus Width: 3.5463**

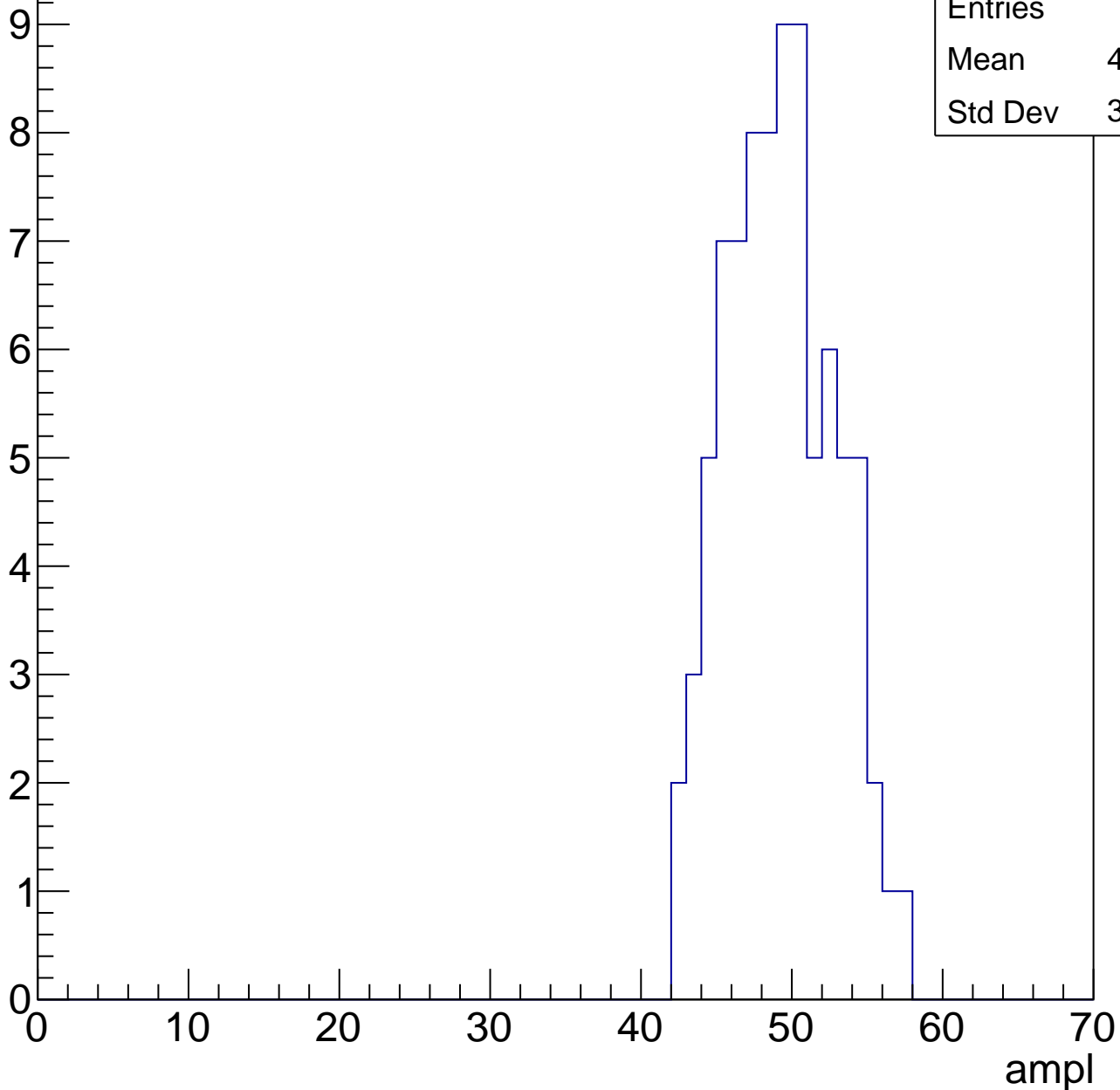


# B0L001S, U10-ch126, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	83
Mean	48.75
Std Dev	3.495

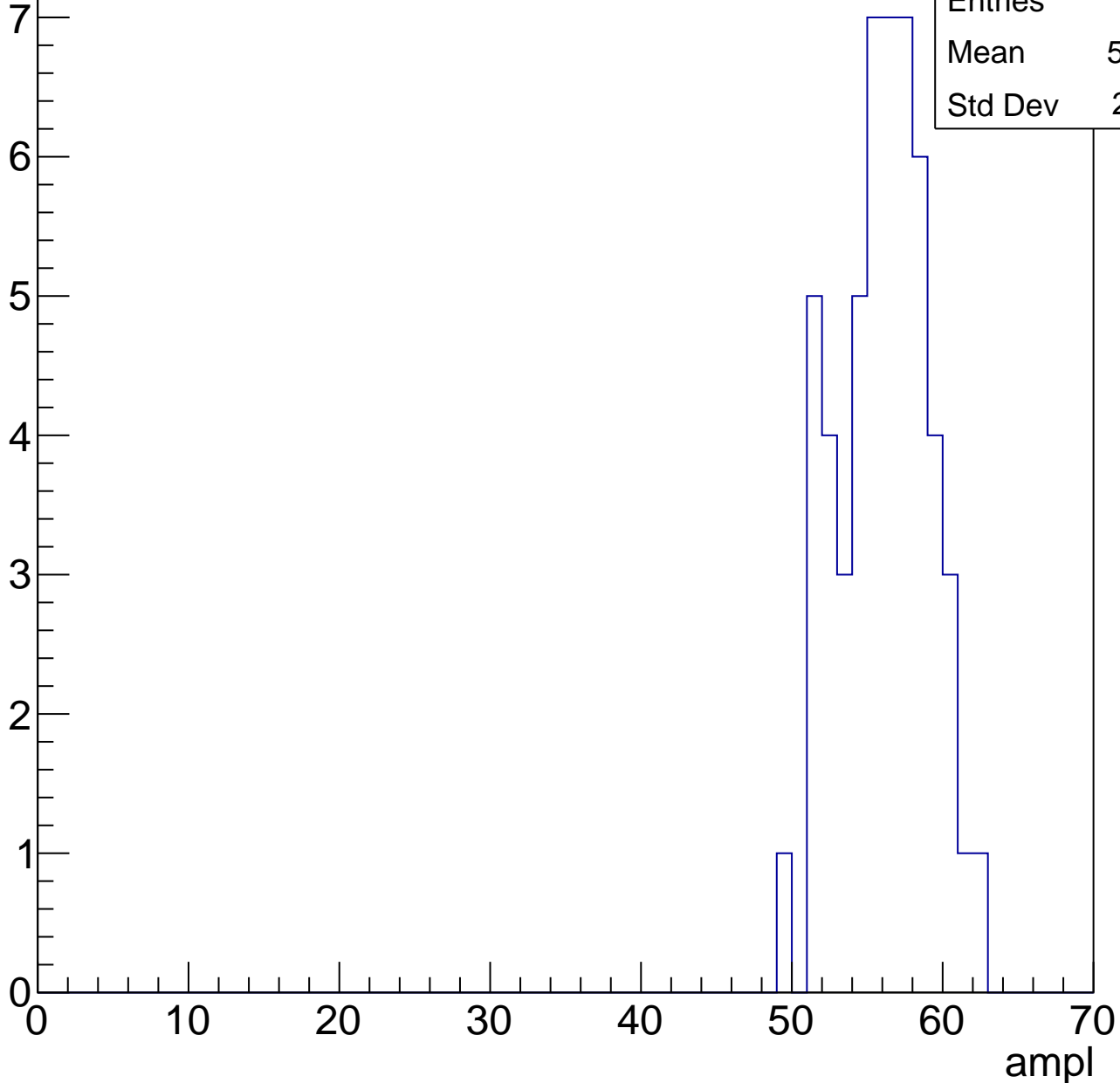


# B0L001S, U10-ch126, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	55.63
Std Dev	2.921

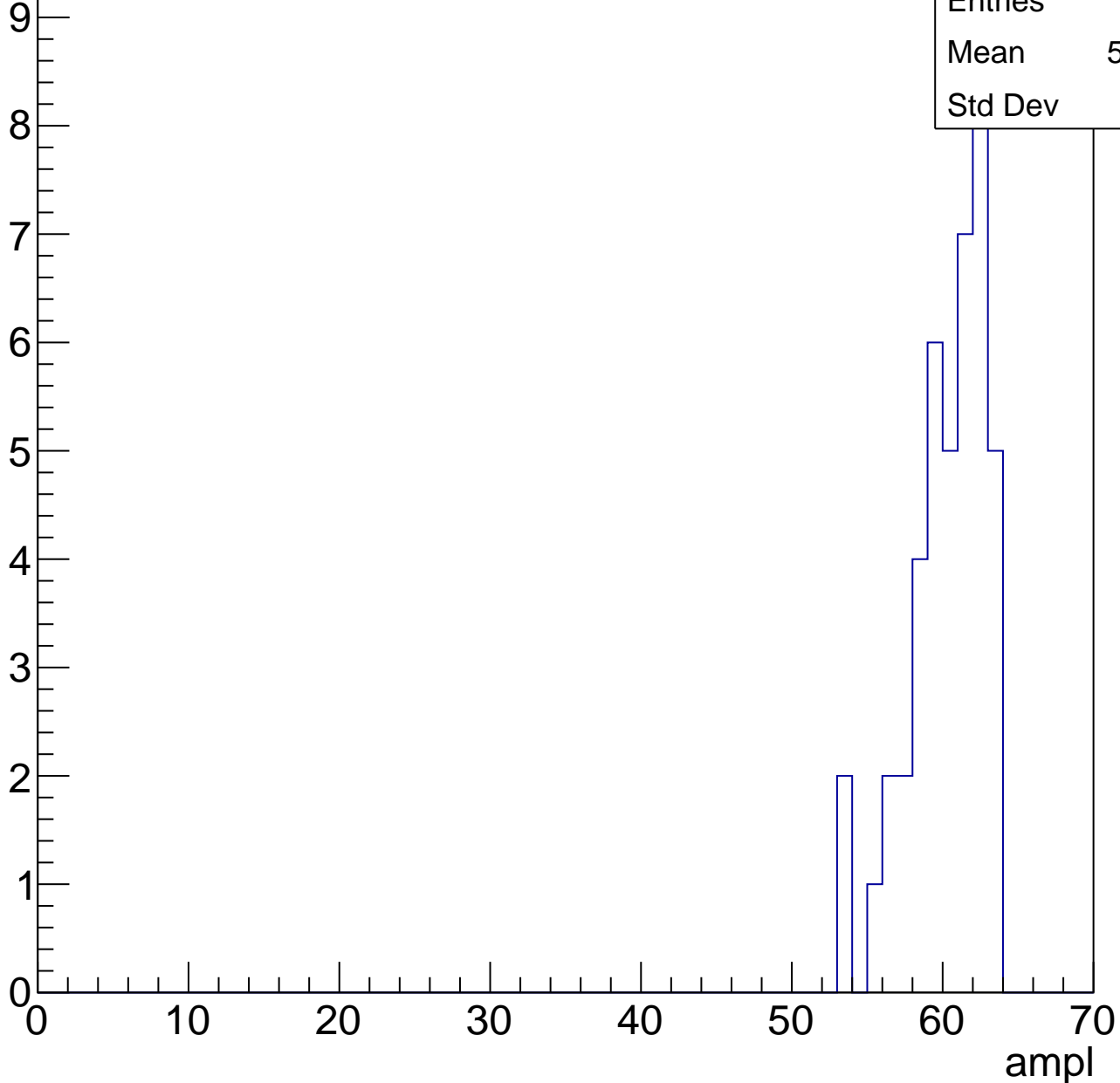


# B0L001S, U10-ch126, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	43
Mean	59.84
Std Dev	2.56

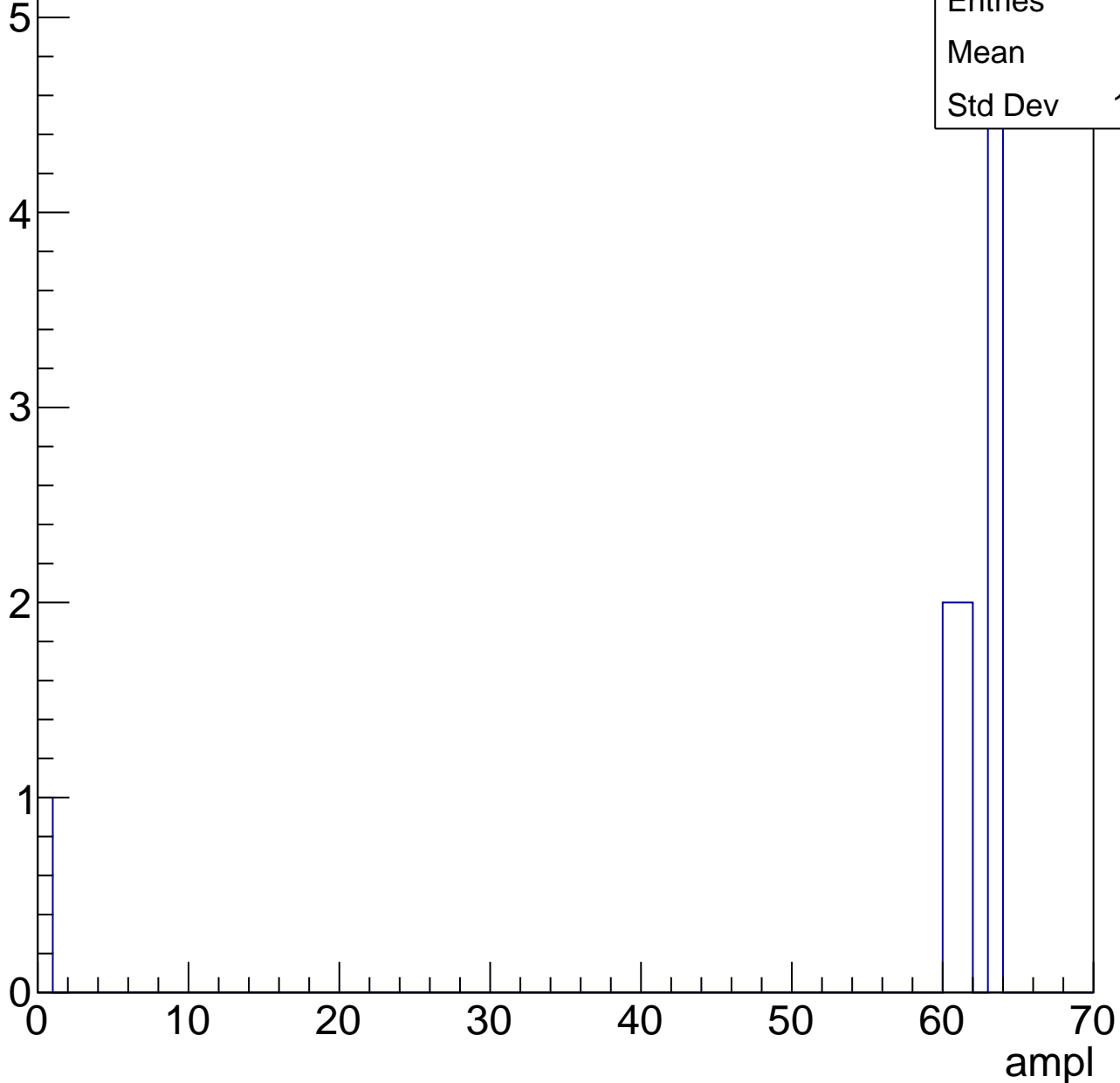


# B0L001S, U10-ch126, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	10
Mean	55.7
Std Dev	18.61





# B0L001S, U10-ch126, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	11
Std Dev	11

# B0L001S, U10-ch127, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	74
Mean	29
Std Dev	6.774

**Gaus mean : 30.2172**

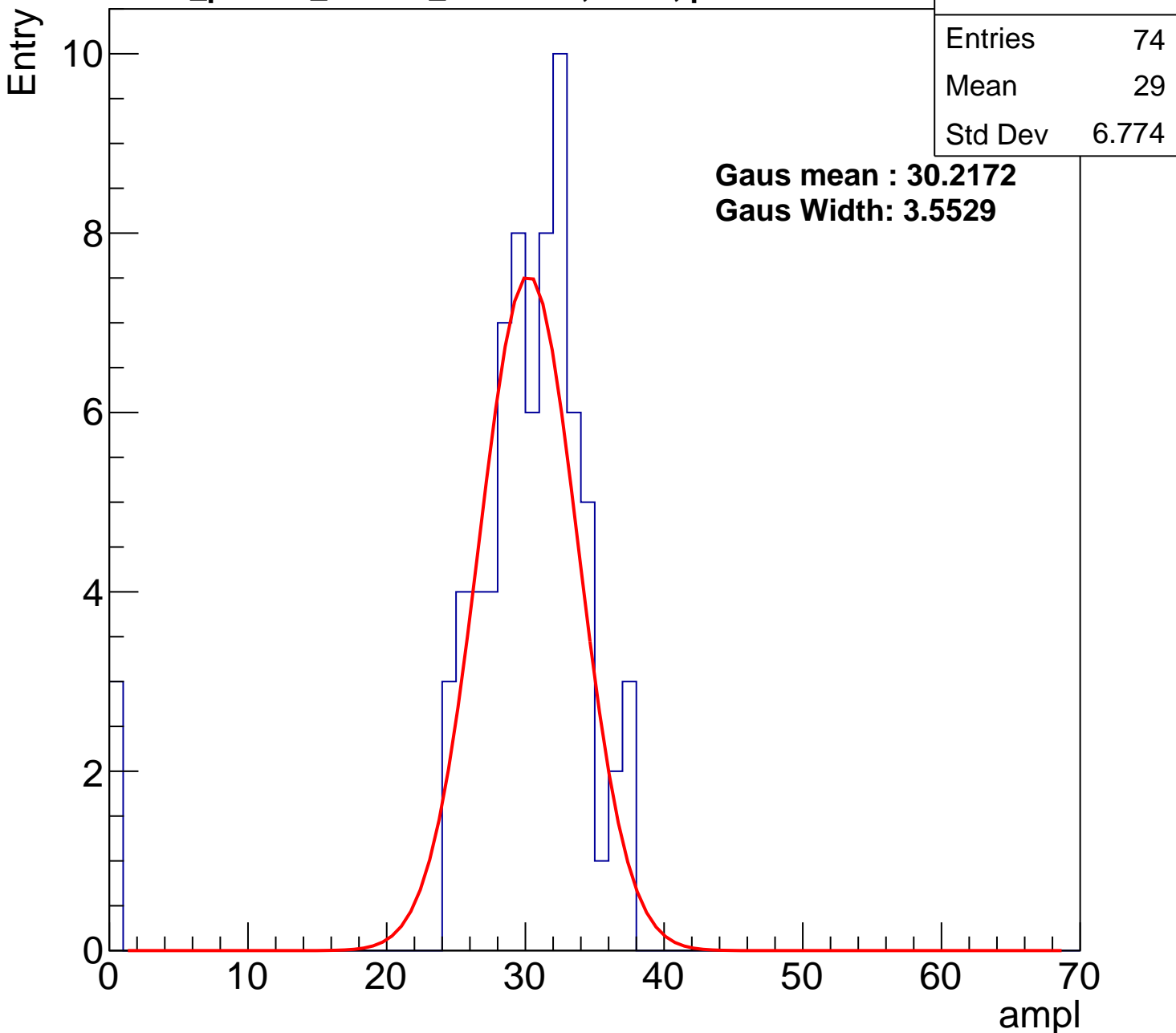
**Gaus Width: 3.5529**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U10-ch127, adc1

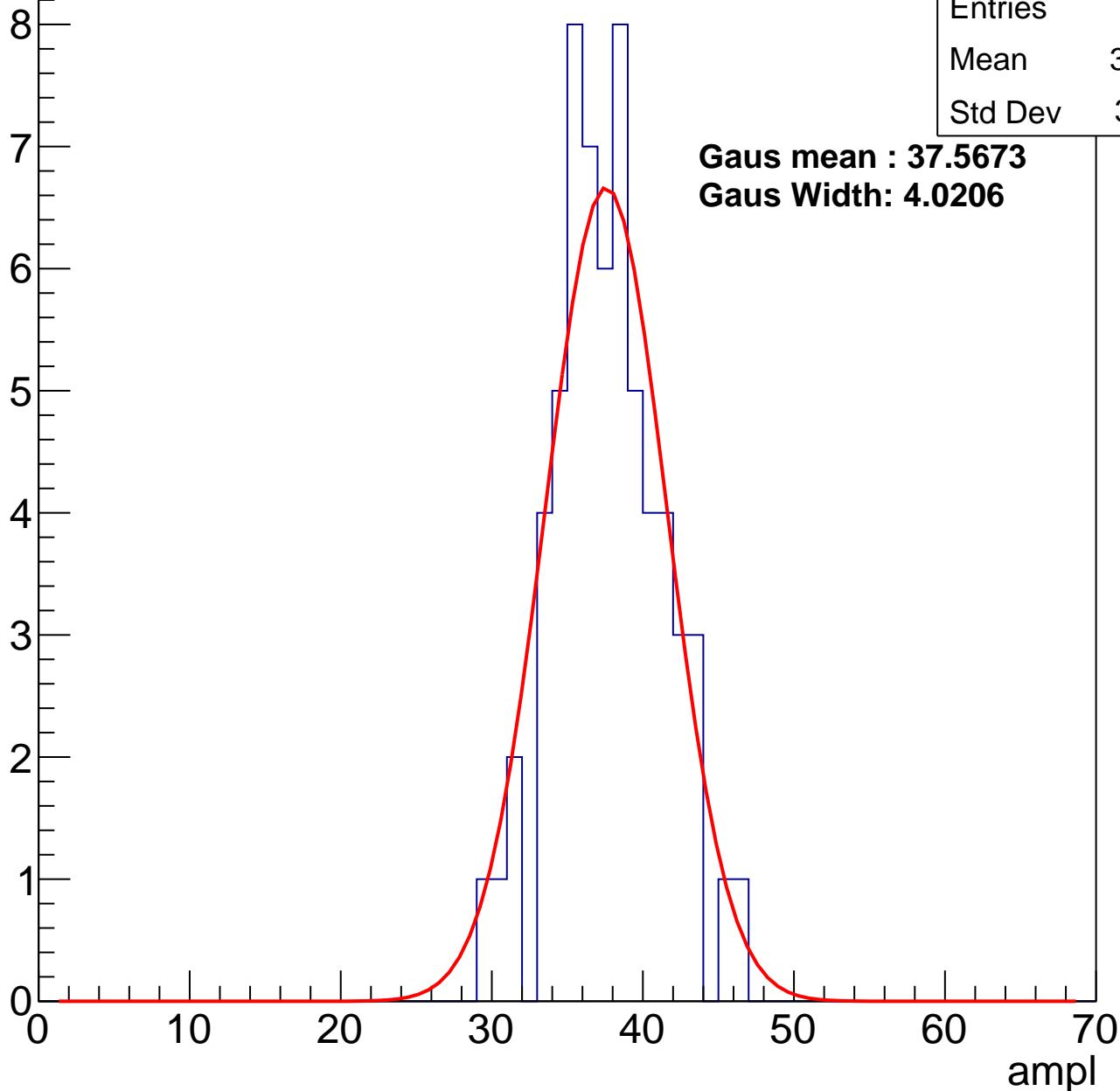
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	37.24
Std Dev	3.531

**Gaus mean : 37.5673**

**Gaus Width: 4.0206**



# B0L001S, U10-ch127, adc2

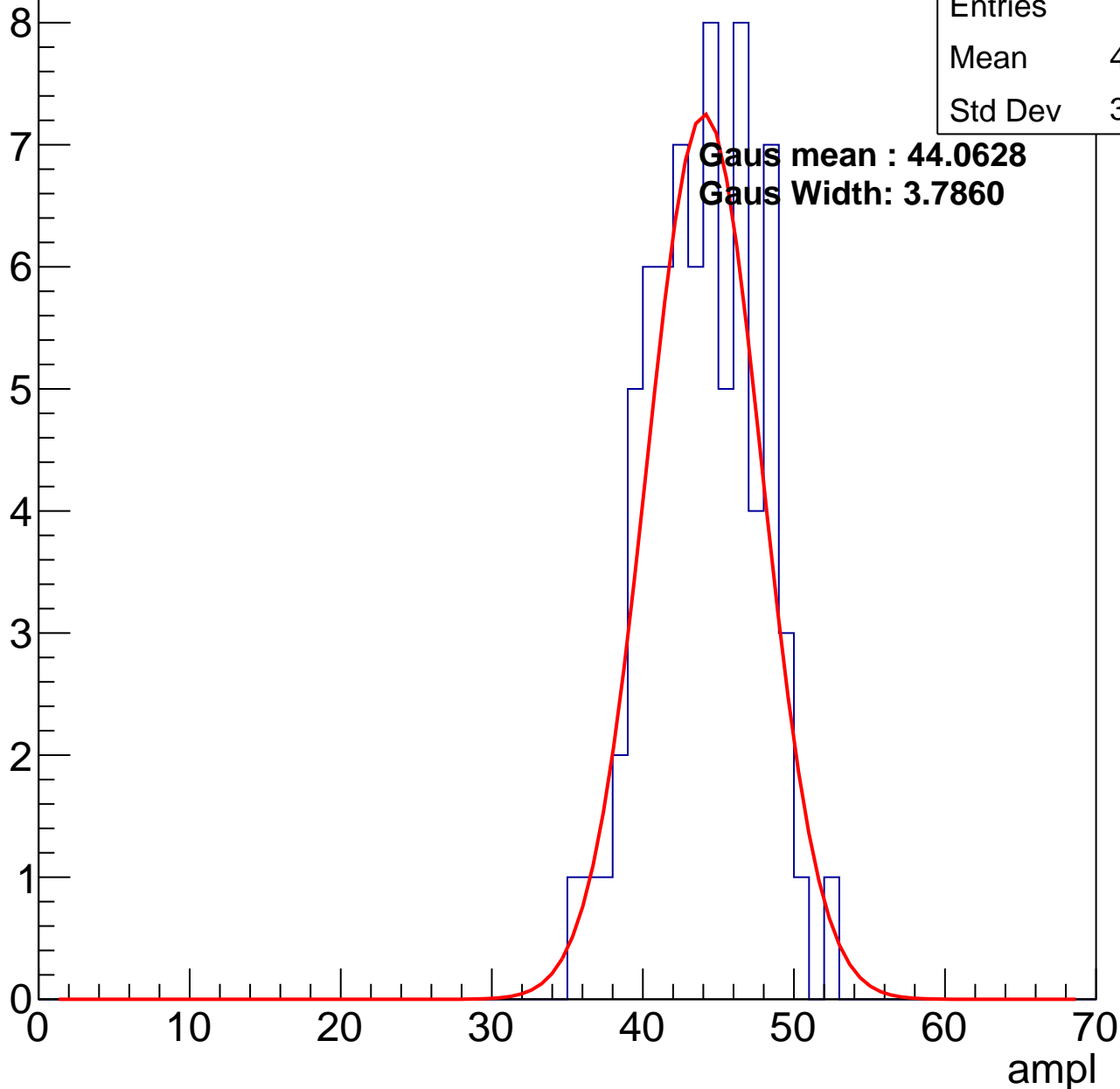
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	43.54
Std Dev	3.574

**Gaus mean : 44.0628**

**Gaus Width: 3.7860**



# B0L001S, U10-ch127, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

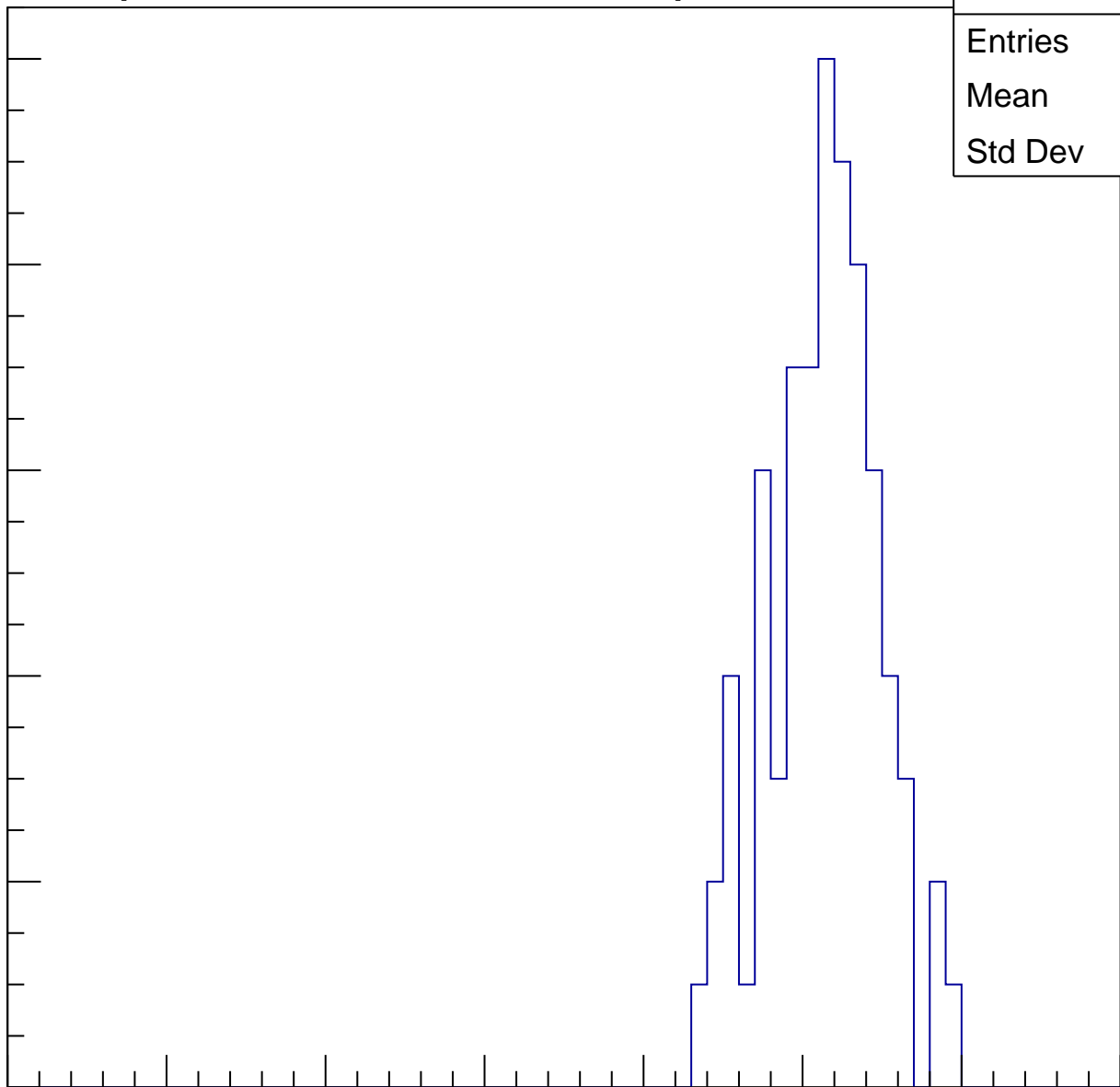
Entries	74
Mean	50.88
Std Dev	3.456

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

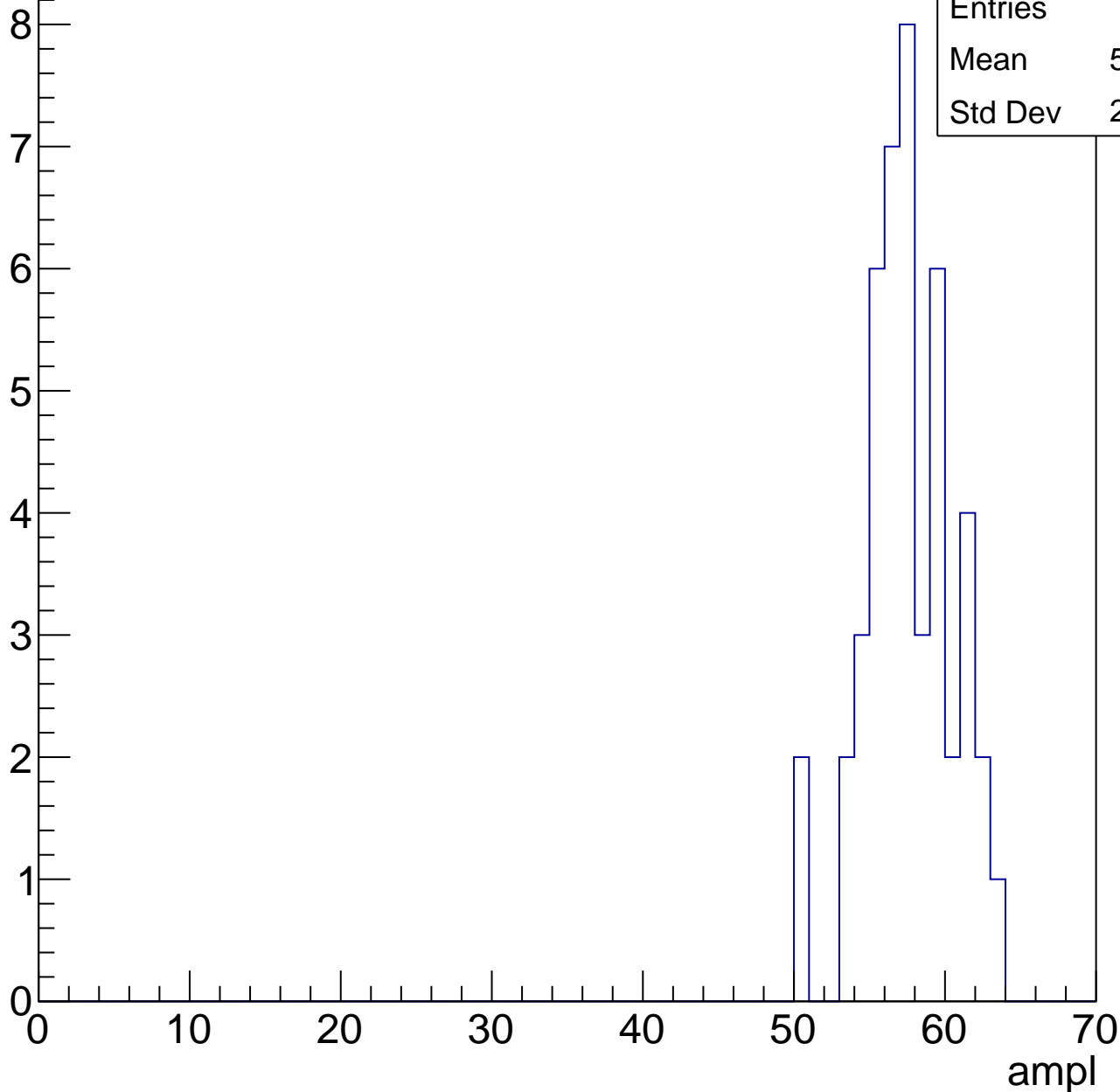


# B0L001S, U10-ch127, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	46
Mean	57.07
Std Dev	2.885

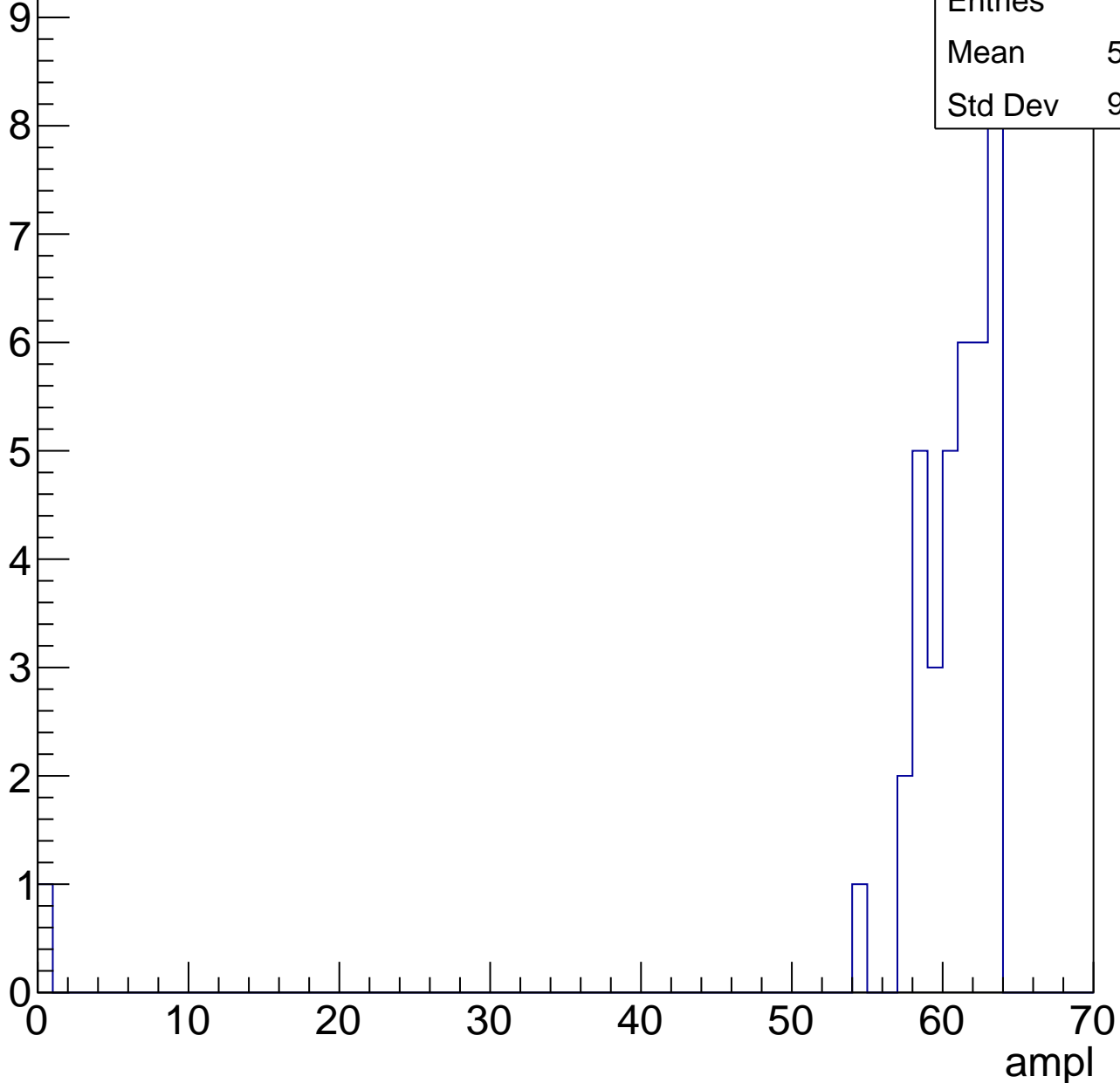


# B0L001S, U10-ch127, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

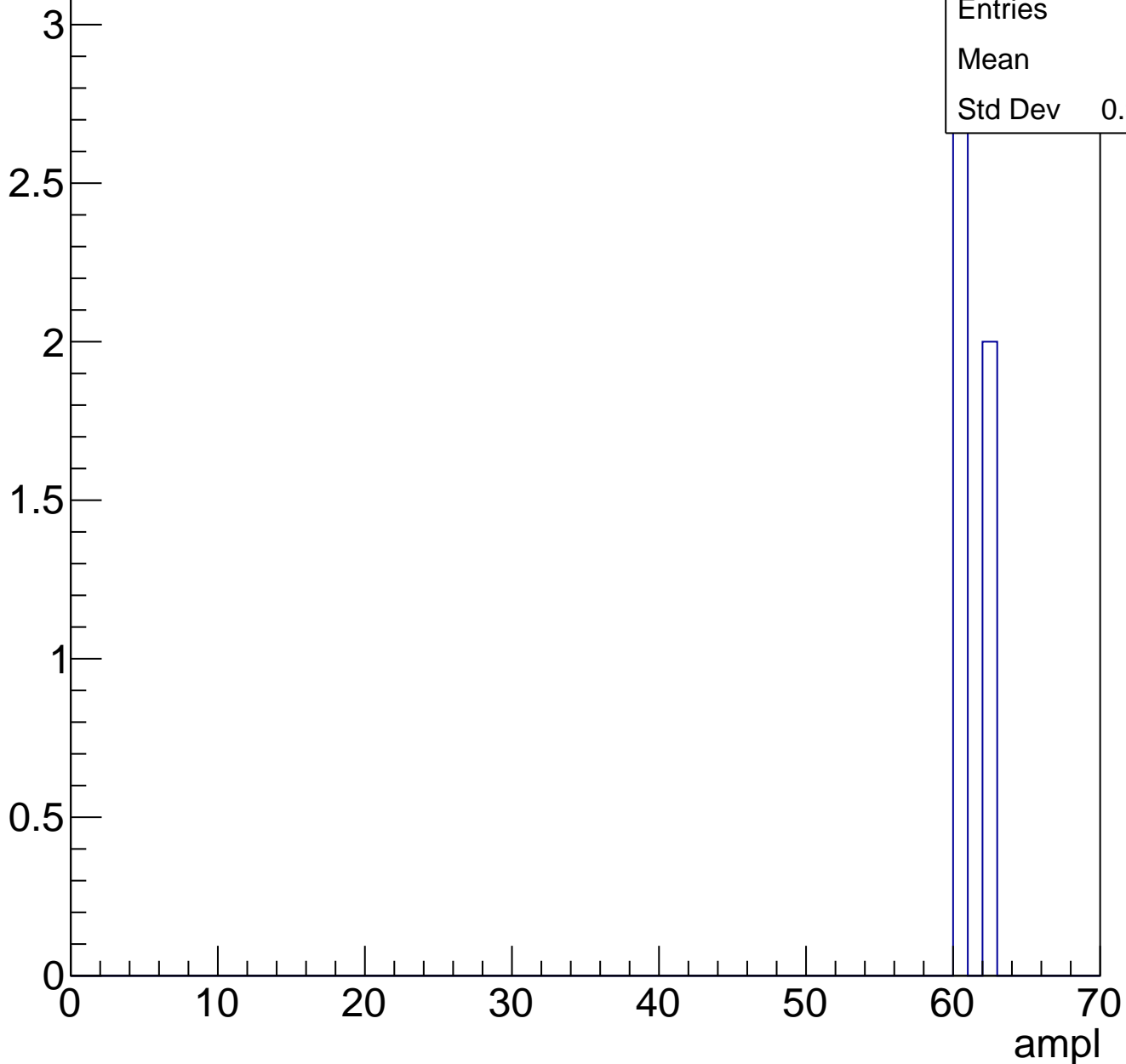
Entries	38
Mean	58.95
Std Dev	9.929



# B0L001S, U10-ch127, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	5
Mean	60.8
Std Dev	0.9798



# B0L001S, U10-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

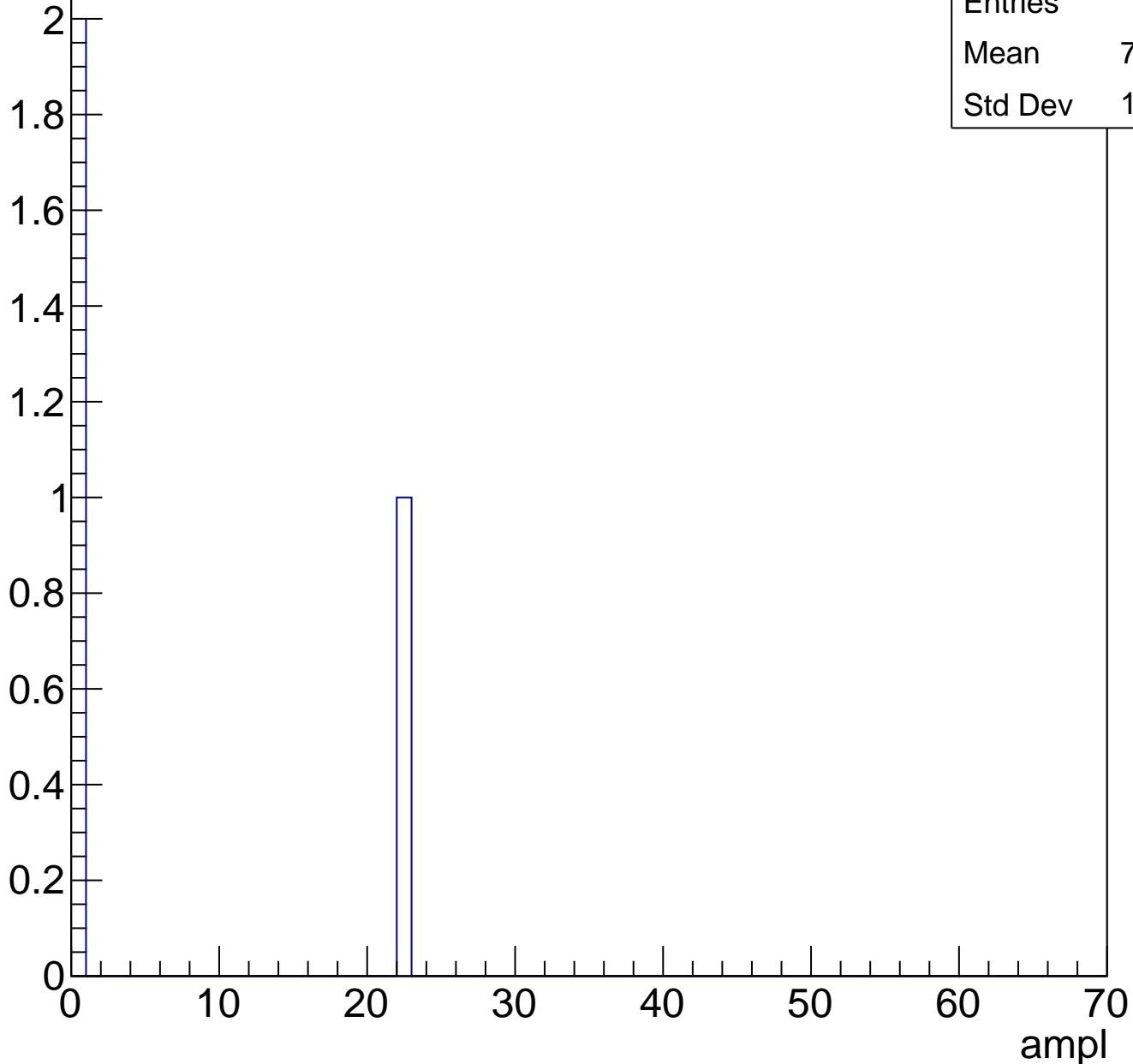


Entries	3
Mean	7.333
Std Dev	10.37

# B0L001S, U10-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	3
Mean	7.333
Std Dev	10.37