

B1L103S, U10-ch0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	455
Mean	38.25
Std Dev	17.72

Turn on : 23.9823

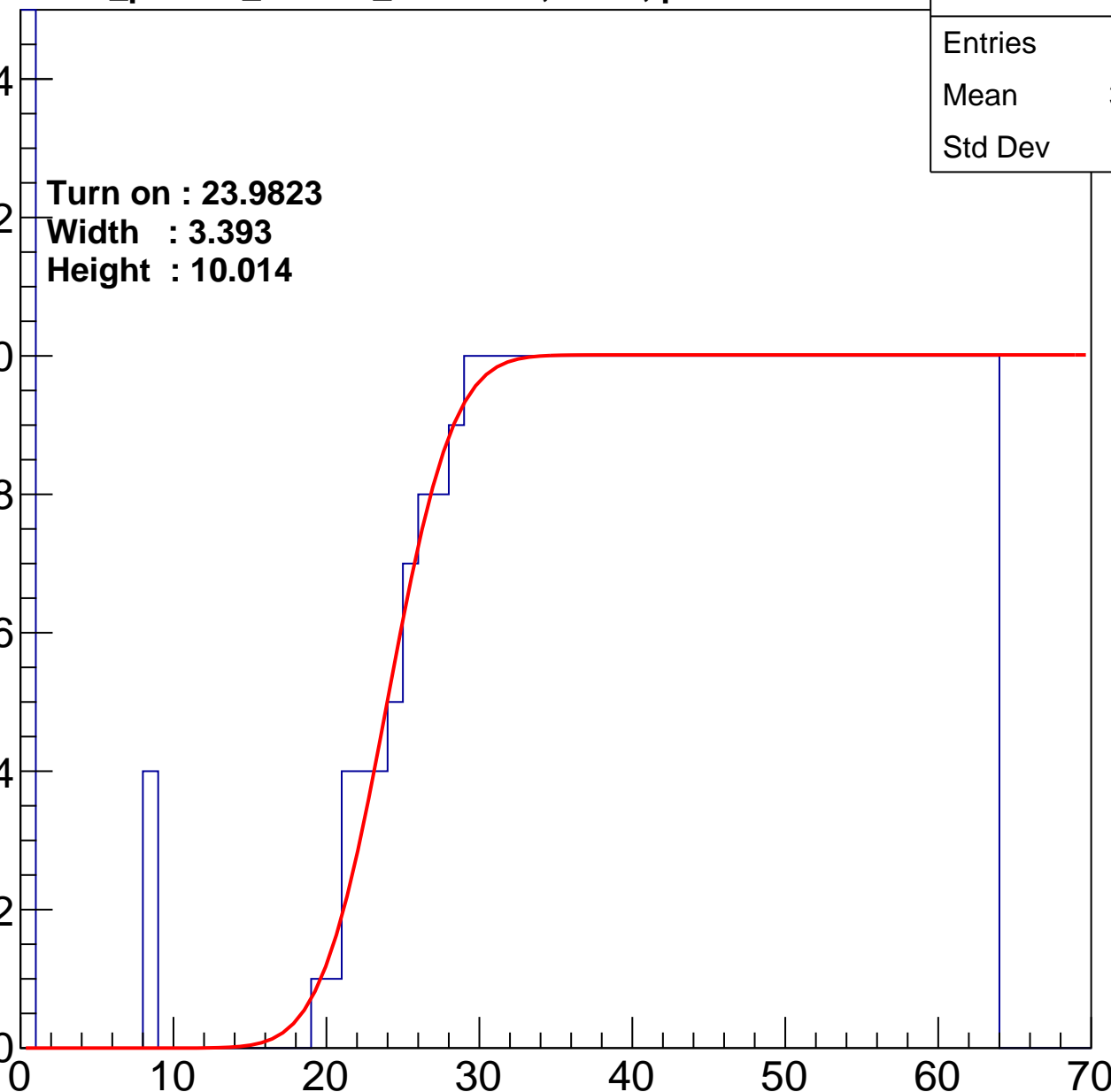
Width : 3.393

Height : 10.014

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	430
Mean	39.95
Std Dev	16.56

Turn on : 25.0768

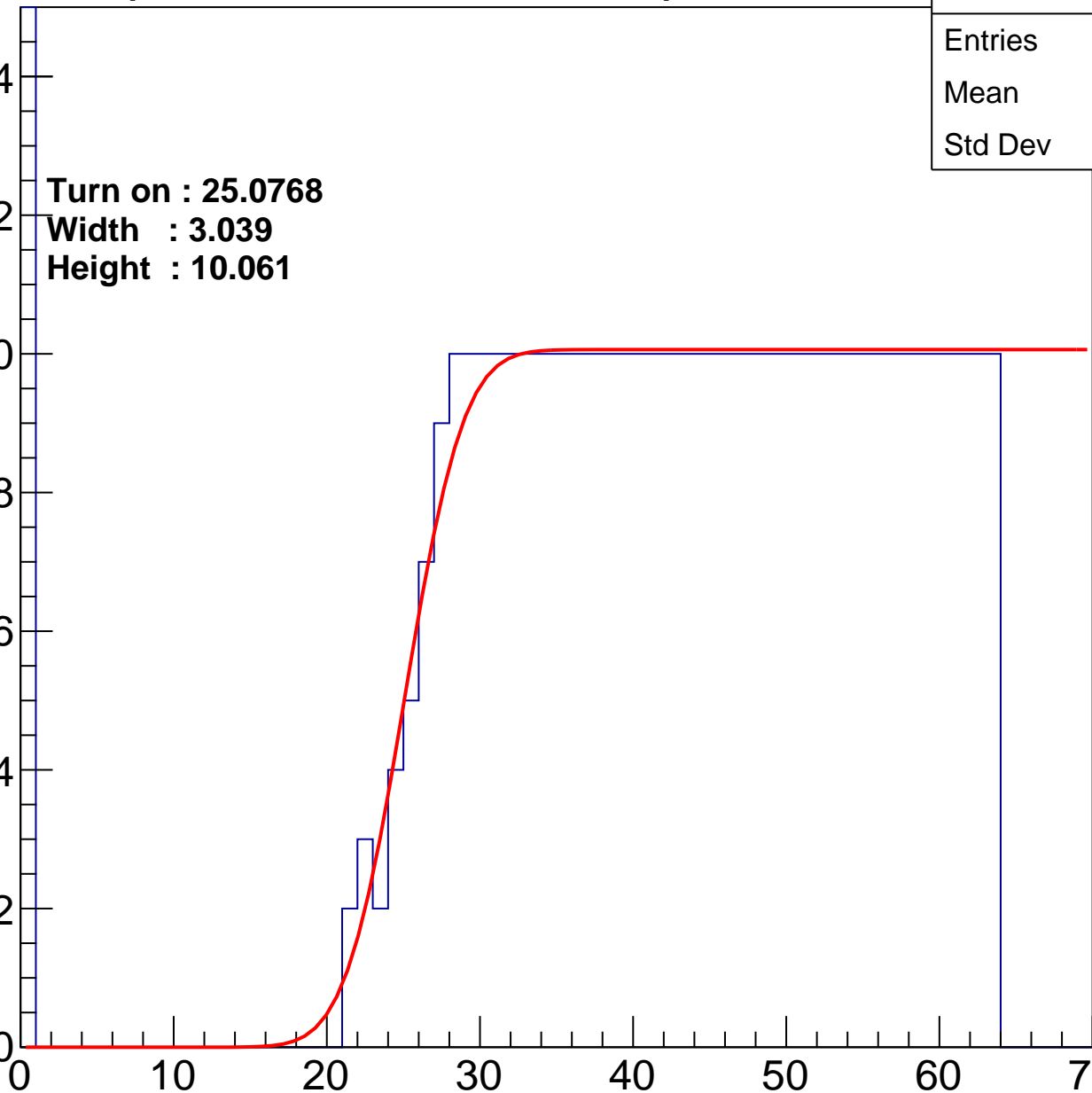
Width : 3.039

Height : 10.061

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	443
Mean	39.49
Std Dev	16.5

Turn on : 23.4440

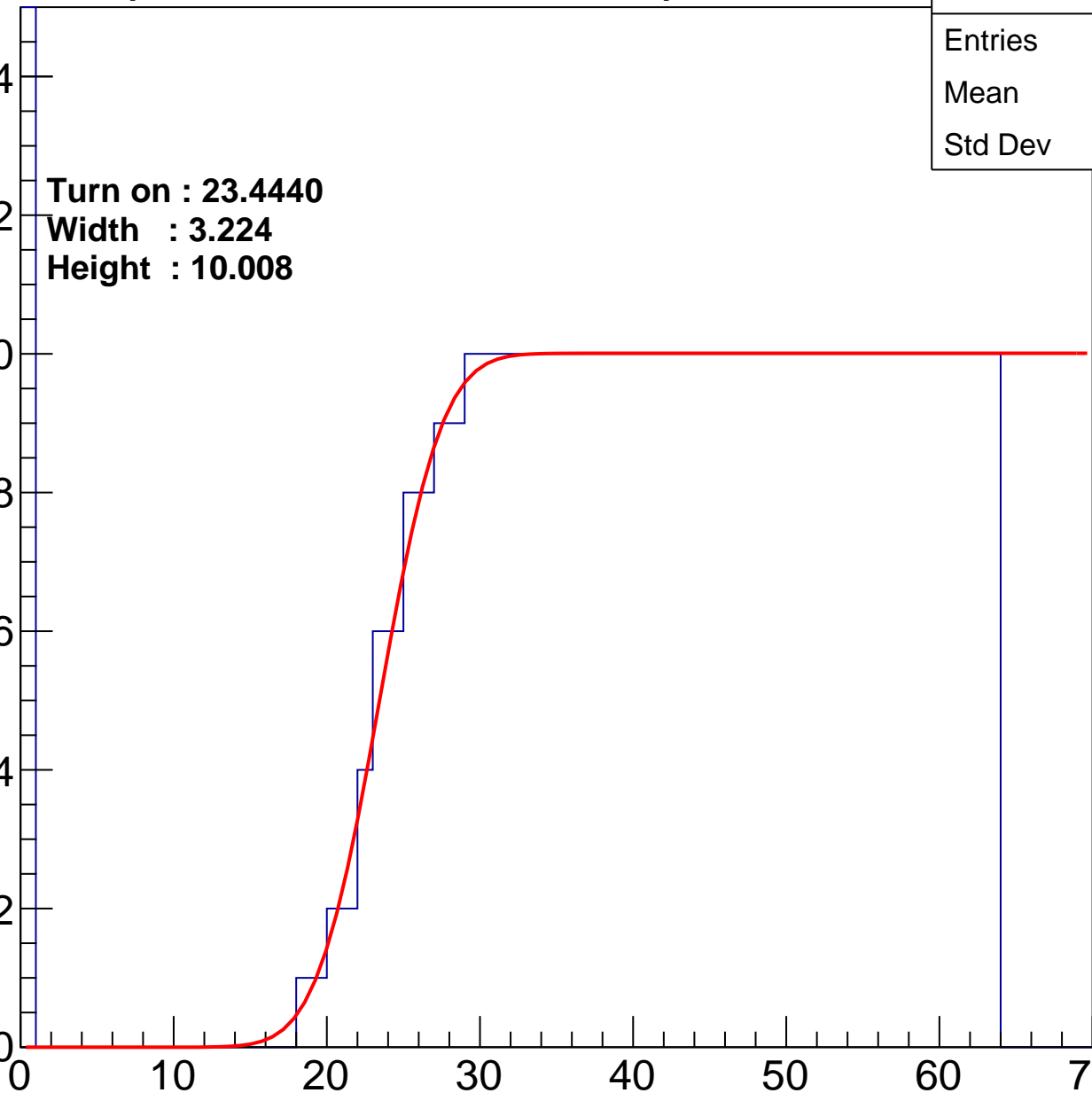
Width : 3.224

Height : 10.008

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	426
Mean	39.35
Std Dev	17.71

Turn on : 26.6097

Width : 2.886

Height : 10.012

Entry

14

12

10

8

6

4

2

0

0

10

20

30

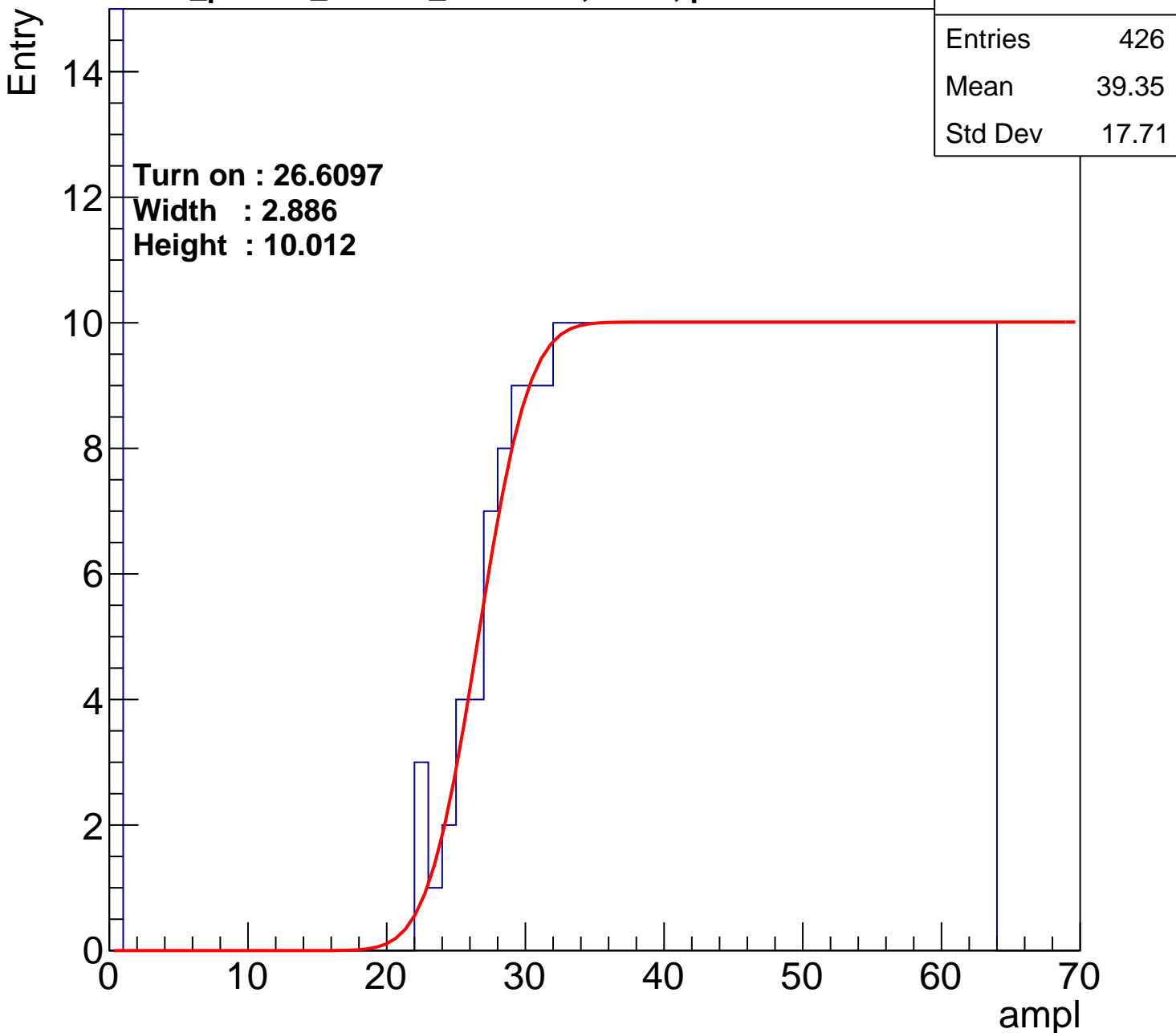
40

50

60

70

ampl



B1L103S, U10-ch4

calib_packv5_041523_1651.root, FC#0, port C2

Entries	416
Mean	40.15
Std Dev	17.1

Turn on : 27.1021

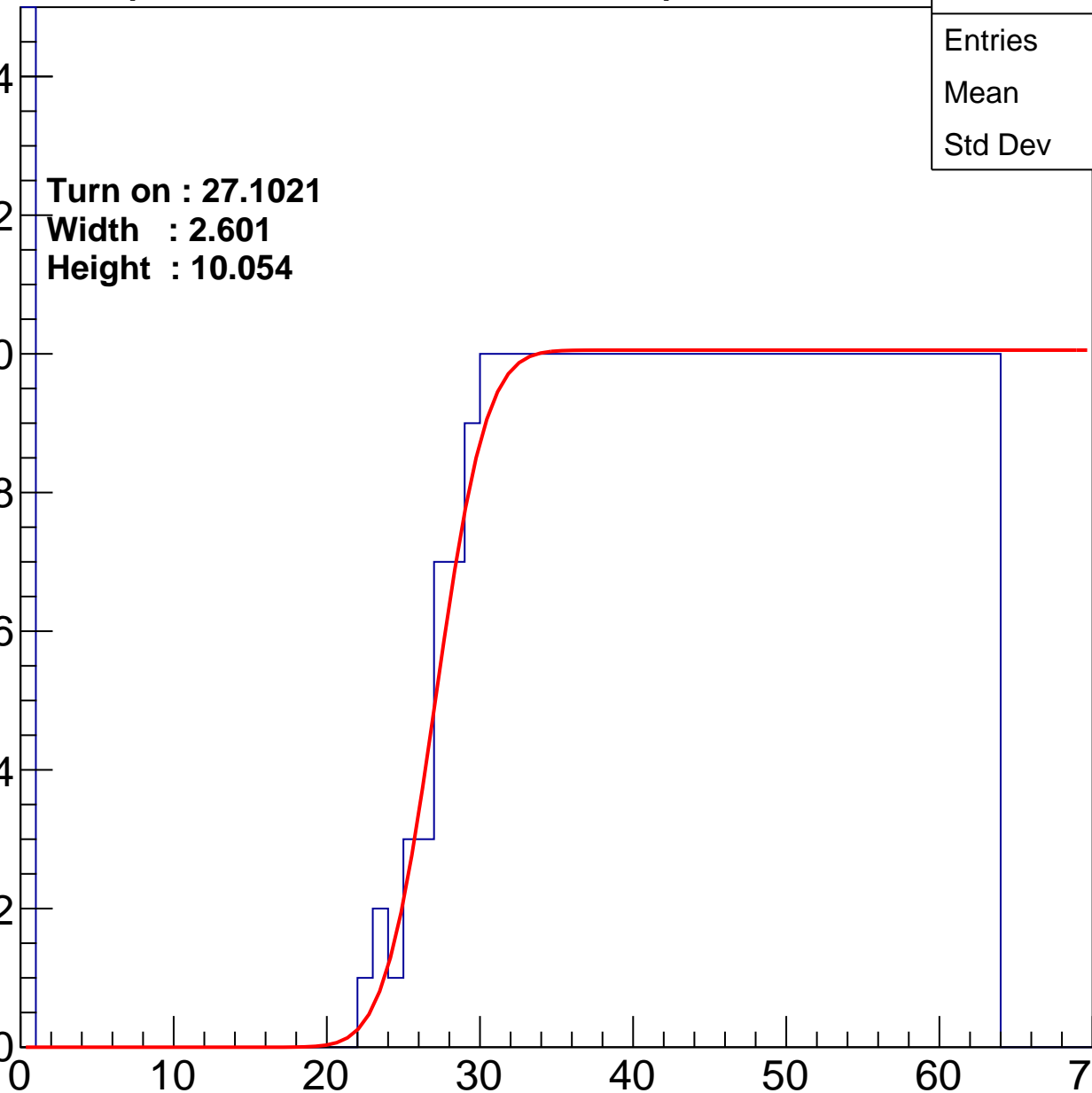
Width : 2.601

Height : 10.054

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch5

calib_packv5_041523_1651.root, FC#0, port C2

Entries	431
Mean	40.23
Std Dev	16

Turn on : 24.0826

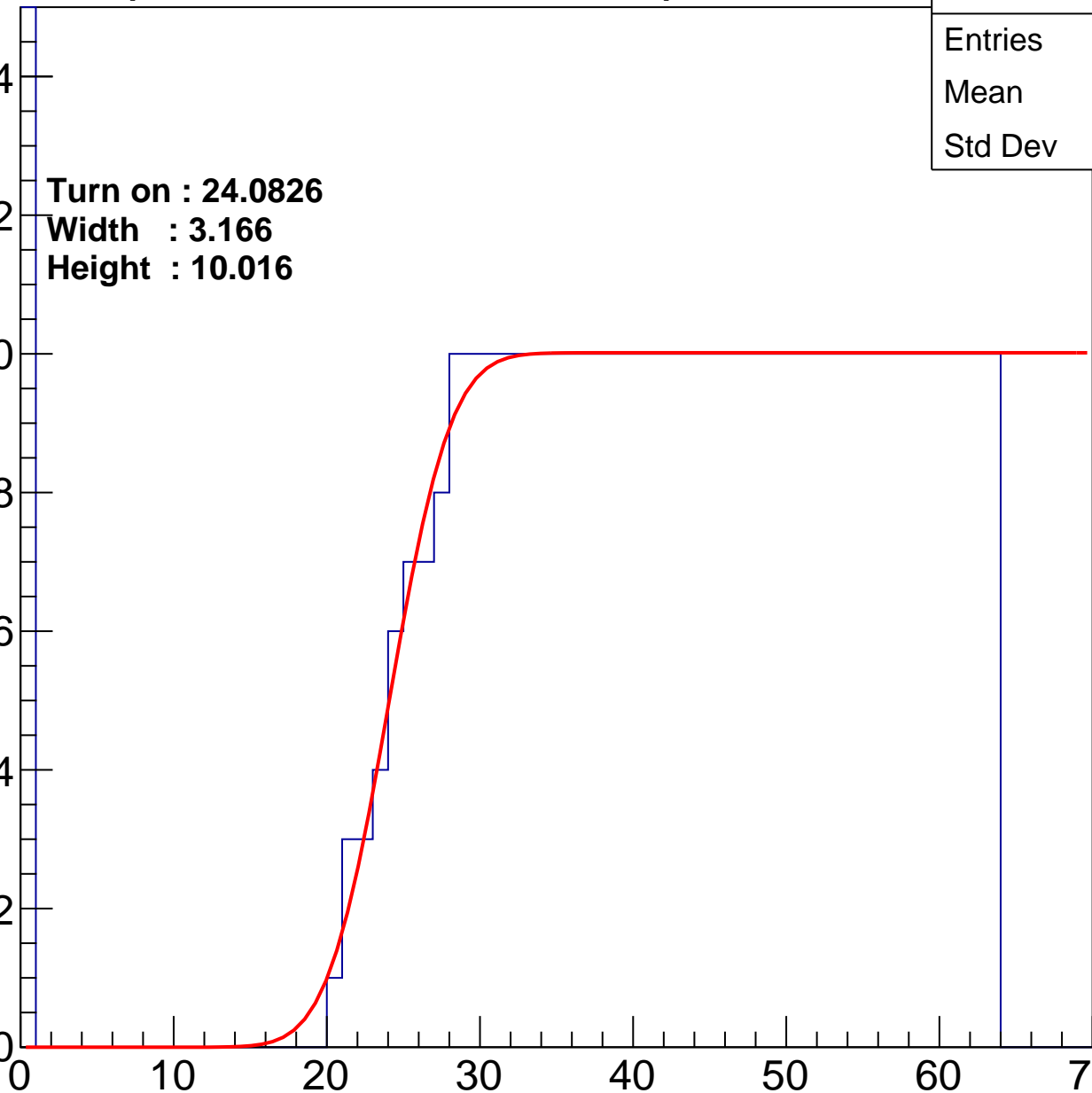
Width : 3.166

Height : 10.016

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch6

calib_packv5_041523_1651.root, FC#0, port C2

Entries	424
Mean	39.81
Std Dev	17.1

Turn on : 26.1054

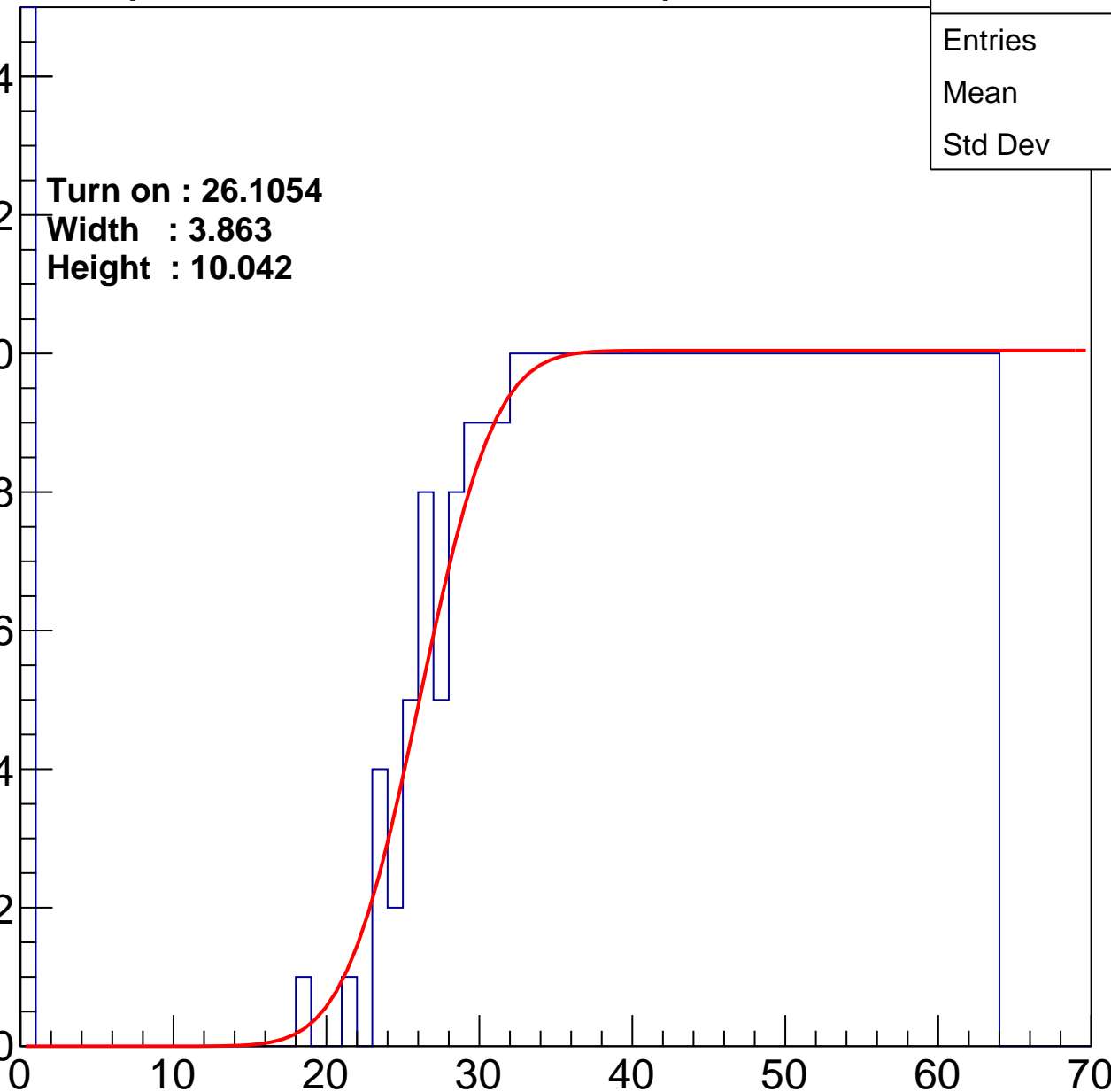
Width : 3.863

Height : 10.042

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	428
Mean	38.42
Std Dev	18.9

Turn on : 27.5378

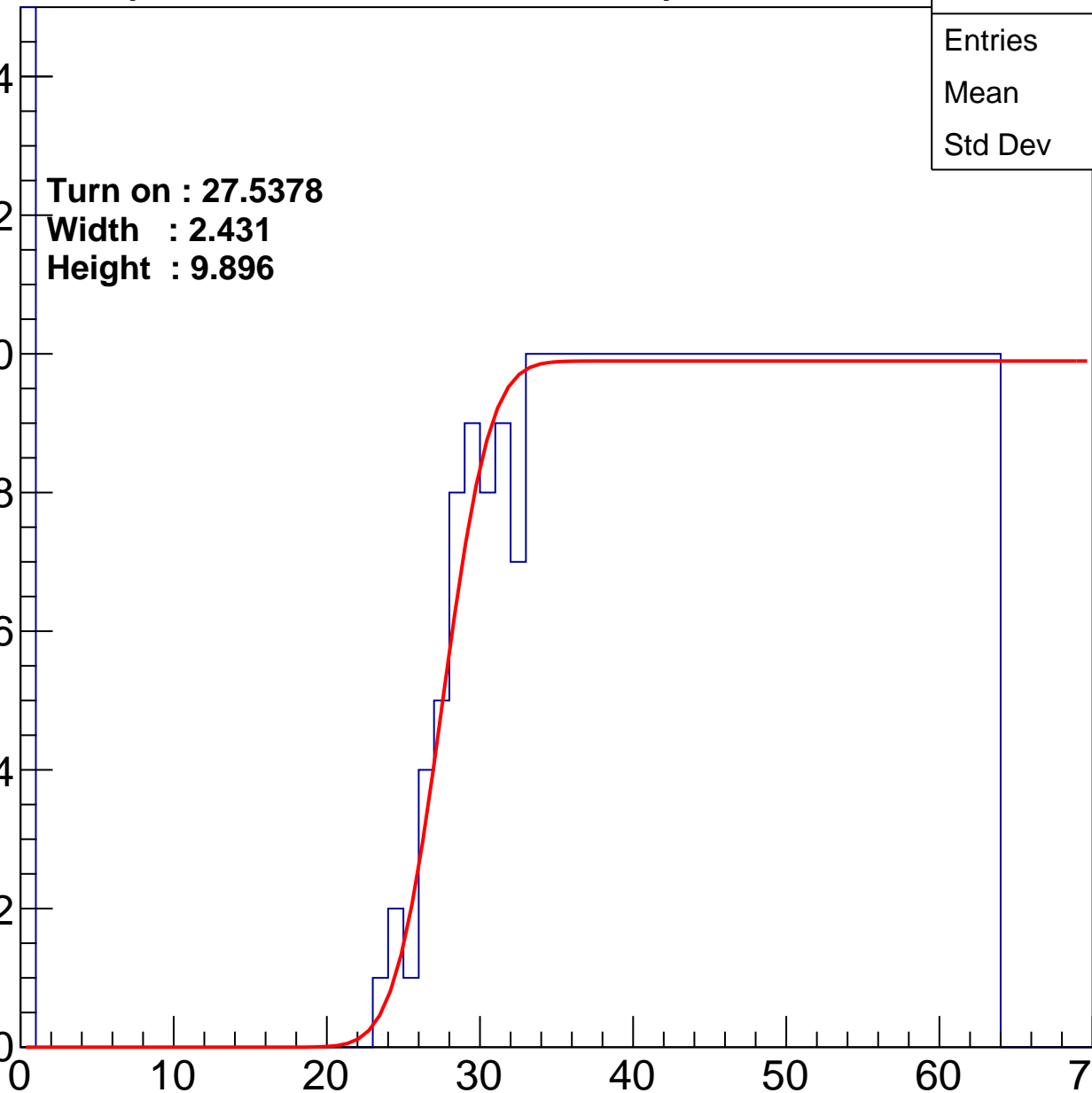
Width : 2.431

Height : 9.896

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch8

calib_packv5_041523_1651.root, FC#0, port C2

Entries	419
Mean	40.38
Std Dev	16.5

Turn on : 25.7803

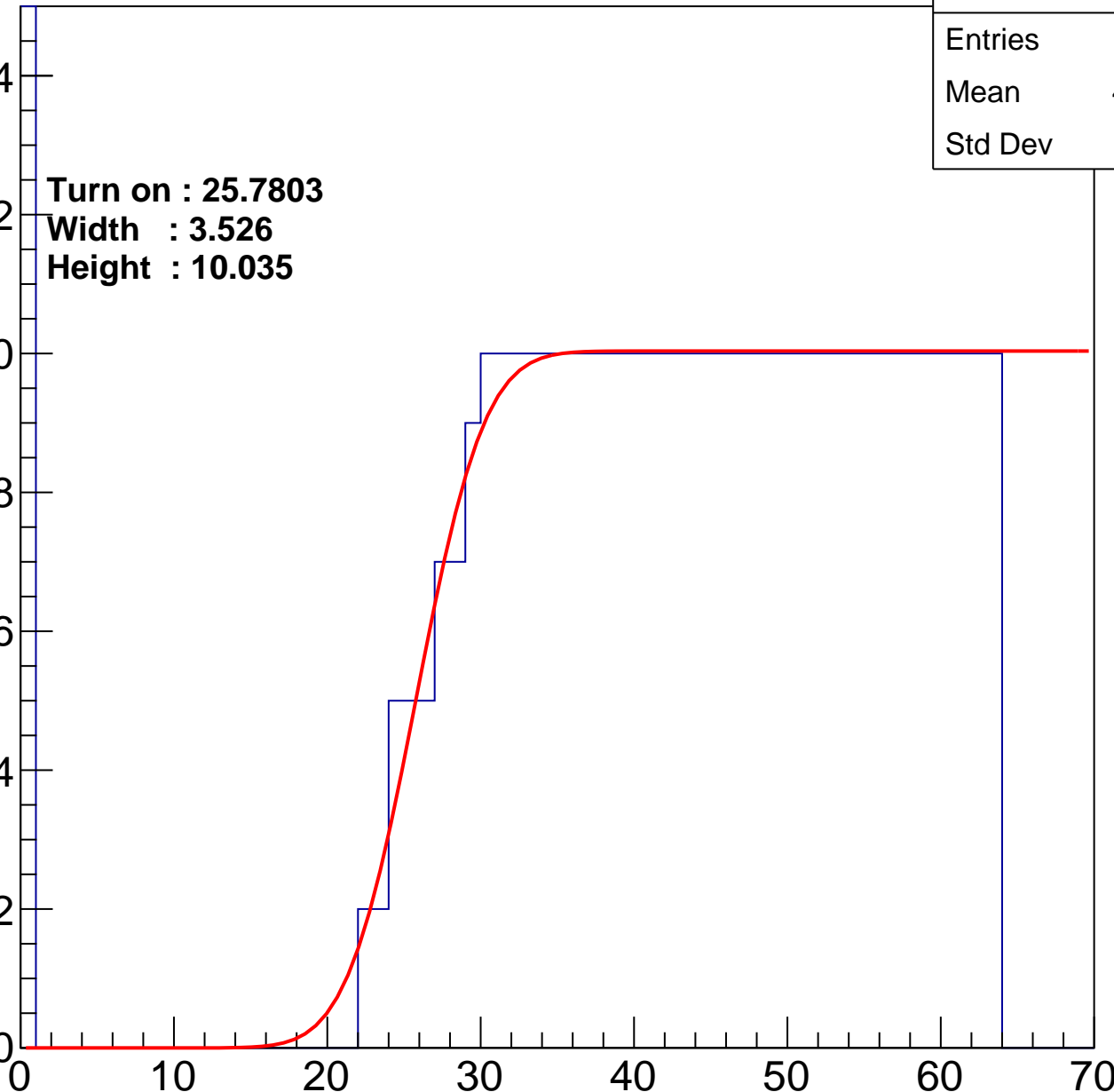
Width : 3.526

Height : 10.035

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch9

calib_packv5_041523_1651.root, FC#0, port C2

Entries	410
Mean	41.1
Std Dev	15.86

Turn on : 25.9949

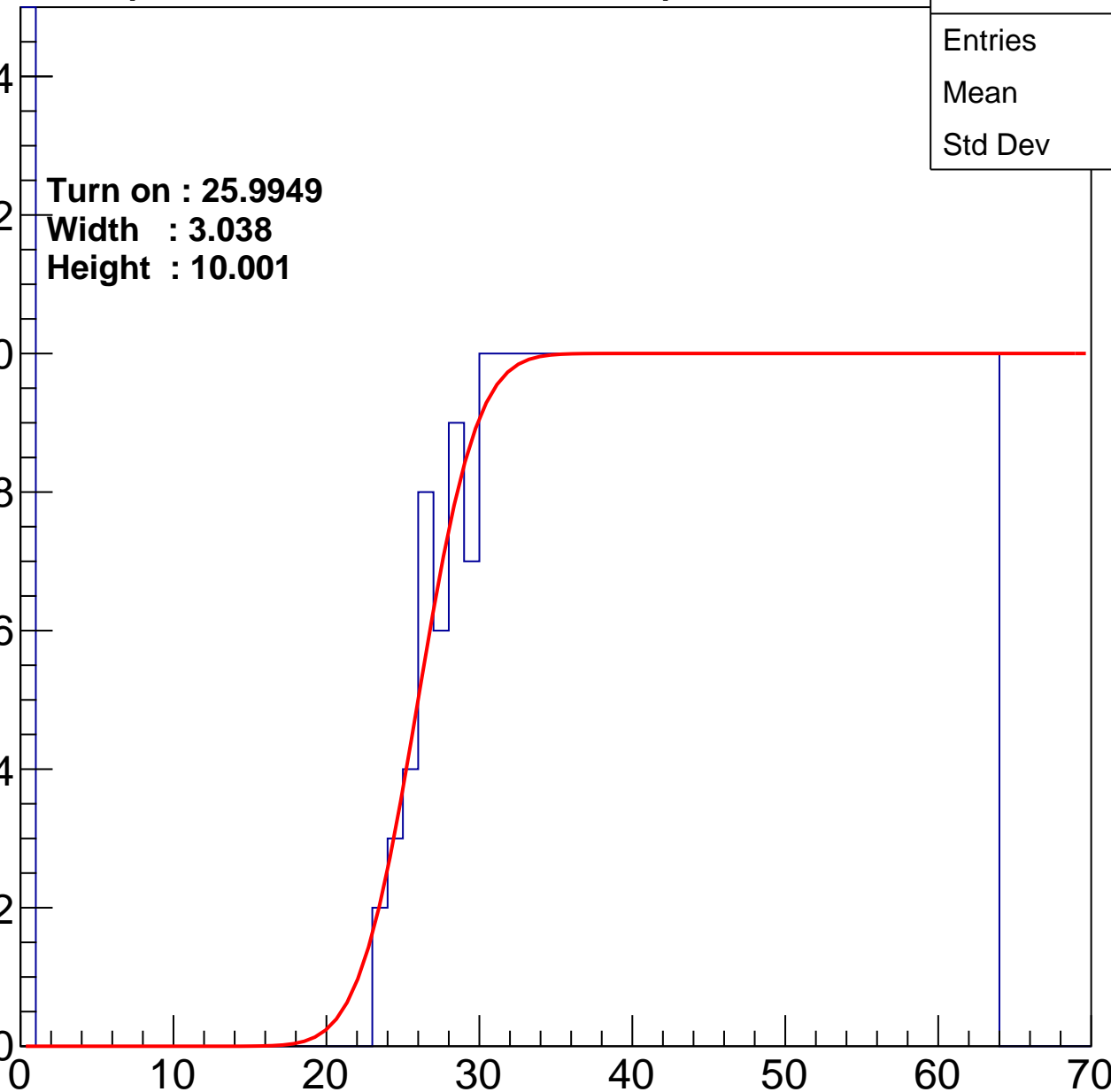
Width : 3.038

Height : 10.001

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch10

calib_packv5_041523_1651.root, FC#0, port C2

Entries	436
Mean	39.91
Std Dev	16.25

Turn on : 23.9822

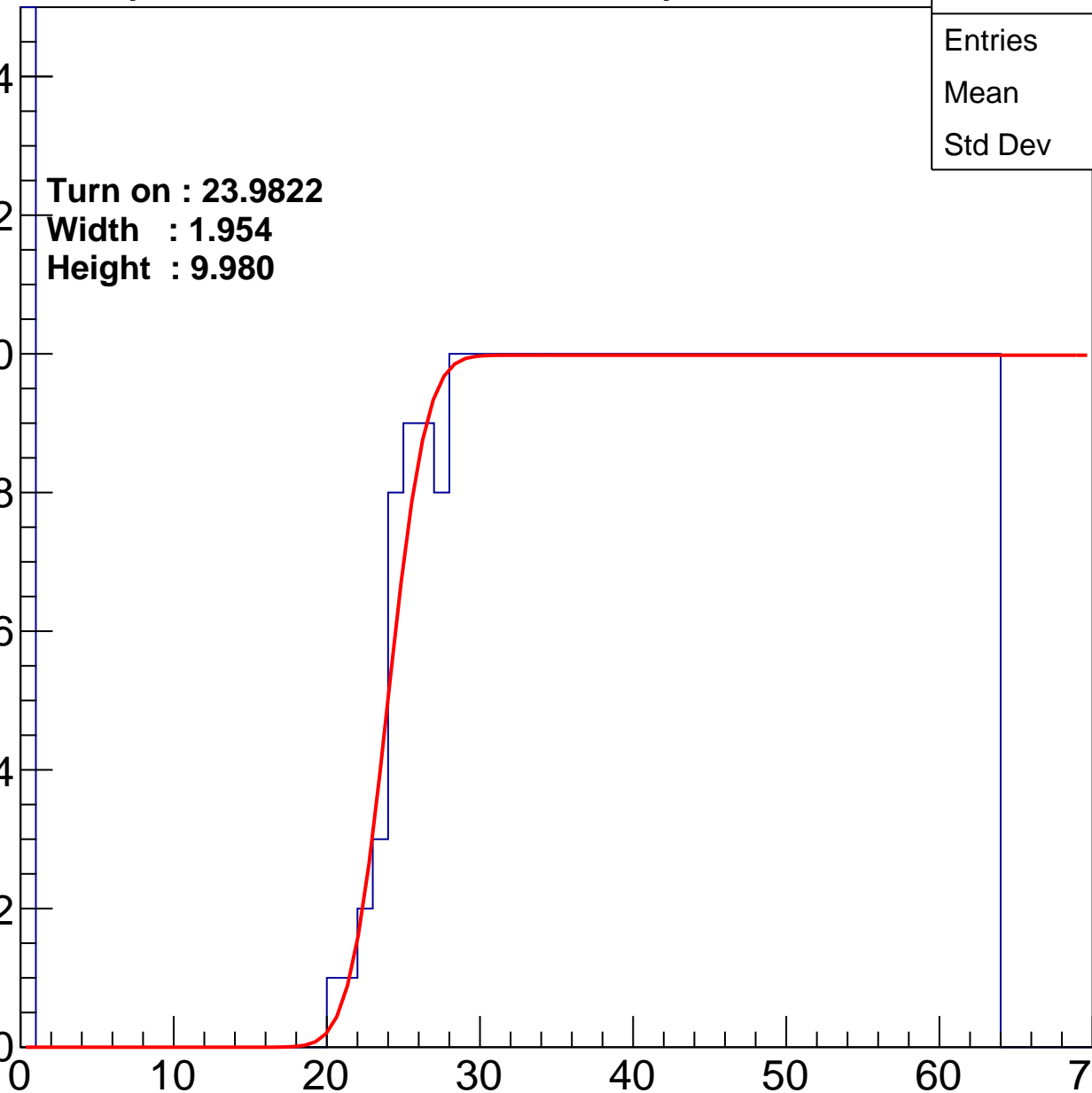
Width : 1.954

Height : 9.980

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch11

calib_packv5_041523_1651.root, FC#0, port C2

Entries	420
Mean	40.12
Std Dev	16.89

Turn on : 26.6243

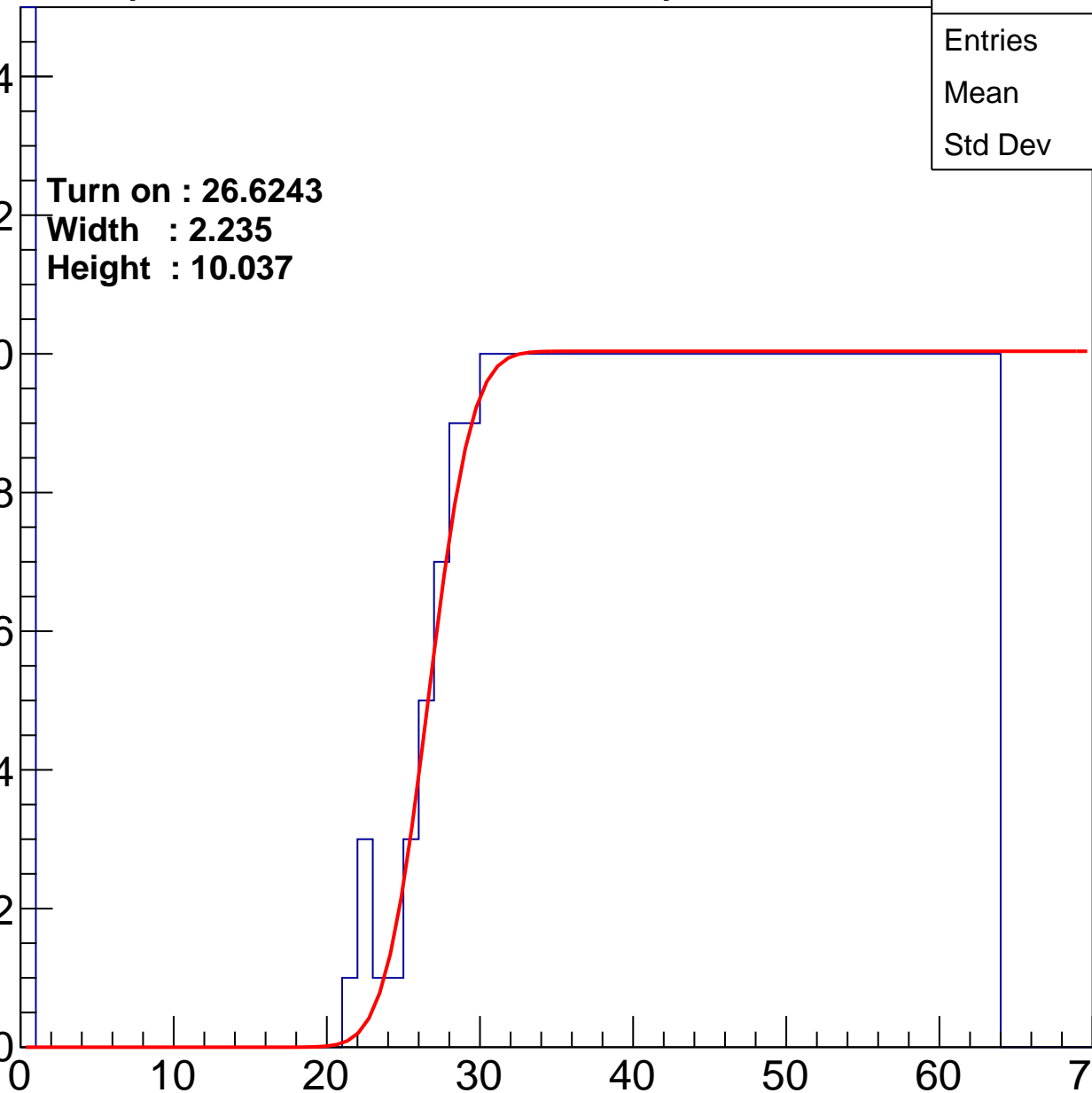
Width : 2.235

Height : 10.037

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch12

calib_packv5_041523_1651.root, FC#0, port C2

Entries	415
Mean	40.24
Std Dev	17

Turn on : 26.8082

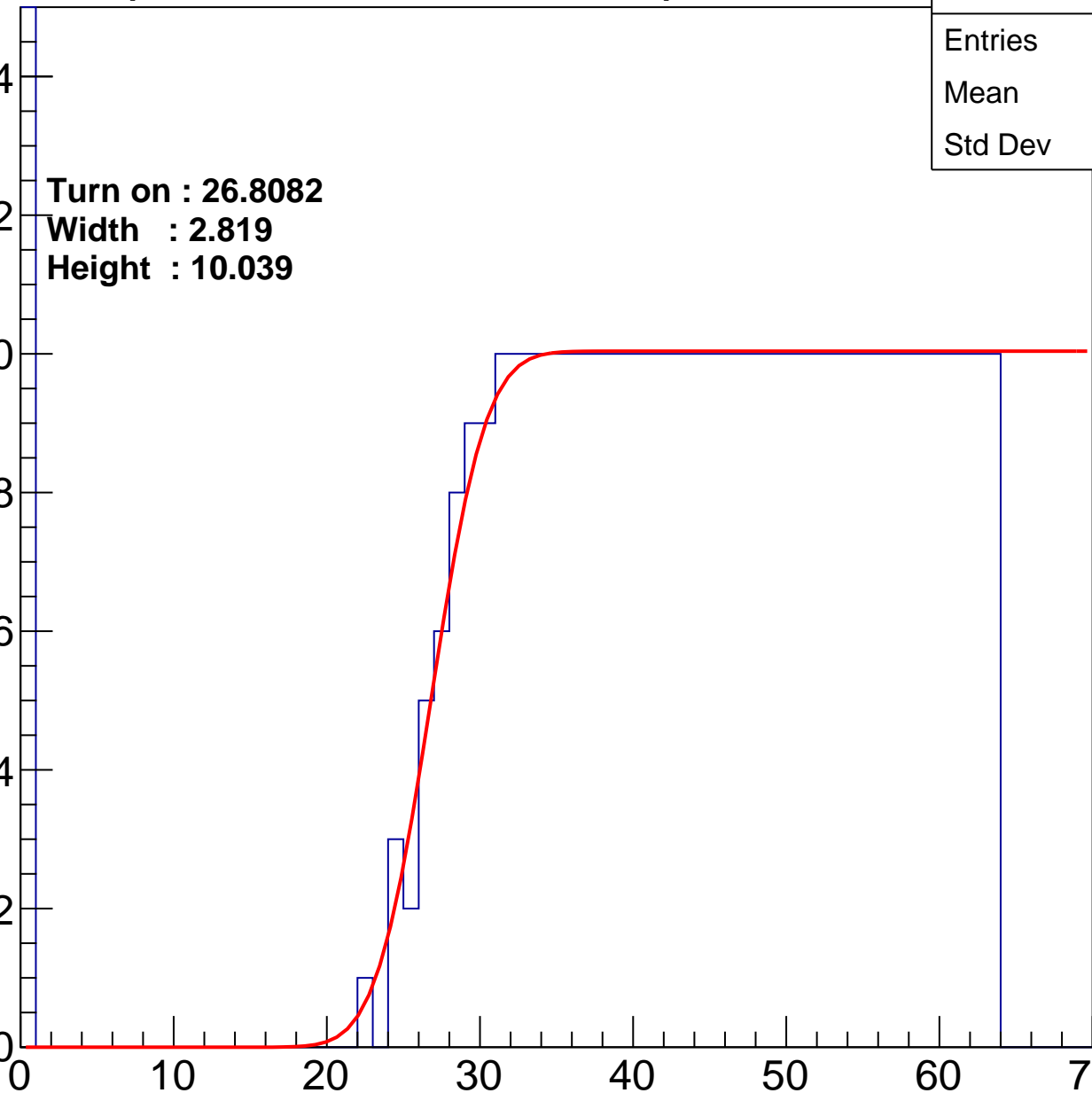
Width : 2.819

Height : 10.039

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch13

calib_packv5_041523_1651.root, FC#0, port C2

Entries	408
Mean	40.6
Std Dev	16.84

Turn on : 27.4506

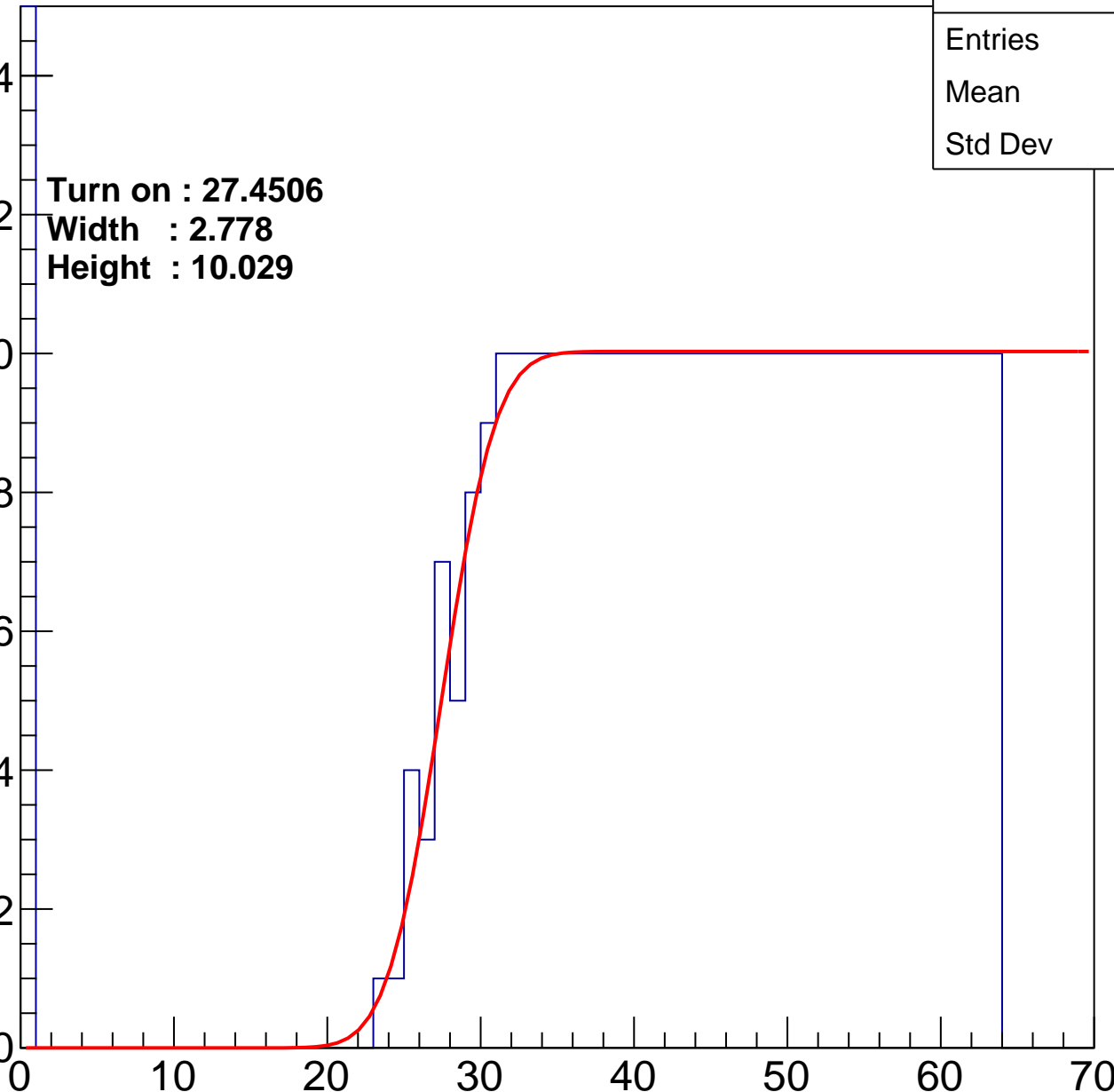
Width : 2.778

Height : 10.029

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch14

calib_packv5_041523_1651.root, FC#0, port C2

Entries	416
Mean	40.68
Std Dev	16.2

Turn on : 26.3784

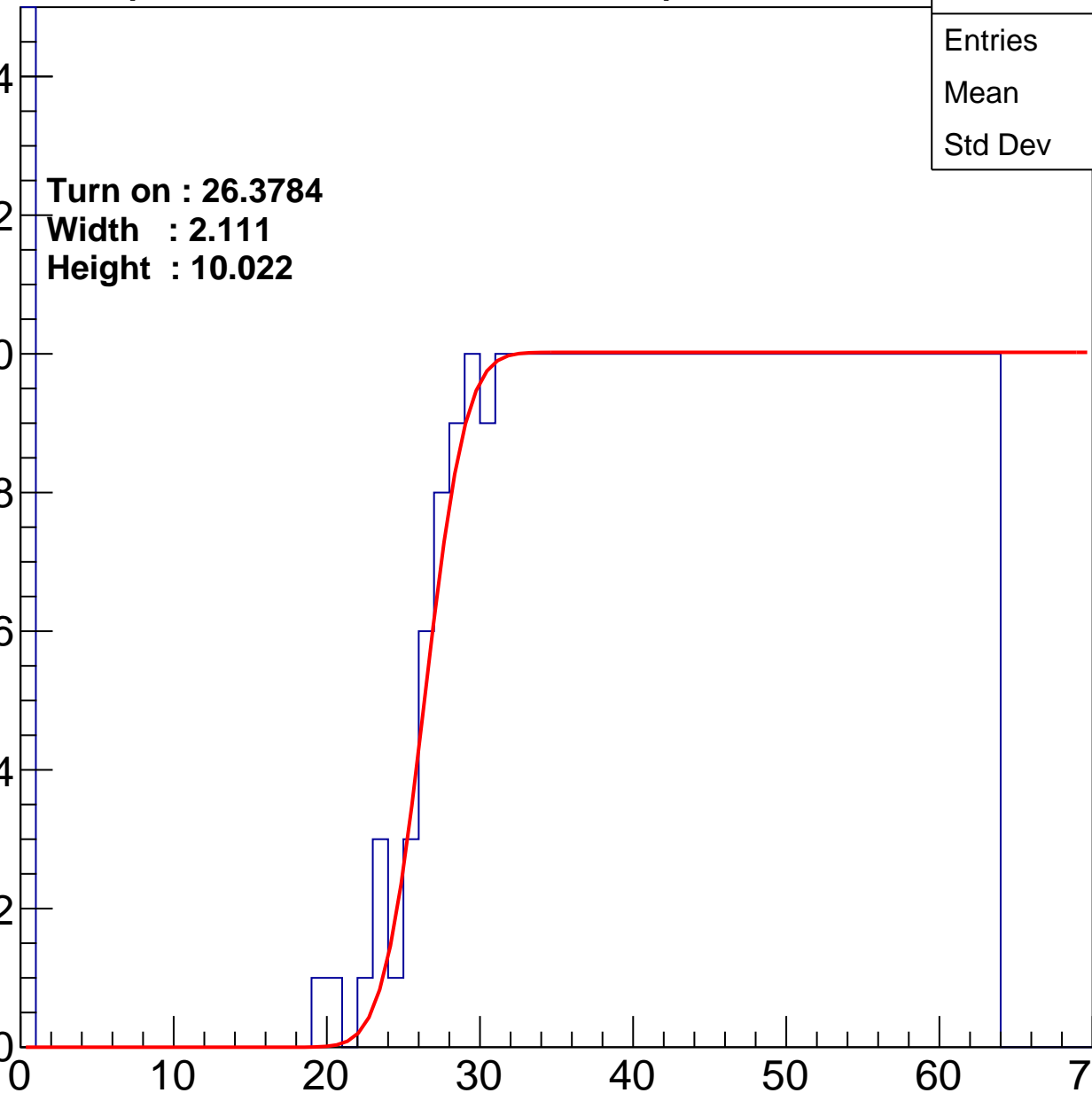
Width : 2.111

Height : 10.022

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch15

calib_packv5_041523_1651.root, FC#0, port C2

Entries	389
Mean	42.16
Std Dev	15.4

Turn on : 27.8301

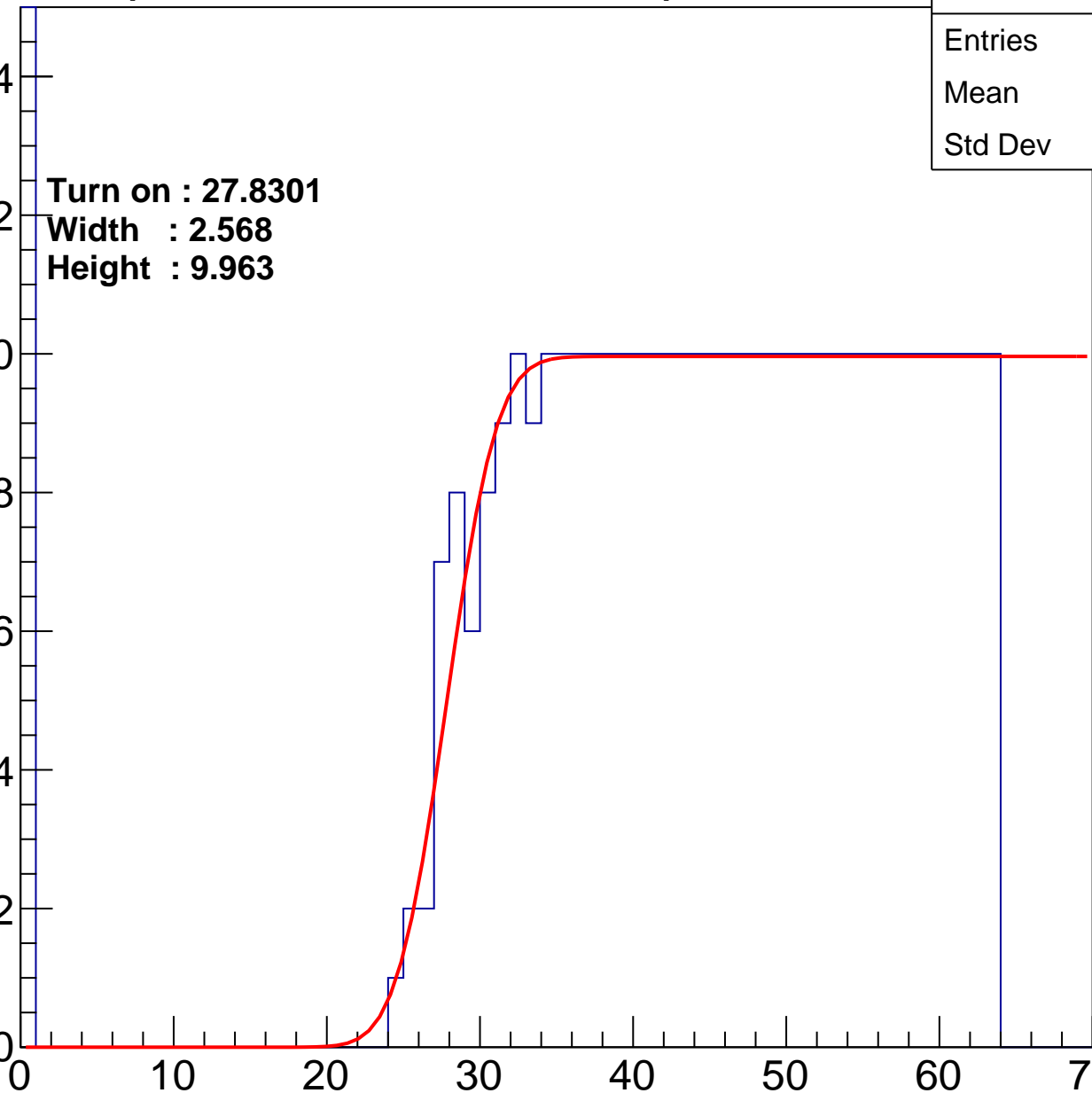
Width : 2.568

Height : 9.963

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch16

calib_packv5_041523_1651.root, FC#0, port C2

Entries	425
Mean	39.39
Std Dev	17.76

Turn on : 26.9660

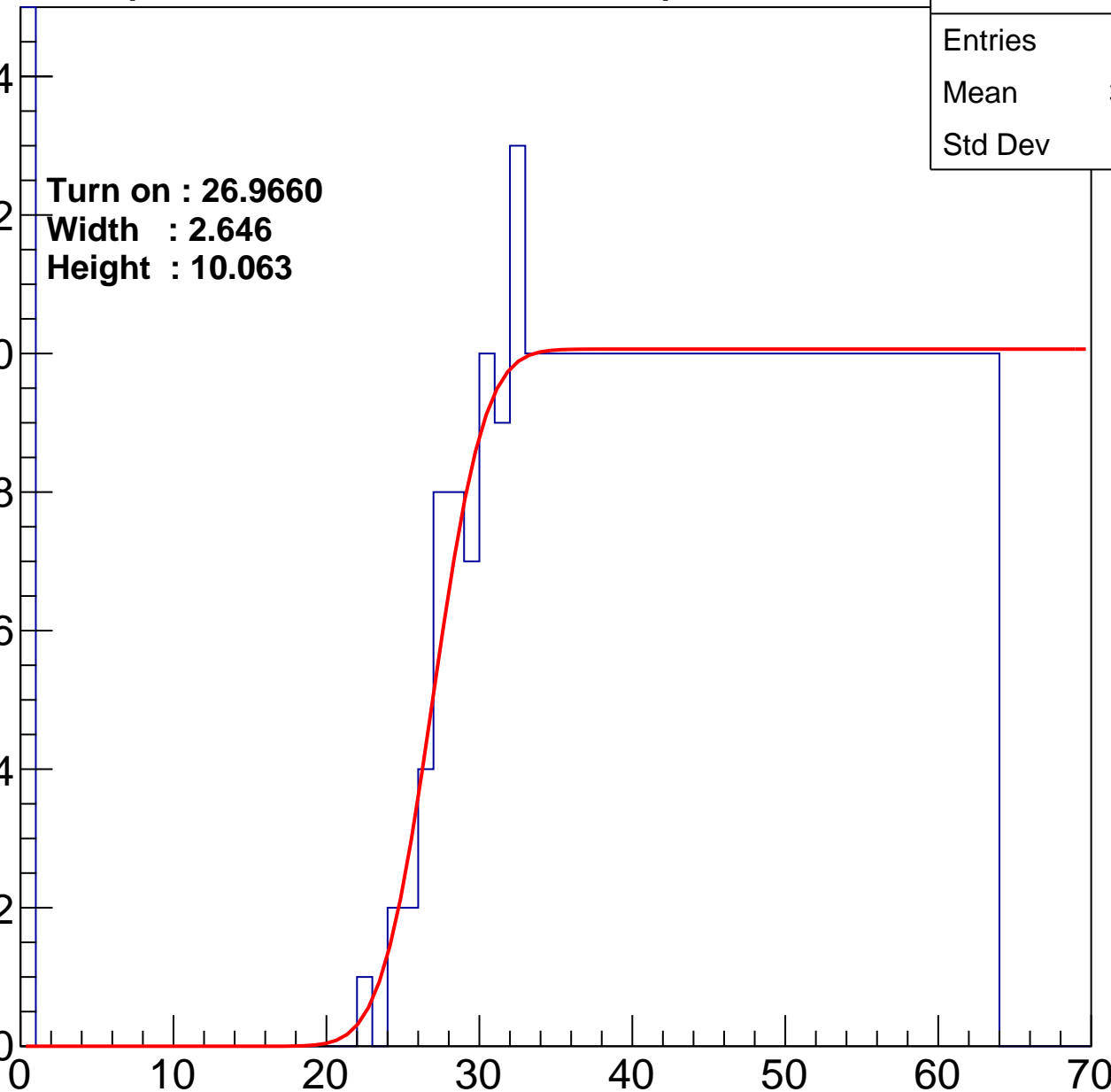
Width : 2.646

Height : 10.063

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch17

calib_packv5_041523_1651.root, FC#0, port C2

Entries	413
Mean	39.88
Std Dev	17.64

Turn on : 27.9962

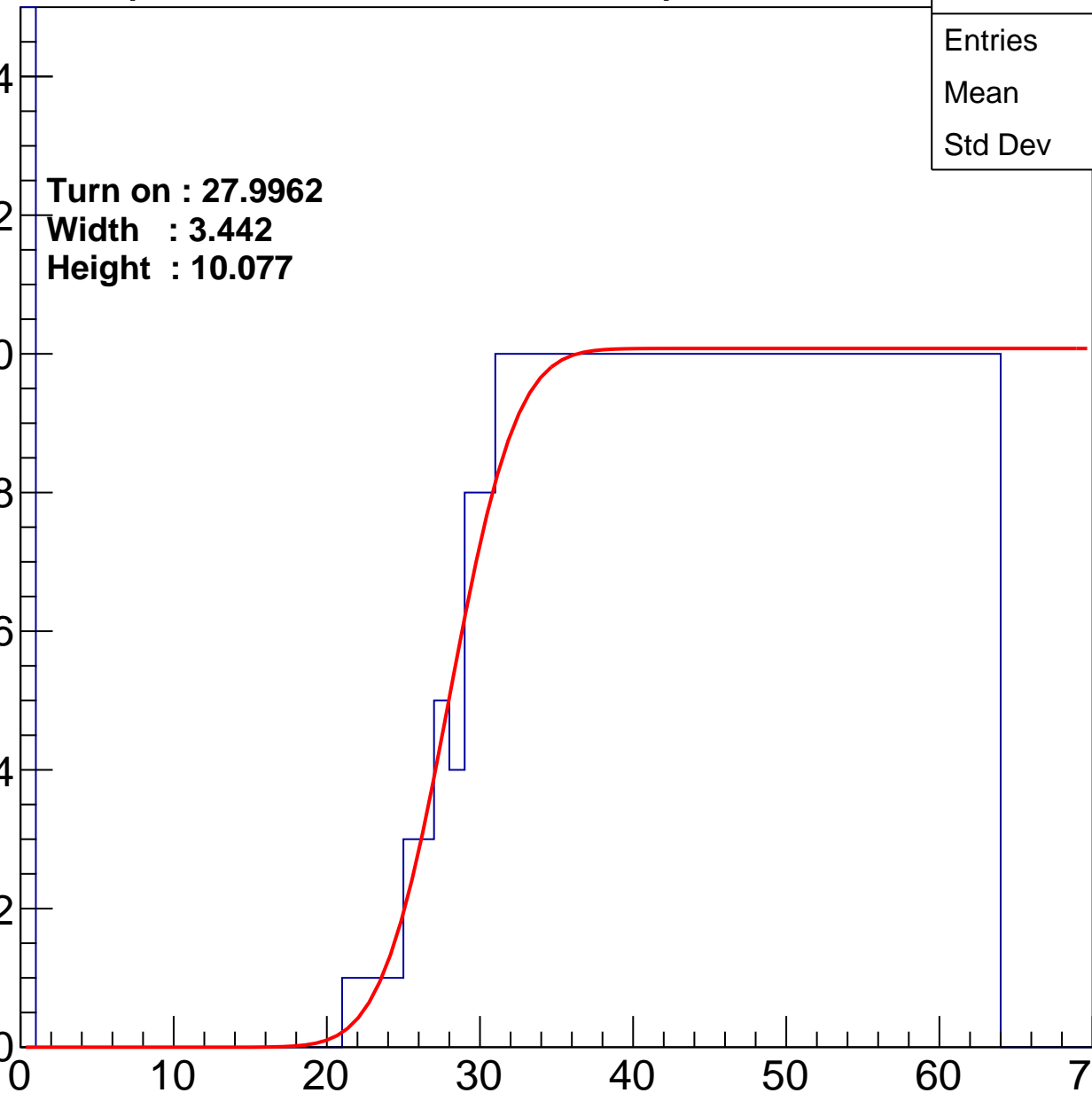
Width : 3.442

Height : 10.077

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch18

calib_packv5_041523_1651.root, FC#0, port C2

Entries	427
Mean	39.88
Std Dev	16.85

Turn on : 25.5913

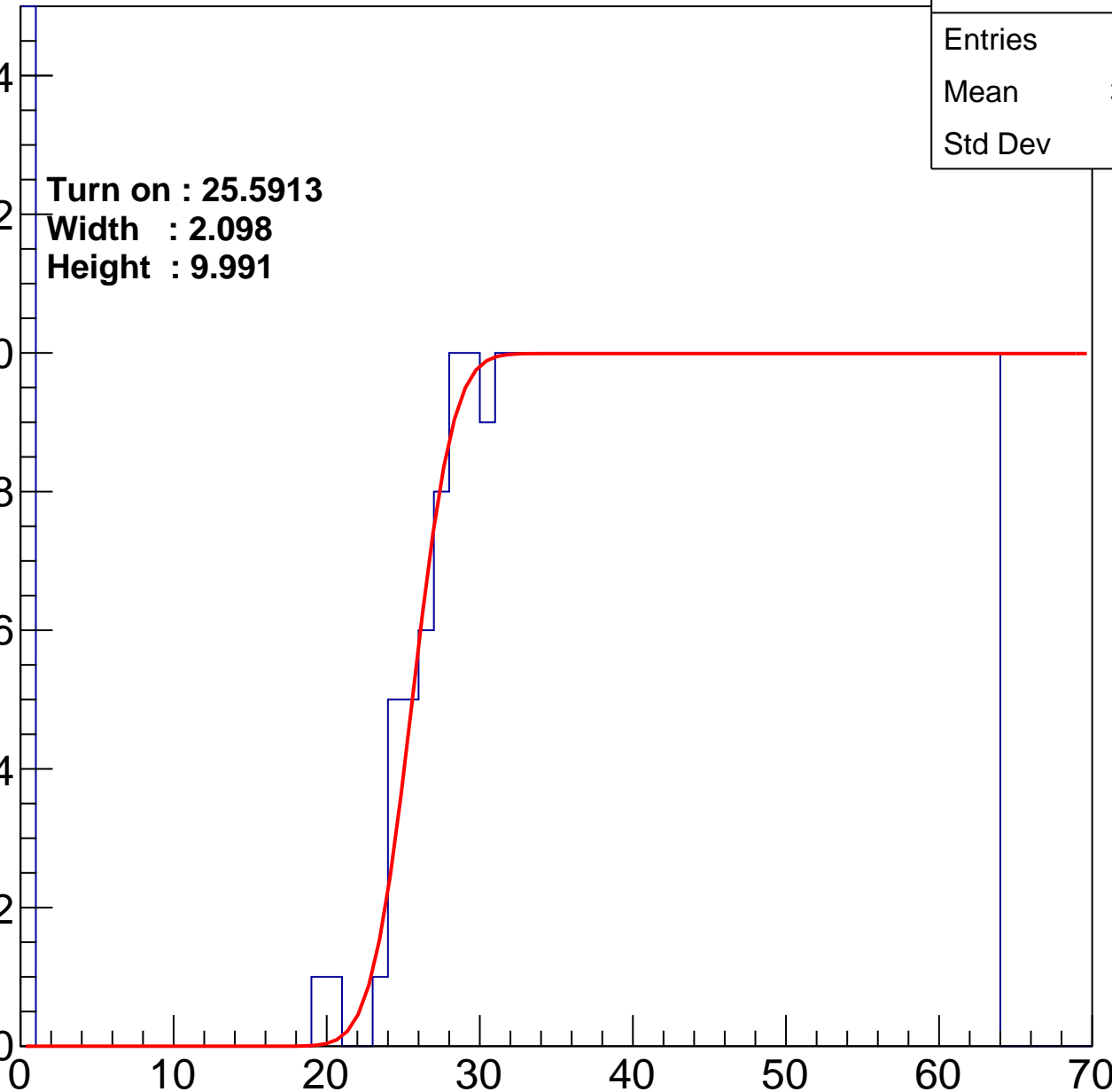
Width : 2.098

Height : 9.991

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch19

calib_packv5_041523_1651.root, FC#0, port C2

Entries	410
Mean	40.41
Std Dev	17.03

Turn on : 27.1256

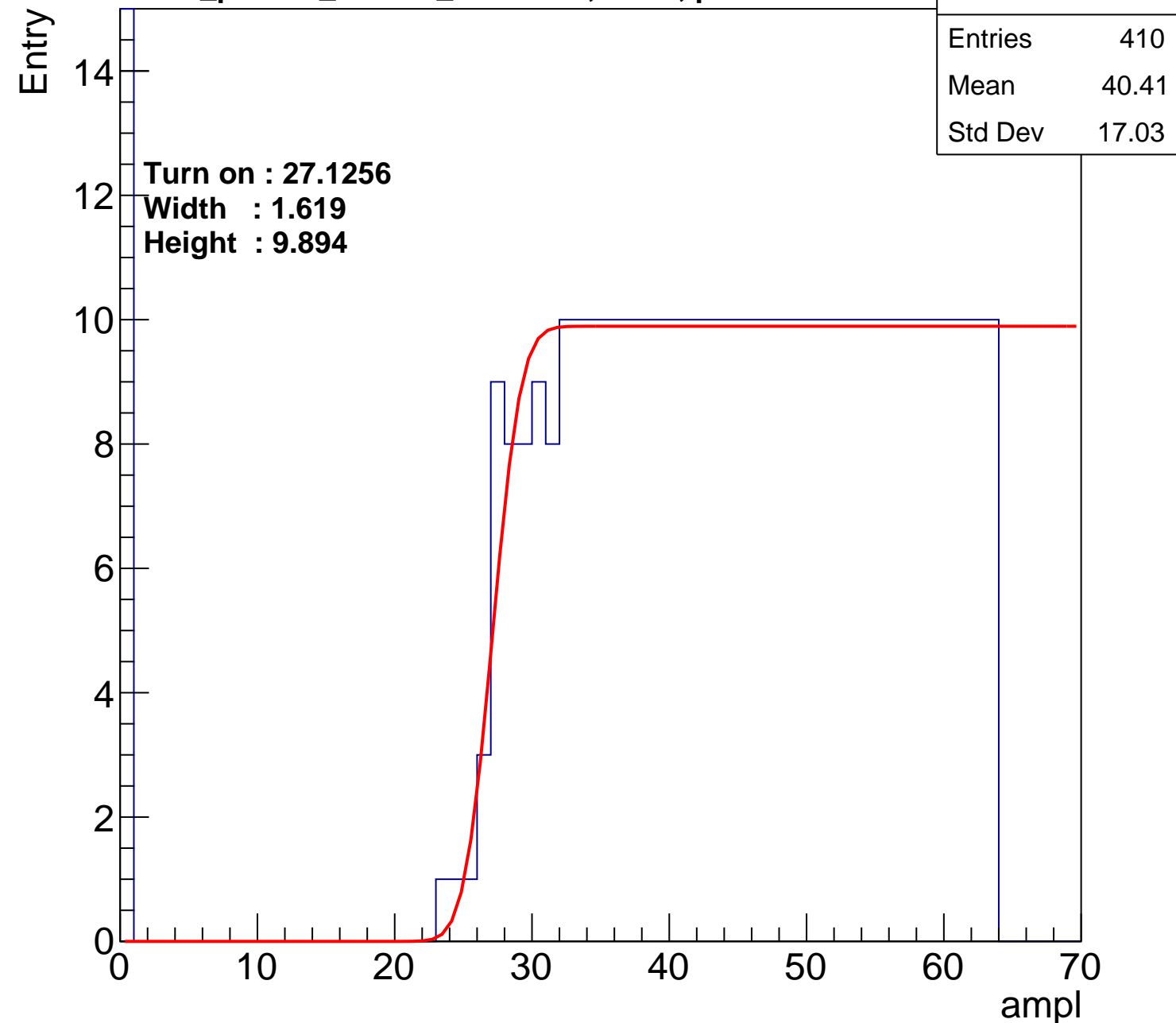
Width : 1.619

Height : 9.894

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch20

calib_packv5_041523_1651.root, FC#0, port C2

Entries	428
Mean	39.46
Std Dev	17.43

Turn on : 26.3797

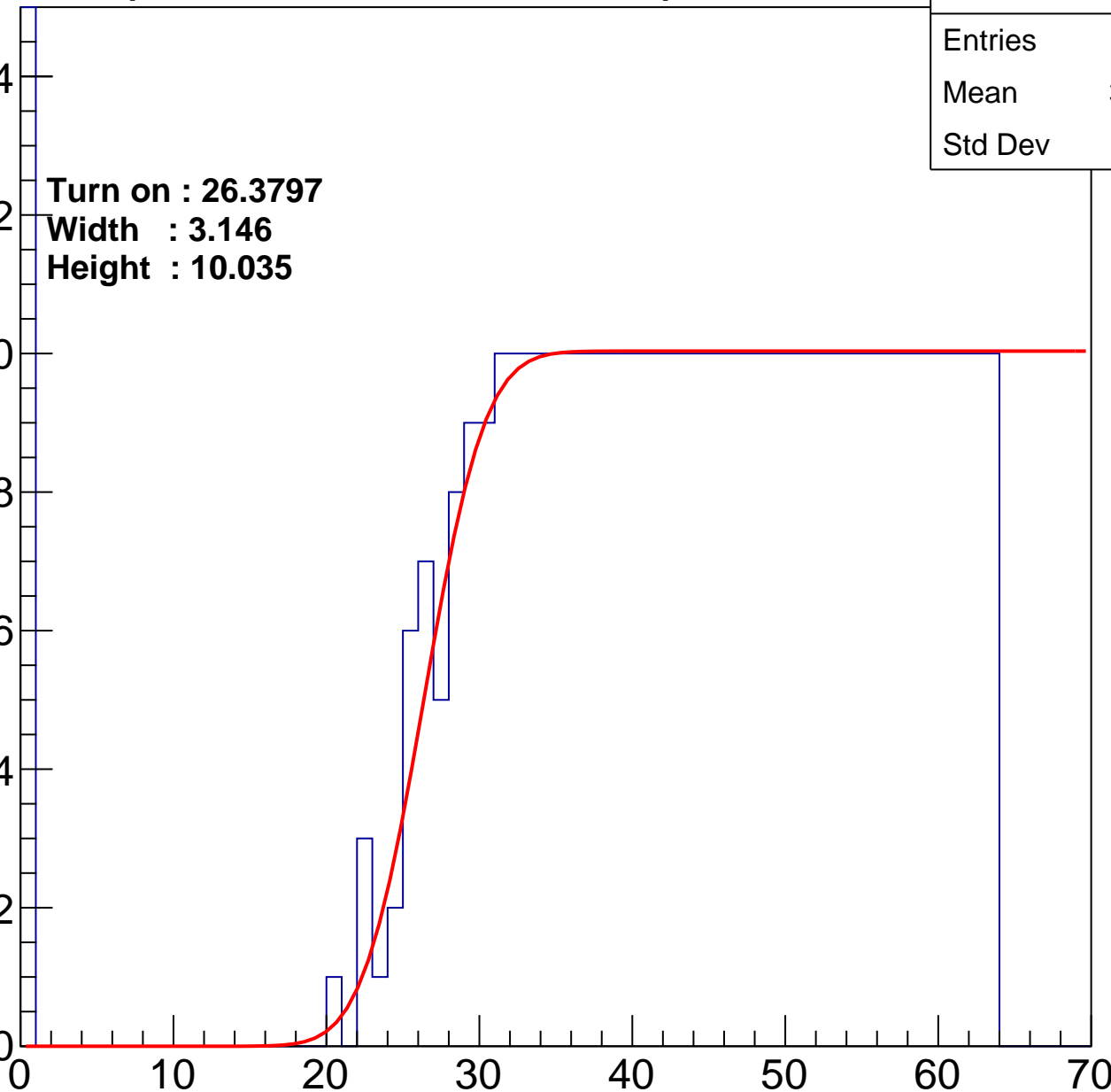
Width : 3.146

Height : 10.035

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch21

calib_packv5_041523_1651.root, FC#0, port C2

Entries	407
Mean	41.13
Std Dev	16

Turn on : 26.2318

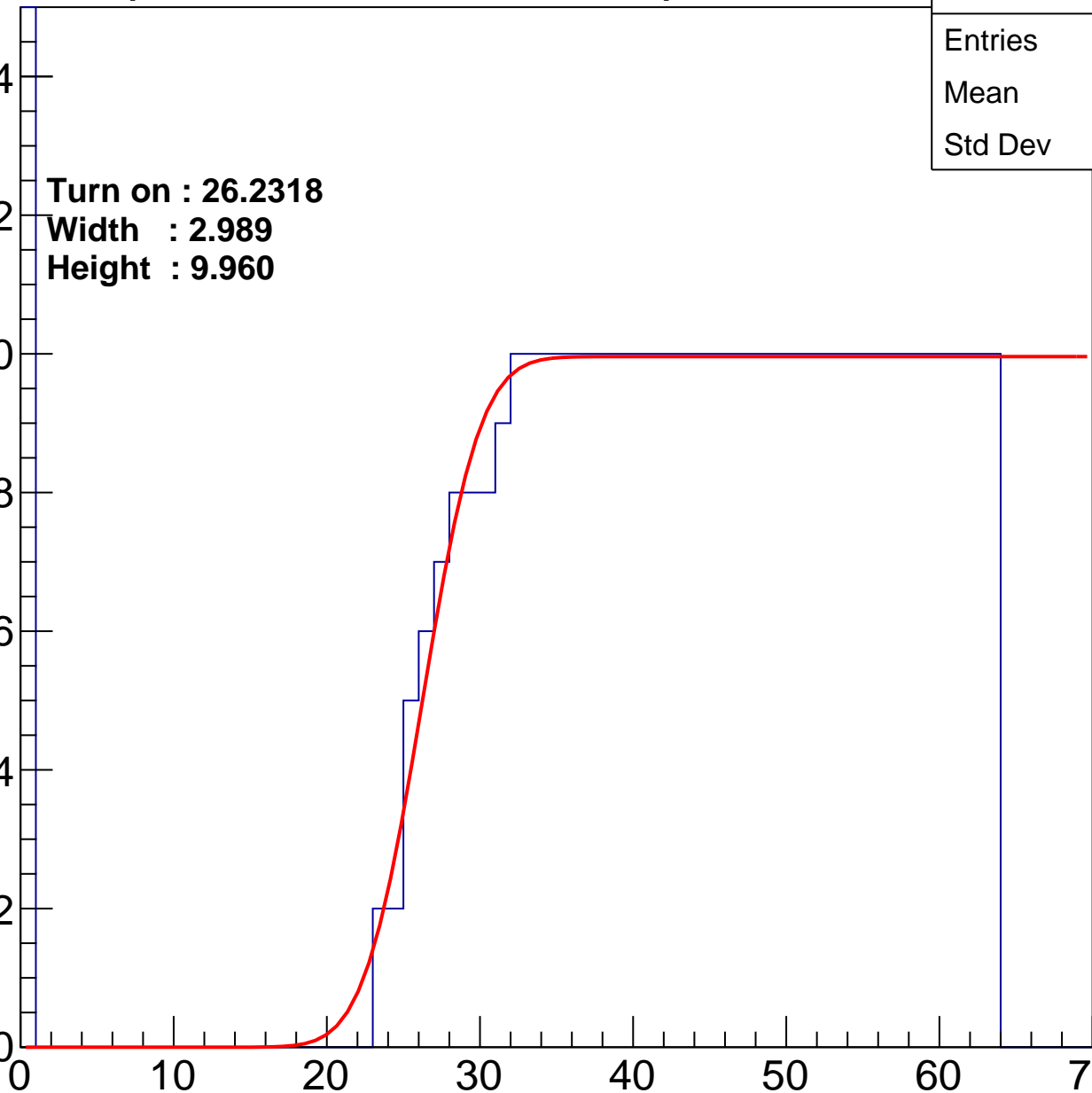
Width : 2.989

Height : 9.960

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch22

calib_packv5_041523_1651.root, FC#0, port C2

Entries	407
Mean	41.01
Std Dev	16.21

Turn on : 26.9218

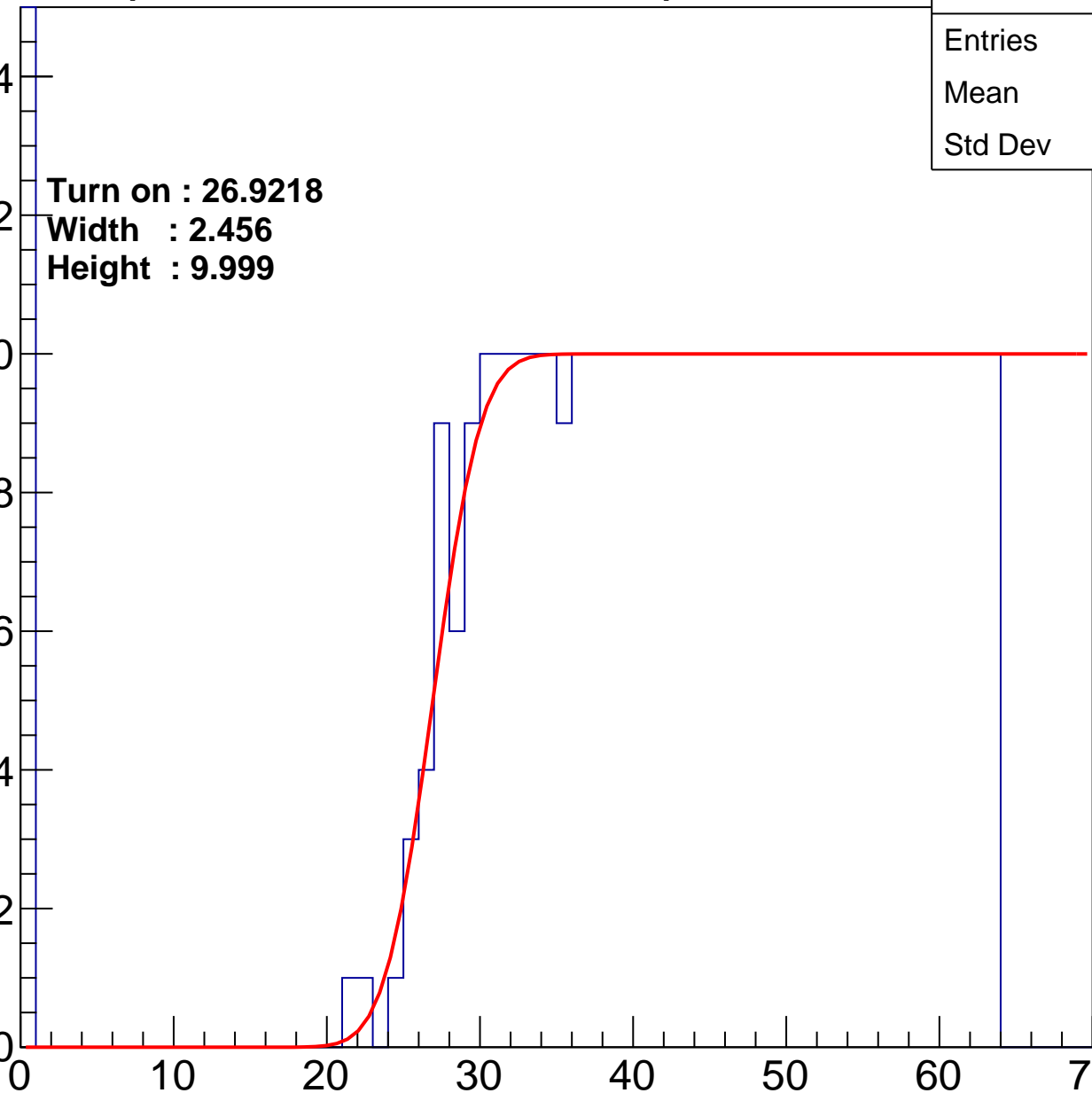
Width : 2.456

Height : 9.999

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch23

calib_packv5_041523_1651.root, FC#0, port C2

Entries	383
Mean	42.01
Std Dev	16.08

Turn on : 29.2683

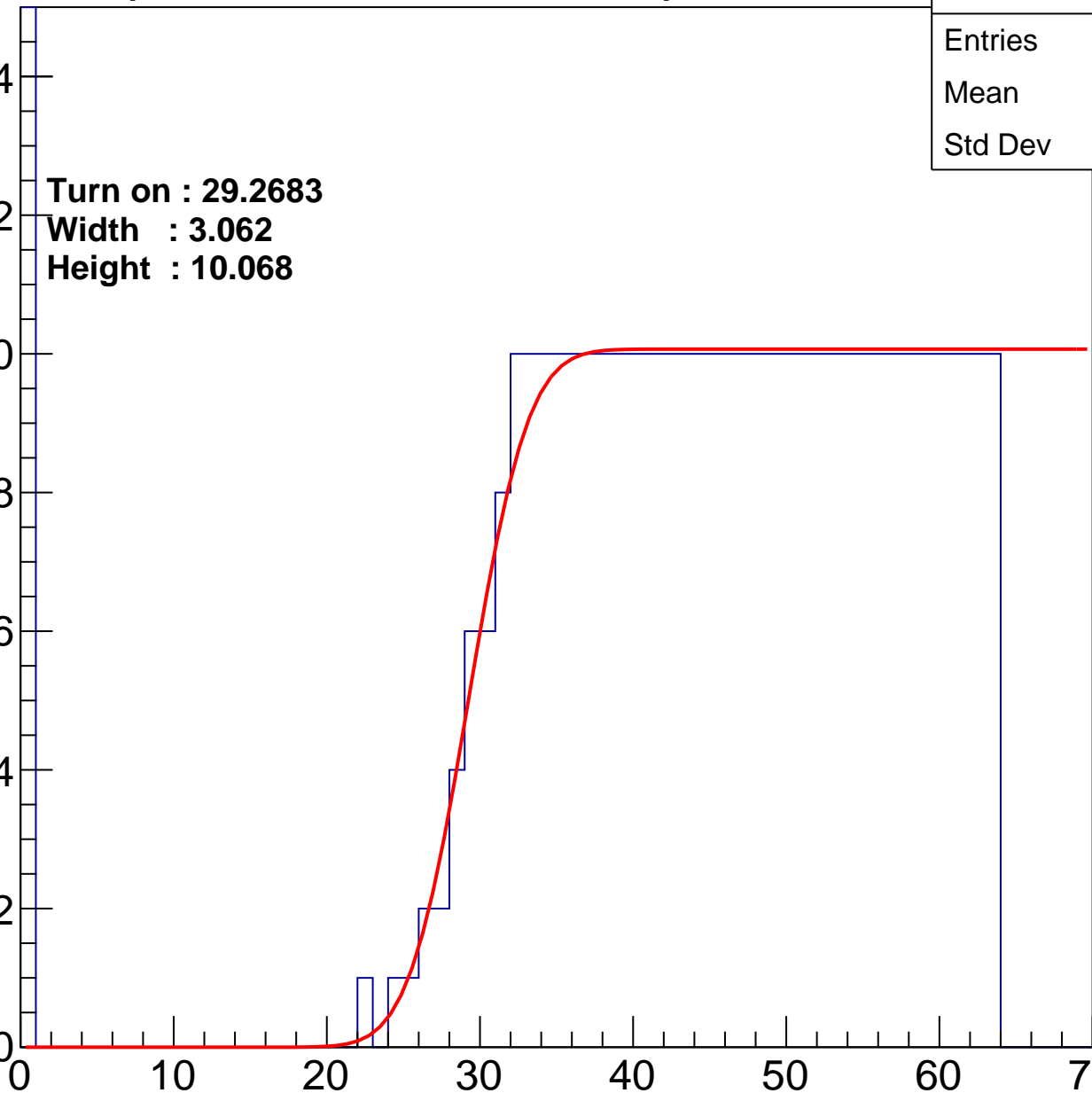
Width : 3.062

Height : 10.068

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch24

calib_packv5_041523_1651.root, FC#0, port C2

Entries	420
Mean	39.2
Std Dev	18.23

Turn on : 27.4748

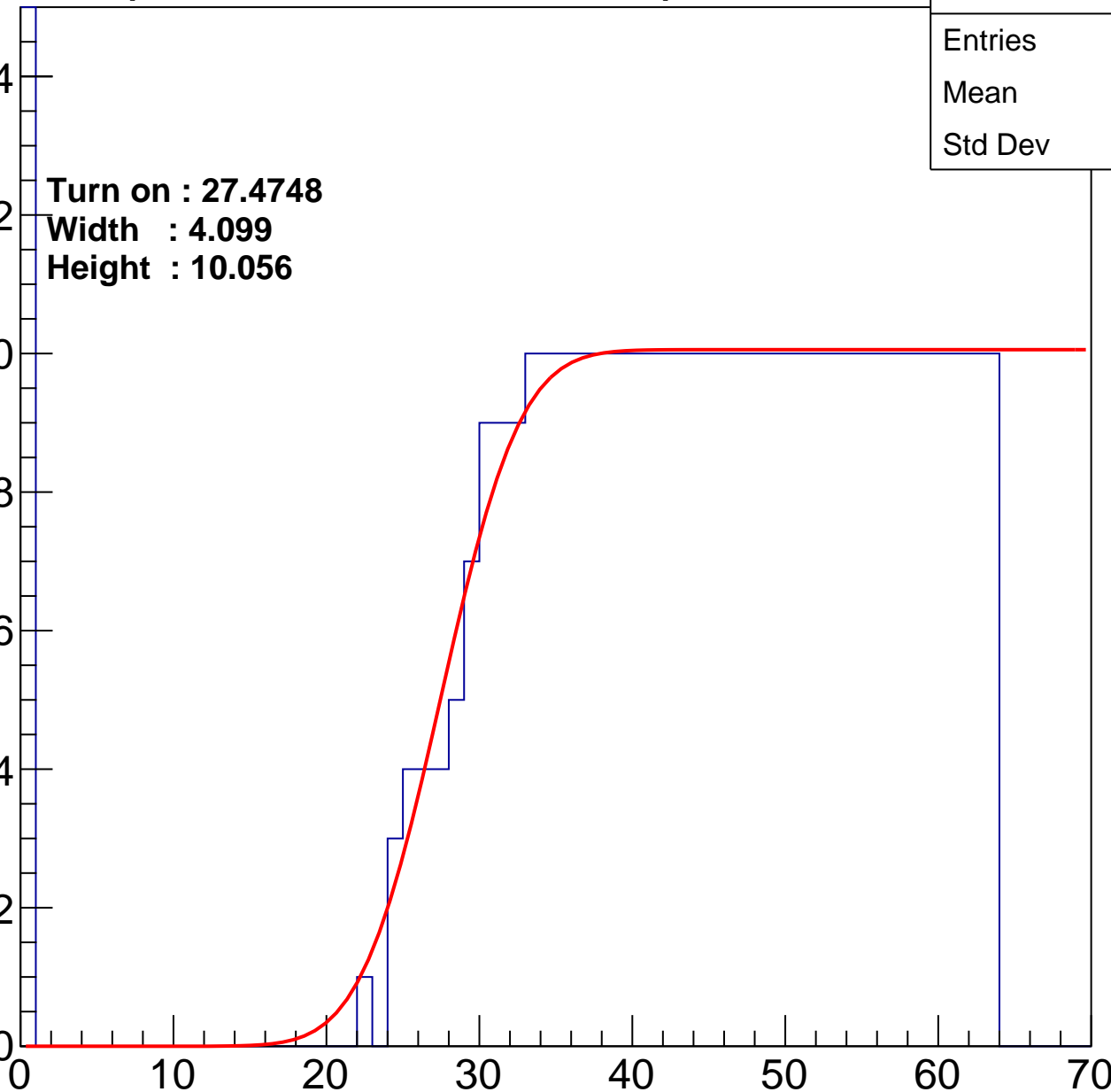
Width : 4.099

Height : 10.056

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch25

calib_packv5_041523_1651.root, FC#0, port C2

Entries	401
Mean	40.92
Std Dev	16.77

Turn on : 27.8360

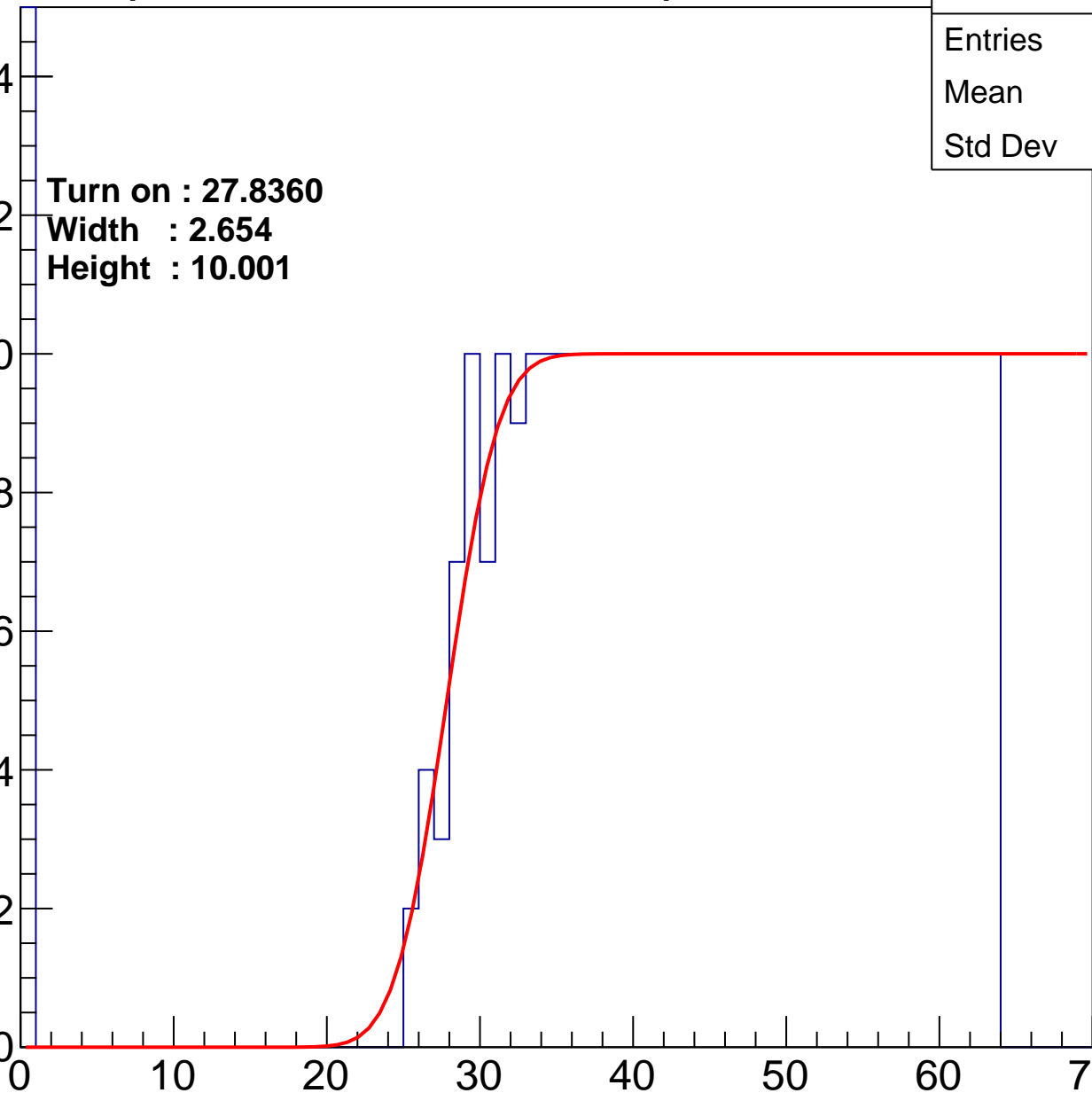
Width : 2.654

Height : 10.001

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch26

calib_packv5_041523_1651.root, FC#0, port C2

Entries	410
Mean	40.88
Std Dev	16.23

Turn on : 26.7330

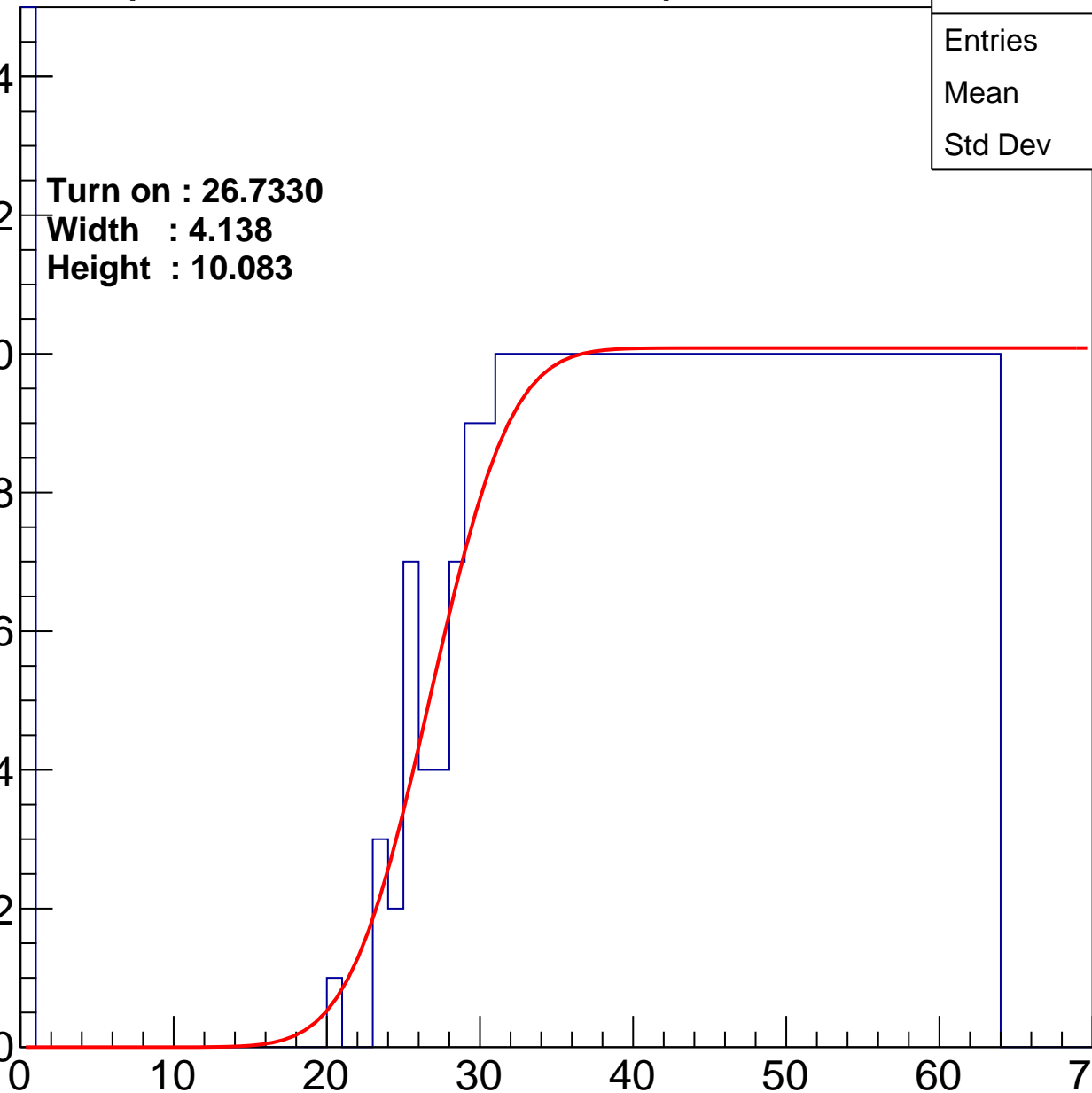
Width : 4.138

Height : 10.083

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch27

calib_packv5_041523_1651.root, FC#0, port C2

Entries	415
Mean	40.33
Std Dev	16.84

Turn on : 27.1147

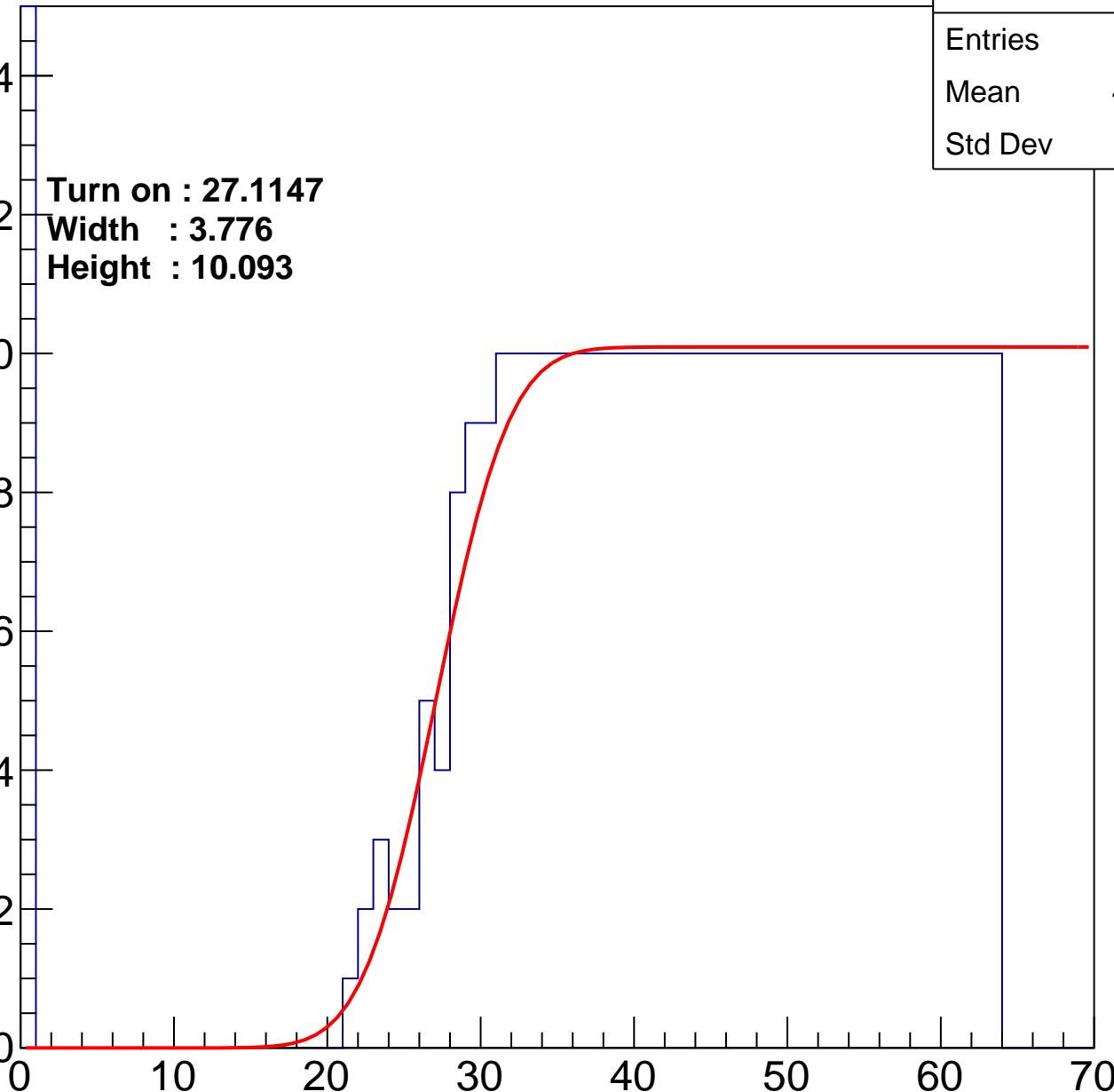
Width : 3.776

Height : 10.093

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch28

calib_packv5_041523_1651.root, FC#0, port C2

Entries	448
Mean	39.17
Std Dev	16.73

Turn on : 22.9100

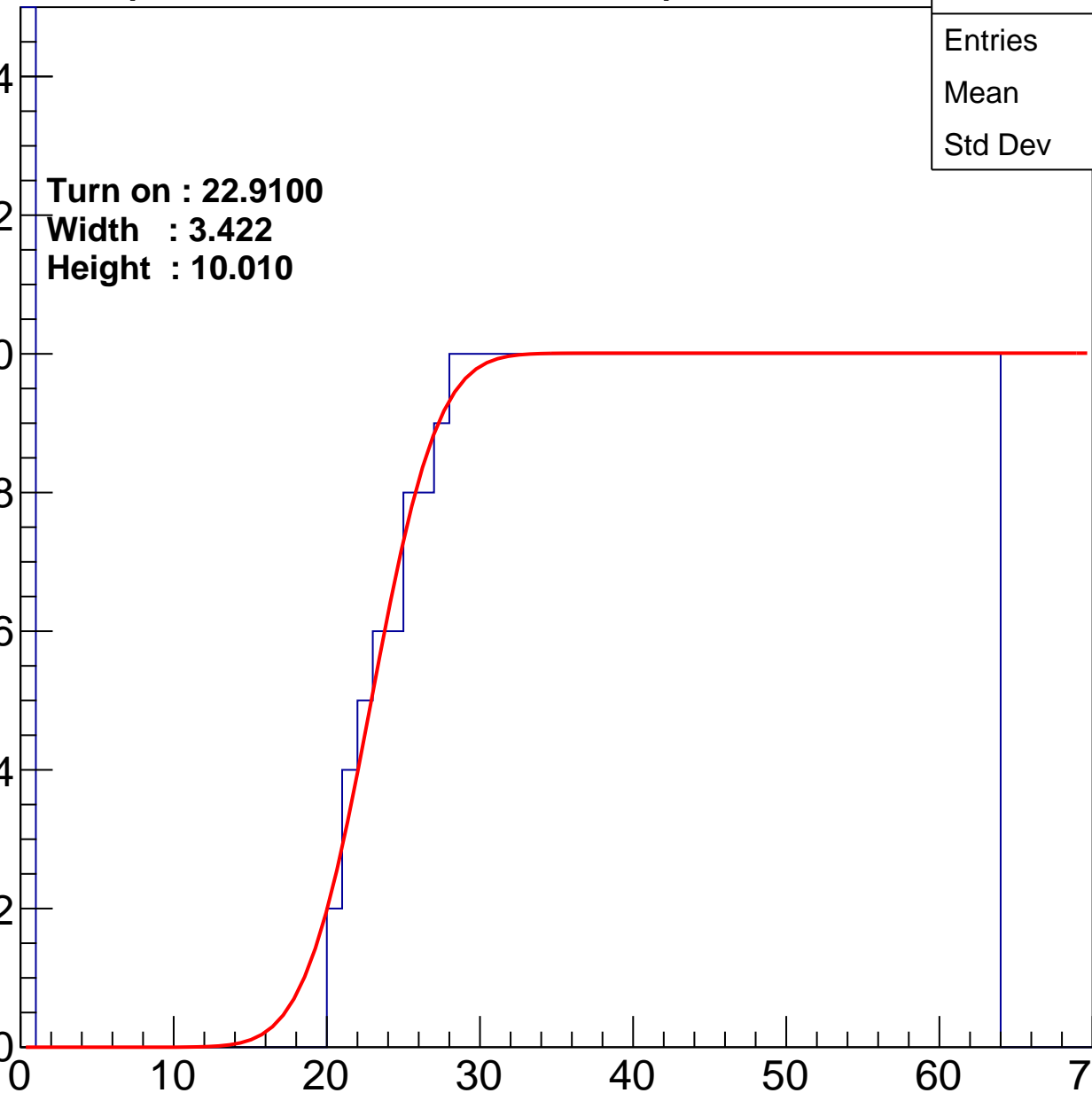
Width : 3.422

Height : 10.010

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch29

calib_packv5_041523_1651.root, FC#0, port C2

Entries	395
Mean	40.38
Std Dev	17.92

Turn on : 29.3991

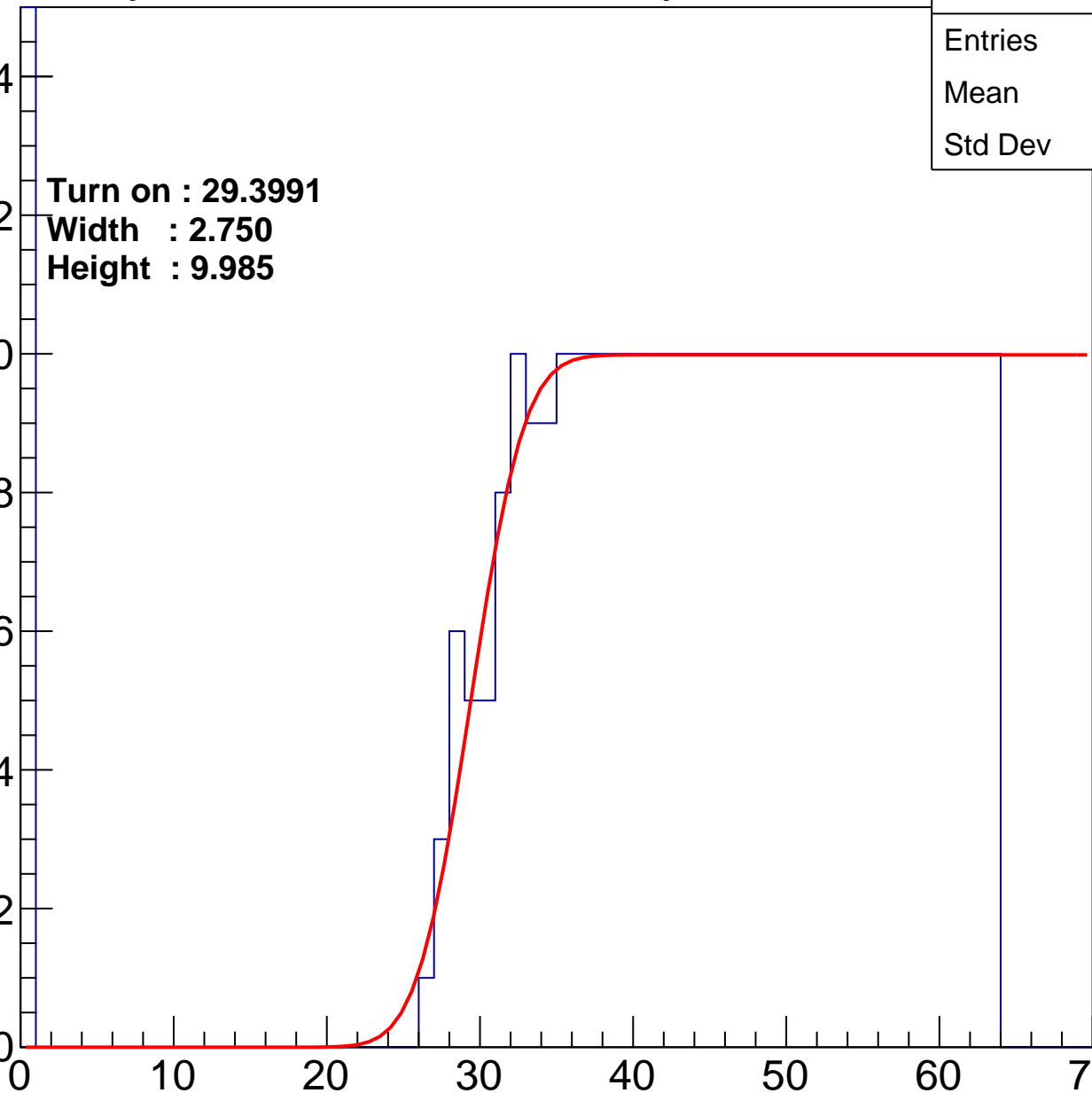
Width : 2.750

Height : 9.985

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch30

calib_packv5_041523_1651.root, FC#0, port C2

Entries	430
Mean	39.6
Std Dev	17.12

Turn on : 25.6355

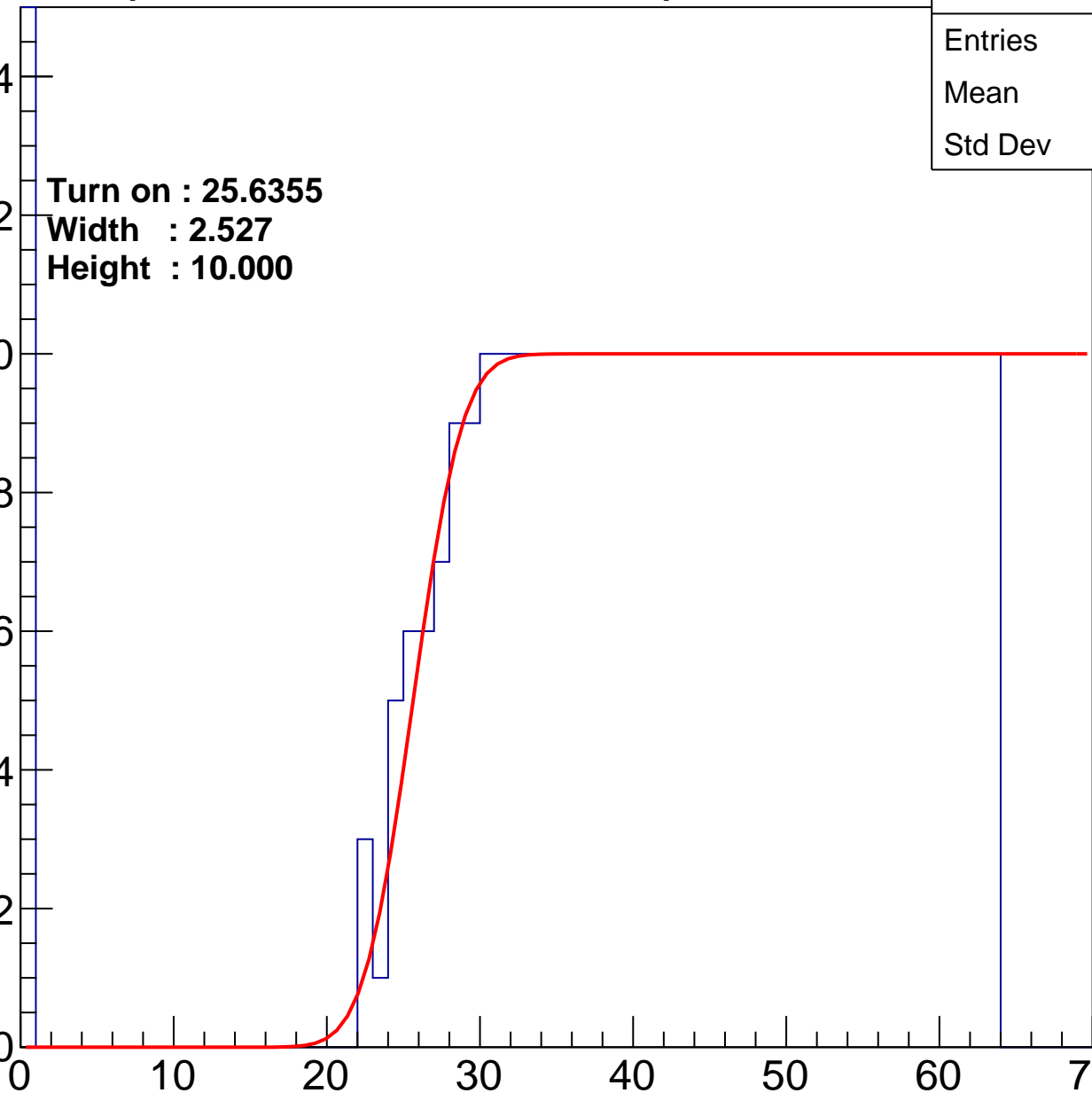
Width : 2.527

Height : 10.000

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch31

calib_packv5_041523_1651.root, FC#0, port C2

Entries	414
Mean	40.66
Std Dev	16.33

Turn on : 26.4263

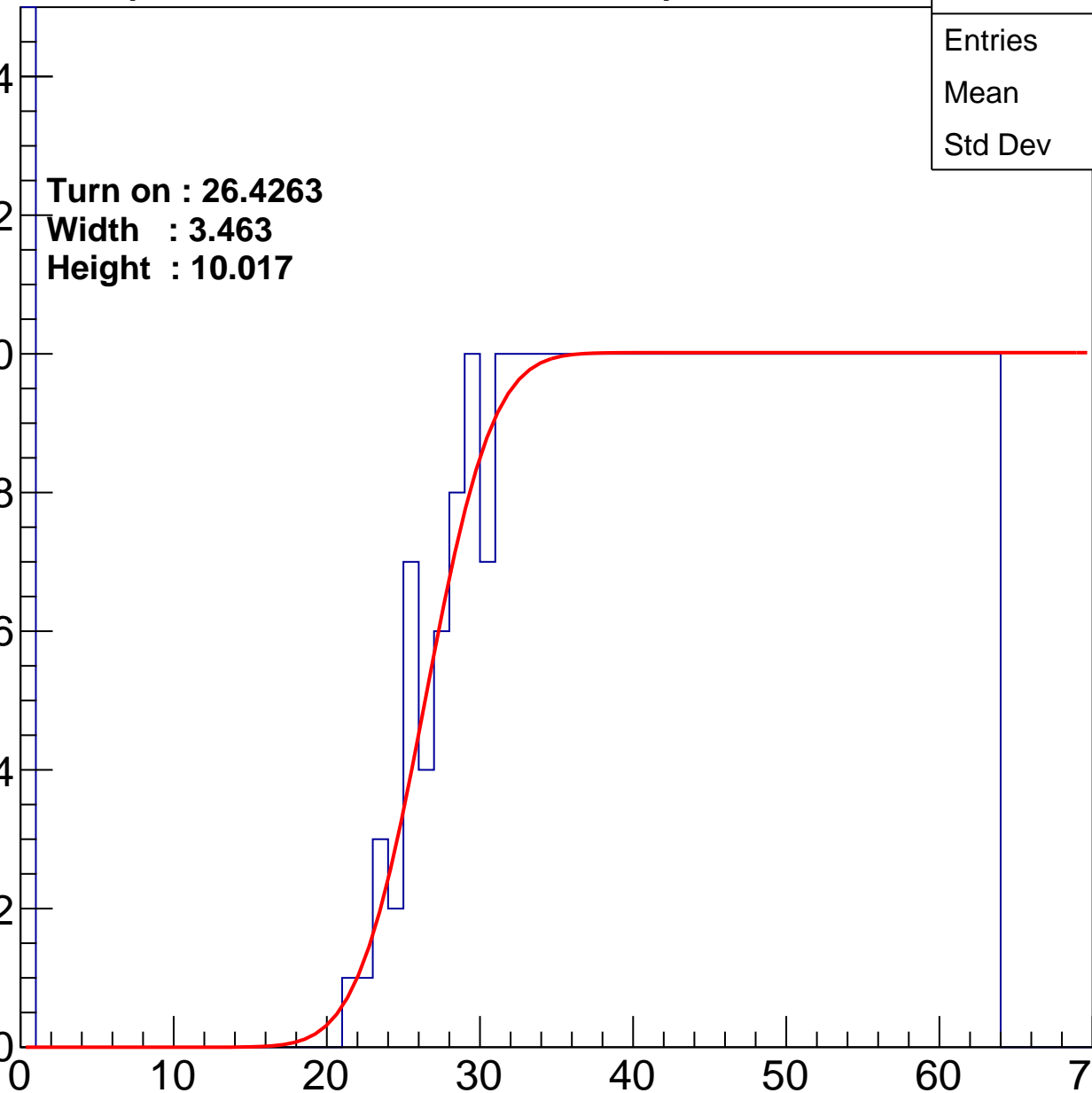
Width : 3.463

Height : 10.017

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch32

calib_packv5_041523_1651.root, FC#0, port C2

Entries	412
Mean	41.13
Std Dev	15.66

Turn on : 25.8163

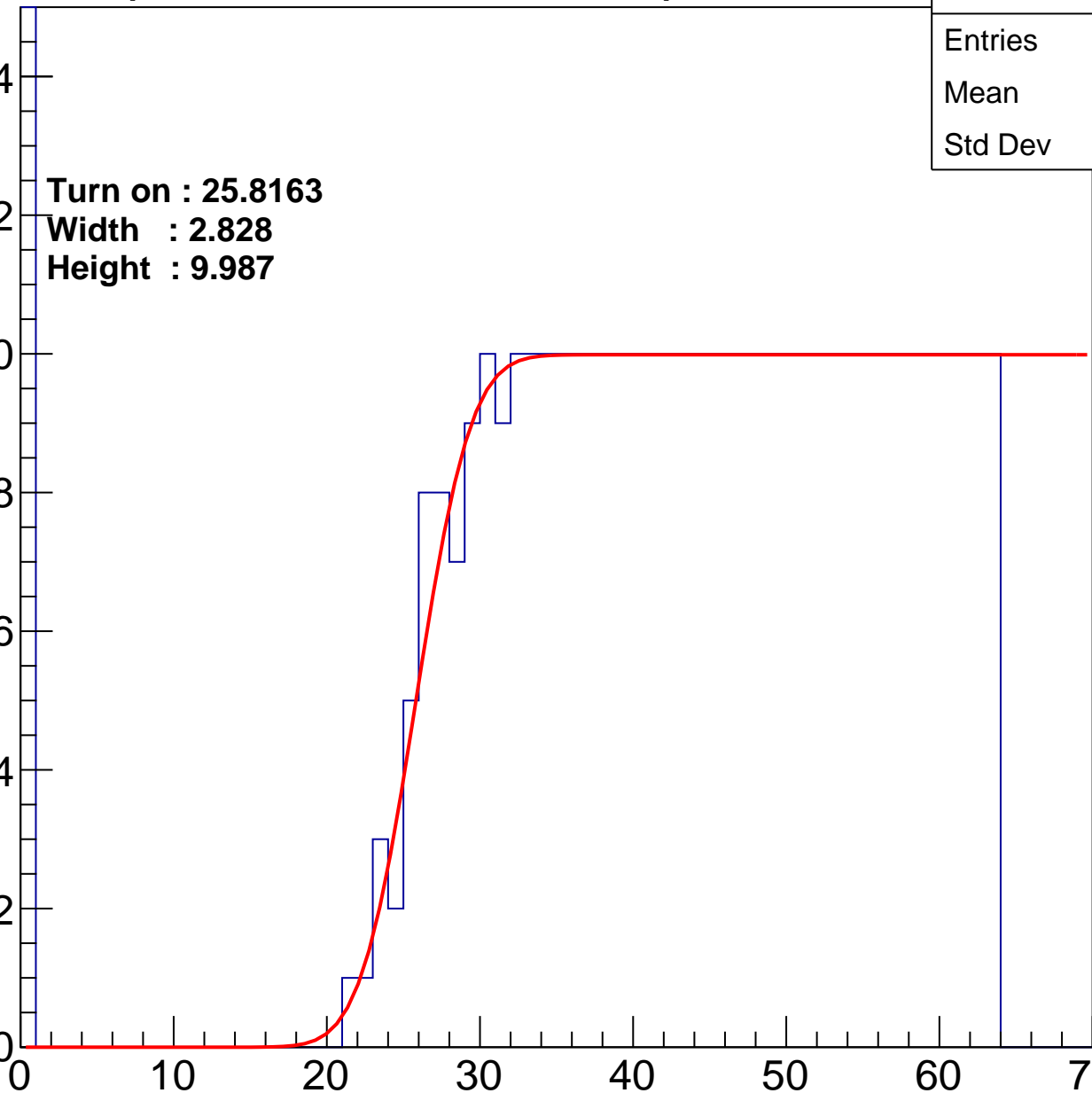
Width : 2.828

Height : 9.987

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch33

calib_packv5_041523_1651.root, FC#0, port C2

Entries	385
Mean	42.2
Std Dev	15.64

Turn on : 28.7753

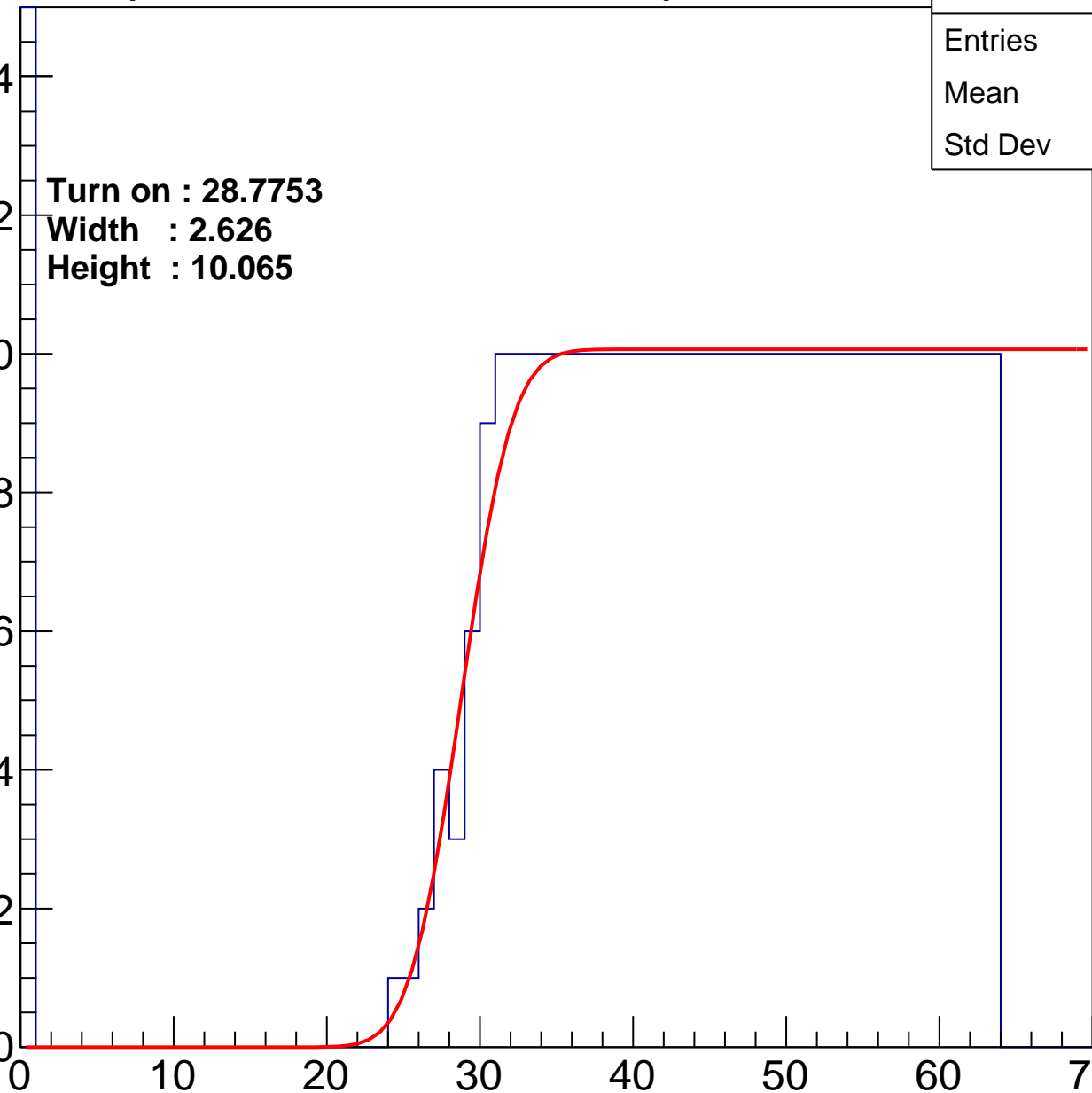
Width : 2.626

Height : 10.065

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch34

calib_packv5_041523_1651.root, FC#0, port C2

Entries	416
Mean	40.77
Std Dev	16.06

Turn on : 25.3806

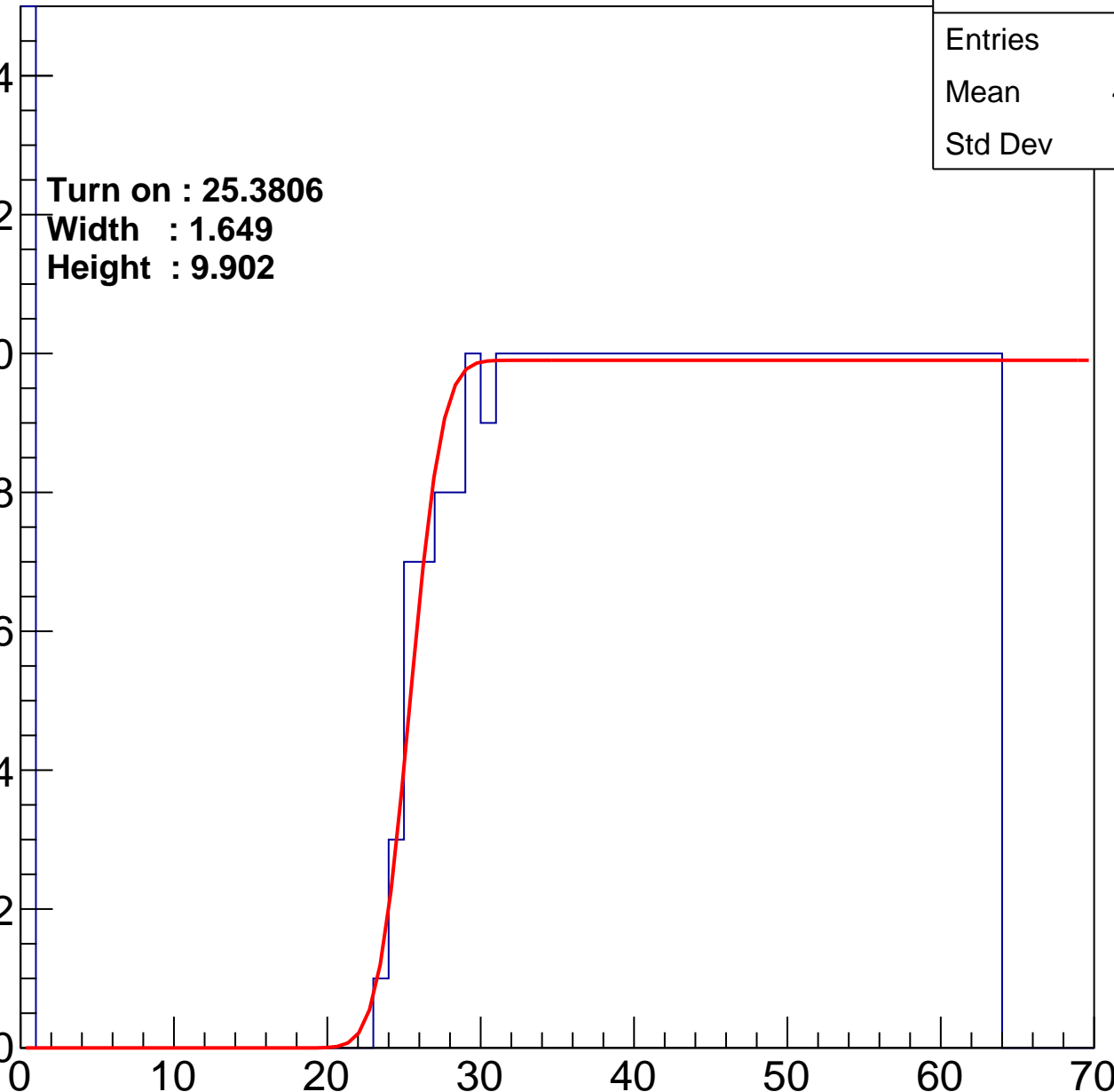
Width : 1.649

Height : 9.902

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch35

calib_packv5_041523_1651.root, FC#0, port C2

Entries	420
Mean	39.83
Std Dev	17.31

Turn on : 26.5888

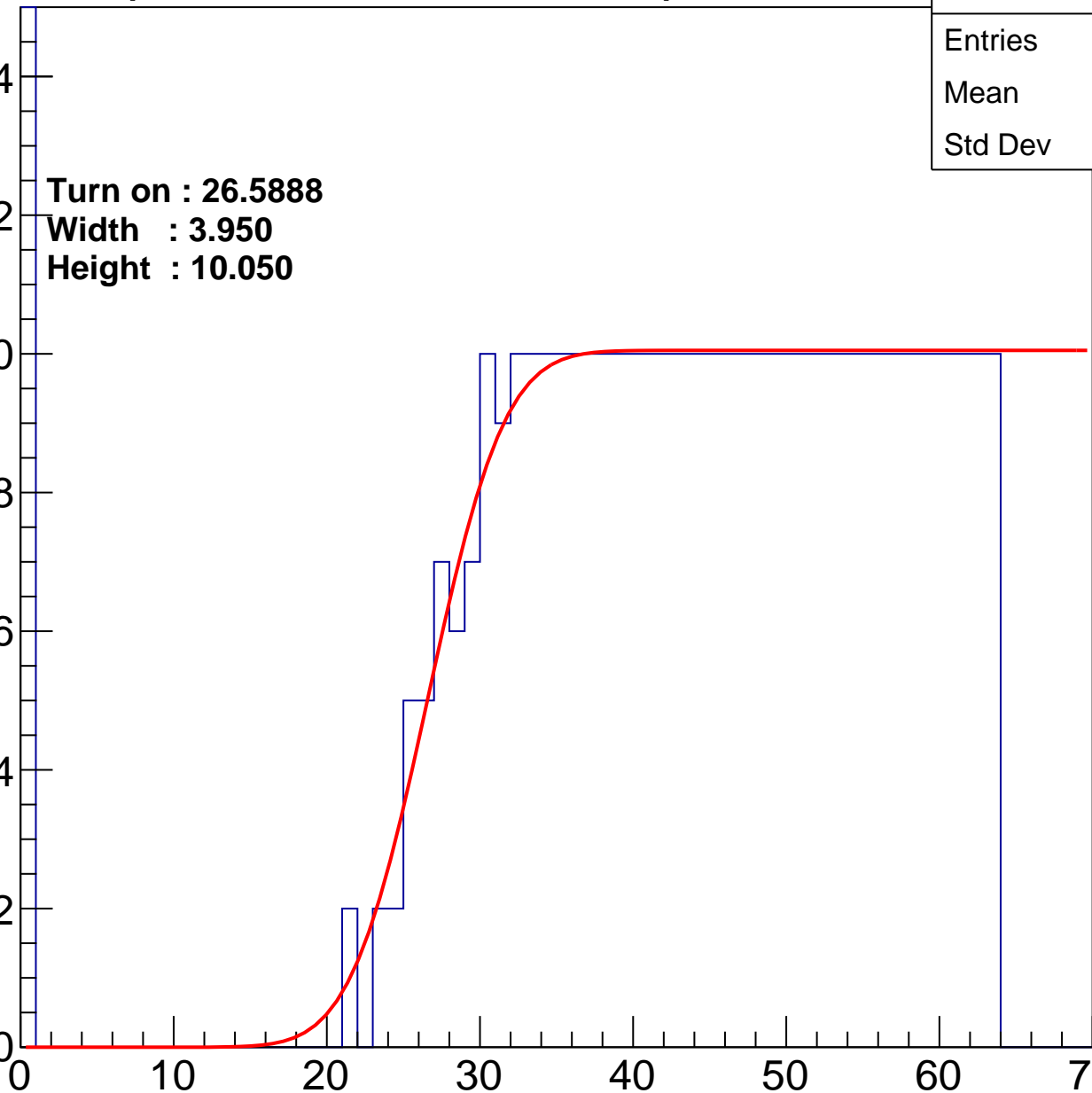
Width : 3.950

Height : 10.050

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch36

calib_packv5_041523_1651.root, FC#0, port C2

Entries	423
Mean	40.37
Std Dev	16.28

Turn on : 25.1182

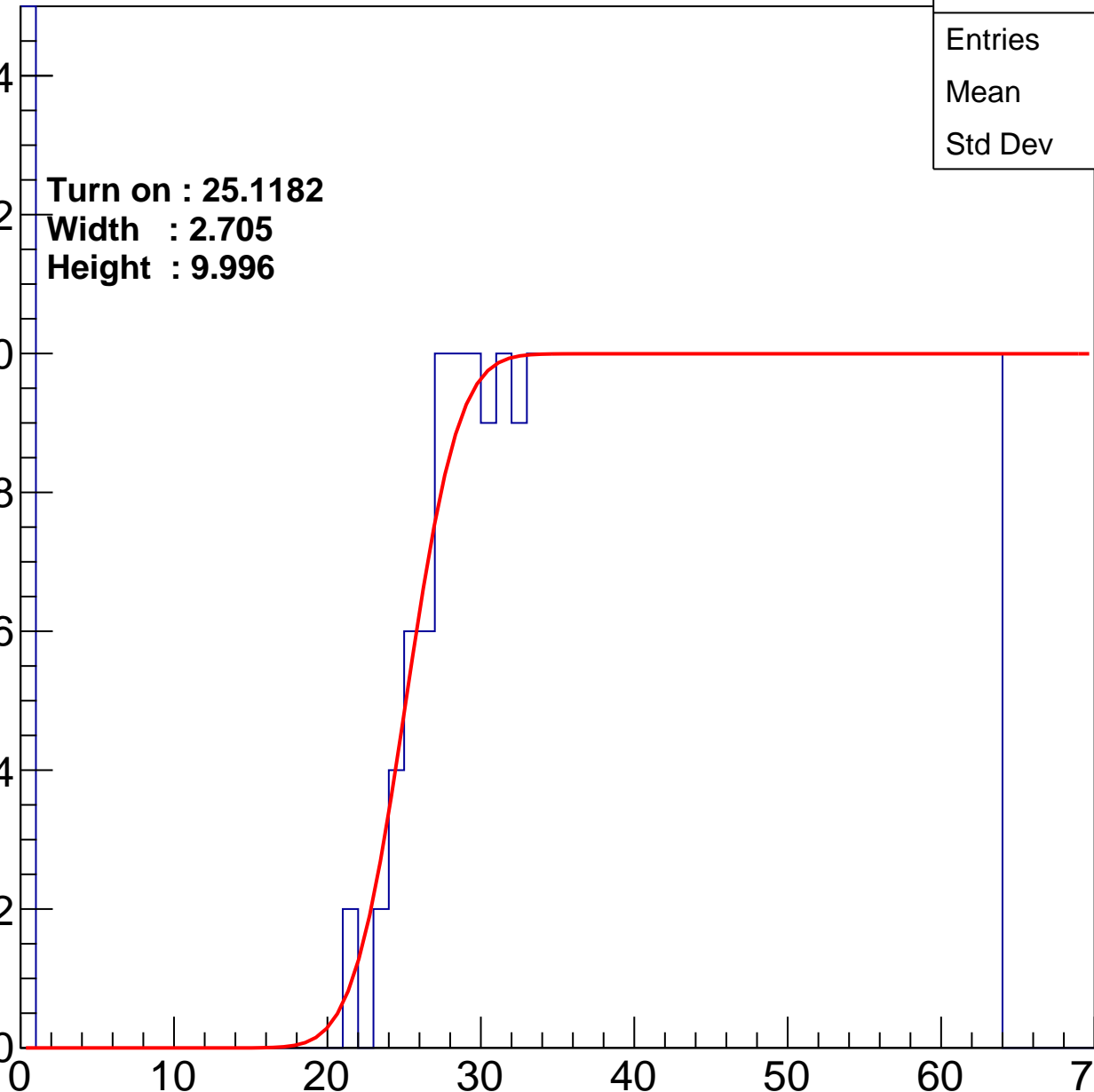
Width : 2.705

Height : 9.996

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch37

calib_packv5_041523_1651.root, FC#0, port C2

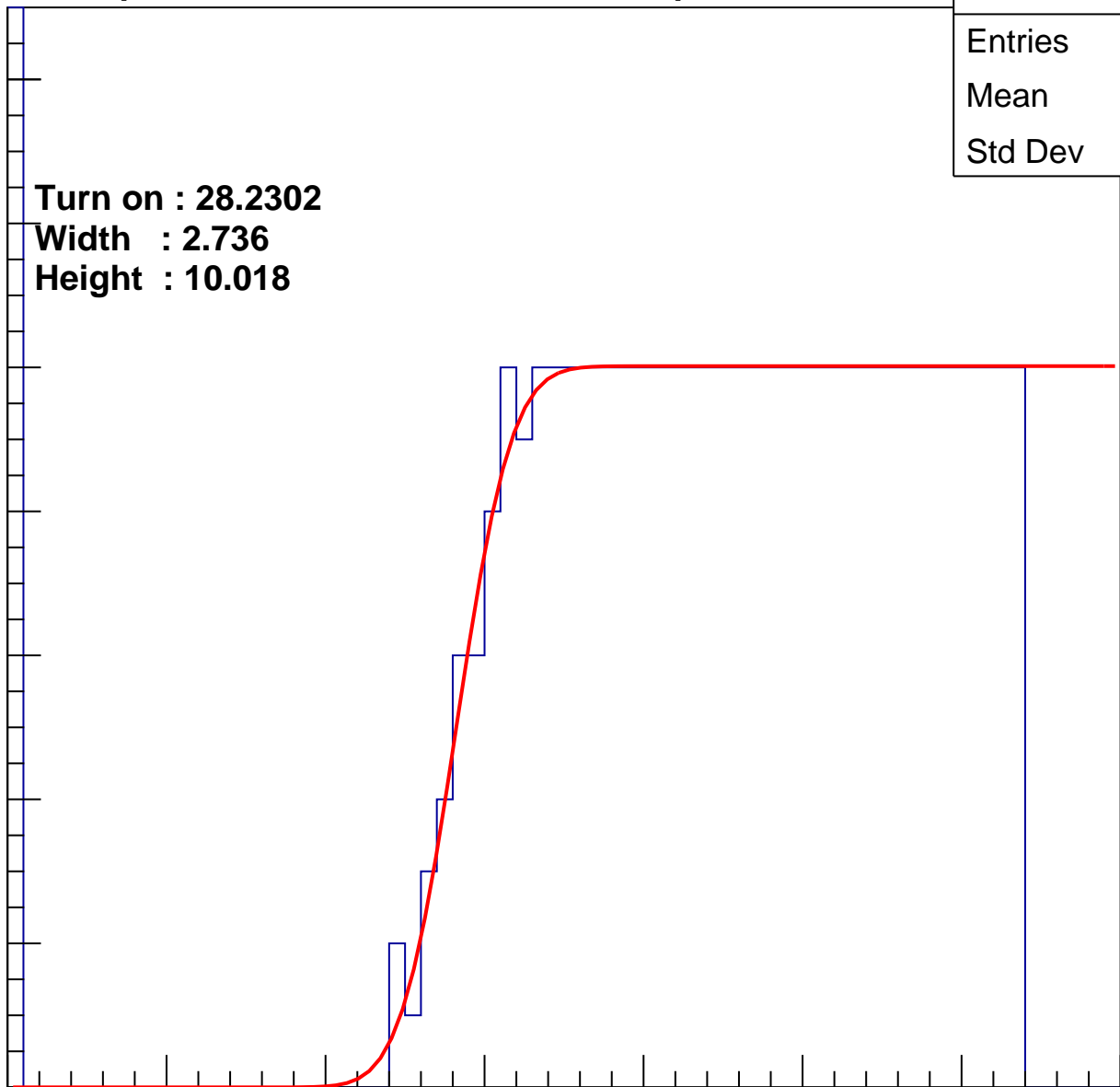
Entry

14
12
10
8
6
4
2
0

Turn on : 28.2302
Width : 2.736
Height : 10.018

Entries	391
Mean	41.74
Std Dev	16.03

ampl



B1L103S, U10-ch38

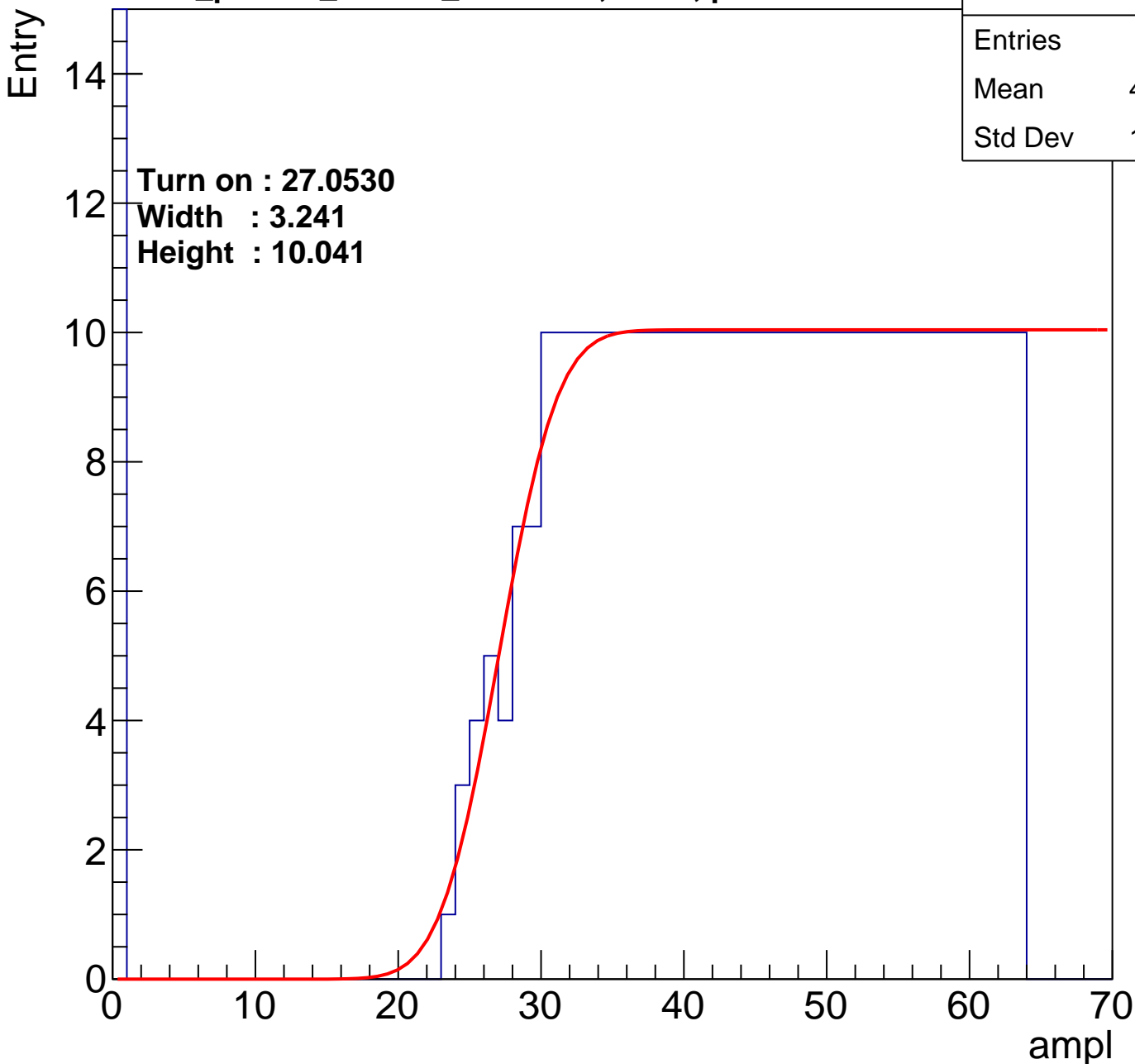
calib_packv5_041523_1651.root, FC#0, port C2

Entries	406
Mean	40.99
Std Dev	16.32

Turn on : 27.0530

Width : 3.241

Height : 10.041



B1L103S, U10-ch39

calib_packv5_041523_1651.root, FC#0, port C2

Entries	404
Mean	40.9
Std Dev	16.63

Turn on : 27.5565

Width : 2.305

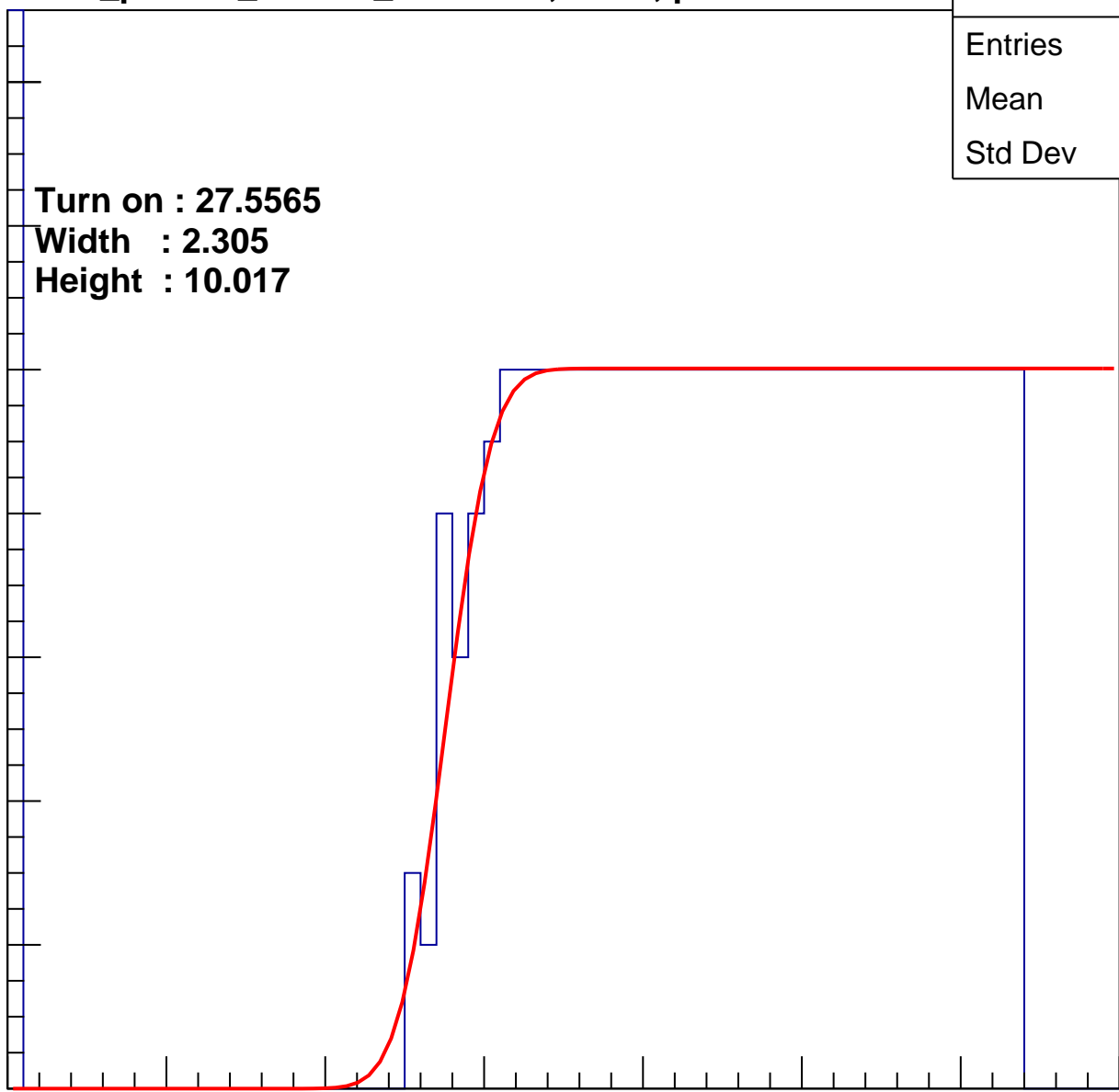
Height : 10.017

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L103S, U10-ch40

calib_packv5_041523_1651.root, FC#0, port C2

Entries	400
Mean	41.31
Std Dev	16.36

Turn on : 28.2508

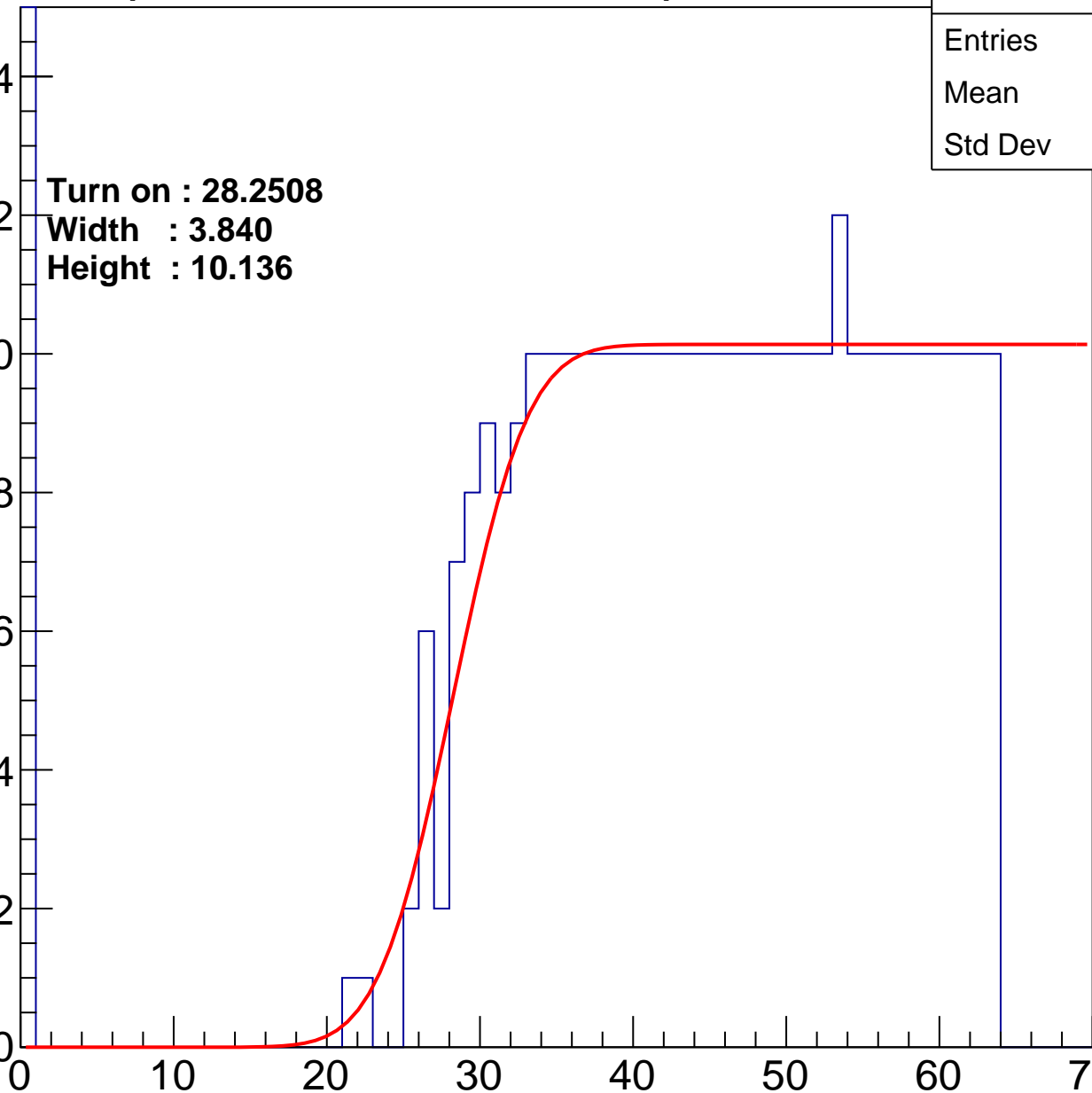
Width : 3.840

Height : 10.136

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch41

calib_packv5_041523_1651.root, FC#0, port C2

Entries	414
Mean	40.64
Std Dev	16.4

Turn on : 26.5857

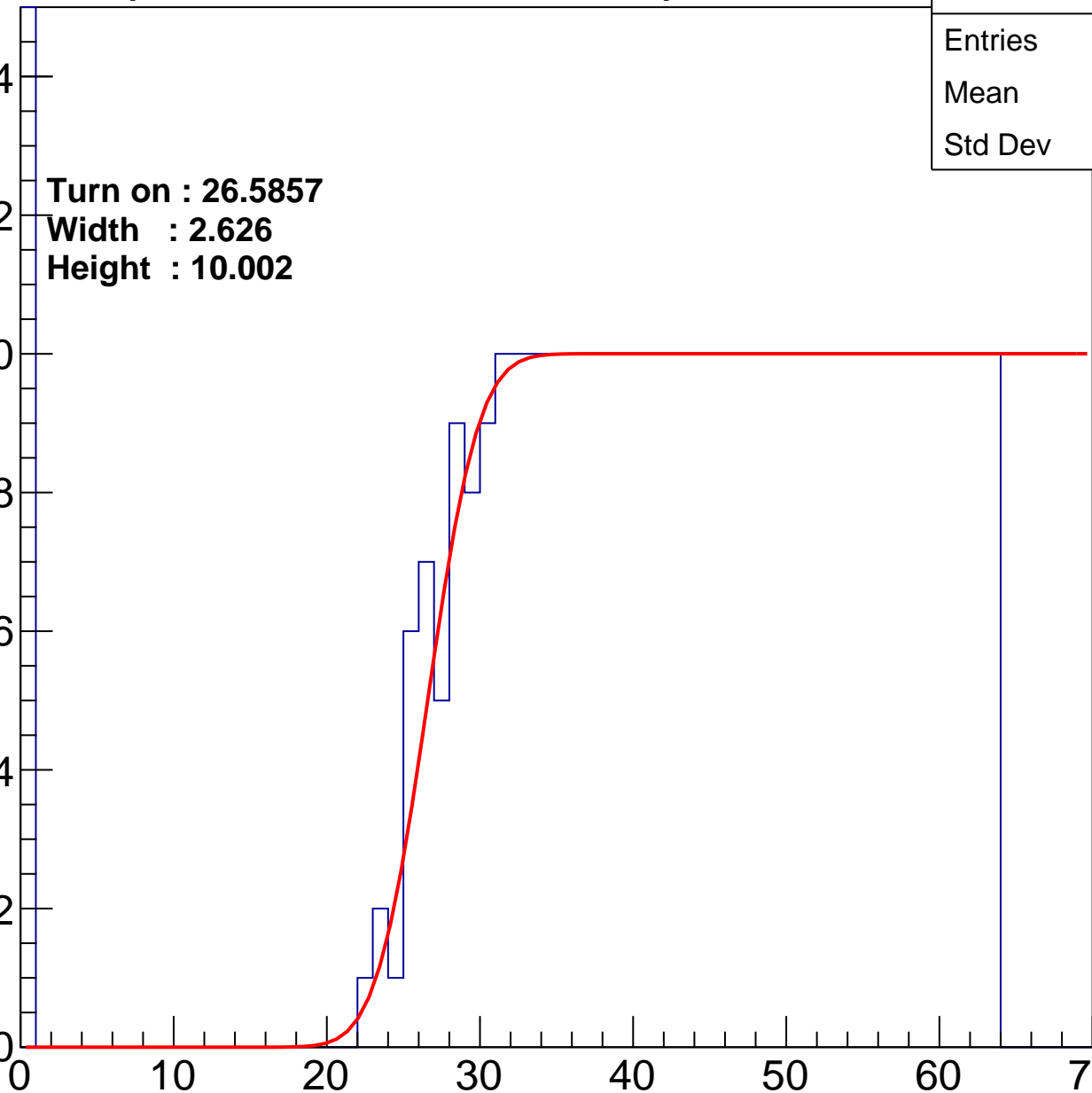
Width : 2.626

Height : 10.002

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch42

calib_packv5_041523_1651.root, FC#0, port C2

Entries	420
Mean	40.38
Std Dev	16.47

Turn on : 26.0683

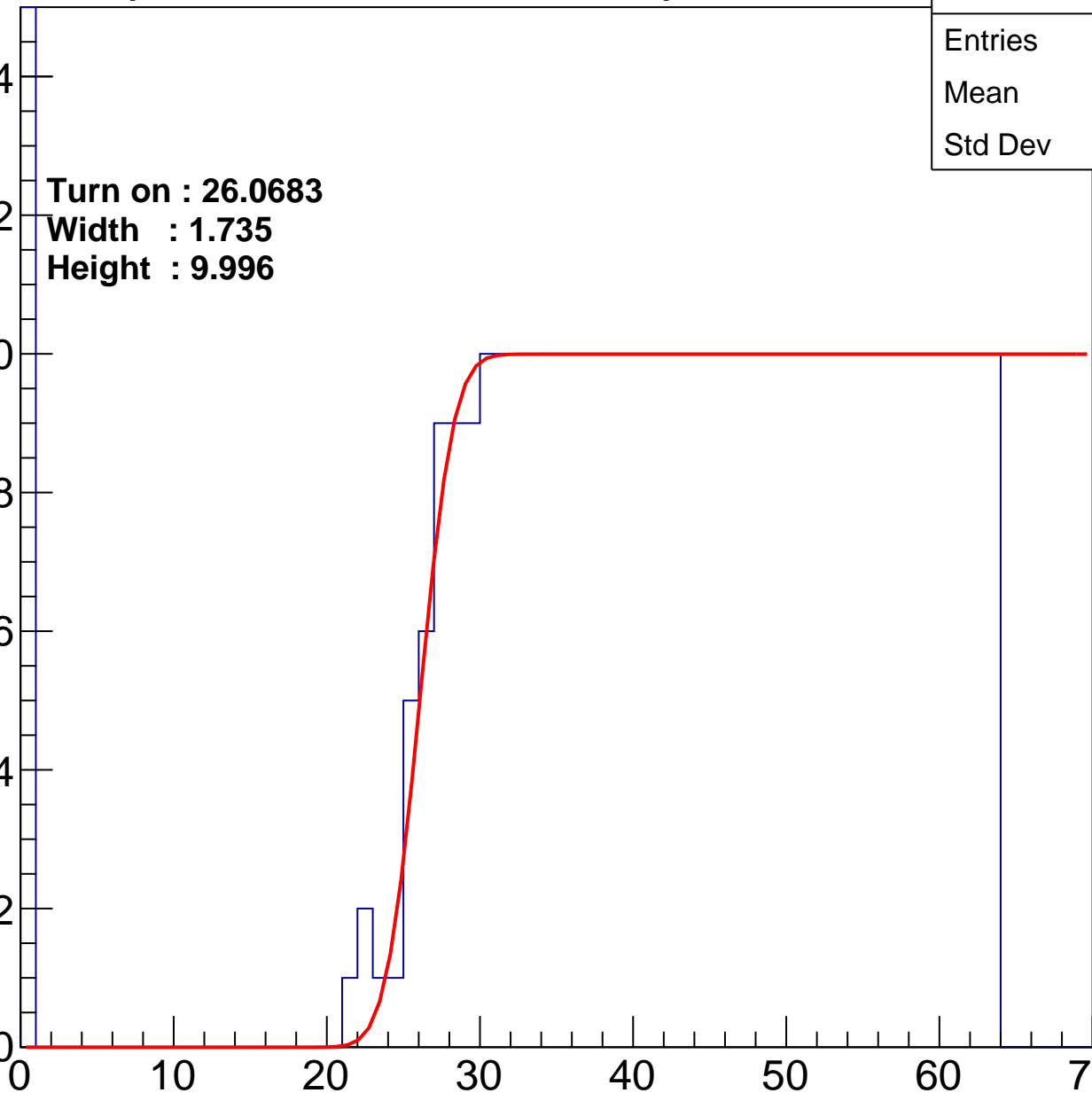
Width : 1.735

Height : 9.996

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch43

calib_packv5_041523_1651.root, FC#0, port C2

Entries	433
Mean	39.82
Std Dev	16.57

Turn on : 24.9290

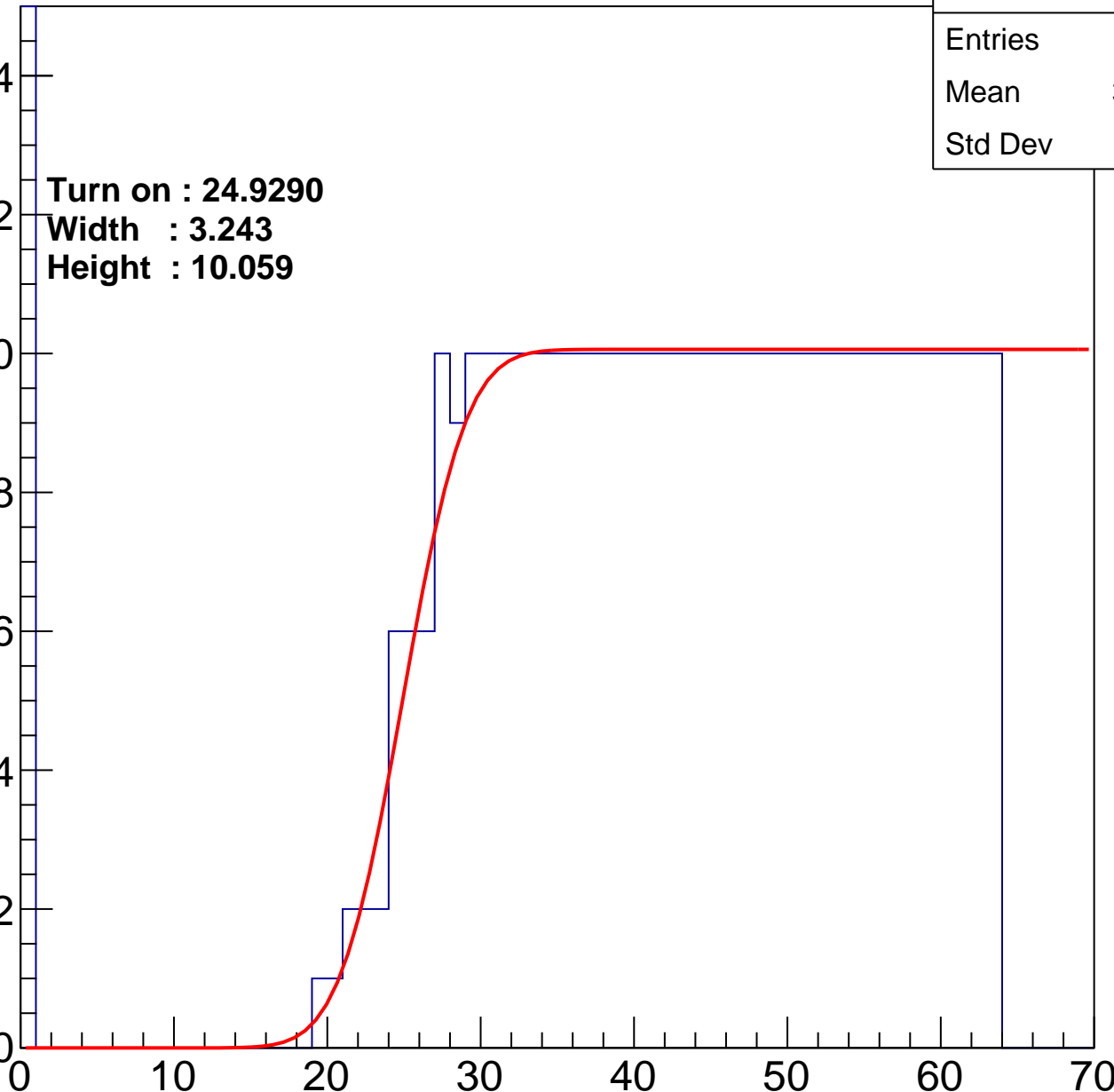
Width : 3.243

Height : 10.059

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch44

calib_packv5_041523_1651.root, FC#0, port C2

Entries	417
Mean	40.13
Std Dev	17.03

Turn on : 26.8355

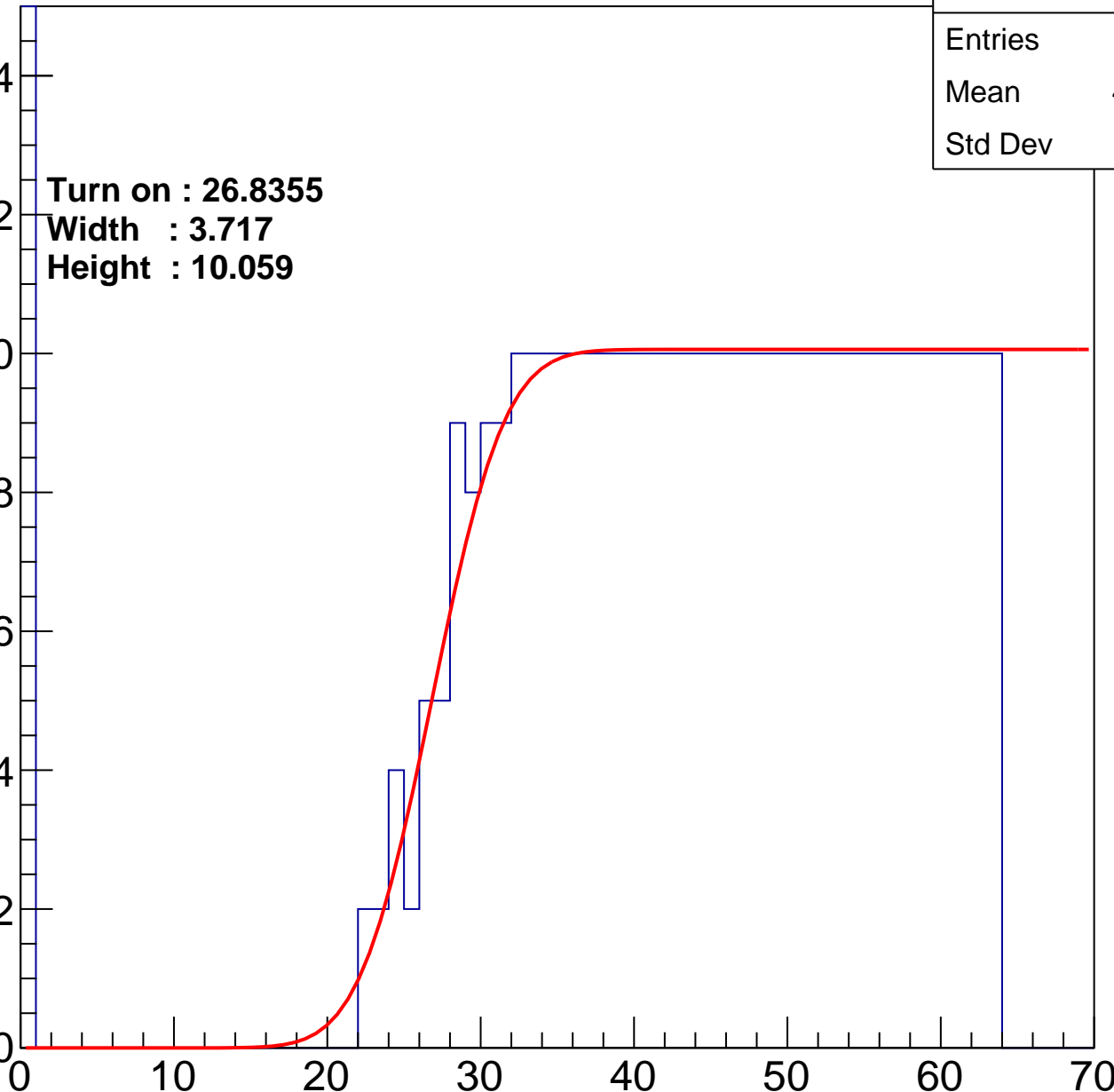
Width : 3.717

Height : 10.059

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch45

calib_packv5_041523_1651.root, FC#0, port C2

Entries	413
Mean	40.35
Std Dev	16.94

Turn on : 27.4148

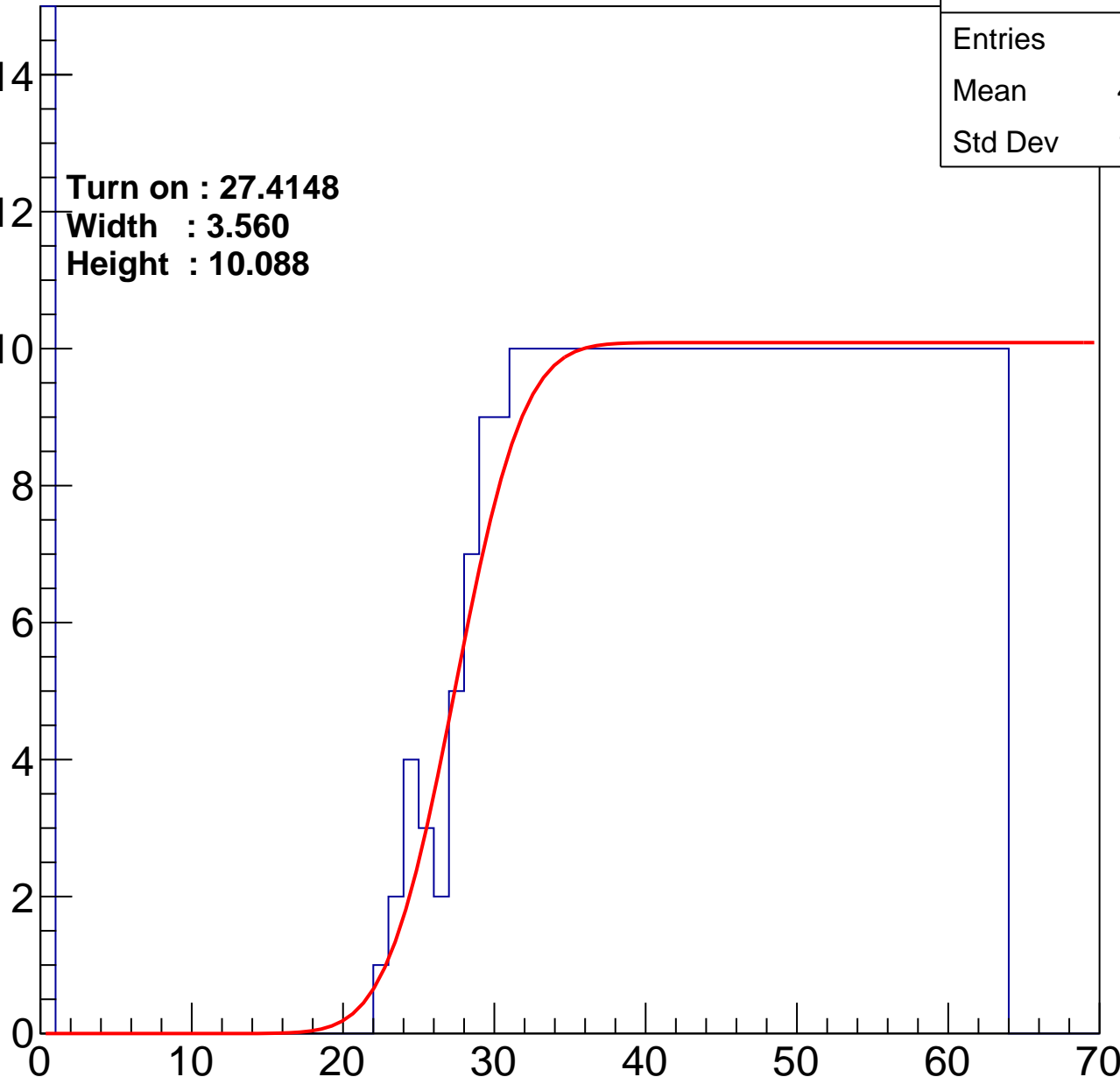
Width : 3.560

Height : 10.088

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch46

calib_packv5_041523_1651.root, FC#0, port C2

Entries	417
Mean	40.36
Std Dev	16.69

Turn on : 26.4220

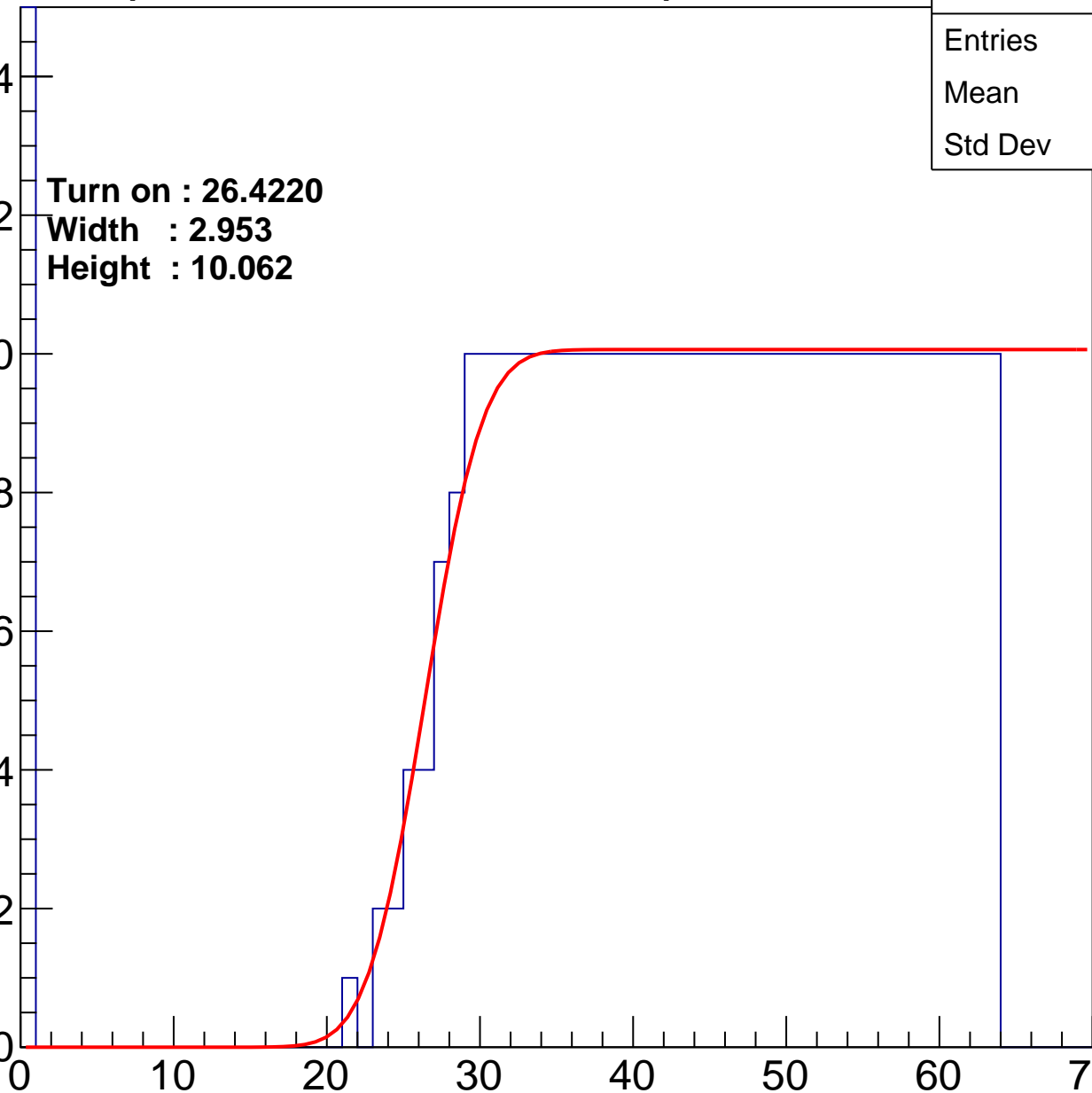
Width : 2.953

Height : 10.062

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch47

calib_packv5_041523_1651.root, FC#0, port C2

Entries	404
Mean	40.78
Std Dev	16.78

Turn on : 26.7055

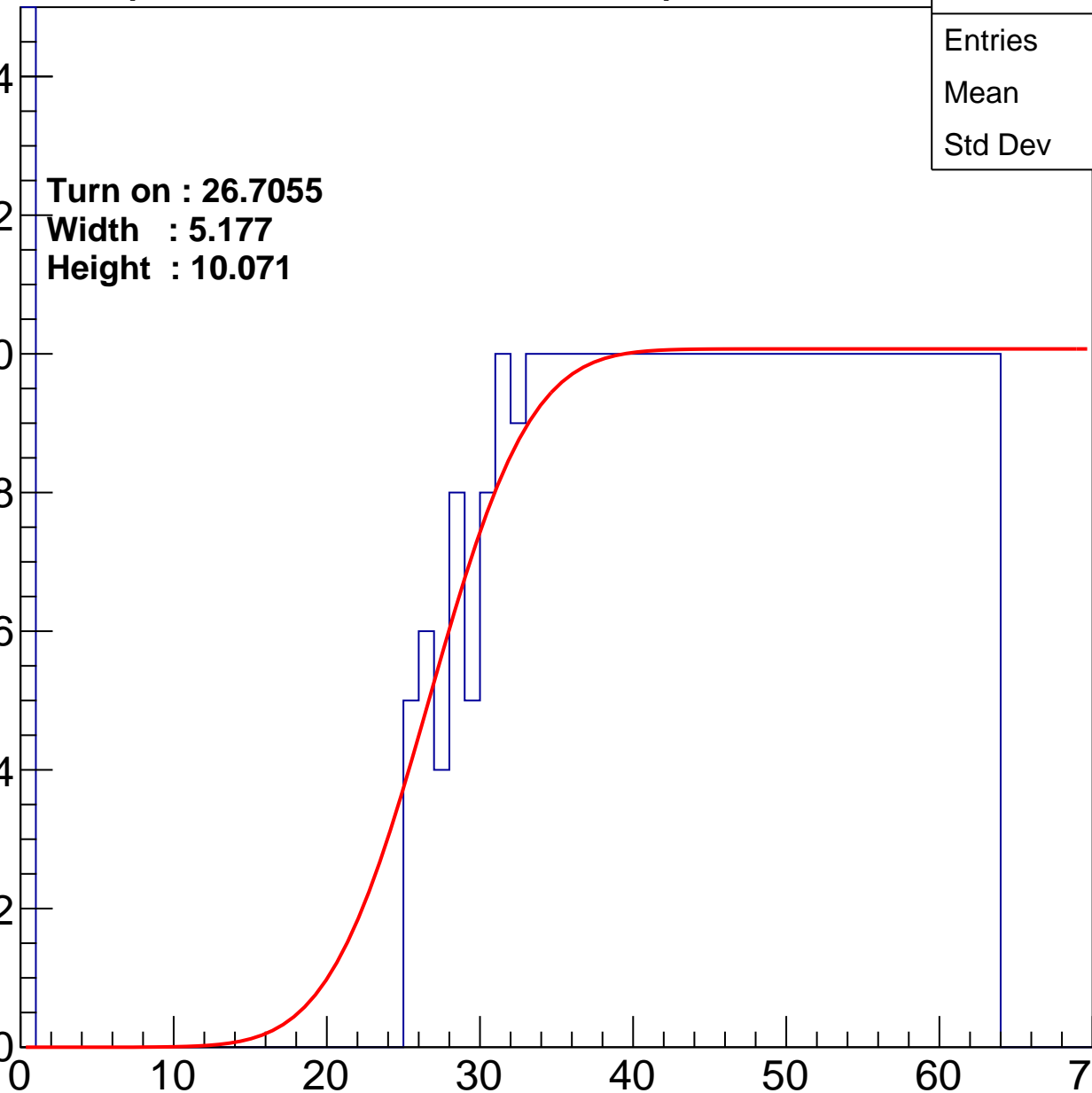
Width : 5.177

Height : 10.071

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch48

calib_packv5_041523_1651.root, FC#0, port C2

Entries	403
Mean	40.37
Std Dev	17.45

Turn on : 28.8146

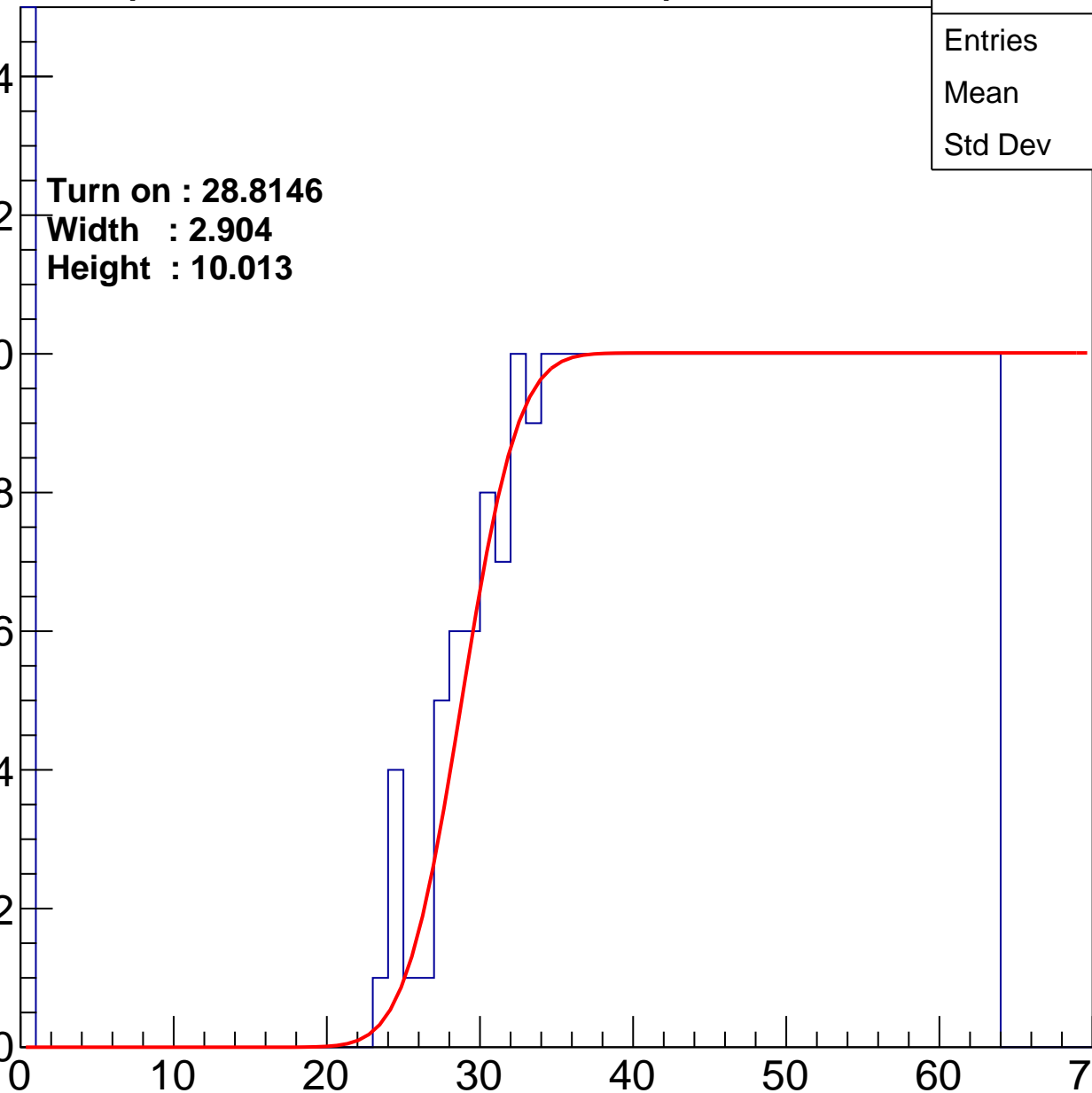
Width : 2.904

Height : 10.013

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch49

calib_packv5_041523_1651.root, FC#0, port C2

Entries	417
Mean	40.2
Std Dev	16.92

Turn on : 26.7690

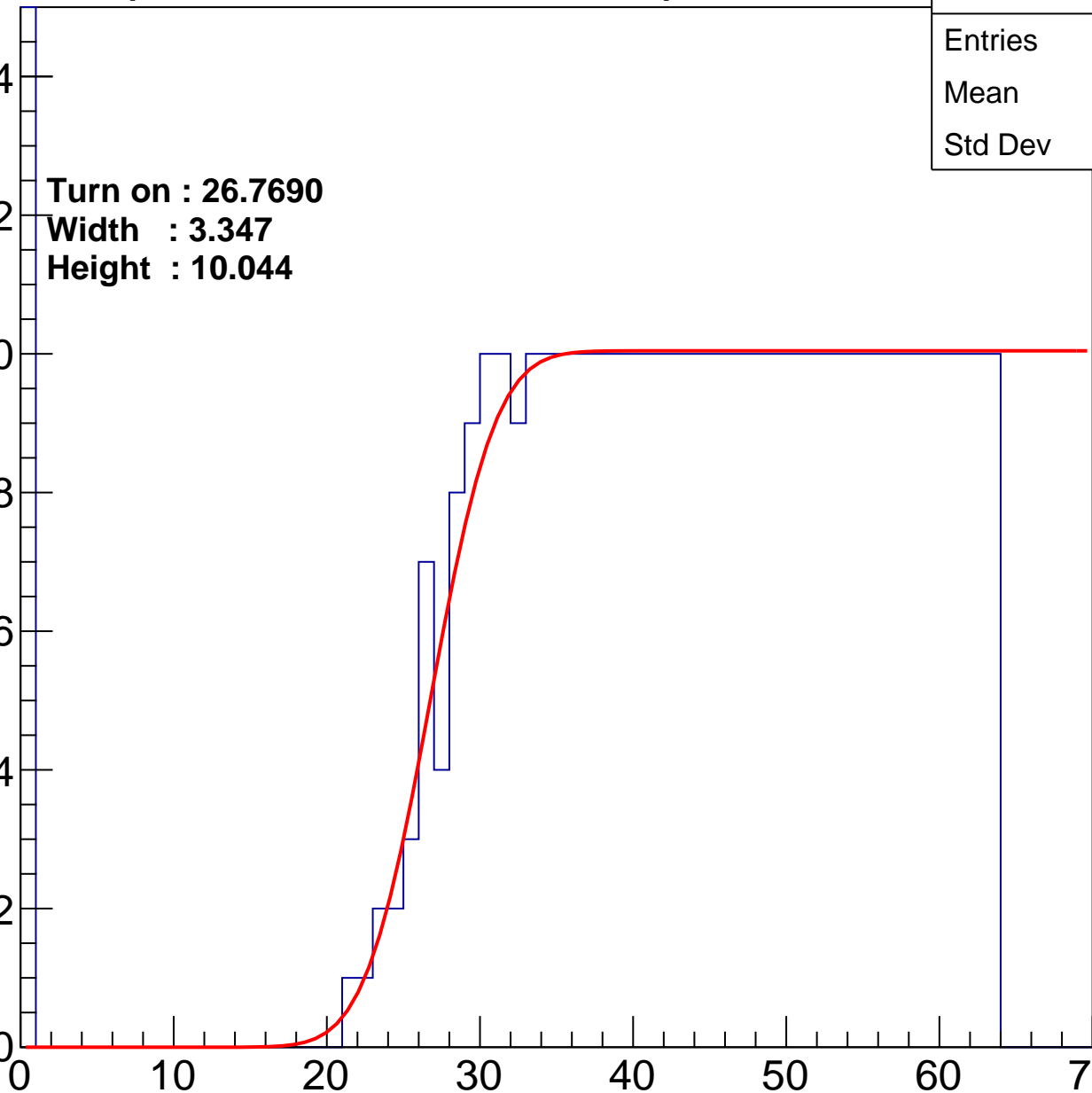
Width : 3.347

Height : 10.044

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch50

calib_packv5_041523_1651.root, FC#0, port C2

Entries	424
Mean	40
Std Dev	16.81

Turn on : 25.9790

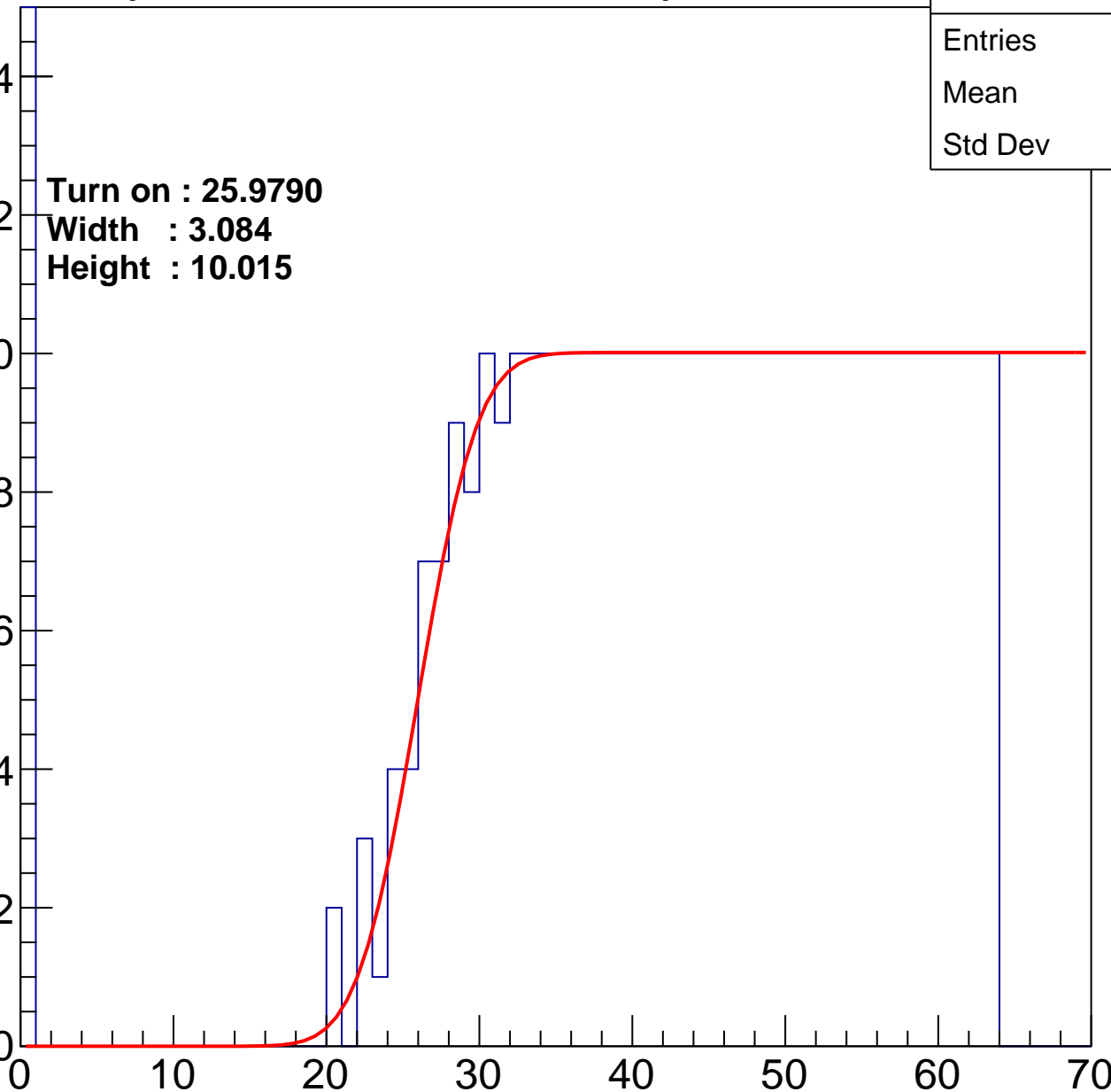
Width : 3.084

Height : 10.015

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch51

calib_packv5_041523_1651.root, FC#0, port C2

Entries	416
Mean	40.69
Std Dev	16.13

Turn on : 25.7341

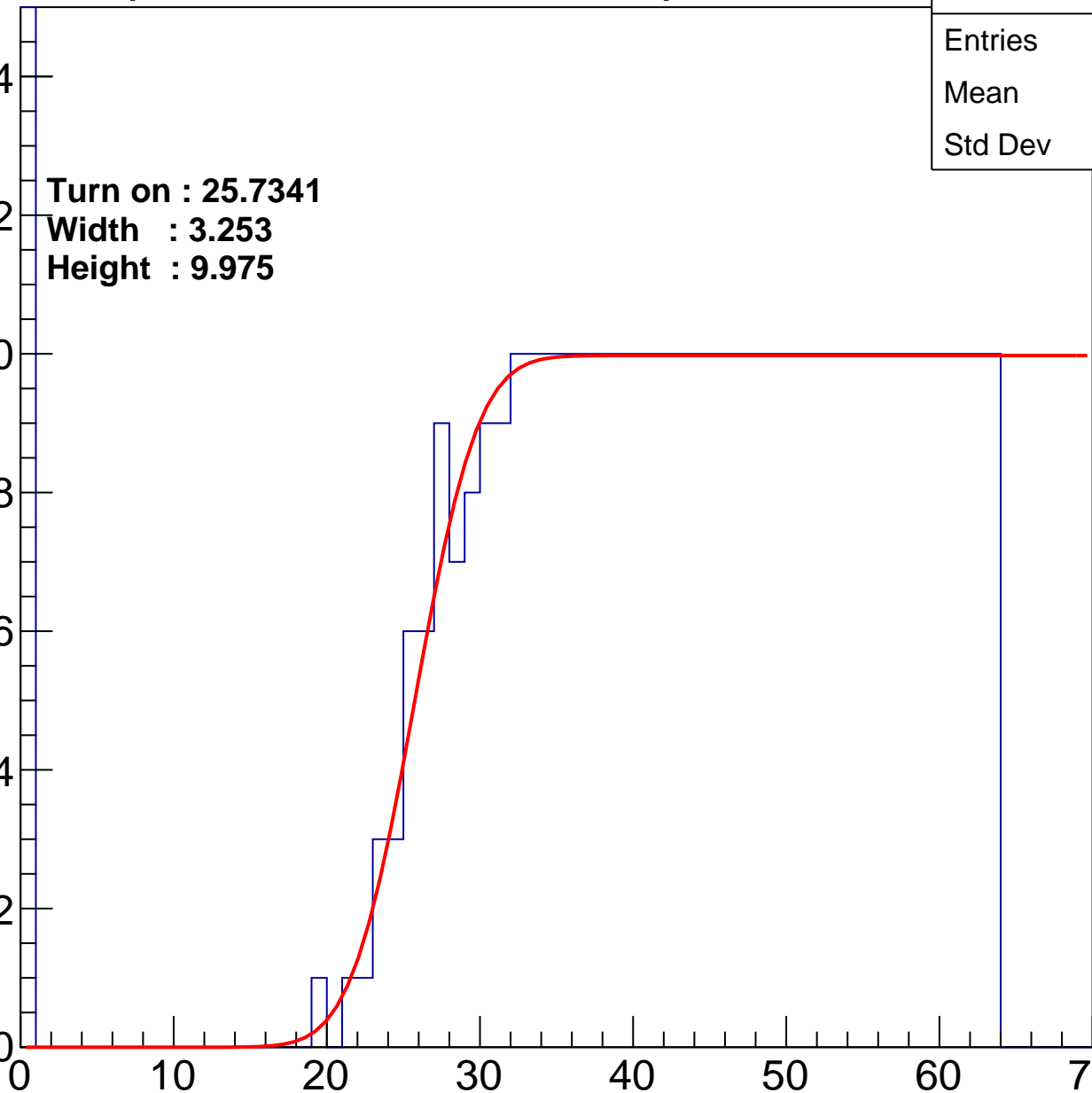
Width : 3.253

Height : 9.975

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch52

calib_packv5_041523_1651.root, FC#0, port C2

Entries	436
Mean	40.1
Std Dev	15.9

Turn on : 23.8247

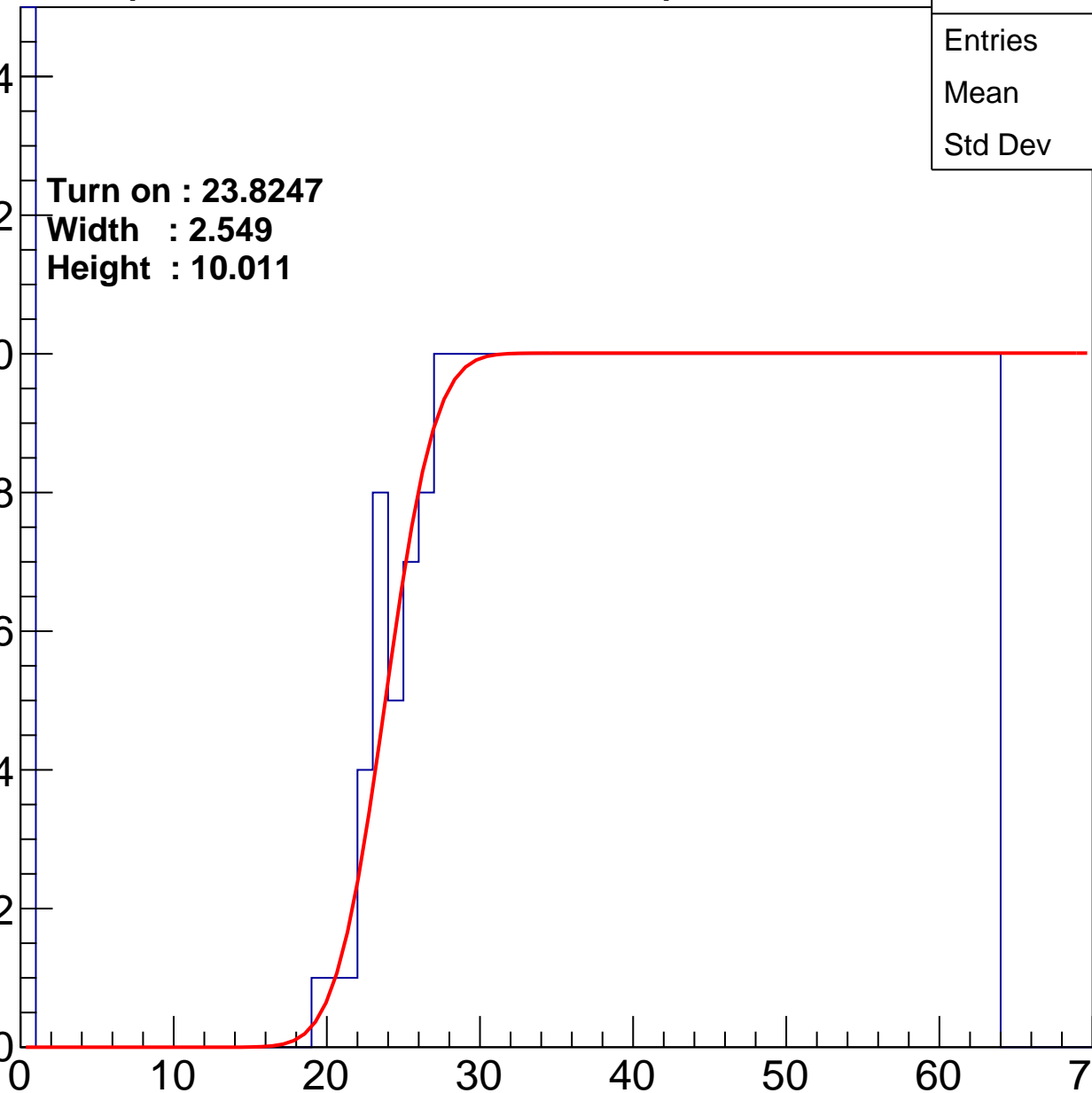
Width : 2.549

Height : 10.011

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch53

calib_packv5_041523_1651.root, FC#0, port C2

Entries	431
Mean	39.1
Std Dev	17.79

Turn on : 26.0834

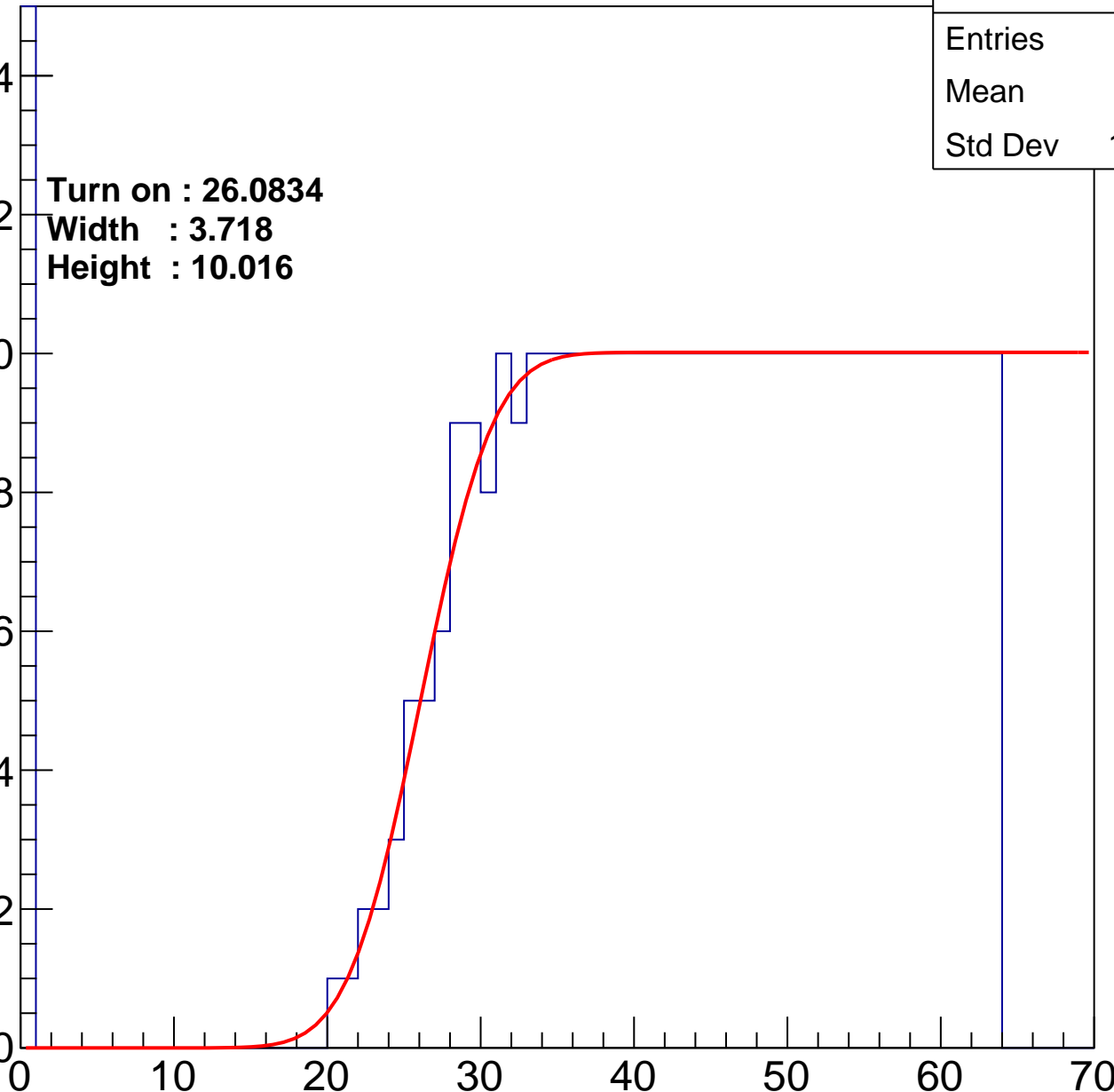
Width : 3.718

Height : 10.016

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch54

calib_packv5_041523_1651.root, FC#0, port C2

Entries	422
Mean	39.55
Std Dev	17.64

Turn on : 26.7960

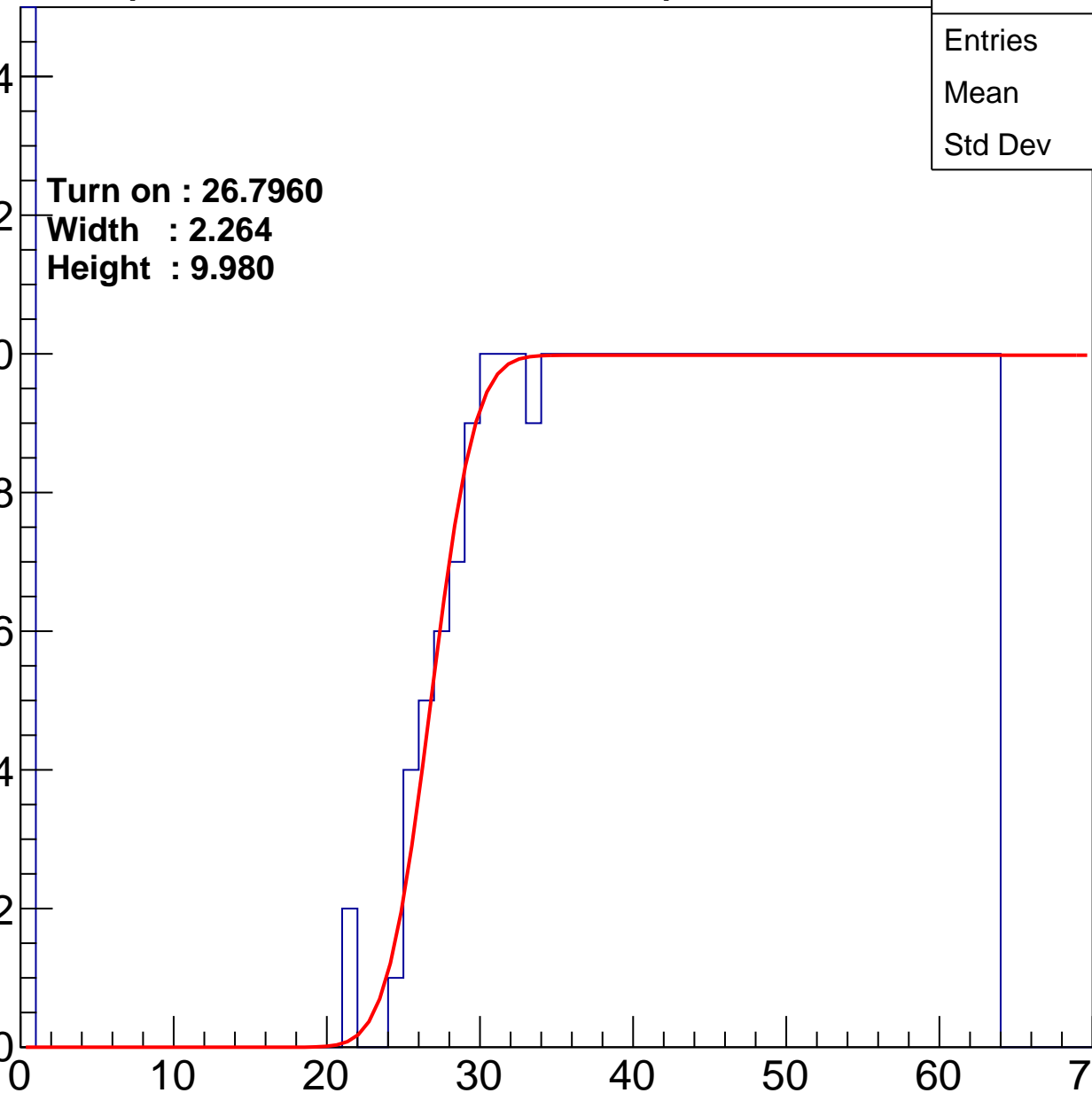
Width : 2.264

Height : 9.980

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch55

calib_packv5_041523_1651.root, FC#0, port C2

Entries	407
Mean	40.38
Std Dev	17.26

Turn on : 27.6424

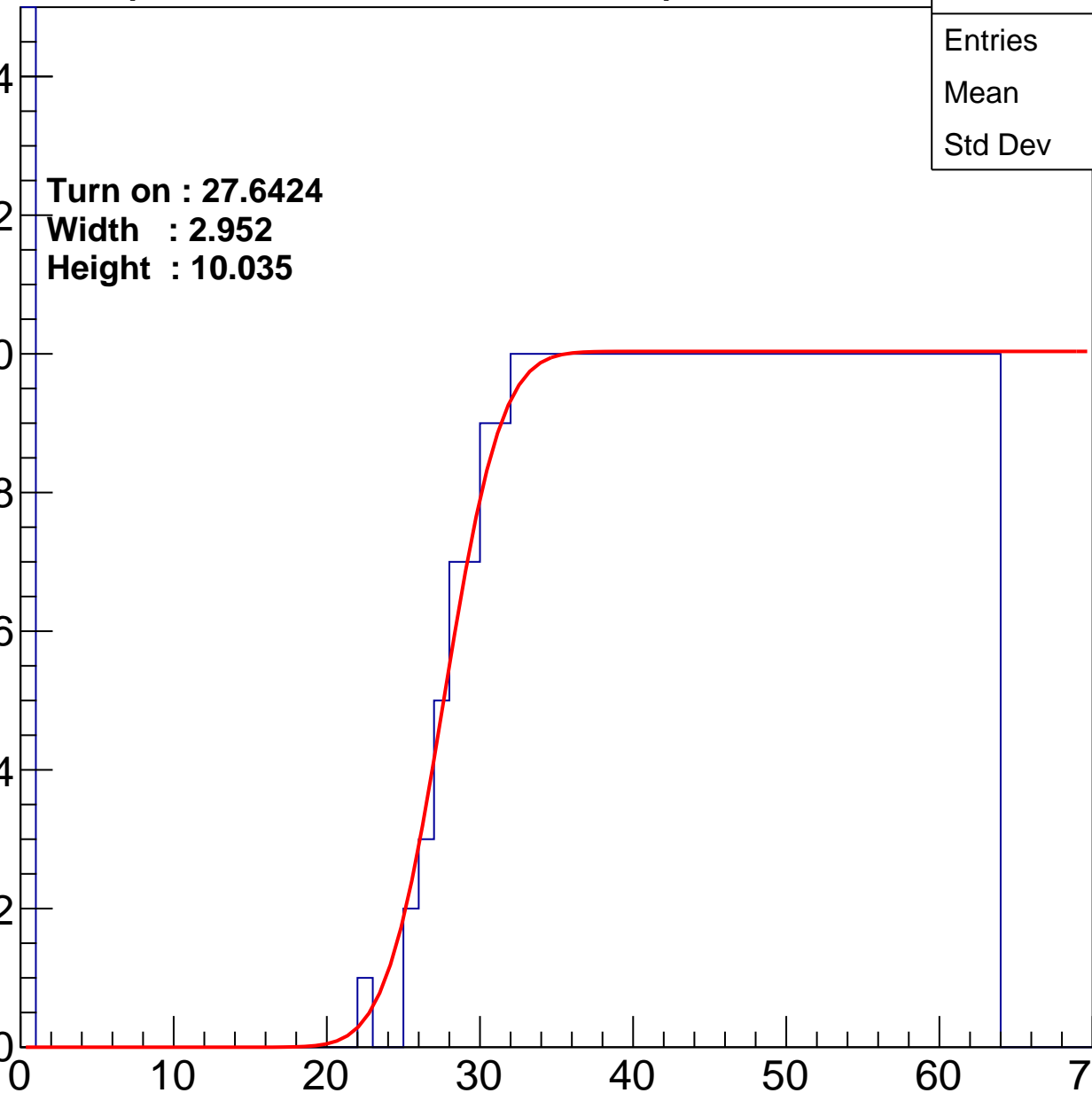
Width : 2.952

Height : 10.035

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch56

calib_packv5_041523_1651.root, FC#0, port C2

Entries	428
Mean	39.88
Std Dev	16.77

Turn on : 25.6489

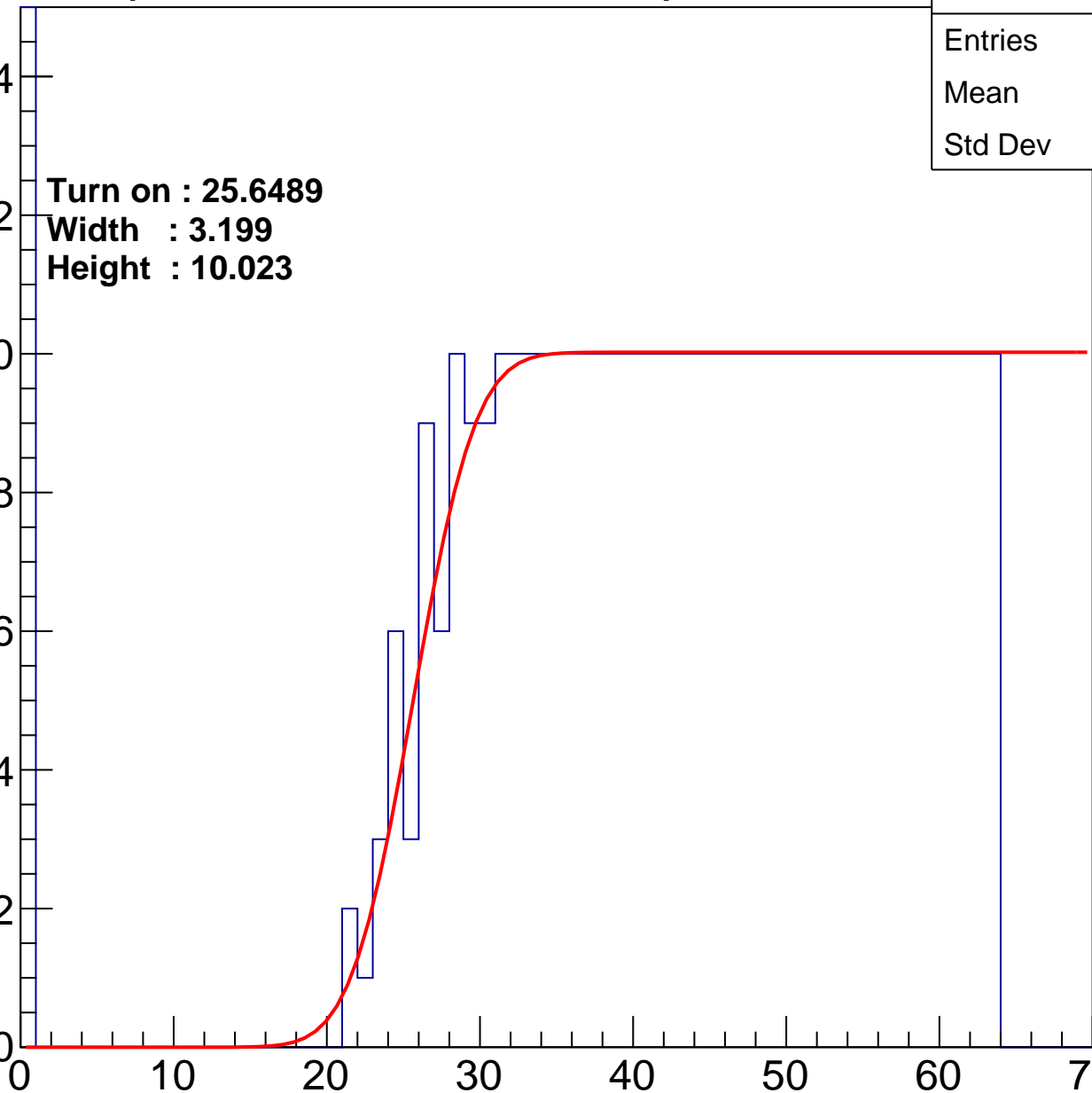
Width : 3.199

Height : 10.023

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch57

calib_packv5_041523_1651.root, FC#0, port C2

Entries	422
Mean	40.28
Std Dev	16.49

Turn on : 25.8786

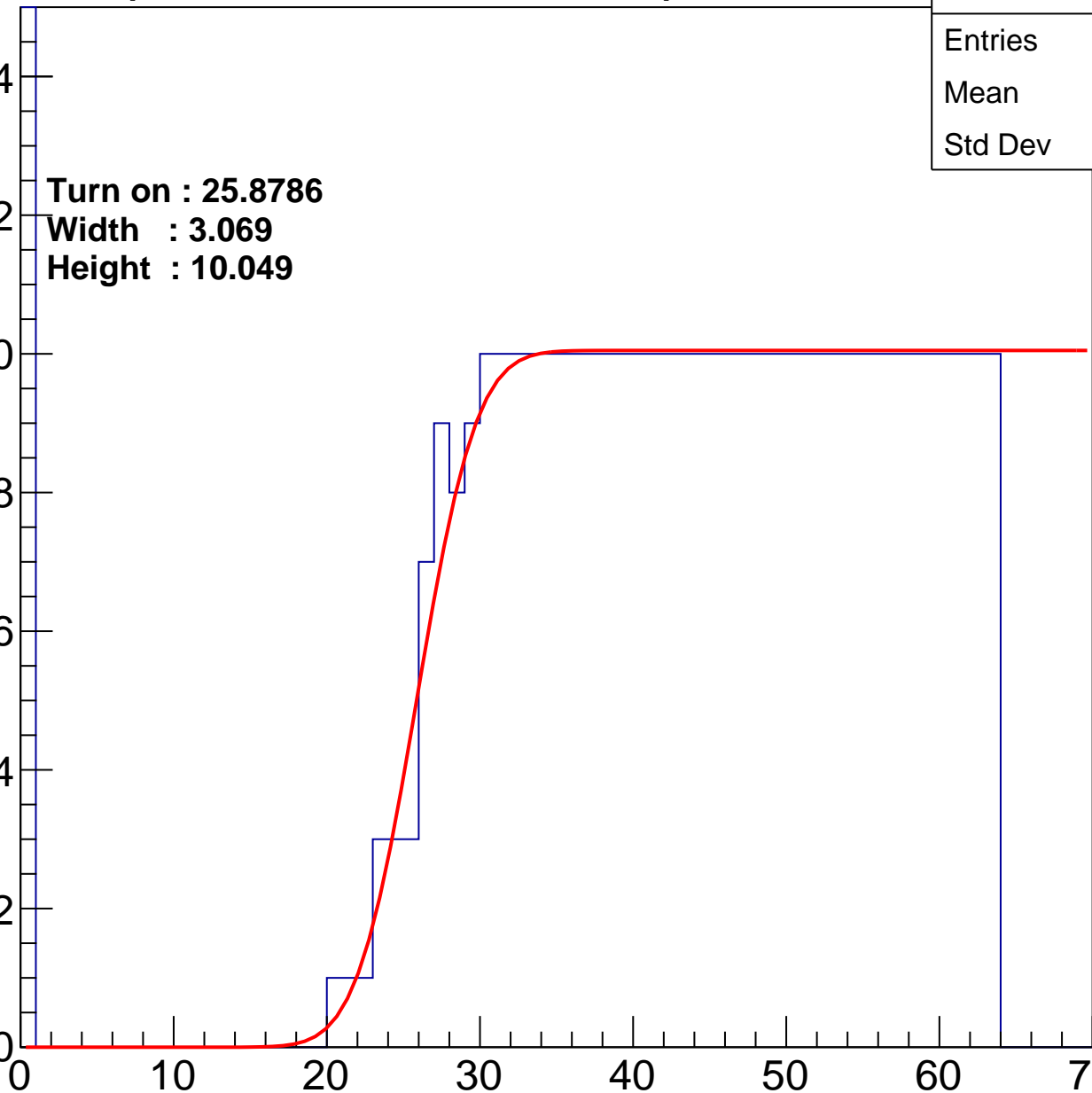
Width : 3.069

Height : 10.049

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch58

calib_packv5_041523_1651.root, FC#0, port C2

Entries	438
Mean	39.69
Std Dev	16.48

Turn on : 23.4699

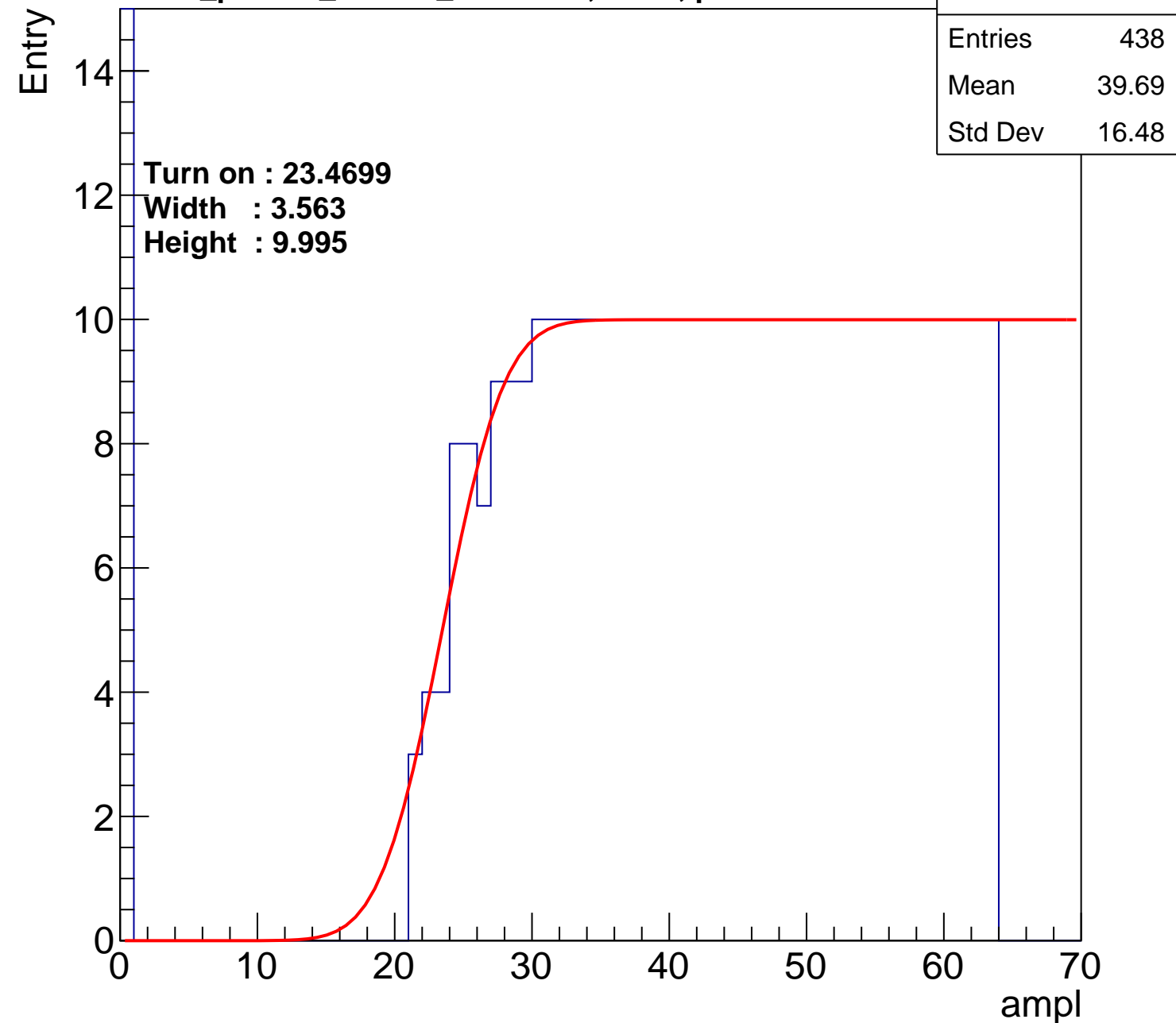
Width : 3.563

Height : 9.995

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch59

calib_packv5_041523_1651.root, FC#0, port C2

Entries	421
Mean	40.29
Std Dev	16.57

Turn on : 26.1397

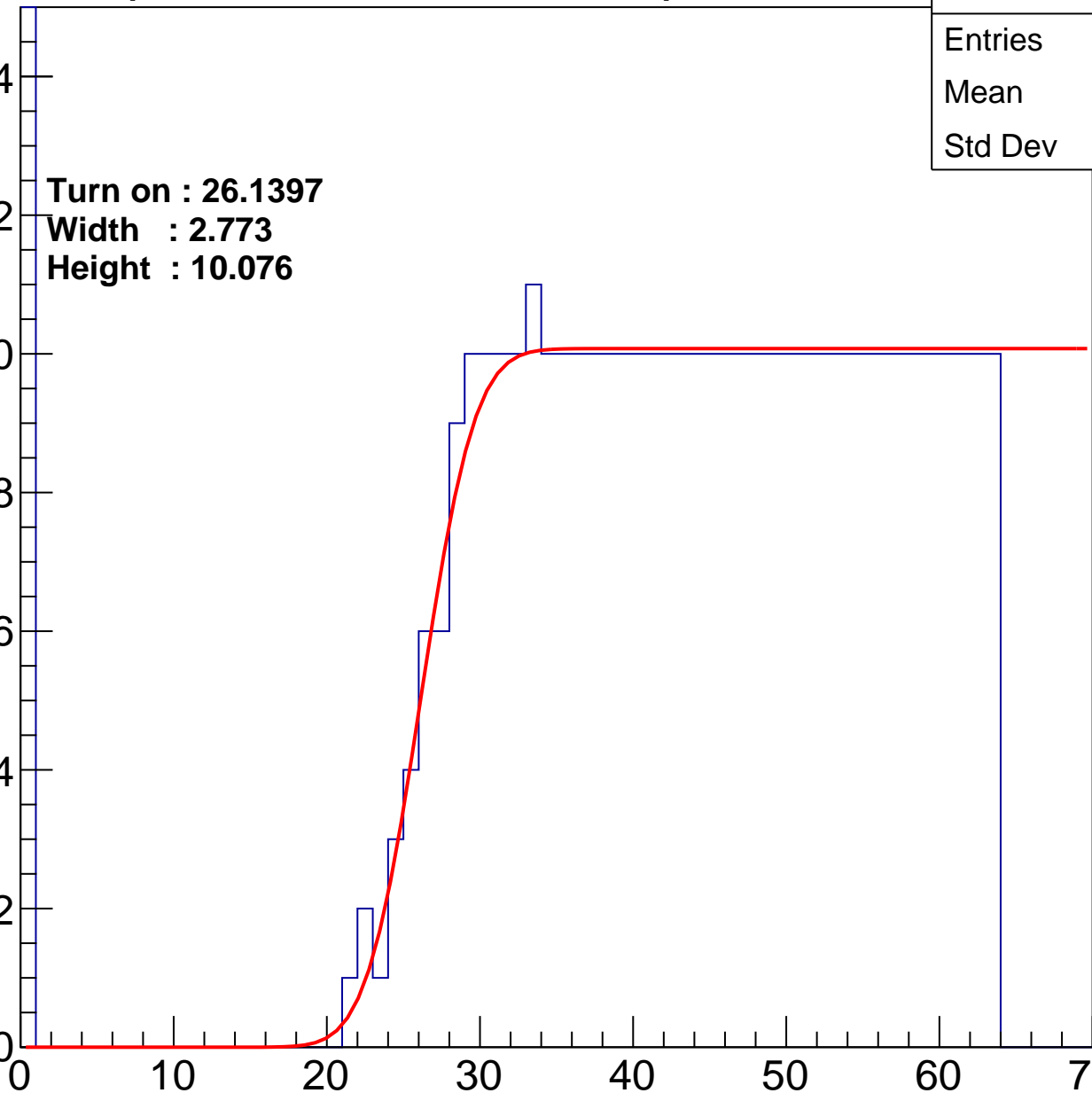
Width : 2.773

Height : 10.076

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch60

calib_packv5_041523_1651.root, FC#0, port C2

Entries	424
Mean	39.85
Std Dev	17.07

Turn on : 25.9530

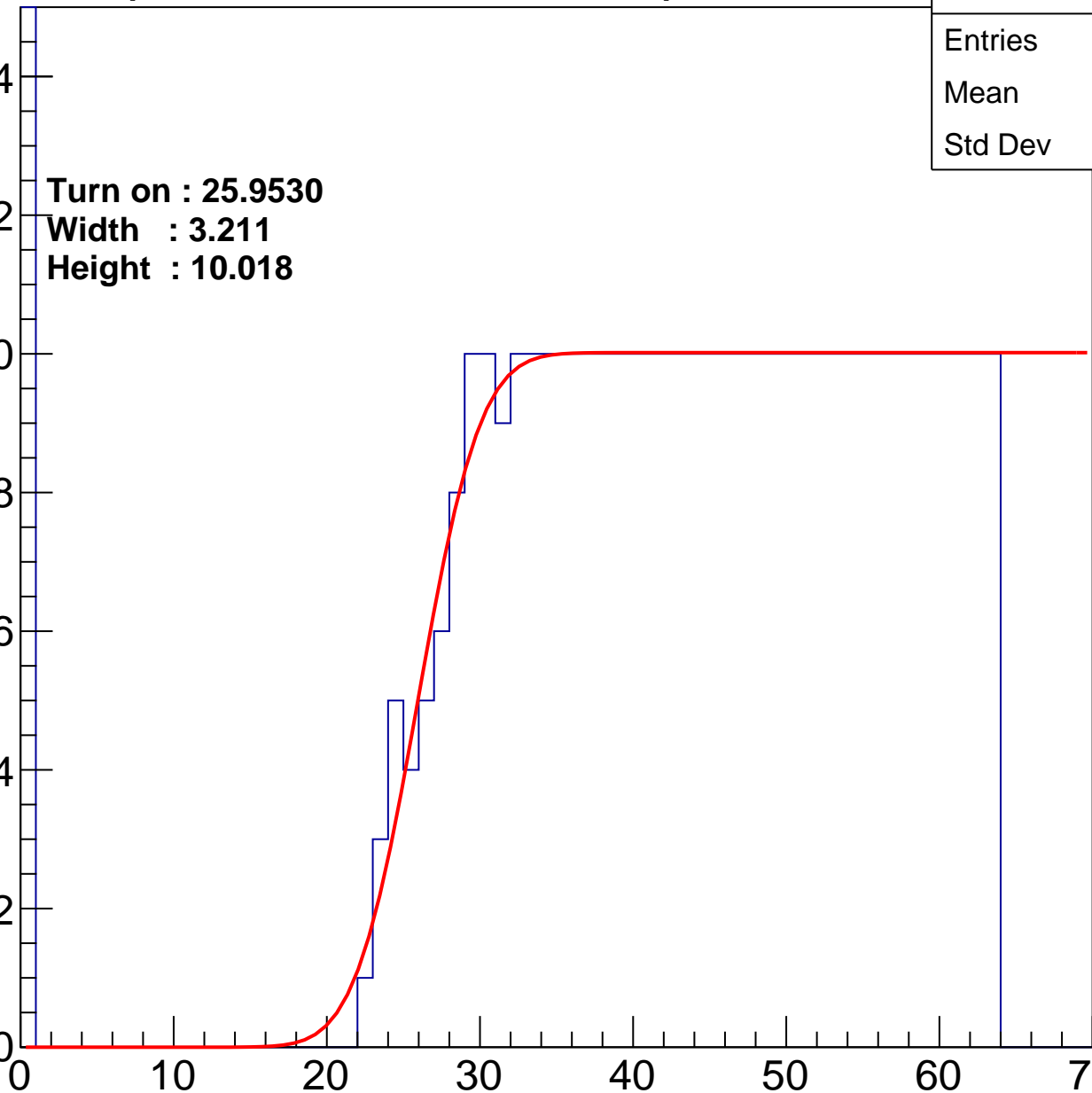
Width : 3.211

Height : 10.018

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch61

calib_packv5_041523_1651.root, FC#0, port C2

Entries	423
Mean	40.07
Std Dev	16.78

Turn on : 26.1114

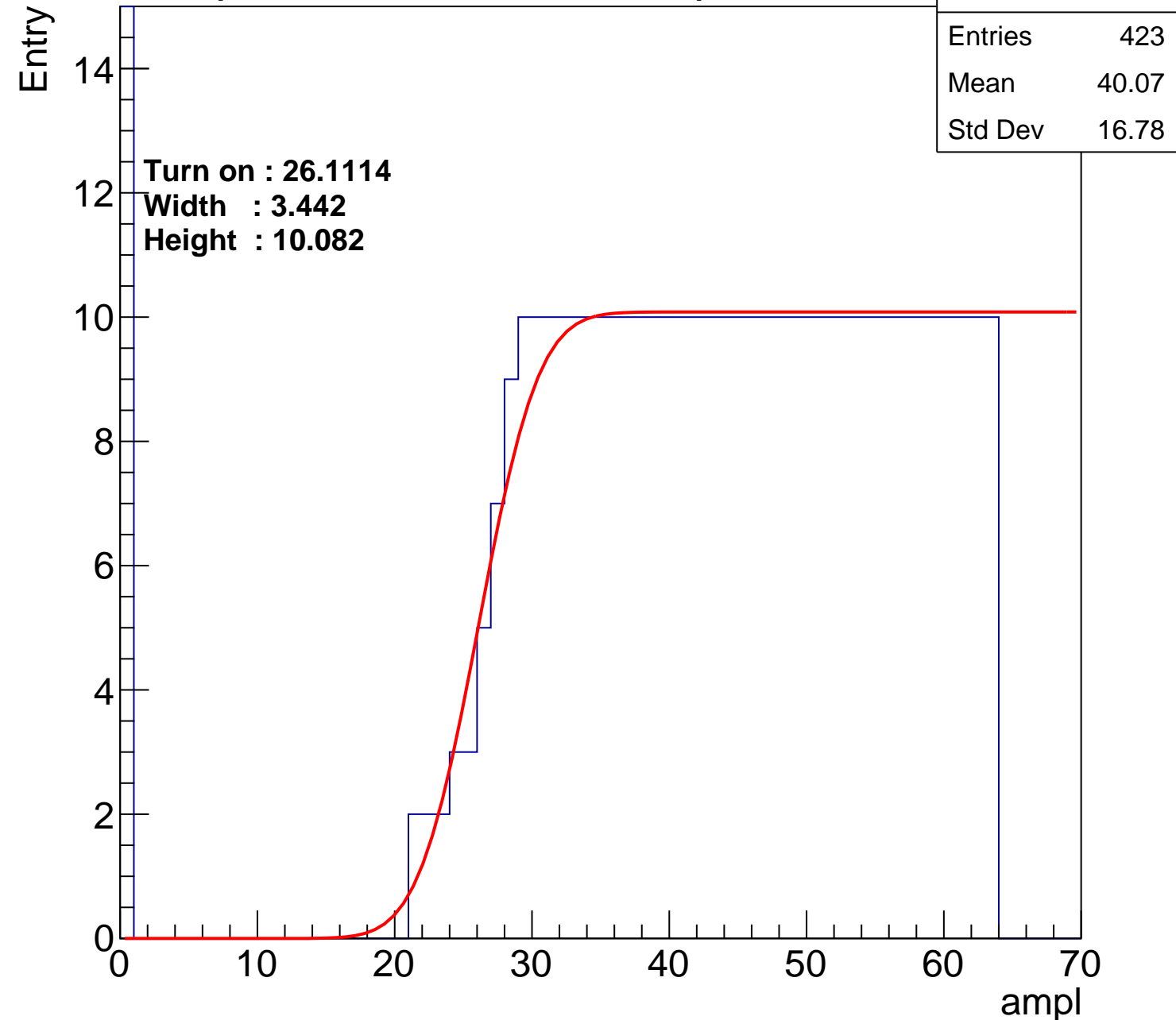
Width : 3.442

Height : 10.082

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch62

calib_packv5_041523_1651.root, FC#0, port C2

Entries	415
Mean	40.67
Std Dev	16.29

Turn on : 26.0698

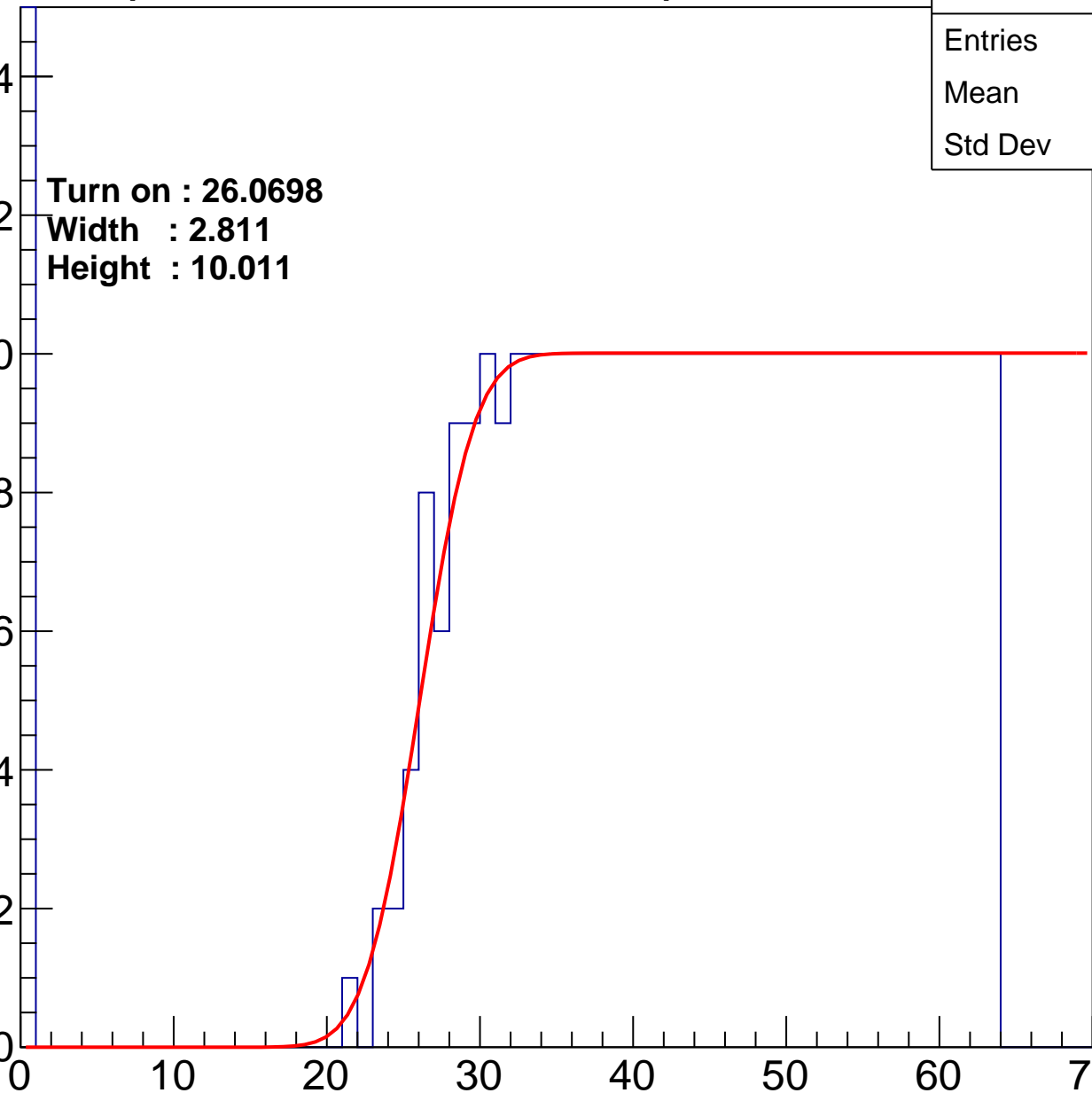
Width : 2.811

Height : 10.011

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch63

calib_packv5_041523_1651.root, FC#0, port C2

Entries	407
Mean	41.1
Std Dev	16.08

Turn on : 26.8628

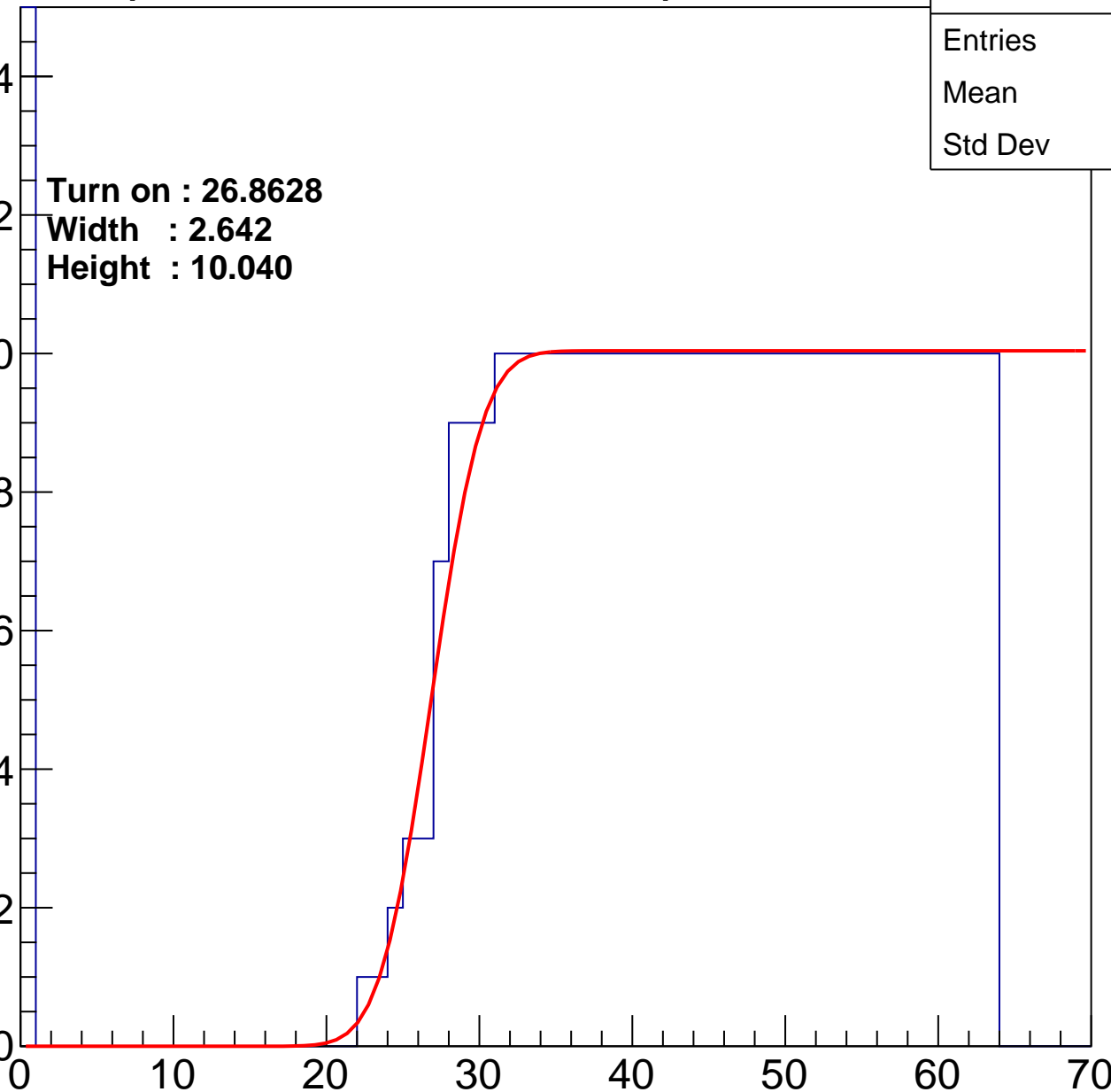
Width : 2.642

Height : 10.040

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch64

calib_packv5_041523_1651.root, FC#0, port C2

Entries	407
Mean	40.83
Std Dev	16.53

Turn on : 27.1228

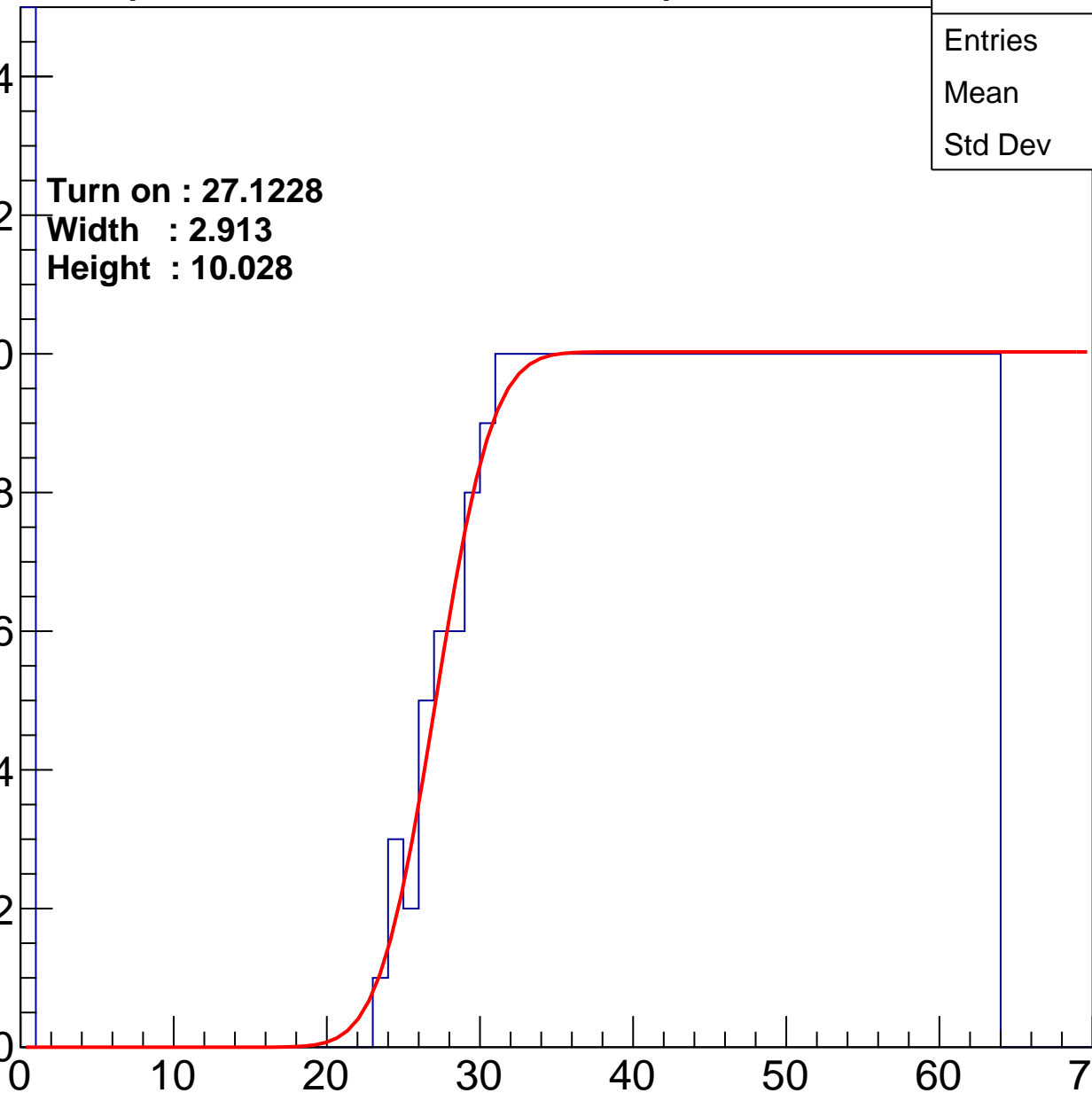
Width : 2.913

Height : 10.028

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch65

calib_packv5_041523_1651.root, FC#0, port C2

Entries	411
Mean	40.37
Std Dev	17.03

Turn on : 27.2268

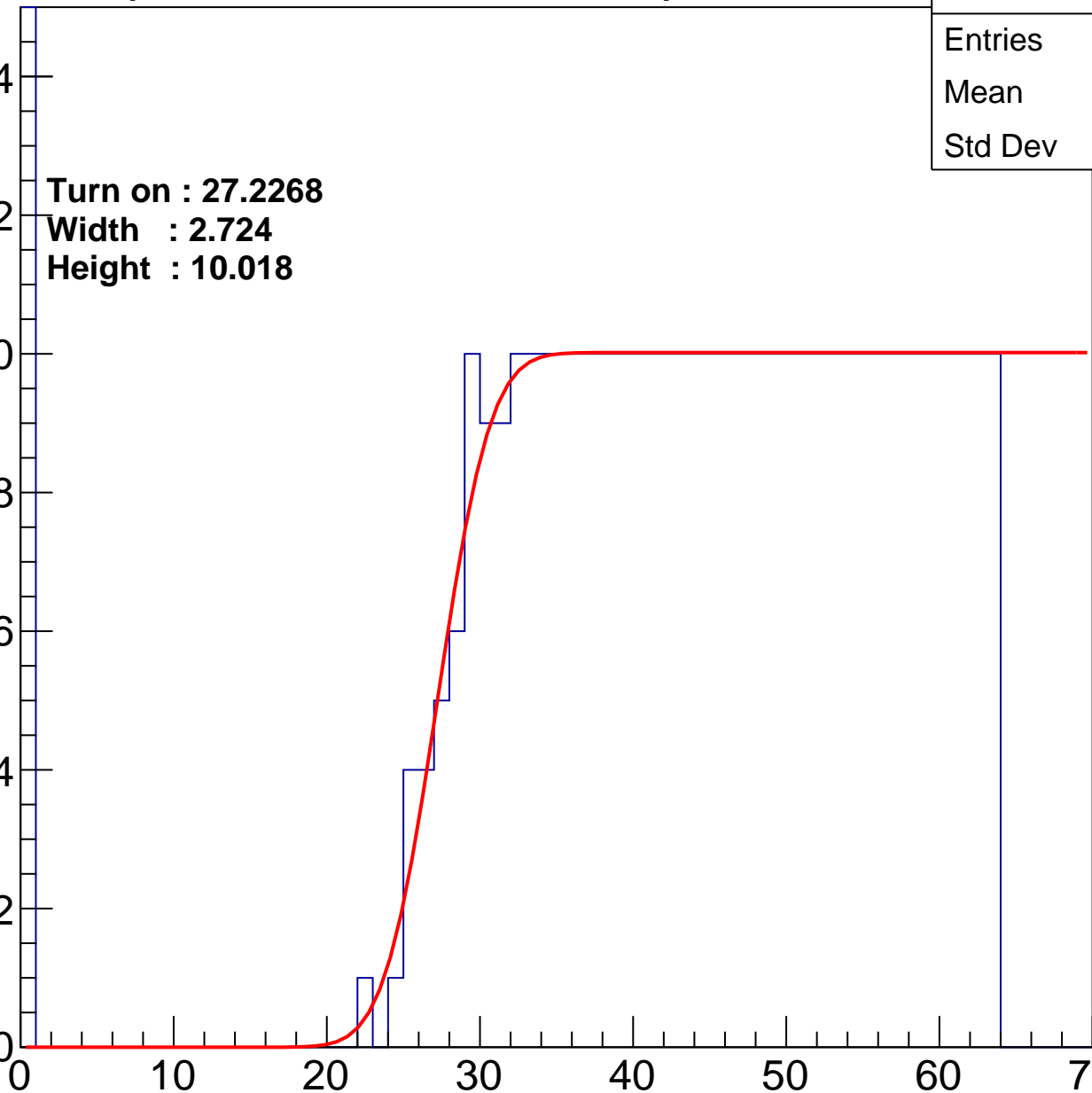
Width : 2.724

Height : 10.018

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch66

calib_packv5_041523_1651.root, FC#0, port C2

Entries	416
Mean	39.9
Std Dev	17.48

Turn on : 26.7183

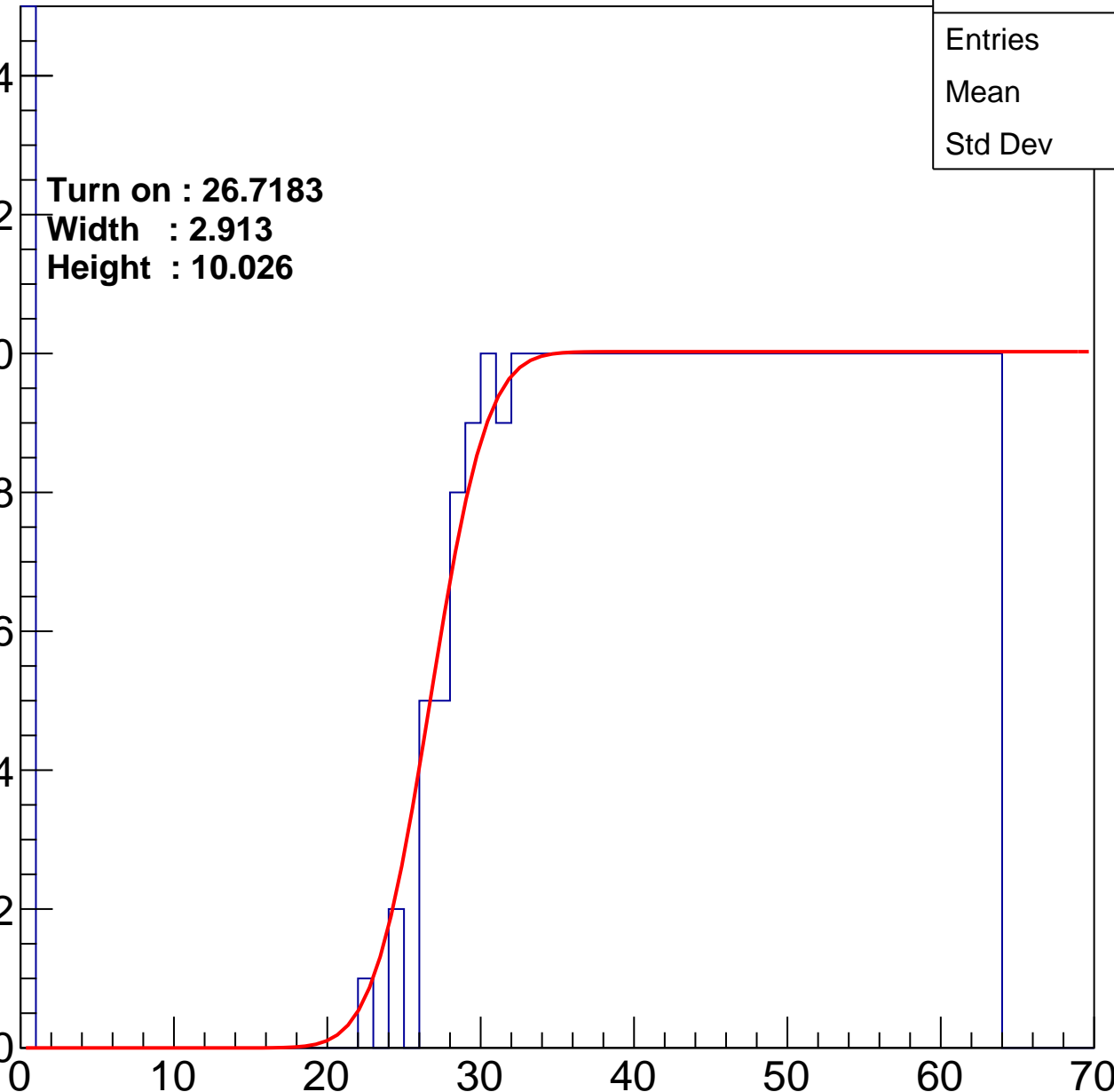
Width : 2.913

Height : 10.026

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch67

calib_packv5_041523_1651.root, FC#0, port C2

Entries	406
Mean	40.65
Std Dev	16.87

Turn on : 27.4507

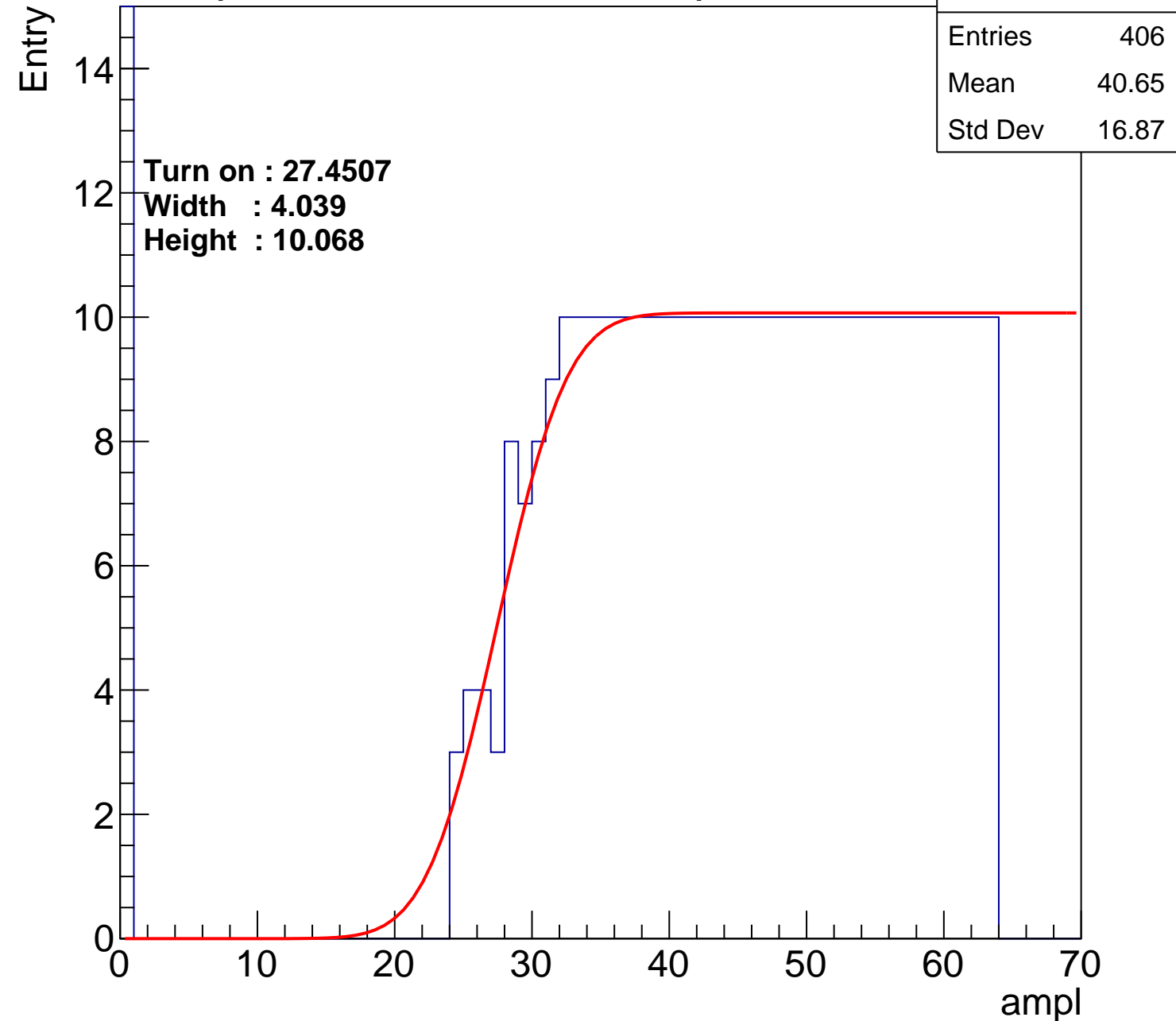
Width : 4.039

Height : 10.068

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch68

calib_packv5_041523_1651.root, FC#0, port C2

Entries	431
Mean	40.02
Std Dev	16.33

Turn on : 25.1044

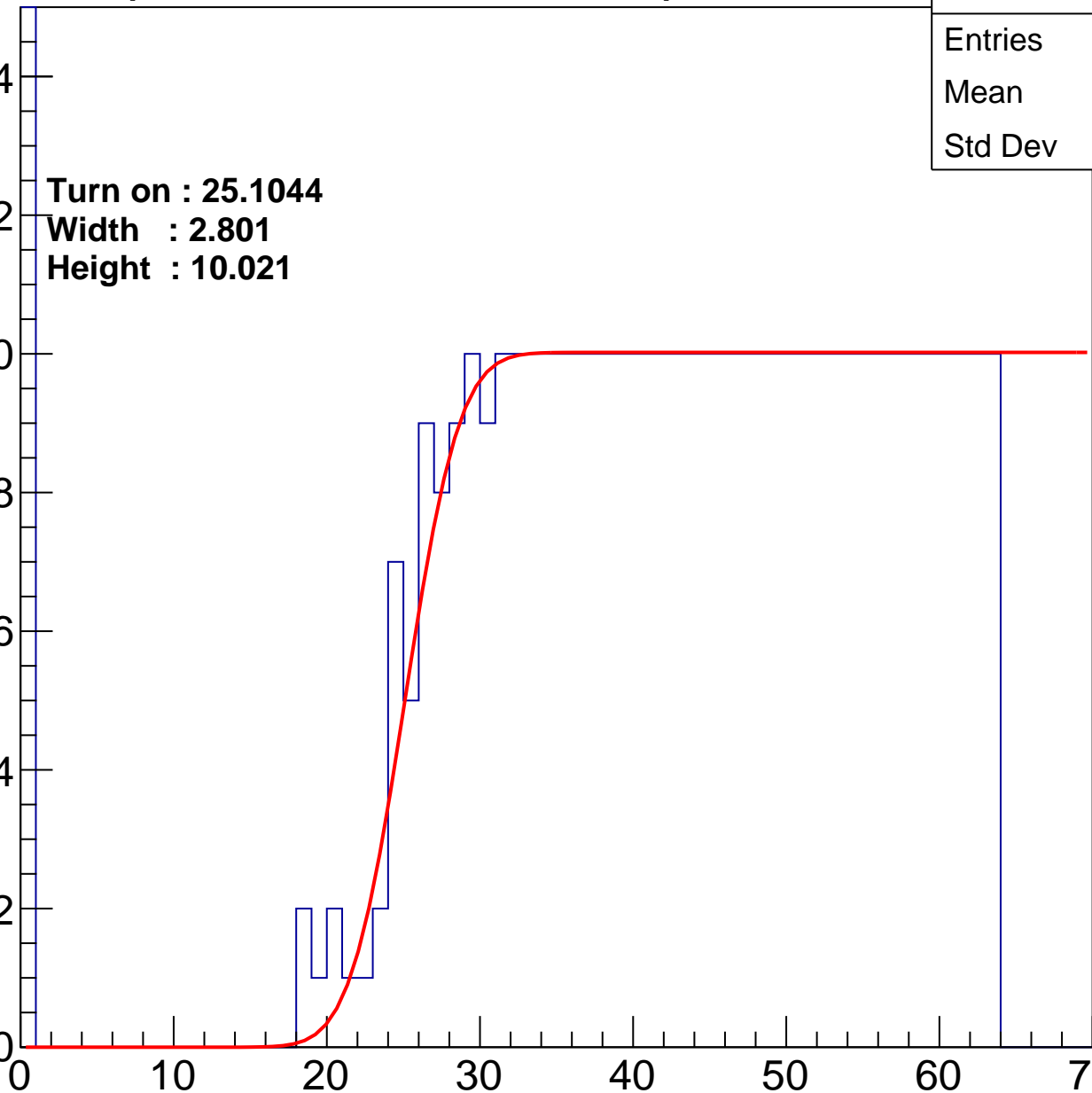
Width : 2.801

Height : 10.021

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch69

calib_packv5_041523_1651.root, FC#0, port C2

Entries	414
Mean	40
Std Dev	17.42

Turn on : 27.7541

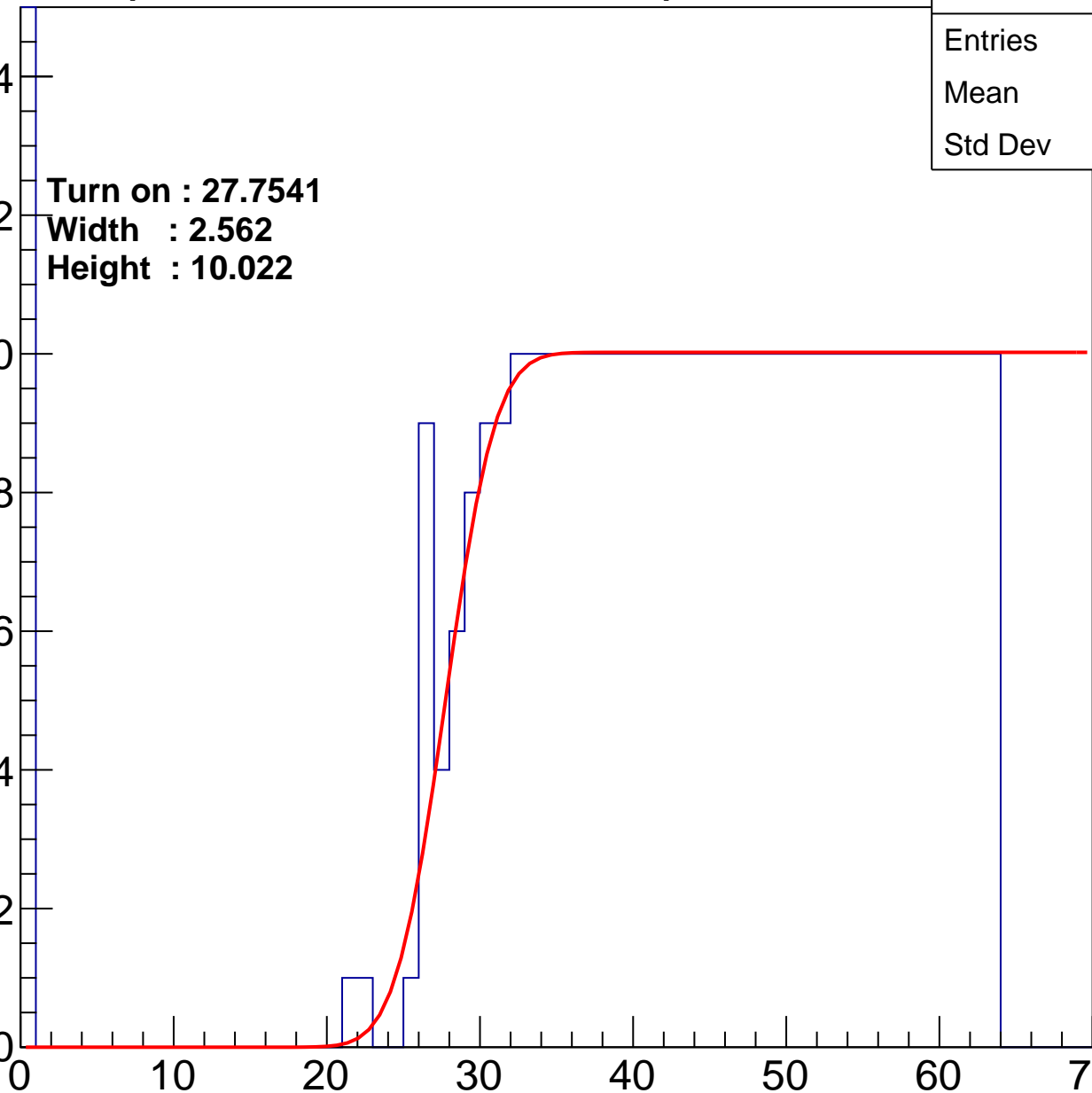
Width : 2.562

Height : 10.022

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch70

calib_packv5_041523_1651.root, FC#0, port C2

Entries	442
Mean	39.3
Std Dev	16.86

Turn on : 24.4274

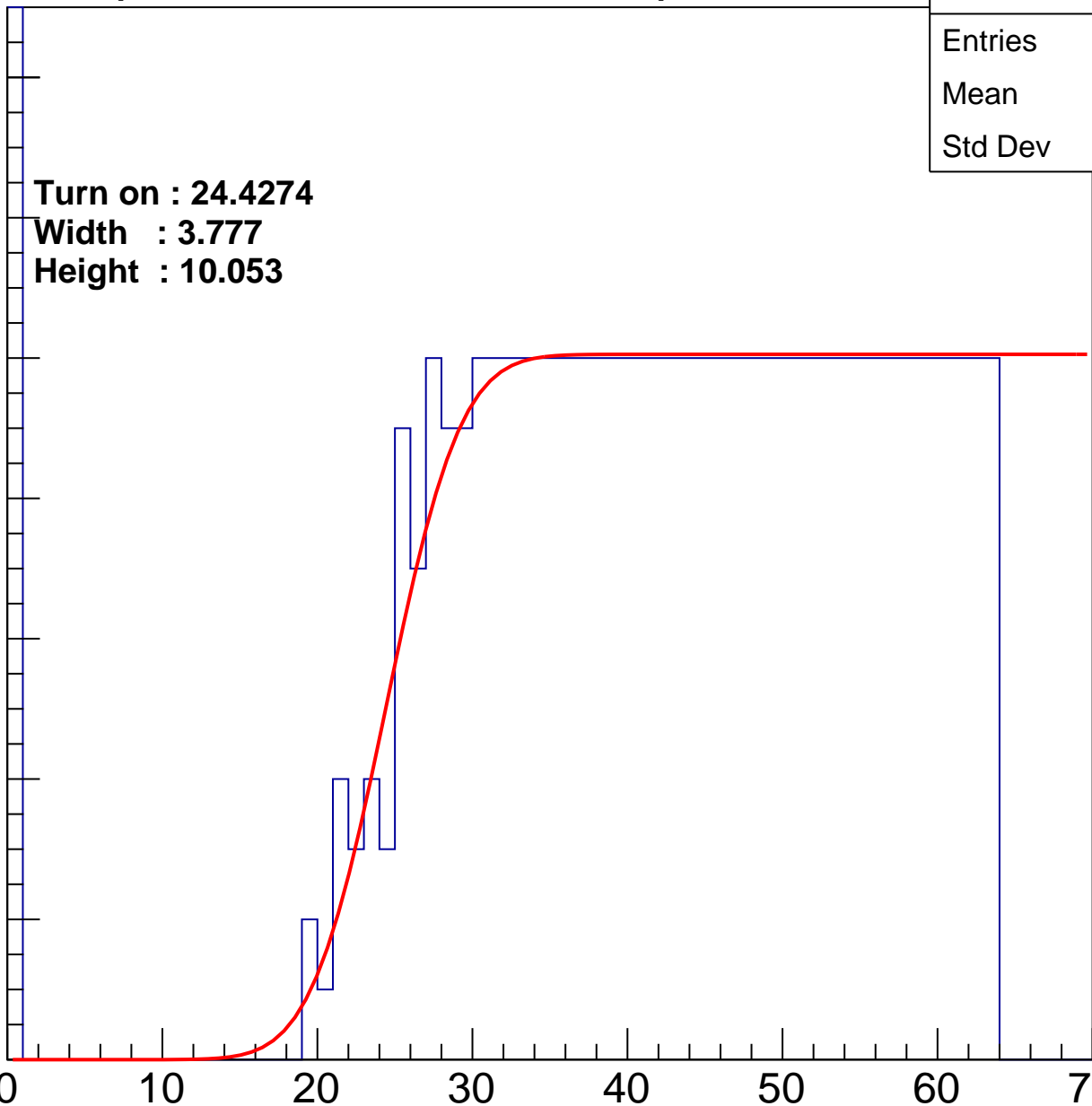
Width : 3.777

Height : 10.053

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch71

calib_packv5_041523_1651.root, FC#0, port C2

Entries	437
Mean	38.5
Std Dev	18.36

Turn on : 26.1033

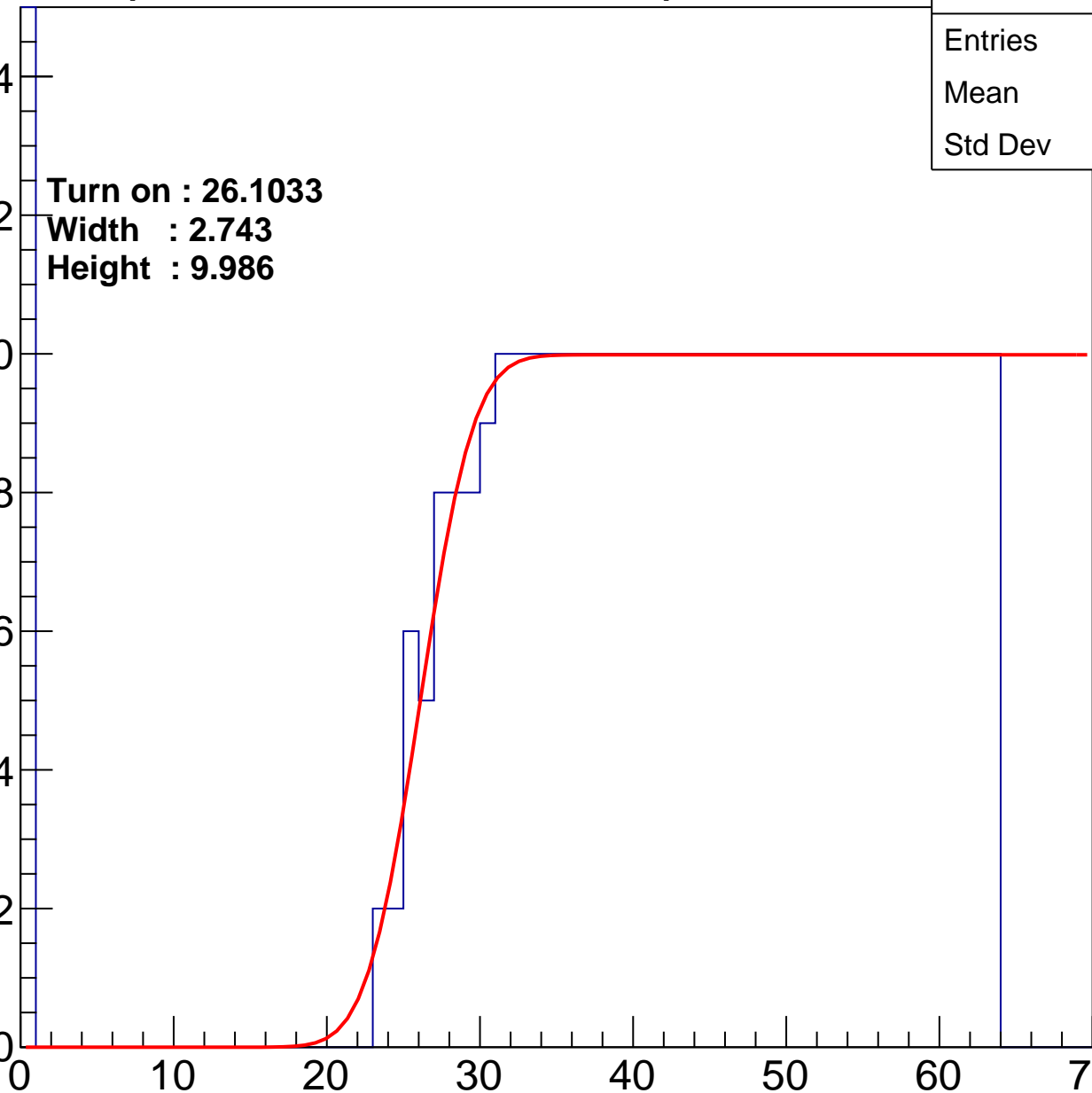
Width : 2.743

Height : 9.986

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch72

calib_packv5_041523_1651.root, FC#0, port C2

Entries	423
Mean	40.37
Std Dev	16.23

Turn on : 24.9684

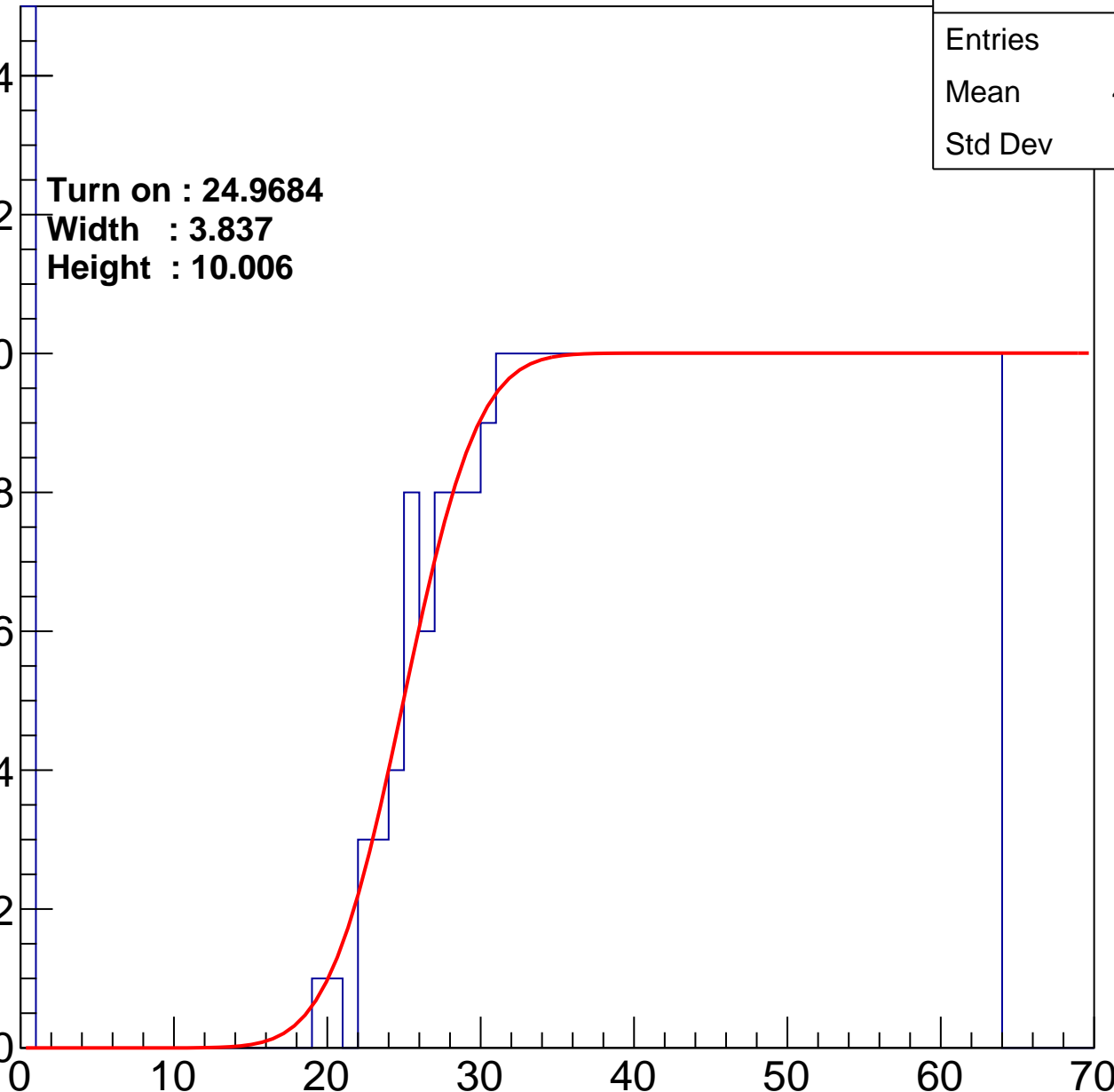
Width : 3.837

Height : 10.006

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch73

calib_packv5_041523_1651.root, FC#0, port C2

Entries	397
Mean	41.73
Std Dev	15.64

Turn on : 27.4077

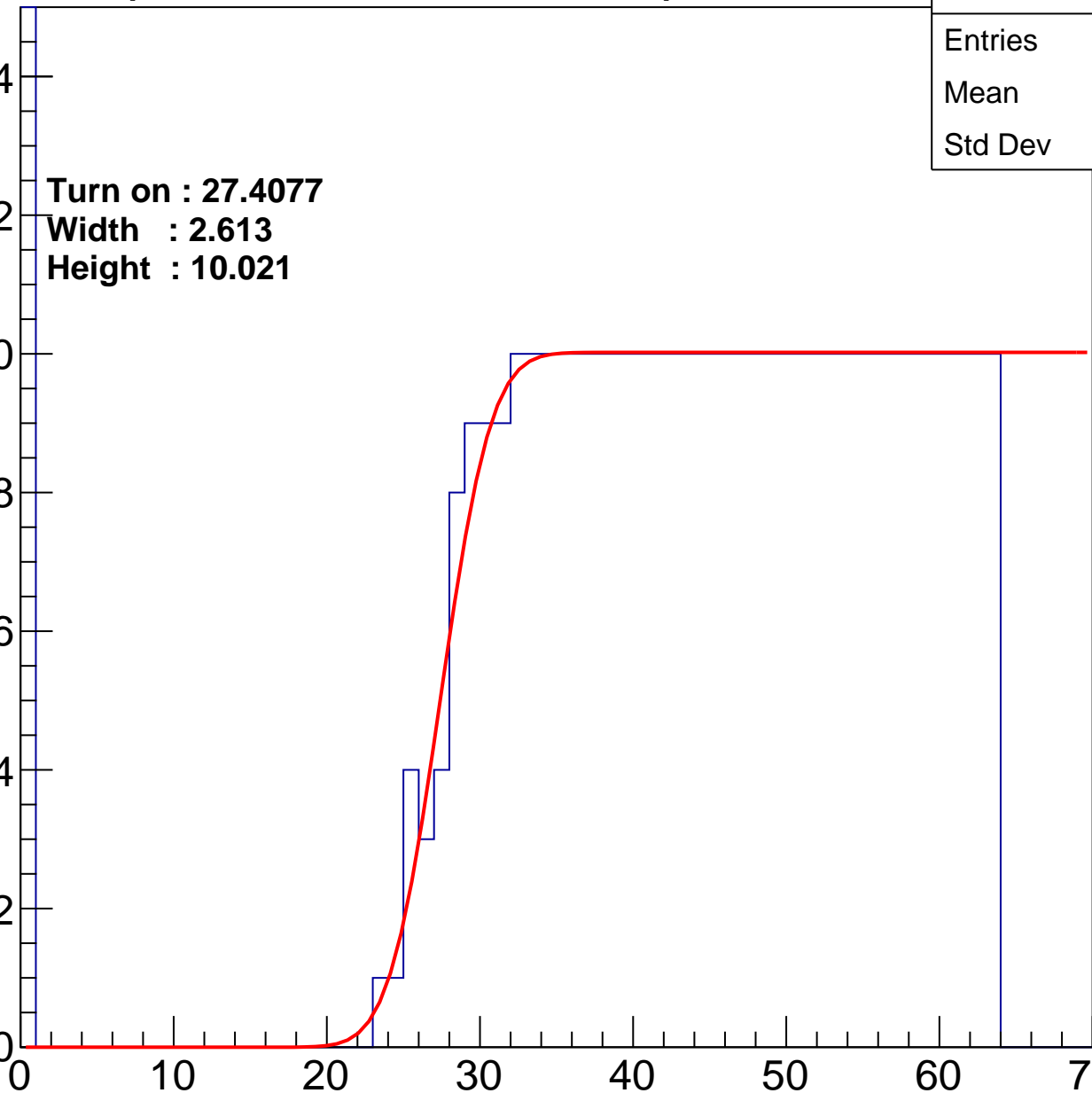
Width : 2.613

Height : 10.021

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch74

calib_packv5_041523_1651.root, FC#0, port C2

Entries	415
Mean	40.78
Std Dev	16.09

Turn on : 25.7512

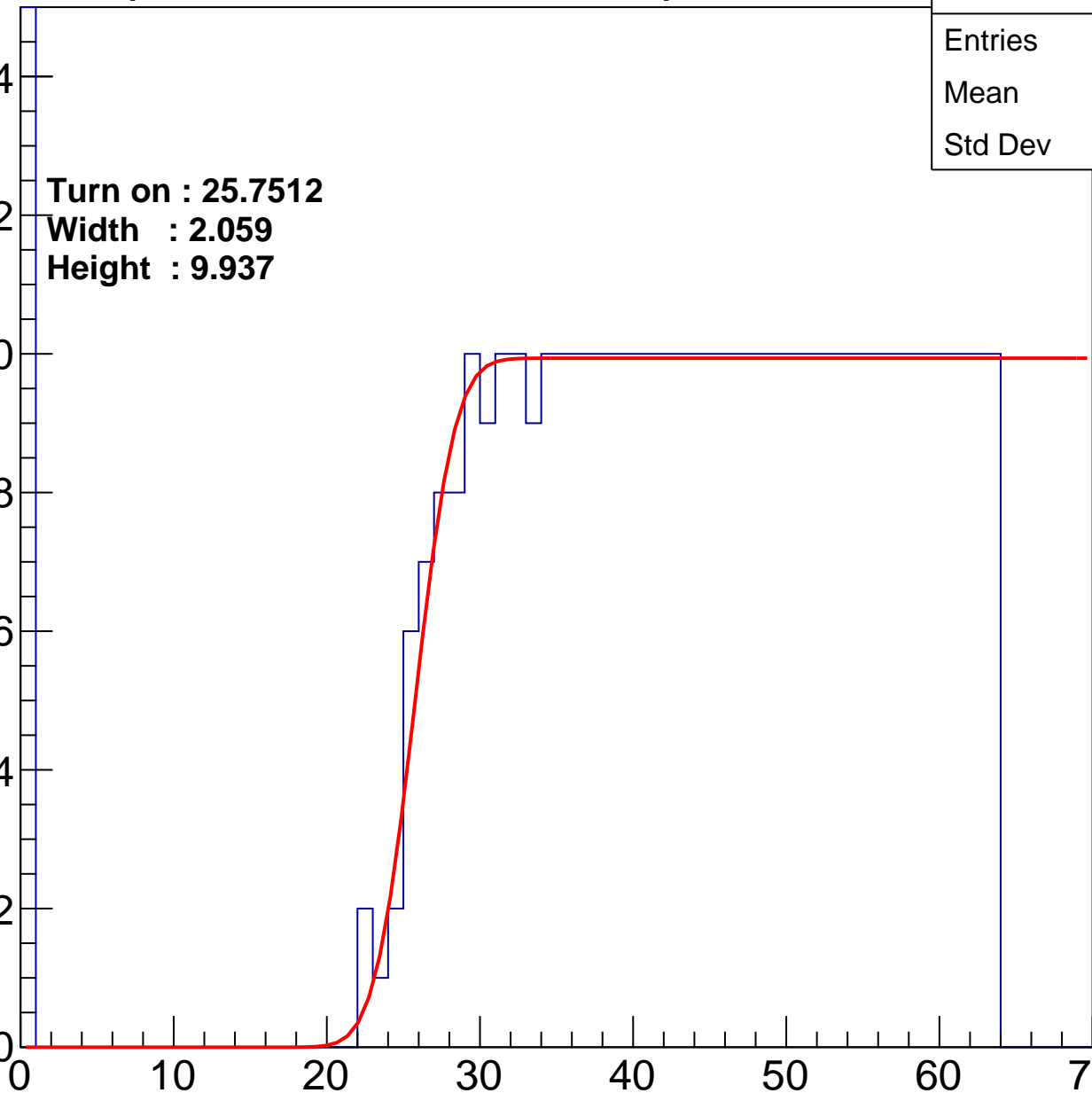
Width : 2.059

Height : 9.937

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch75

calib_packv5_041523_1651.root, FC#0, port C2

Entries	425
Mean	39.85
Std Dev	17.03

Turn on : 26.2982

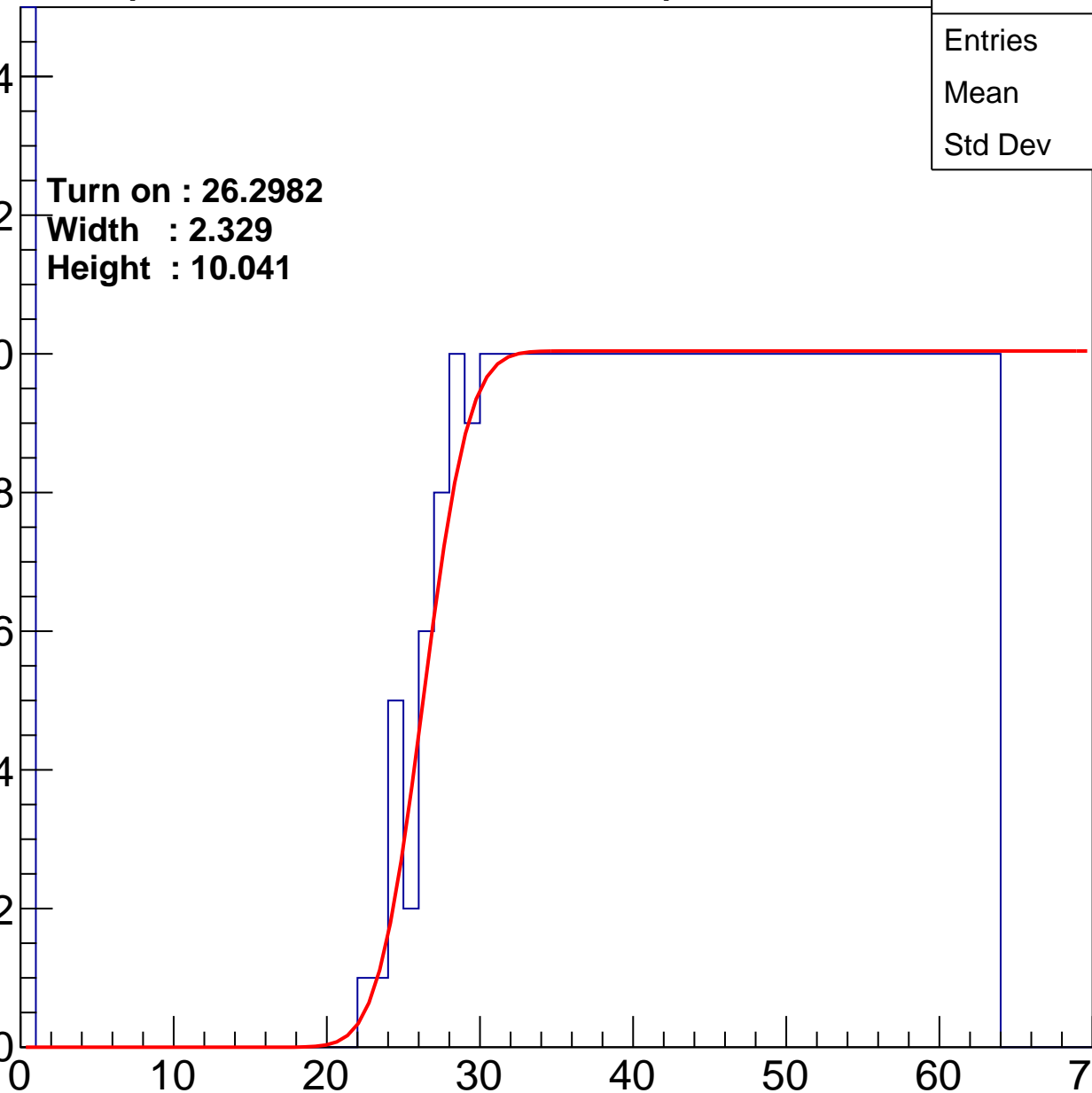
Width : 2.329

Height : 10.041

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch76

calib_packv5_041523_1651.root, FC#0, port C2

Entries	454
Mean	38.18
Std Dev	17.93

Turn on : 24.0461

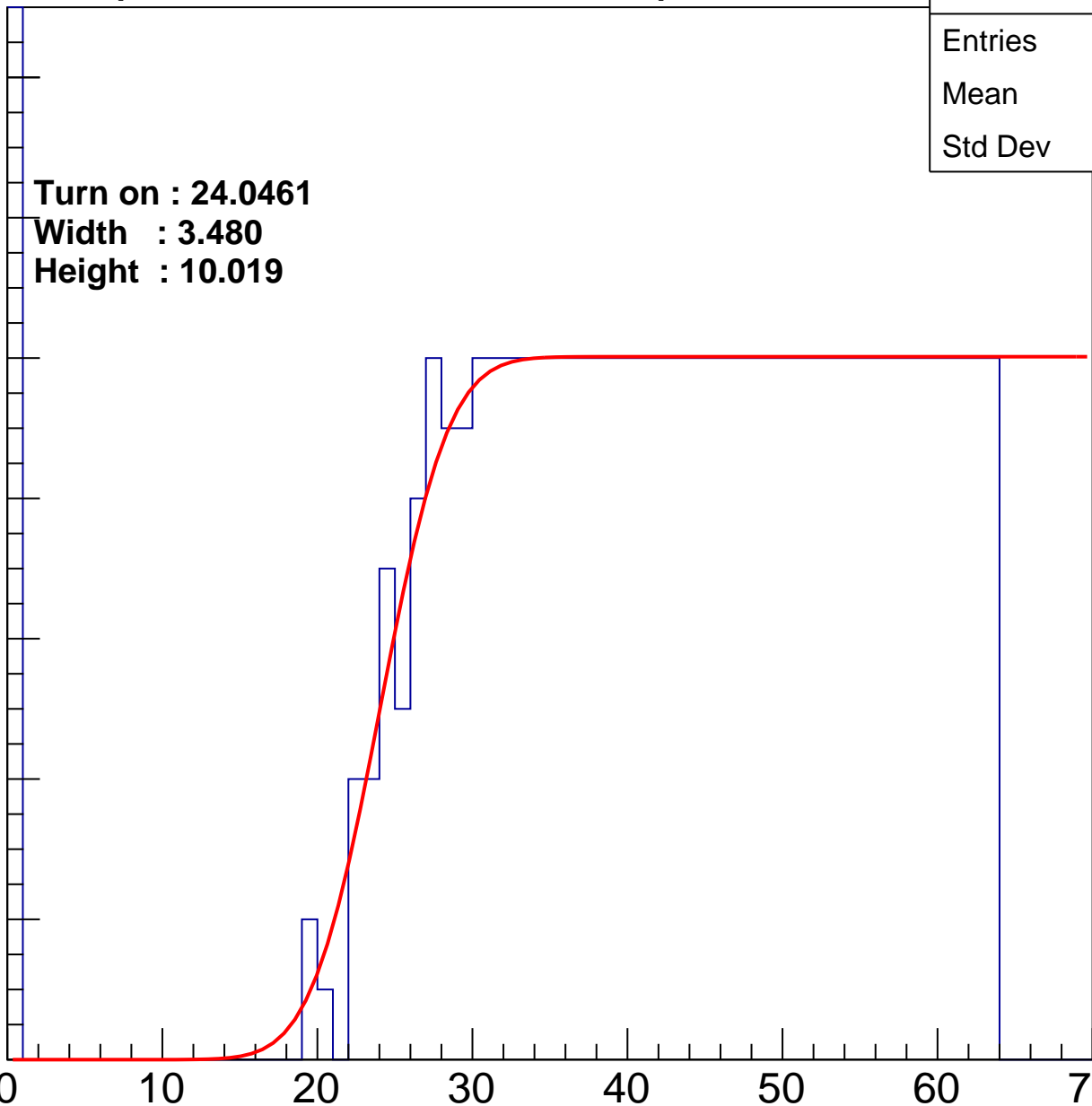
Width : 3.480

Height : 10.019

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch77

calib_packv5_041523_1651.root, FC#0, port C2

Entries	434
Mean	39.04
Std Dev	17.74

Turn on : 25.9030

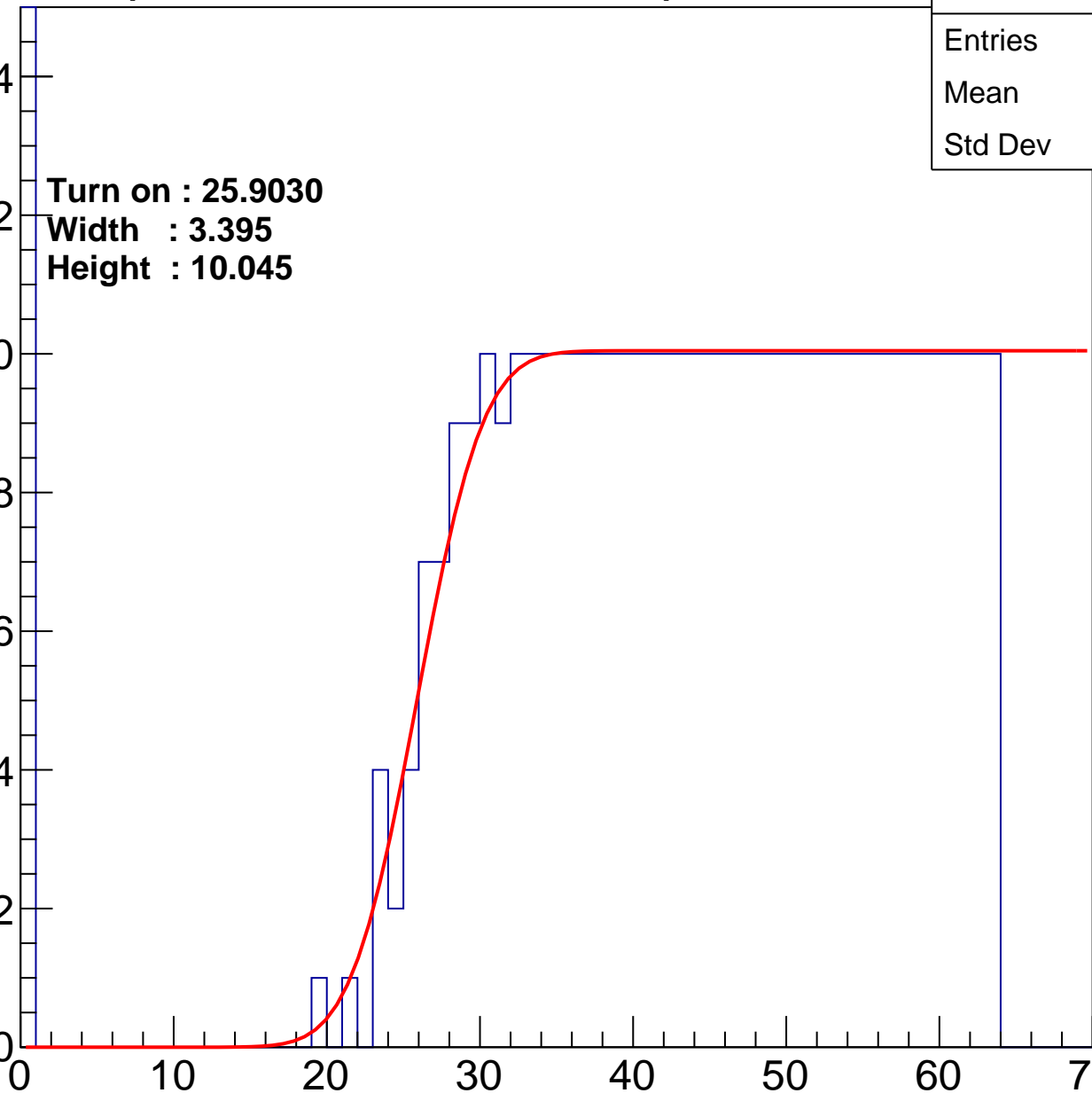
Width : 3.395

Height : 10.045

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch78

calib_packv5_041523_1651.root, FC#0, port C2

Entries	427
Mean	39.58
Std Dev	17.32

Turn on : 26.4455

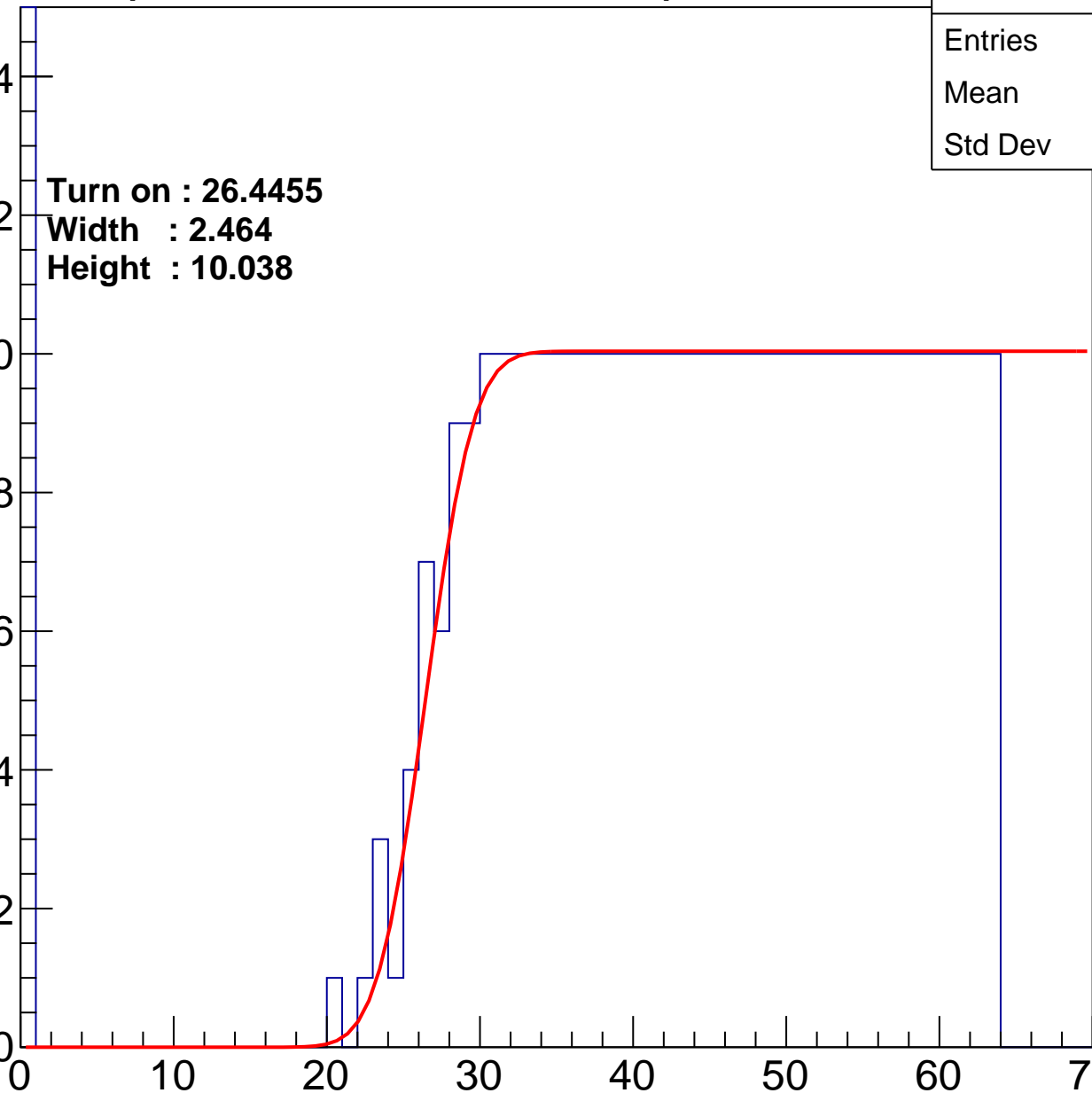
Width : 2.464

Height : 10.038

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch79

calib_packv5_041523_1651.root, FC#0, port C2

Entries	427
Mean	39.95
Std Dev	16.75

Turn on : 25.6564

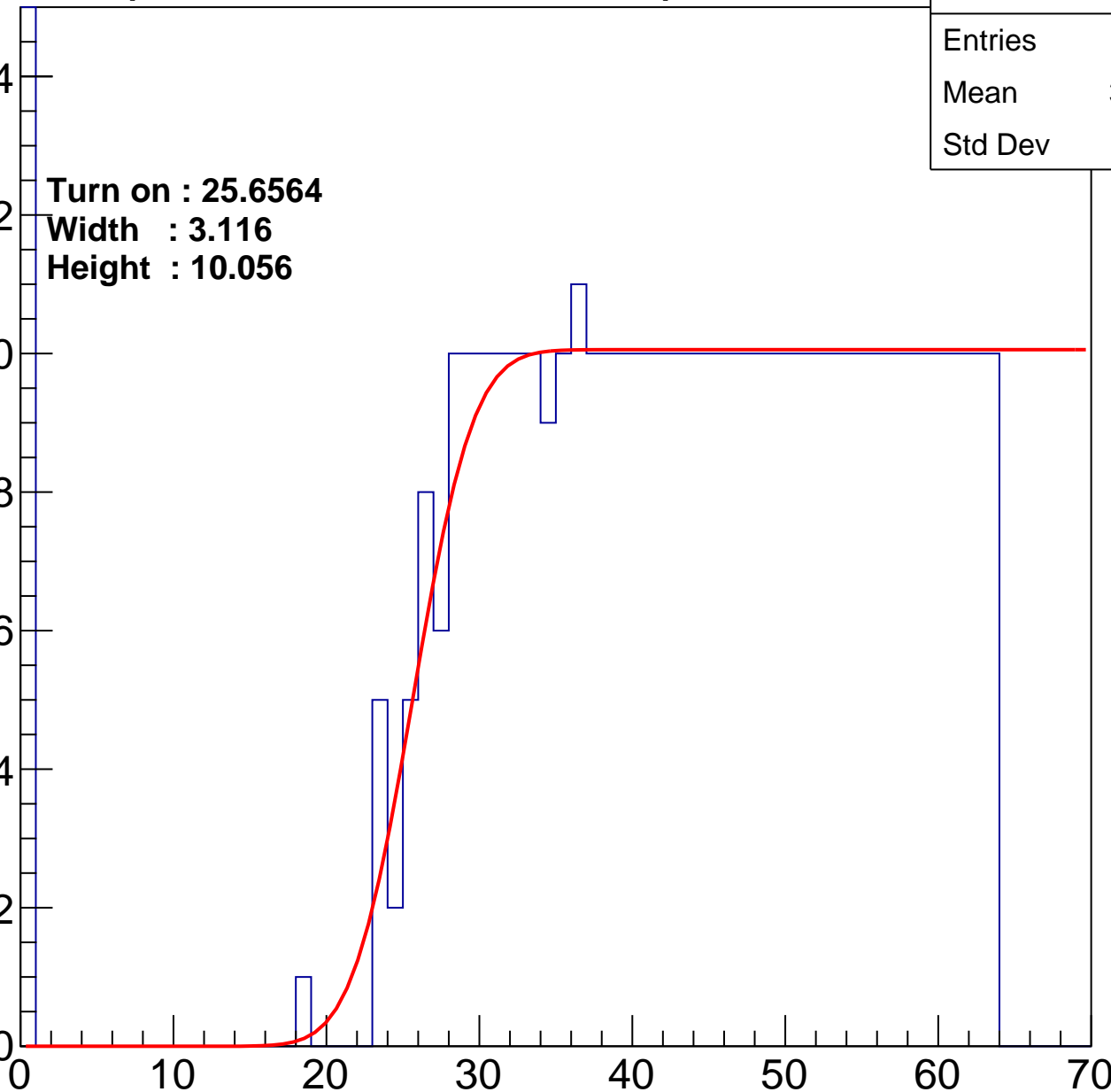
Width : 3.116

Height : 10.056

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch80

calib_packv5_041523_1651.root, FC#0, port C2

Entries	427
Mean	39.47
Std Dev	17.5

Turn on : 26.6947

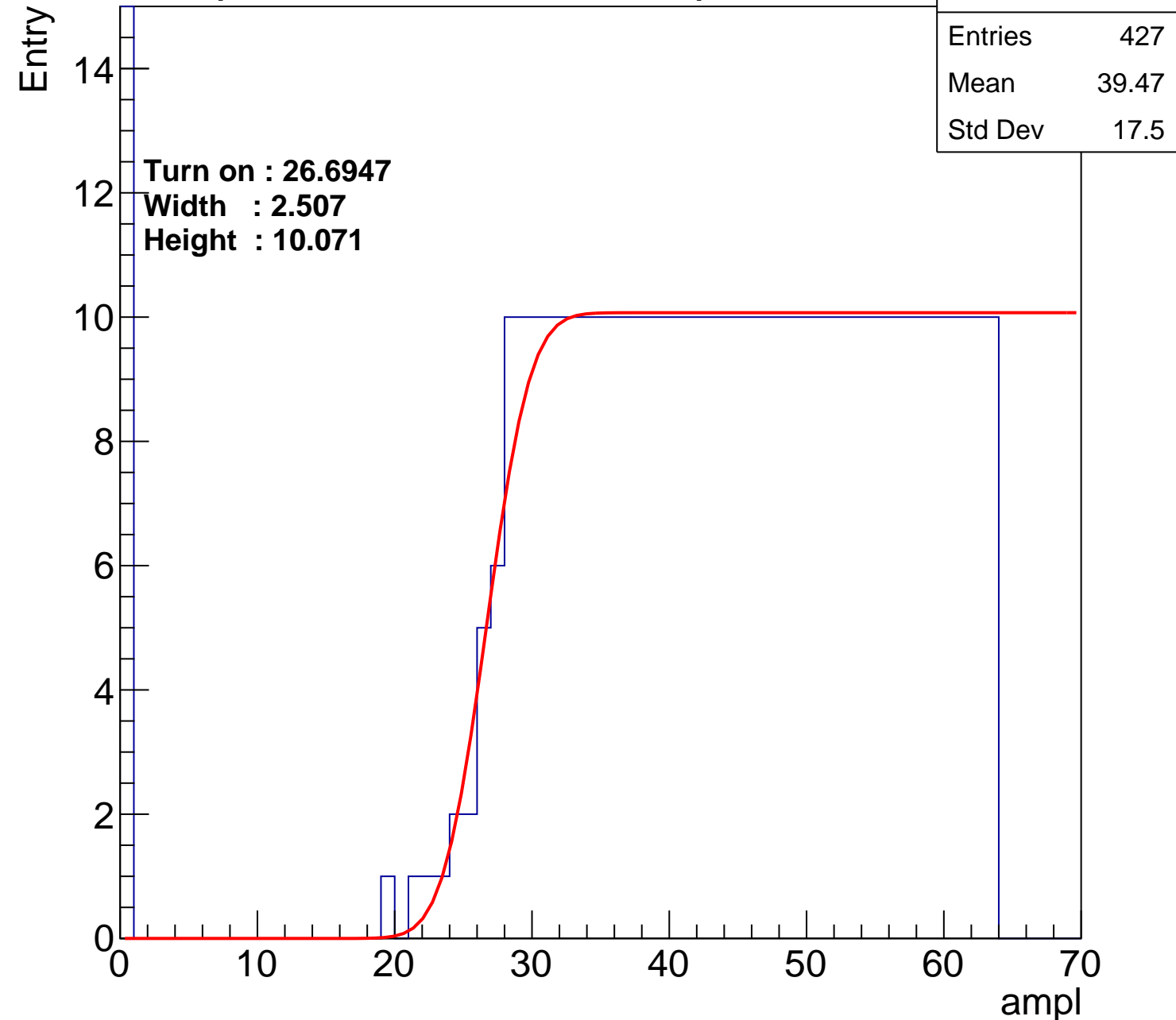
Width : 2.507

Height : 10.071

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch81

calib_packv5_041523_1651.root, FC#0, port C2

Entries	426
Mean	39.2
Std Dev	17.95

Turn on : 26.7496

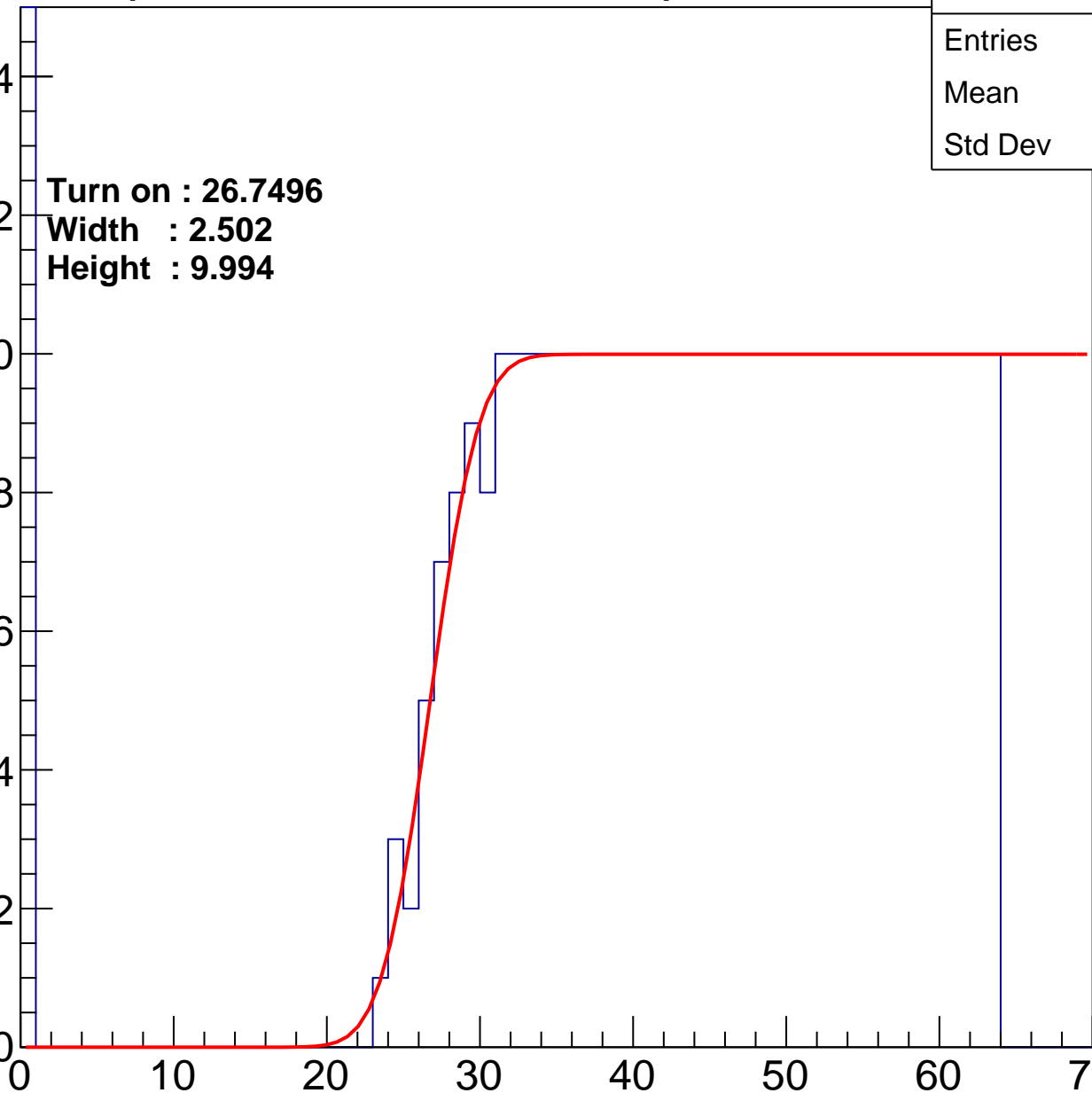
Width : 2.502

Height : 9.994

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch82

calib_packv5_041523_1651.root, FC#0, port C2

Entries	525
Mean	33.48
Std Dev	20.55

Turn on : 24.4350

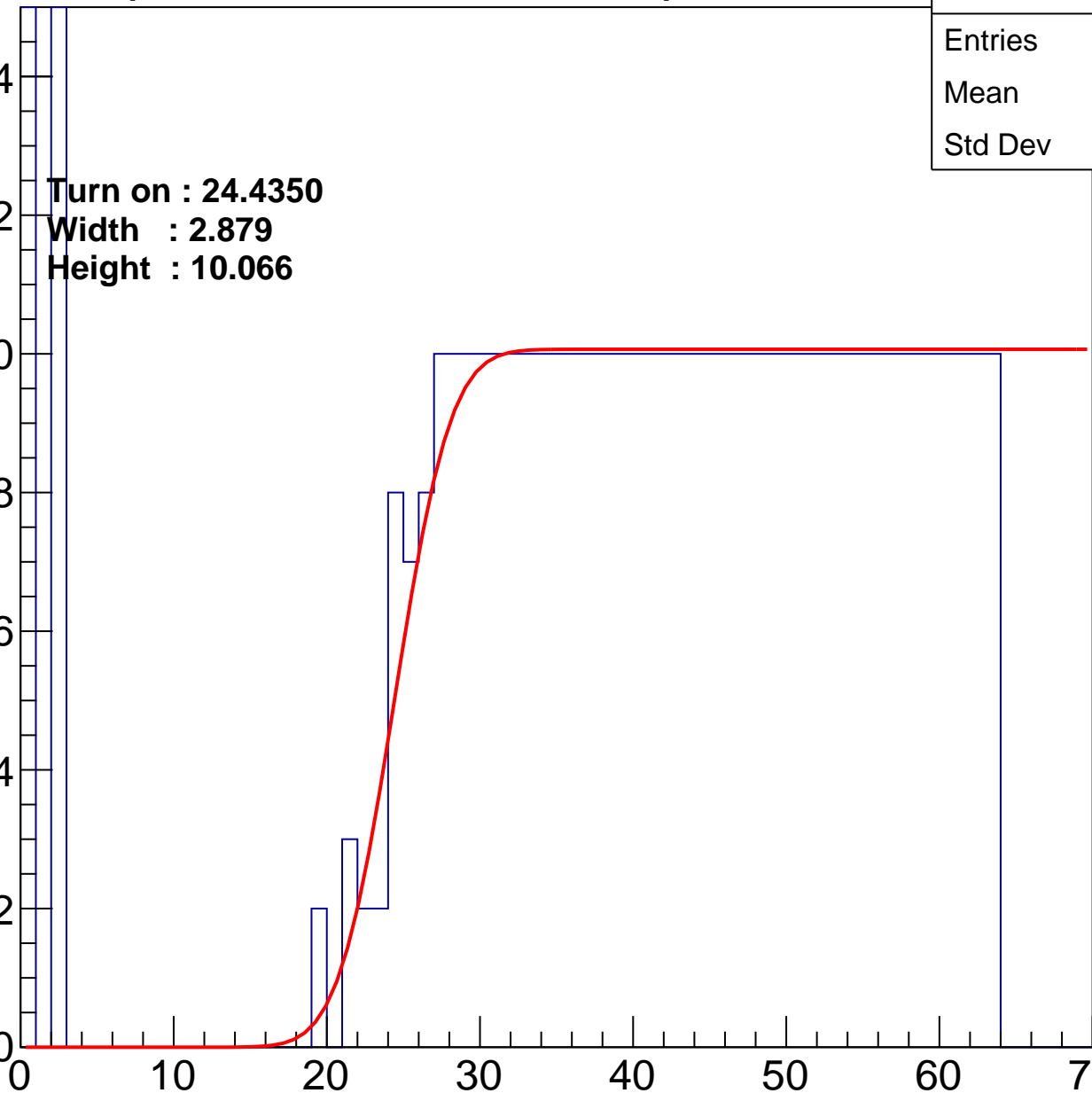
Width : 2.879

Height : 10.066

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch83

calib_packv5_041523_1651.root, FC#0, port C2

Entries	423
Mean	39.94
Std Dev	16.95

Turn on : 26.6745

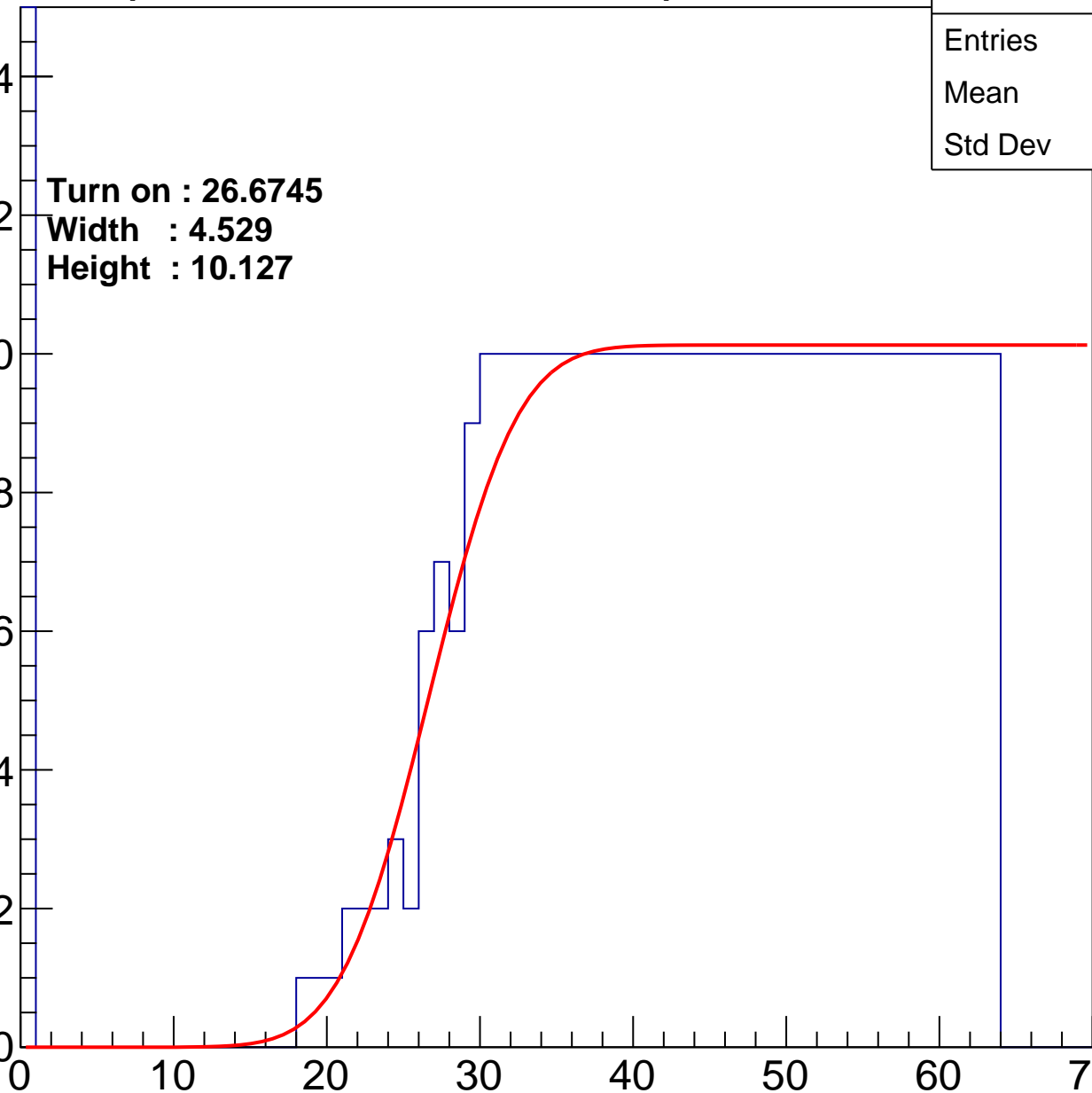
Width : 4.529

Height : 10.127

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch84

calib_packv5_041523_1651.root, FC#0, port C2

Entries	424
Mean	39.83
Std Dev	17.08

Turn on : 25.5530

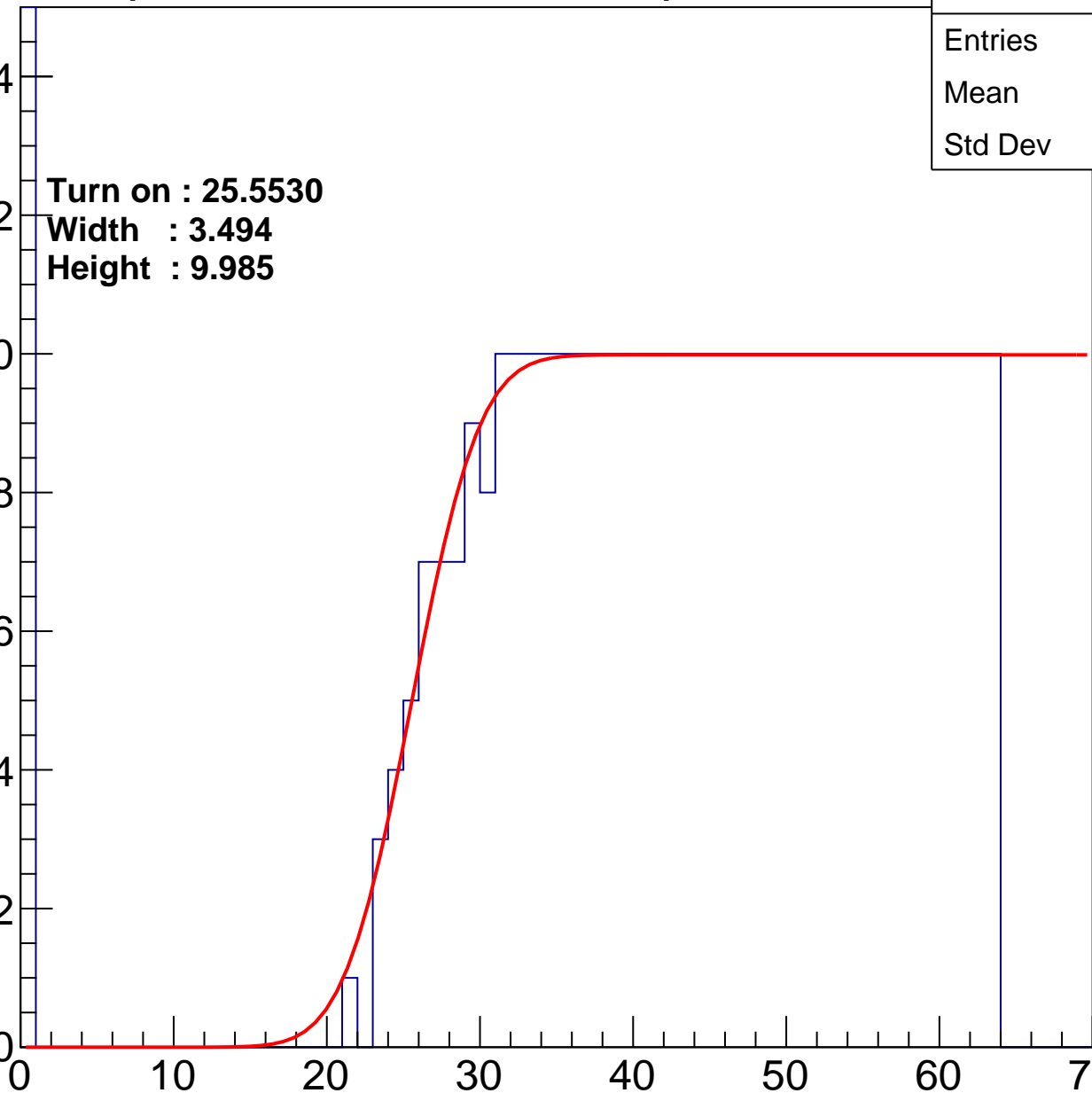
Width : 3.494

Height : 9.985

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch85

calib_packv5_041523_1651.root, FC#0, port C2

Entries	419
Mean	40.19
Std Dev	16.82

Turn on : 26.2909

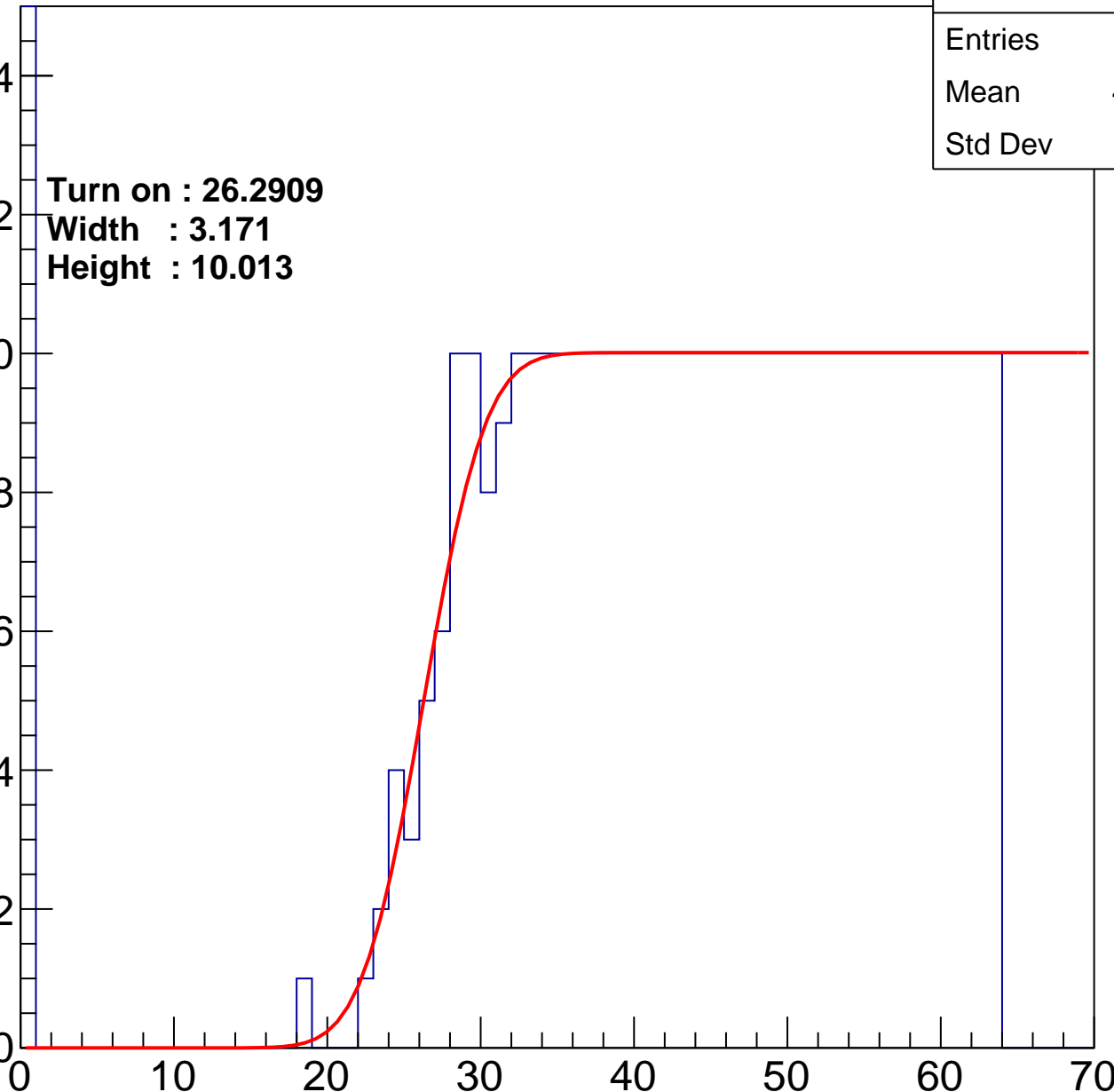
Width : 3.171

Height : 10.013

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch86

calib_packv5_041523_1651.root, FC#0, port C2

Entries	446
Mean	38.97
Std Dev	17.17

Turn on : 24.2657

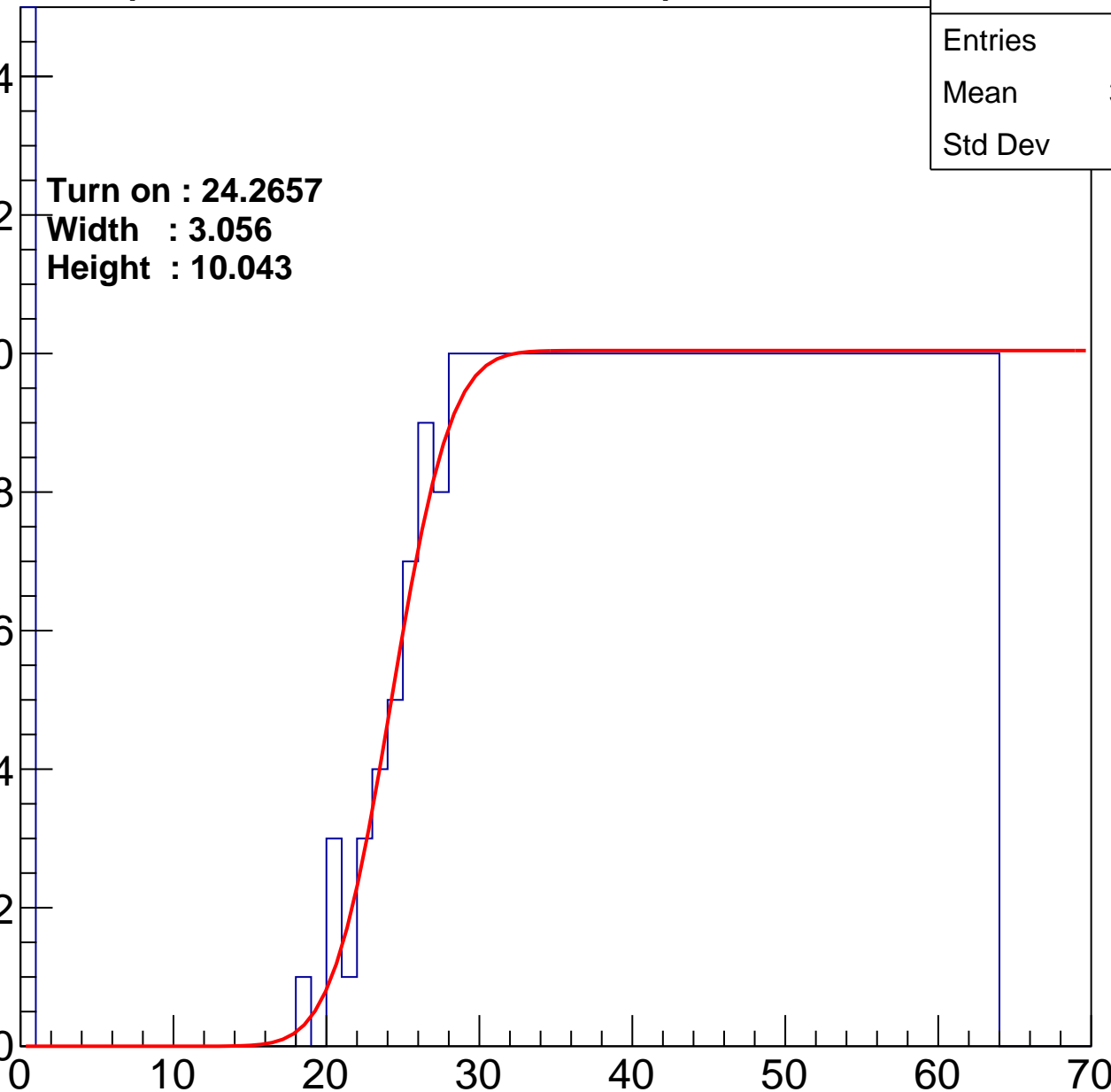
Width : 3.056

Height : 10.043

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch87

calib_packv5_041523_1651.root, FC#0, port C2

Entries	420
Mean	40.21
Std Dev	16.76

Turn on : 25.8428

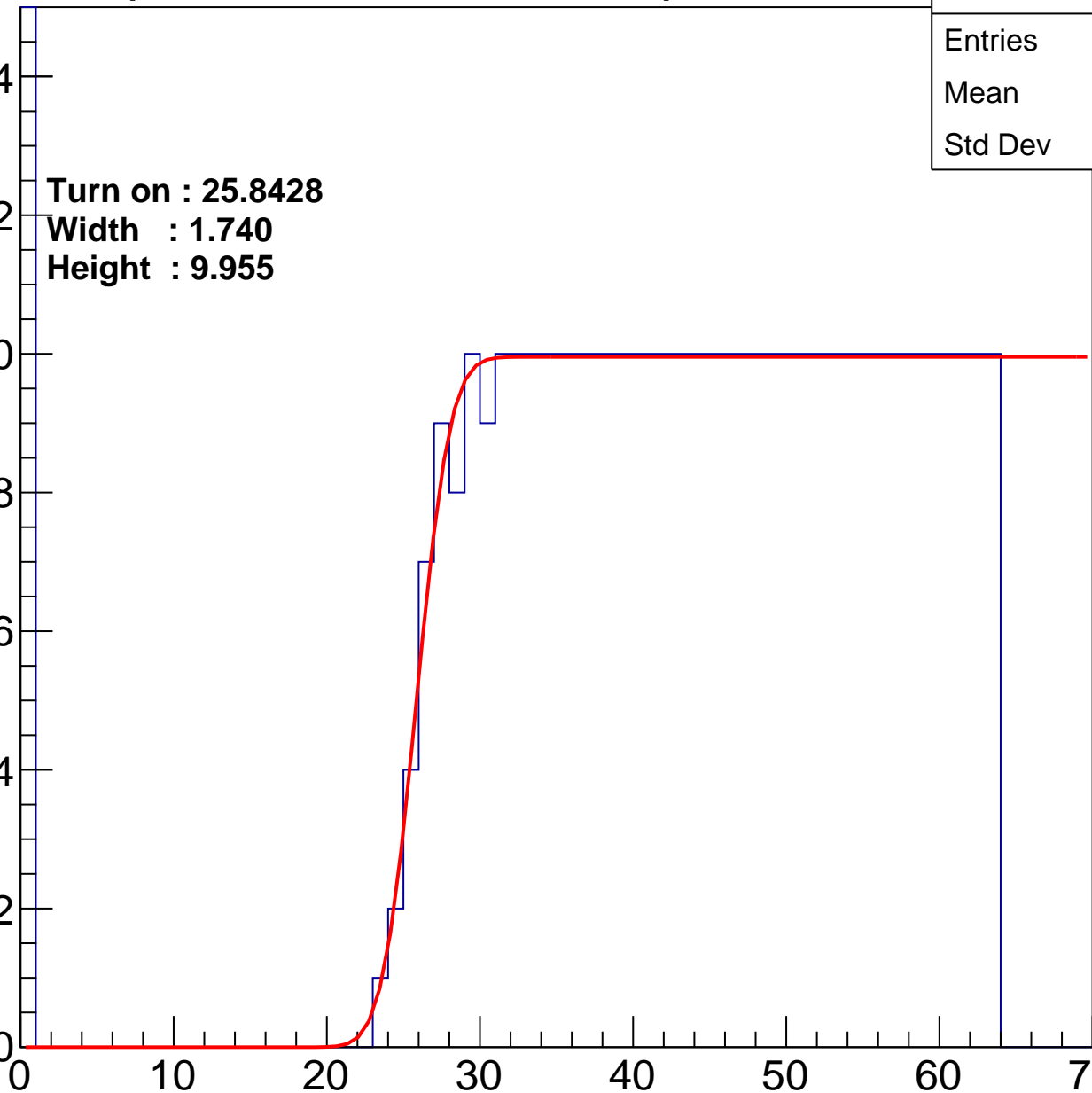
Width : 1.740

Height : 9.955

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch88

calib_packv5_041523_1651.root, FC#0, port C2

Entries	453
Mean	39.11
Std Dev	16.48

Turn on : 23.3911

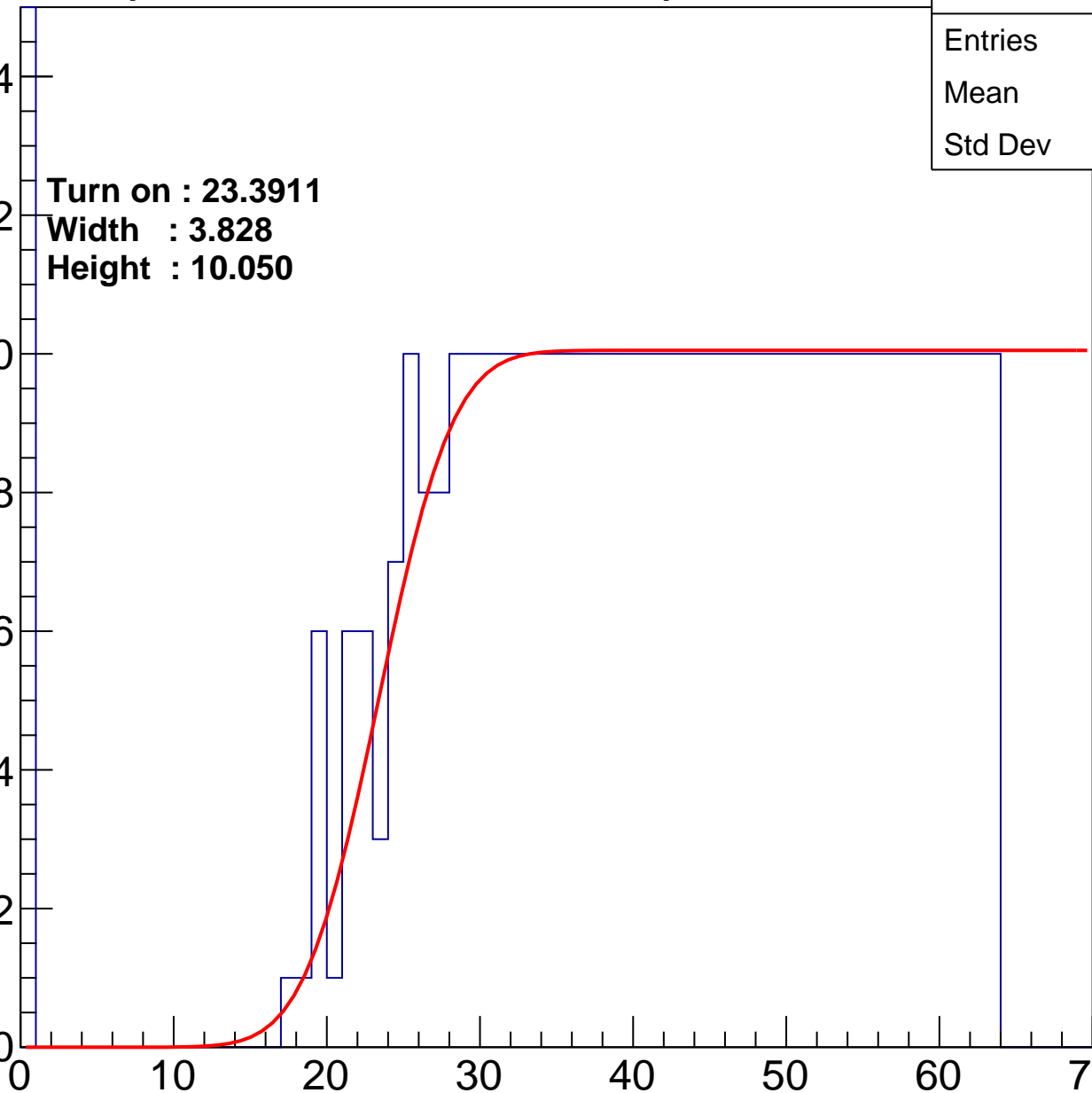
Width : 3.828

Height : 10.050

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch89

calib_packv5_041523_1651.root, FC#0, port C2

Entries	426
Mean	39.62
Std Dev	17.28

Turn on : 26.0147

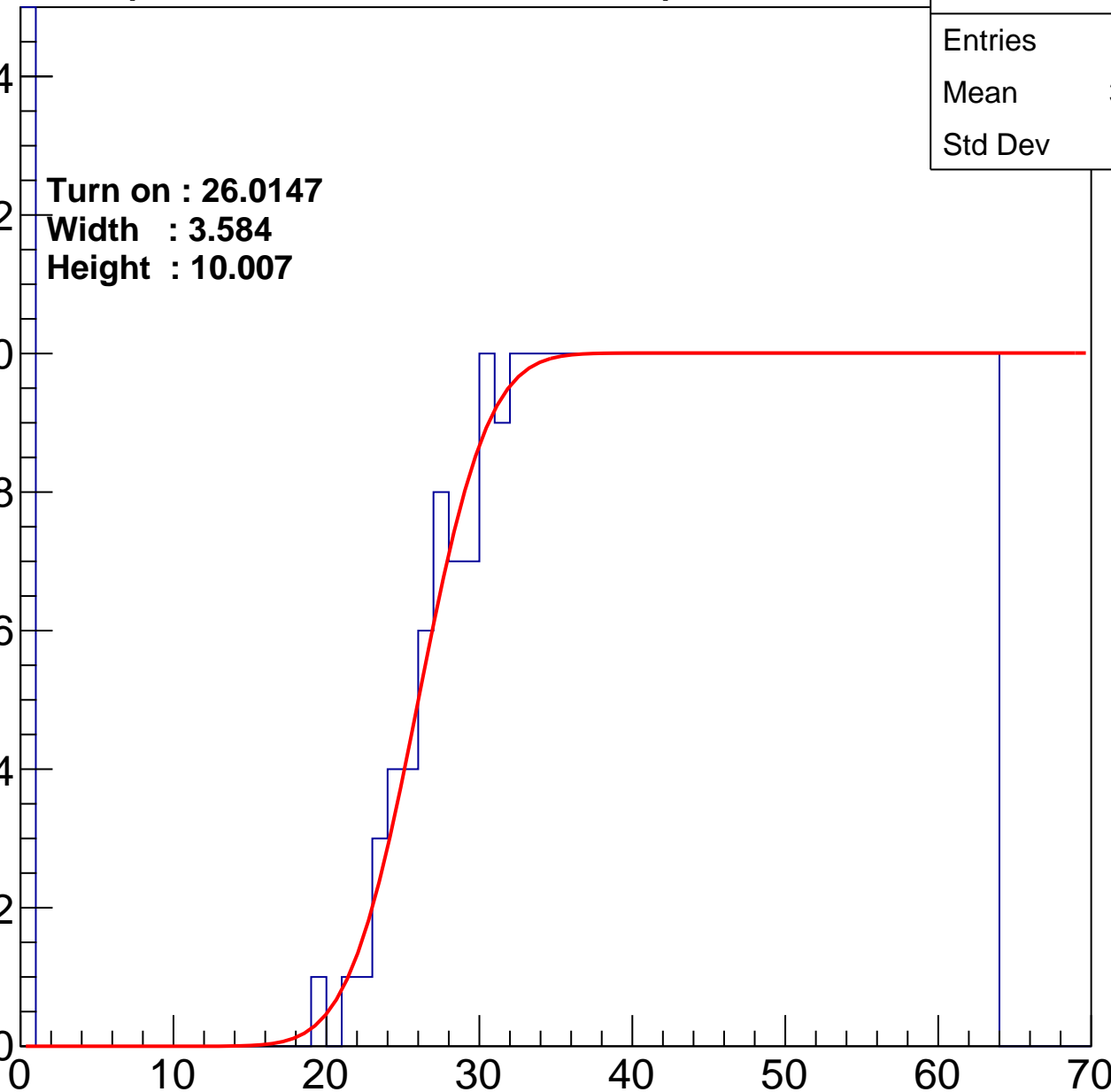
Width : 3.584

Height : 10.007

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch90

calib_packv5_041523_1651.root, FC#0, port C2

Entries	420
Mean	39.95
Std Dev	17.12

Turn on : 26.1251

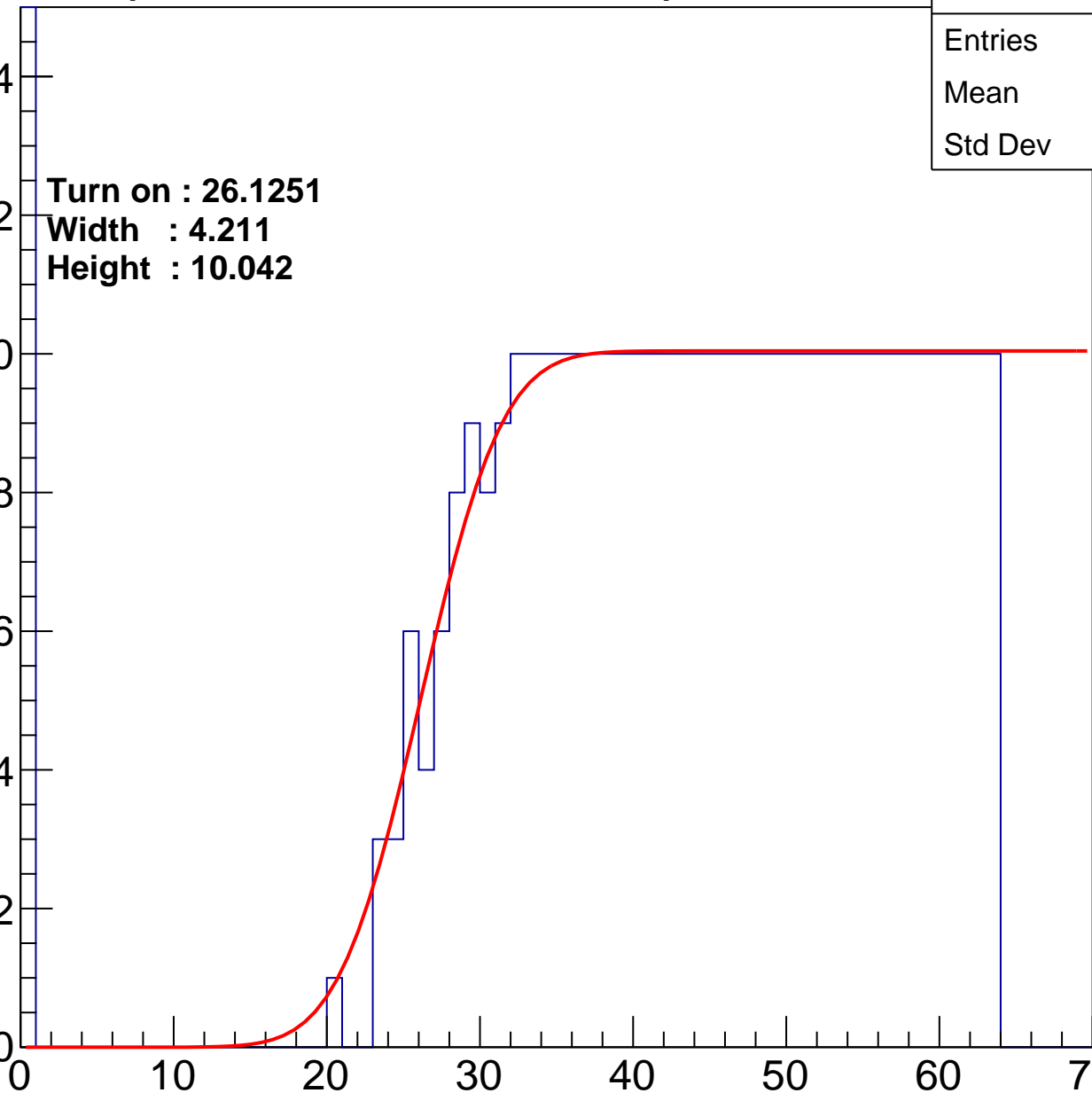
Width : 4.211

Height : 10.042

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch91

calib_packv5_041523_1651.root, FC#0, port C2

Entries	414
Mean	40.64
Std Dev	16.4

Turn on : 26.4198

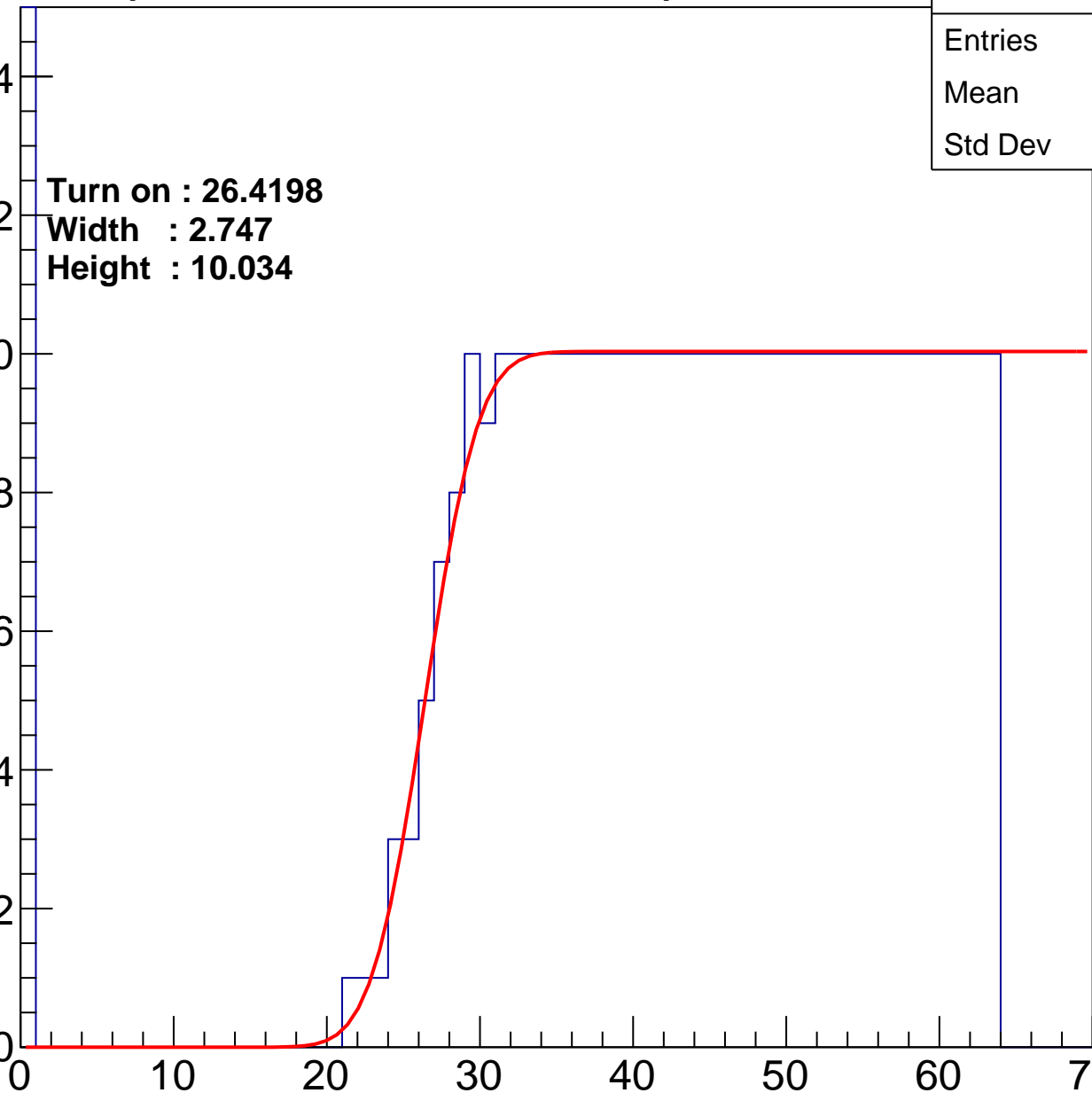
Width : 2.747

Height : 10.034

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch92

calib_packv5_041523_1651.root, FC#0, port C2

Entries	448
Mean	38.85
Std Dev	17.24

Turn on : 22.8961

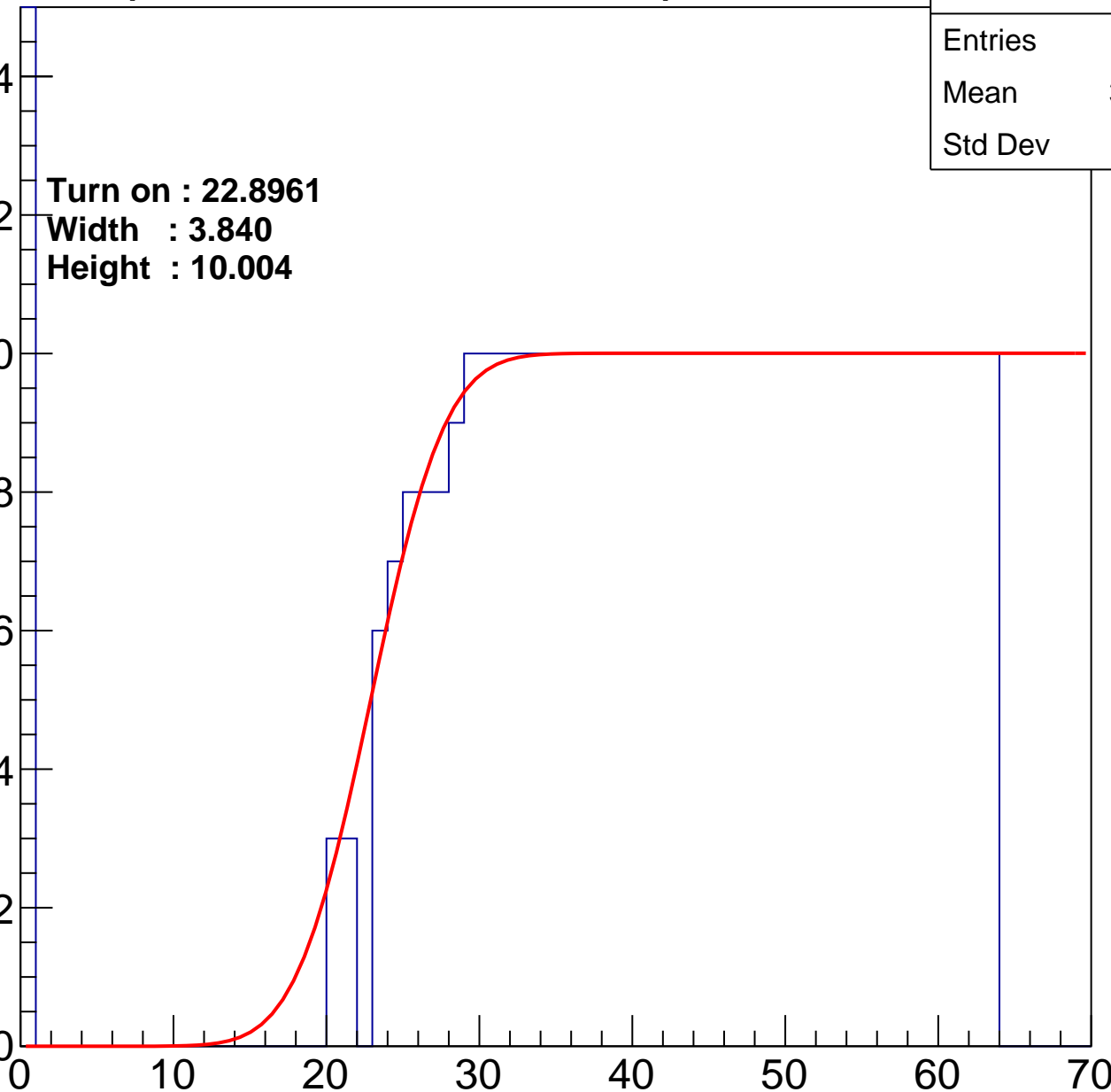
Width : 3.840

Height : 10.004

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch93

calib_packv5_041523_1651.root, FC#0, port C2

Entries	416
Mean	39.71
Std Dev	17.72

Turn on : 27.3059

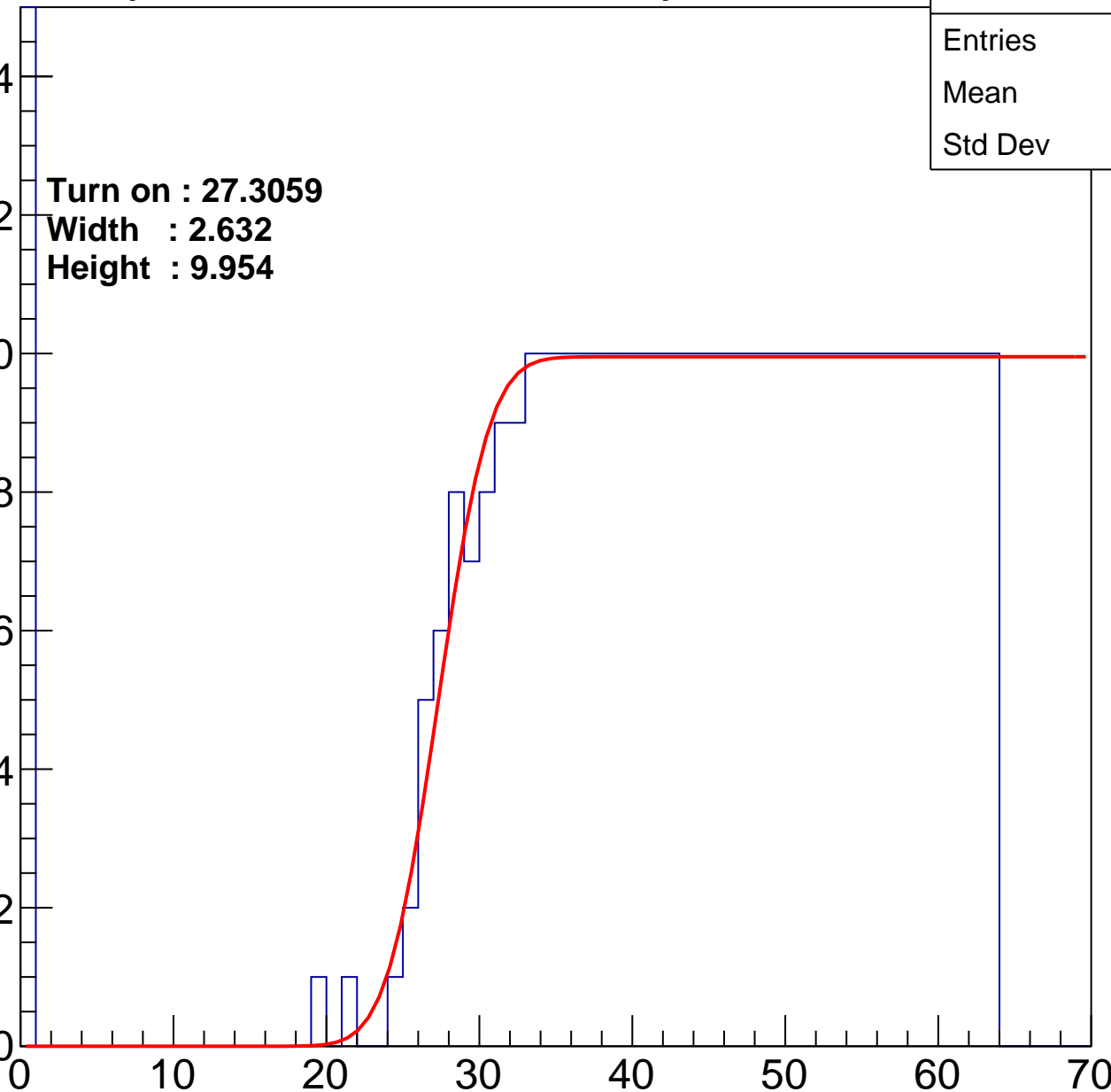
Width : 2.632

Height : 9.954

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch94

calib_packv5_041523_1651.root, FC#0, port C2

Entries	430
Mean	39.9
Std Dev	16.65

Turn on : 25.2767

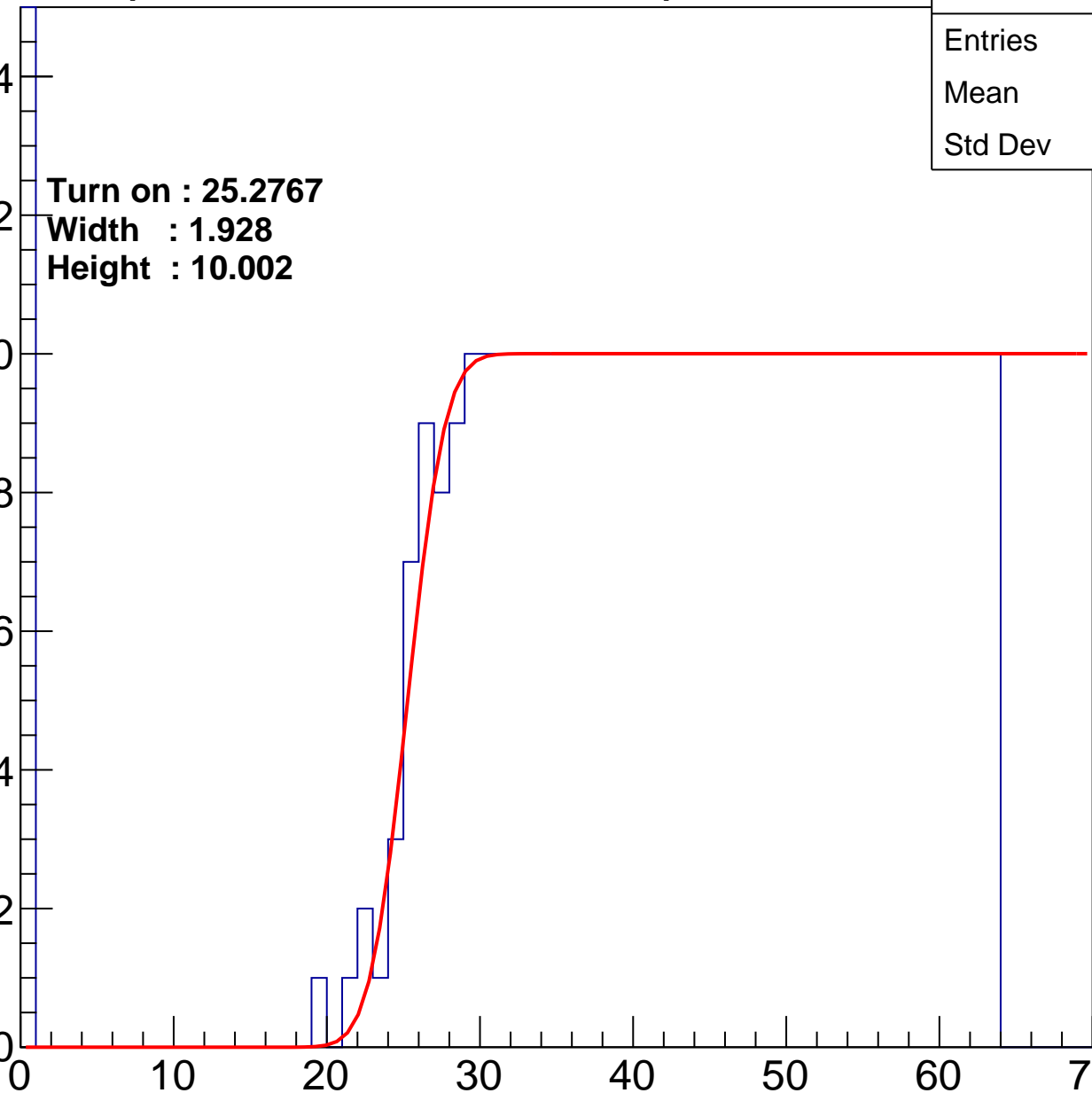
Width : 1.928

Height : 10.002

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch95

calib_packv5_041523_1651.root, FC#0, port C2

Entries	455
Mean	38.21
Std Dev	17.83

Turn on : 23.9922

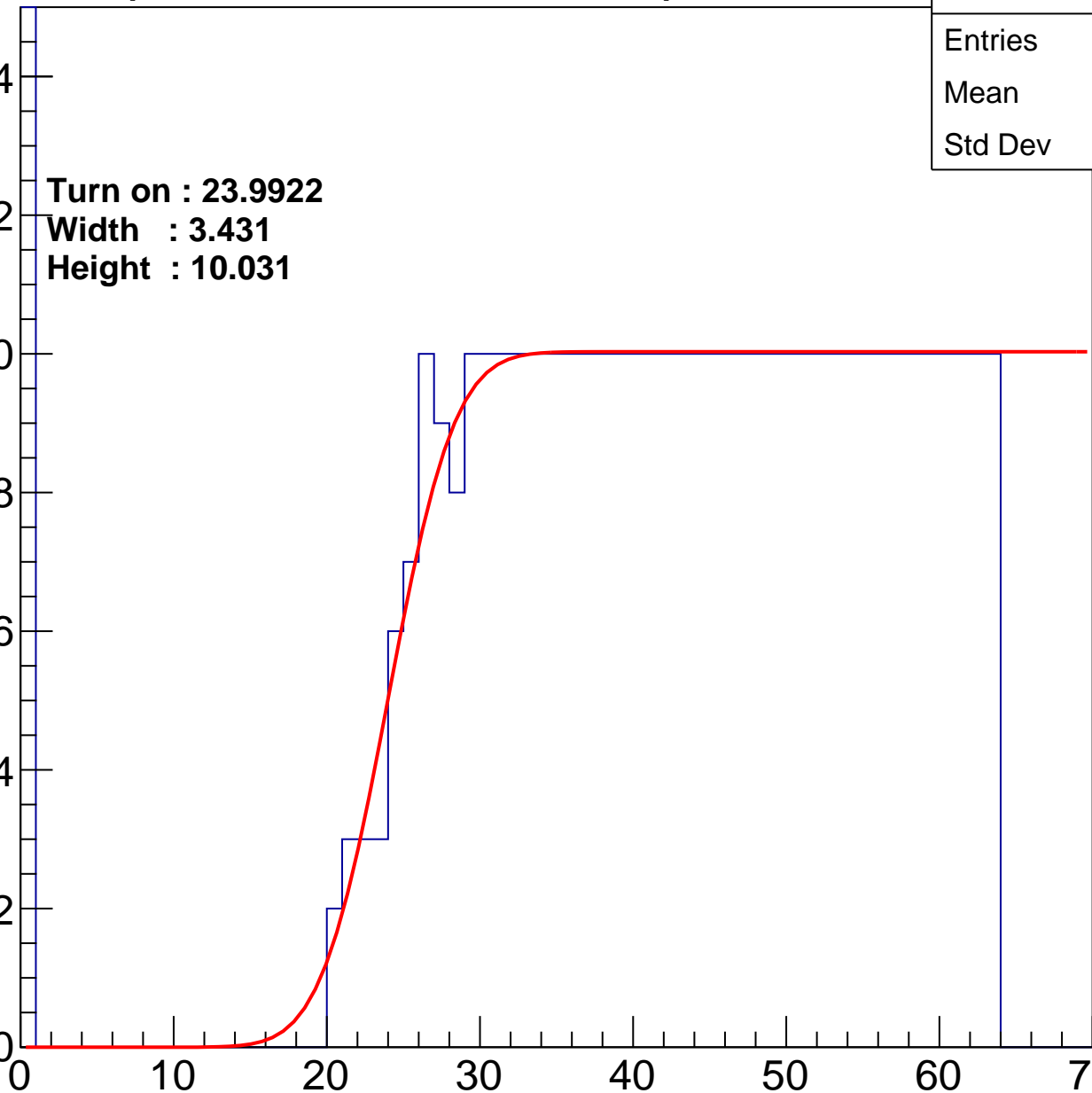
Width : 3.431

Height : 10.031

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch96

calib_packv5_041523_1651.root, FC#0, port C2

Entries	429
Mean	39.72
Std Dev	16.92

Turn on : 25.0541

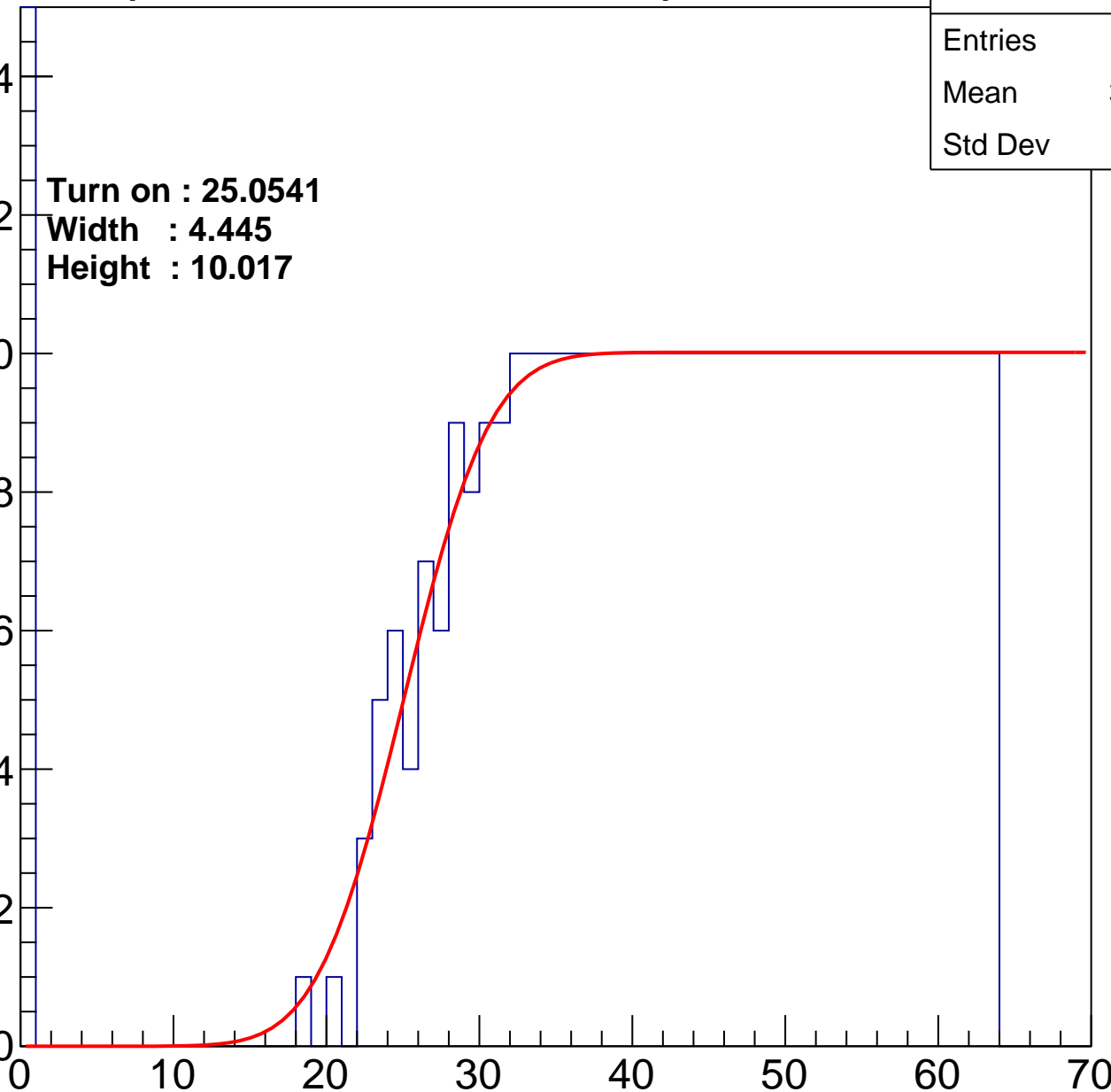
Width : 4.445

Height : 10.017

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch97

calib_packv5_041523_1651.root, FC#0, port C2

Entries	401
Mean	40.56
Std Dev	17.32

Turn on : 28.1620

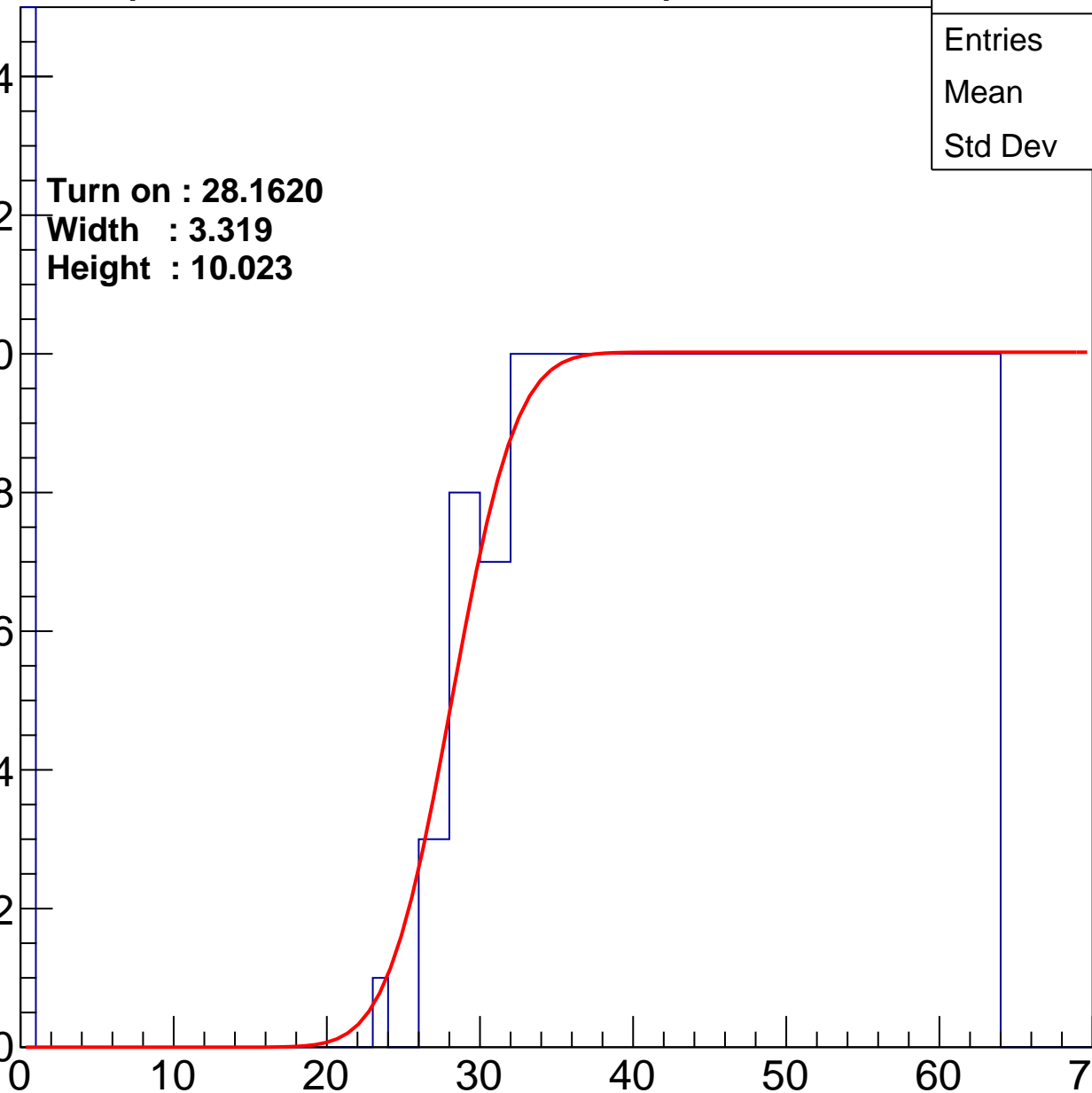
Width : 3.319

Height : 10.023

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch98

calib_packv5_041523_1651.root, FC#0, port C2

Entries	447
Mean	38.27
Std Dev	18.14

Turn on : 25.4229

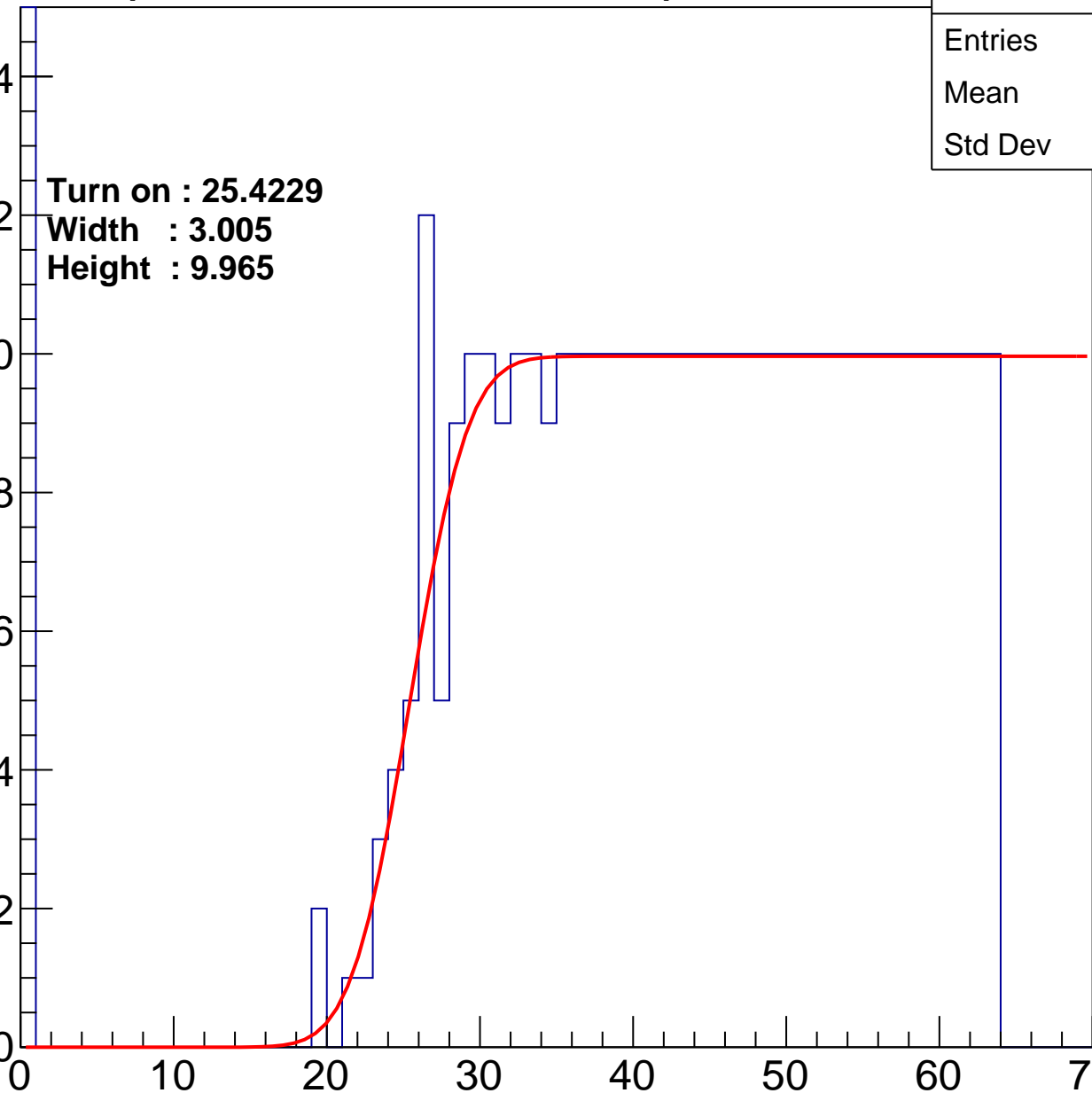
Width : 3.005

Height : 9.965

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch99

calib_packv5_041523_1651.root, FC#0, port C2

Entries	422
Mean	39.78
Std Dev	17.28

Turn on : 26.4276

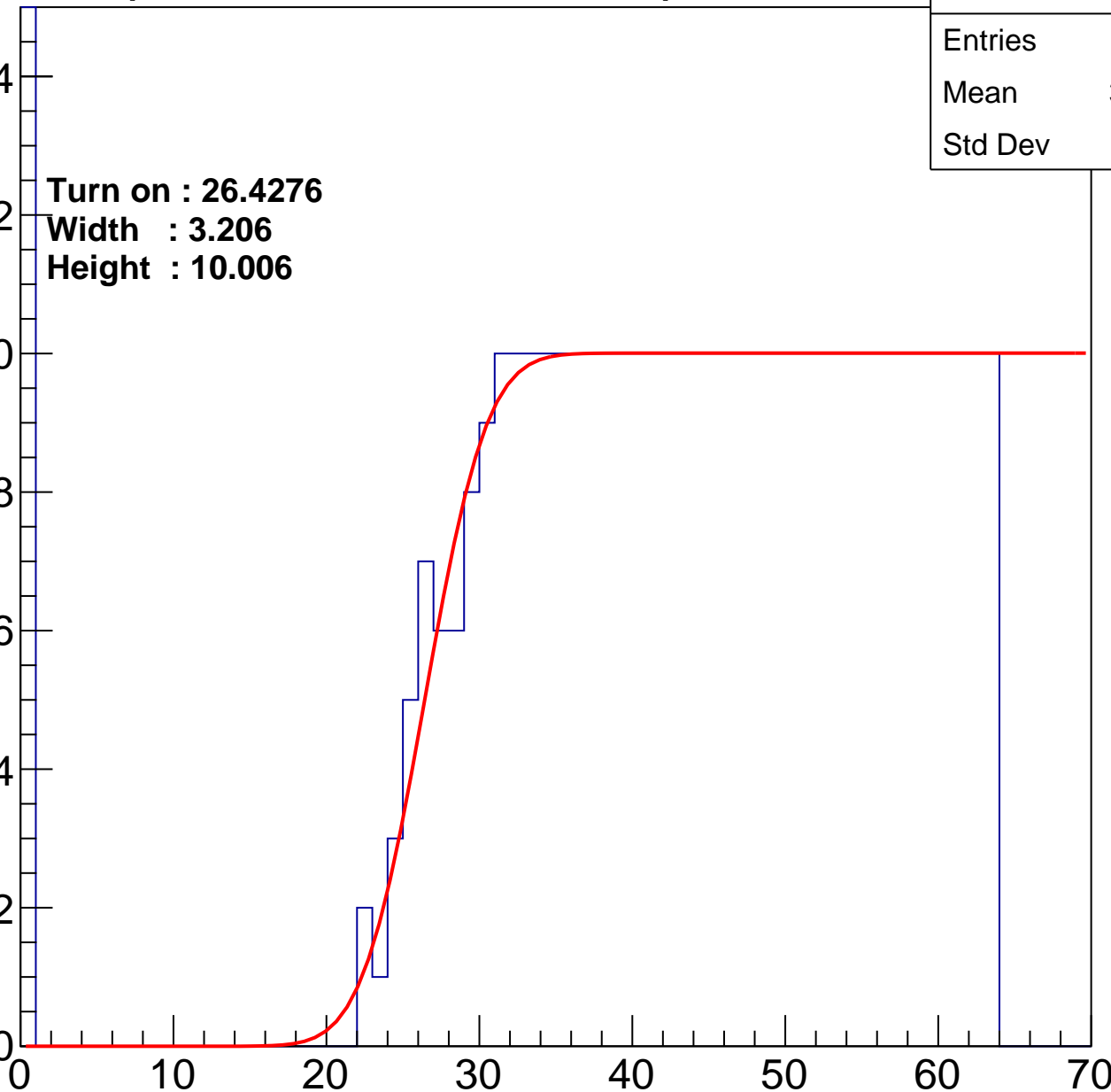
Width : 3.206

Height : 10.006

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch100

calib_packv5_041523_1651.root, FC#0, port C2

Entries	425
Mean	39.69
Std Dev	17.26

Turn on : 26.1840

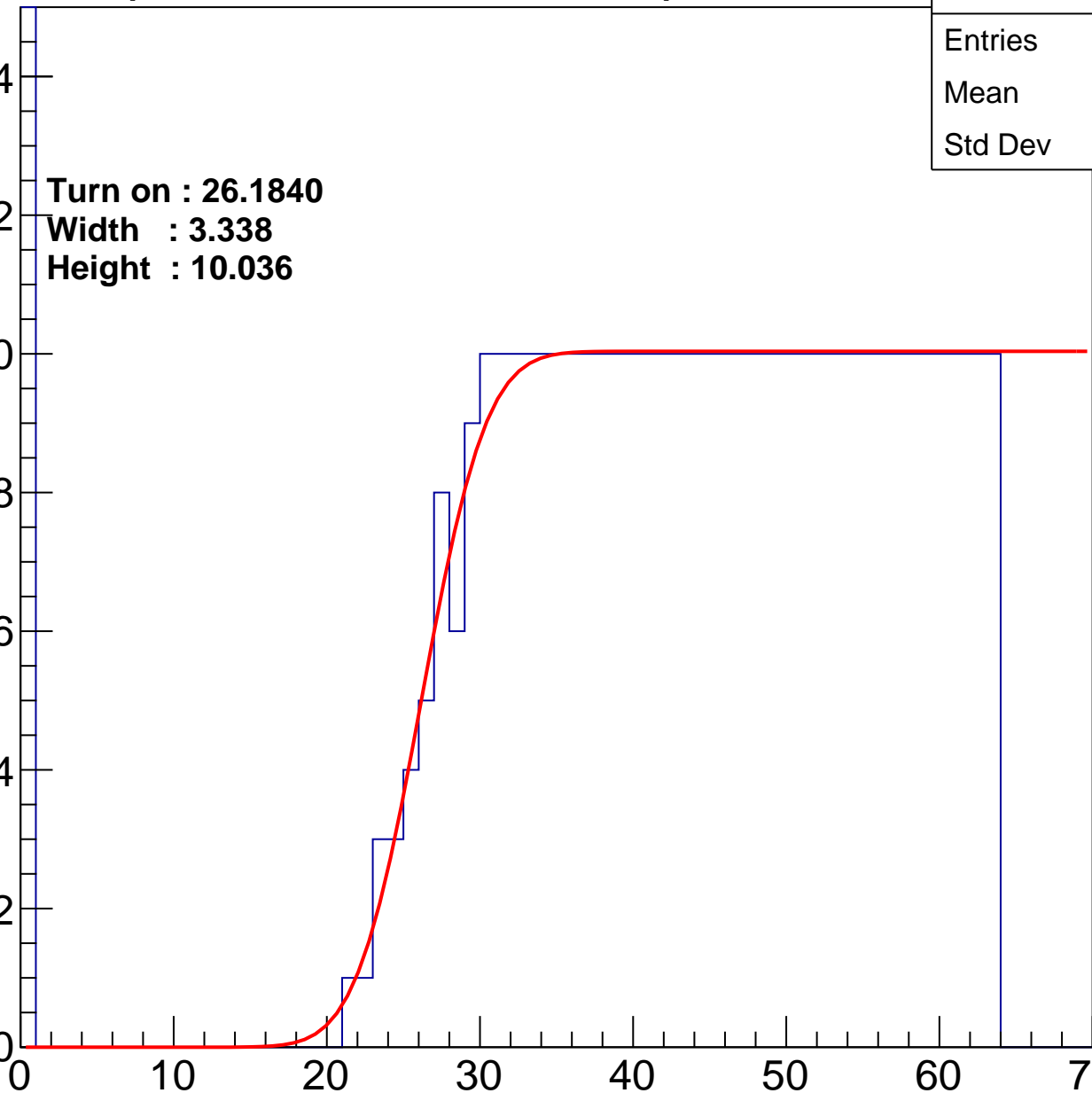
Width : 3.338

Height : 10.036

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch101

calib_packv5_041523_1651.root, FC#0, port C2

Entries	437
Mean	39.57
Std Dev	16.75

Turn on : 24.5047

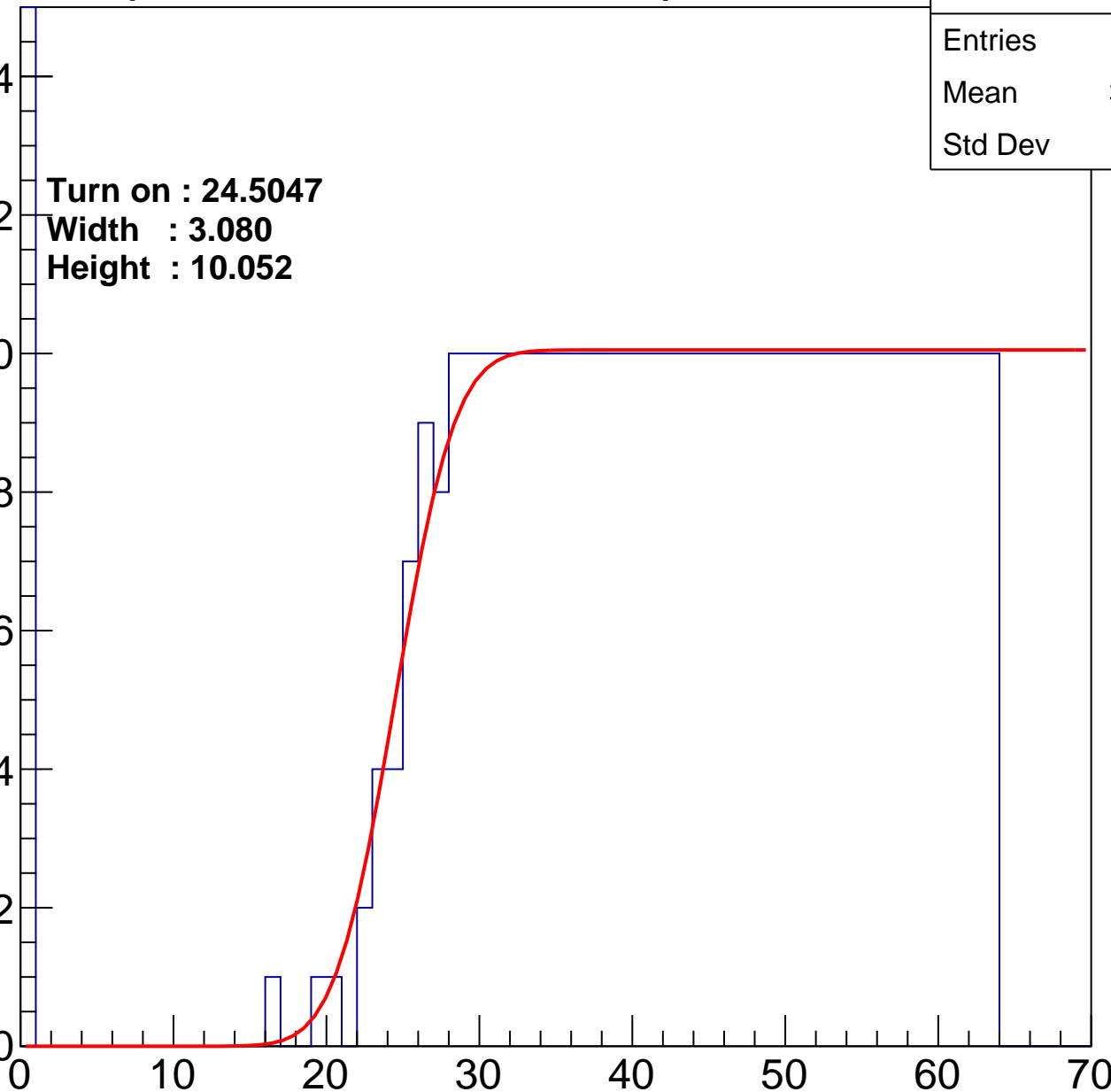
Width : 3.080

Height : 10.052

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch102

calib_packv5_041523_1651.root, FC#0, port C2

Entries	458
Mean	37.94
Std Dev	18.05

Turn on : 24.0258

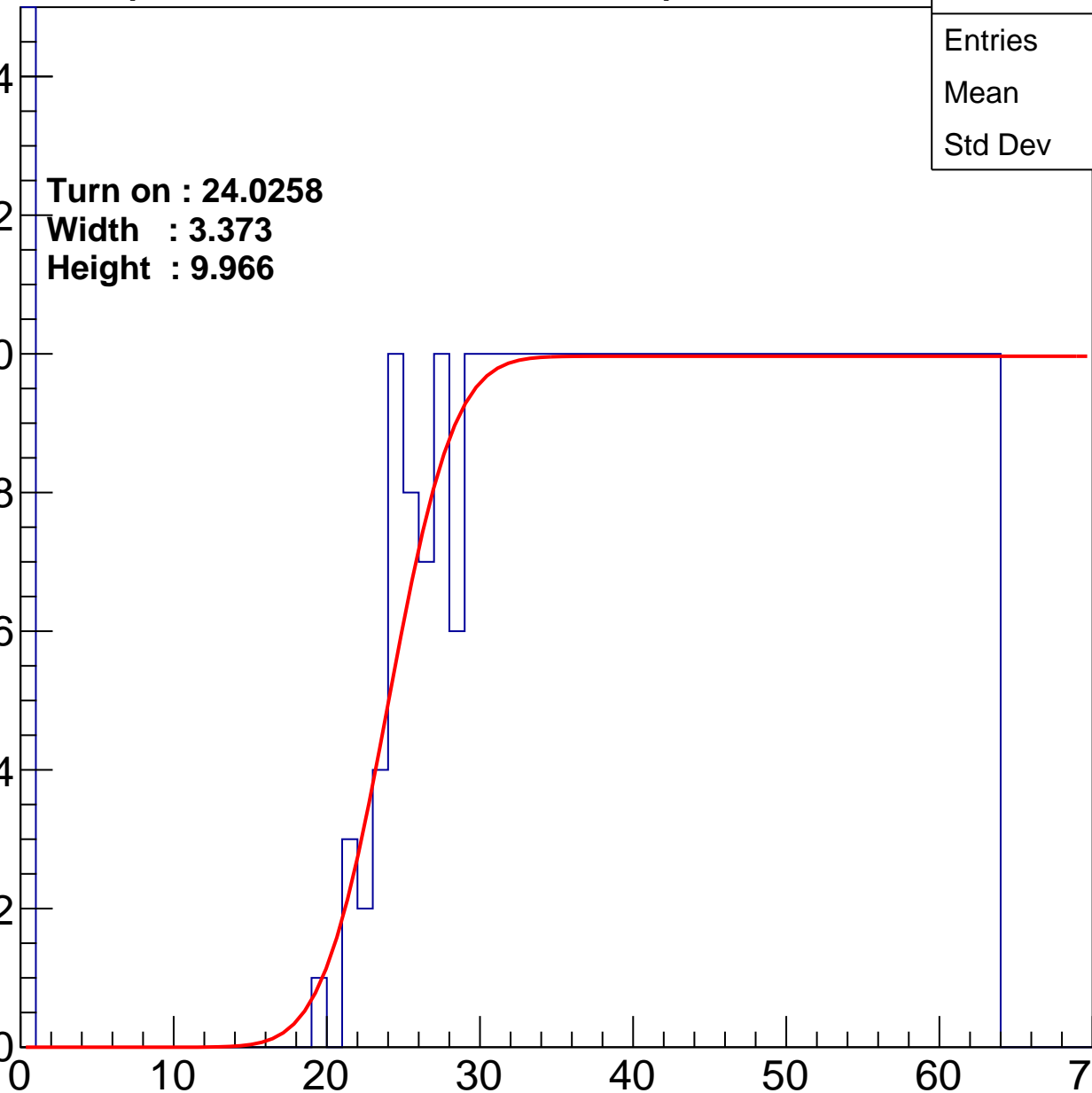
Width : 3.373

Height : 9.966

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch103

calib_packv5_041523_1651.root, FC#0, port C2

Entries	417
Mean	40.27
Std Dev	16.81

Turn on : 26.9008

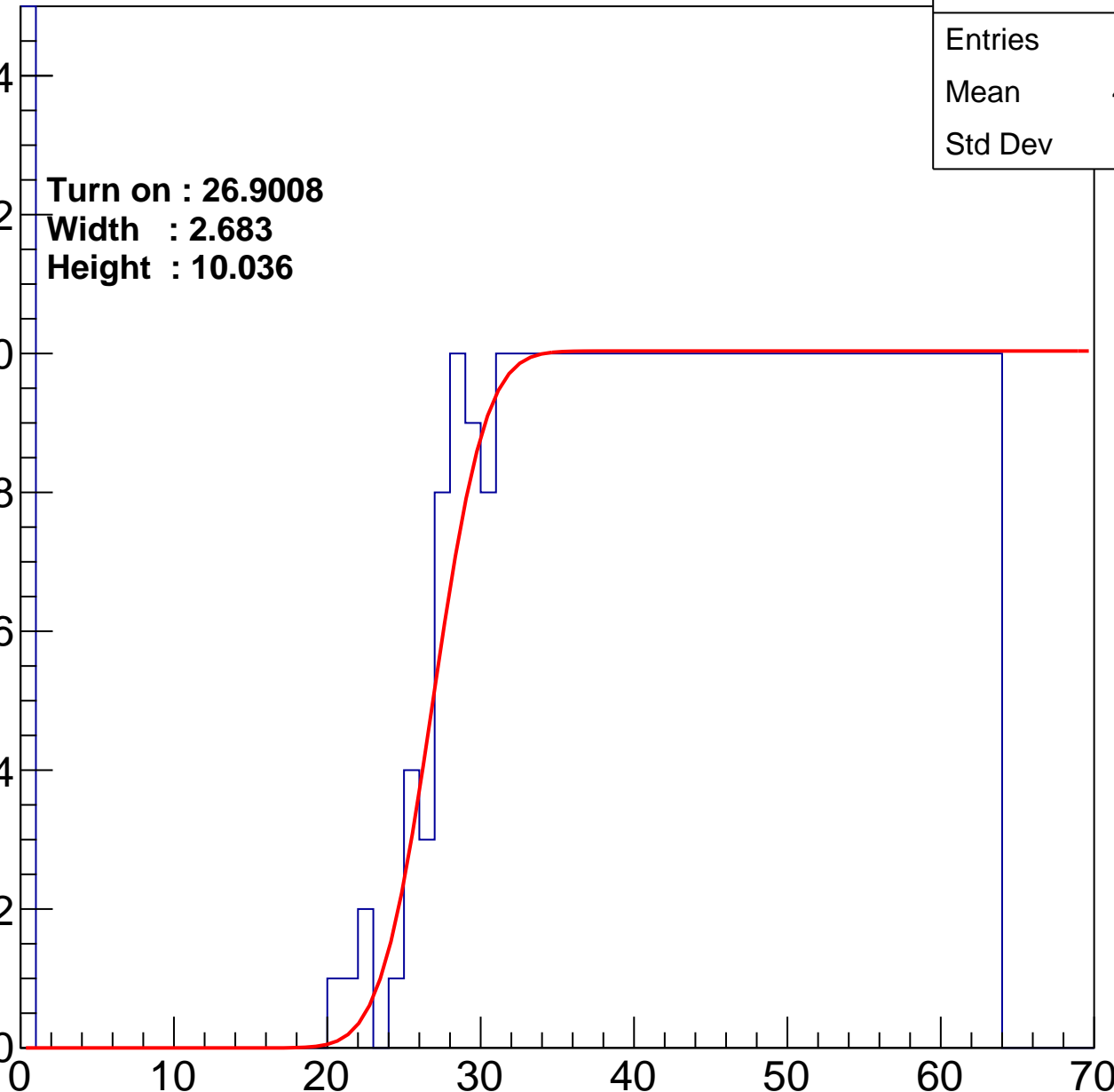
Width : 2.683

Height : 10.036

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch104

calib_packv5_041523_1651.root, FC#0, port C2

Entries	432
Mean	39.52
Std Dev	17.12

Turn on : 25.3891

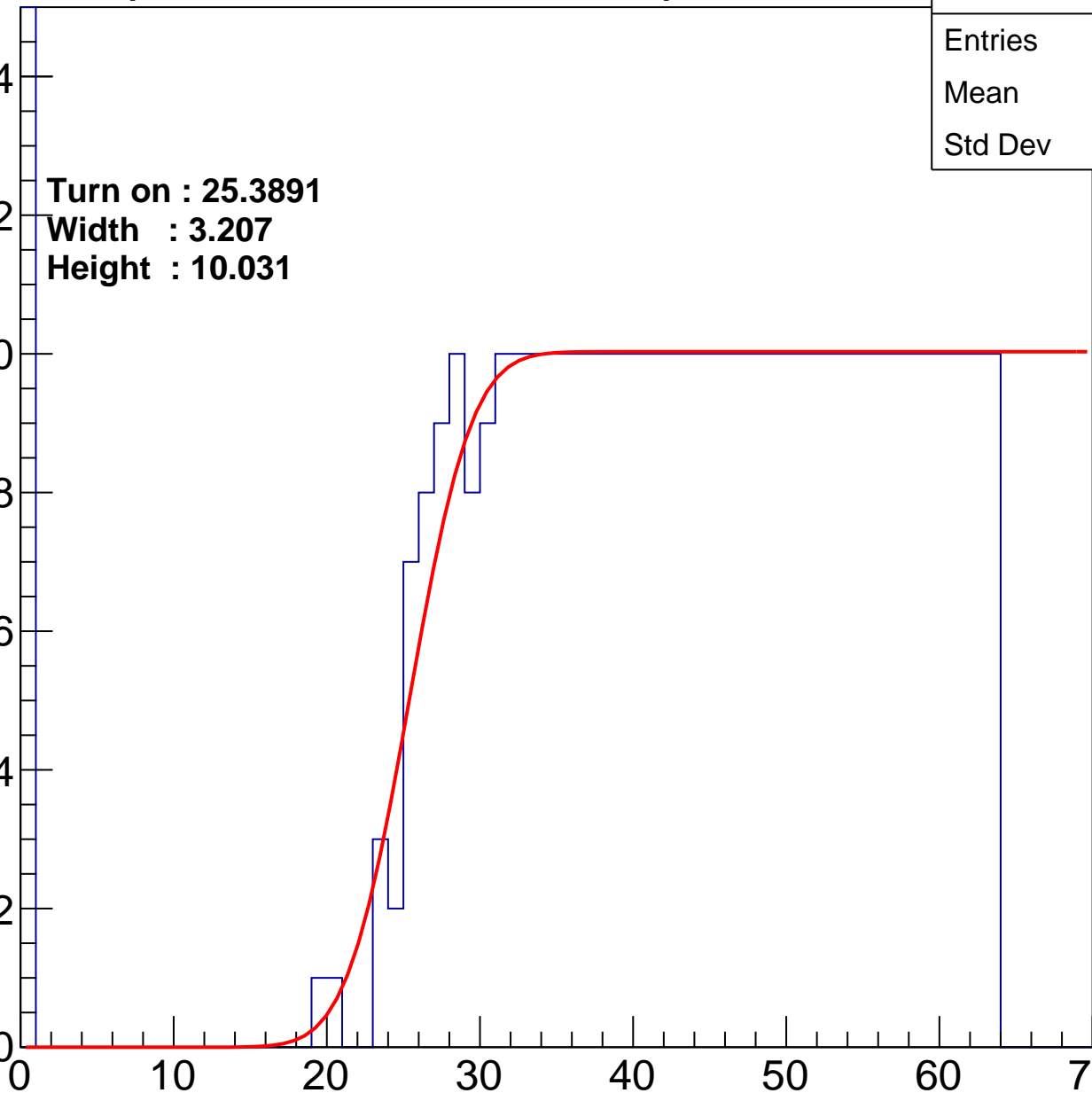
Width : 3.207

Height : 10.031

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch105

calib_packv5_041523_1651.root, FC#0, port C2

Entries	462
Mean	37.31
Std Dev	18.74

Turn on : 24.4598

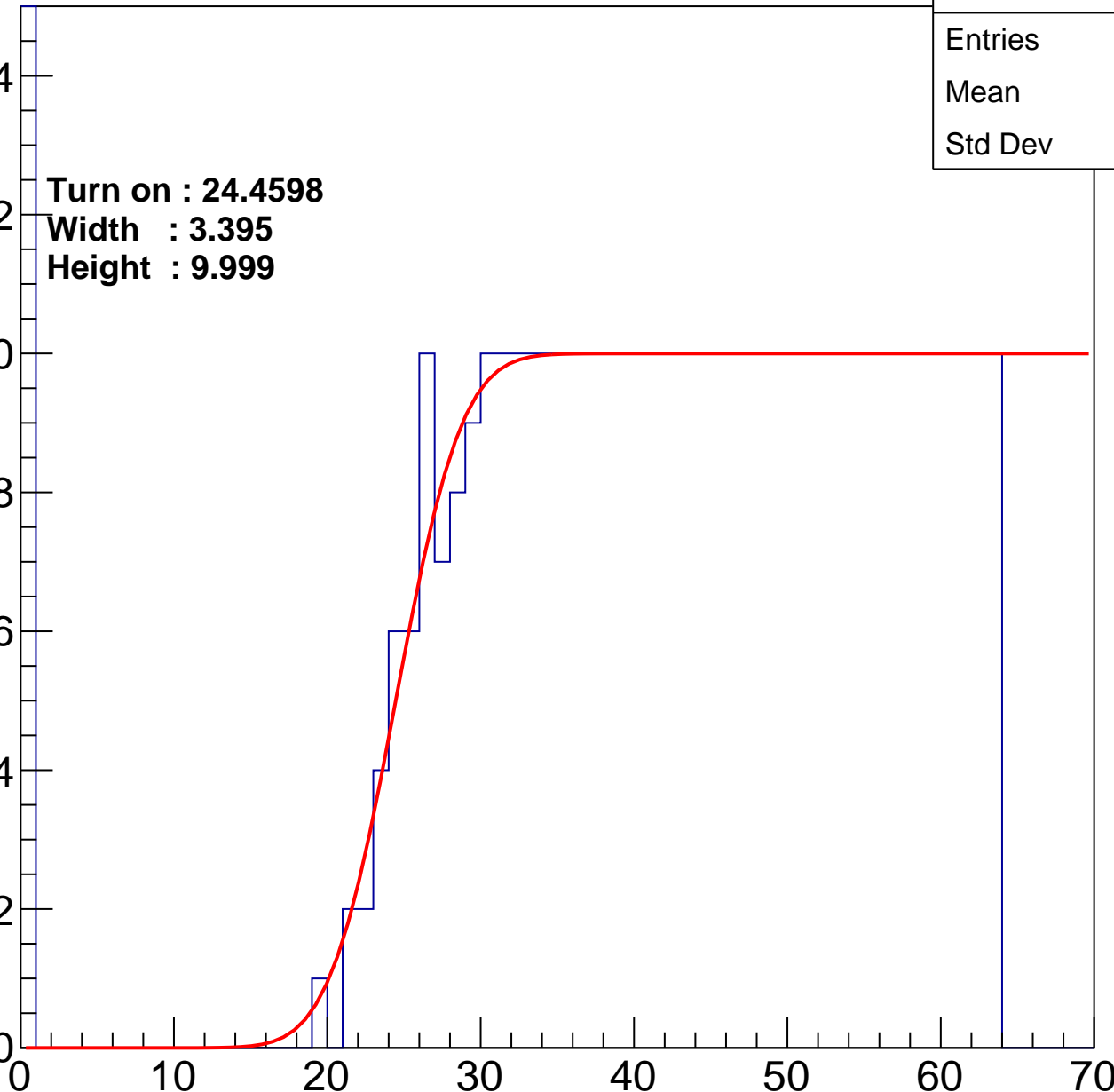
Width : 3.395

Height : 9.999

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch106

calib_packv5_041523_1651.root, FC#0, port C2

Entries	434
Mean	38.8
Std Dev	17.99

Turn on : 25.8006

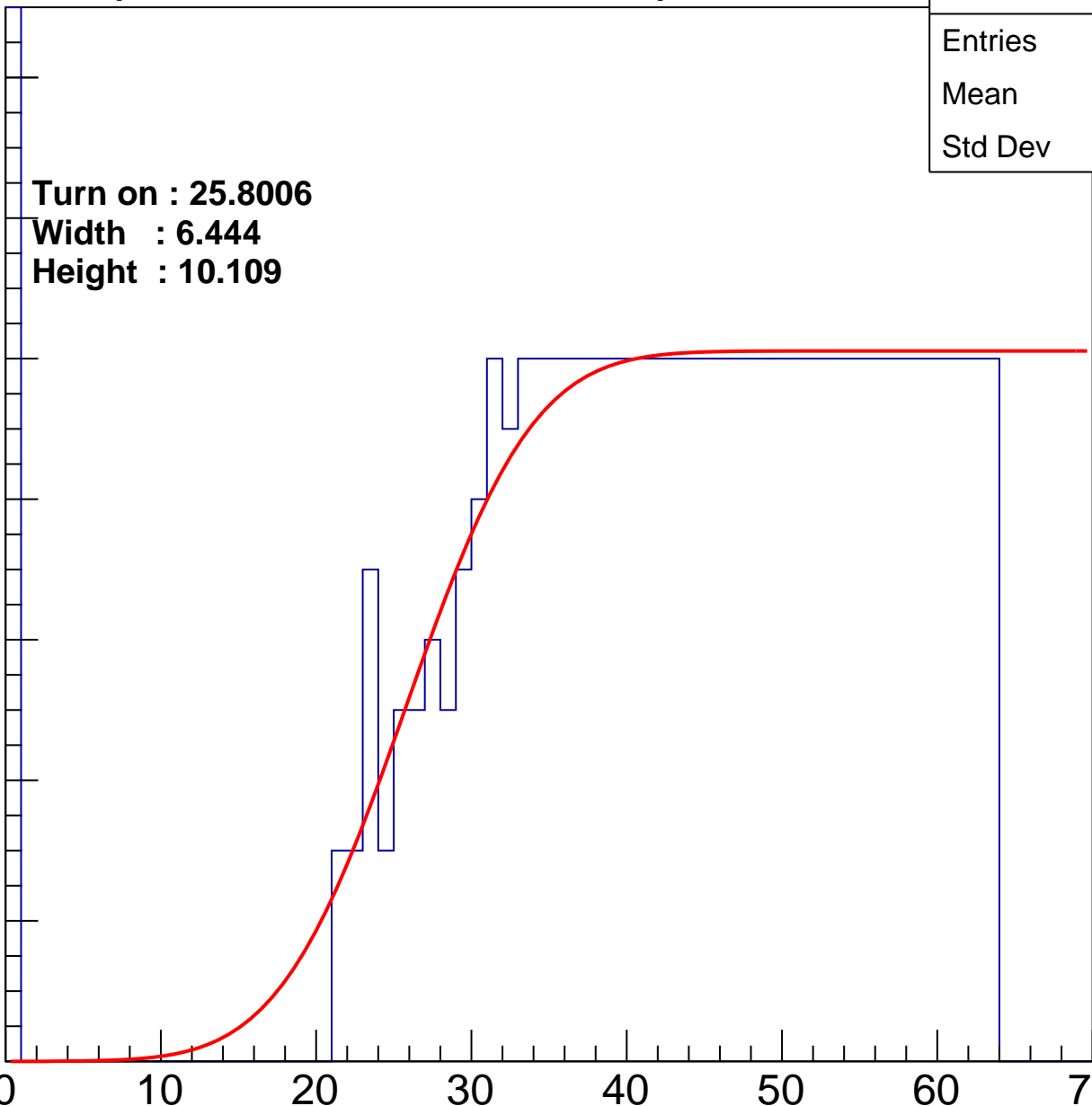
Width : 6.444

Height : 10.109

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch107

calib_packv5_041523_1651.root, FC#0, port C2

Entries	447
Mean	38.85
Std Dev	17.31

Turn on : 24.1128

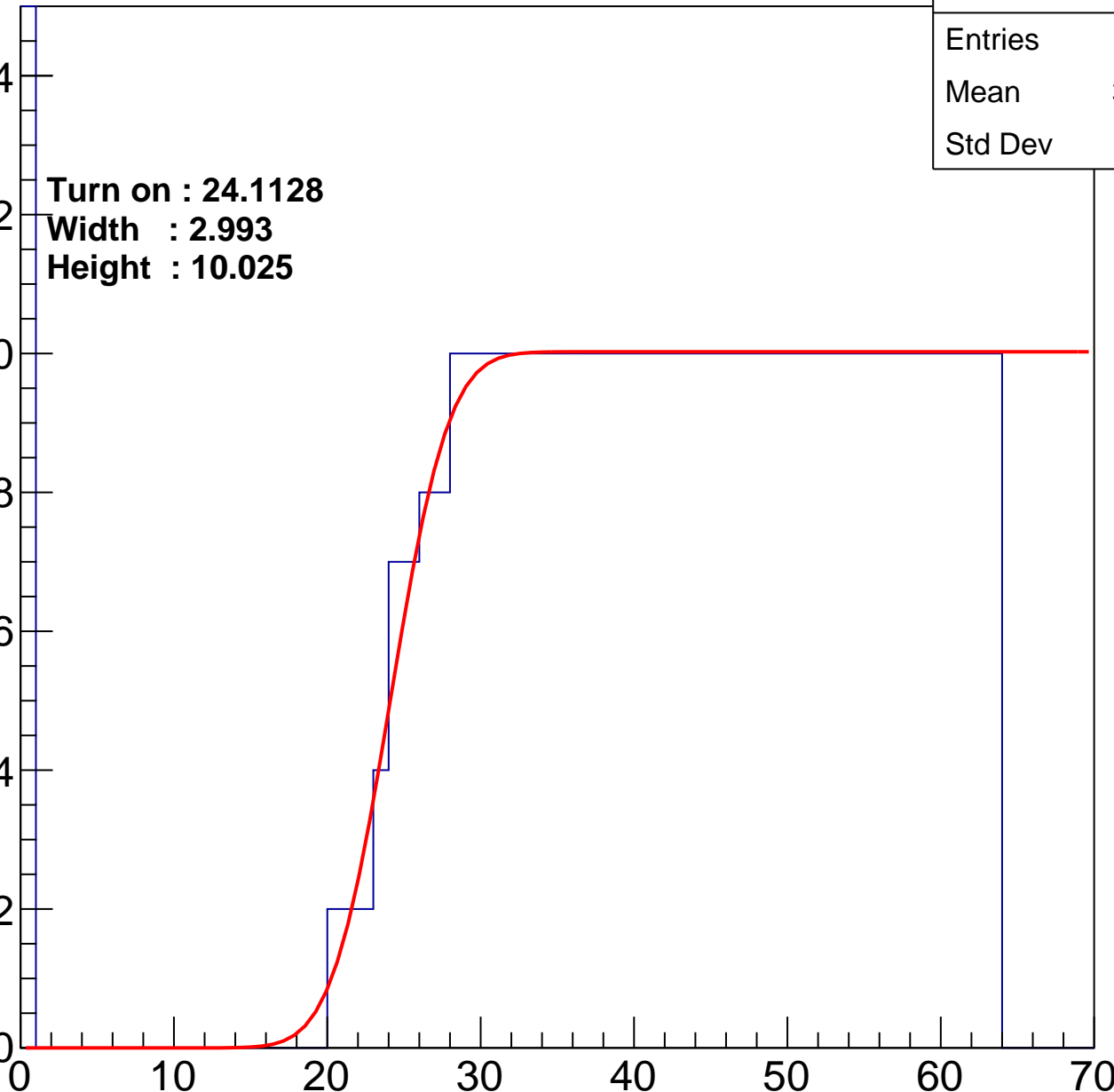
Width : 2.993

Height : 10.025

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch108

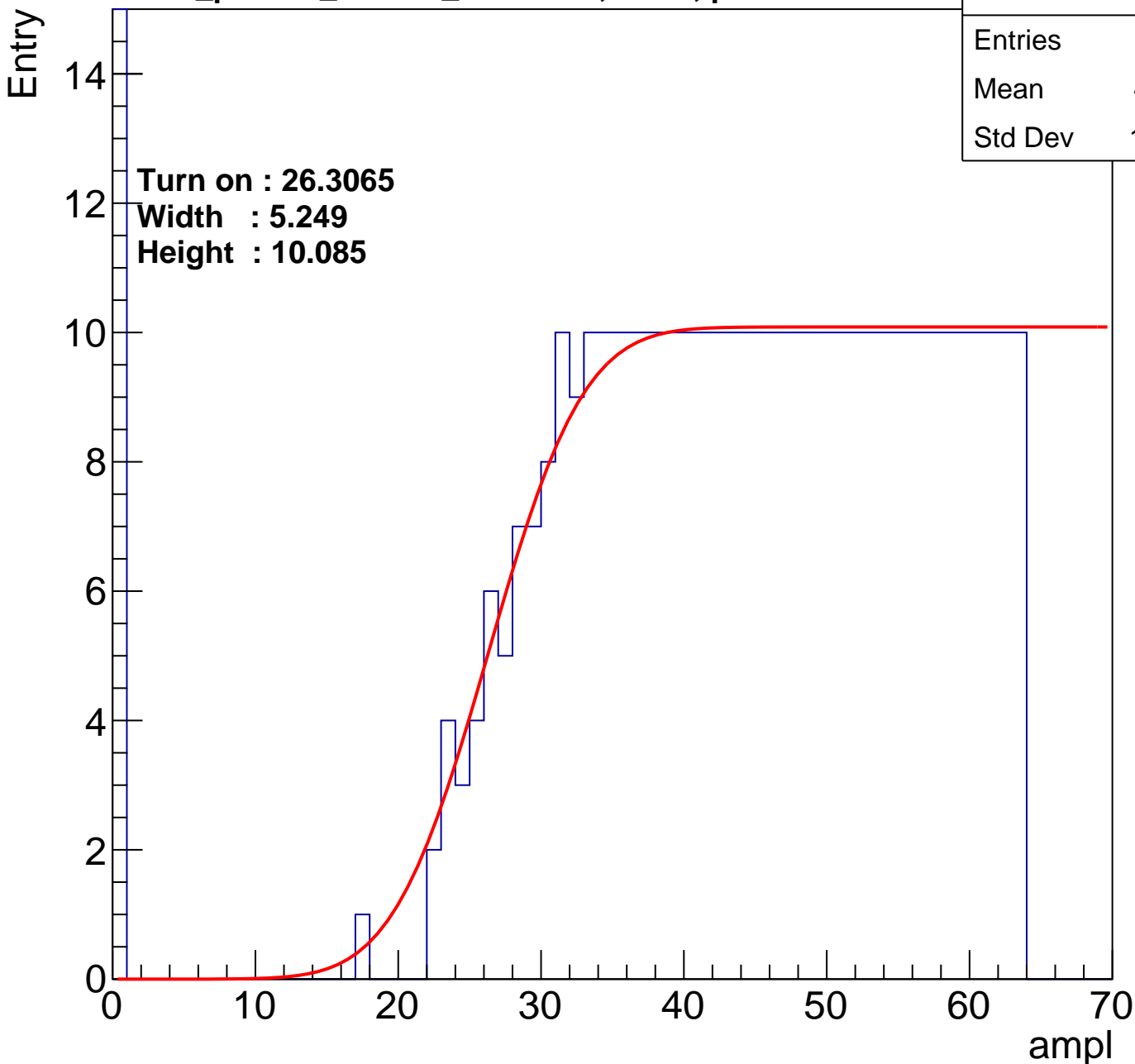
calib_packv5_041523_1651.root, FC#0, port C2

Entries	410
Mean	40.81
Std Dev	16.29

Turn on : 26.3065

Width : 5.249

Height : 10.085



B1L103S, U10-ch109

calib_packv5_041523_1651.root, FC#0, port C2

Entries	394
Mean	40.74
Std Dev	17.42

Turn on : 29.1787

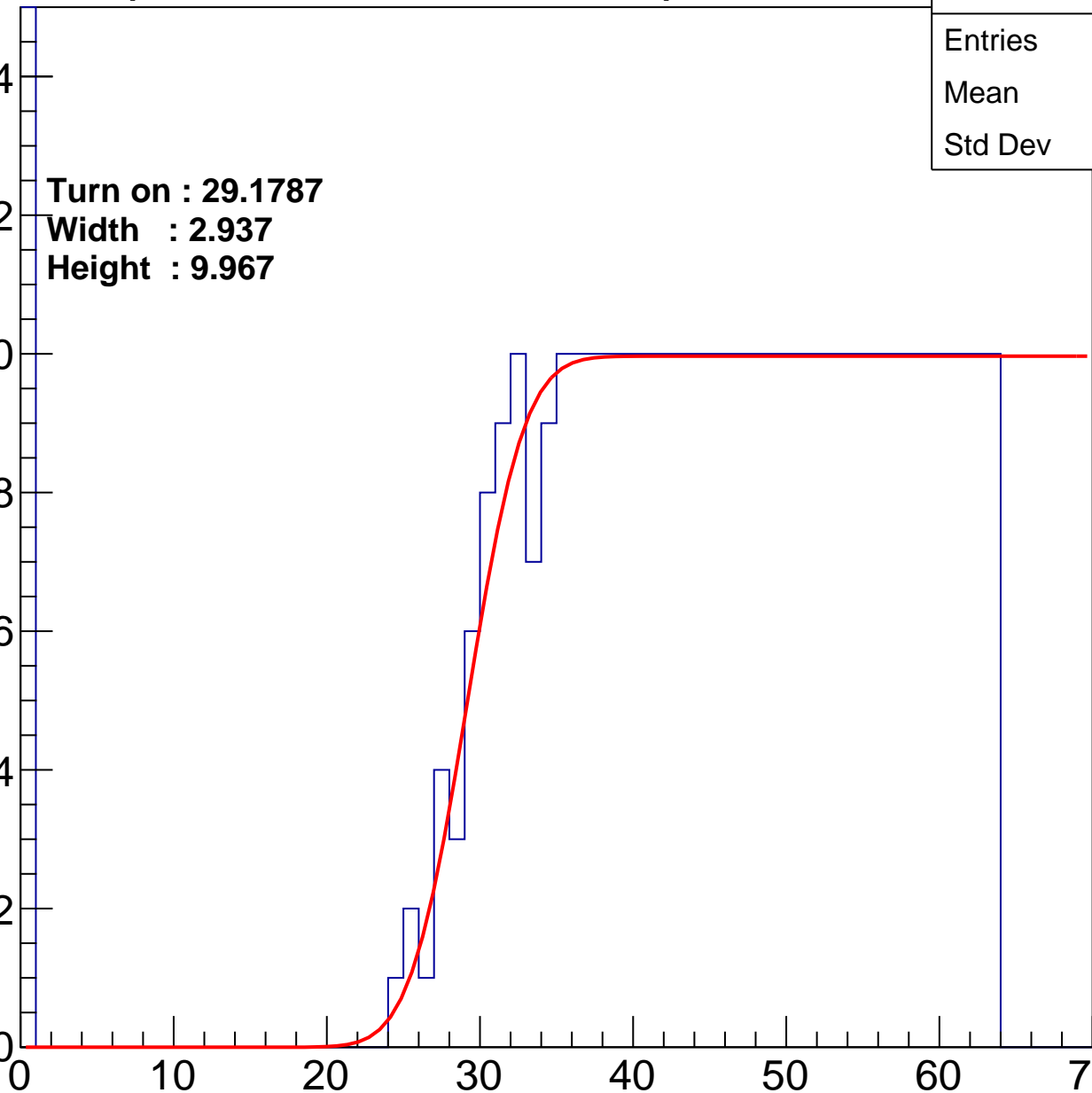
Width : 2.937

Height : 9.967

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch110

calib_packv5_041523_1651.root, FC#0, port C2

Entries	426
Mean	39.74
Std Dev	17.14

Turn on : 26.0278

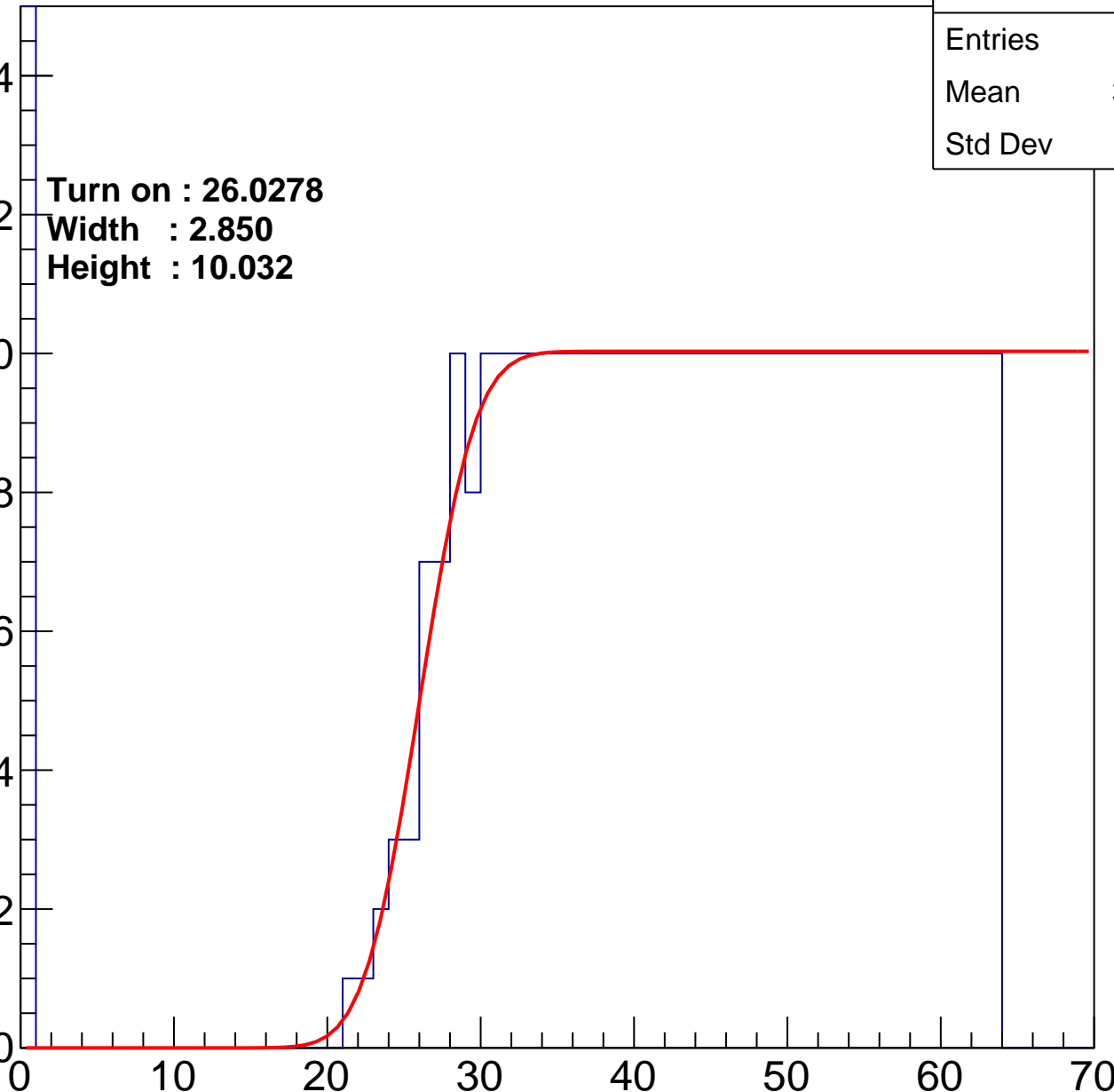
Width : 2.850

Height : 10.032

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch111

calib_packv5_041523_1651.root, FC#0, port C2

Entries	422
Mean	39.49
Std Dev	17.74

Turn on : 27.3197

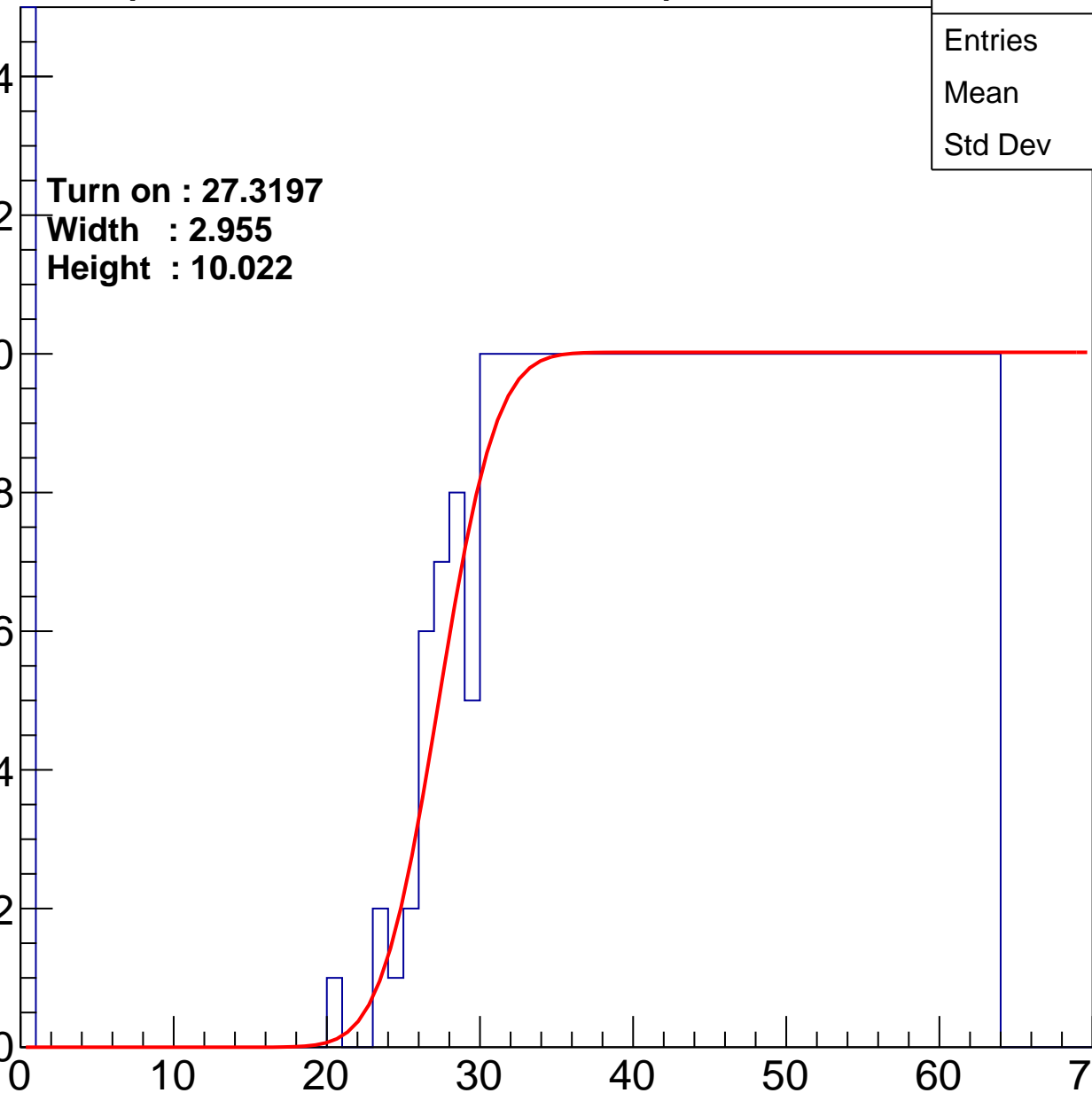
Width : 2.955

Height : 10.022

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch112

calib_packv5_041523_1651.root, FC#0, port C2

Entries	417
Mean	40.83
Std Dev	15.82

Turn on : 25.1973

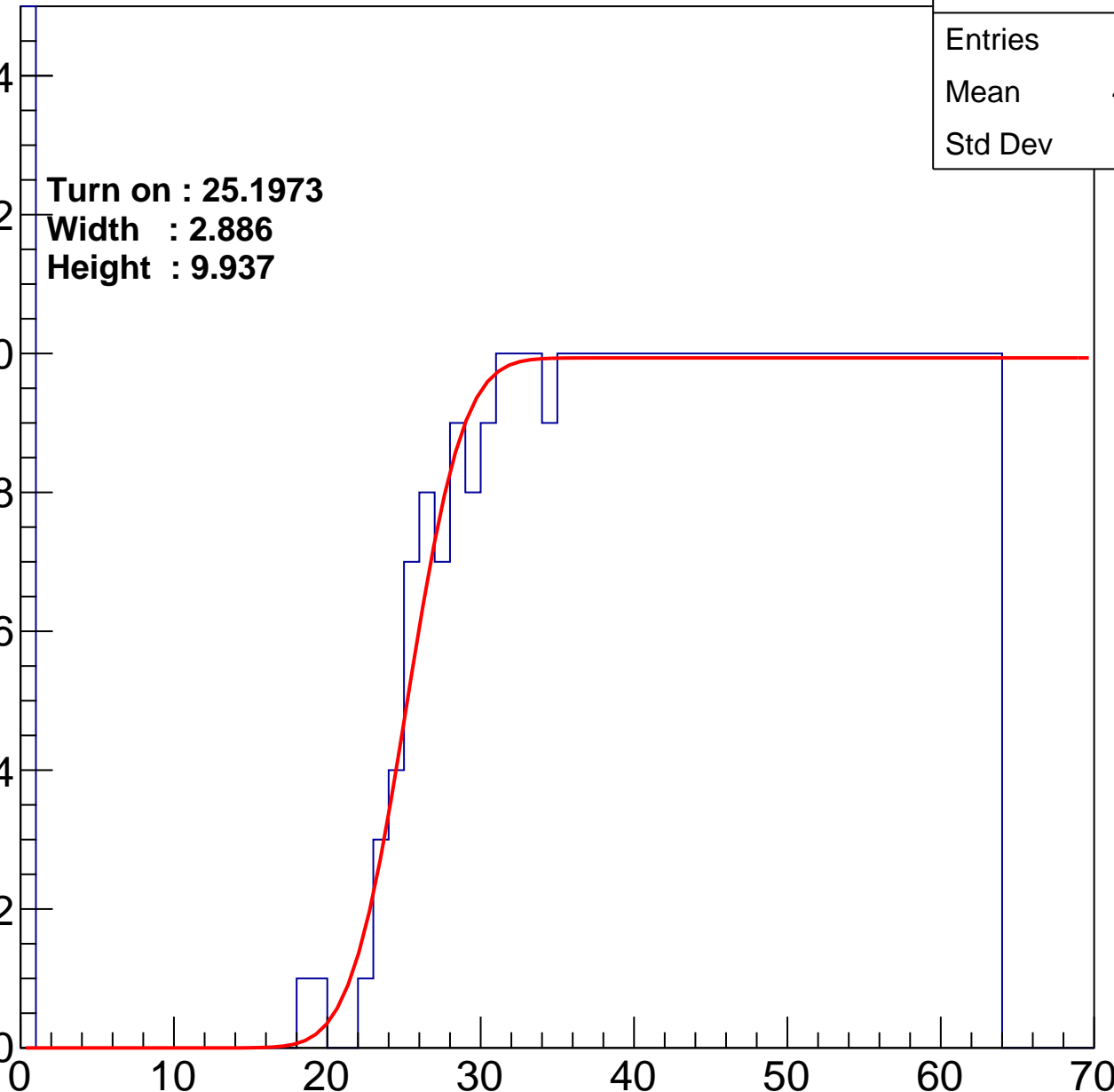
Width : 2.886

Height : 9.937

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch113

calib_packv5_041523_1651.root, FC#0, port C2

Entries	397
Mean	41.4
Std Dev	16.18

Turn on : 28.0363

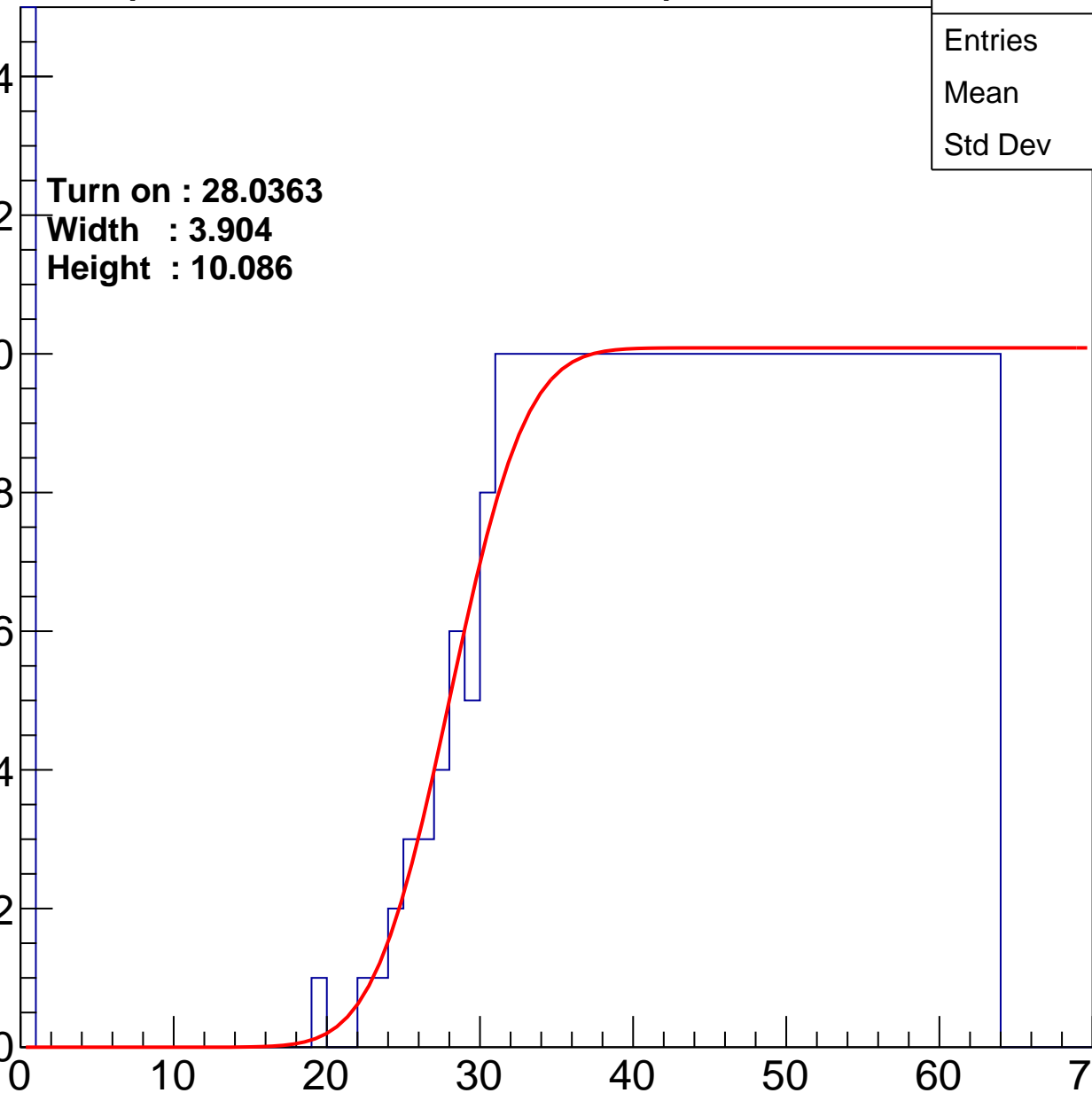
Width : 3.904

Height : 10.086

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch114

calib_packv5_041523_1651.root, FC#0, port C2

Entries	429
Mean	39.82
Std Dev	16.79

Turn on : 25.4454

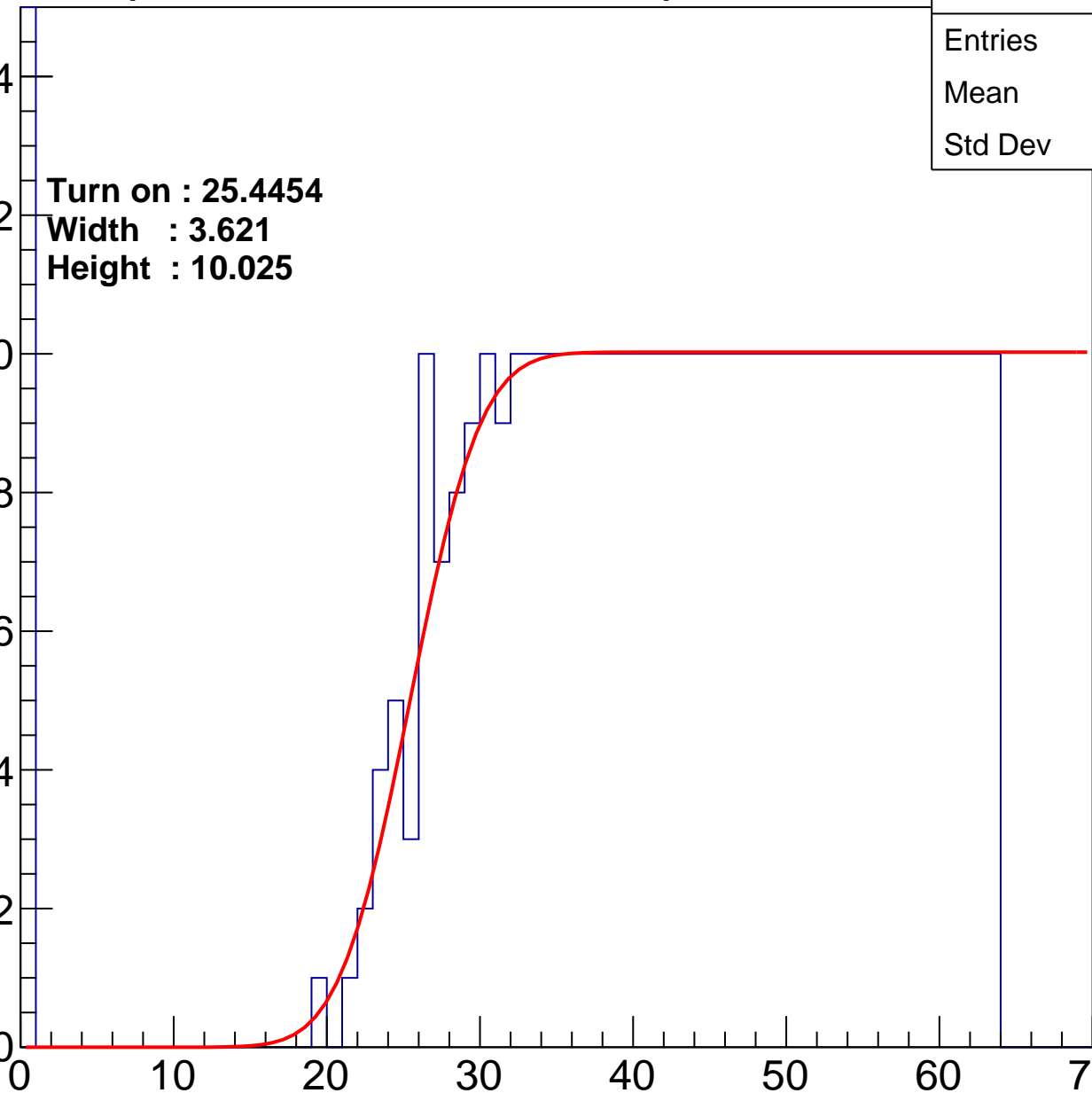
Width : 3.621

Height : 10.025

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch115

calib_packv5_041523_1651.root, FC#0, port C2

Entries	410
Mean	40.9
Std Dev	16.16

Turn on : 26.6620

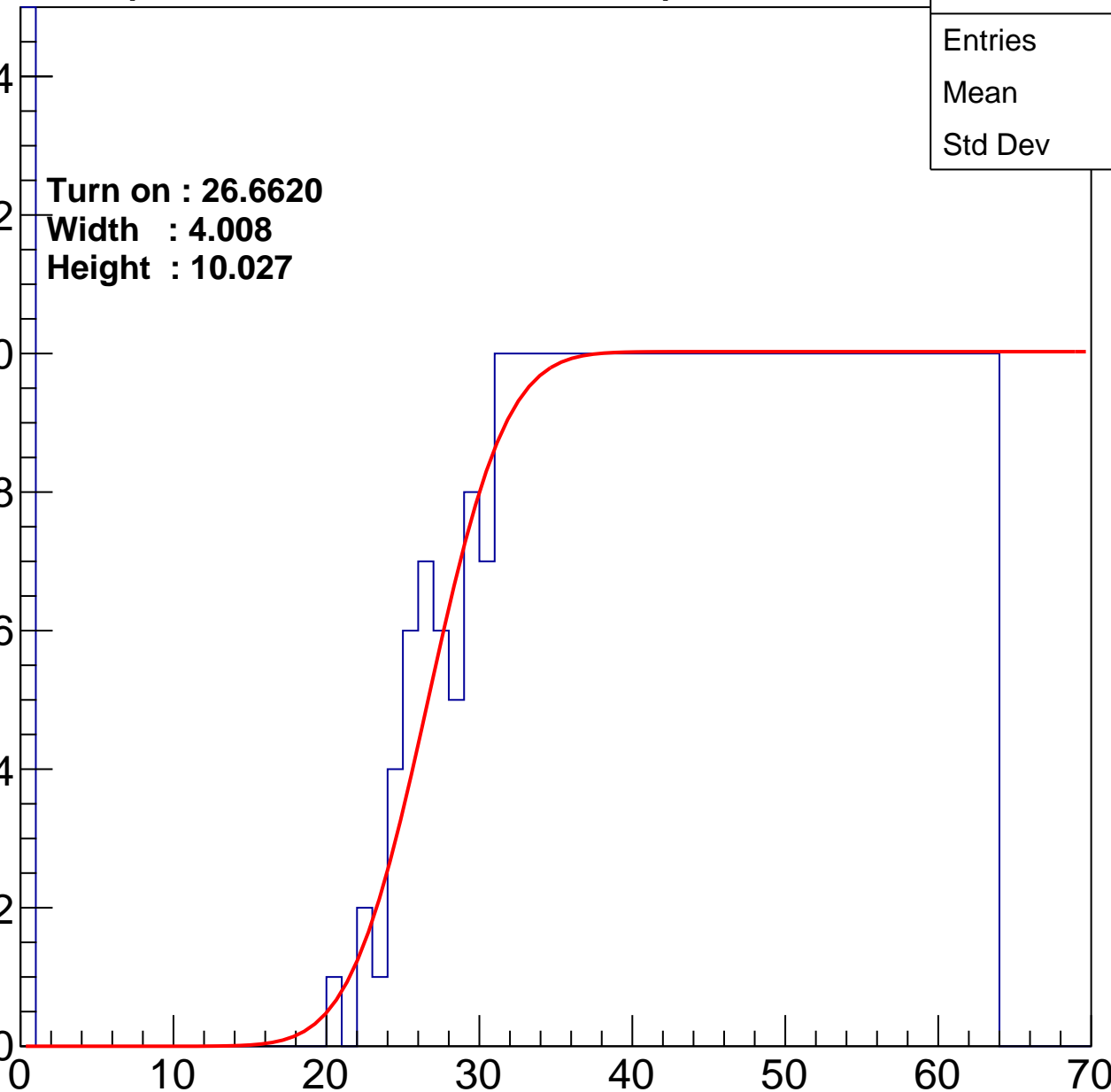
Width : 4.008

Height : 10.027

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch116

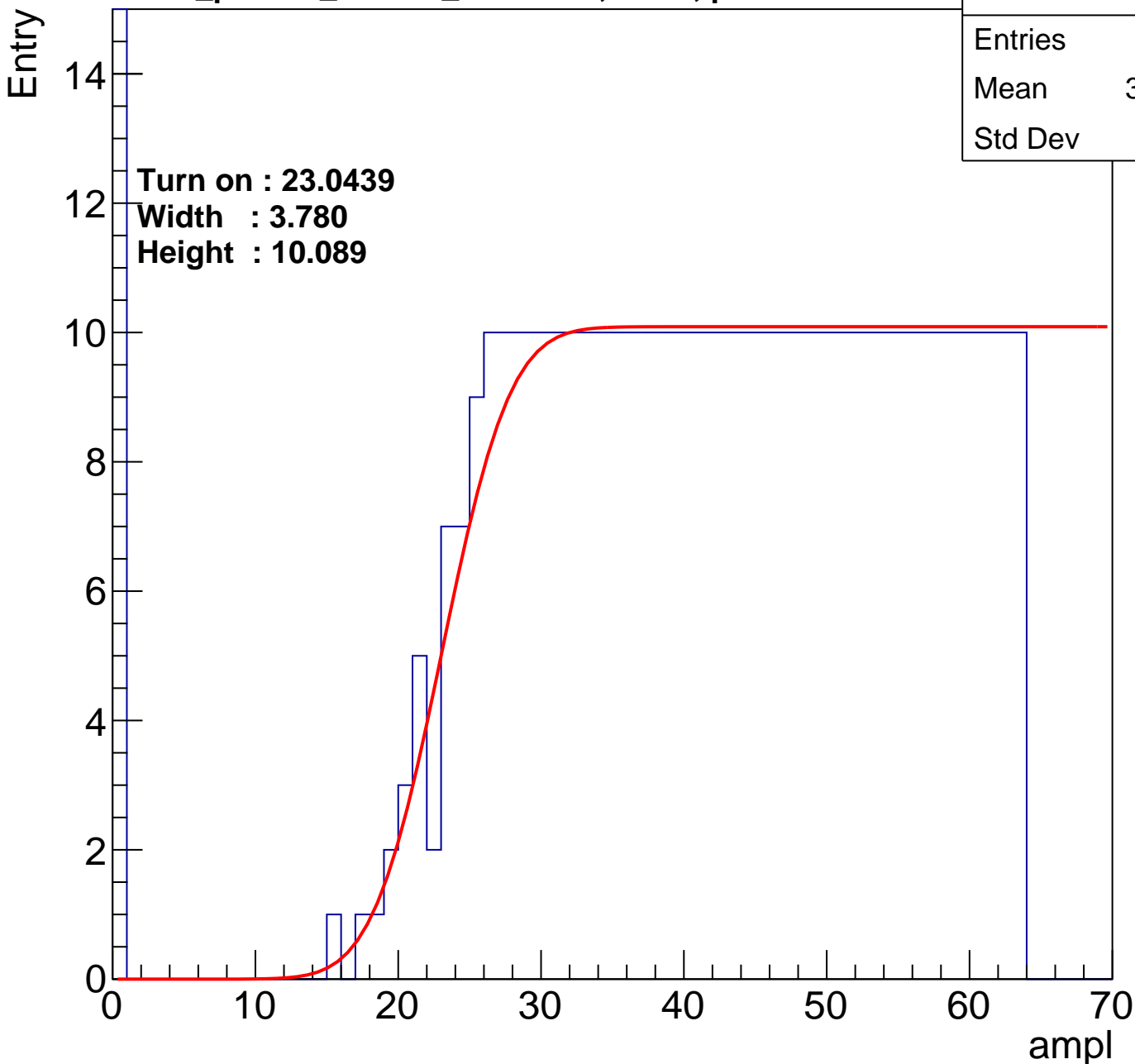
calib_packv5_041523_1651.root, FC#0, port C2

Entries	461
Mean	38.53
Std Dev	17

Turn on : 23.0439

Width : 3.780

Height : 10.089



B1L103S, U10-ch117

calib_packv5_041523_1651.root, FC#0, port C2

Entries	429
Mean	39.43
Std Dev	17.42

Turn on : 25.9632

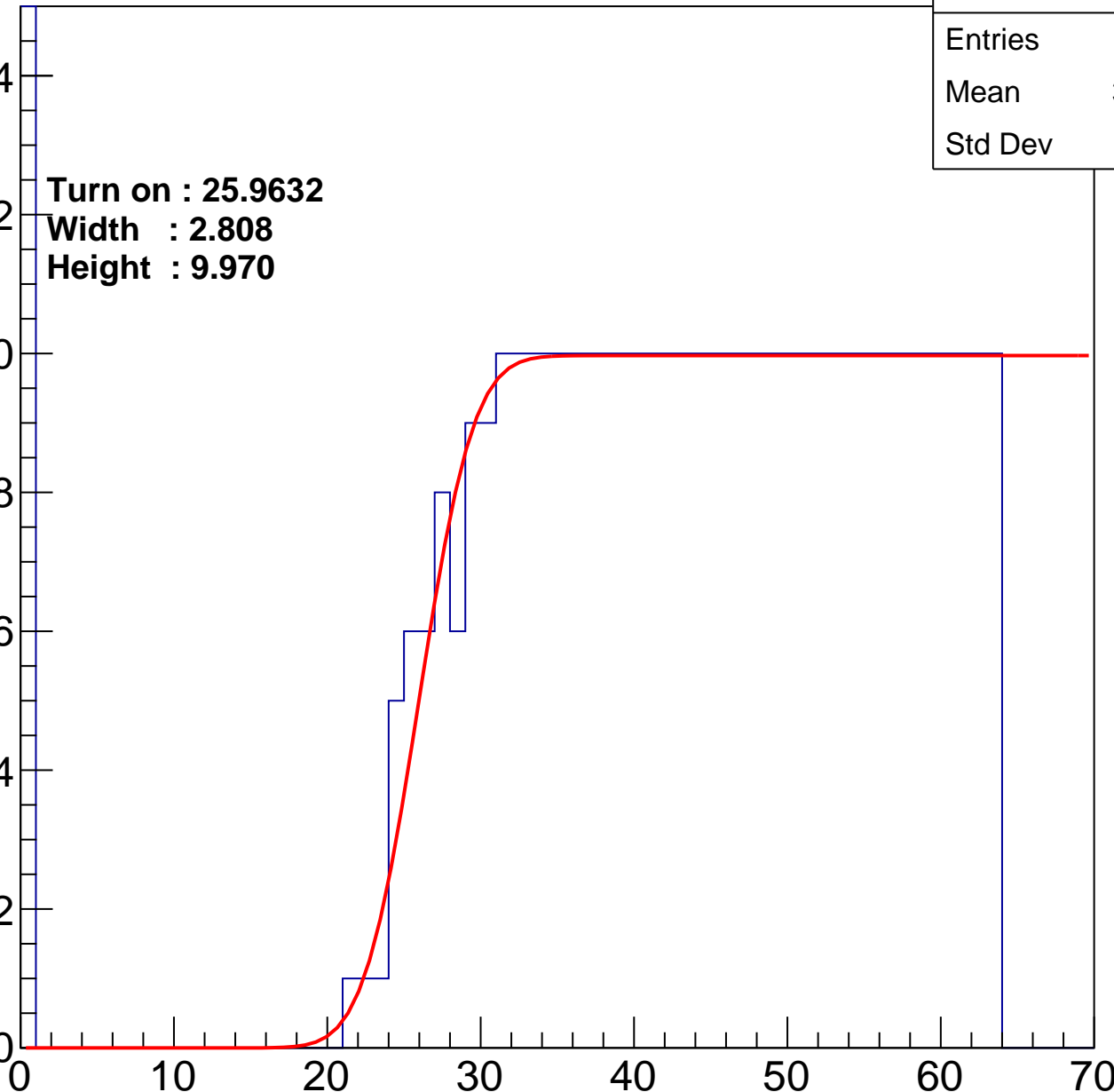
Width : 2.808

Height : 9.970

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch118

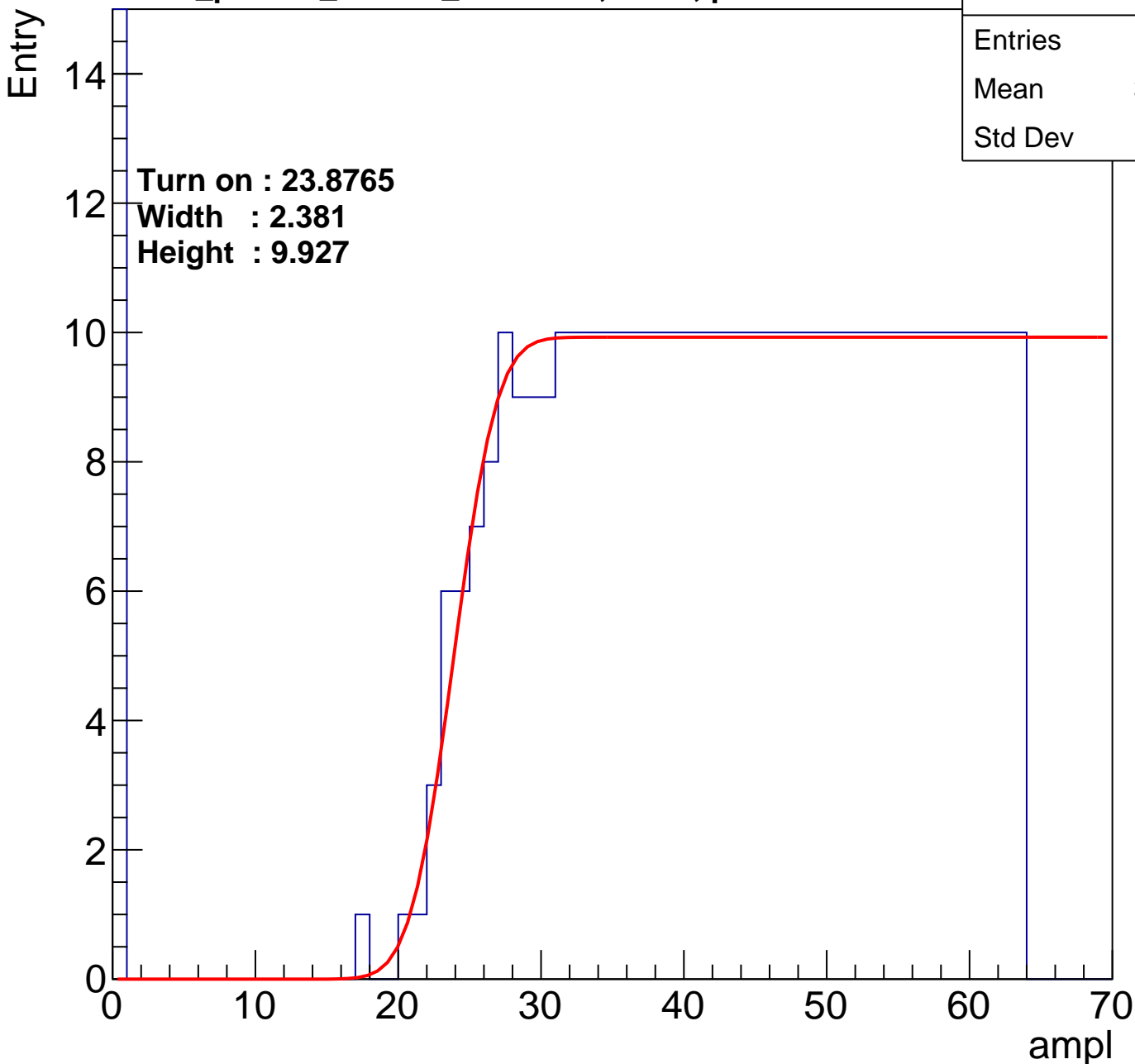
calib_packv5_041523_1651.root, FC#0, port C2

Entries	437
Mean	39.71
Std Dev	16.5

Turn on : 23.8765

Width : 2.381

Height : 9.927



B1L103S, U10-ch119

calib_packv5_041523_1651.root, FC#0, port C2

Entries	429
Mean	39.47
Std Dev	17.39

Turn on : 25.9867

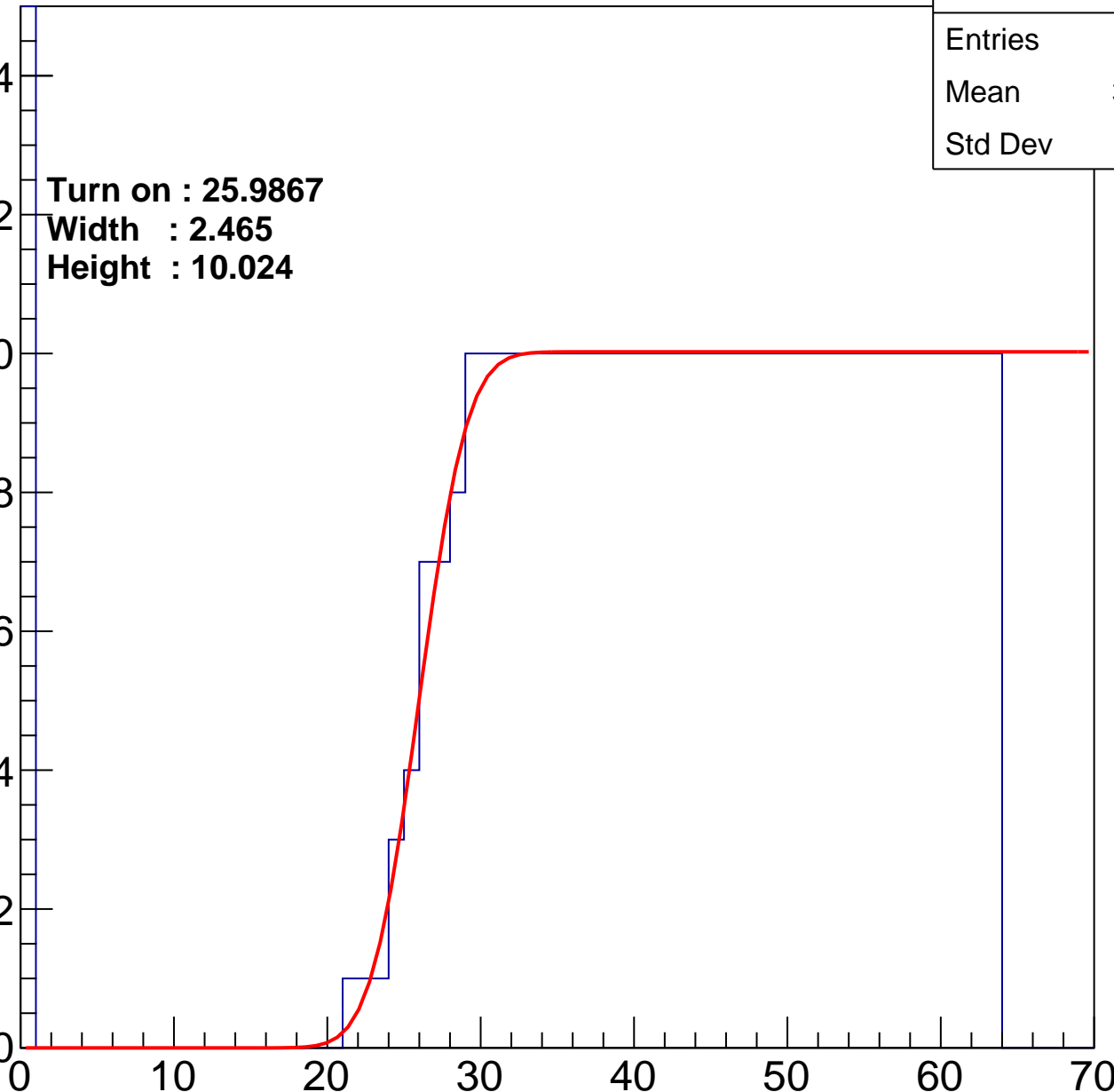
Width : 2.465

Height : 10.024

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch120

calib_packv5_041523_1651.root, FC#0, port C2

Entries	447
Mean	38.96
Std Dev	17.11

Turn on : 23.8456

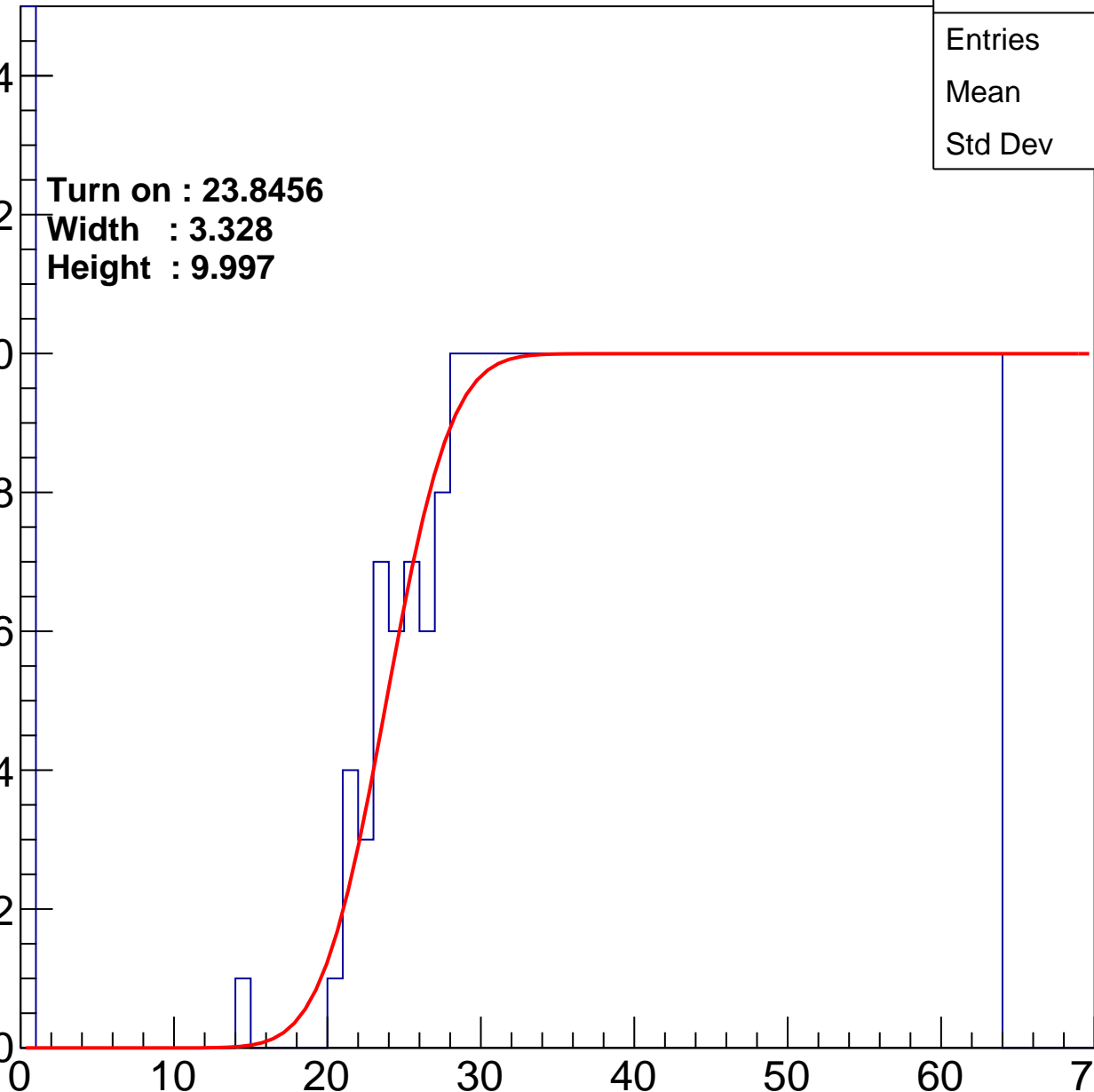
Width : 3.328

Height : 9.997

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch121

calib_packv5_041523_1651.root, FC#0, port C2

Entries	429
Mean	40.28
Std Dev	16.02

Turn on : 24.5465

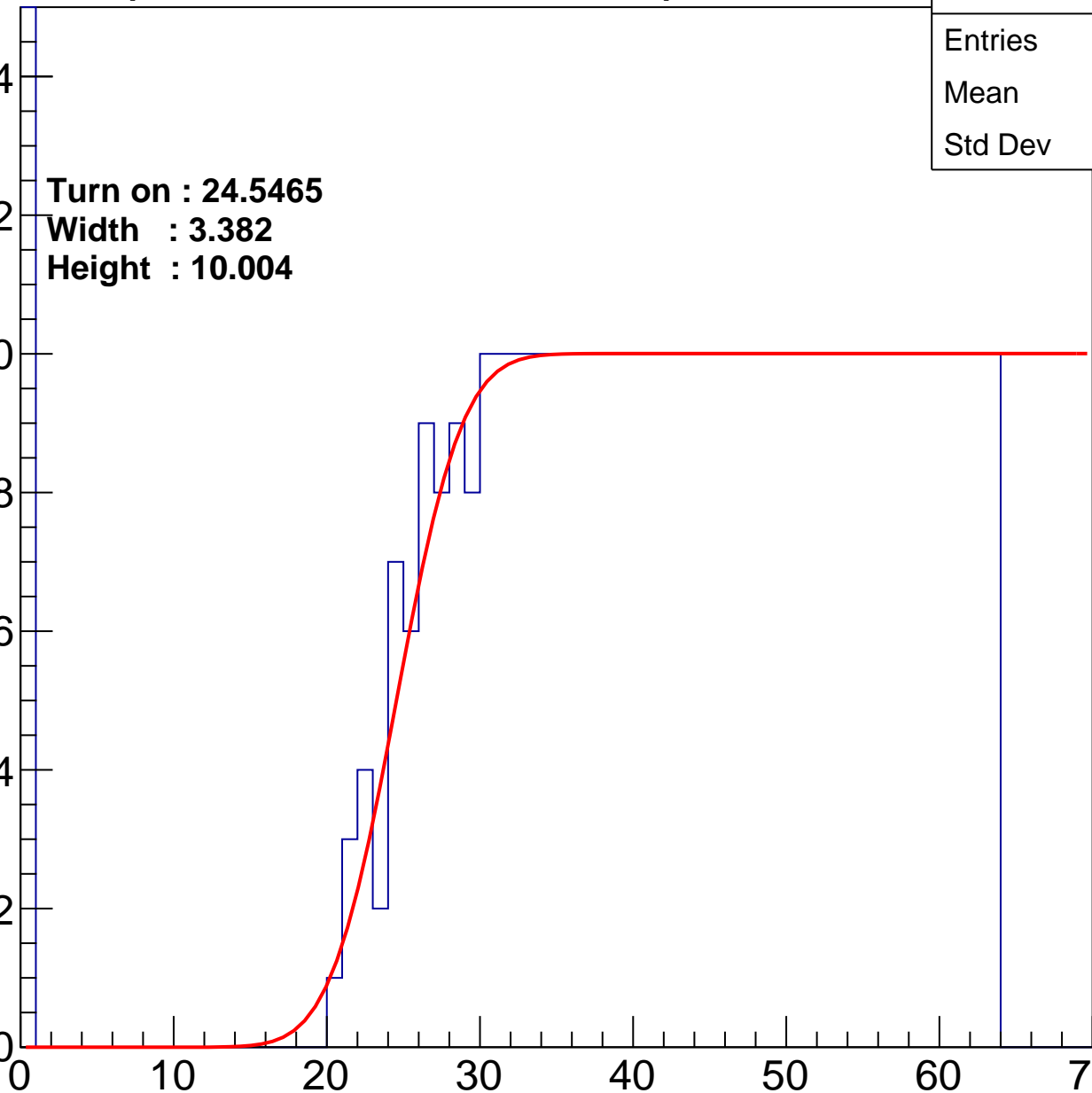
Width : 3.382

Height : 10.004

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch122

calib_packv5_041523_1651.root, FC#0, port C2

Entries	467
Mean	37.4
Std Dev	18.38

Turn on : 23.6434

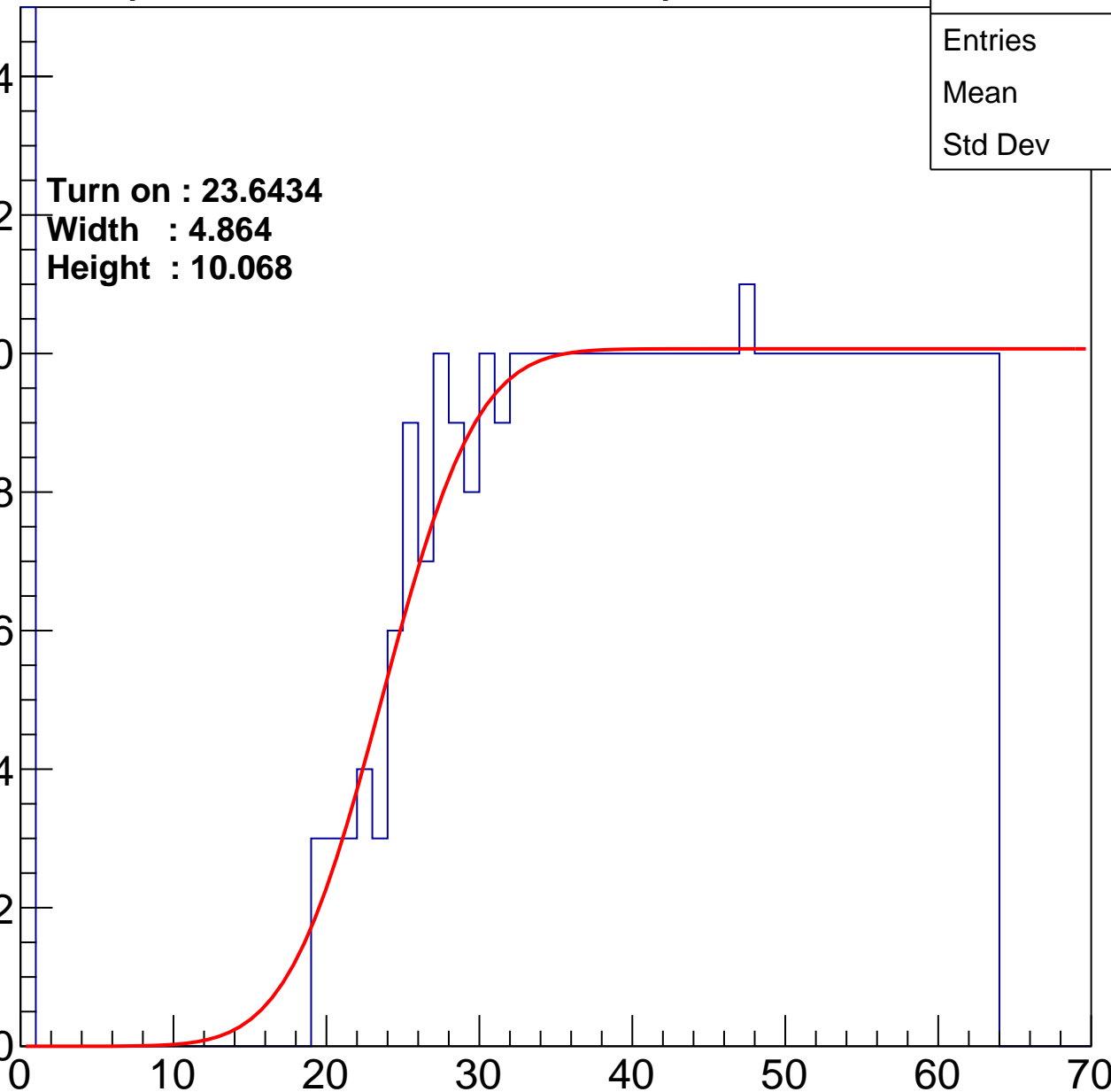
Width : 4.864

Height : 10.068

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch123

calib_packv5_041523_1651.root, FC#0, port C2

Entries	415
Mean	39.72
Std Dev	17.79

Turn on : 27.7708

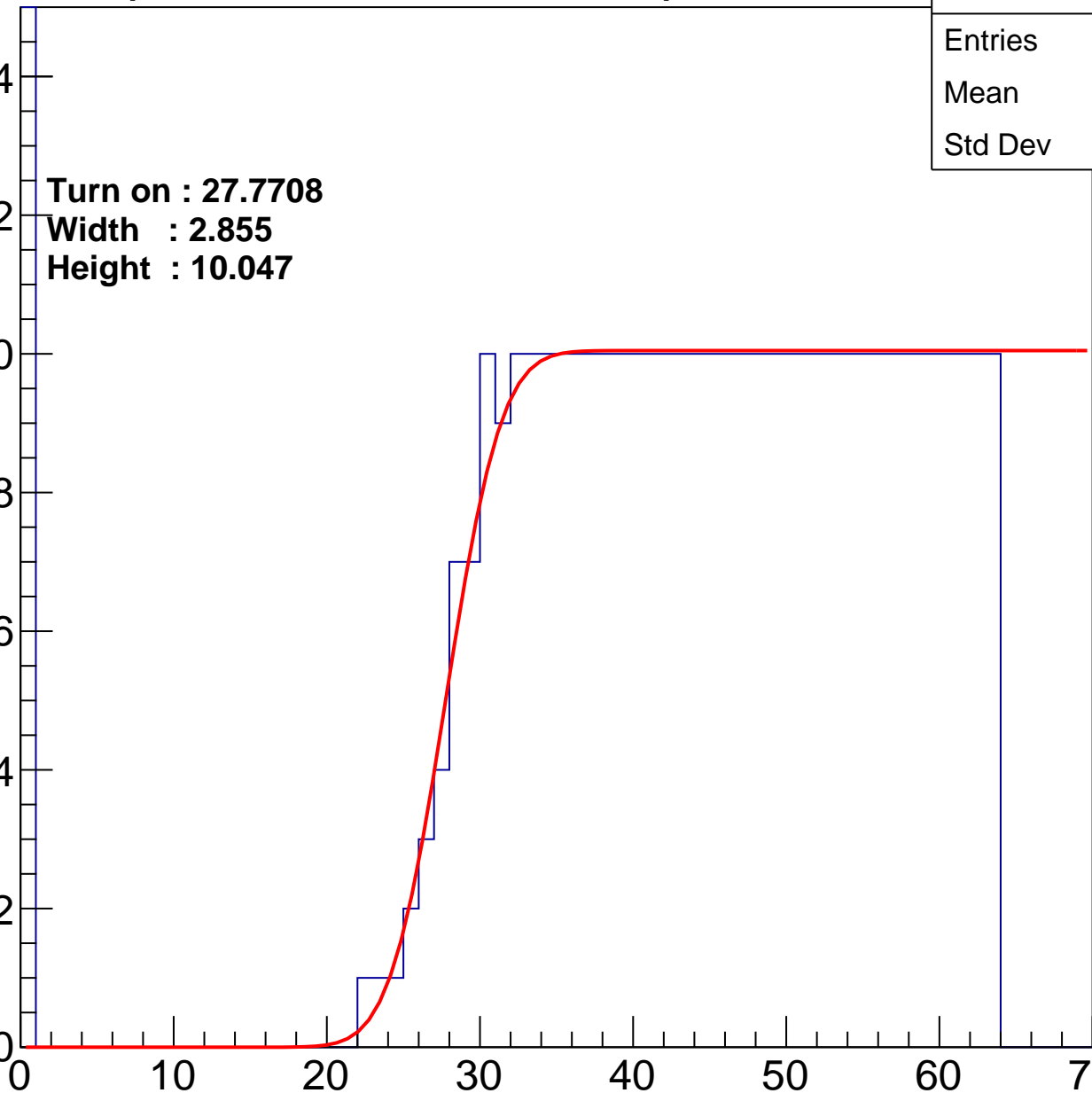
Width : 2.855

Height : 10.047

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch124

calib_packv5_041523_1651.root, FC#0, port C2

Entries	420
Mean	39.88
Std Dev	17.22

Turn on : 26.8666

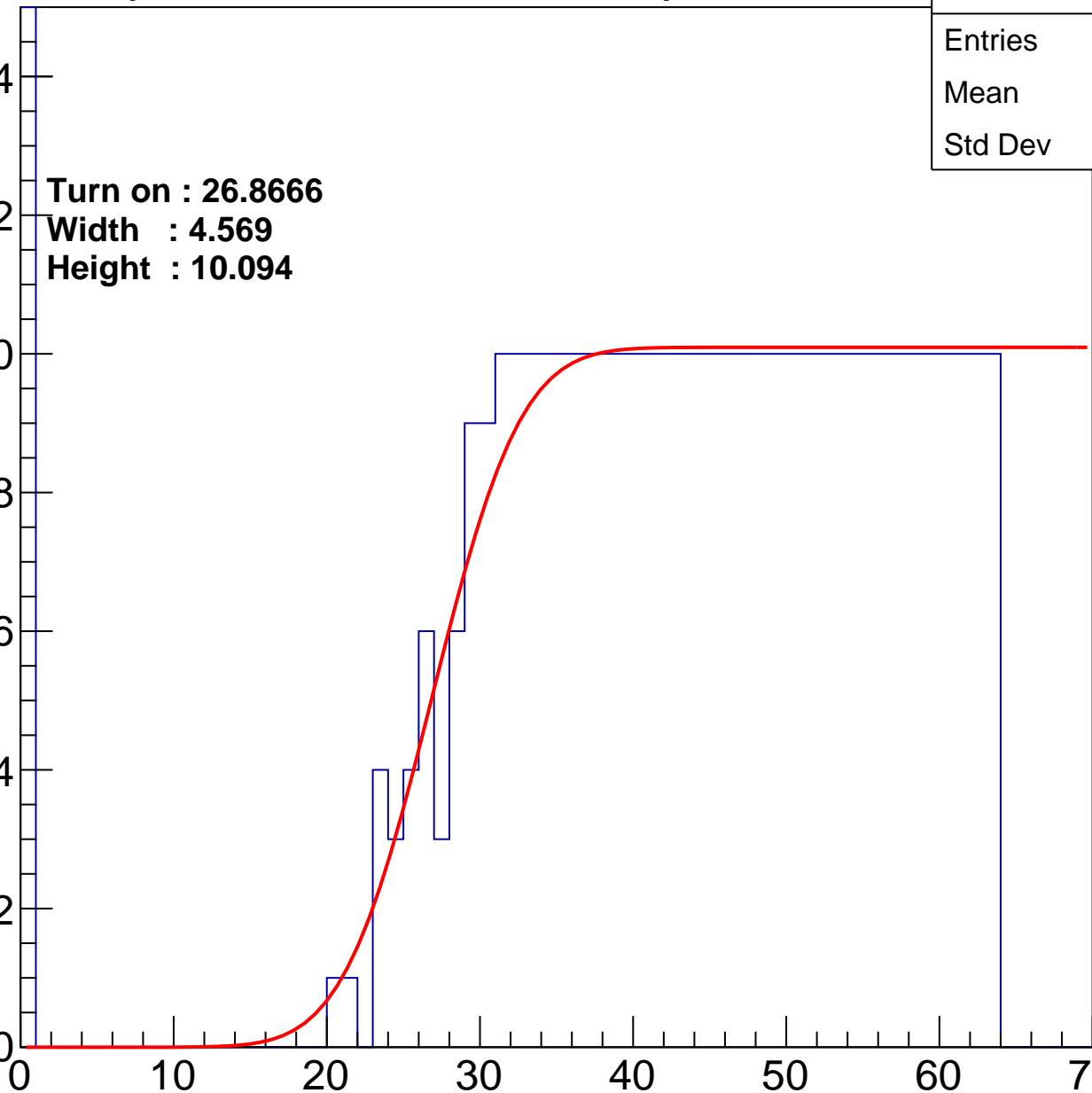
Width : 4.569

Height : 10.094

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch125

calib_packv5_041523_1651.root, FC#0, port C2

Entries	419
Mean	39.25
Std Dev	18.23

Turn on : 28.5138

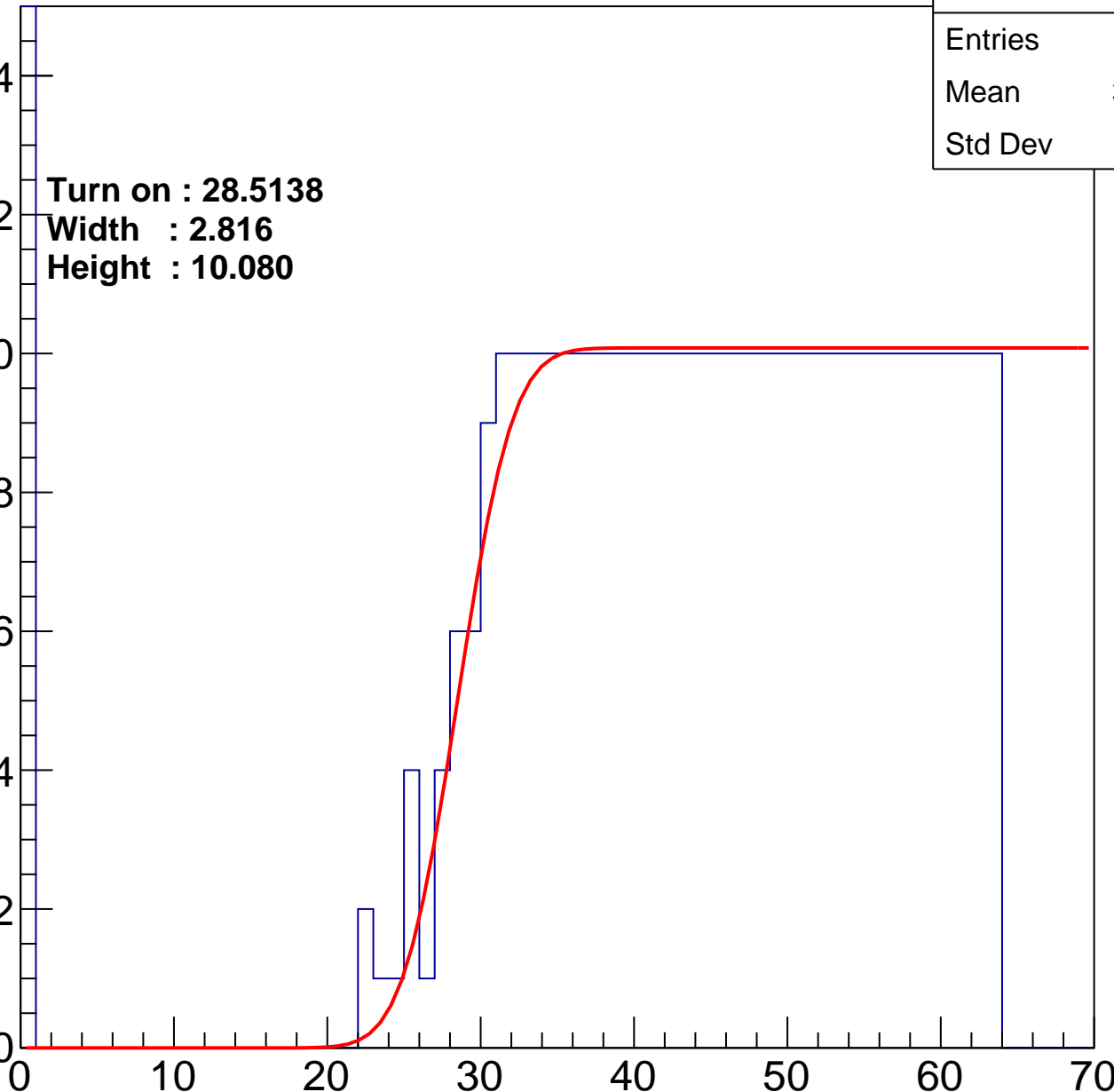
Width : 2.816

Height : 10.080

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch126

calib_packv5_041523_1651.root, FC#0, port C2

Entries	438
Mean	39.08
Std Dev	17.41

Turn on : 25.2433

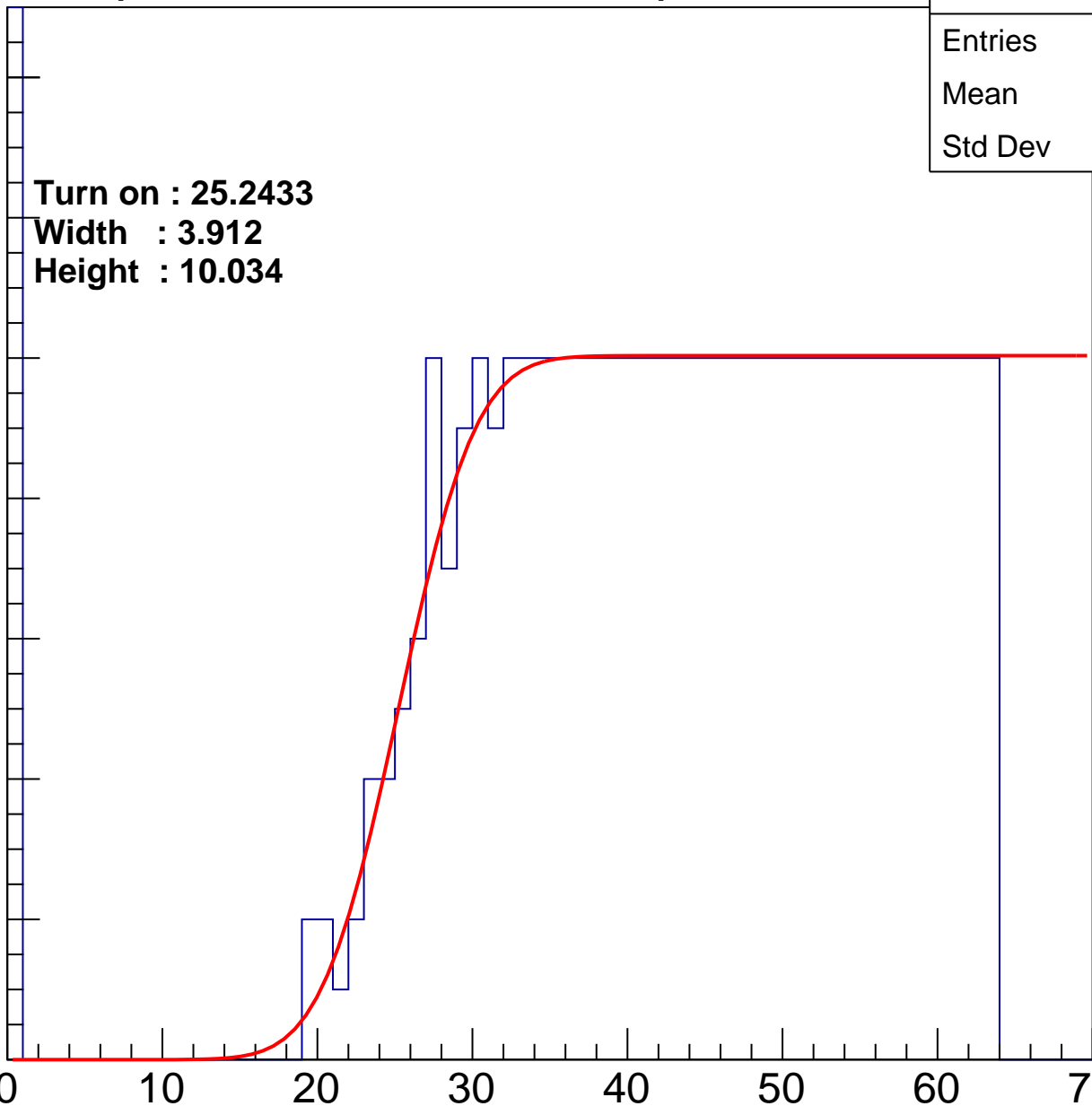
Width : 3.912

Height : 10.034

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch127

calib_packv5_041523_1651.root, FC#0, port C2

Entries	424
Mean	40
Std Dev	16.77

Turn on : 25.7055

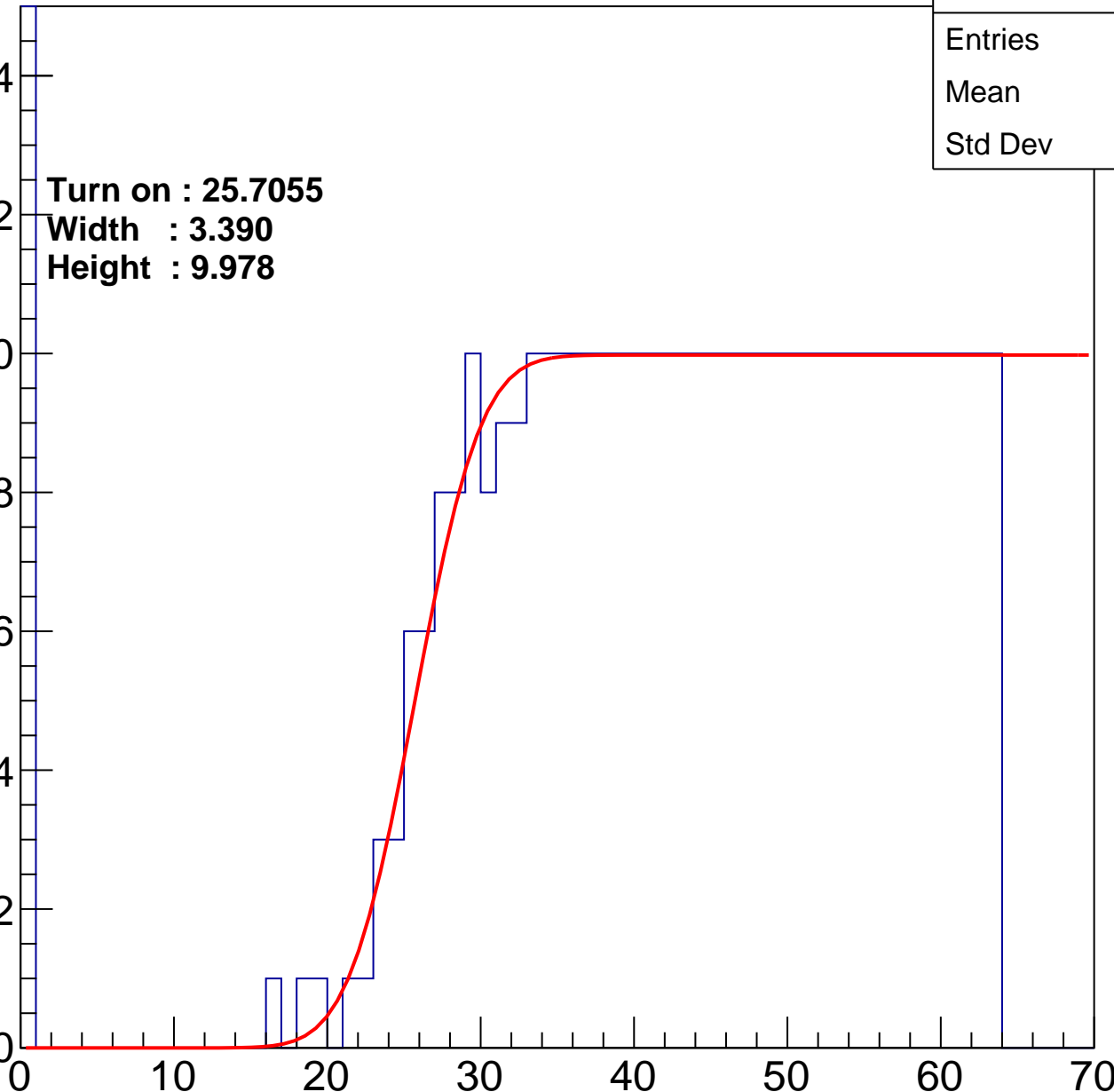
Width : 3.390

Height : 9.978

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U10-ch127

calib_packv5_041523_1651.root, FC#0, port C2

Entries	424
Mean	40
Std Dev	16.77

Turn on : 25.7055

Width : 3.390

Height : 9.978

Entry

14
12
10
8
6
4
2
0

ampl

