



# B1L101S, U11-ch0, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	77
Mean	29.29
Std Dev	5.175

**Gaus mean : 30.7271**

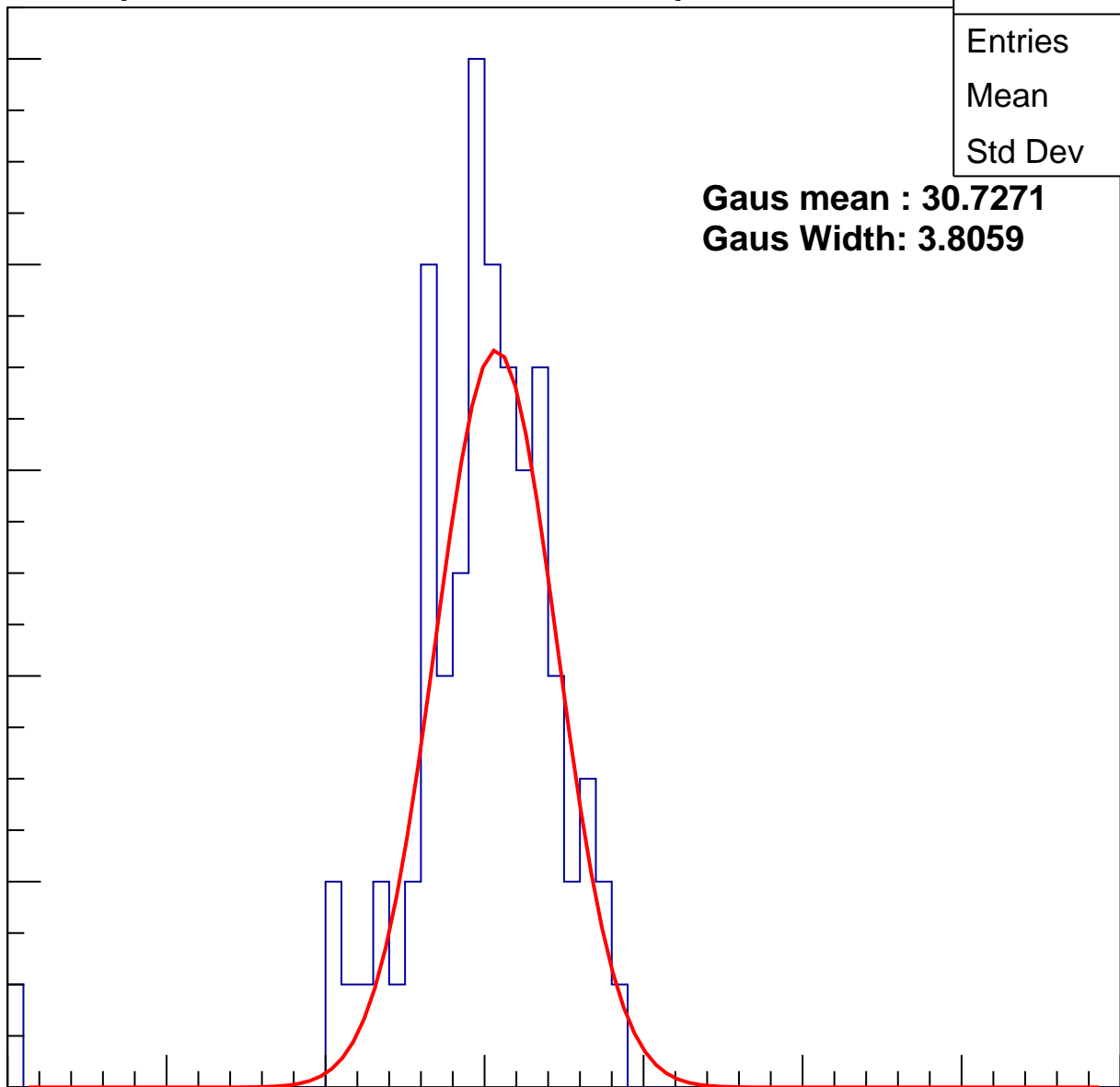
**Gaus Width: 3.8059**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U11-ch0, adc1

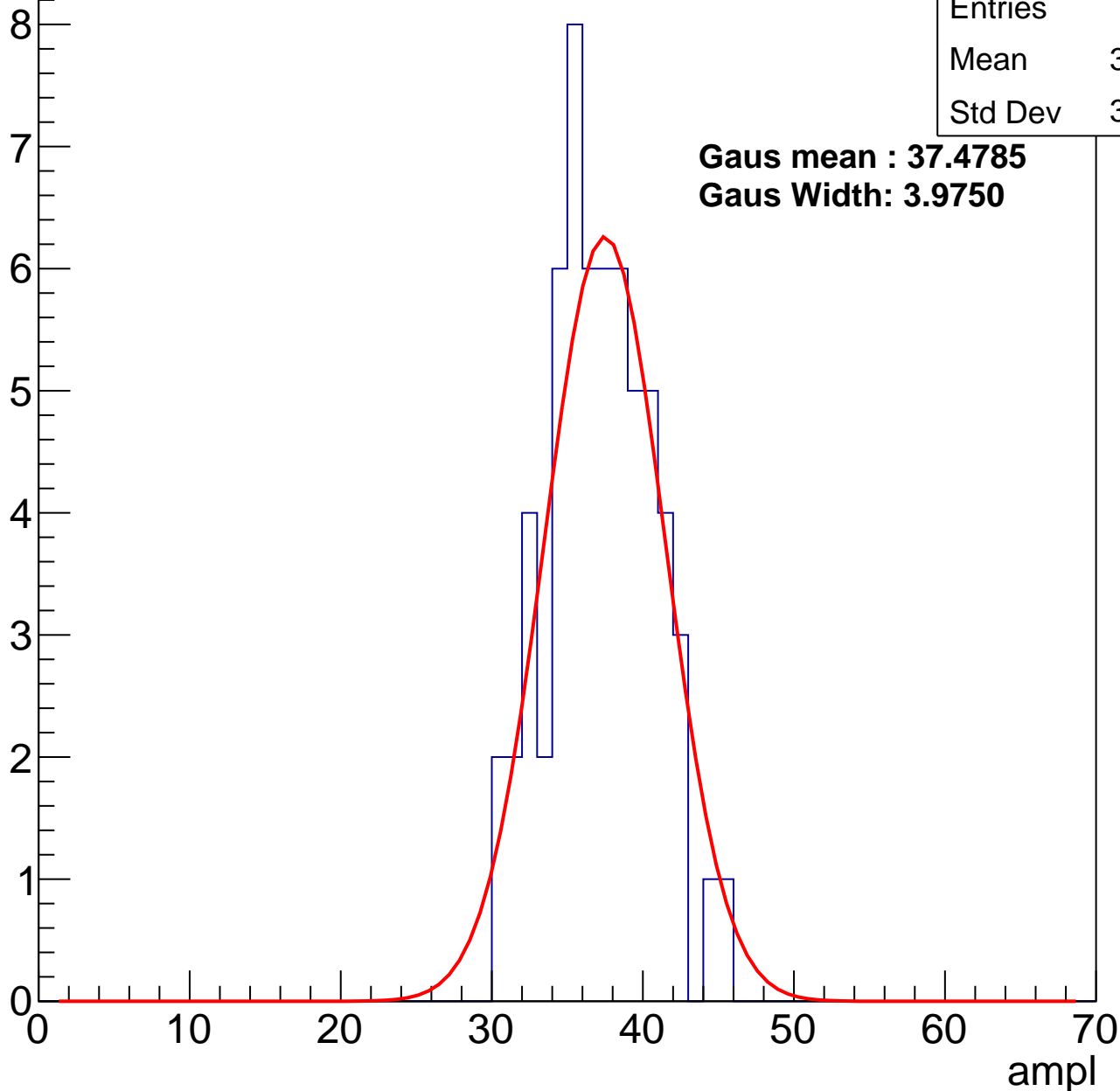
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	36.72
Std Dev	3.417

**Gaus mean : 37.4785**

**Gaus Width: 3.9750**



# B1L101S, U11-ch0, adc2

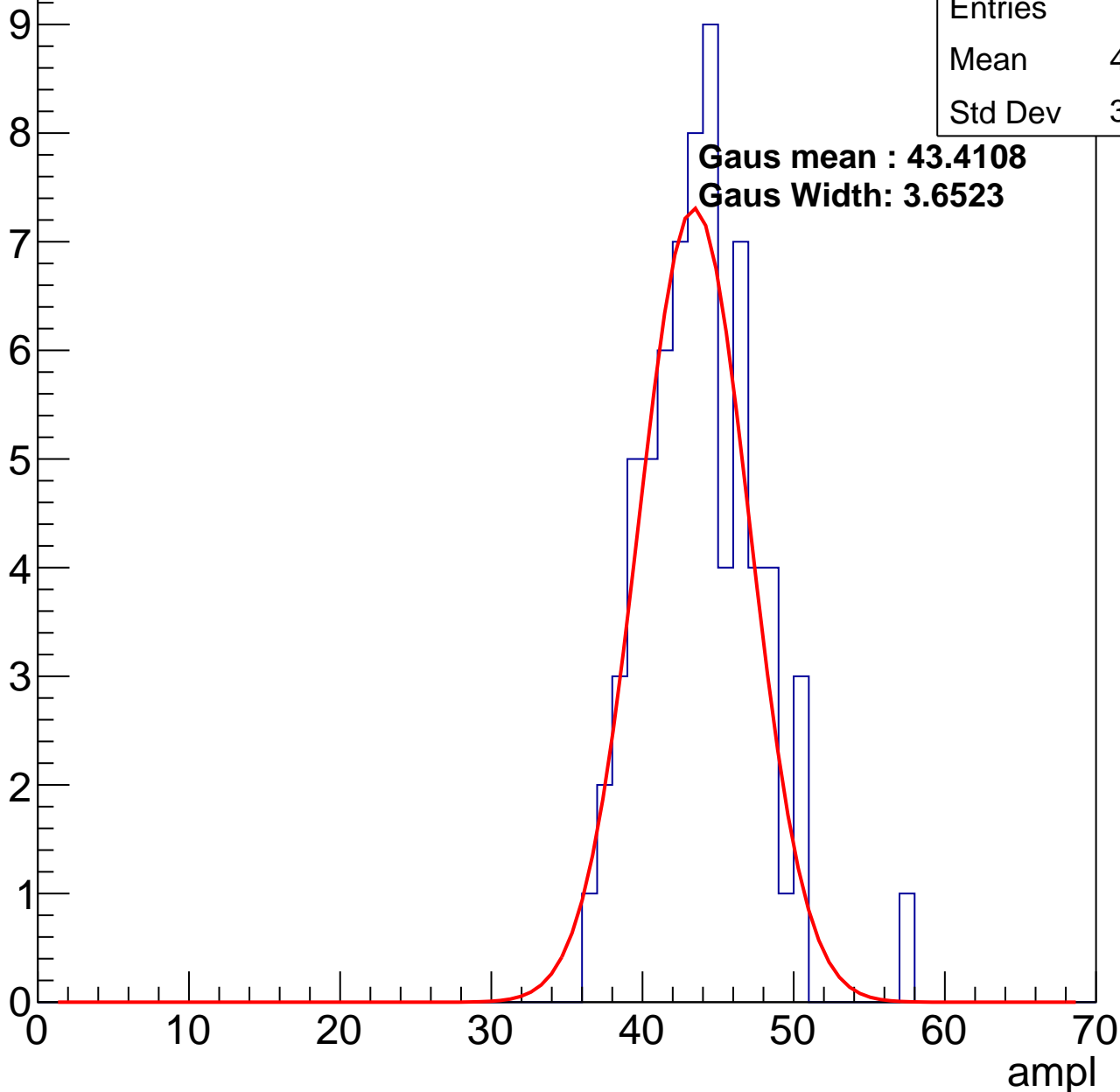
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	43.39
Std Dev	3.727

**Gaus mean : 43.4108**

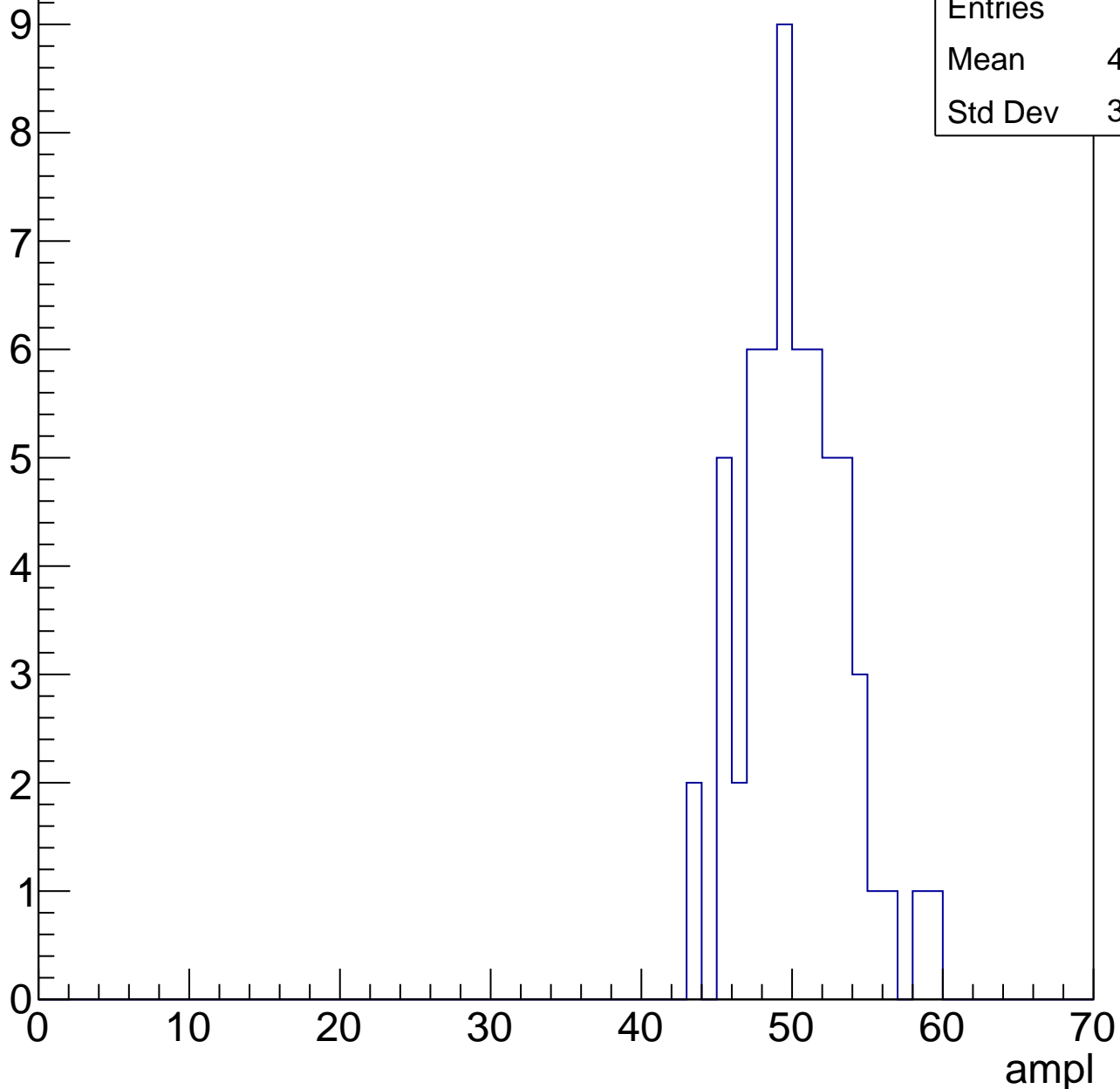
**Gaus Width: 3.6523**



# B1L101S, U11-ch0, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



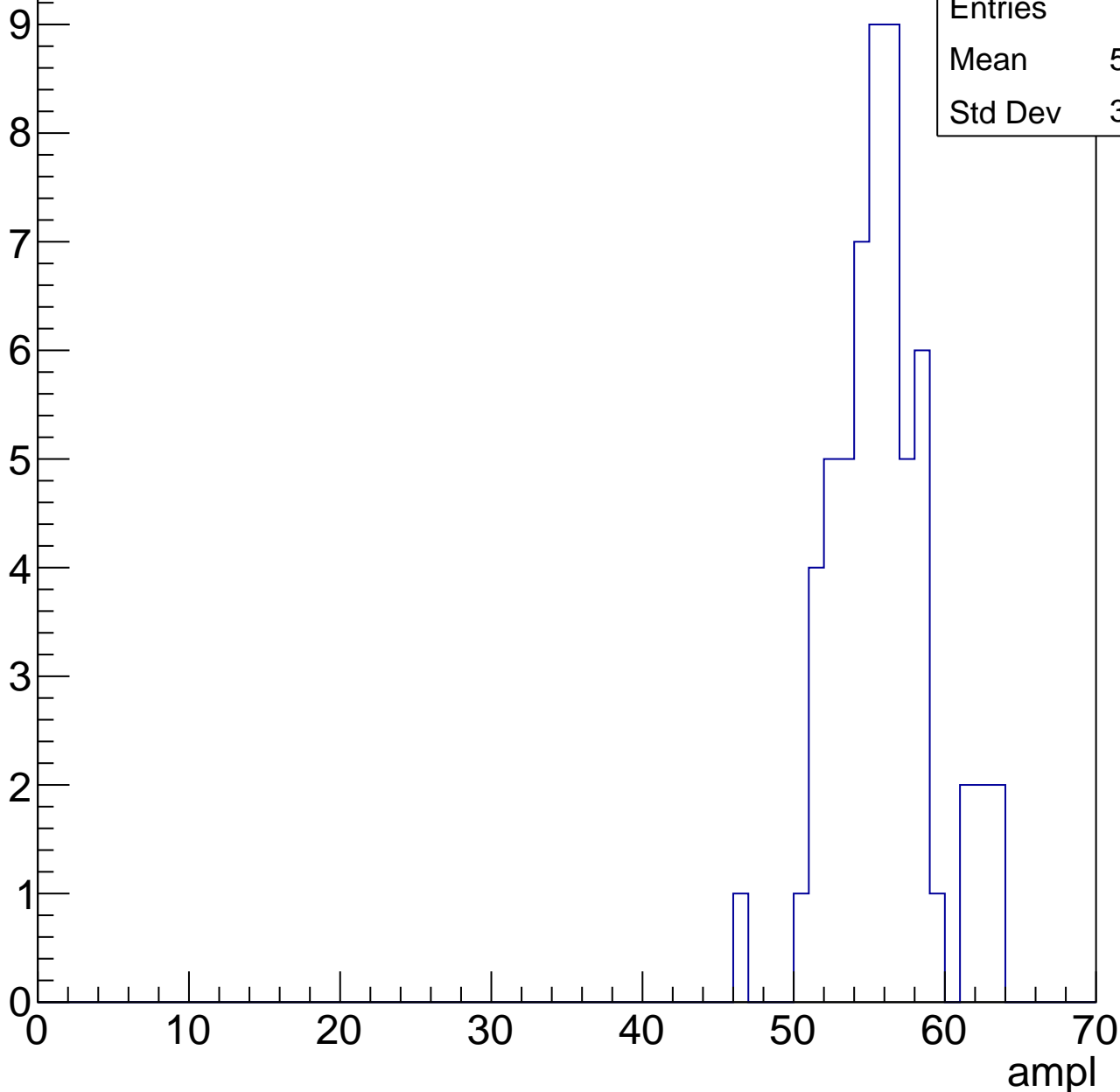
Entries	59
Mean	49.75
Std Dev	3.353

# B1L101S, U11-ch0, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	55.36
Std Dev	3.272



# B1L101S, U11-ch0, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

70

ampl

Entries	44
Mean	60.36
Std Dev	1.72

0

2

4

6

8

10

# B1L101S, U11-ch0, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

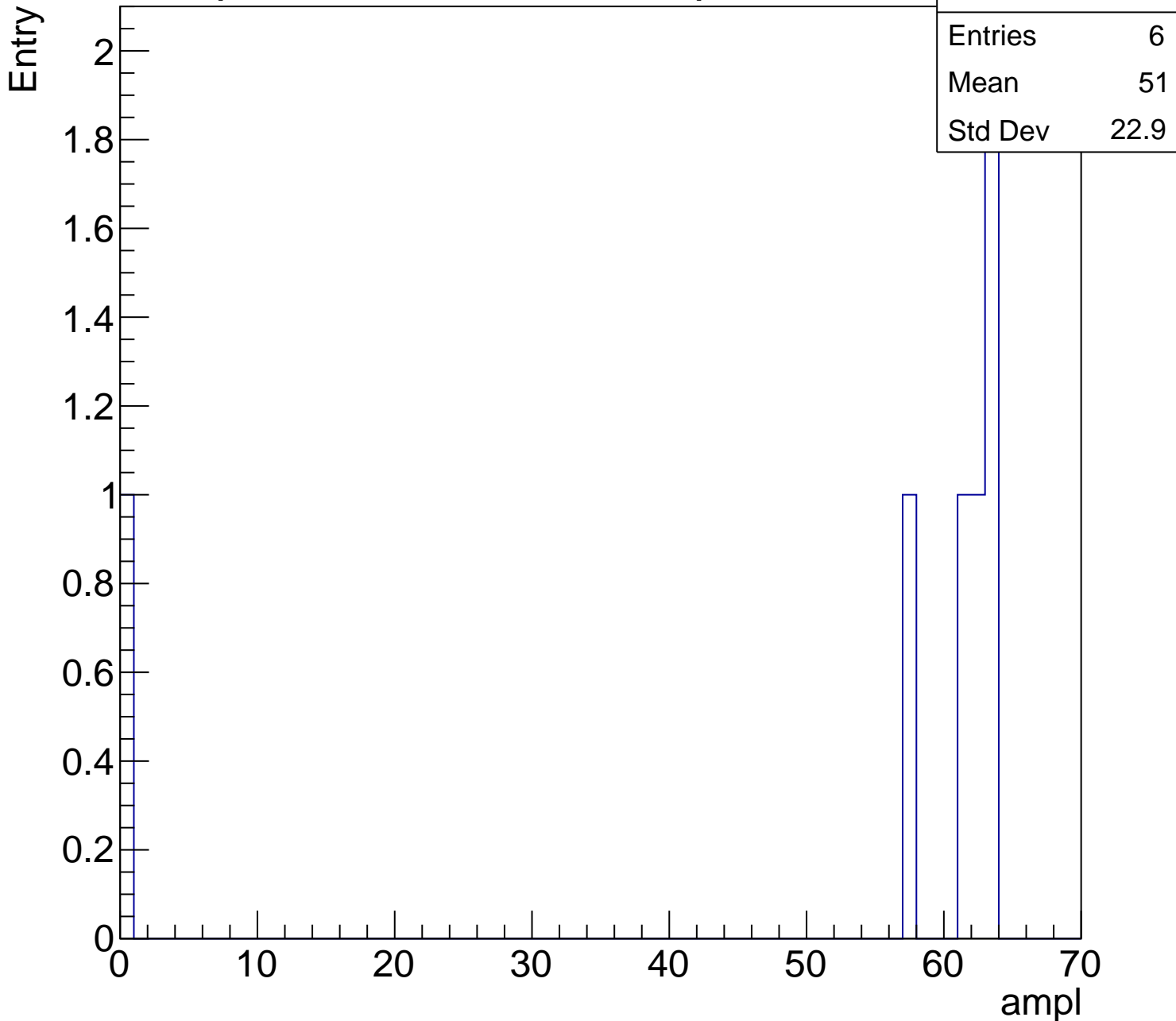
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	51
Std Dev	22.9

ampl

0 10 20 30 40 50 60 70





# B1L101S, U11-ch0, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U11-ch1, adc0

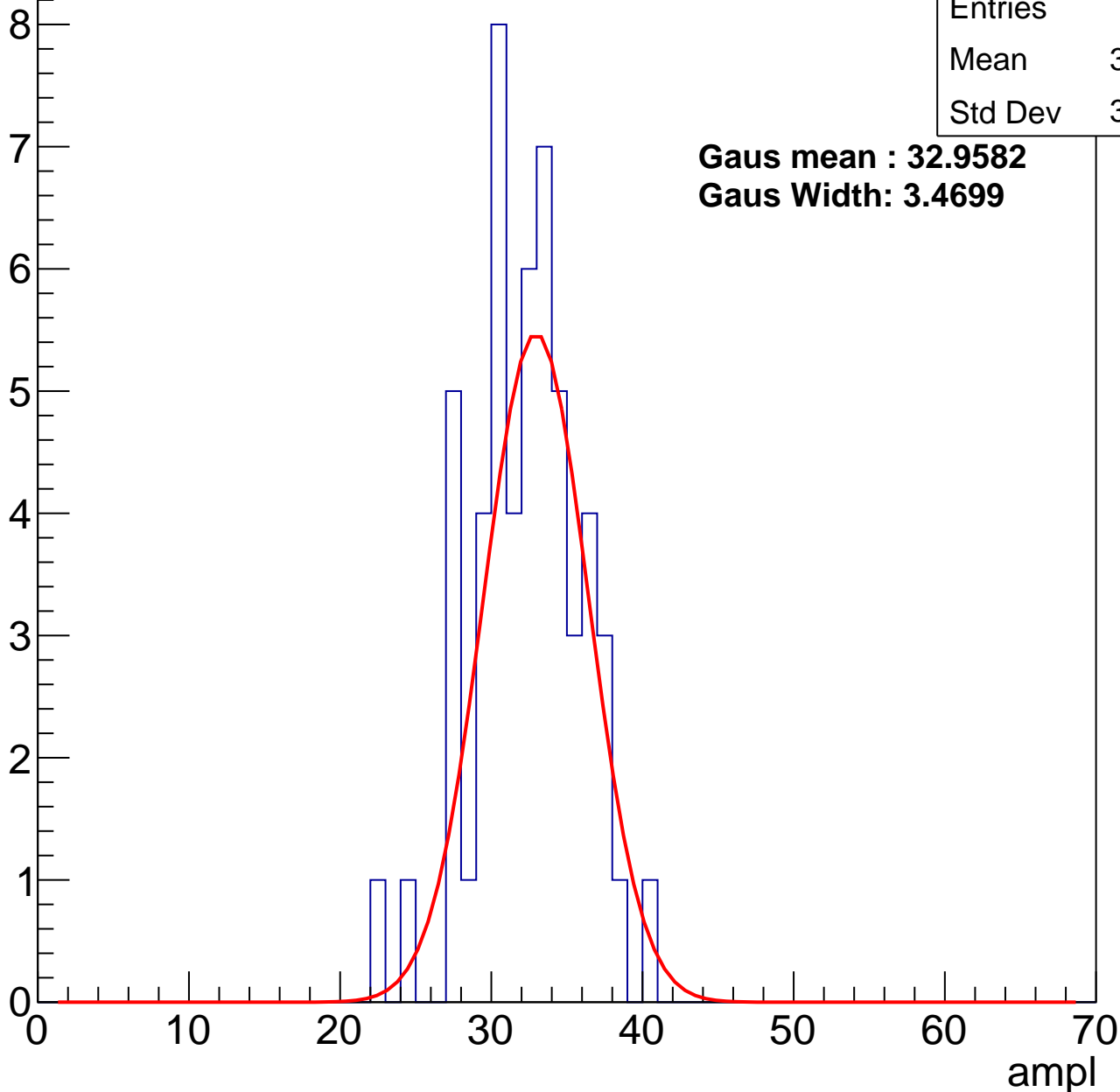
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	31.85
Std Dev	3.519

**Gaus mean : 32.9582**

**Gaus Width: 3.4699**



# B1L101S, U11-ch1, adc1

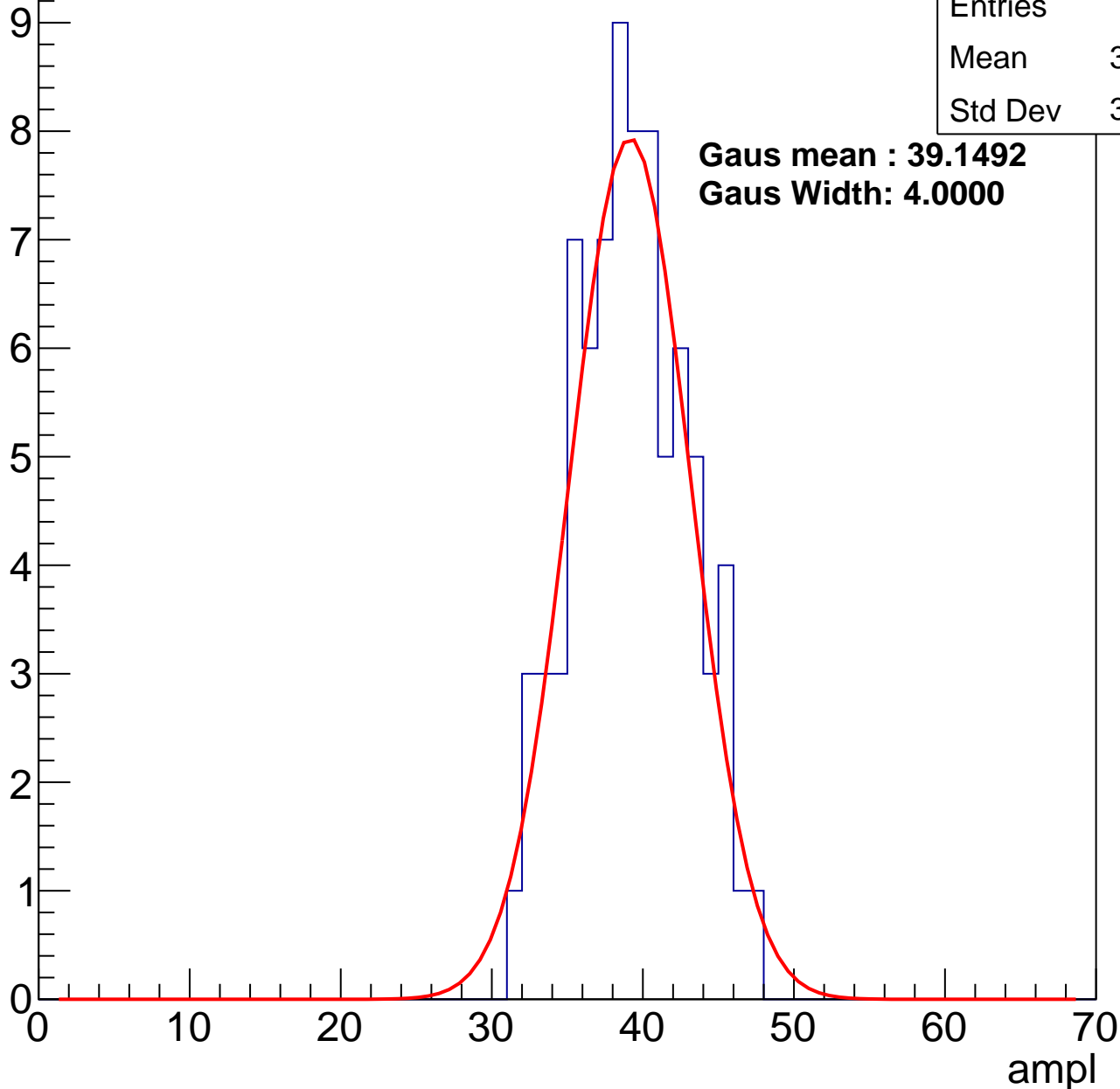
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	80
Mean	38.74
Std Dev	3.684

**Gaus mean : 39.1492**

**Gaus Width: 4.0000**



# B1L101S, U11-ch1, adc2

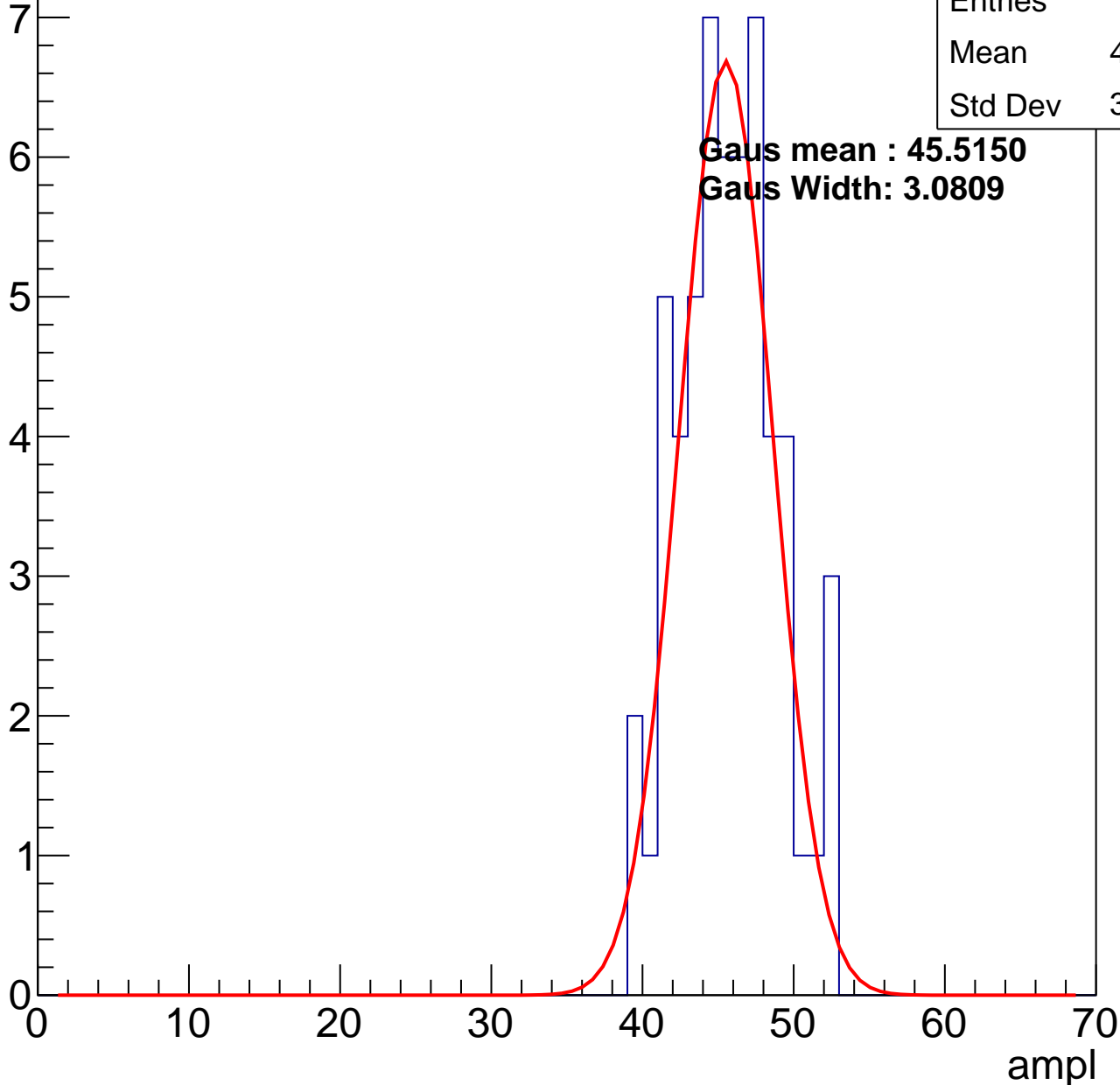
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	45.25
Std Dev	3.214

**Gaus mean : 45.5150**

**Gaus Width: 3.0809**

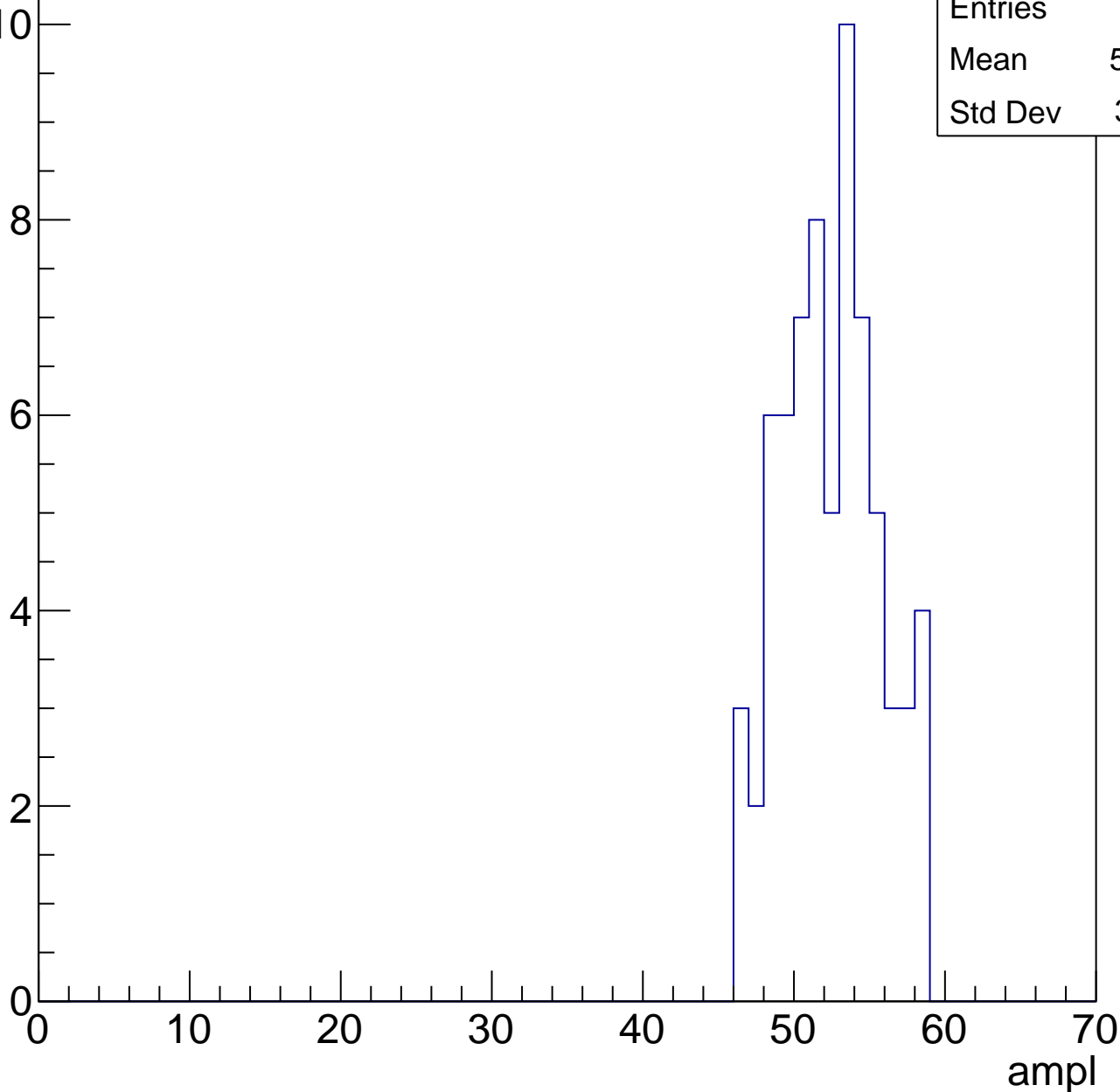


# B1L101S, U11-ch1, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	51.97
Std Dev	3.171

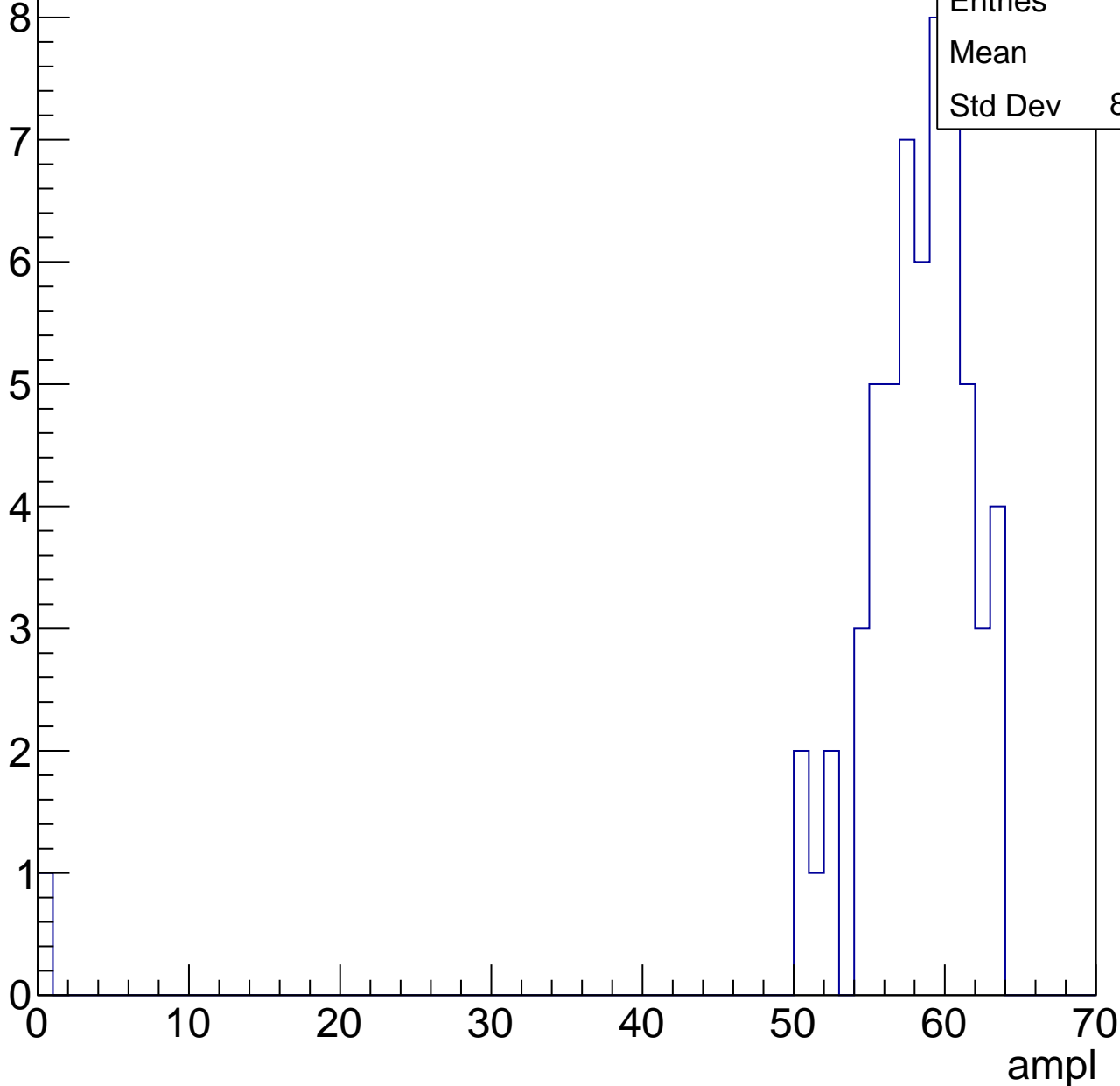


# B1L101S, U11-ch1, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	56.9
Std Dev	8.055

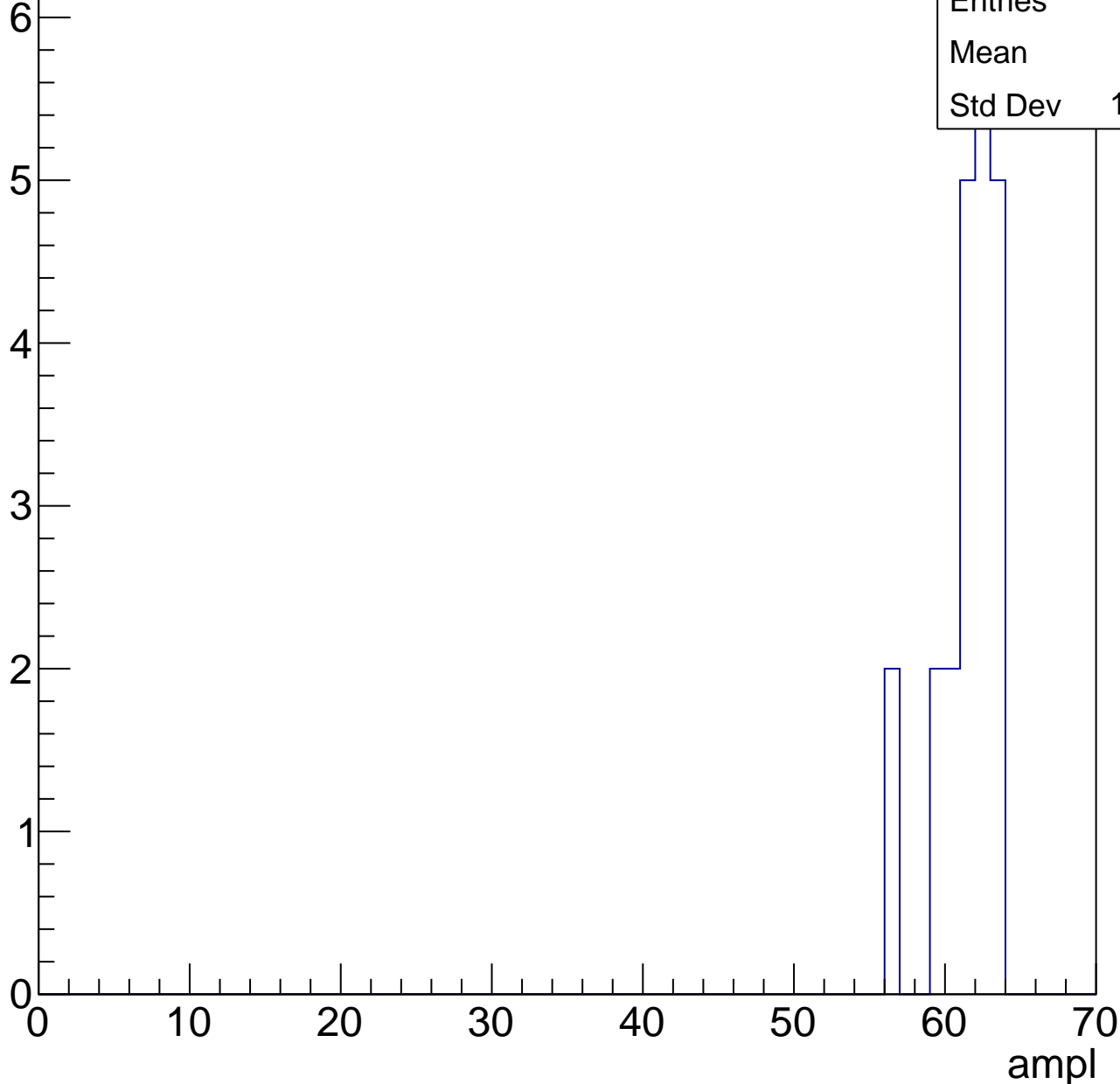


# B1L101S, U11-ch1, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	22
Mean	61
Std Dev	1.977



# B1L101S, U11-ch1, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch1, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U11-ch2, adc0

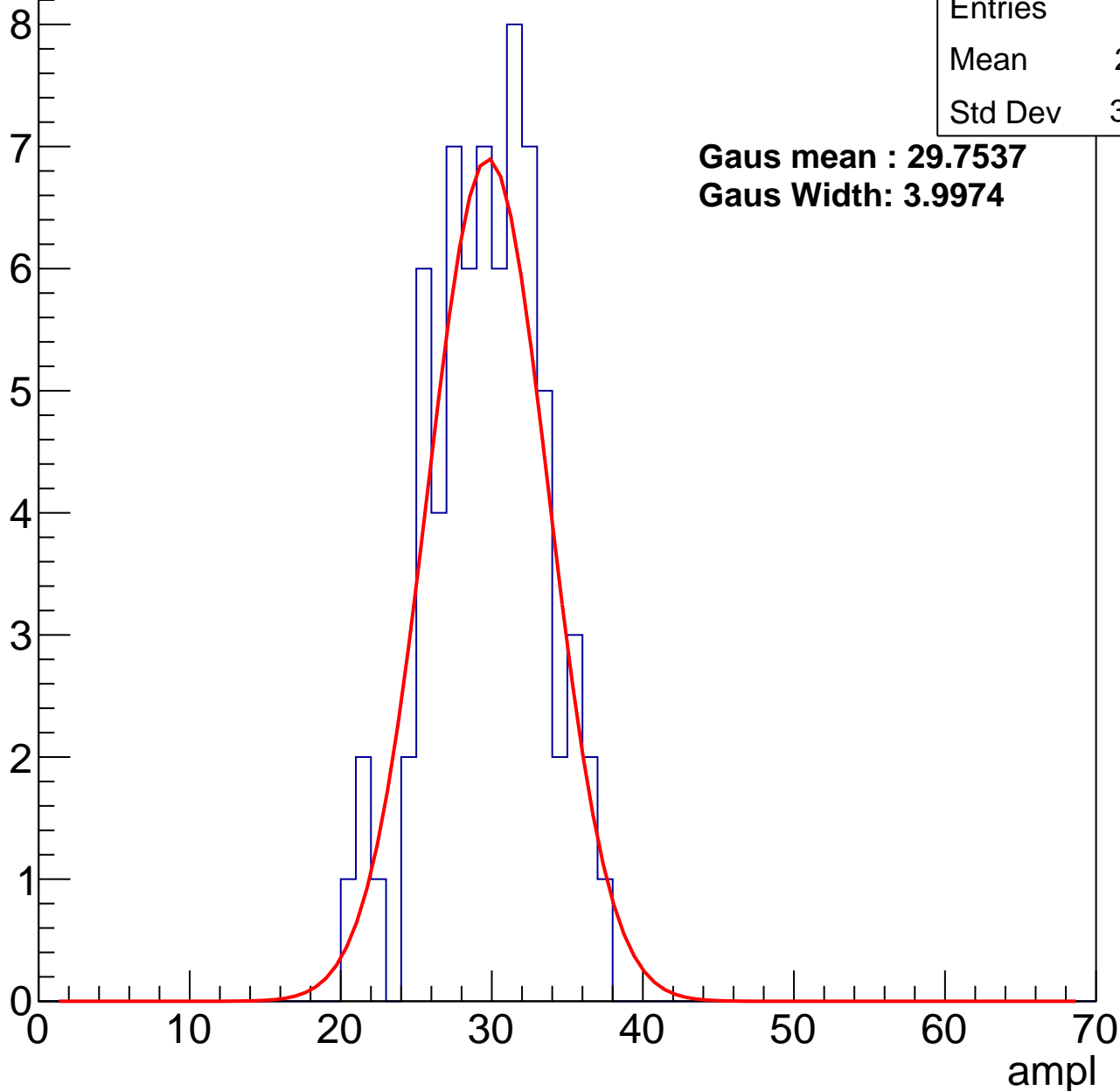
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	29.21
Std Dev	3.726

**Gaus mean : 29.7537**

**Gaus Width: 3.9974**



# B1L101S, U11-ch2, adc1

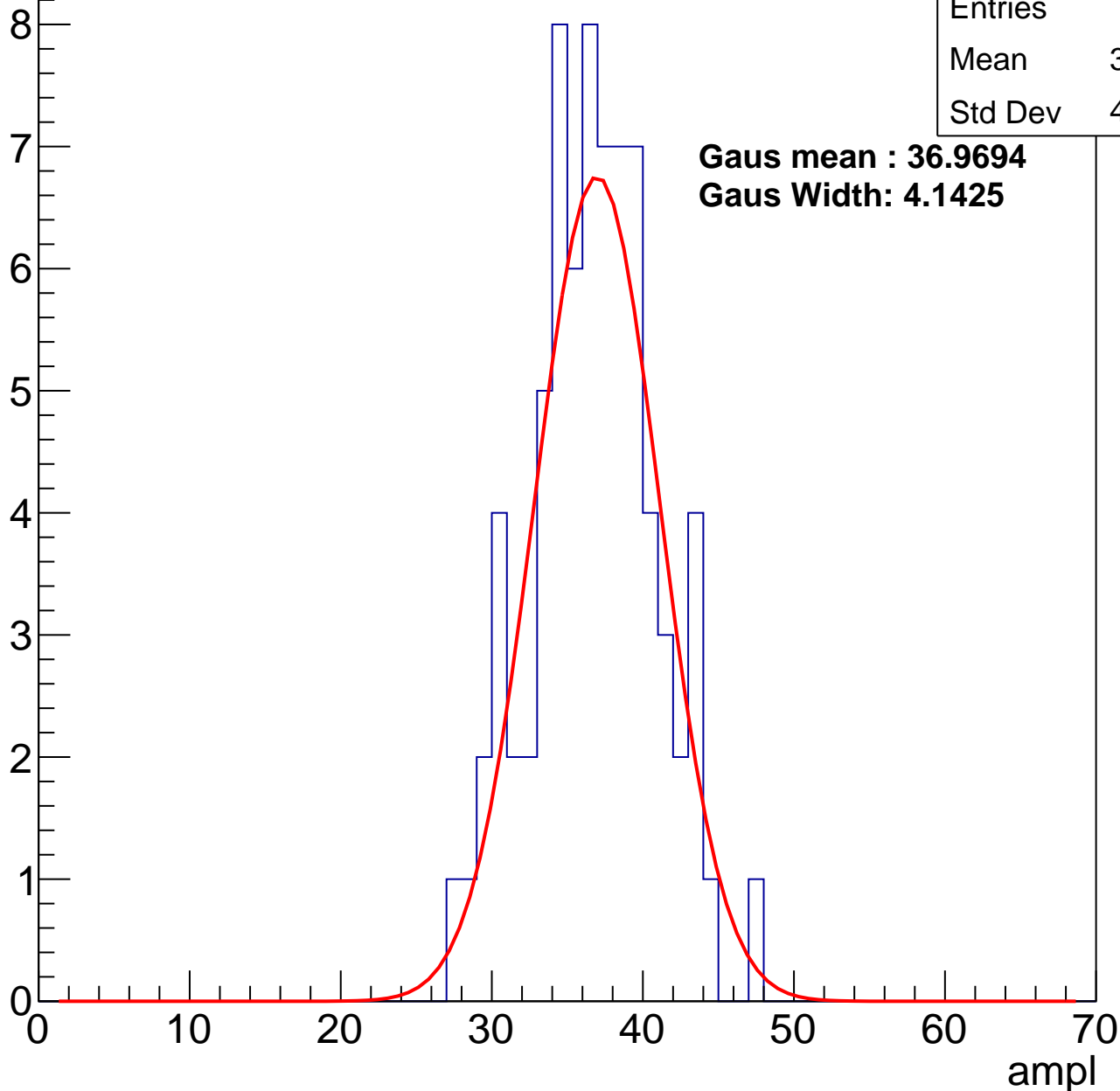
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	36.29
Std Dev	4.059

**Gaus mean : 36.9694**

**Gaus Width: 4.1425**



# B1L101S, U11-ch2, adc2

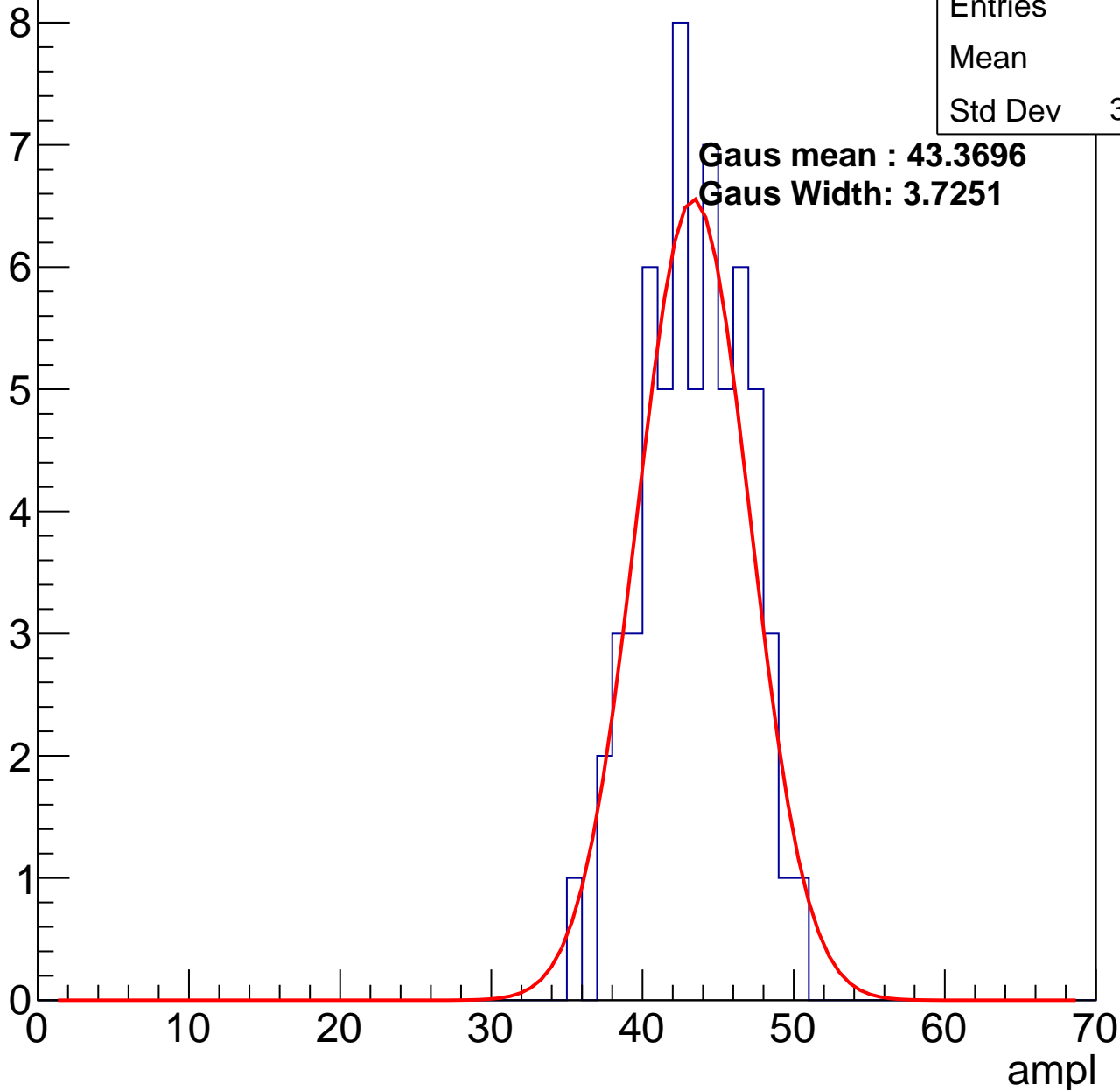
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	43
Std Dev	3.294

**Gaus mean : 43.3696**

**Gaus Width: 3.7251**

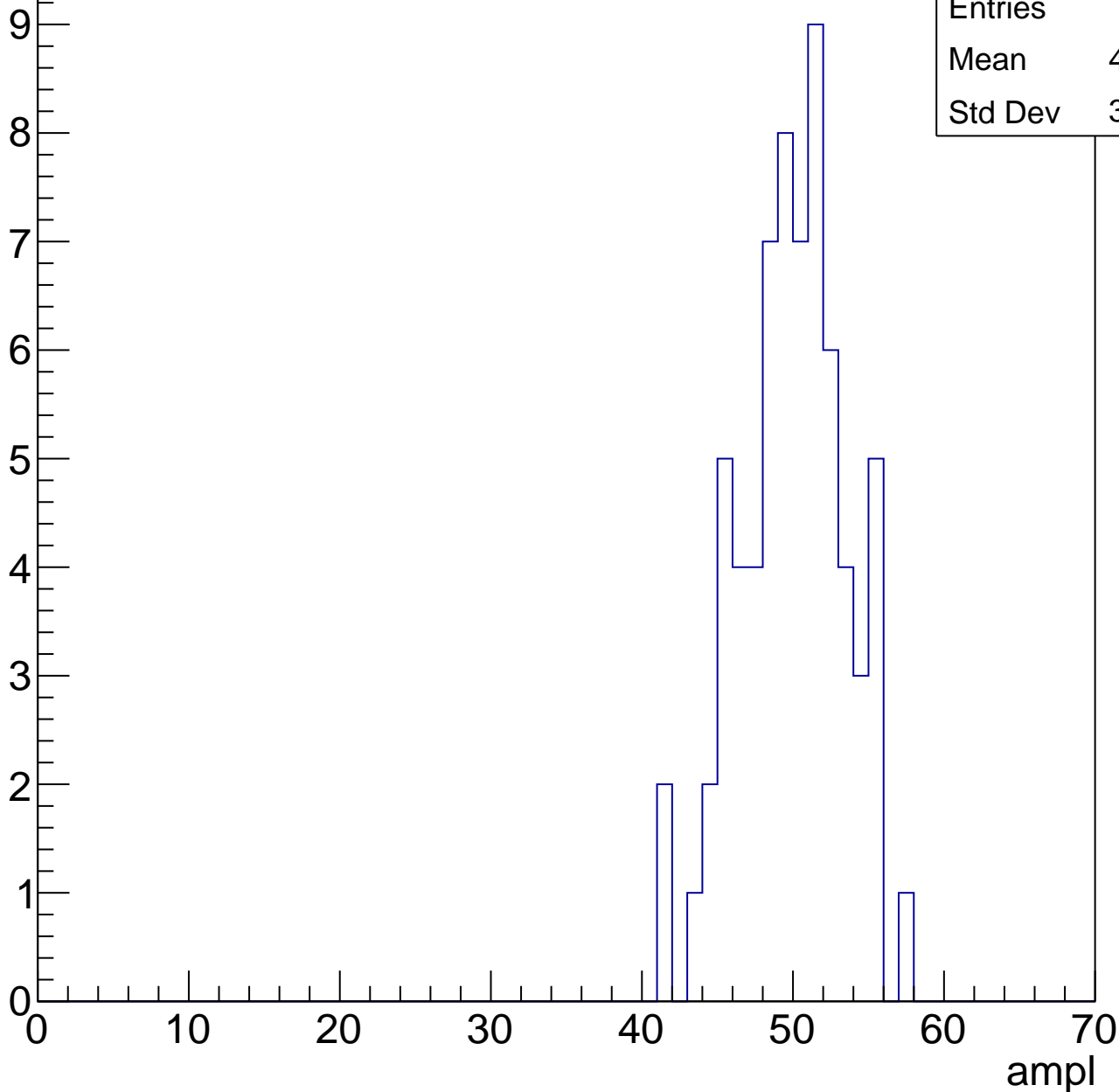


# B1L101S, U11-ch2, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	49.49
Std Dev	3.466



# B1L101S, U11-ch2, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

7

6

5

4

3

2

1

0

Entries 49

Mean 55.57

Std Dev 2.928

ampl

0

10

20

30

40

50

60

70

0

1

2

3

4

5

6

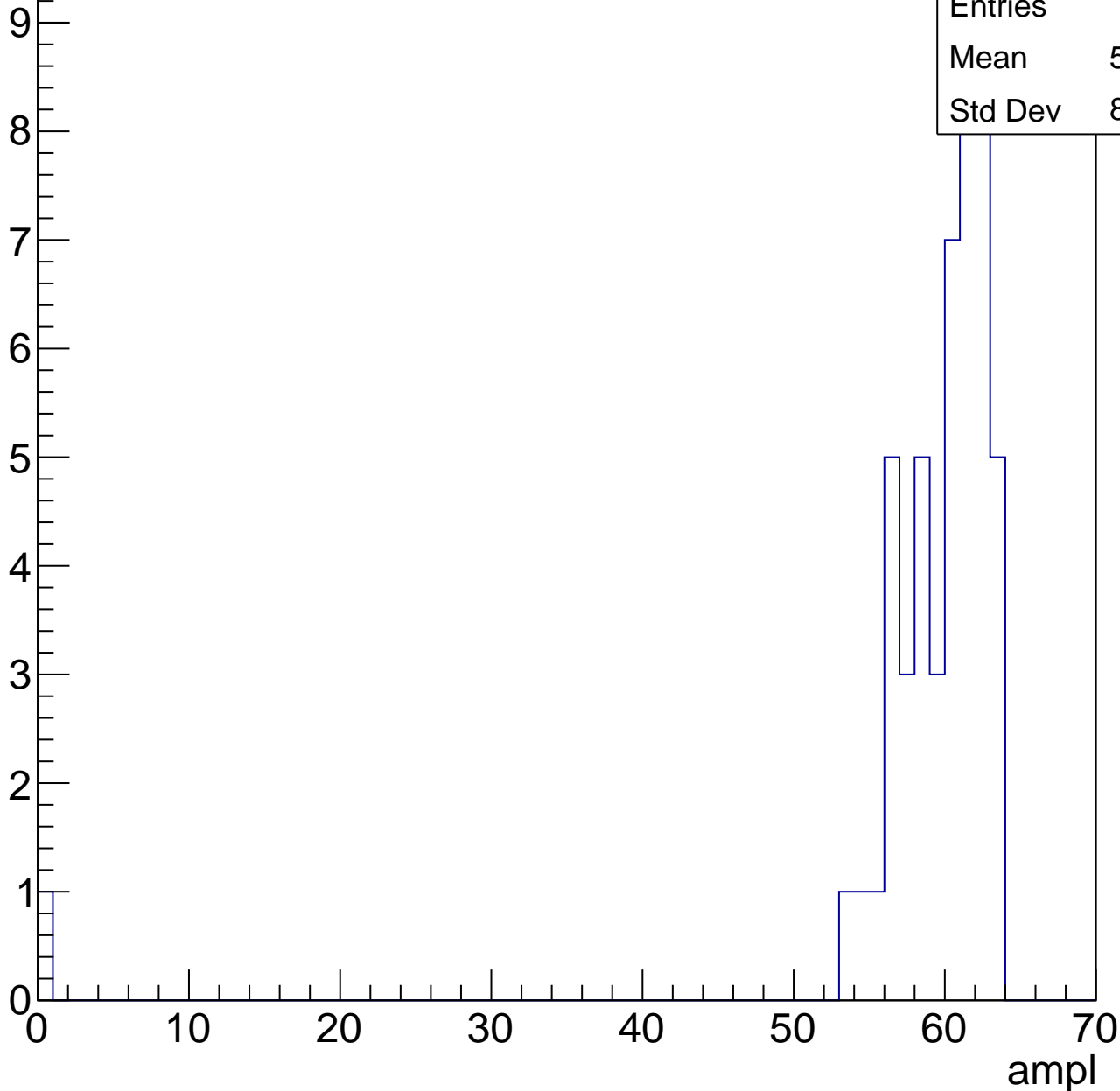
7

# B1L101S, U11-ch2, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	58.44
Std Dev	8.727

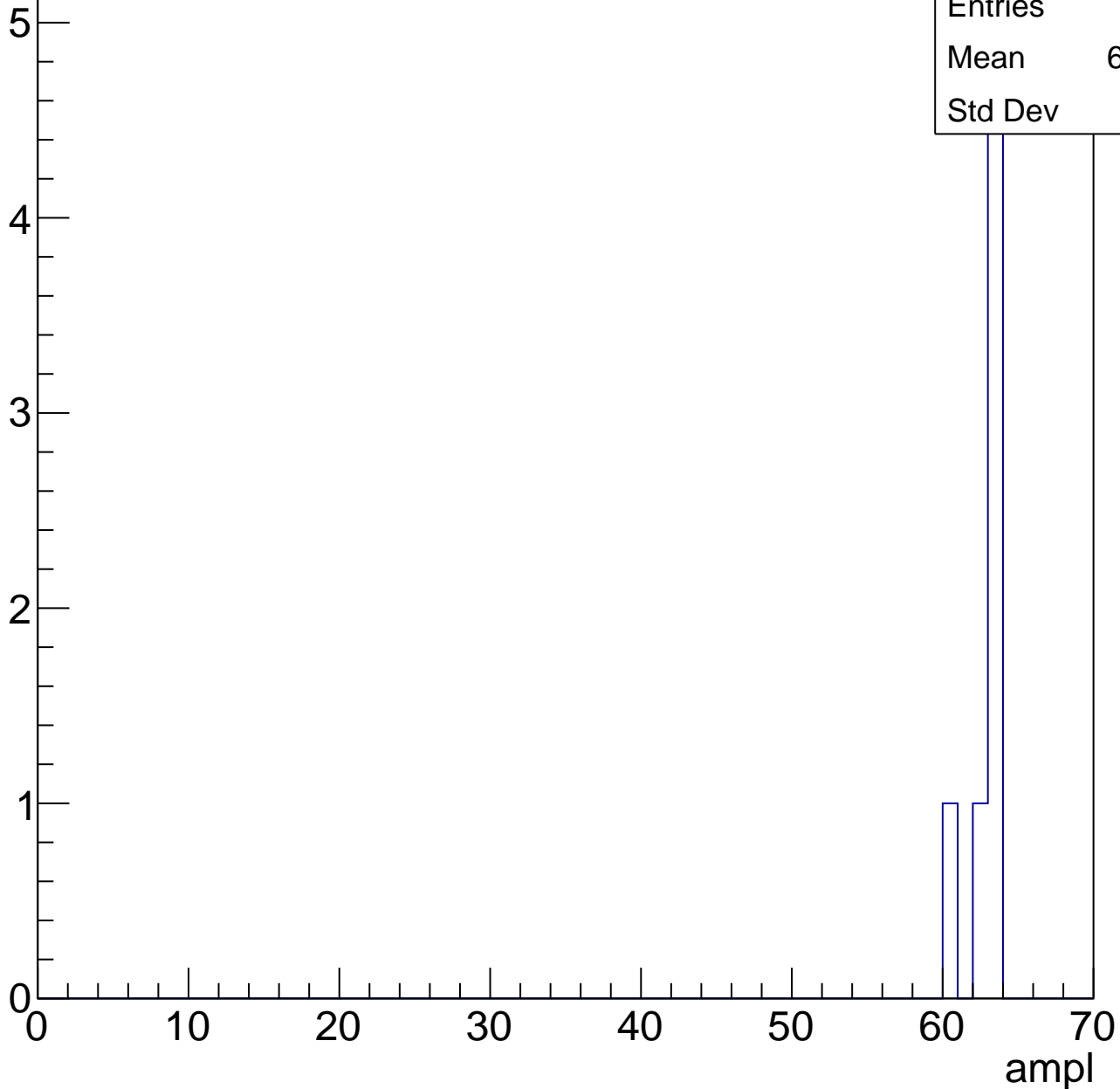


# B1L101S, U11-ch2, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	7
Mean	62.43
Std Dev	1.05





# B1L101S, U11-ch2, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U11-ch3, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	73
Mean	30.49
Std Dev	3.124

**Gaus mean : 31.2190**

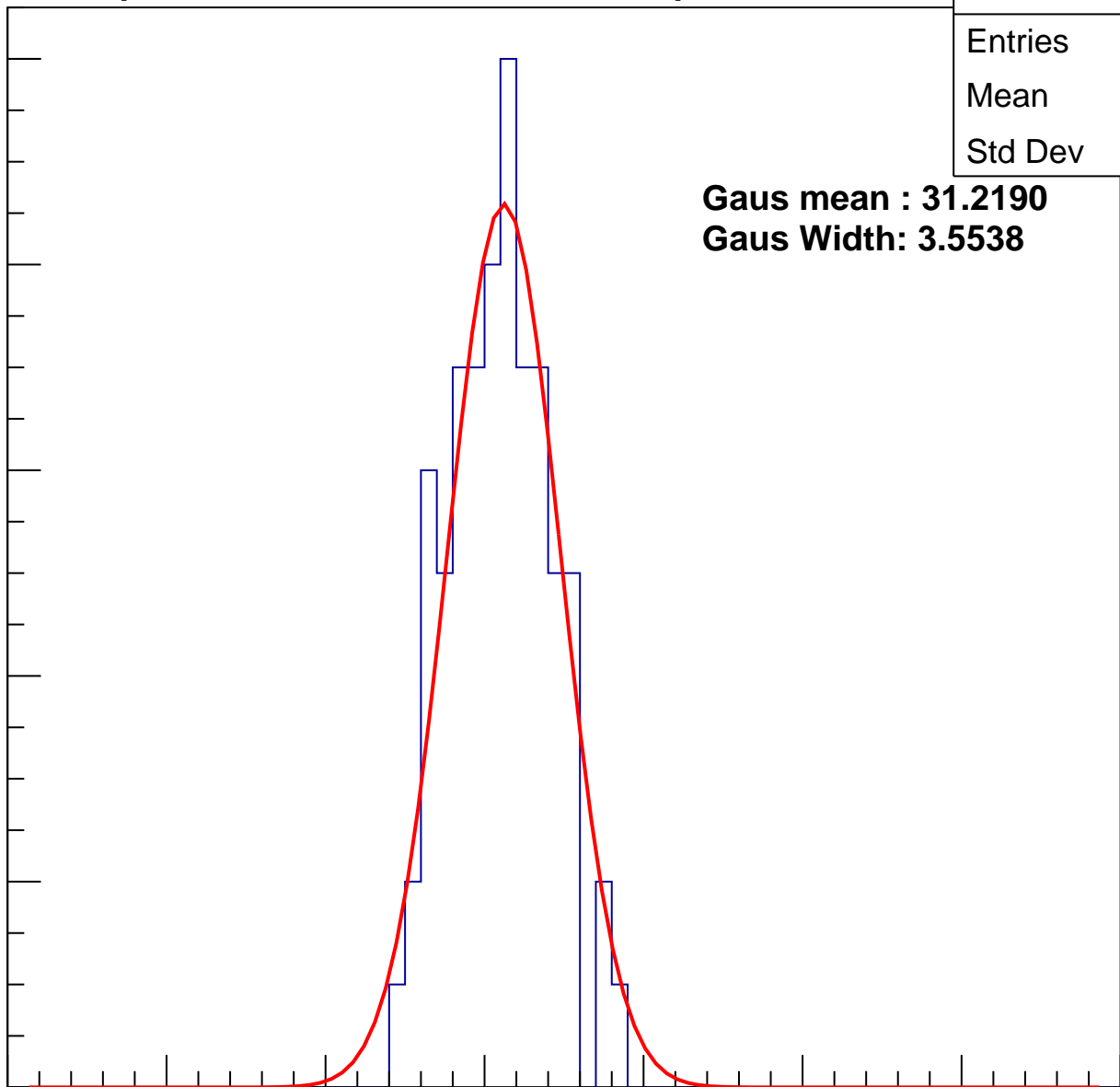
**Gaus Width: 3.5538**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U11-ch3, adc1

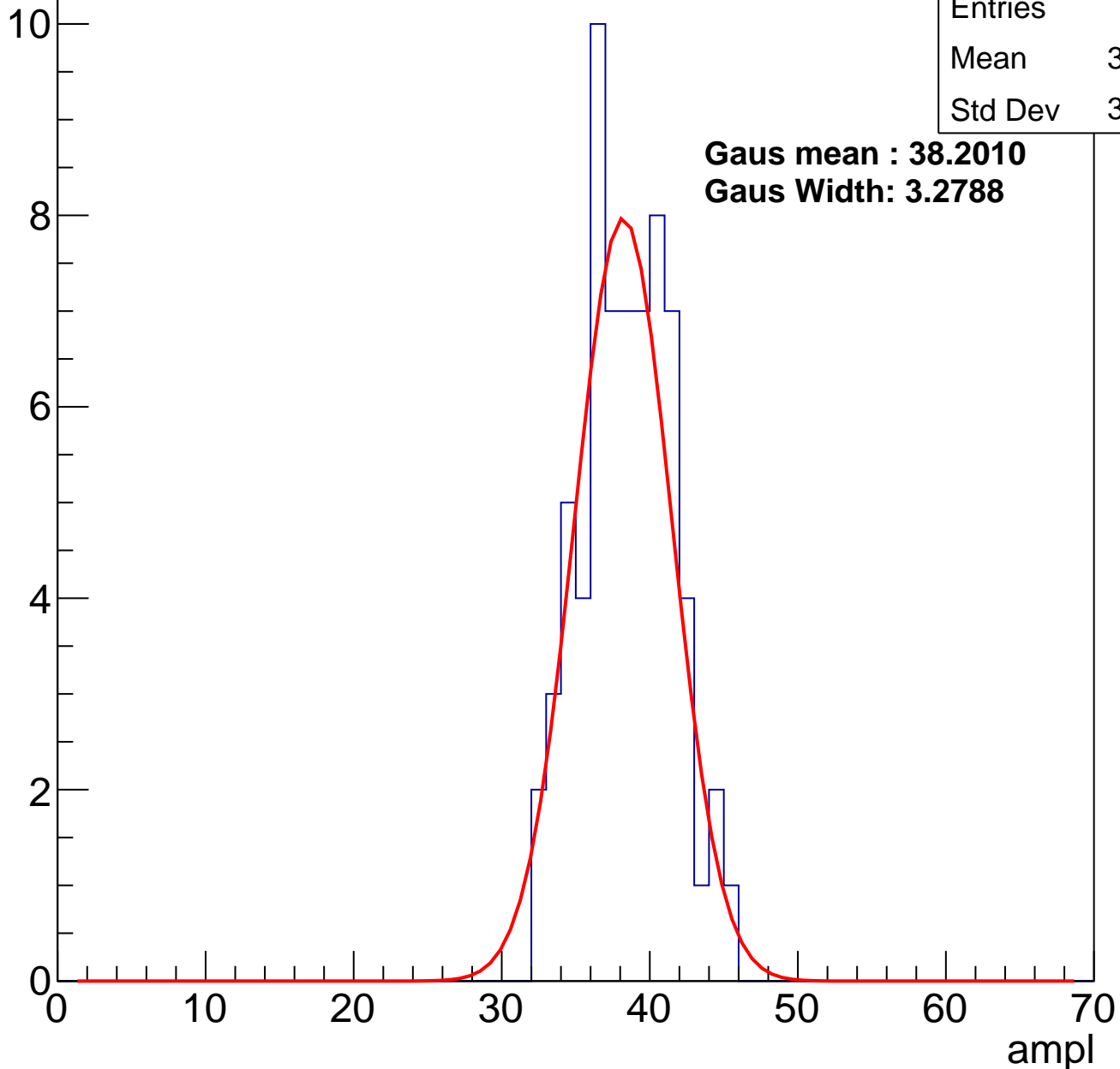
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	68
Mean	37.97
Std Dev	3.024

**Gaus mean : 38.2010**

**Gaus Width: 3.2788**

Entry



# B1L101S, U11-ch3, adc2

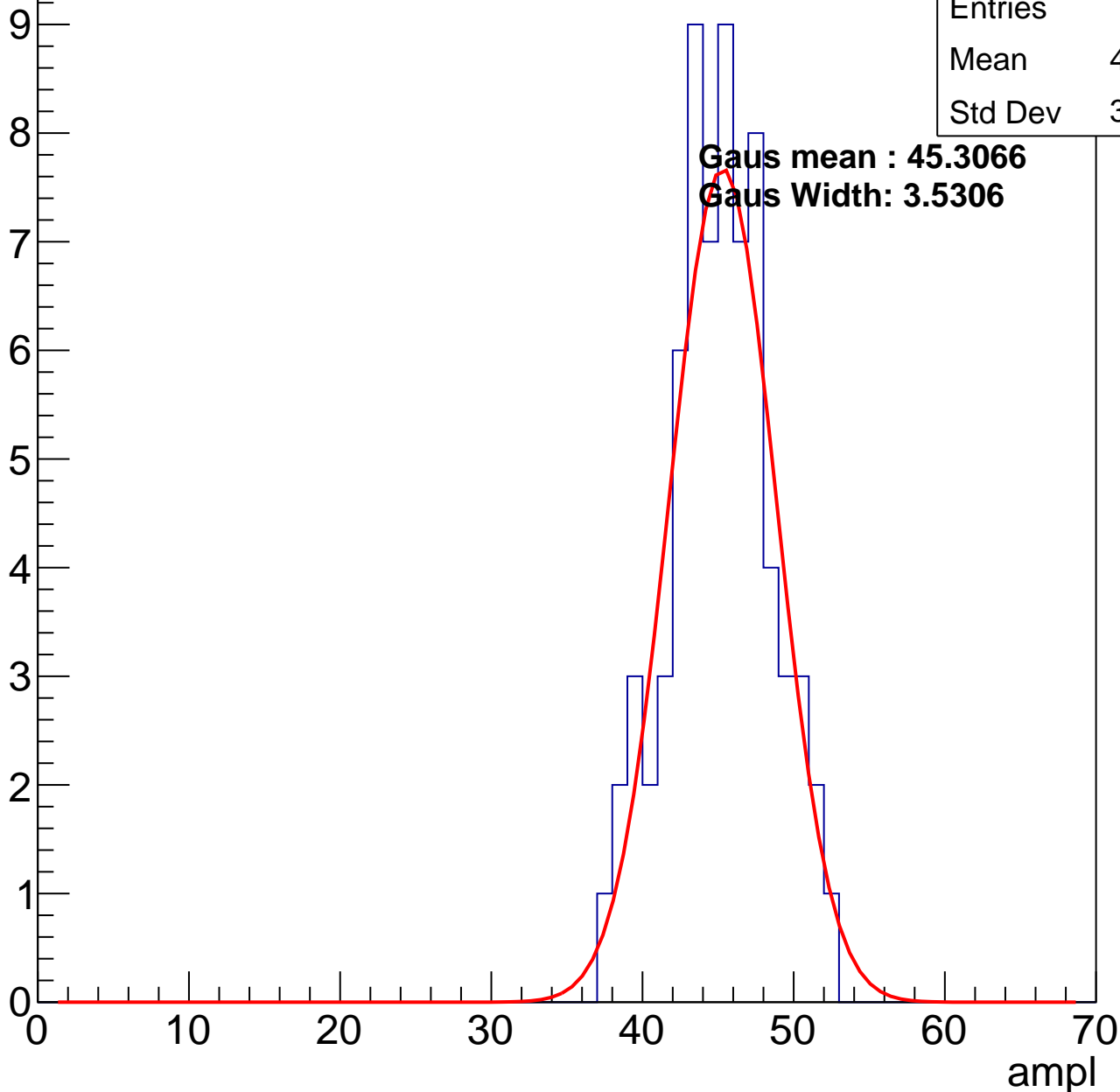
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	44.66
Std Dev	3.329

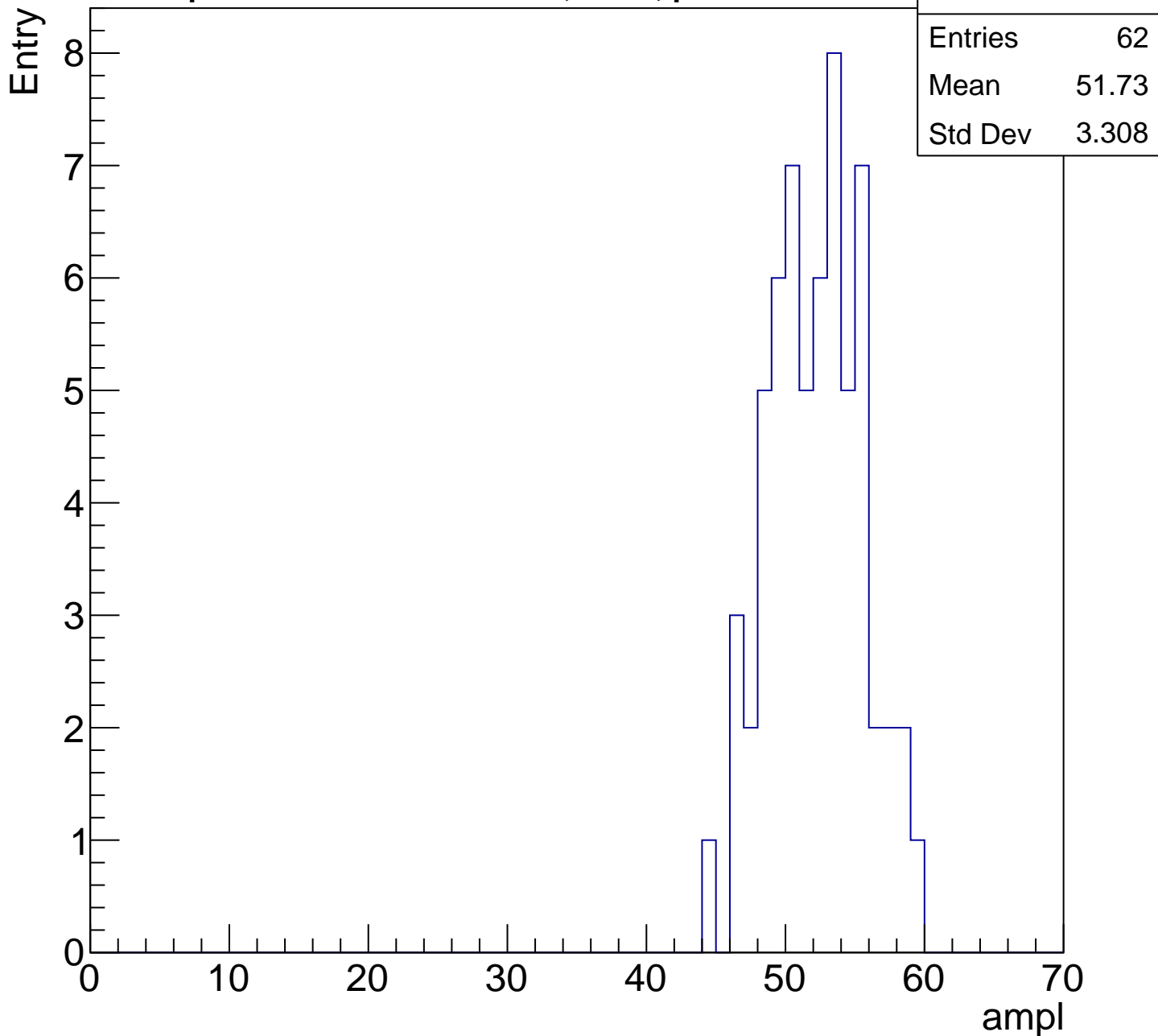
**Gaus mean : 45.3066**

**Gaus Width: 3.5306**



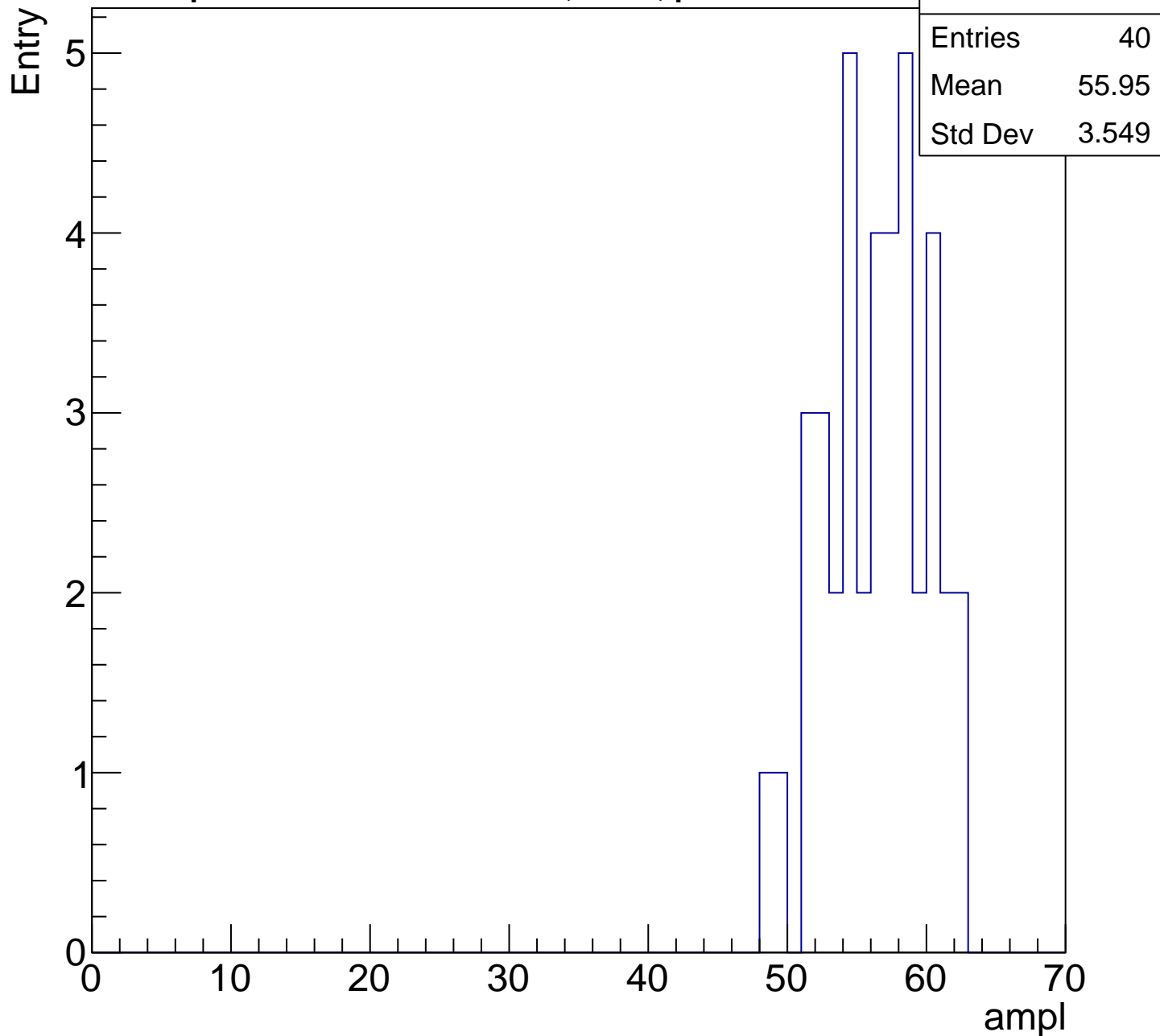
# B1L101S, U11-ch3, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U11-ch3, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

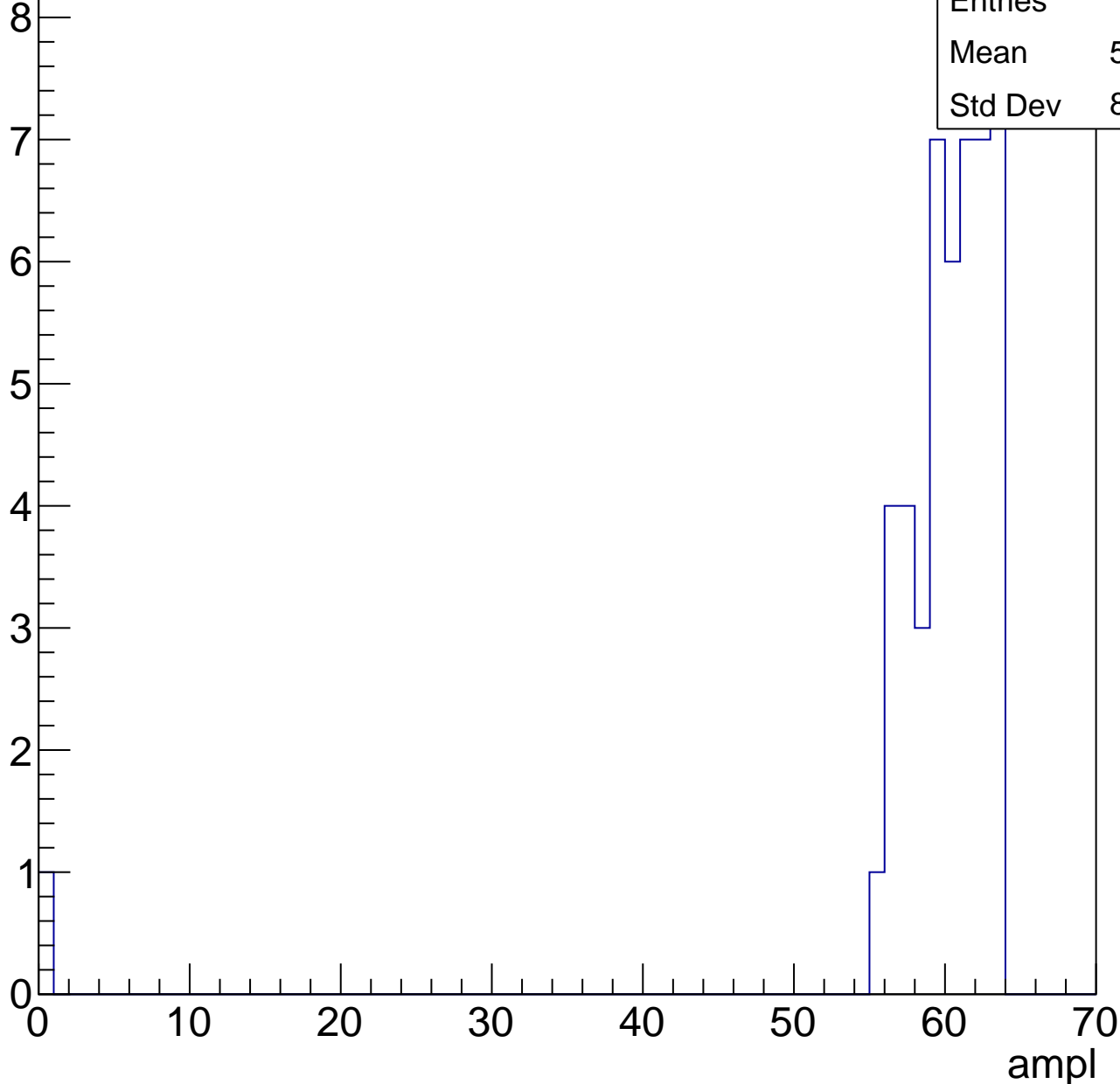


# B1L101S, U11-ch3, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

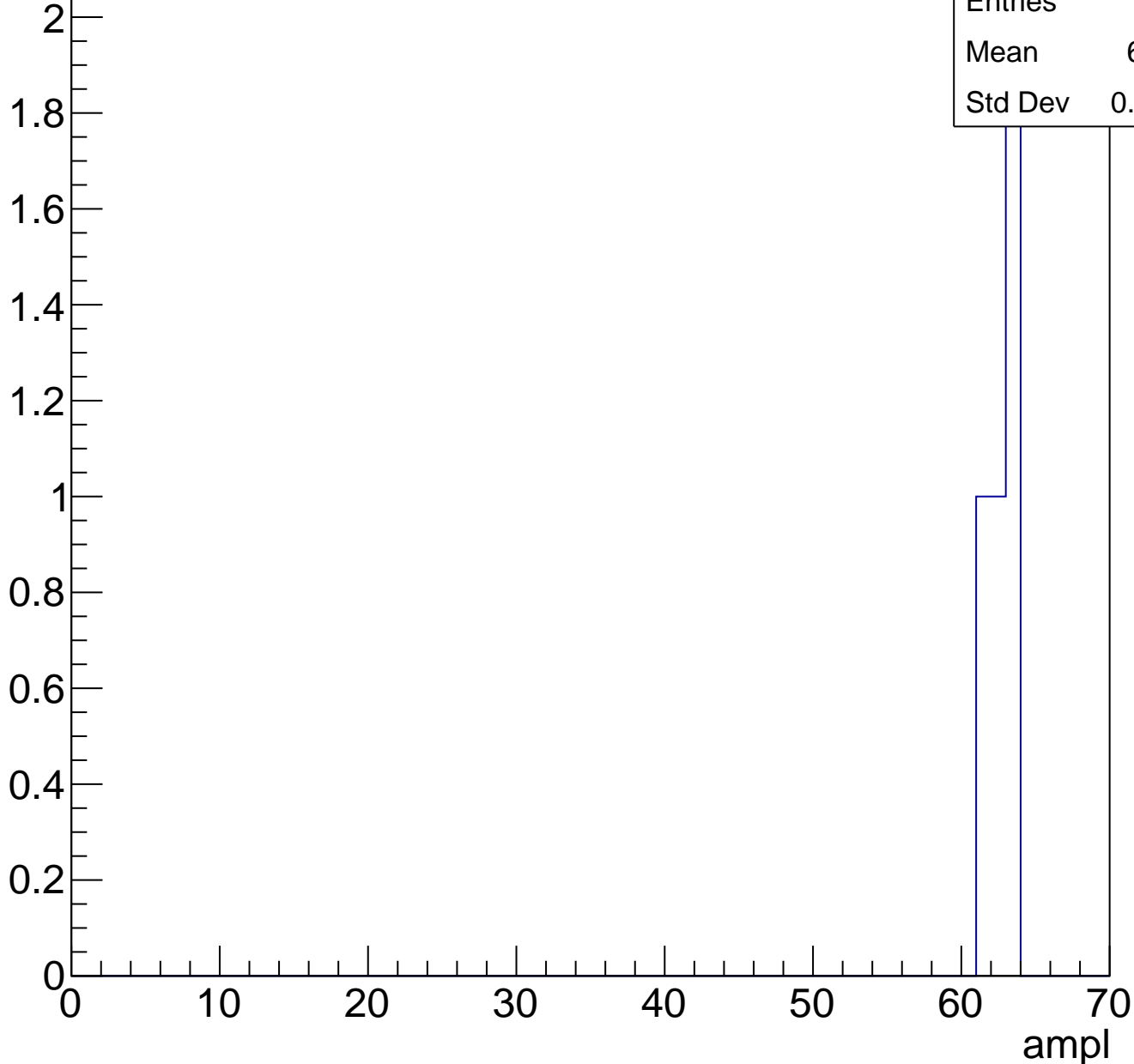
Entries	48
Mean	58.73
Std Dev	8.866



# B1L101S, U11-ch3, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch3, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	24
Std Dev	0

ampl

# B1L101S, U11-ch4, adc0

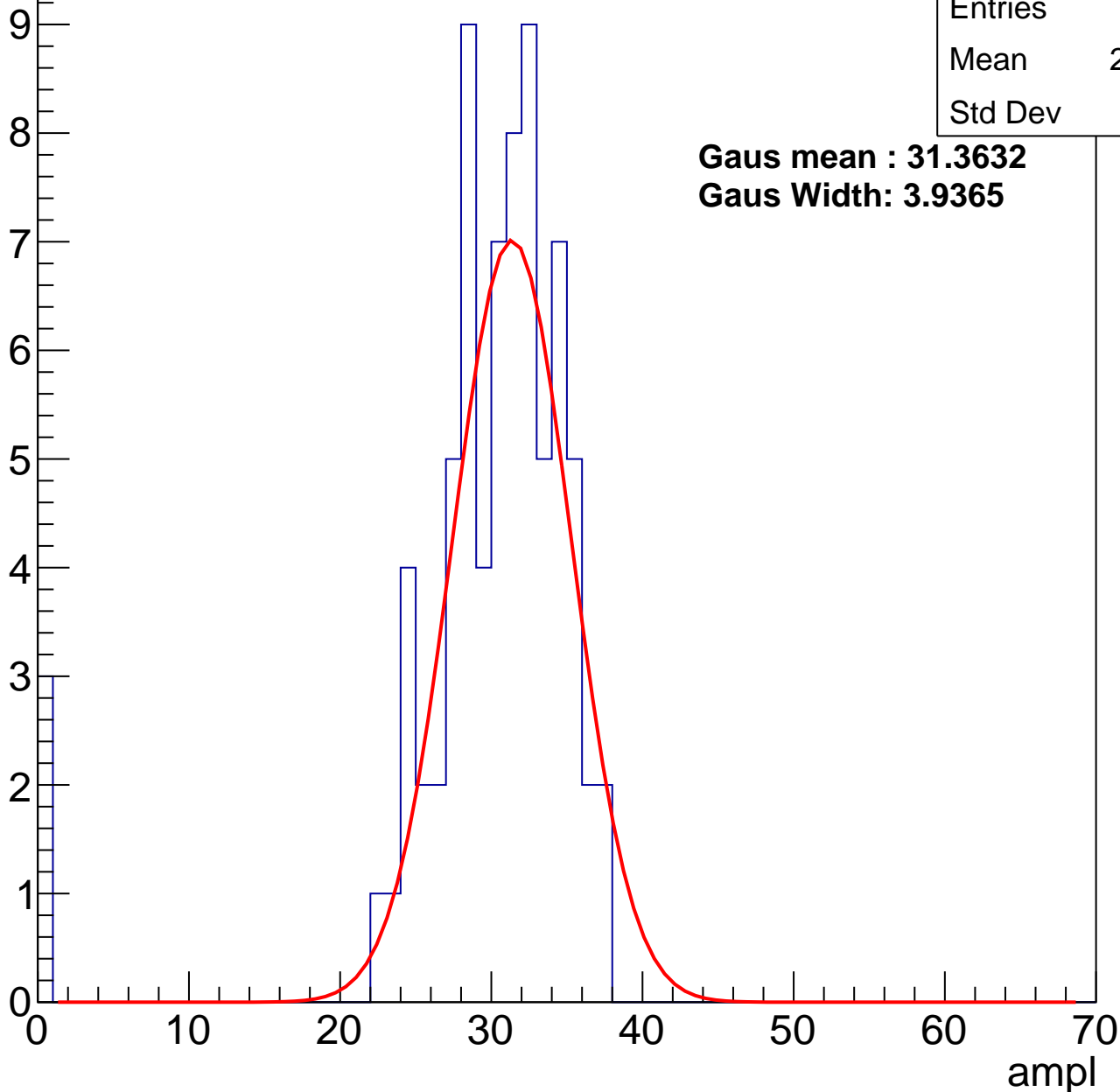
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	29.16
Std Dev	6.85

**Gaus mean : 31.3632**

**Gaus Width: 3.9365**



# B1L101S, U11-ch4, adc1

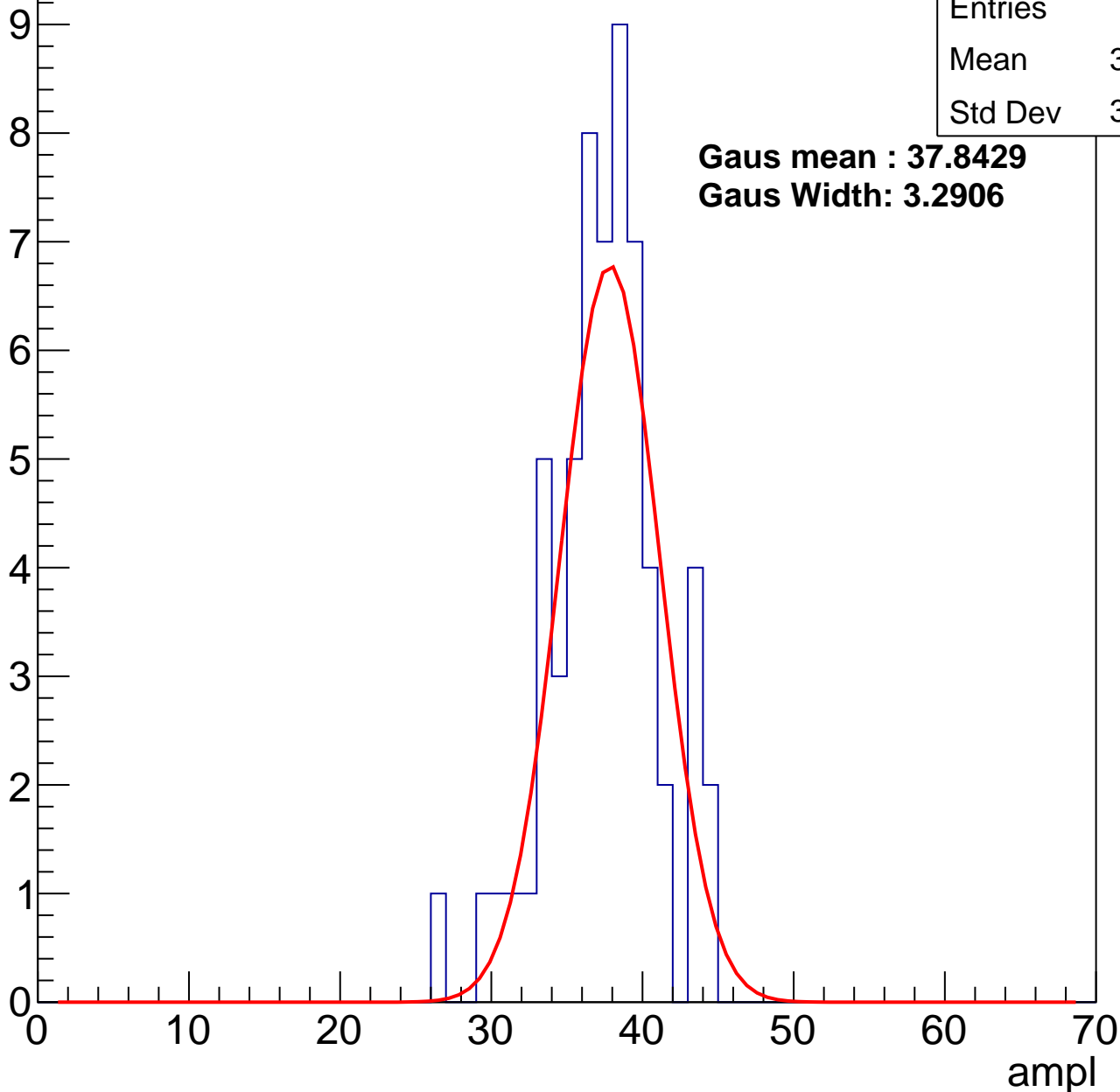
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	36.95
Std Dev	3.569

**Gaus mean : 37.8429**

**Gaus Width: 3.2906**



# B1L101S, U11-ch4, adc2

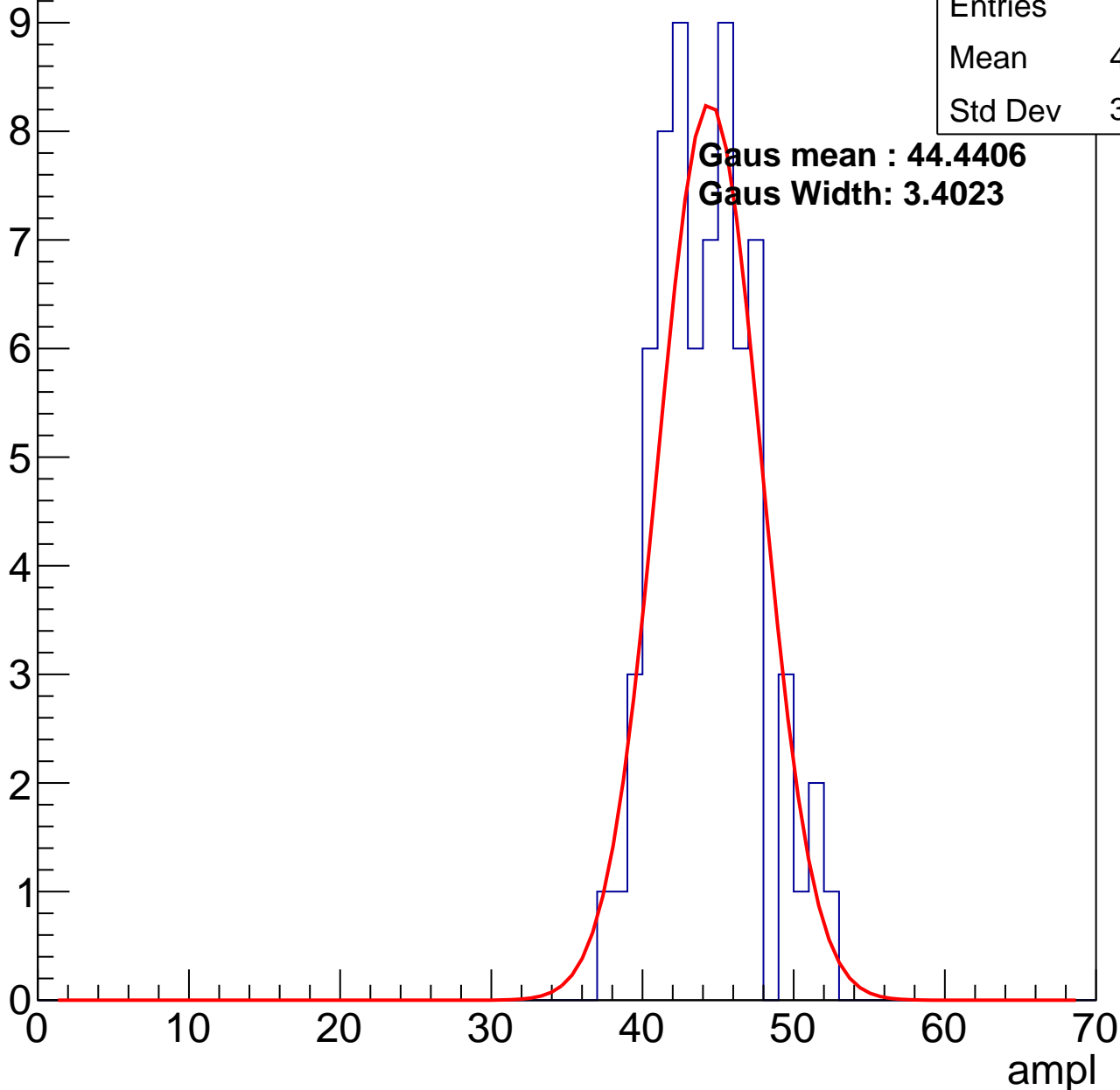
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	43.79
Std Dev	3.242

**Gaus mean : 44.4406**

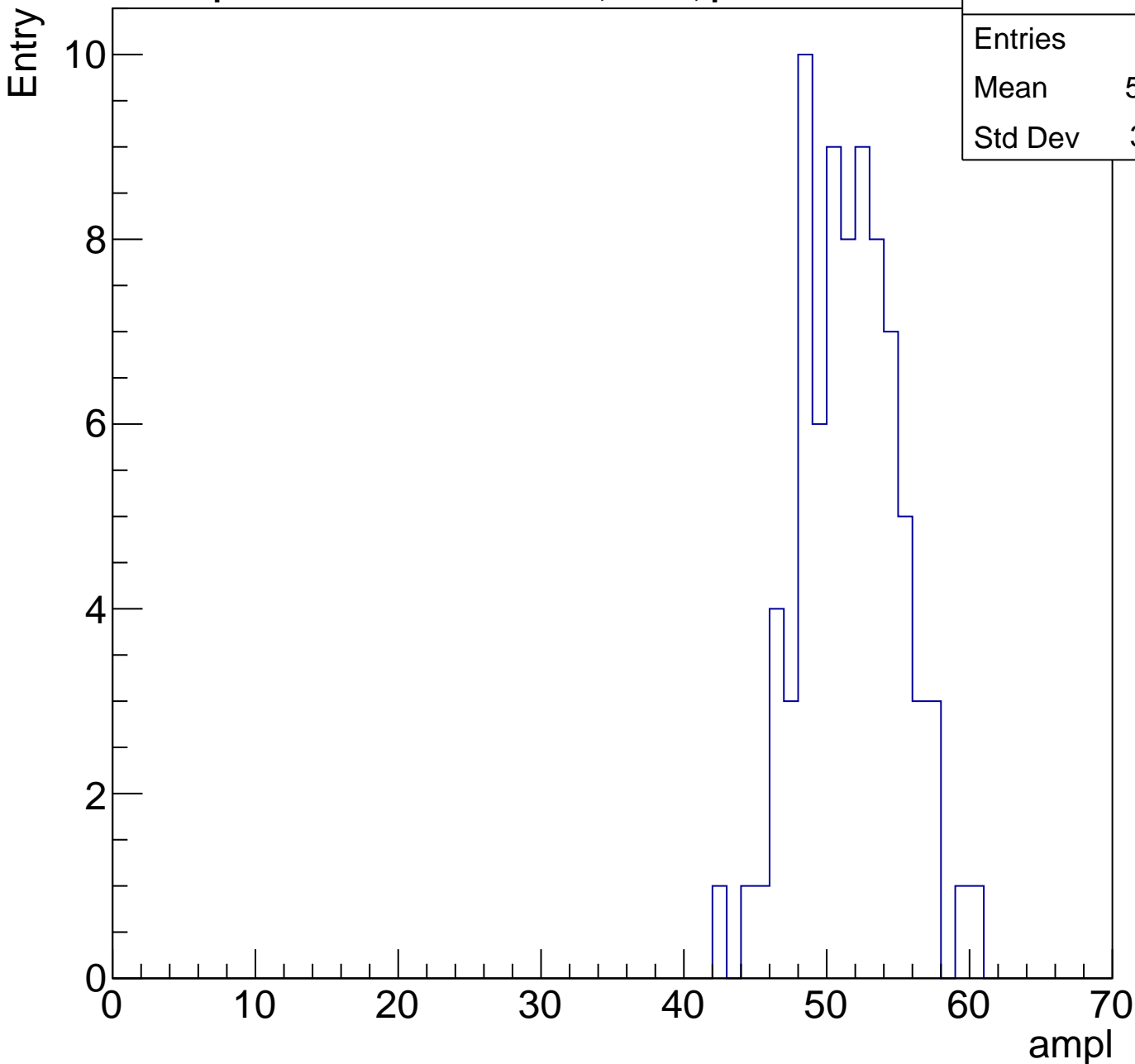
**Gaus Width: 3.4023**



# B1L101S, U11-ch4, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	80
Mean	51.14
Std Dev	3.441

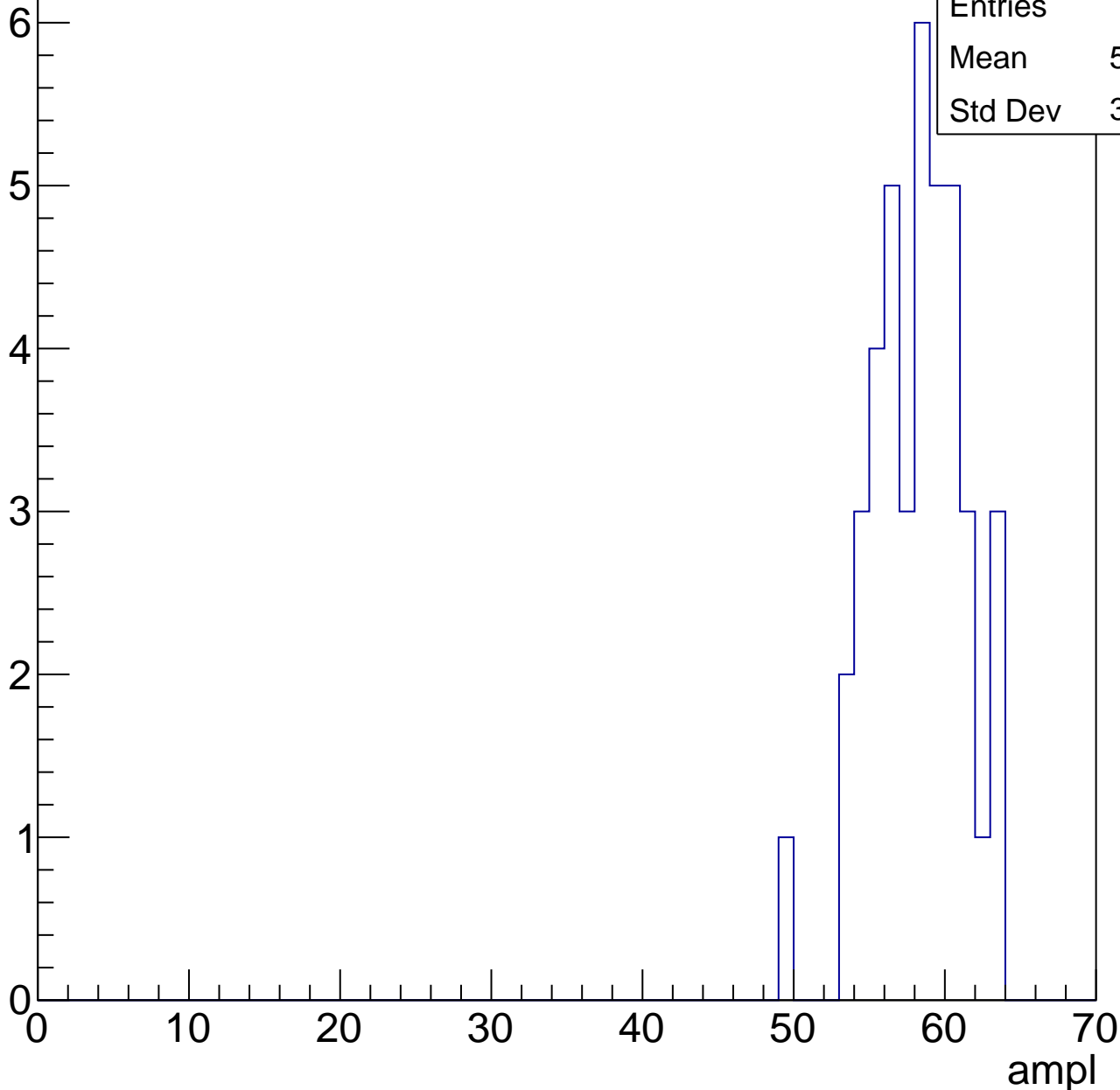


# B1L101S, U11-ch4, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	41
Mean	57.68
Std Dev	3.032

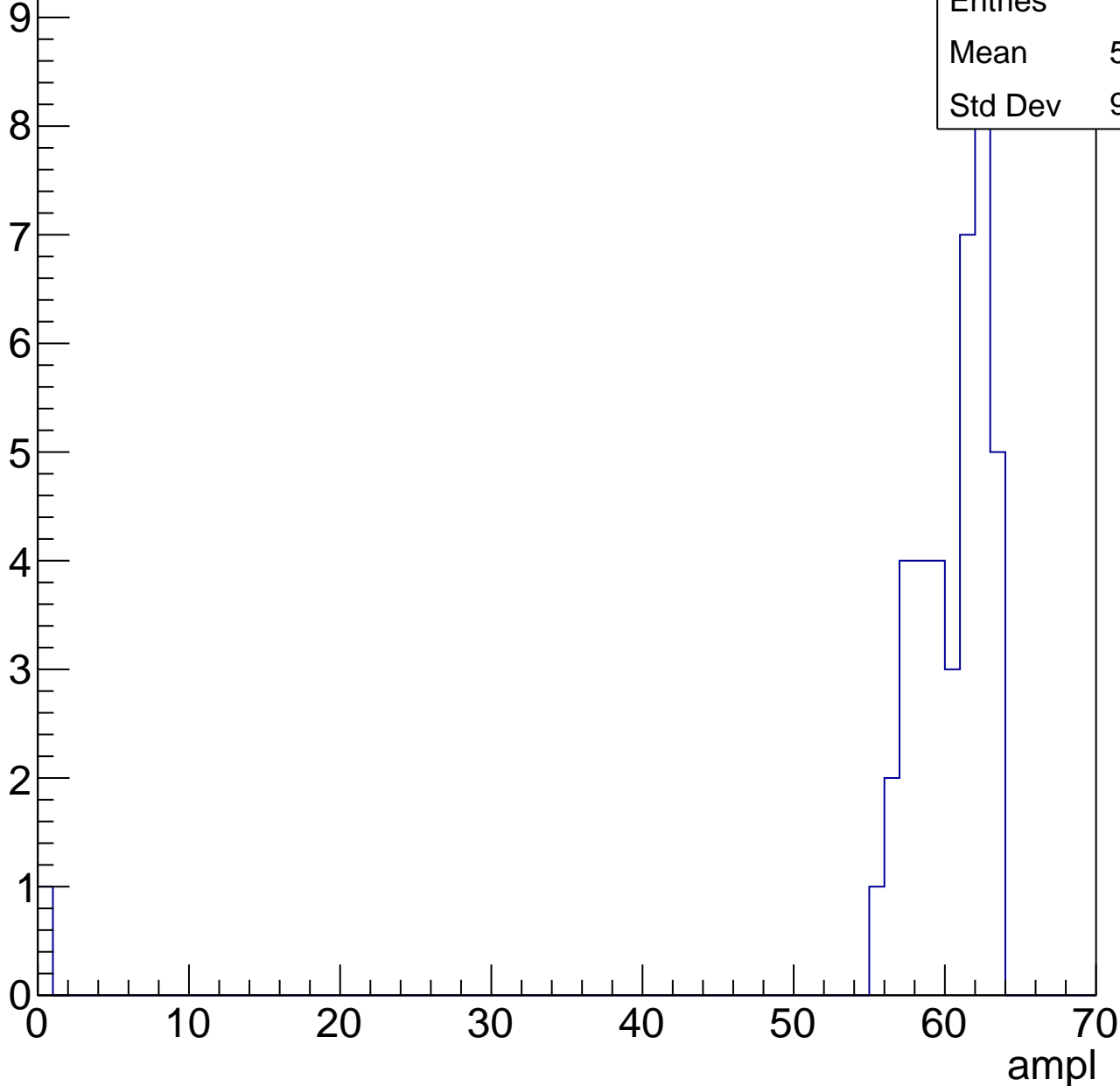


# B1L101S, U11-ch4, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	40
Mean	58.58
Std Dev	9.643



# B1L101S, U11-ch4, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch4, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U11-ch5, adc0

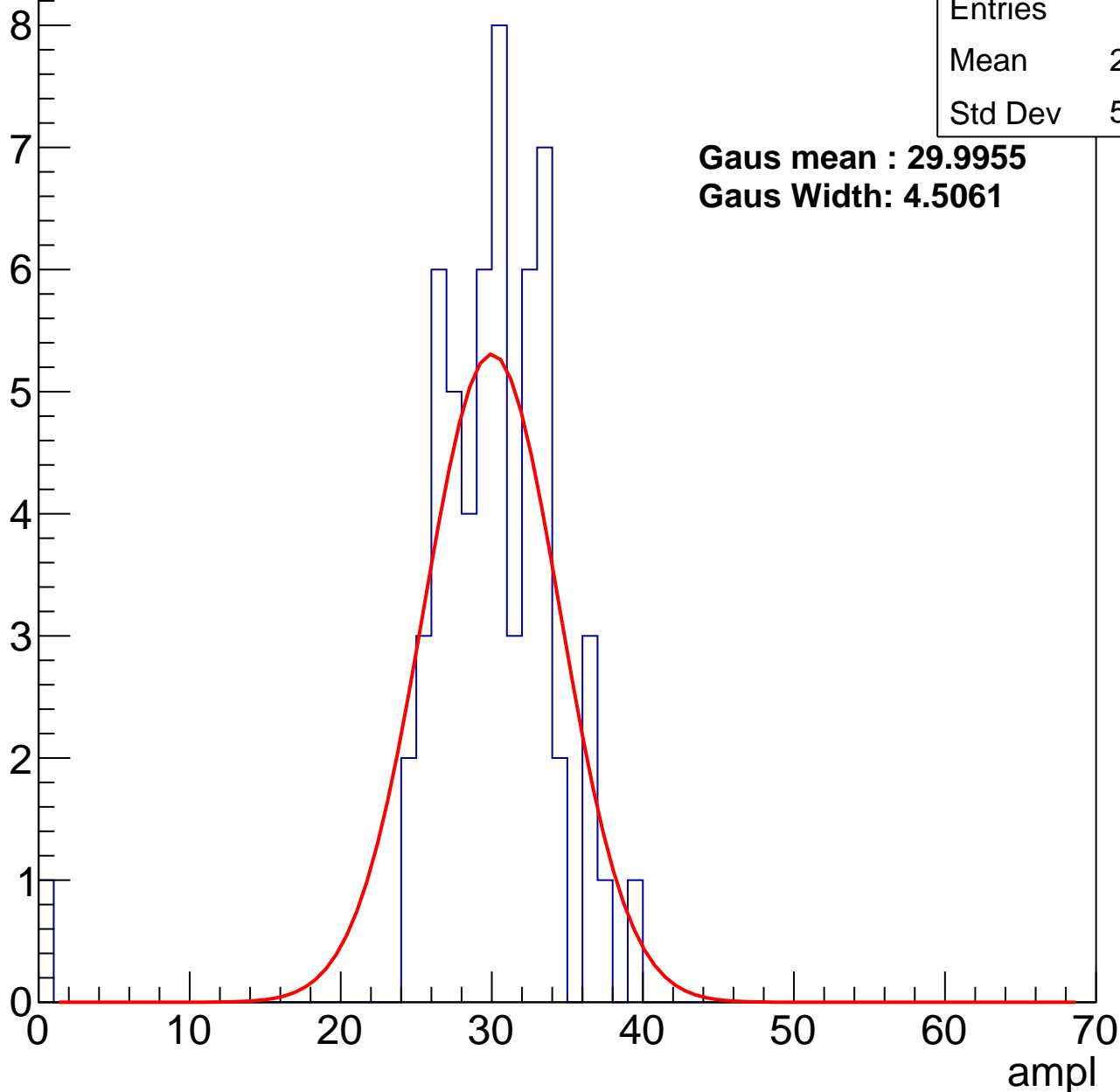
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	29.45
Std Dev	5.173

**Gaus mean : 29.9955**

**Gaus Width: 4.5061**



# B1L101S, U11-ch5, adc1

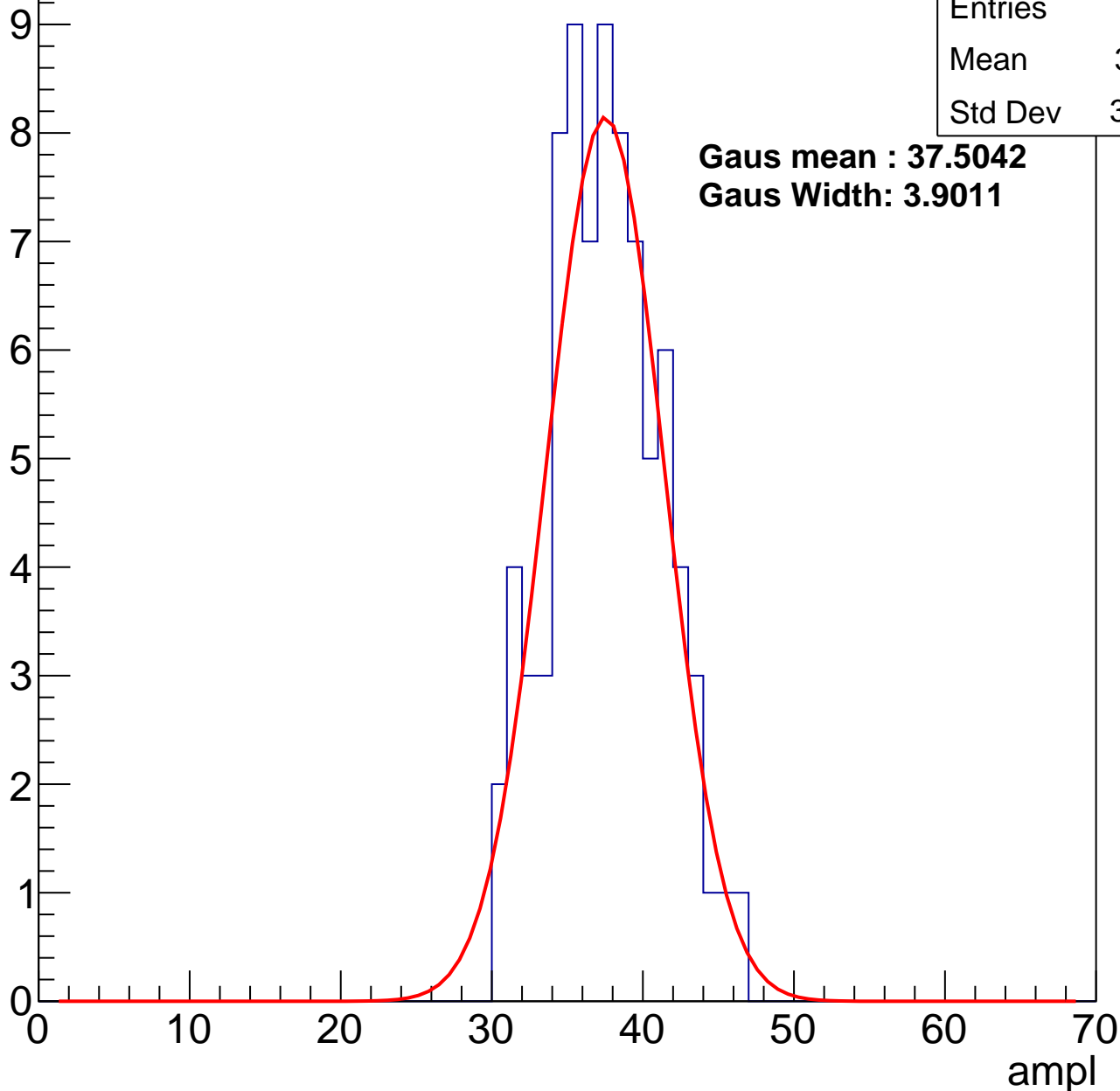
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	81
Mean	37.11
Std Dev	3.614

**Gaus mean : 37.5042**

**Gaus Width: 3.9011**



# B1L101S, U11-ch5, adc2

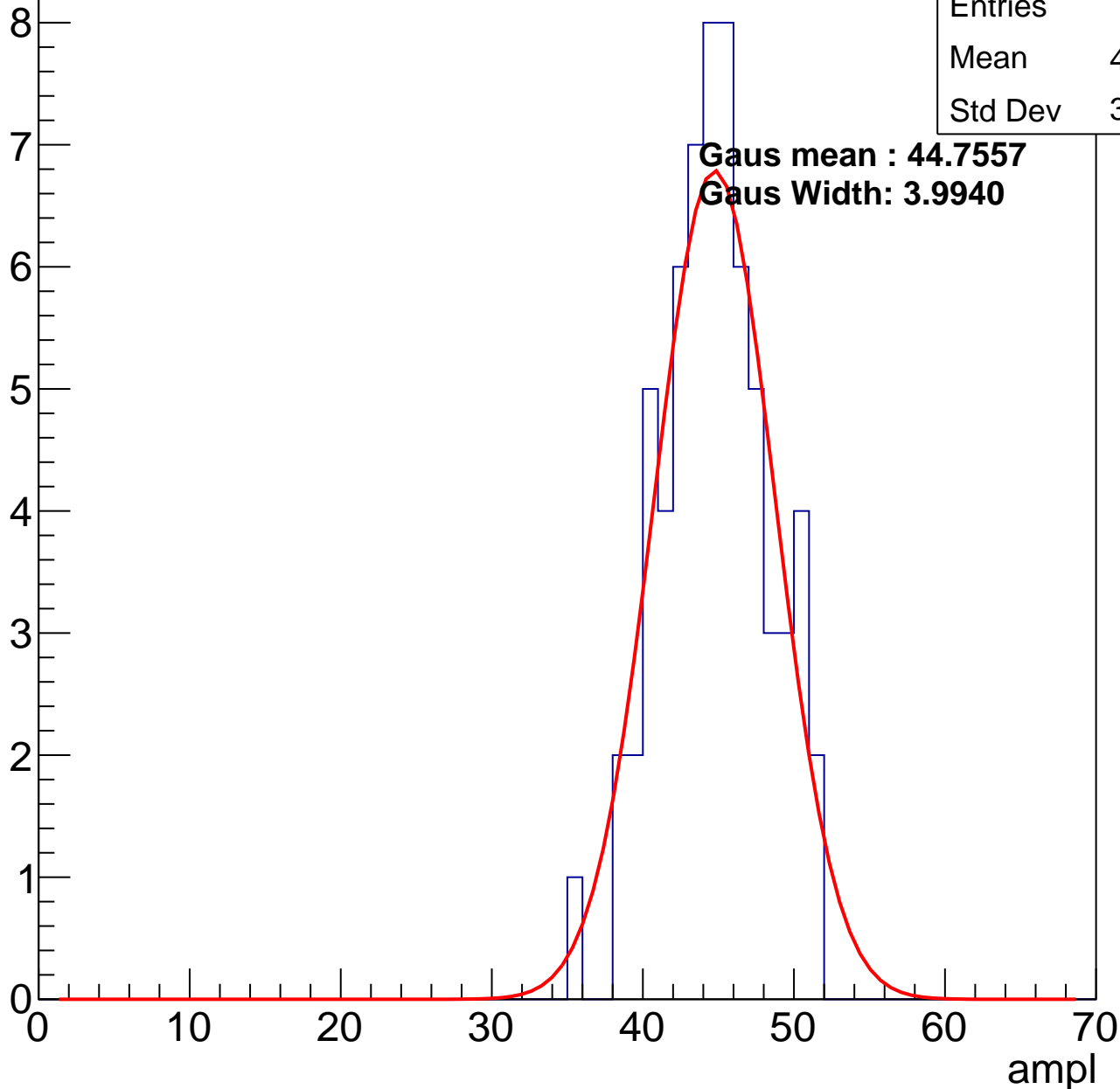
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	44.27
Std Dev	3.453

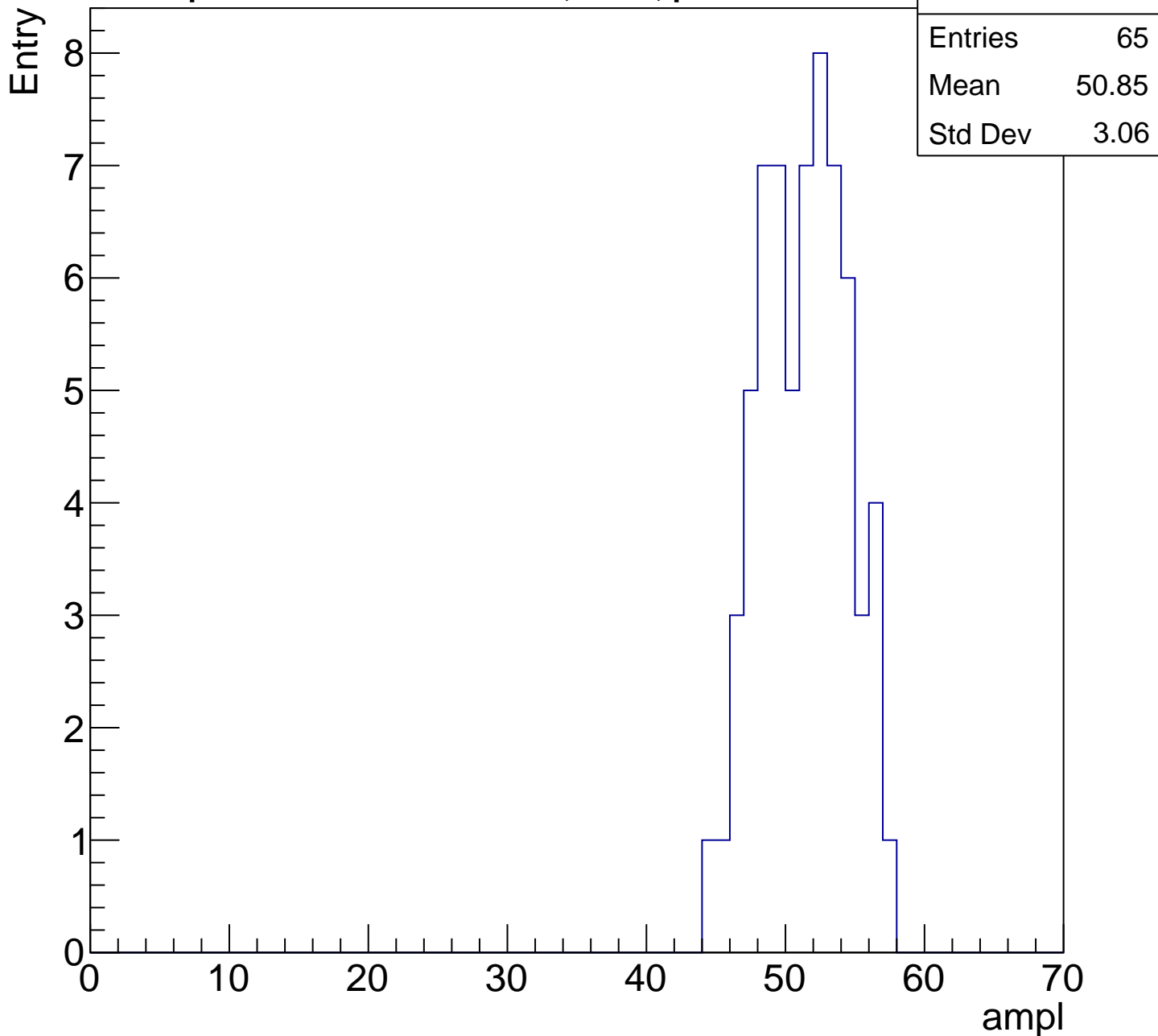
**Gaus mean : 44.7557**

**Gaus Width: 3.9940**



# B1L101S, U11-ch5, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

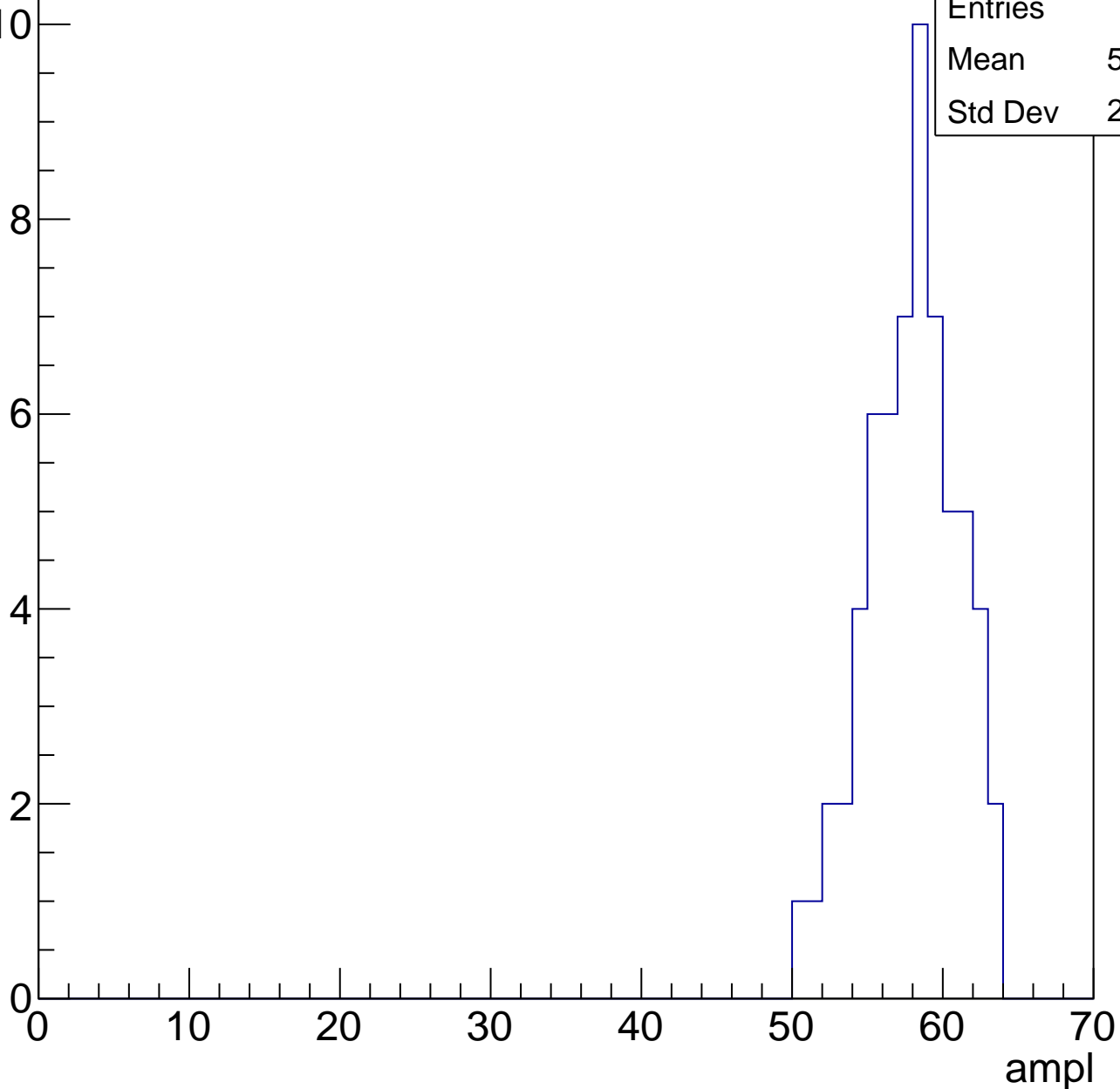


# B1L101S, U11-ch5, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	57.48
Std Dev	2.988

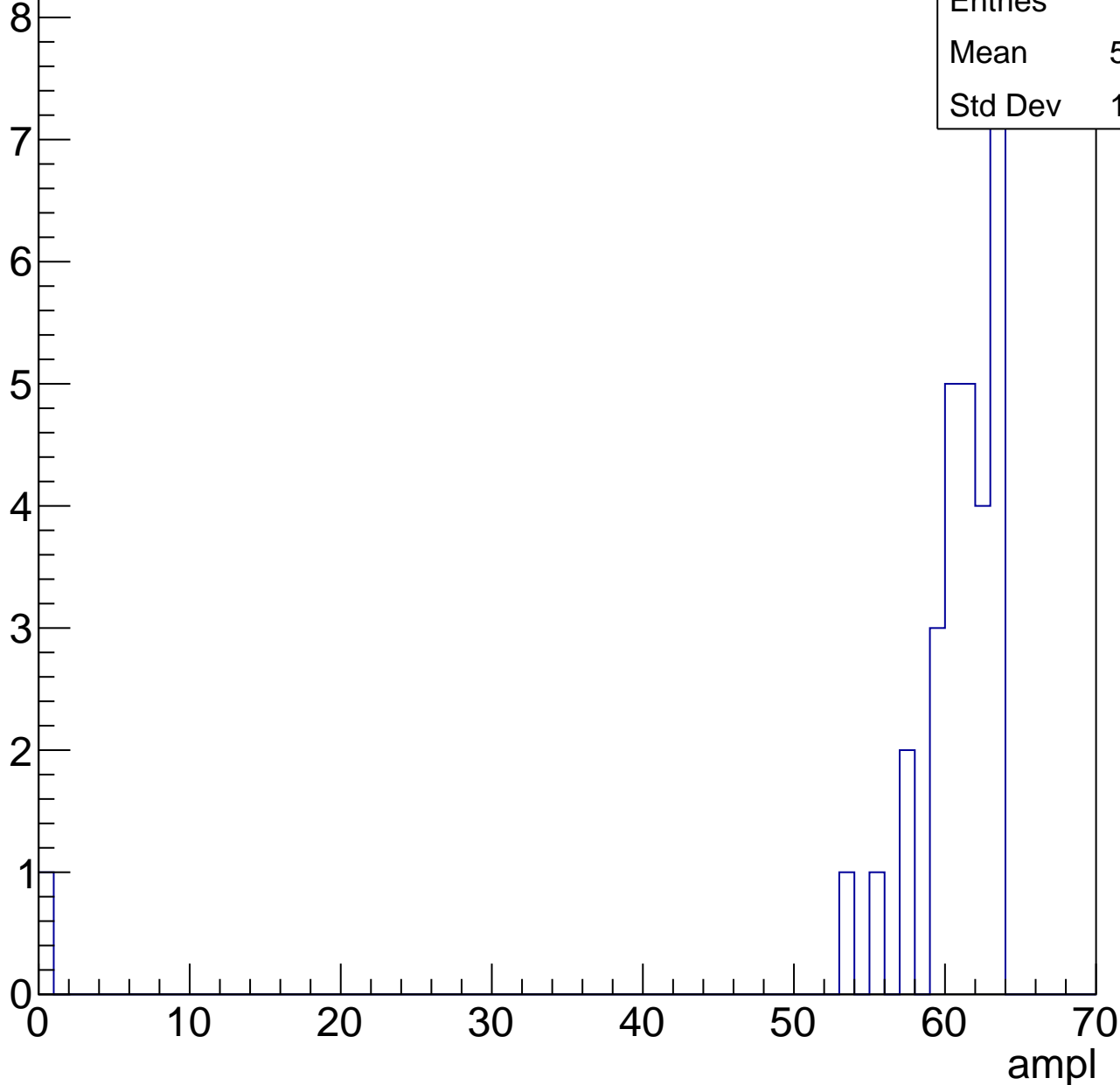


# B1L101S, U11-ch5, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	30
Mean	58.53
Std Dev	11.14



# B1L101S, U11-ch5, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch5, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U11-ch6, adc0

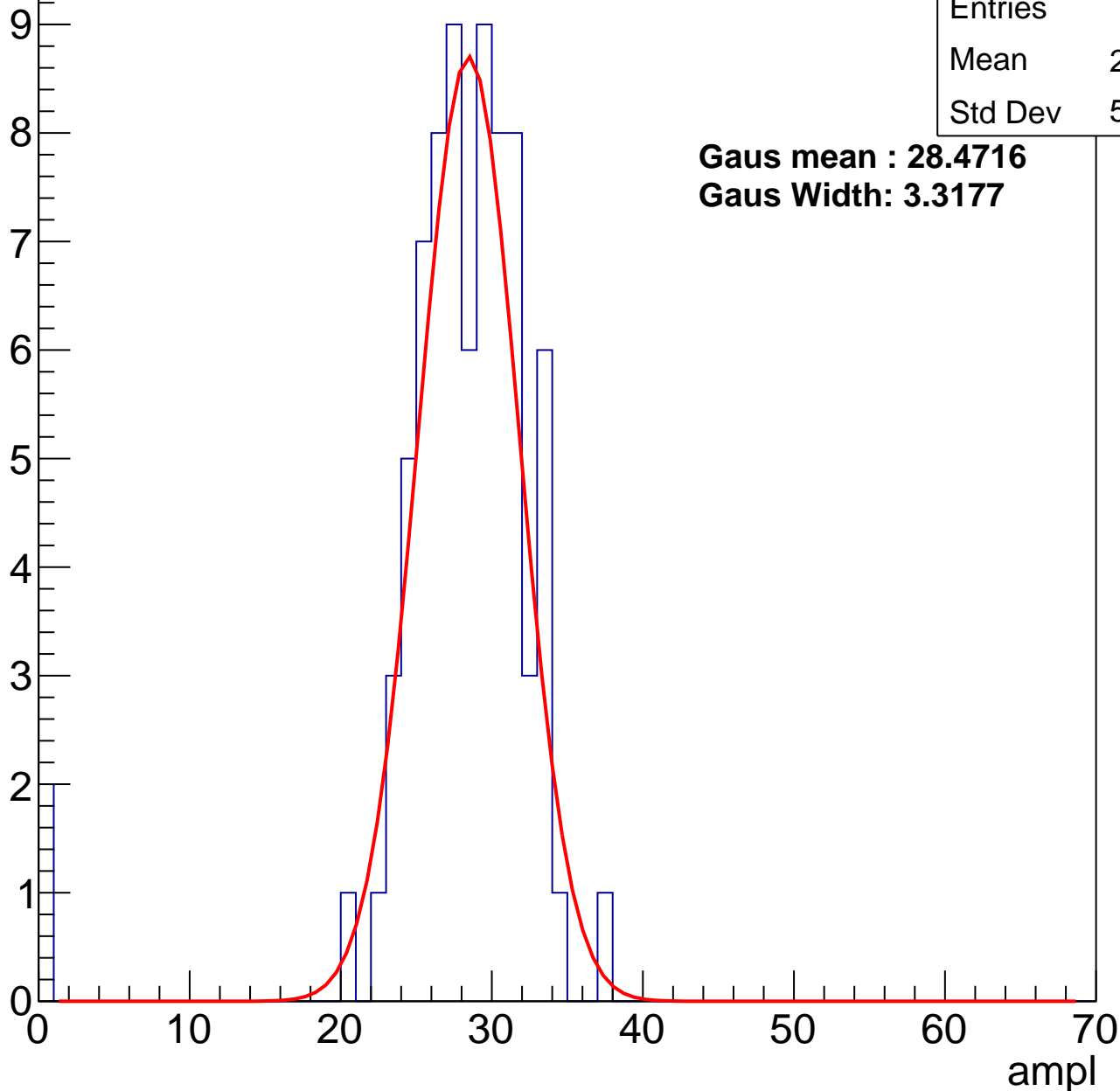
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	78
Mean	27.42
Std Dev	5.464

**Gaus mean : 28.4716**

**Gaus Width: 3.3177**



# B1L101S, U11-ch6, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	82
Mean	35.71
Std Dev	3.469

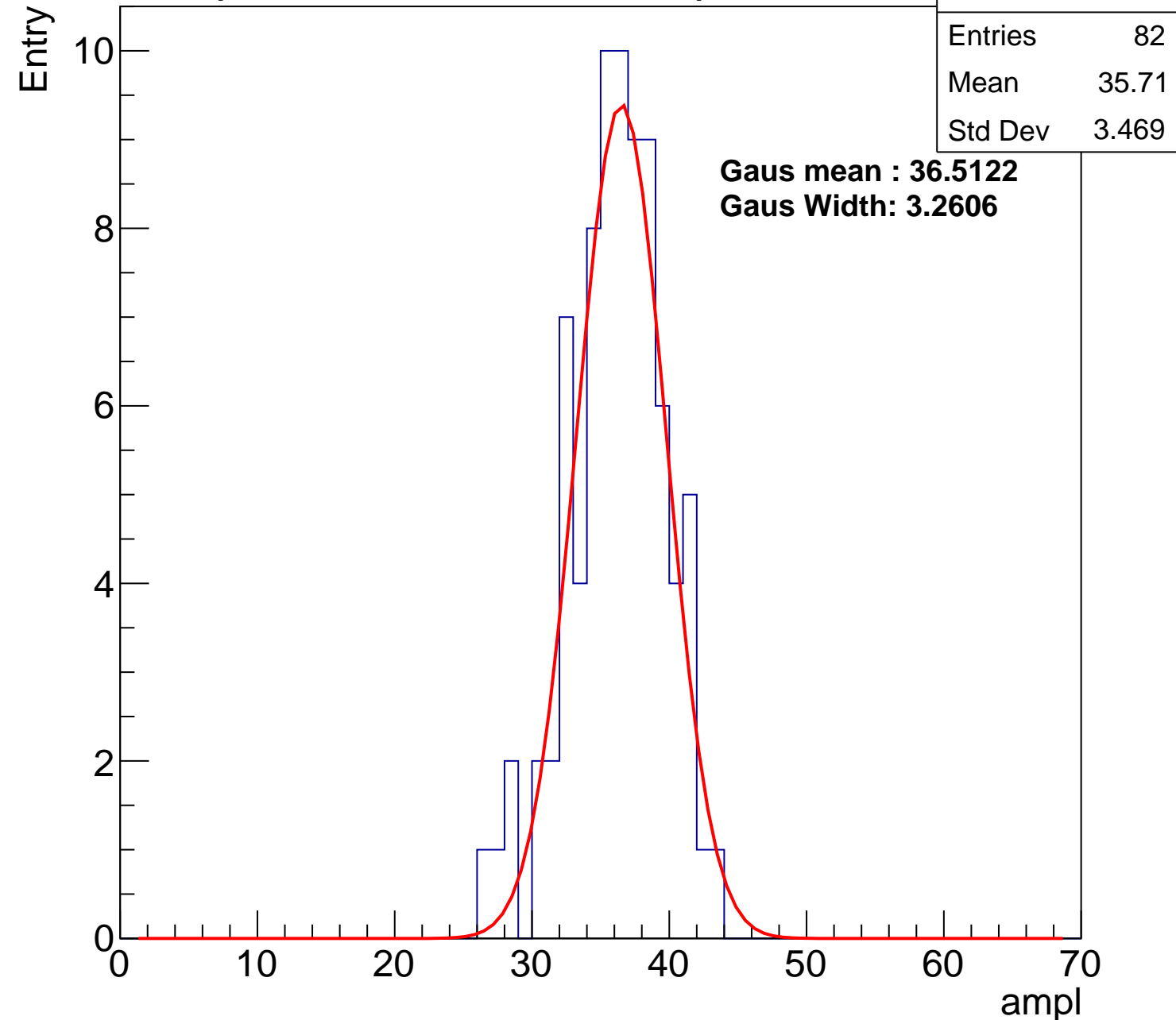
**Gaus mean : 36.5122**  
**Gaus Width: 3.2606**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U11-ch6, adc2

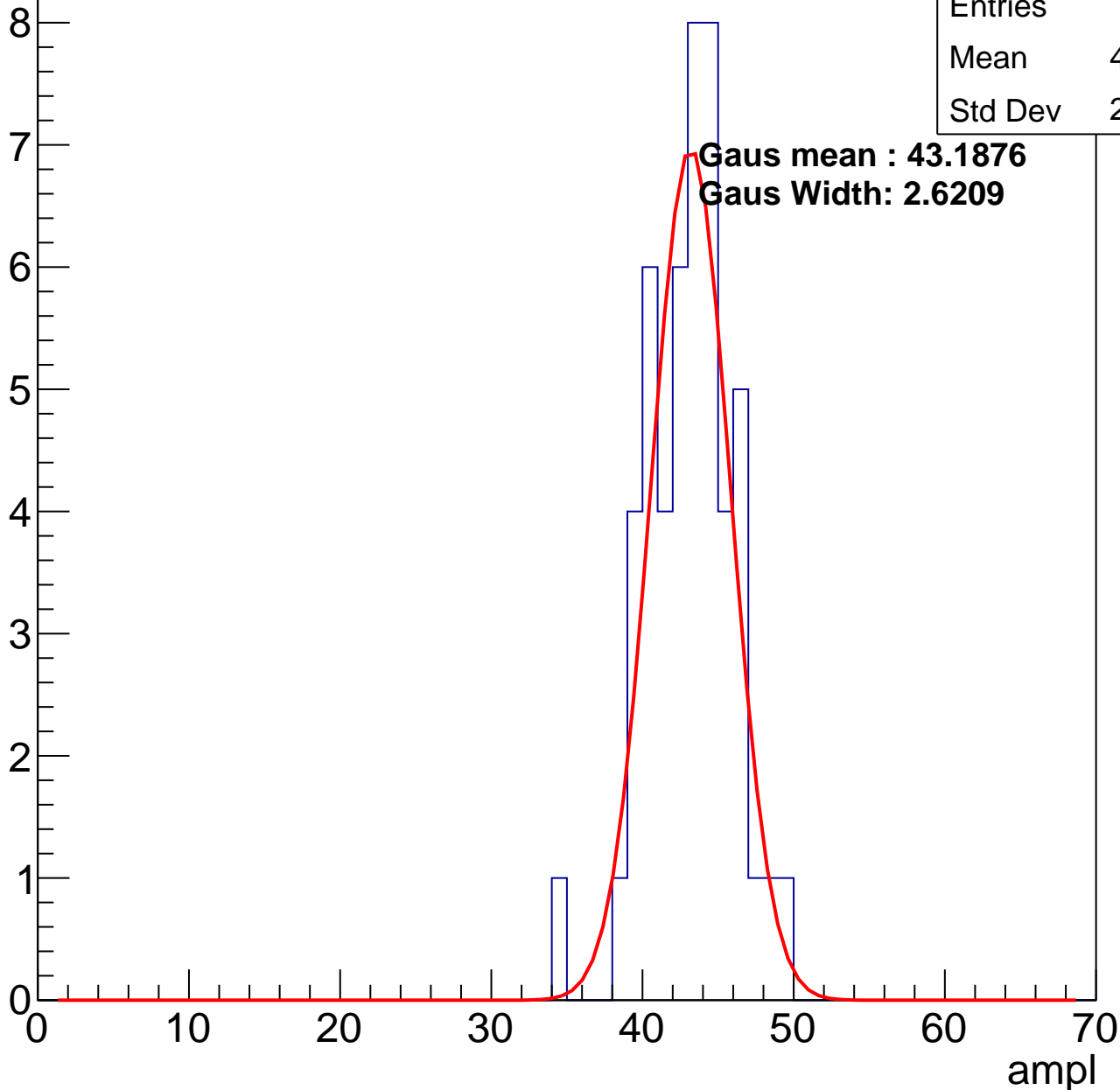
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	42.68
Std Dev	2.782

**Gaus mean : 43.1876**

**Gaus Width: 2.6209**

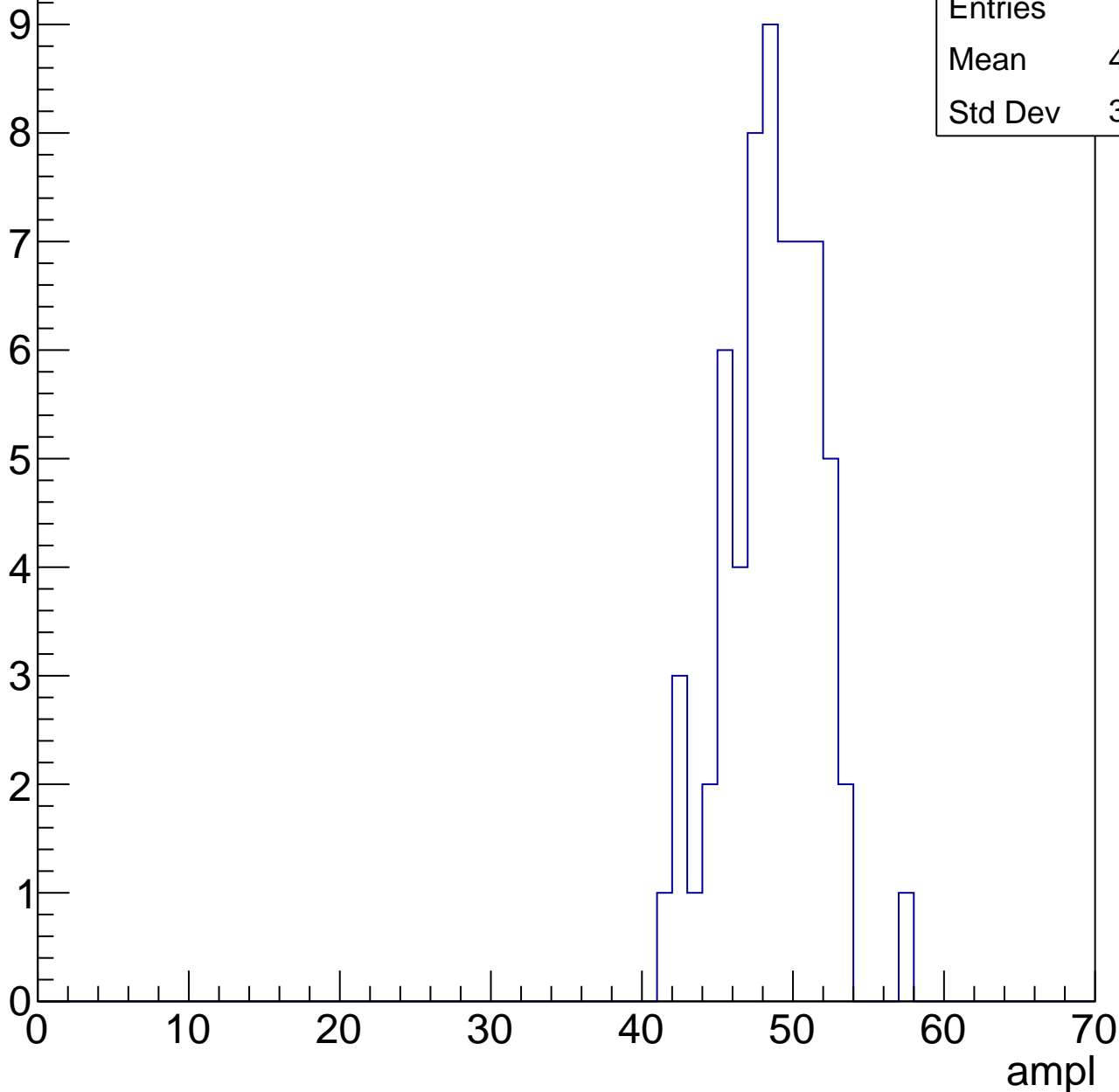


# B1L101S, U11-ch6, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	48.14
Std Dev	3.085

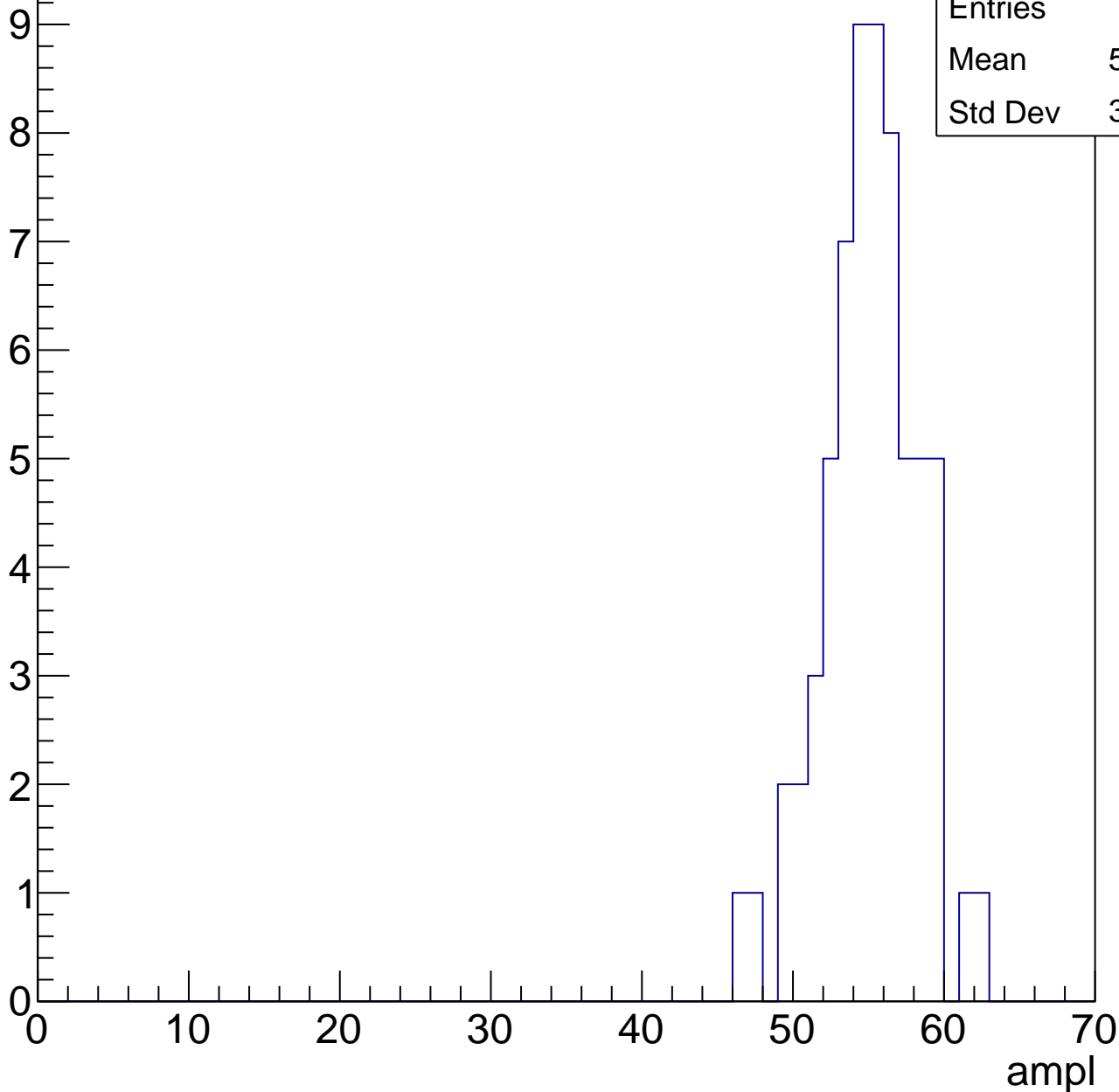


# B1L101S, U11-ch6, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

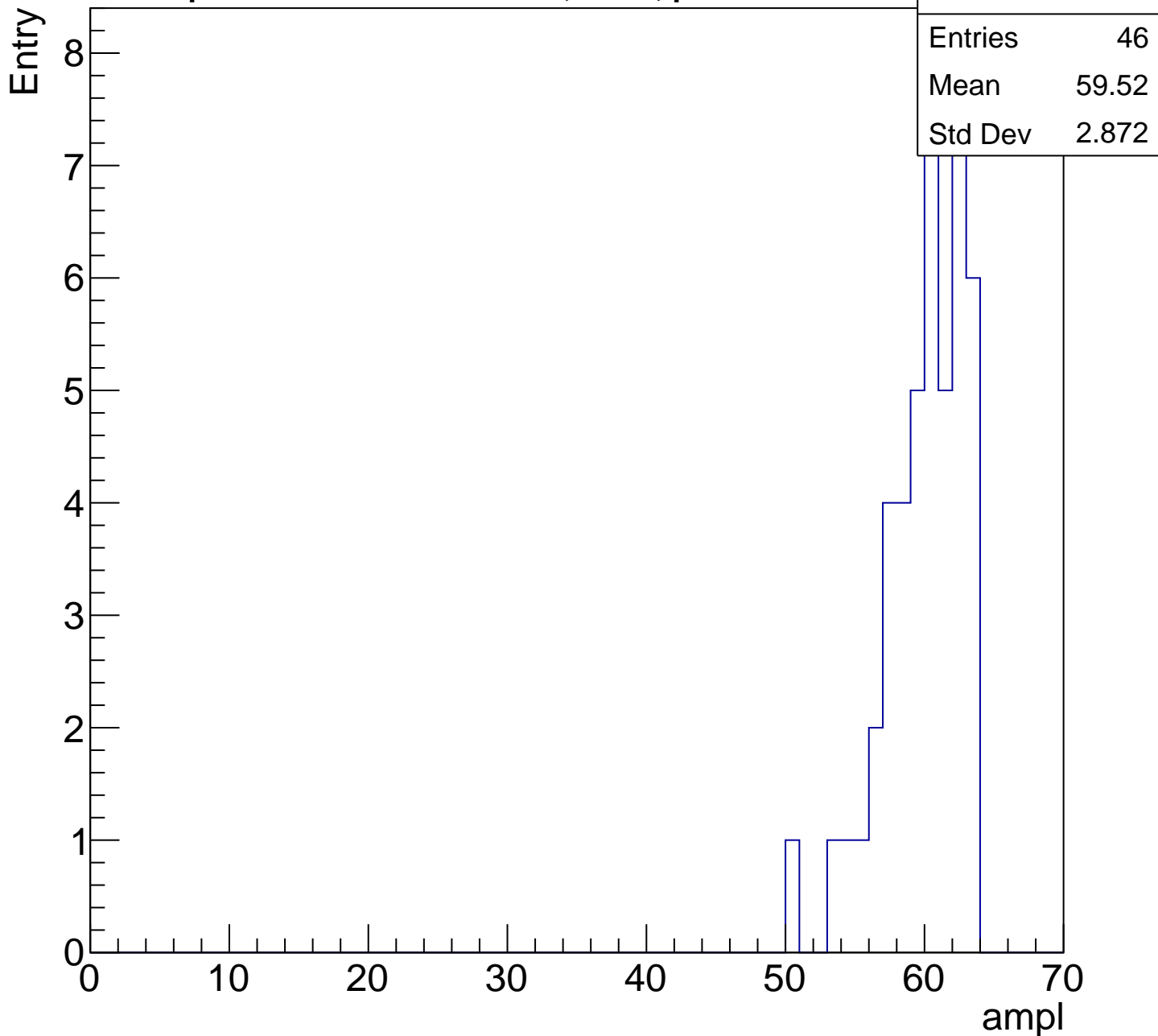
Entry

Entries	64
Mean	54.64
Std Dev	3.129



# B1L101S, U11-ch6, adc5

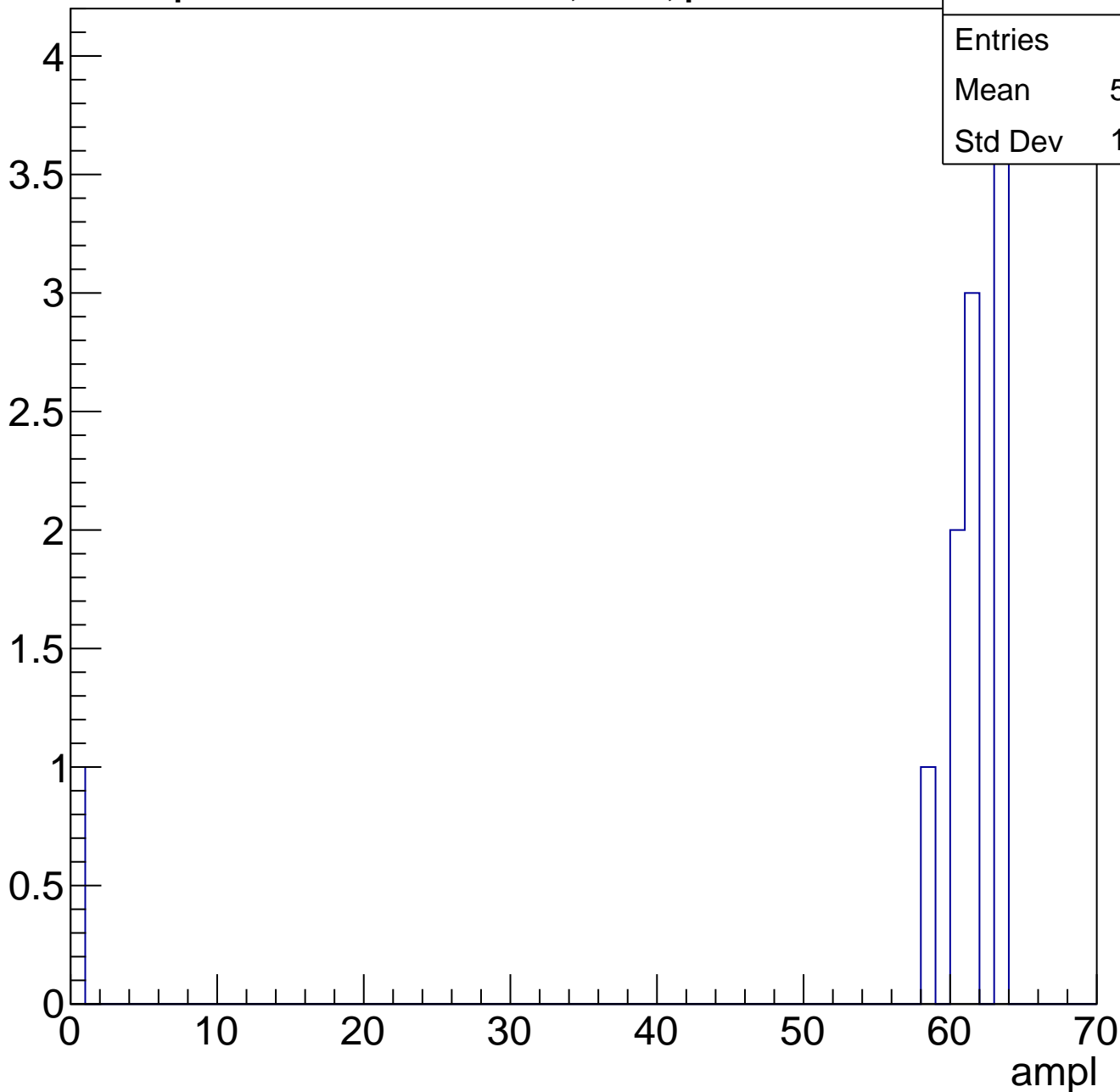
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U11-ch6, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

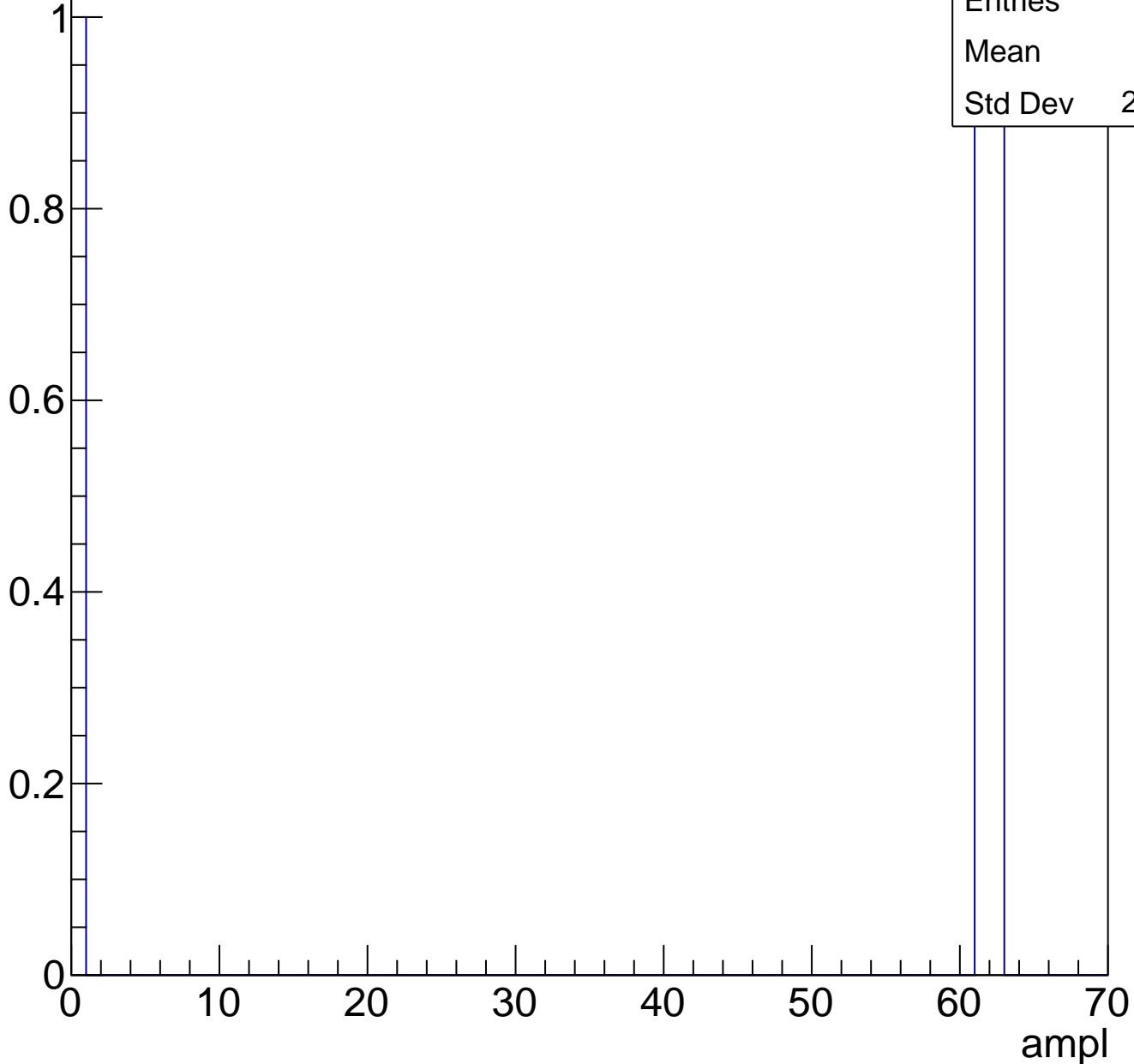




# B1L101S, U11-ch6, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U11-ch7, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	83
Mean	30.67
Std Dev	3.151

**Gaus mean : 31.0257**

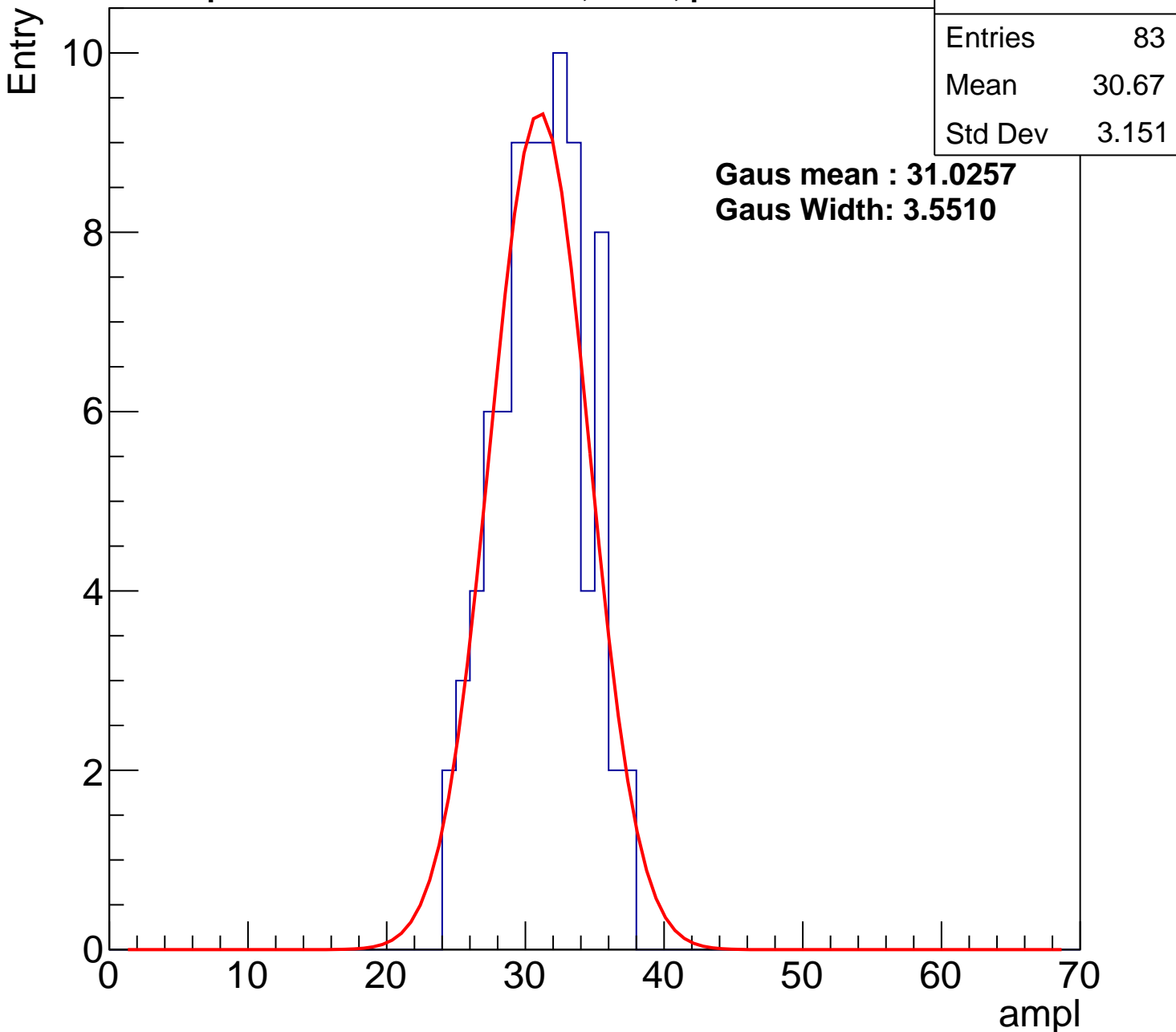
**Gaus Width: 3.5510**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U11-ch7, adc1

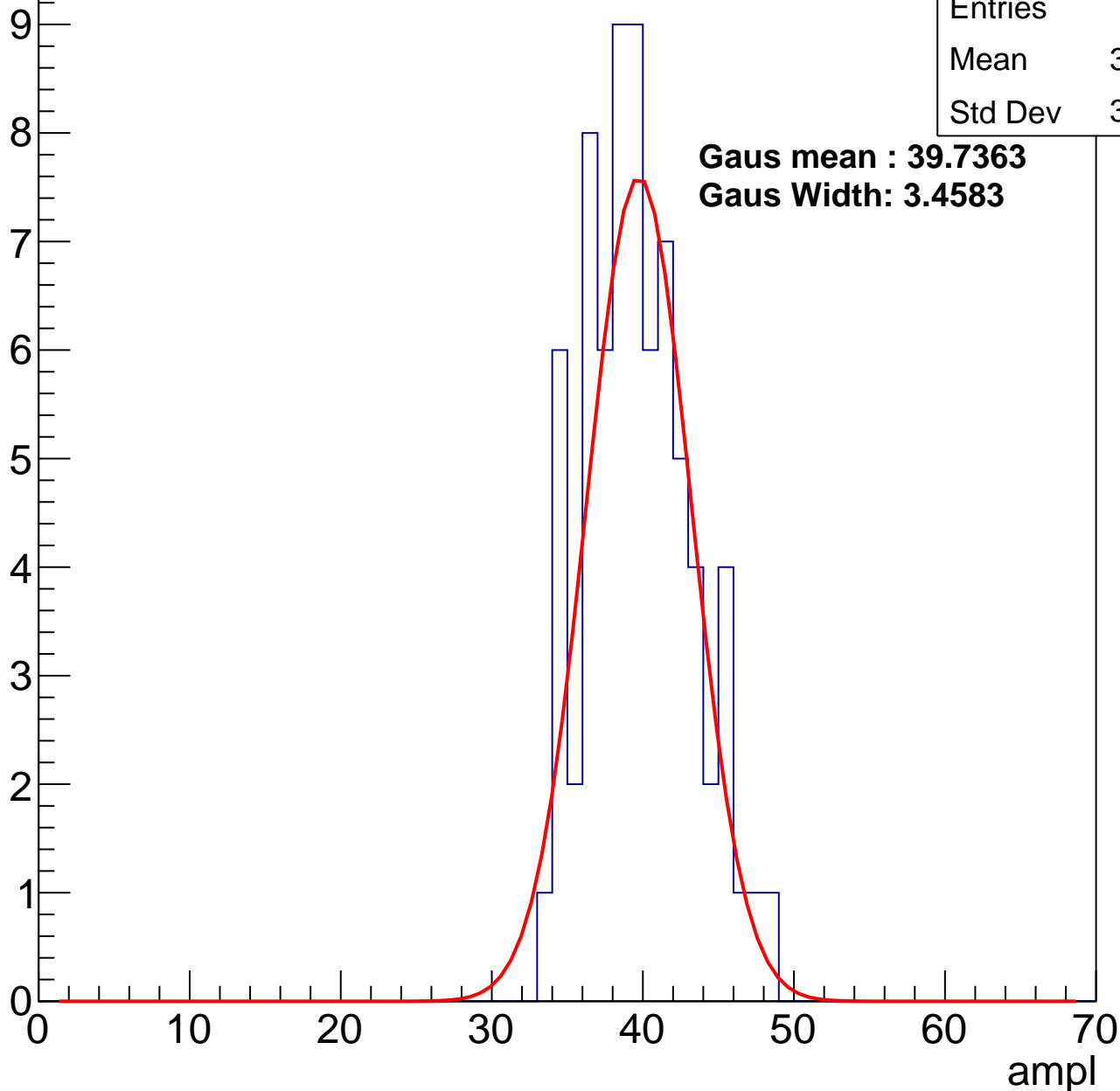
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	39.28
Std Dev	3.433

**Gaus mean : 39.7363**

**Gaus Width: 3.4583**



# B1L101S, U11-ch7, adc2

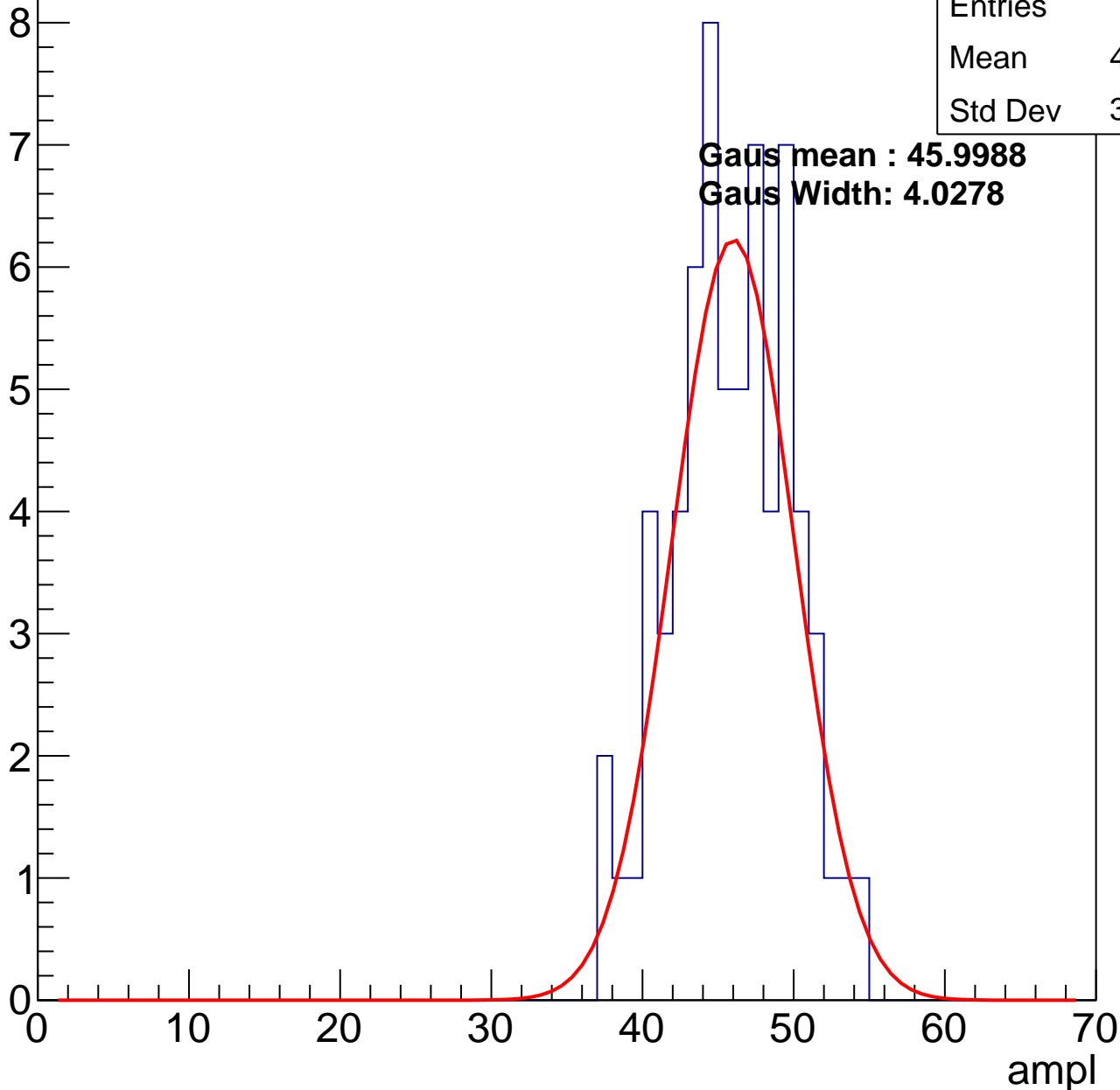
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	45.42
Std Dev	3.864

Gaus mean : 45.9988

Gaus Width: 4.0278

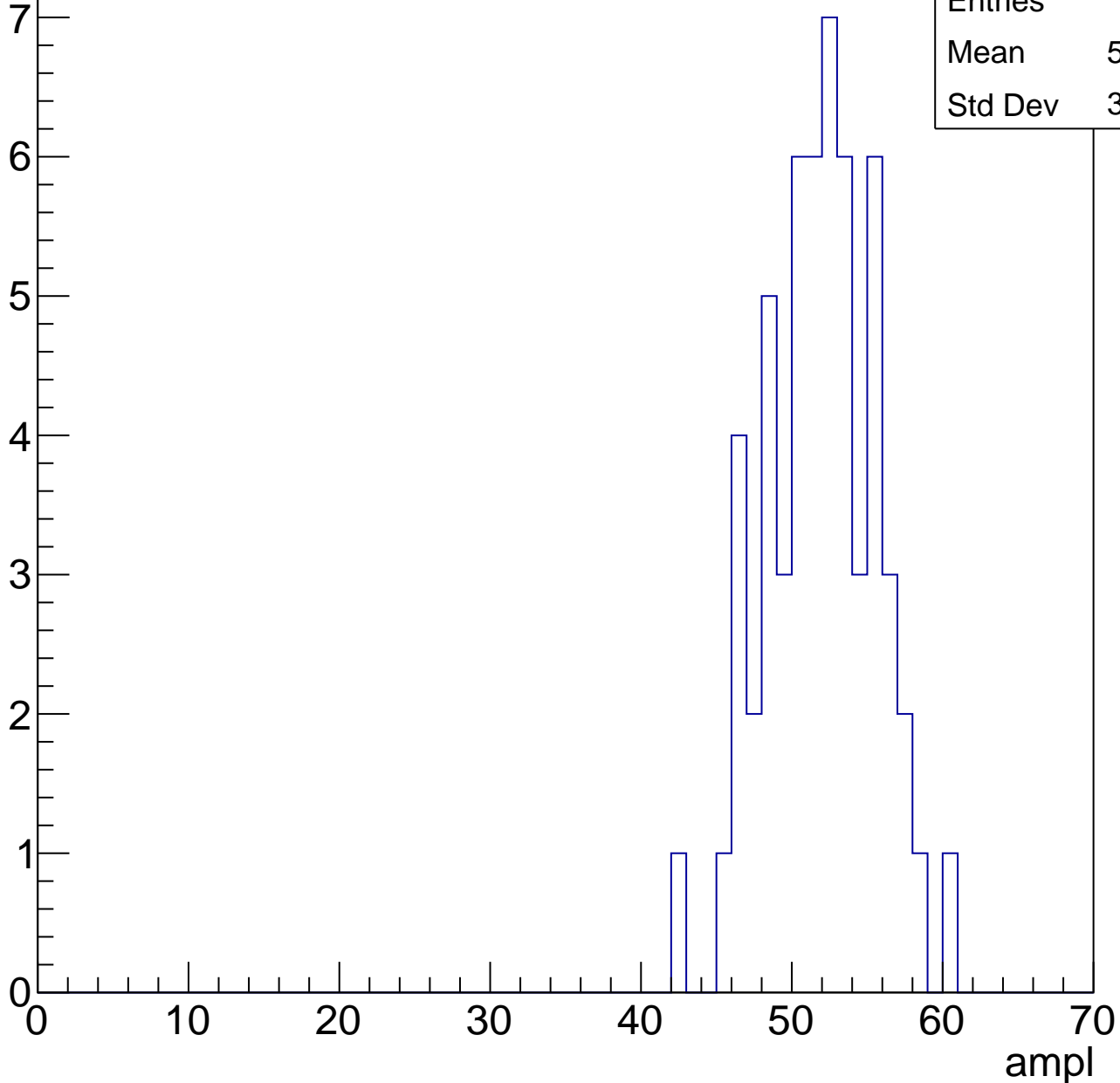


# B1L101S, U11-ch7, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	51.44
Std Dev	3.584

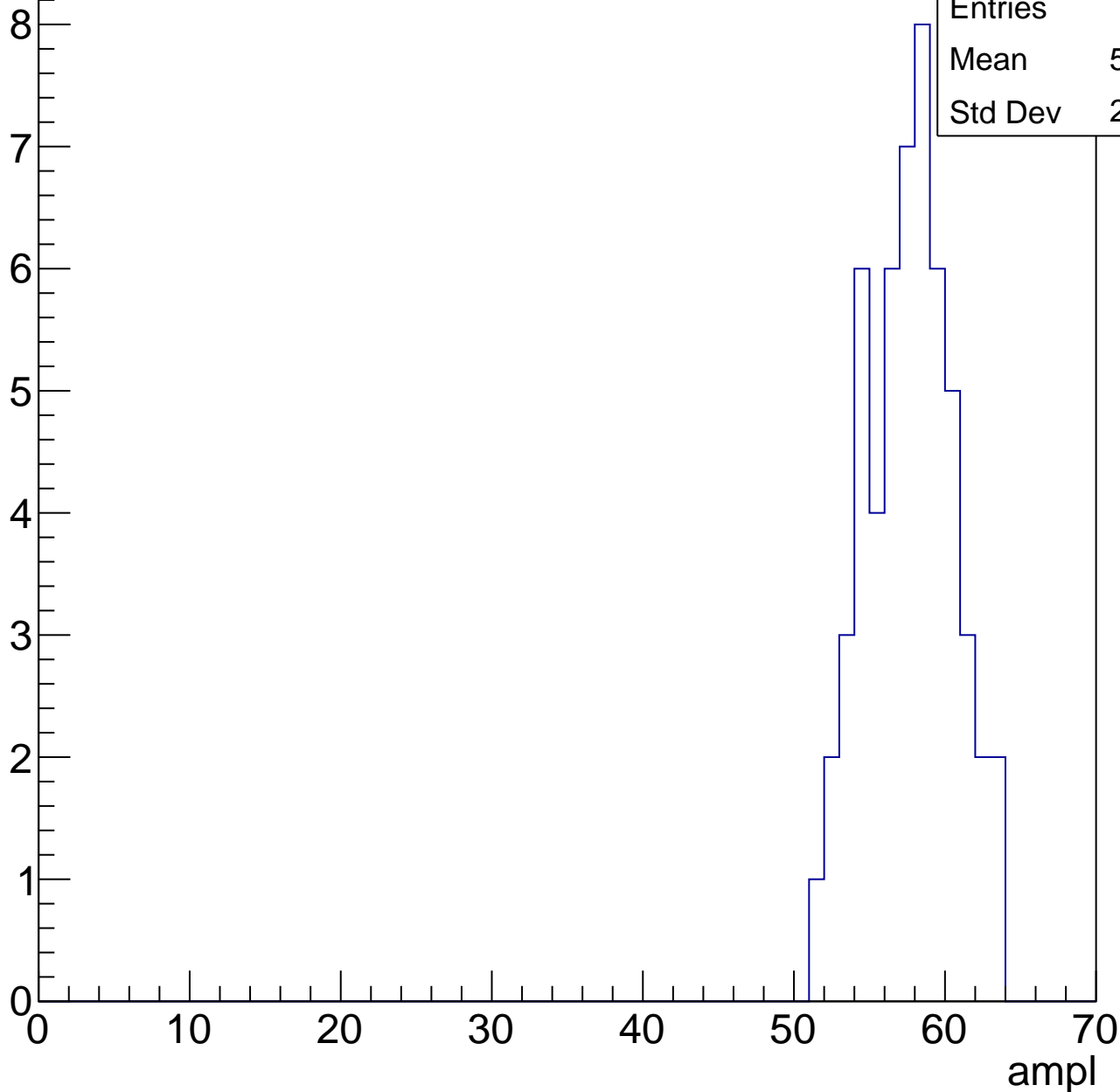


# B1L101S, U11-ch7, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	57.16
Std Dev	2.878

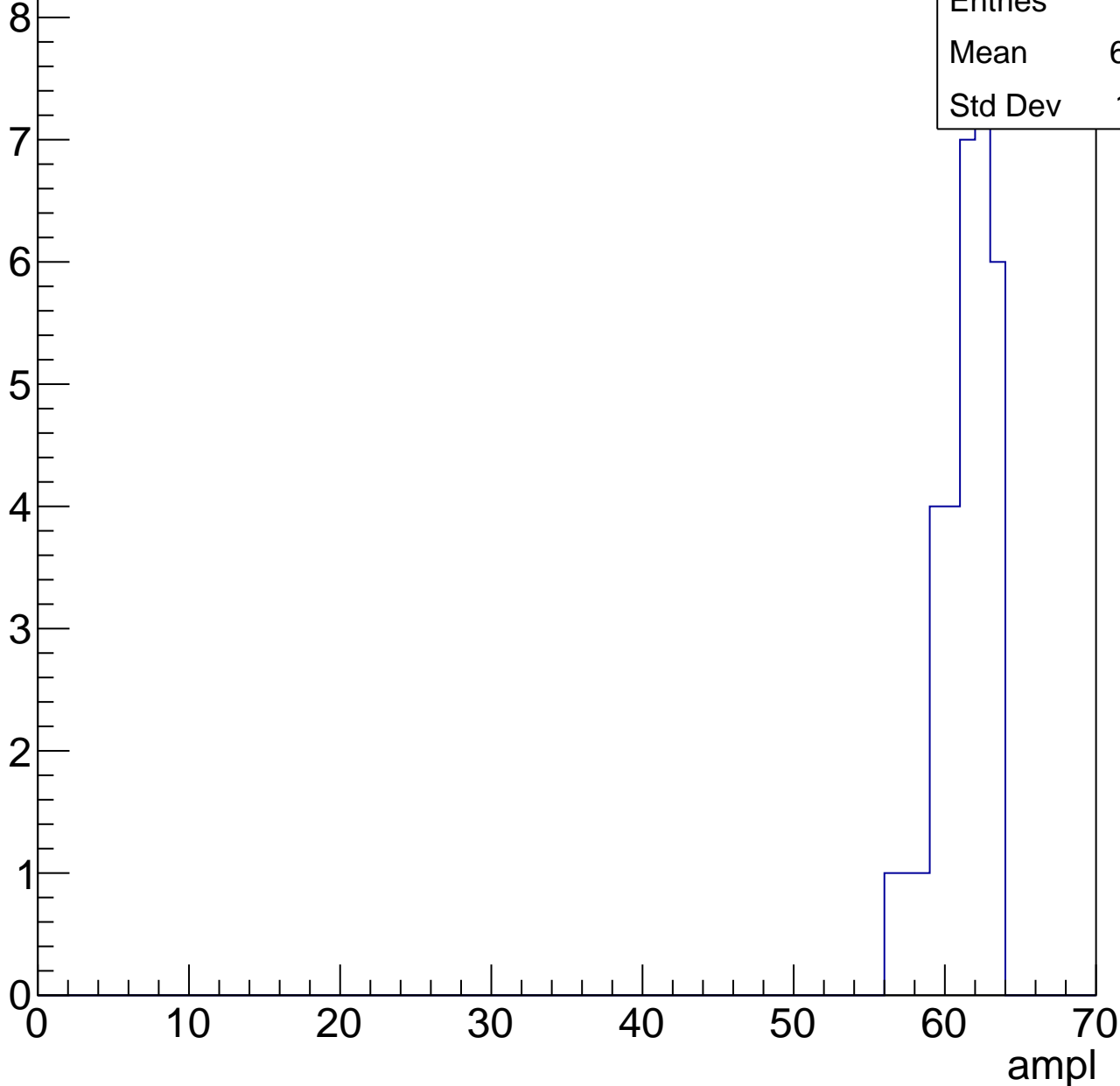


# B1L101S, U11-ch7, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	32
Mean	60.88
Std Dev	1.781



# B1L101S, U11-ch7, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch7, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U11-ch8, adc0

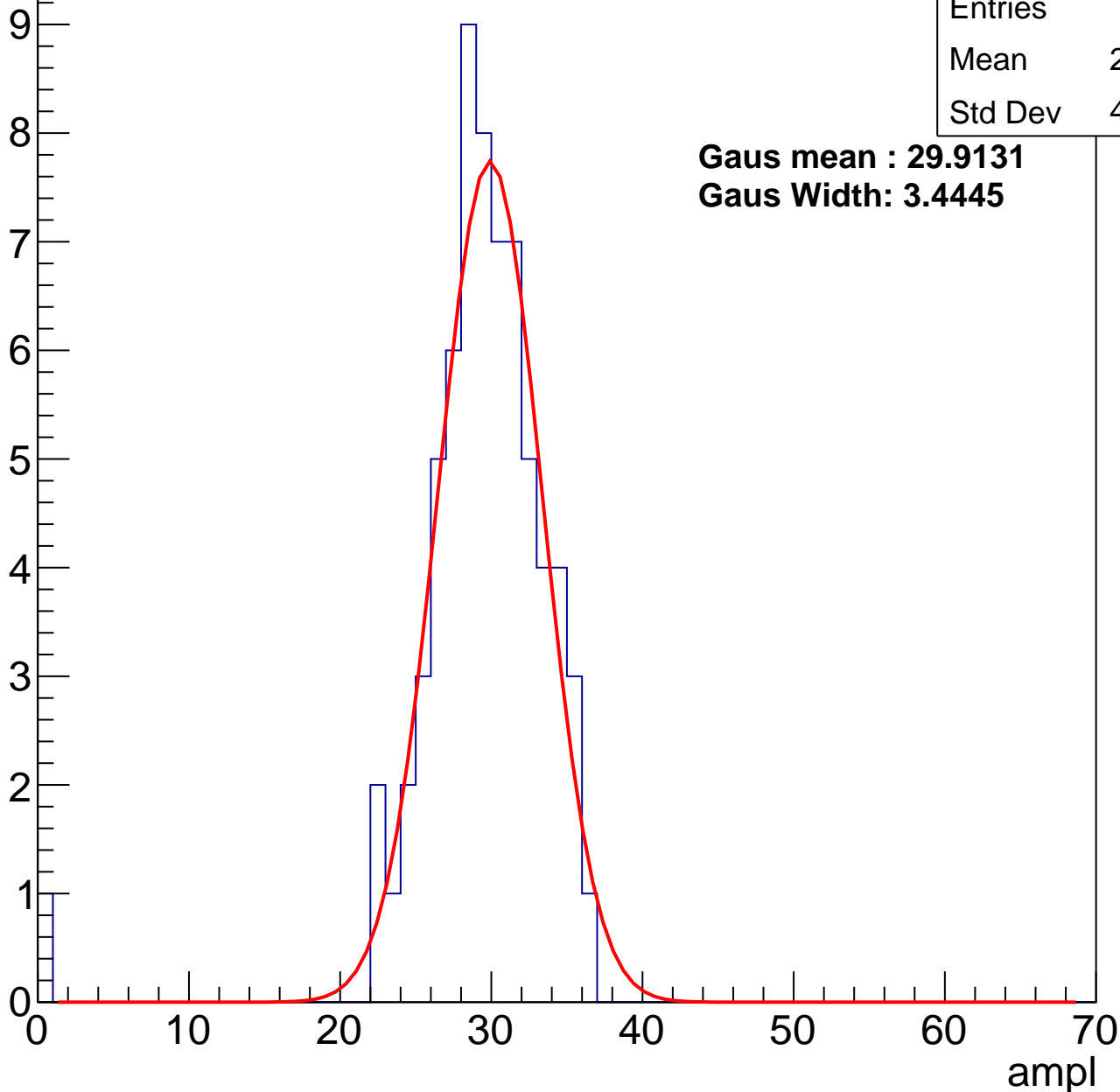
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	28.85
Std Dev	4.775

**Gaus mean : 29.9131**

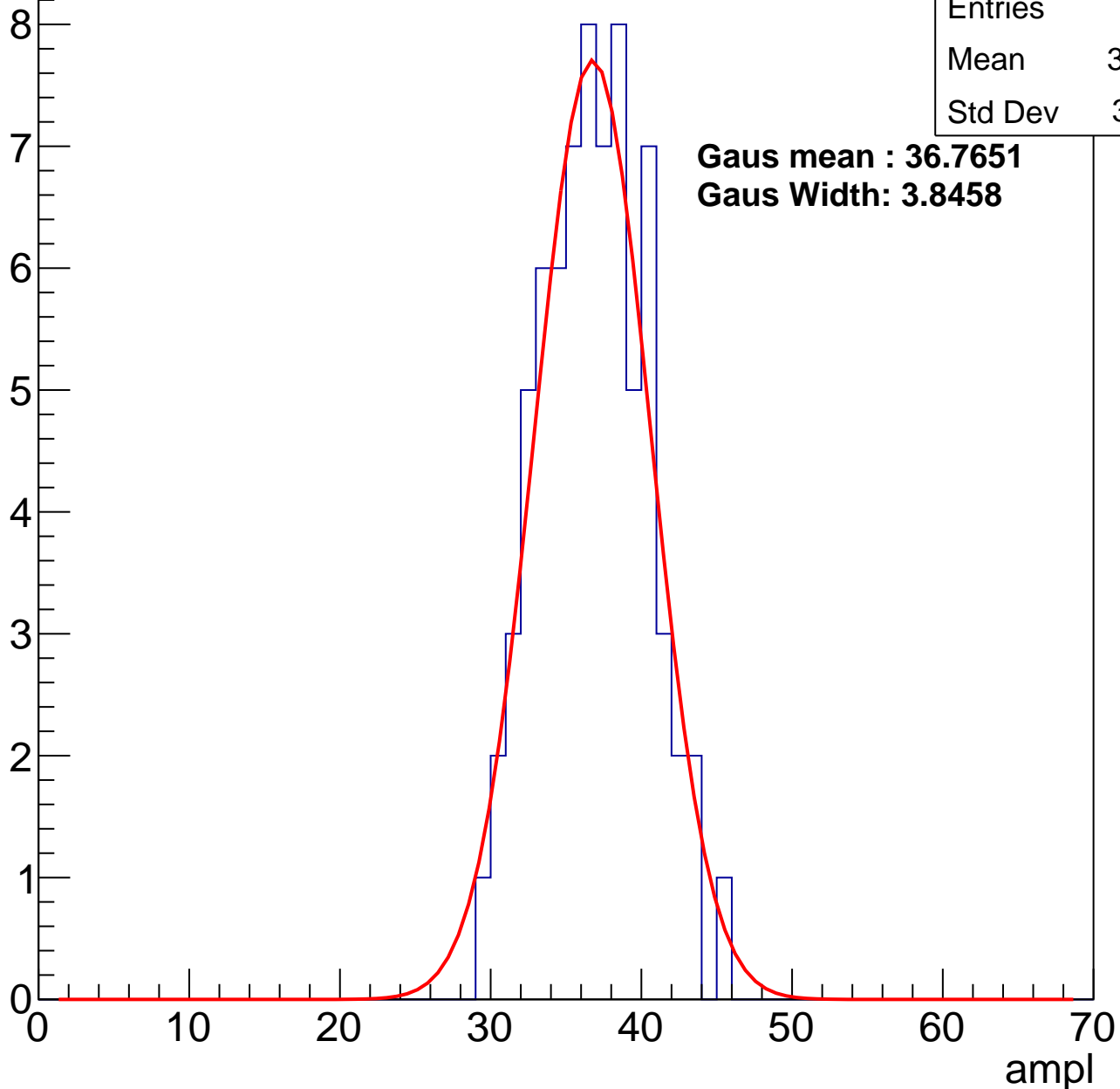
**Gaus Width: 3.4445**



# B1L101S, U11-ch8, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U11-ch8, adc2

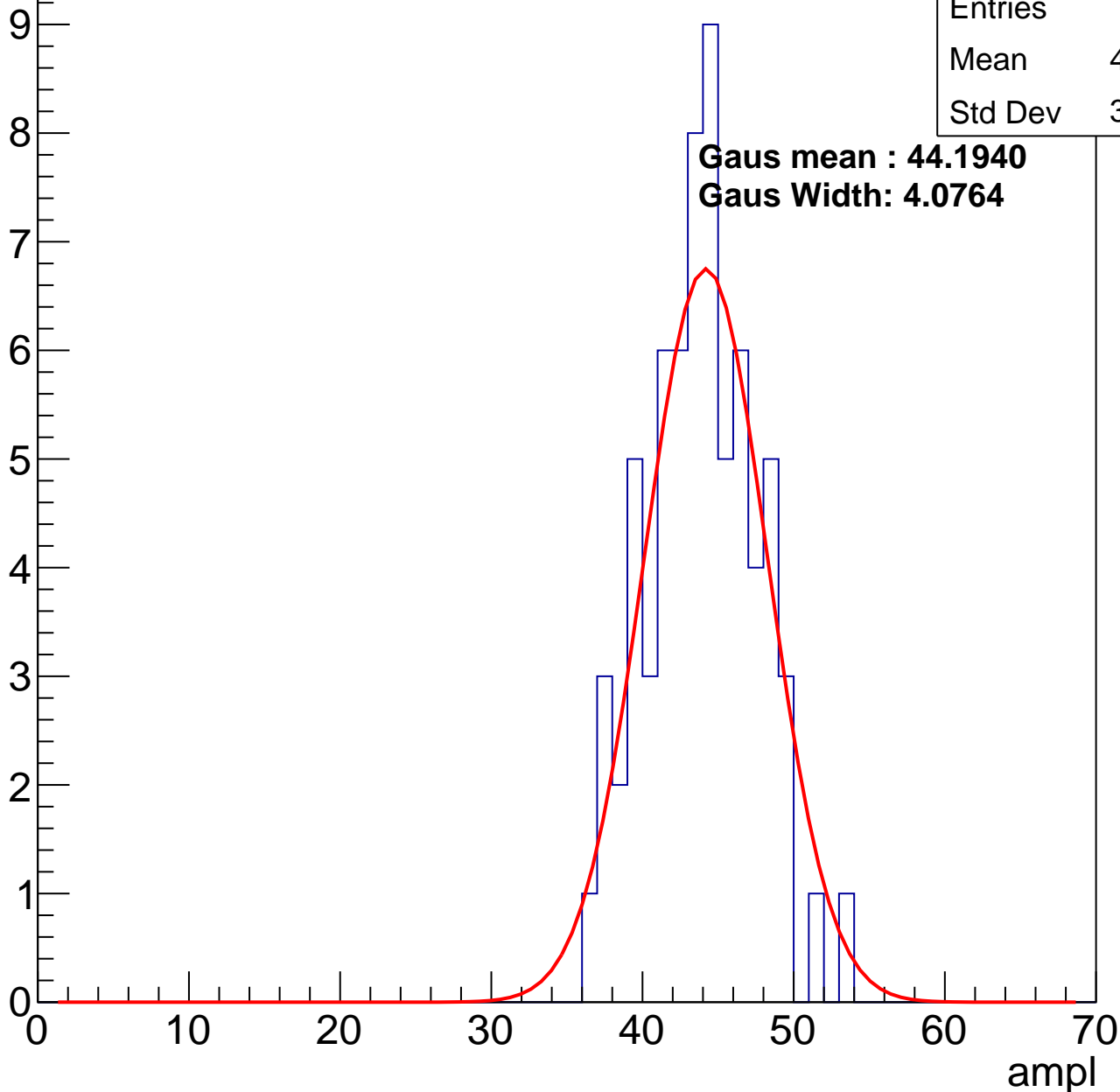
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	43.47
Std Dev	3.583

**Gaus mean : 44.1940**

**Gaus Width: 4.0764**

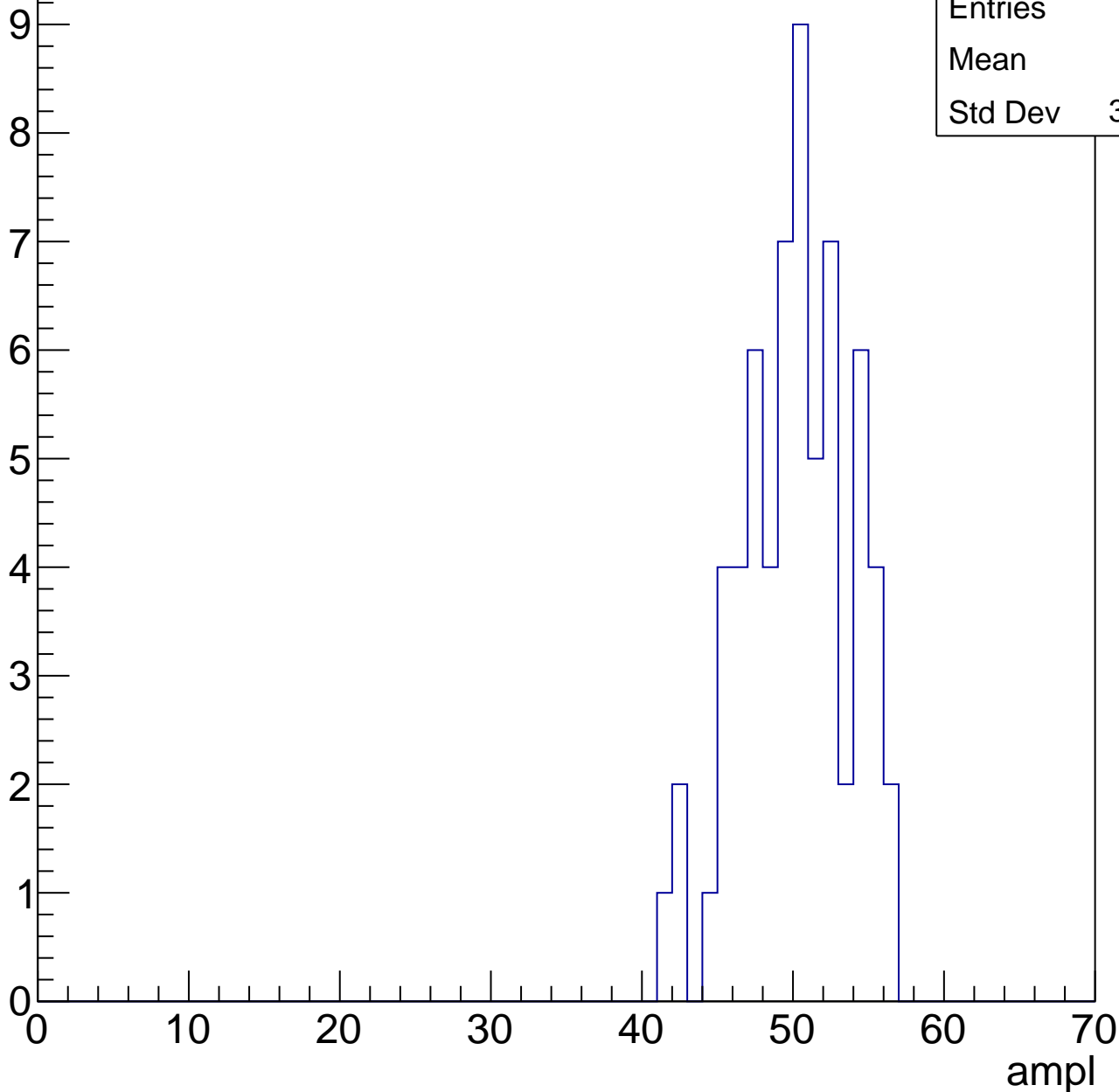


# B1L101S, U11-ch8, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

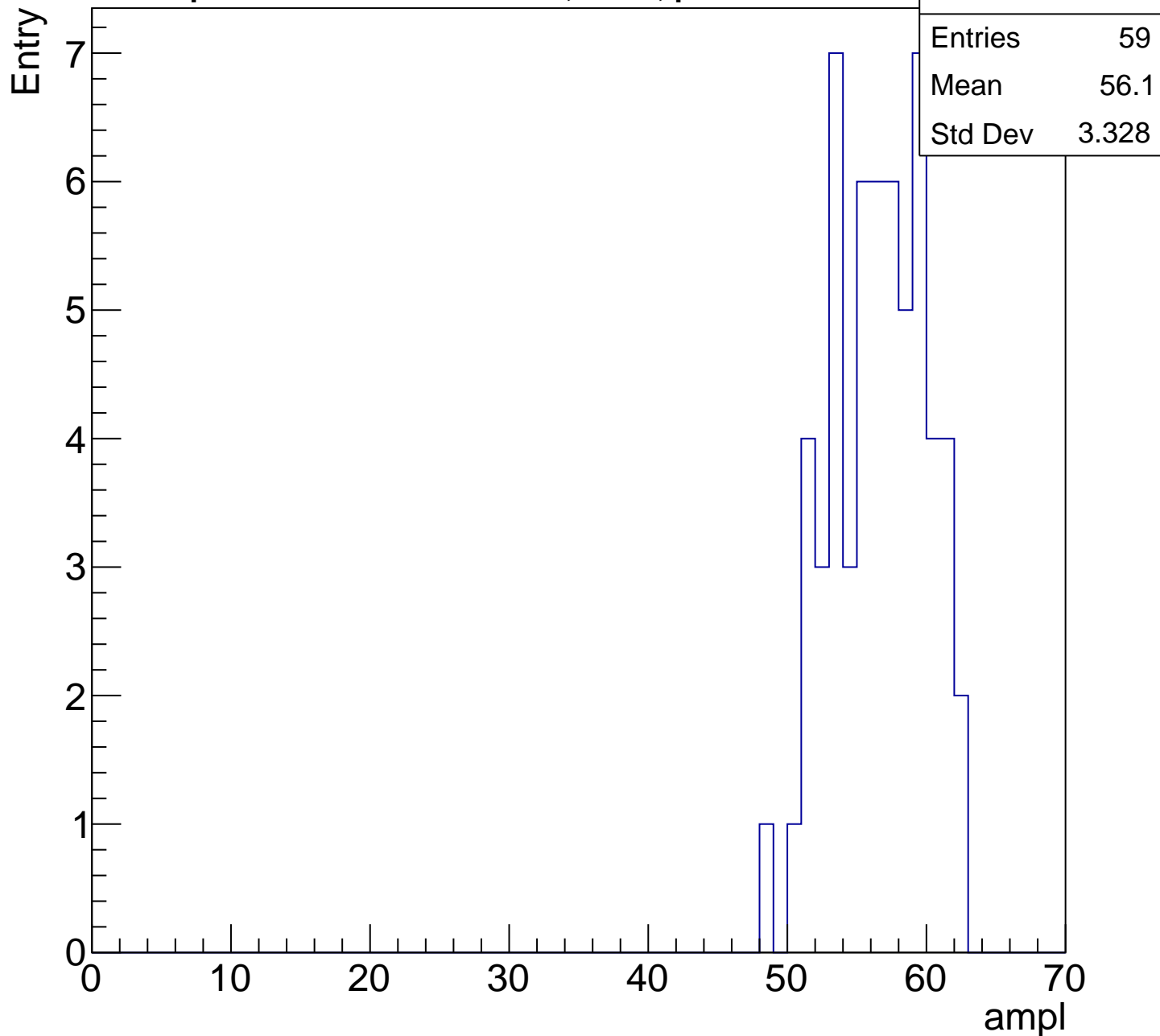
Entry

Entries	64
Mean	49.7
Std Dev	3.534



# B1L101S, U11-ch8, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U11-ch8, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

ampl

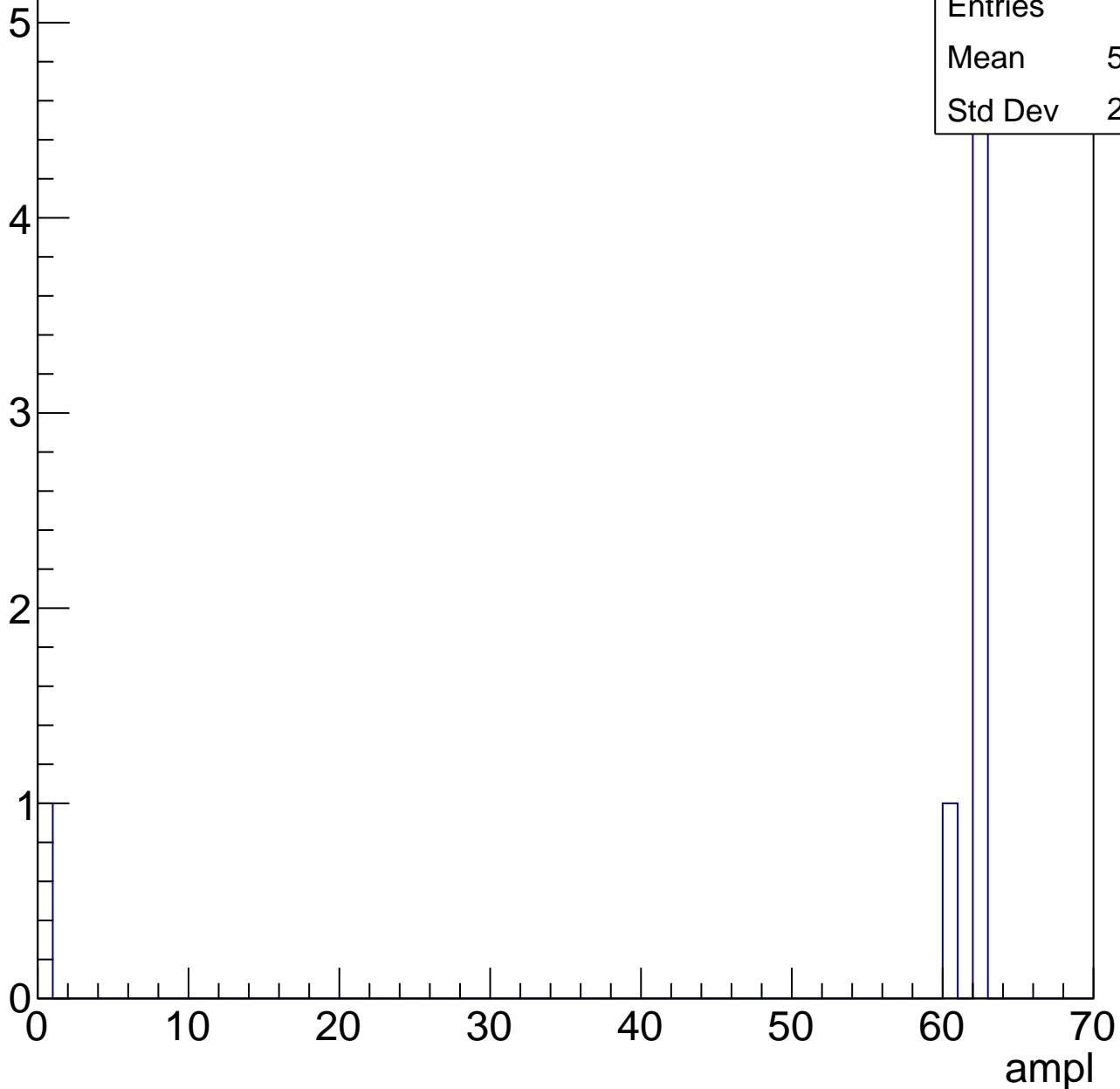
Entries	39
Mean	60.08
Std Dev	2.454

# B1L101S, U11-ch8, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	7
Mean	52.86
Std Dev	21.59





# B1L101S, U11-ch8, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U11-ch9, adc0

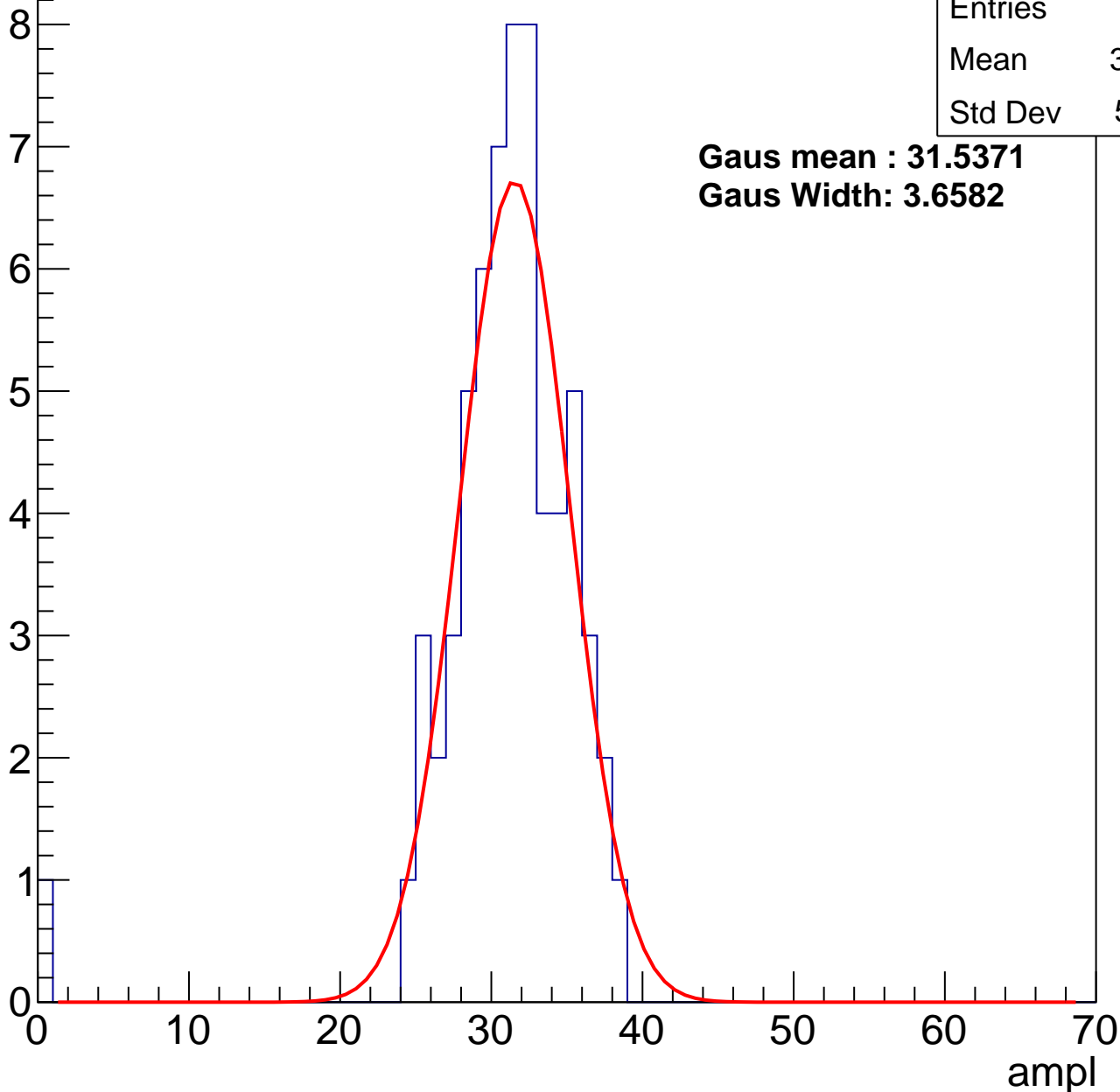
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	30.52
Std Dev	5.061

**Gaus mean : 31.5371**

**Gaus Width: 3.6582**



# B1L101S, U11-ch9, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	65
Mean	37.09
Std Dev	2.923

**Gaus mean : 37.3889**

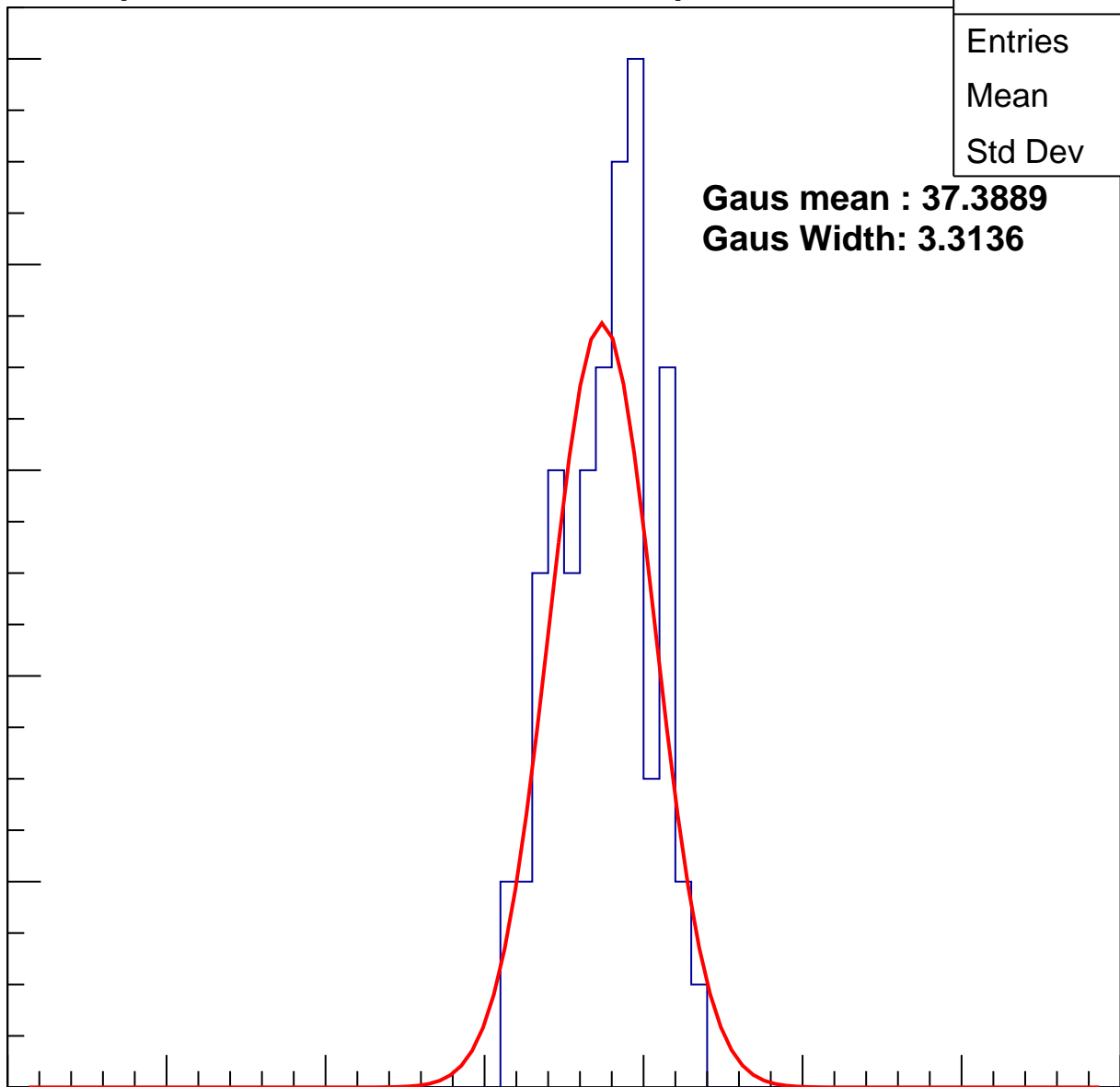
**Gaus Width: 3.3136**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

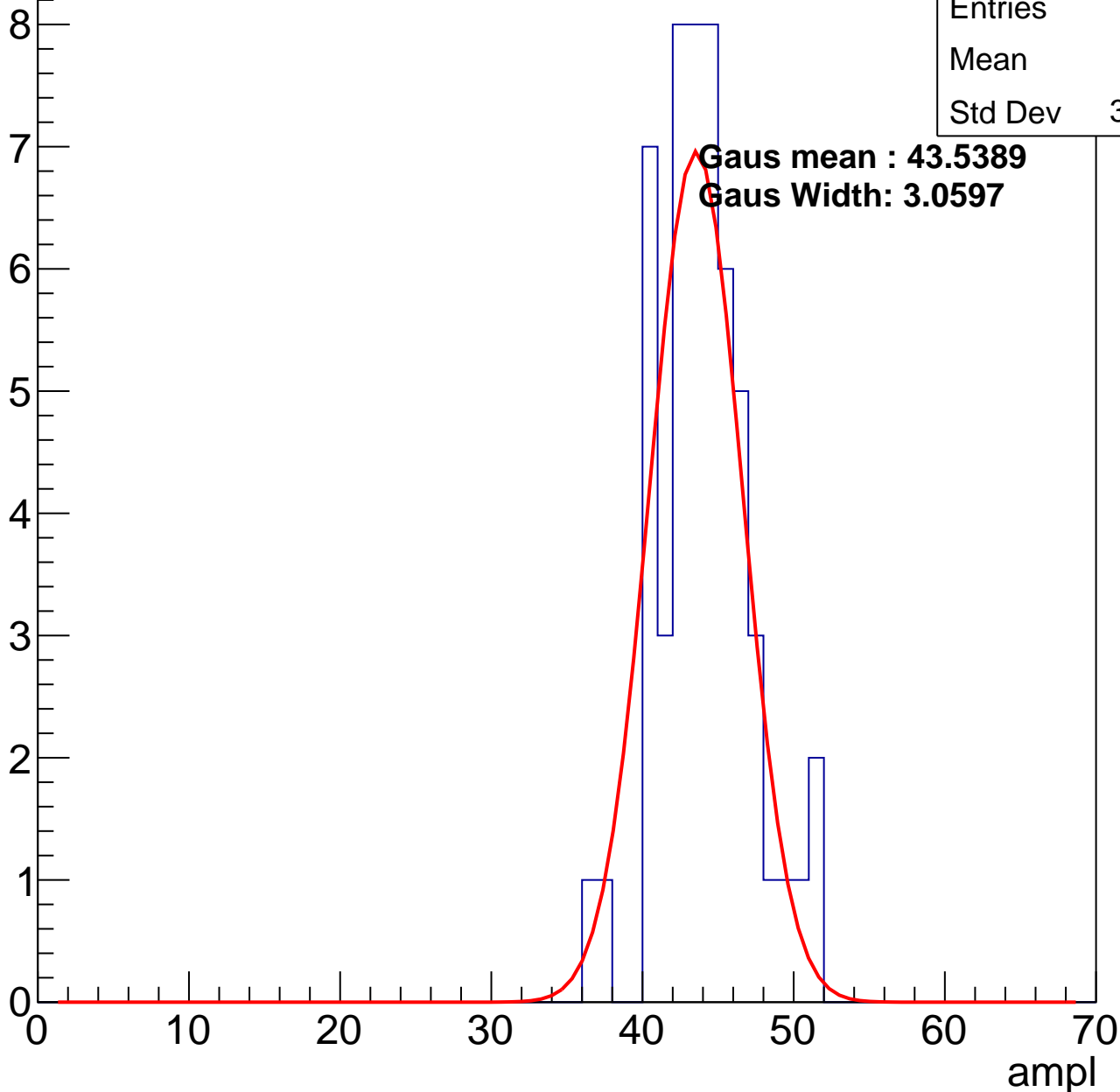


# B1L101S, U11-ch9, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

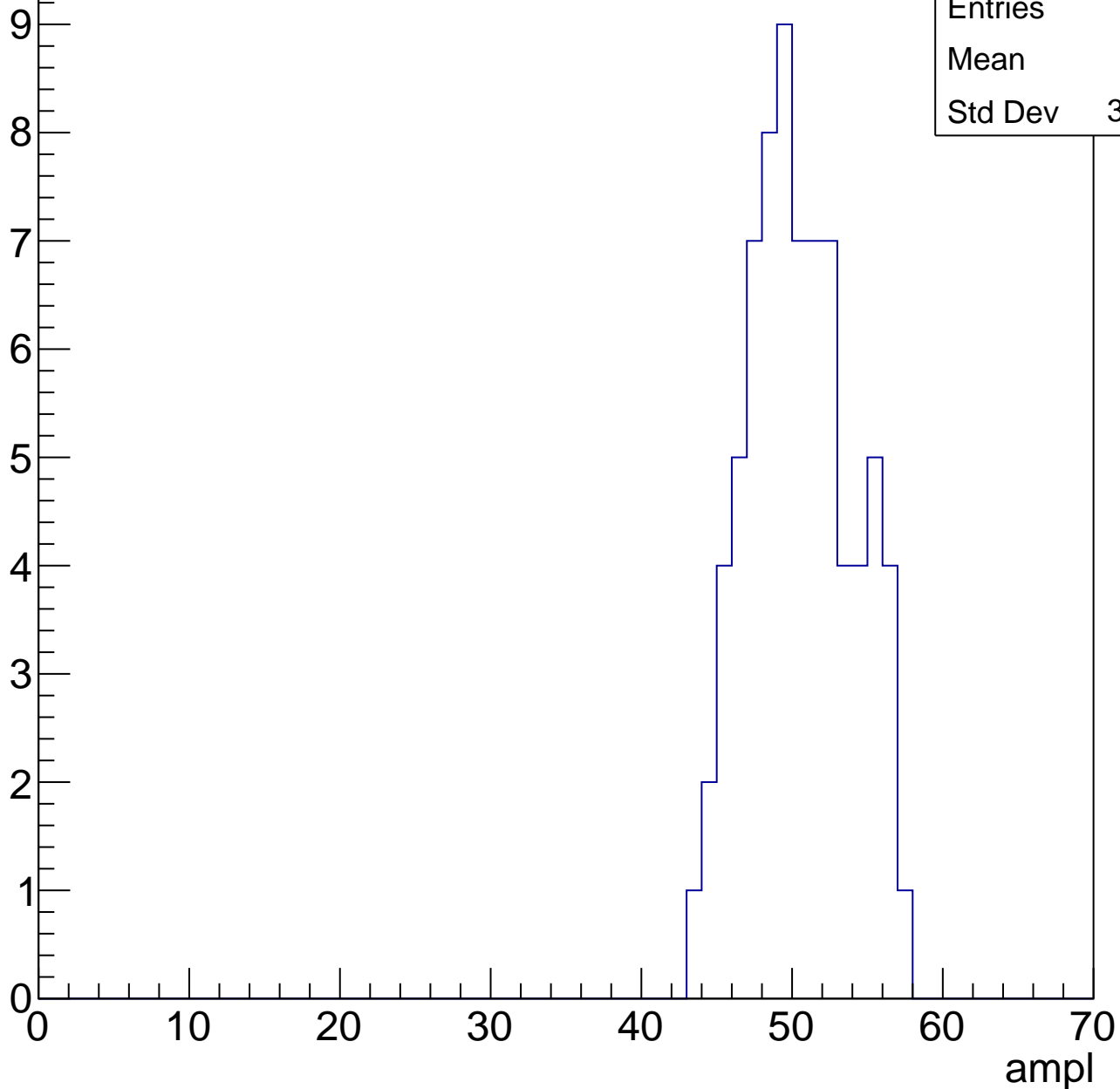
Entries	55
Mean	43.6
Std Dev	3.049



# B1L101S, U11-ch9, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

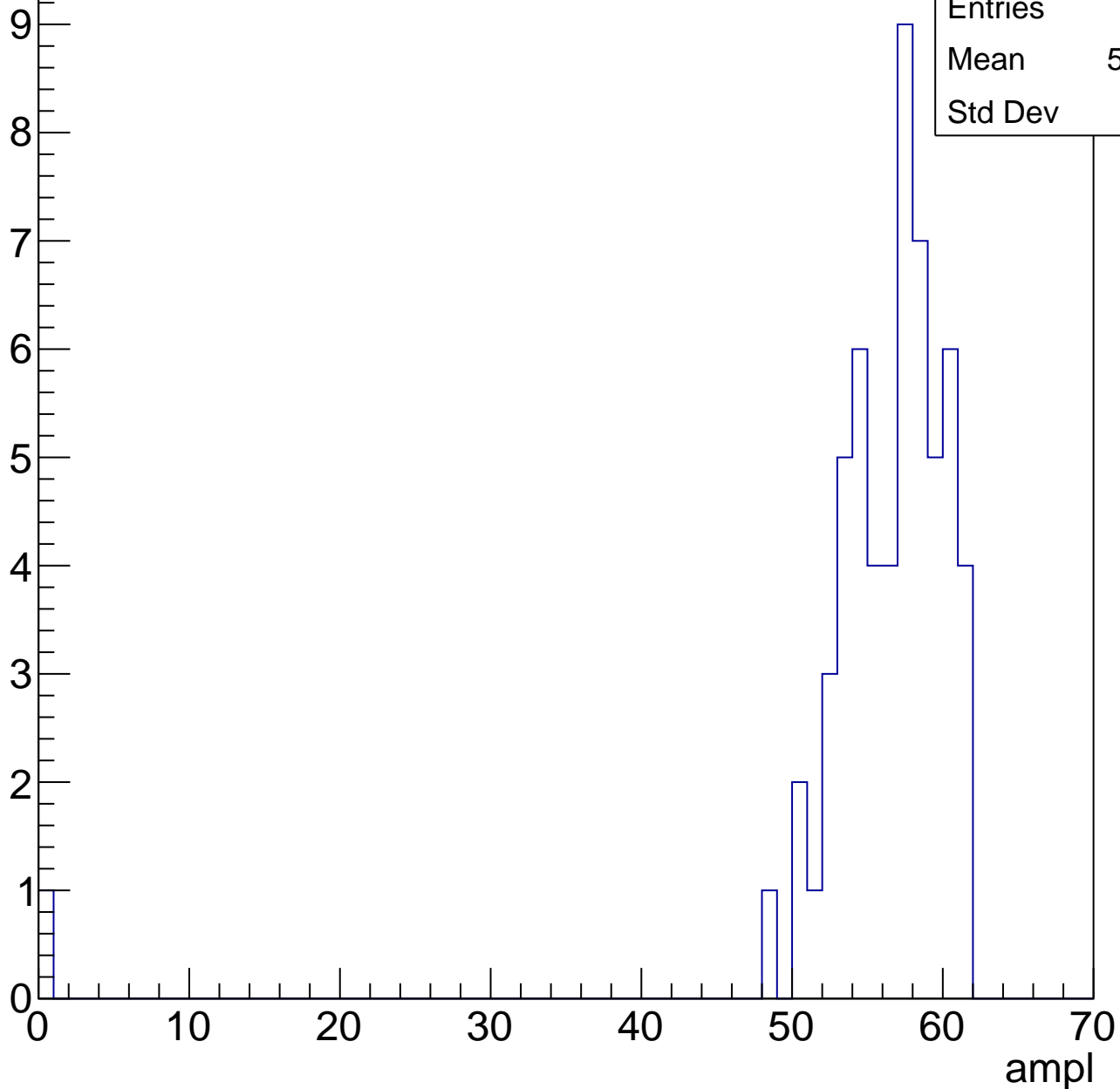


Entries	75
Mean	50
Std Dev	3.382

# B1L101S, U11-ch9, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



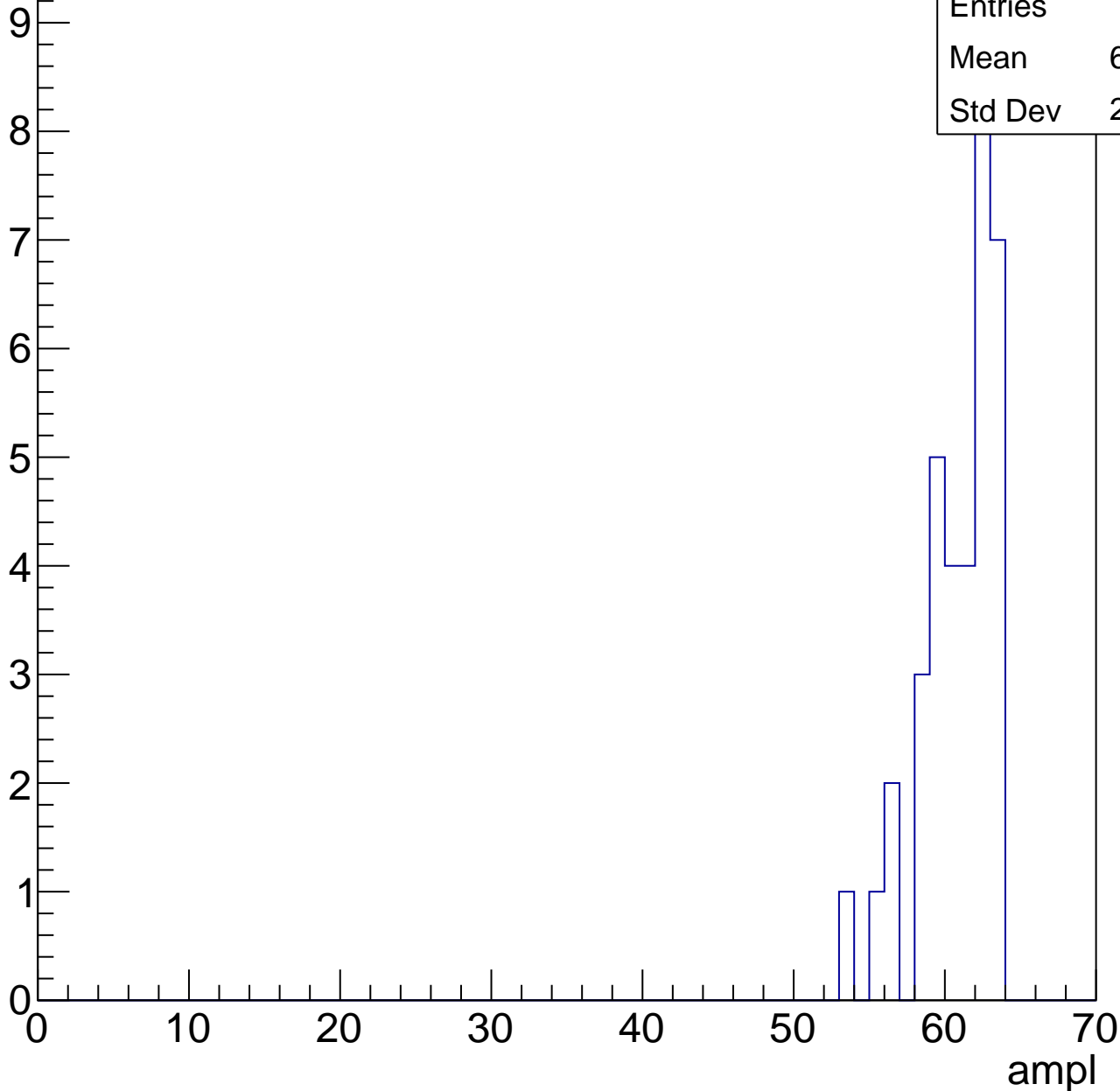
Entries	58
Mean	55.28
Std Dev	7.95

# B1L101S, U11-ch9, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

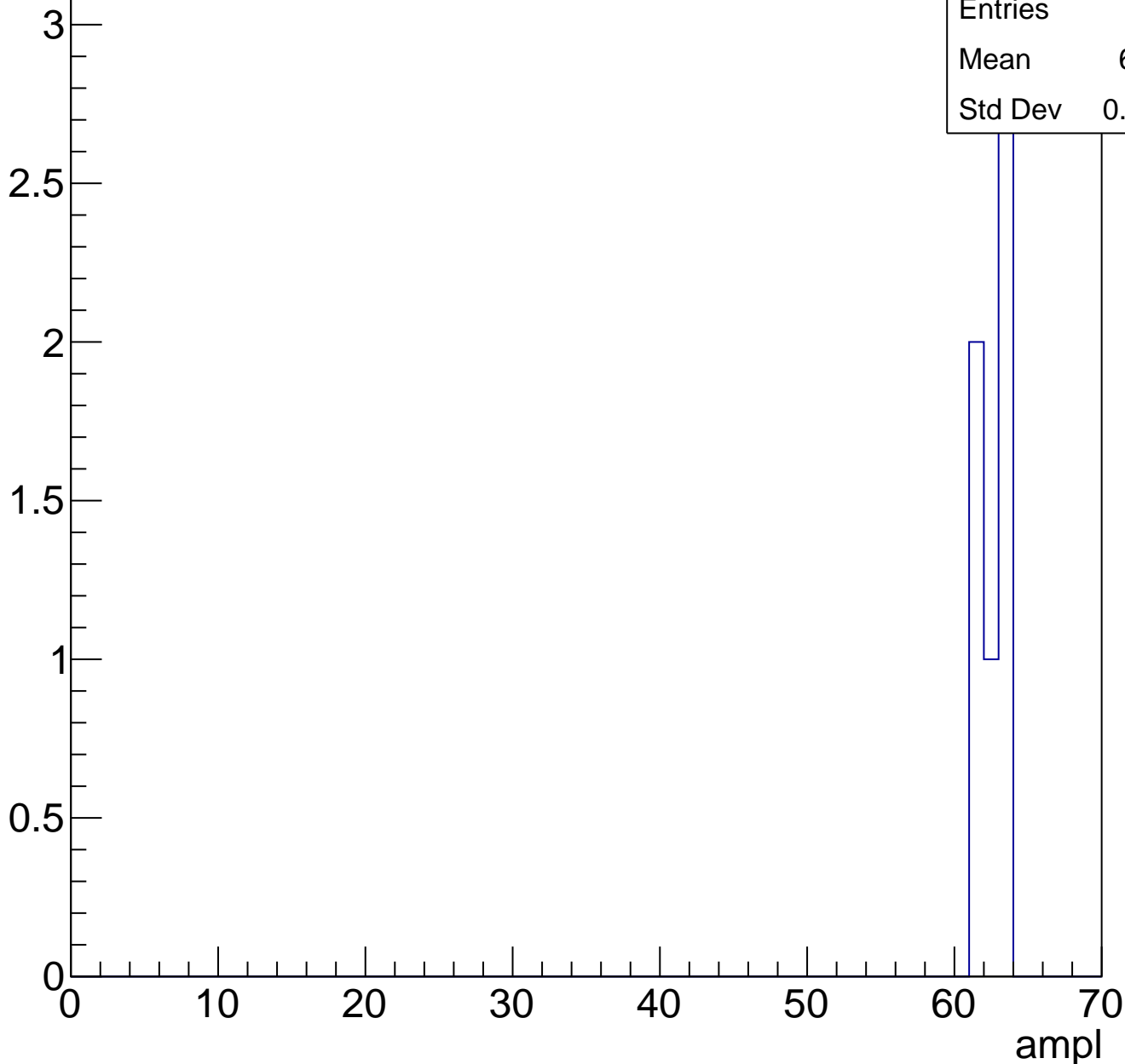
Entries	36
Mean	60.33
Std Dev	2.483



# B1L101S, U11-ch9, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch9, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U11-ch10, adc0

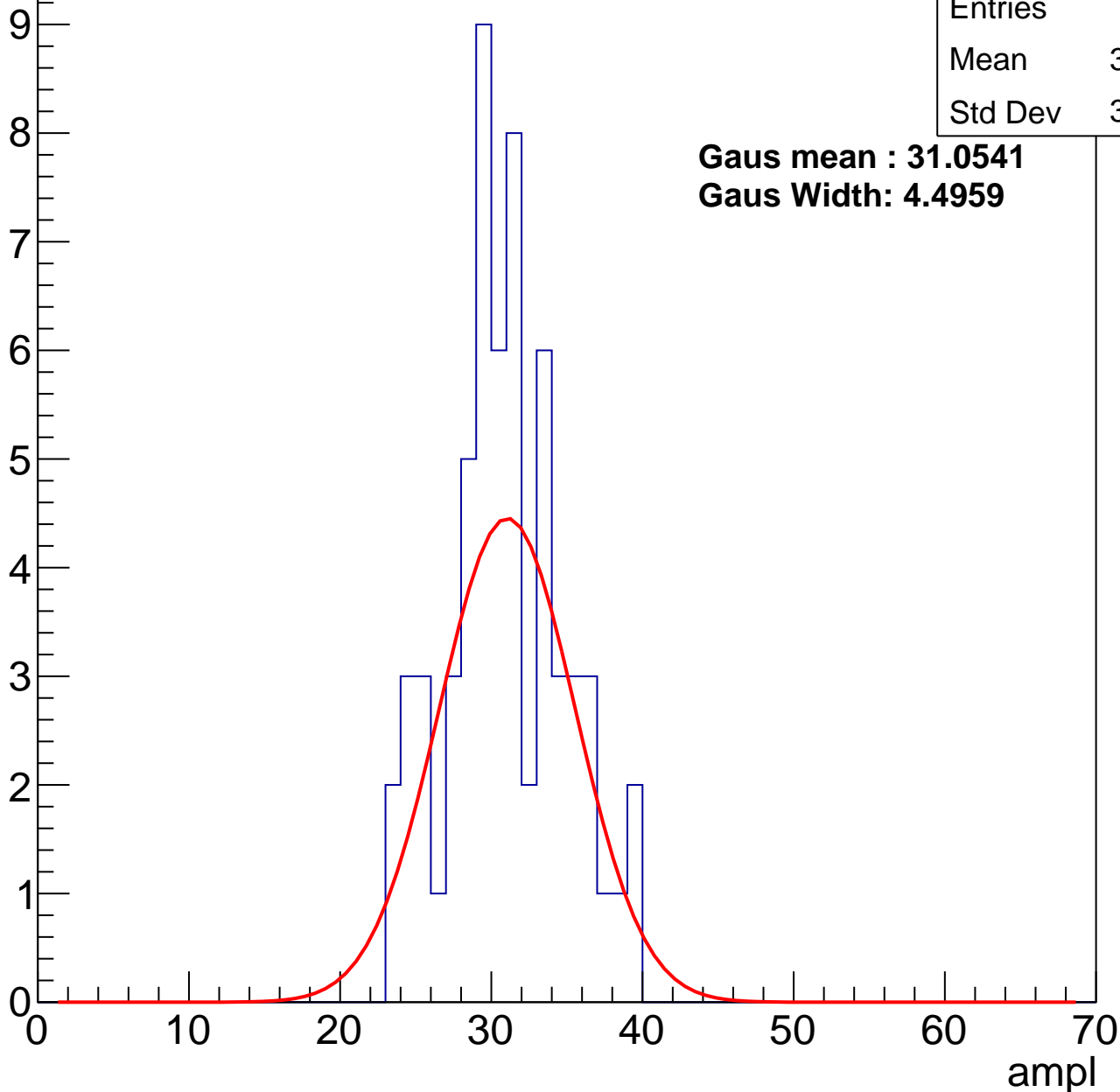
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	30.48
Std Dev	3.873

**Gaus mean : 31.0541**

**Gaus Width: 4.4959**



# B1L101S, U11-ch10, adc1

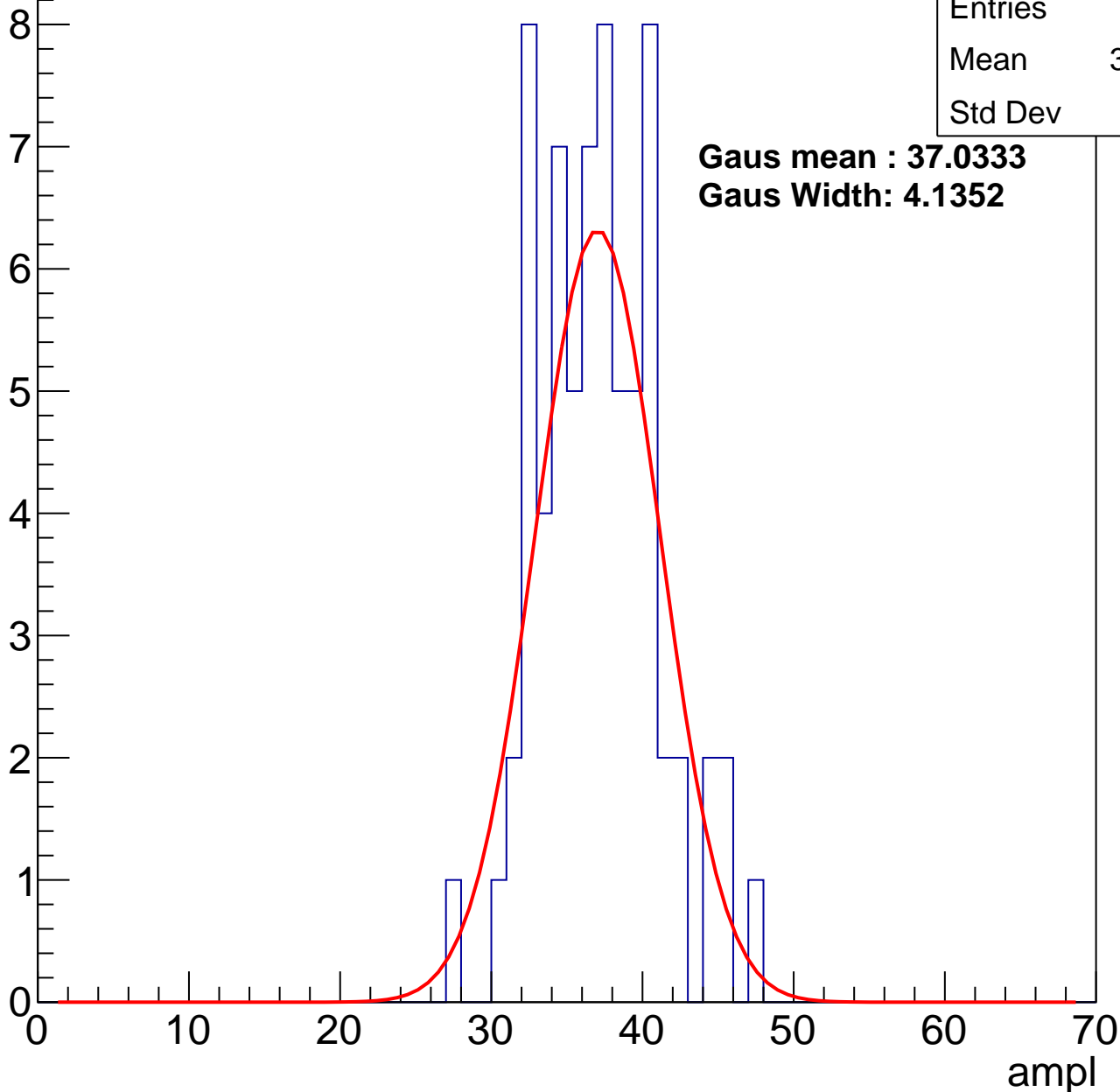
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	36.63
Std Dev	3.91

**Gaus mean : 37.0333**

**Gaus Width: 4.1352**



# B1L101S, U11-ch10, adc2

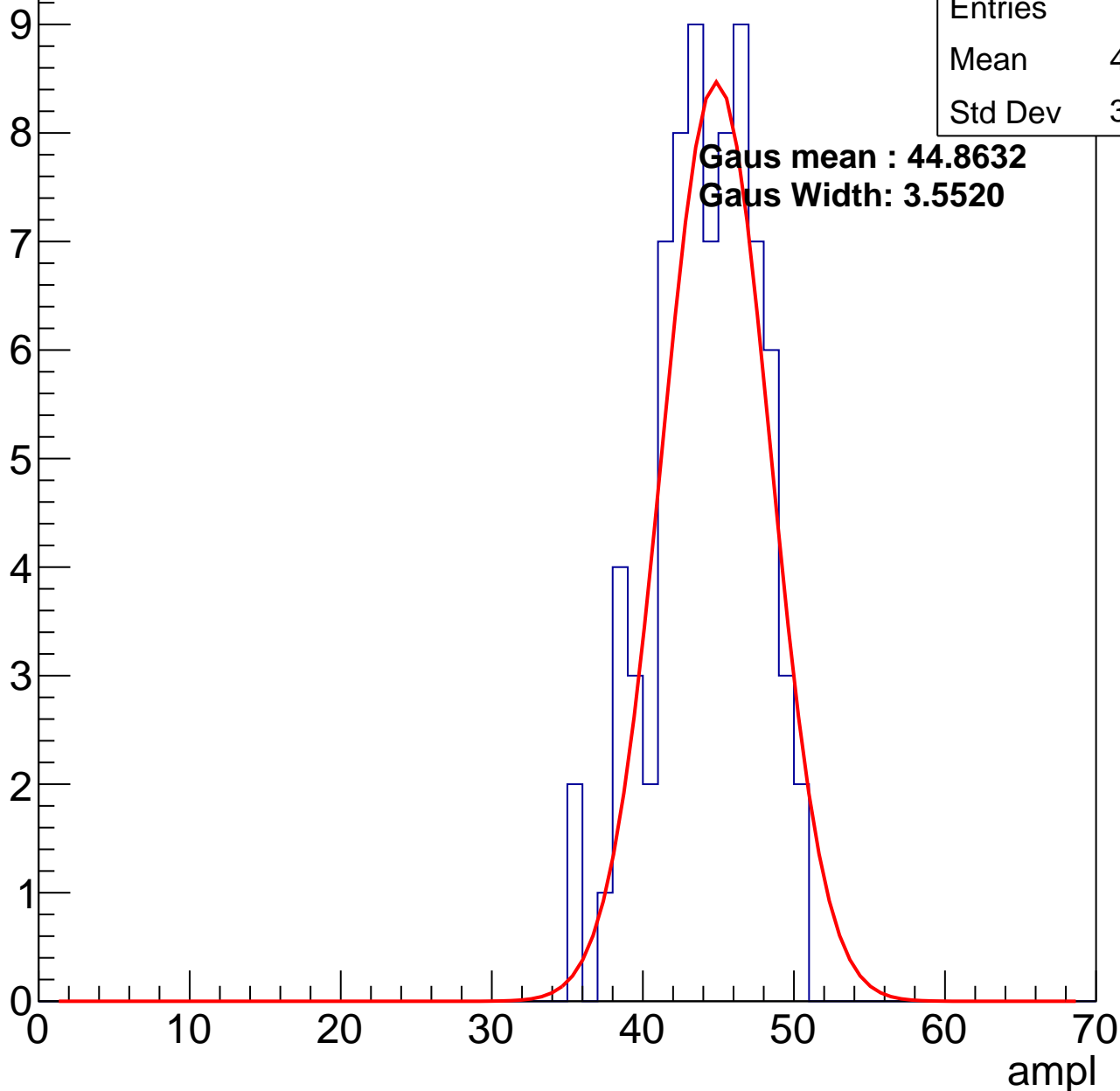
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	78
Mean	43.74
Std Dev	3.417

**Gaus mean : 44.8632**

**Gaus Width: 3.5520**

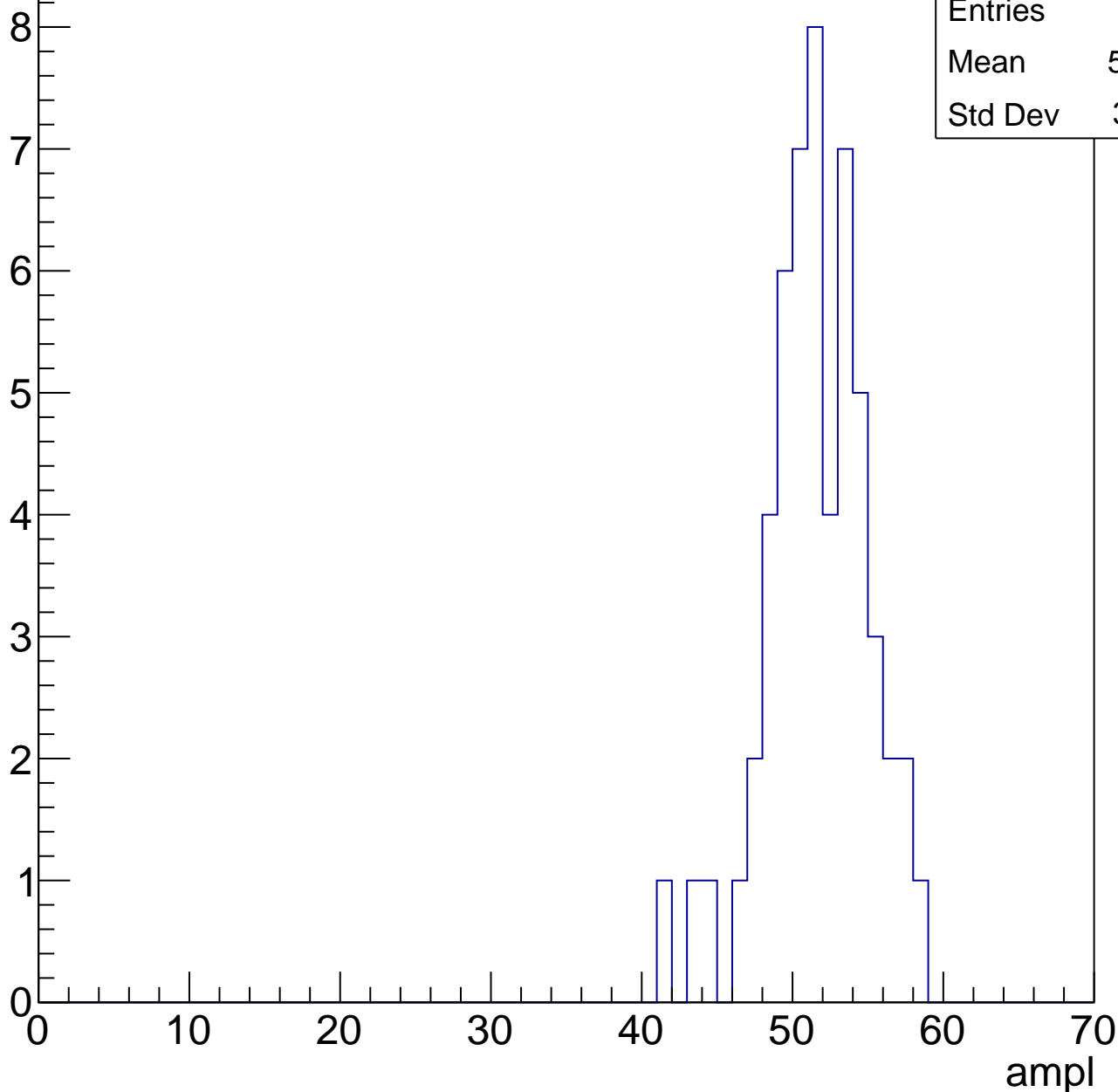


# B1L101S, U11-ch10, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

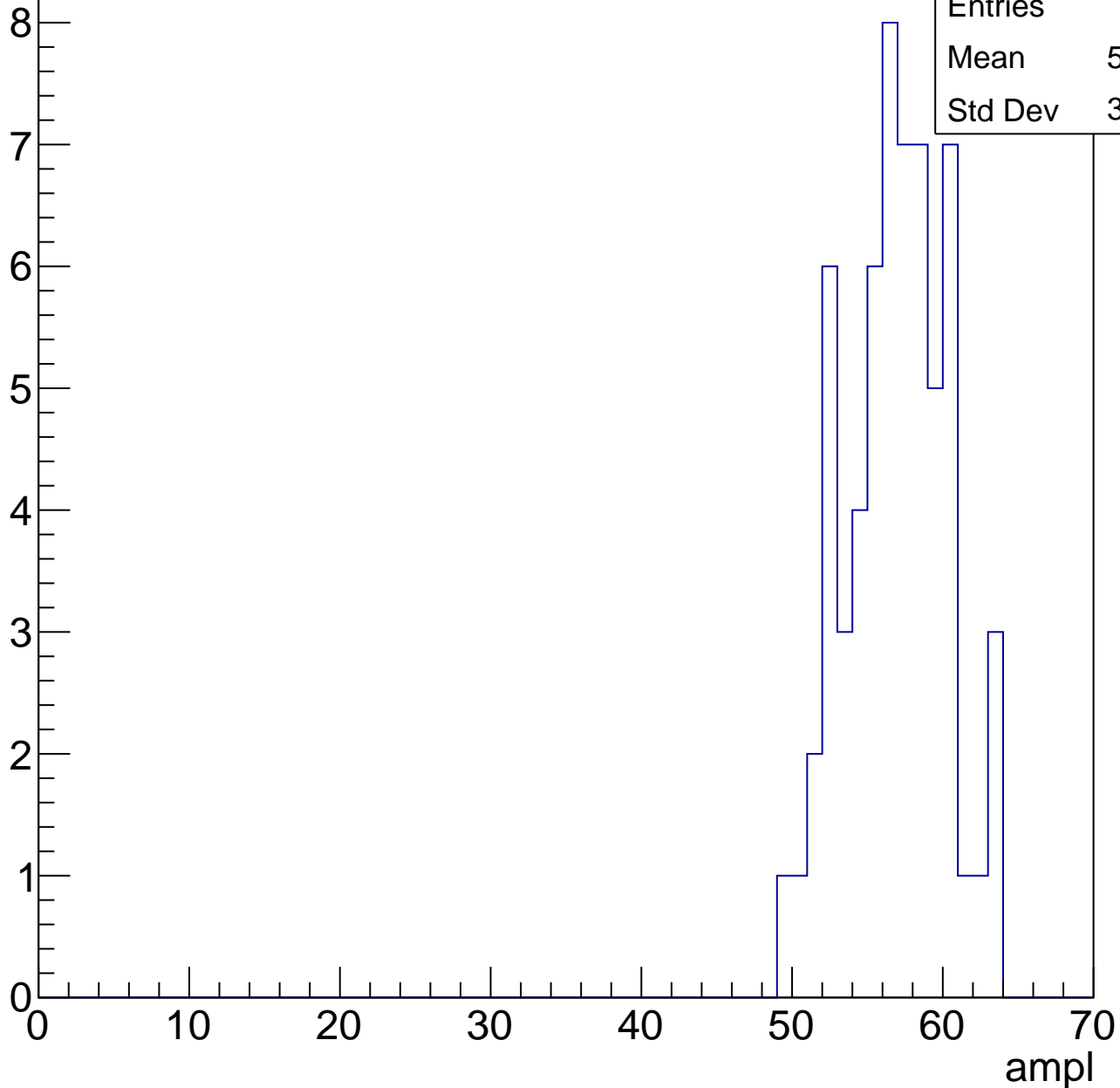
Entries	55
Mean	51.09
Std Dev	3.391



# B1L101S, U11-ch10, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



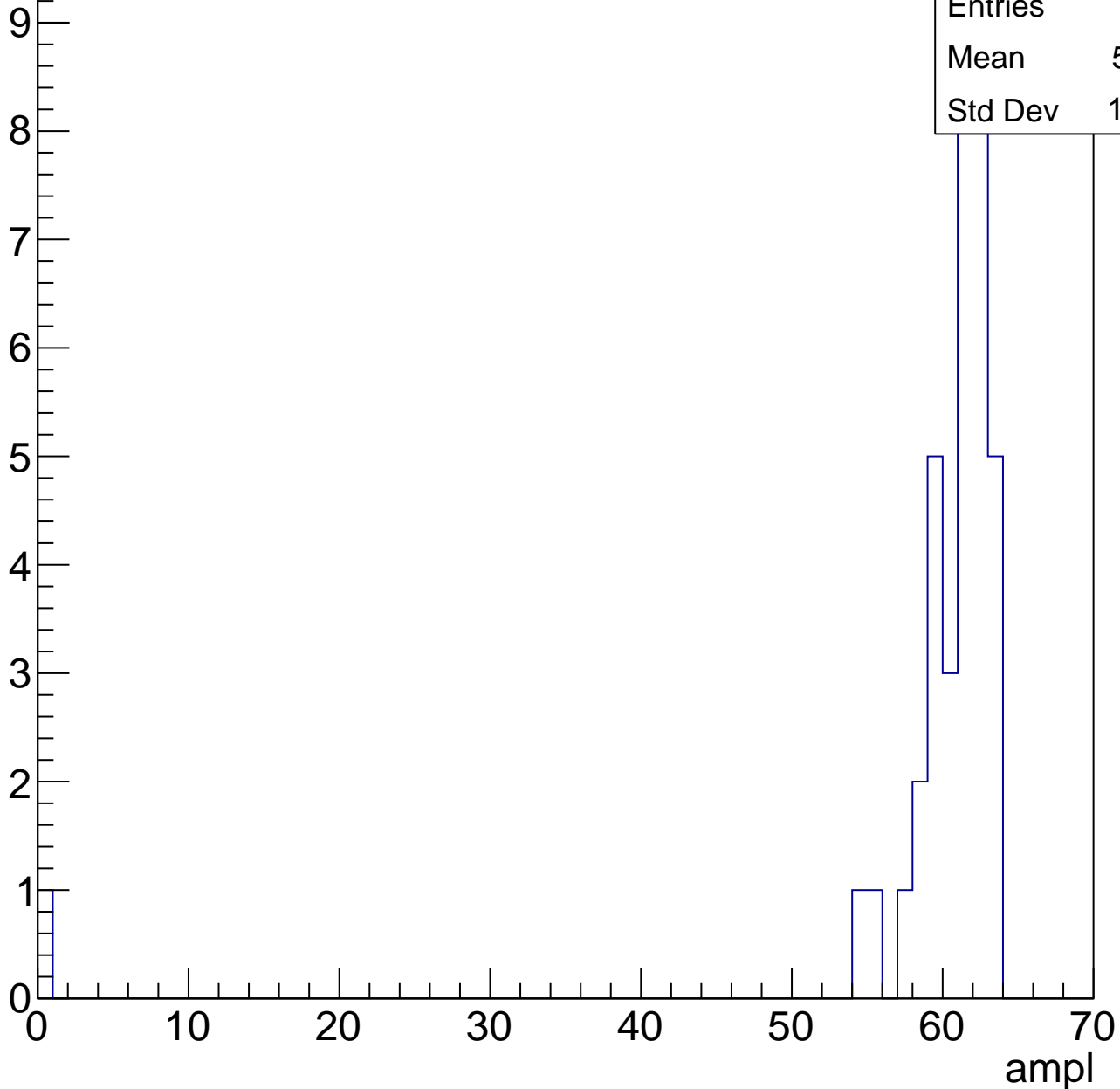
Entries	62
Mean	56.42
Std Dev	3.285

# B1L101S, U11-ch10, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	36
Mean	58.81
Std Dev	10.16



# B1L101S, U11-ch10, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch10, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	11.5
Std Dev	11.5

# B1L101S, U11-ch11, adc0

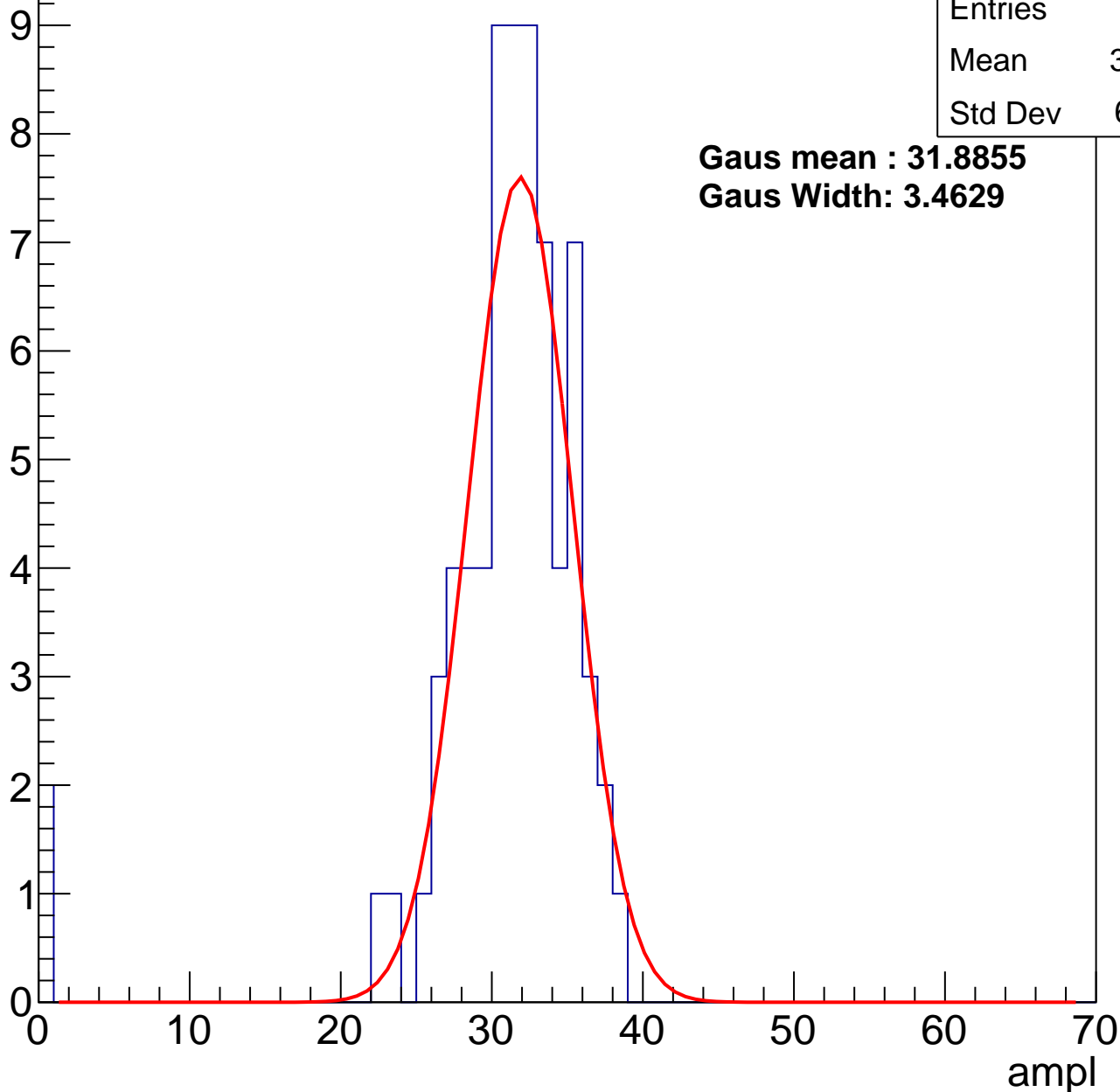
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	30.32
Std Dev	6.111

**Gaus mean : 31.8855**

**Gaus Width: 3.4629**



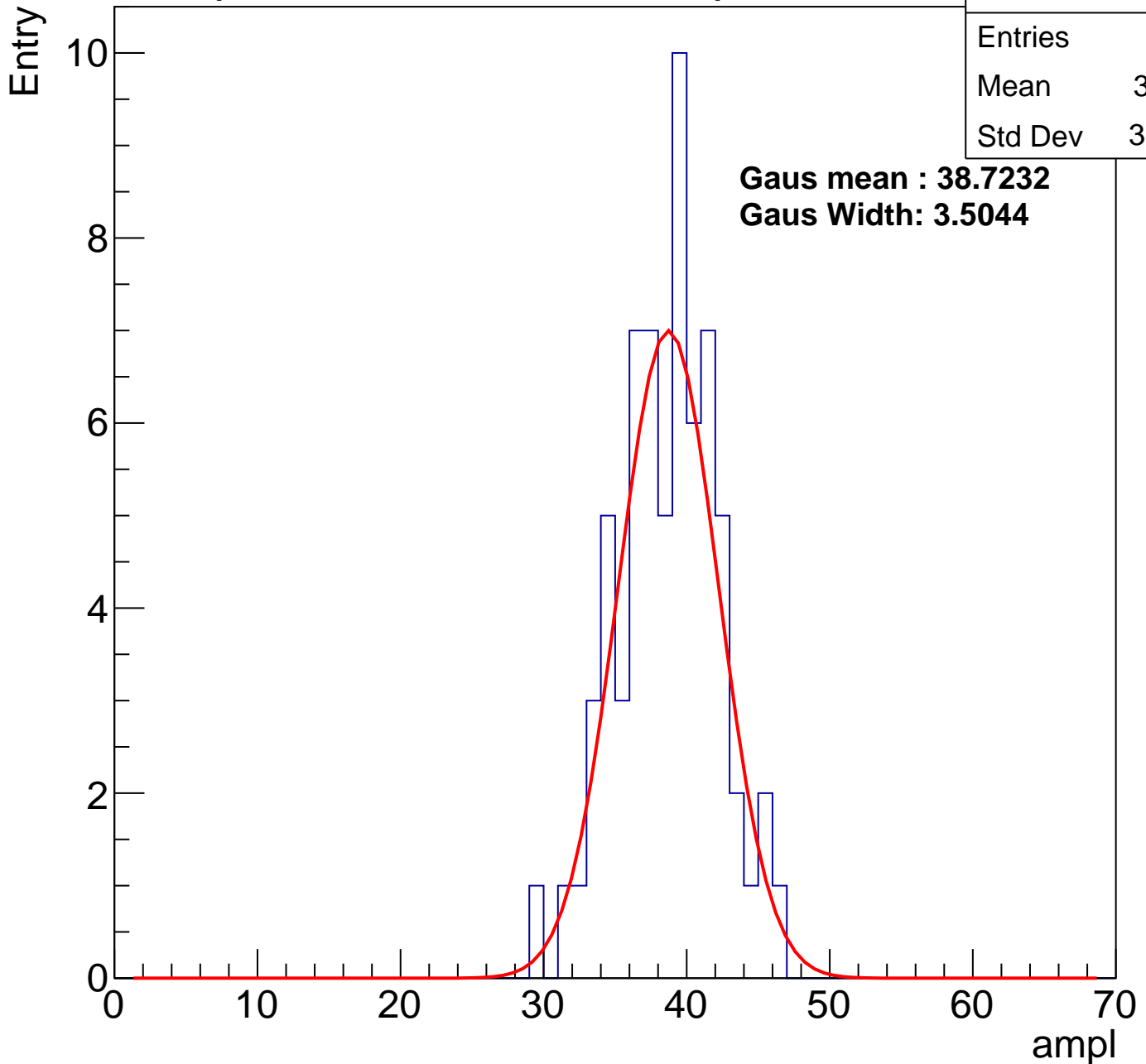
# B1L101S, U11-ch11, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	67
Mean	38.21
Std Dev	3.466

**Gaus mean : 38.7232**

**Gaus Width: 3.5044**



# B1L101S, U11-ch11, adc2

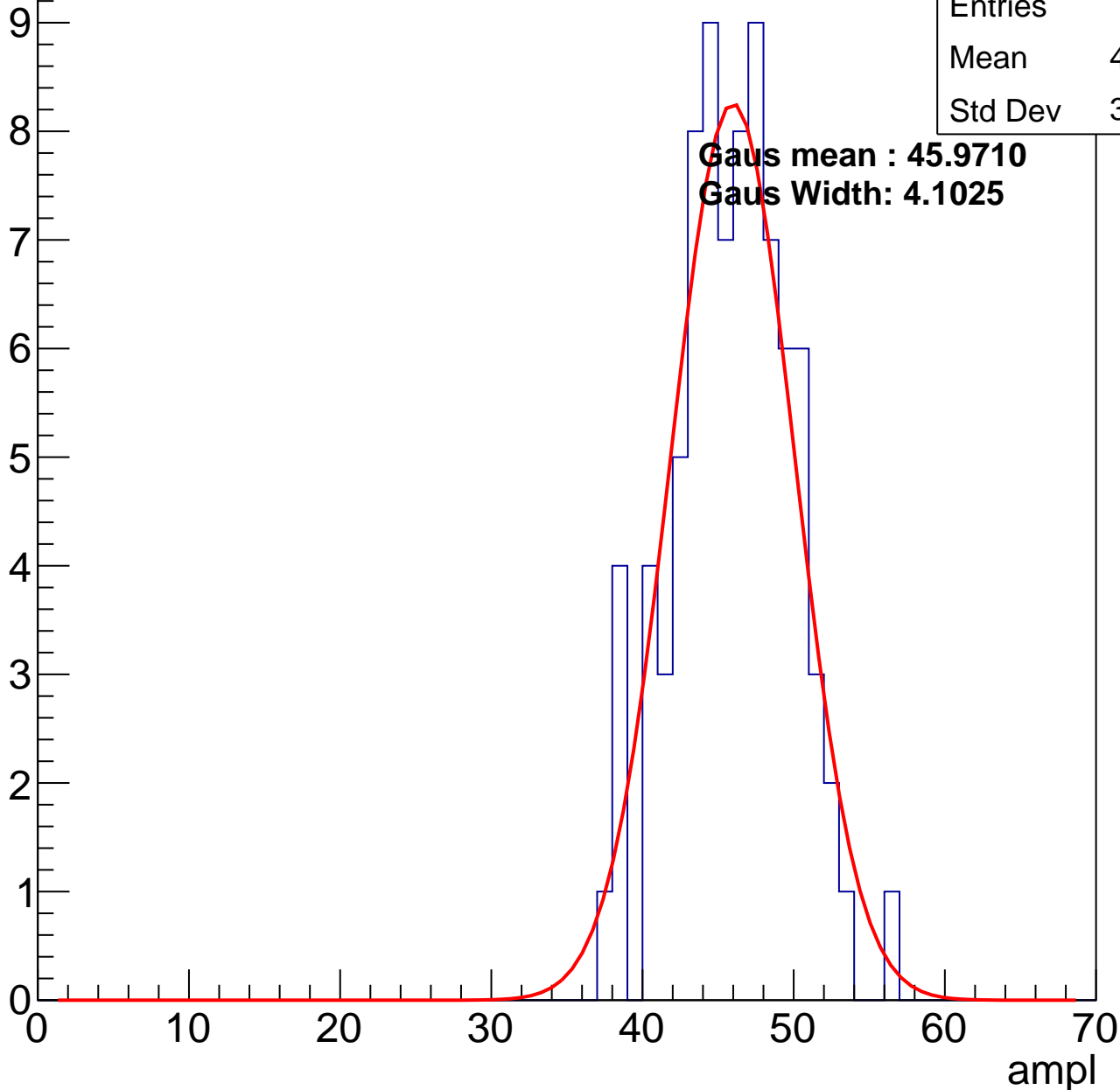
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	84
Mean	45.52
Std Dev	3.803

**Gaus mean : 45.9710**

**Gaus Width: 4.1025**

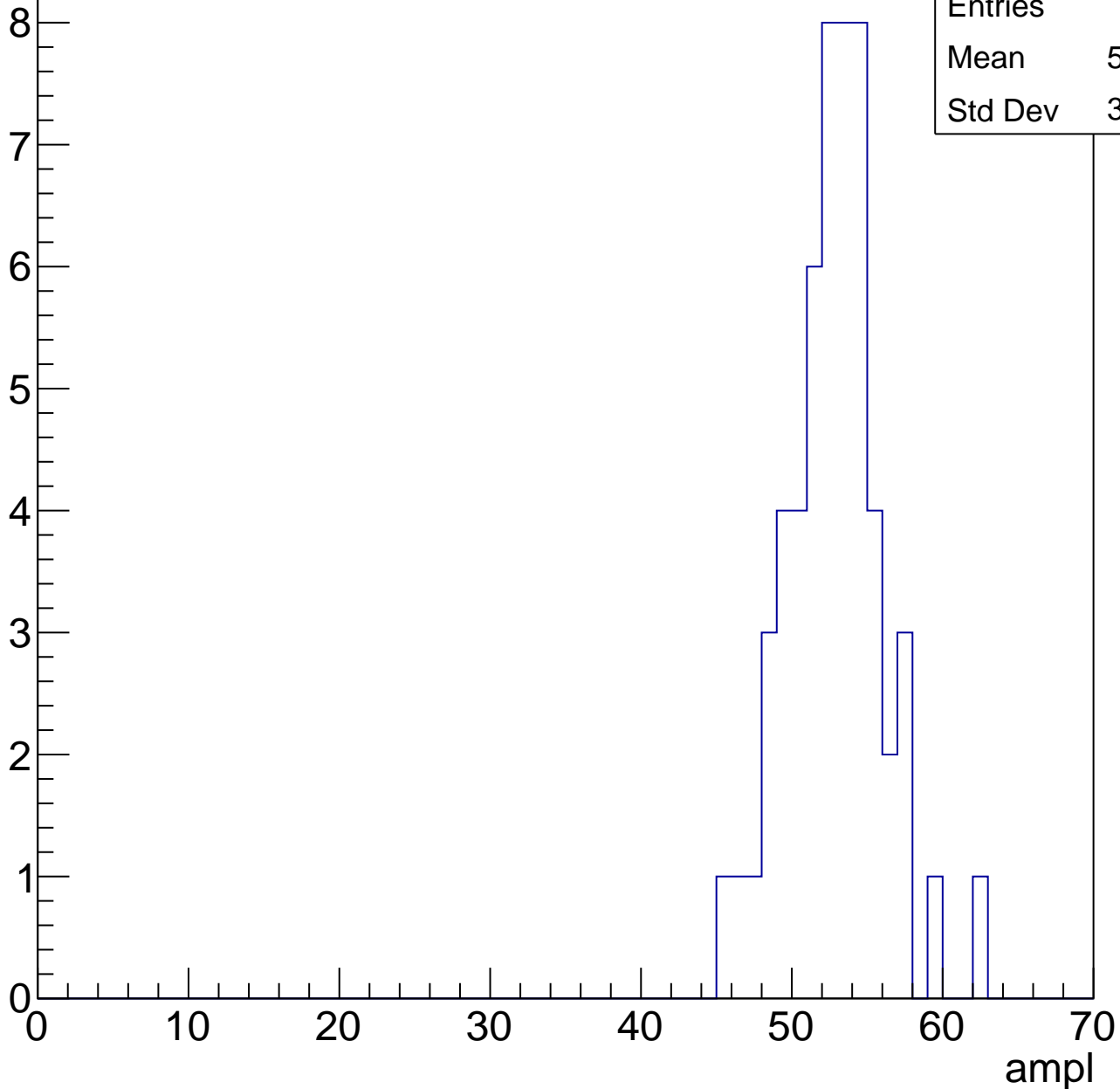


# B1L101S, U11-ch11, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	52.36
Std Dev	3.136

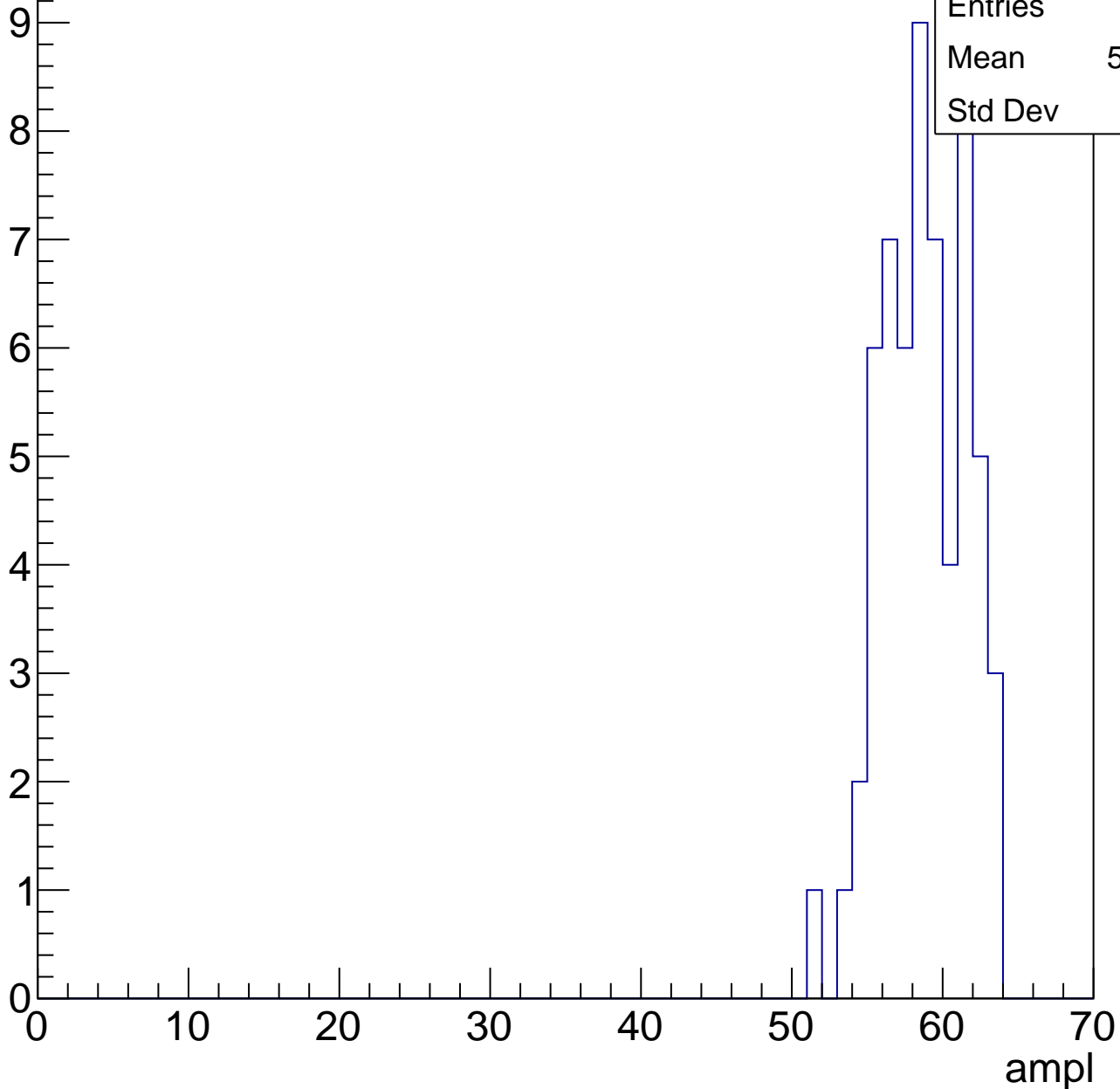


# B1L101S, U11-ch11, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	58.27
Std Dev	2.73

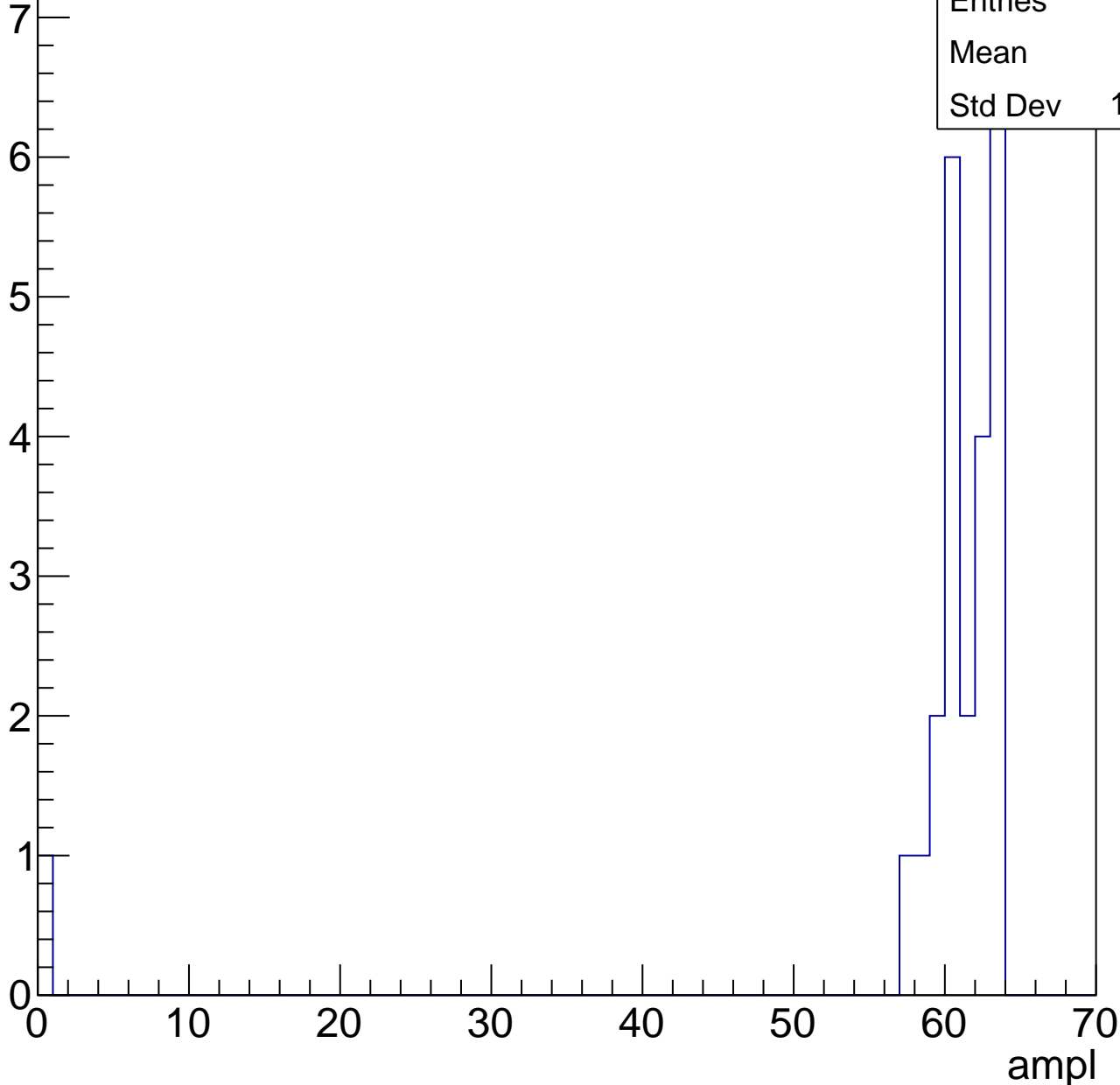


# B1L101S, U11-ch11, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	24
Mean	58.5
Std Dev	12.32



# B1L101S, U11-ch11, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L101S, U11-ch11, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U11-ch12, adc0

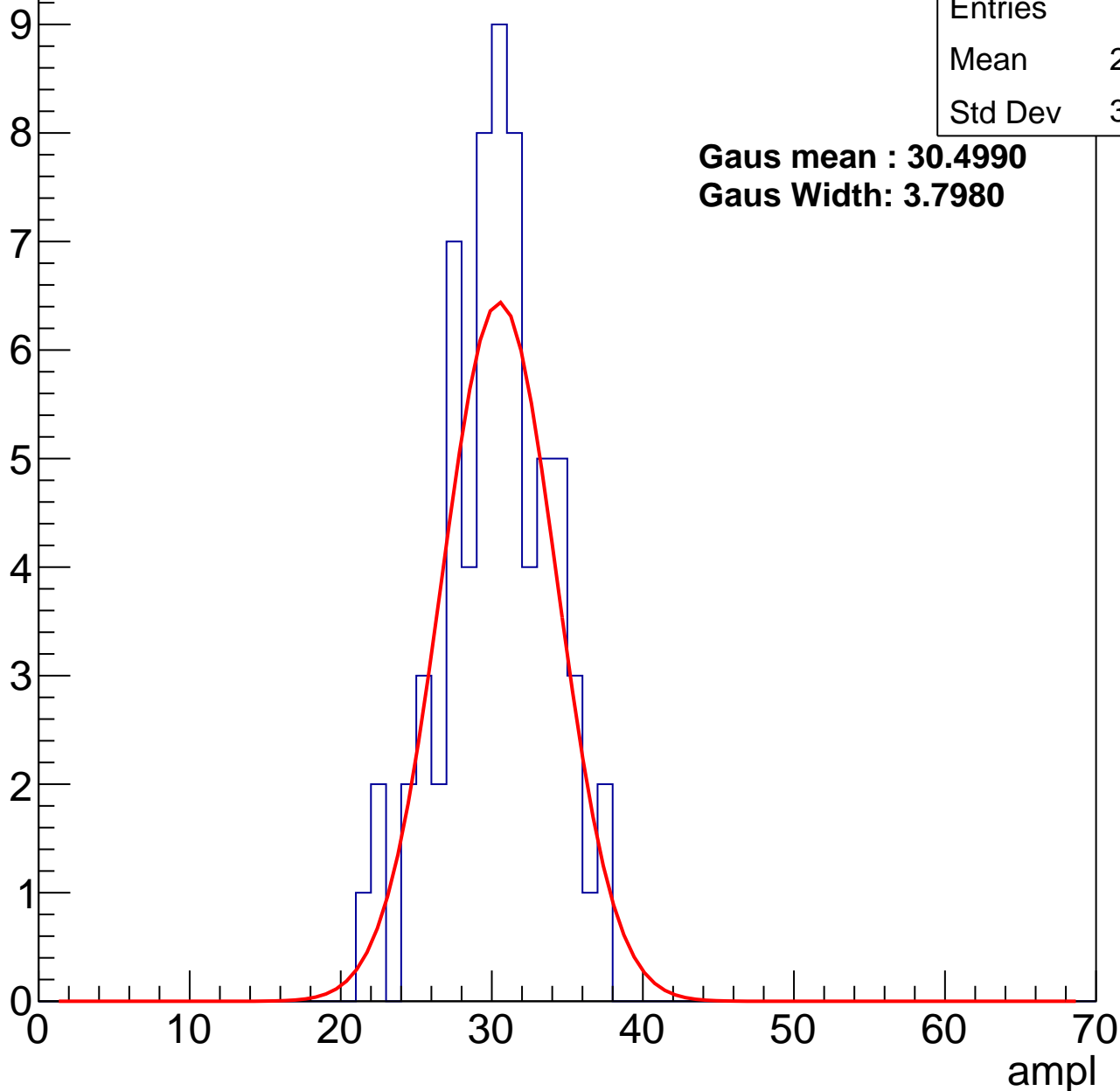
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	29.83
Std Dev	3.549

**Gaus mean : 30.4990**

**Gaus Width: 3.7980**



# B1L101S, U11-ch12, adc1

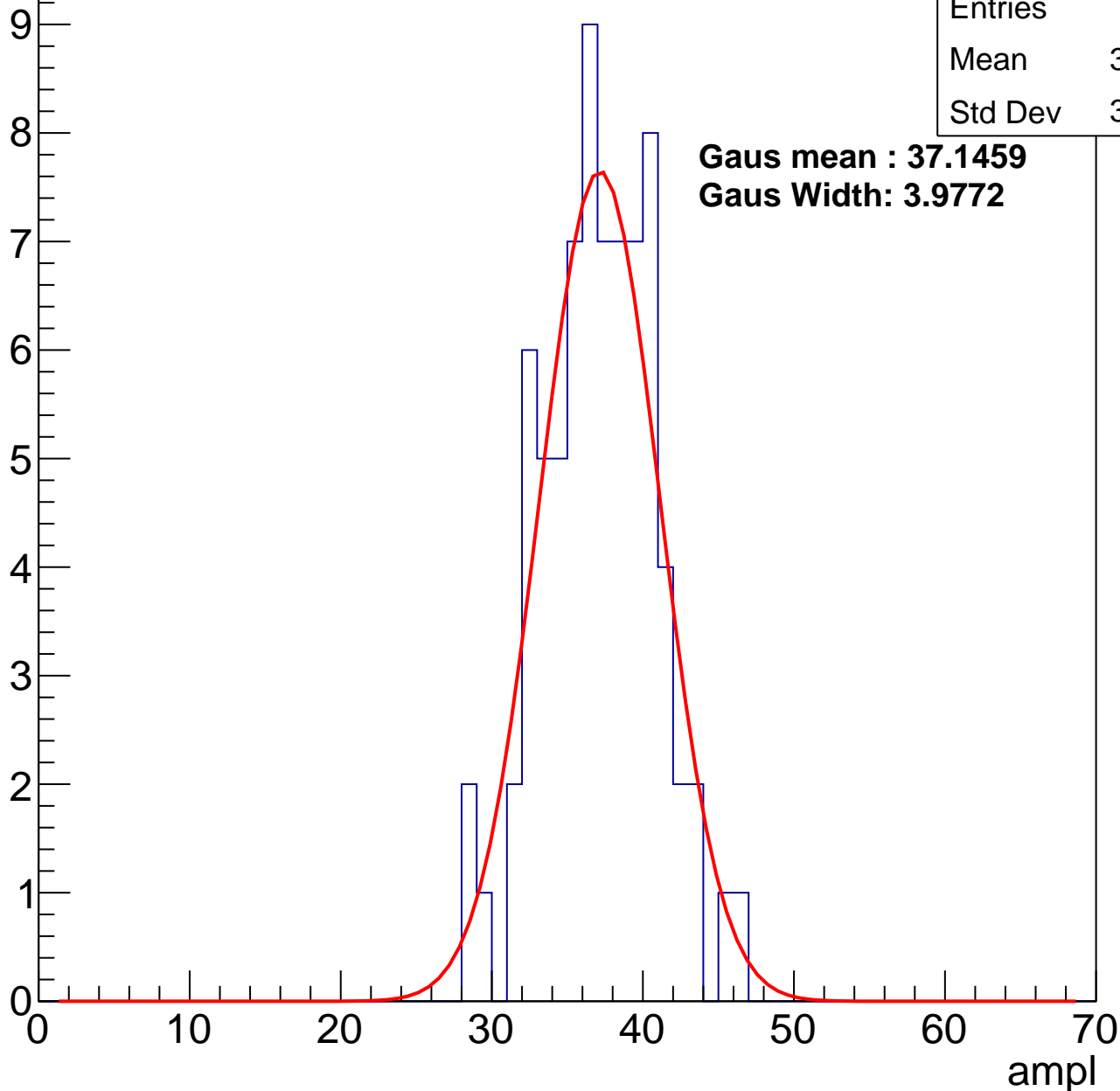
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	36.66
Std Dev	3.698

**Gaus mean : 37.1459**

**Gaus Width: 3.9772**



# B1L101S, U11-ch12, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	76
Mean	44.42
Std Dev	3.522

**Gaus mean : 44.9680**

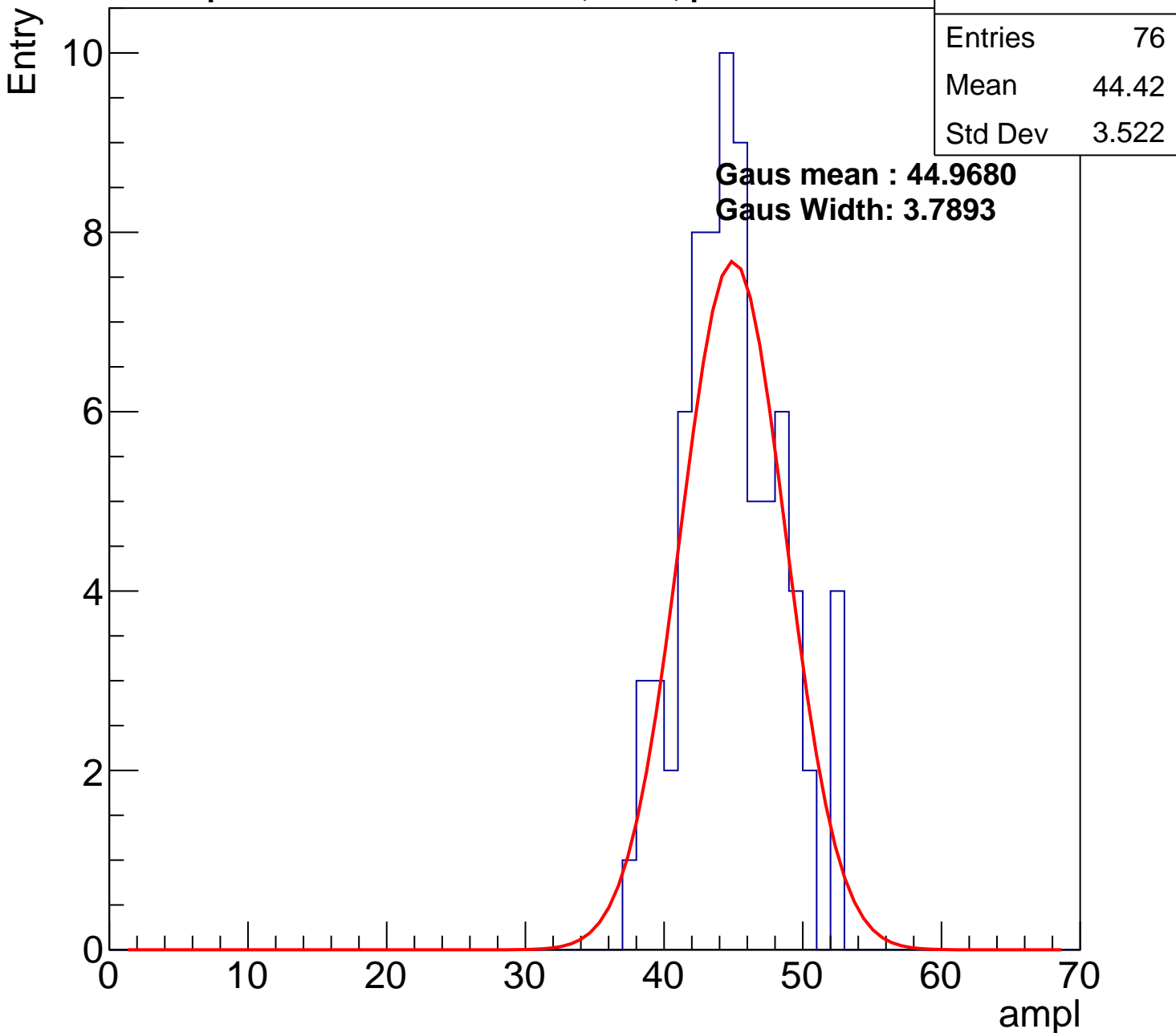
**Gaus Width: 3.7893**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

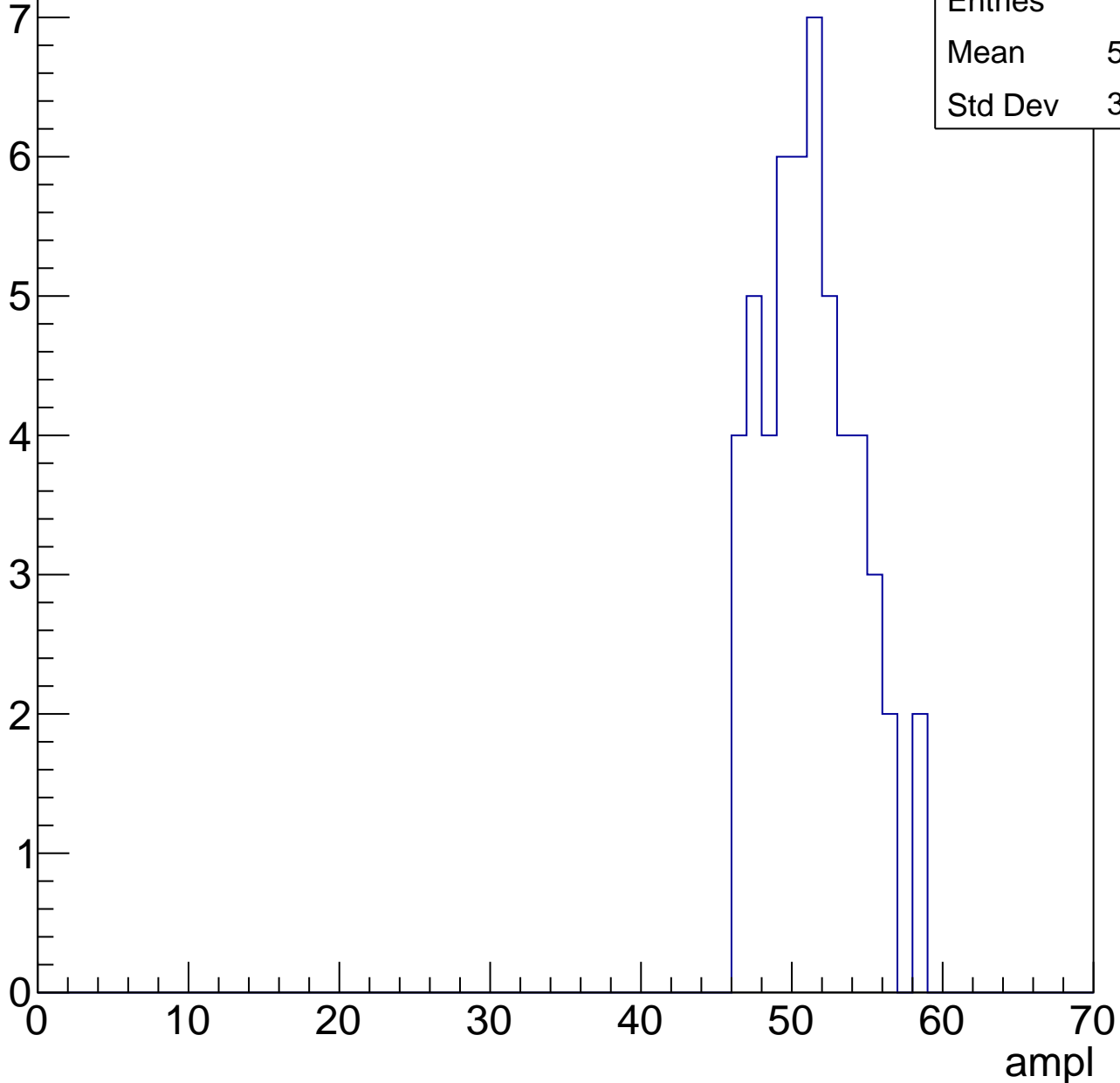


# B1L101S, U11-ch12, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

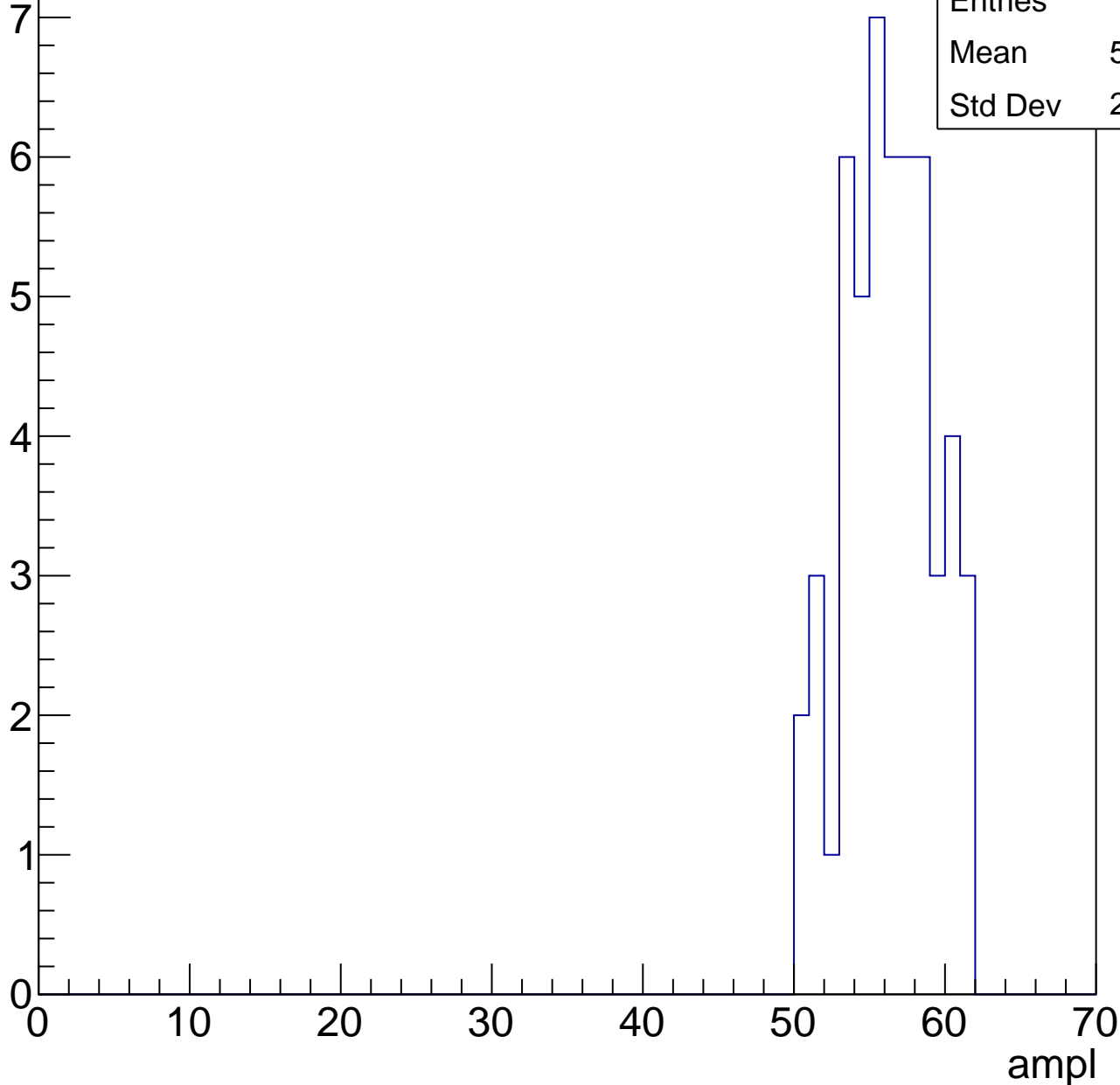
Entries	52
Mean	50.83
Std Dev	3.093



# B1L101S, U11-ch12, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



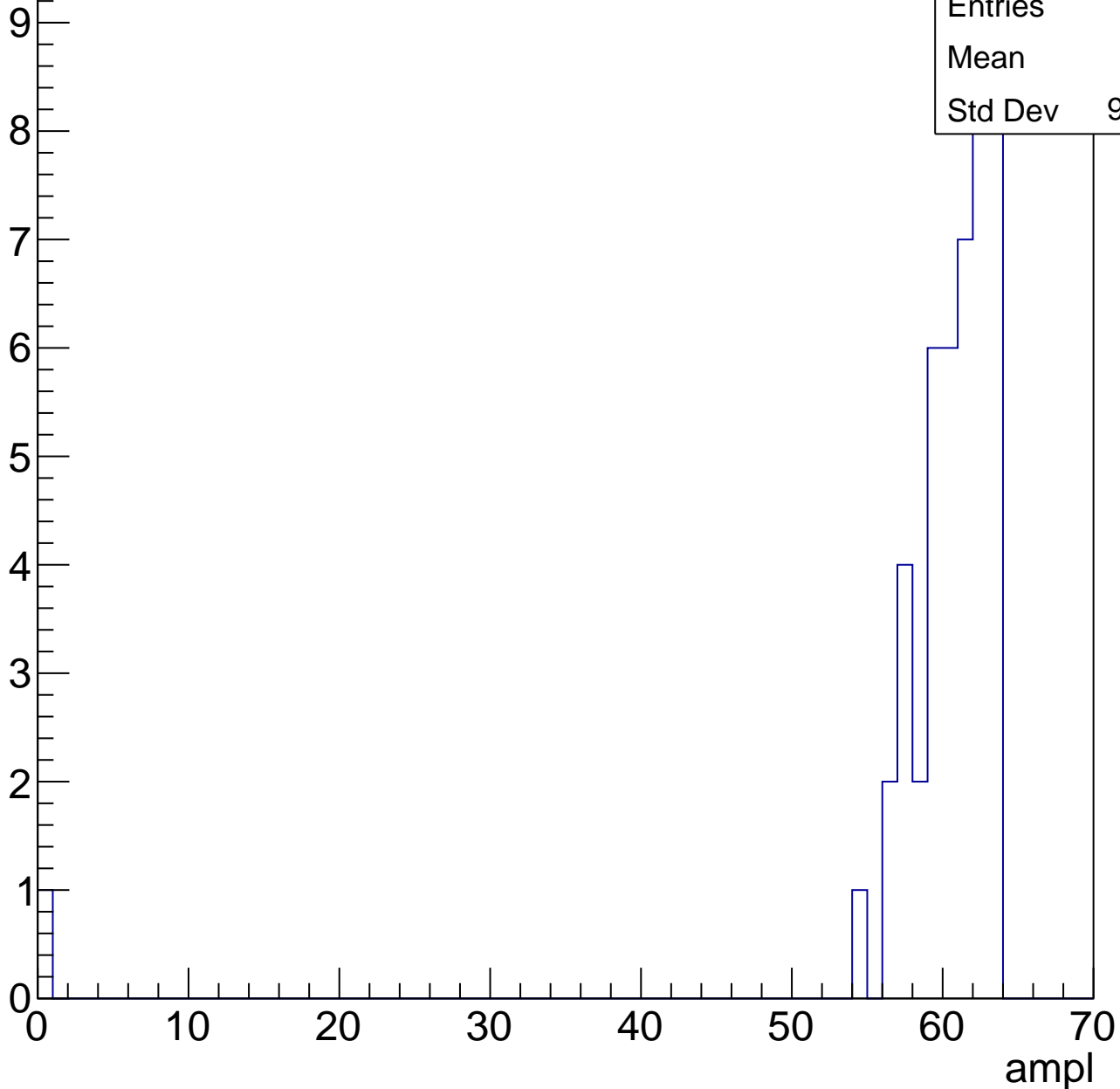
Entries	52
Mean	55.85
Std Dev	2.905

# B1L101S, U11-ch12, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	46
Mean	59
Std Dev	9.079



# B1L101S, U11-ch12, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

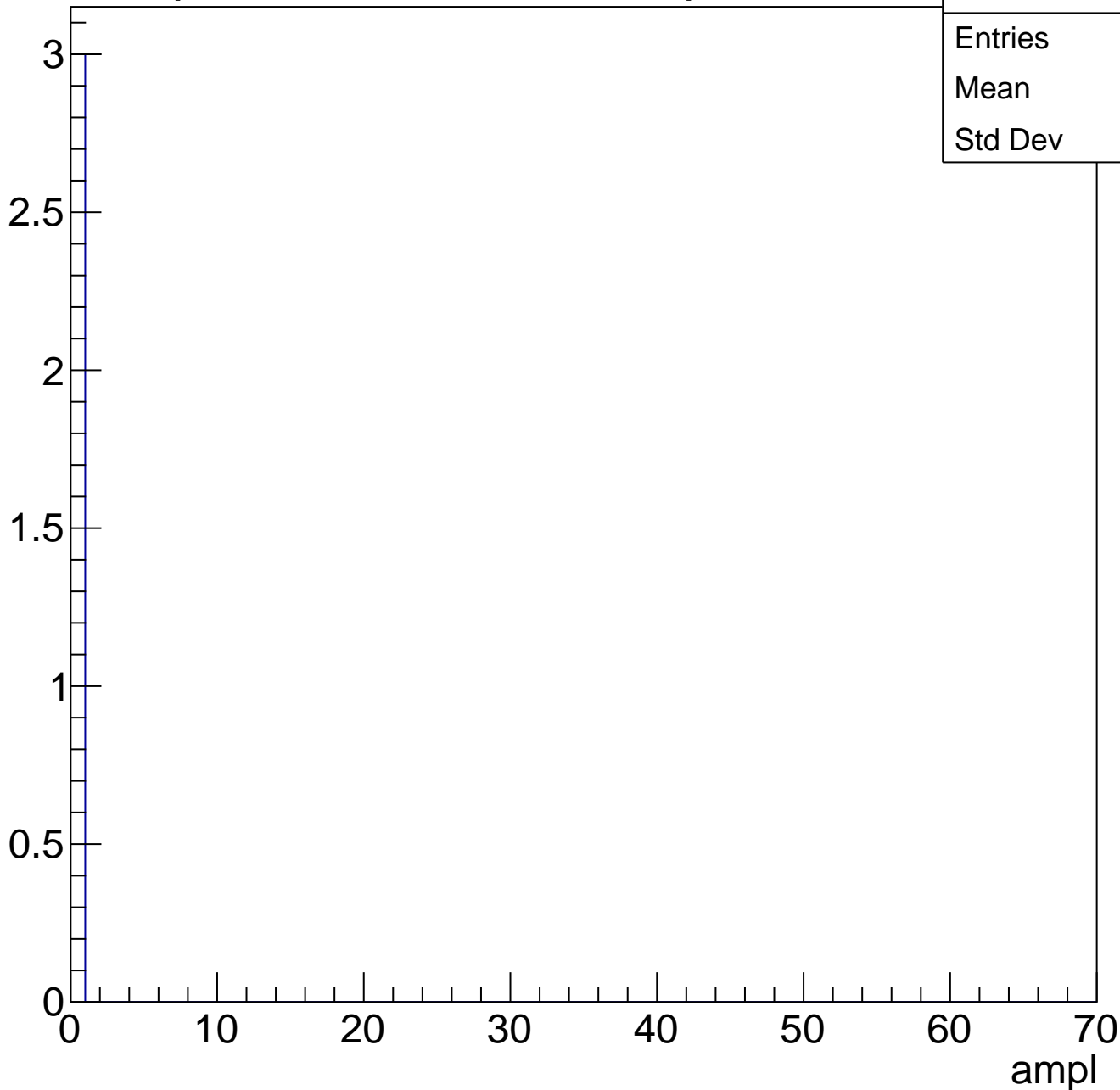




# B1L101S, U11-ch12, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U11-ch13, adc0

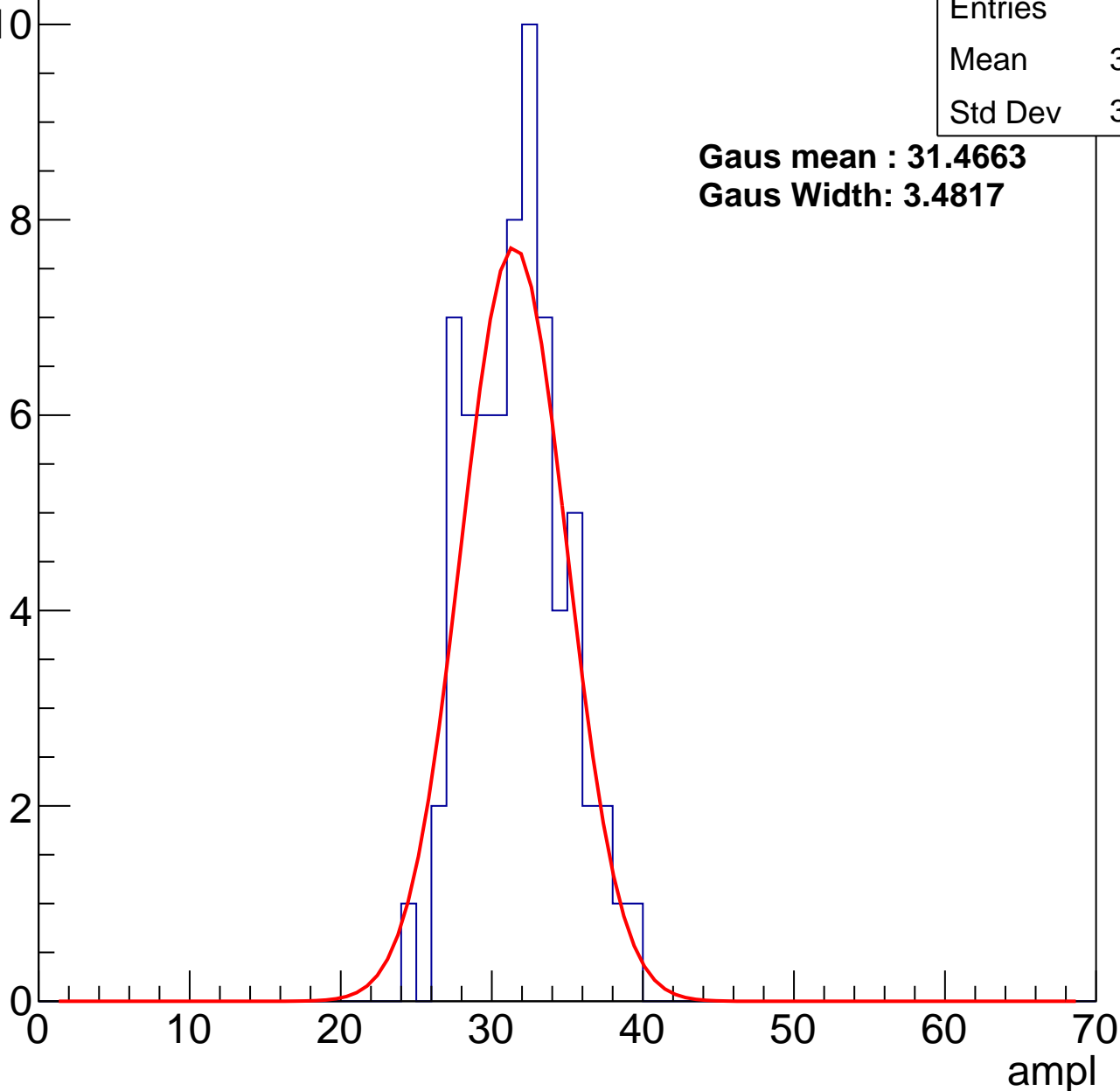
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	31.18
Std Dev	3.167

**Gaus mean : 31.4663**

**Gaus Width: 3.4817**



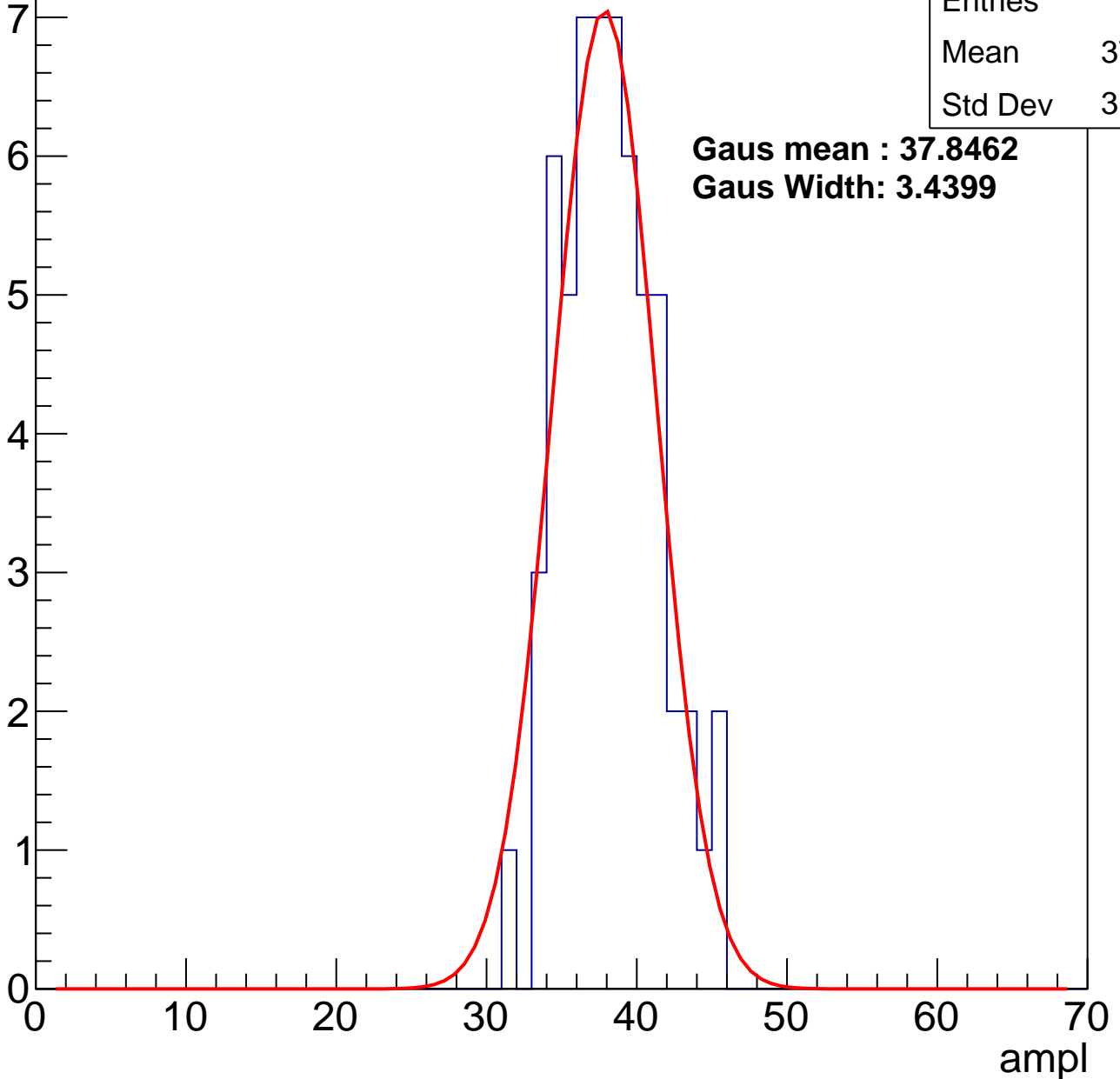
# B1L101S, U11-ch13, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	37.78
Std Dev	3.147

**Gaus mean : 37.8462**  
**Gaus Width: 3.4399**



# B1L101S, U11-ch13, adc2

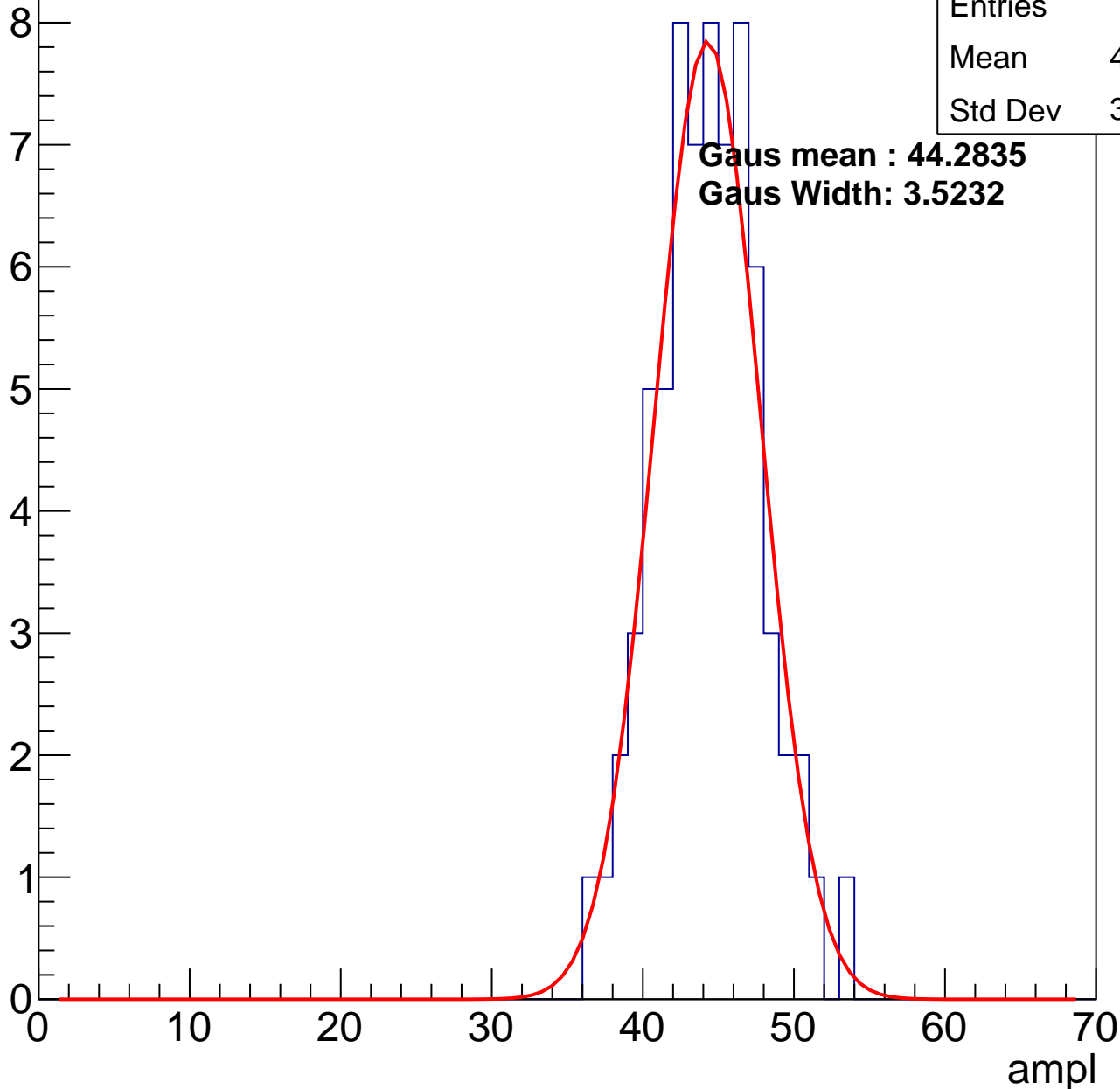
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	43.87
Std Dev	3.414

**Gaus mean : 44.2835**

**Gaus Width: 3.5232**



# B1L101S, U11-ch13, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	90
Mean	52.07
Std Dev	3.708

Entry

10

8

6

4

2

0

0

10

20

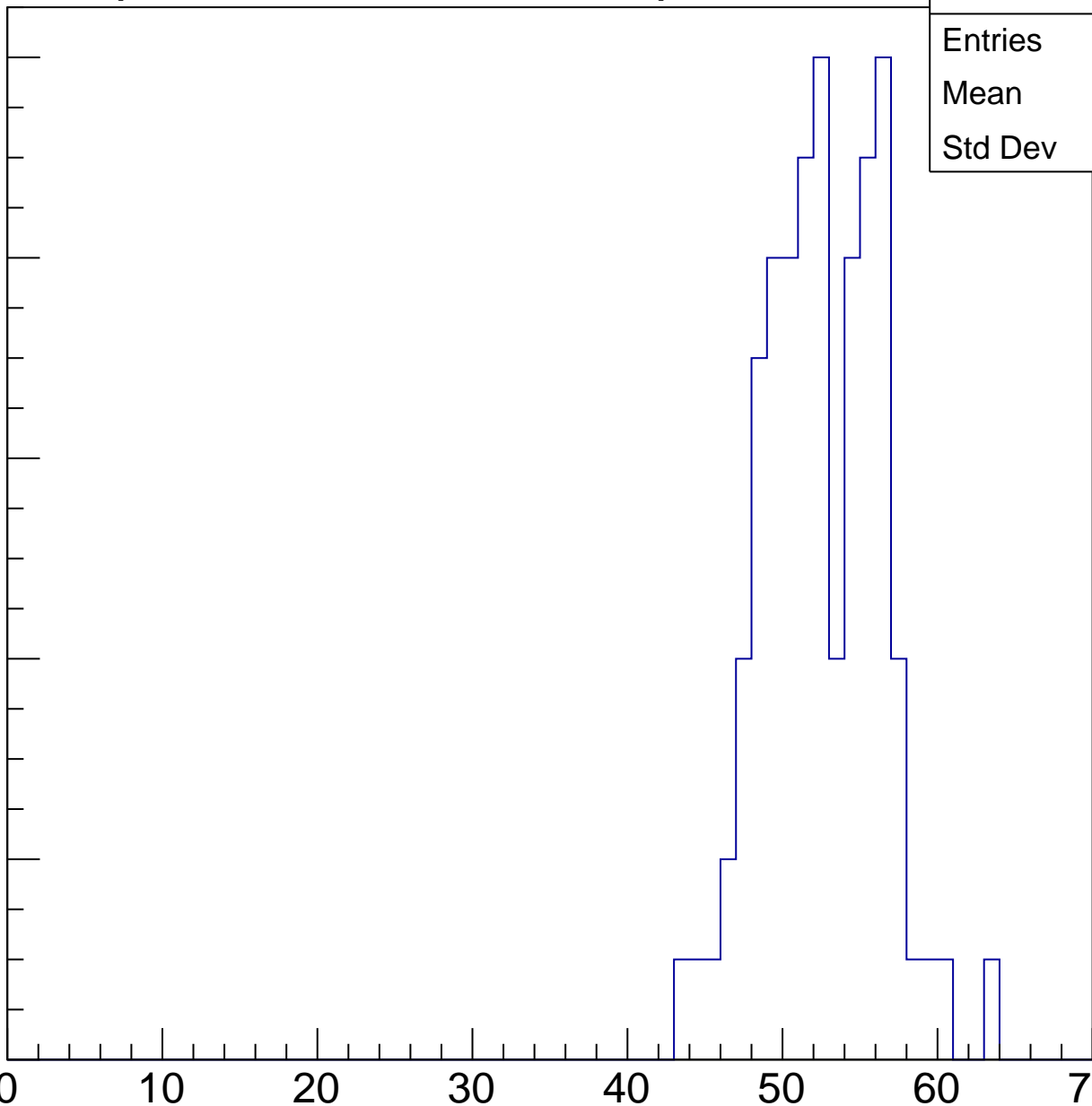
30

40

50

60

ampl

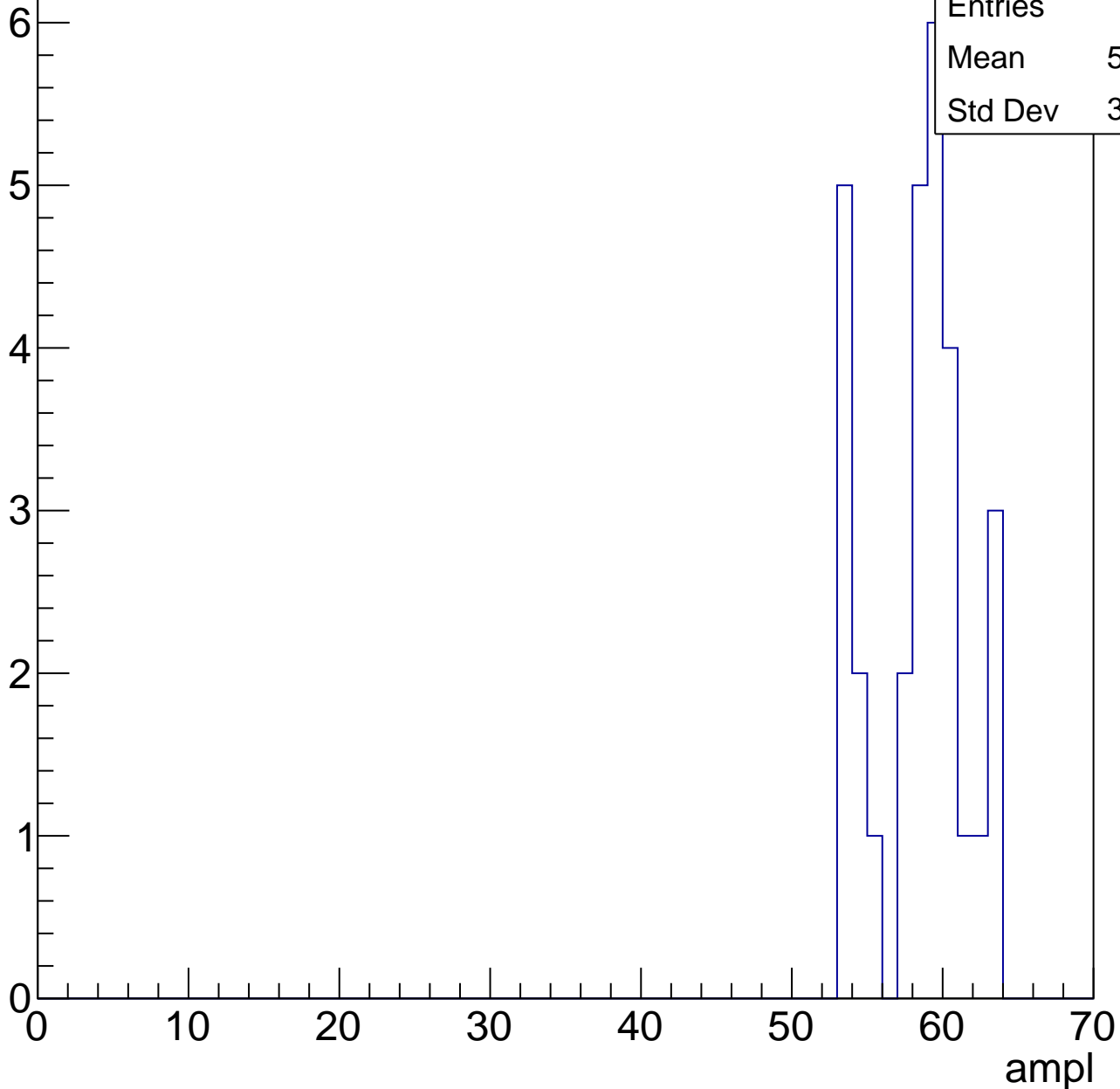


# B1L101S, U11-ch13, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	30
Mean	57.93
Std Dev	3.108

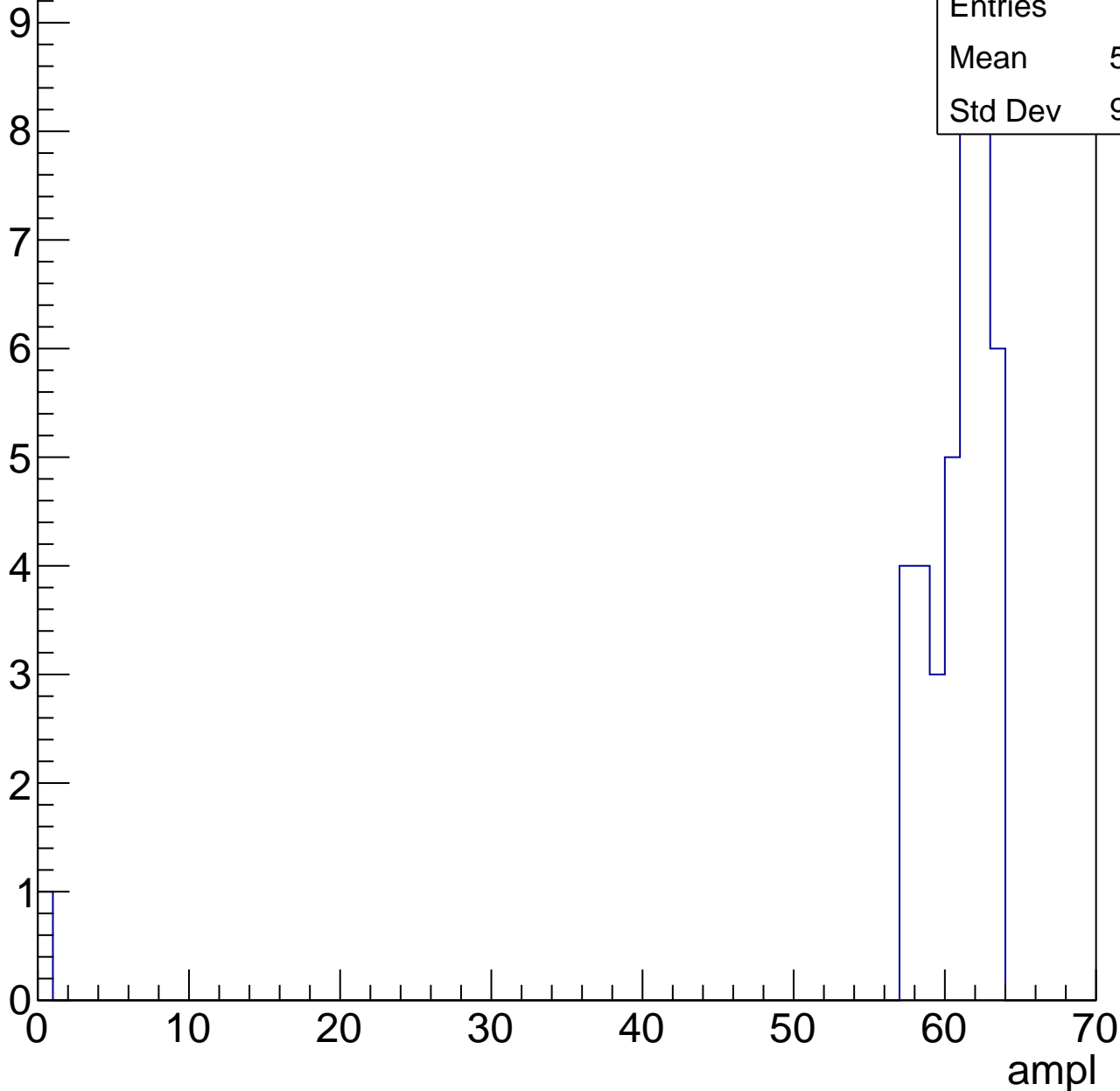


# B1L101S, U11-ch13, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	41
Mean	59.07
Std Dev	9.524



# B1L101S, U11-ch13, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch13, adc7

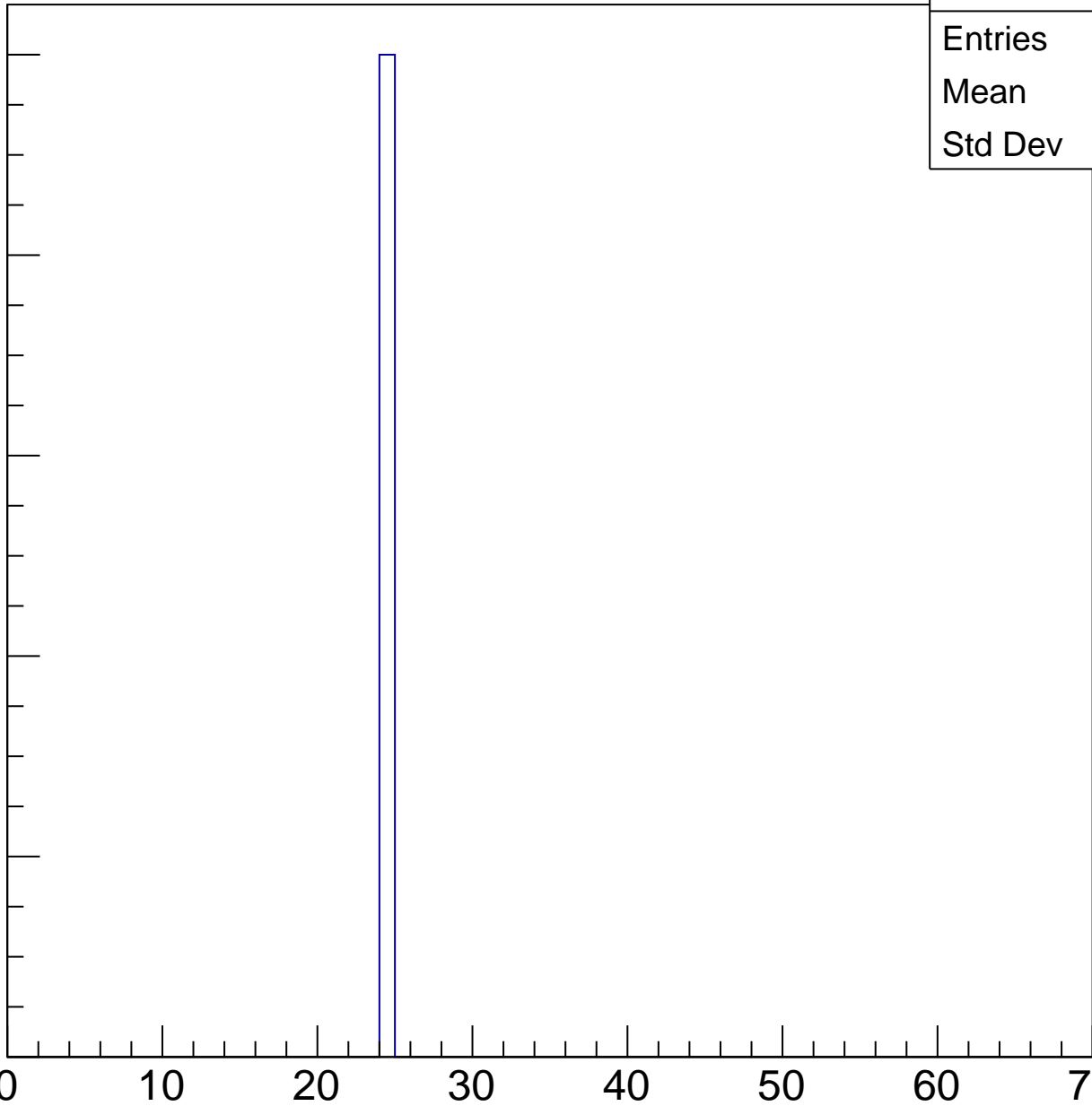
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	24
Std Dev	0

ampl



# B1L101S, U11-ch14, adc0

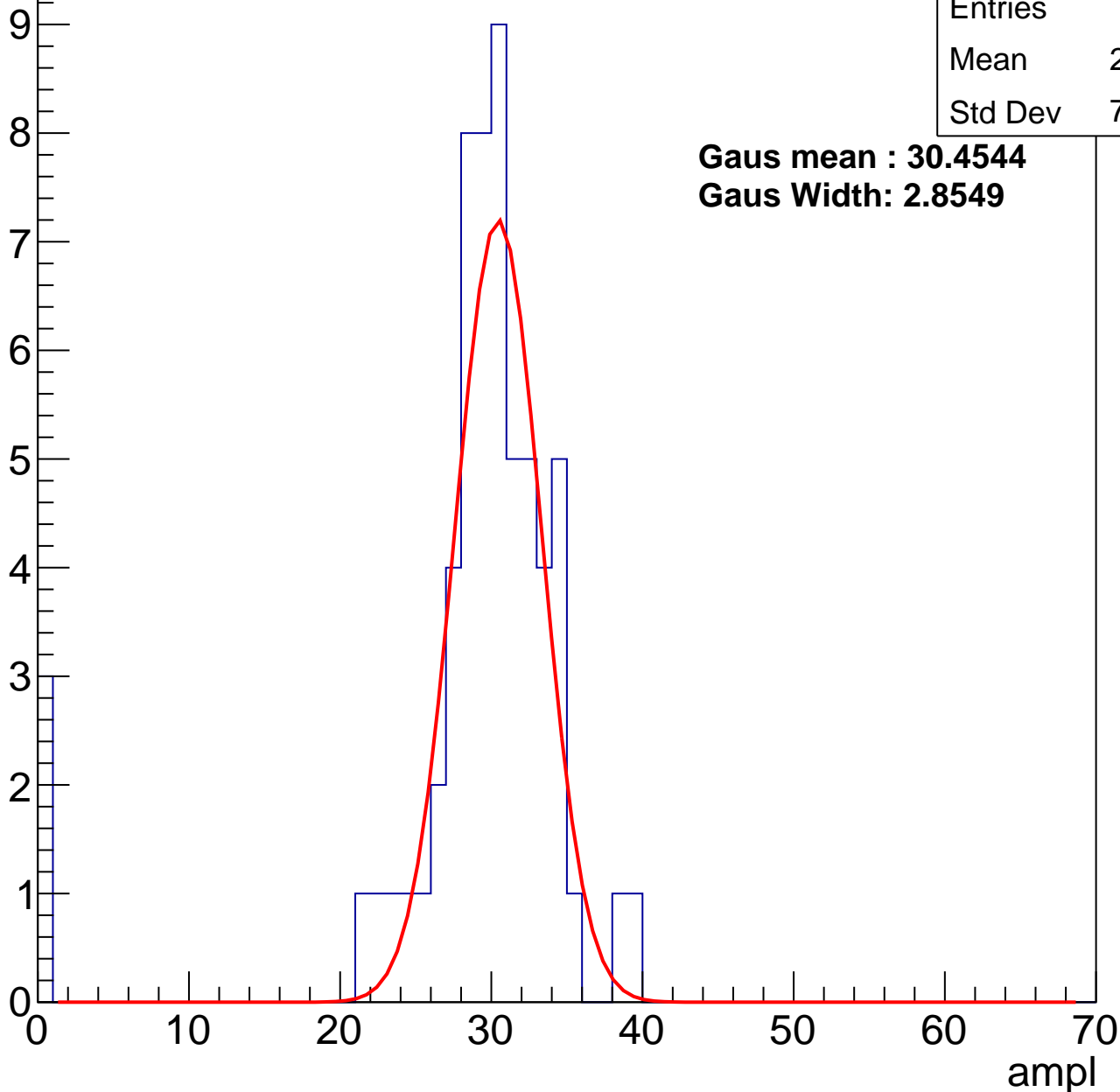
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	28.36
Std Dev	7.254

**Gaus mean : 30.4544**

**Gaus Width: 2.8549**



# B1L101S, U11-ch14, adc1

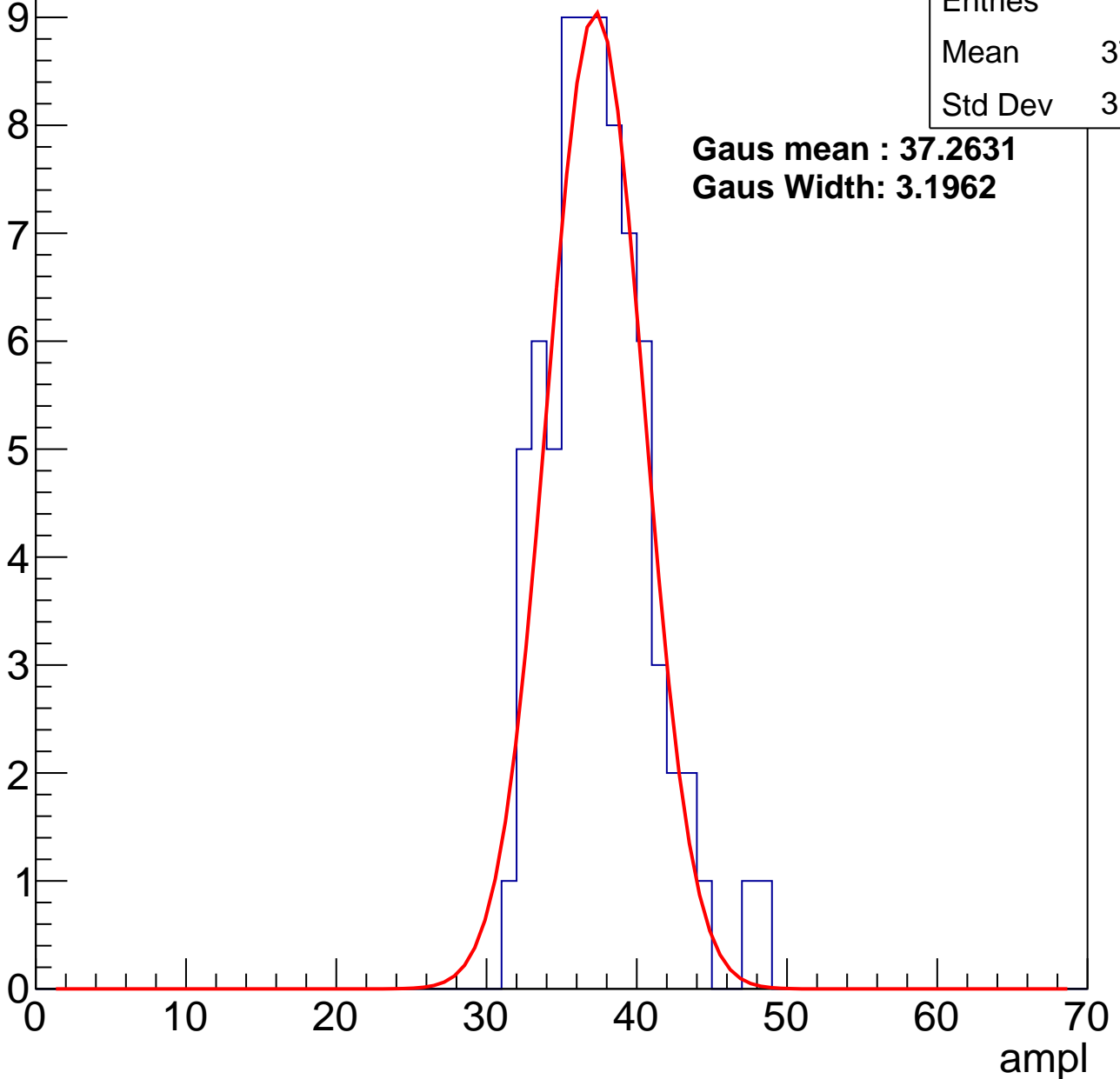
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	37.07
Std Dev	3.419

**Gaus mean : 37.2631**

**Gaus Width: 3.1962**



# B1L101S, U11-ch14, adc2

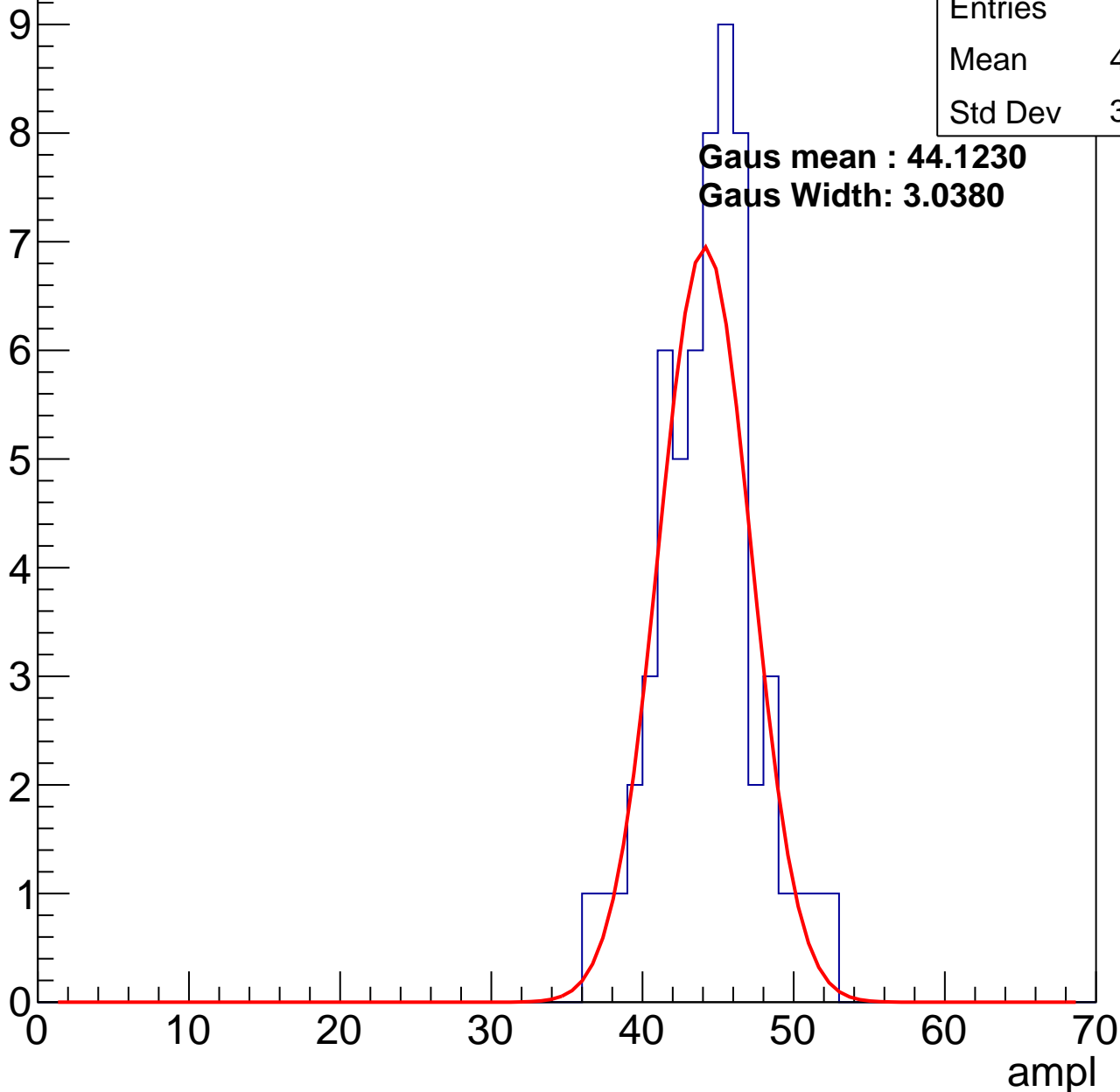
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	43.86
Std Dev	3.207

**Gaus mean : 44.1230**

**Gaus Width: 3.0380**

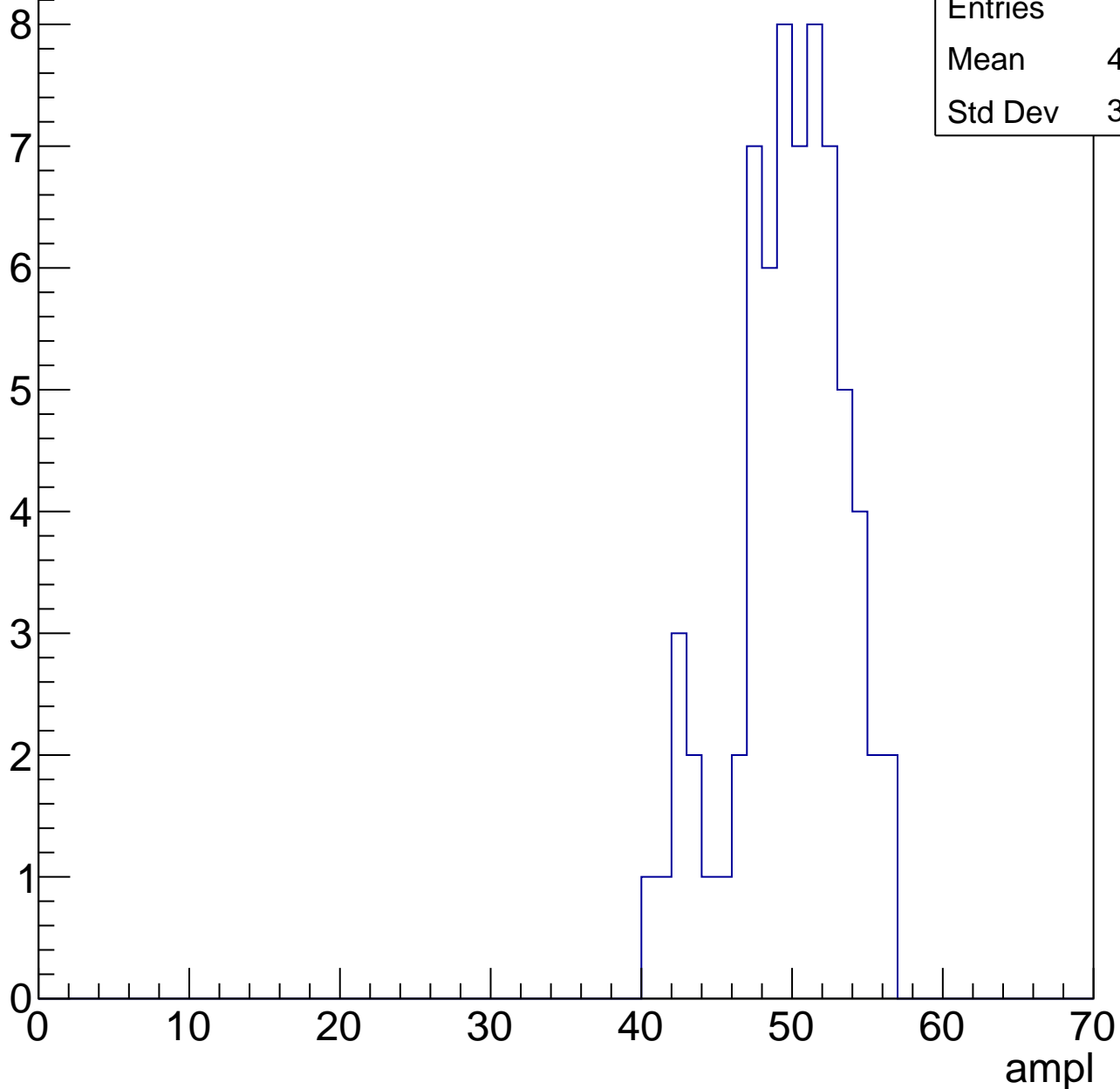


# B1L101S, U11-ch14, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	49.37
Std Dev	3.664

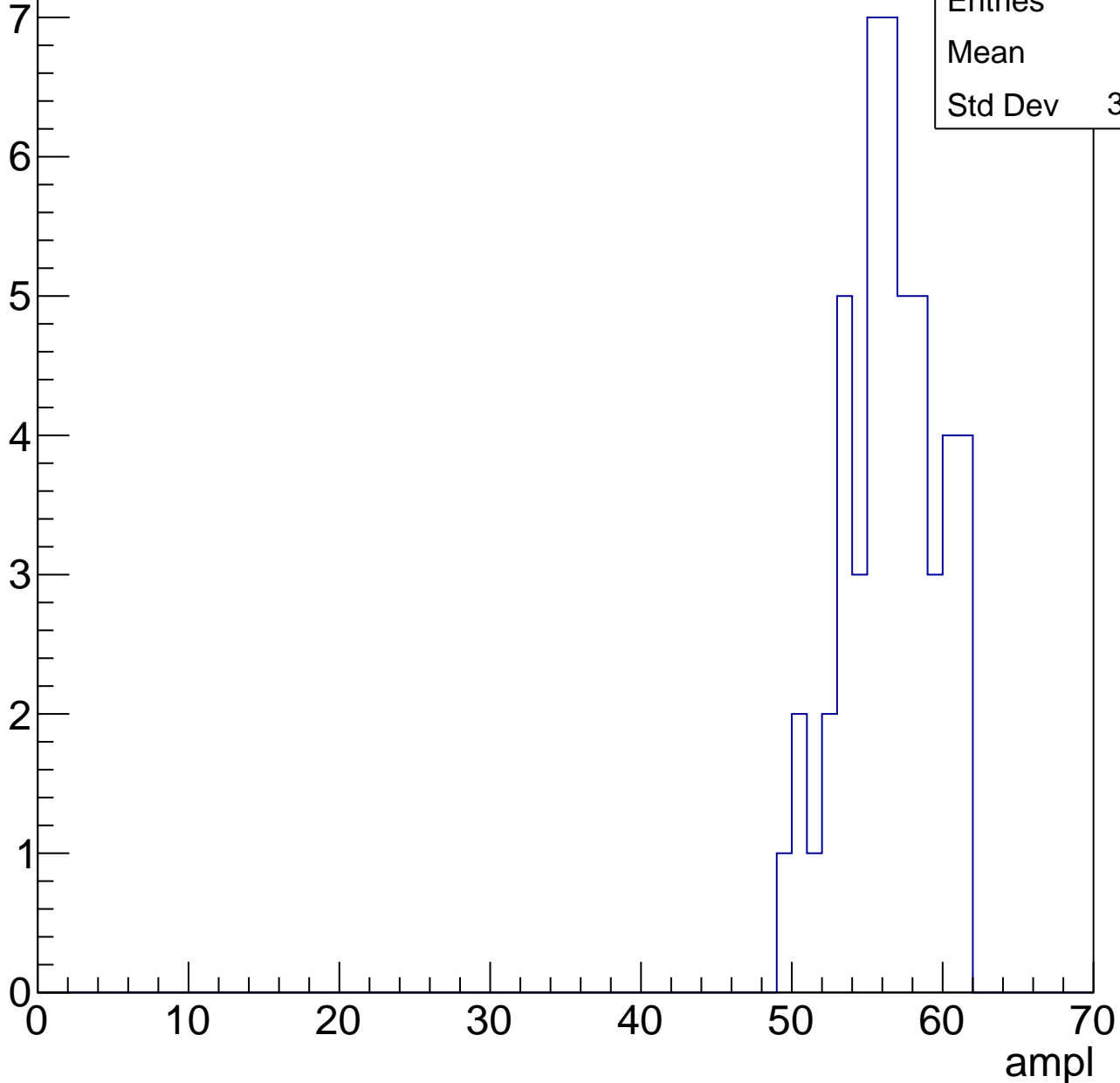


# B1L101S, U11-ch14, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	49
Mean	56
Std Dev	3.057

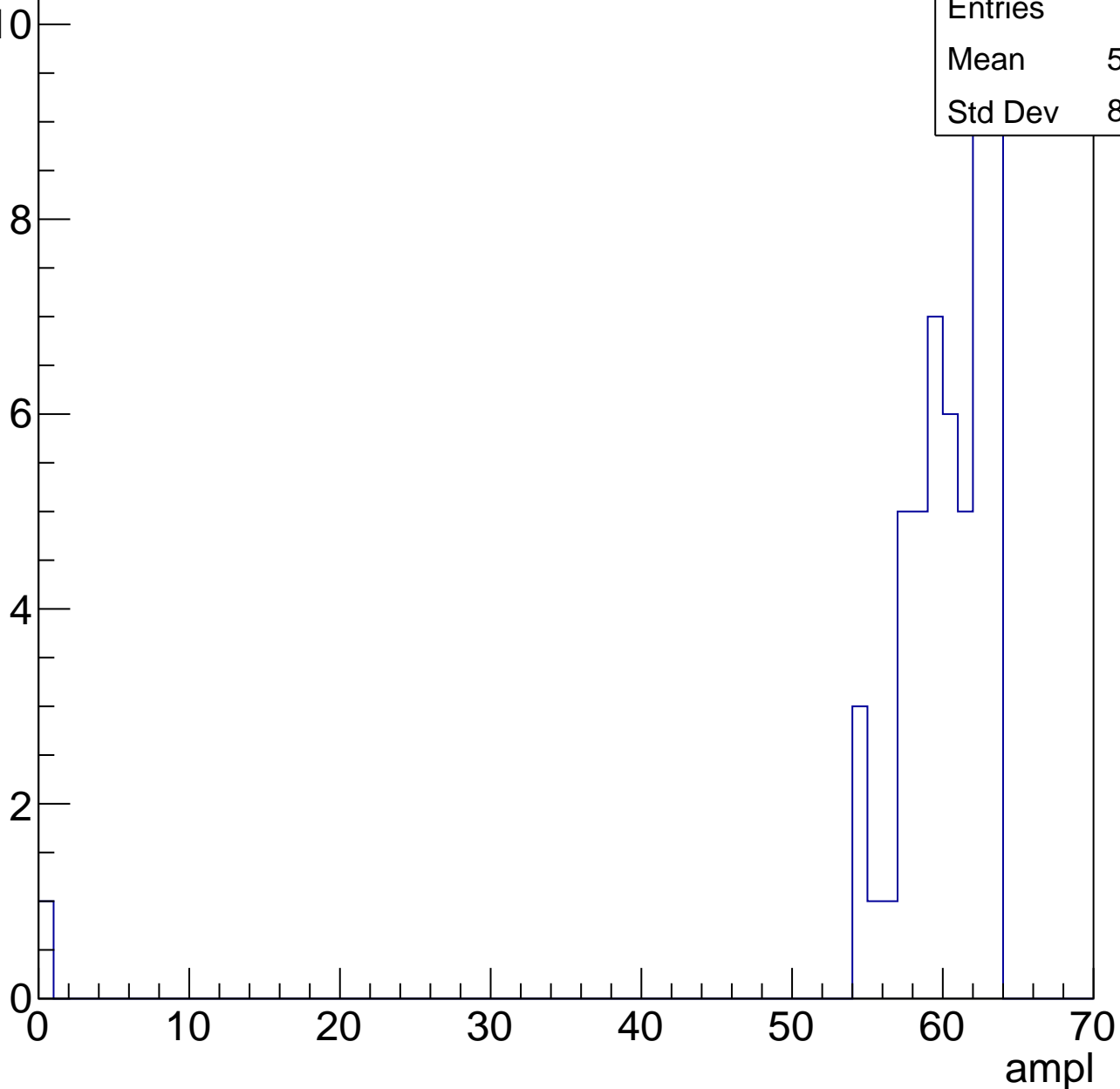


# B1L101S, U11-ch14, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	58.74
Std Dev	8.537



# B1L101S, U11-ch14, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch14, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U11-ch15, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	67
Mean	31.52
Std Dev	3.329

**Gaus mean : 32.0648**

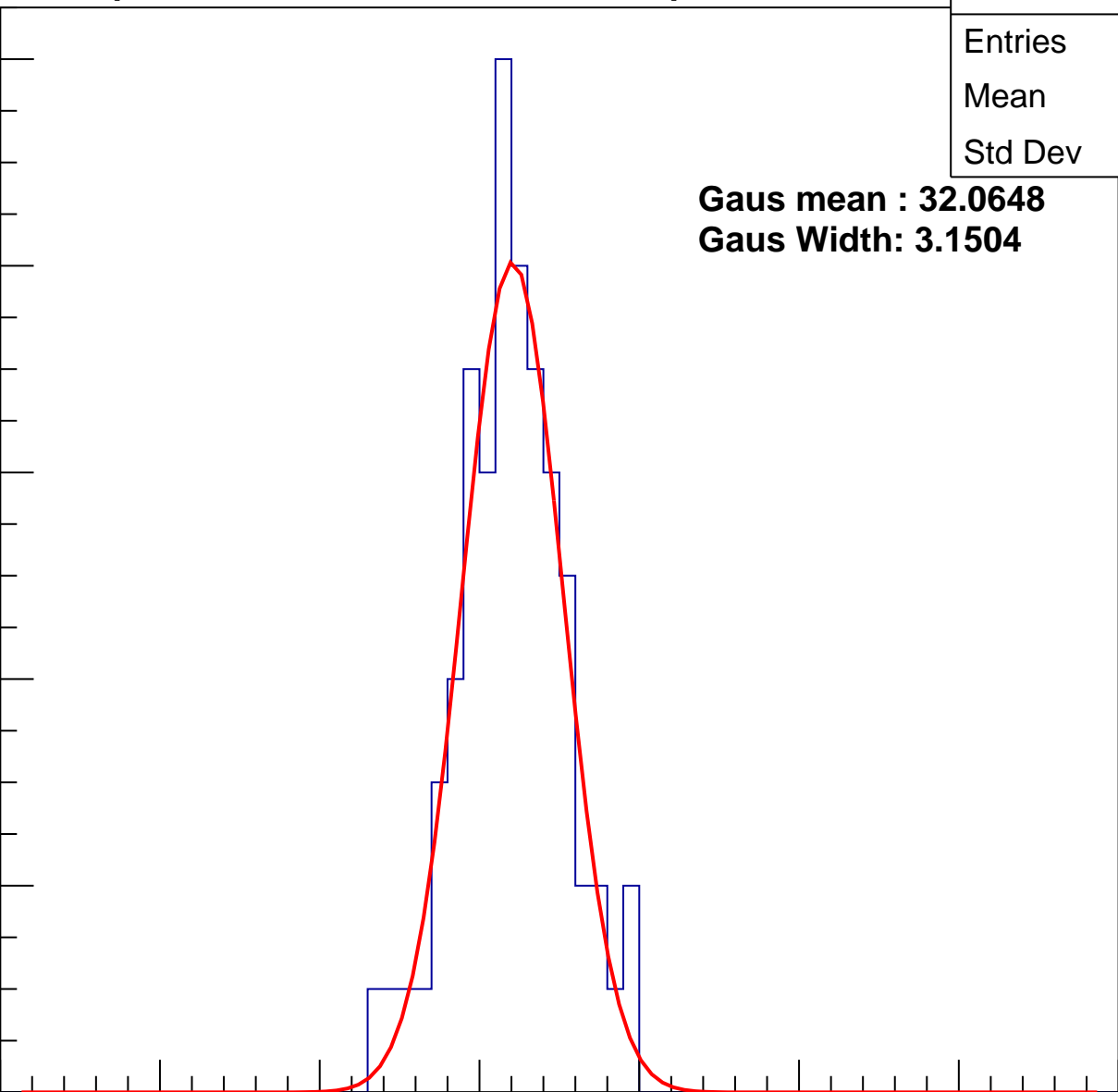
**Gaus Width: 3.1504**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U11-ch15, adc1

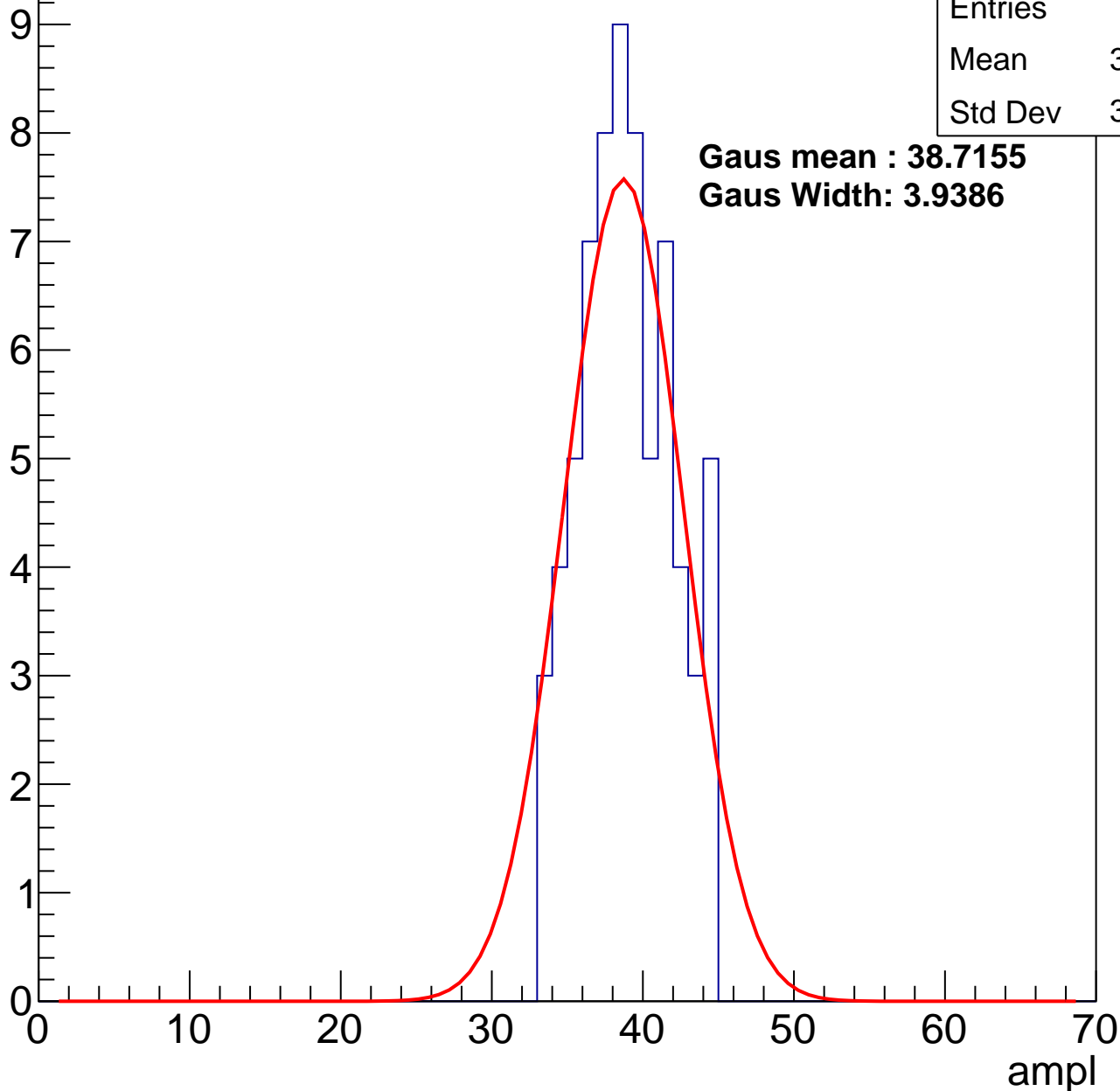
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	38.47
Std Dev	3.007

**Gaus mean : 38.7155**

**Gaus Width: 3.9386**



# B1L101S, U11-ch15, adc2

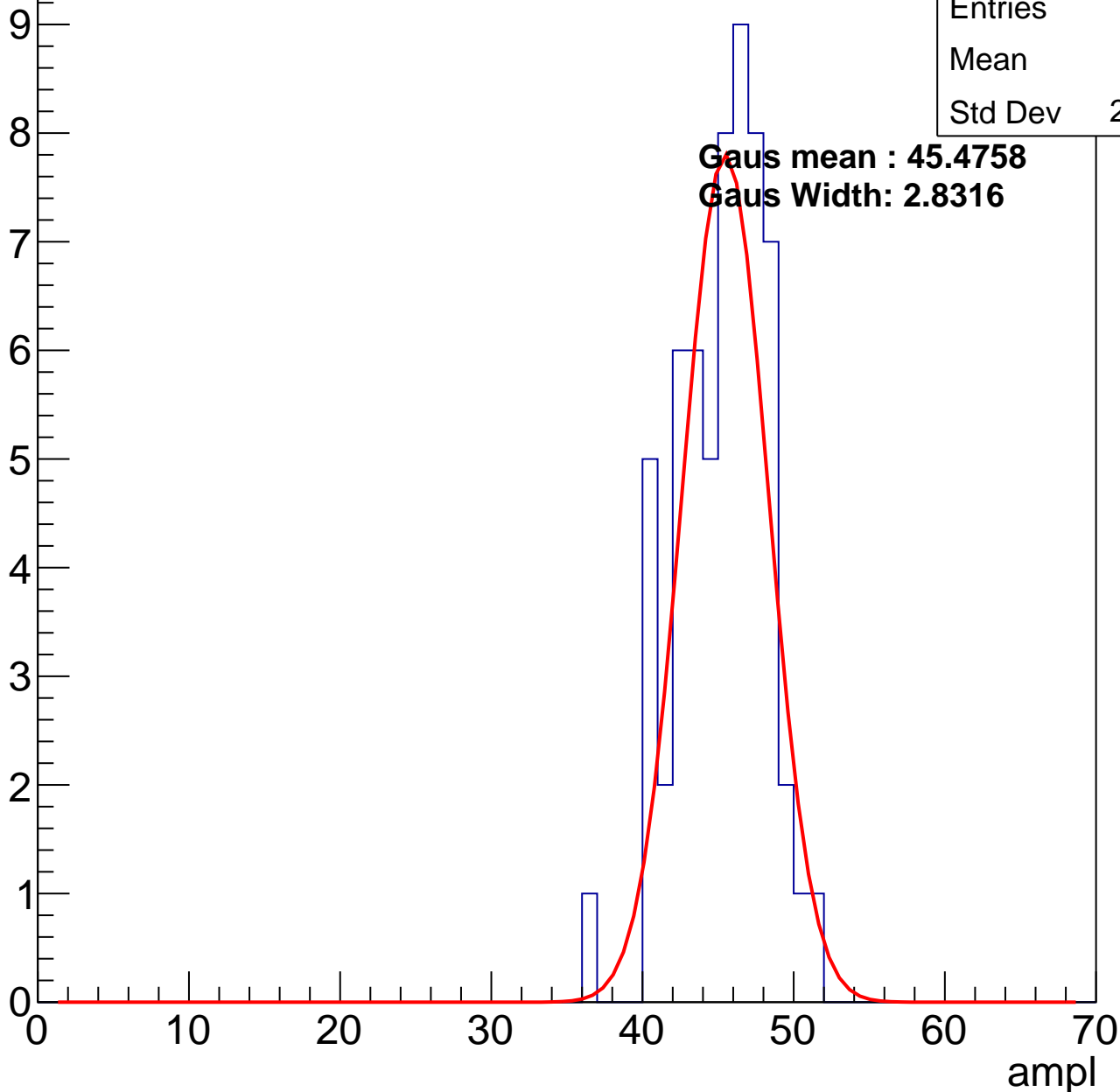
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	44.8
Std Dev	2.907

**Gaus mean : 45.4758**

**Gaus Width: 2.8316**

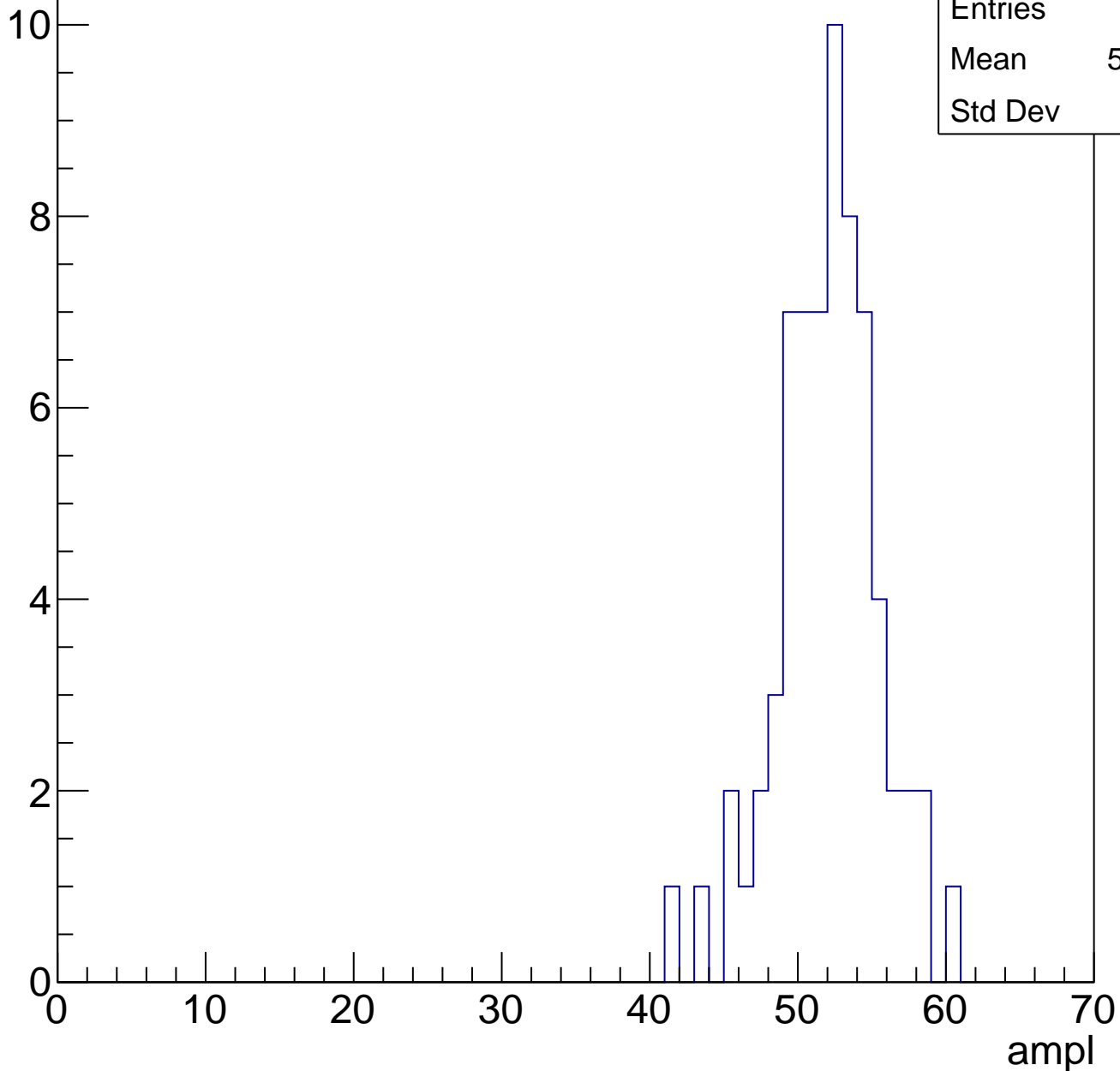


# B1L101S, U11-ch15, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	67
Mean	51.52
Std Dev	3.47

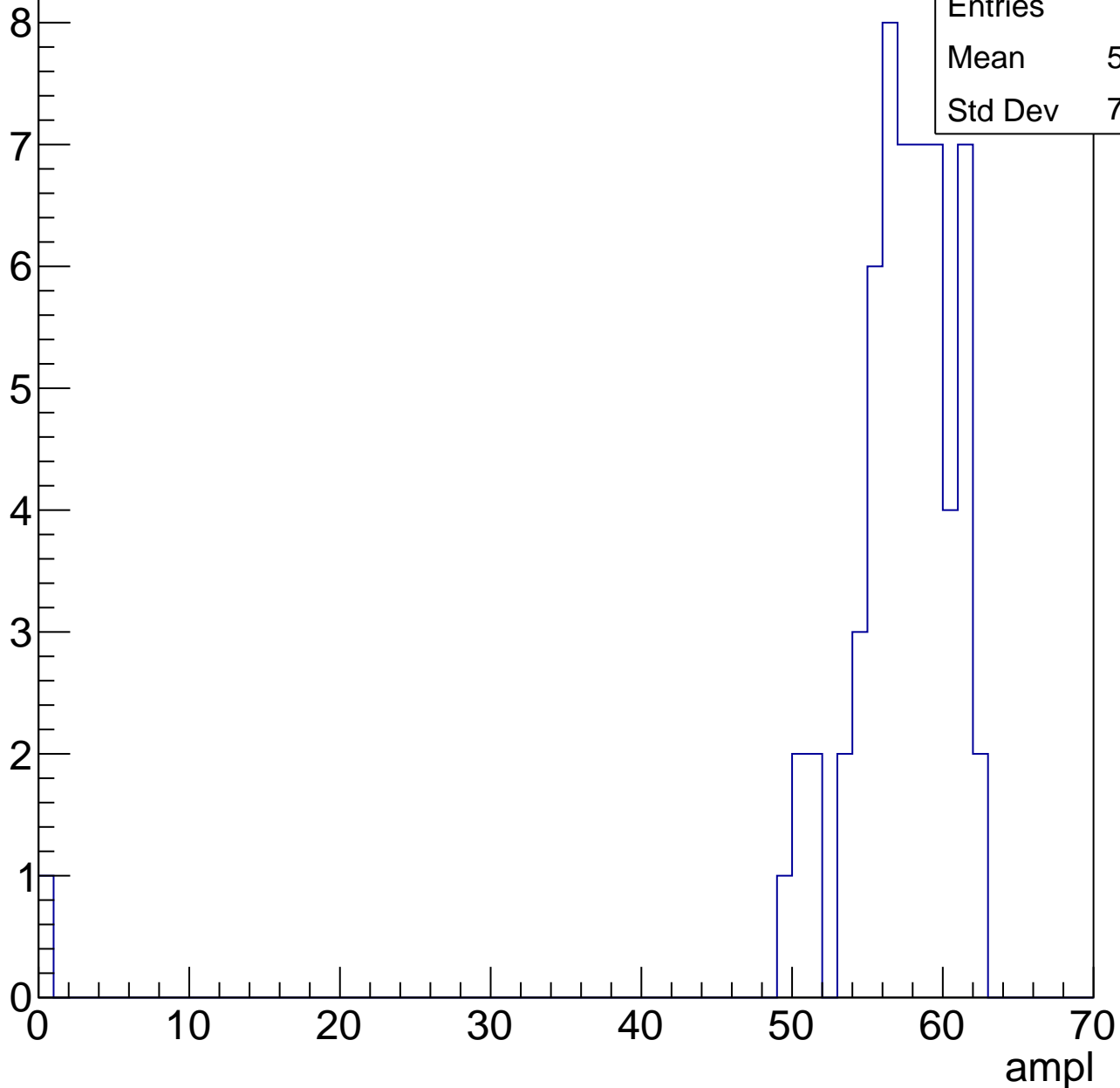
Entry



# B1L101S, U11-ch15, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

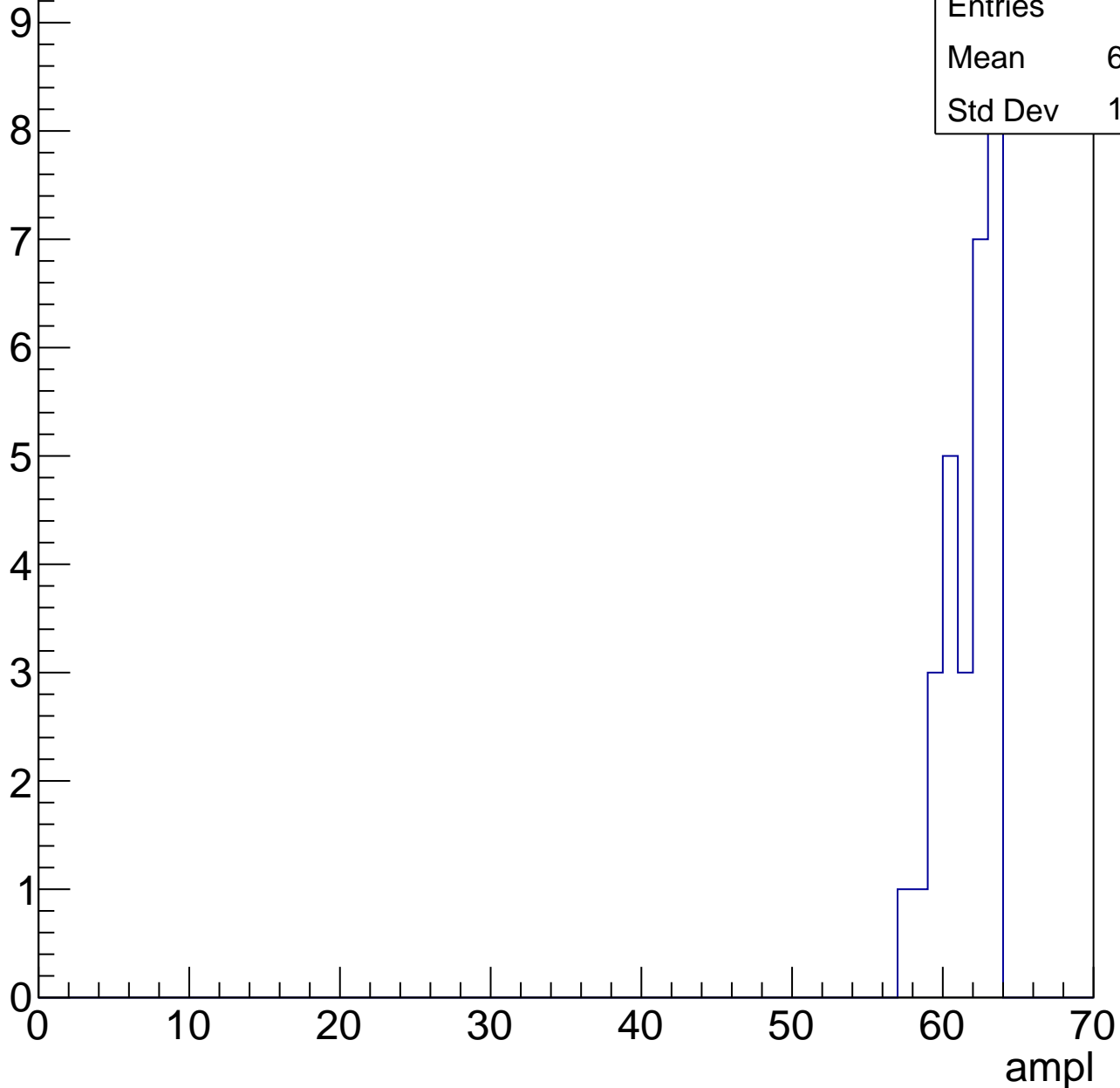
Entry



# B1L101S, U11-ch15, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U11-ch15, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch15, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U11-ch16, adc0

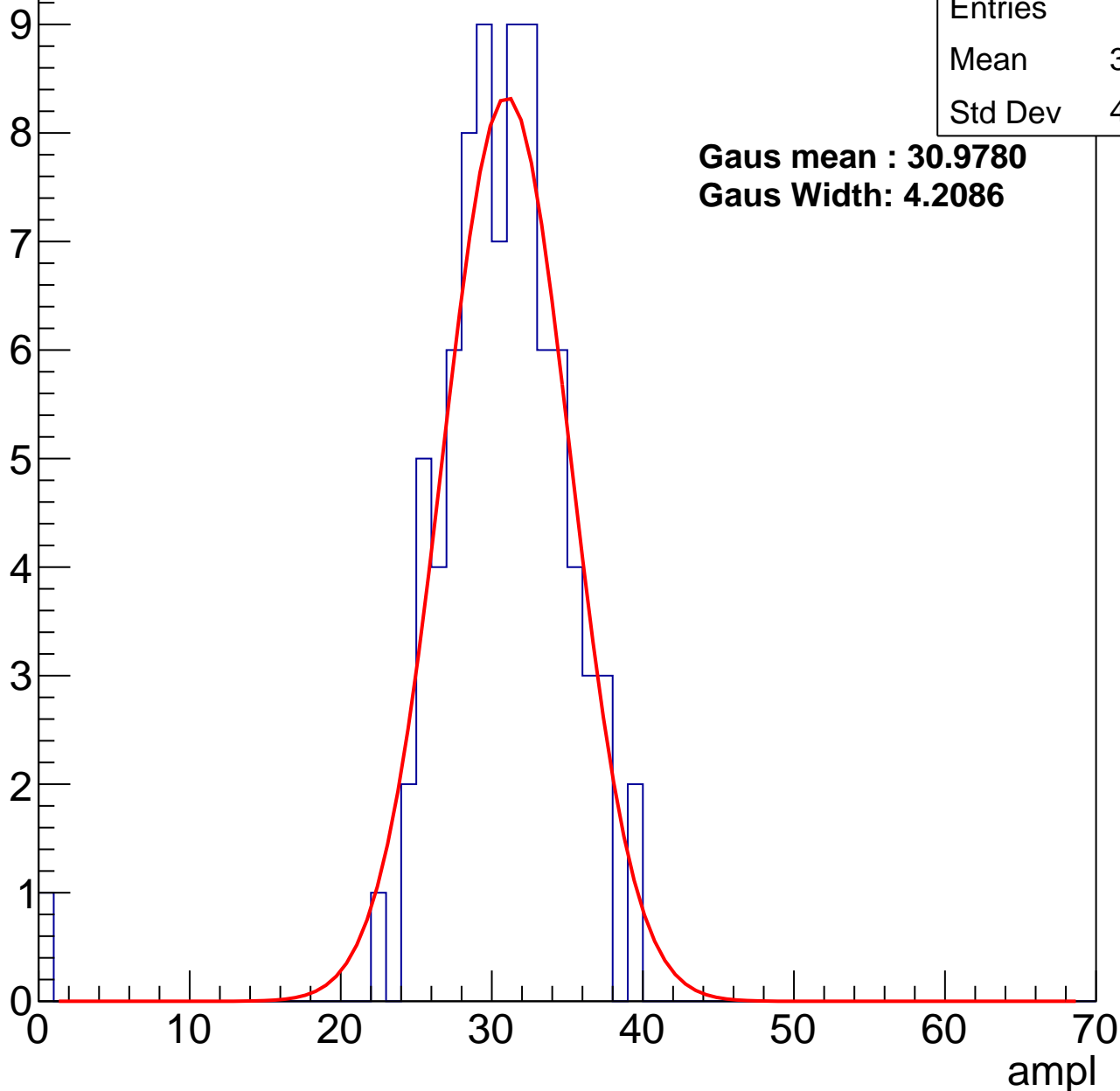
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	85
Mean	30.14
Std Dev	4.887

**Gaus mean : 30.9780**

**Gaus Width: 4.2086**



# B1L101S, U11-ch16, adc1

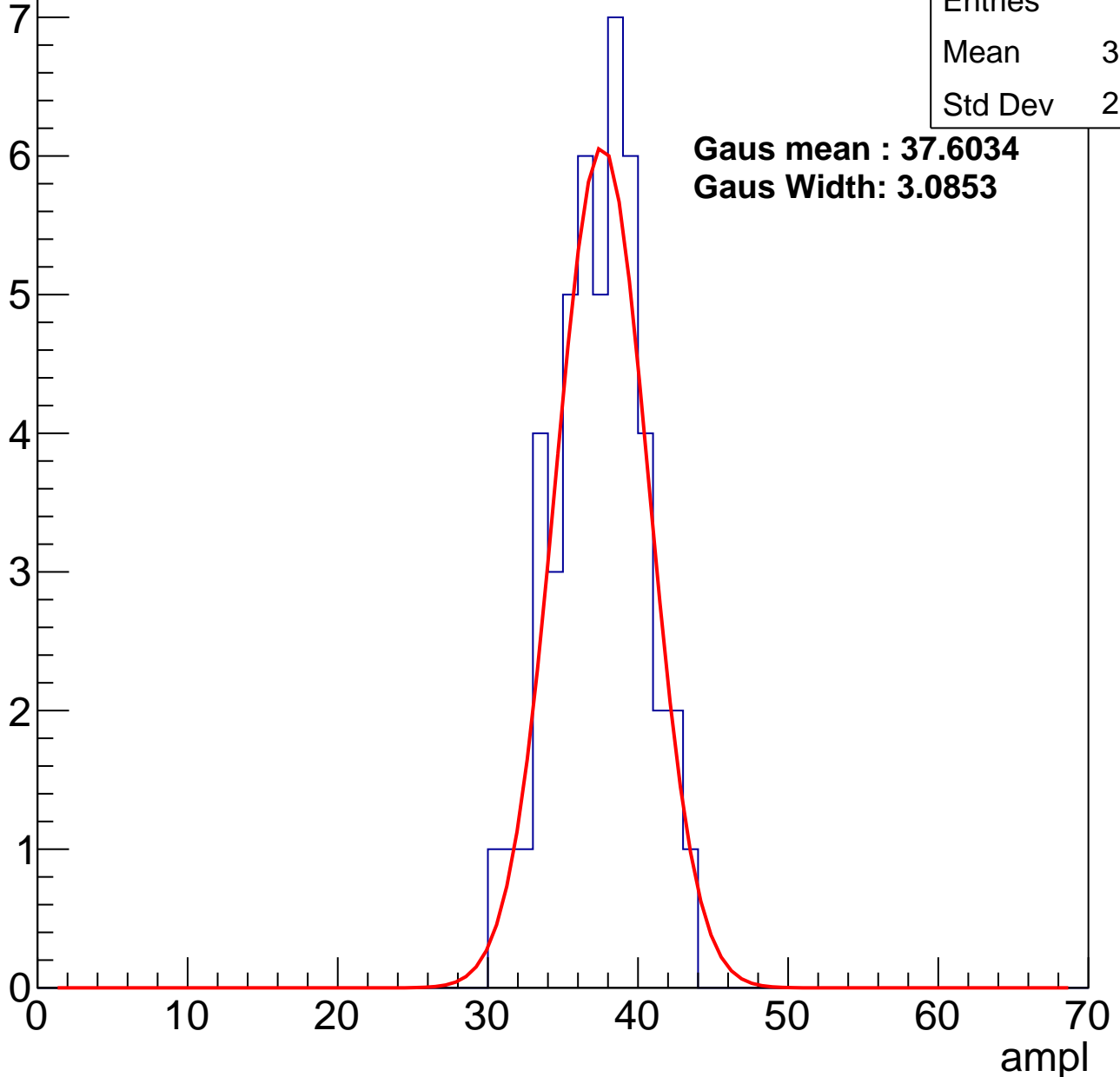
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	48
Mean	36.92
Std Dev	2.929

**Gaus mean : 37.6034**

**Gaus Width: 3.0853**



# B1L101S, U11-ch16, adc2

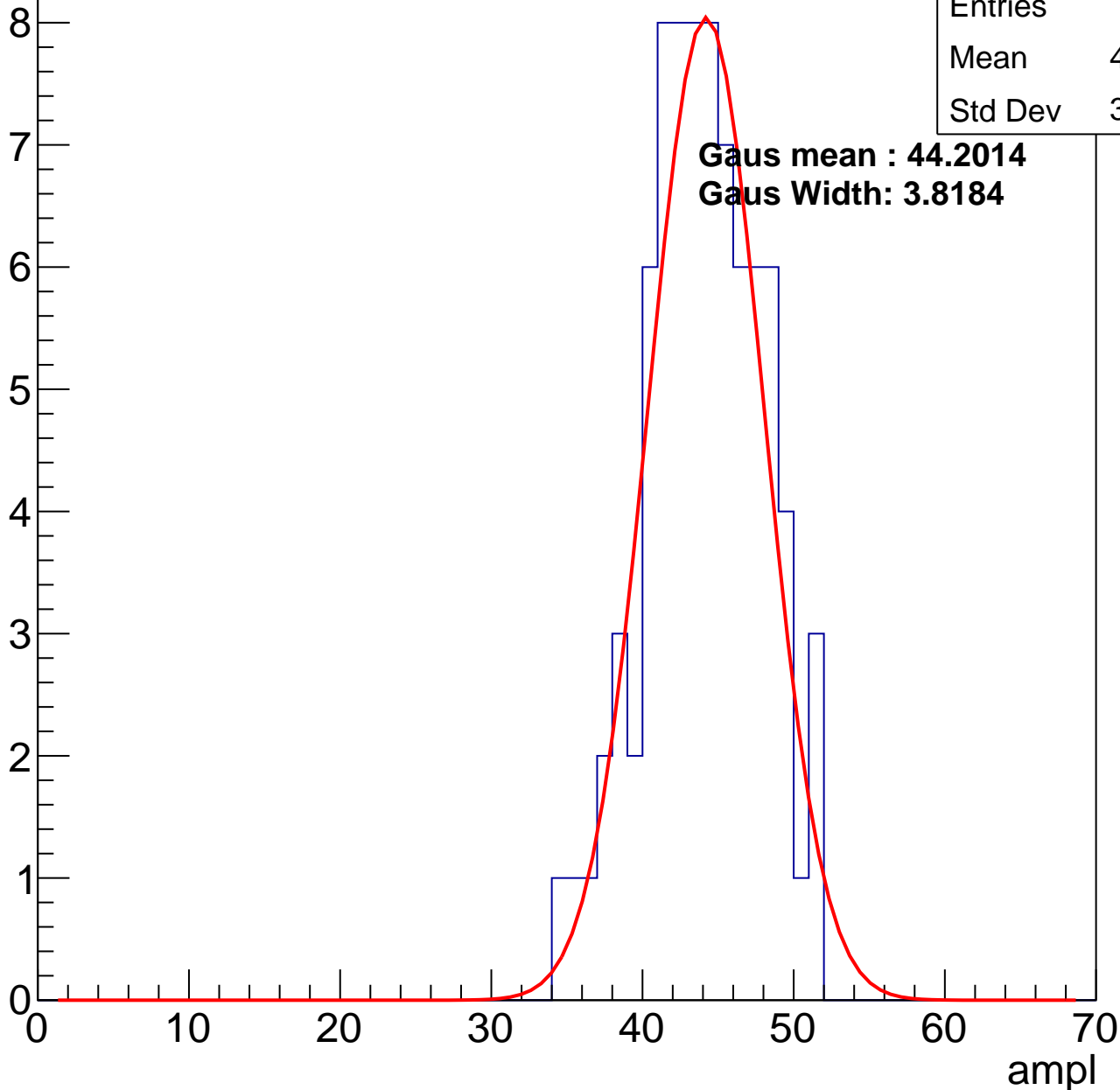
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	81
Mean	43.59
Std Dev	3.784

**Gaus mean : 44.2014**

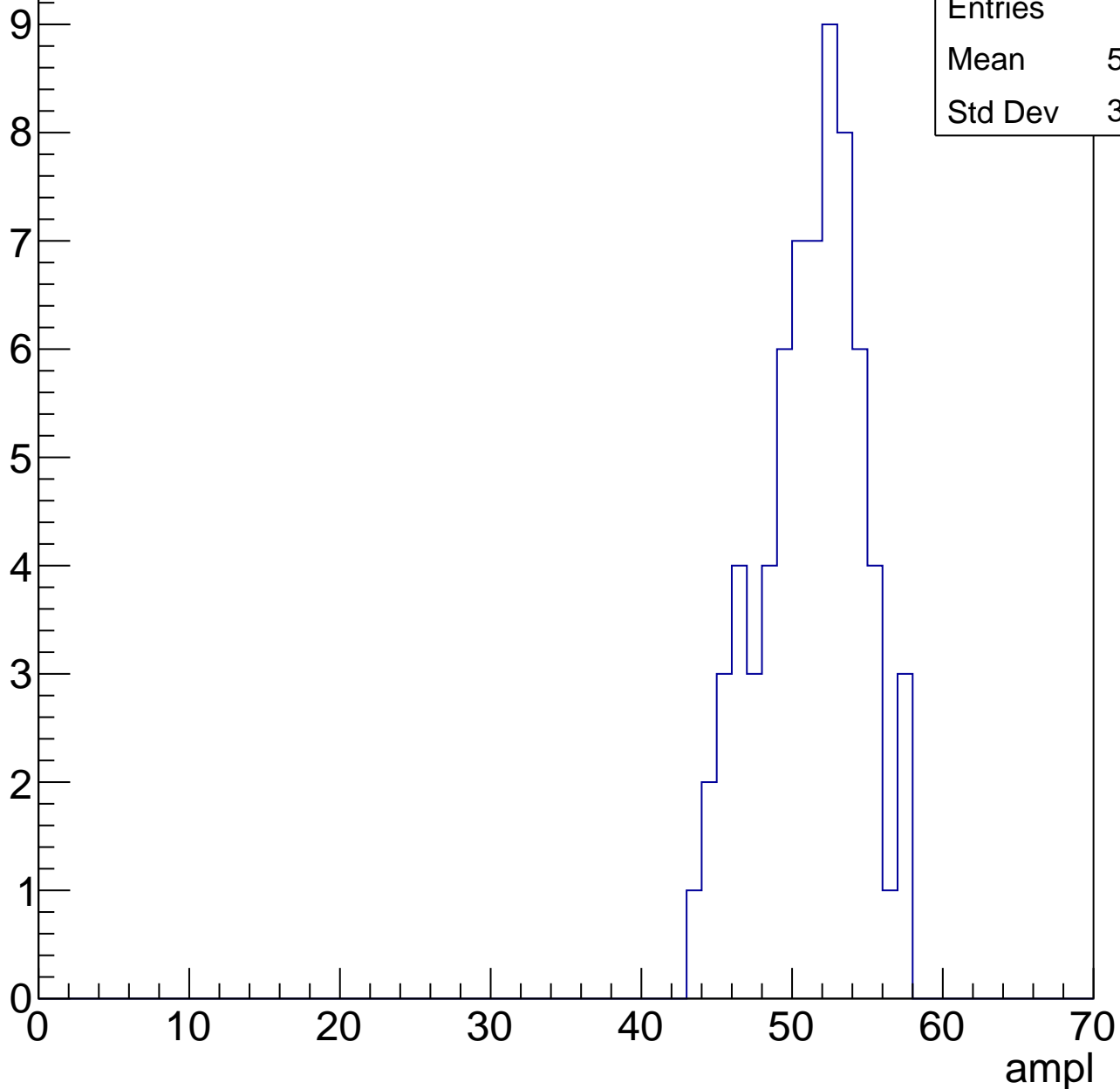
**Gaus Width: 3.8184**



# B1L101S, U11-ch16, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



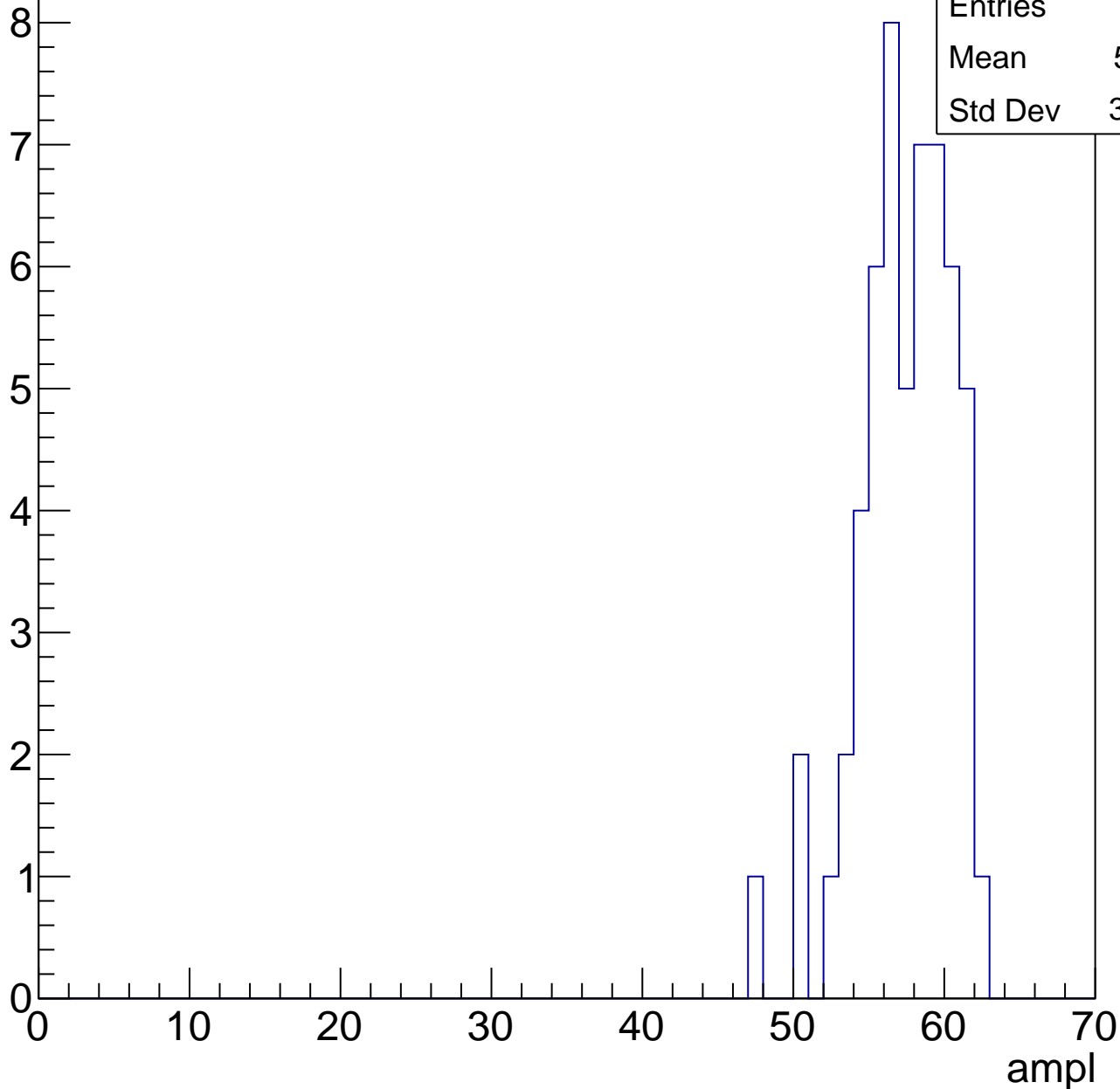
Entries	68
Mean	50.69
Std Dev	3.366

# B1L101S, U11-ch16, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	56.91
Std Dev	3.065

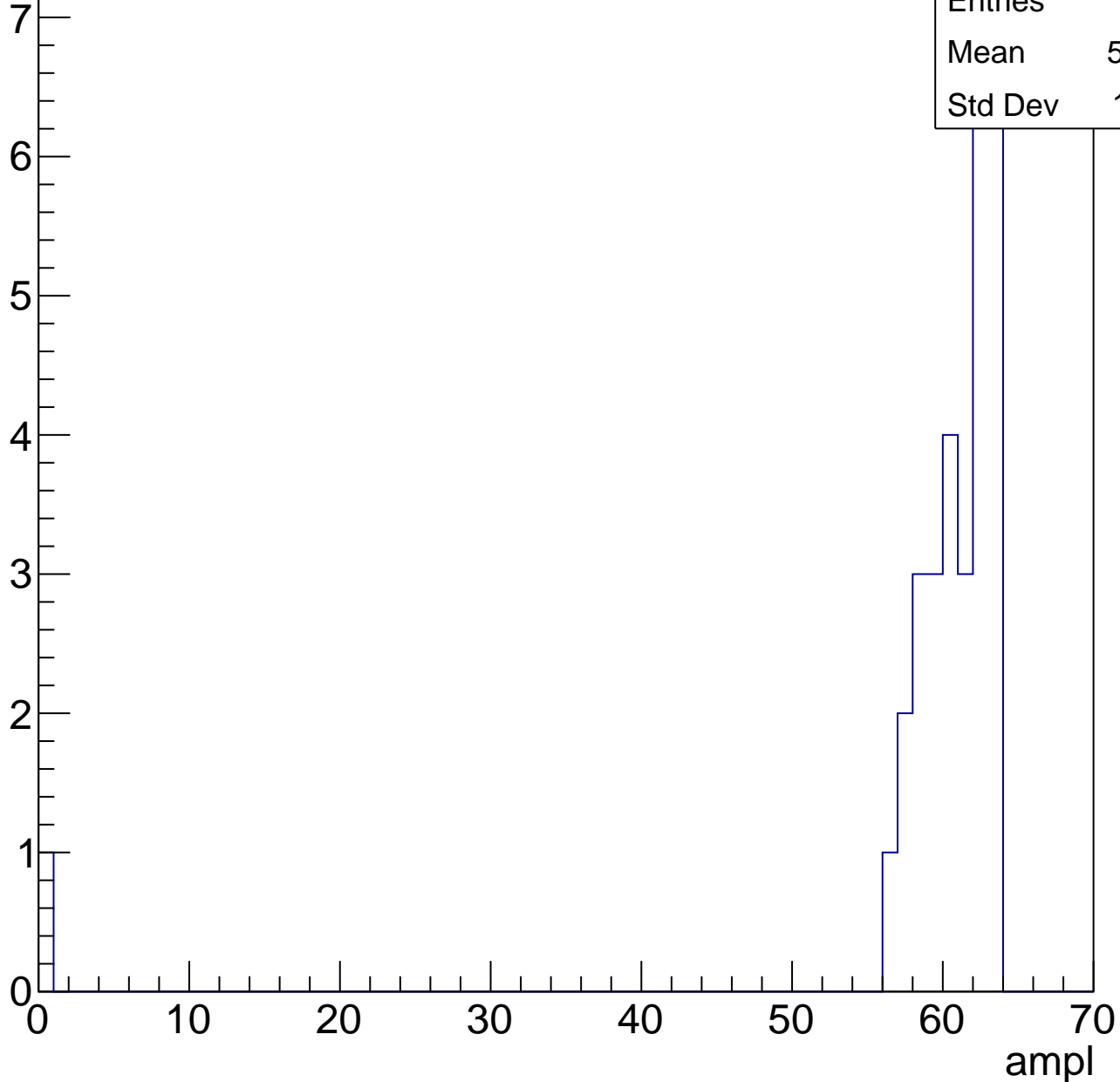


# B1L101S, U11-ch16, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	31
Mean	58.68
Std Dev	10.91



# B1L101S, U11-ch16, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch16, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U11-ch17, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	80
Mean	30.15
Std Dev	3.256

**Gaus mean : 30.5912**

**Gaus Width: 3.2255**

10

8

6

4

2

0

0

10

20

30

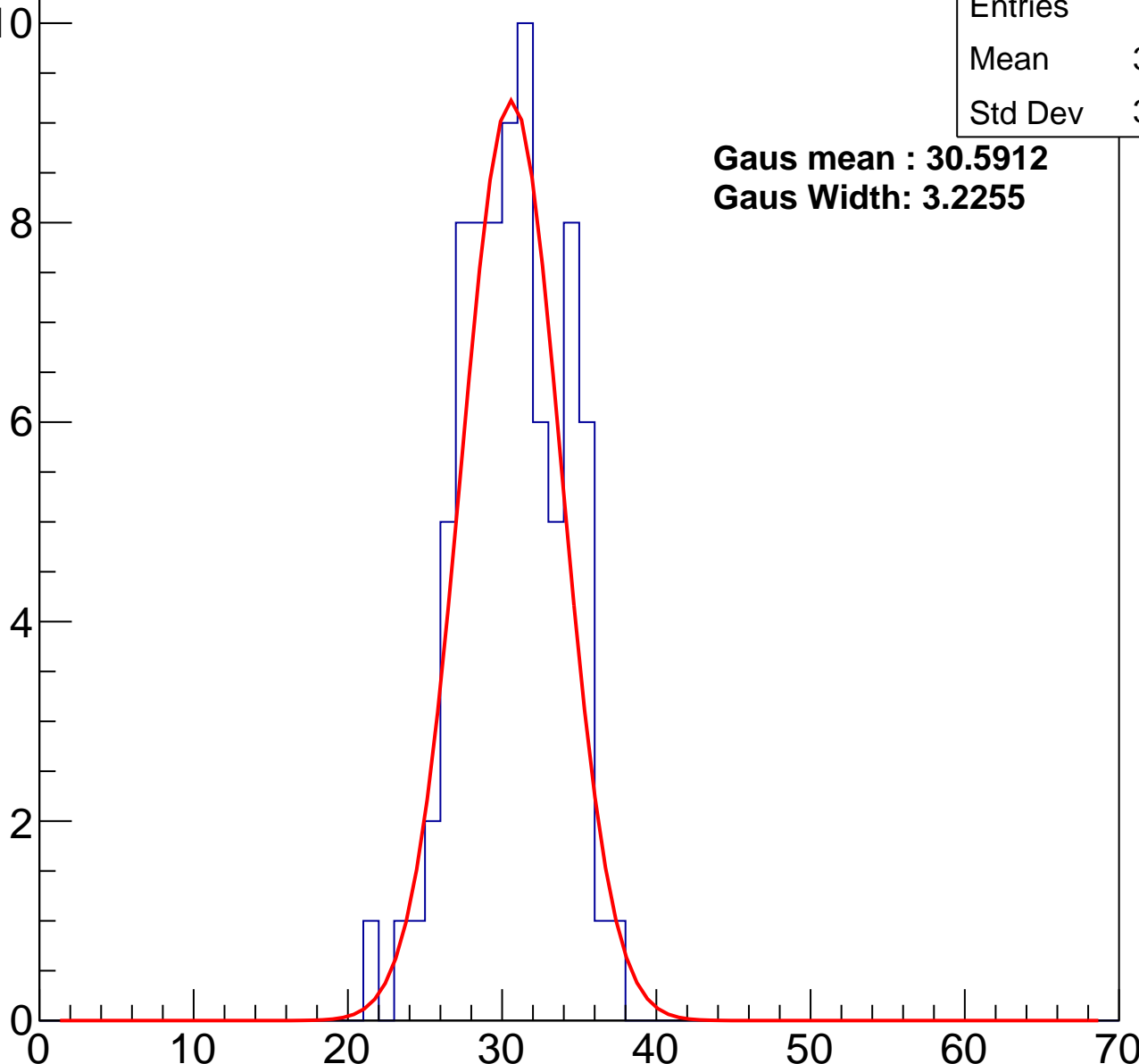
40

50

60

70

ampl



# B1L101S, U11-ch17, adc1

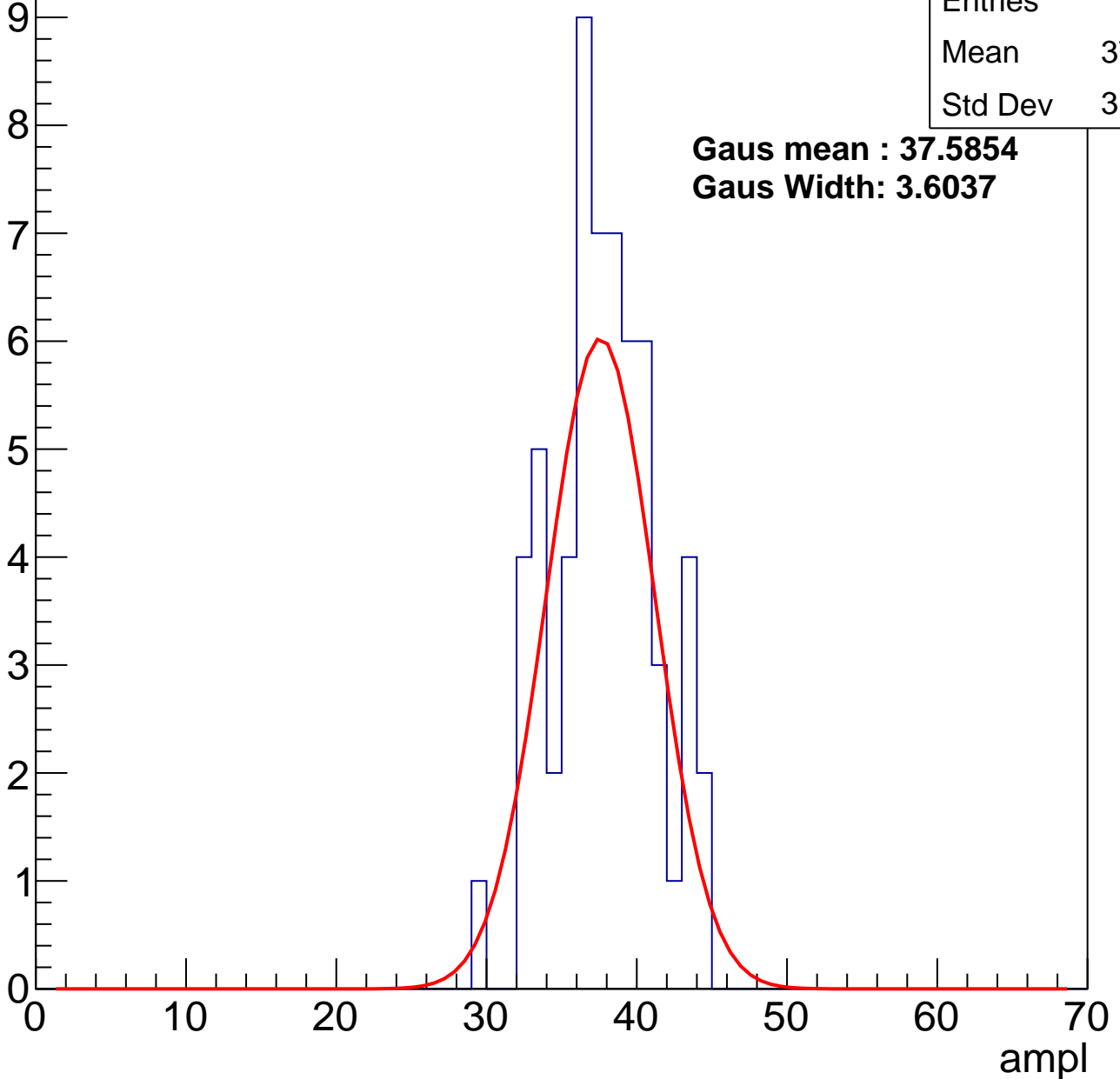
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	37.34
Std Dev	3.338

**Gaus mean : 37.5854**

**Gaus Width: 3.6037**



# B1L101S, U11-ch17, adc2

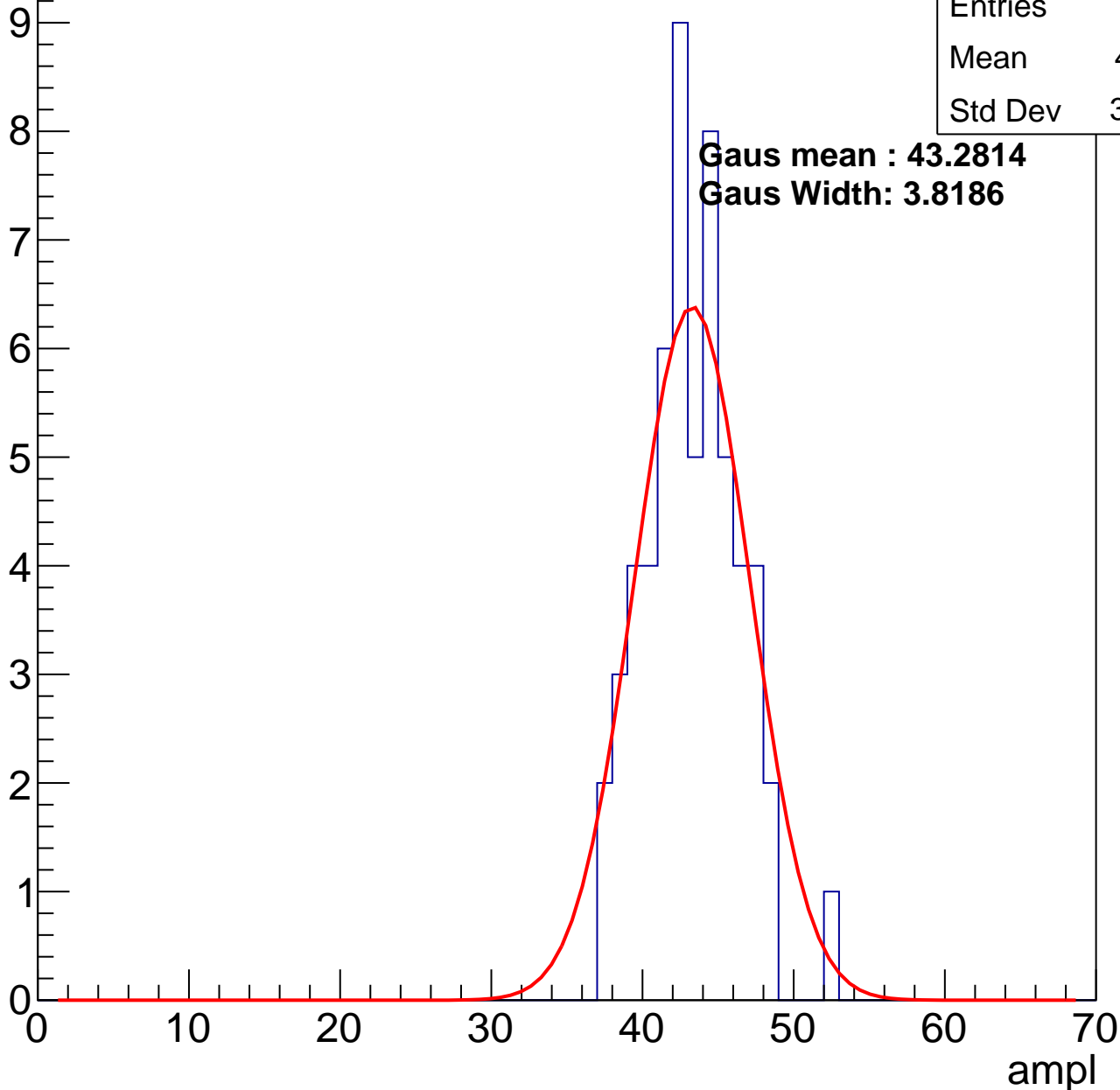
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	42.81
Std Dev	3.069

**Gaus mean : 43.2814**

**Gaus Width: 3.8186**

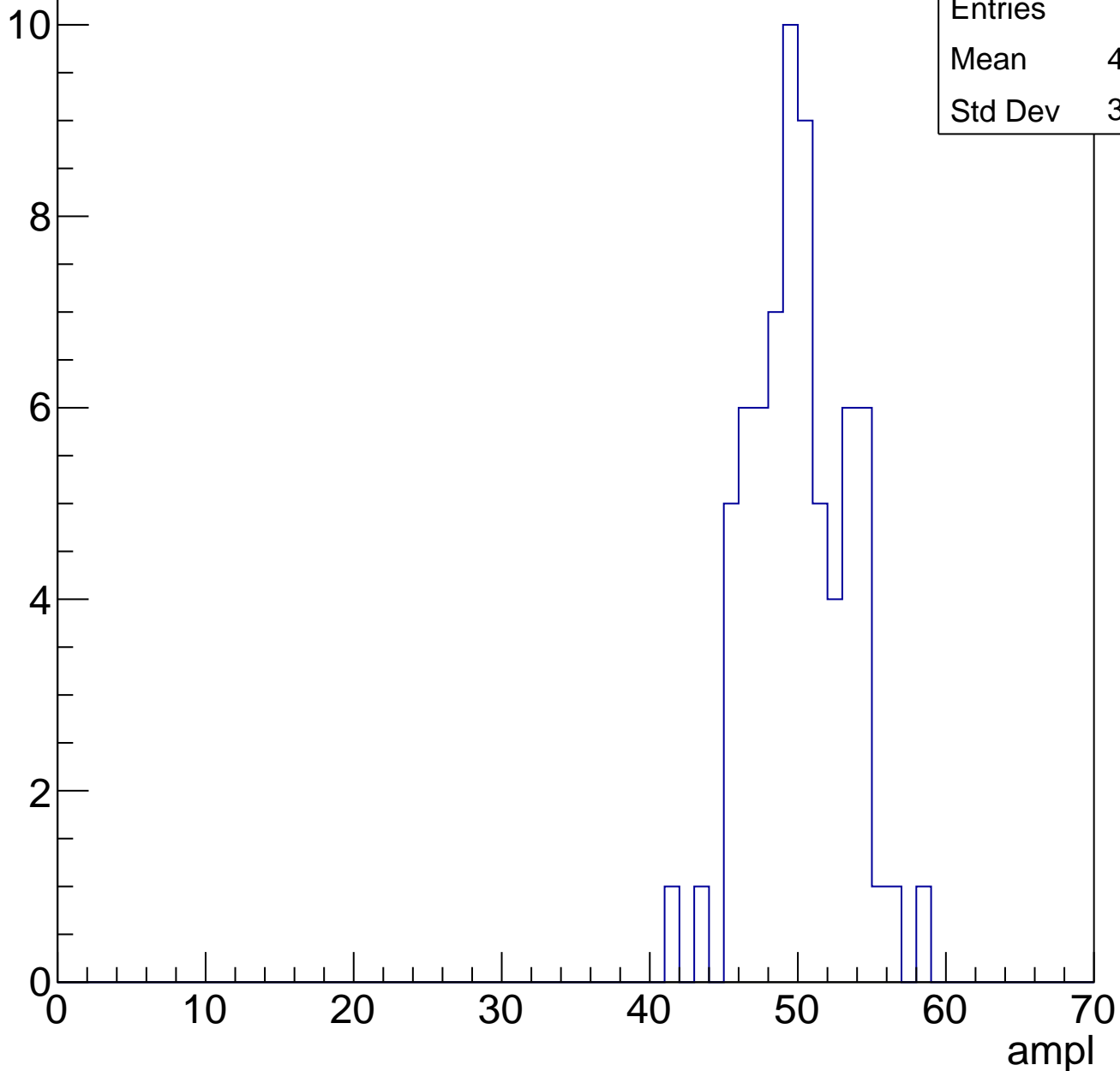


# B1L101S, U11-ch17, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	69
Mean	49.52
Std Dev	3.238

Entry

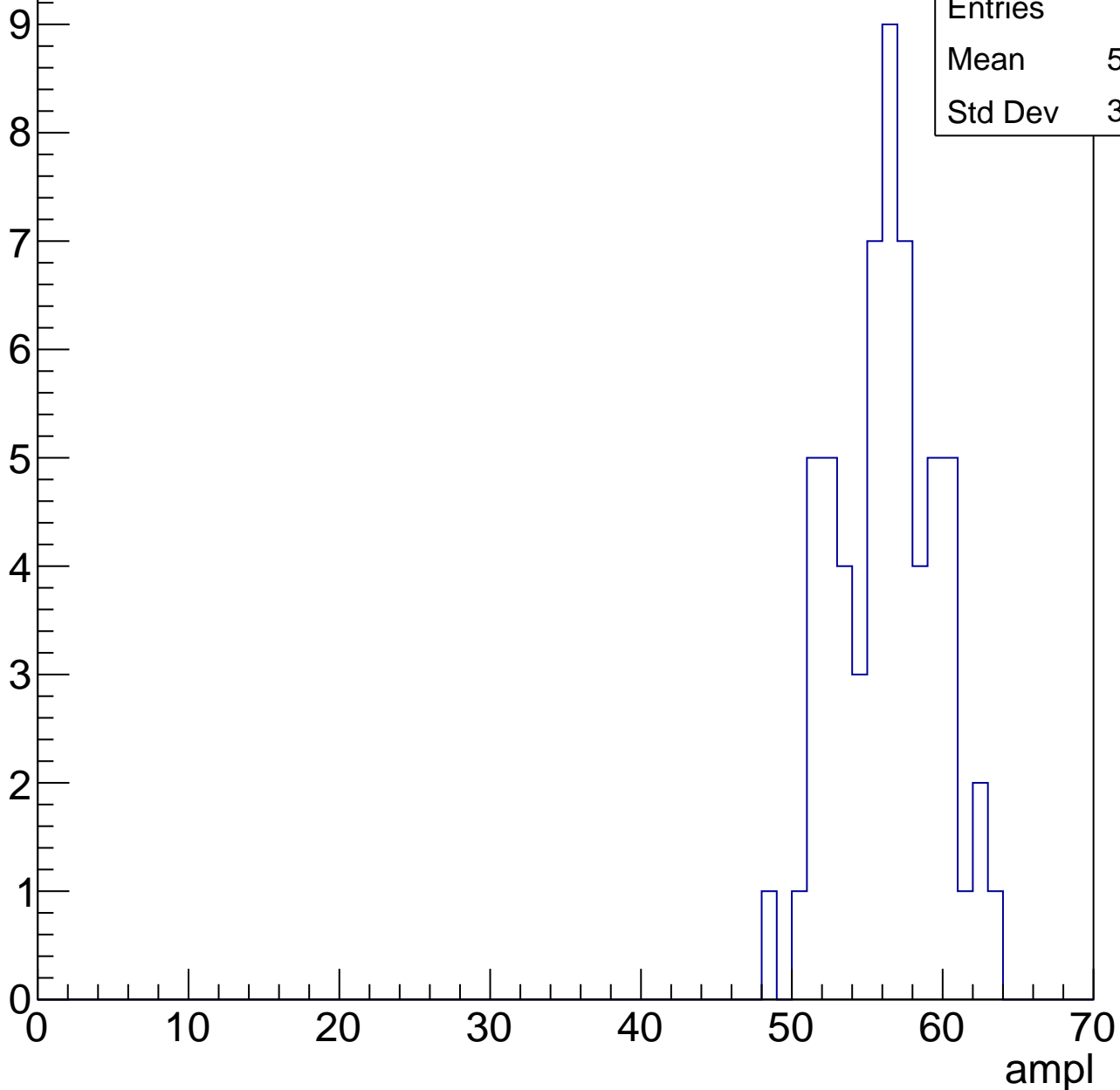


# B1L101S, U11-ch17, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	55.83
Std Dev	3.297

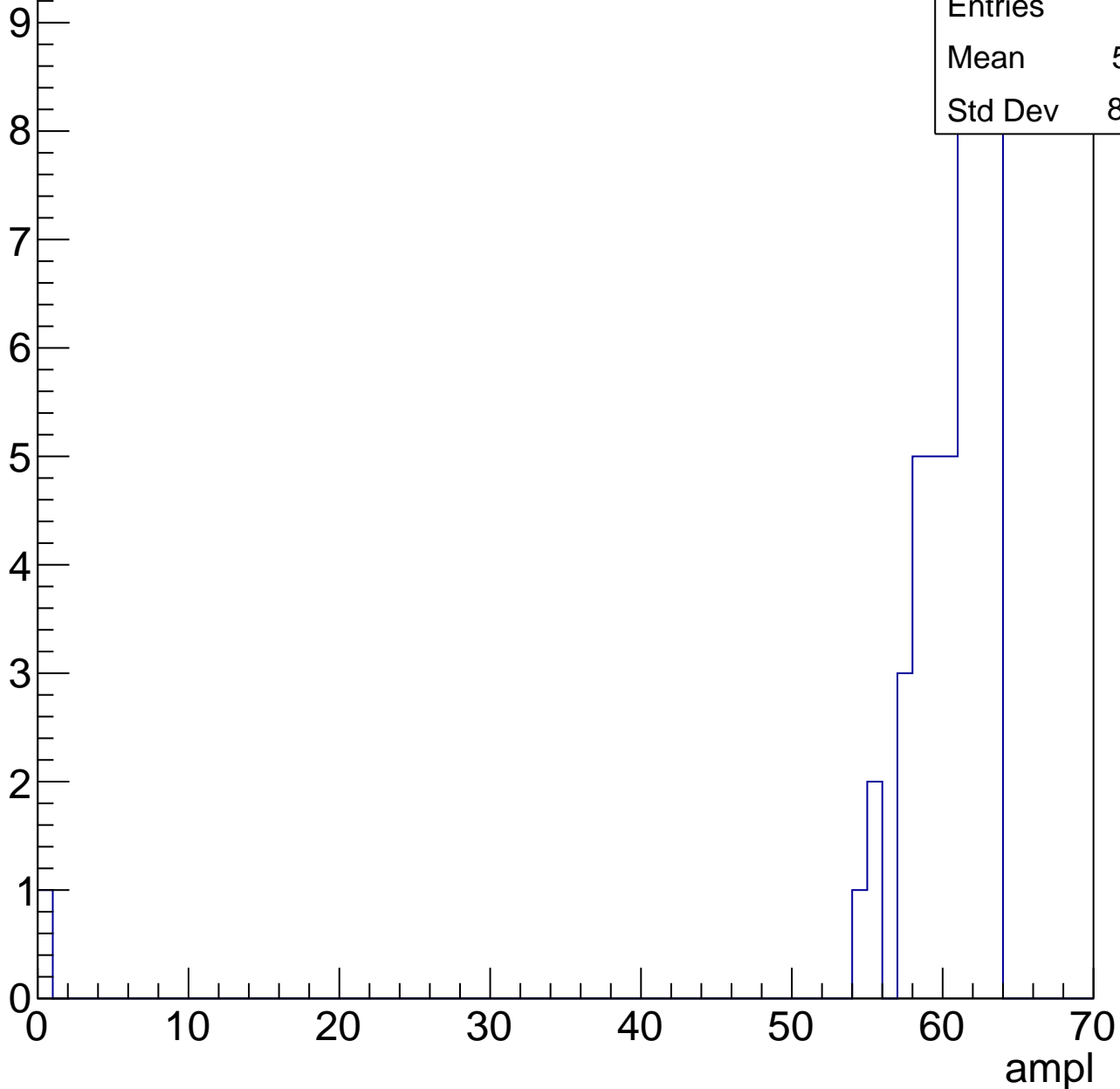


# B1L101S, U11-ch17, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	47
Mean	58.91
Std Dev	8.987



# B1L101S, U11-ch17, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch17, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U11-ch18, adc0

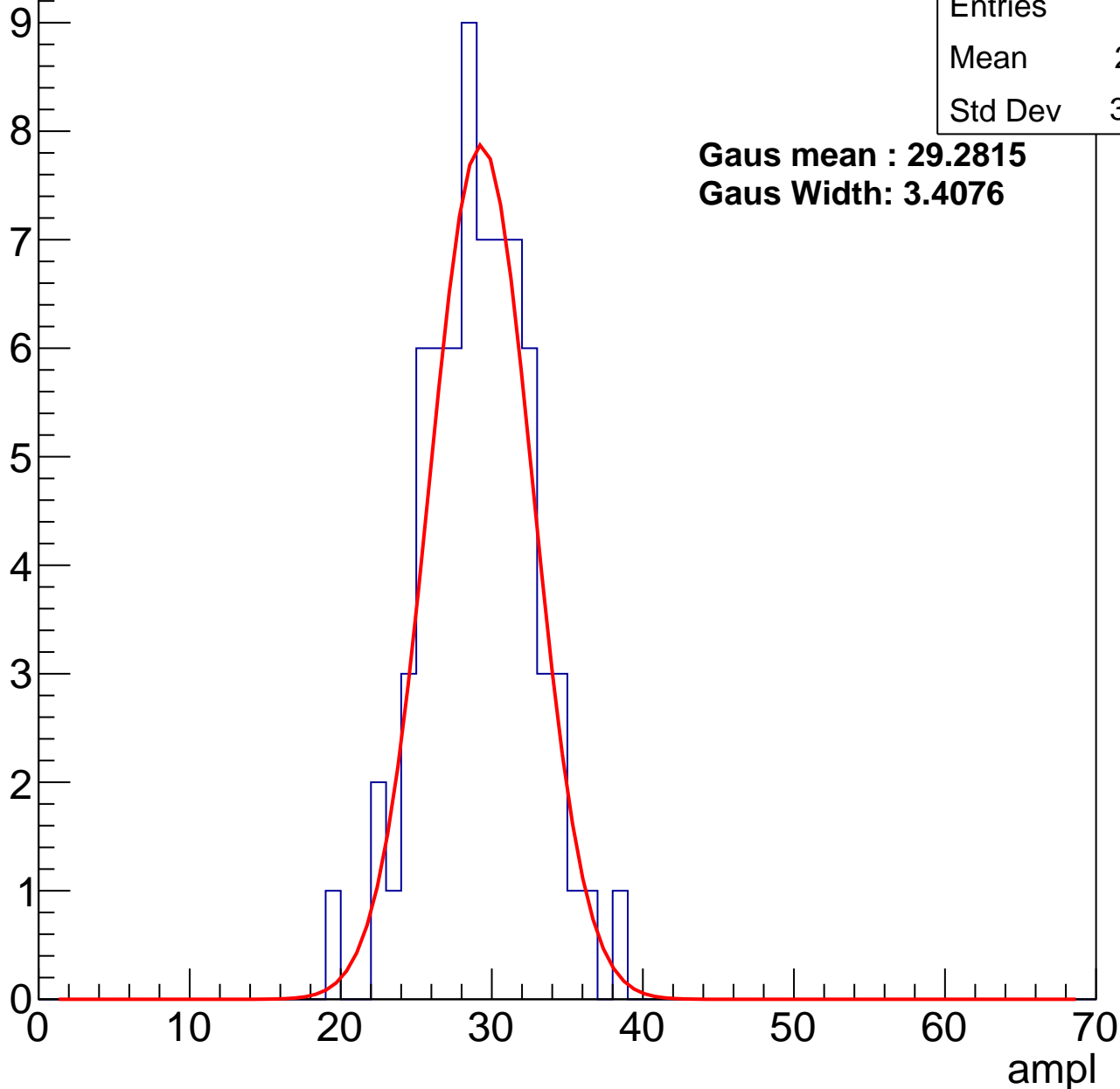
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	28.71
Std Dev	3.514

**Gaus mean : 29.2815**

**Gaus Width: 3.4076**



# B1L101S, U11-ch18, adc1

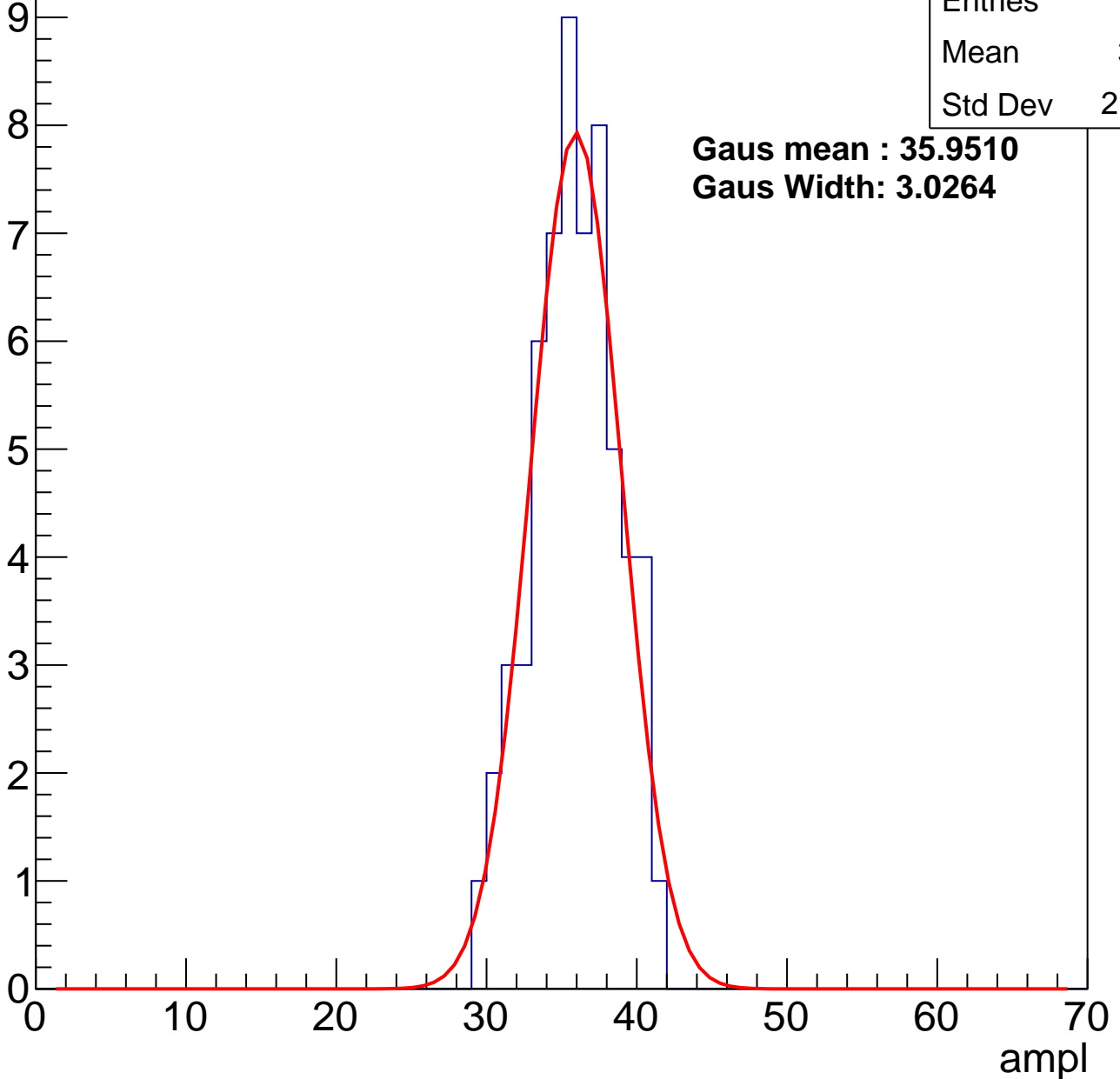
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	35.4
Std Dev	2.788

**Gaus mean : 35.9510**

**Gaus Width: 3.0264**



# B1L101S, U11-ch18, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	83
Mean	42.72
Std Dev	3.71

**Gaus mean : 43.0588**

**Gaus Width: 3.7885**

10

8

6

4

2

0

0

10

20

30

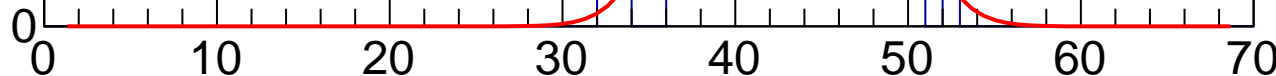
40

50

60

70

ampl

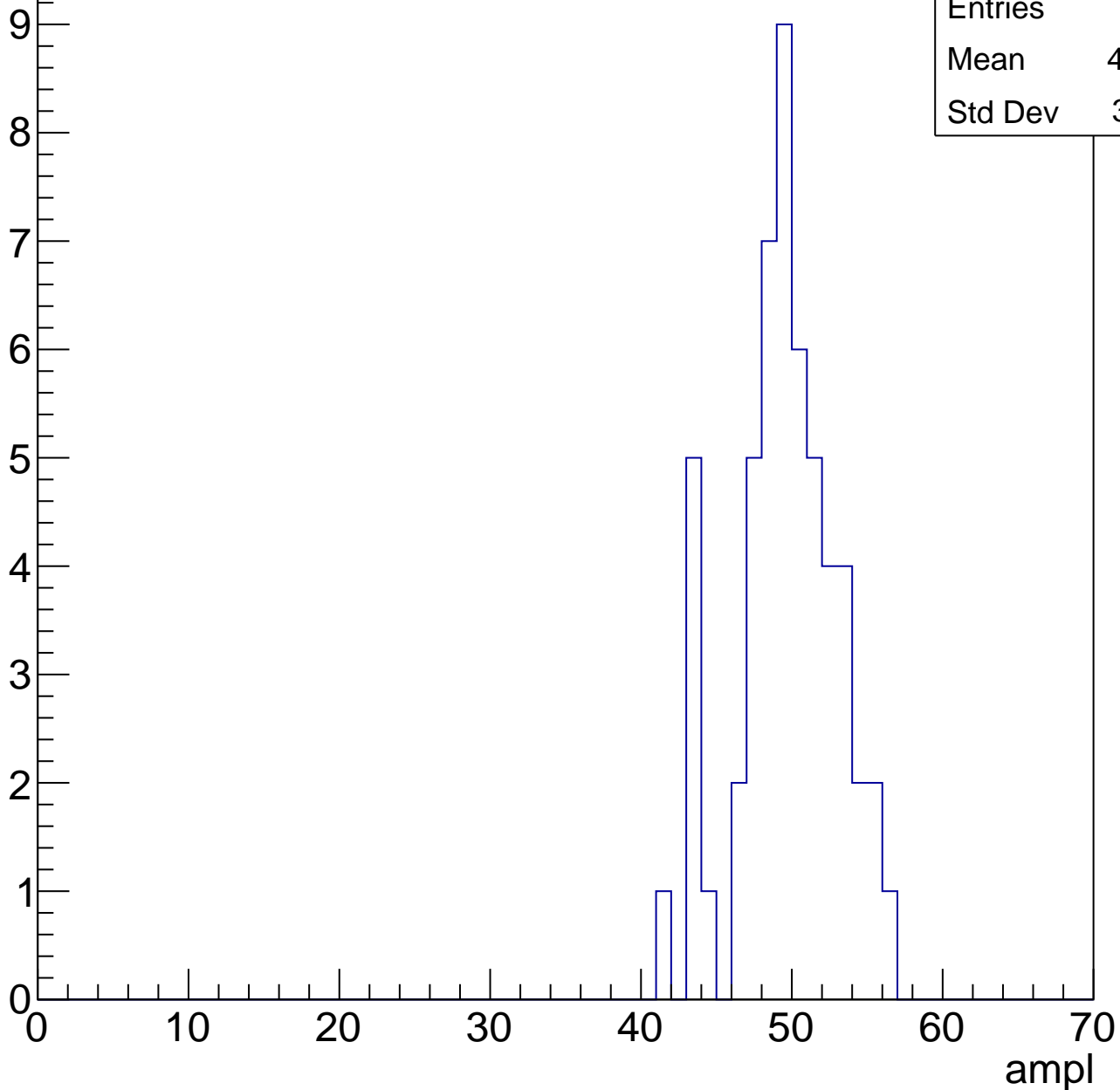


# B1L101S, U11-ch18, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	49.13
Std Dev	3.361

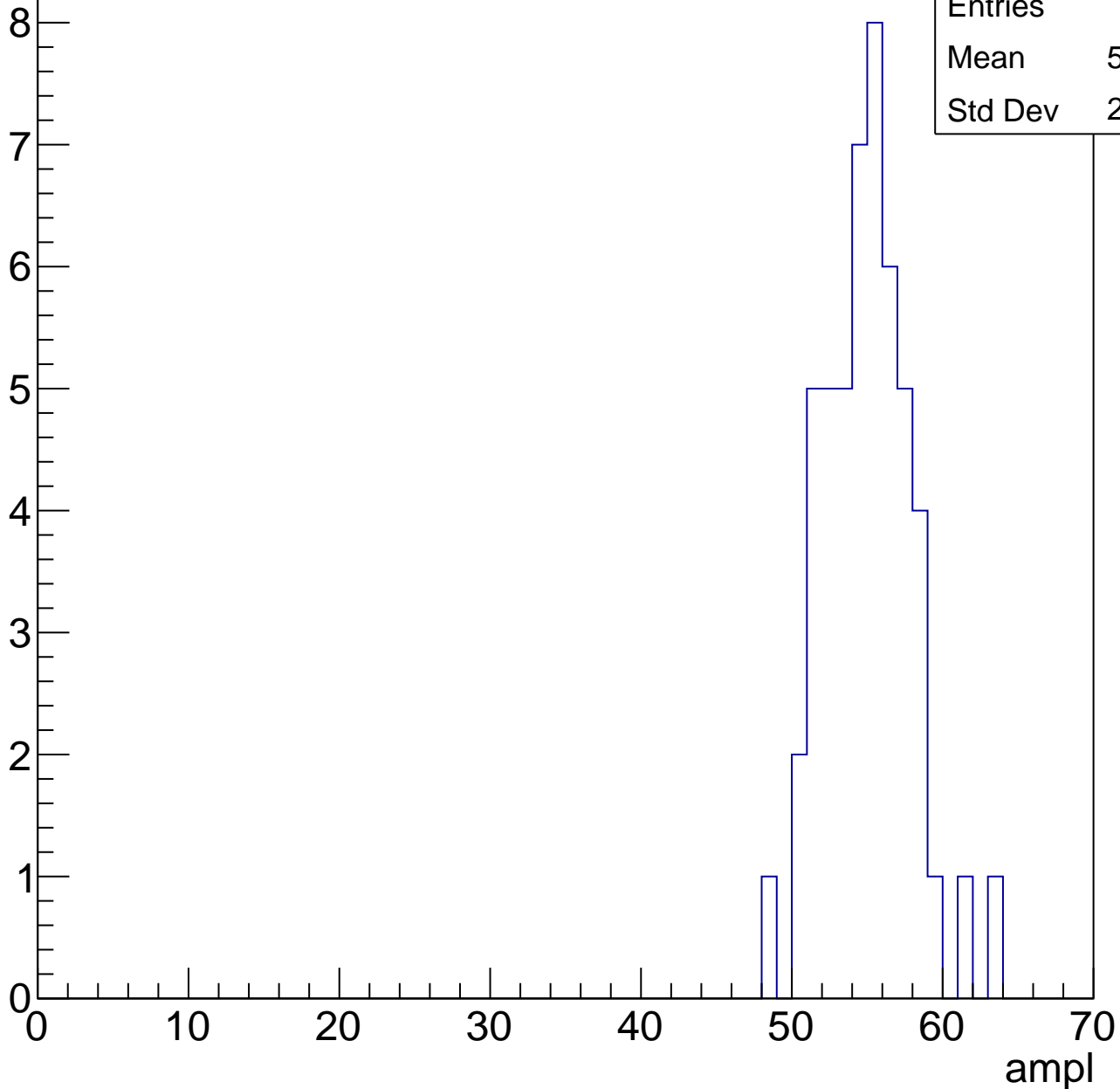


# B1L101S, U11-ch18, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	54.55
Std Dev	2.865



# B1L101S, U11-ch18, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

70

ampl

Entries

54

Mean

59.52

Std Dev

2.25

1

2

3

4

5

6

7

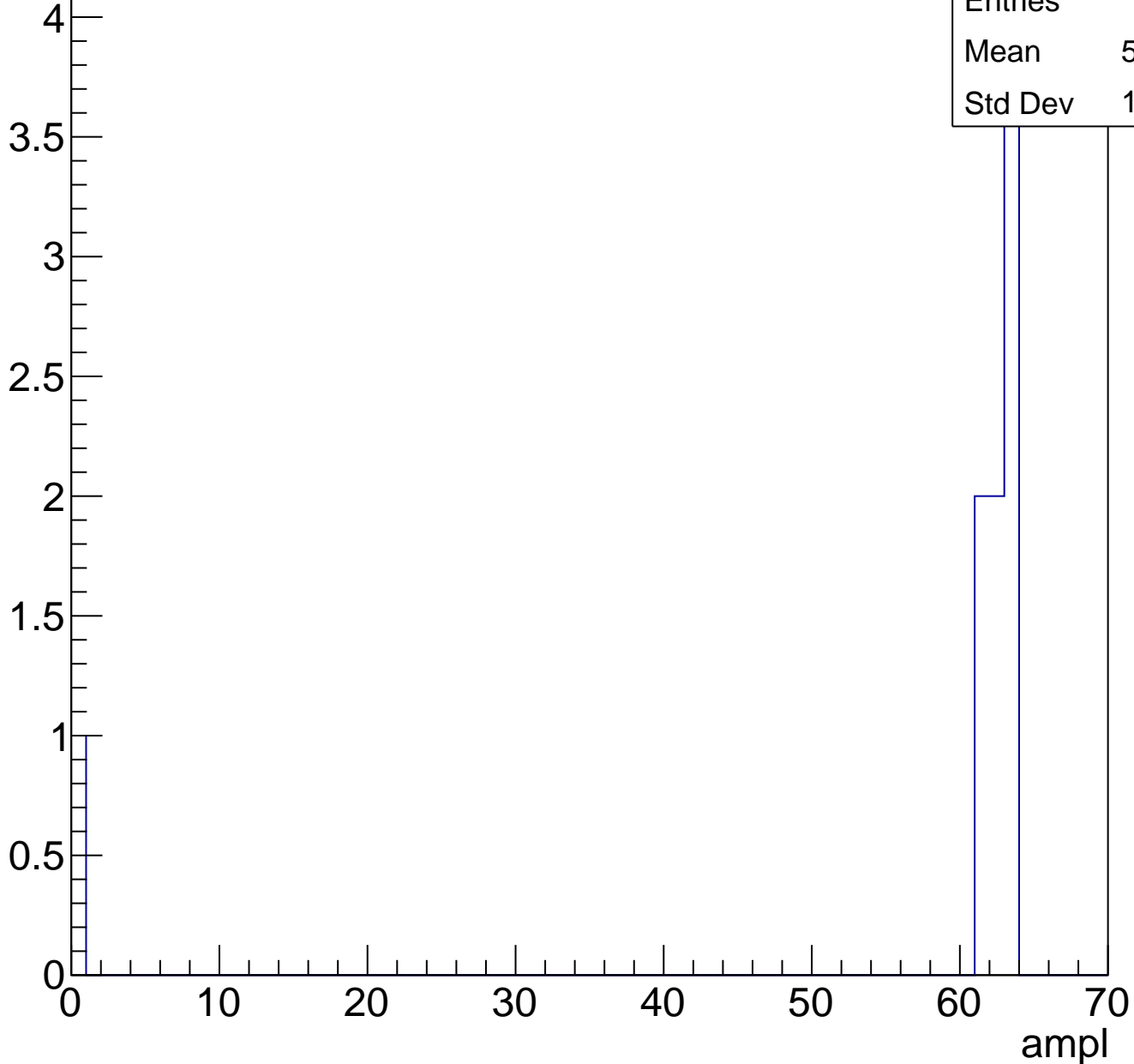
8

9

# B1L101S, U11-ch18, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch18, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U11-ch19, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	69
Mean	30.46
Std Dev	4.968

**Gaus mean : 31.3408**

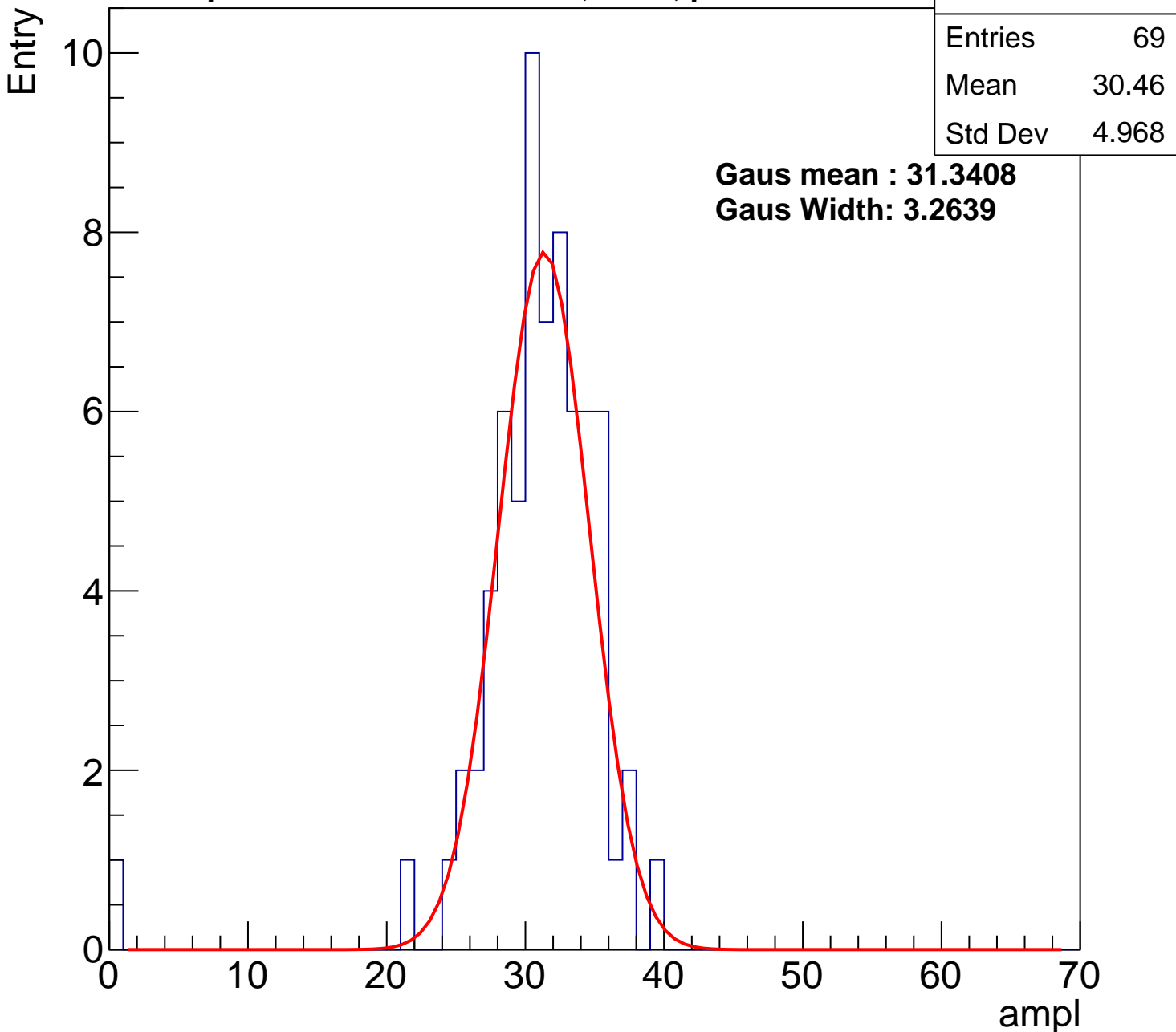
**Gaus Width: 3.2639**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



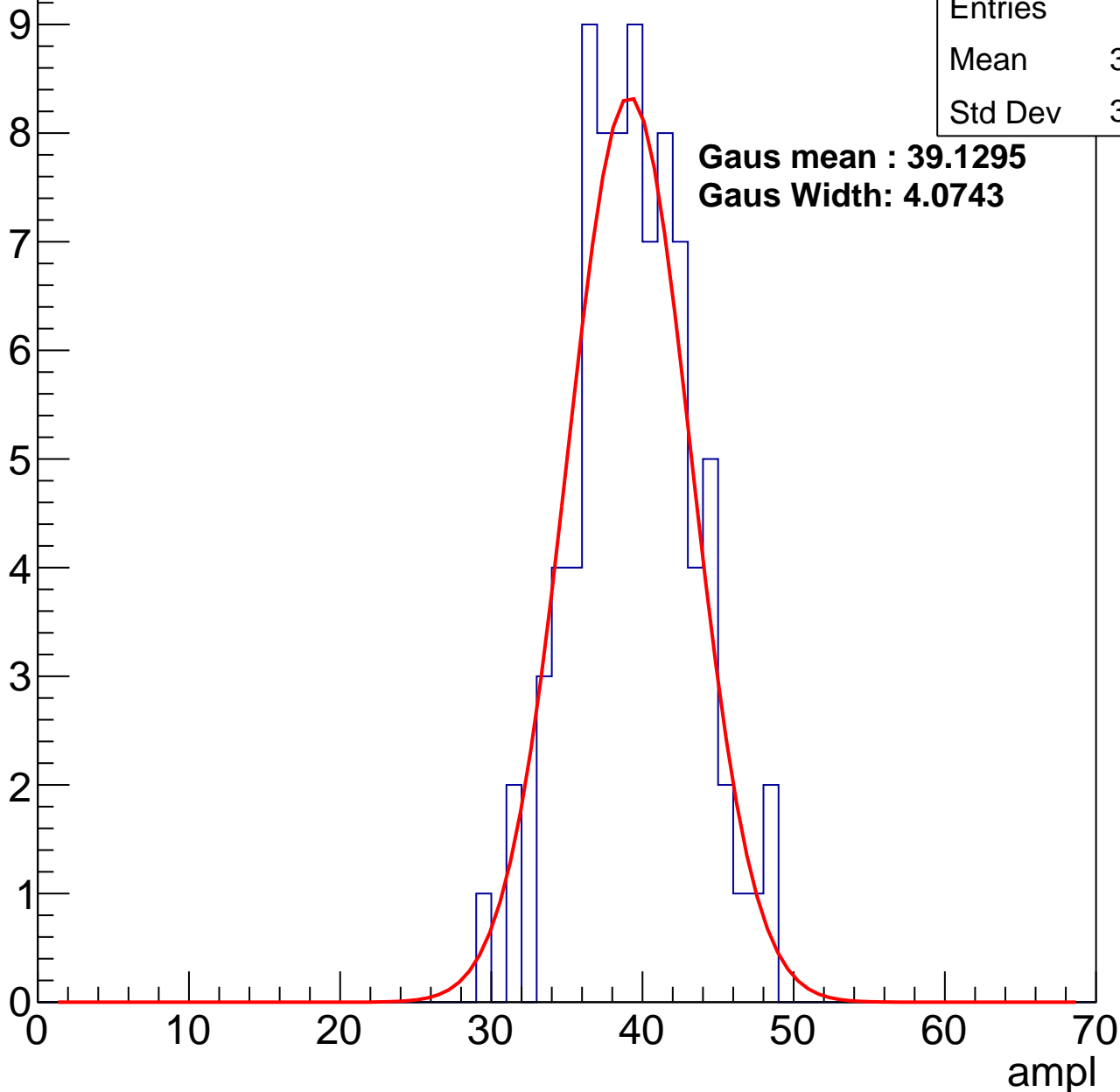
# B1L101S, U11-ch19, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	85
Mean	38.99
Std Dev	3.849

**Gaus mean : 39.1295**  
**Gaus Width: 4.0743**



# B1L101S, U11-ch19, adc2

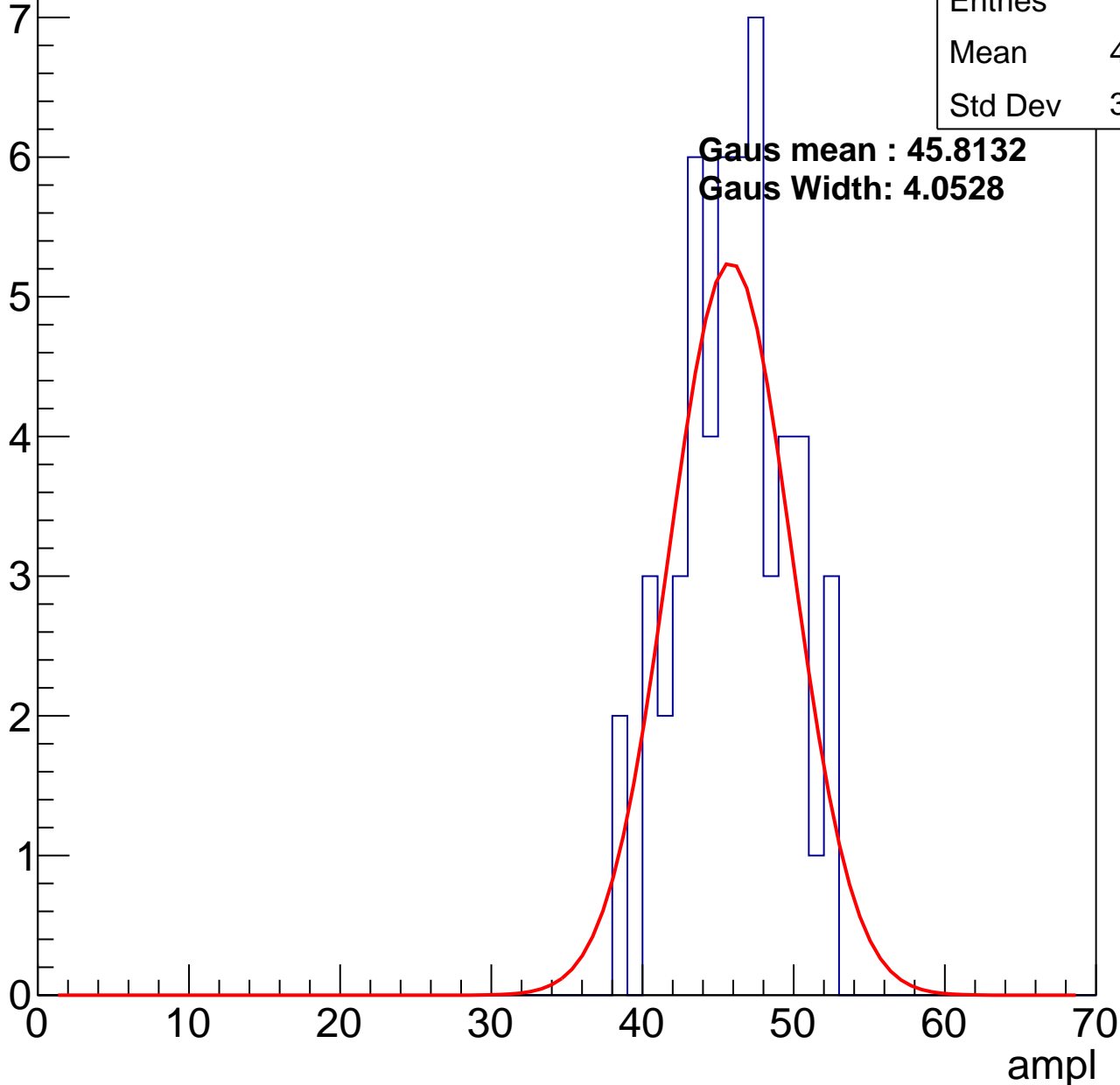
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	45.56
Std Dev	3.473

**Gaus mean : 45.8132**

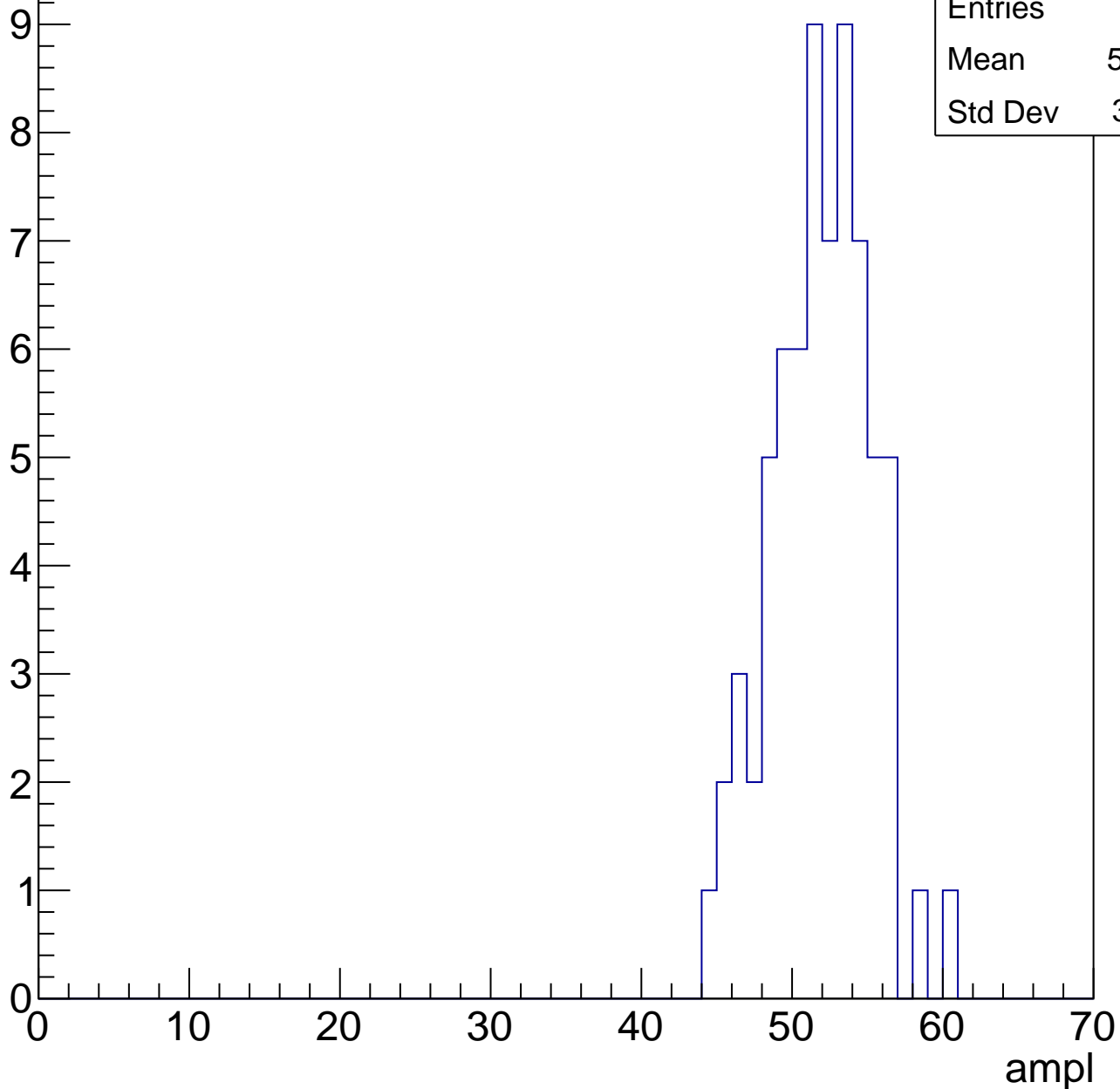
**Gaus Width: 4.0528**



# B1L101S, U11-ch19, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

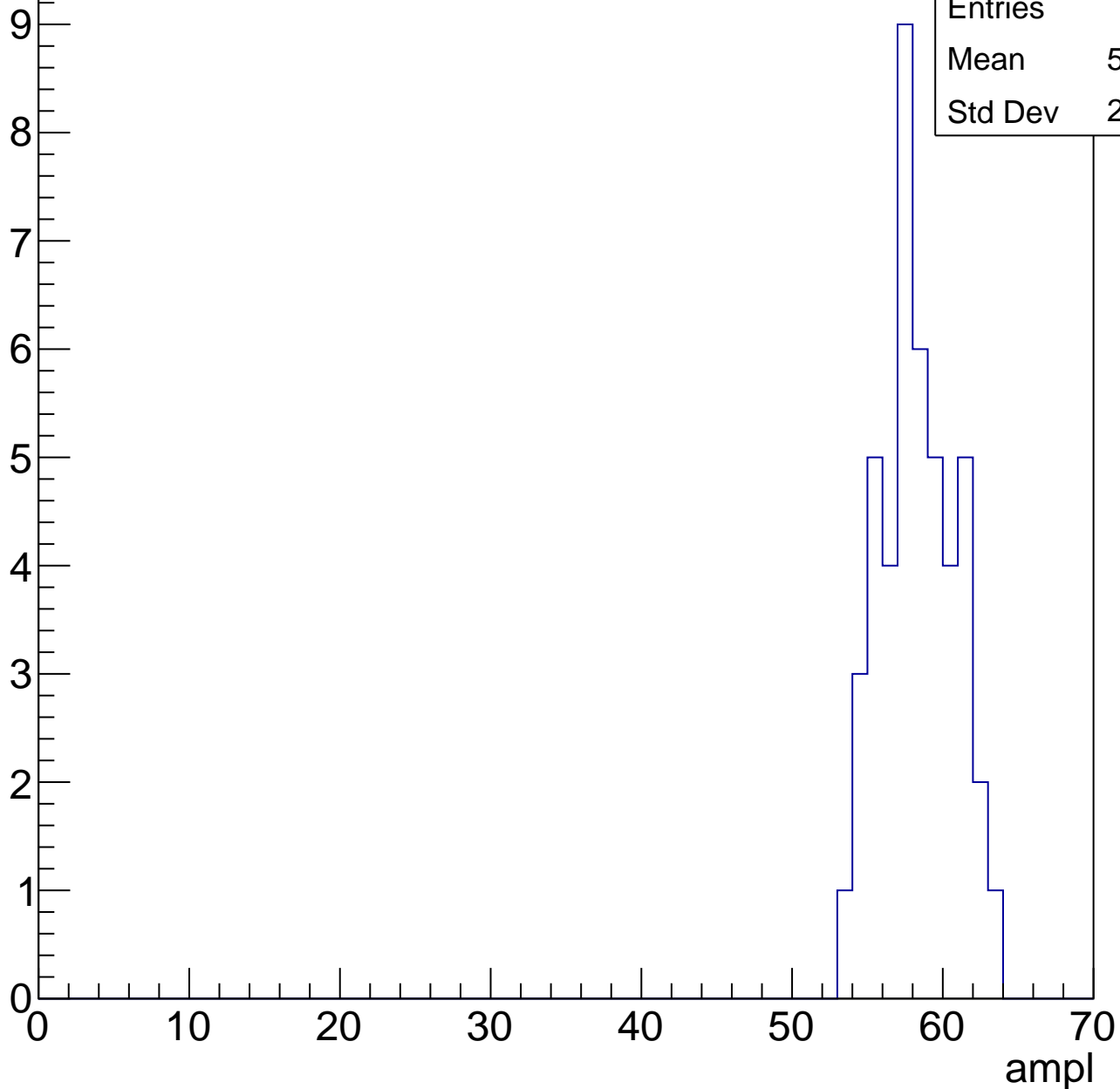
Entry



# B1L101S, U11-ch19, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



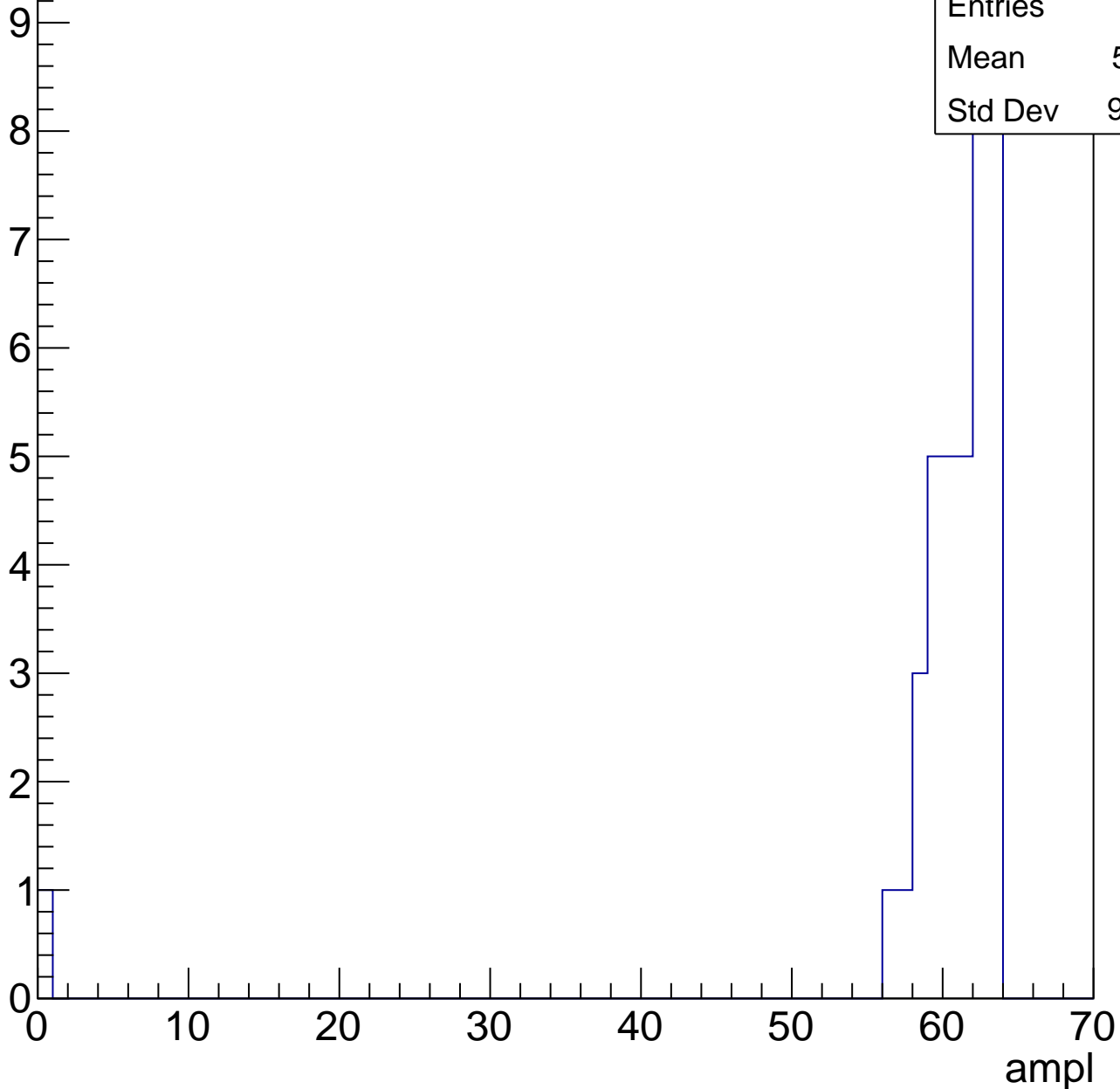
Entries	45
Mean	57.82
Std Dev	2.425

# B1L101S, U11-ch19, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	38
Mean	59.21
Std Dev	9.916



# B1L101S, U11-ch19, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch19, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U11-ch20, adc0

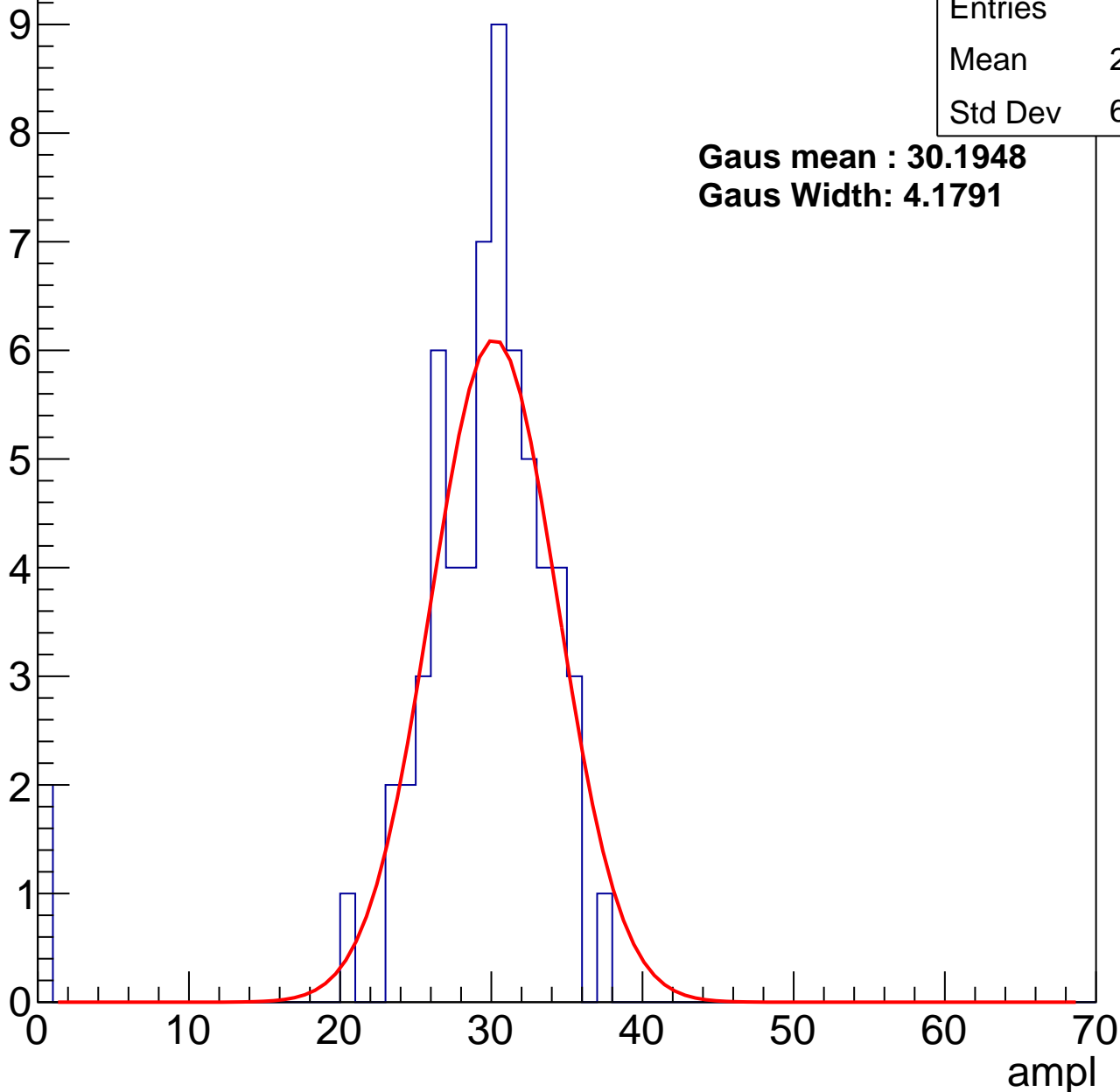
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	28.48
Std Dev	6.177

**Gaus mean : 30.1948**

**Gaus Width: 4.1791**



# B1L101S, U11-ch20, adc1

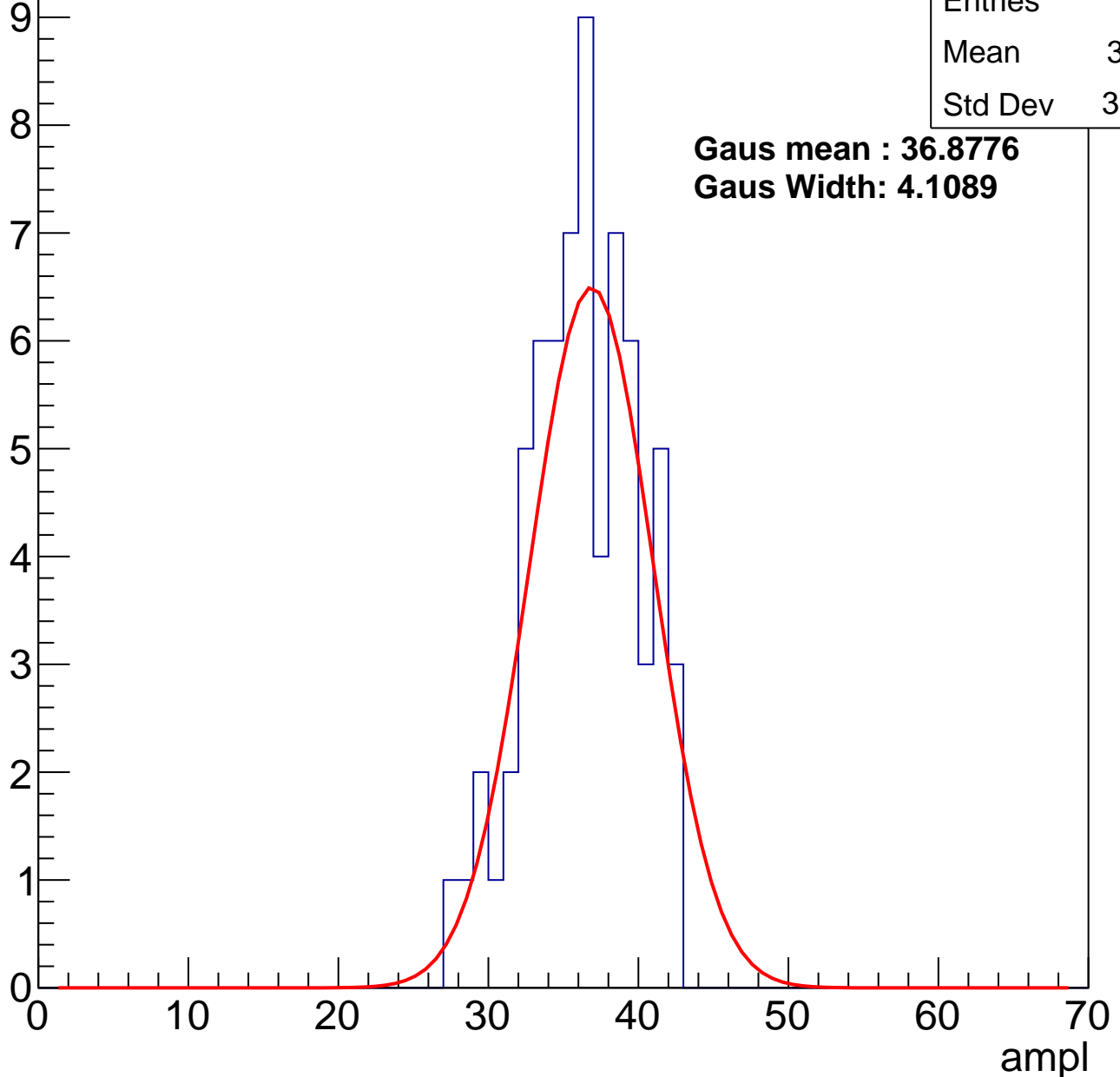
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	35.81
Std Dev	3.553

**Gaus mean : 36.8776**

**Gaus Width: 4.1089**



# B1L101S, U11-ch20, adc2

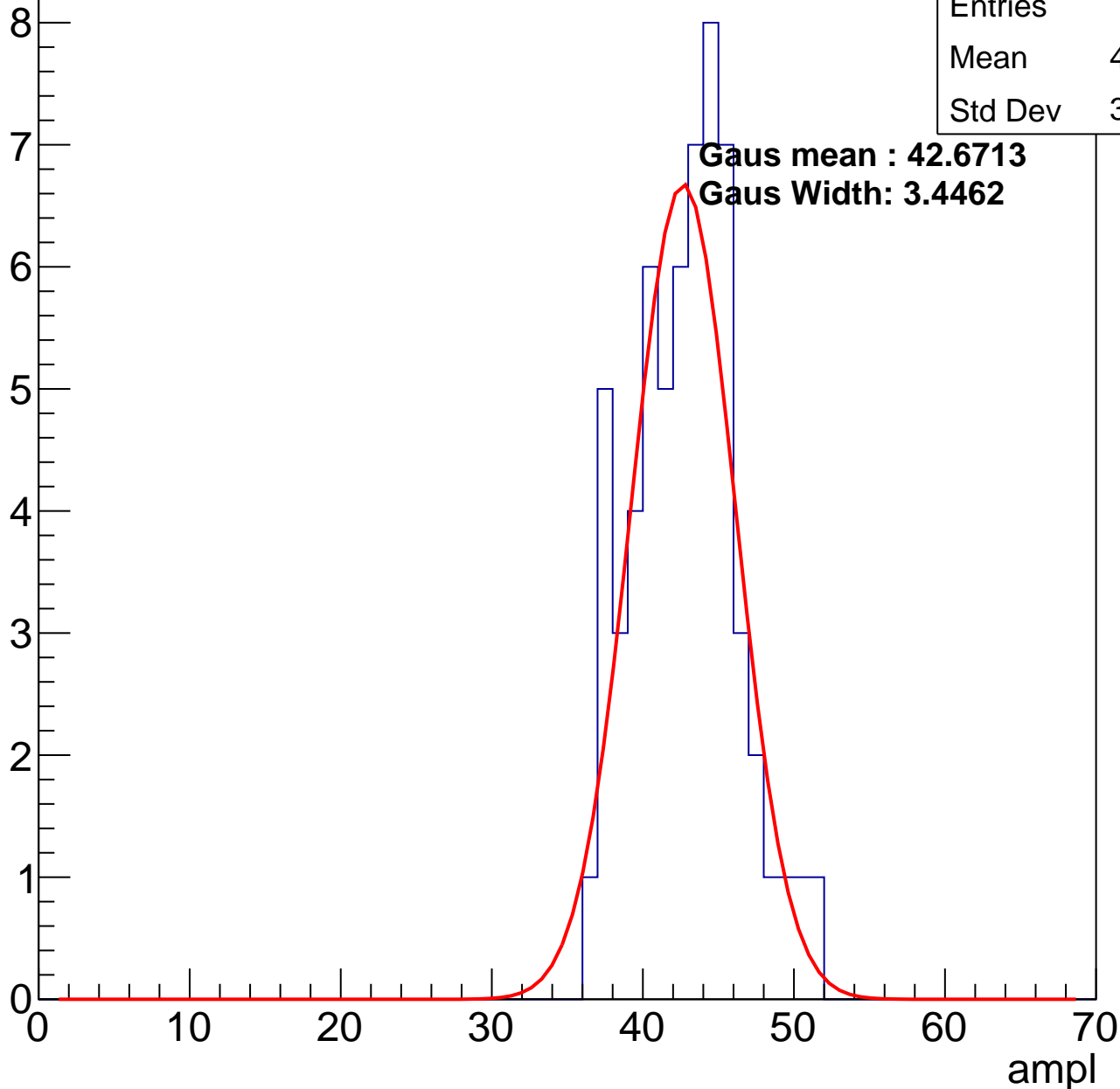
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	42.39
Std Dev	3.374

**Gaus mean : 42.6713**

**Gaus Width: 3.4462**

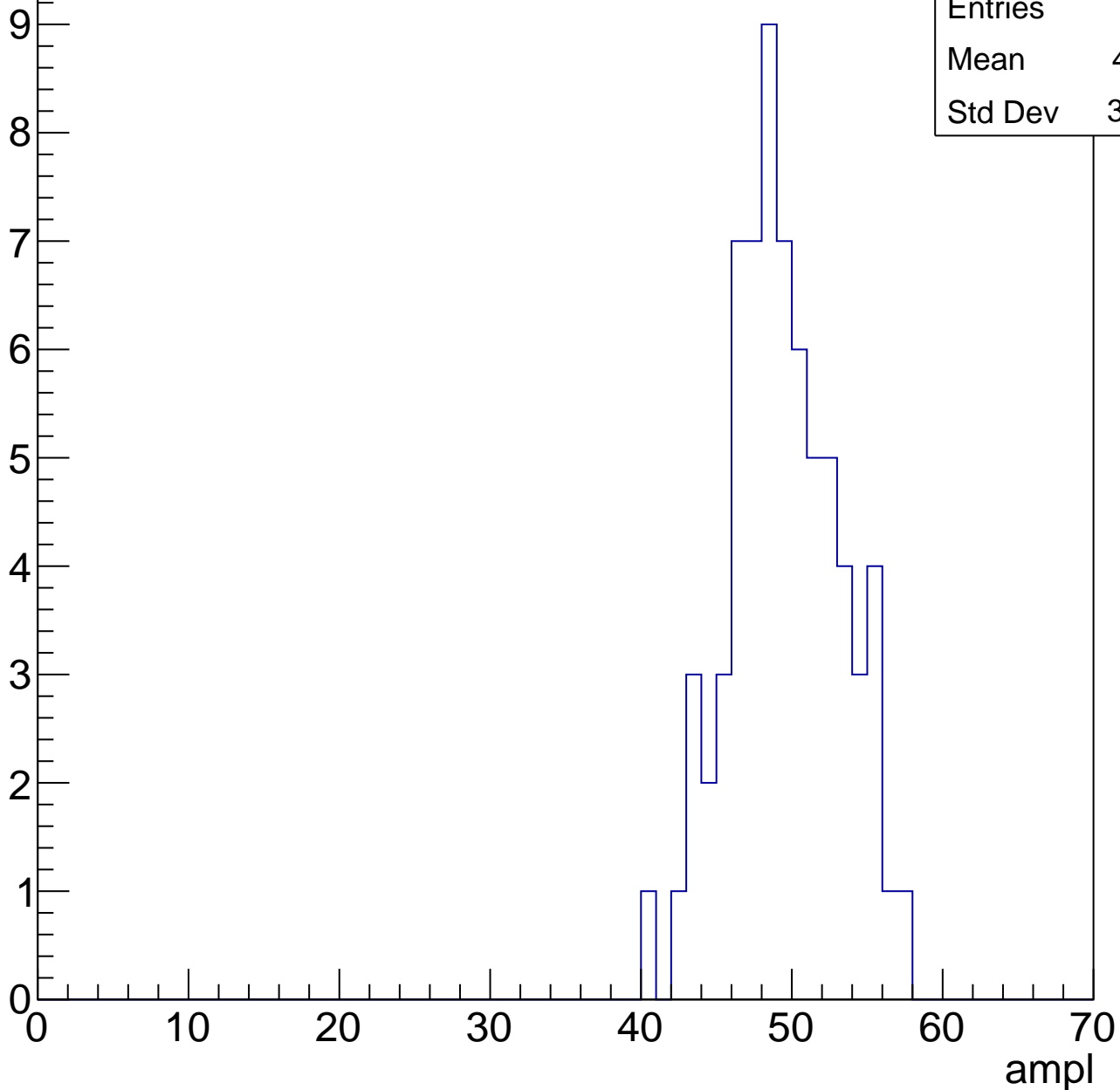


# B1L101S, U11-ch20, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	49.01
Std Dev	3.618

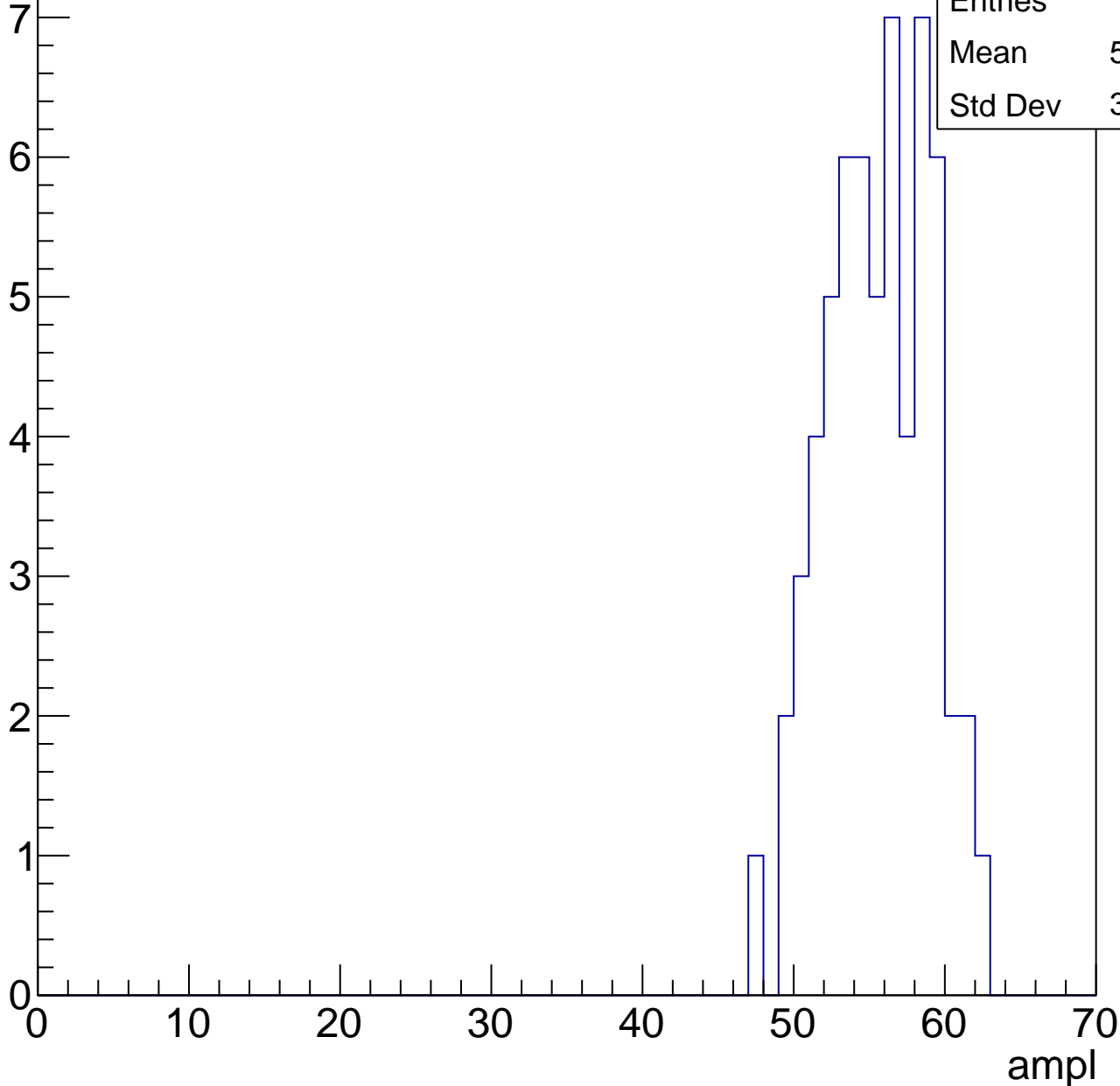


# B1L101S, U11-ch20, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	55.08
Std Dev	3.394



# B1L101S, U11-ch20, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	45
Mean	60.02
Std Dev	2.408

ampl

0 10 20 30 40 50 60 70

0

1

2

3

4

5

6

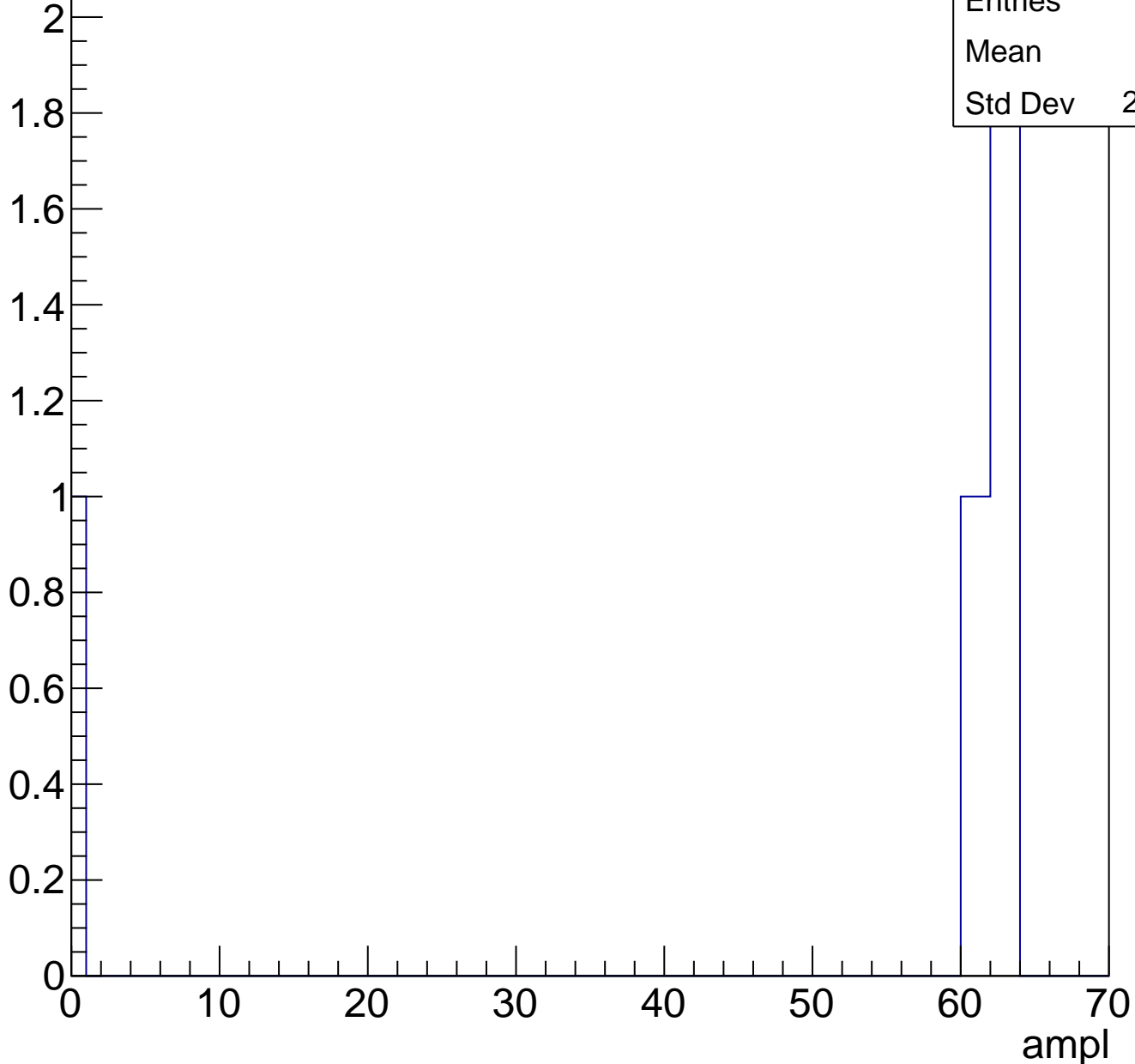
7

8

# B1L101S, U11-ch20, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch20, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U11-ch21, adc0

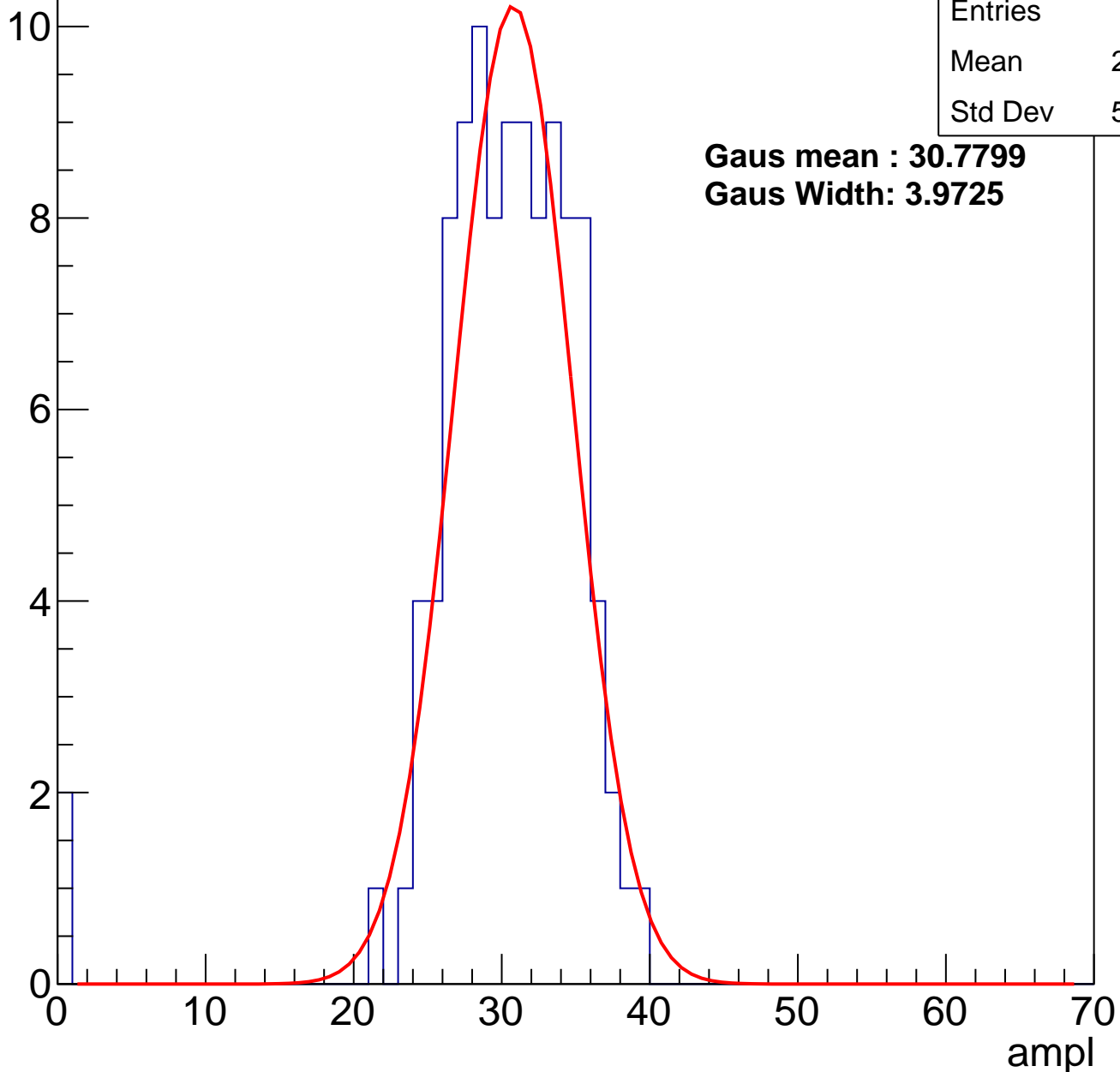
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	106
Mean	29.74
Std Dev	5.546

**Gaus mean : 30.7799**

**Gaus Width: 3.9725**

Entry



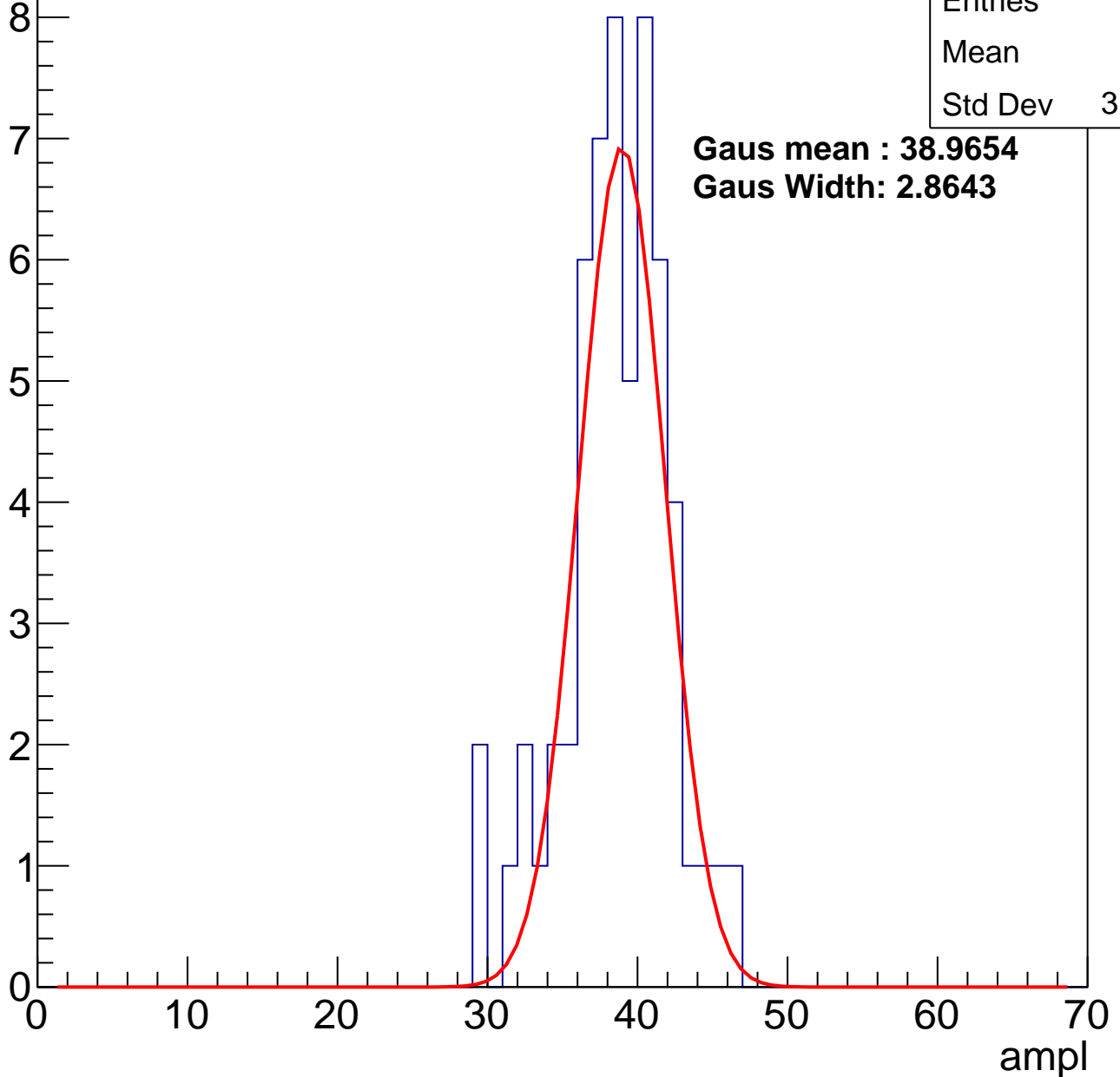
# B1L101S, U11-ch21, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	38.1
Std Dev	3.517

**Gaus mean : 38.9654**  
**Gaus Width: 2.8643**



# B1L101S, U11-ch21, adc2

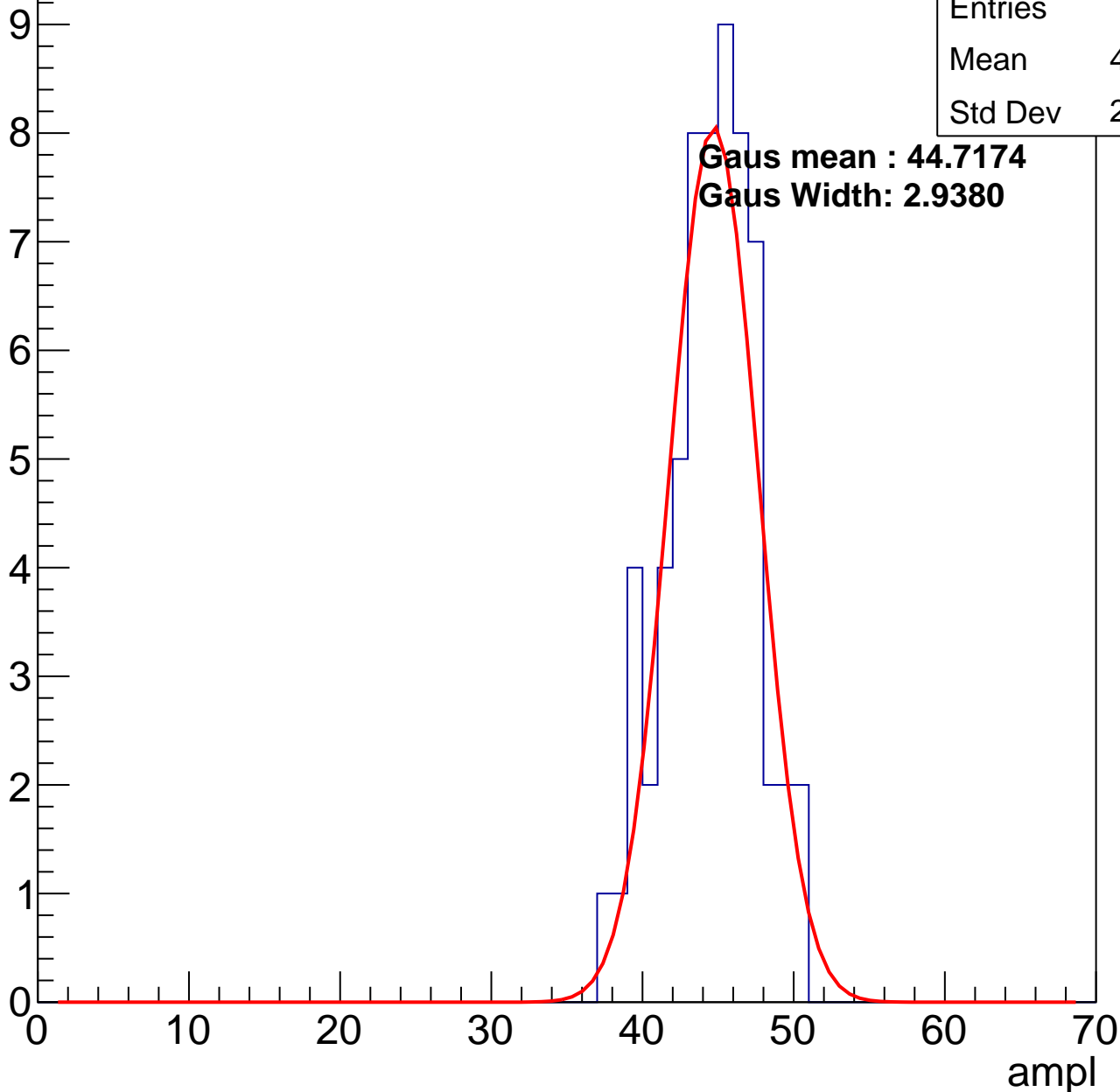
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	44.08
Std Dev	2.924

**Gaus mean : 44.7174**

**Gaus Width: 2.9380**

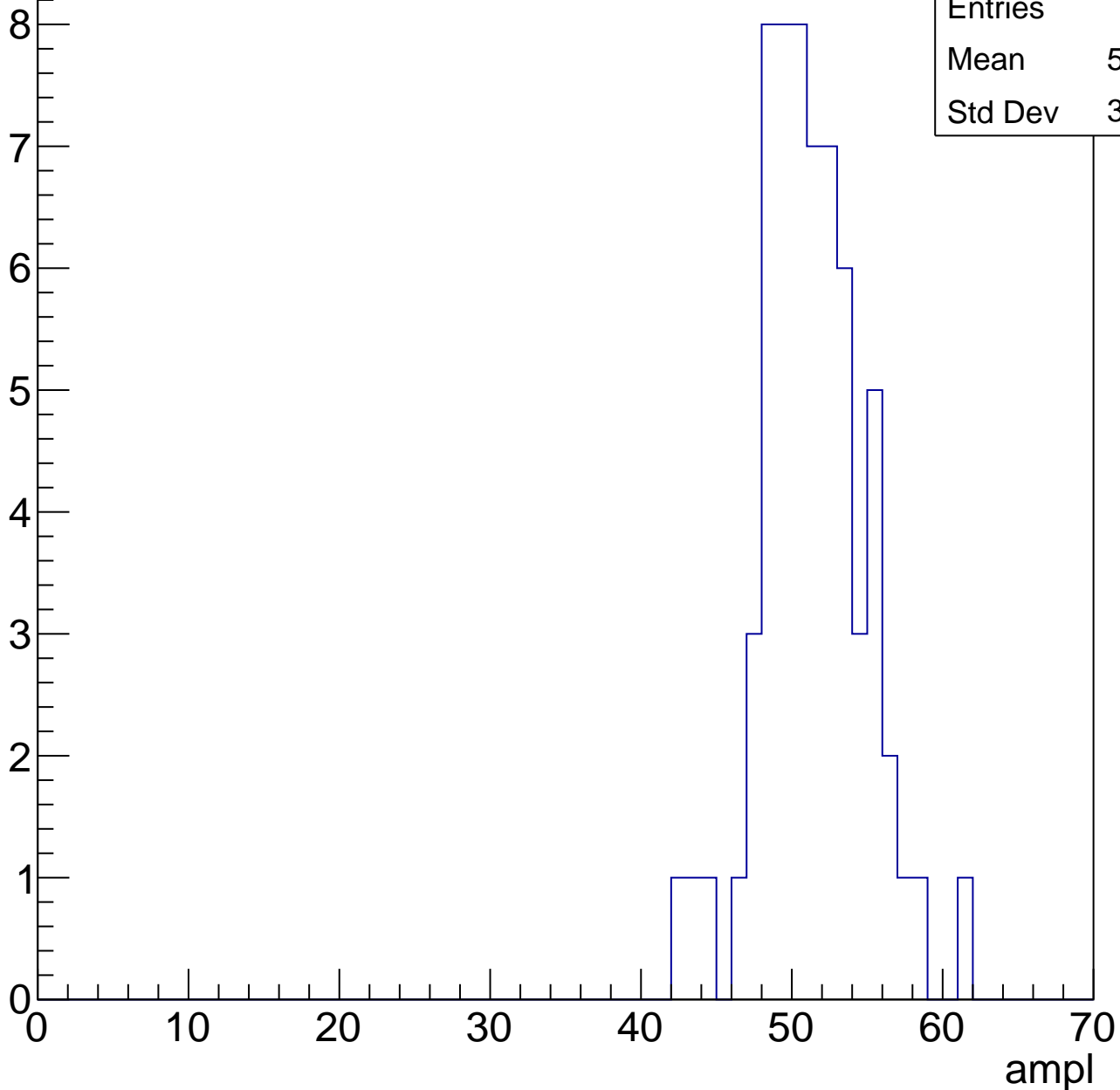


# B1L101S, U11-ch21, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

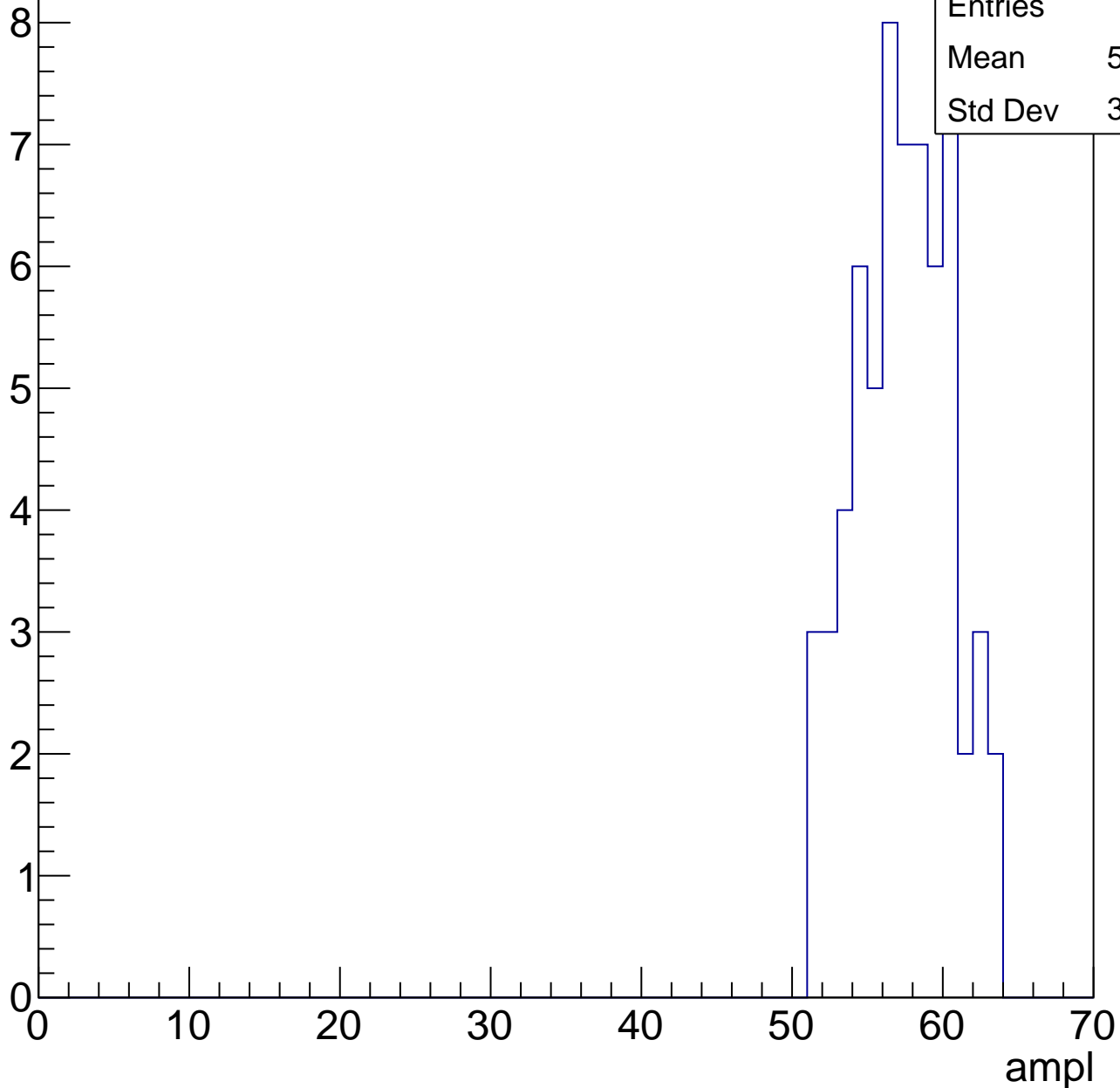
Entries	64
Mean	50.88
Std Dev	3.426



# B1L101S, U11-ch21, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	64
Mean	56.89
Std Dev	3.088

# B1L101S, U11-ch21, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

7

6

5

4

3

2

1

0

Entries	30
Mean	58.6
Std Dev	11.09

ampl

0

10

20

30

40

50

60

70

# B1L101S, U11-ch21, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch21, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U11-ch22, adc0

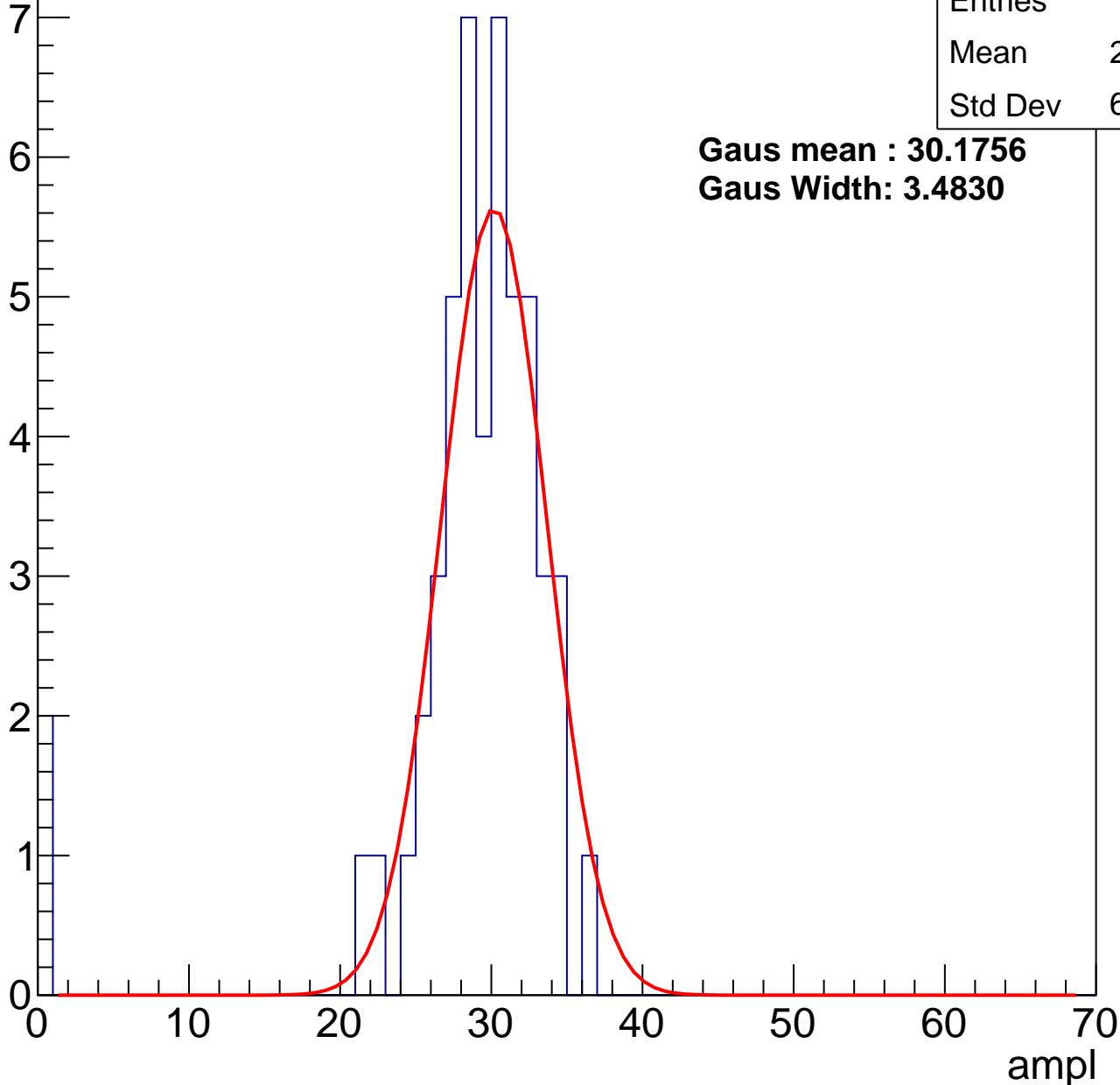
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	28.08
Std Dev	6.493

**Gaus mean : 30.1756**

**Gaus Width: 3.4830**



# B1L101S, U11-ch22, adc1

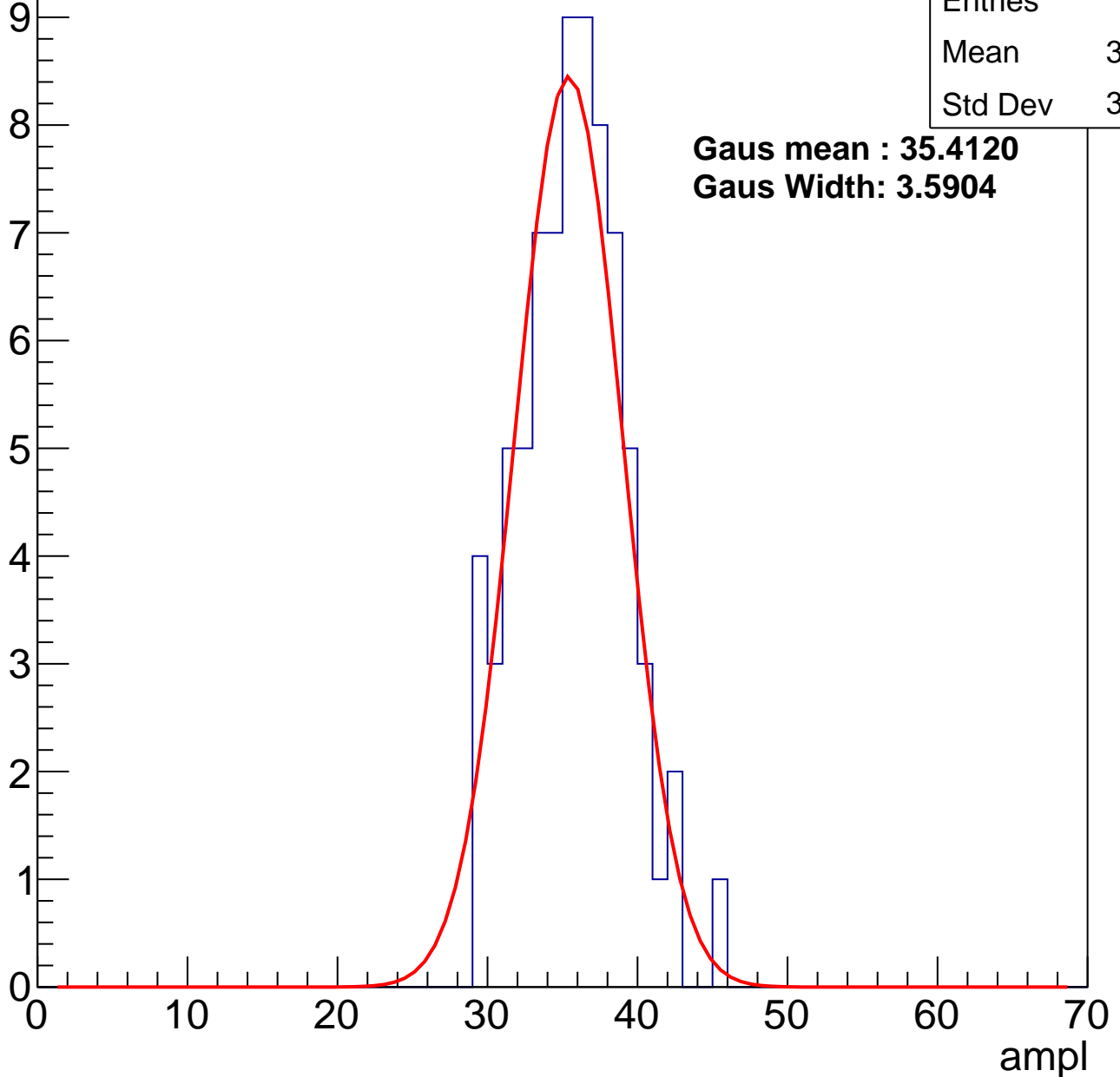
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	35.21
Std Dev	3.381

**Gaus mean : 35.4120**

**Gaus Width: 3.5904**



# B1L101S, U11-ch22, adc2

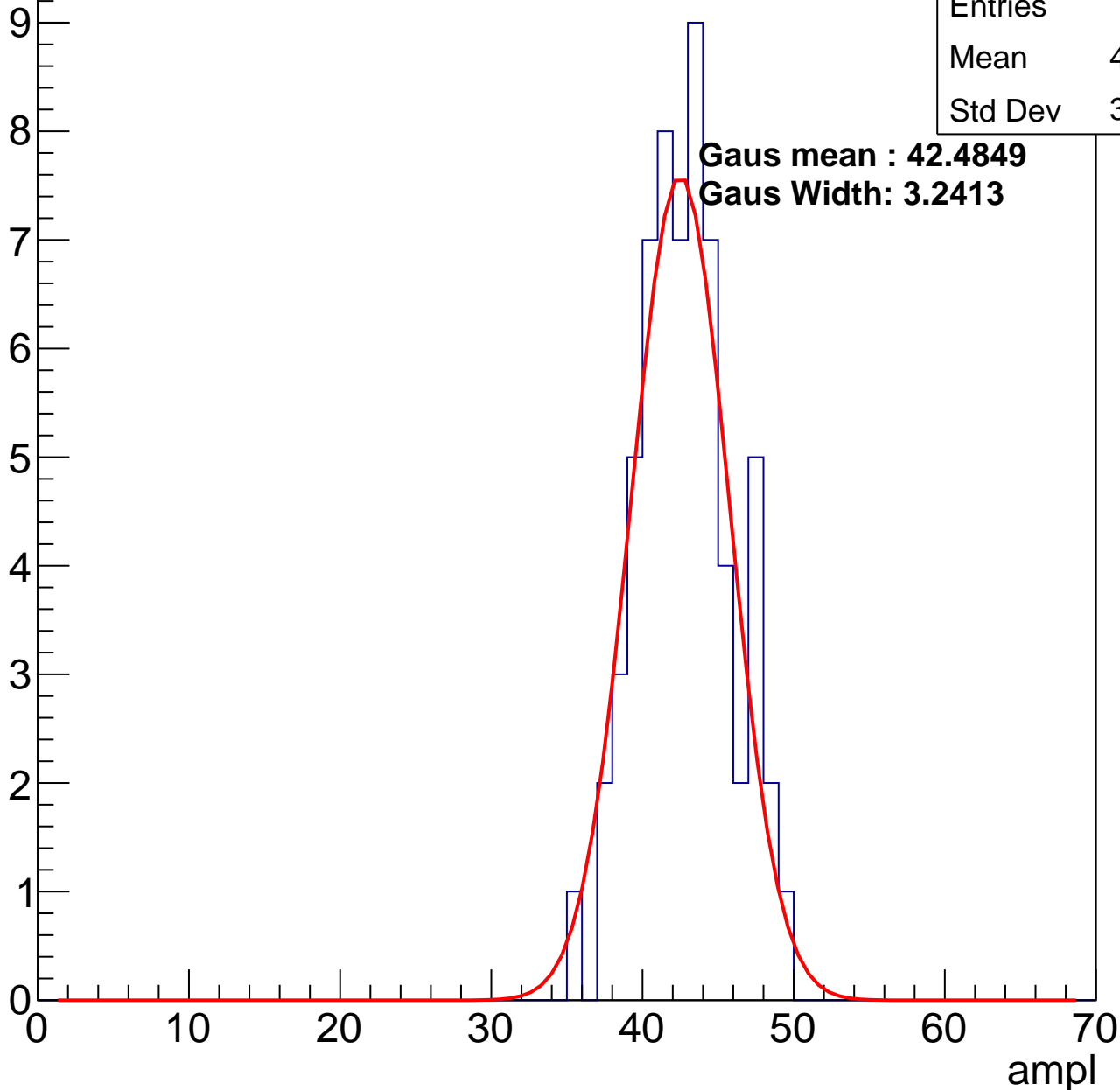
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	42.33
Std Dev	3.013

**Gaus mean : 42.4849**

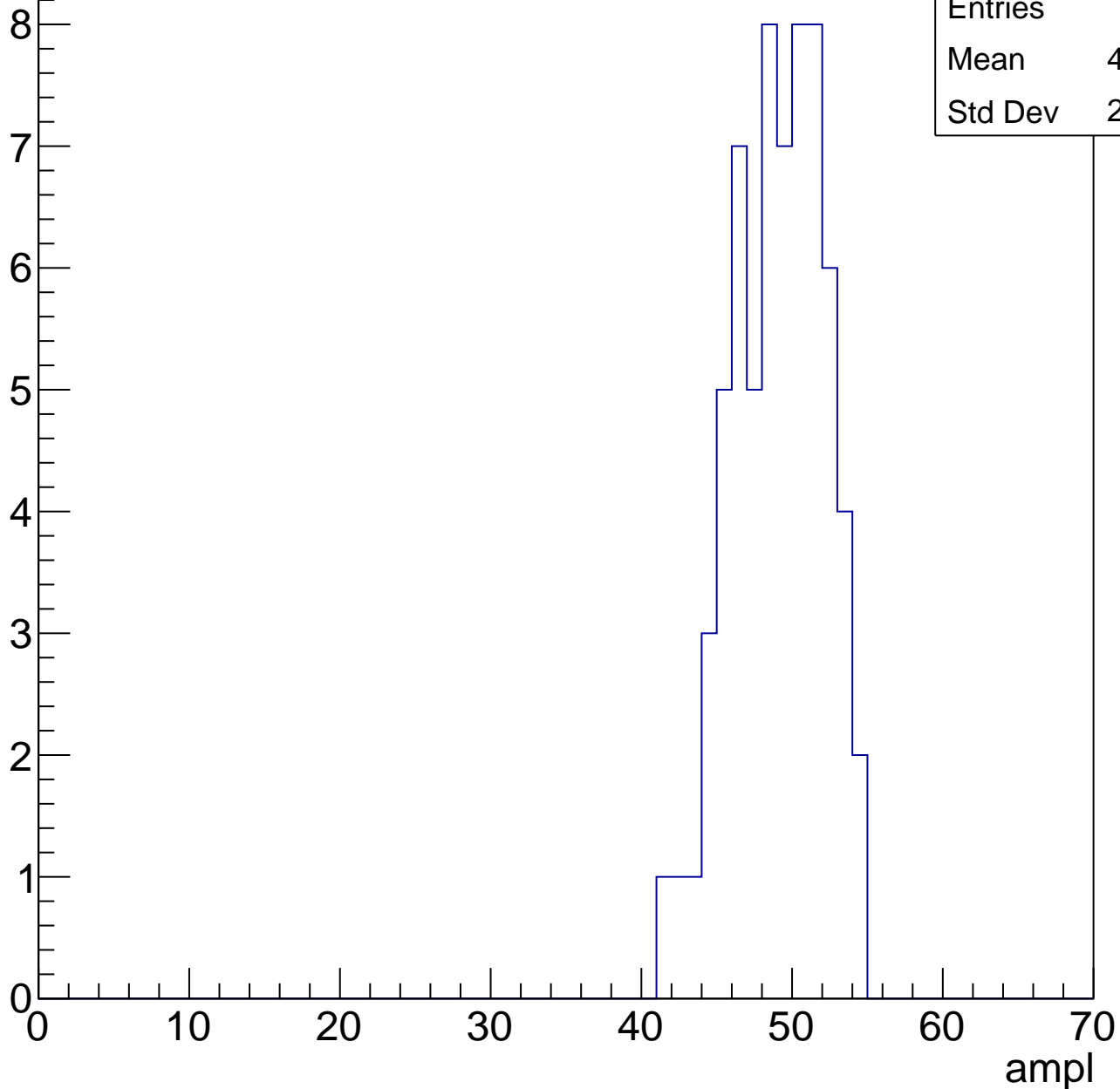
**Gaus Width: 3.2413**



# B1L101S, U11-ch22, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



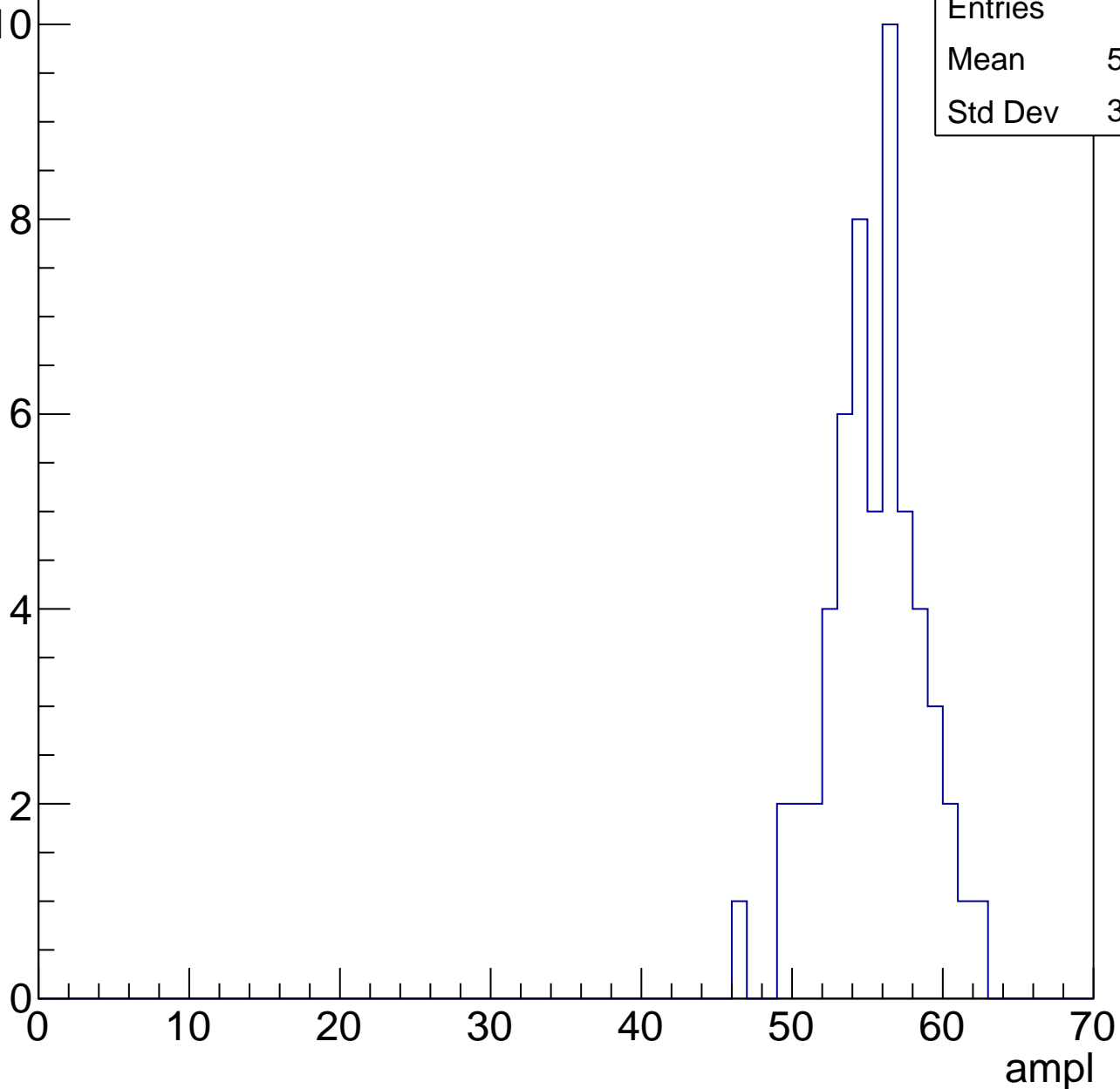
Entries	66
Mean	48.59
Std Dev	2.995

# B1L101S, U11-ch22, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	54.93
Std Dev	3.139

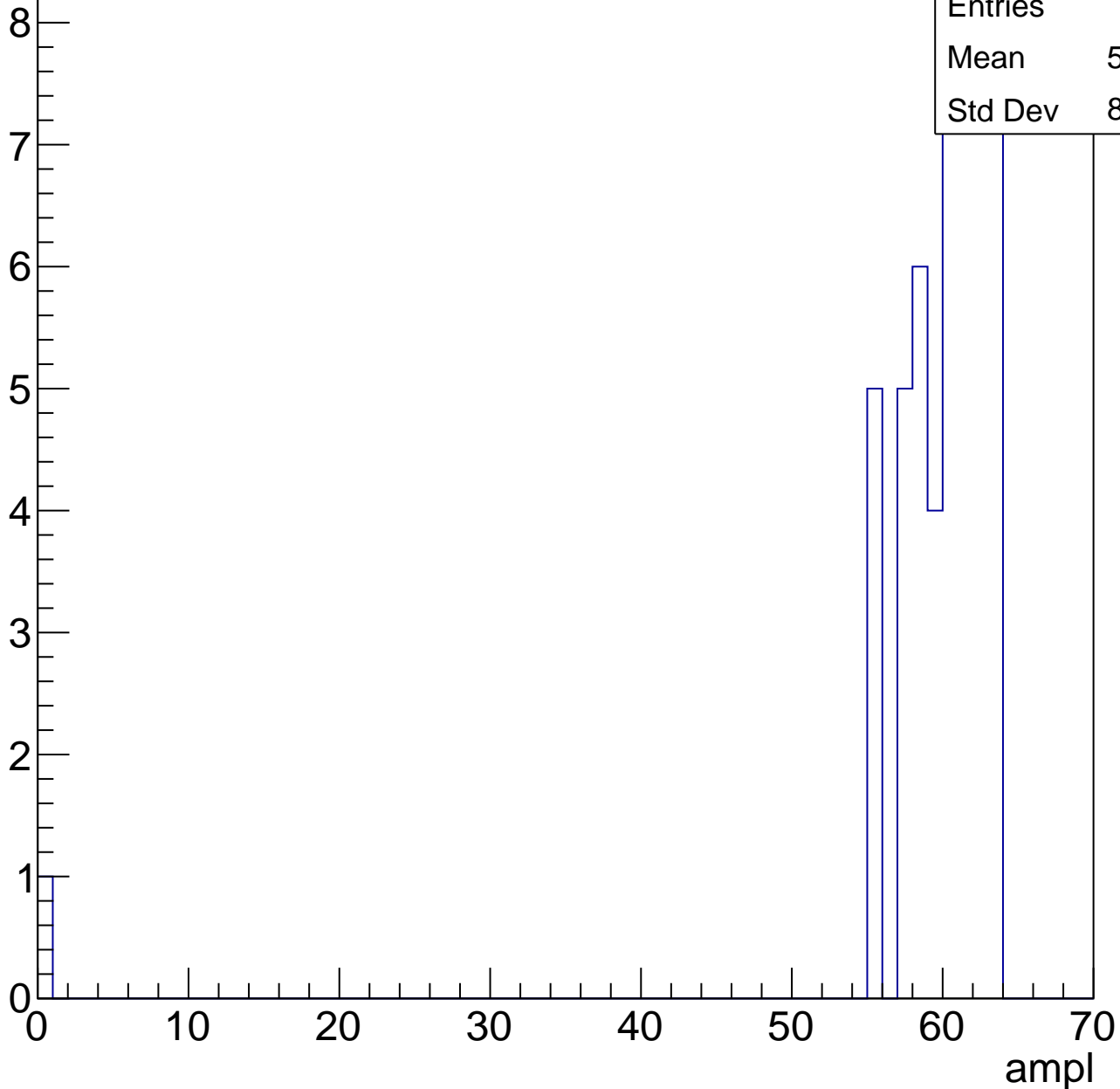


# B1L101S, U11-ch22, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	58.72
Std Dev	8.493



# B1L101S, U11-ch22, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries

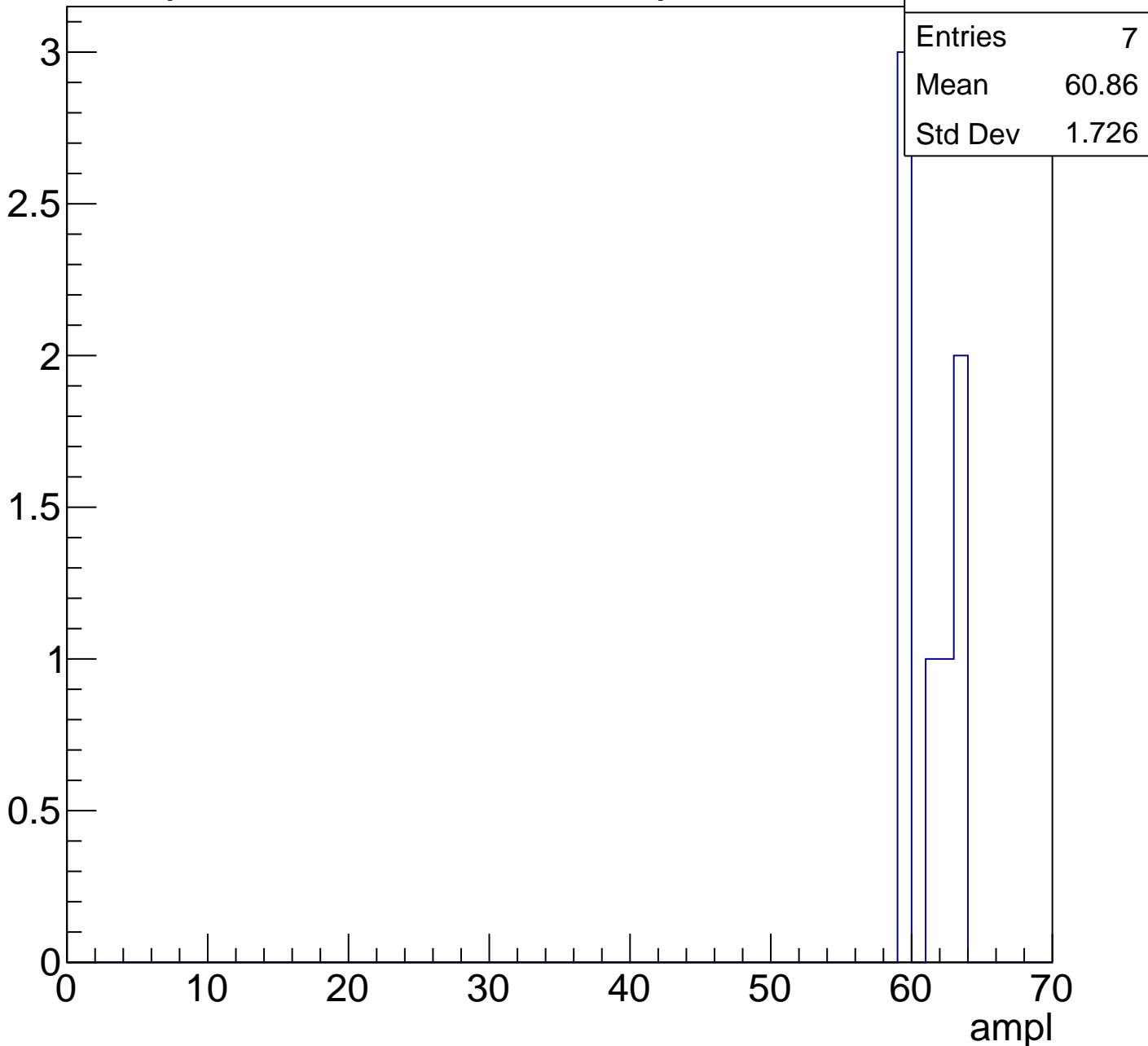
7

Mean

60.86

Std Dev

1.726





# B1L101S, U11-ch22, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U11-ch23, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	89
Mean	31.88
Std Dev	3.483

**Gaus mean : 32.4468**

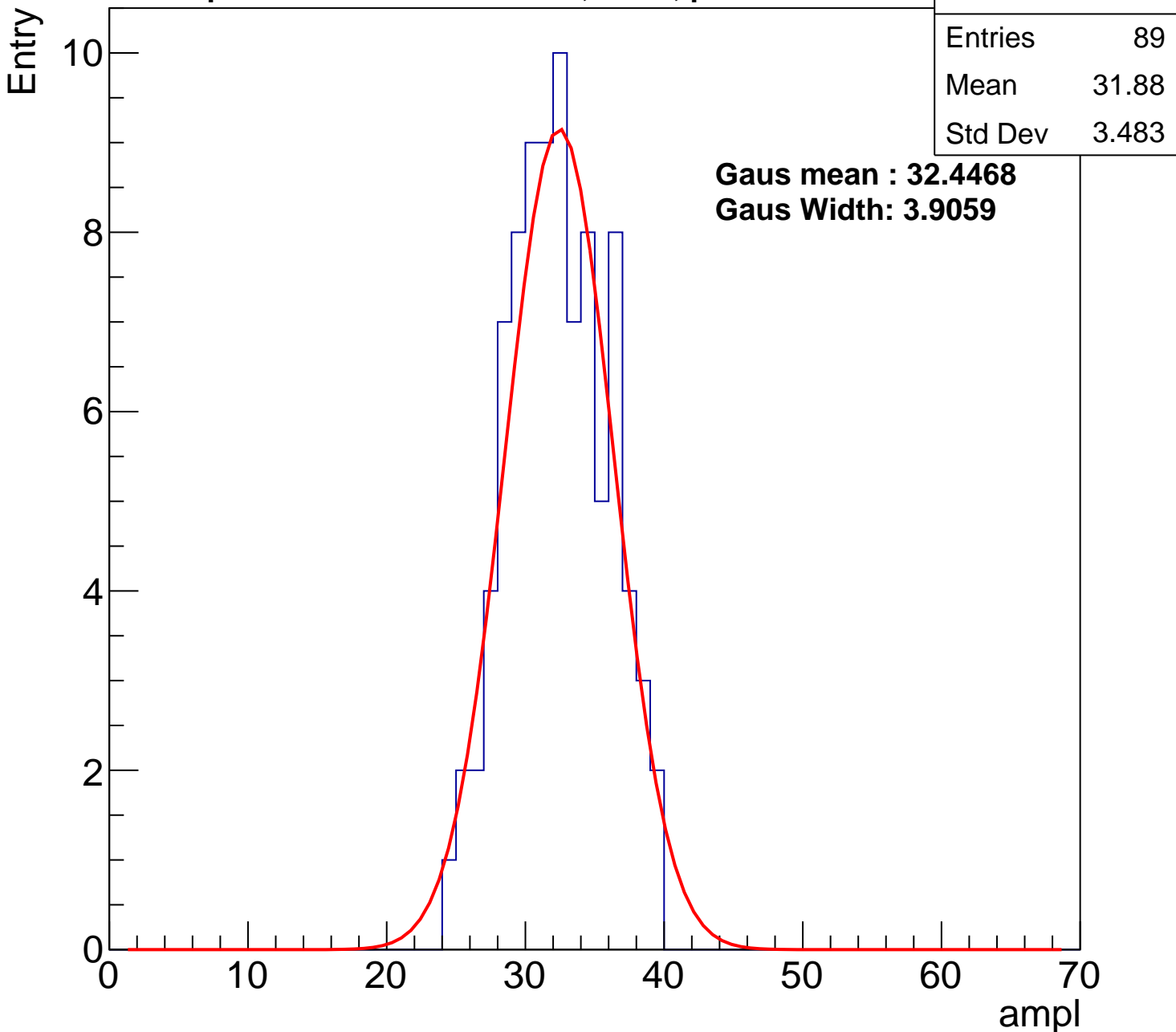
**Gaus Width: 3.9059**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U11-ch23, adc1

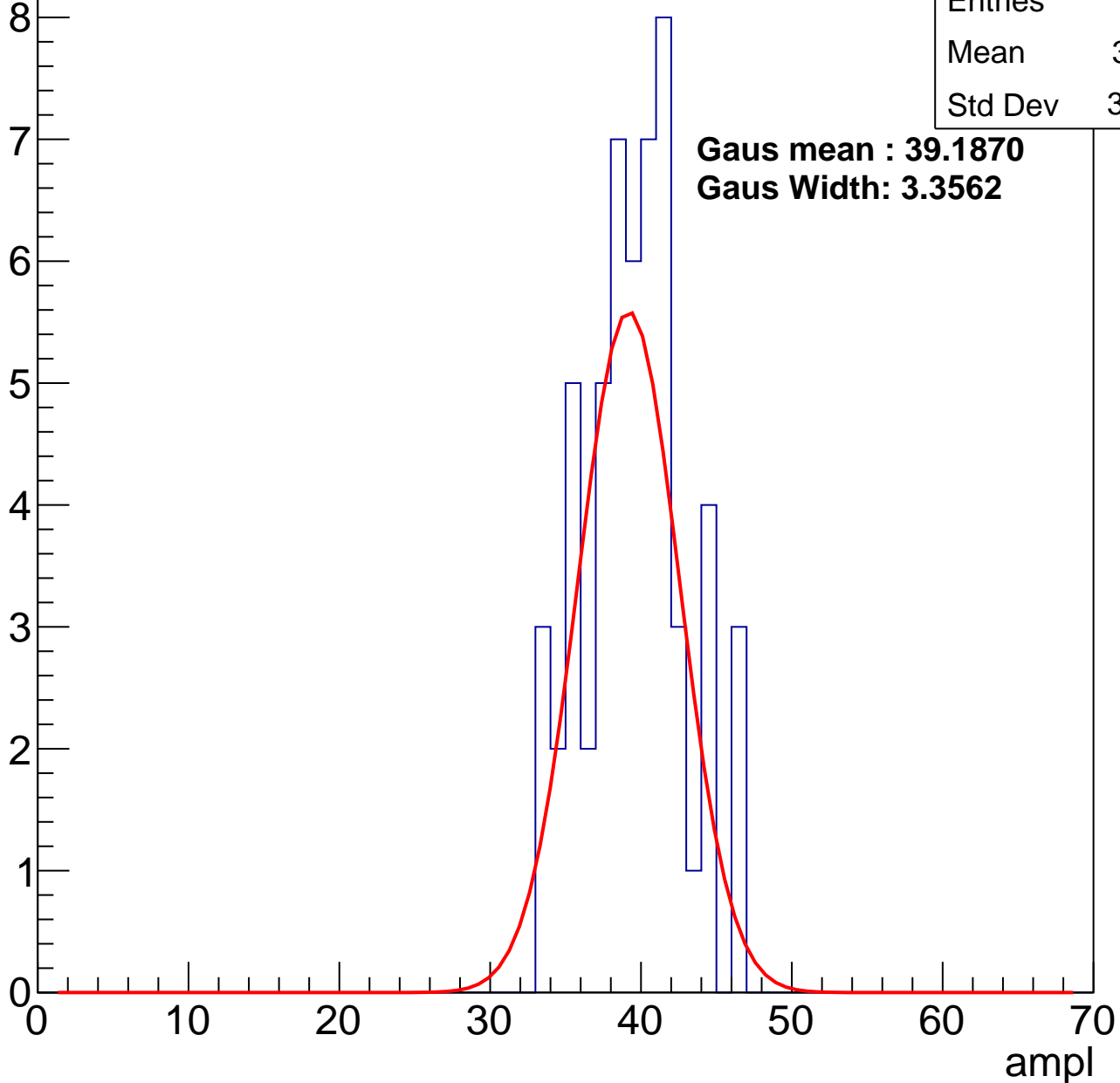
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	39.11
Std Dev	3.304

**Gaus mean : 39.1870**

**Gaus Width: 3.3562**



# B1L101S, U11-ch23, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	77
Mean	45.6
Std Dev	3.424

**Gaus mean : 46.1569**

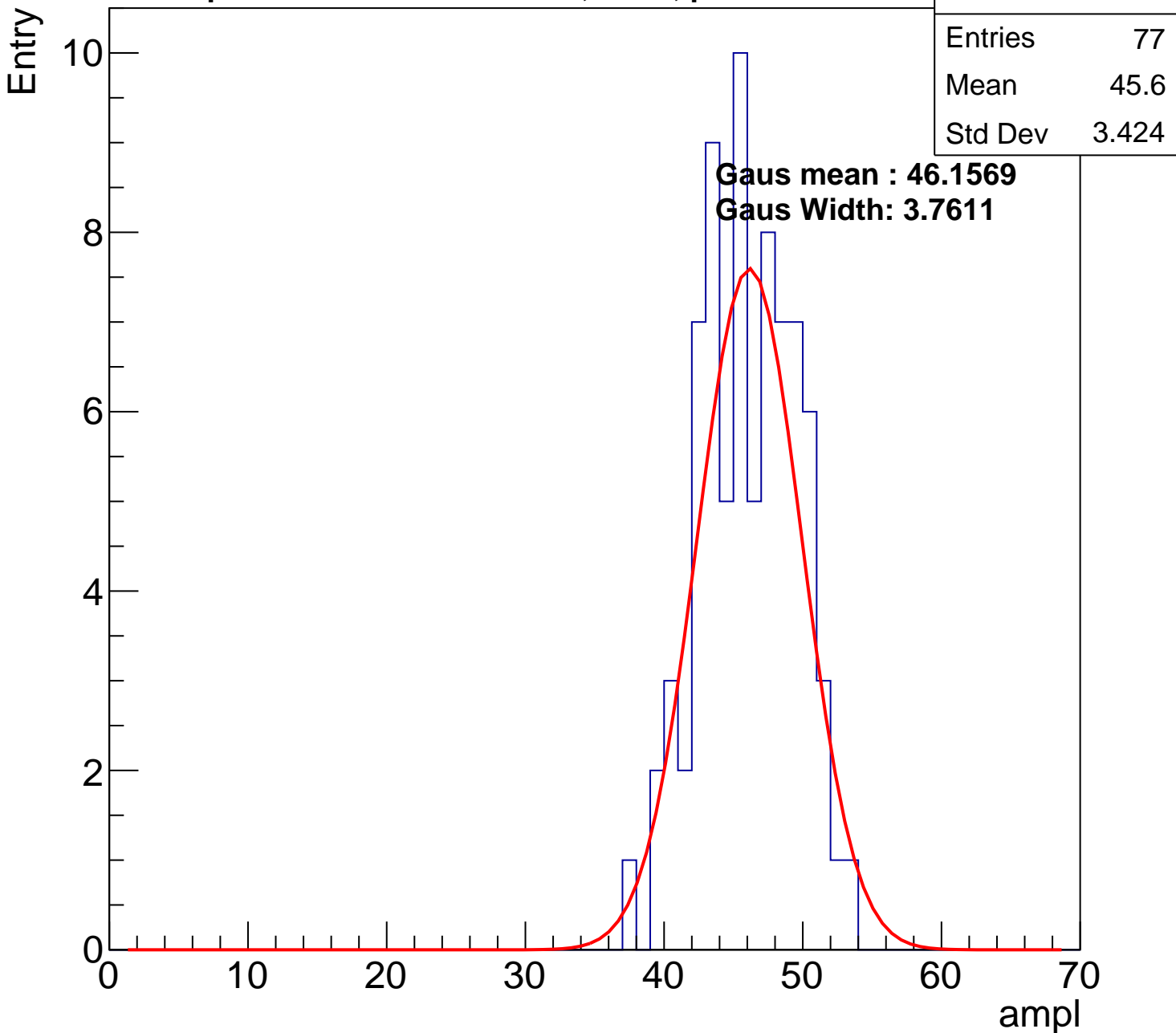
**Gaus Width: 3.7611**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

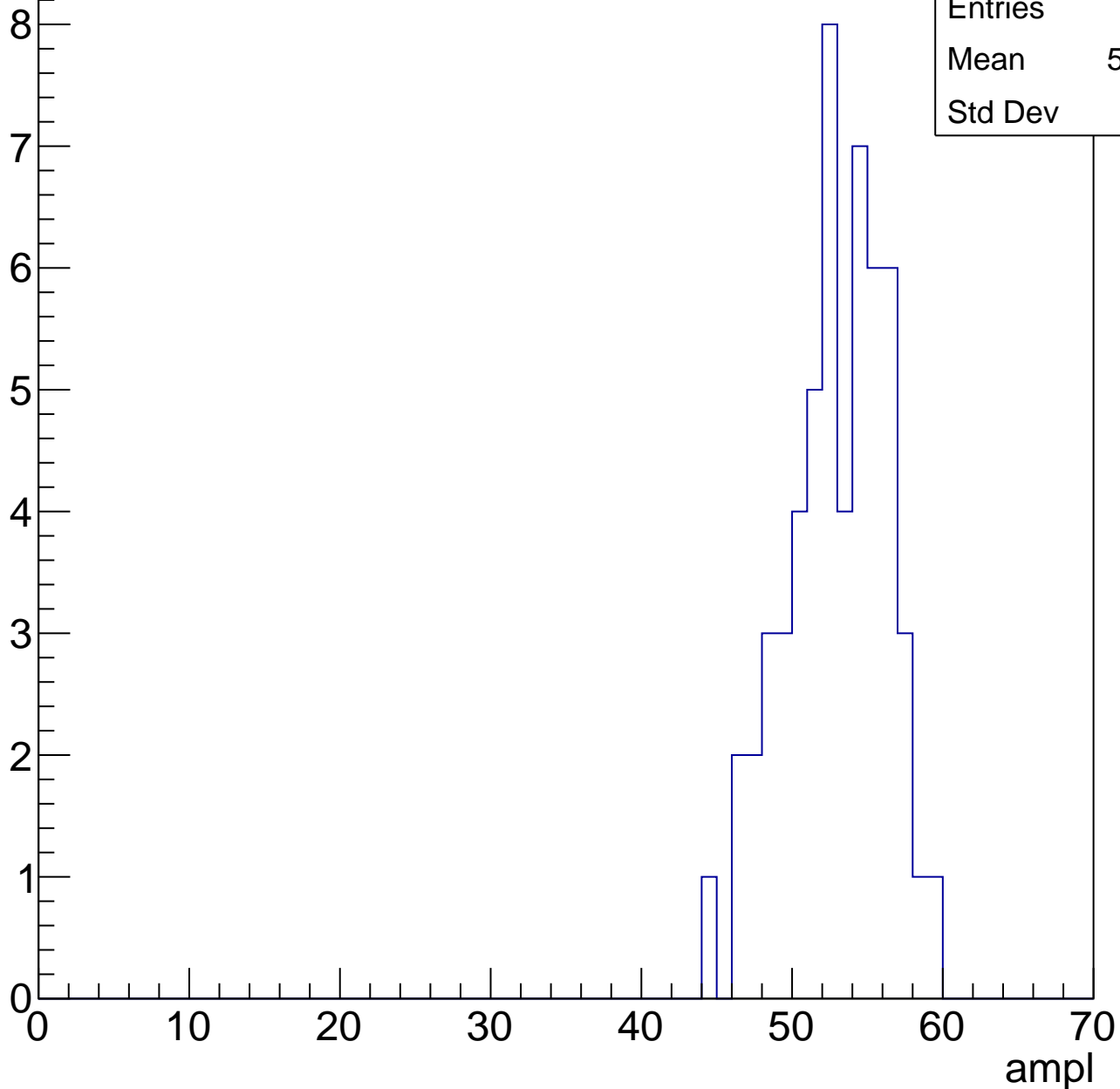


# B1L101S, U11-ch23, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

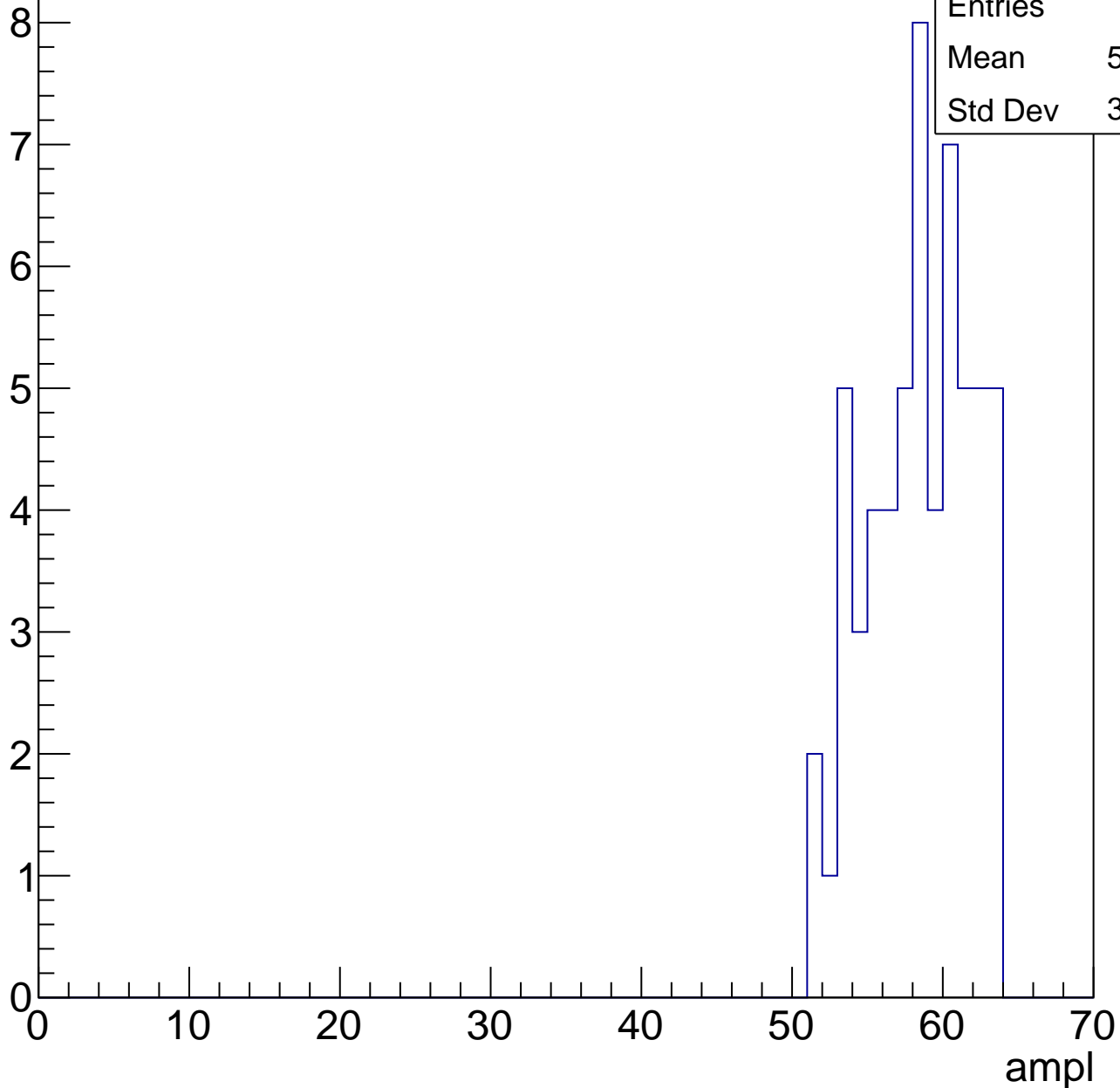
Entries	56
Mean	52.43
Std Dev	3.31



# B1L101S, U11-ch23, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

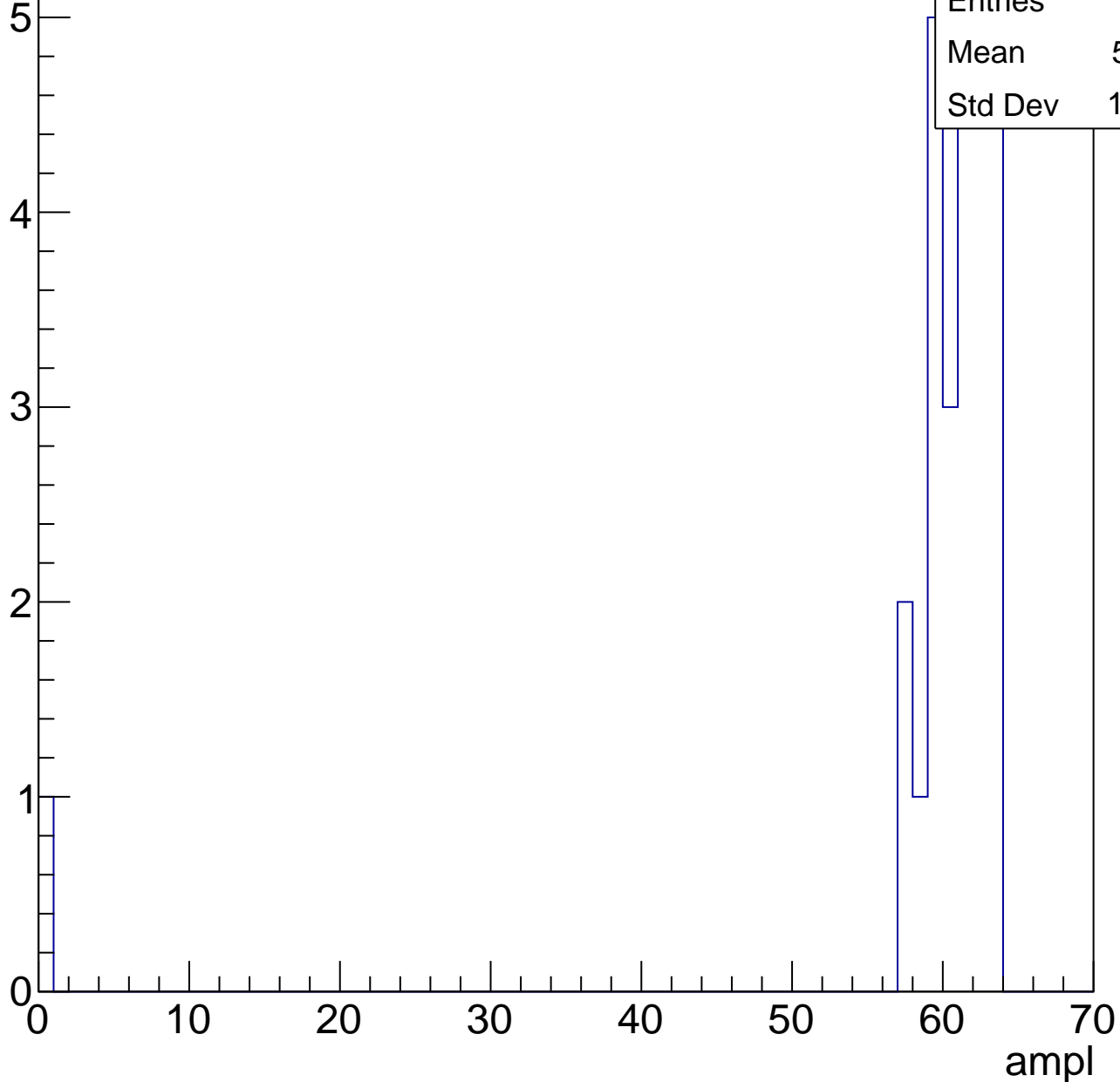
Entry



# B1L101S, U11-ch23, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U11-ch23, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L101S, U11-ch23, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	22
Std Dev	0

ampl

# B1L101S, U11-ch24, adc0

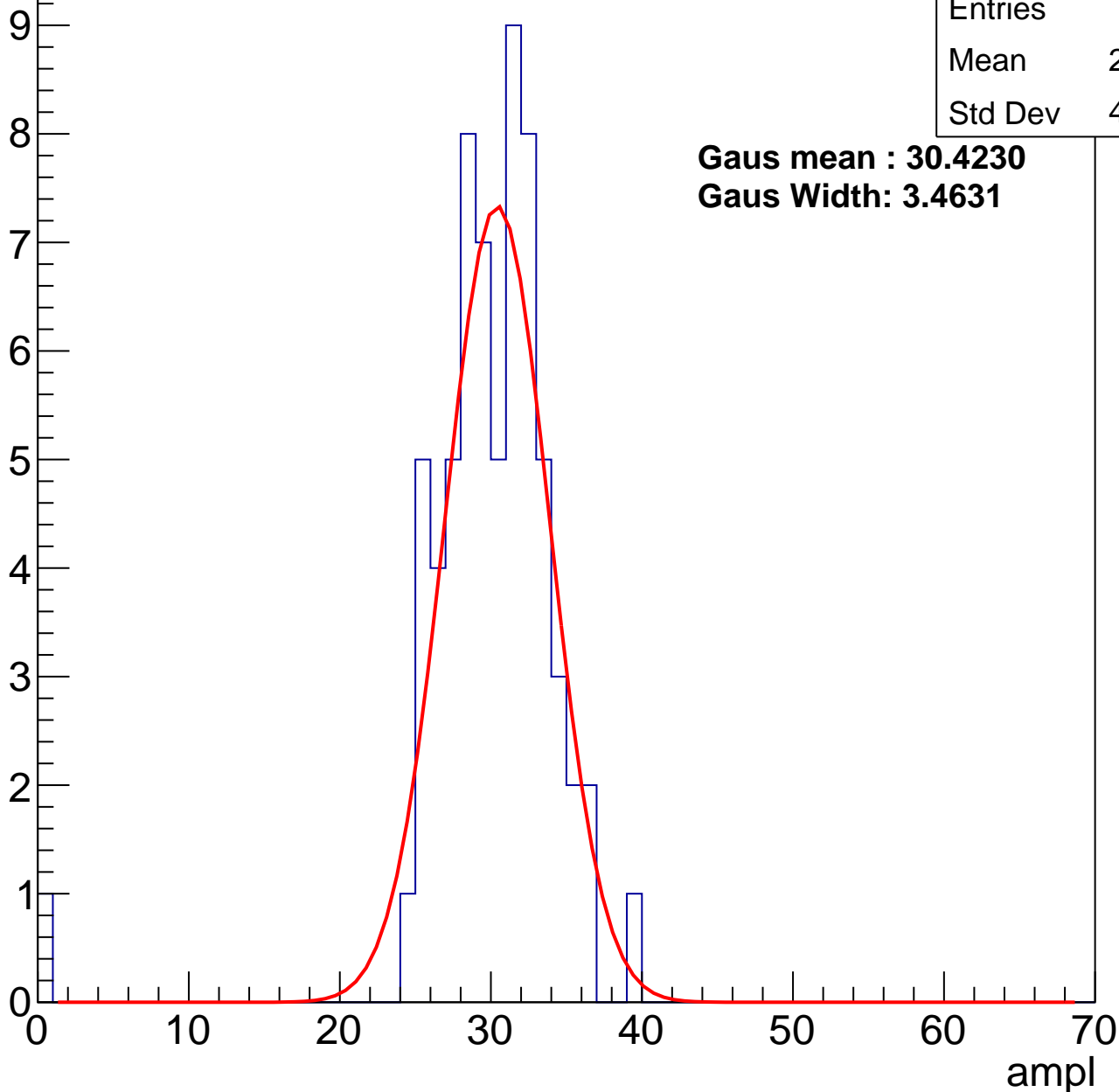
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	29.52
Std Dev	4.816

**Gaus mean : 30.4230**

**Gaus Width: 3.4631**



# B1L101S, U11-ch24, adc1

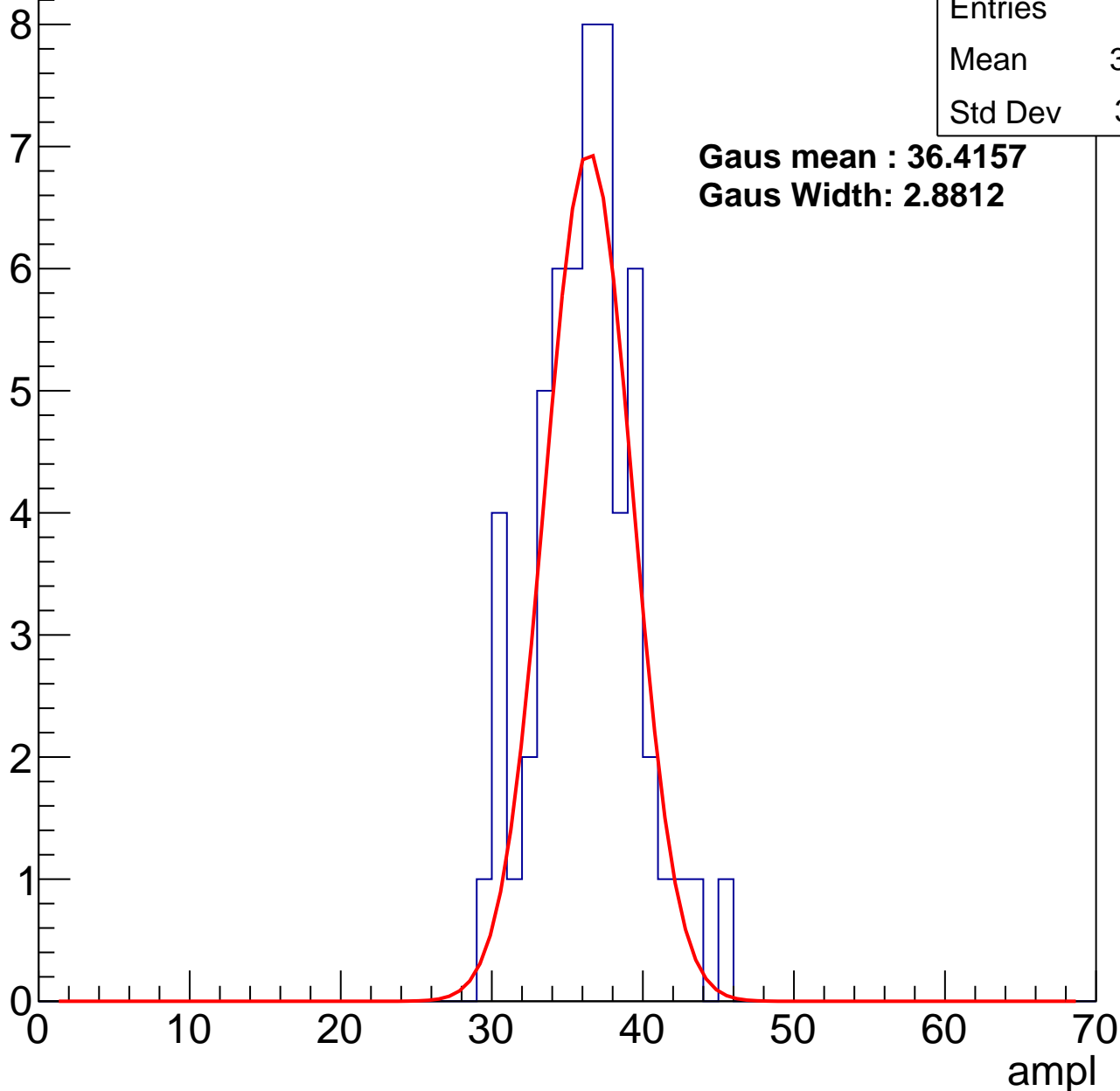
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	35.86
Std Dev	3.311

**Gaus mean : 36.4157**

**Gaus Width: 2.8812**



# B1L101S, U11-ch24, adc2

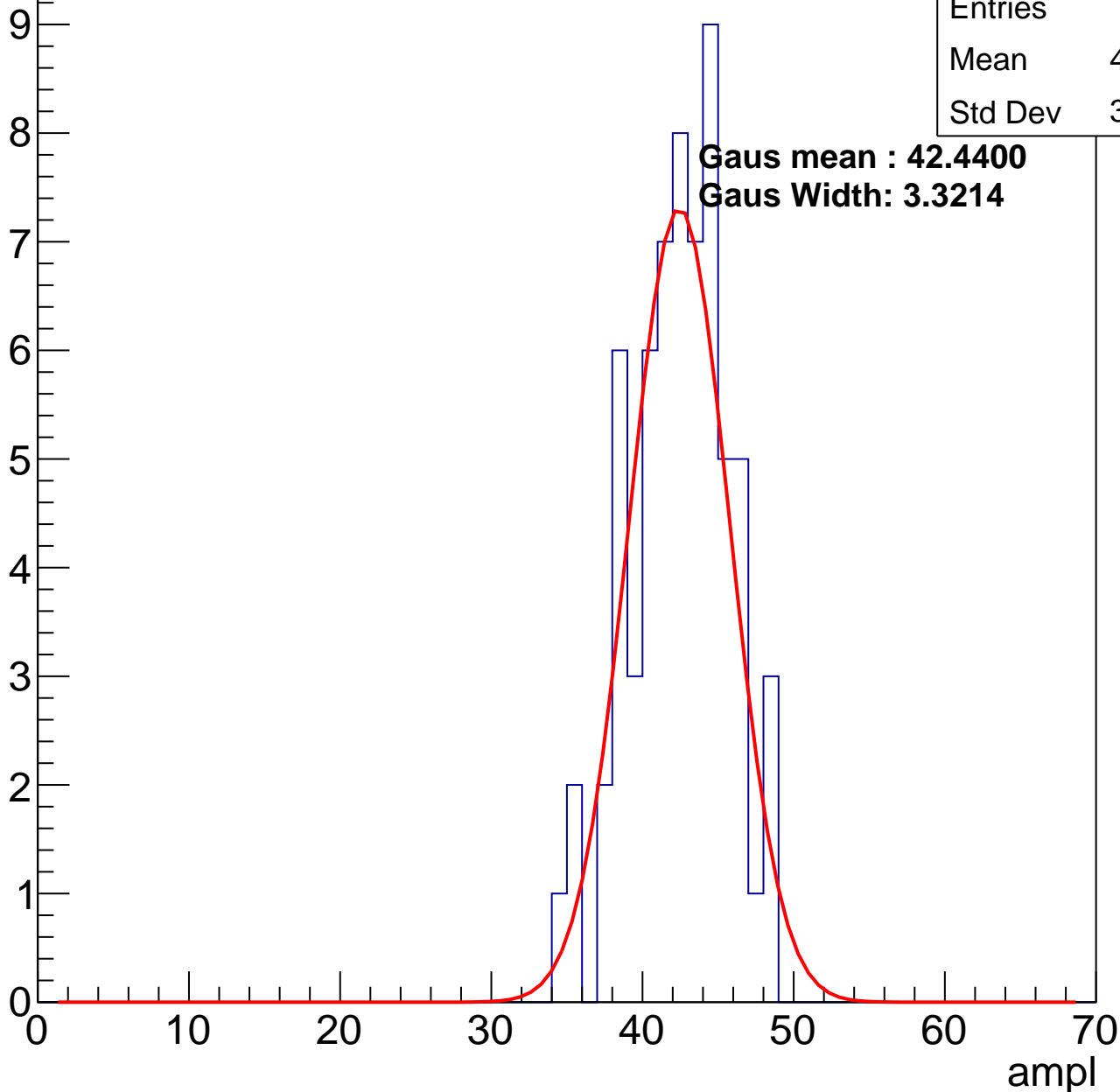
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	41.98
Std Dev	3.203

**Gaus mean : 42.4400**

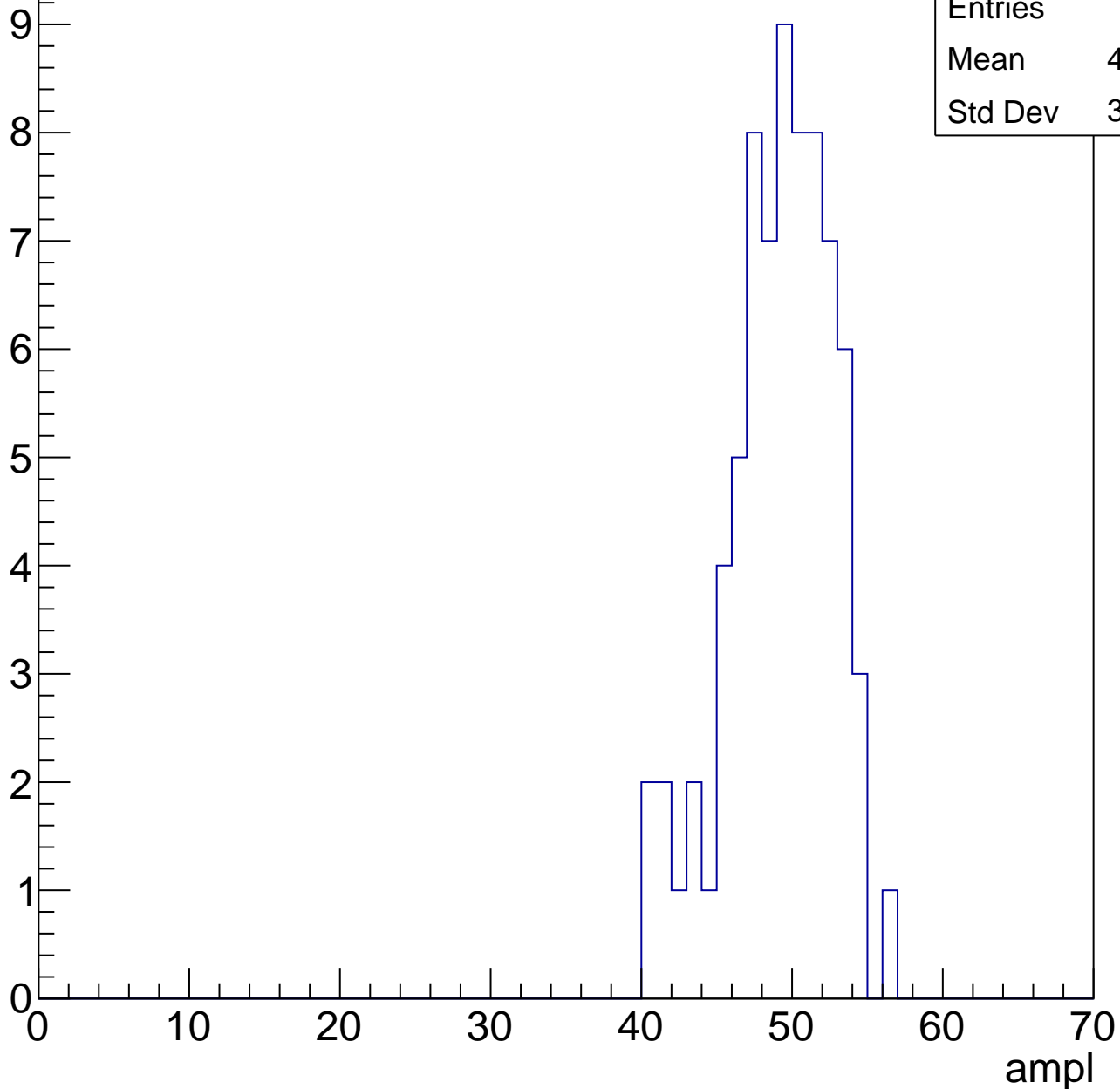
**Gaus Width: 3.3214**



# B1L101S, U11-ch24, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

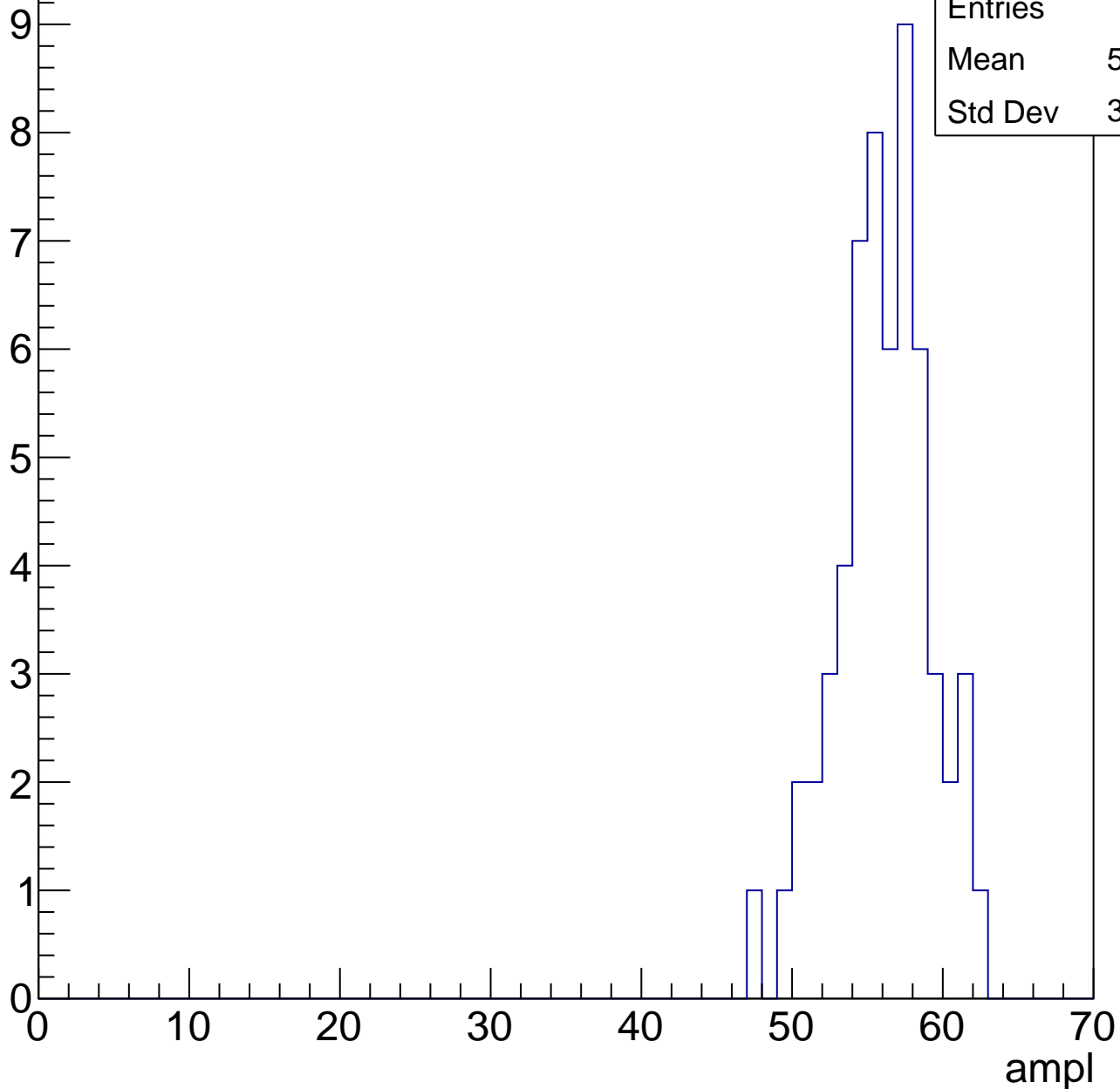
Entry



# B1L101S, U11-ch24, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

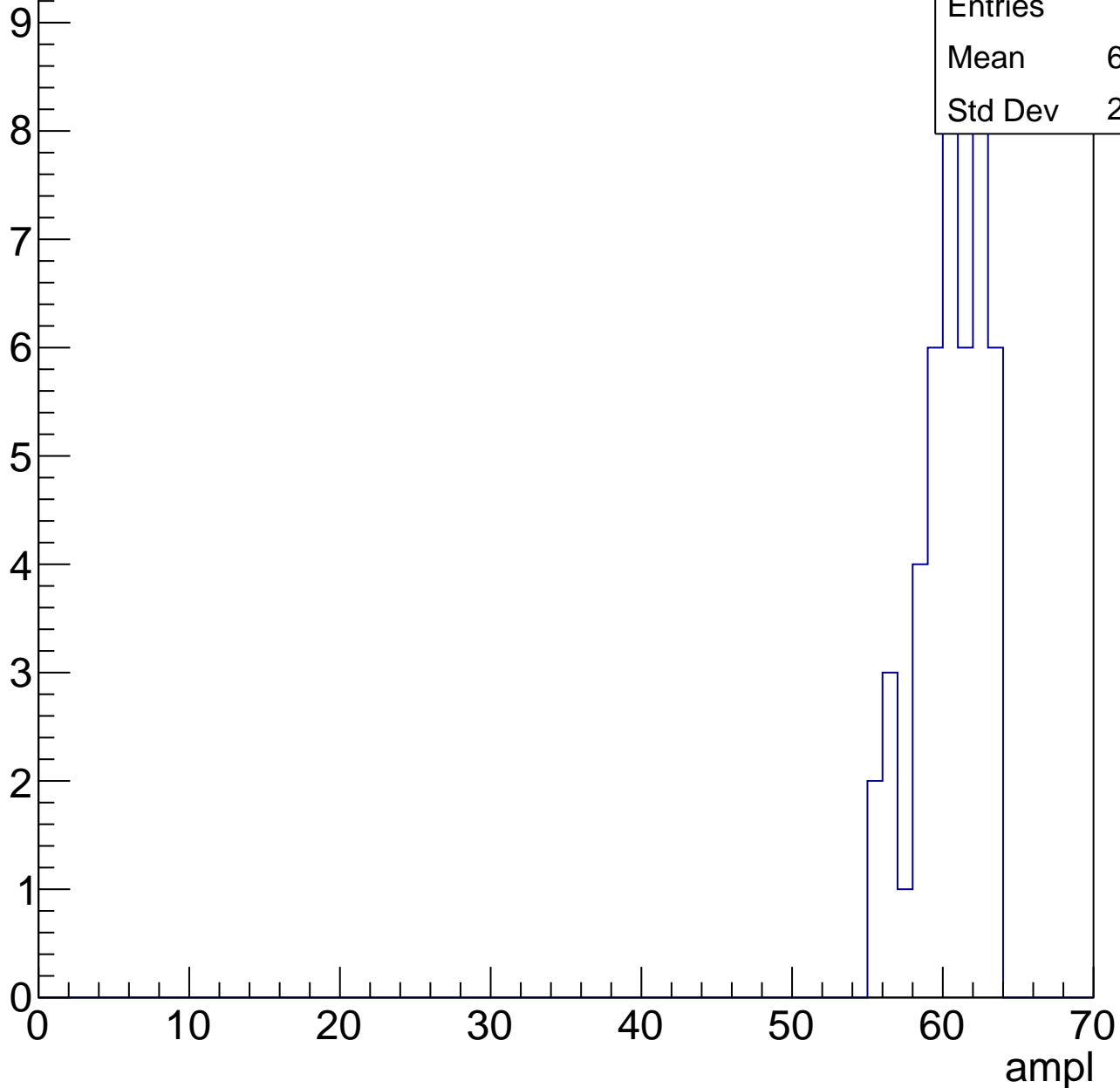


Entries	58
Mean	55.57
Std Dev	3.119

# B1L101S, U11-ch24, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

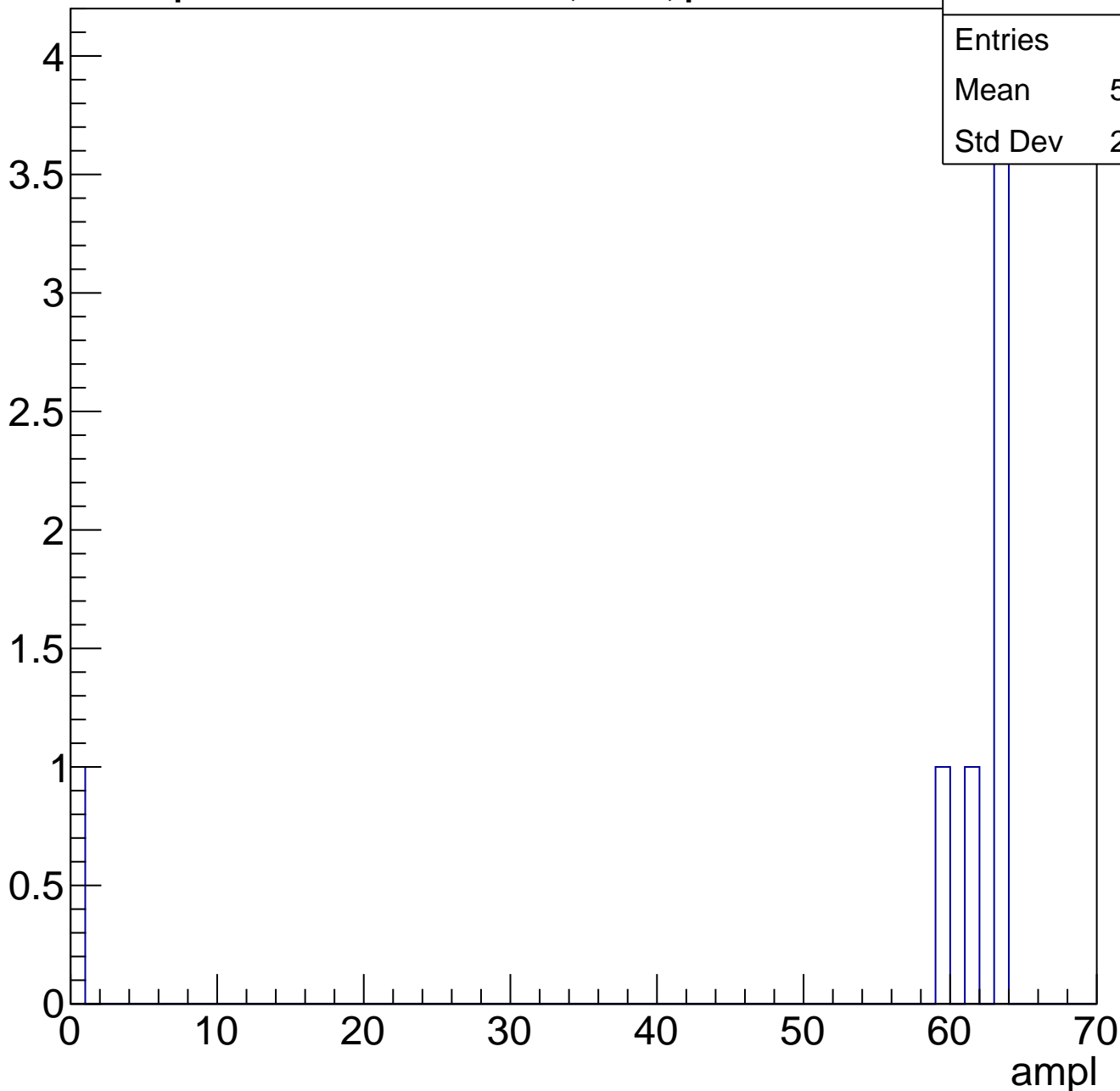
Entry



# B1L101S, U11-ch24, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch24, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U11-ch25, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	87
Mean	29.92
Std Dev	3.595

**Gaus mean : 30.6216**

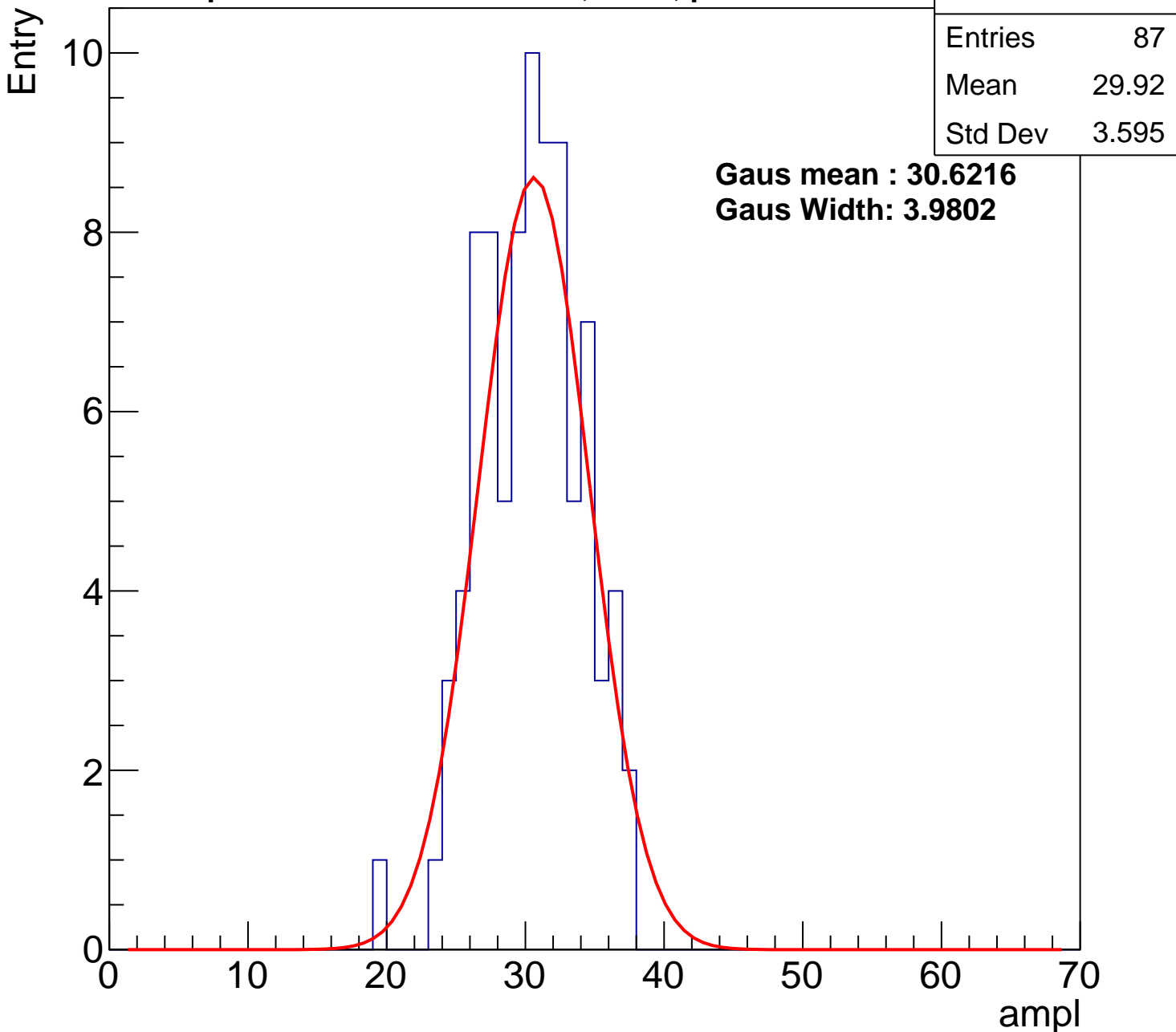
**Gaus Width: 3.9802**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



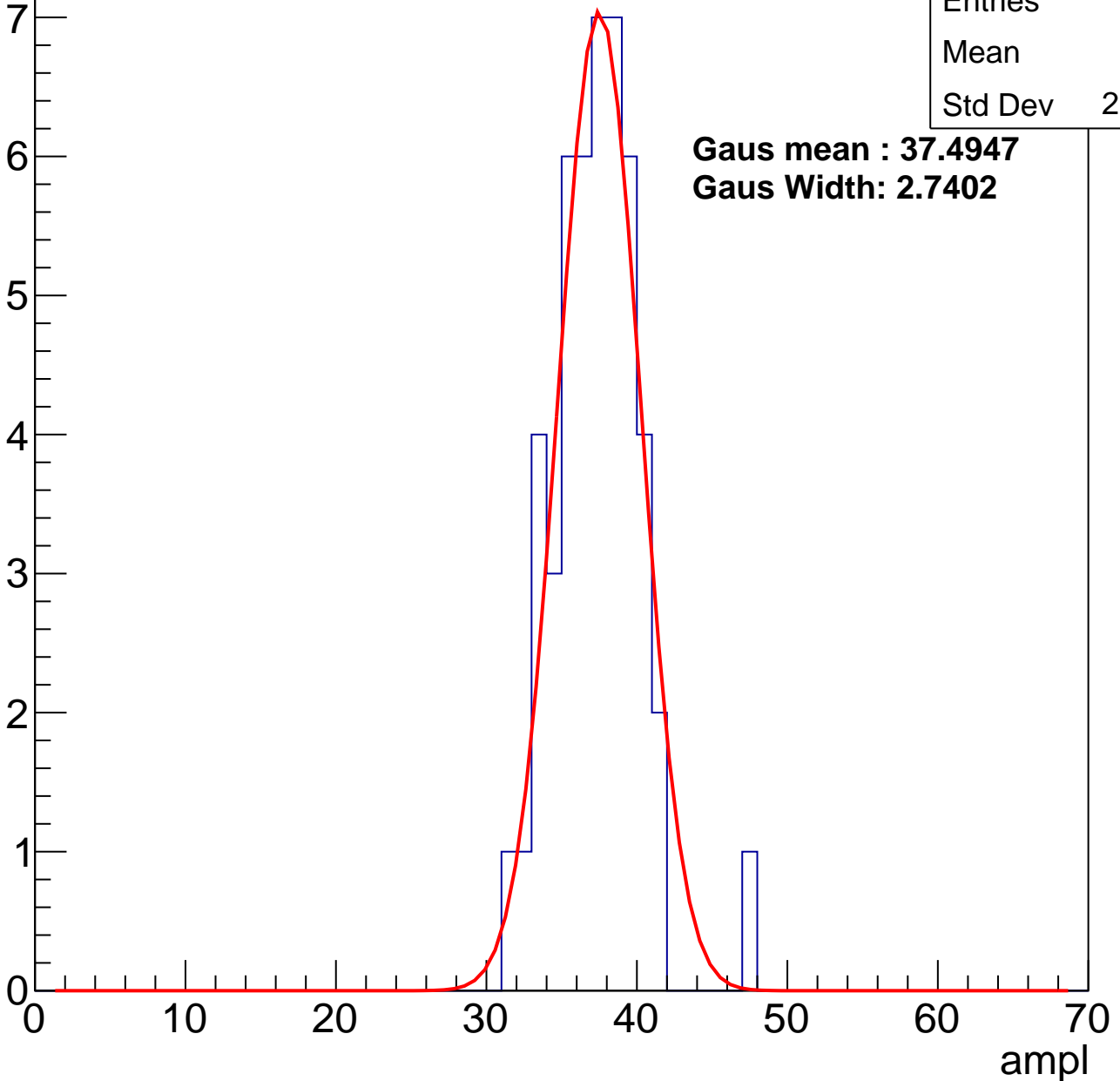
# B1L101S, U11-ch25, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	48
Mean	36.9
Std Dev	2.815

**Gaus mean : 37.4947**  
**Gaus Width: 2.7402**



# B1L101S, U11-ch25, adc2

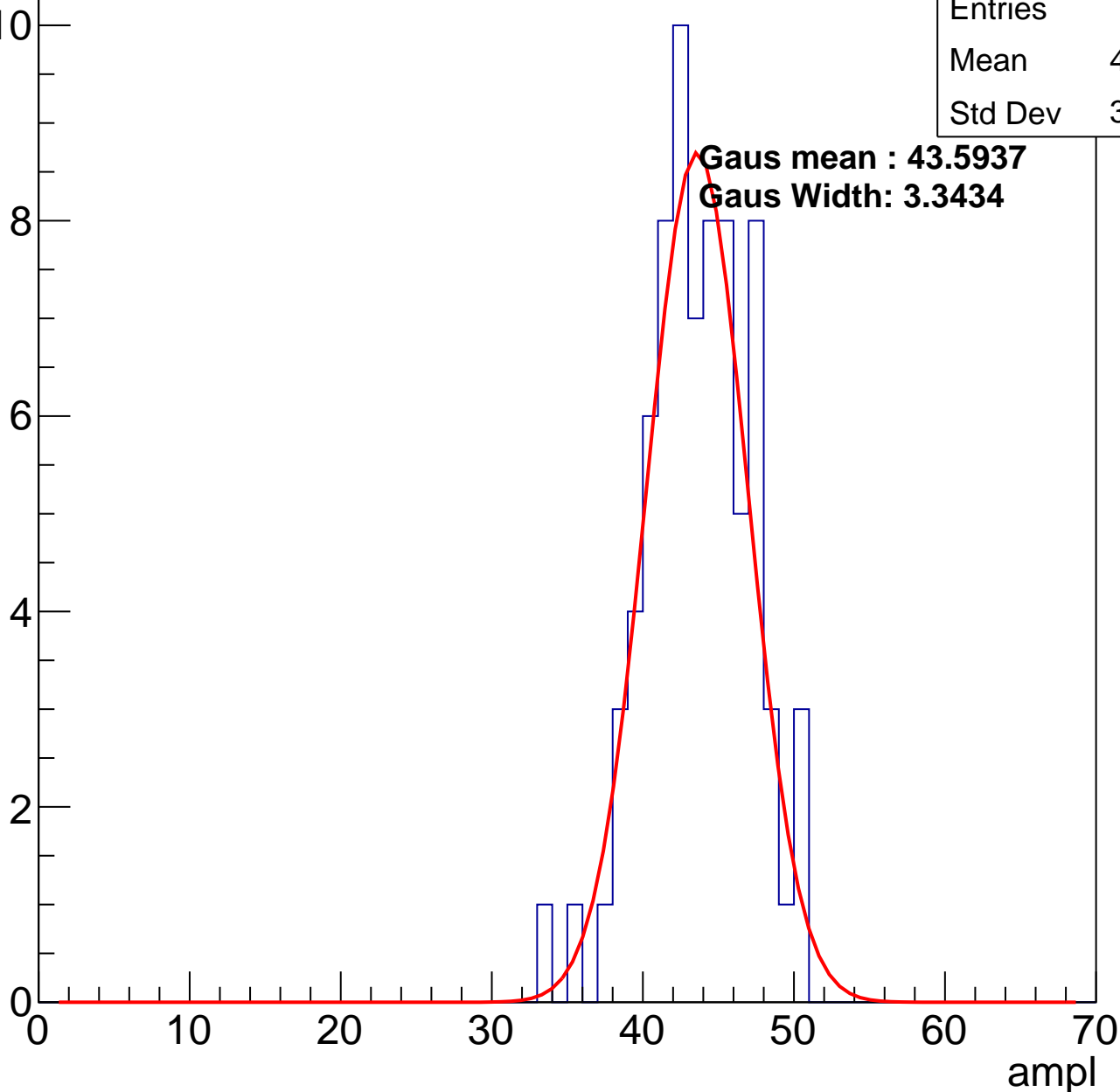
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	43.18
Std Dev	3.425

**Gaus mean : 43.5937**

**Gaus Width: 3.3434**



# B1L101S, U11-ch25, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	81
Mean	50.9
Std Dev	3.704

Entry

10

8

6

4

2

0

0

10

20

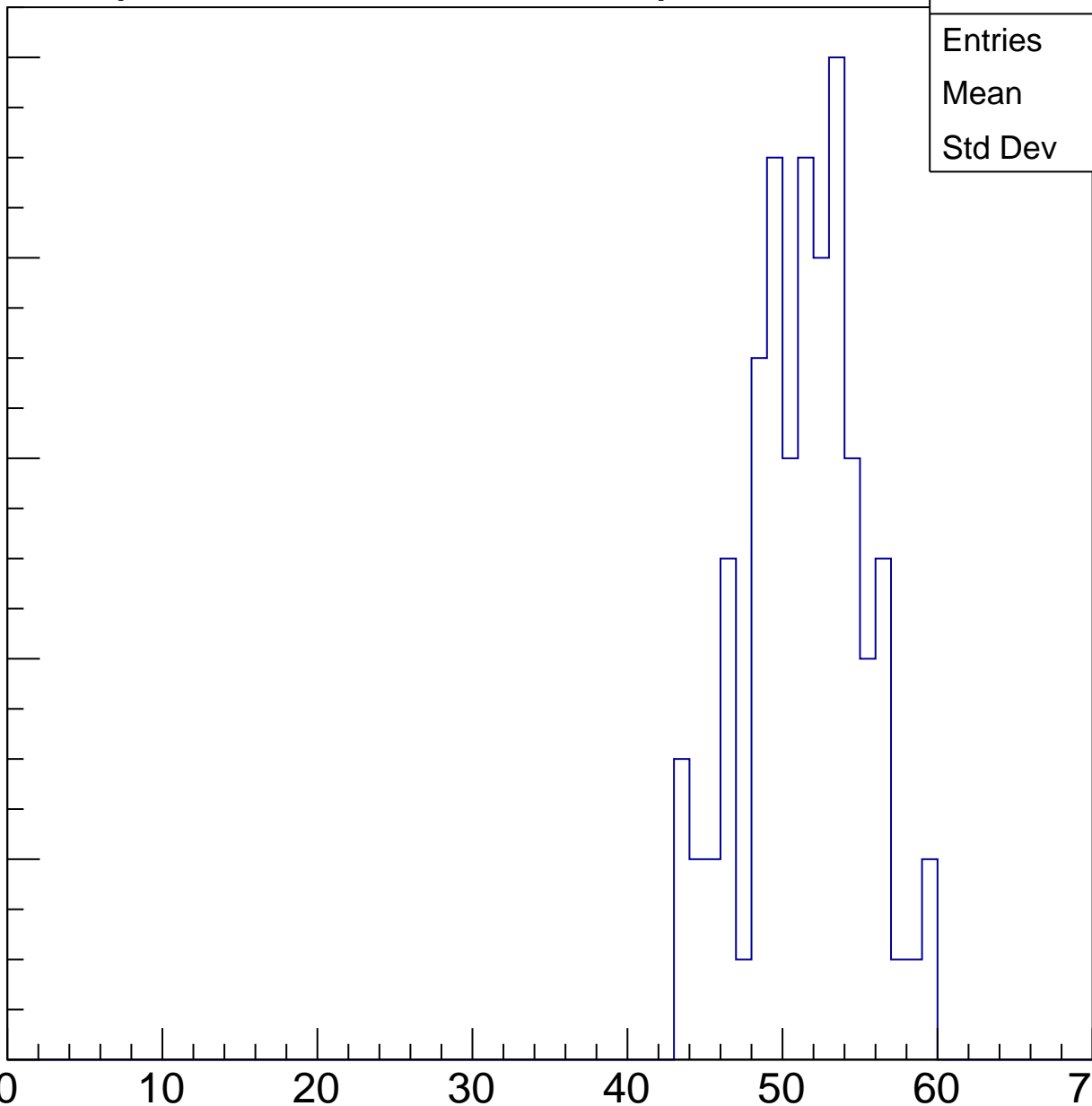
30

40

50

60

ampl

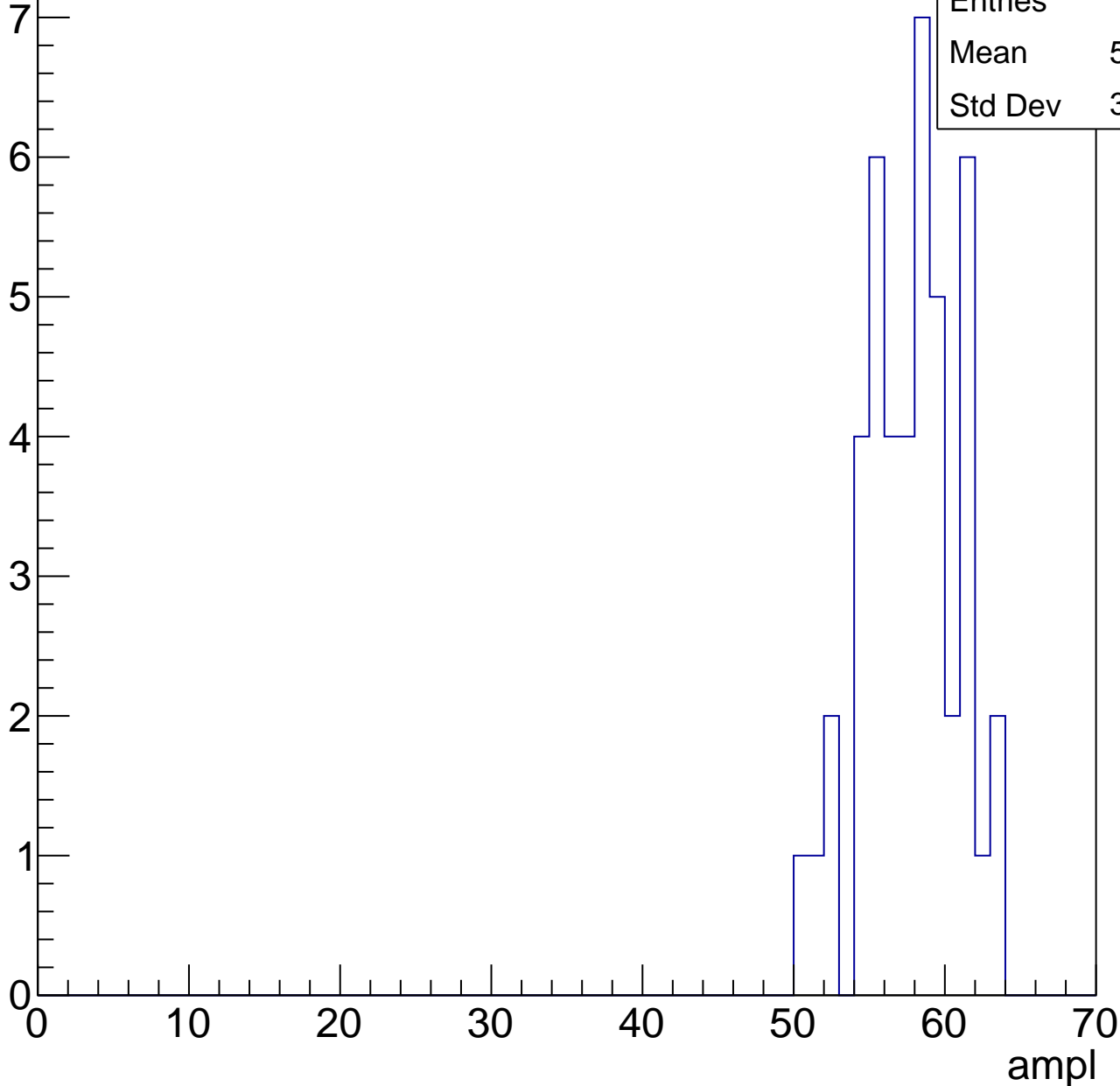


# B1L101S, U11-ch25, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

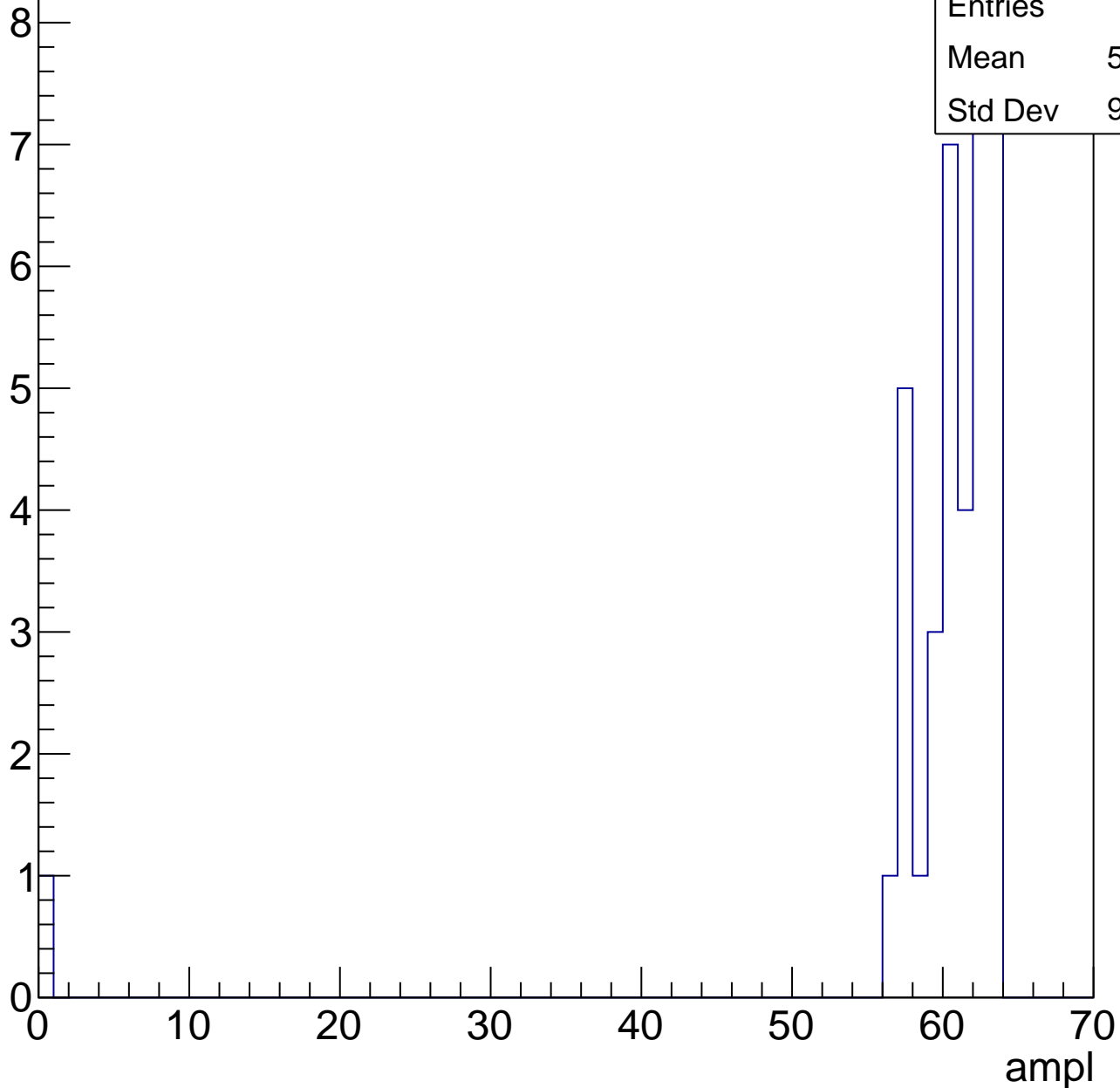
Entries	45
Mean	57.29
Std Dev	3.103



# B1L101S, U11-ch25, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

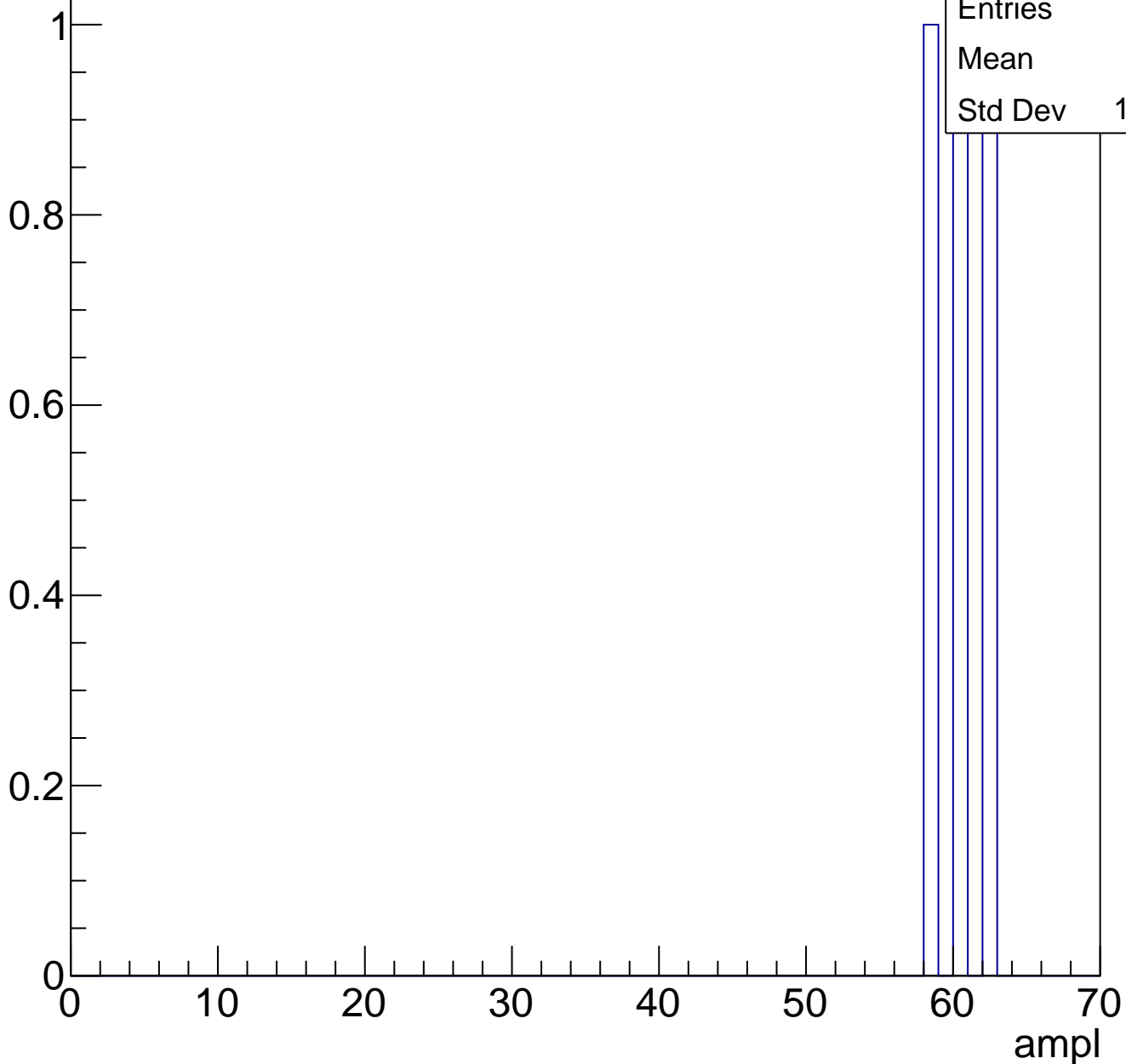
Entry



# B1L101S, U11-ch25, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch25, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U11-ch26, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	95
Mean	29.72
Std Dev	7.289

**Gaus mean : 31.8081**

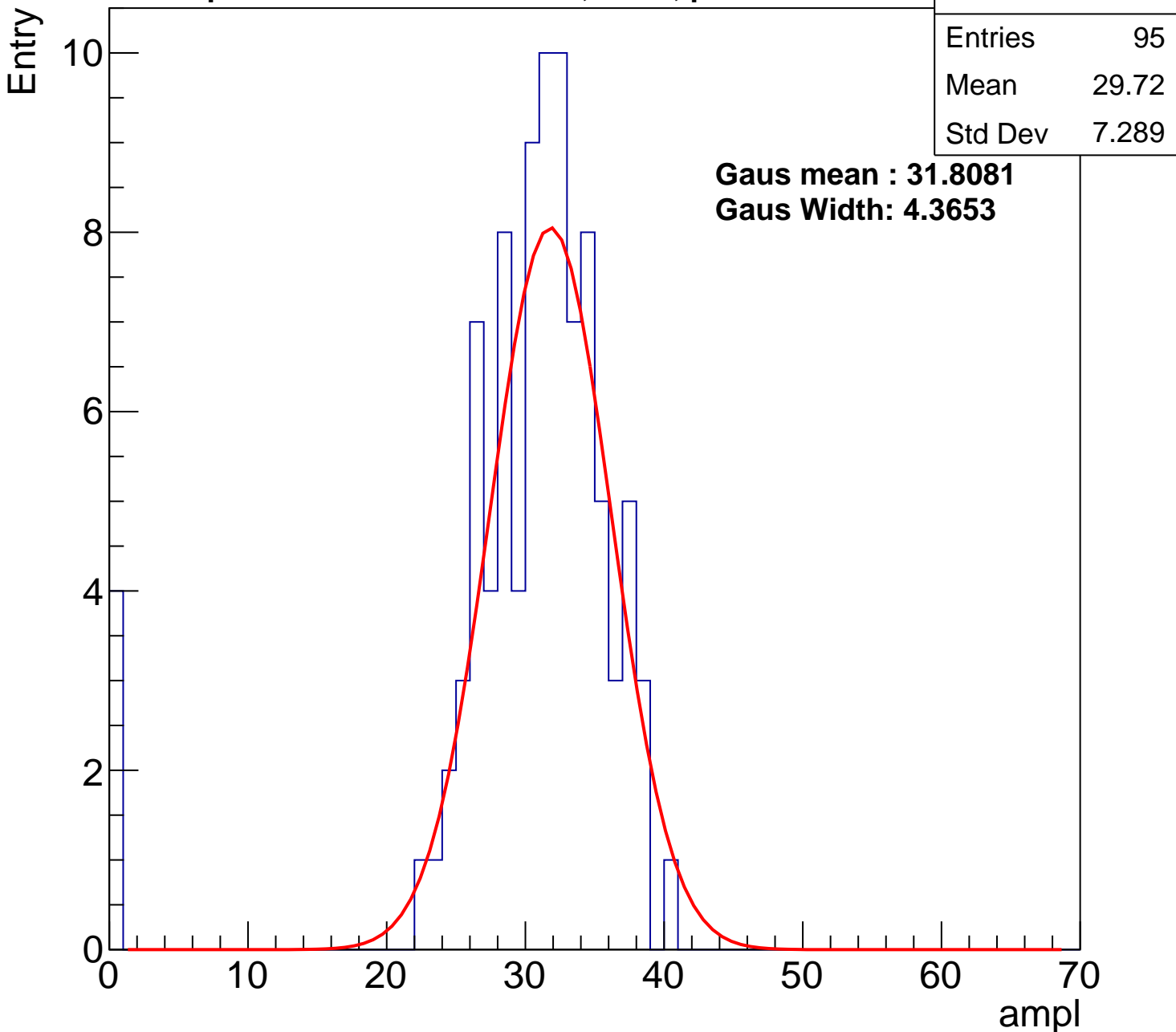
**Gaus Width: 4.3653**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L101S, U11-ch26, adc1

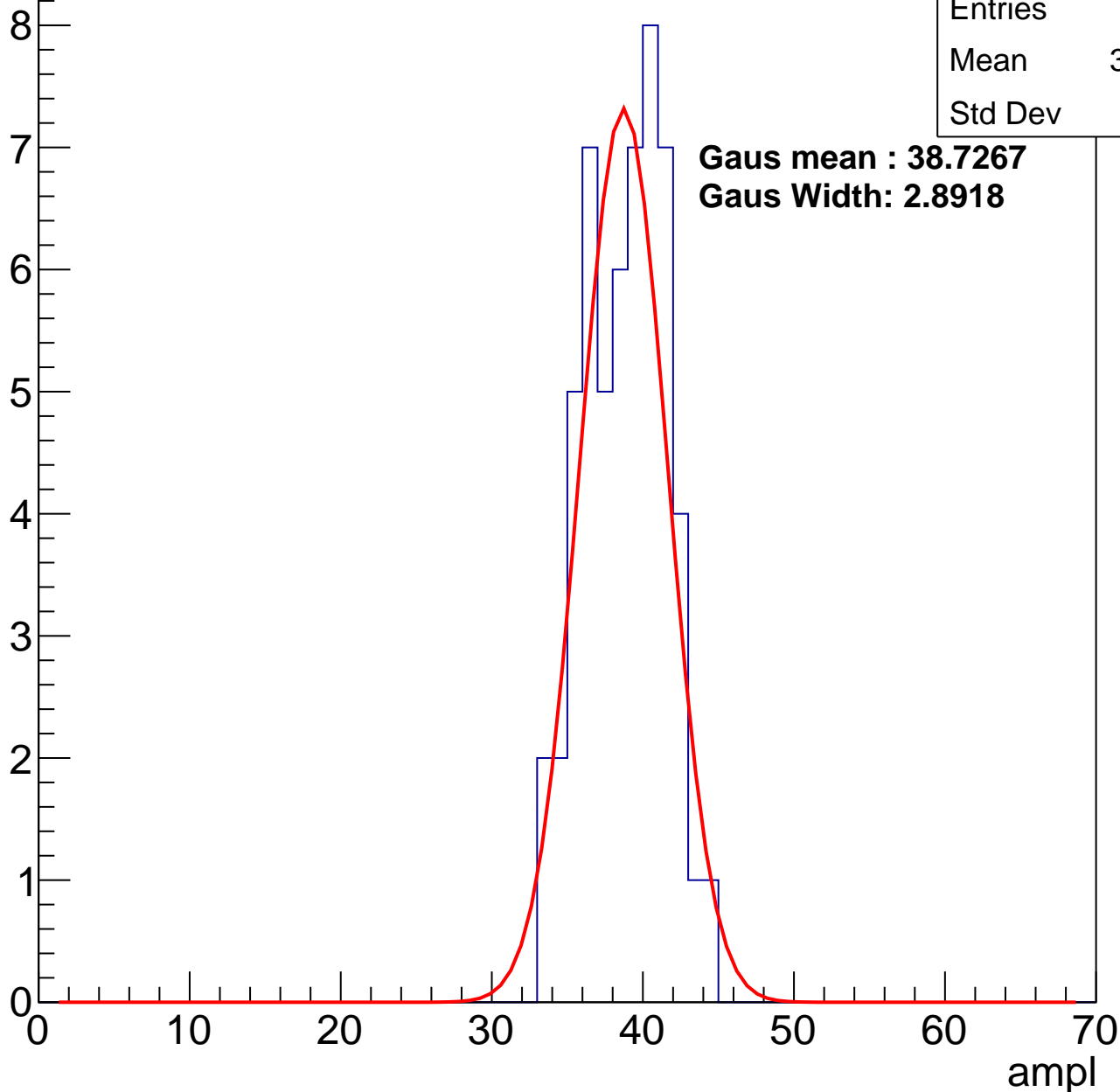
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	38.35
Std Dev	2.63

**Gaus mean : 38.7267**

**Gaus Width: 2.8918**



# B1L101S, U11-ch26, adc2

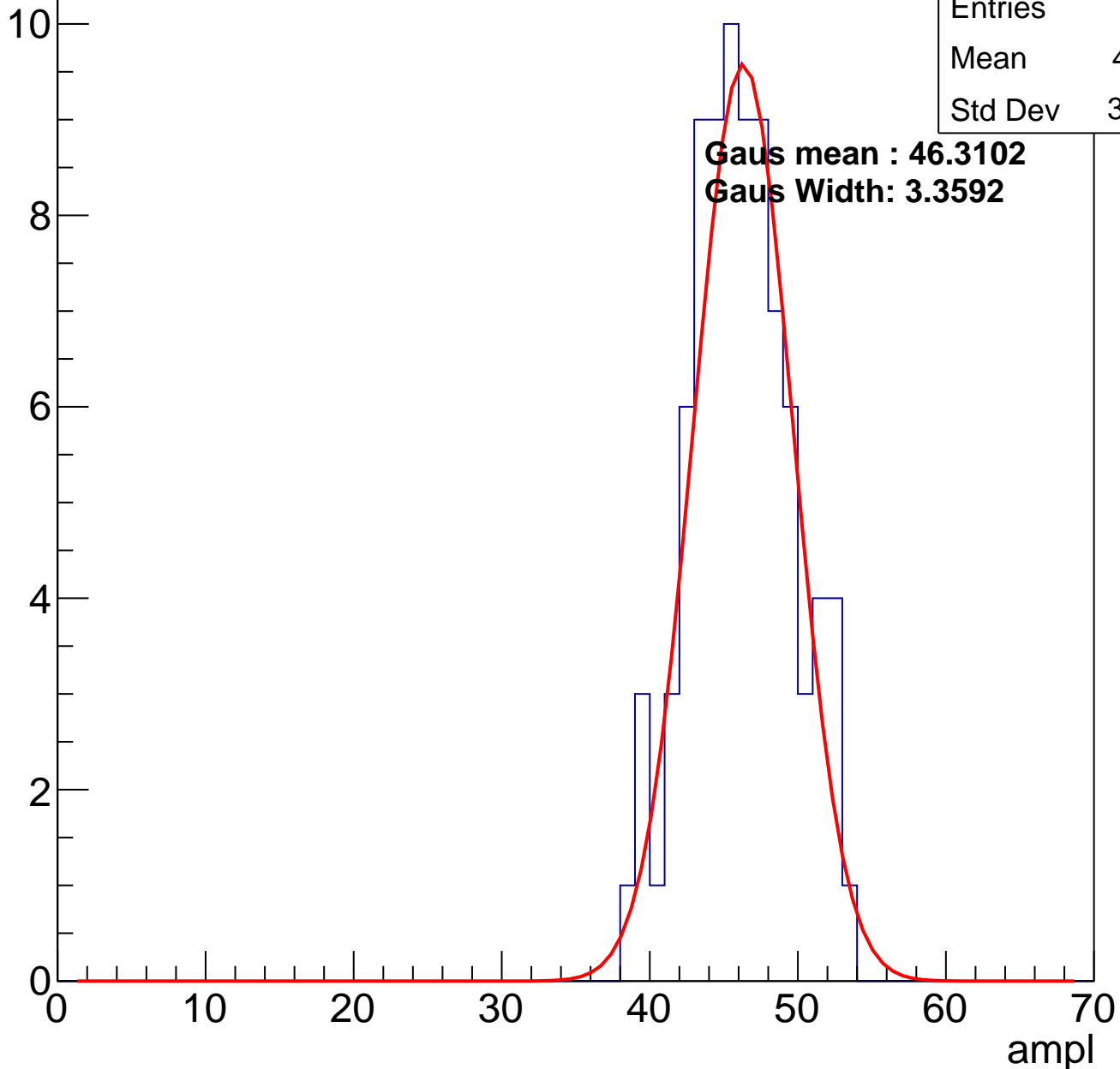
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	85
Mean	45.71
Std Dev	3.378

**Gaus mean : 46.3102**

**Gaus Width: 3.3592**

Entry

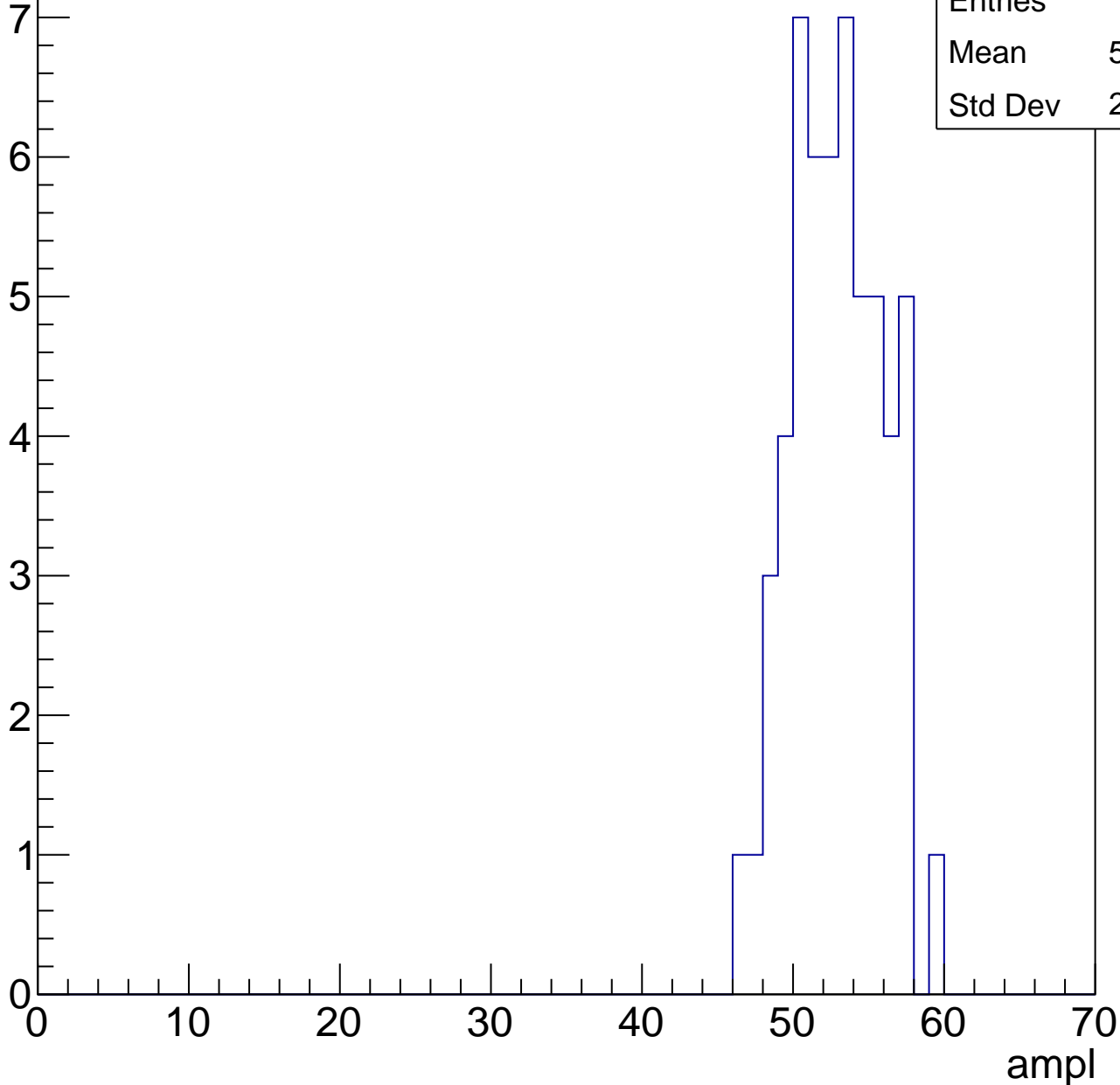


# B1L101S, U11-ch26, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	52.45
Std Dev	2.947



# B1L101S, U11-ch26, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	54
Mean	57.89
Std Dev	2.692

Entry

10

8

6

4

2

0

0

10

20

30

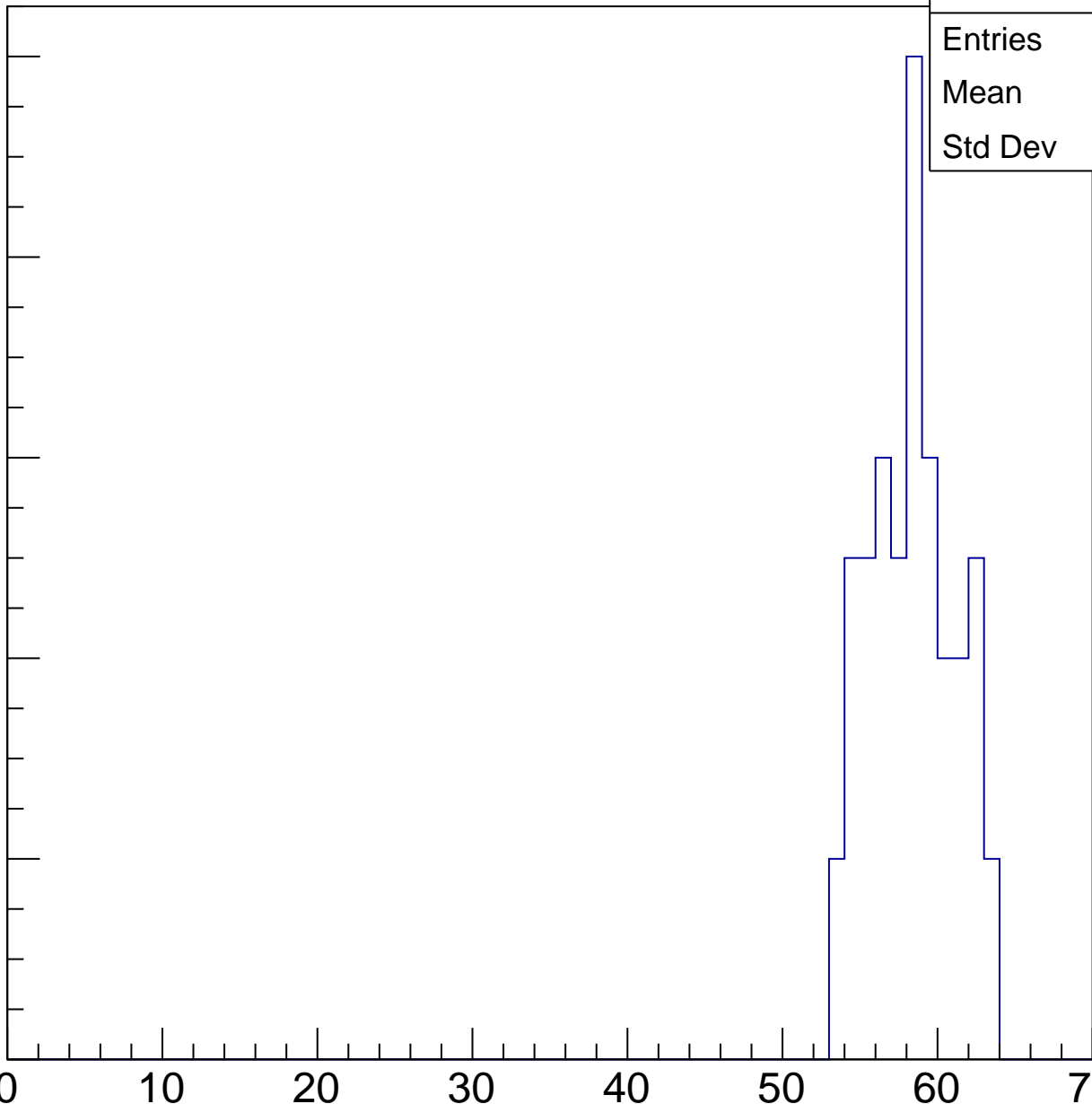
40

50

60

70

ampl

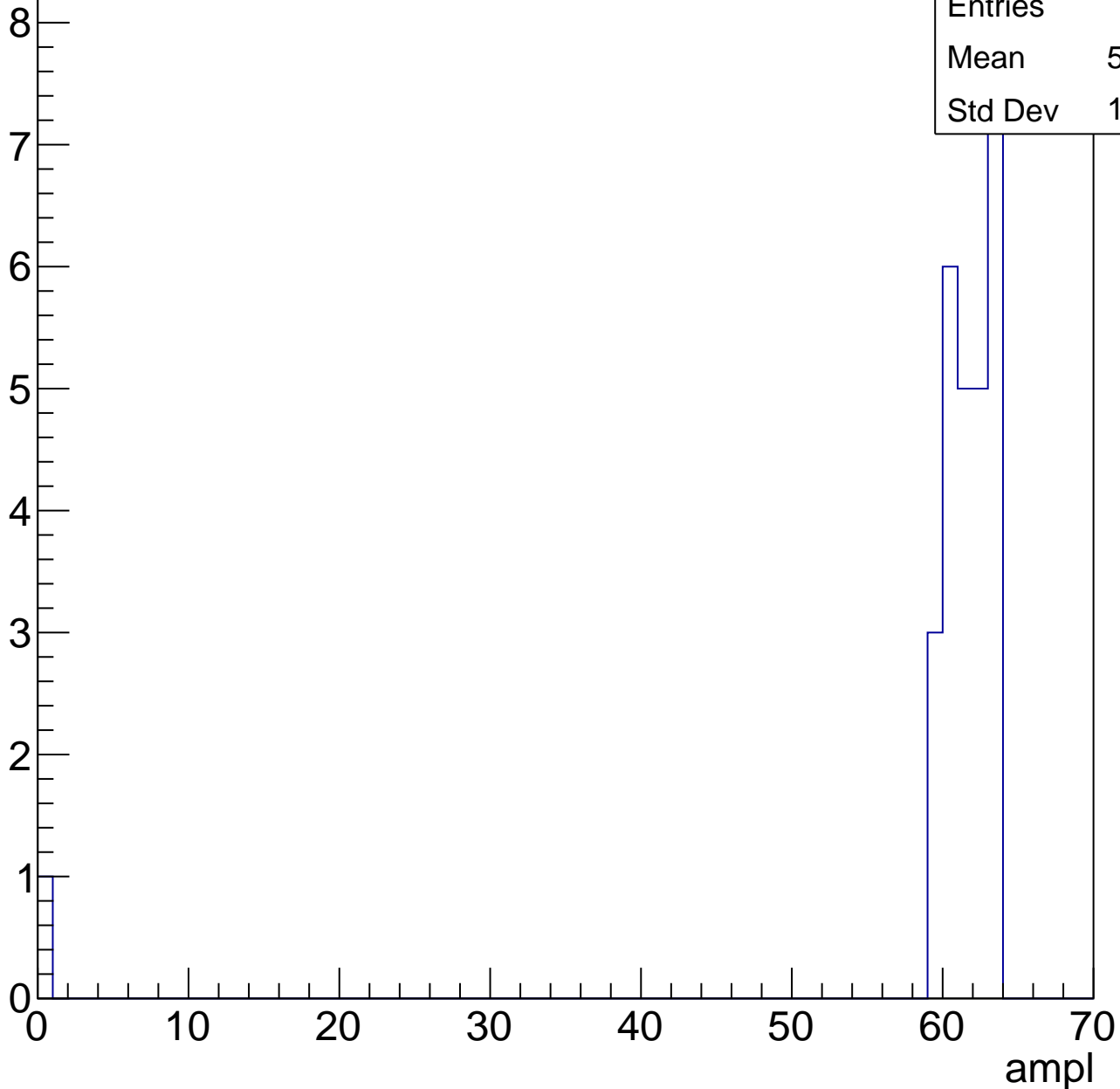


# B1L101S, U11-ch26, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	28
Mean	59.14
Std Dev	11.46



# B1L101S, U11-ch26, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch26, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U11-ch27, adc0

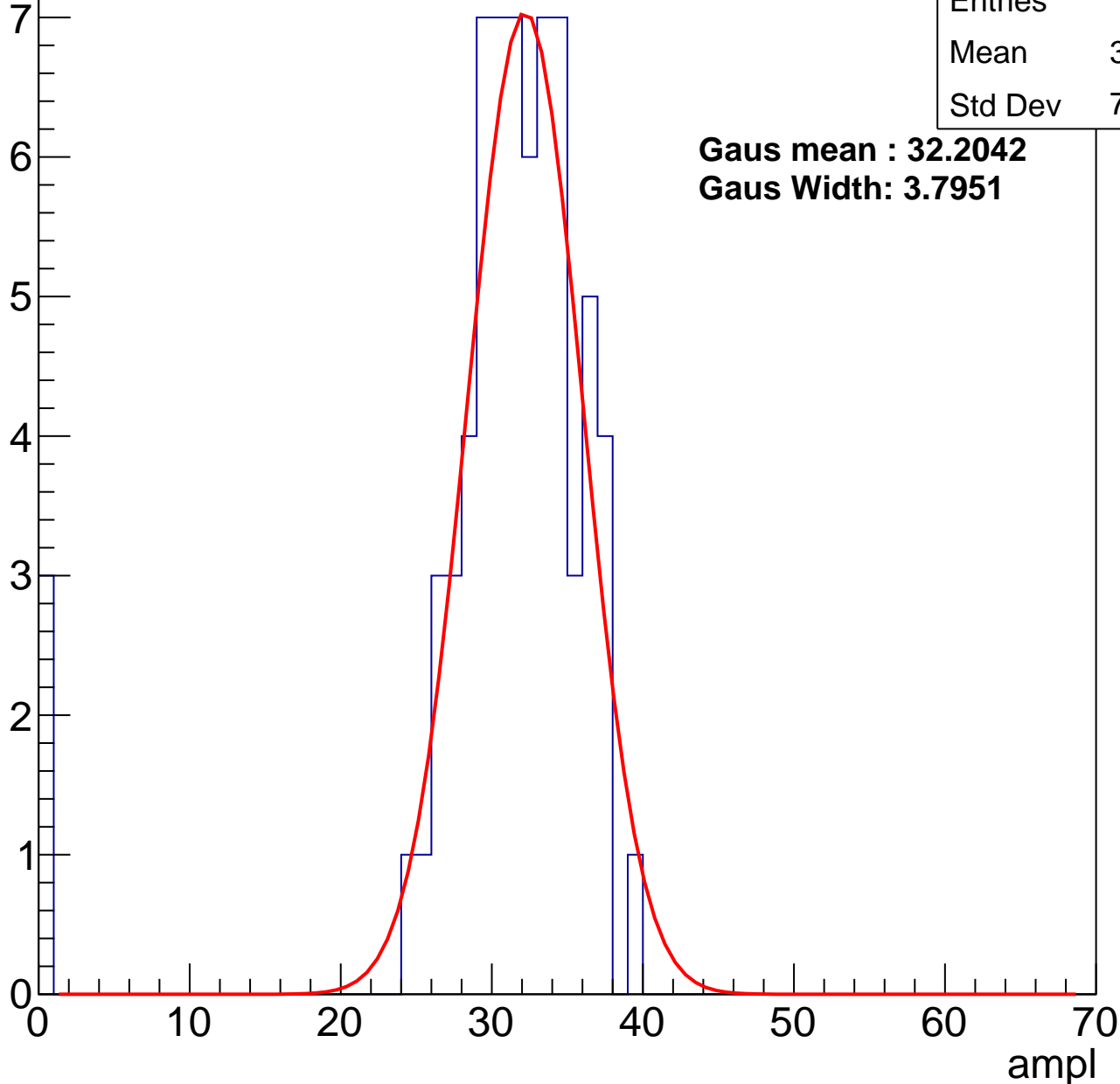
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	30.19
Std Dev	7.218

**Gaus mean : 32.2042**

**Gaus Width: 3.7951**



# B1L101S, U11-ch27, adc1

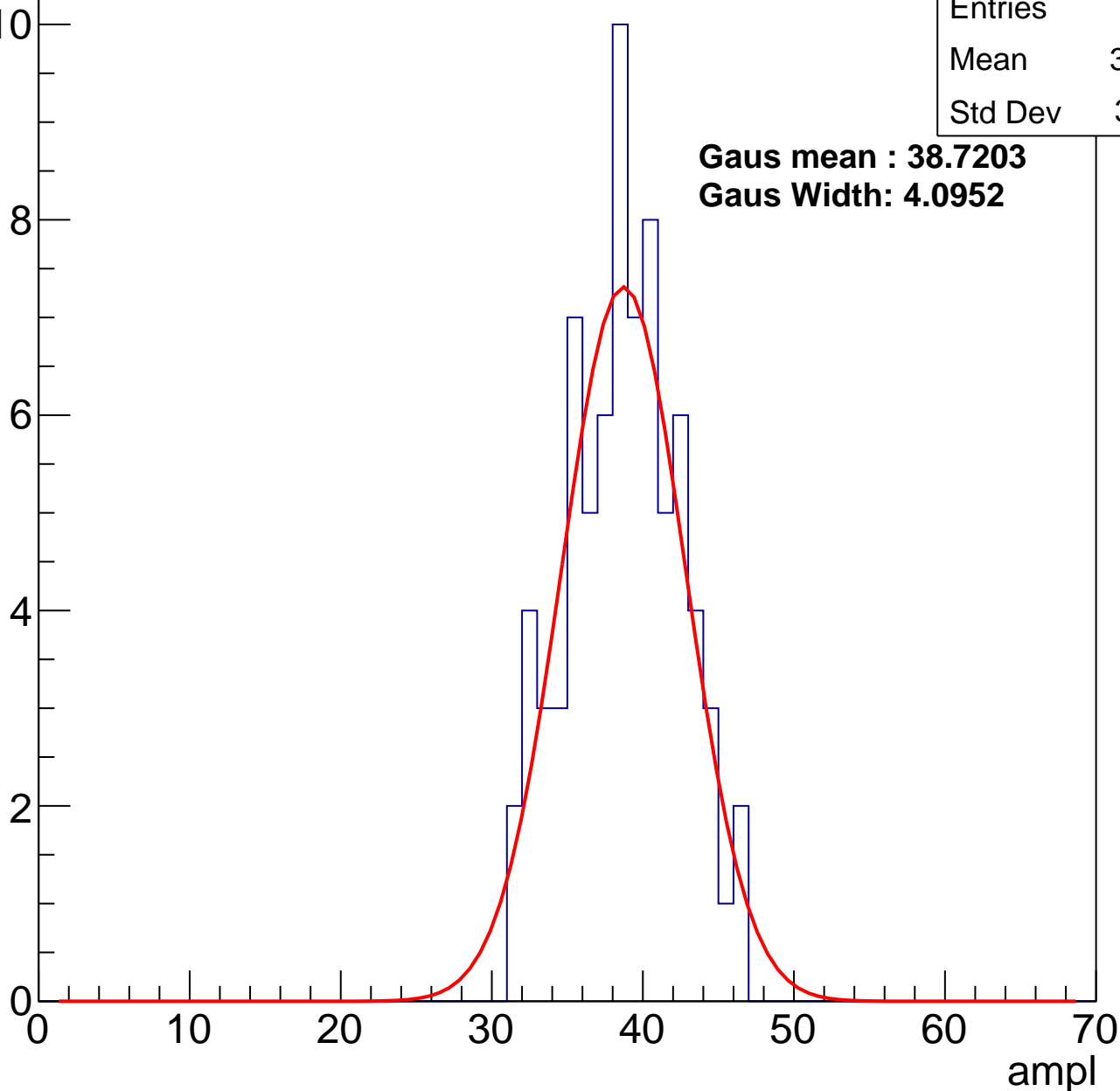
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	38.28
Std Dev	3.651

**Gaus mean : 38.7203**

**Gaus Width: 4.0952**



# B1L101S, U11-ch27, adc2

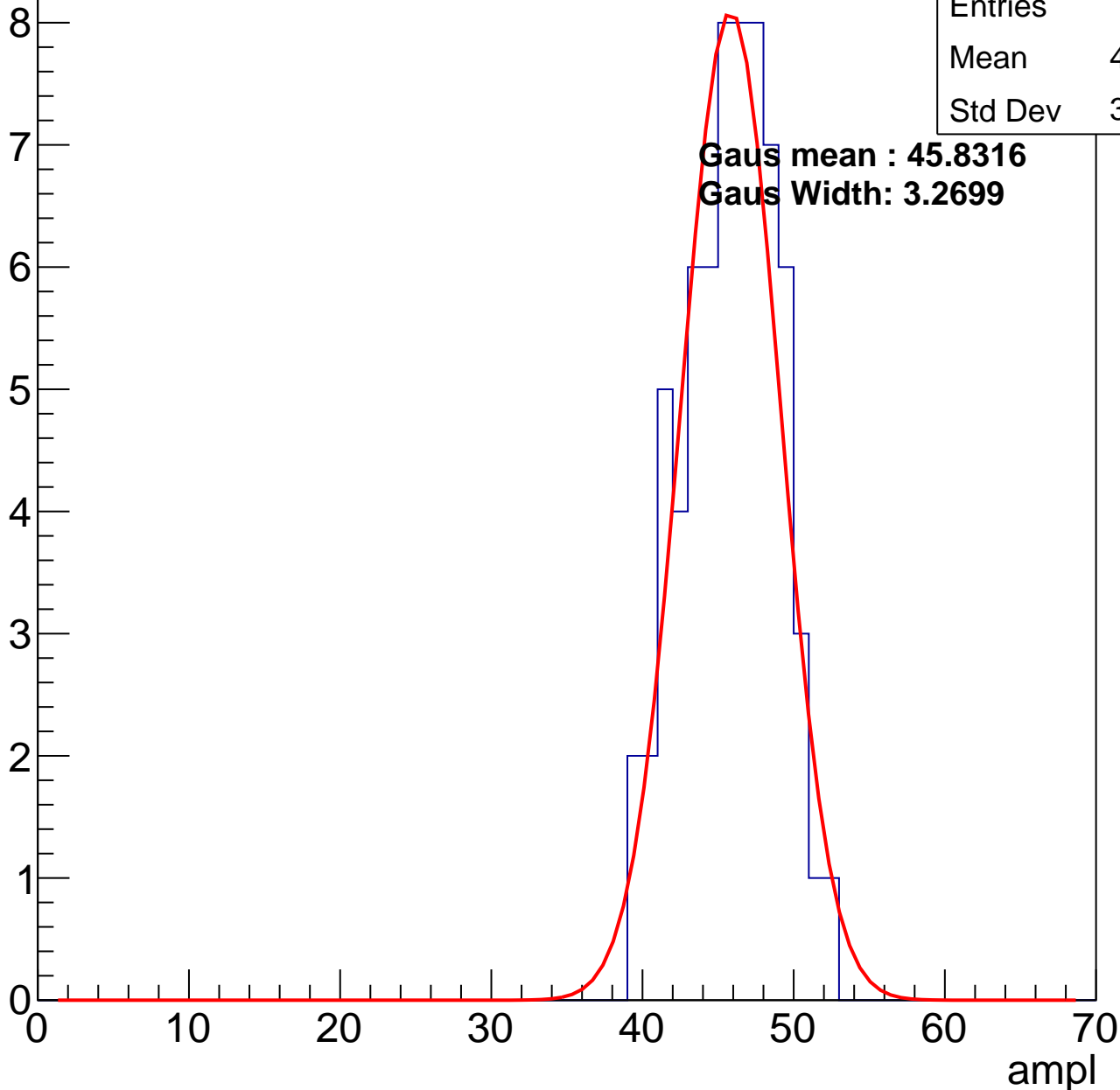
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	45.37
Std Dev	3.036

Gaus mean : 45.8316

Gaus Width: 3.2699

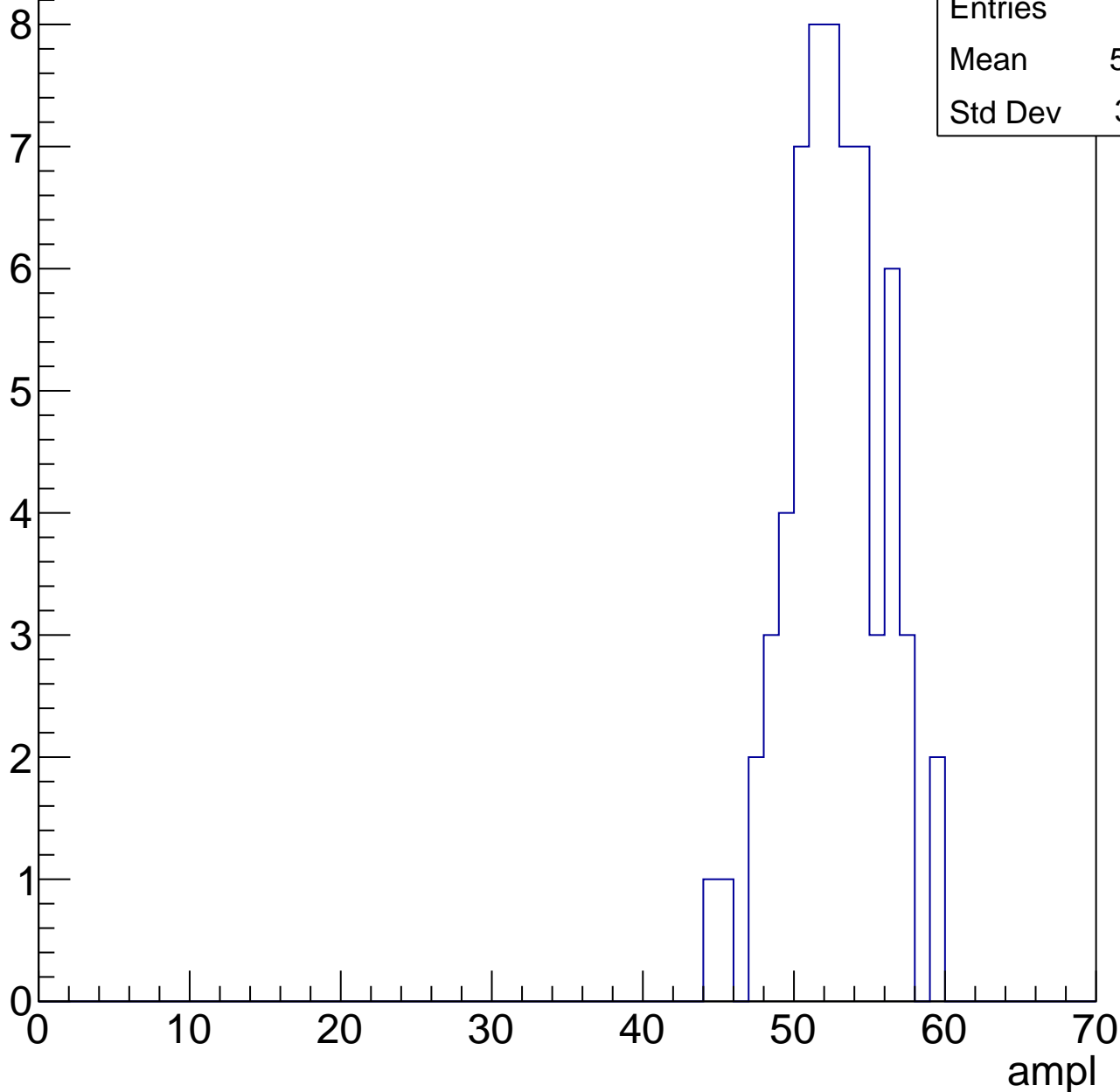


# B1L101S, U11-ch27, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	52.19
Std Dev	3.141



# B1L101S, U11-ch27, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	55
Mean	56.6
Std Dev	8.241

Entry

10

8

6

4

2

0

0

10

20

30

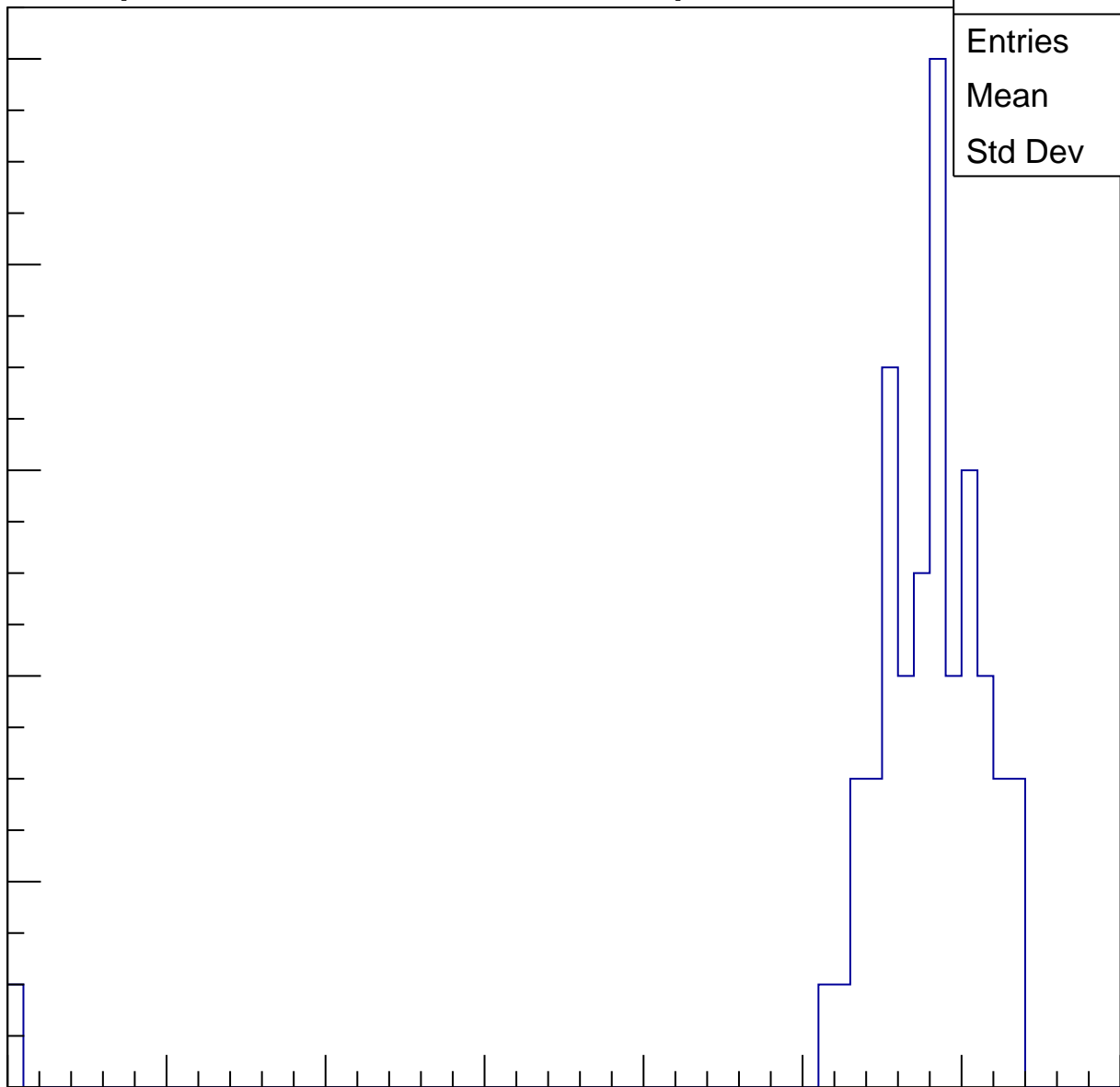
40

50

60

70

ampl

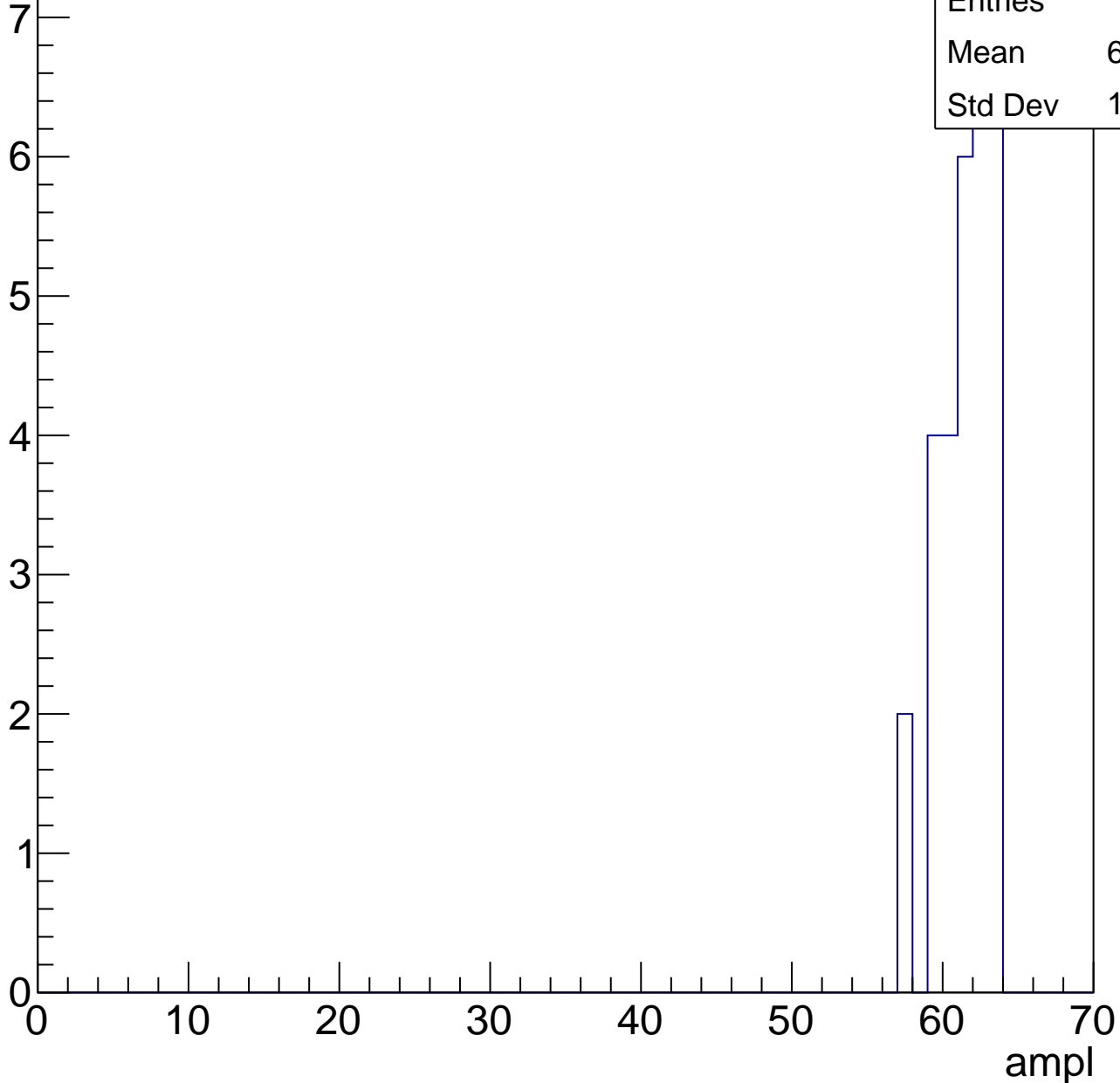


# B1L101S, U11-ch27, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	30
Mean	61.03
Std Dev	1.703



# B1L101S, U11-ch27, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L101S, U11-ch27, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U11-ch28, adc0

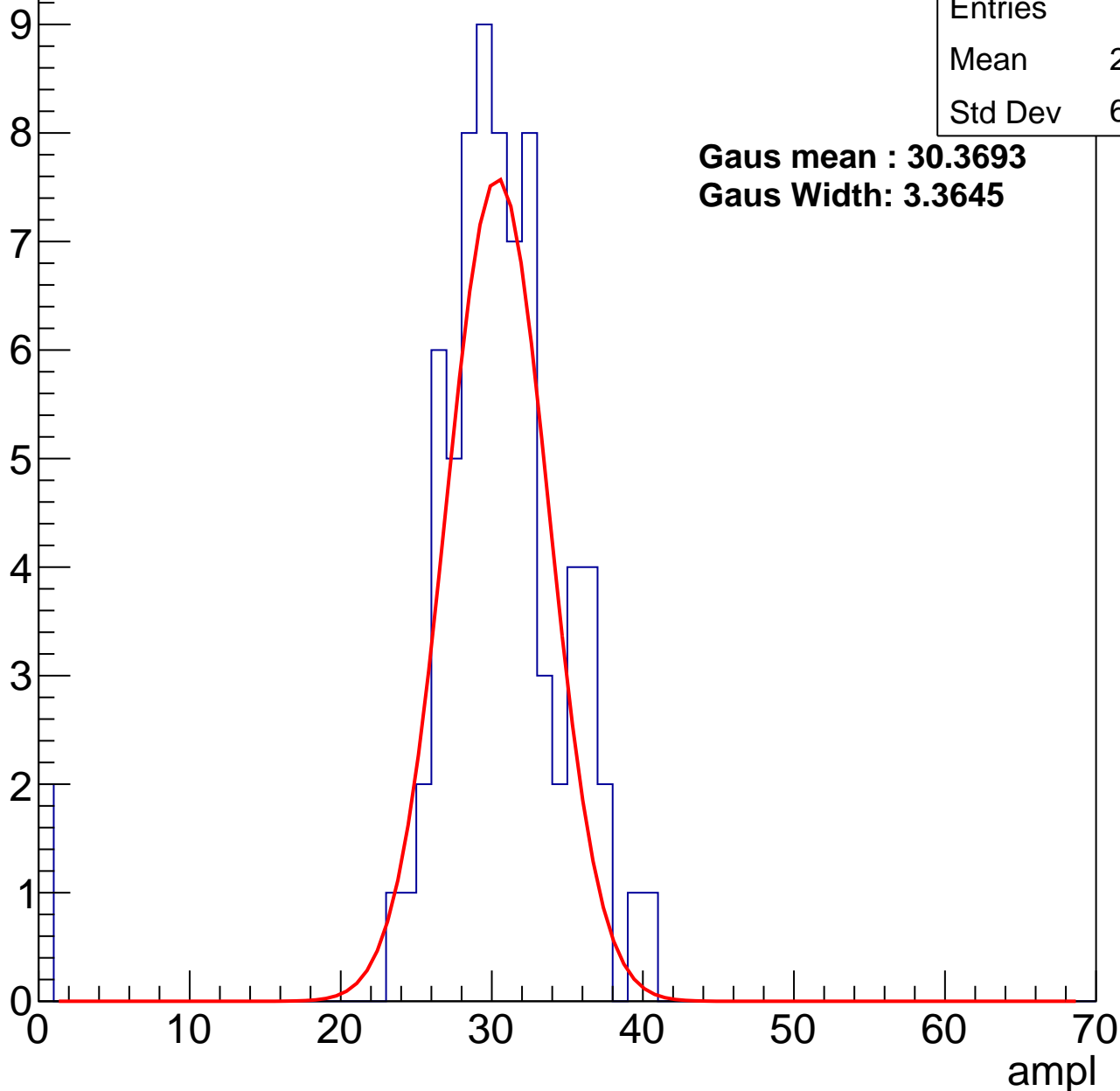
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	29.59
Std Dev	6.069

**Gaus mean : 30.3693**

**Gaus Width: 3.3645**



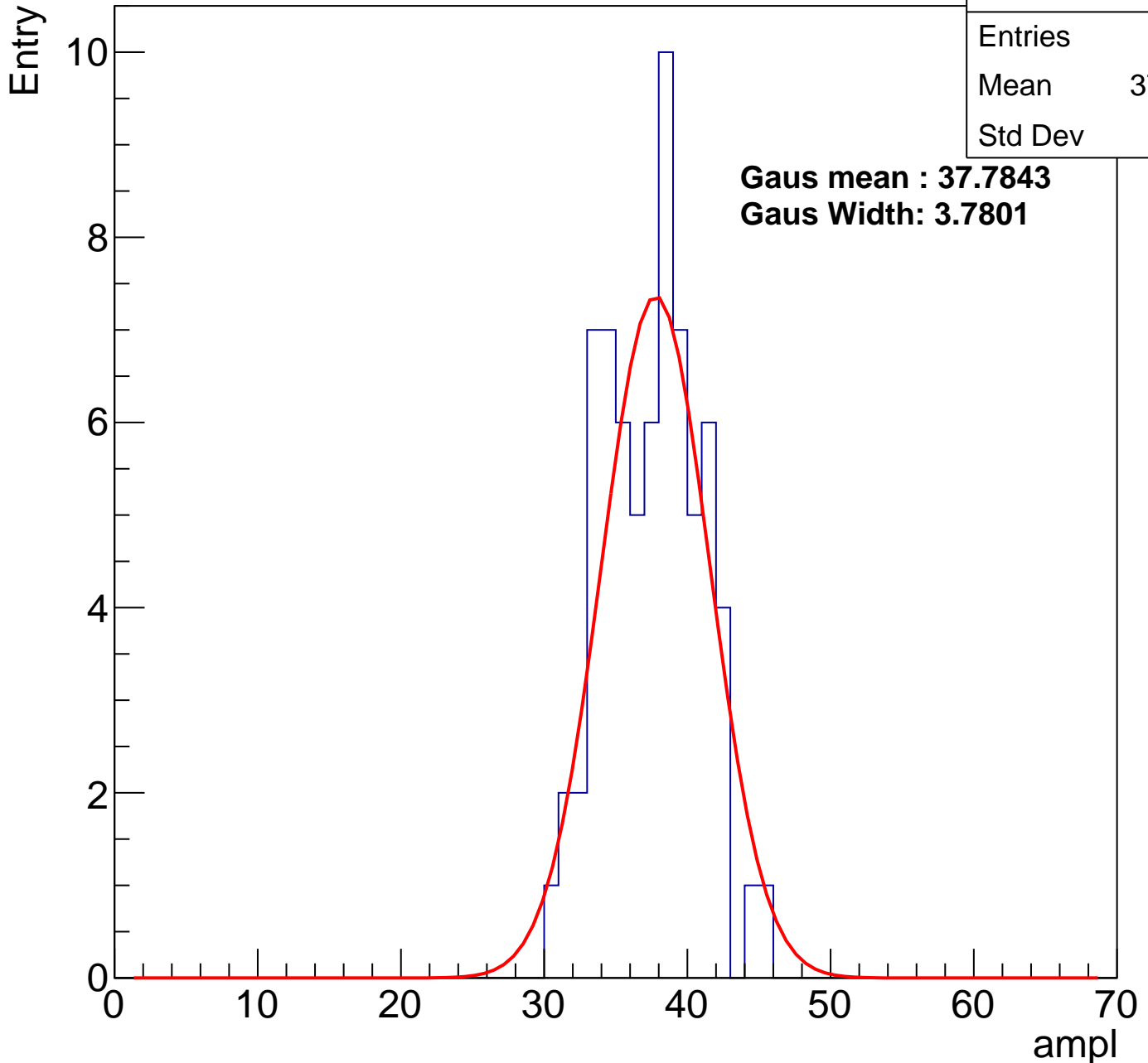
# B1L101S, U11-ch28, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	70
Mean	37.04
Std Dev	3.31

**Gaus mean : 37.7843**

**Gaus Width: 3.7801**



# B1L101S, U11-ch28, adc2

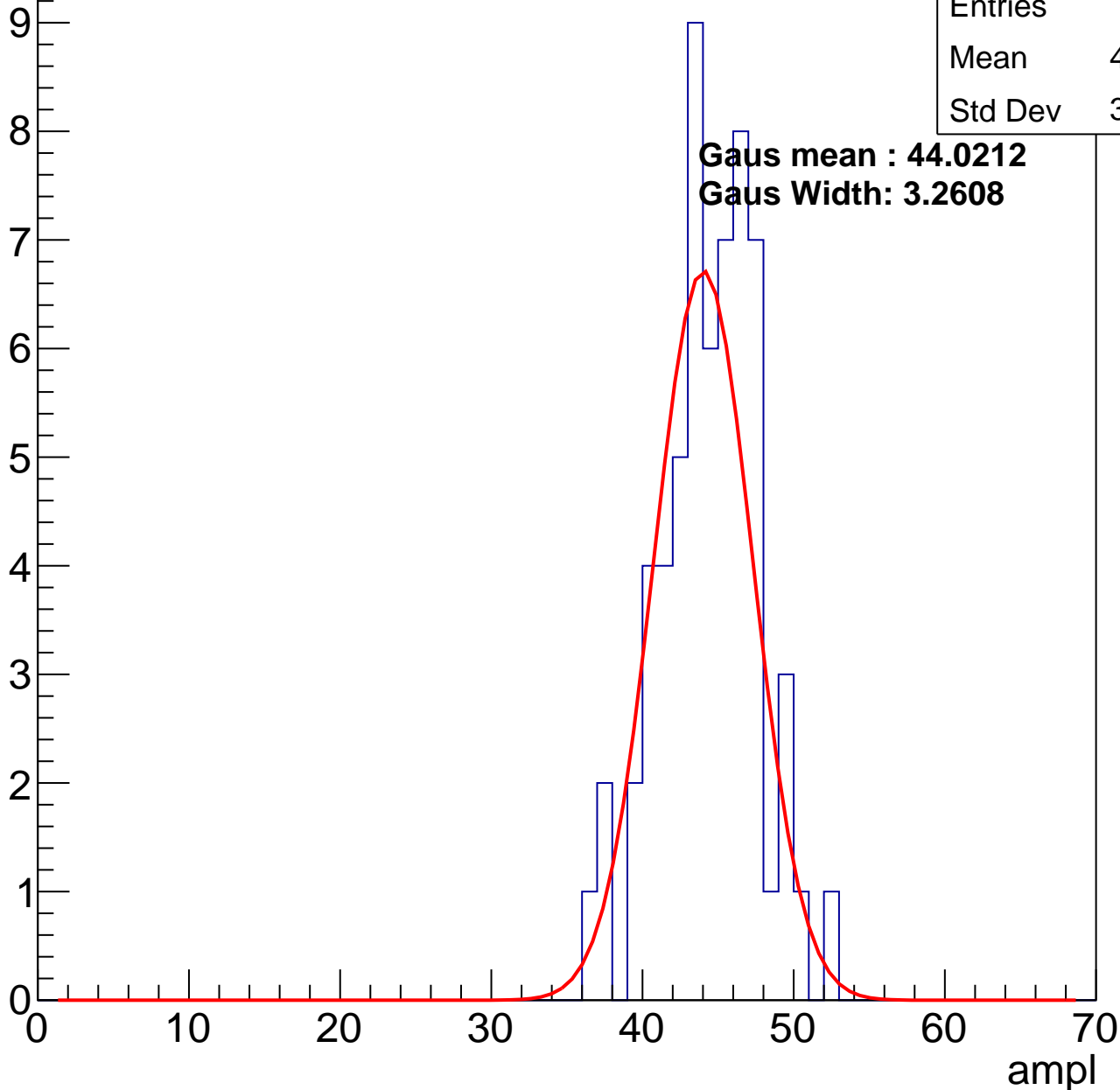
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	43.97
Std Dev	3.224

**Gaus mean : 44.0212**

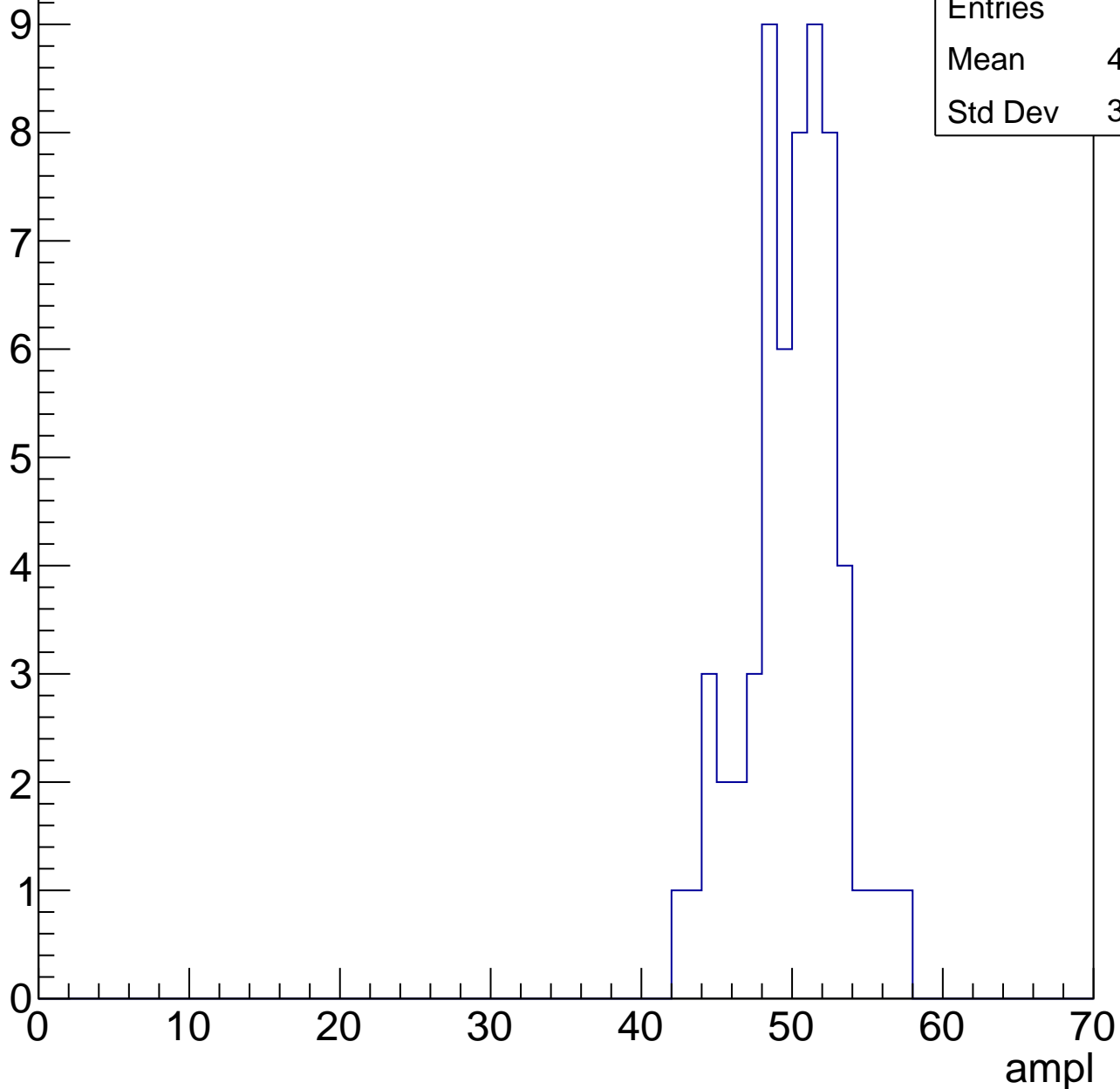
**Gaus Width: 3.2608**



# B1L101S, U11-ch28, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

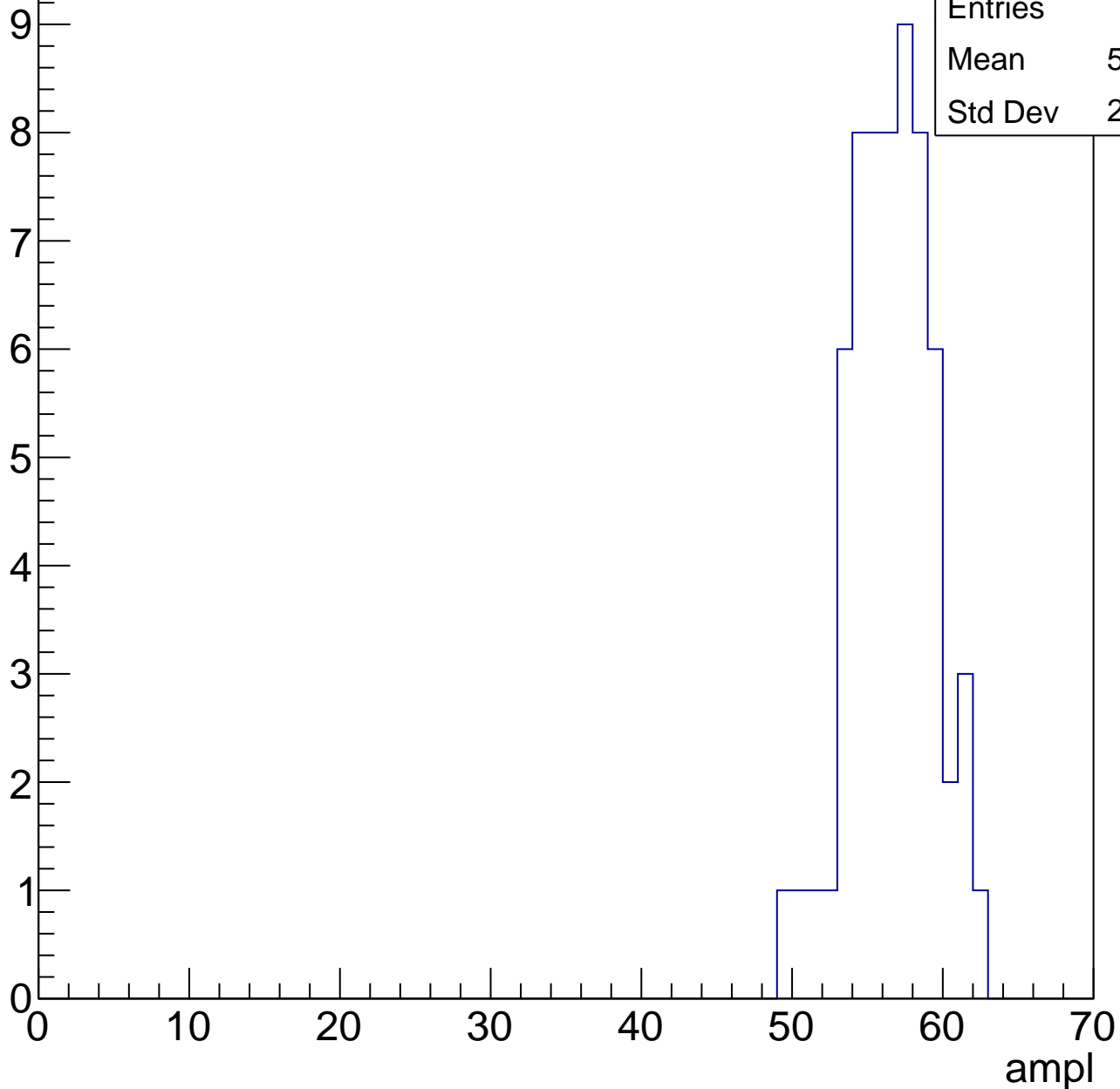


Entries	60
Mean	49.58
Std Dev	3.068

# B1L101S, U11-ch28, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U11-ch28, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

10

Entries 44

Mean 59.36

Std Dev 9.298

8

6

4

2

0

0

10

20

30

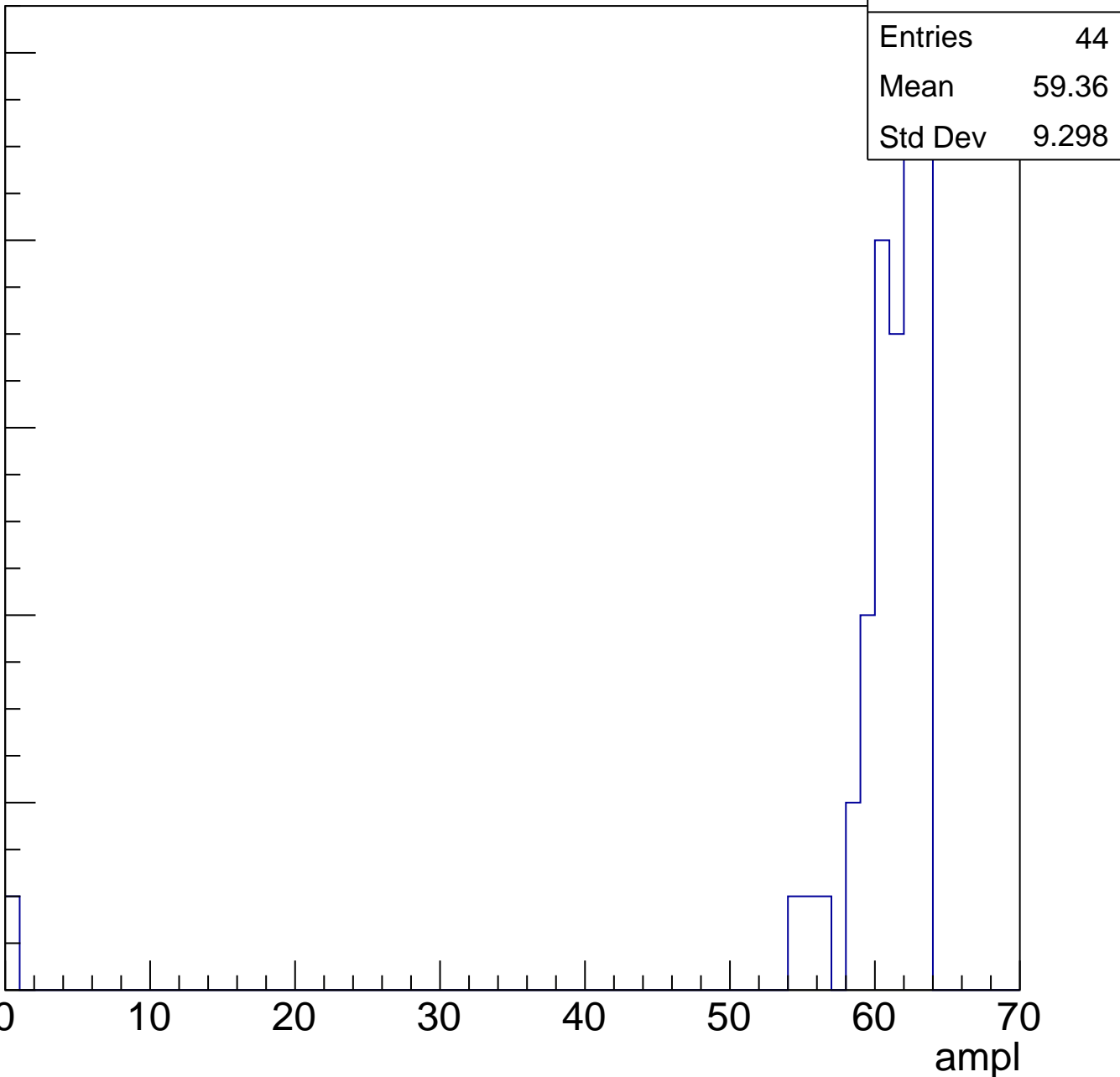
40

50

60

70

ampl



# B1L101S, U11-ch28, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch28, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U11-ch29, adc0

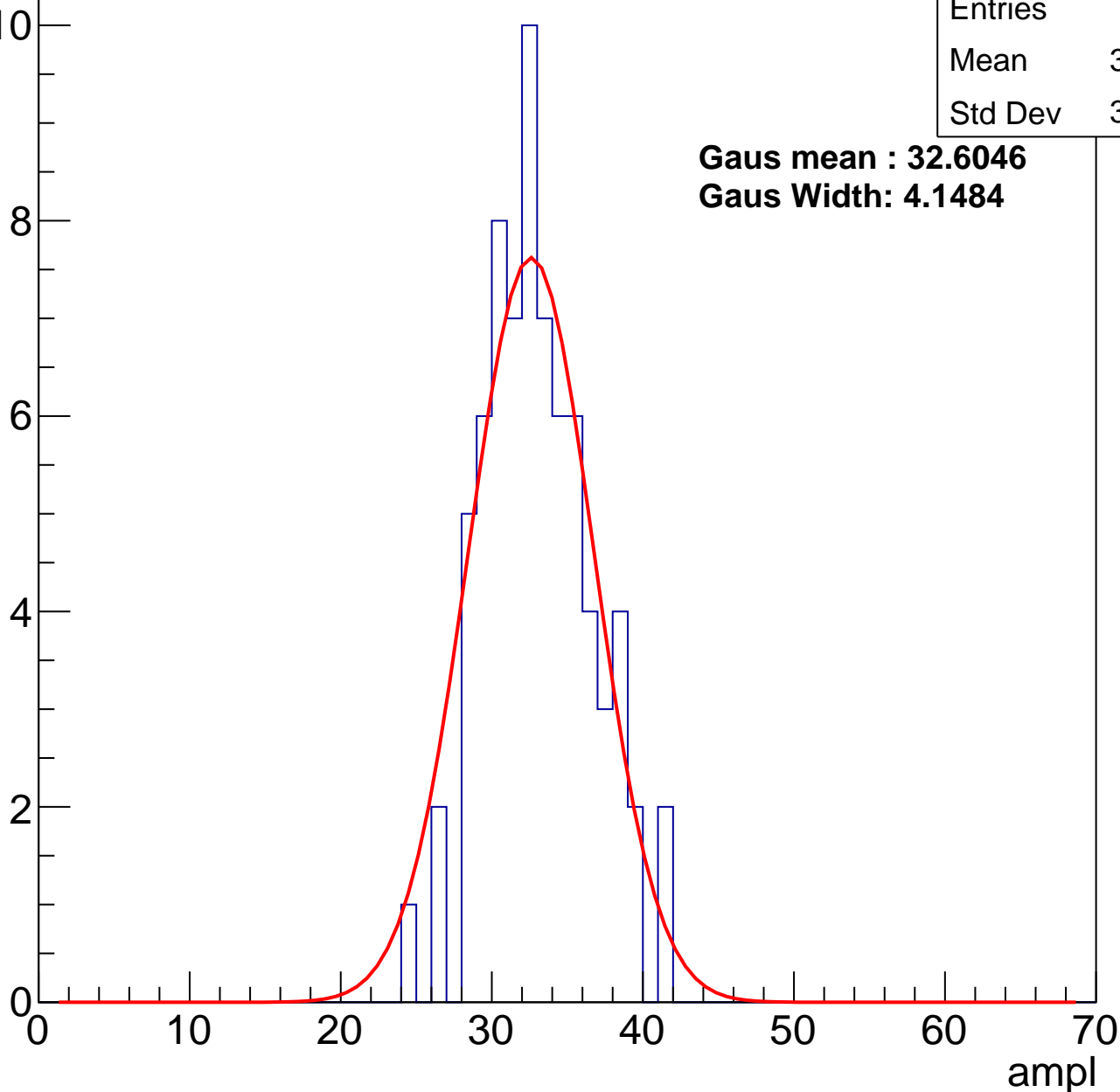
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	32.59
Std Dev	3.534

**Gaus mean : 32.6046**

**Gaus Width: 4.1484**



# B1L101S, U11-ch29, adc1

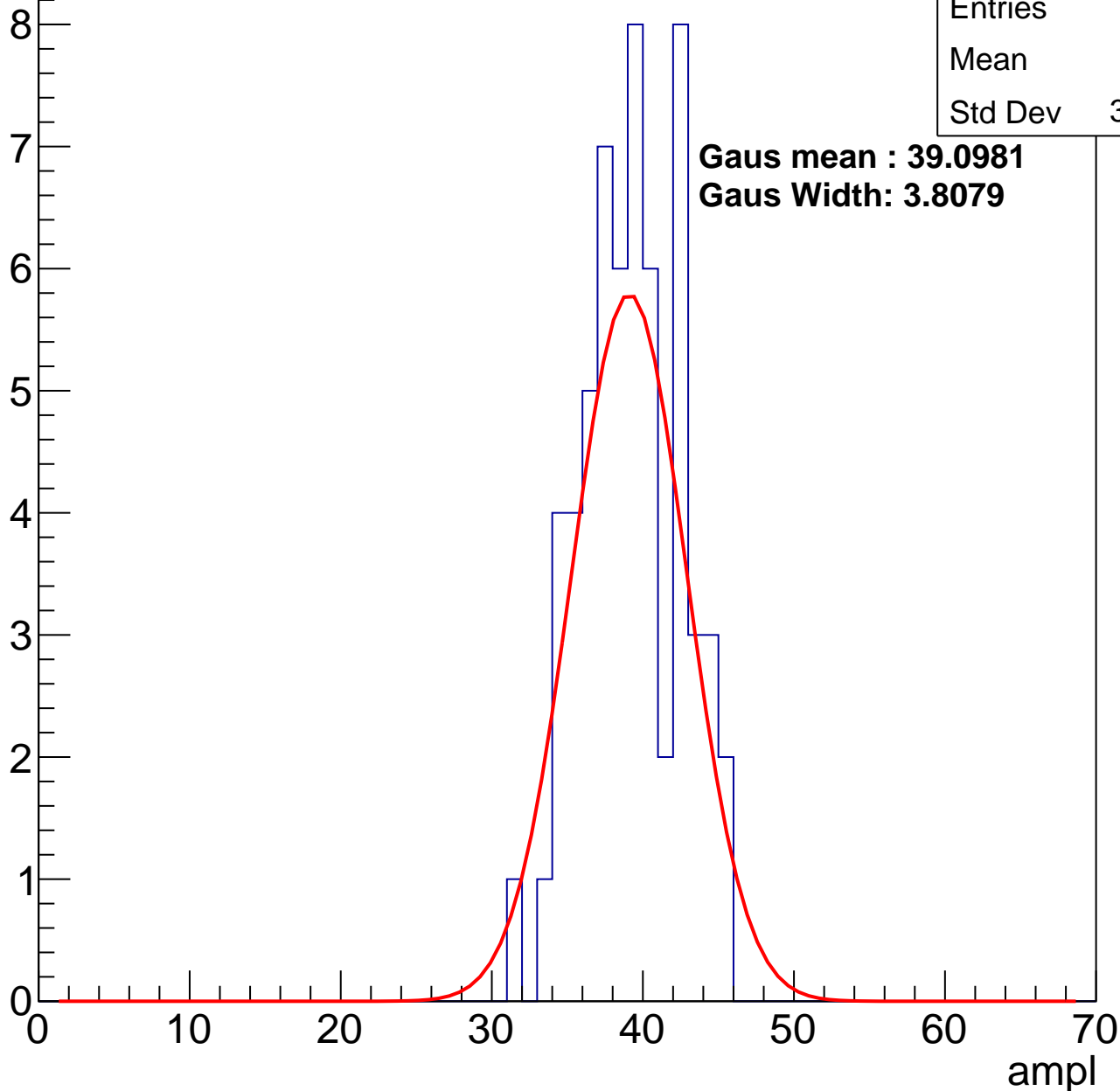
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	38.8
Std Dev	3.219

**Gaus mean : 39.0981**

**Gaus Width: 3.8079**



# B1L101S, U11-ch29, adc2

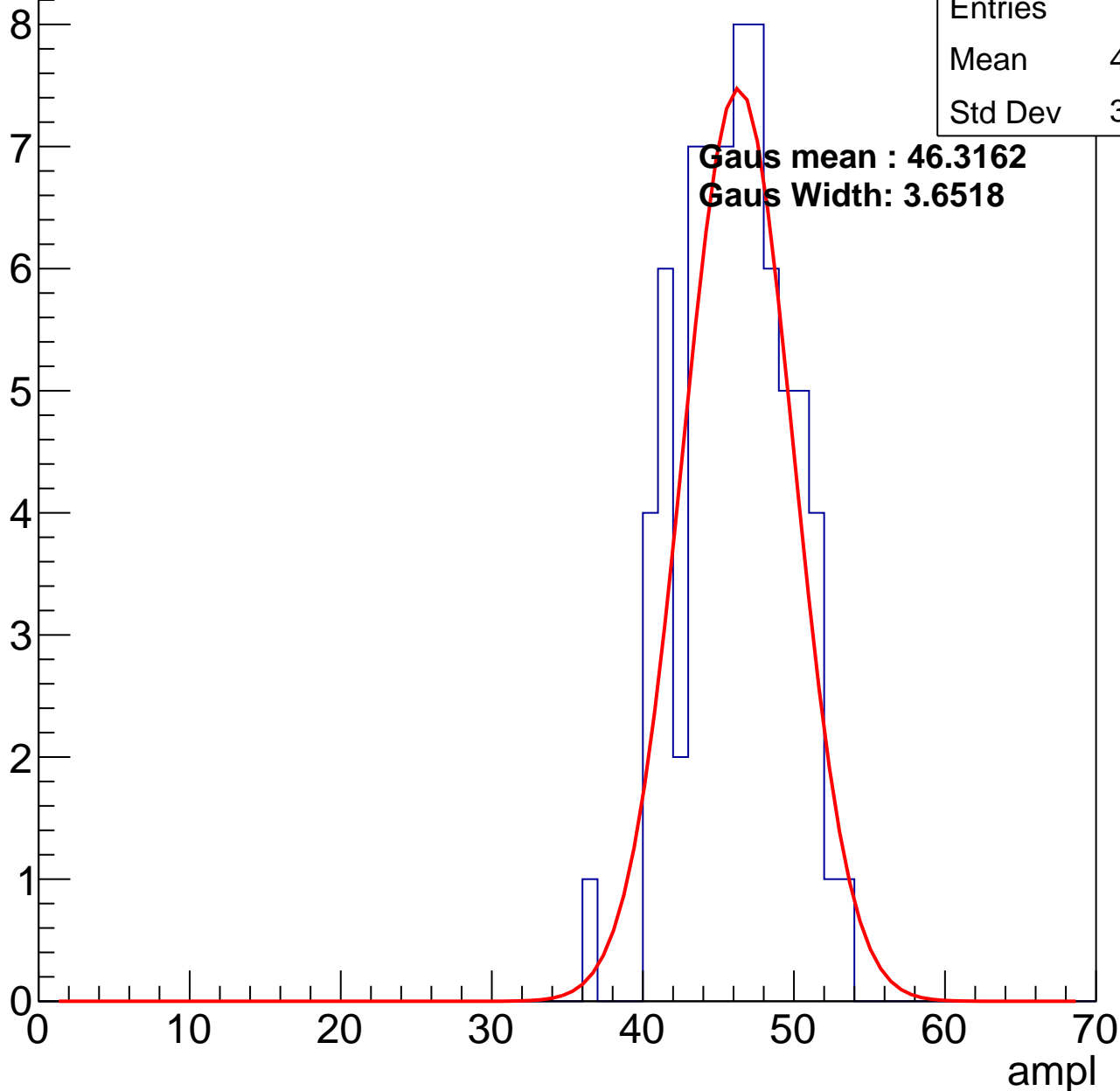
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	45.64
Std Dev	3.449

**Gaus mean : 46.3162**

**Gaus Width: 3.6518**

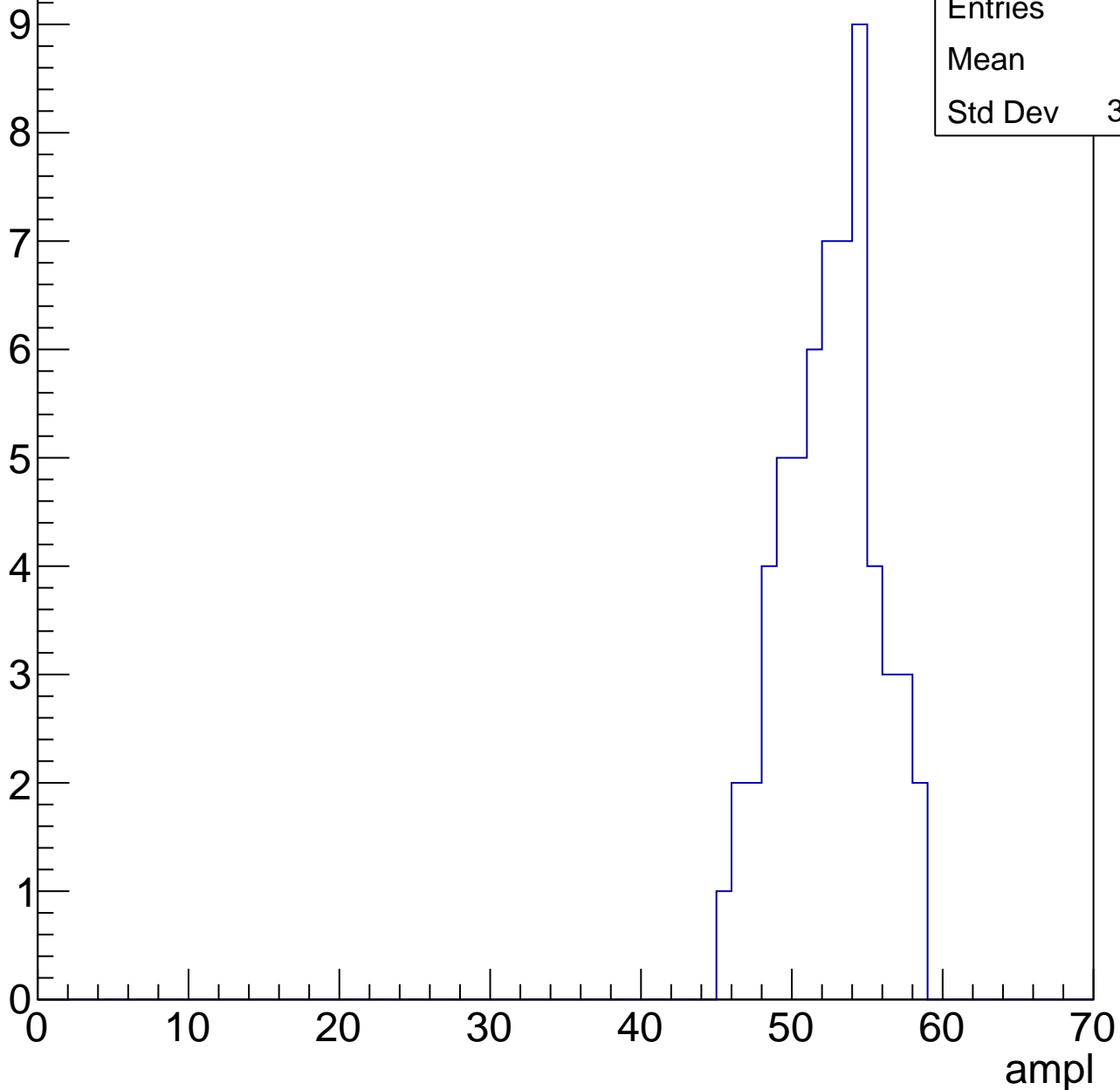


# B1L101S, U11-ch29, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

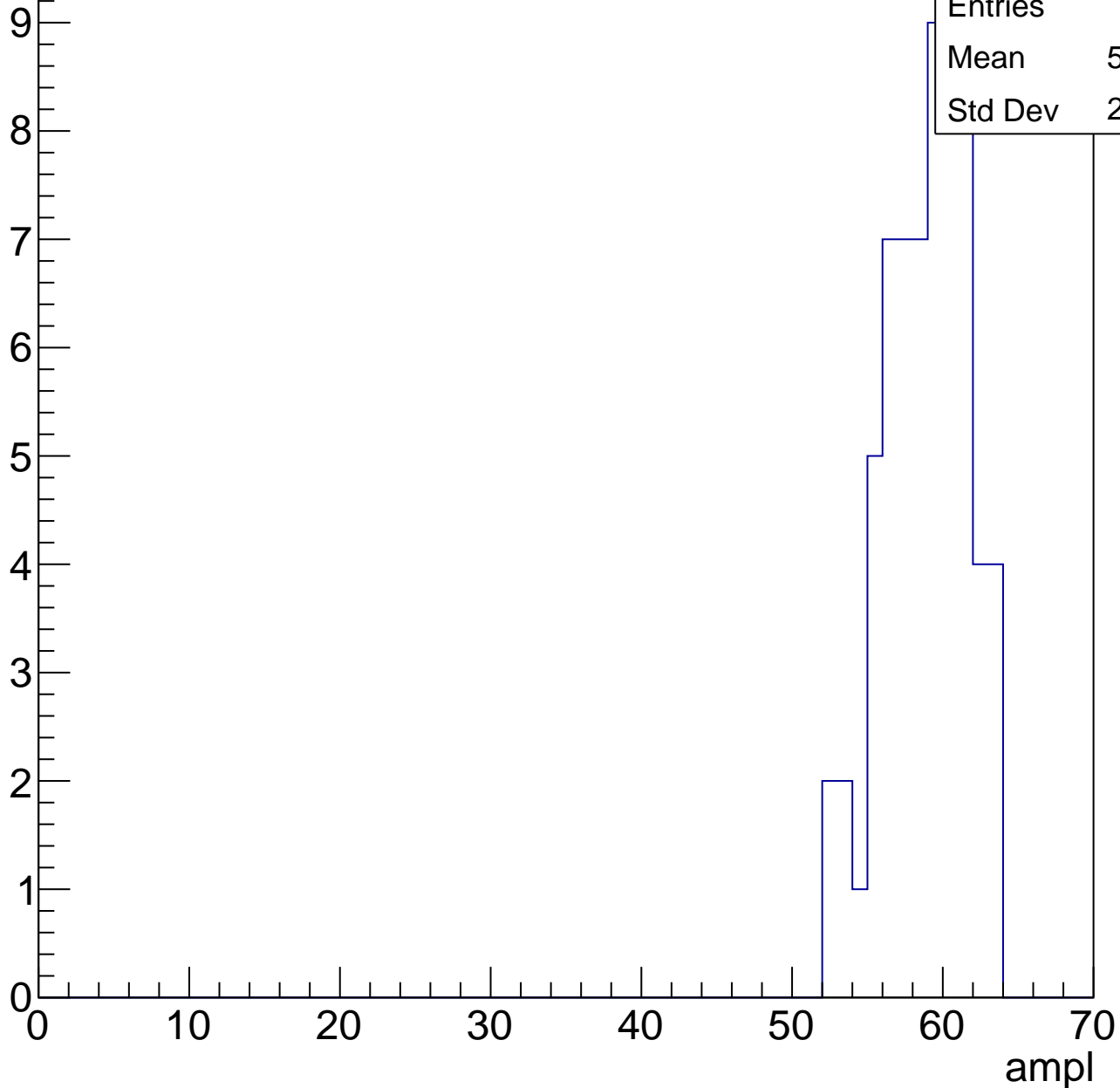
Entries	60
Mean	52
Std Dev	3.109



# B1L101S, U11-ch29, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

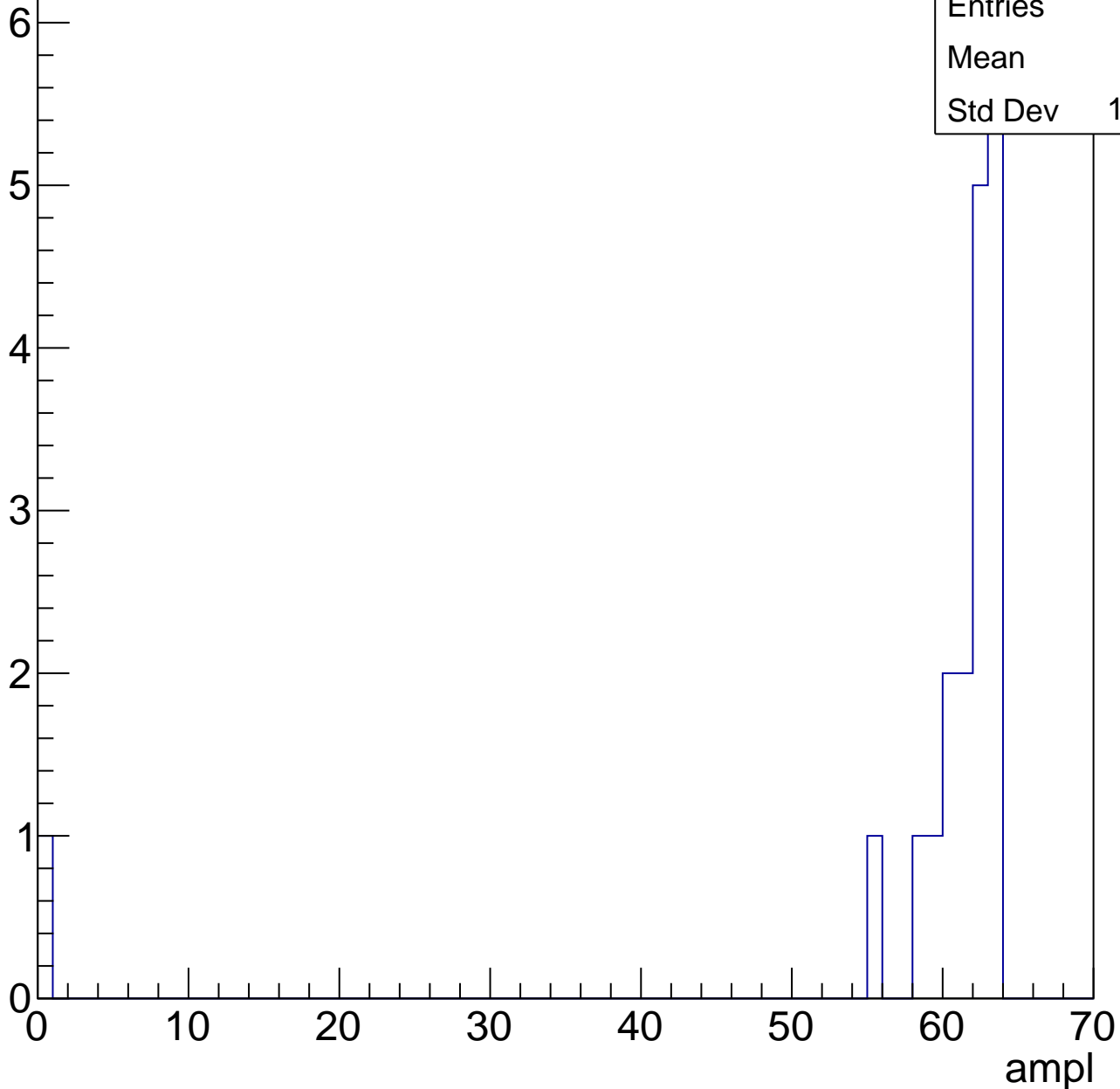


# B1L101S, U11-ch29, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	19
Mean	58
Std Dev	13.82



# B1L101S, U11-ch29, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch29, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U11-ch30, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	64
Mean	29.39
Std Dev	2.87

**Gaus mean : 30.1332**

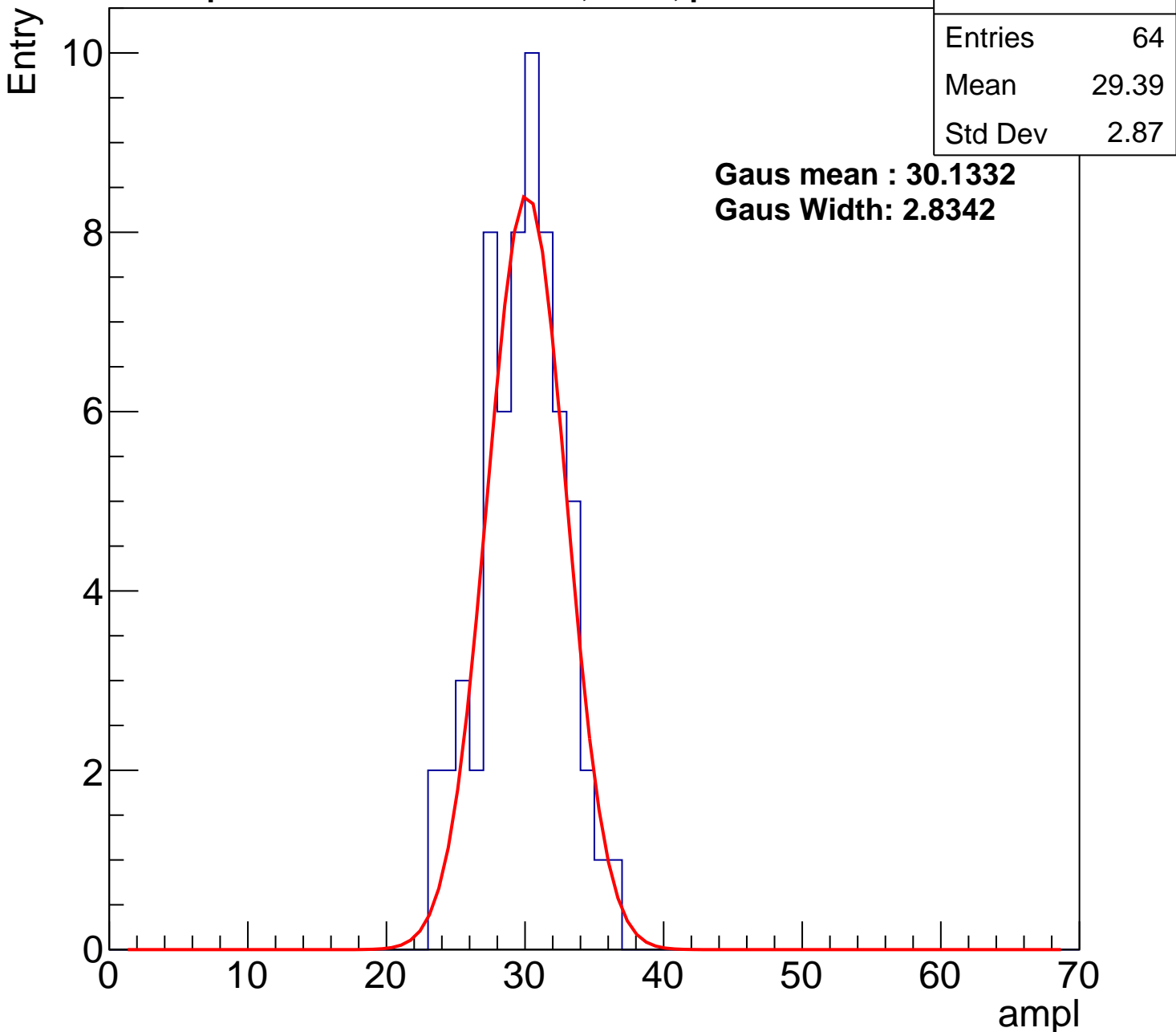
**Gaus Width: 2.8342**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U11-ch30, adc1

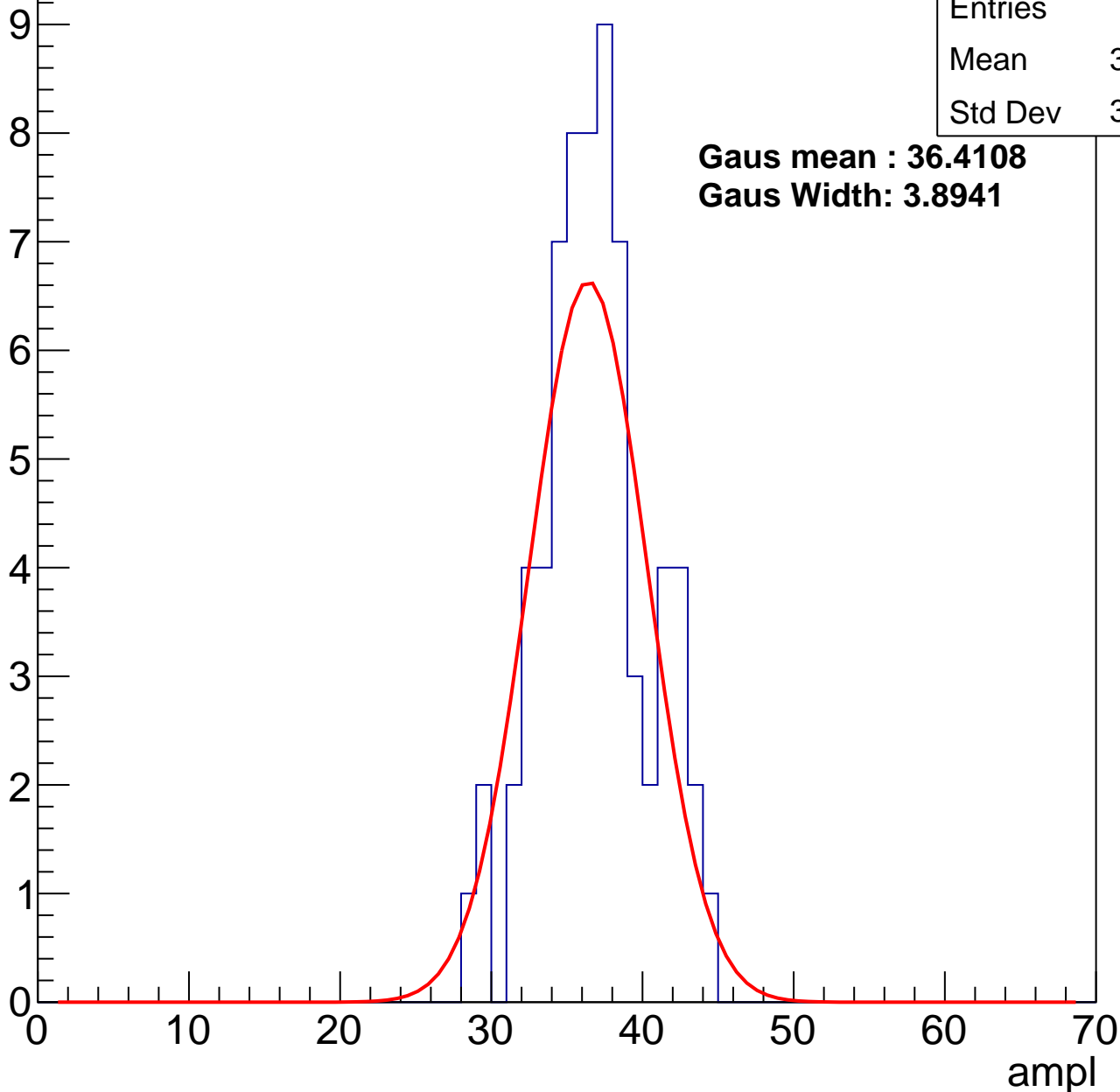
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	36.35
Std Dev	3.518

**Gaus mean : 36.4108**

**Gaus Width: 3.8941**



# B1L101S, U11-ch30, adc2

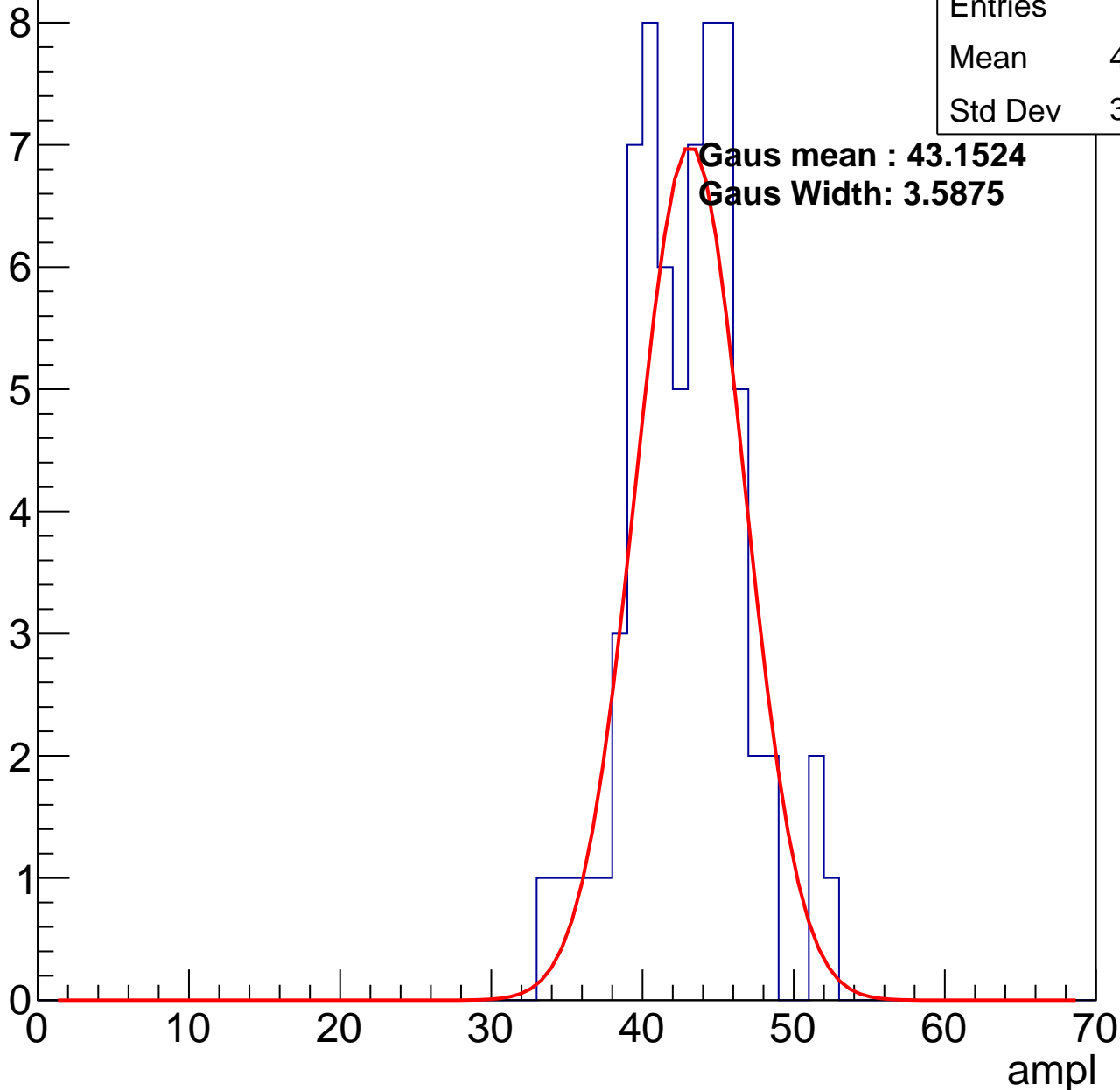
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	42.39
Std Dev	3.746

**Gaus mean : 43.1524**

**Gaus Width: 3.5875**

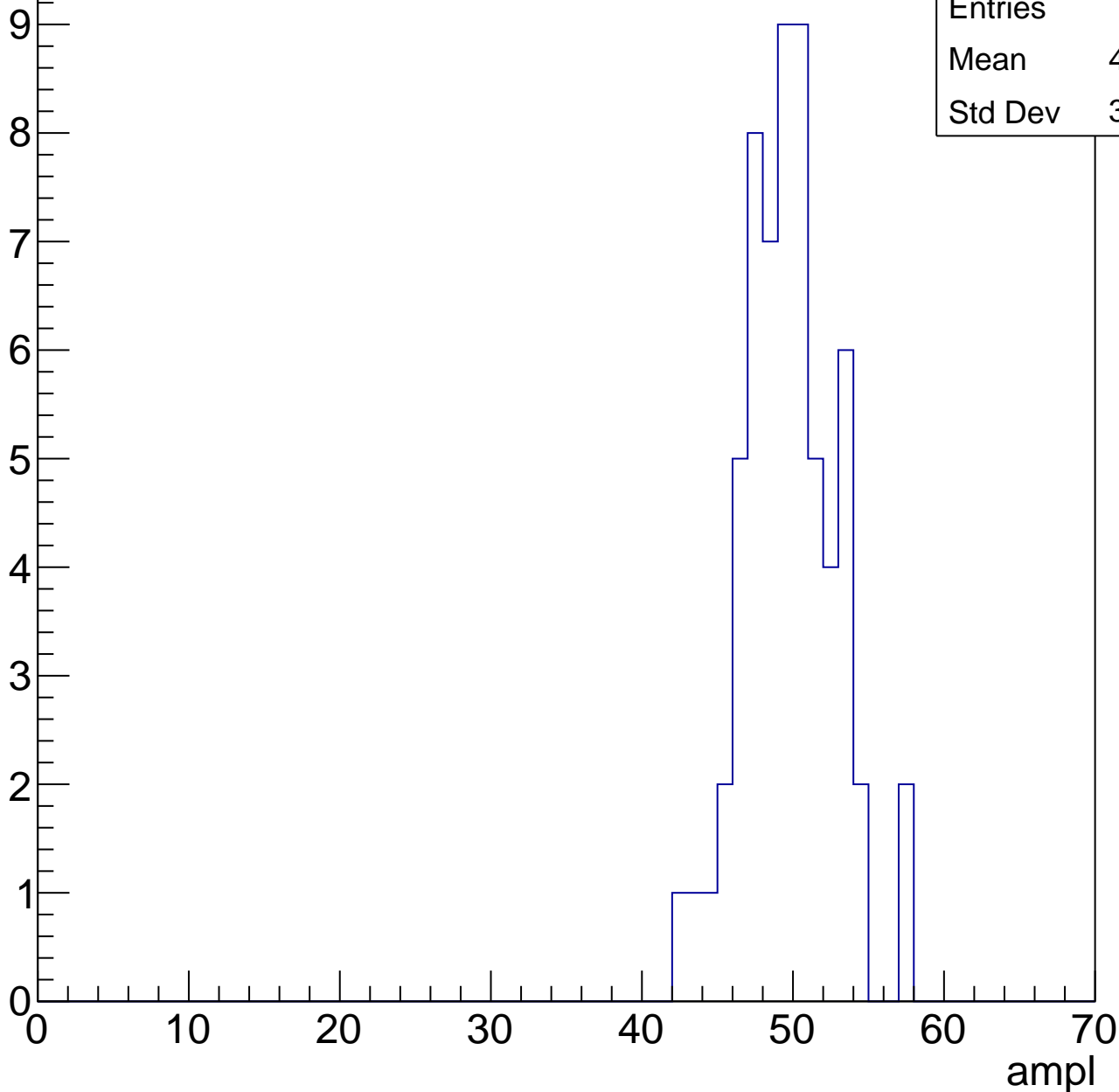


# B1L101S, U11-ch30, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

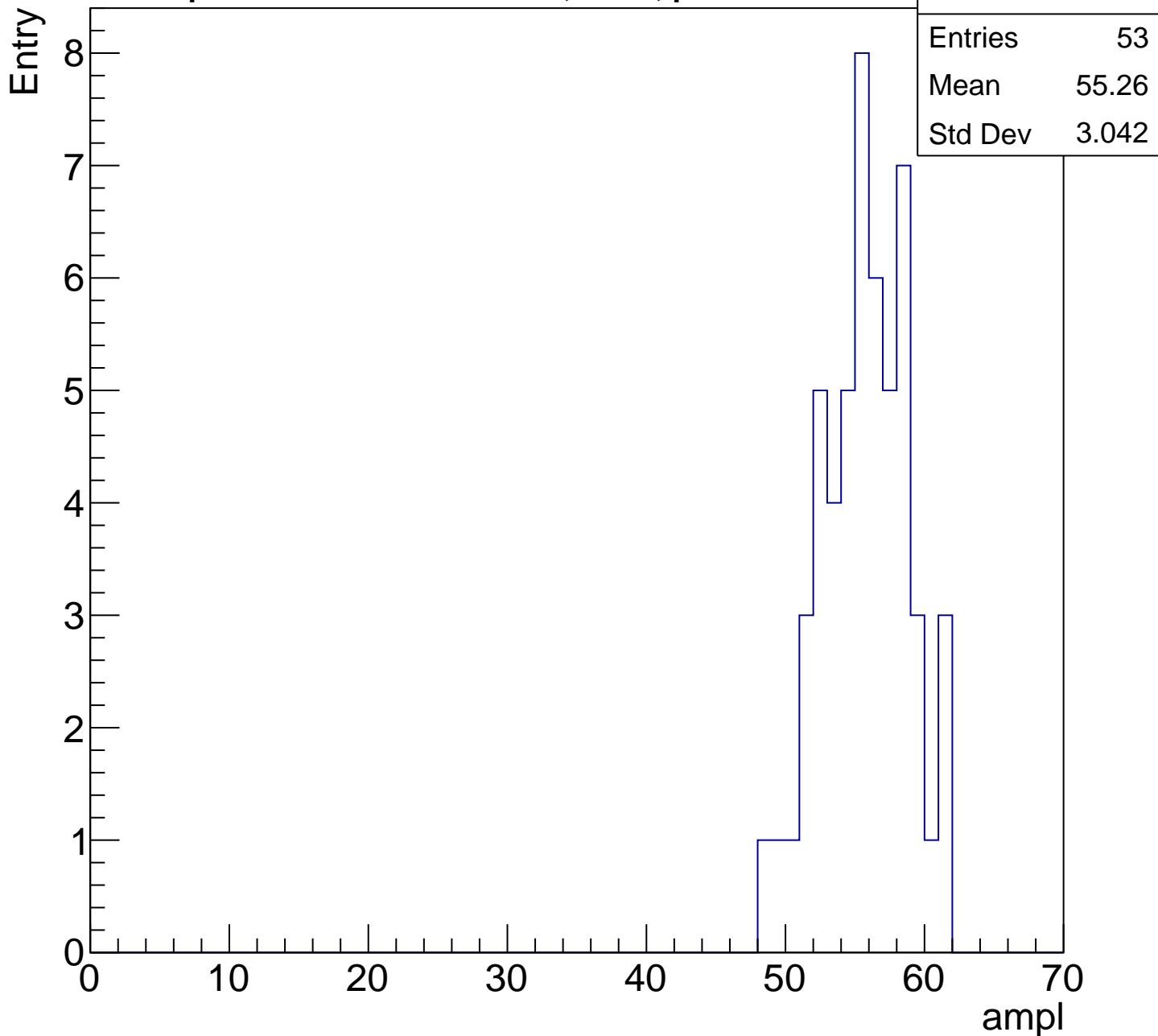
Entry

Entries	62
Mean	49.27
Std Dev	3.006



# B1L101S, U11-ch30, adc4

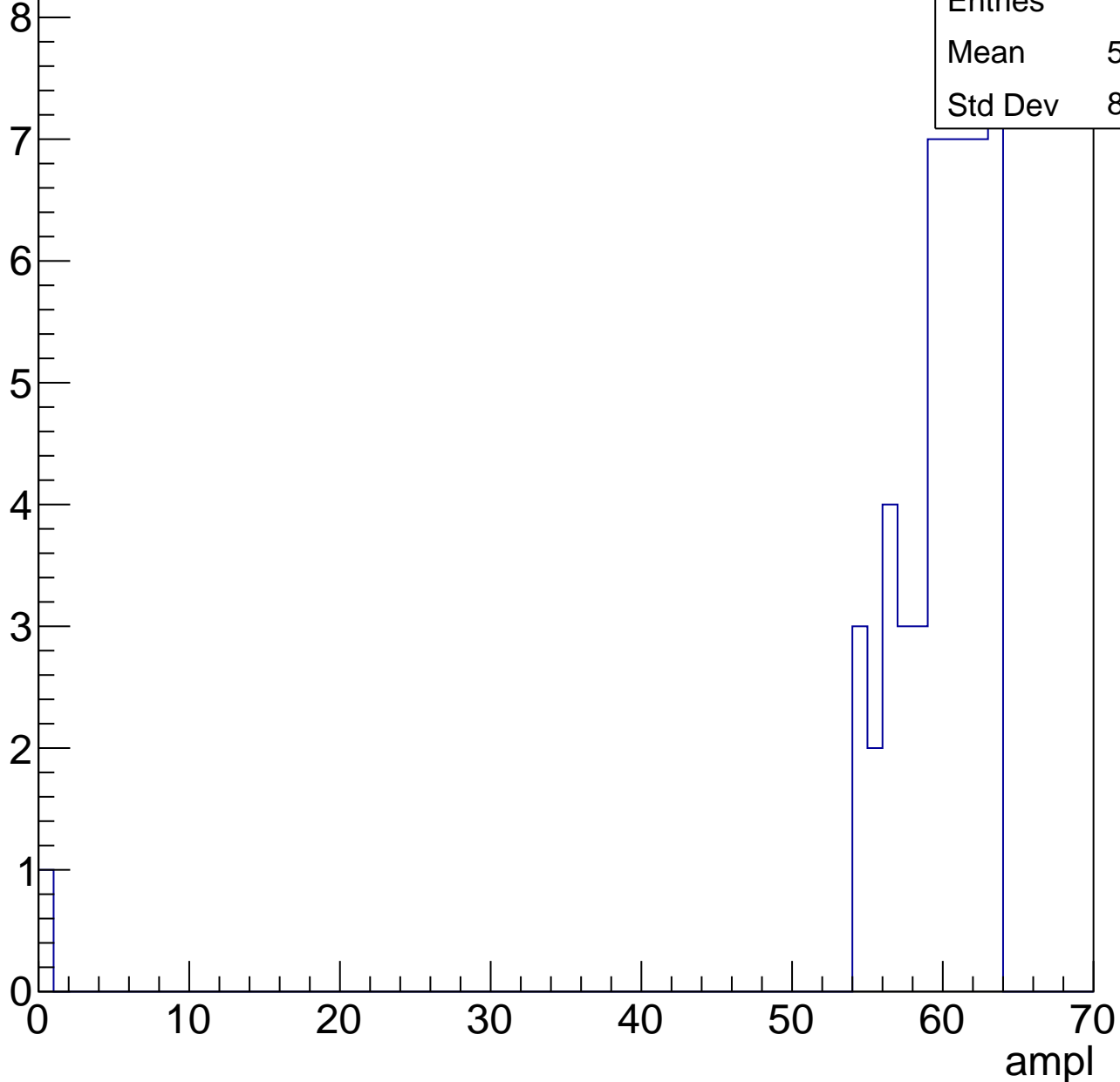
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U11-ch30, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

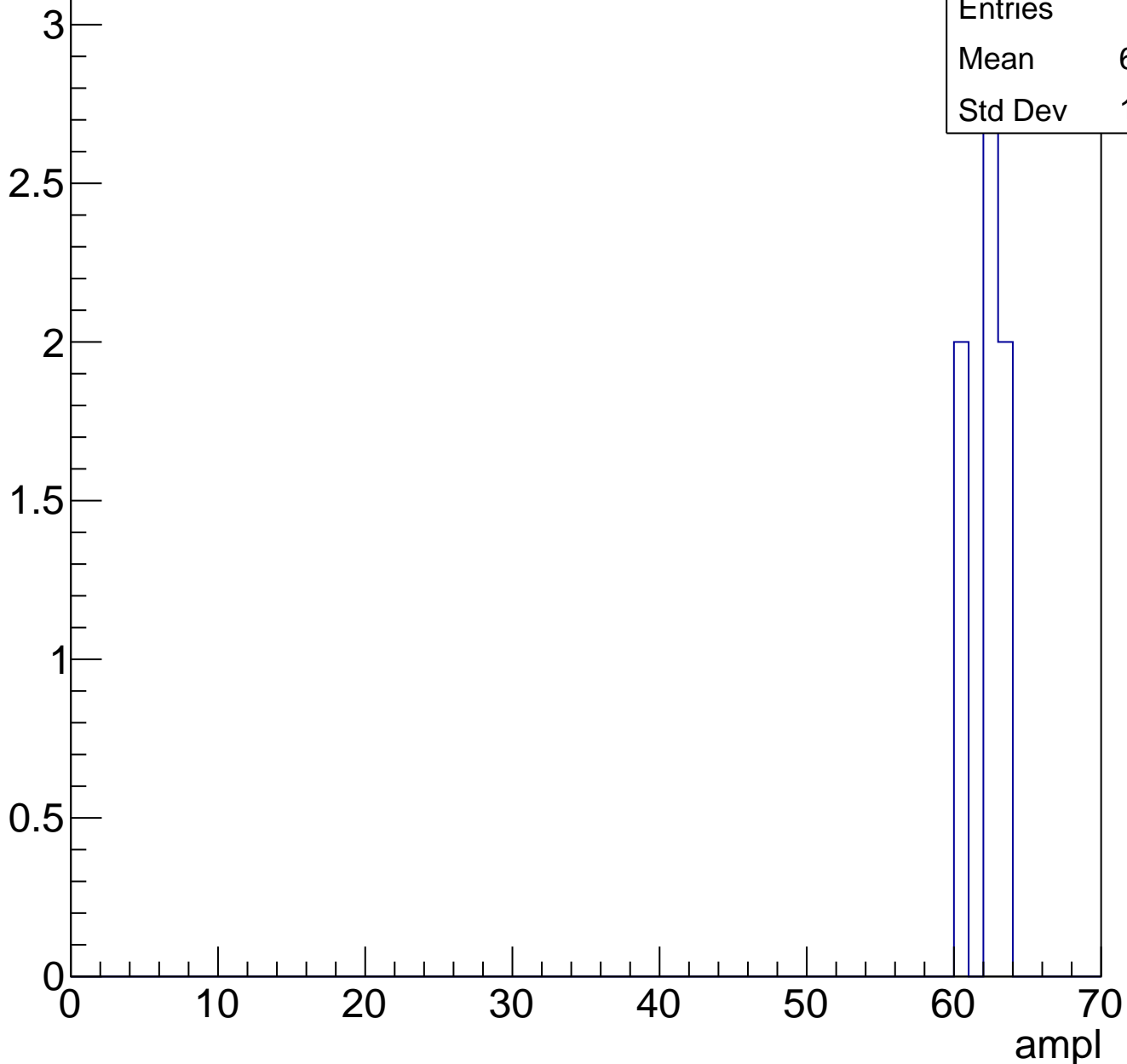
Entry



# B1L101S, U11-ch30, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch30, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U11-ch31, adc0

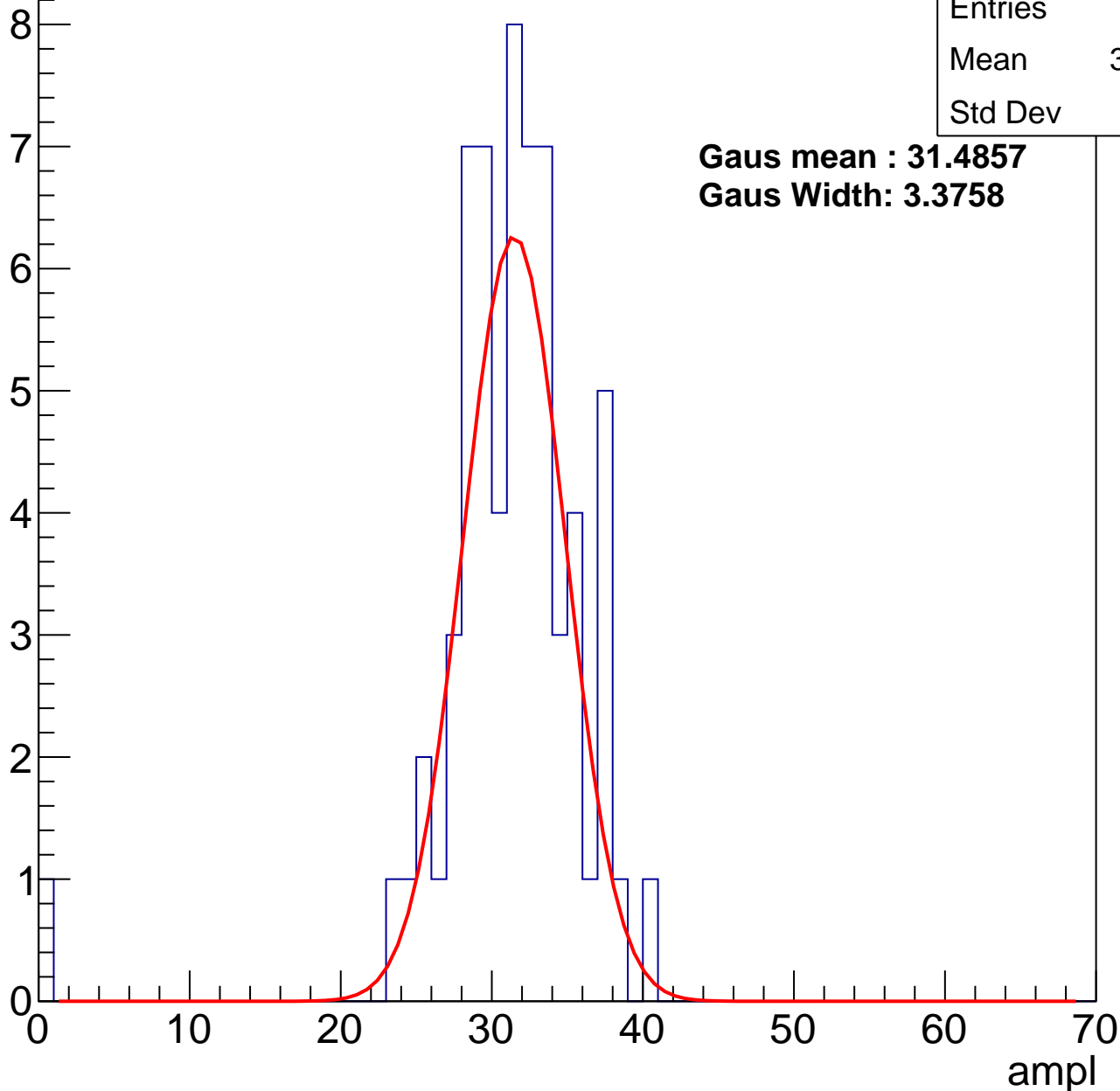
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	30.73
Std Dev	5.26

**Gaus mean : 31.4857**

**Gaus Width: 3.3758**



# B1L101S, U11-ch31, adc1

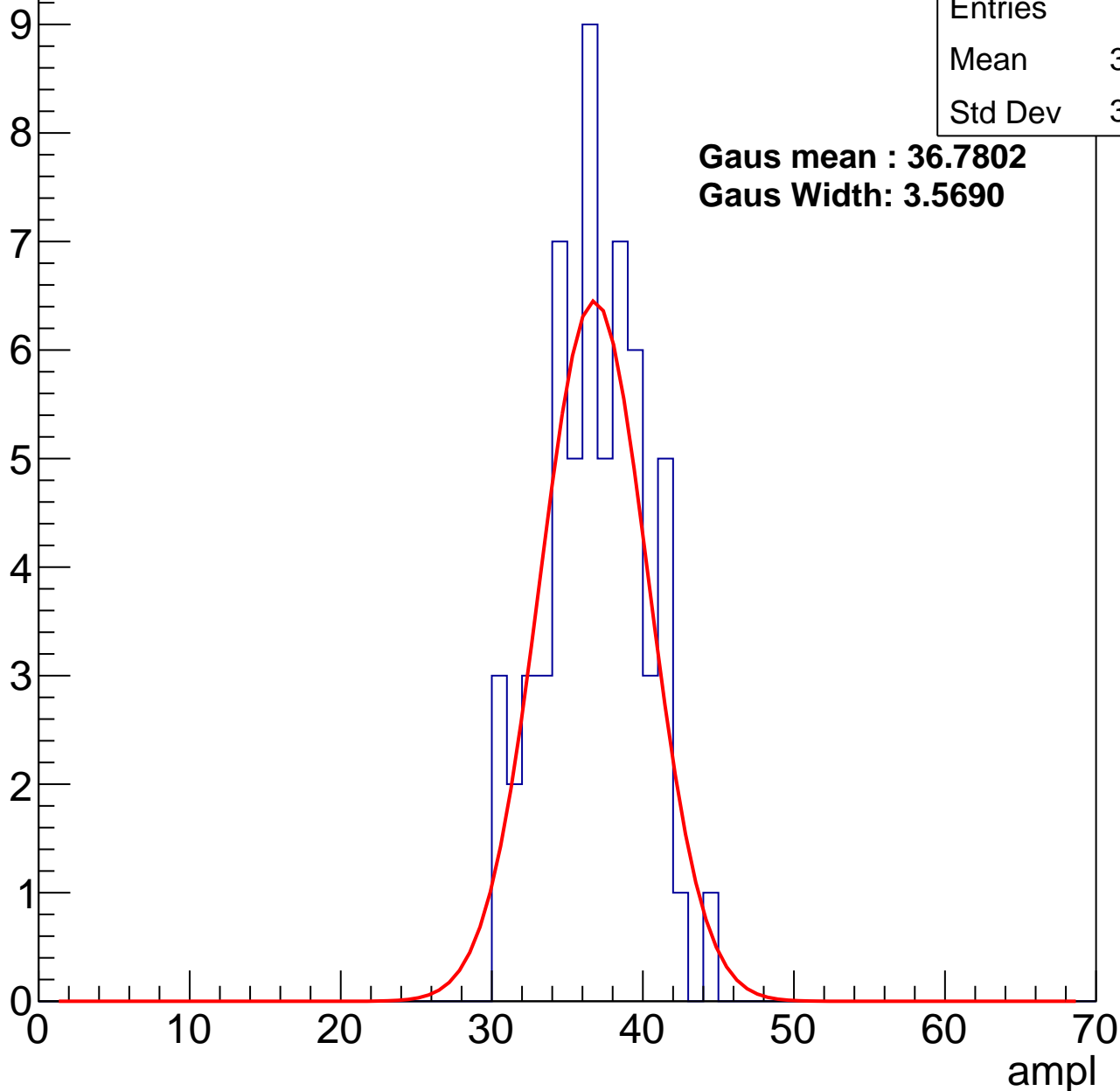
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	36.33
Std Dev	3.213

**Gaus mean : 36.7802**

**Gaus Width: 3.5690**



# B1L101S, U11-ch31, adc2

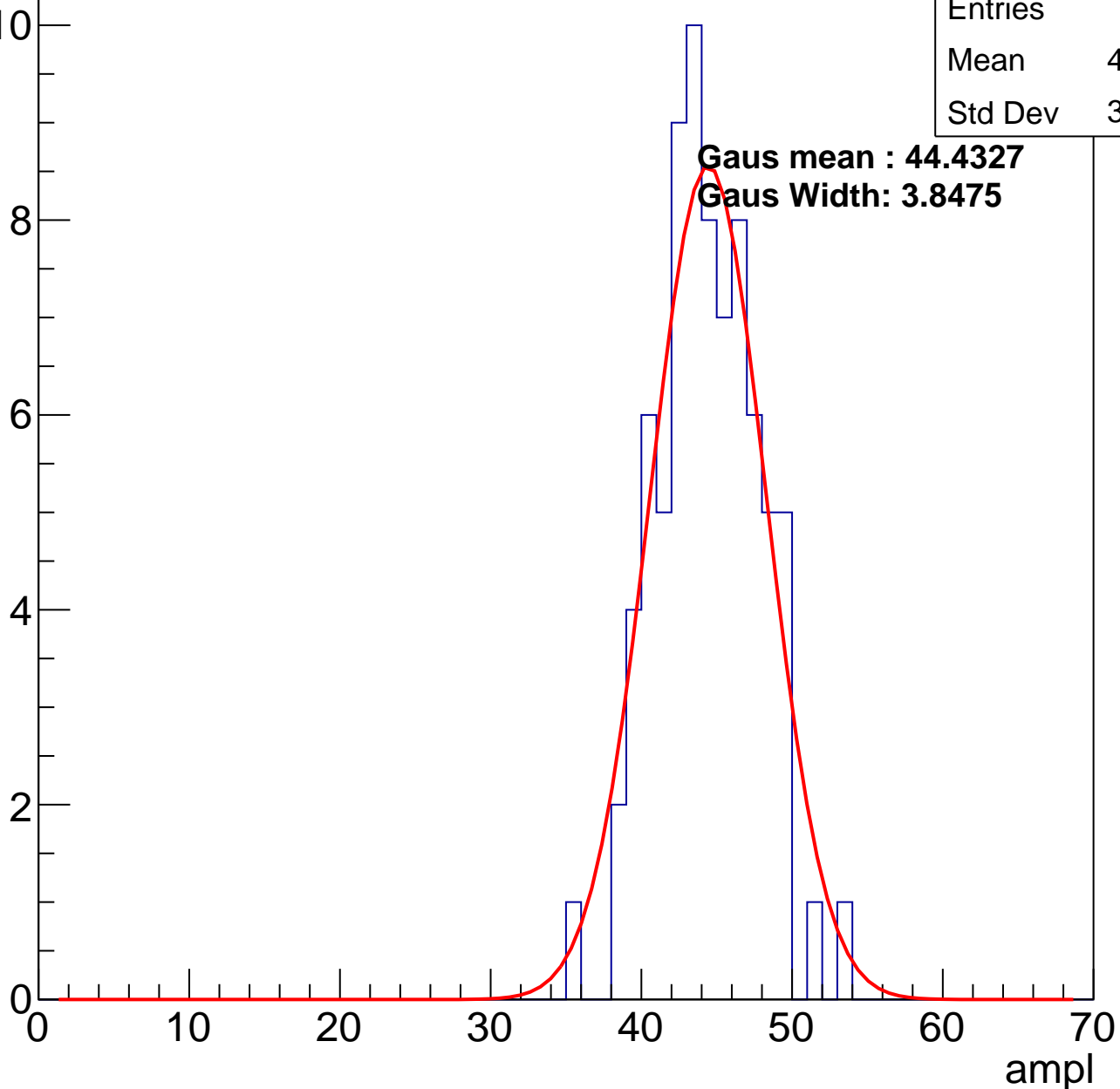
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	78
Mean	43.92
Std Dev	3.335

**Gaus mean : 44.4327**

**Gaus Width: 3.8475**

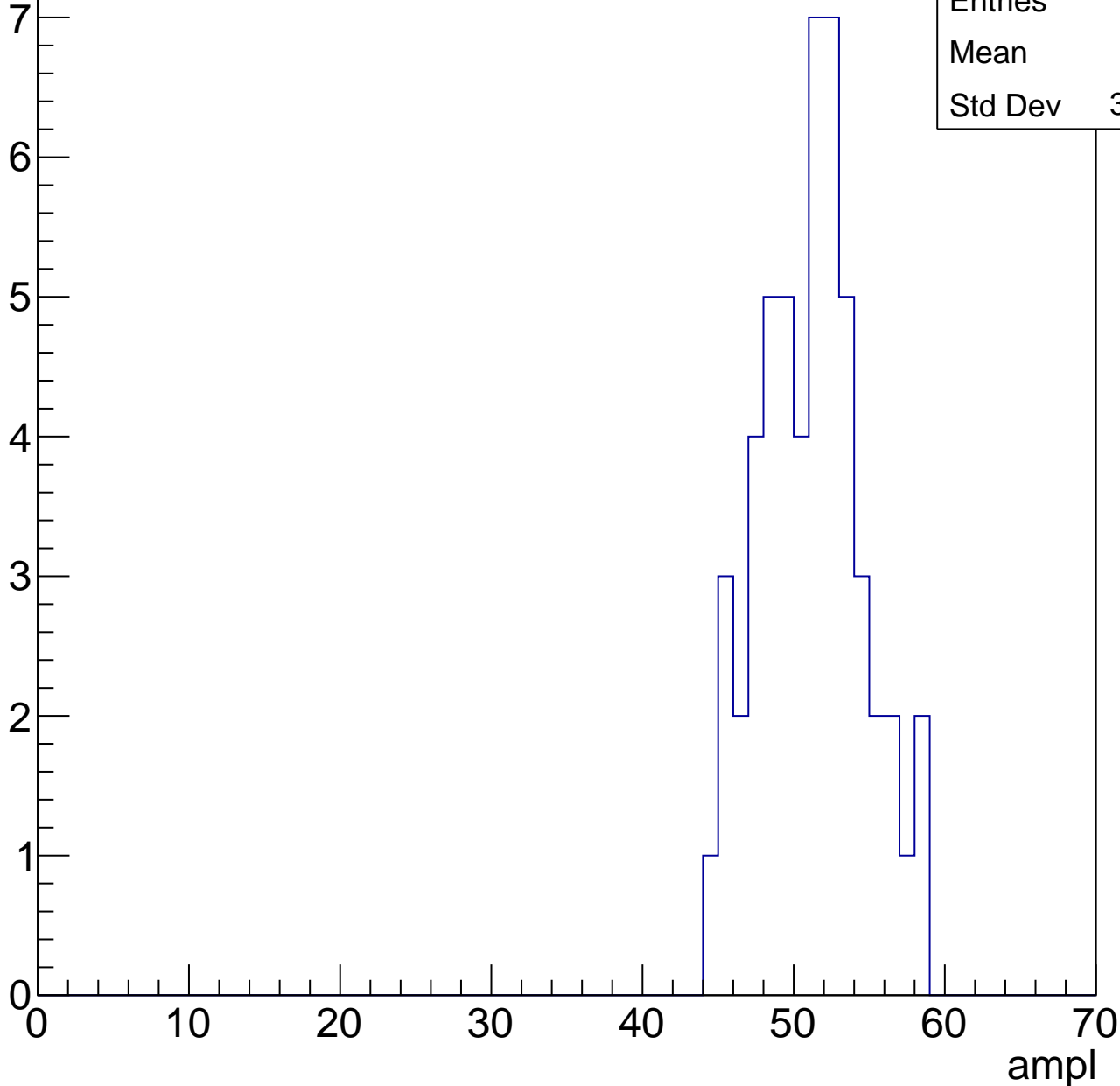


# B1L101S, U11-ch31, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	50.7
Std Dev	3.379

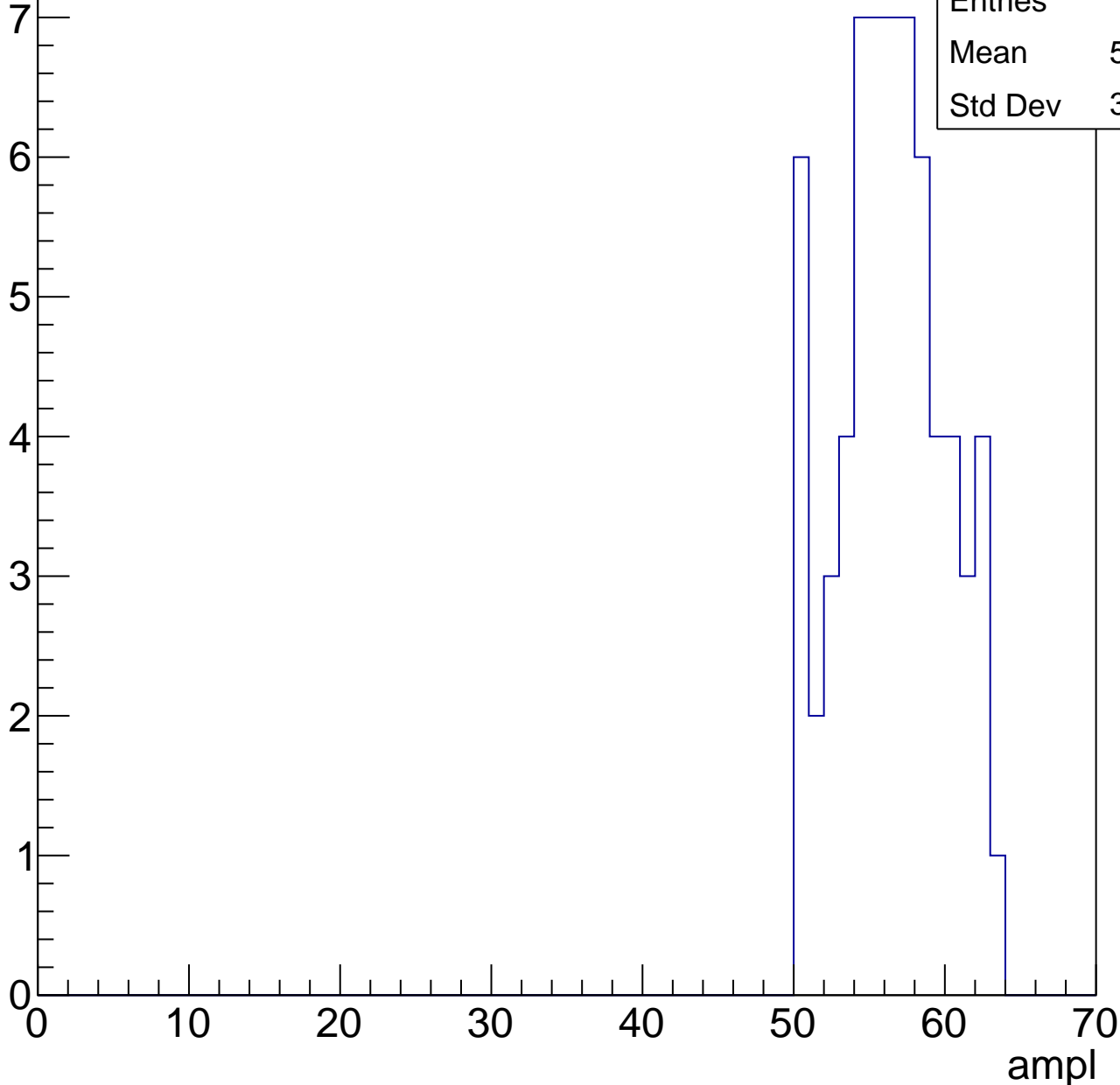


# B1L101S, U11-ch31, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

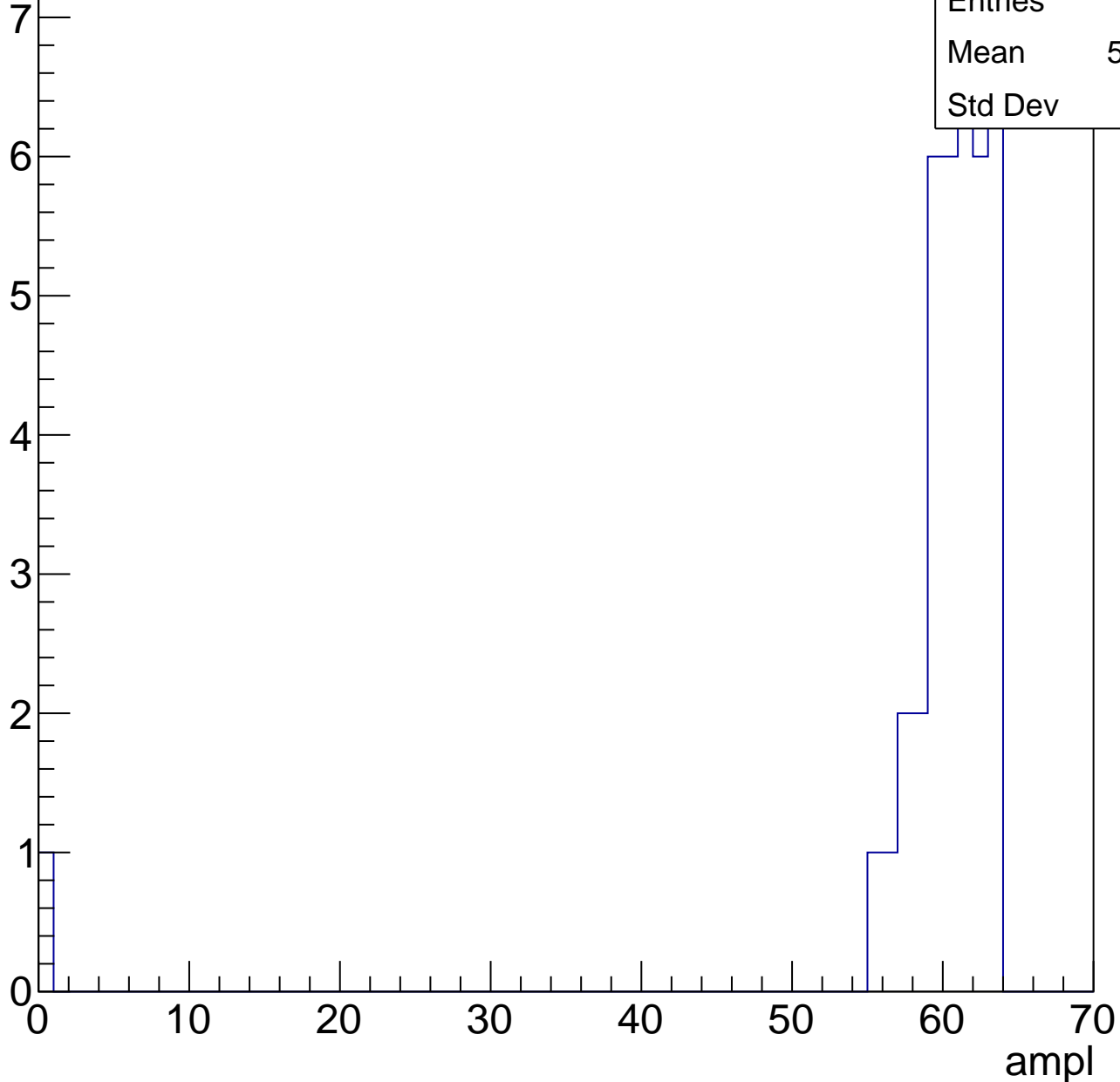
Entries	65
Mean	56.03
Std Dev	3.473



# B1L101S, U11-ch31, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U11-ch31, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch31, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U11-ch32, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	80
Mean	29.96
Std Dev	3.393

**Gaus mean : 30.4819**

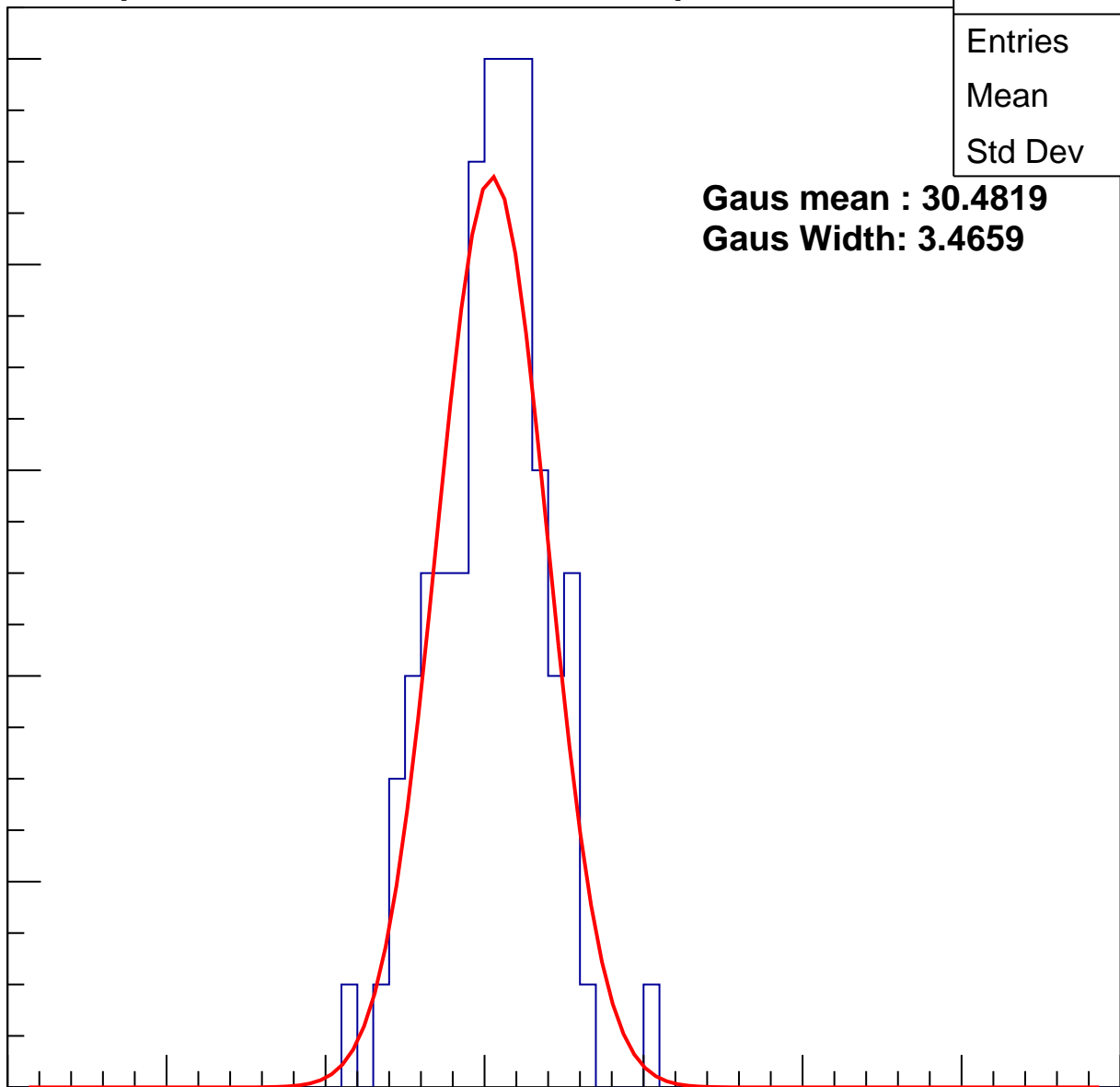
**Gaus Width: 3.4659**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



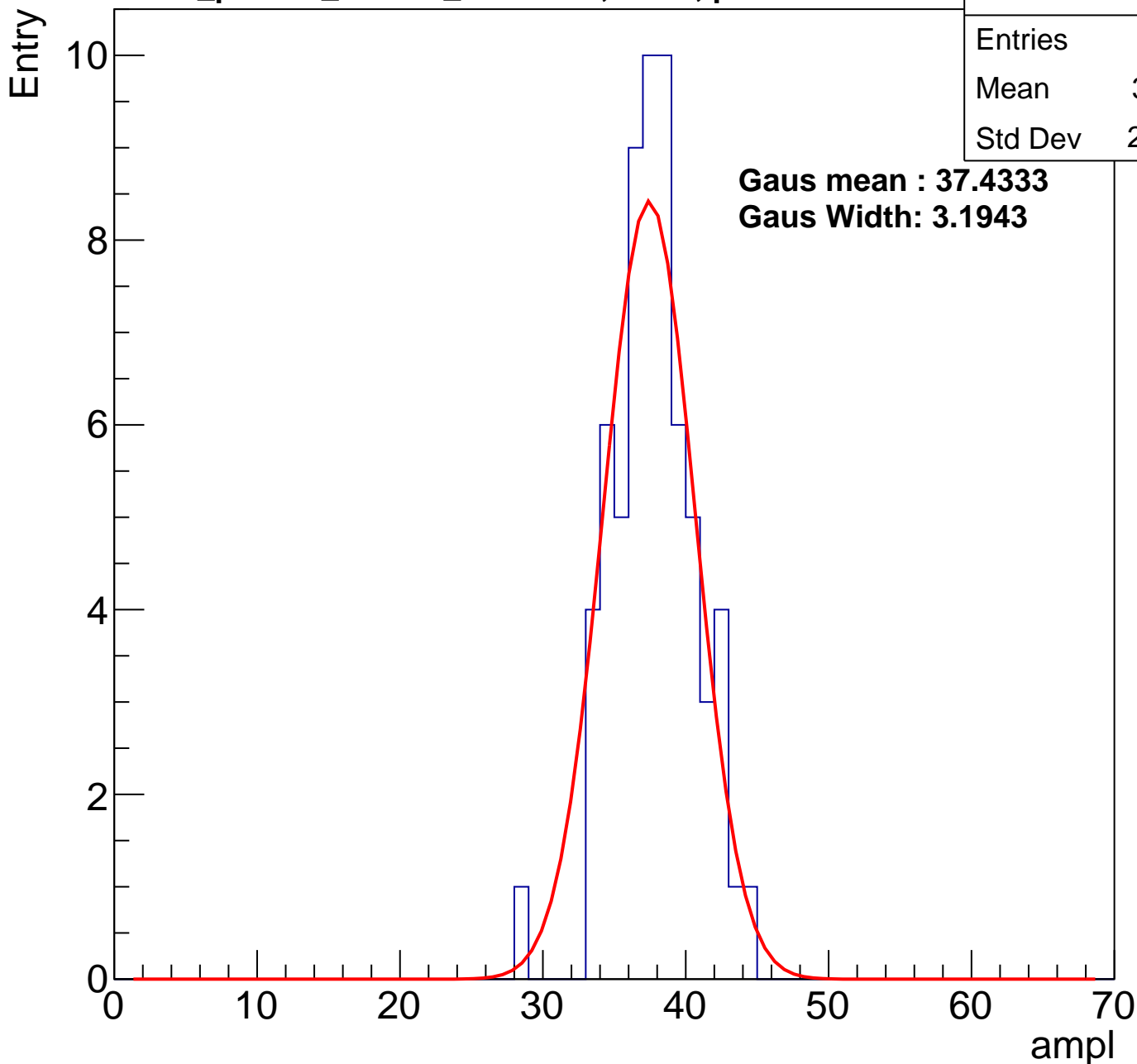
# B1L101S, U11-ch32, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	65
Mean	37.31
Std Dev	2.866

**Gaus mean : 37.4333**

**Gaus Width: 3.1943**



# B1L101S, U11-ch32, adc2

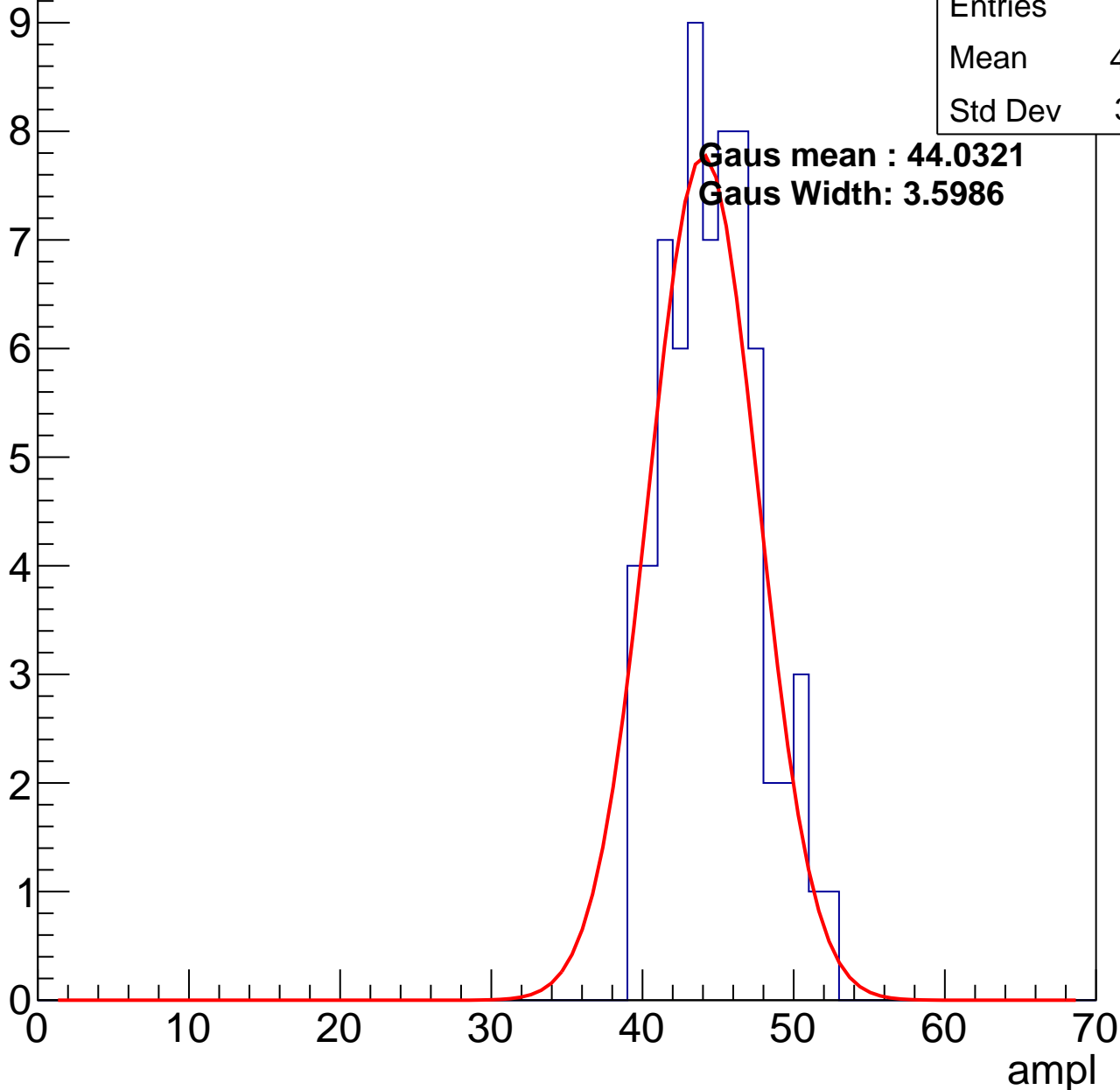
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	44.22
Std Dev	3.101

**Gaus mean : 44.0321**

**Gaus Width: 3.5986**

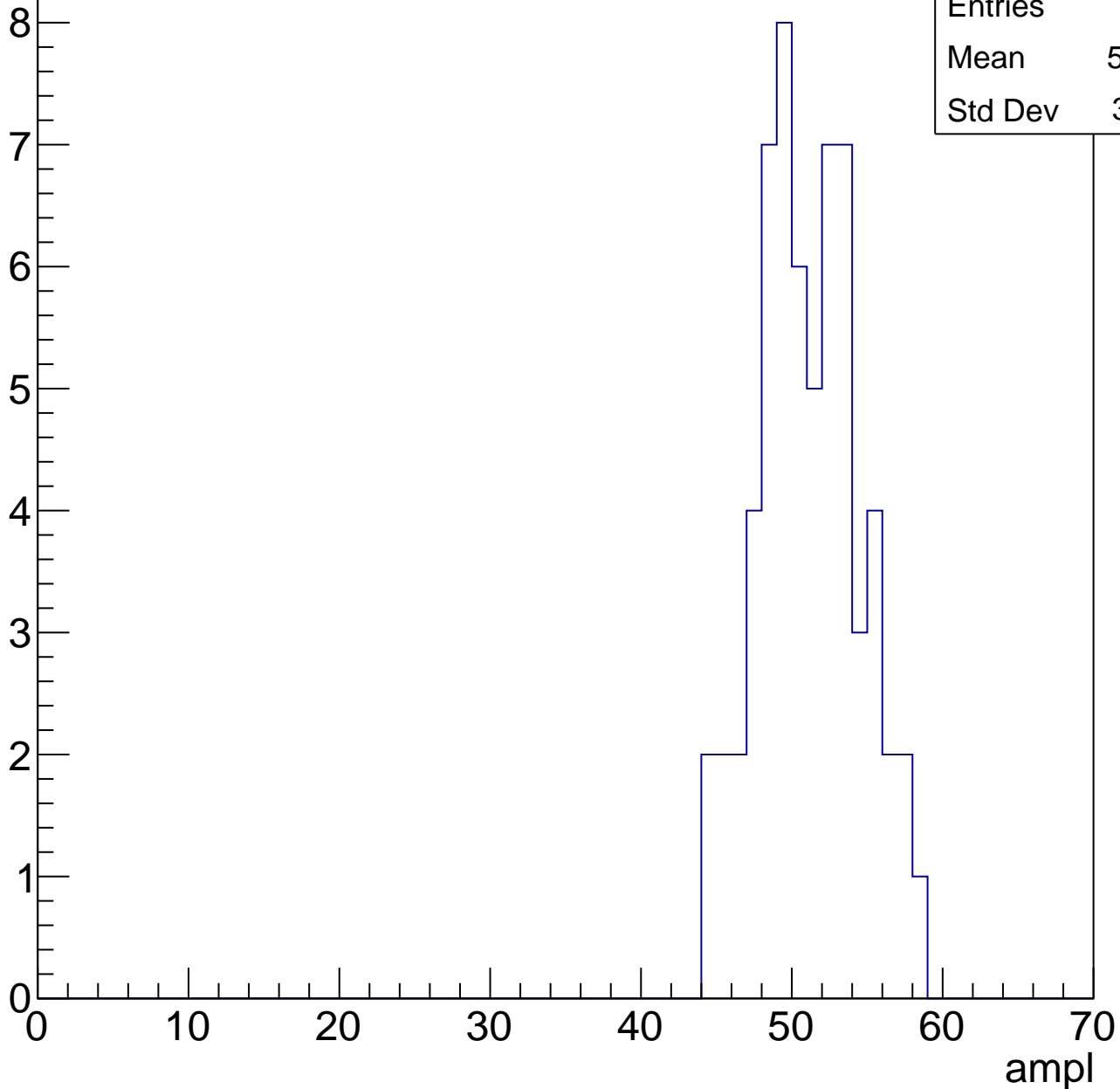


# B1L101S, U11-ch32, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	50.68
Std Dev	3.301

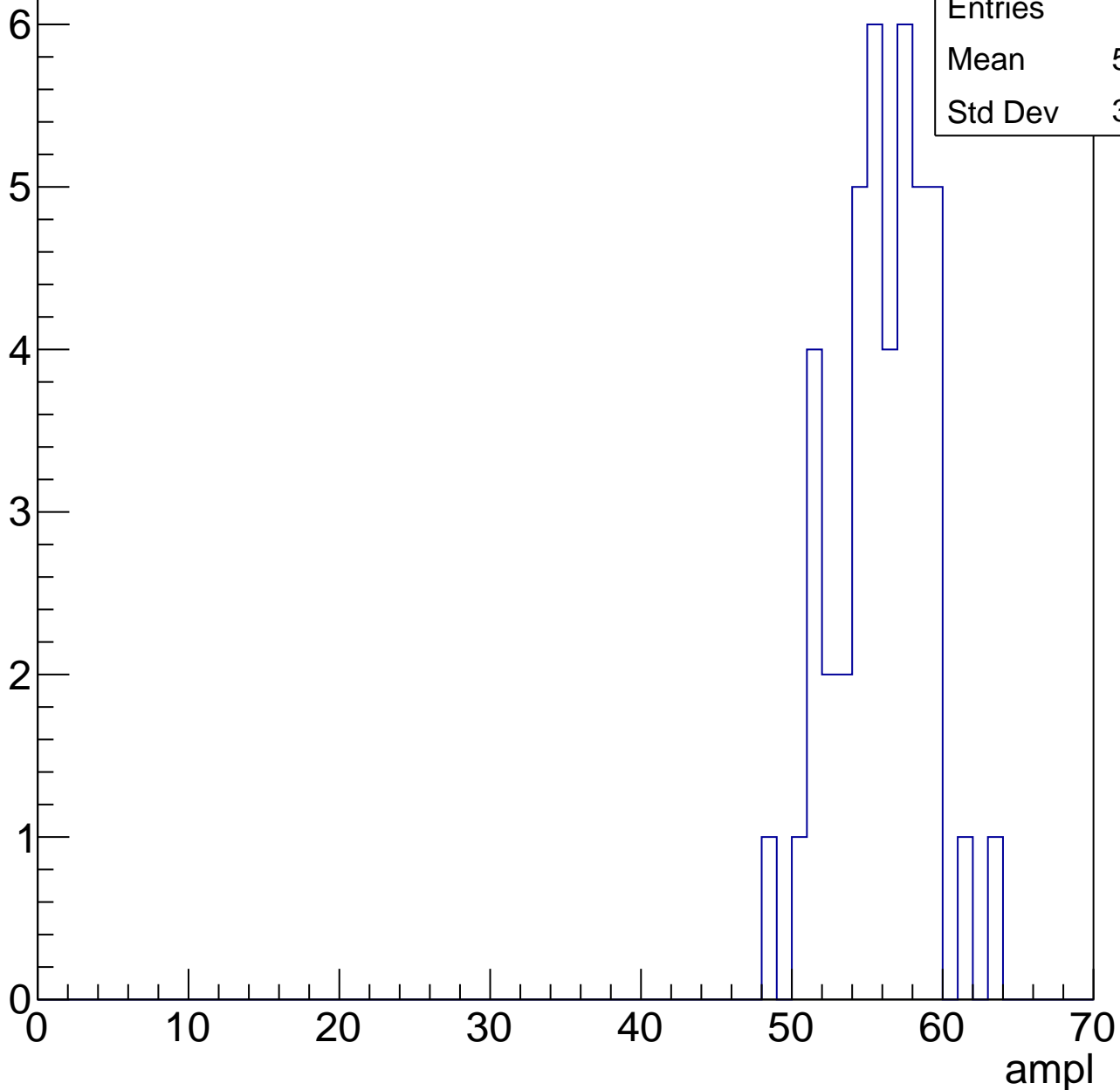


# B1L101S, U11-ch32, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

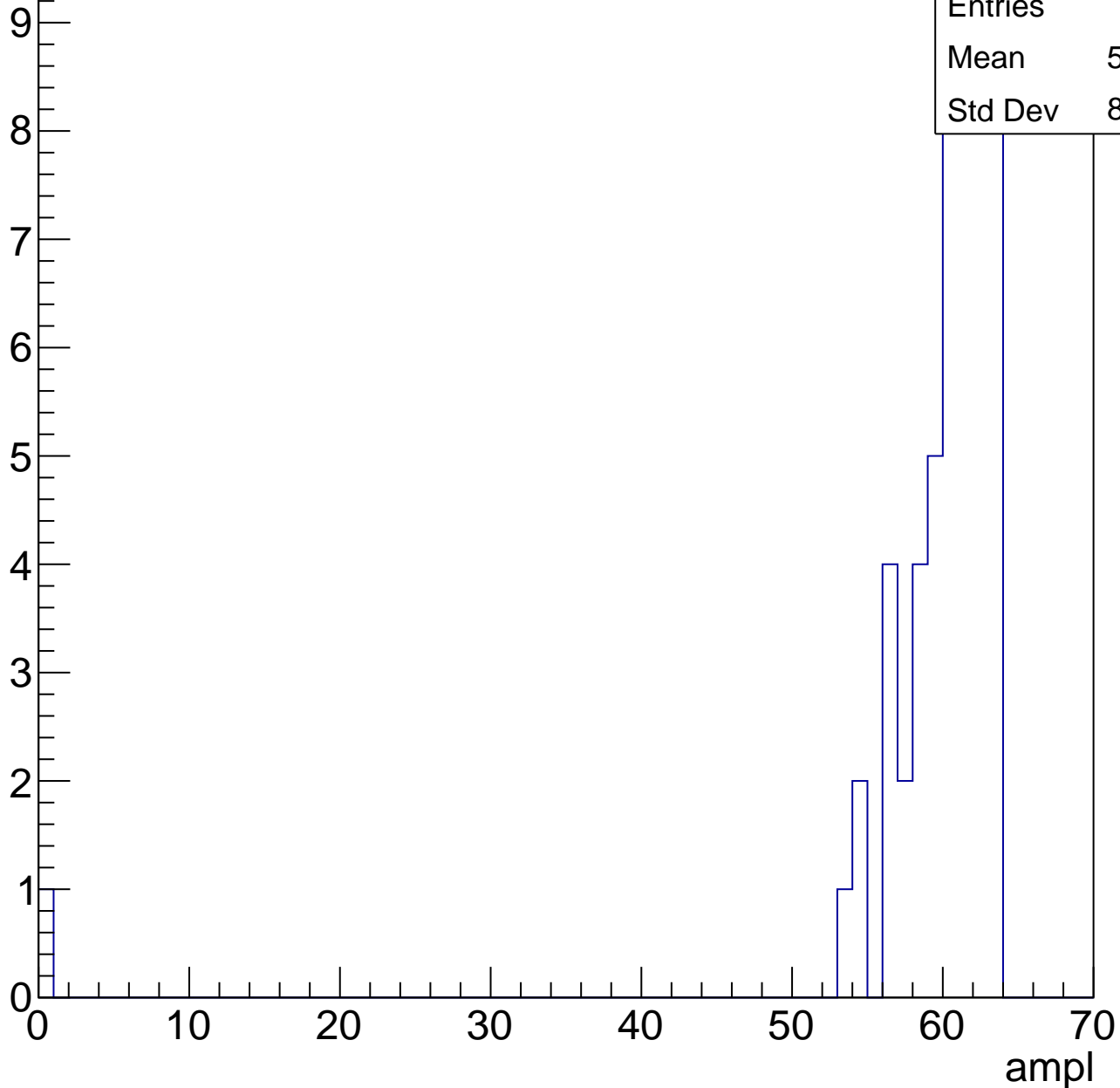
Entries	43
Mean	55.51
Std Dev	3.091



# B1L101S, U11-ch32, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U11-ch32, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch32, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U11-ch33, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	90
Mean	29.44
Std Dev	4.636

**Gaus mean : 30.3498**

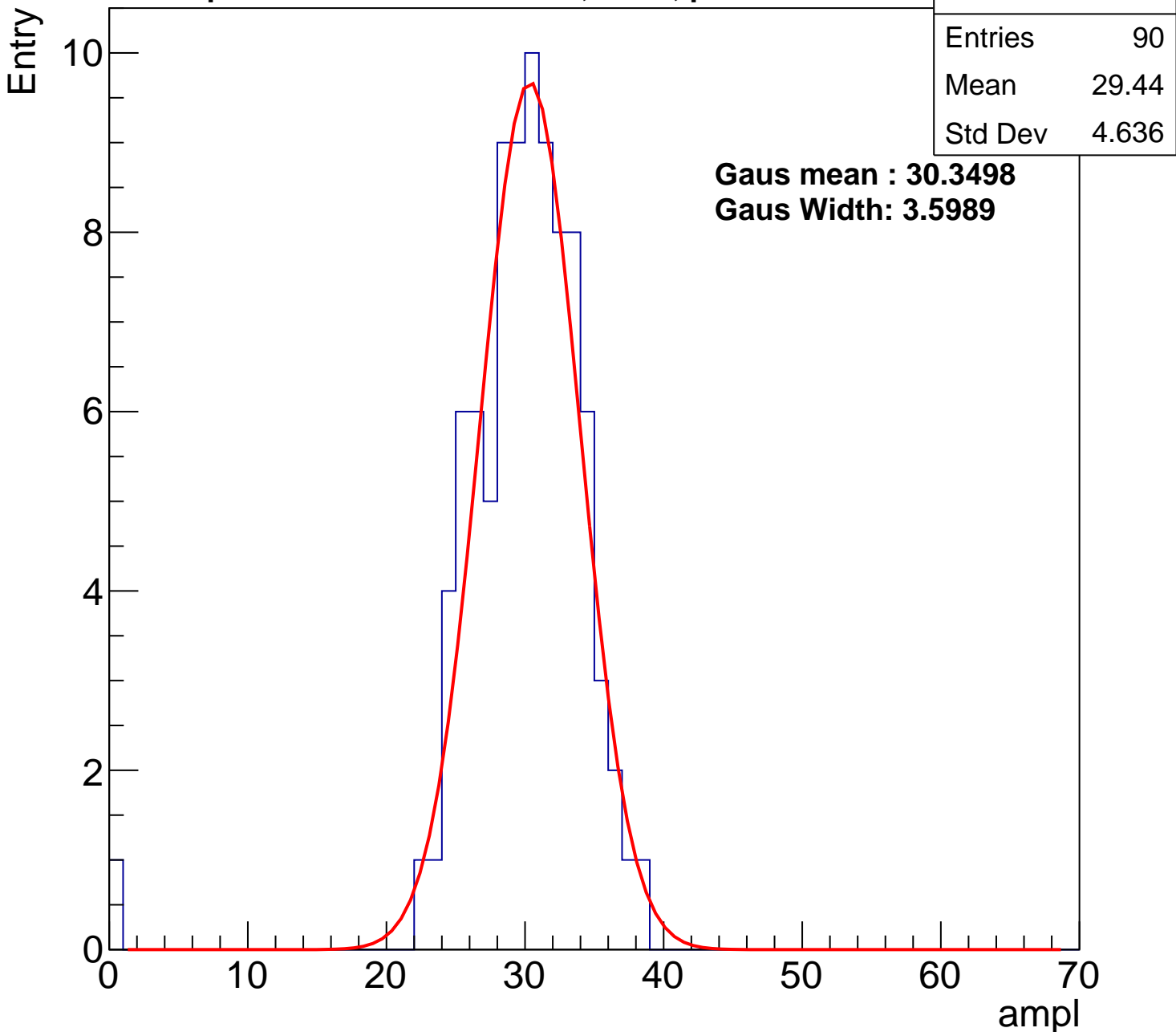
**Gaus Width: 3.5989**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U11-ch33, adc1

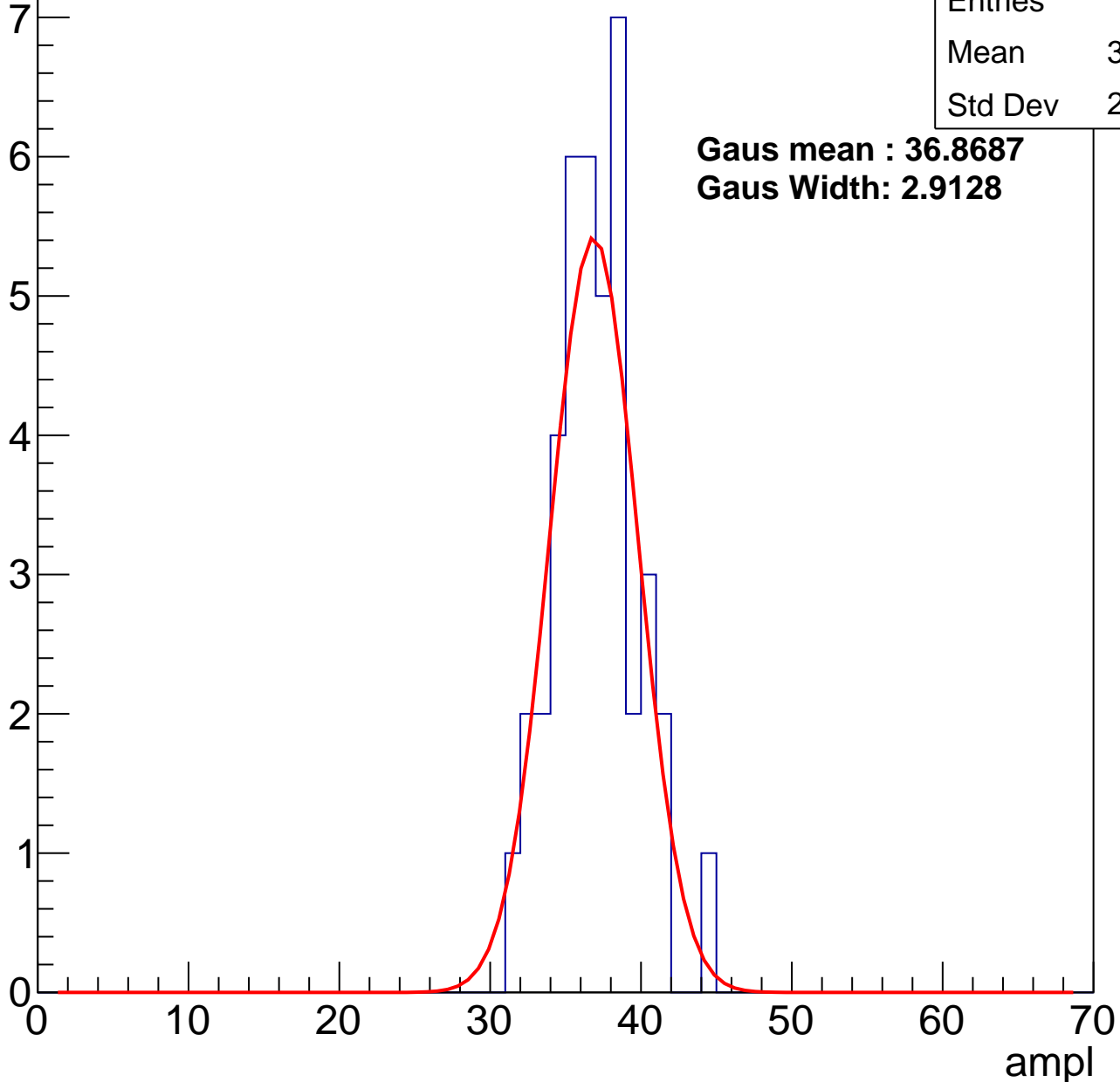
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	41
Mean	36.54
Std Dev	2.697

**Gaus mean : 36.8687**

**Gaus Width: 2.9128**



# B1L101S, U11-ch33, adc2

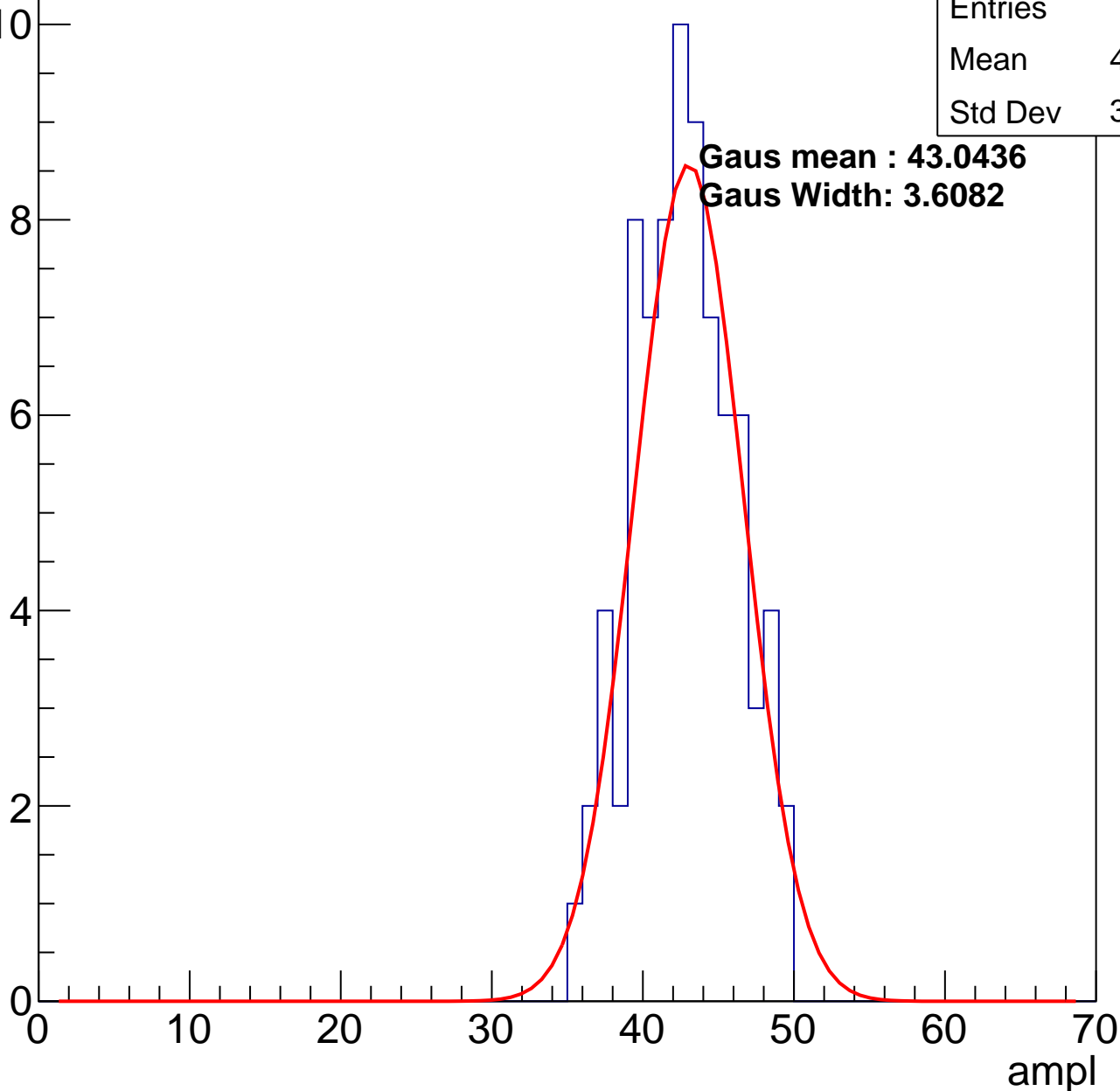
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	79
Mean	42.32
Std Dev	3.294

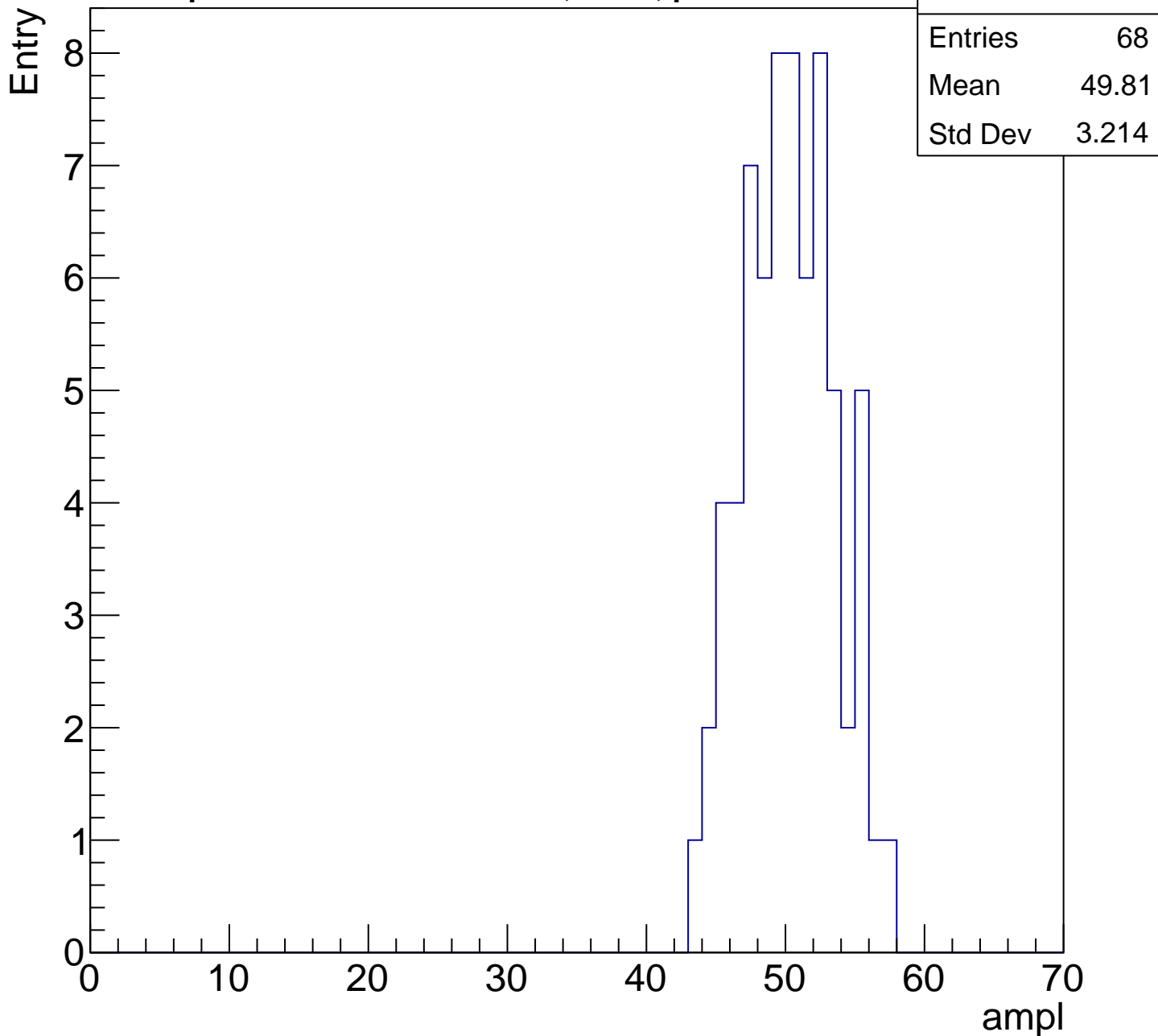
**Gaus mean : 43.0436**

**Gaus Width: 3.6082**



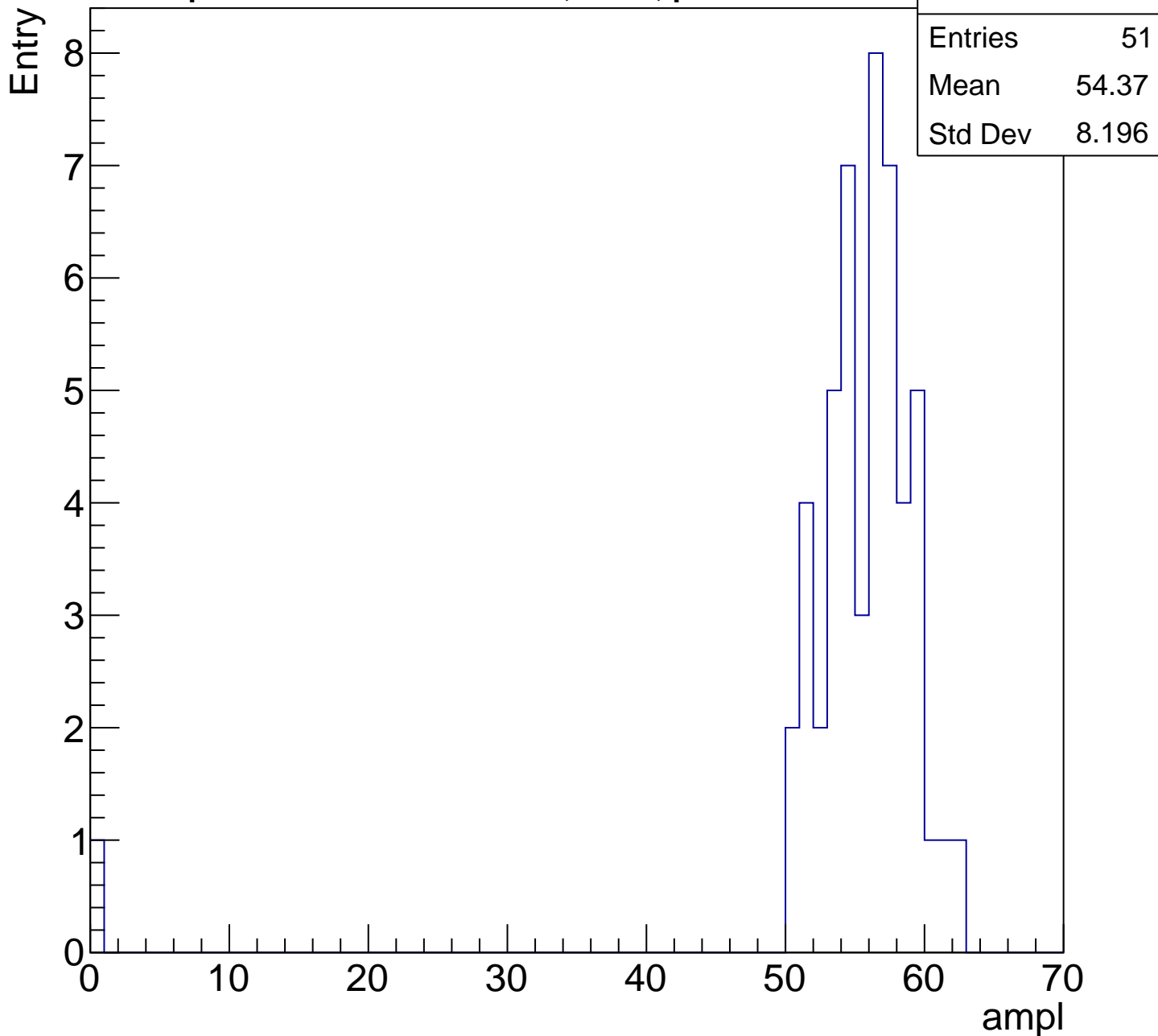
# B1L101S, U11-ch33, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U11-ch33, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

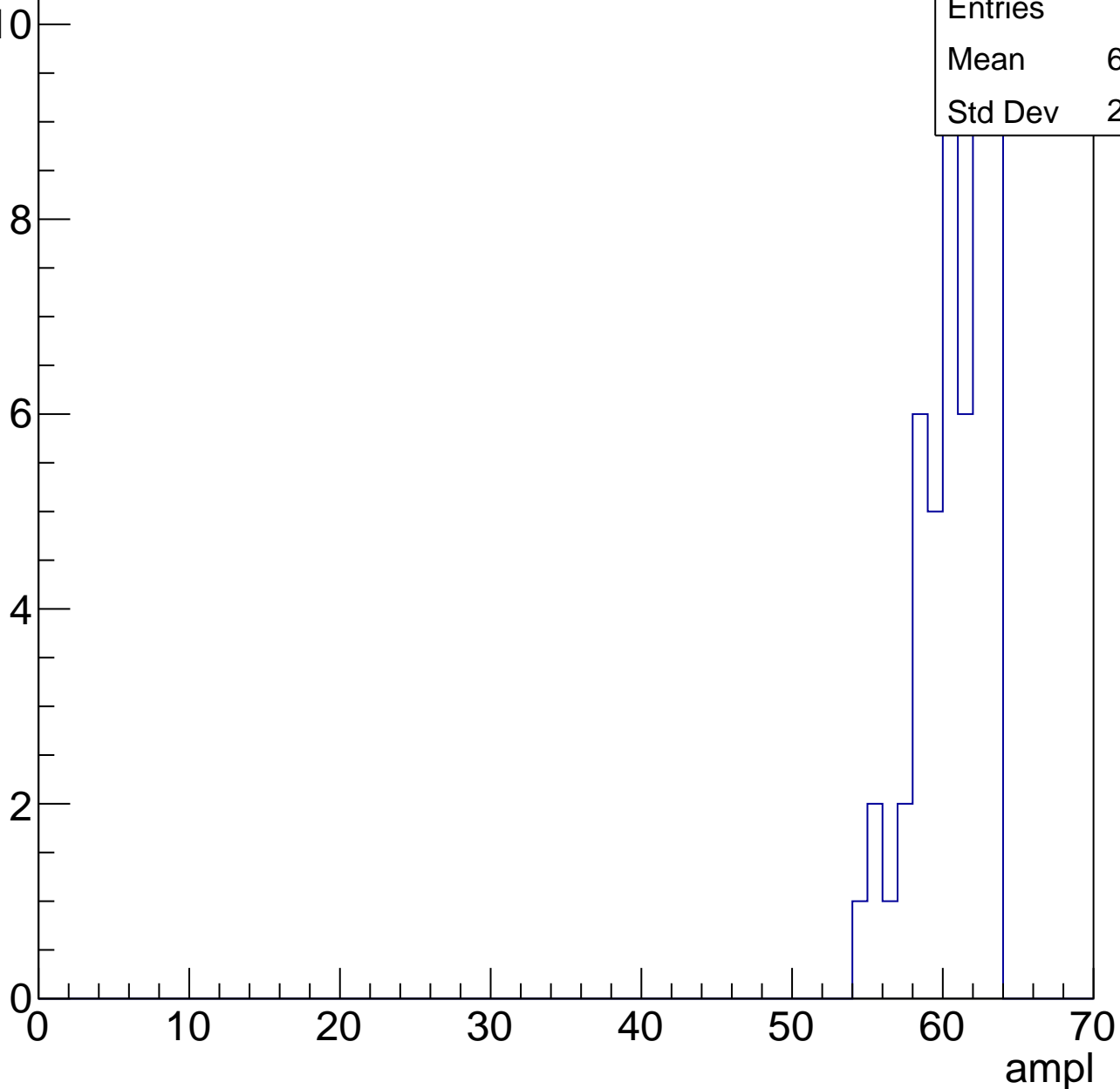


# B1L101S, U11-ch33, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

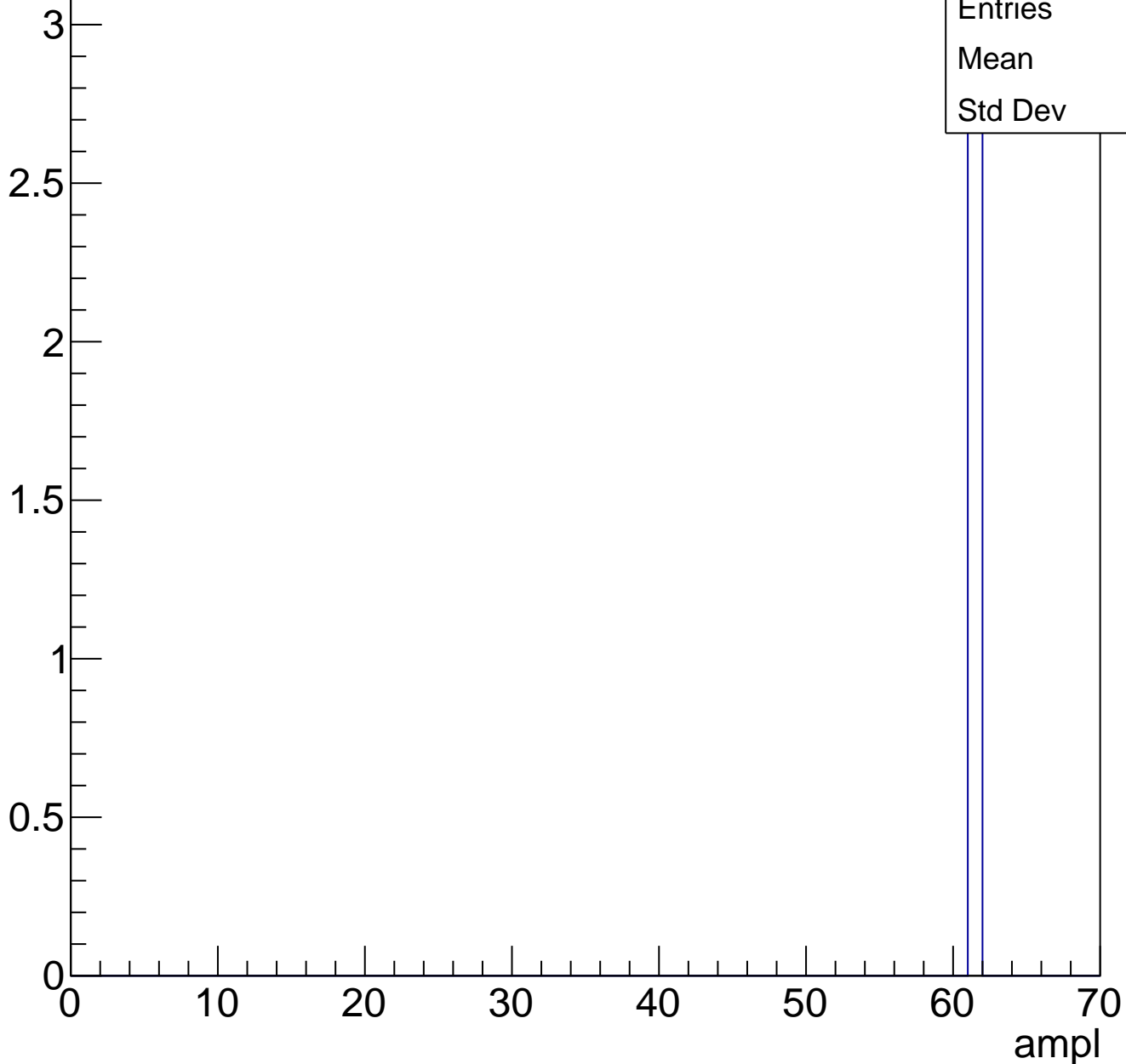
Entries	51
Mean	60.22
Std Dev	2.337



# B1L101S, U11-ch33, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch33, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U11-ch34, adc0

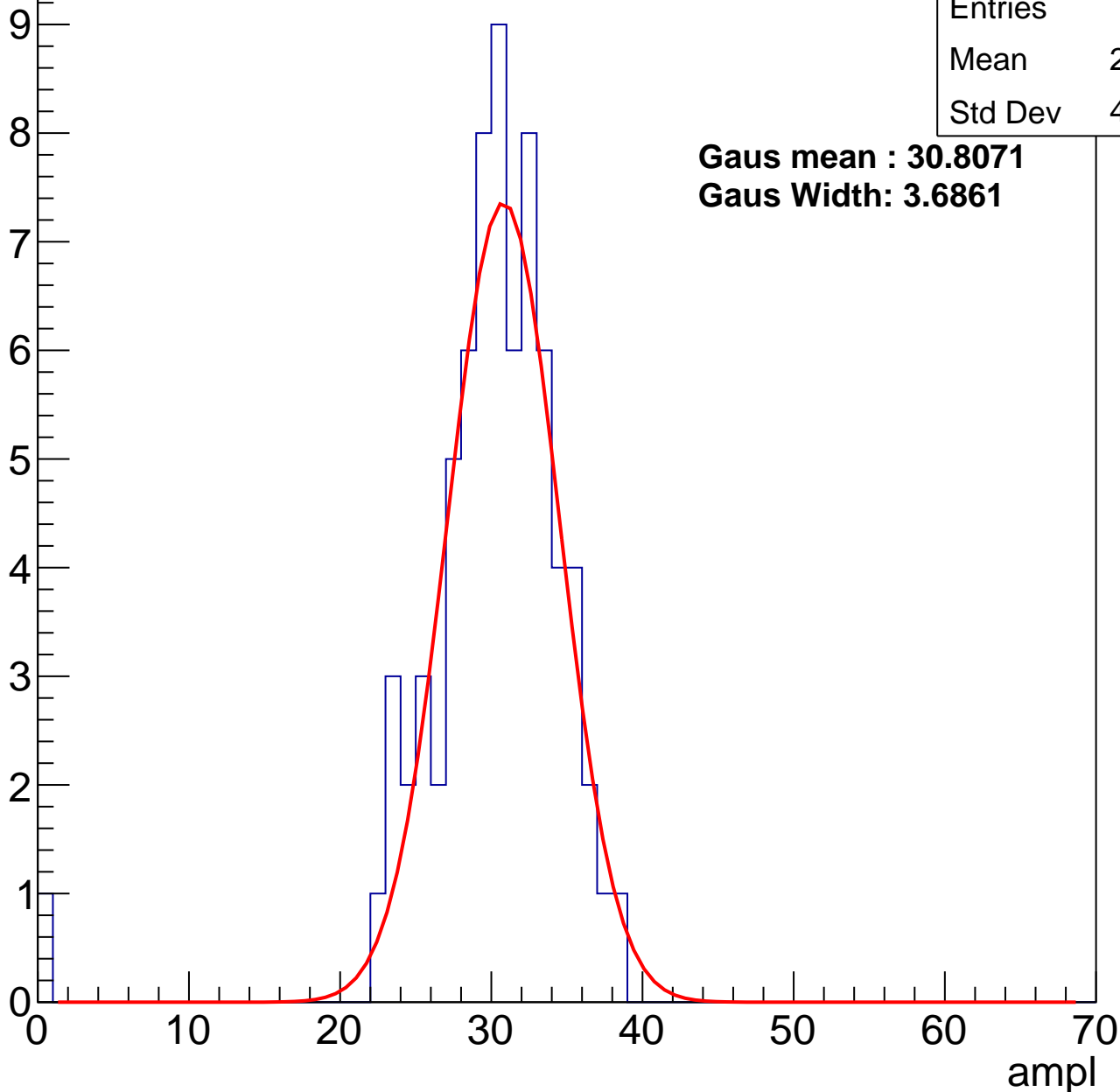
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	29.64
Std Dev	4.998

**Gaus mean : 30.8071**

**Gaus Width: 3.6861**



# B1L101S, U11-ch34, adc1

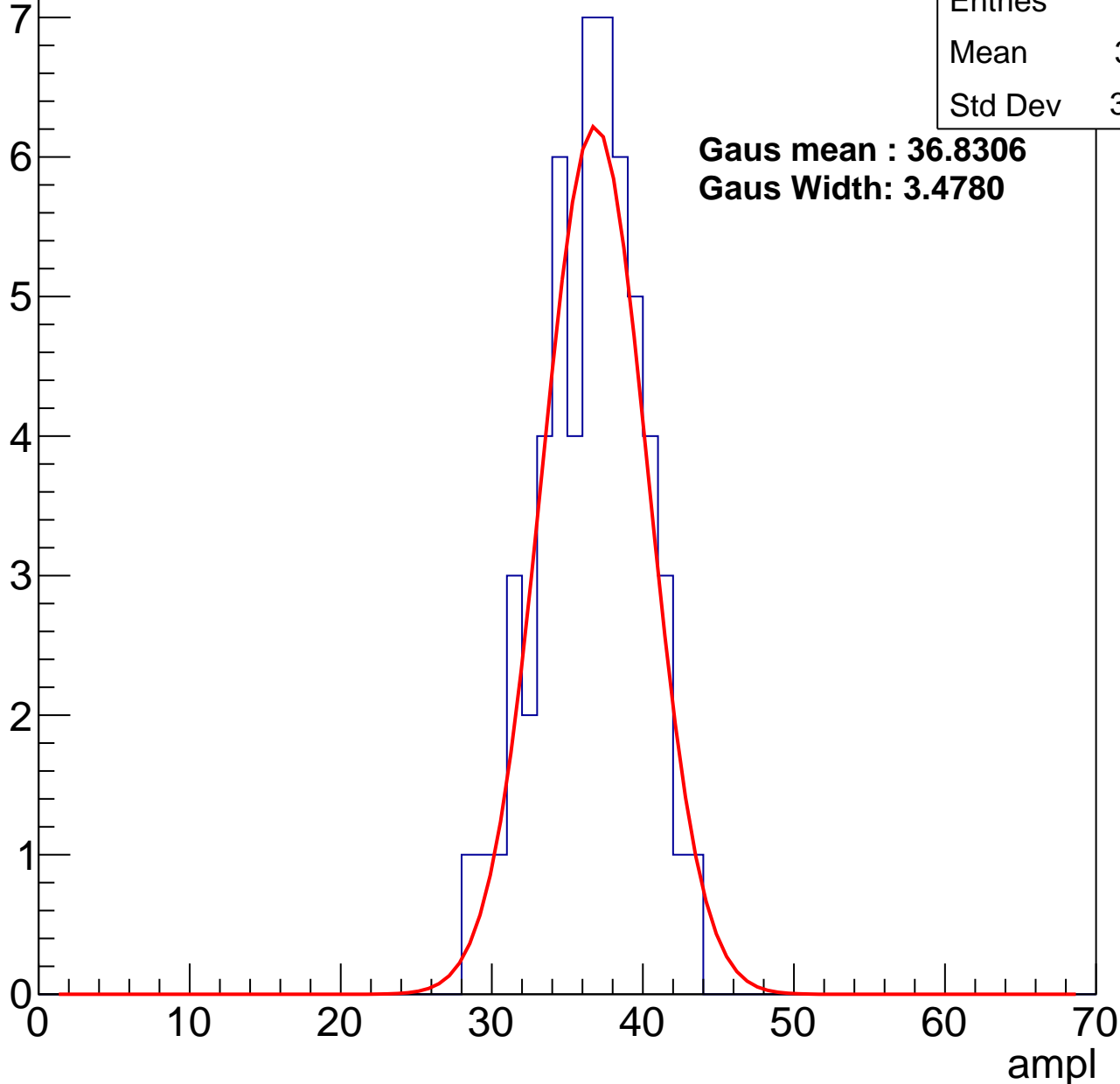
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	36.11
Std Dev	3.326

**Gaus mean : 36.8306**

**Gaus Width: 3.4780**



# B1L101S, U11-ch34, adc2

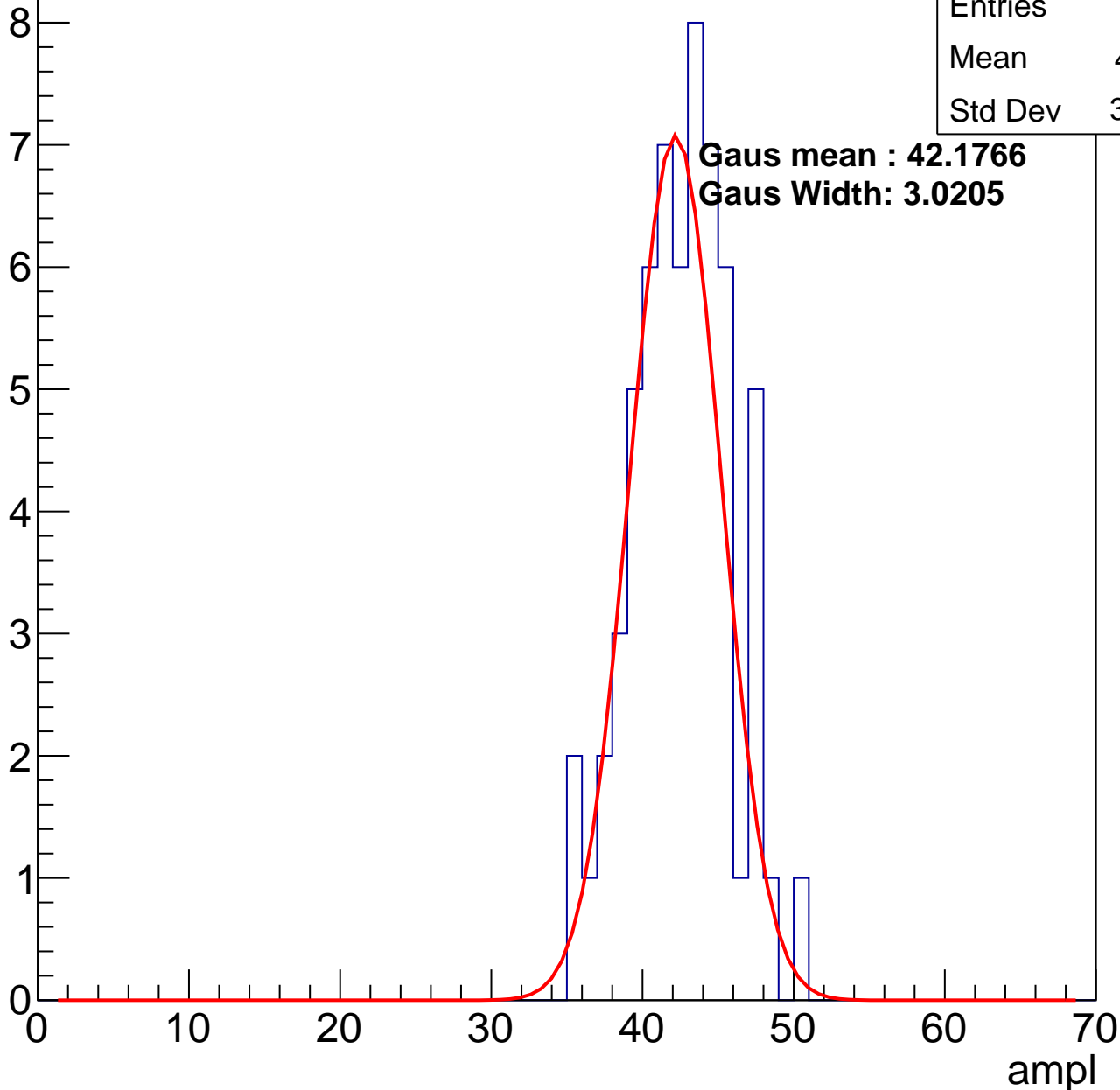
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	42.11
Std Dev	3.235

**Gaus mean : 42.1766**

**Gaus Width: 3.0205**



# B1L101S, U11-ch34, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	88
Mean	49.77
Std Dev	3.692

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

ampl

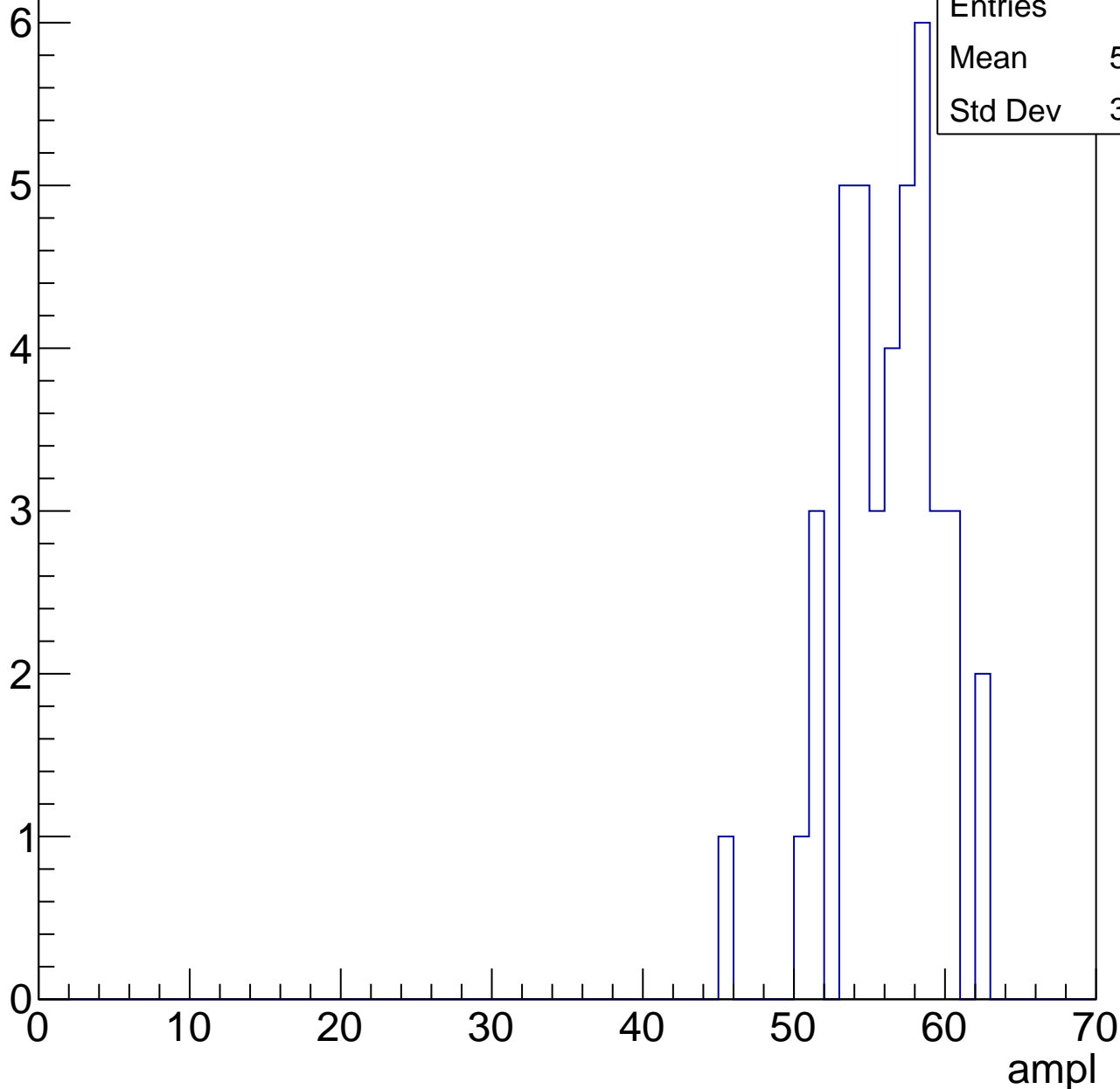
70

# B1L101S, U11-ch34, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	41
Mean	55.76
Std Dev	3.399

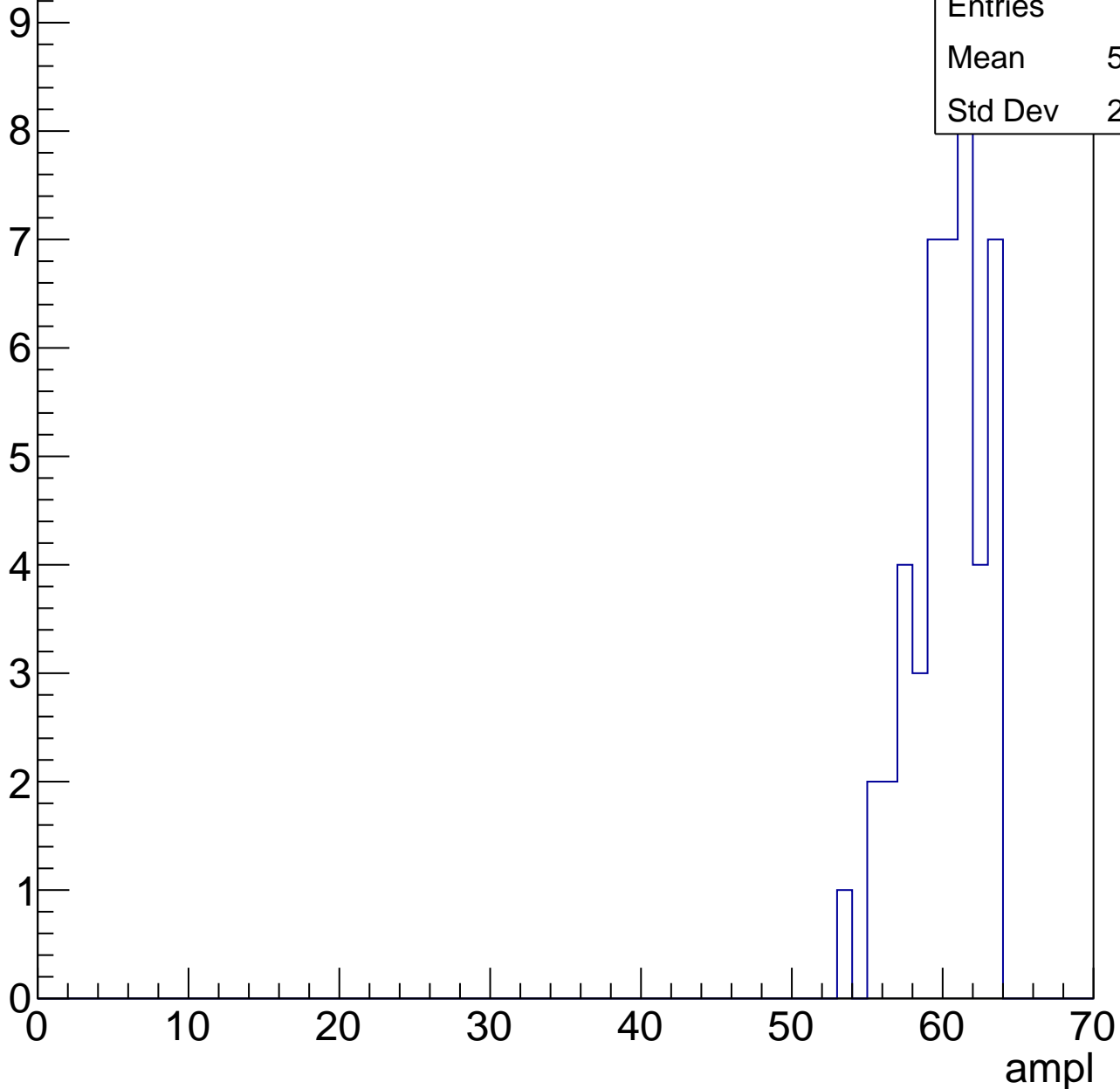


# B1L101S, U11-ch34, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

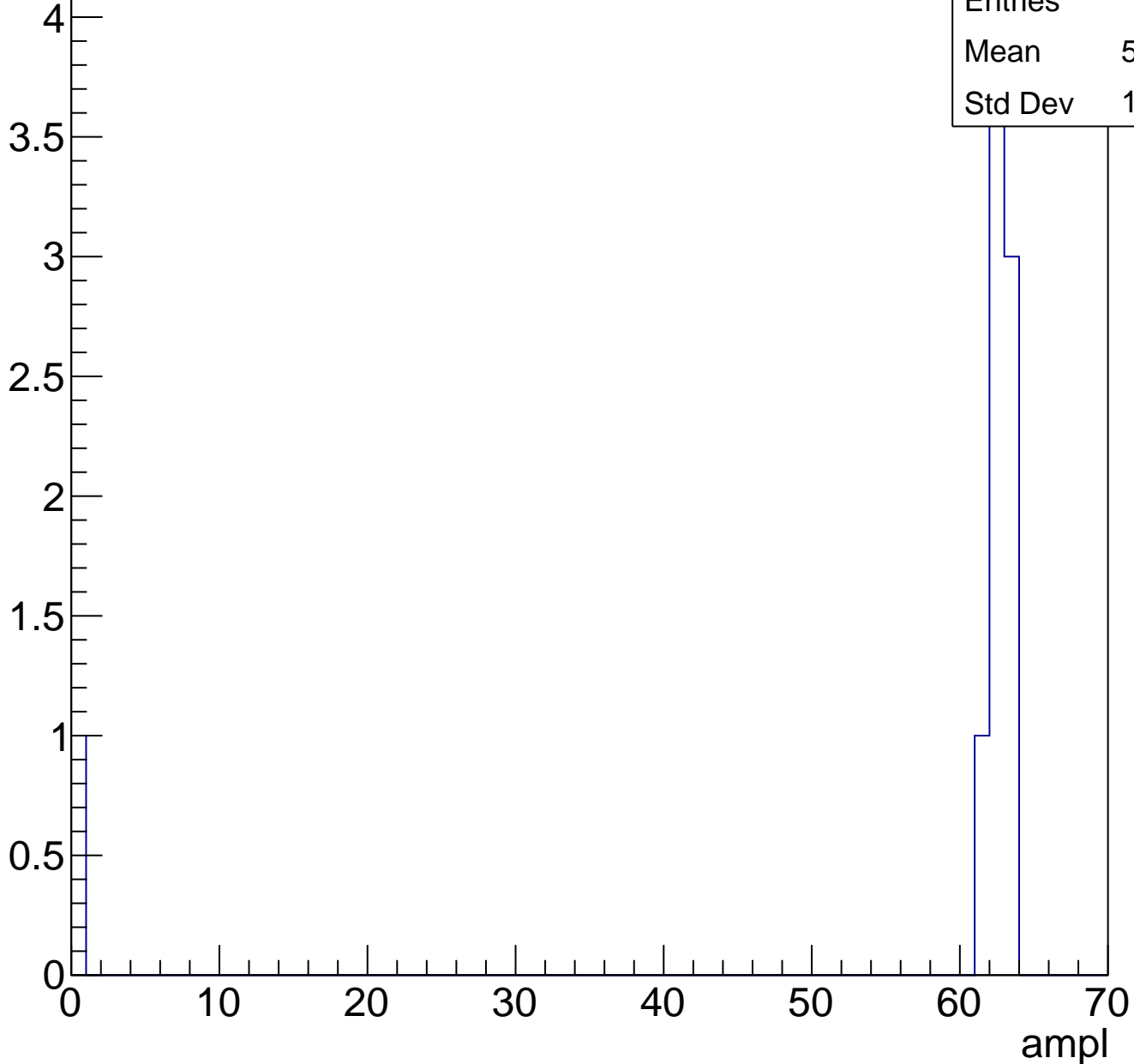
Entries	46
Mean	59.74
Std Dev	2.427



# B1L101S, U11-ch34, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch34, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U11-ch35, adc0

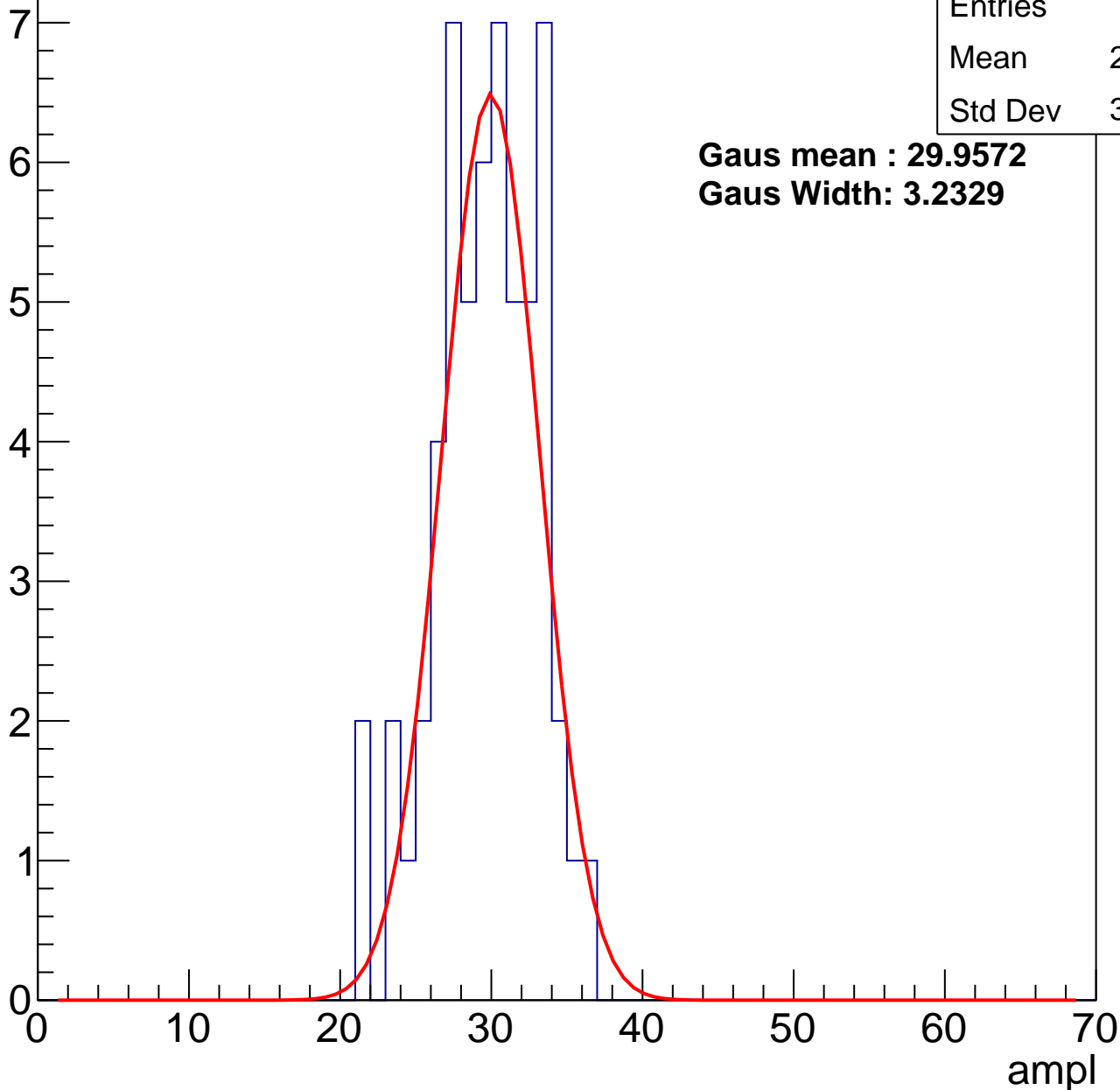
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	29.19
Std Dev	3.358

**Gaus mean : 29.9572**

**Gaus Width: 3.2329**



# B1L101S, U11-ch35, adc1

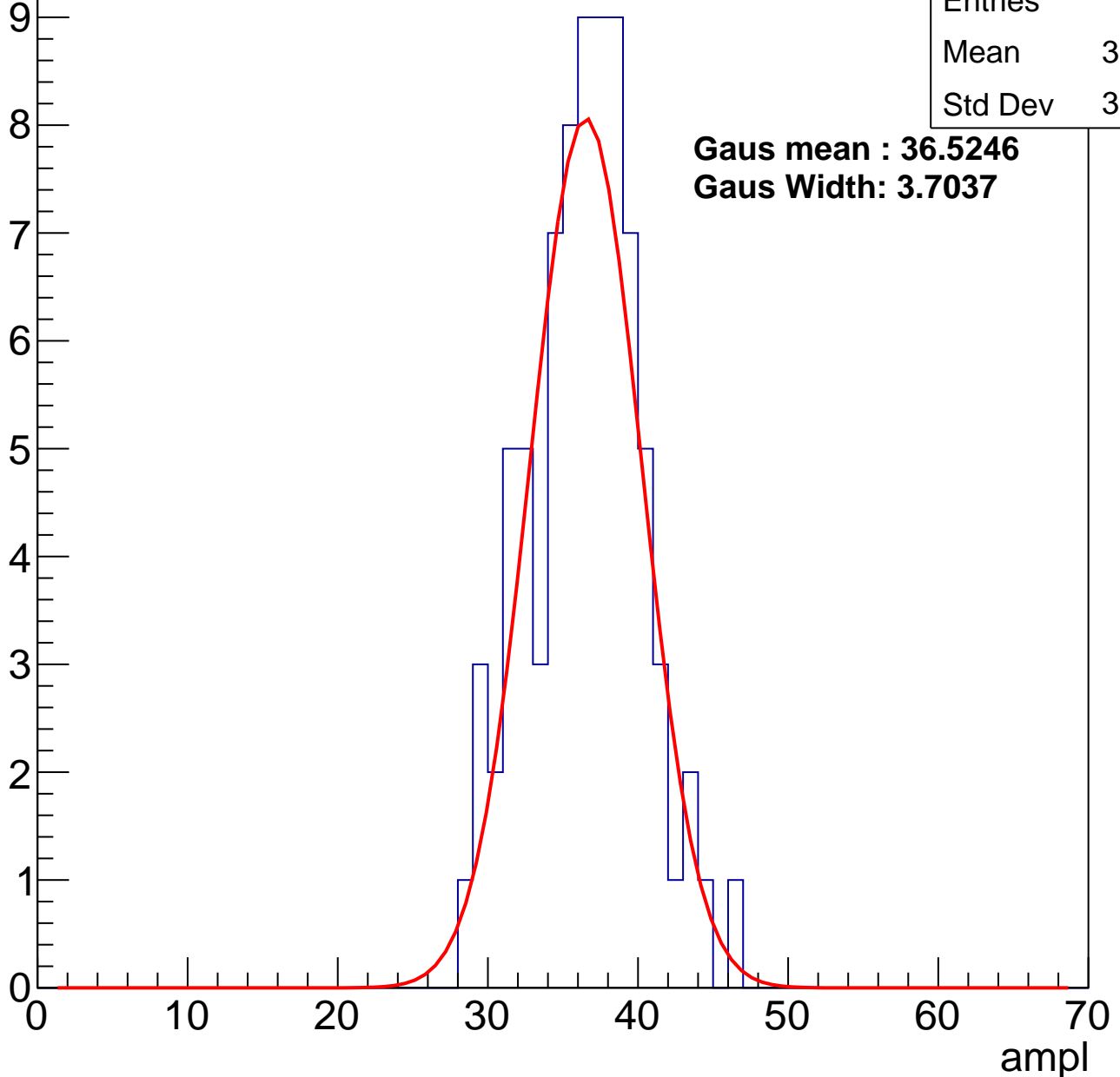
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	81
Mean	36.05
Std Dev	3.705

**Gaus mean : 36.5246**

**Gaus Width: 3.7037**



# B1L101S, U11-ch35, adc2

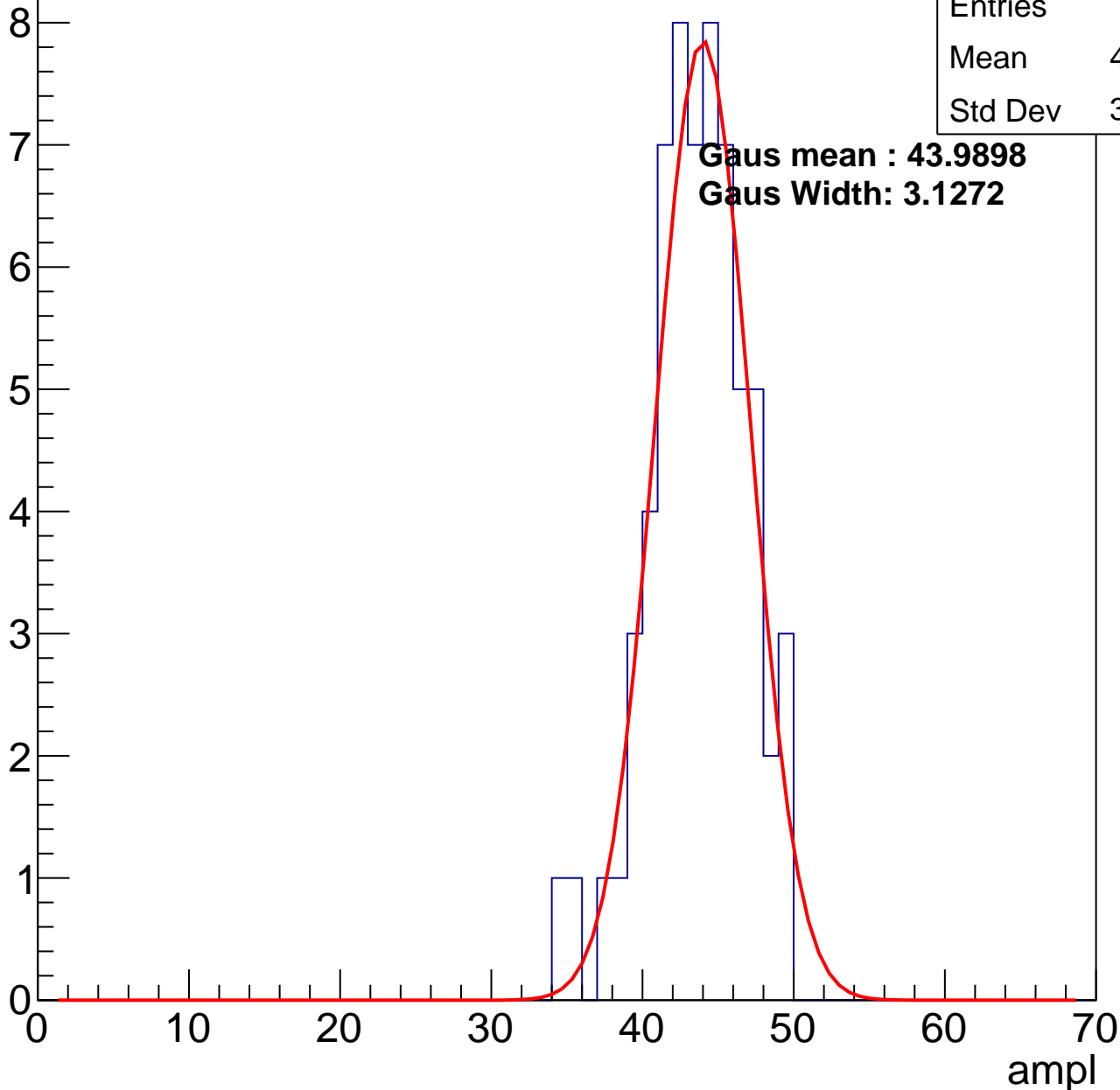
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	43.17
Std Dev	3.195

**Gaus mean : 43.9898**

**Gaus Width: 3.1272**



# B1L101S, U11-ch35, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	84
Mean	50.79
Std Dev	3.867

Entry

10

8

6

4

2

0

0

10

20

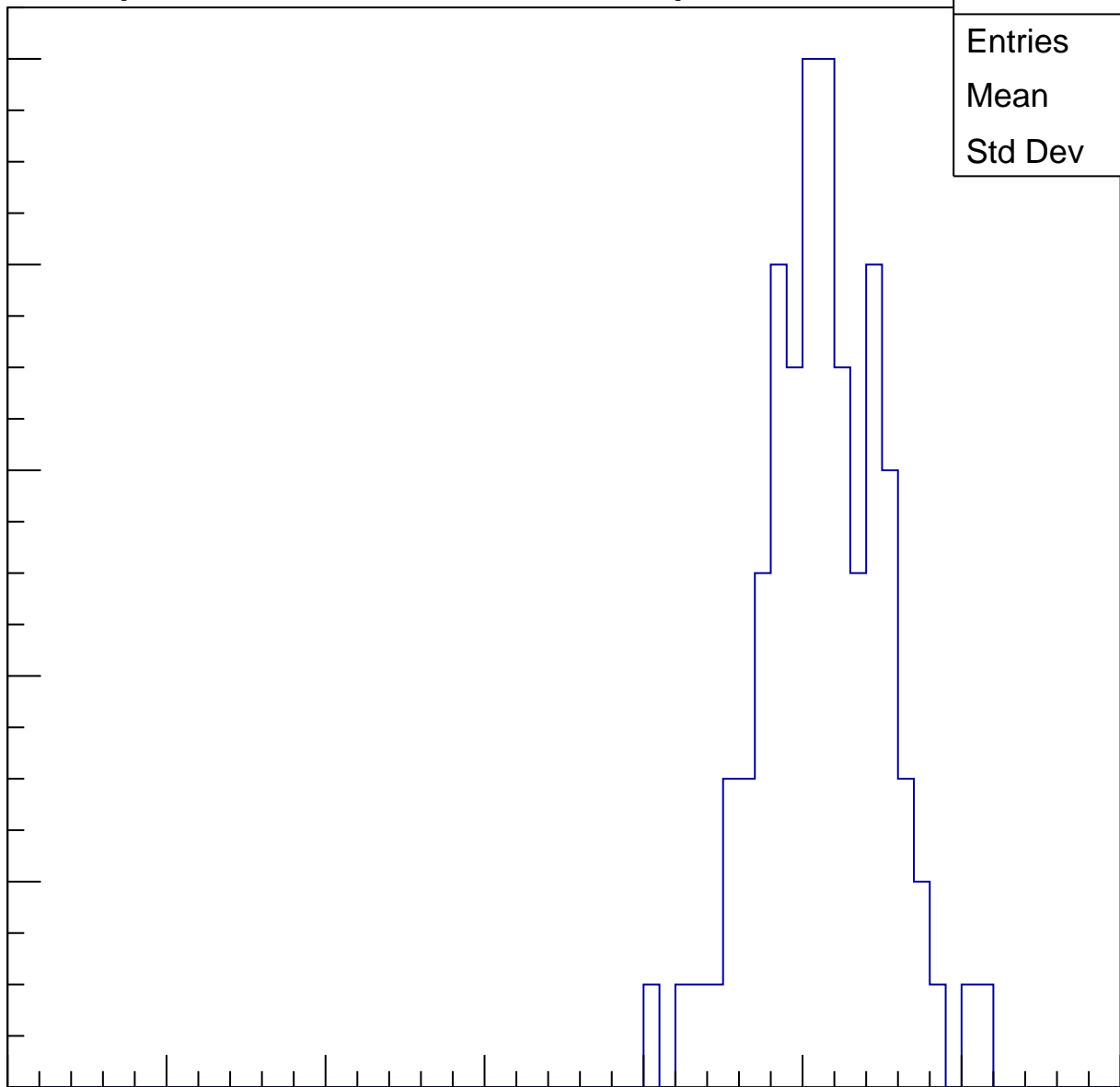
30

40

50

60

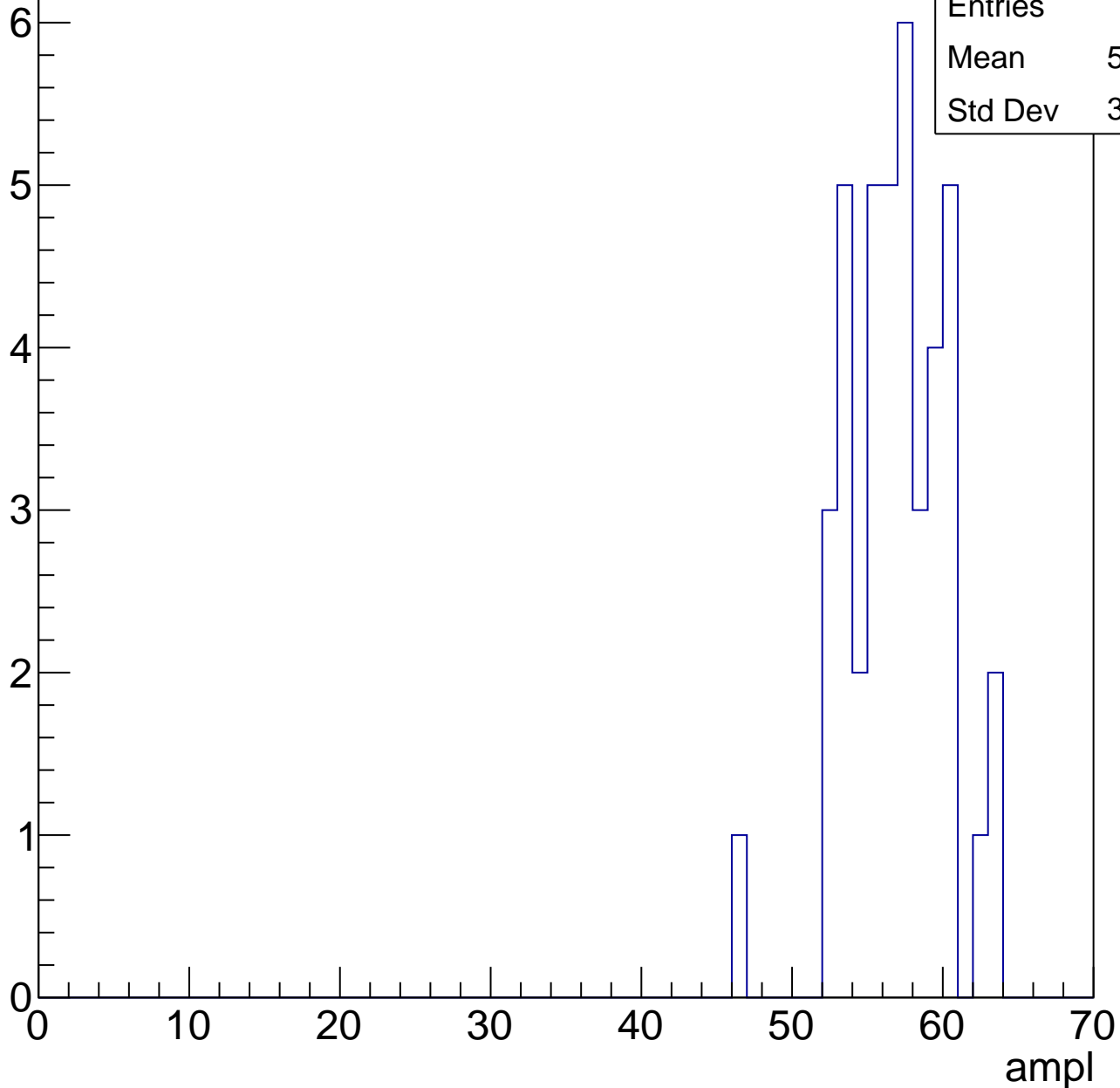
ampl



# B1L101S, U11-ch35, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

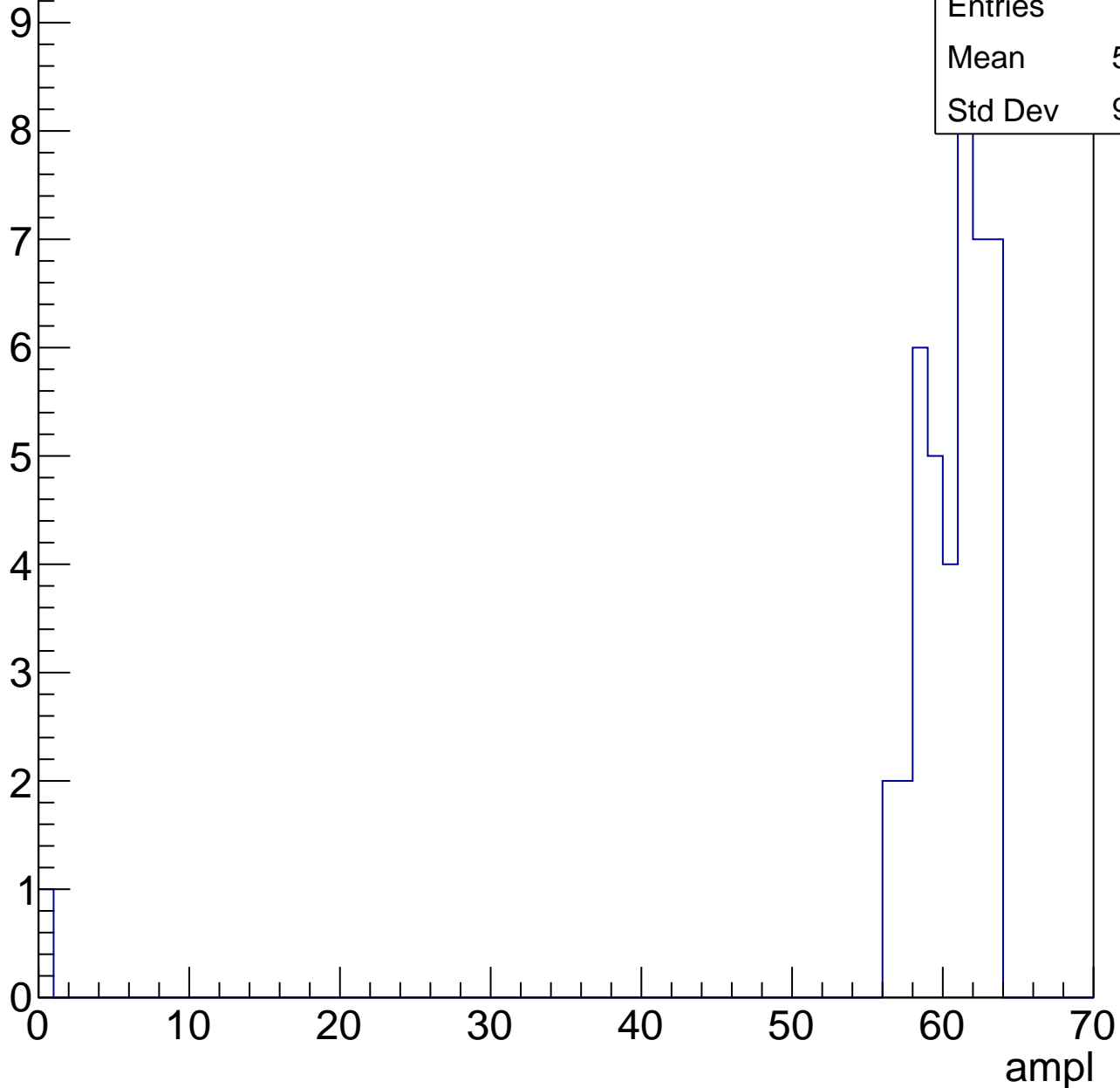
Entry



# B1L101S, U11-ch35, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U11-ch35, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch35, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U11-ch36, adc0

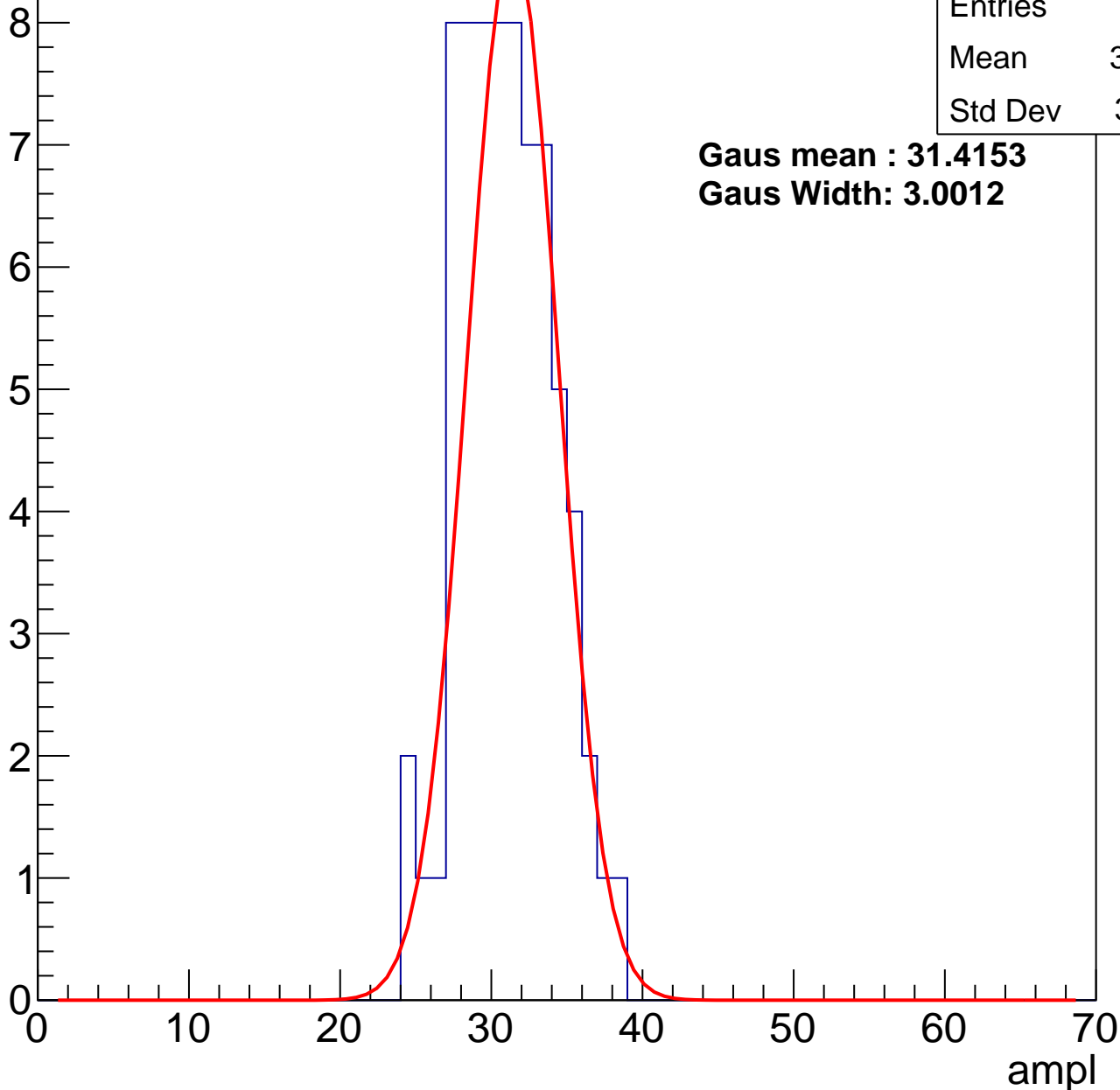
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	30.58
Std Dev	3.061

**Gaus mean : 31.4153**

**Gaus Width: 3.0012**



# B1L101S, U11-ch36, adc1

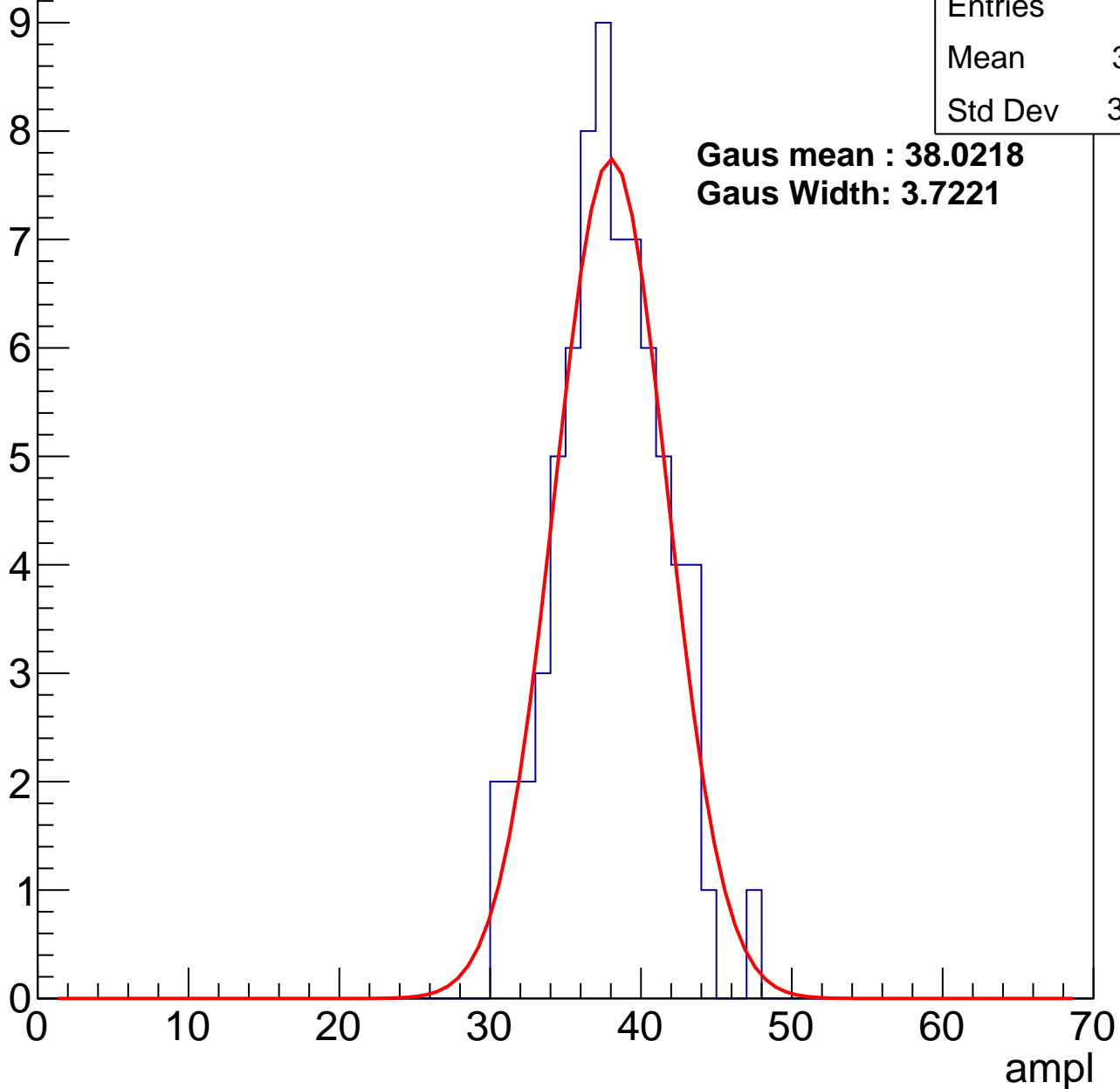
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	37.51
Std Dev	3.512

**Gaus mean : 38.0218**

**Gaus Width: 3.7221**



# B1L101S, U11-ch36, adc2

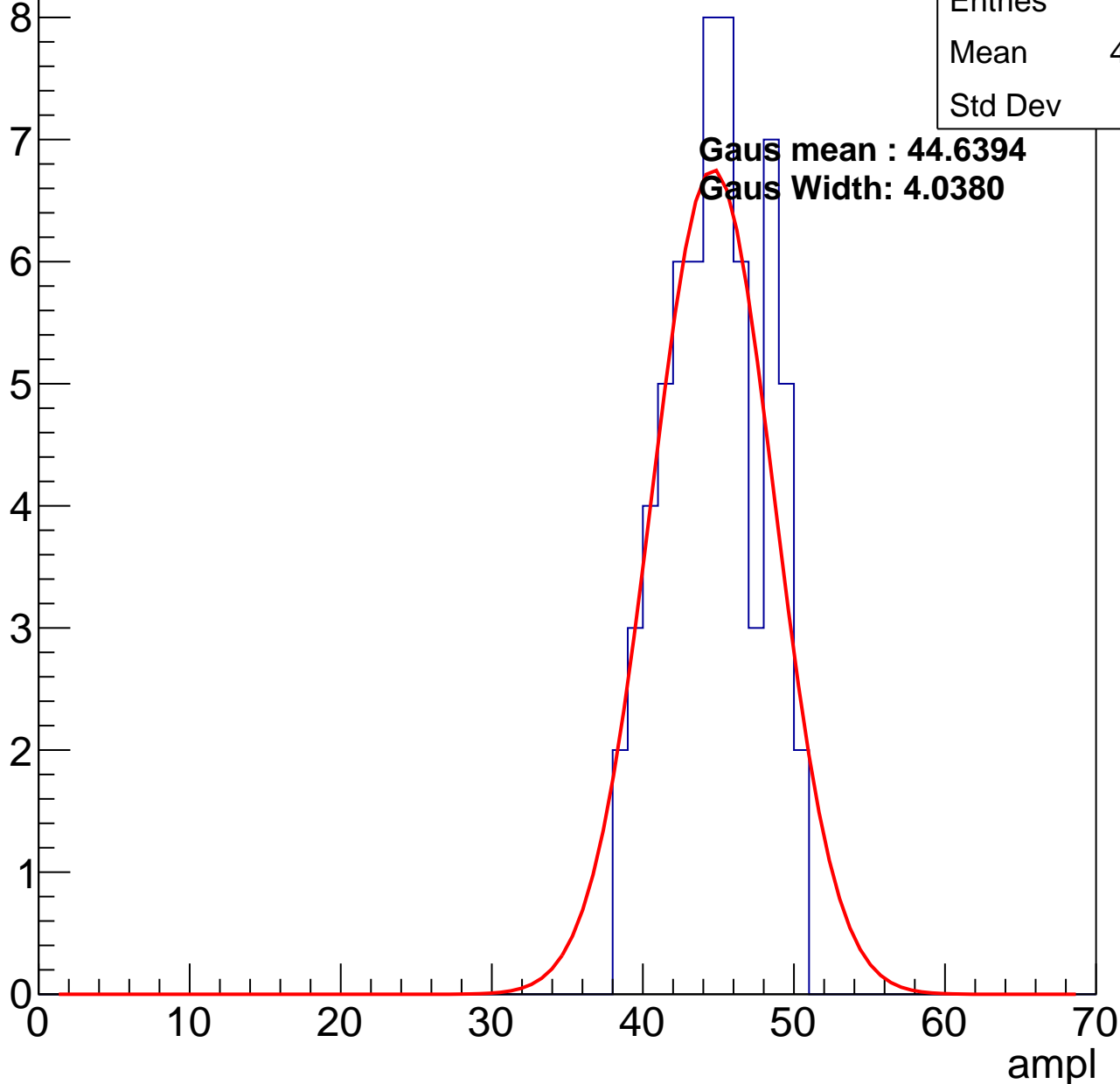
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	44.28
Std Dev	3.16

Gaus mean : 44.6394

Gaus Width: 4.0380

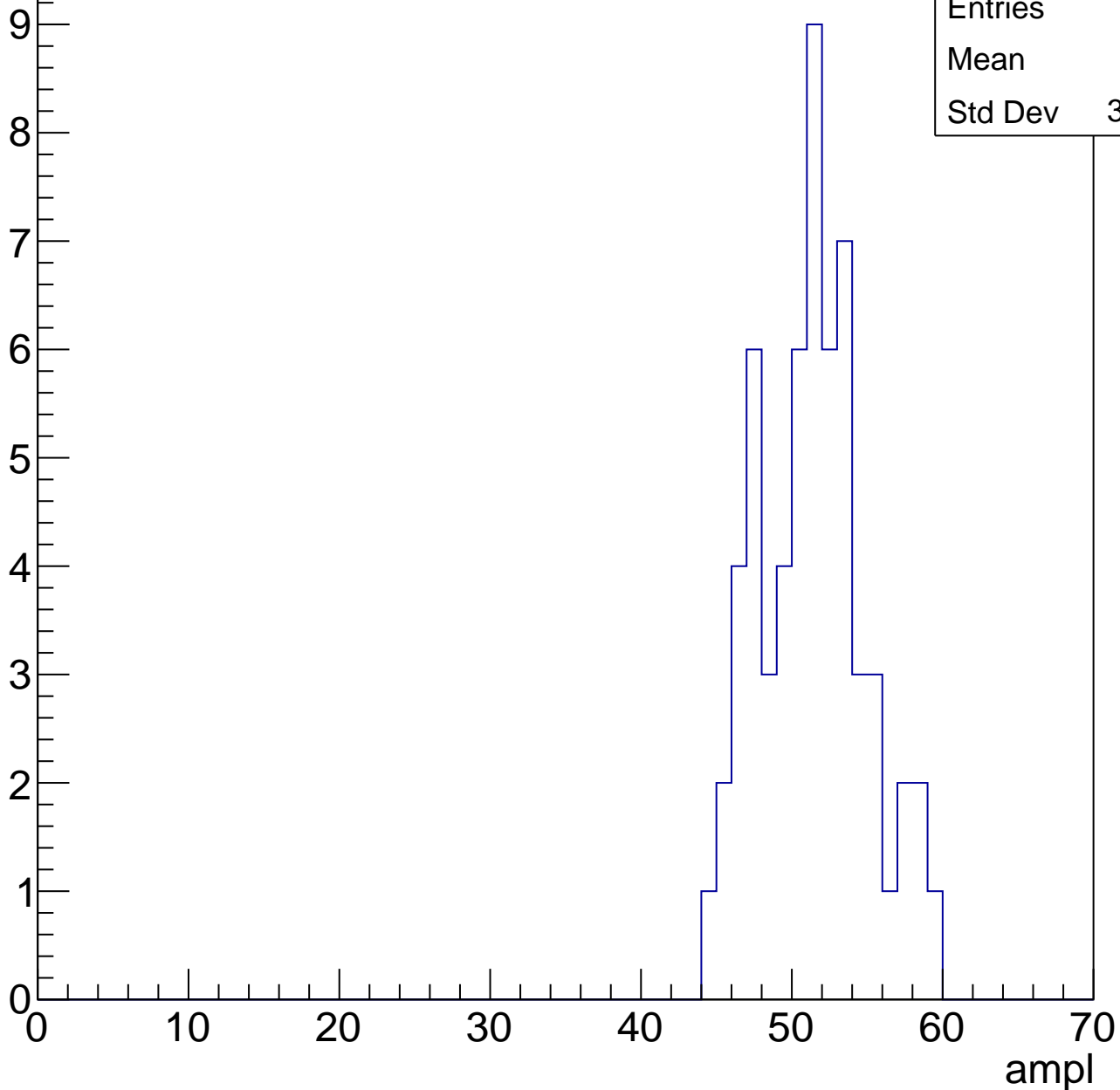


# B1L101S, U11-ch36, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

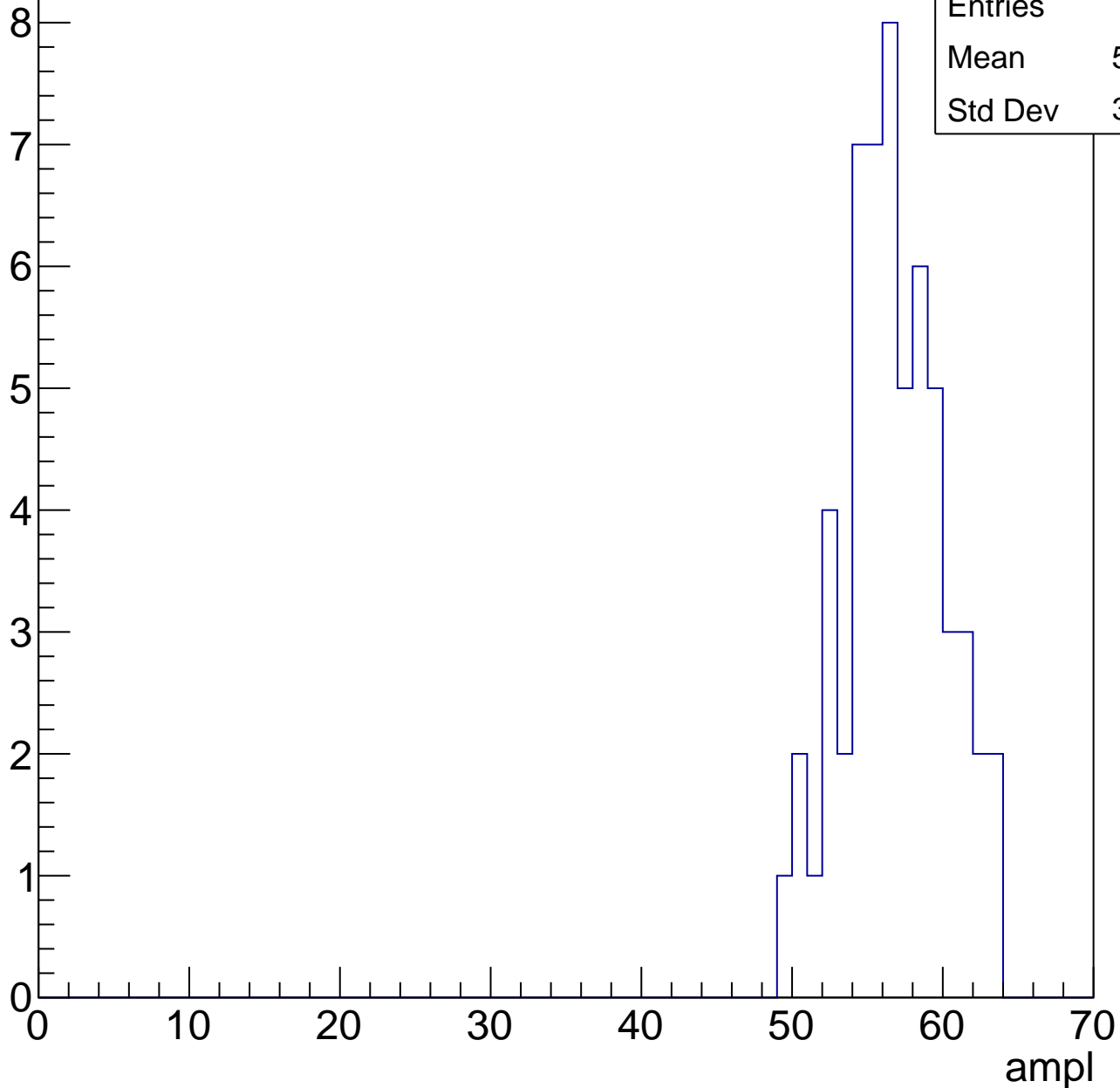
Entries	60
Mean	50.9
Std Dev	3.496



# B1L101S, U11-ch36, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



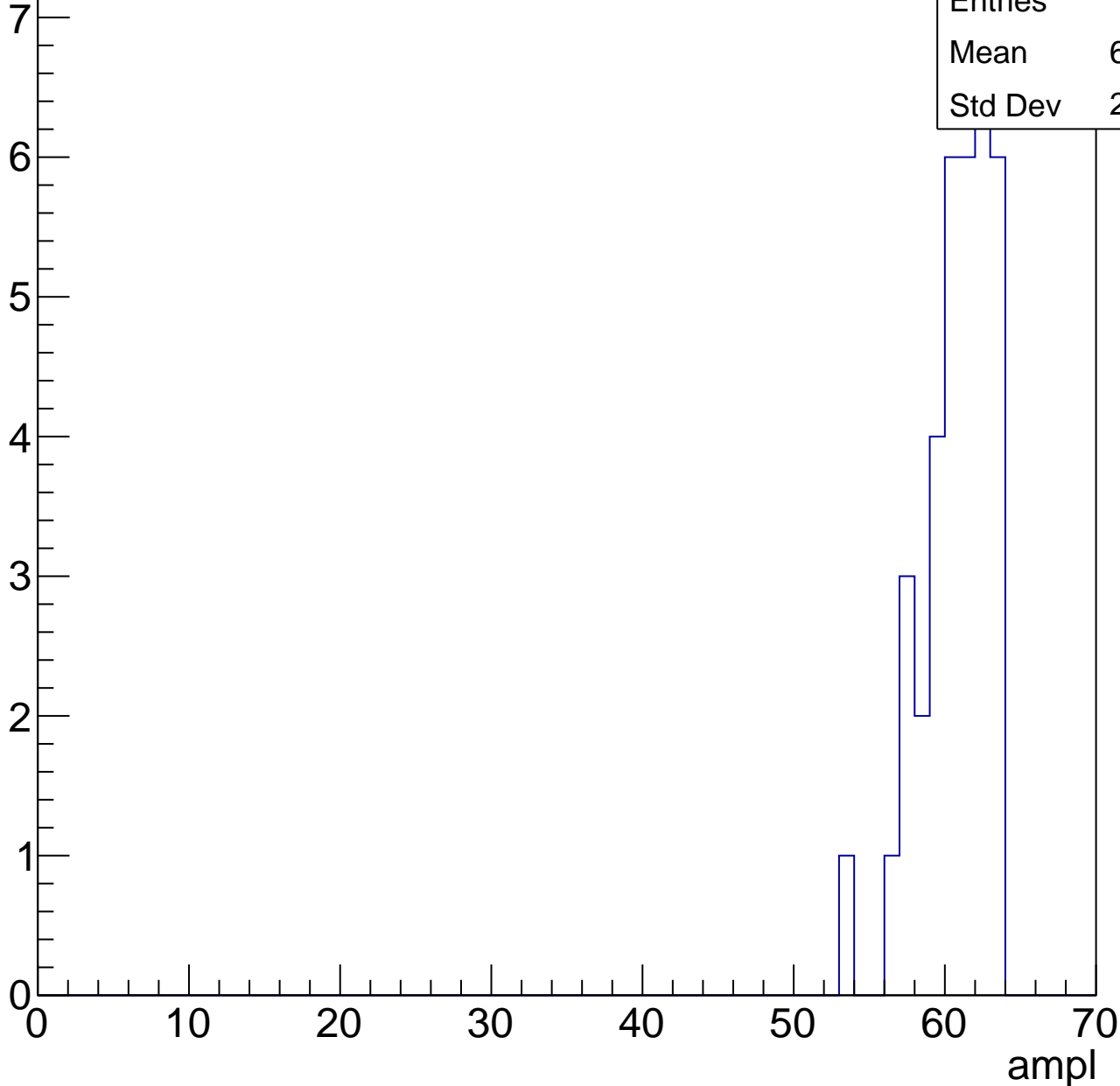
Entries	58
Mean	56.31
Std Dev	3.281

# B1L101S, U11-ch36, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	36
Mean	60.28
Std Dev	2.293



# B1L101S, U11-ch36, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

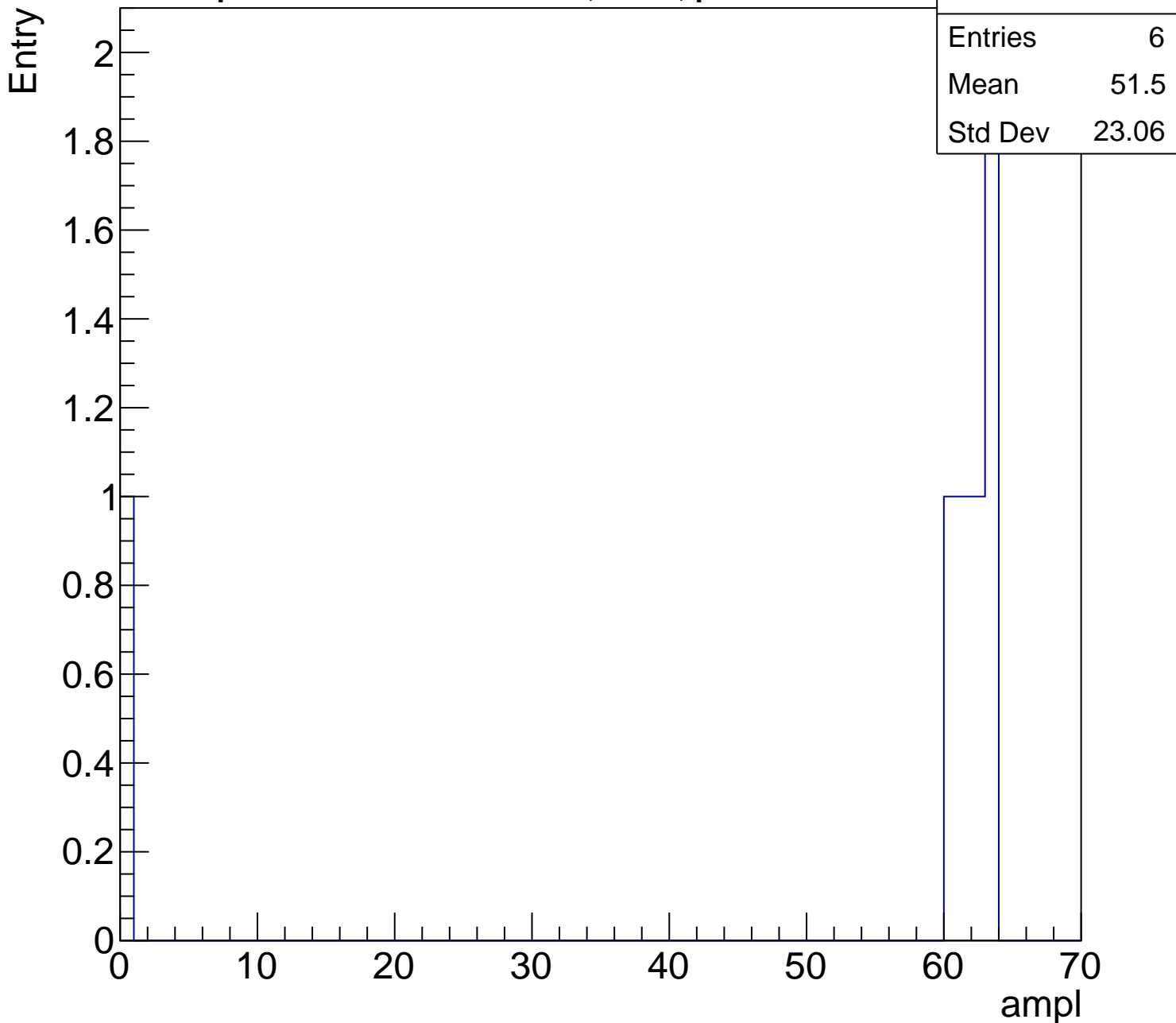
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	51.5
Std Dev	23.06

0 10 20 30 40 50 60 70

ampl





# B1L101S, U11-ch36, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U11-ch37, adc0

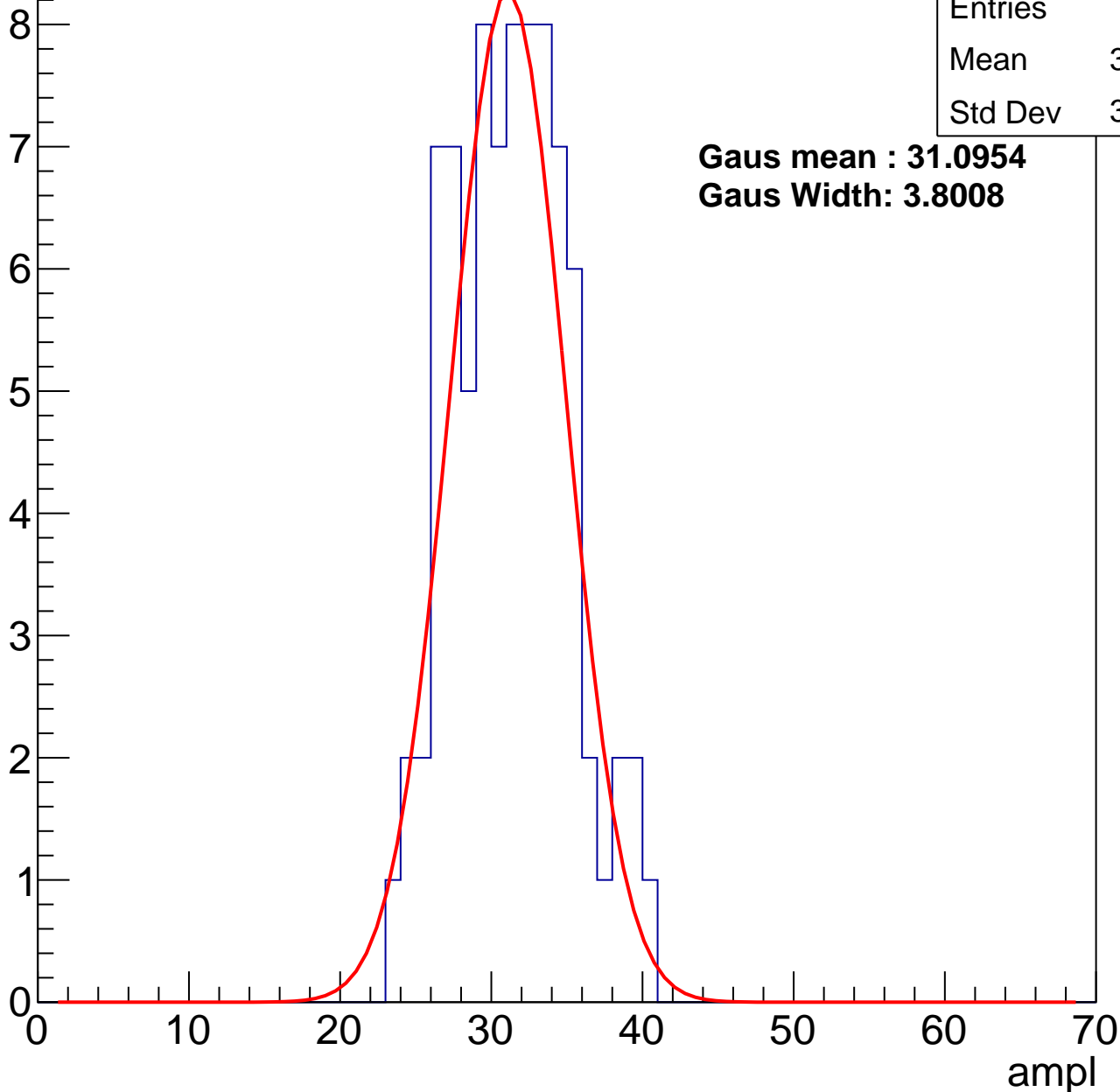
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	84
Mean	30.87
Std Dev	3.773

**Gaus mean : 31.0954**

**Gaus Width: 3.8008**



# B1L101S, U11-ch37, adc1

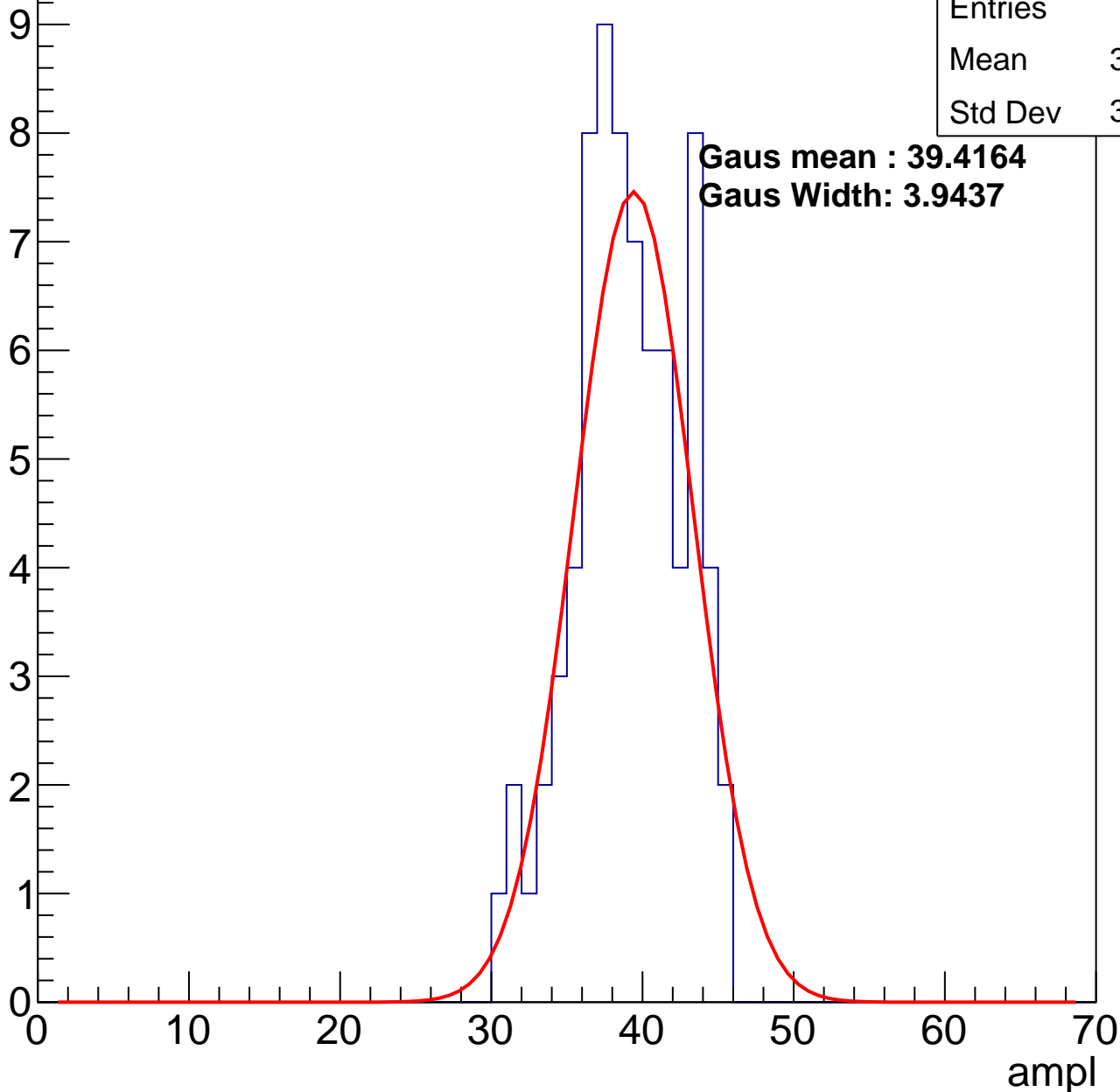
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	38.59
Std Dev	3.537

**Gaus mean : 39.4164**

**Gaus Width: 3.9437**



# B1L101S, U11-ch37, adc2

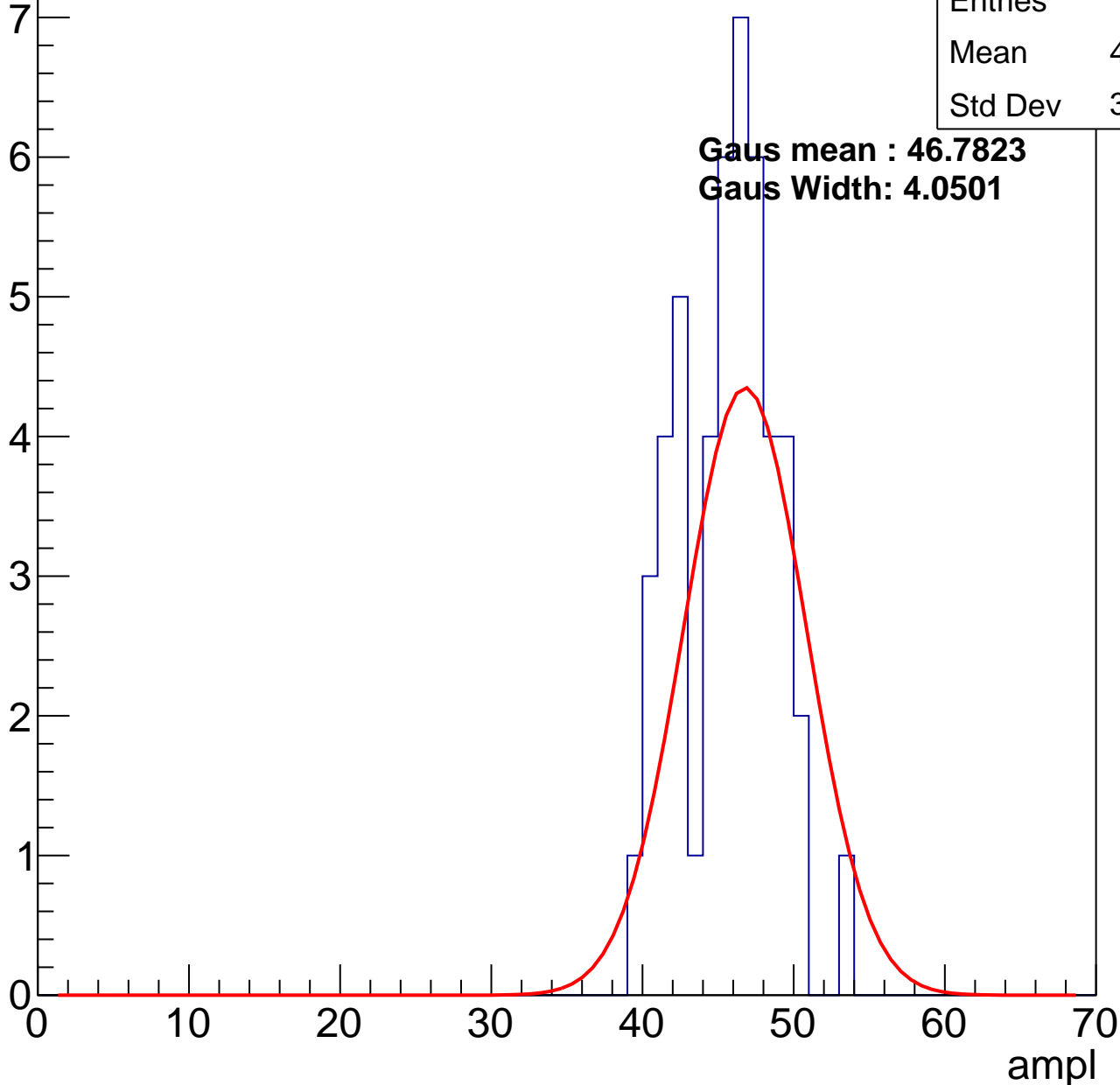
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	48
Mean	45.15
Std Dev	3.136

**Gaus mean : 46.7823**

**Gaus Width: 4.0501**

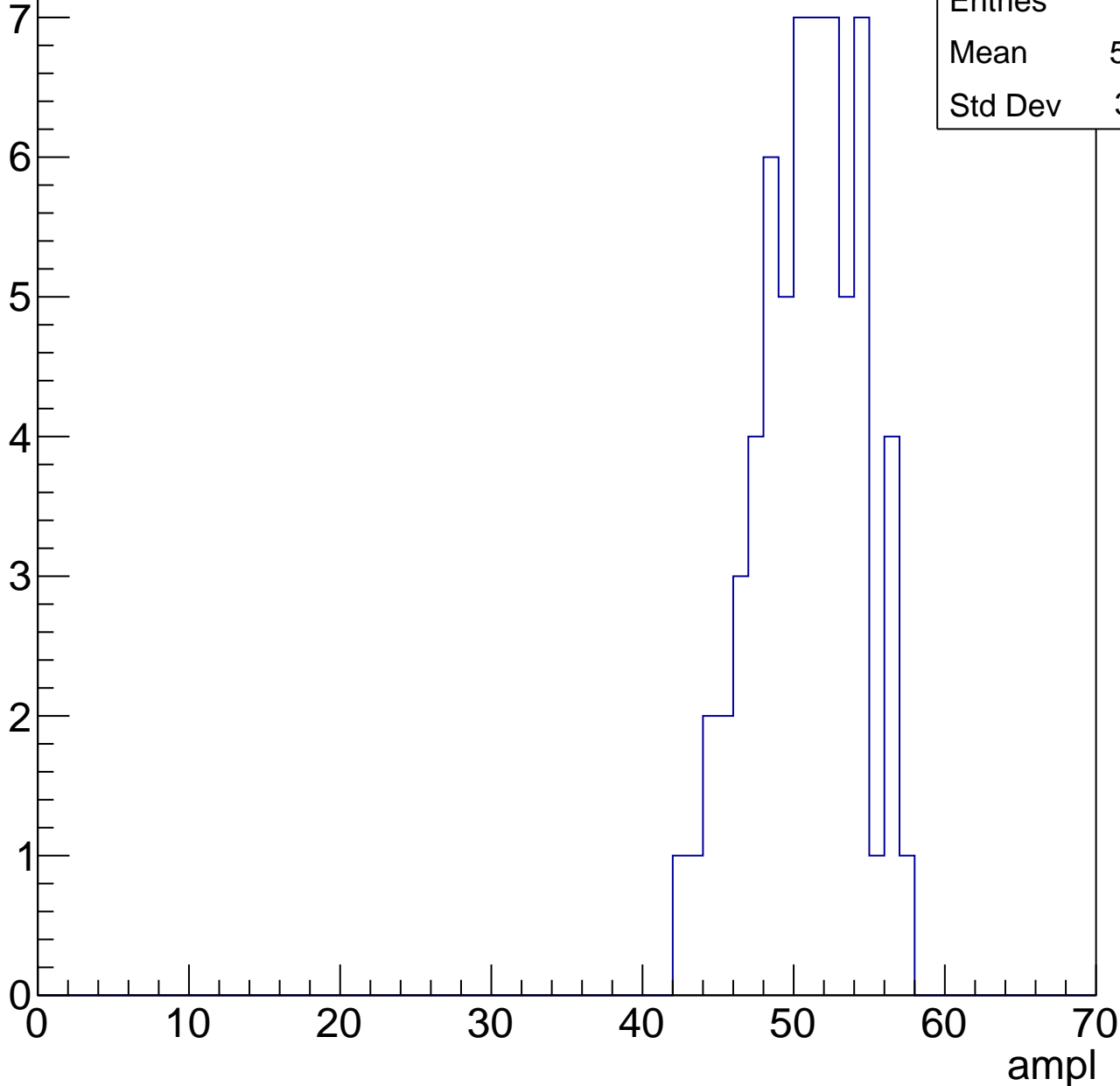


# B1L101S, U11-ch37, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

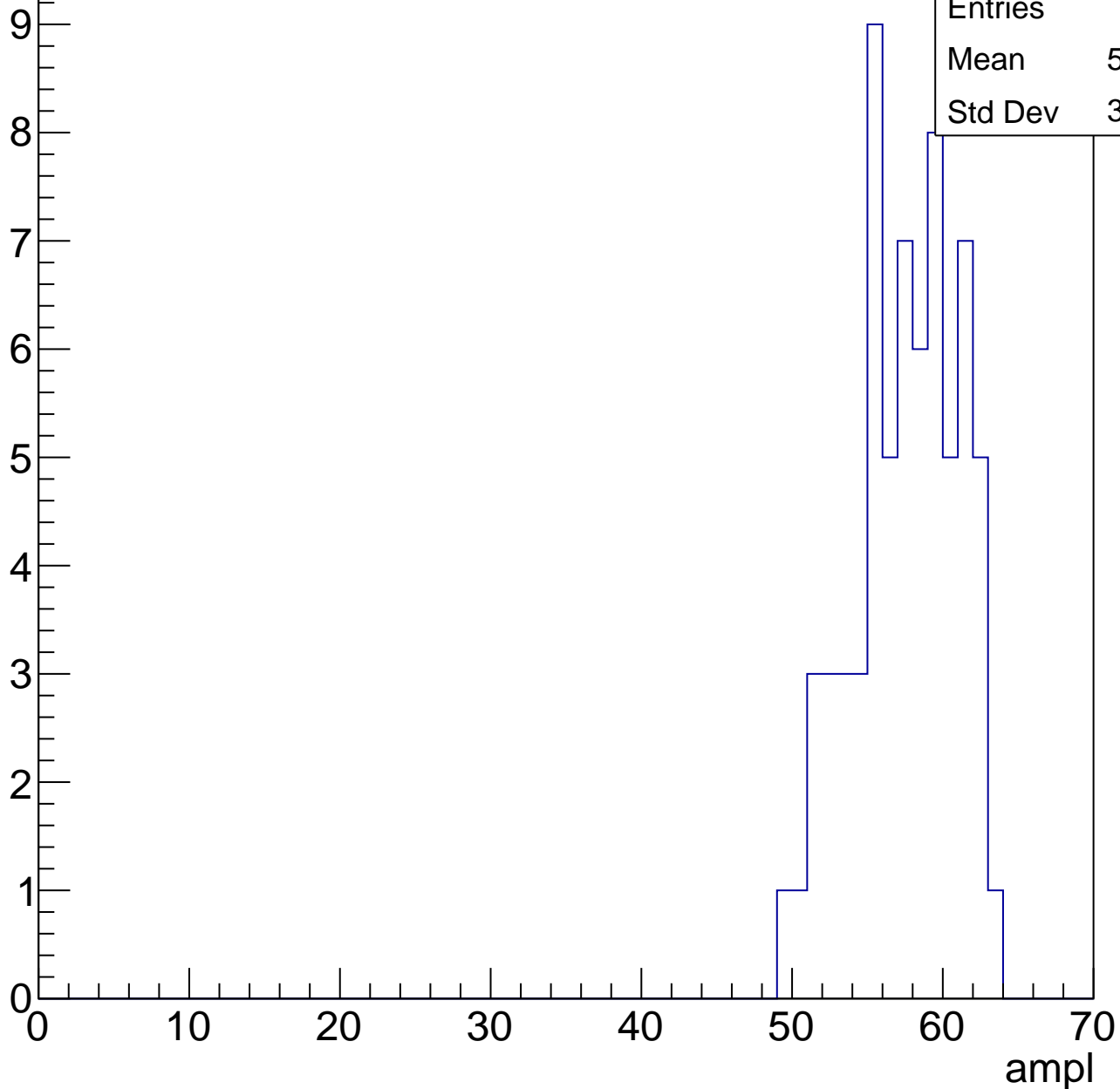
Entries	63
Mean	50.35
Std Dev	3.451



# B1L101S, U11-ch37, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



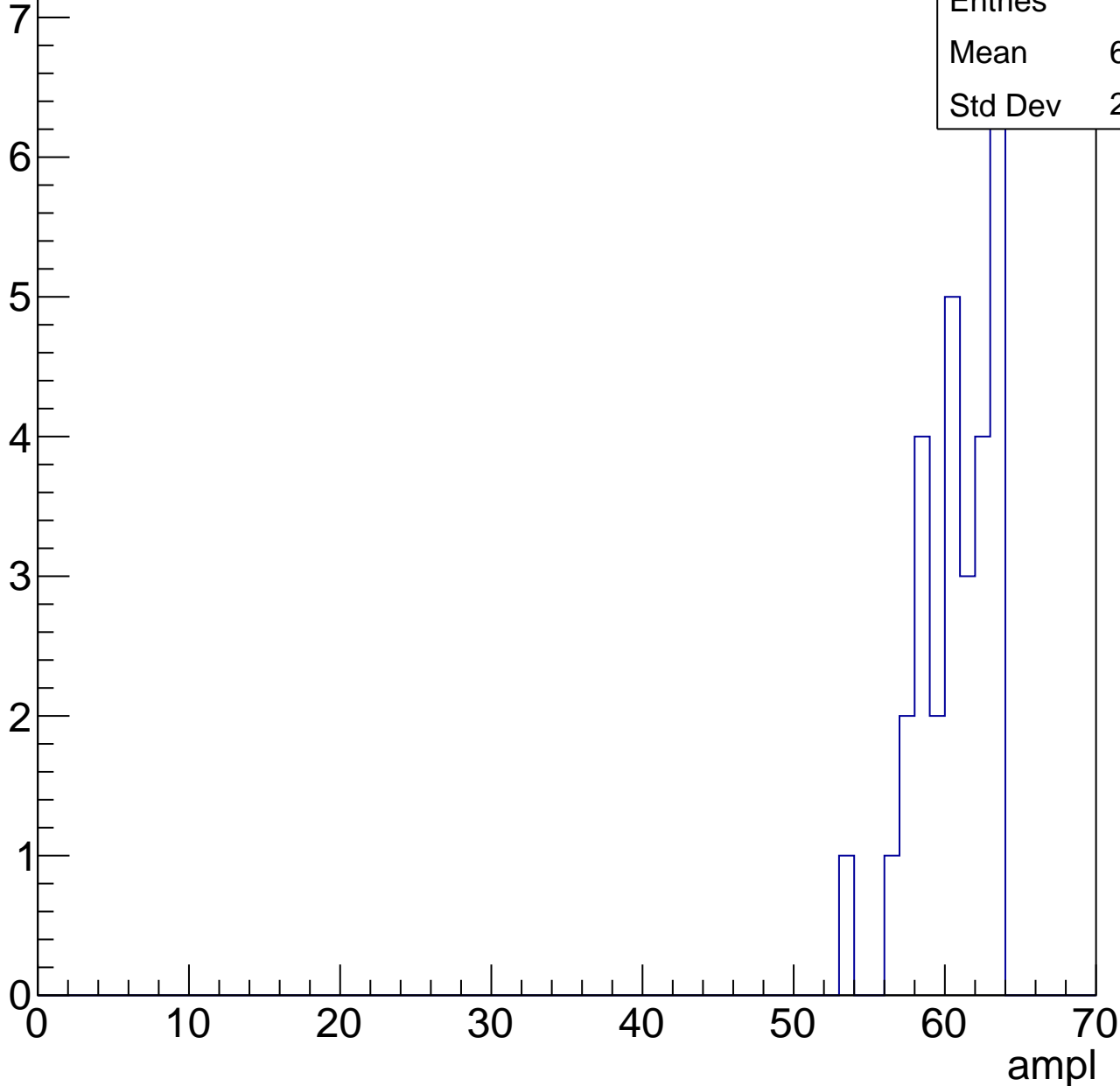
Entries	67
Mean	57.06
Std Dev	3.385

# B1L101S, U11-ch37, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	29
Mean	60.17
Std Dev	2.506



# B1L101S, U11-ch37, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch37, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U11-ch38, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	75
Mean	28.83
Std Dev	3.292

**Gaus mean : 29.1587**

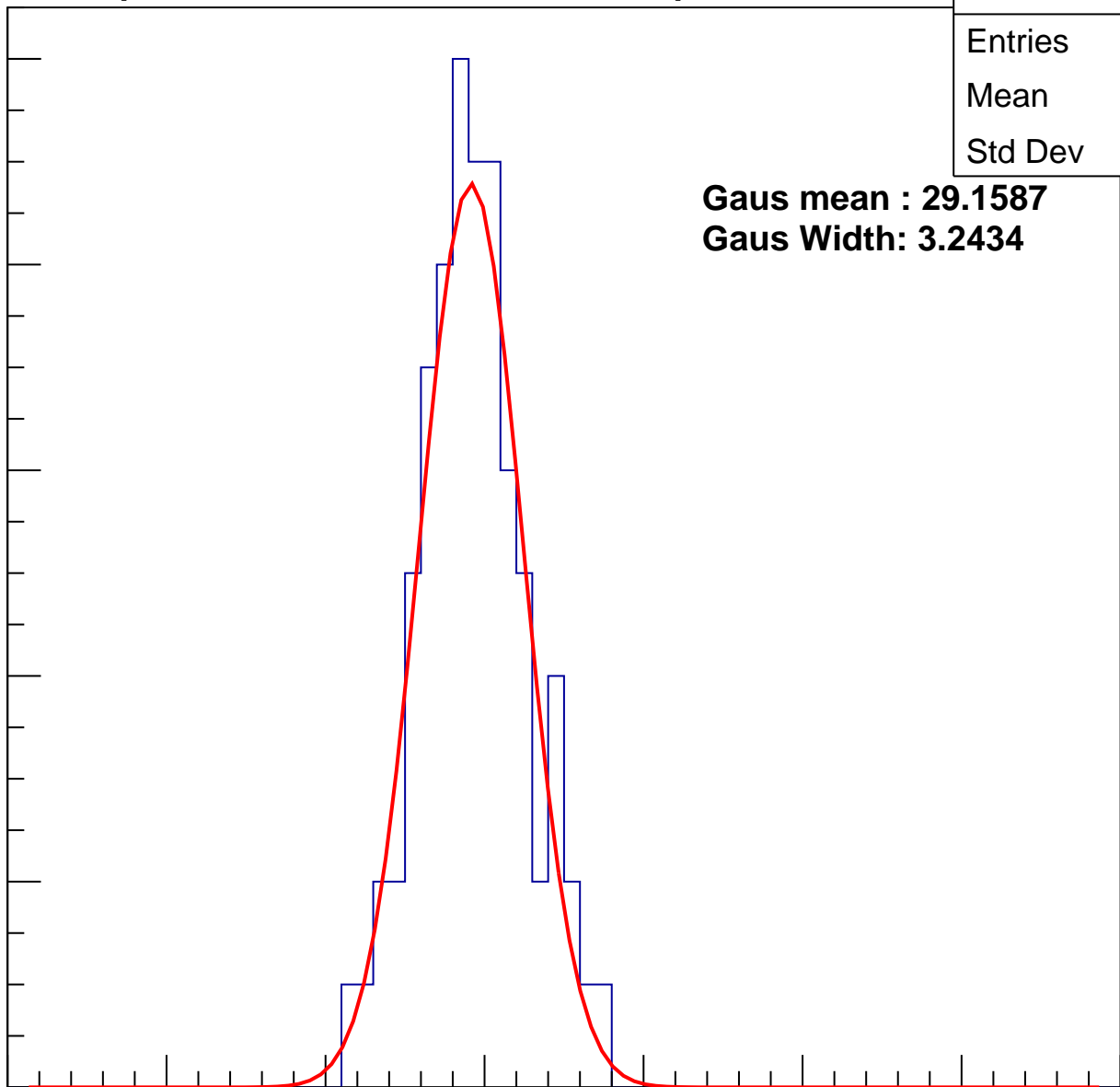
**Gaus Width: 3.2434**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



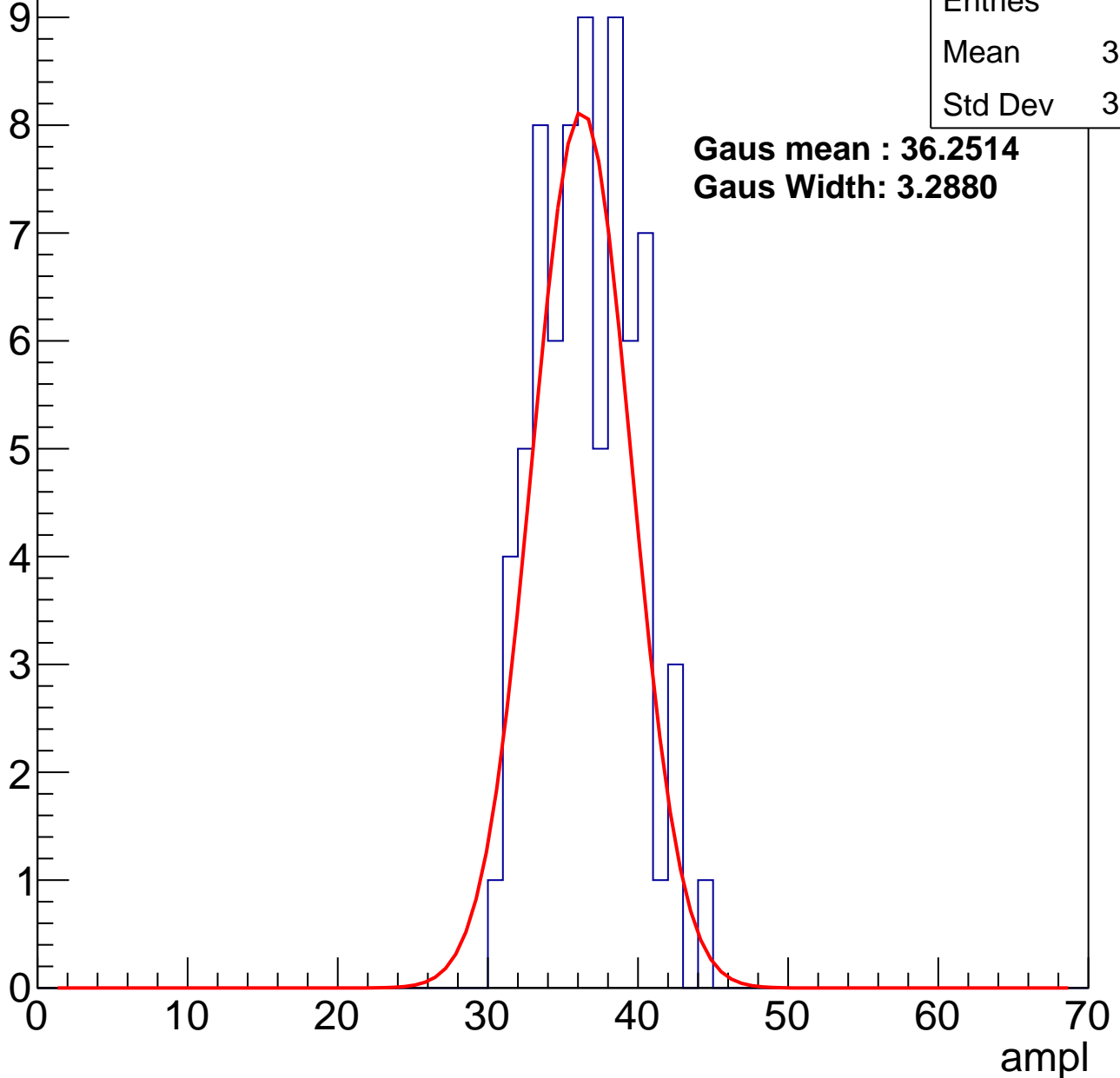
# B1L101S, U11-ch38, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	36.14
Std Dev	3.146

**Gaus mean : 36.2514**  
**Gaus Width: 3.2880**



# B1L101S, U11-ch38, adc2

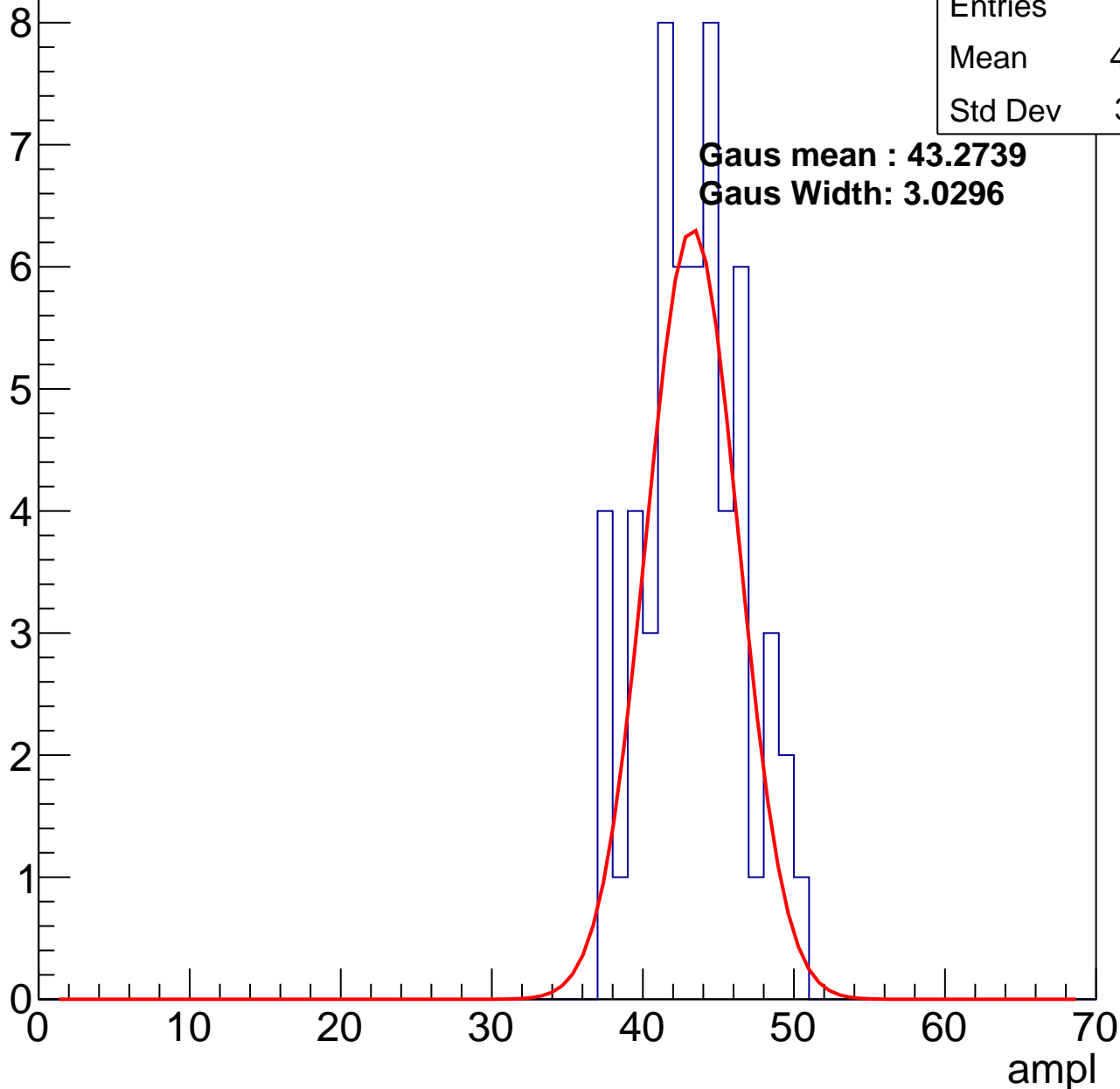
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	42.93
Std Dev	3.211

**Gaus mean : 43.2739**

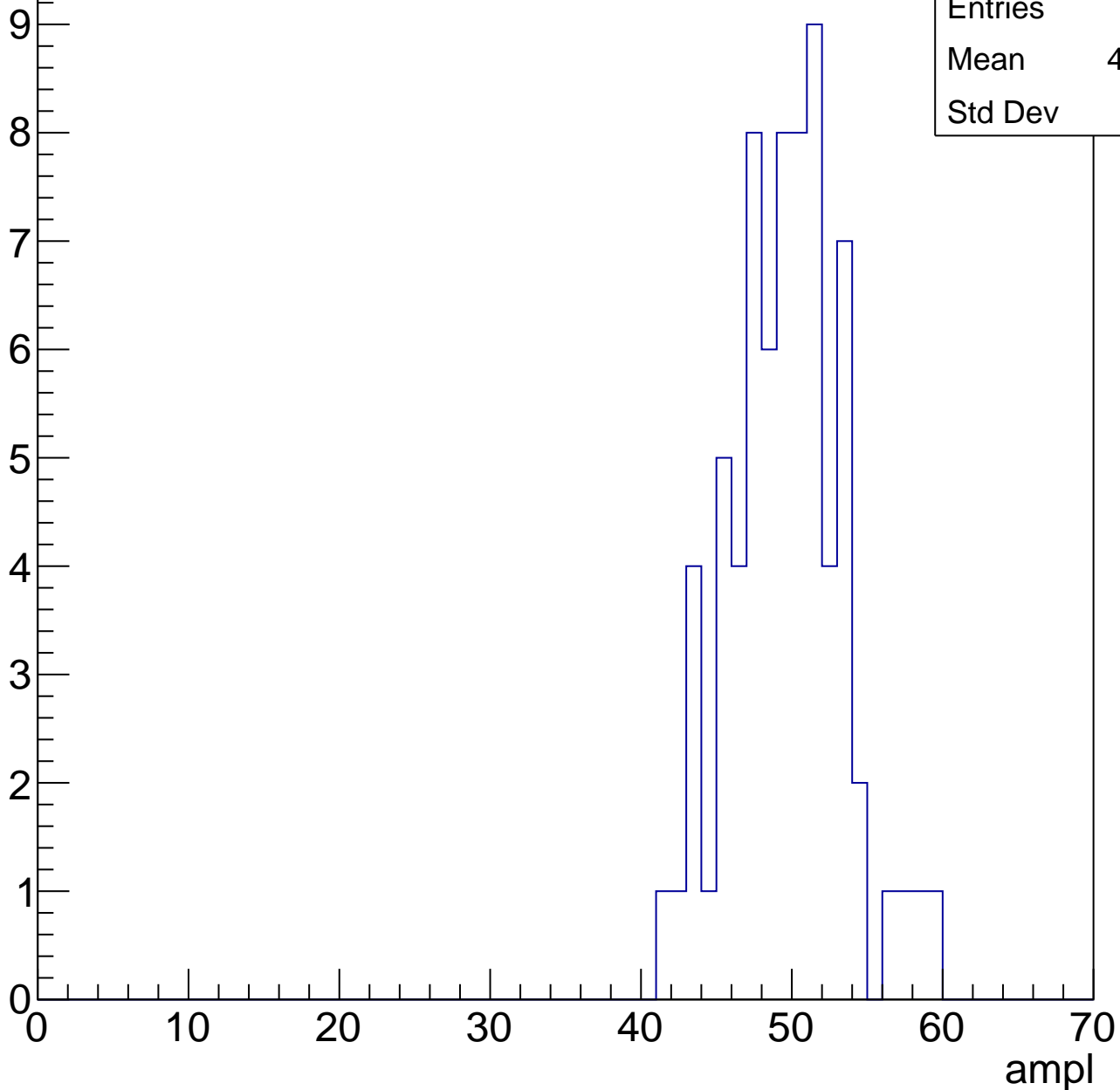
**Gaus Width: 3.0296**



# B1L101S, U11-ch38, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

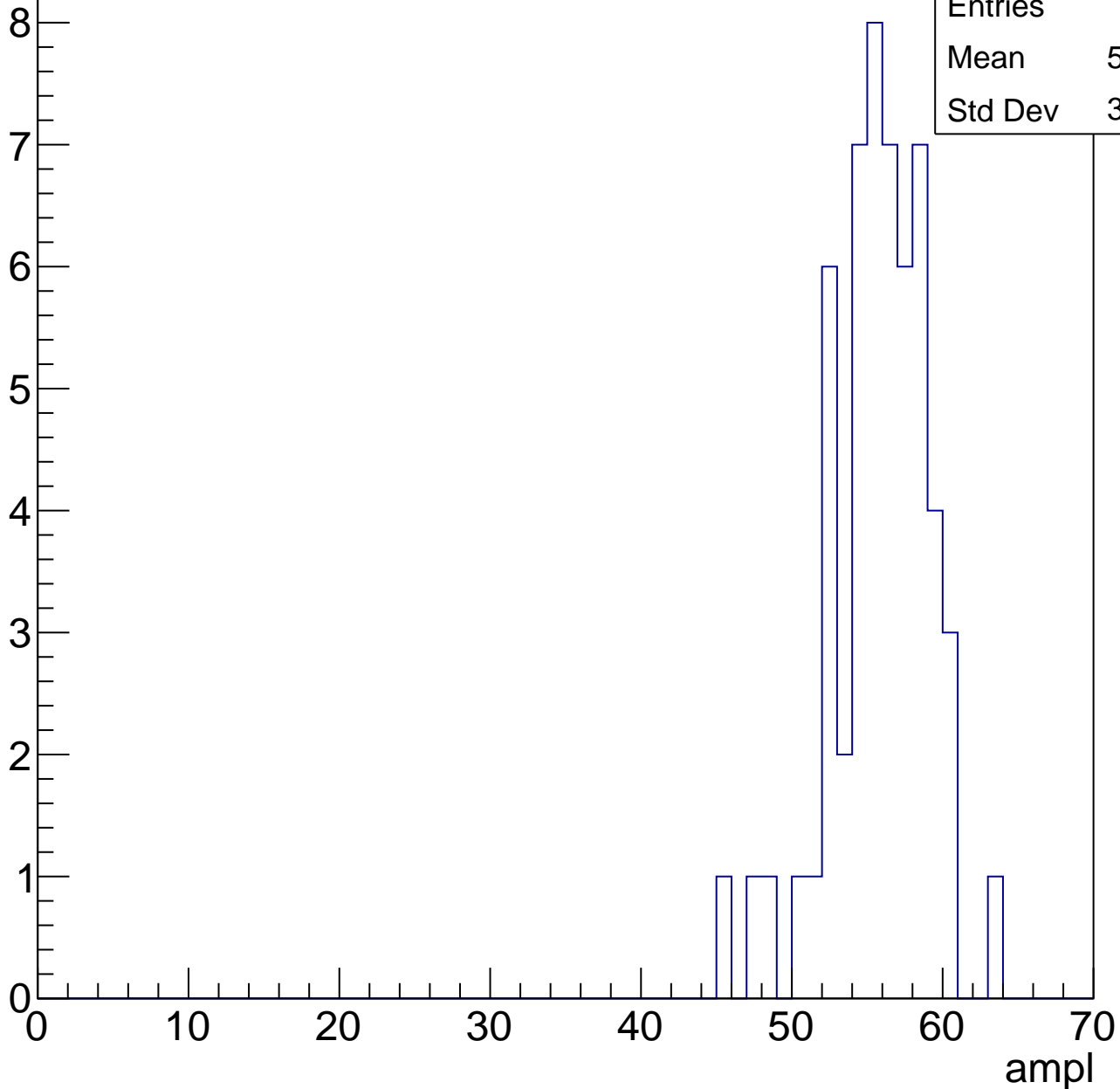


# B1L101S, U11-ch38, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	55.29
Std Dev	3.315

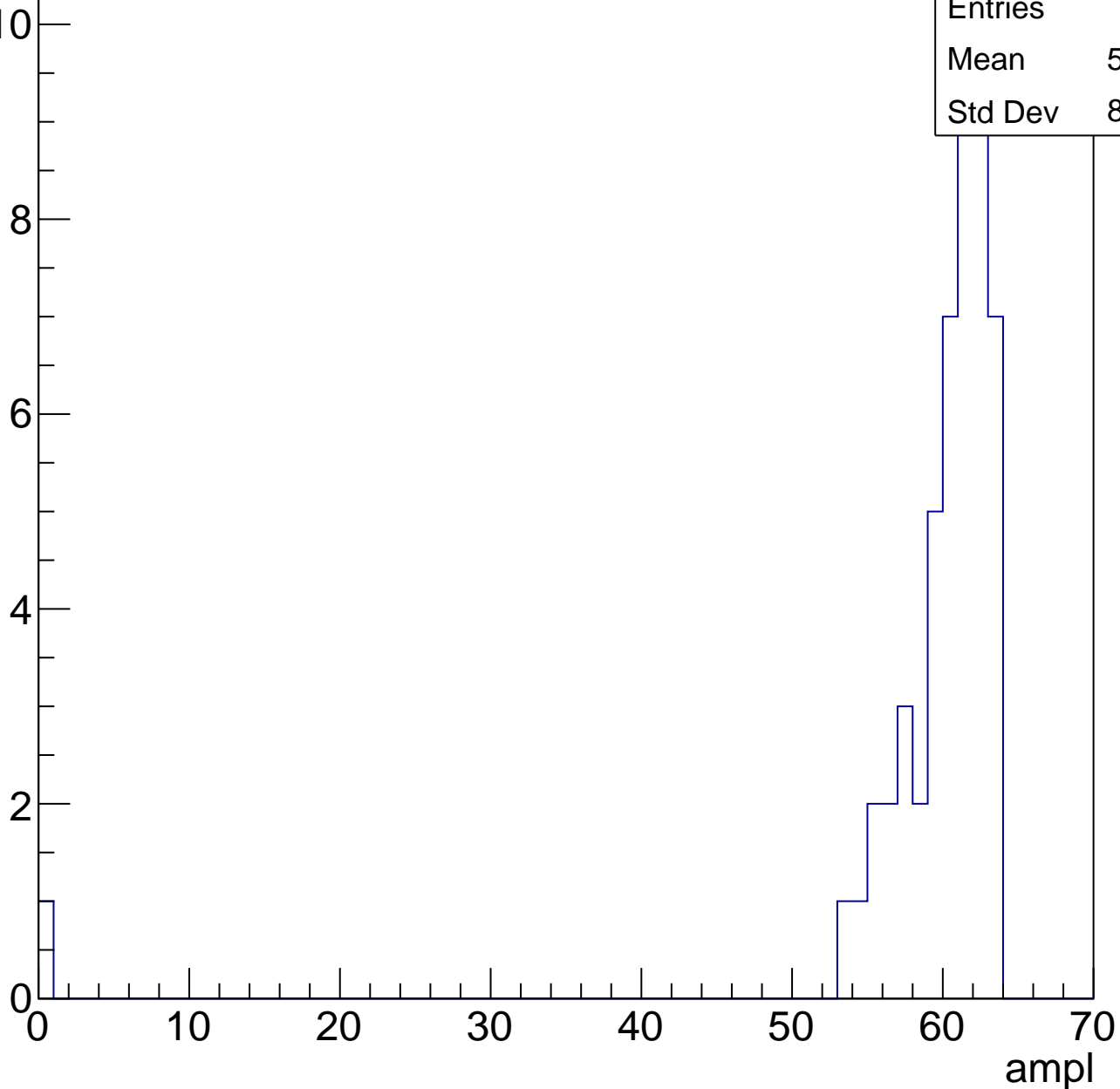


# B1L101S, U11-ch38, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	58.86
Std Dev	8.693



# B1L101S, U11-ch38, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	63
Std Dev	0

0 10 20 30 40 50 60 70

ampl



# B1L101S, U11-ch38, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U11-ch39, adc0

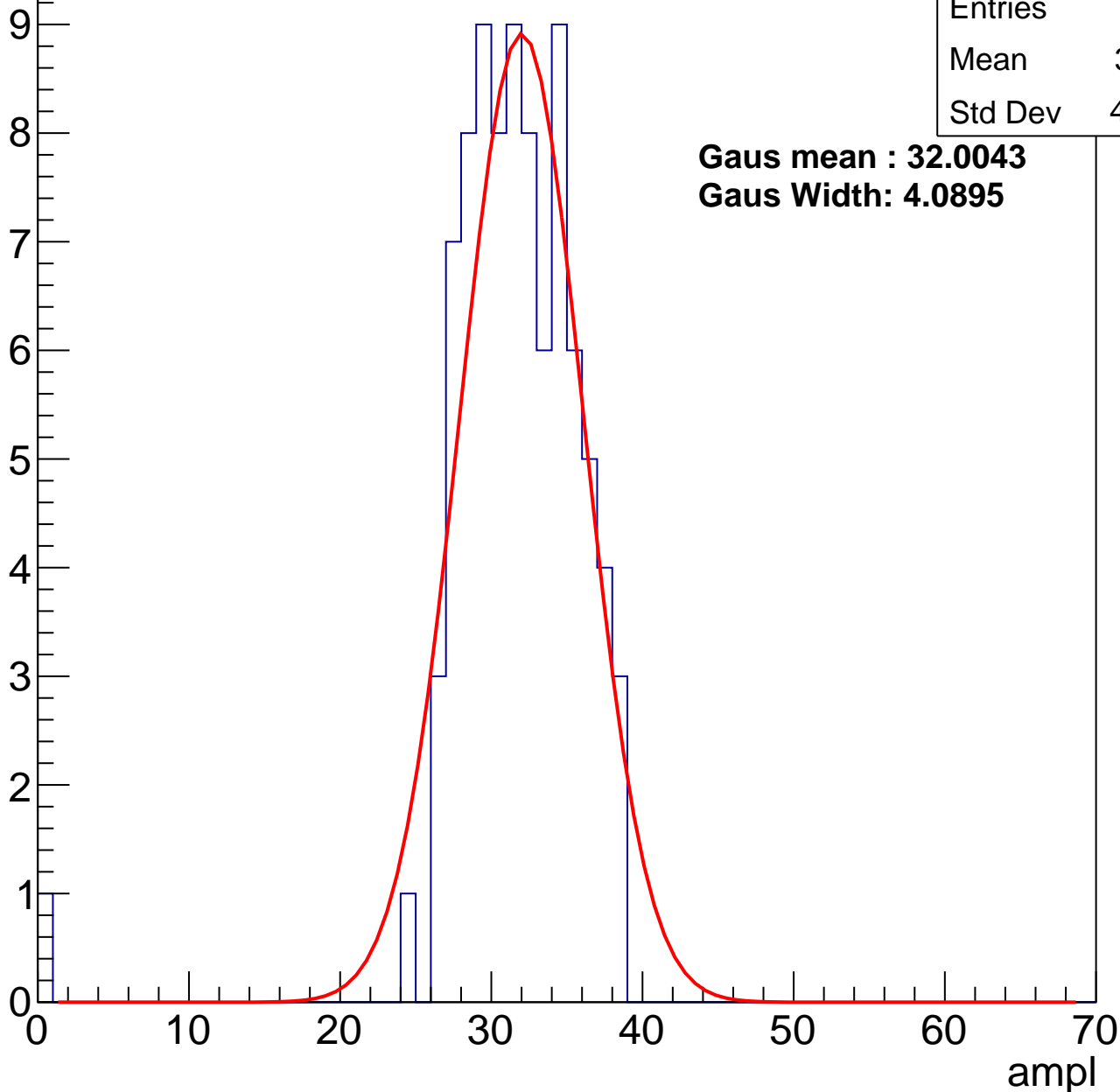
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	87
Mean	31.11
Std Dev	4.718

**Gaus mean : 32.0043**

**Gaus Width: 4.0895**



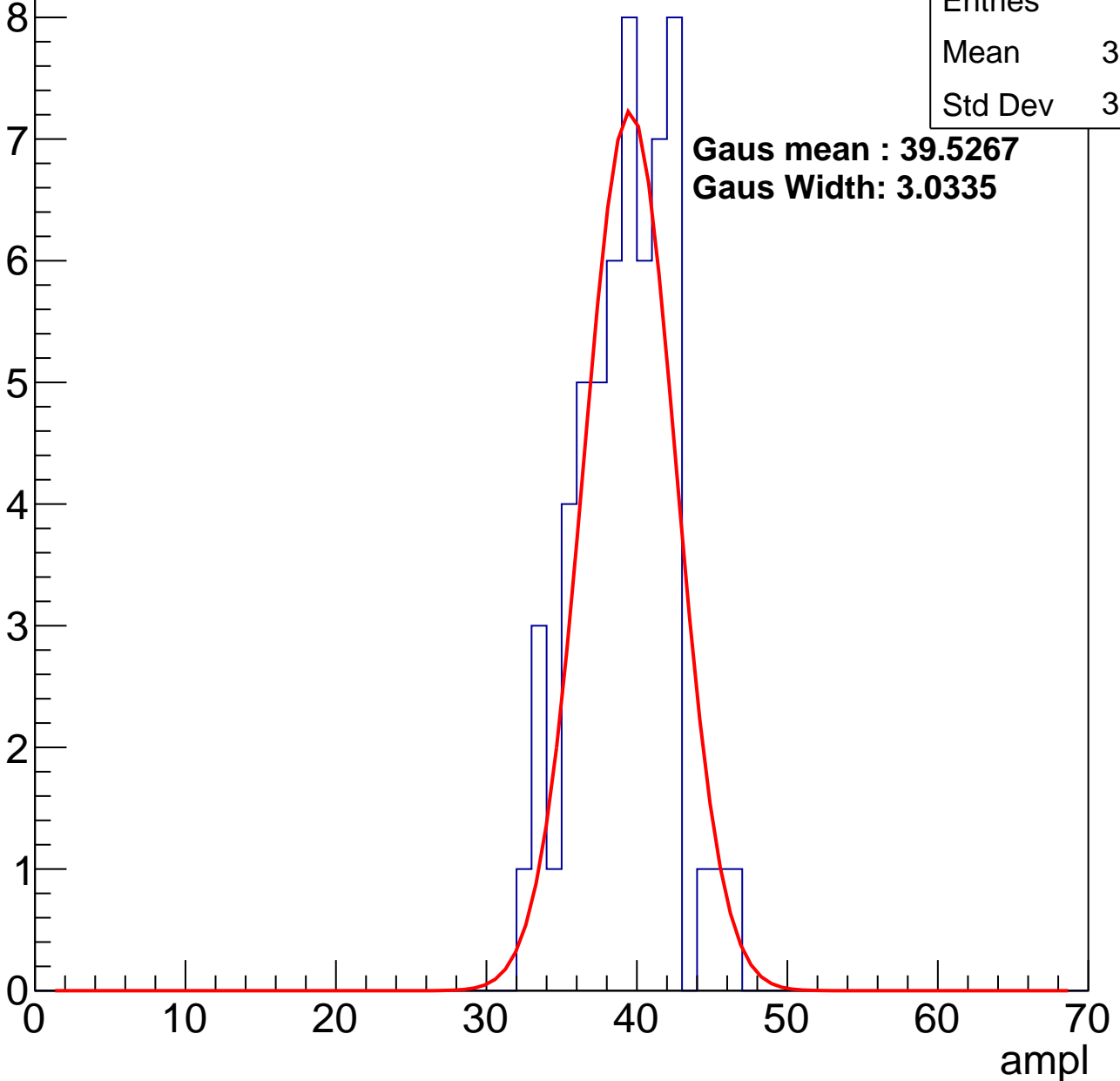
# B1L101S, U11-ch39, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	38.74
Std Dev	3.047

**Gaus mean : 39.5267**  
**Gaus Width: 3.0335**



# B1L101S, U11-ch39, adc2

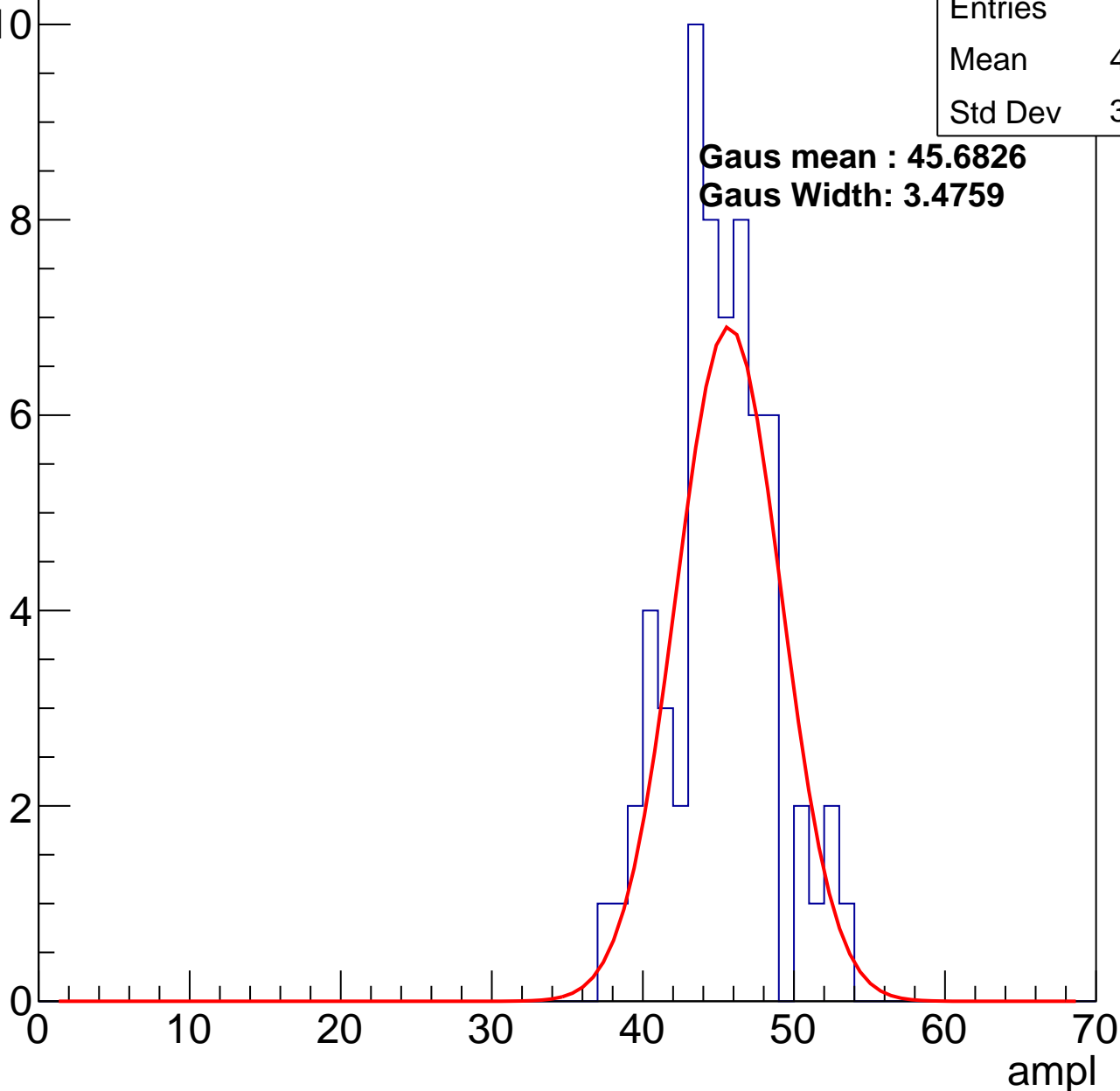
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	44.73
Std Dev	3.374

**Gaus mean : 45.6826**

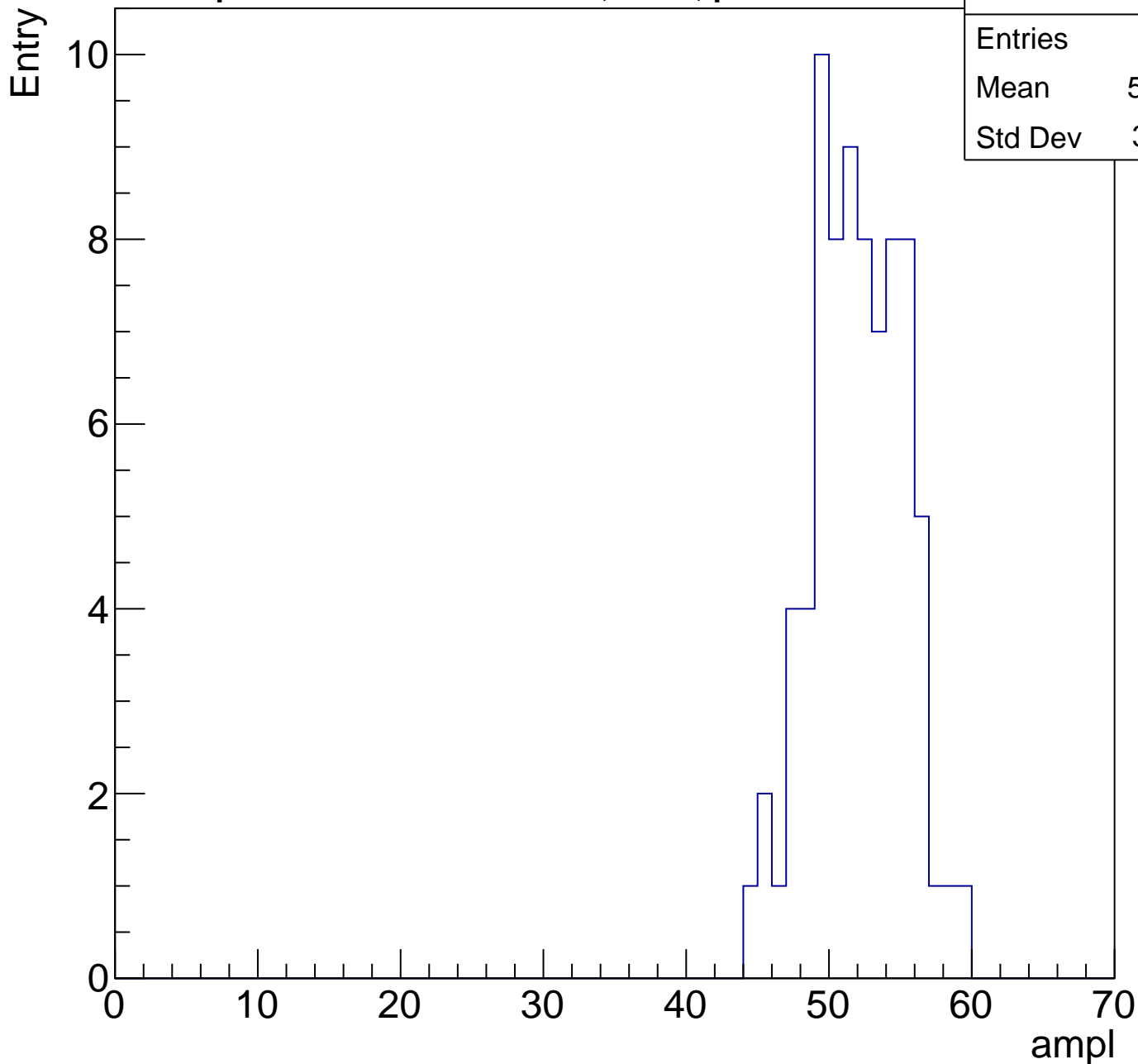
**Gaus Width: 3.4759**



# B1L101S, U11-ch39, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

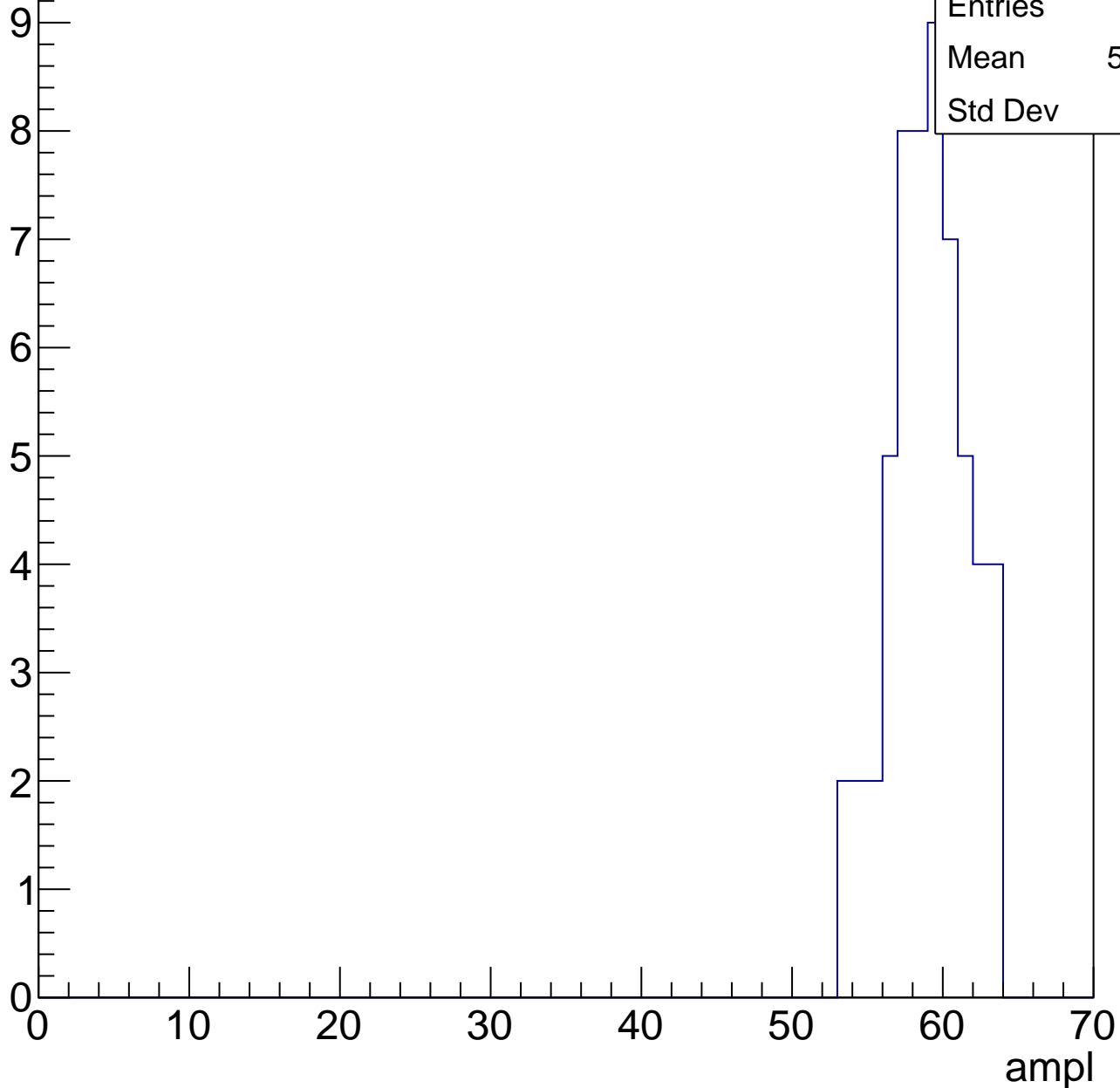
Entries	78
Mean	51.56
Std Dev	3.161



# B1L101S, U11-ch39, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

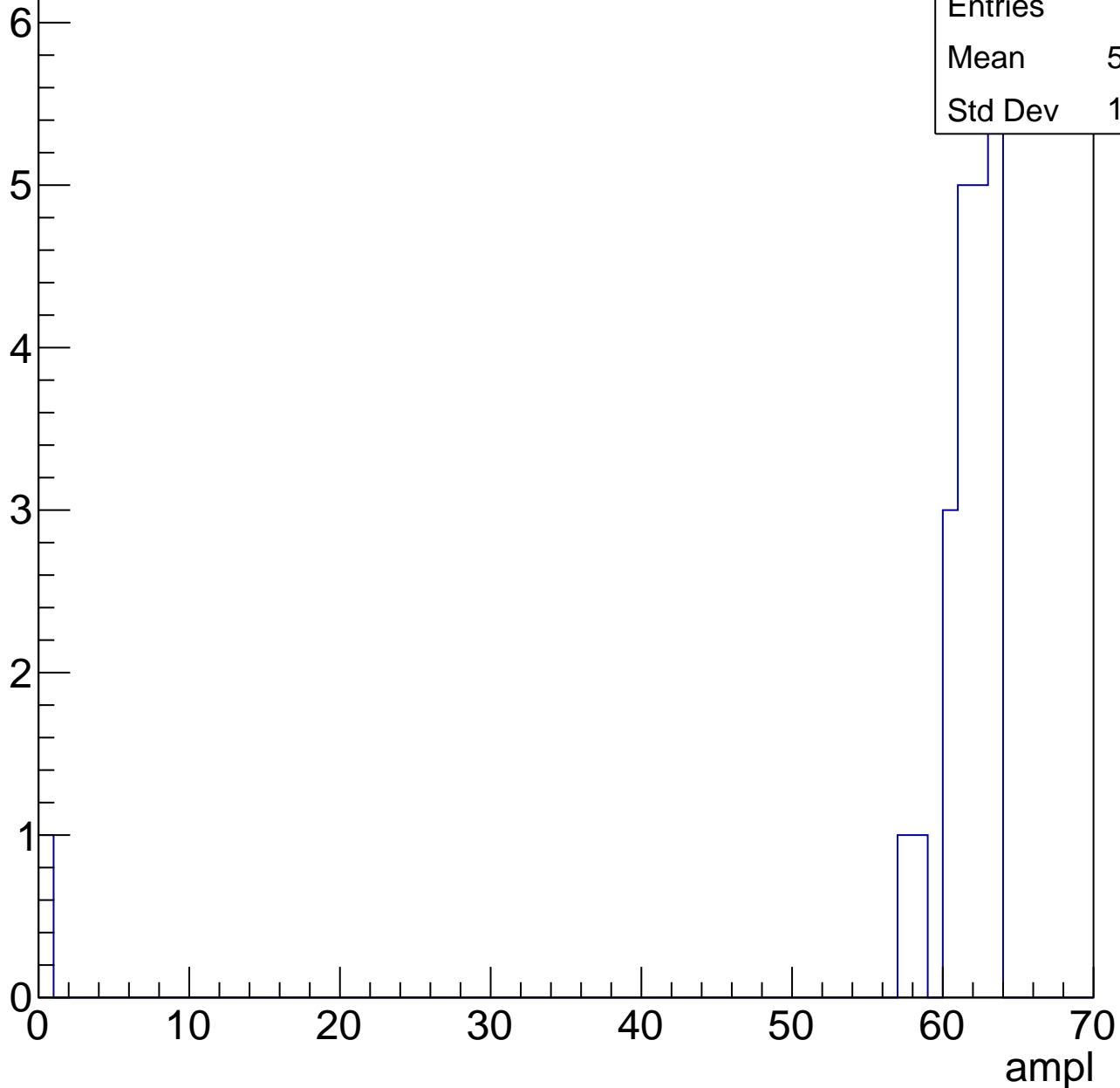


Entries	56
Mean	58.57
Std Dev	2.52

# B1L101S, U11-ch39, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	22
Mean	58.55
Std Dev	12.87

# B1L101S, U11-ch39, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch39, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U11-ch40, adc0

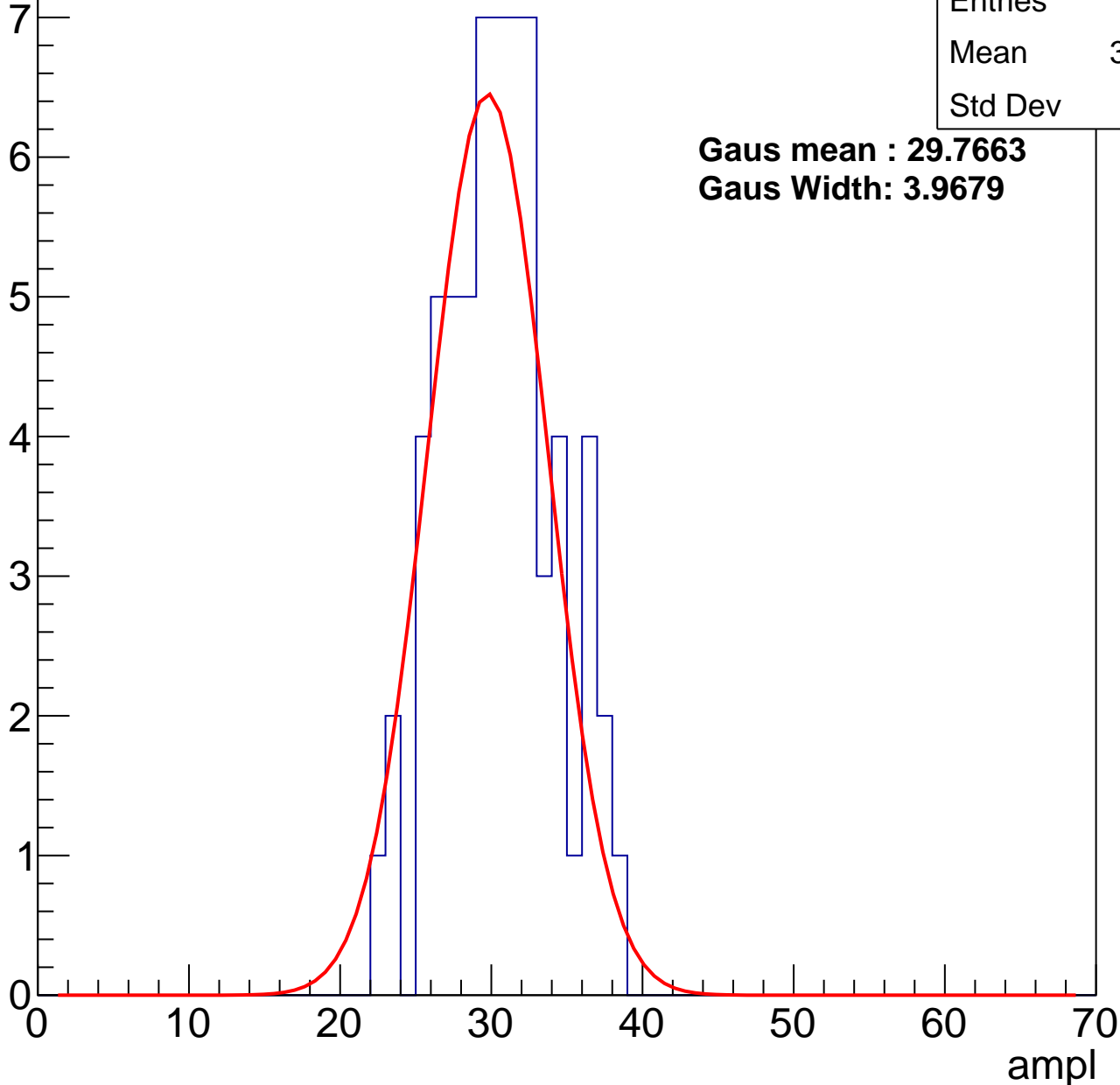
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	30.05
Std Dev	3.66

**Gaus mean : 29.7663**

**Gaus Width: 3.9679**



# B1L101S, U11-ch40, adc1

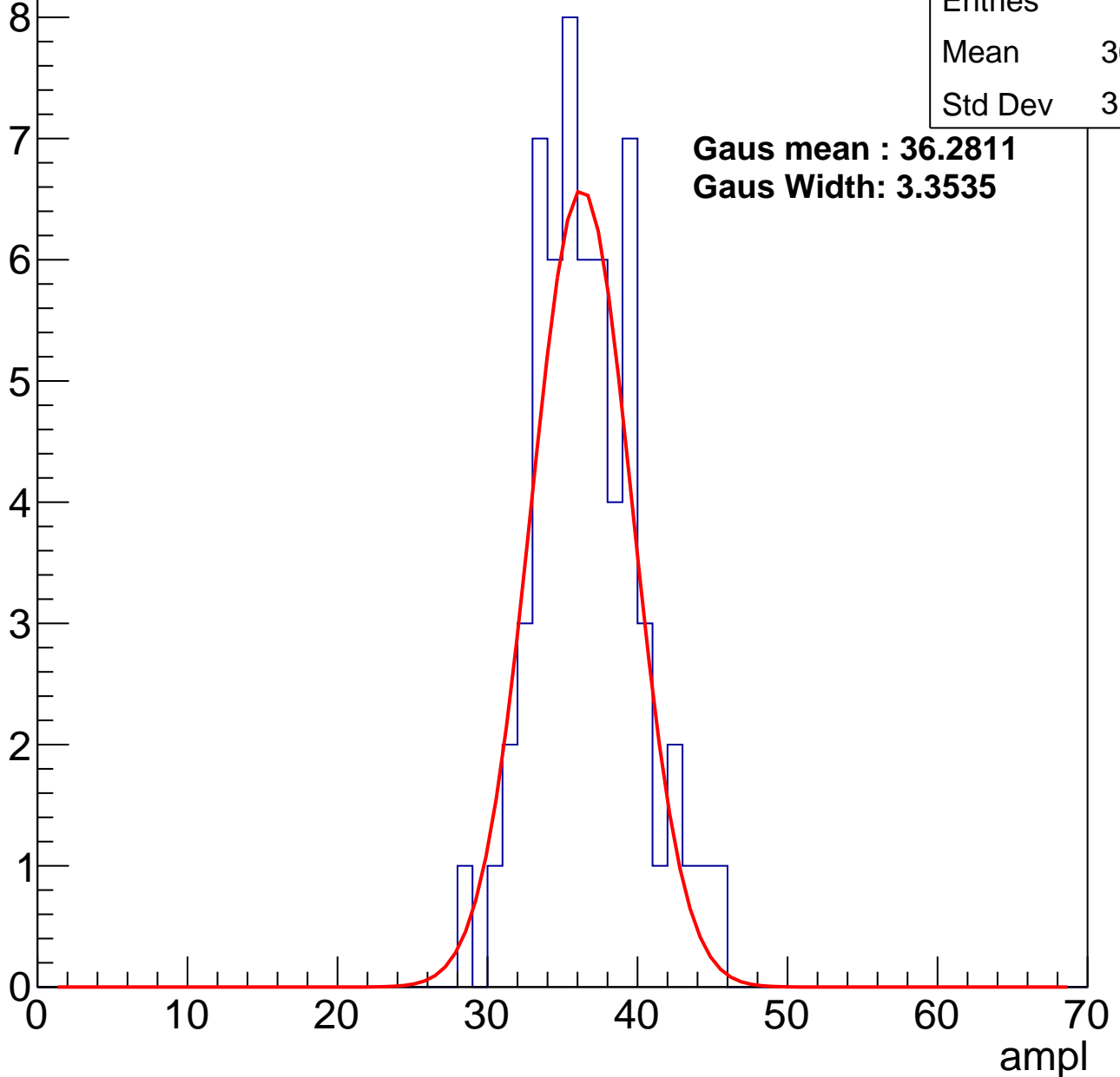
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	36.18
Std Dev	3.452

**Gaus mean : 36.2811**

**Gaus Width: 3.3535**



# B1L101S, U11-ch40, adc2

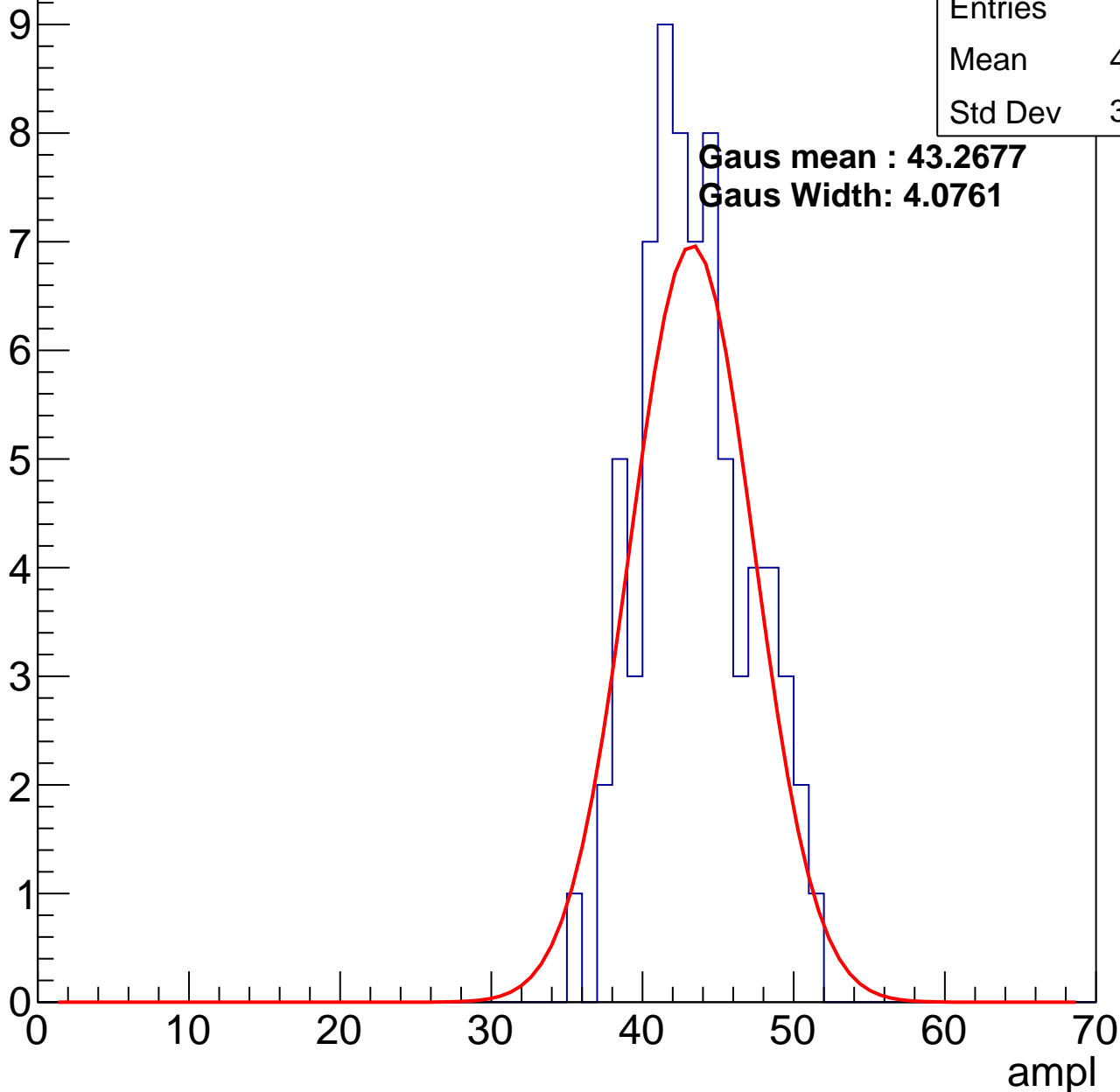
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	42.99
Std Dev	3.545

**Gaus mean : 43.2677**

**Gaus Width: 4.0761**

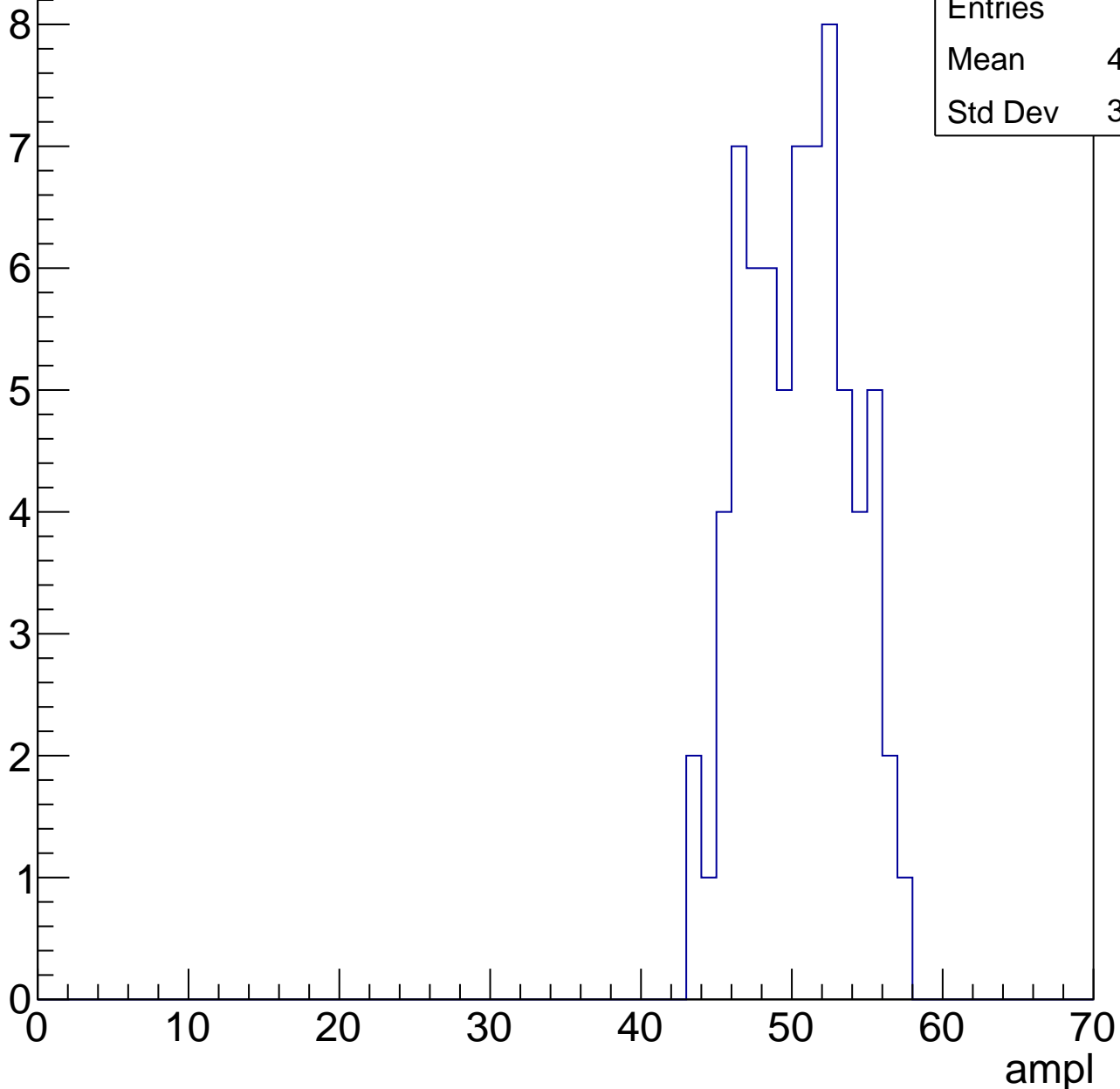


# B1L101S, U11-ch40, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	49.93
Std Dev	3.428

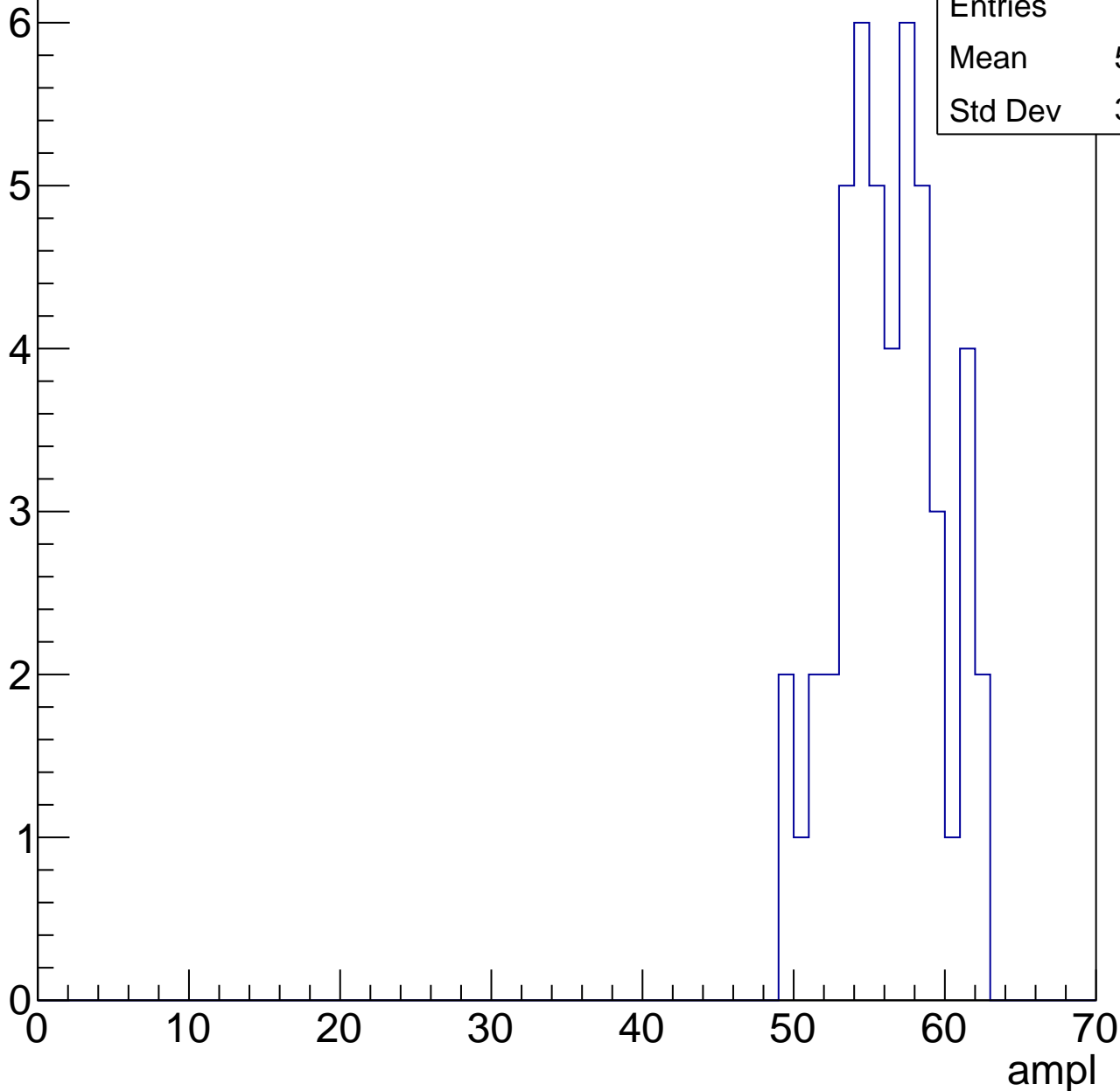


# B1L101S, U11-ch40, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	48
Mean	55.81
Std Dev	3.321



# B1L101S, U11-ch40, adc5

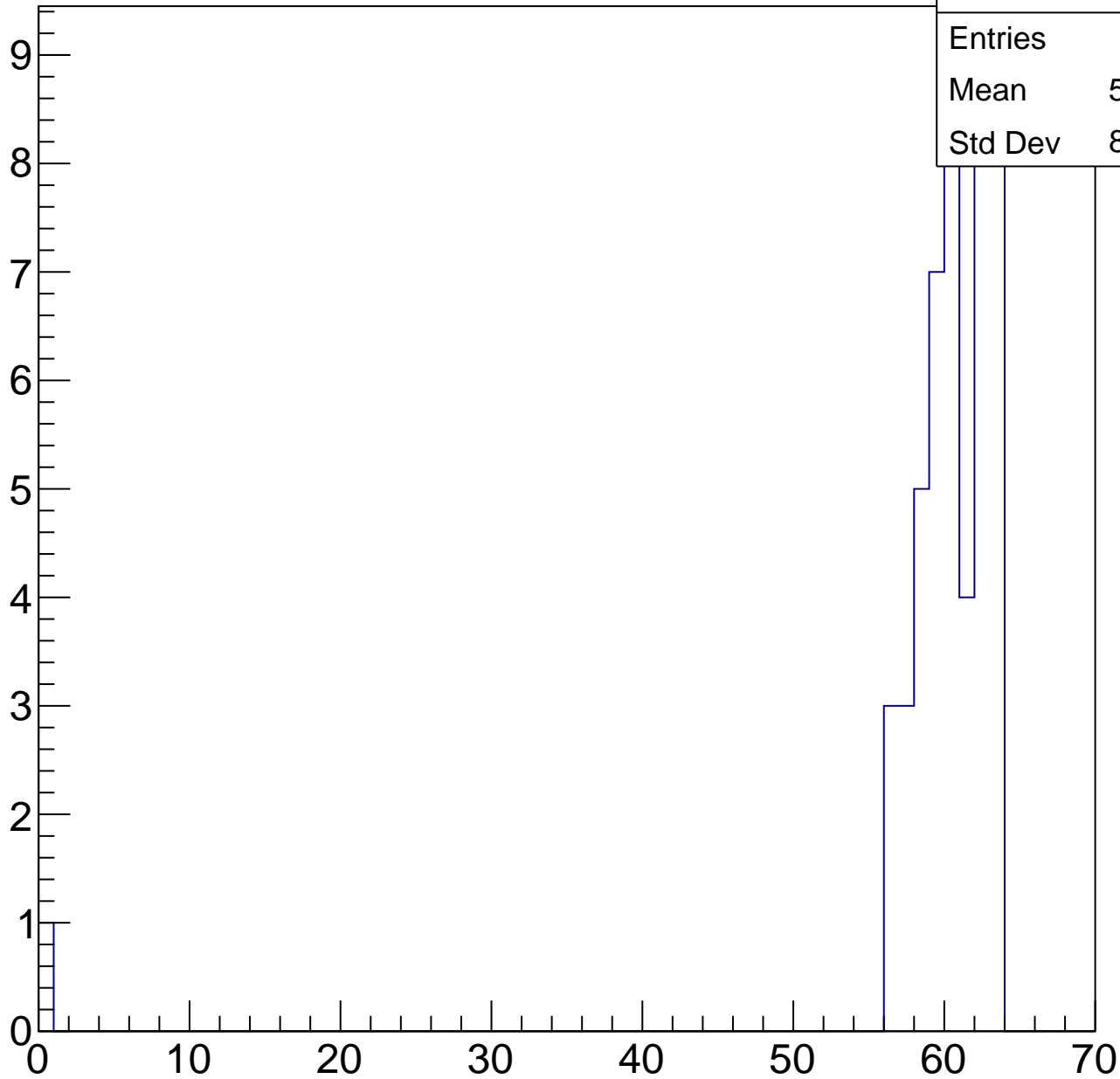
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	48
Mean	58.94
Std Dev	8.856

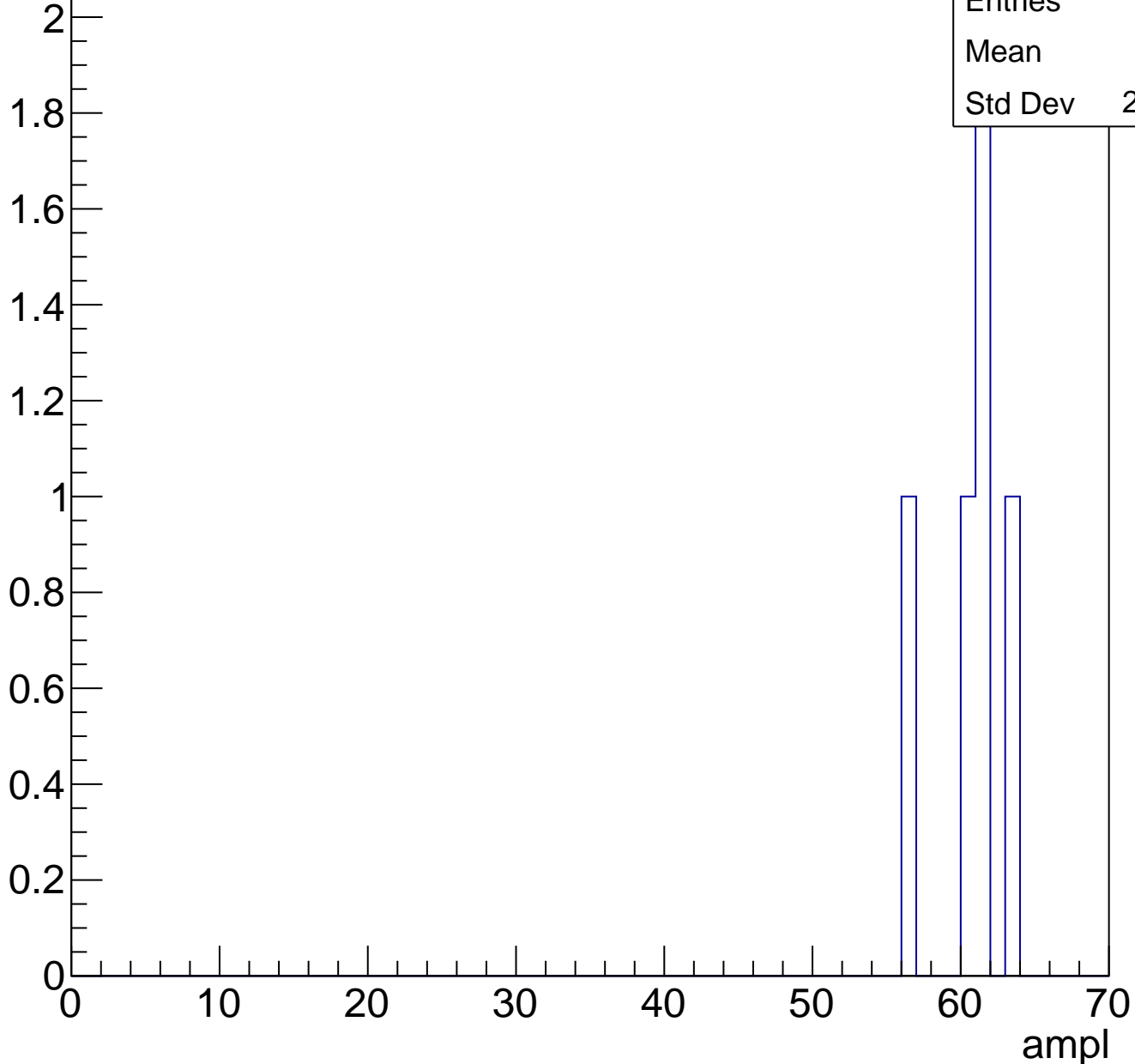
ampl



# B1L101S, U11-ch40, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch40, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U11-ch41, adc0

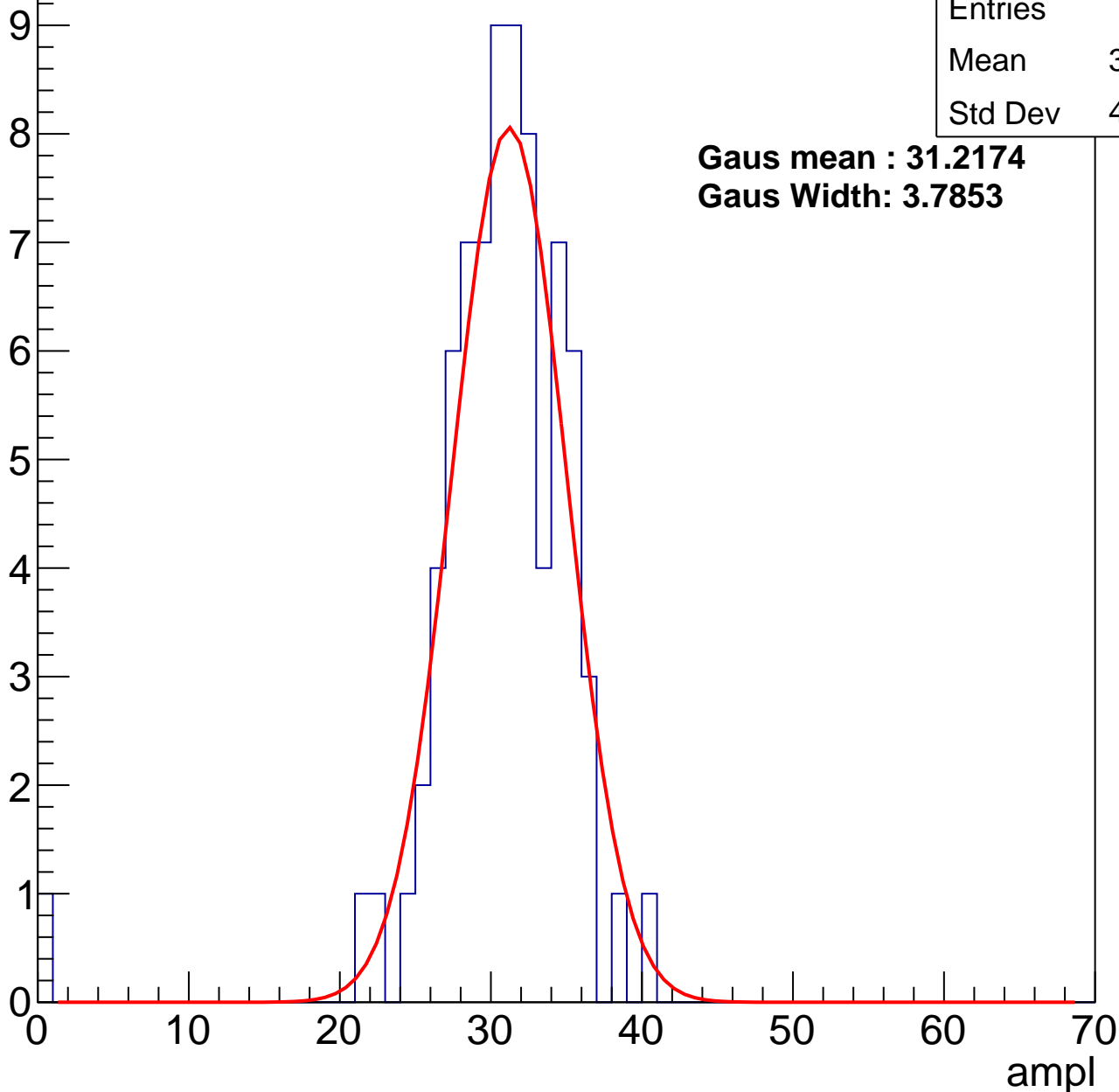
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	78
Mean	30.17
Std Dev	4.926

**Gaus mean : 31.2174**

**Gaus Width: 3.7853**



# B1L101S, U11-ch41, adc1

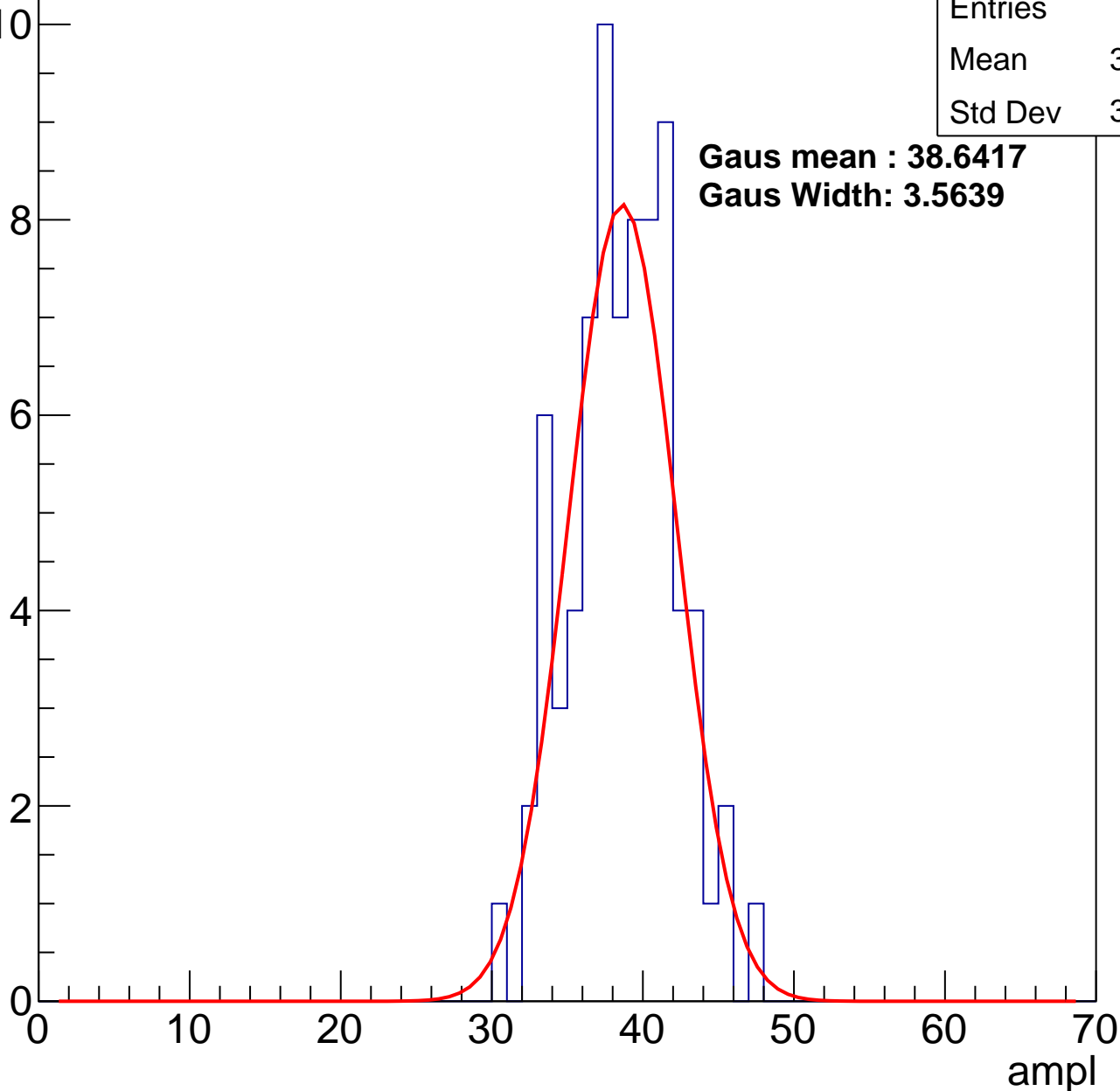
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	38.23
Std Dev	3.426

**Gaus mean : 38.6417**

**Gaus Width: 3.5639**



# B1L101S, U11-ch41, adc2

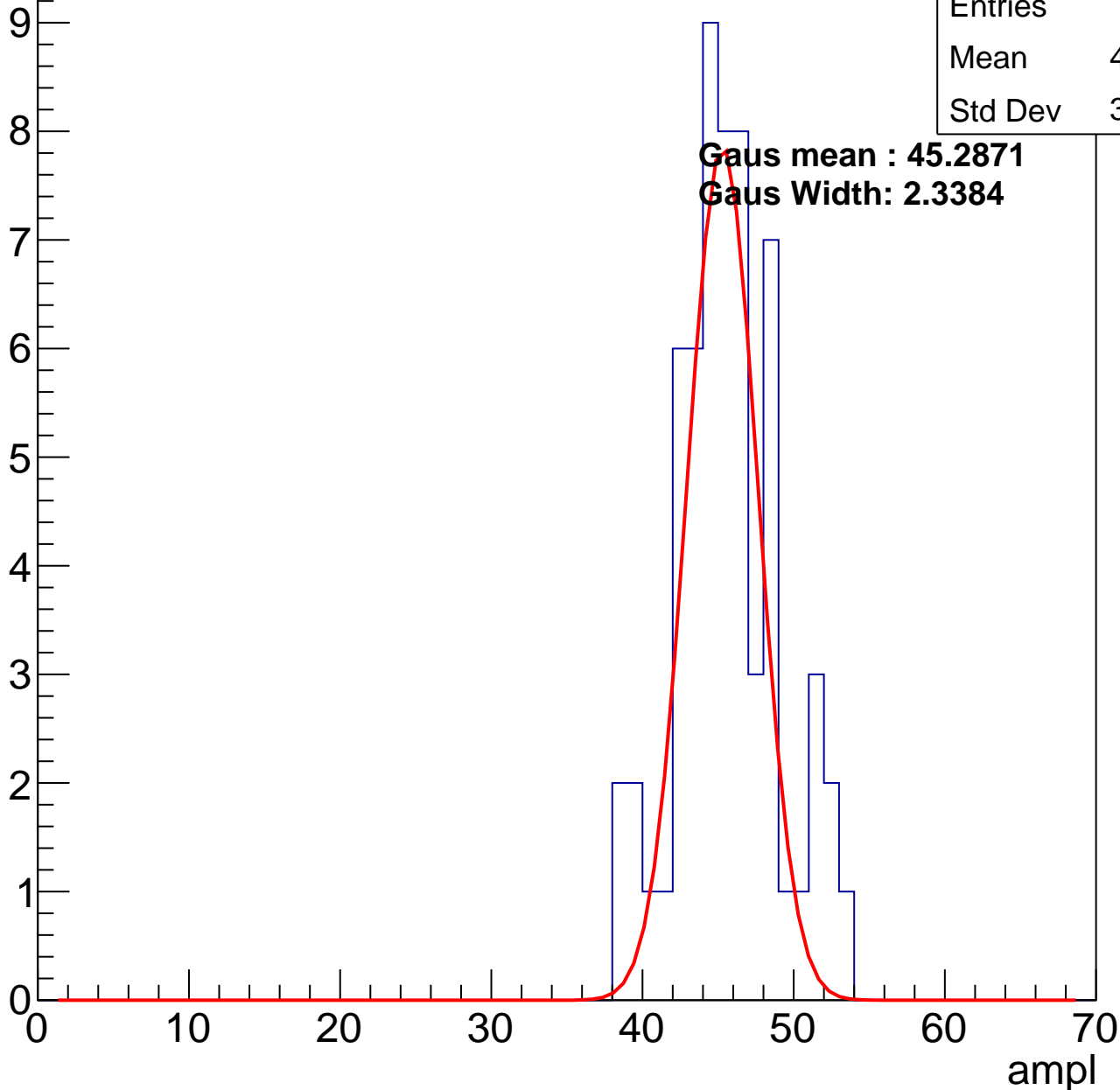
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	45.16
Std Dev	3.364

**Gaus mean : 45.2871**

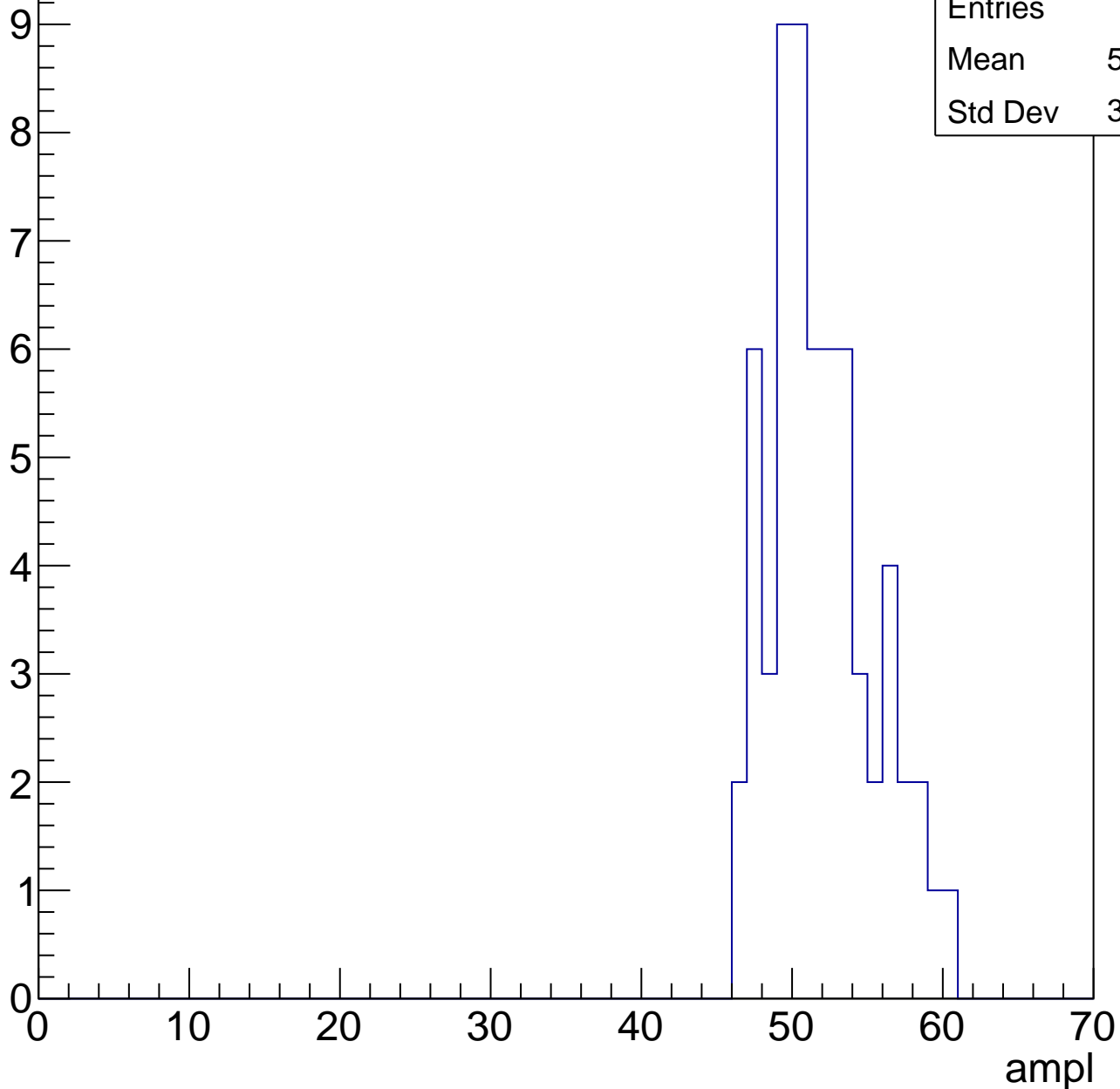
**Gaus Width: 2.3384**



# B1L101S, U11-ch41, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

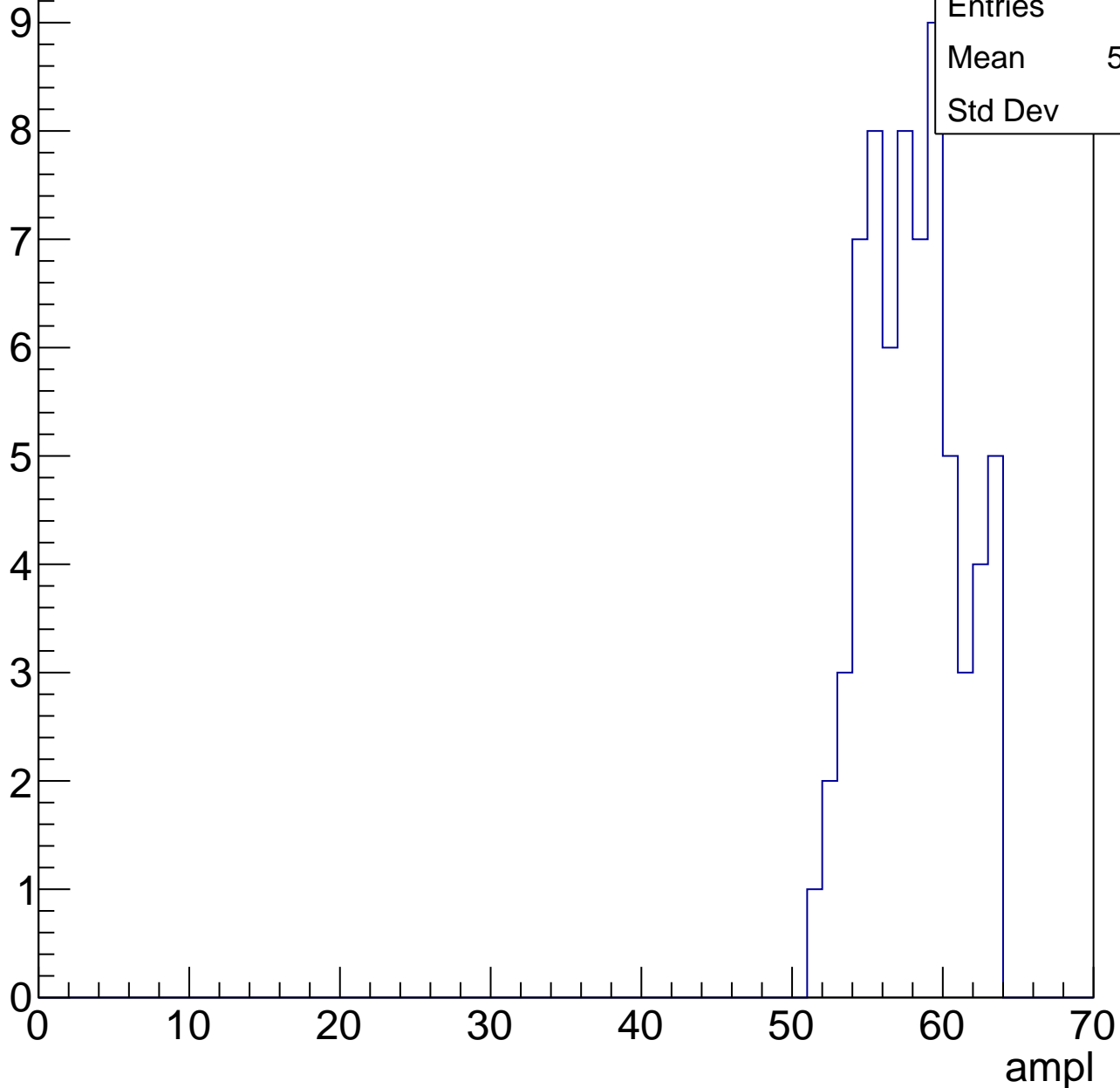
Entry



# B1L101S, U11-ch41, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



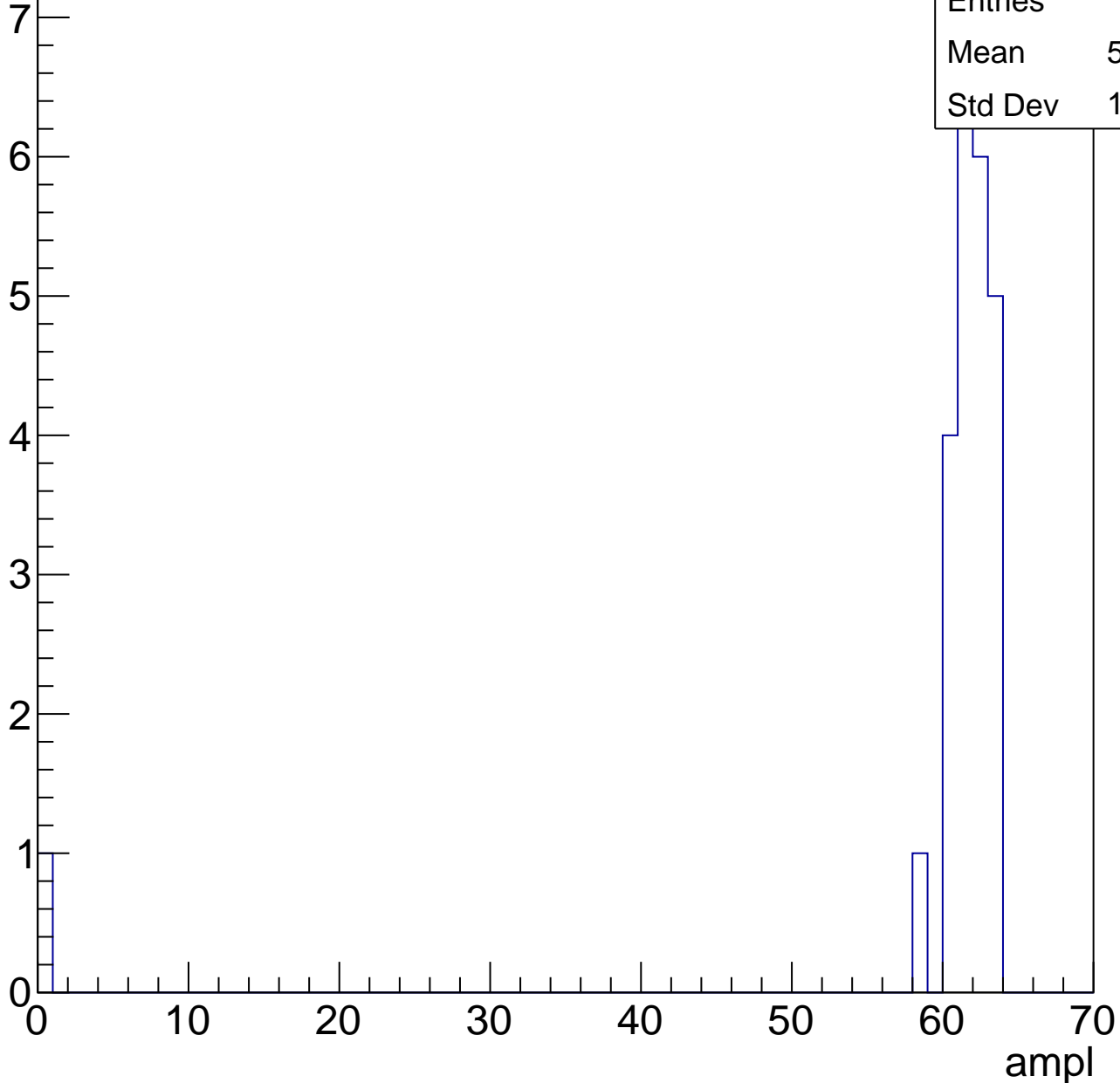
Entries	68
Mean	57.46
Std Dev	3.06

# B1L101S, U11-ch41, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	24
Mean	58.83
Std Dev	12.33



# B1L101S, U11-ch41, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L101S, U11-ch41, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U11-ch42, adc0

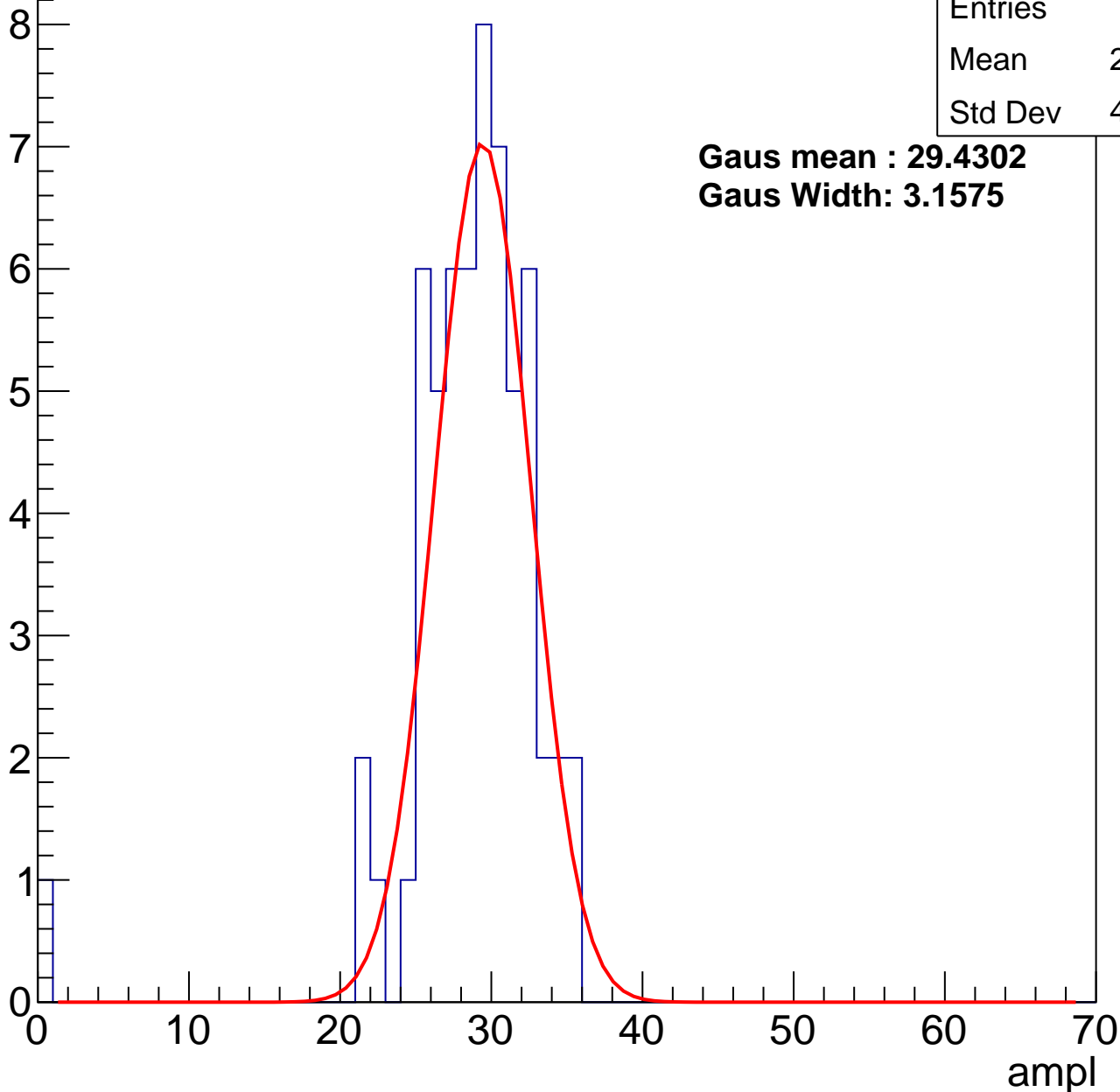
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	28.18
Std Dev	4.846

**Gaus mean : 29.4302**

**Gaus Width: 3.1575**



# B1L101S, U11-ch42, adc1

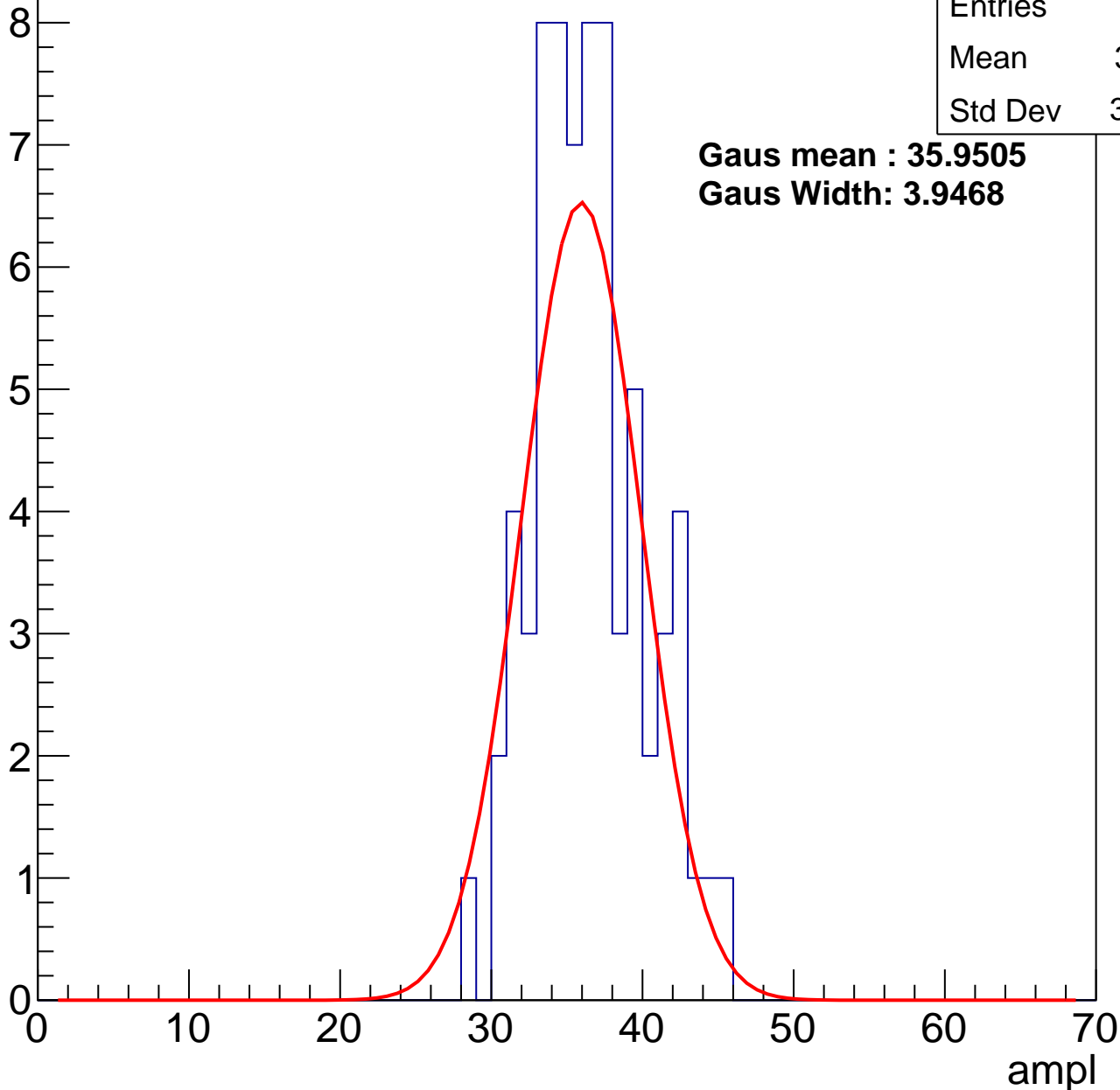
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	36.01
Std Dev	3.622

**Gaus mean : 35.9505**

**Gaus Width: 3.9468**



# B1L101S, U11-ch42, adc2

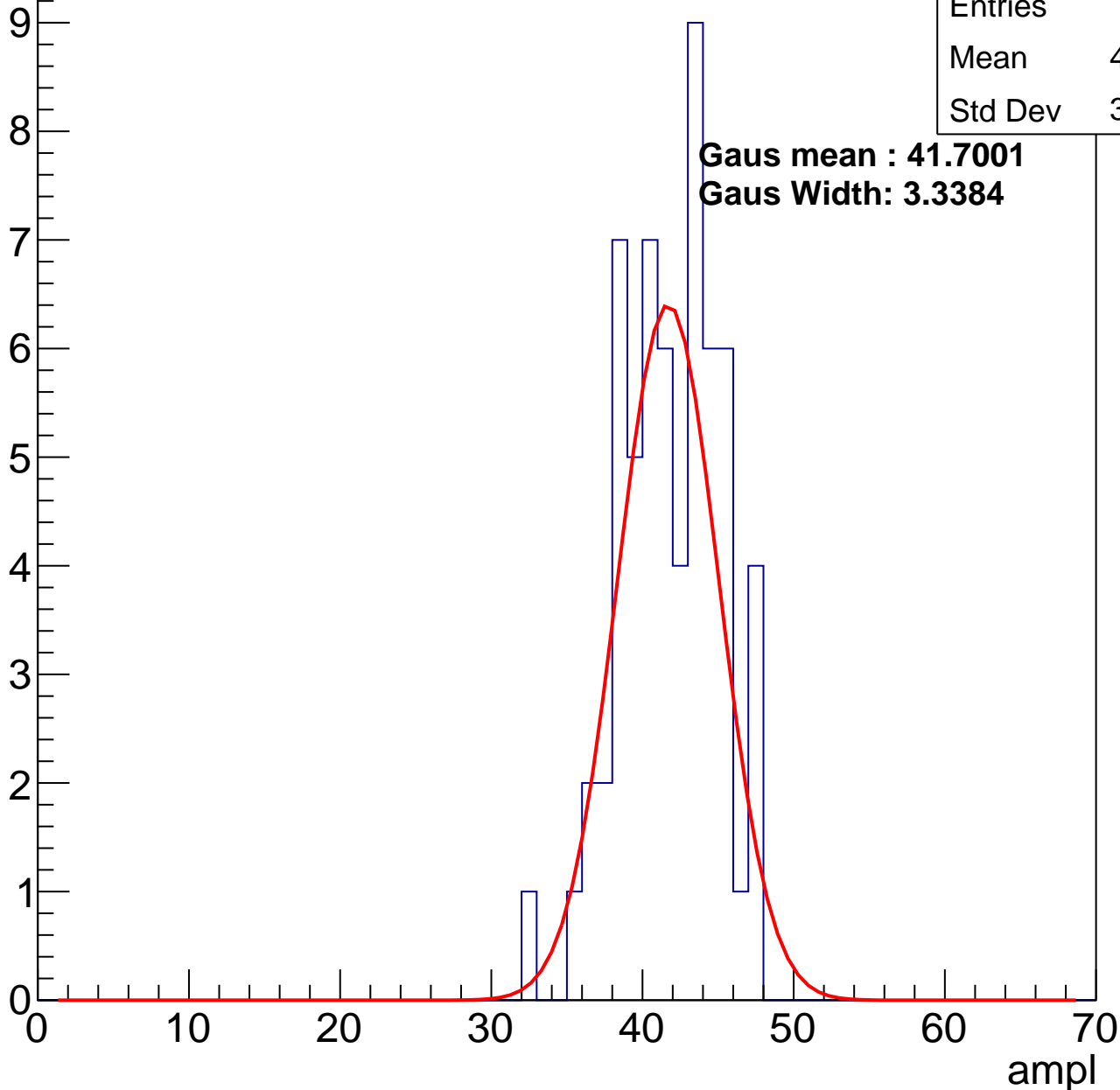
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	41.36
Std Dev	3.239

**Gaus mean : 41.7001**

**Gaus Width: 3.3384**

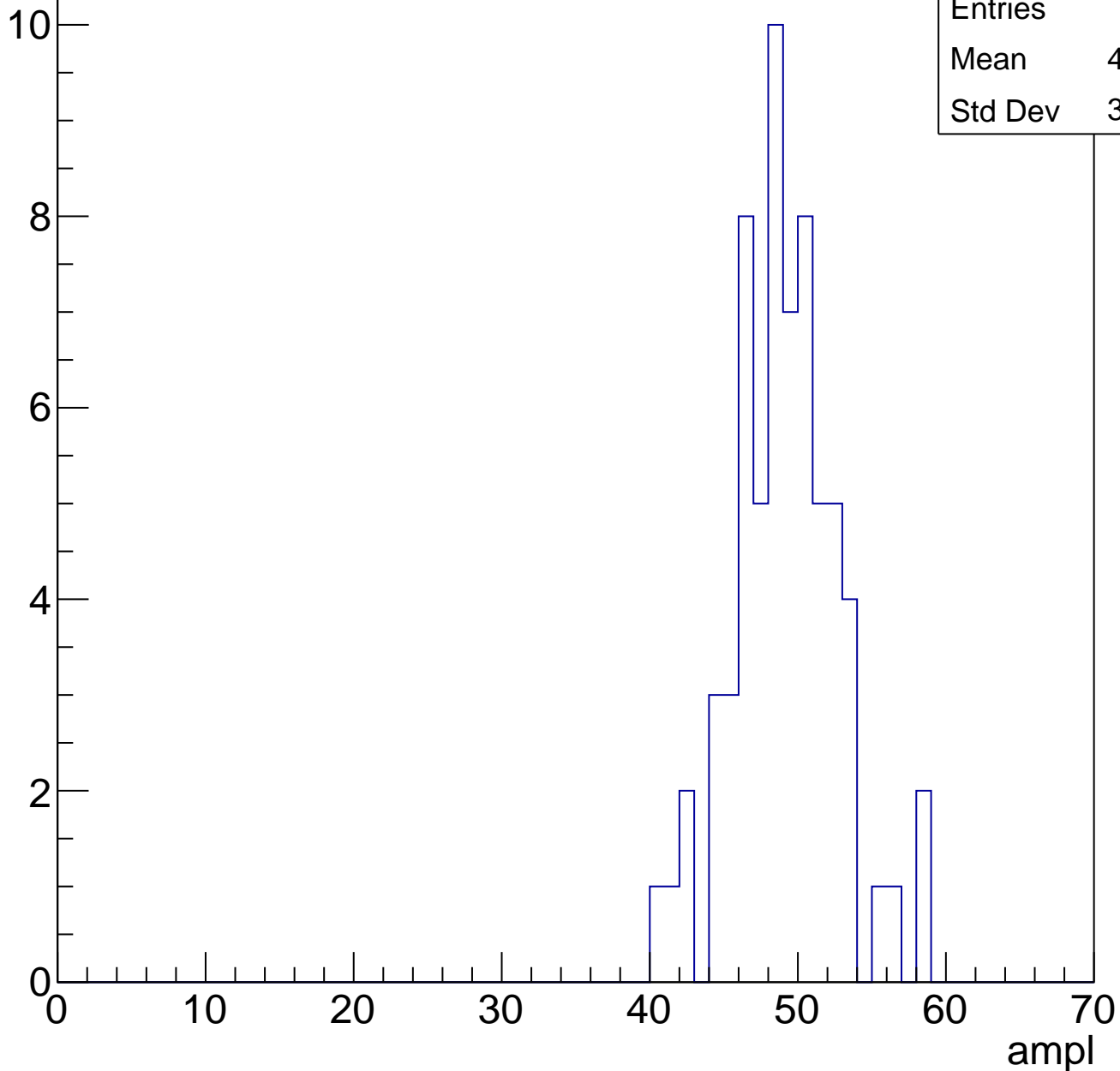


# B1L101S, U11-ch42, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	66
Mean	48.67
Std Dev	3.577

Entry

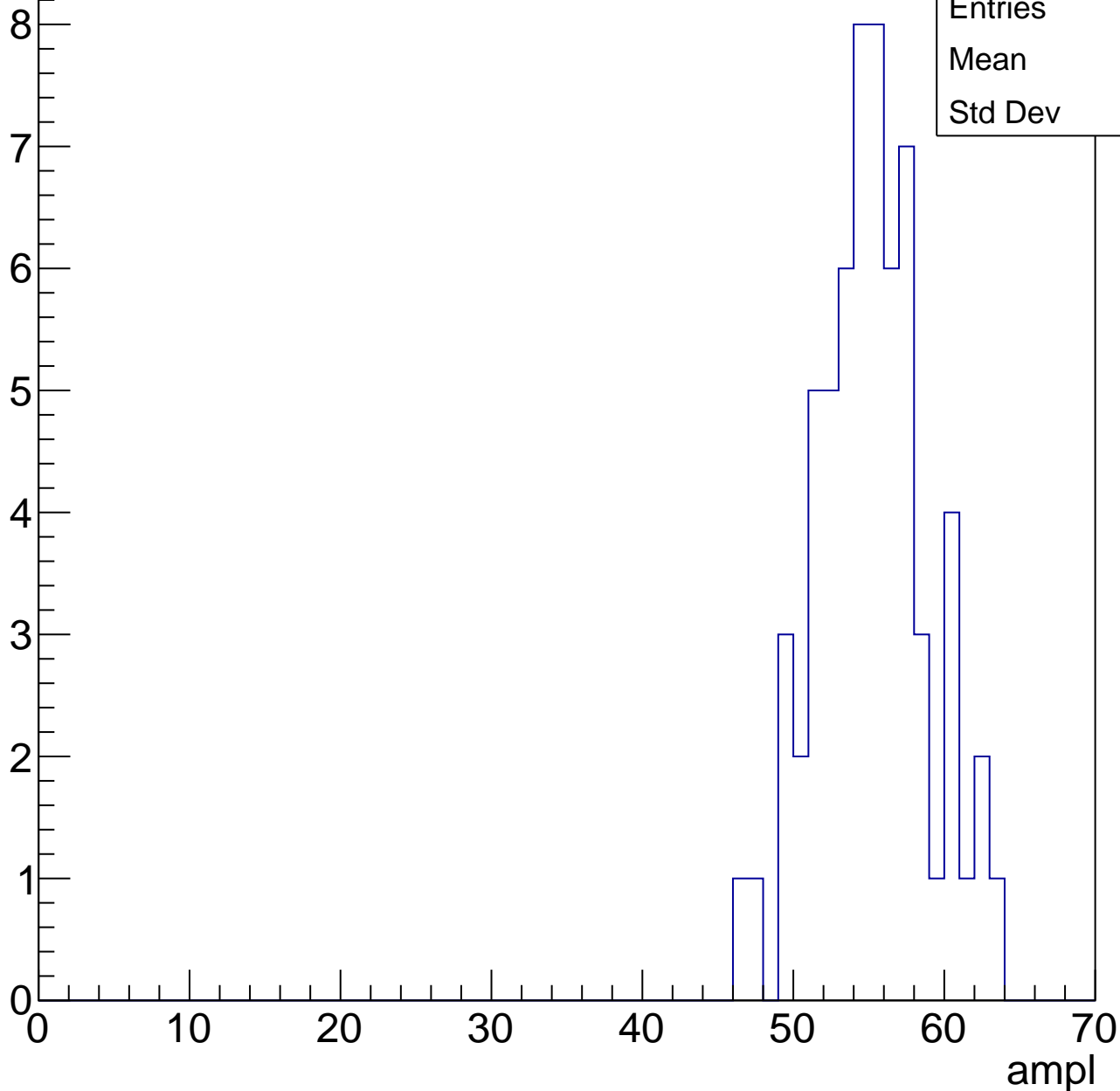


# B1L101S, U11-ch42, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	54.7
Std Dev	3.6

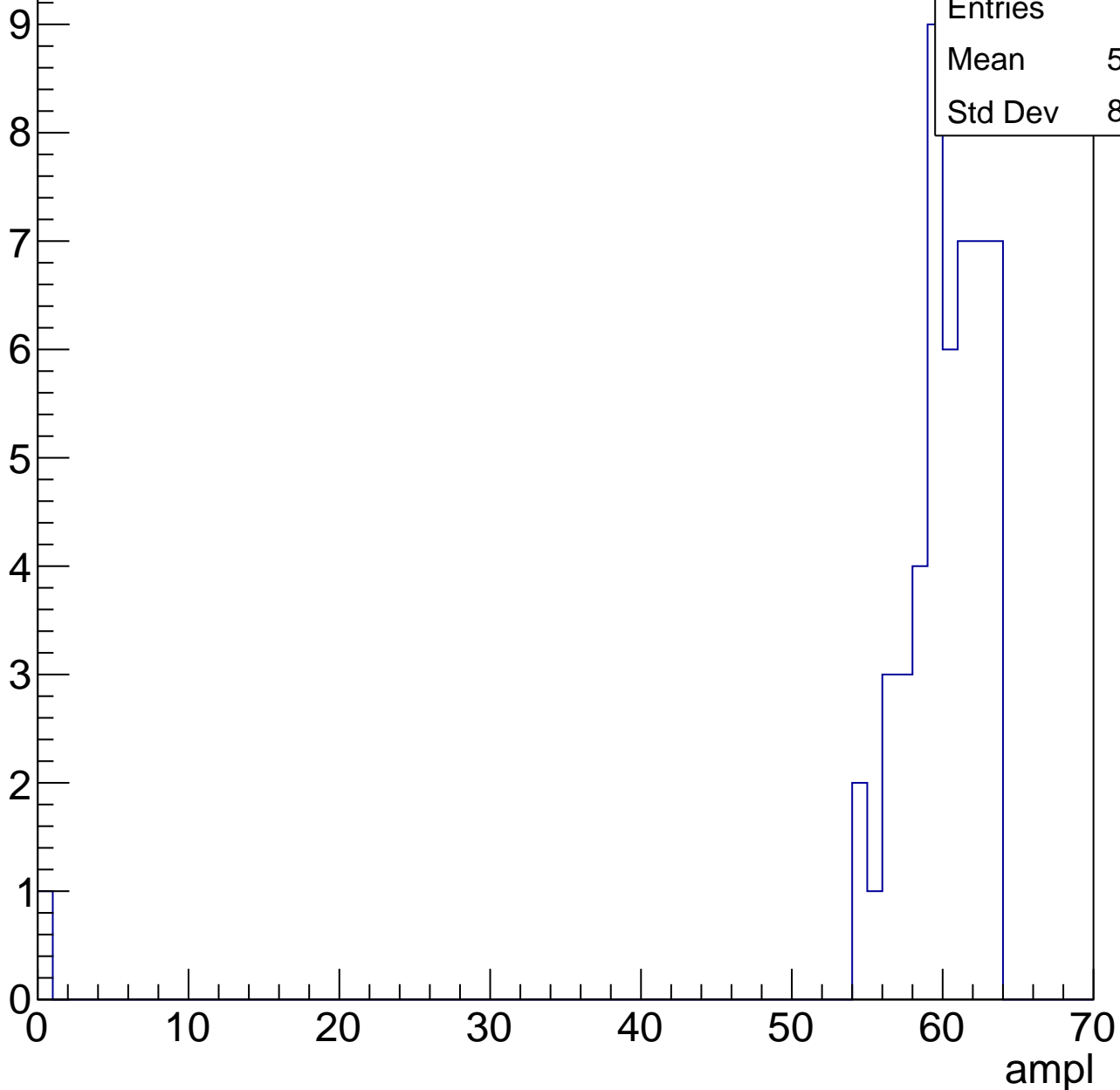


# B1L101S, U11-ch42, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

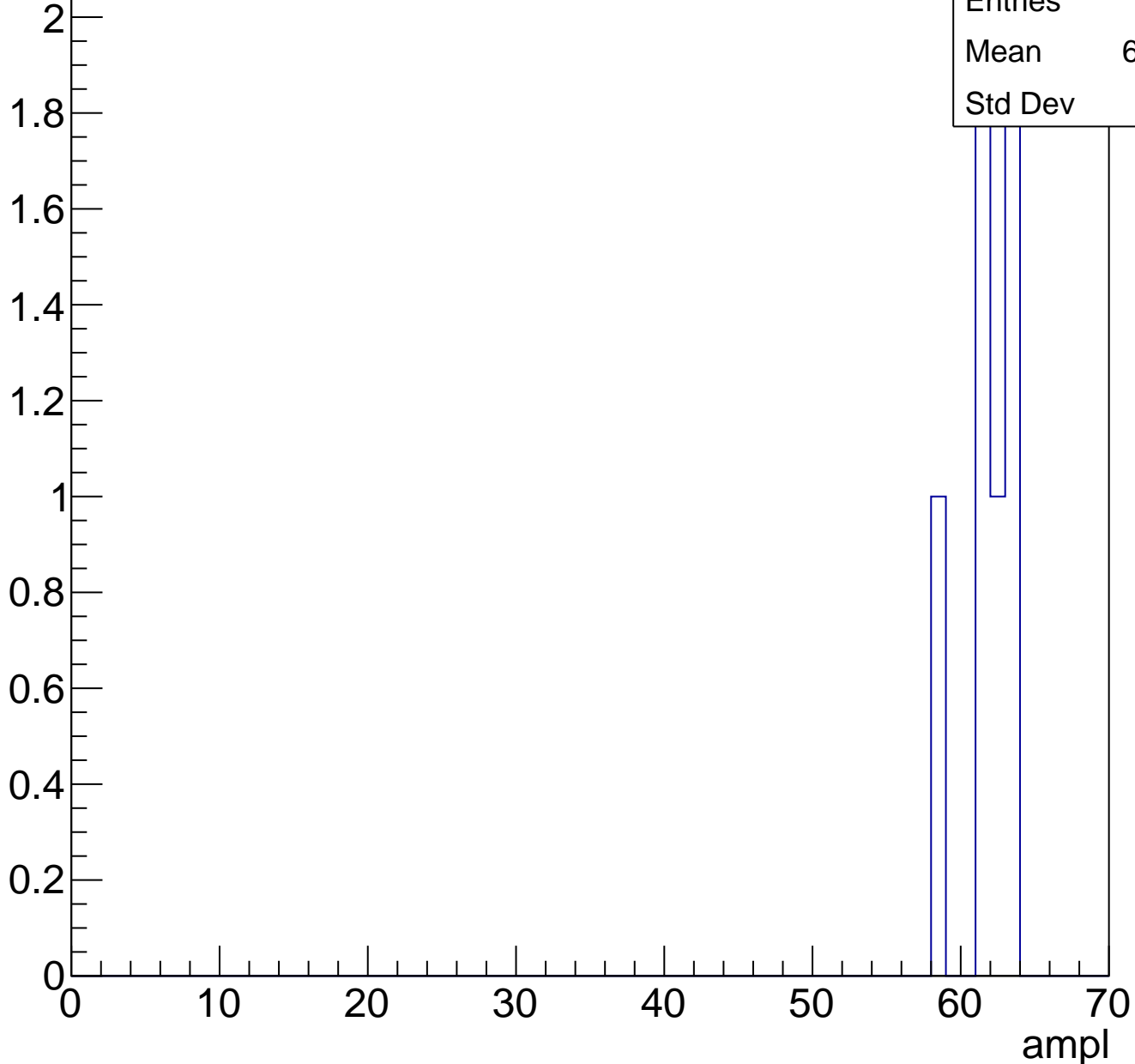
Entries	50
Mean	58.54
Std Dev	8.705



# B1L101S, U11-ch42, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch42, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U11-ch43, adc0

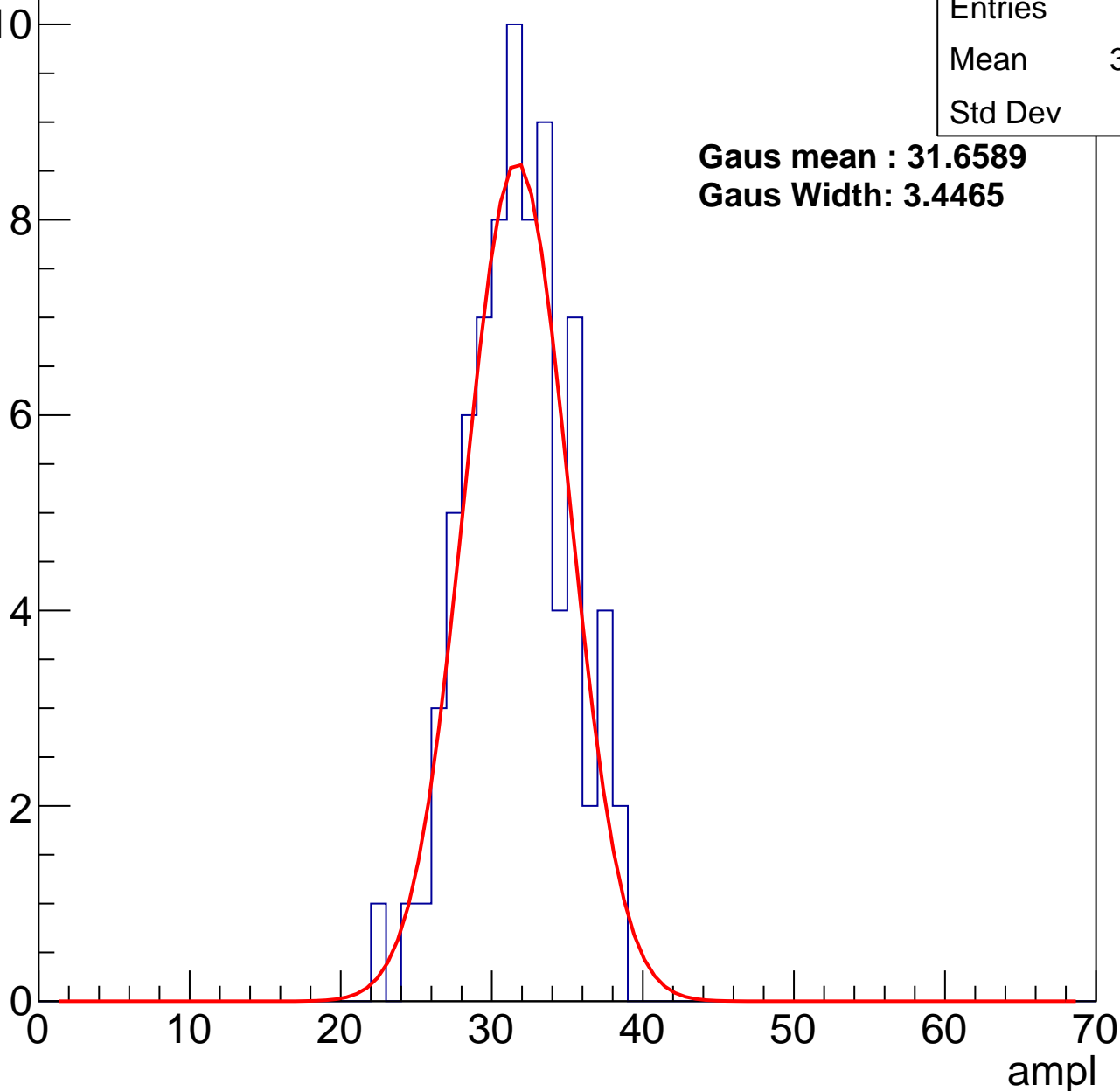
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	78
Mean	31.22
Std Dev	3.38

**Gaus mean : 31.6589**

**Gaus Width: 3.4465**



# B1L101S, U11-ch43, adc1

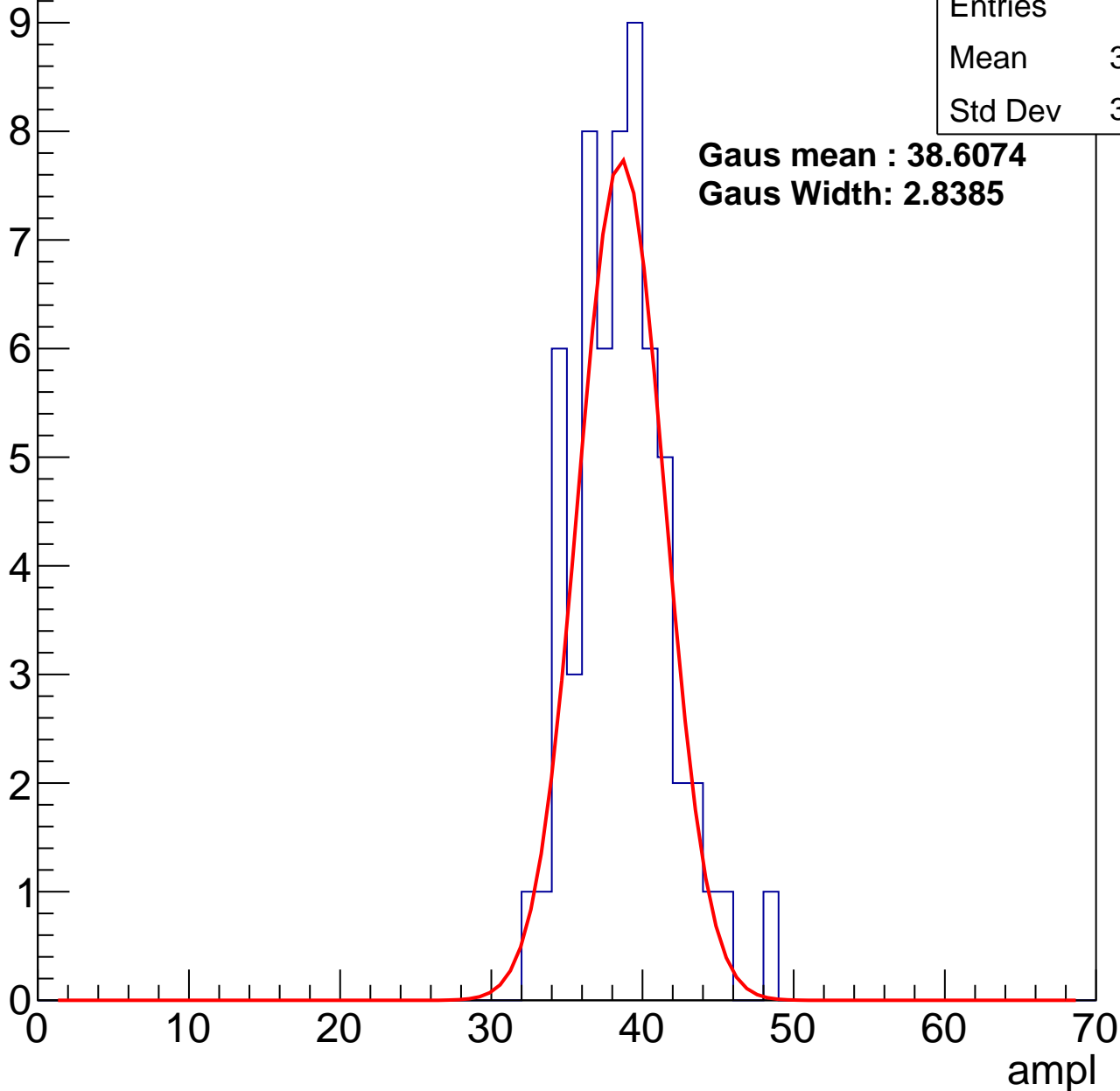
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	38.18
Std Dev	3.069

**Gaus mean : 38.6074**

**Gaus Width: 2.8385**



# B1L101S, U11-ch43, adc2

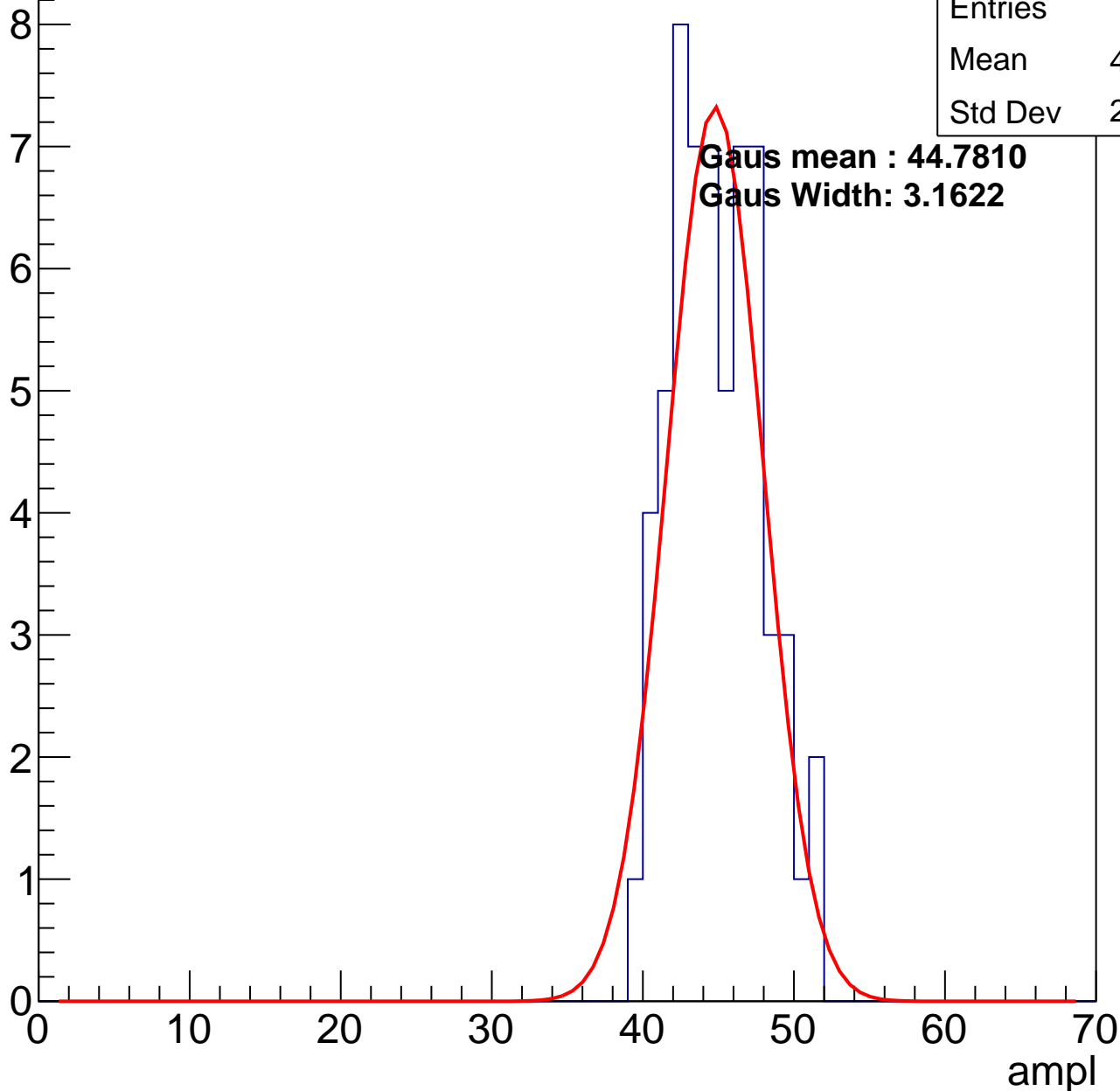
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	44.47
Std Dev	2.924

**Gaus mean : 44.7810**

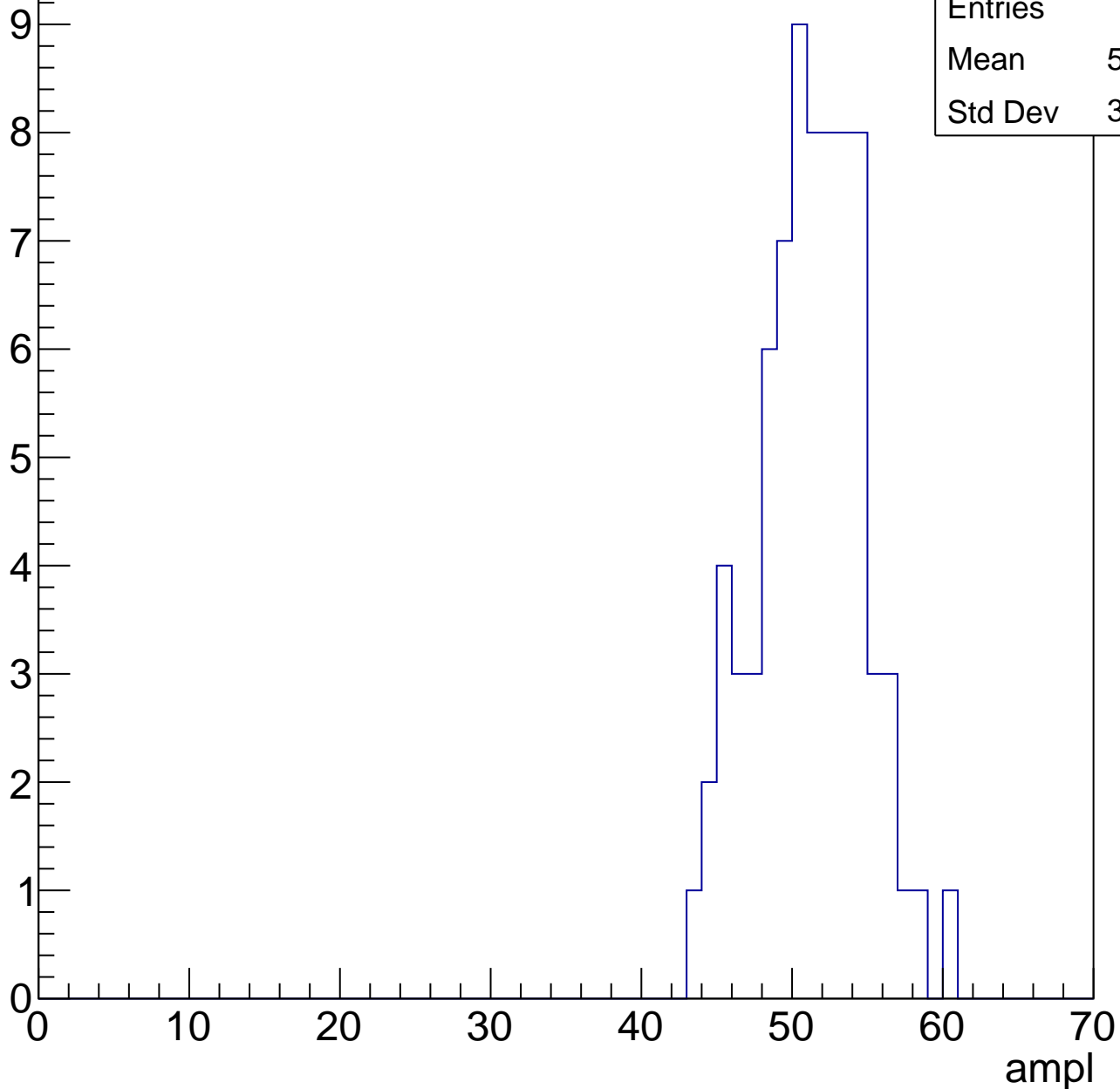
**Gaus Width: 3.1622**



# B1L101S, U11-ch43, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

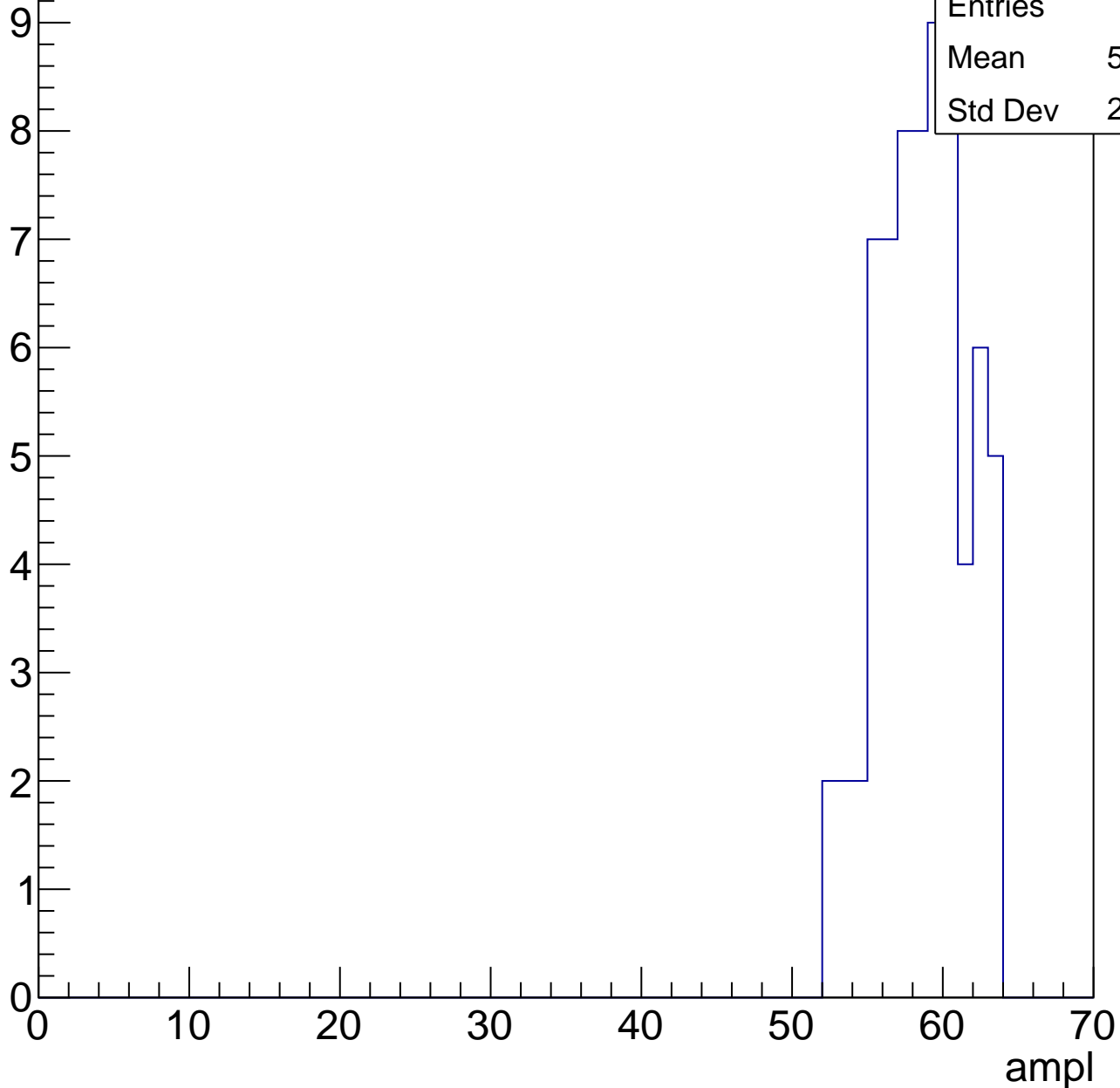
Entry



# B1L101S, U11-ch43, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

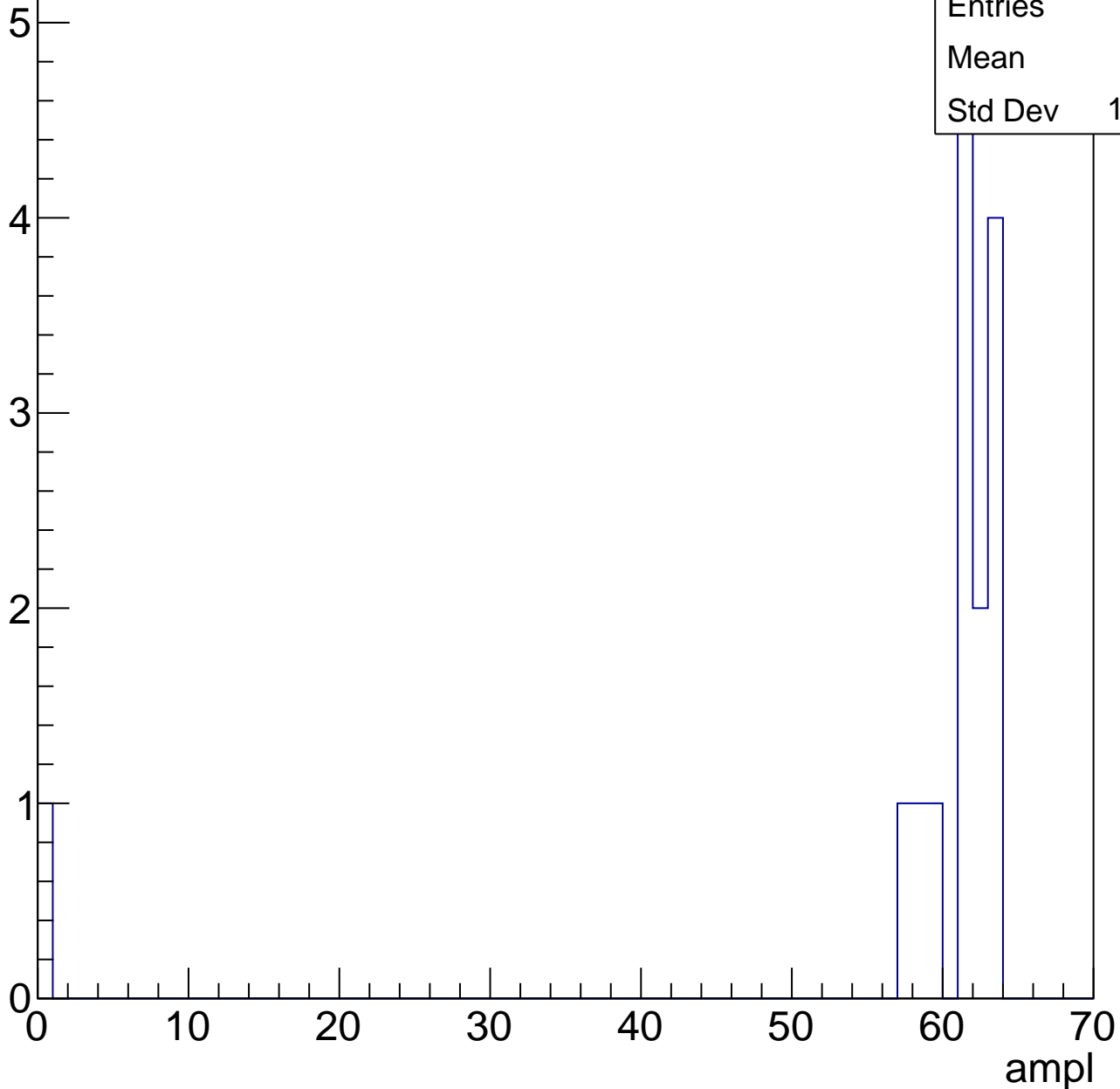


# B1L101S, U11-ch43, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	15
Mean	57
Std Dev	15.34



# B1L101S, U11-ch43, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

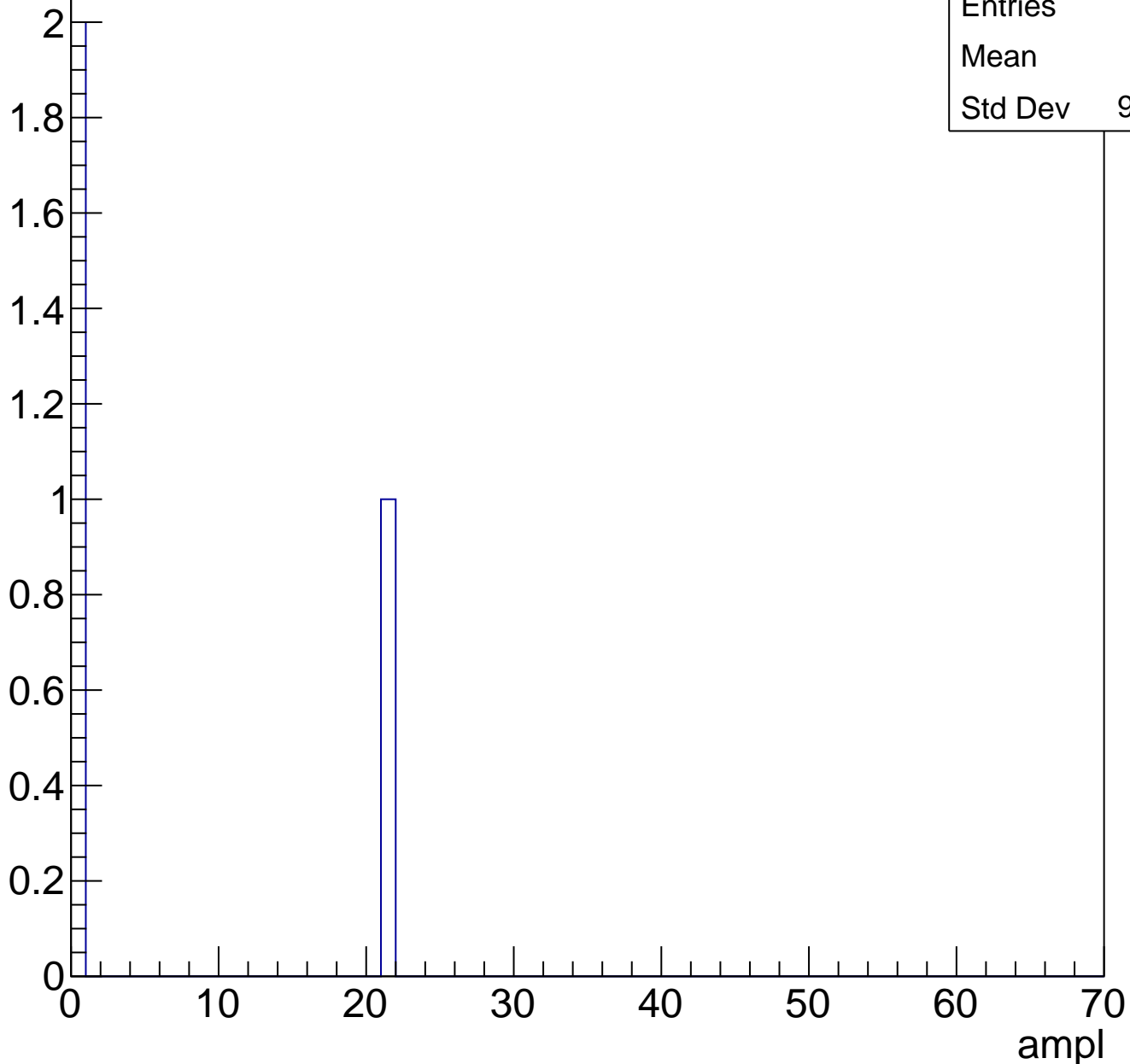




# B1L101S, U11-ch43, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	7
Std Dev	9.899

# B1L101S, U11-ch44, adc0

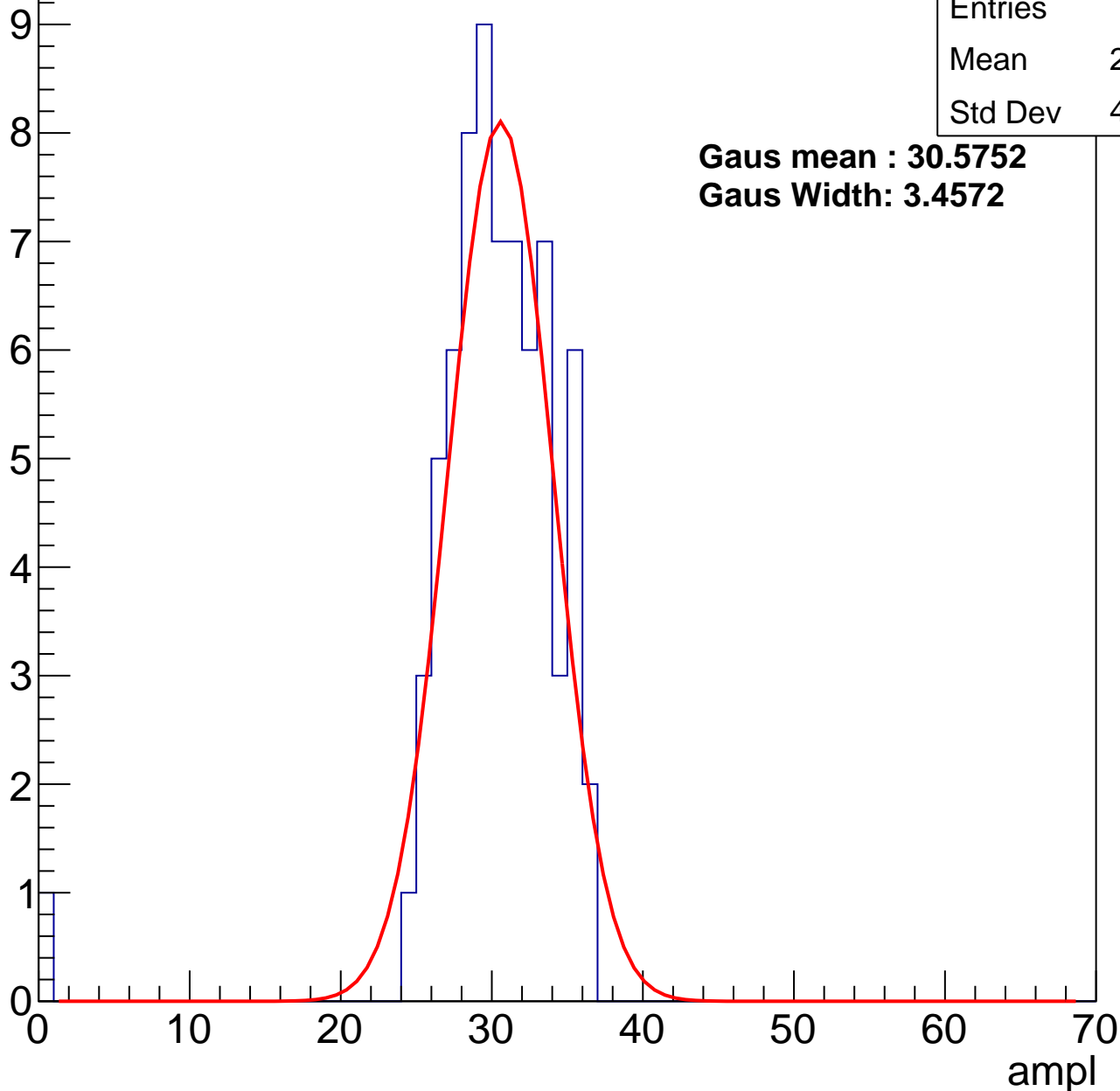
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	29.72
Std Dev	4.664

**Gaus mean : 30.5752**

**Gaus Width: 3.4572**



# B1L101S, U11-ch44, adc1

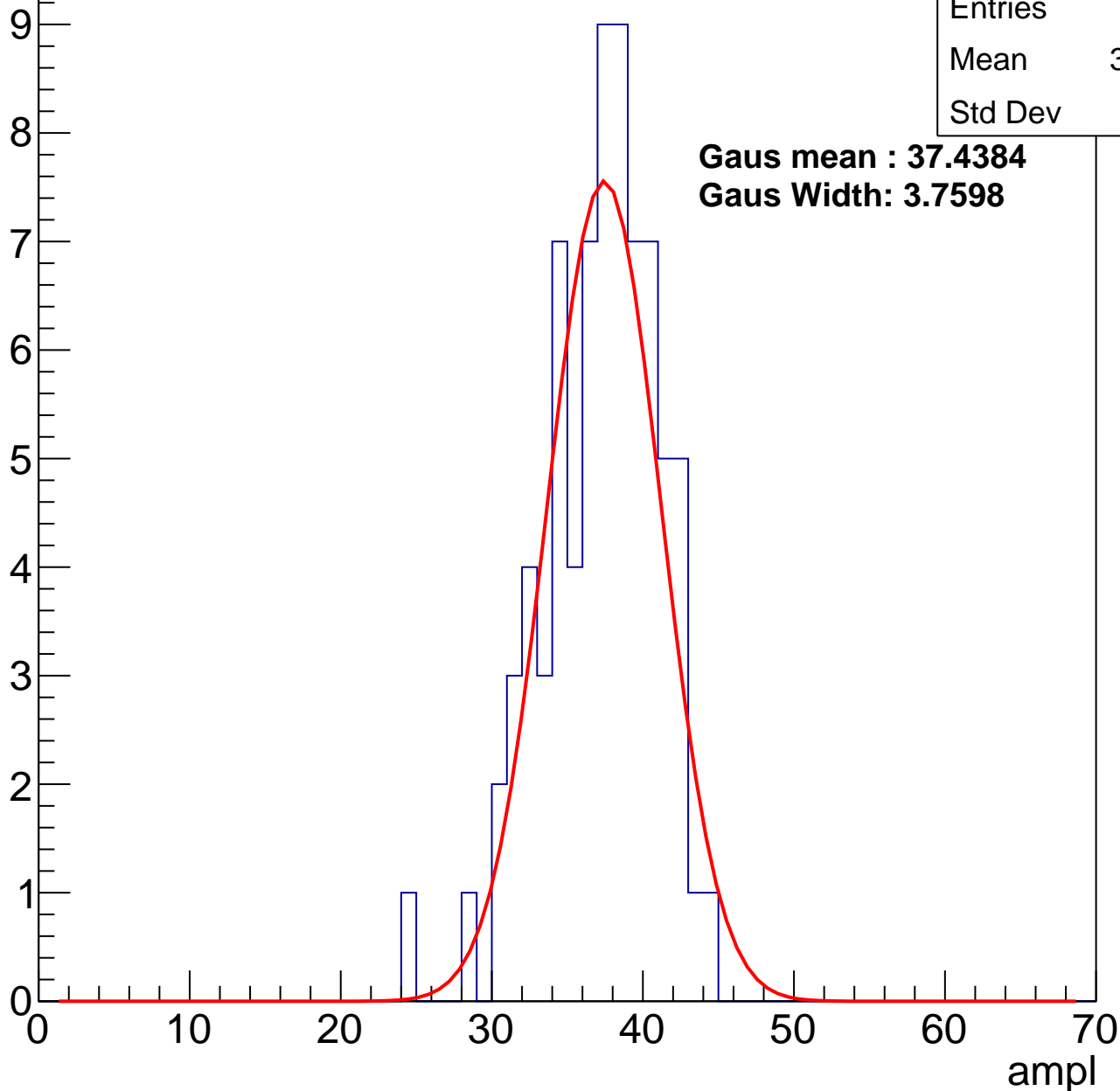
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	36.74
Std Dev	3.76

**Gaus mean : 37.4384**

**Gaus Width: 3.7598**



# B1L101S, U11-ch44, adc2

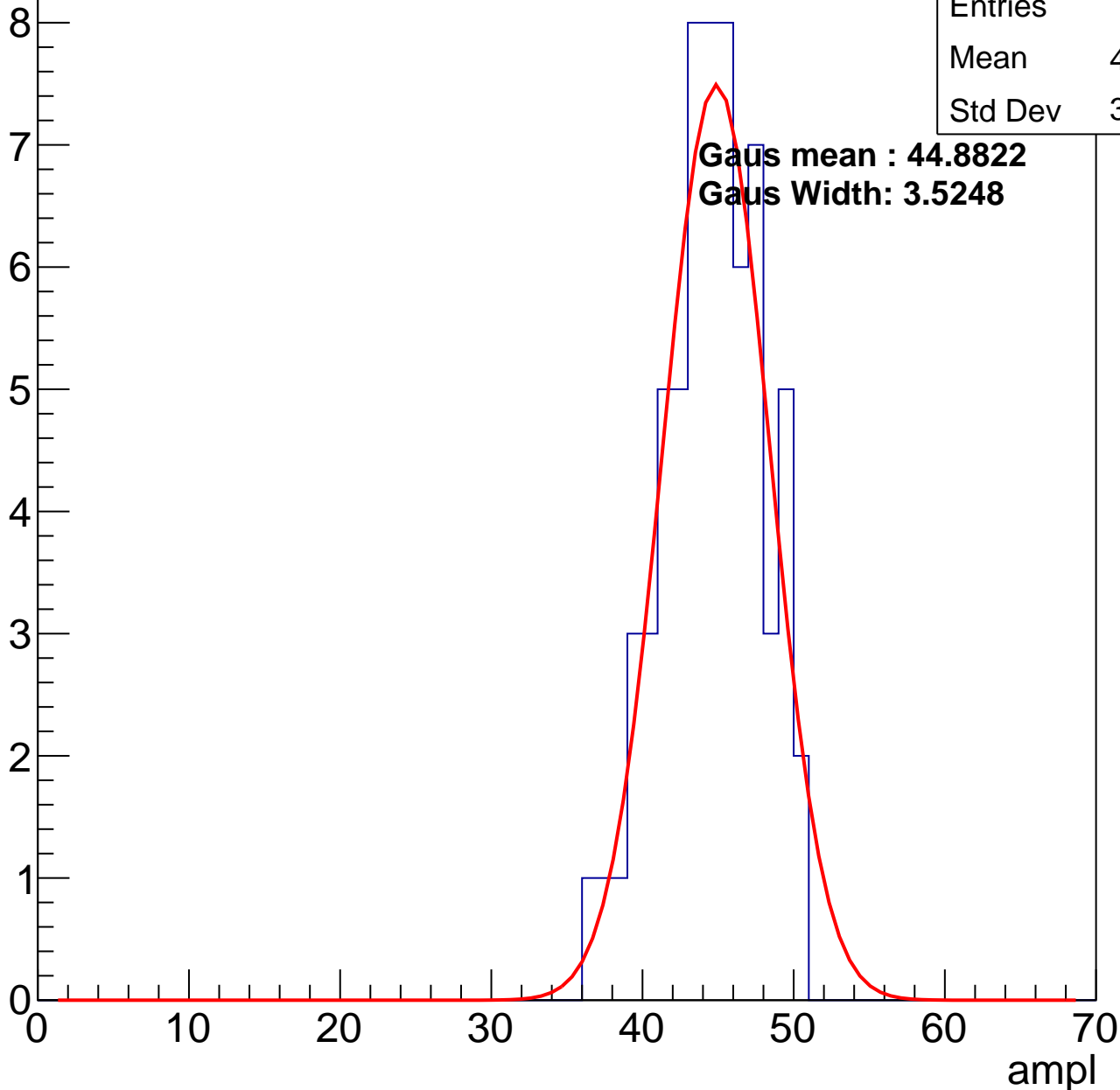
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	44.14
Std Dev	3.219

**Gaus mean : 44.8822**

**Gaus Width: 3.5248**

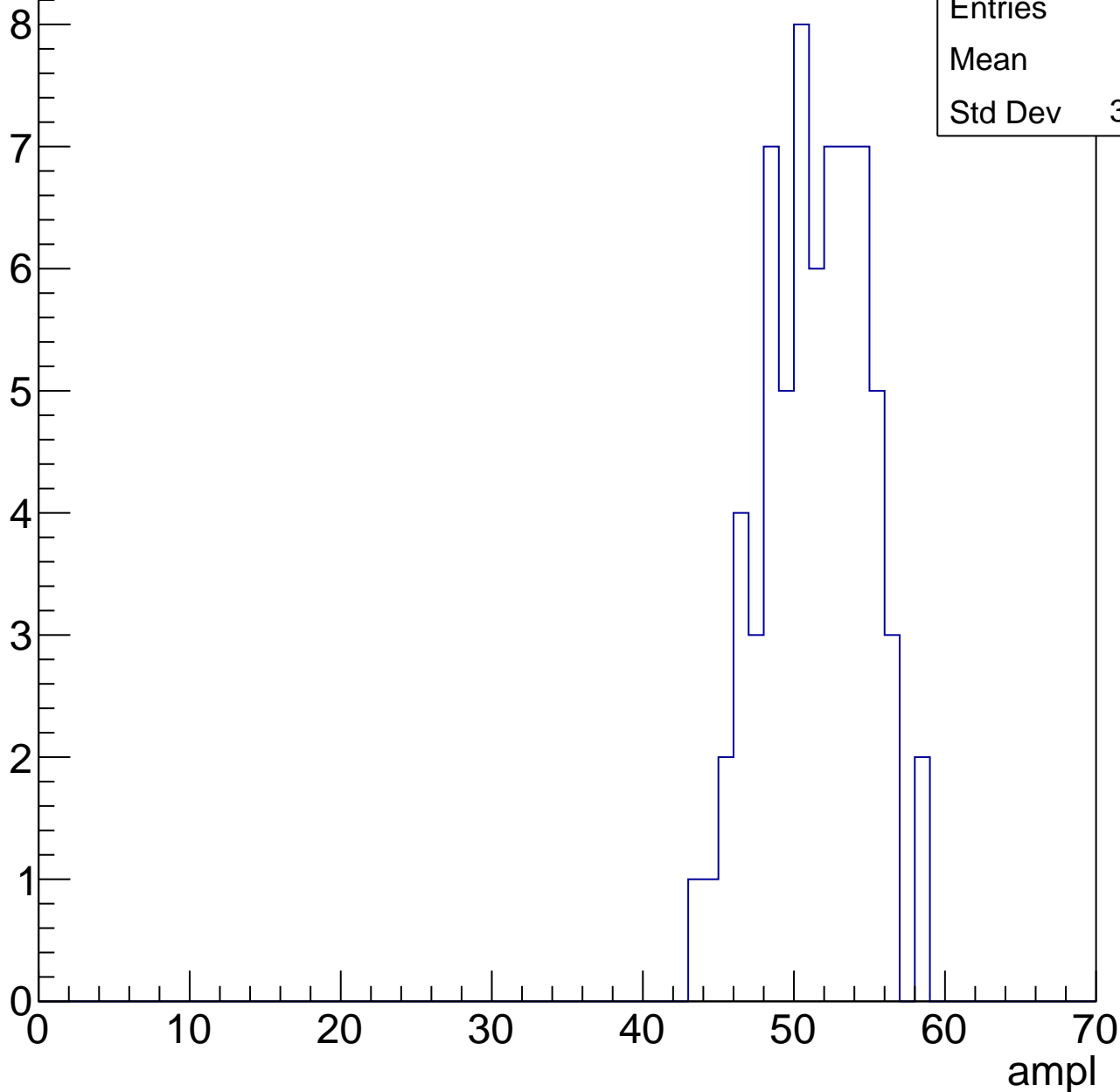


# B1L101S, U11-ch44, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

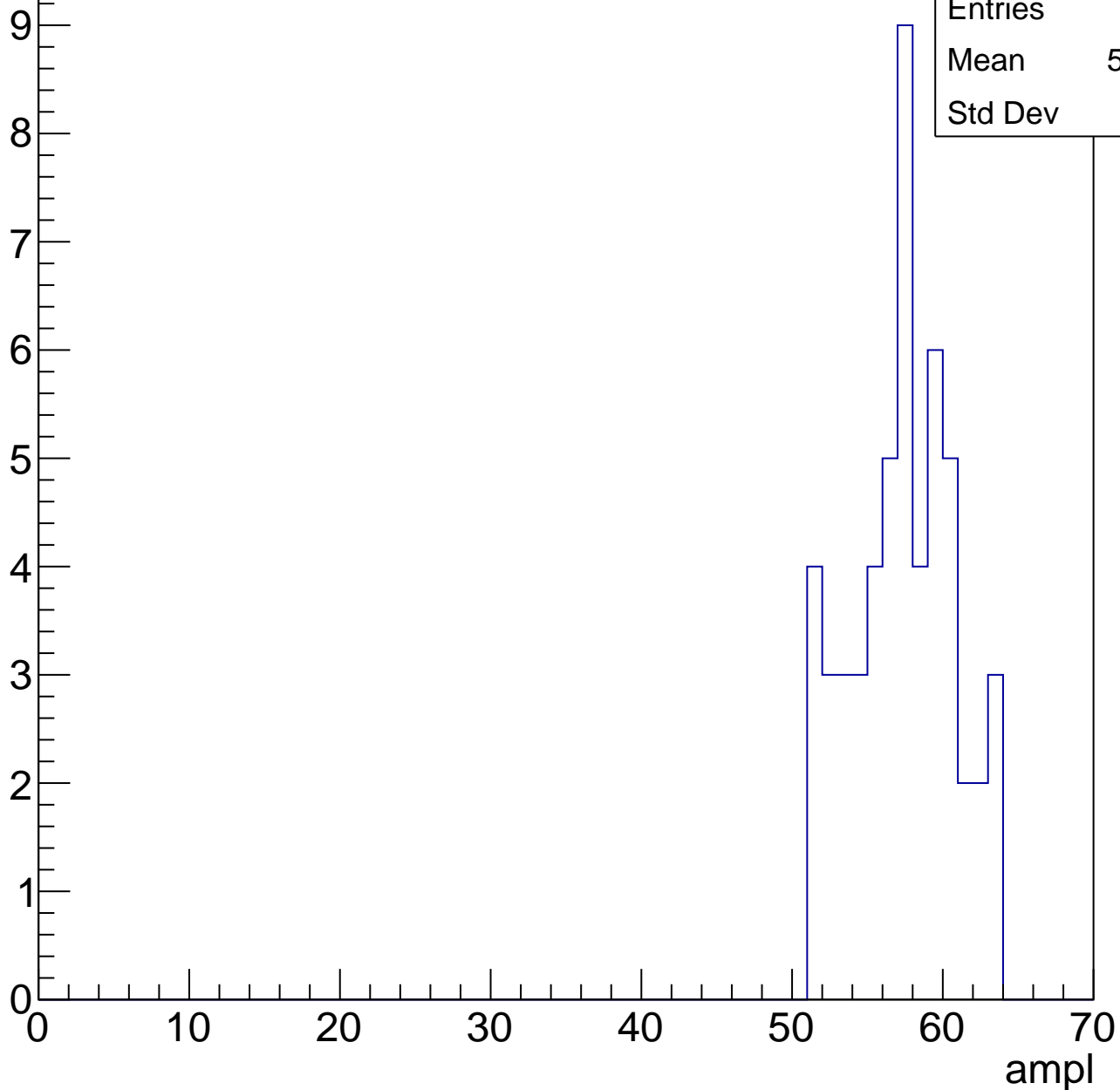
Entries	68
Mean	50.9
Std Dev	3.374



# B1L101S, U11-ch44, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



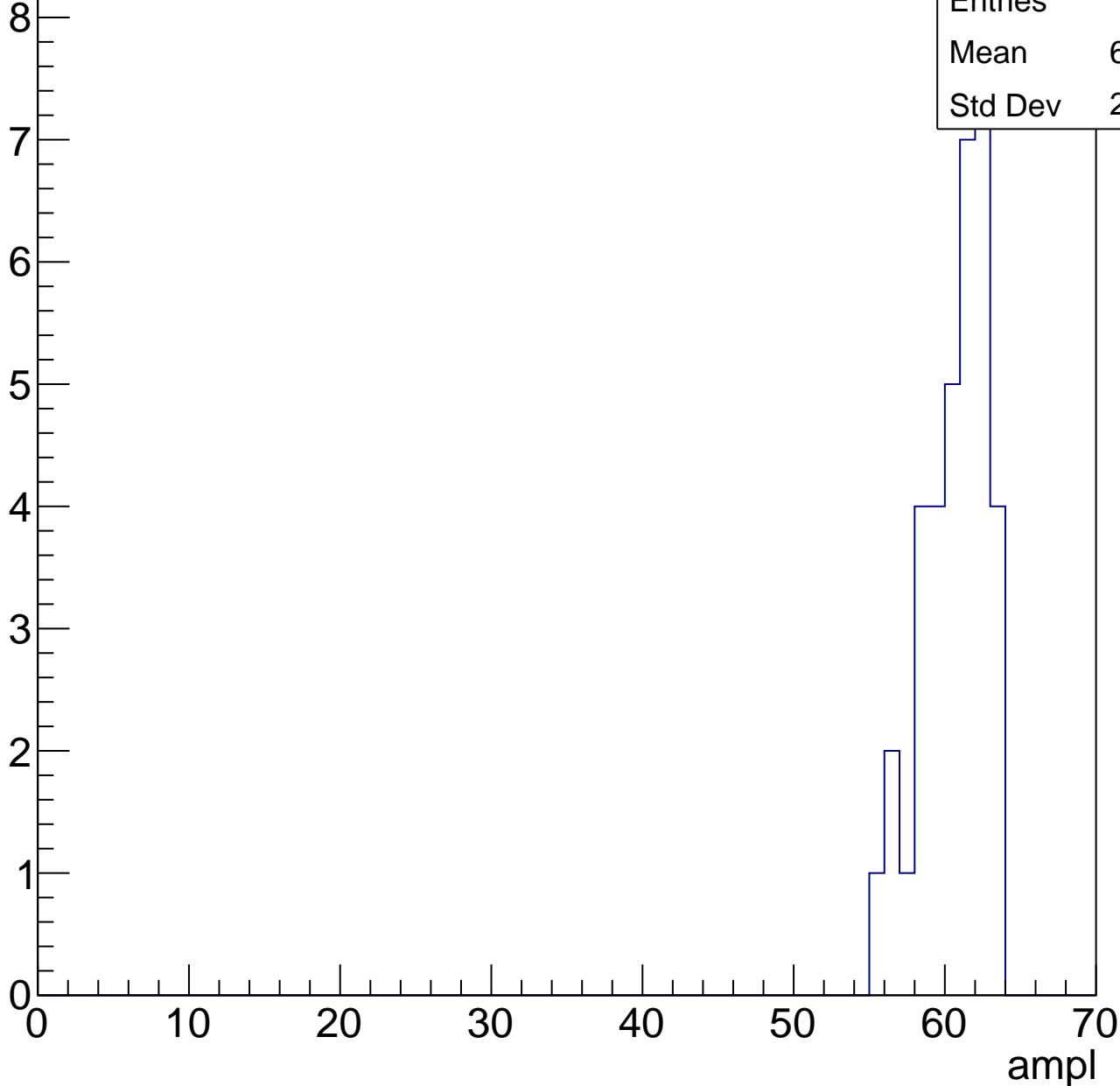
Entries	53
Mean	56.89
Std Dev	3.3

# B1L101S, U11-ch44, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

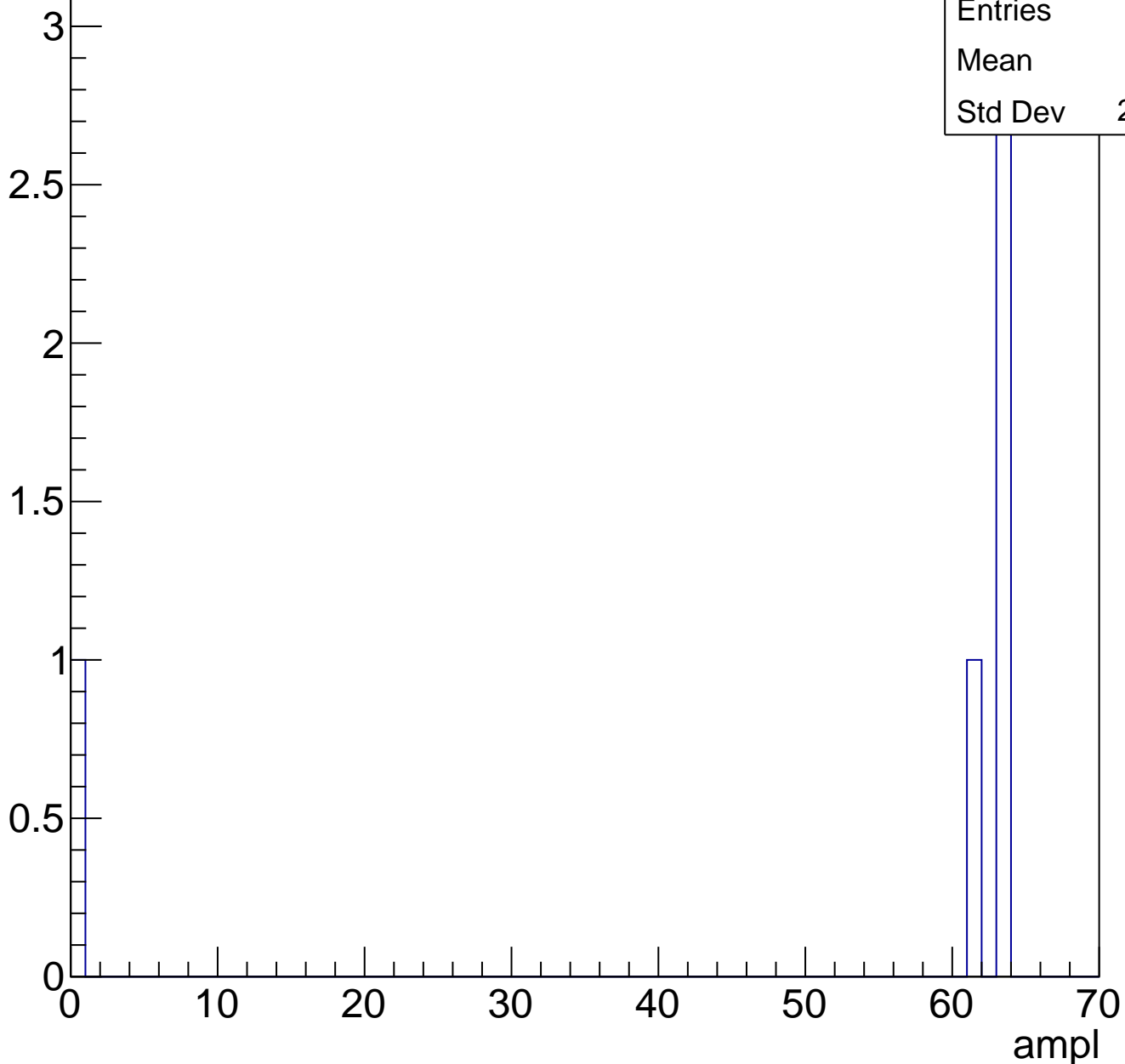
Entries	36
Mean	60.19
Std Dev	2.106



# B1L101S, U11-ch44, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch44, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U11-ch45, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	82
Mean	29.83
Std Dev	3.453

**Gaus mean : 30.1228**

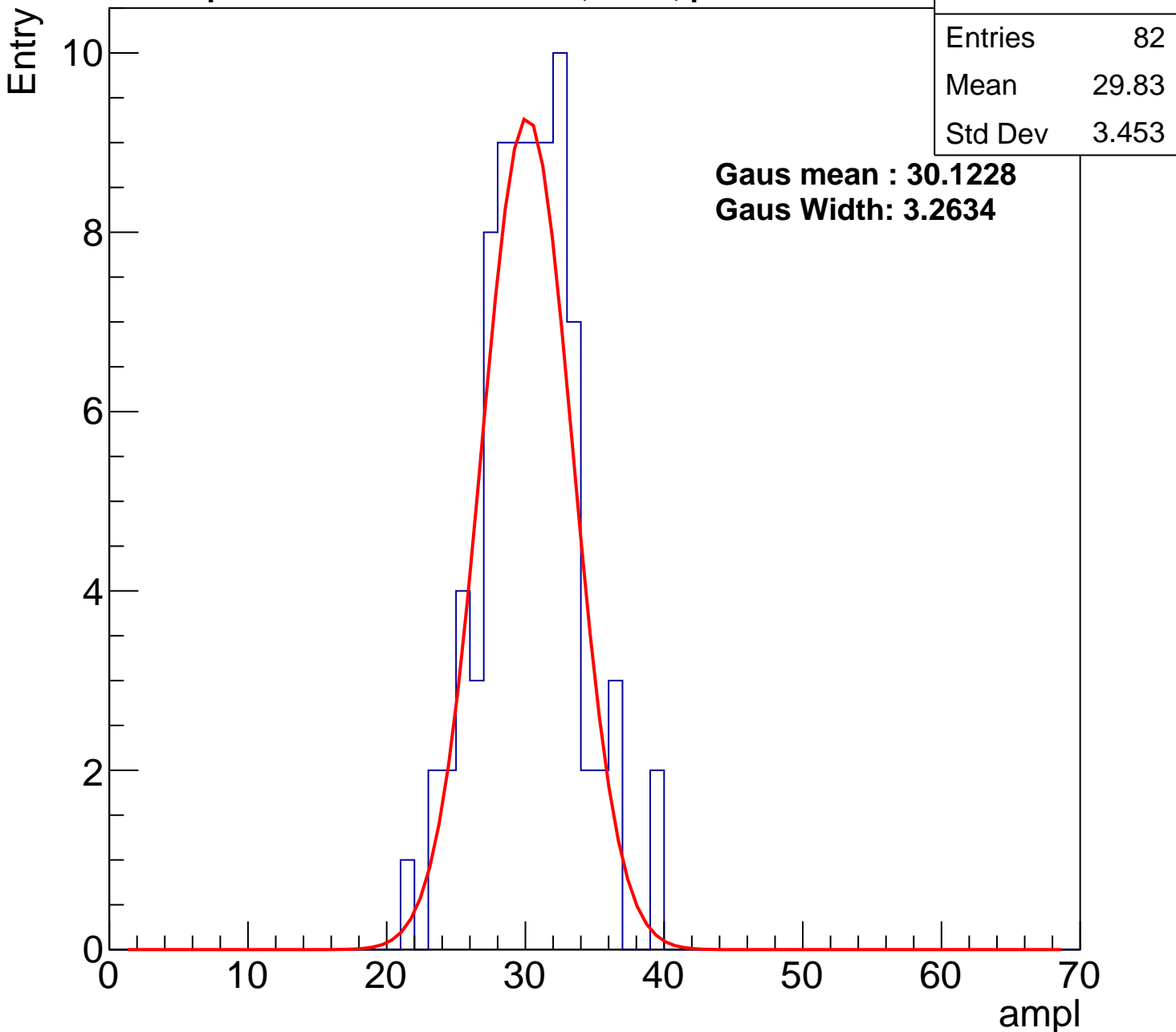
**Gaus Width: 3.2634**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



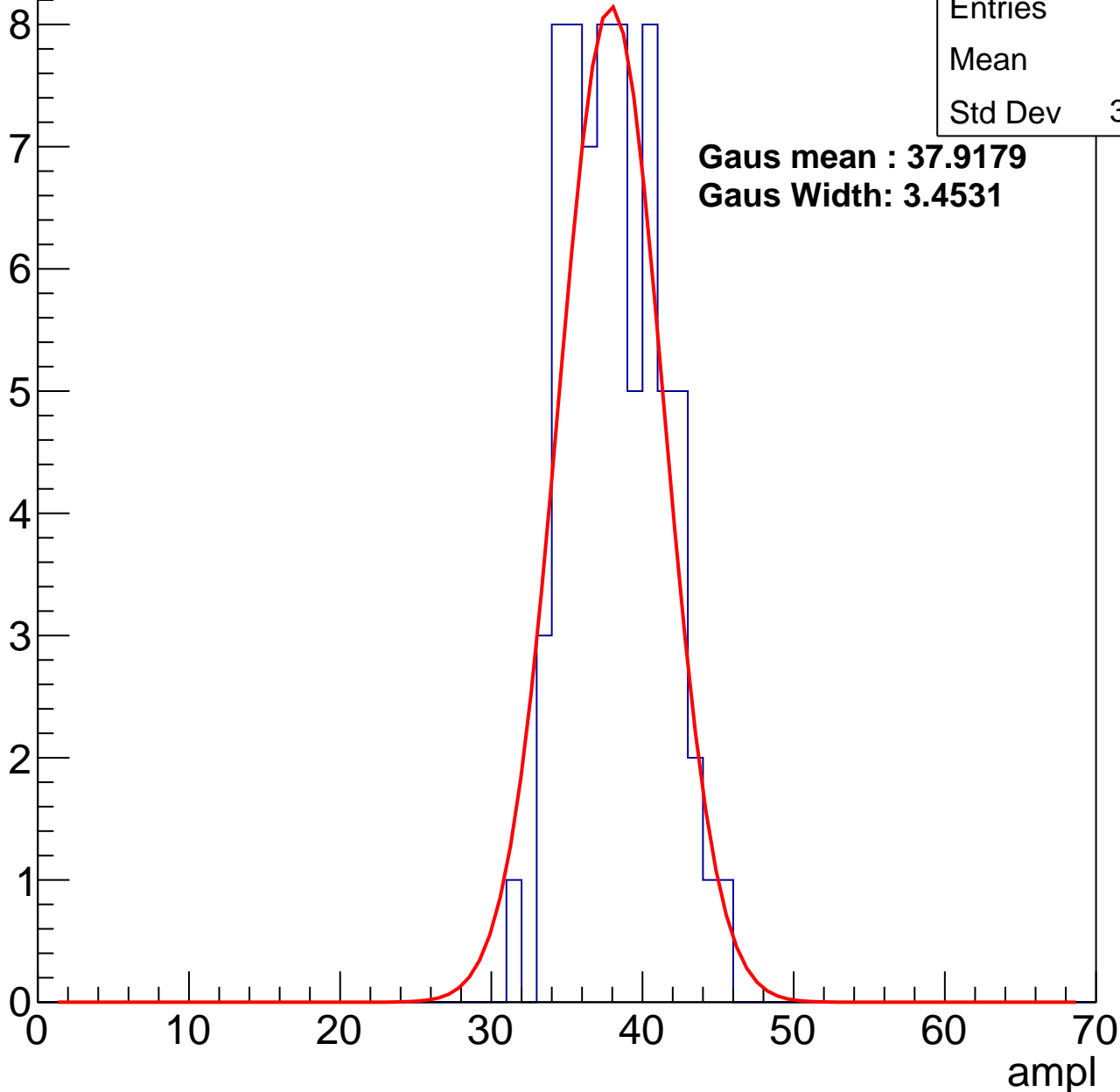
# B1L101S, U11-ch45, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	37.7
Std Dev	3.049

**Gaus mean : 37.9179**  
**Gaus Width: 3.4531**



# B1L101S, U11-ch45, adc2

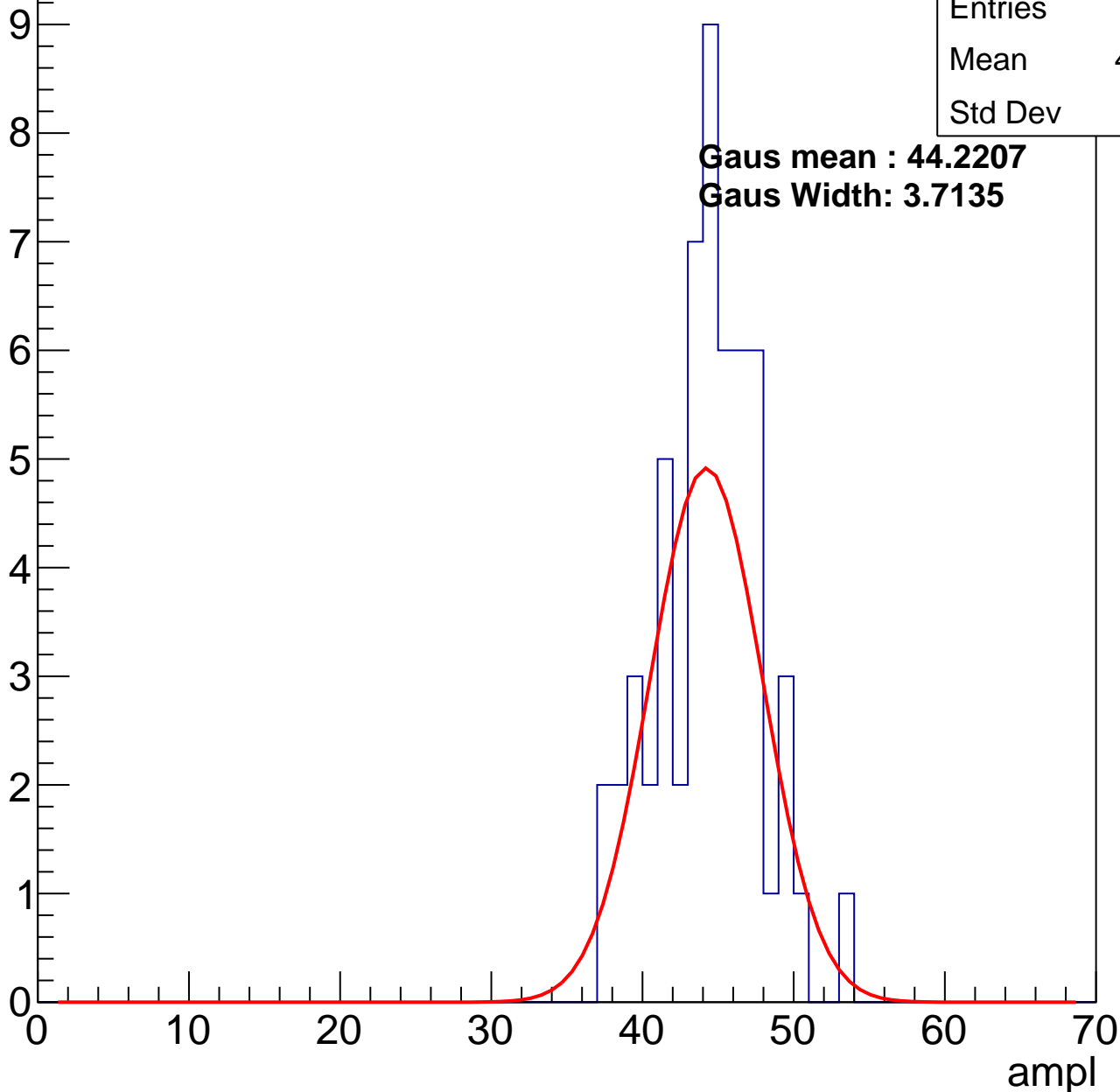
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	43.91
Std Dev	3.35

**Gaus mean : 44.2207**

**Gaus Width: 3.7135**

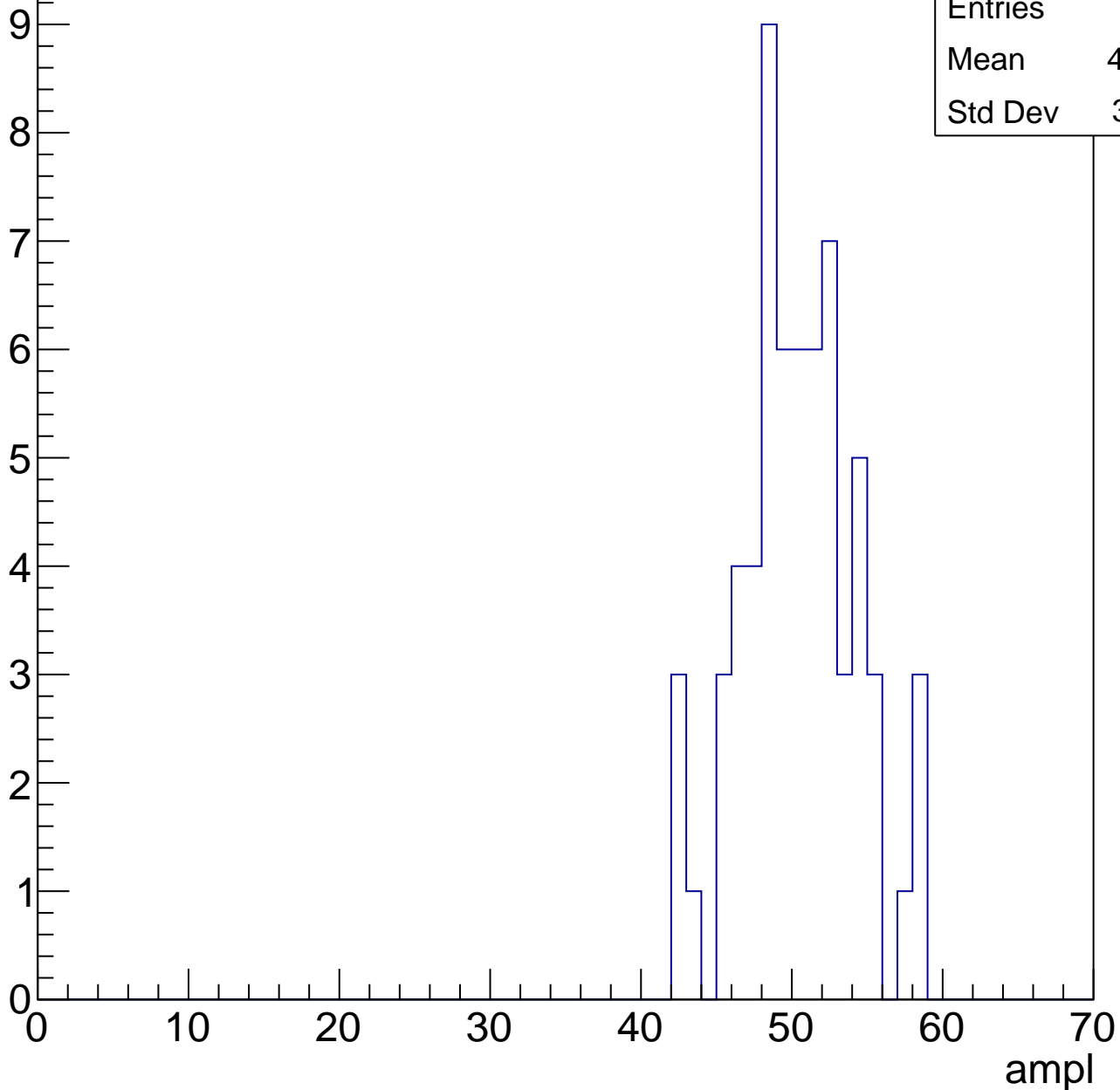


# B1L101S, U11-ch45, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	49.95
Std Dev	3.781

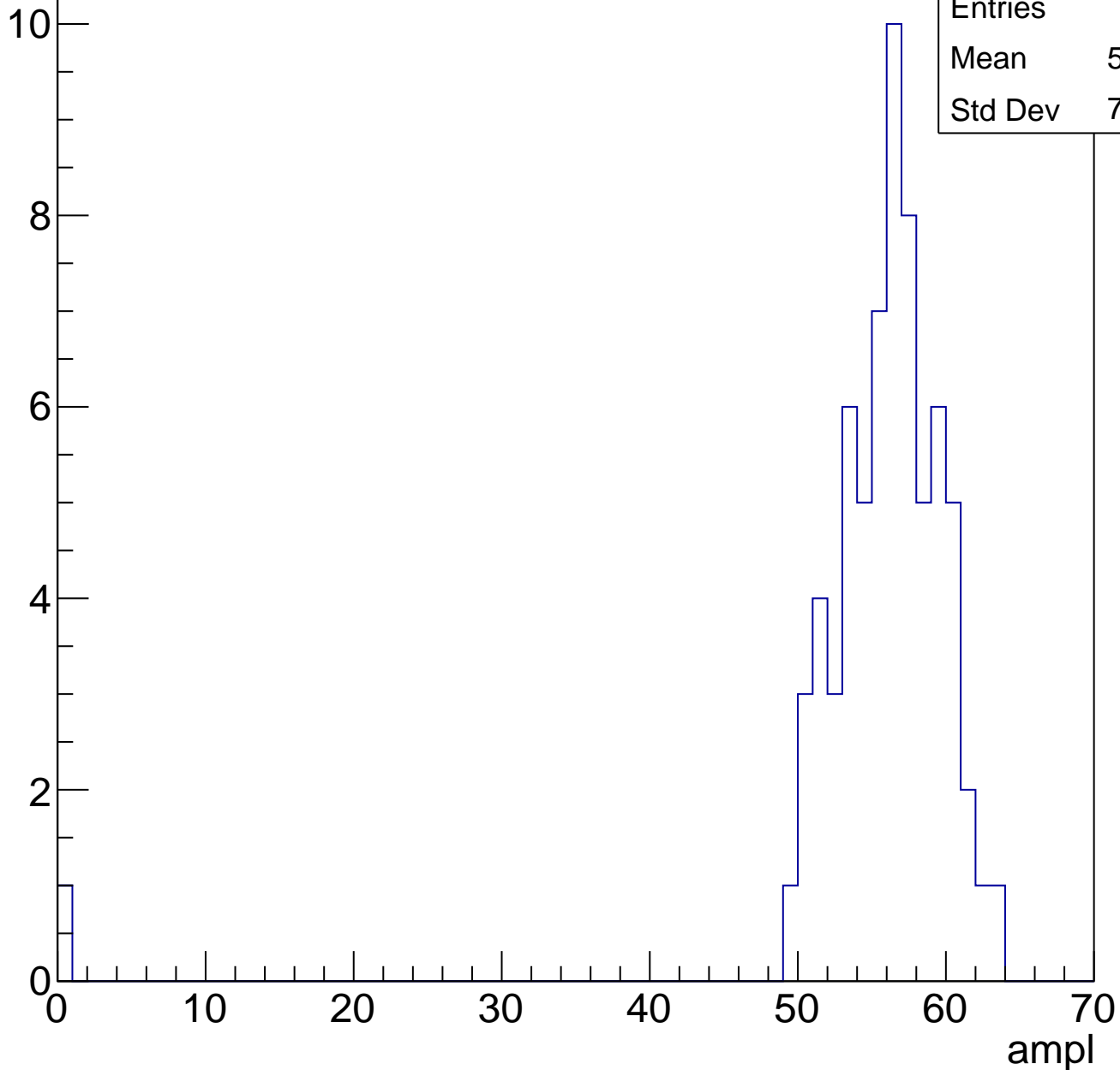


# B1L101S, U11-ch45, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	68
Mean	54.99
Std Dev	7.425

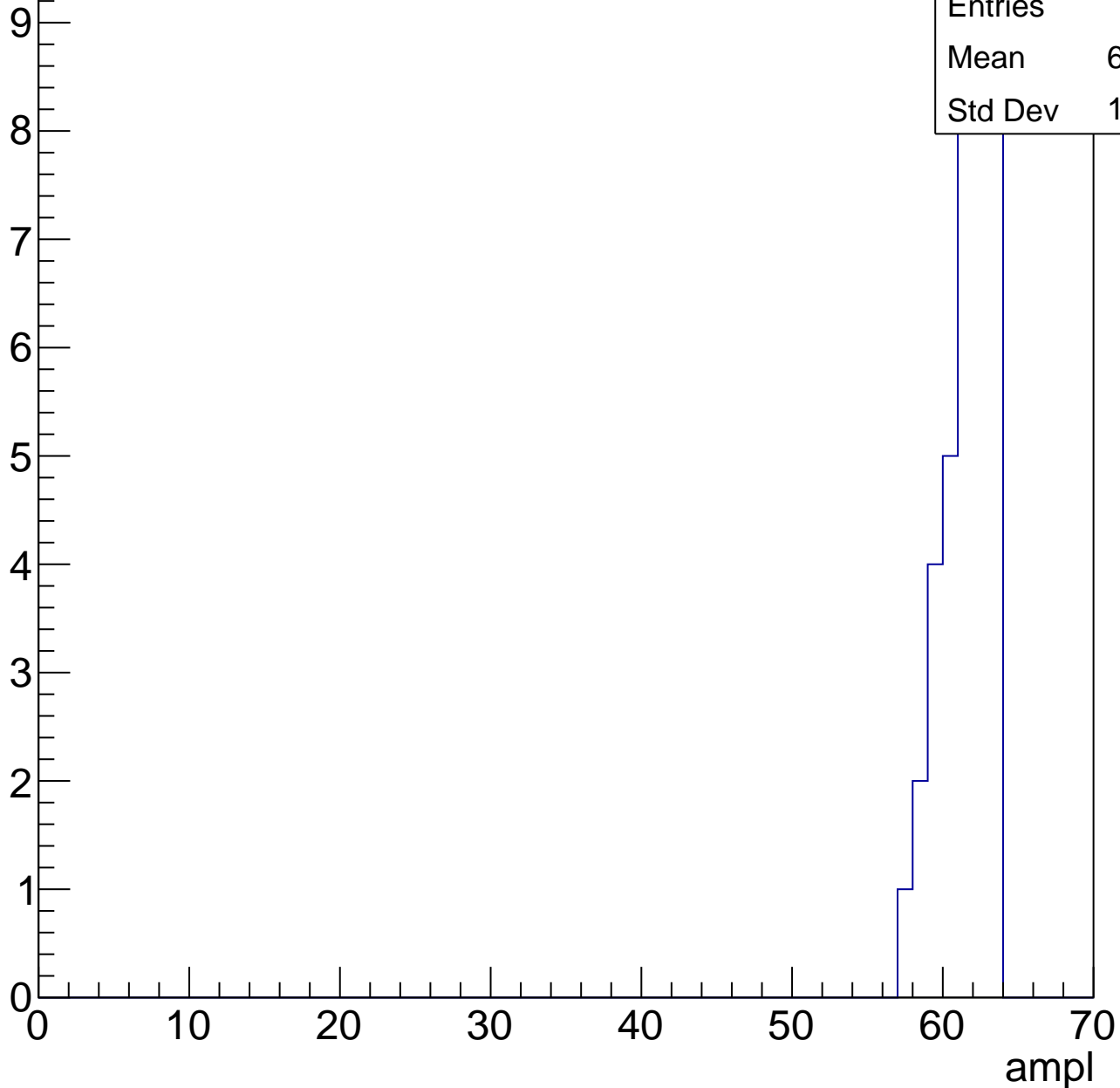
Entry



# B1L101S, U11-ch45, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U11-ch45, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch45, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U11-ch46, adc0

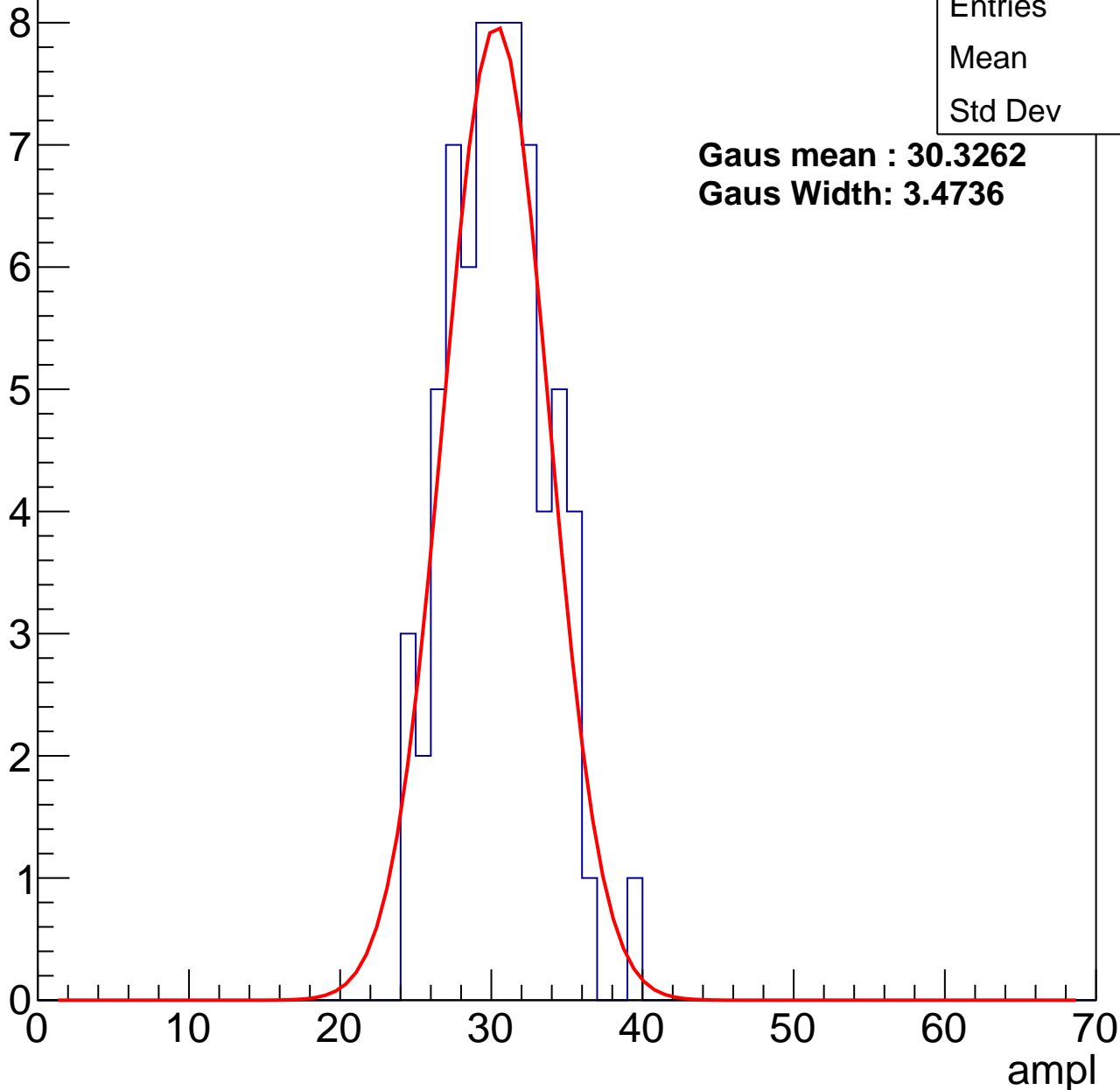
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	30
Std Dev	3.19

**Gaus mean : 30.3262**

**Gaus Width: 3.4736**



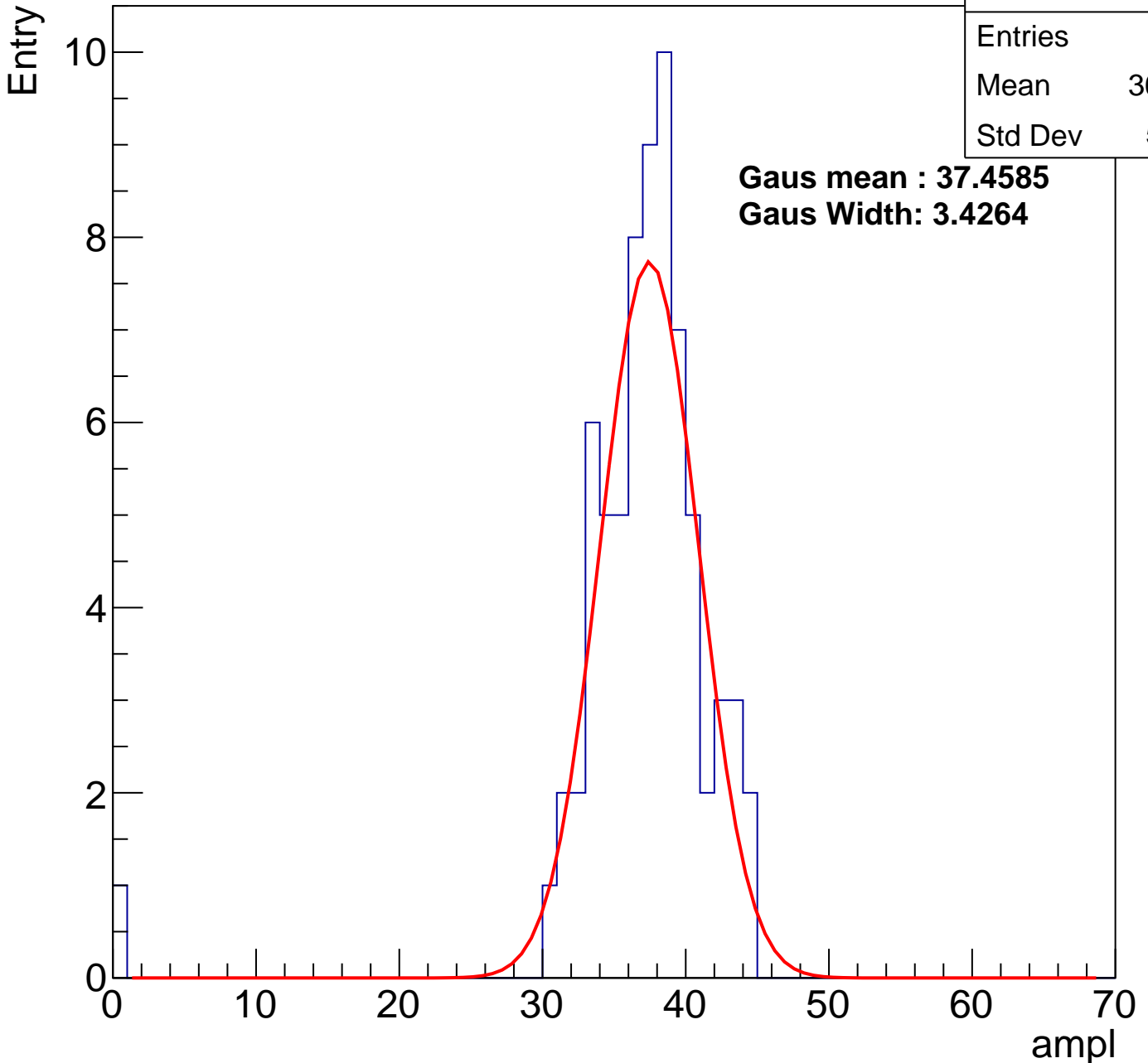
# B1L101S, U11-ch46, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	71
Mean	36.59
Std Dev	5.43

**Gaus mean : 37.4585**

**Gaus Width: 3.4264**



# B1L101S, U11-ch46, adc2

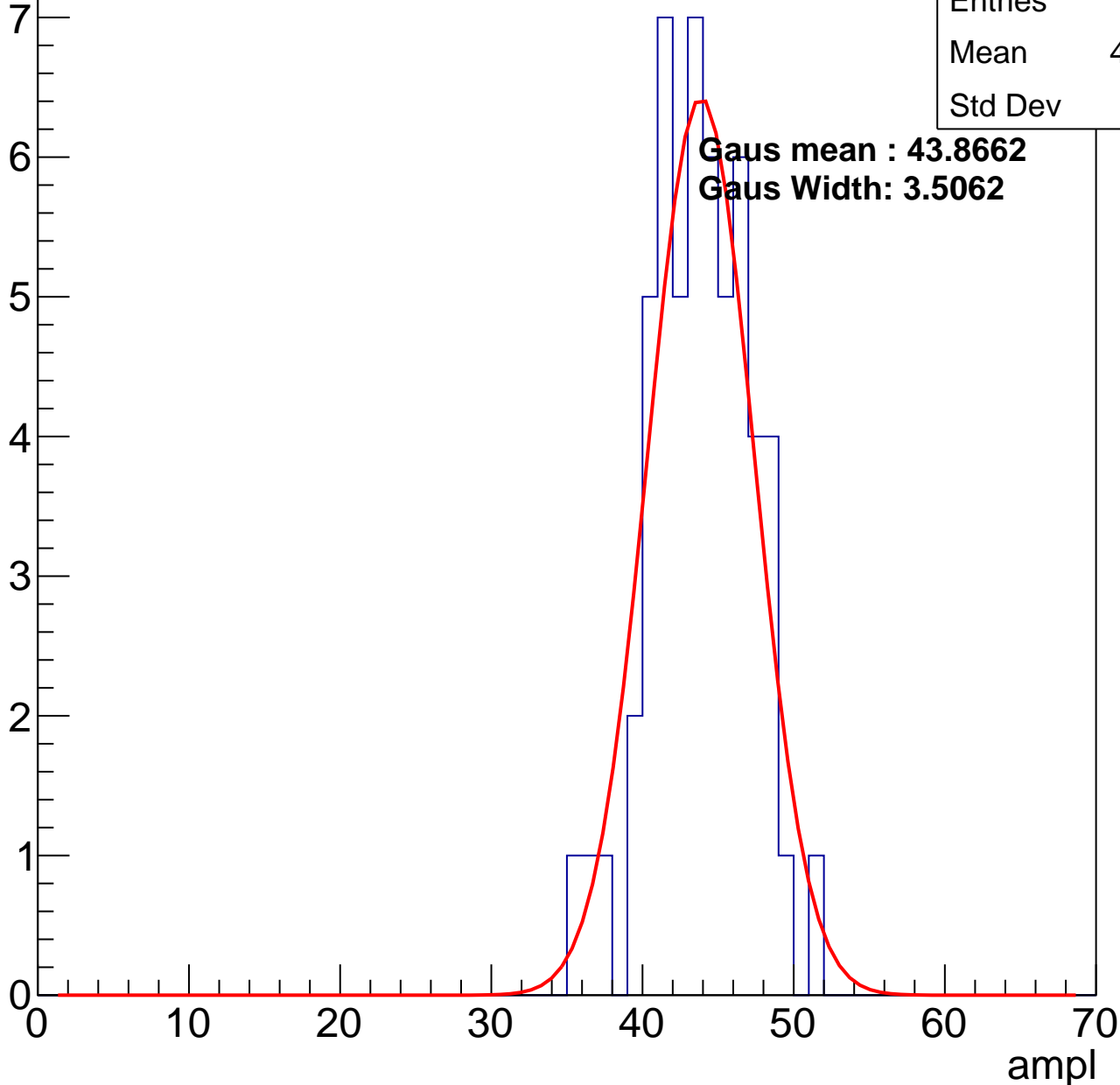
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	43.38
Std Dev	3.26

**Gaus mean : 43.8662**

**Gaus Width: 3.5062**



# B1L101S, U11-ch46, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

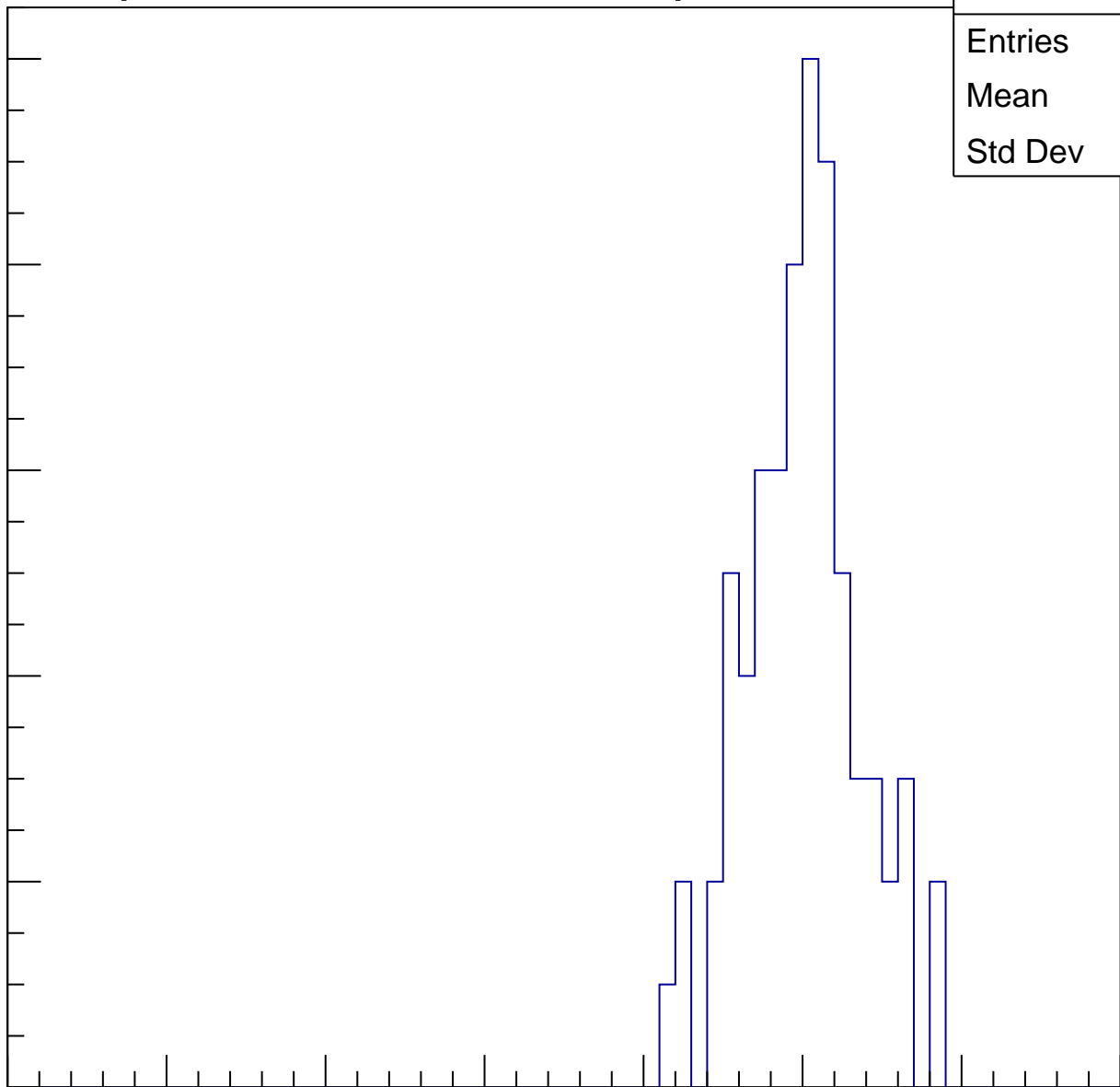
Entries	71
Mean	49.55
Std Dev	3.622

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

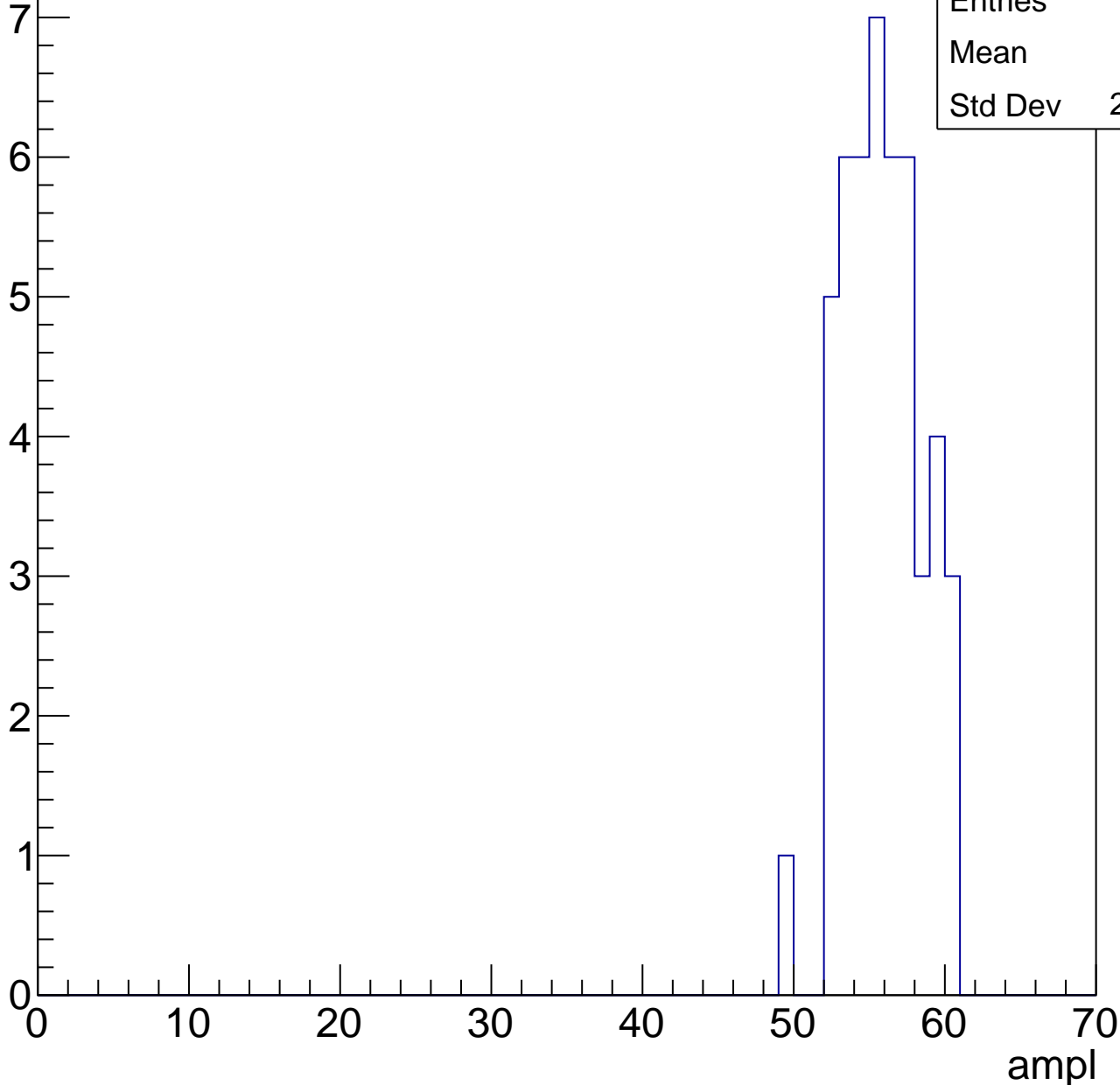


# B1L101S, U11-ch46, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

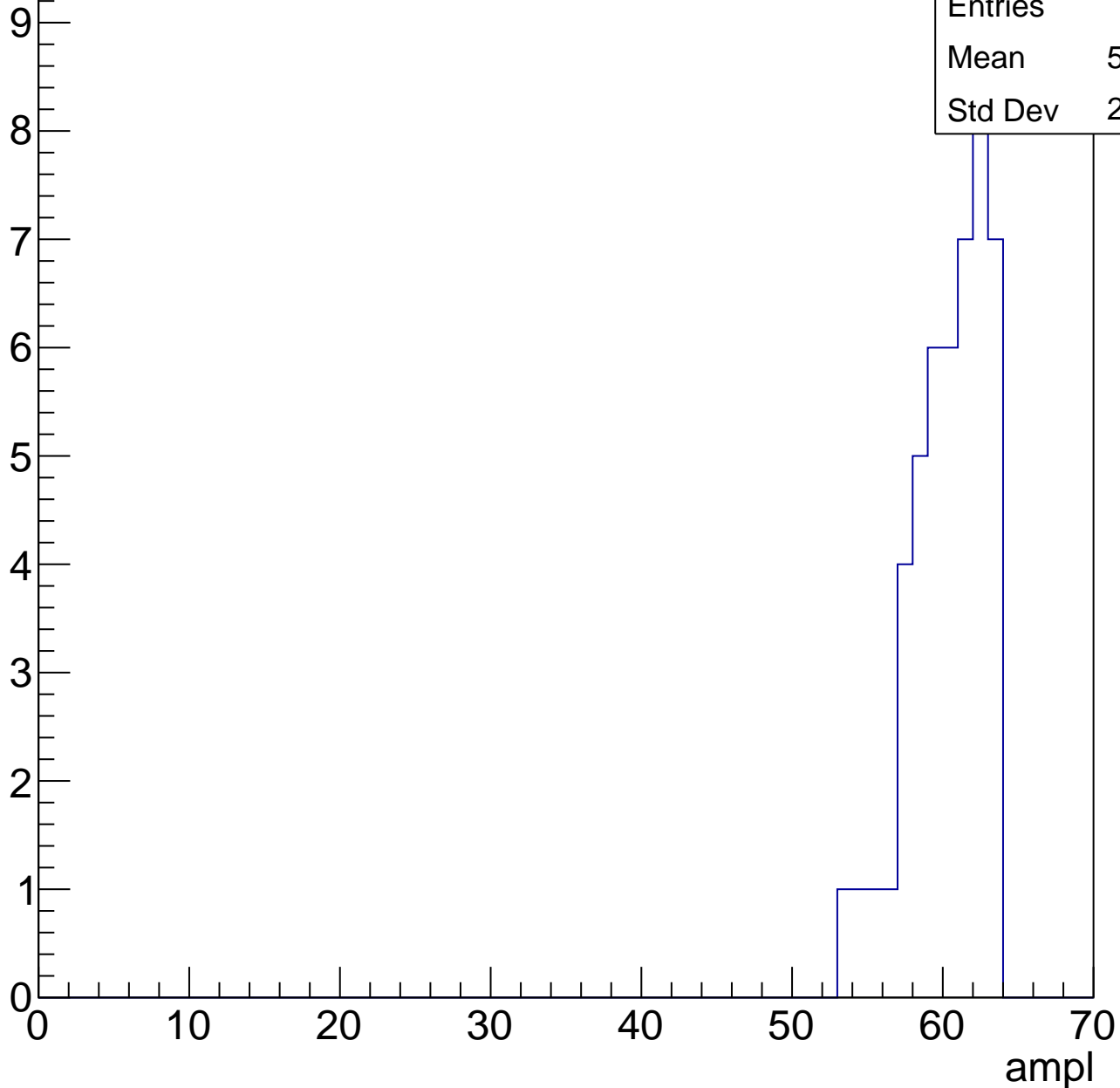
Entries	47
Mean	55.4
Std Dev	2.524



# B1L101S, U11-ch46, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

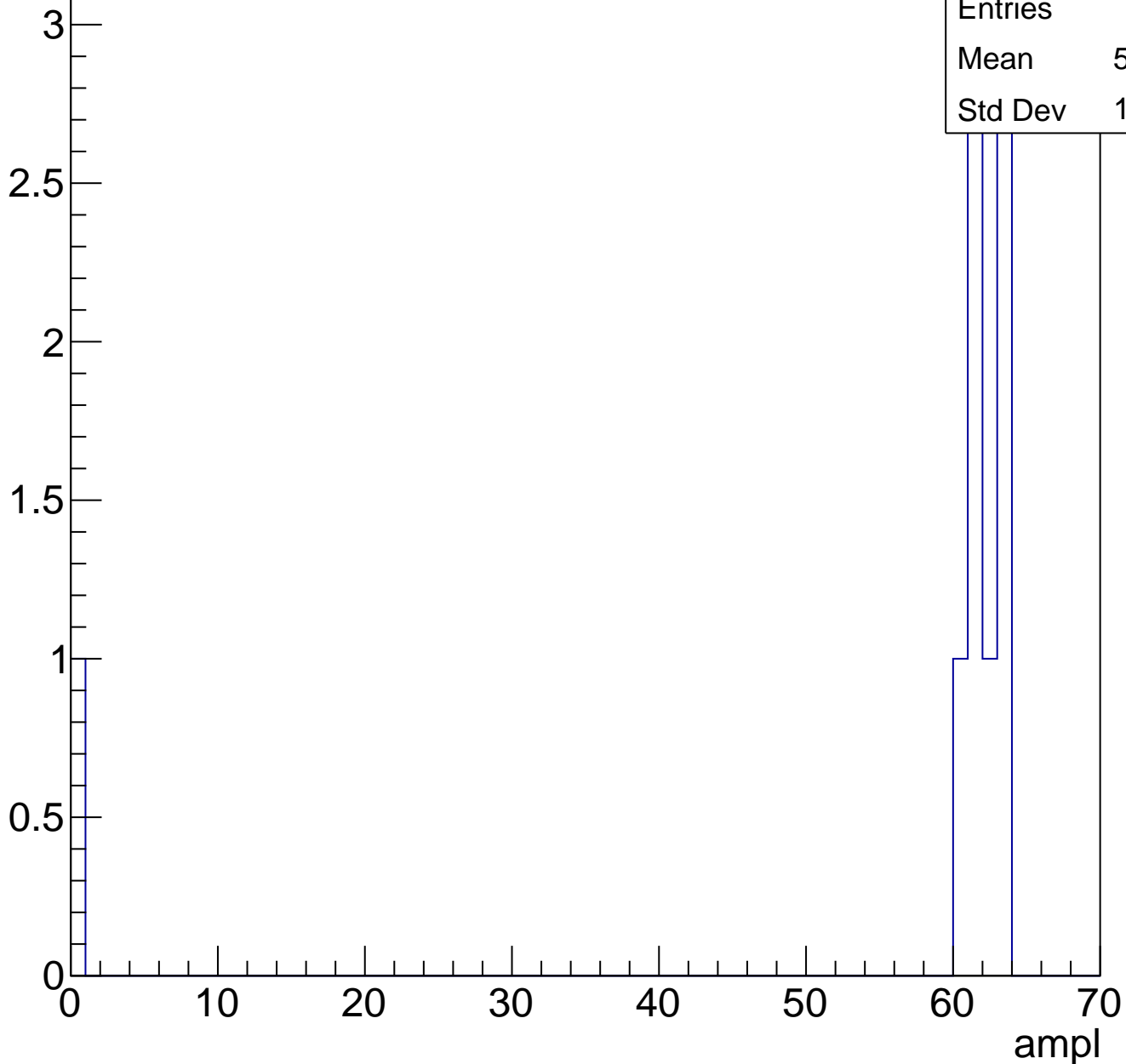
Entry



# B1L101S, U11-ch46, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

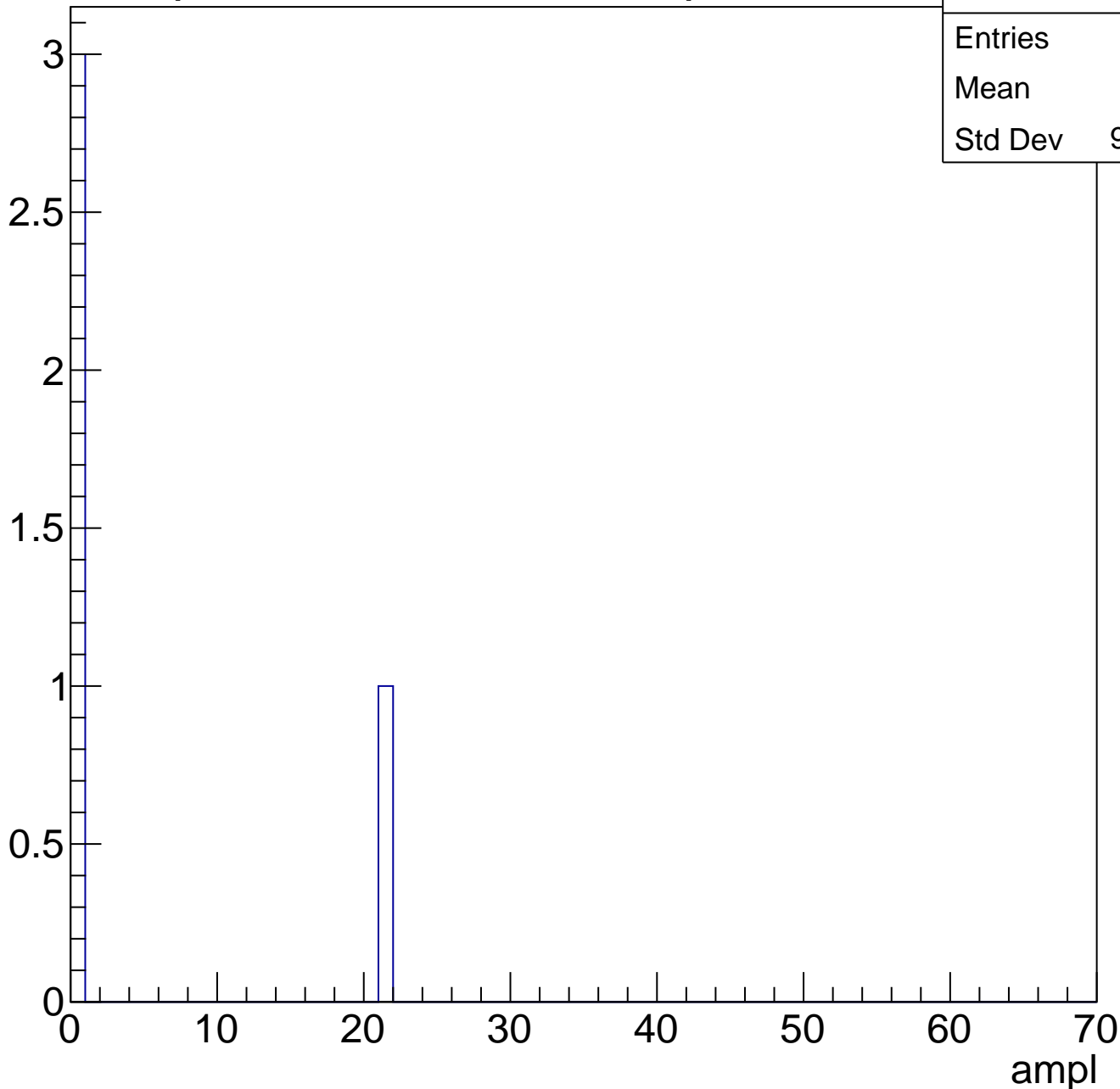




# B1L101S, U11-ch46, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	4
Mean	5.25
Std Dev	9.093

# B1L101S, U11-ch47, adc0

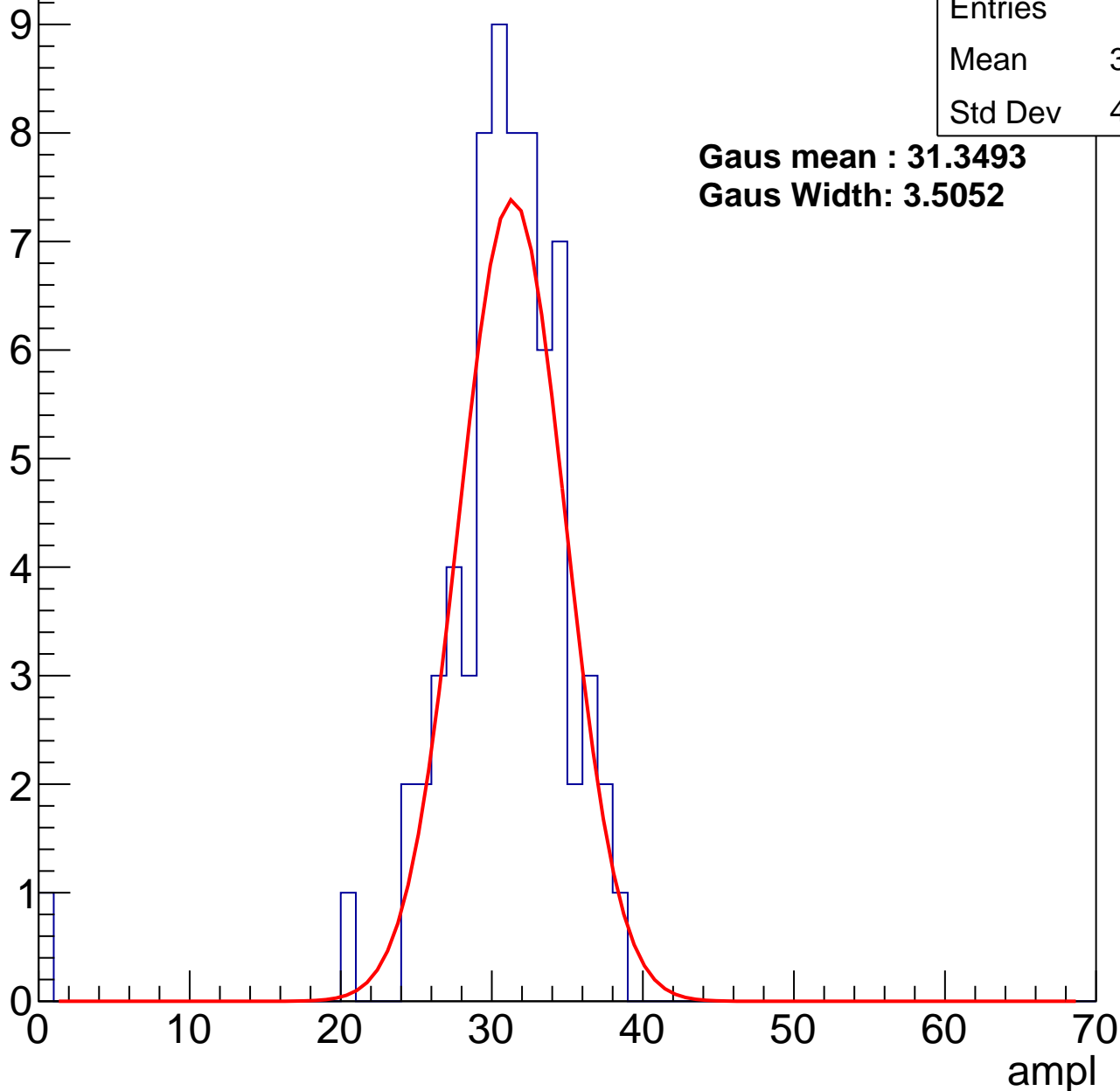
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	30.29
Std Dev	4.995

**Gaus mean : 31.3493**

**Gaus Width: 3.5052**



# B1L101S, U11-ch47, adc1

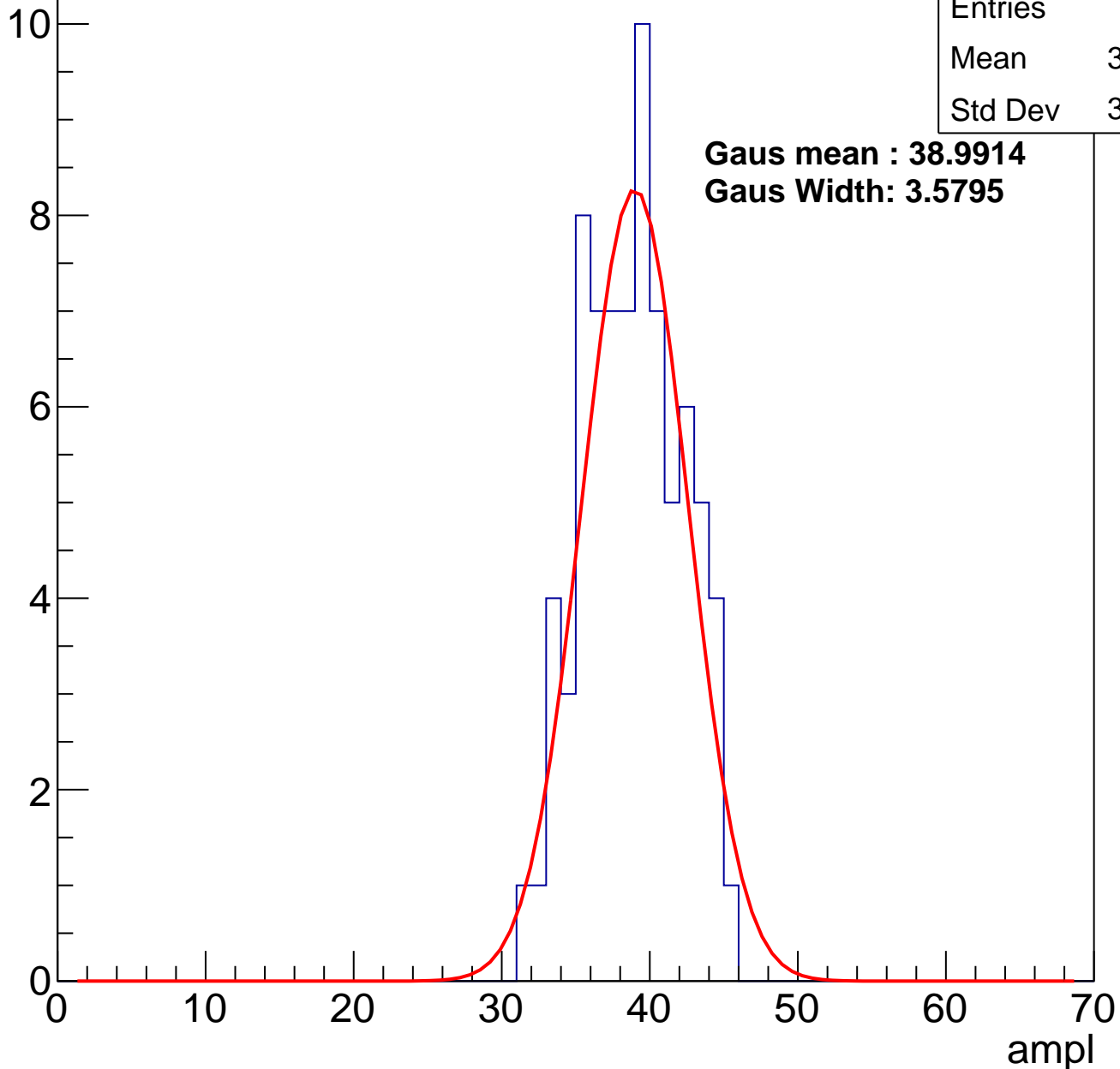
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	76
Mean	38.38
Std Dev	3.297

**Gaus mean : 38.9914**

**Gaus Width: 3.5795**

Entry



# B1L101S, U11-ch47, adc2

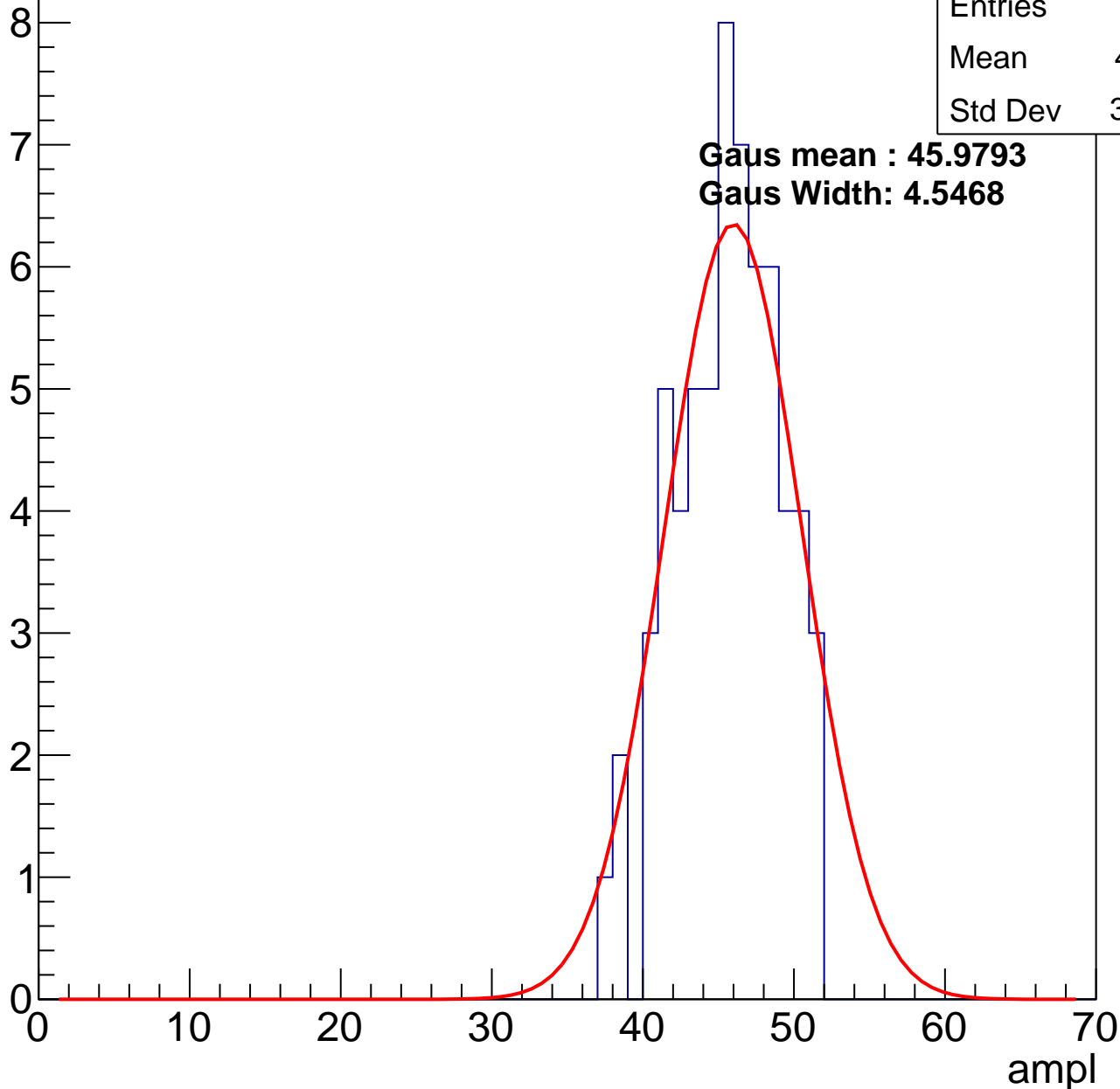
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	45.11
Std Dev	3.414

**Gaus mean : 45.9793**

**Gaus Width: 4.5468**



# B1L101S, U11-ch47, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	64
Mean	51.34
Std Dev	3.188

Entry

10

8

6

4

2

0

0

10

20

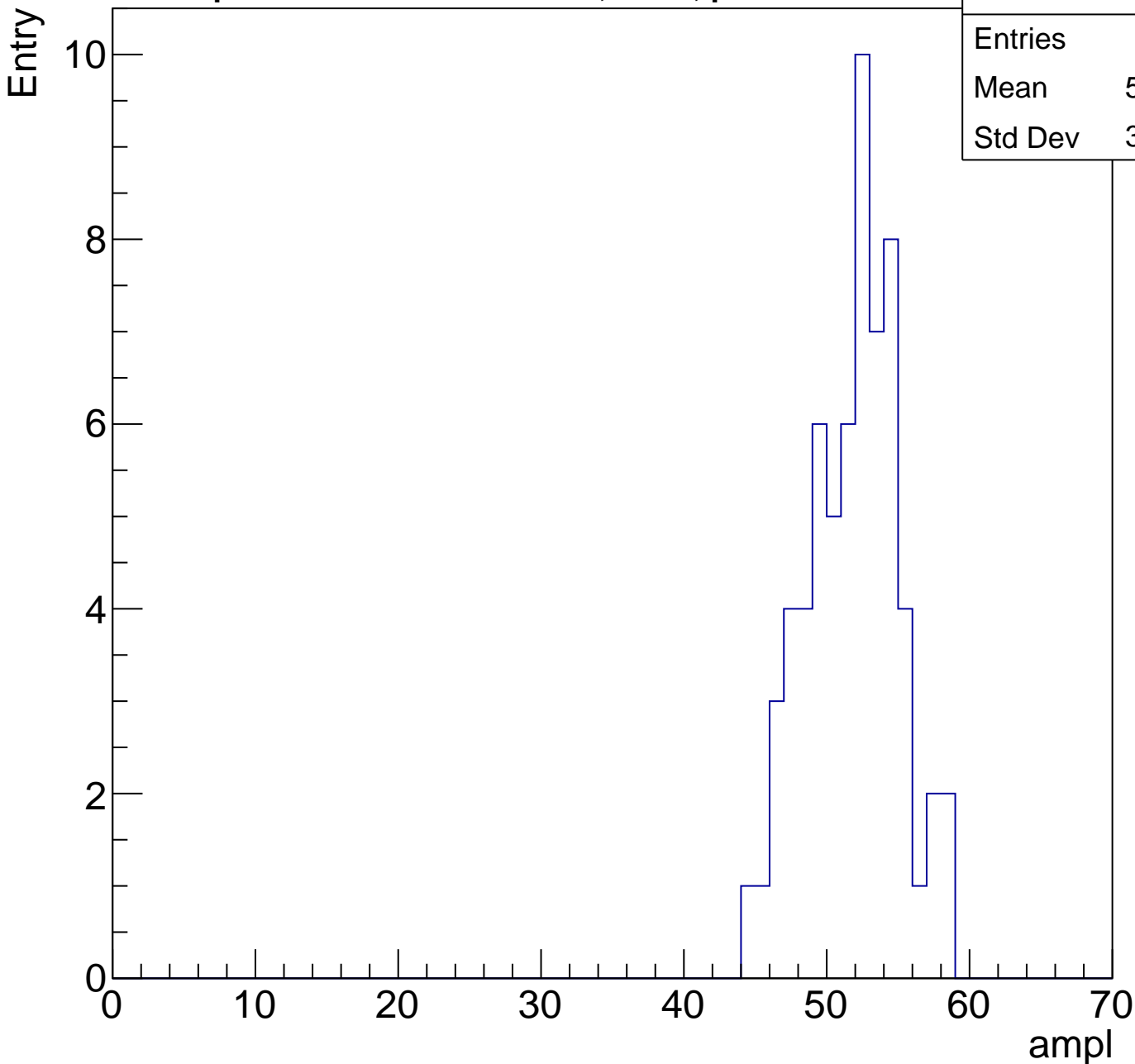
30

40

50

60

ampl

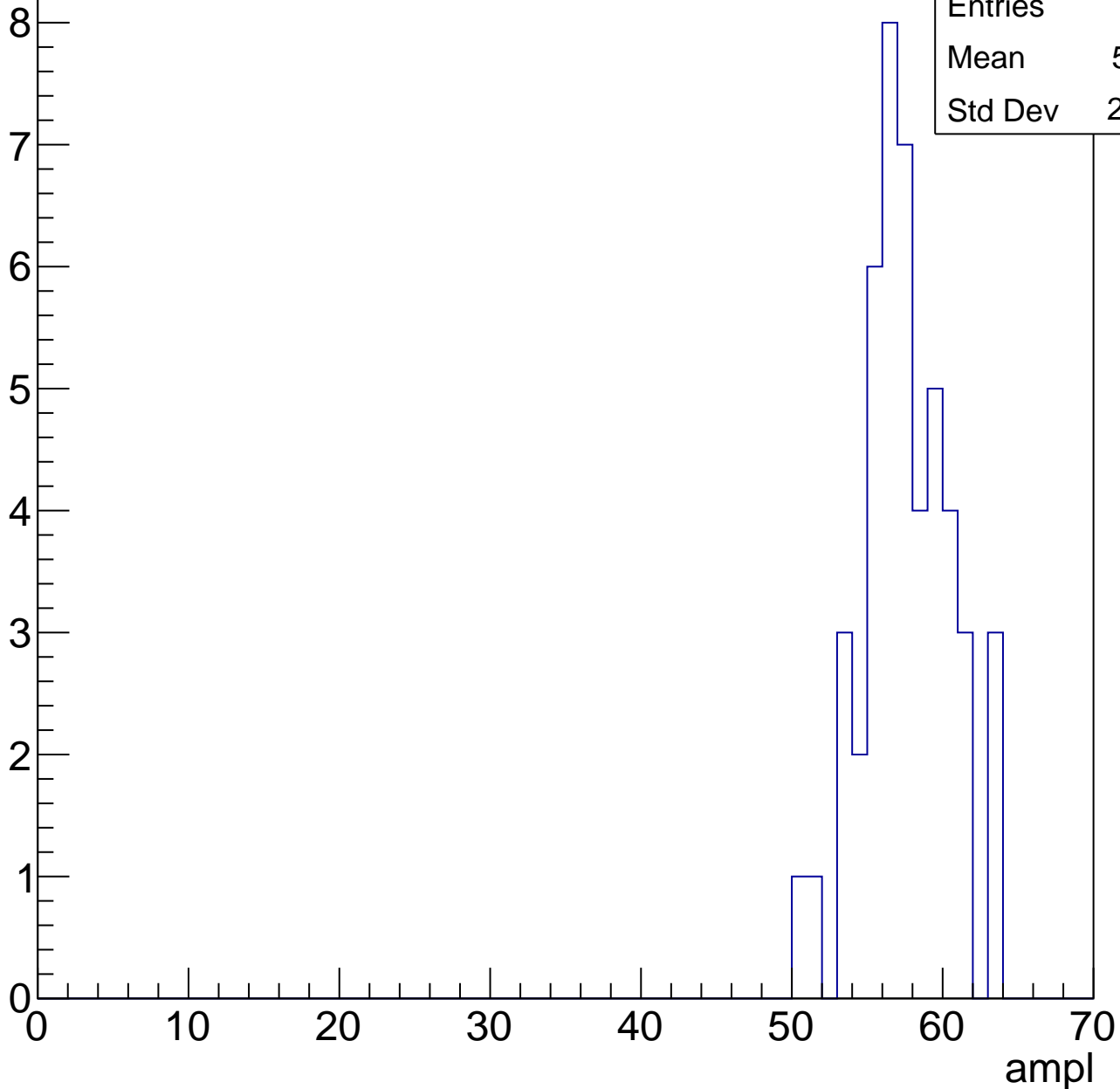


# B1L101S, U11-ch47, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	47
Mean	57.11
Std Dev	2.912



# B1L101S, U11-ch47, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	42
Mean	59.24
Std Dev	9.426

Entry

10

8

6

4

2

0

0

10

20

30

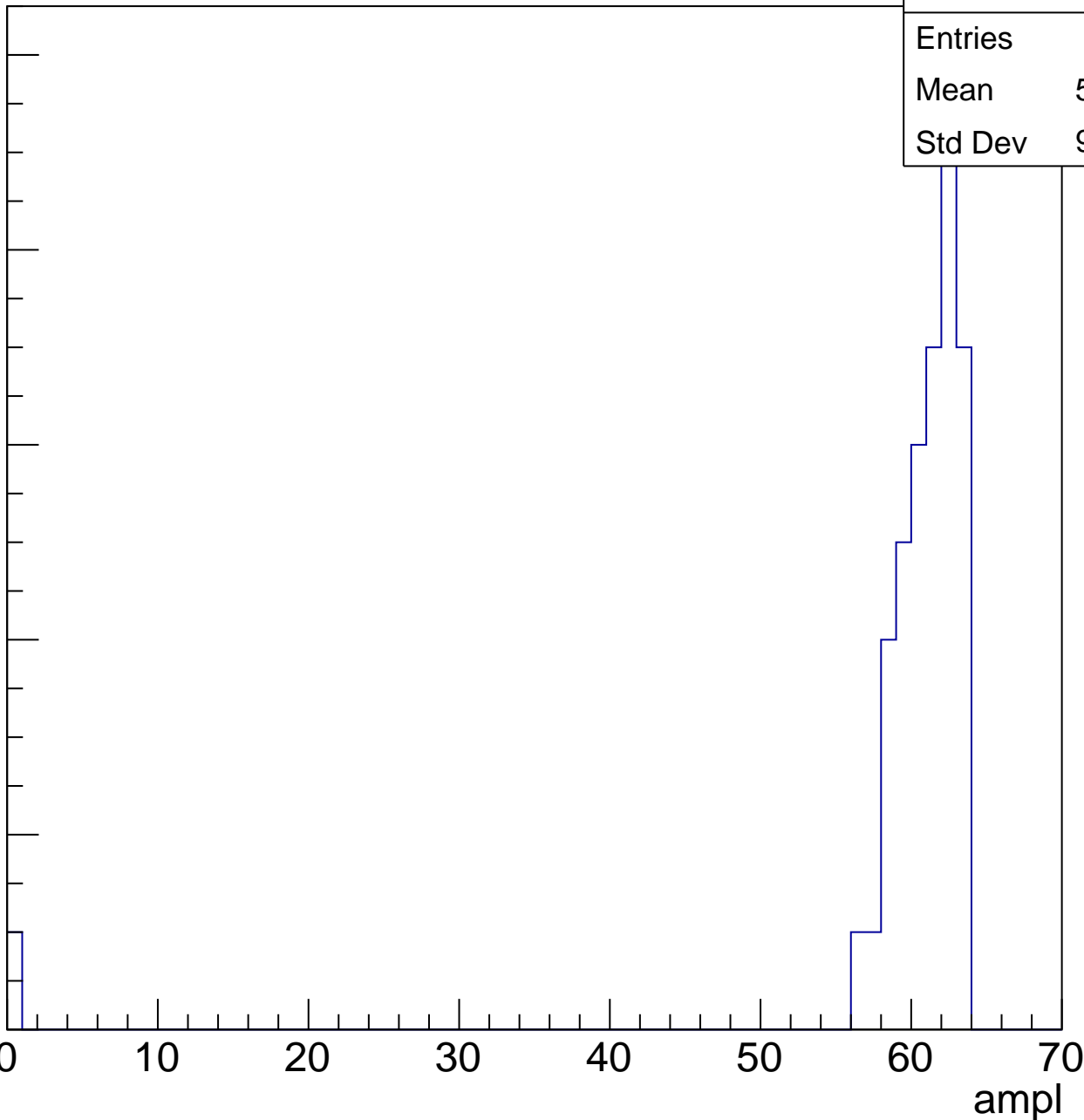
40

50

60

70

ampl



# B1L101S, U11-ch47, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L101S, U11-ch47, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U11-ch48, adc0

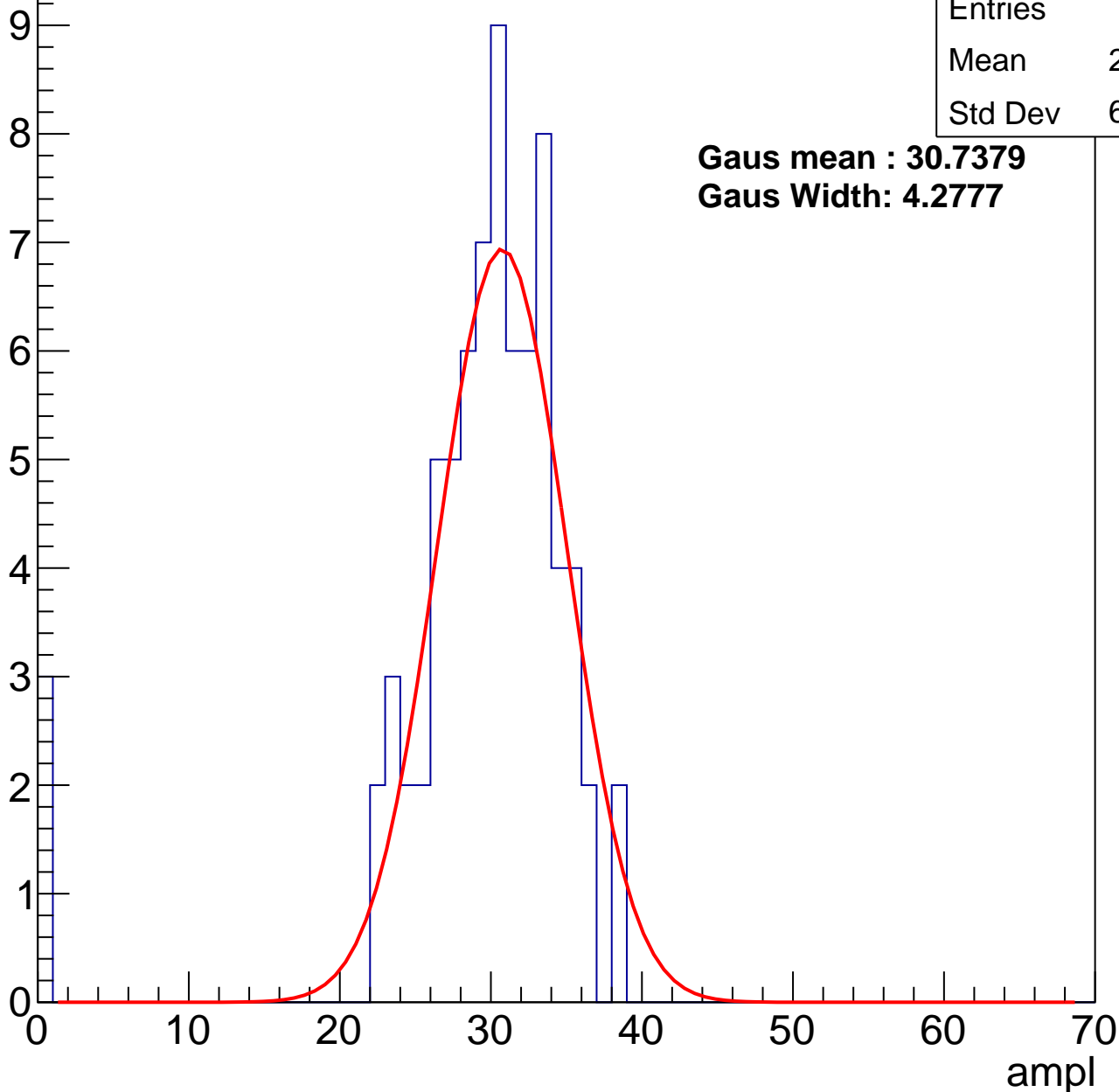
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	28.72
Std Dev	6.878

**Gaus mean : 30.7379**

**Gaus Width: 4.2777**



# B1L101S, U11-ch48, adc1

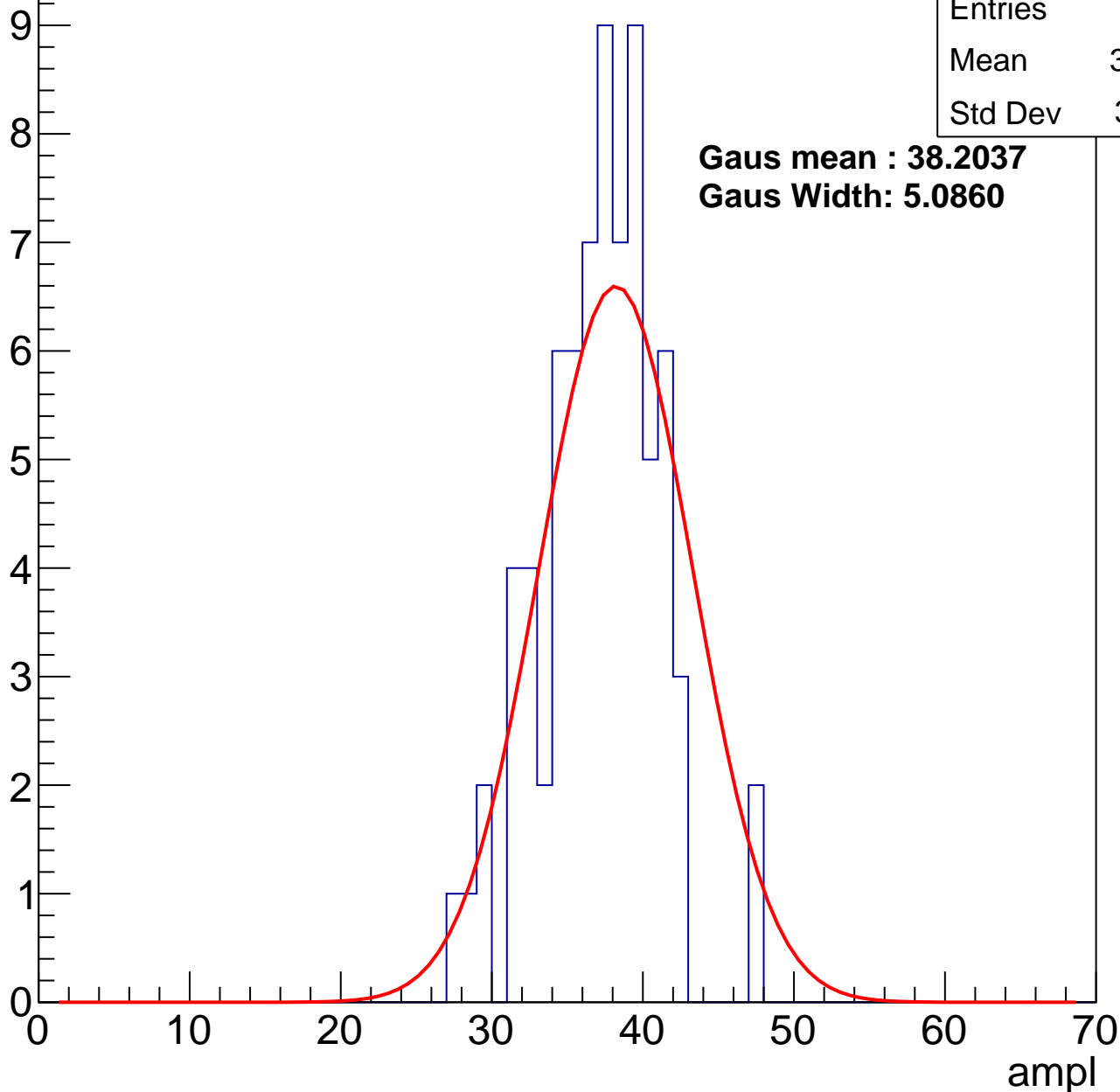
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	36.66
Std Dev	3.891

**Gaus mean : 38.2037**

**Gaus Width: 5.0860**



# B1L101S, U11-ch48, adc2

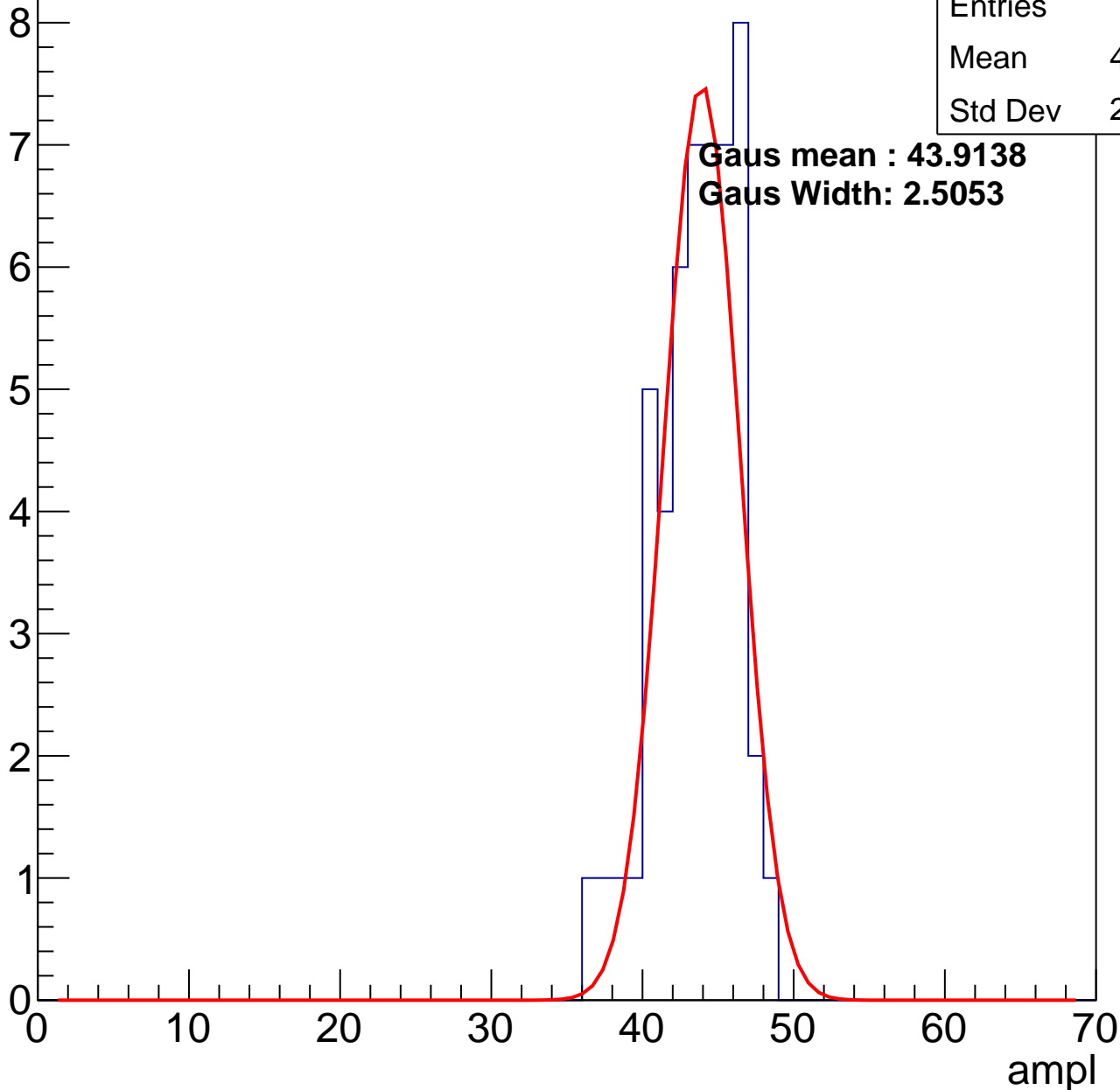
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	43.14
Std Dev	2.642

**Gaus mean : 43.9138**

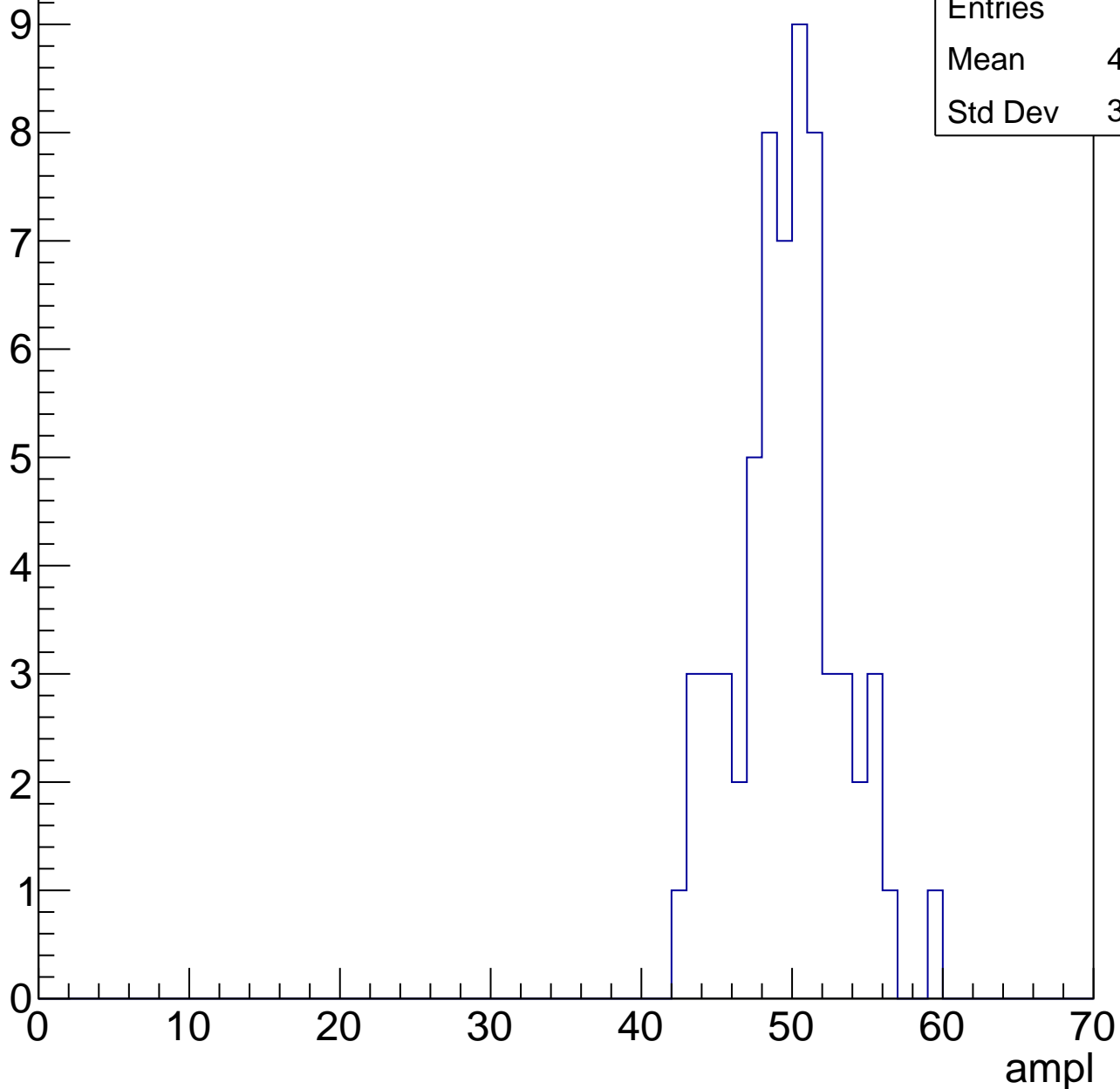
**Gaus Width: 2.5053**



# B1L101S, U11-ch48, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

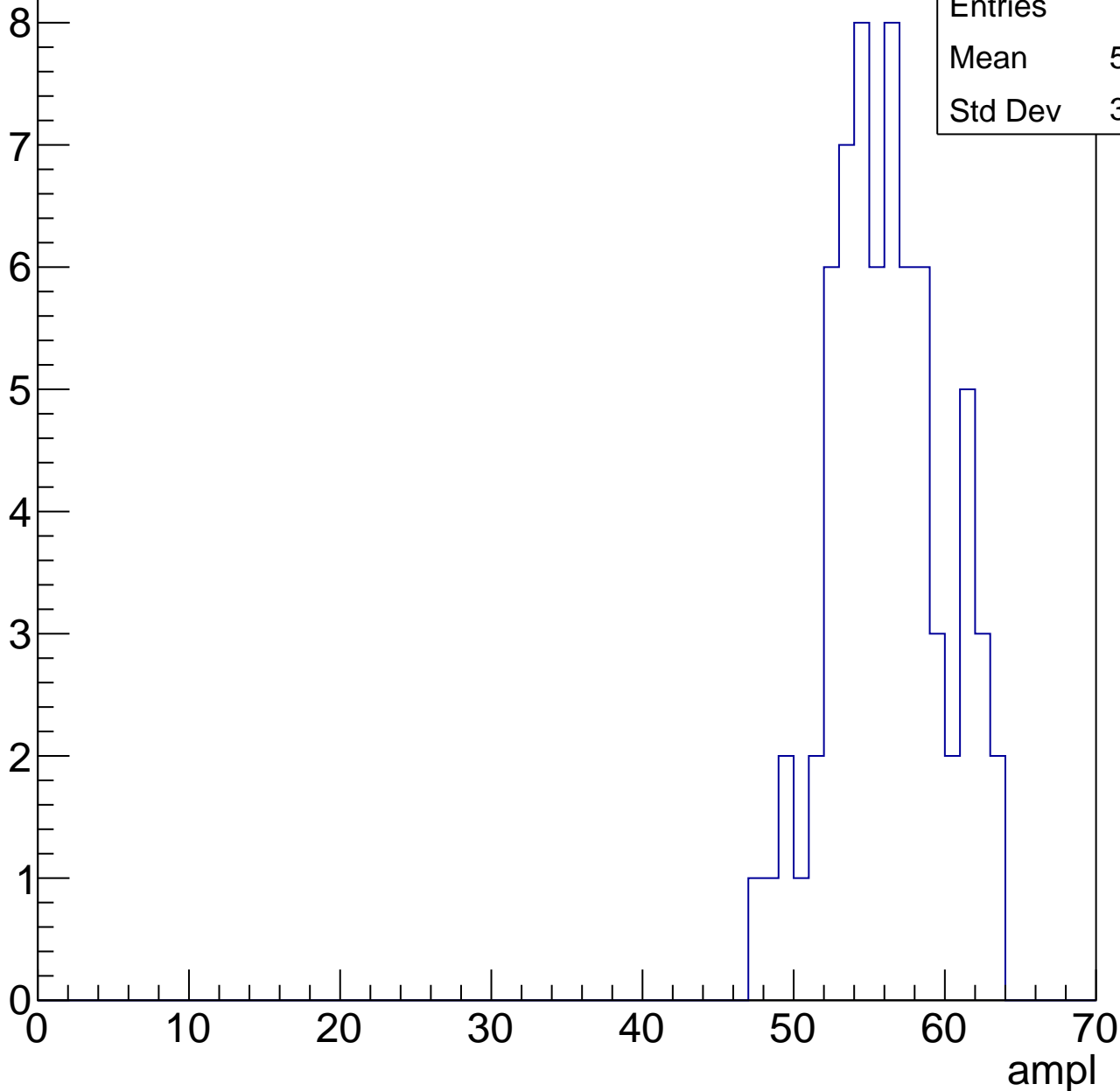


# B1L101S, U11-ch48, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	55.68
Std Dev	3.689



# B1L101S, U11-ch48, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

7

6

5

4

3

2

1

0

Entries

41

Mean

58

Std Dev

9.622

ampl

0

10

20

30

40

50

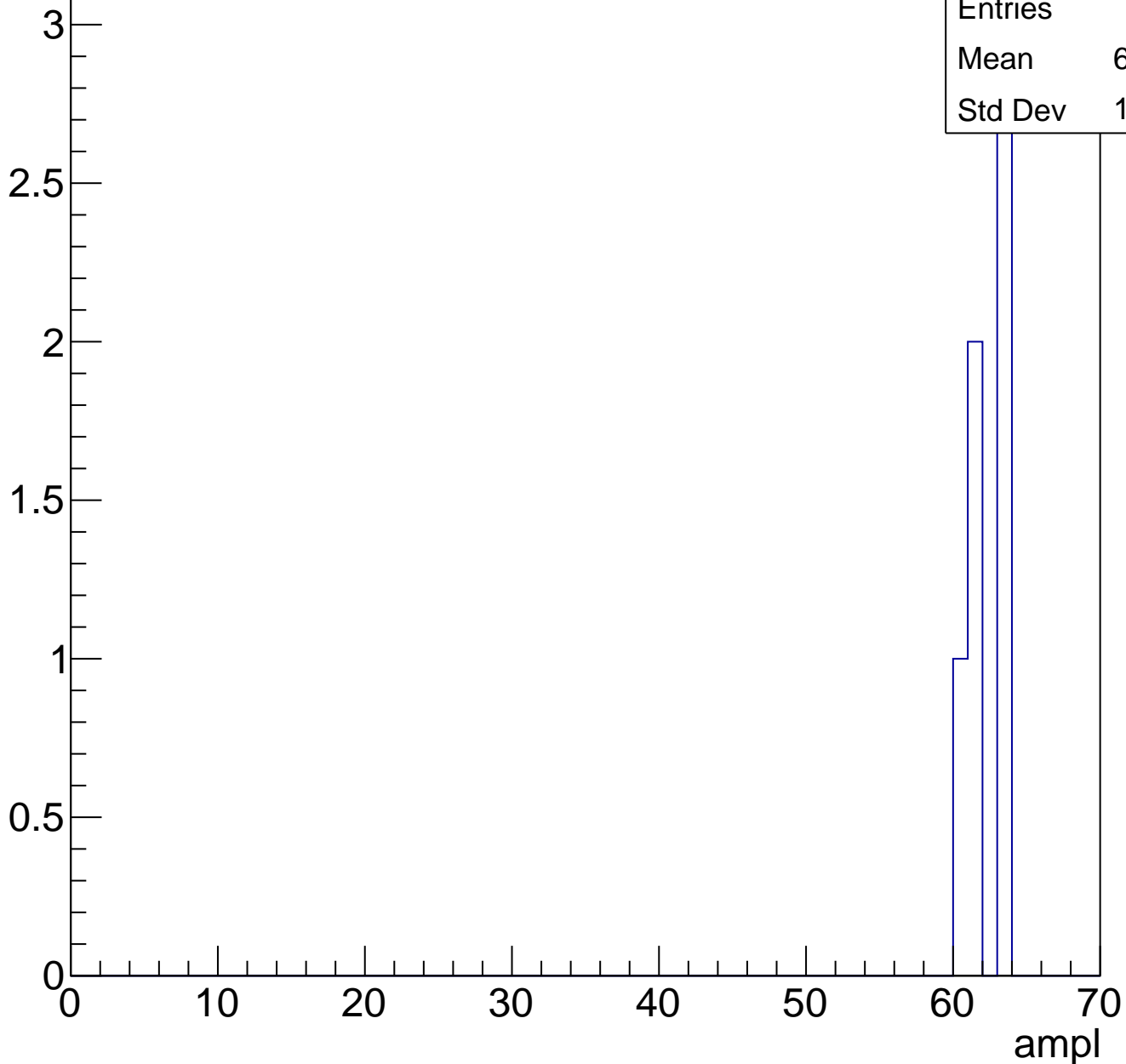
60

70

# B1L101S, U11-ch48, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch48, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	21
Std Dev	0

ampl

0 10 20 30 40 50 60 70

# B1L101S, U11-ch49, adc0

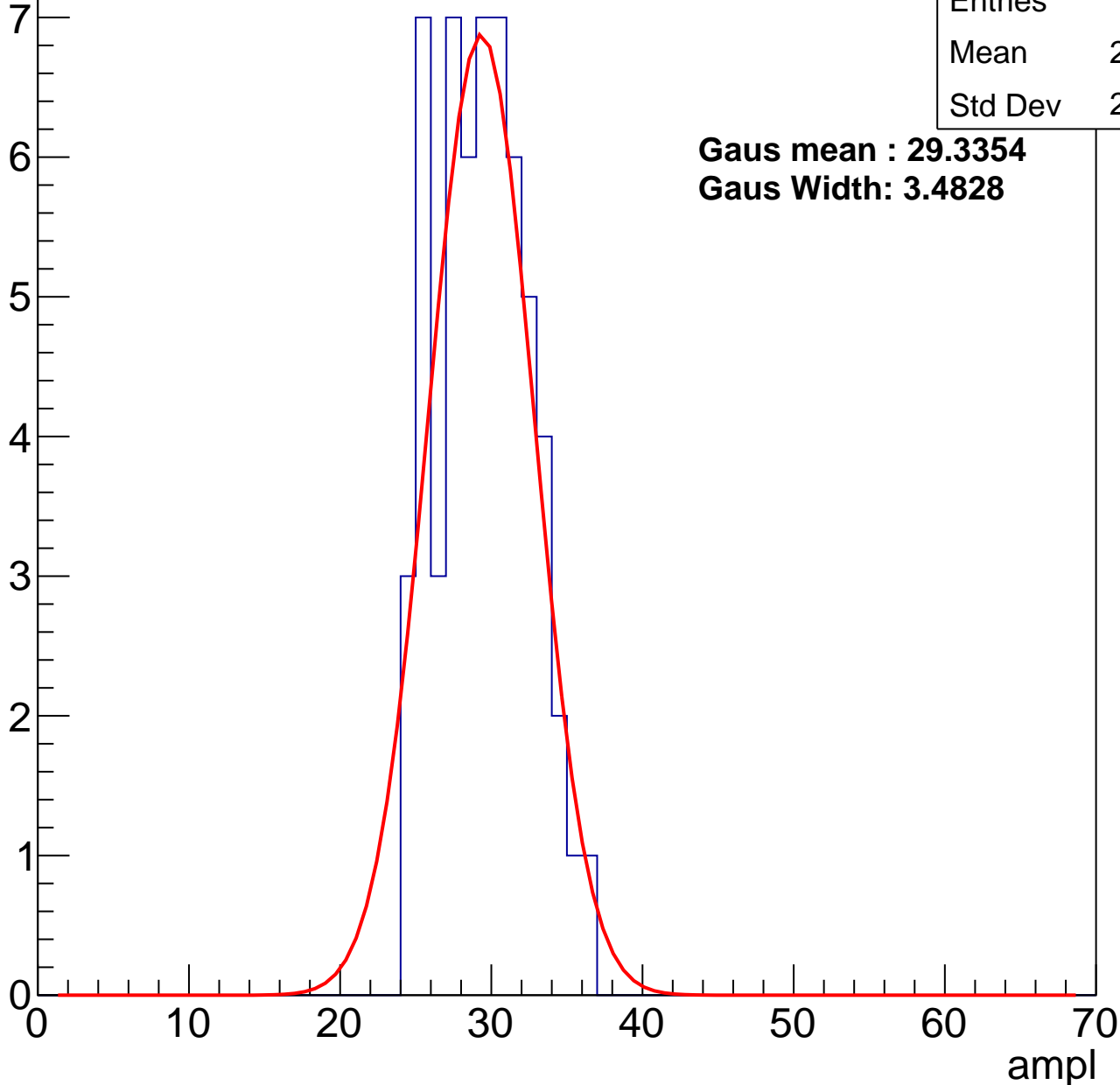
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	29.02
Std Dev	2.977

**Gaus mean : 29.3354**

**Gaus Width: 3.4828**



# B1L101S, U11-ch49, adc1

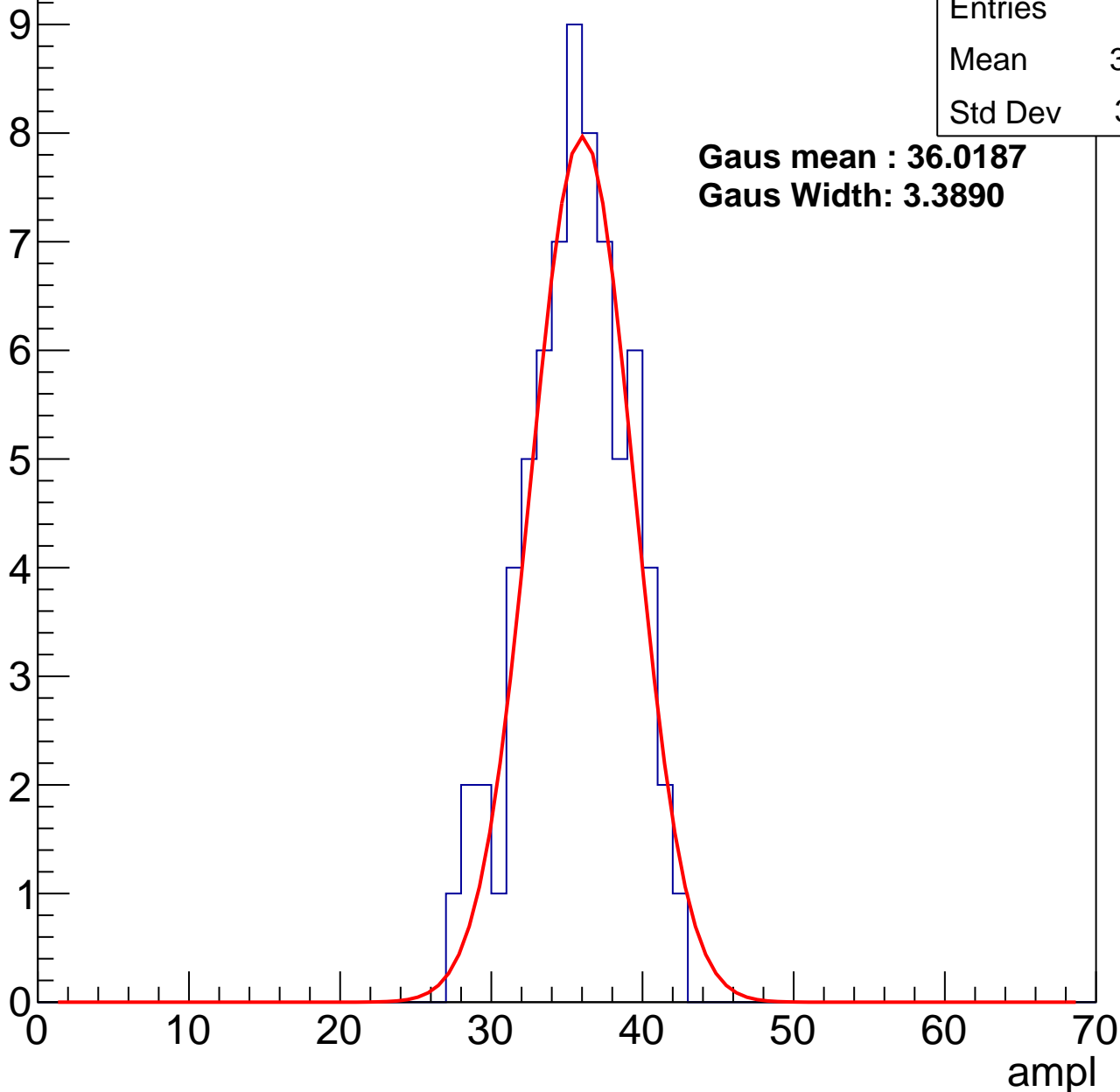
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	35.16
Std Dev	3.371

**Gaus mean : 36.0187**

**Gaus Width: 3.3890**



# B1L101S, U11-ch49, adc2

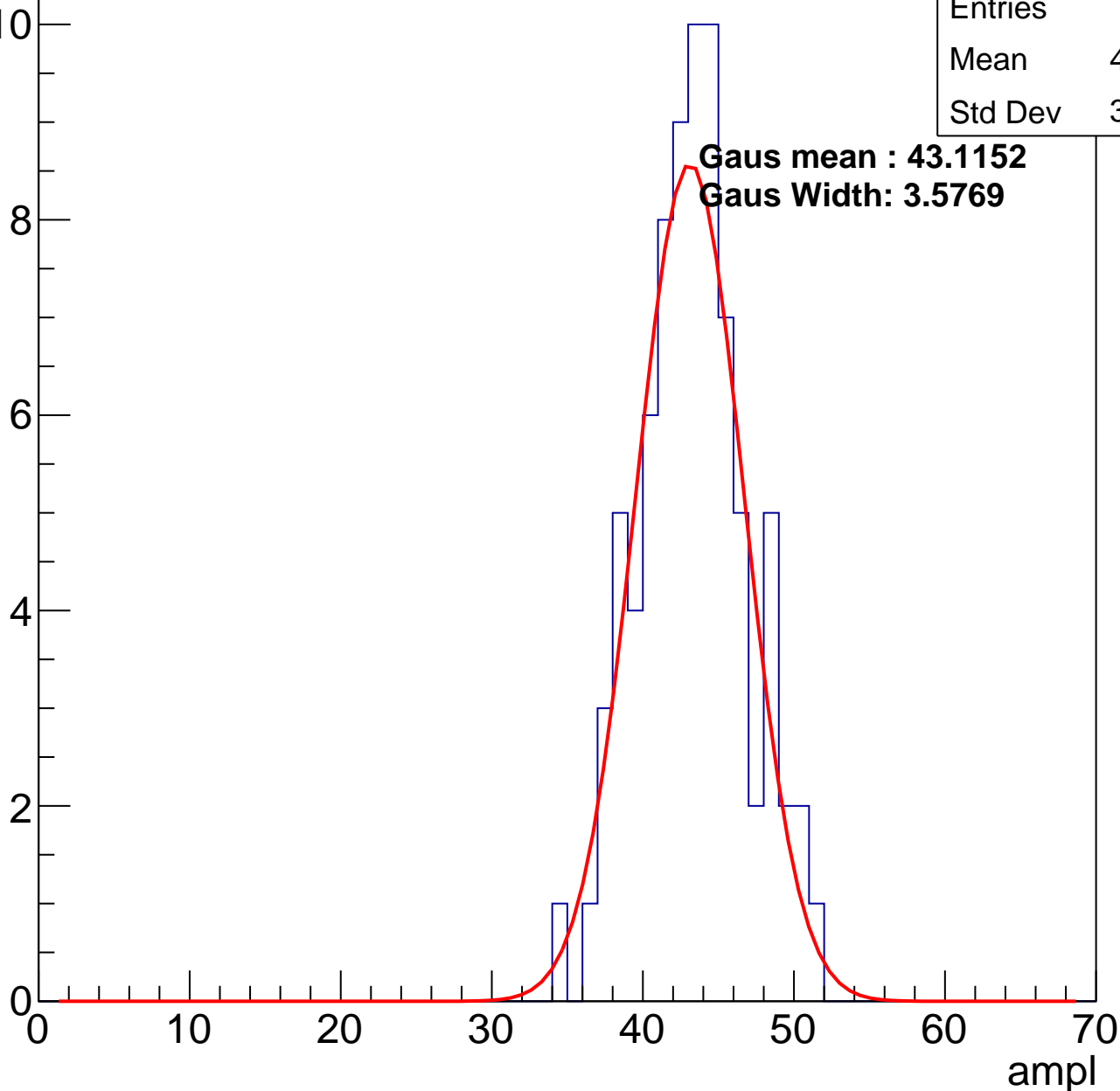
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	81
Mean	42.85
Std Dev	3.503

**Gaus mean : 43.1152**

**Gaus Width: 3.5769**

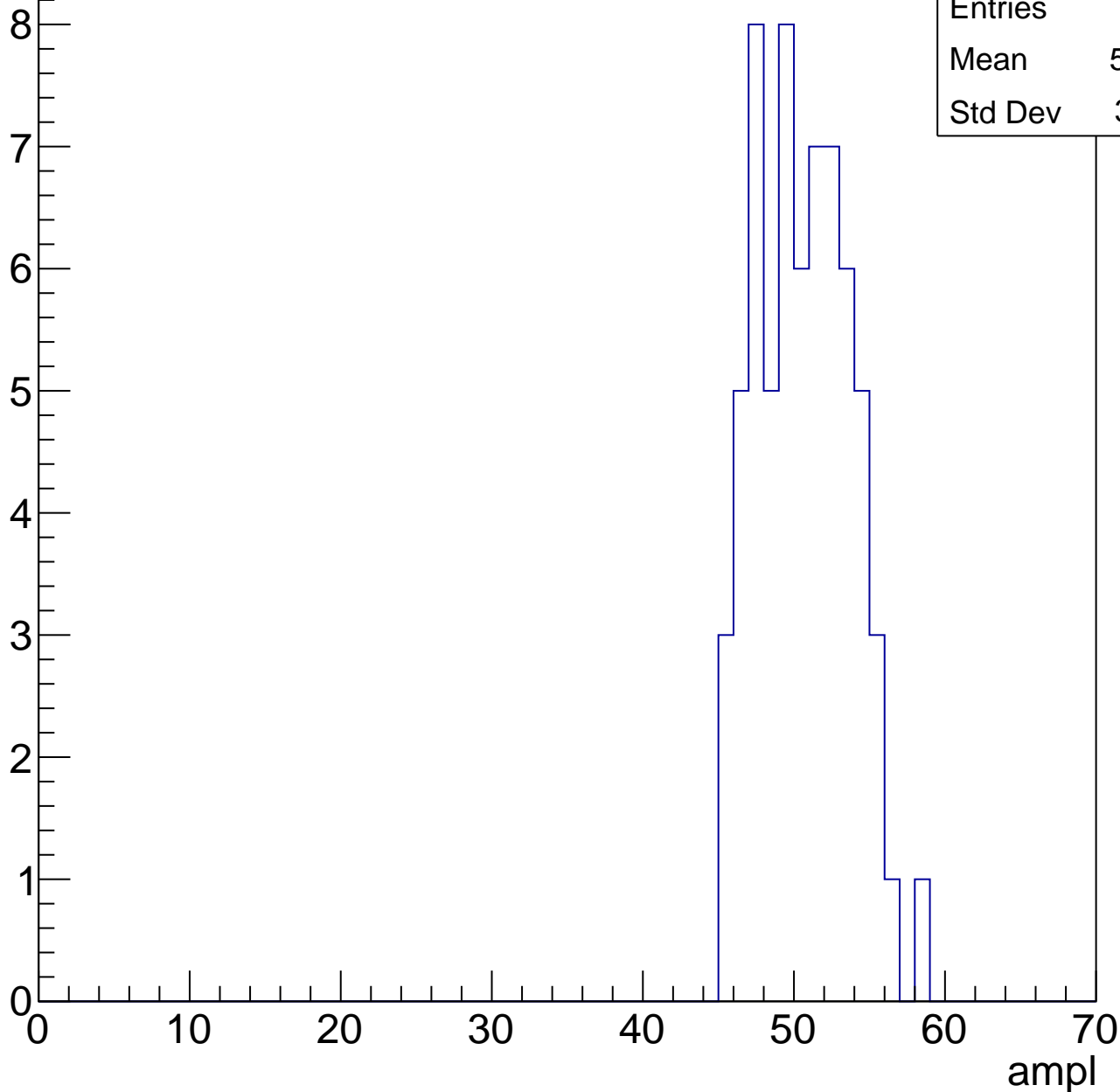


# B1L101S, U11-ch49, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

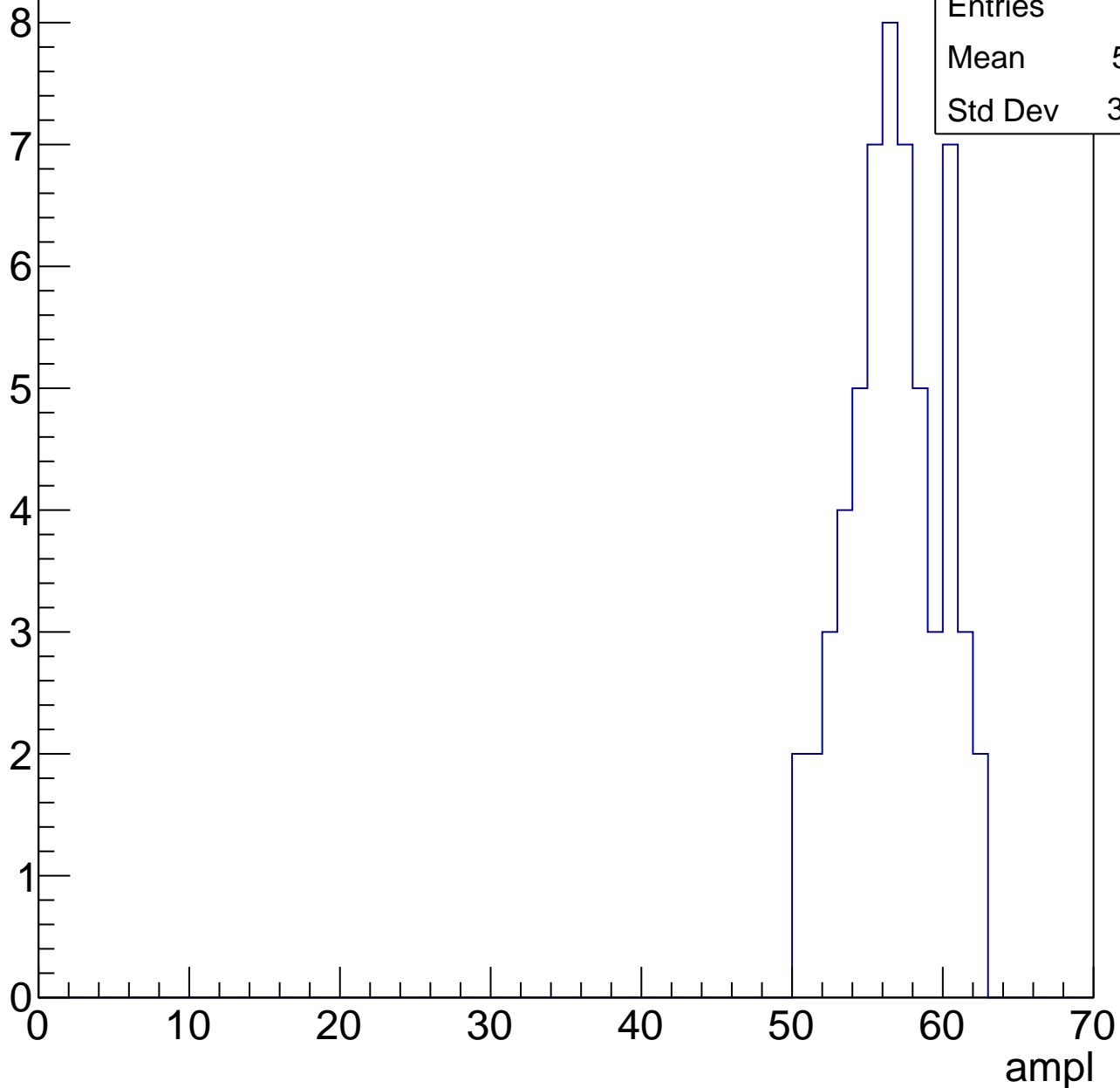
Entries	65
Mean	50.17
Std Dev	3.031



# B1L101S, U11-ch49, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



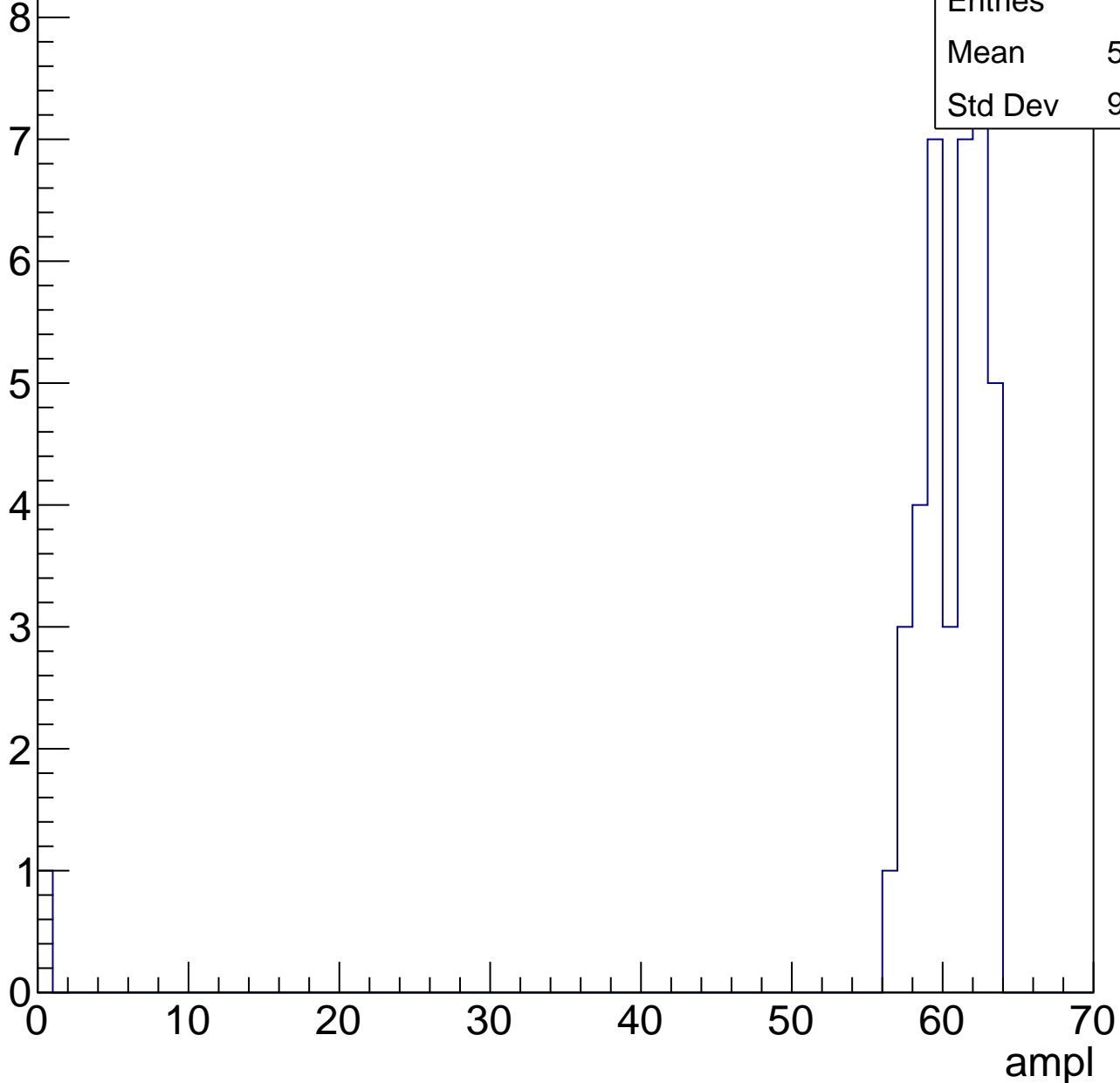
Entries	58
Mean	56.31
Std Dev	3.052

# B1L101S, U11-ch49, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	39
Mean	58.72
Std Dev	9.722



# B1L101S, U11-ch49, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch49, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U11-ch50, adc0

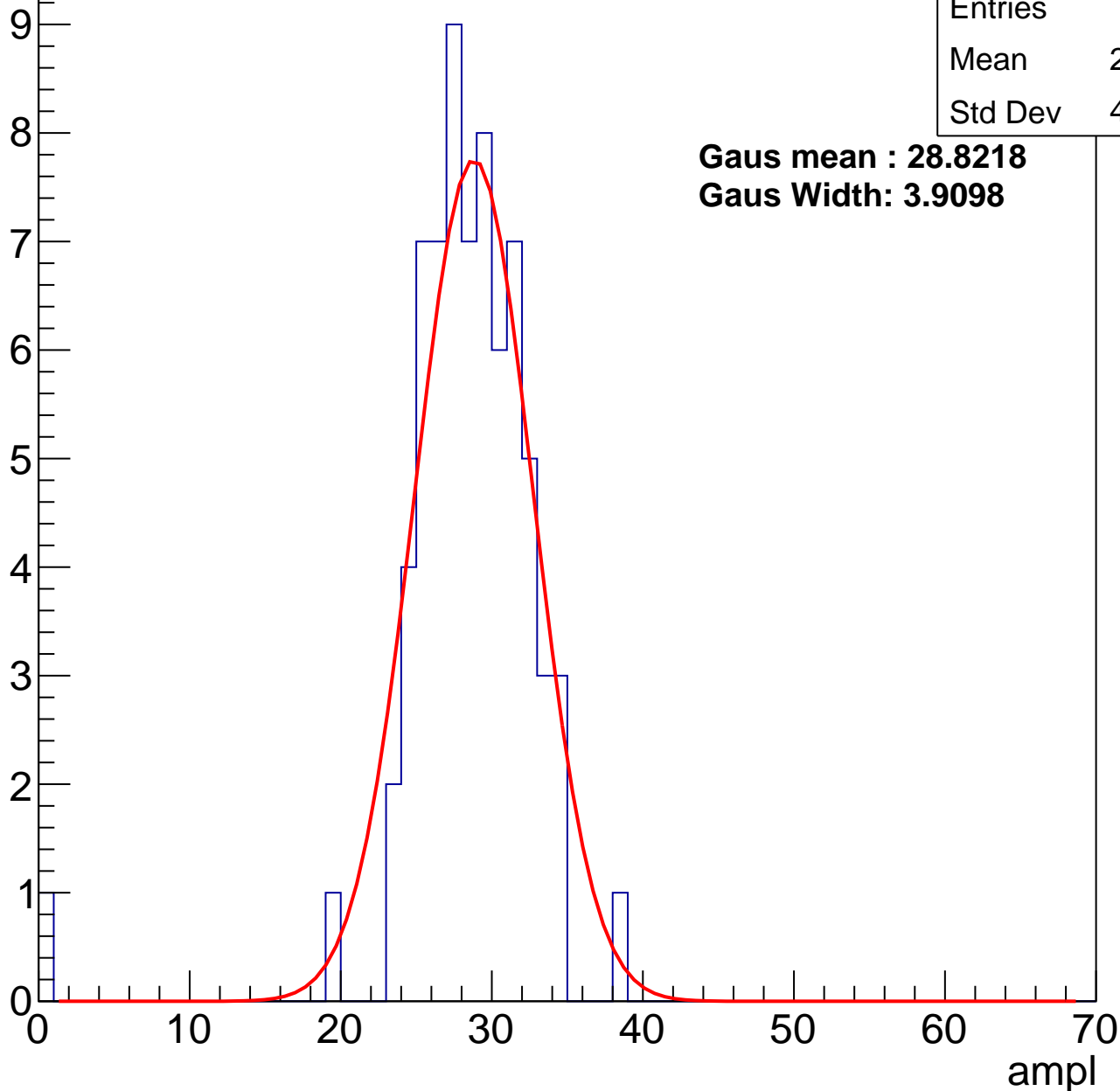
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	27.96
Std Dev	4.653

**Gaus mean : 28.8218**

**Gaus Width: 3.9098**

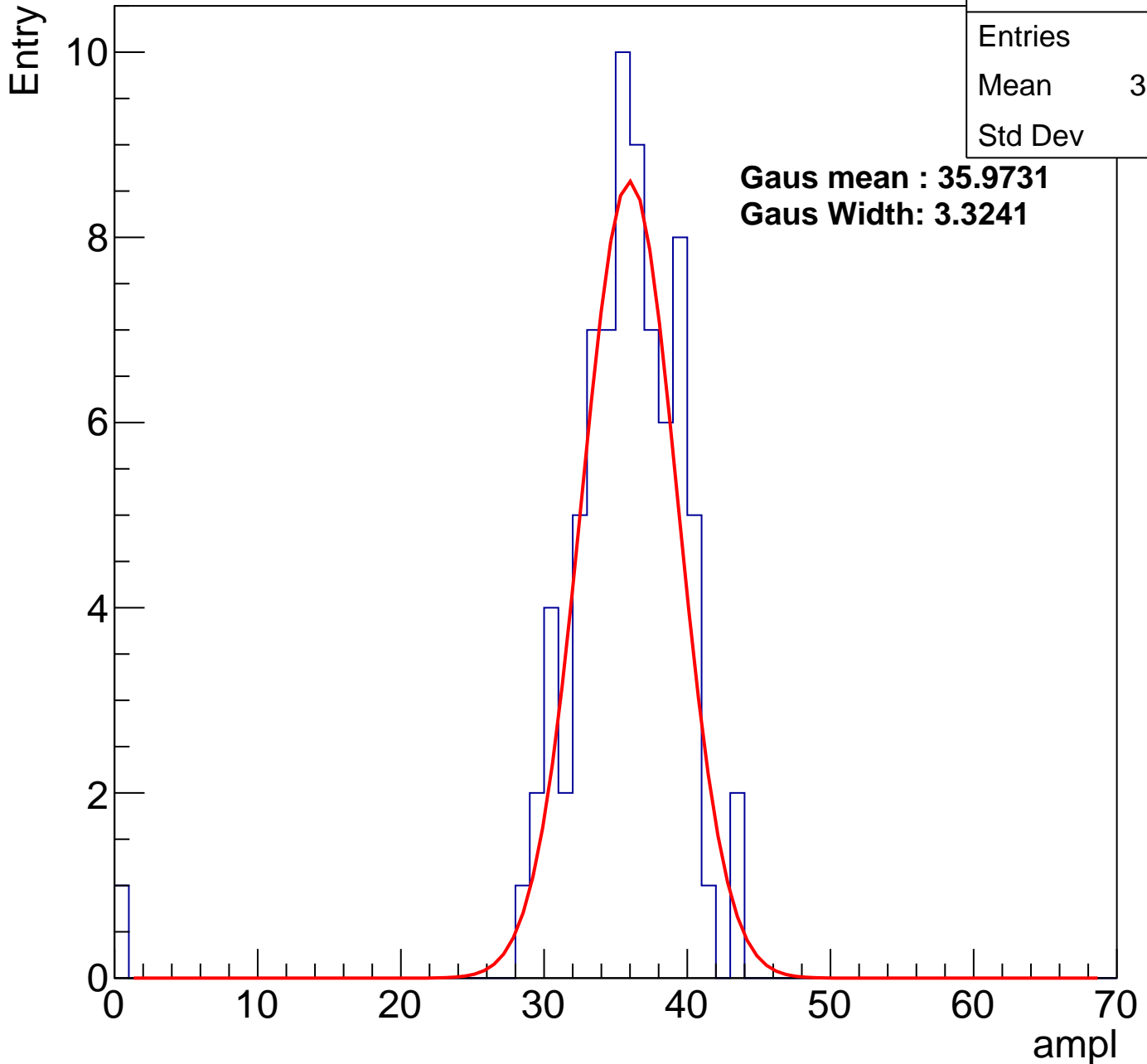


# B1L101S, U11-ch50, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	77
Mean	35.03
Std Dev	5.18

**Gaus mean : 35.9731**  
**Gaus Width: 3.3241**



# B1L101S, U11-ch50, adc2

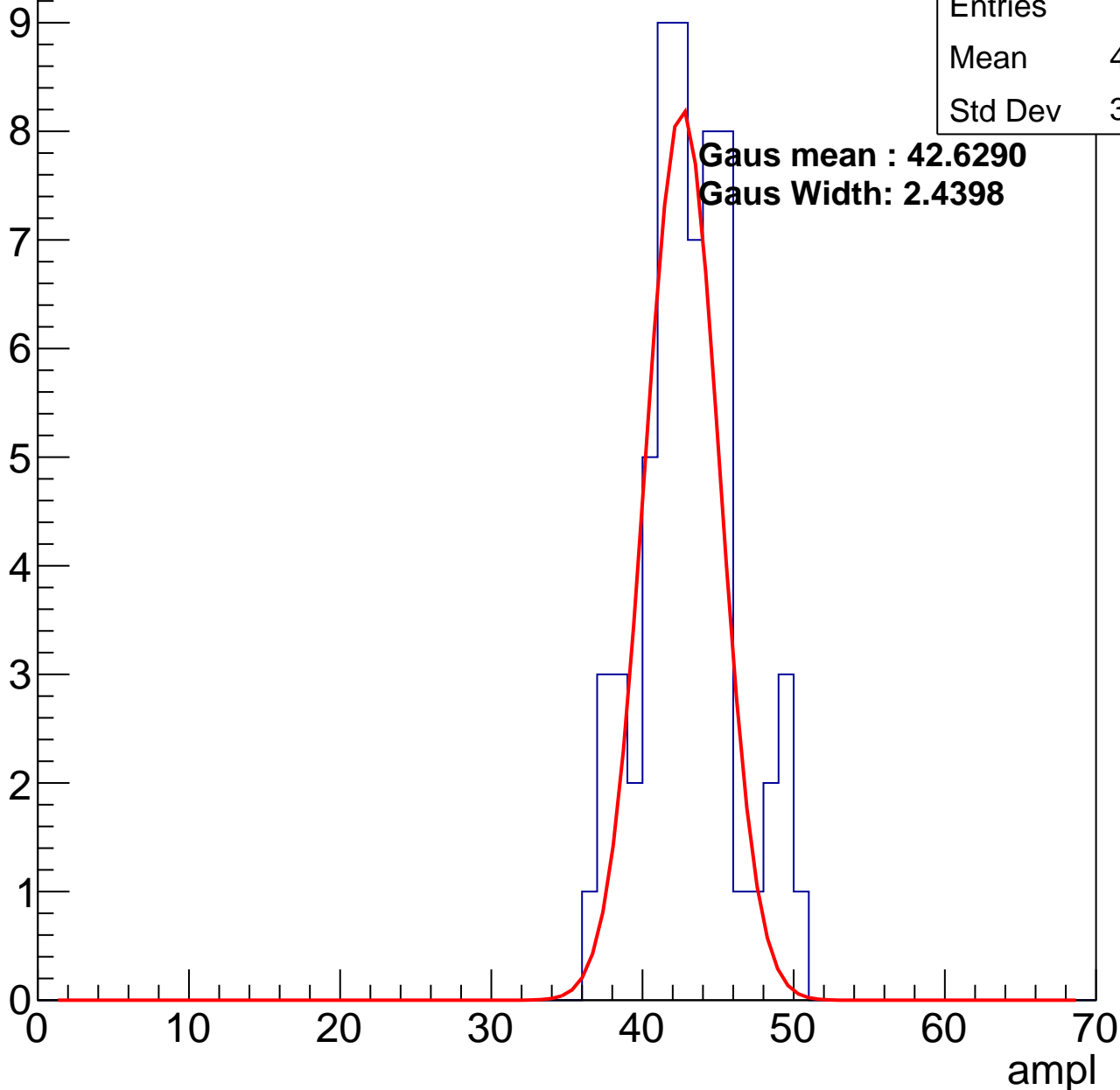
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	42.62
Std Dev	3.129

**Gaus mean : 42.6290**

**Gaus Width: 2.4398**

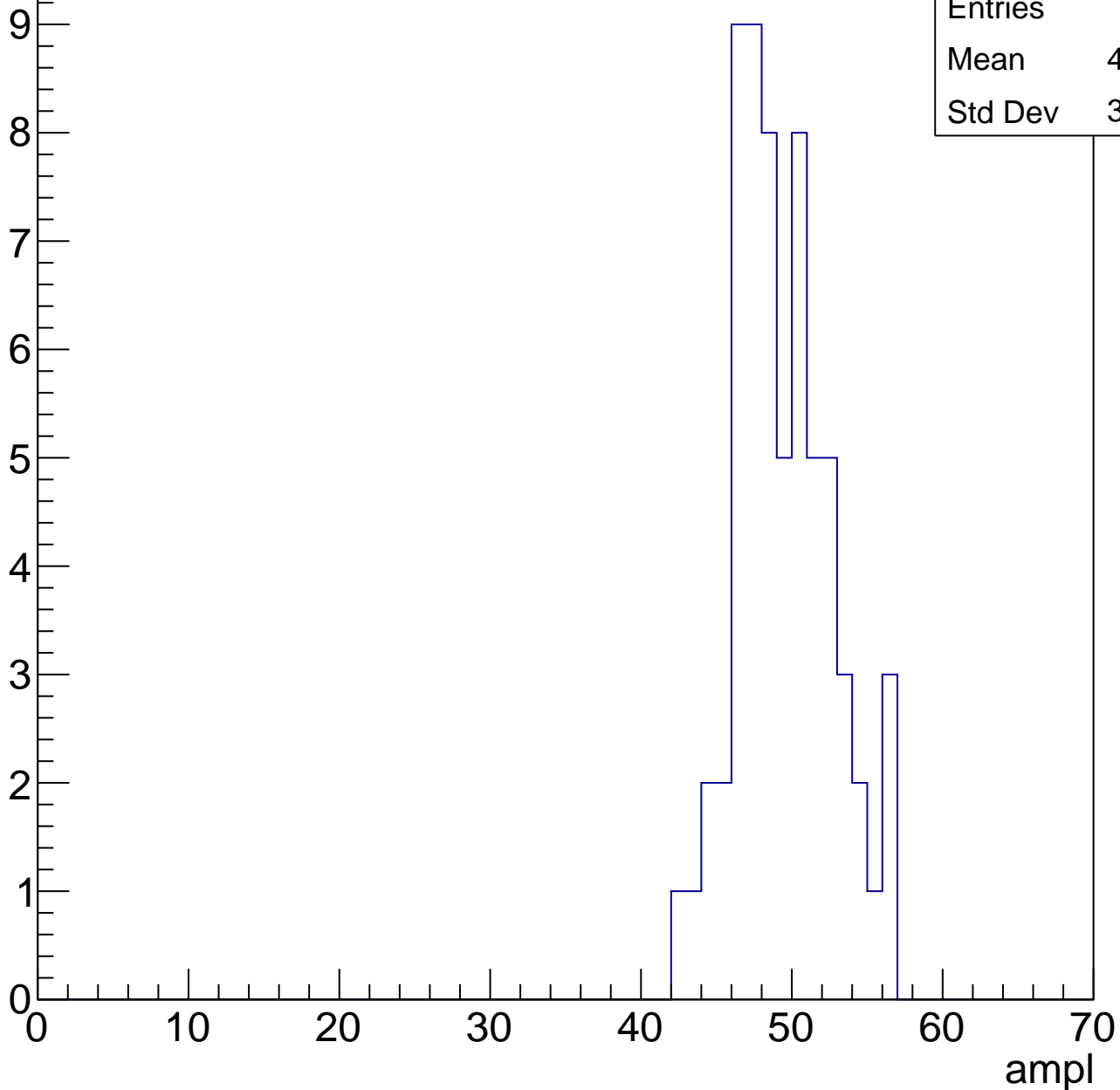


# B1L101S, U11-ch50, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	48.97
Std Dev	3.177

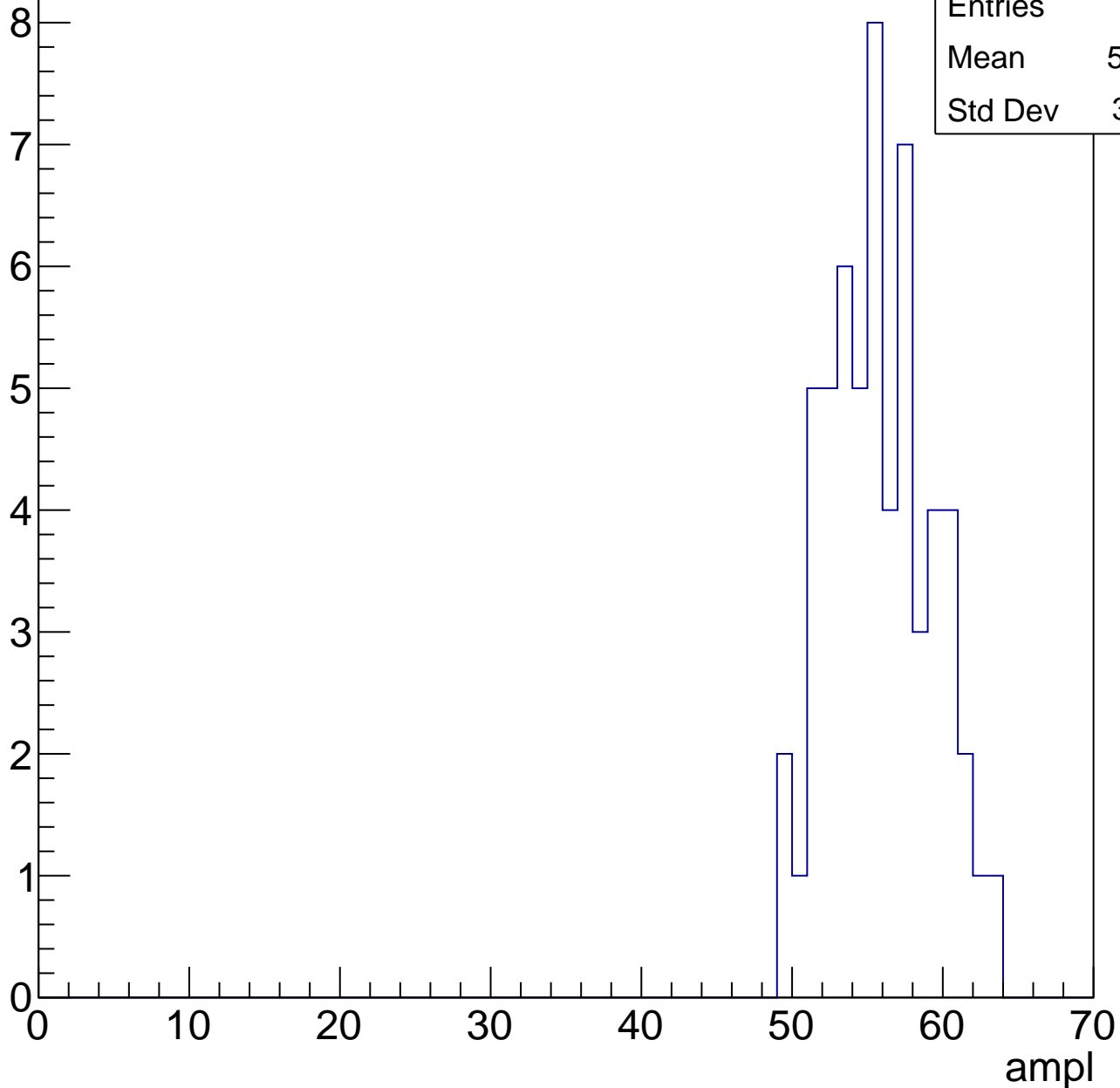


# B1L101S, U11-ch50, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	55.36
Std Dev	3.351

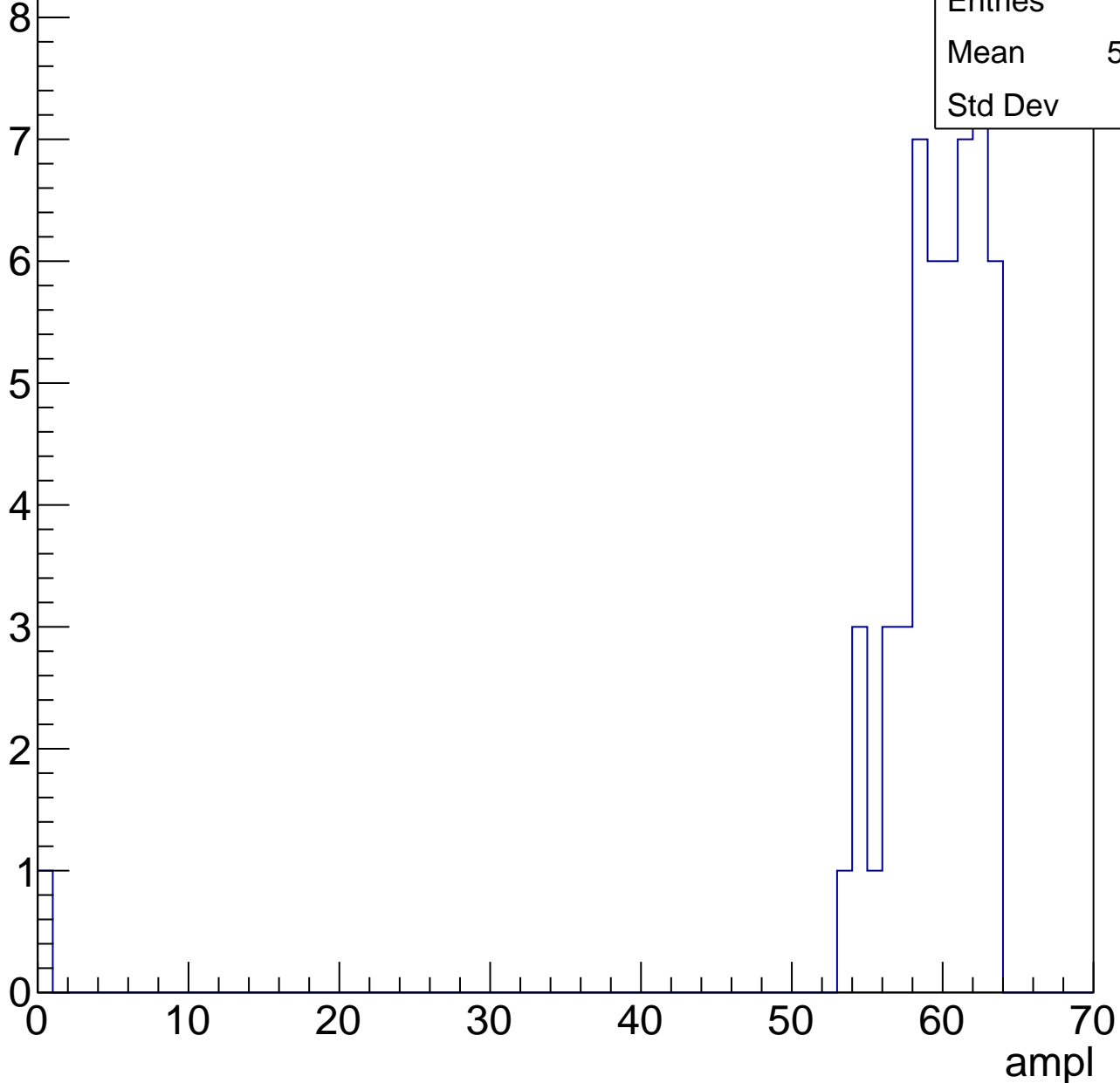


# B1L101S, U11-ch50, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	58.27
Std Dev	8.58



# B1L101S, U11-ch50, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch50, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U11-ch51, adc0

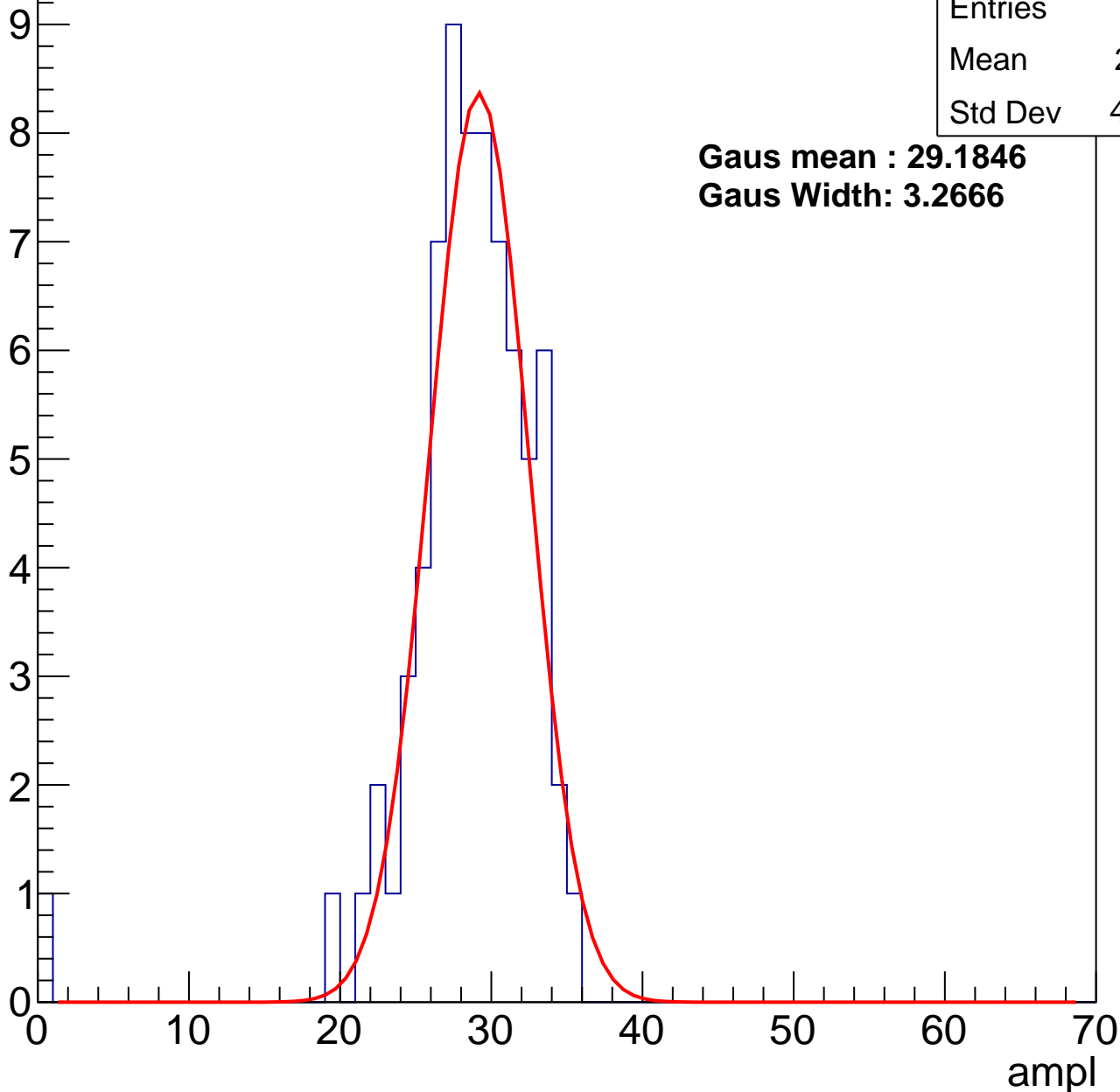
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	28.01
Std Dev	4.674

**Gaus mean : 29.1846**

**Gaus Width: 3.2666**



# B1L101S, U11-ch51, adc1

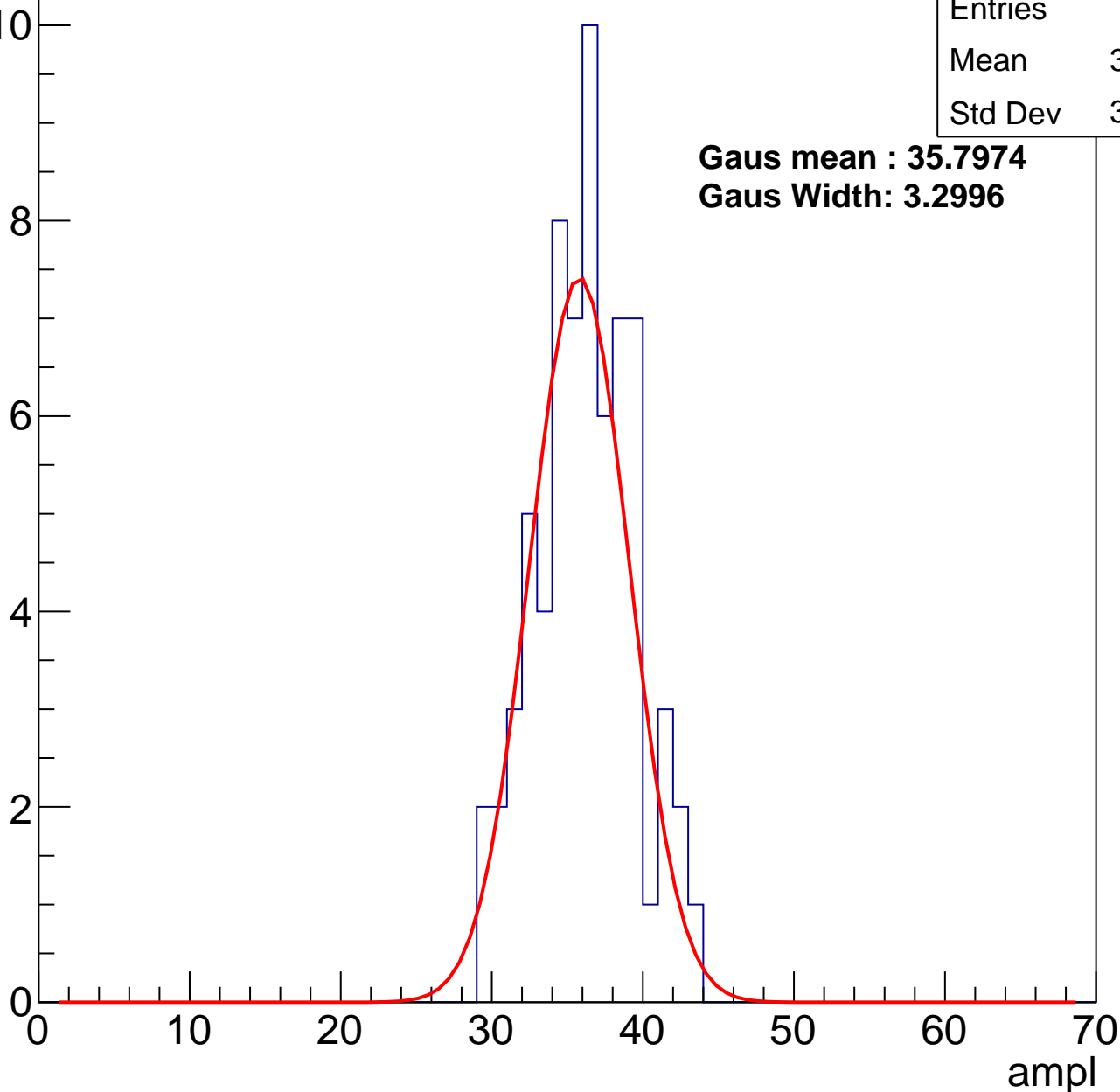
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	35.75
Std Dev	3.219

**Gaus mean : 35.7974**

**Gaus Width: 3.2996**



# B1L101S, U11-ch51, adc2

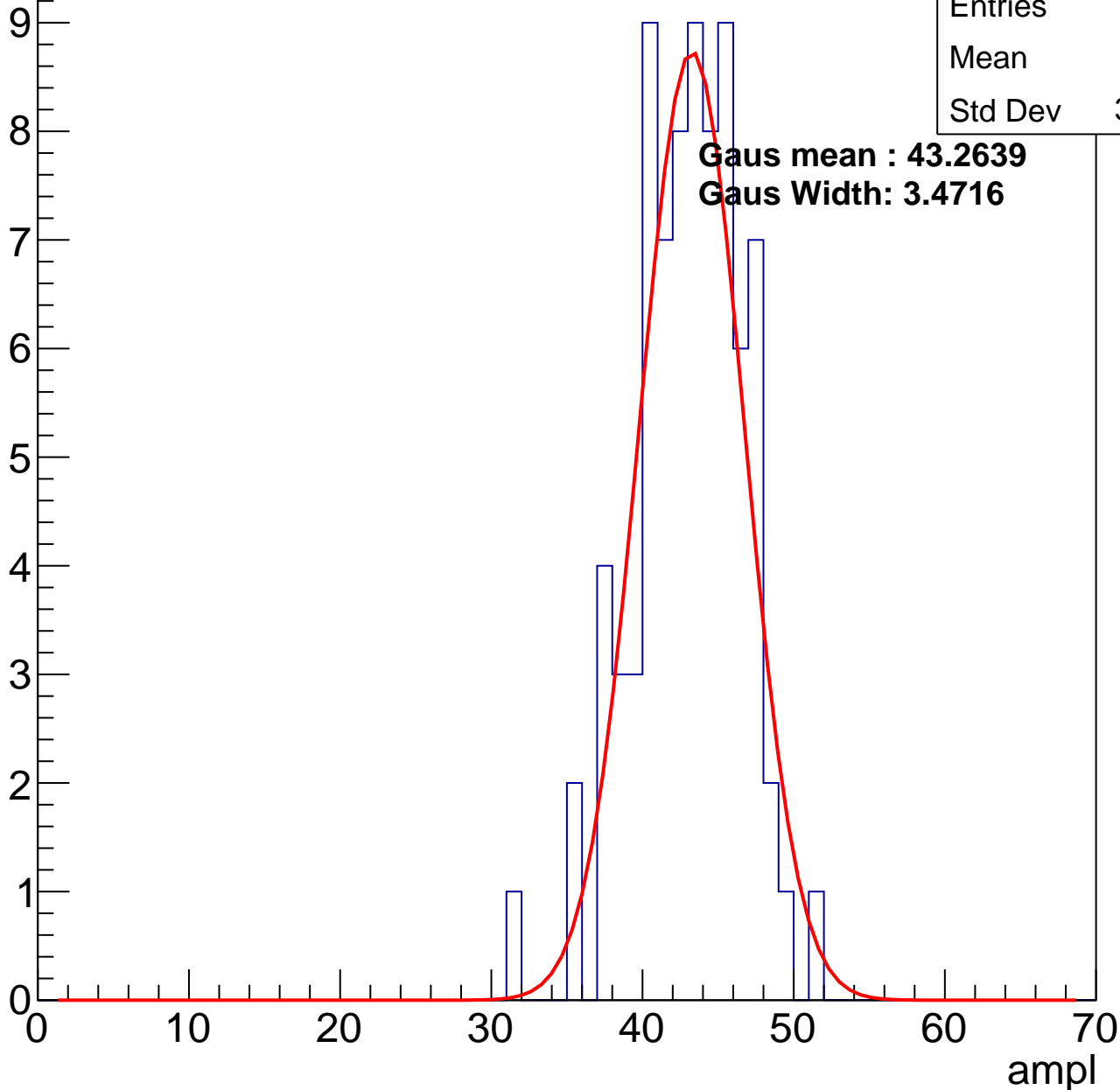
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	80
Mean	42.6
Std Dev	3.541

**Gaus mean : 43.2639**

**Gaus Width: 3.4716**

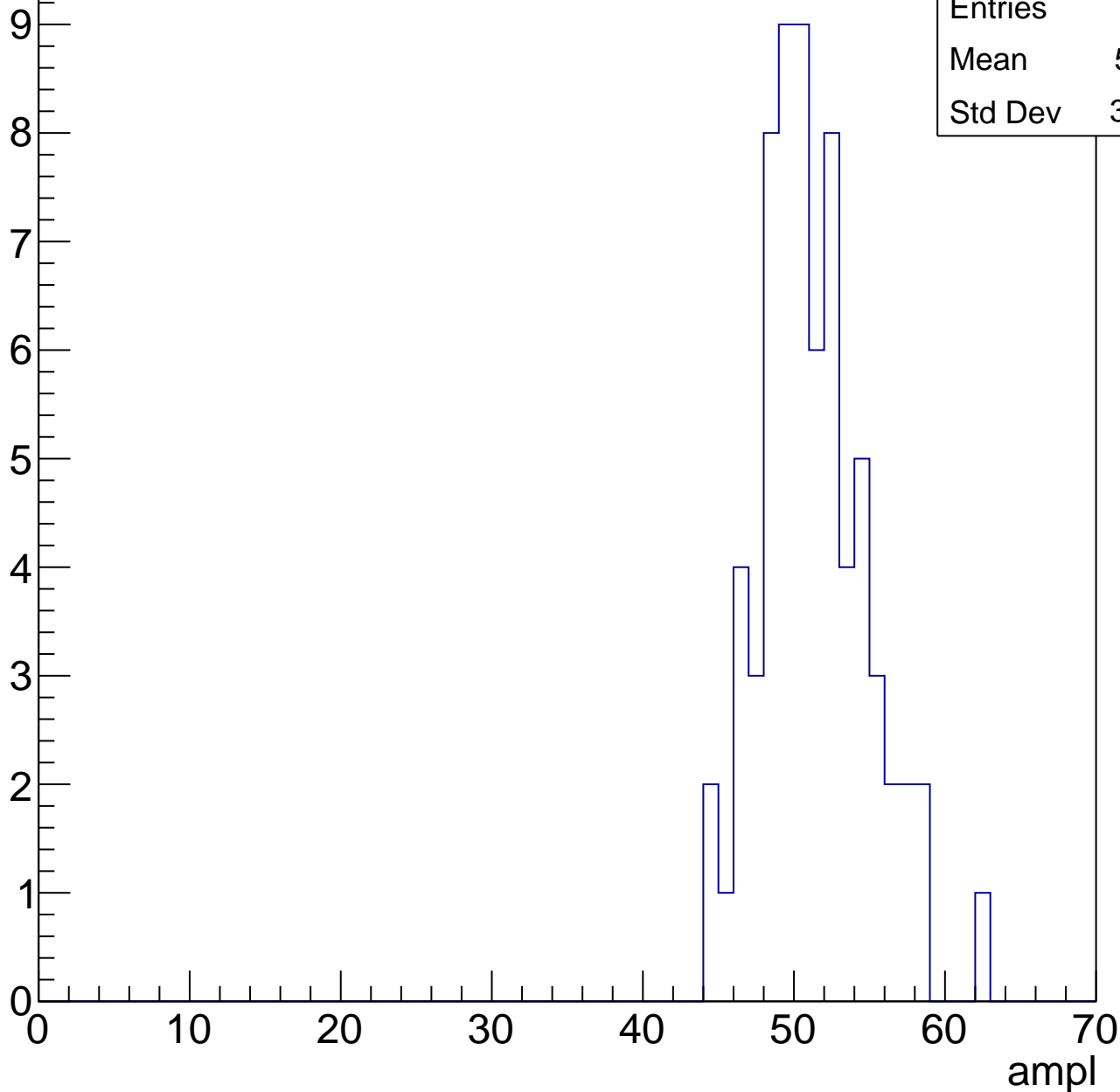


# B1L101S, U11-ch51, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	50.81
Std Dev	3.519



# B1L101S, U11-ch51, adc4

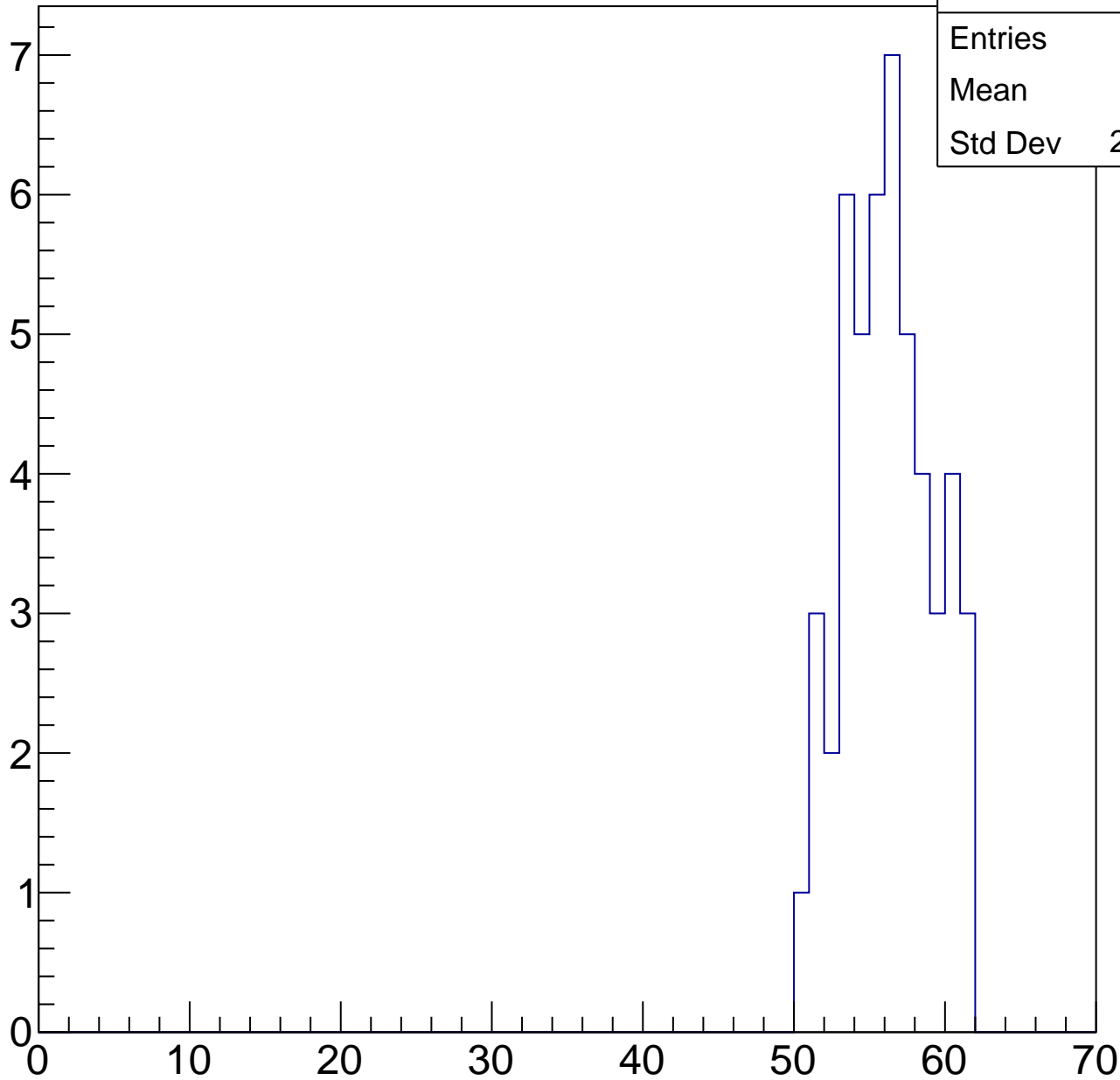
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

7  
6  
5  
4  
3  
2  
1  
0

Entries	49
Mean	55.8
Std Dev	2.885

ampl

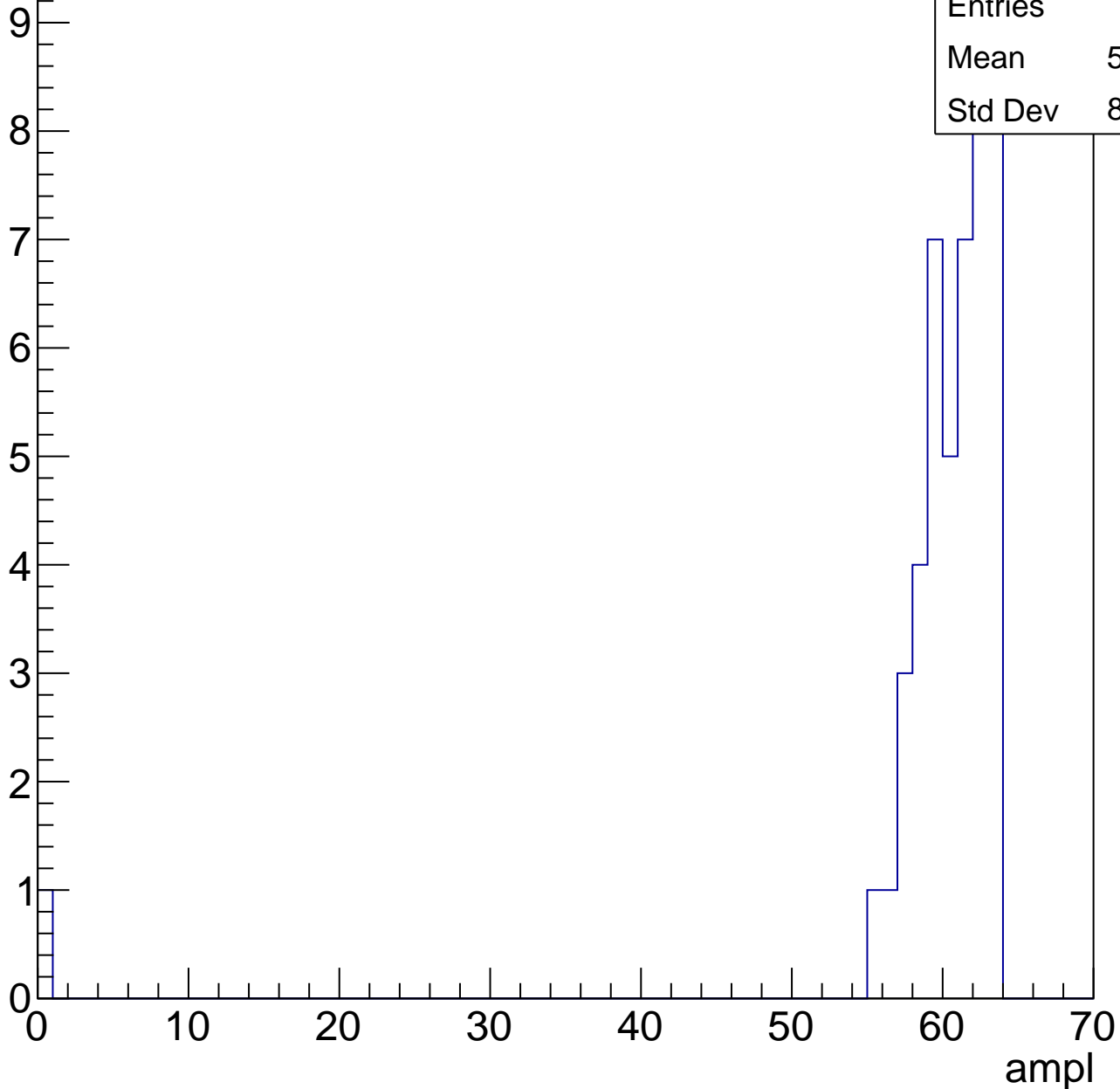


# B1L101S, U11-ch51, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	47
Mean	59.13
Std Dev	8.967



# B1L101S, U11-ch51, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch51, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U11-ch52, adc0

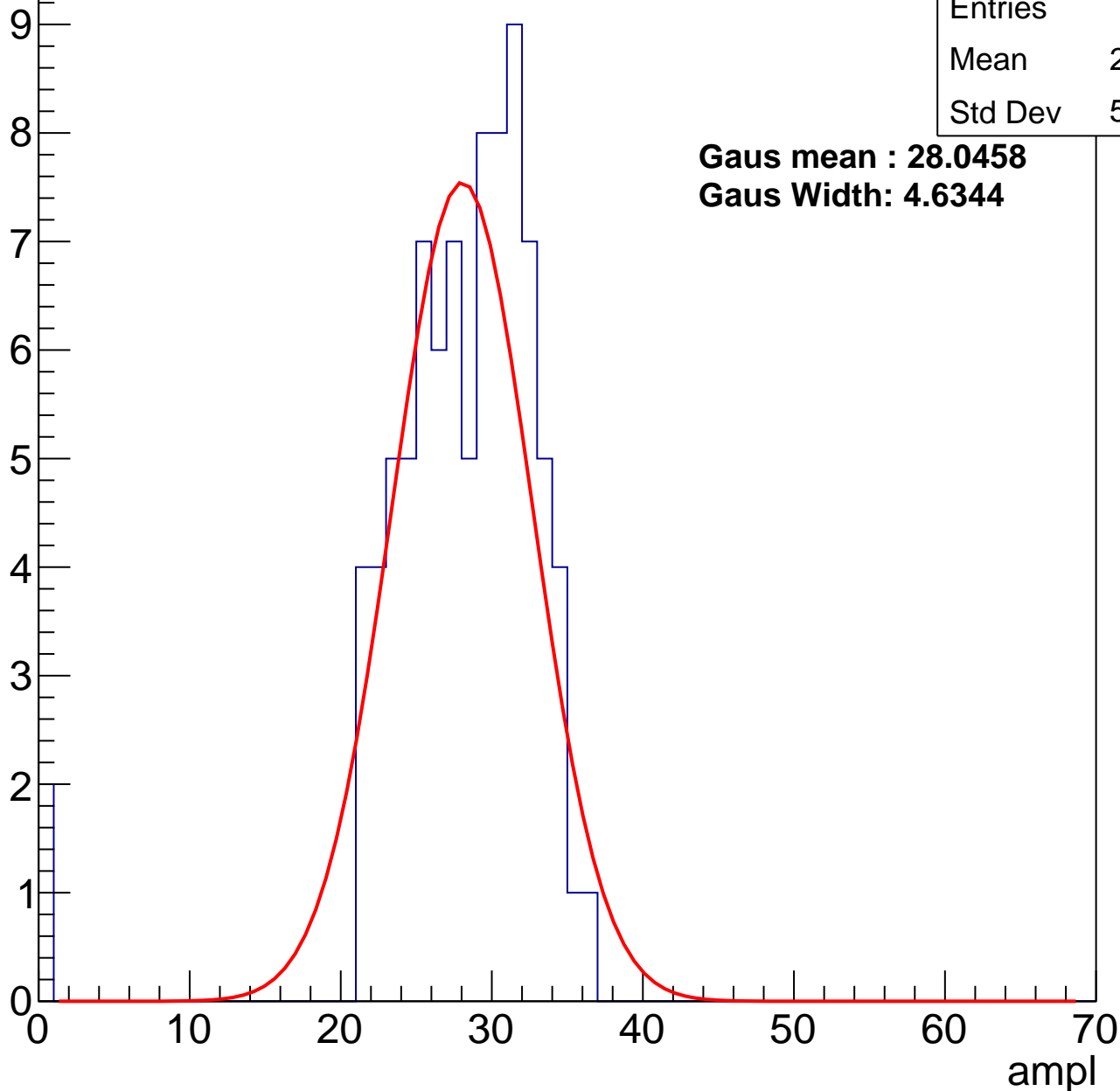
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	88
Mean	27.43
Std Dev	5.634

**Gaus mean : 28.0458**

**Gaus Width: 4.6344**



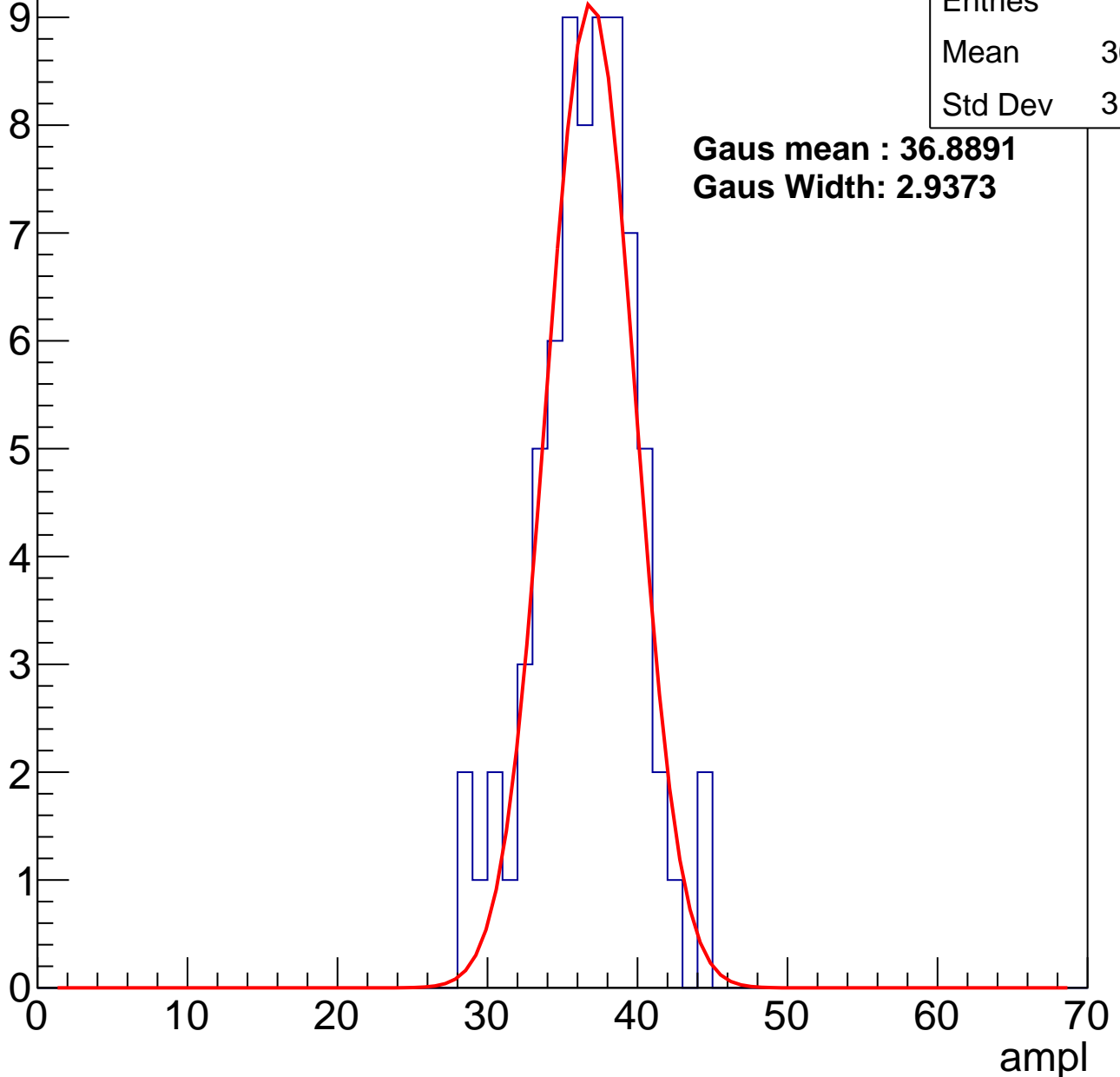
# B1L101S, U11-ch52, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	36.17
Std Dev	3.333

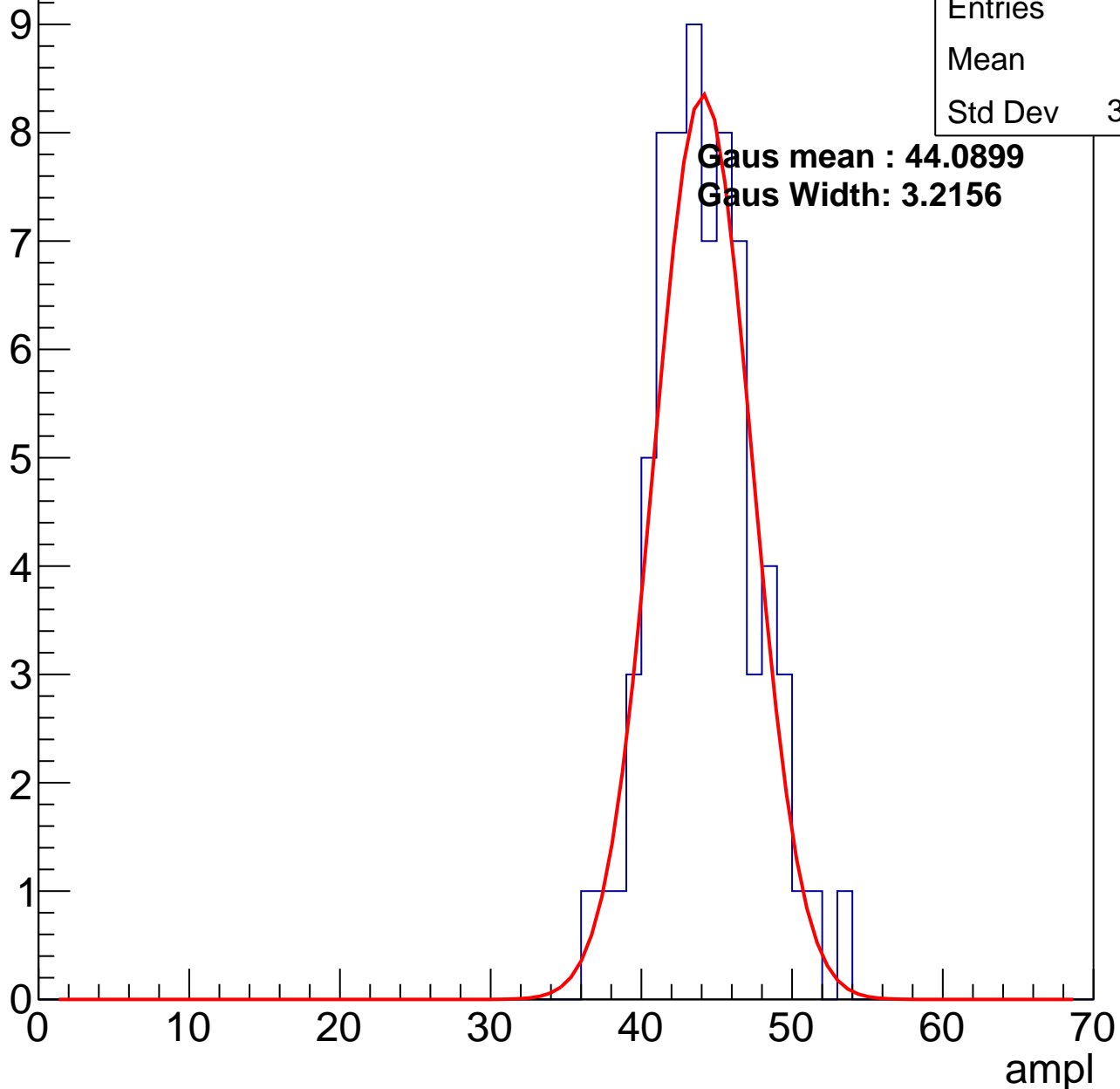
**Gaus mean : 36.8891**  
**Gaus Width: 2.9373**



# B1L101S, U11-ch52, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	71
Mean	43.7
Std Dev	3.312

**Gaus mean : 44.0899**

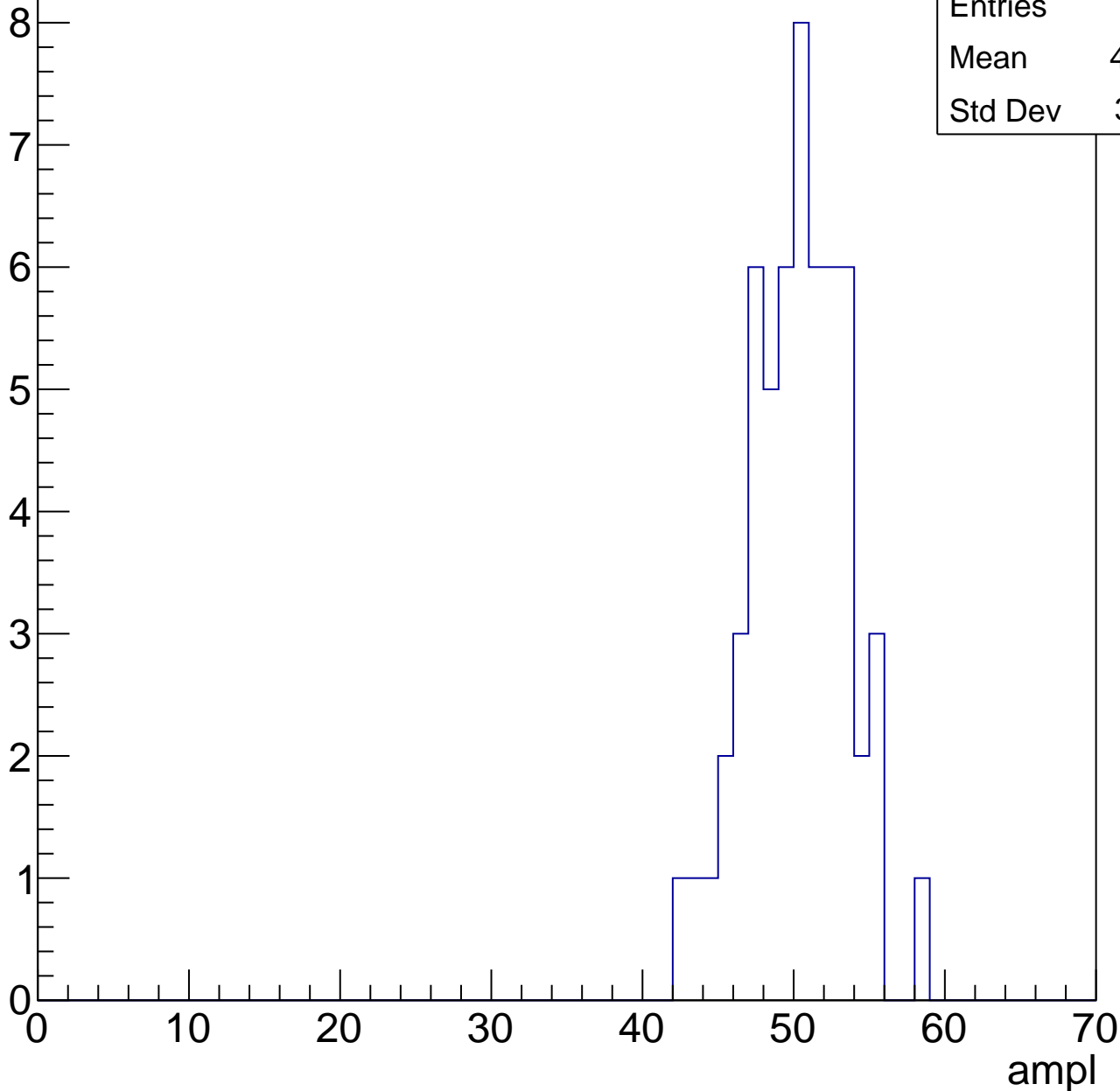
**Gaus Width: 3.2156**

# B1L101S, U11-ch52, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	49.82
Std Dev	3.191

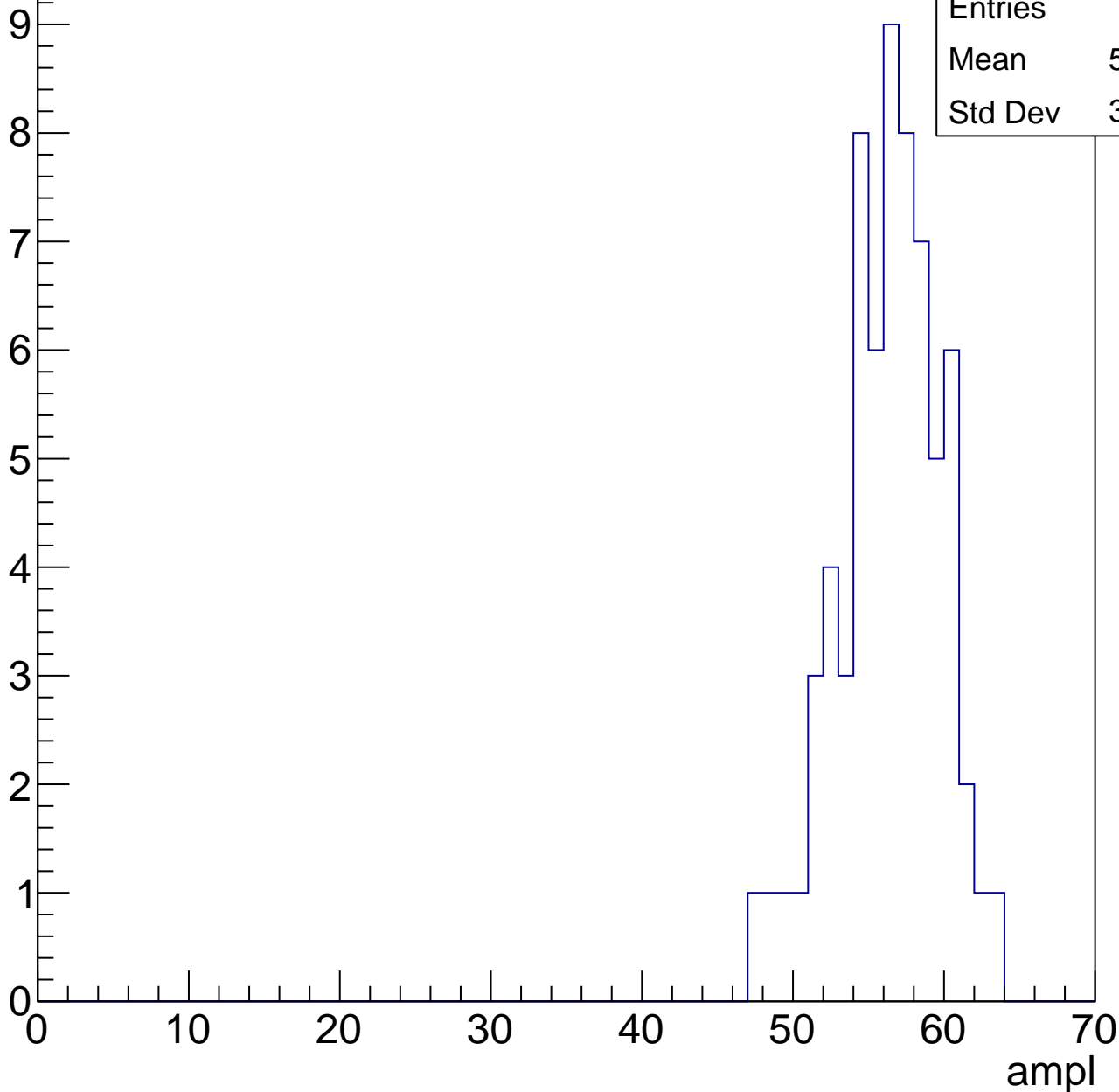


# B1L101S, U11-ch52, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	55.88
Std Dev	3.335



# B1L101S, U11-ch52, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

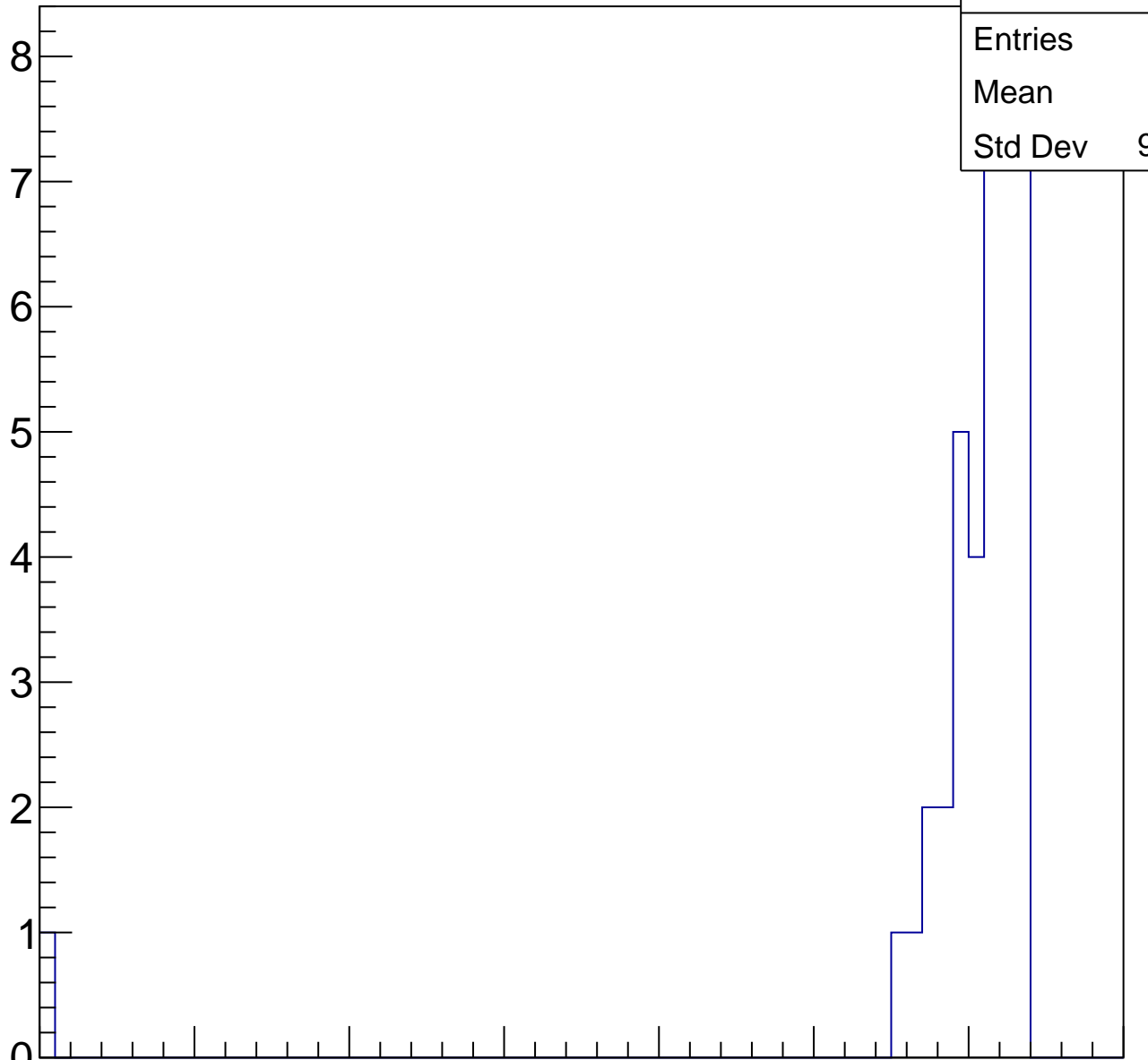
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	40
Mean	59.1
Std Dev	9.685

ampl

0 10 20 30 40 50 60 70



# B1L101S, U11-ch52, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch52, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U11-ch53, adc0

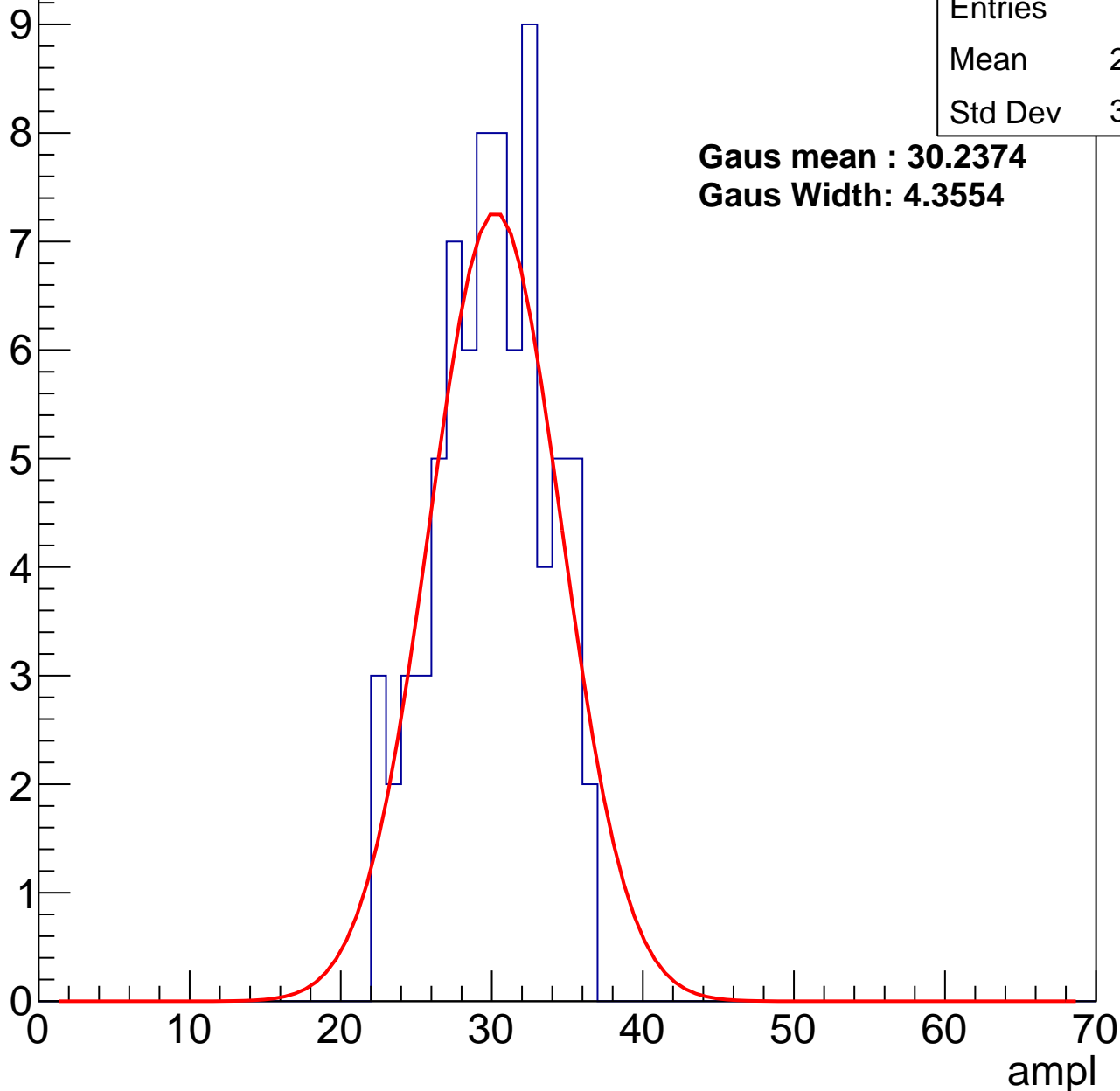
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	29.49
Std Dev	3.596

**Gaus mean : 30.2374**

**Gaus Width: 4.3554**



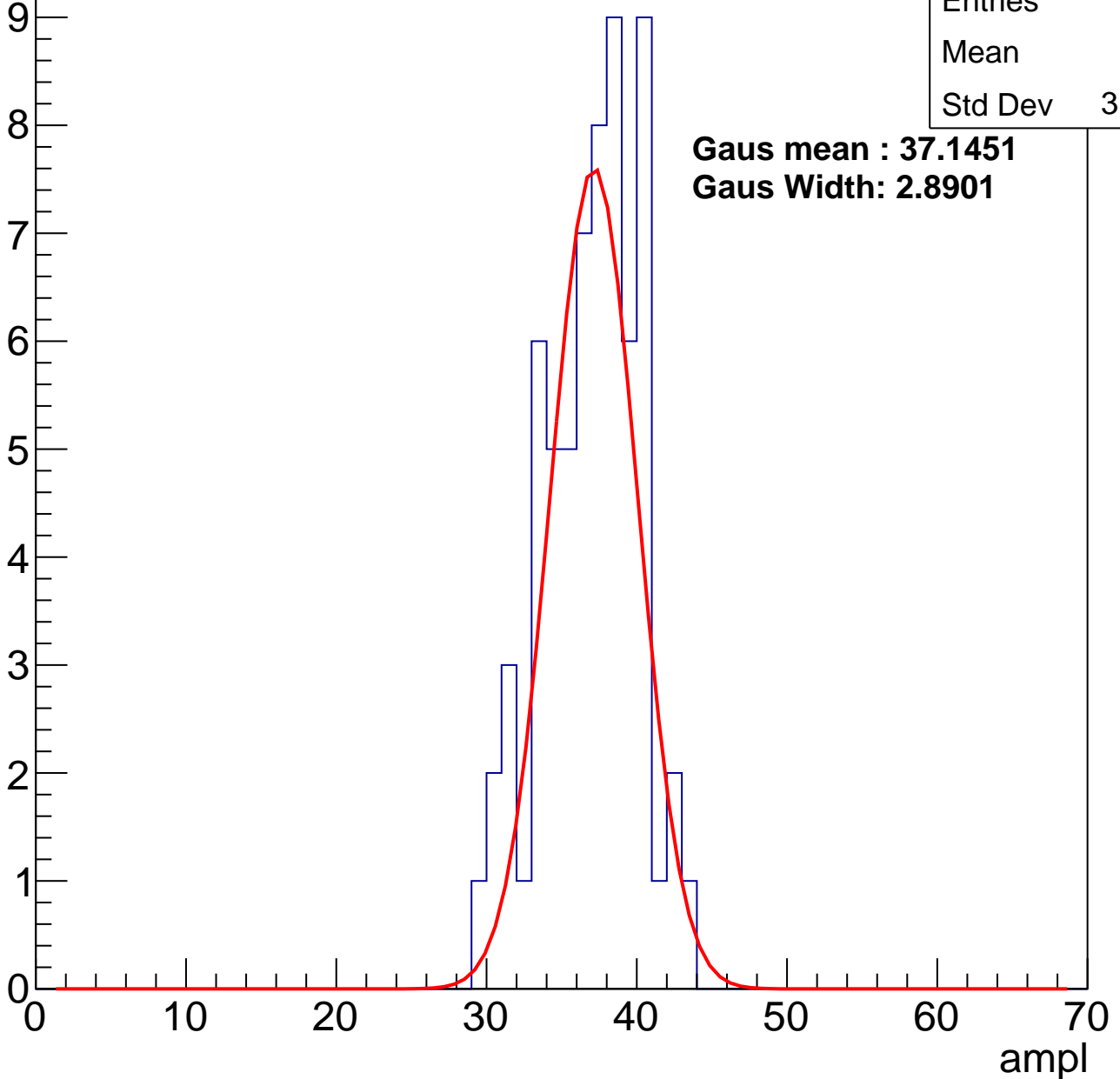
# B1L101S, U11-ch53, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	36.5
Std Dev	3.168

**Gaus mean : 37.1451**  
**Gaus Width: 2.8901**



# B1L101S, U11-ch53, adc2

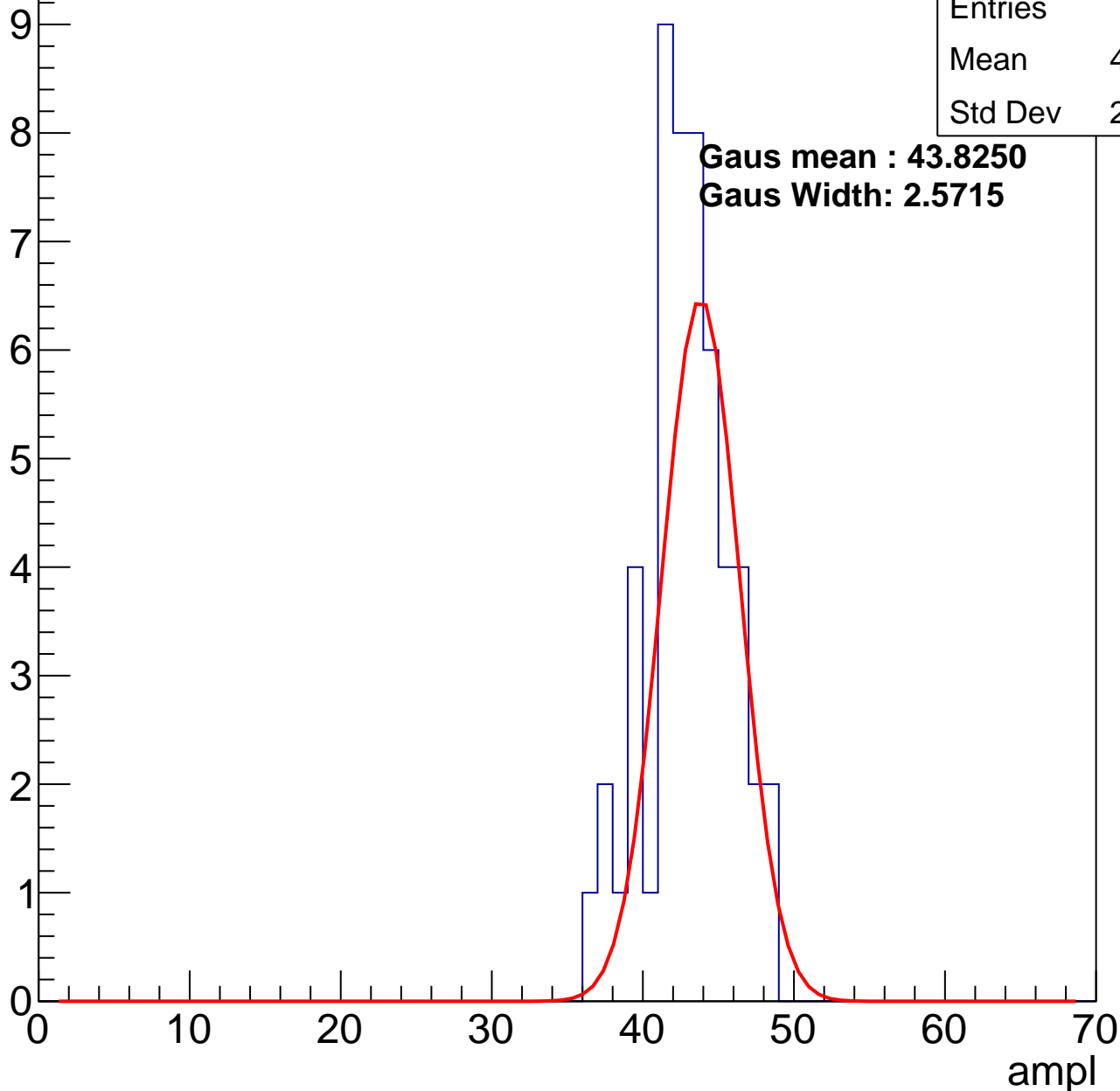
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	42.52
Std Dev	2.742

**Gaus mean : 43.8250**

**Gaus Width: 2.5715**



# B1L101S, U11-ch53, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	76
Mean	49.12
Std Dev	3.095

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

ampl

1

2

3

4

5

6

7

8

9

10

11

12

13

14

15

16

17

18

19

20

21

22

23

24

25

26

27

28

29

30

31

32

33

34

35

36

37

38

39

40

41

42

43

44

45

46

47

48

49

50

51

52

53

54

55

56

57

58

59

60

61

62

63

64

65

66

67

68

69

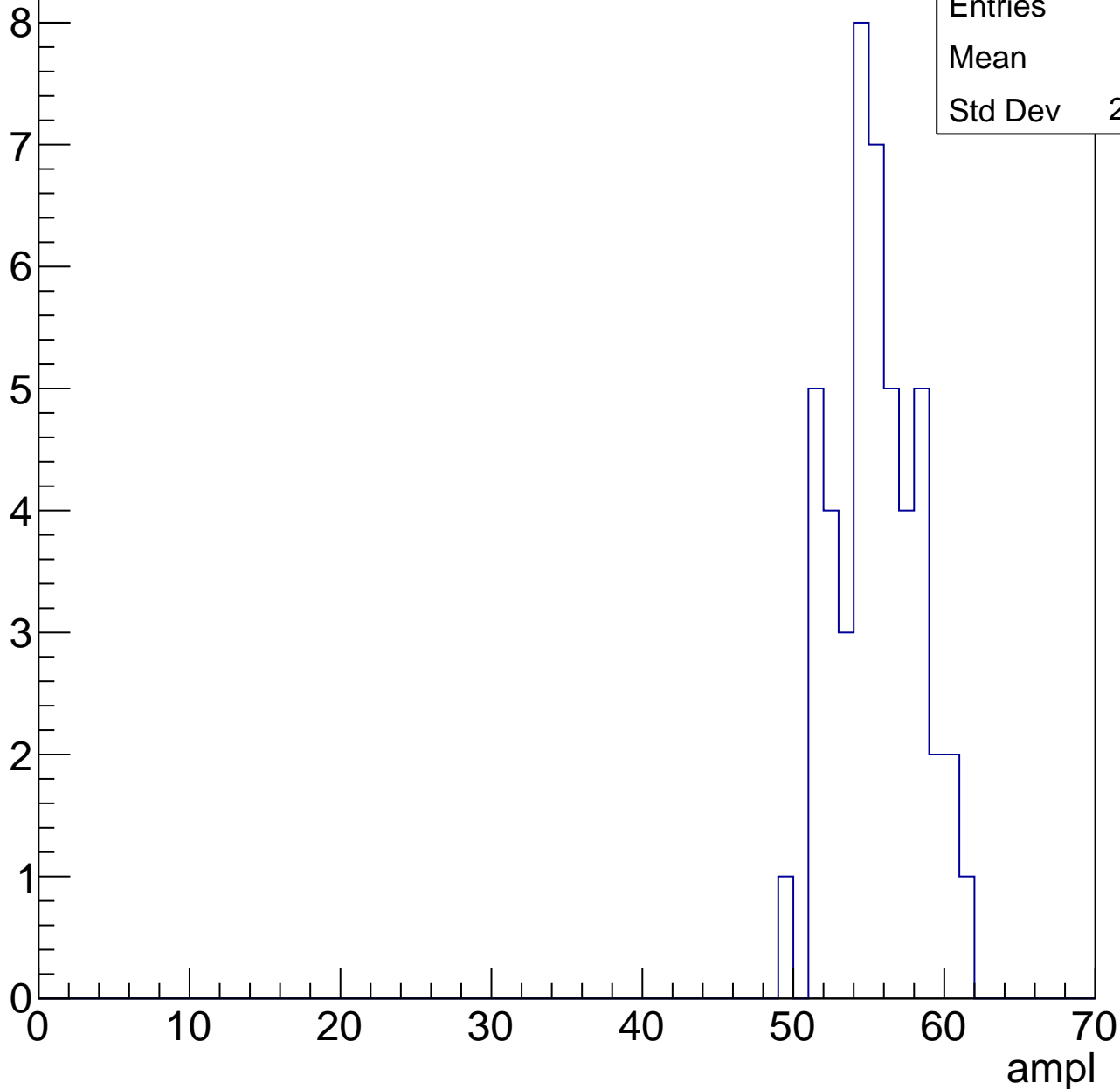
70

# B1L101S, U11-ch53, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

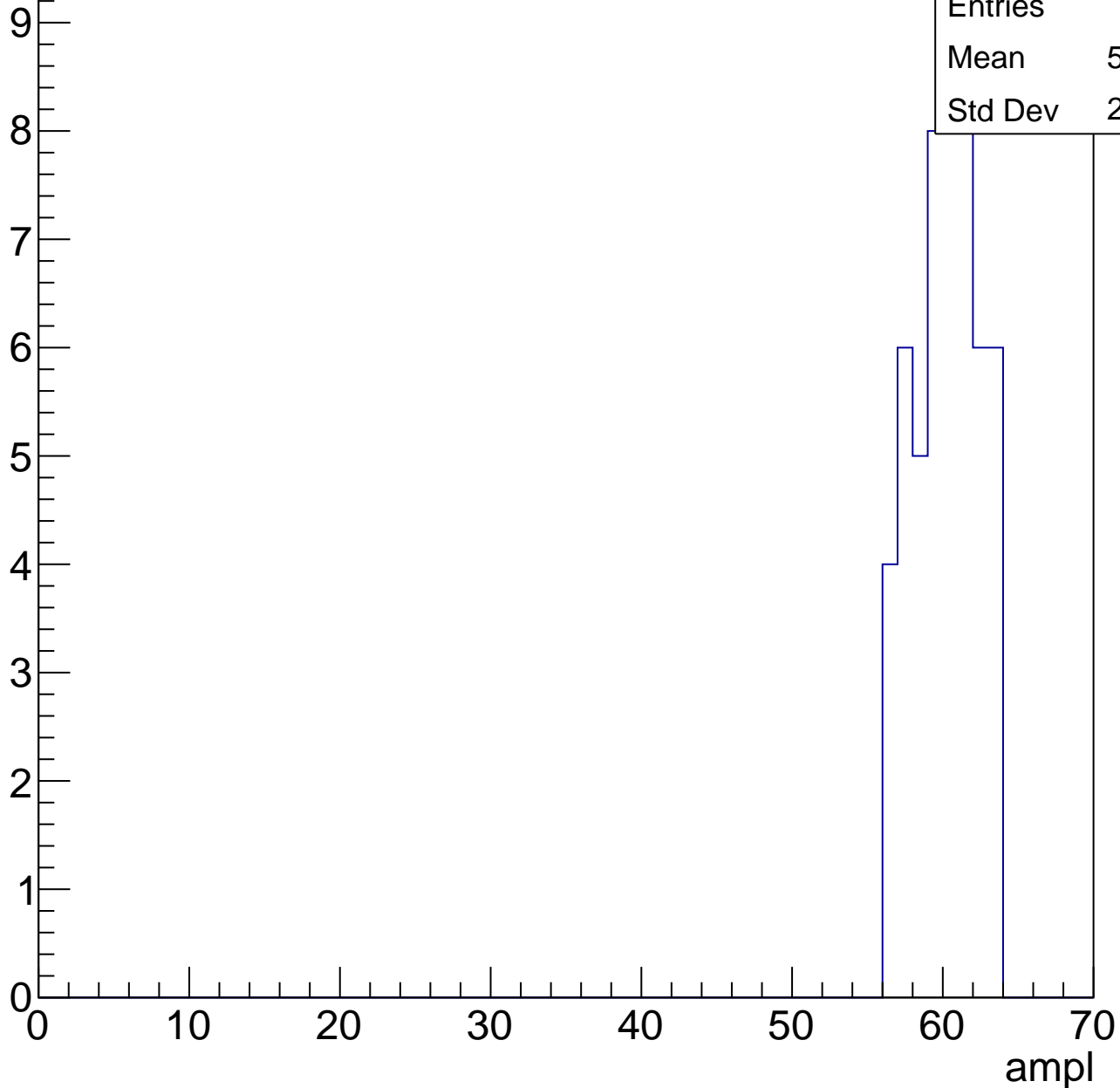
Entries	47
Mean	55
Std Dev	2.752



# B1L101S, U11-ch53, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

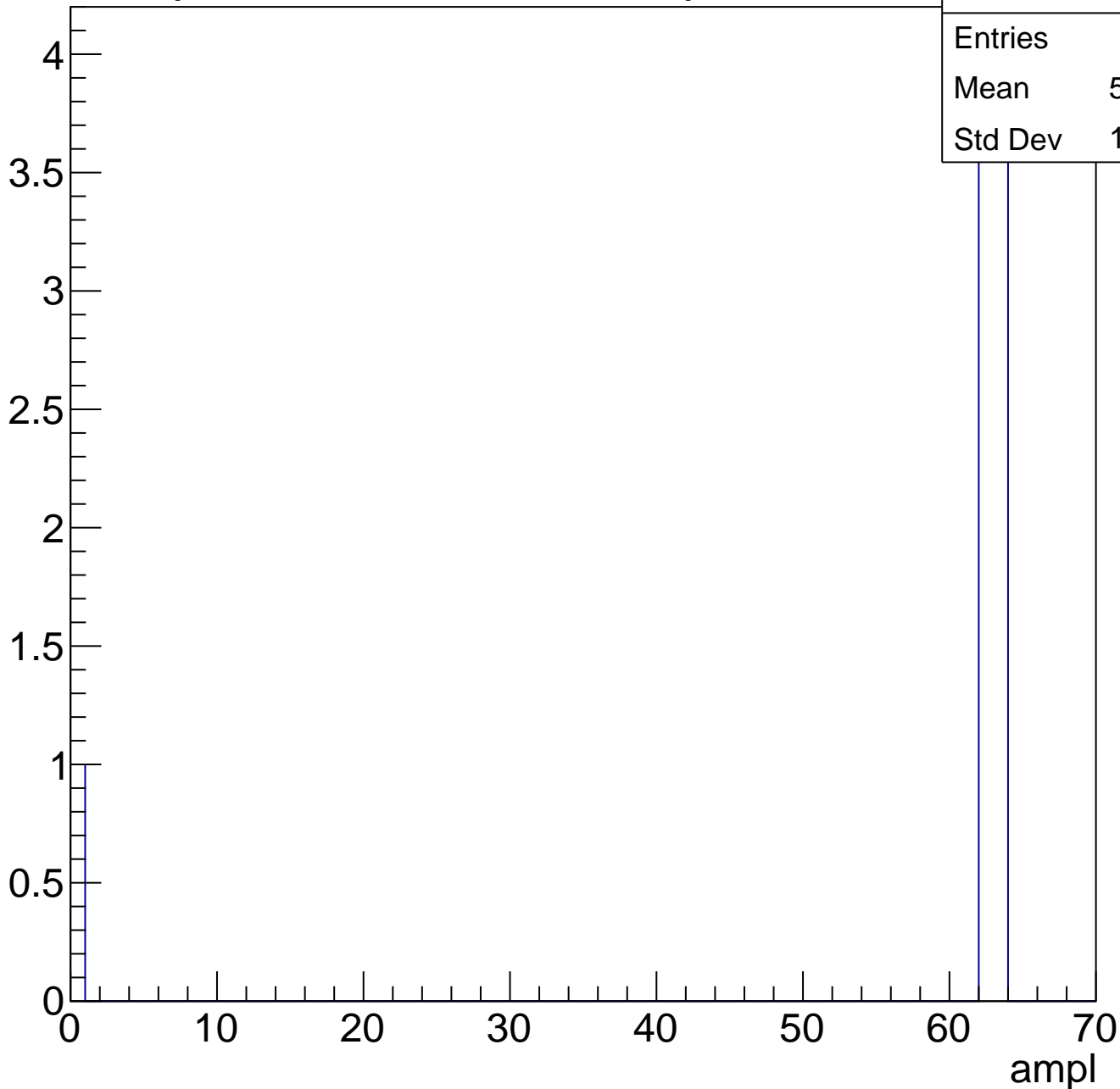


Entries	52
Mean	59.75
Std Dev	2.102

# B1L101S, U11-ch53, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch53, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U11-ch54, adc0

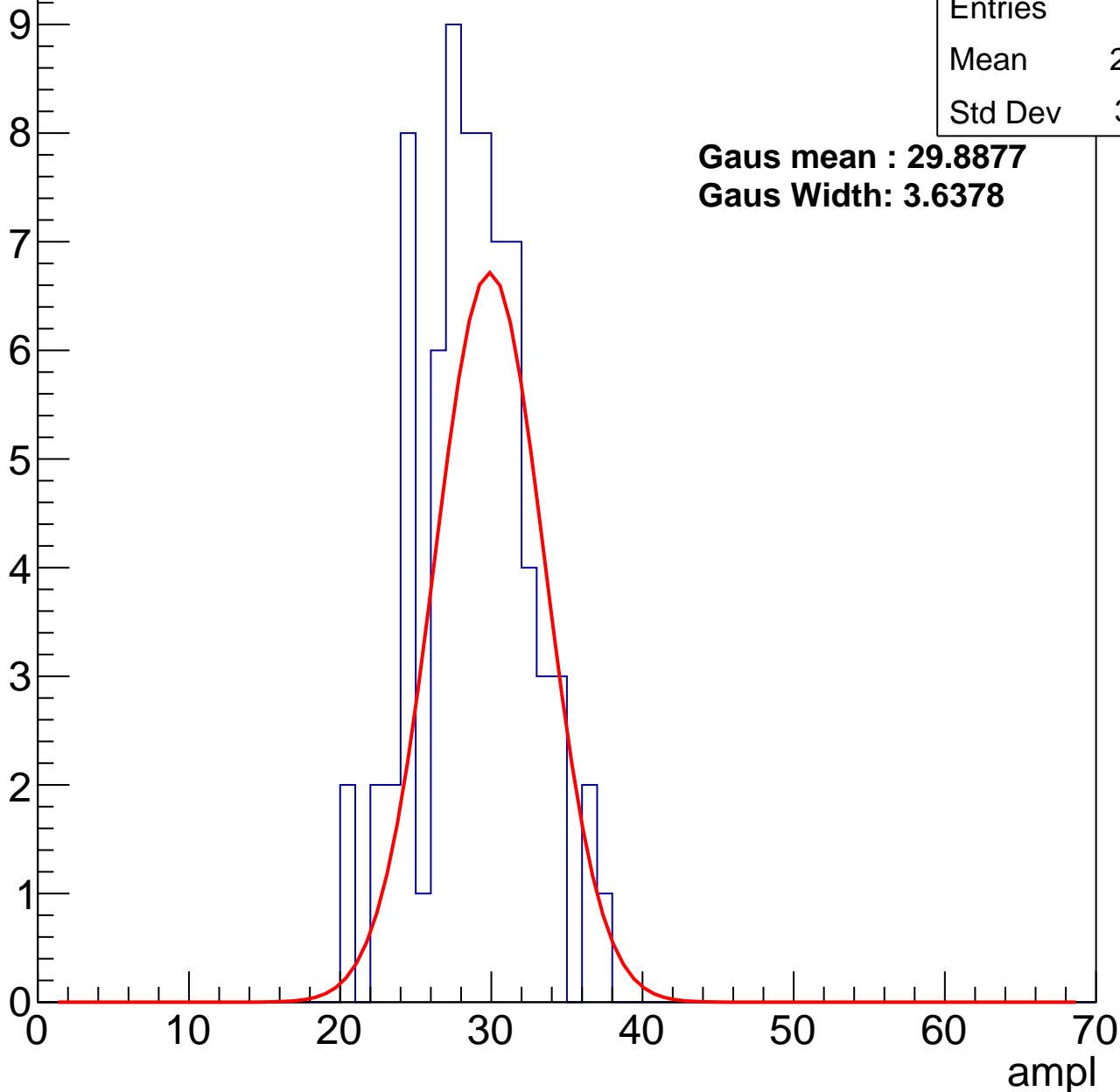
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	28.32
Std Dev	3.641

**Gaus mean : 29.8877**

**Gaus Width: 3.6378**



# B1L101S, U11-ch54, adc1

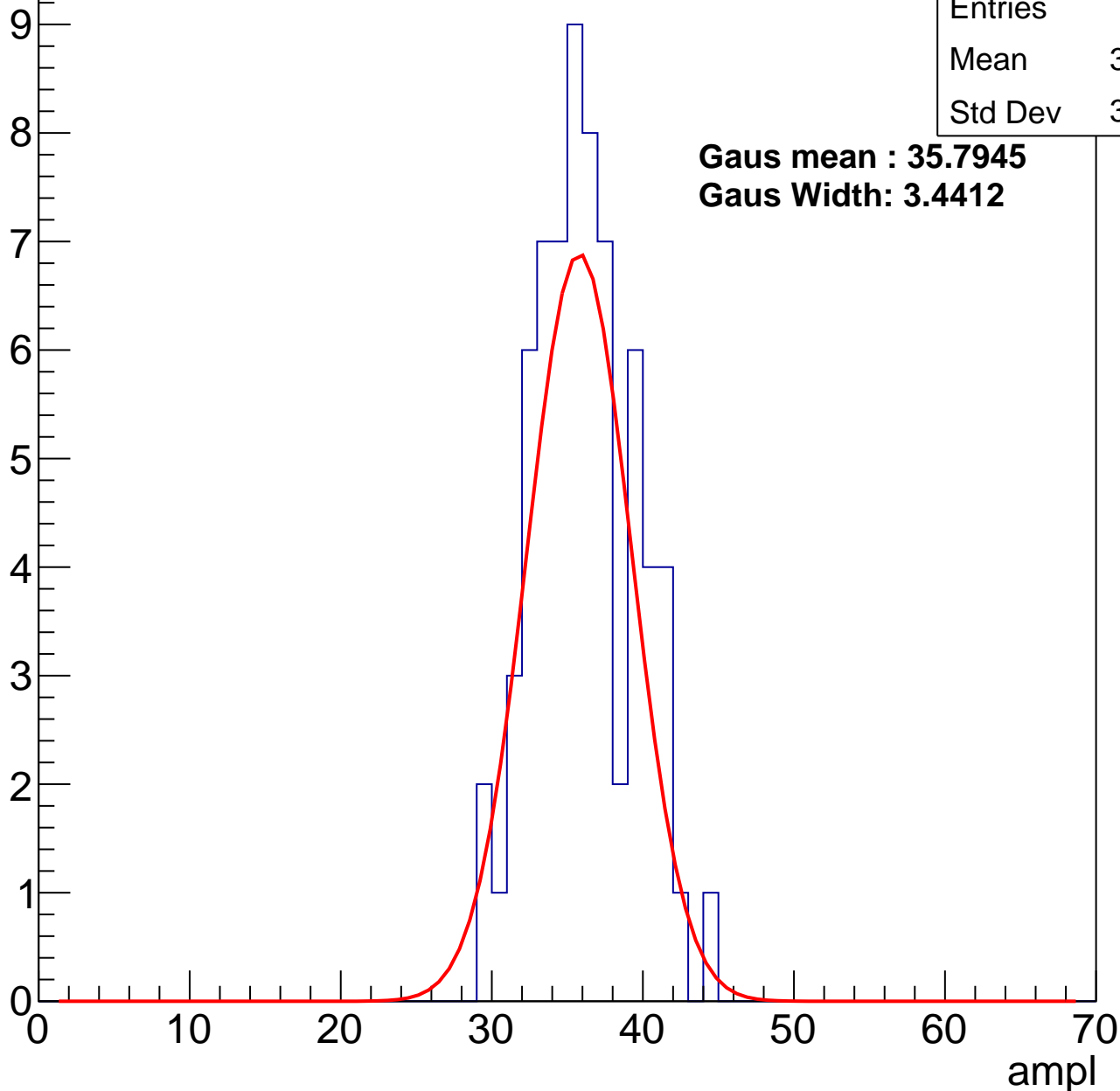
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	35.65
Std Dev	3.275

**Gaus mean : 35.7945**

**Gaus Width: 3.4412**



# B1L101S, U11-ch54, adc2

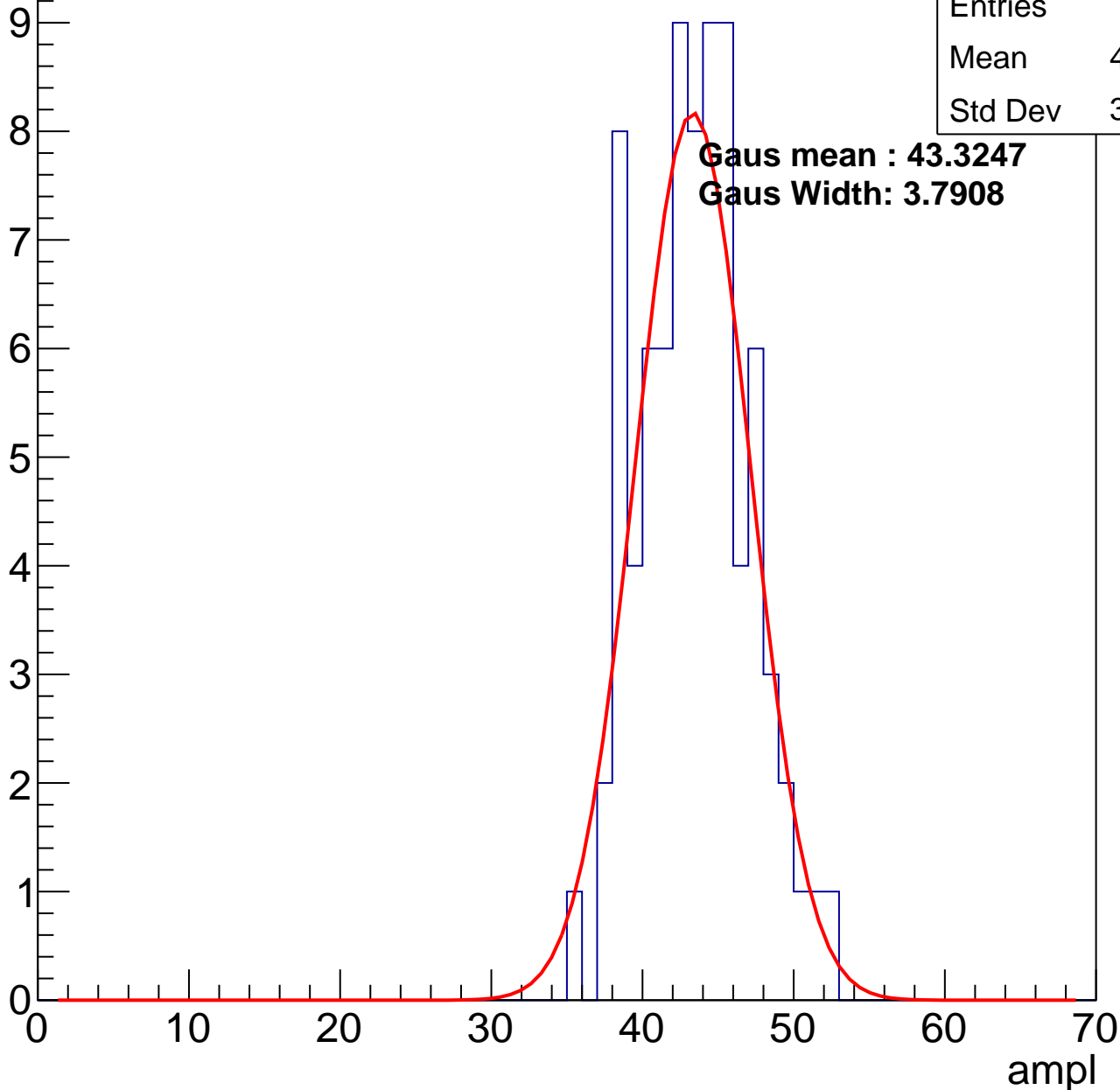
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	80
Mean	42.99
Std Dev	3.544

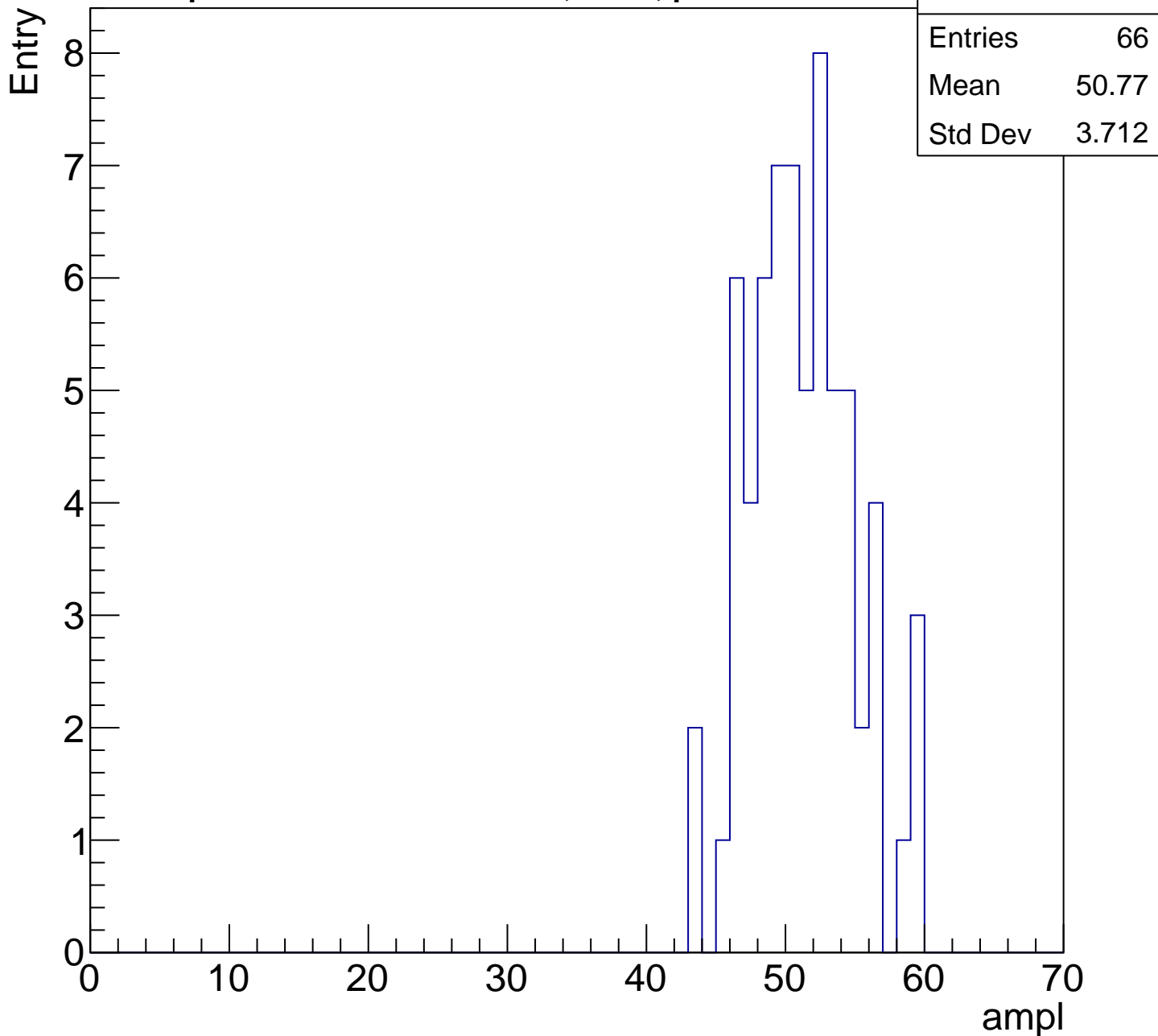
**Gaus mean : 43.3247**

**Gaus Width: 3.7908**



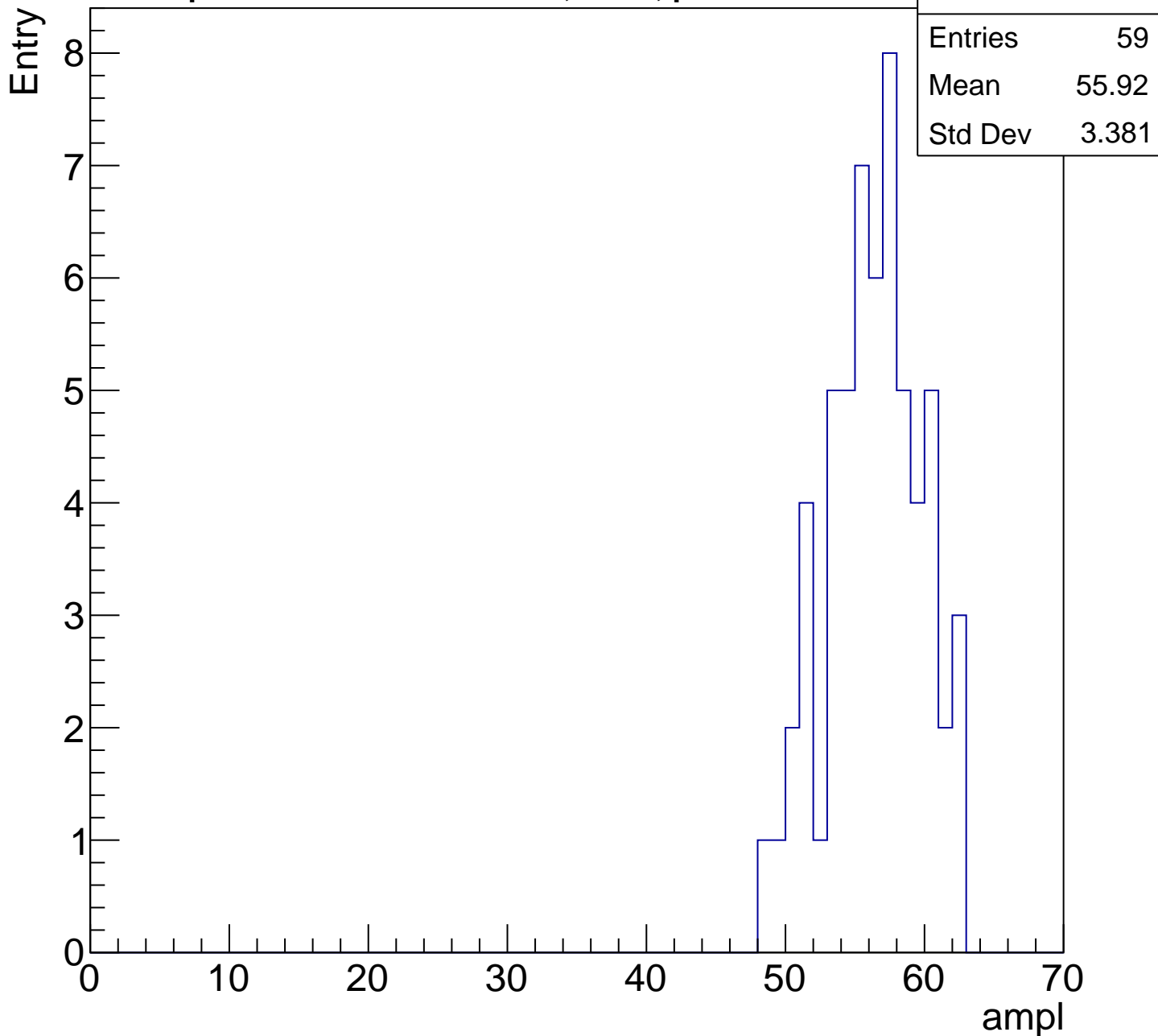
# B1L101S, U11-ch54, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U11-ch54, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

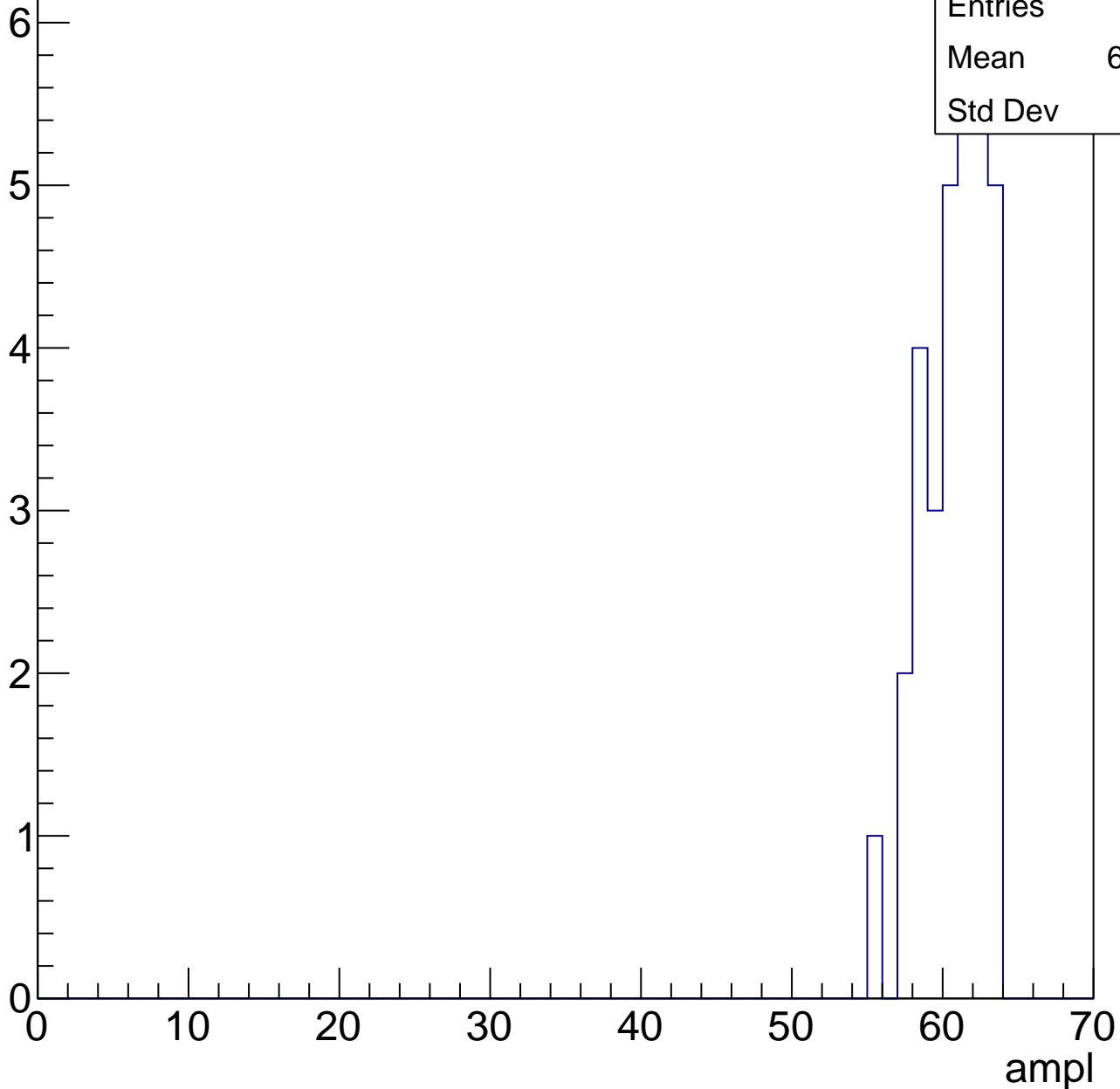


# B1L101S, U11-ch54, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	32
Mean	60.34
Std Dev	2.04

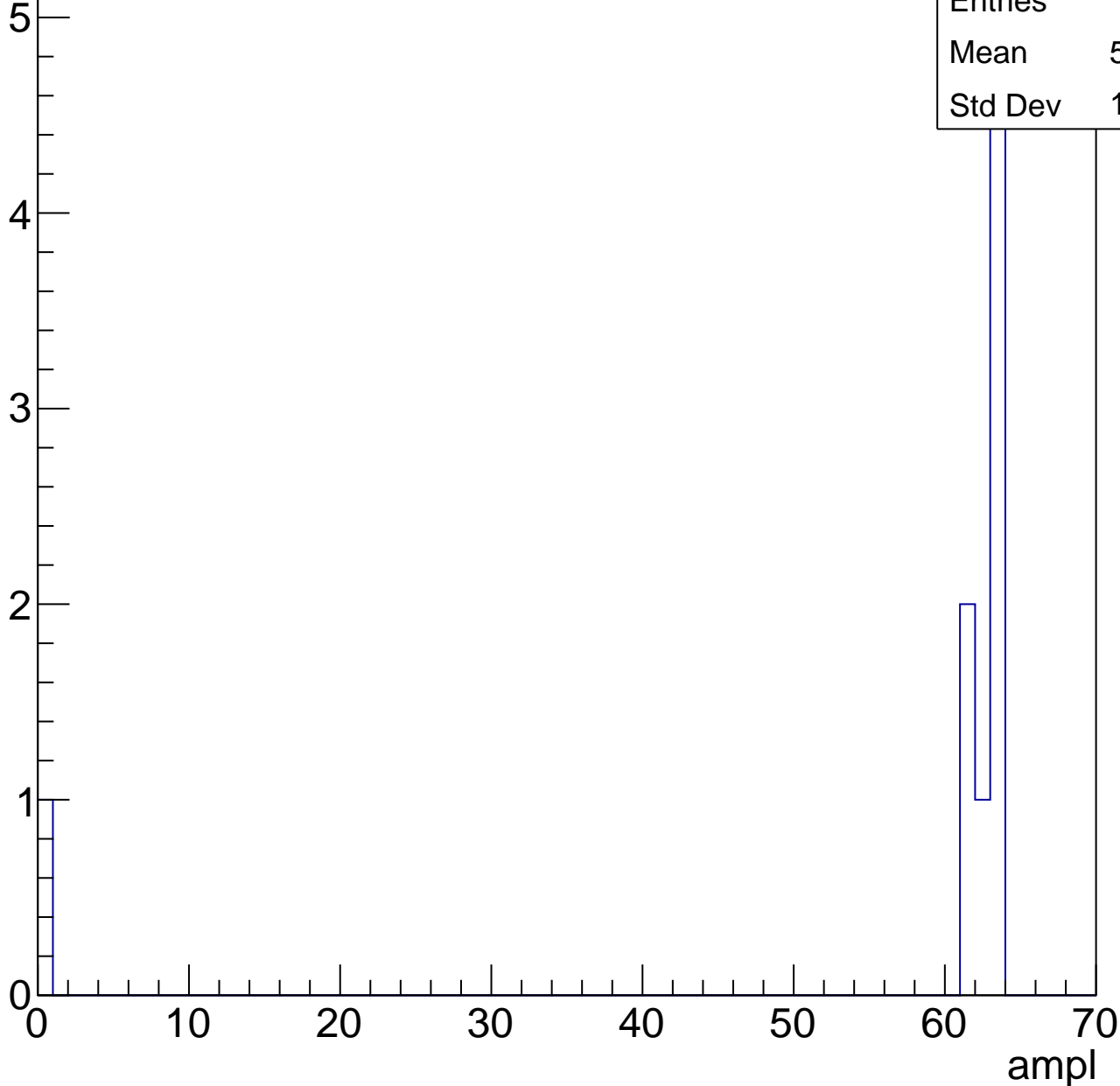


# B1L101S, U11-ch54, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	9
Mean	55.44
Std Dev	19.62





# B1L101S, U11-ch54, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U11-ch55, adc0

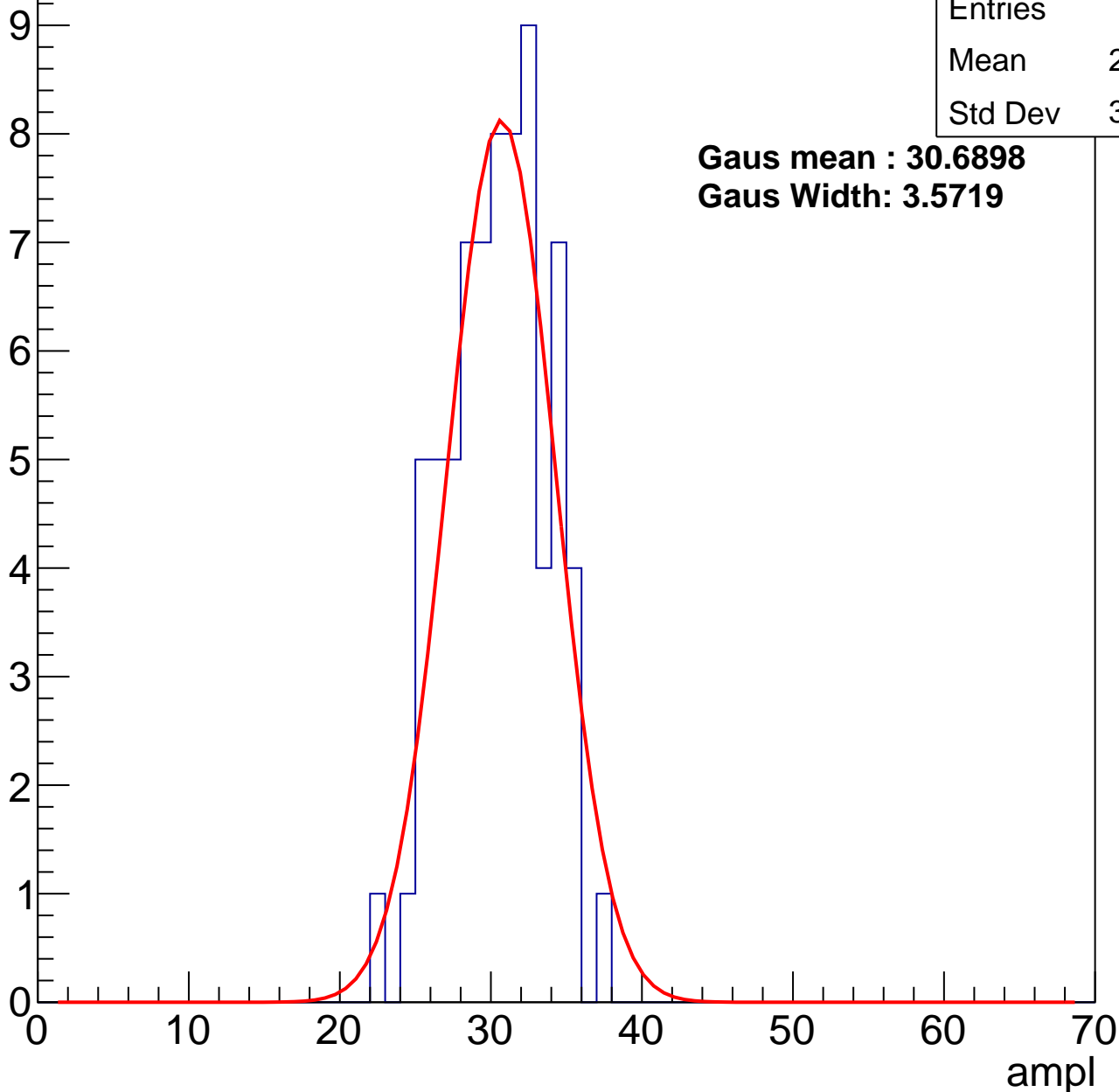
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	29.97
Std Dev	3.175

**Gaus mean : 30.6898**

**Gaus Width: 3.5719**



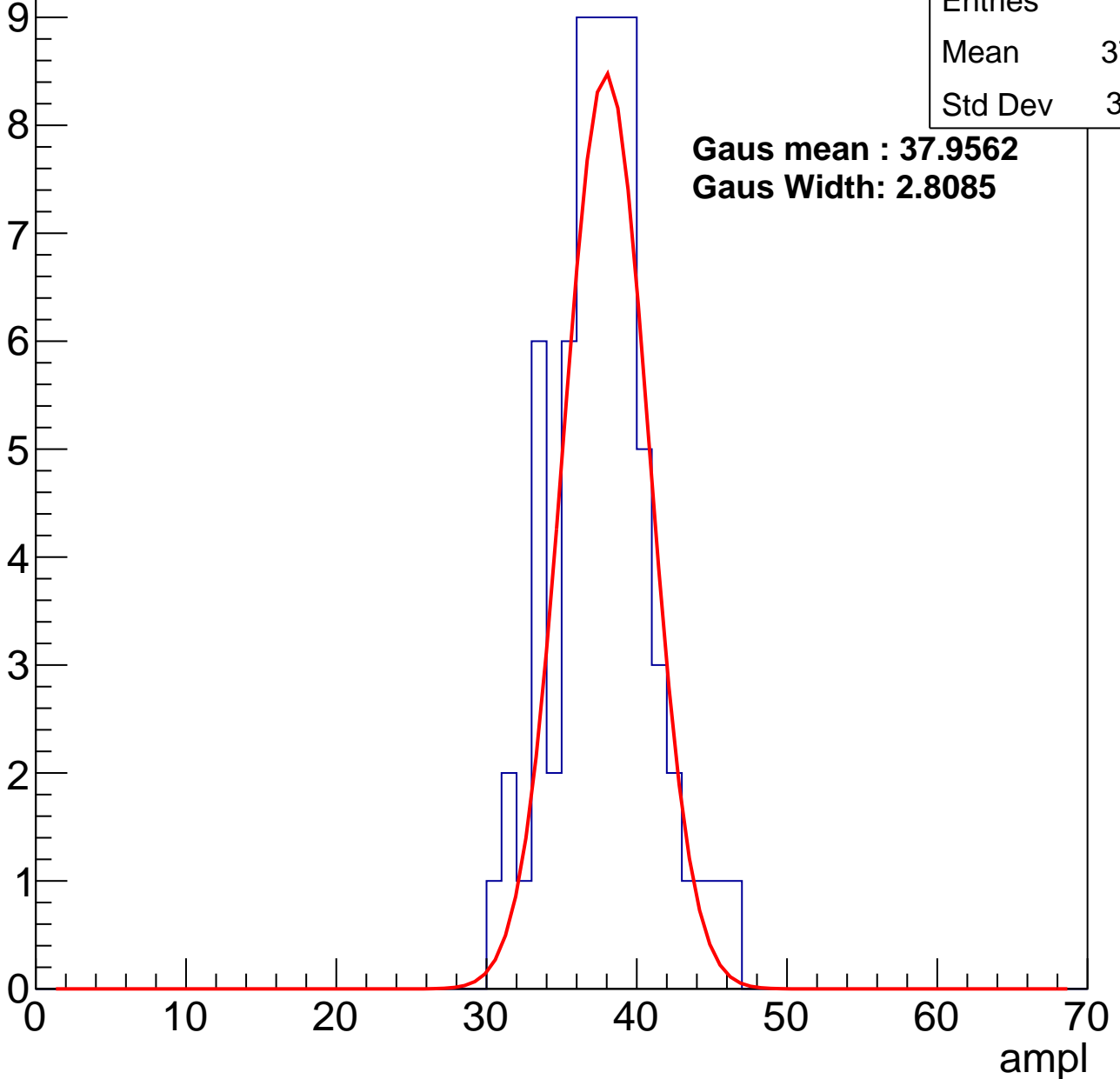
# B1L101S, U11-ch55, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	37.28
Std Dev	3.221

**Gaus mean : 37.9562**  
**Gaus Width: 2.8085**



# B1L101S, U11-ch55, adc2

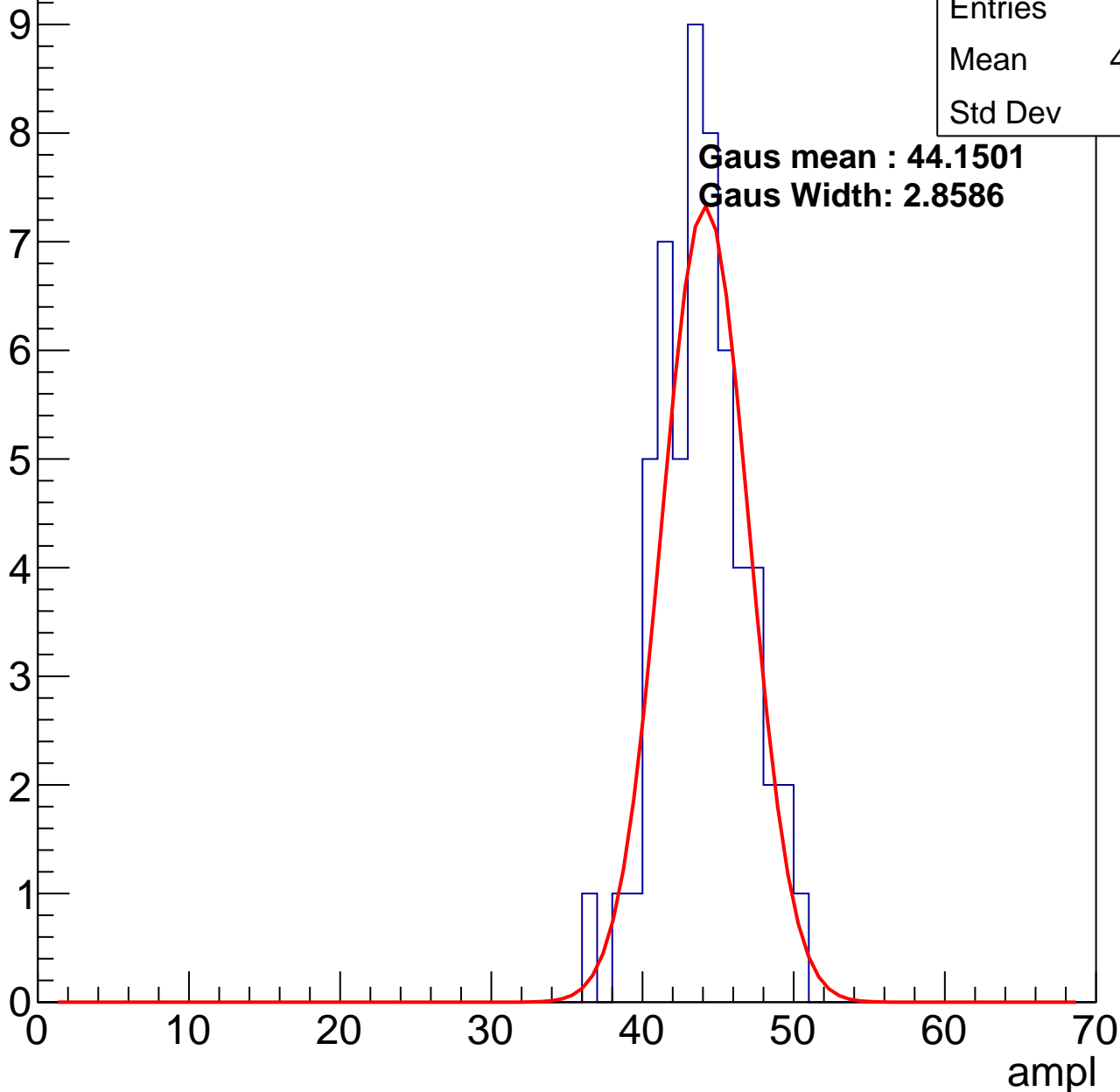
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	43.48
Std Dev	2.86

**Gaus mean : 44.1501**

**Gaus Width: 2.8586**

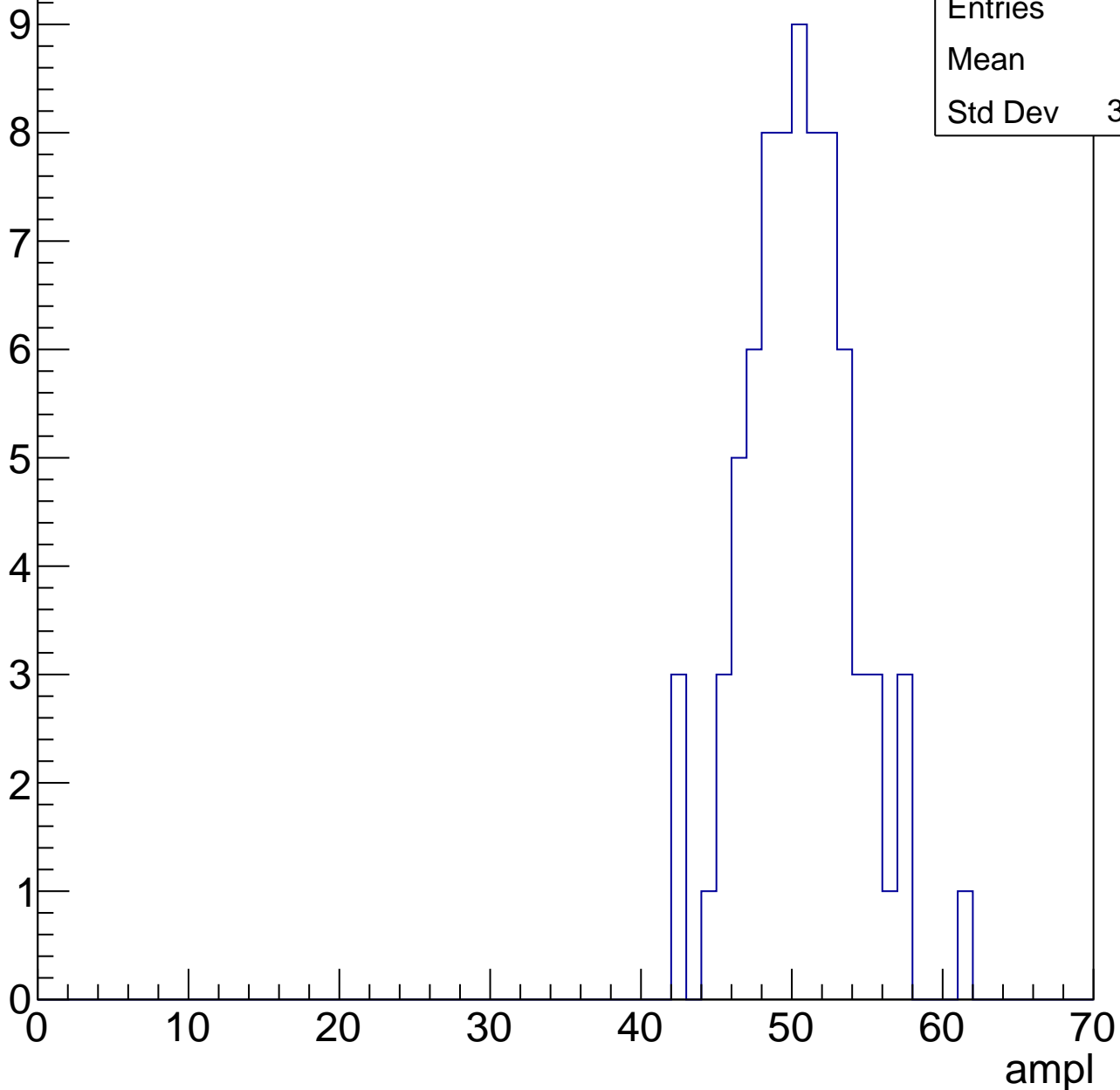


# B1L101S, U11-ch55, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

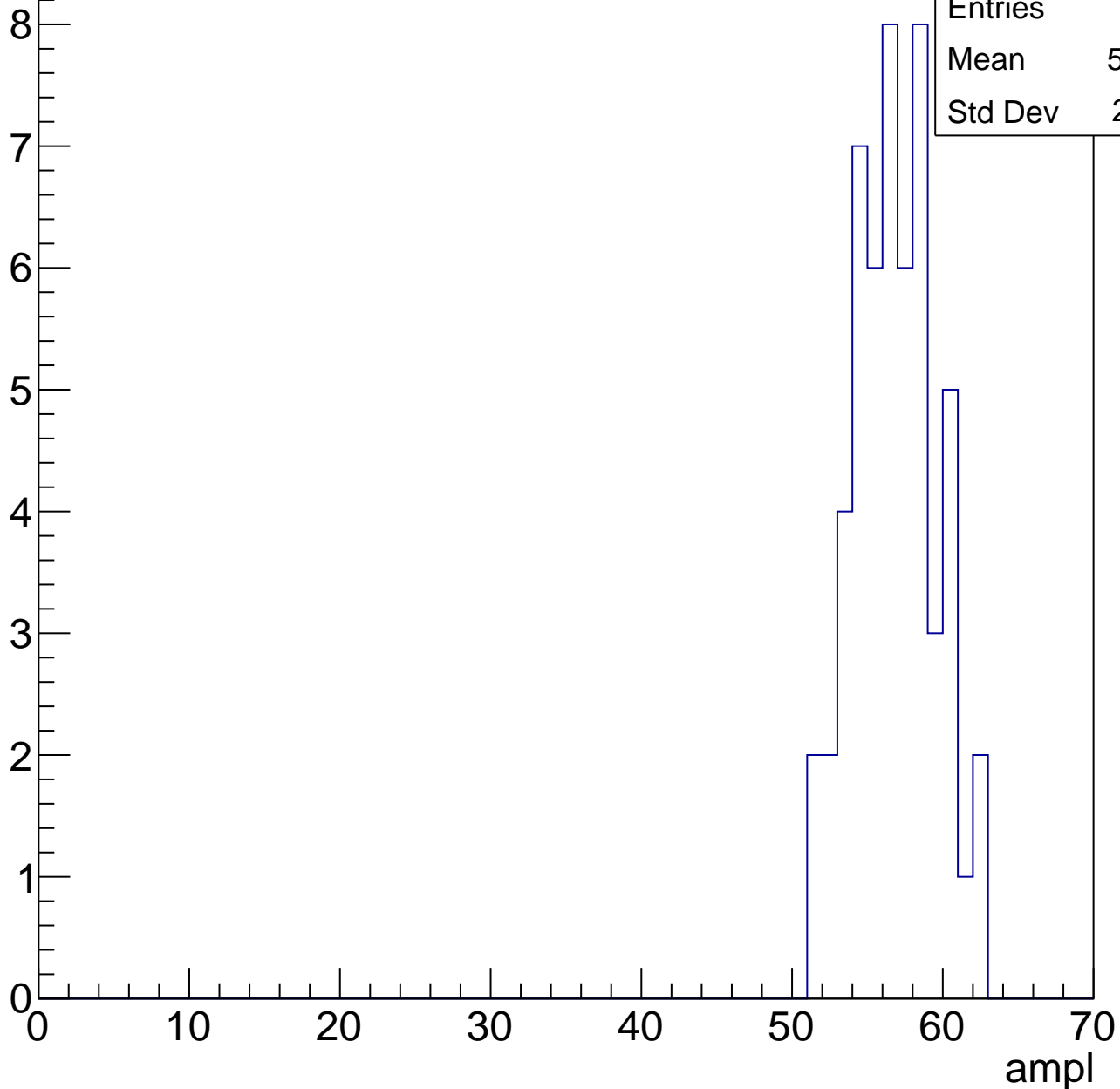
Entries	76
Mean	50
Std Dev	3.624



# B1L101S, U11-ch55, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



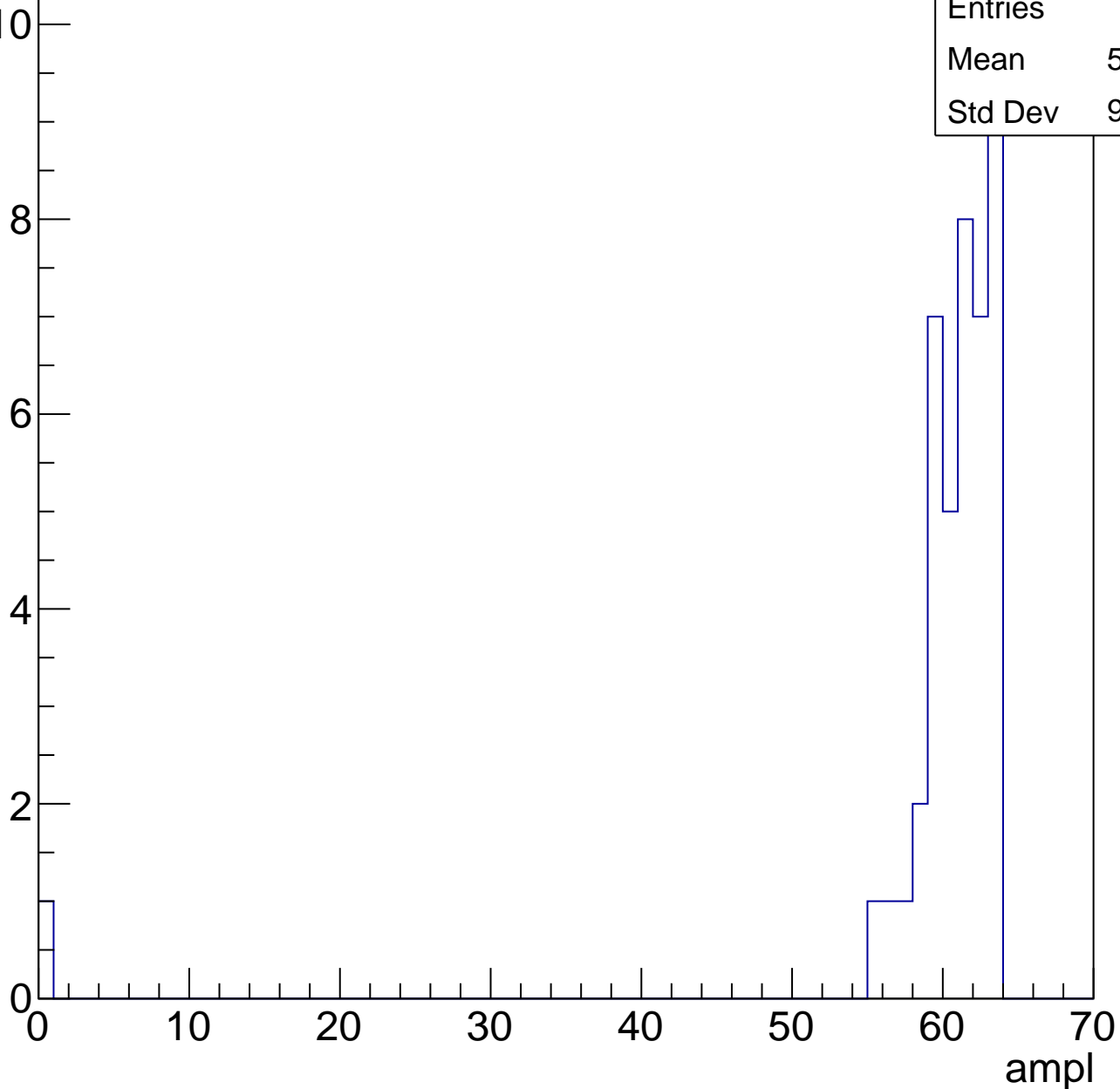
Entries	54
Mean	56.33
Std Dev	2.681

# B1L101S, U11-ch55, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	43
Mean	59.28
Std Dev	9.362



# B1L101S, U11-ch55, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch55, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U11-ch56, adc0

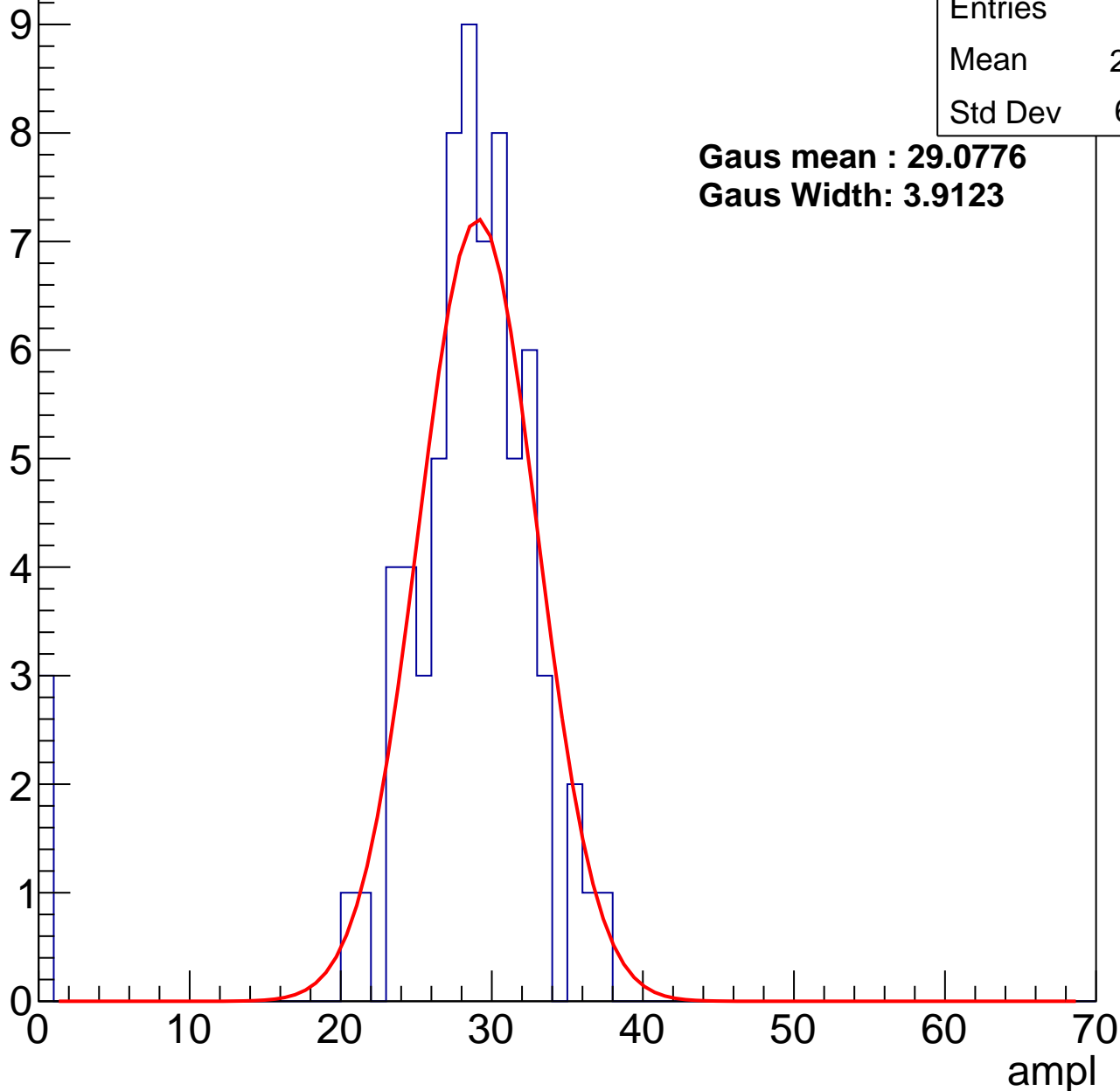
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	27.24
Std Dev	6.651

**Gaus mean : 29.0776**

**Gaus Width: 3.9123**



# B1L101S, U11-ch56, adc1

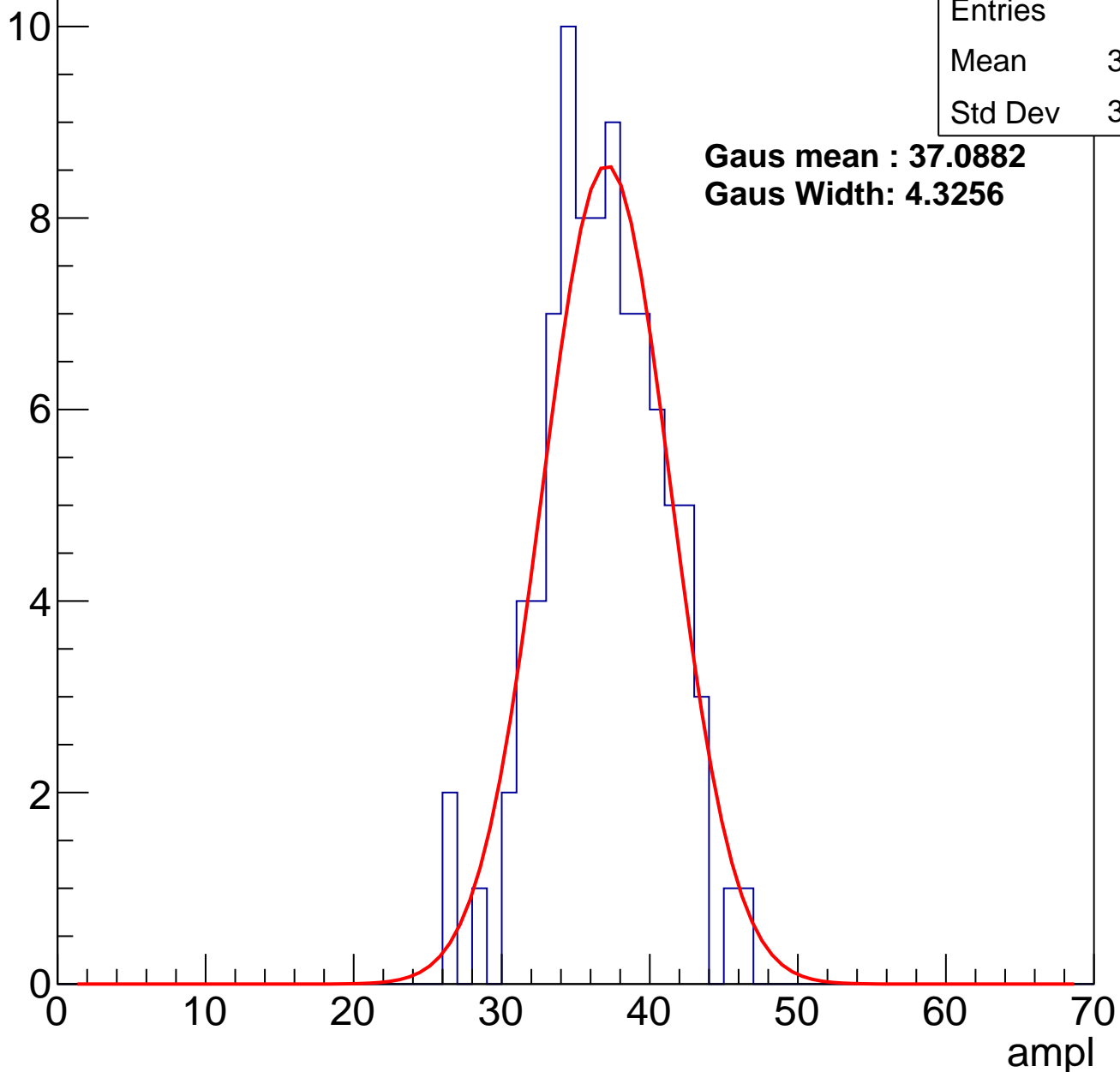
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	90
Mean	36.42
Std Dev	3.978

**Gaus mean : 37.0882**

**Gaus Width: 4.3256**

Entry



# B1L101S, U11-ch56, adc2

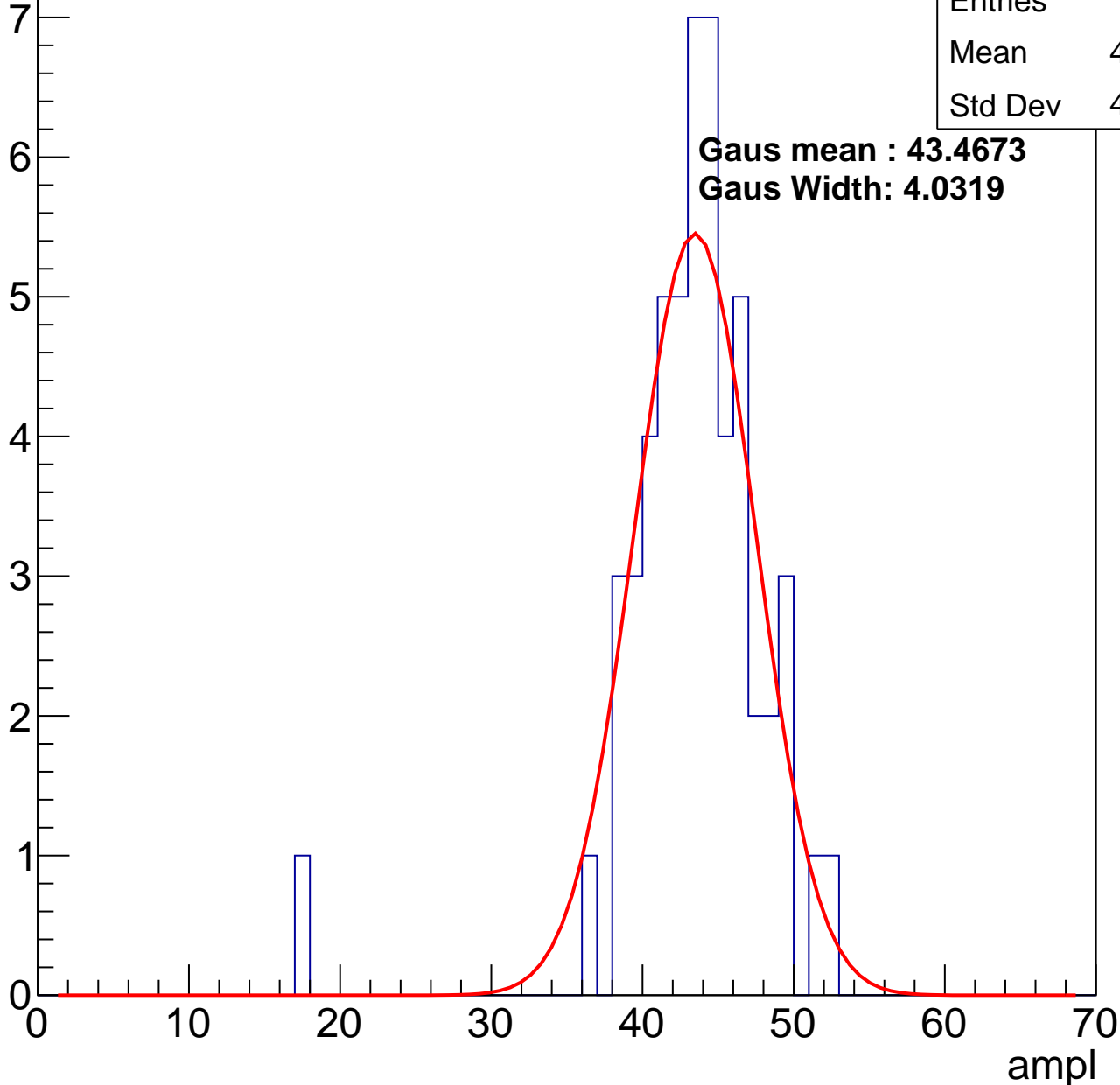
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	42.93
Std Dev	4.929

**Gaus mean : 43.4673**

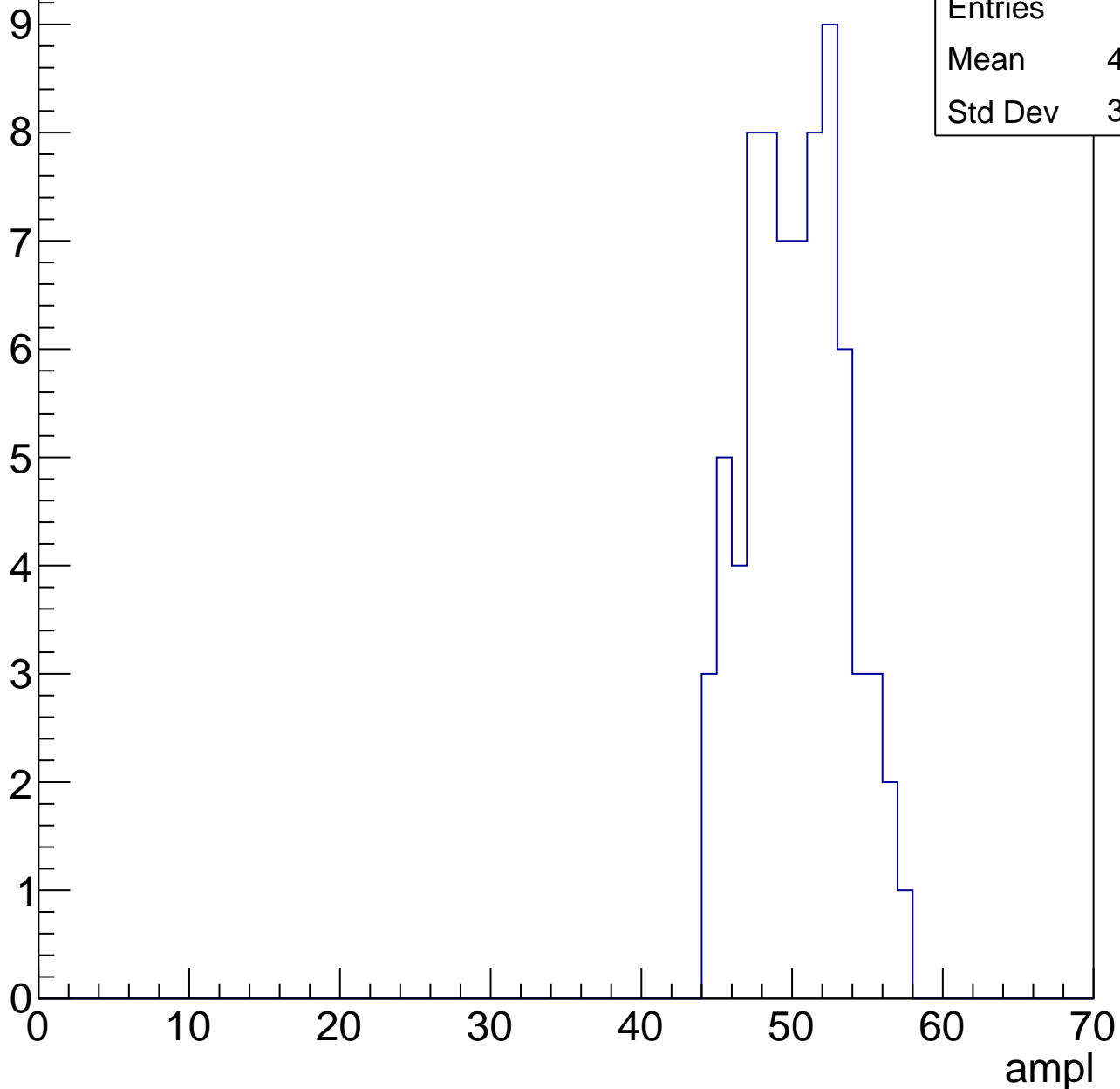
**Gaus Width: 4.0319**



# B1L101S, U11-ch56, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

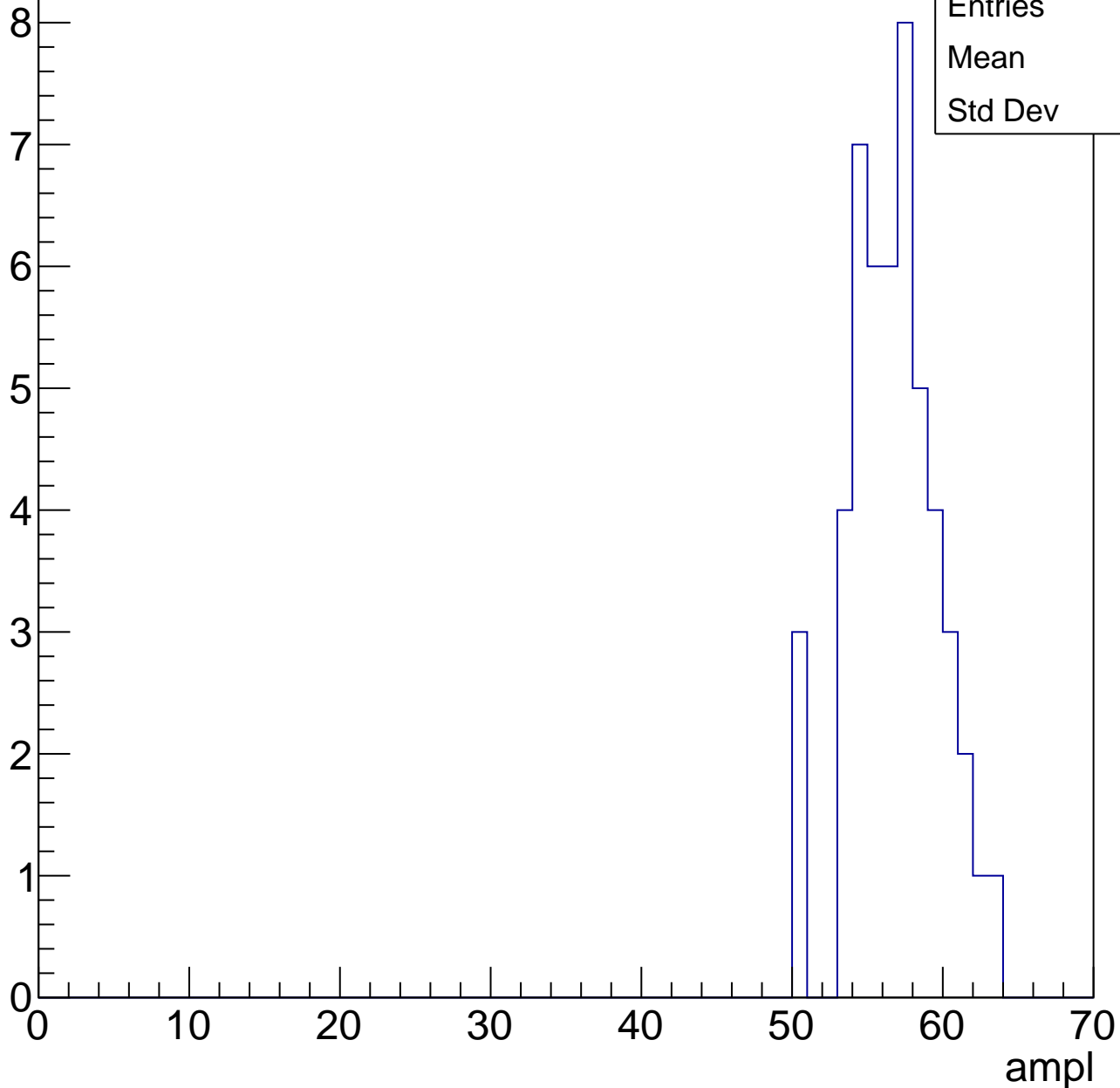


Entries	74
Mean	49.78
Std Dev	3.176

# B1L101S, U11-ch56, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

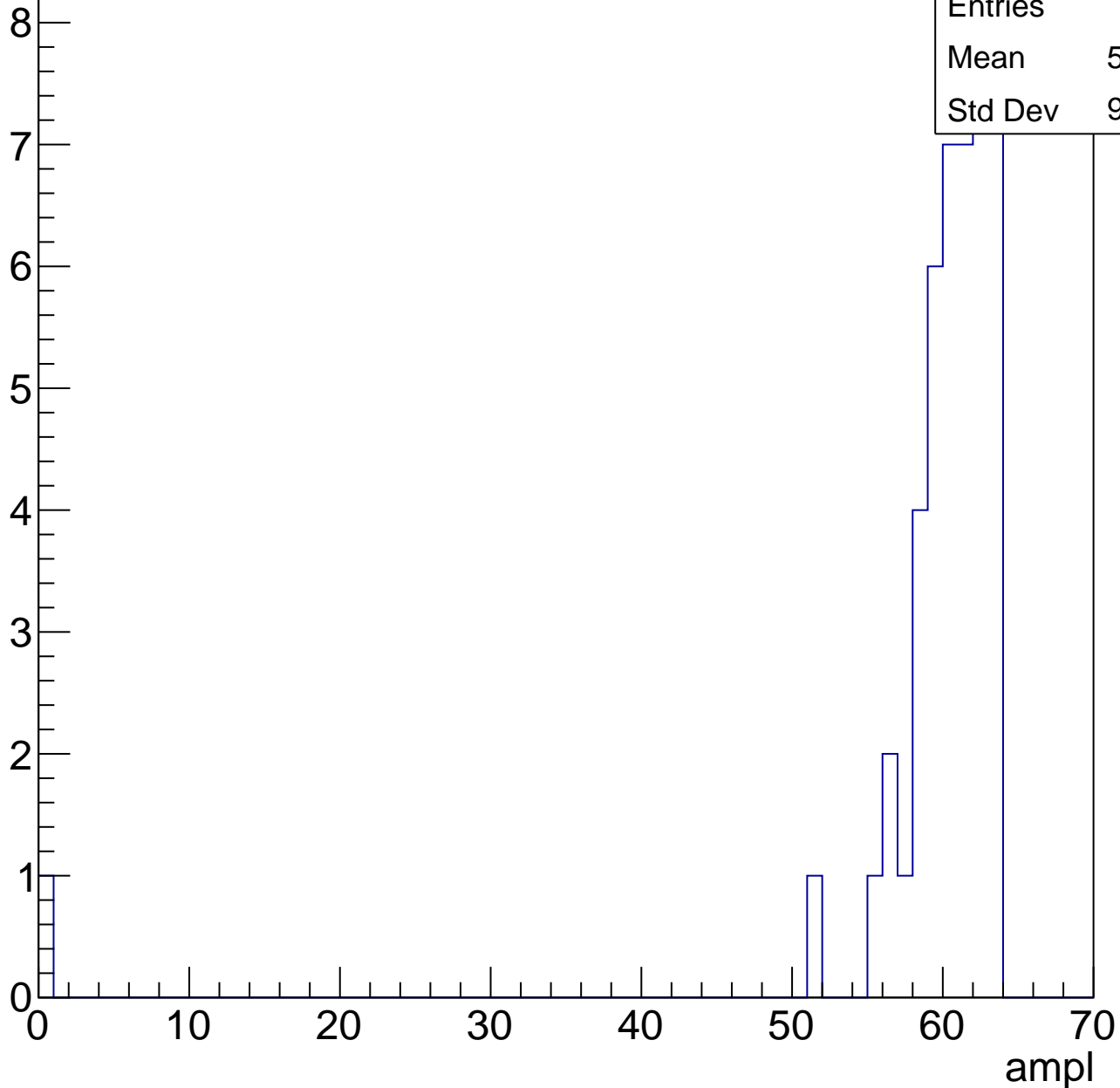


Entries	50
Mean	56.3
Std Dev	2.9

# B1L101S, U11-ch56, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

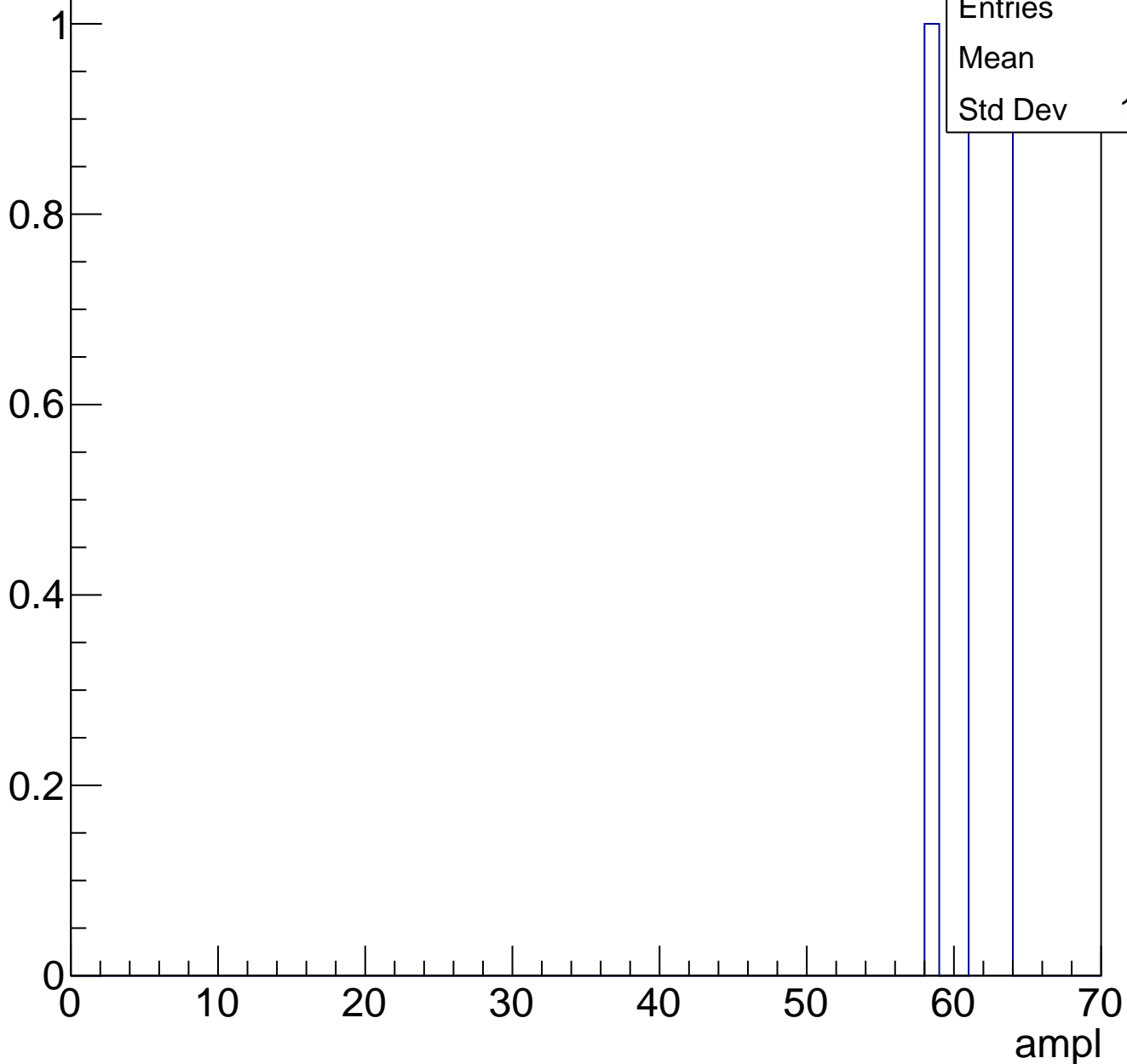
Entry



# B1L101S, U11-ch56, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch56, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U11-ch57, adc0

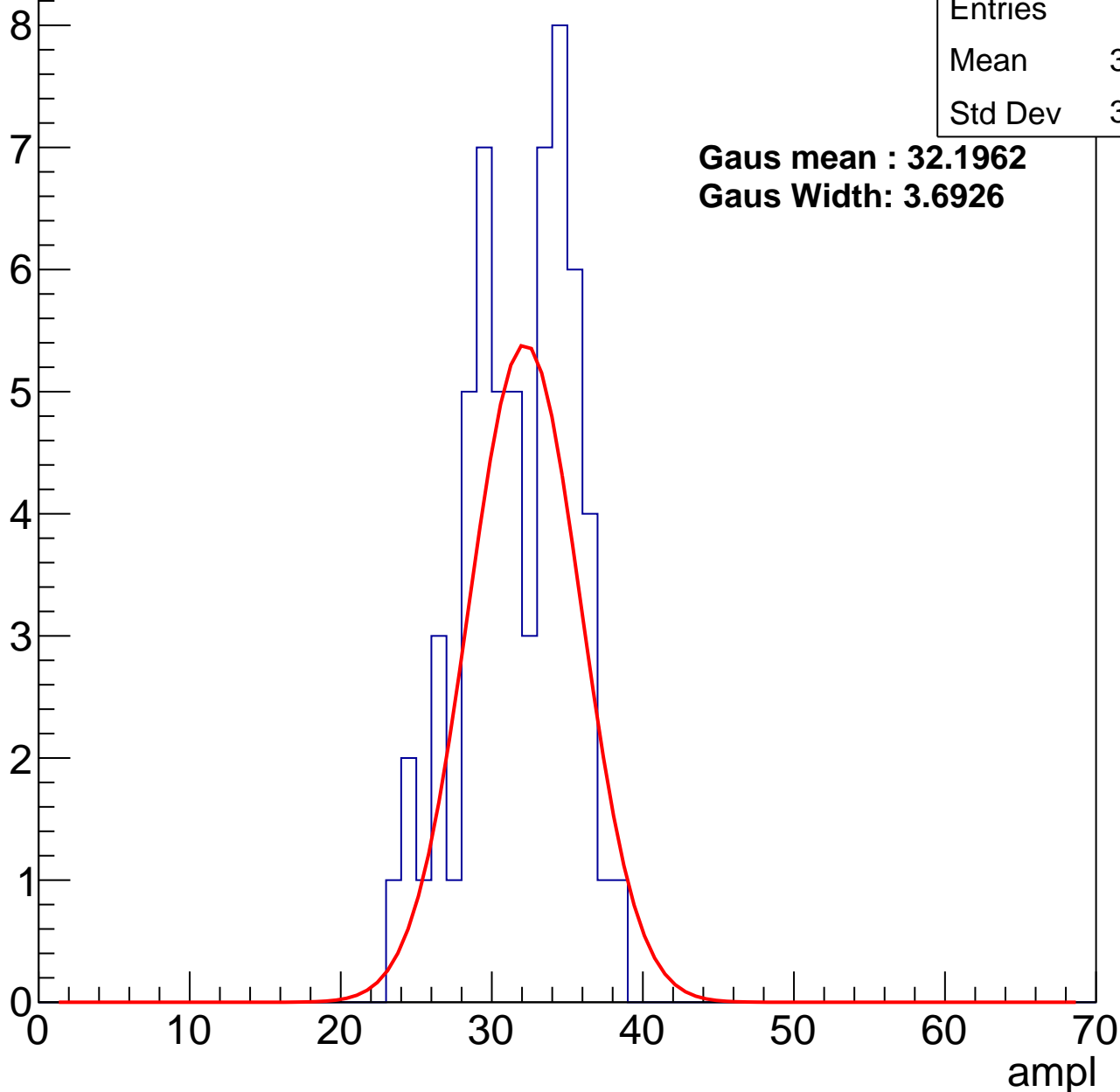
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	31.28
Std Dev	3.527

**Gaus mean : 32.1962**

**Gaus Width: 3.6926**



# B1L101S, U11-ch57, adc1

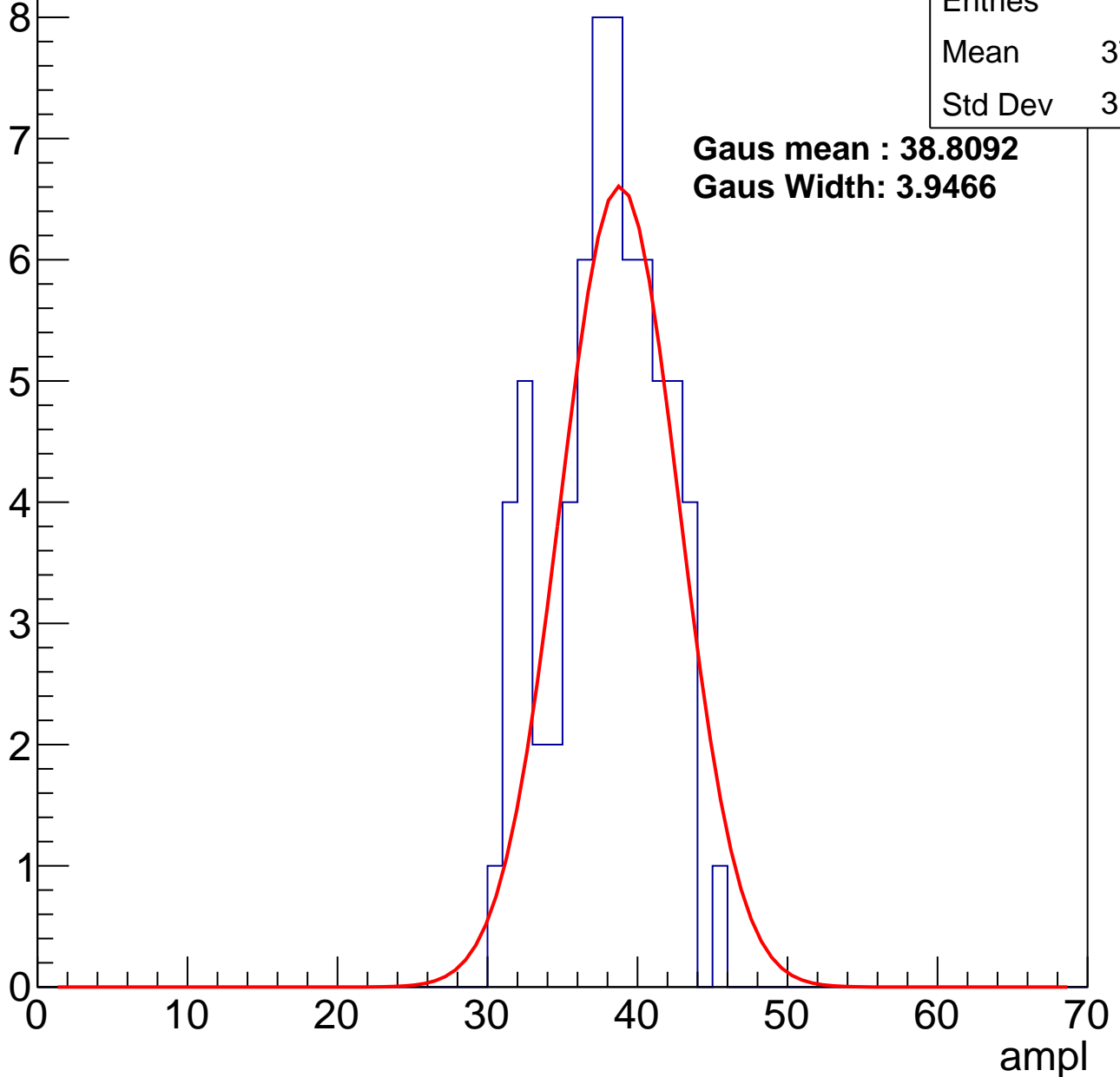
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	37.46
Std Dev	3.613

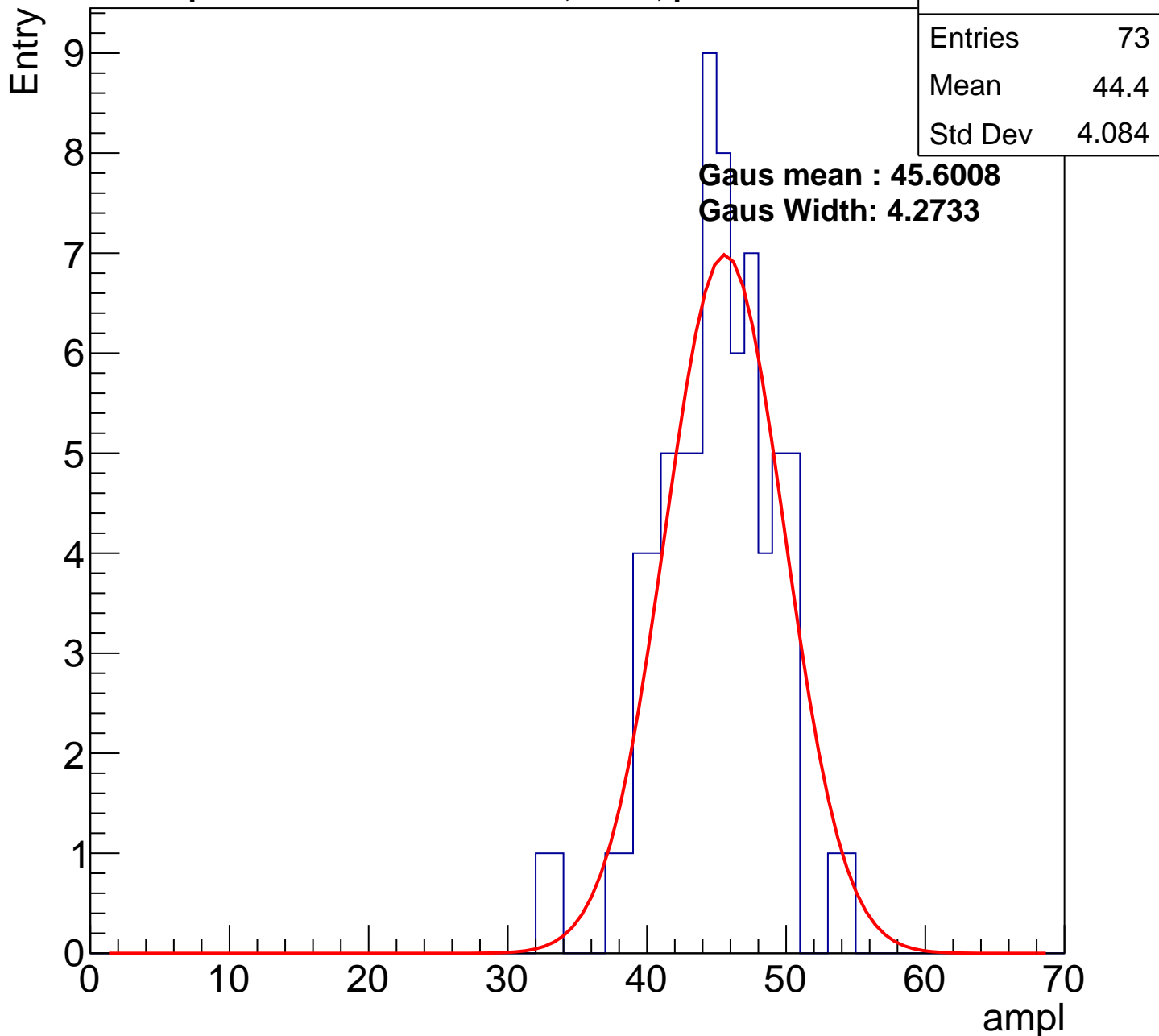
**Gaus mean : 38.8092**

**Gaus Width: 3.9466**



# B1L101S, U11-ch57, adc2

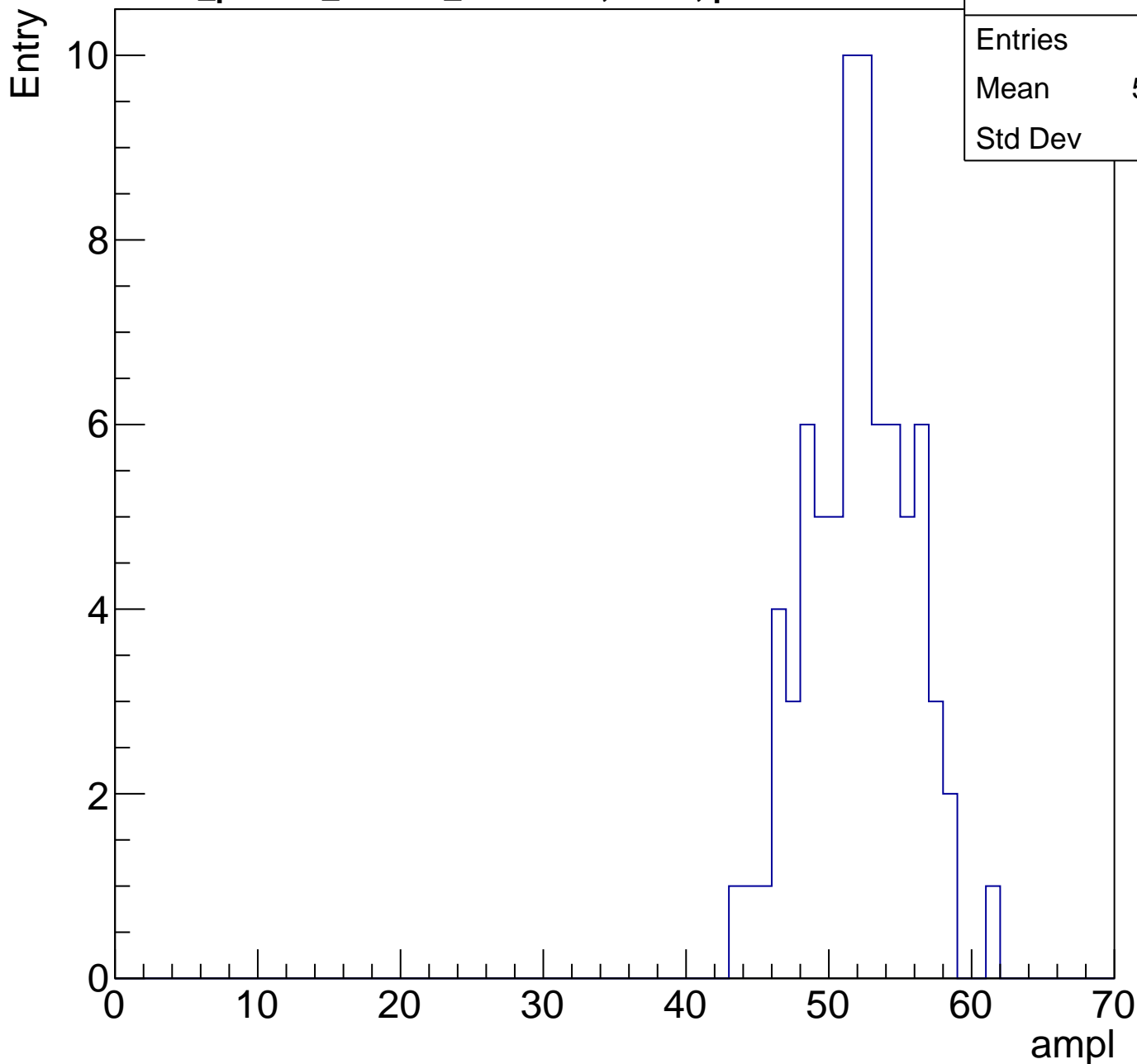
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U11-ch57, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

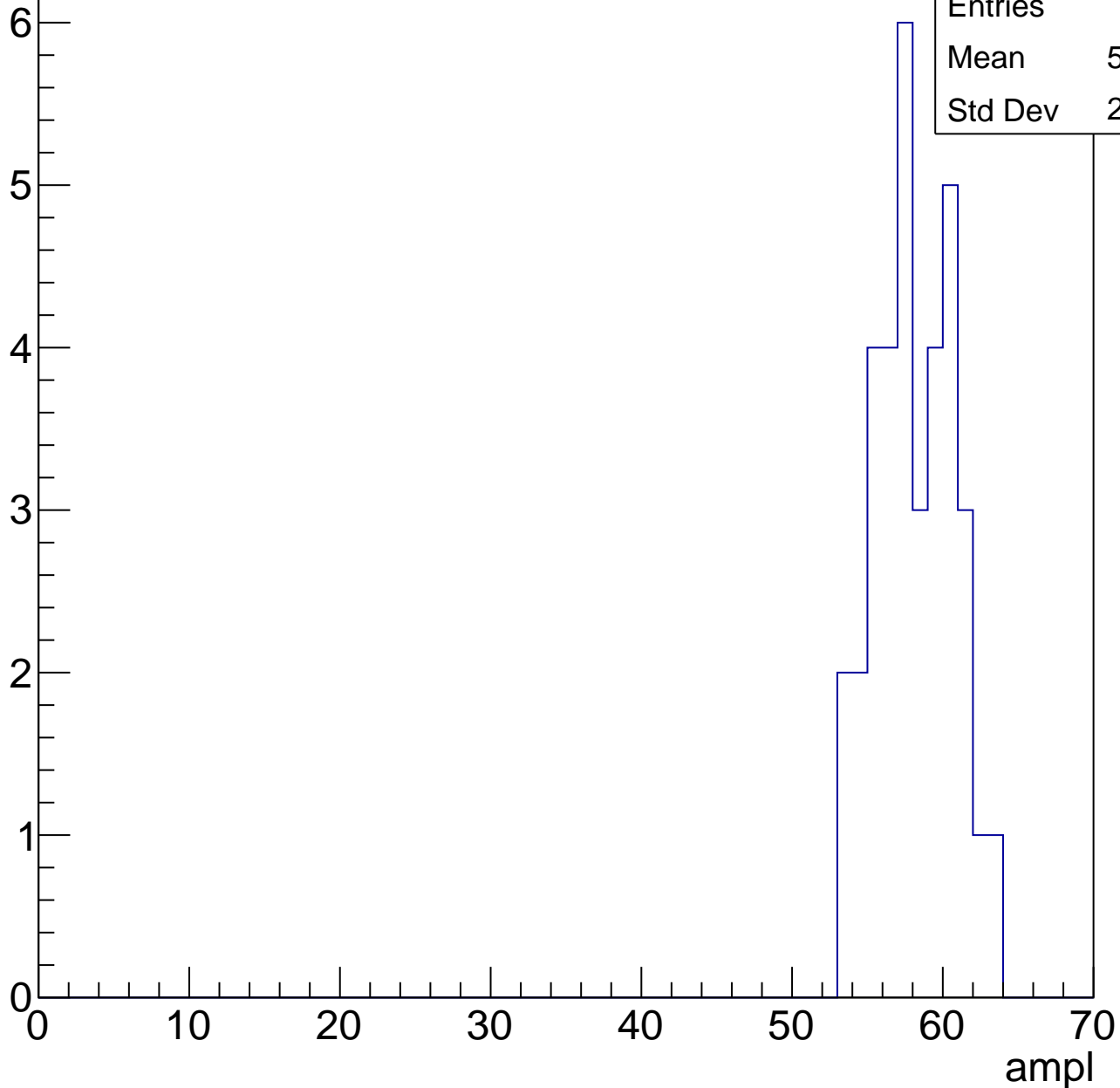
Entries	75
Mean	51.61
Std Dev	3.6



# B1L101S, U11-ch57, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



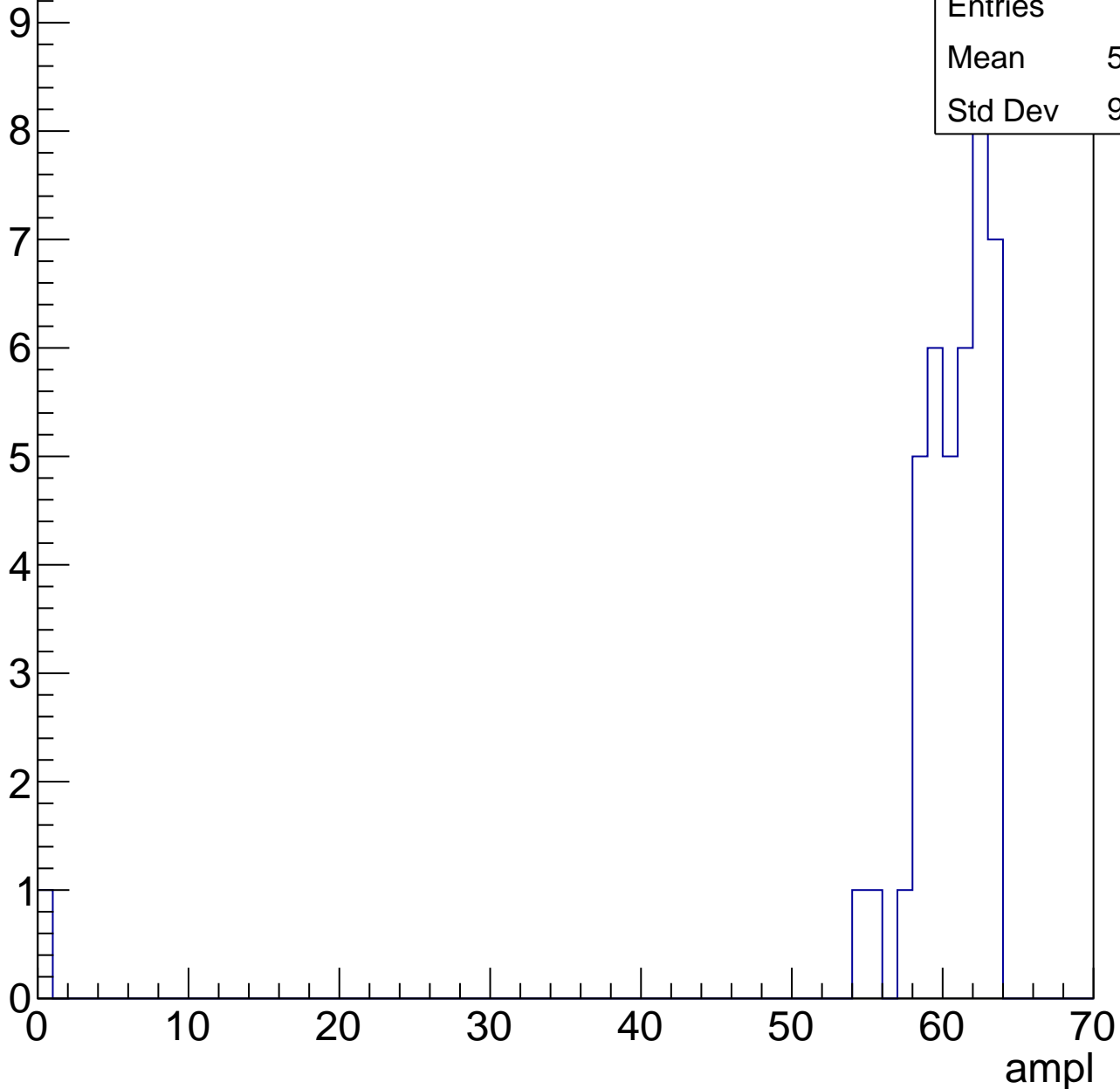
Entries	35
Mean	57.66
Std Dev	2.552

# B1L101S, U11-ch57, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

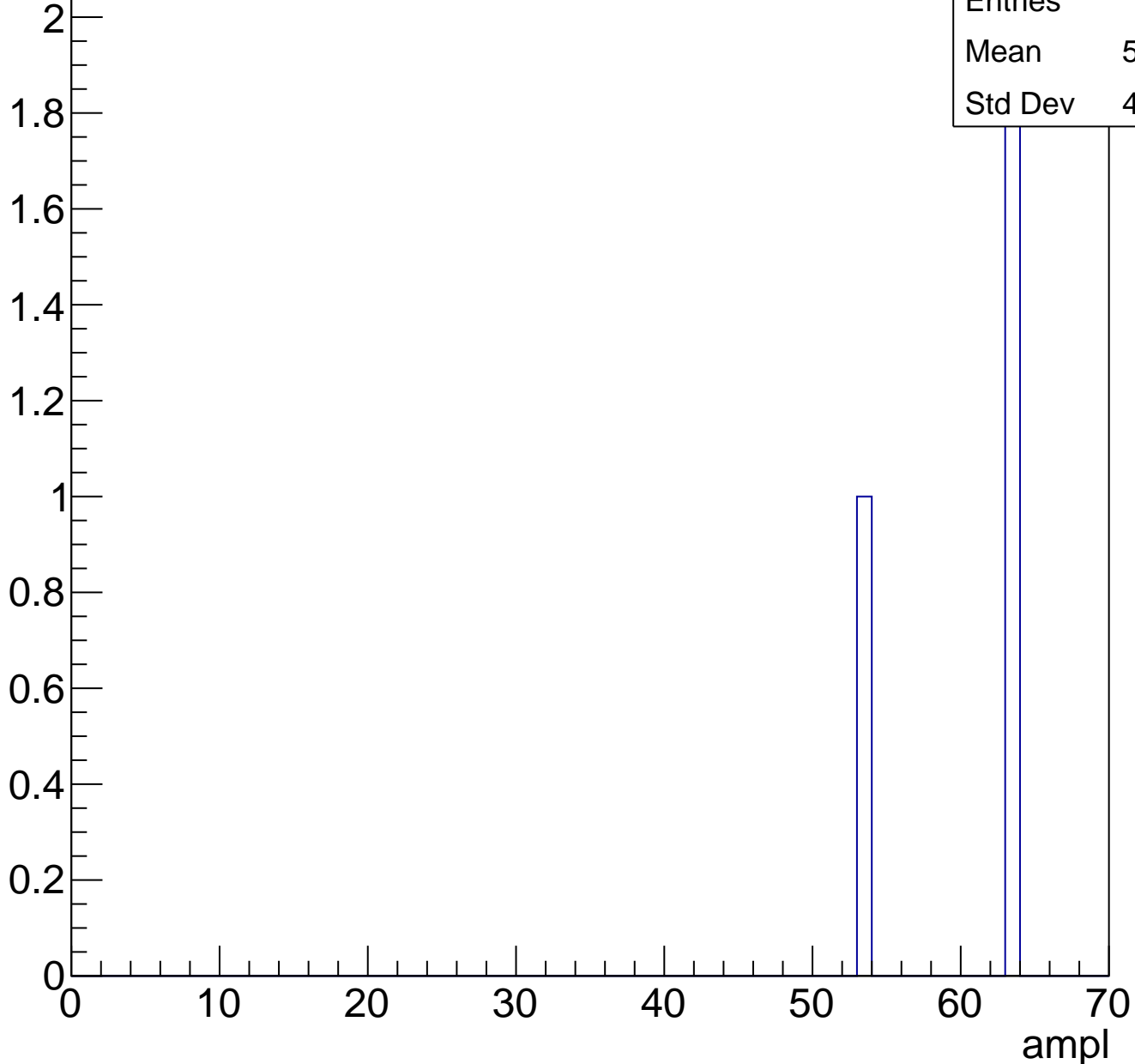
Entries	42
Mean	58.93
Std Dev	9.453



# B1L101S, U11-ch57, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



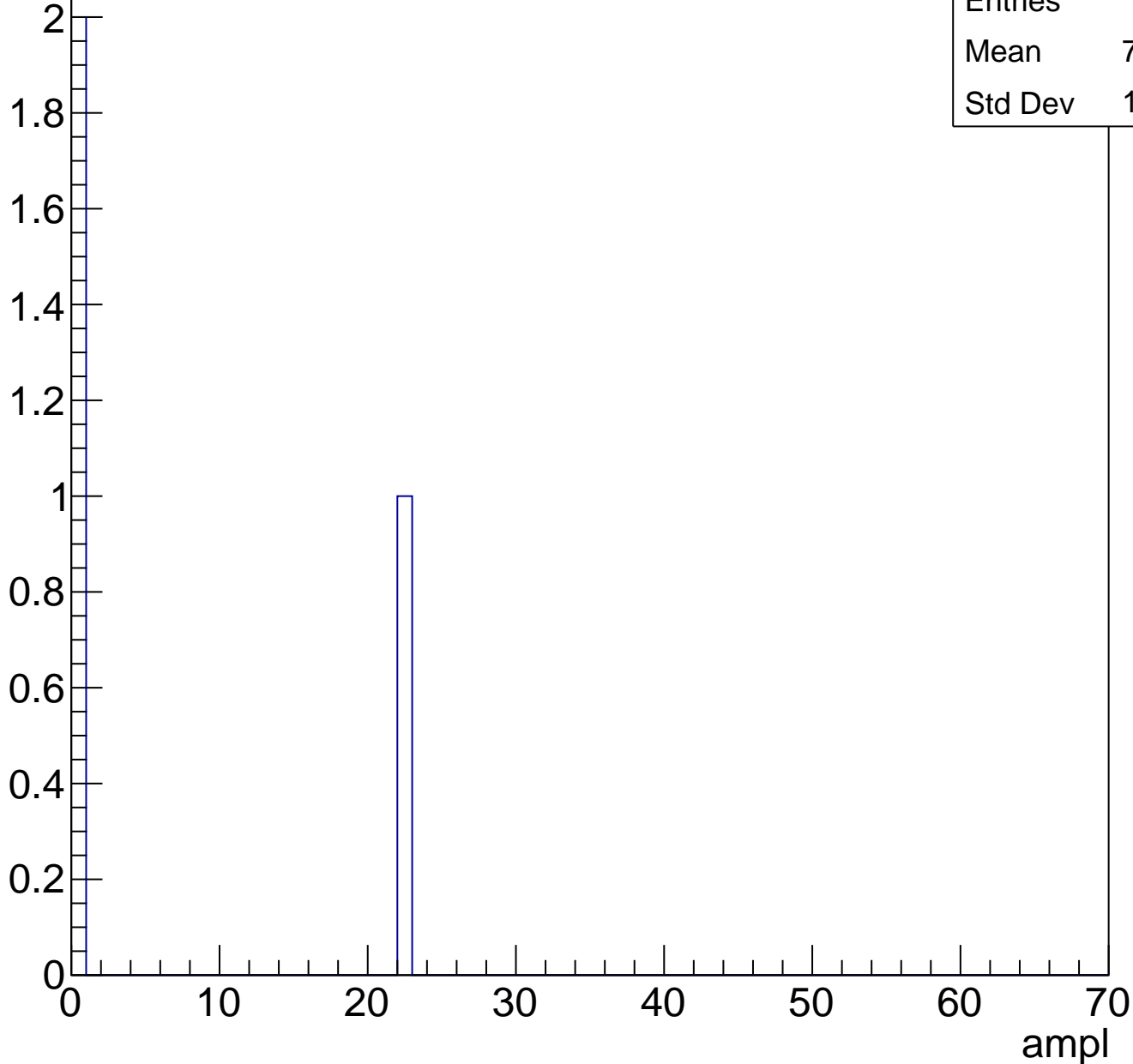
Entries	3
Mean	59.67
Std Dev	4.714



# B1L101S, U11-ch57, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U11-ch58, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	73
Mean	29.68
Std Dev	3.526

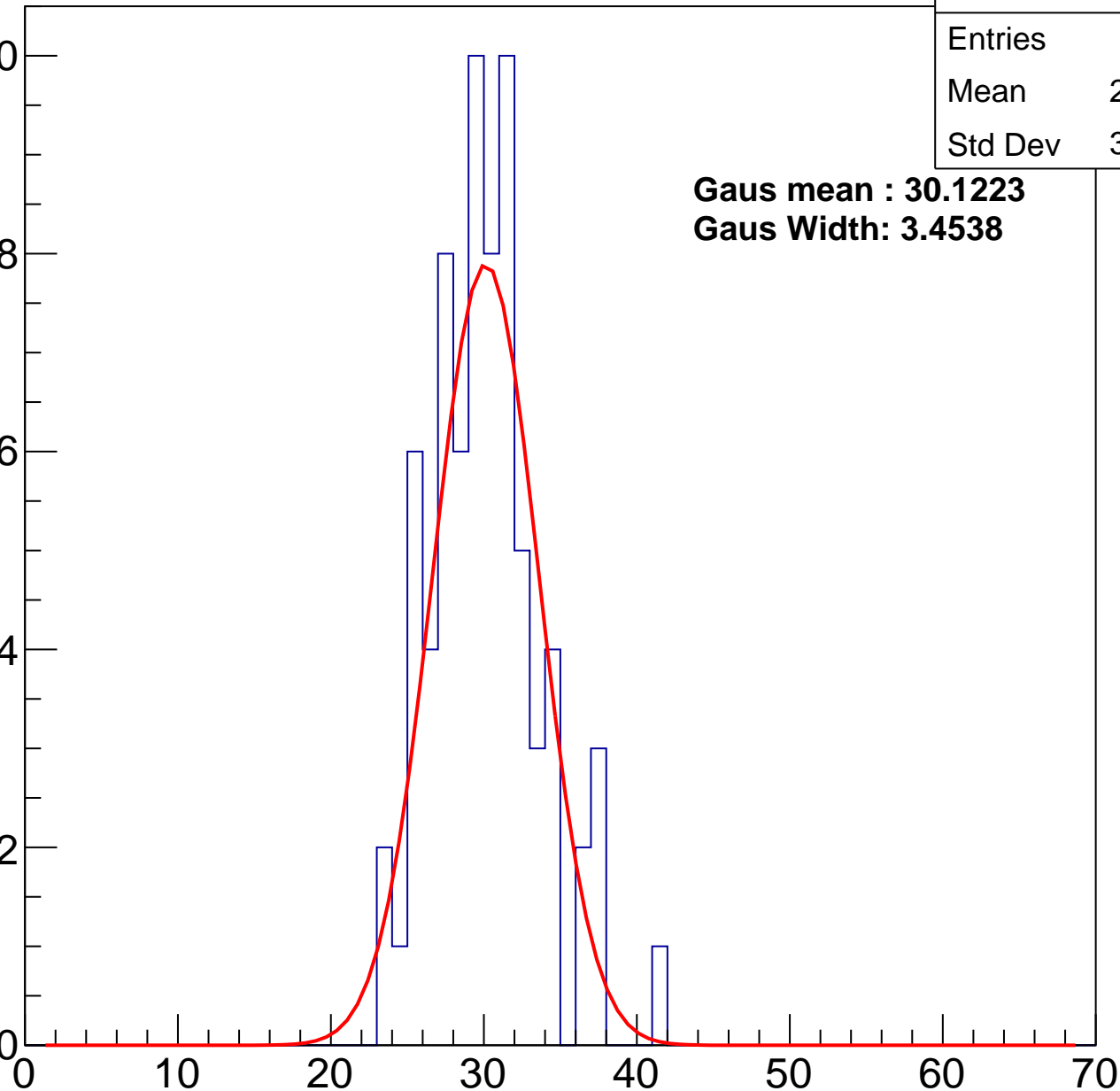
**Gaus mean : 30.1223**

**Gaus Width: 3.4538**

Entry

10  
8  
6  
4  
2  
0

ampl



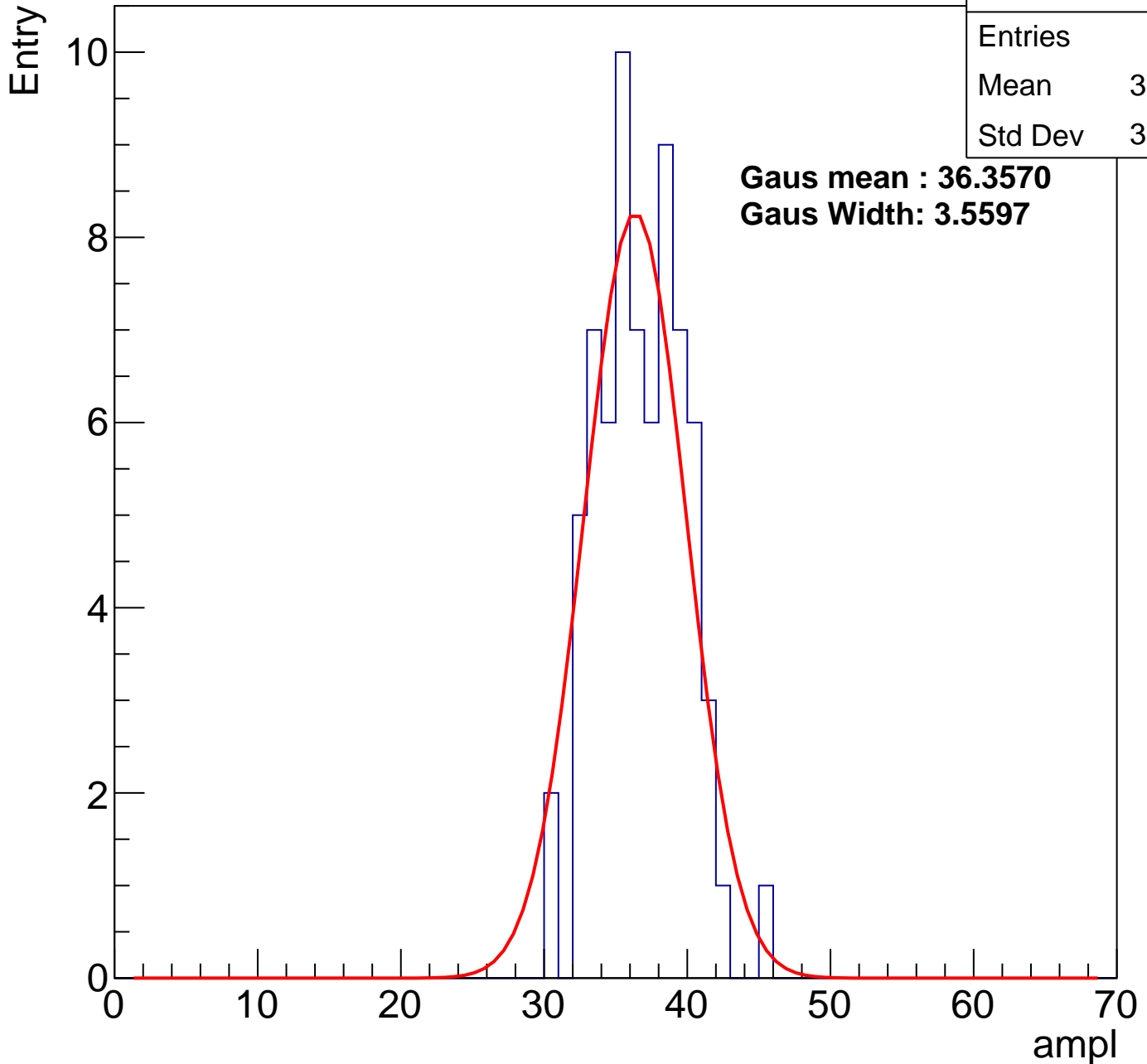
# B1L101S, U11-ch58, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	70
Mean	36.34
Std Dev	3.009

**Gaus mean : 36.3570**

**Gaus Width: 3.5597**



# B1L101S, U11-ch58, adc2

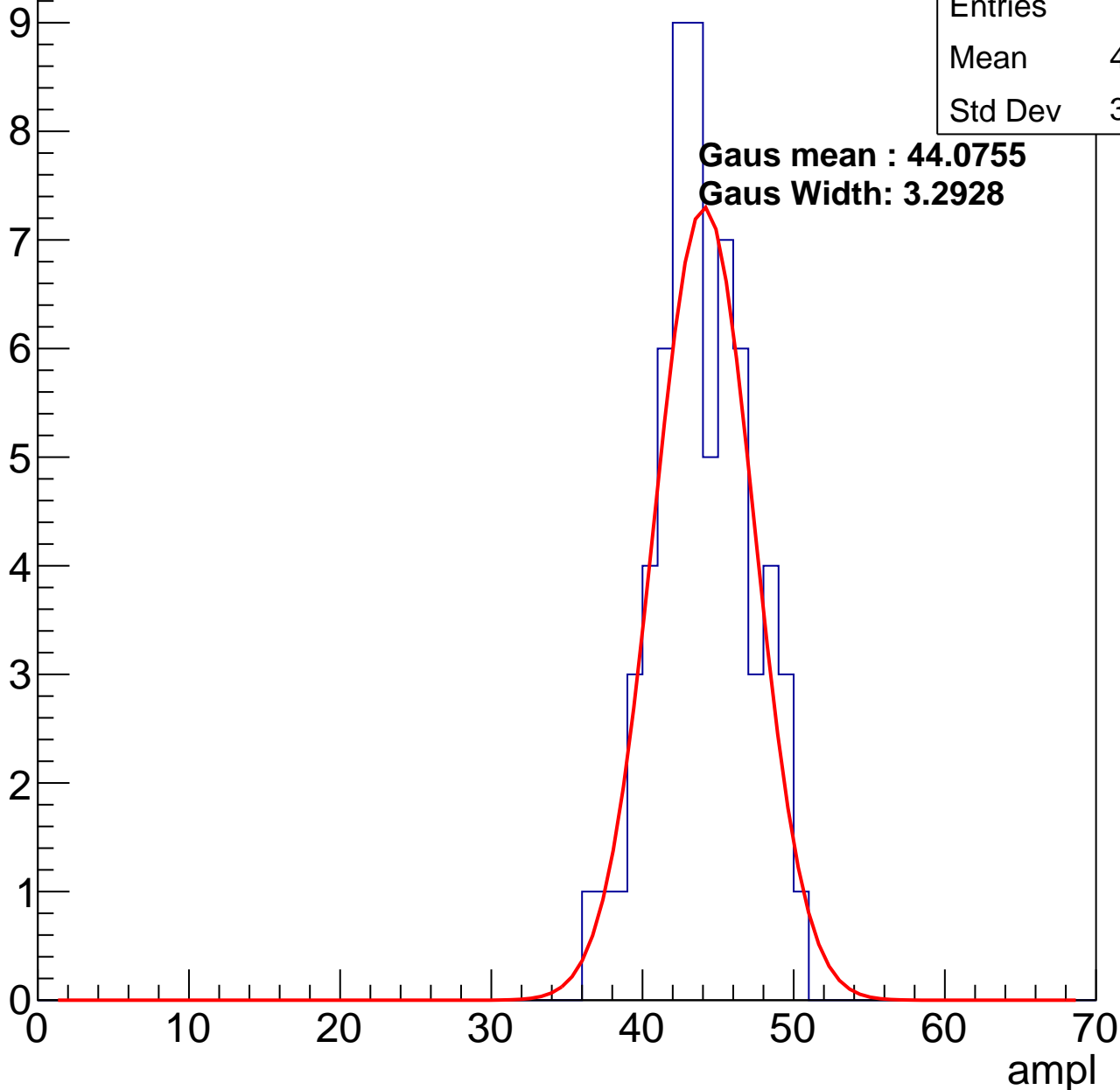
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	43.49
Std Dev	3.096

**Gaus mean : 44.0755**

**Gaus Width: 3.2928**

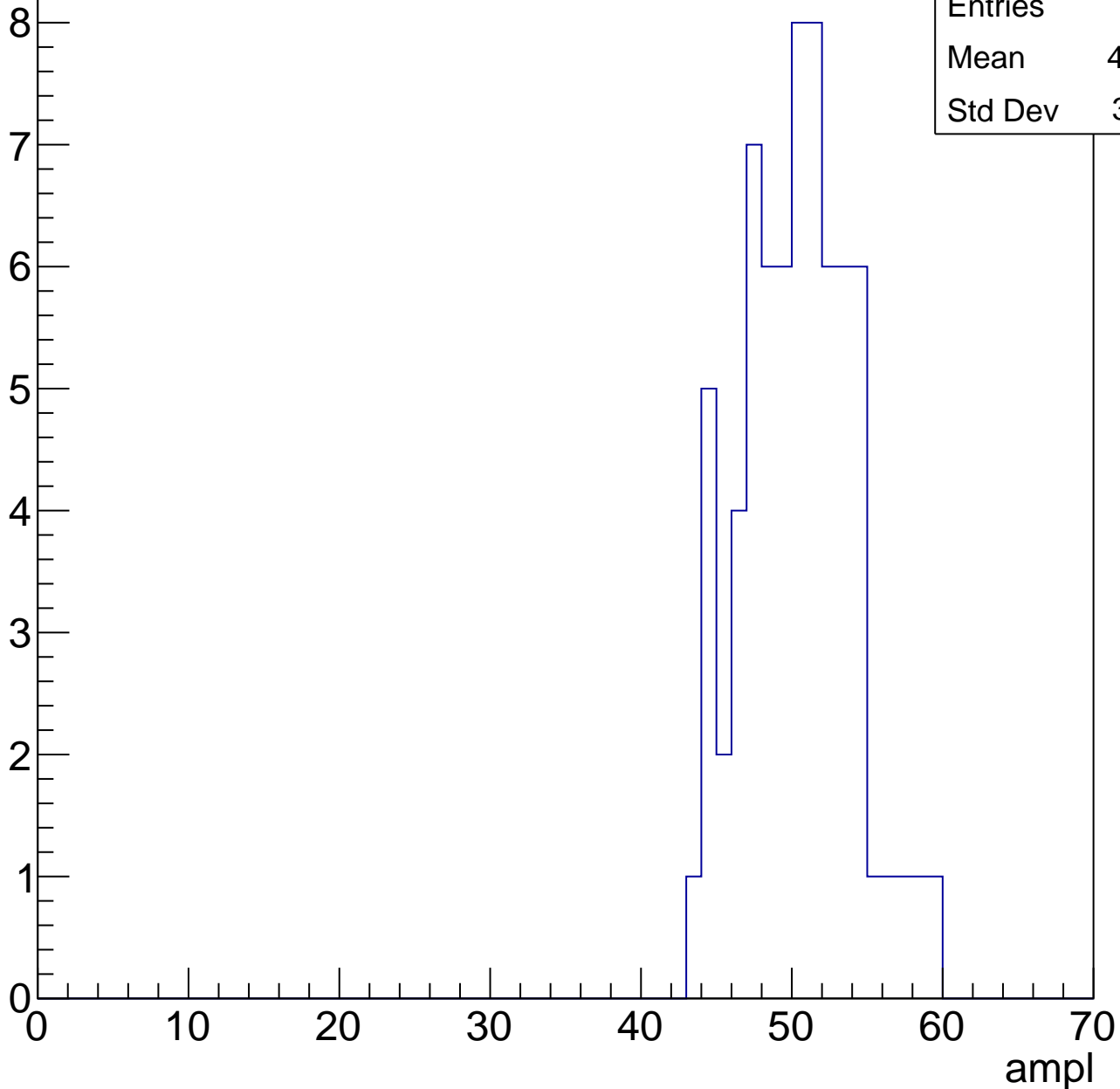


# B1L101S, U11-ch58, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

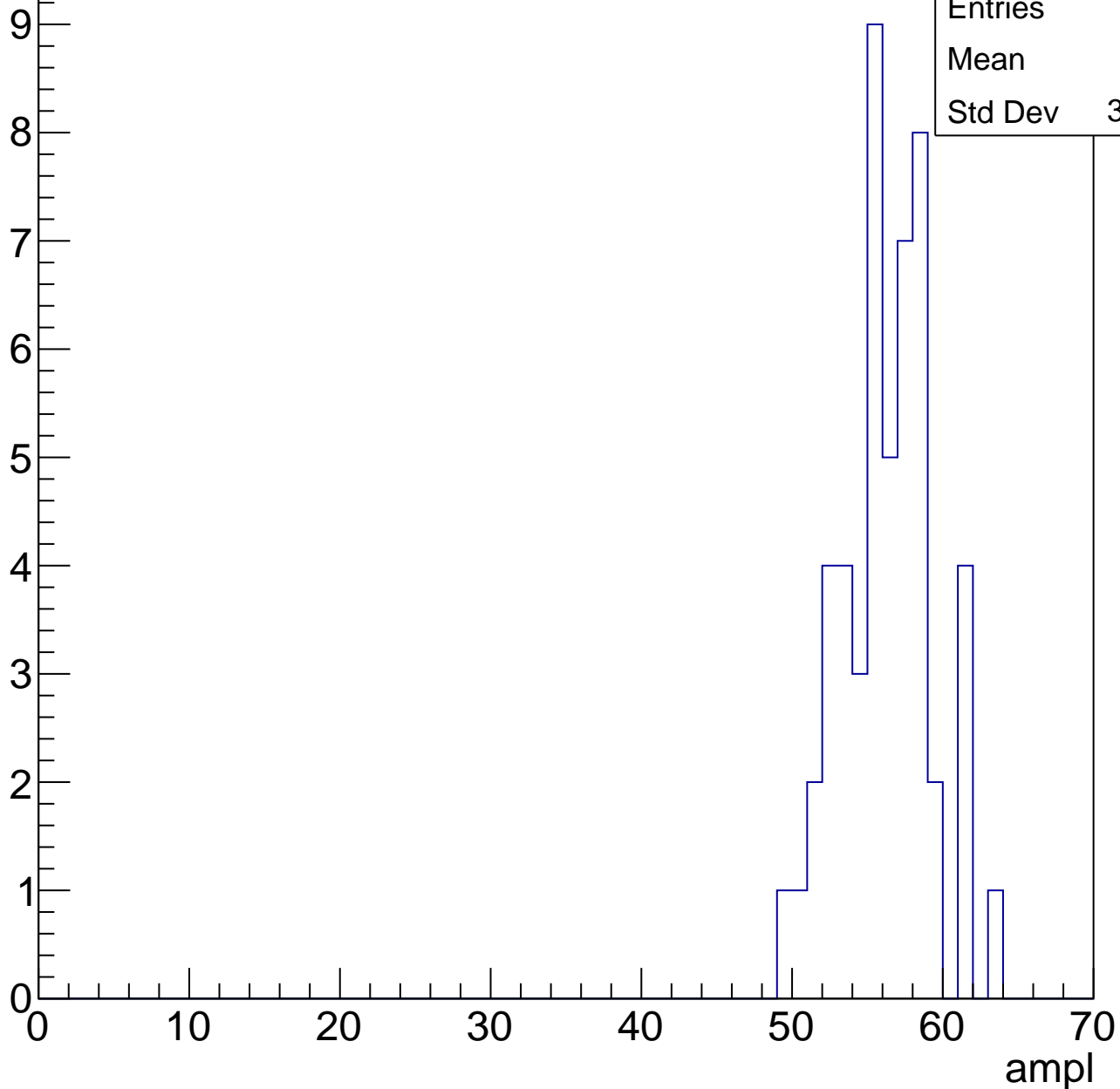
Entries	70
Mean	49.93
Std Dev	3.531



# B1L101S, U11-ch58, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

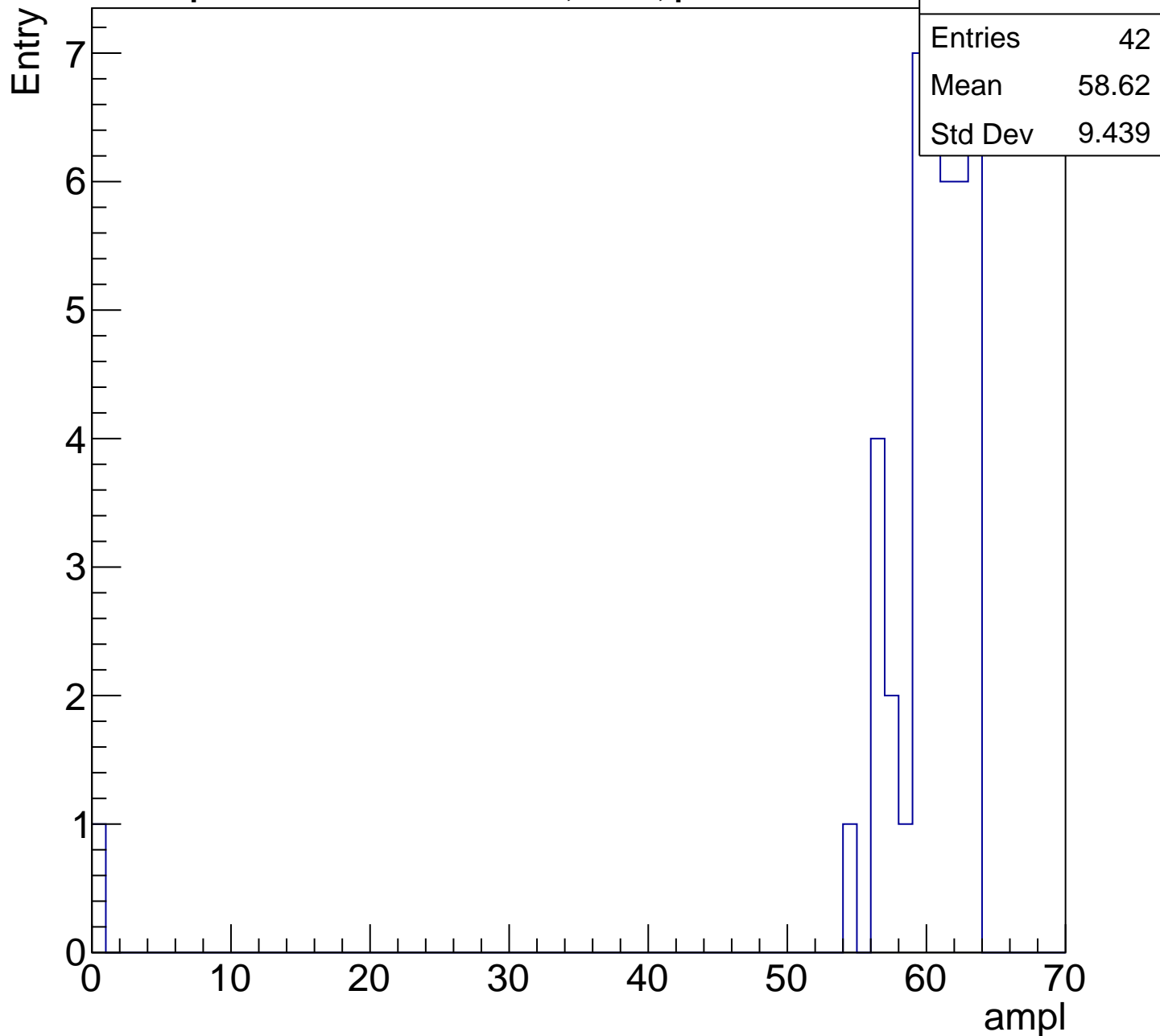
Entry



Entries	51
Mean	55.8
Std Dev	3.003

# B1L101S, U11-ch58, adc5

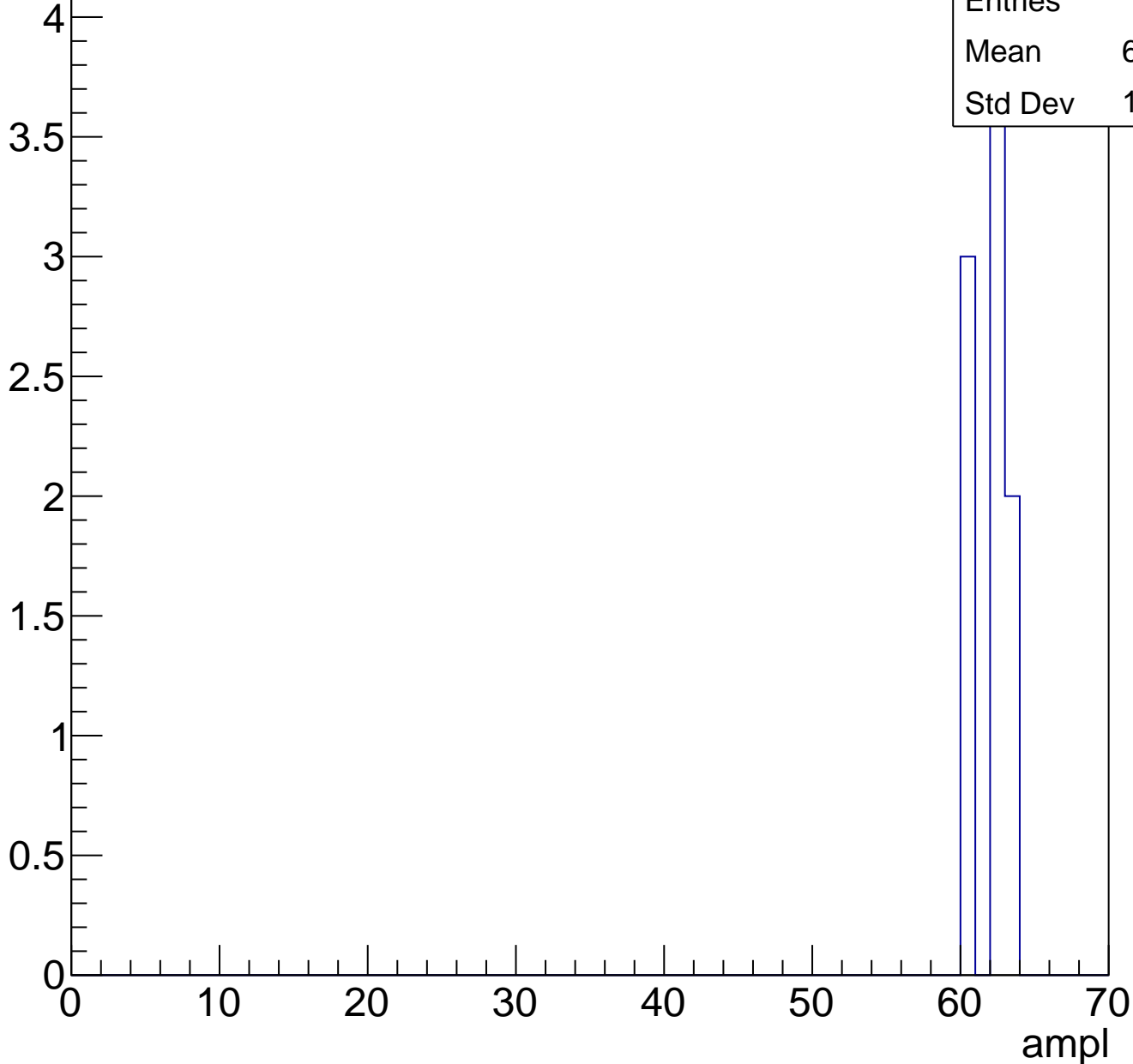
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U11-ch58, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

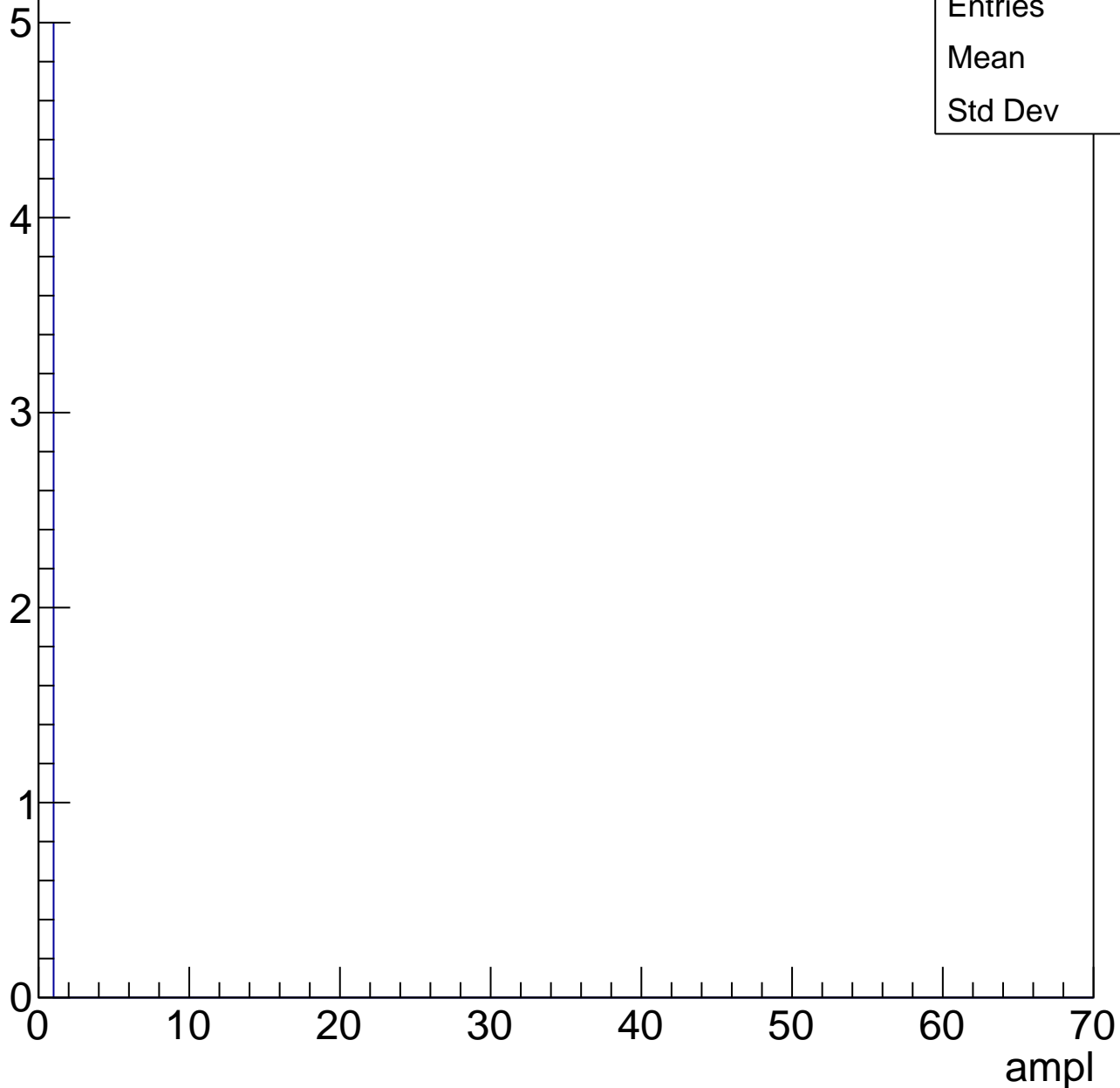




# B1L101S, U11-ch58, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	5
Mean	0
Std Dev	0

# B1L101S, U11-ch59, adc0

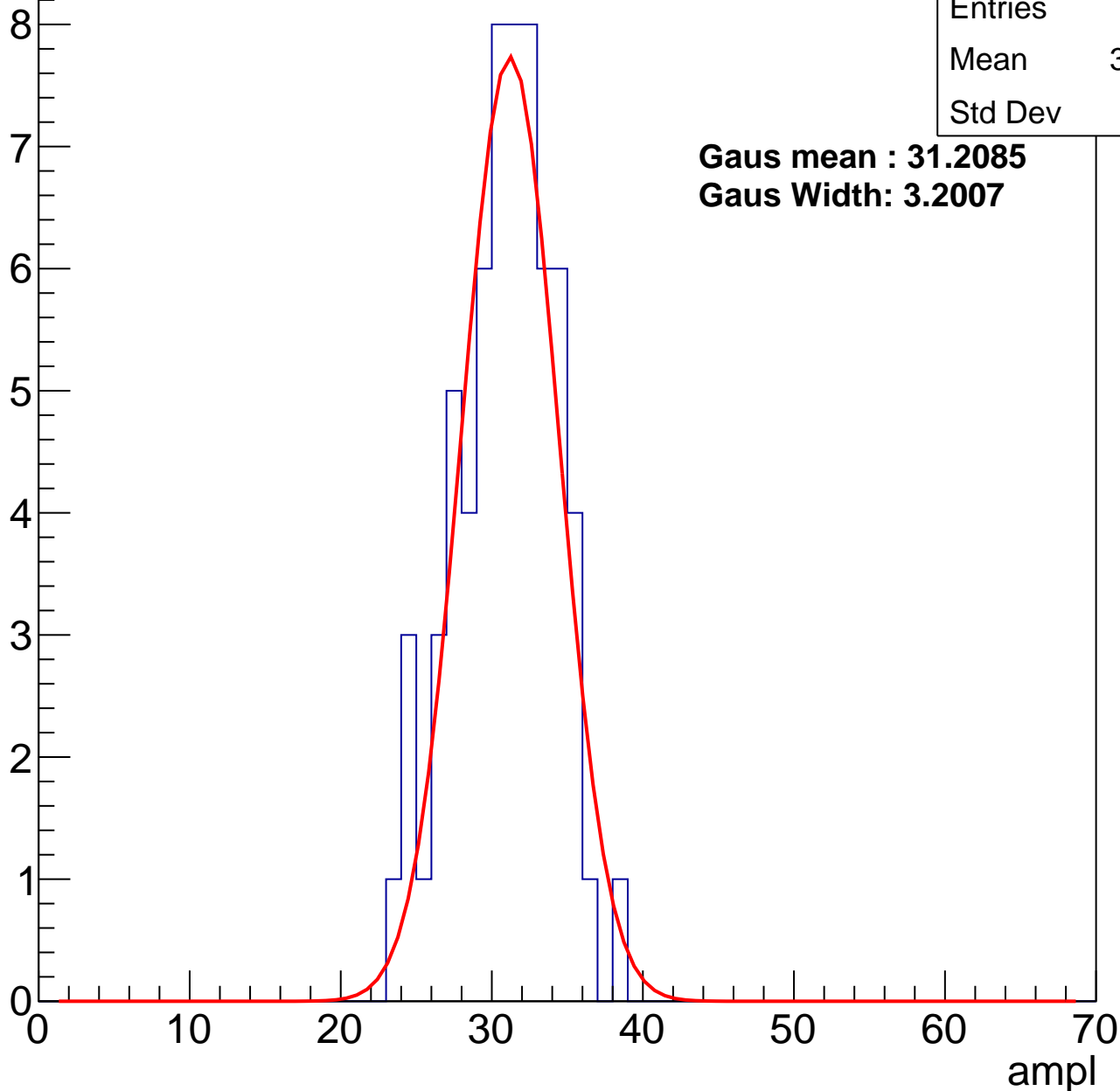
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	30.45
Std Dev	3.22

**Gaus mean : 31.2085**

**Gaus Width: 3.2007**



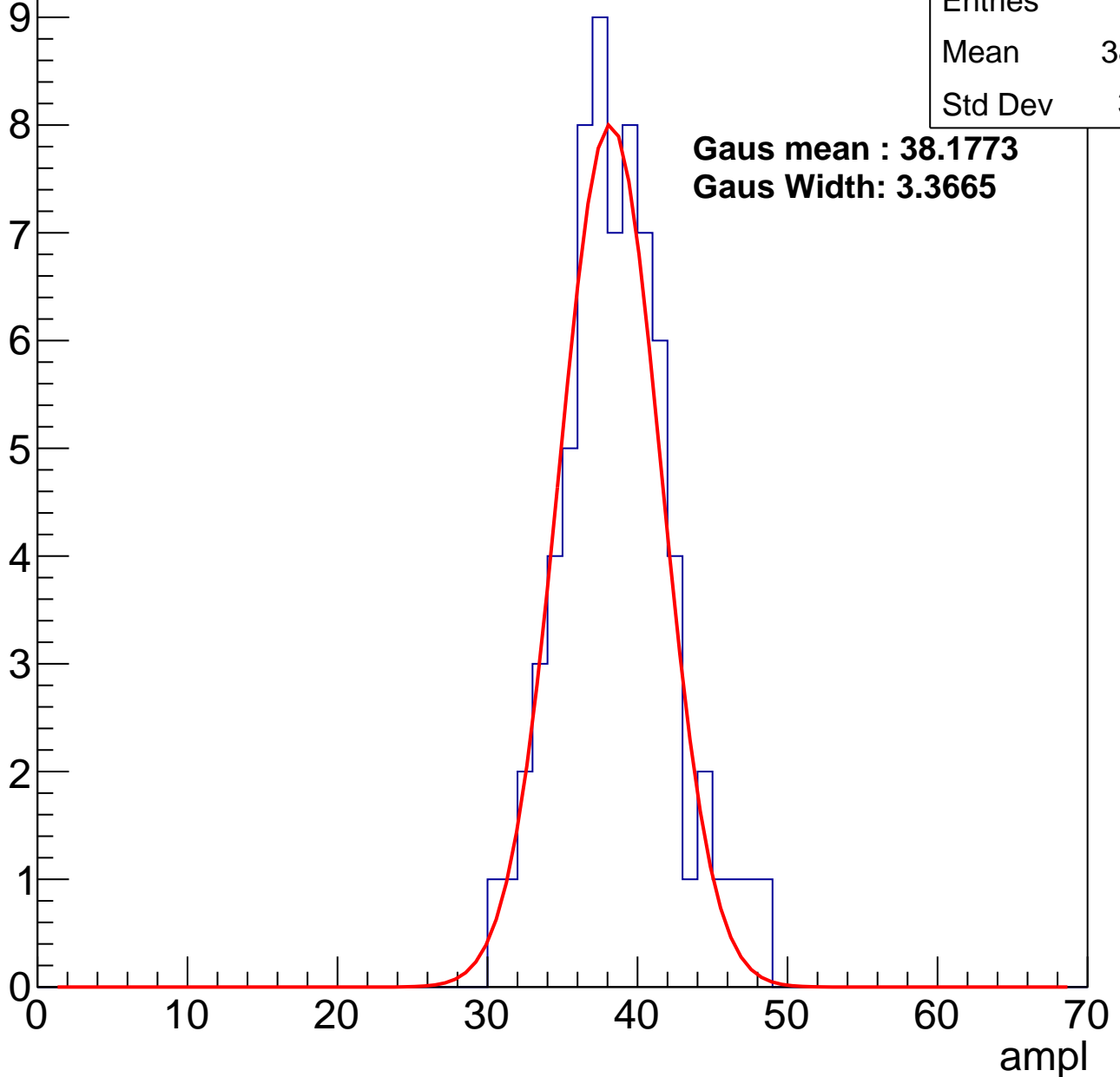
# B1L101S, U11-ch59, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	38.12
Std Dev	3.64

**Gaus mean : 38.1773**  
**Gaus Width: 3.3665**



# B1L101S, U11-ch59, adc2

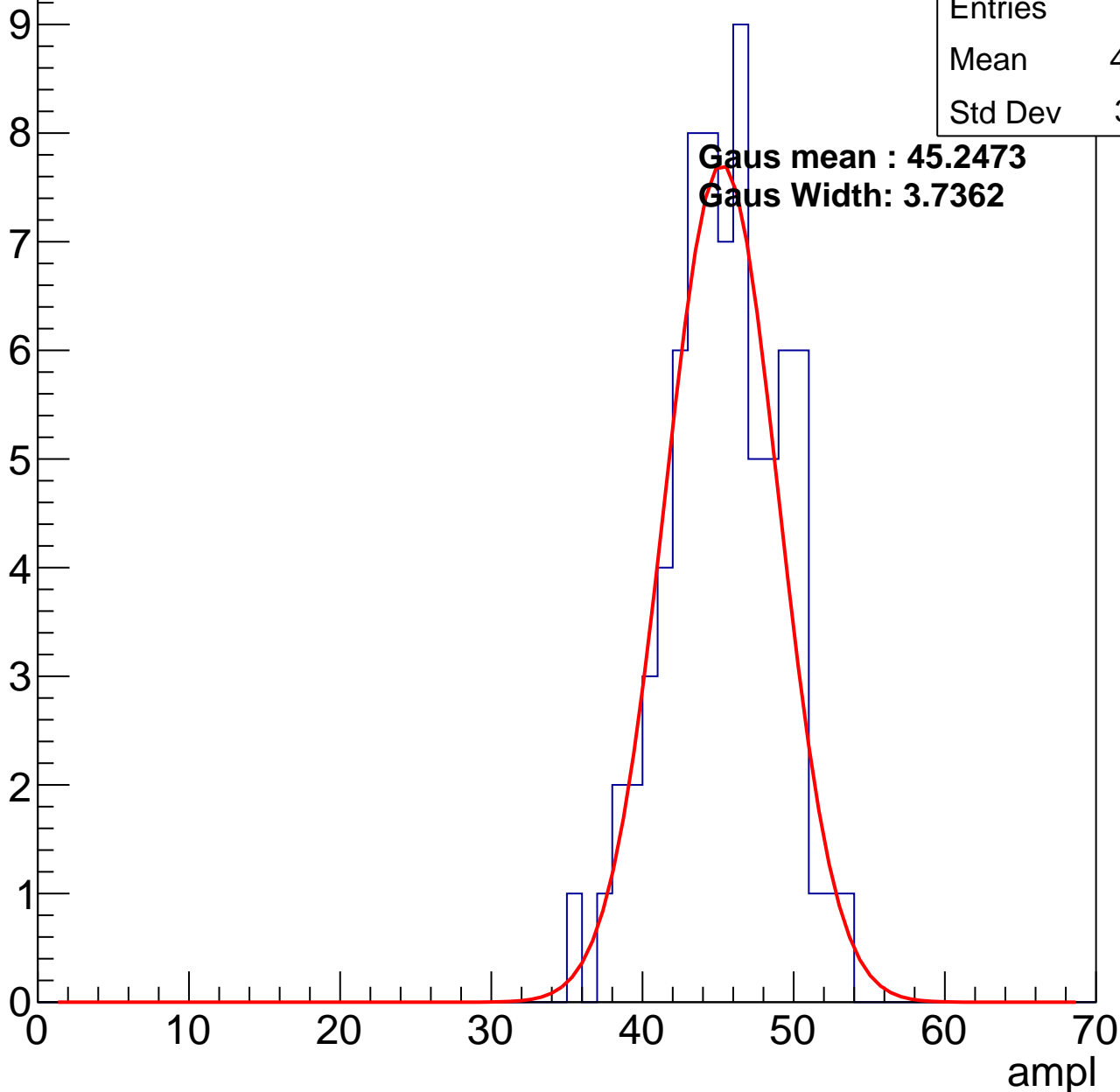
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	44.89
Std Dev	3.691

**Gaus mean : 45.2473**

**Gaus Width: 3.7362**

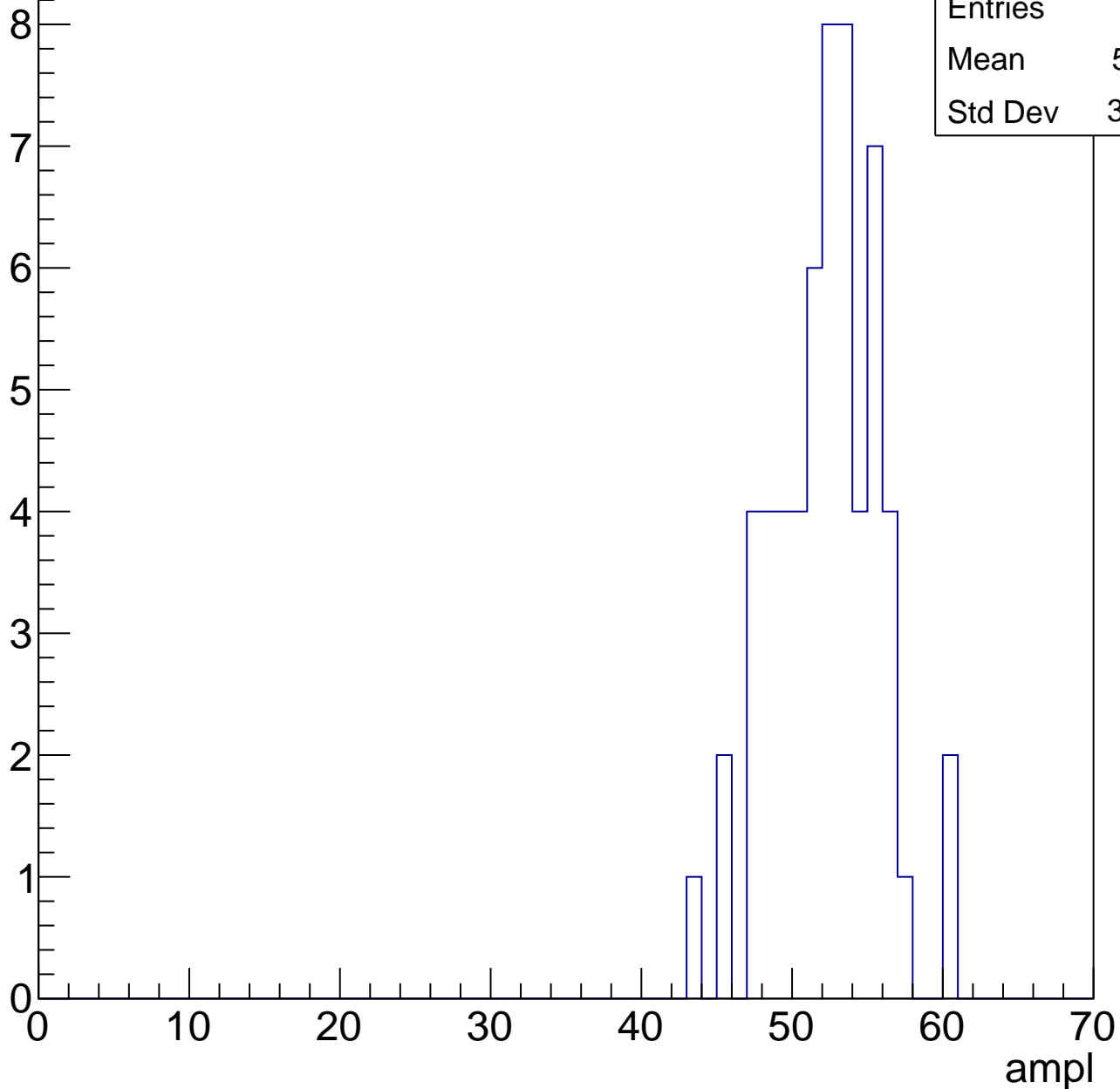


# B1L101S, U11-ch59, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

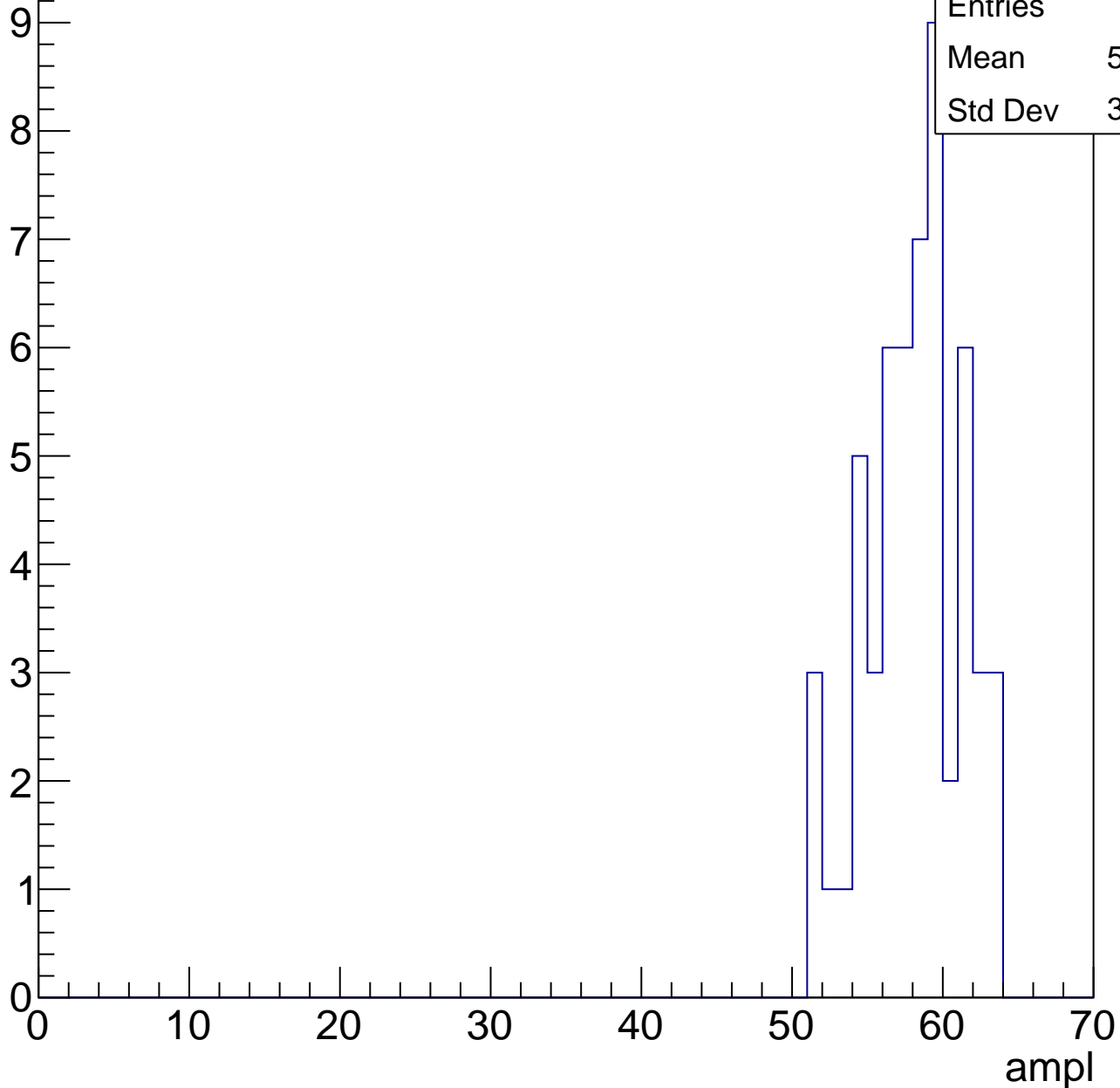
Entries	59
Mean	51.81
Std Dev	3.452



# B1L101S, U11-ch59, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

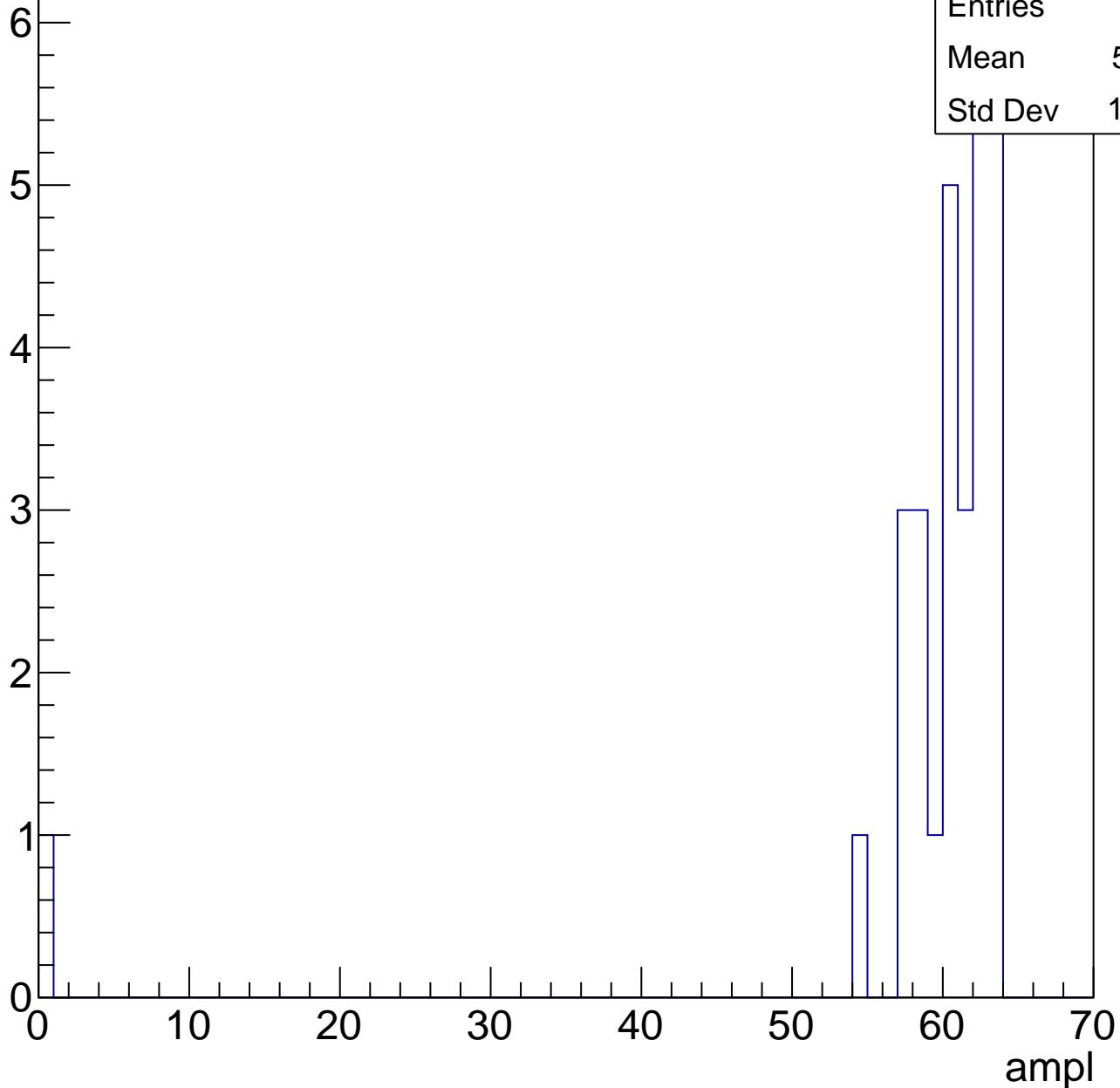


# B1L101S, U11-ch59, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

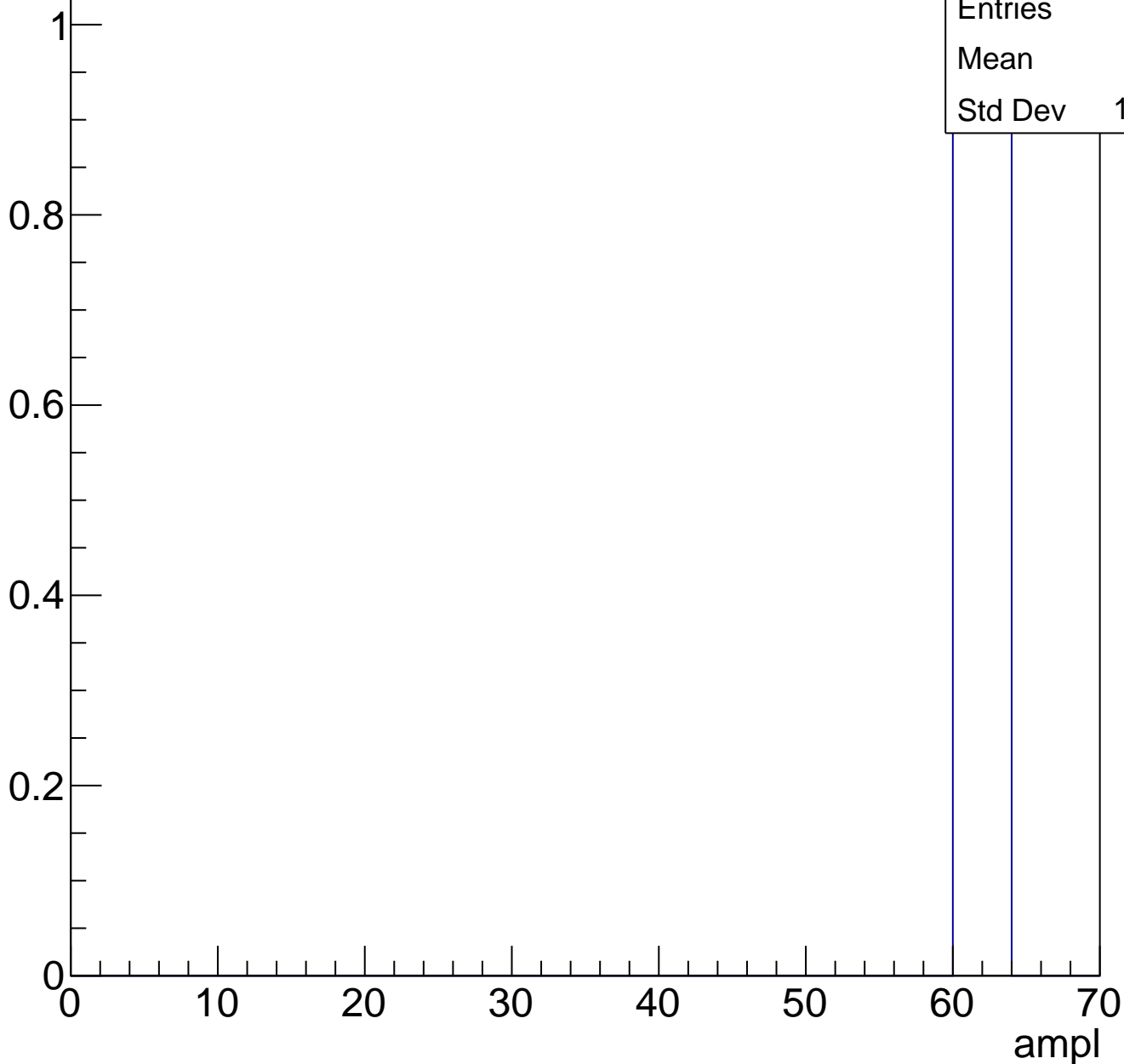
Entries	29
Mean	58.31
Std Dev	11.26



# B1L101S, U11-ch59, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch59, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U11-ch60, adc0

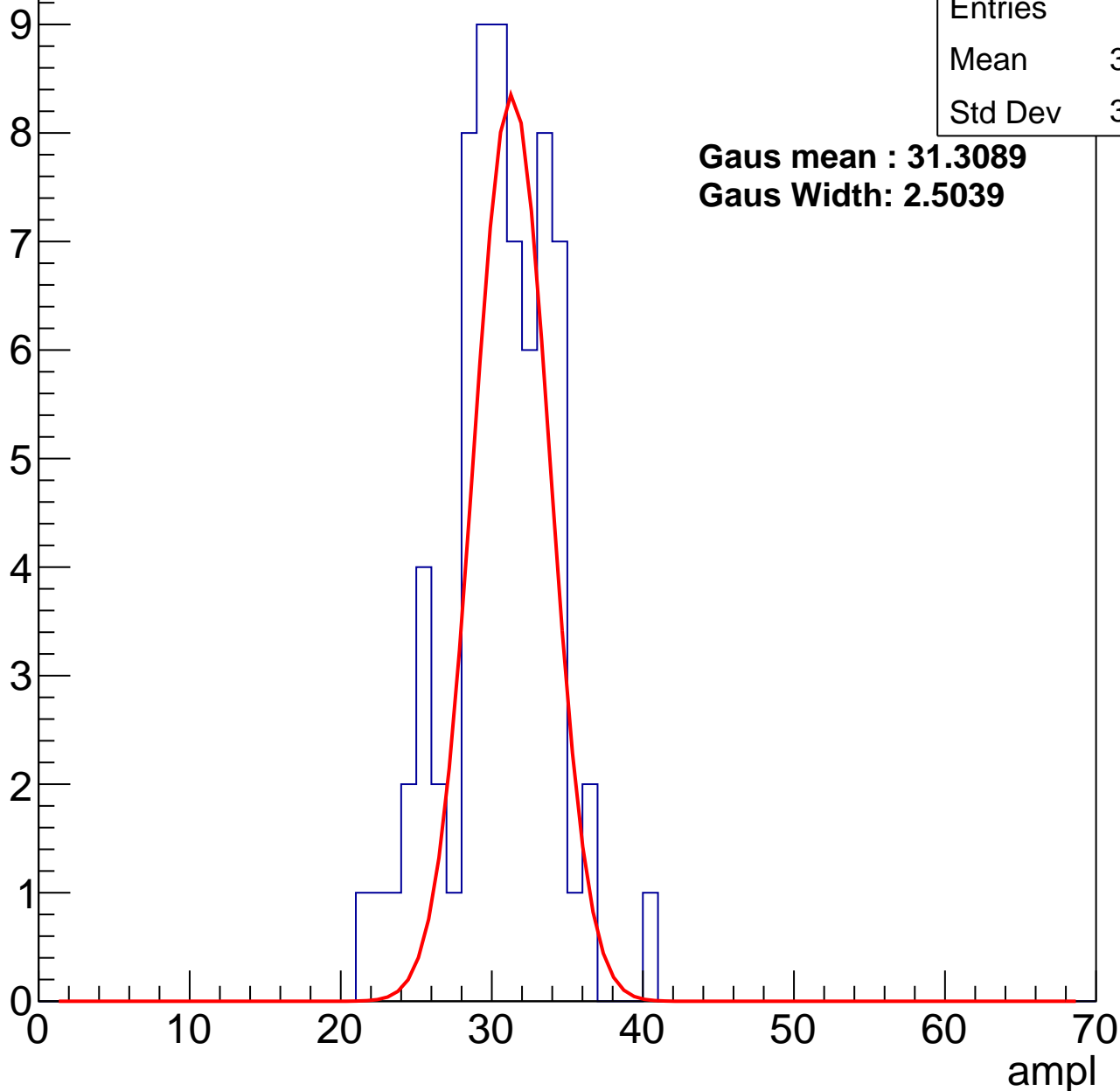
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	30.09
Std Dev	3.504

**Gaus mean : 31.3089**

**Gaus Width: 2.5039**



# B1L101S, U11-ch60, adc1

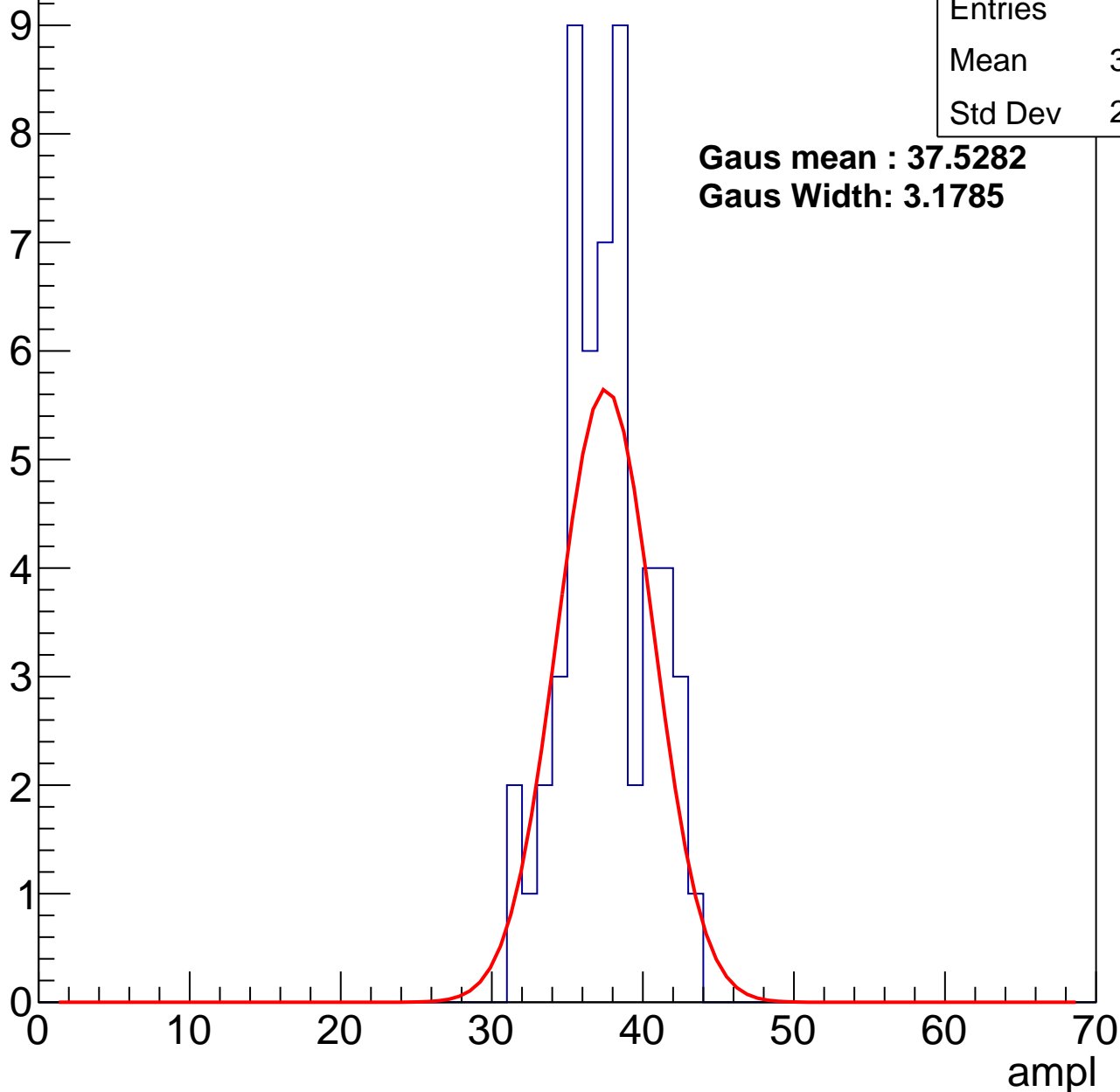
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	37.08
Std Dev	2.834

**Gaus mean : 37.5282**

**Gaus Width: 3.1785**



# B1L101S, U11-ch60, adc2

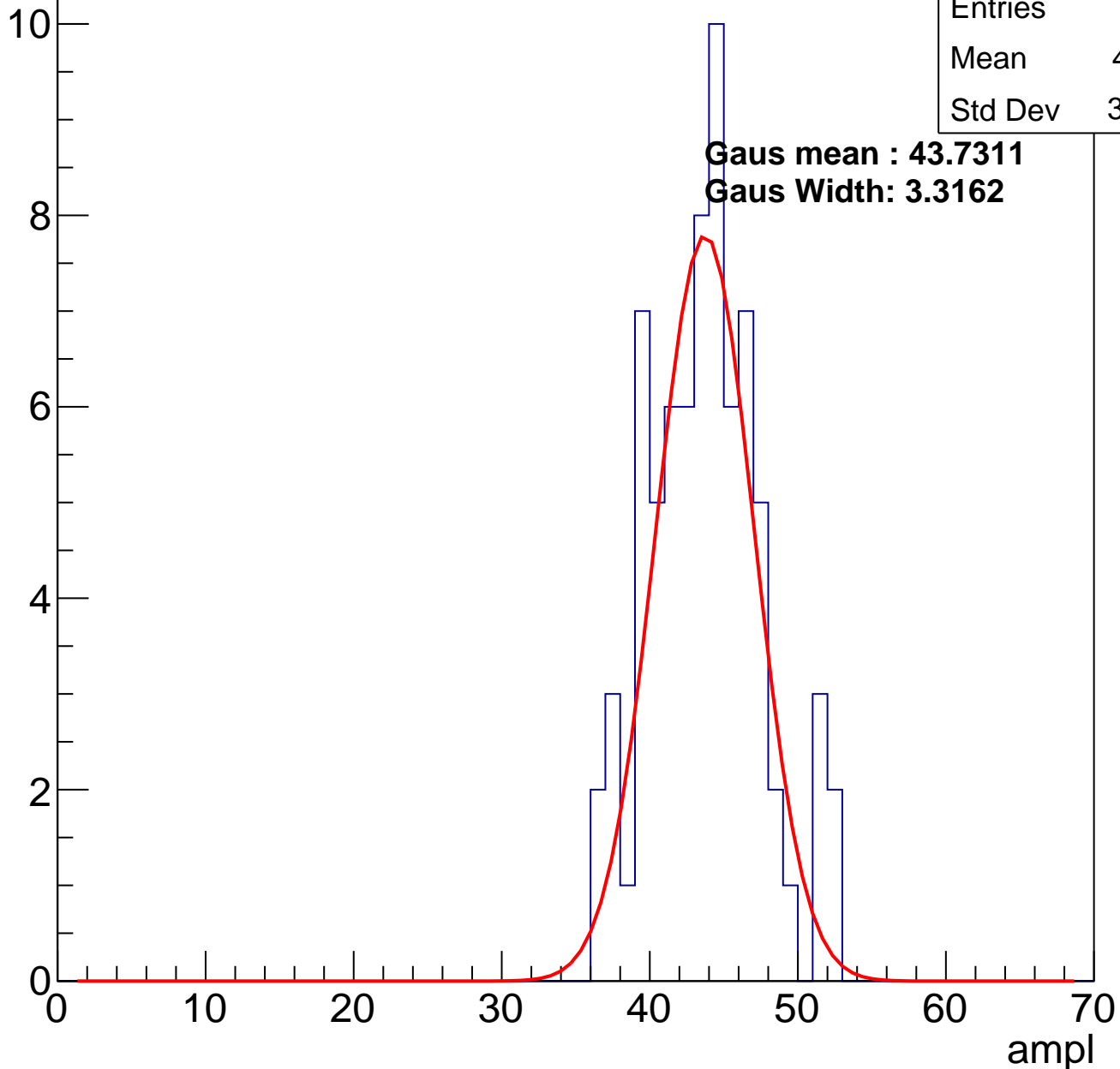
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	74
Mean	43.31
Std Dev	3.727

**Gaus mean : 43.7311**

**Gaus Width: 3.3162**

Entry

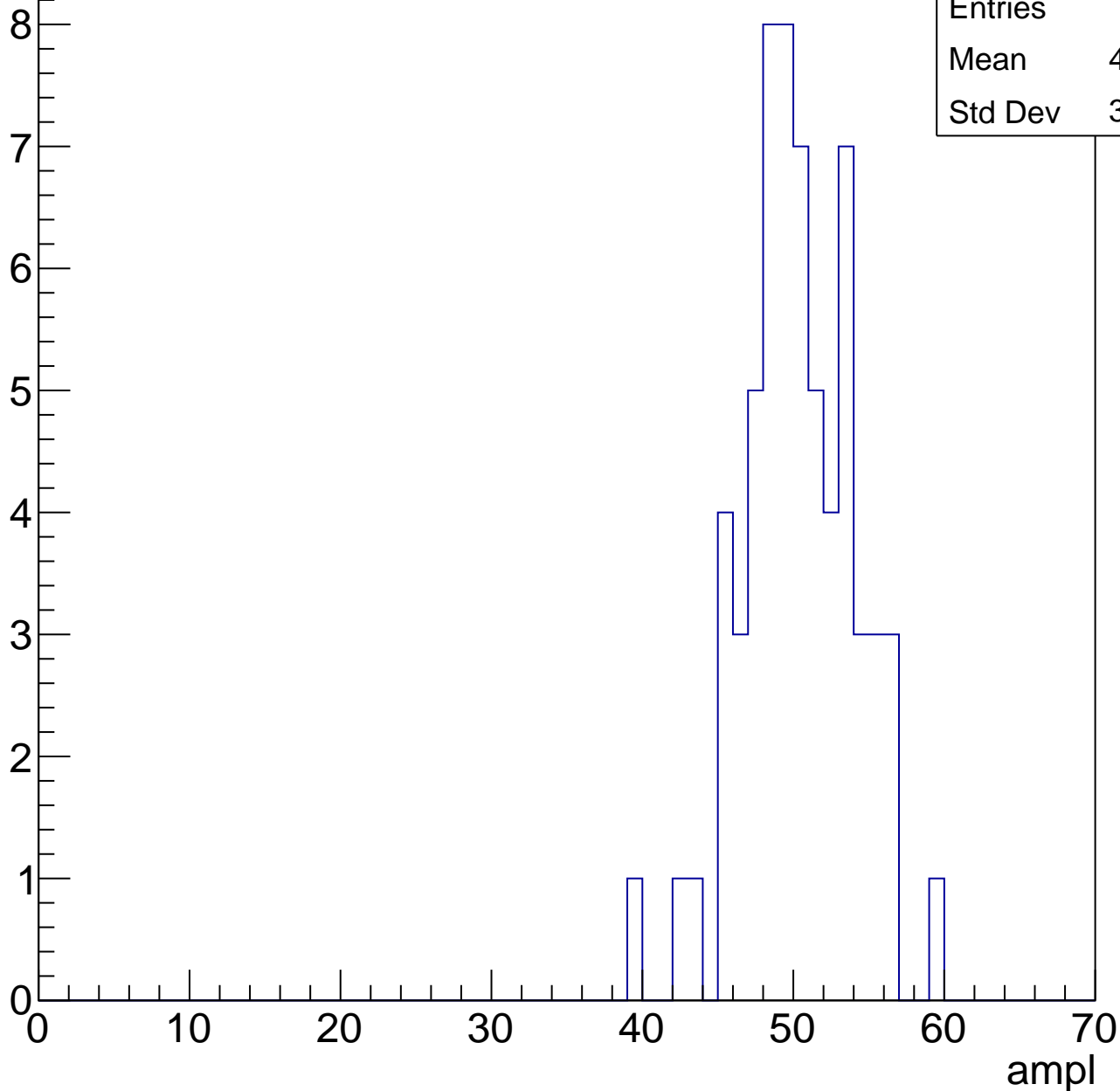


# B1L101S, U11-ch60, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

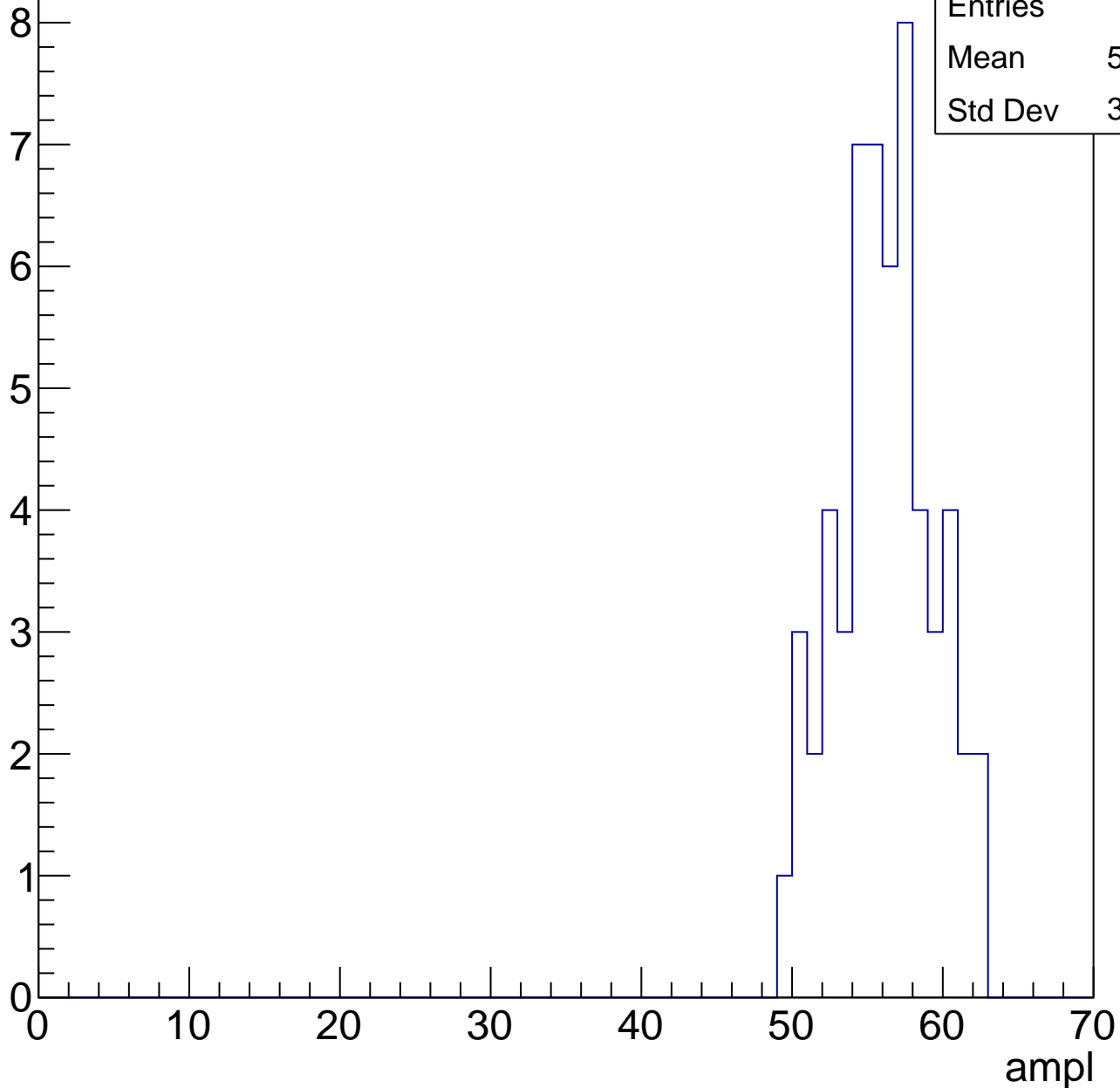
Entries	64
Mean	49.86
Std Dev	3.669



# B1L101S, U11-ch60, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

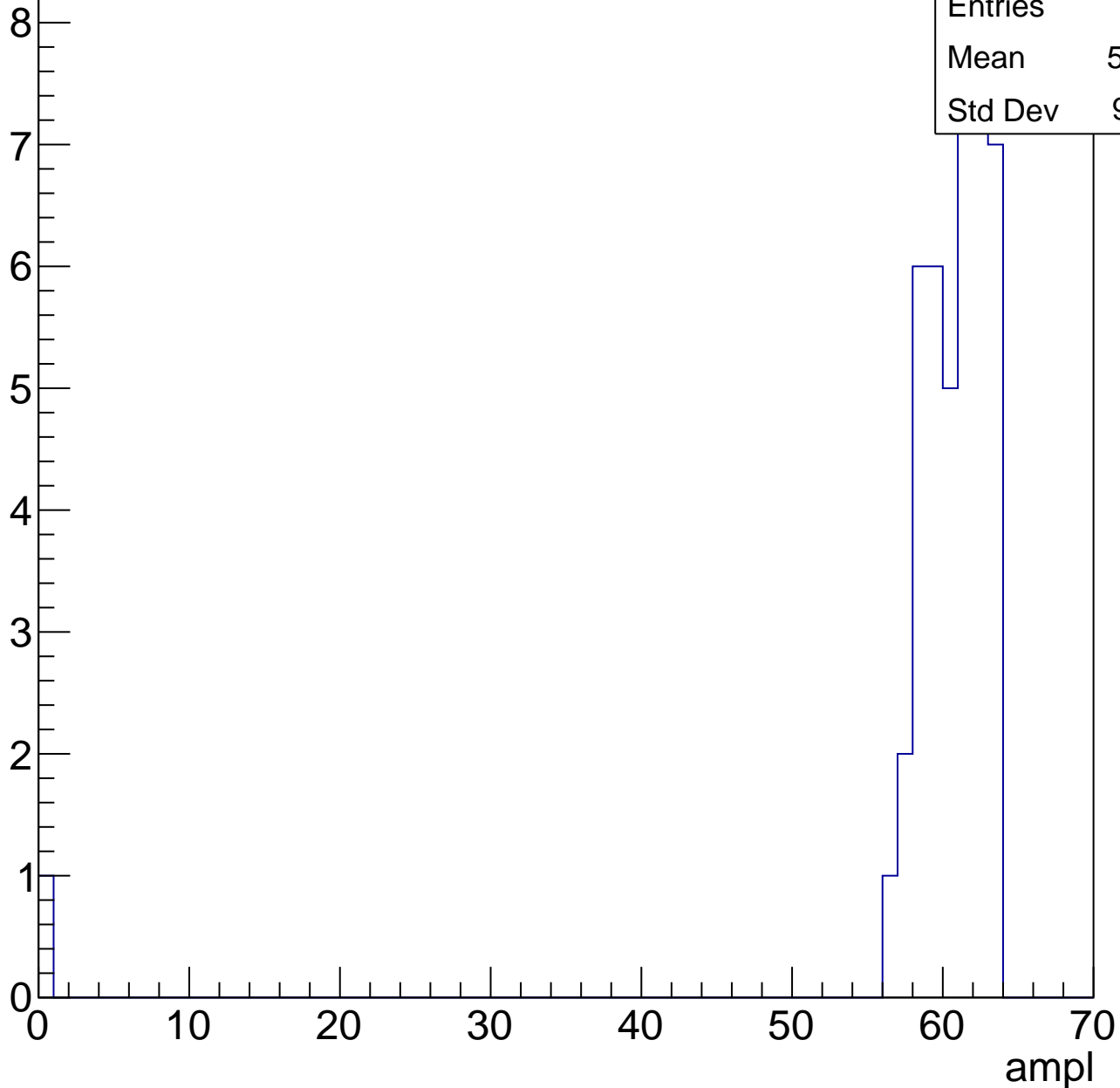
Entry



# B1L101S, U11-ch60, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U11-ch60, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch60, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U11-ch61, adc0

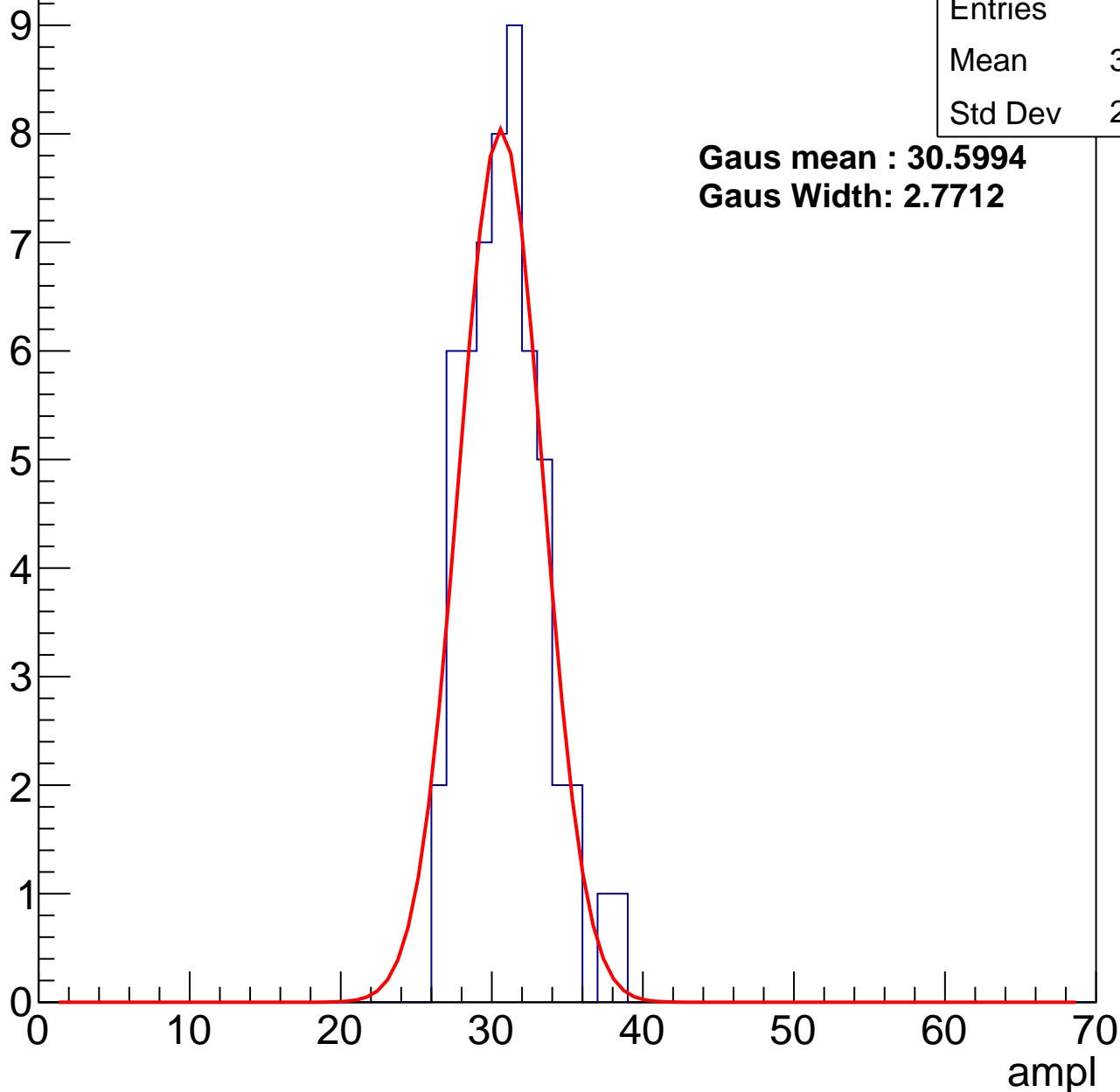
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	30.44
Std Dev	2.627

**Gaus mean : 30.5994**

**Gaus Width: 2.7712**



# B1L101S, U11-ch61, adc1

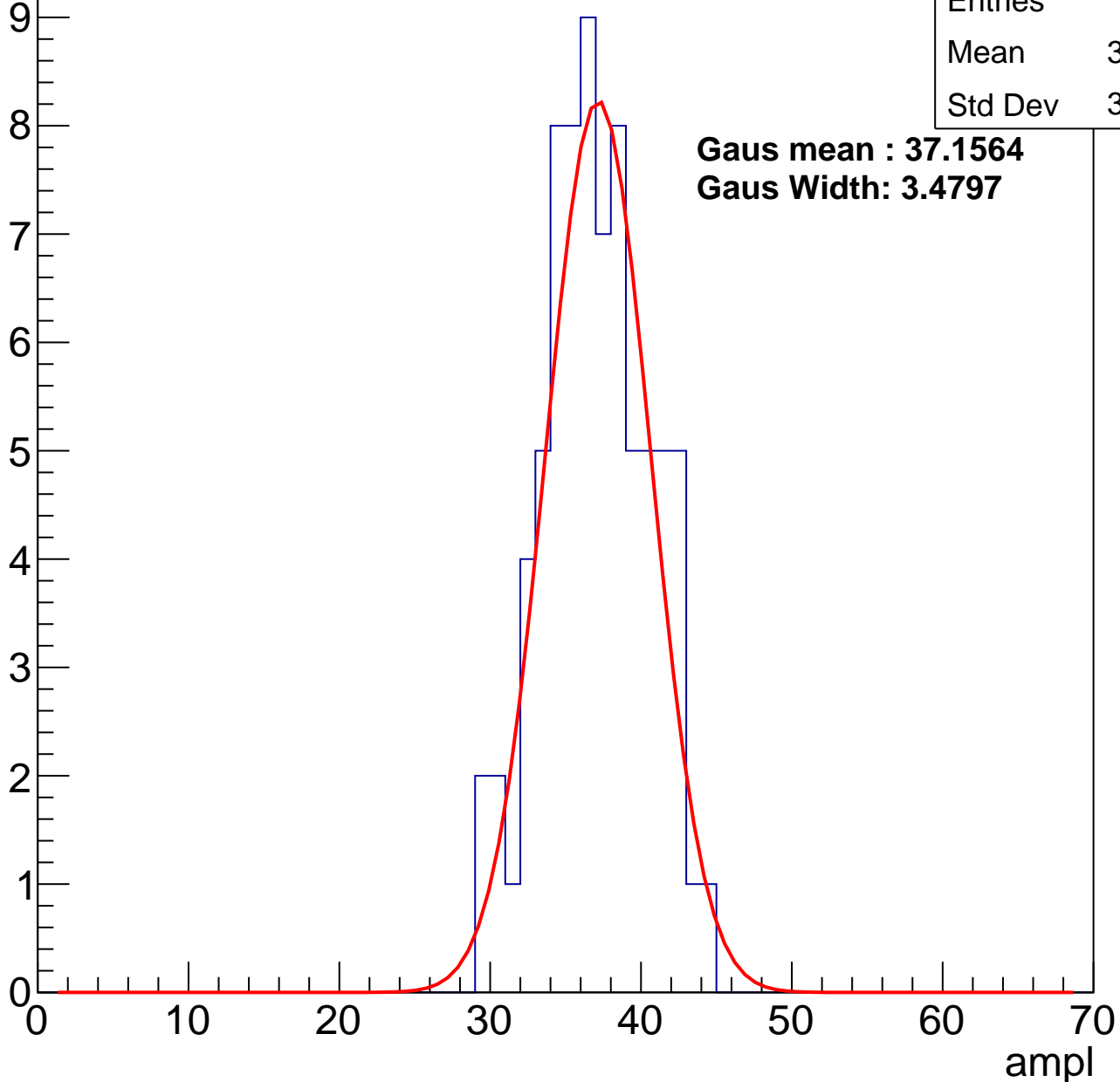
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	36.55
Std Dev	3.447

**Gaus mean : 37.1564**

**Gaus Width: 3.4797**



# B1L101S, U11-ch61, adc2

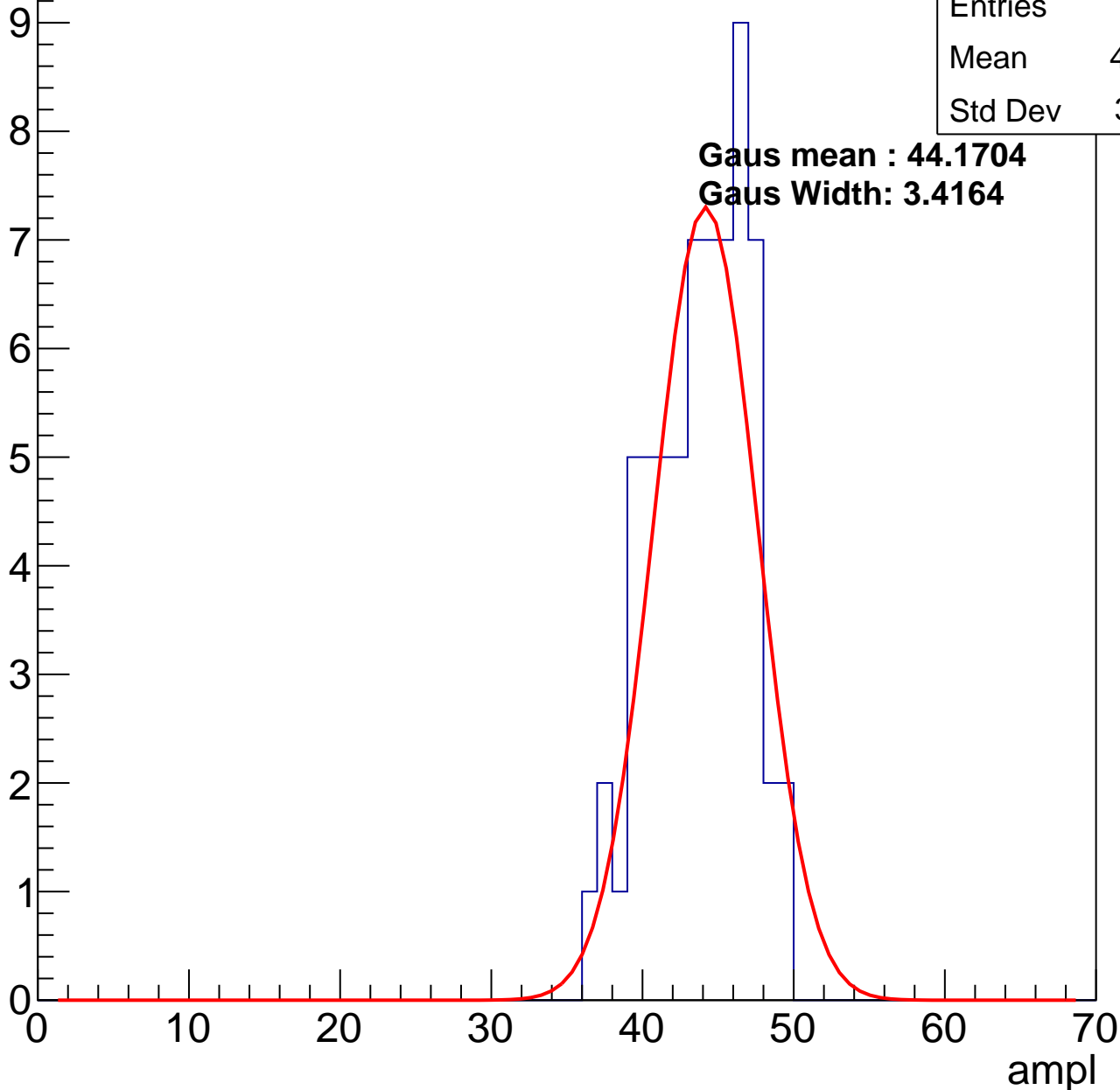
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	43.37
Std Dev	3.131

**Gaus mean : 44.1704**

**Gaus Width: 3.4164**

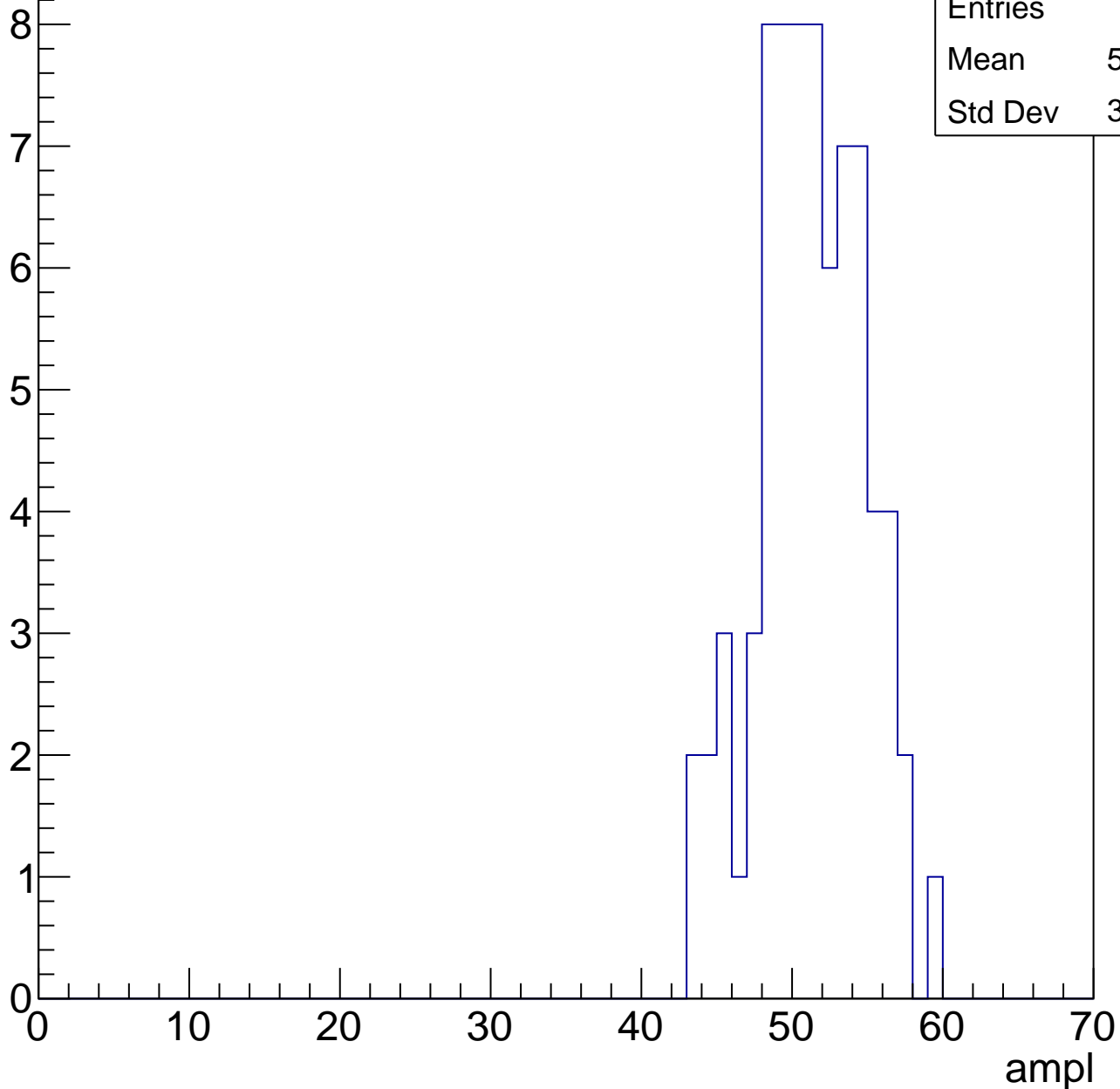


# B1L101S, U11-ch61, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	50.78
Std Dev	3.512

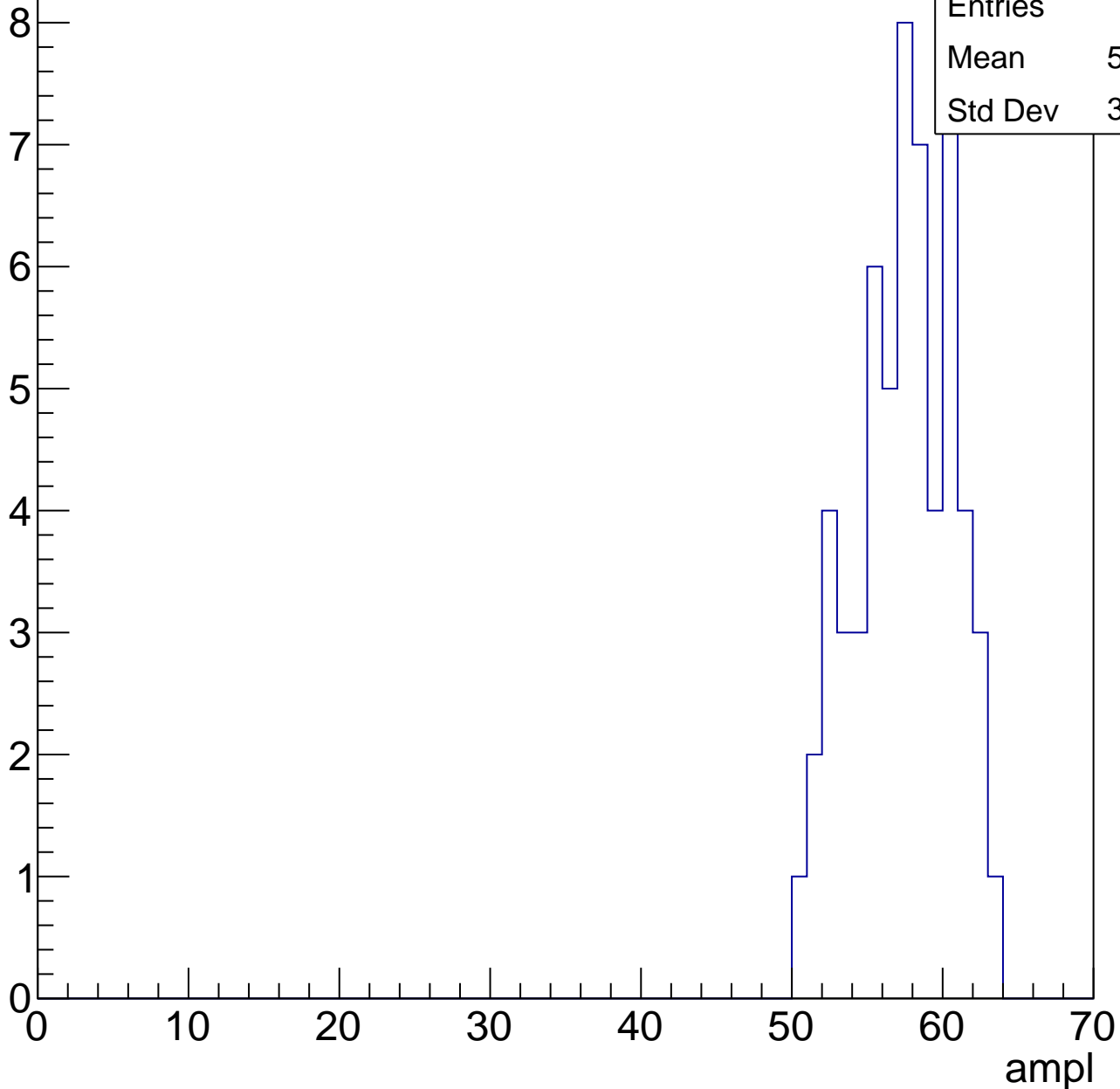


# B1L101S, U11-ch61, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	56.98
Std Dev	3.176

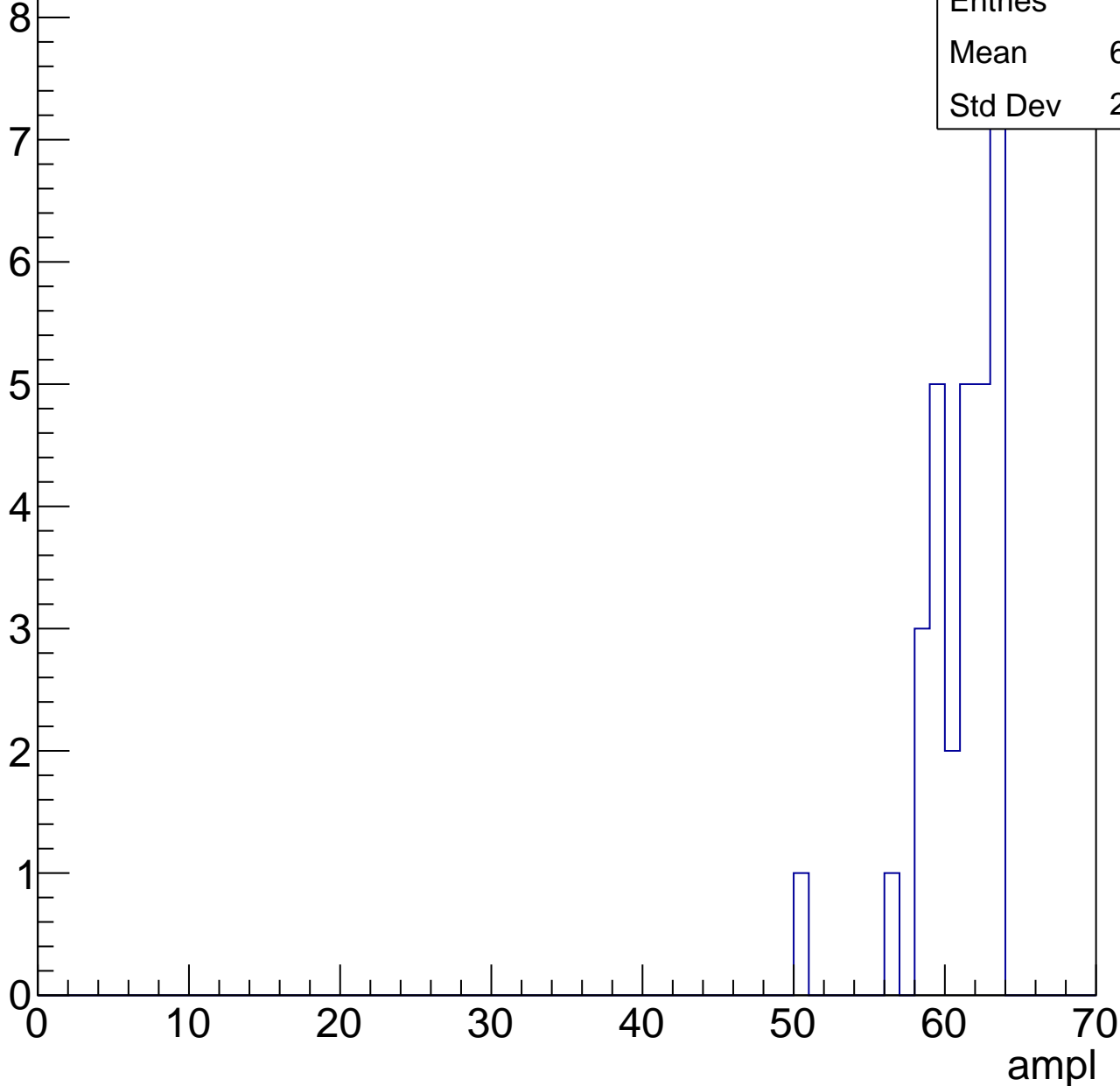


# B1L101S, U11-ch61, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	30
Mean	60.47
Std Dev	2.729



# B1L101S, U11-ch61, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

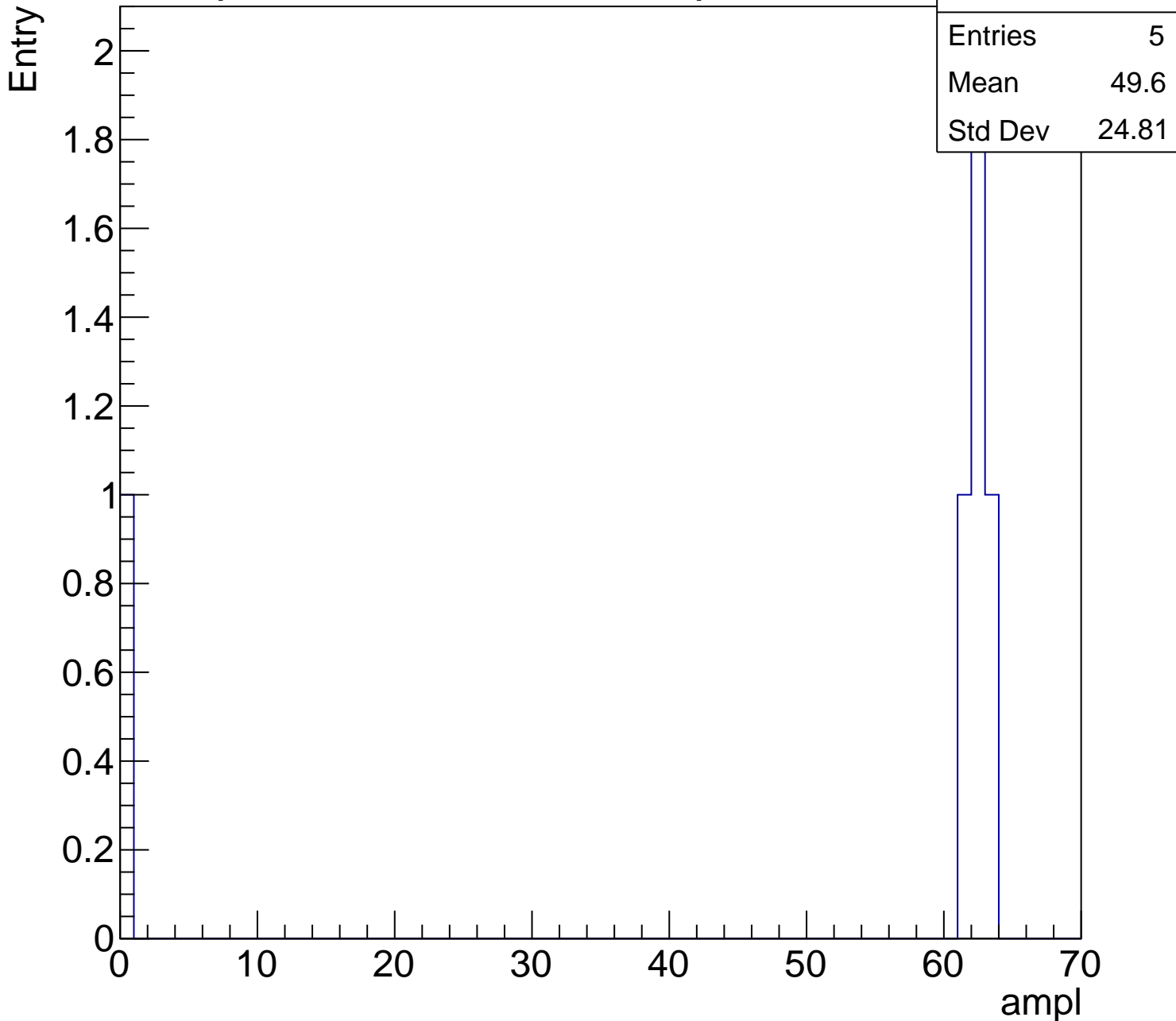
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	49.6
Std Dev	24.81

0 10 20 30 40 50 60 70

ampl

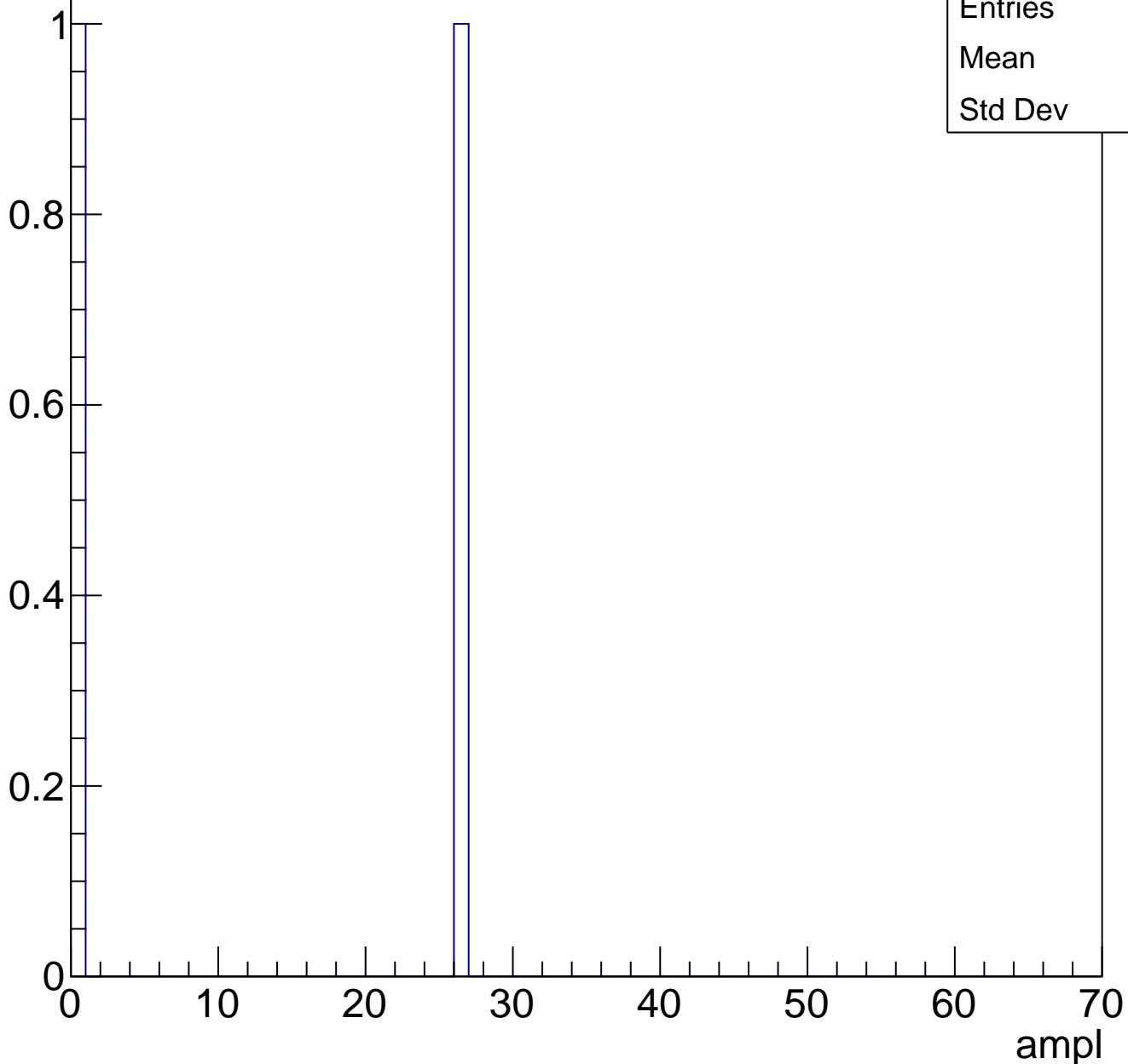




# B1L101S, U11-ch61, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	13
Std Dev	13

# B1L101S, U11-ch62, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	73
Mean	29.99
Std Dev	3.125

**Gaus mean : 29.9852**

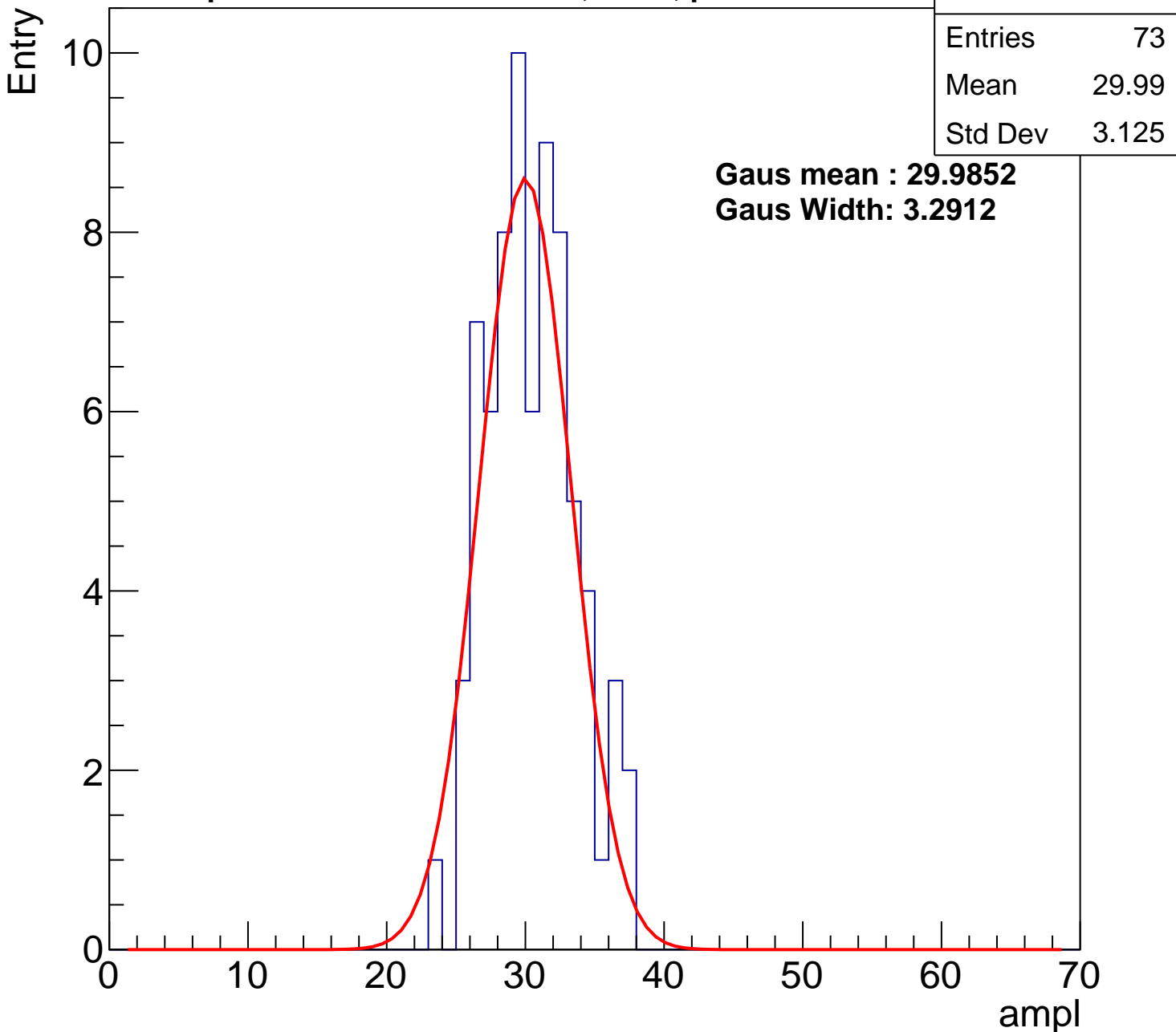
**Gaus Width: 3.2912**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L101S, U11-ch62, adc1

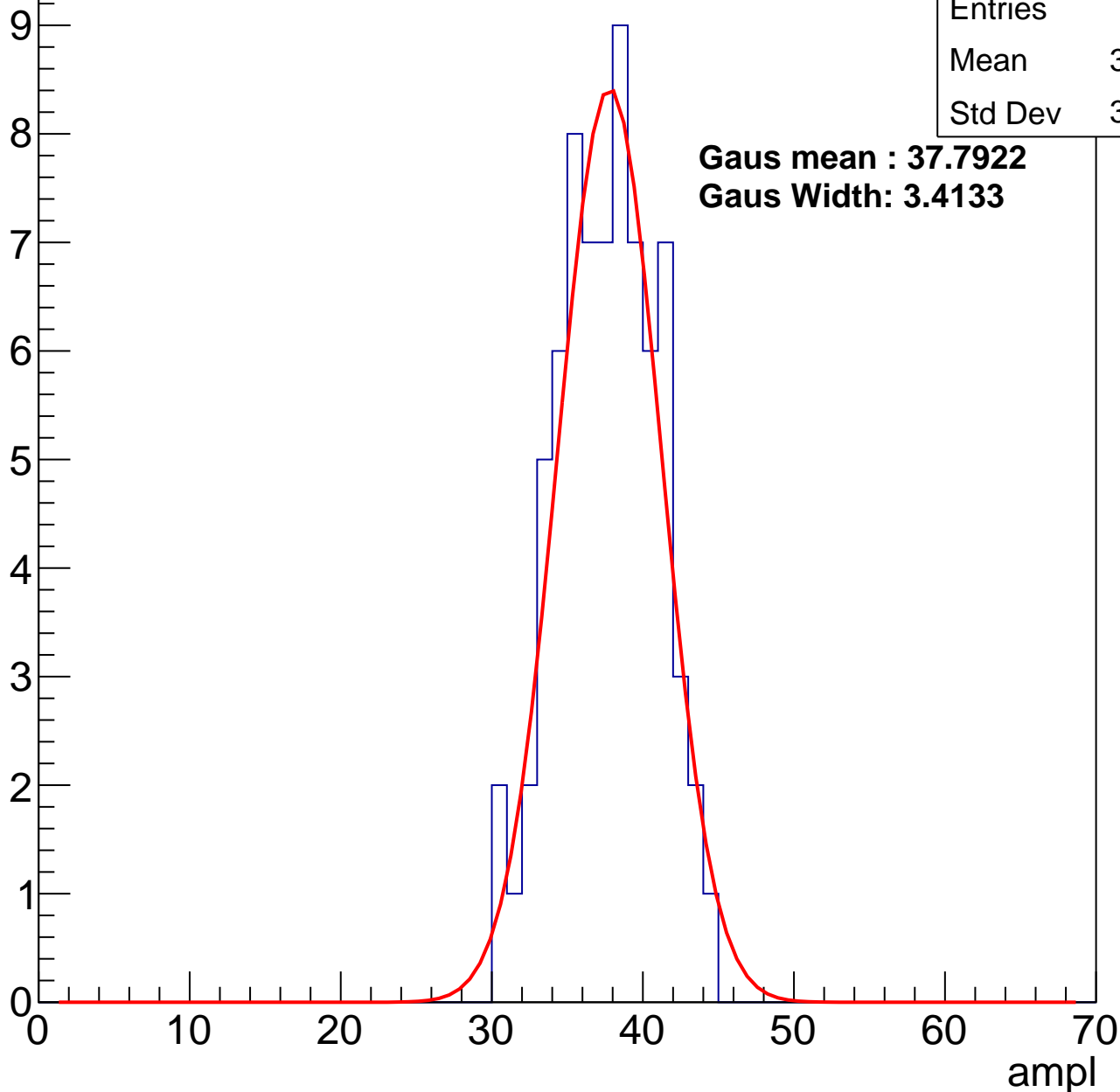
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	37.16
Std Dev	3.214

**Gaus mean : 37.7922**

**Gaus Width: 3.4133**



# B1L101S, U11-ch62, adc2

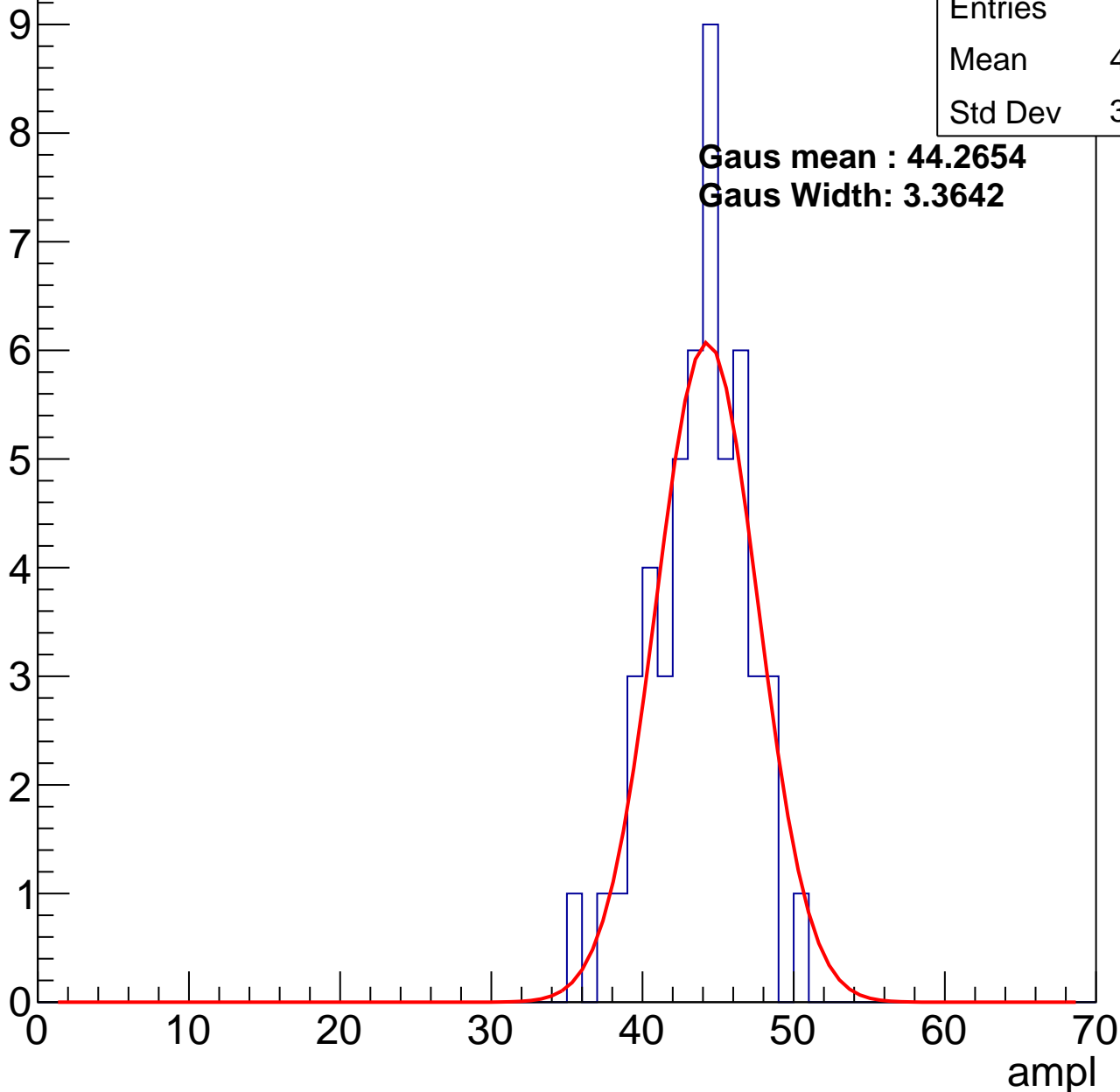
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	43.33
Std Dev	3.053

**Gaus mean : 44.2654**

**Gaus Width: 3.3642**

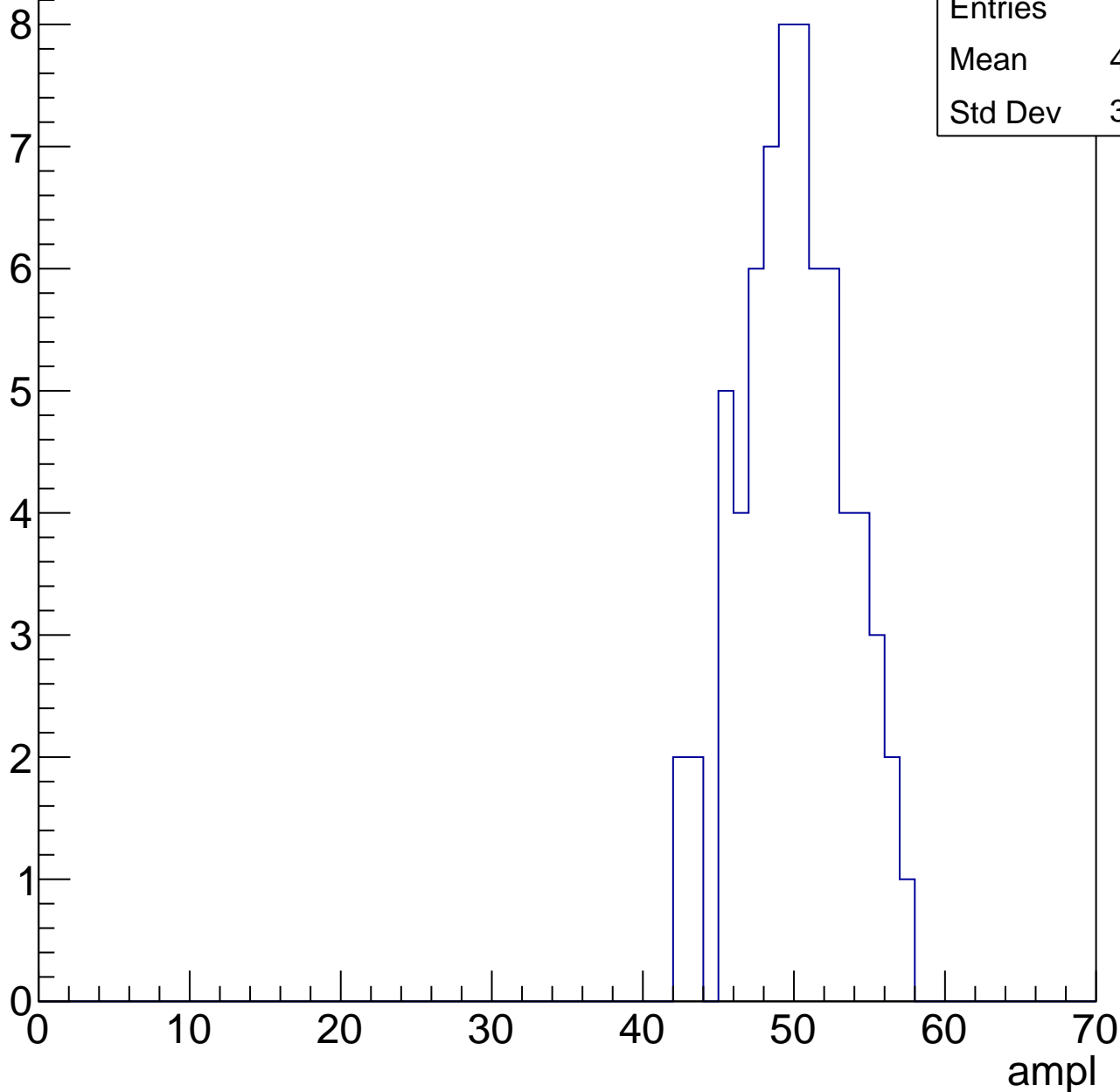


# B1L101S, U11-ch62, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	49.54
Std Dev	3.466

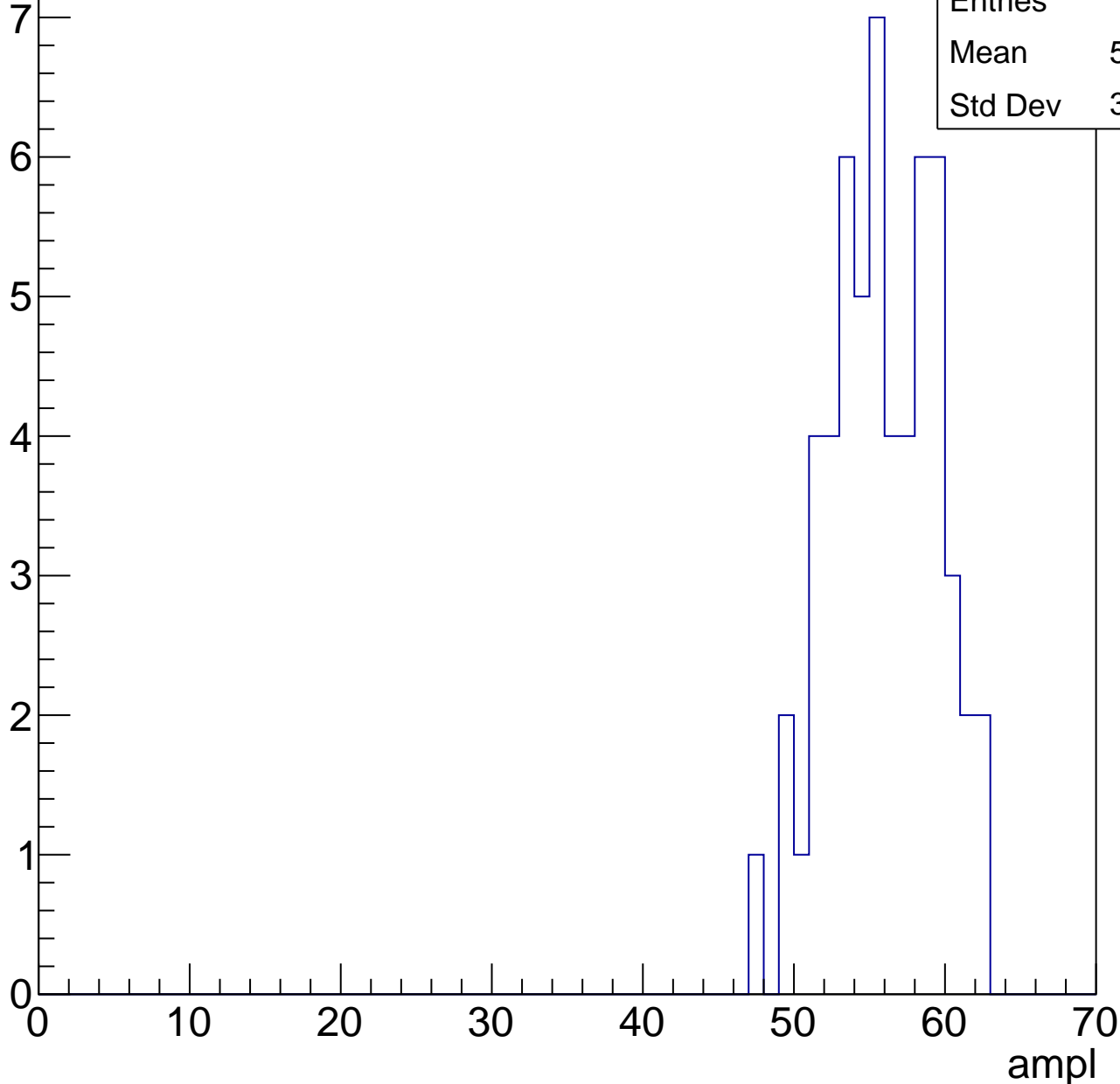


# B1L101S, U11-ch62, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	55.44
Std Dev	3.489

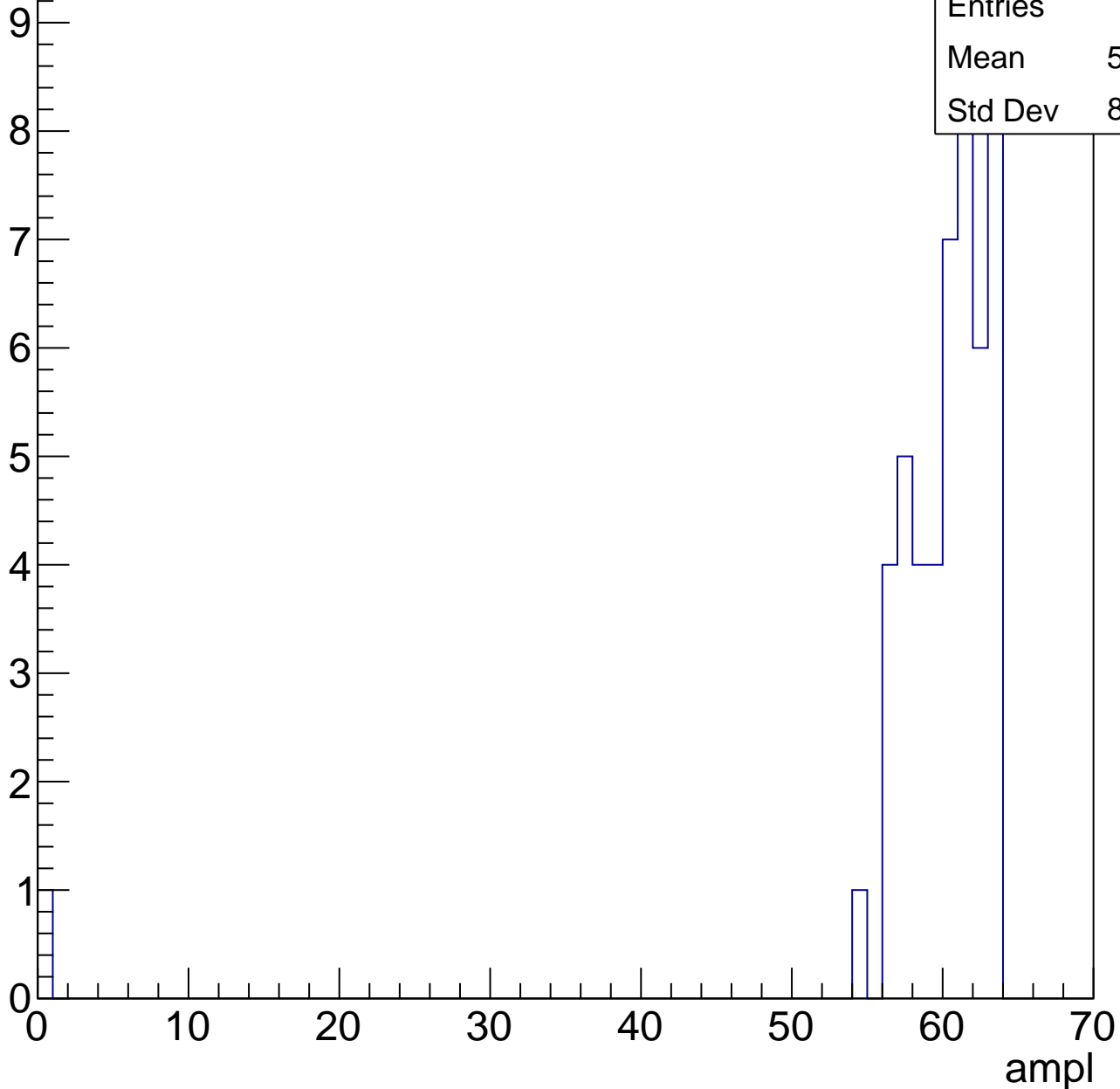


# B1L101S, U11-ch62, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	49
Mean	58.73
Std Dev	8.806



# B1L101S, U11-ch62, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.33
Std Dev	0.4714

ampl





# B1L101S, U11-ch62, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U11-ch63, adc0

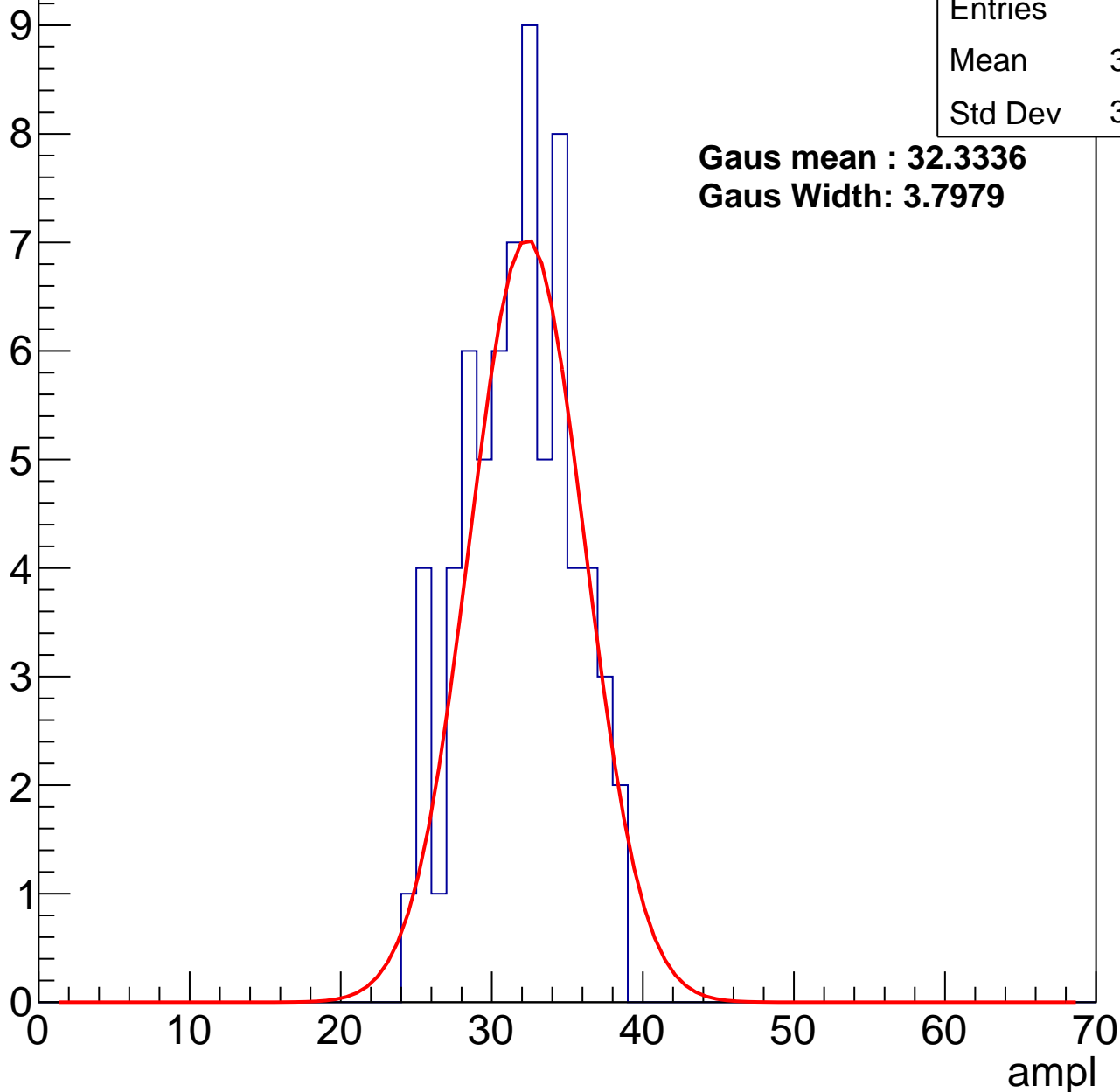
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	31.36
Std Dev	3.456

**Gaus mean : 32.3336**

**Gaus Width: 3.7979**



# B1L101S, U11-ch63, adc1

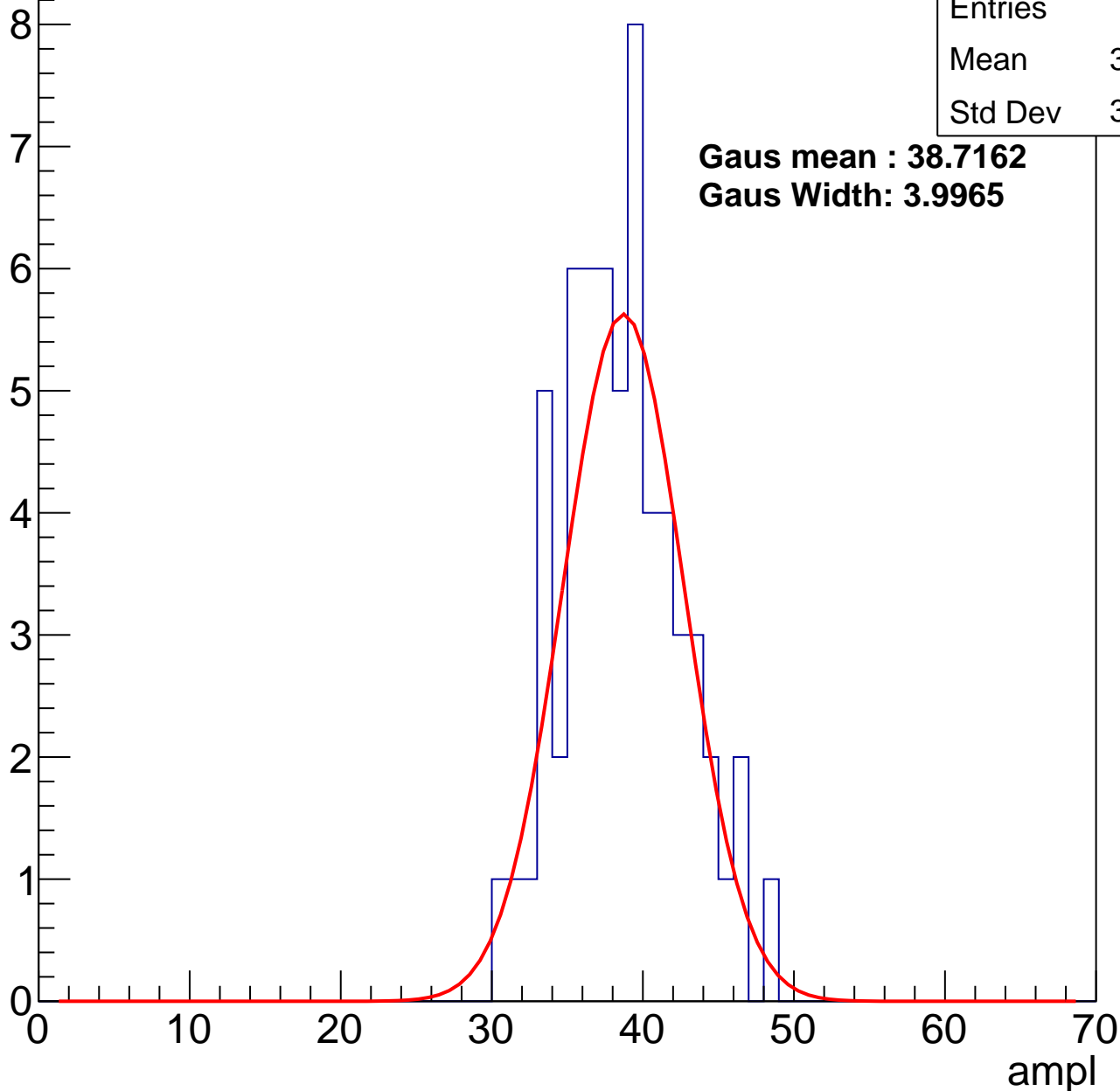
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	38.16
Std Dev	3.884

**Gaus mean : 38.7162**

**Gaus Width: 3.9965**



# B1L101S, U11-ch63, adc2

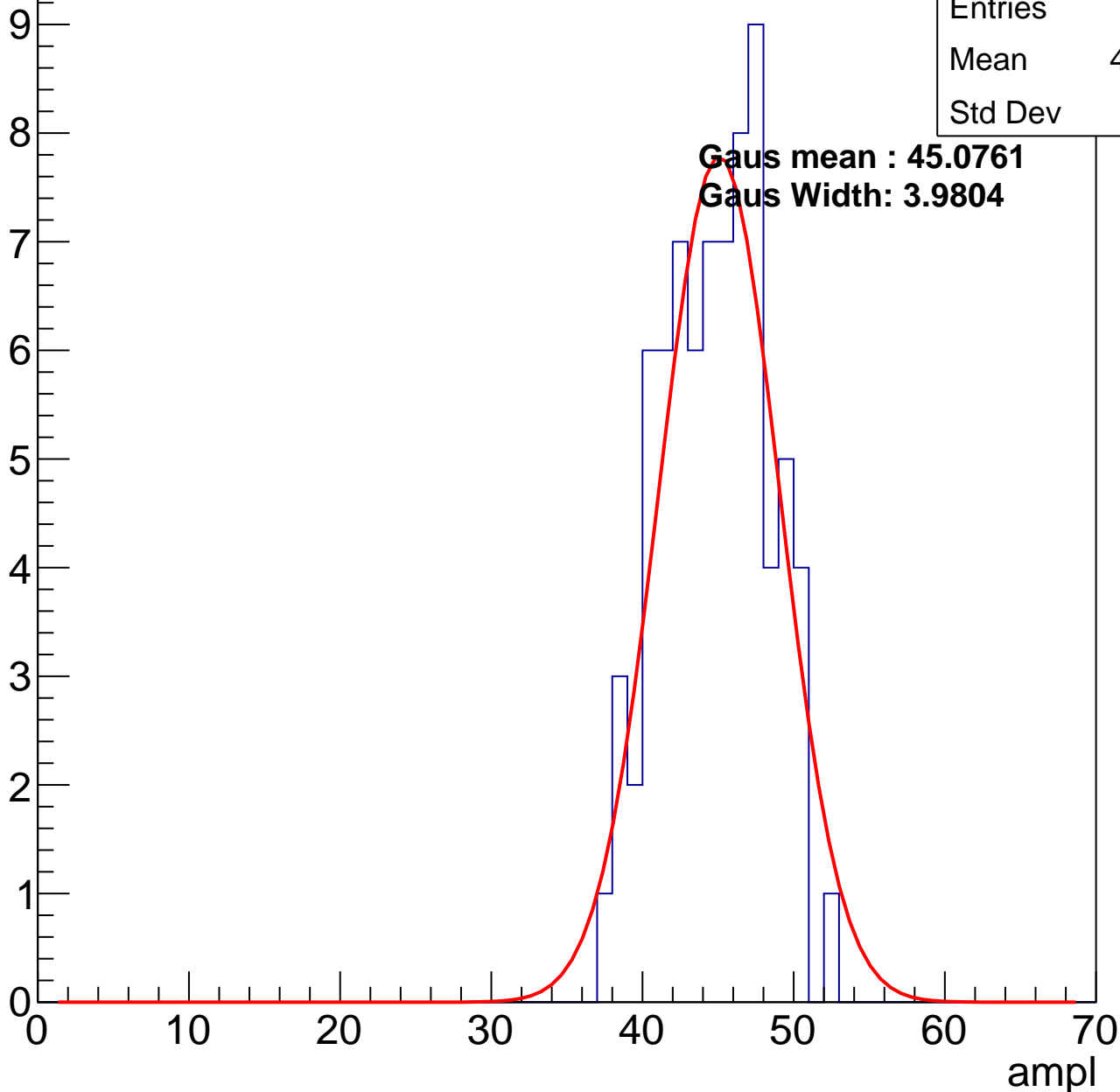
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	44.34
Std Dev	3.44

**Gaus mean : 45.0761**

**Gaus Width: 3.9804**

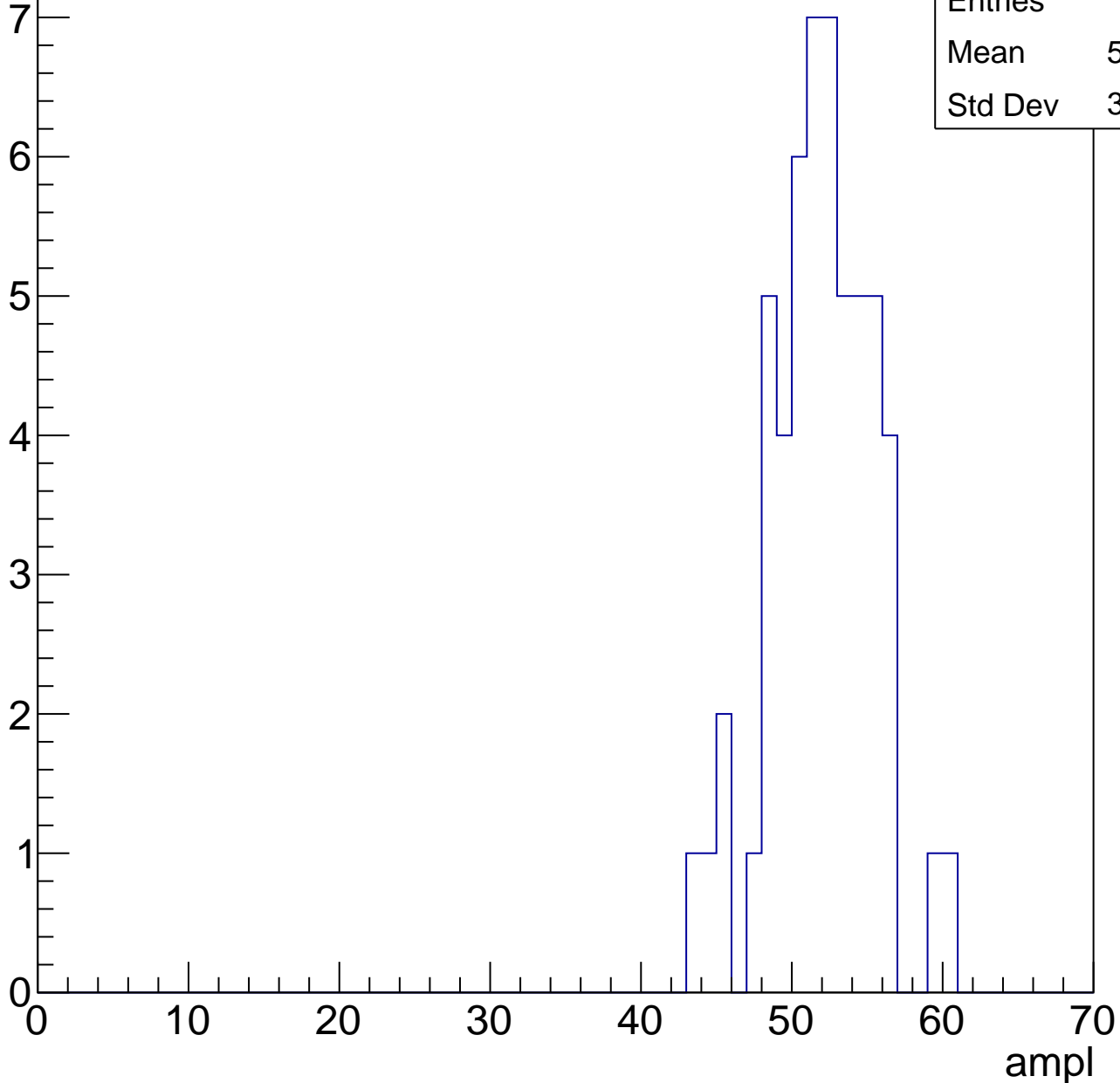


# B1L101S, U11-ch63, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	51.53
Std Dev	3.437

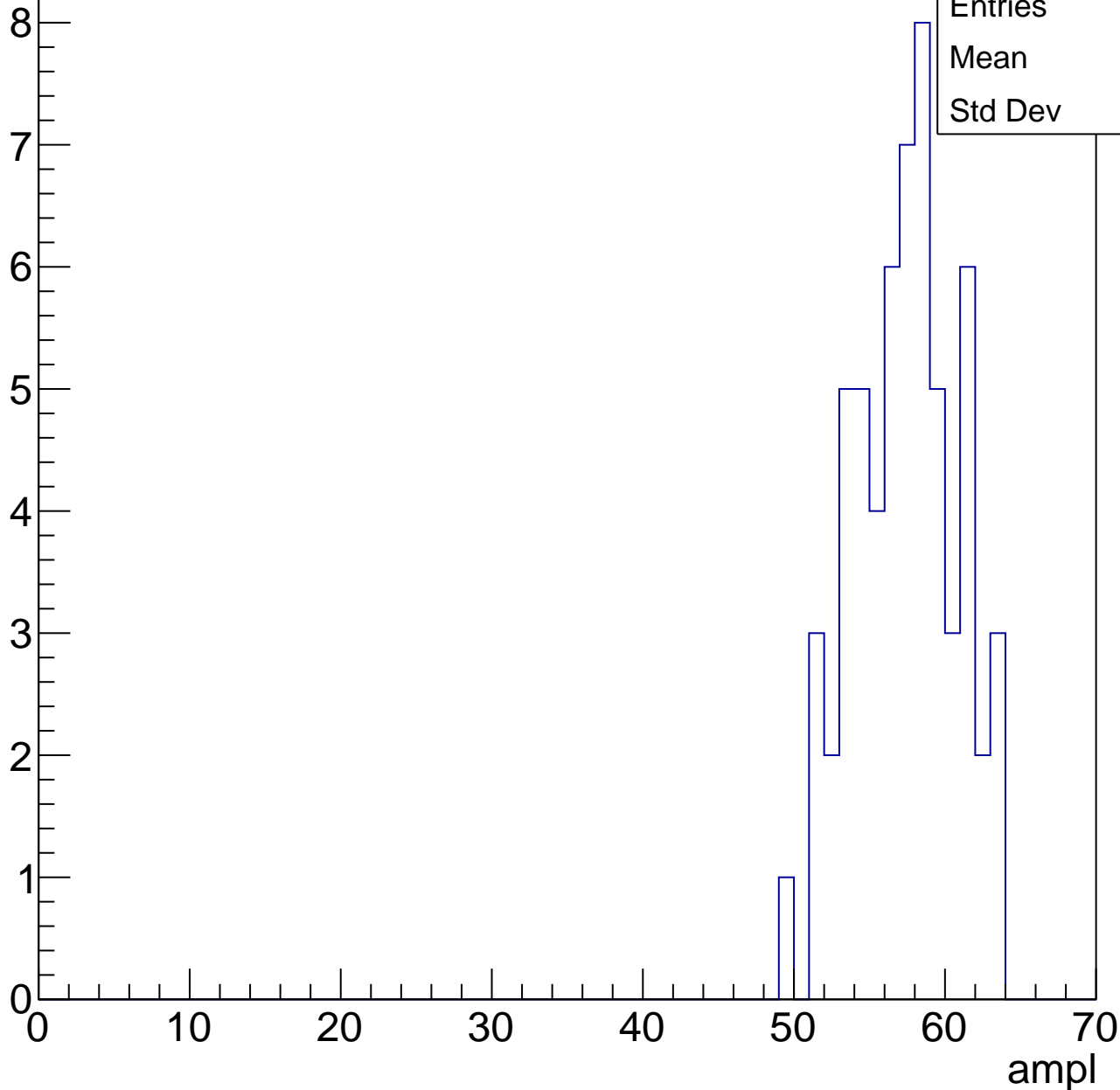


# B1L101S, U11-ch63, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	56.9
Std Dev	3.36

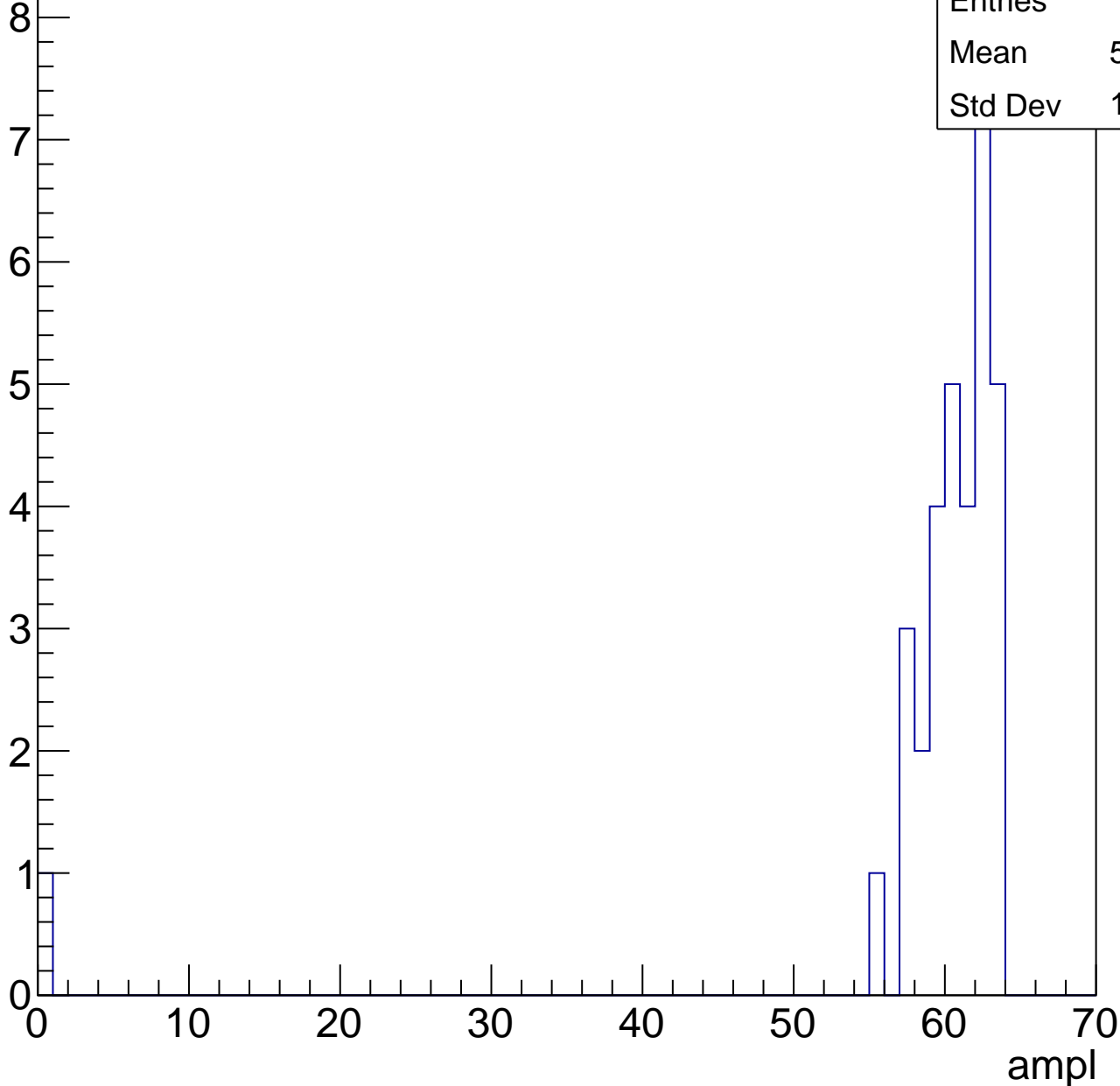


# B1L101S, U11-ch63, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	33
Mean	58.58
Std Dev	10.56



# B1L101S, U11-ch63, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch63, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	11
Std Dev	11

# B1L101S, U11-ch64, adc0

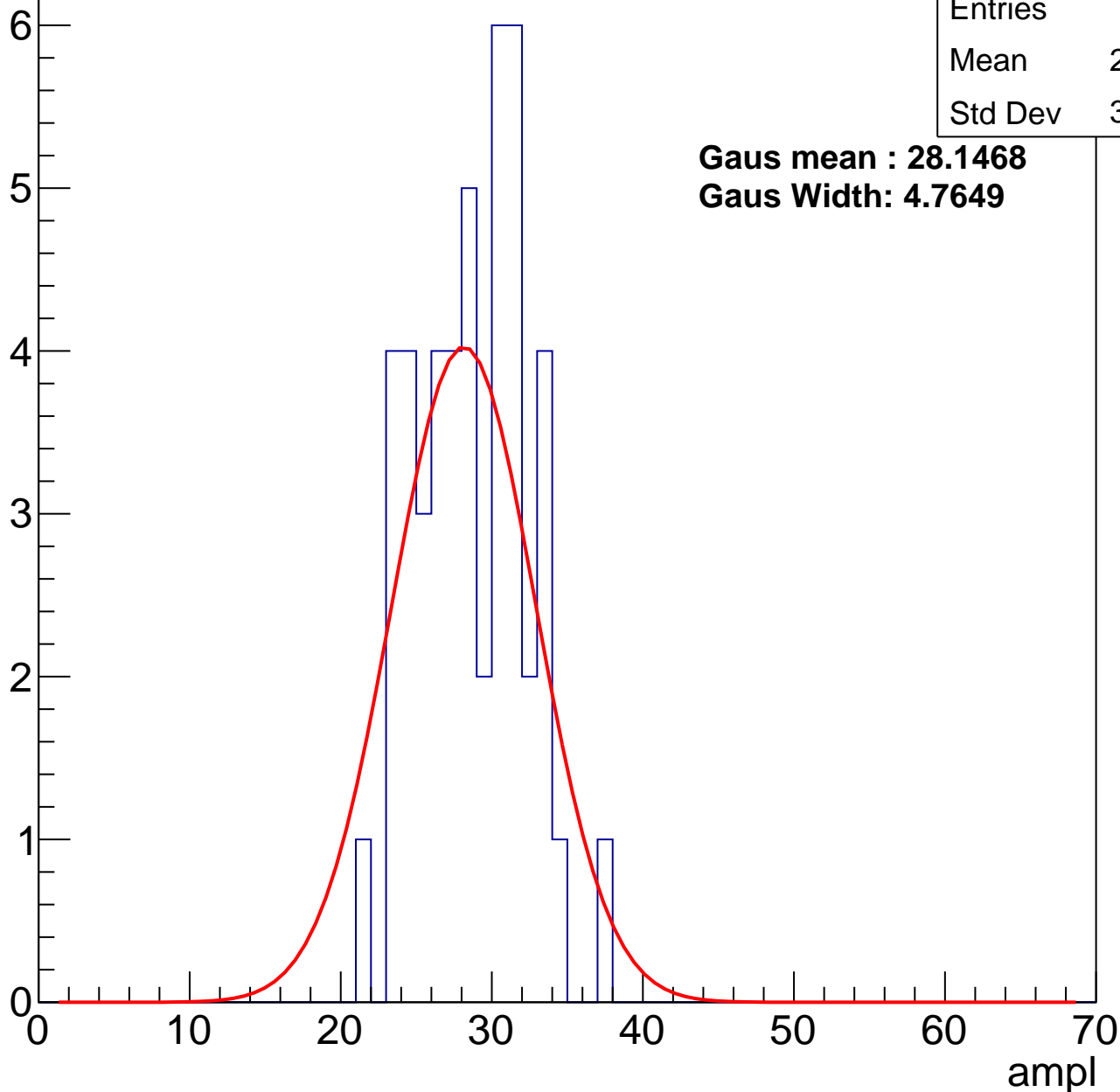
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	47
Mean	28.23
Std Dev	3.532

**Gaus mean : 28.1468**

**Gaus Width: 4.7649**



# B1L101S, U11-ch64, adc1

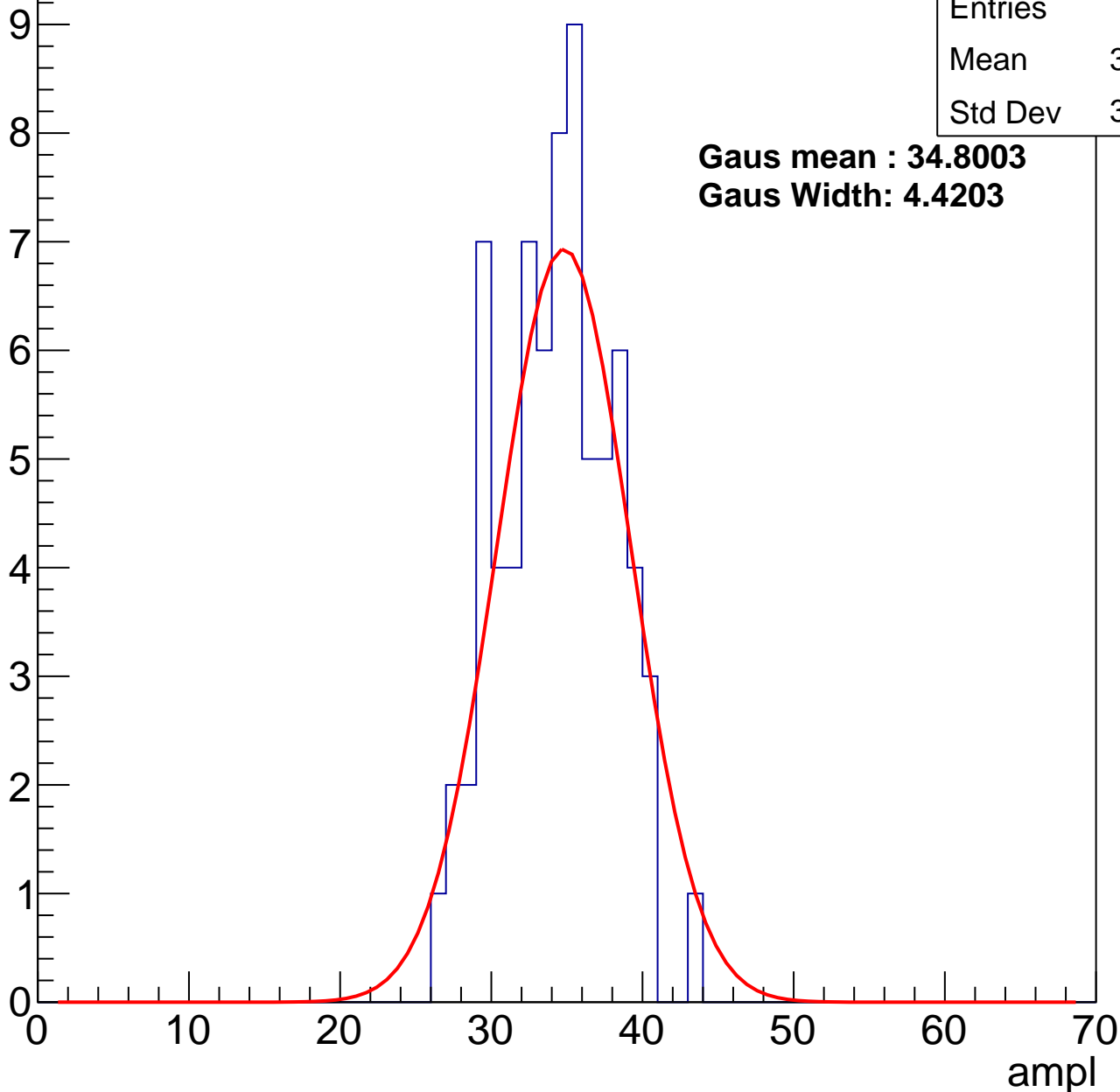
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	33.84
Std Dev	3.676

**Gaus mean : 34.8003**

**Gaus Width: 4.4203**



# B1L101S, U11-ch64, adc2

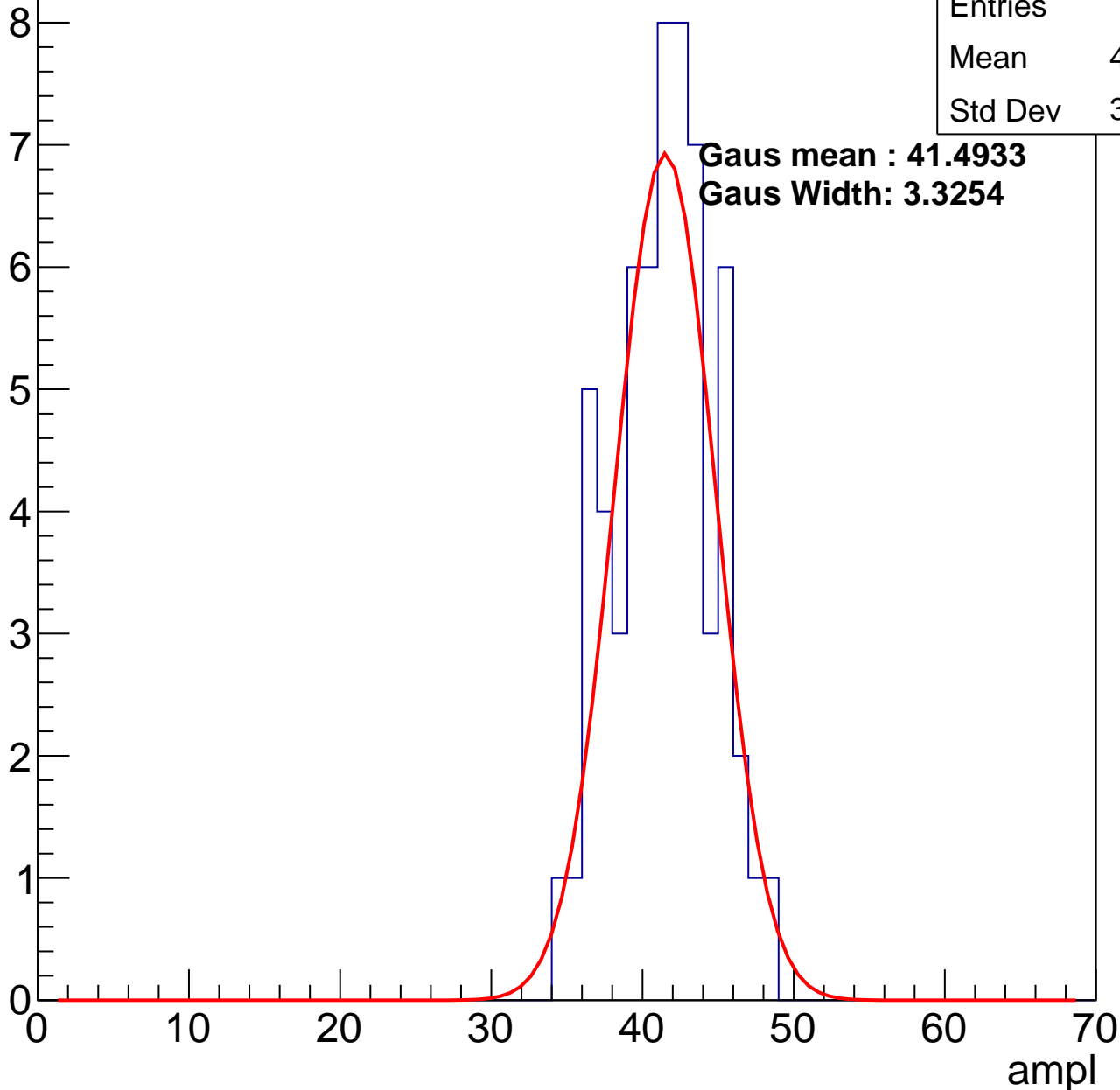
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	40.95
Std Dev	3.175

**Gaus mean : 41.4933**

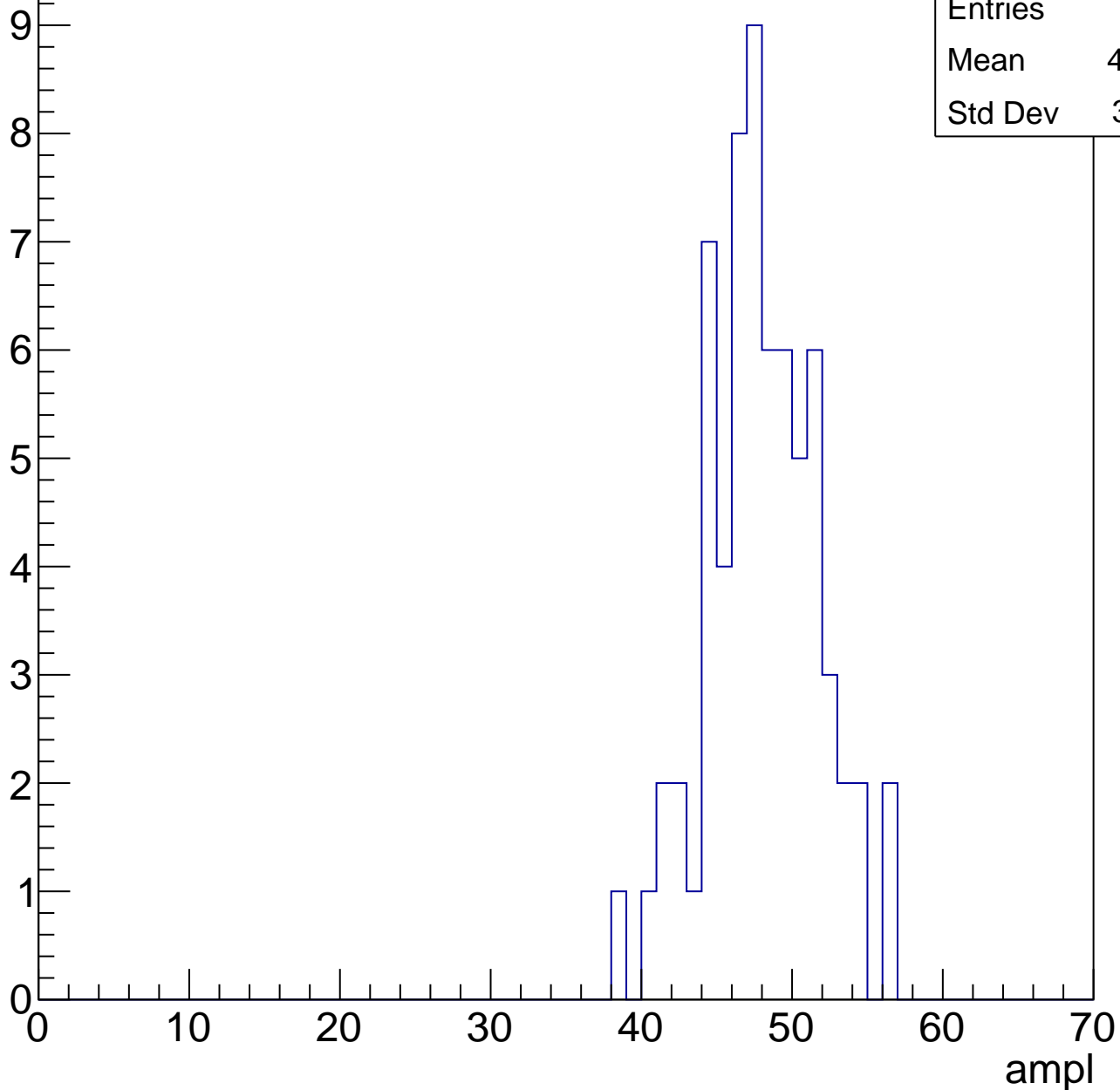
**Gaus Width: 3.3254**



# B1L101S, U11-ch64, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



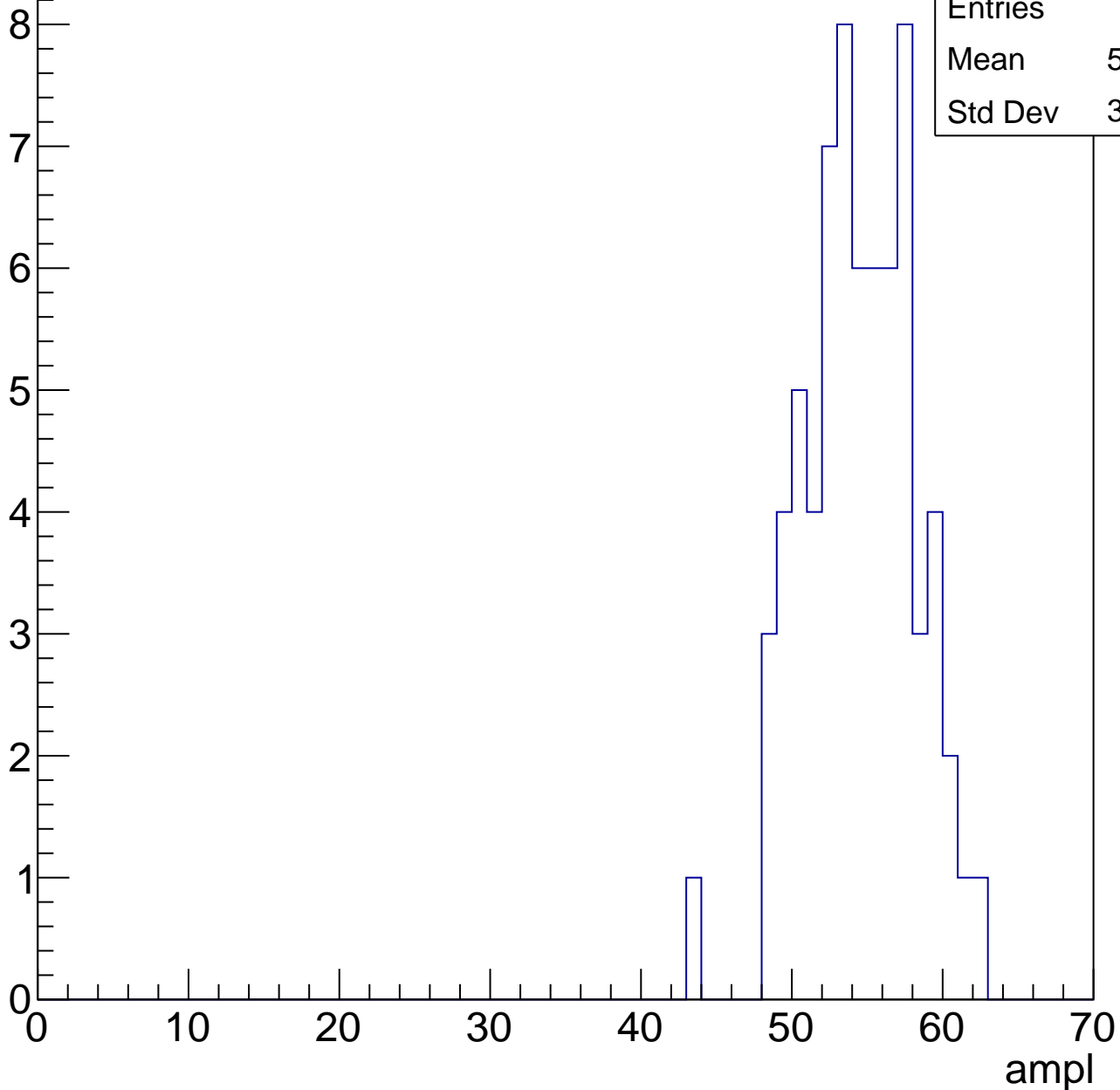
Entries	67
Mean	47.55
Std Dev	3.691

# B1L101S, U11-ch64, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	53.97
Std Dev	3.643

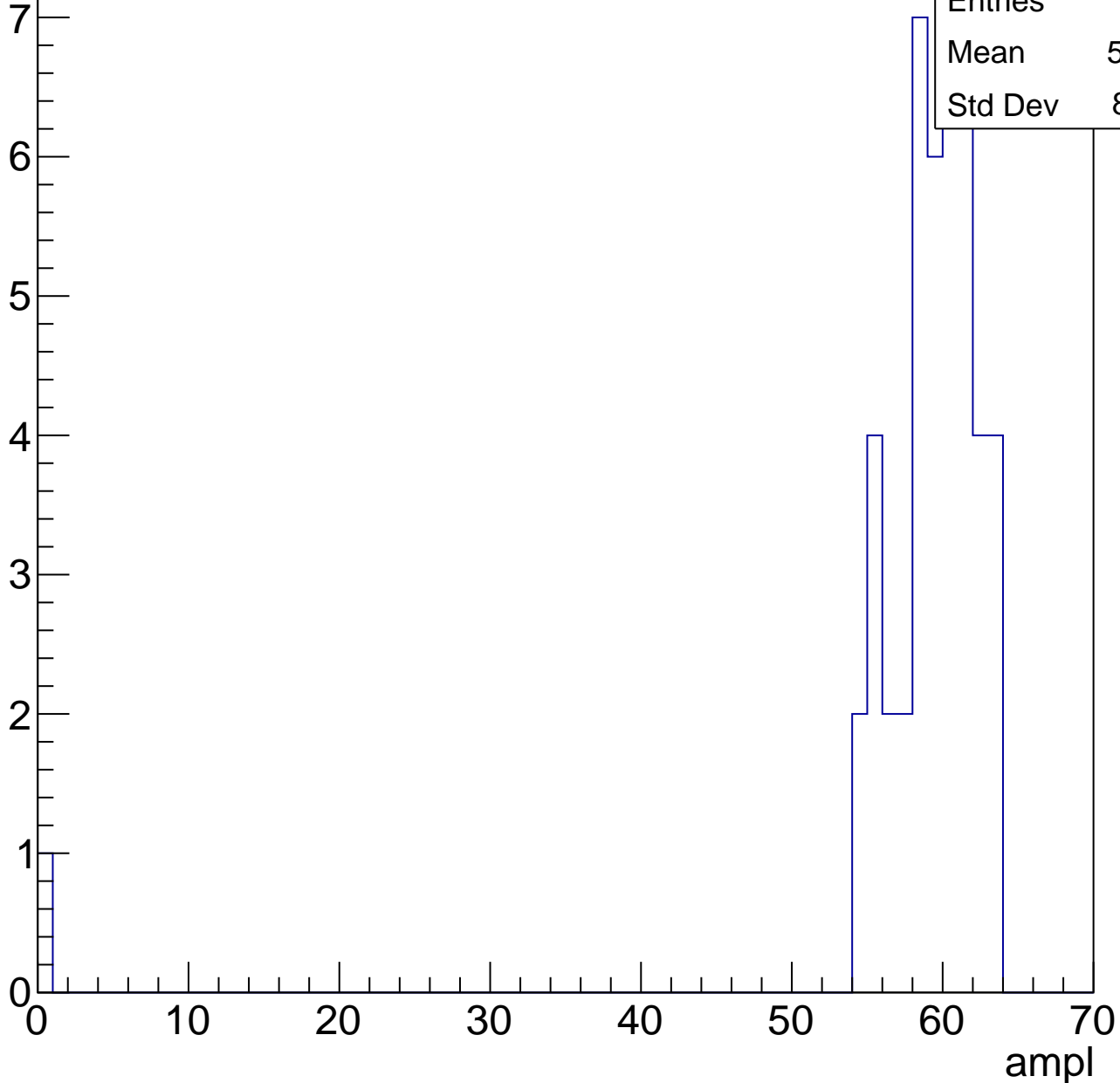


# B1L101S, U11-ch64, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

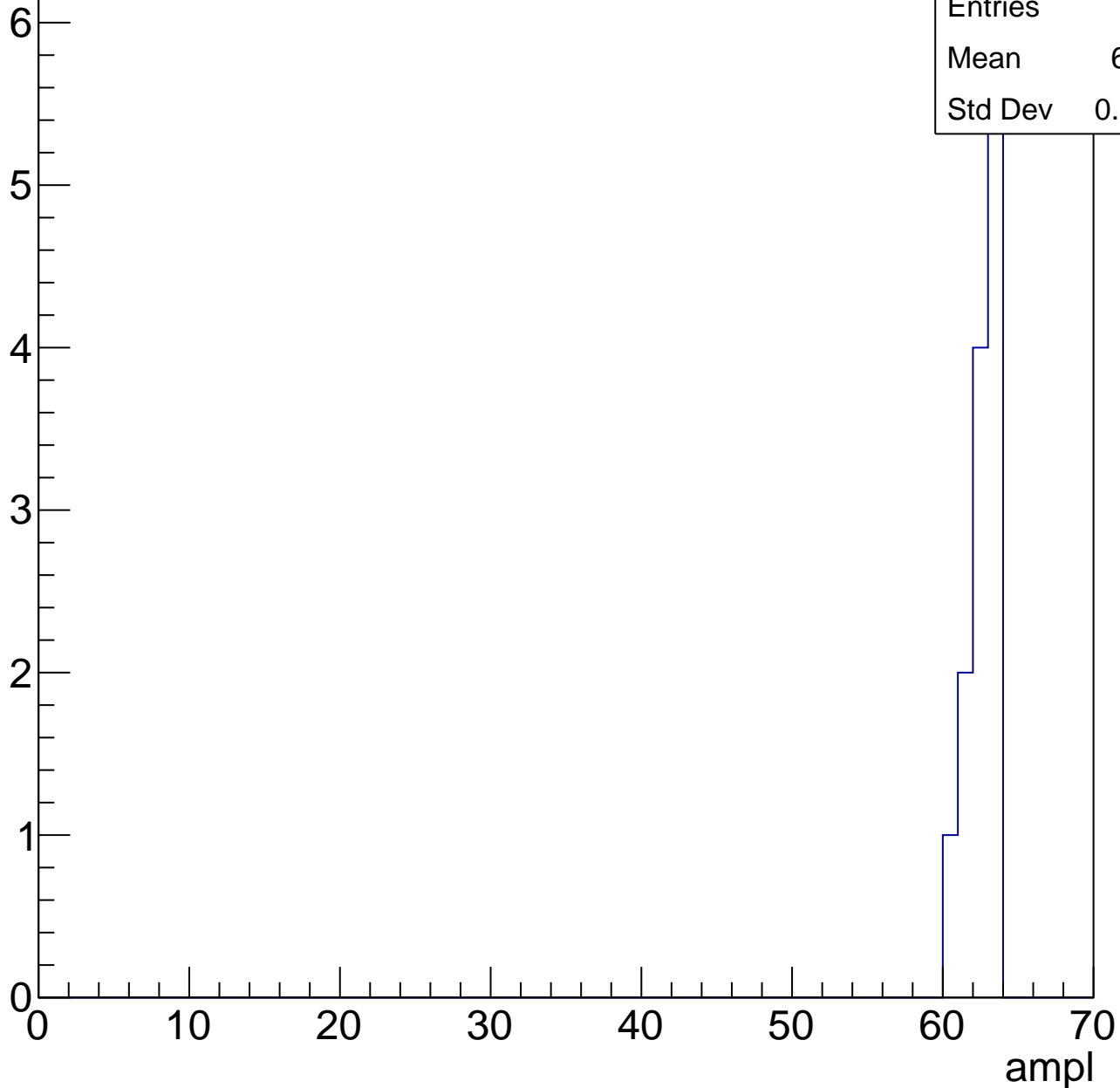
Entries	46
Mean	57.85
Std Dev	8.971



# B1L101S, U11-ch64, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch64, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U11-ch65, adc0

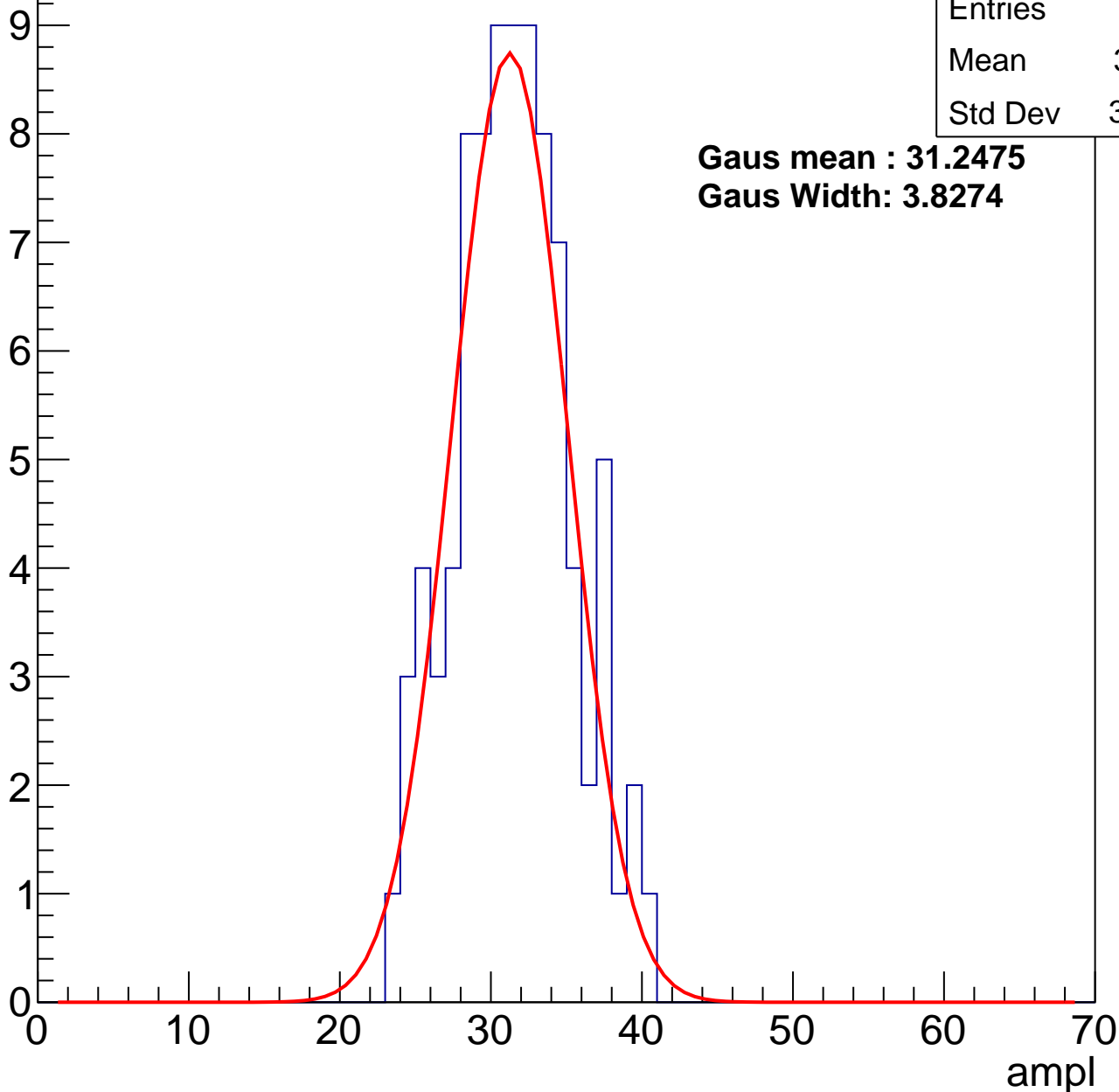
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	88
Mean	31.01
Std Dev	3.788

**Gaus mean : 31.2475**

**Gaus Width: 3.8274**



# B1L101S, U11-ch65, adc1

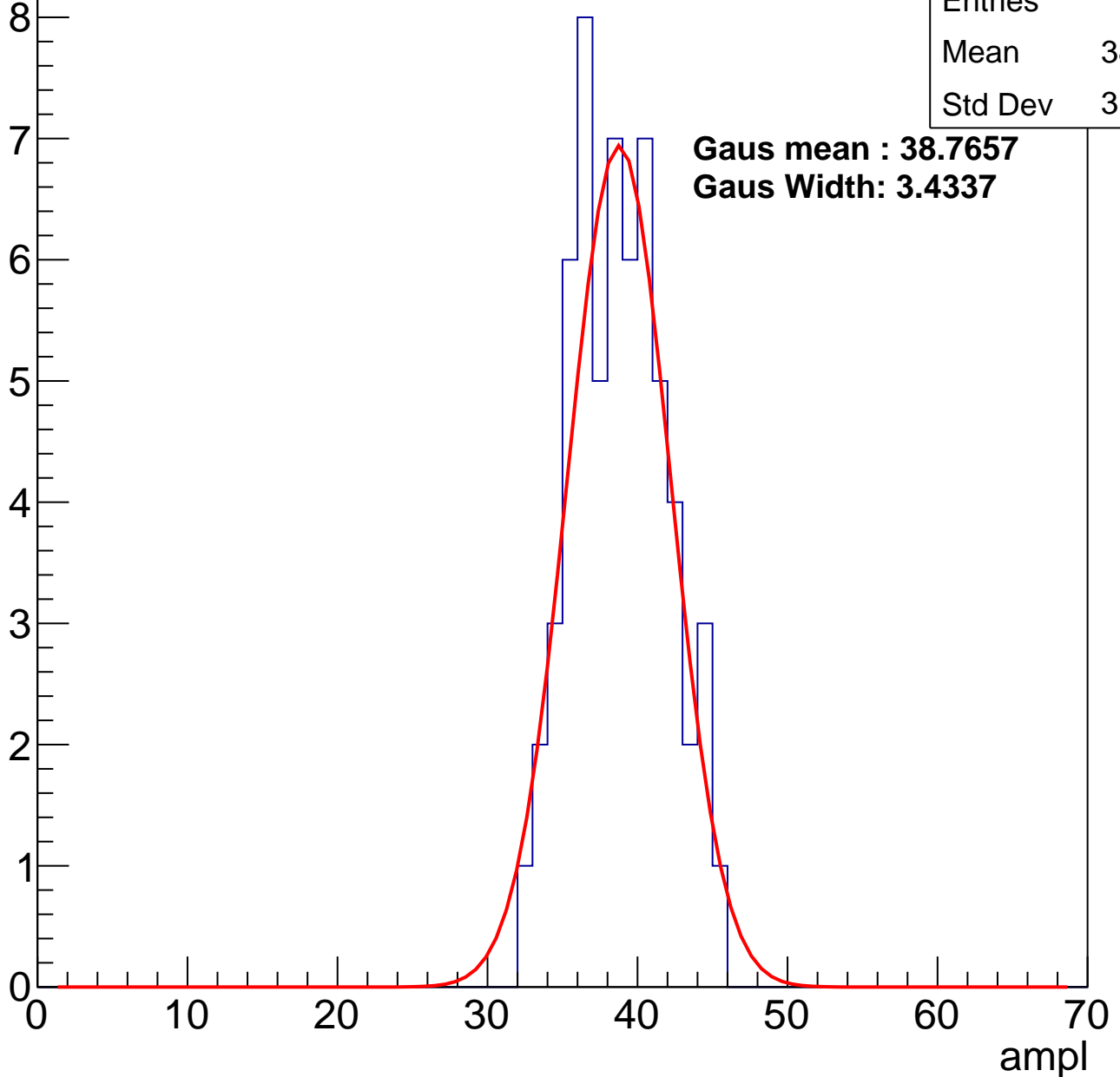
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	38.32
Std Dev	3.079

**Gaus mean : 38.7657**

**Gaus Width: 3.4337**



# B1L101S, U11-ch65, adc2

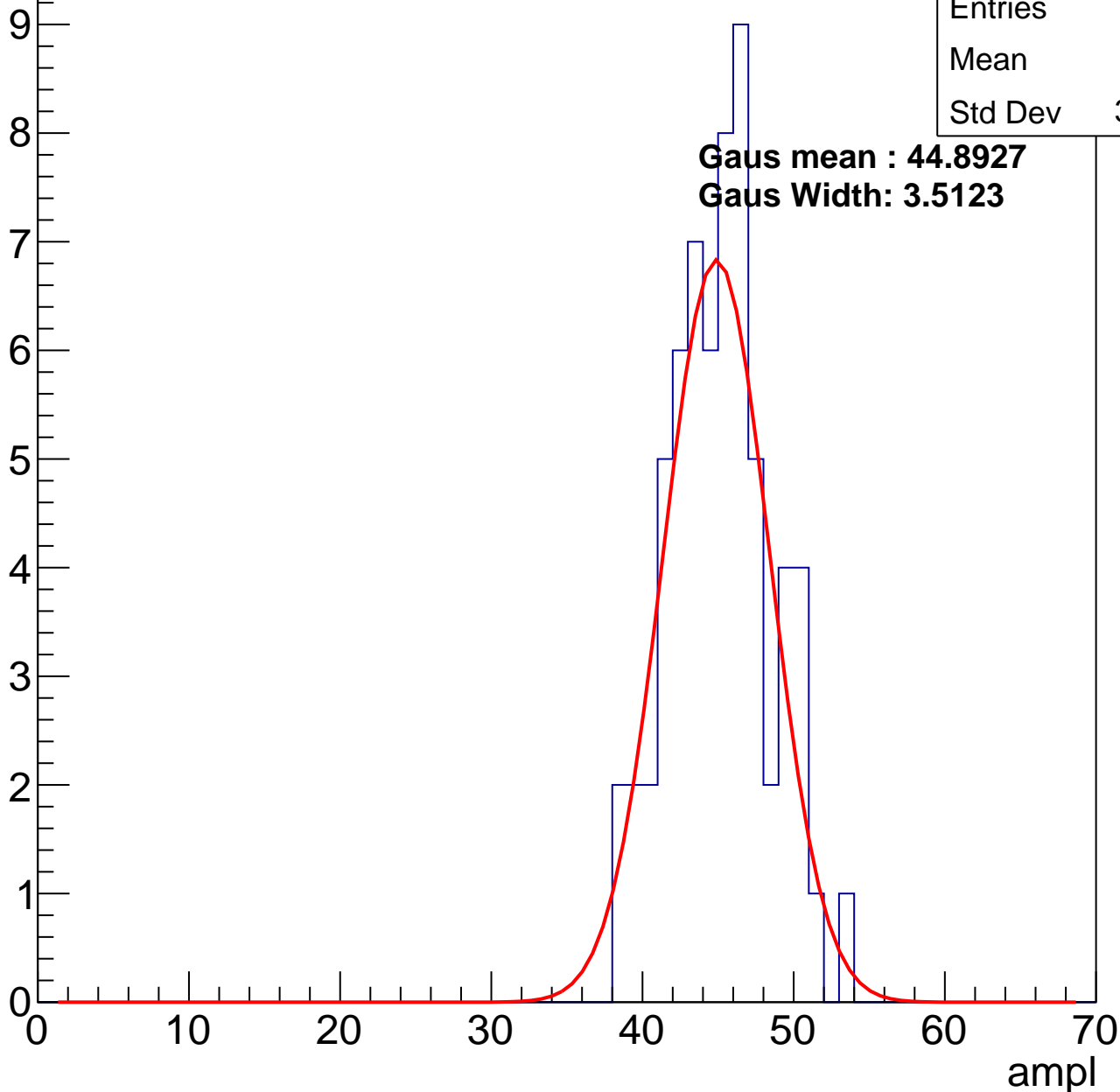
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	44.7
Std Dev	3.291

**Gaus mean : 44.8927**

**Gaus Width: 3.5123**

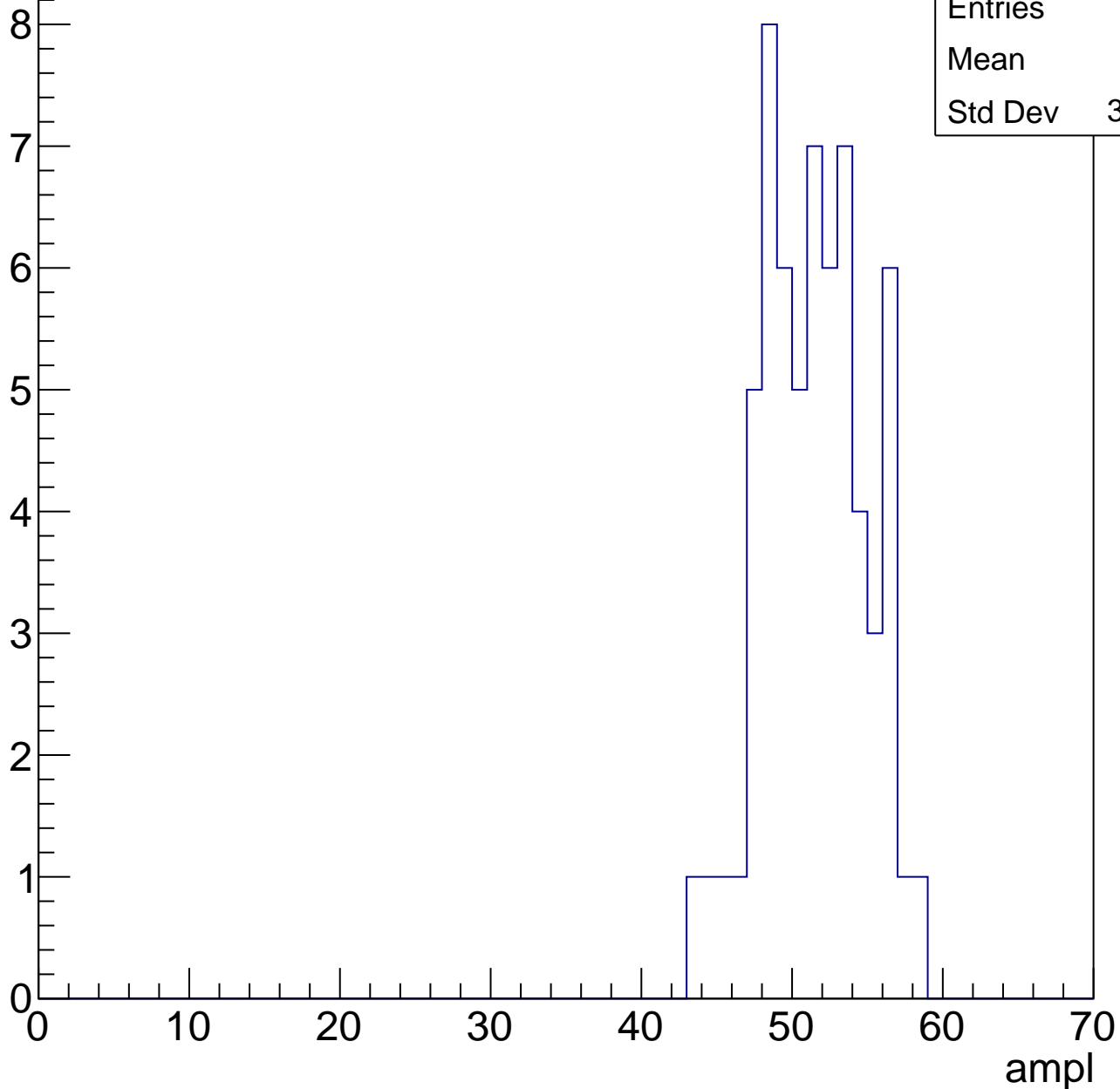


# B1L101S, U11-ch65, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	51
Std Dev	3.352

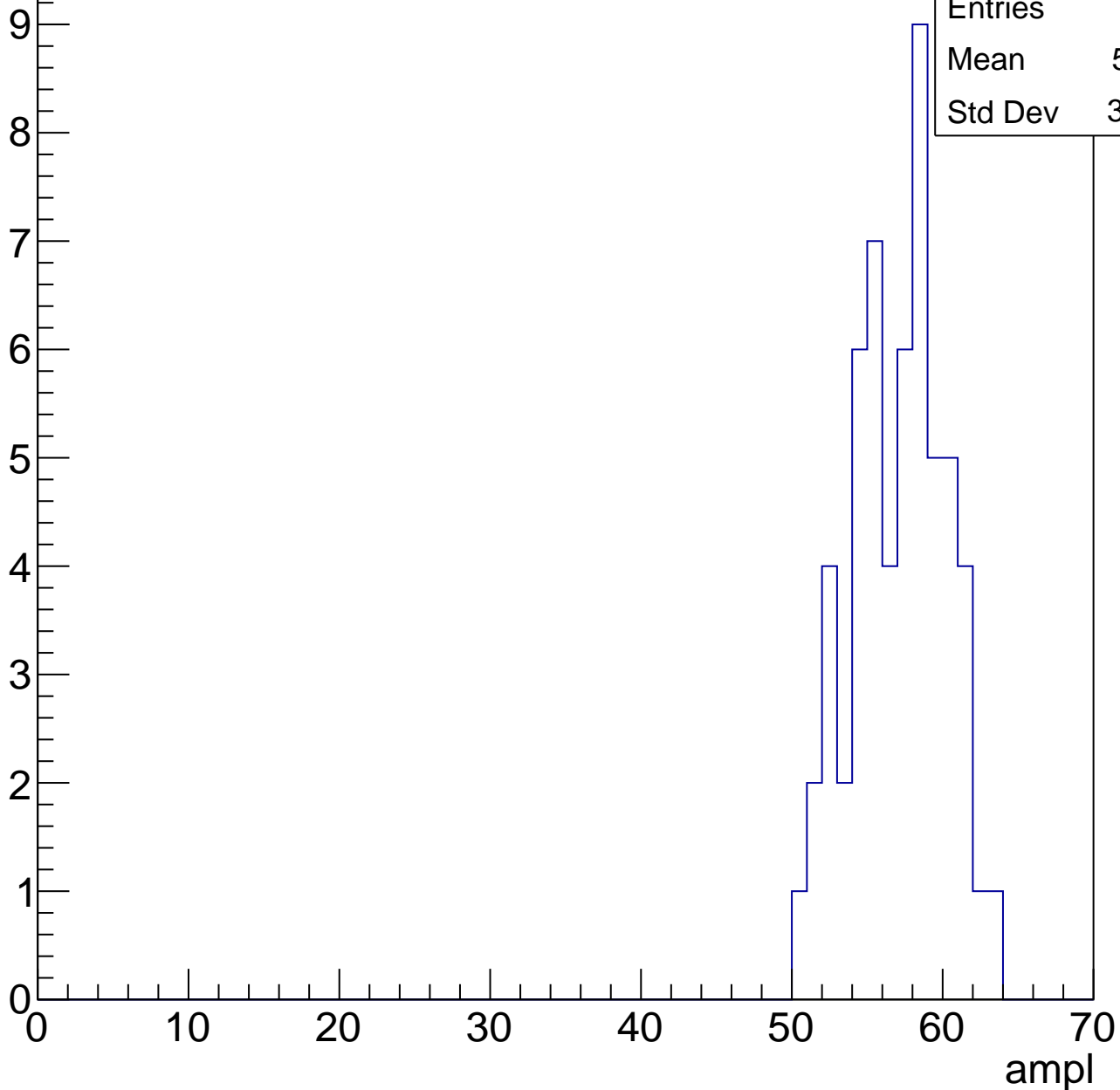


# B1L101S, U11-ch65, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	56.61
Std Dev	3.048

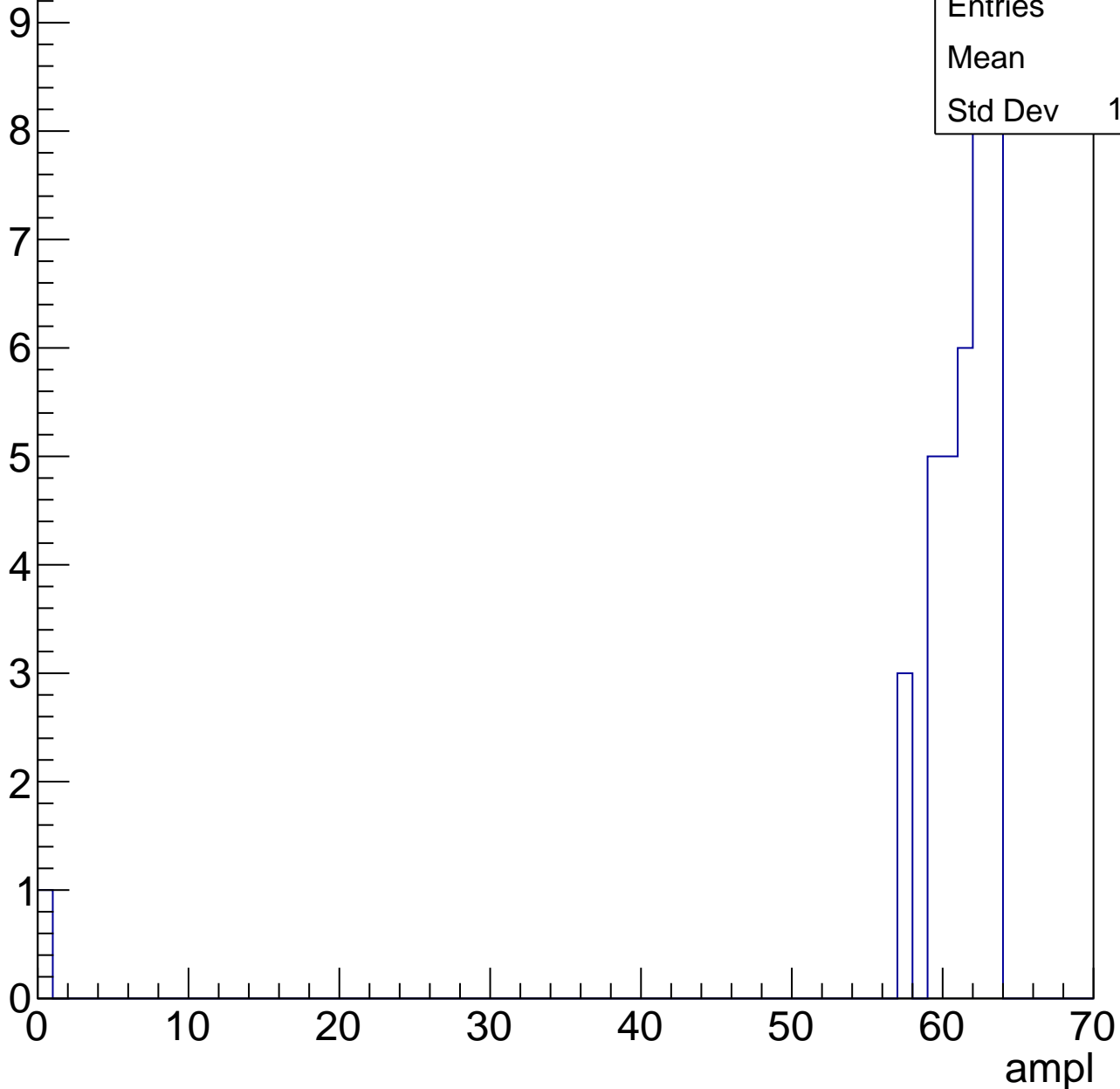


# B1L101S, U11-ch65, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	37
Mean	59.3
Std Dev	10.04



# B1L101S, U11-ch65, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch65, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U11-ch66, adc0

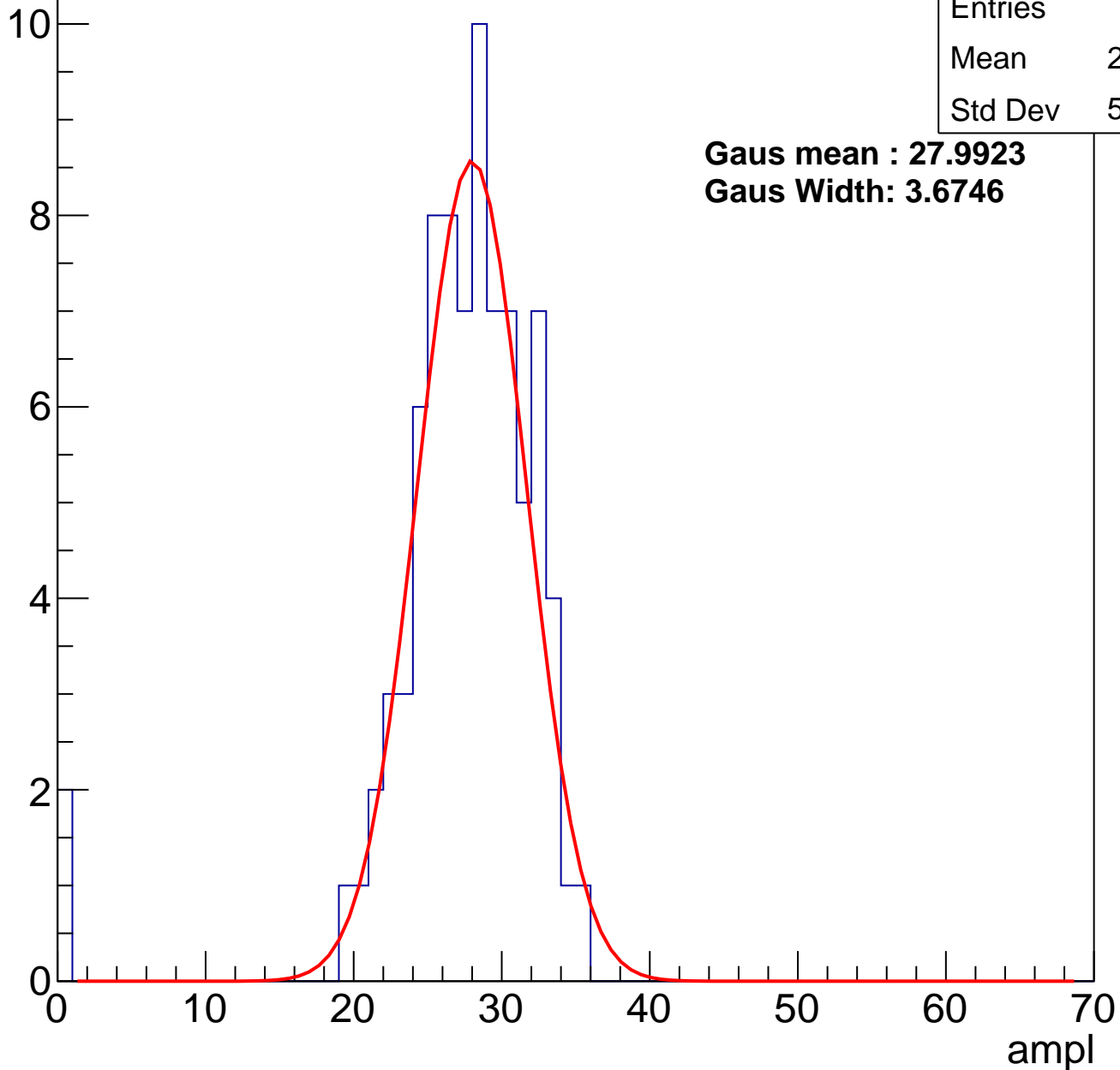
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	83
Mean	26.87
Std Dev	5.457

**Gaus mean : 27.9923**

**Gaus Width: 3.6746**

Entry



# B1L101S, U11-ch66, adc1

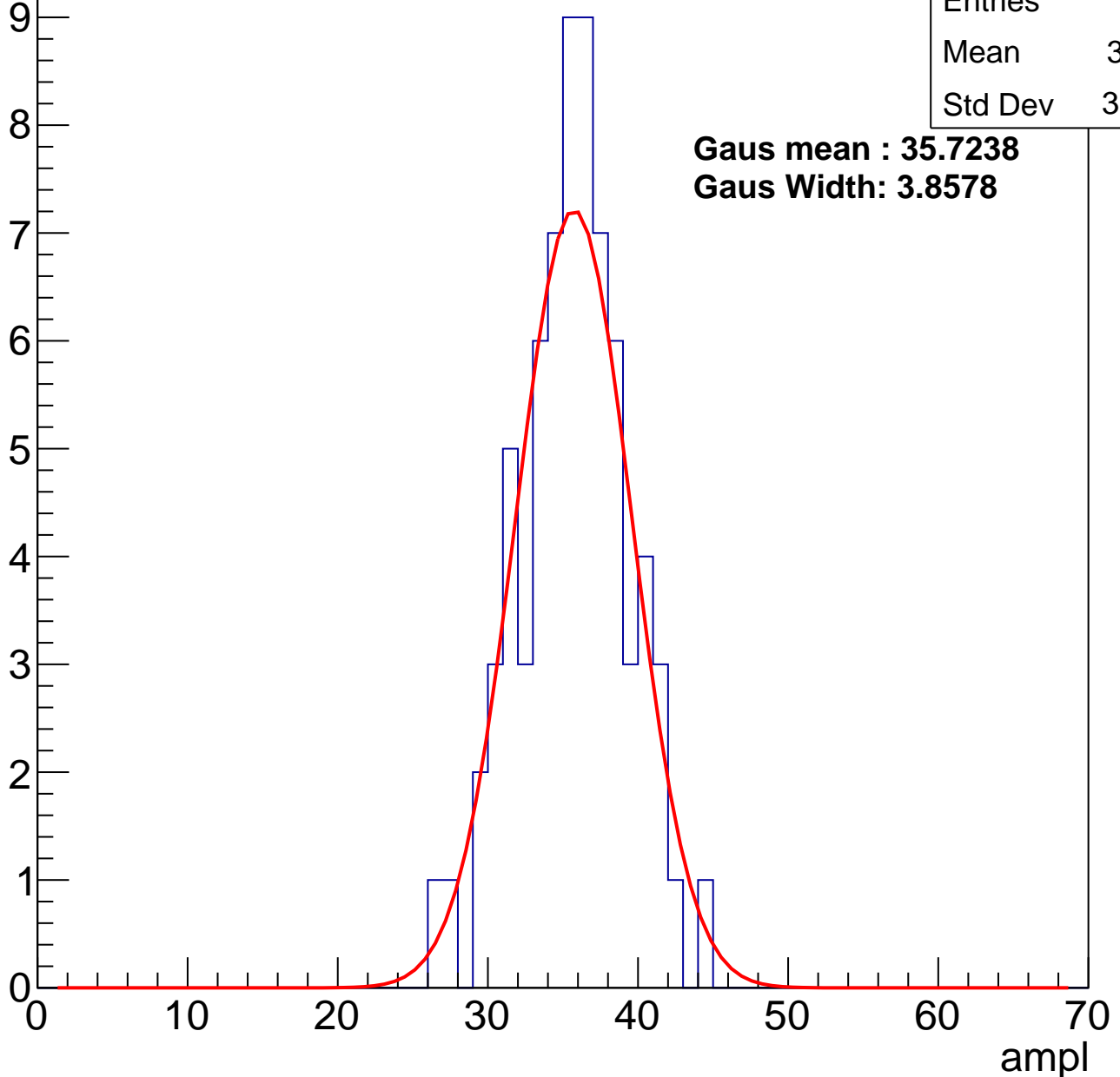
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	35.21
Std Dev	3.568

**Gaus mean : 35.7238**

**Gaus Width: 3.8578**



# B1L101S, U11-ch66, adc2

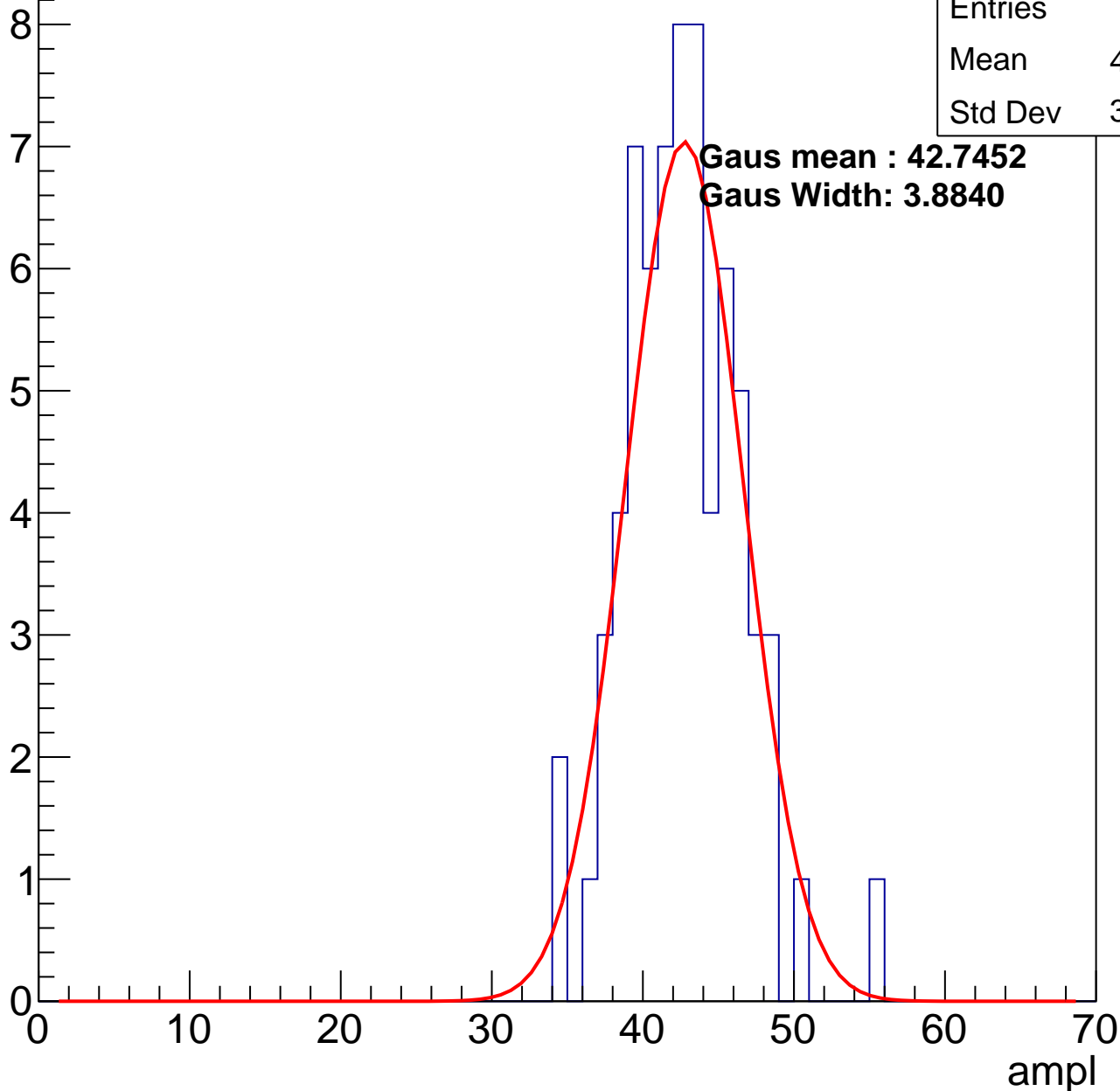
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	42.22
Std Dev	3.745

**Gaus mean : 42.7452**

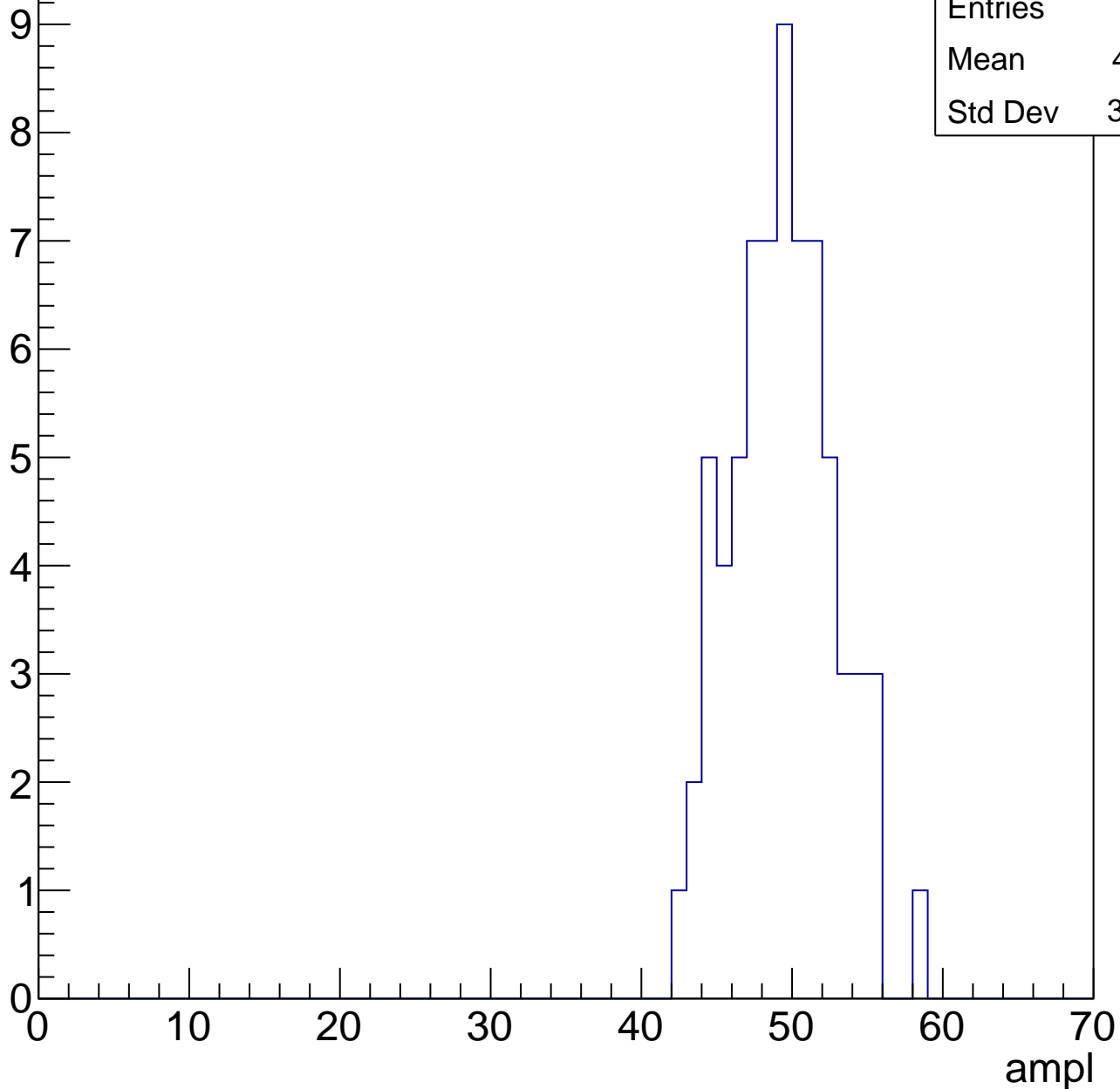
**Gaus Width: 3.8840**



# B1L101S, U11-ch66, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

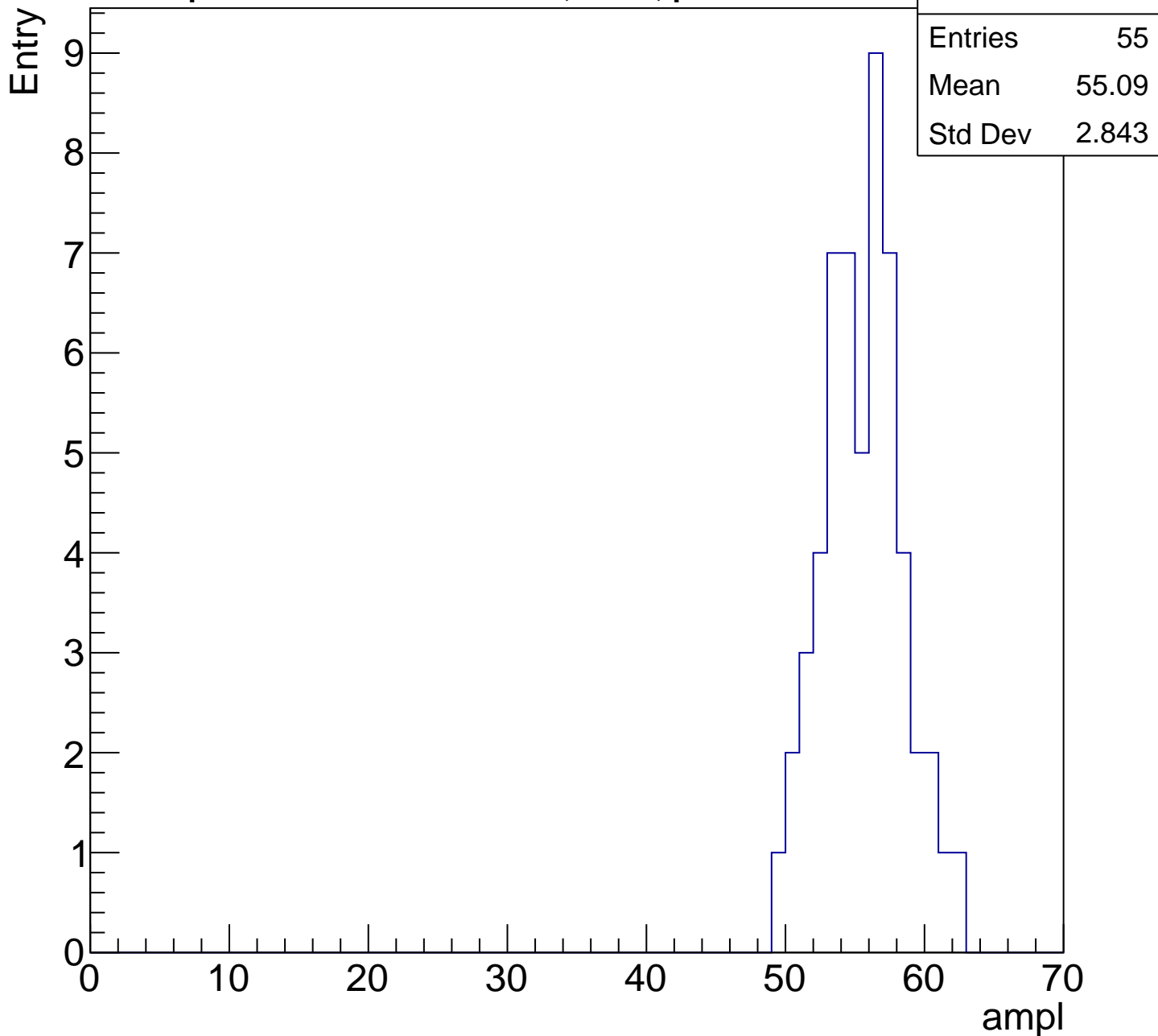
Entry



Entries	69
Mean	48.91
Std Dev	3.365

# B1L101S, U11-ch66, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

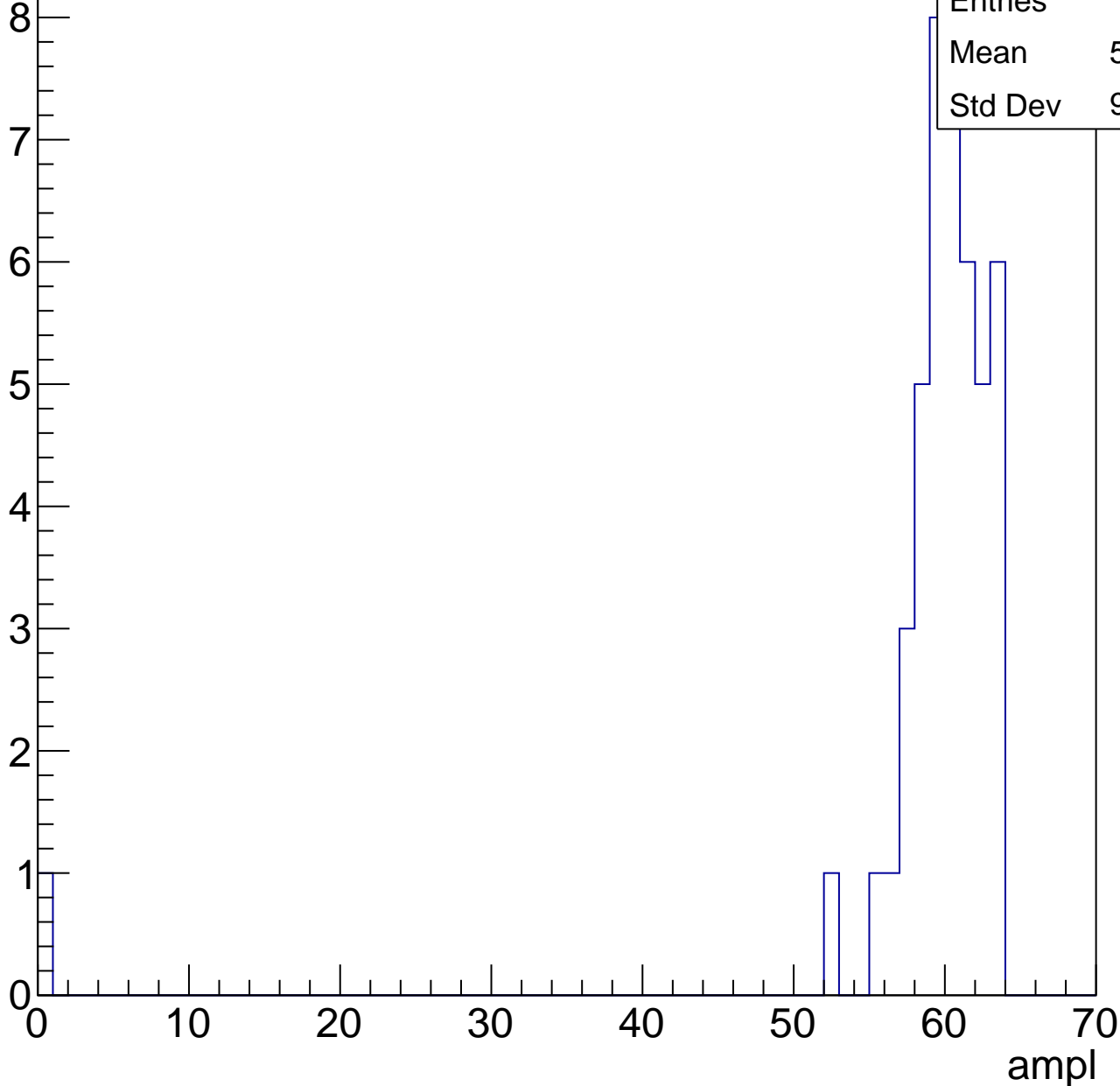


# B1L101S, U11-ch66, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

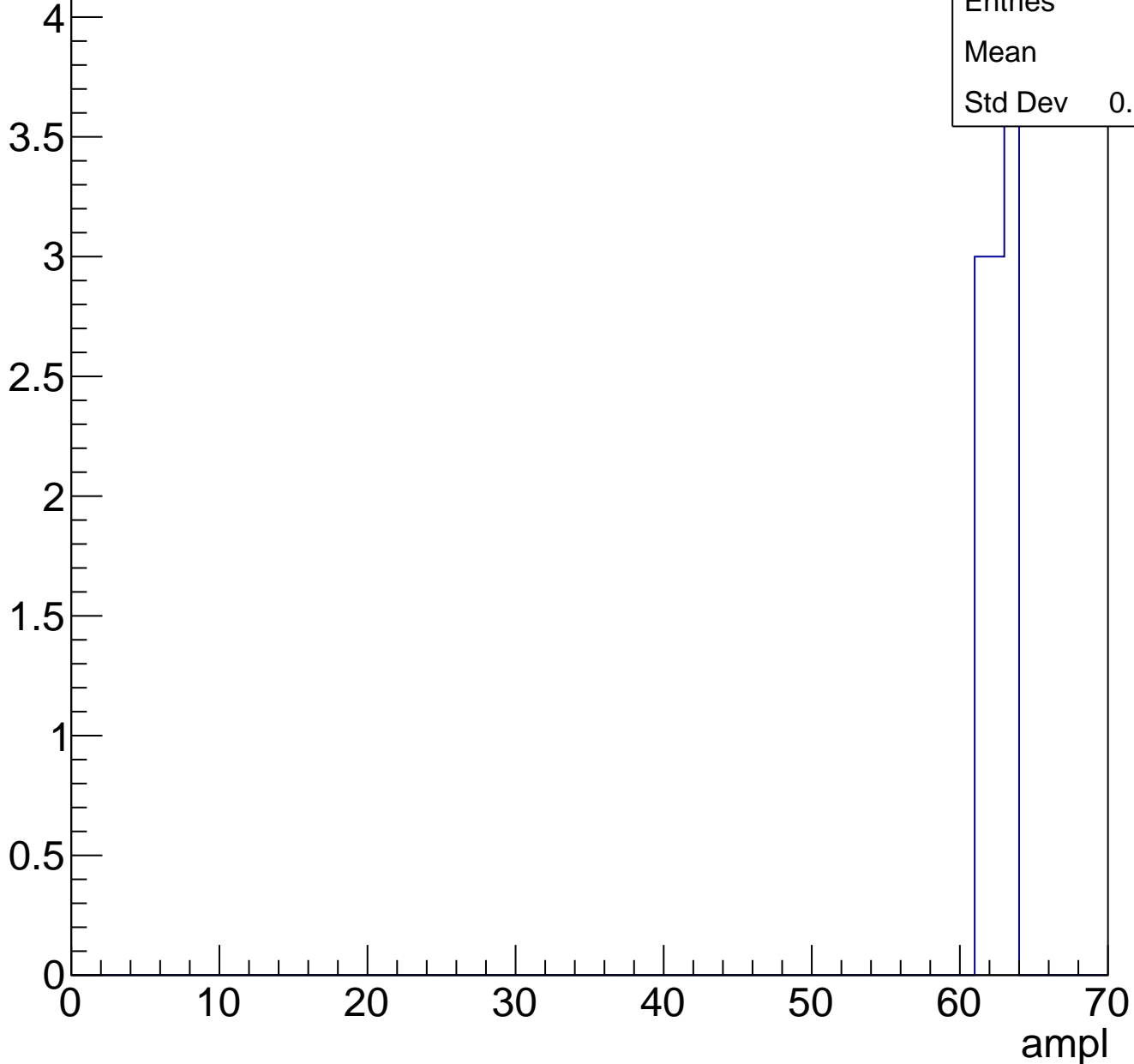
Entries	45
Mean	58.44
Std Dev	9.106



# B1L101S, U11-ch66, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch66, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U11-ch67, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	63
Mean	31.03
Std Dev	3.863

**Gaus mean : 30.4389**

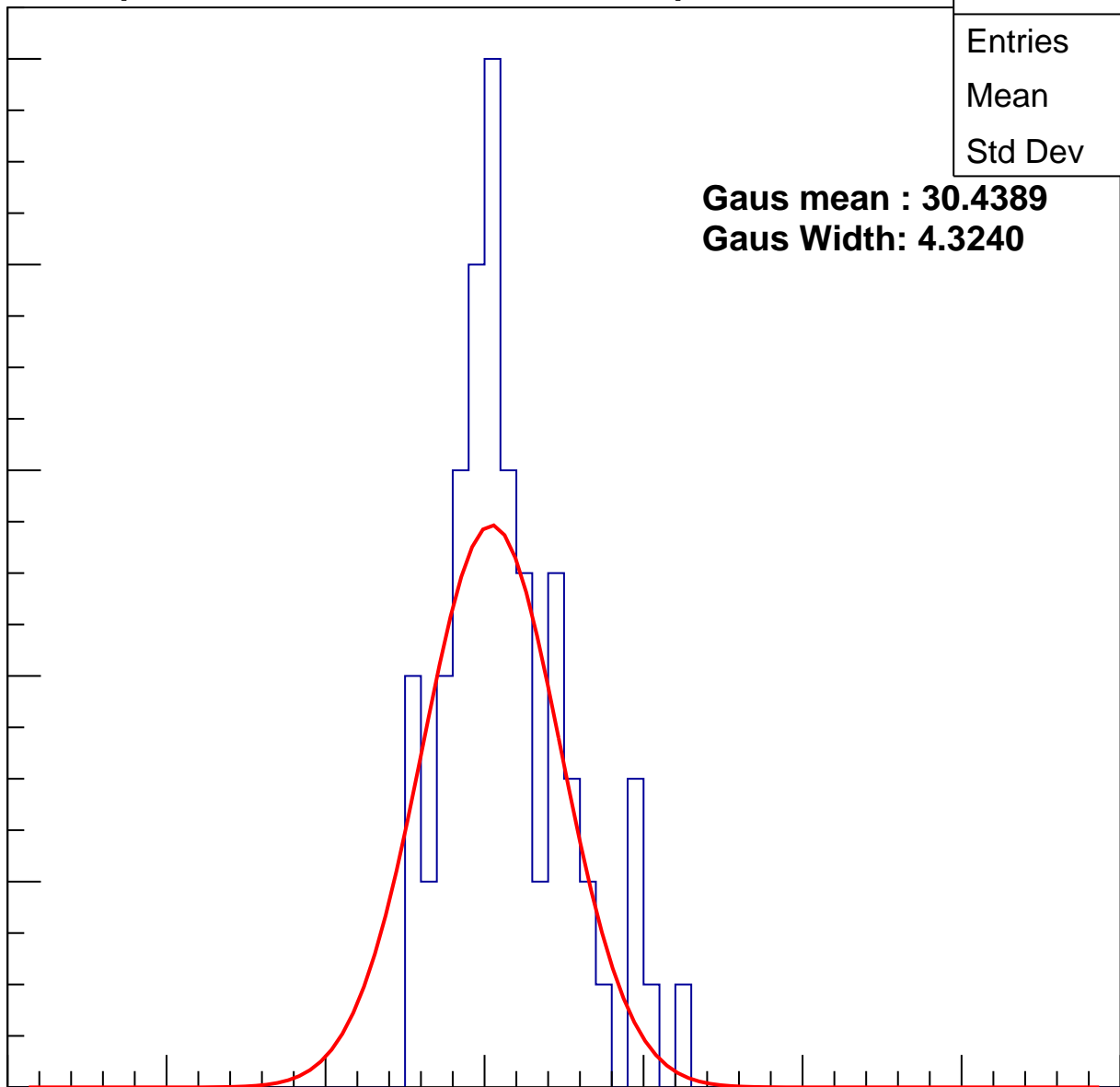
**Gaus Width: 4.3240**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U11-ch67, adc1

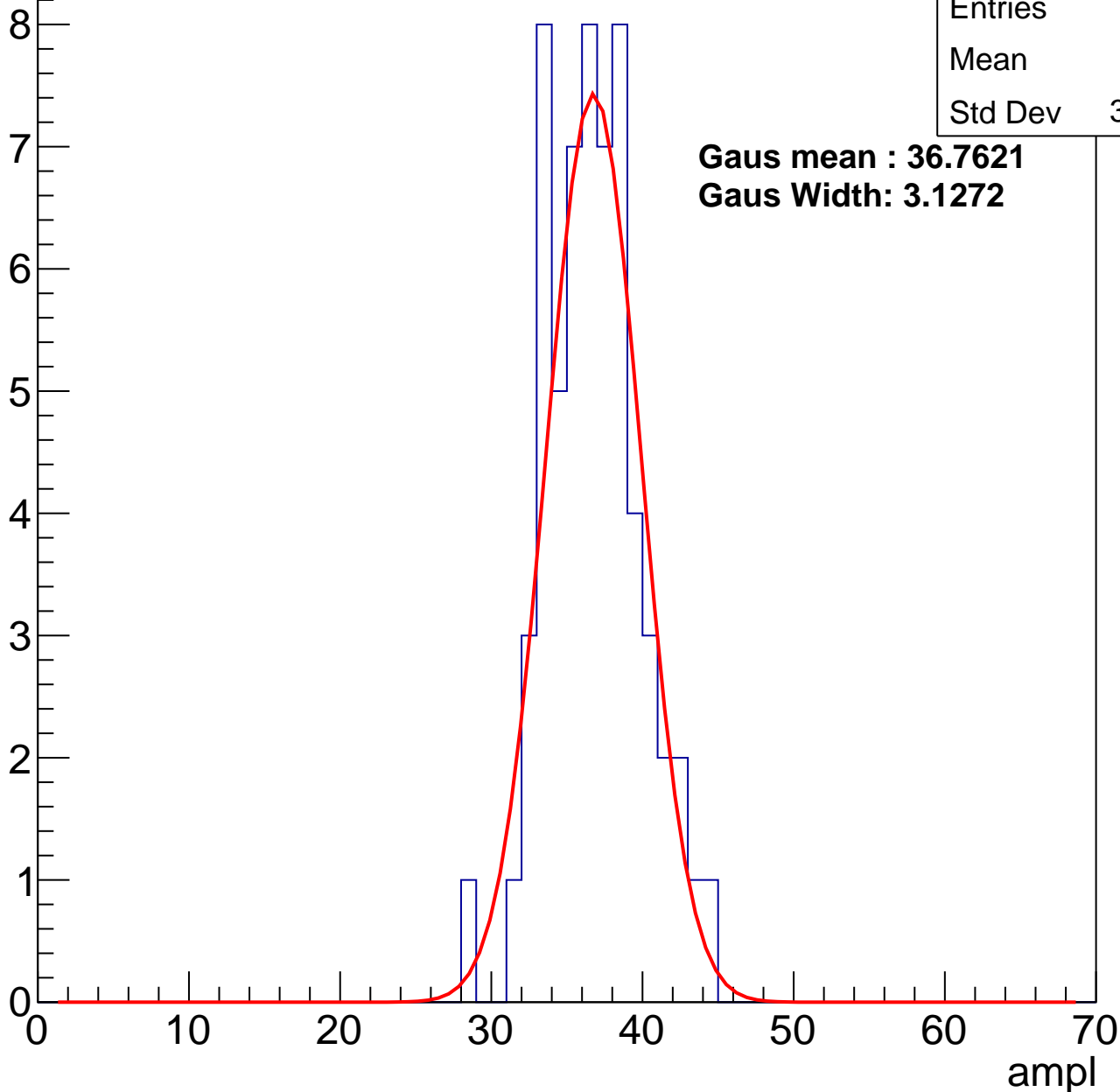
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	36.3
Std Dev	3.107

**Gaus mean : 36.7621**

**Gaus Width: 3.1272**



# B1L101S, U11-ch67, adc2

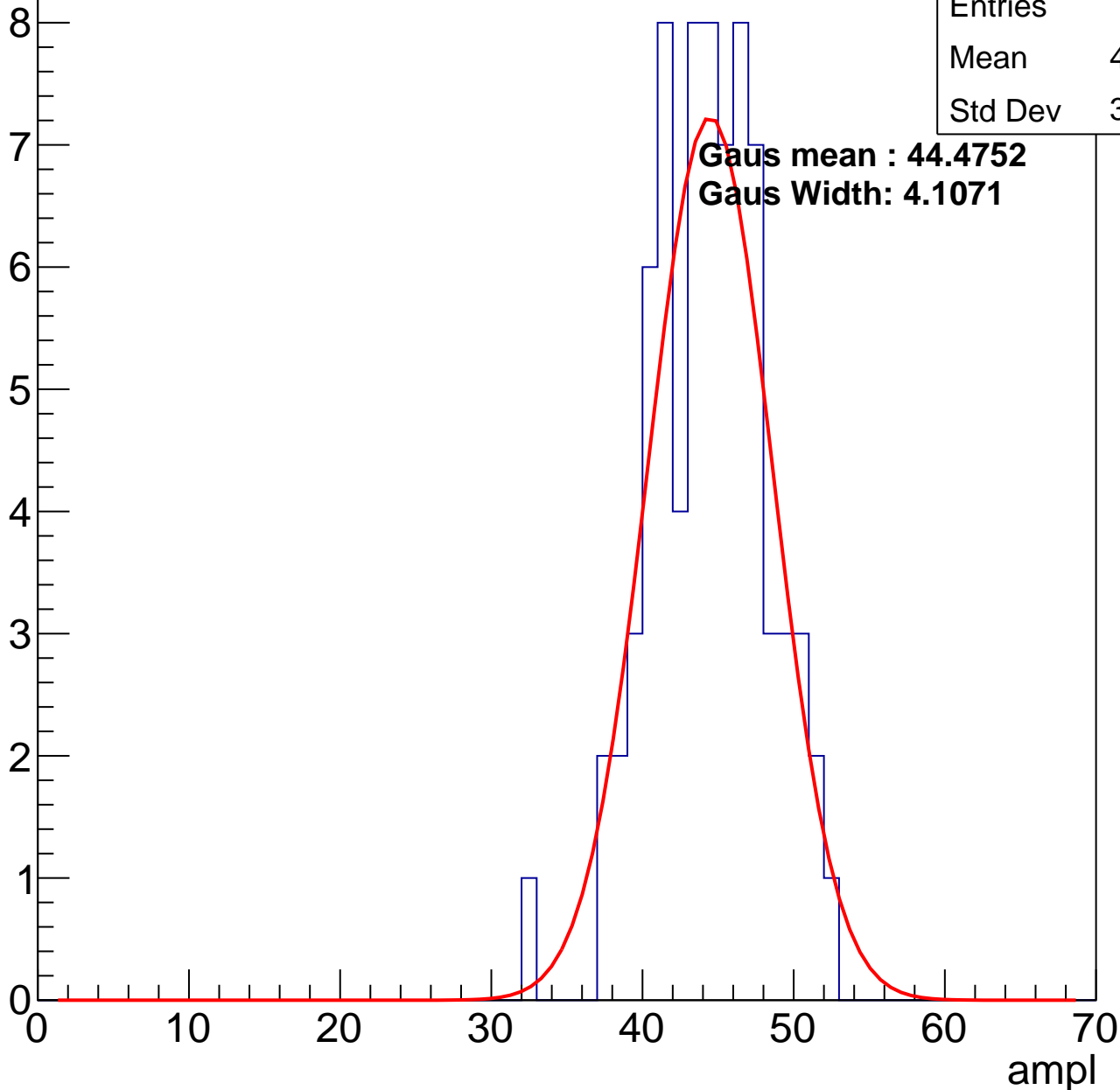
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	43.92
Std Dev	3.762

**Gaus mean : 44.4752**

**Gaus Width: 4.1071**

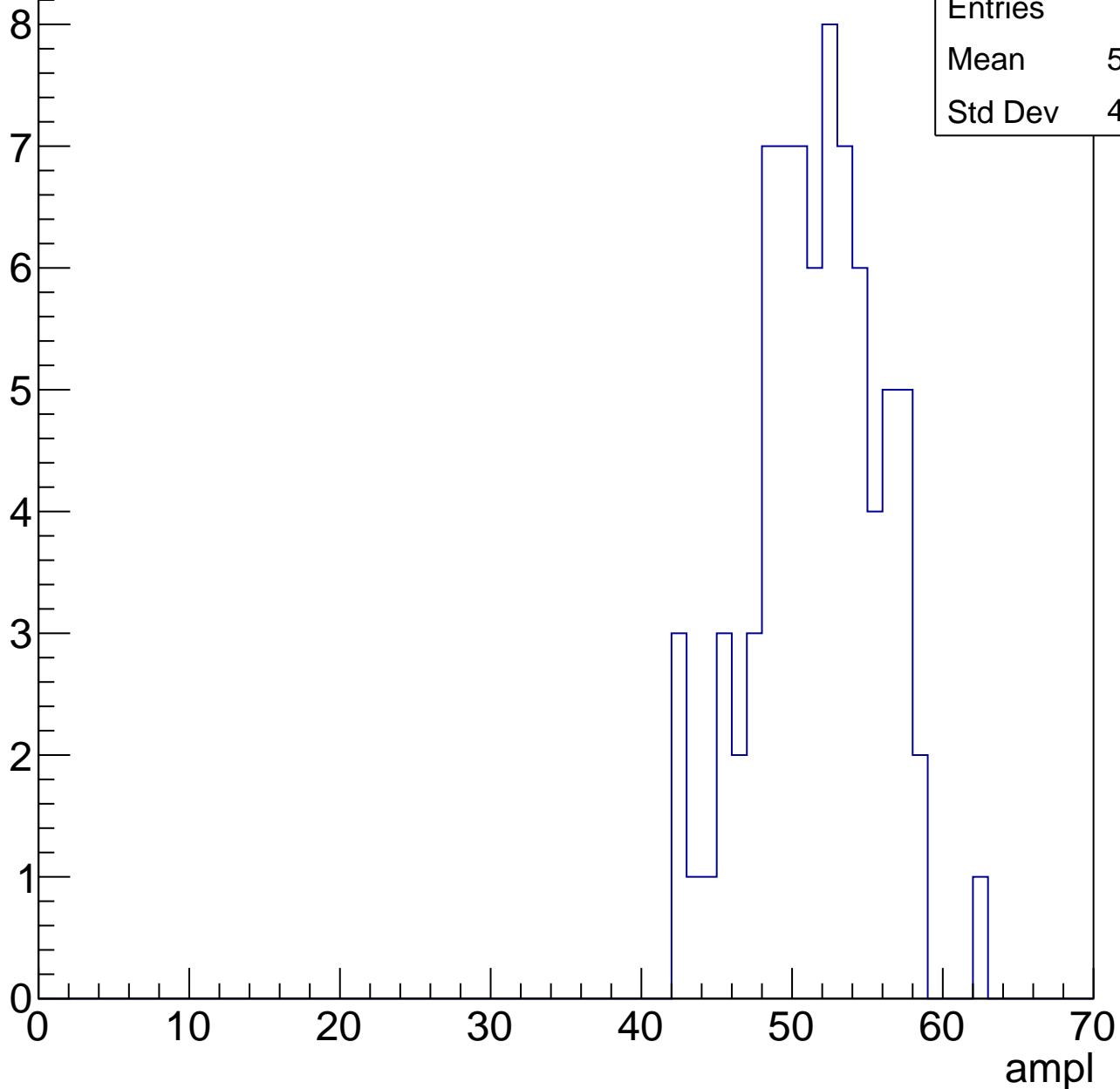


# B1L101S, U11-ch67, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

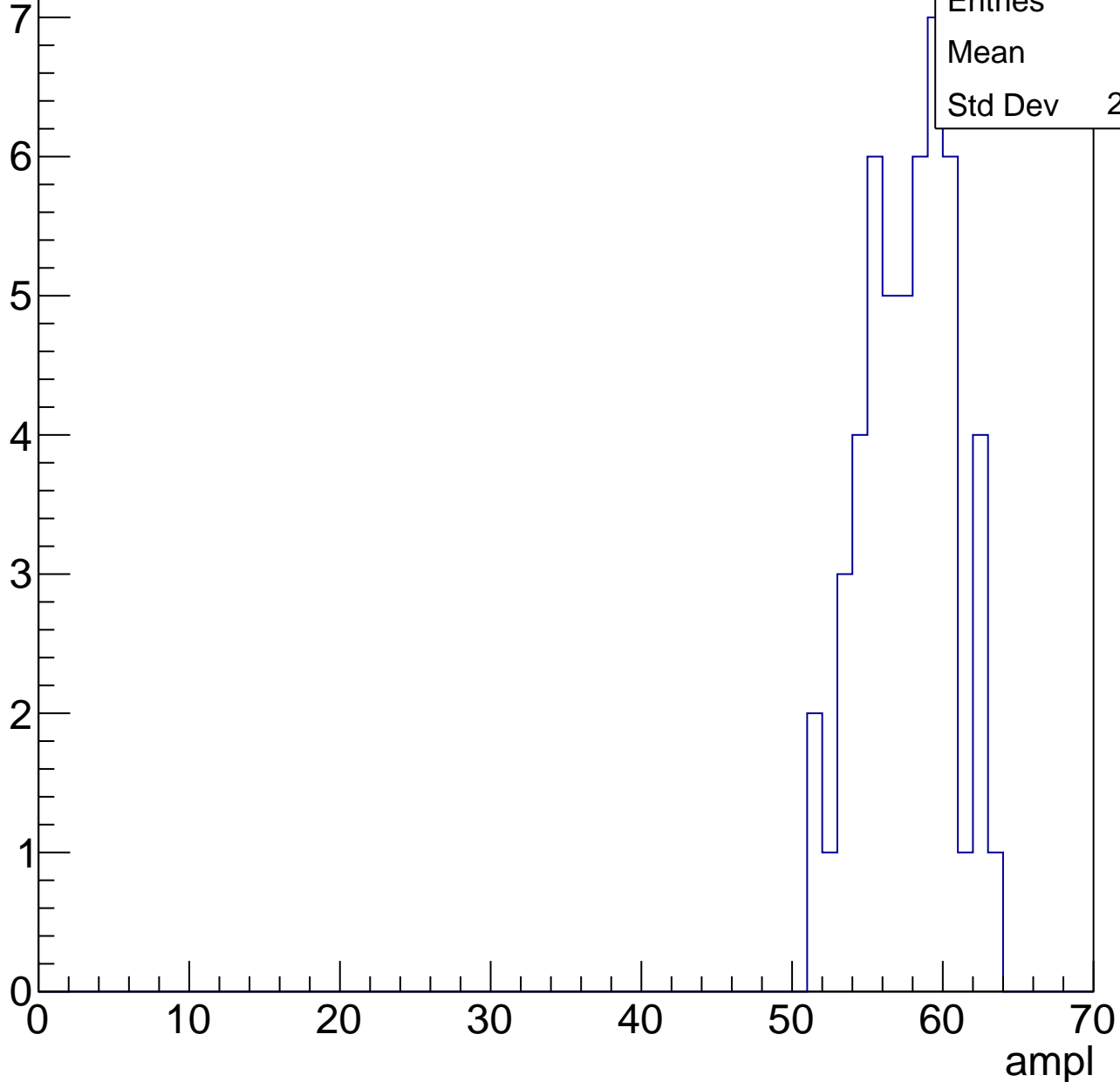
Entries	78
Mean	51.15
Std Dev	4.139



# B1L101S, U11-ch67, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

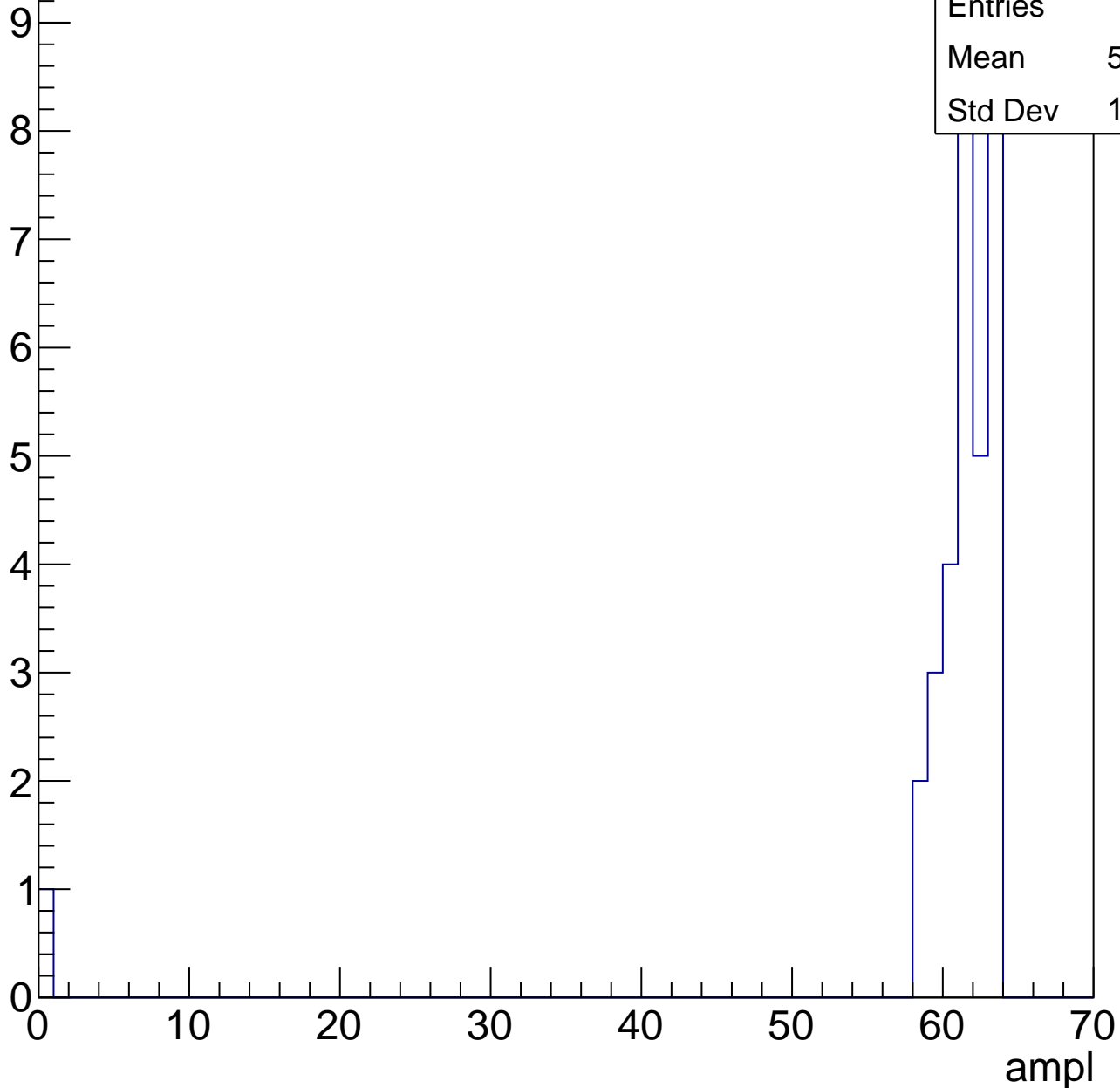
Entry



# B1L101S, U11-ch67, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U11-ch67, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch67, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U11-ch68, adc0

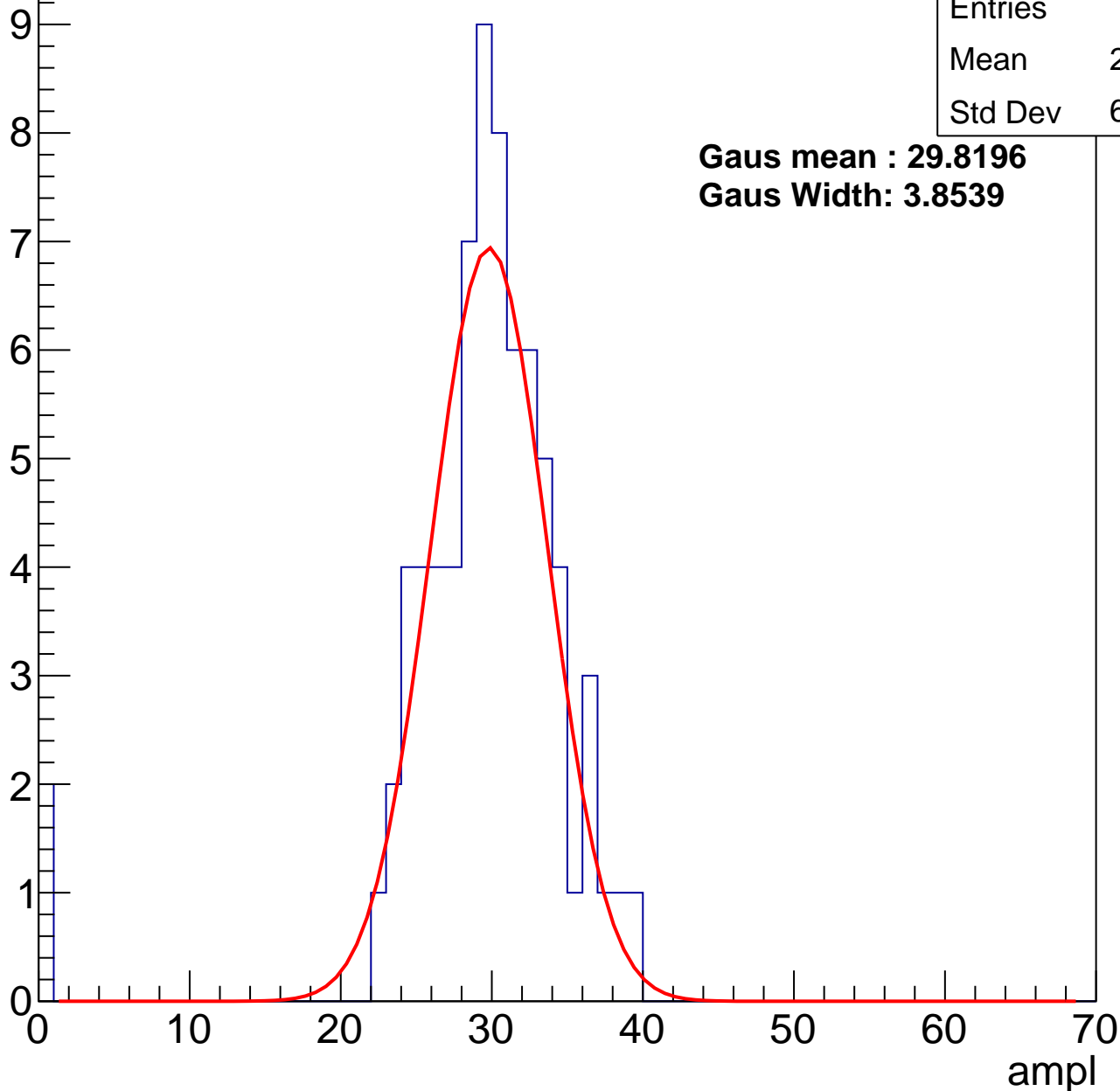
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	28.89
Std Dev	6.103

**Gaus mean : 29.8196**

**Gaus Width: 3.8539**



# B1L101S, U11-ch68, adc1

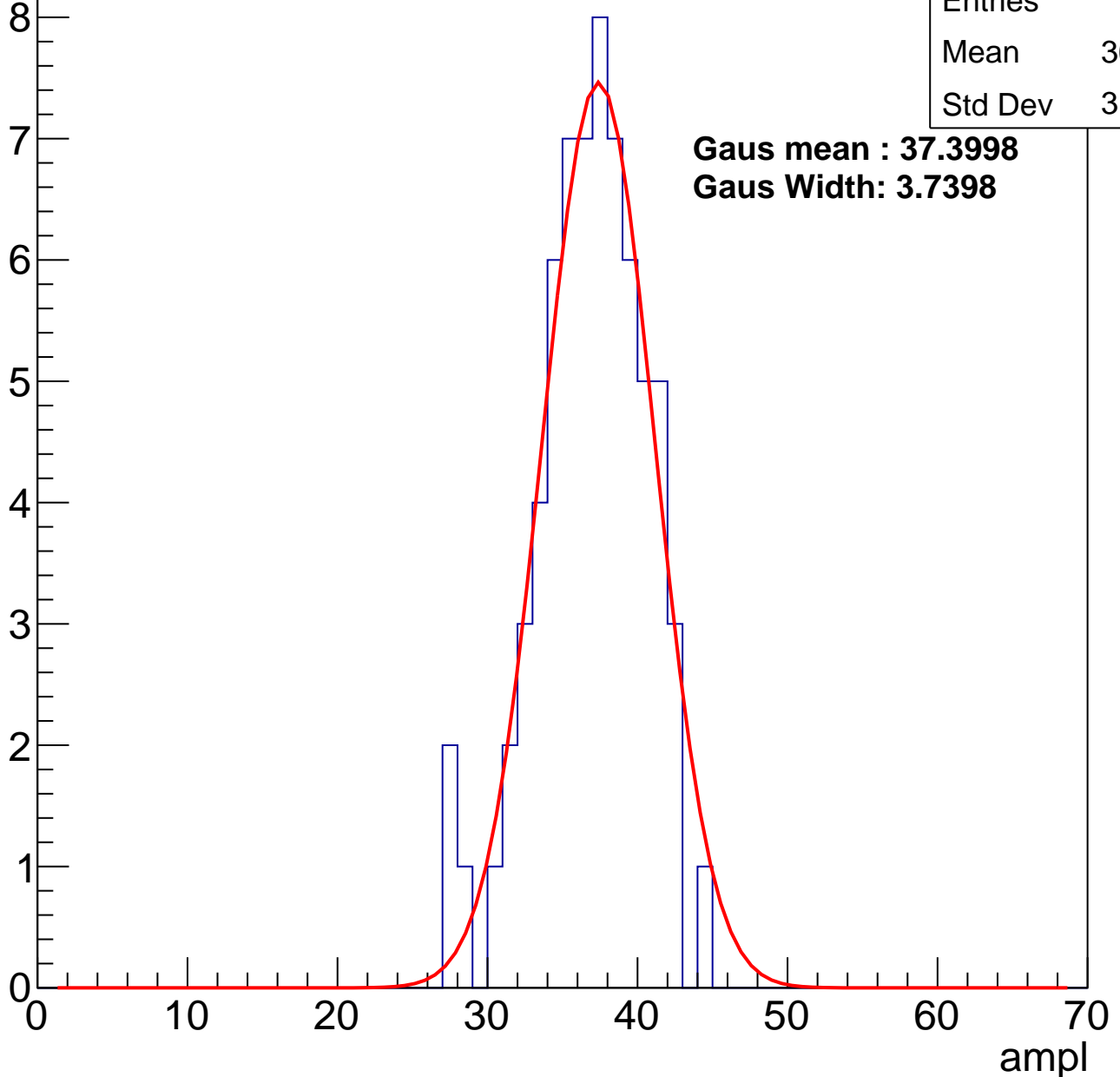
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	36.38
Std Dev	3.606

**Gaus mean : 37.3998**

**Gaus Width: 3.7398**



# B1L101S, U11-ch68, adc2

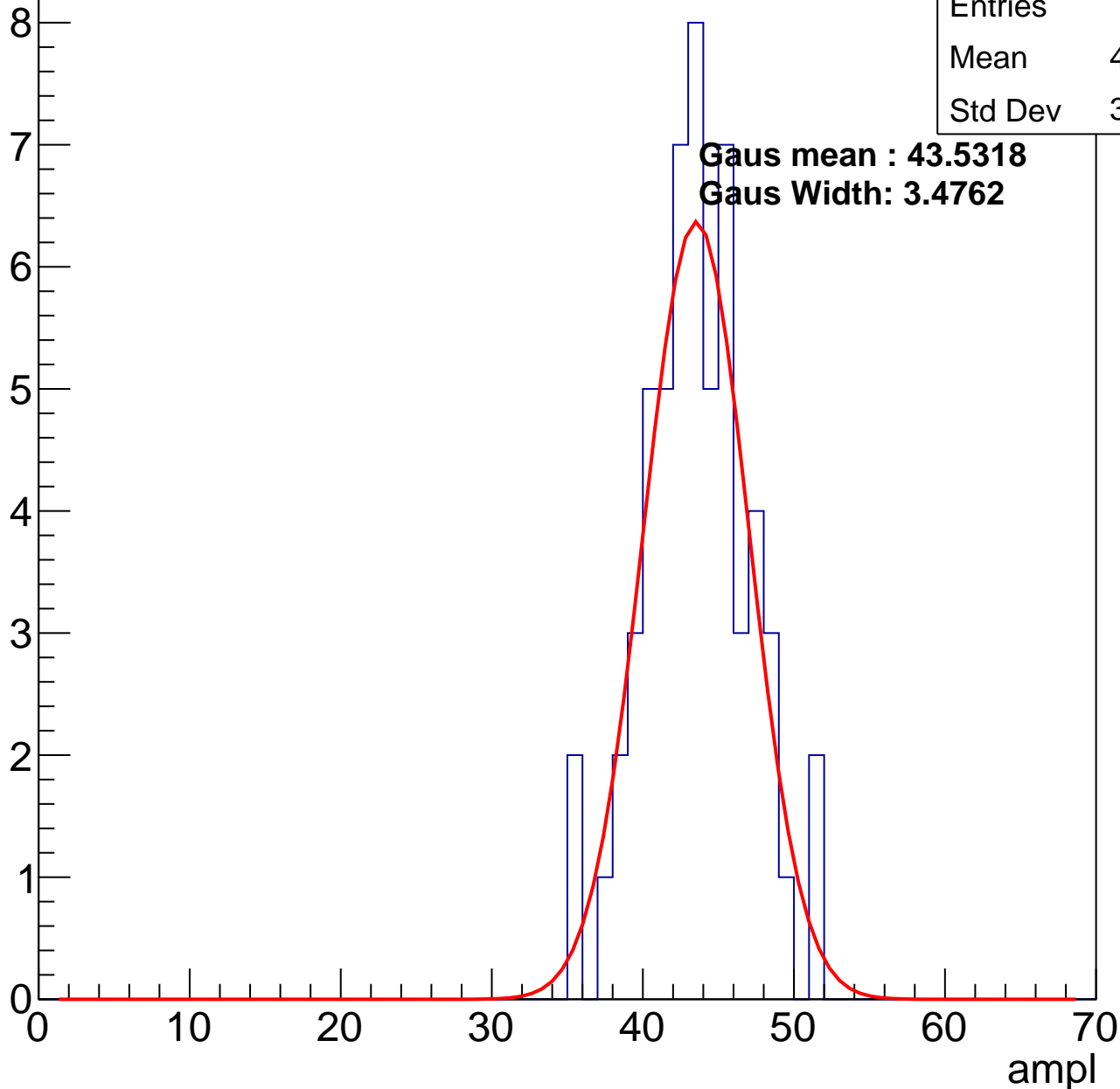
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	43.09
Std Dev	3.466

**Gaus mean : 43.5318**

**Gaus Width: 3.4762**

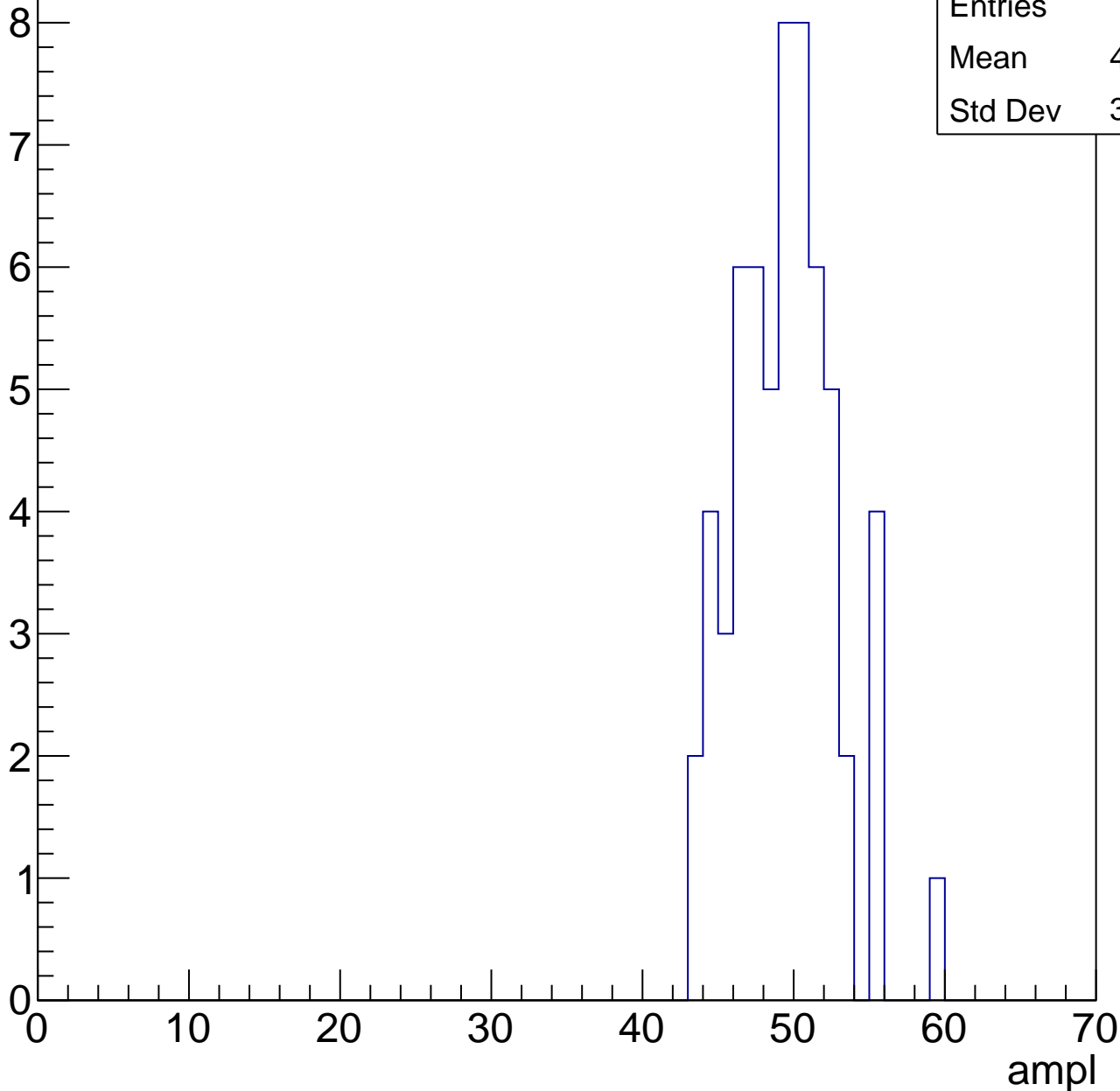


# B1L101S, U11-ch68, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

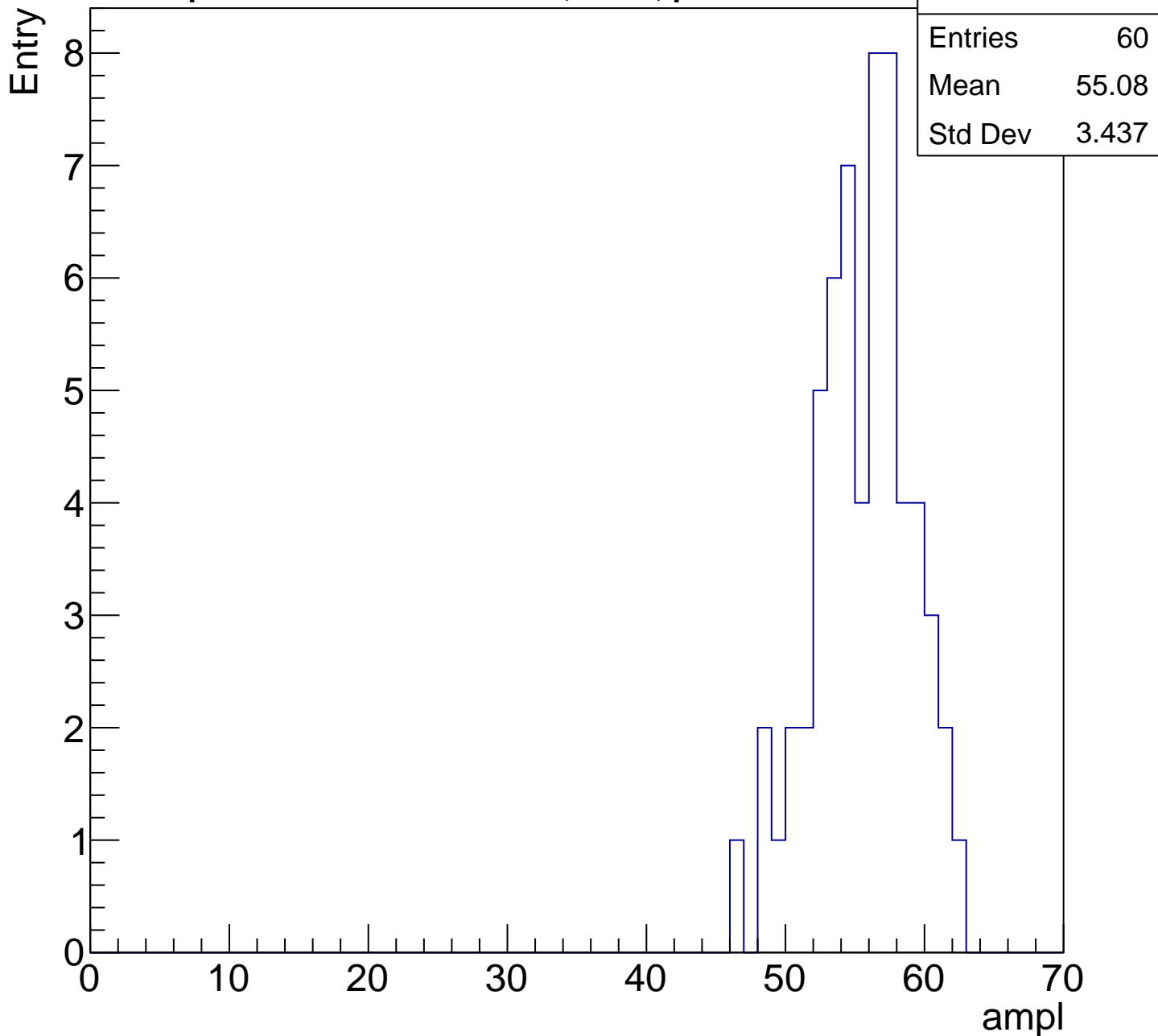
Entry

Entries	60
Mean	48.97
Std Dev	3.306



# B1L101S, U11-ch68, adc4

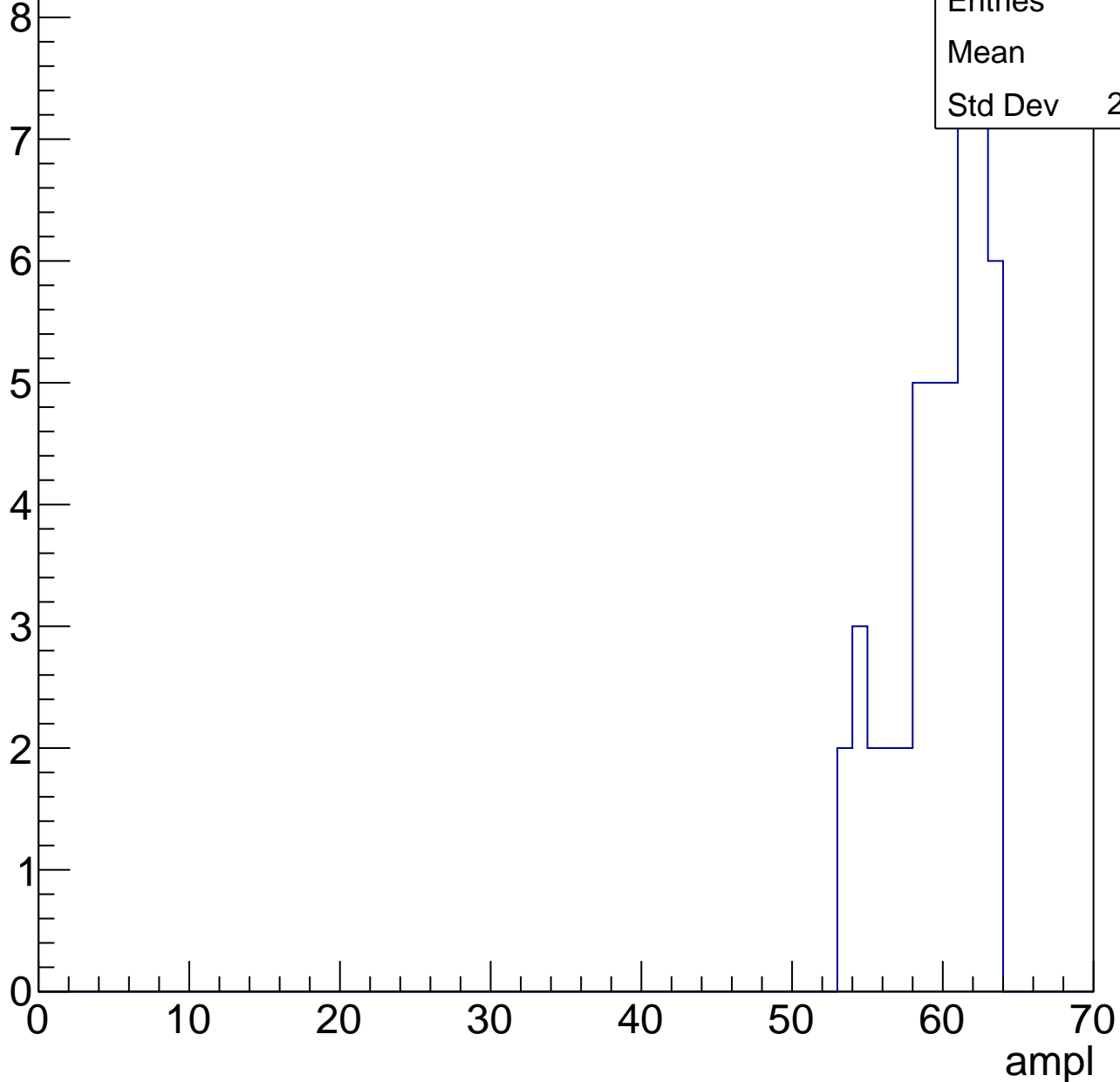
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U11-ch68, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

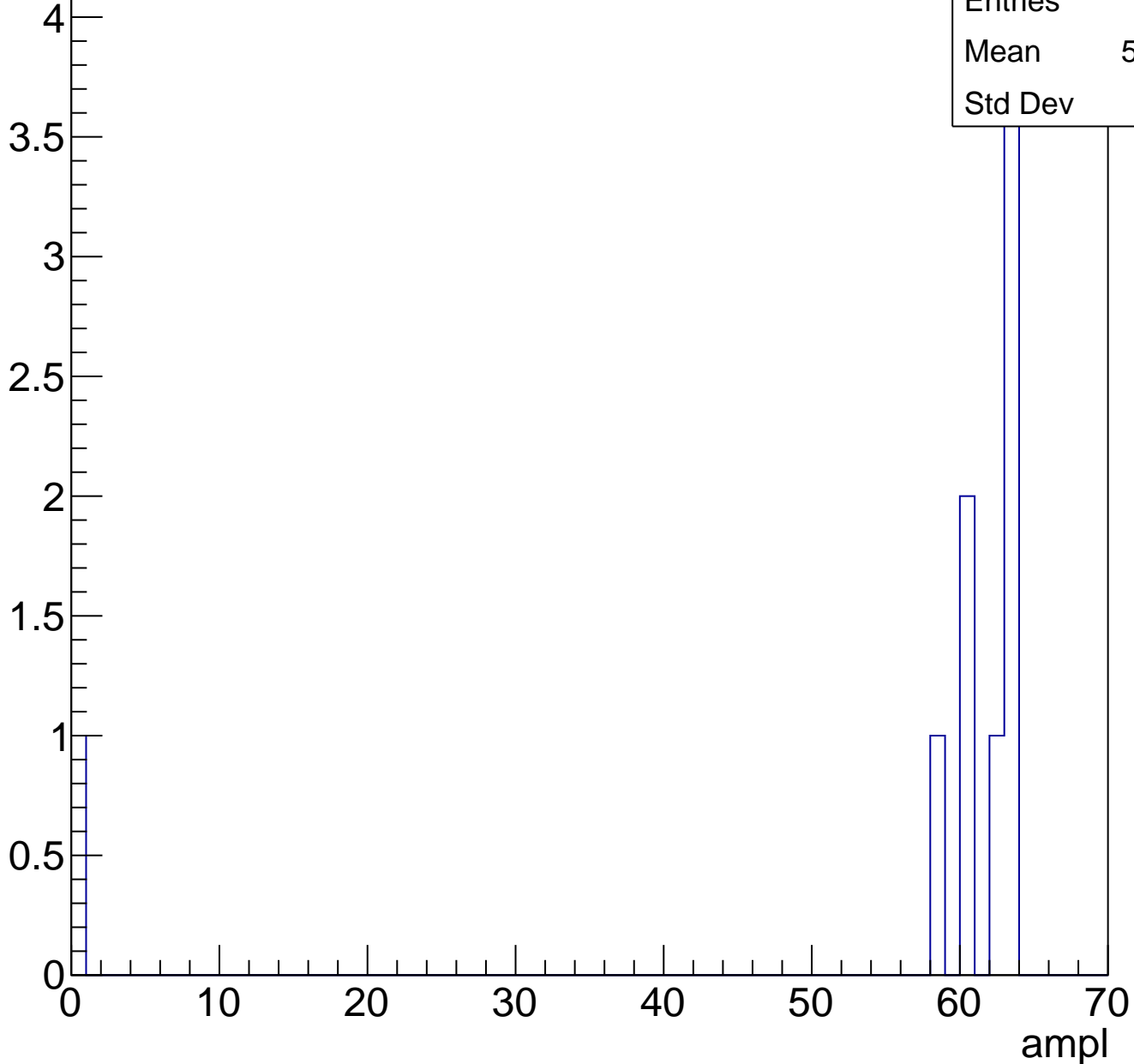


Entries	48
Mean	59.4
Std Dev	2.914

# B1L101S, U11-ch68, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch68, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U11-ch69, adc0

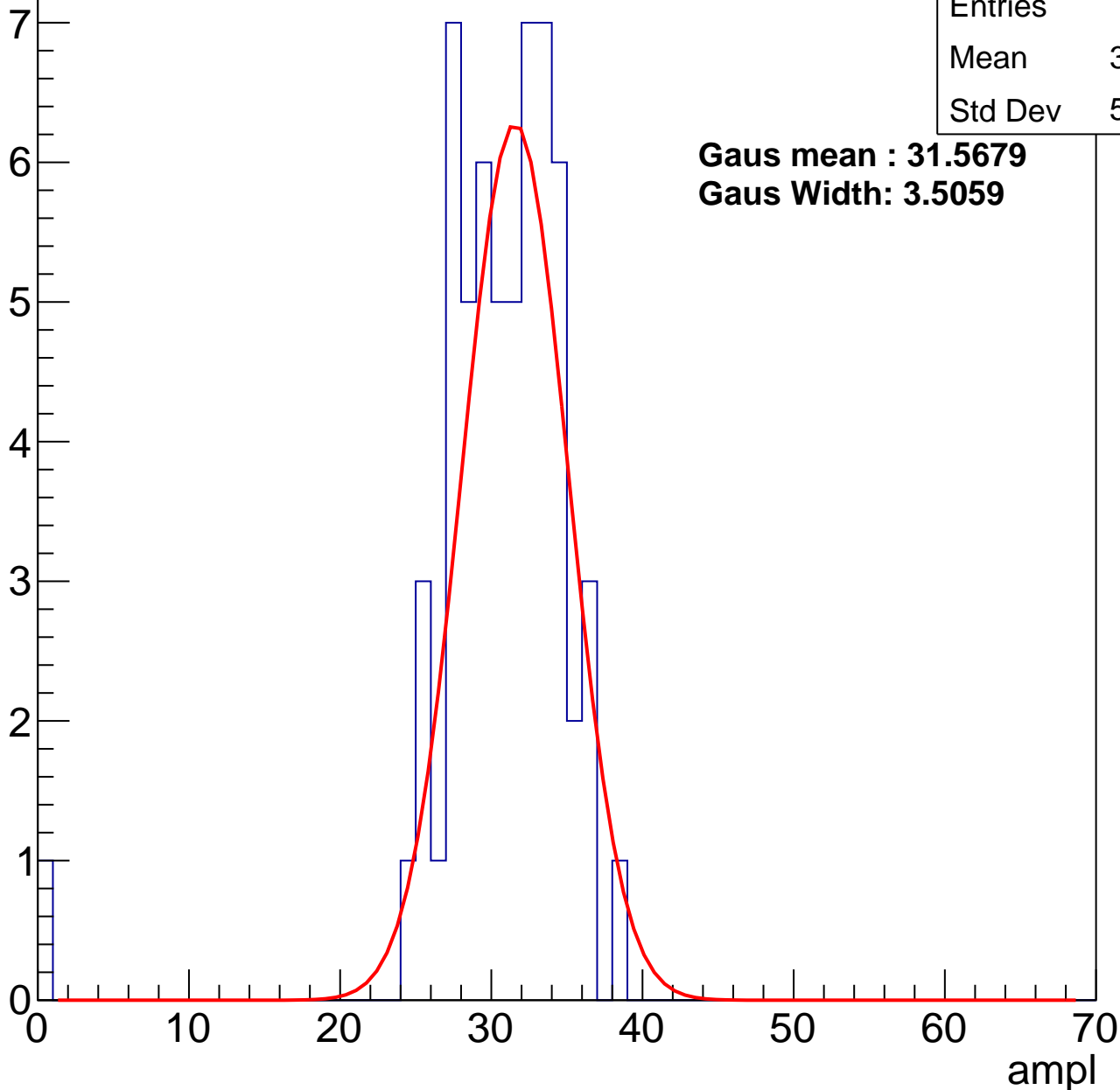
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	30.13
Std Dev	5.048

**Gaus mean : 31.5679**

**Gaus Width: 3.5059**



# B1L101S, U11-ch69, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	37.03
Std Dev	3.354

**Gaus mean : 37.7816**

**Gaus Width: 3.4328**

10

8

6

4

2

0

0

10

20

30

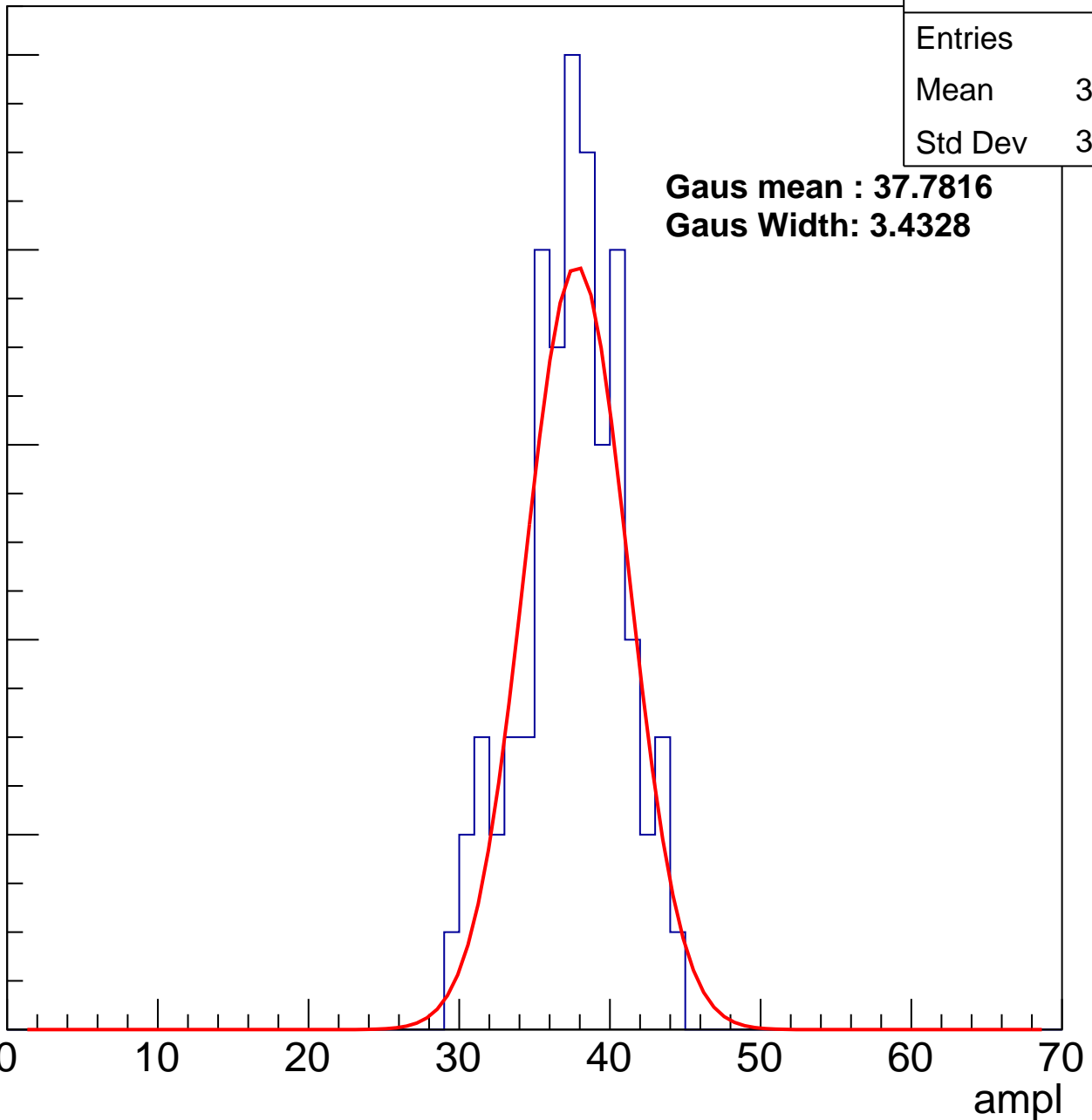
40

50

60

70

ampl



# B1L101S, U11-ch69, adc2

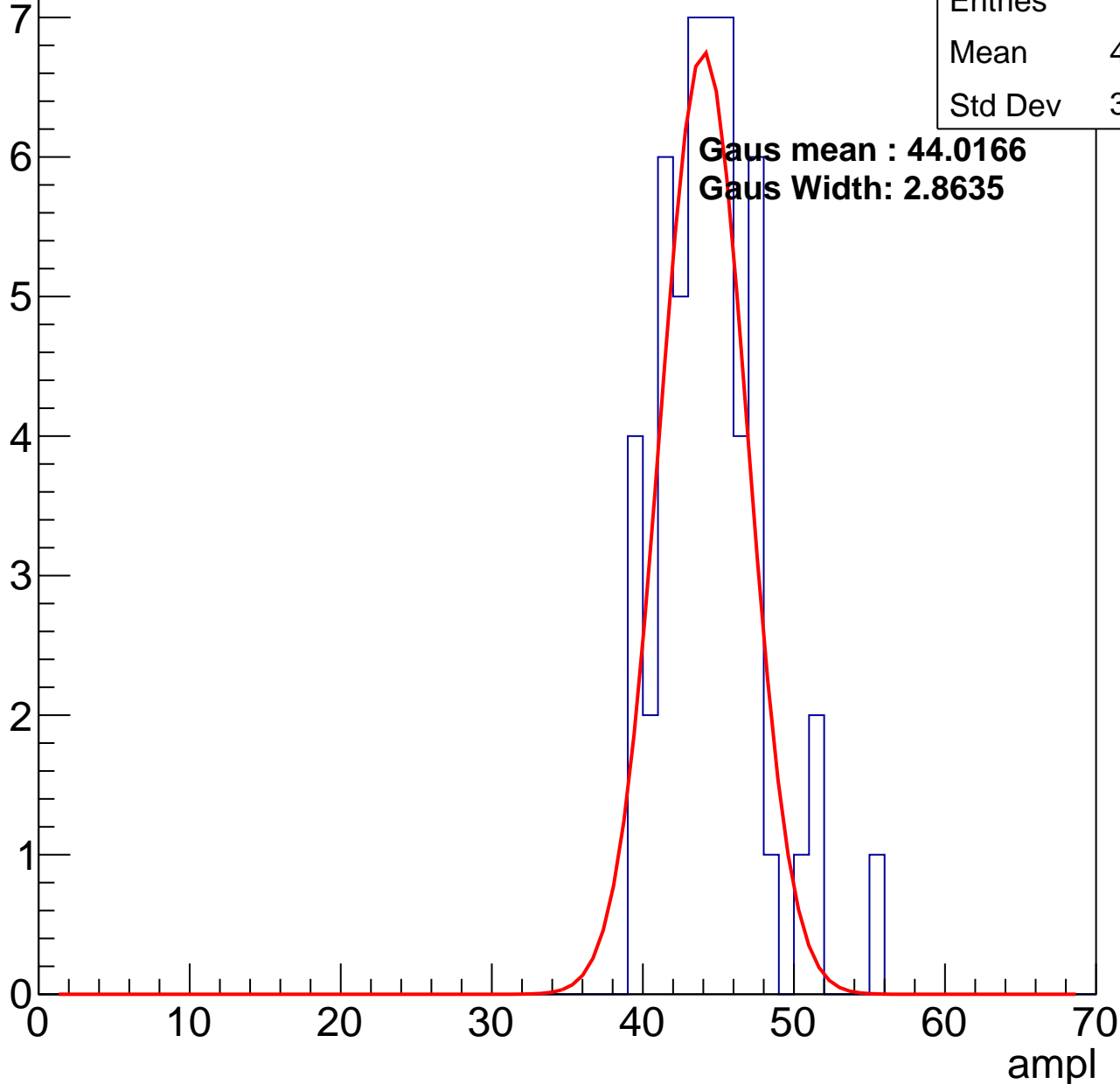
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	44.09
Std Dev	3.252

**Gaus mean : 44.0166**

**Gaus Width: 2.8635**

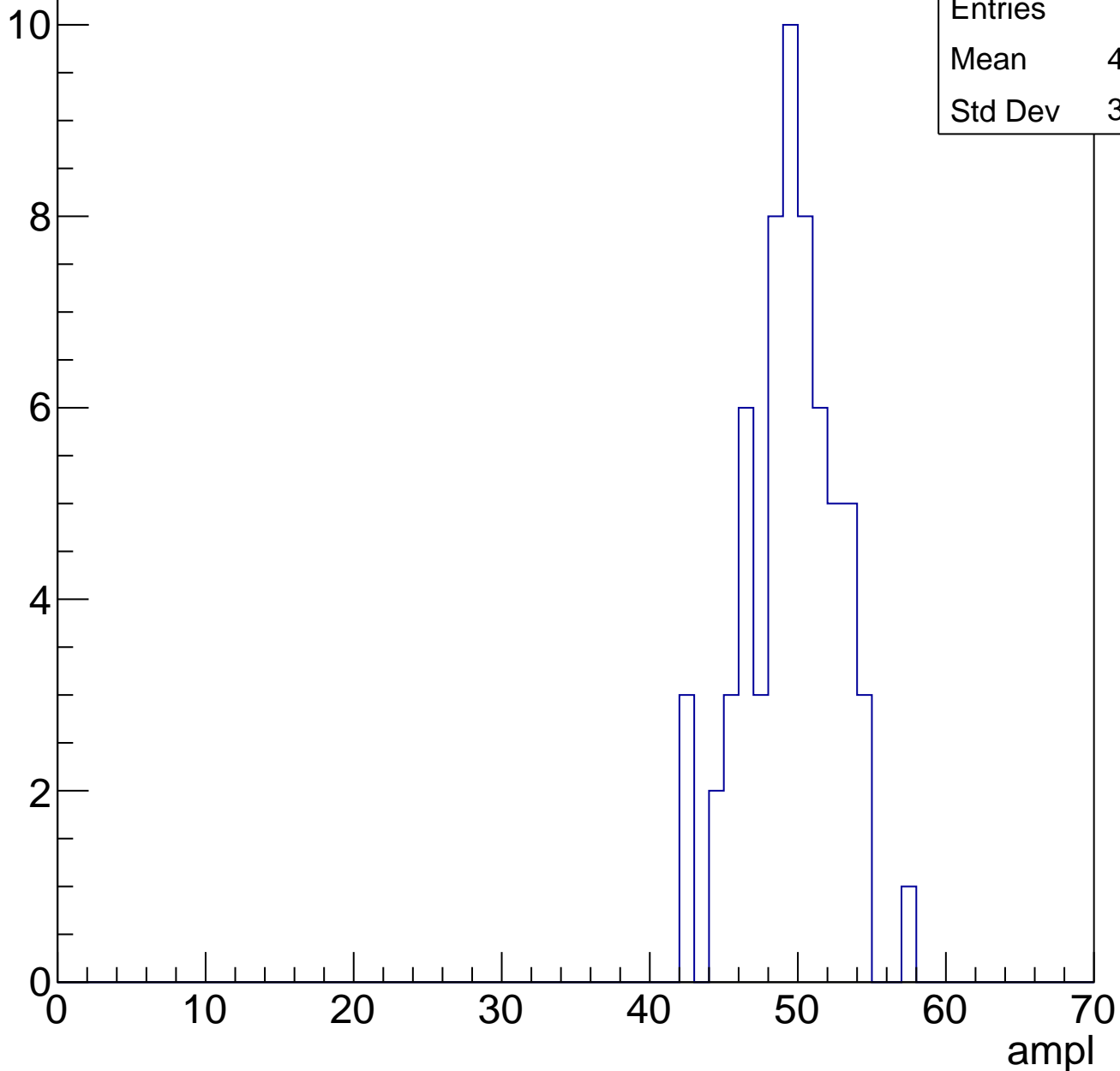


# B1L101S, U11-ch69, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	49.05
Std Dev	3.124

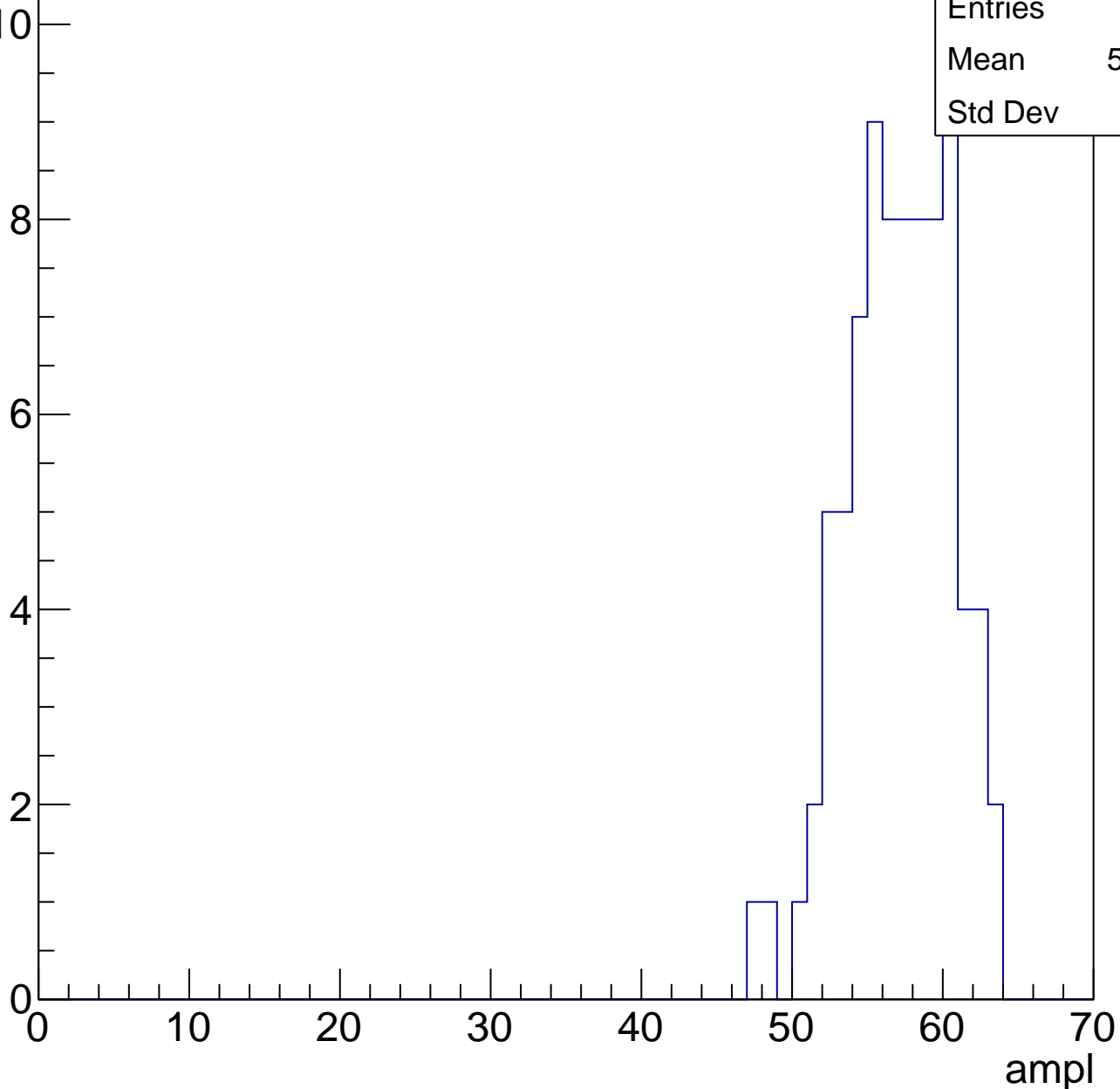


# B1L101S, U11-ch69, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	83
Mean	56.66
Std Dev	3.42

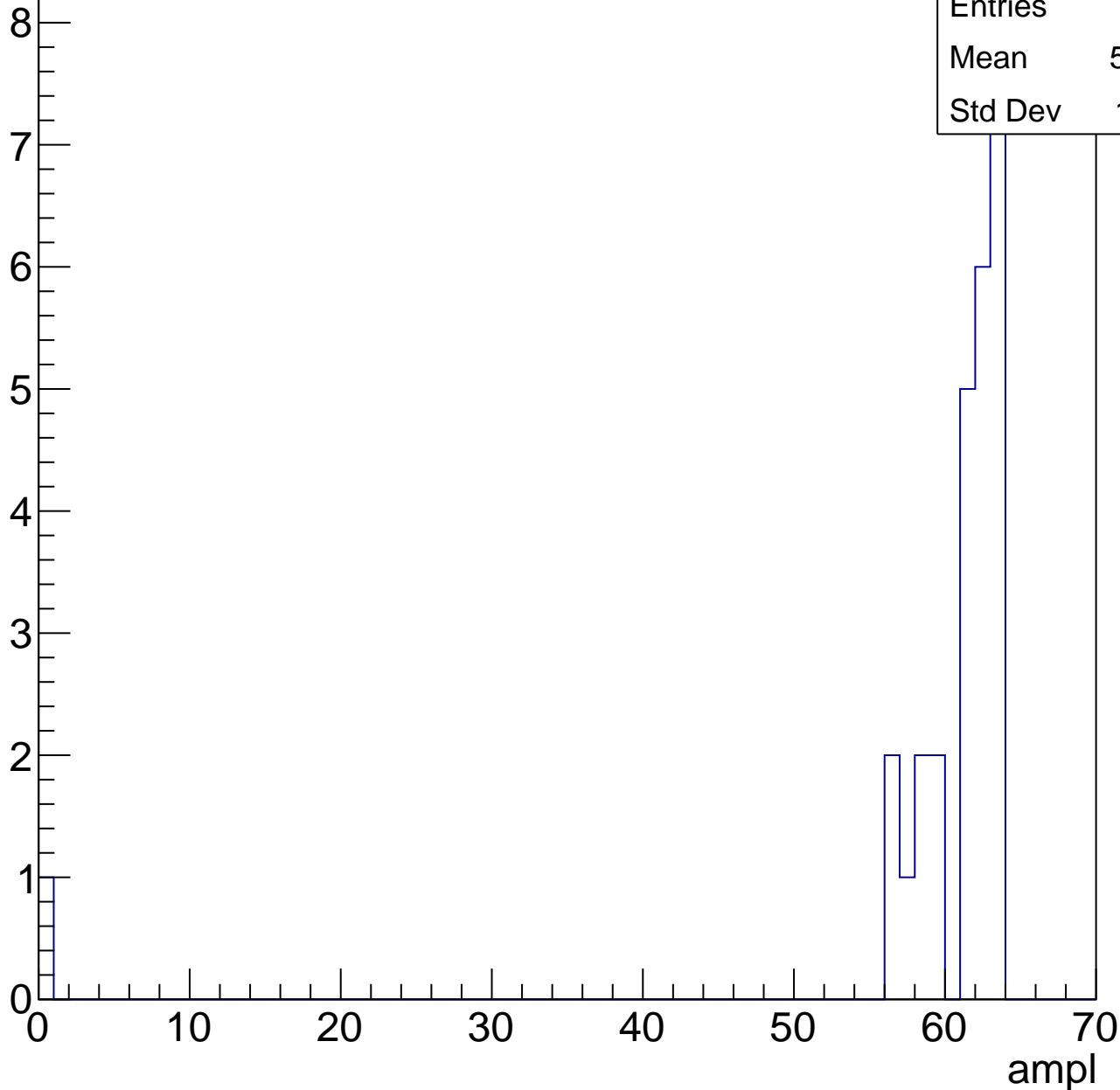


# B1L101S, U11-ch69, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	27
Mean	58.67
Std Dev	11.71



# B1L101S, U11-ch69, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

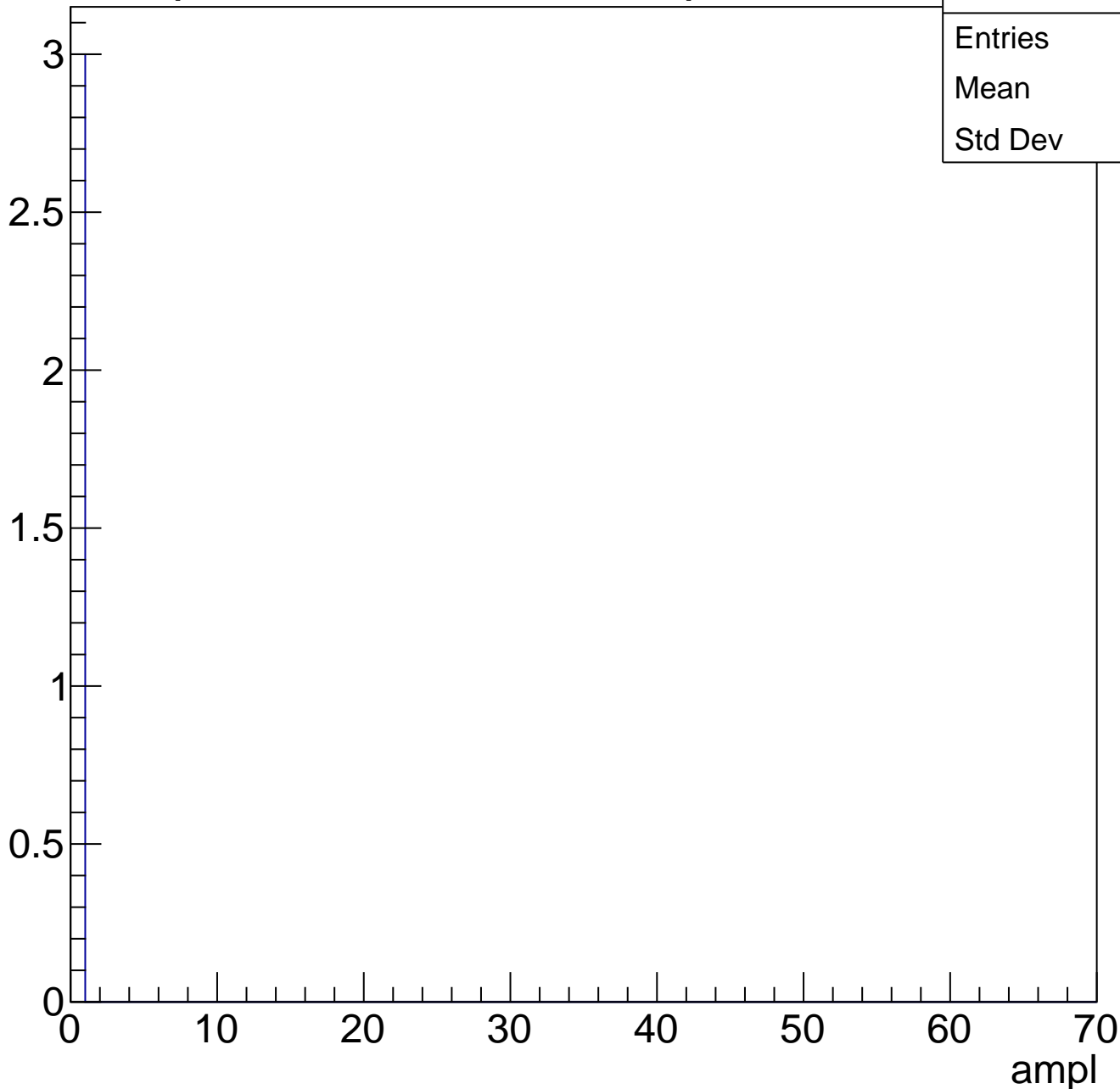




# B1L101S, U11-ch69, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L101S, U11-ch70, adc0

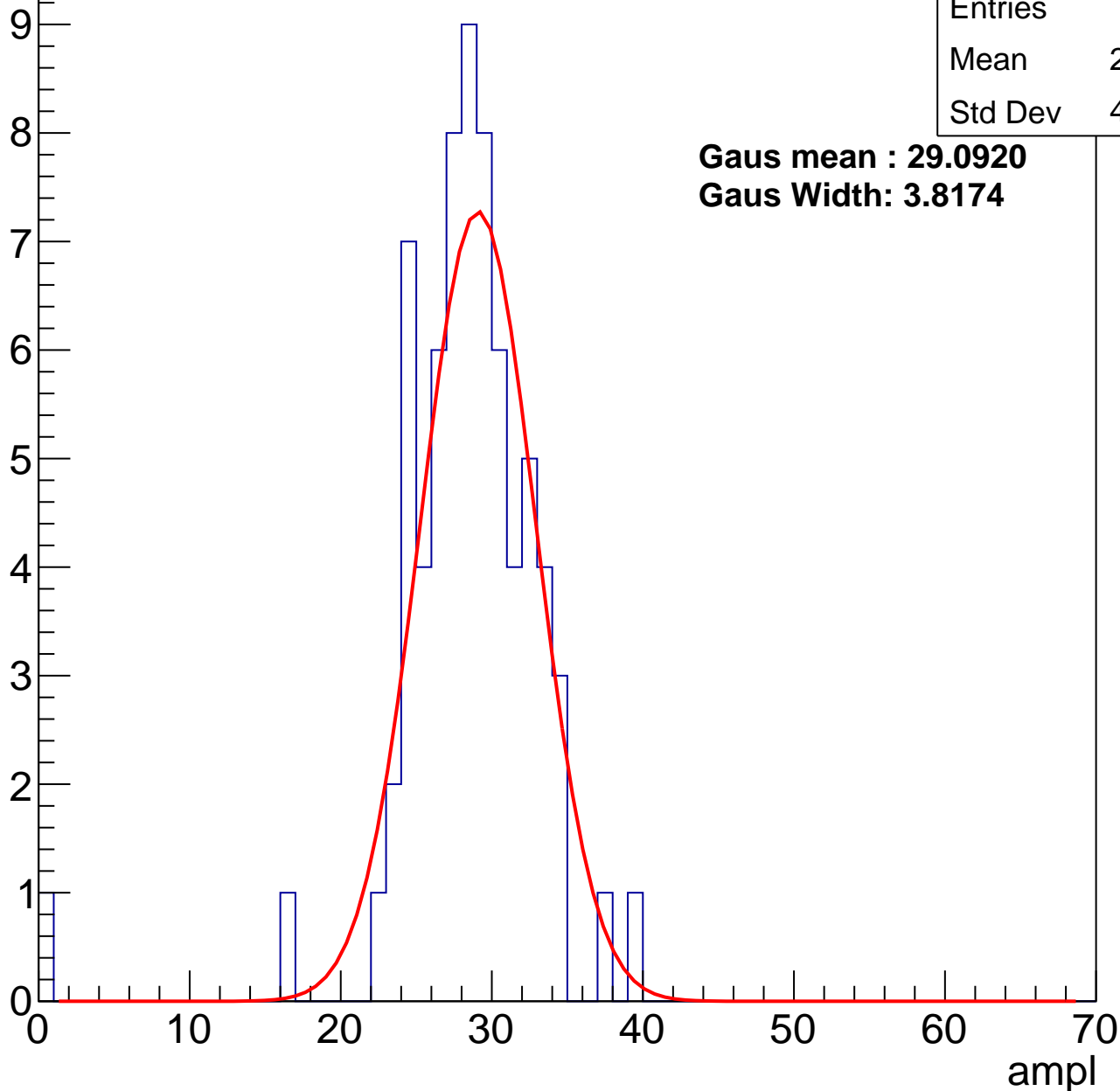
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	27.92
Std Dev	4.967

**Gaus mean : 29.0920**

**Gaus Width: 3.8174**



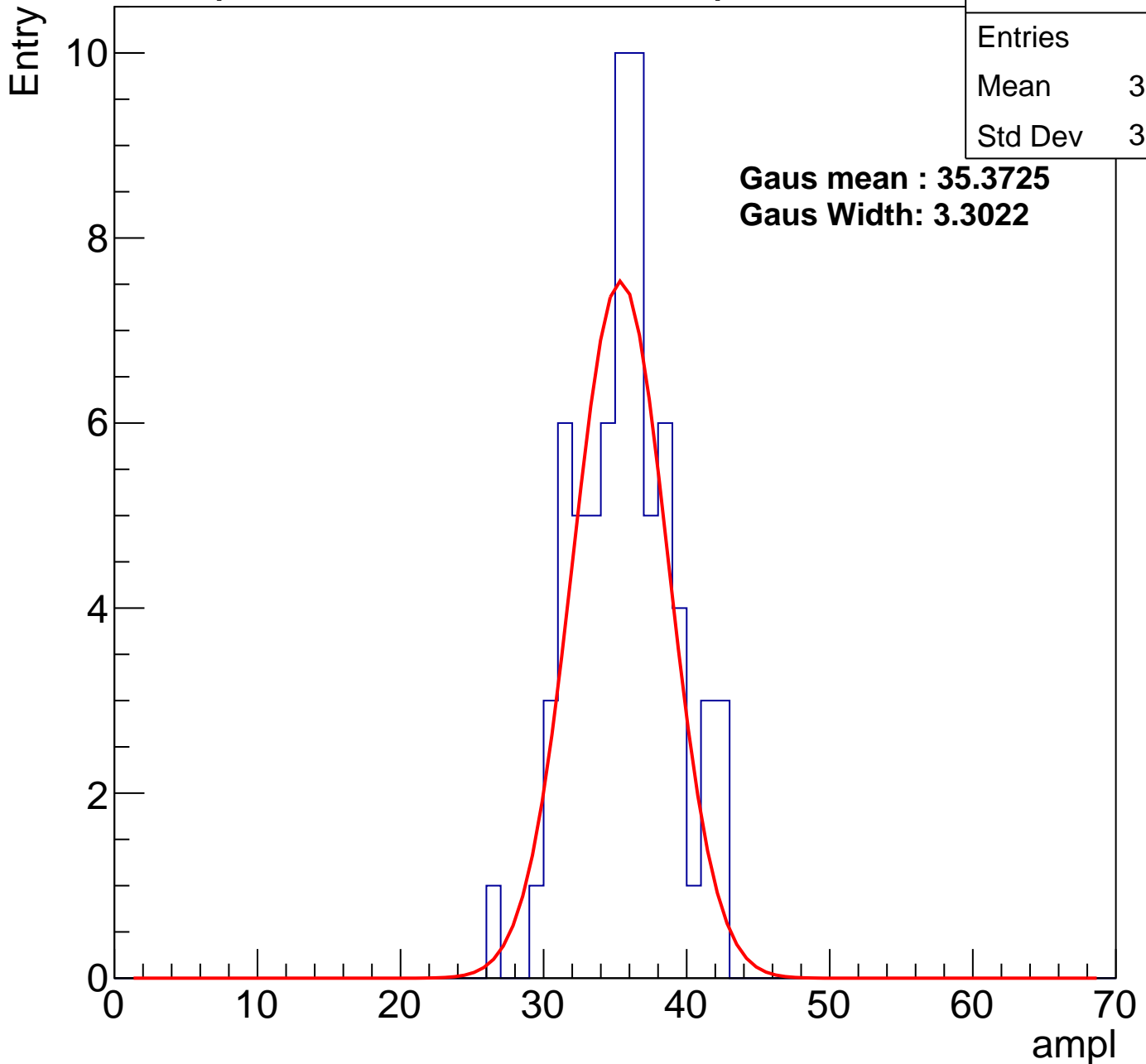
# B1L101S, U11-ch70, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	69
Mean	35.19
Std Dev	3.372

**Gaus mean : 35.3725**

**Gaus Width: 3.3022**



# B1L101S, U11-ch70, adc2

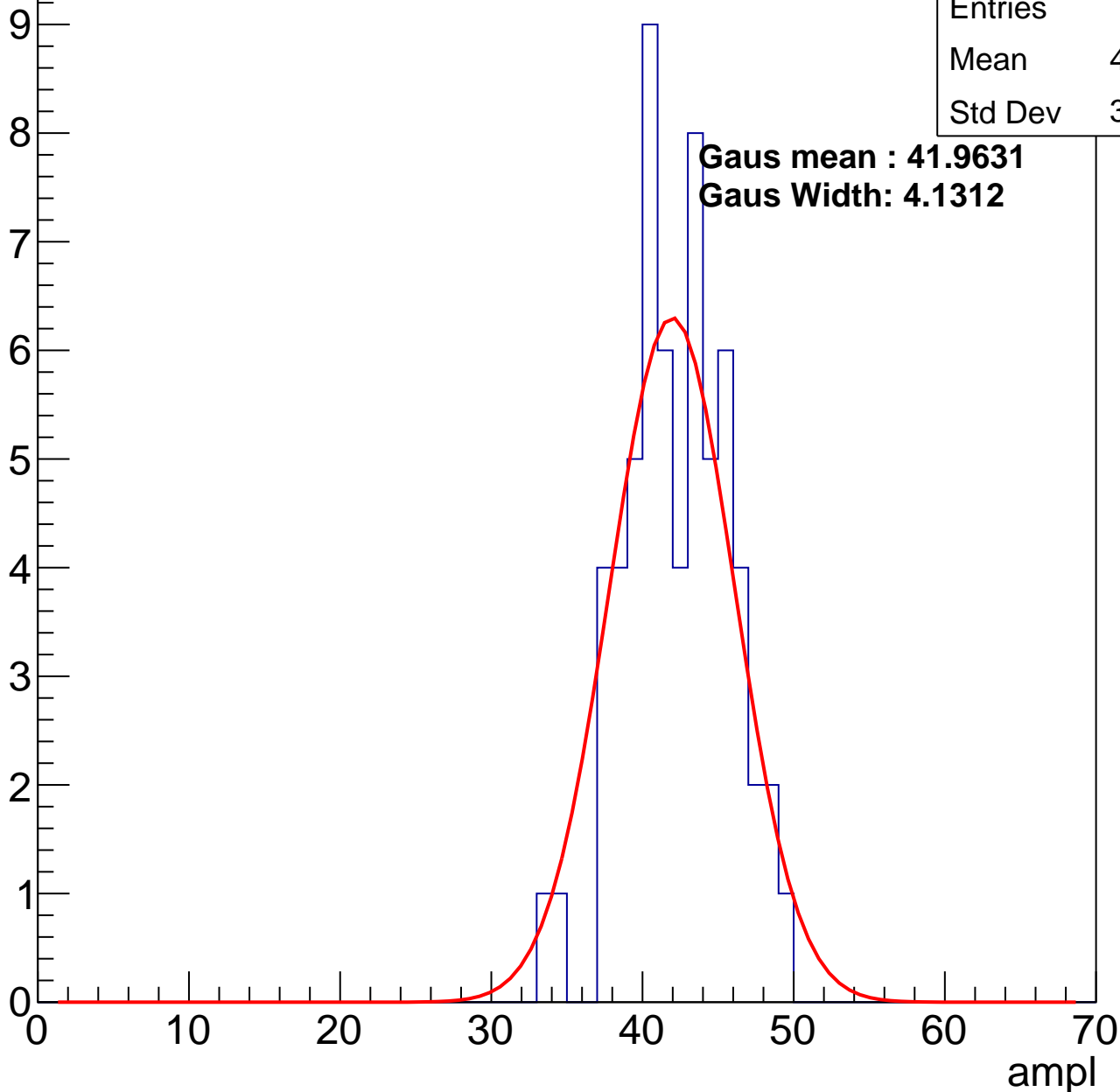
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	41.82
Std Dev	3.387

**Gaus mean : 41.9631**

**Gaus Width: 4.1312**

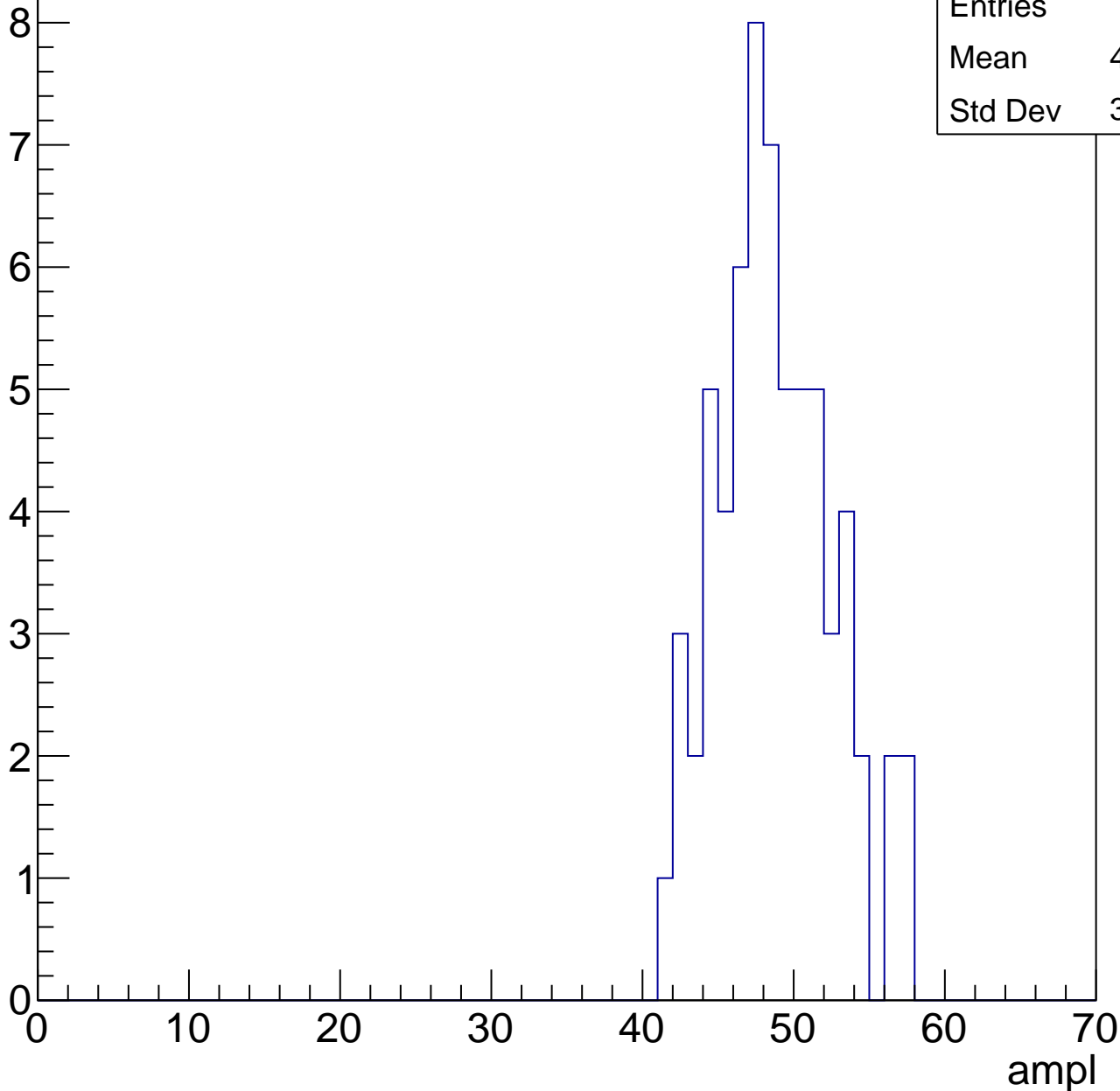


# B1L101S, U11-ch70, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	48.33
Std Dev	3.808

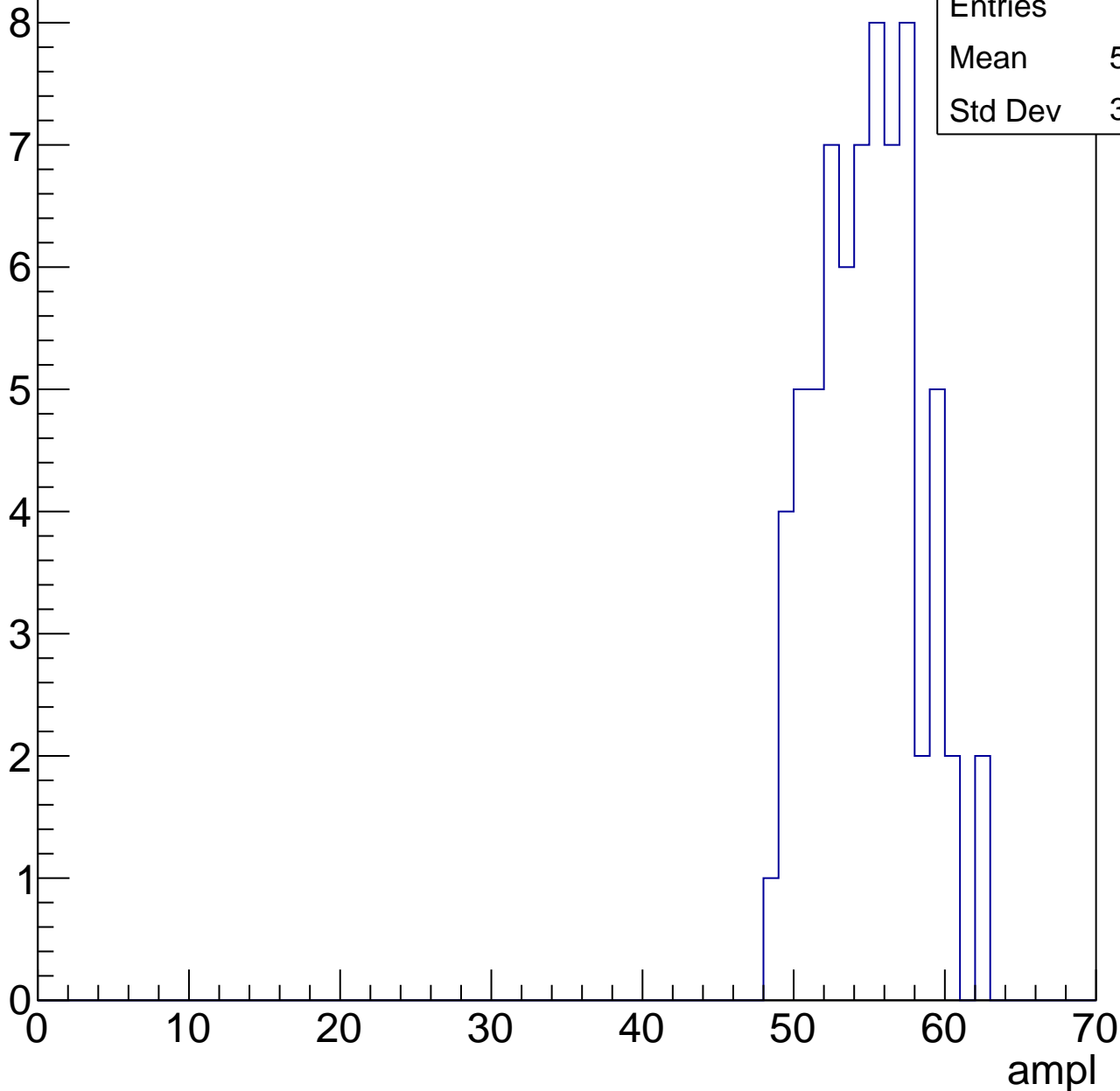


# B1L101S, U11-ch70, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

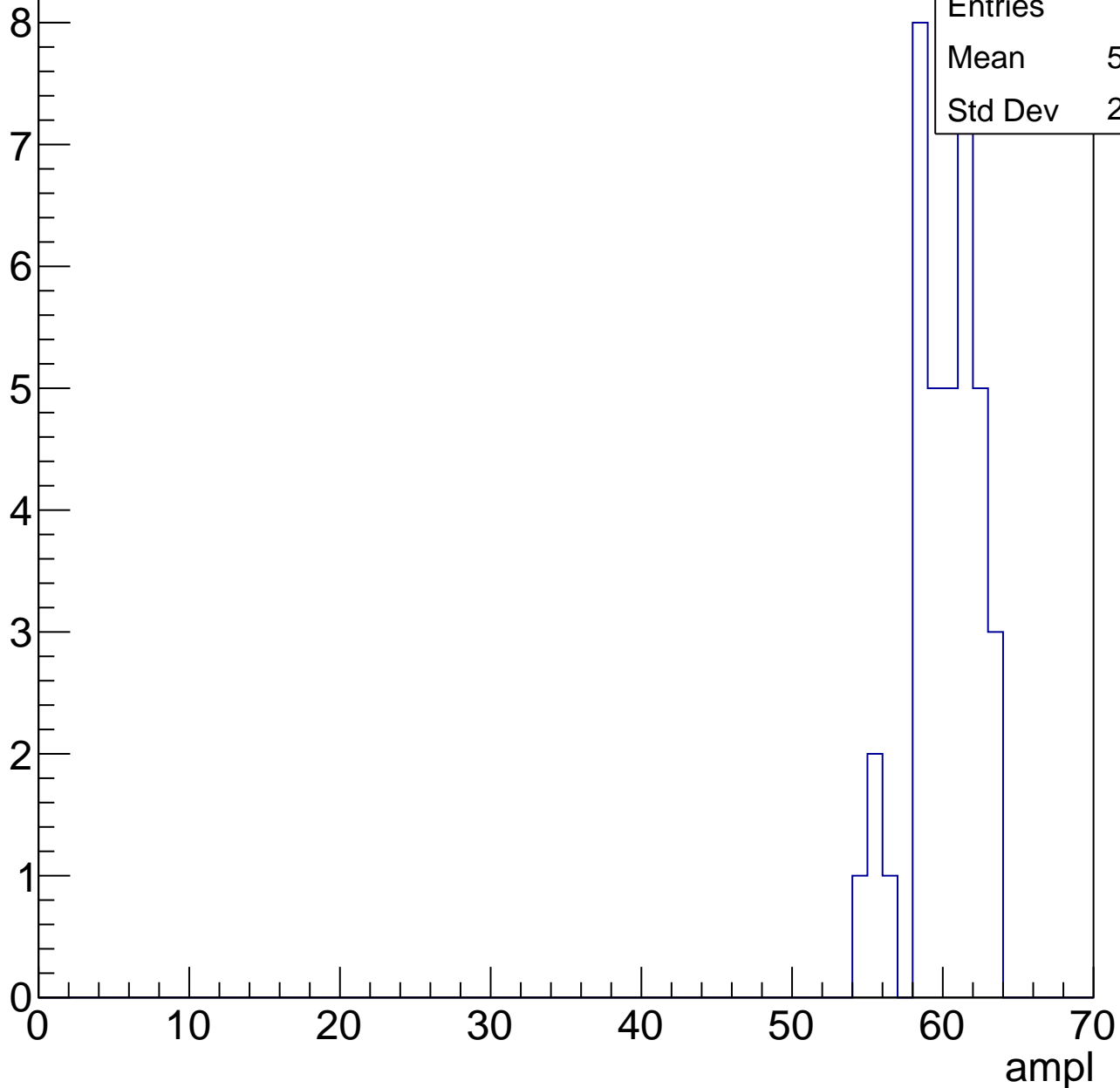
Entries	69
Mean	54.38
Std Dev	3.297



# B1L101S, U11-ch70, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

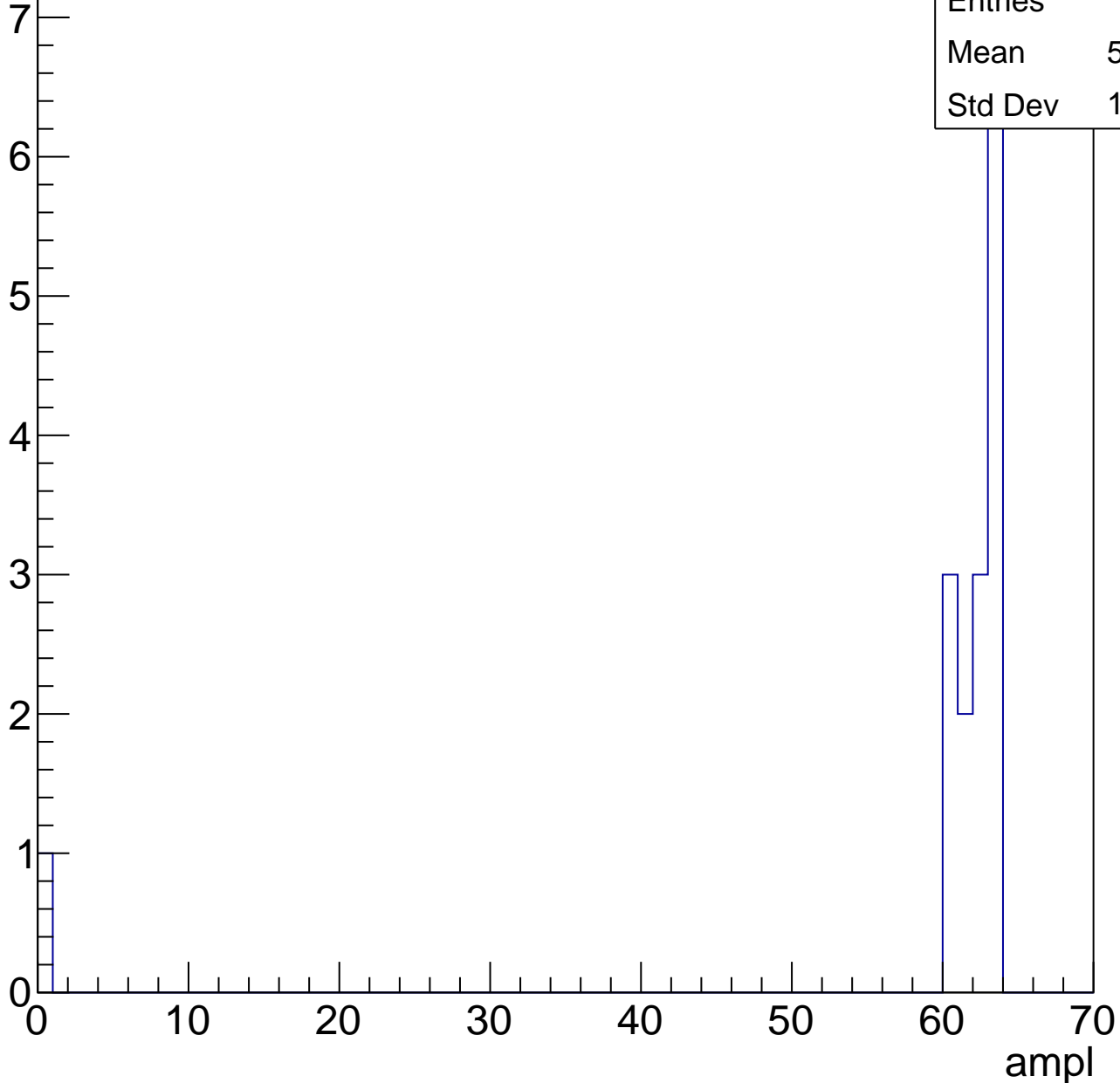


# B1L101S, U11-ch70, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	16
Mean	58.06
Std Dev	15.04





# B1L101S, U11-ch70, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U11-ch71, adc0

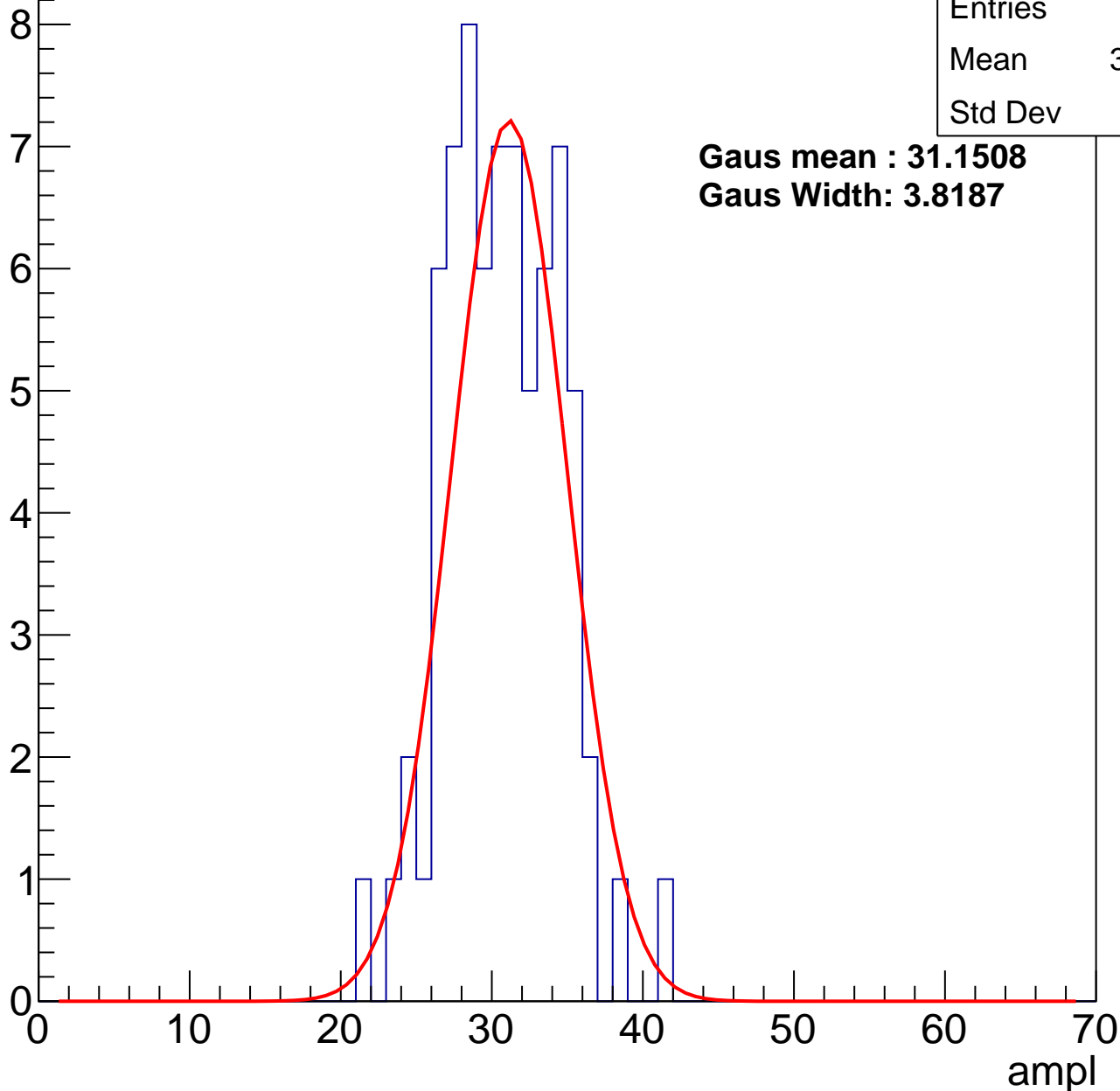
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	30.26
Std Dev	3.69

**Gaus mean : 31.1508**

**Gaus Width: 3.8187**



# B1L101S, U11-ch71, adc1

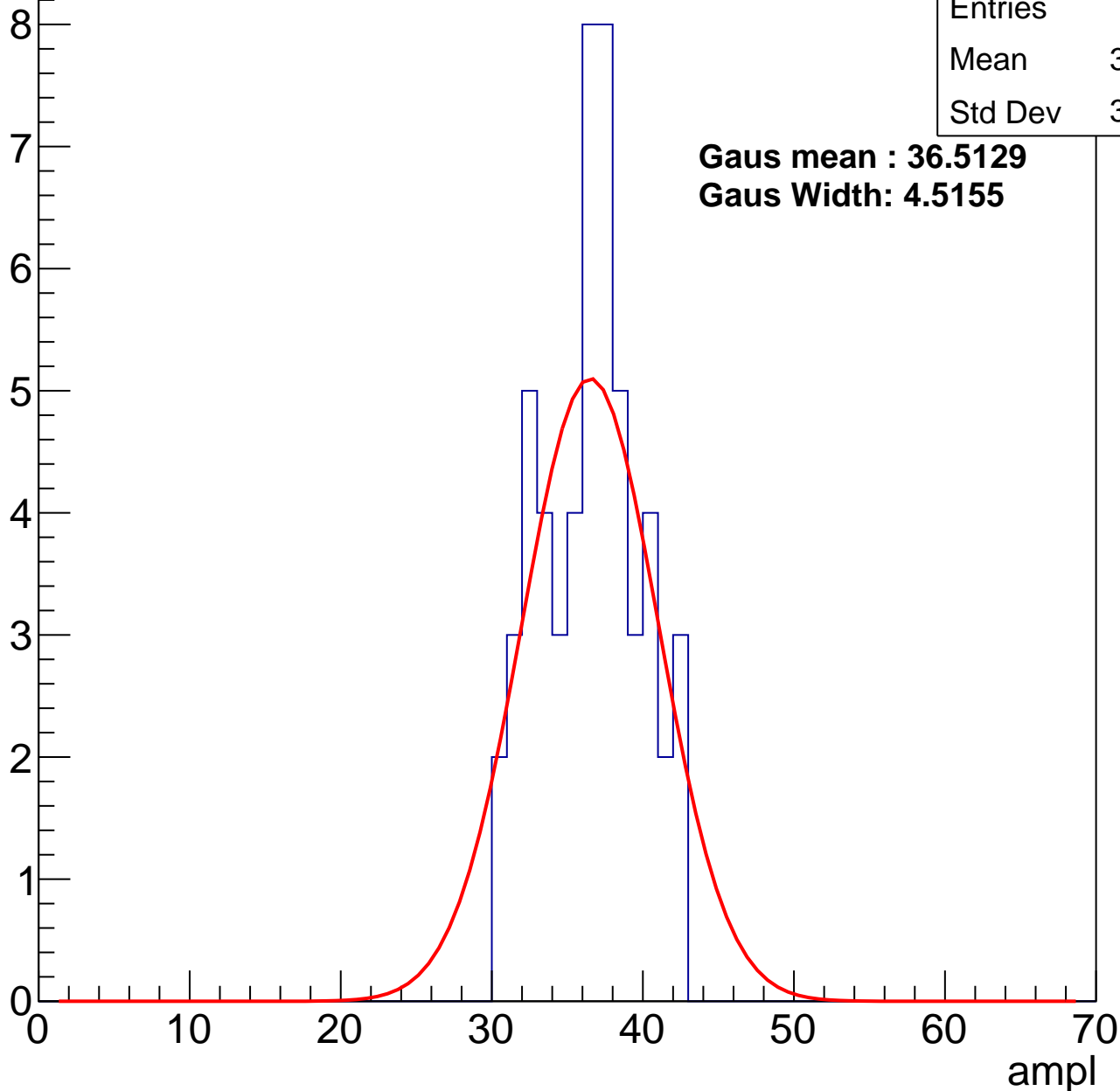
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	36.04
Std Dev	3.209

**Gaus mean : 36.5129**

**Gaus Width: 4.5155**



# B1L101S, U11-ch71, adc2

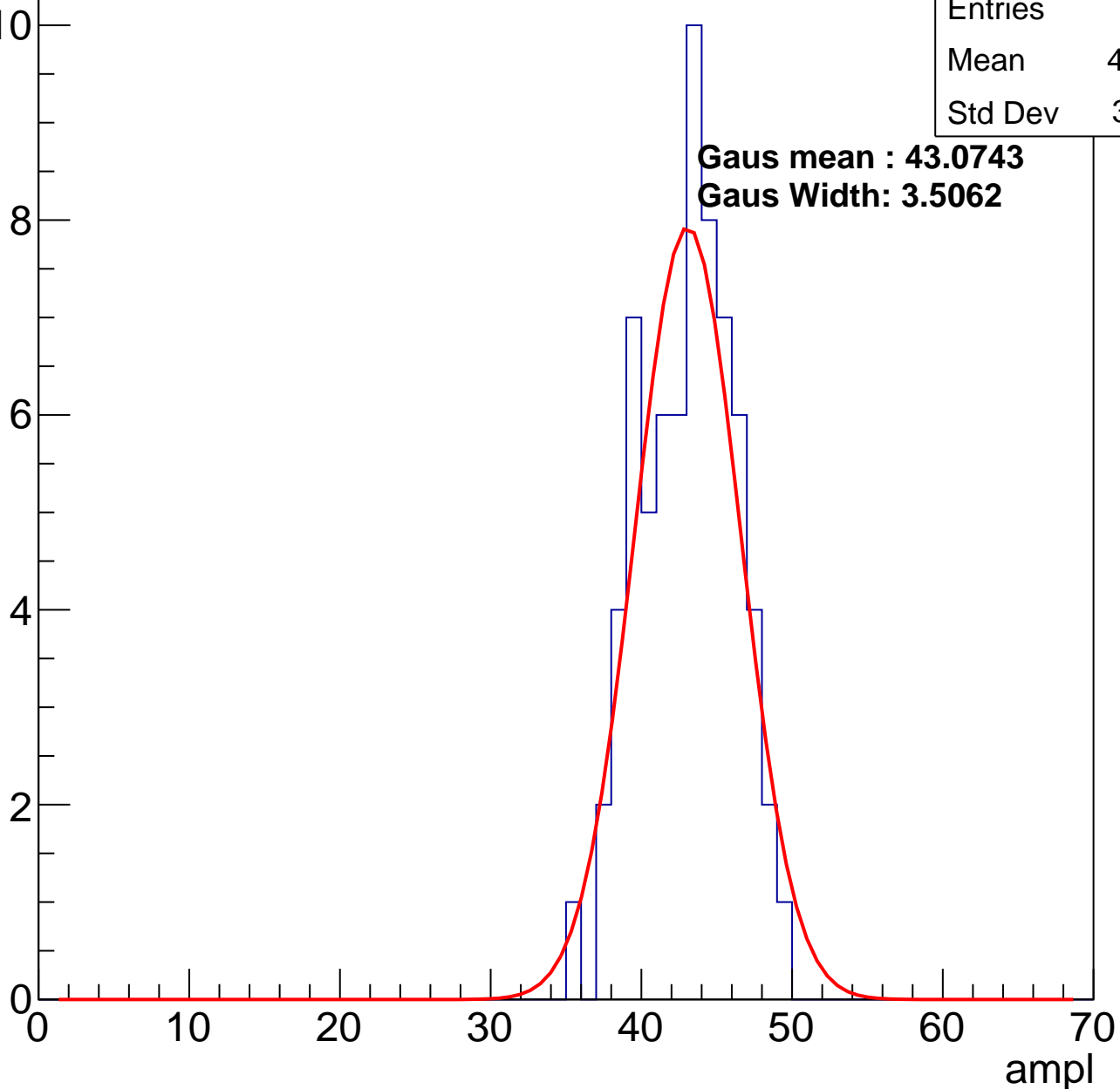
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	42.58
Std Dev	3.071

**Gaus mean : 43.0743**

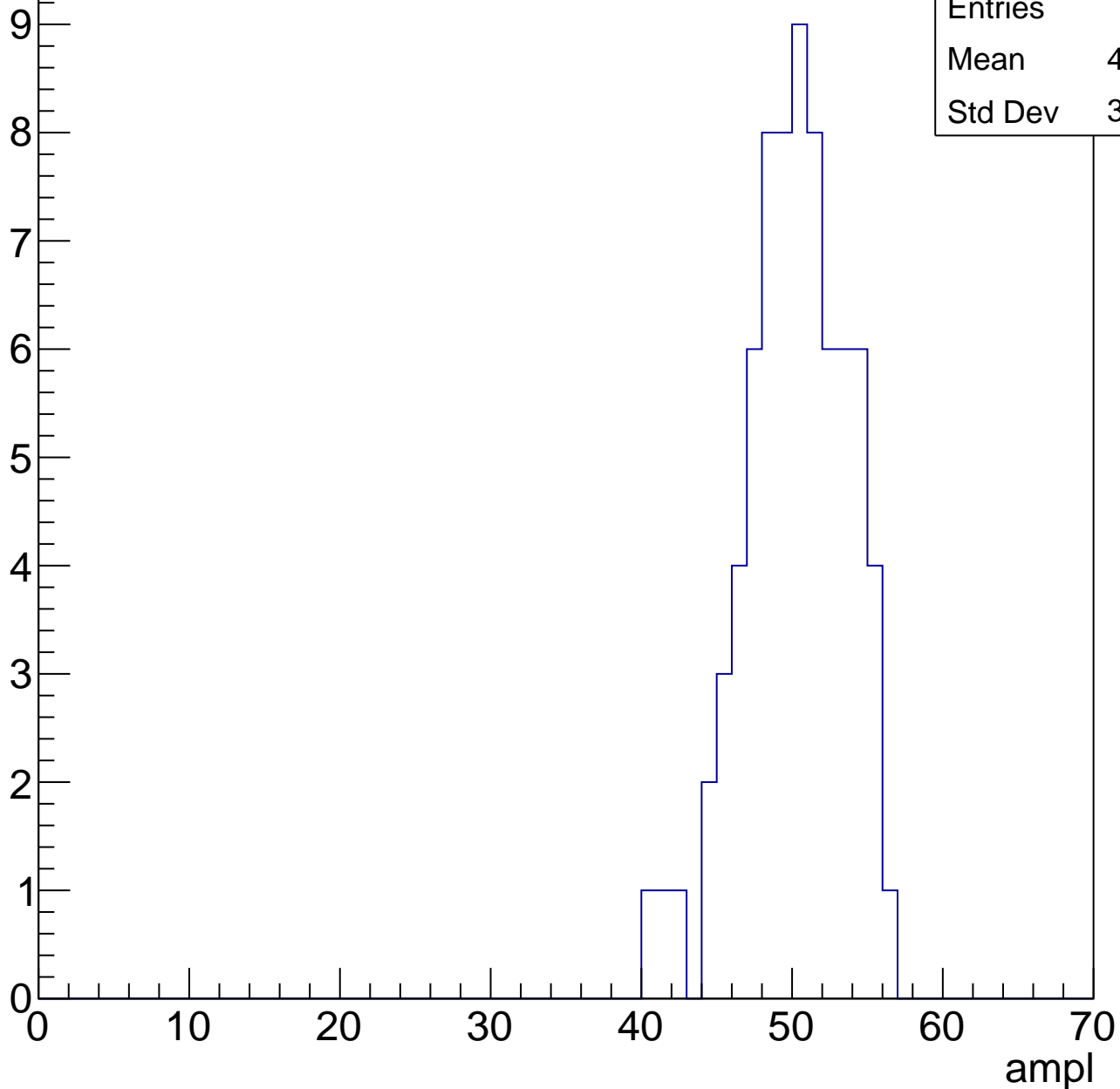
**Gaus Width: 3.5062**



# B1L101S, U11-ch71, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

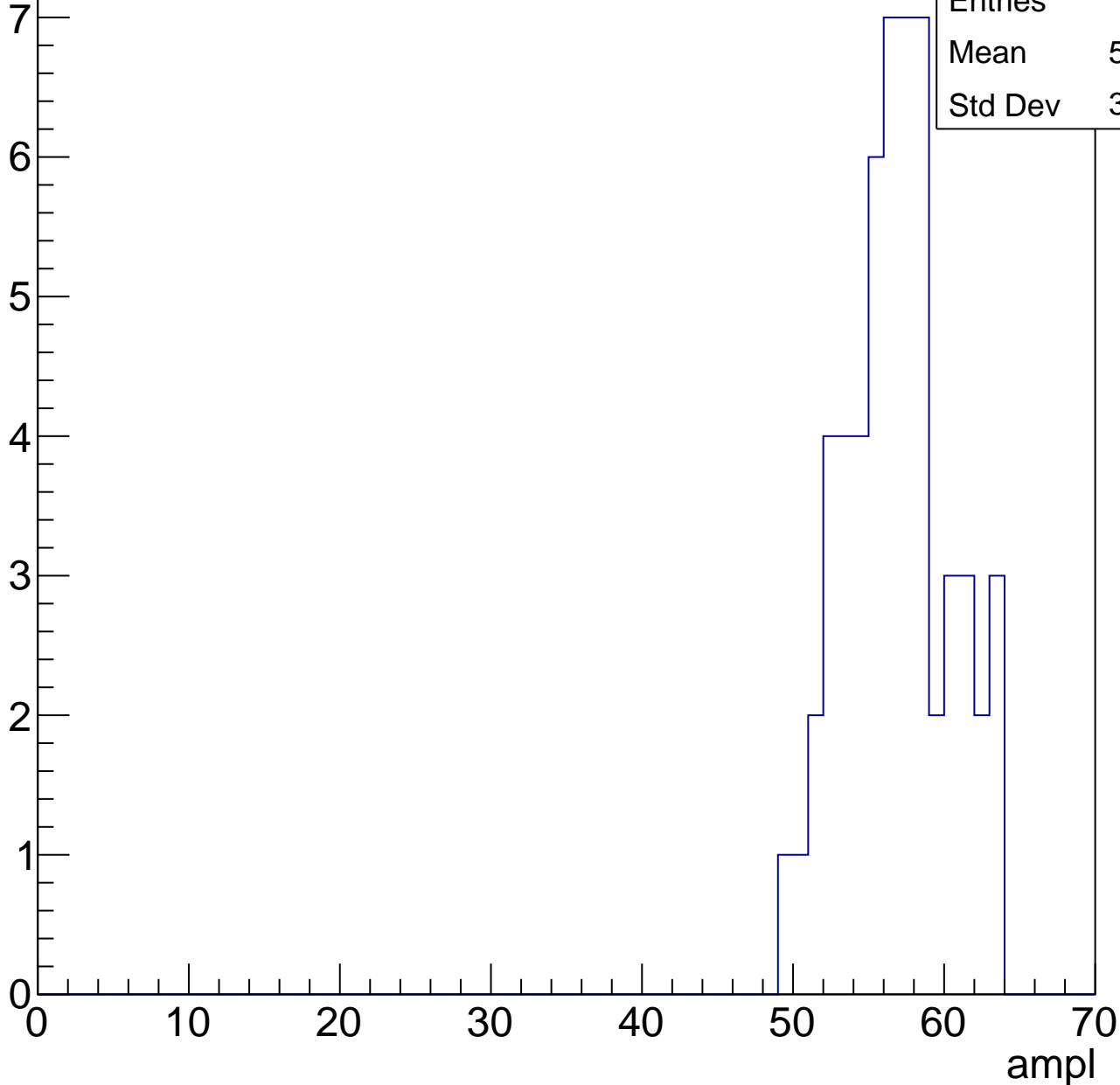


# B1L101S, U11-ch71, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

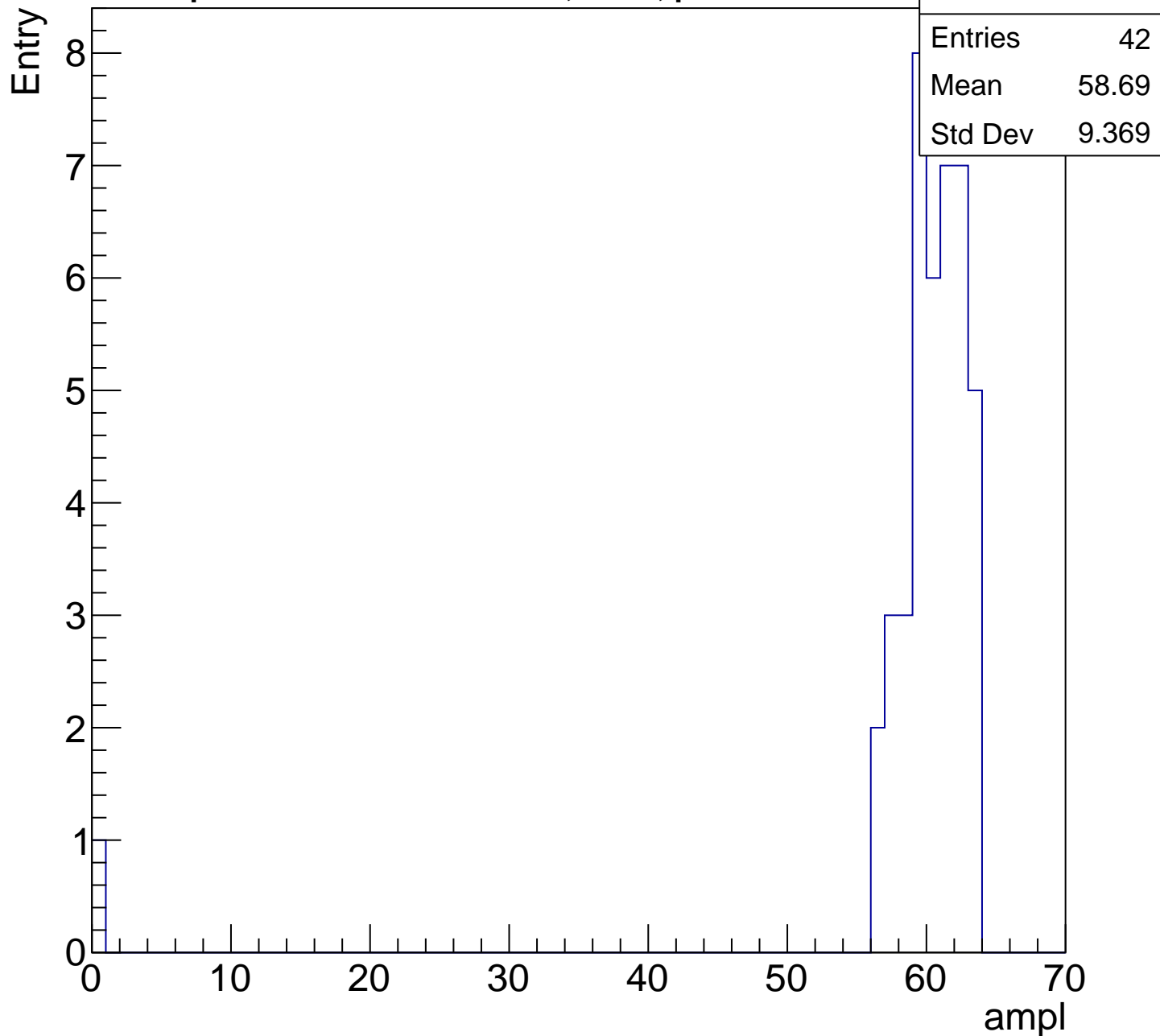
Entry

Entries	56
Mean	56.39
Std Dev	3.389



# B1L101S, U11-ch71, adc5

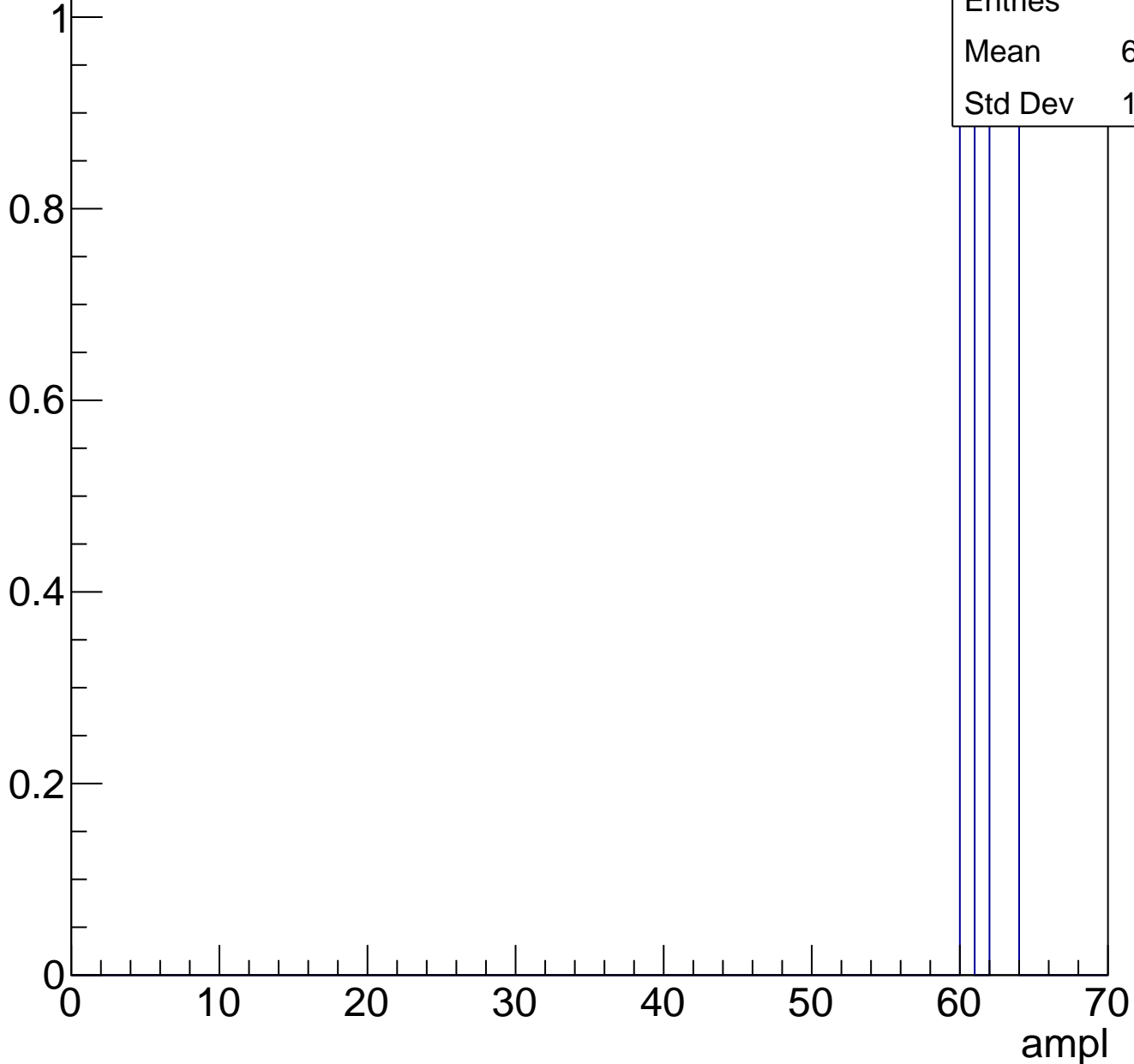
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U11-ch71, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch71, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	21
Std Dev	29.7

# B1L101S, U11-ch72, adc0

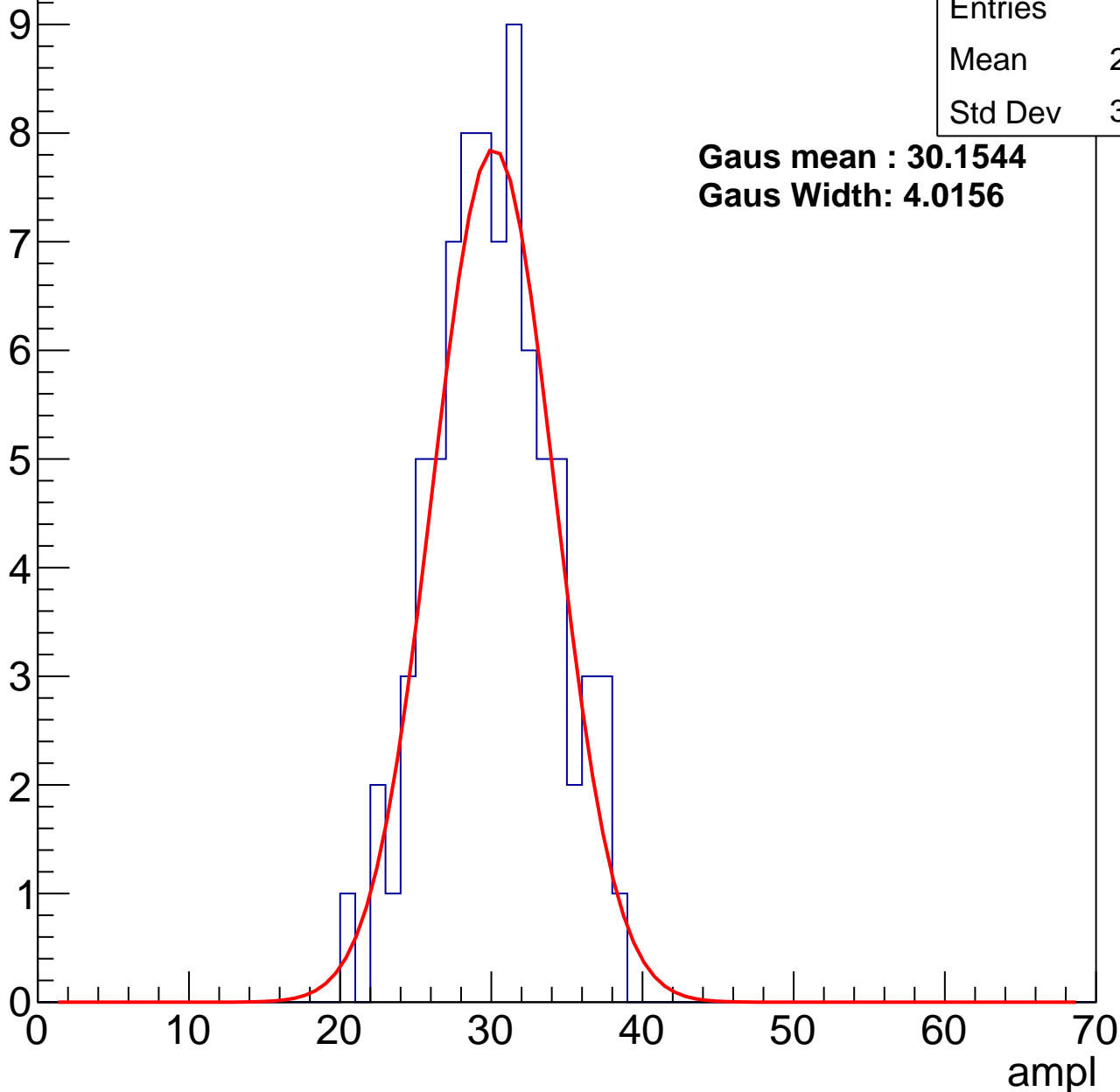
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	81
Mean	29.65
Std Dev	3.866

**Gaus mean : 30.1544**

**Gaus Width: 4.0156**



# B1L101S, U11-ch72, adc1

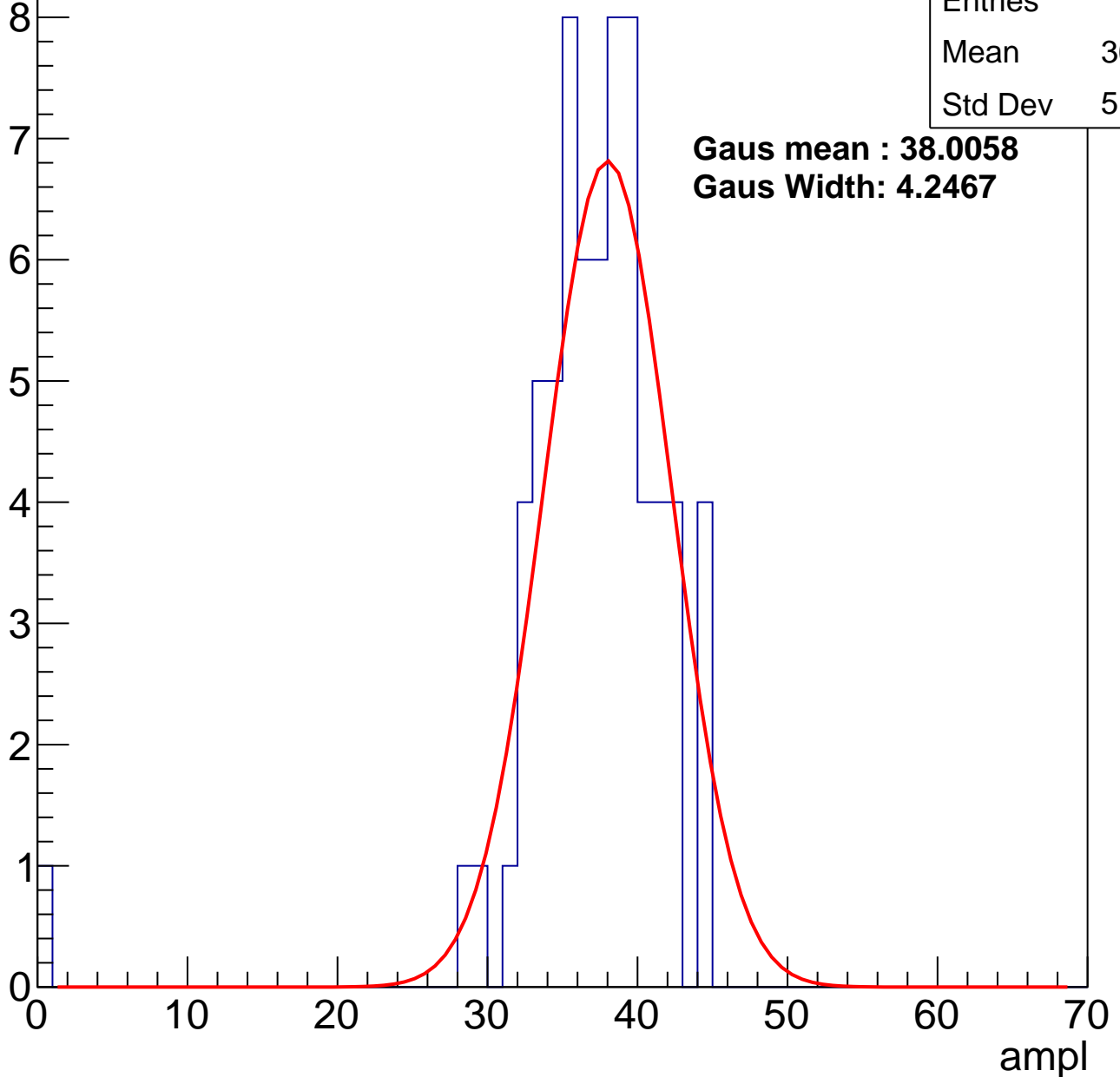
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	36.47
Std Dev	5.644

**Gaus mean : 38.0058**

**Gaus Width: 4.2467**



# B1L101S, U11-ch72, adc2

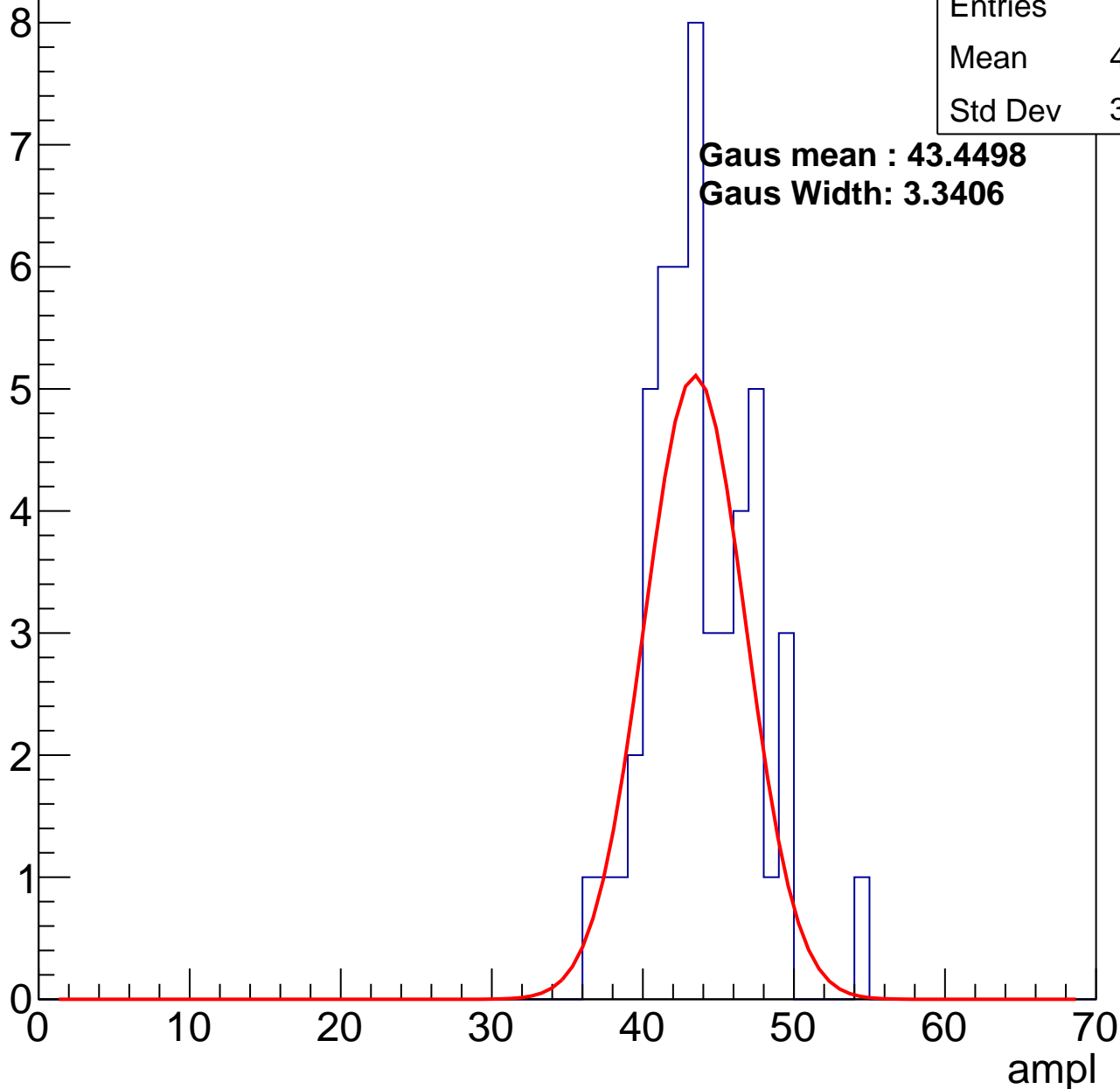
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	43.32
Std Dev	3.455

**Gaus mean : 43.4498**

**Gaus Width: 3.3406**

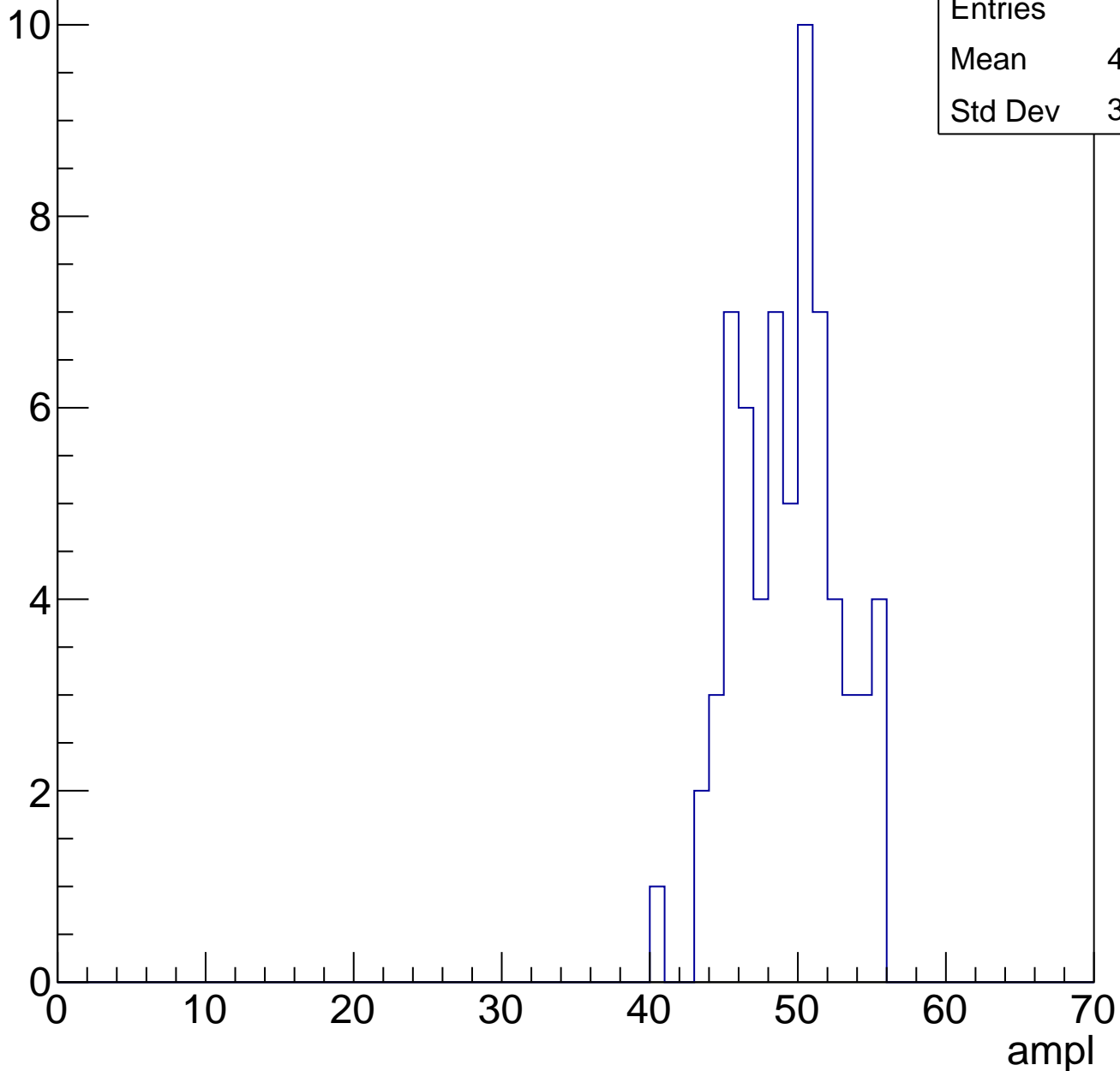


# B1L101S, U11-ch72, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	48.85
Std Dev	3.386

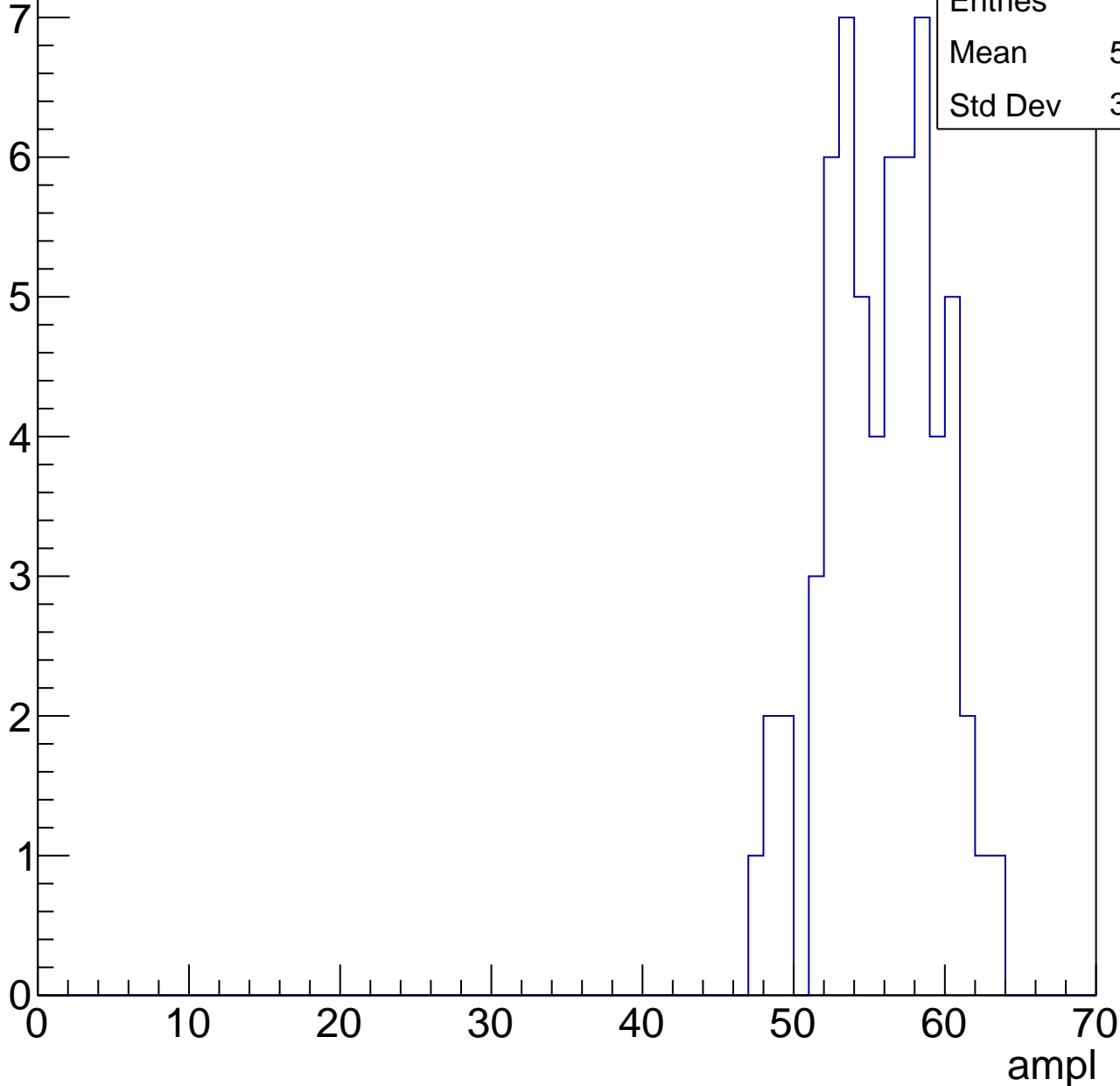


# B1L101S, U11-ch72, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

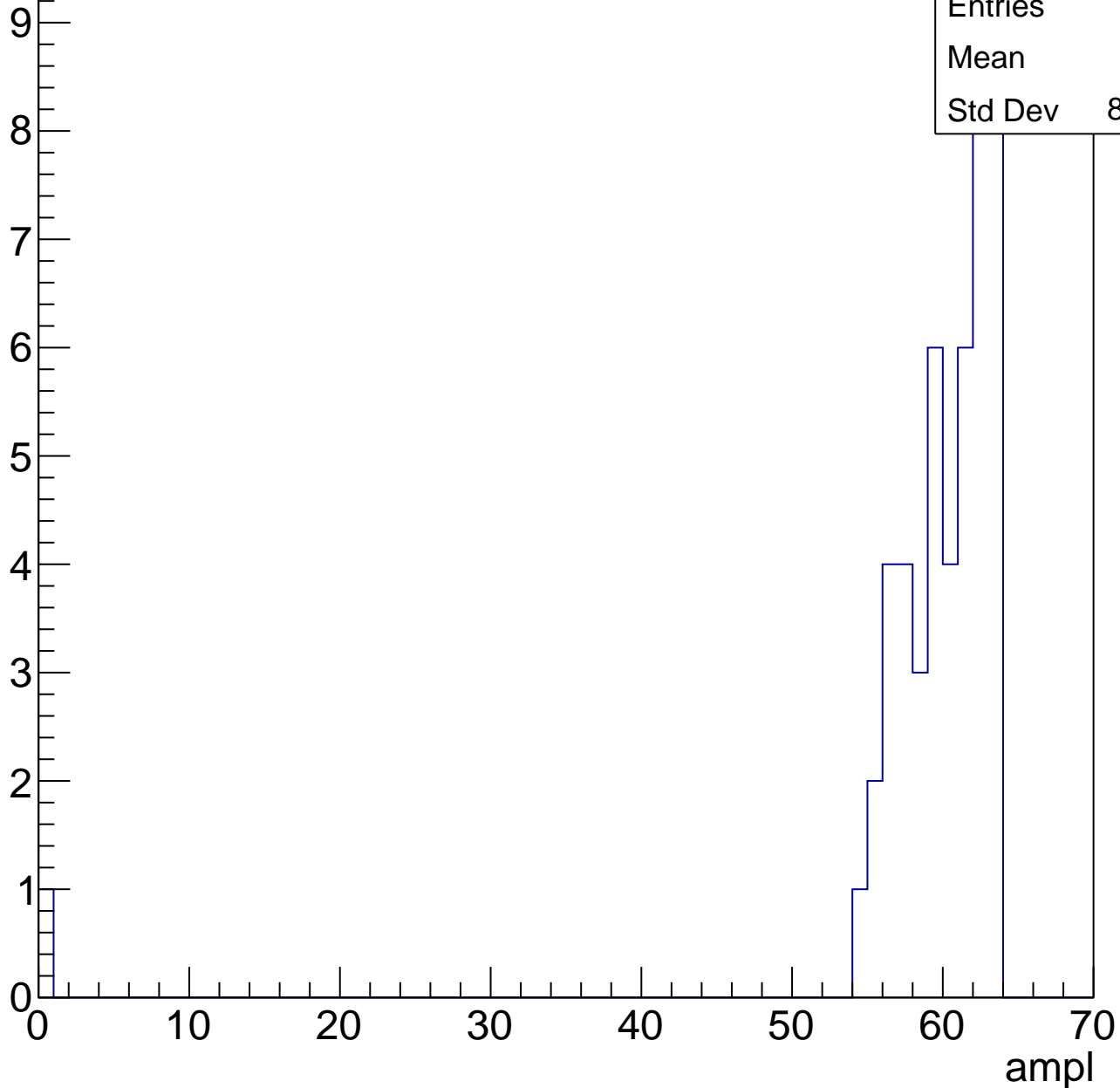
Entries	62
Mean	55.39
Std Dev	3.652



# B1L101S, U11-ch72, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

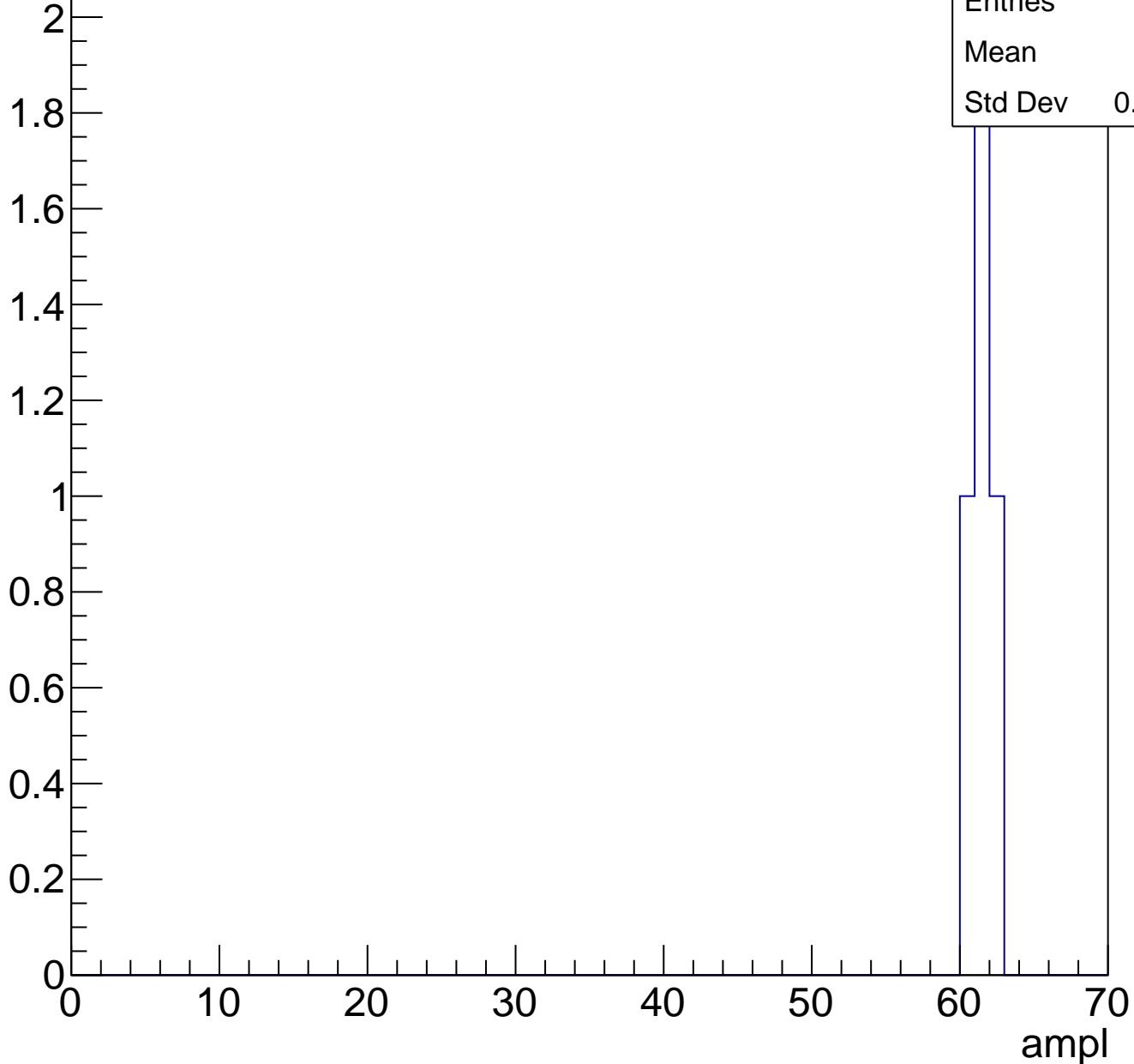
Entry



# B1L101S, U11-ch72, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	4
Mean	61
Std Dev	0.7071



# B1L101S, U11-ch72, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U11-ch73, adc0

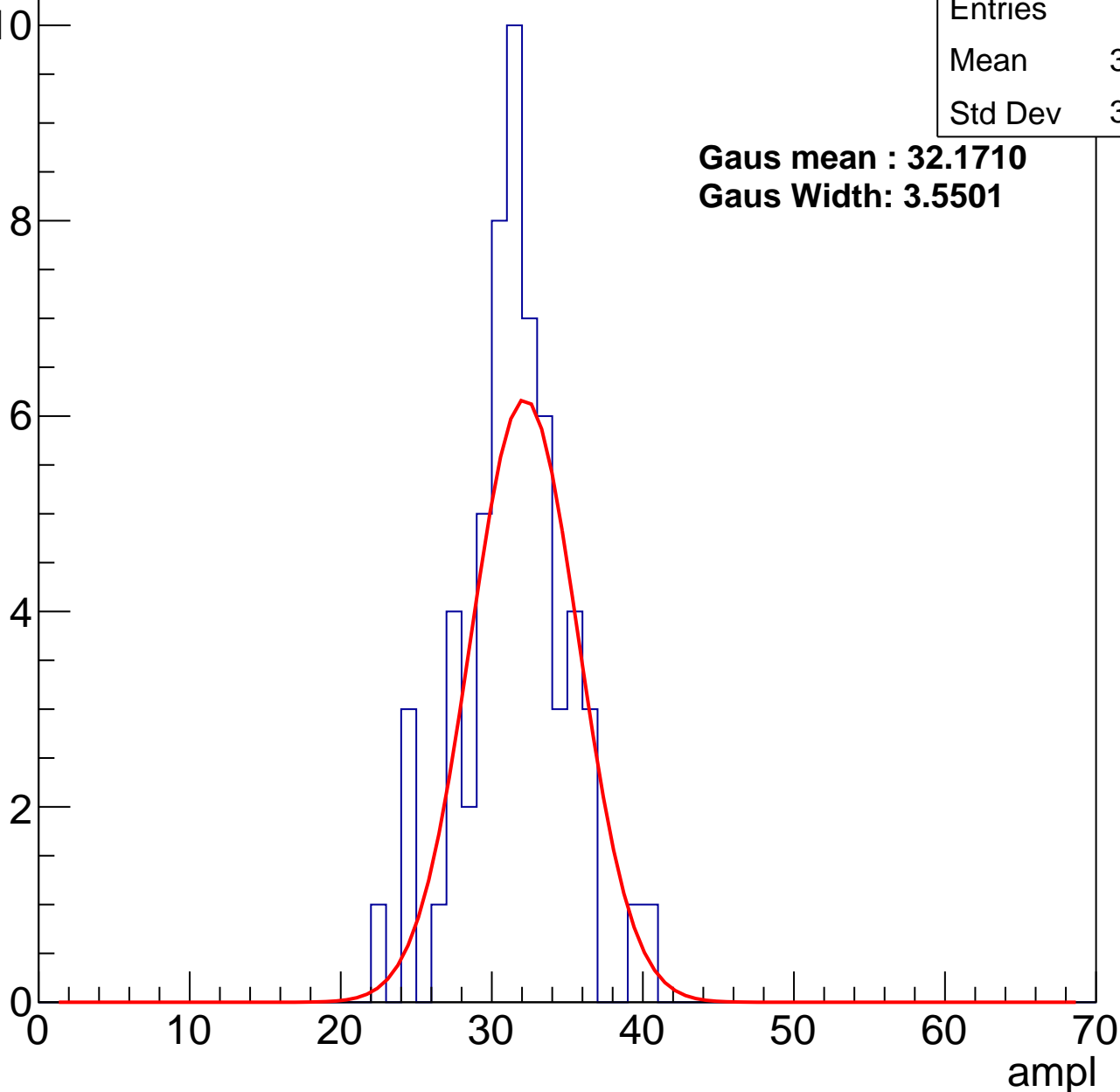
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	31.02
Std Dev	3.457

**Gaus mean : 32.1710**

**Gaus Width: 3.5501**



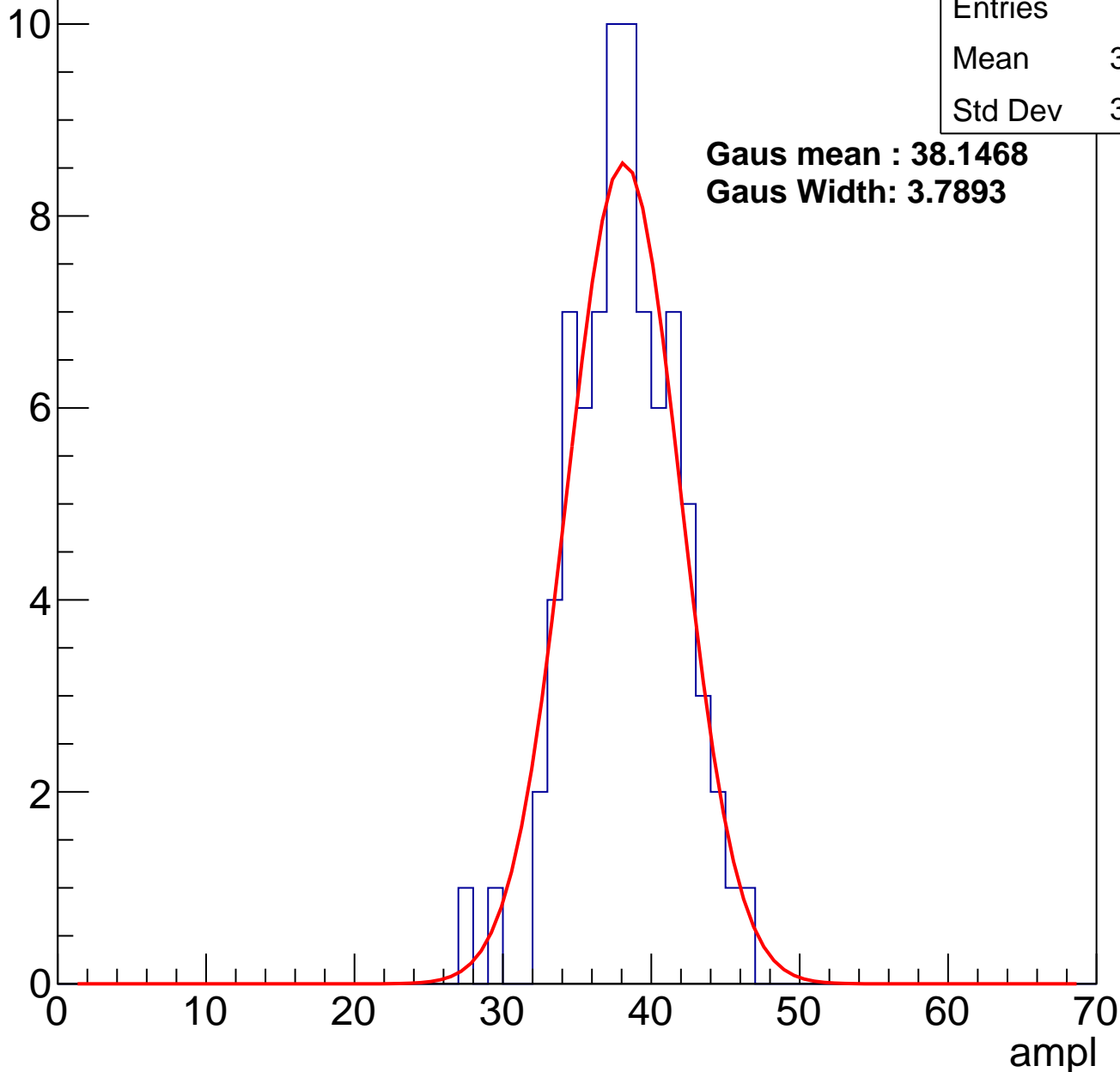
# B1L101S, U11-ch73, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	80
Mean	37.75
Std Dev	3.548

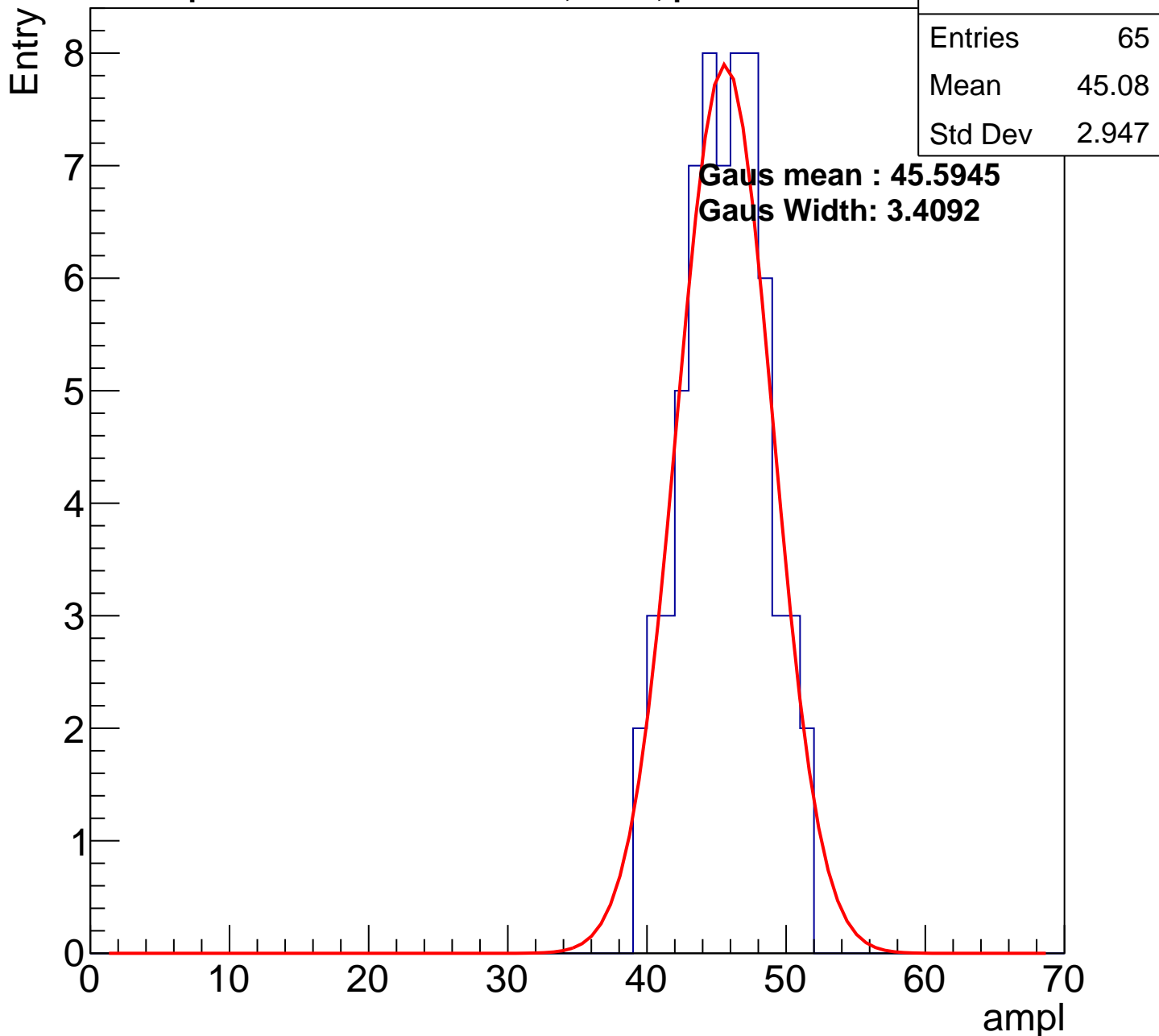
**Gaus mean : 38.1468**  
**Gaus Width: 3.7893**

Entry



# B1L101S, U11-ch73, adc2

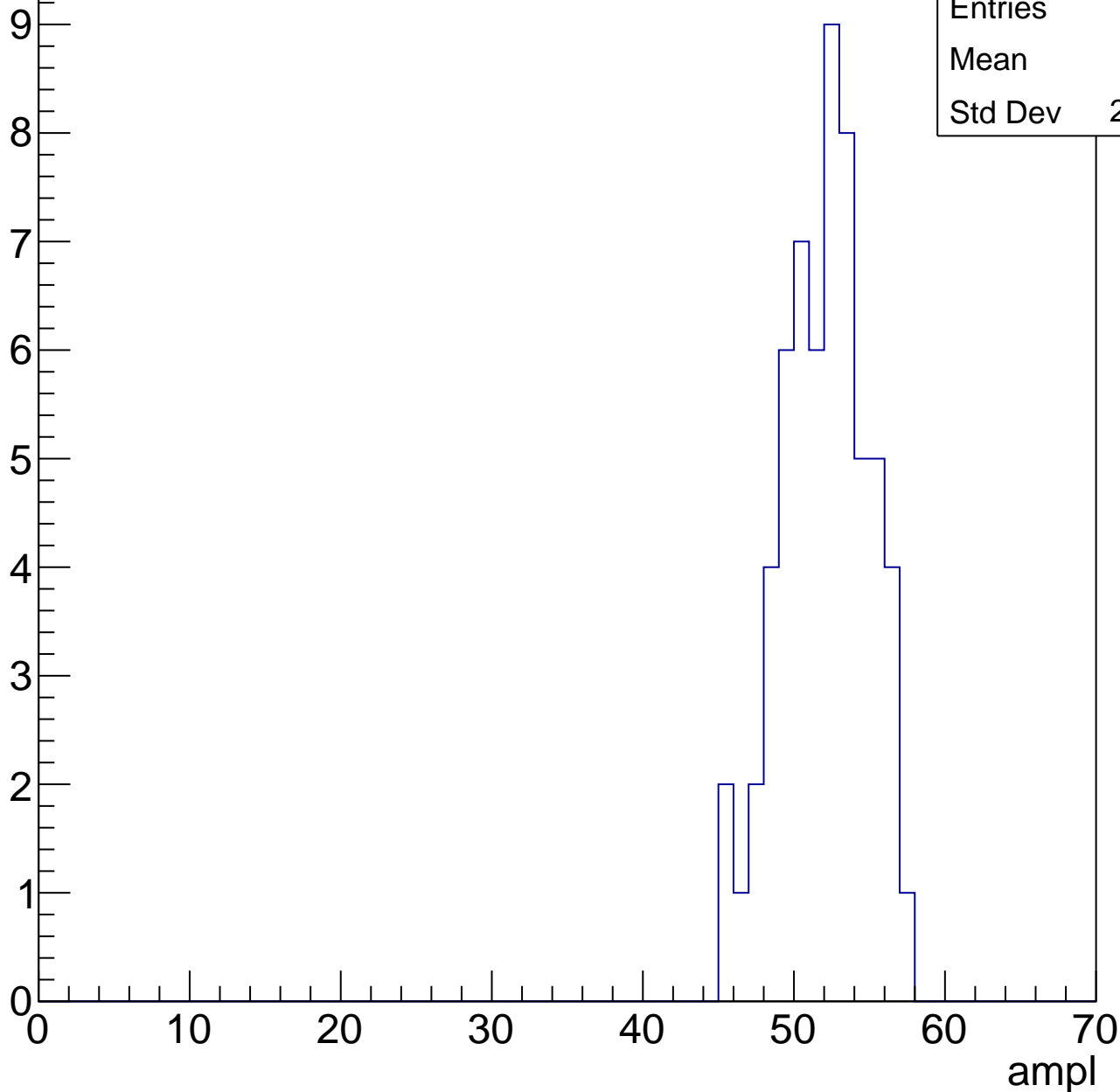
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U11-ch73, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

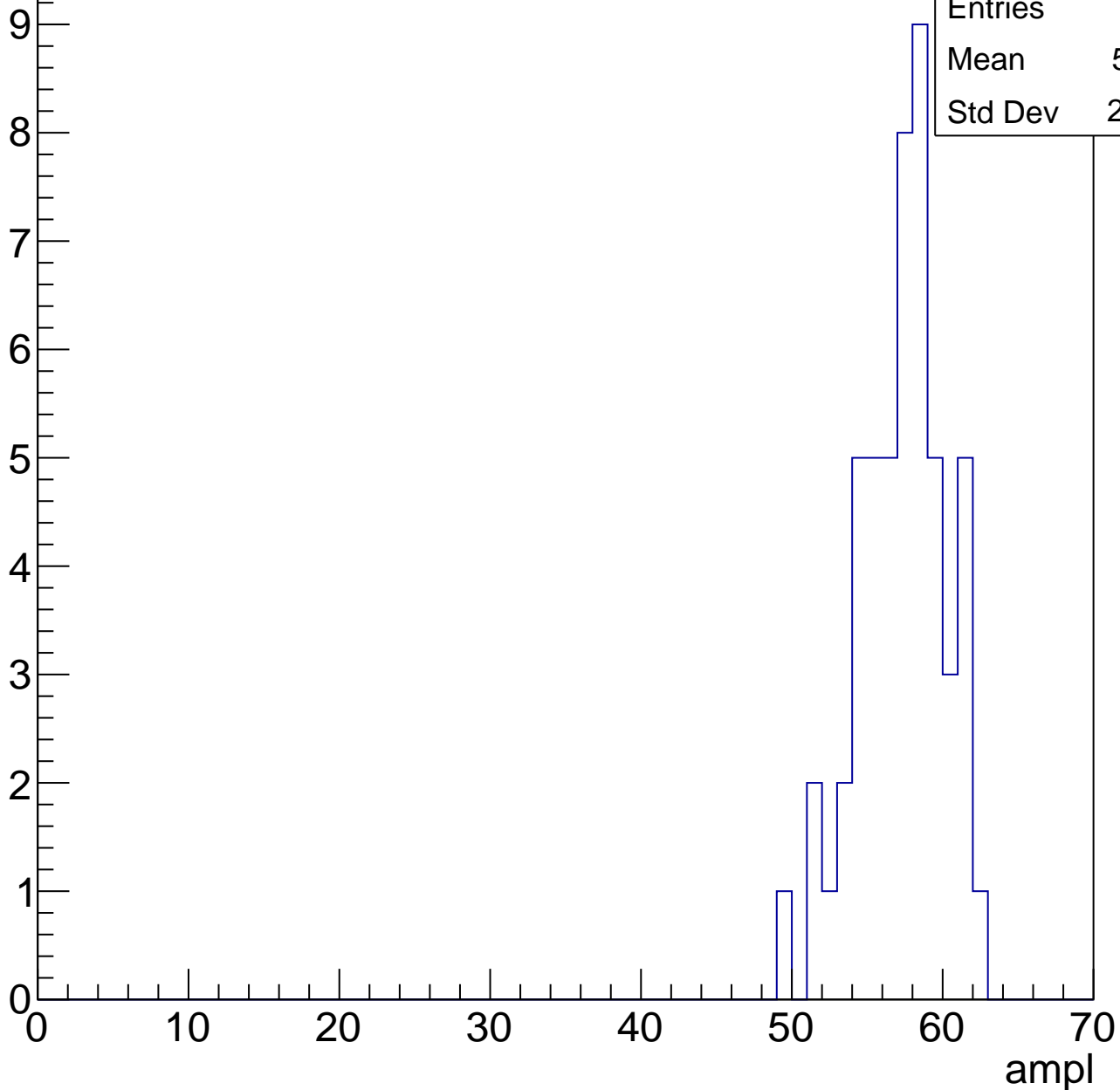


# B1L101S, U11-ch73, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

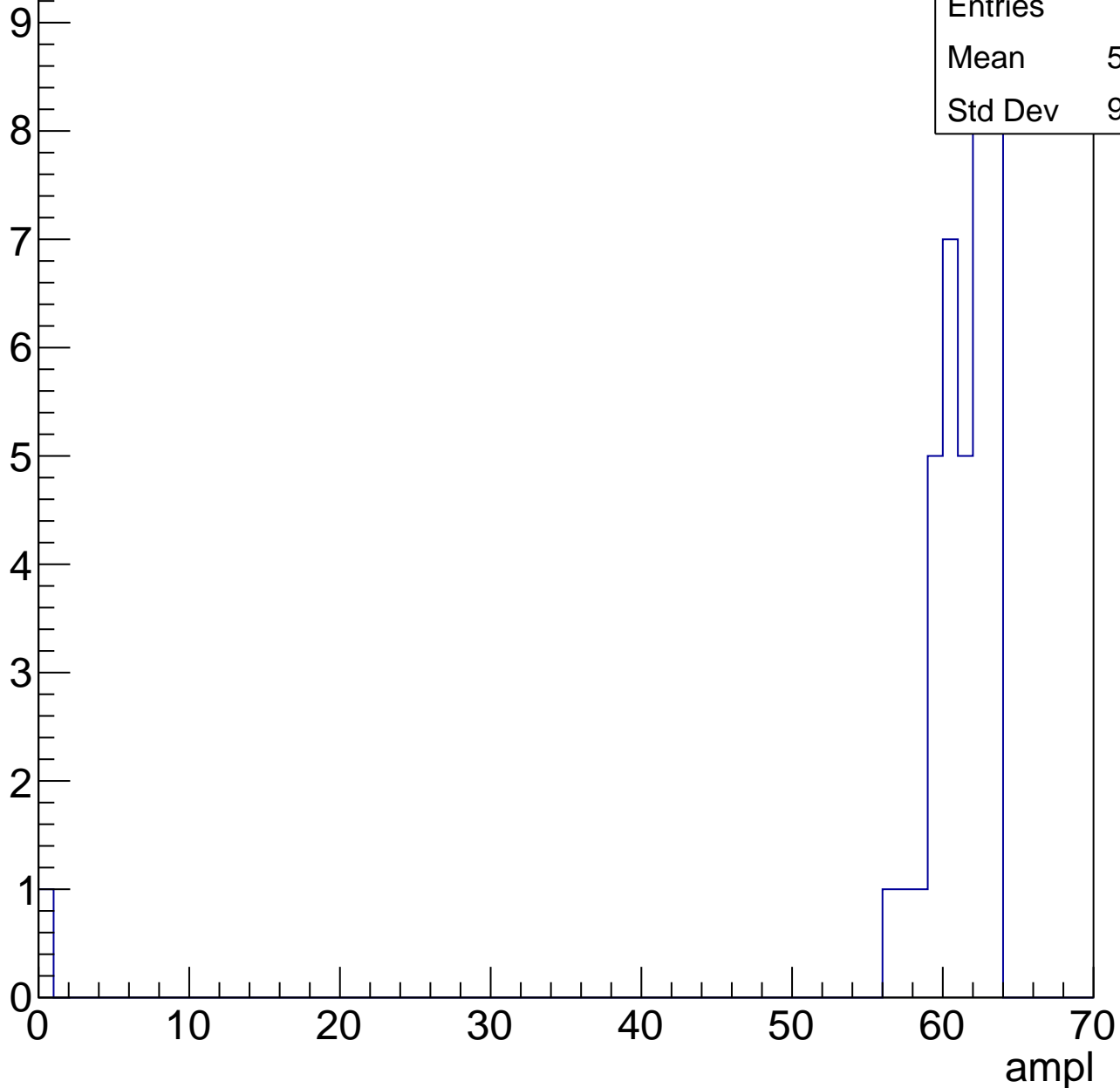
Entries	52
Mean	56.81
Std Dev	2.849



# B1L101S, U11-ch73, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U11-ch73, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch73, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U11-ch74, adc0

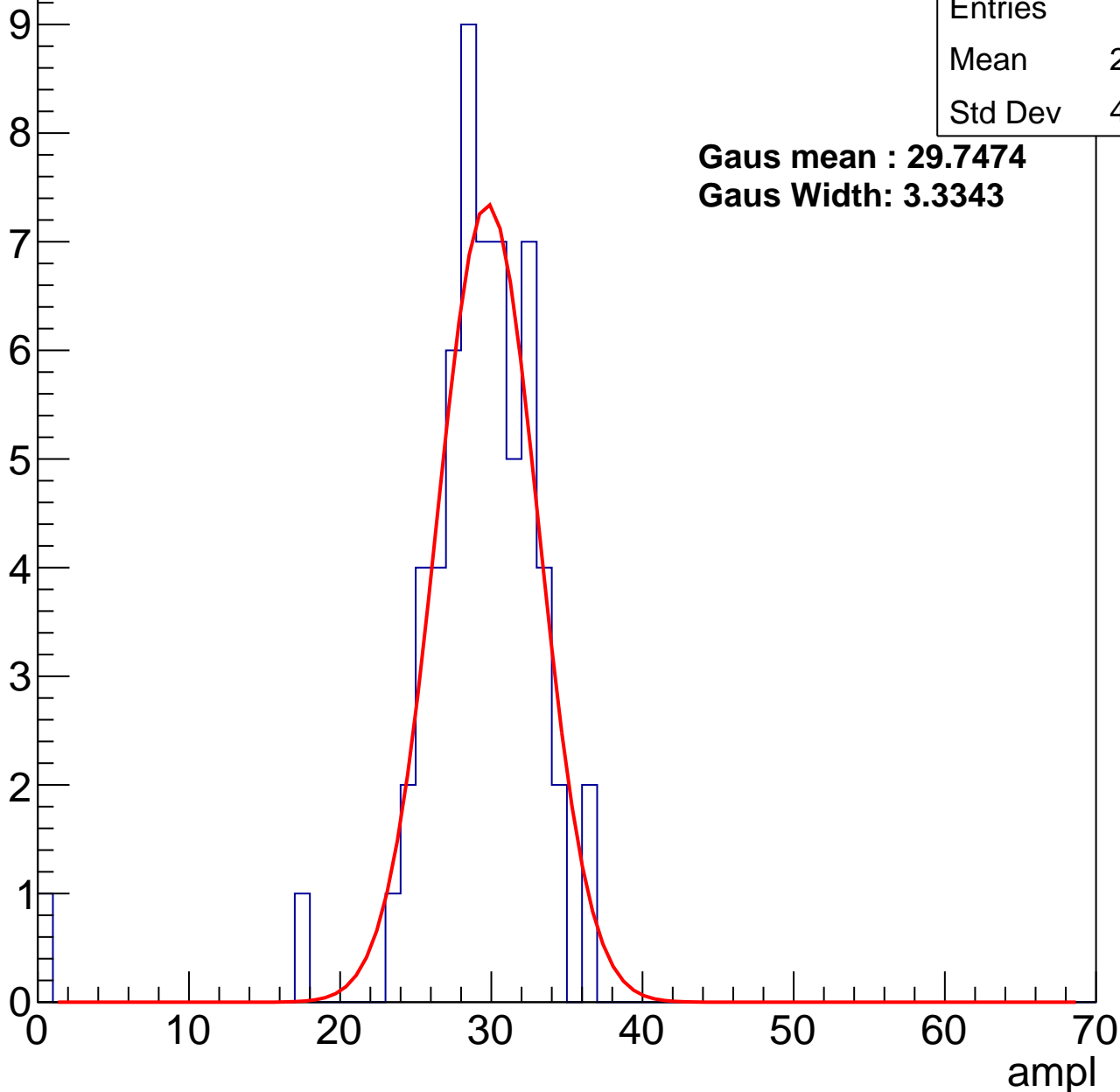
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	28.55
Std Dev	4.908

**Gaus mean : 29.7474**

**Gaus Width: 3.3343**



# B1L101S, U11-ch74, adc1

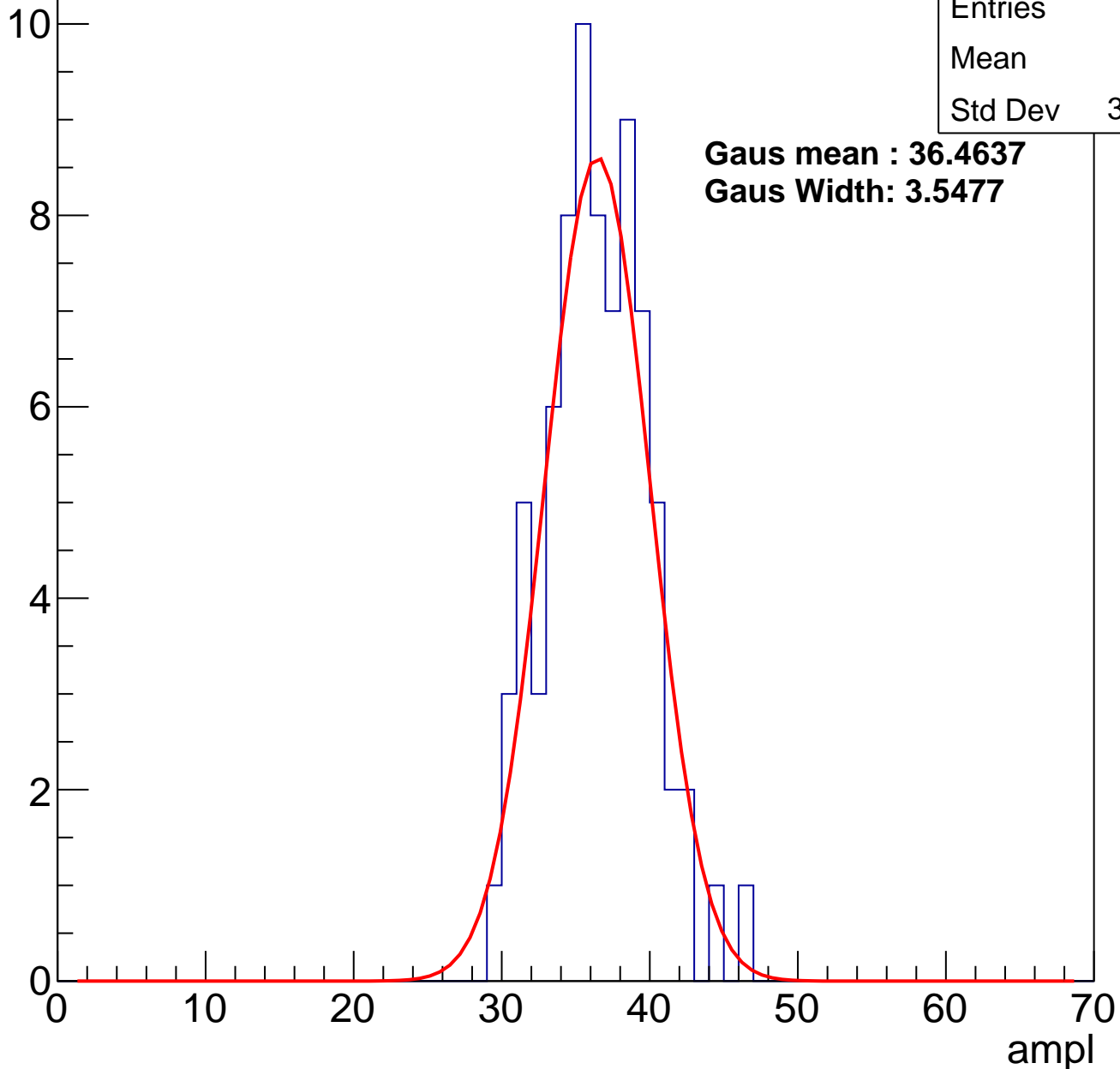
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	78
Mean	36
Std Dev	3.393

**Gaus mean : 36.4637**

**Gaus Width: 3.5477**

Entry



# B1L101S, U11-ch74, adc2

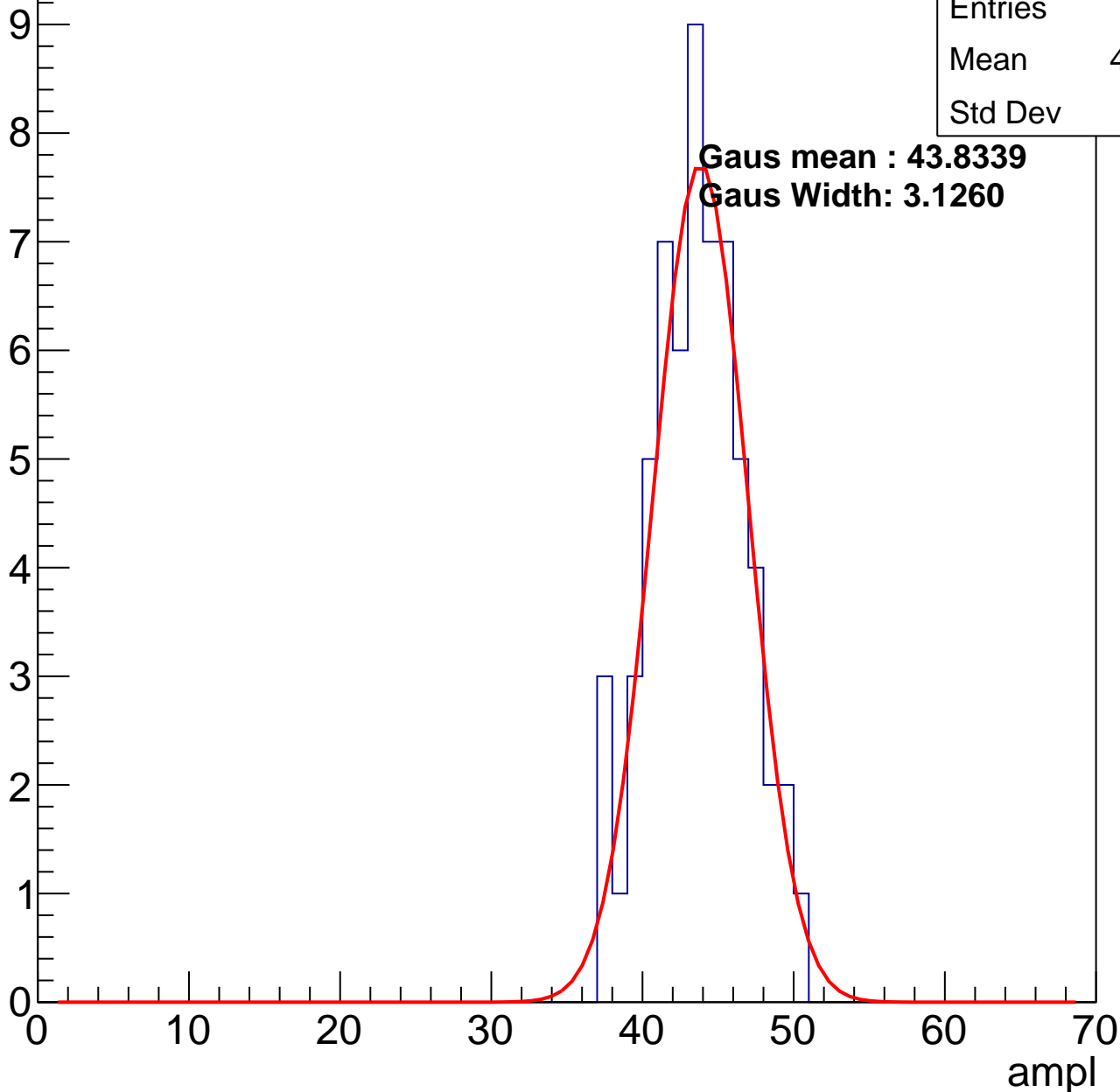
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	43.18
Std Dev	3.04

**Gaus mean : 43.8339**

**Gaus Width: 3.1260**

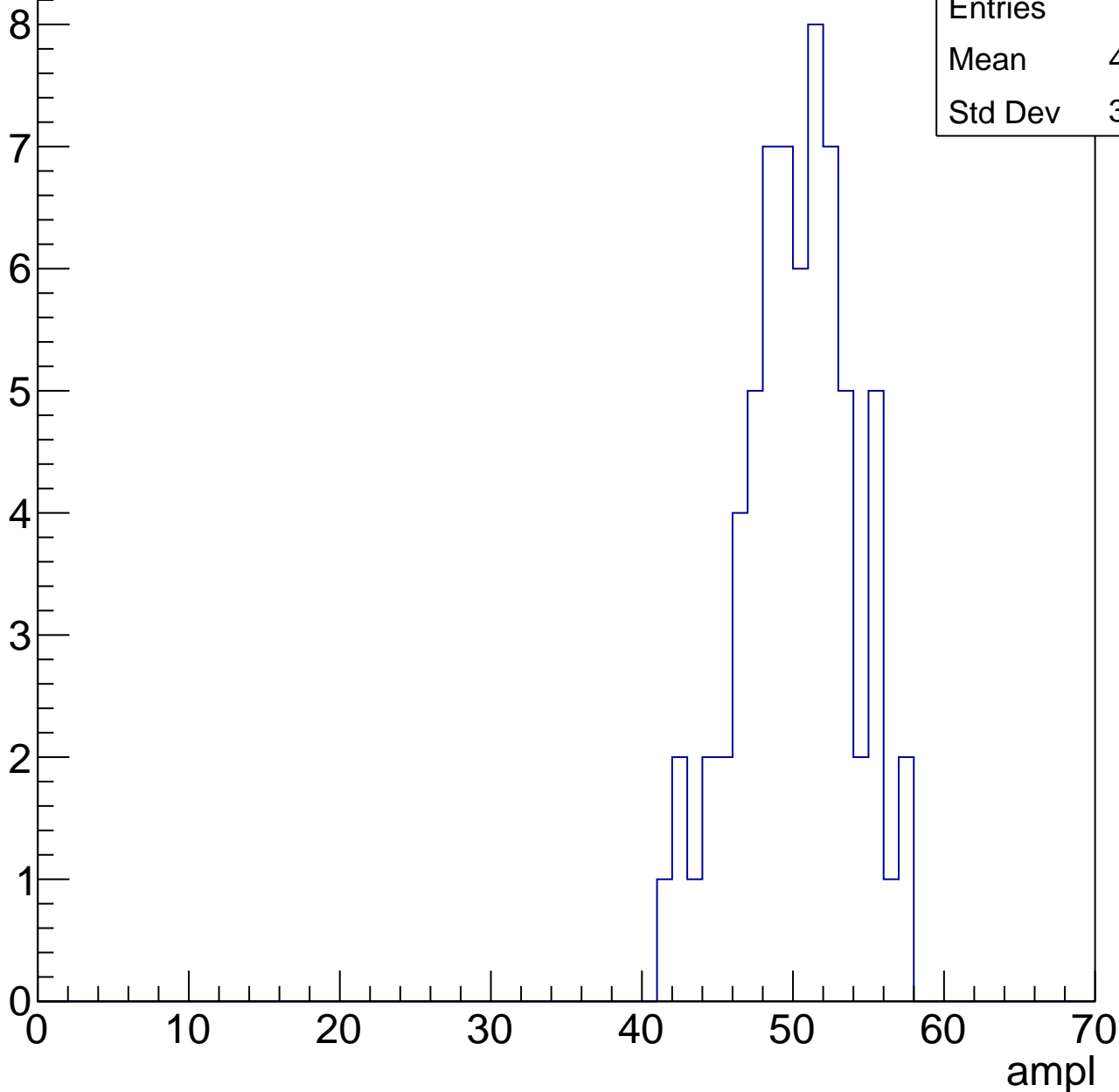


# B1L101S, U11-ch74, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	49.76
Std Dev	3.649

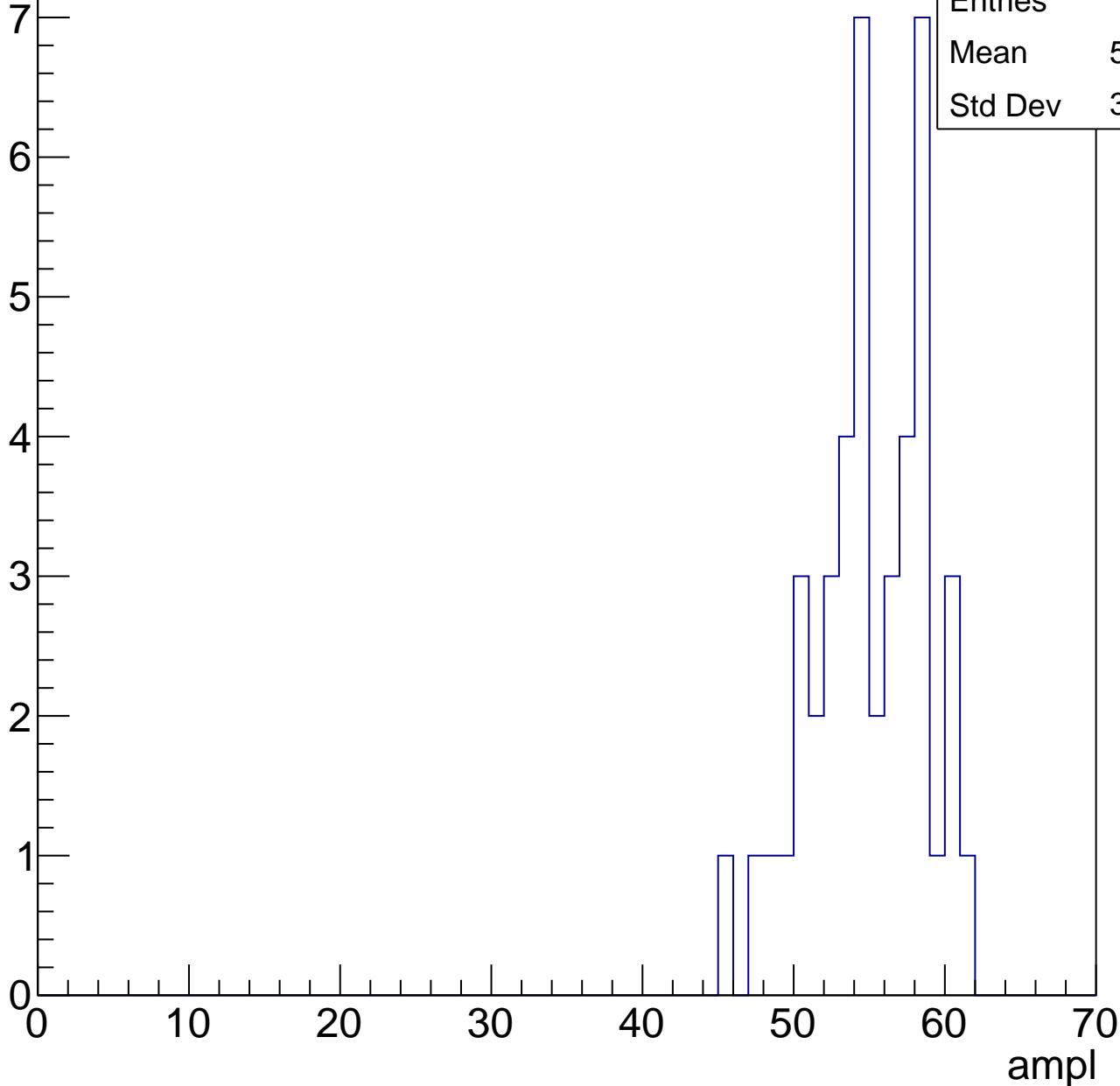


# B1L101S, U11-ch74, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	44
Mean	54.52
Std Dev	3.708



# B1L101S, U11-ch74, adc5

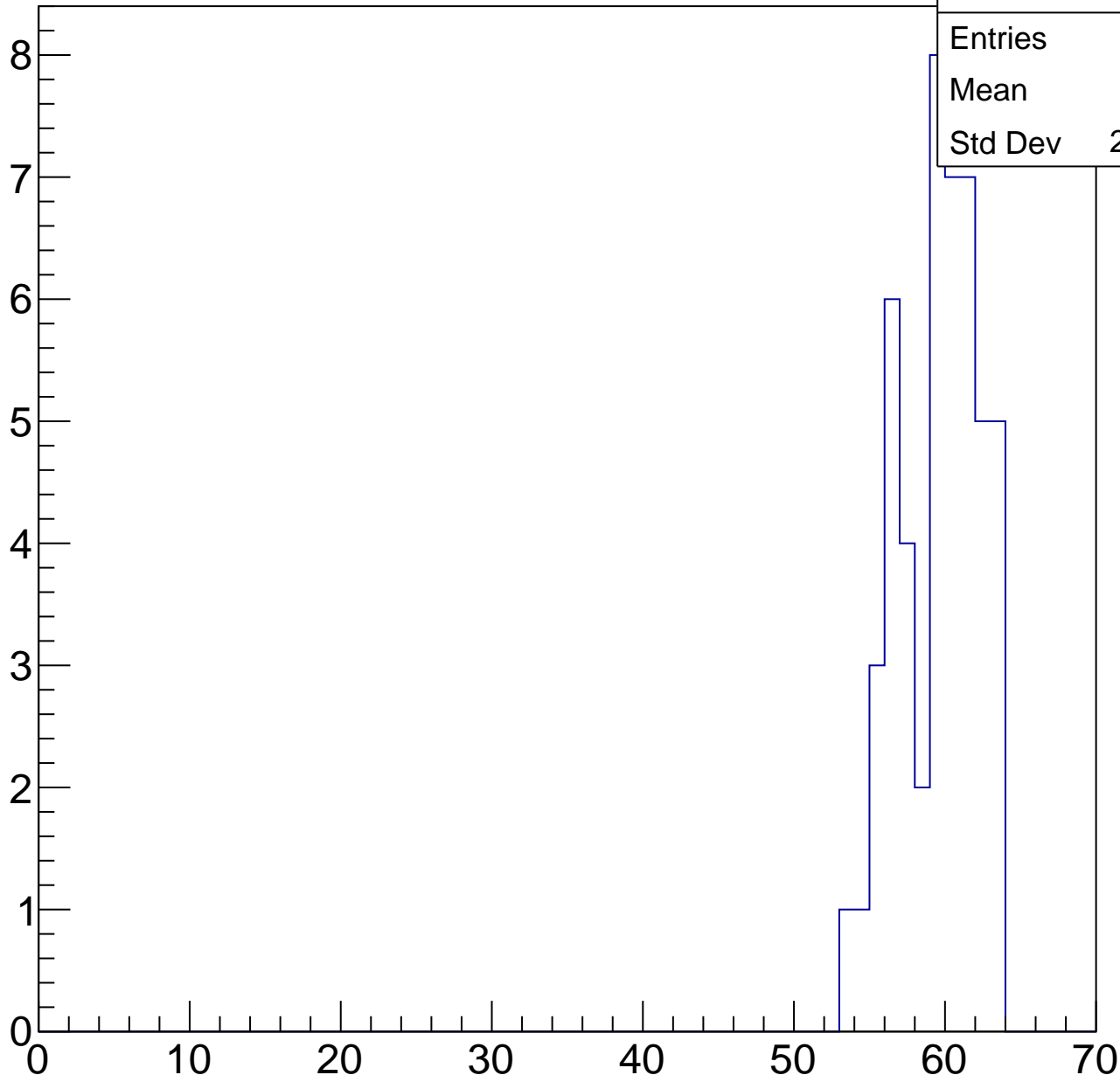
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	49
Mean	59.1
Std Dev	2.636

ampl

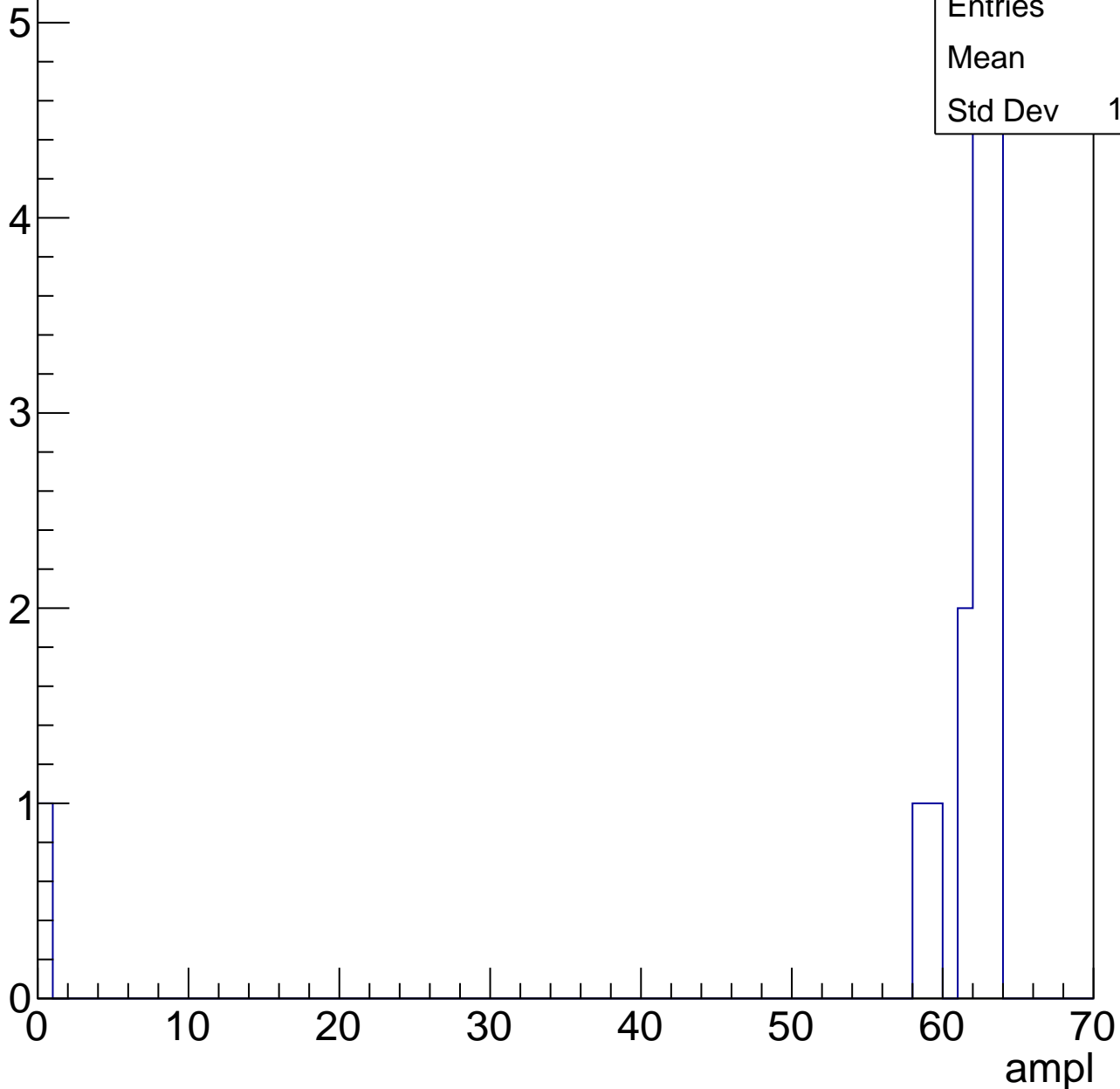


# B1L101S, U11-ch74, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	15
Mean	57.6
Std Dev	15.46





# B1L101S, U11-ch74, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L101S, U11-ch75, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	72
Mean	28.17
Std Dev	4.723

**Gaus mean : 29.1189**

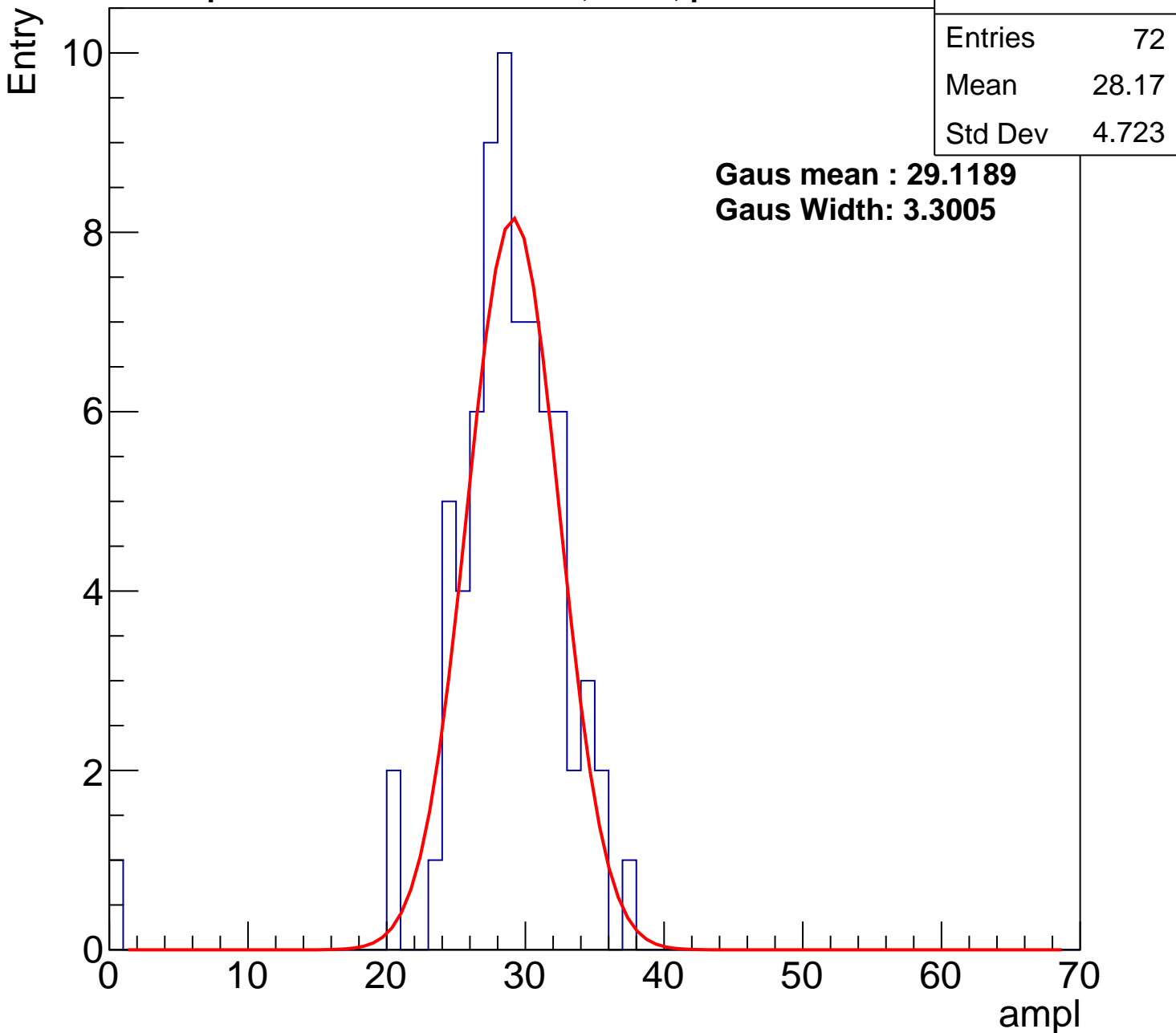
**Gaus Width: 3.3005**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U11-ch75, adc1

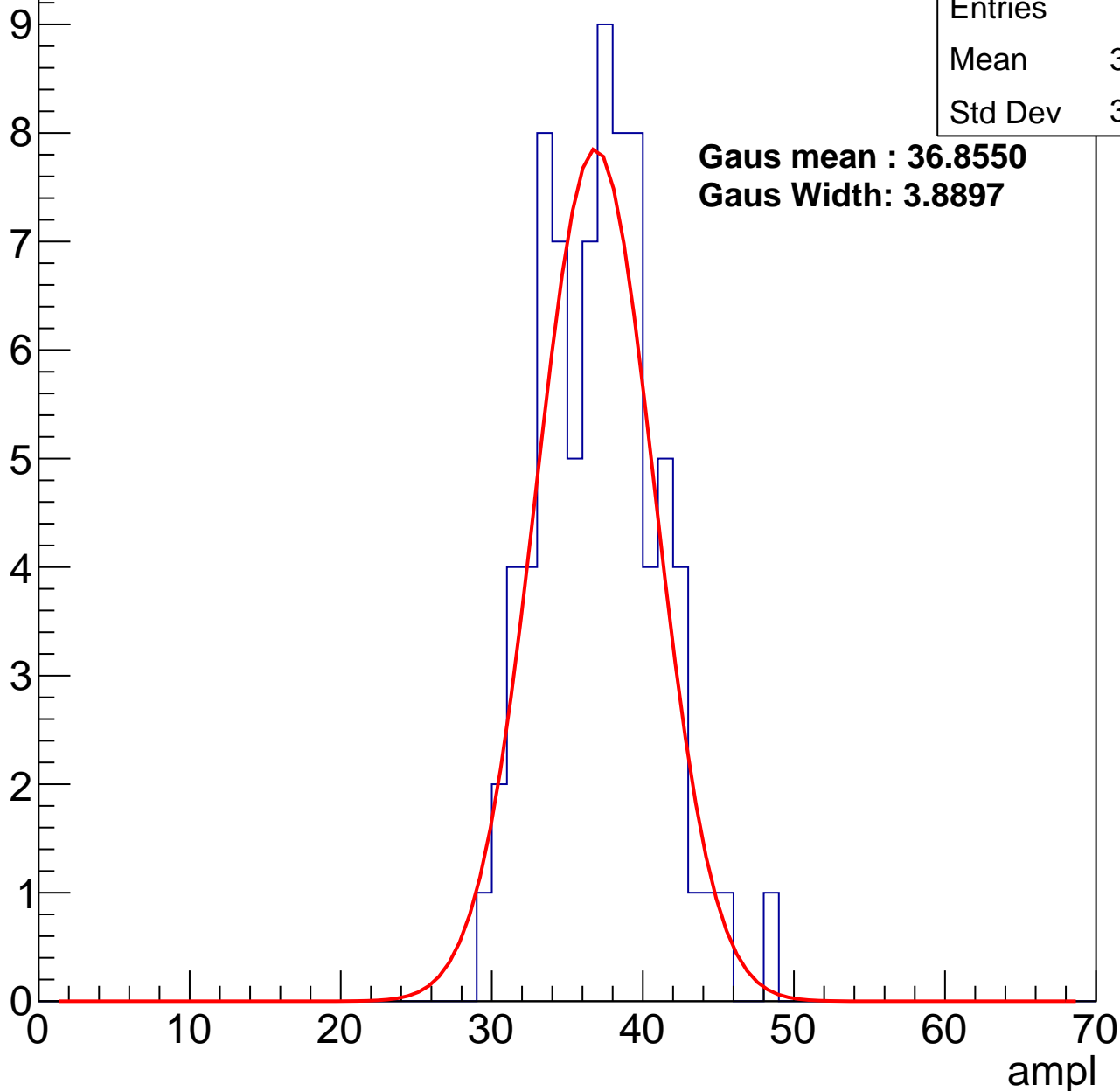
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	80
Mean	36.65
Std Dev	3.775

**Gaus mean : 36.8550**

**Gaus Width: 3.8897**



# B1L101S, U11-ch75, adc2

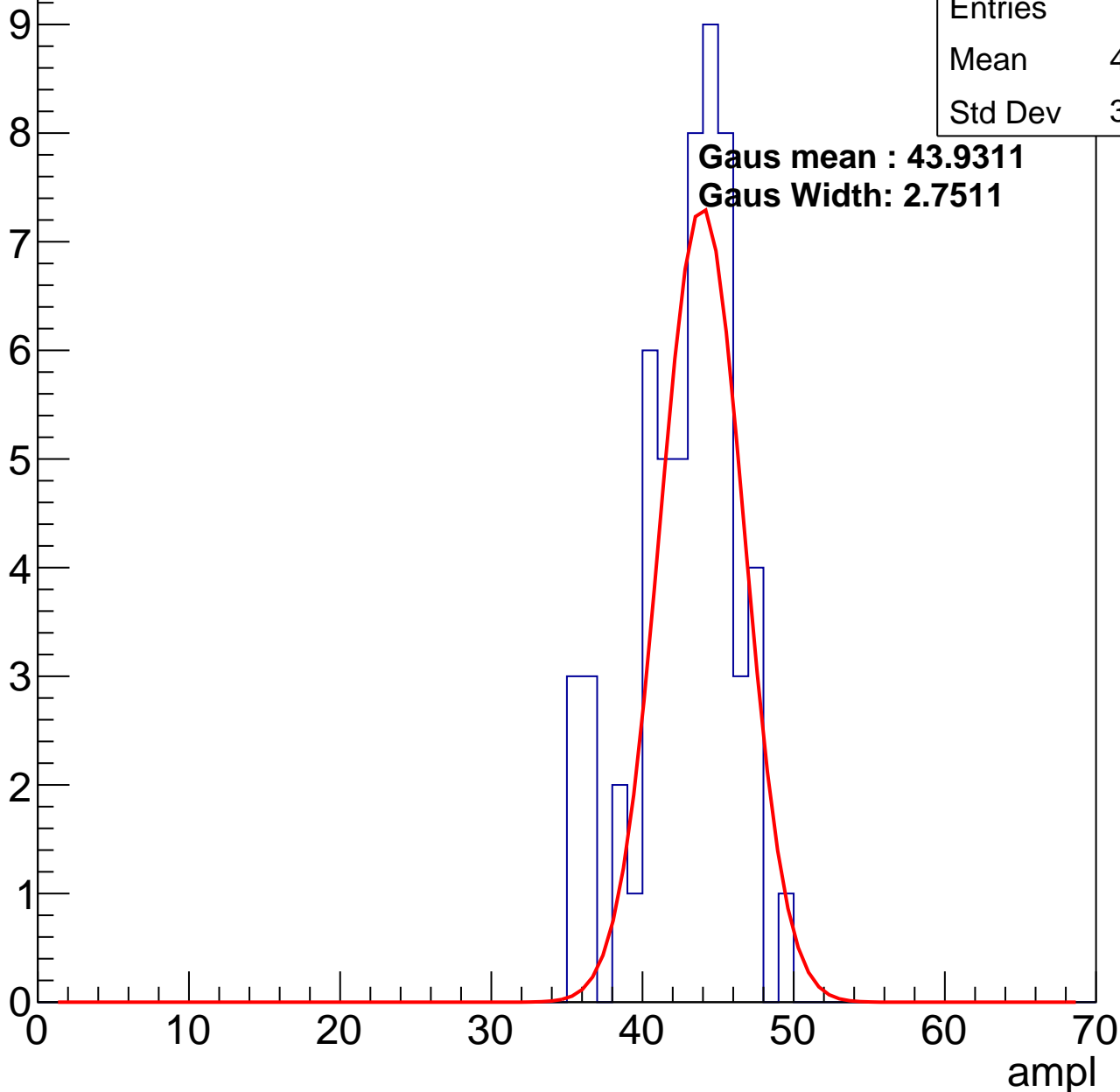
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	42.38
Std Dev	3.295

**Gaus mean : 43.9311**

**Gaus Width: 2.7511**

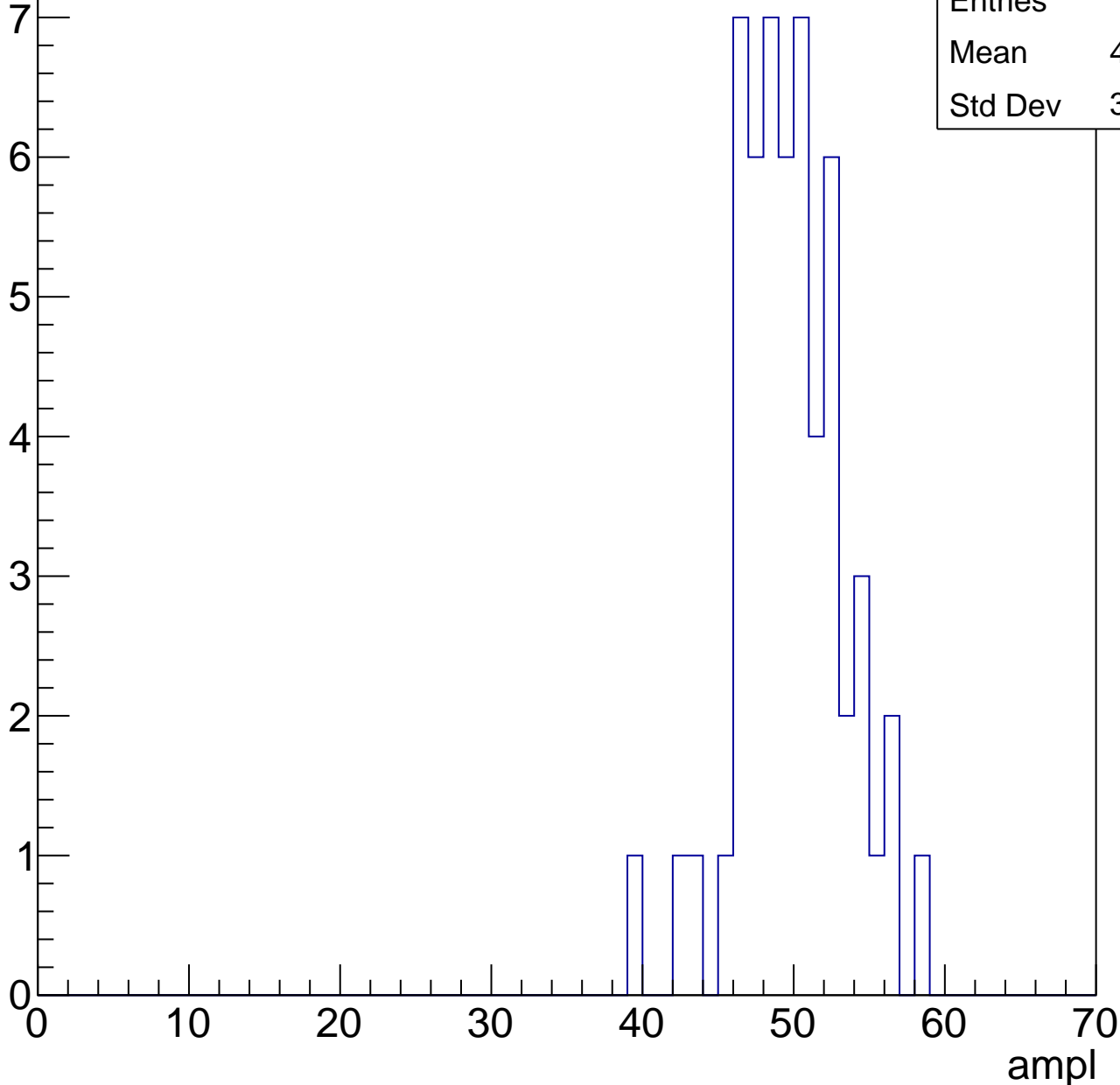


# B1L101S, U11-ch75, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

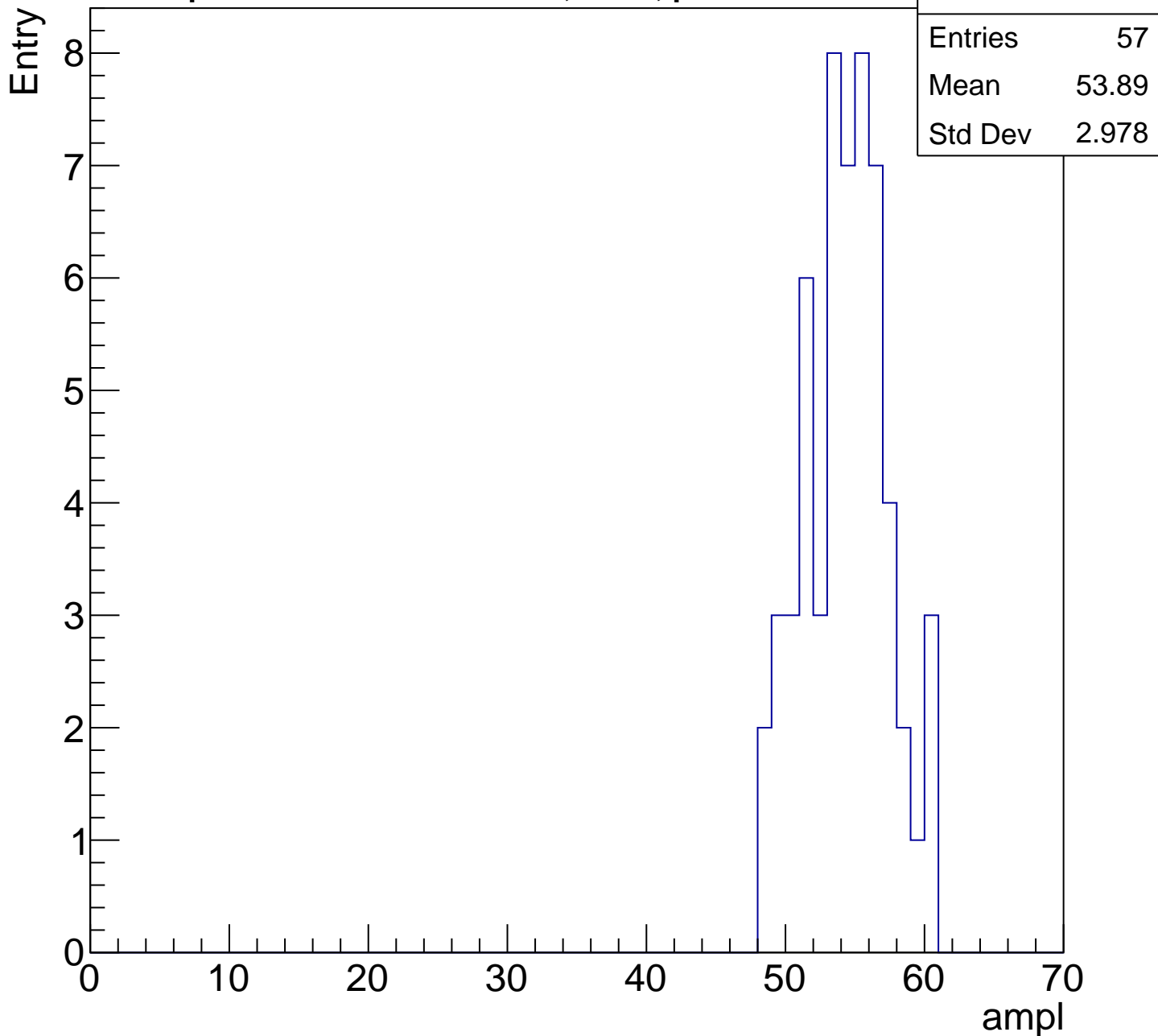
Entry

Entries	56
Mean	49.32
Std Dev	3.506



# B1L101S, U11-ch75, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

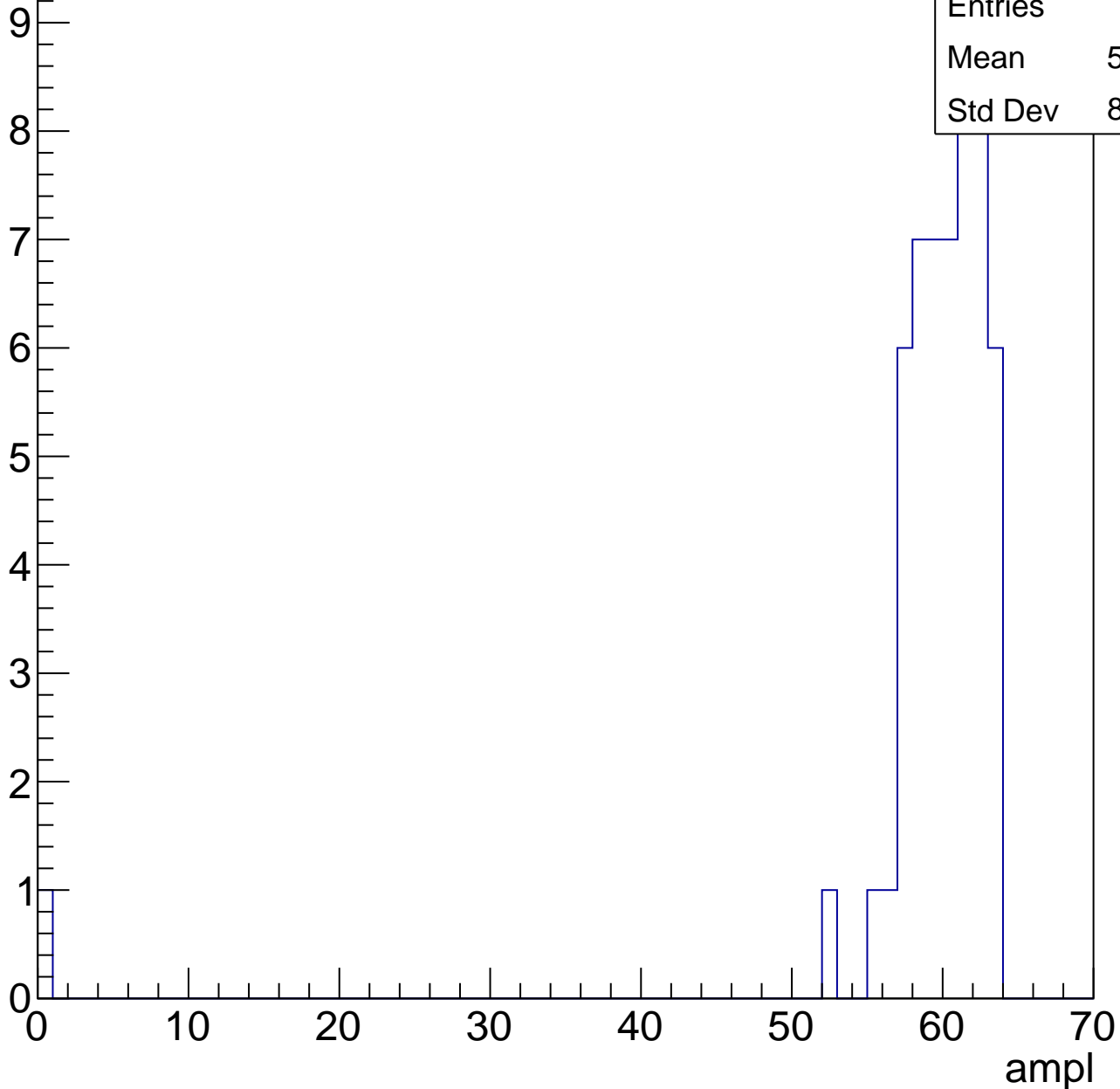


# B1L101S, U11-ch75, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

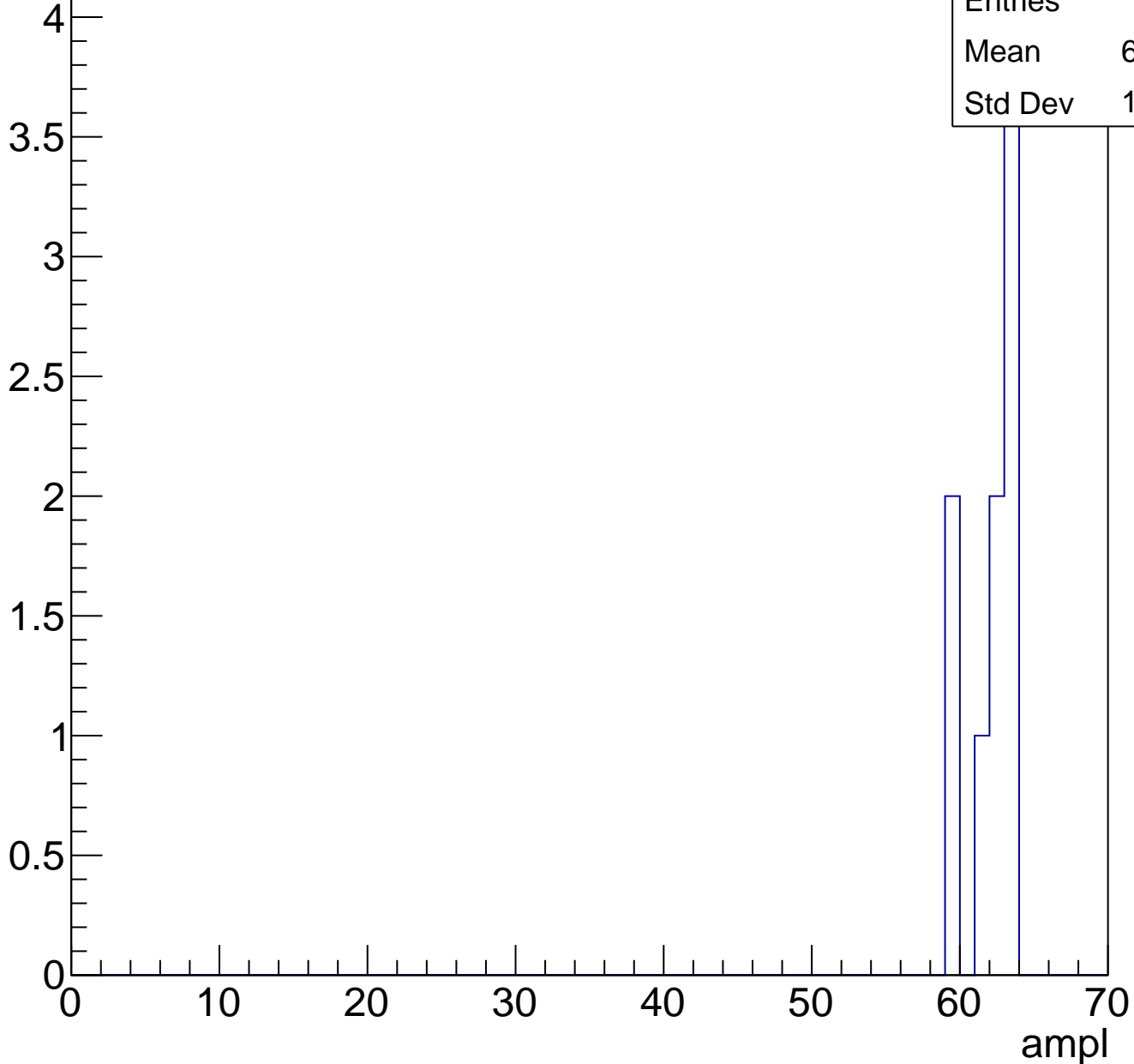
Entries	54
Mean	58.65
Std Dev	8.378



# B1L101S, U11-ch75, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch75, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U11-ch76, adc0

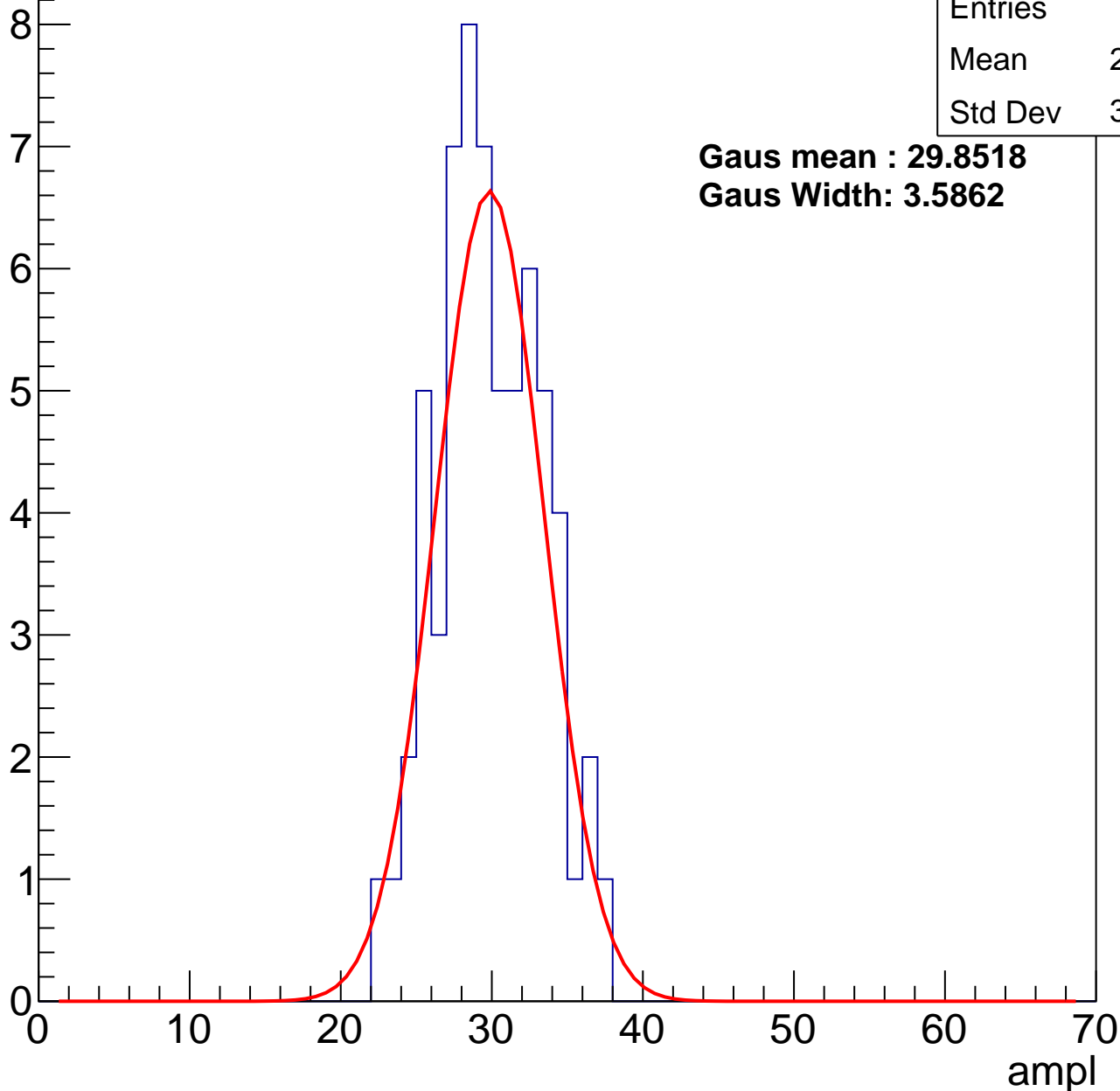
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	29.43
Std Dev	3.389

**Gaus mean : 29.8518**

**Gaus Width: 3.5862**



# B1L101S, U11-ch76, adc1

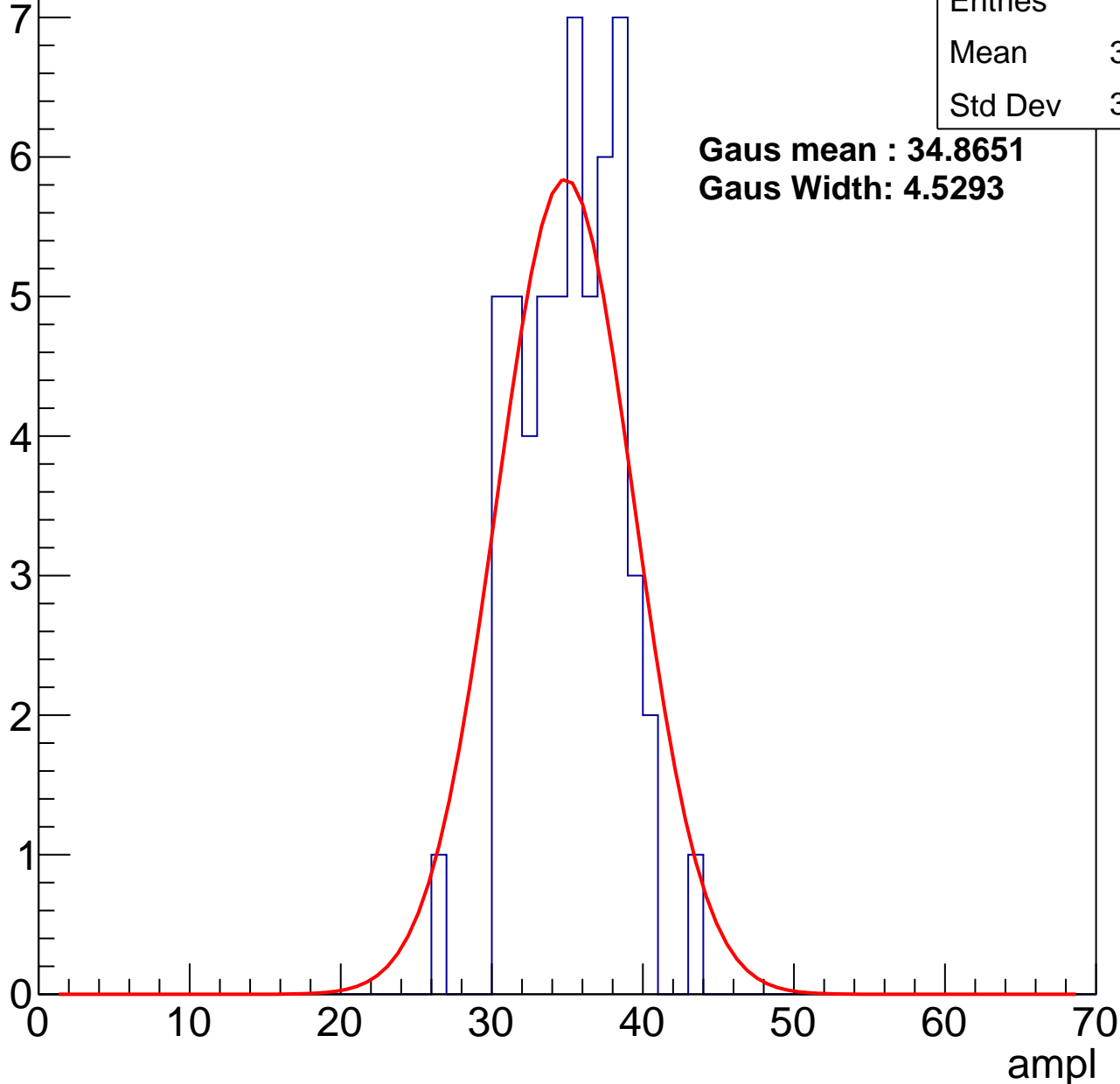
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	34.77
Std Dev	3.268

**Gaus mean : 34.8651**

**Gaus Width: 4.5293**



# B1L101S, U11-ch76, adc2

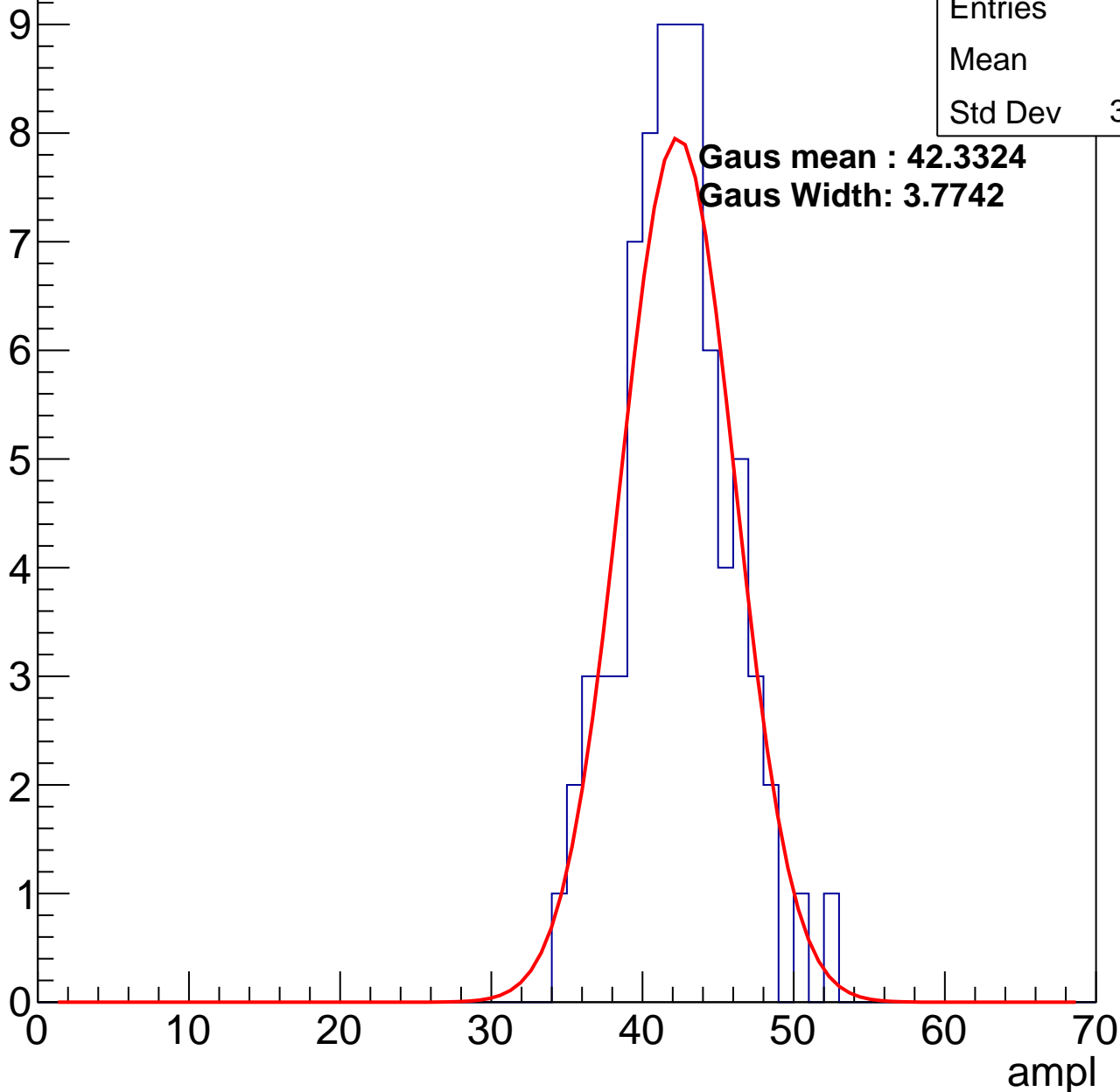
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	41.8
Std Dev	3.543

**Gaus mean : 42.3324**

**Gaus Width: 3.7742**

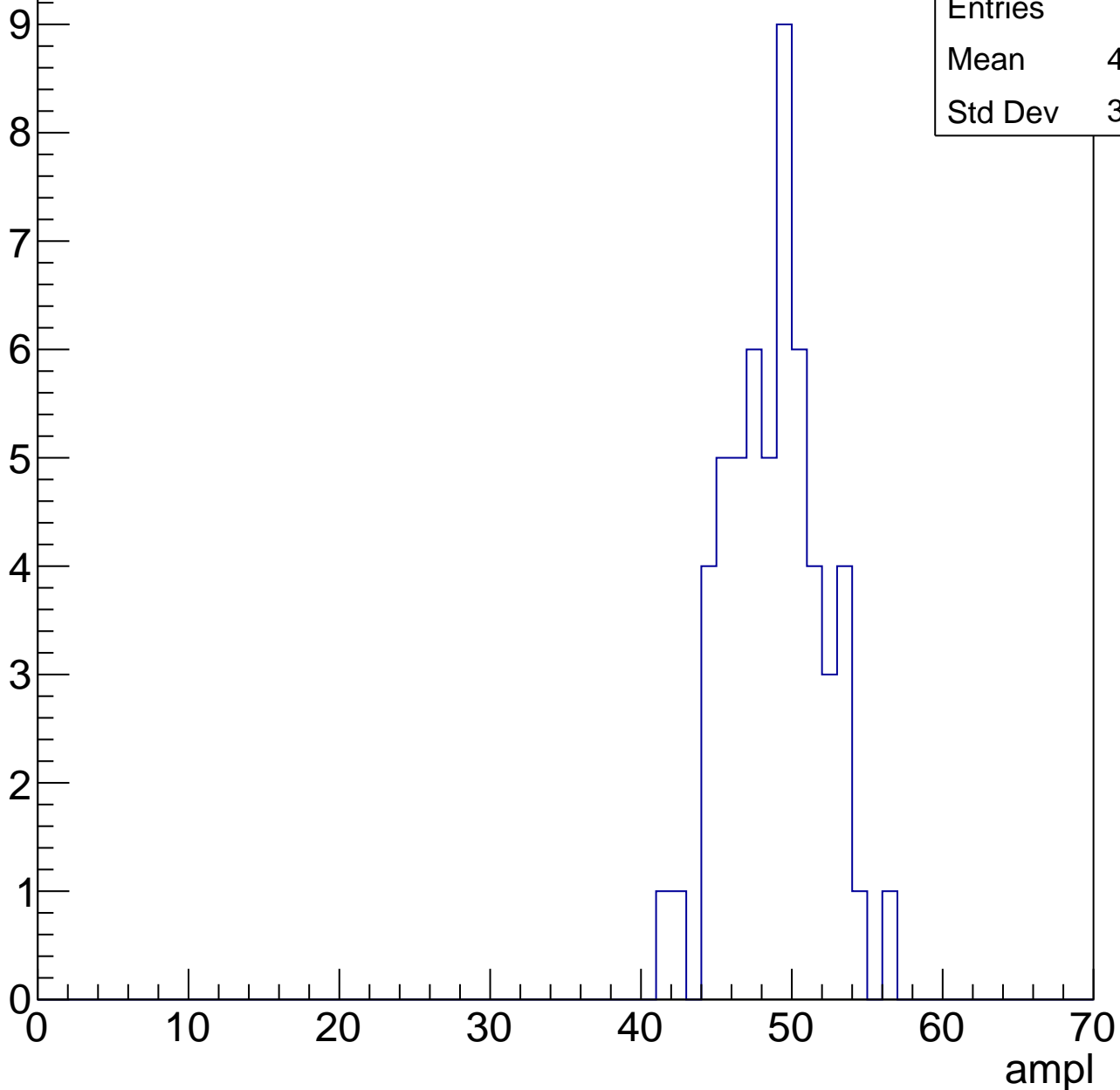


# B1L101S, U11-ch76, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	48.35
Std Dev	3.106

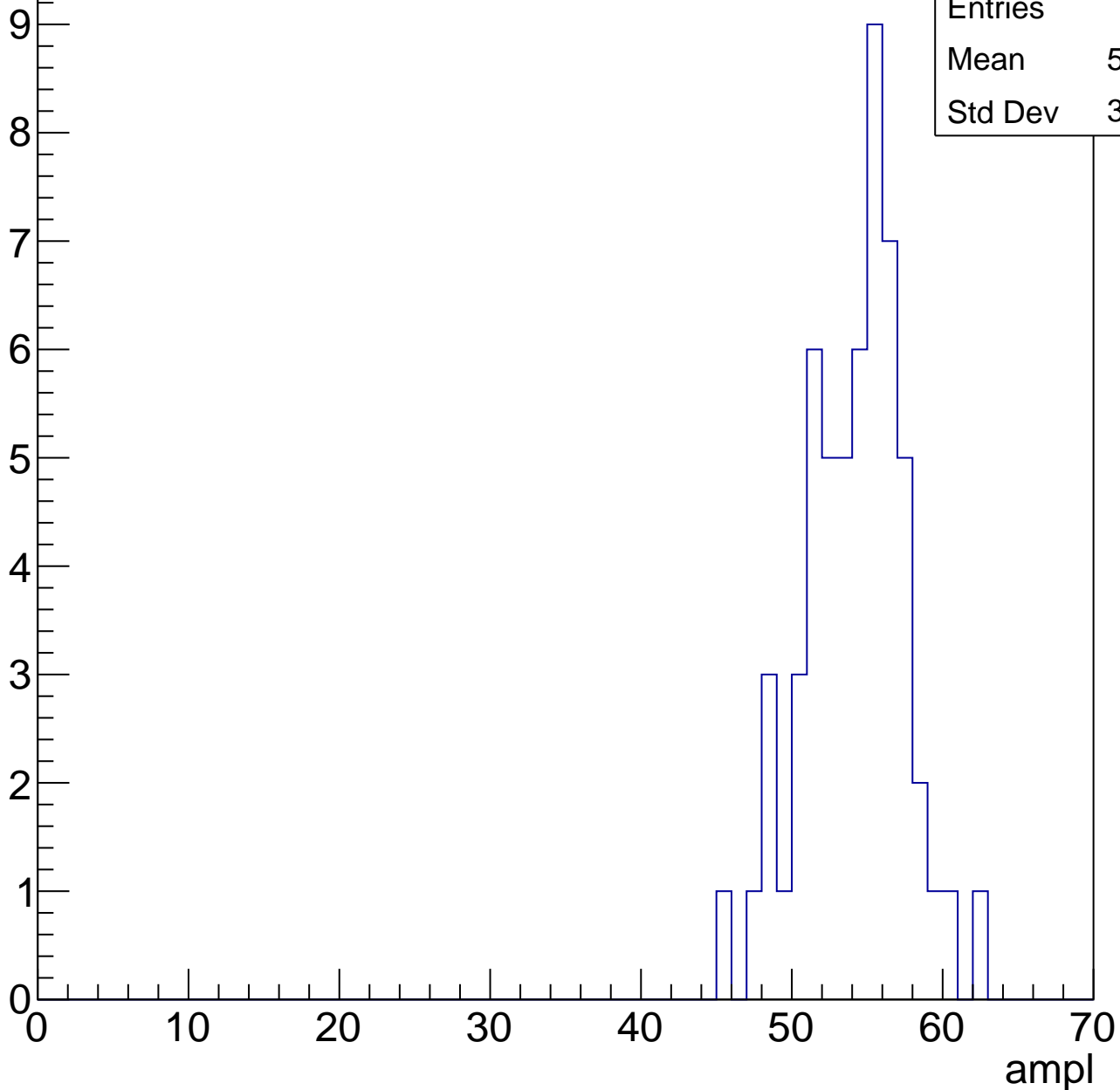


# B1L101S, U11-ch76, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	53.67
Std Dev	3.305

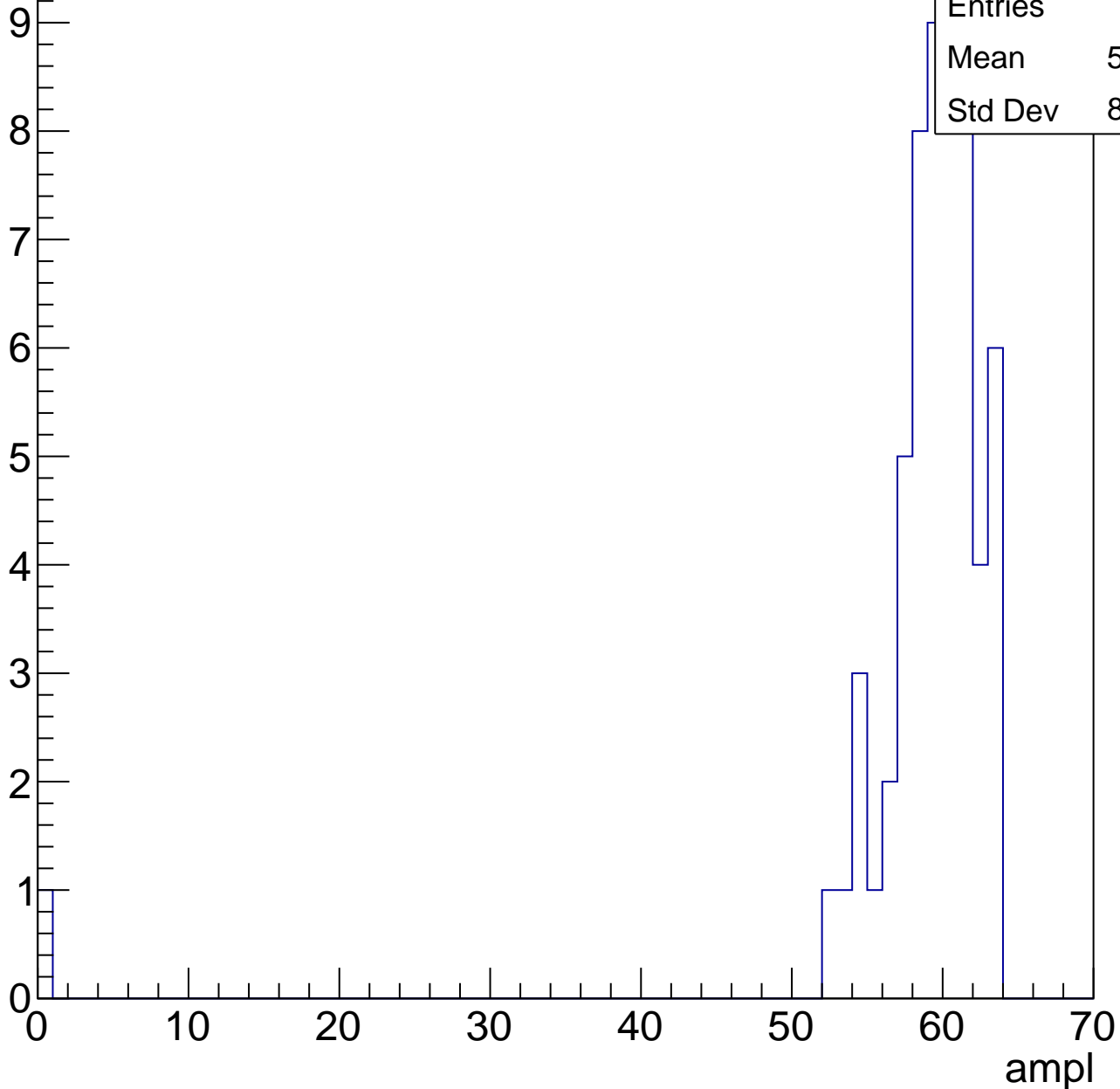


# B1L101S, U11-ch76, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	58.09
Std Dev	8.127

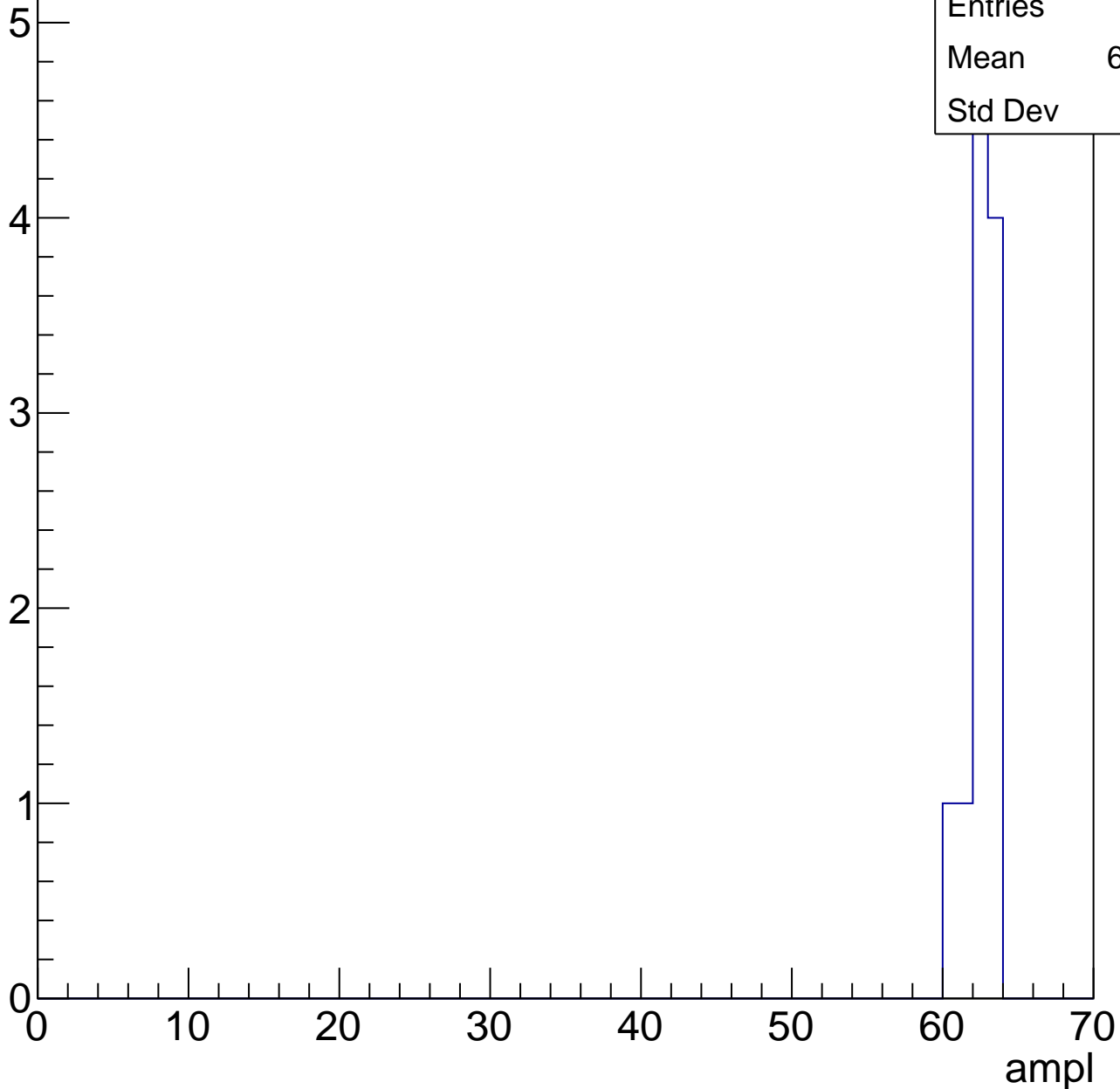


# B1L101S, U11-ch76, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	11
Mean	62.09
Std Dev	0.9





# B1L101S, U11-ch76, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U11-ch77, adc0

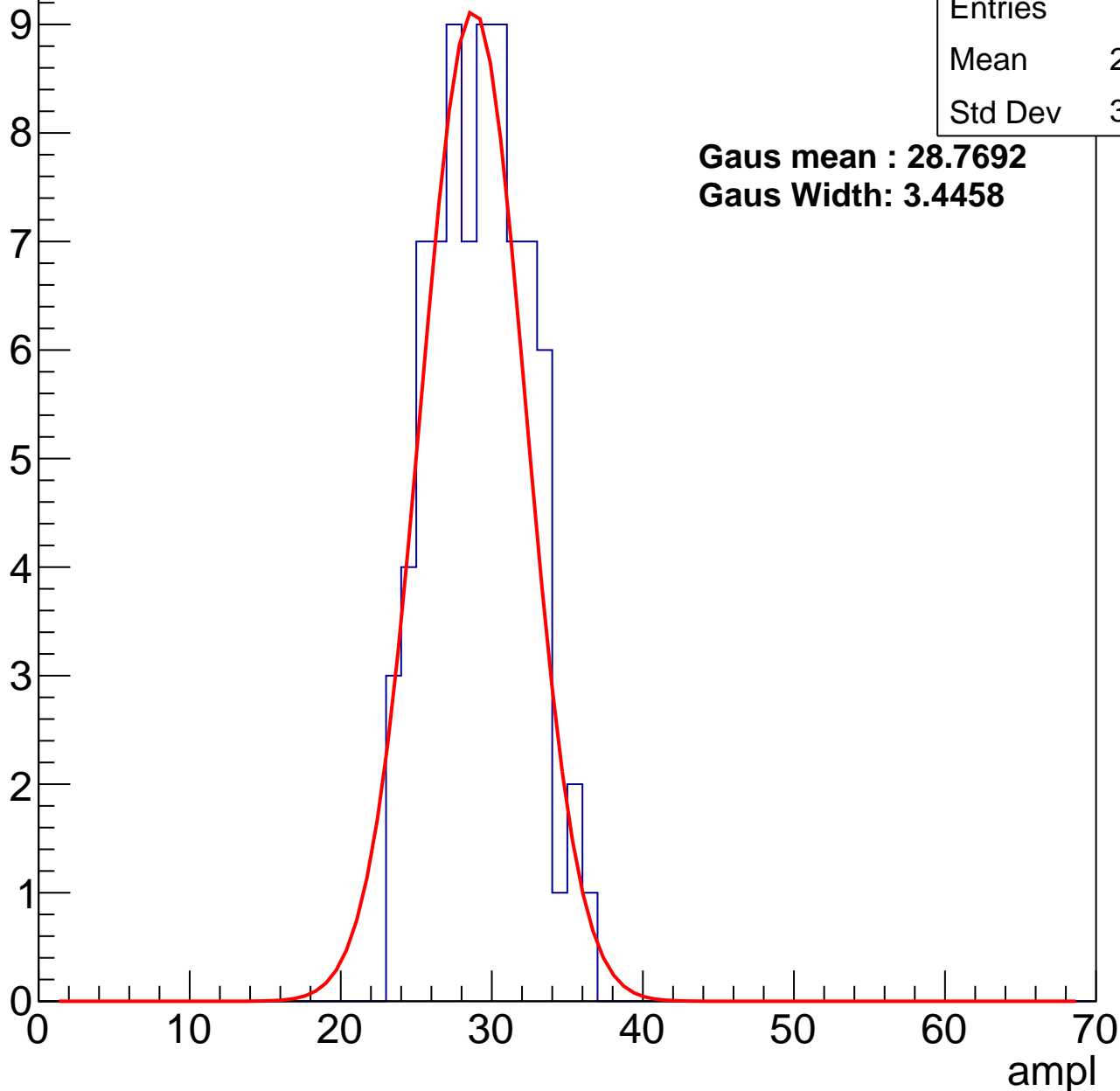
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	79
Mean	28.75
Std Dev	3.108

**Gaus mean : 28.7692**

**Gaus Width: 3.4458**



# B1L101S, U11-ch77, adc1

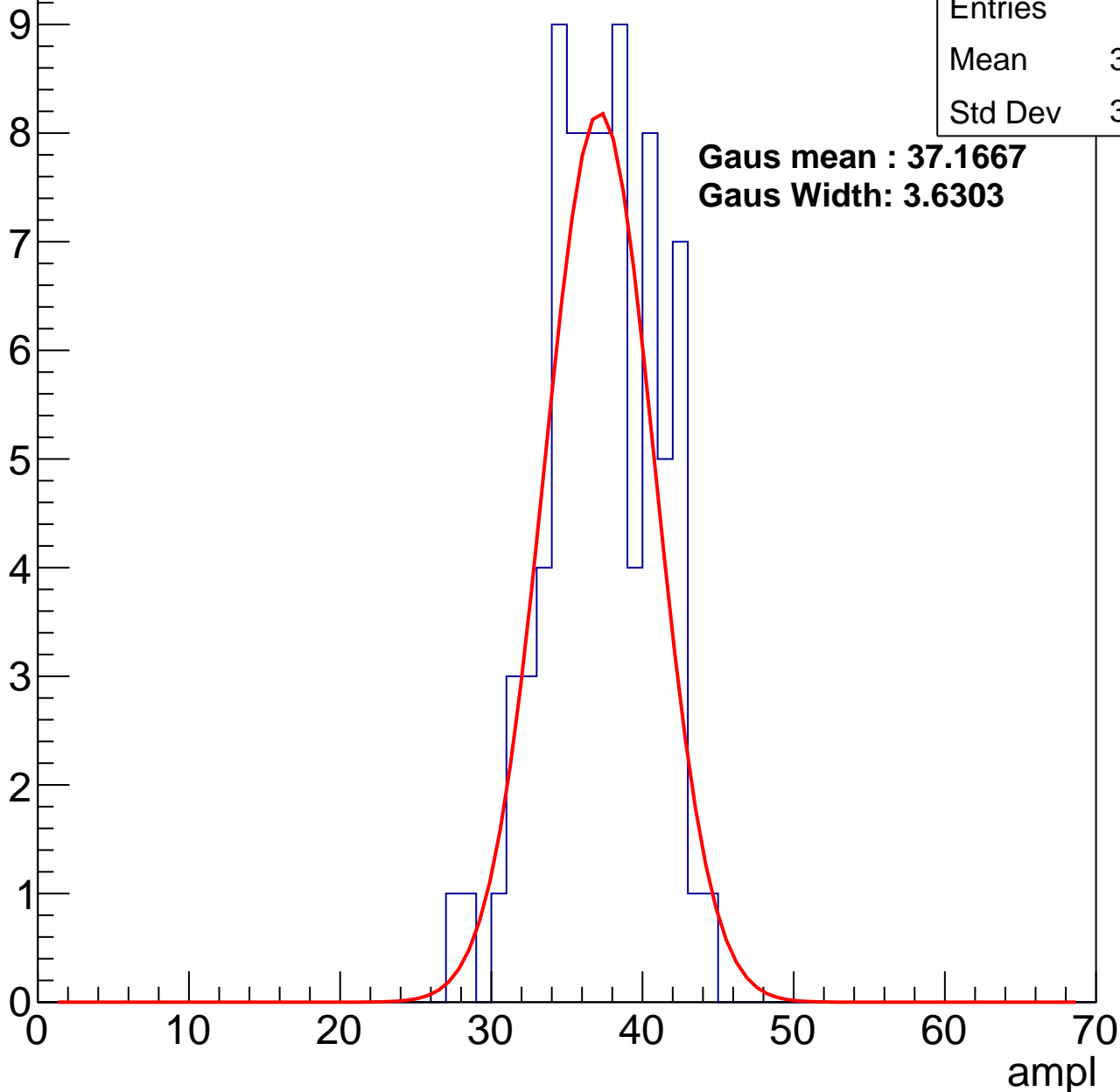
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	81
Mean	36.79
Std Dev	3.568

**Gaus mean : 37.1667**

**Gaus Width: 3.6303**



# B1L101S, U11-ch77, adc2

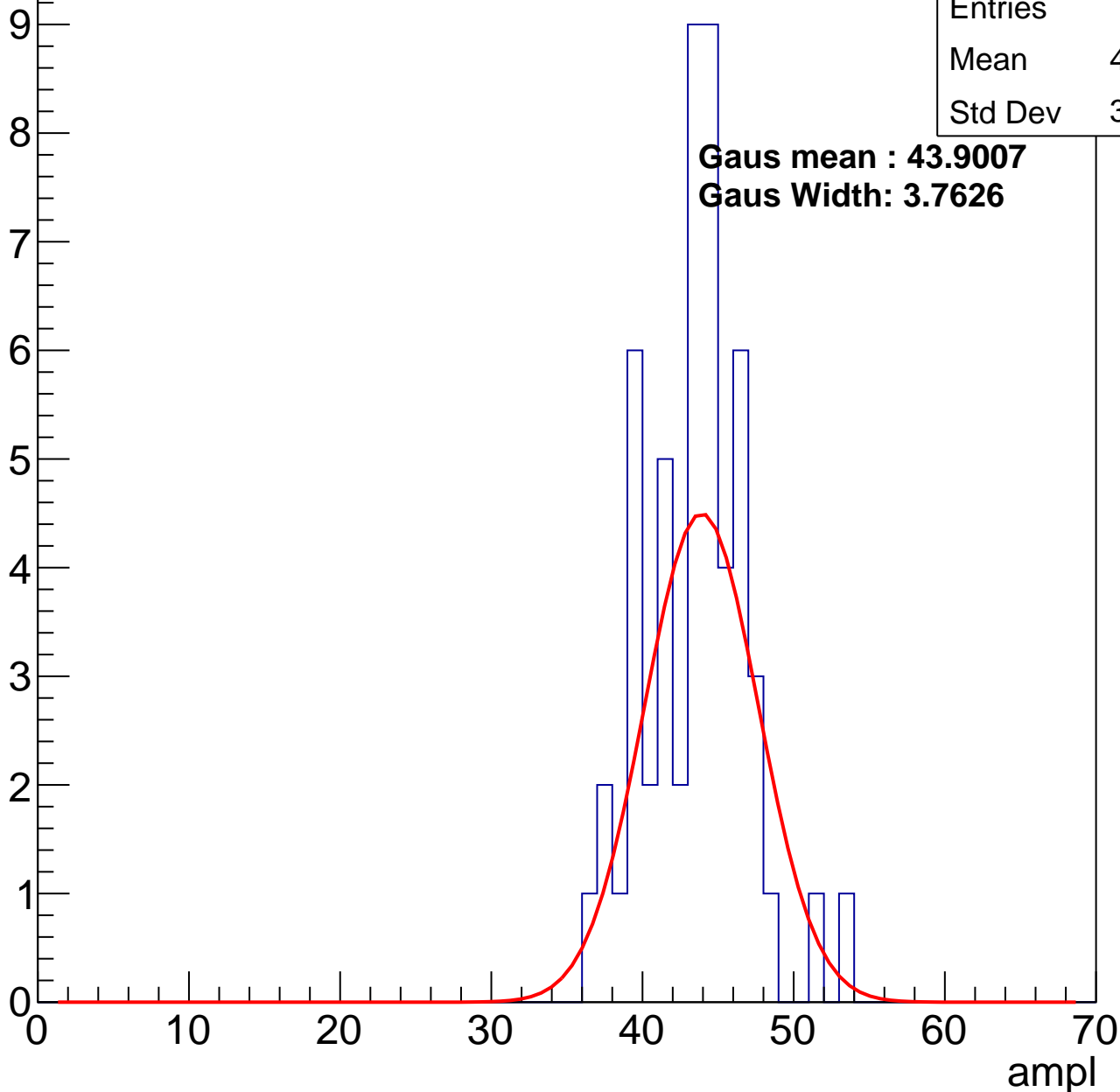
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	43.08
Std Dev	3.358

**Gaus mean : 43.9007**

**Gaus Width: 3.7626**

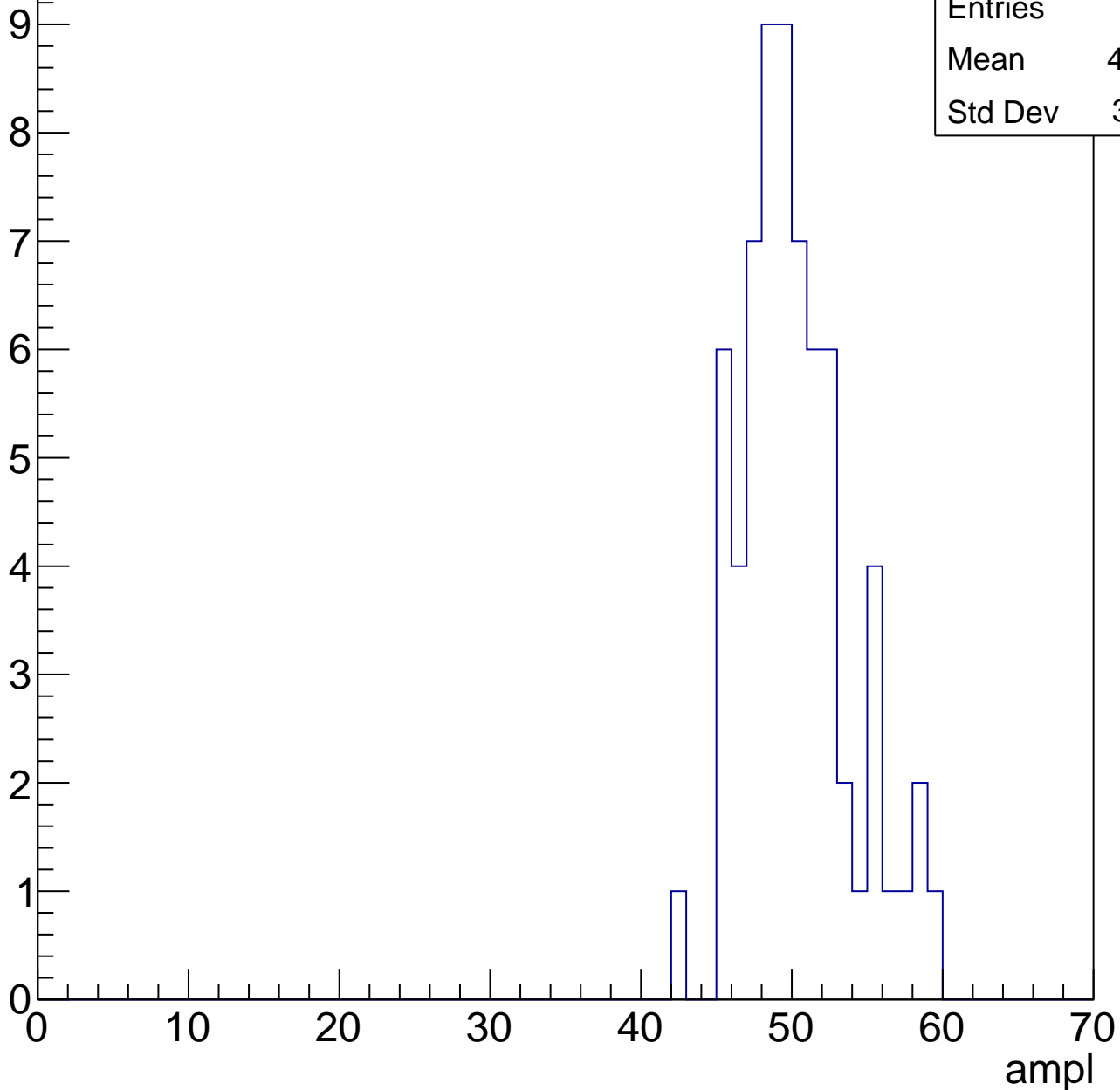


# B1L101S, U11-ch77, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	49.76
Std Dev	3.541

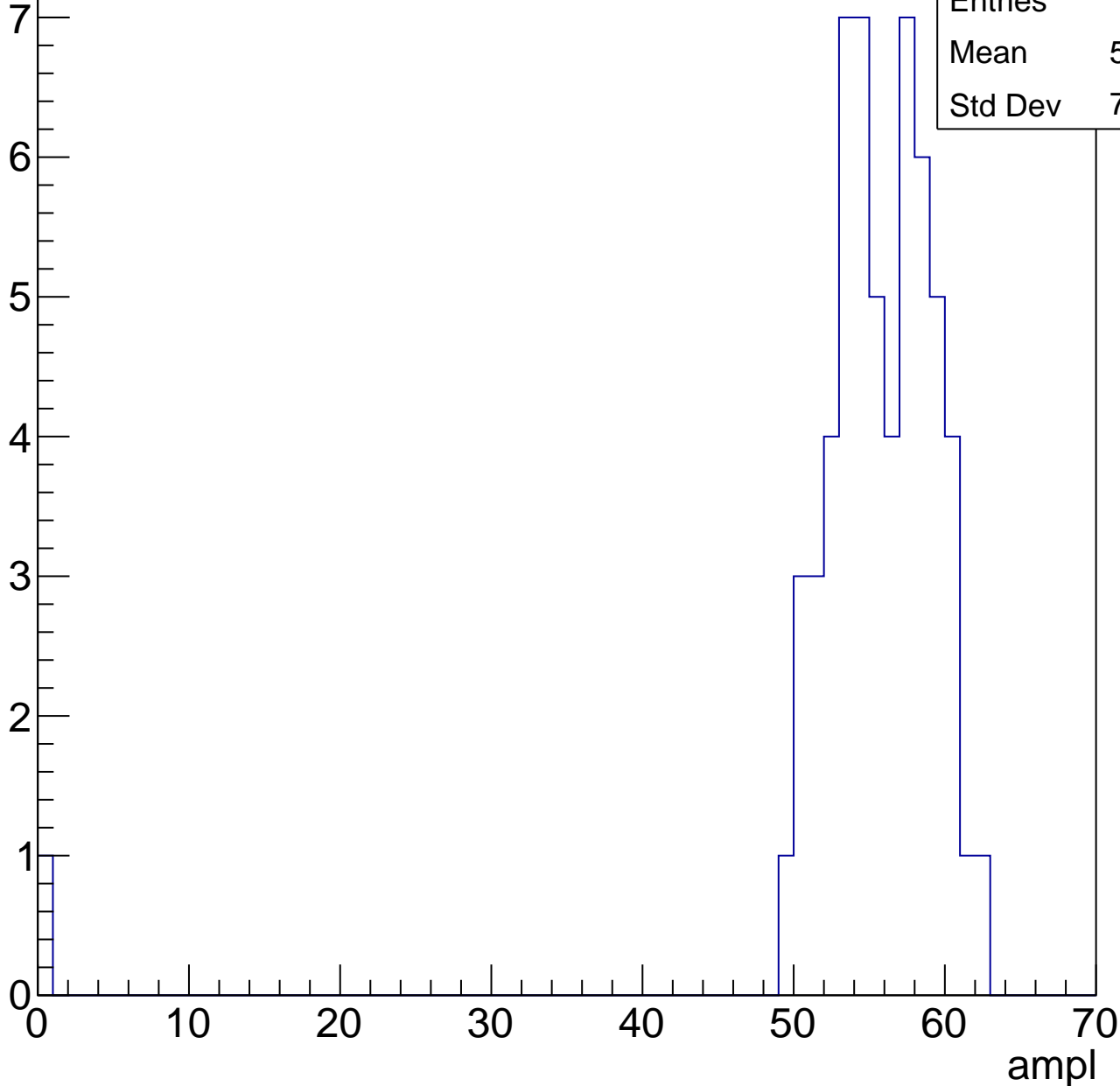


# B1L101S, U11-ch77, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

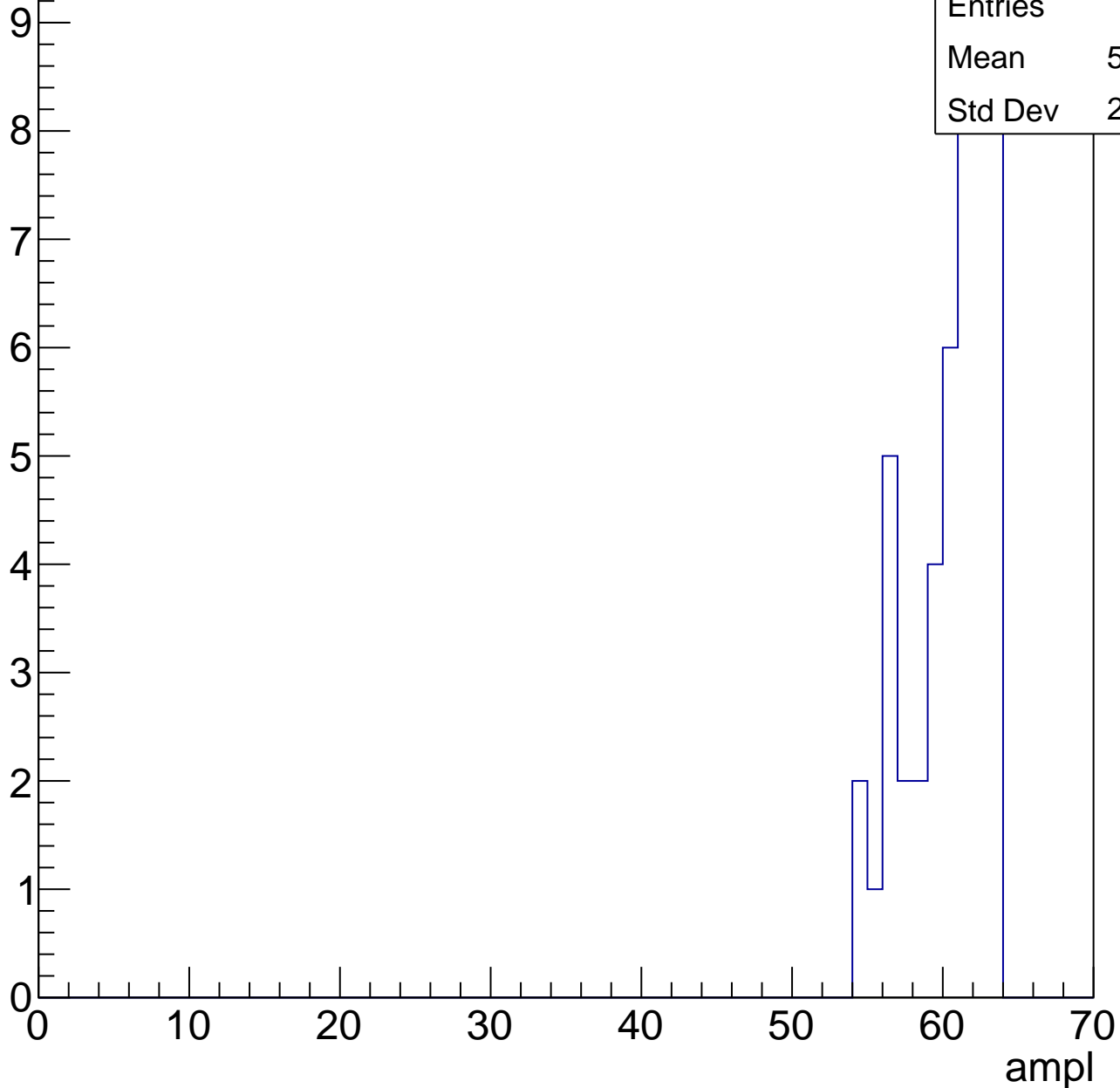
Entries	59
Mean	54.46
Std Dev	7.799



# B1L101S, U11-ch77, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U11-ch77, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.67
Std Dev	0.4714

ampl

0 10 20 30 40 50 60 70



# B1L101S, U11-ch77, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U11-ch78, adc0

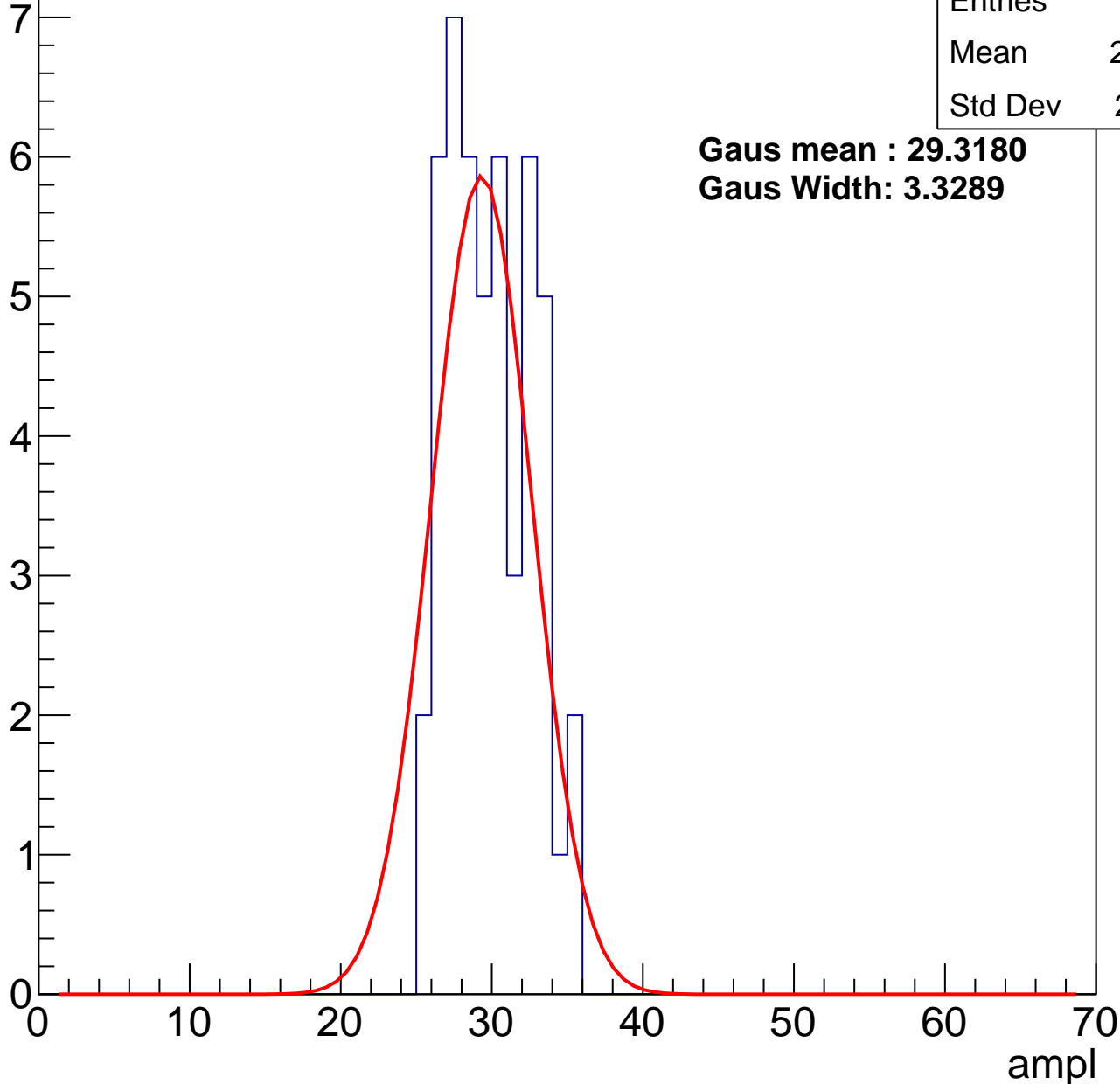
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	49
Mean	29.43
Std Dev	2.711

**Gaus mean : 29.3180**

**Gaus Width: 3.3289**



# B1L101S, U11-ch78, adc1

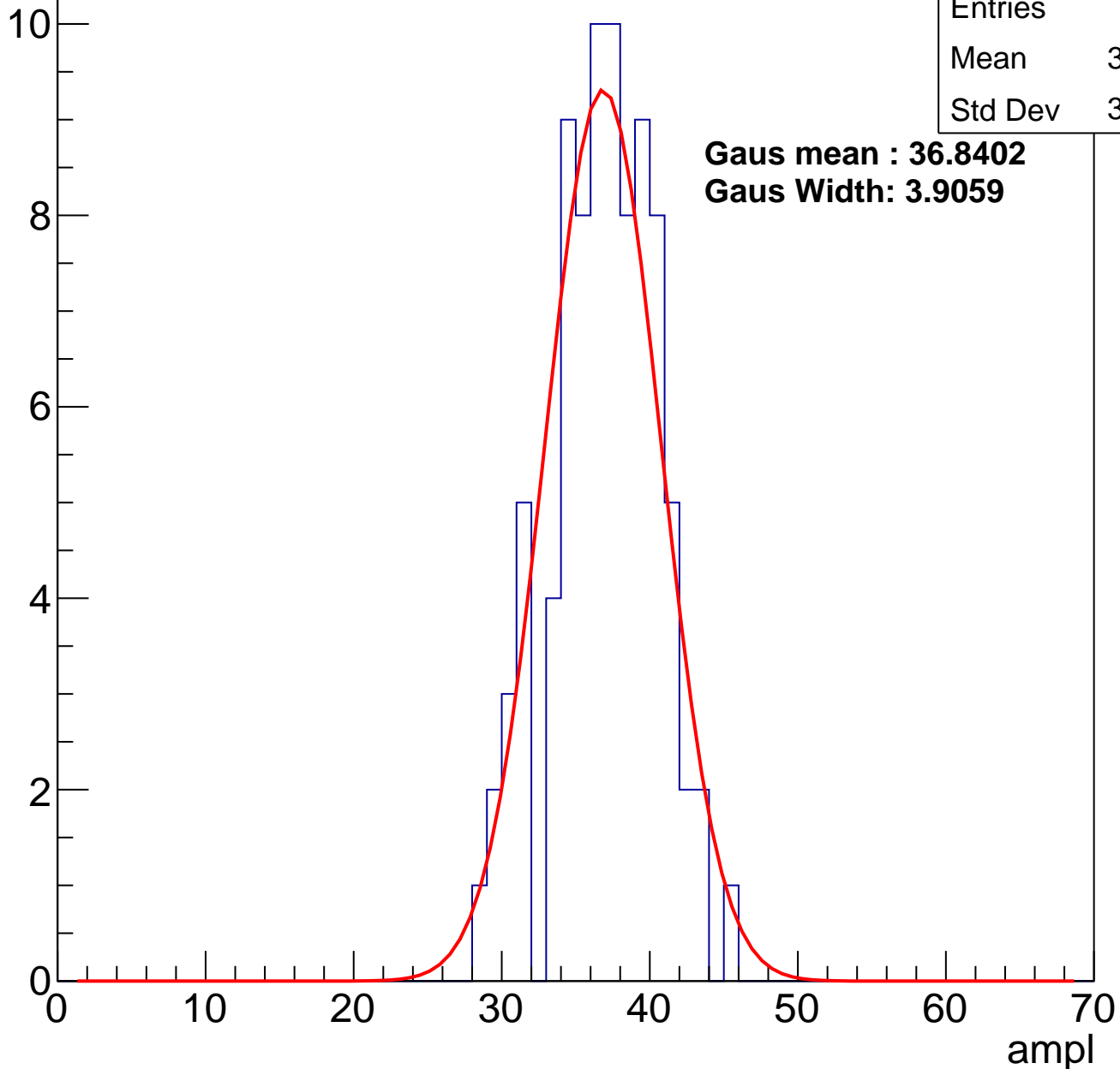
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	87
Mean	36.48
Std Dev	3.526

**Gaus mean : 36.8402**

**Gaus Width: 3.9059**

Entry



# B1L101S, U11-ch78, adc2

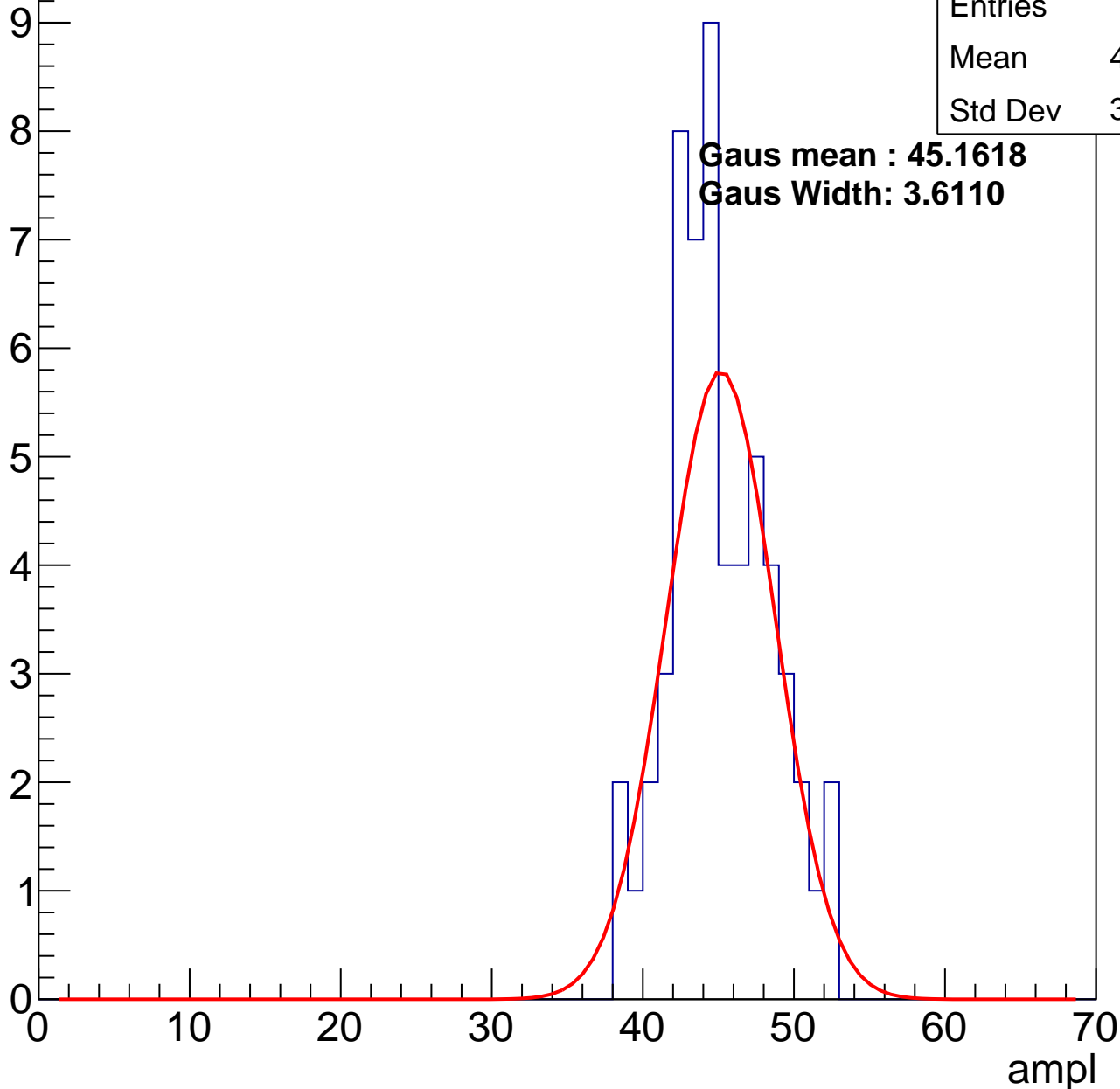
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	44.63
Std Dev	3.312

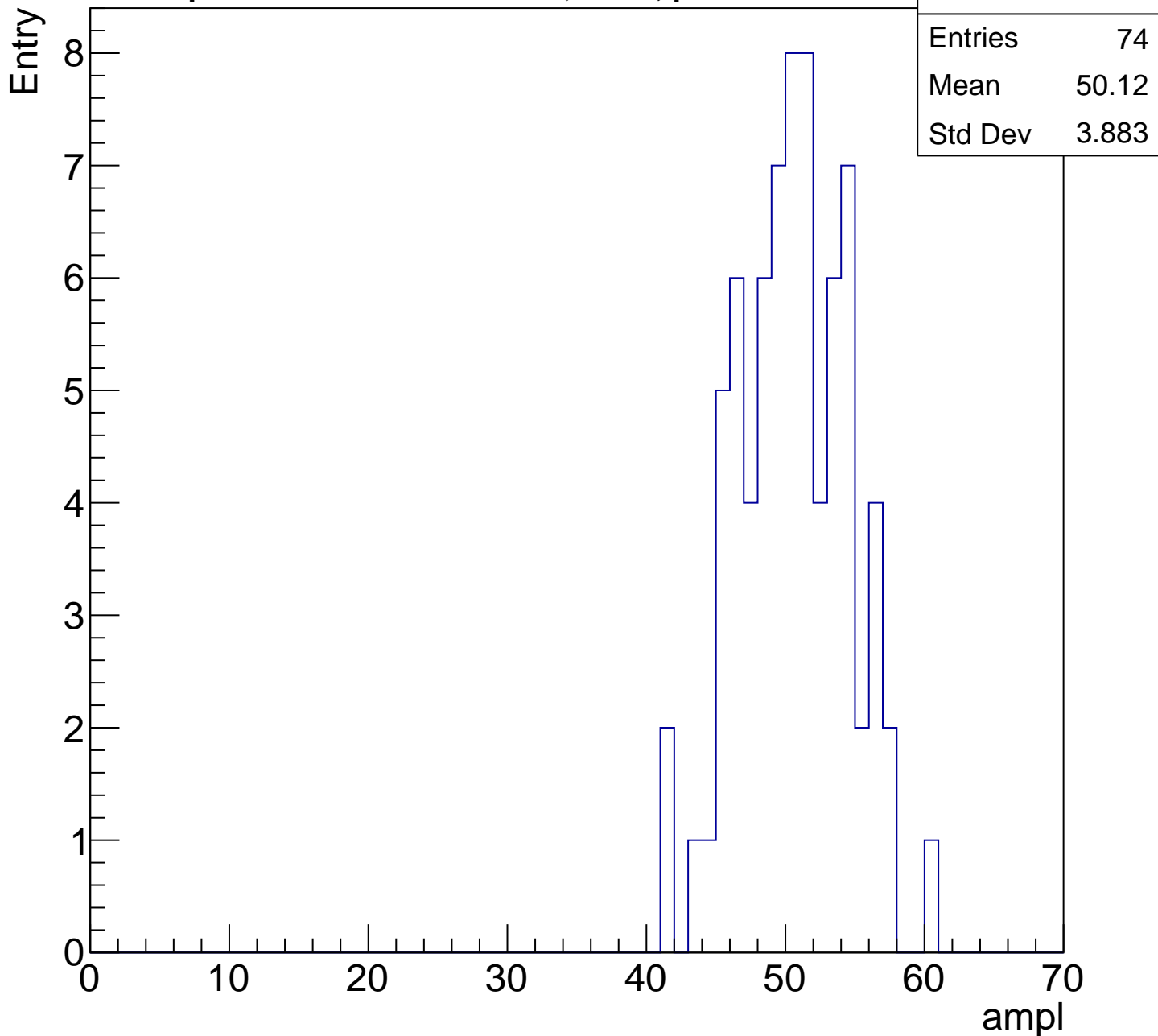
**Gaus mean : 45.1618**

**Gaus Width: 3.6110**



# B1L101S, U11-ch78, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

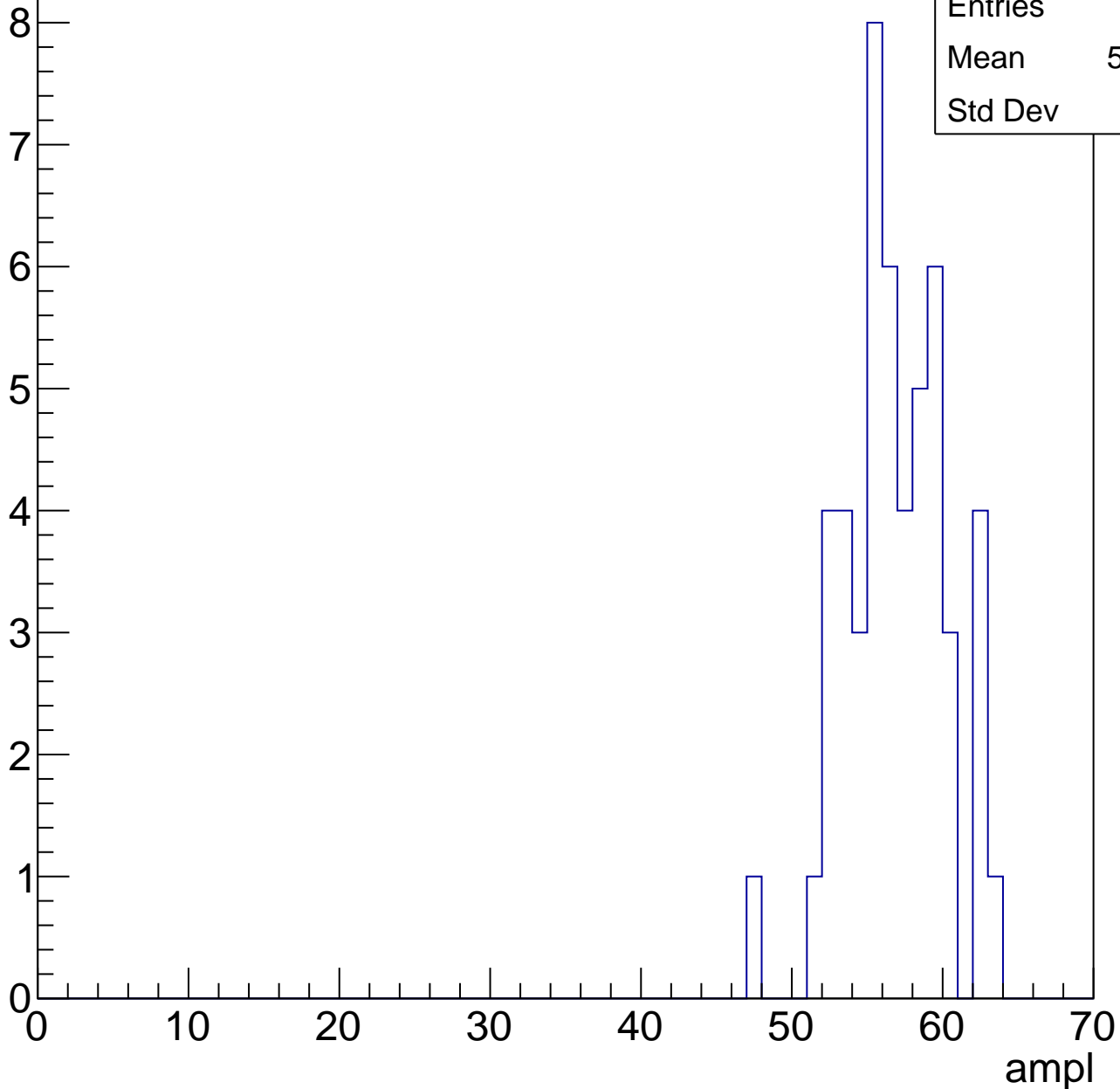


# B1L101S, U11-ch78, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	56.38
Std Dev	3.28



# B1L101S, U11-ch78, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

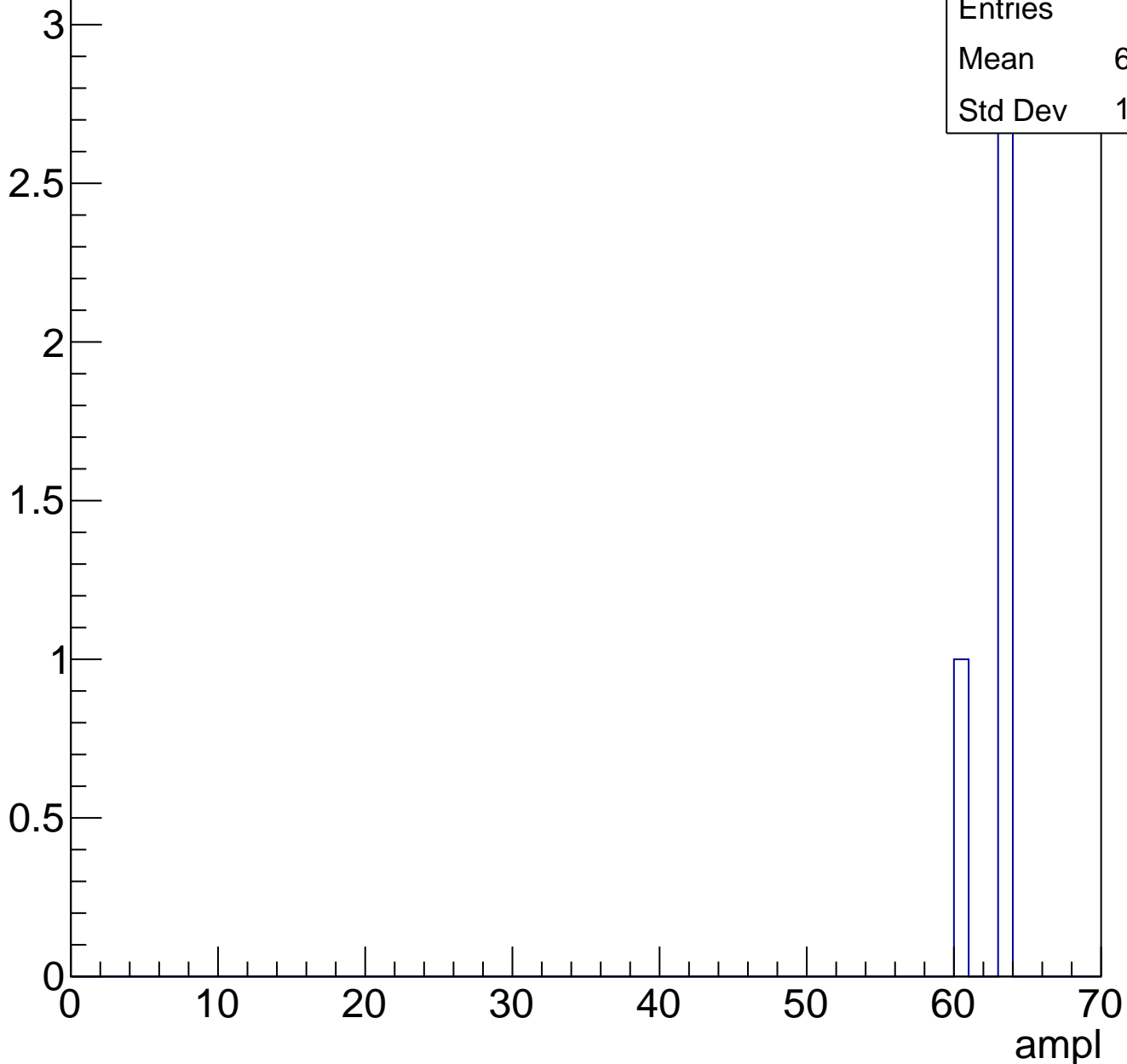
ampl

Entries	41
Mean	58.88
Std Dev	9.495

# B1L101S, U11-ch78, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

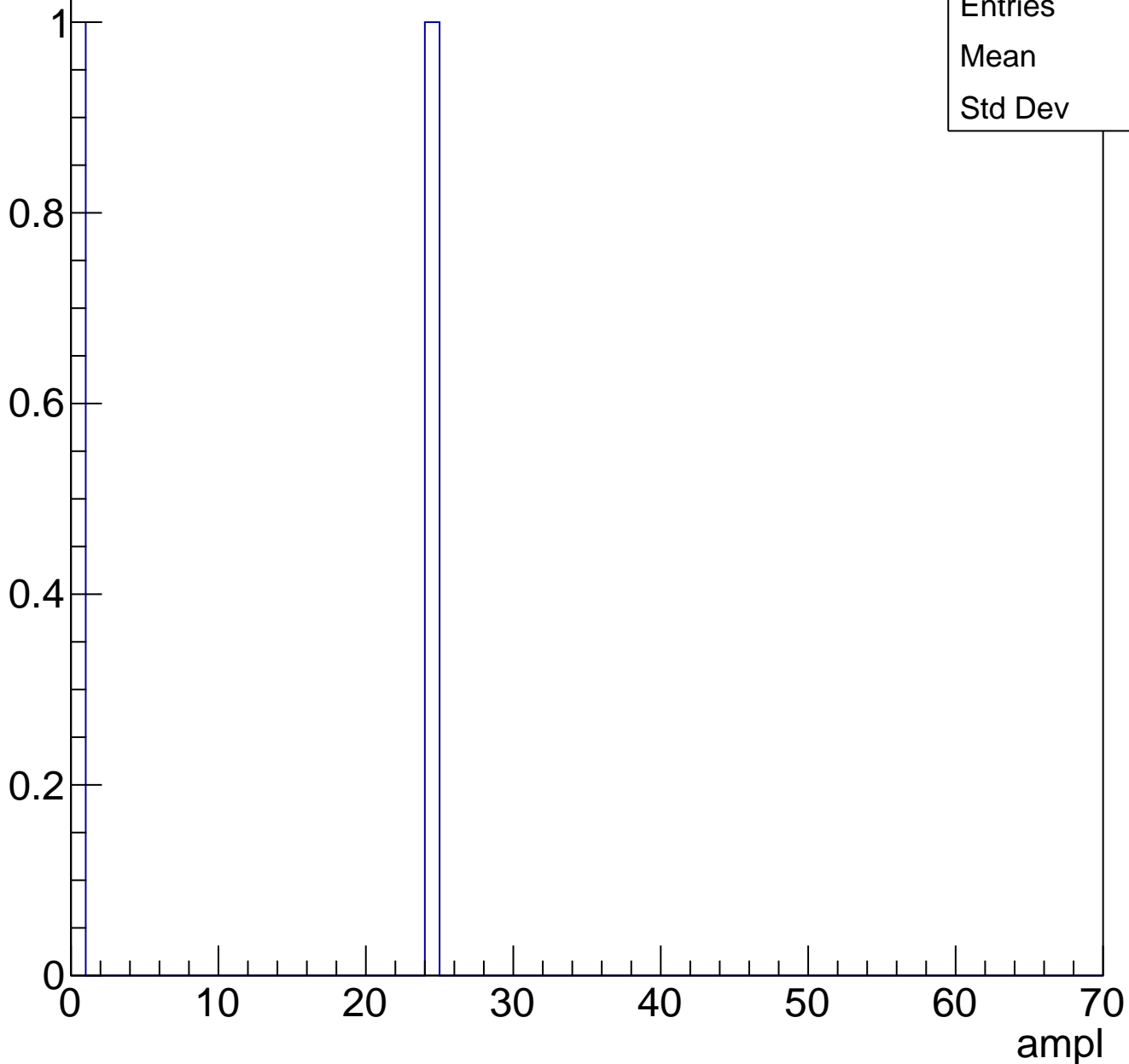




# B1L101S, U11-ch78, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U11-ch79, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	62
Mean	29.03
Std Dev	6.122

**Gaus mean : 31.2300**

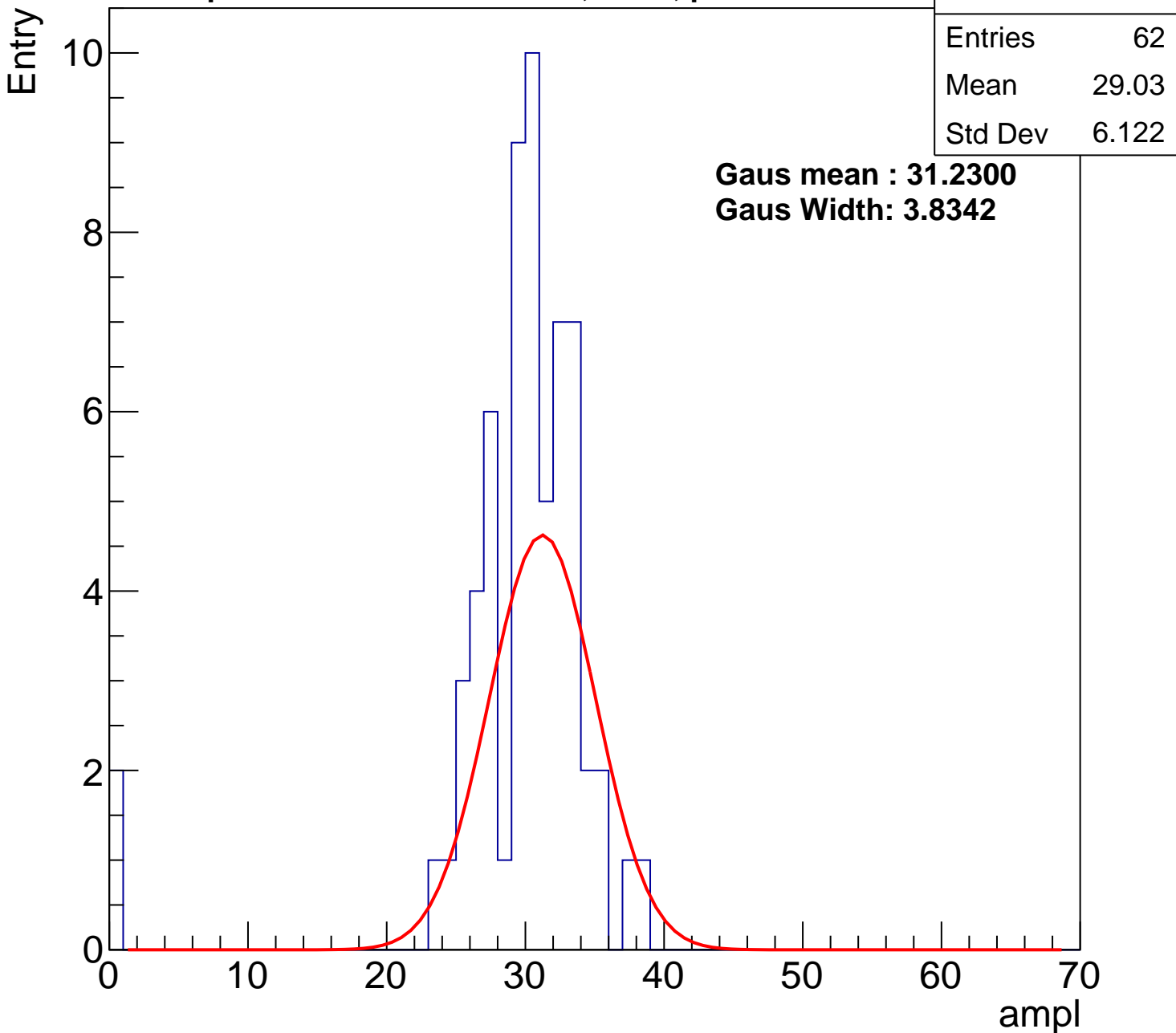
**Gaus Width: 3.8342**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U11-ch79, adc1

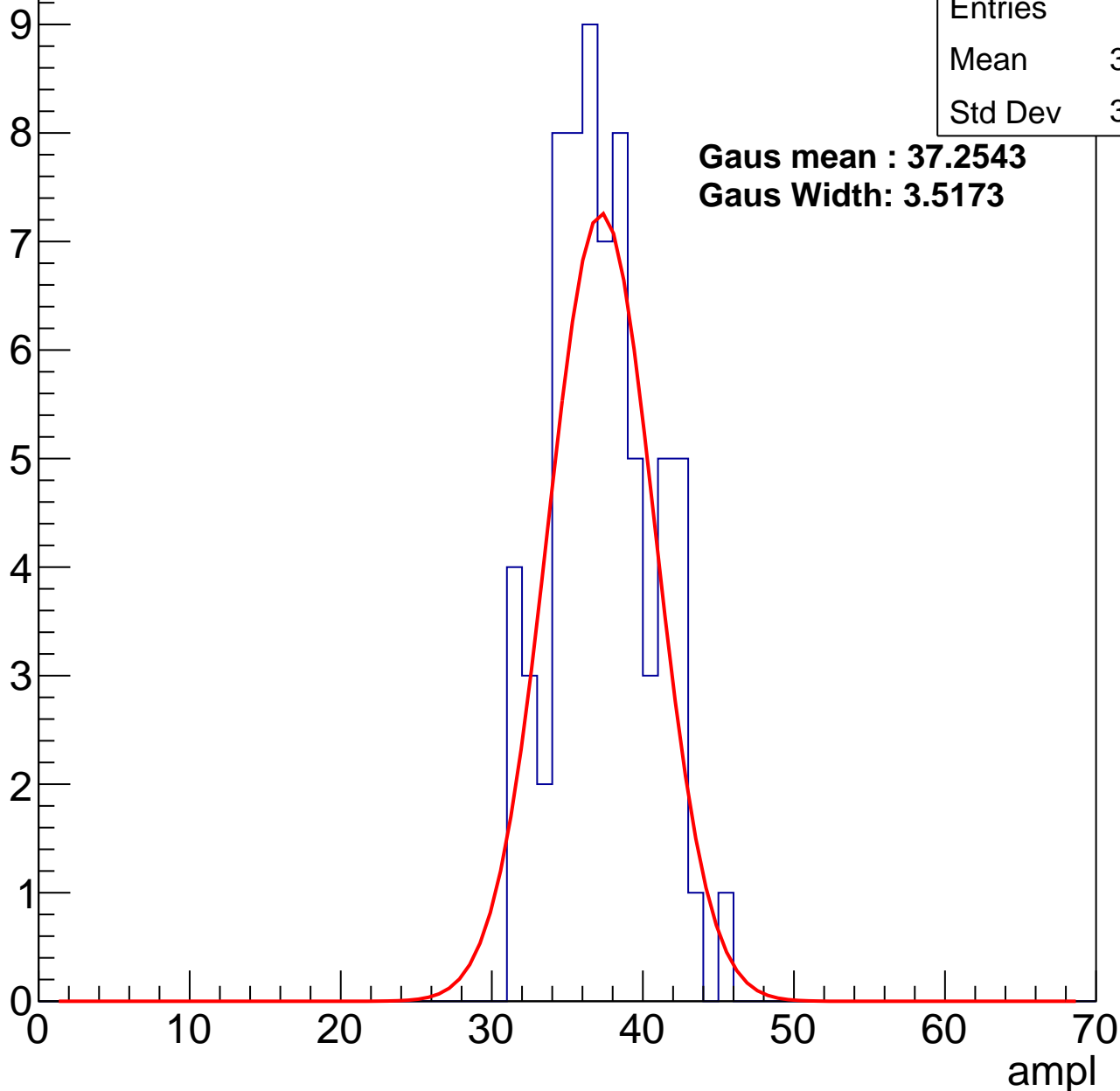
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	36.86
Std Dev	3.236

**Gaus mean : 37.2543**

**Gaus Width: 3.5173**



# B1L101S, U11-ch79, adc2

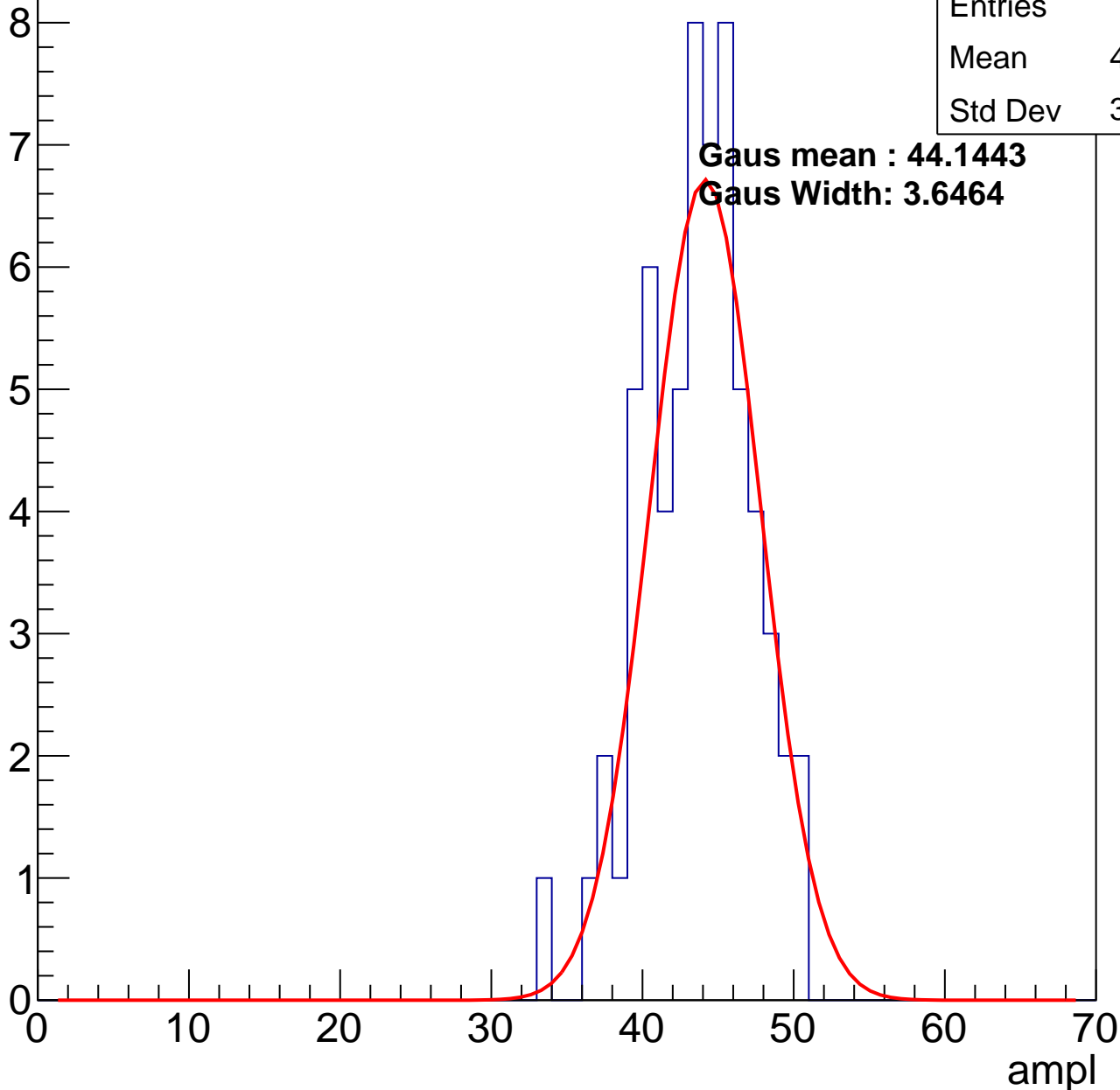
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	43.16
Std Dev	3.519

**Gaus mean : 44.1443**

**Gaus Width: 3.6464**

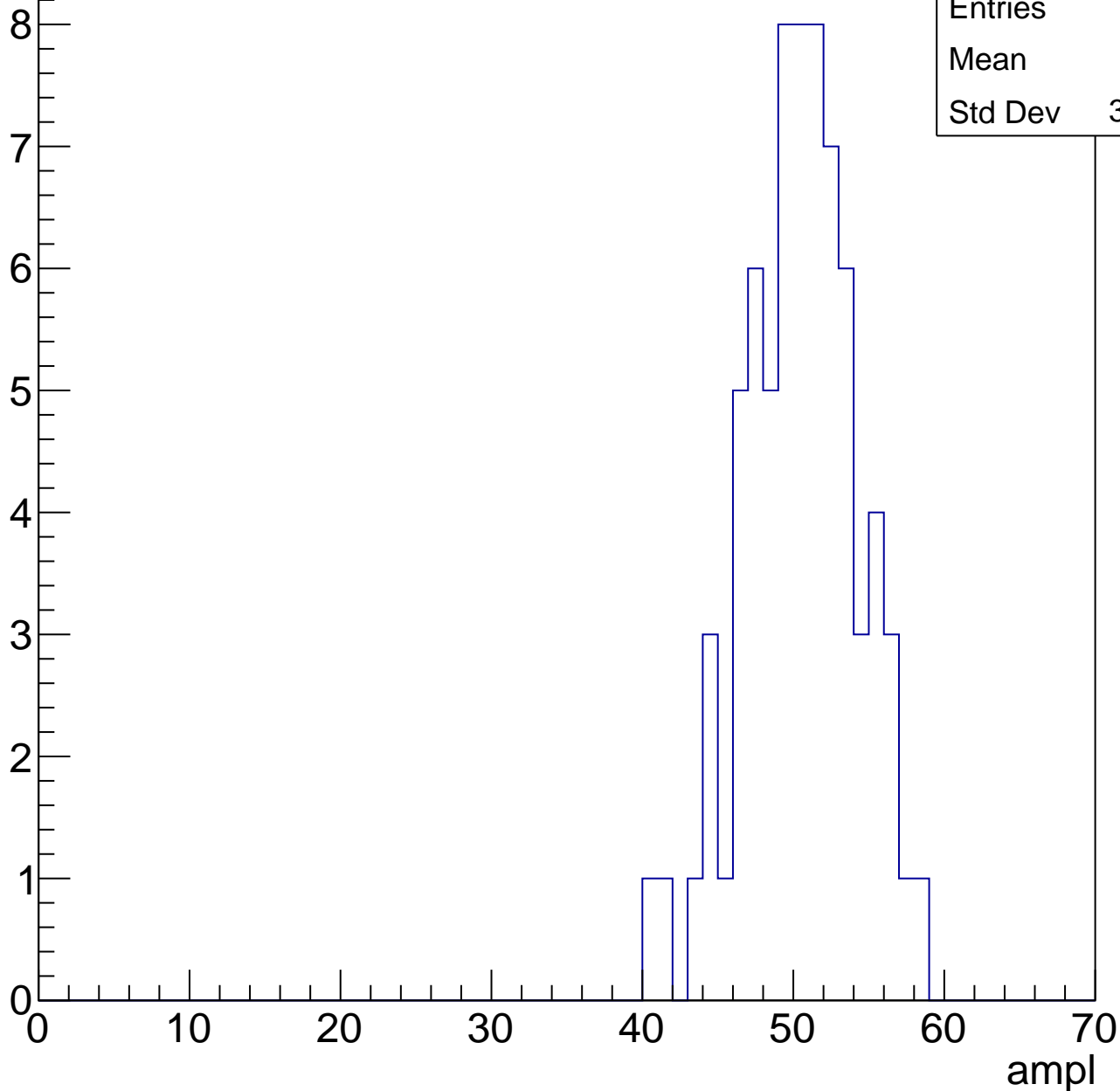


# B1L101S, U11-ch79, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

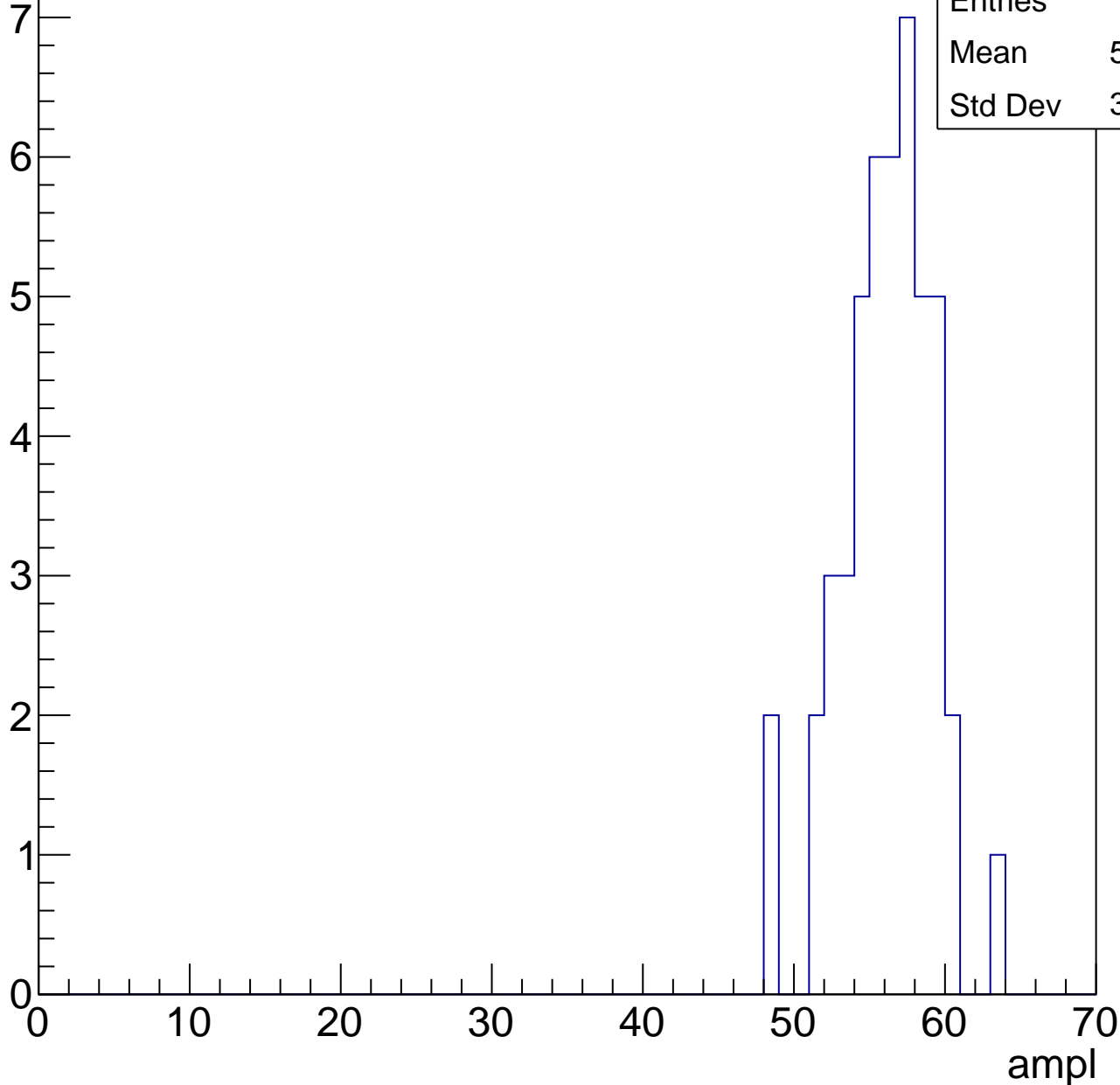
Entries	72
Mean	50
Std Dev	3.697



# B1L101S, U11-ch79, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

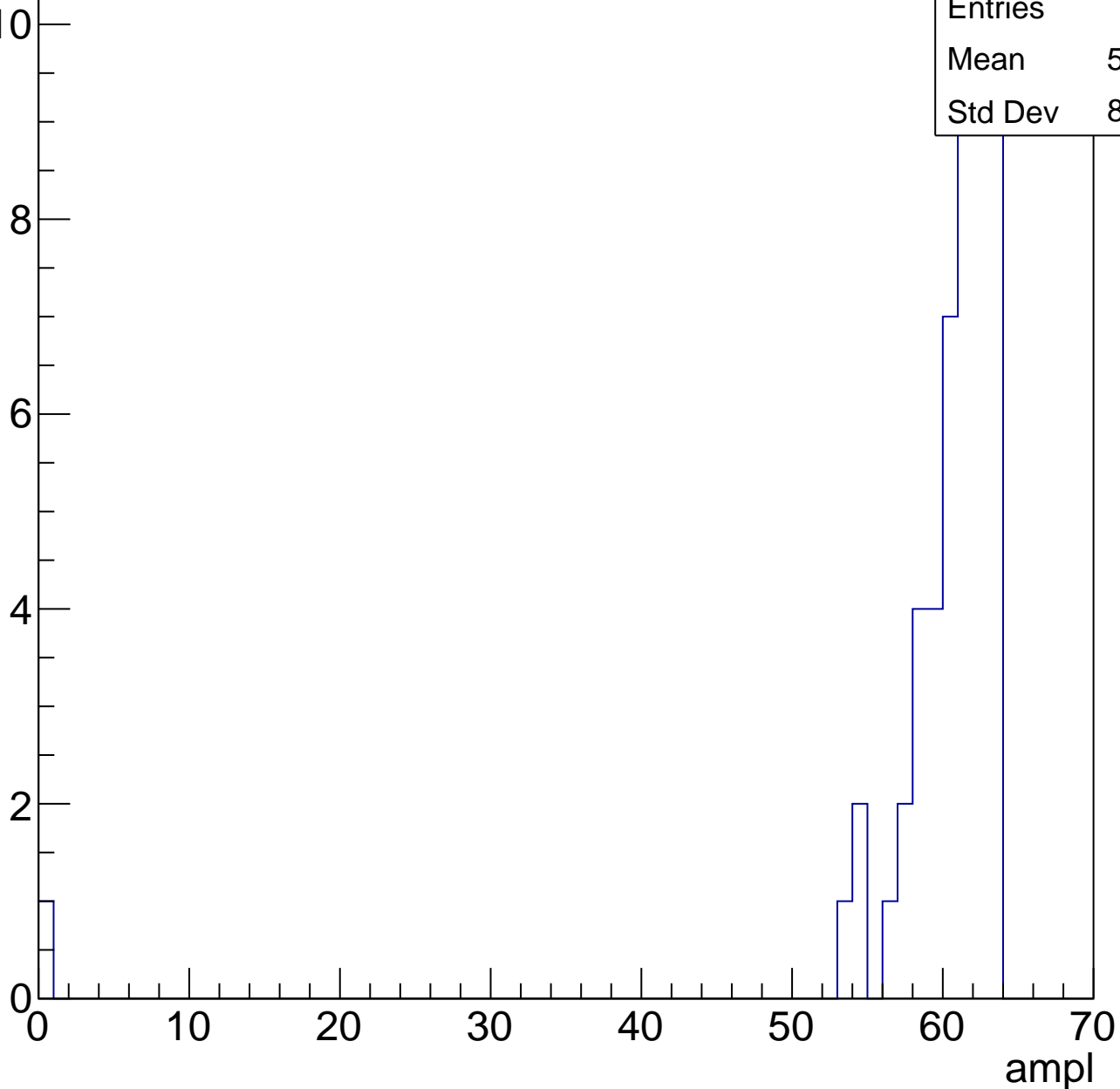


# B1L101S, U11-ch79, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

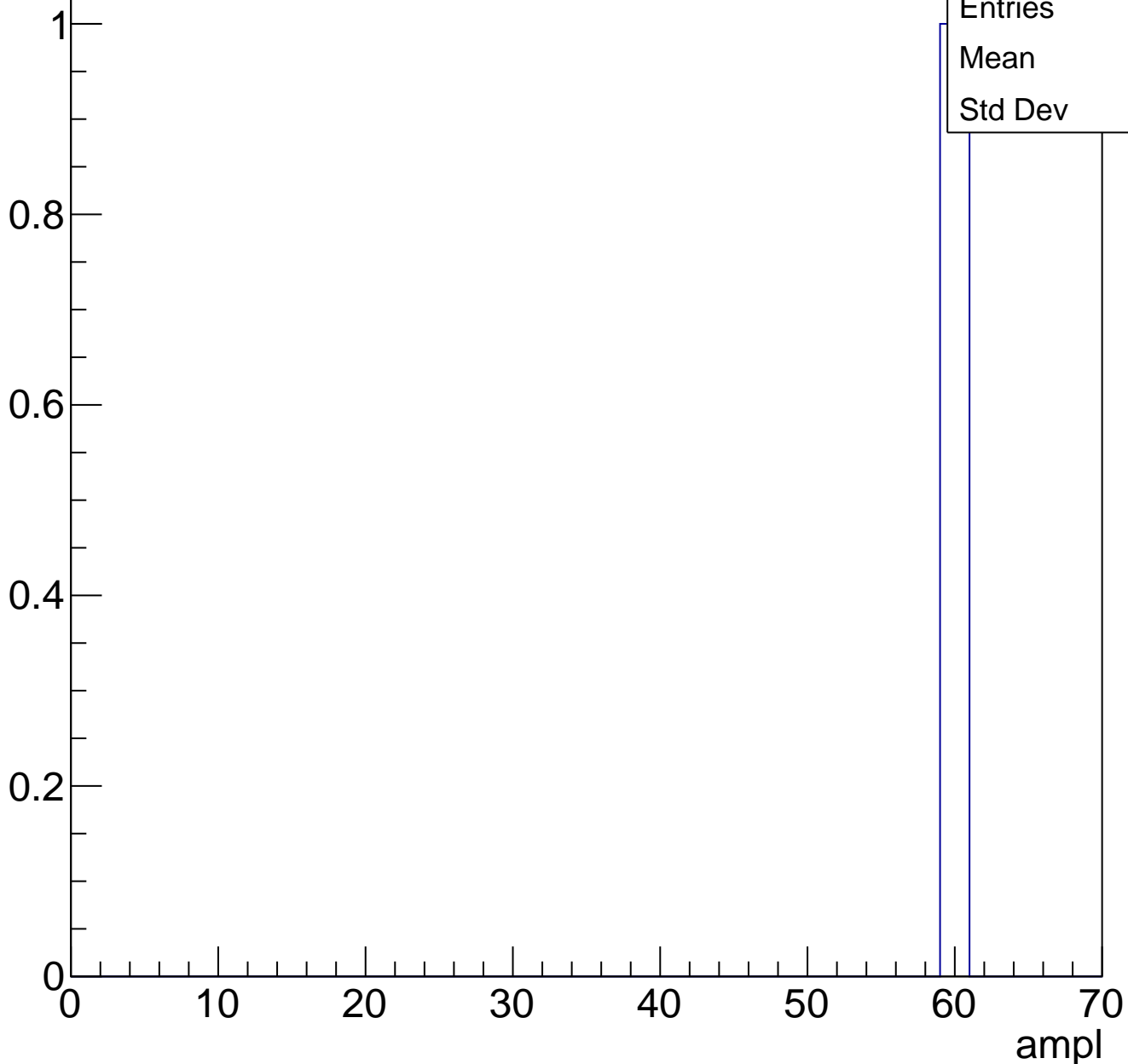
Entries	51
Mean	59.14
Std Dev	8.709



# B1L101S, U11-ch79, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	59.5
Std Dev	0.5



# B1L101S, U11-ch79, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U11-ch80, adc0

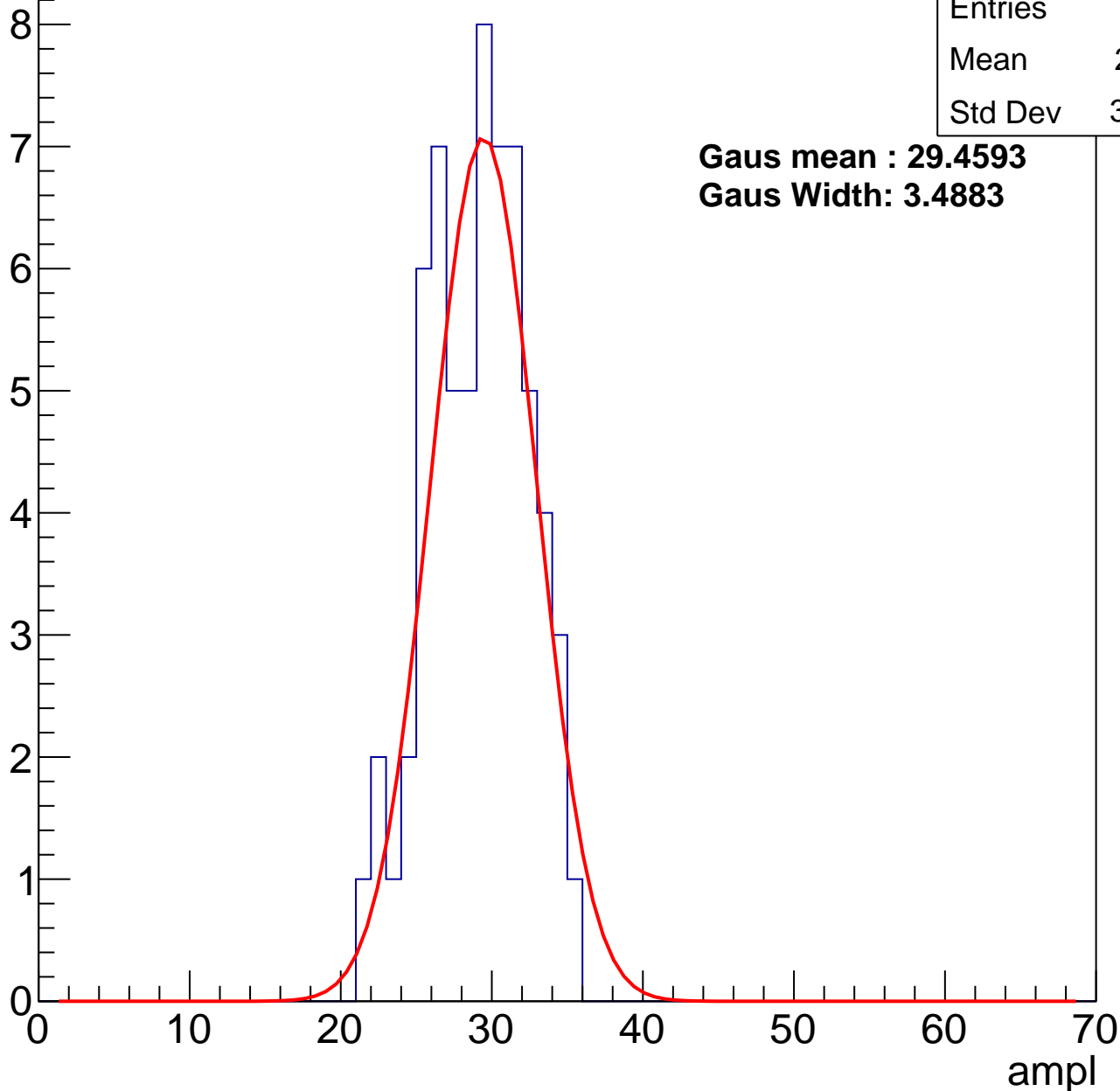
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	28.61
Std Dev	3.253

**Gaus mean : 29.4593**

**Gaus Width: 3.4883**



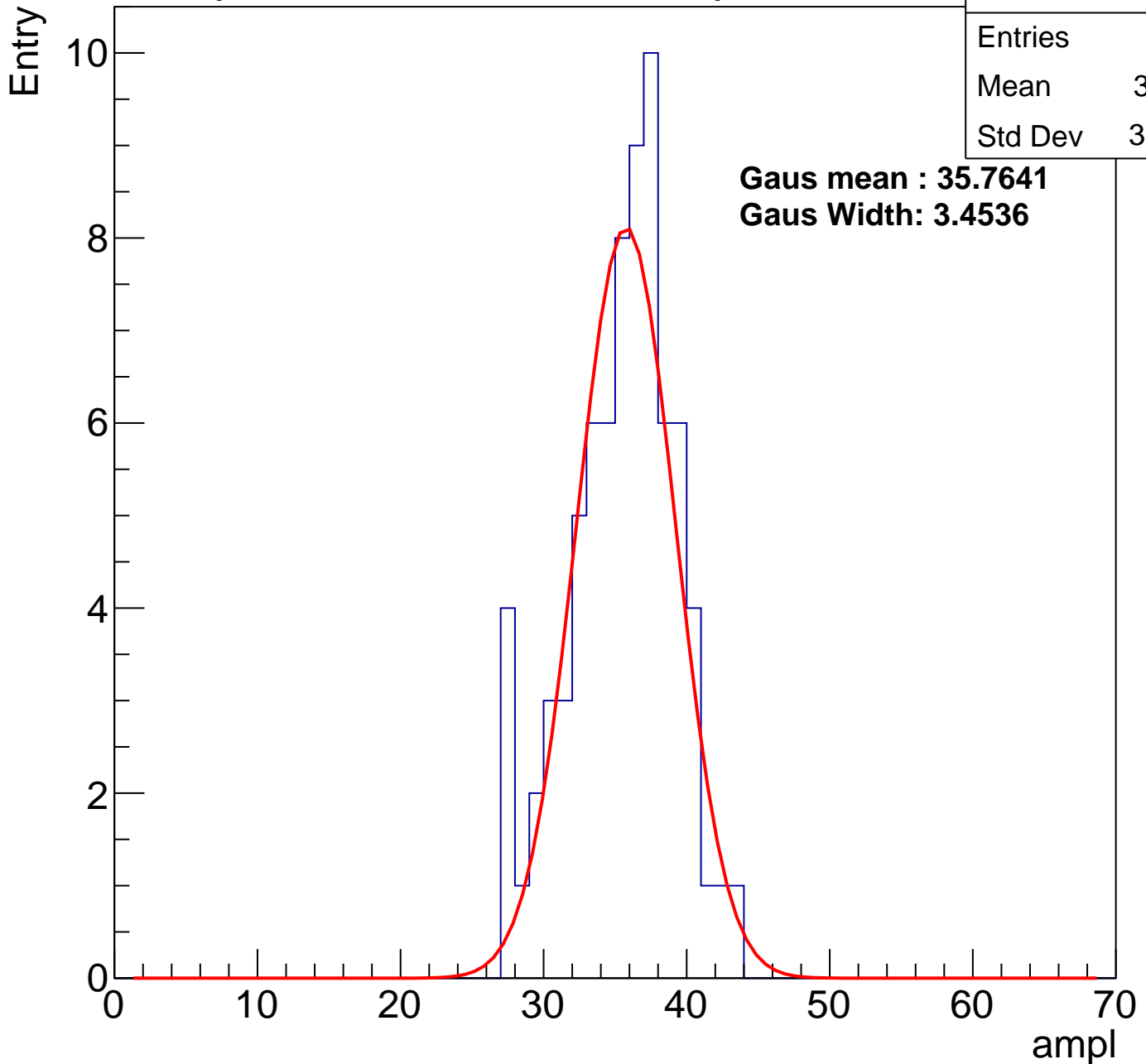
# B1L101S, U11-ch80, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	76
Mean	35.01
Std Dev	3.669

**Gaus mean : 35.7641**

**Gaus Width: 3.4536**



# B1L101S, U11-ch80, adc2

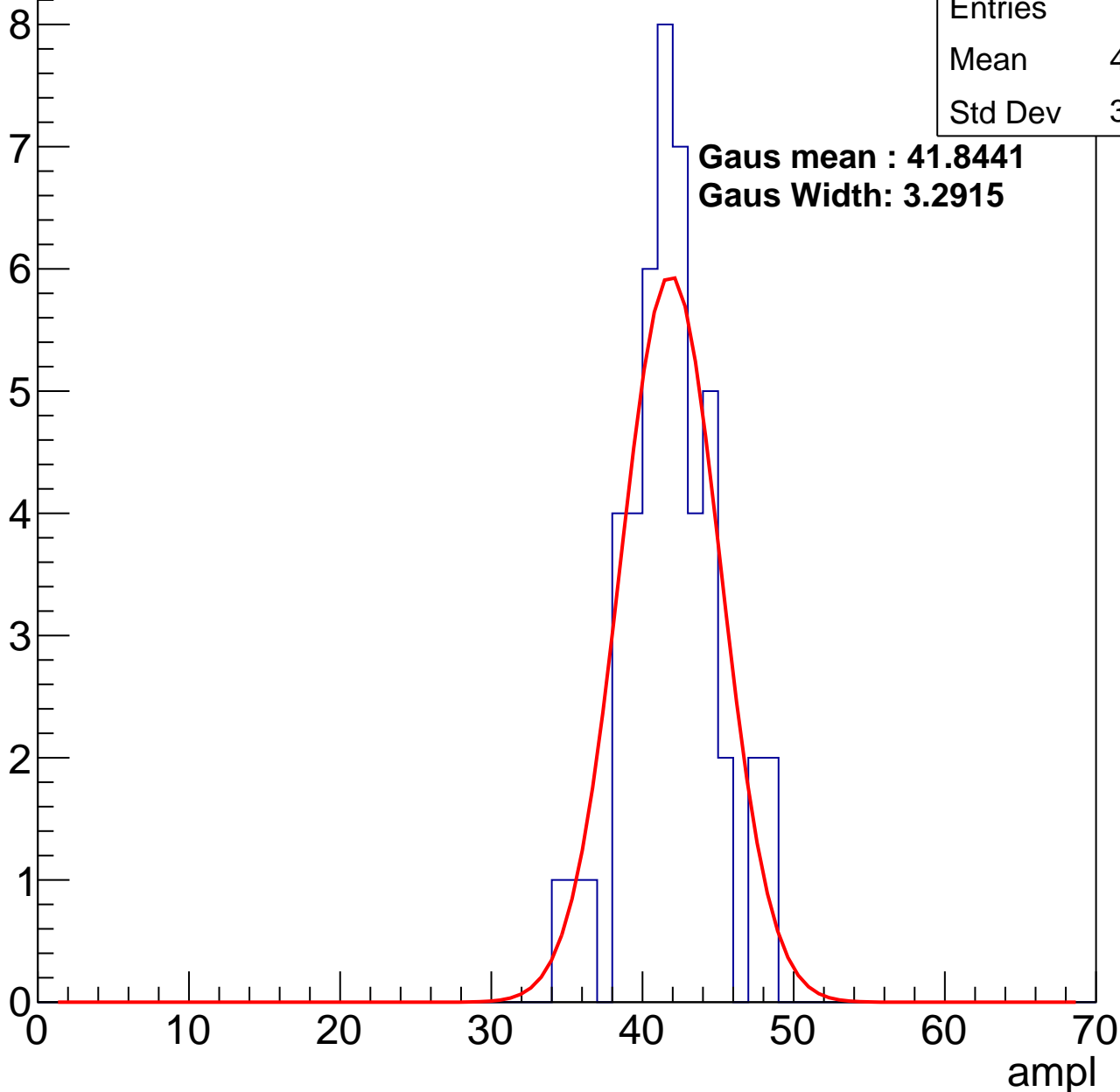
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	47
Mean	41.43
Std Dev	3.023

**Gaus mean : 41.8441**

**Gaus Width: 3.2915**



# B1L101S, U11-ch80, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	80
Mean	48.21
Std Dev	3.71

Entry

10

8

6

4

2

0

0

10

20

30

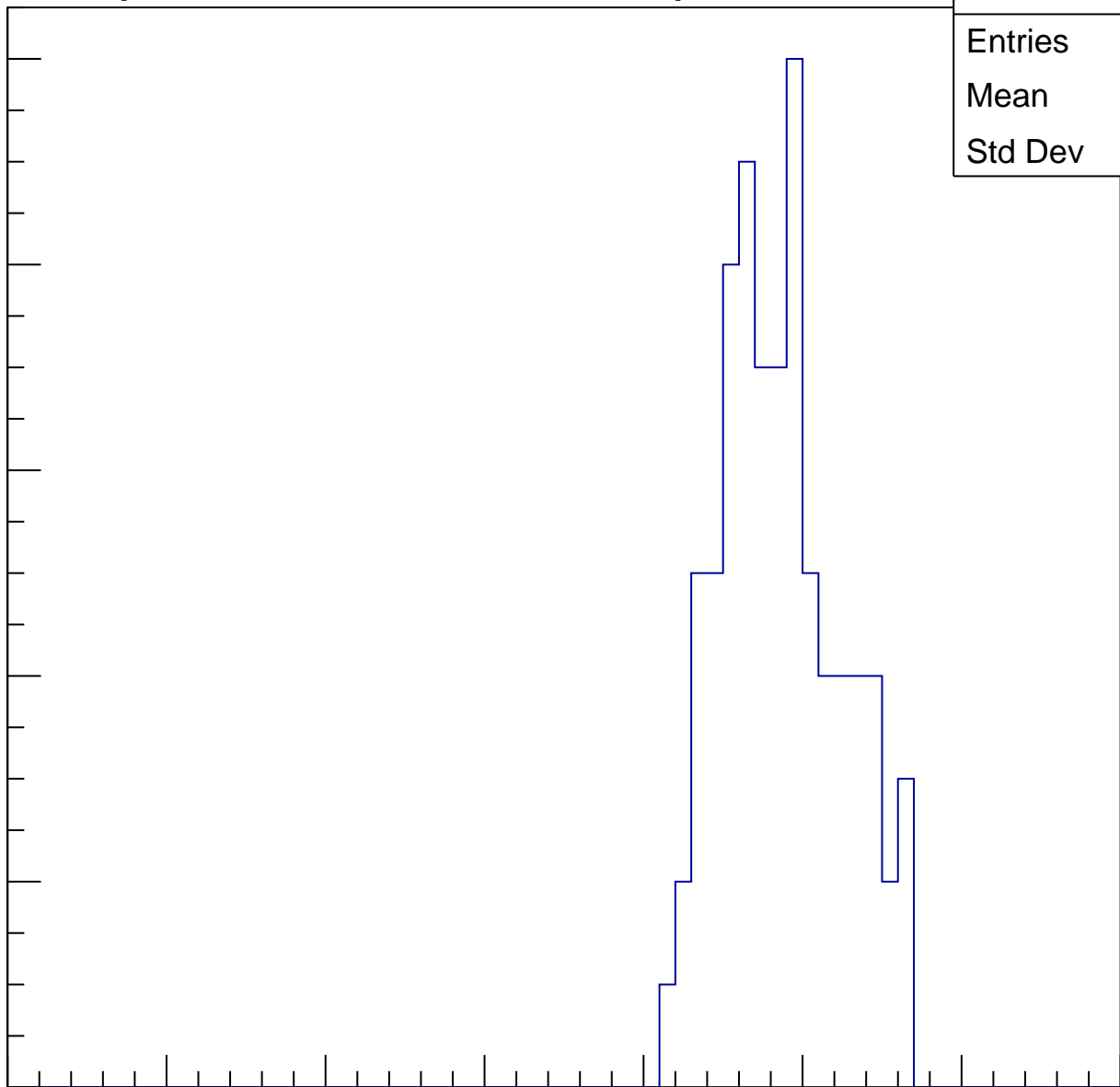
40

50

60

70

ampl

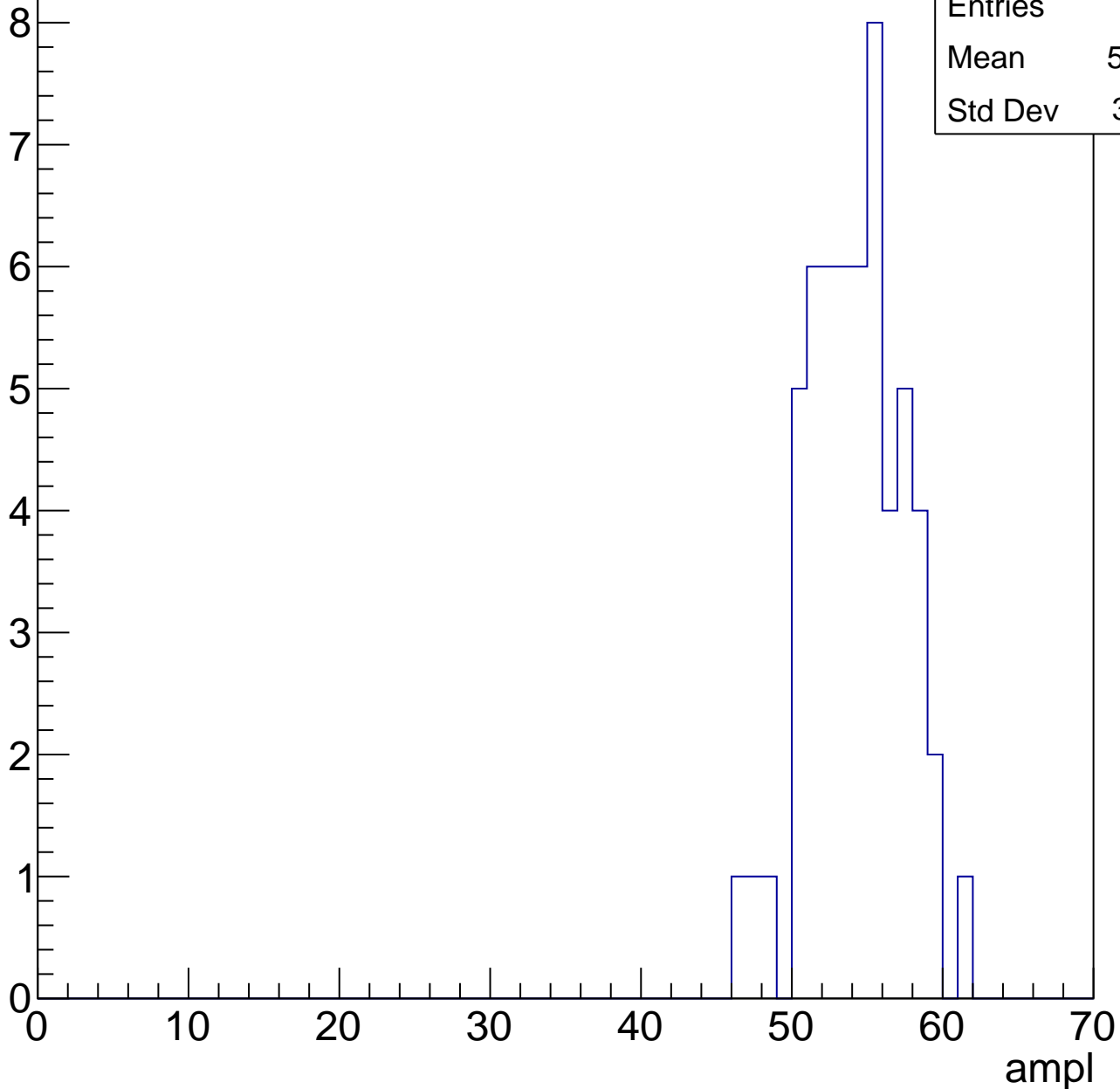


# B1L101S, U11-ch80, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

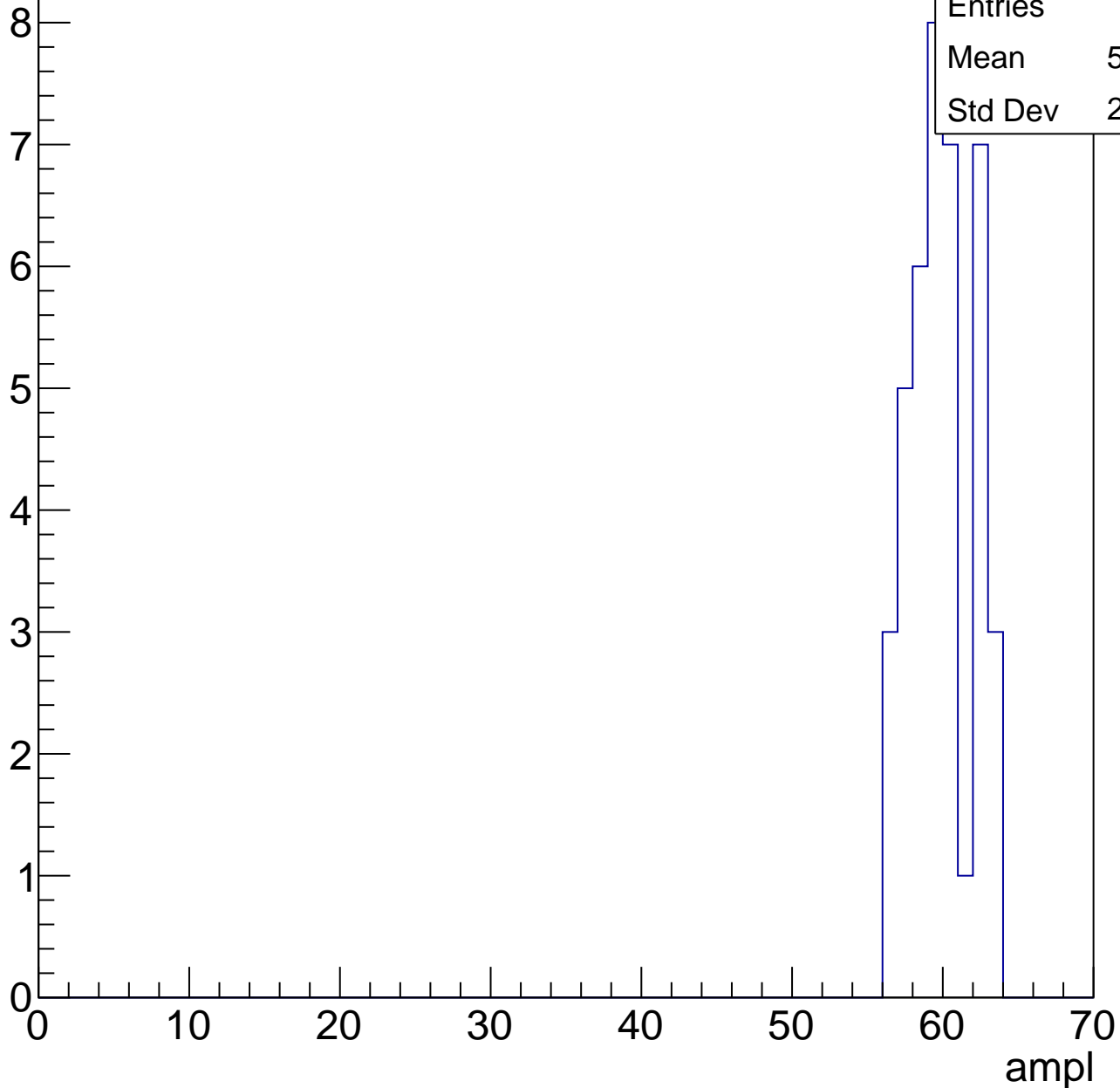
Entries	56
Mean	53.77
Std Dev	3.111



# B1L101S, U11-ch80, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

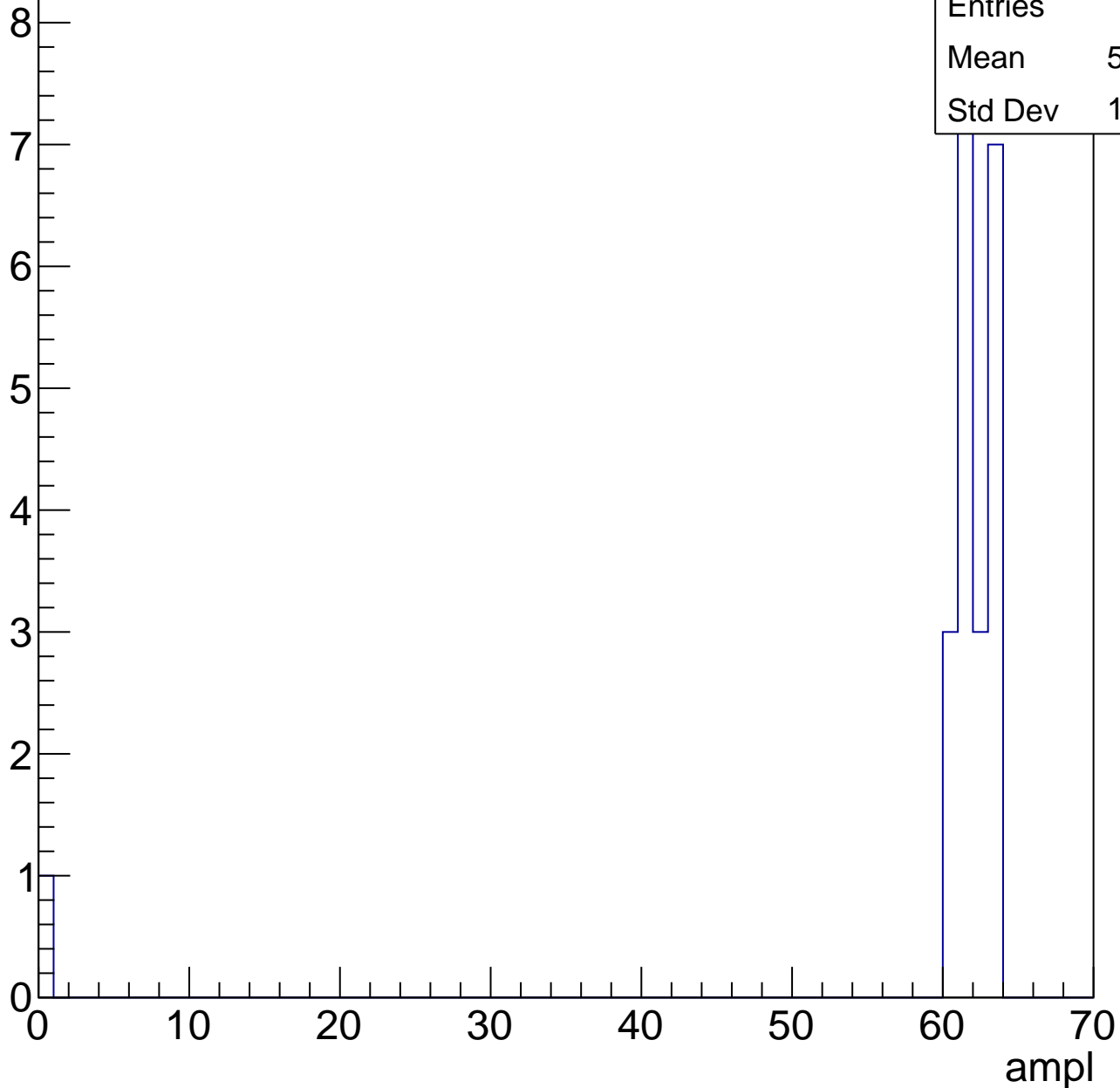
Entry



# B1L101S, U11-ch80, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch80, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U11-ch81, adc0

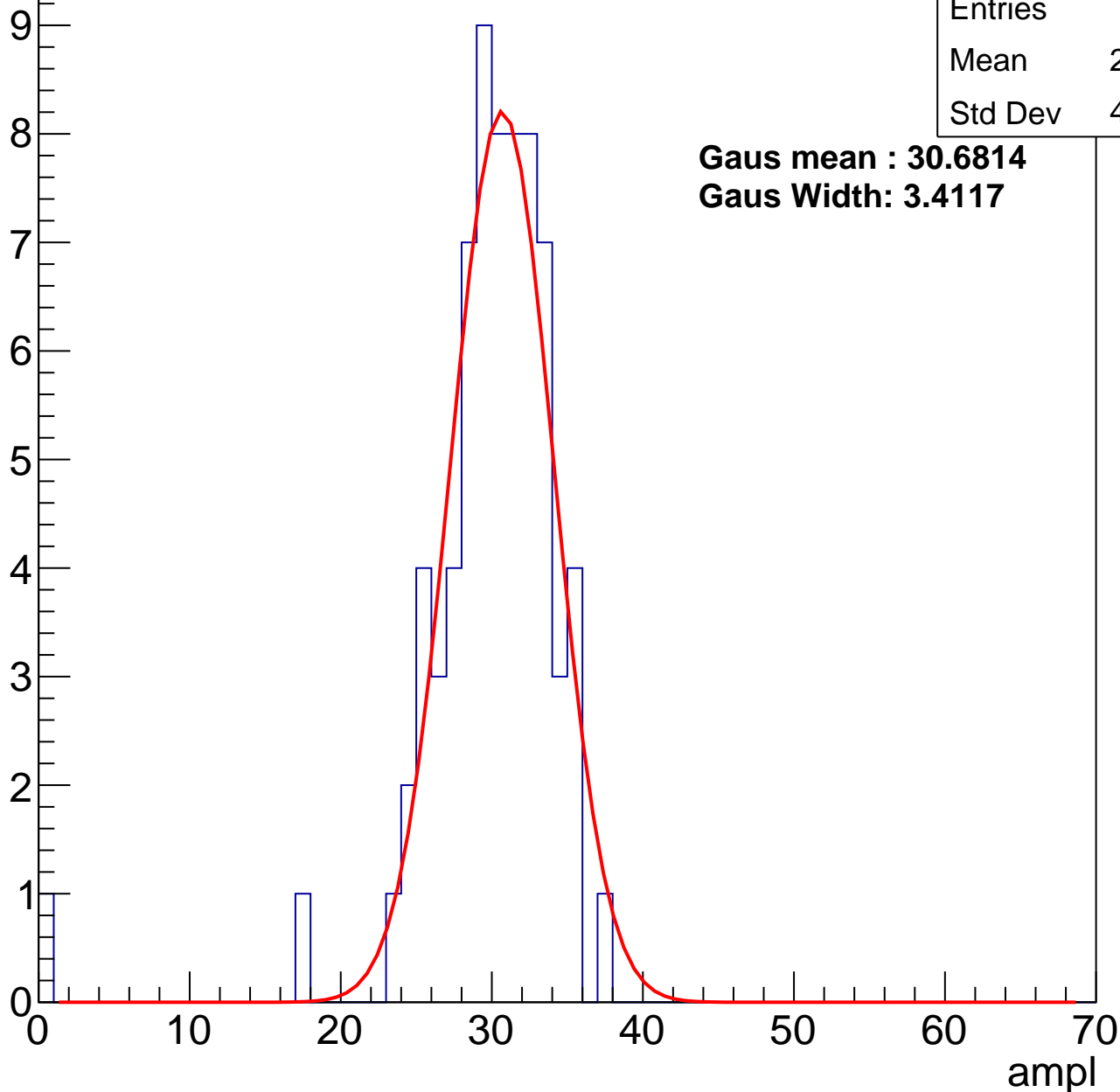
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	29.37
Std Dev	4.868

**Gaus mean : 30.6814**

**Gaus Width: 3.4117**



# B1L101S, U11-ch81, adc1

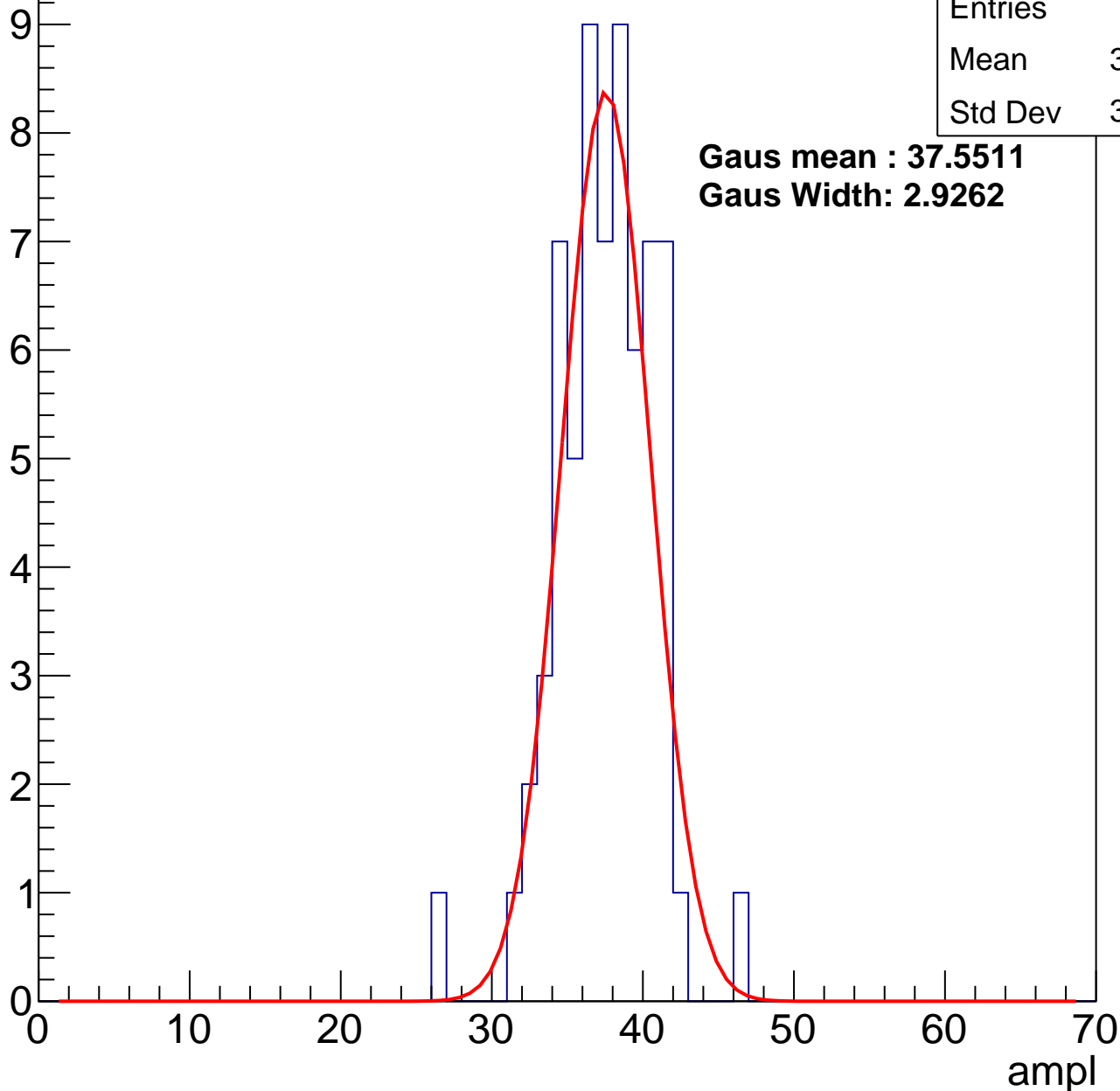
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	37.08
Std Dev	3.164

**Gaus mean : 37.5511**

**Gaus Width: 2.9262**



# B1L101S, U11-ch81, adc2

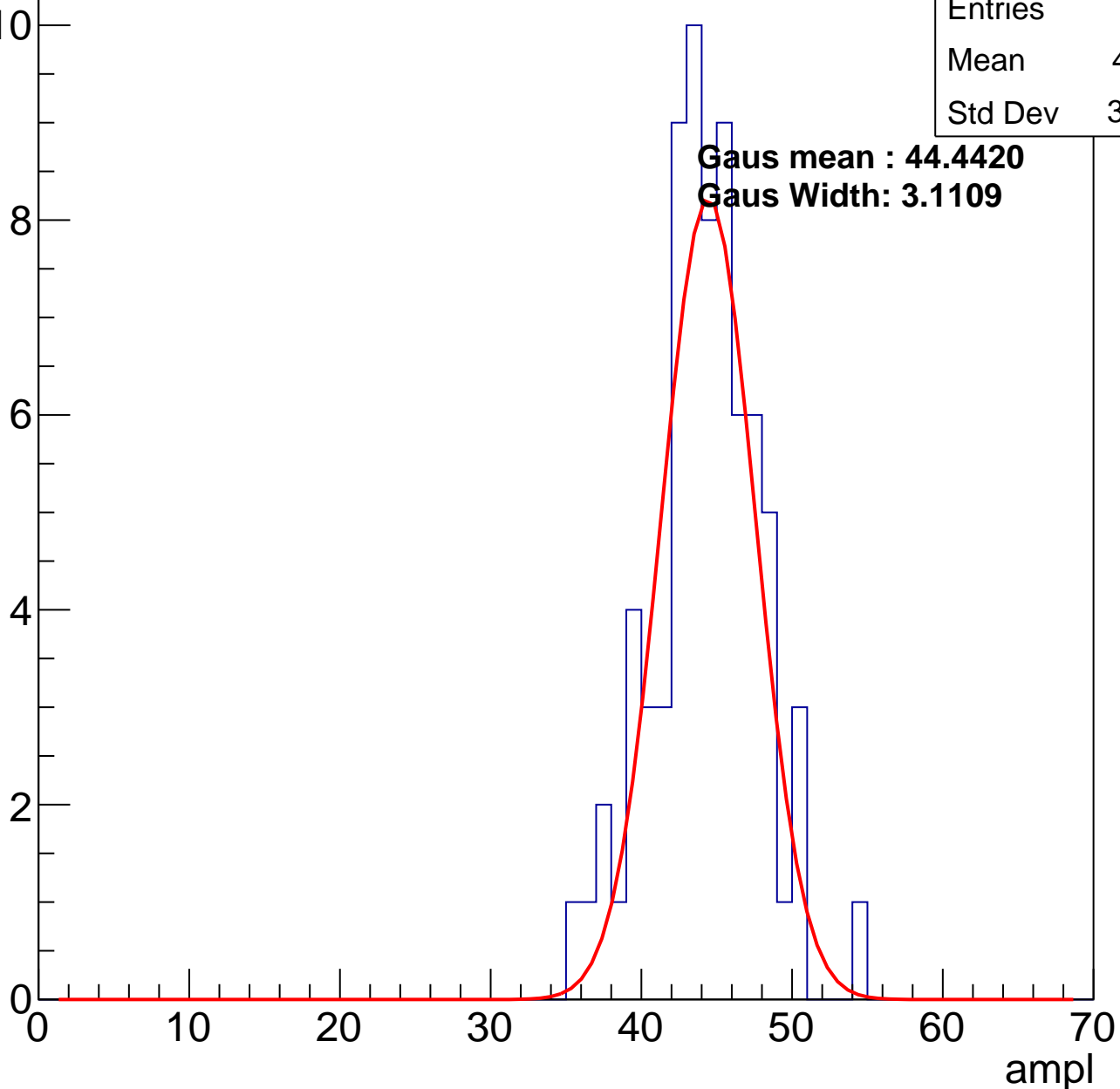
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	73
Mean	43.81
Std Dev	3.506

Entry

**Gaus mean : 44.4420**

**Gaus Width: 3.1109**

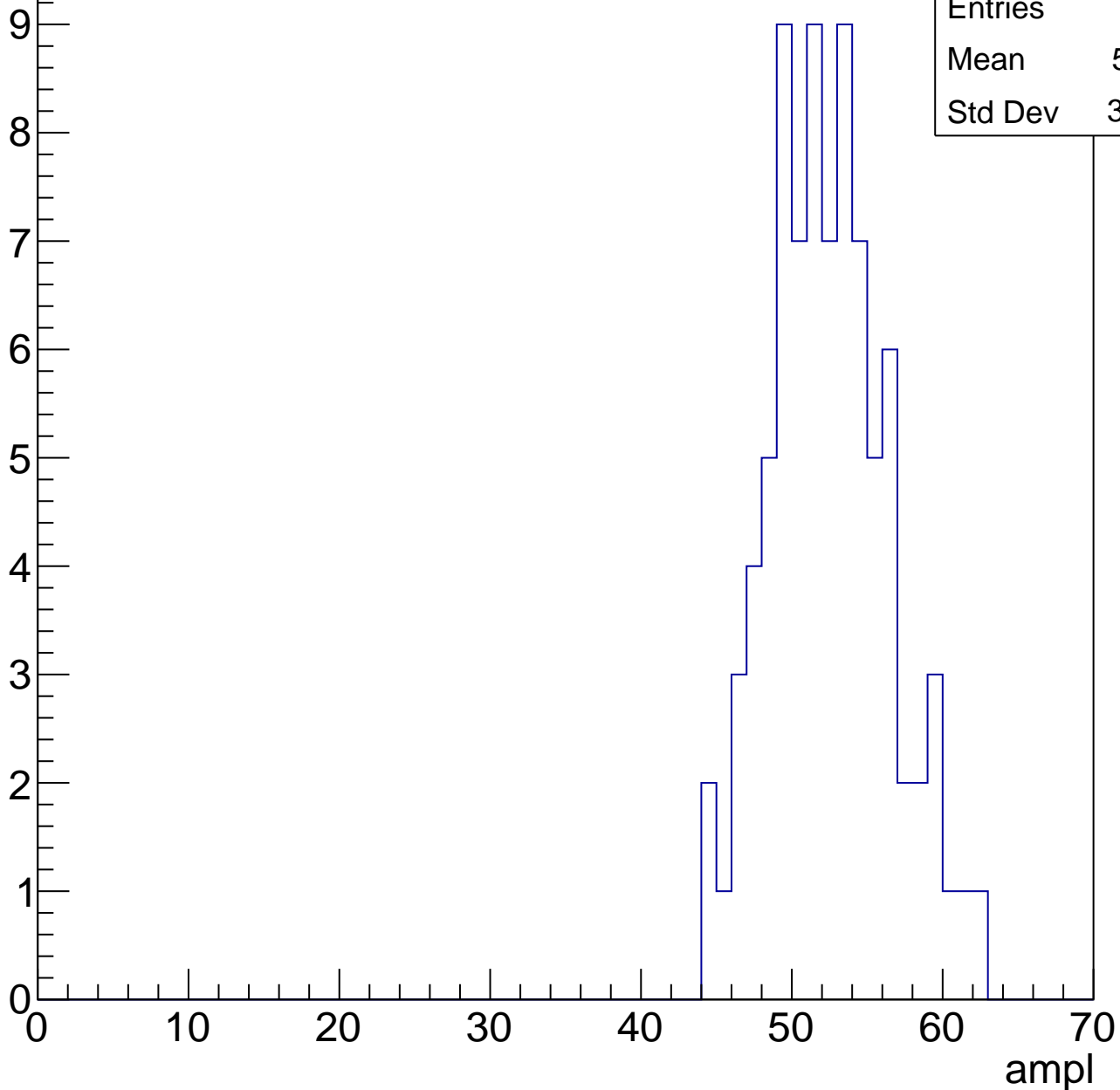


# B1L101S, U11-ch81, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	84
Mean	52.01
Std Dev	3.896

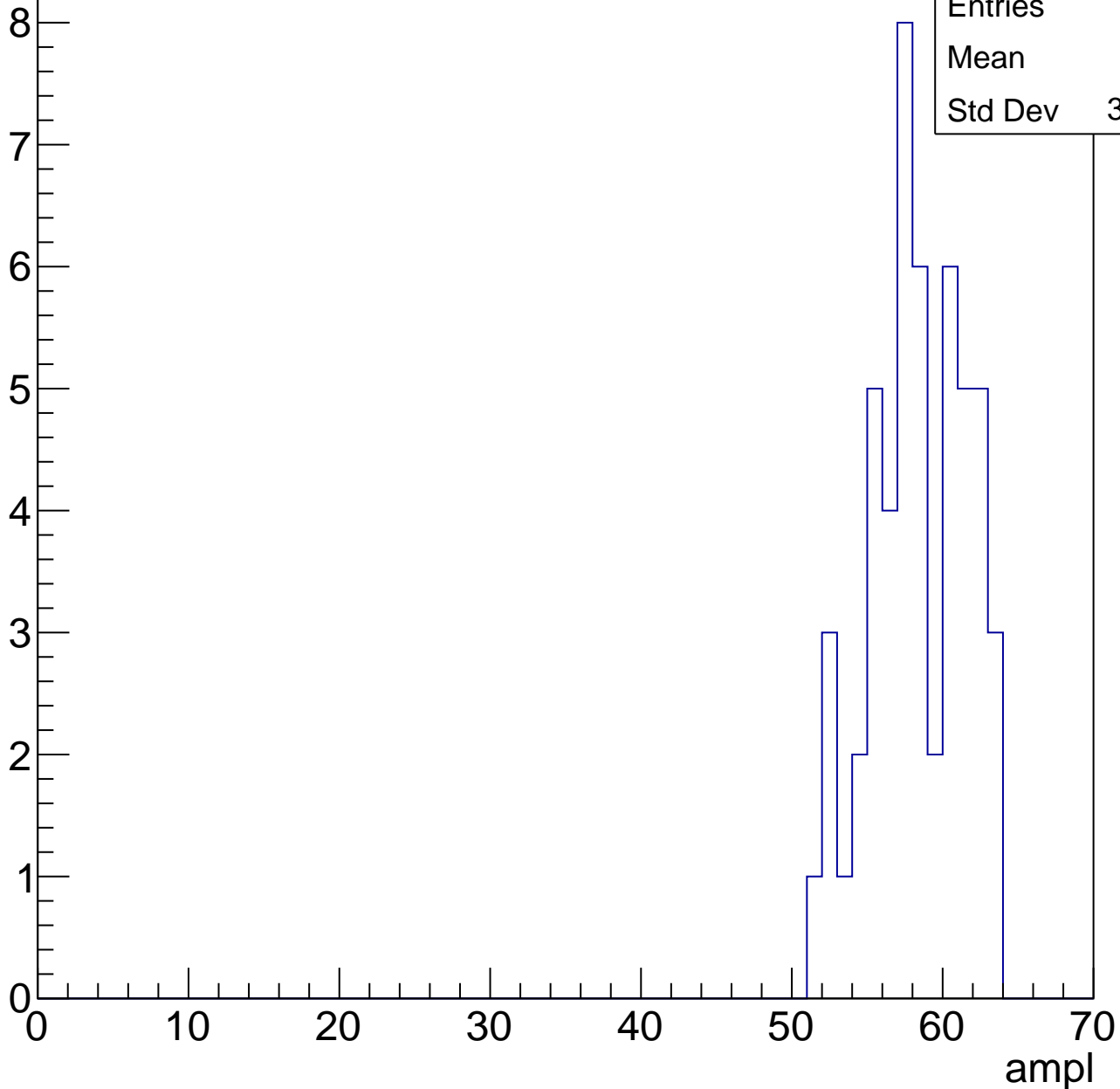


# B1L101S, U11-ch81, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	57.9
Std Dev	3.158

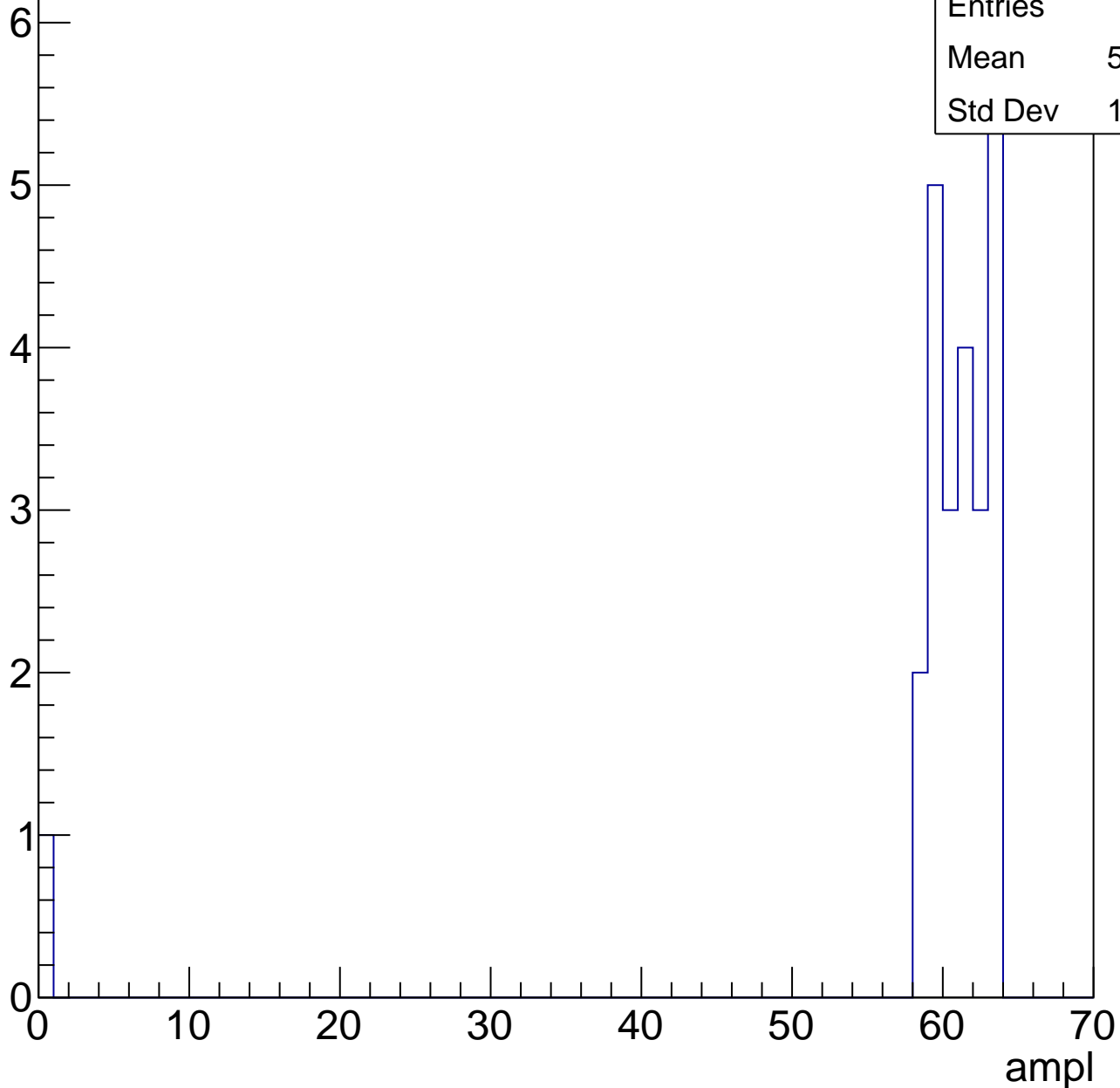


# B1L101S, U11-ch81, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	24
Mean	58.29
Std Dev	12.27



# B1L101S, U11-ch81, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch81, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U11-ch82, adc0

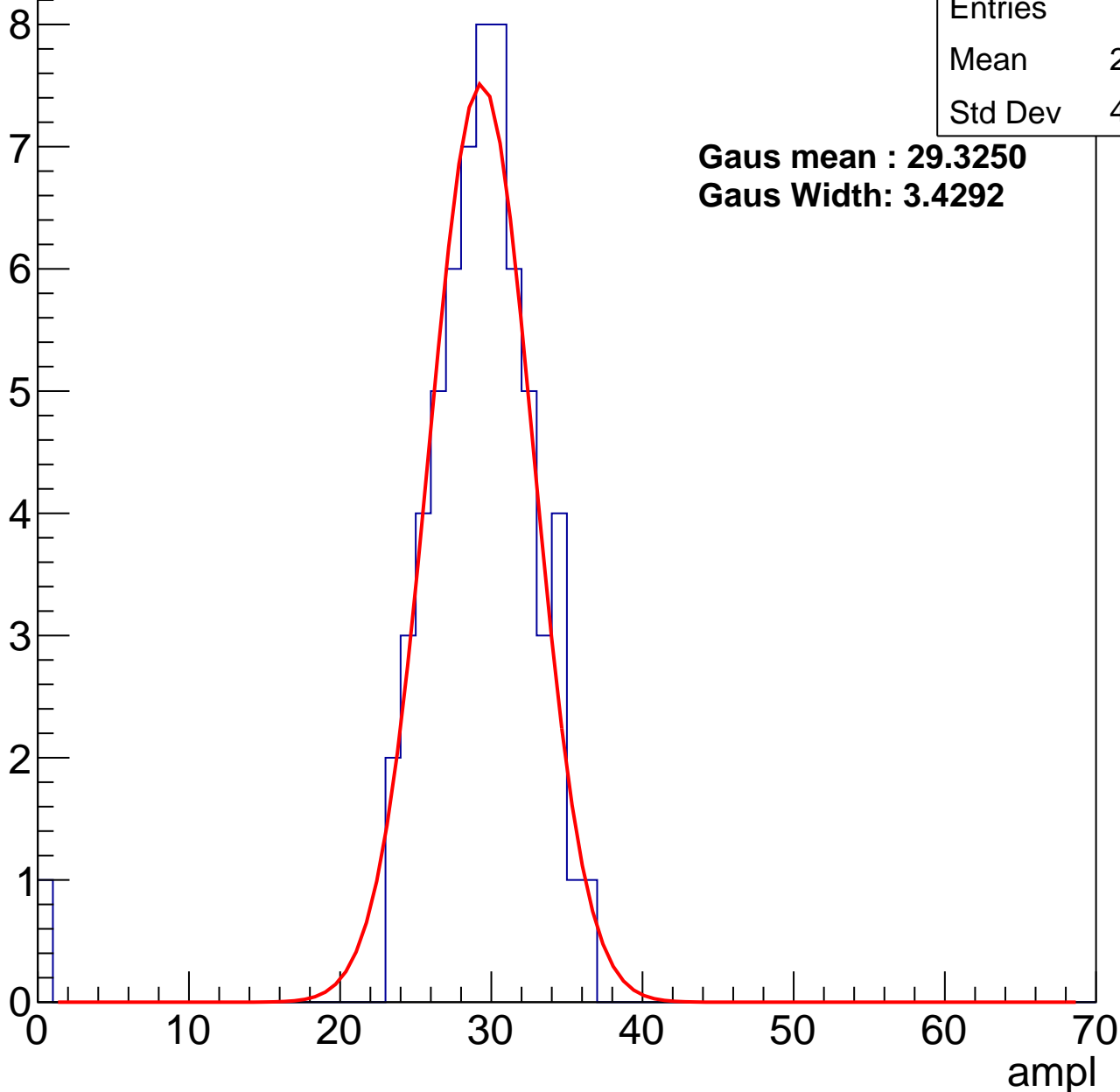
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	28.59
Std Dev	4.723

**Gaus mean : 29.3250**

**Gaus Width: 3.4292**



# B1L101S, U11-ch82, adc1

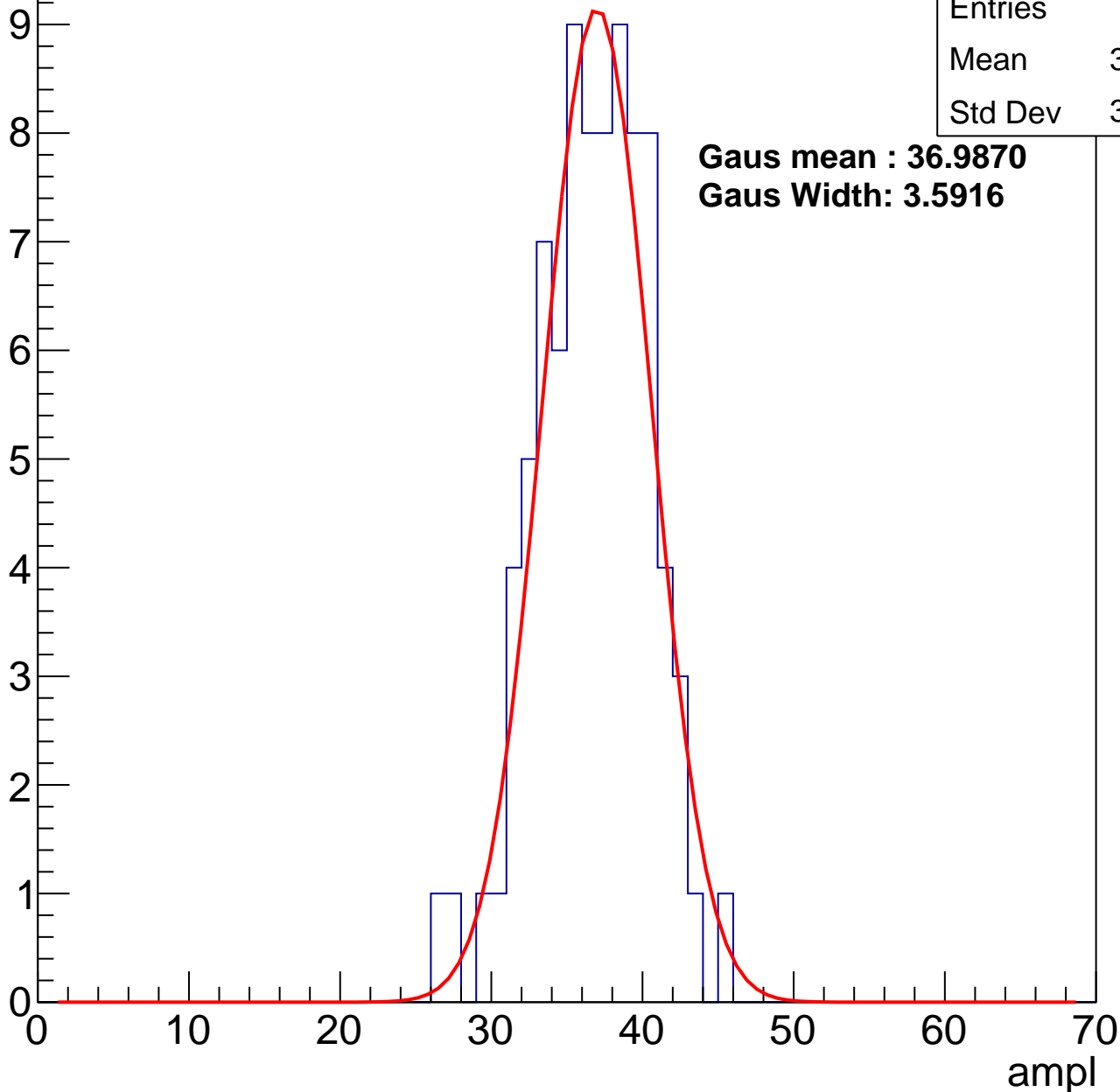
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	85
Mean	36.26
Std Dev	3.627

**Gaus mean : 36.9870**

**Gaus Width: 3.5916**



# B1L101S, U11-ch82, adc2

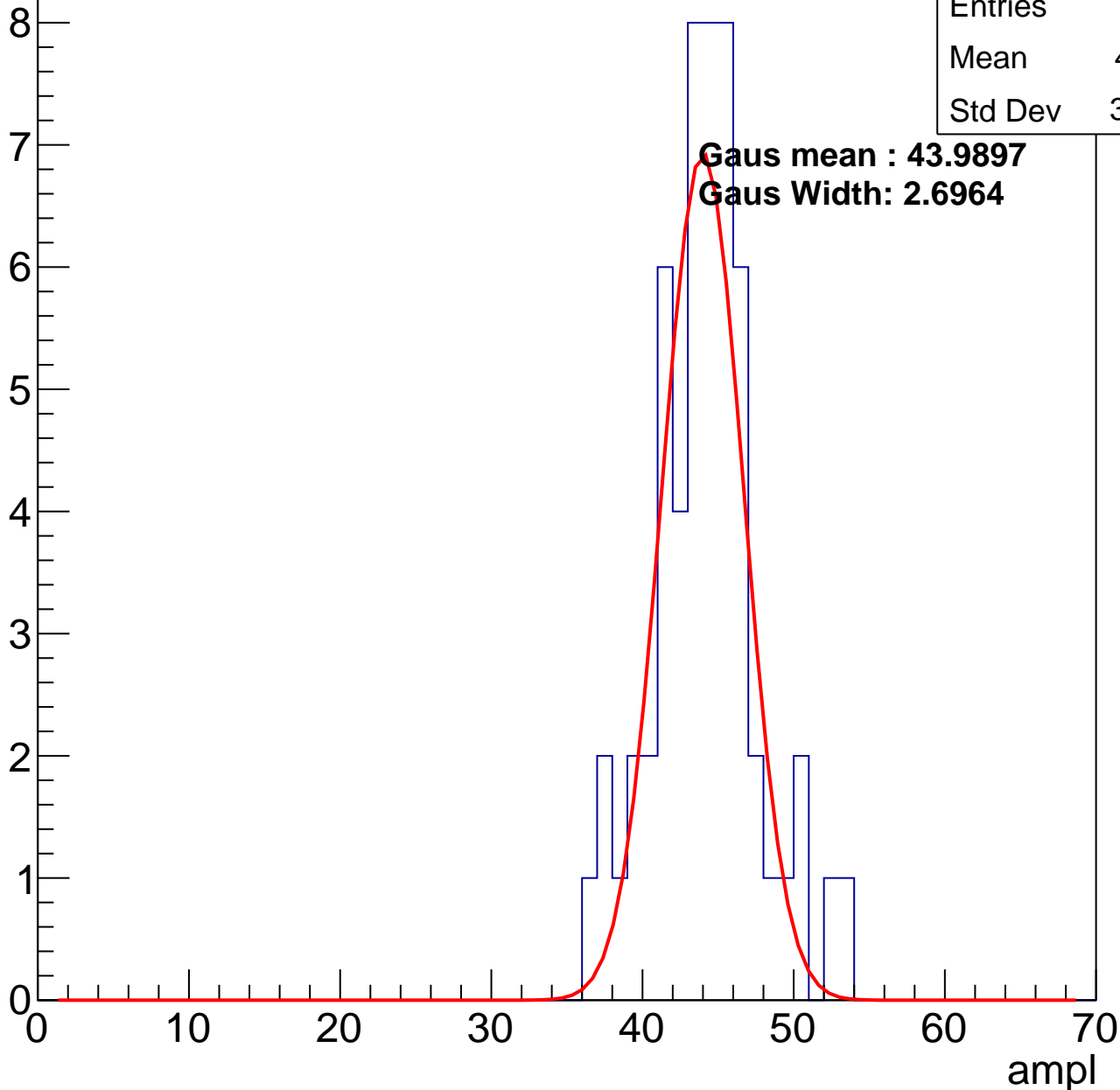
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	43.71
Std Dev	3.437

**Gaus mean : 43.9897**

**Gaus Width: 2.6964**

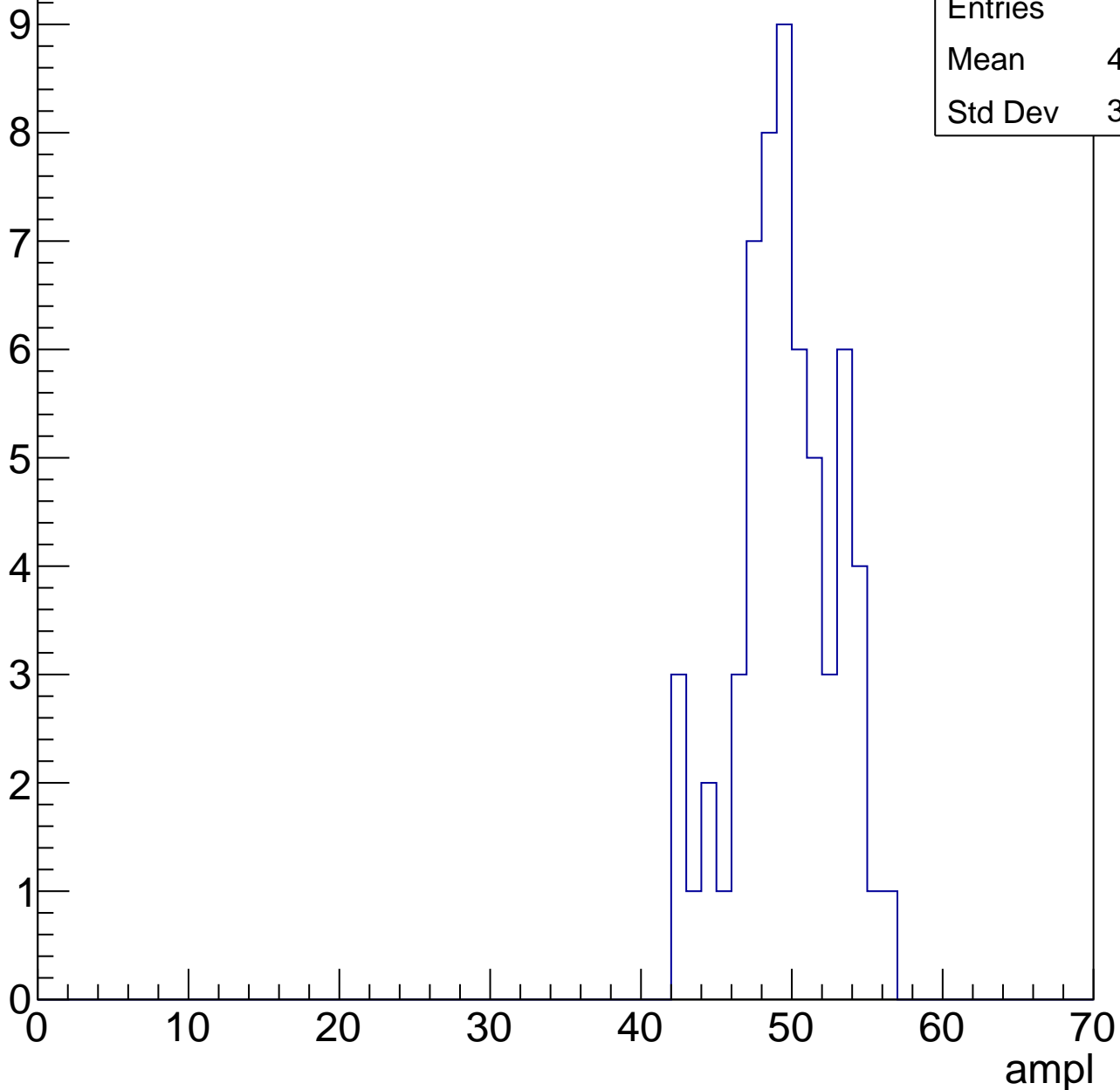


# B1L101S, U11-ch82, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	49.17
Std Dev	3.277

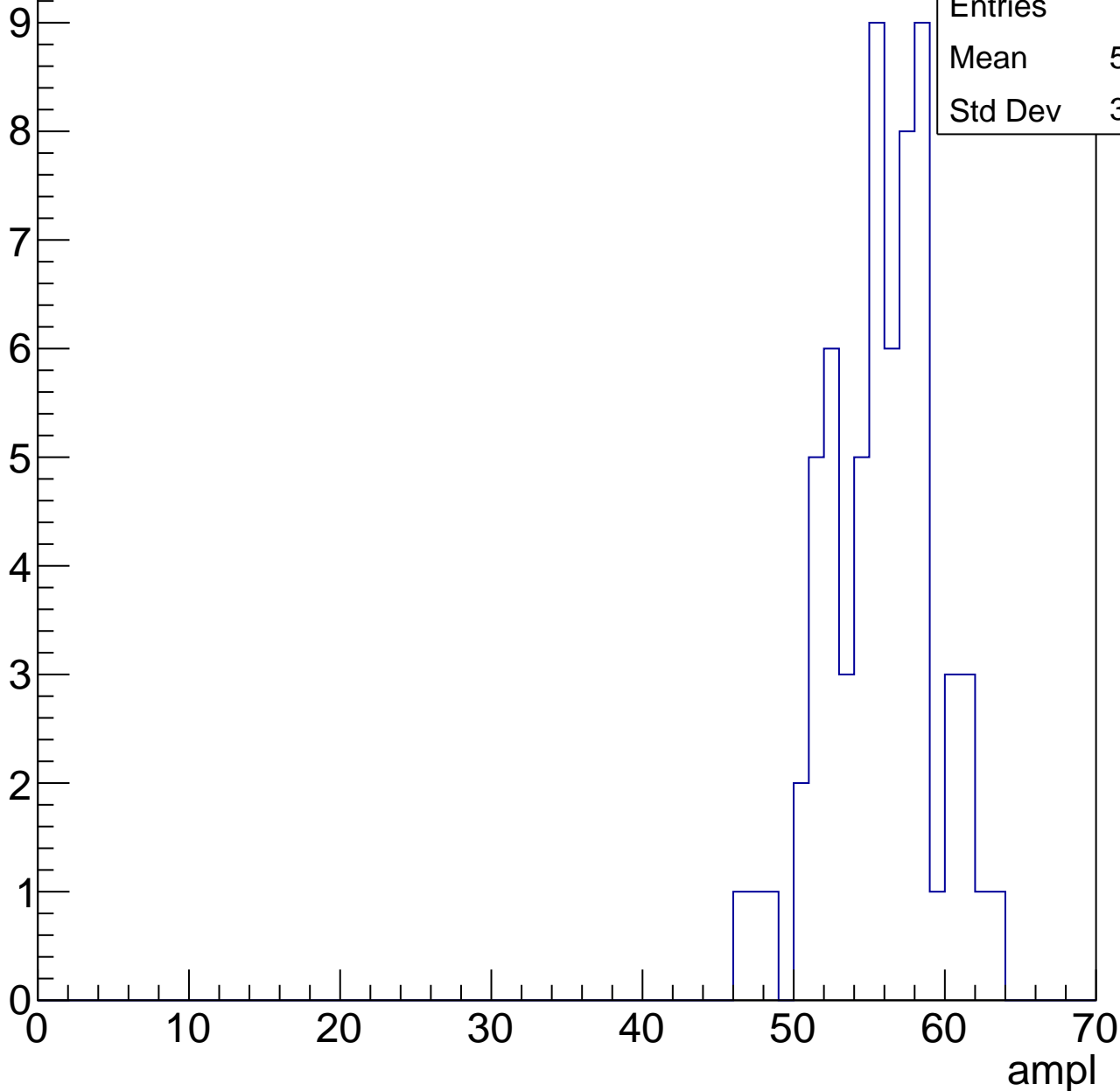


# B1L101S, U11-ch82, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	55.28
Std Dev	3.554



# B1L101S, U11-ch82, adc5

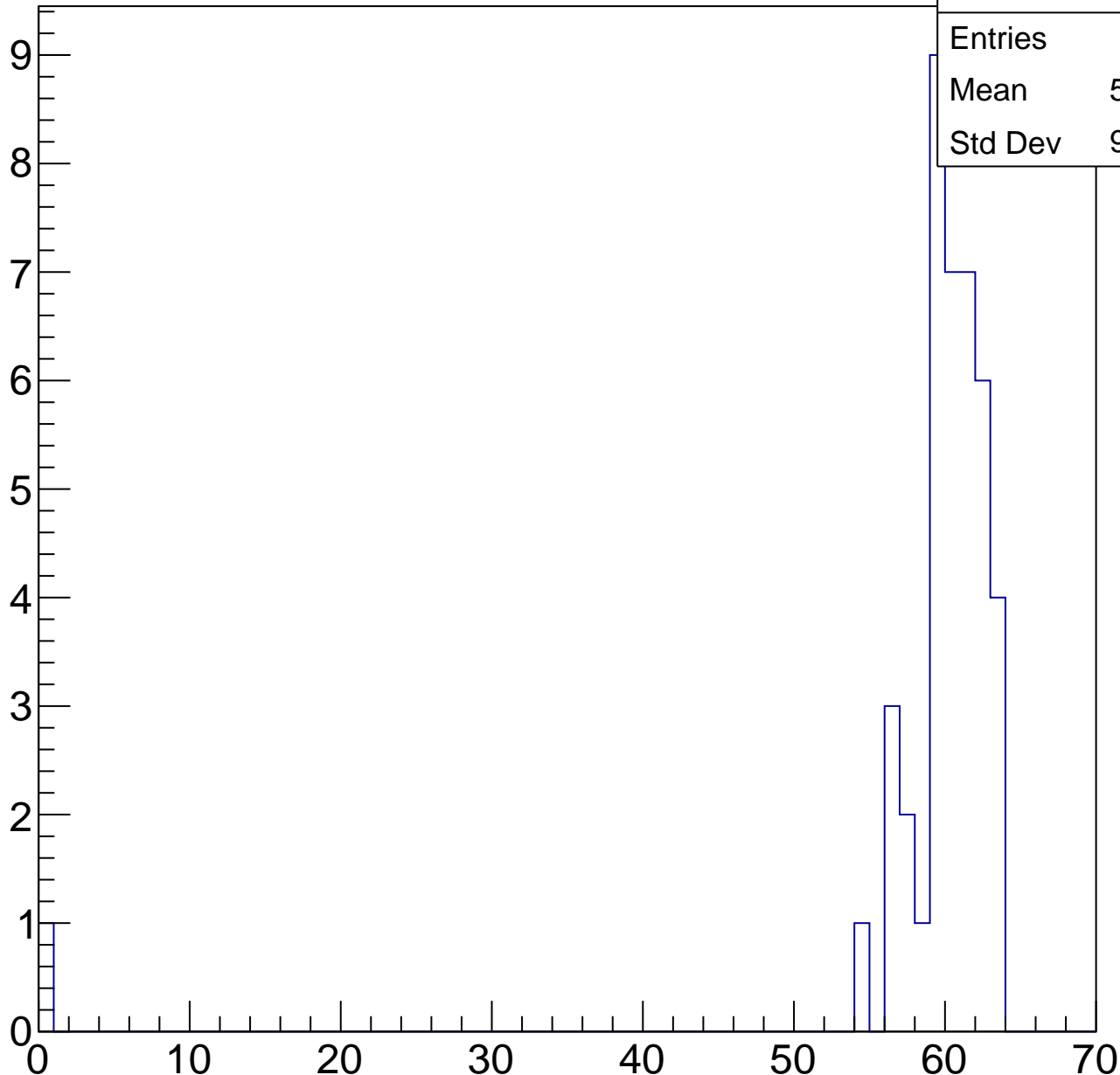
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	41
Mean	58.44
Std Dev	9.477

ampl



# B1L101S, U11-ch82, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch82, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U11-ch83, adc0

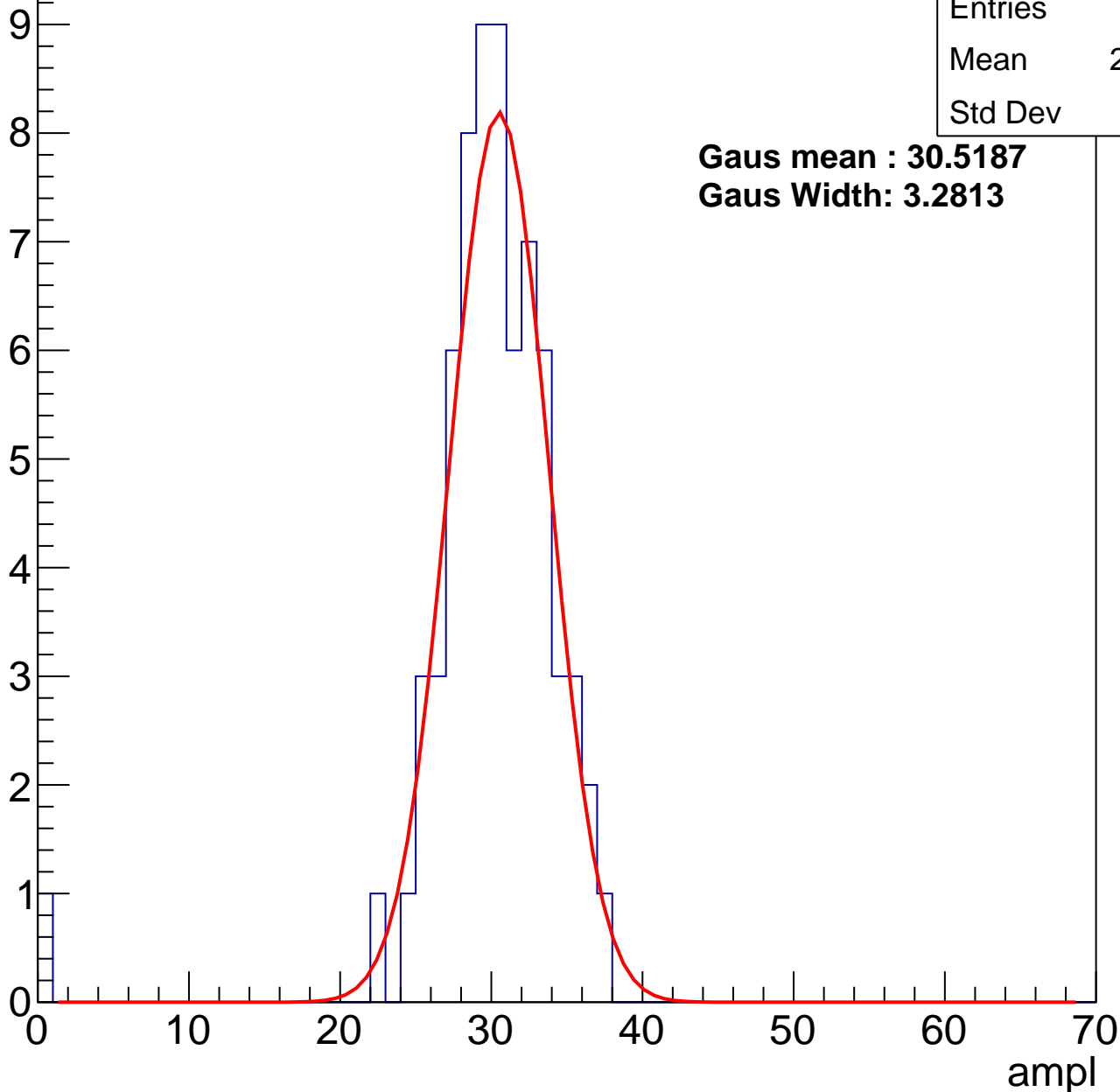
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	29.57
Std Dev	4.72

**Gaus mean : 30.5187**

**Gaus Width: 3.2813**



# B1L101S, U11-ch83, adc1

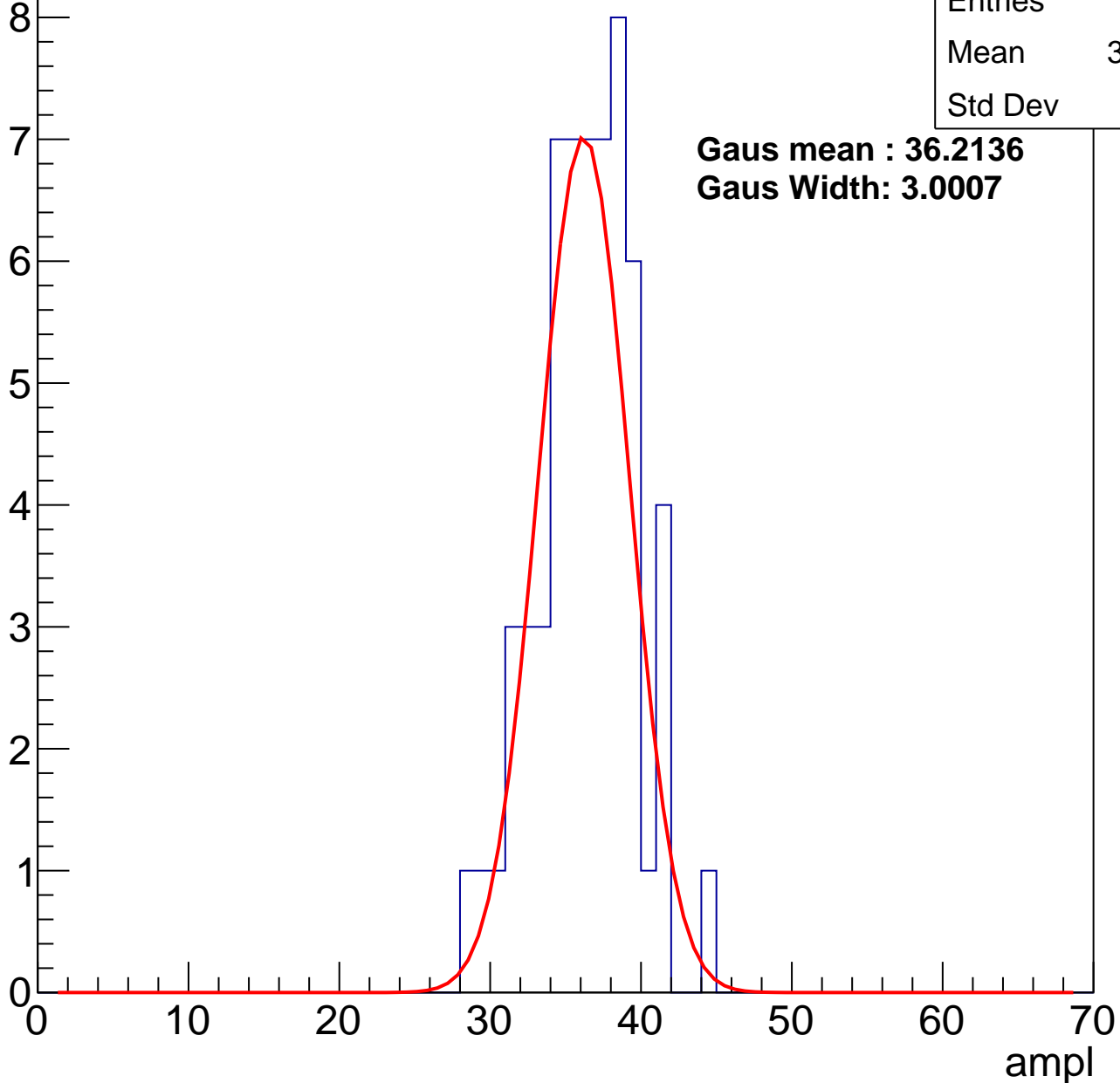
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	35.92
Std Dev	3.18

**Gaus mean : 36.2136**

**Gaus Width: 3.0007**



# B1L101S, U11-ch83, adc2

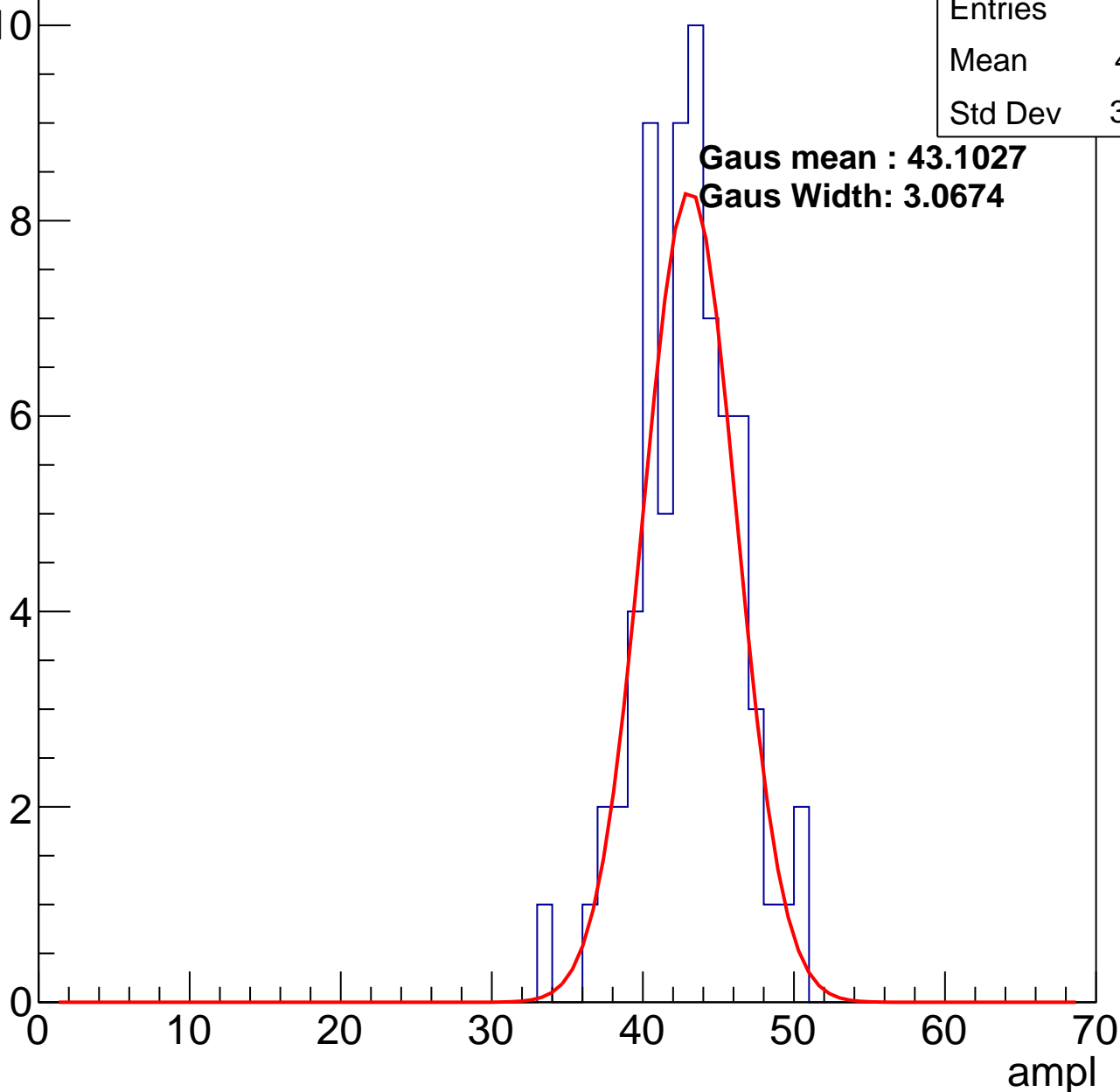
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	42.61
Std Dev	3.245

**Gaus mean : 43.1027**

**Gaus Width: 3.0674**

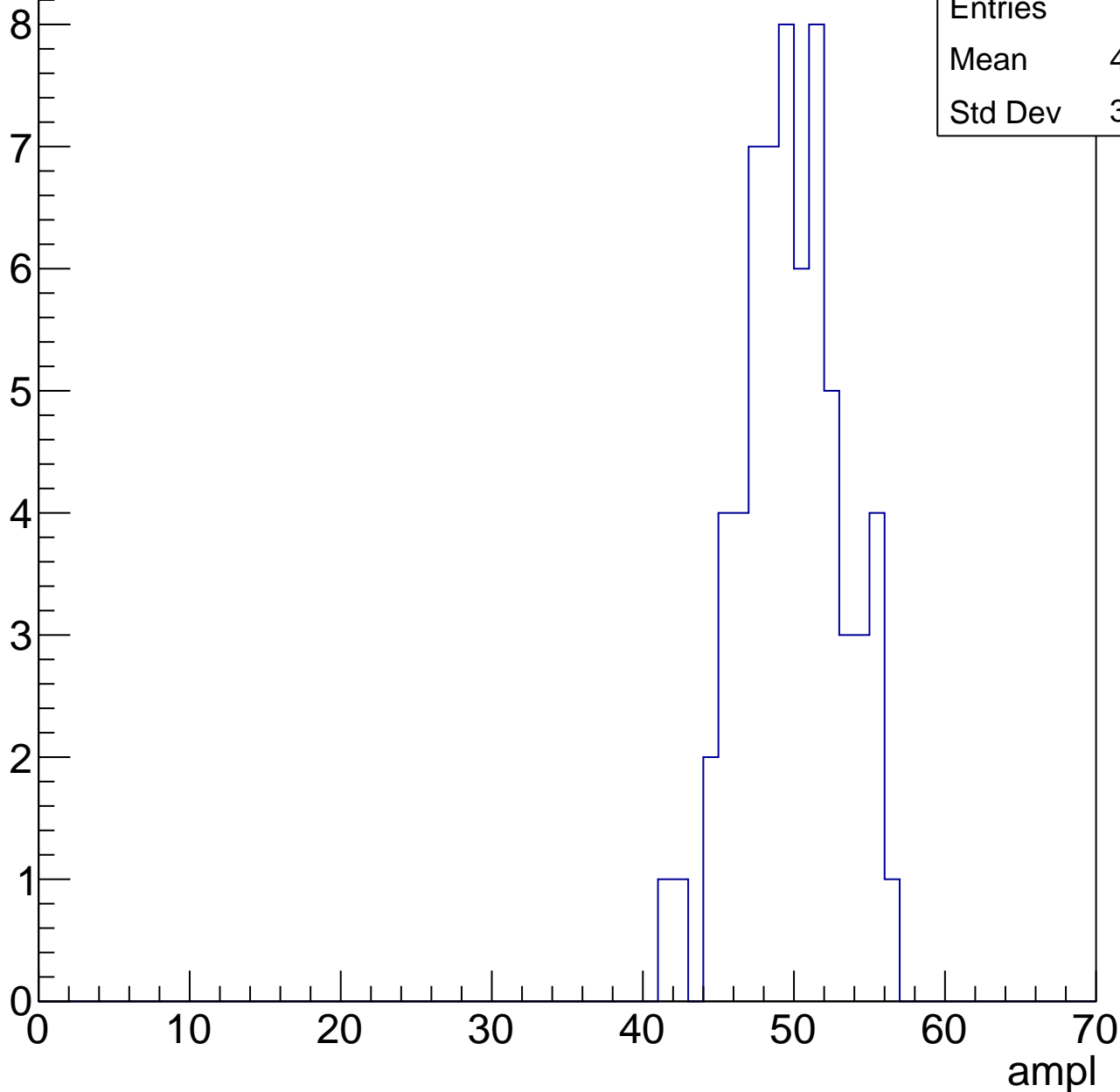


# B1L101S, U11-ch83, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	49.33
Std Dev	3.284

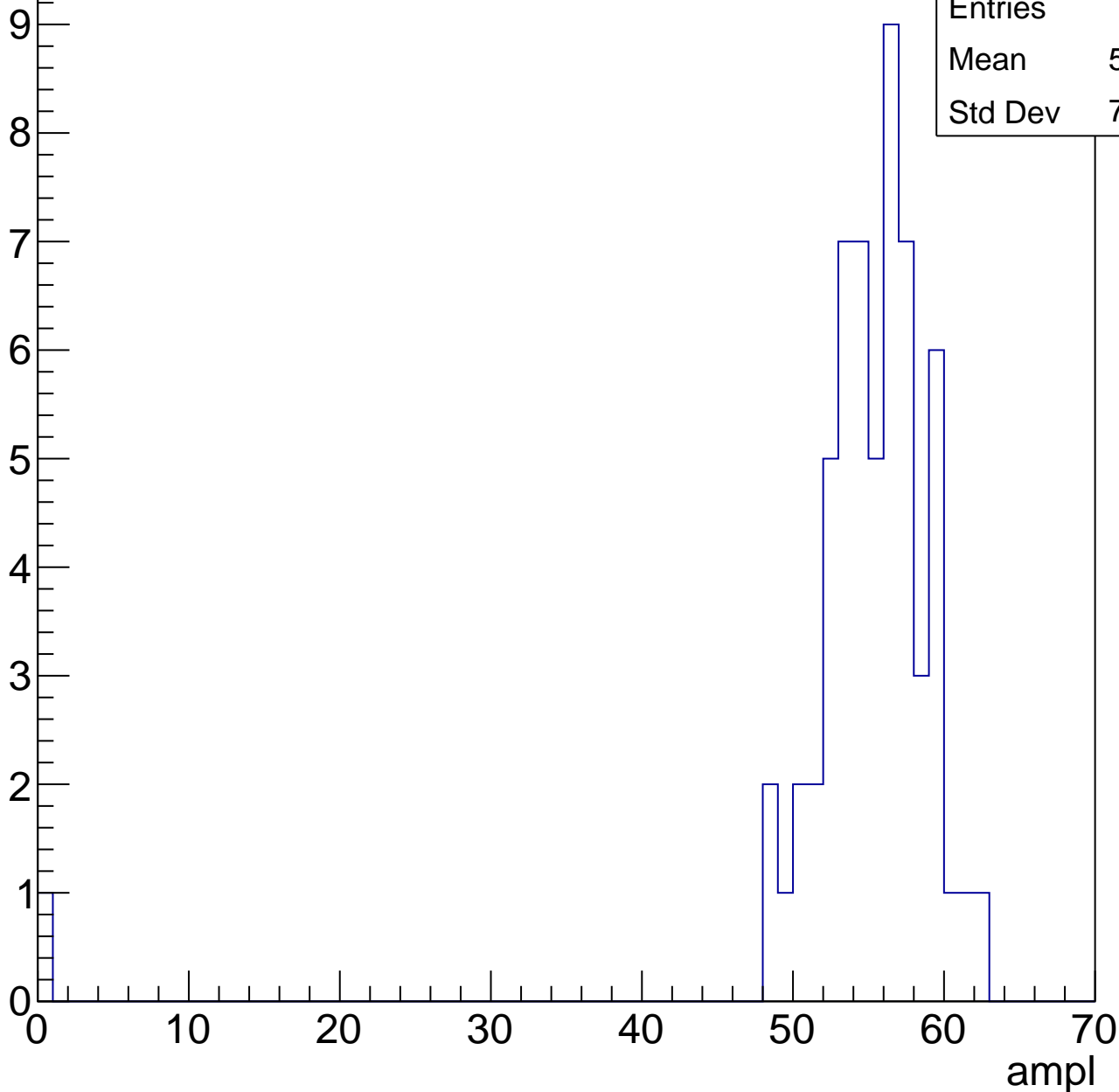


# B1L101S, U11-ch83, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	54.08
Std Dev	7.682

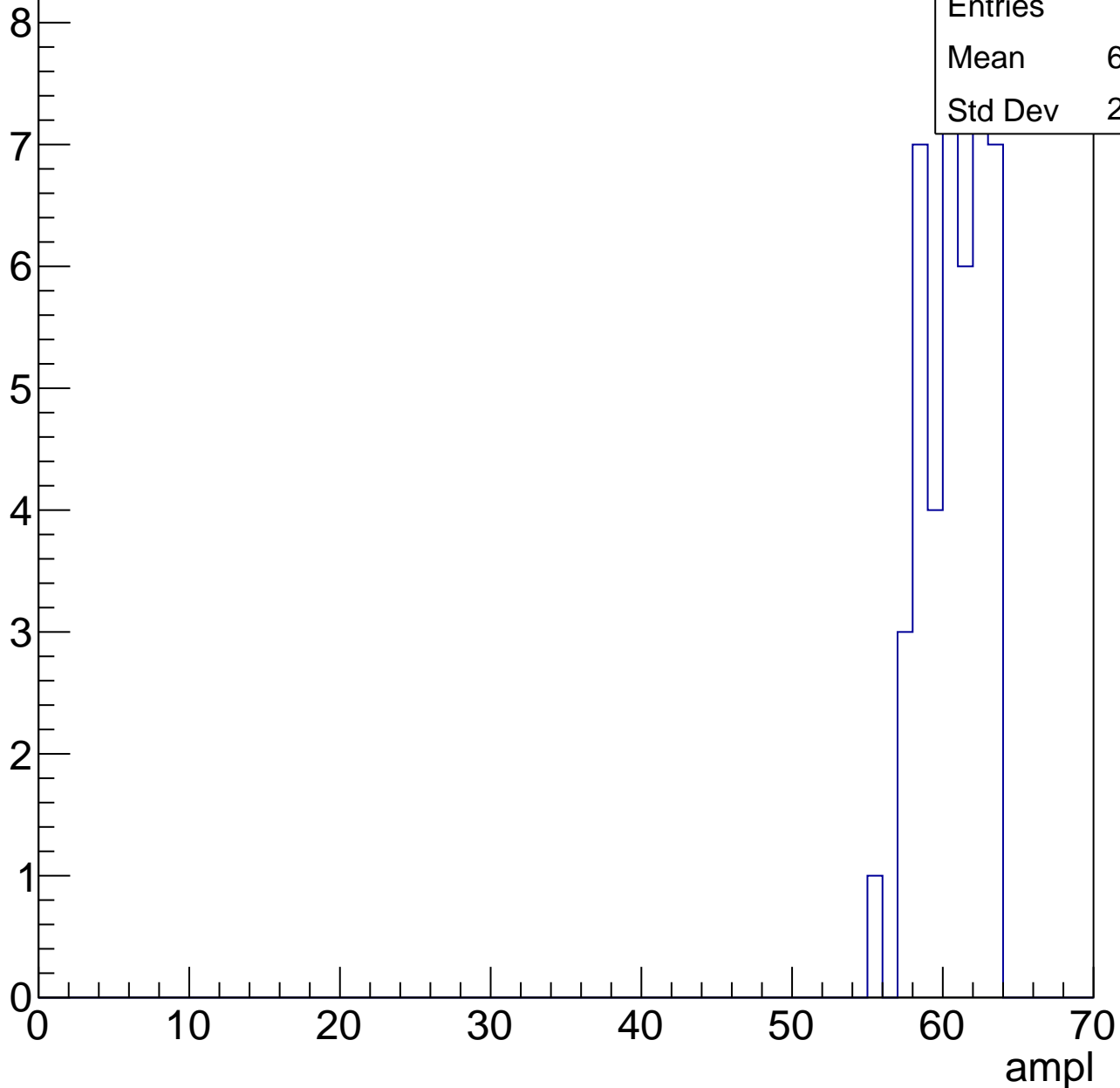


# B1L101S, U11-ch83, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

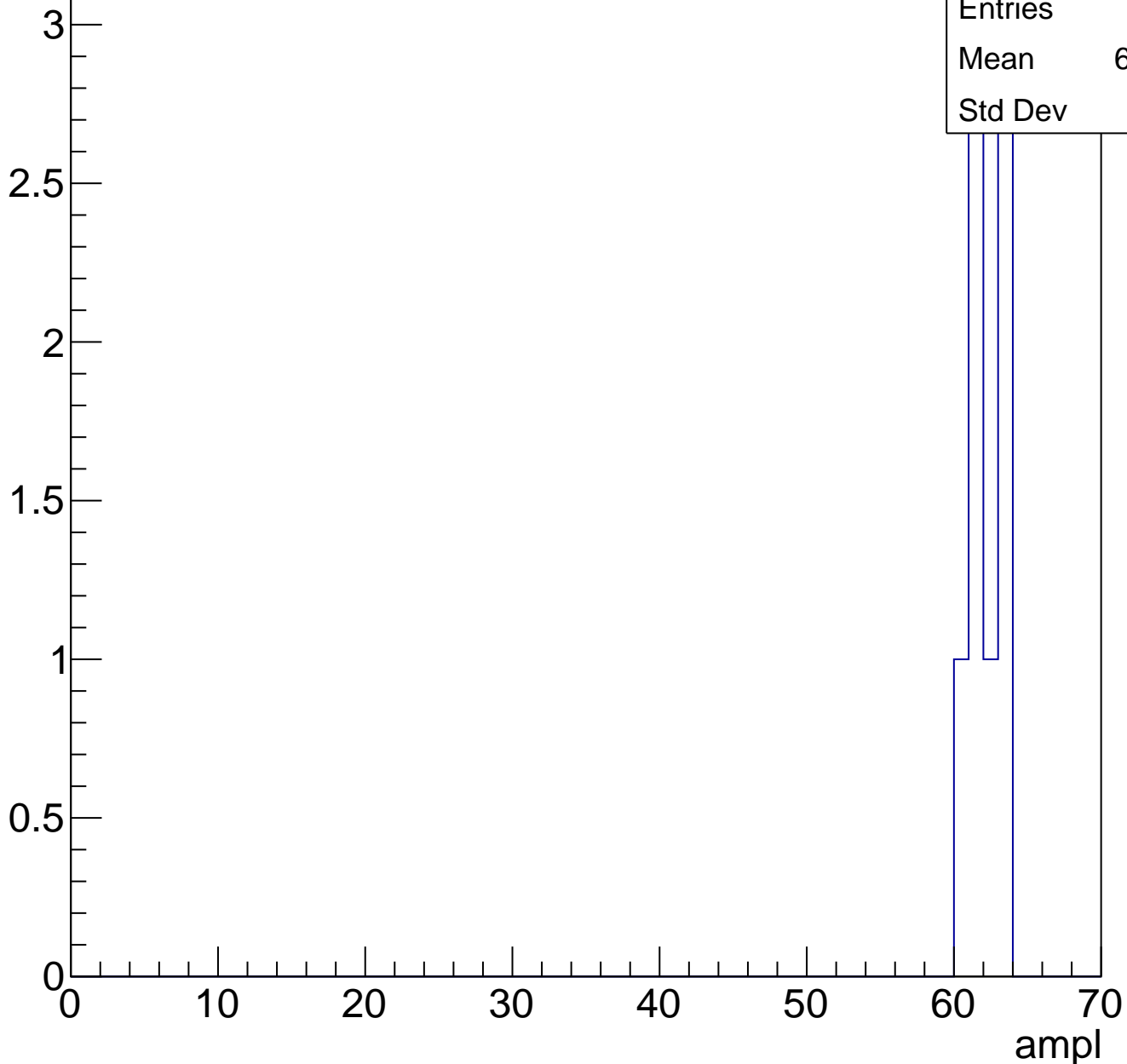
Entries	44
Mean	60.25
Std Dev	2.035



# B1L101S, U11-ch83, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	8
Mean	61.75
Std Dev	1.09



# B1L101S, U11-ch83, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	11
Std Dev	11

# B1L101S, U11-ch84, adc0

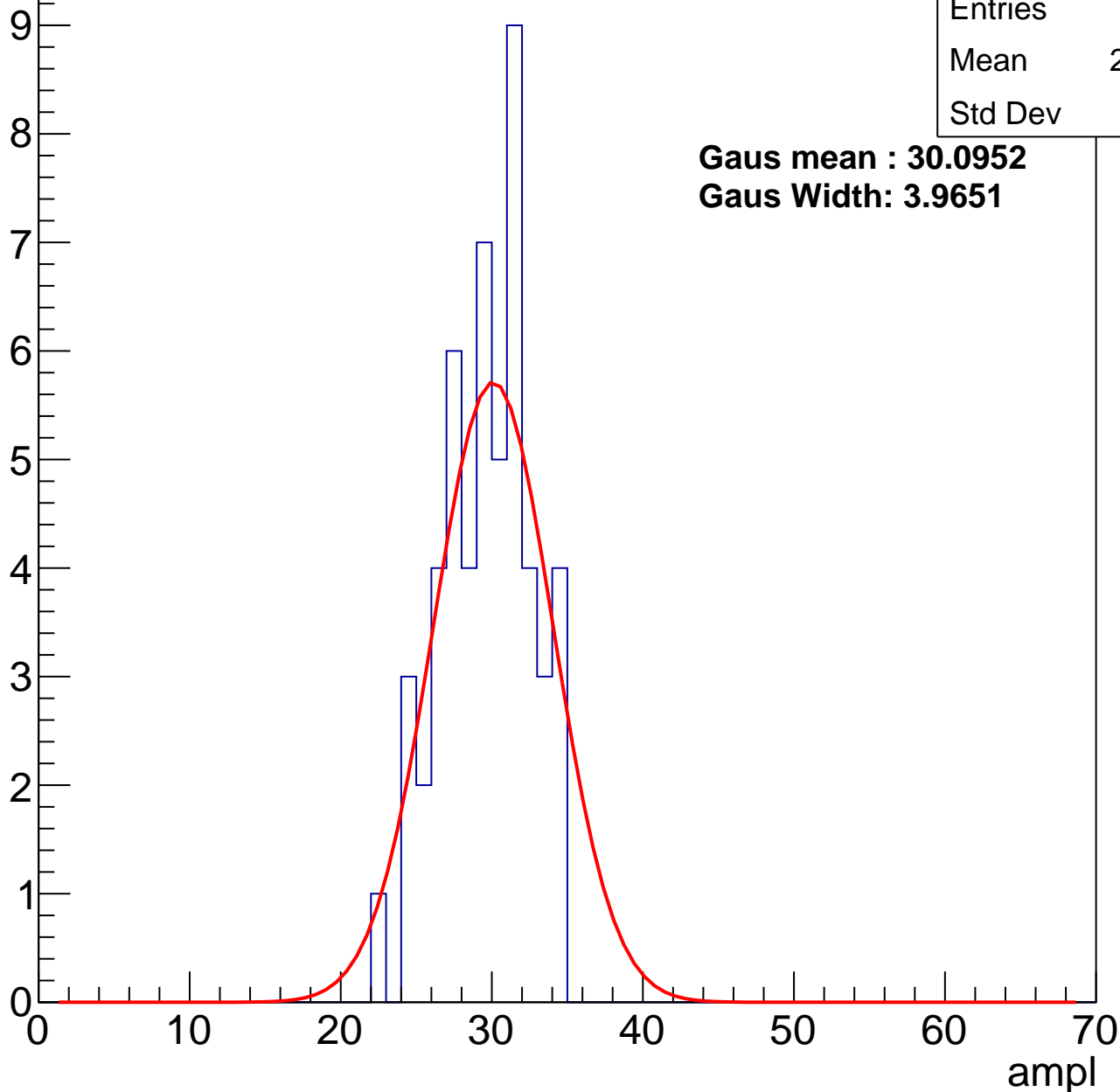
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	29.17
Std Dev	2.92

**Gaus mean : 30.0952**

**Gaus Width: 3.9651**



# B1L101S, U11-ch84, adc1

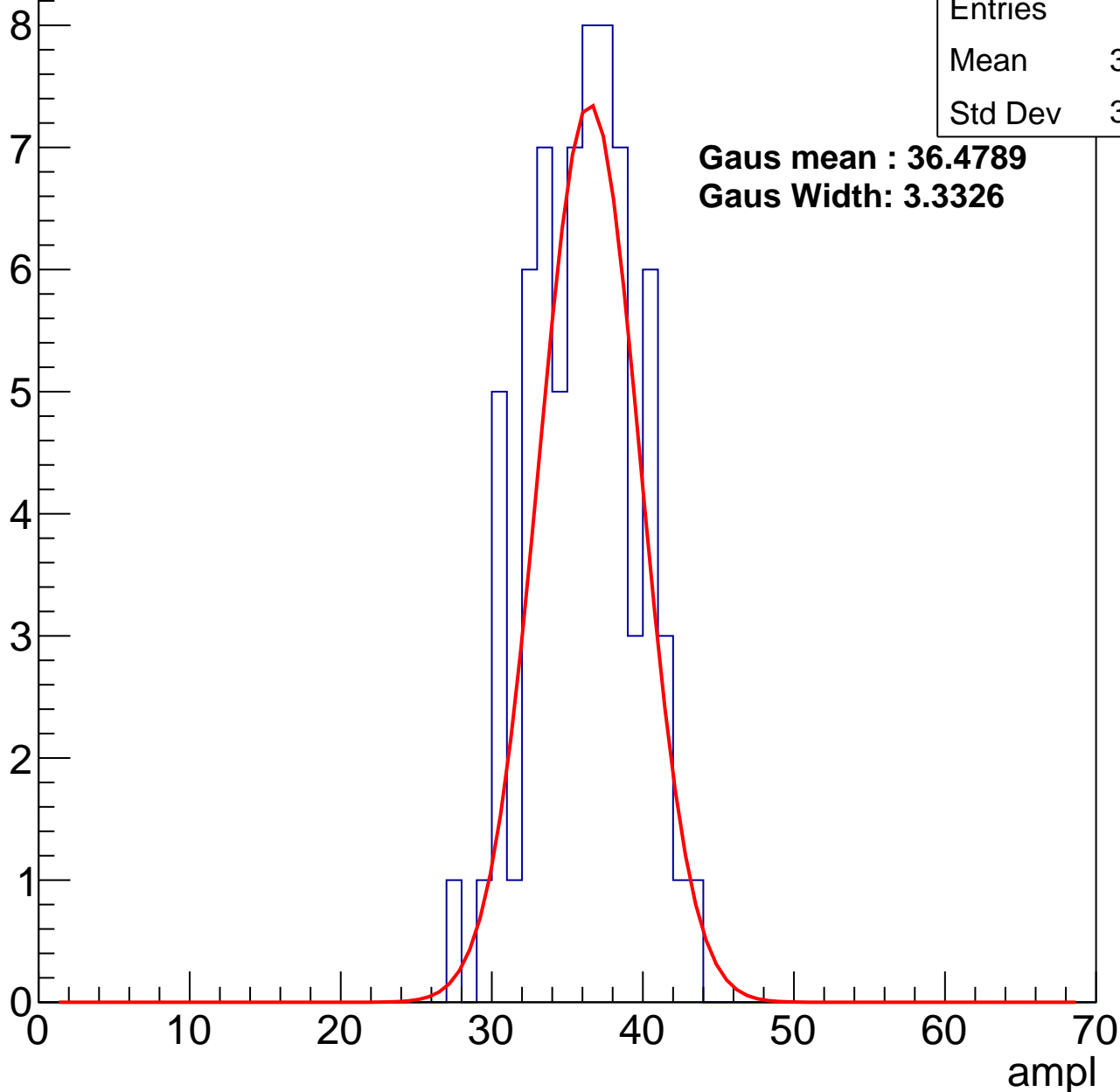
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	35.57
Std Dev	3.437

**Gaus mean : 36.4789**

**Gaus Width: 3.3326**



# B1L101S, U11-ch84, adc2

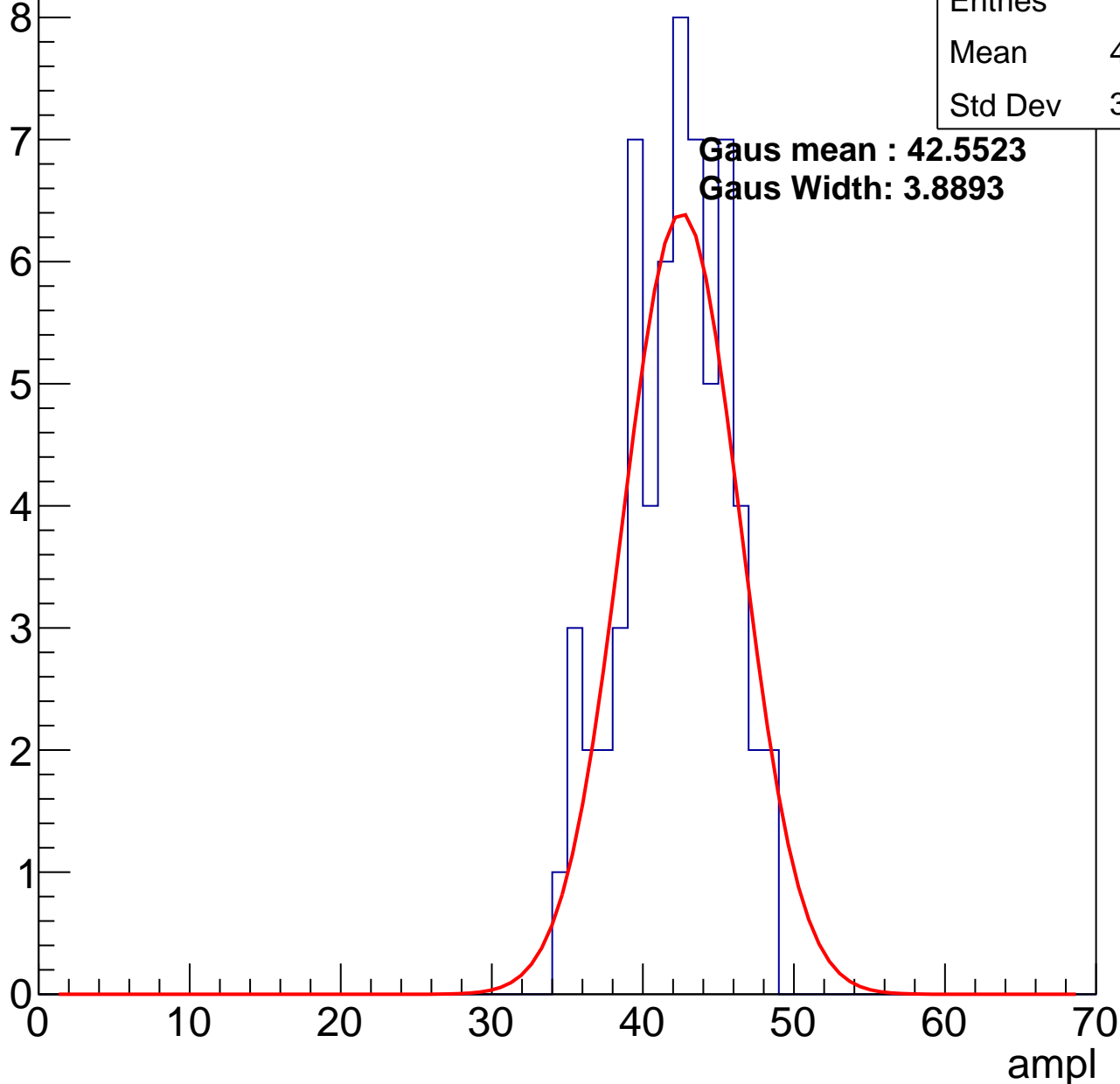
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	41.65
Std Dev	3.414

**Gaus mean : 42.5523**

**Gaus Width: 3.8893**



# B1L101S, U11-ch84, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	68
Mean	48.76
Std Dev	3.352

Entry

10

8

6

4

2

0

0

10

20

30

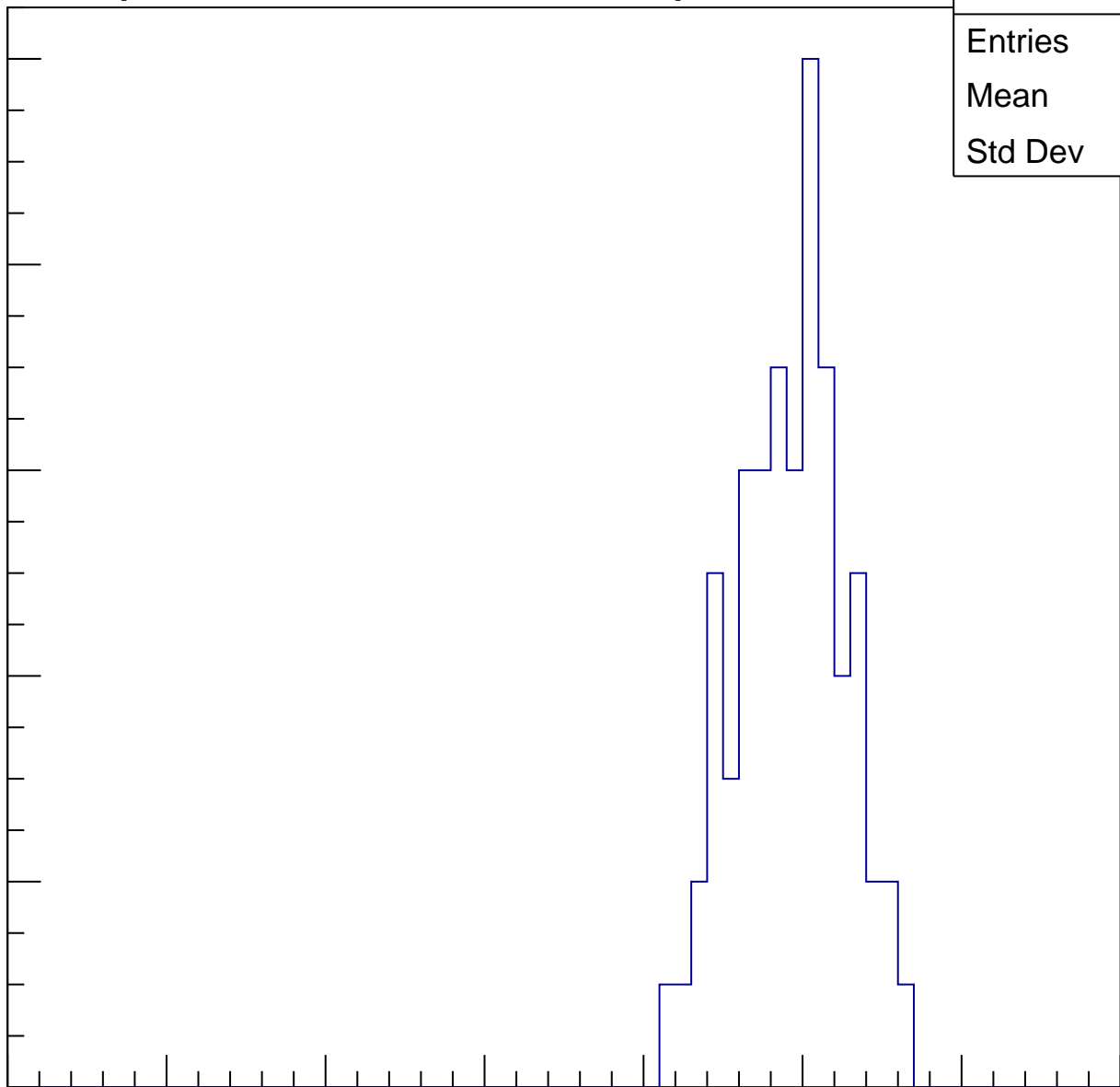
40

50

60

70

ampl

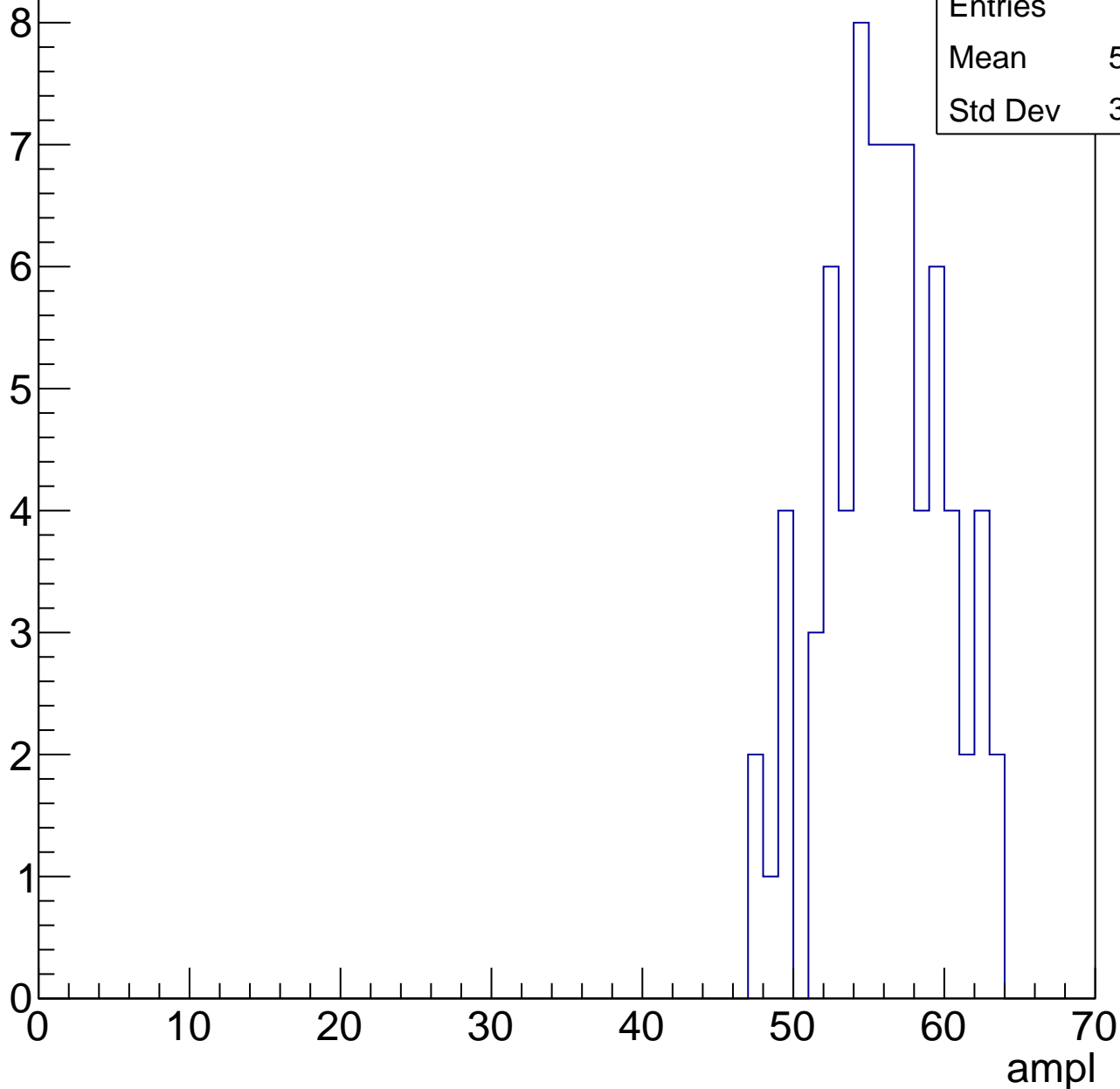


# B1L101S, U11-ch84, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	55.56
Std Dev	3.914

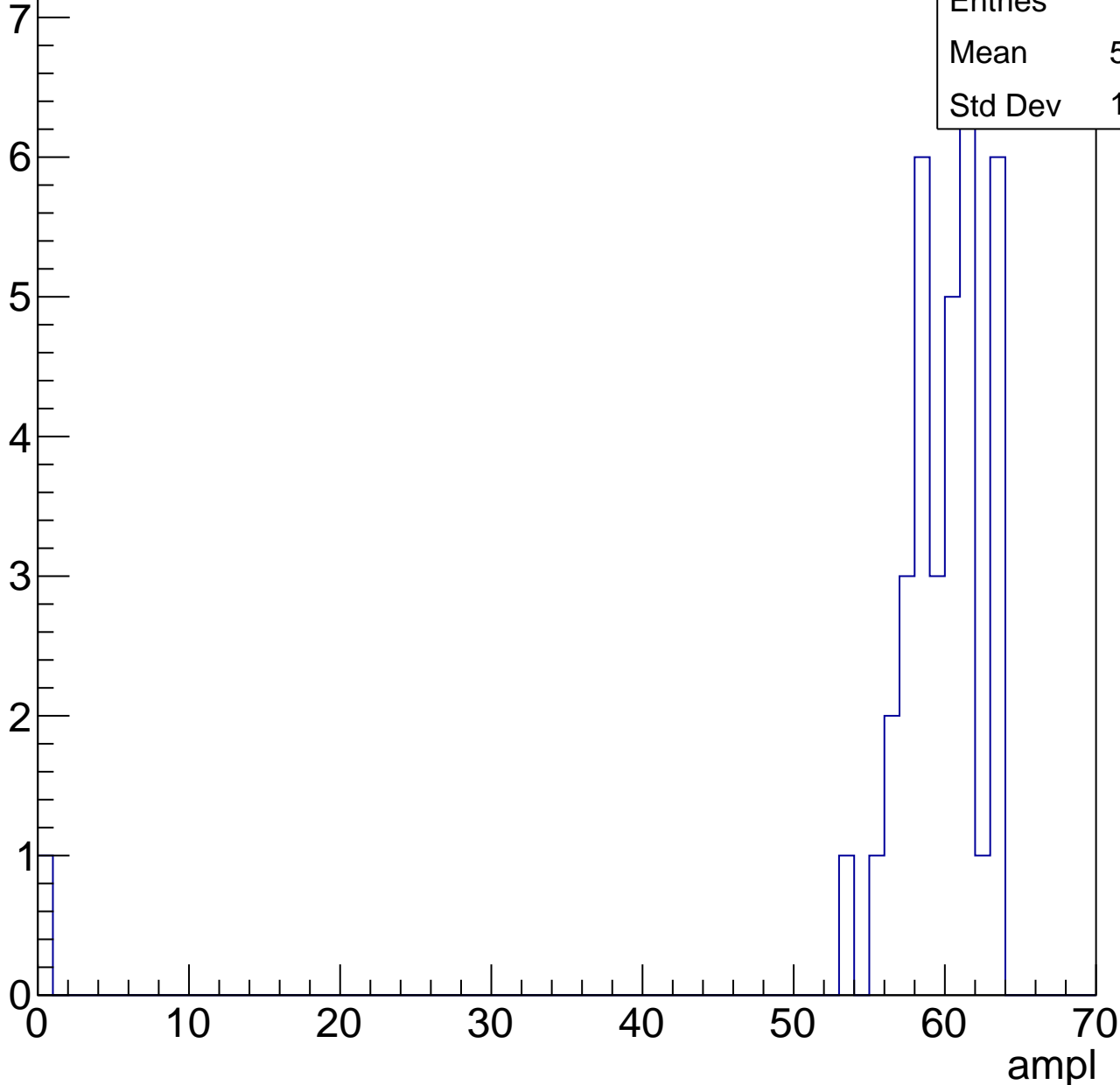


# B1L101S, U11-ch84, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	36
Mean	57.86
Std Dev	10.08

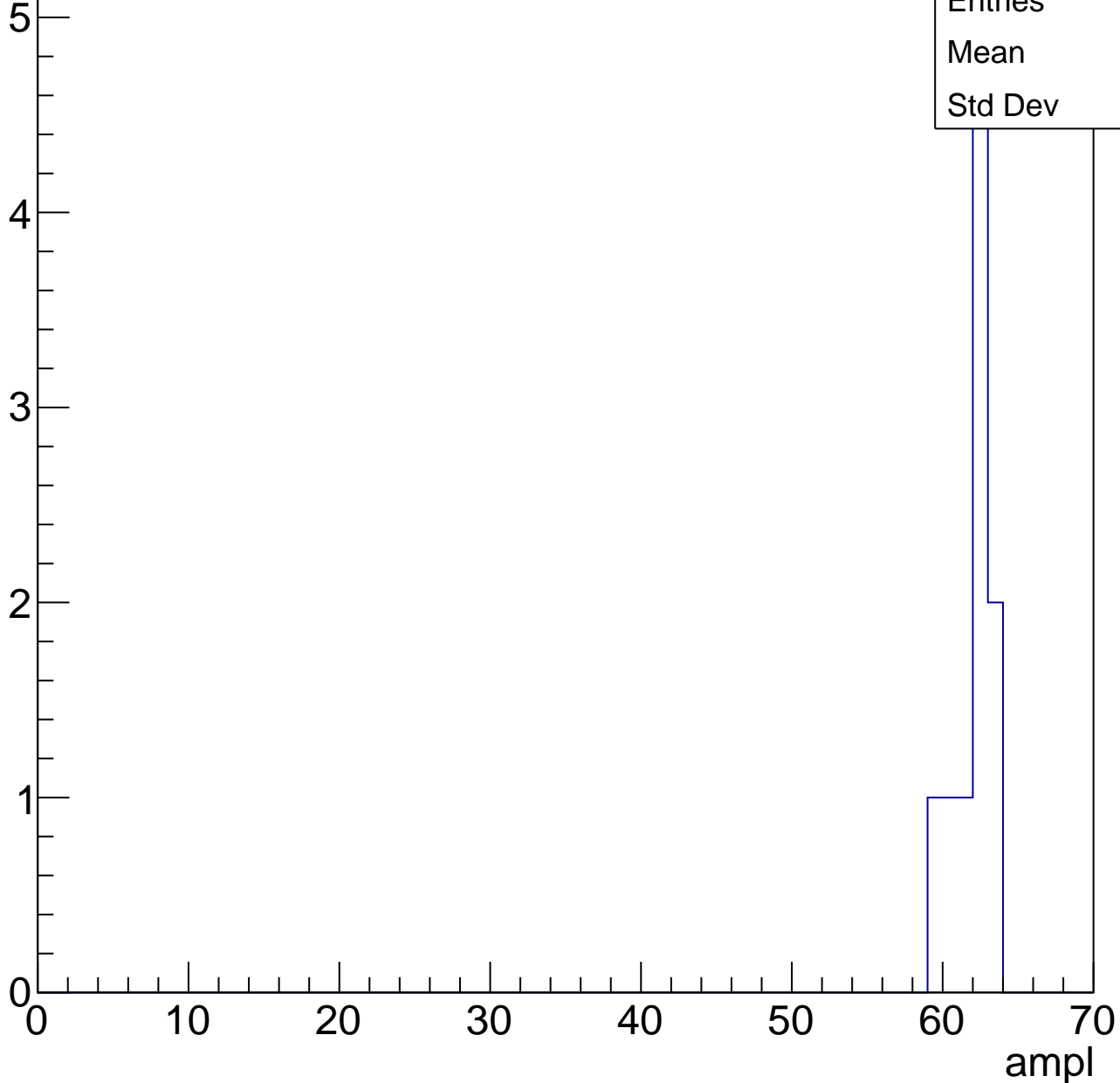


# B1L101S, U11-ch84, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	10
Mean	61.6
Std Dev	1.2





# B1L101S, U11-ch84, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U11-ch85, adc0

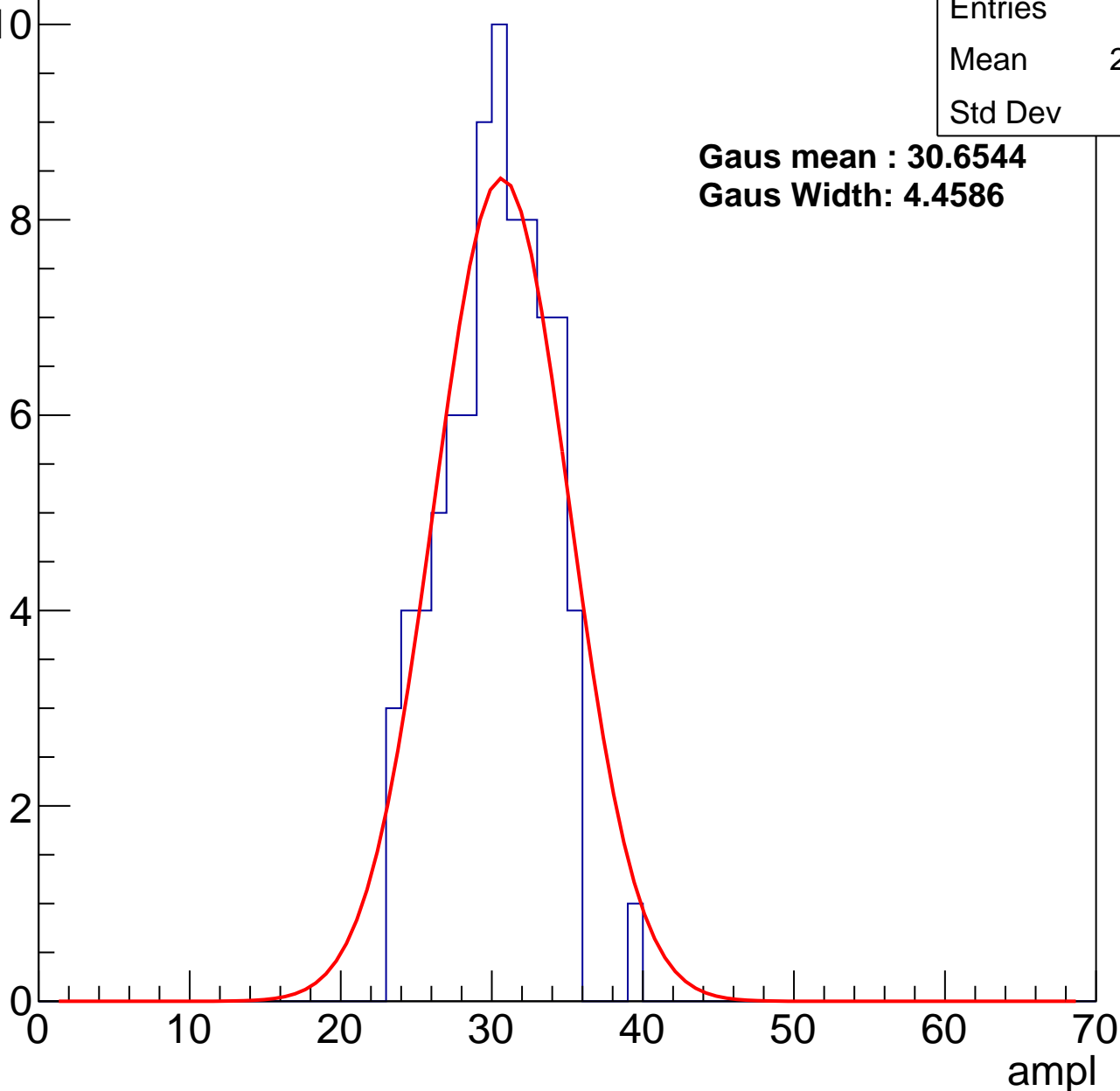
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	82
Mean	29.73
Std Dev	3.4

**Gaus mean : 30.6544**

**Gaus Width: 4.4586**



# B1L101S, U11-ch85, adc1

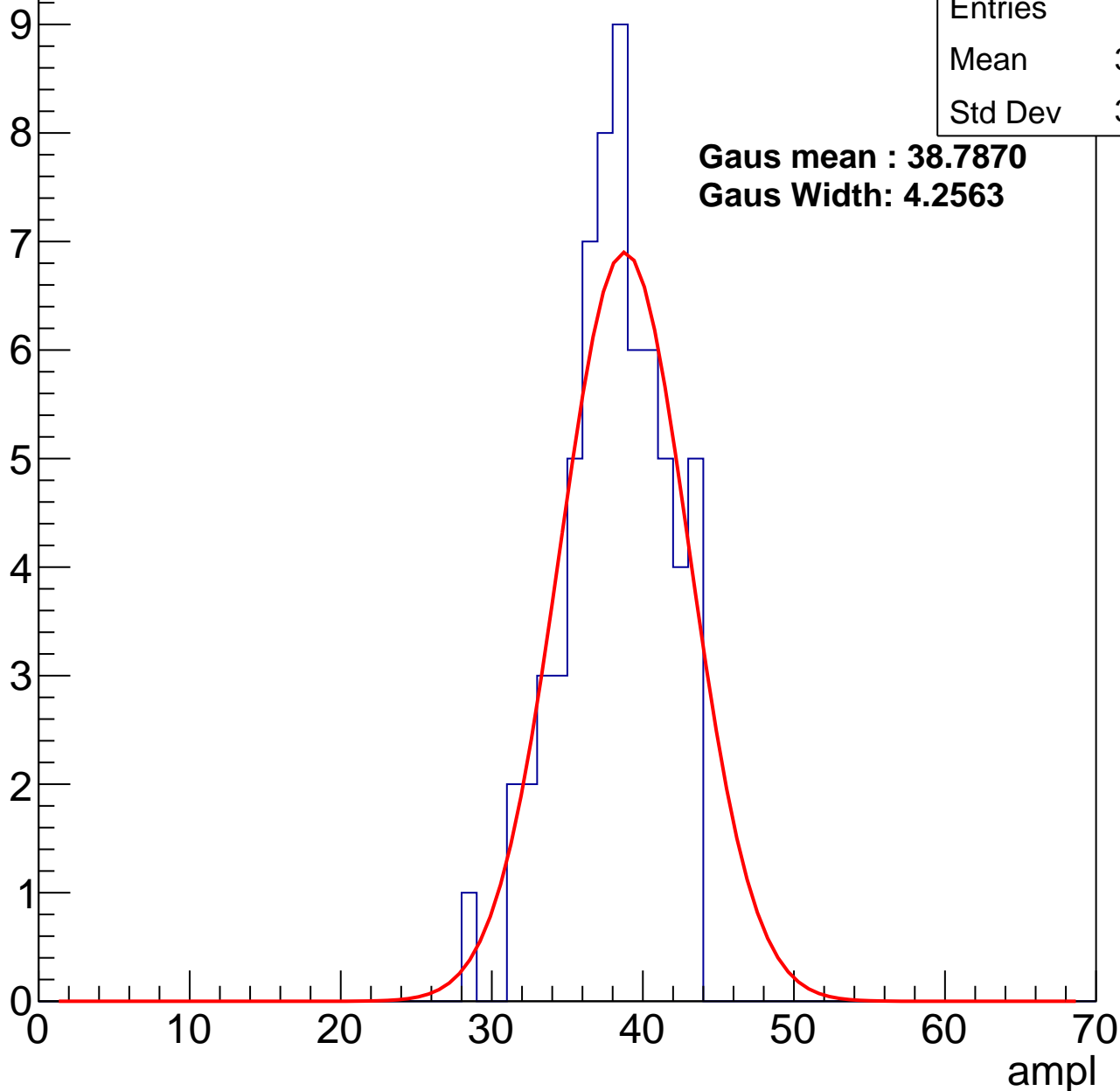
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	37.61
Std Dev	3.321

**Gaus mean : 38.7870**

**Gaus Width: 4.2563**



# B1L101S, U11-ch85, adc2

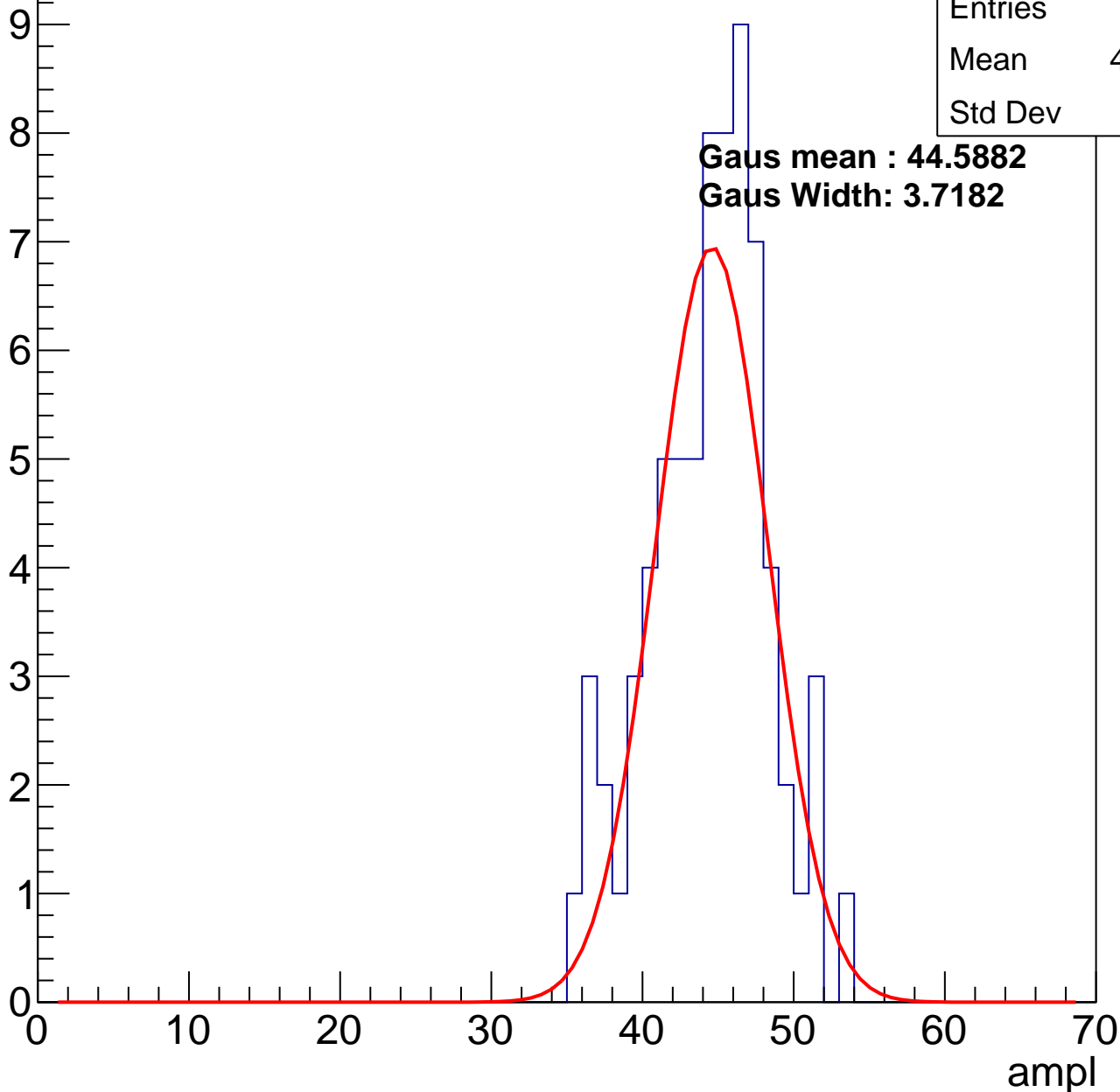
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	43.93
Std Dev	3.91

**Gaus mean : 44.5882**

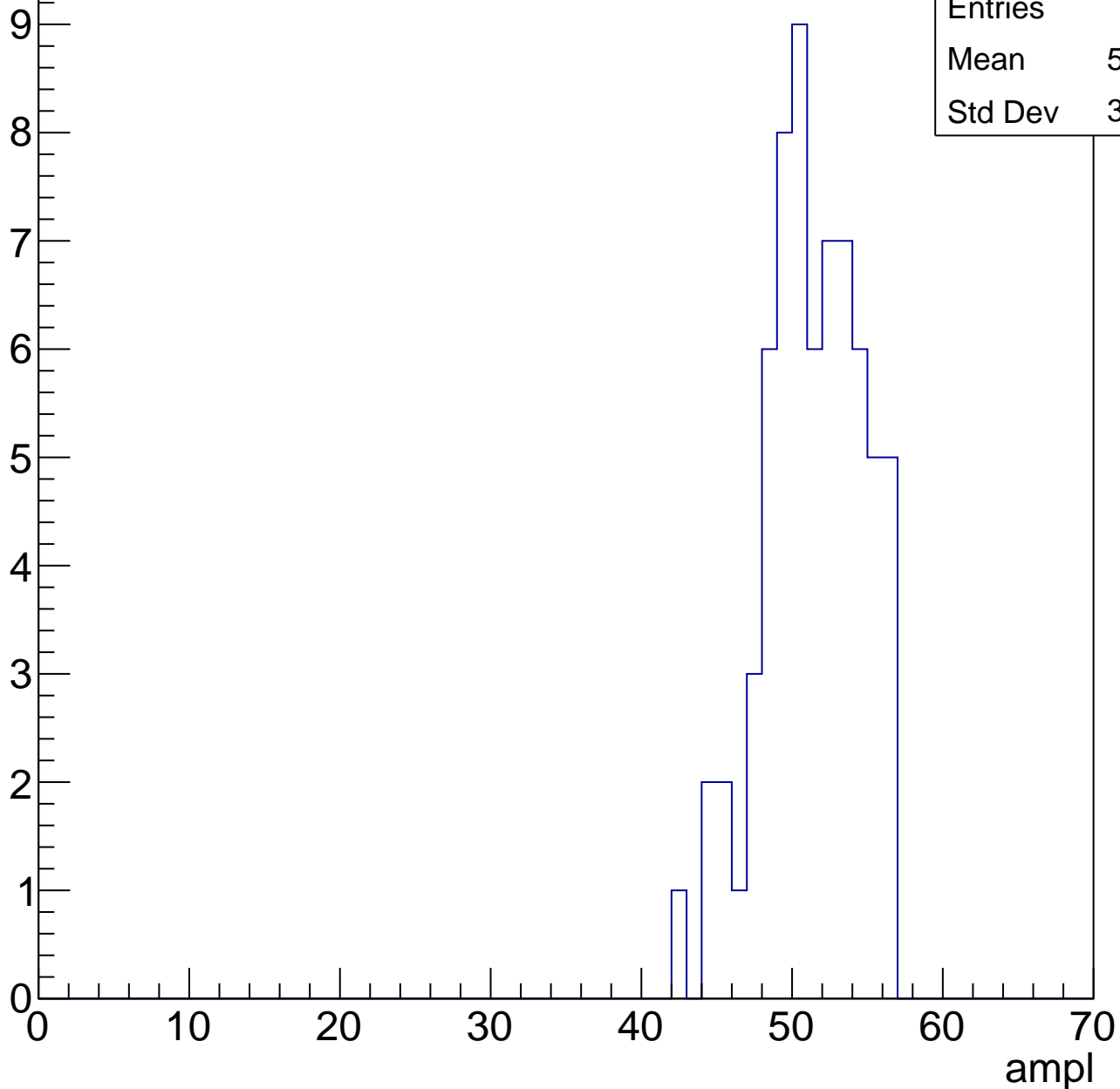
**Gaus Width: 3.7182**



# B1L101S, U11-ch85, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

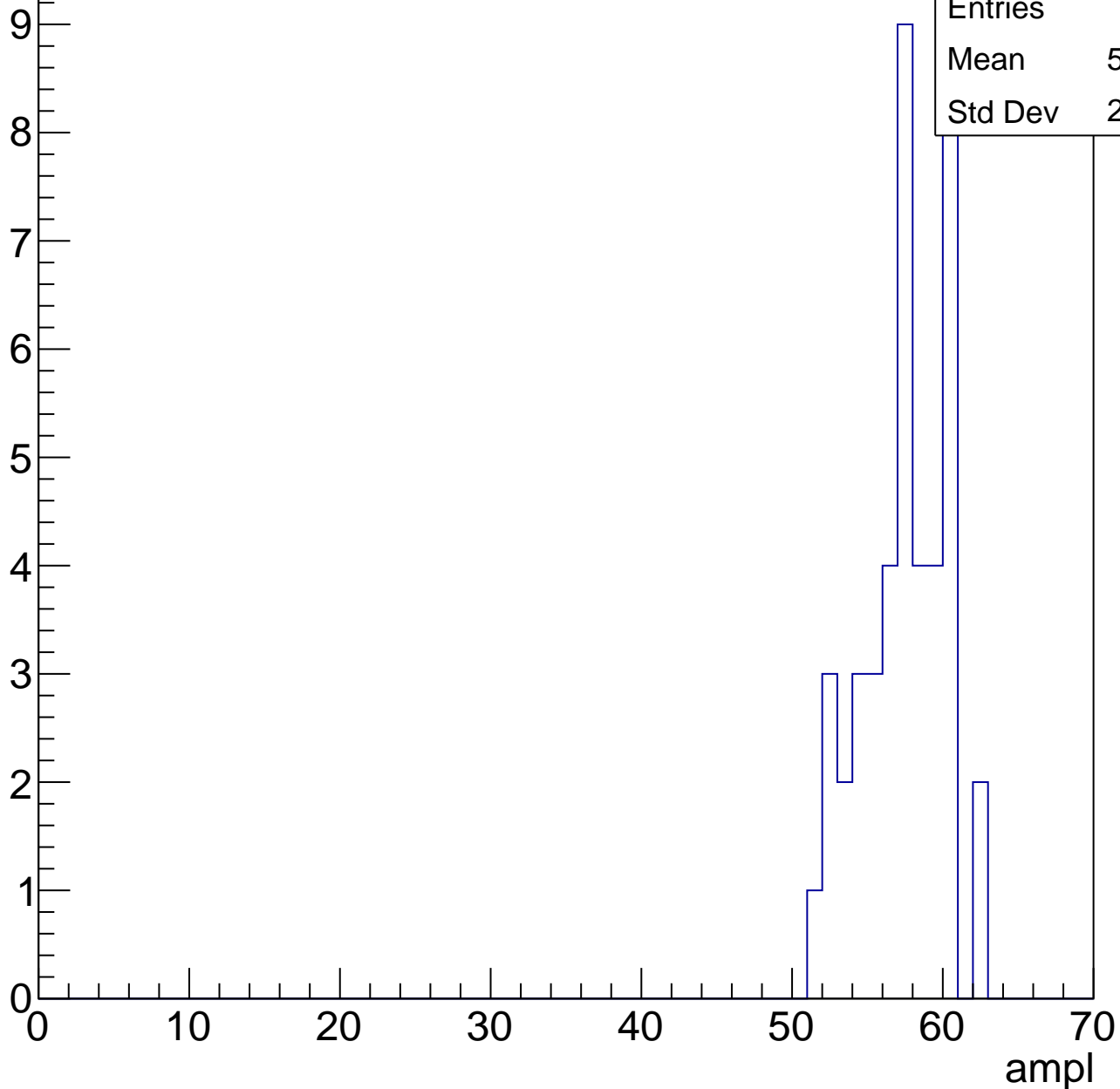
Entry



# B1L101S, U11-ch85, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	44
Mean	57.02
Std Dev	2.767

# B1L101S, U11-ch85, adc5

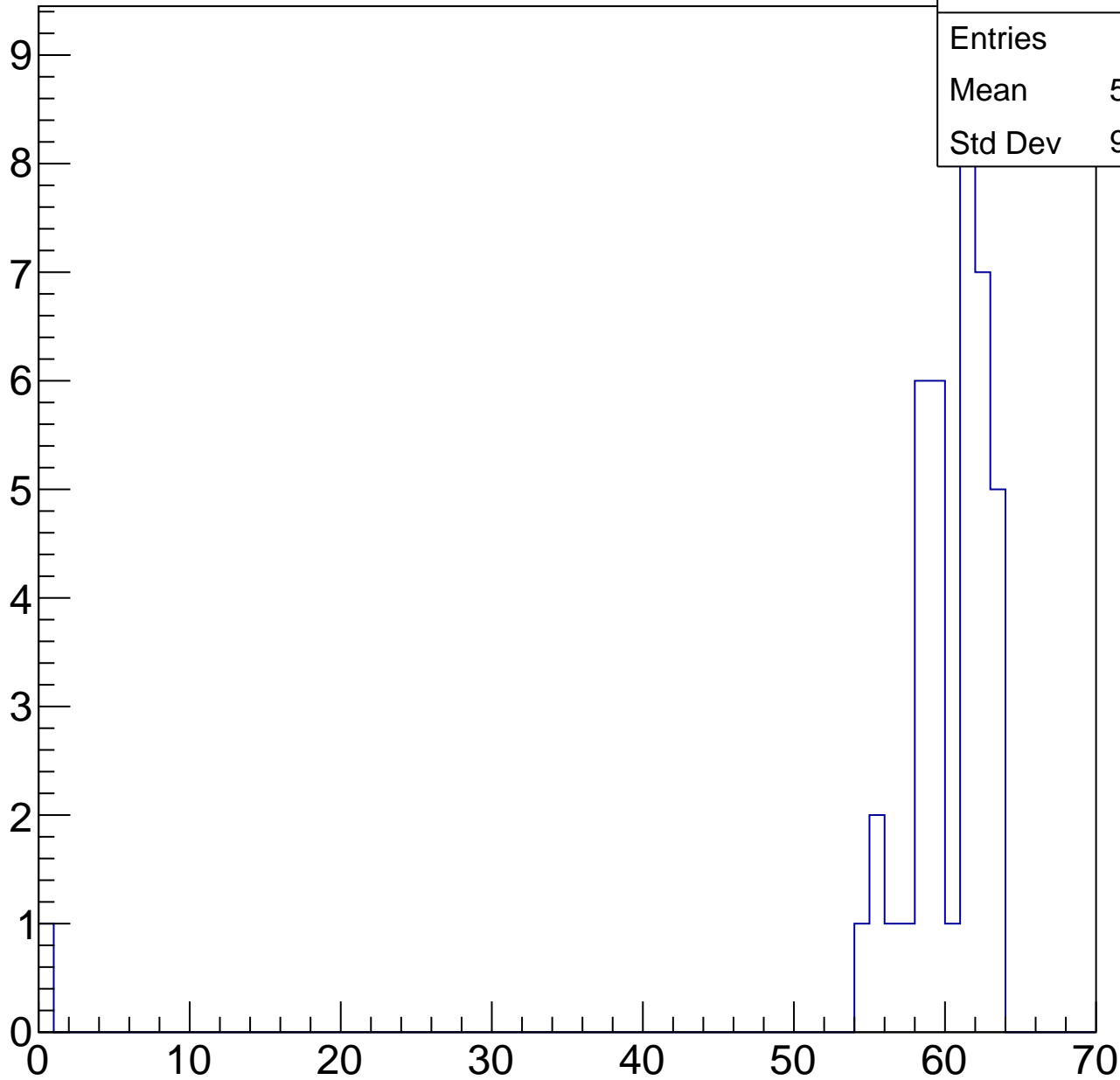
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	40
Mean	58.42
Std Dev	9.649

ampl

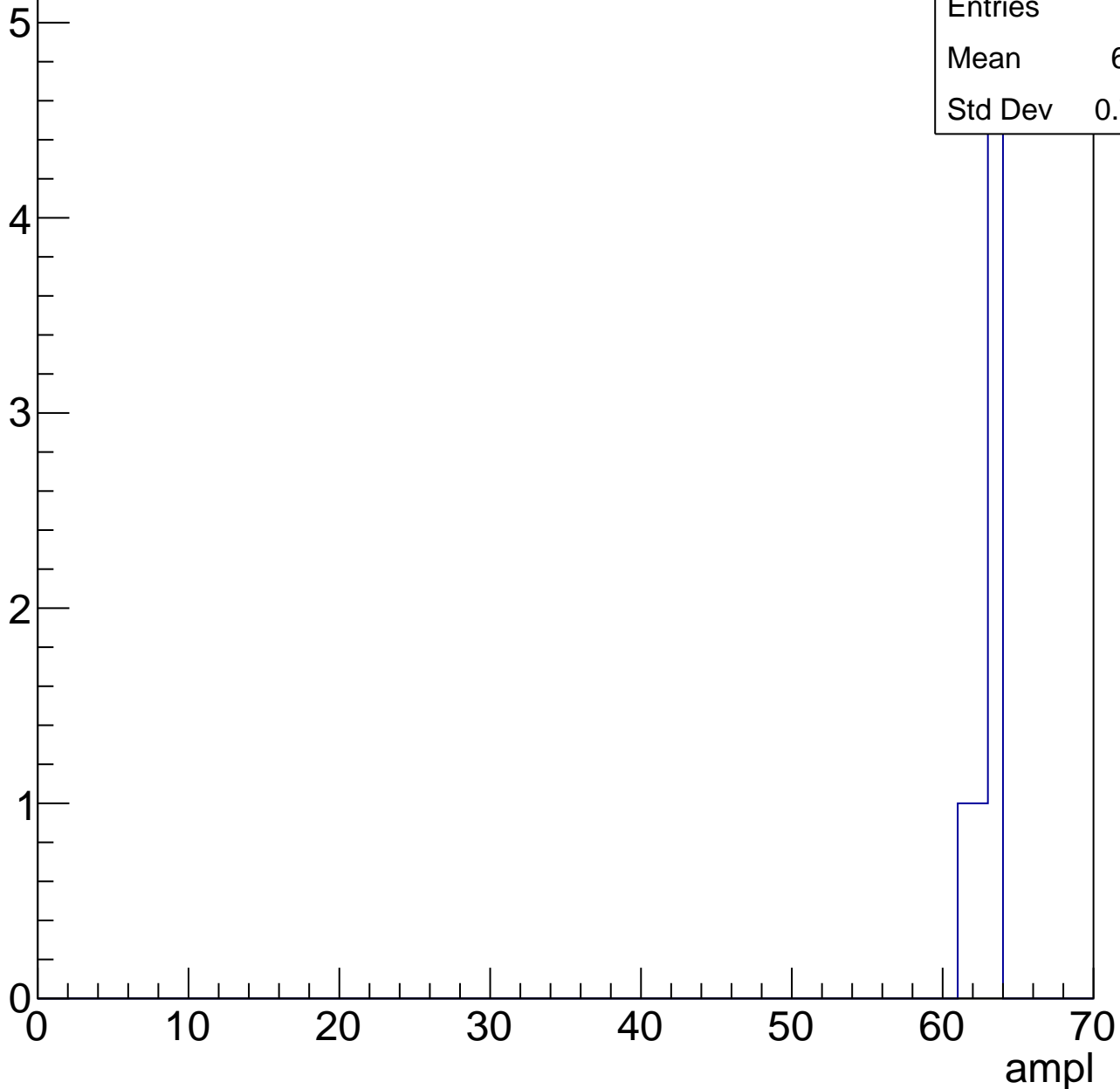


# B1L101S, U11-ch85, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	7
Mean	62.57
Std Dev	0.7284





# B1L101S, U11-ch85, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U11-ch86, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	73
Mean	30.66
Std Dev	5.051

**Gaus mean : 32.0720**

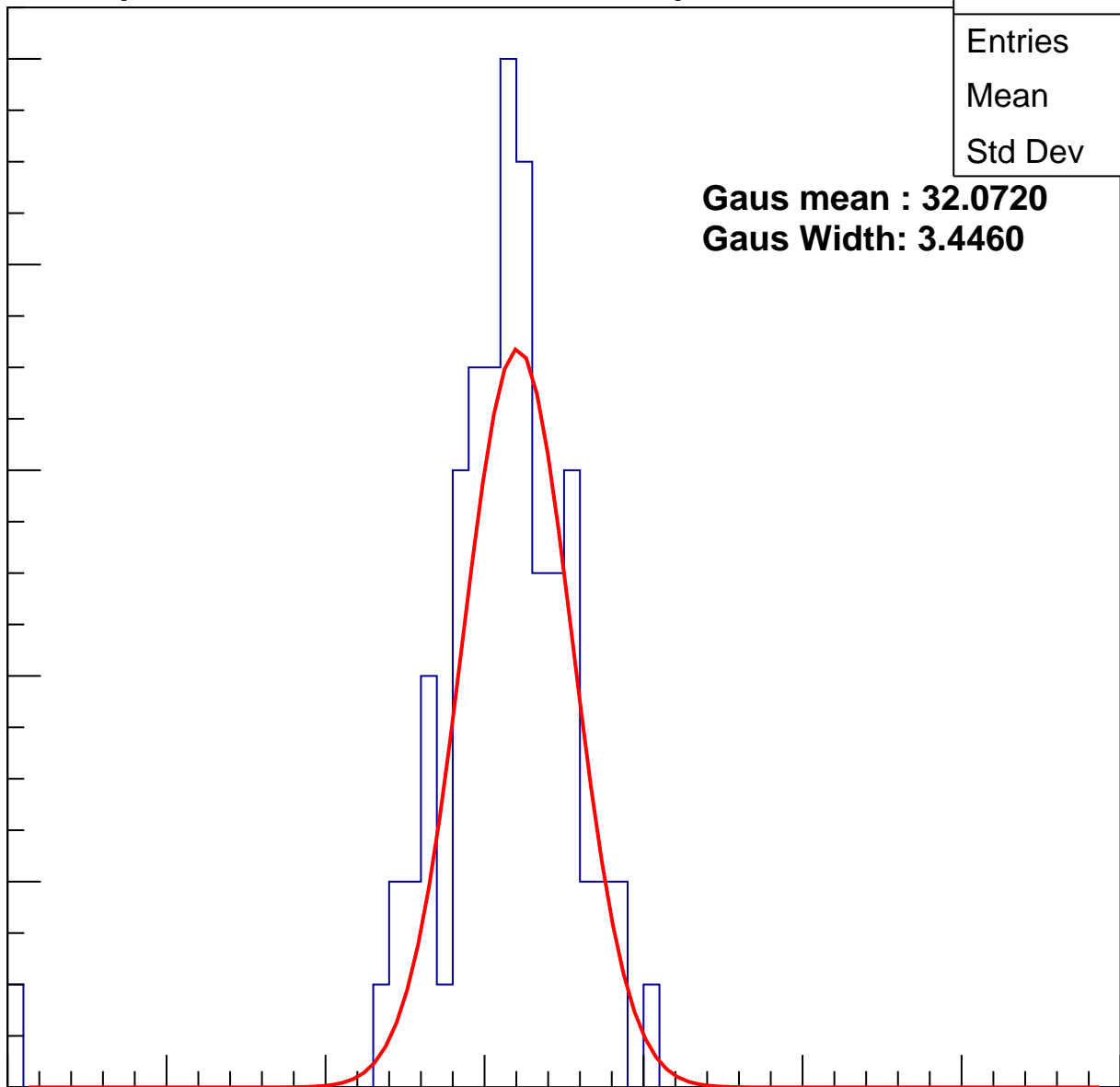
**Gaus Width: 3.4460**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U11-ch86, adc1

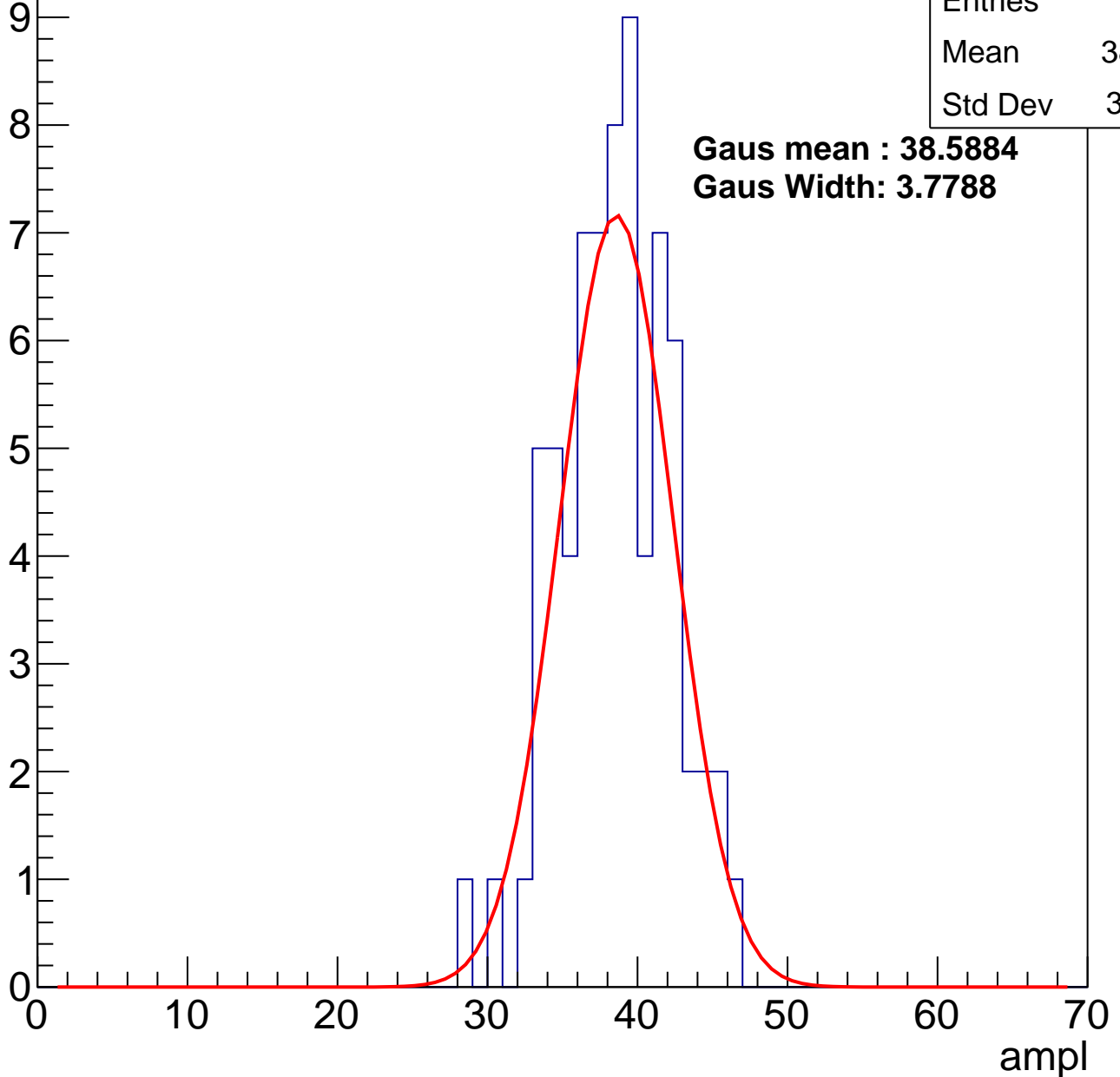
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	38.06
Std Dev	3.621

**Gaus mean : 38.5884**

**Gaus Width: 3.7788**



# B1L101S, U11-ch86, adc2

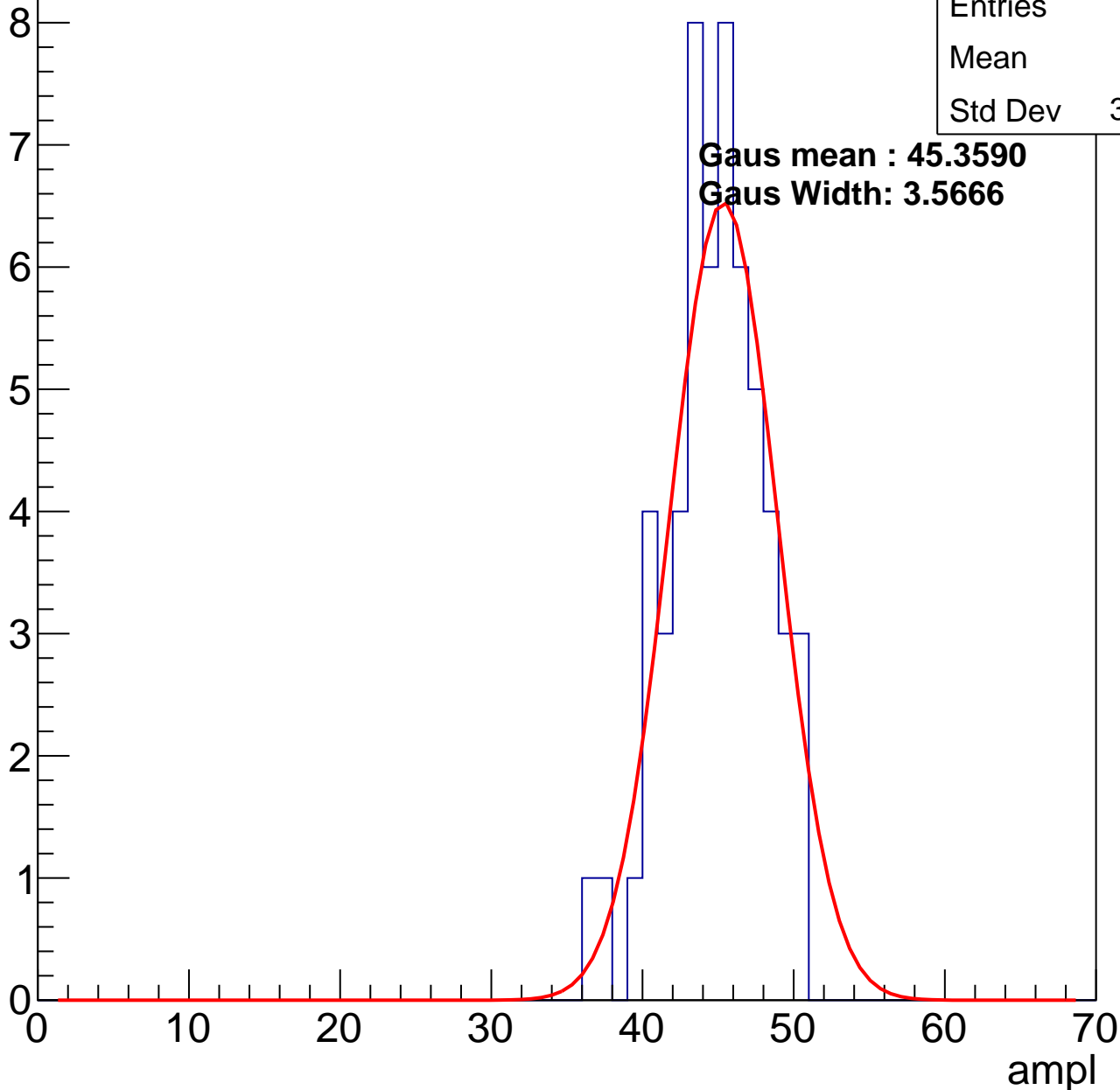
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	44.4
Std Dev	3.156

**Gaus mean : 45.3590**

**Gaus Width: 3.5666**

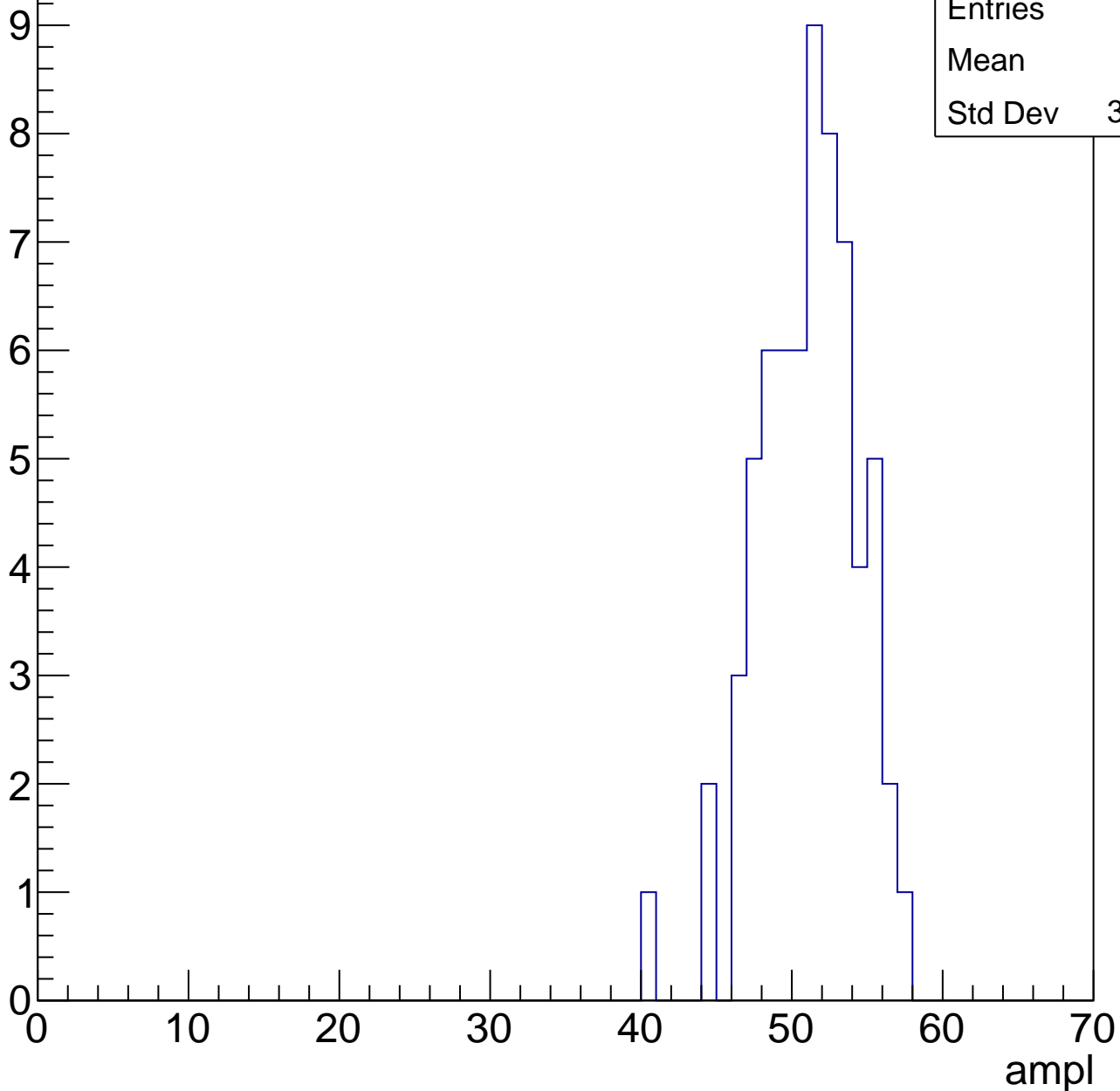


# B1L101S, U11-ch86, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	50.6
Std Dev	3.248

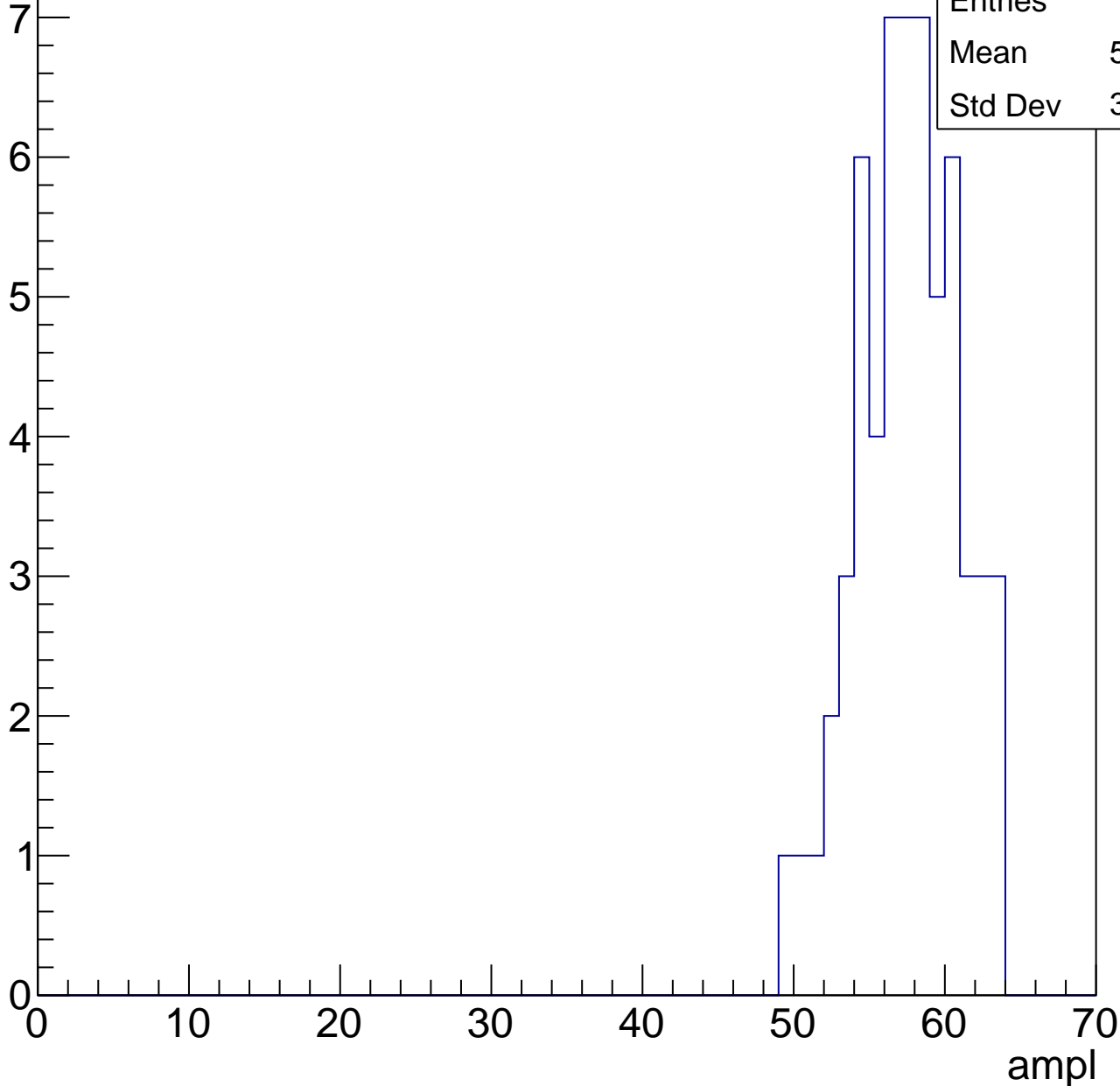


# B1L101S, U11-ch86, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	57.07
Std Dev	3.283

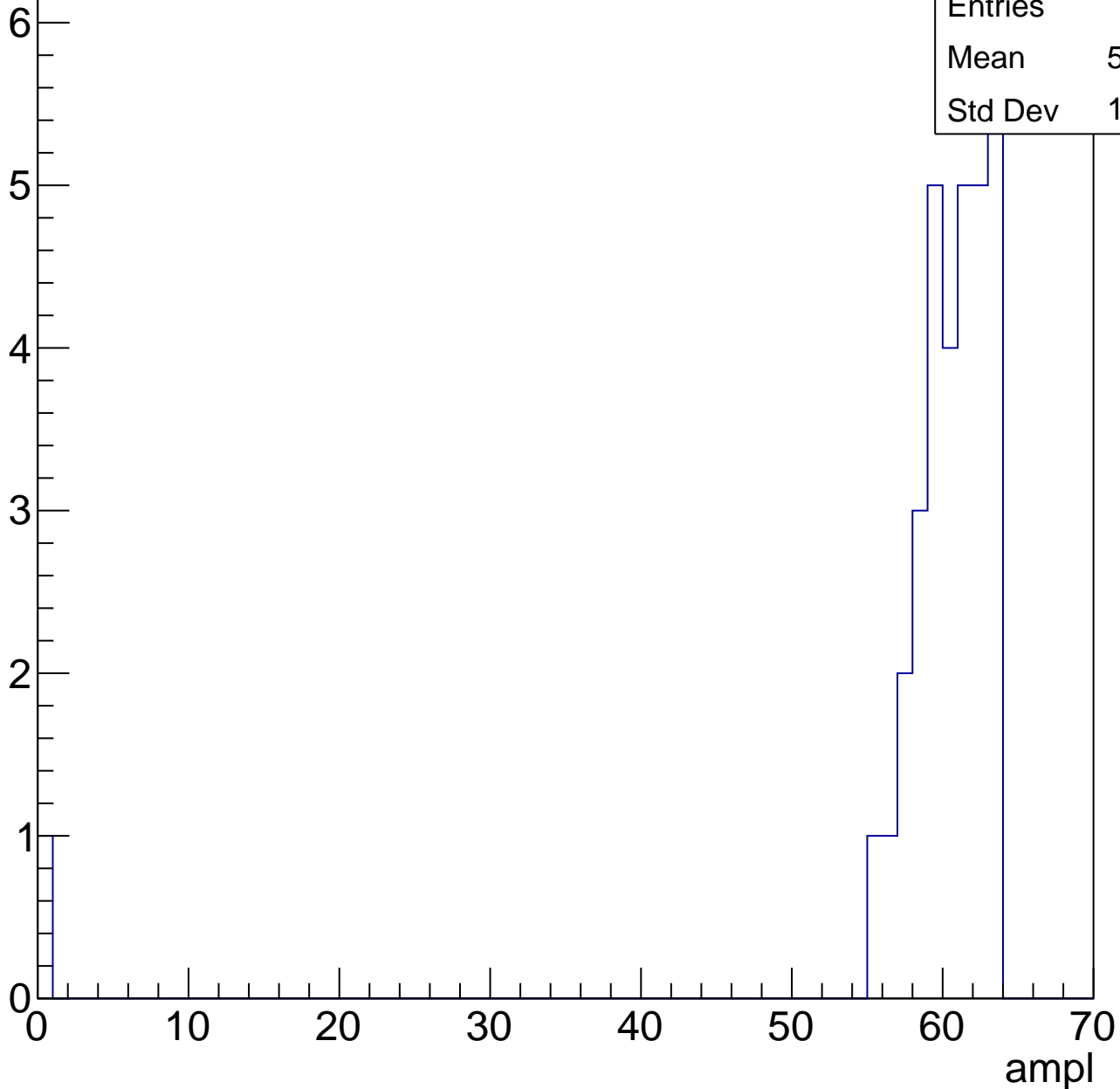


# B1L101S, U11-ch86, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

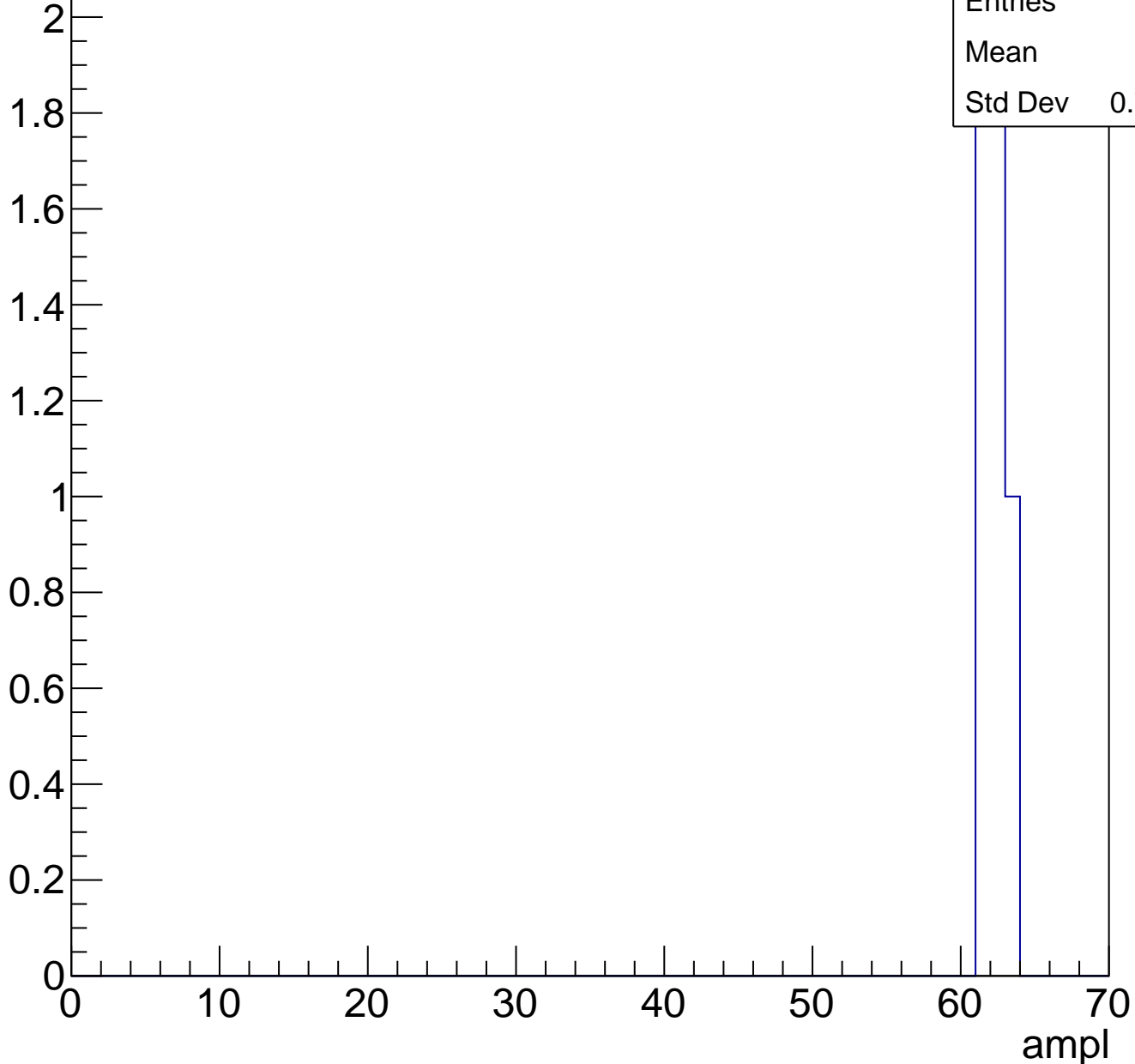
Entries	33
Mean	58.39
Std Dev	10.55



# B1L101S, U11-ch86, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch86, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	23
Std Dev	0

# B1L101S, U11-ch87, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	68
Mean	29.9
Std Dev	7.22

**Gaus mean : 31.5871**

**Gaus Width: 3.7566**

Entry

10  
8  
6  
4  
2  
0

ampl

0

10

20

30

40

50

60

70

# B1L101S, U11-ch87, adc1

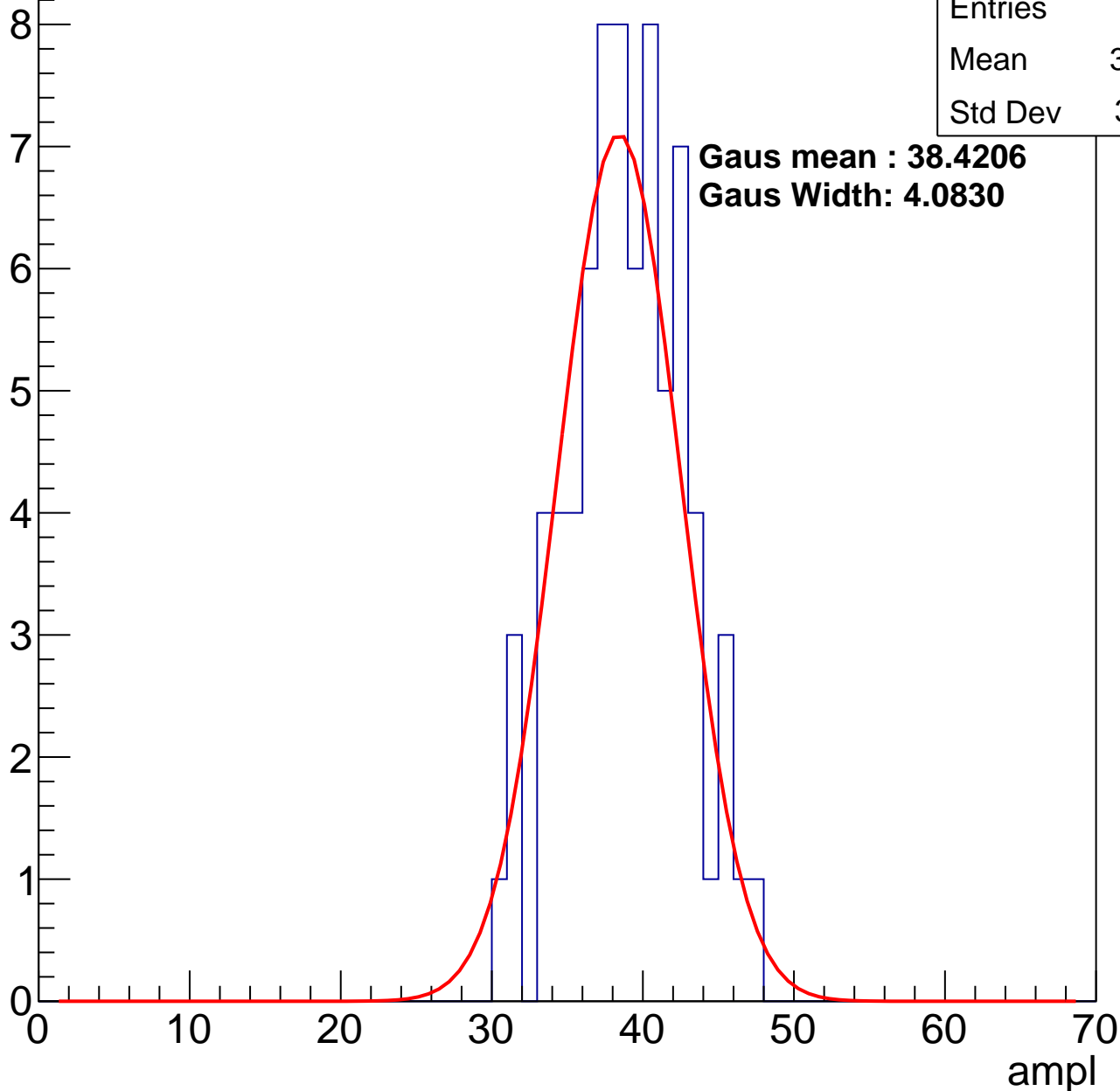
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	38.43
Std Dev	3.771

**Gaus mean : 38.4206**

**Gaus Width: 4.0830**



# B1L101S, U11-ch87, adc2

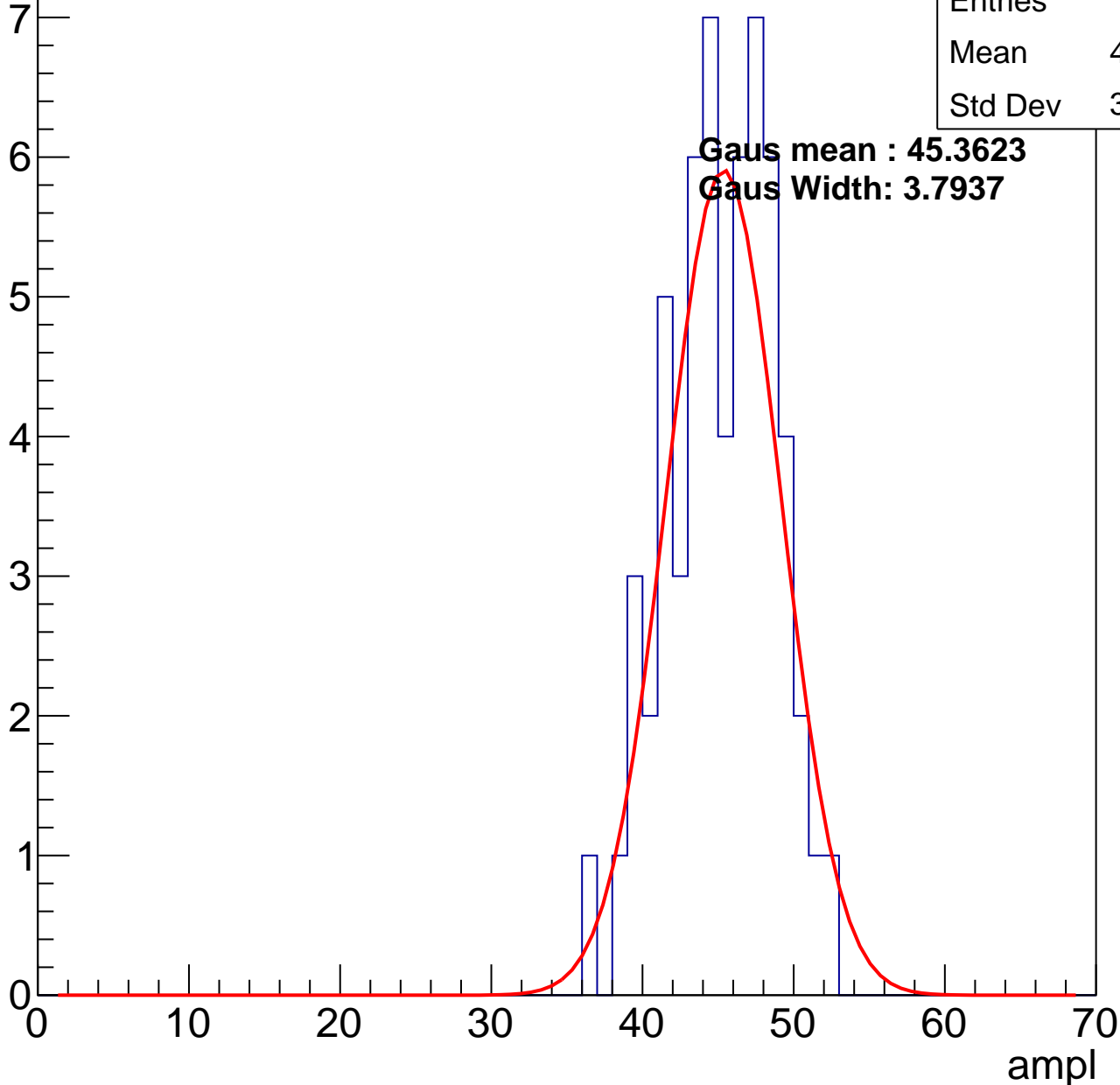
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	44.75
Std Dev	3.467

Gaus mean : 45.3623

Gaus Width: 3.7937

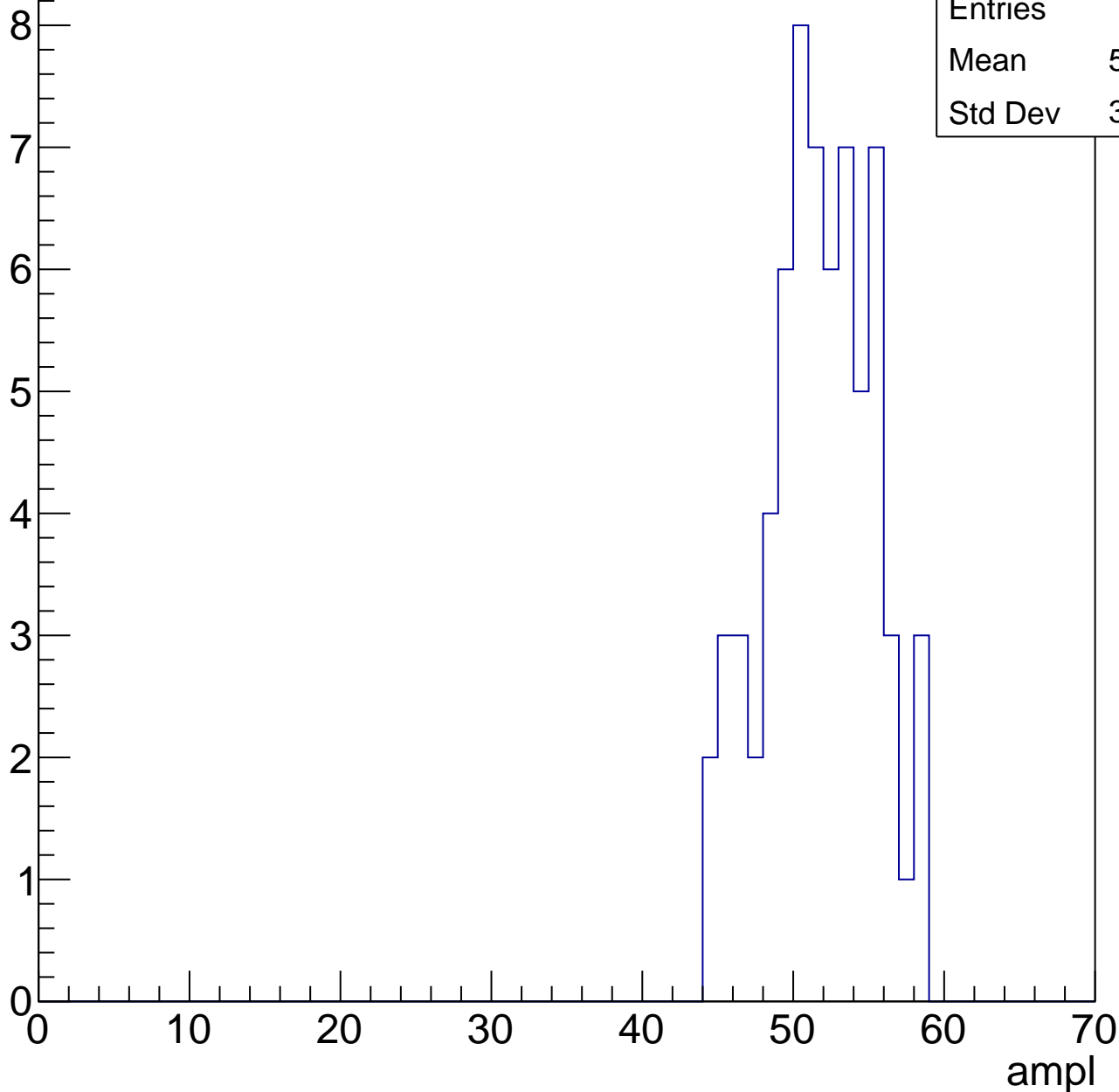


# B1L101S, U11-ch87, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

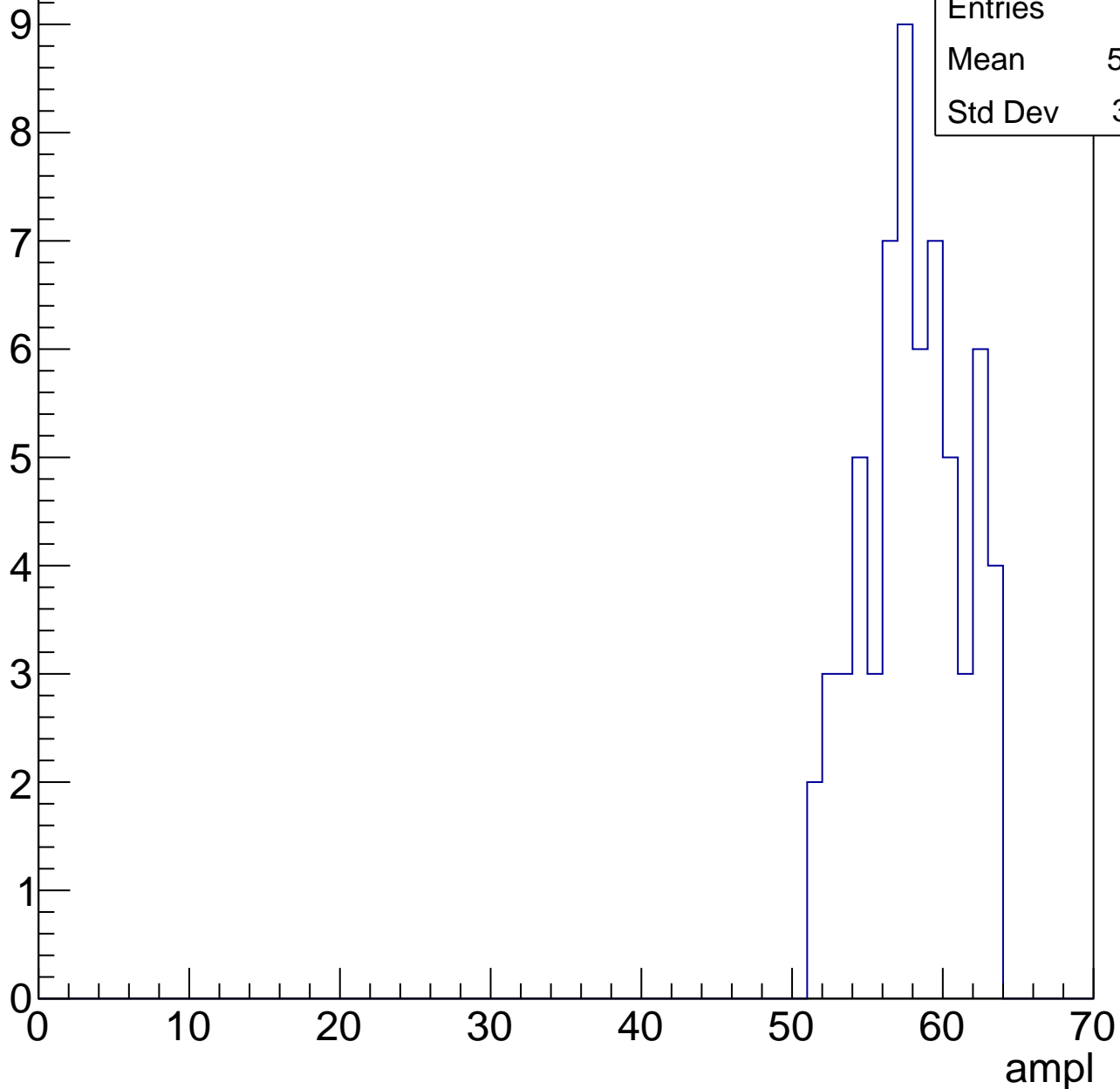
Entries	67
Mean	51.27
Std Dev	3.509



# B1L101S, U11-ch87, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



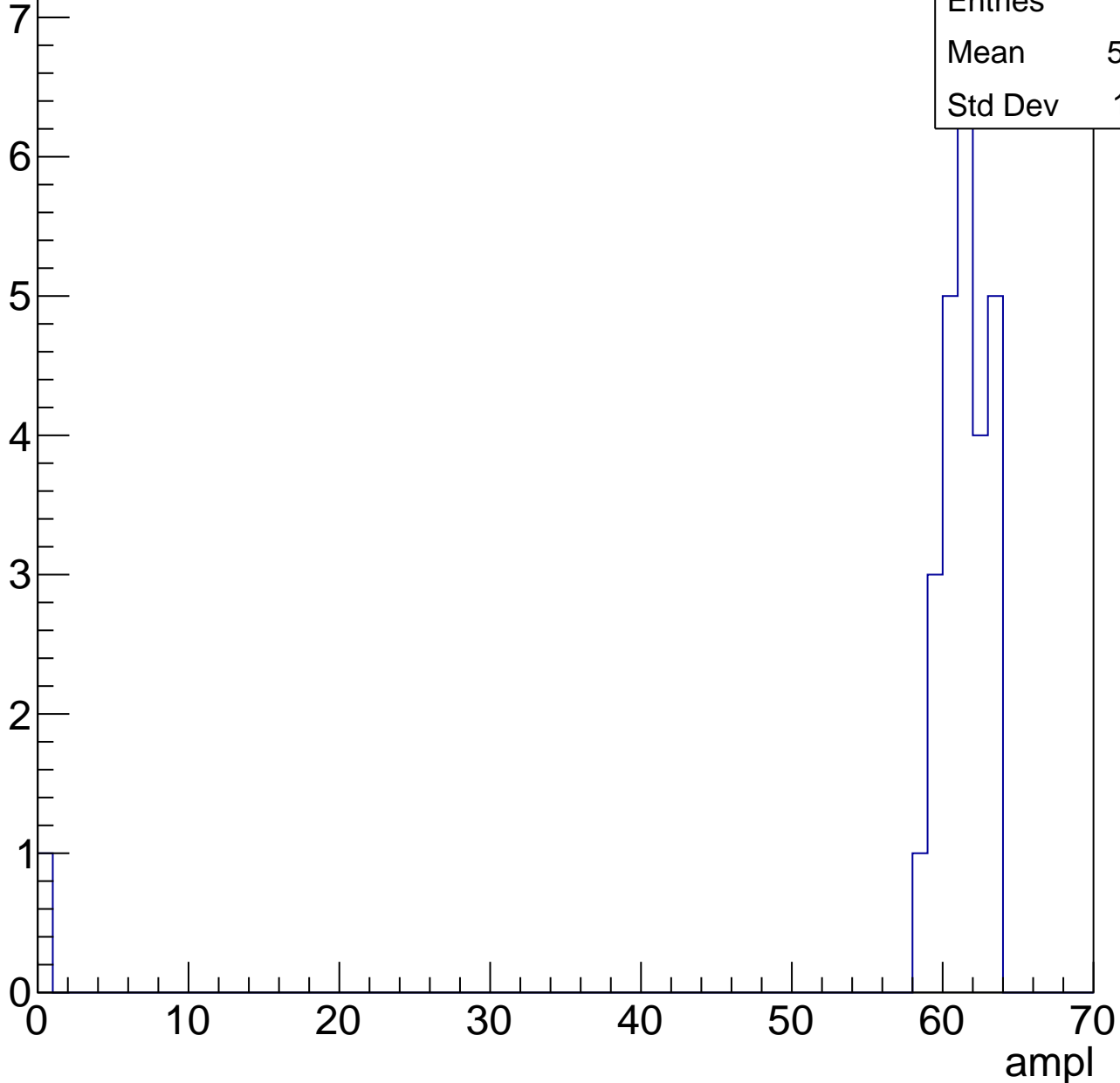
Entries	63
Mean	57.54
Std Dev	3.241

# B1L101S, U11-ch87, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	26
Mean	58.65
Std Dev	11.81



# B1L101S, U11-ch87, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch87, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U11-ch88, adc0

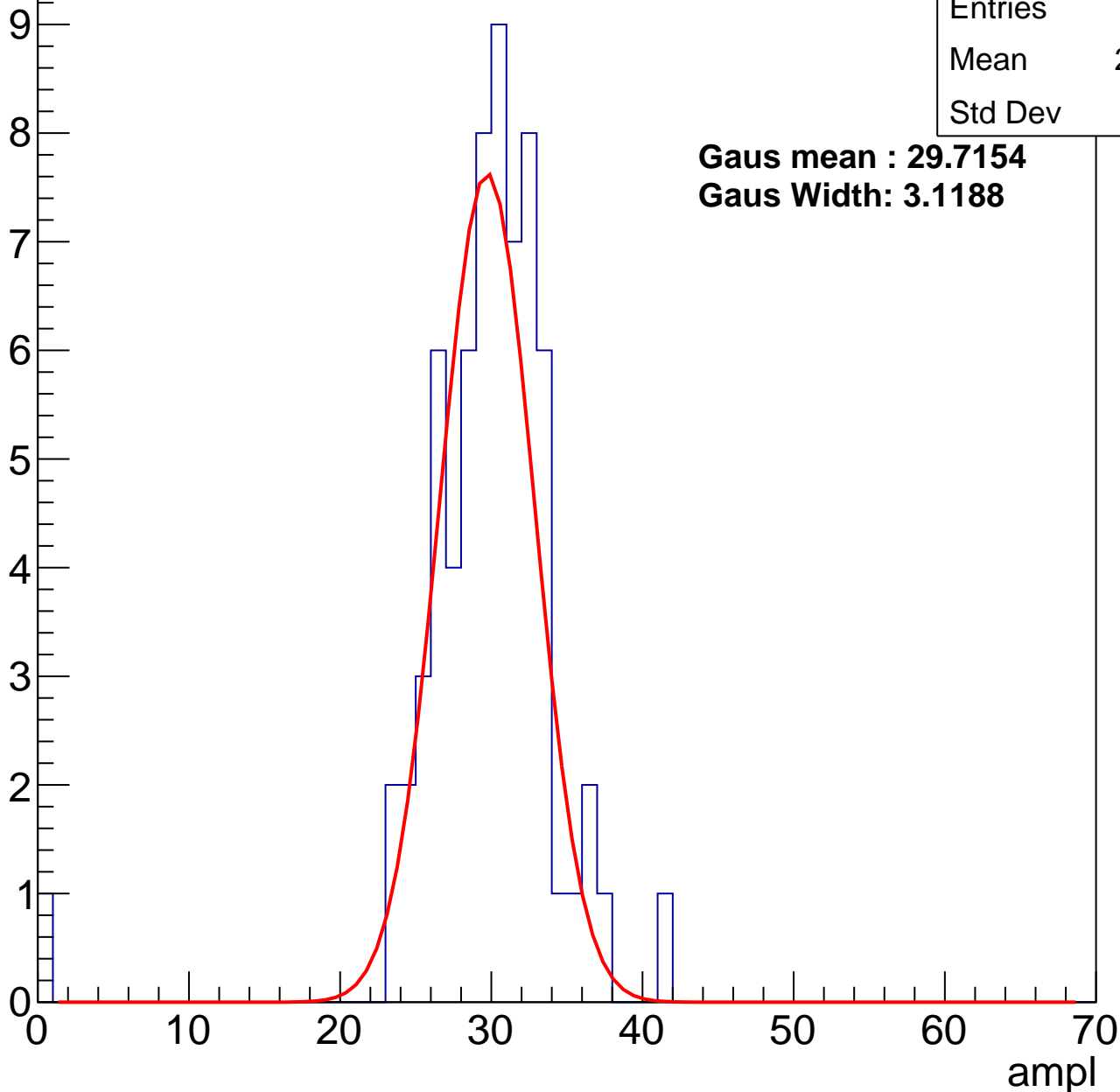
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	29.31
Std Dev	4.93

**Gaus mean : 29.7154**

**Gaus Width: 3.1188**



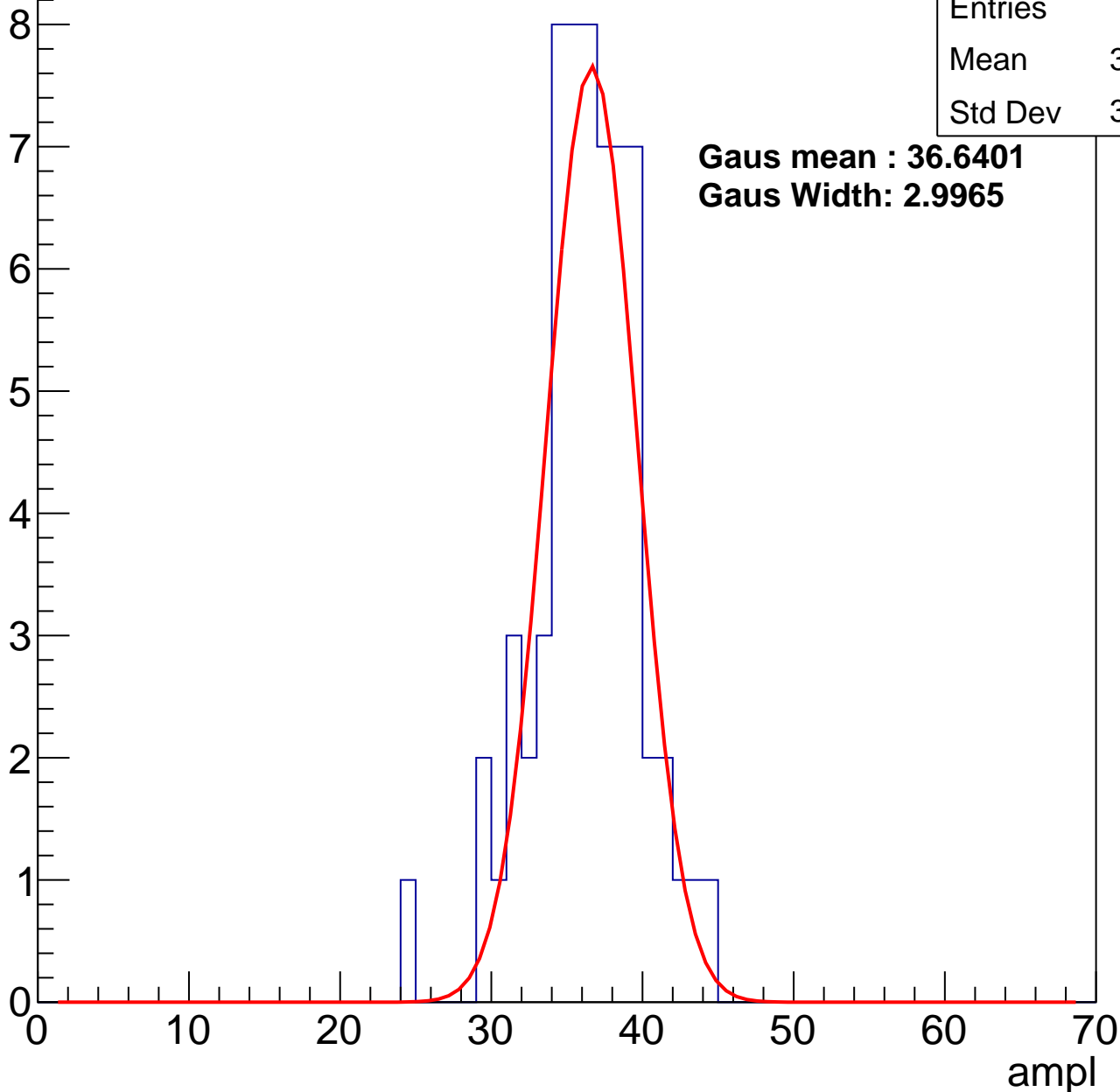
# B1L101S, U11-ch88, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	35.89
Std Dev	3.492

**Gaus mean : 36.6401**  
**Gaus Width: 2.9965**



# B1L101S, U11-ch88, adc2

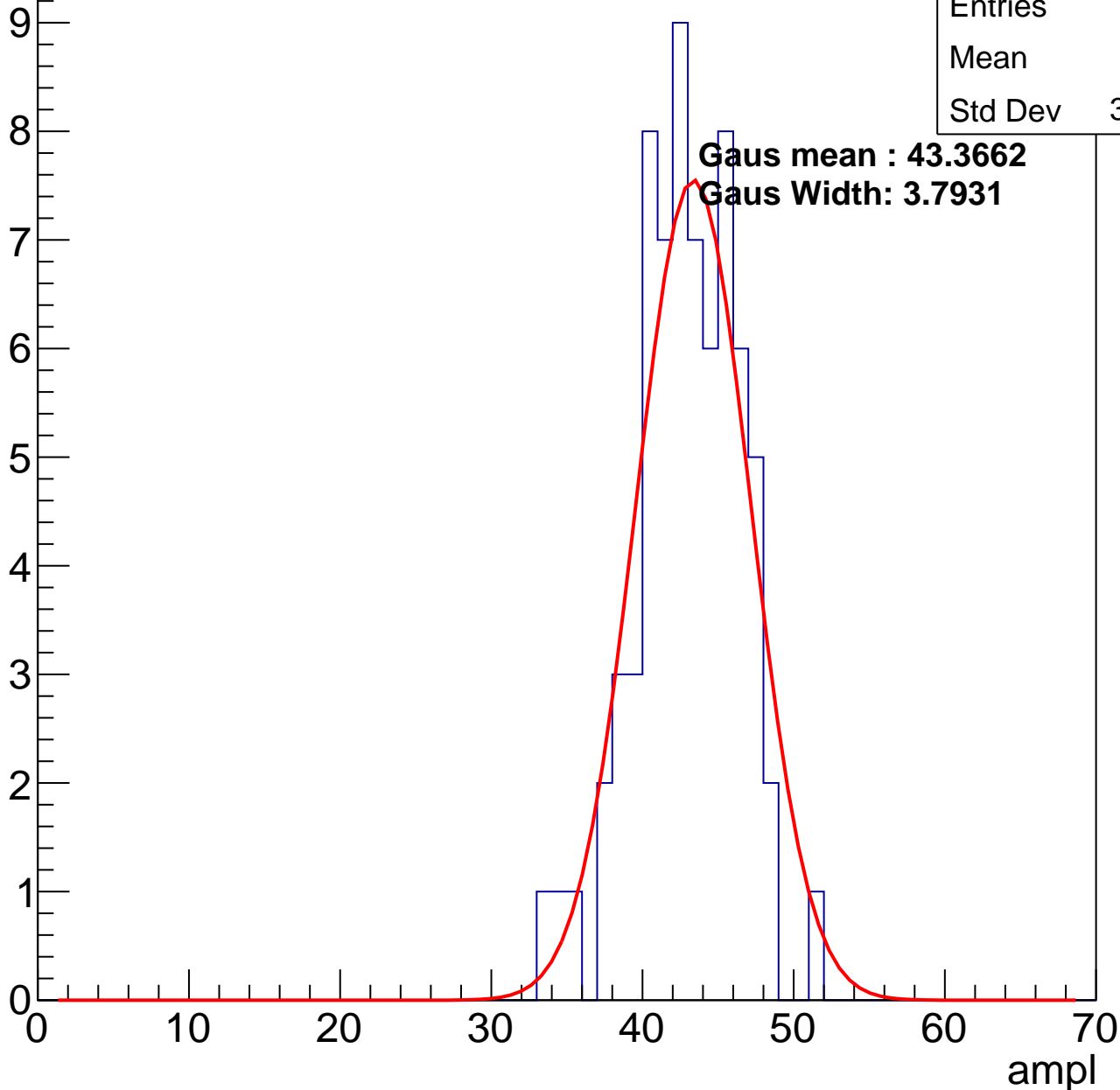
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	42.5
Std Dev	3.417

**Gaus mean : 43.3662**

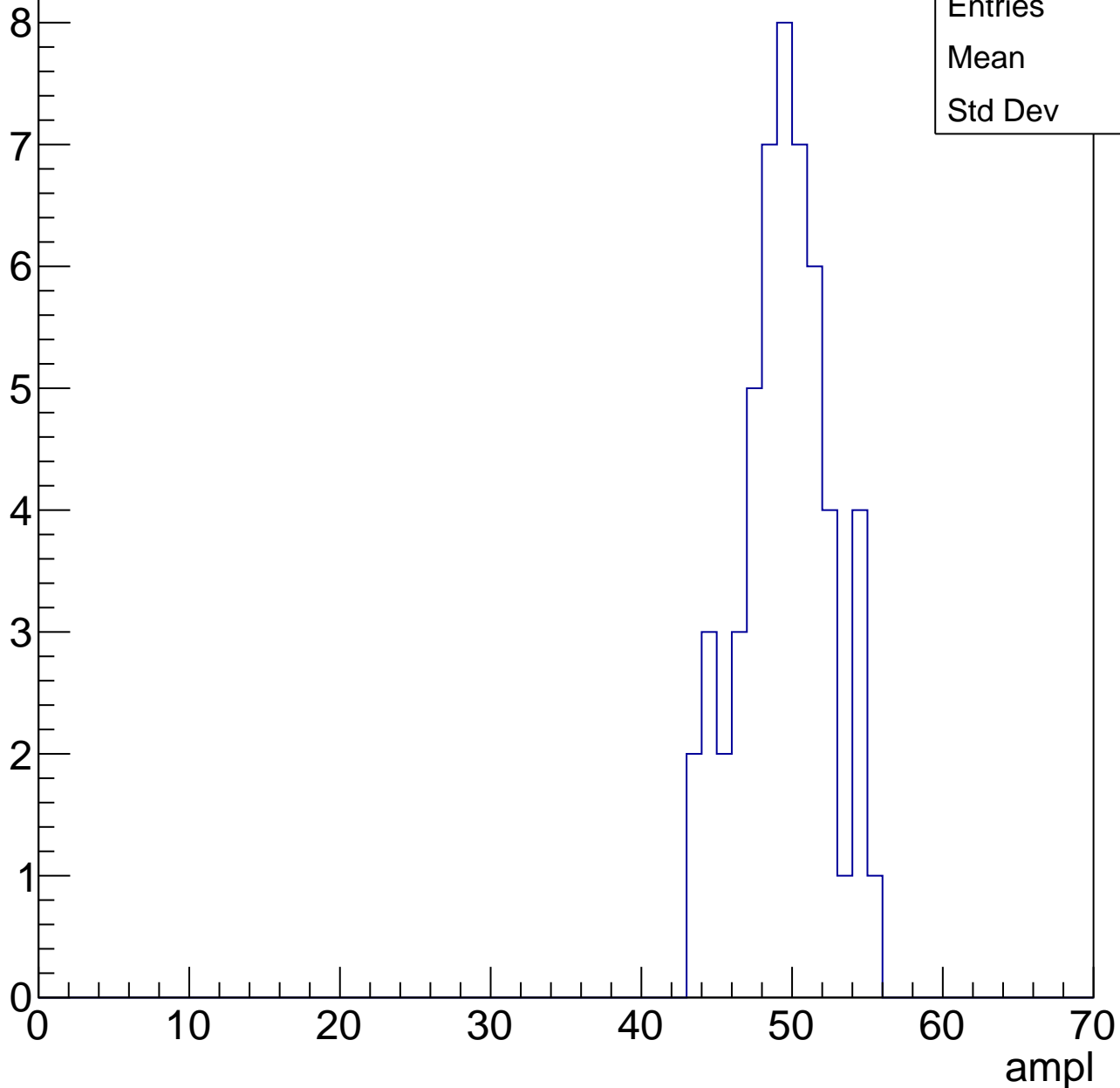
**Gaus Width: 3.7931**



# B1L101S, U11-ch88, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



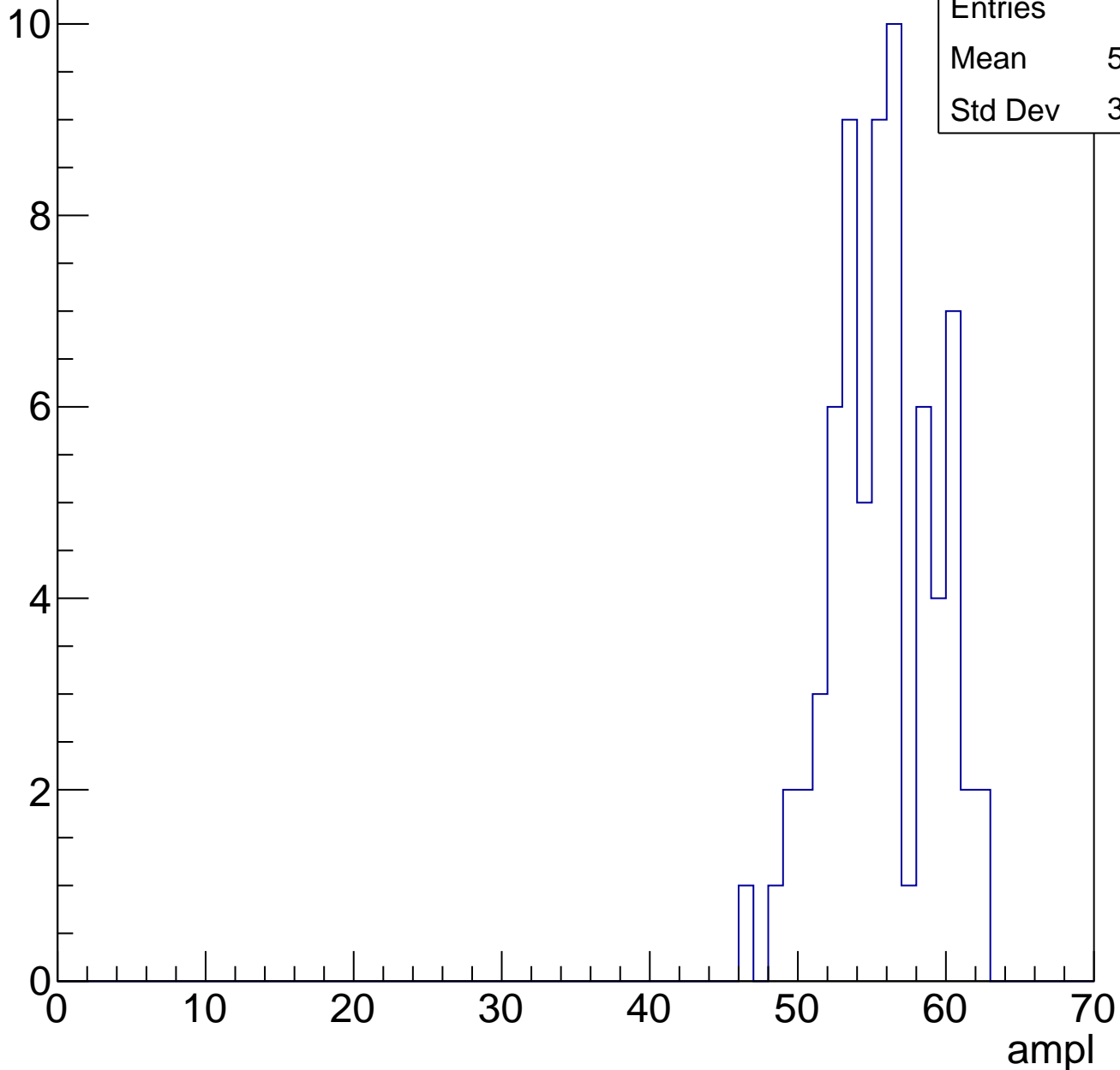
Entries	53
Mean	49
Std Dev	2.92

# B1L101S, U11-ch88, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	70
Mean	55.23
Std Dev	3.522

Entry

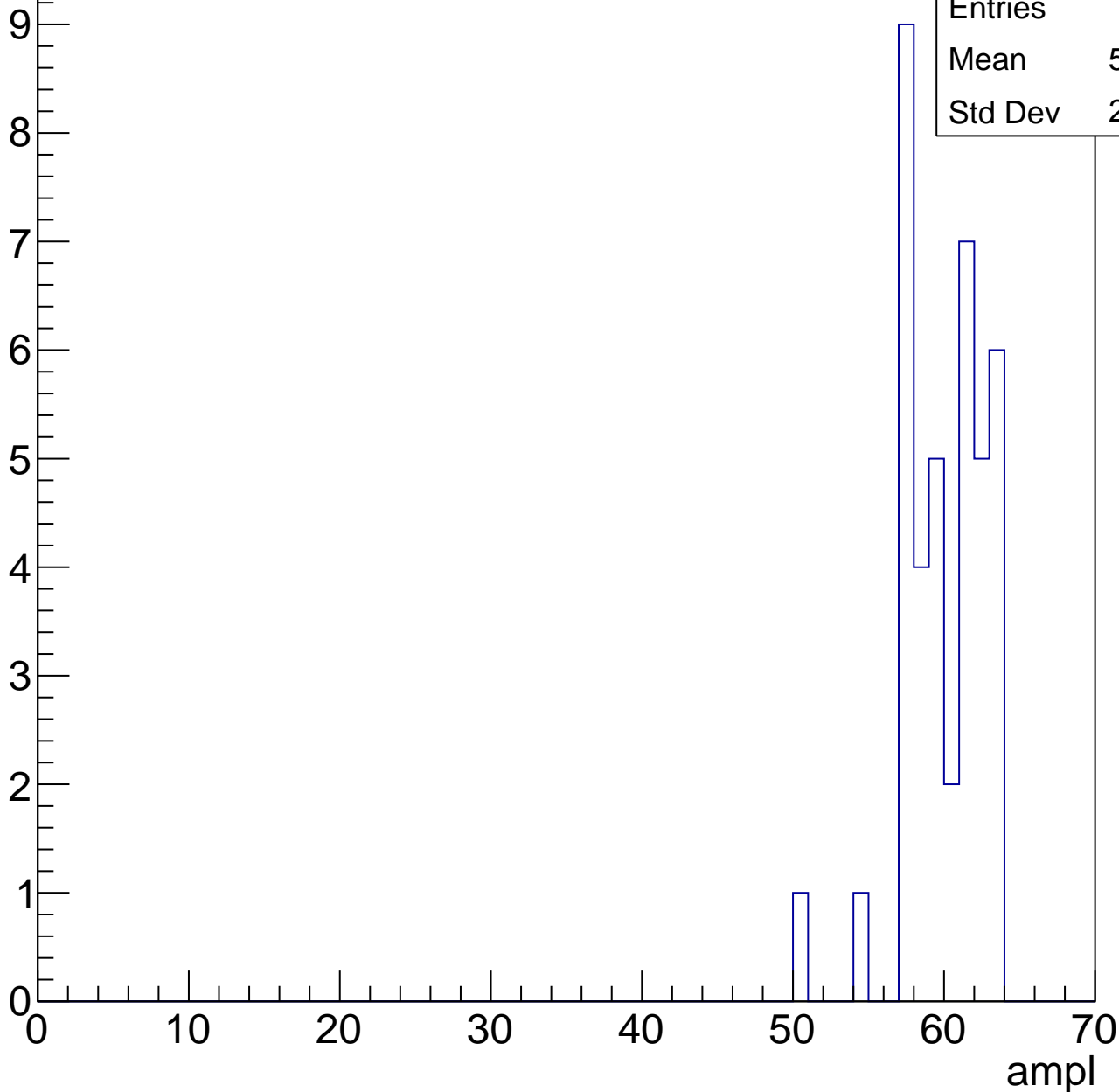


# B1L101S, U11-ch88, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

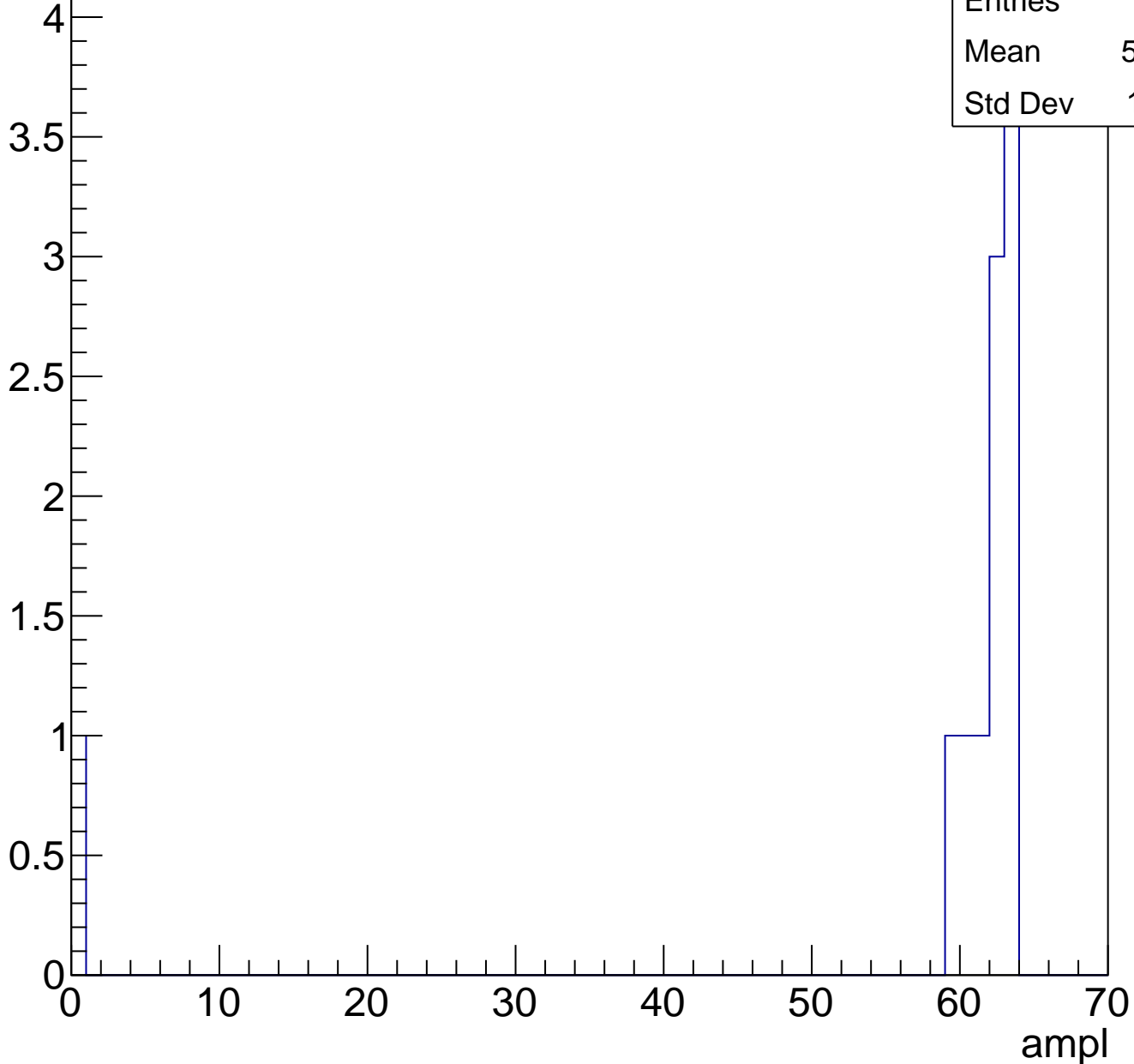
Entries	40
Mean	59.48
Std Dev	2.775



# B1L101S, U11-ch88, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch88, adc7

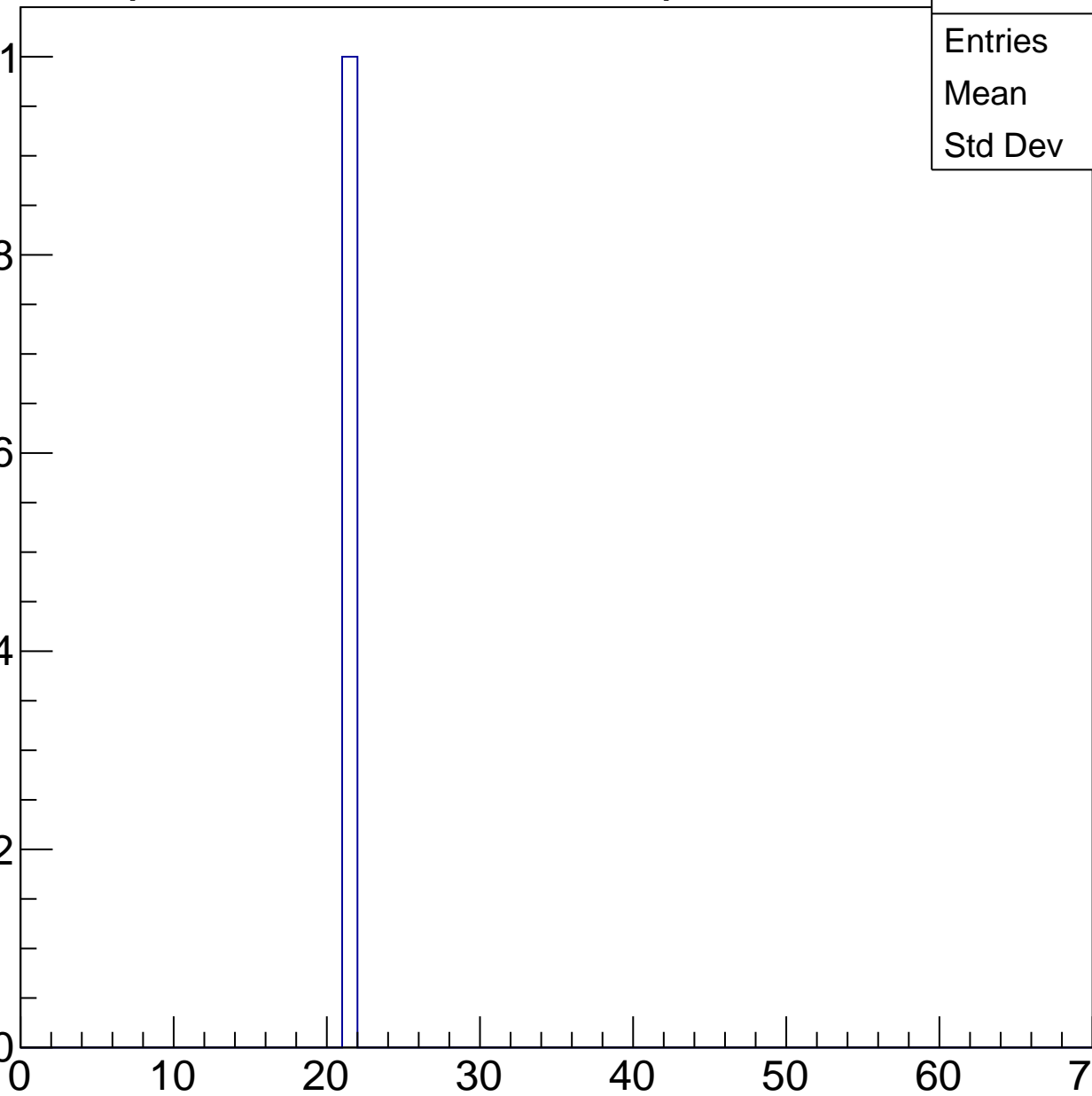
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	21
Std Dev	0

ampl



# B1L101S, U11-ch89, adc0

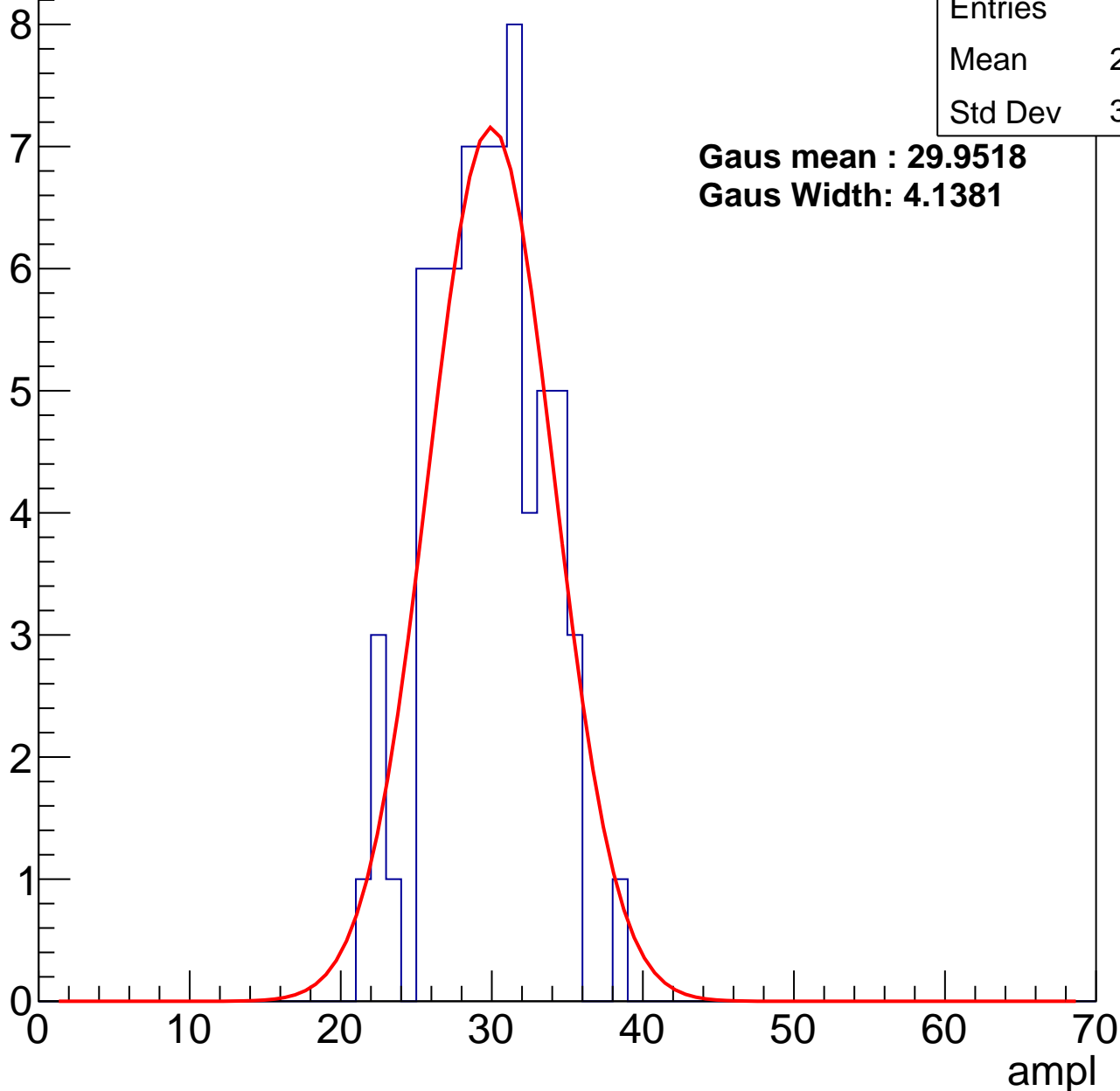
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	29.16
Std Dev	3.576

**Gaus mean : 29.9518**

**Gaus Width: 4.1381**



# B1L101S, U11-ch89, adc1

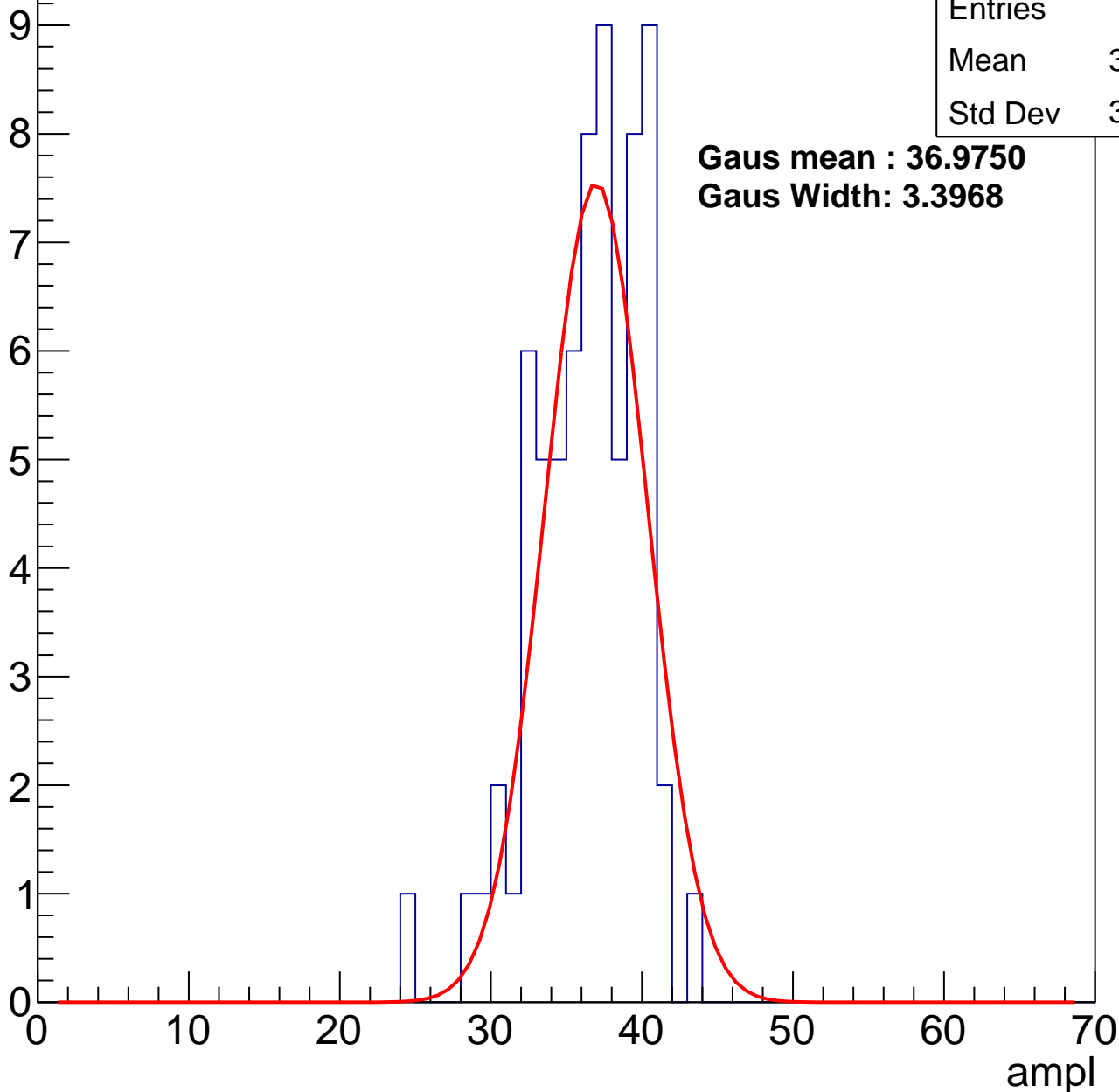
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	35.96
Std Dev	3.515

**Gaus mean : 36.9750**

**Gaus Width: 3.3968**



# B1L101S, U11-ch89, adc2

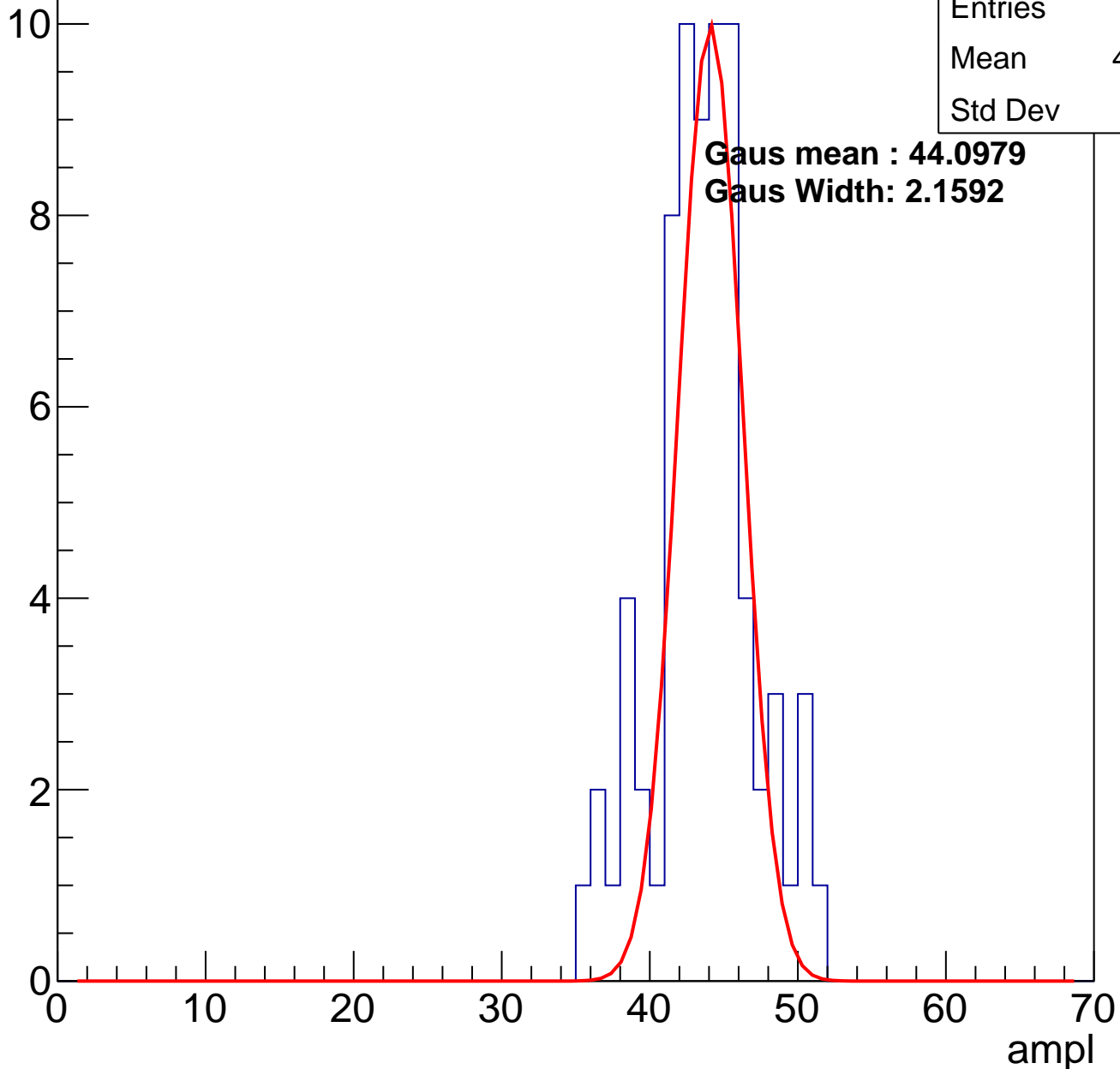
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	72
Mean	43.21
Std Dev	3.37

**Gaus mean : 44.0979**

**Gaus Width: 2.1592**

Entry

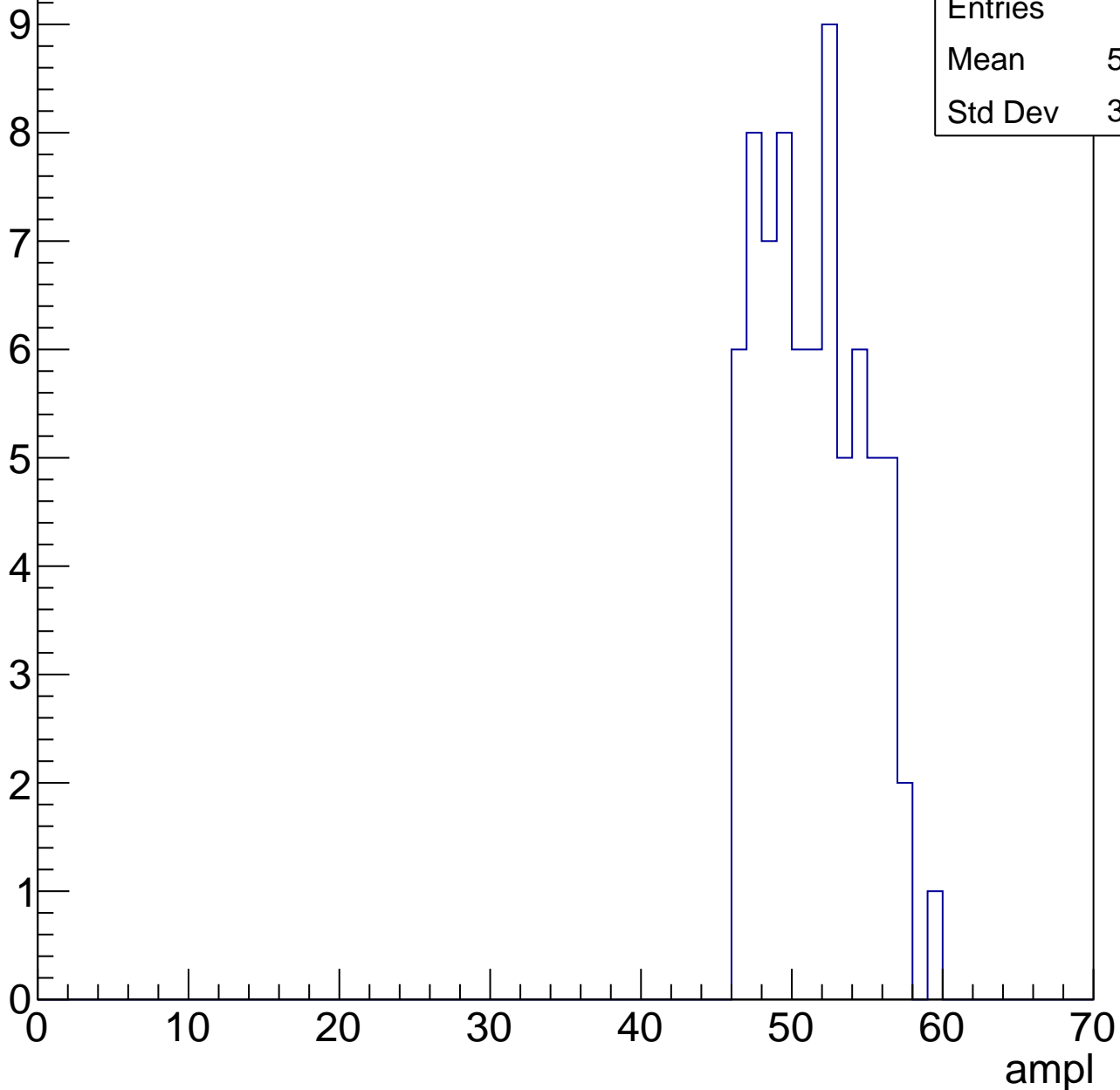


# B1L101S, U11-ch89, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

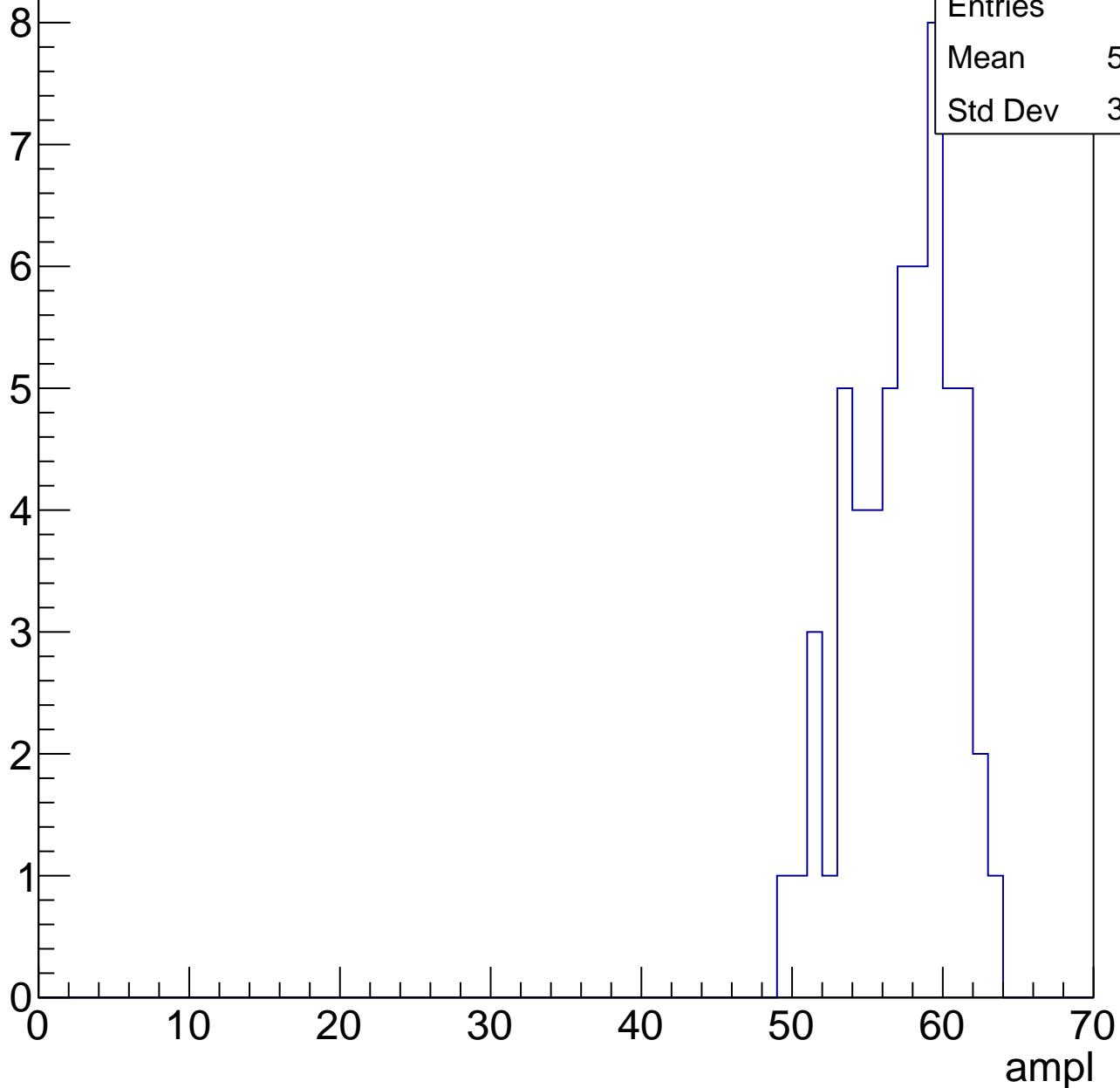
Entries	74
Mean	50.96
Std Dev	3.294



# B1L101S, U11-ch89, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



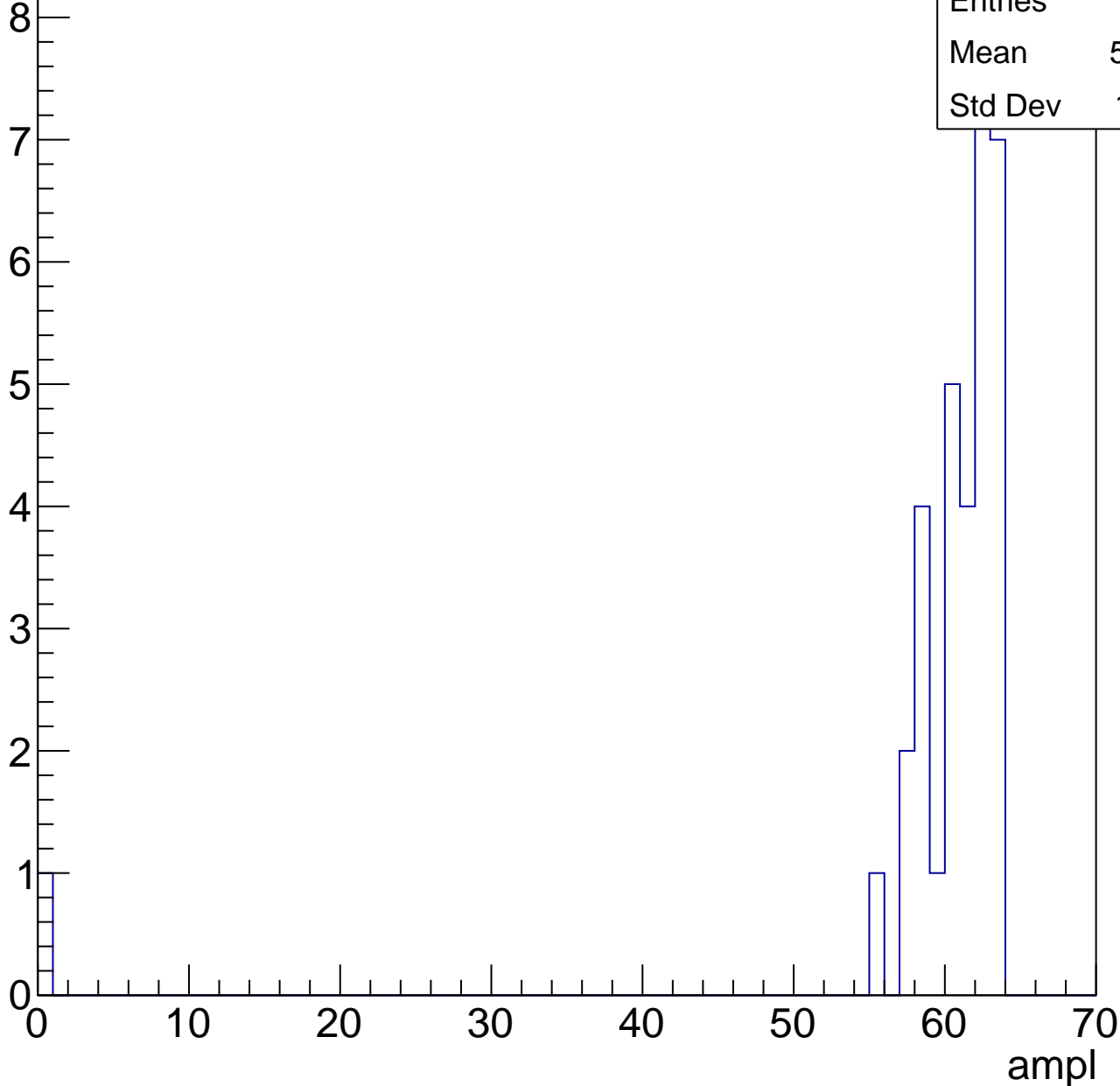
Entries	57
Mean	56.82
Std Dev	3.325

# B1L101S, U11-ch89, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	33
Mean	58.82
Std Dev	10.61



# B1L101S, U11-ch89, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch89, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U11-ch90, adc0

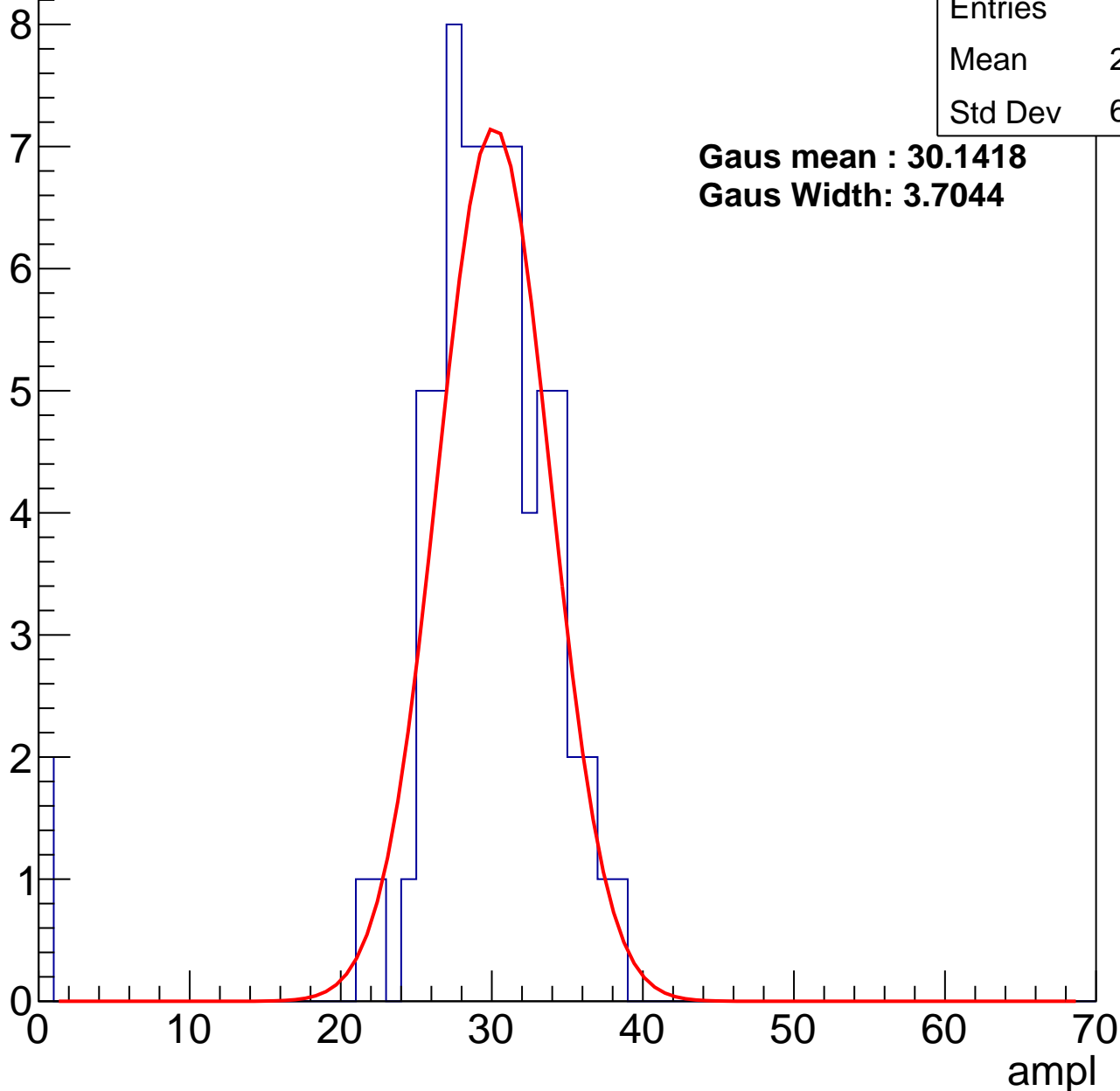
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	28.79
Std Dev	6.019

**Gaus mean : 30.1418**

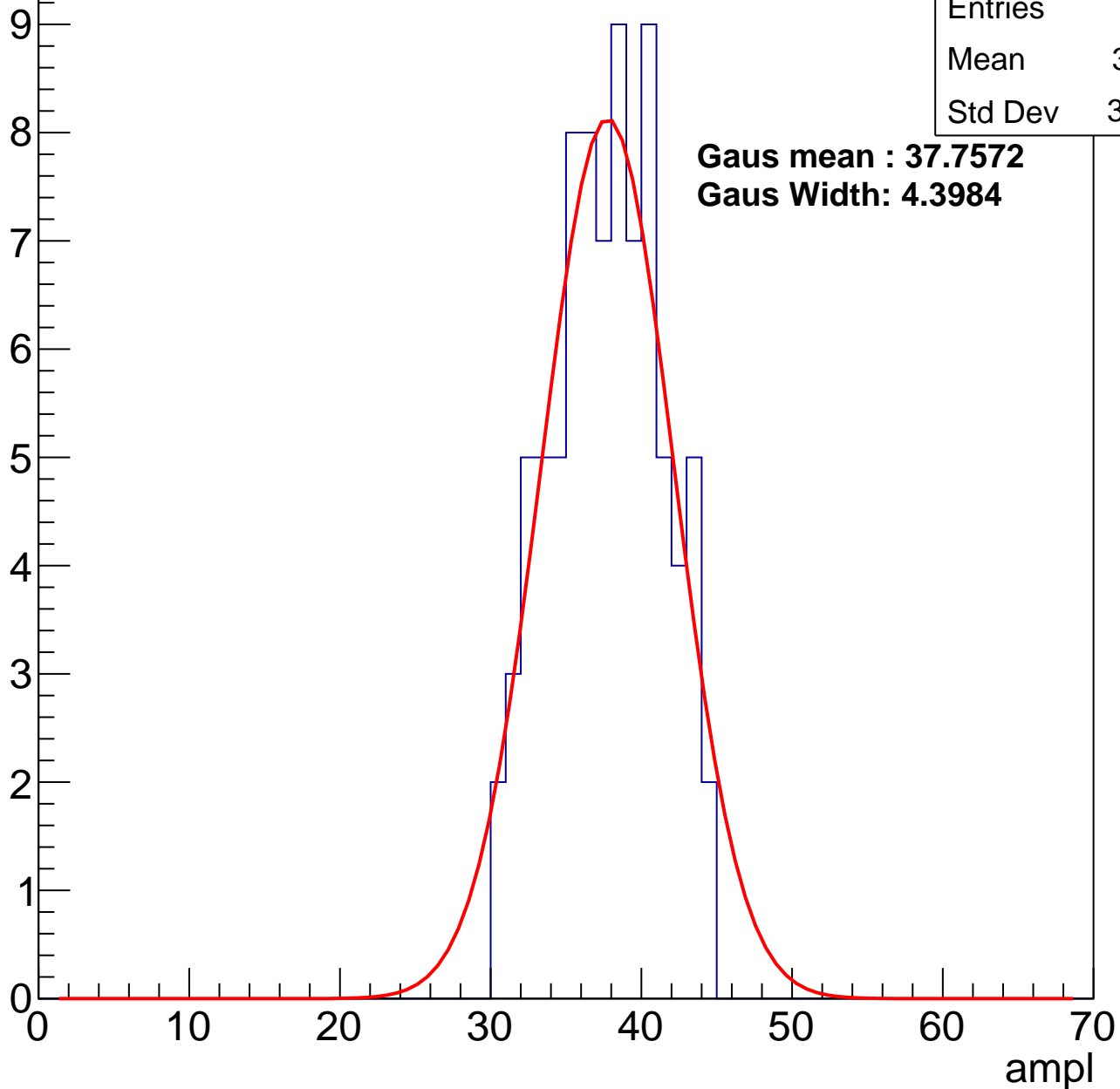
**Gaus Width: 3.7044**



# B1L101S, U11-ch90, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U11-ch90, adc2

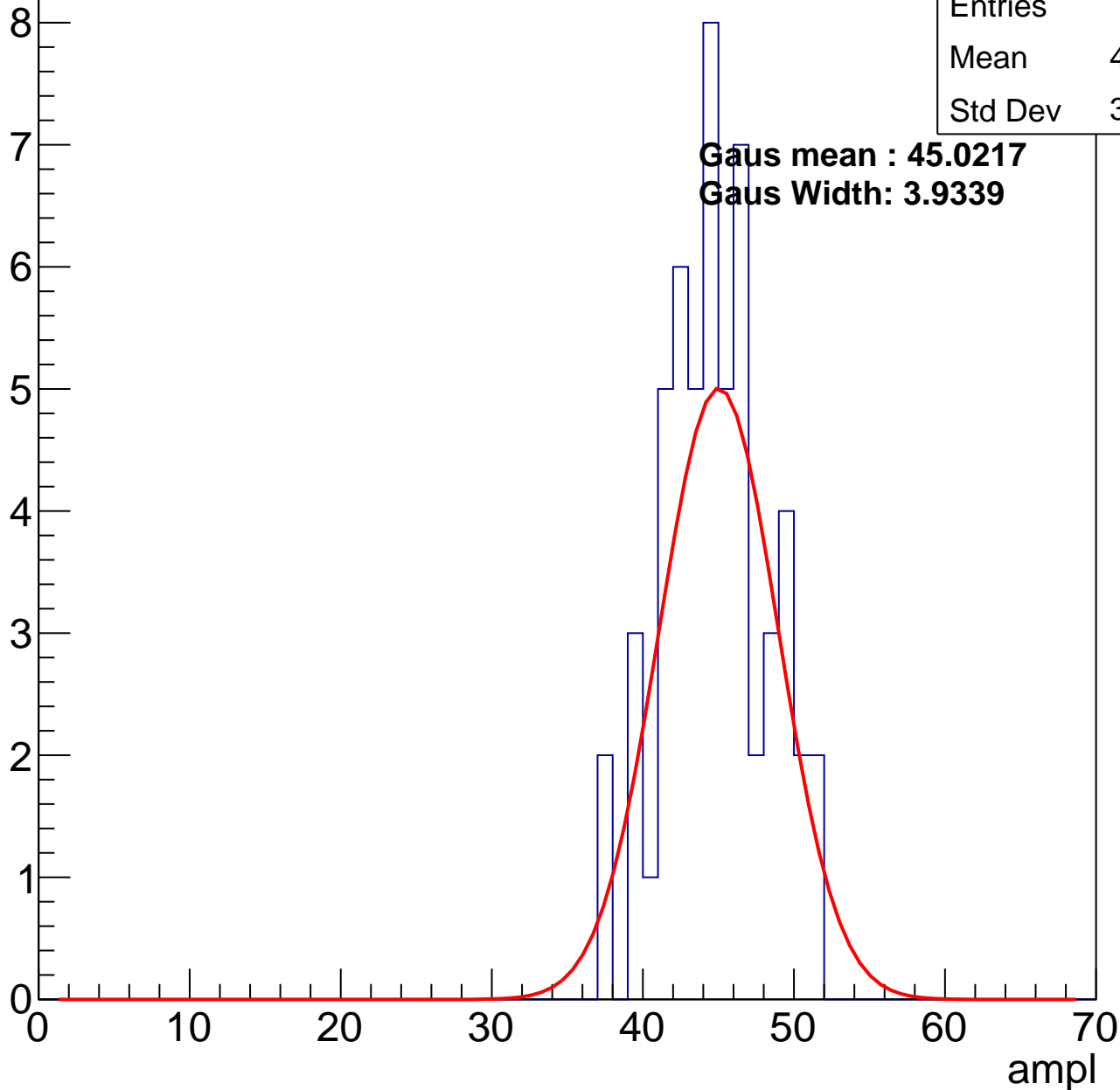
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	44.33
Std Dev	3.374

**Gaus mean : 45.0217**

**Gaus Width: 3.9339**

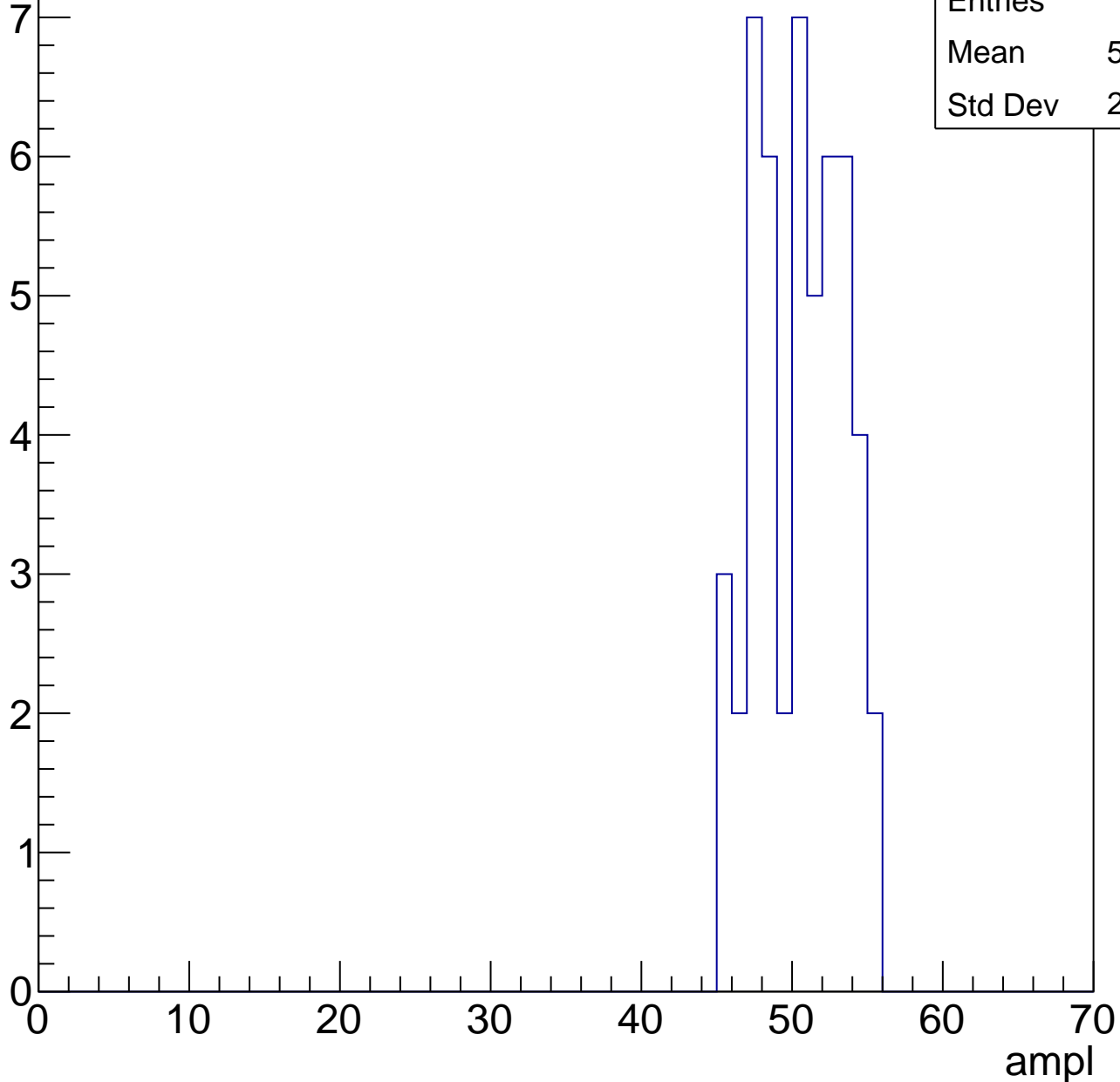


# B1L101S, U11-ch90, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	50.06
Std Dev	2.803



# B1L101S, U11-ch90, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

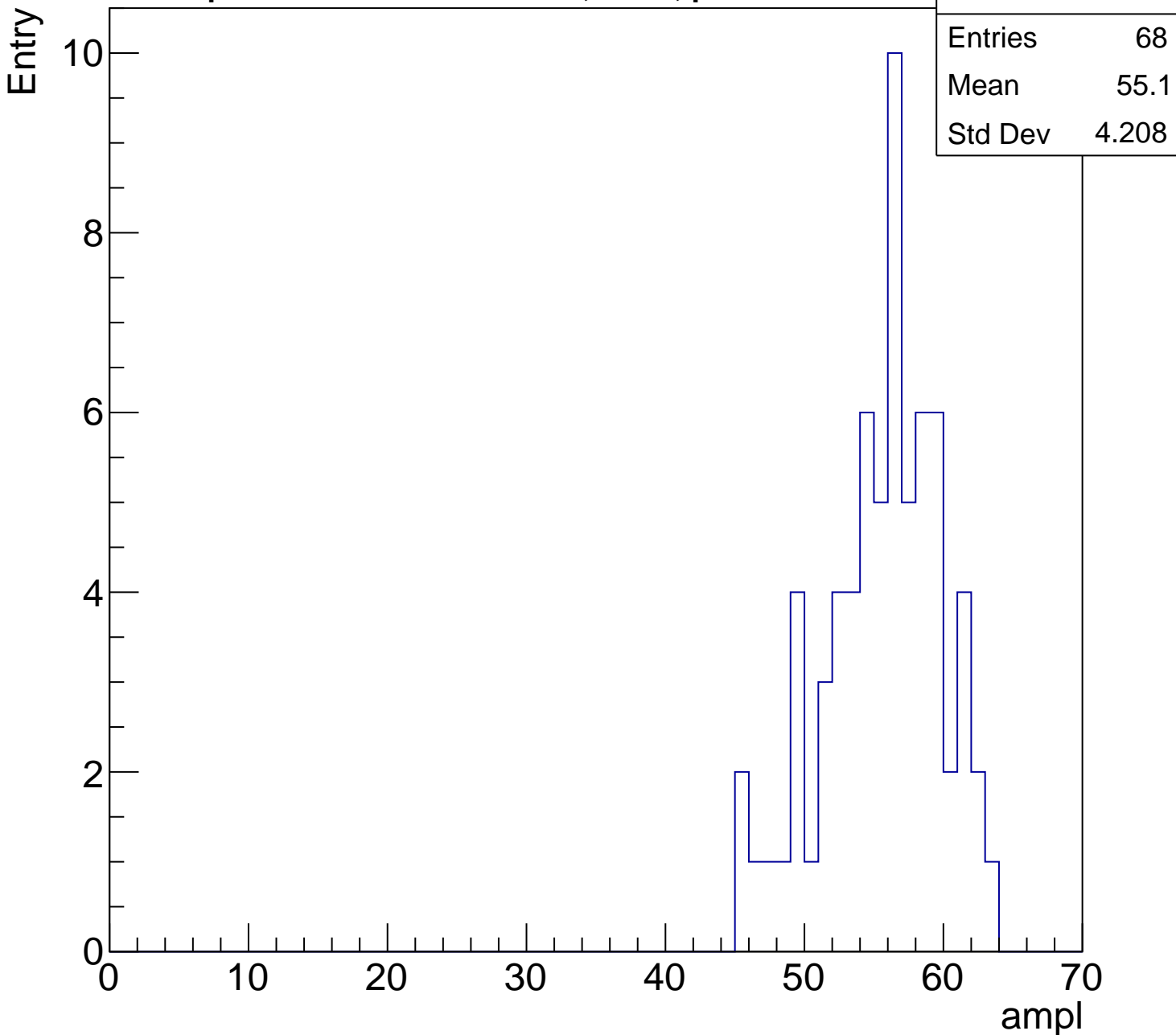
Entries	68
Mean	55.1
Std Dev	4.208

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L101S, U11-ch90, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	43
Mean	58.58
Std Dev	9.317

ampl

0

10

20

30

40

50

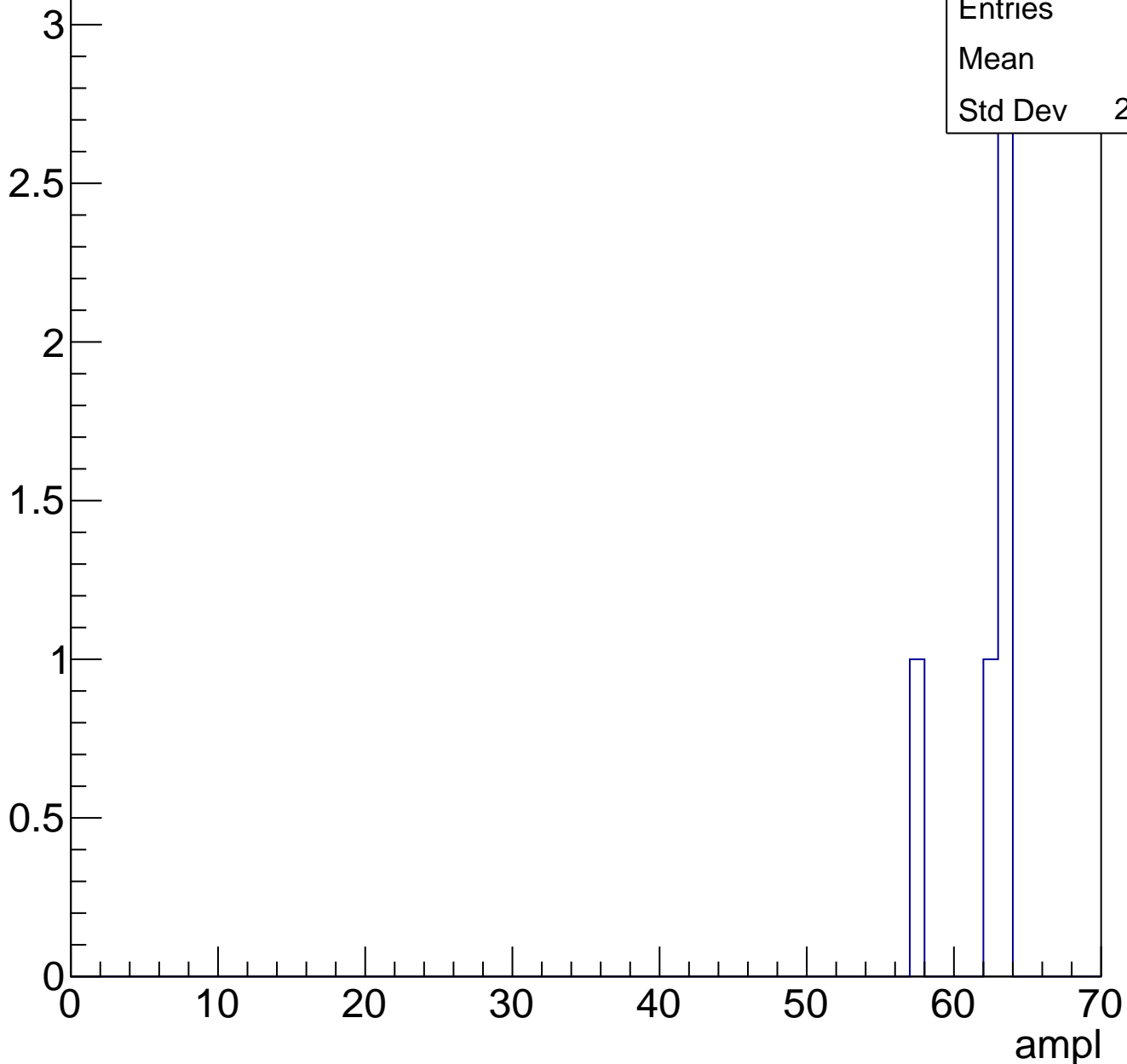
60

70

# B1L101S, U11-ch90, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch90, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U11-ch91, adc0

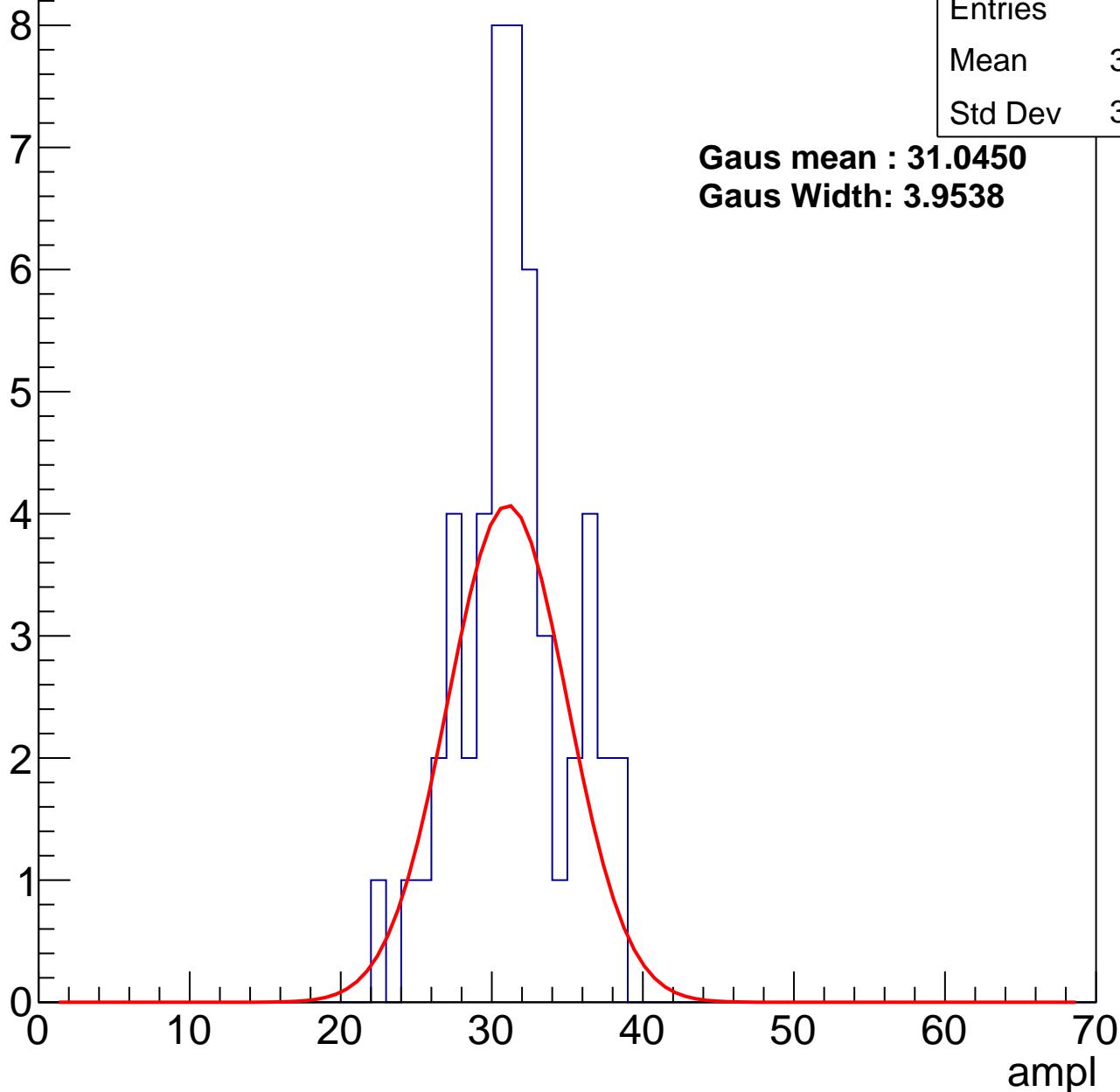
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	30.98
Std Dev	3.573

**Gaus mean : 31.0450**

**Gaus Width: 3.9538**



# B1L101S, U11-ch91, adc1

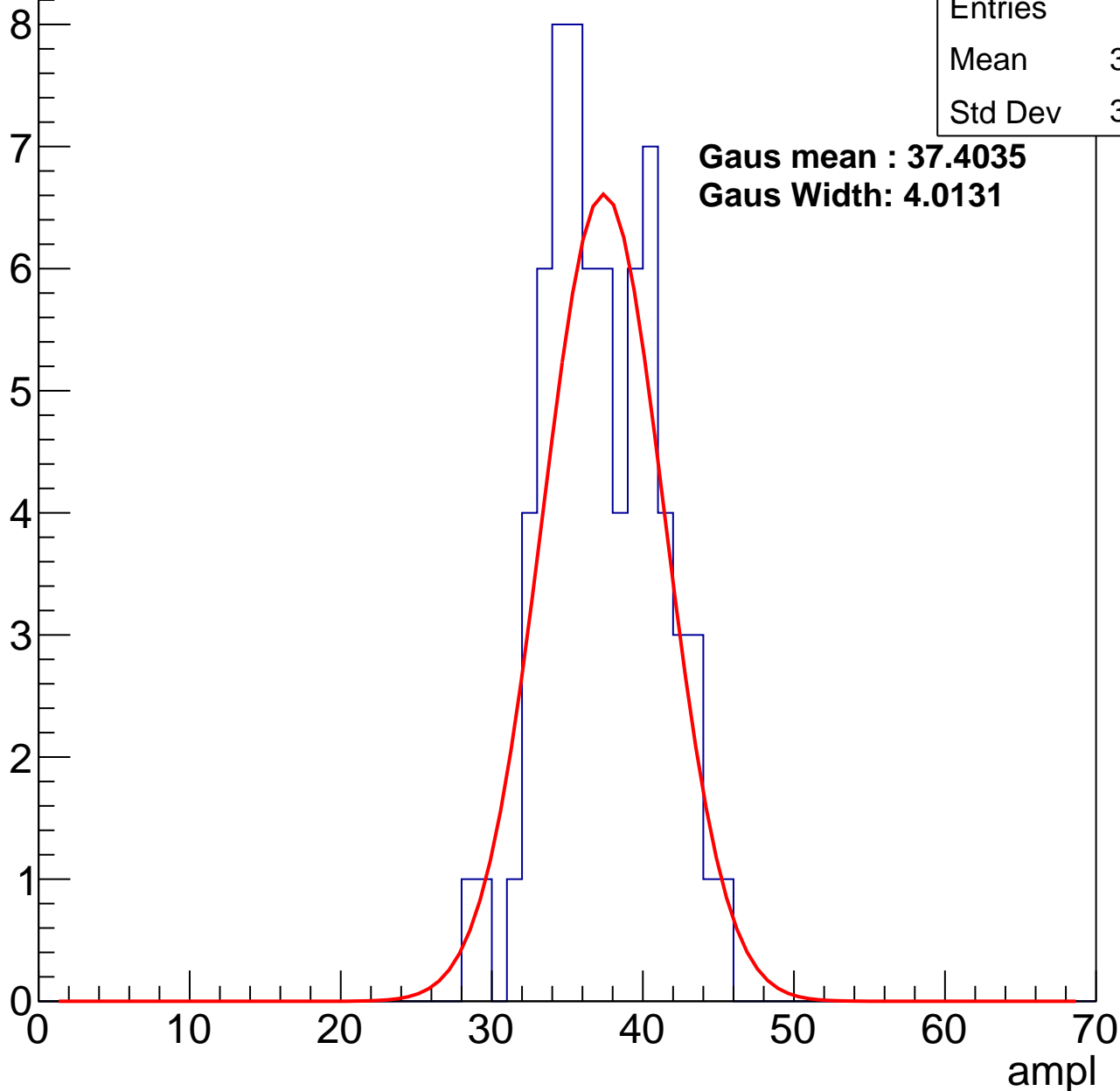
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	36.83
Std Dev	3.657

**Gaus mean : 37.4035**

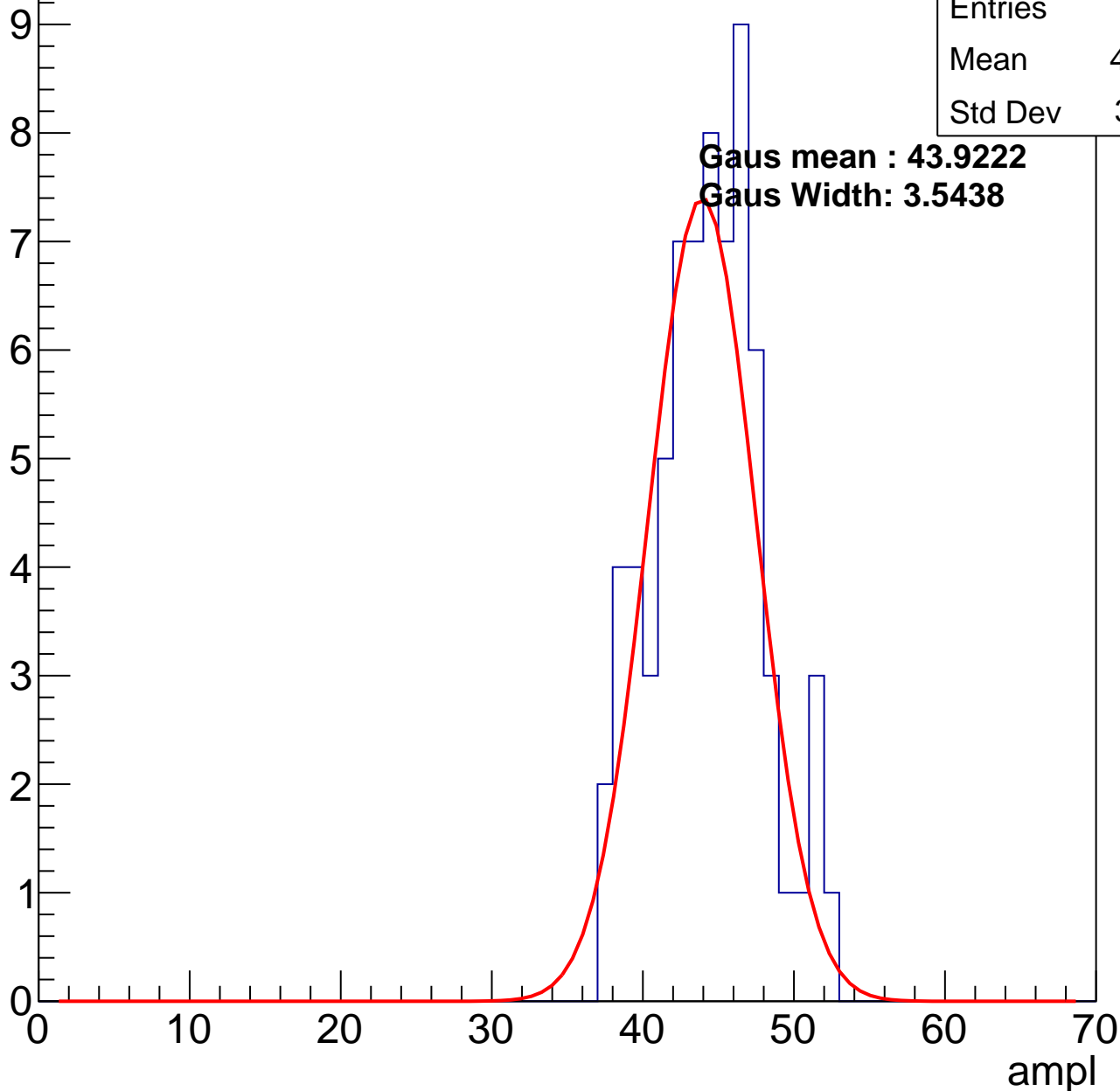
**Gaus Width: 4.0131**



# B1L101S, U11-ch91, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

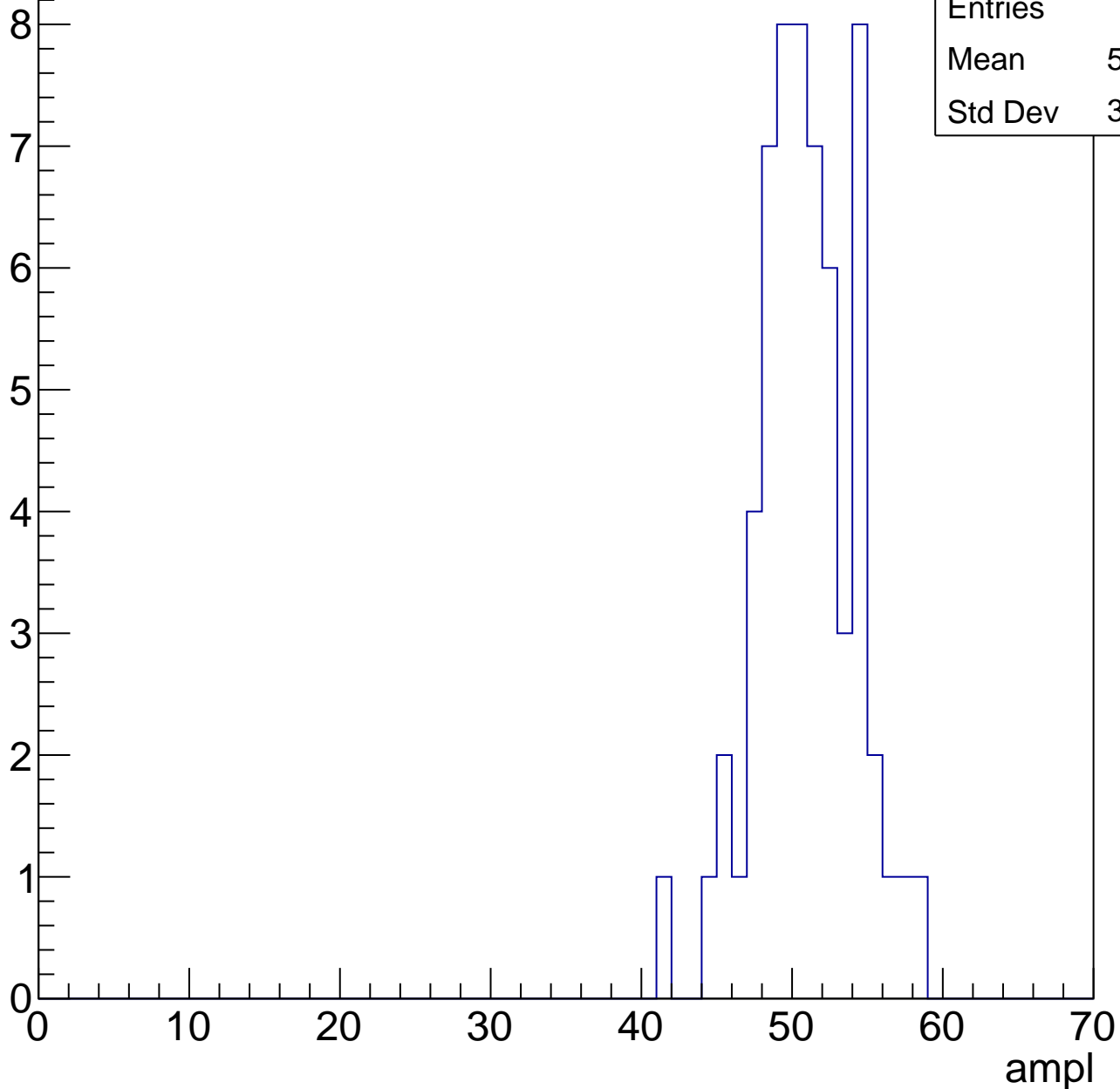


# B1L101S, U11-ch91, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	50.46
Std Dev	3.206

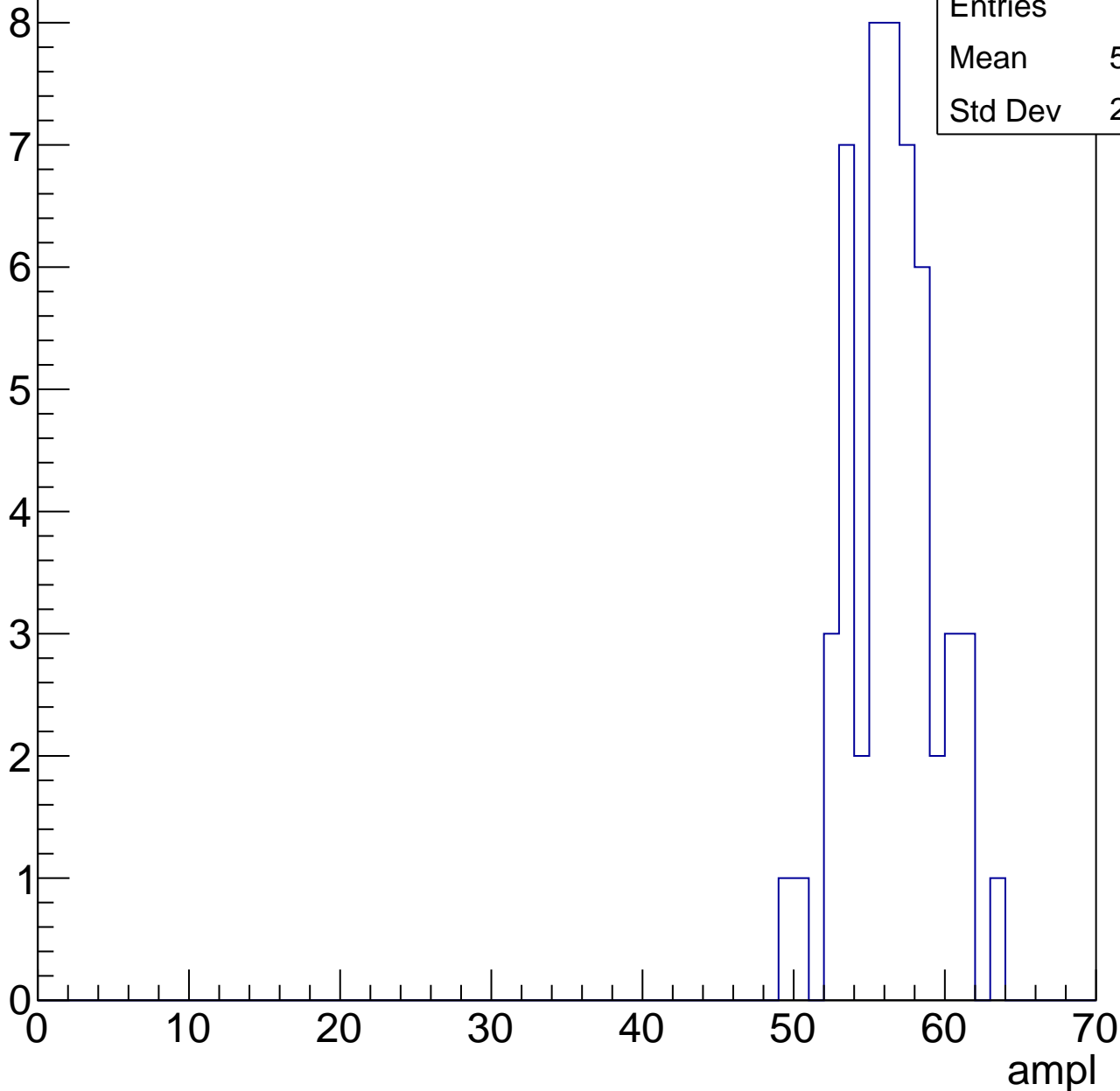


# B1L101S, U11-ch91, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

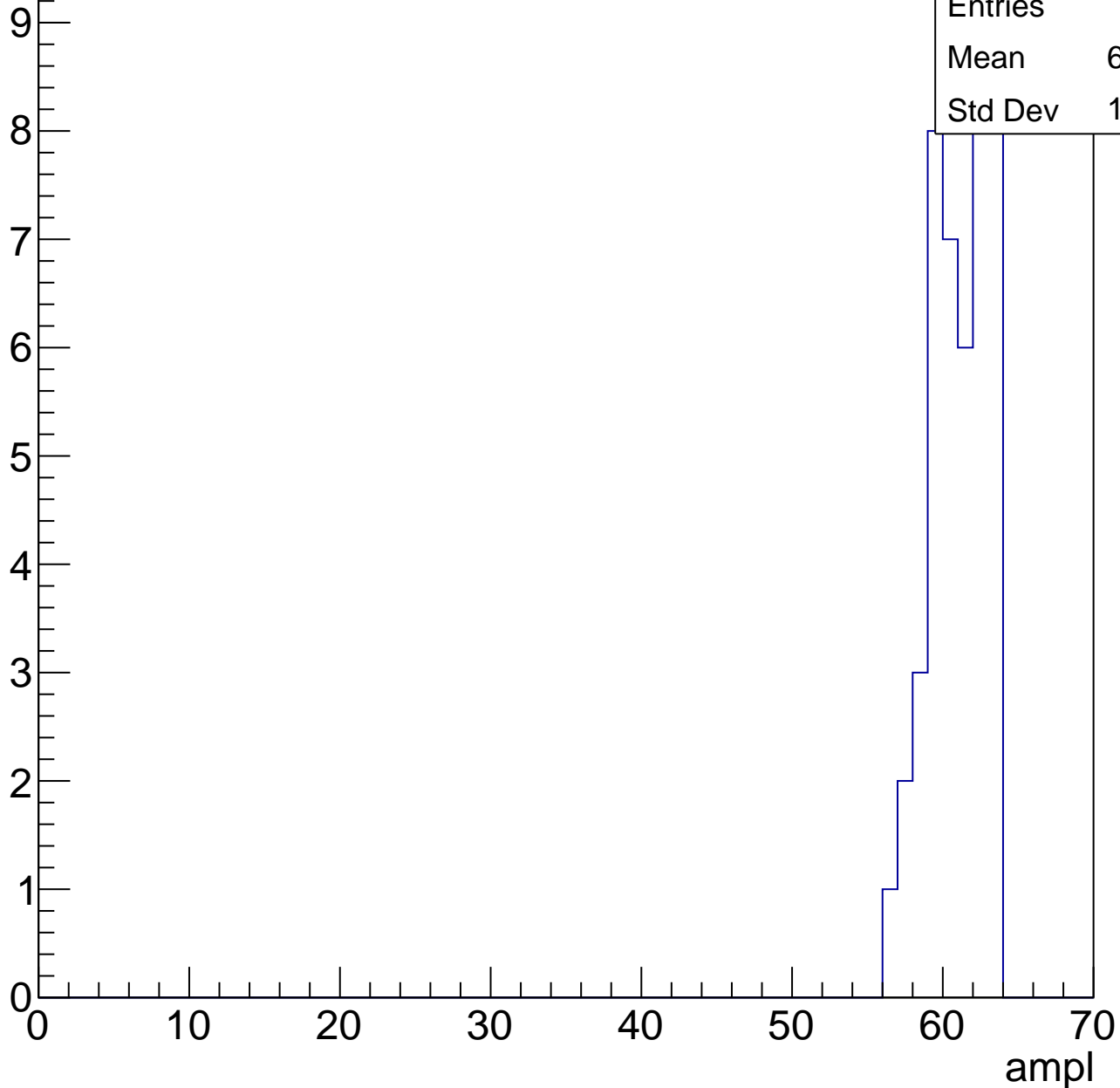
Entries	52
Mean	56.02
Std Dev	2.886



# B1L101S, U11-ch91, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U11-ch91, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch91, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L101S, U11-ch92, adc0

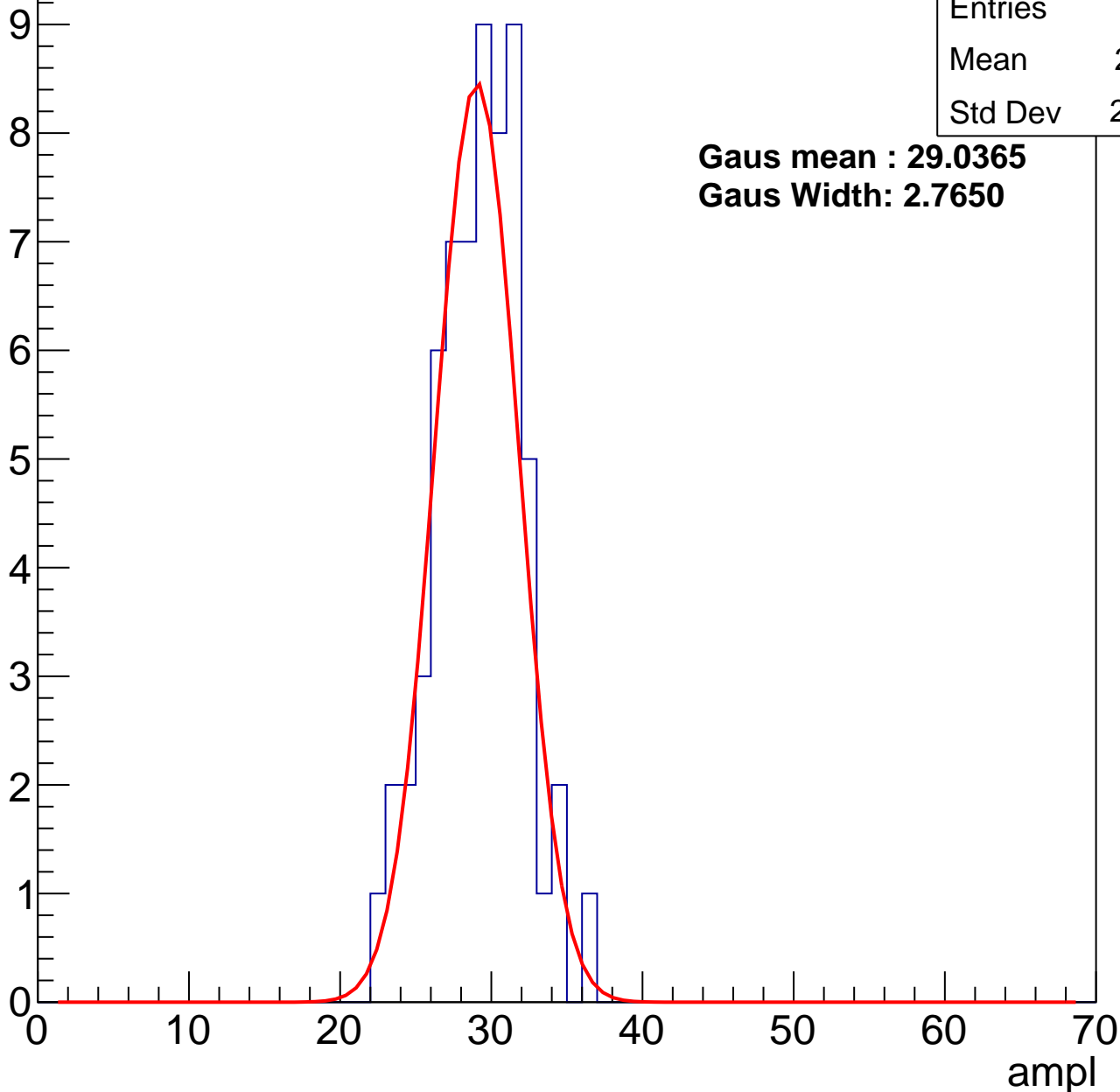
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	28.71
Std Dev	2.836

**Gaus mean : 29.0365**

**Gaus Width: 2.7650**



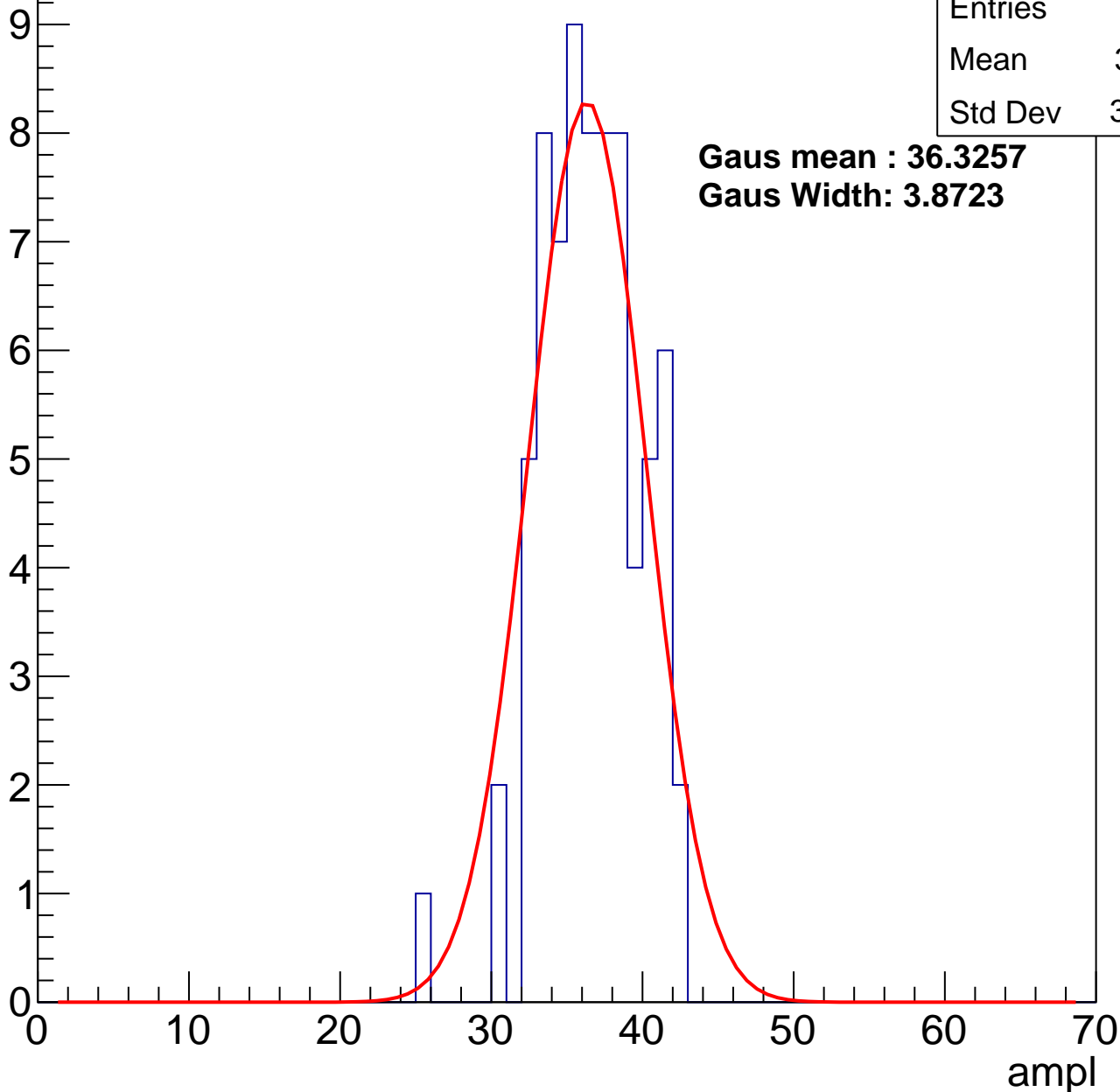
# B1L101S, U11-ch92, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	36.11
Std Dev	3.225

**Gaus mean : 36.3257**  
**Gaus Width: 3.8723**



# B1L101S, U11-ch92, adc2

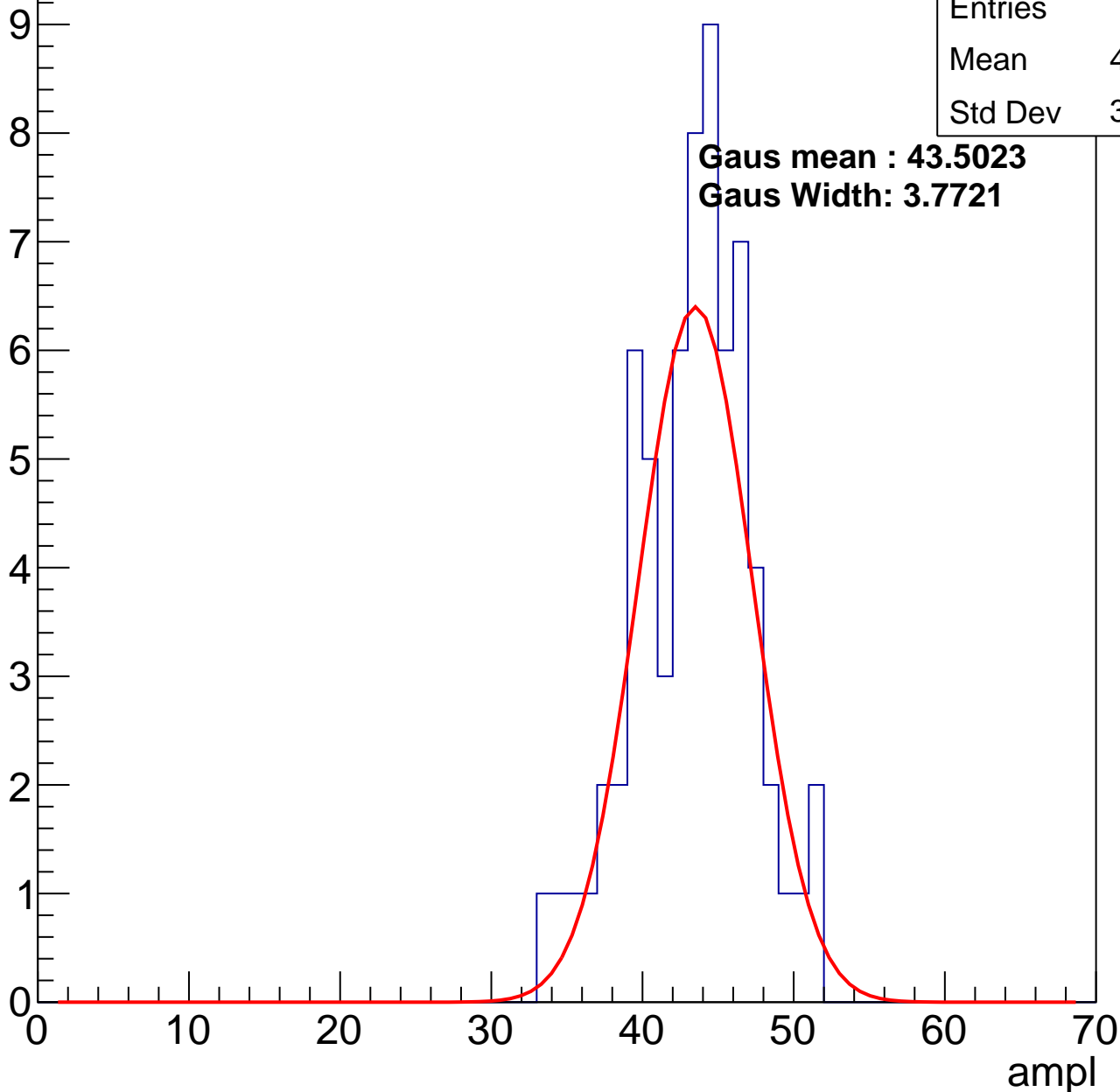
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	42.85
Std Dev	3.828

**Gaus mean : 43.5023**

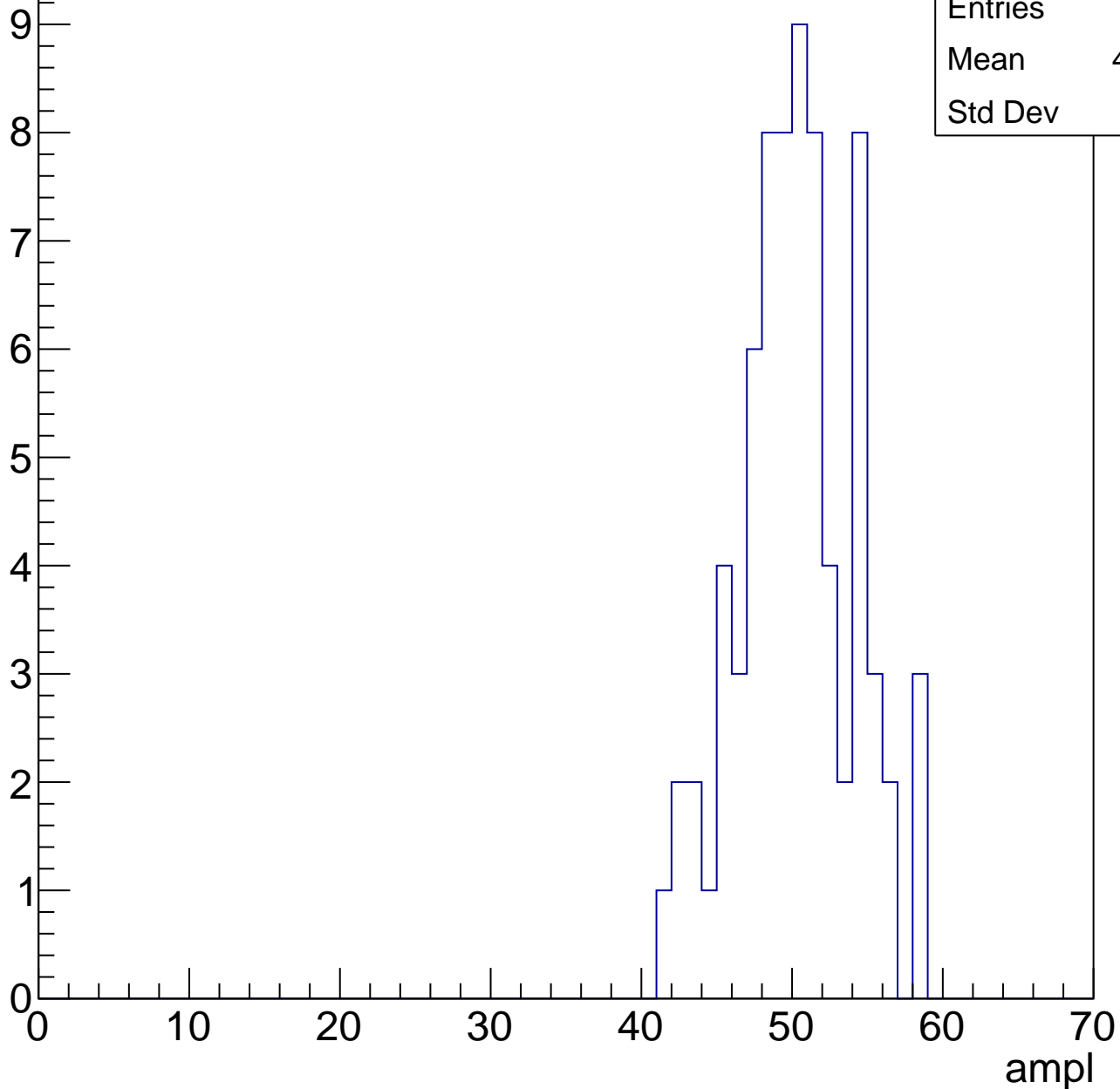
**Gaus Width: 3.7721**



# B1L101S, U11-ch92, adc3

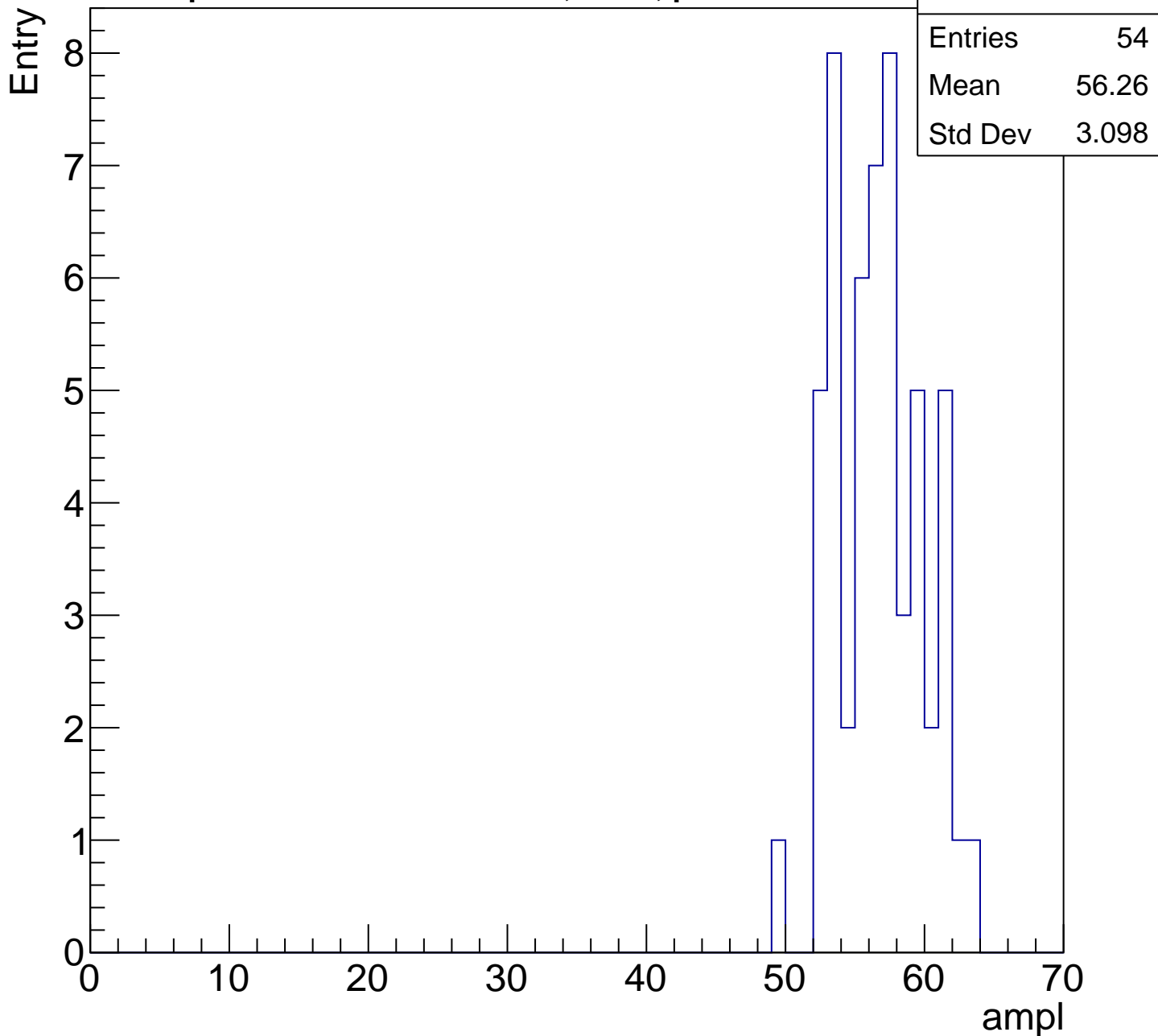
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U11-ch92, adc4

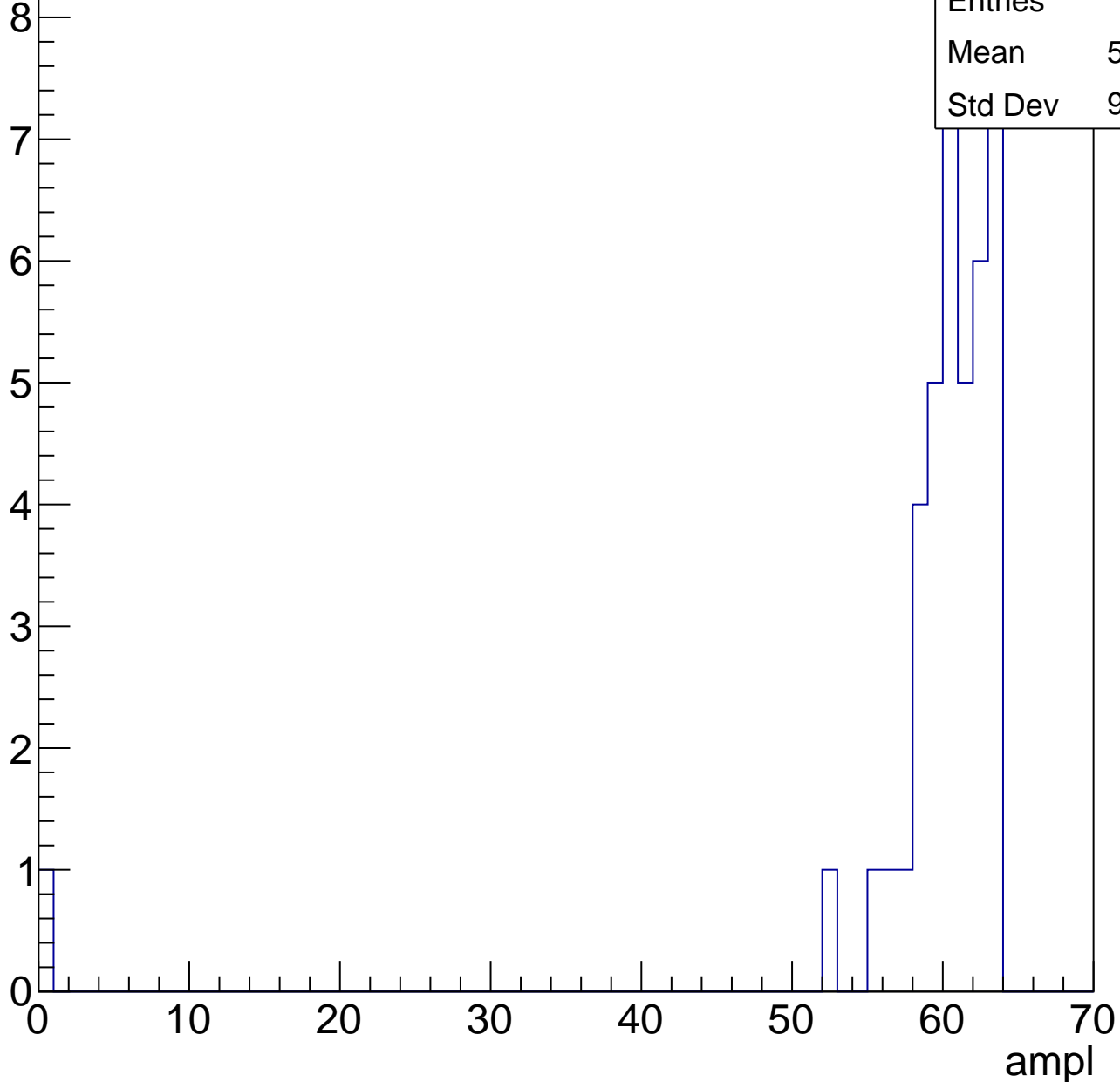
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U11-ch92, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

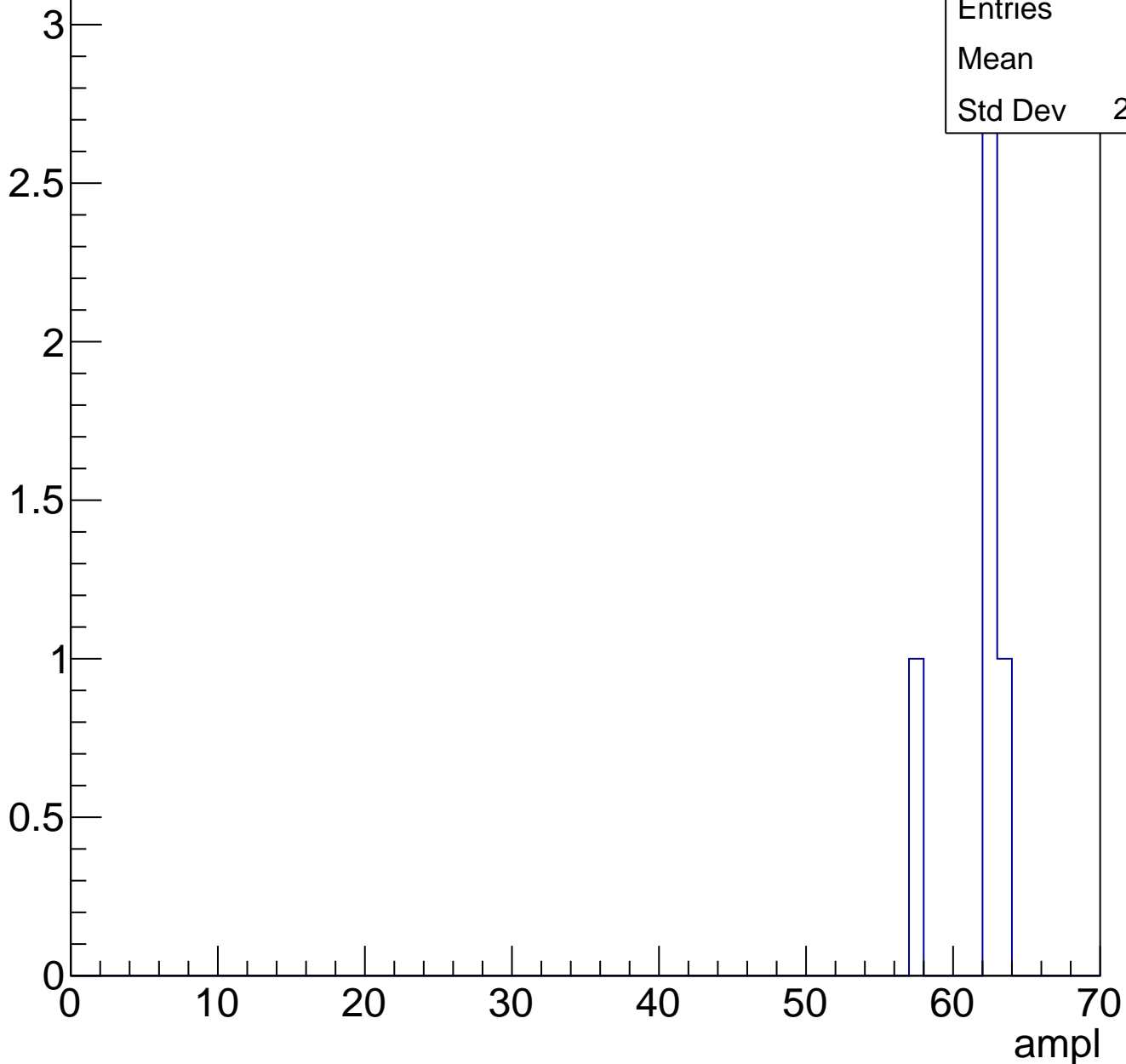
Entry



# B1L101S, U11-ch92, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch92, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U11-ch93, adc0

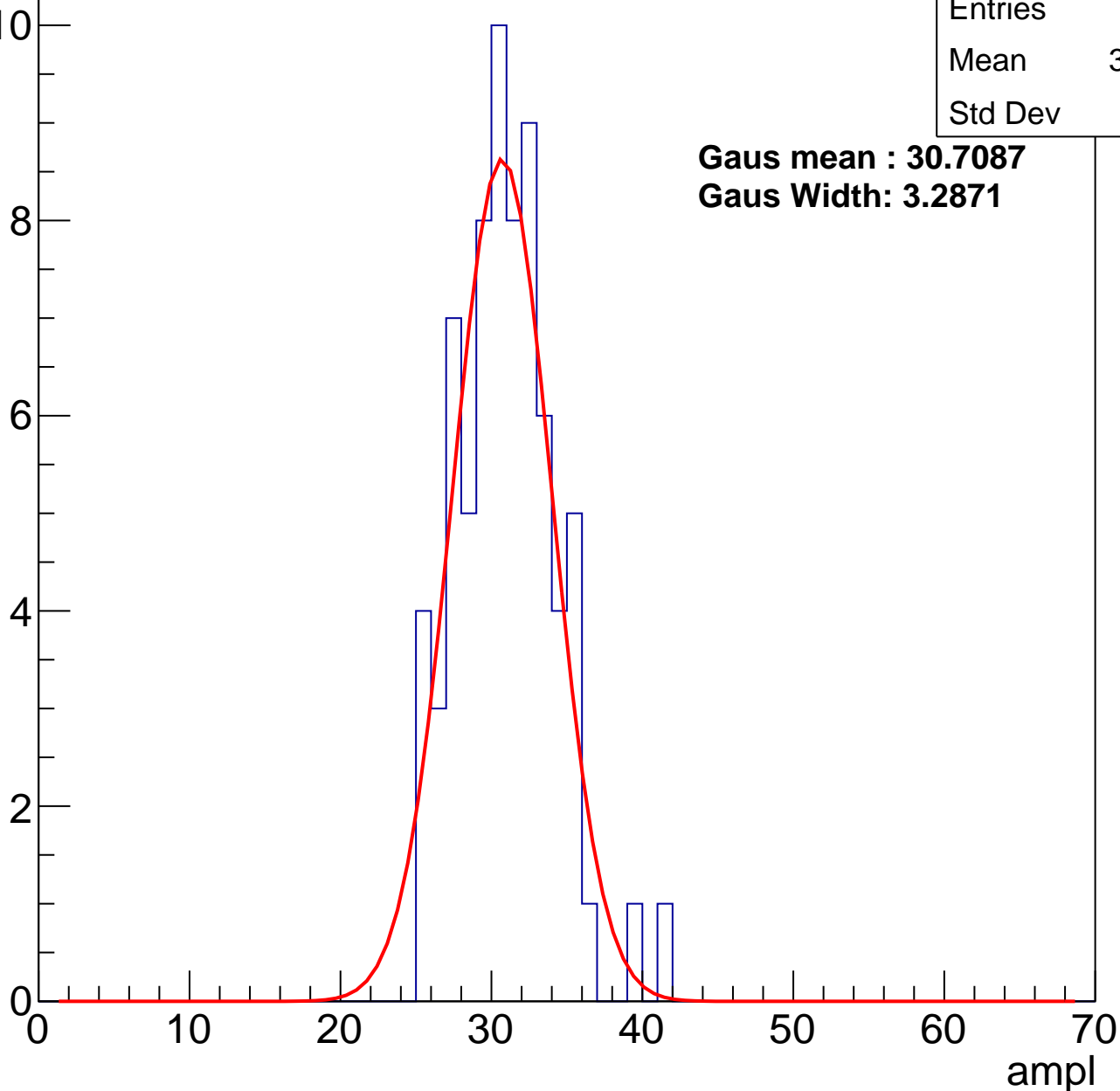
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	30.56
Std Dev	3.21

**Gaus mean : 30.7087**

**Gaus Width: 3.2871**



# B1L101S, U11-ch93, adc1

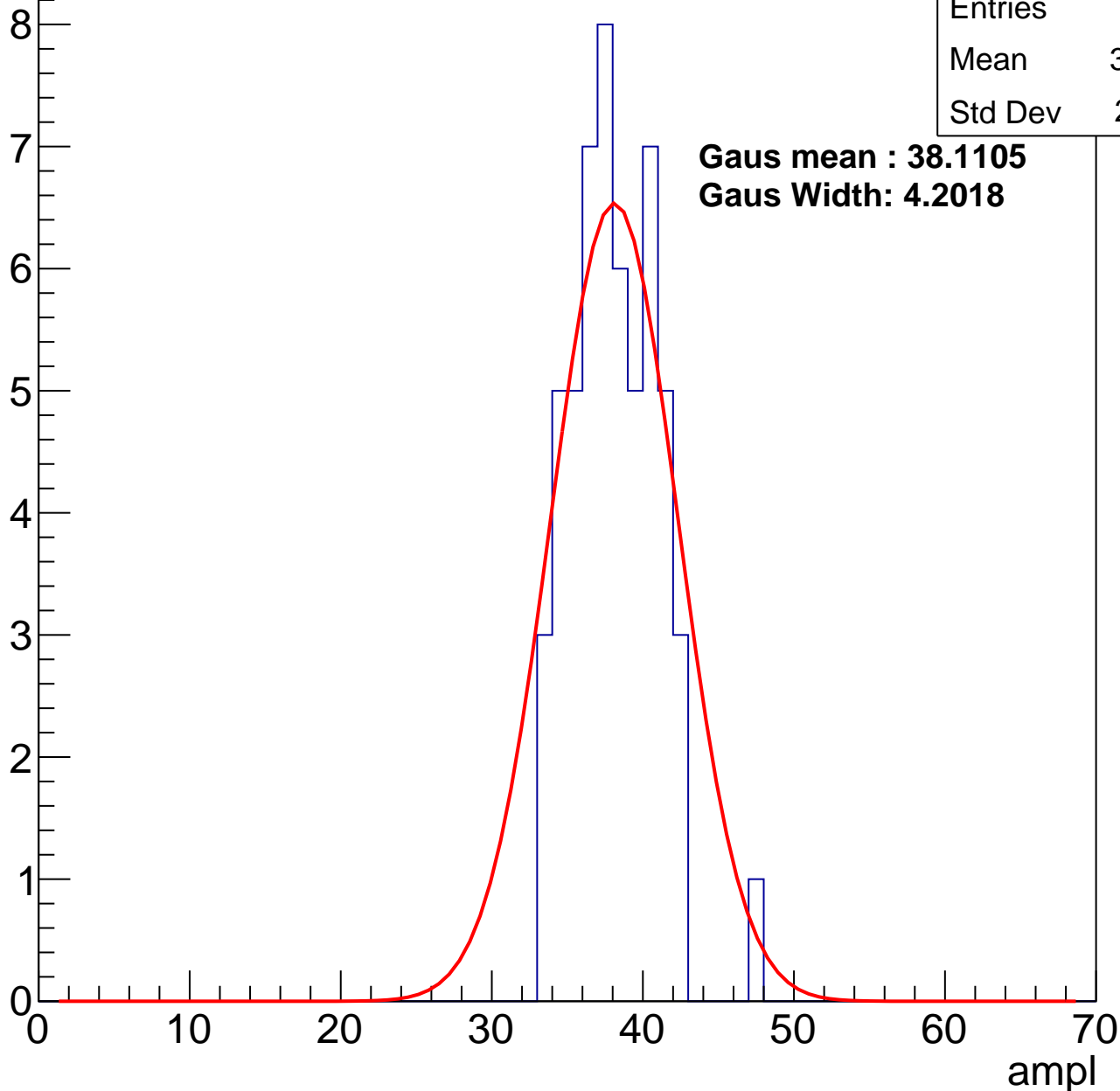
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	37.69
Std Dev	2.821

**Gaus mean : 38.1105**

**Gaus Width: 4.2018**



# B1L101S, U11-ch93, adc2

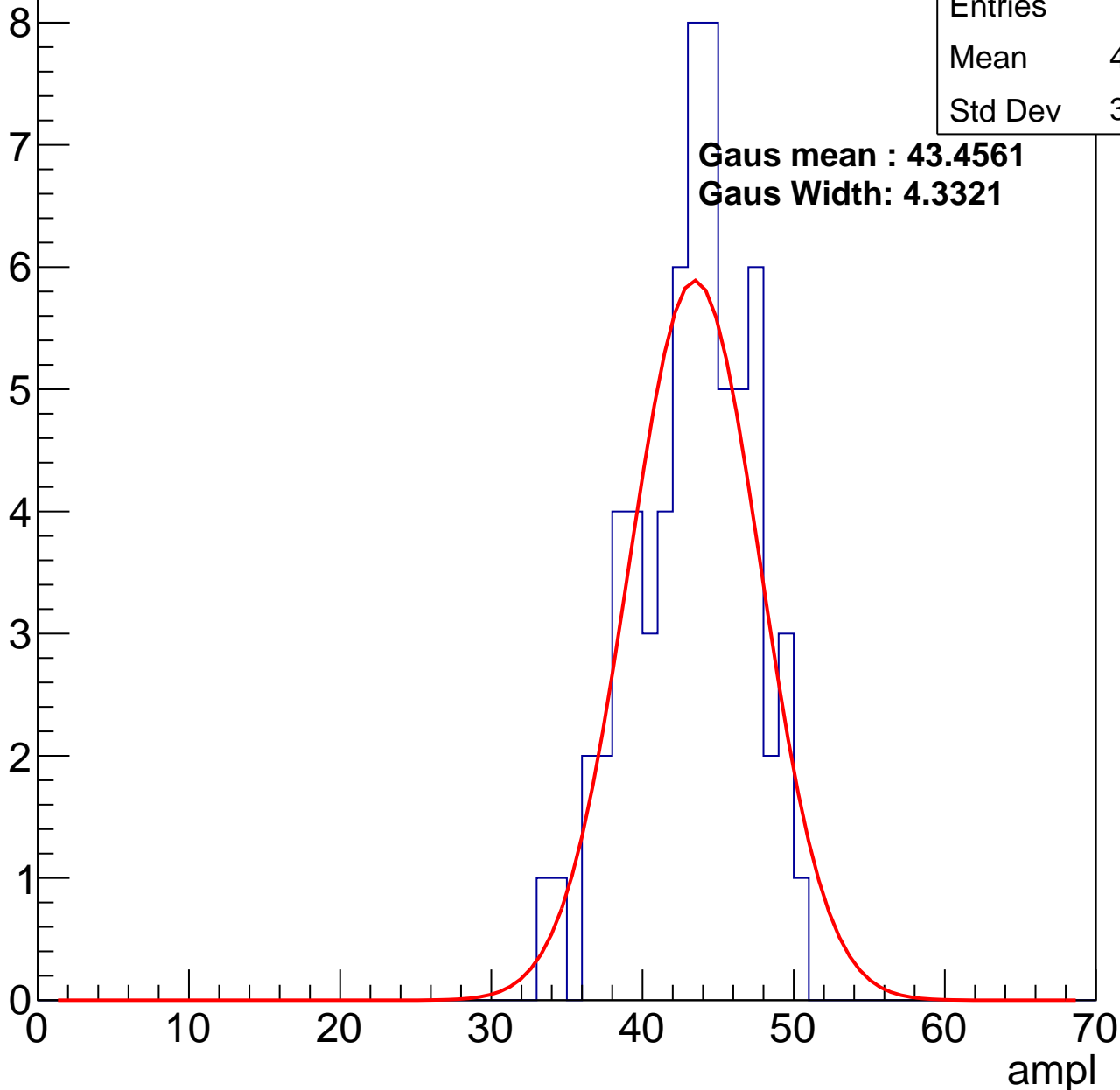
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	42.82
Std Dev	3.798

**Gaus mean : 43.4561**

**Gaus Width: 4.3321**

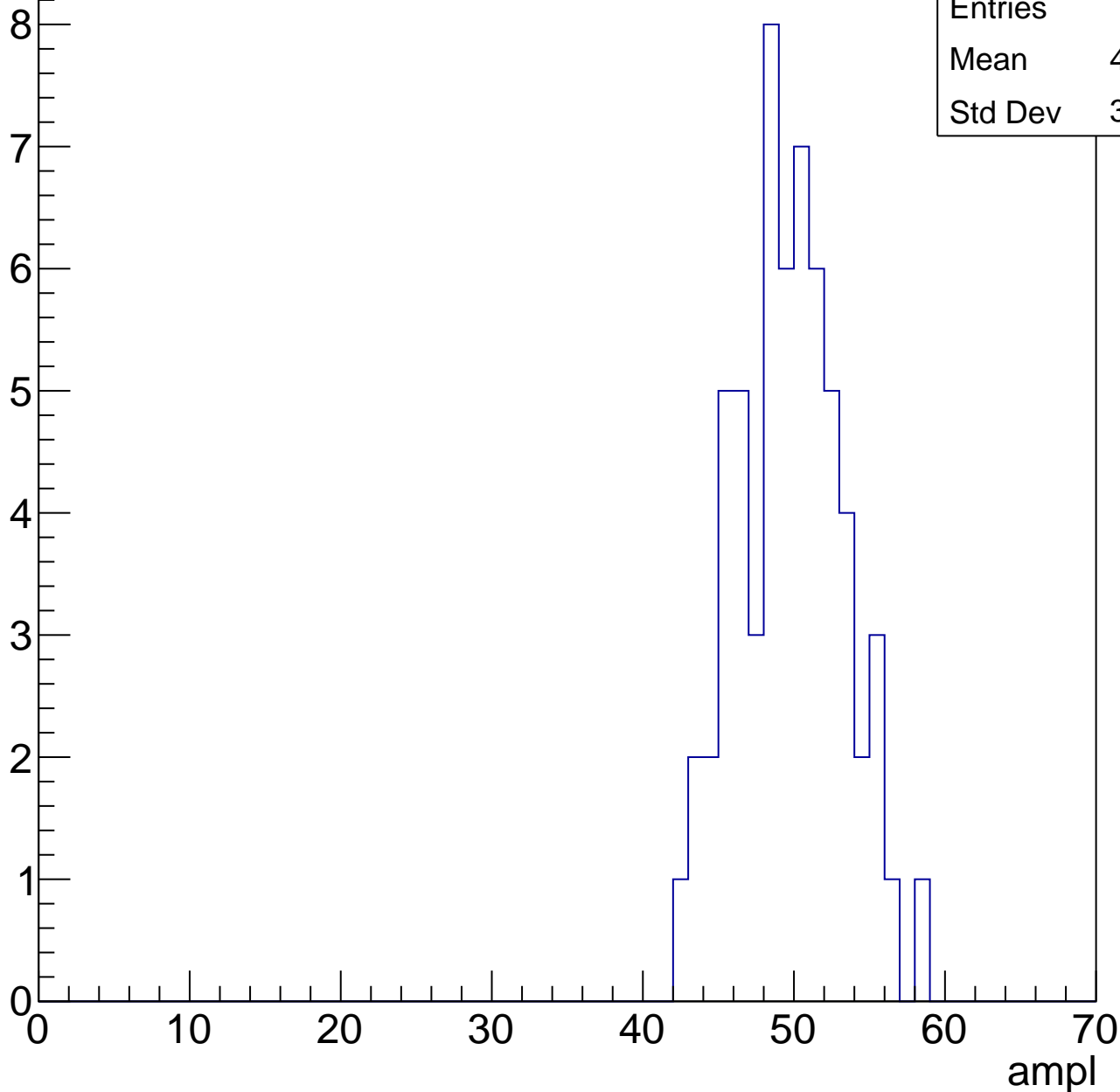


# B1L101S, U11-ch93, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	49.26
Std Dev	3.483

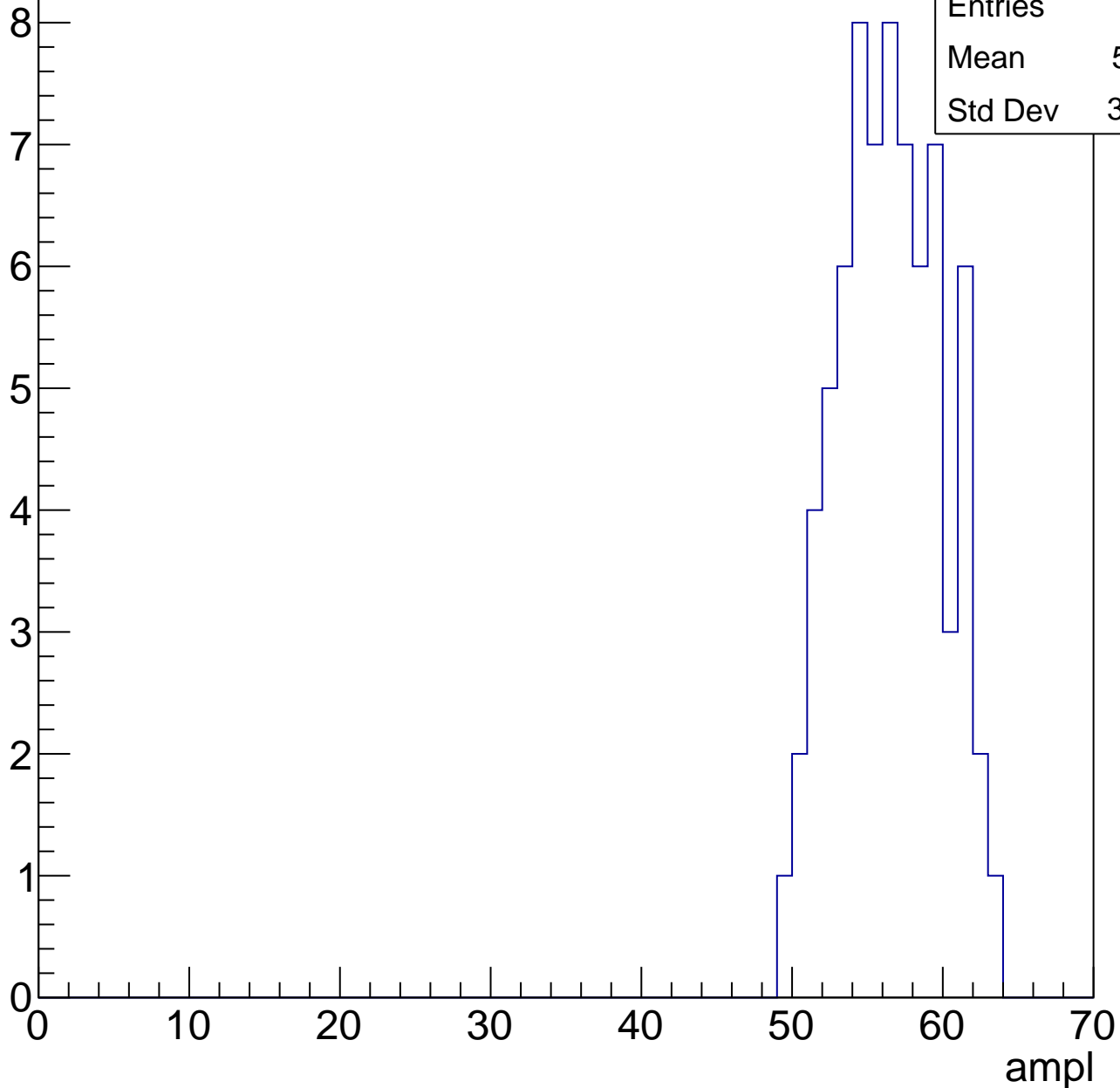


# B1L101S, U11-ch93, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

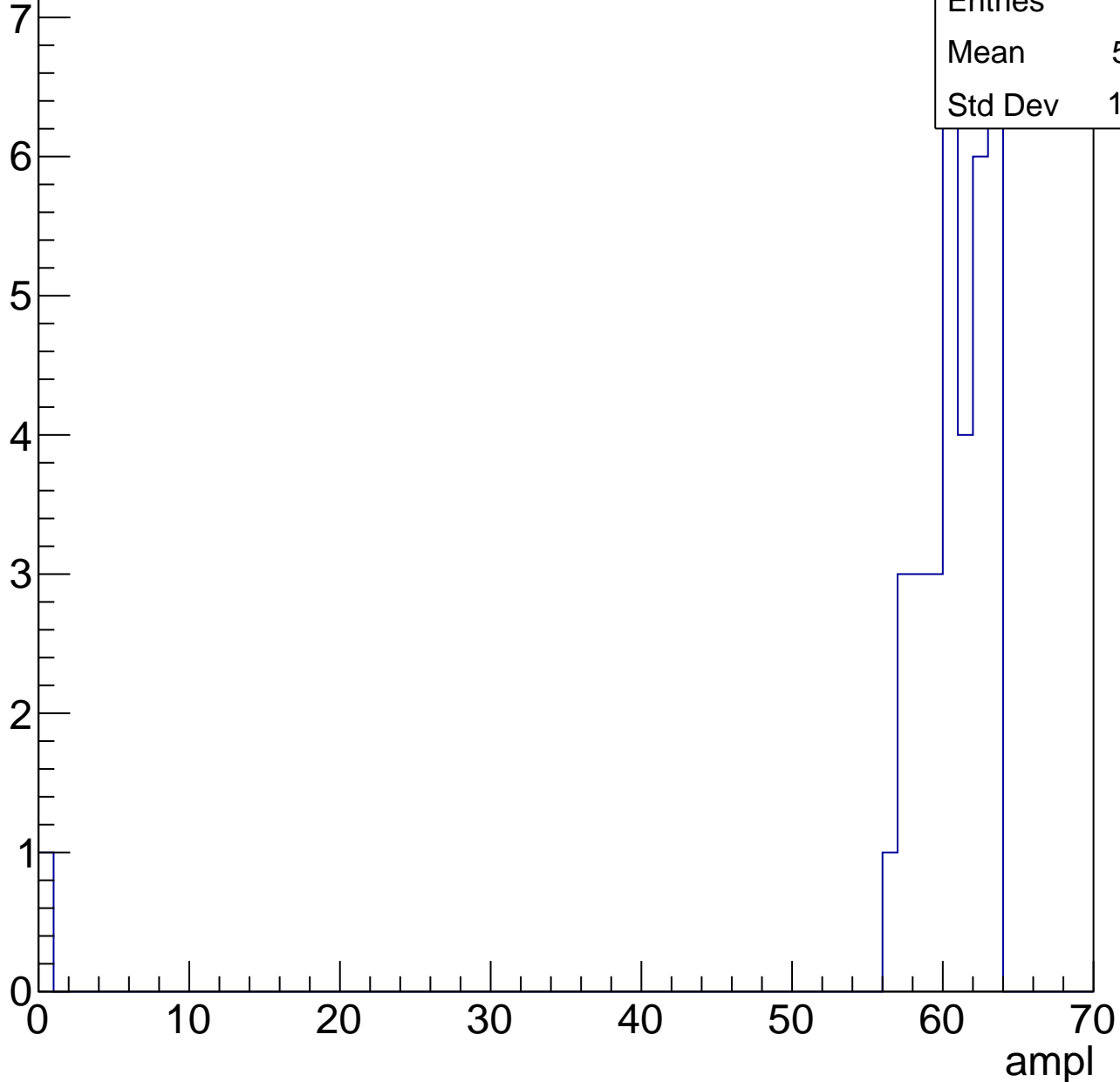
Entries	73
Mean	56.01
Std Dev	3.325



# B1L101S, U11-ch93, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	35
Mean	58.71
Std Dev	10.27

# B1L101S, U11-ch93, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch93, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U11-ch94, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	83
Mean	28.58
Std Dev	4.785

**Gaus mean : 29.5913**

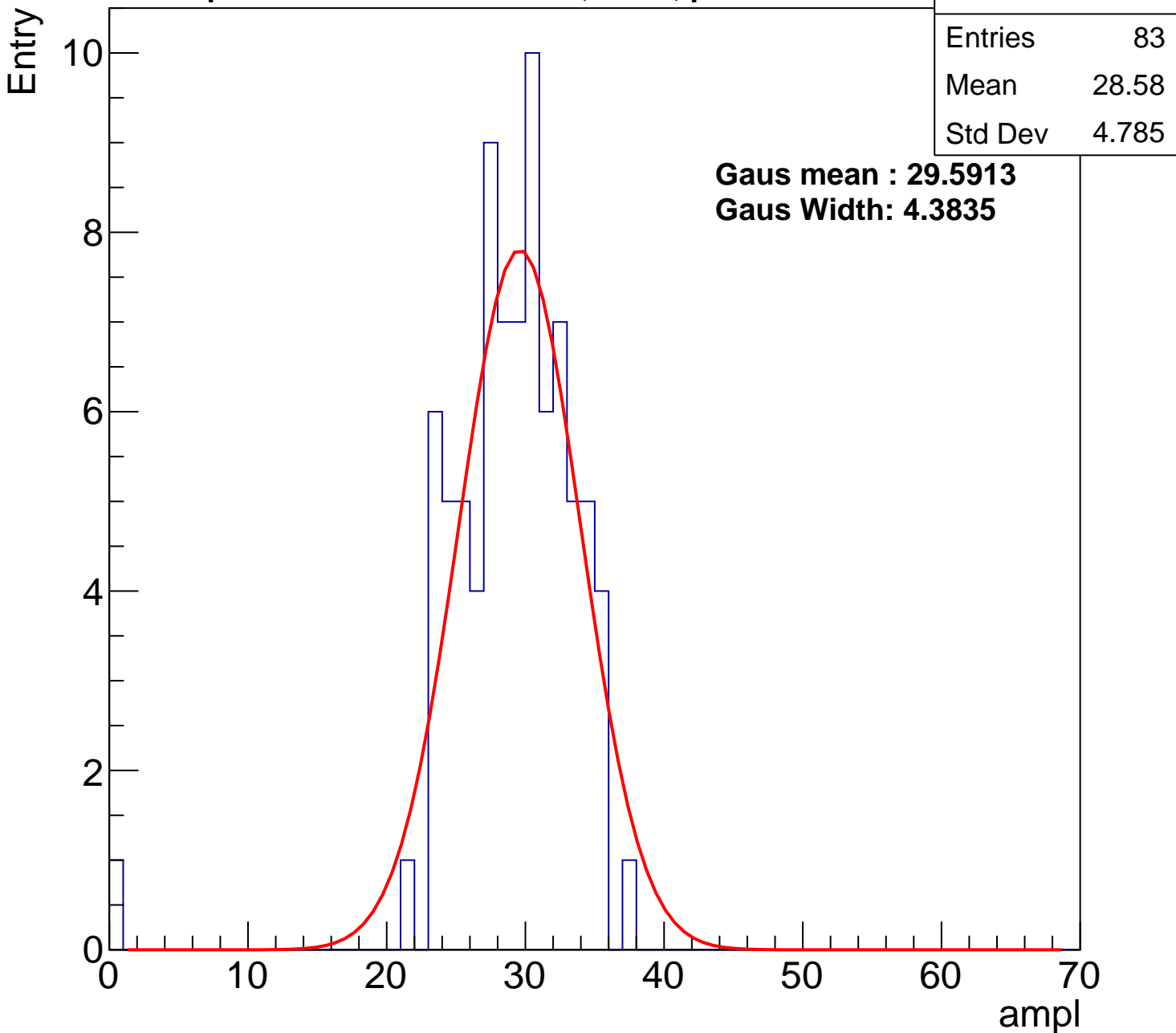
**Gaus Width: 4.3835**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L101S, U11-ch94, adc1

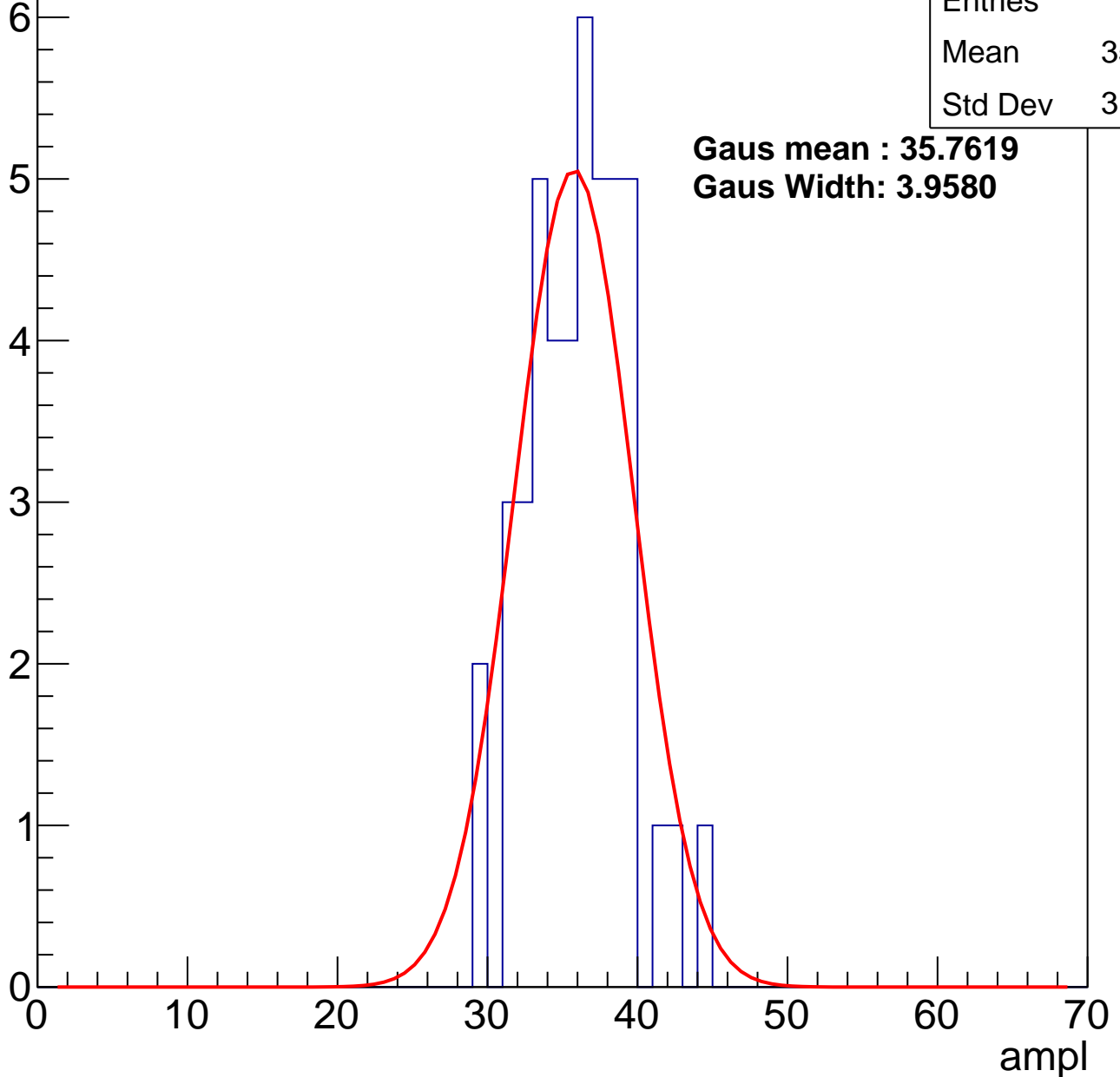
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	45
Mean	35.58
Std Dev	3.242

**Gaus mean : 35.7619**

**Gaus Width: 3.9580**



# B1L101S, U11-ch94, adc2

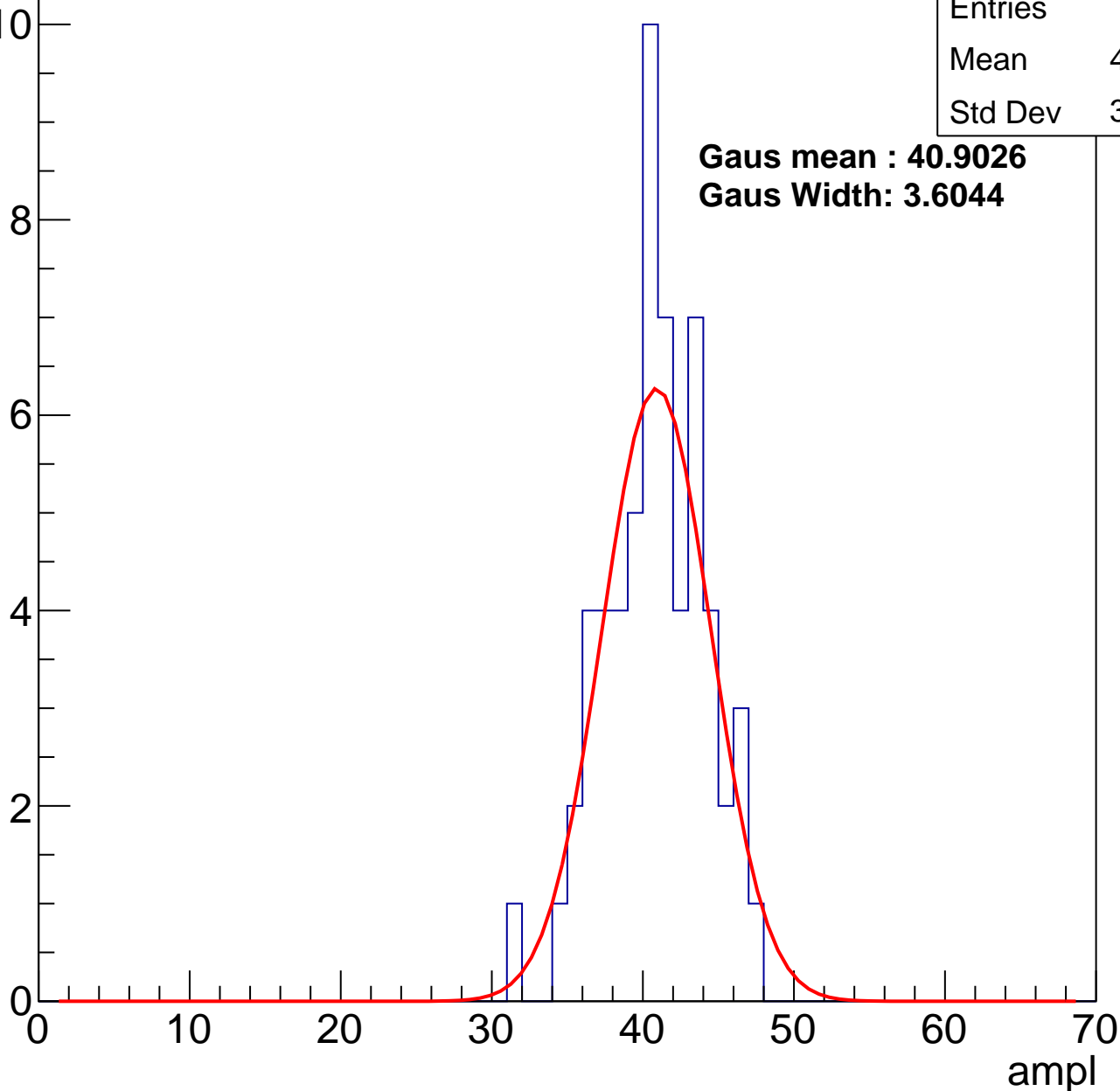
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	40.36
Std Dev	3.287

**Gaus mean : 40.9026**

**Gaus Width: 3.6044**

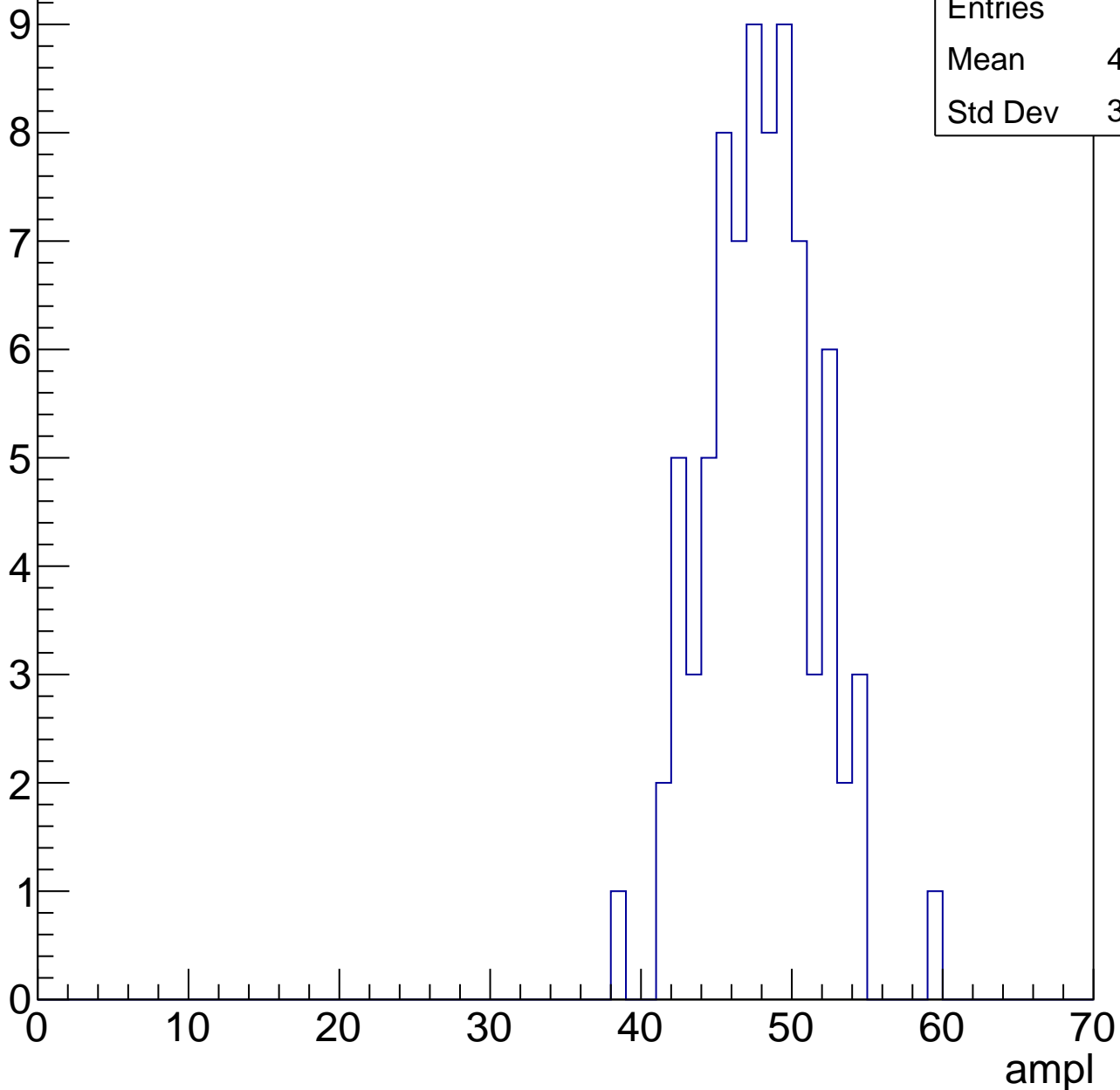


# B1L101S, U11-ch94, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	79
Mean	47.48
Std Dev	3.663

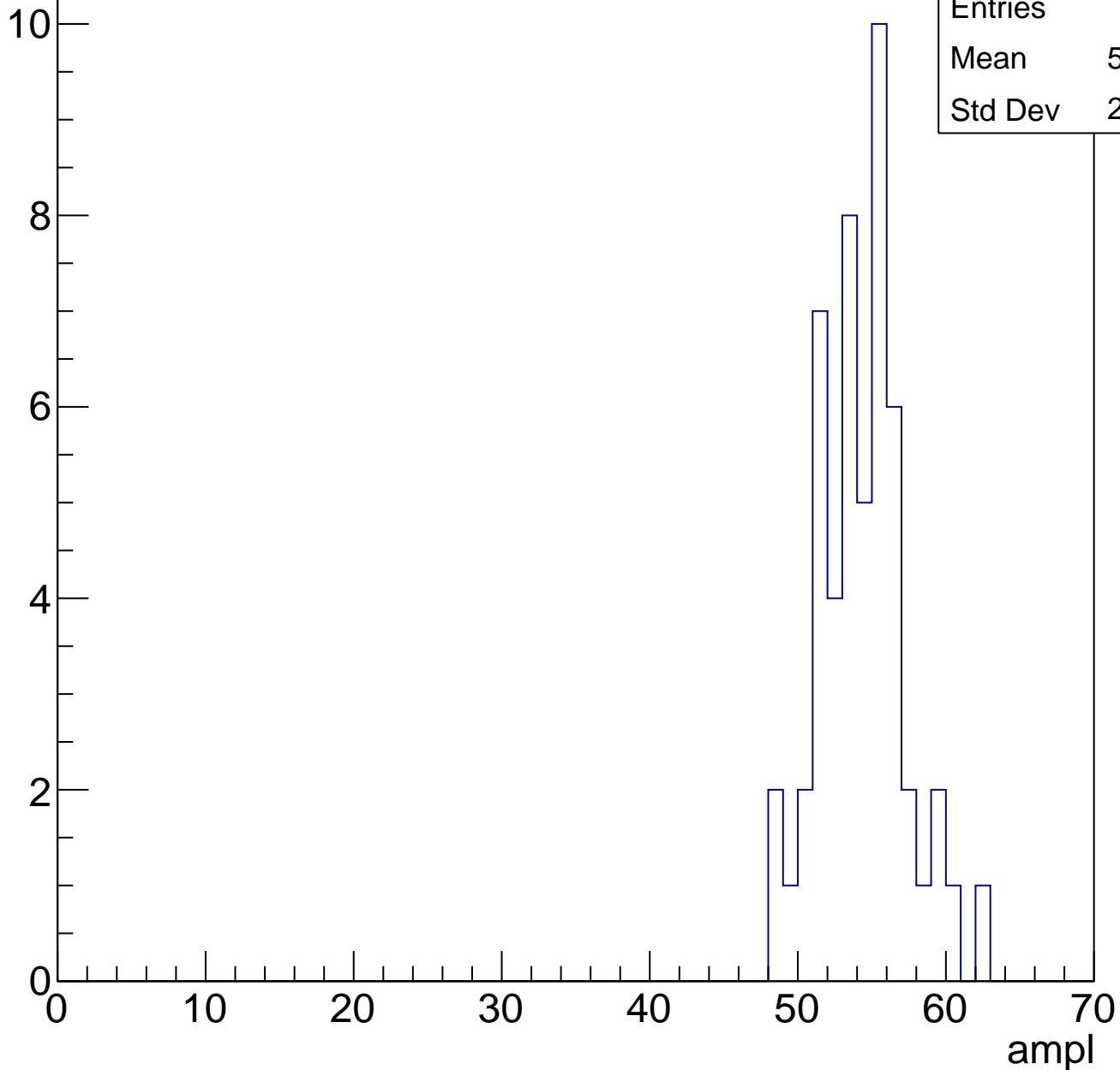


# B1L101S, U11-ch94, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	52
Mean	53.88
Std Dev	2.887

Entry

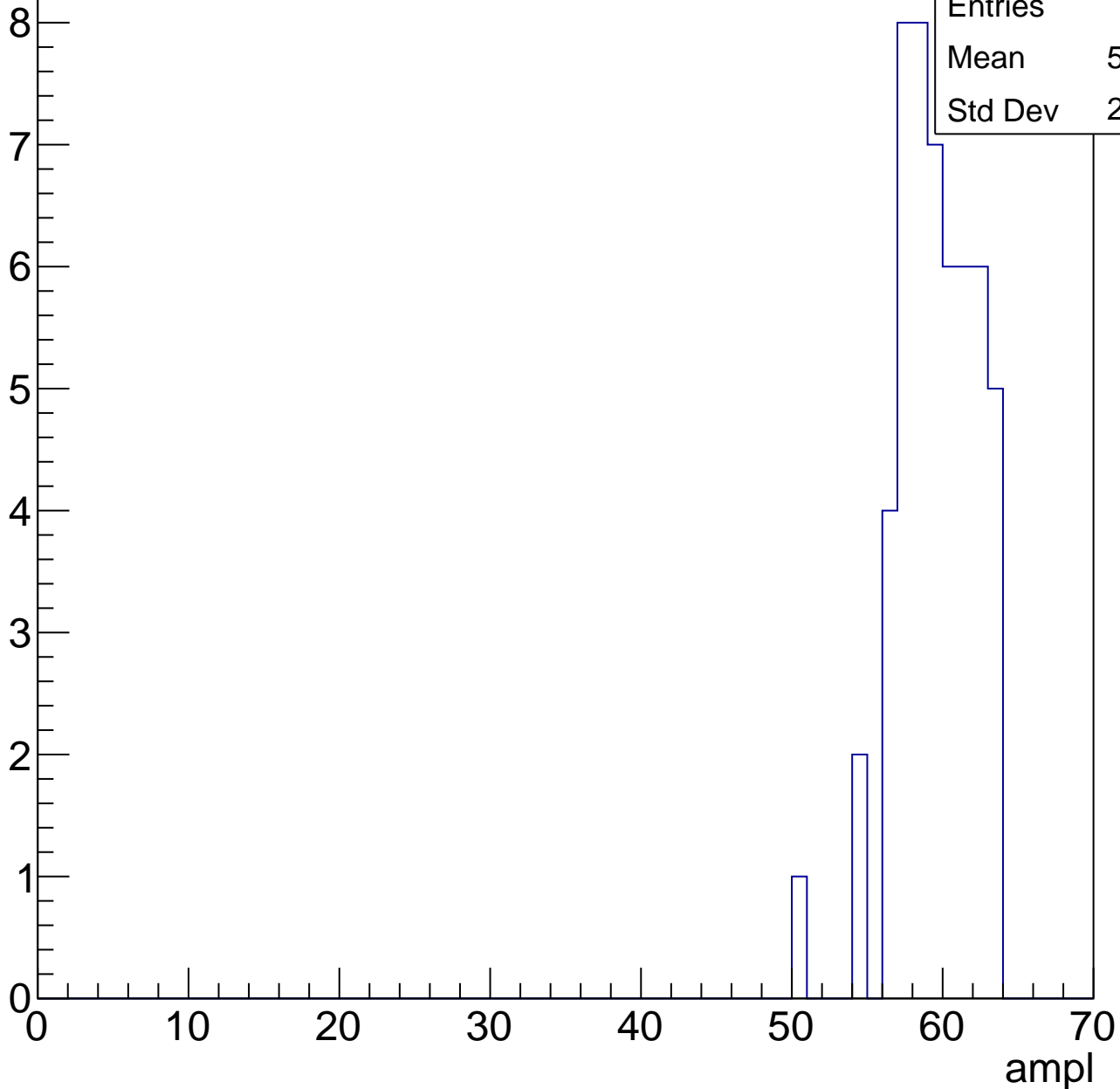


# B1L101S, U11-ch94, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	59.02
Std Dev	2.646

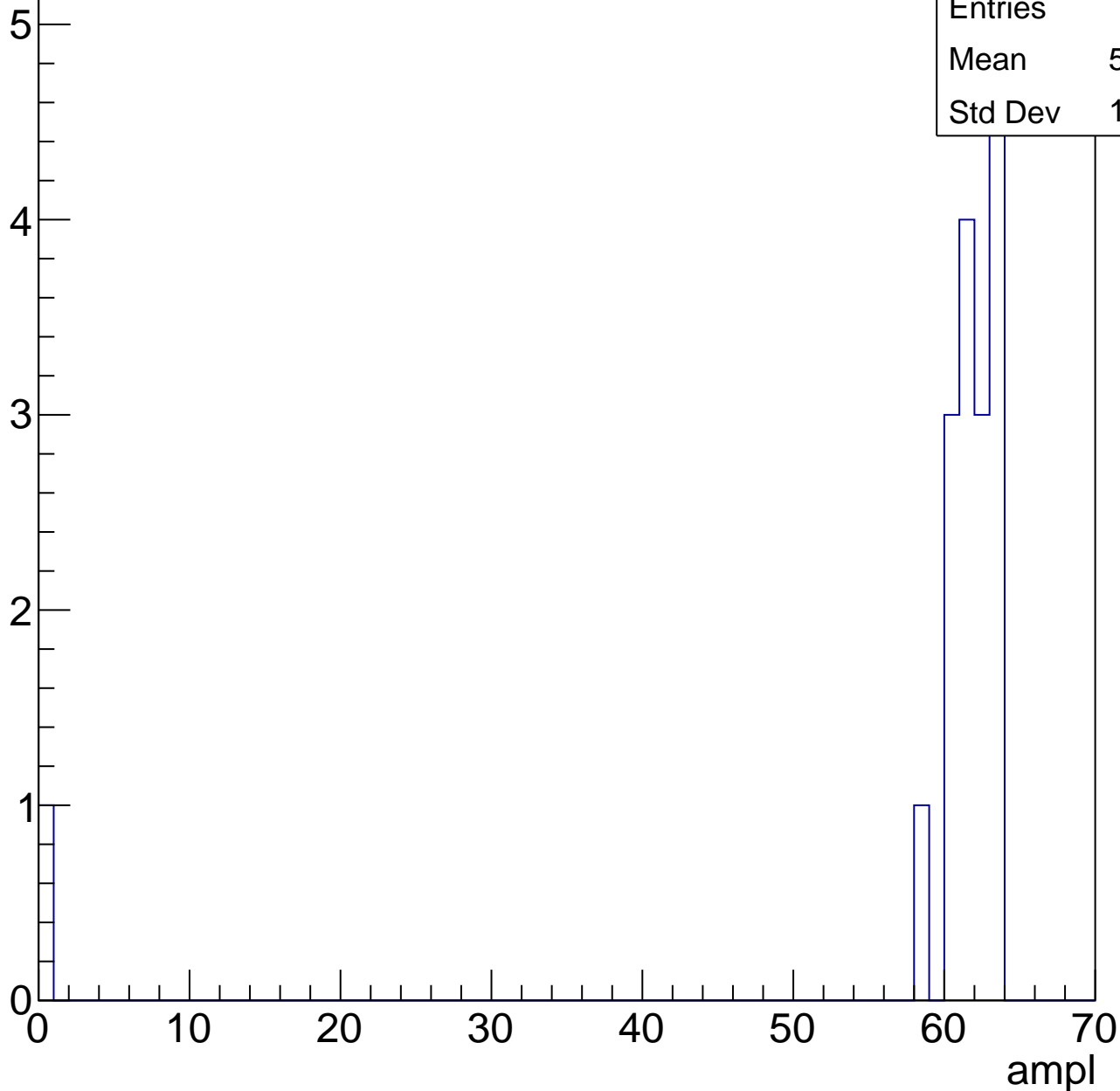


# B1L101S, U11-ch94, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	17
Mean	57.82
Std Dev	14.52





# B1L101S, U11-ch94, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U11-ch95, adc0

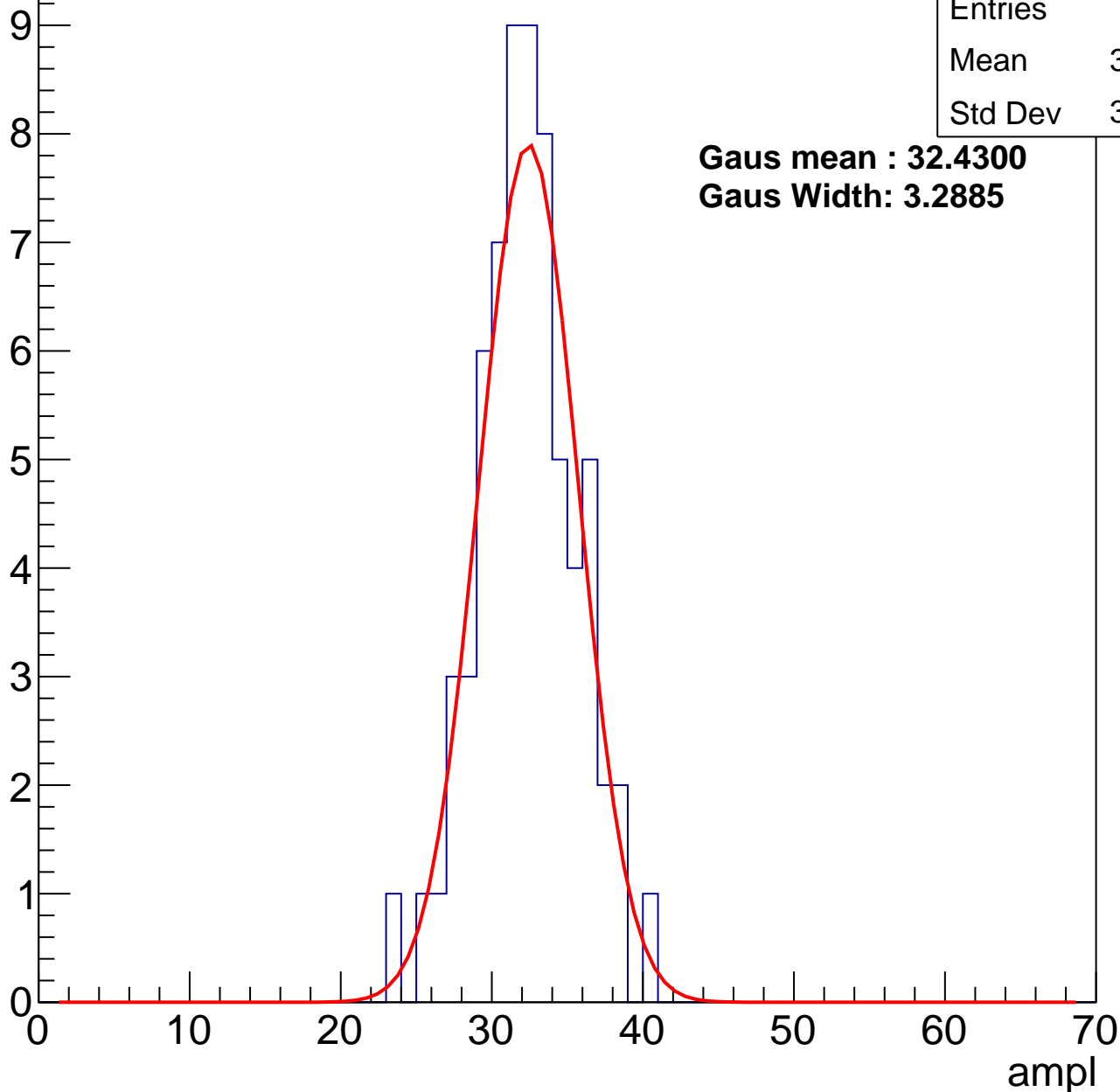
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	31.85
Std Dev	3.252

**Gaus mean : 32.4300**

**Gaus Width: 3.2885**



# B1L101S, U11-ch95, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	38.38
Std Dev	3.3

7

6

5

4

3

2

1

0

**Gaus mean : 38.3411**

**Gaus Width: 3.2711**

0

10

20

30

40

50

60

70

ampl

# B1L101S, U11-ch95, adc2

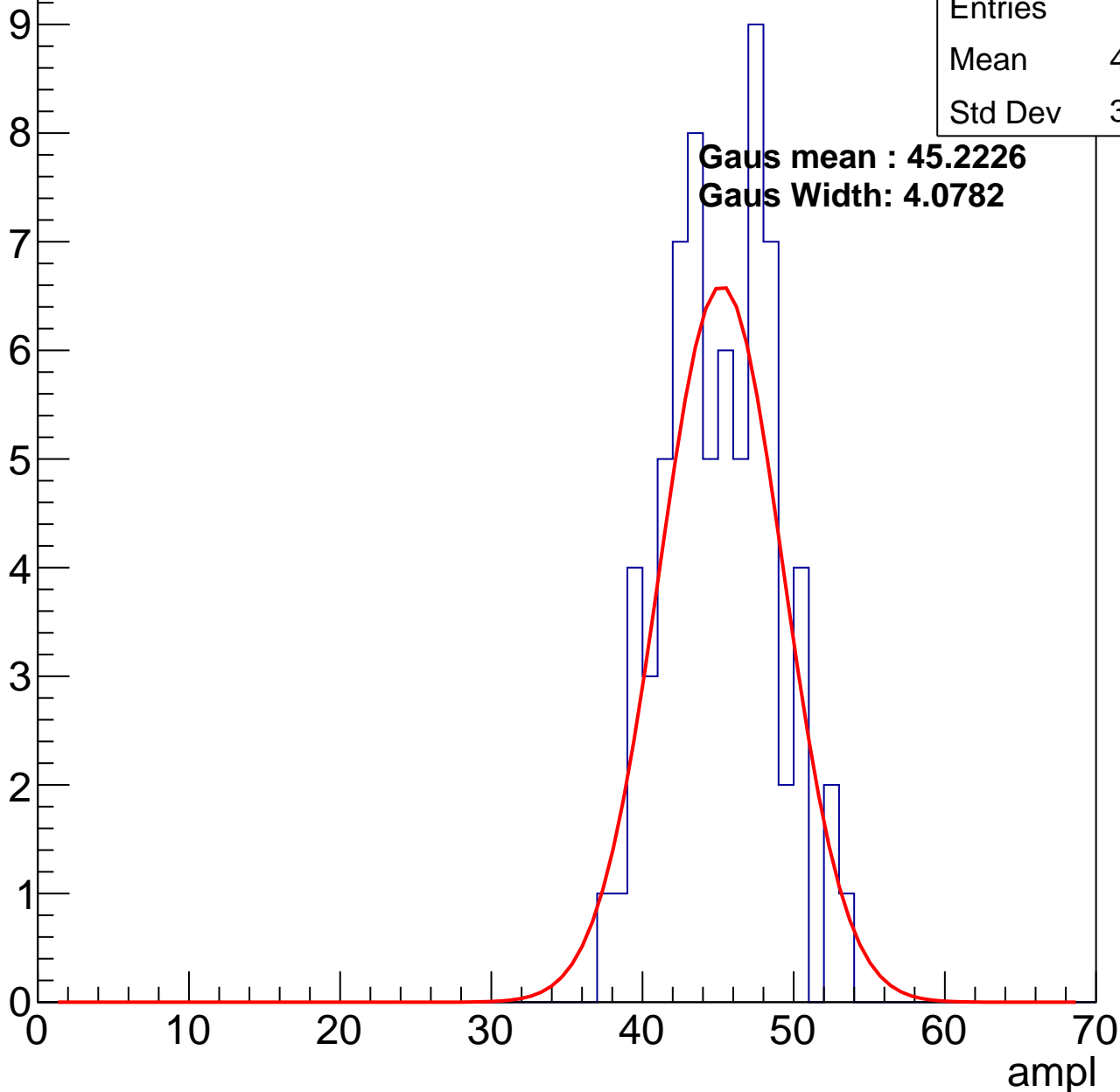
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	44.69
Std Dev	3.592

**Gaus mean : 45.2226**

**Gaus Width: 4.0782**

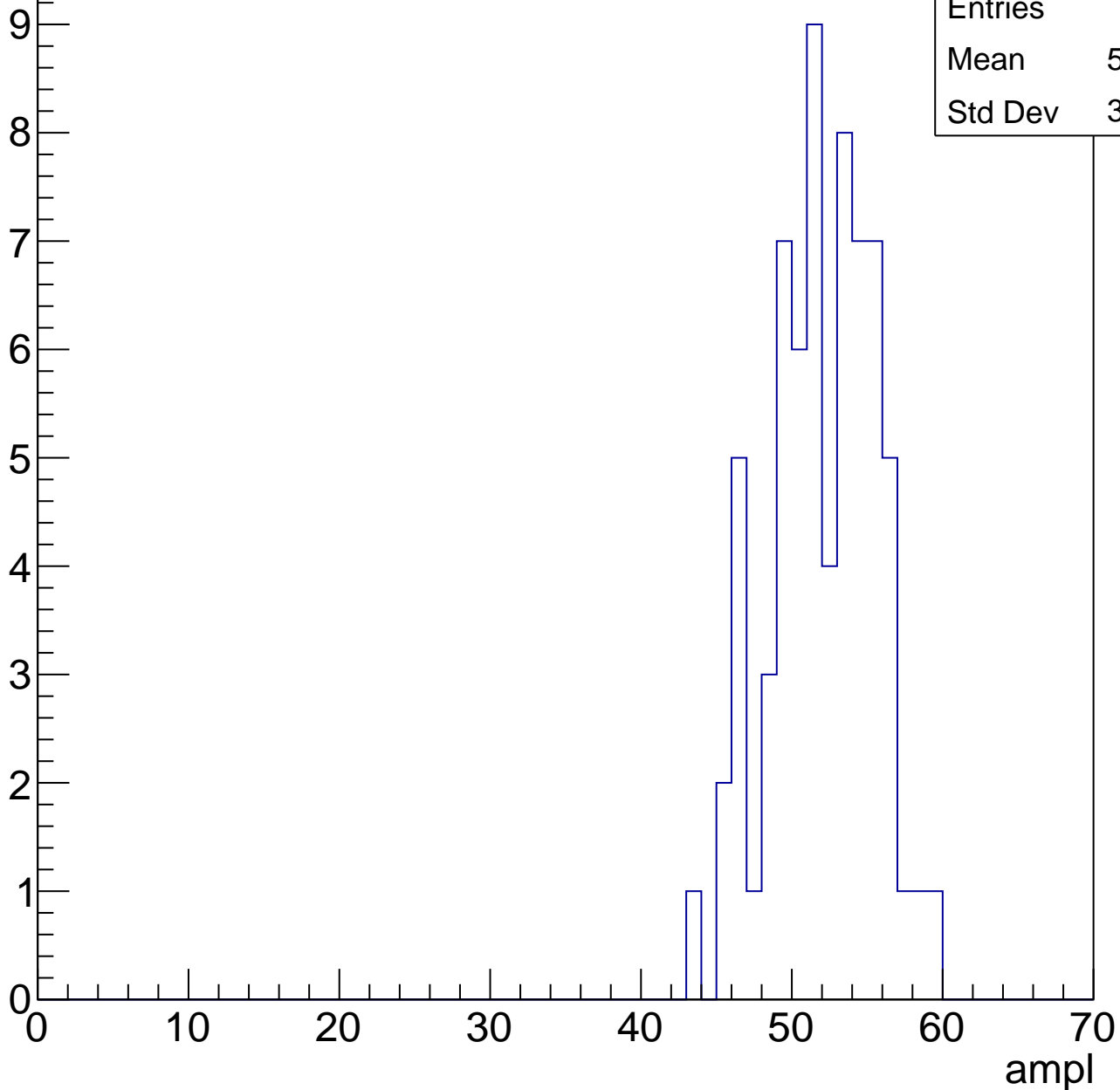


# B1L101S, U11-ch95, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

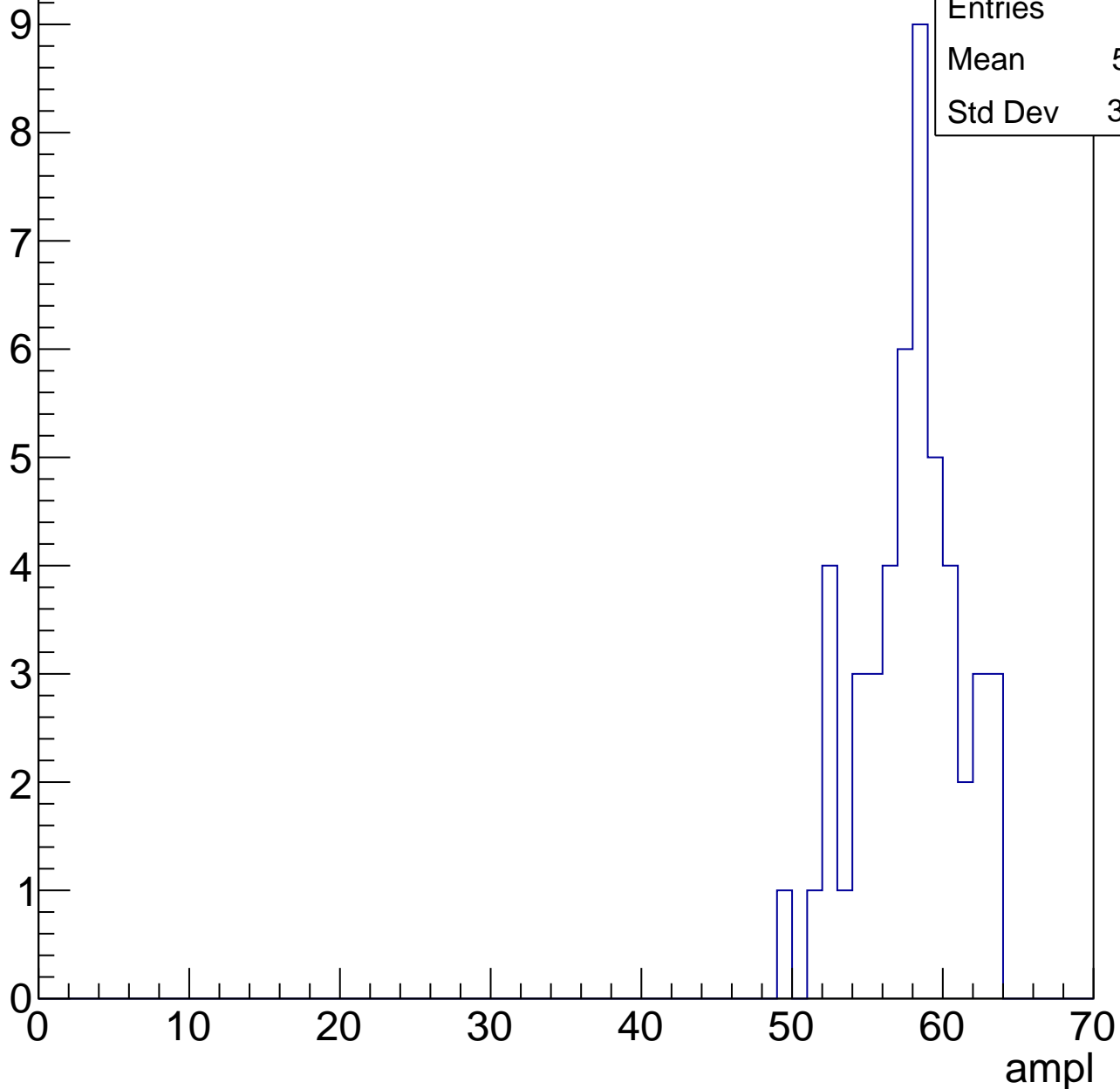
Entries	68
Mean	51.54
Std Dev	3.436



# B1L101S, U11-ch95, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

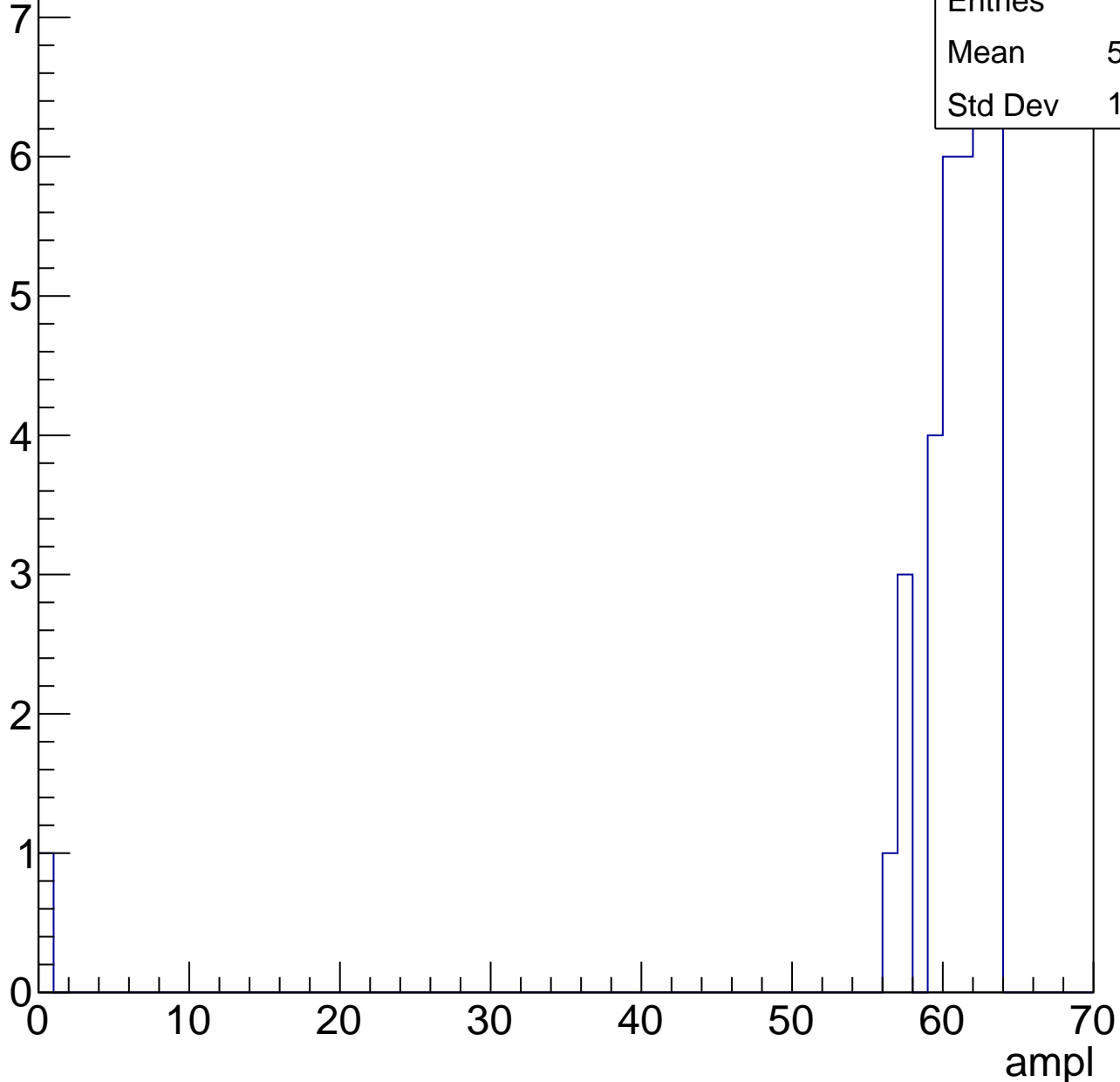


Entries	49
Mean	57.31
Std Dev	3.302

# B1L101S, U11-ch95, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

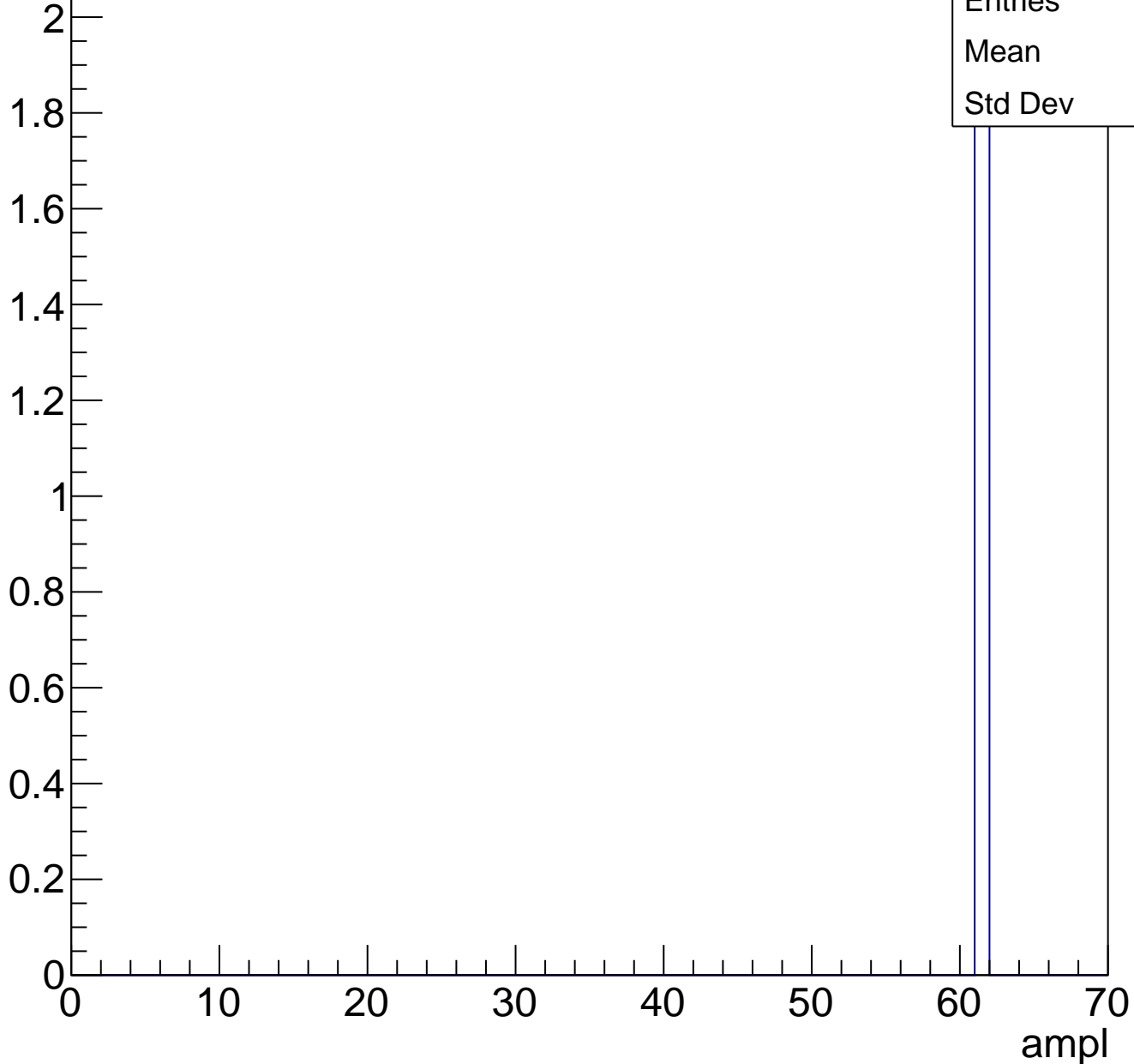
Entry



# B1L101S, U11-ch95, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch95, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U11-ch96, adc0

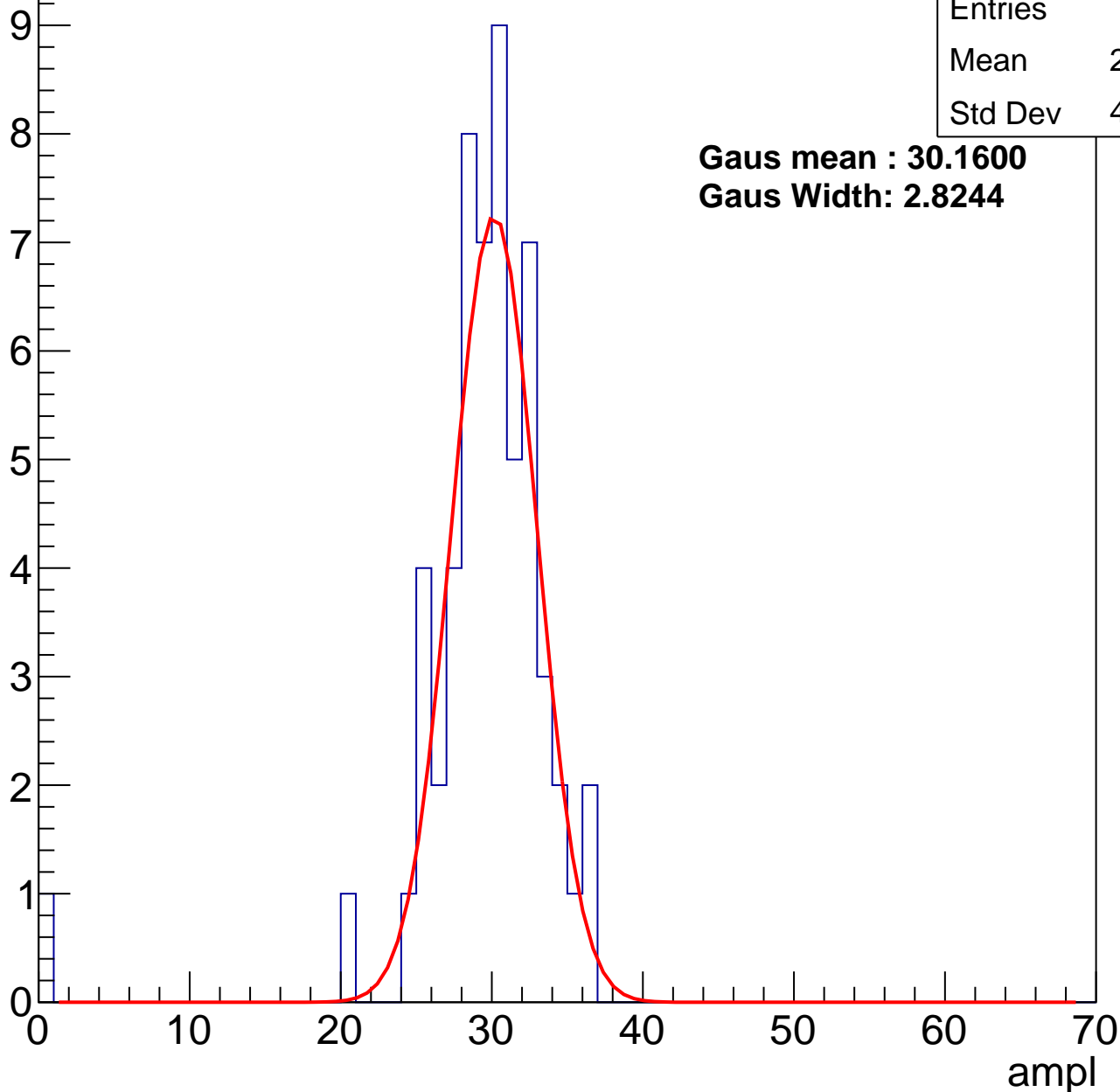
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	29.02
Std Dev	4.915

**Gaus mean : 30.1600**

**Gaus Width: 2.8244**



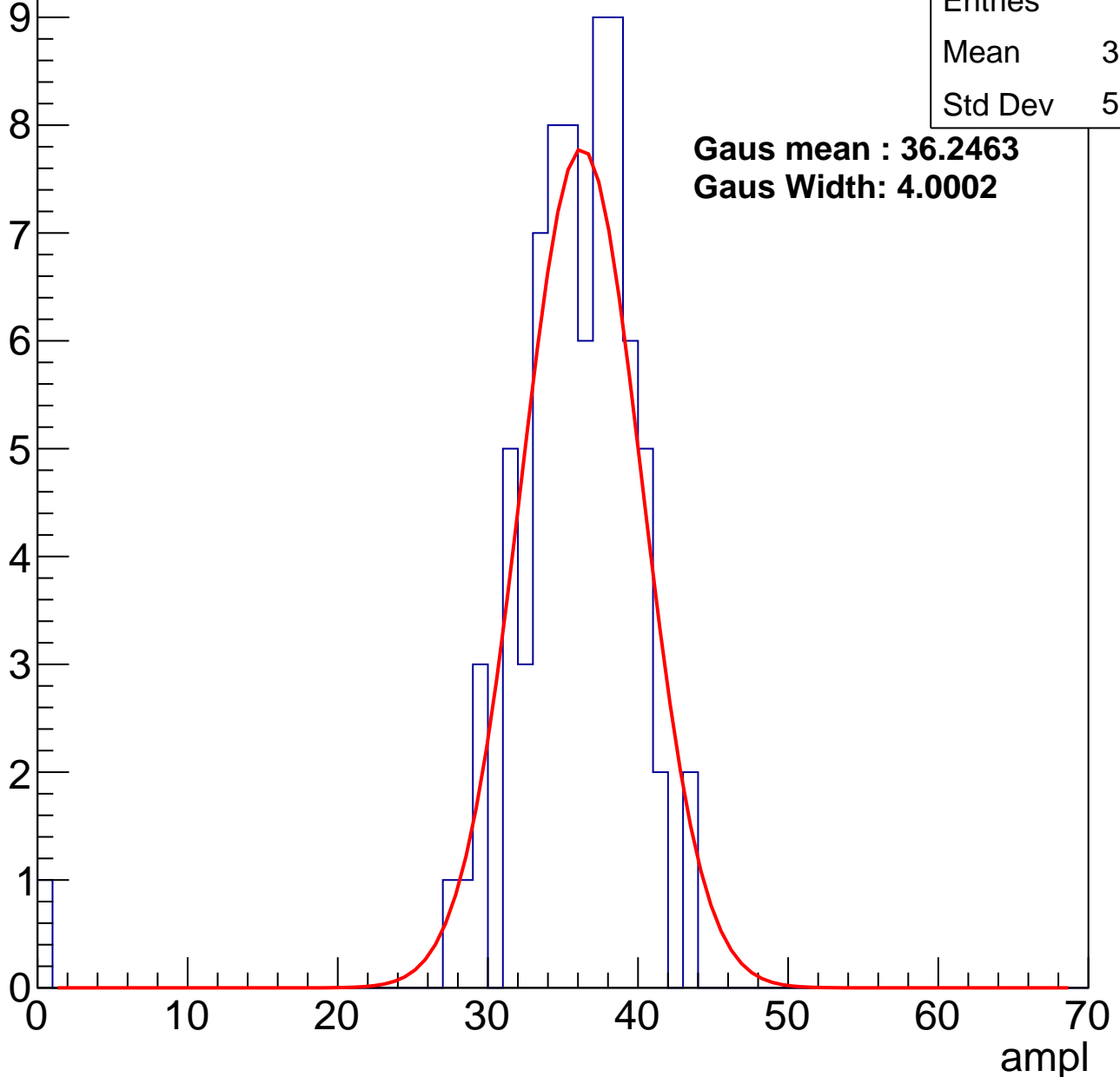
# B1L101S, U11-ch96, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	35.12
Std Dev	5.296

**Gaus mean : 36.2463**  
**Gaus Width: 4.0002**



# B1L101S, U11-ch96, adc2

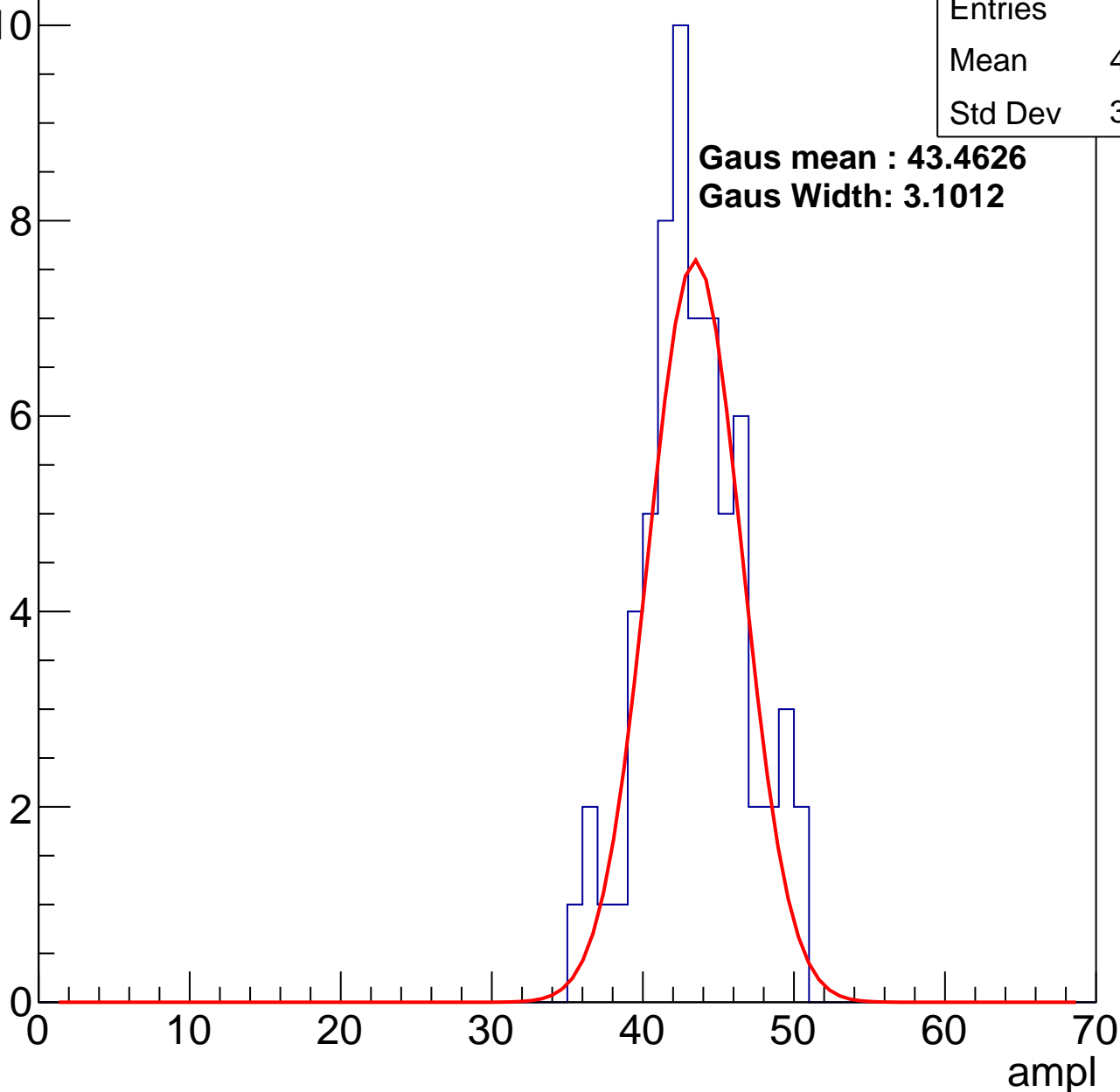
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	42.92
Std Dev	3.354

**Gaus mean : 43.4626**

**Gaus Width: 3.1012**

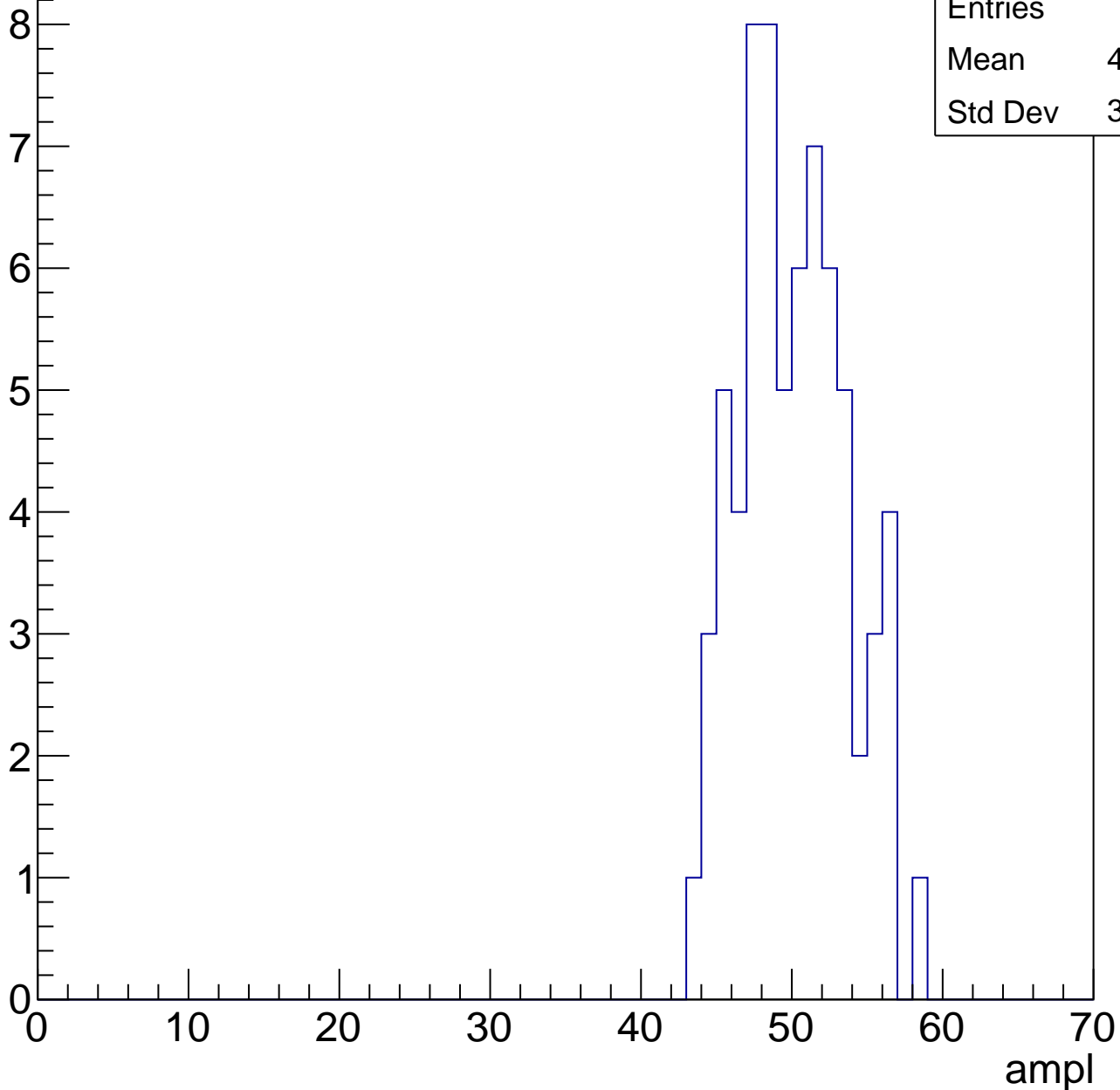


# B1L101S, U11-ch96, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	49.68
Std Dev	3.512

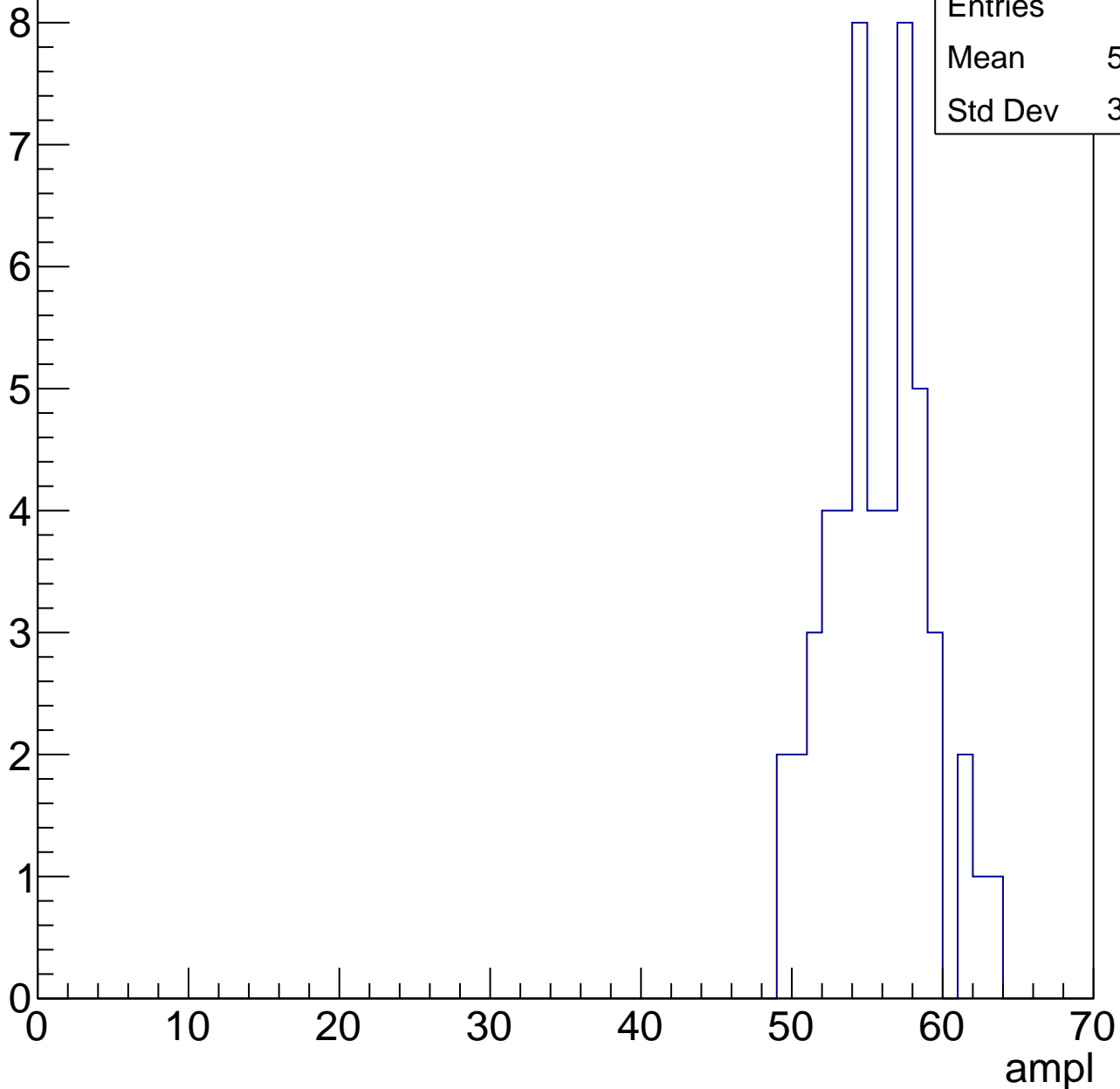


# B1L101S, U11-ch96, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	55.24
Std Dev	3.257

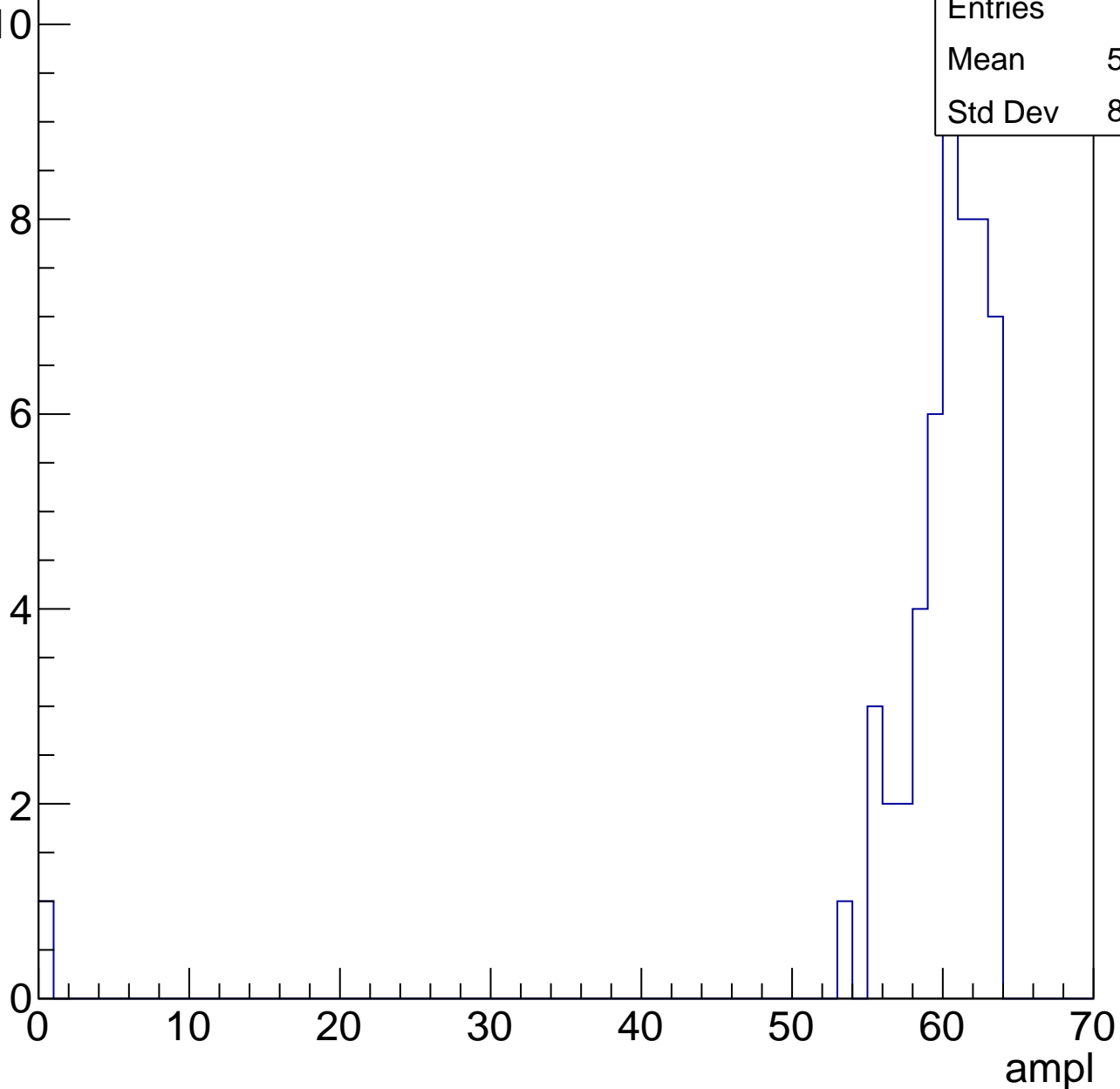


# B1L101S, U11-ch96, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	58.75
Std Dev	8.568



# B1L101S, U11-ch96, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch96, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U11-ch97, adc0

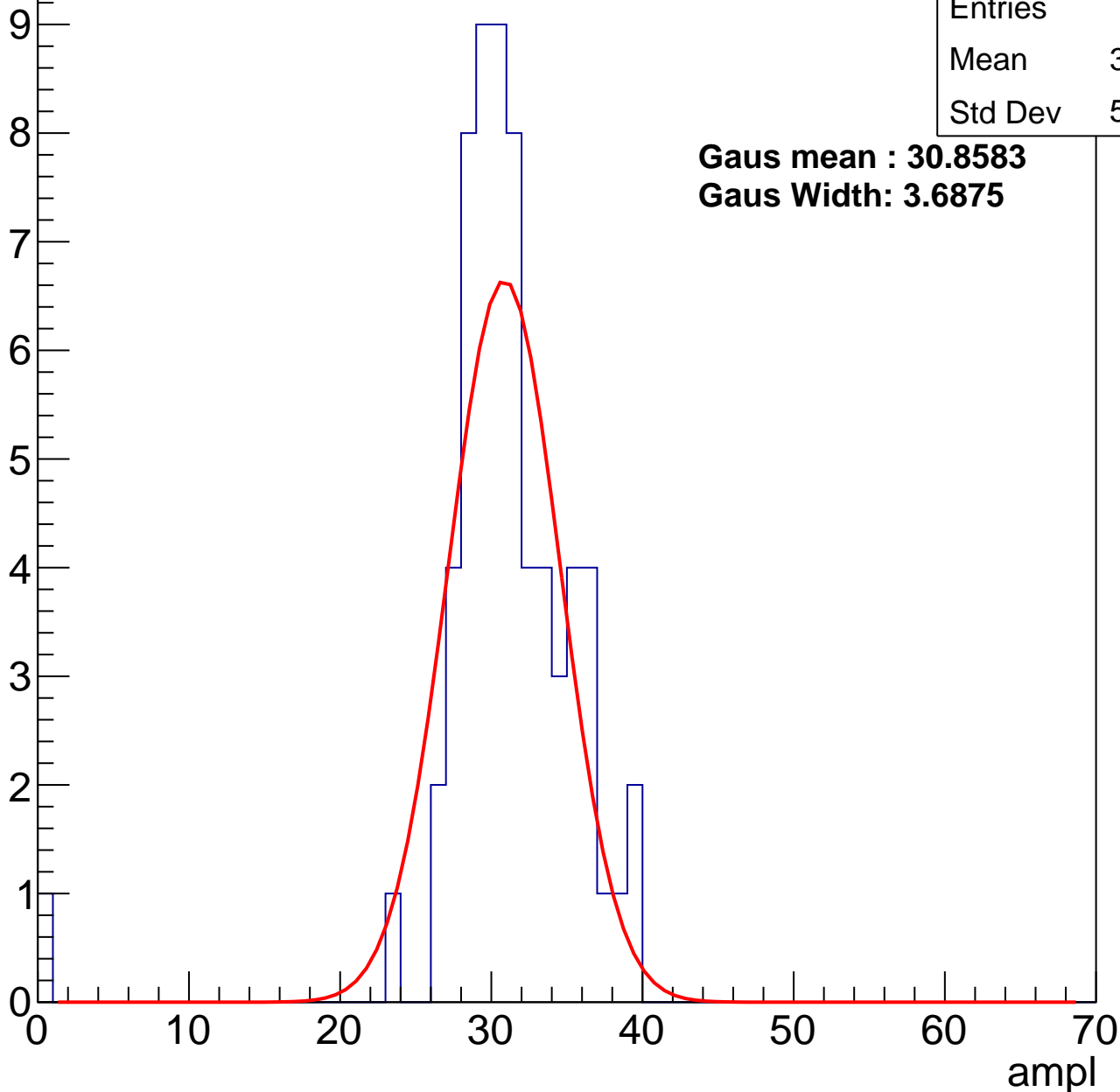
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	30.54
Std Dev	5.063

**Gaus mean : 30.8583**

**Gaus Width: 3.6875**



# B1L101S, U11-ch97, adc1

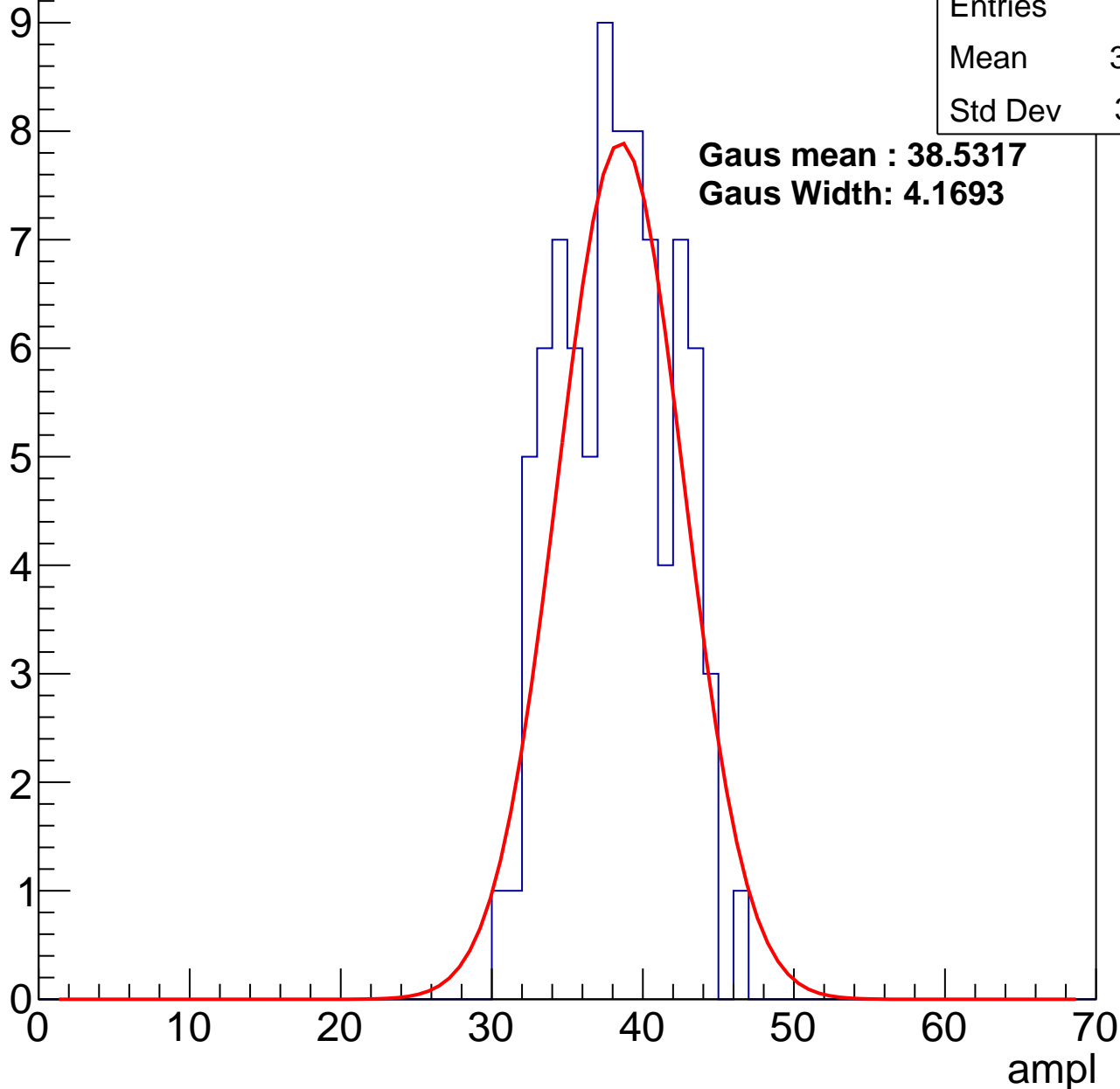
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	84
Mean	37.74
Std Dev	3.681

**Gaus mean : 38.5317**

**Gaus Width: 4.1693**



# B1L101S, U11-ch97, adc2

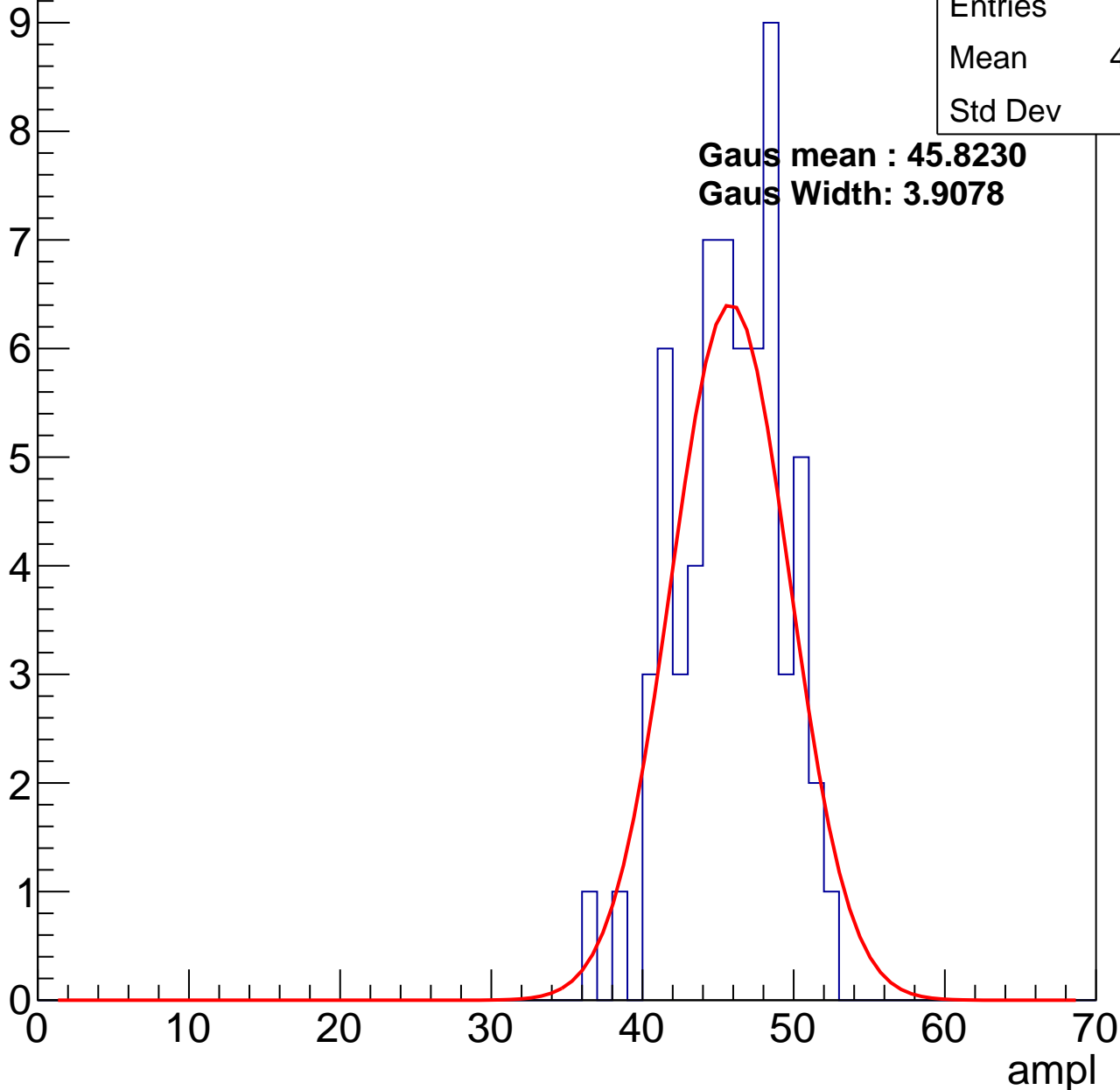
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	45.34
Std Dev	3.42

**Gaus mean : 45.8230**

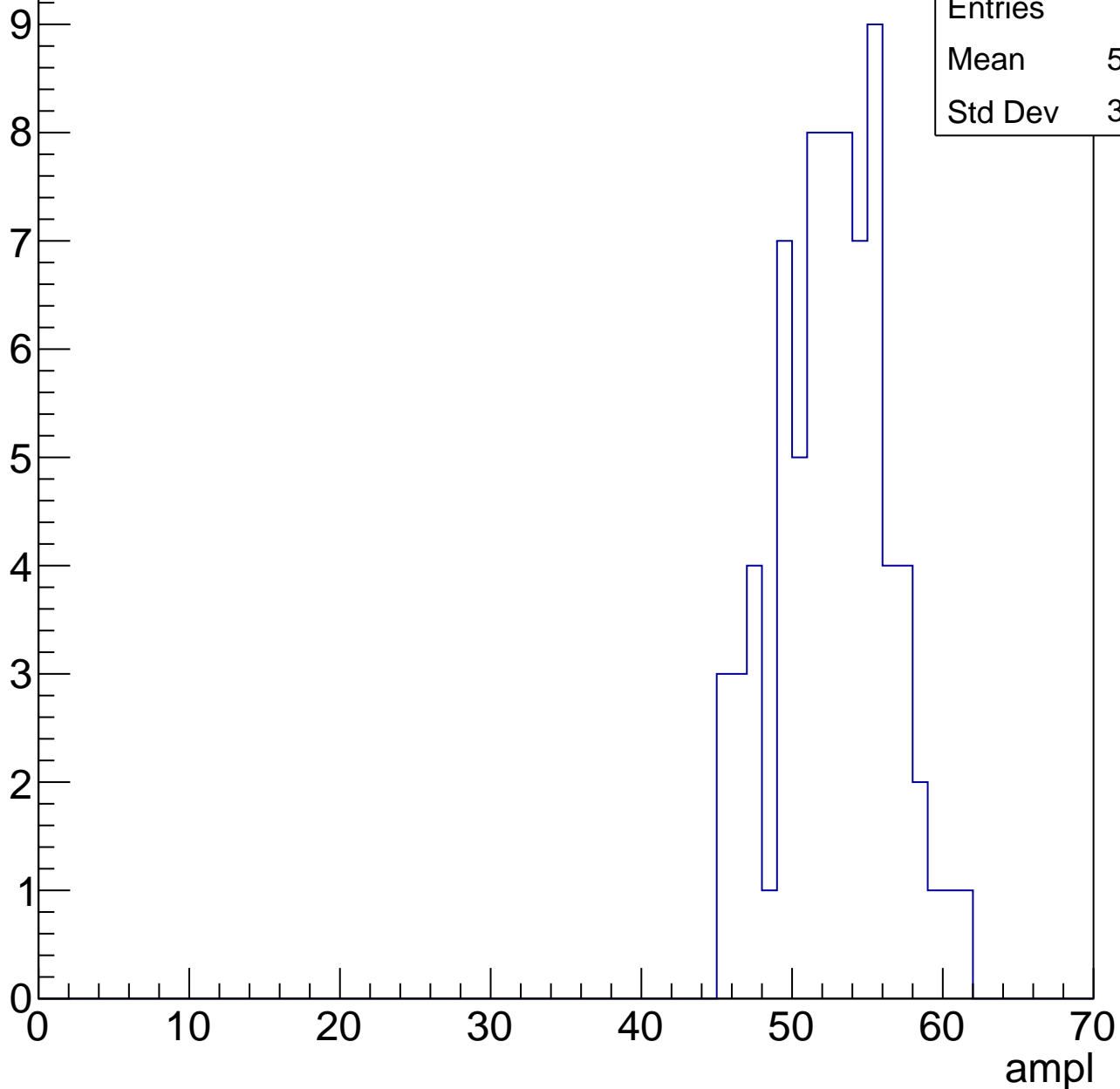
**Gaus Width: 3.9078**



# B1L101S, U11-ch97, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

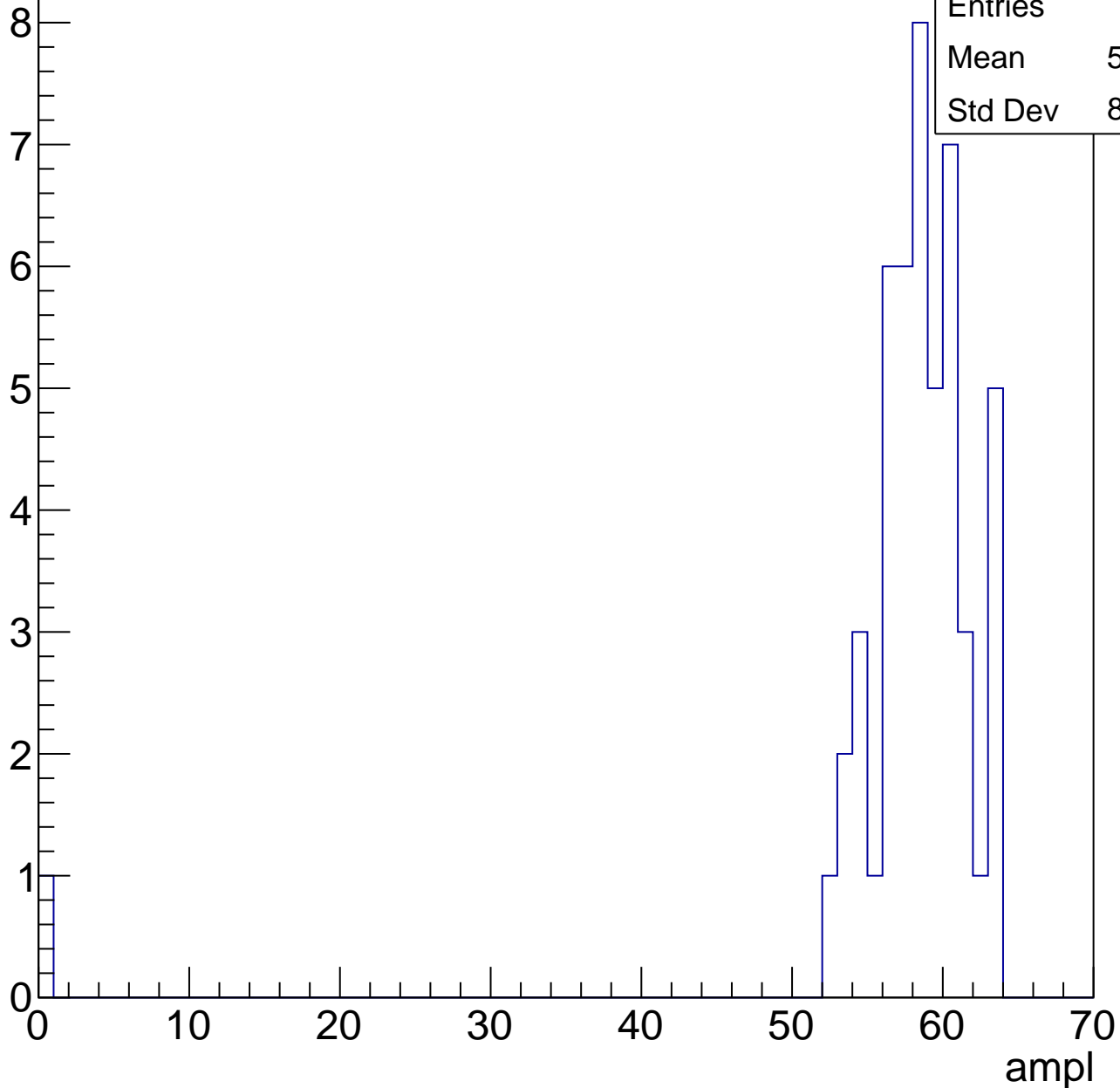
Entry



# B1L101S, U11-ch97, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

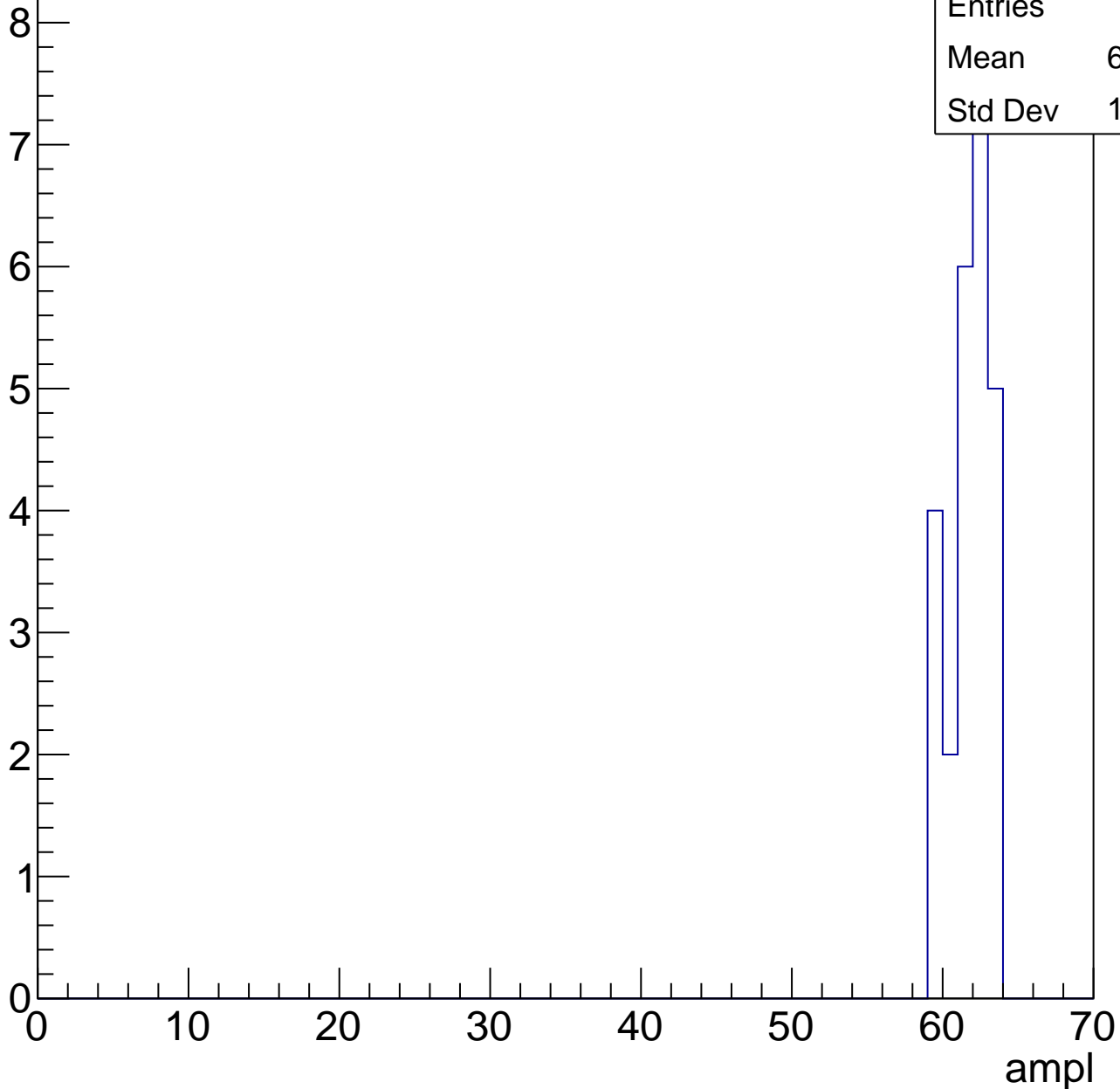


# B1L101S, U11-ch97, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	25
Mean	61.32
Std Dev	1.318



# B1L101S, U11-ch97, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch97, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U11-ch98, adc0

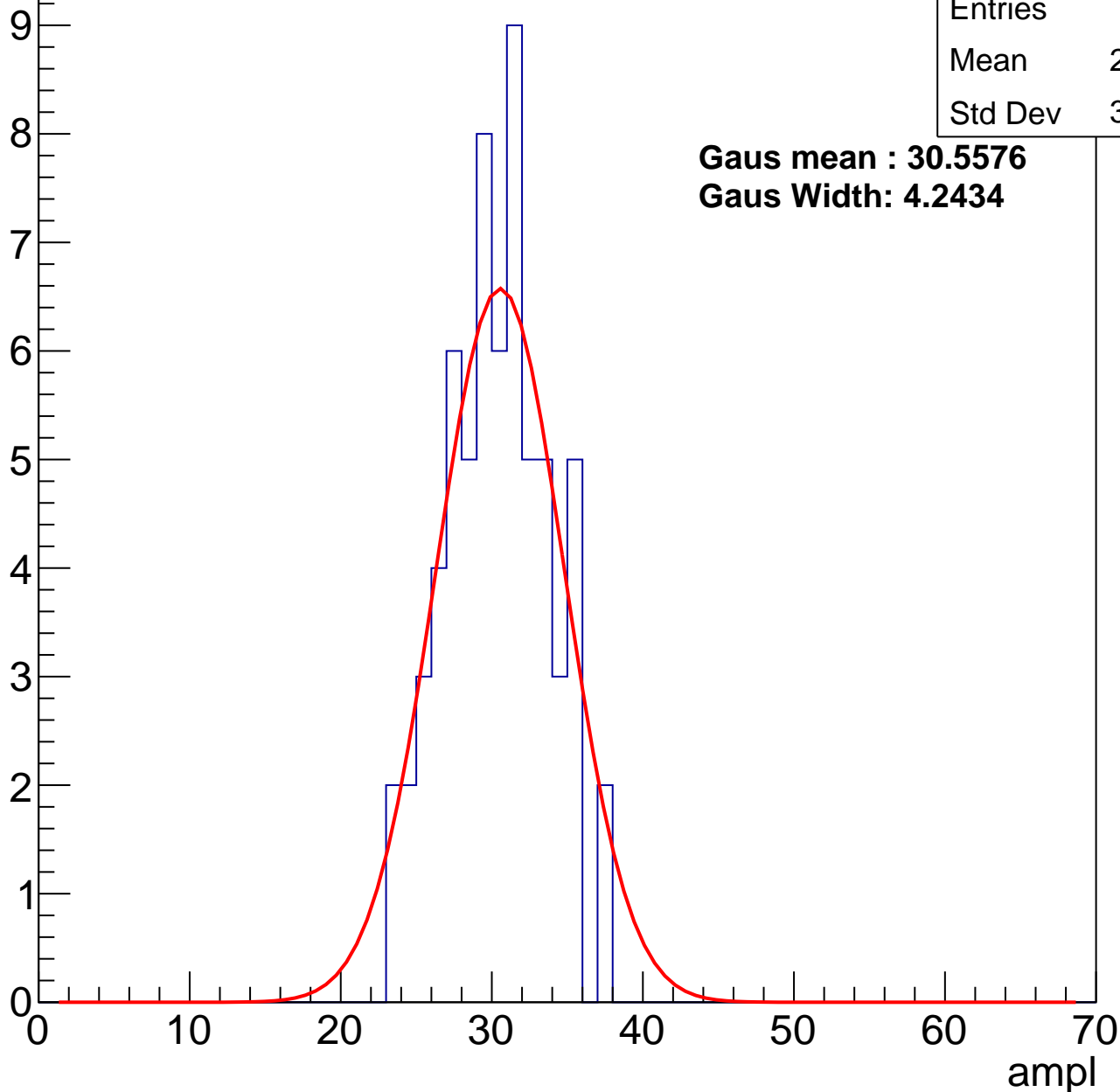
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	29.88
Std Dev	3.363

**Gaus mean : 30.5576**

**Gaus Width: 4.2434**



# B1L101S, U11-ch98, adc1

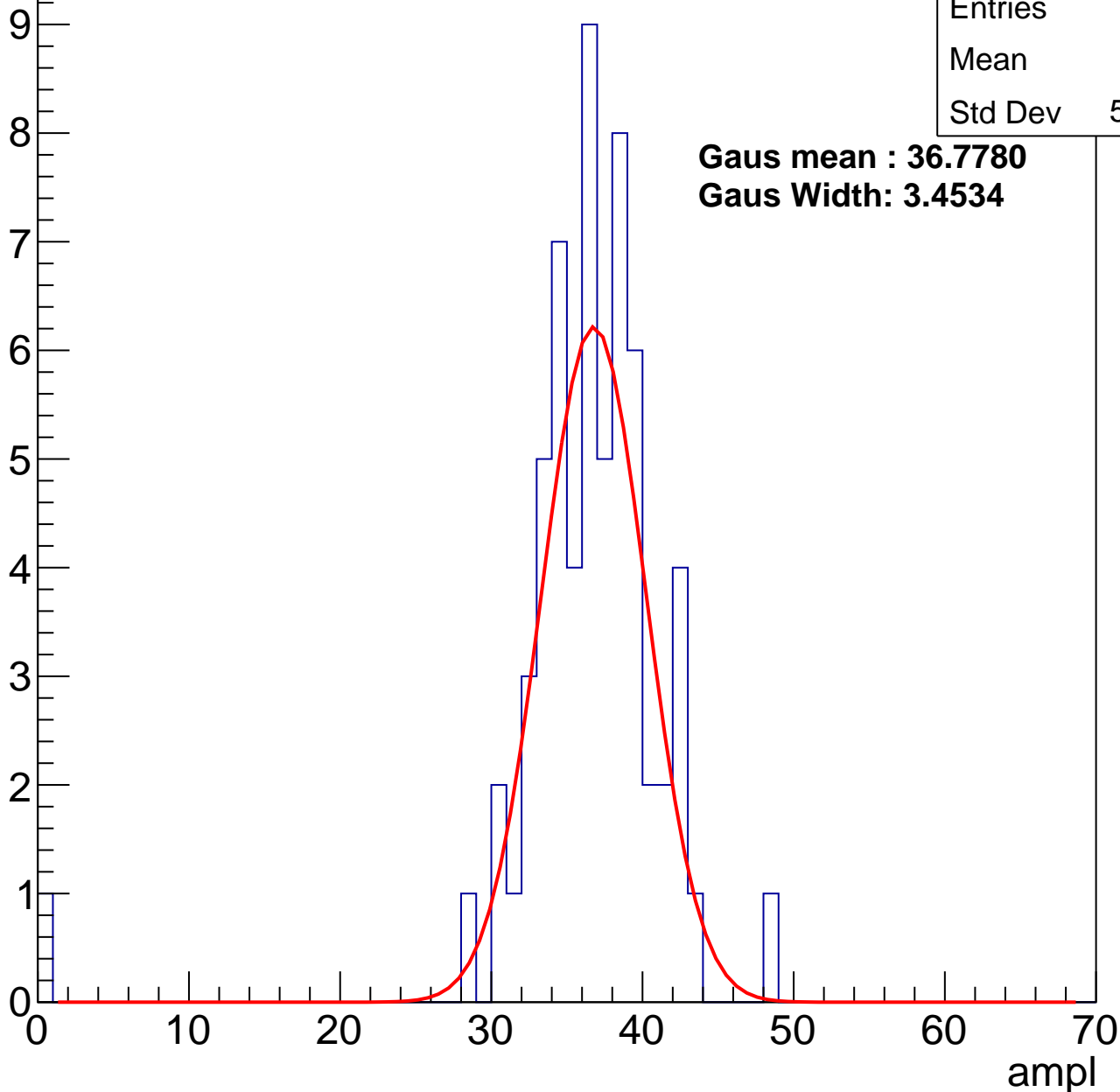
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	35.9
Std Dev	5.808

**Gaus mean : 36.7780**

**Gaus Width: 3.4534**



# B1L101S, U11-ch98, adc2

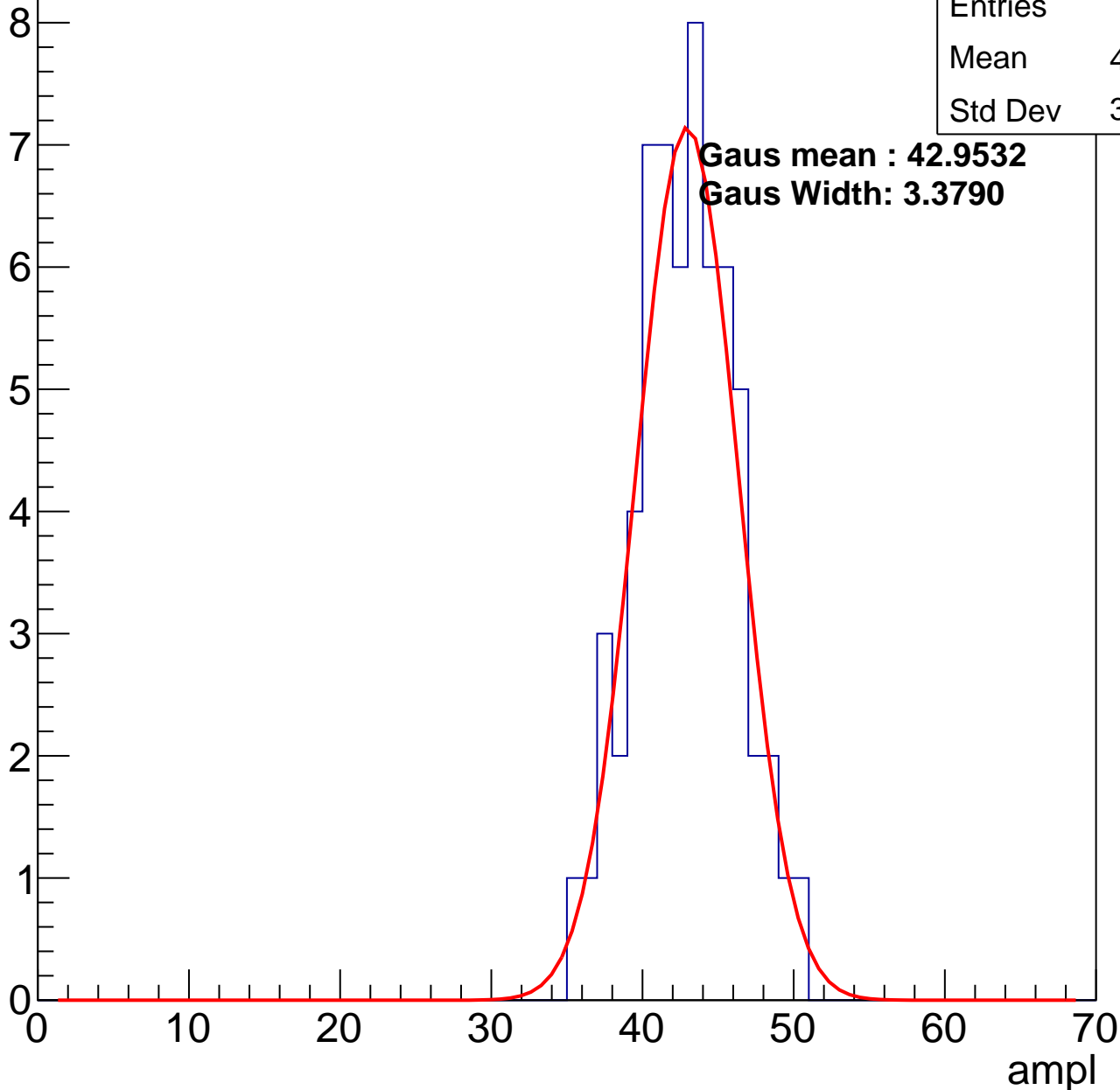
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	42.42
Std Dev	3.246

**Gaus mean : 42.9532**

**Gaus Width: 3.3790**

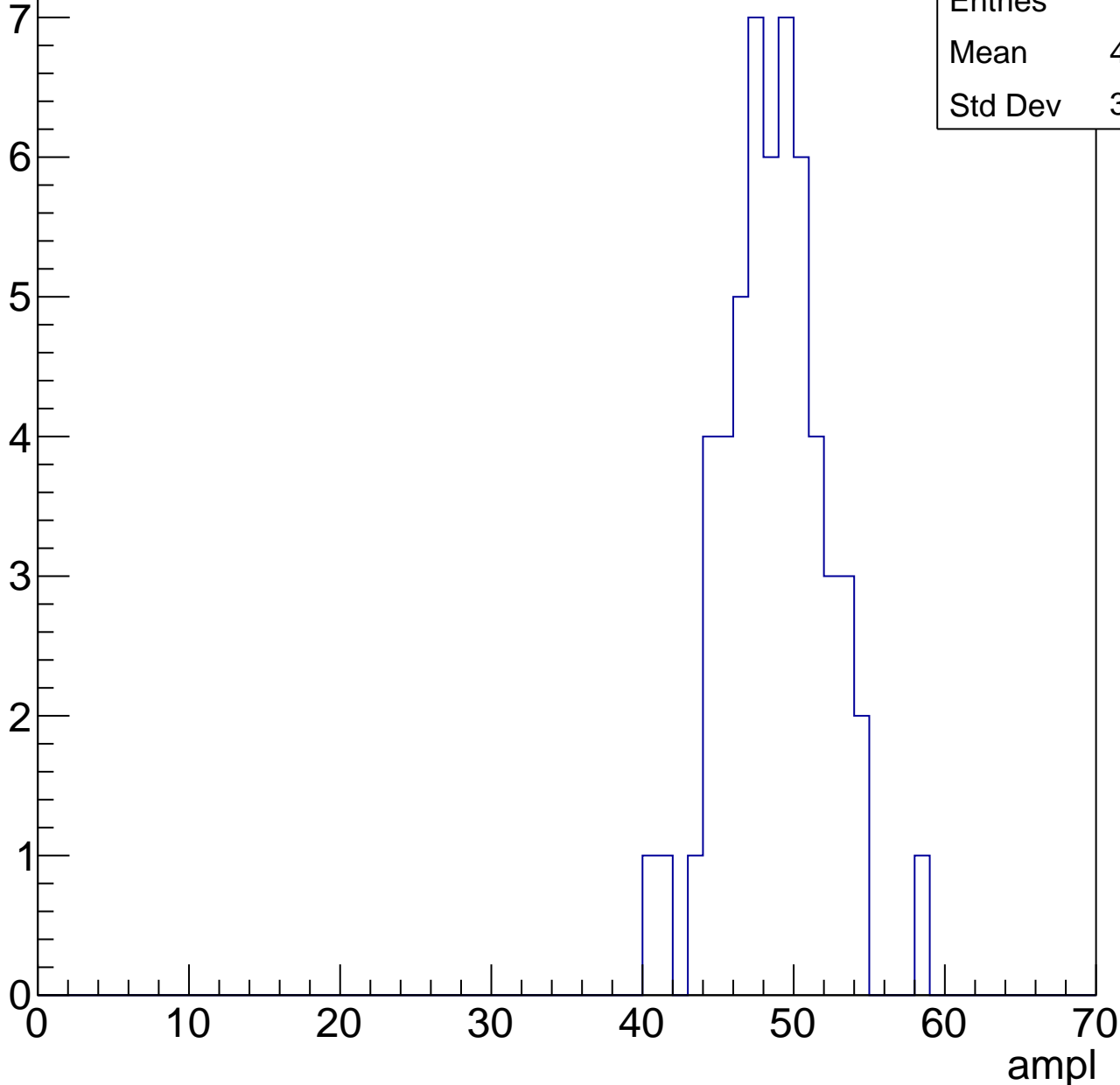


# B1L101S, U11-ch98, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	48.27
Std Dev	3.365

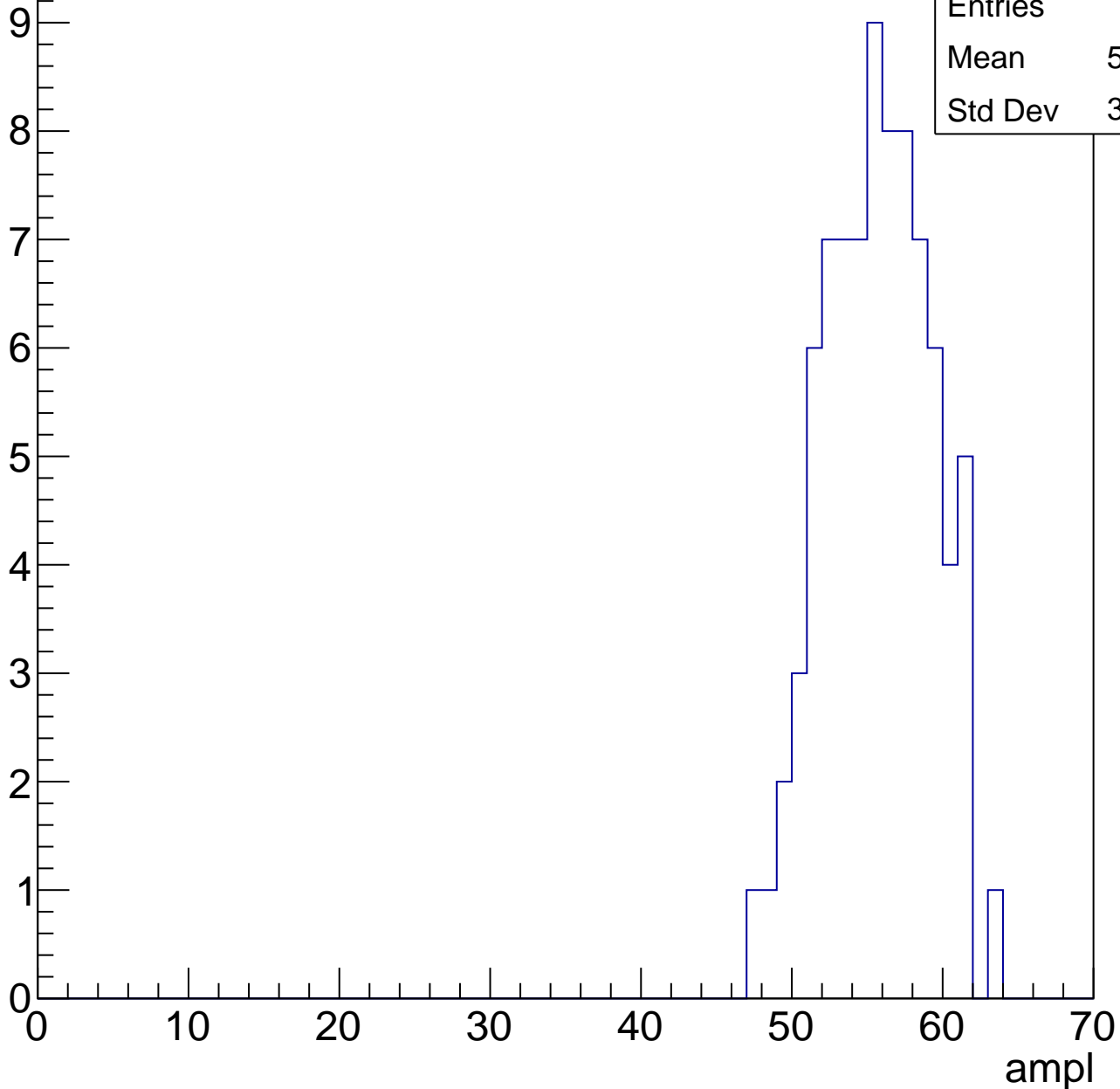


# B1L101S, U11-ch98, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

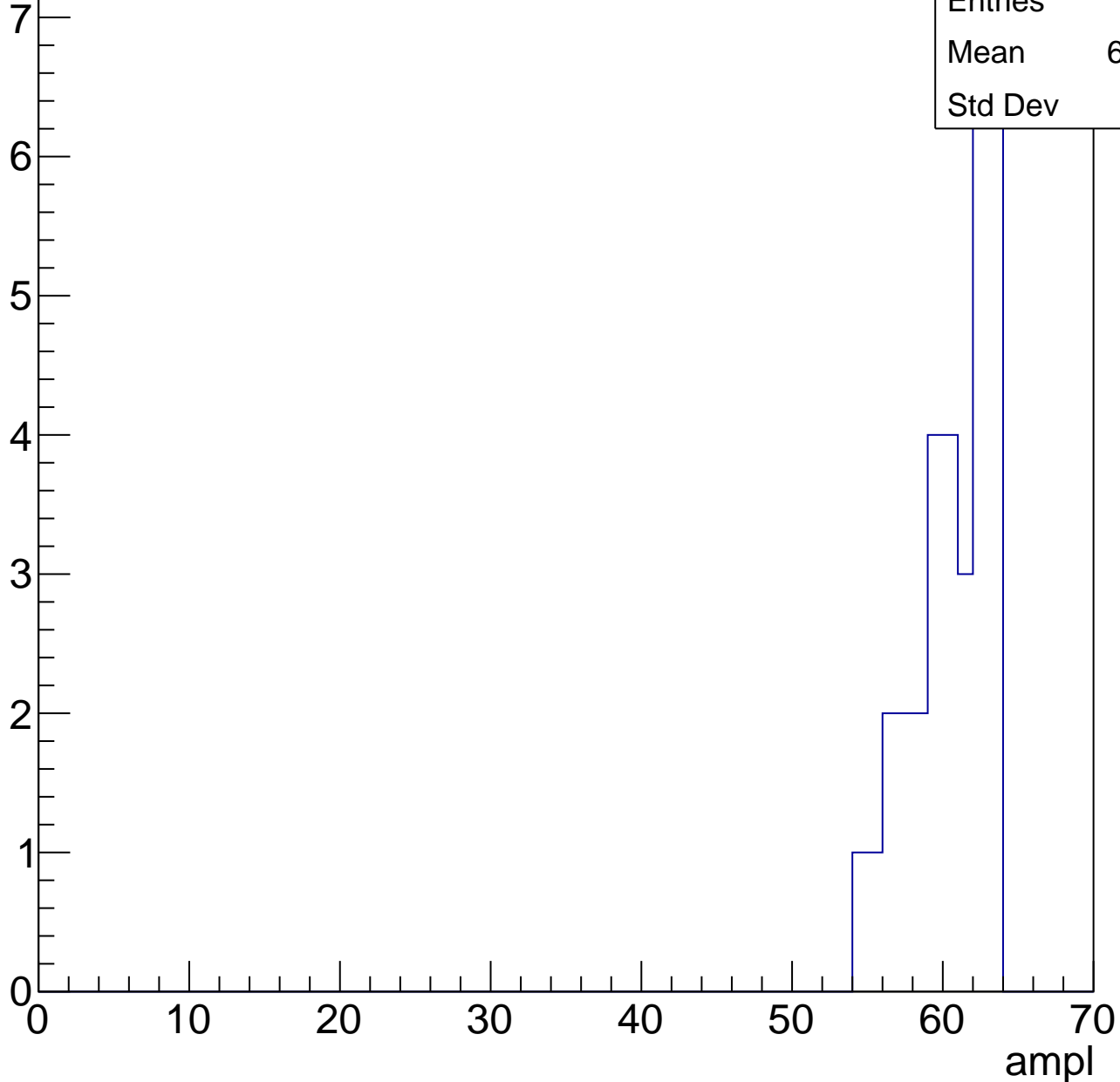
Entries	82
Mean	55.23
Std Dev	3.479



# B1L101S, U11-ch98, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

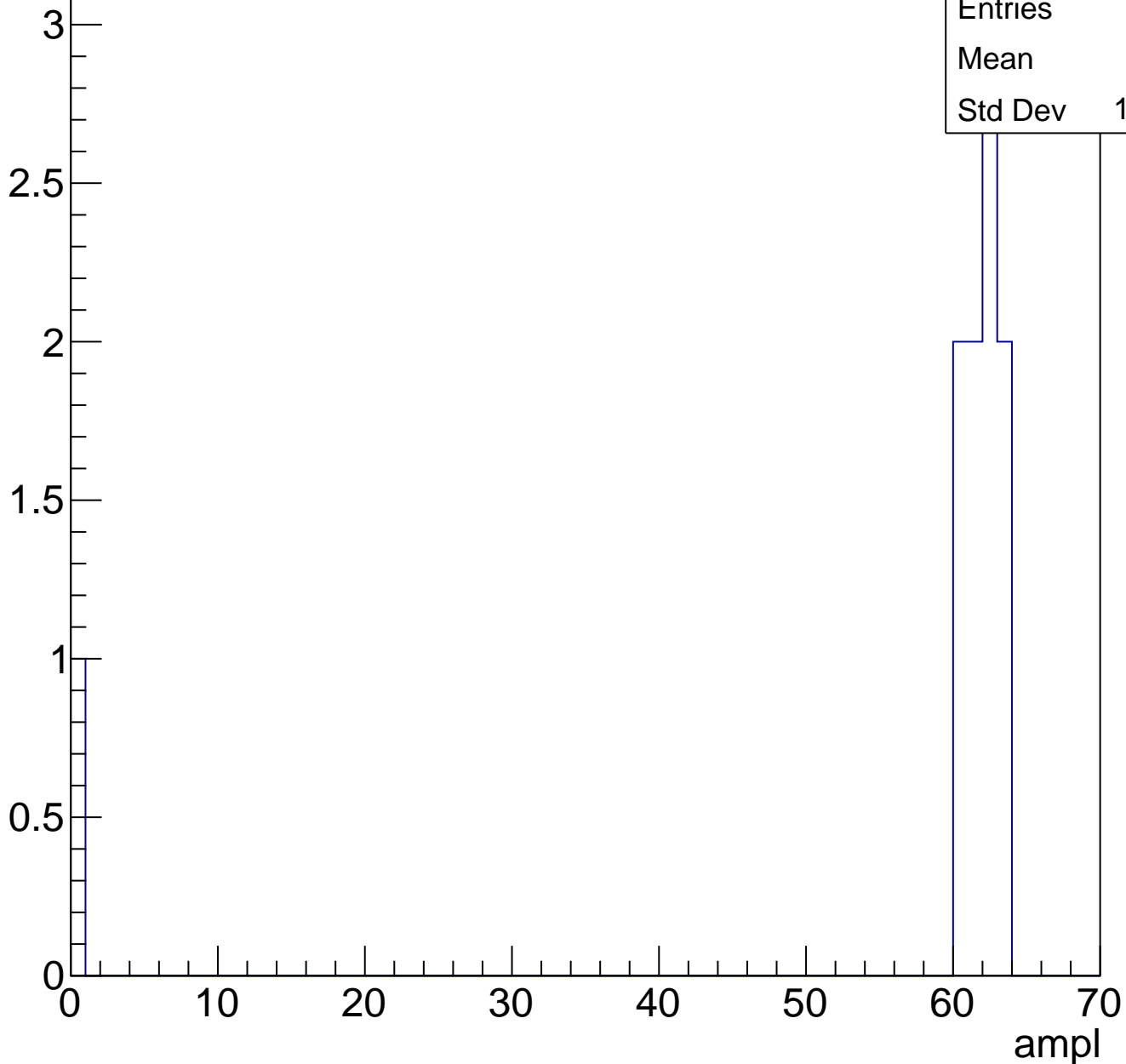
Entry



# B1L101S, U11-ch98, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	10
Mean	55.4
Std Dev	18.49



# B1L101S, U11-ch98, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U11-ch99, adc0

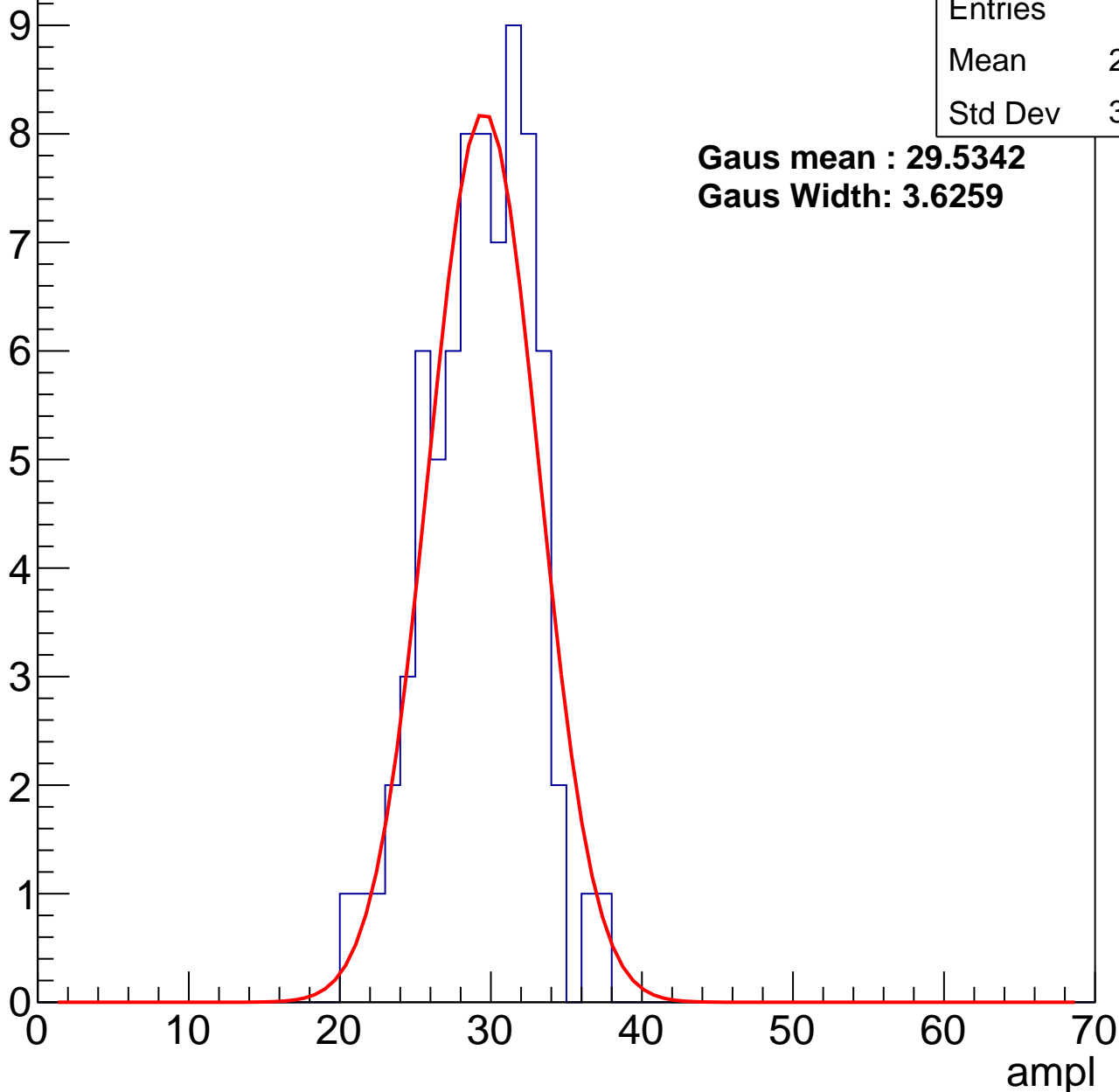
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	28.84
Std Dev	3.437

**Gaus mean : 29.5342**

**Gaus Width: 3.6259**



# B1L101S, U11-ch99, adc1

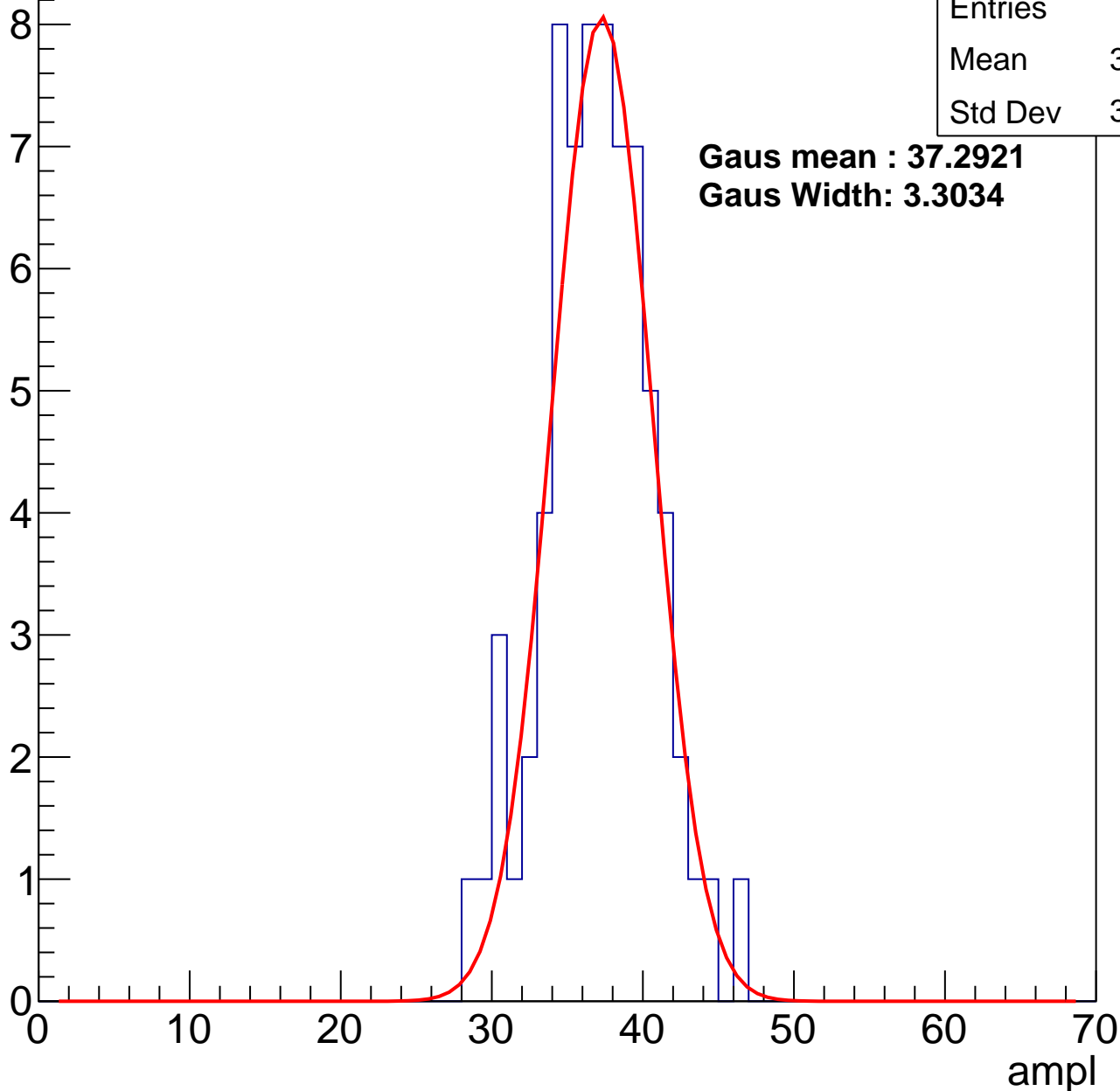
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	36.55
Std Dev	3.552

**Gaus mean : 37.2921**

**Gaus Width: 3.3034**



# B1L101S, U11-ch99, adc2

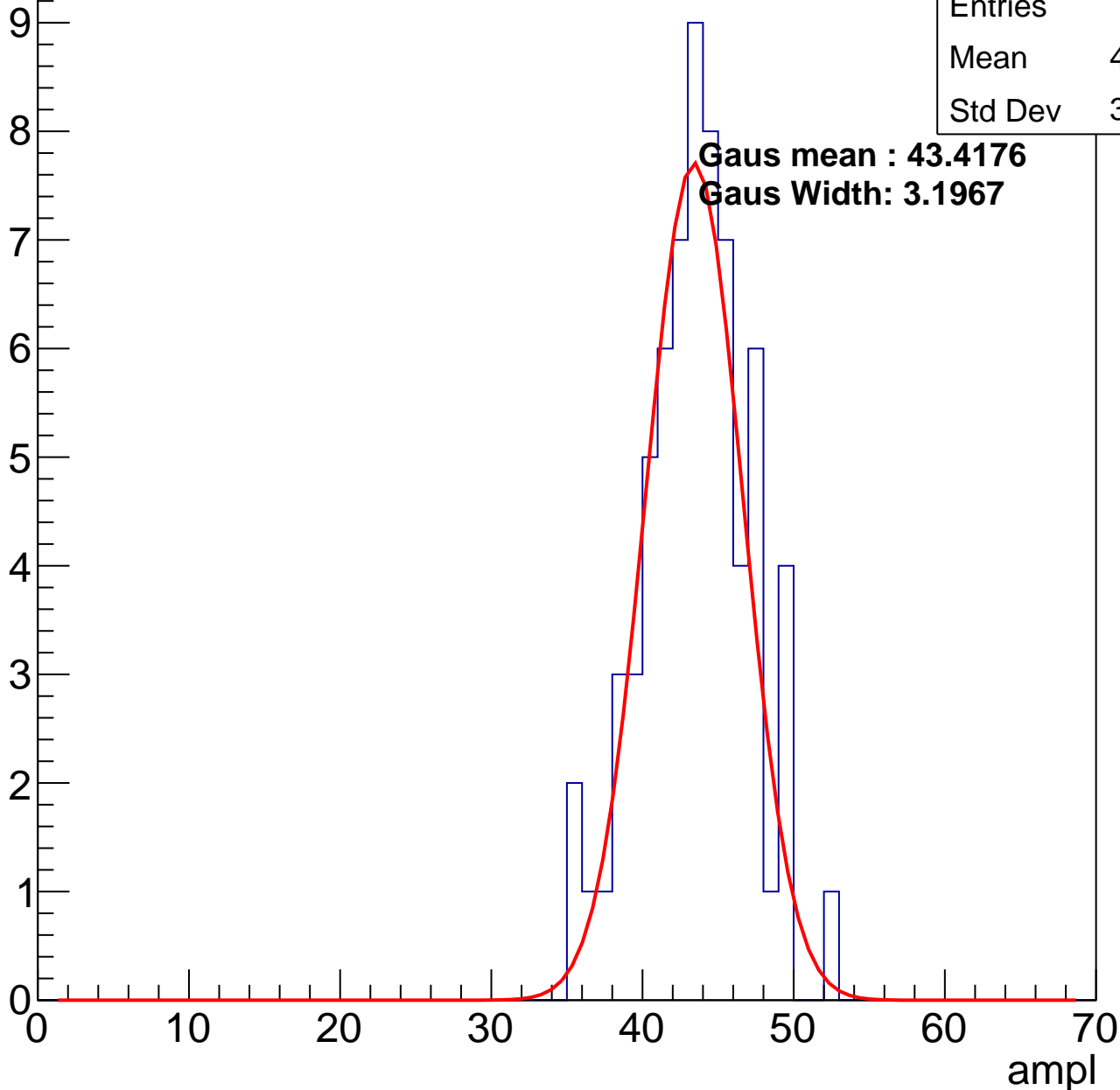
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	43.09
Std Dev	3.493

**Gaus mean : 43.4176**

**Gaus Width: 3.1967**

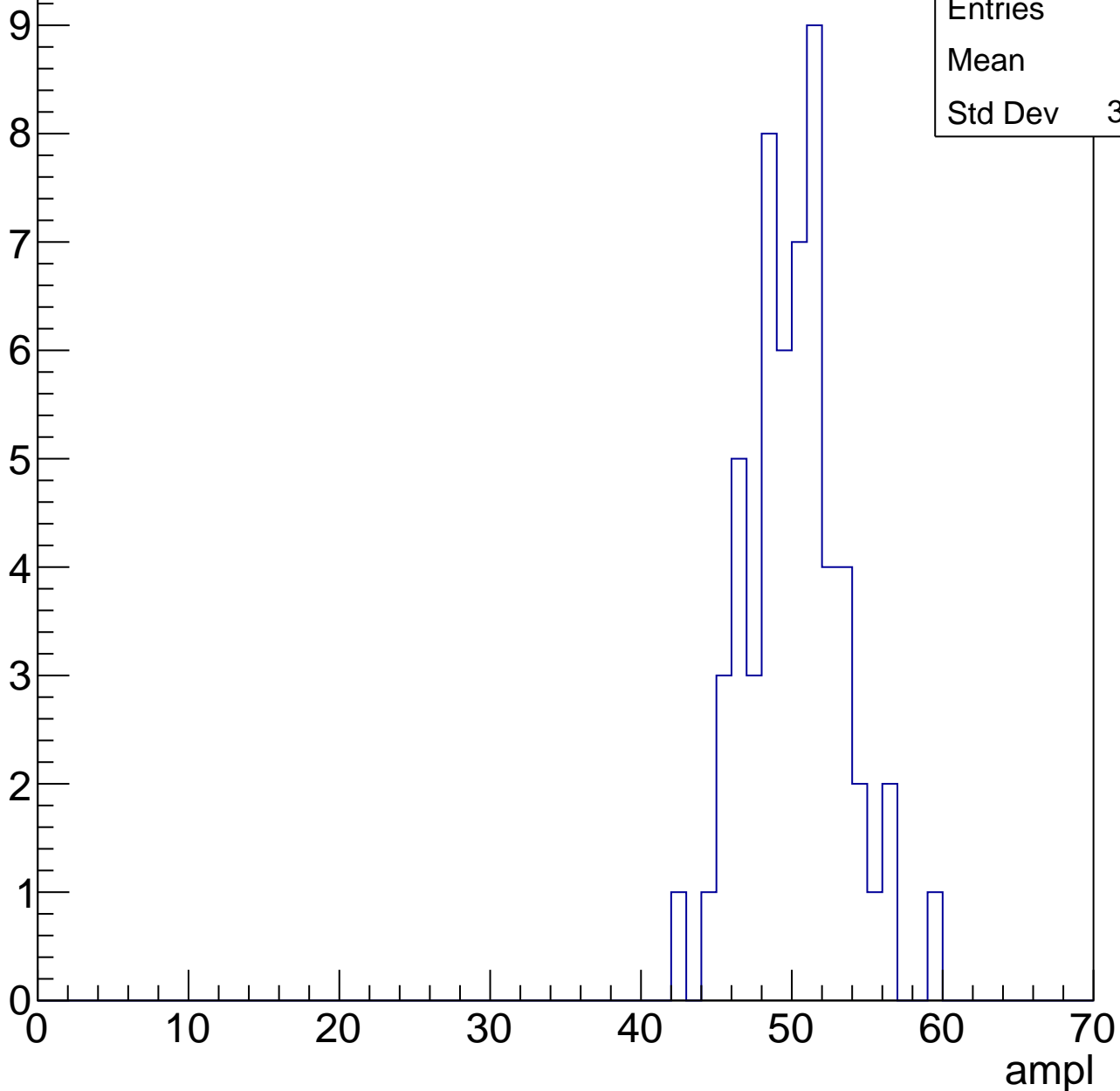


# B1L101S, U11-ch99, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	49.7
Std Dev	3.206

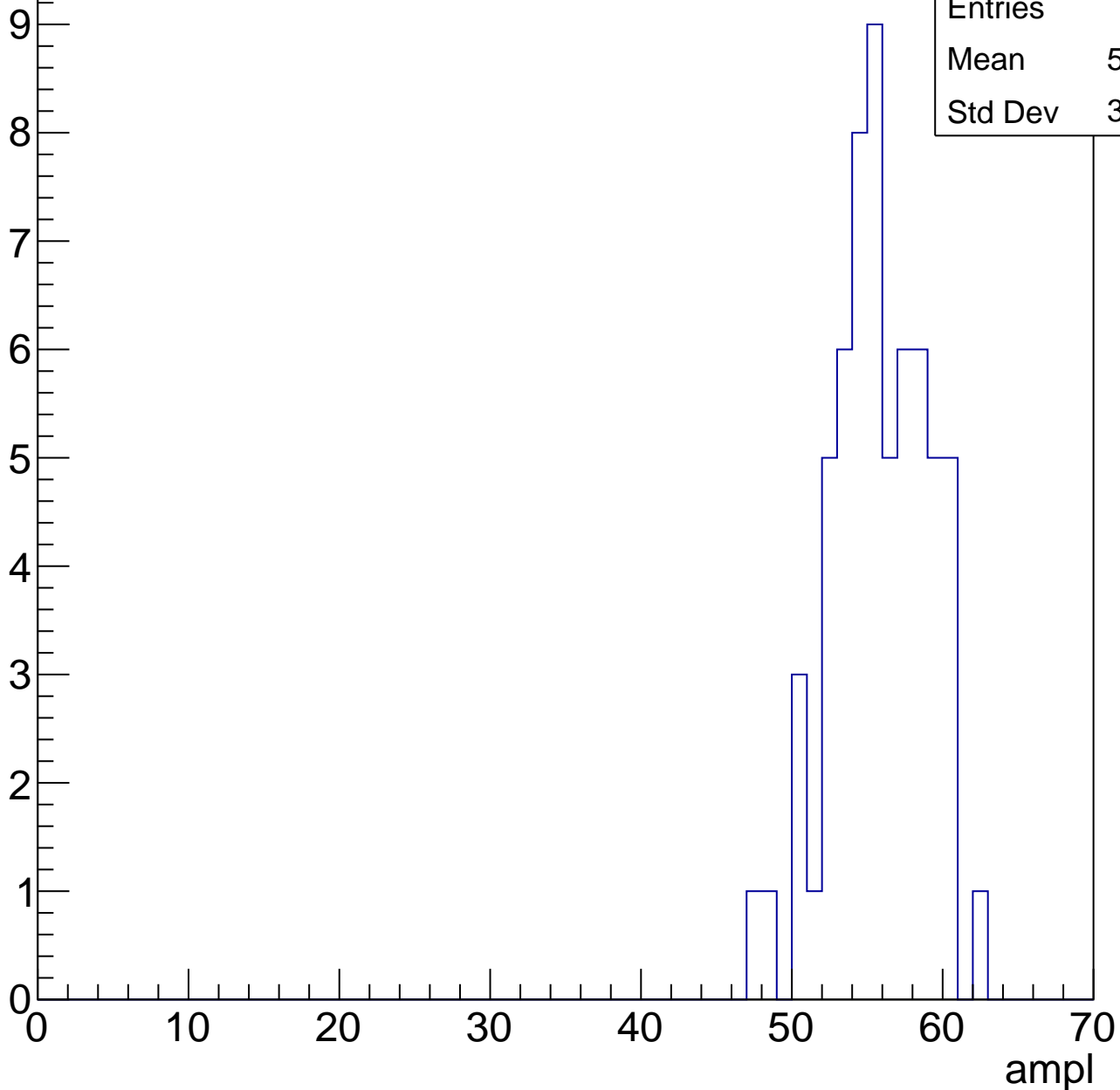


# B1L101S, U11-ch99, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	55.29
Std Dev	3.144

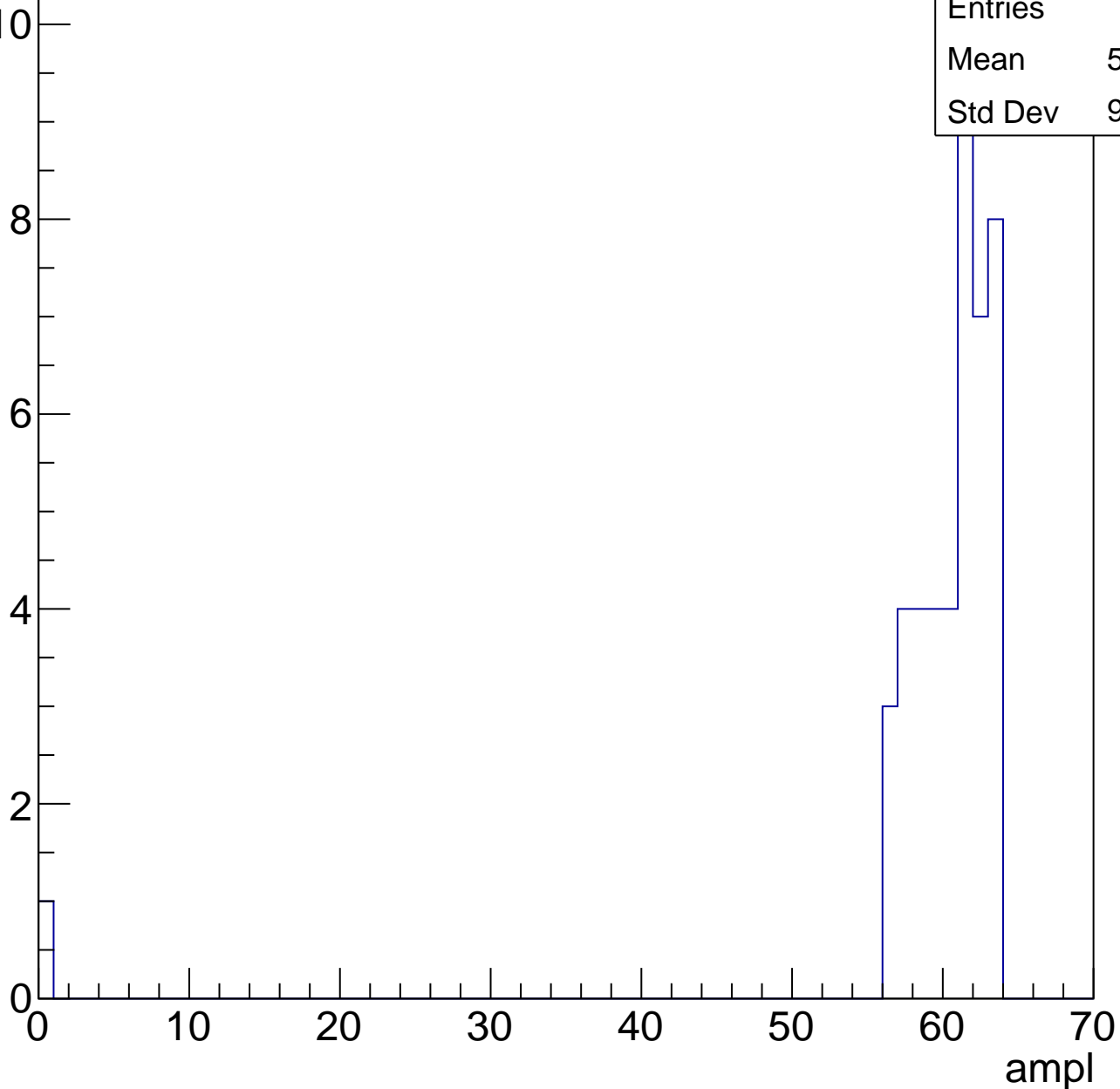


# B1L101S, U11-ch99, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	45
Mean	58.93
Std Dev	9.144



# B1L101S, U11-ch99, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch99, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U11-ch100, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	84
Mean	26.89
Std Dev	6.388

**Gaus mean : 28.4483**

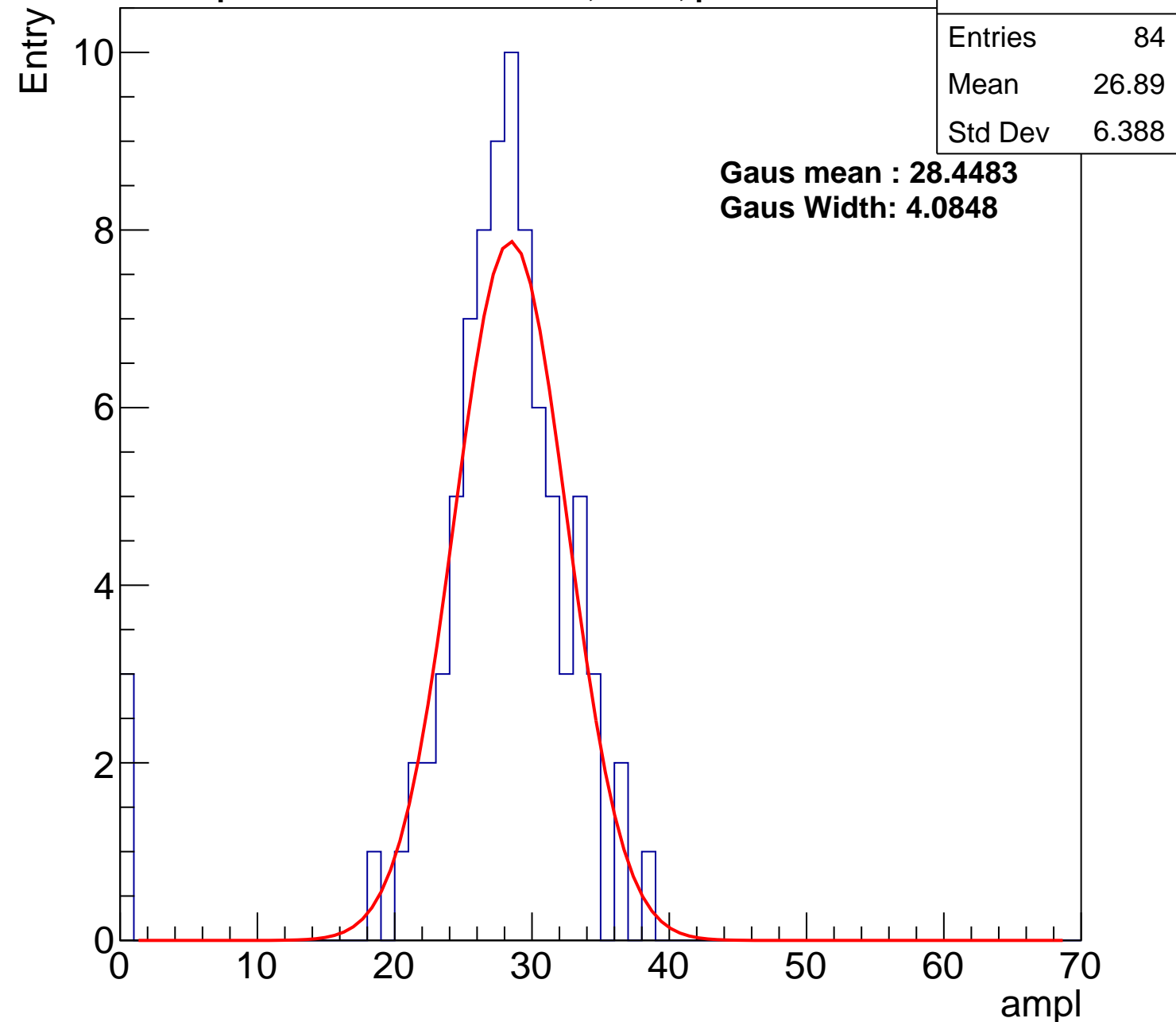
**Gaus Width: 4.0848**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U11-ch100, adc1

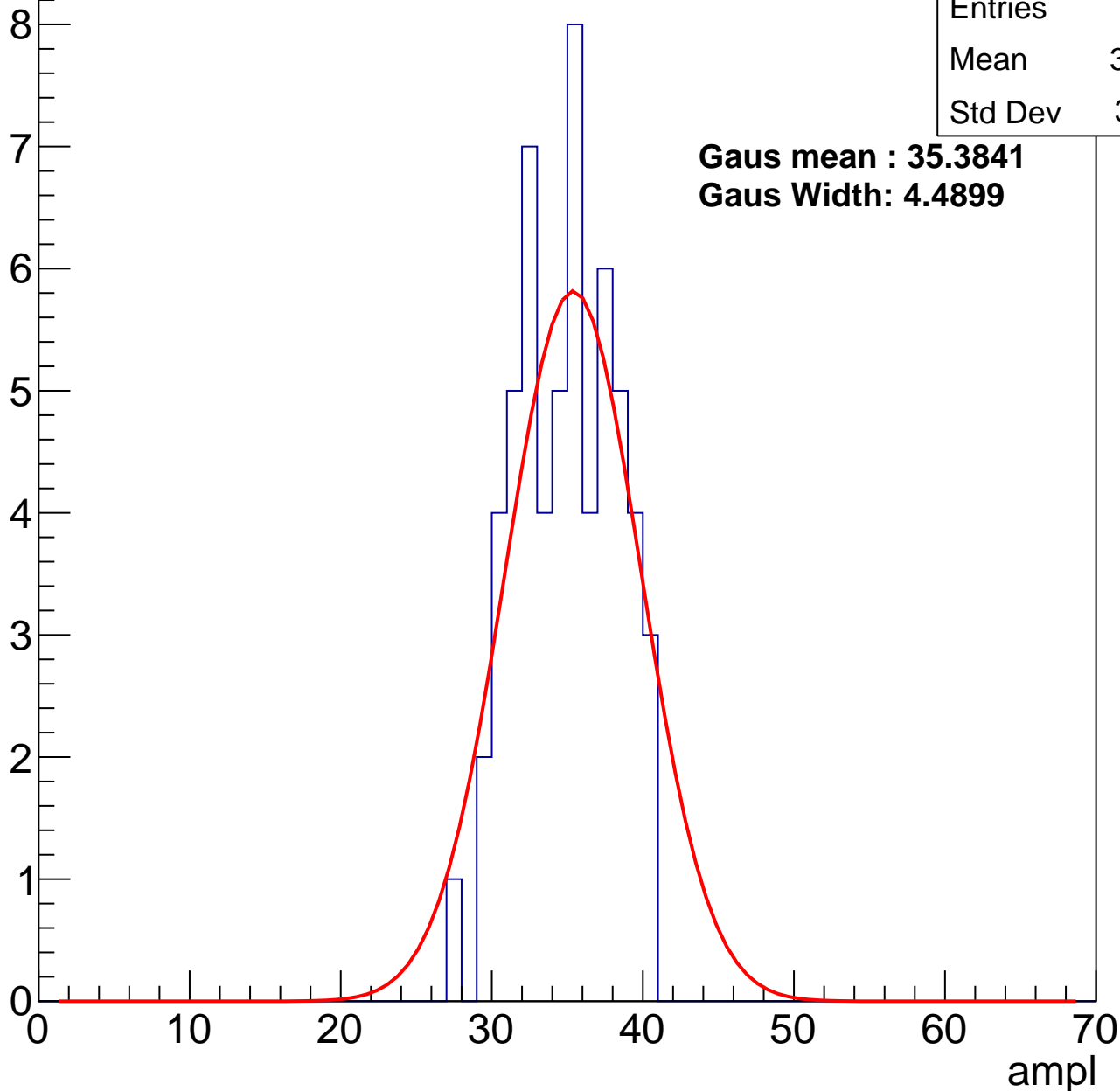
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	34.45
Std Dev	3.201

**Gaus mean : 35.3841**

**Gaus Width: 4.4899**



# B1L101S, U11-ch100, adc2

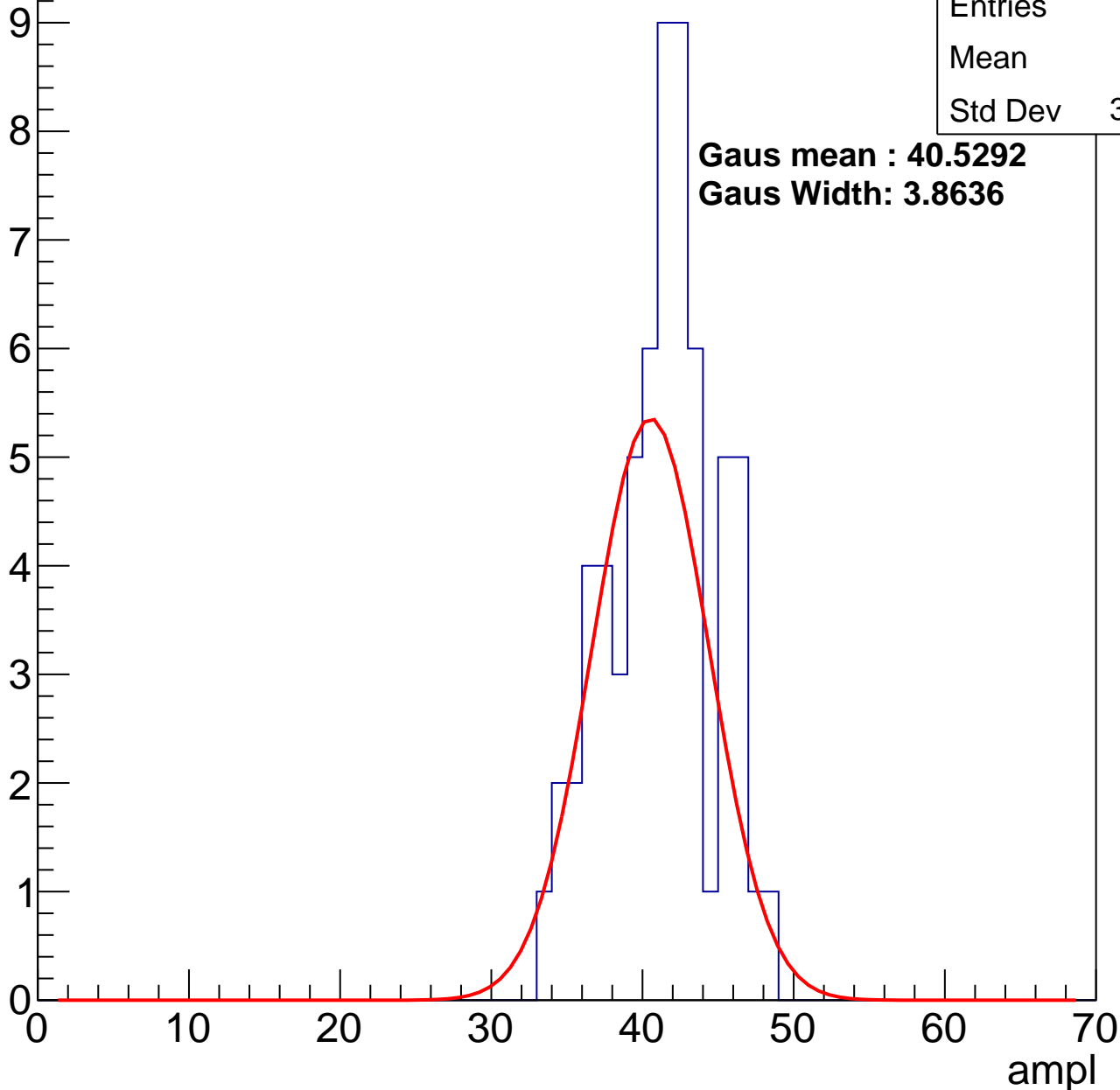
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	40.8
Std Dev	3.492

**Gaus mean : 40.5292**

**Gaus Width: 3.8636**

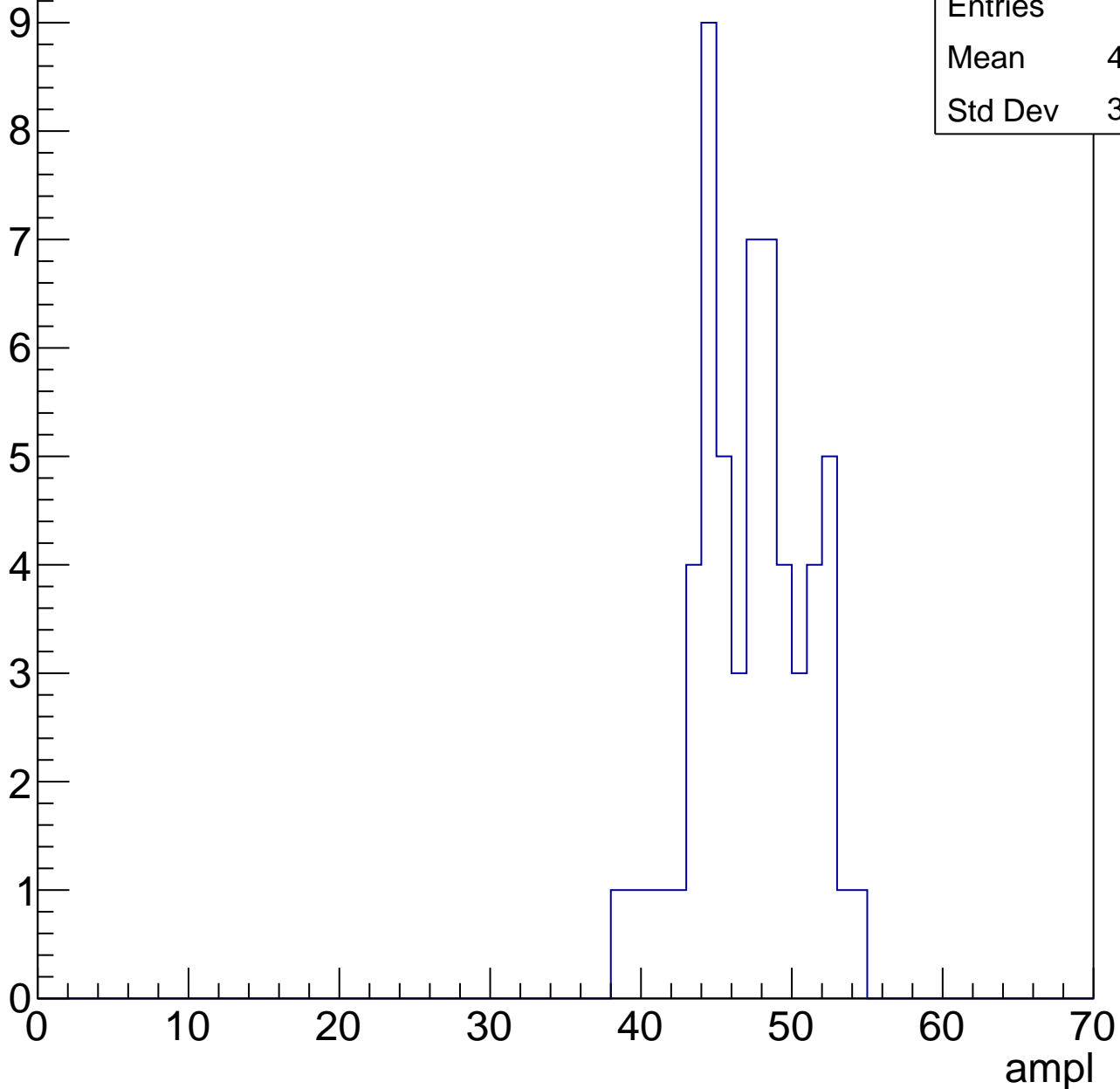


# B1L101S, U11-ch100, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	46.78
Std Dev	3.582

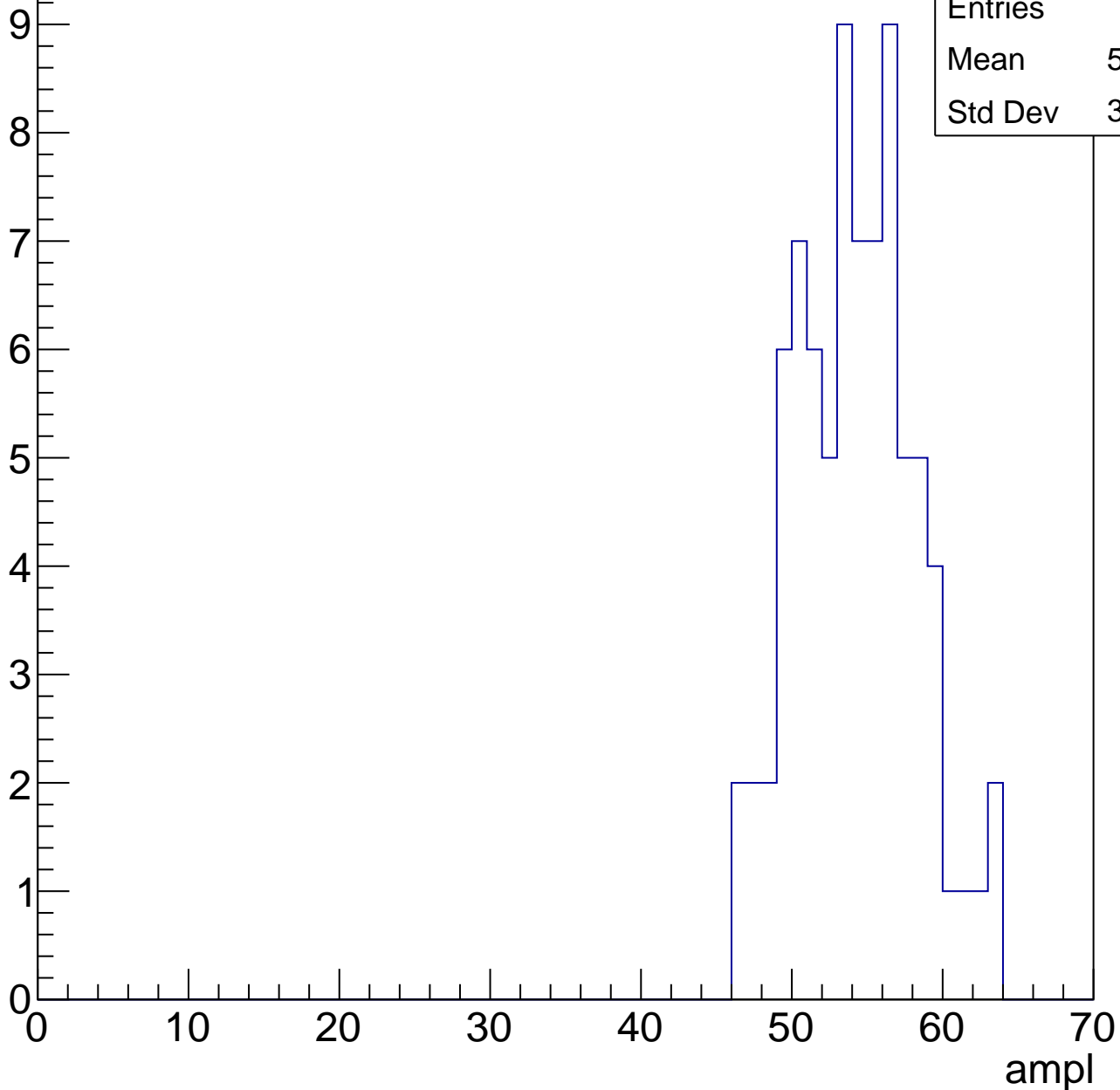


# B1L101S, U11-ch100, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	81
Mean	53.78
Std Dev	3.878



# B1L101S, U11-ch100, adc5

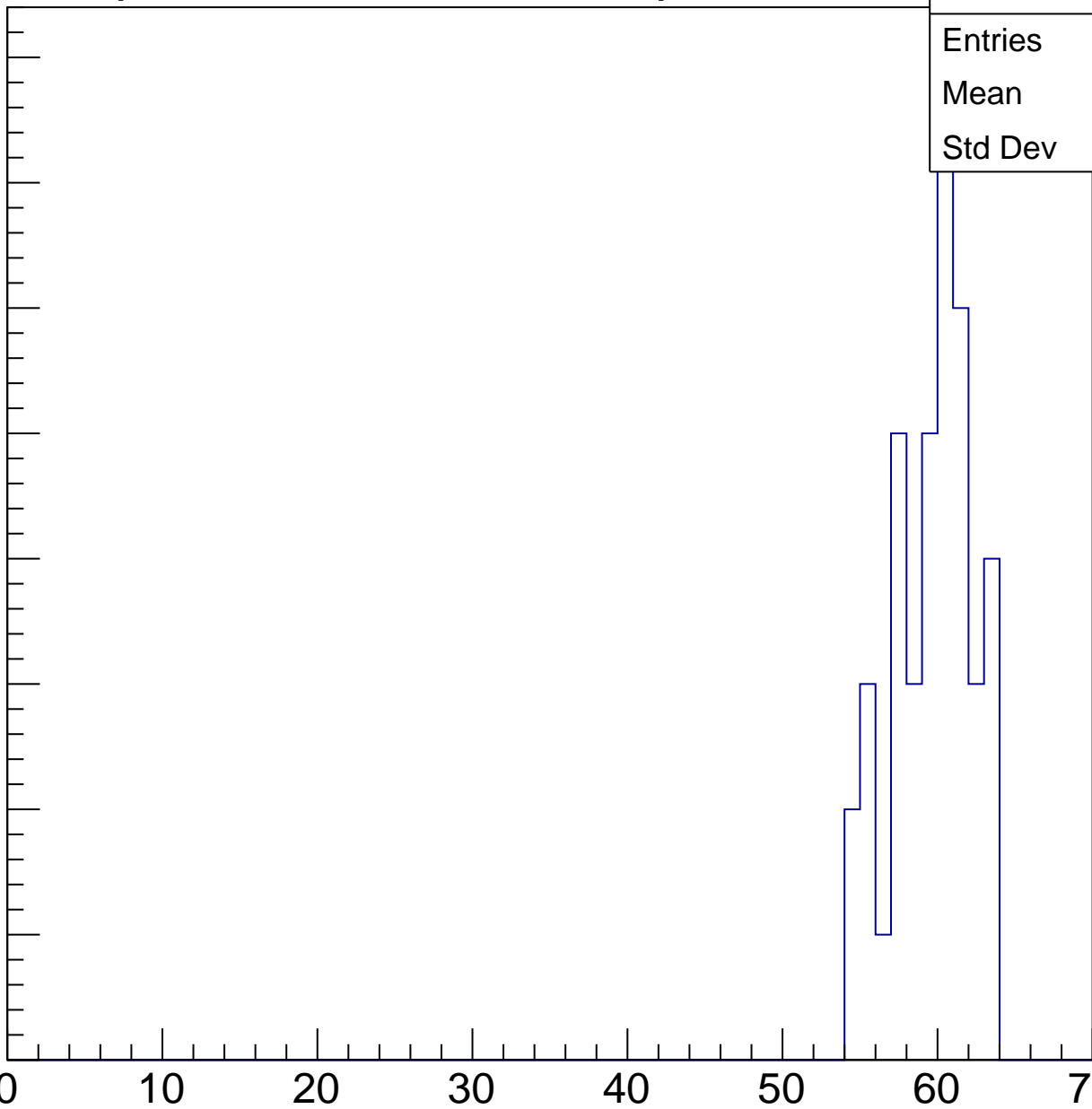
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	40
Mean	59.17
Std Dev	2.509

ampl

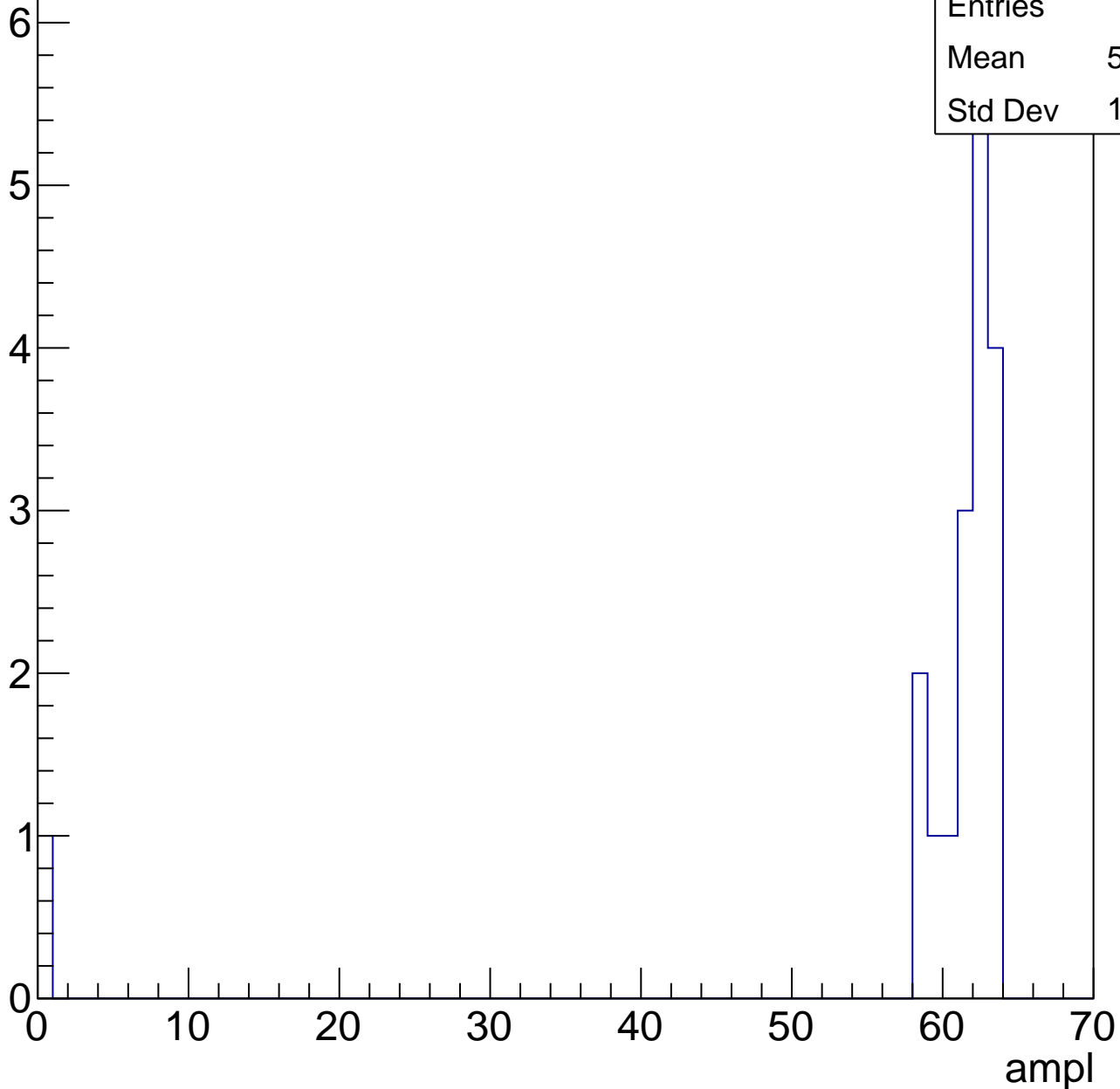


# B1L101S, U11-ch100, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	18
Mean	57.89
Std Dev	14.13





# B1L101S, U11-ch100, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U11-ch101, adc0

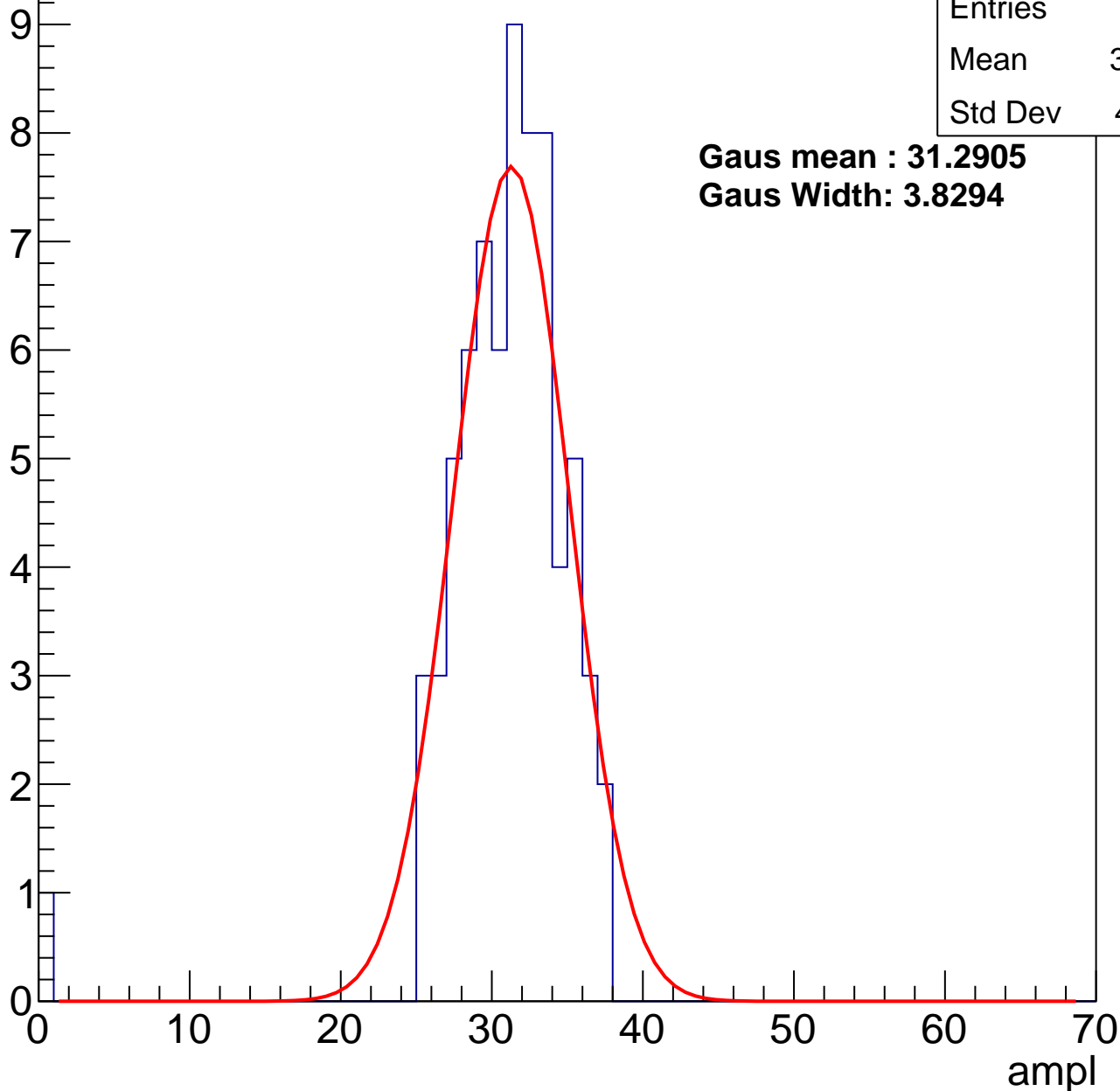
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	30.44
Std Dev	4.771

**Gaus mean : 31.2905**

**Gaus Width: 3.8294**



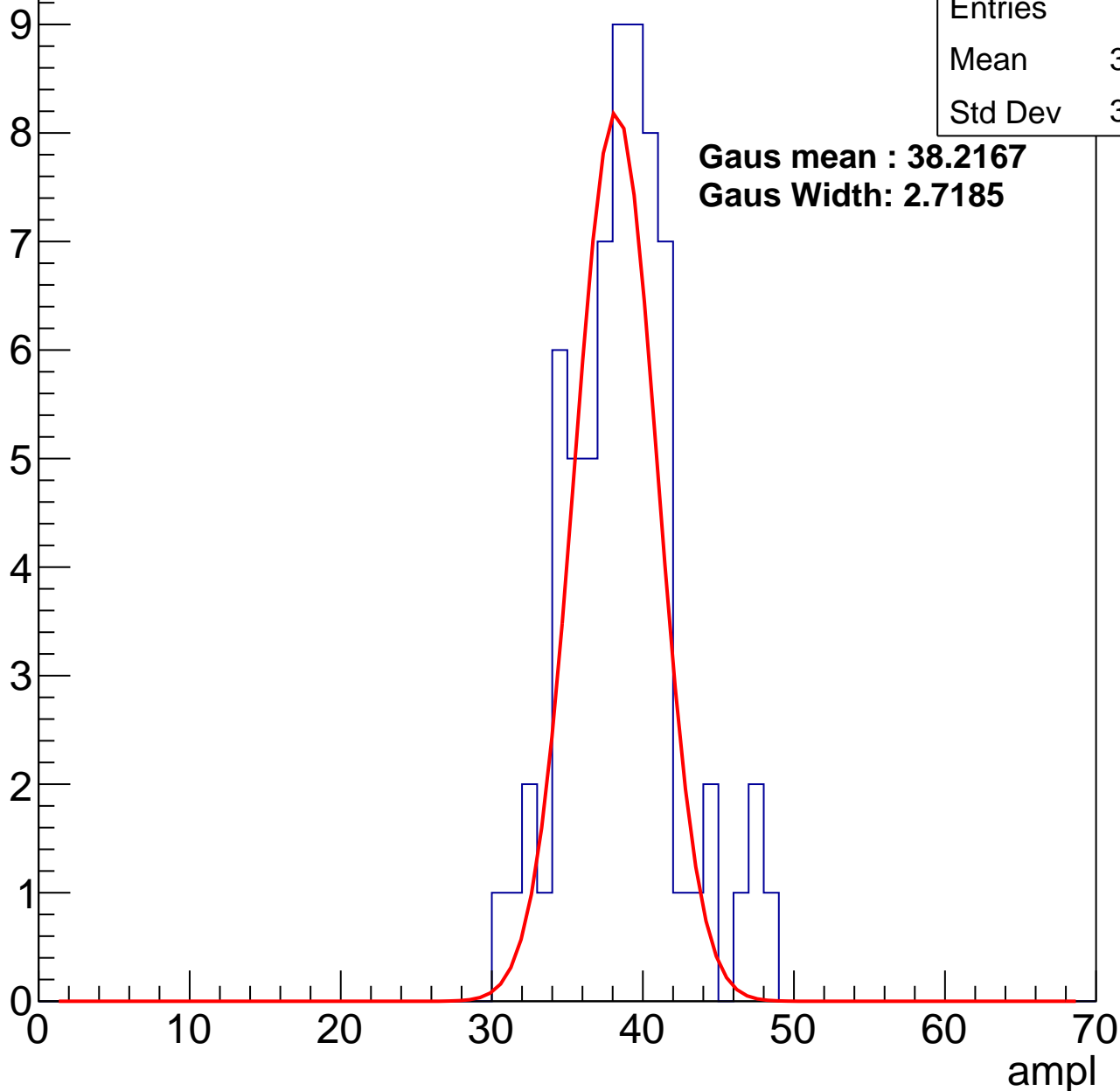
# B1L101S, U11-ch101, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	38.22
Std Dev	3.647

**Gaus mean : 38.2167**  
**Gaus Width: 2.7185**



# B1L101S, U11-ch101, adc2

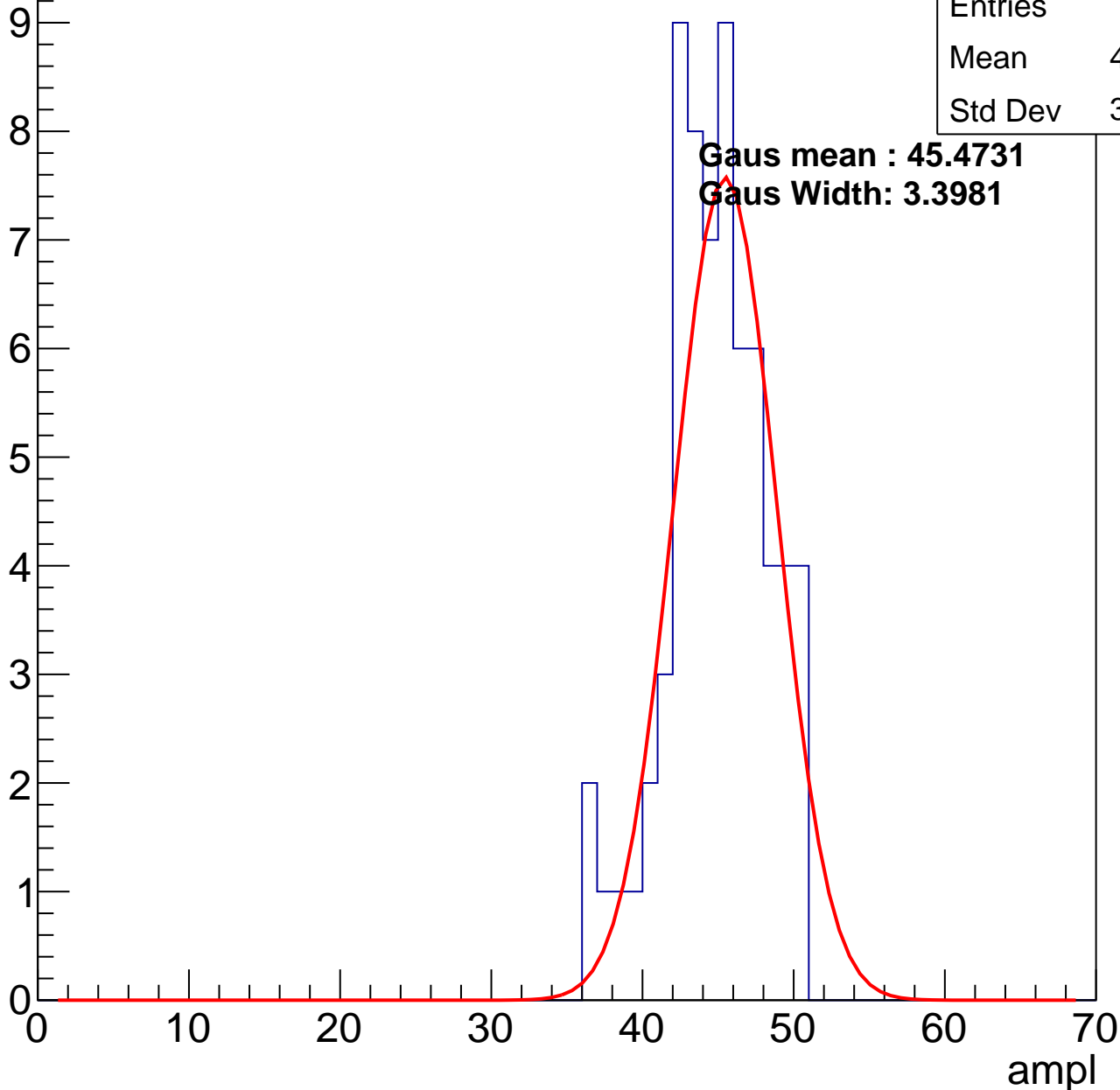
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	44.33
Std Dev	3.298

**Gaus mean : 45.4731**

**Gaus Width: 3.3981**

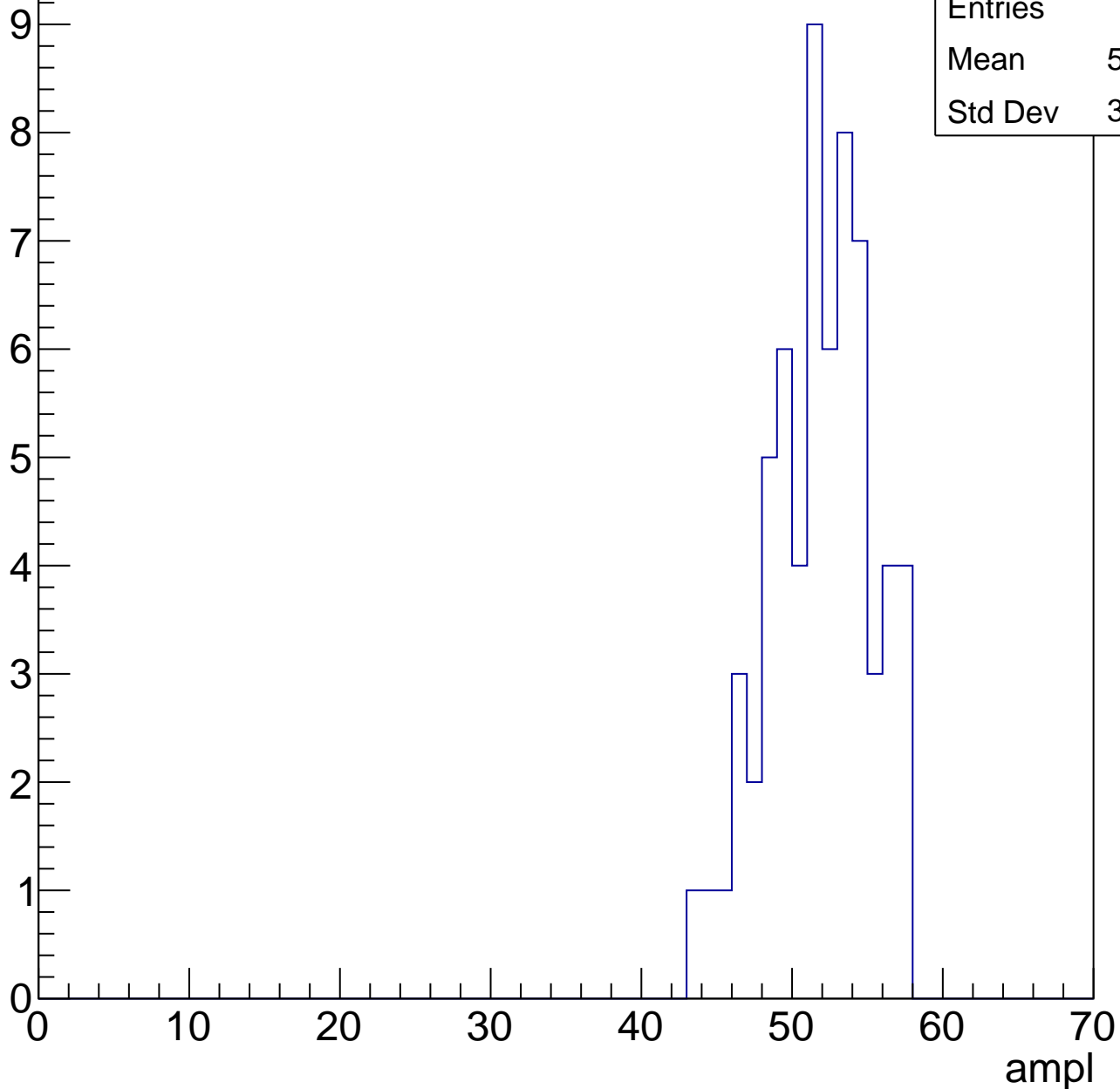


# B1L101S, U11-ch101, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

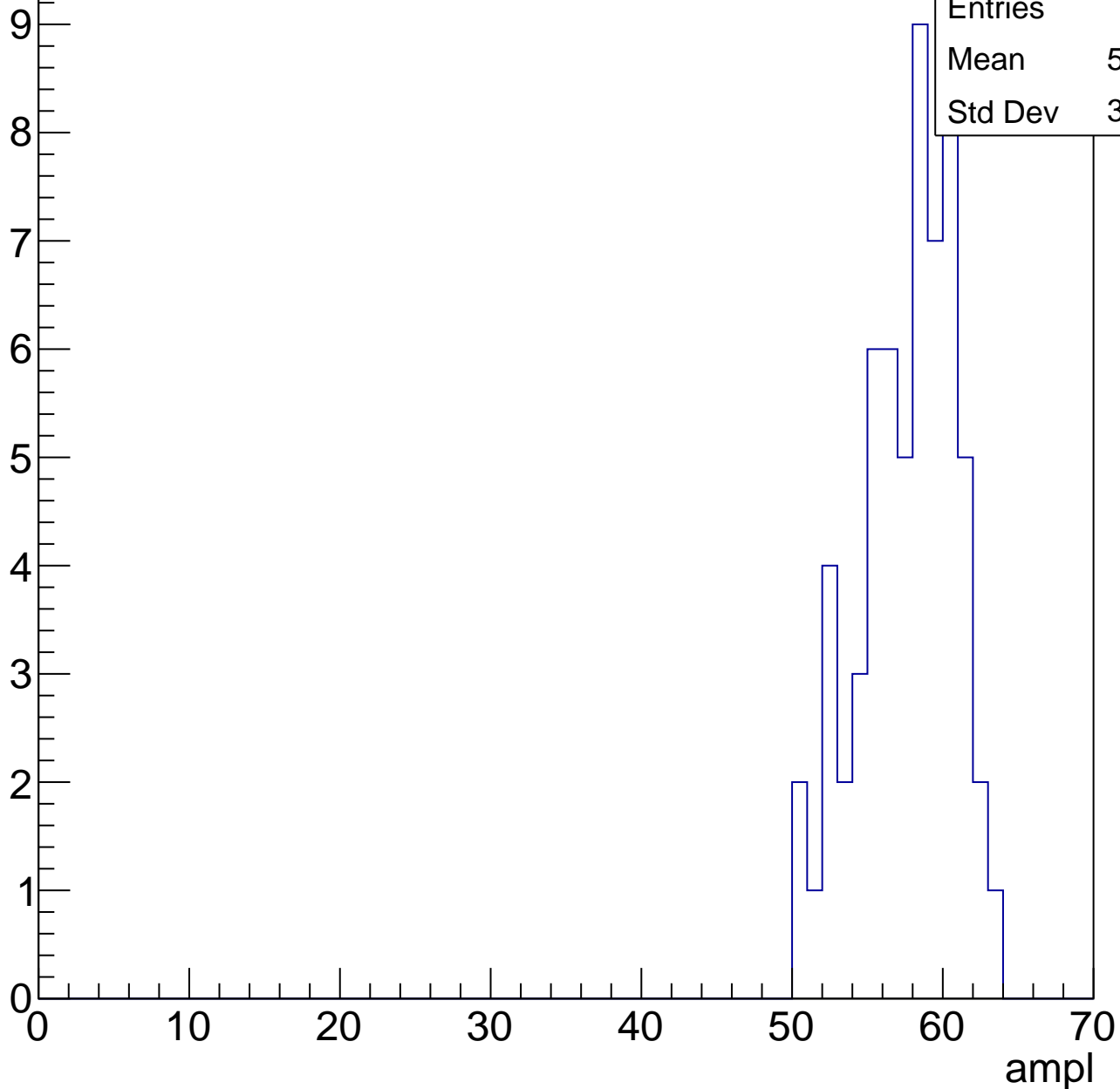
Entries	64
Mean	51.38
Std Dev	3.338



# B1L101S, U11-ch101, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

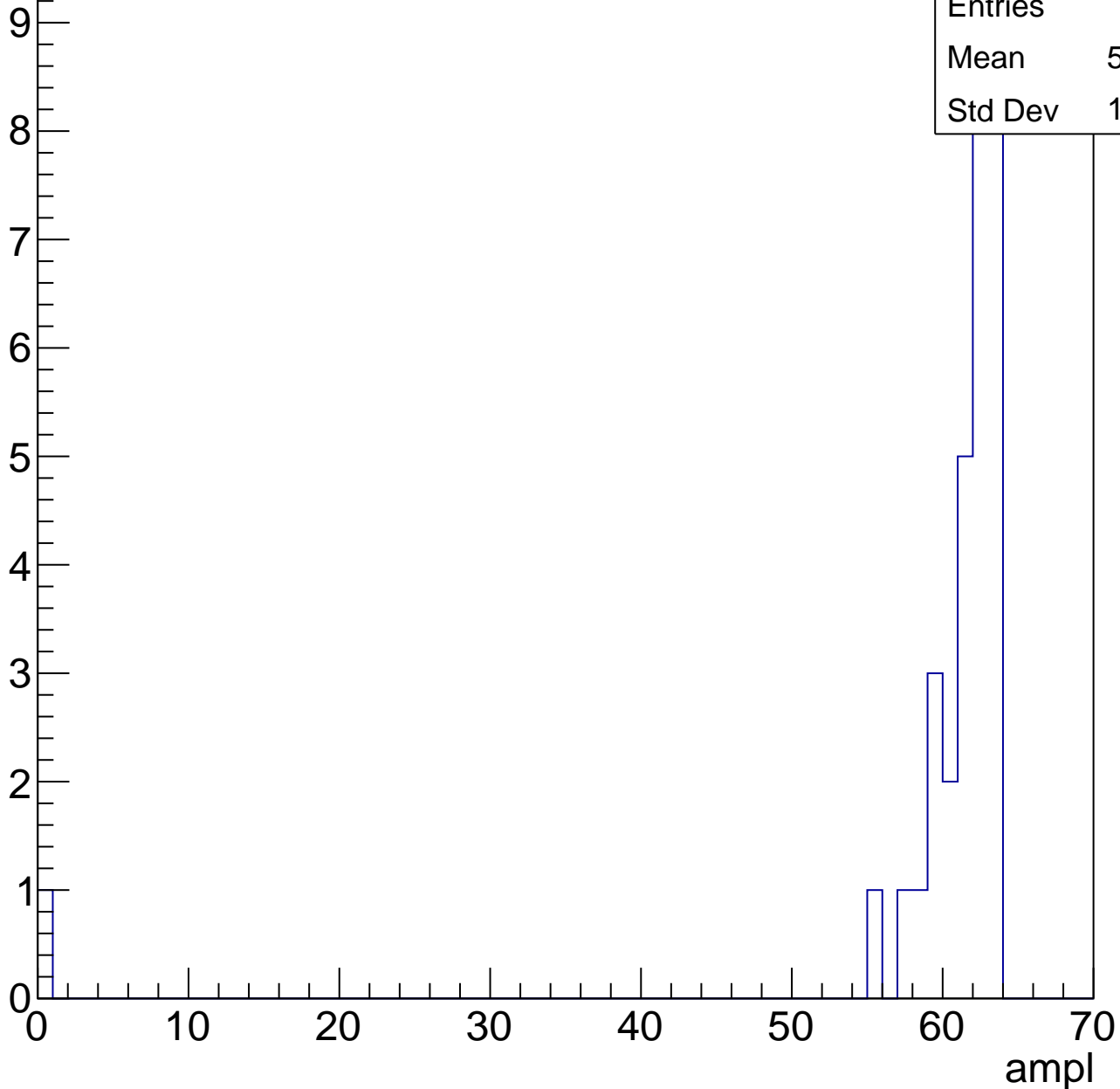


# B1L101S, U11-ch101, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	31
Mean	59.19
Std Dev	10.98



# B1L101S, U11-ch101, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



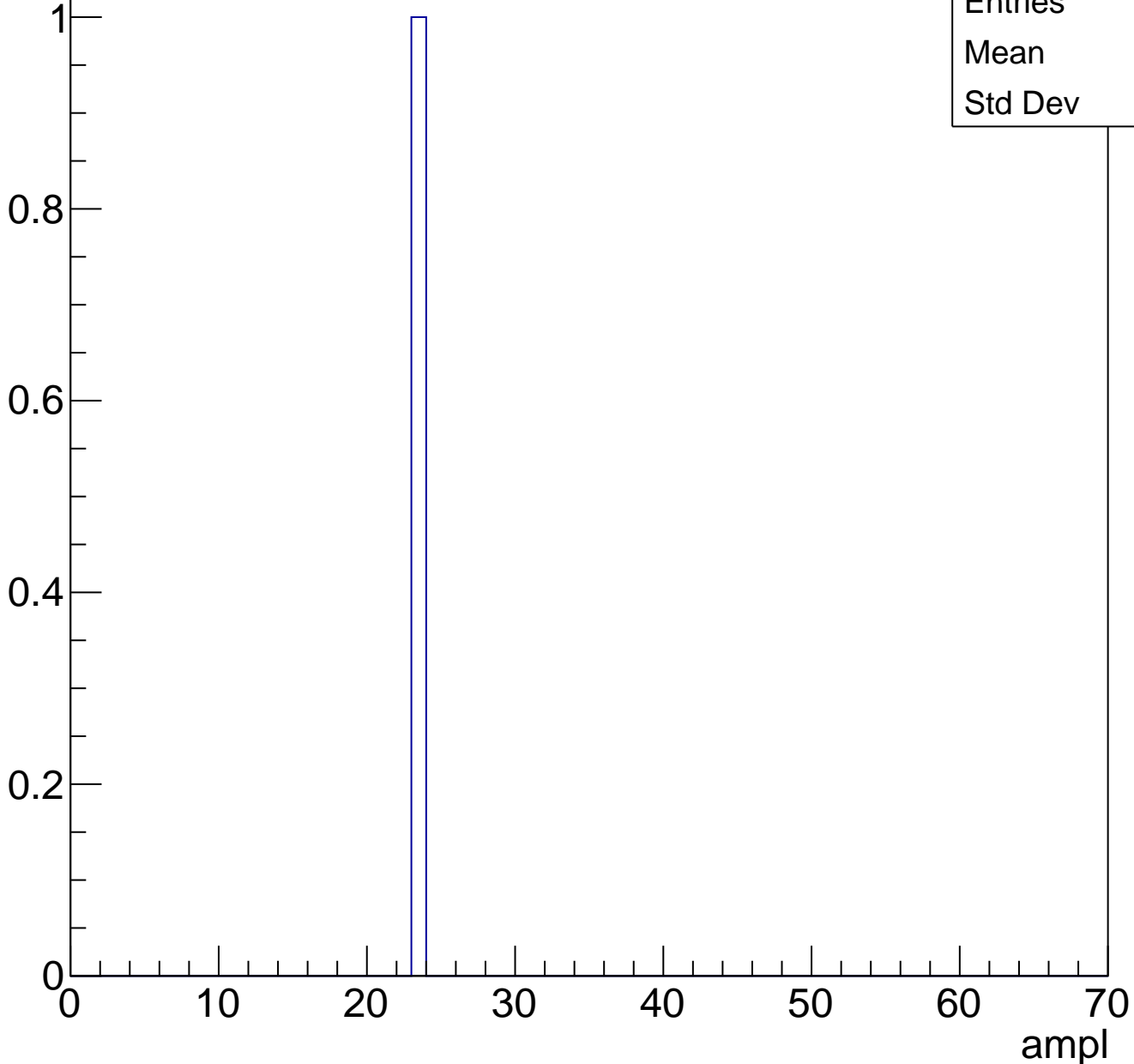
Entries	0
Mean	0
Std Dev	0



# B1L101S, U11-ch101, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	23
Std Dev	0

# B1L101S, U11-ch102, adc0

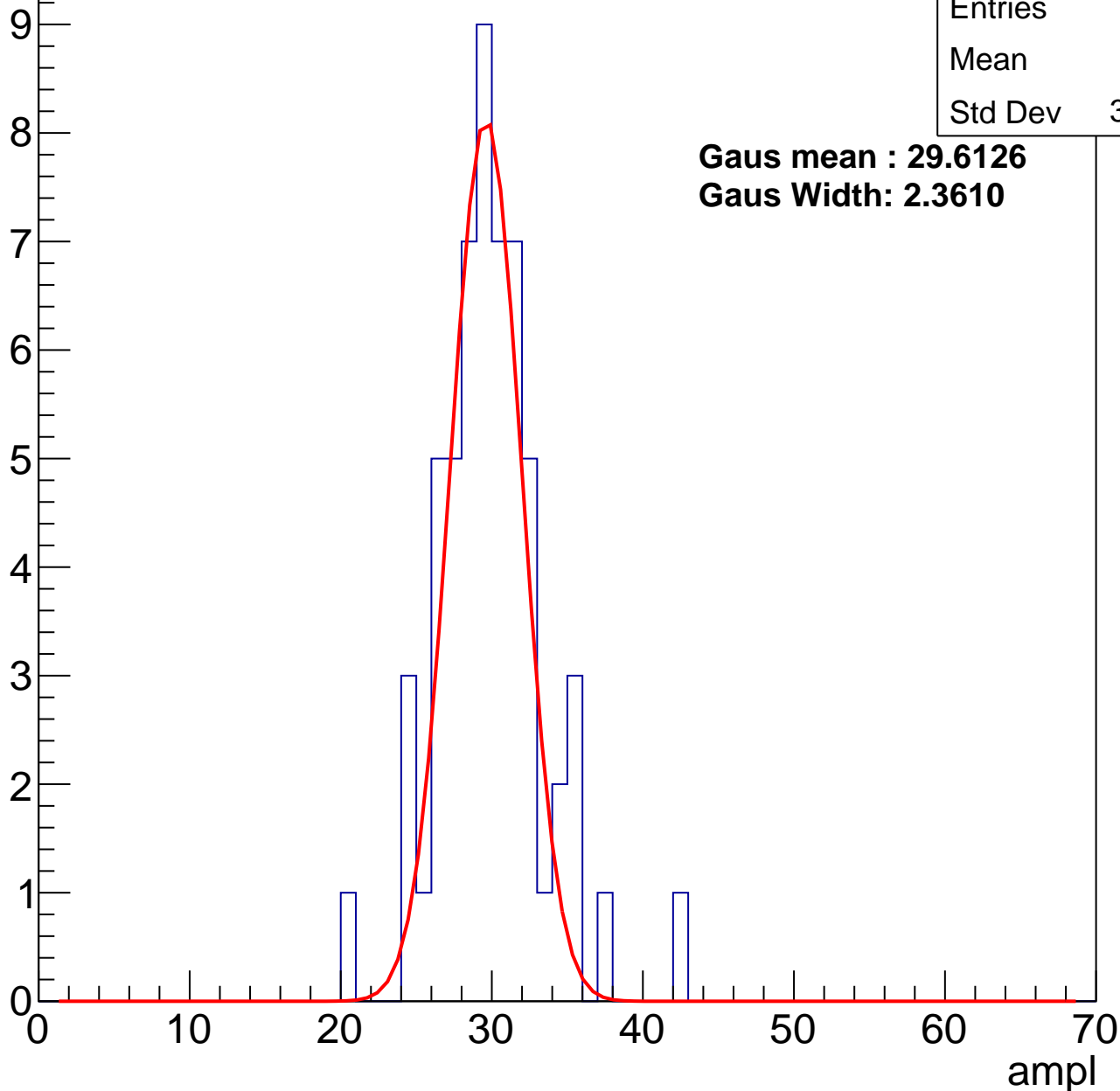
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	29.5
Std Dev	3.515

**Gaus mean : 29.6126**

**Gaus Width: 2.3610**



# B1L101S, U11-ch102, adc1

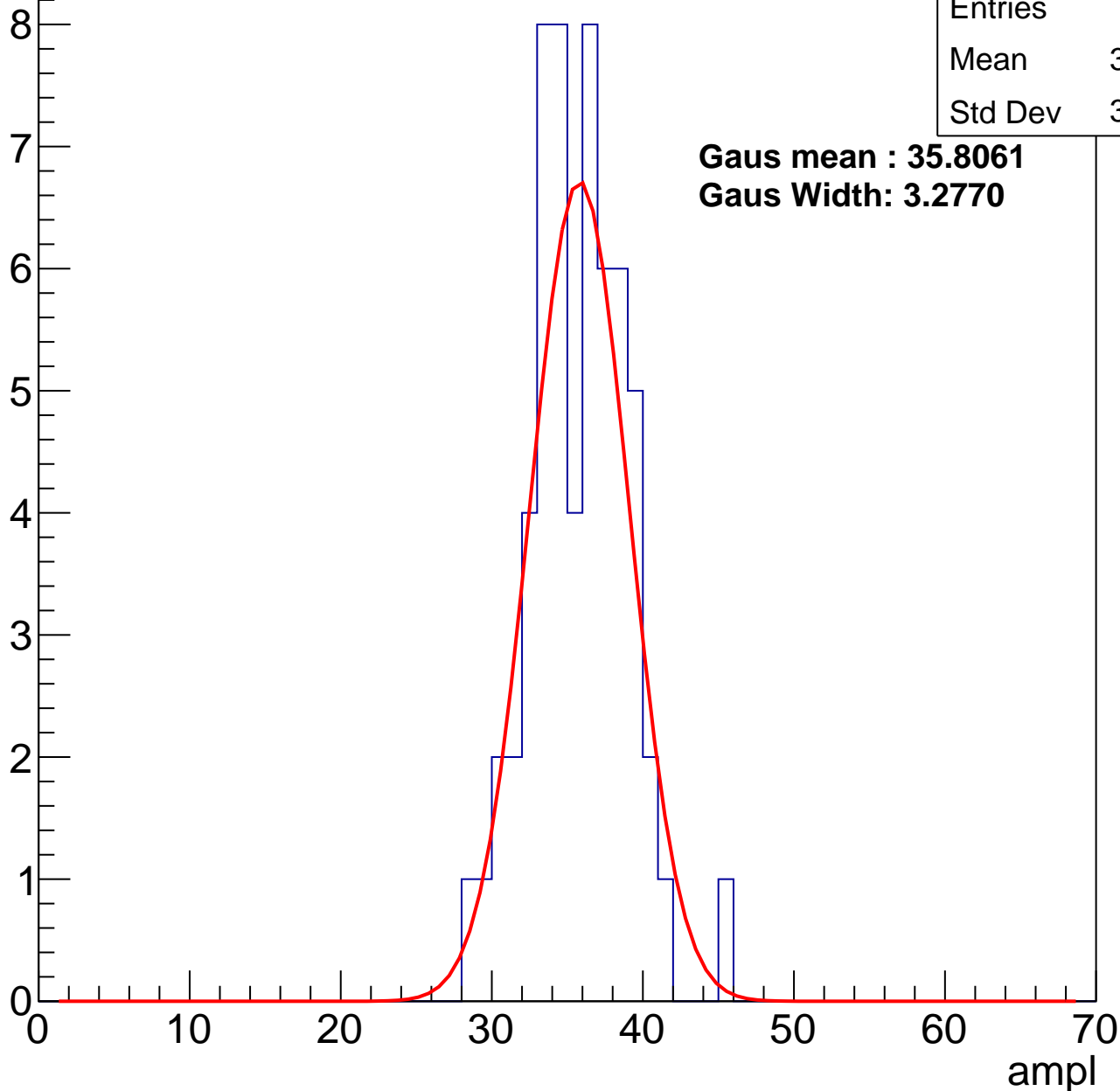
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	35.29
Std Dev	3.163

**Gaus mean : 35.8061**

**Gaus Width: 3.2770**



# B1L101S, U11-ch102, adc2

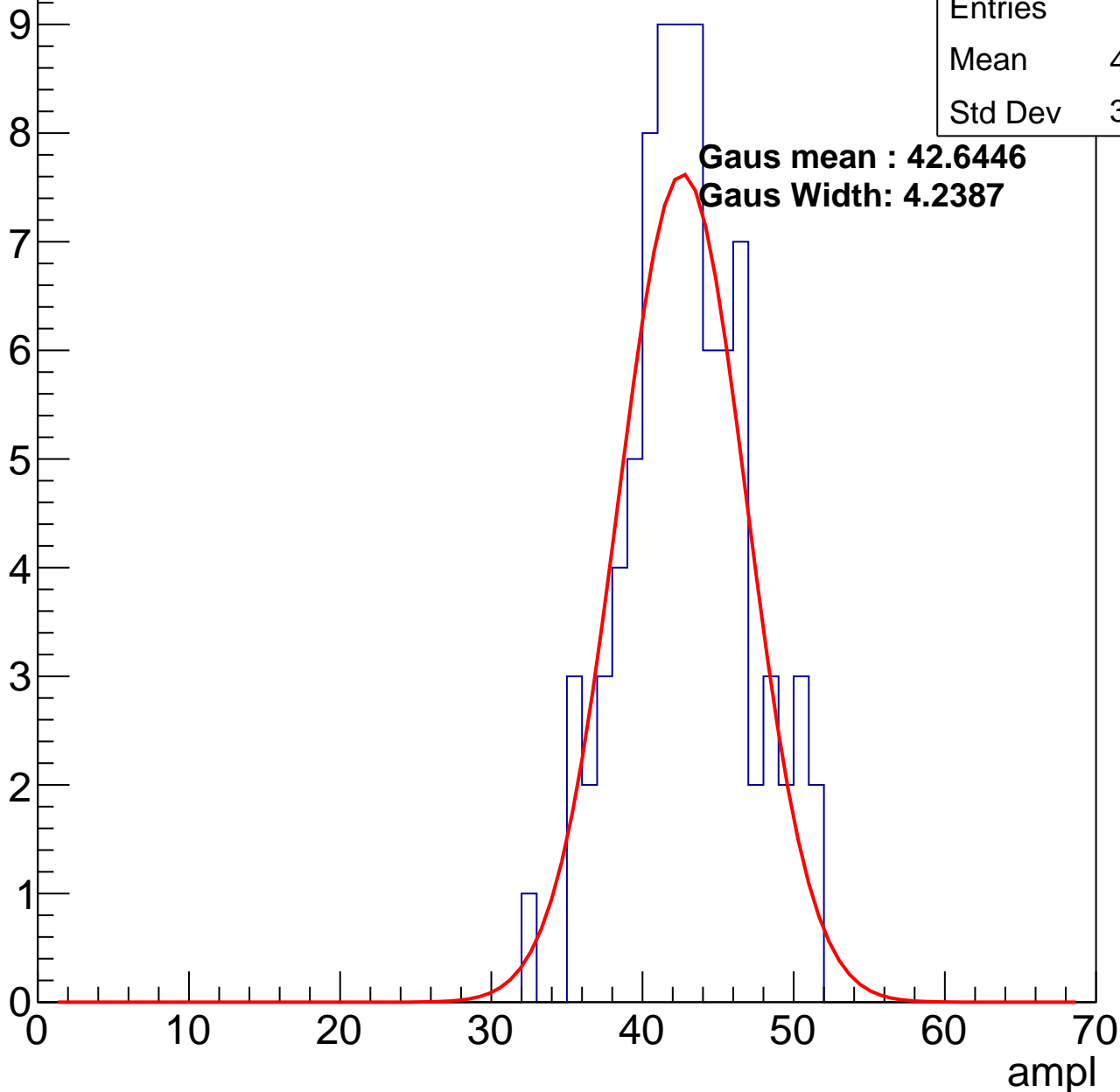
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	84
Mean	42.44
Std Dev	3.989

**Gaus mean : 42.6446**

**Gaus Width: 4.2387**

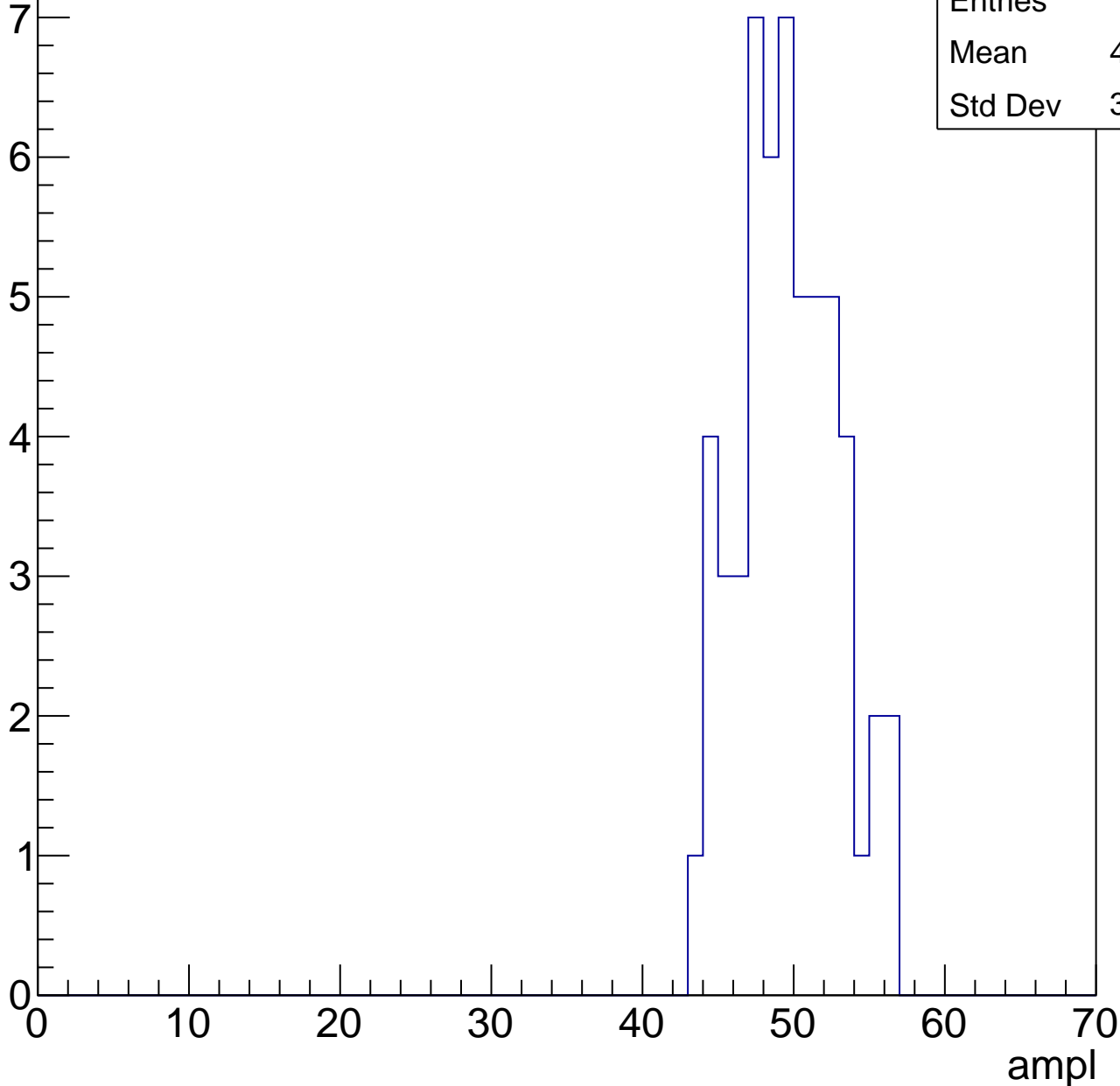


# B1L101S, U11-ch102, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

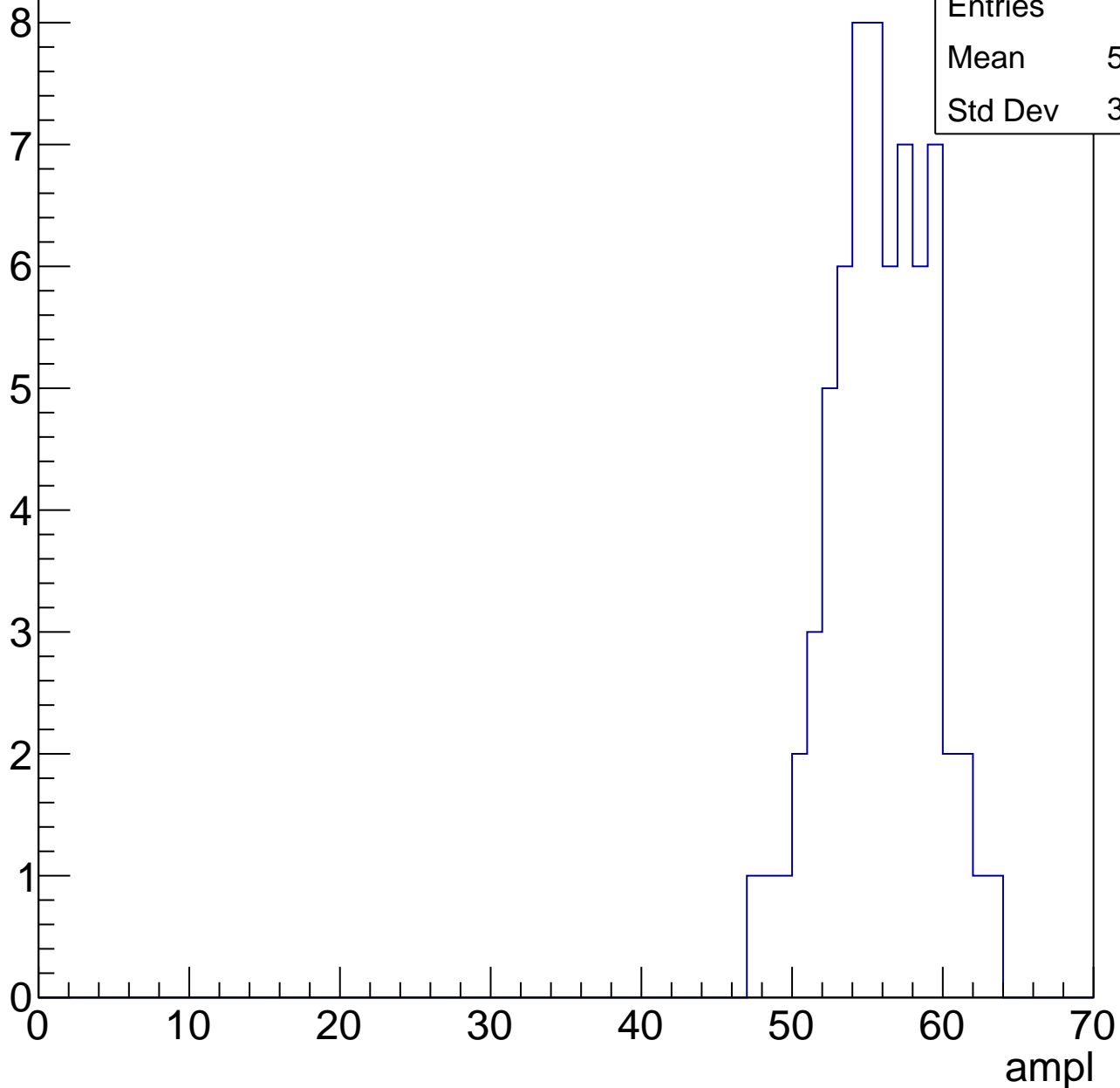
Entries	55
Mean	49.18
Std Dev	3.225



# B1L101S, U11-ch102, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



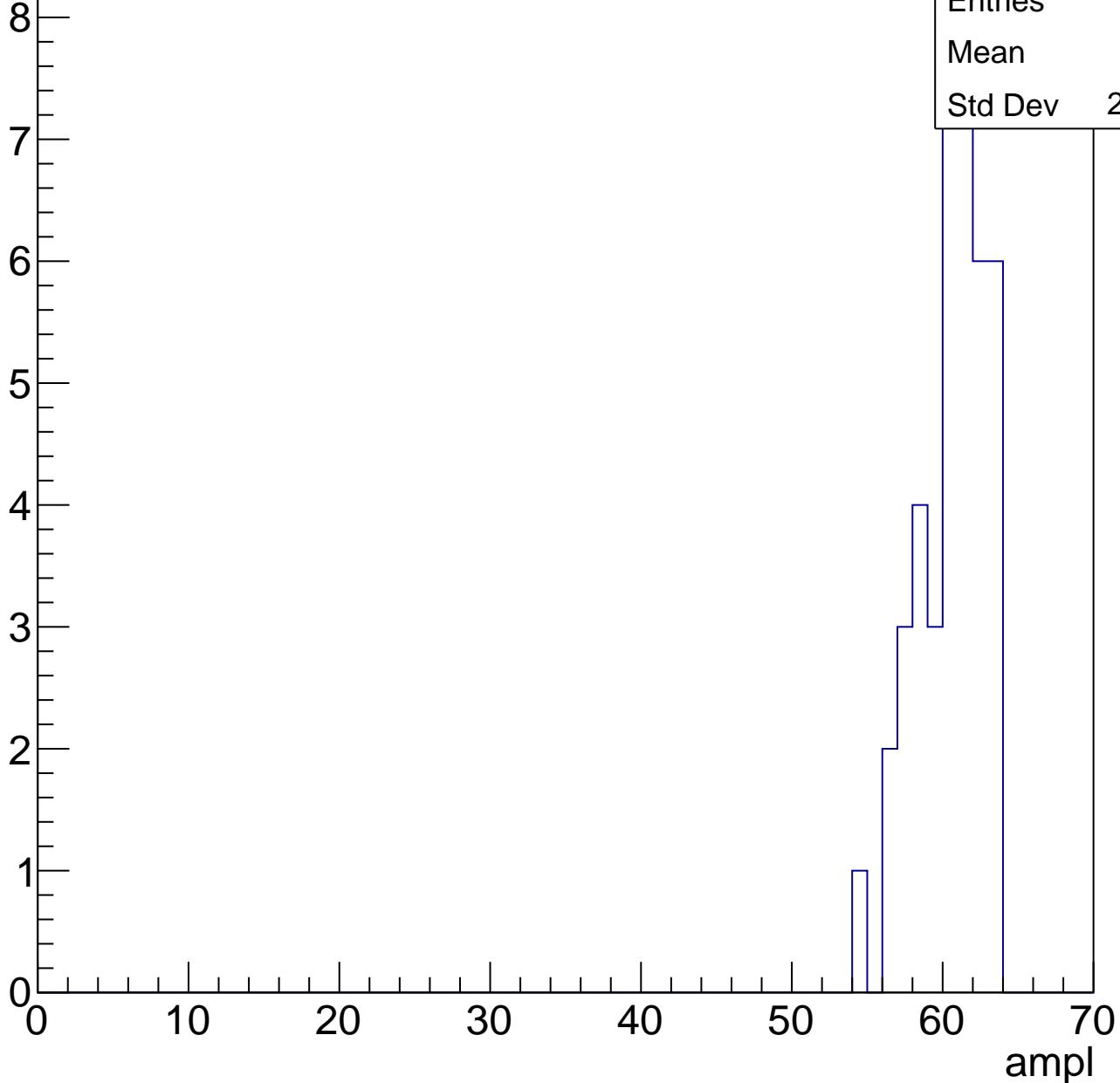
Entries	67
Mean	55.37
Std Dev	3.345

# B1L101S, U11-ch102, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

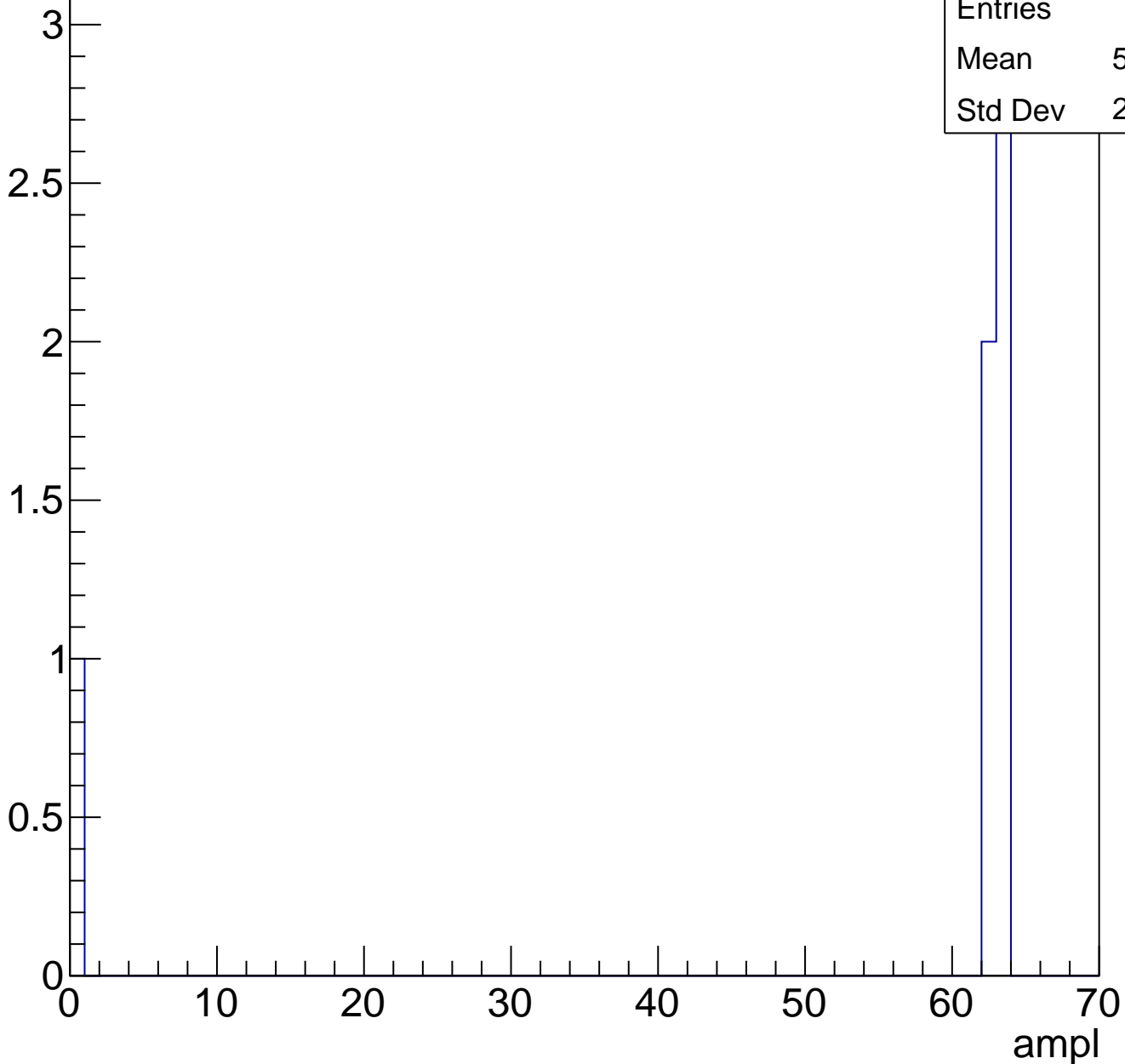
Entries	41
Mean	60.1
Std Dev	2.206



# B1L101S, U11-ch102, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch102, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U11-ch103, adc0

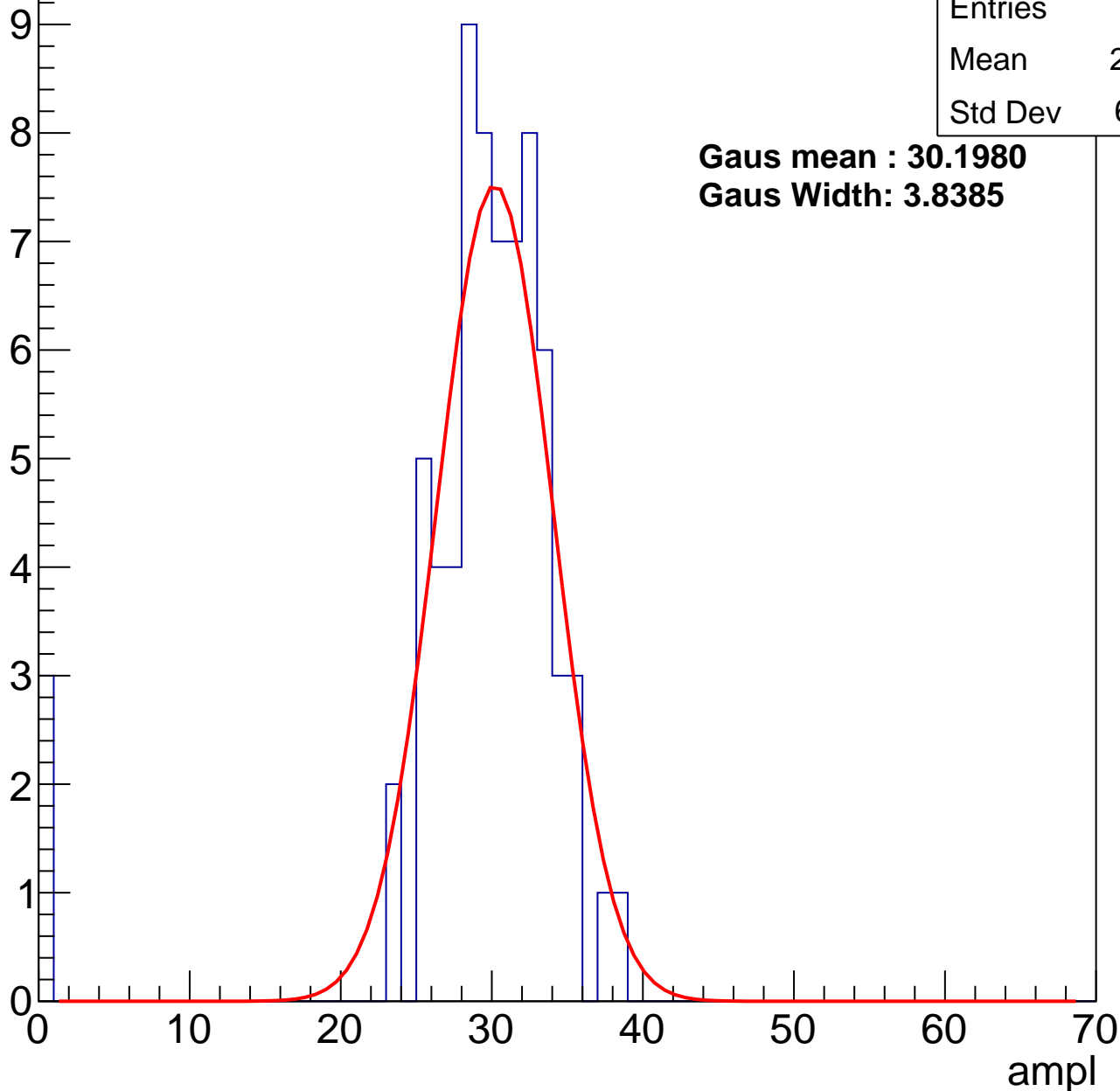
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	28.59
Std Dev	6.771

**Gaus mean : 30.1980**

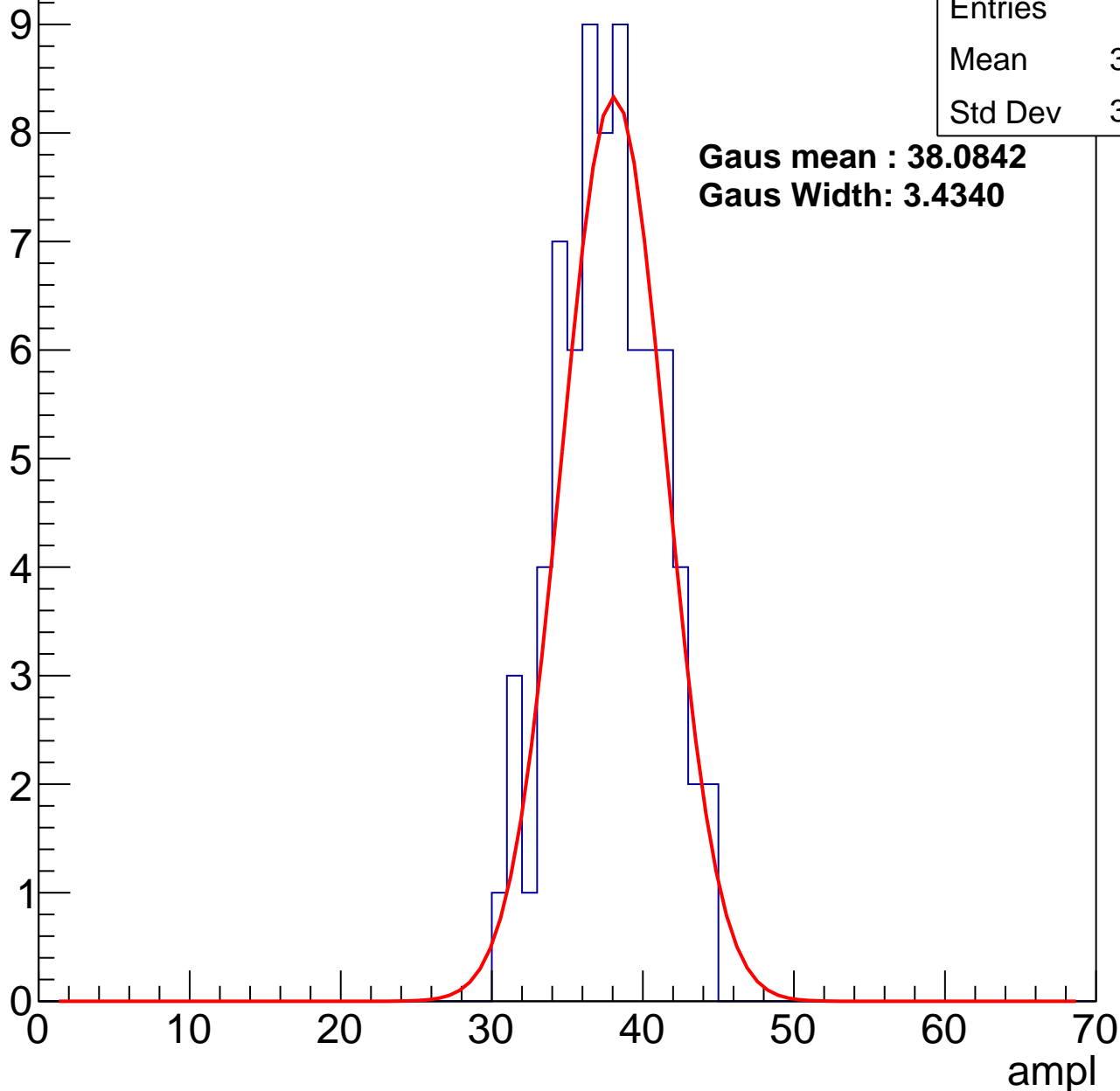
**Gaus Width: 3.8385**



# B1L101S, U11-ch103, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

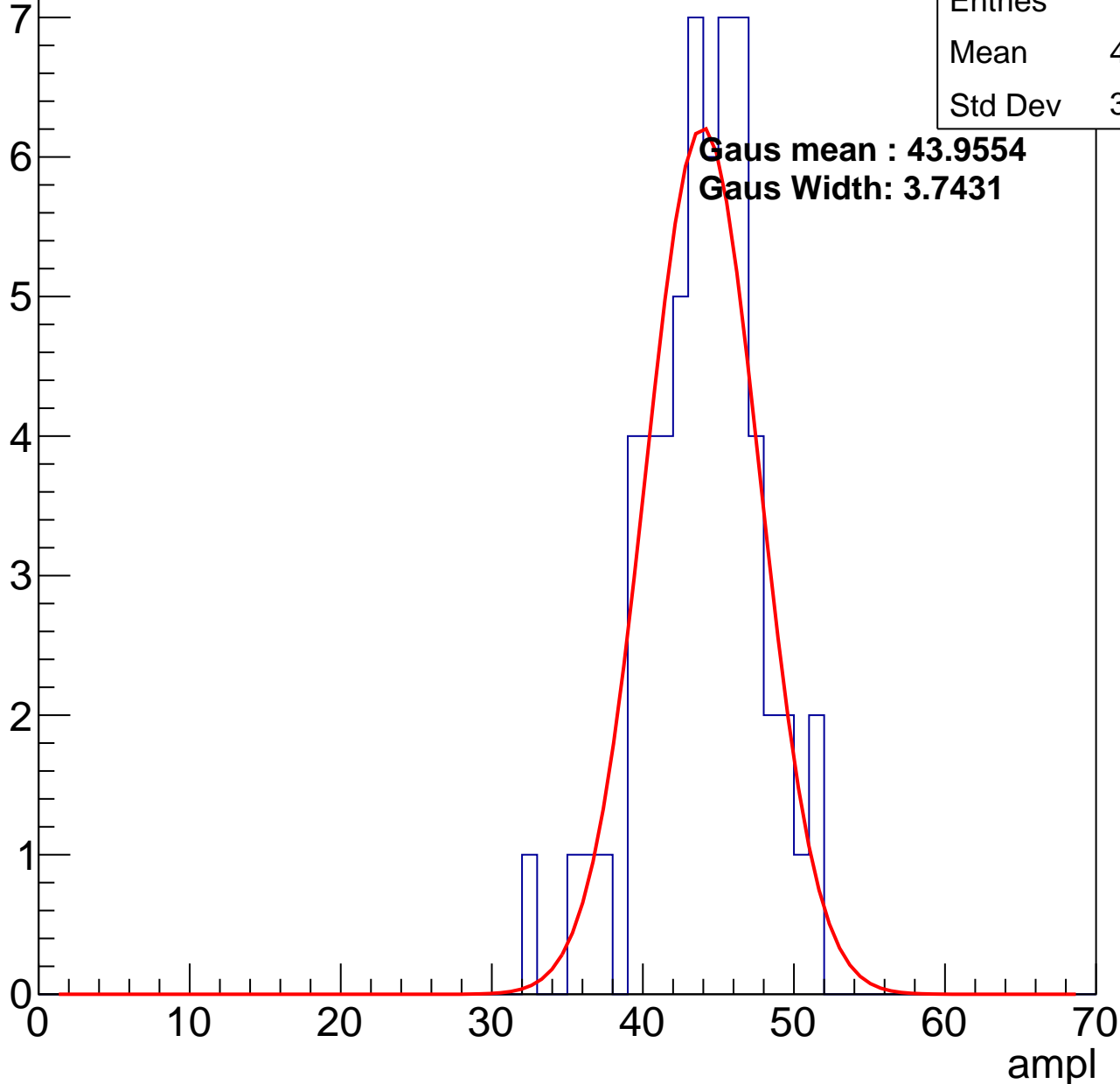


# B1L101S, U11-ch103, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	43.49
Std Dev	3.766



# B1L101S, U11-ch103, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	76
Mean	50.32
Std Dev	3.61

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

ampl

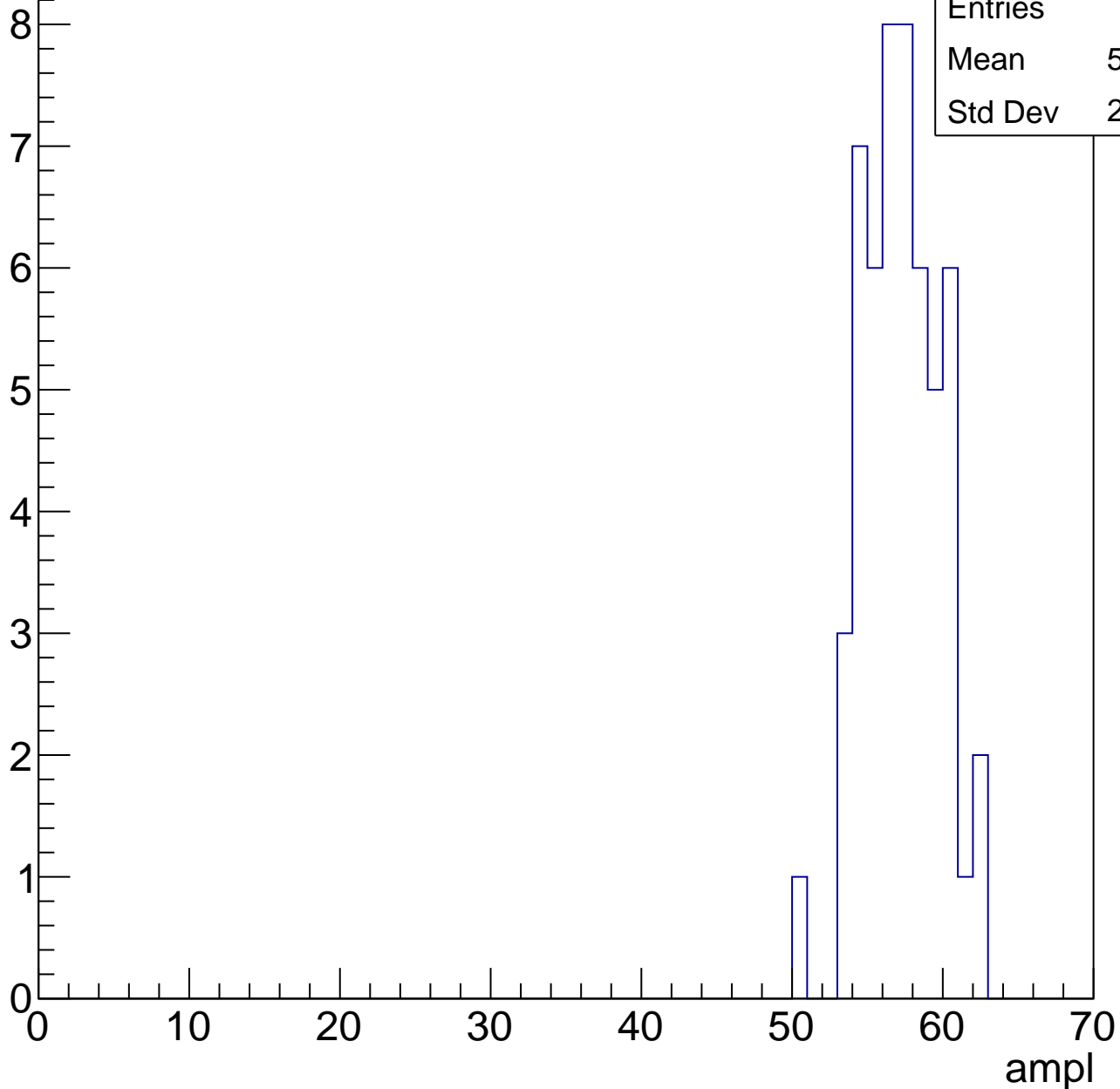
70

# B1L101S, U11-ch103, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	56.77
Std Dev	2.515

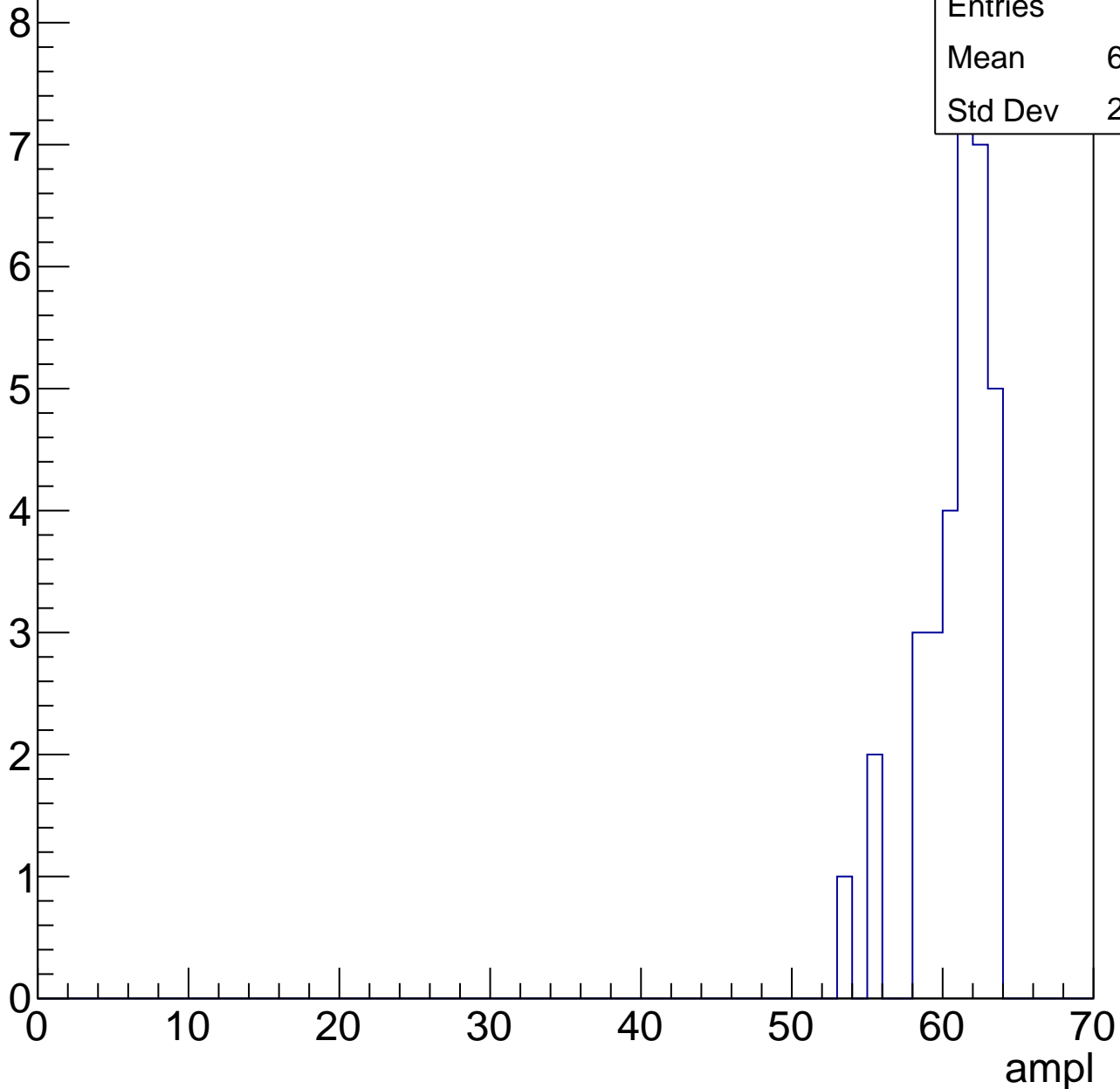


# B1L101S, U11-ch103, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	33
Mean	60.33
Std Dev	2.408

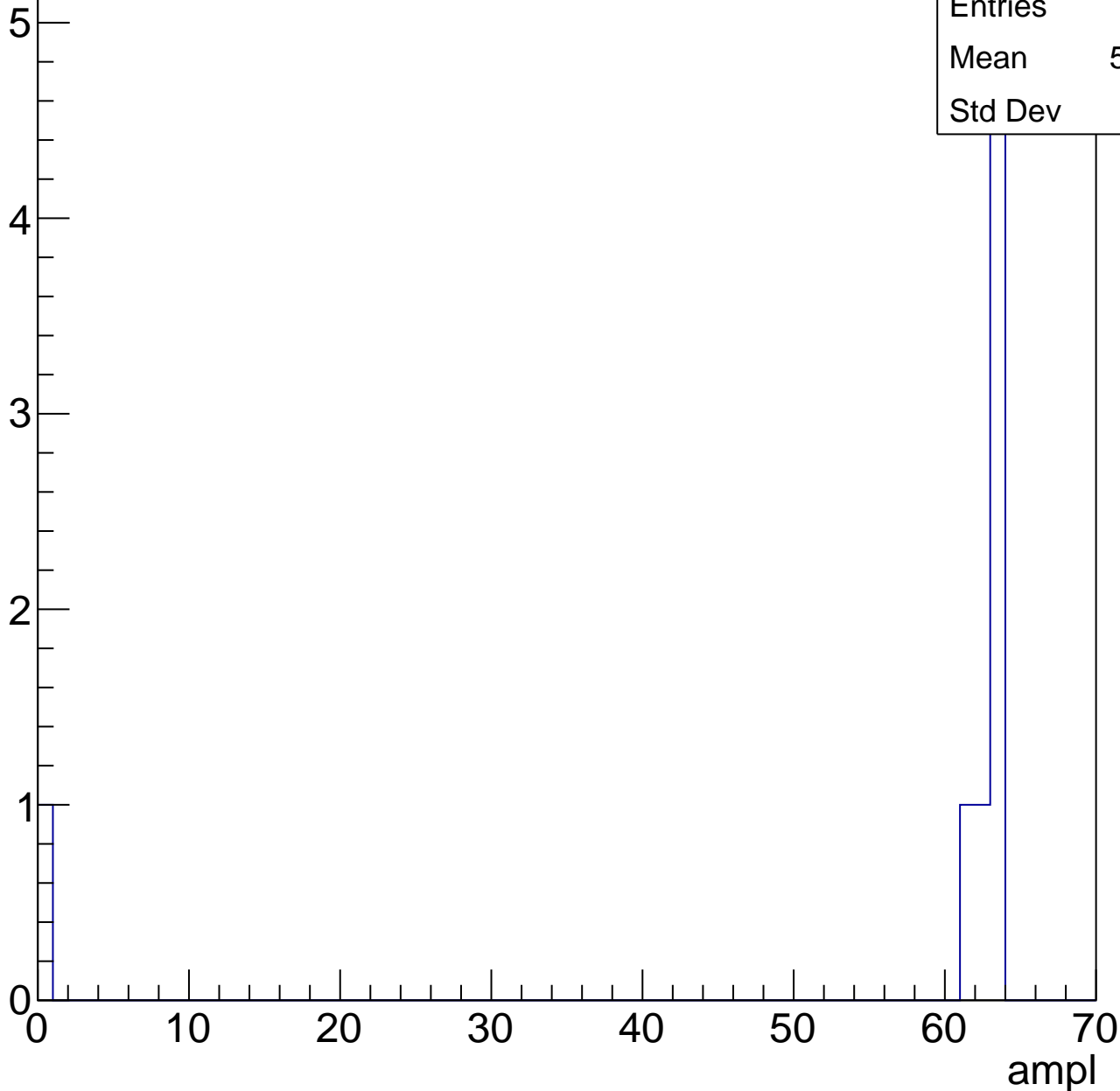


# B1L101S, U11-ch103, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	8
Mean	54.75
Std Dev	20.7

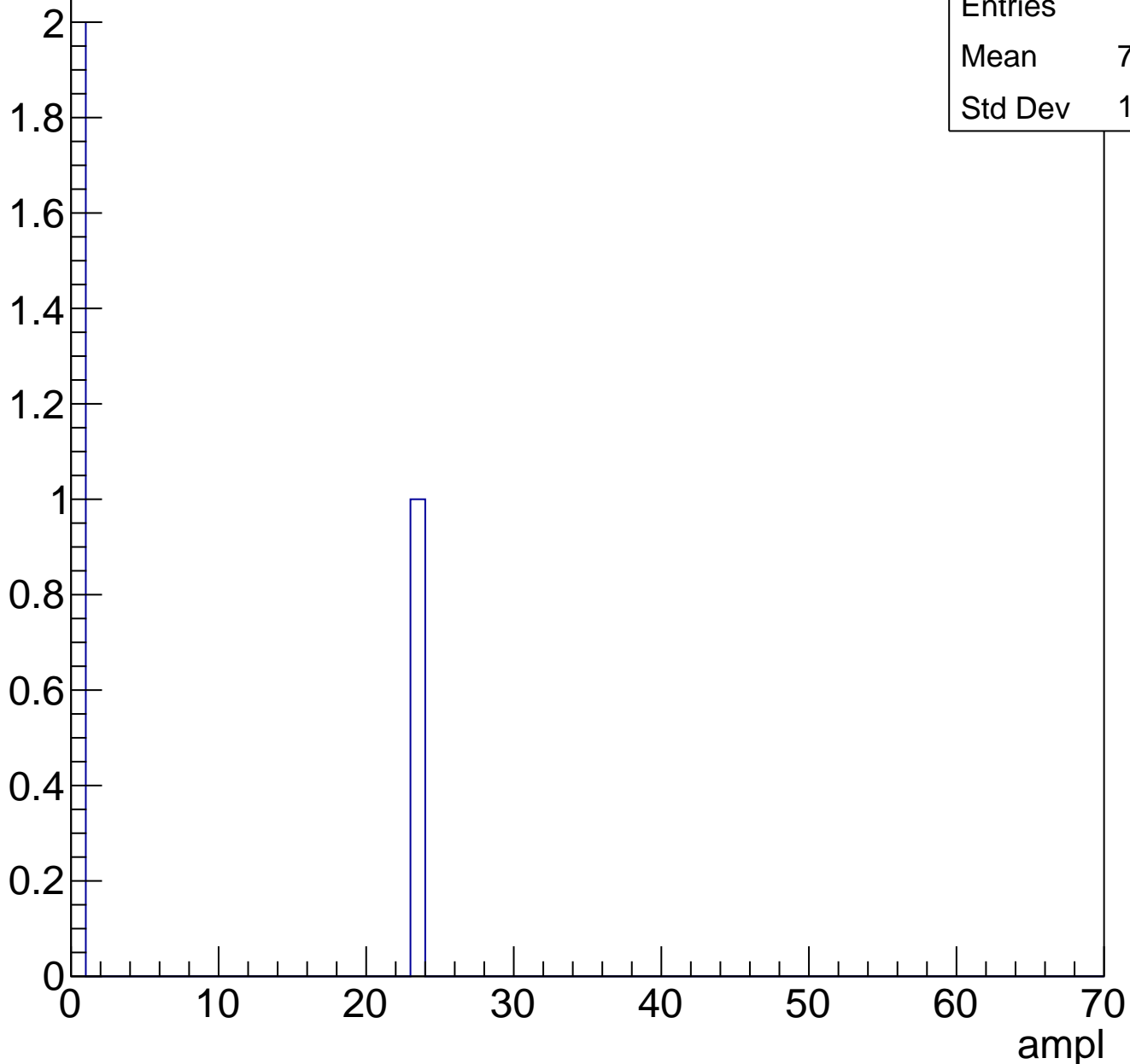




# B1L101S, U11-ch103, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	7.667
Std Dev	10.84

# B1L101S, U11-ch104, adc0

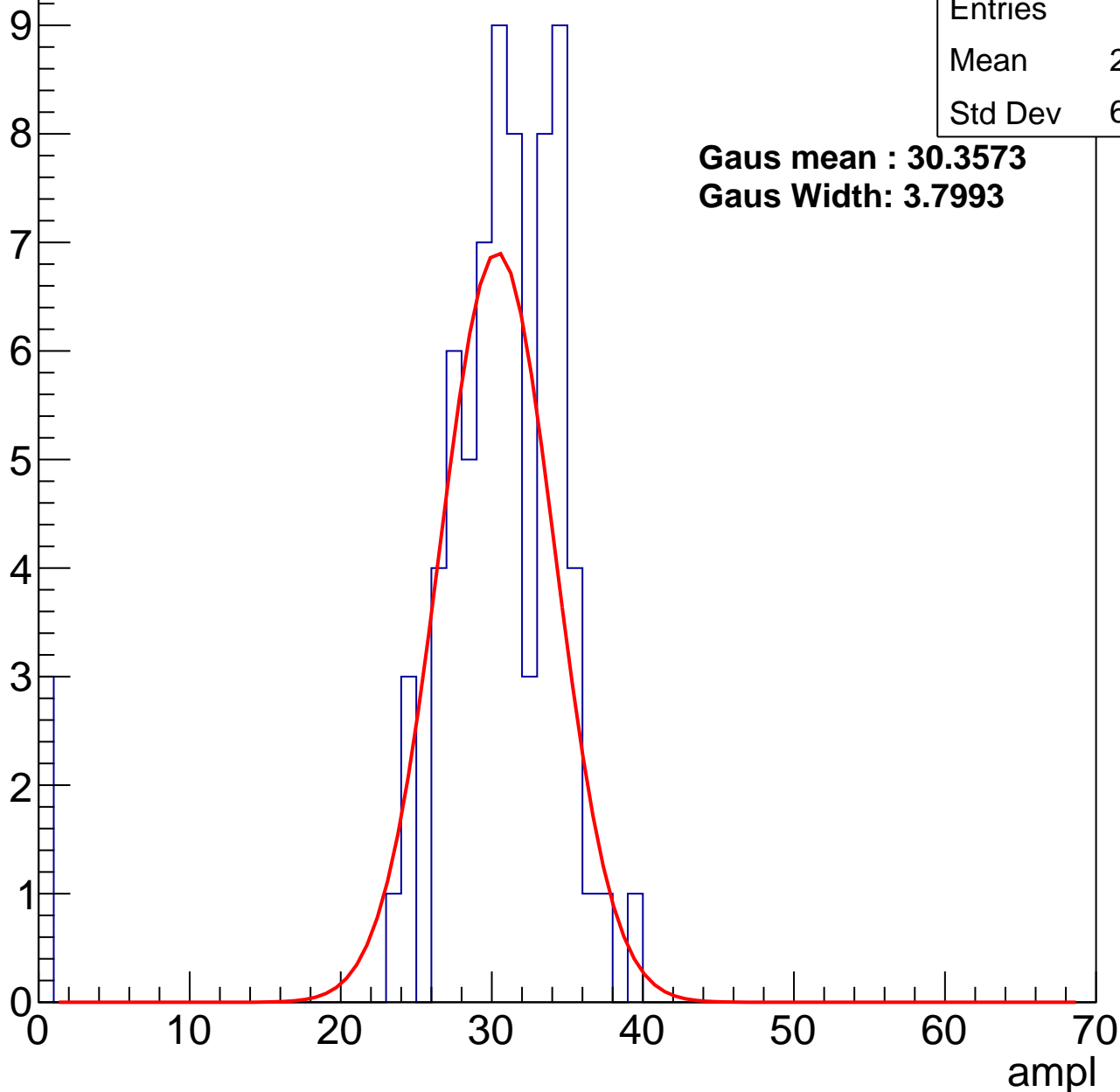
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	29.32
Std Dev	6.894

**Gaus mean : 30.3573**

**Gaus Width: 3.7993**



# B1L101S, U11-ch104, adc1

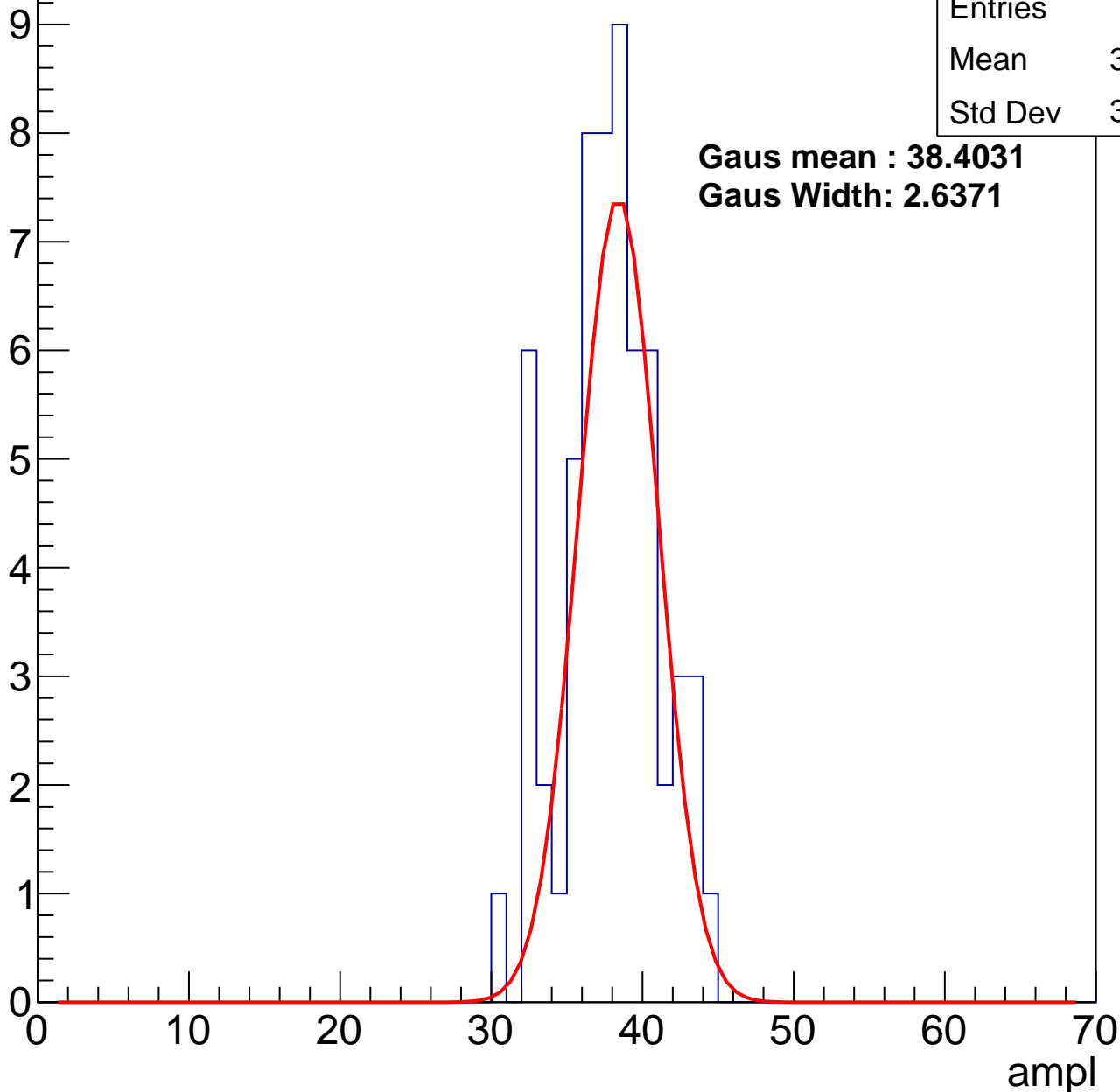
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	37.34
Std Dev	3.167

**Gaus mean : 38.4031**

**Gaus Width: 2.6371**



# B1L101S, U11-ch104, adc2

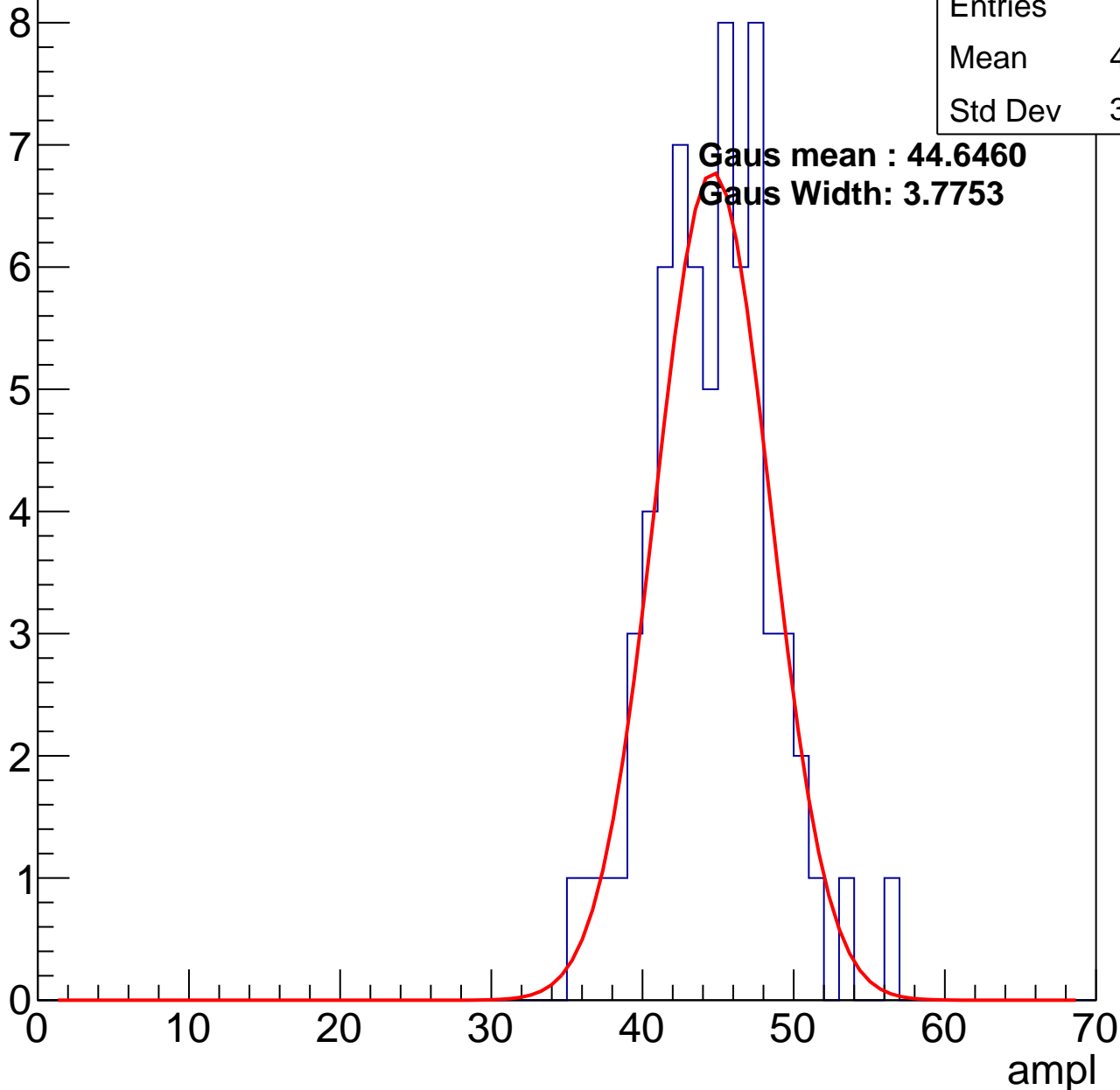
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	44.18
Std Dev	3.888

**Gaus mean : 44.6460**

**Gaus Width: 3.7753**

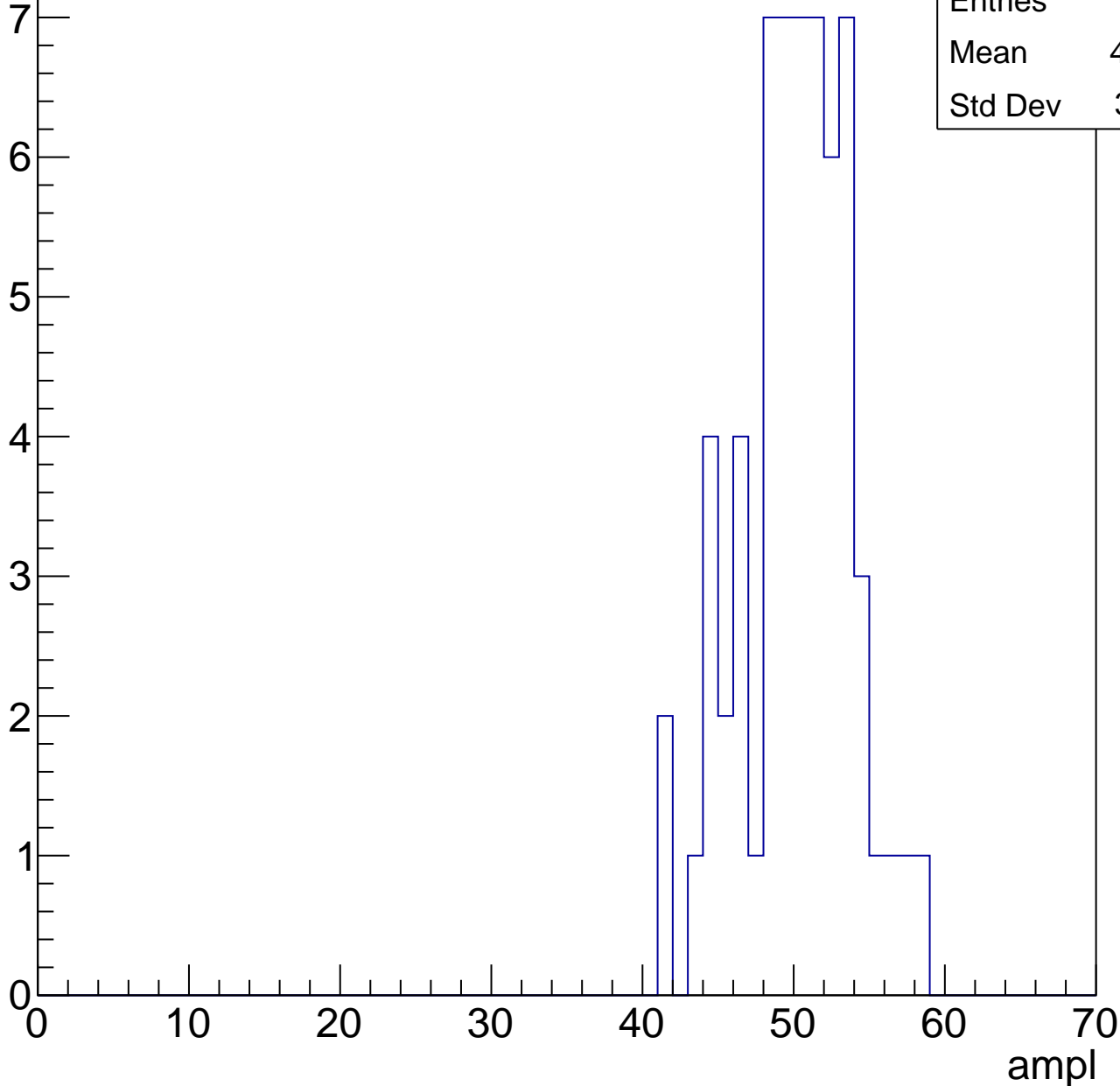


# B1L101S, U11-ch104, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	49.66
Std Dev	3.641

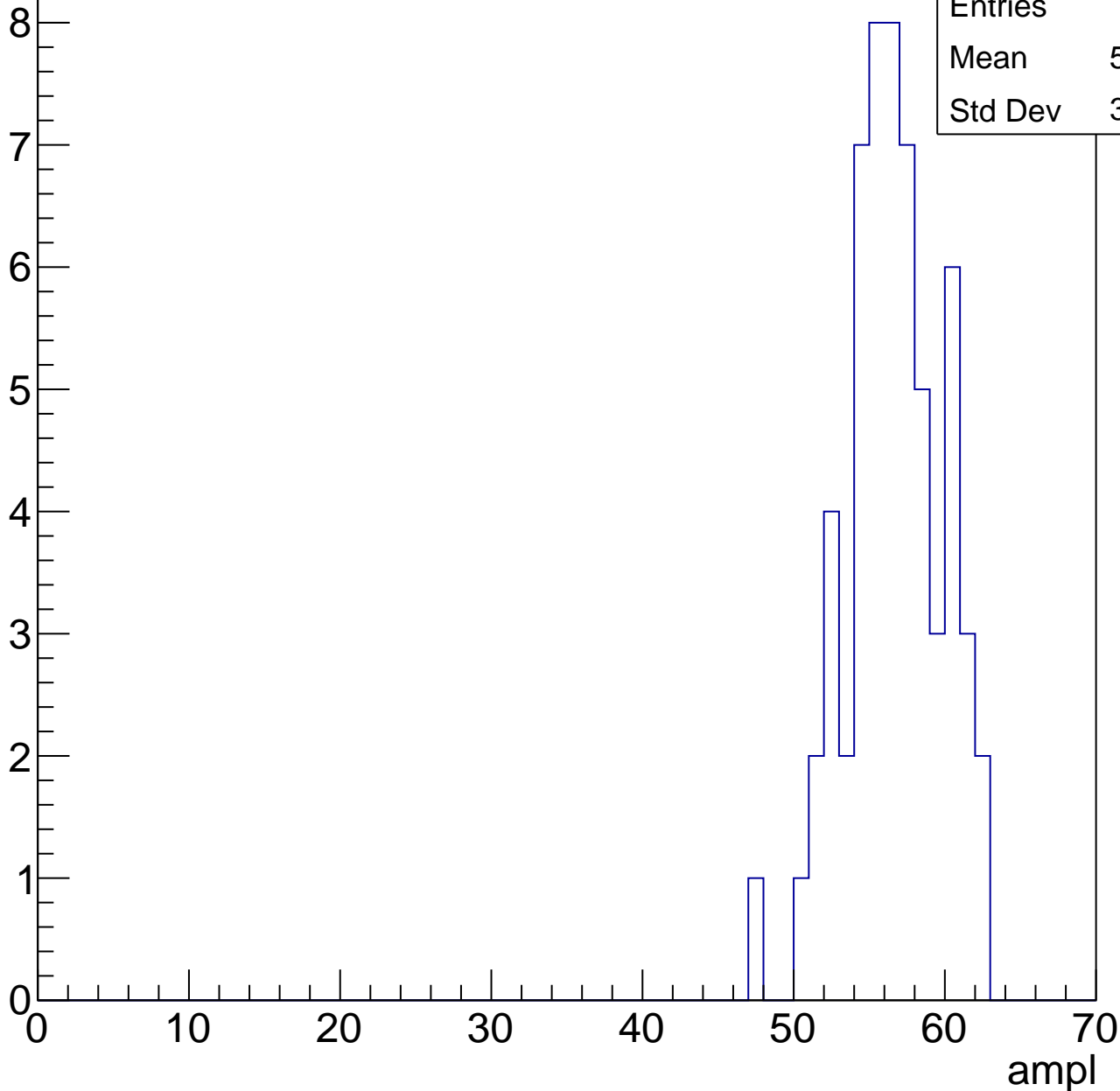


# B1L101S, U11-ch104, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	56.14
Std Dev	3.138

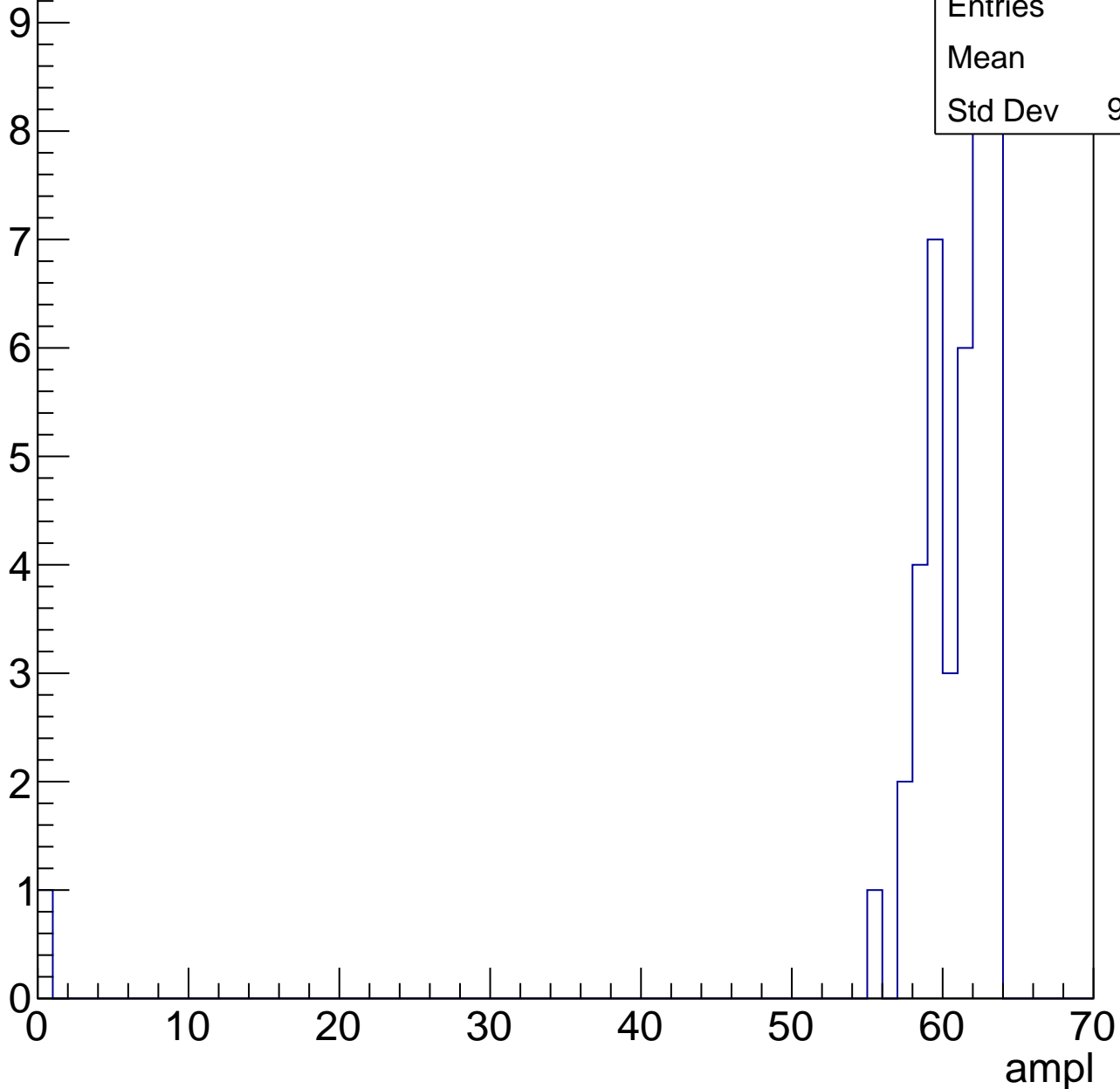


# B1L101S, U11-ch104, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	41
Mean	59.1
Std Dev	9.566



# B1L101S, U11-ch104, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch104, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U11-ch105, adc0

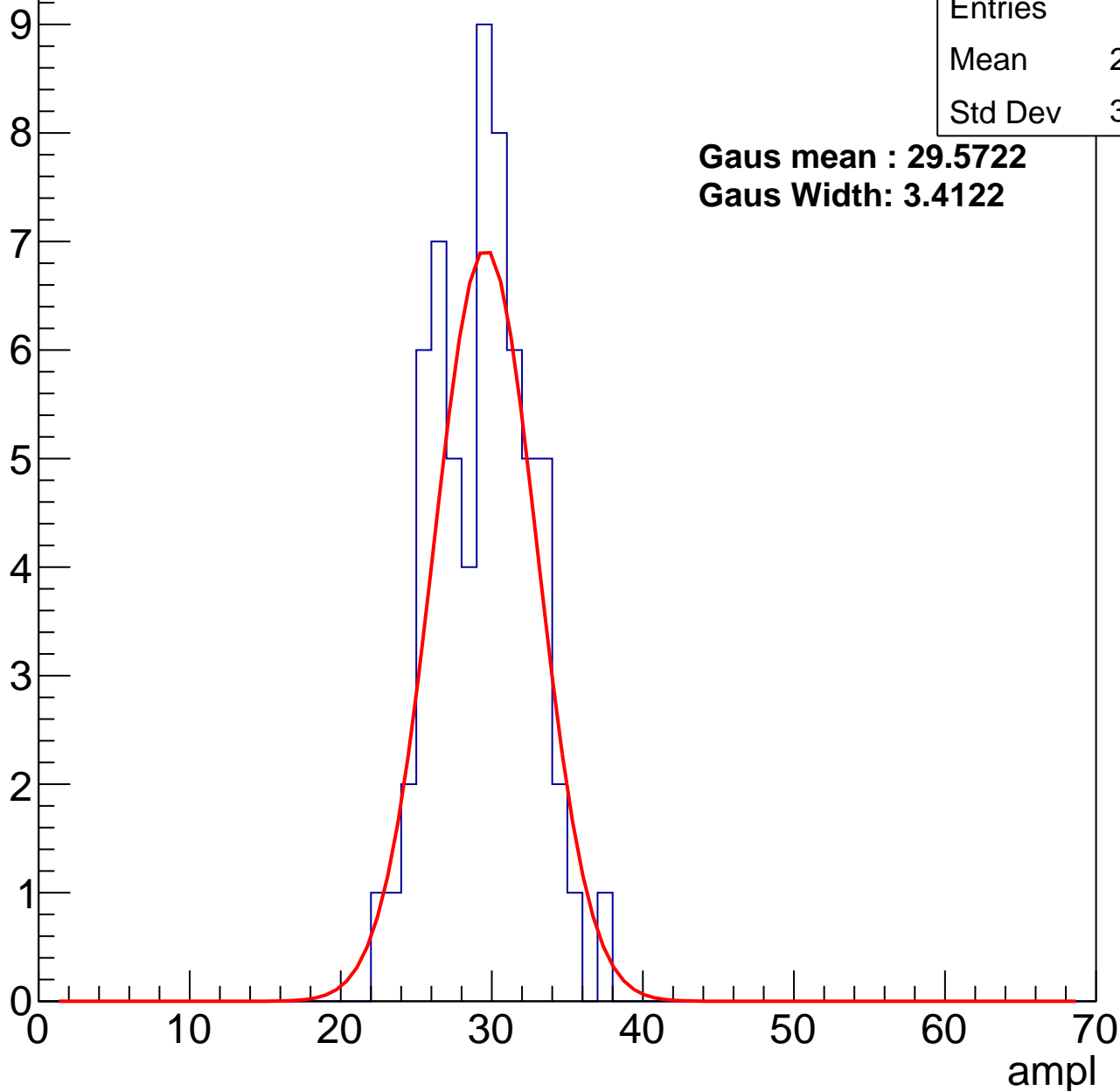
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	28.95
Std Dev	3.149

**Gaus mean : 29.5722**

**Gaus Width: 3.4122**



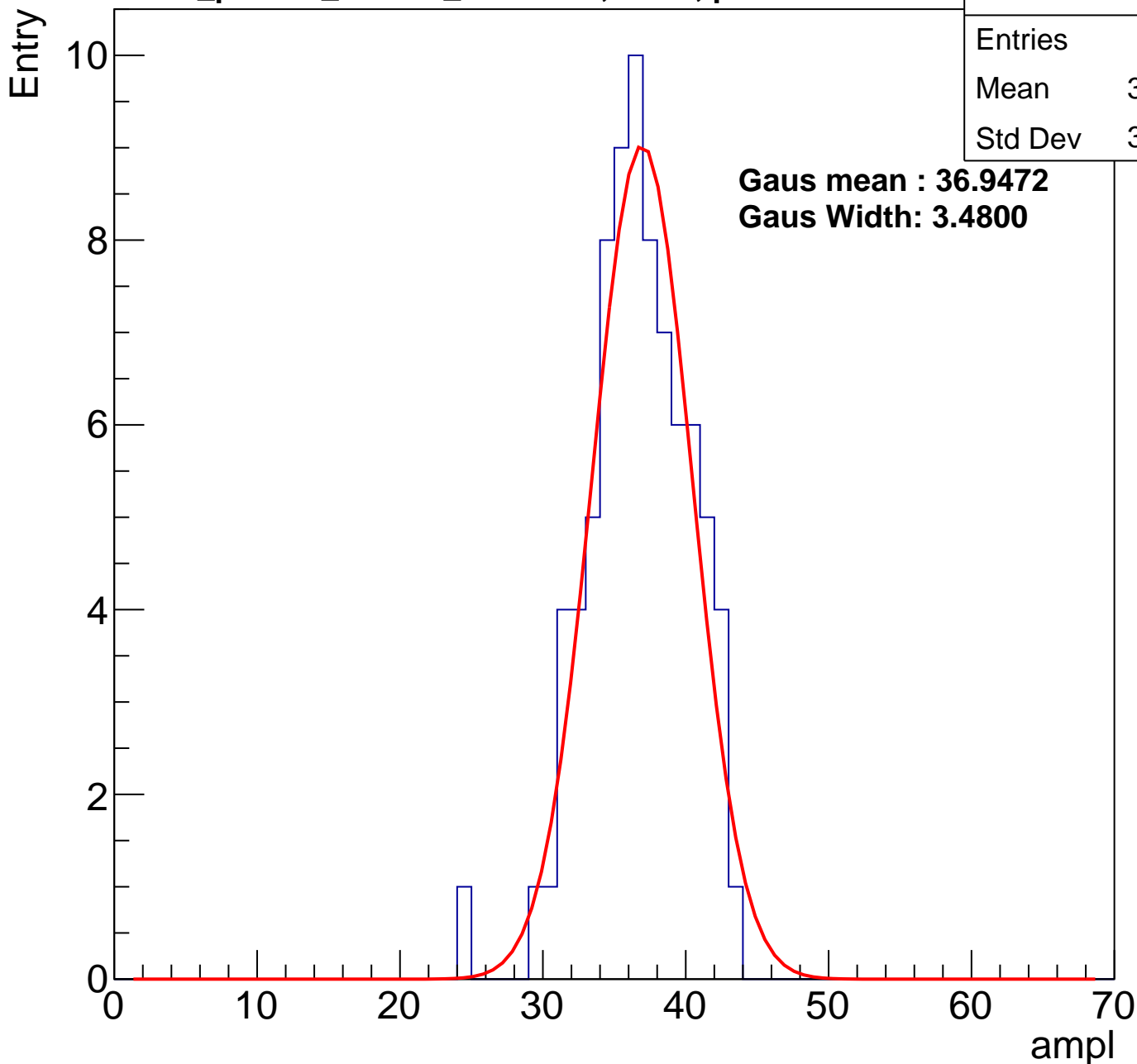
# B1L101S, U11-ch105, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	80
Mean	36.24
Std Dev	3.497

**Gaus mean : 36.9472**

**Gaus Width: 3.4800**



# B1L101S, U11-ch105, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

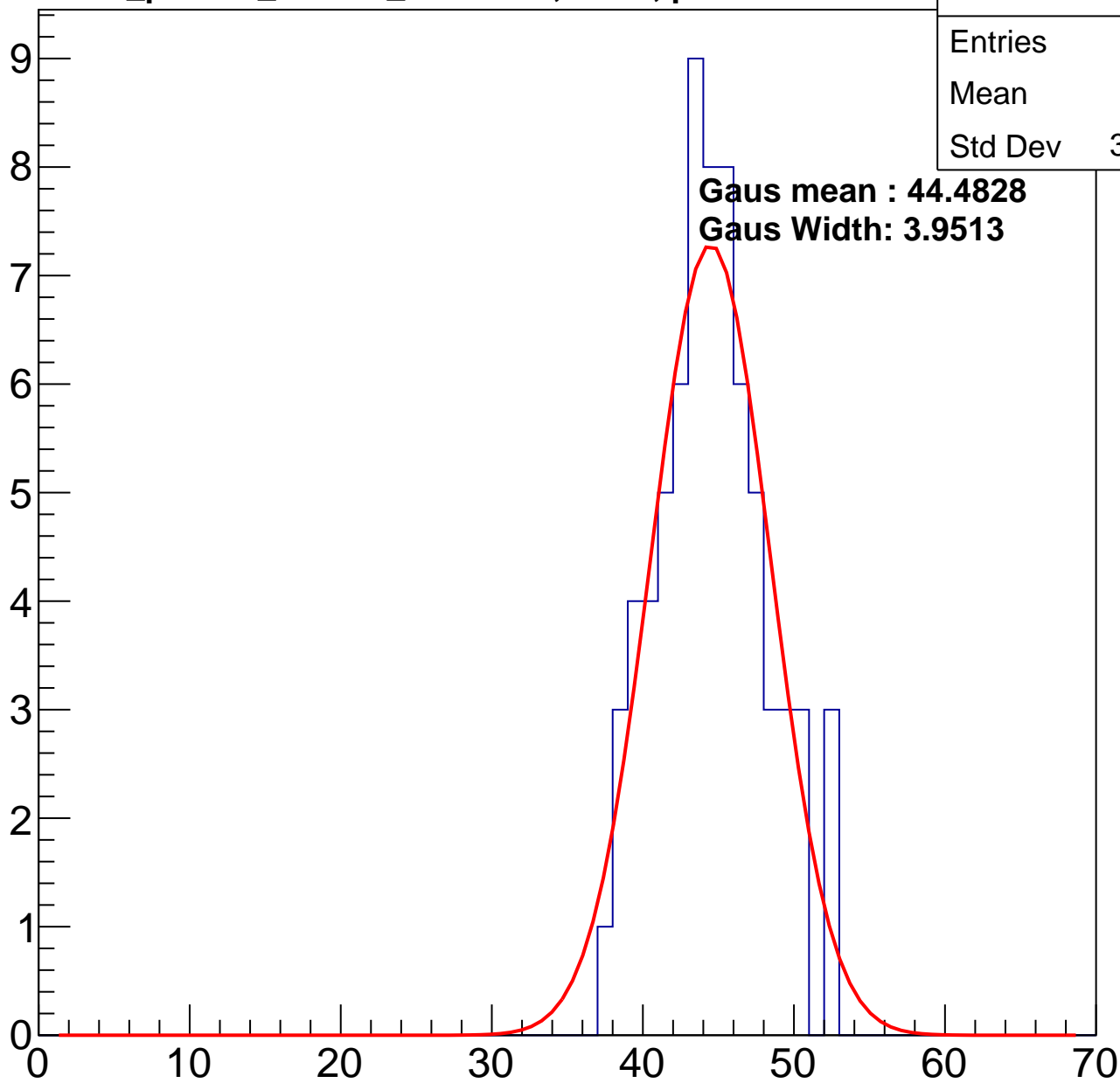
9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	71
Mean	44.1
Std Dev	3.557

**Gaus mean : 44.4828**

**Gaus Width: 3.9513**

ampl

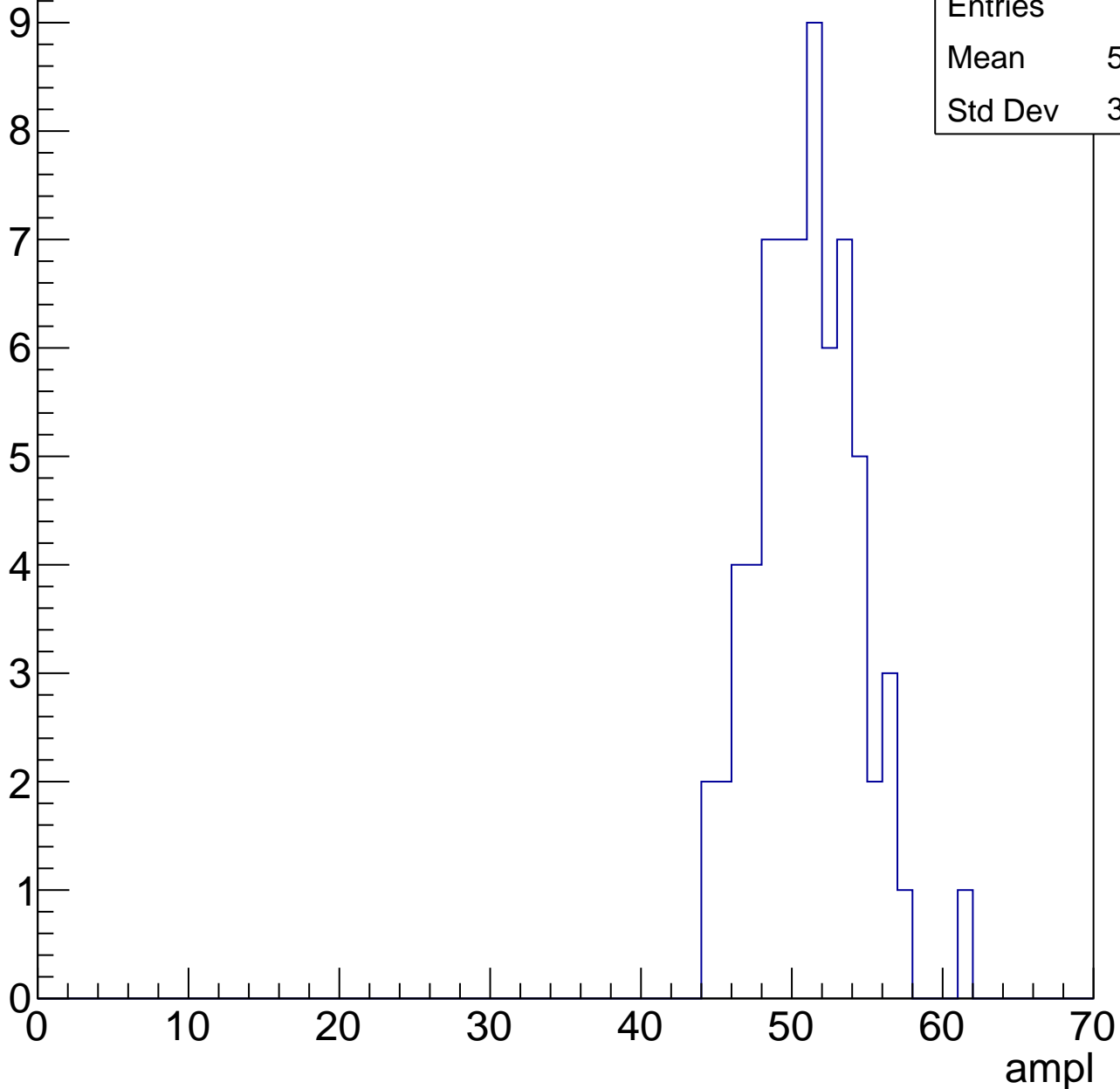


# B1L101S, U11-ch105, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	50.55
Std Dev	3.325

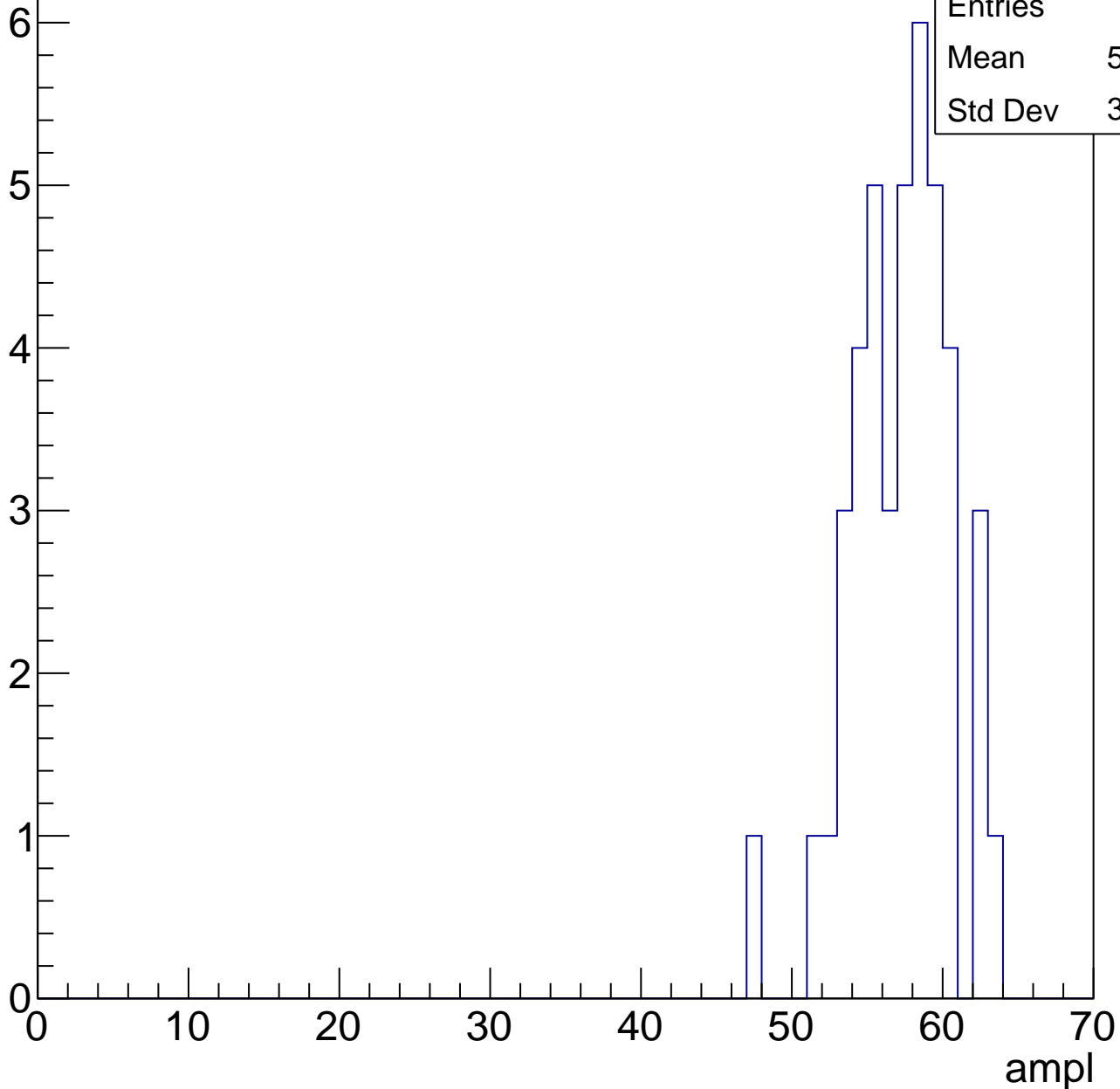


# B1L101S, U11-ch105, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	42
Mean	56.79
Std Dev	3.233

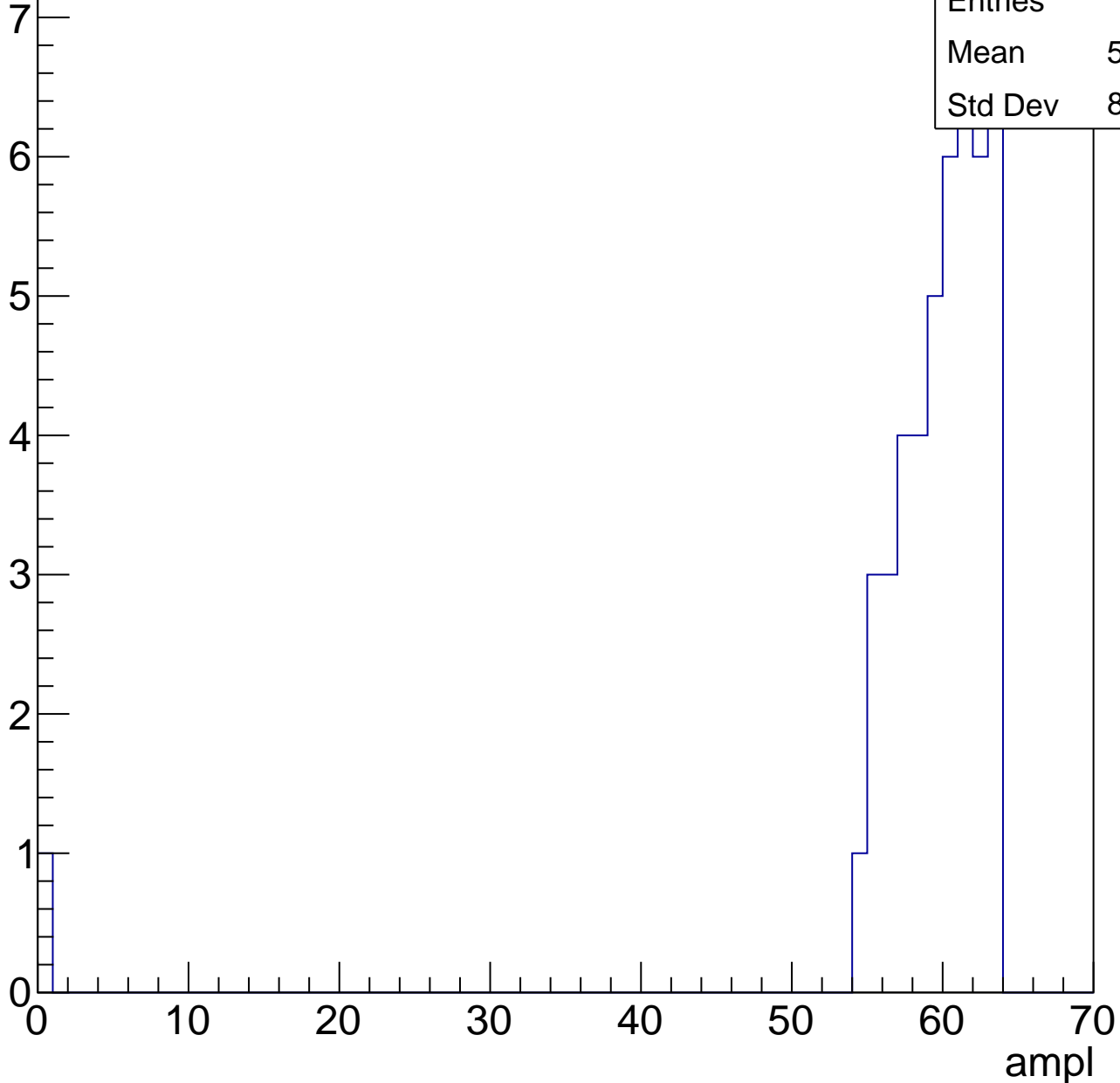


# B1L101S, U11-ch105, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

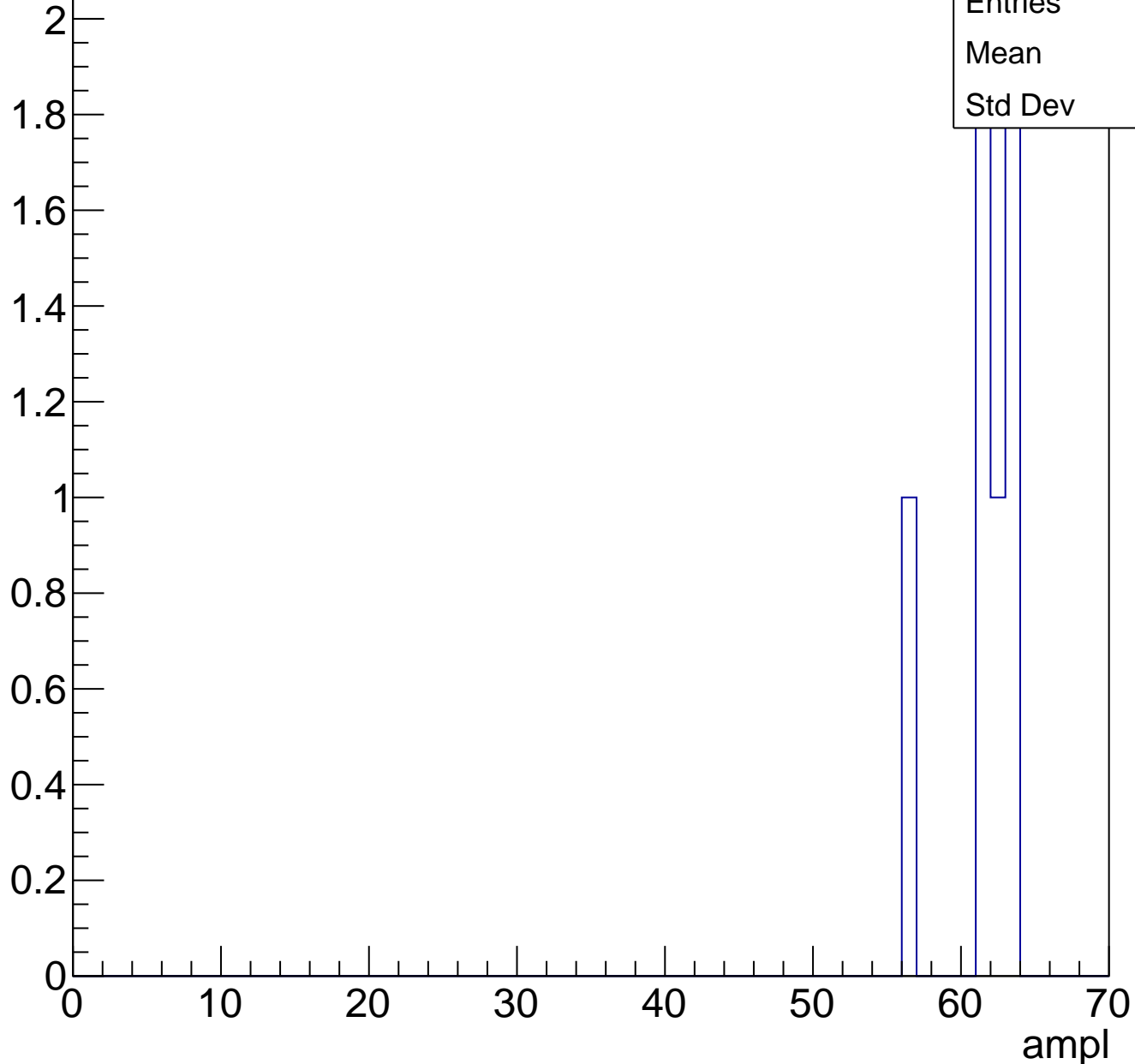
Entries	47
Mean	58.34
Std Dev	8.969



# B1L101S, U11-ch105, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch105, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U11-ch106, adc0

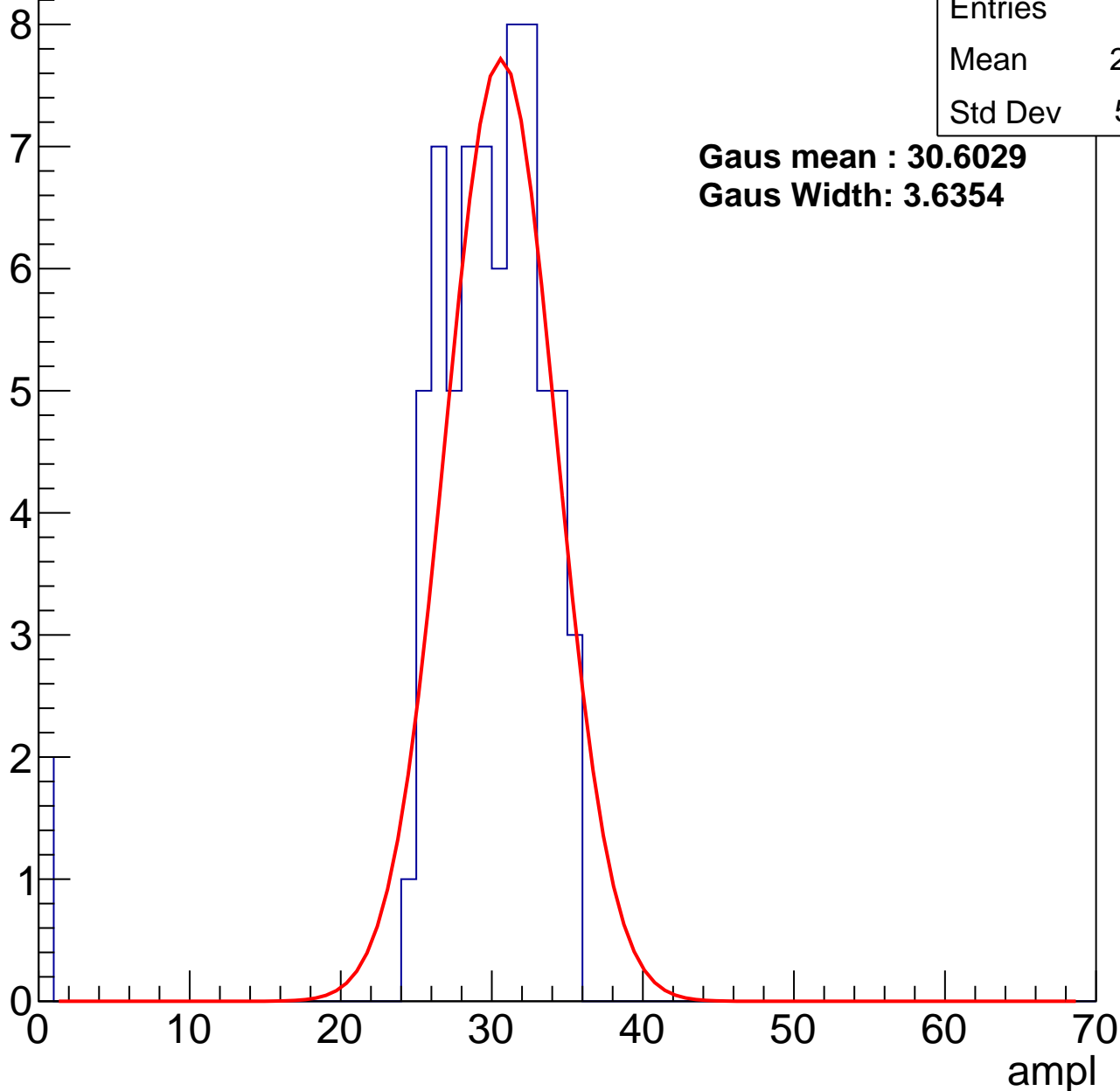
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	28.83
Std Dev	5.771

**Gaus mean : 30.6029**

**Gaus Width: 3.6354**



# B1L101S, U11-ch106, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	77
Mean	37.12
Std Dev	3.35

**Gaus mean : 37.9048**

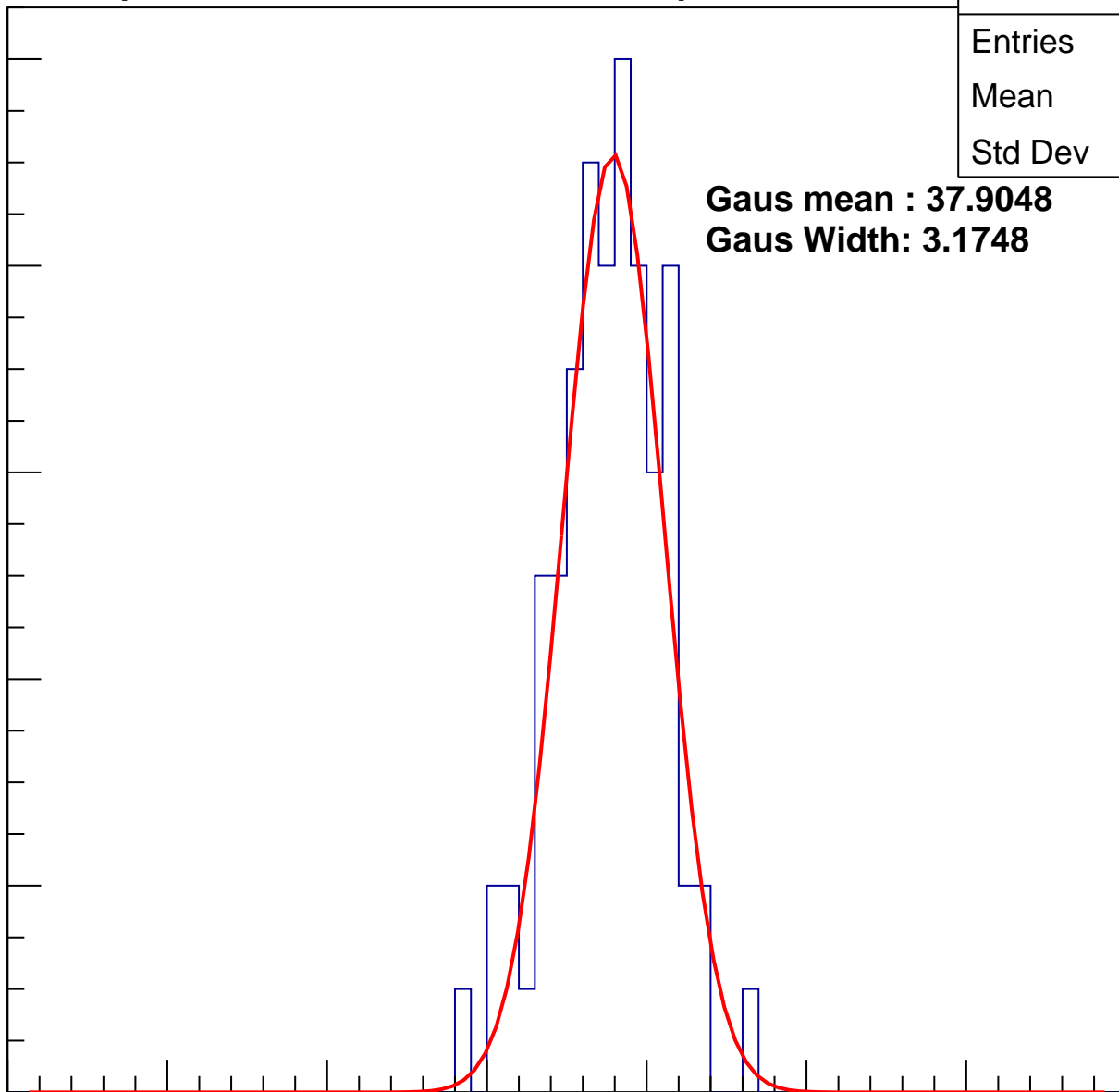
**Gaus Width: 3.1748**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L101S, U11-ch106, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	65
Mean	44.49
Std Dev	3.143

**Gaus mean : 44.7367**

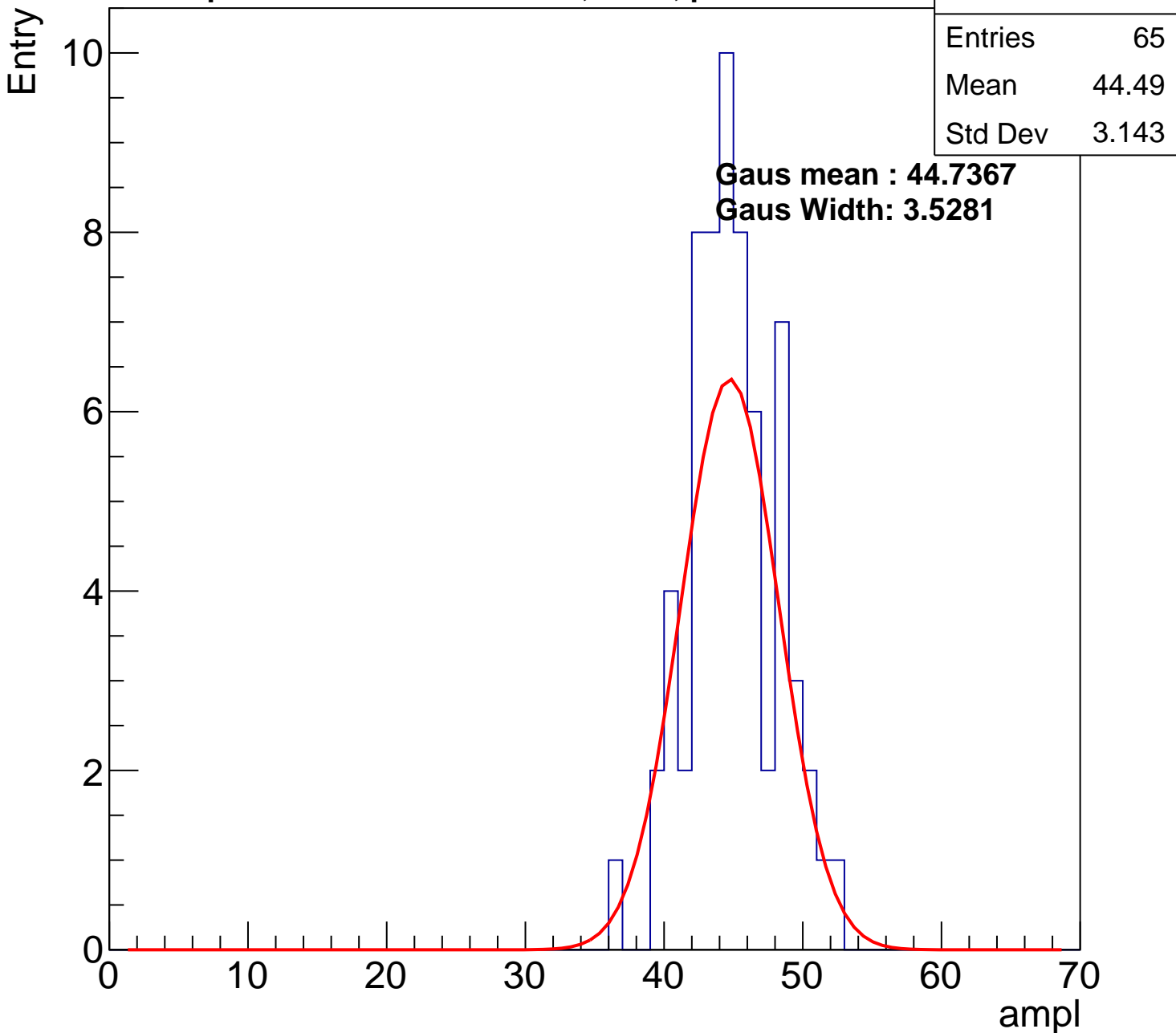
**Gaus Width: 3.5281**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

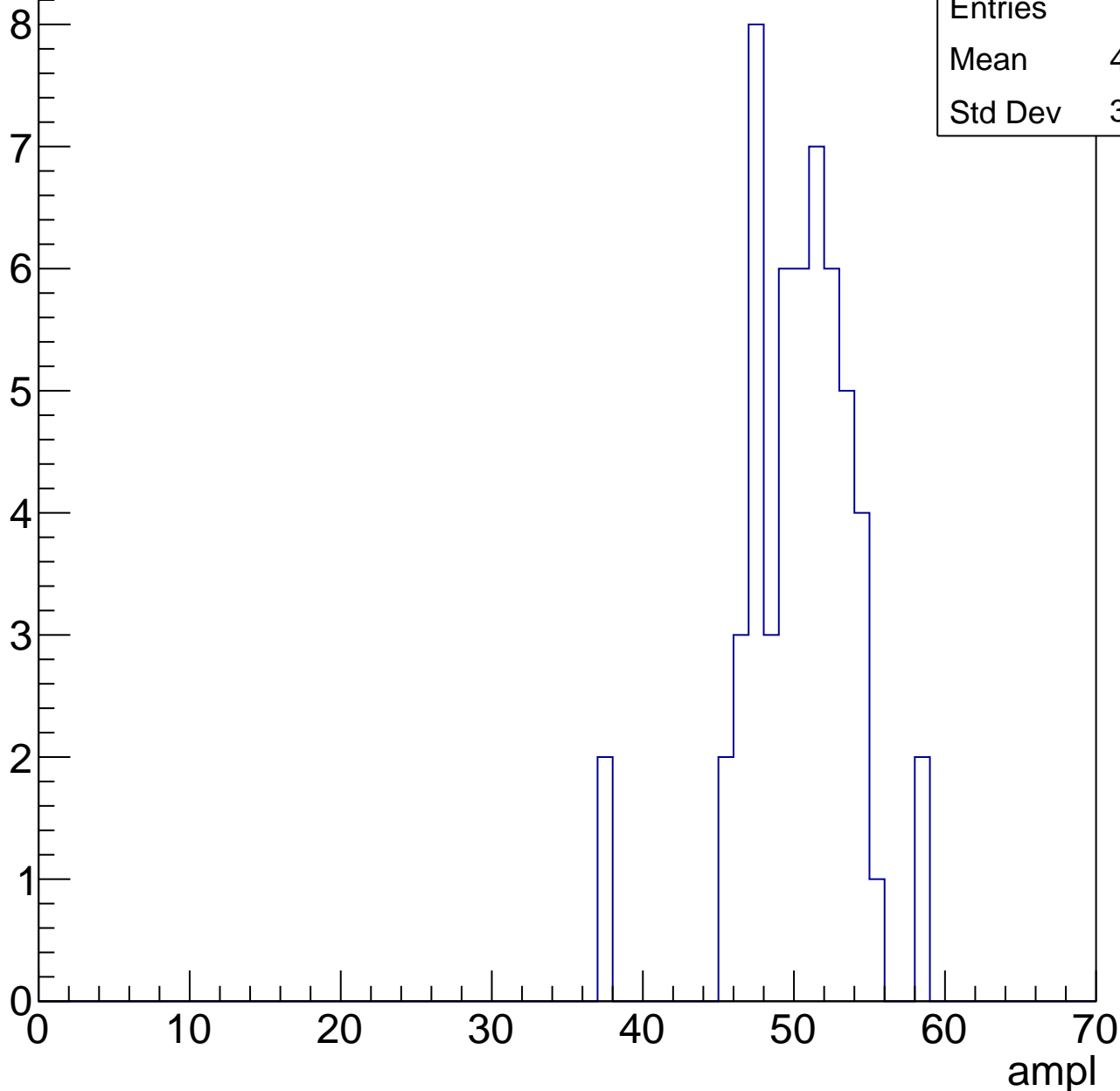


# B1L101S, U11-ch106, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	49.76
Std Dev	3.852

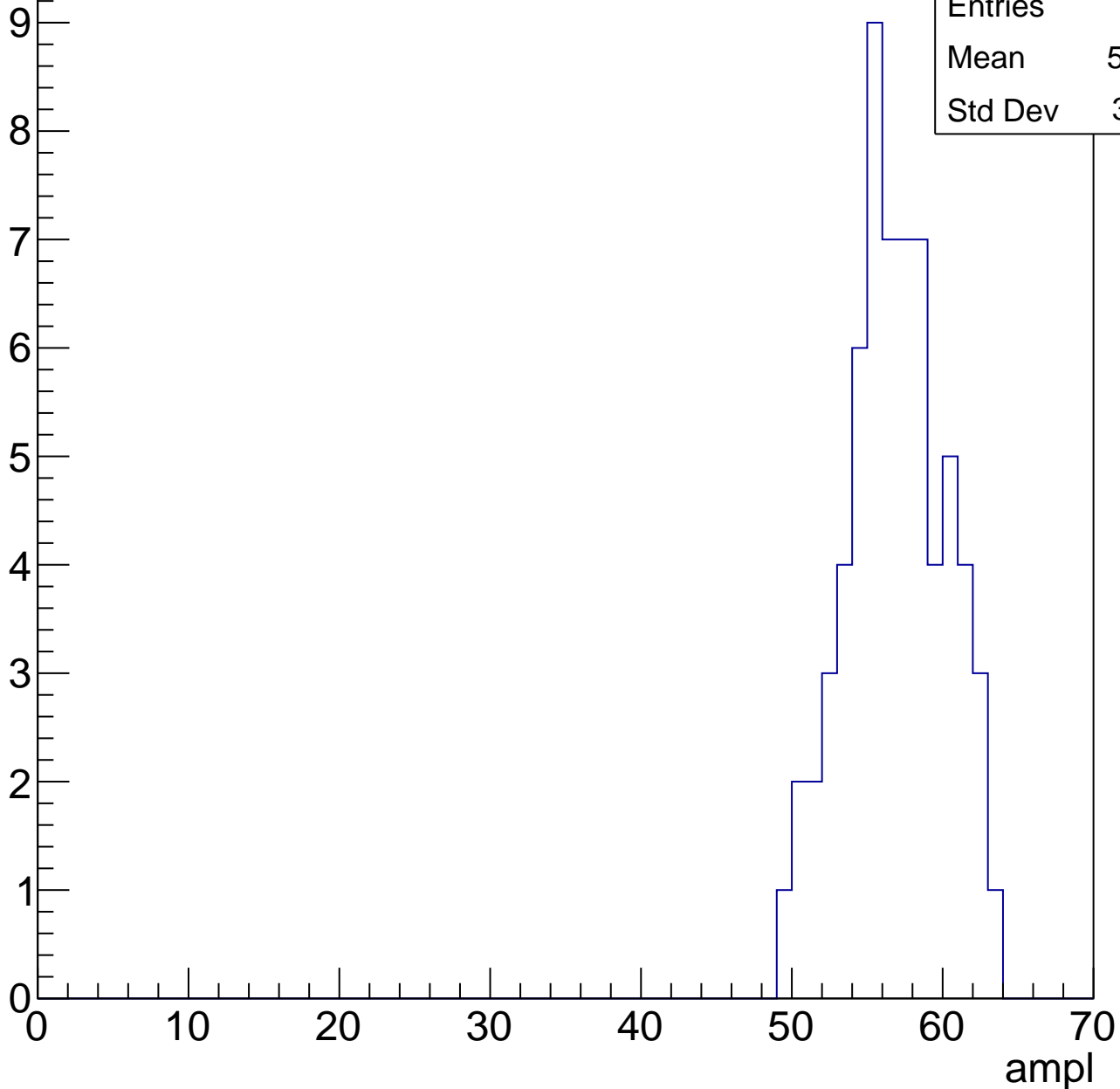


# B1L101S, U11-ch106, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	56.37
Std Dev	3.251

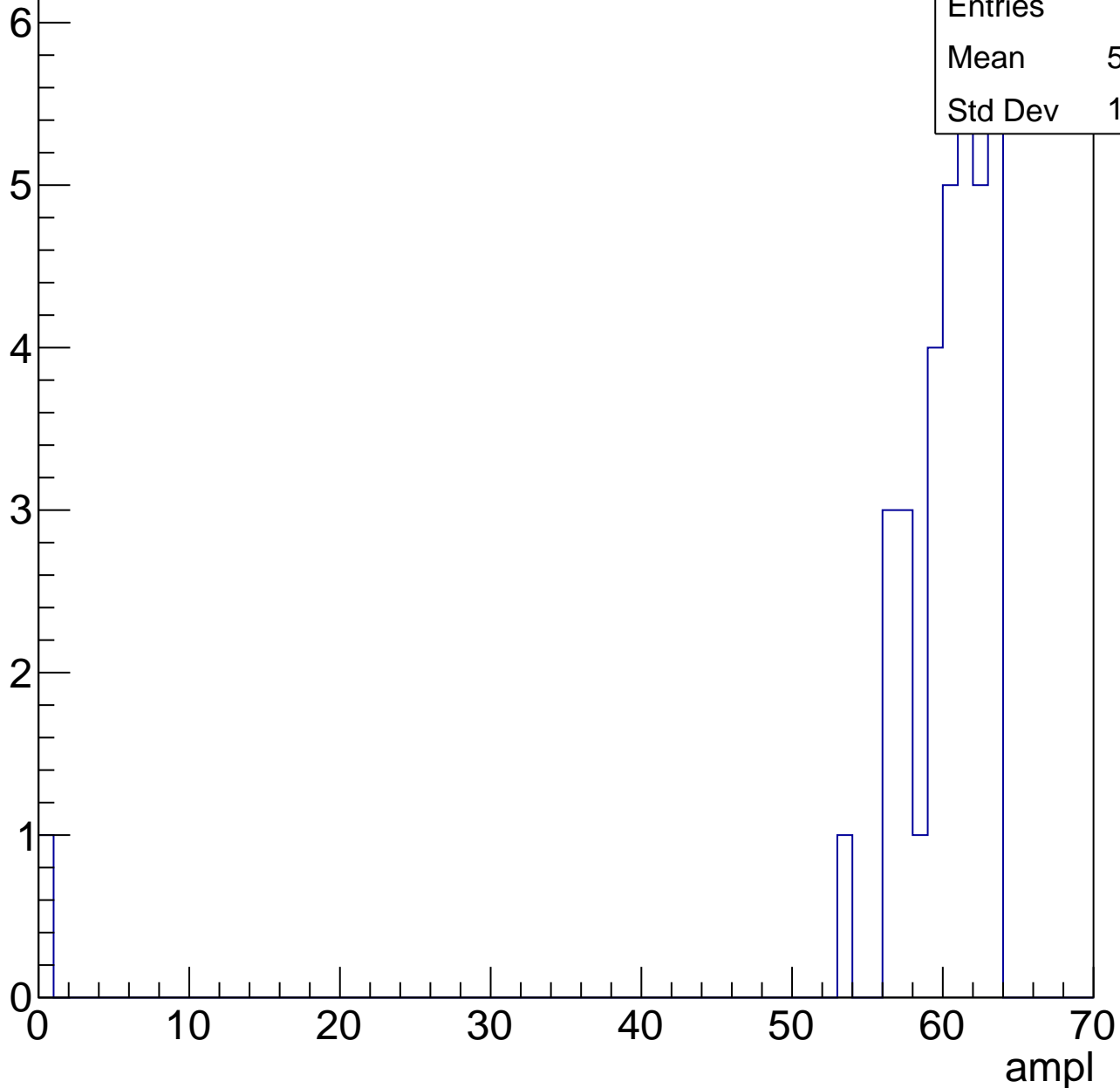


# B1L101S, U11-ch106, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

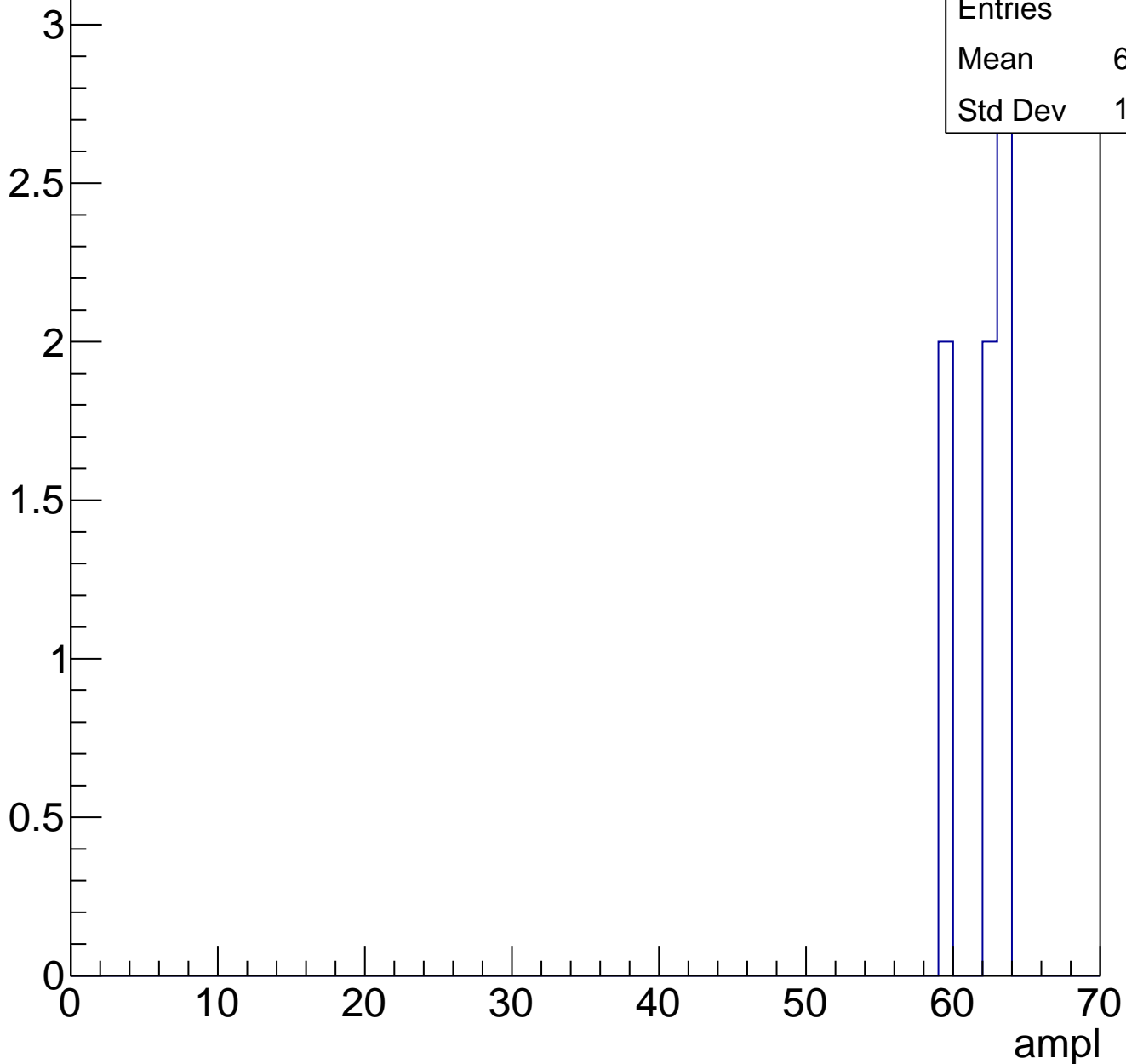
Entries	35
Mean	58.29
Std Dev	10.29



# B1L101S, U11-ch106, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	7
Mean	61.57
Std Dev	1.678



# B1L101S, U11-ch106, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U11-ch107, adc0

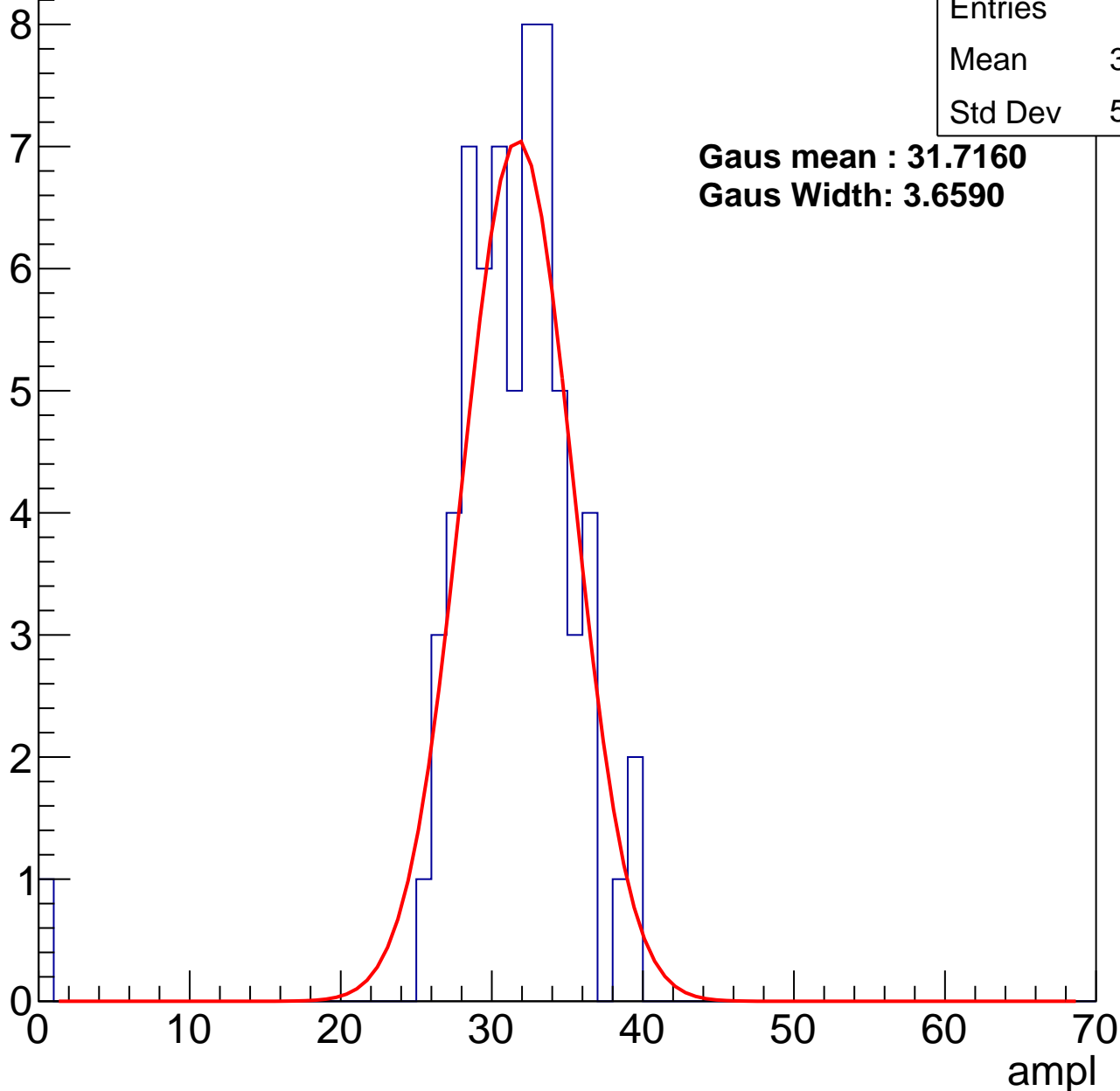
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	30.78
Std Dev	5.018

**Gaus mean : 31.7160**

**Gaus Width: 3.6590**



# B1L101S, U11-ch107, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	76
Mean	37.87
Std Dev	3.83

**Gaus mean : 38.7571**

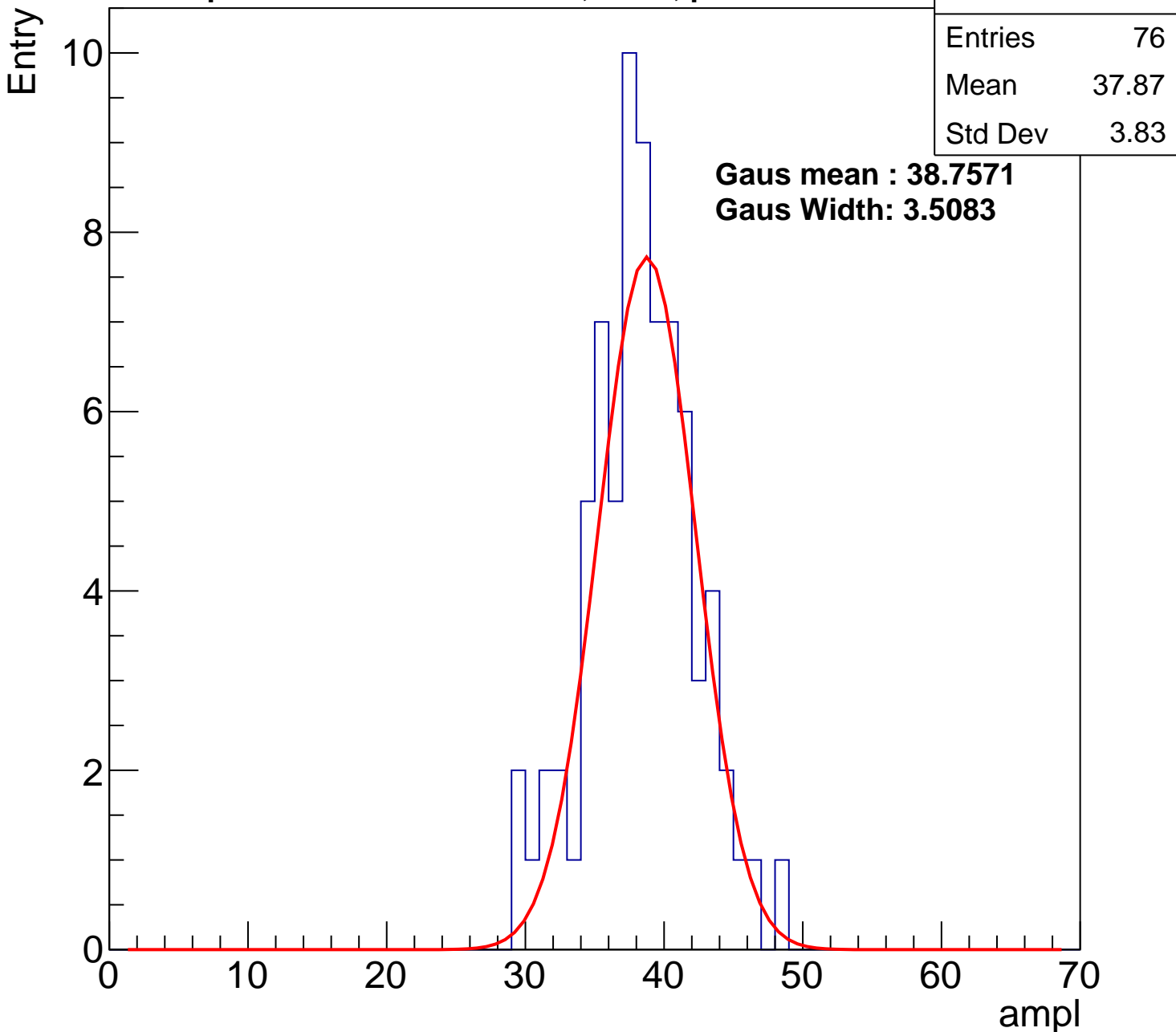
**Gaus Width: 3.5083**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



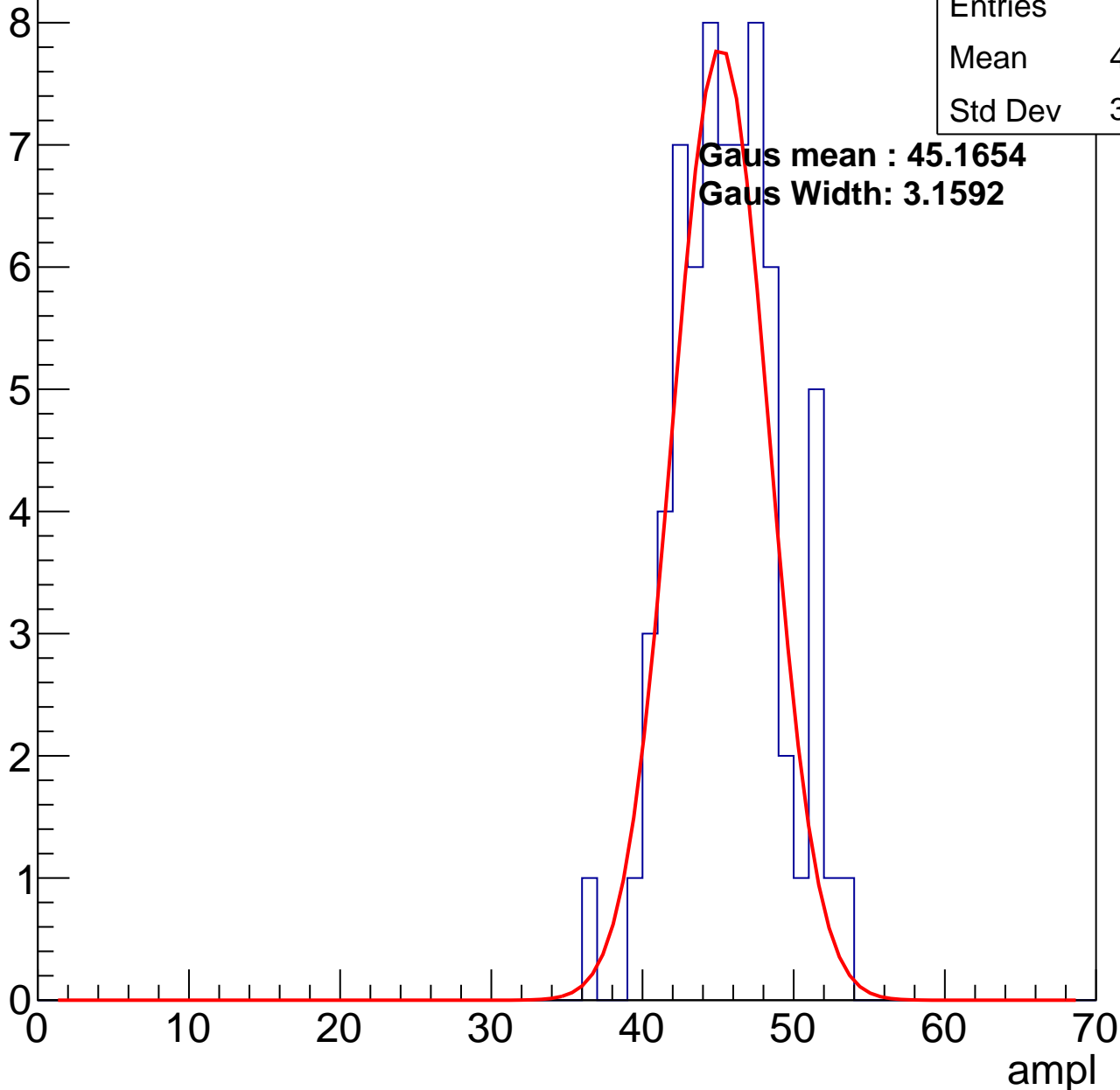
# B1L101S, U11-ch107, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	45.18
Std Dev	3.413

**Gaus mean : 45.1654**  
**Gaus Width: 3.1592**

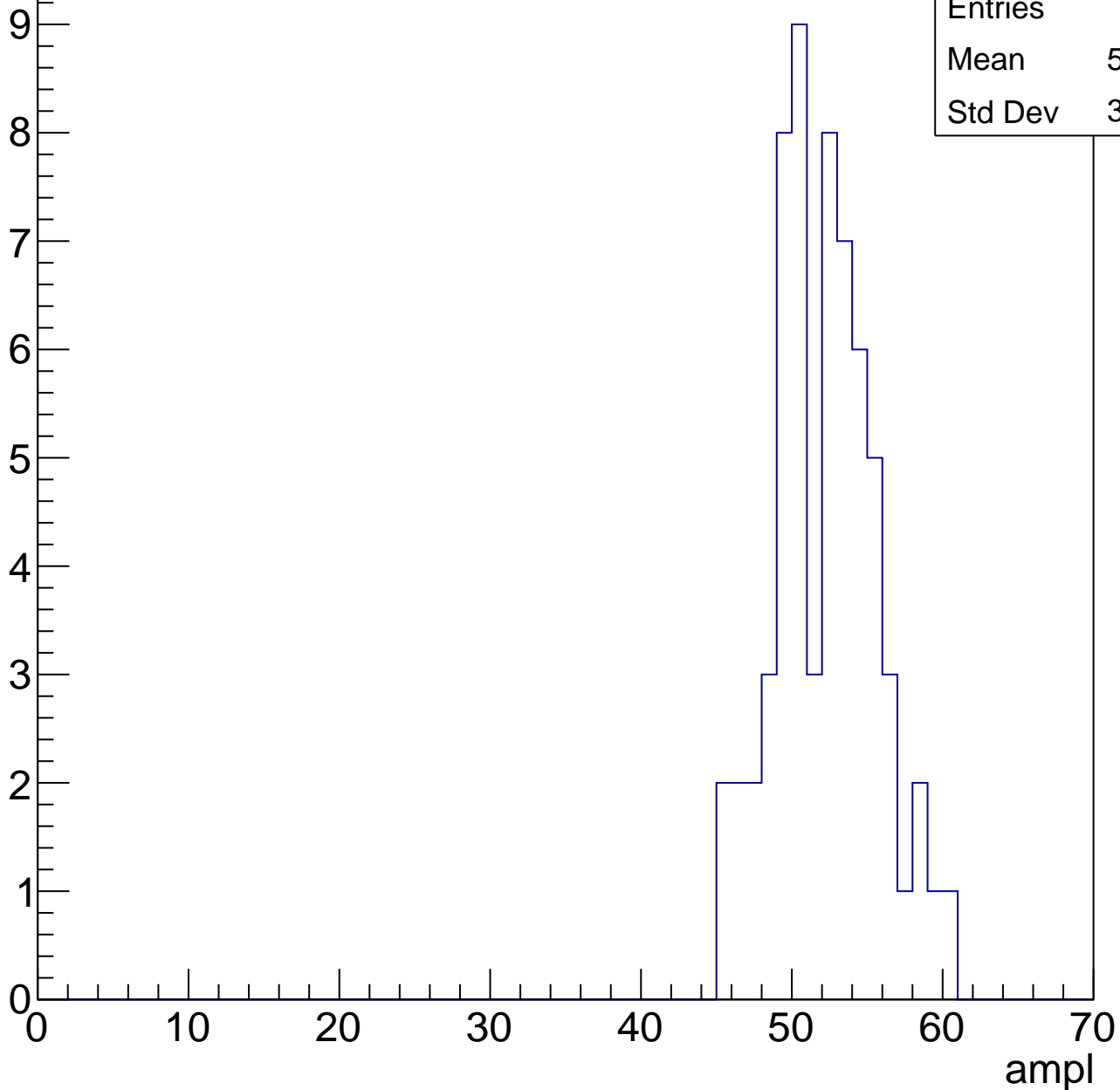


# B1L101S, U11-ch107, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

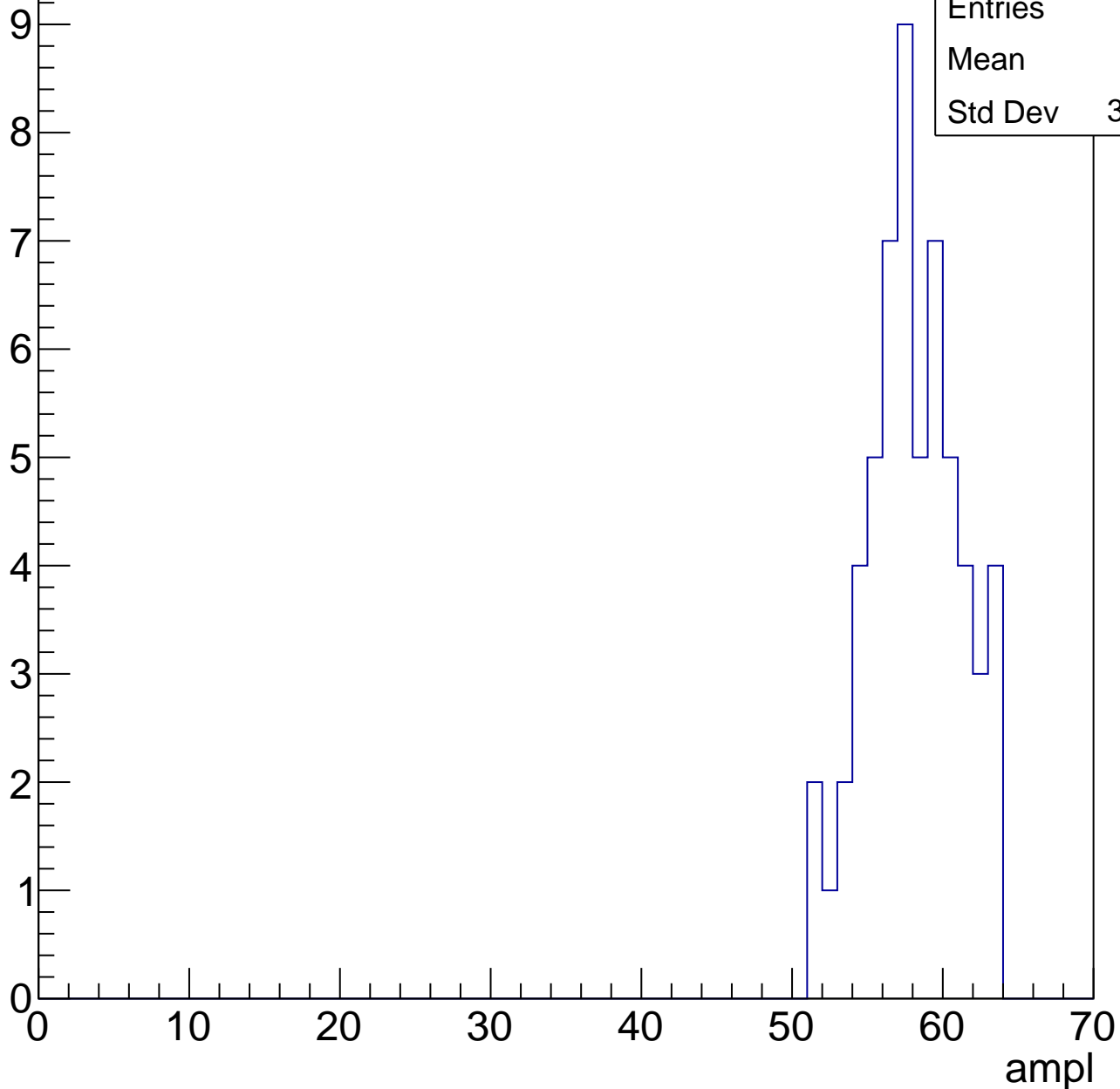
Entries	63
Mean	51.76
Std Dev	3.356



# B1L101S, U11-ch107, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

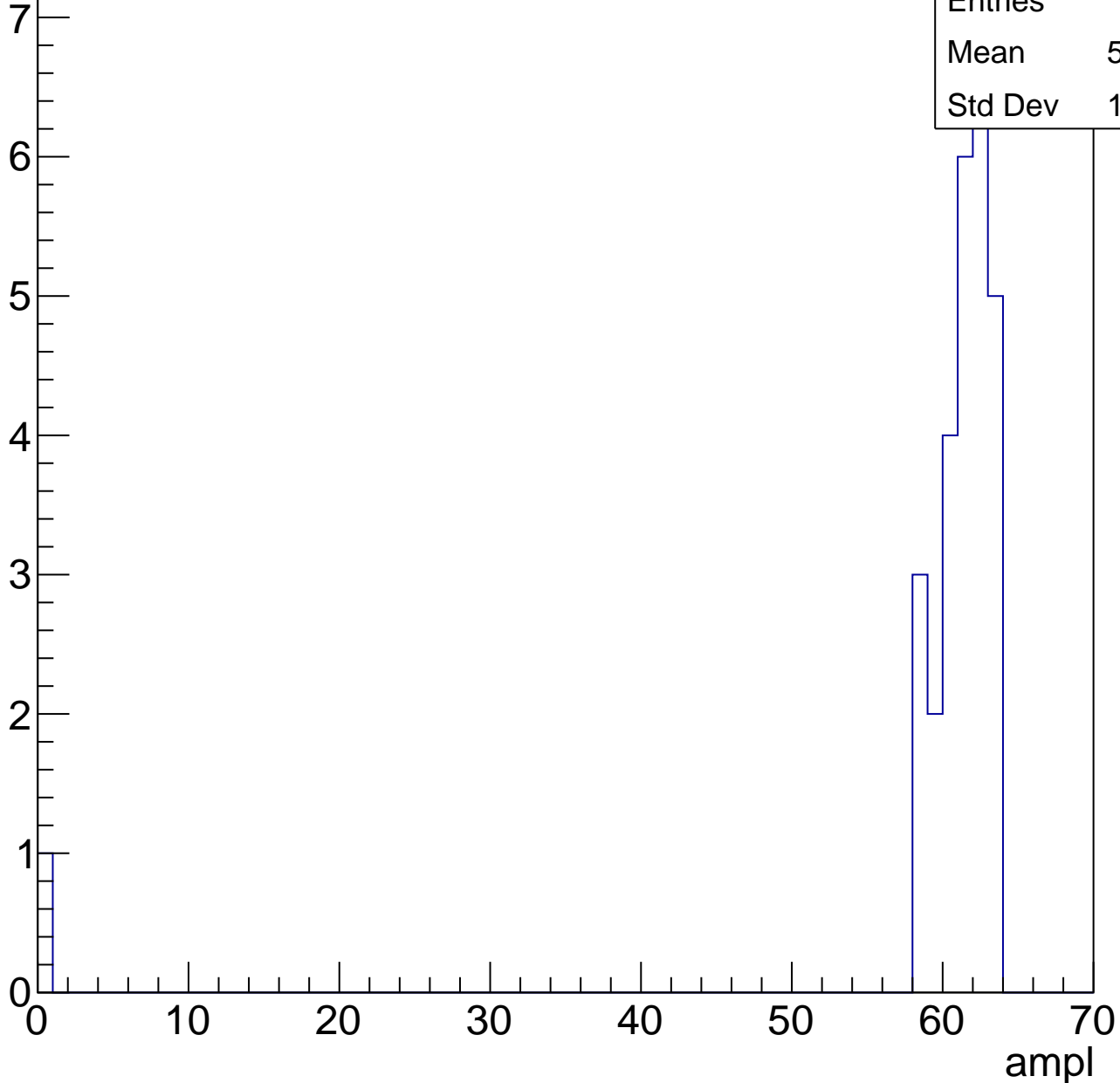


# B1L101S, U11-ch107, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	28
Mean	58.82
Std Dev	11.42



# B1L101S, U11-ch107, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch107, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	12.5
Std Dev	12.5

# B1L101S, U11-ch108, adc0

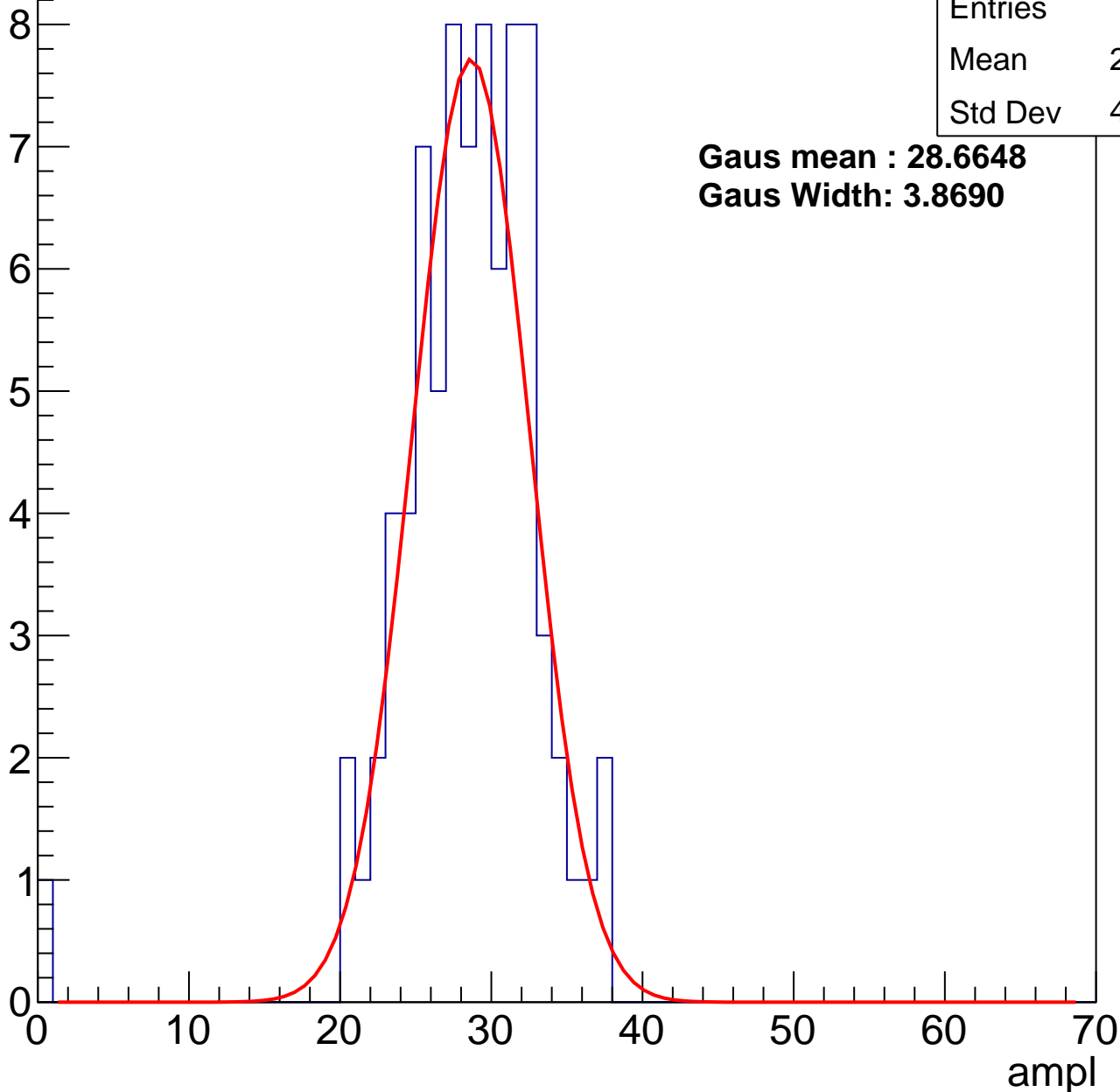
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	80
Mean	27.98
Std Dev	4.927

**Gaus mean : 28.6648**

**Gaus Width: 3.8690**



# B1L101S, U11-ch108, adc1

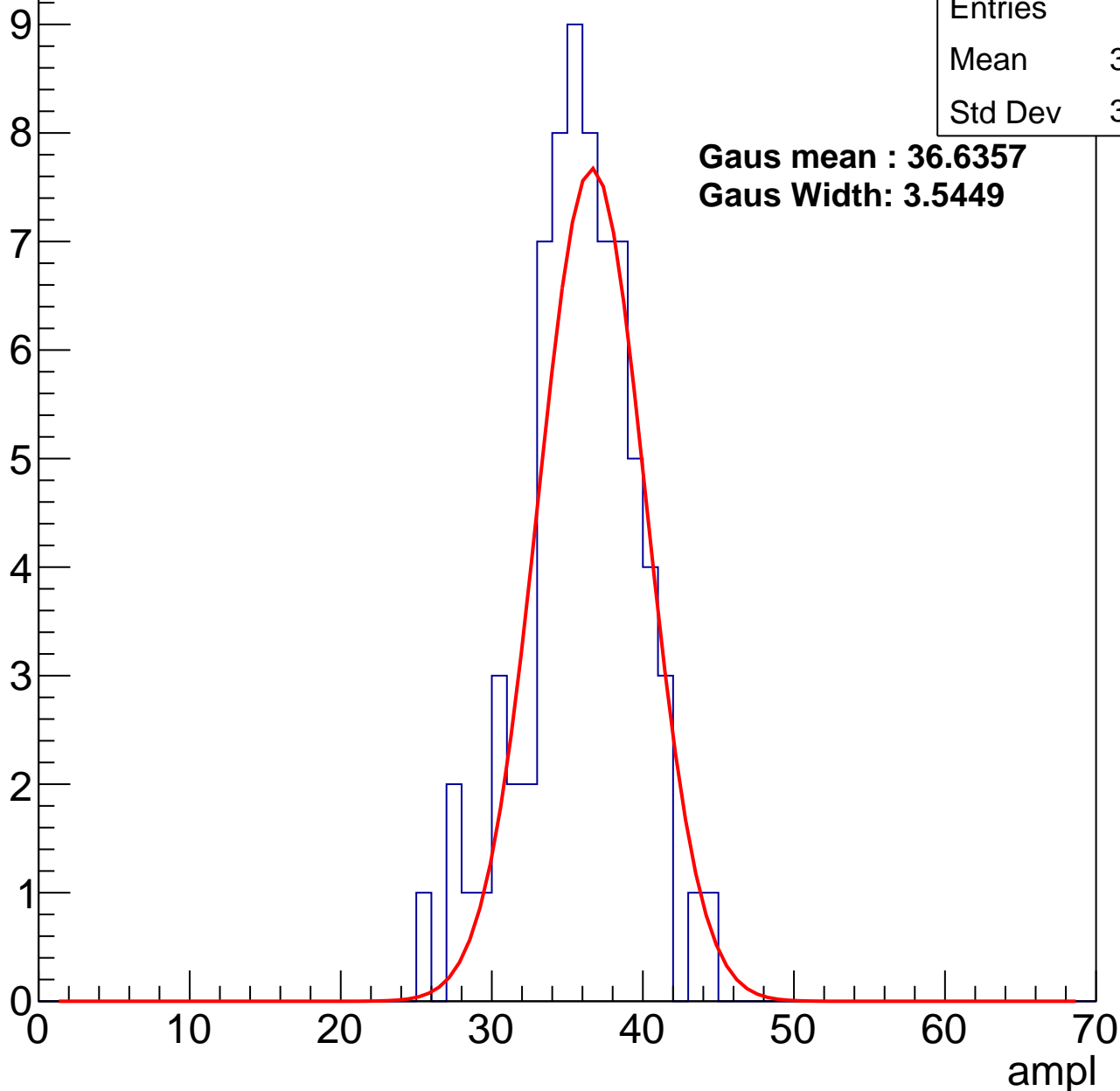
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	35.39
Std Dev	3.718

**Gaus mean : 36.6357**

**Gaus Width: 3.5449**



# B1L101S, U11-ch108, adc2

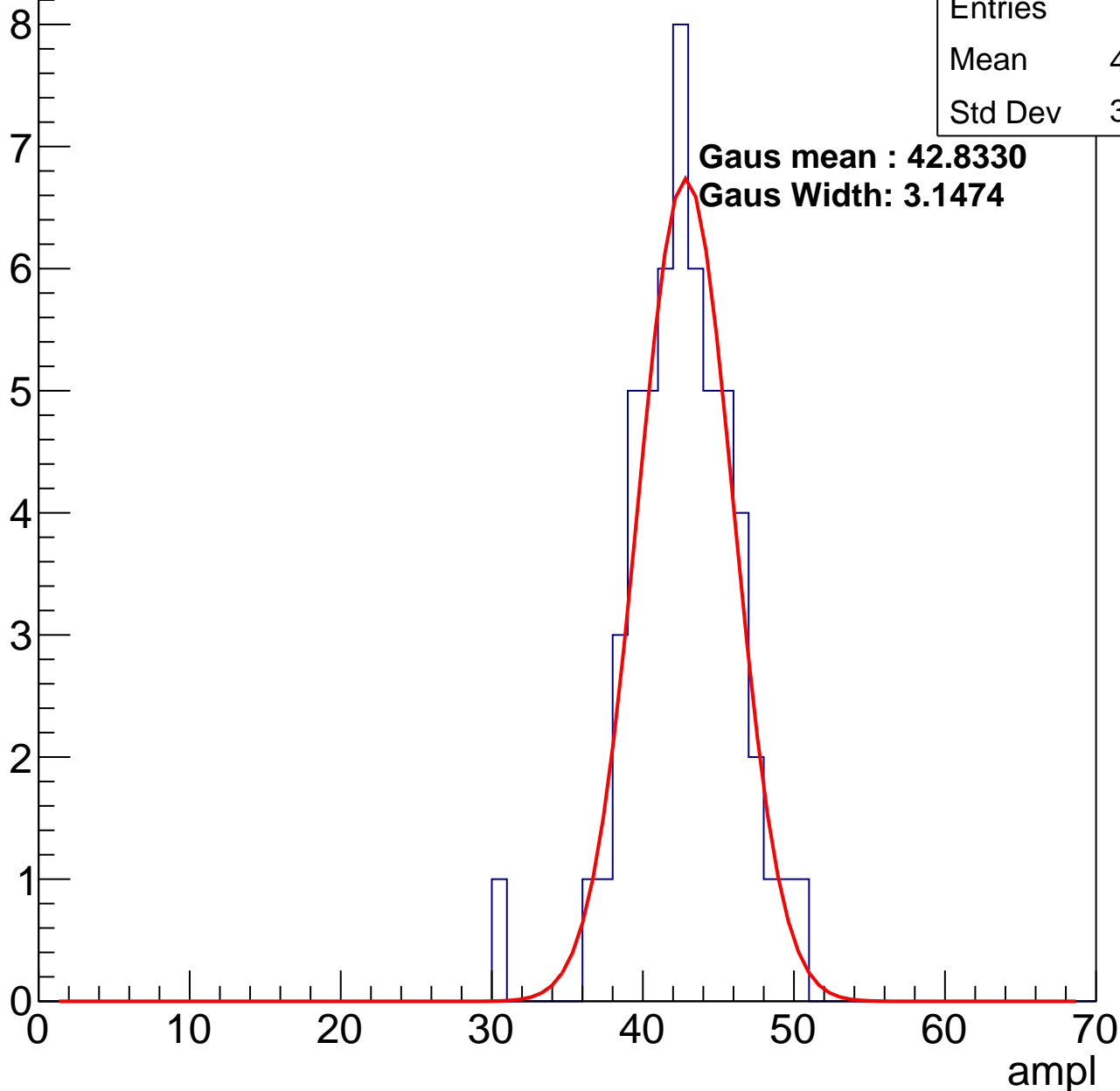
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	42.22
Std Dev	3.452

**Gaus mean : 42.8330**

**Gaus Width: 3.1474**

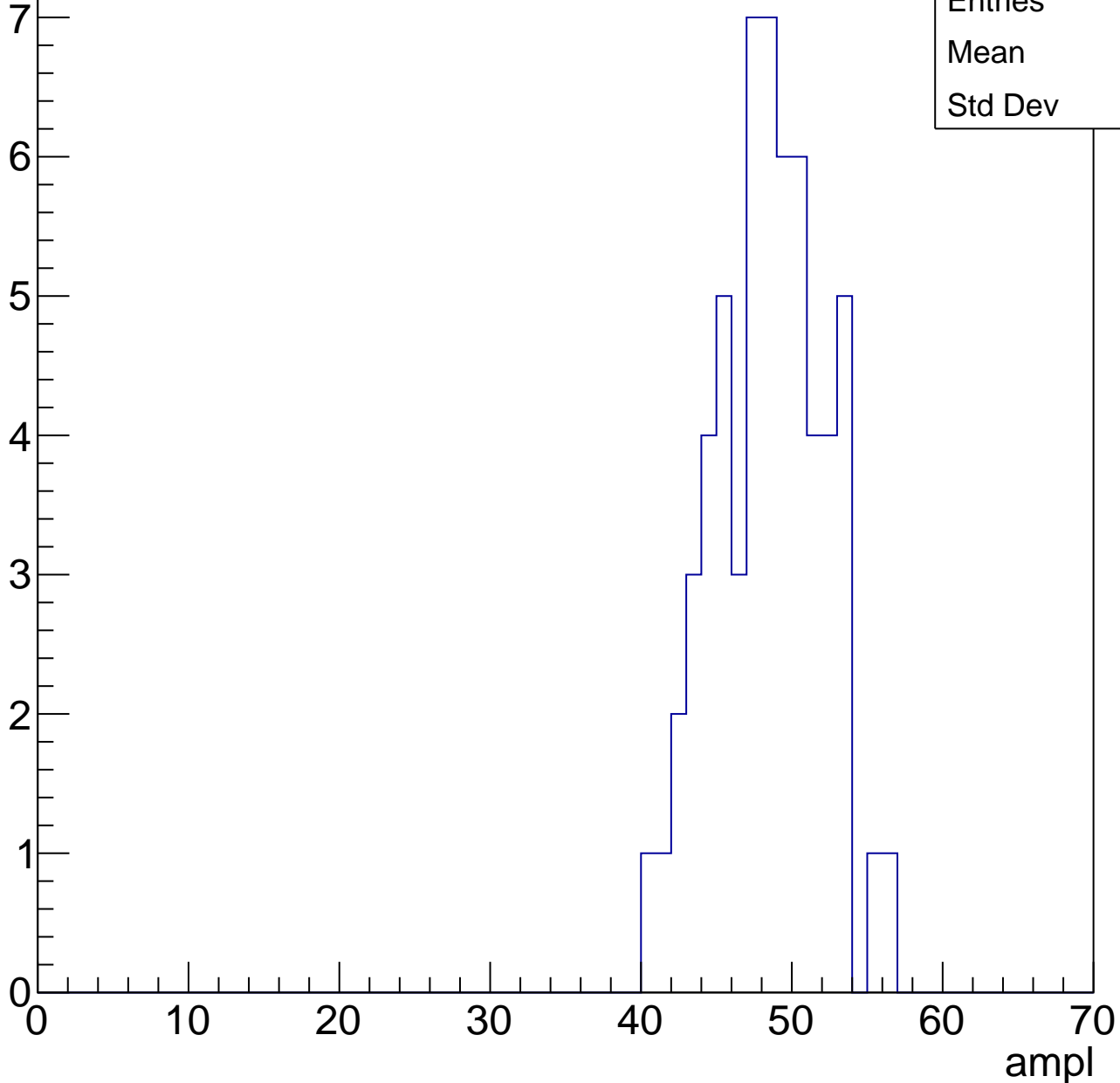


# B1L101S, U11-ch108, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	48
Std Dev	3.55

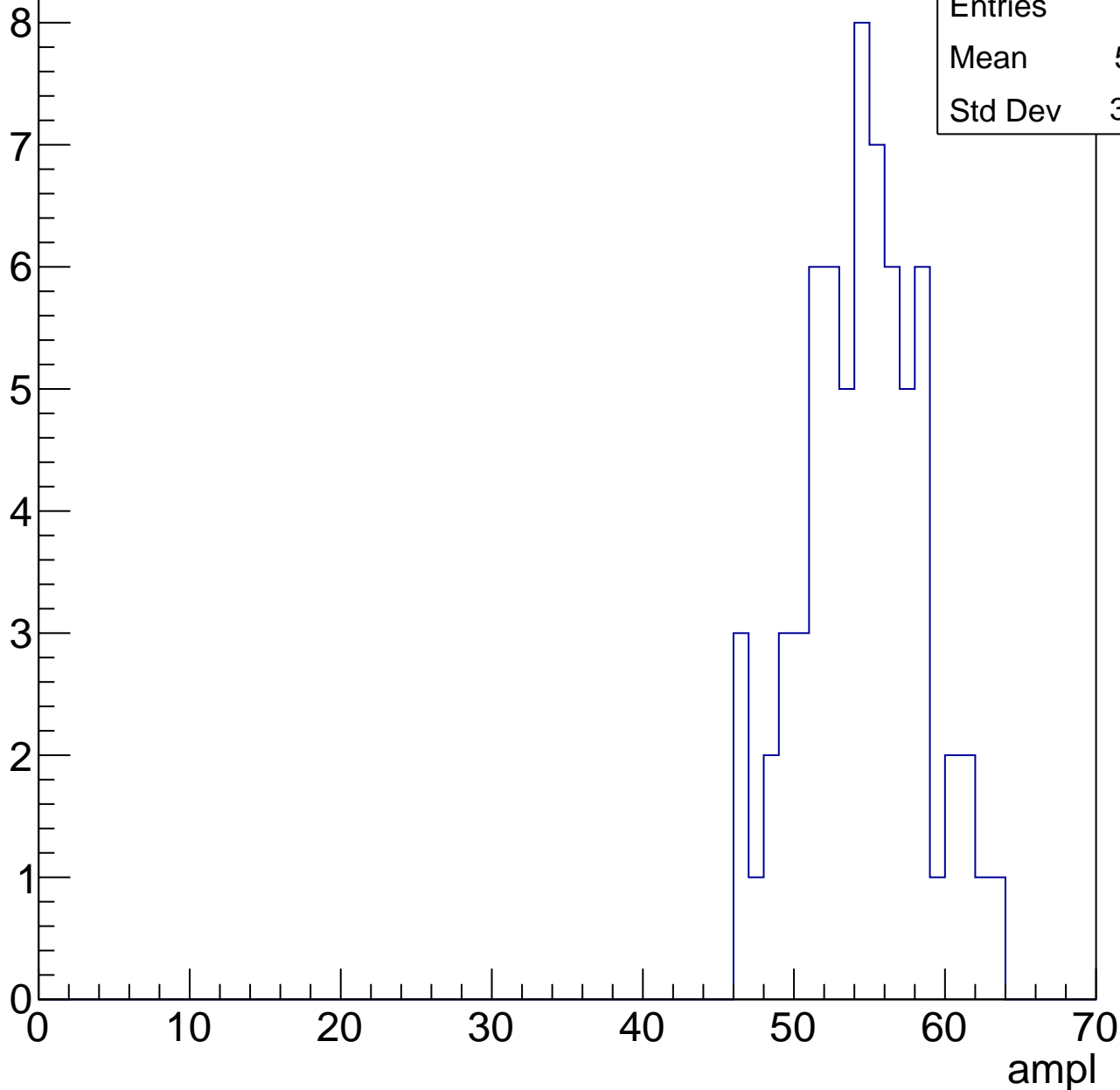


# B1L101S, U11-ch108, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	54.01
Std Dev	3.894

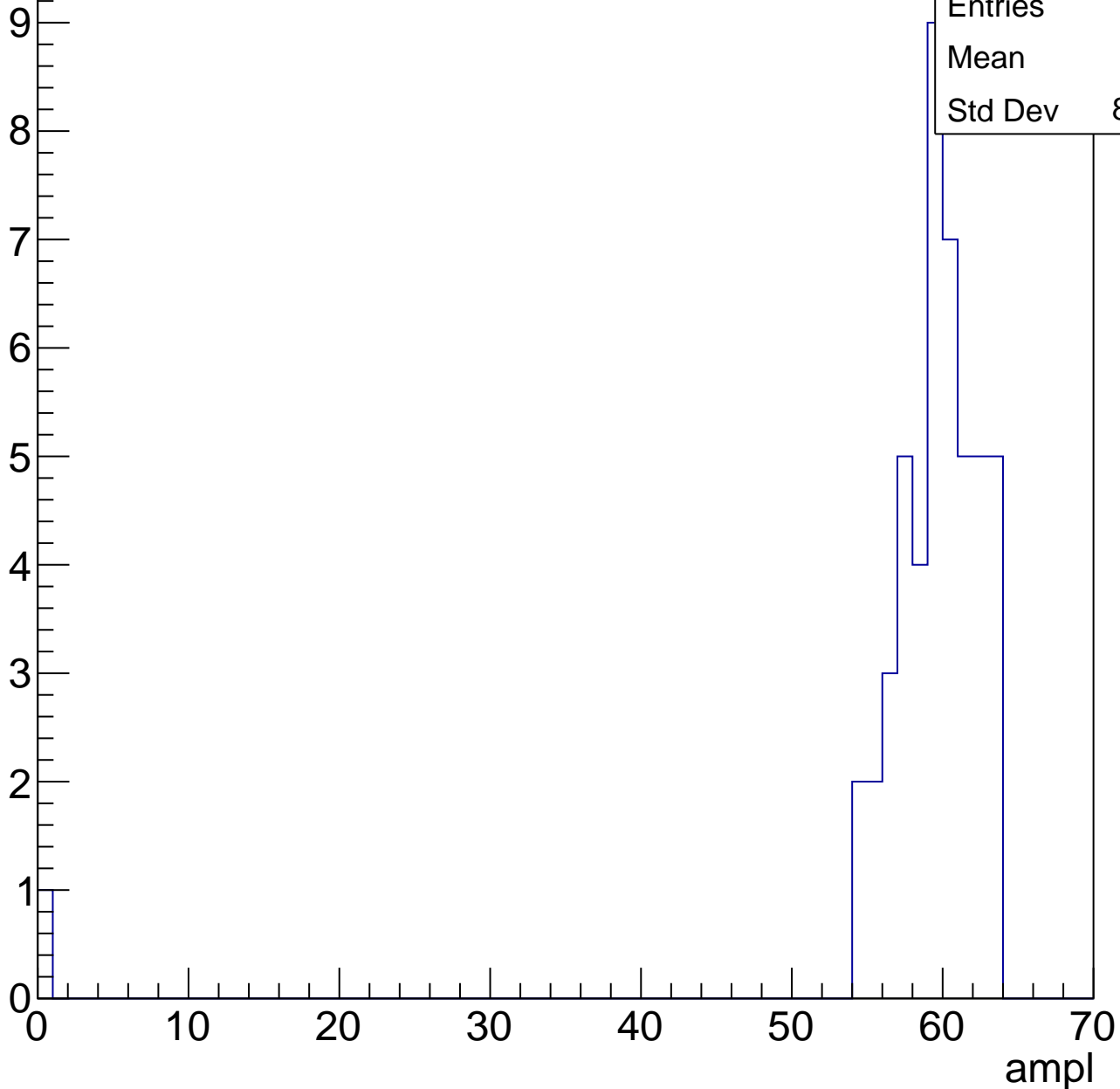


# B1L101S, U11-ch108, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

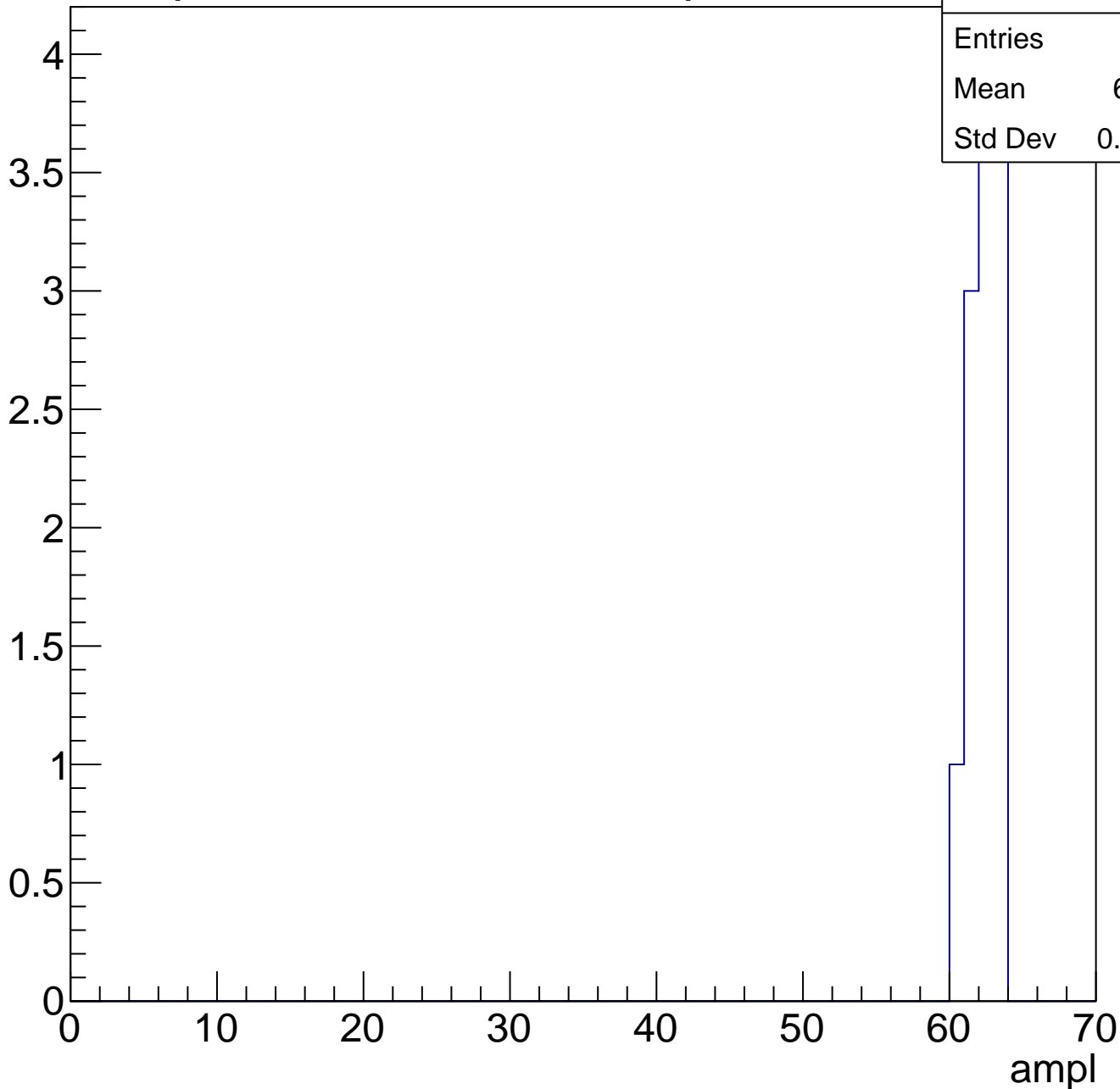
Entries	48
Mean	58
Std Dev	8.801



# B1L101S, U11-ch108, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch108, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U11-ch109, adc0

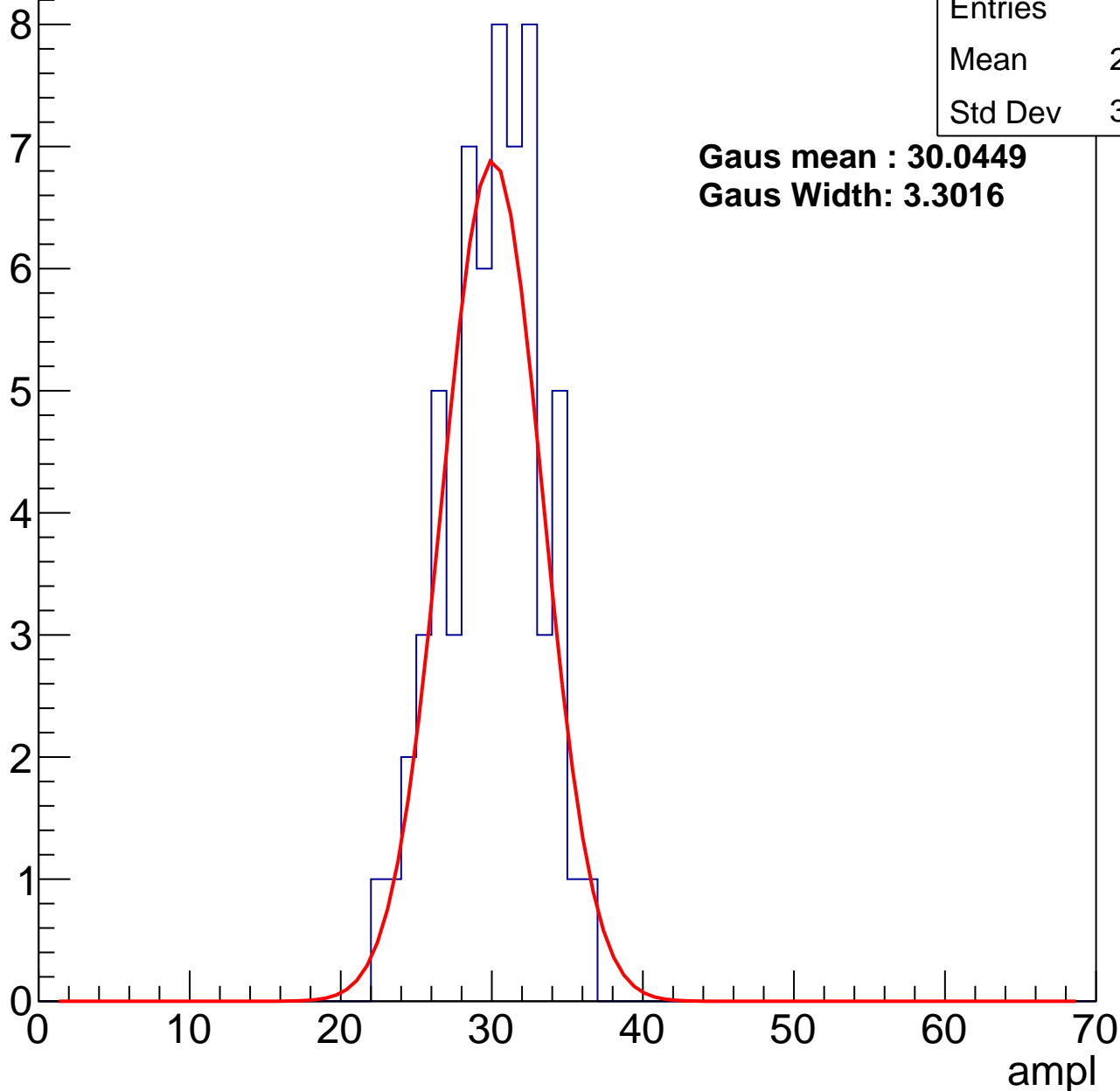
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	29.54
Std Dev	3.124

**Gaus mean : 30.0449**

**Gaus Width: 3.3016**



# B1L101S, U11-ch109, adc1

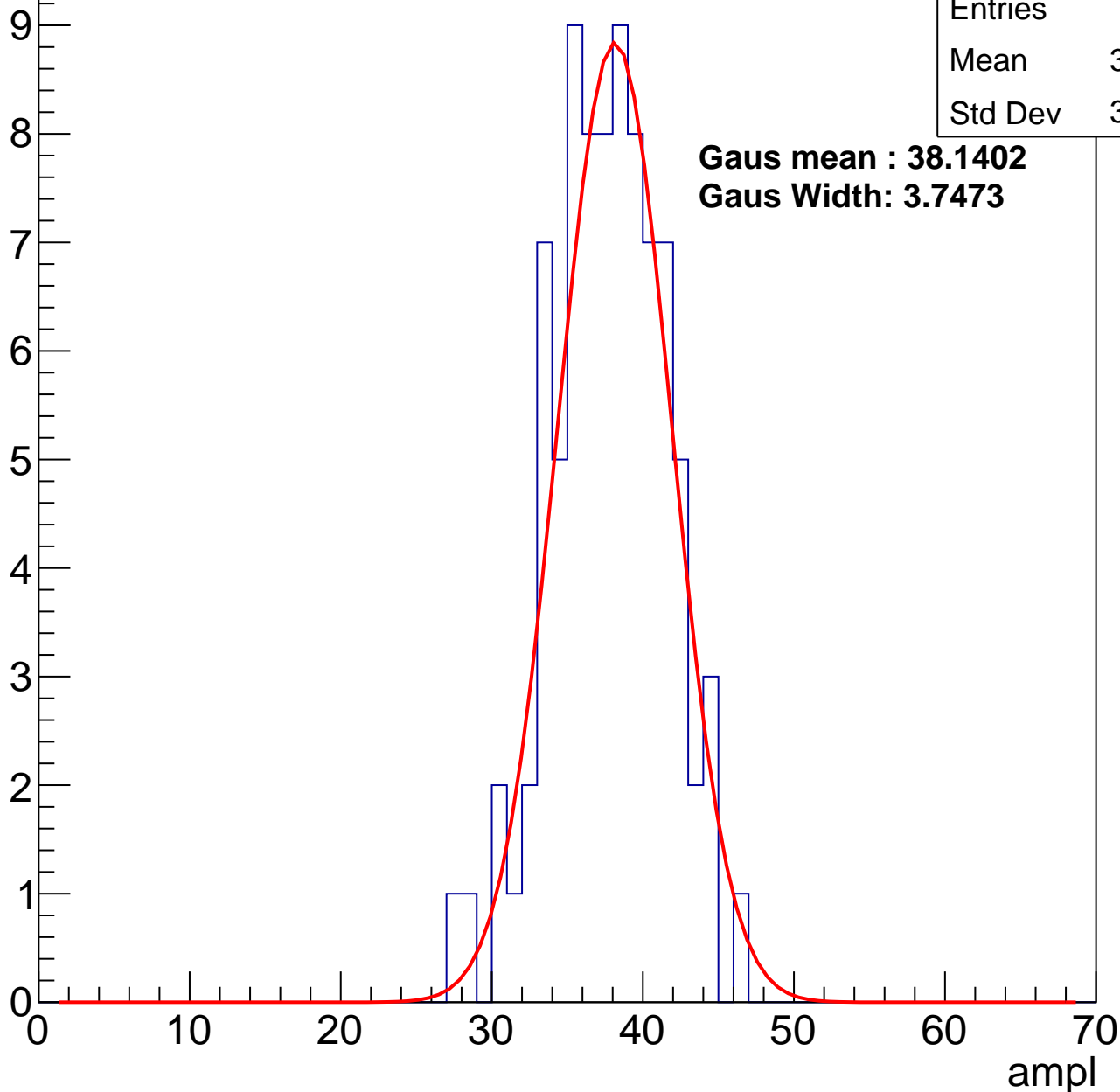
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	86
Mean	37.27
Std Dev	3.737

**Gaus mean : 38.1402**

**Gaus Width: 3.7473**



# B1L101S, U11-ch109, adc2

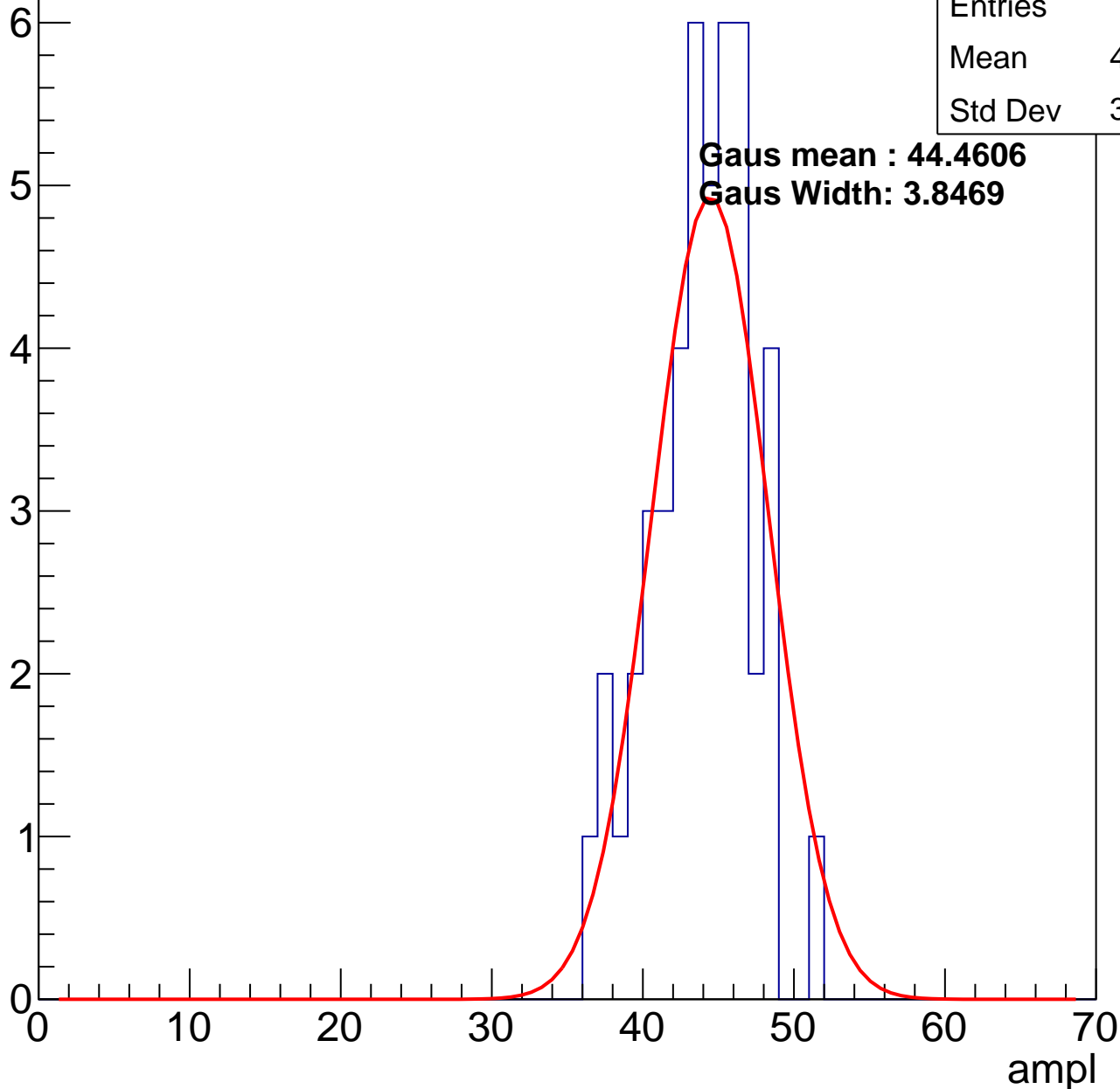
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	46
Mean	43.43
Std Dev	3.268

**Gaus mean : 44.4606**

**Gaus Width: 3.8469**

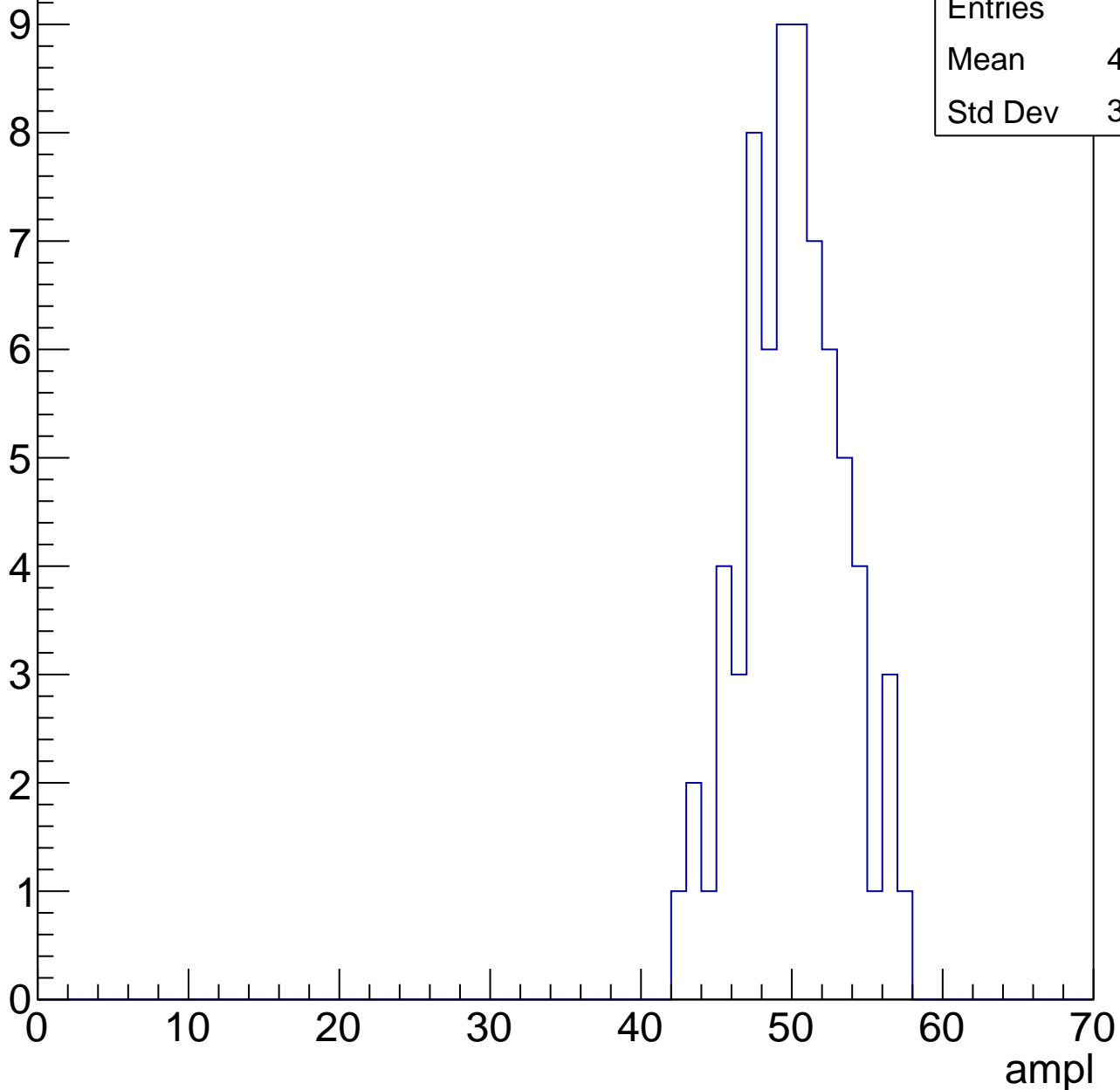


# B1L101S, U11-ch109, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	49.64
Std Dev	3.304

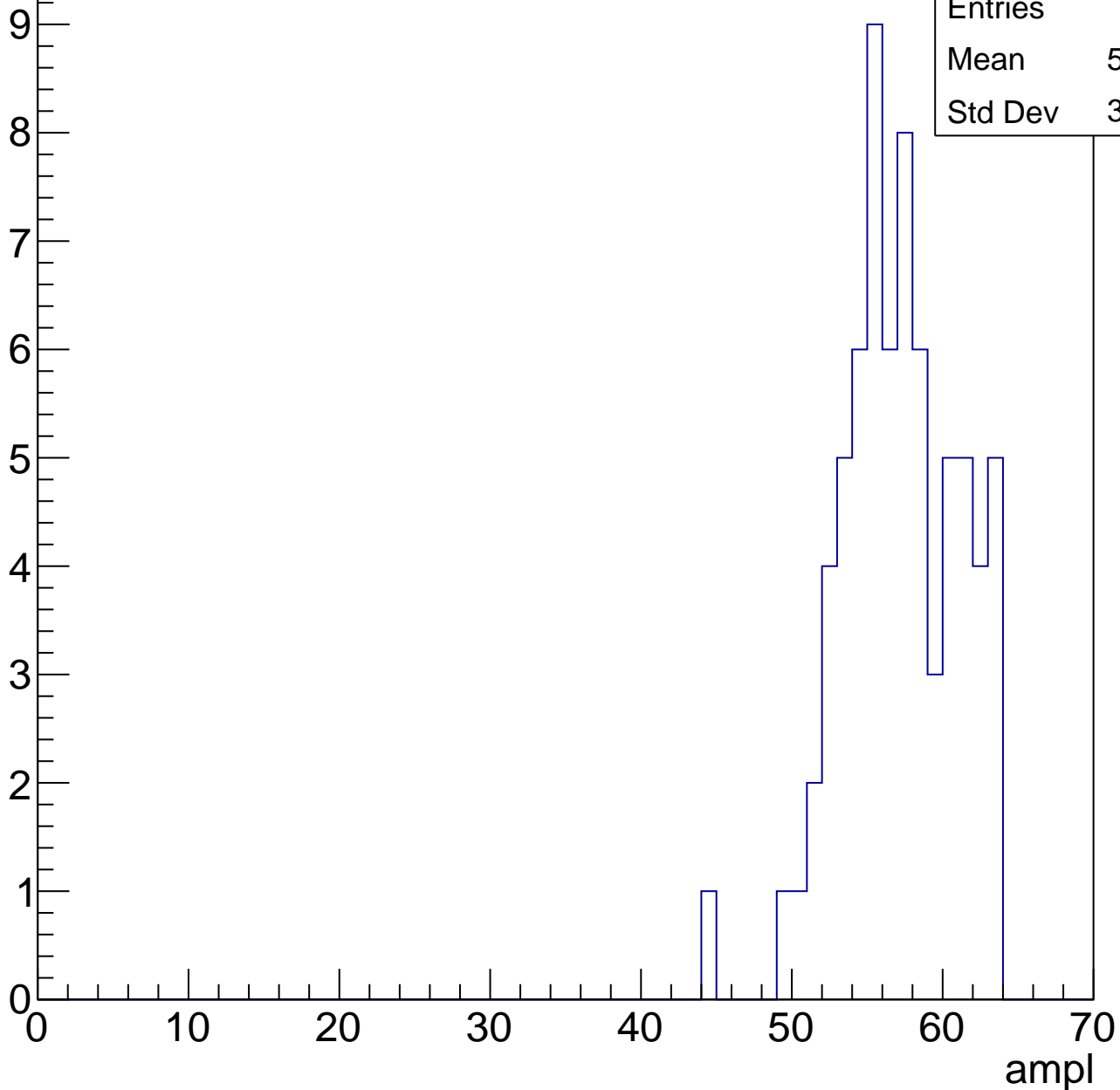


# B1L101S, U11-ch109, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	56.65
Std Dev	3.835

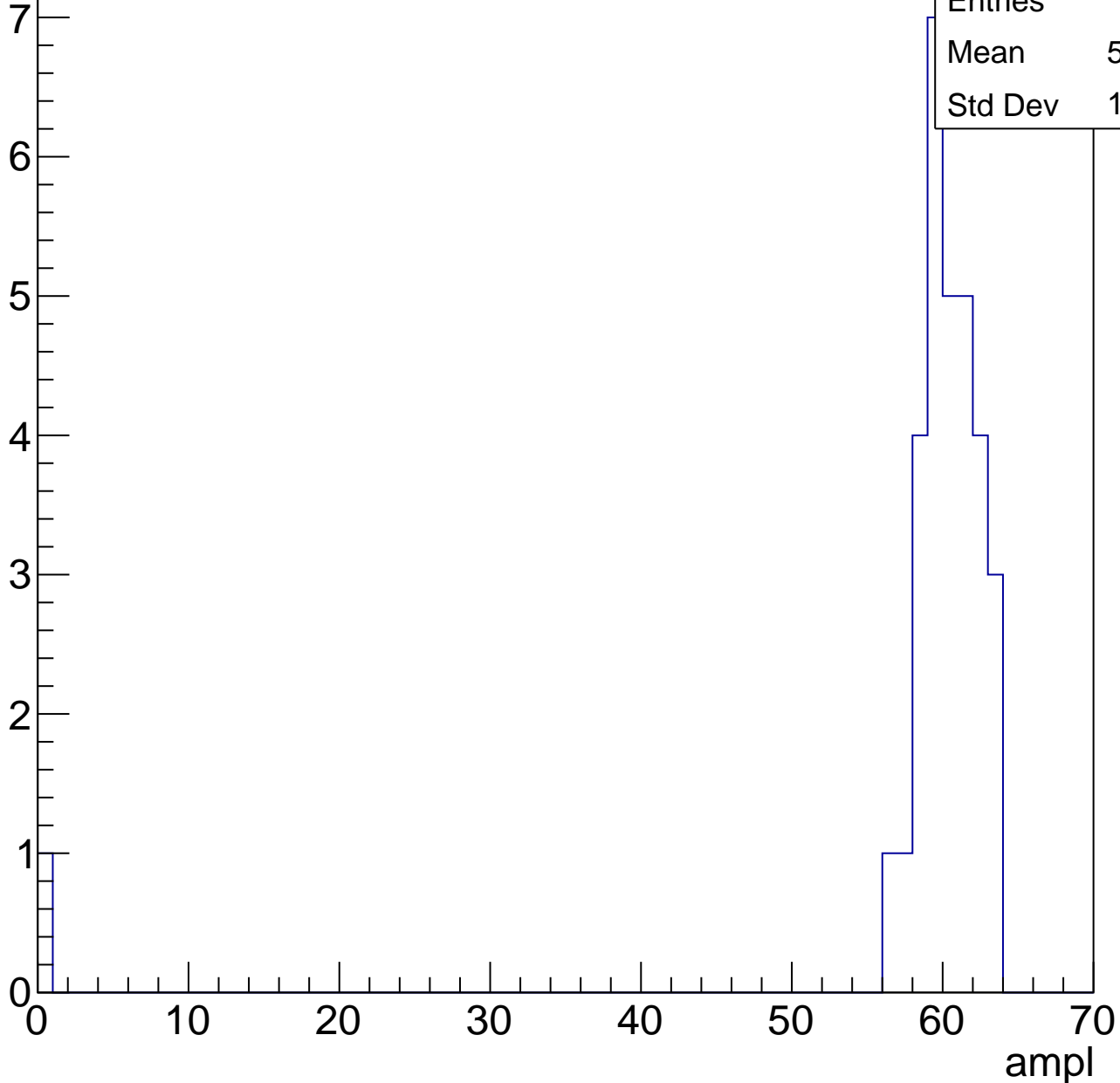


# B1L101S, U11-ch109, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	31
Mean	58.06
Std Dev	10.75



# B1L101S, U11-ch109, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch109, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U11-ch110, adc0

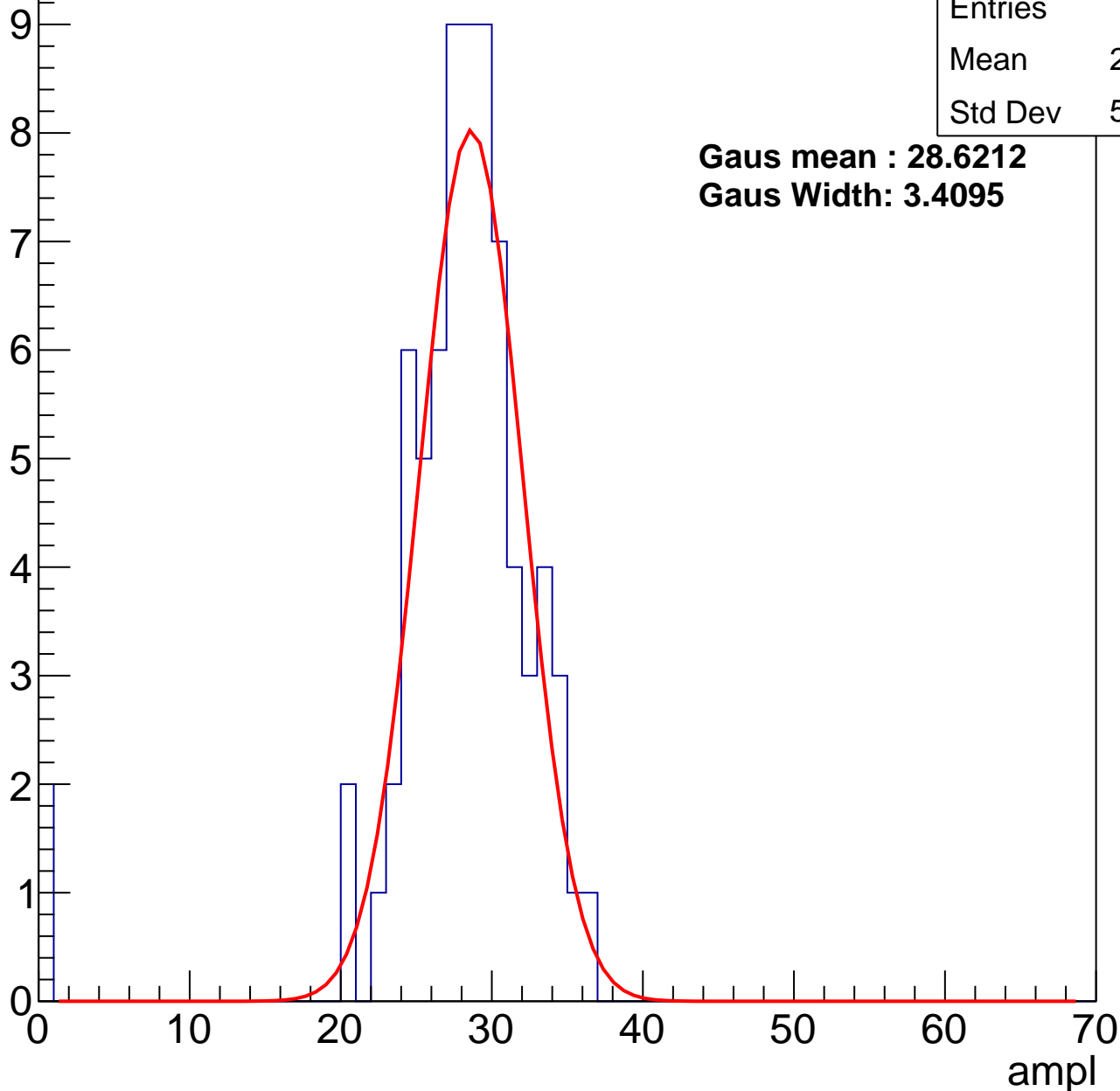
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	27.35
Std Dev	5.655

**Gaus mean : 28.6212**

**Gaus Width: 3.4095**



# B1L101S, U11-ch110, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

7

6

5

4

3

2

1

0

Entries

61

Mean

35.2

Std Dev

3.67

**Gaus mean : 35.0062**

**Gaus Width: 3.4082**

ampl

0

10

20

30

40

50

60

70

Entry

7

6

5

4

3

2

1

0

Entries

61

Mean

35.2

Std Dev

3.67

**Gaus mean : 35.0062**

**Gaus Width: 3.4082**

ampl

0

10

20

30

40

50

60

70

# B1L101S, U11-ch110, adc2

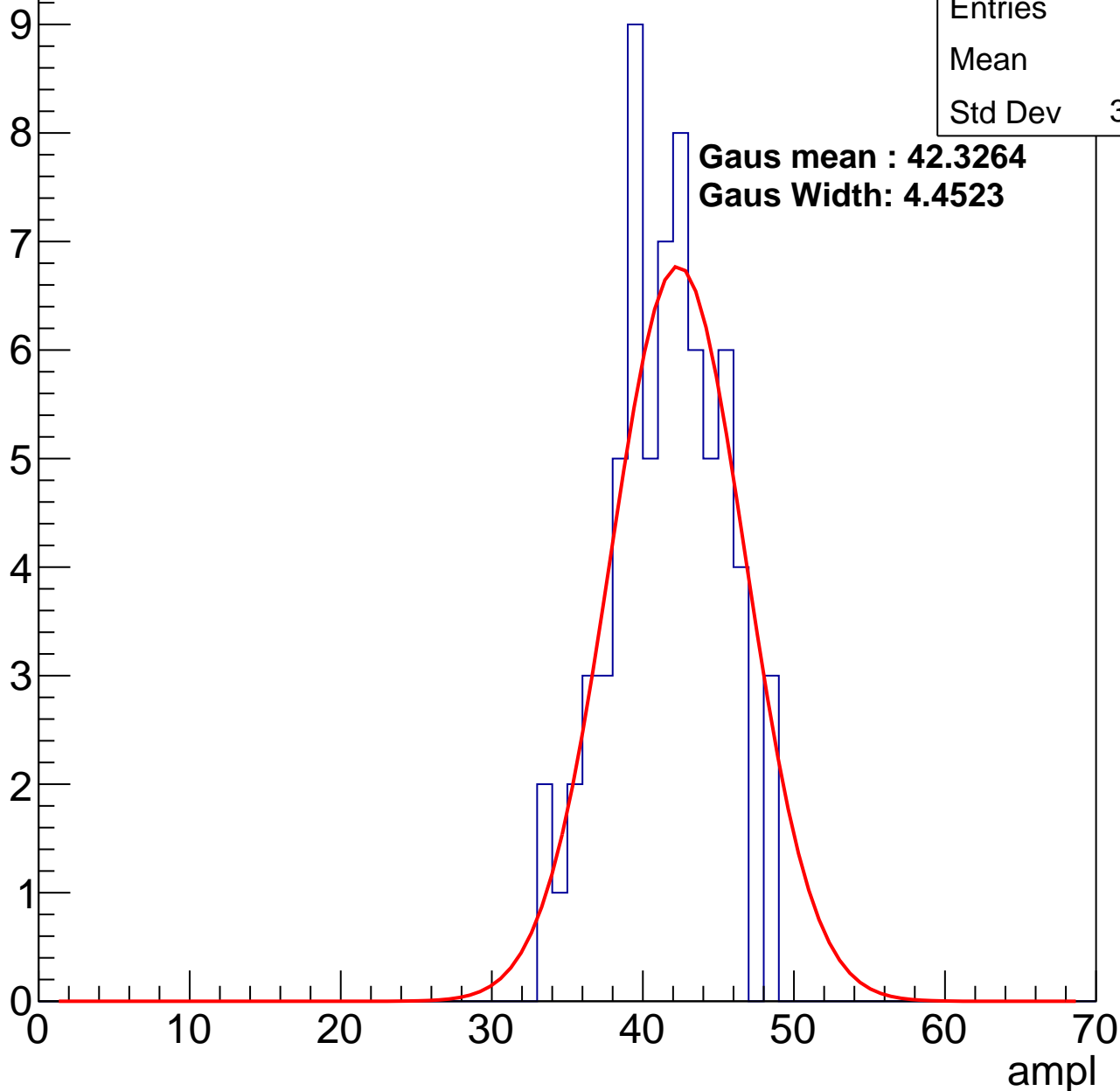
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	41
Std Dev	3.567

**Gaus mean : 42.3264**

**Gaus Width: 4.4523**

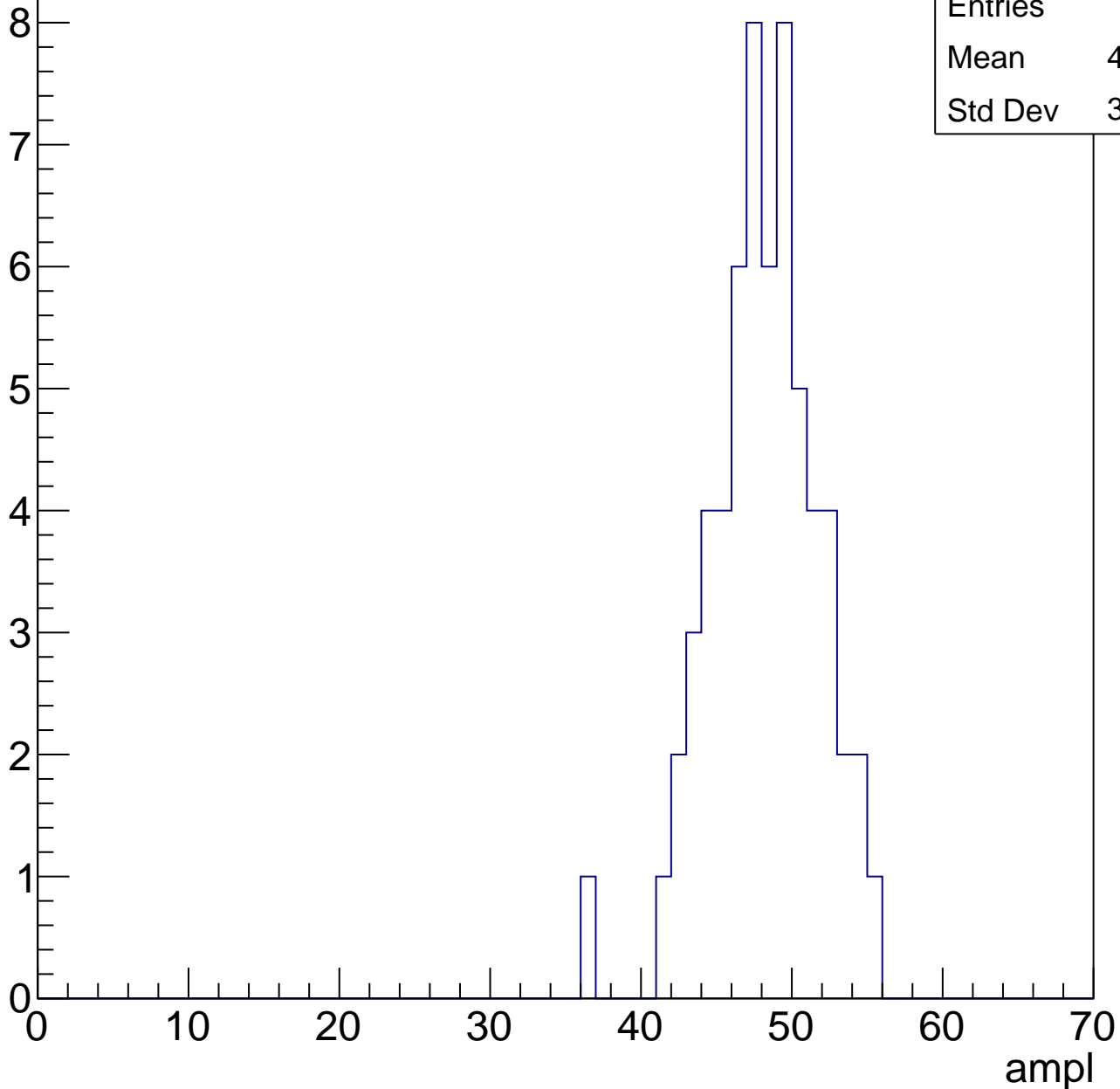


# B1L101S, U11-ch110, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	47.69
Std Dev	3.542

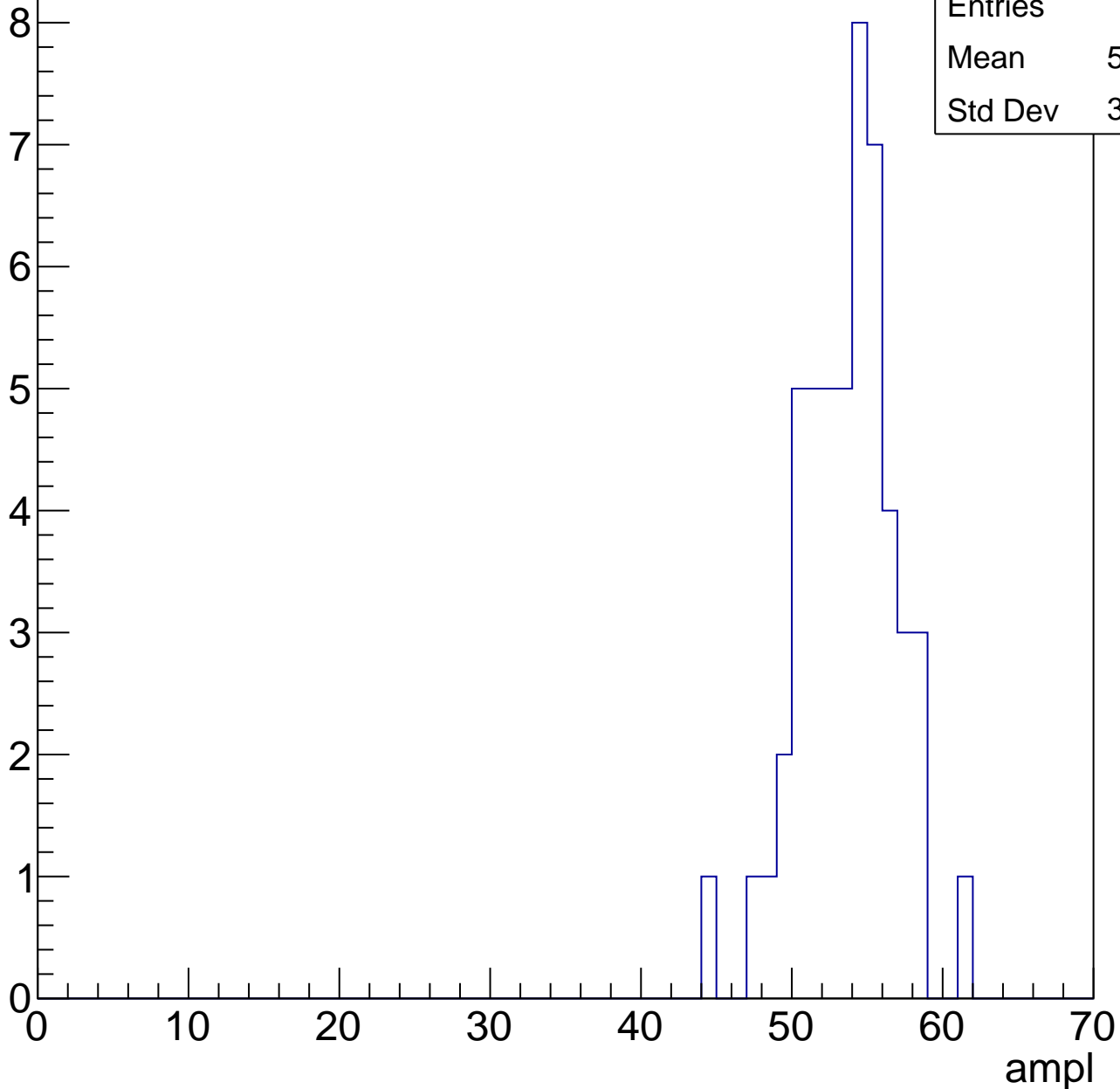


# B1L101S, U11-ch110, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	53.22
Std Dev	3.133

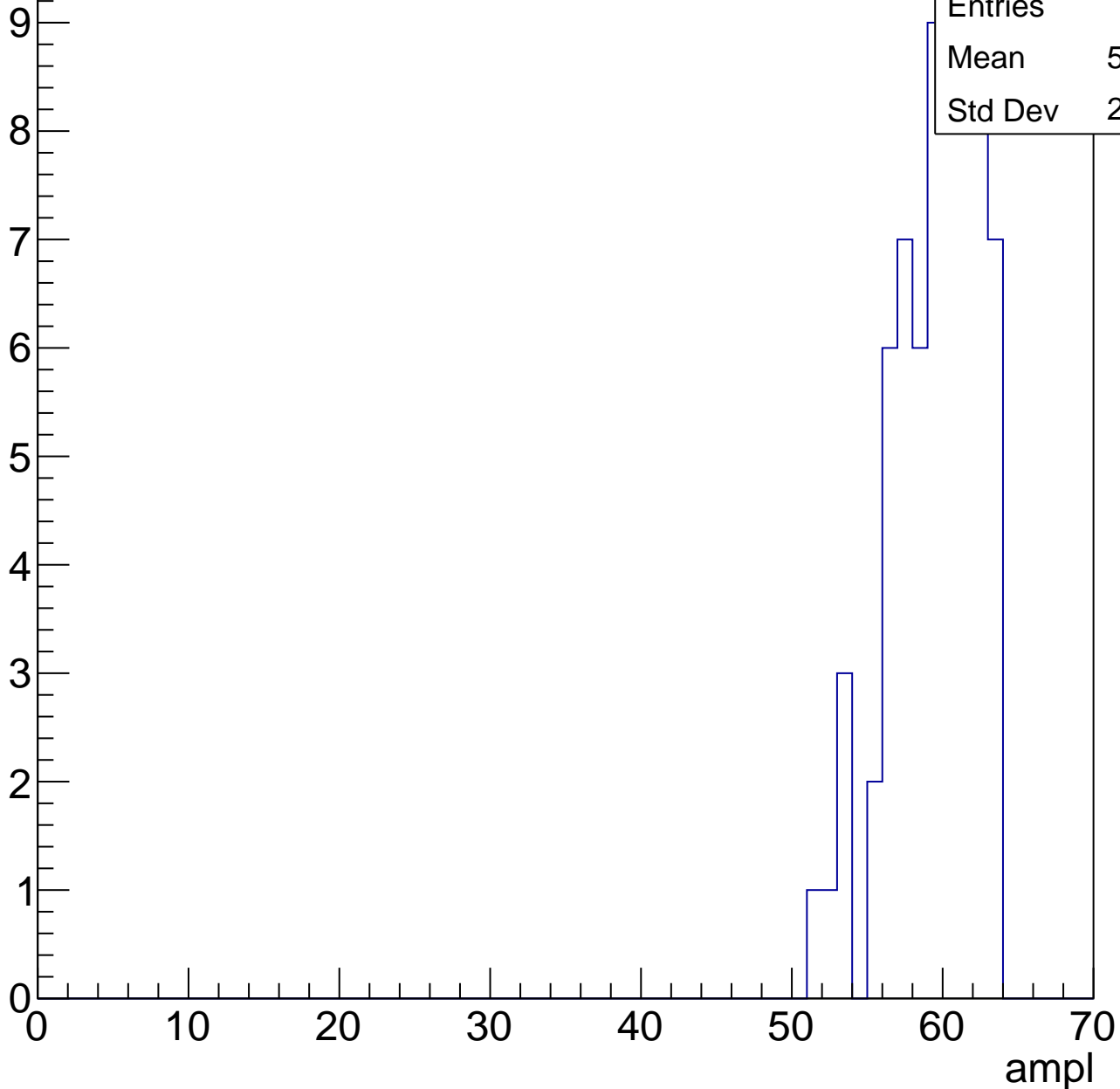


# B1L101S, U11-ch110, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	58.97
Std Dev	2.906



# B1L101S, U11-ch110, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

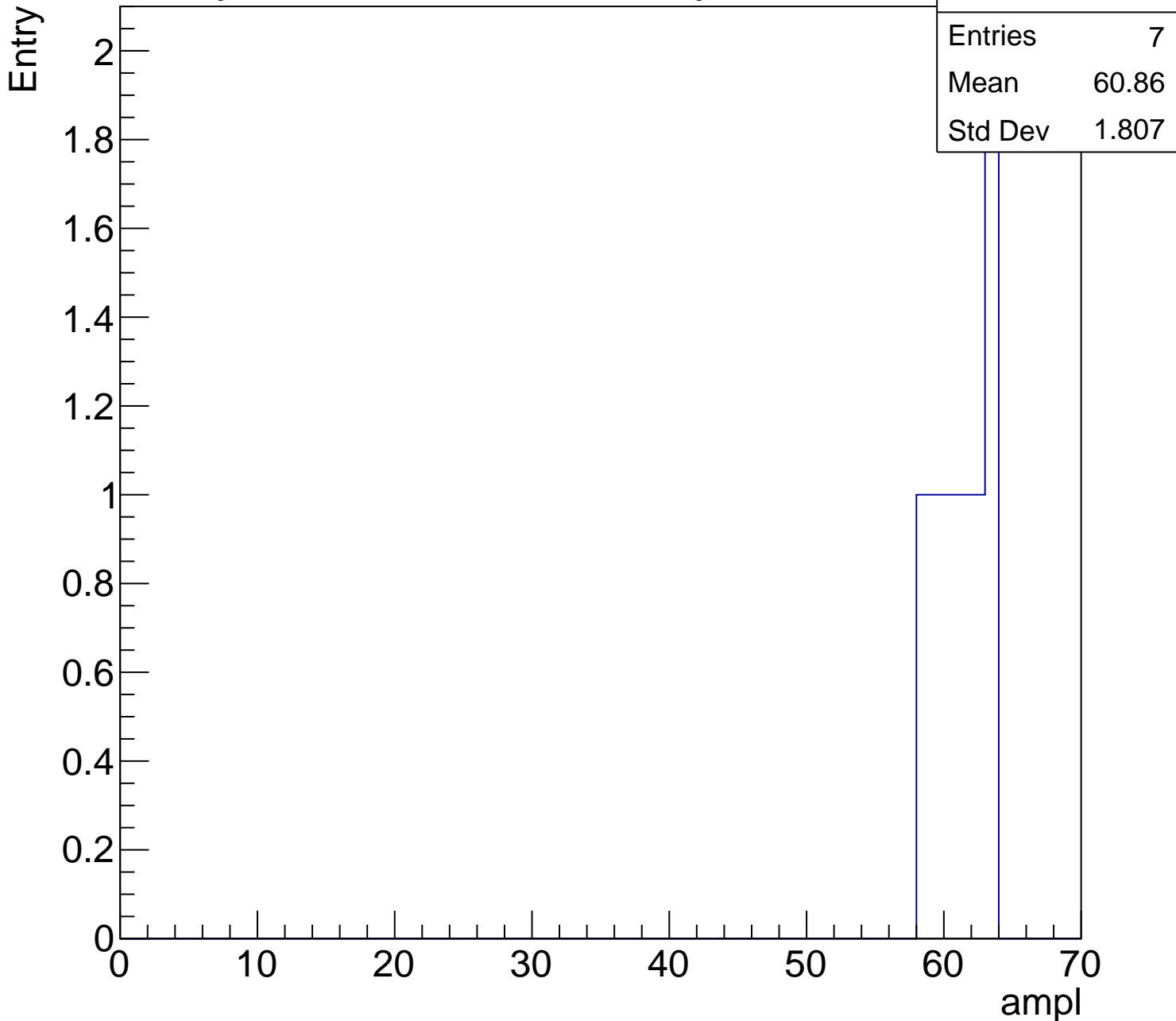
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	7
Mean	60.86
Std Dev	1.807

ampl

0 10 20 30 40 50 60 70

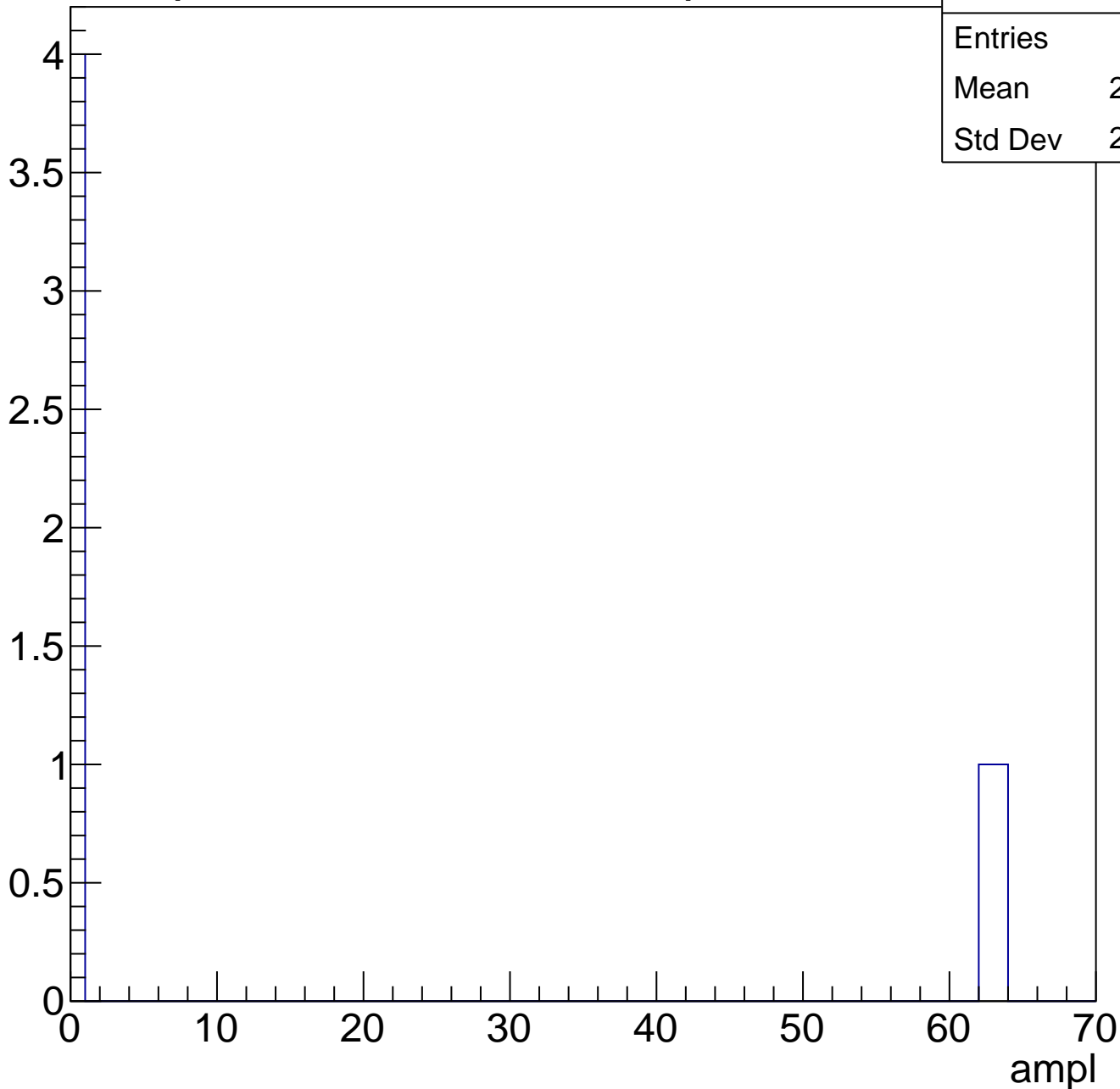




# B1L101S, U11-ch110, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U11-ch111, adc0

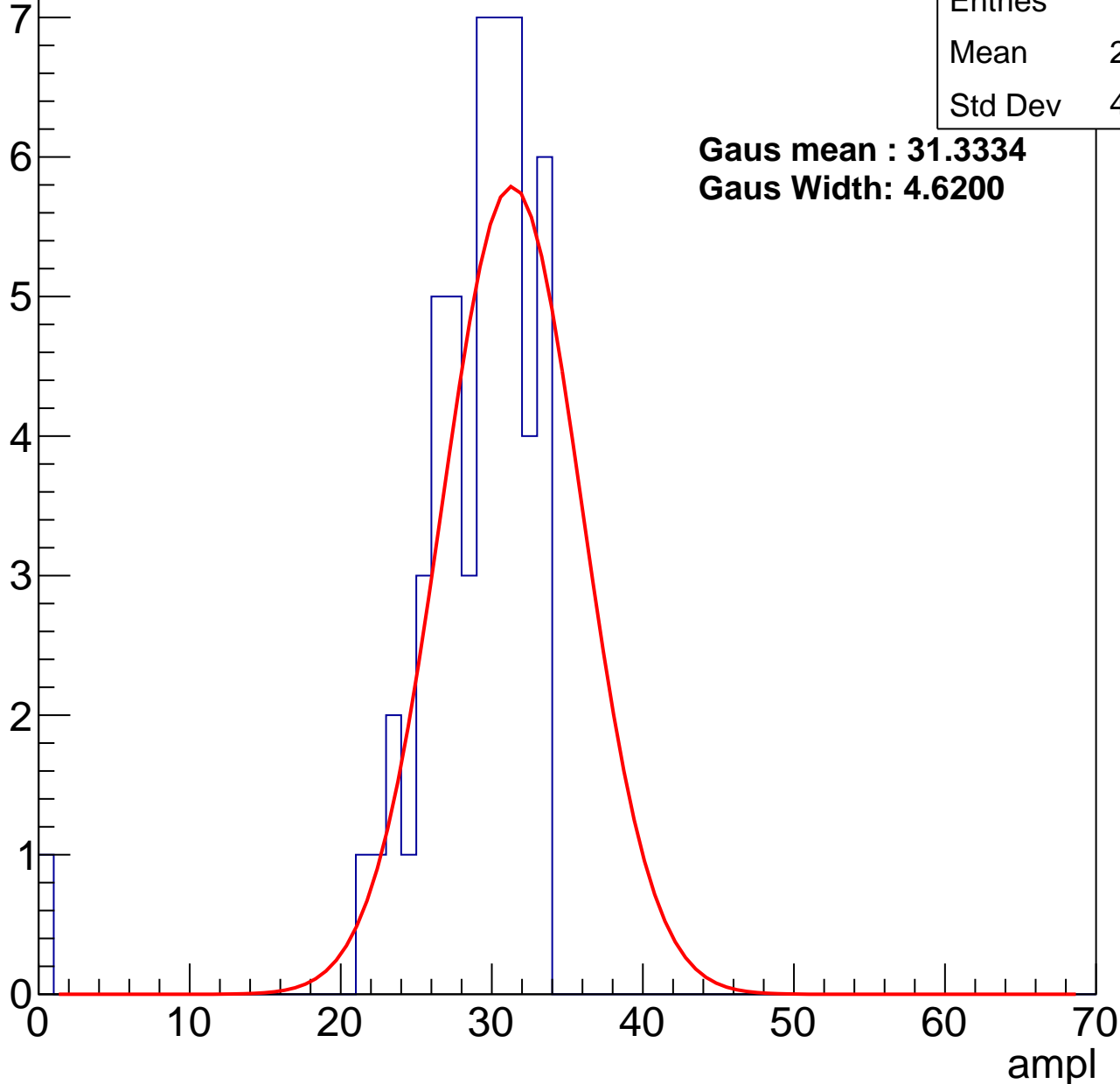
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	28.17
Std Dev	4.948

**Gaus mean : 31.3334**

**Gaus Width: 4.6200**



# B1L101S, U11-ch111, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	82
Mean	36.35
Std Dev	3.251

**Gaus mean : 36.8954**

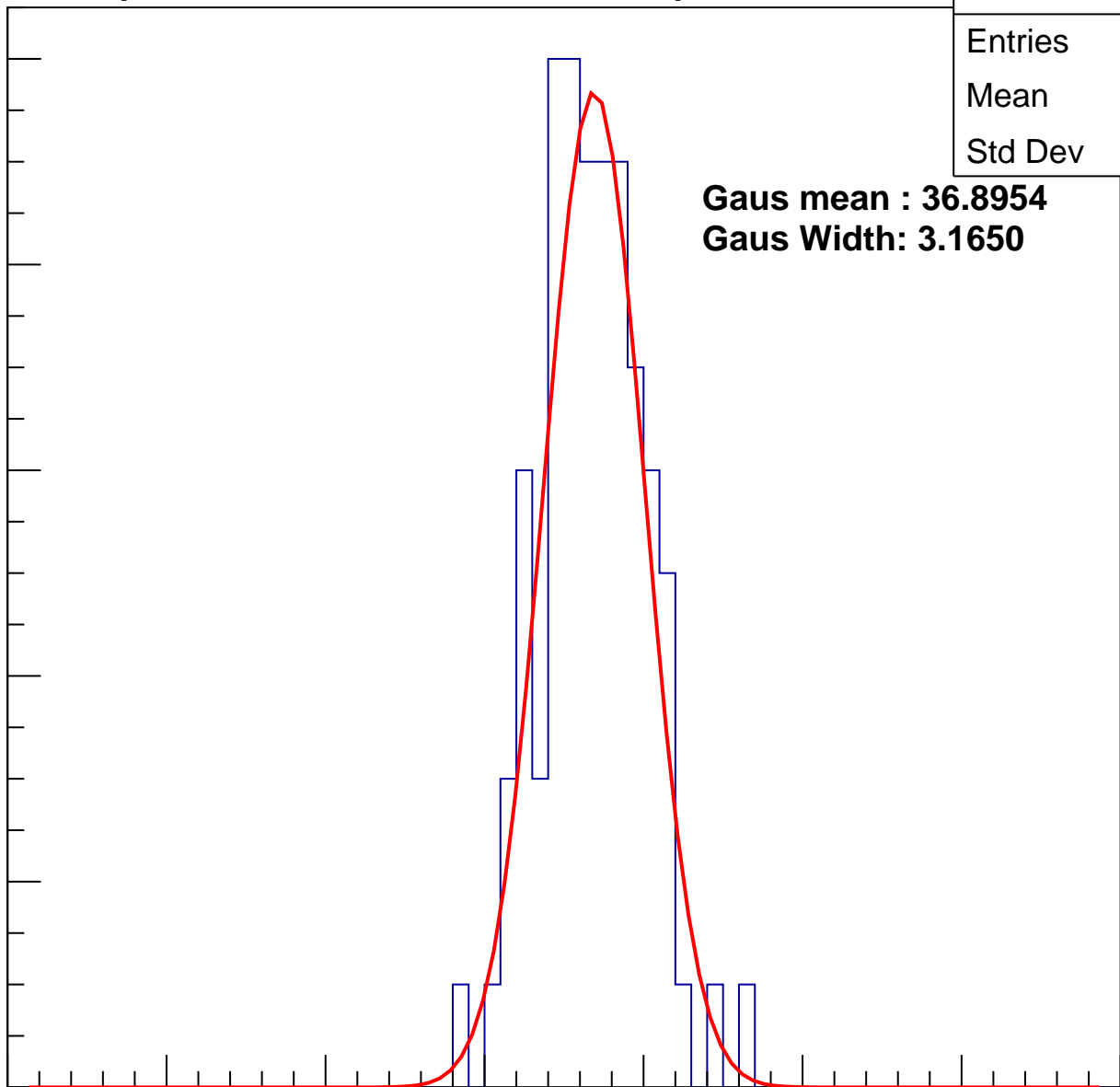
**Gaus Width: 3.1650**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L101S, U11-ch111, adc2

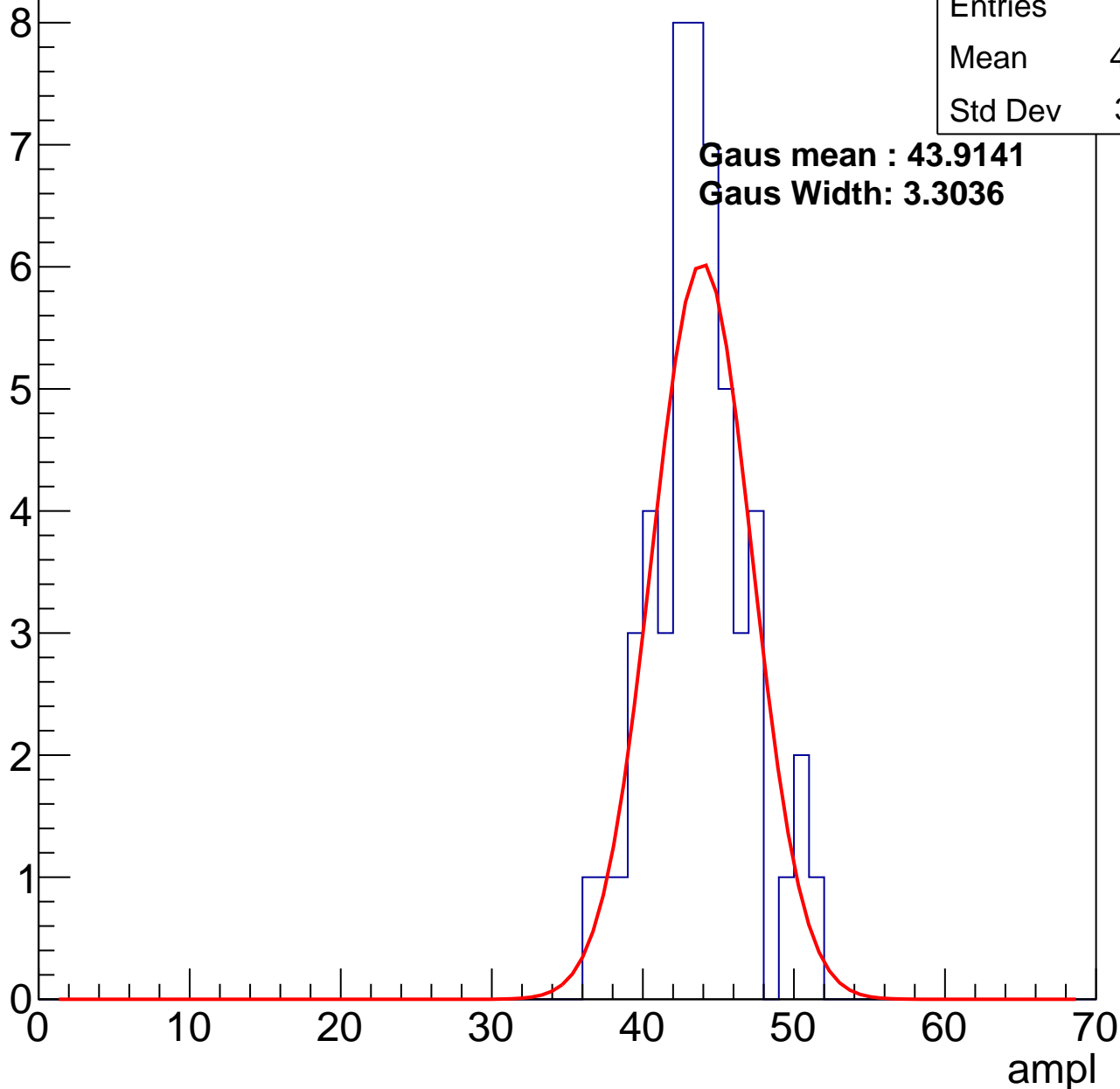
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	43.27
Std Dev	3.181

**Gaus mean : 43.9141**

**Gaus Width: 3.3036**



# B1L101S, U11-ch111, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

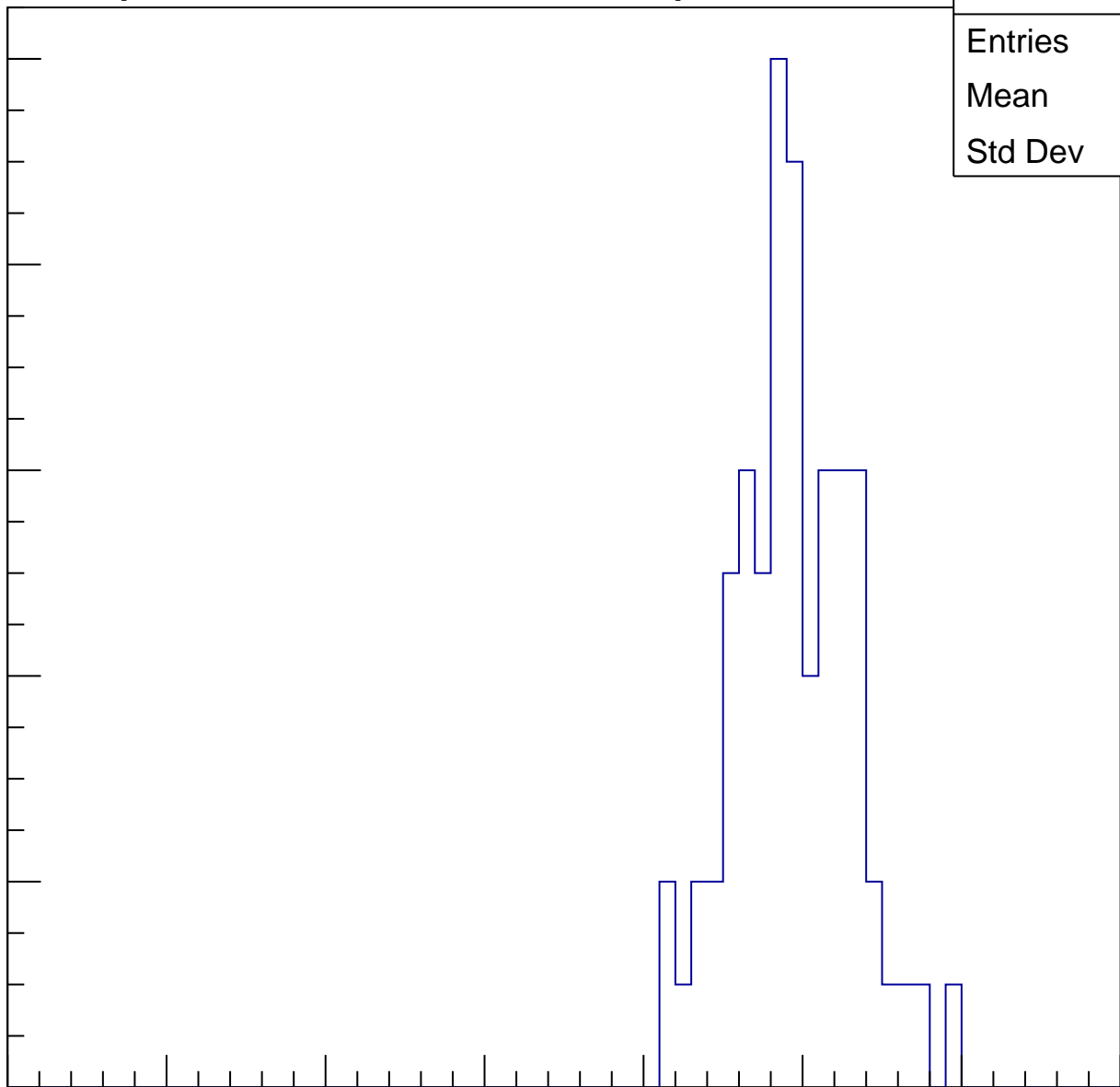
Entries	70
Mean	48.94
Std Dev	3.664

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

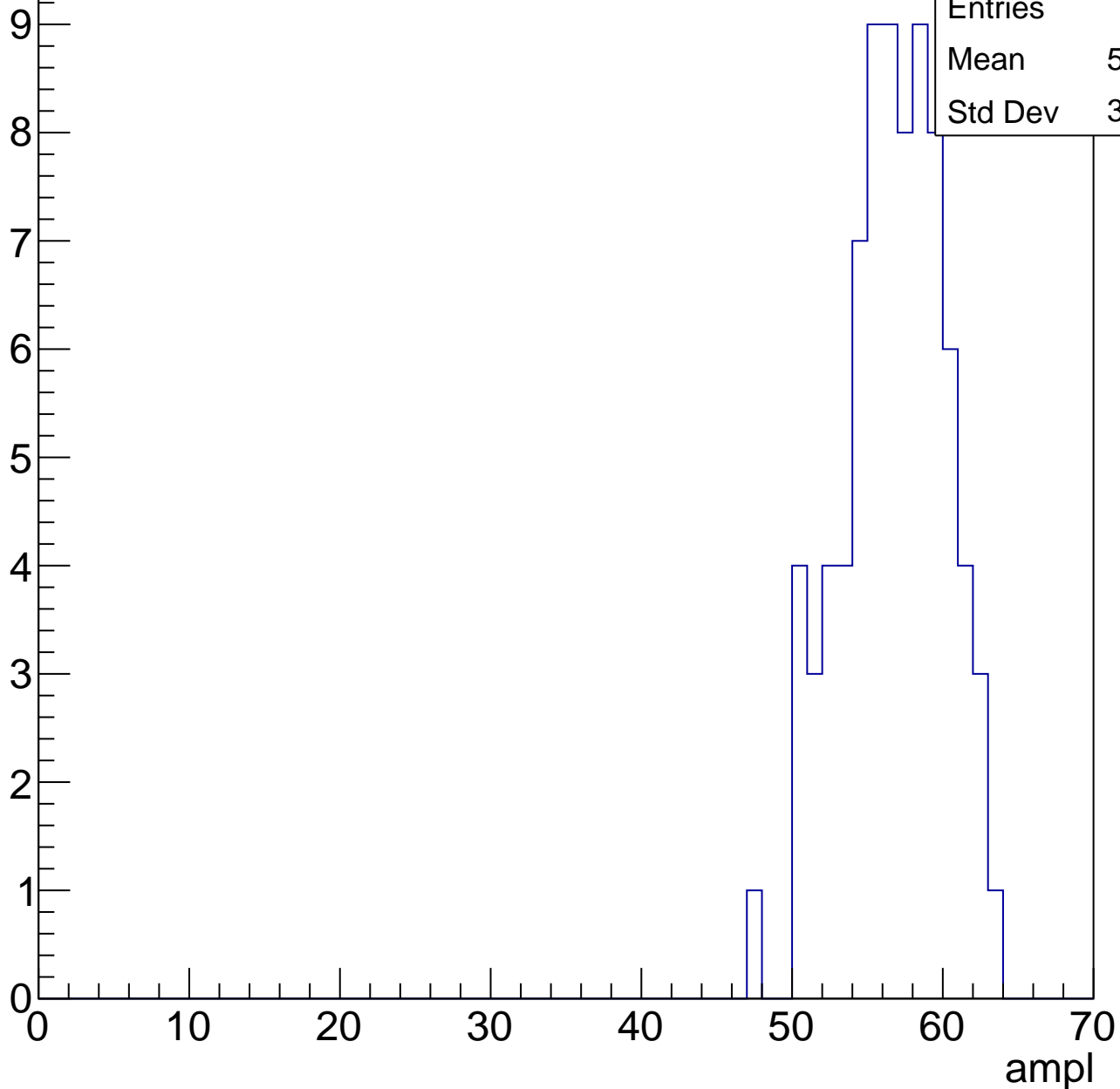
ampl



# B1L101S, U11-ch111, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



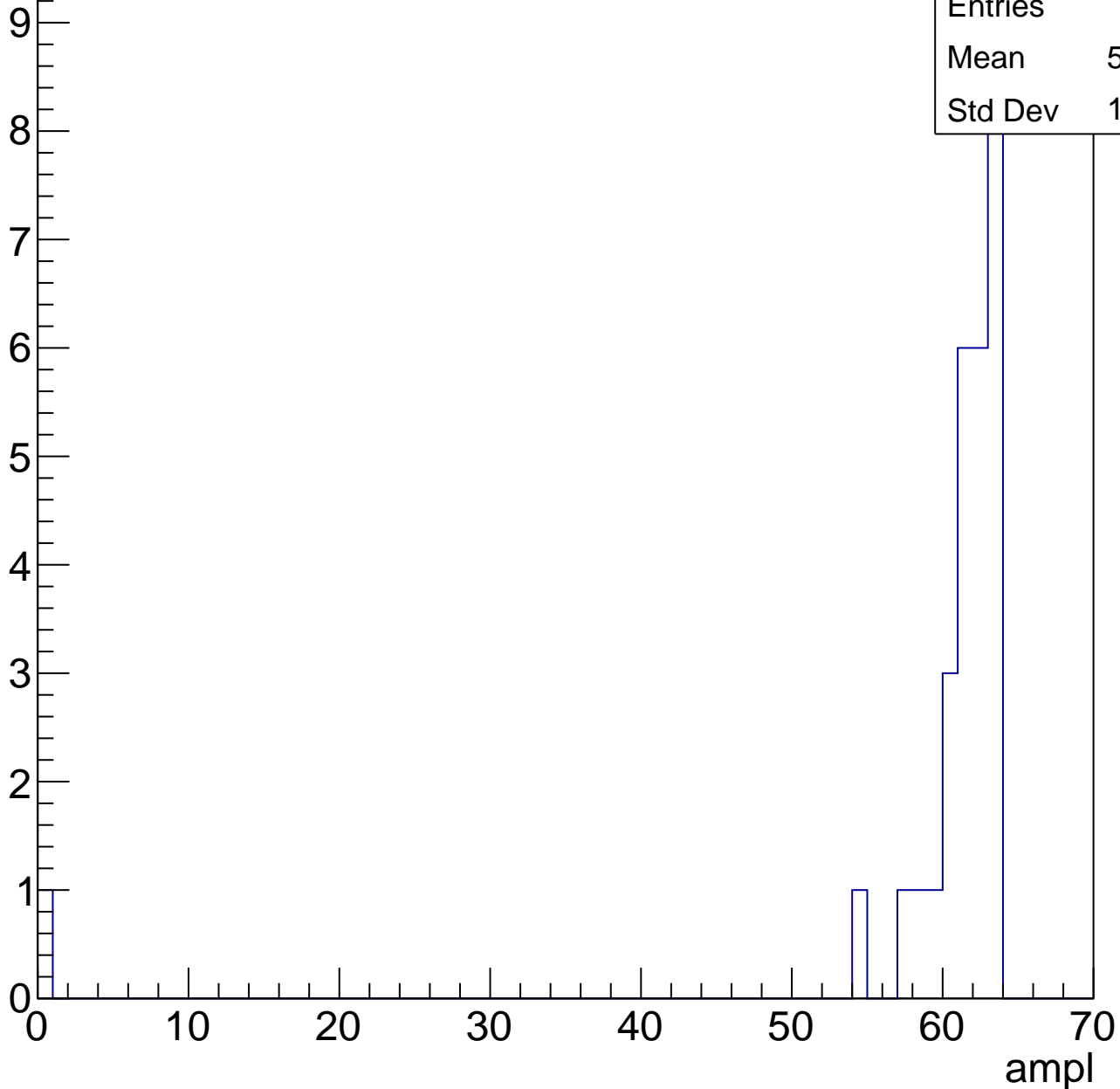
Entries	80
Mean	56.25
Std Dev	3.356

# B1L101S, U11-ch111, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	29
Mean	59.07
Std Dev	11.35



# B1L101S, U11-ch111, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch111, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U11-ch112, adc0

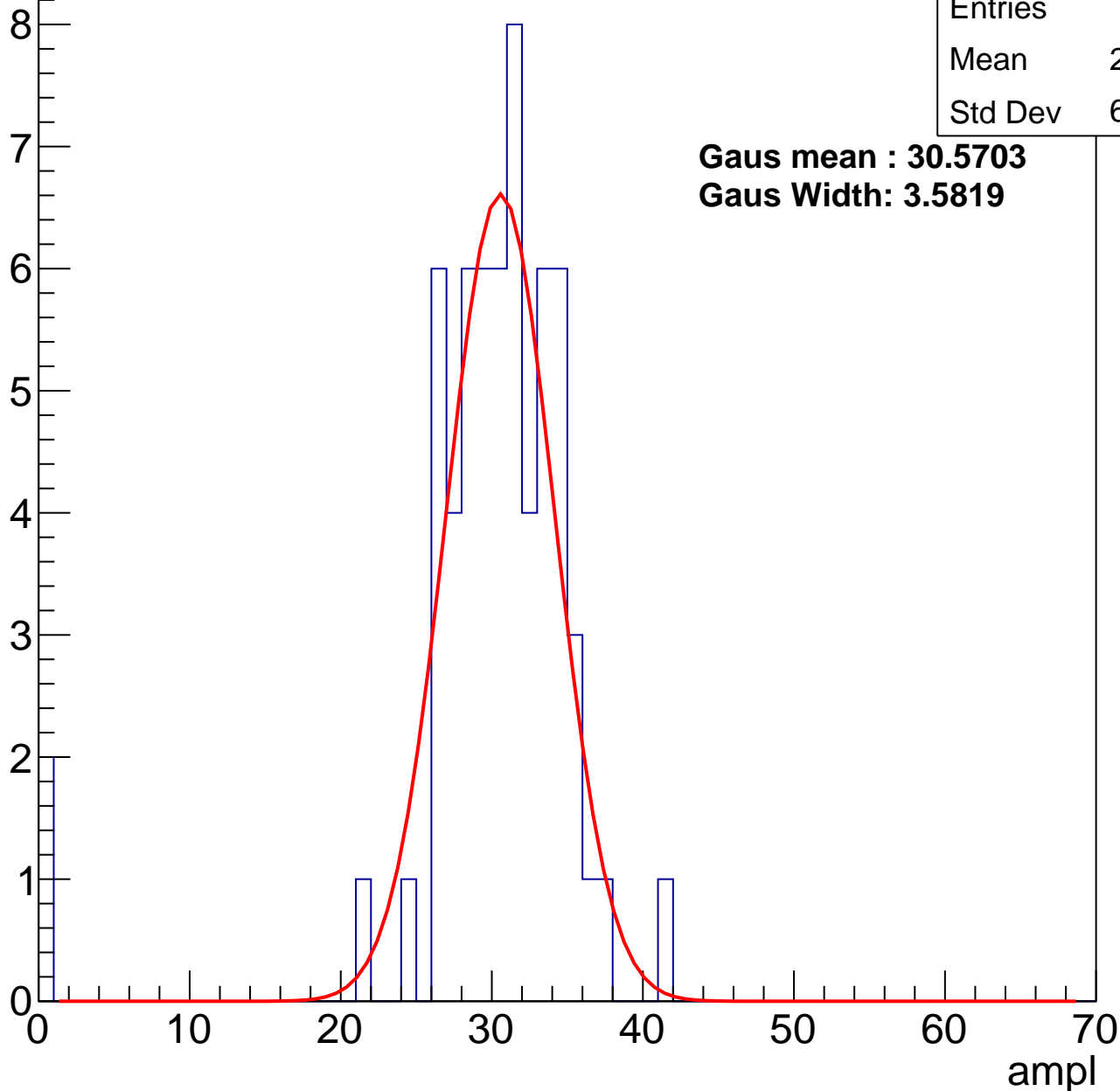
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	29.48
Std Dev	6.372

**Gaus mean : 30.5703**

**Gaus Width: 3.5819**



# B1L101S, U11-ch112, adc1

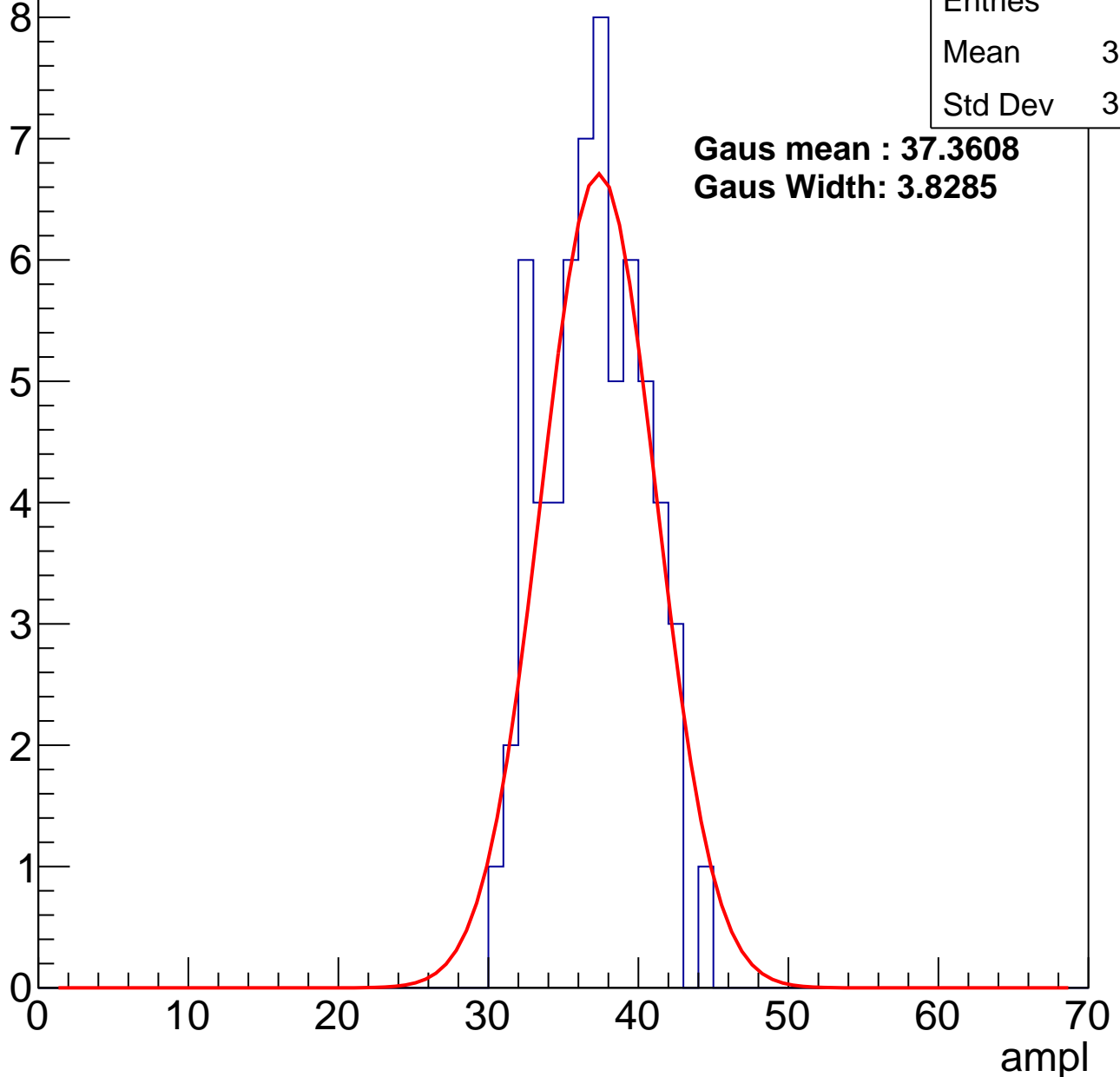
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	36.58
Std Dev	3.246

**Gaus mean : 37.3608**

**Gaus Width: 3.8285**



# B1L101S, U11-ch112, adc2

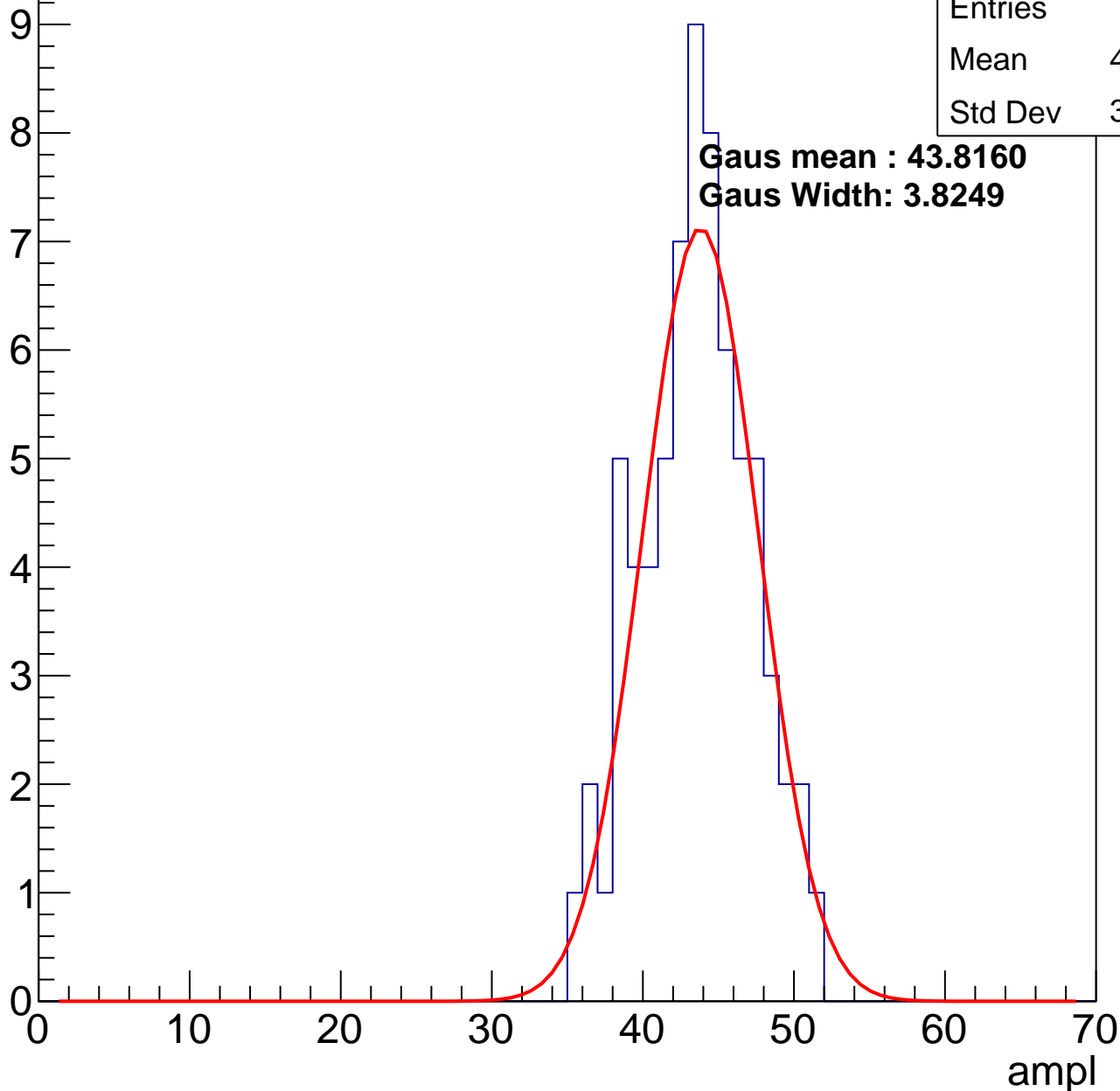
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	43.09
Std Dev	3.616

**Gaus mean : 43.8160**

**Gaus Width: 3.8249**

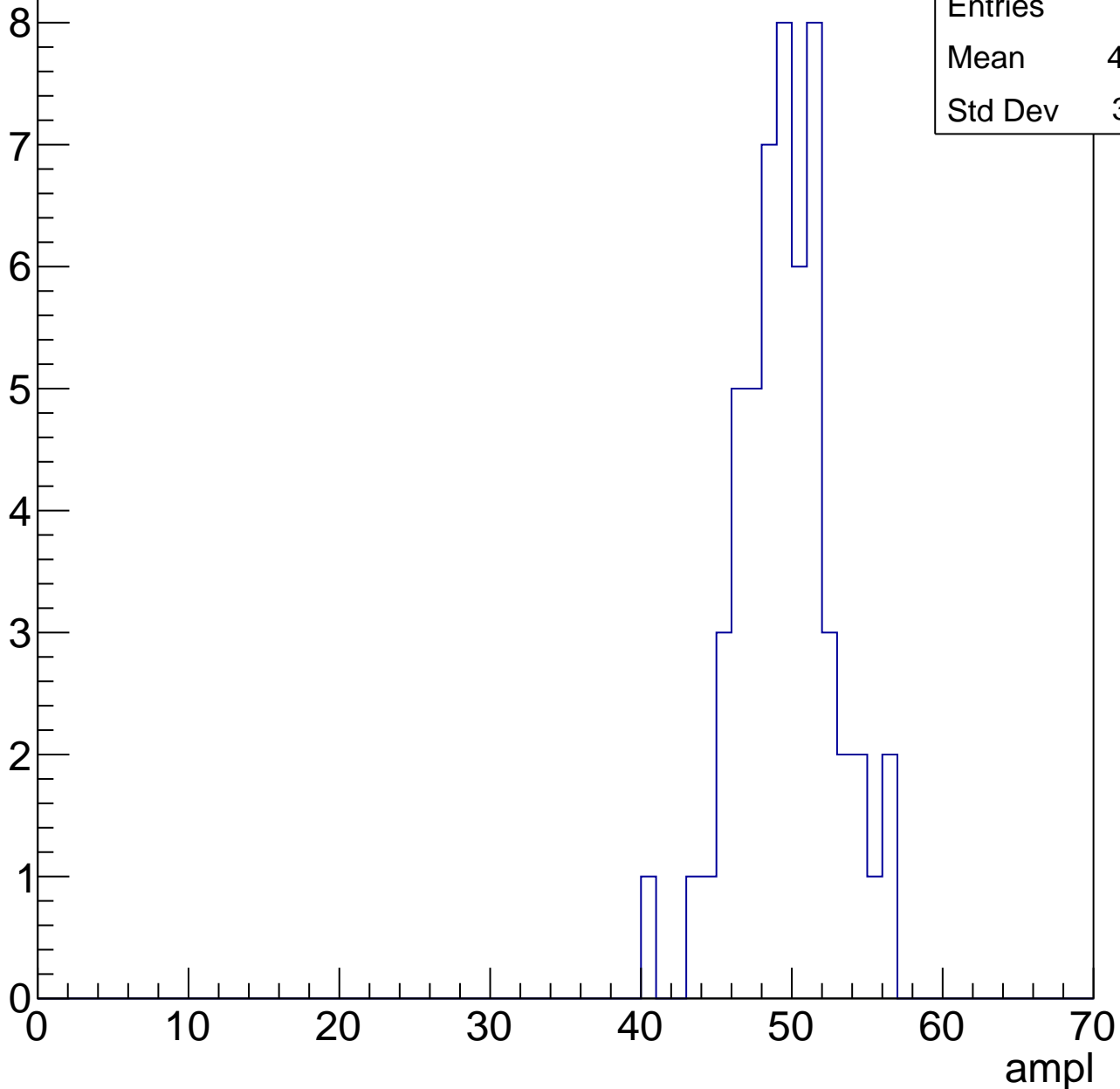


# B1L101S, U11-ch112, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	49.09
Std Dev	3.141

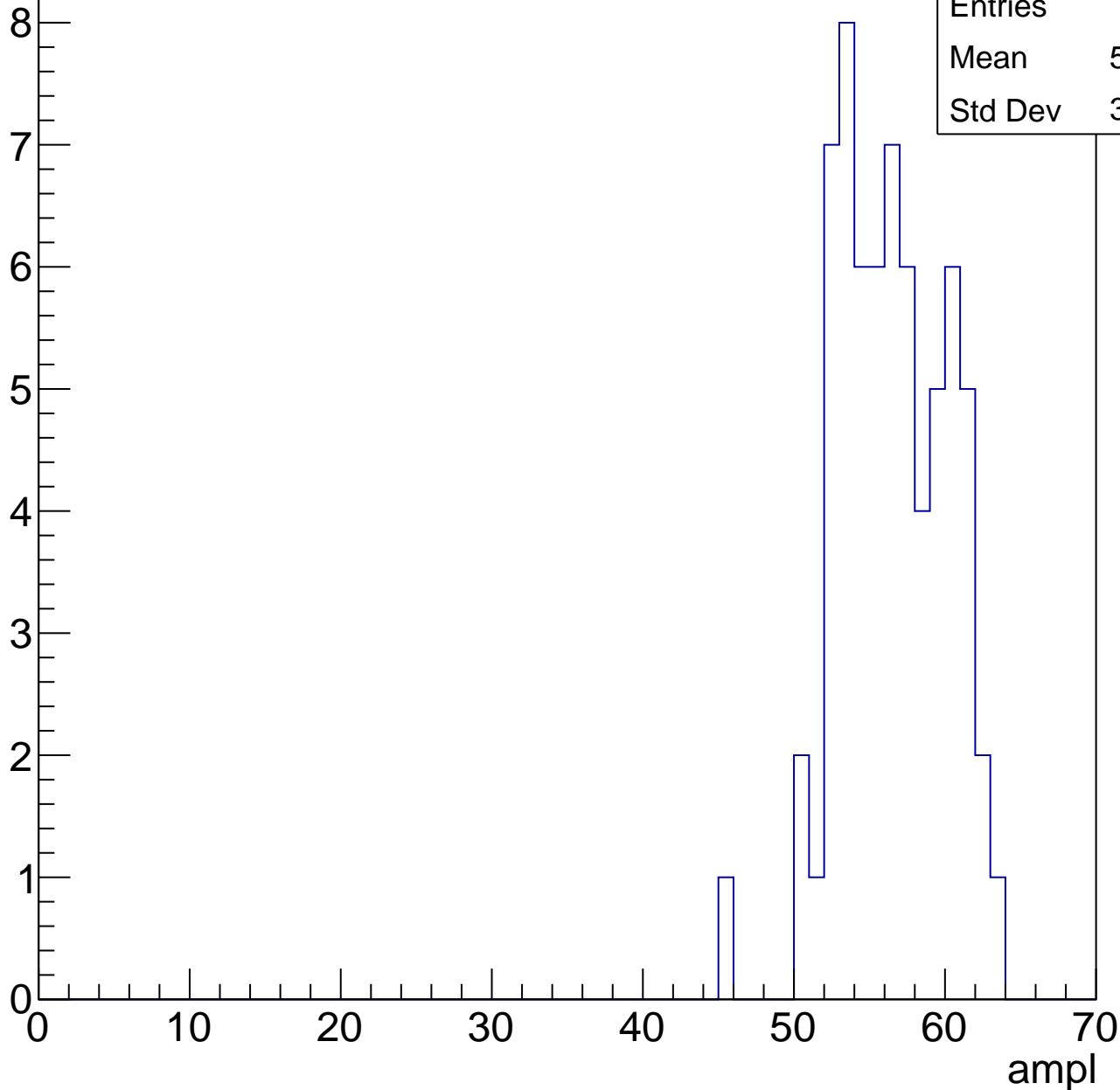


# B1L101S, U11-ch112, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	55.99
Std Dev	3.543

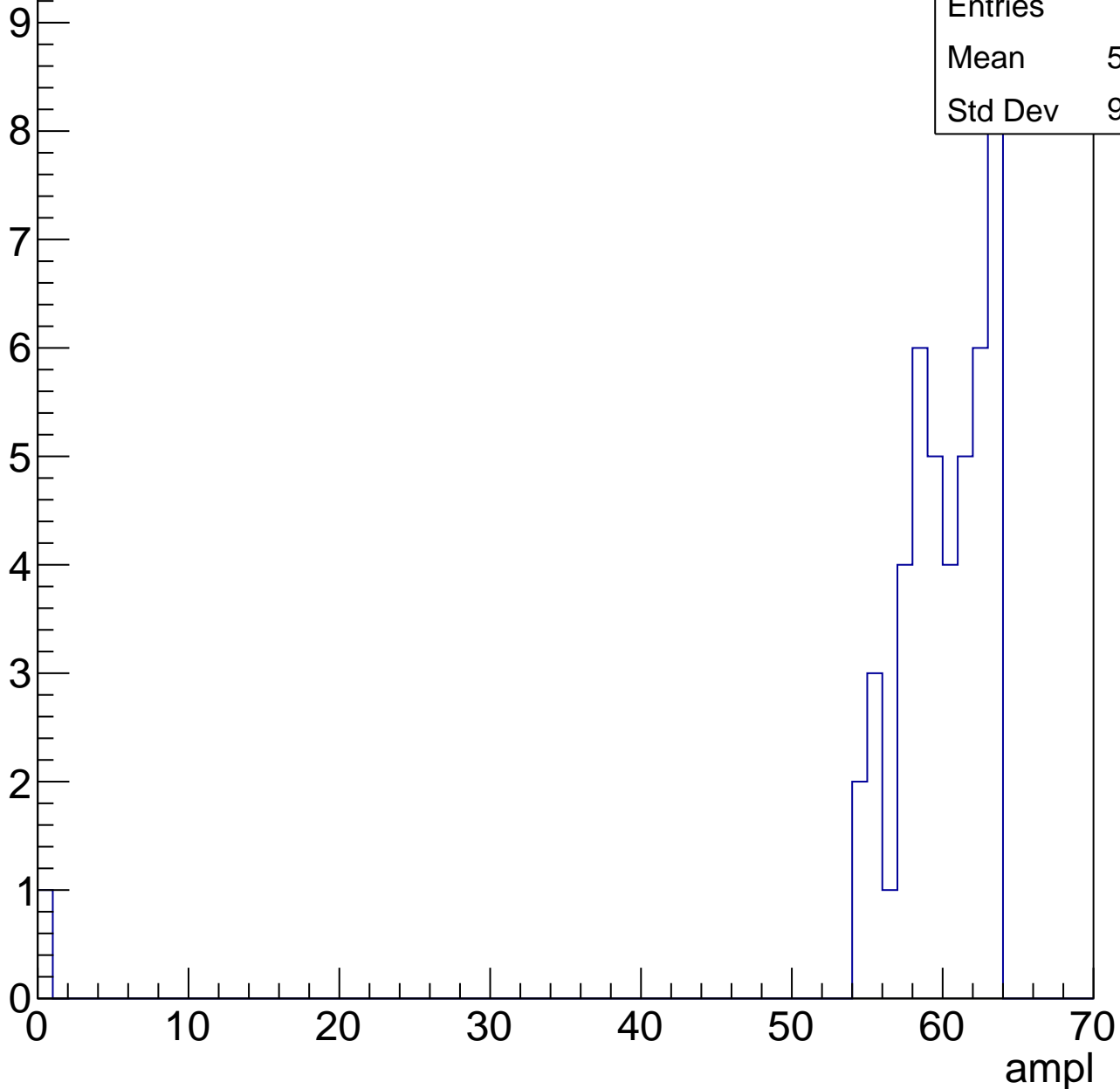


# B1L101S, U11-ch112, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	46
Mean	58.35
Std Dev	9.104



# B1L101S, U11-ch112, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch112, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	10.5
Std Dev	10.5

# B1L101S, U11-ch113, adc0

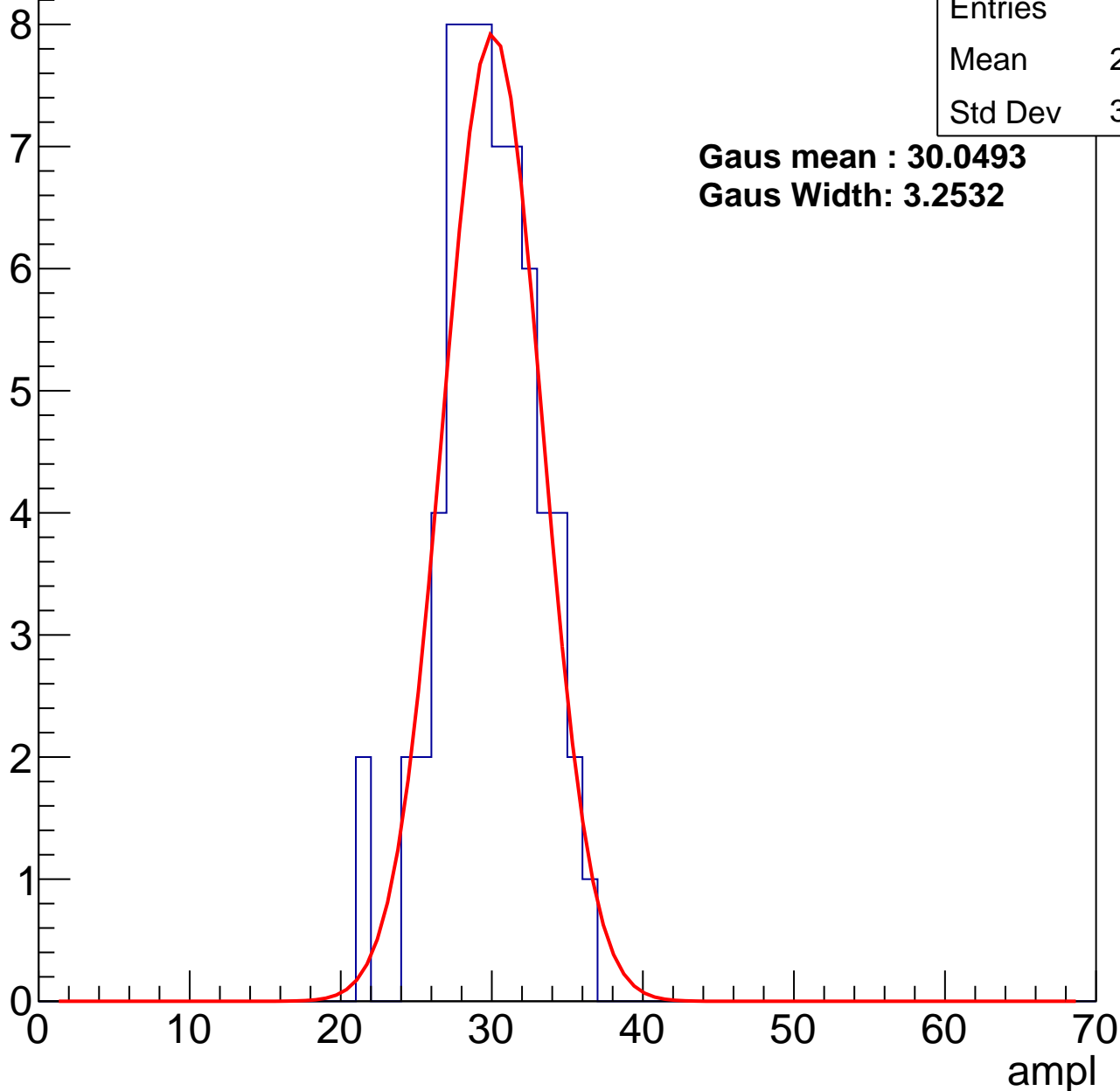
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	29.37
Std Dev	3.165

**Gaus mean : 30.0493**

**Gaus Width: 3.2532**



# B1L101S, U11-ch113, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	70
Mean	35.93
Std Dev	3.42

**Gaus mean : 36.4983**

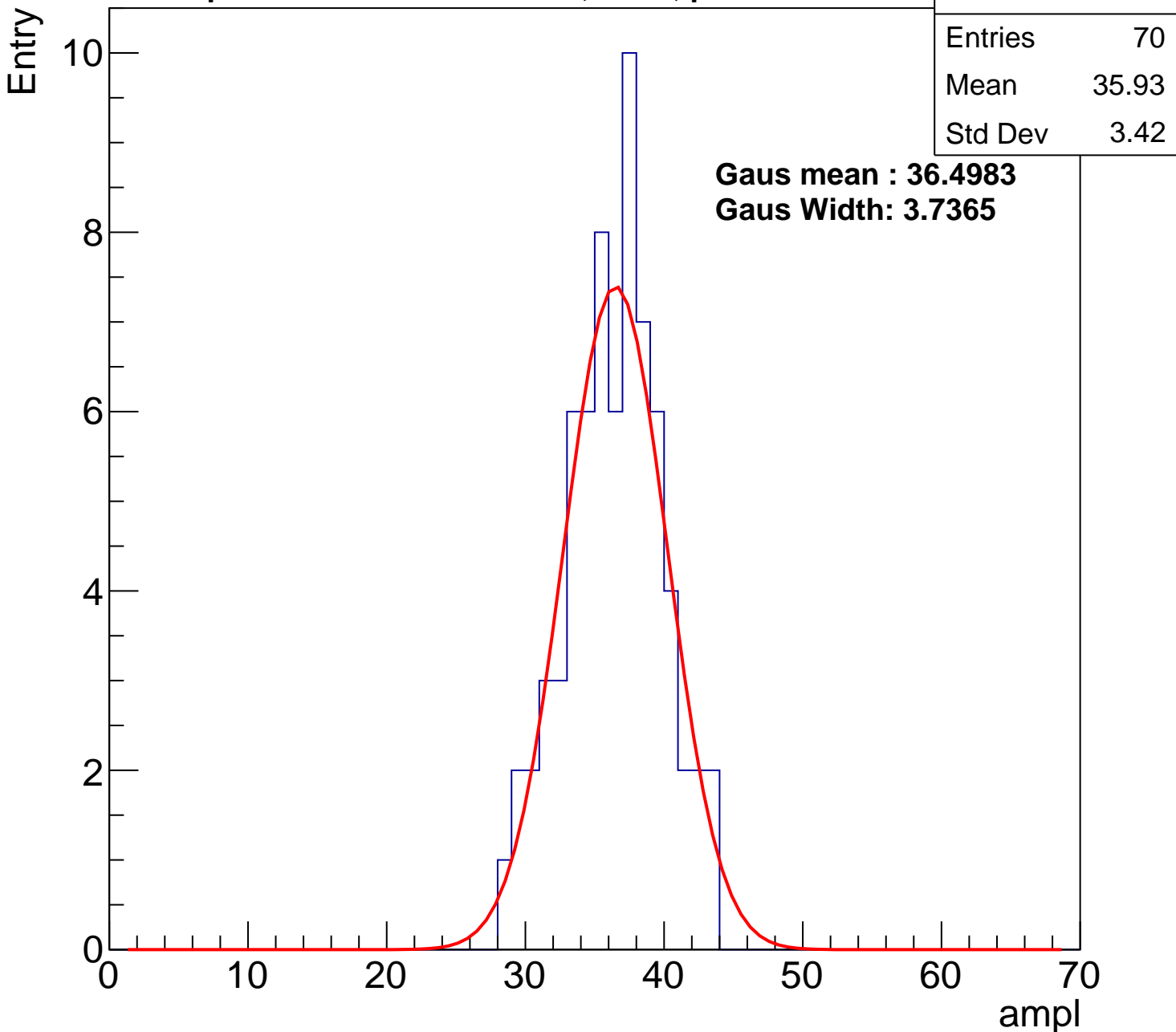
**Gaus Width: 3.7365**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L101S, U11-ch113, adc2

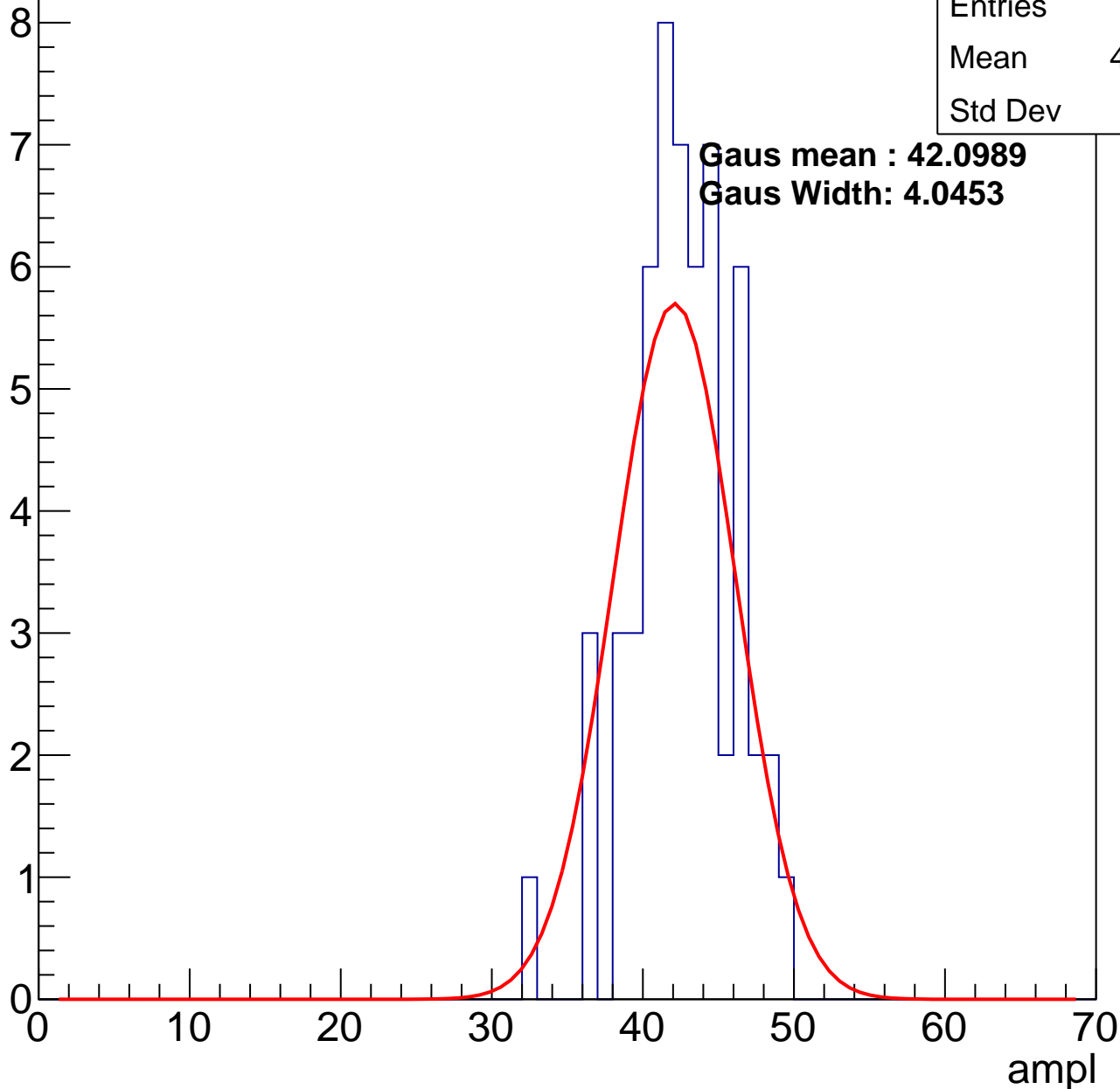
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	42.18
Std Dev	3.33

**Gaus mean : 42.0989**

**Gaus Width: 4.0453**

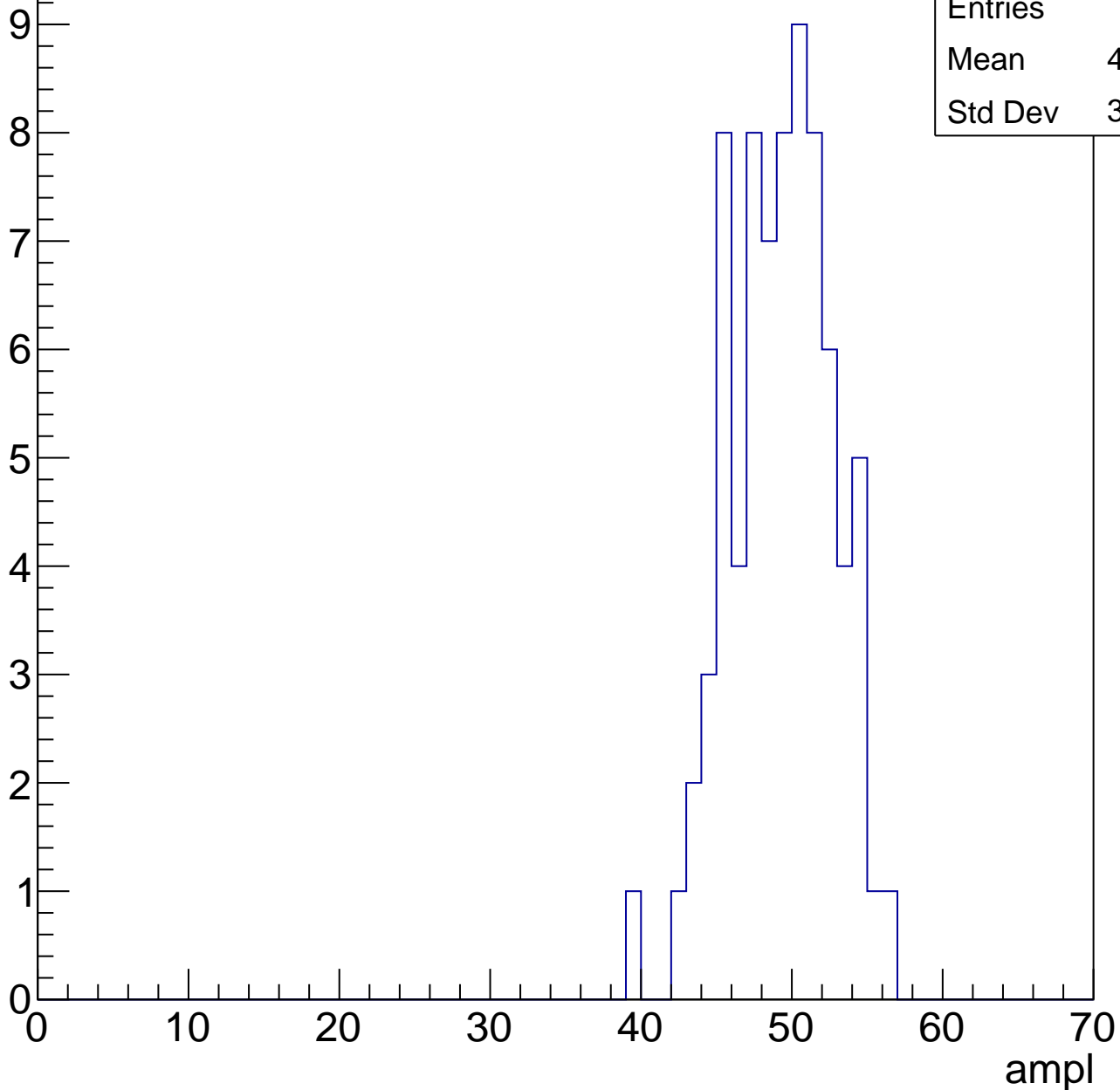


# B1L101S, U11-ch113, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

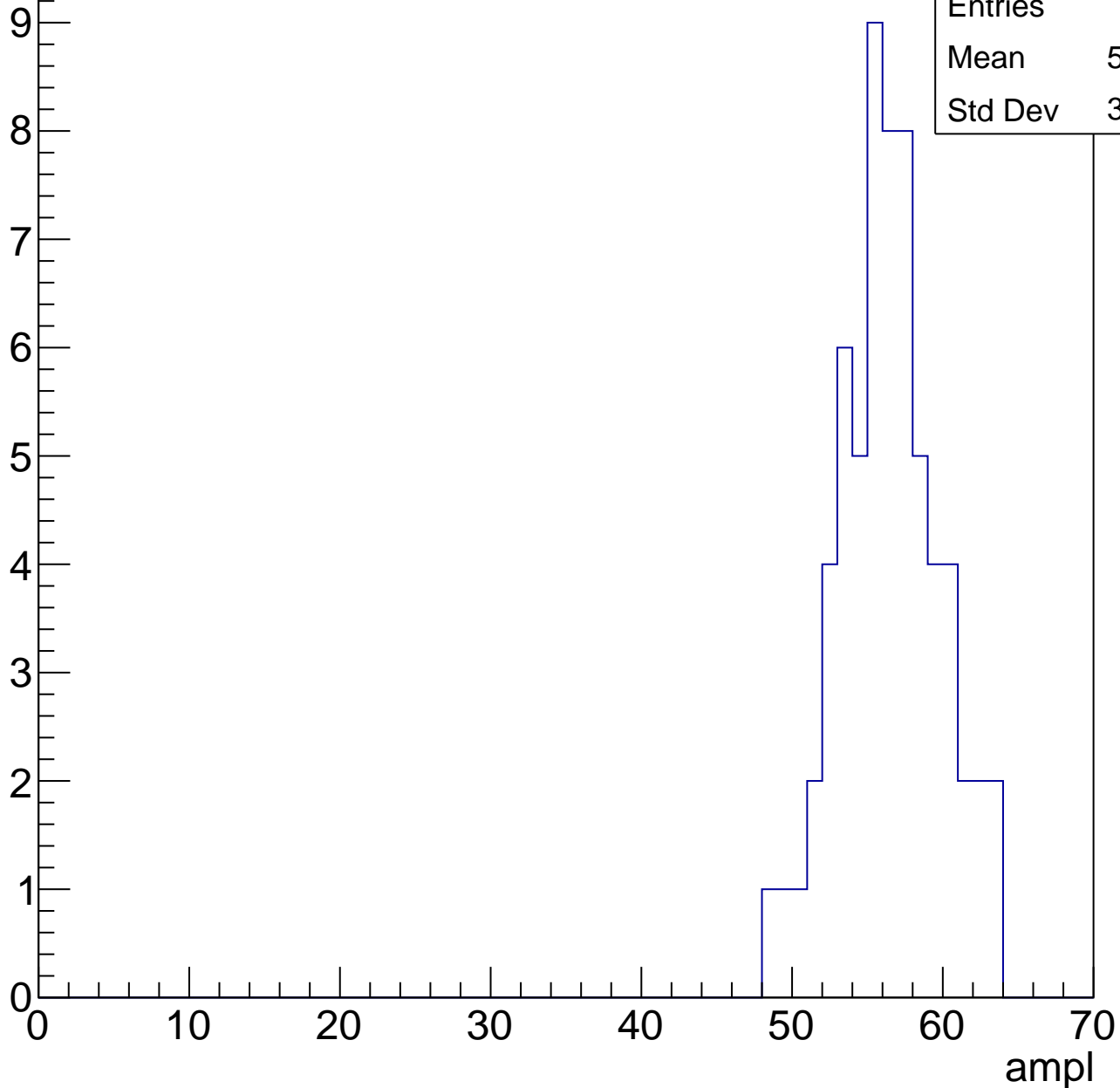
Entries	76
Mean	48.82
Std Dev	3.374



# B1L101S, U11-ch113, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



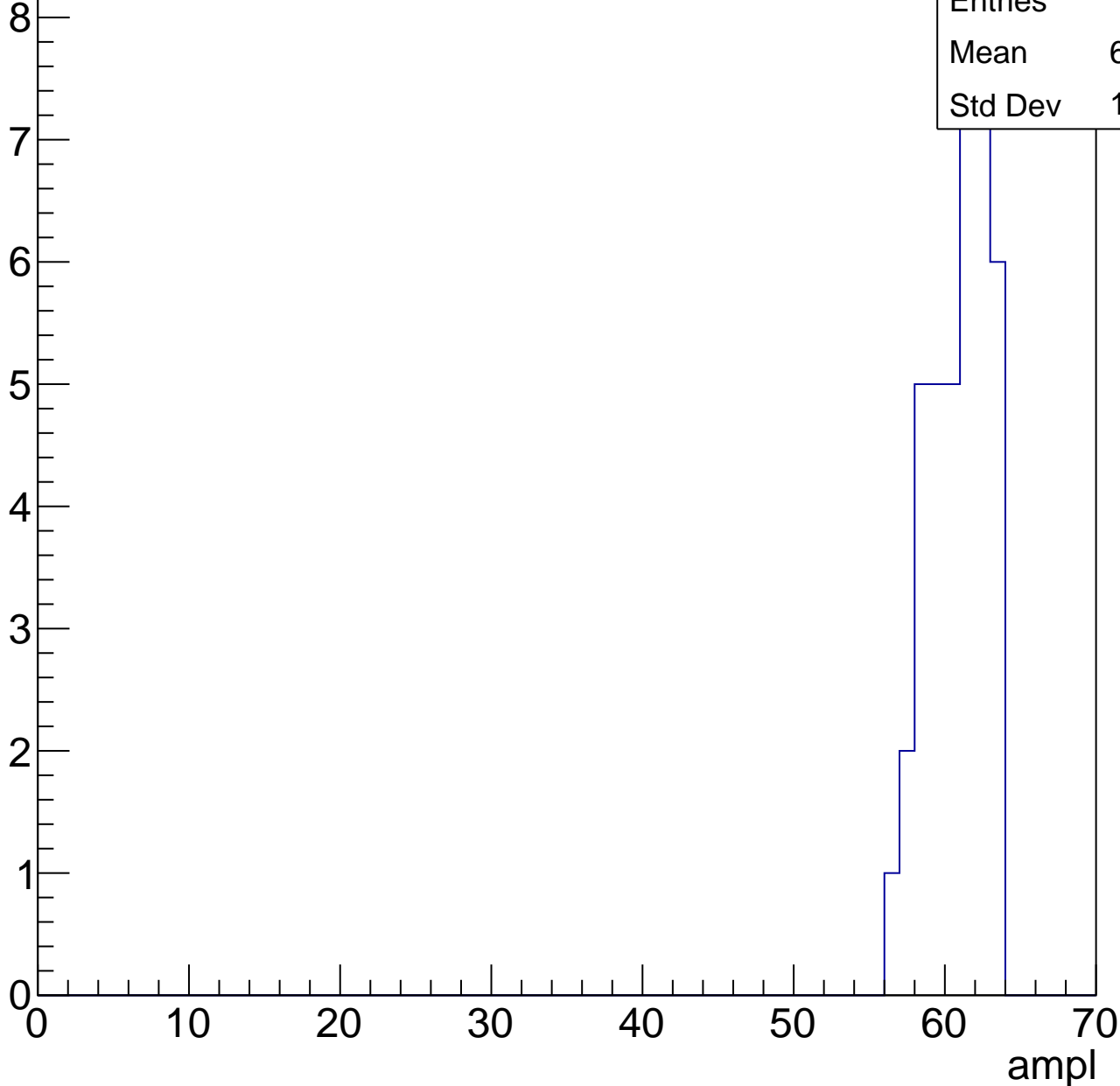
Entries	64
Mean	55.97
Std Dev	3.293

# B1L101S, U11-ch113, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

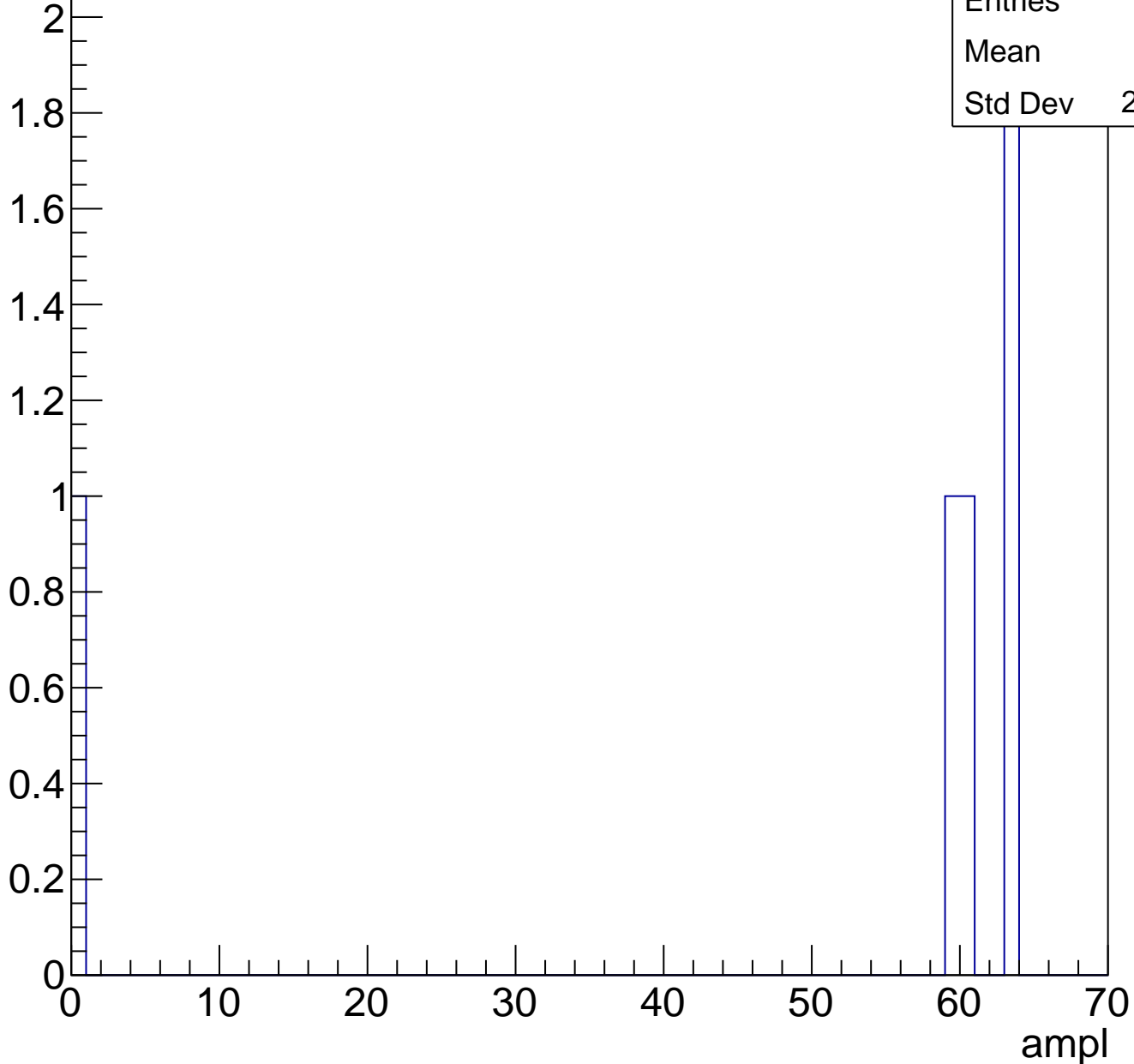
Entries	40
Mean	60.42
Std Dev	1.909



# B1L101S, U11-ch113, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch113, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U11-ch114, adc0

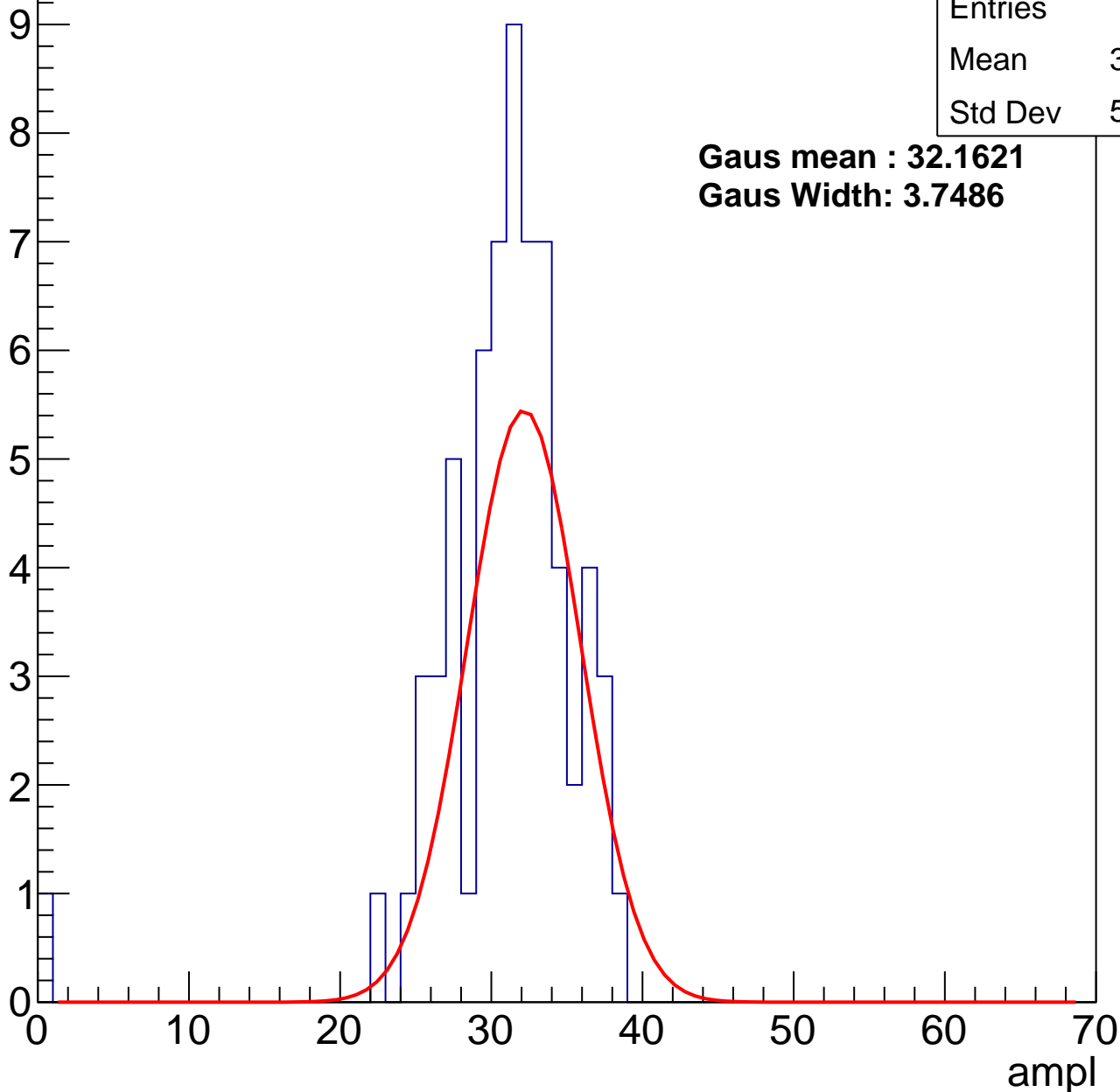
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	30.45
Std Dev	5.165

**Gaus mean : 32.1621**

**Gaus Width: 3.7486**

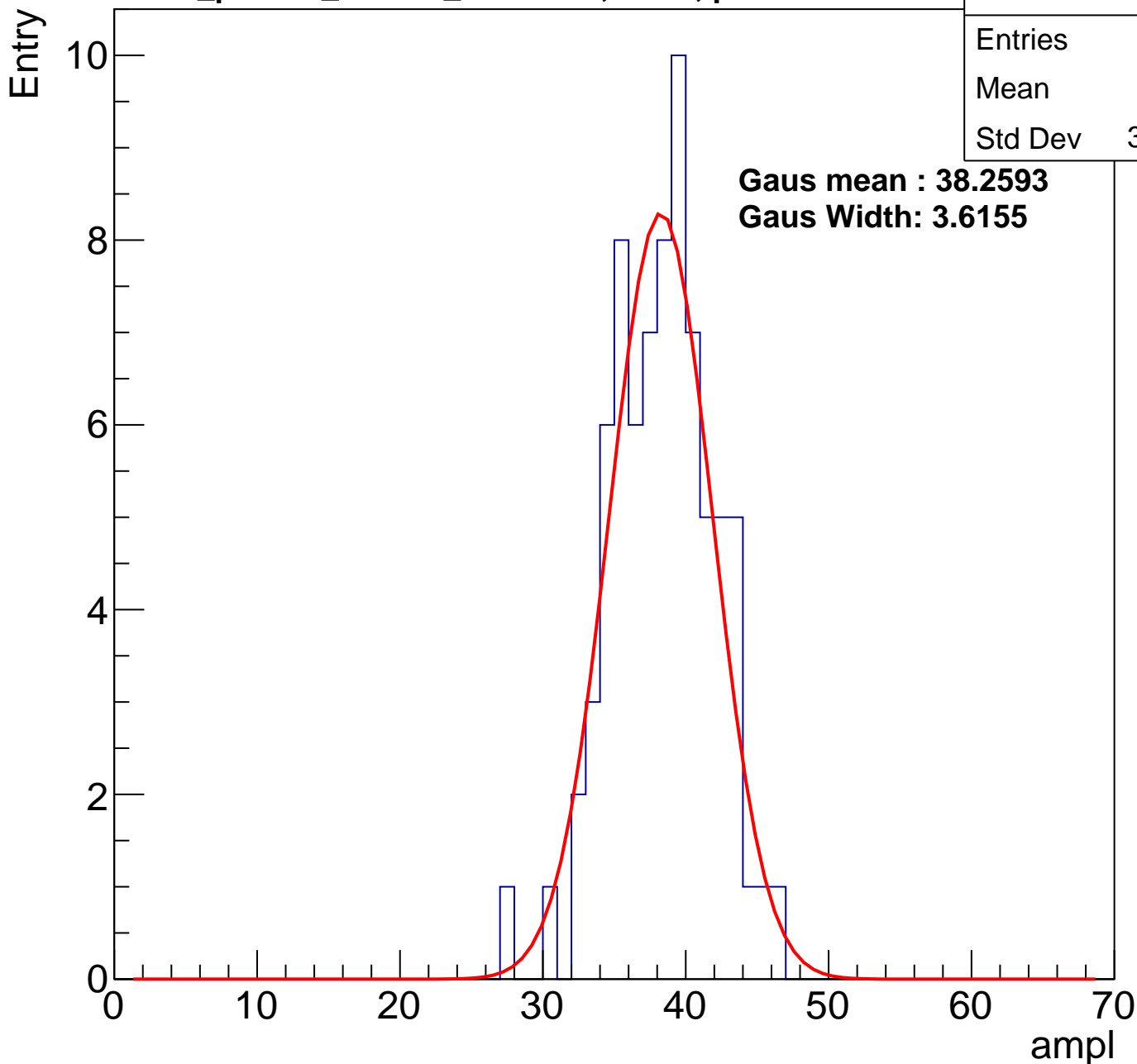


# B1L101S, U11-ch114, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	77
Mean	37.9
Std Dev	3.544

**Gaus mean : 38.2593**  
**Gaus Width: 3.6155**



# B1L101S, U11-ch114, adc2

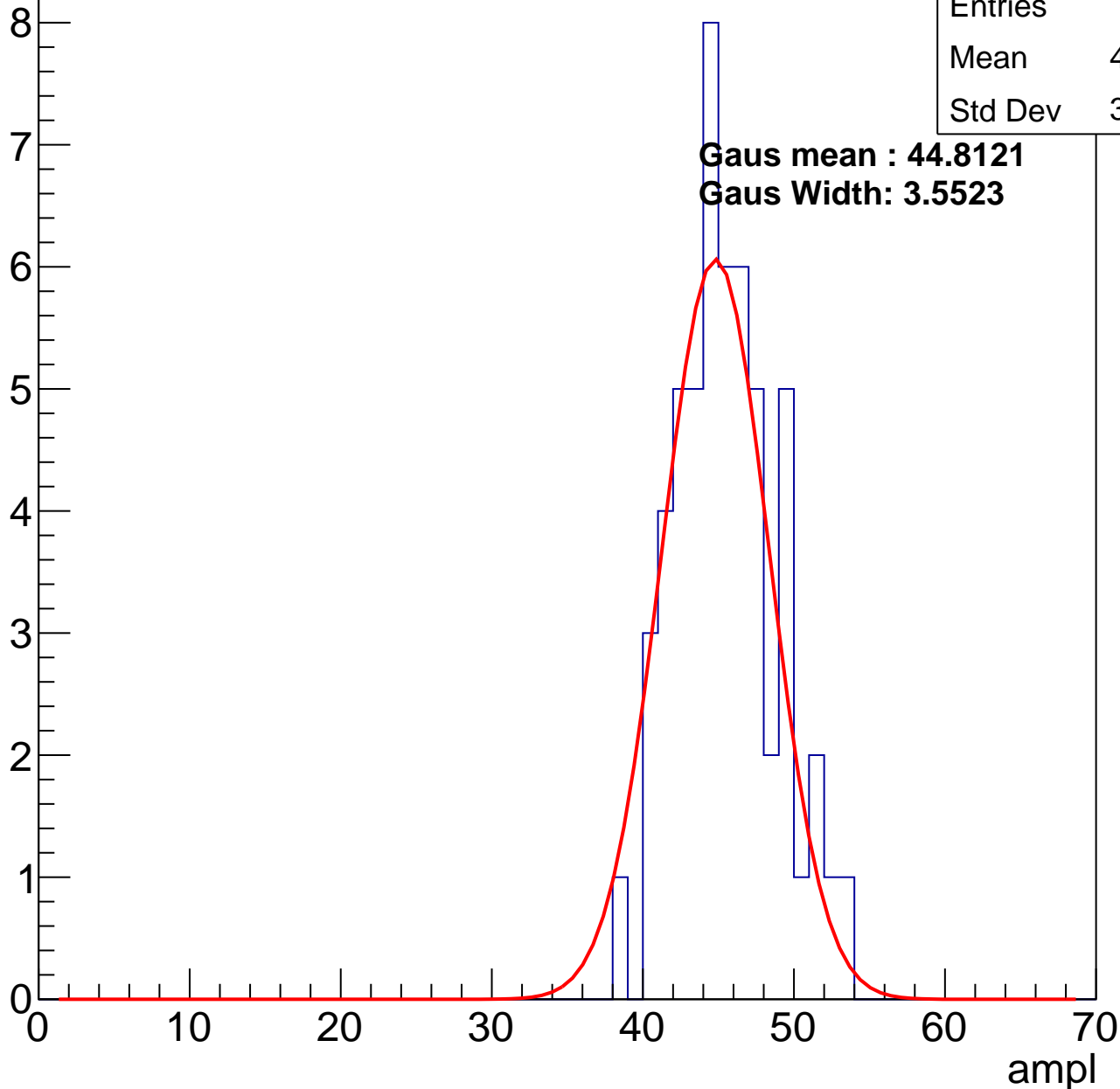
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	45.05
Std Dev	3.289

**Gaus mean : 44.8121**

**Gaus Width: 3.5523**

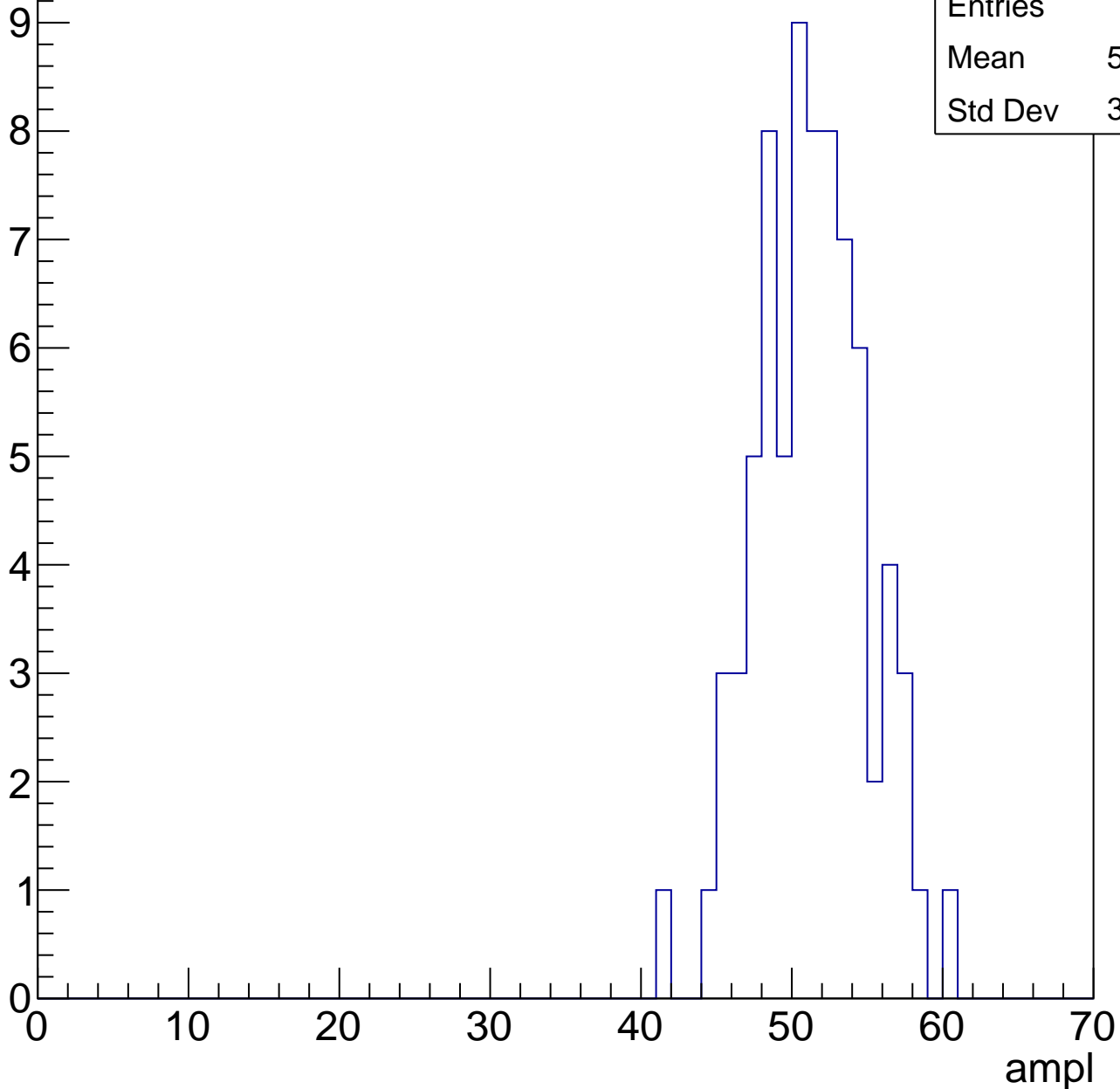


# B1L101S, U11-ch114, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

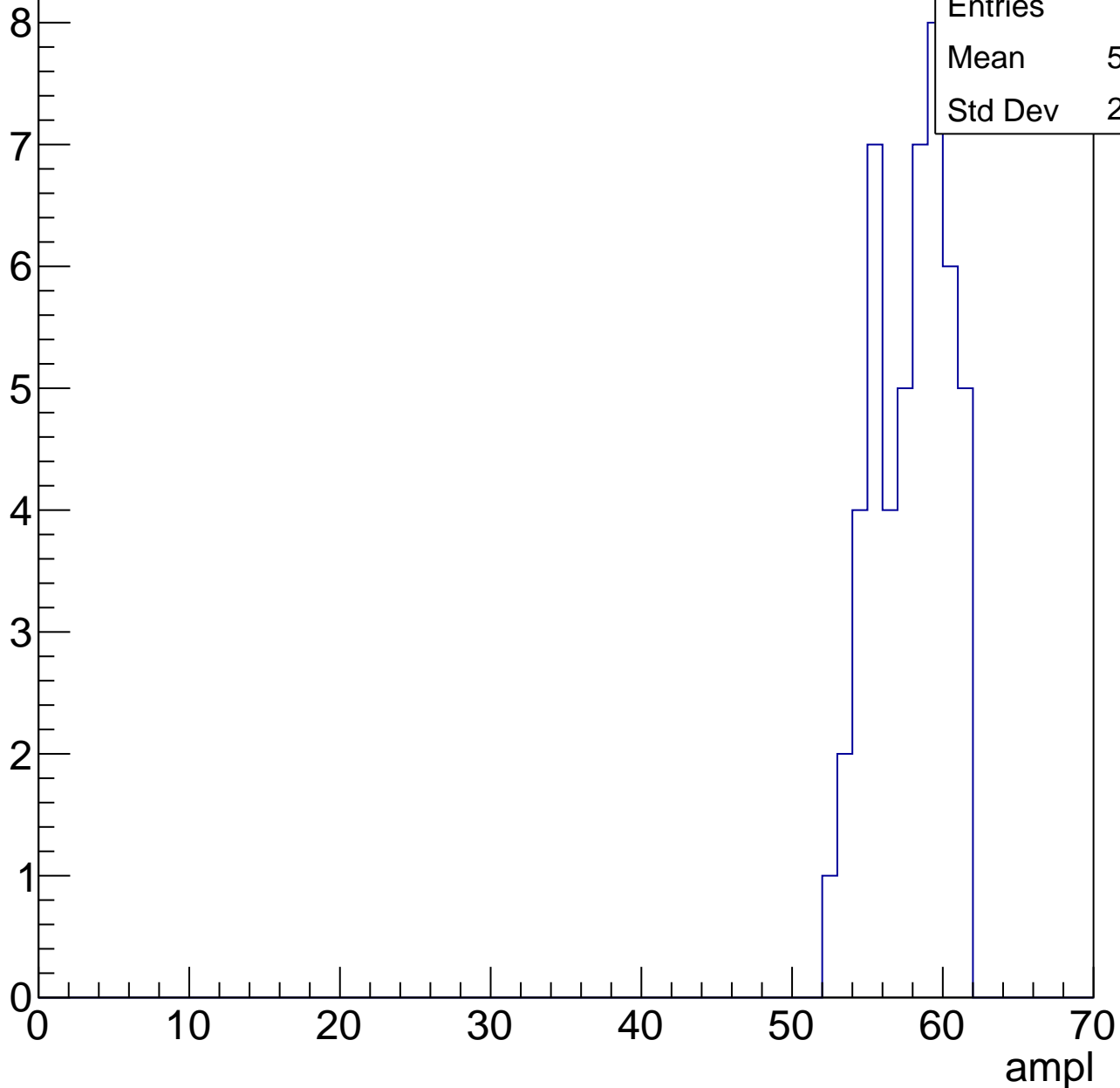
Entries	75
Mean	50.85
Std Dev	3.599



# B1L101S, U11-ch114, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

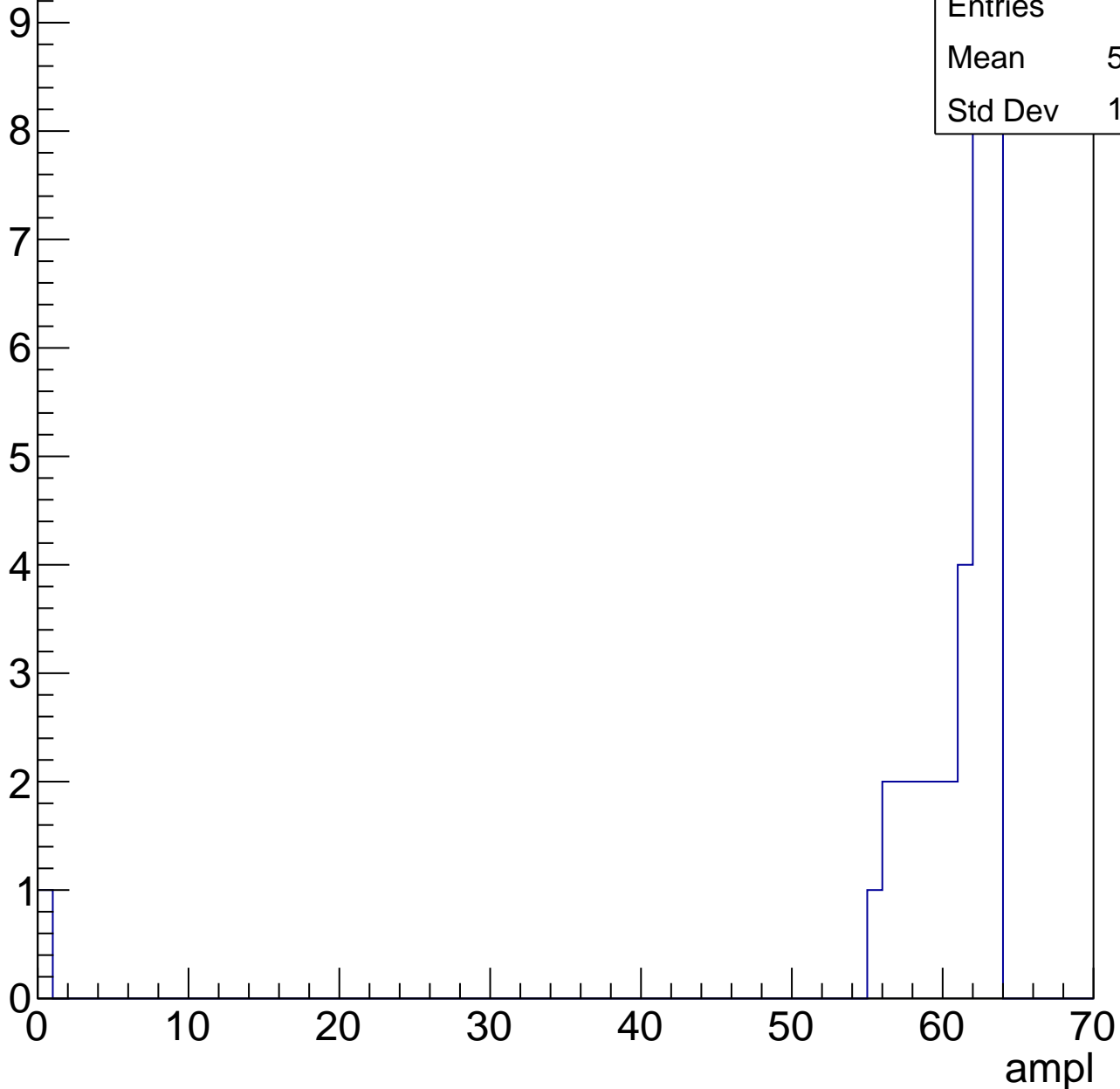


# B1L101S, U11-ch114, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

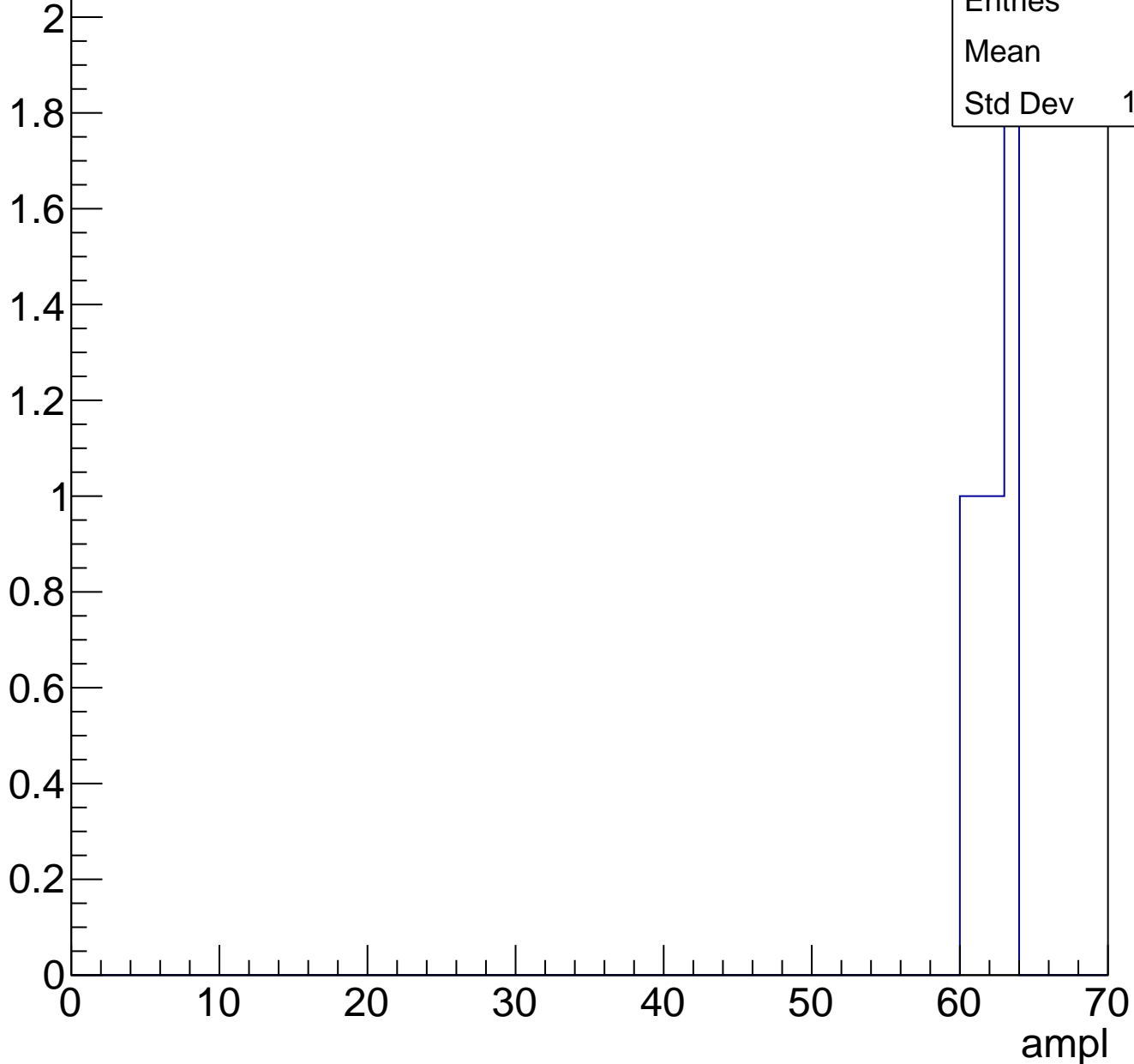
Entries	33
Mean	58.82
Std Dev	10.66



# B1L101S, U11-ch114, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch114, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U11-ch115, adc0

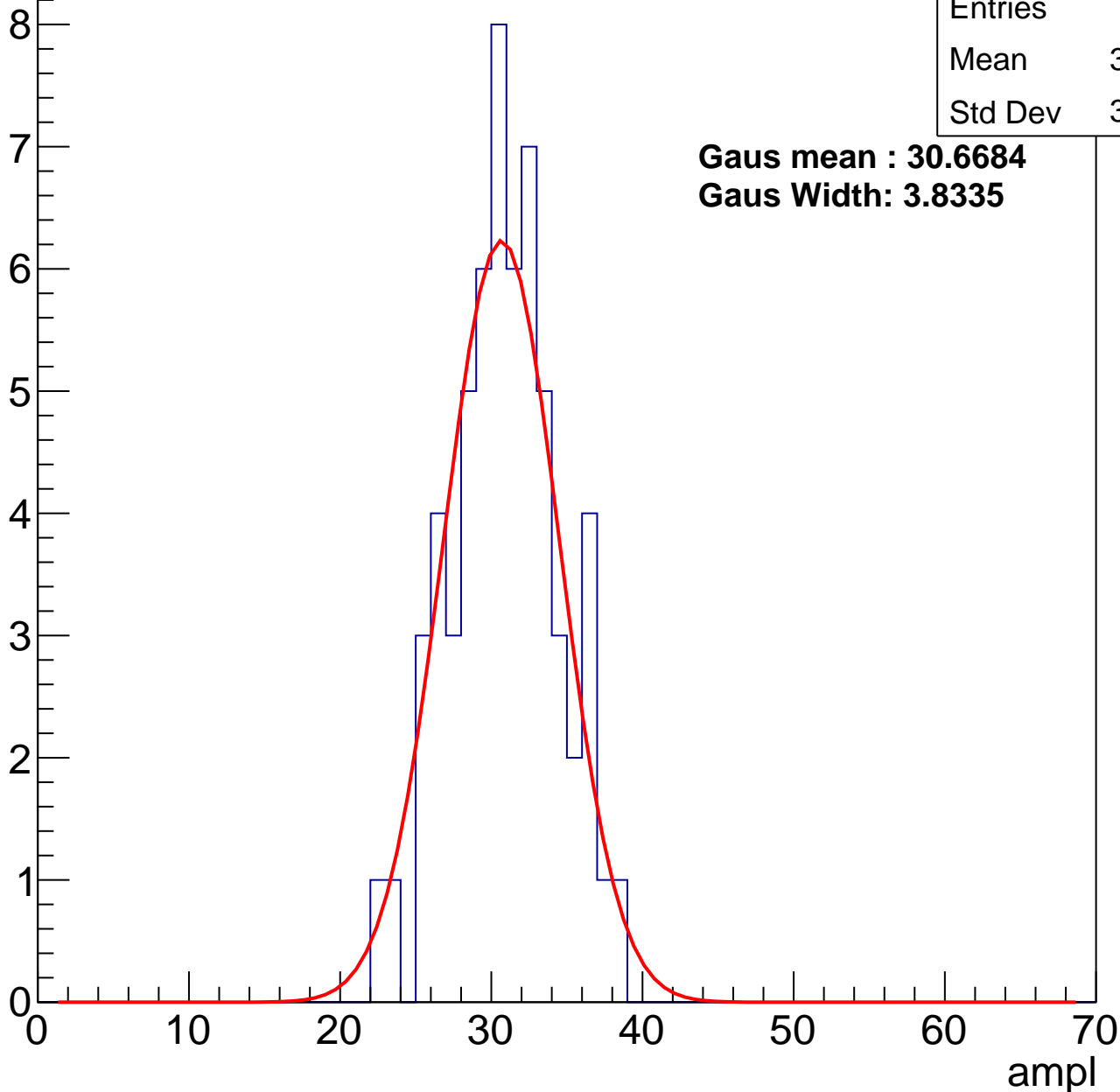
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	30.42
Std Dev	3.485

**Gaus mean : 30.6684**

**Gaus Width: 3.8335**



# B1L101S, U11-ch115, adc1

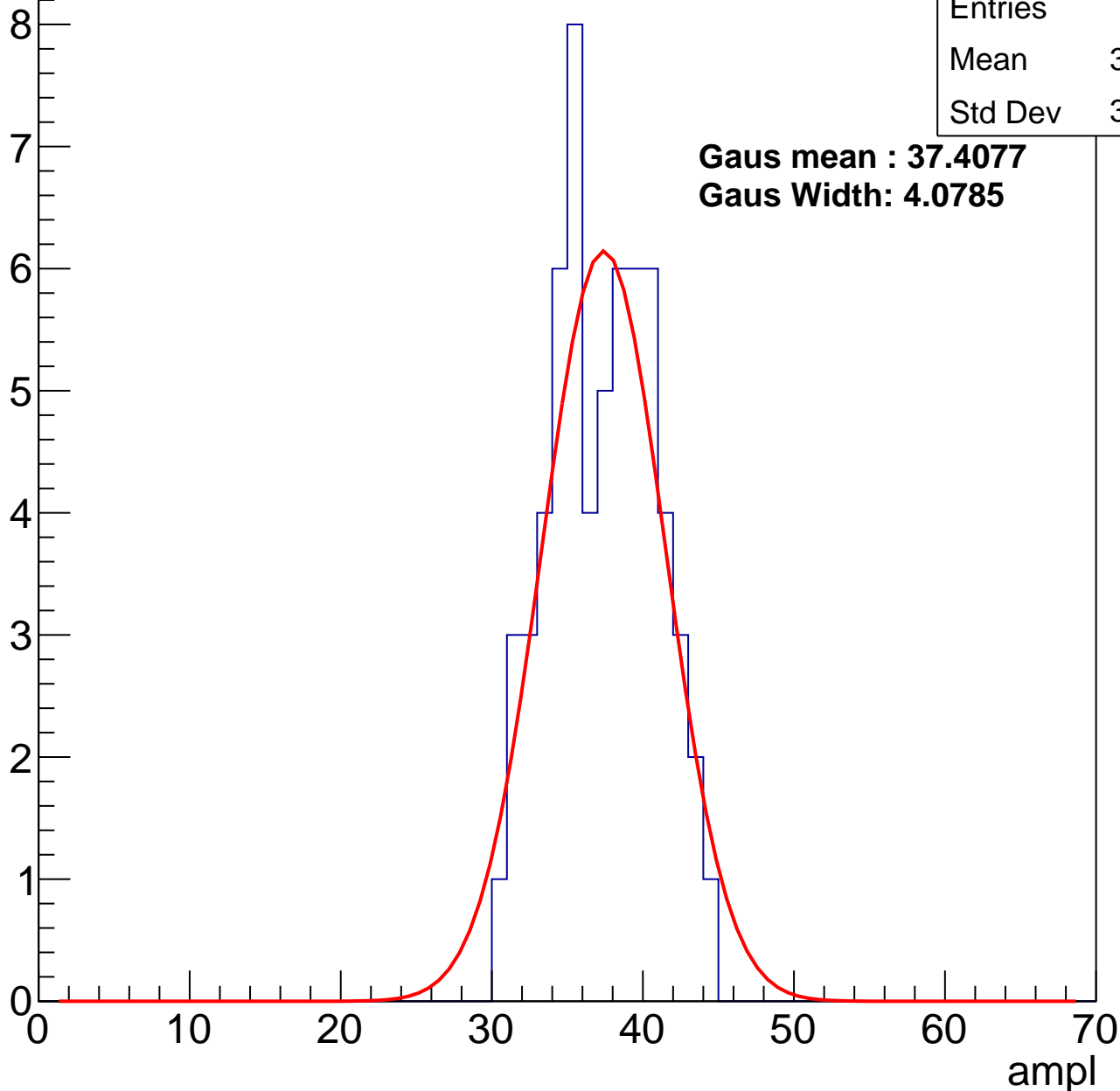
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	36.87
Std Dev	3.429

**Gaus mean : 37.4077**

**Gaus Width: 4.0785**



# B1L101S, U11-ch115, adc2

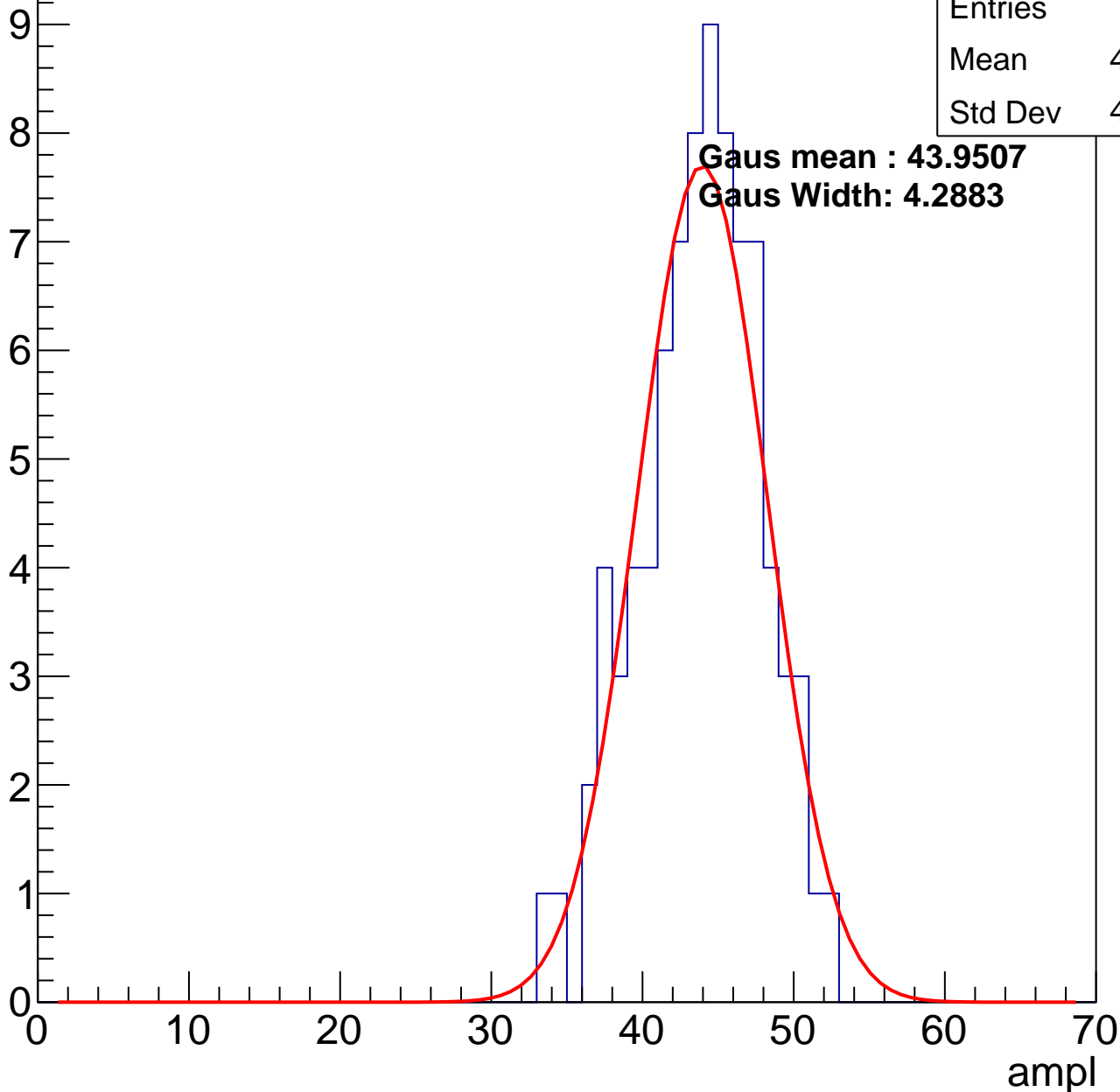
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	83
Mean	43.37
Std Dev	4.008

**Gaus mean : 43.9507**

**Gaus Width: 4.2883**

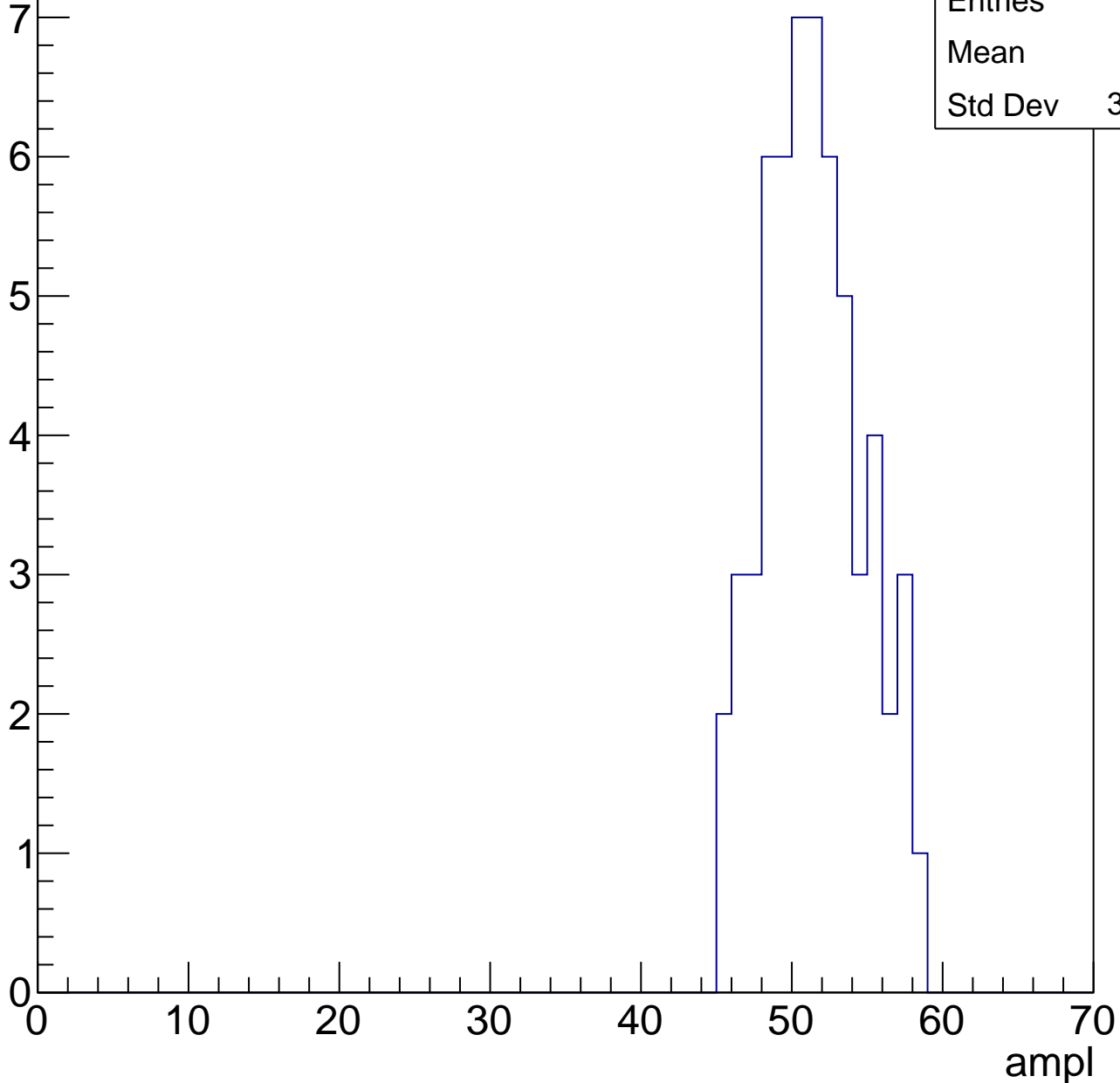


# B1L101S, U11-ch115, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	51
Std Dev	3.227

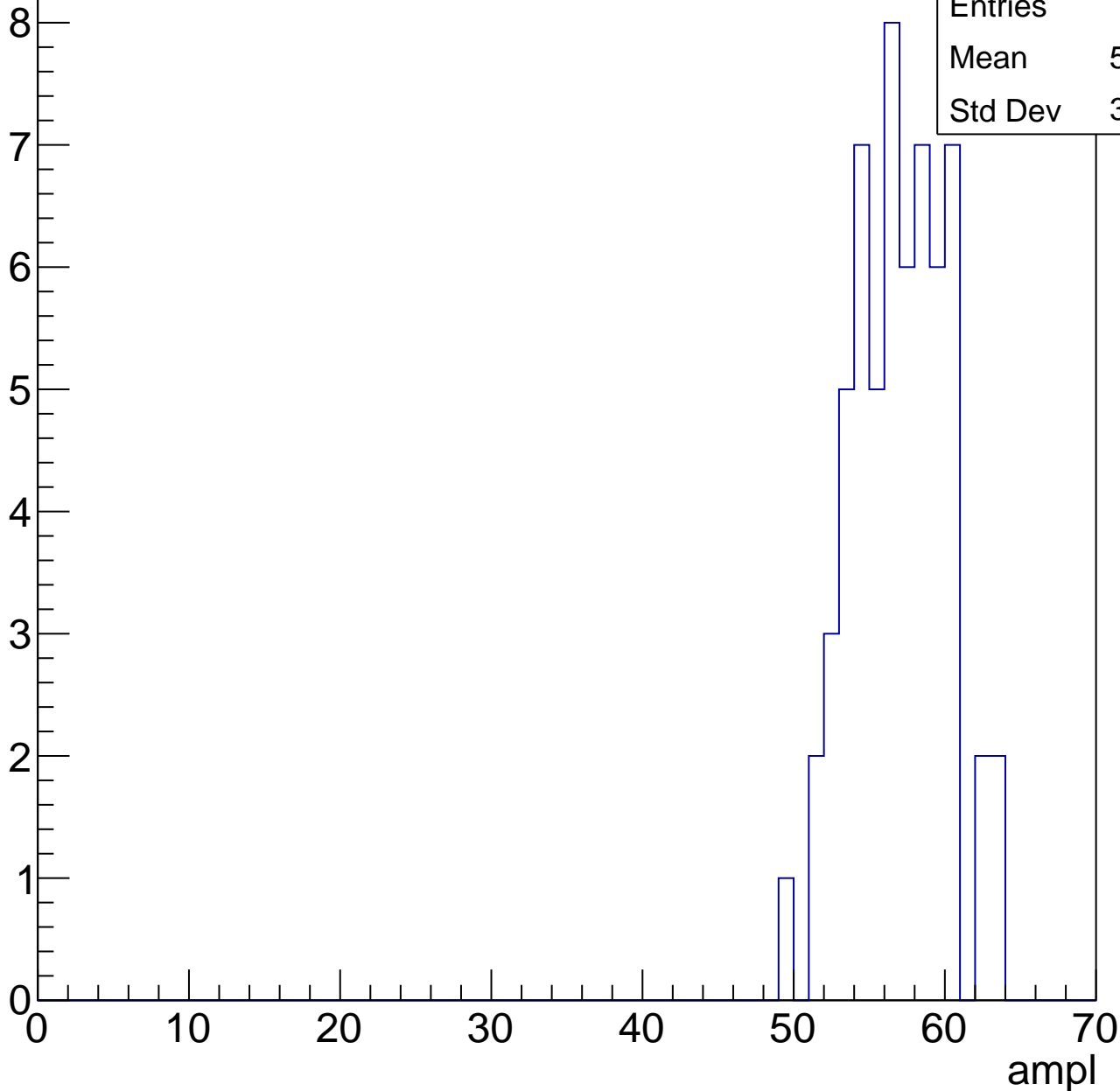


# B1L101S, U11-ch115, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	56.48
Std Dev	3.087

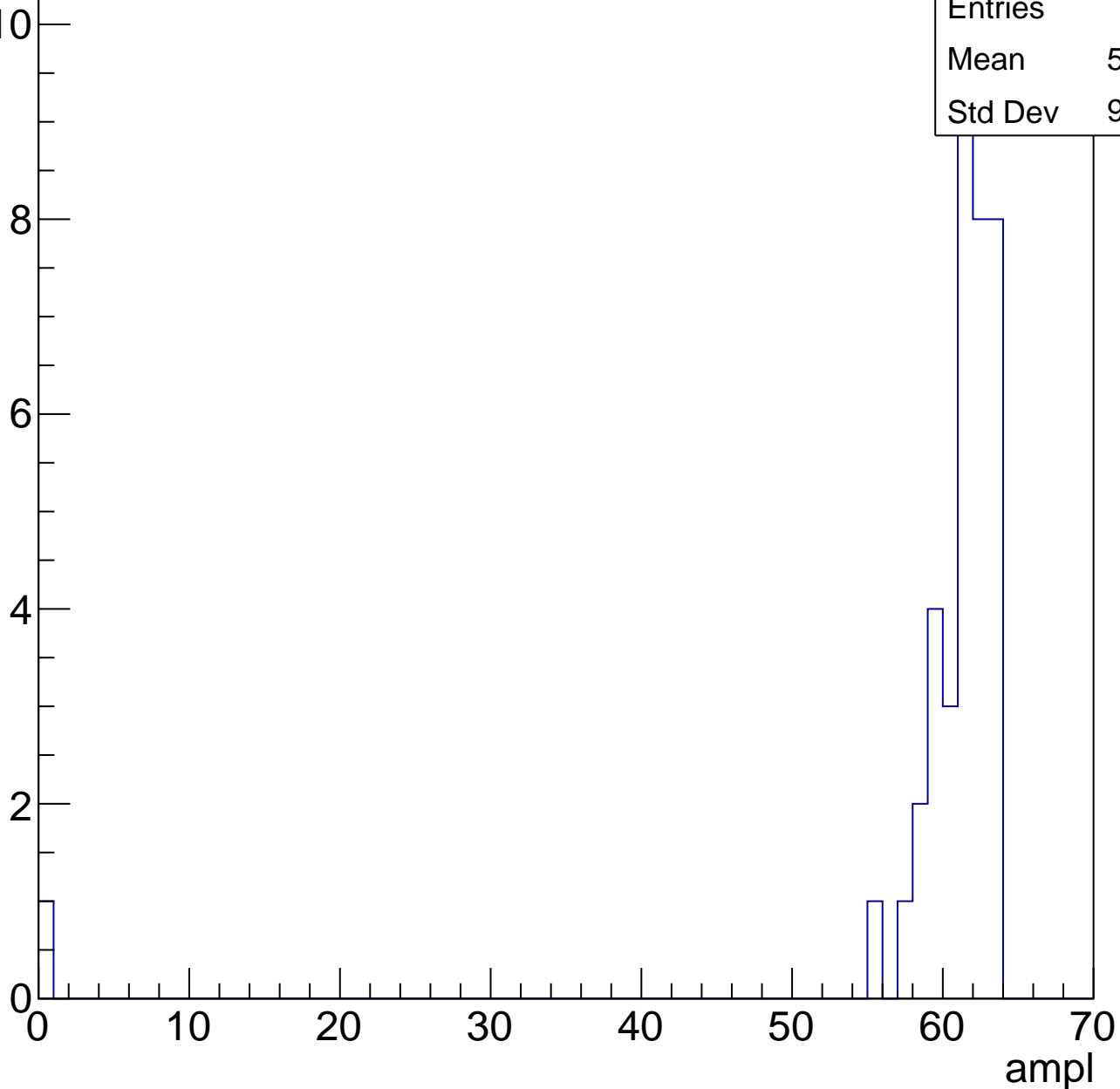


# B1L101S, U11-ch115, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	38
Mean	59.32
Std Dev	9.924



# B1L101S, U11-ch115, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L101S, U11-ch115, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U11-ch116, adc0

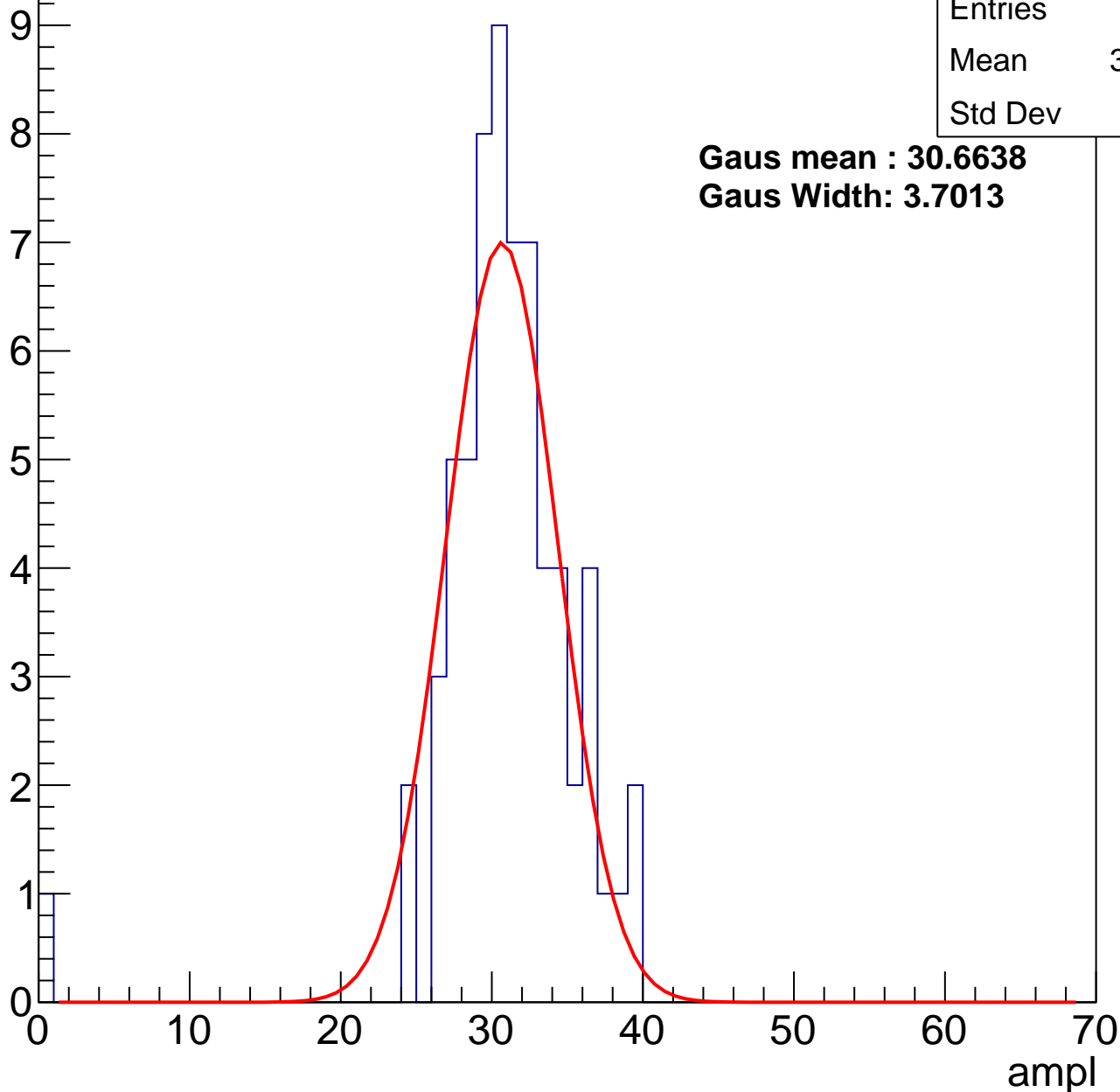
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	30.45
Std Dev	5.09

**Gaus mean : 30.6638**

**Gaus Width: 3.7013**



# B1L101S, U11-ch116, adc1

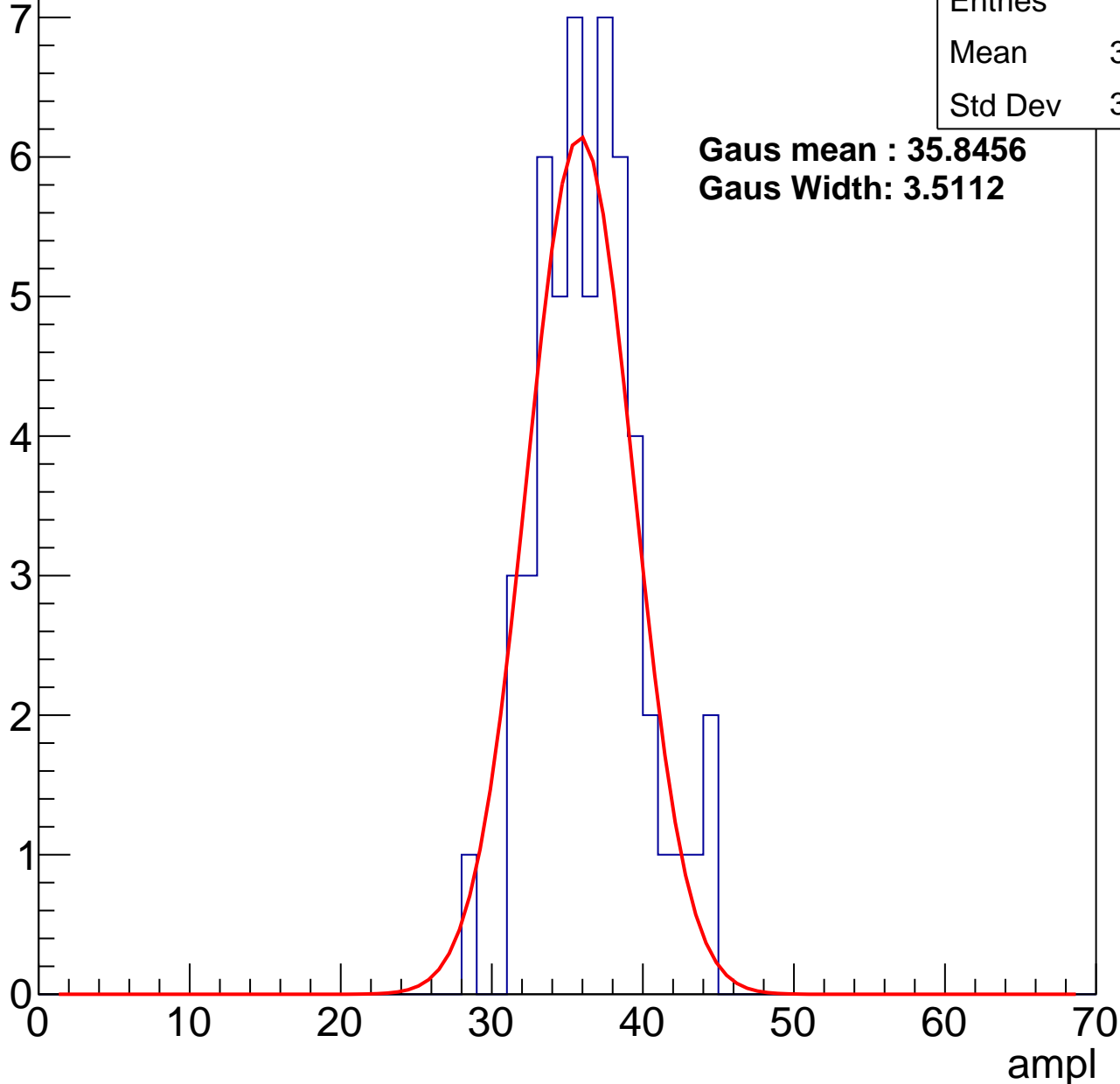
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	36.06
Std Dev	3.347

**Gaus mean : 35.8456**

**Gaus Width: 3.5112**



# B1L101S, U11-ch116, adc2

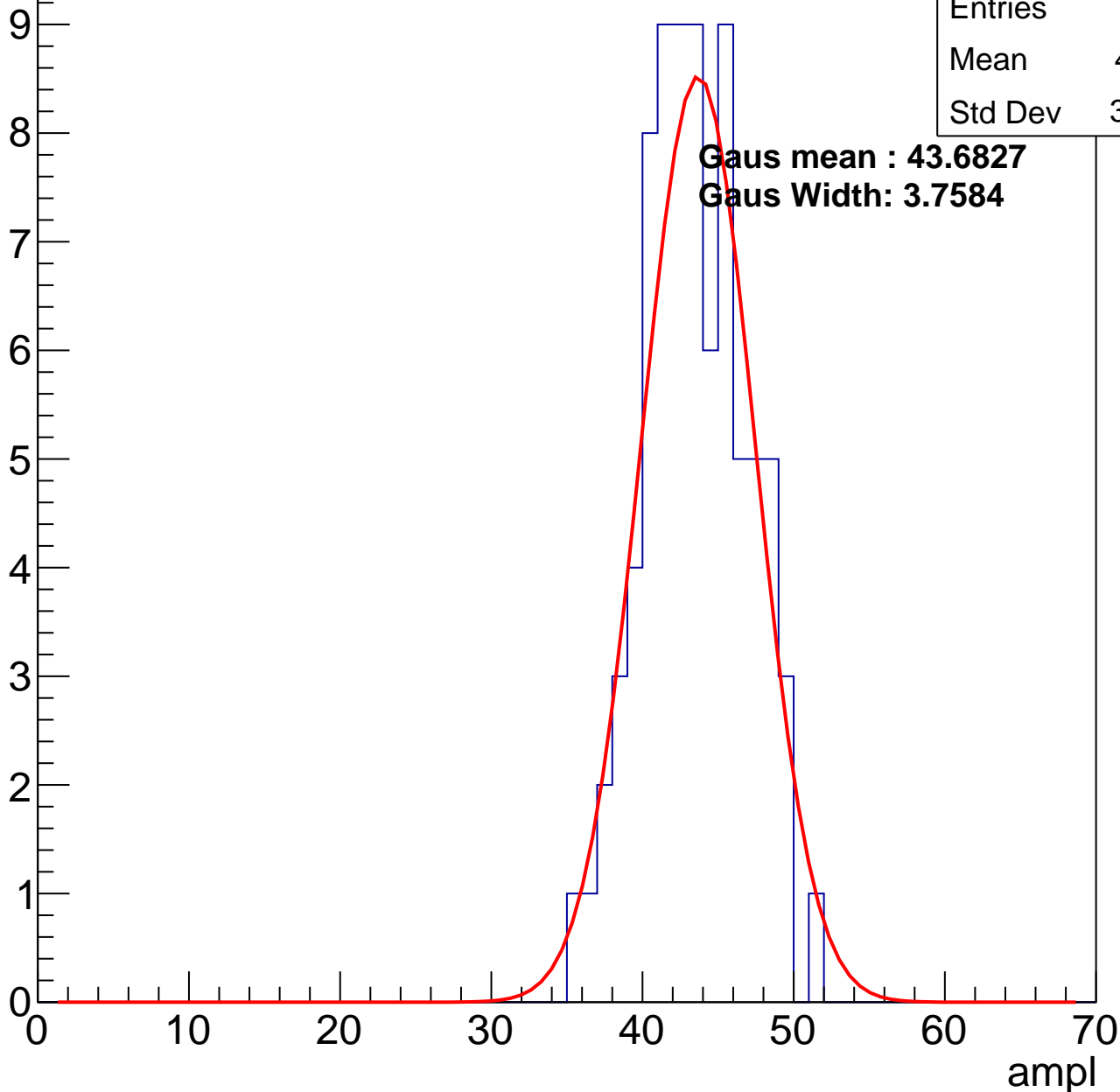
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	80
Mean	43.01
Std Dev	3.363

**Gaus mean : 43.6827**

**Gaus Width: 3.7584**

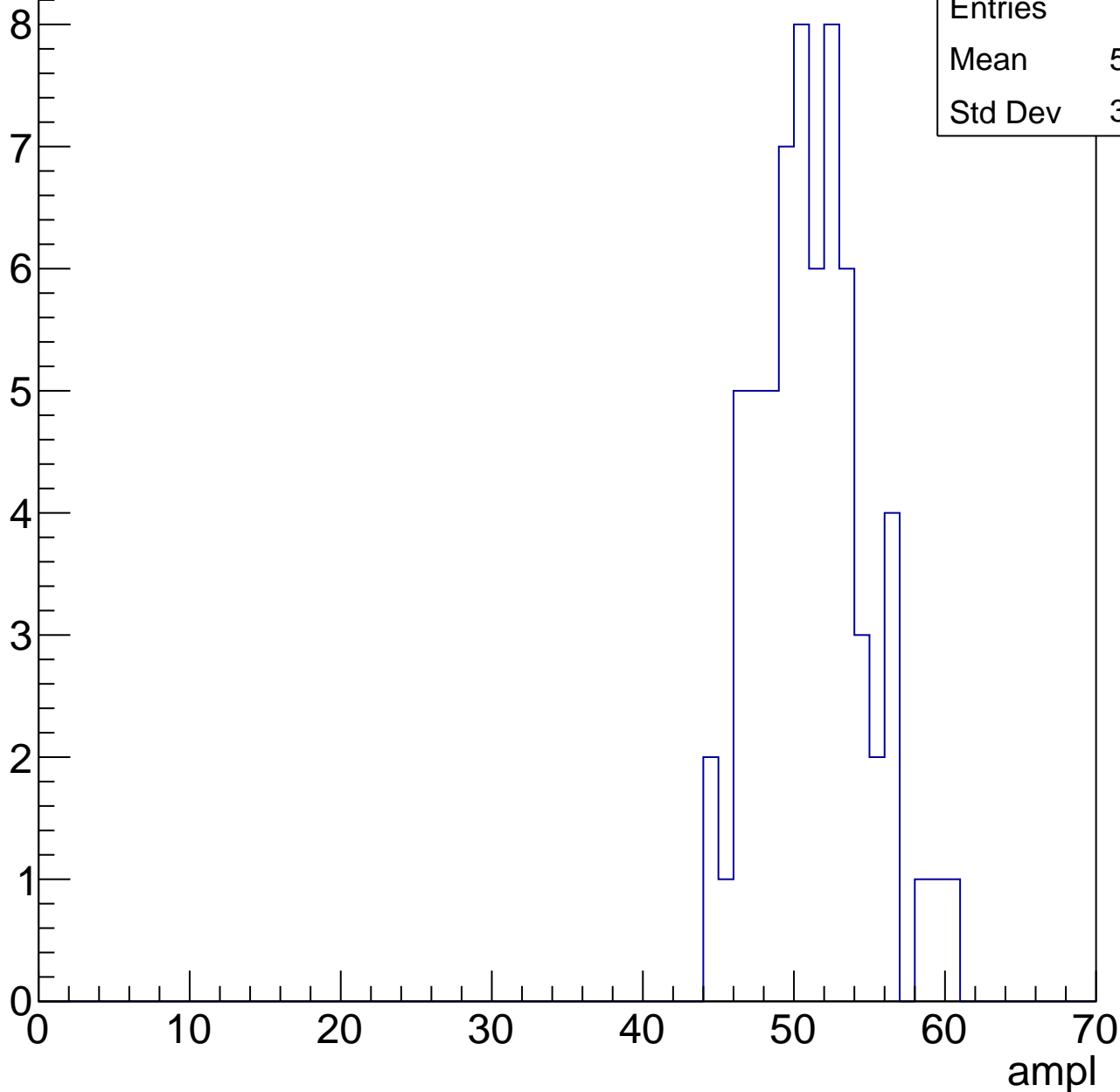


# B1L101S, U11-ch116, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	50.68
Std Dev	3.504

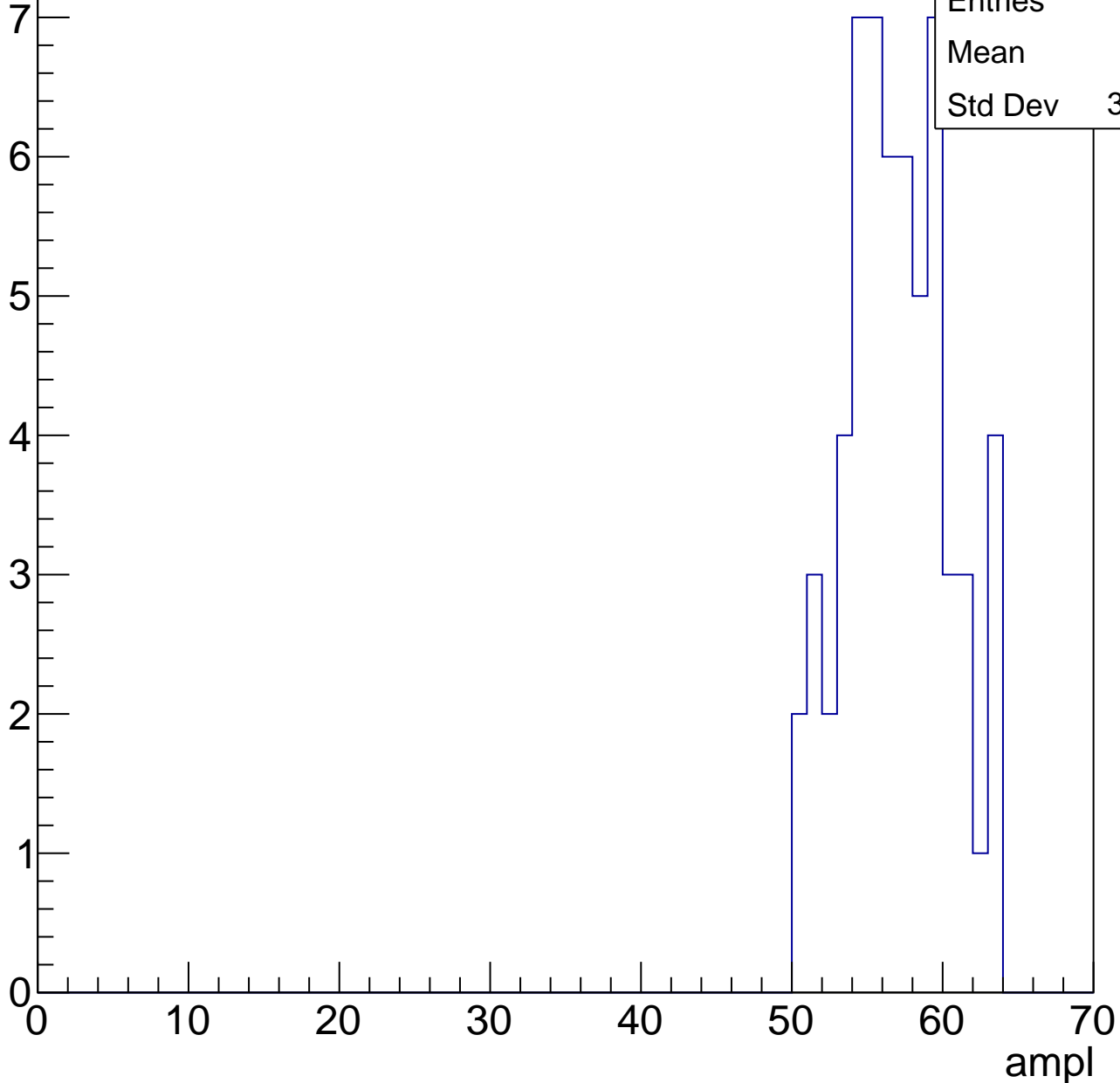


# B1L101S, U11-ch116, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	56.5
Std Dev	3.364

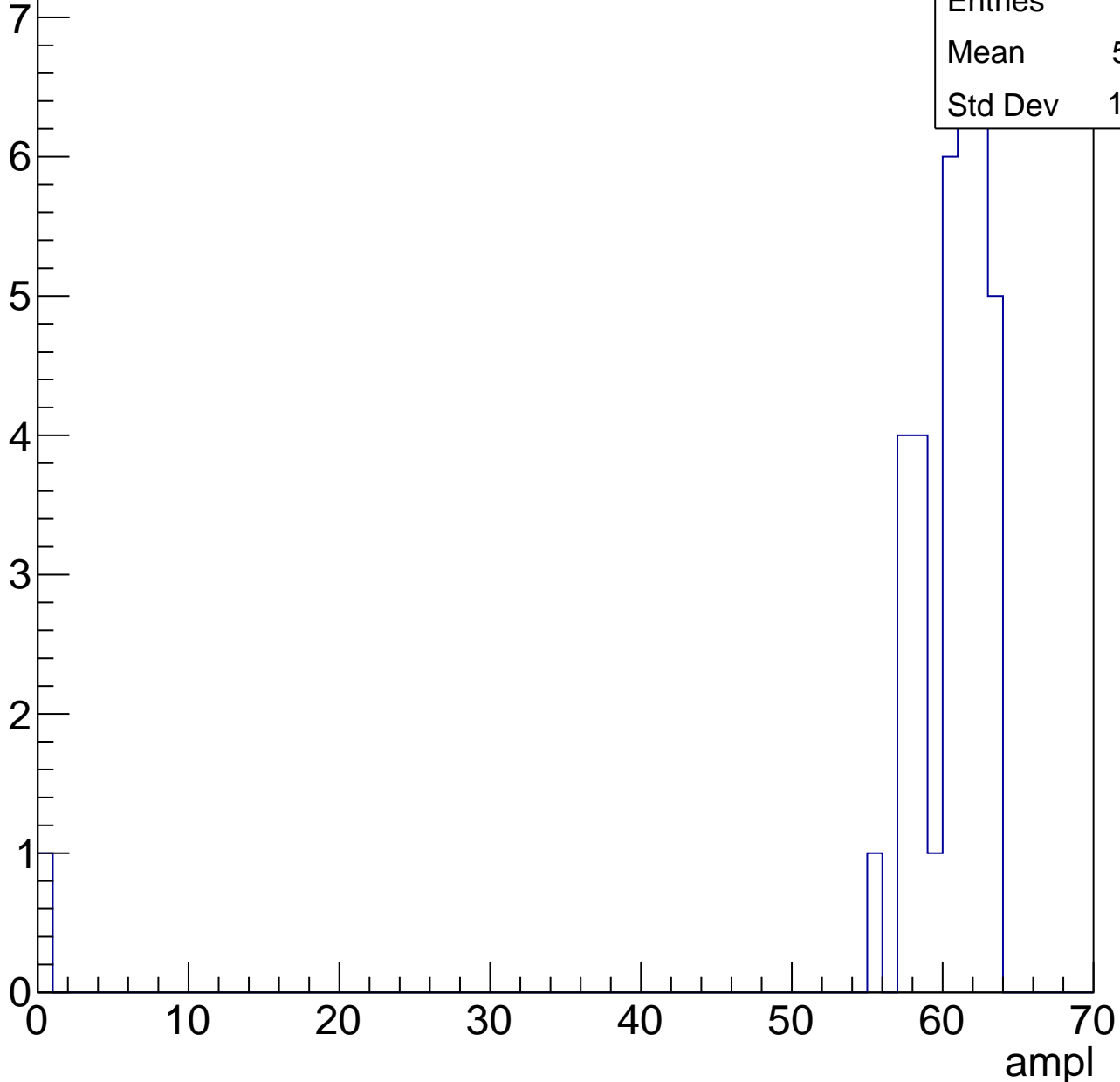


# B1L101S, U11-ch116, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	36
Mean	58.61
Std Dev	10.12



# B1L101S, U11-ch116, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	4
Mean	61.5
Std Dev	1.5



# B1L101S, U11-ch116, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U11-ch117, adc0

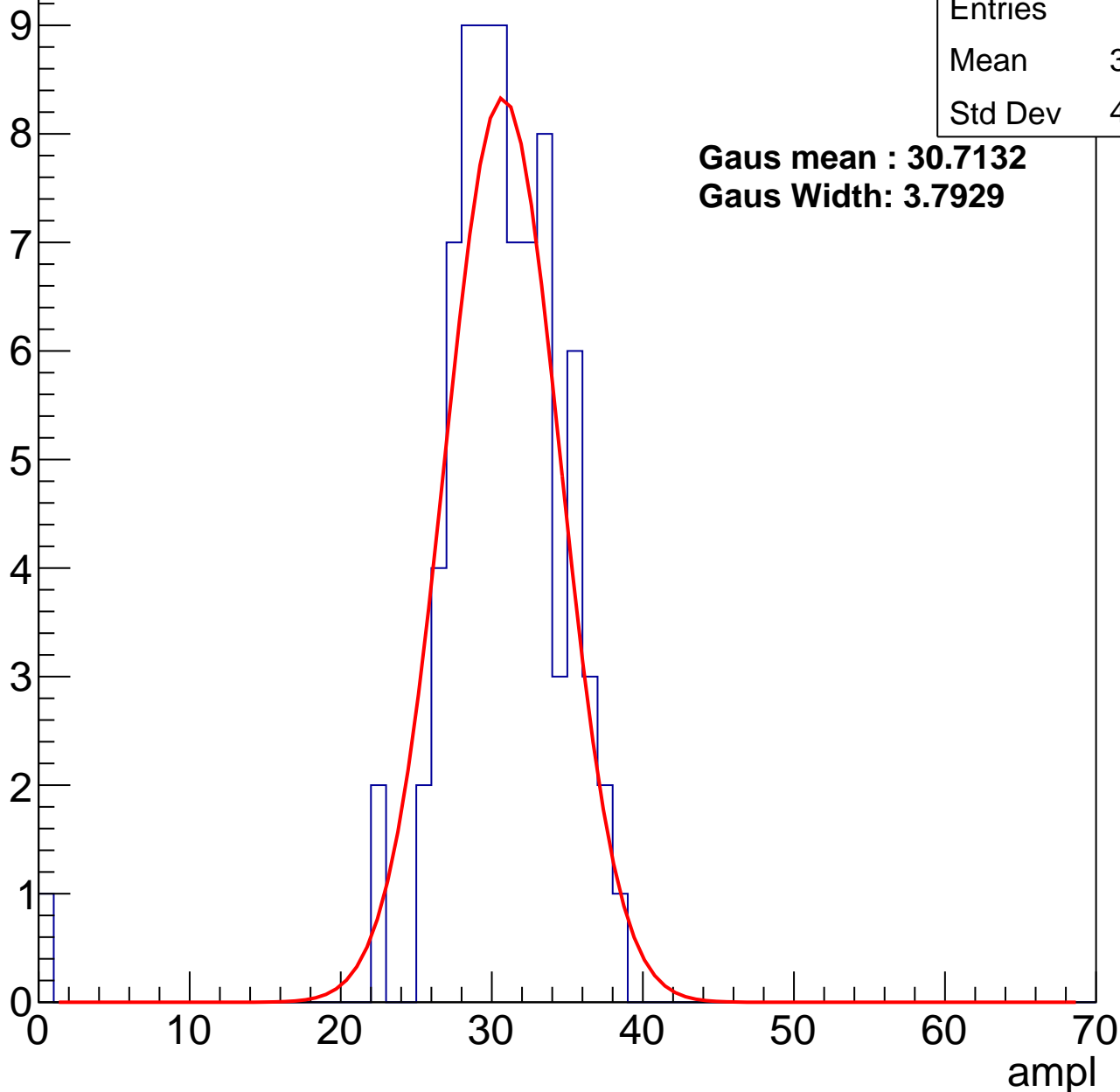
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	80
Mean	30.09
Std Dev	4.775

**Gaus mean : 30.7132**

**Gaus Width: 3.7929**



# B1L101S, U11-ch117, adc1

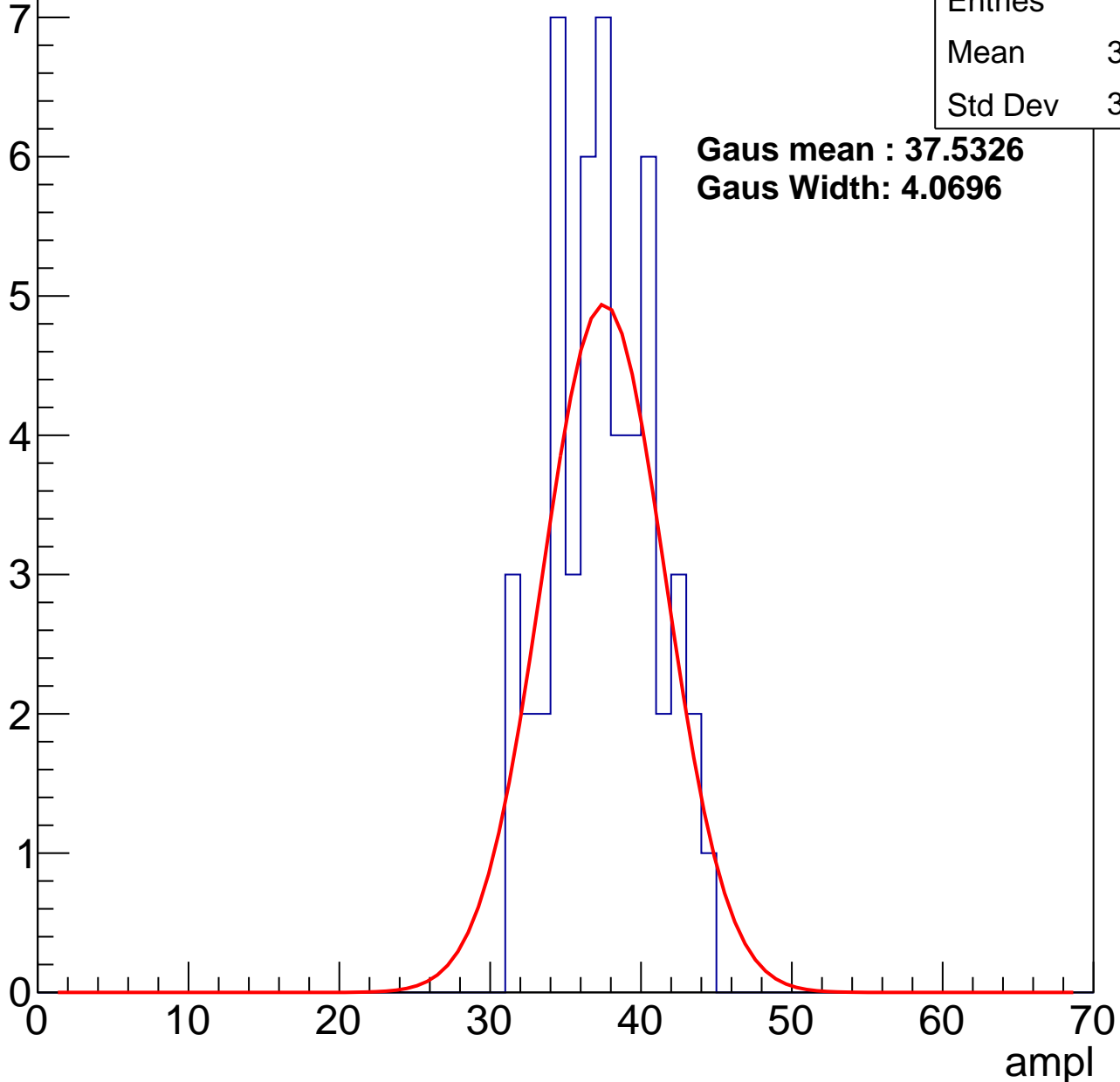
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	37.06
Std Dev	3.319

**Gaus mean : 37.5326**

**Gaus Width: 4.0696**



# B1L101S, U11-ch117, adc2

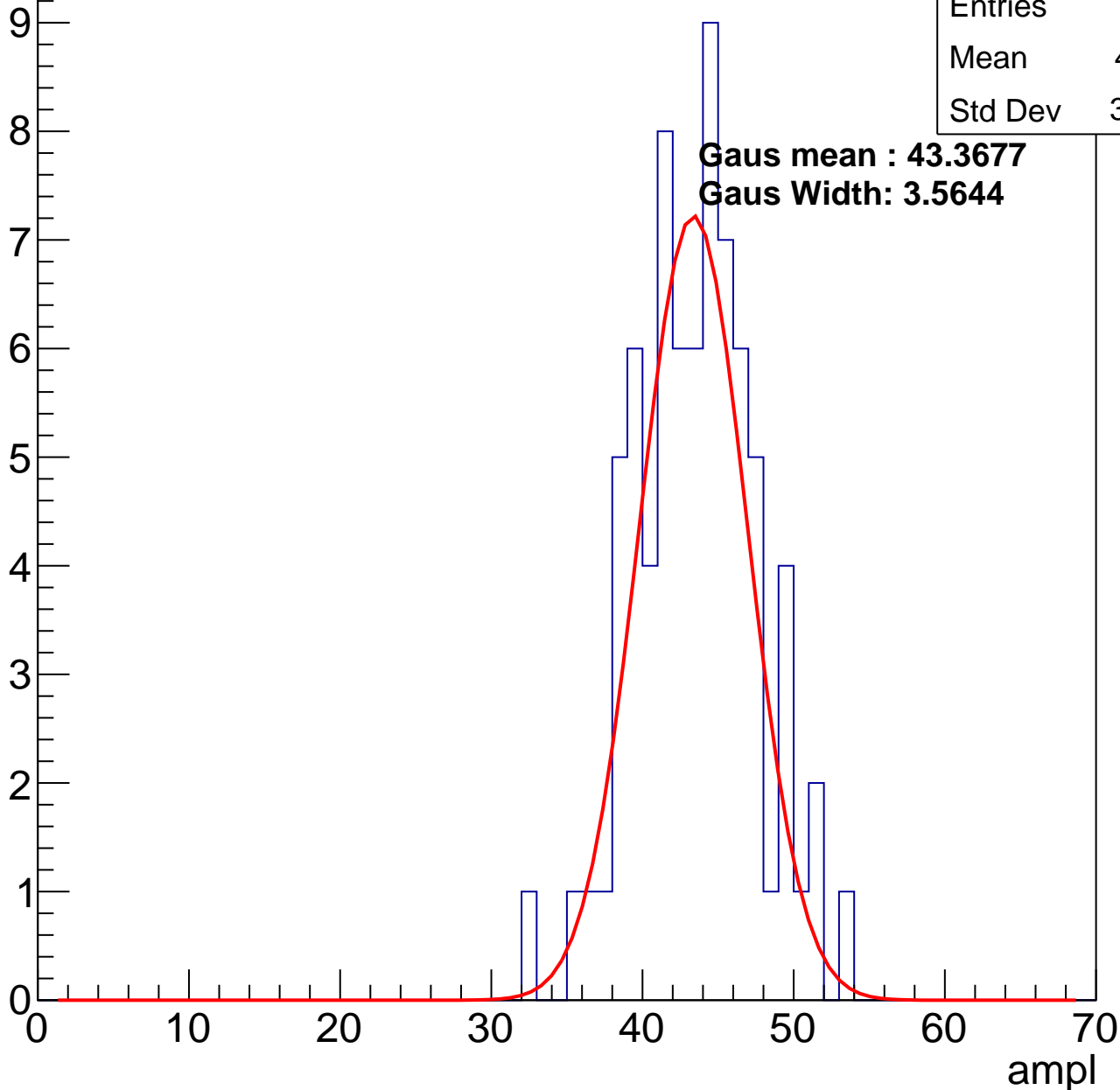
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	43.11
Std Dev	3.968

**Gaus mean : 43.3677**

**Gaus Width: 3.5644**

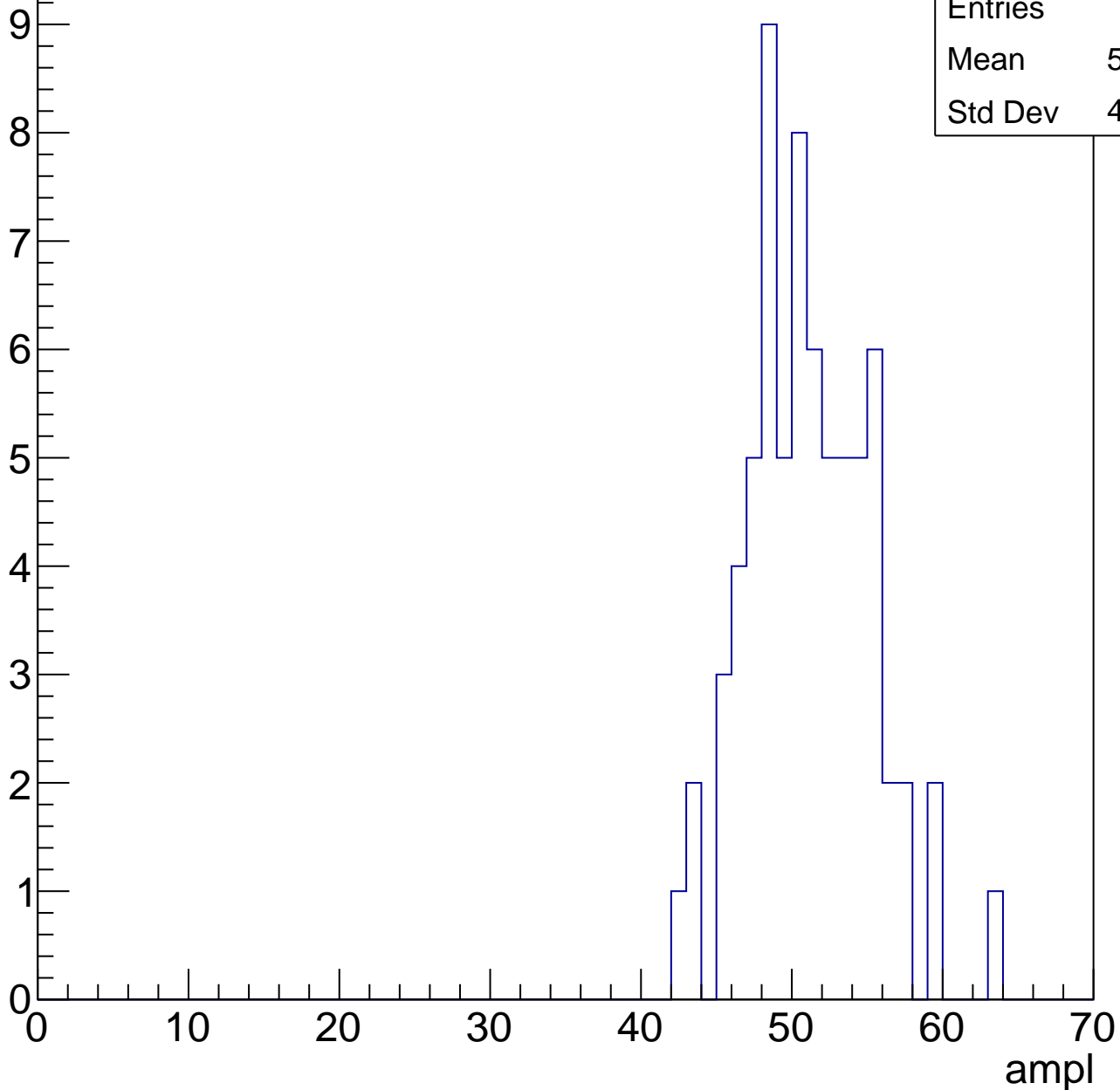


# B1L101S, U11-ch117, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

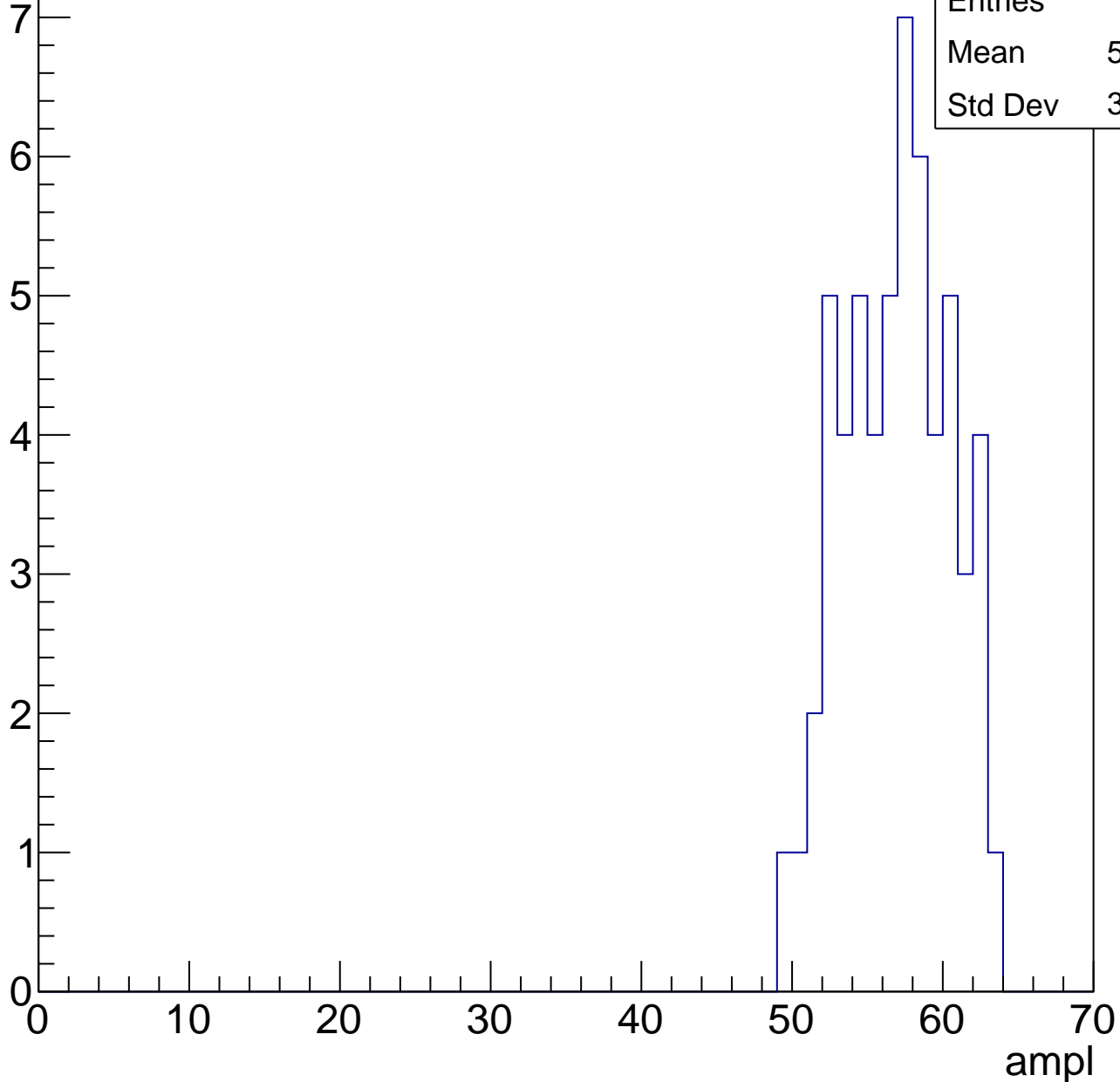
Entries	71
Mean	50.66
Std Dev	4.038



# B1L101S, U11-ch117, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



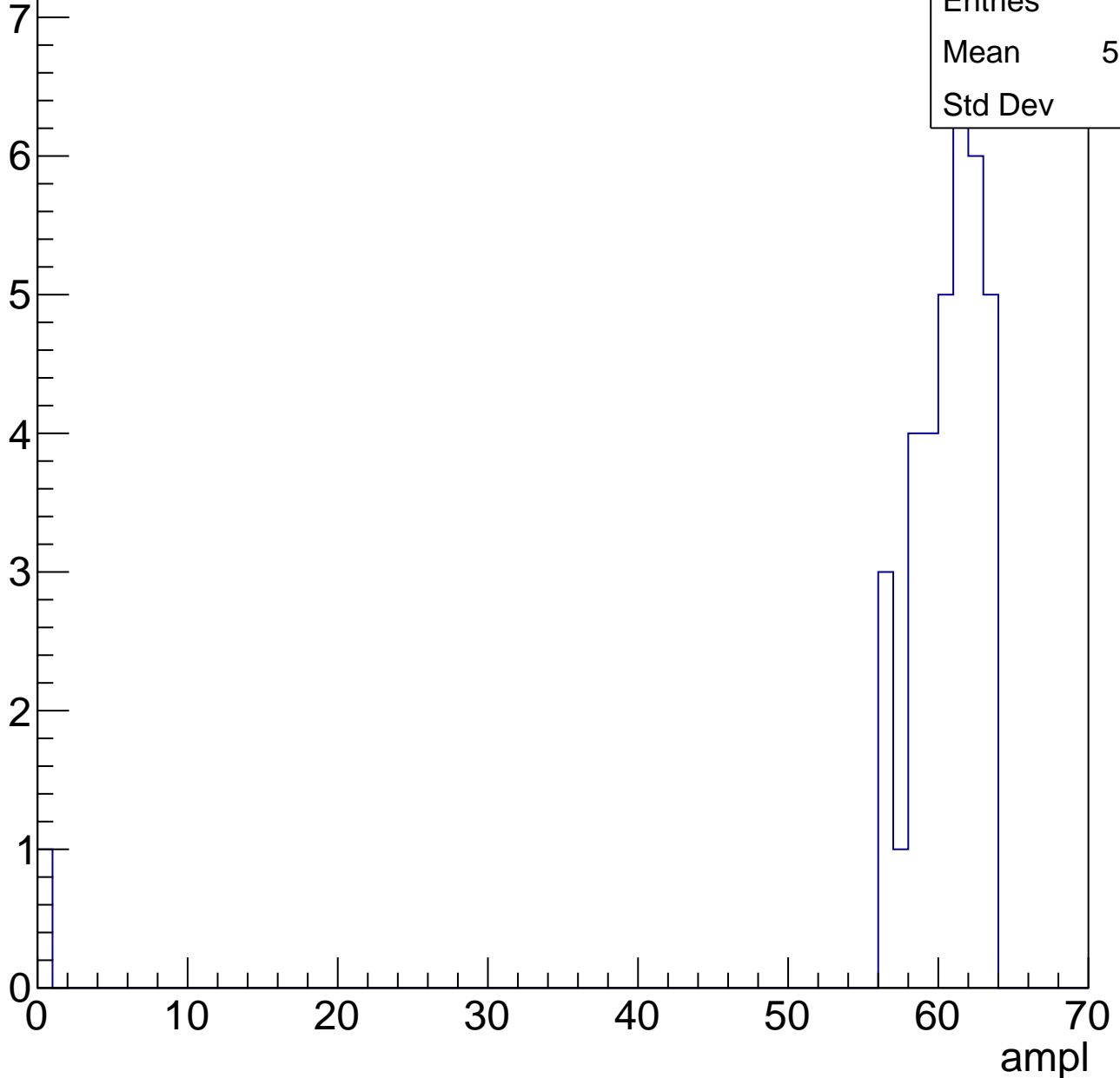
Entries	57
Mean	56.49
Std Dev	3.444

# B1L101S, U11-ch117, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	36
Mean	58.53
Std Dev	10.1



# B1L101S, U11-ch117, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

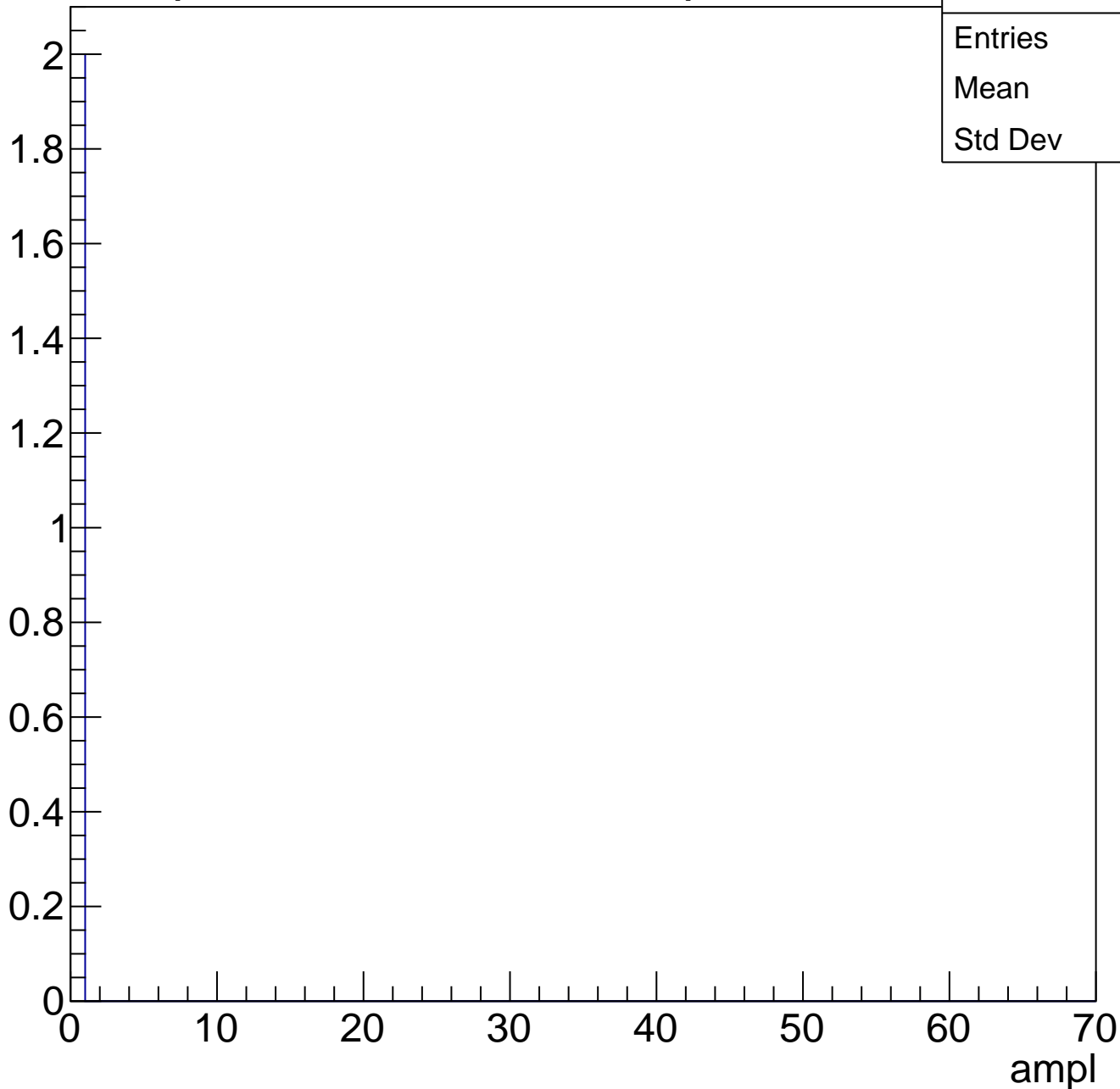




# B1L101S, U11-ch117, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U11-ch118, adc0

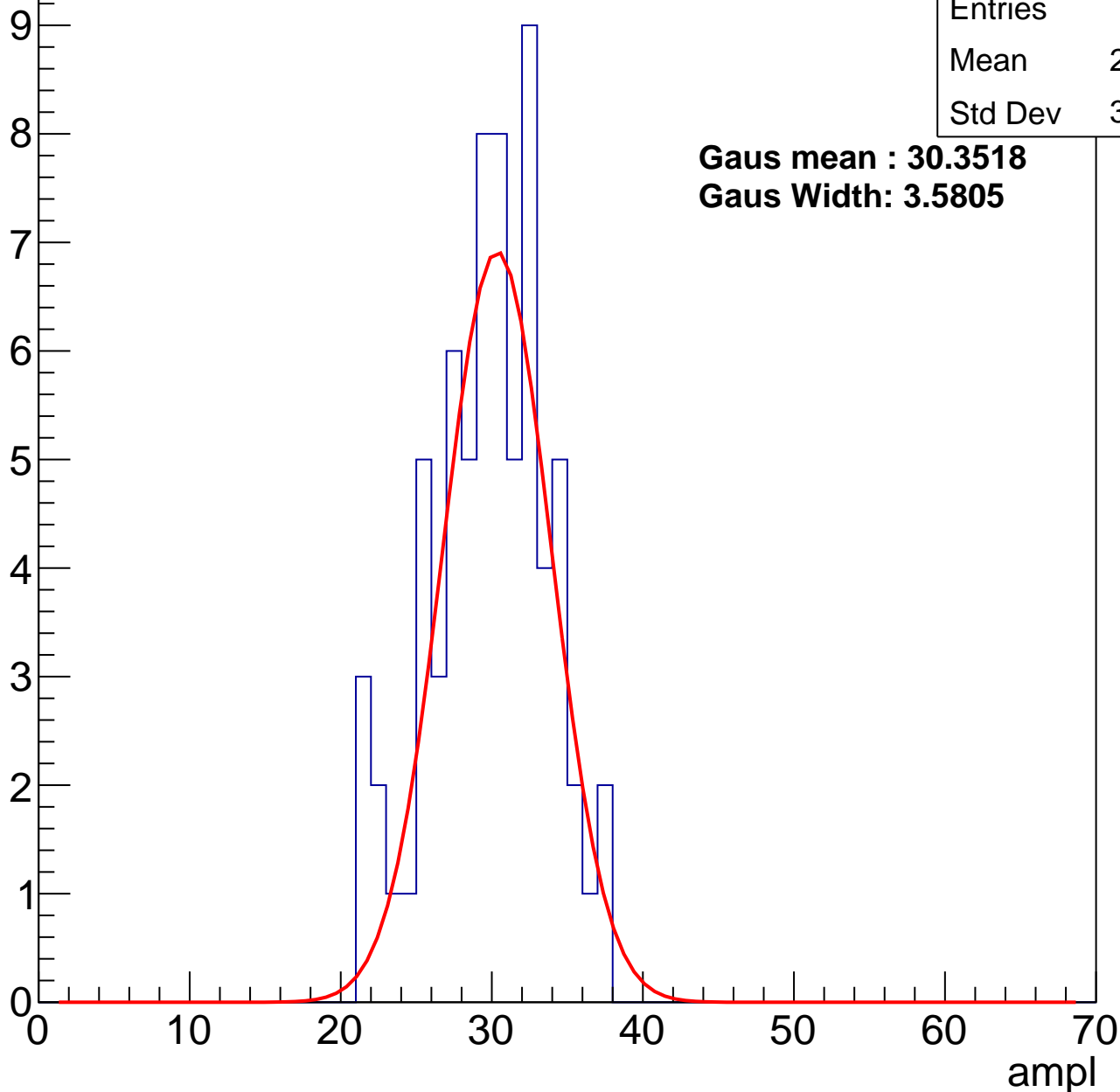
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	29.37
Std Dev	3.825

**Gaus mean : 30.3518**

**Gaus Width: 3.5805**



# B1L101S, U11-ch118, adc1

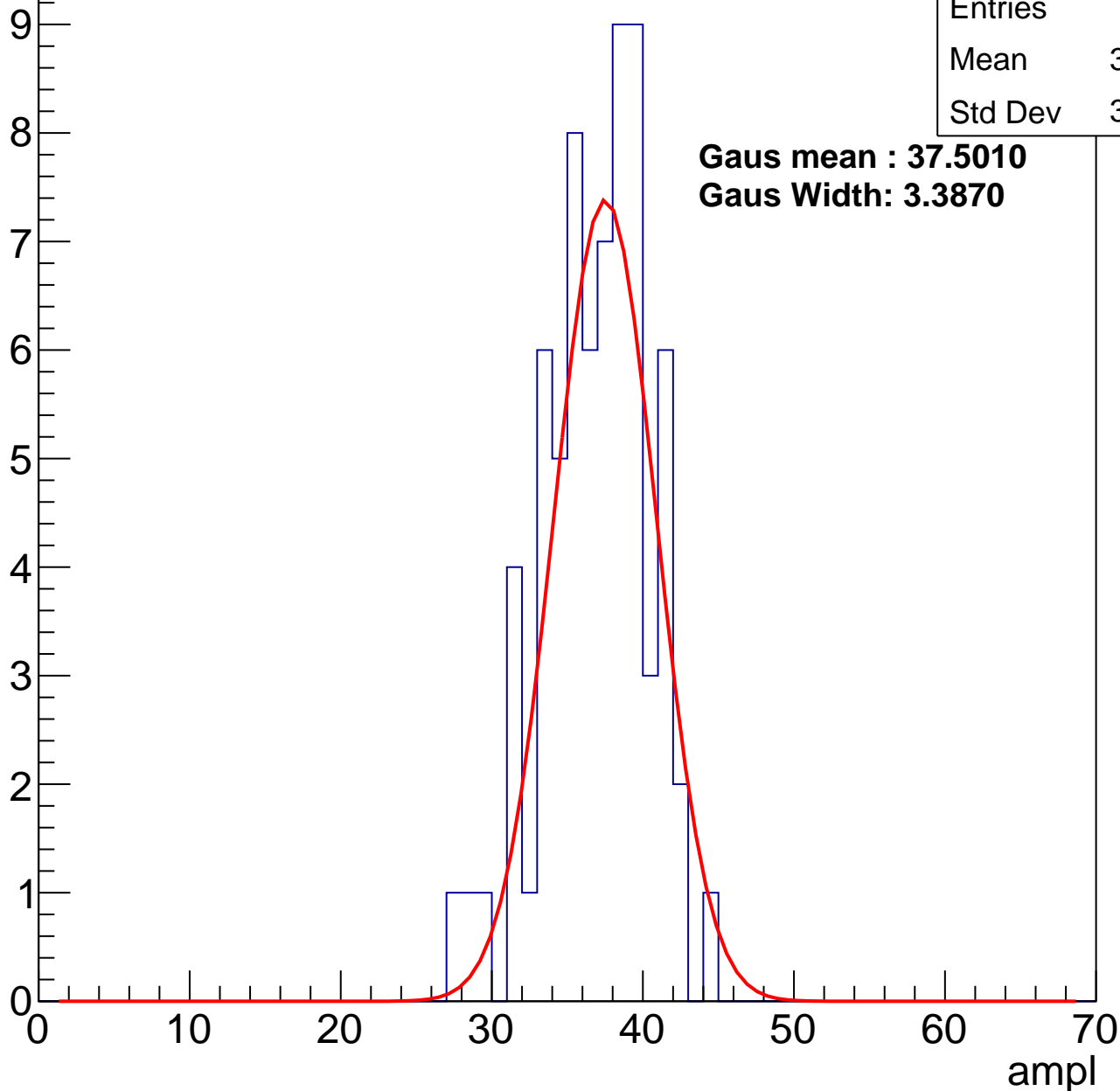
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	36.43
Std Dev	3.458

**Gaus mean : 37.5010**

**Gaus Width: 3.3870**



# B1L101S, U11-ch118, adc2

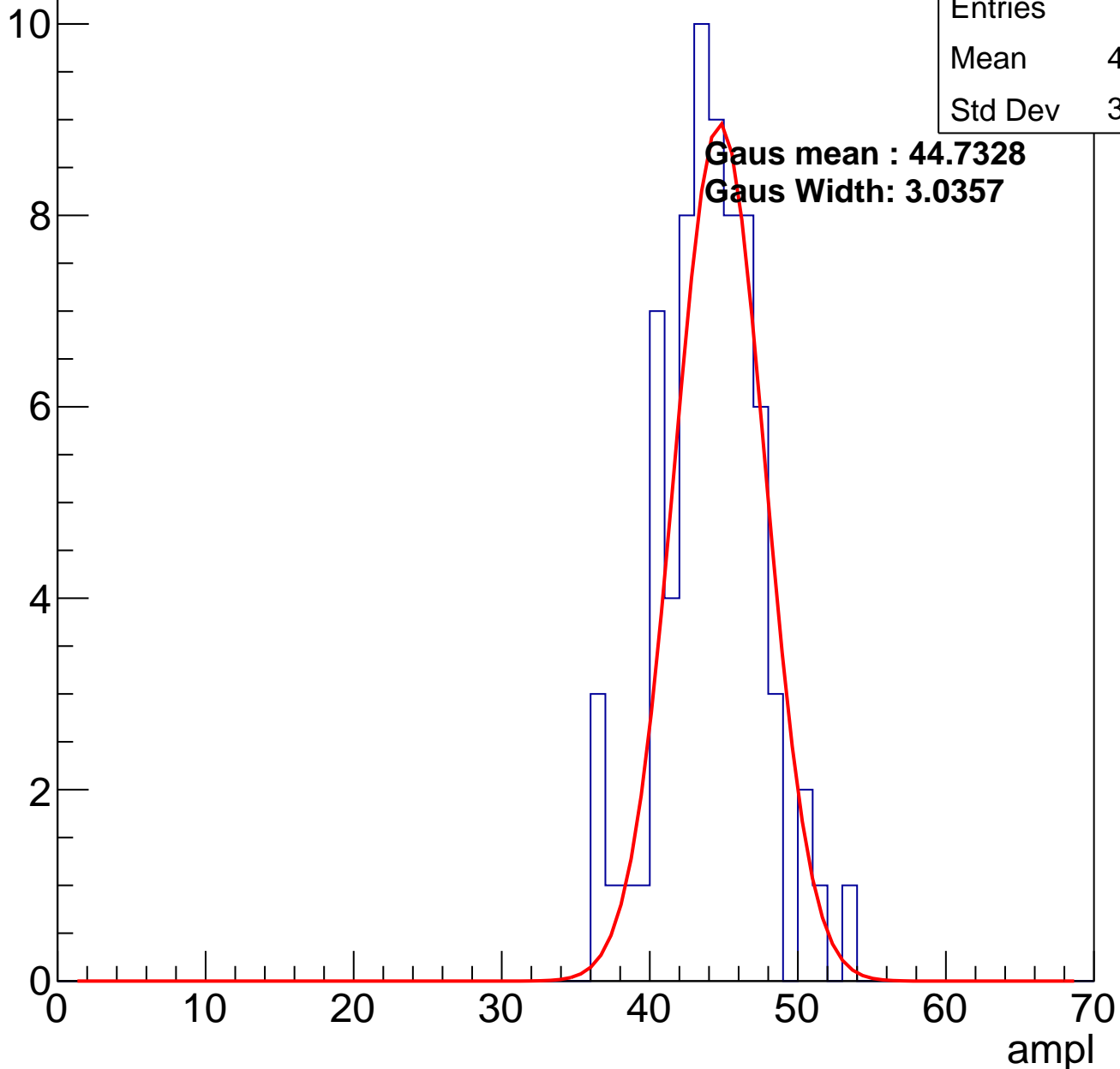
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	73
Mean	43.64
Std Dev	3.365

**Gaus mean : 44.7328**

**Gaus Width: 3.0357**

Entry



# B1L101S, U11-ch118, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

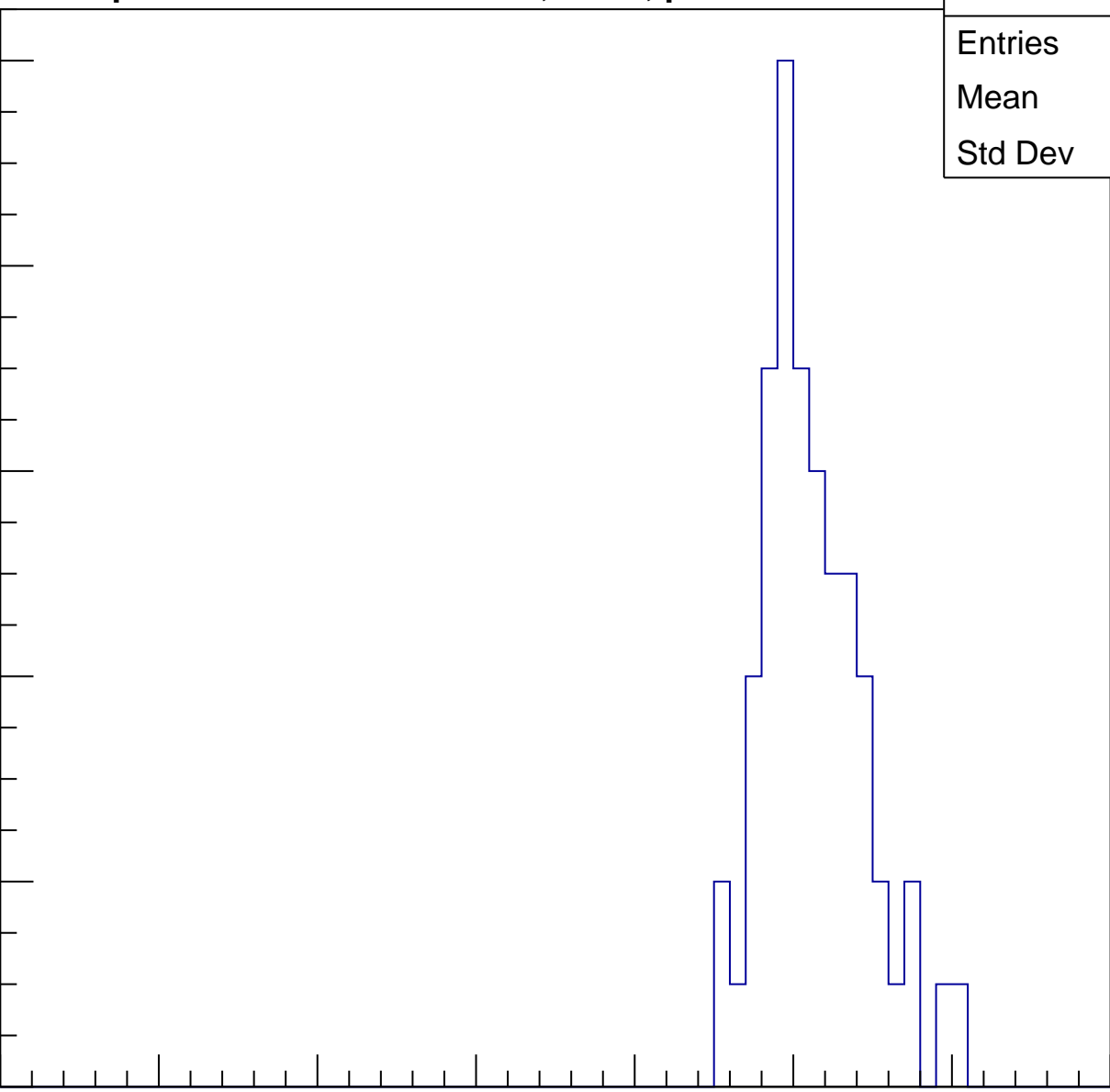
Entries	58
Mean	50.79
Std Dev	3.226

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

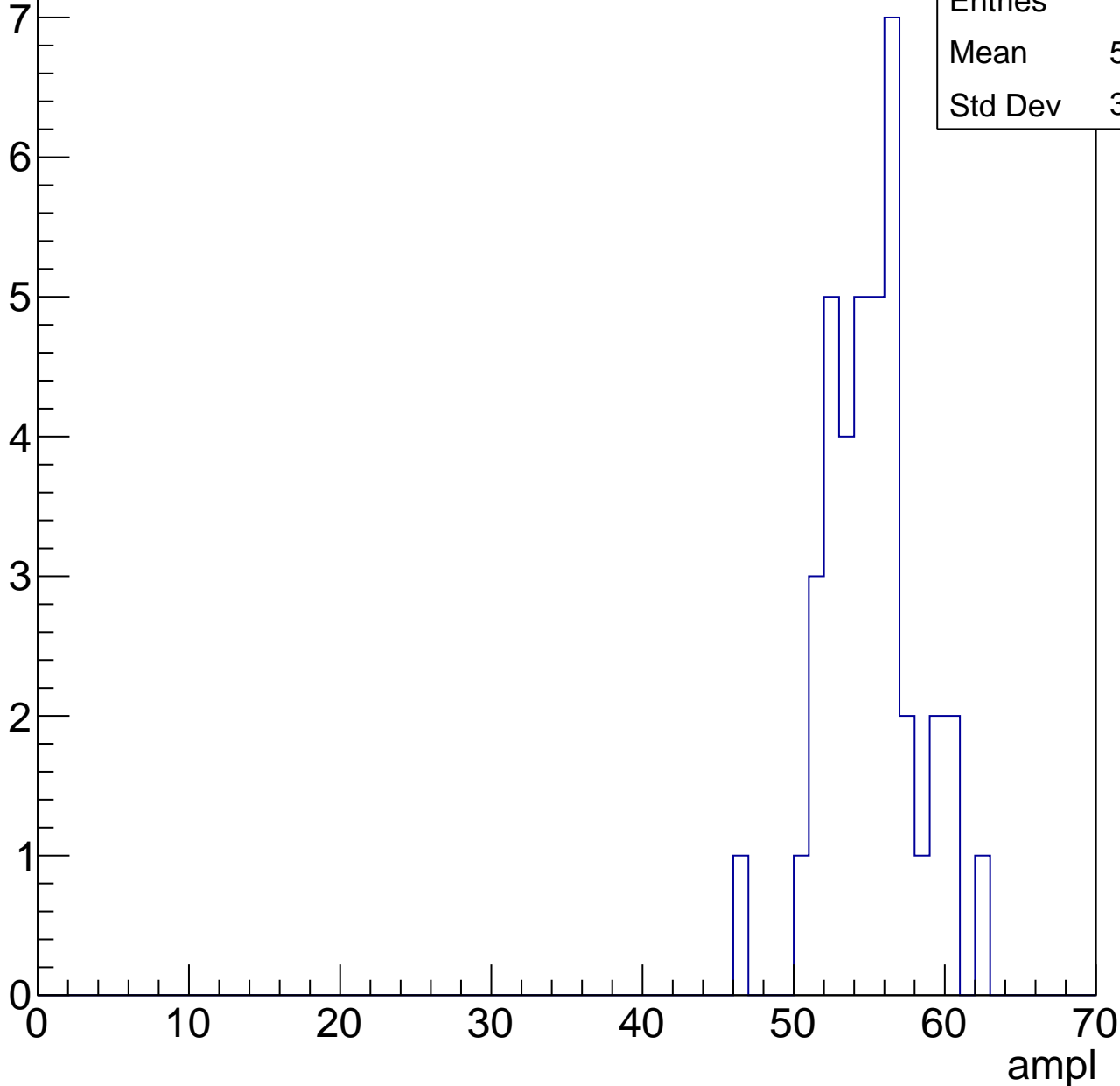


# B1L101S, U11-ch118, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	39
Mean	54.62
Std Dev	3.077

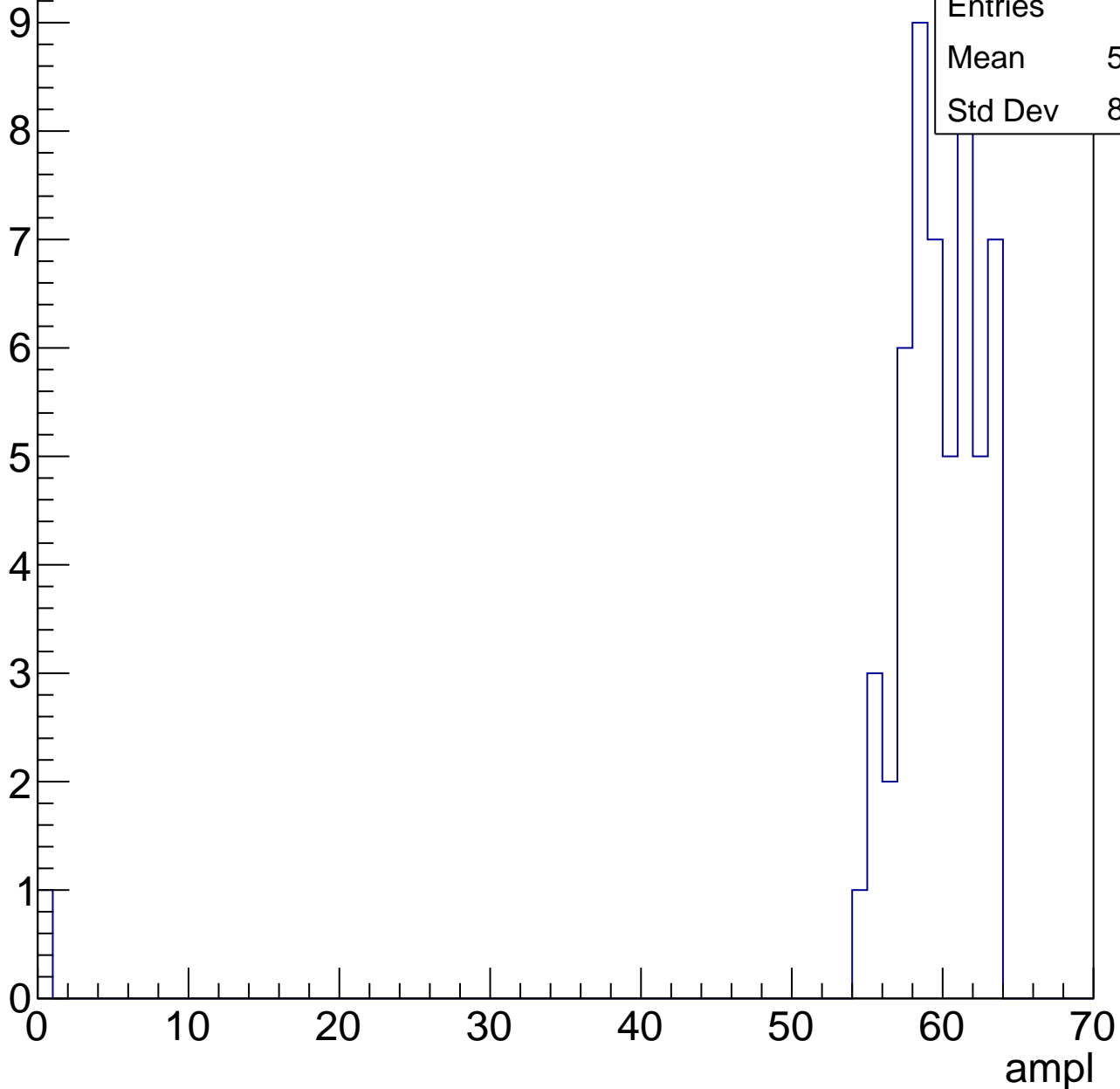


# B1L101S, U11-ch118, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

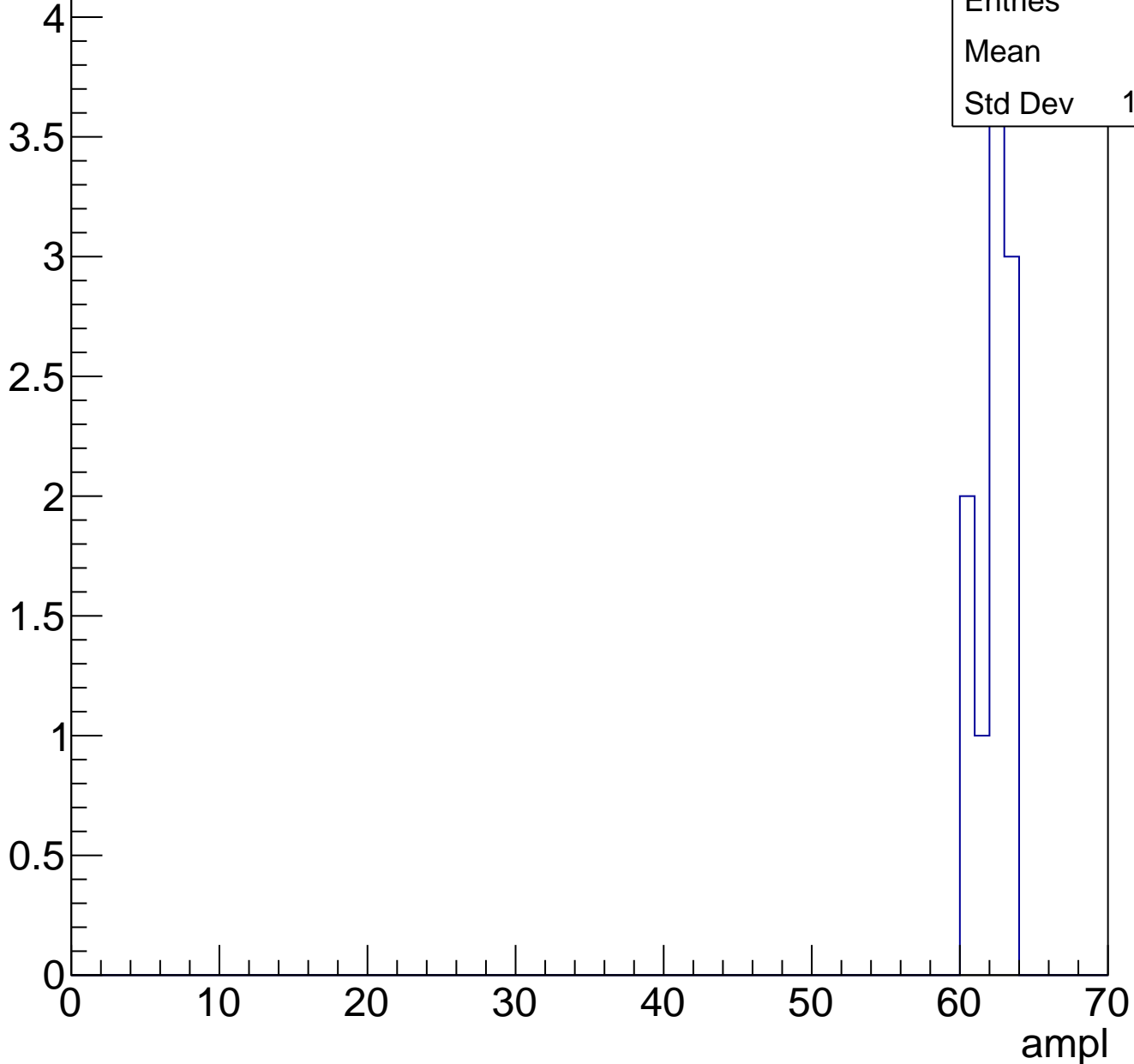
Entries	55
Mean	58.33
Std Dev	8.288



# B1L101S, U11-ch118, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch118, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U11-ch119, adc0

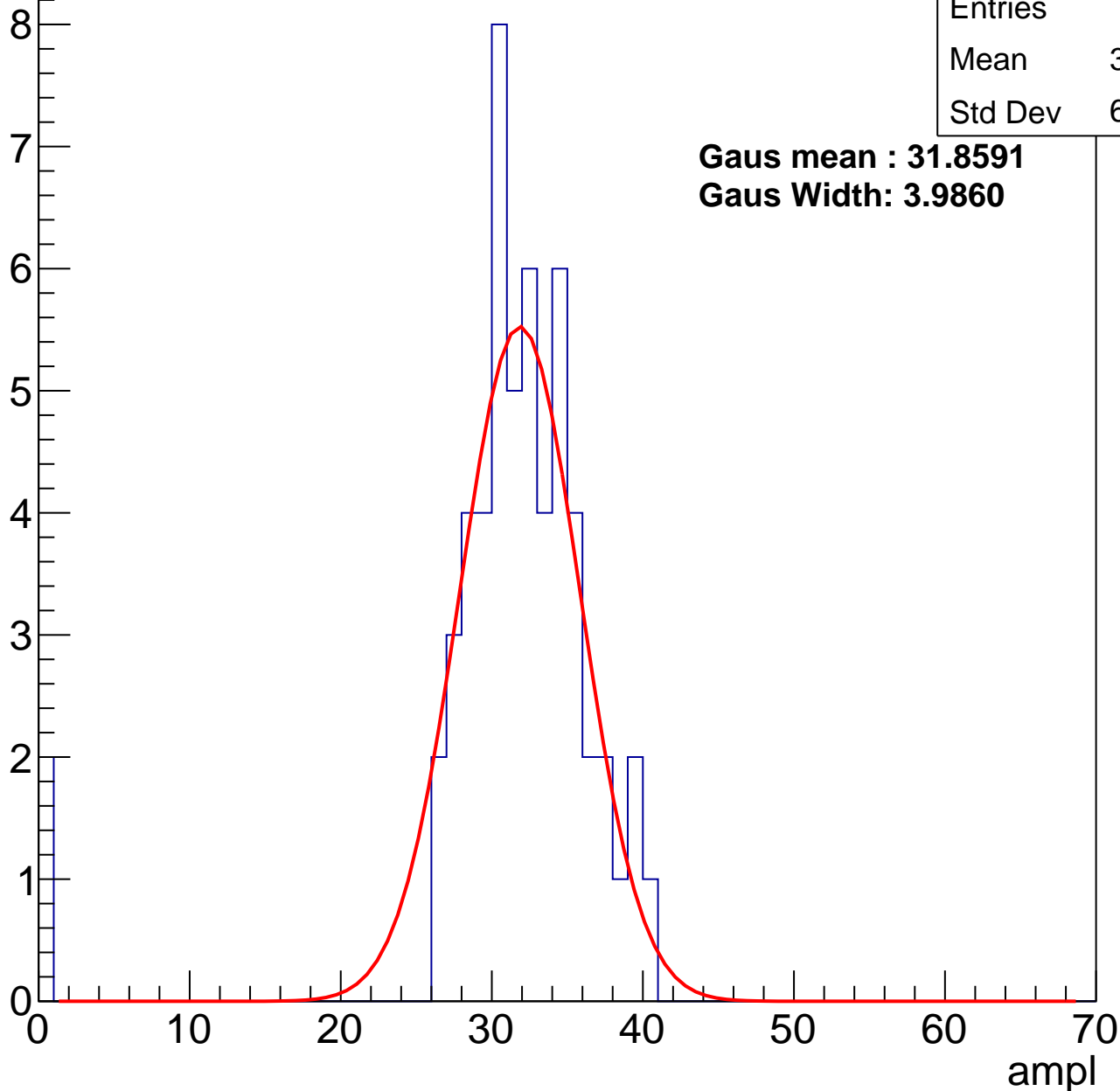
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	30.82
Std Dev	6.812

**Gaus mean : 31.8591**

**Gaus Width: 3.9860**



# B1L101S, U11-ch119, adc1

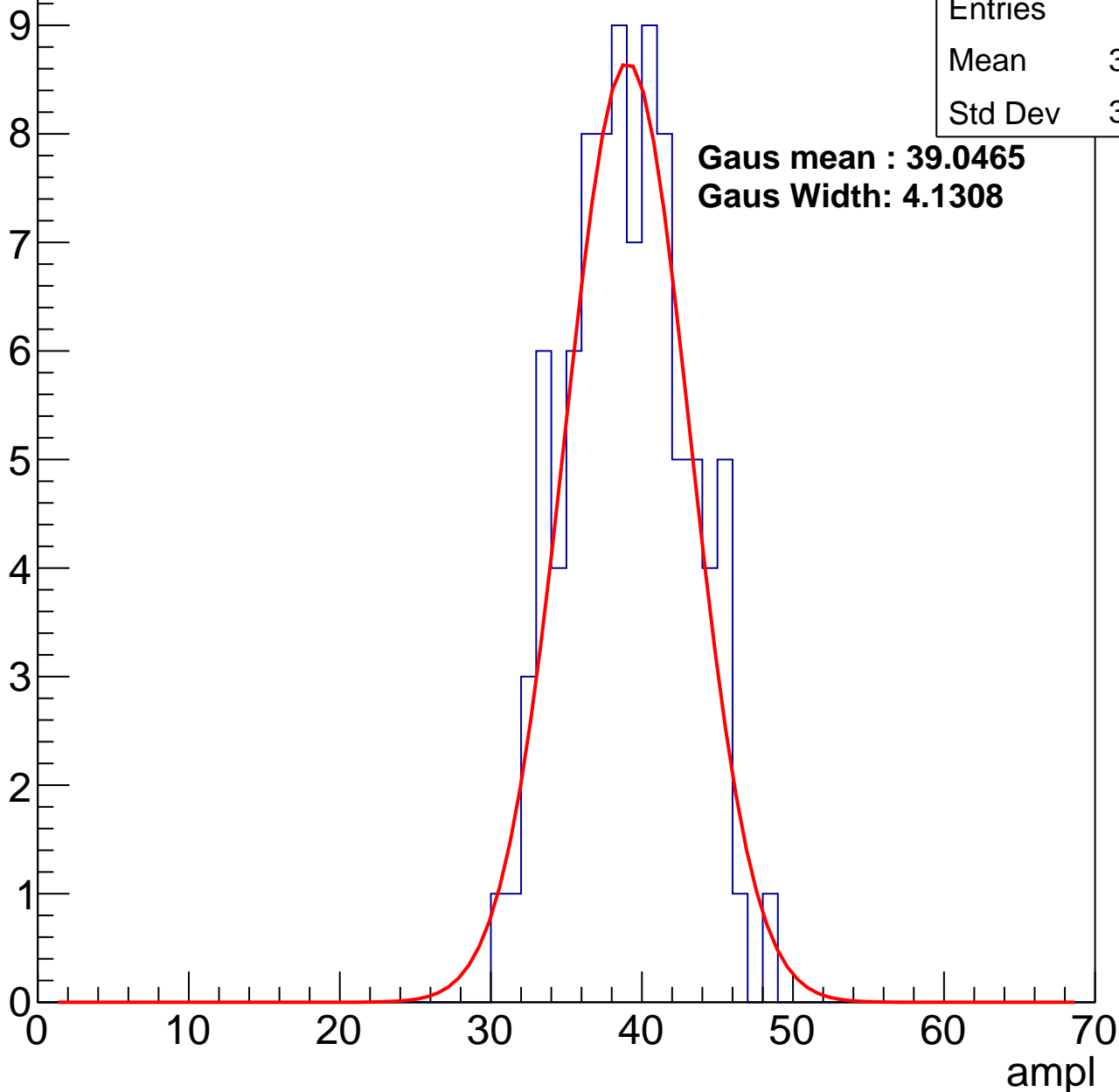
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	91
Mean	38.55
Std Dev	3.886

**Gaus mean : 39.0465**

**Gaus Width: 4.1308**



# B1L101S, U11-ch119, adc2

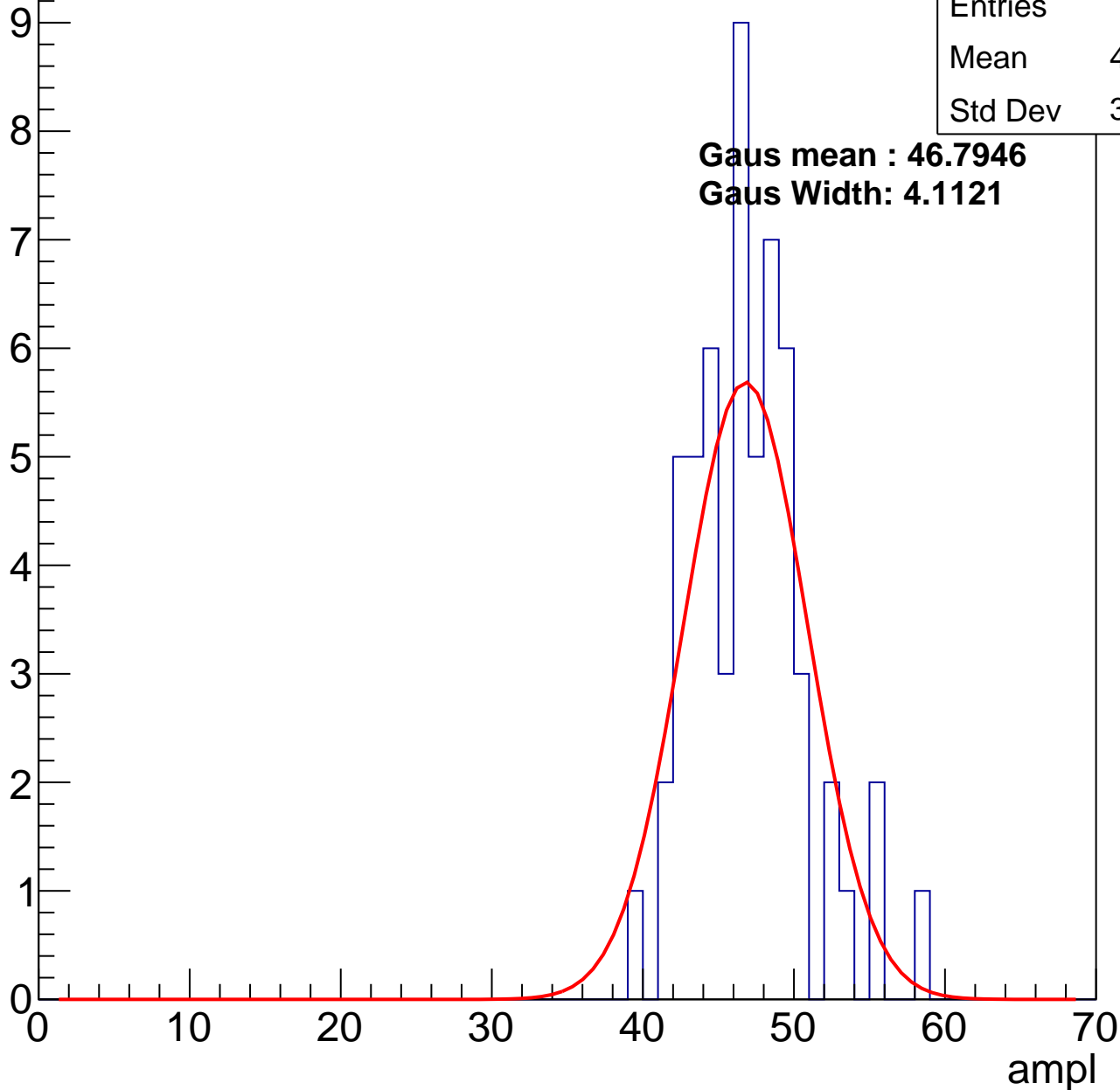
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	46.53
Std Dev	3.706

**Gaus mean : 46.7946**

**Gaus Width: 4.1121**



# B1L101S, U11-ch119, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	65
Mean	51.97
Std Dev	3.21

Entry

10

8

6

4

2

0

0

10

20

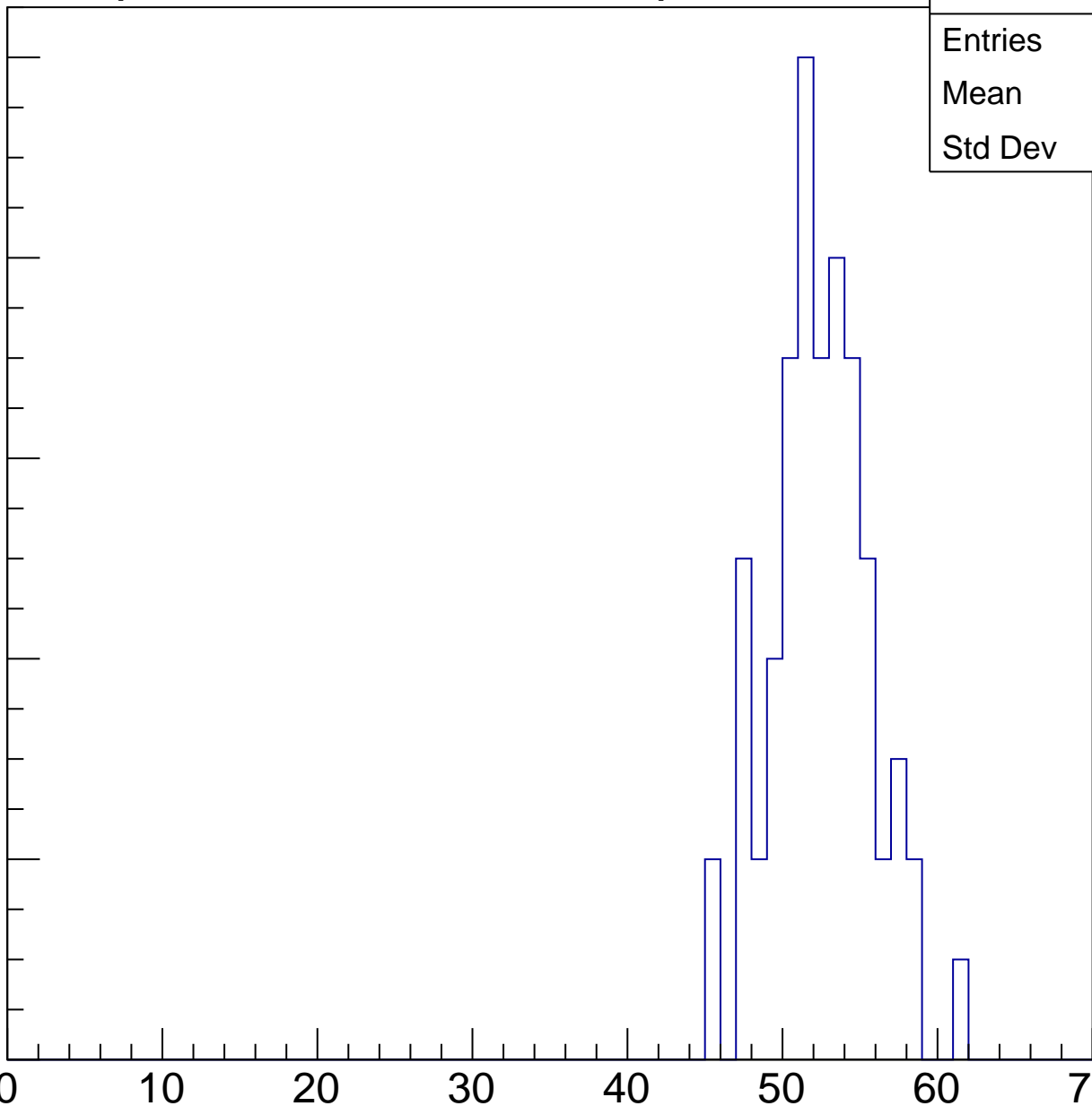
30

40

50

60

ampl

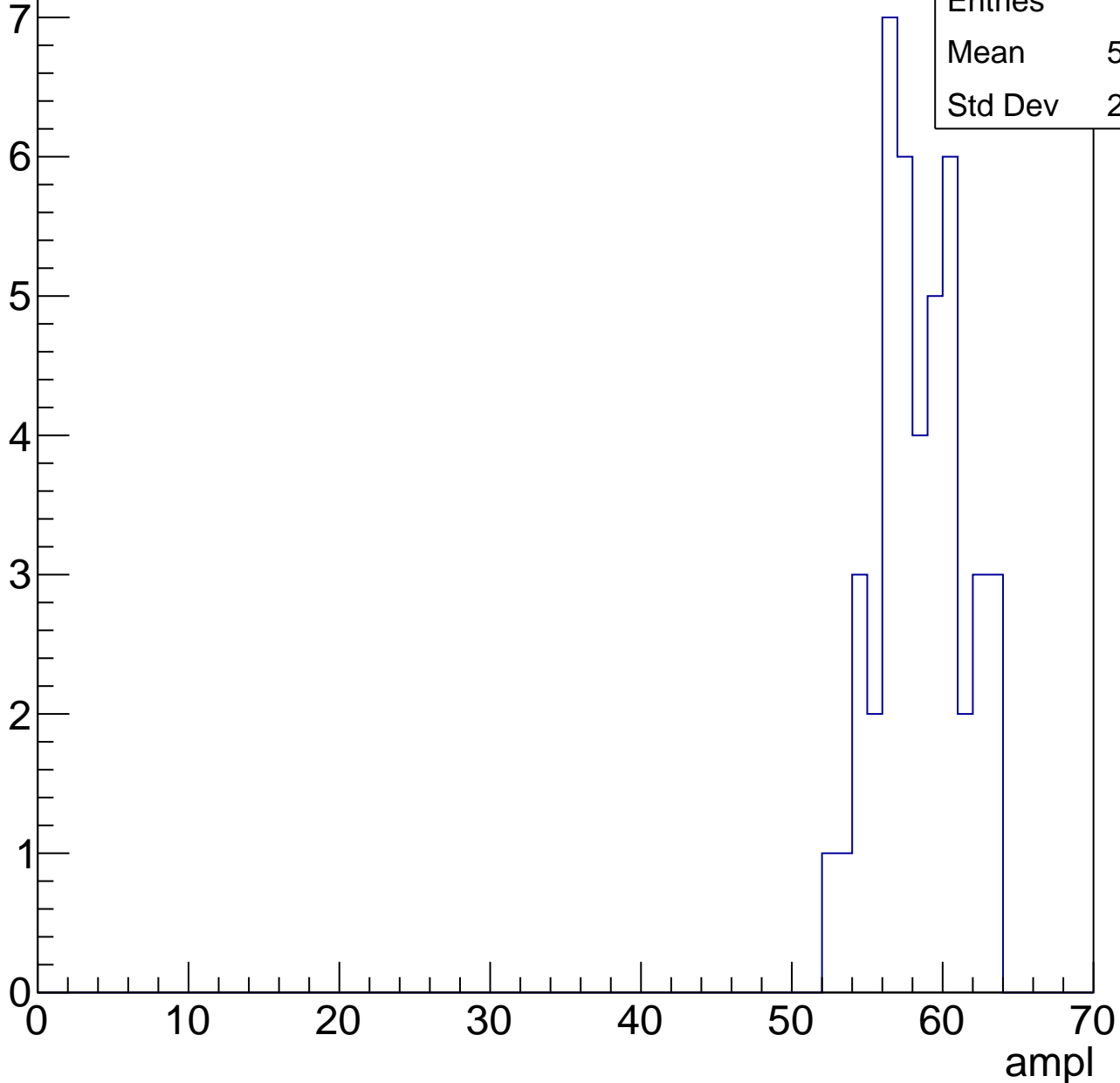


# B1L101S, U11-ch119, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	43
Mean	58.02
Std Dev	2.774

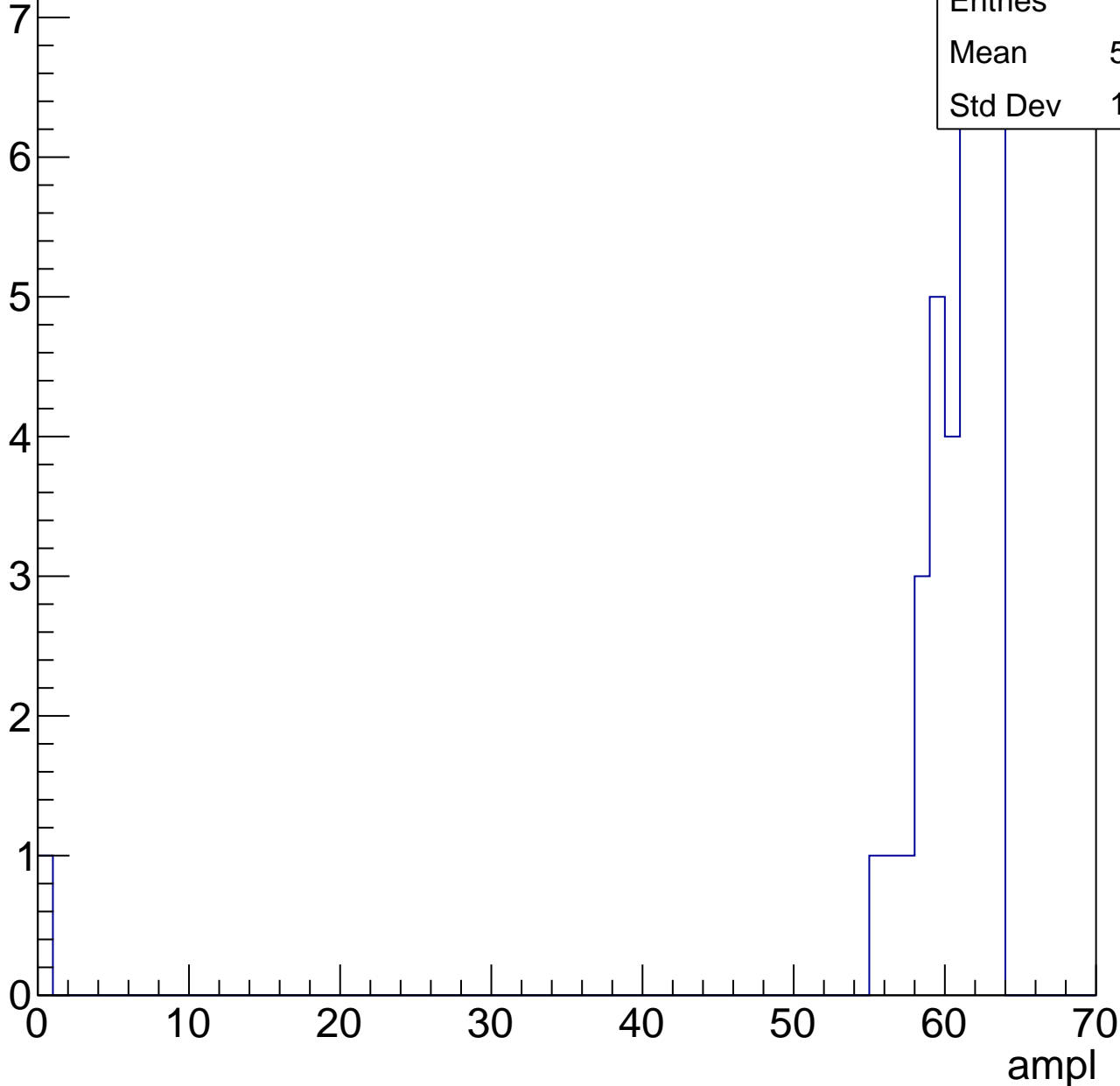


# B1L101S, U11-ch119, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	37
Mean	58.89
Std Dev	10.03



# B1L101S, U11-ch119, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L101S, U11-ch119, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U11-ch120, adc0

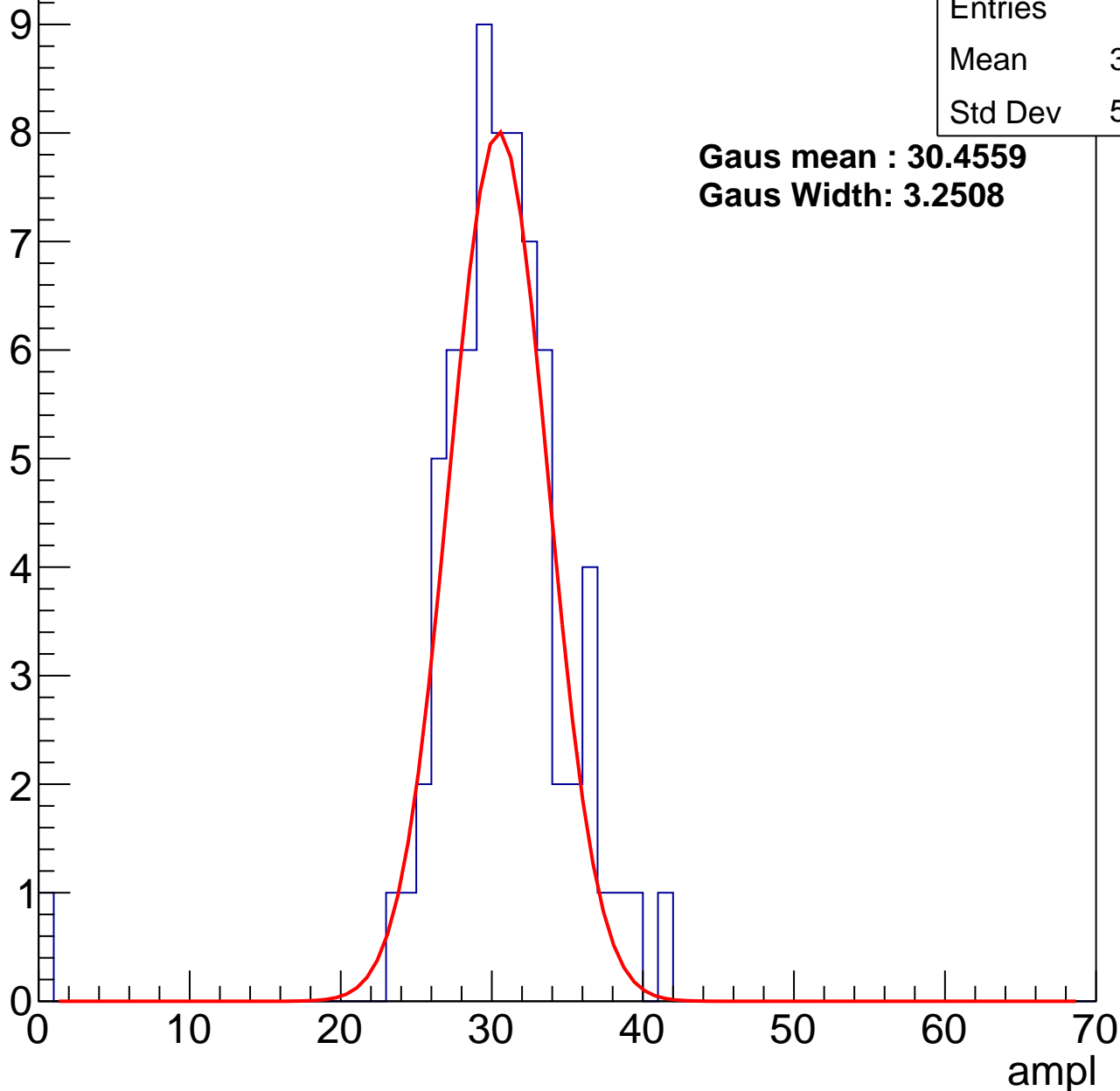
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	30.07
Std Dev	5.045

**Gaus mean : 30.4559**

**Gaus Width: 3.2508**



# B1L101S, U11-ch120, adc1

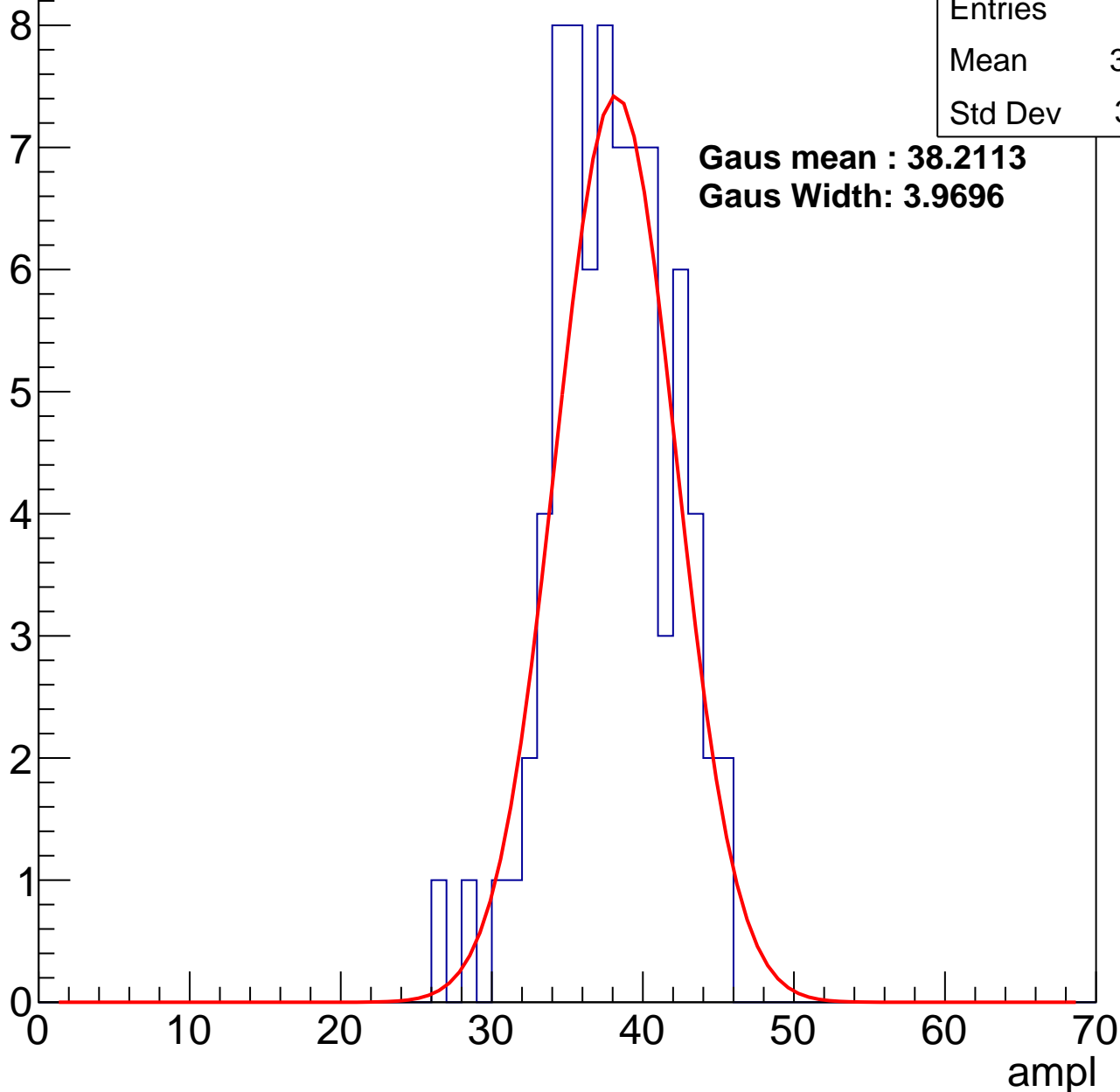
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	78
Mean	37.42
Std Dev	3.861

**Gaus mean : 38.2113**

**Gaus Width: 3.9696**



# B1L101S, U11-ch120, adc2

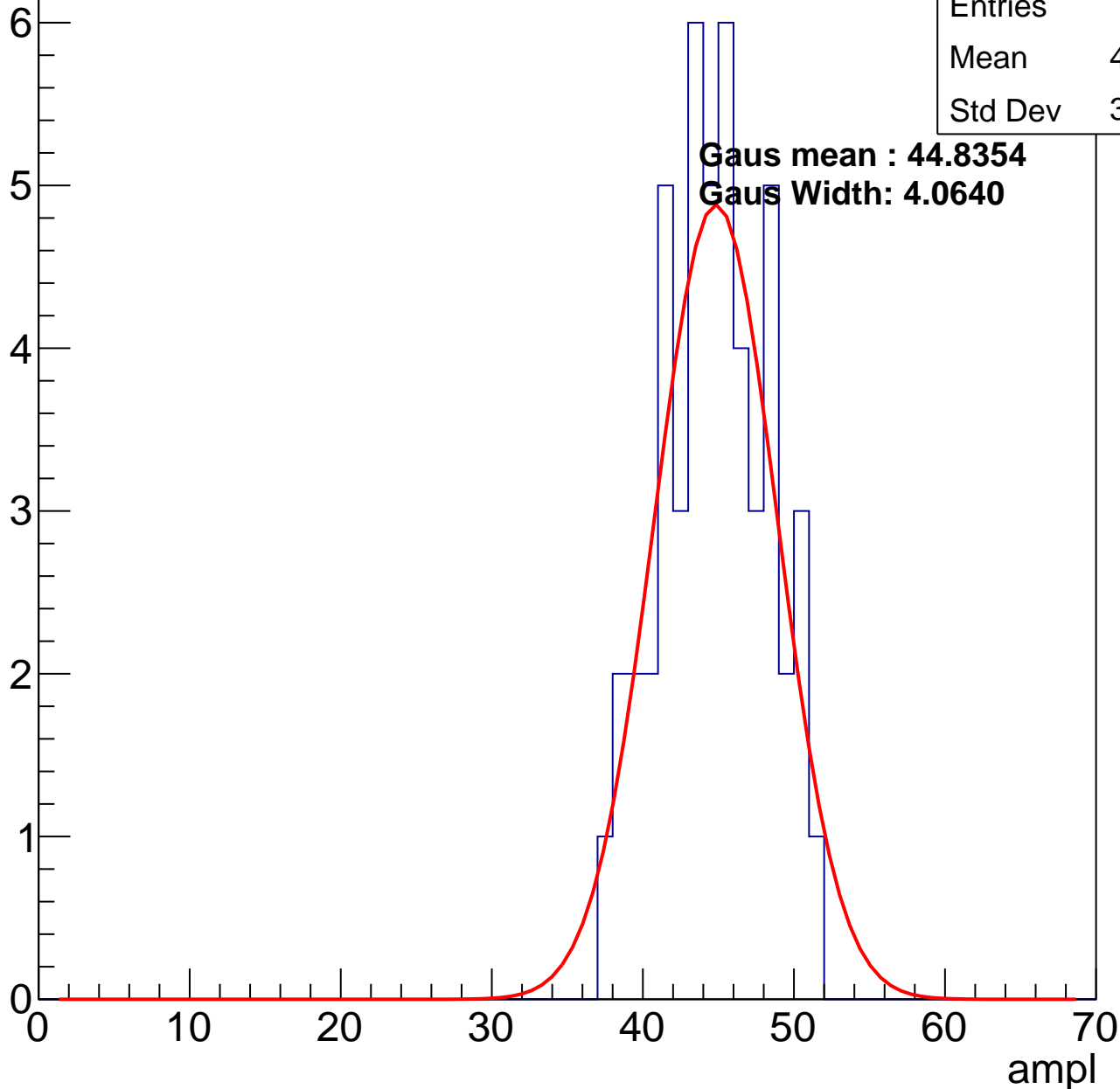
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	44.28
Std Dev	3.459

**Gaus mean : 44.8354**

**Gaus Width: 4.0640**

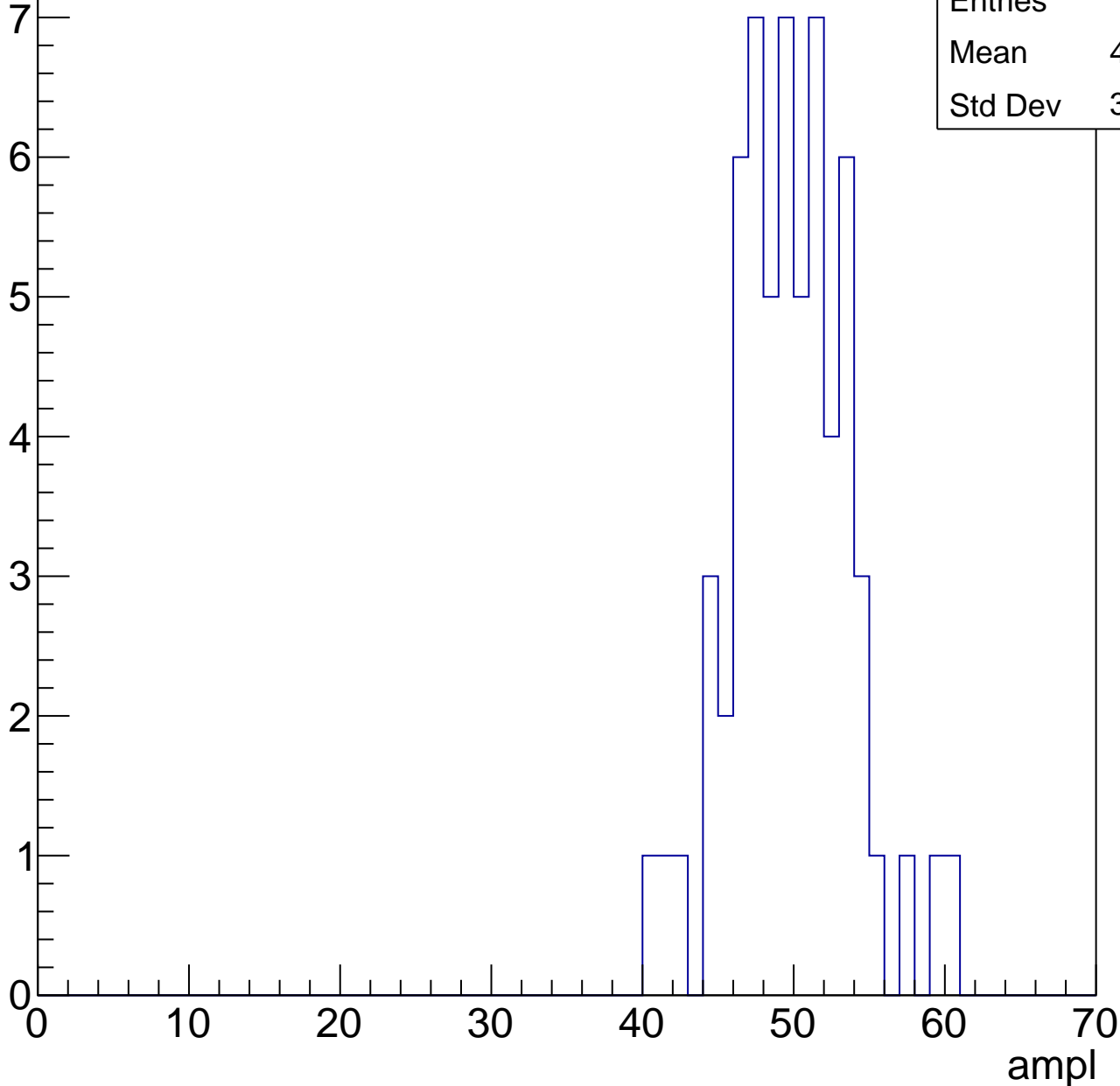


# B1L101S, U11-ch120, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	49.34
Std Dev	3.898

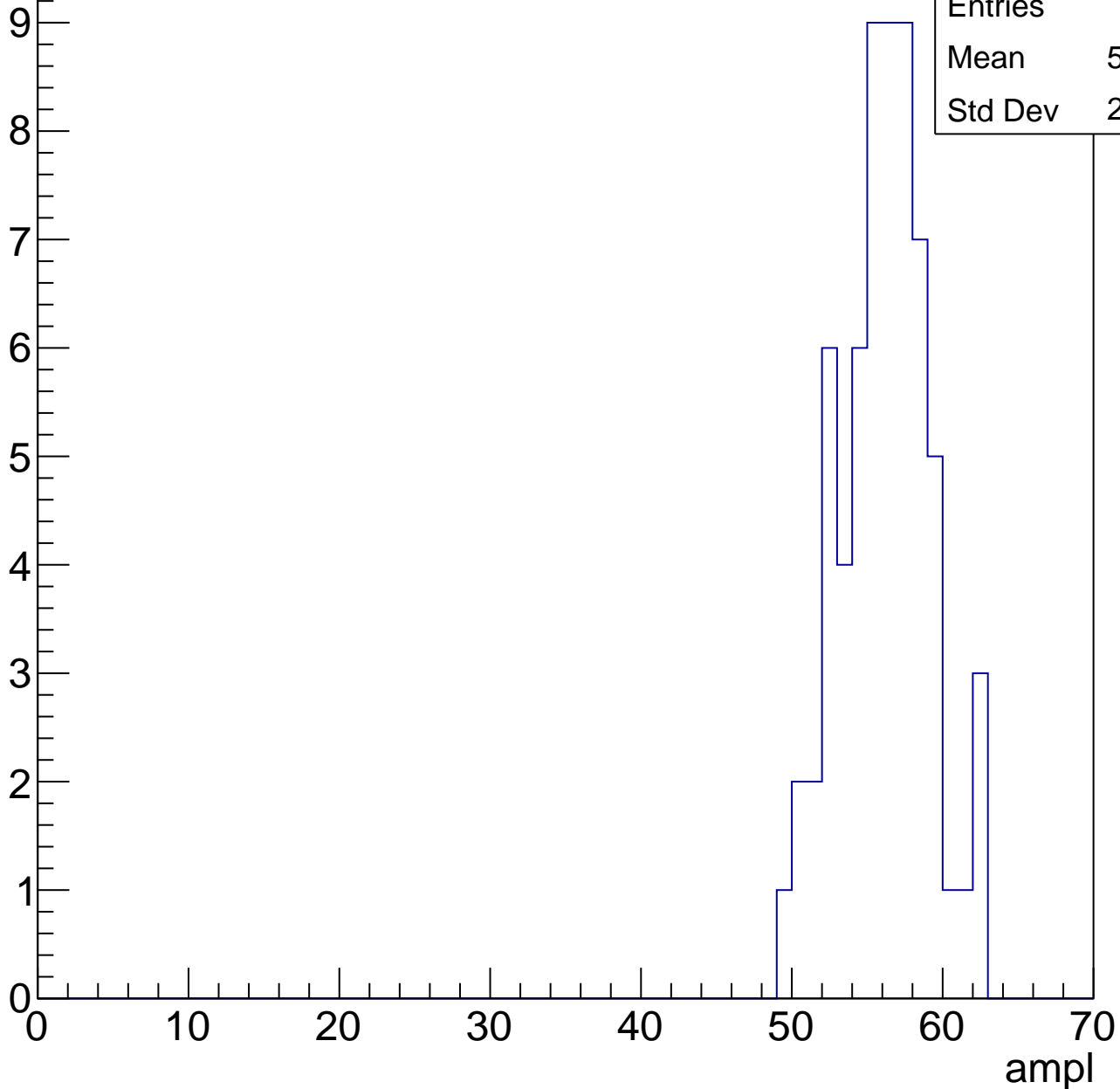


# B1L101S, U11-ch120, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	55.68
Std Dev	2.936

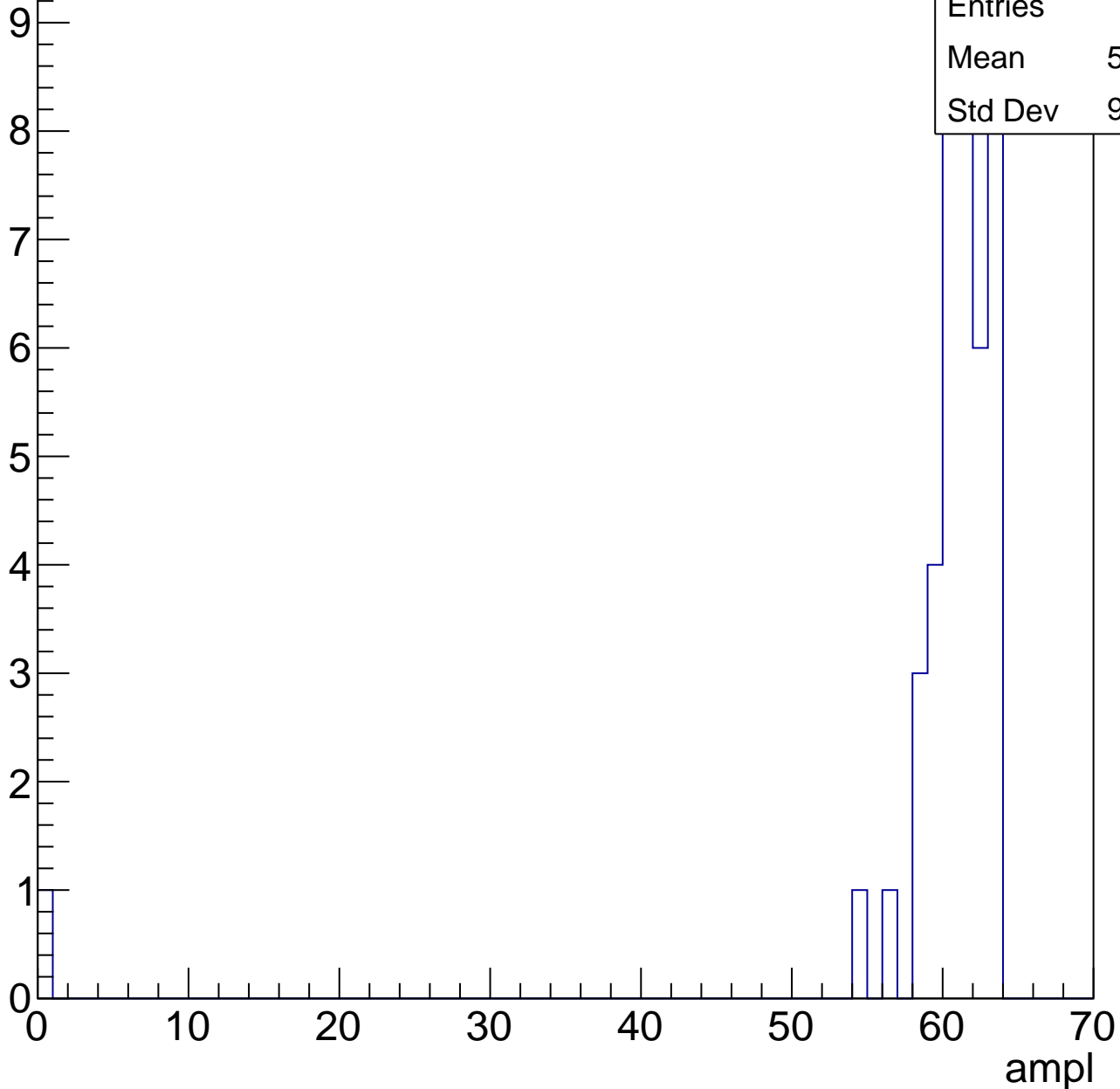


# B1L101S, U11-ch120, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	42
Mean	59.24
Std Dev	9.459



# B1L101S, U11-ch120, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch120, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U11-ch121, adc0

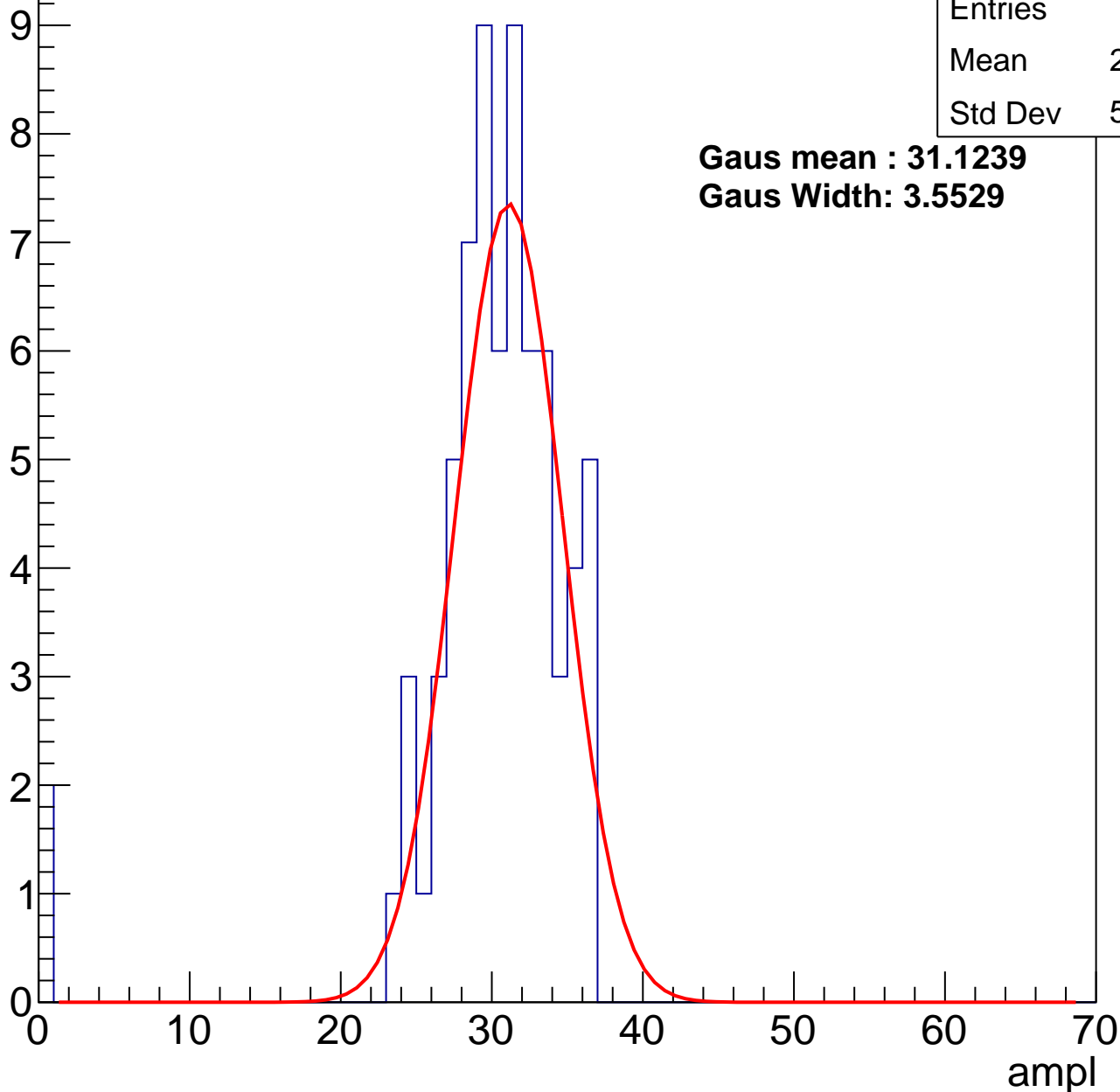
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	29.44
Std Dev	5.982

**Gaus mean : 31.1239**

**Gaus Width: 3.5529**



# B1L101S, U11-ch121, adc1

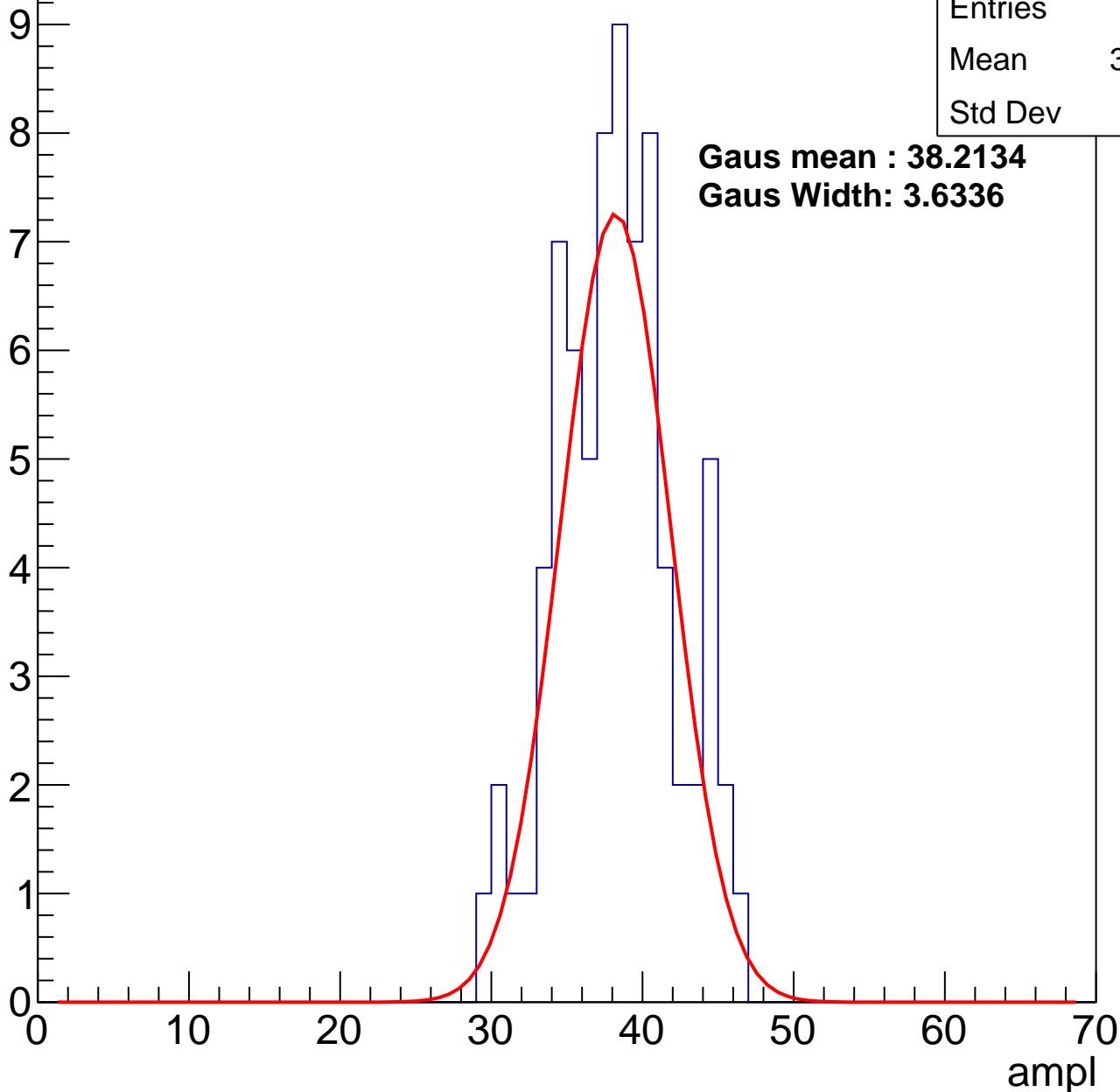
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	37.77
Std Dev	3.8

**Gaus mean : 38.2134**

**Gaus Width: 3.6336**



# B1L101S, U11-ch121, adc2

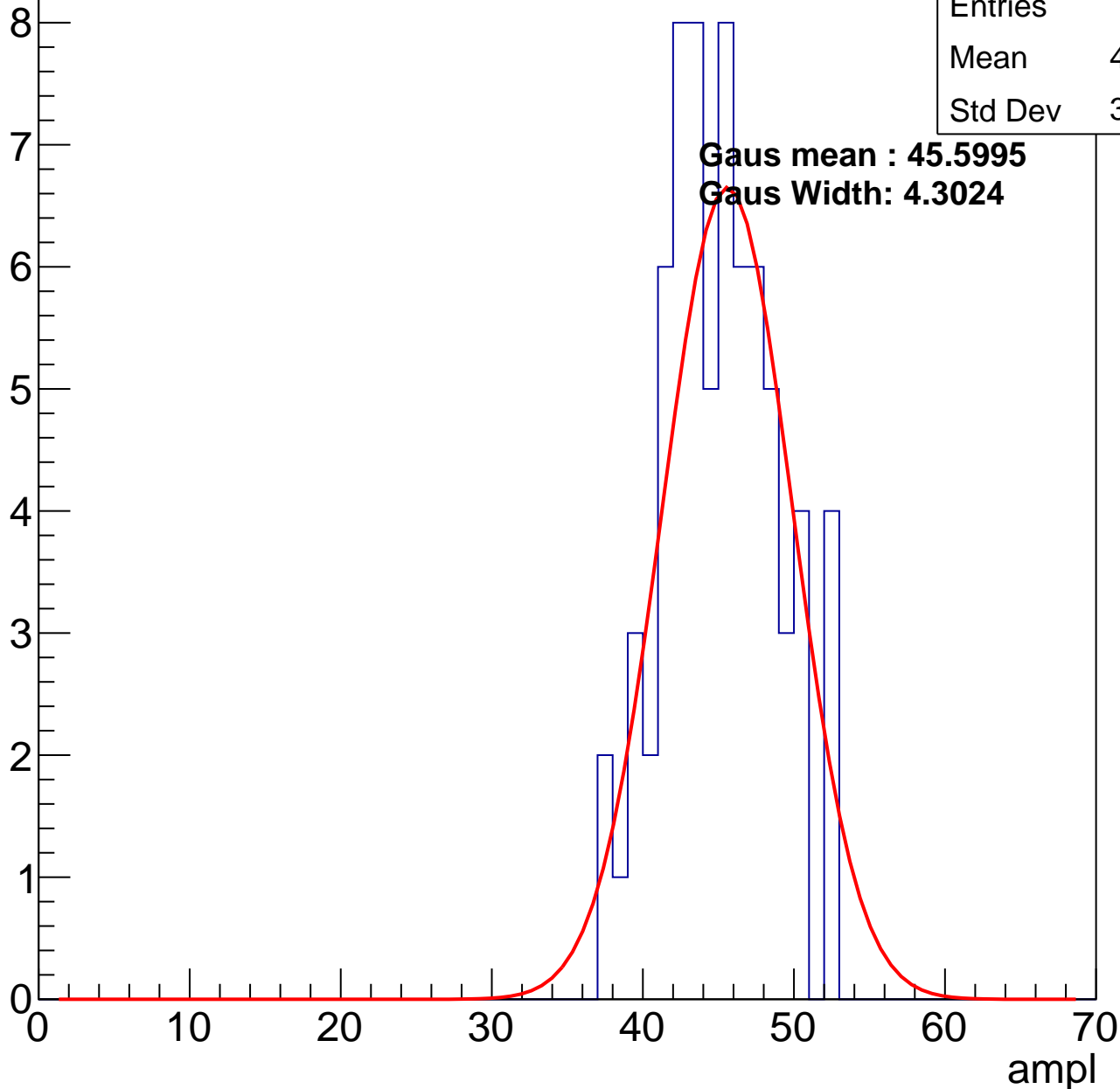
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	44.62
Std Dev	3.655

**Gaus mean : 45.5995**

**Gaus Width: 4.3024**

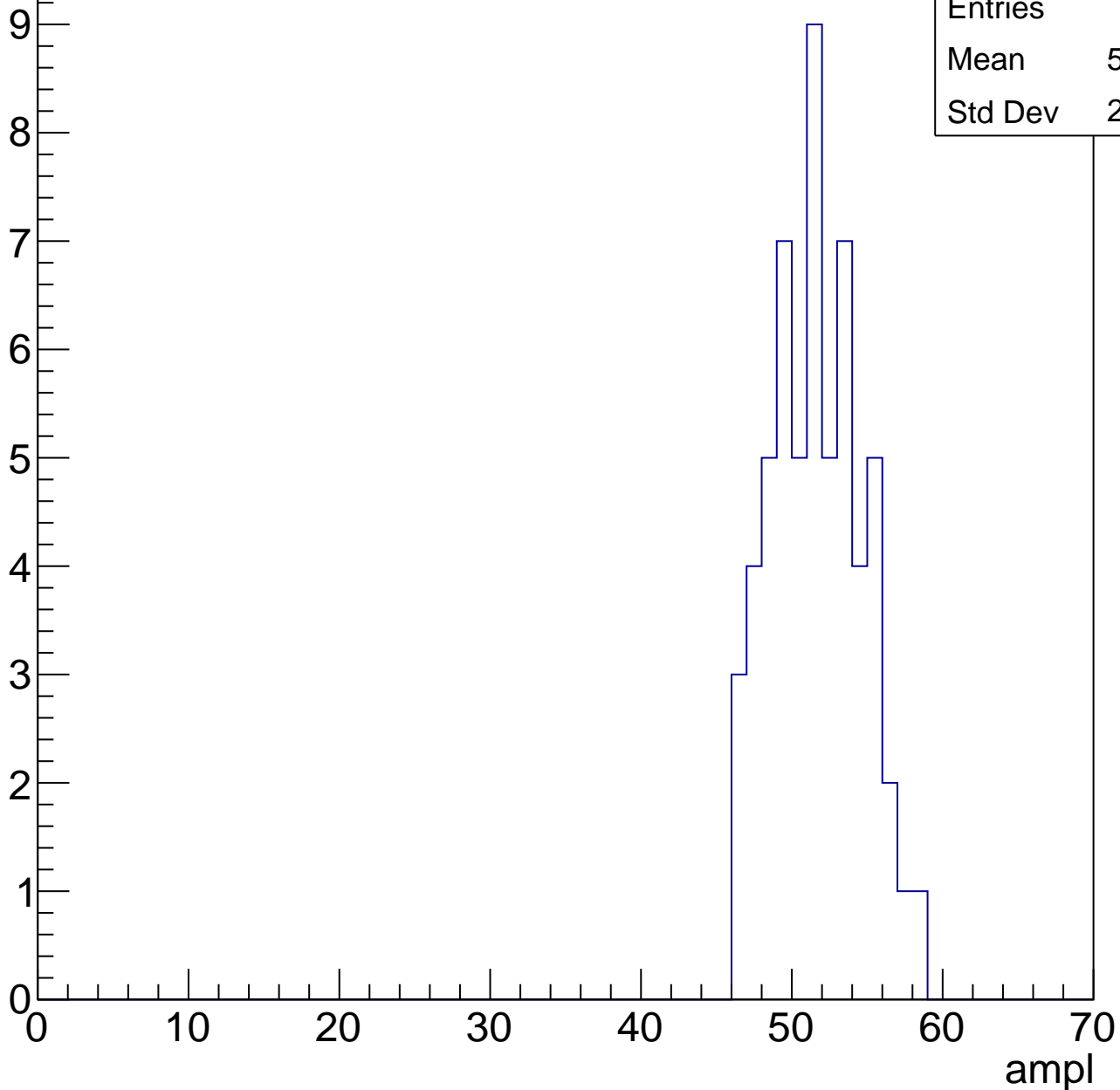


# B1L101S, U11-ch121, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

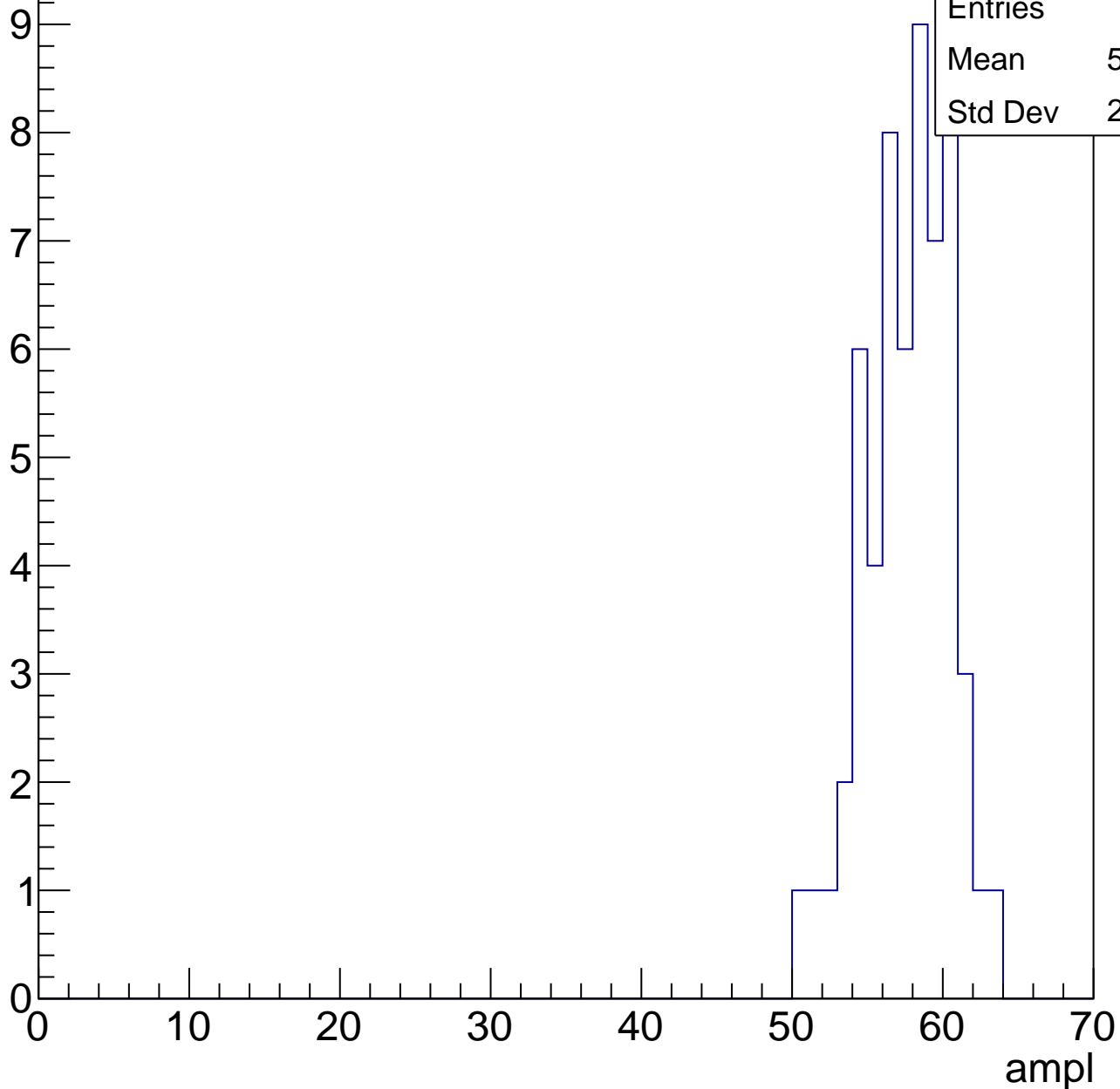
Entries	58
Mean	51.16
Std Dev	2.935



# B1L101S, U11-ch121, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



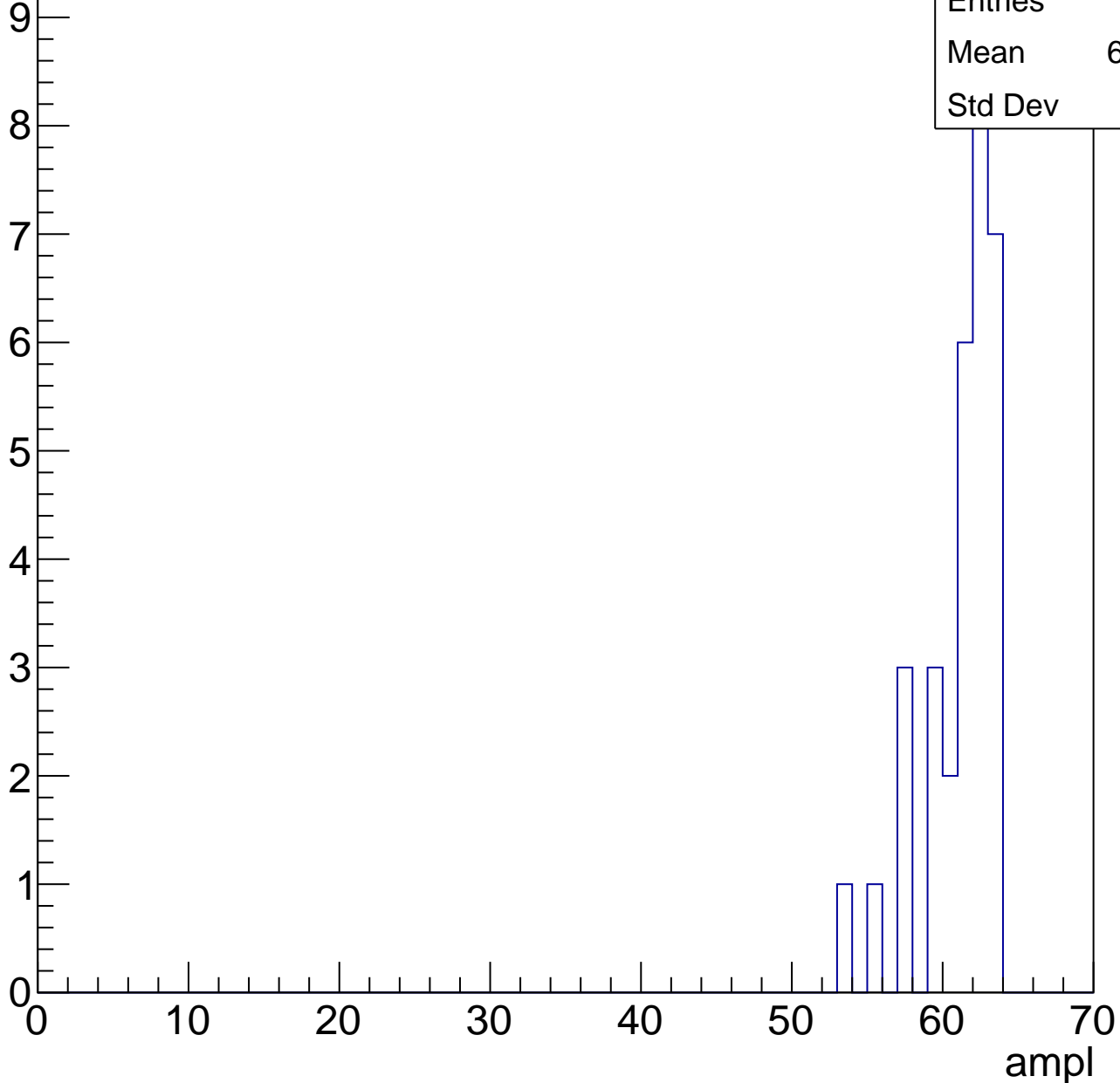
Entries	58
Mean	57.17
Std Dev	2.743

# B1L101S, U11-ch121, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	32
Mean	60.66
Std Dev	2.47



# B1L101S, U11-ch121, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

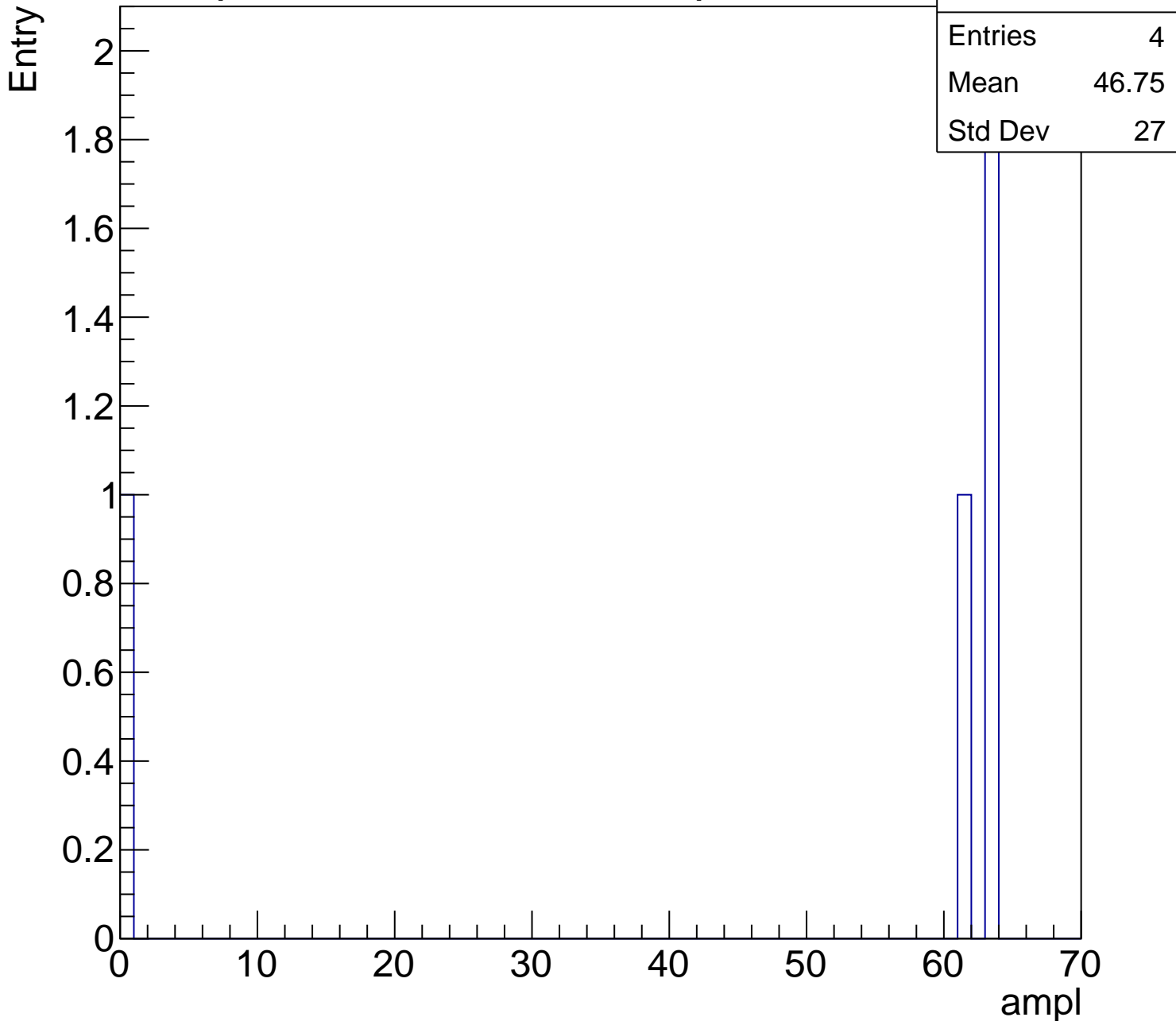
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	46.75
Std Dev	27

0 10 20 30 40 50 60 70

ampl





# B1L101S, U11-ch121, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U11-ch122, adc0

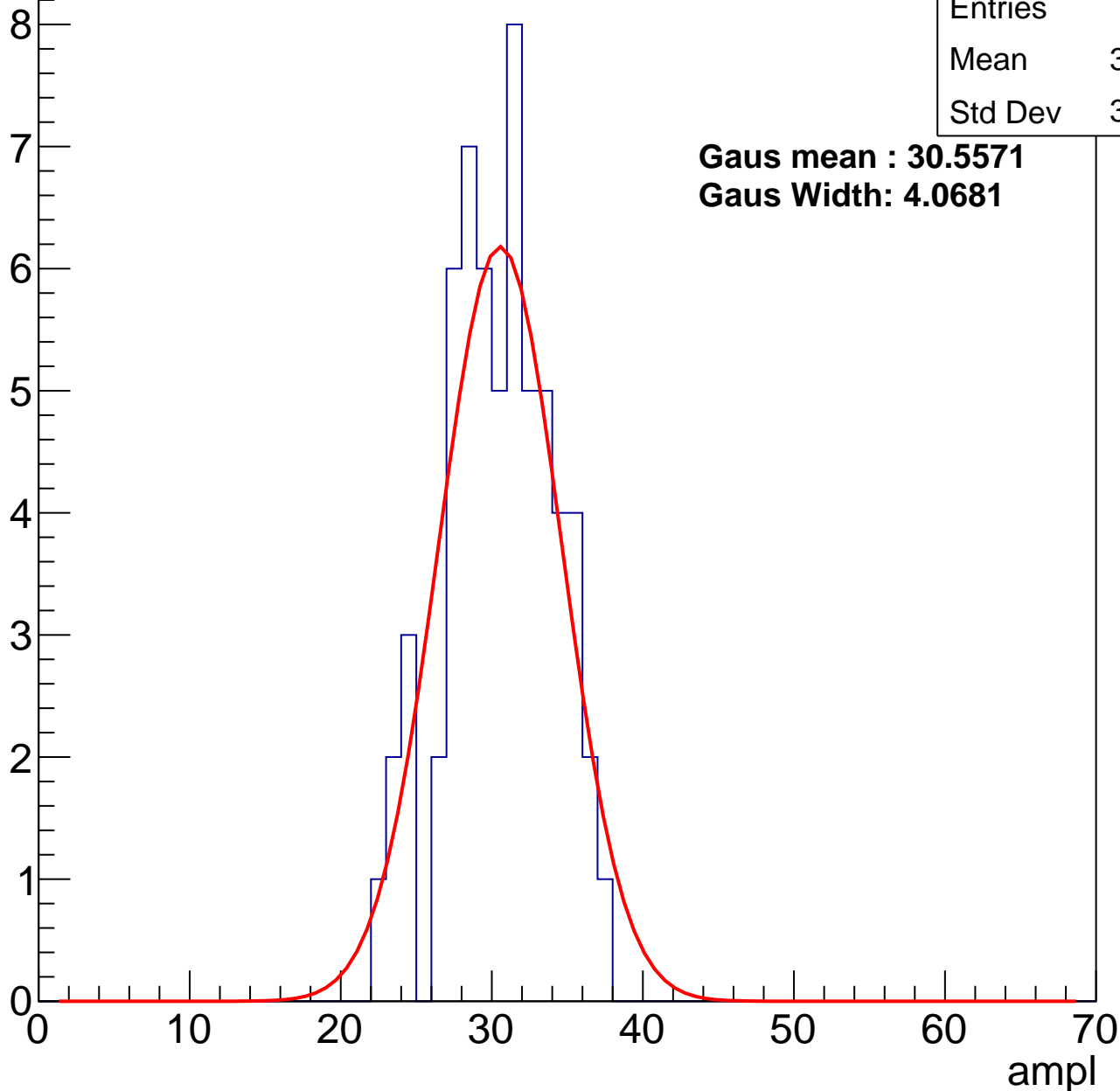
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	30.03
Std Dev	3.502

**Gaus mean : 30.5571**

**Gaus Width: 4.0681**



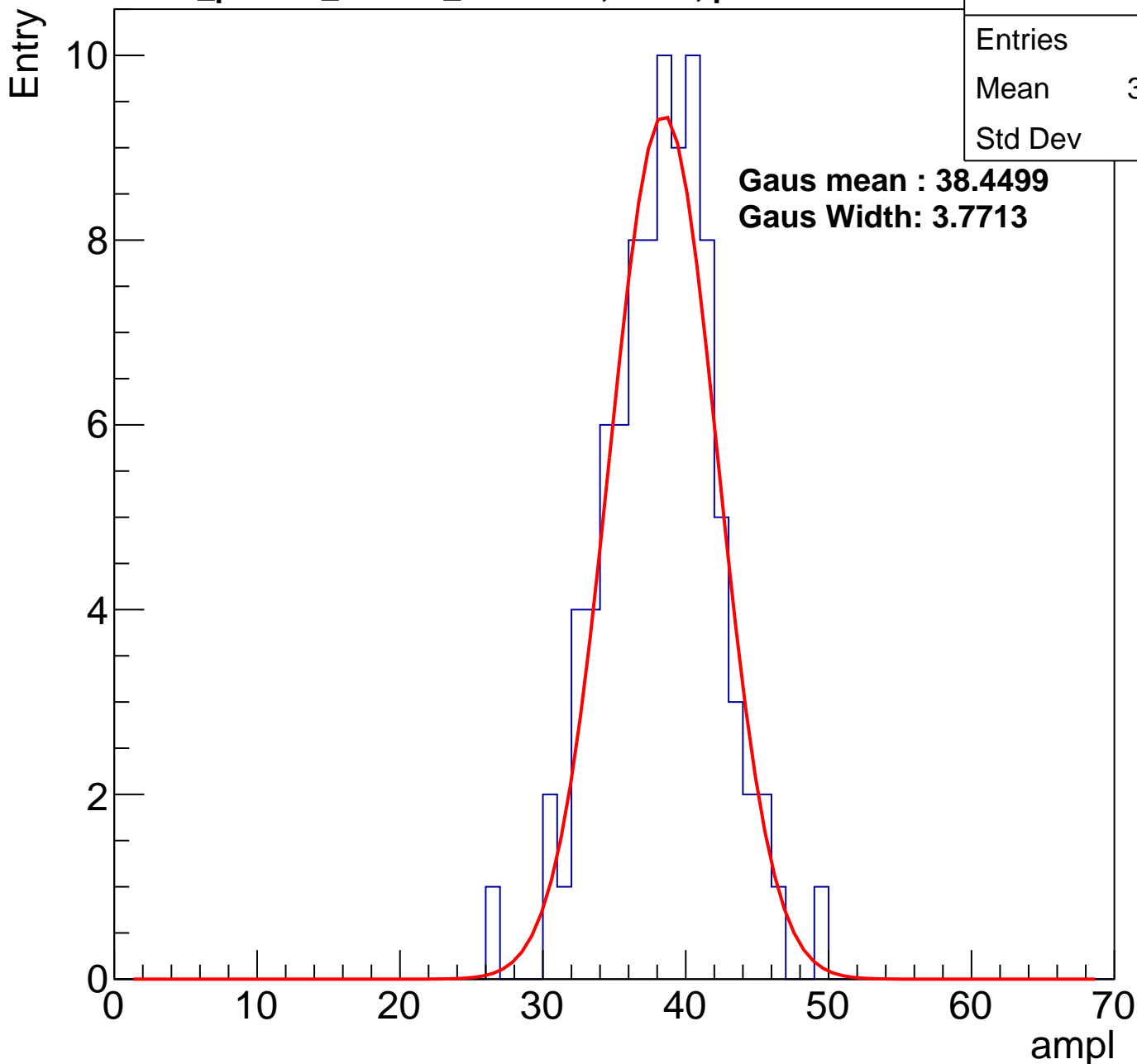
# B1L101S, U11-ch122, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	91
Mean	37.87
Std Dev	3.9

**Gaus mean : 38.4499**

**Gaus Width: 3.7713**



# B1L101S, U11-ch122, adc2

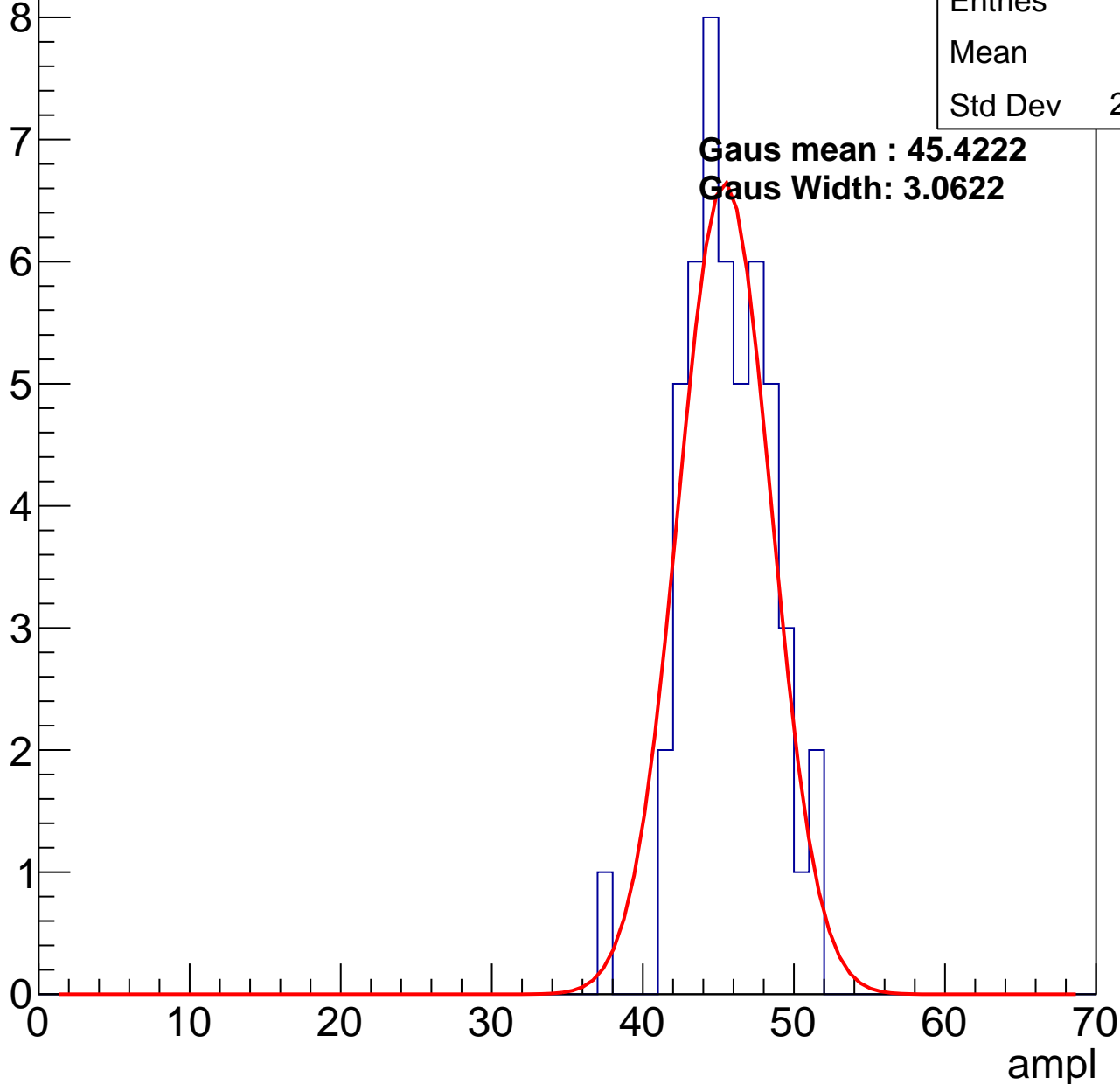
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	45.2
Std Dev	2.793

**Gaus mean : 45.4222**

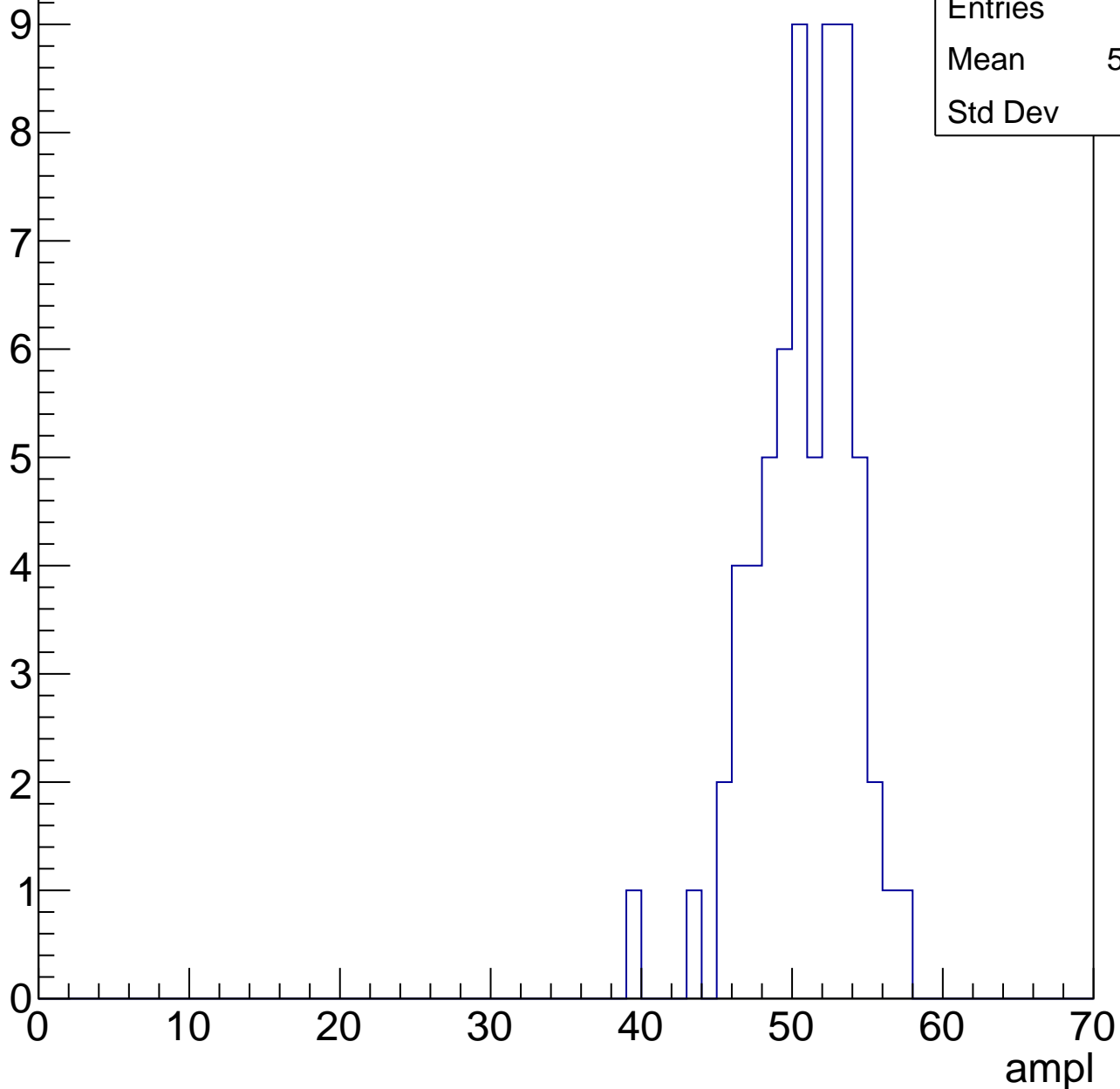
**Gaus Width: 3.0622**



# B1L101S, U11-ch122, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



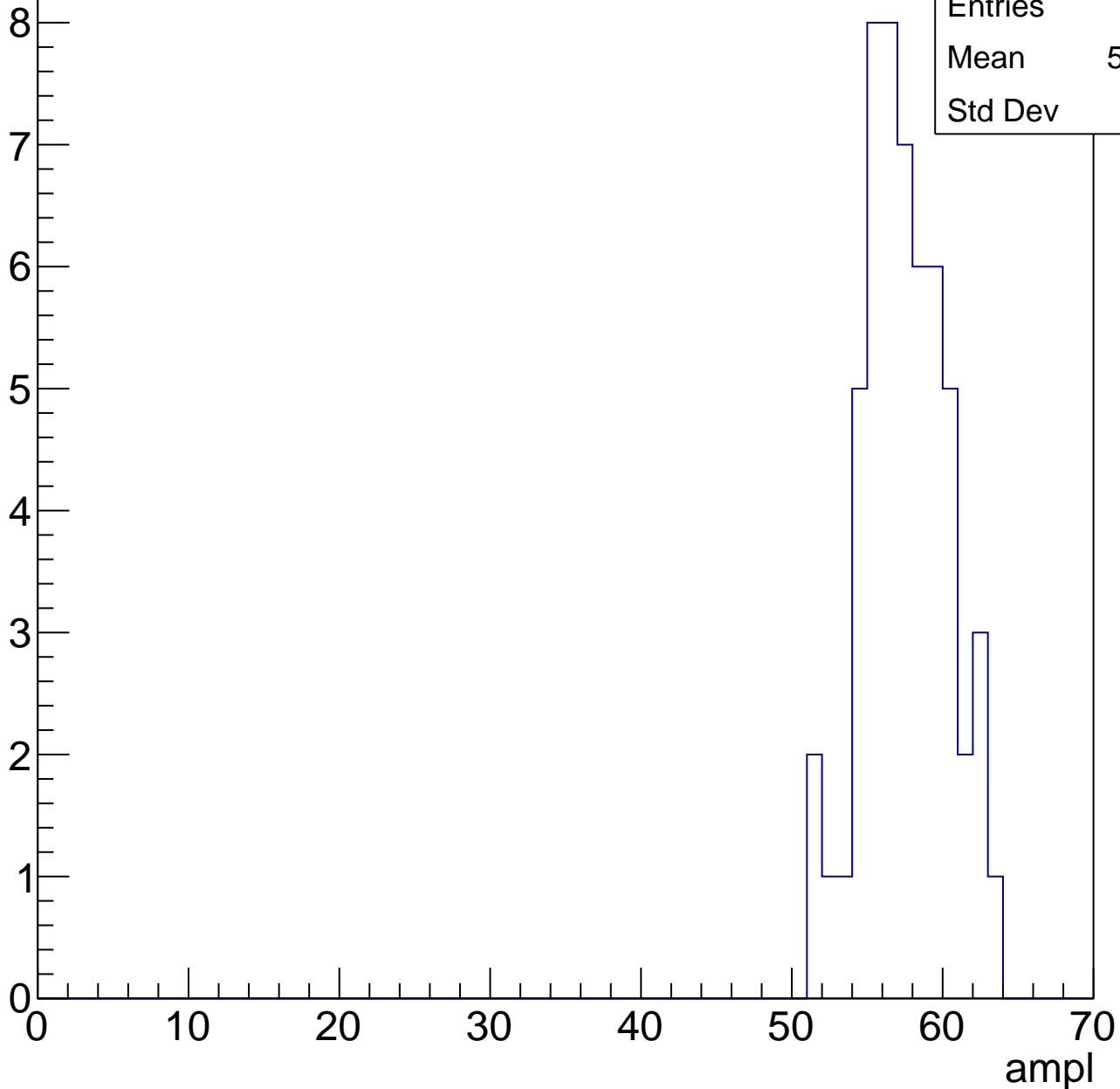
Entries	64
Mean	50.33
Std Dev	3.25

# B1L101S, U11-ch122, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	57.04
Std Dev	2.75

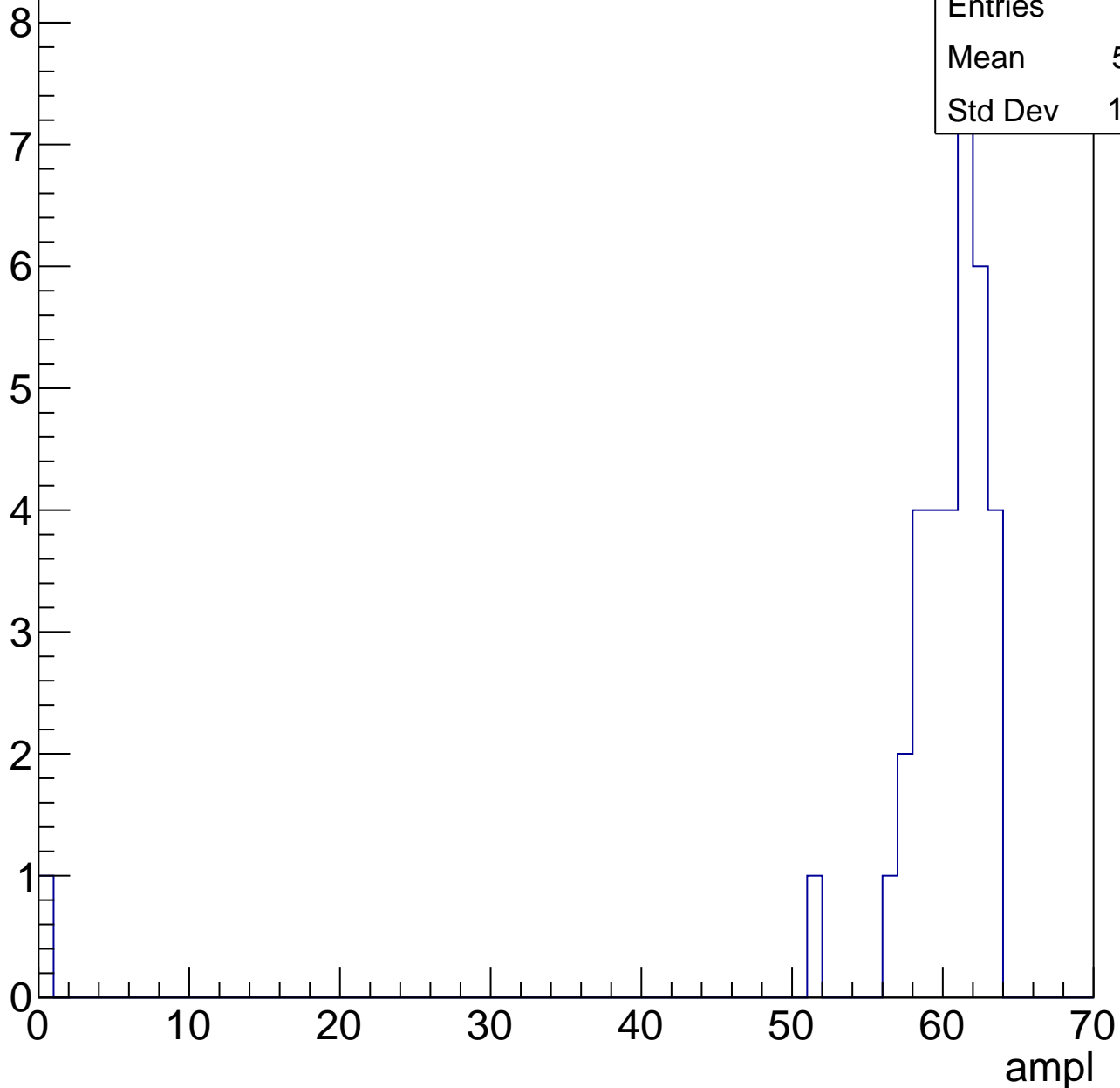


# B1L101S, U11-ch122, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	35
Mean	58.31
Std Dev	10.29

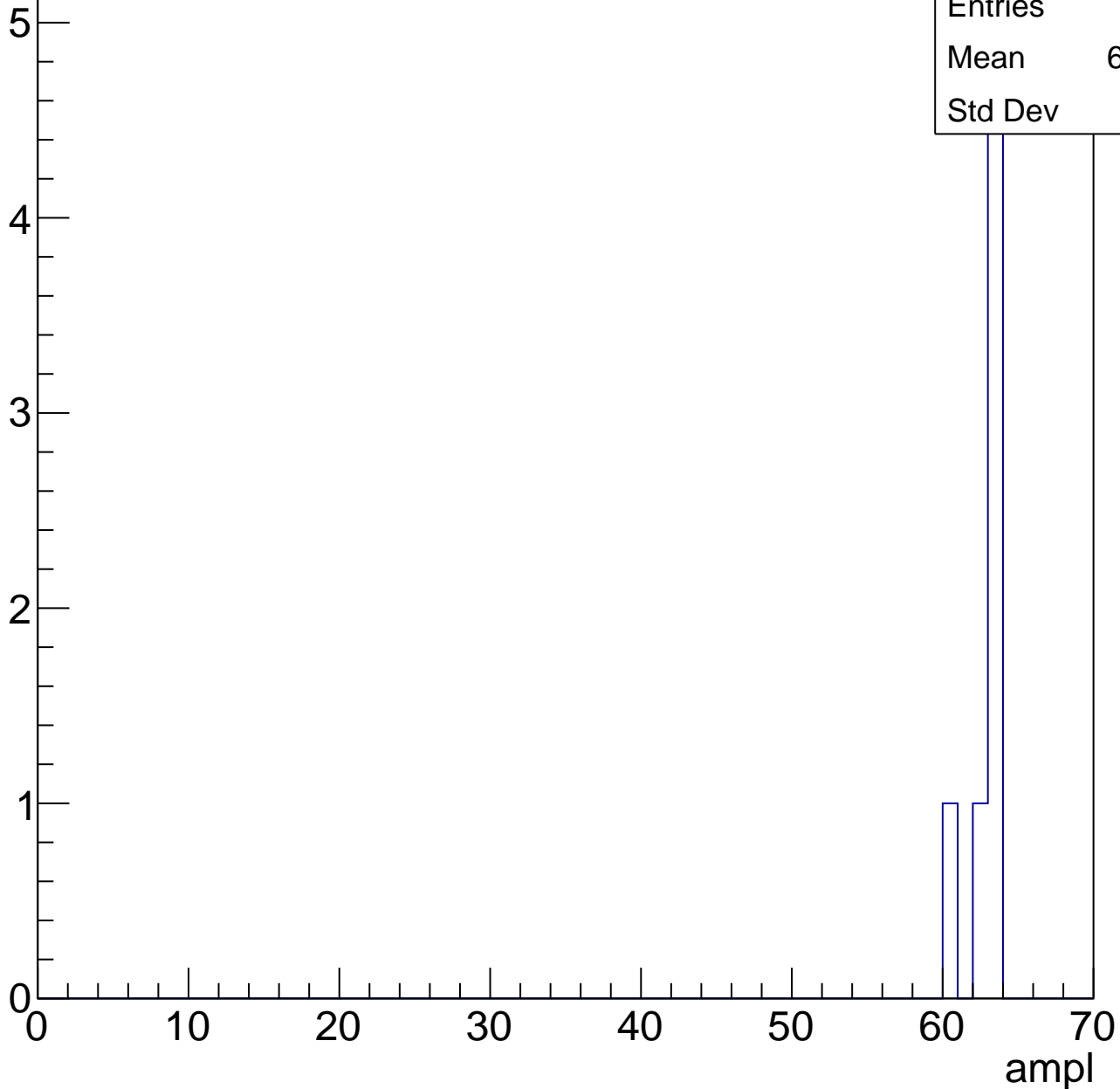


# B1L101S, U11-ch122, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	7
Mean	62.43
Std Dev	1.05





# B1L101S, U11-ch122, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U11-ch123, adc0

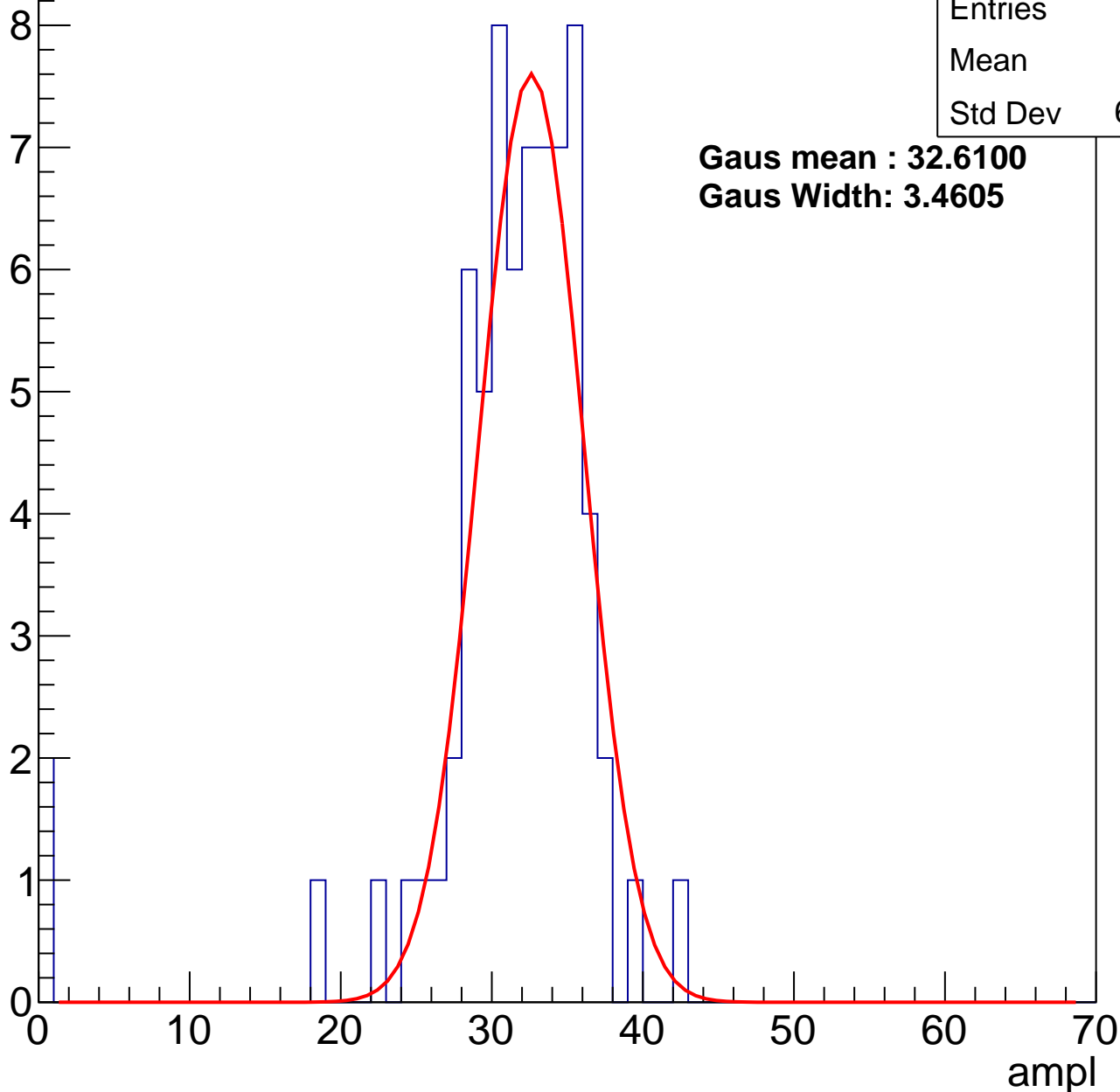
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	30.7
Std Dev	6.471

**Gaus mean : 32.6100**

**Gaus Width: 3.4605**



# B1L101S, U11-ch123, adc1

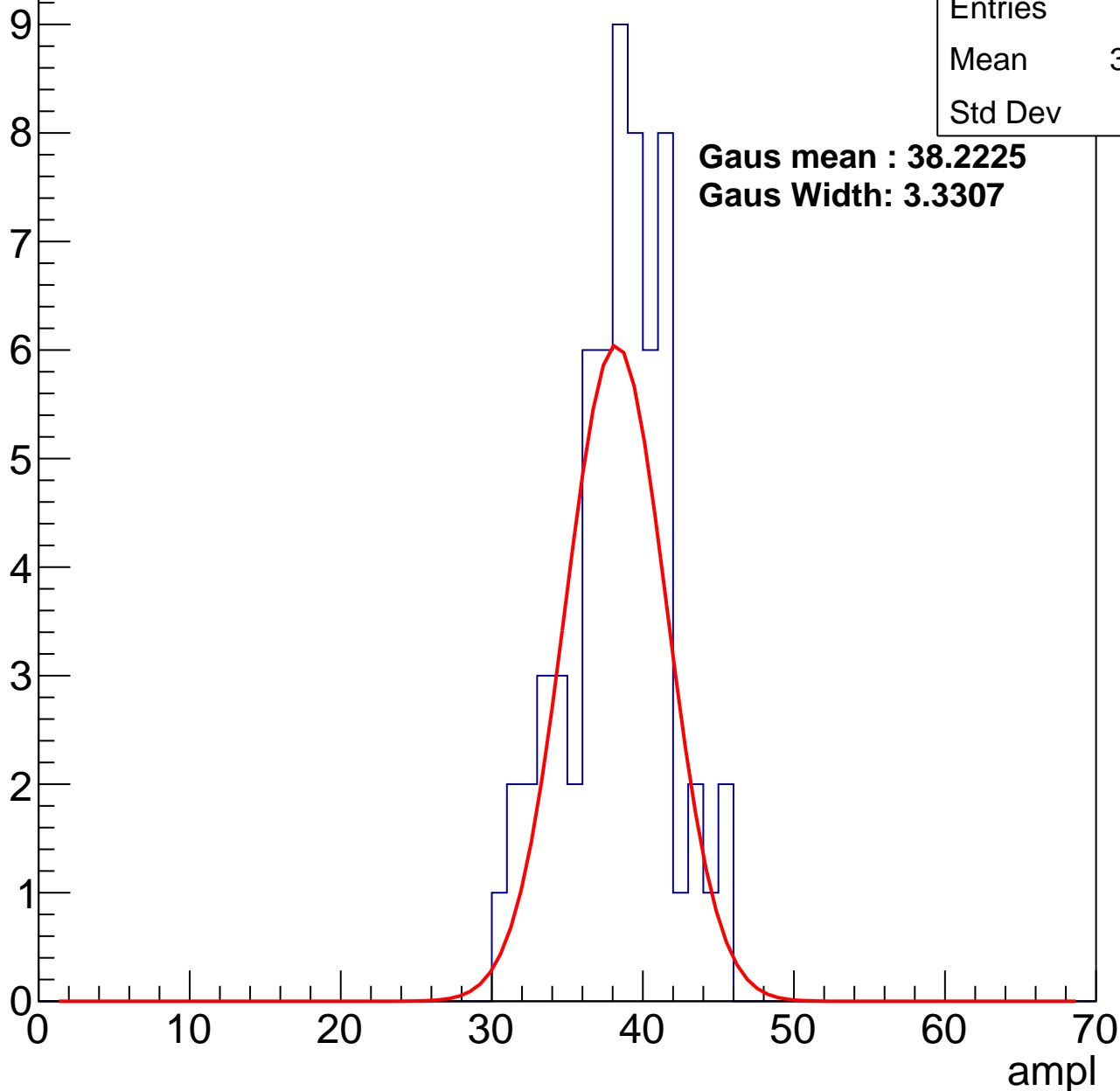
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	37.89
Std Dev	3.38

**Gaus mean : 38.2225**

**Gaus Width: 3.3307**



# B1L101S, U11-ch123, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	72
Mean	44.93
Std Dev	3.497

**Gaus mean : 45.8243**

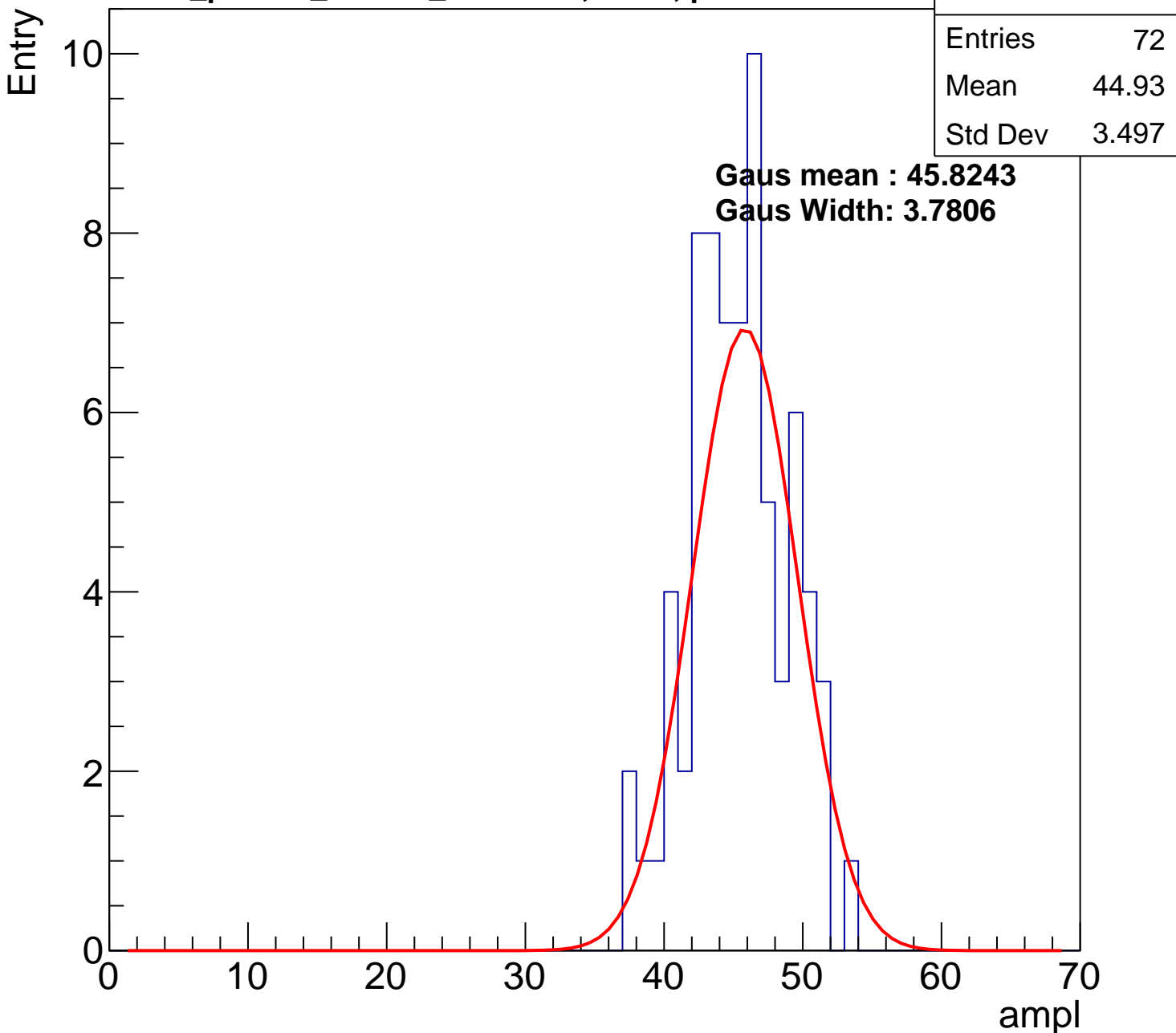
**Gaus Width: 3.7806**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

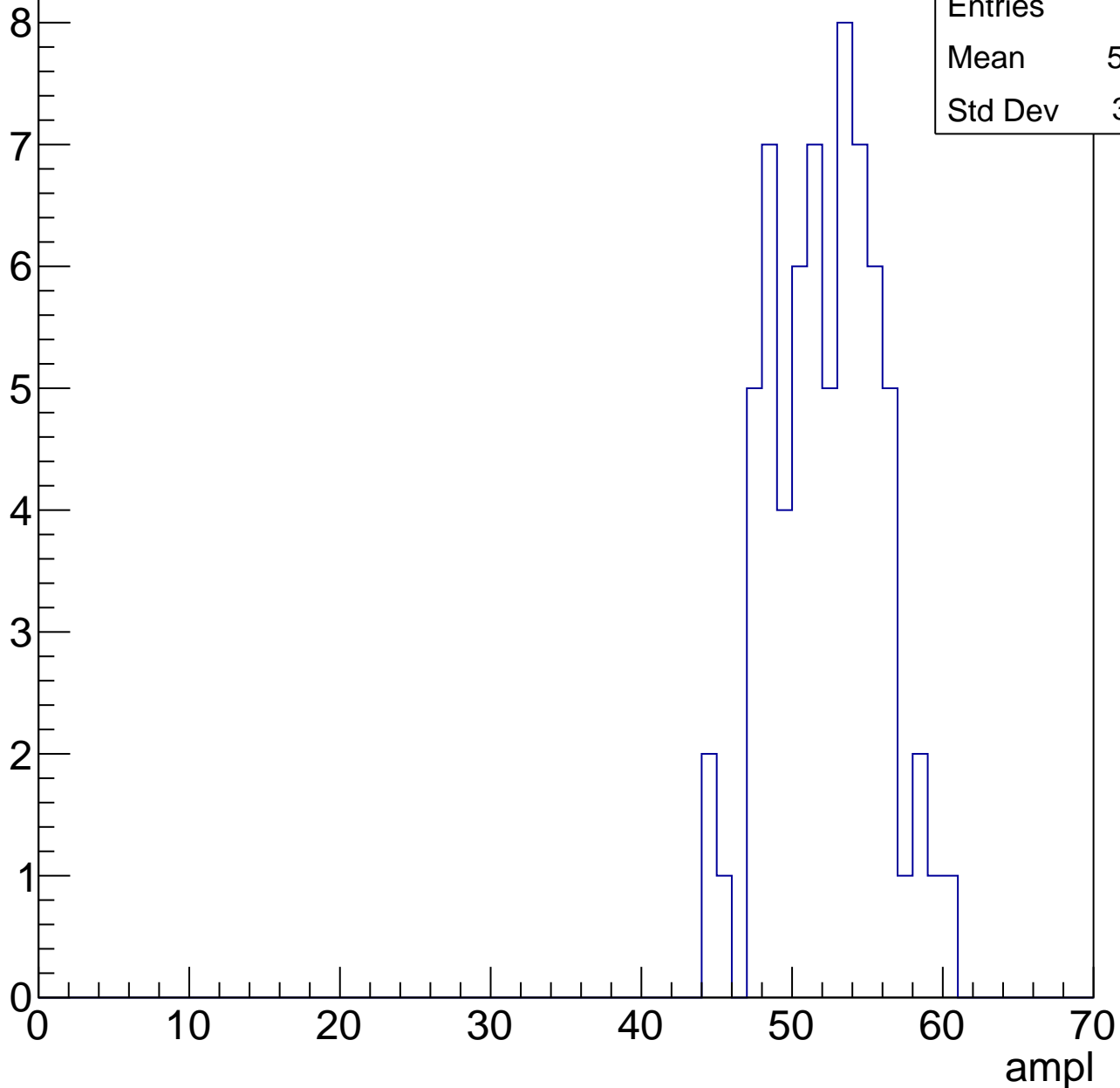


# B1L101S, U11-ch123, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	51.78
Std Dev	3.551

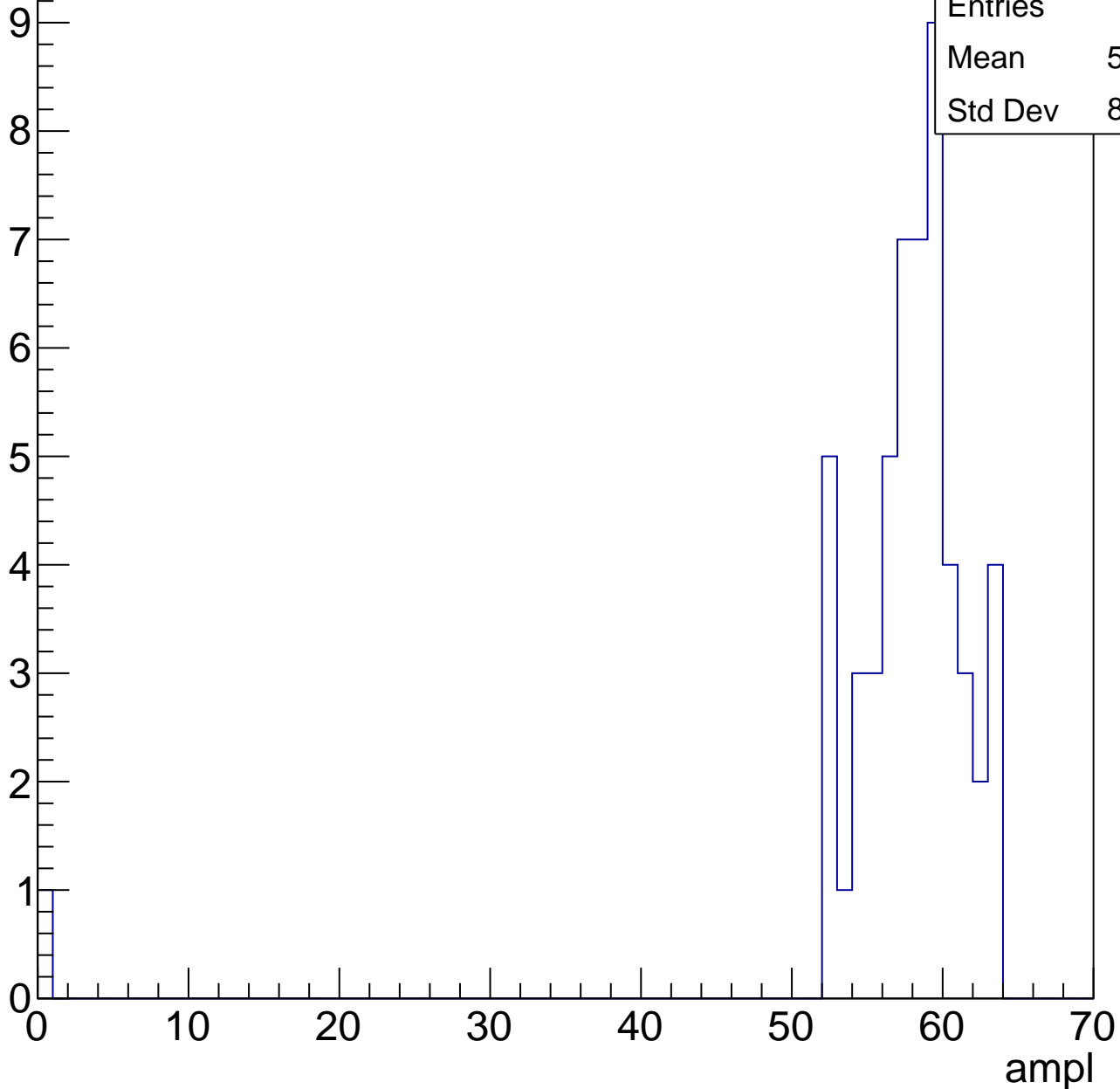


# B1L101S, U11-ch123, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	56.57
Std Dev	8.328

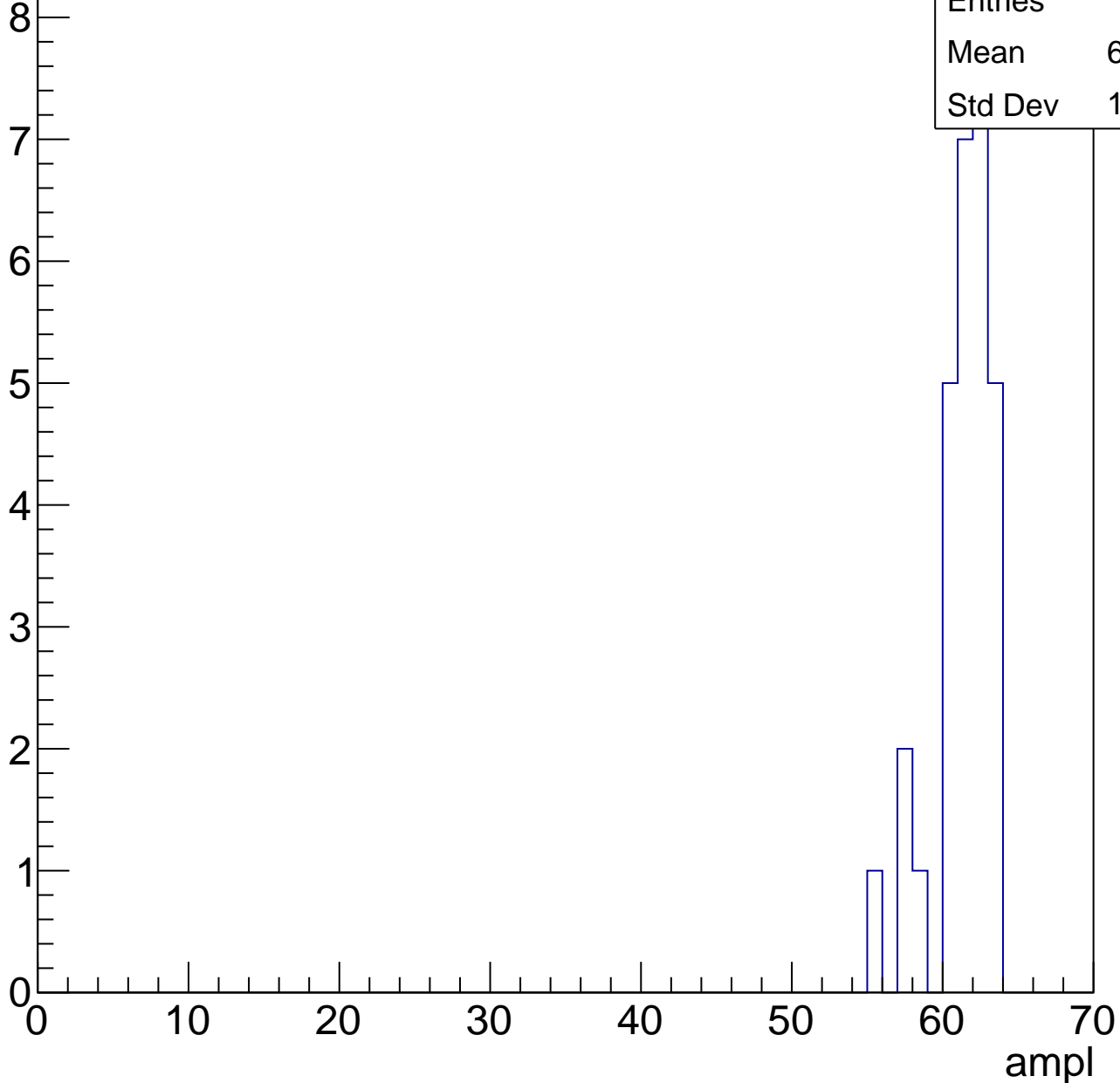


# B1L101S, U11-ch123, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	29
Mean	60.86
Std Dev	1.943



# B1L101S, U11-ch123, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	63
Std Dev	0



# B1L101S, U11-ch123, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U11-ch124, adc0

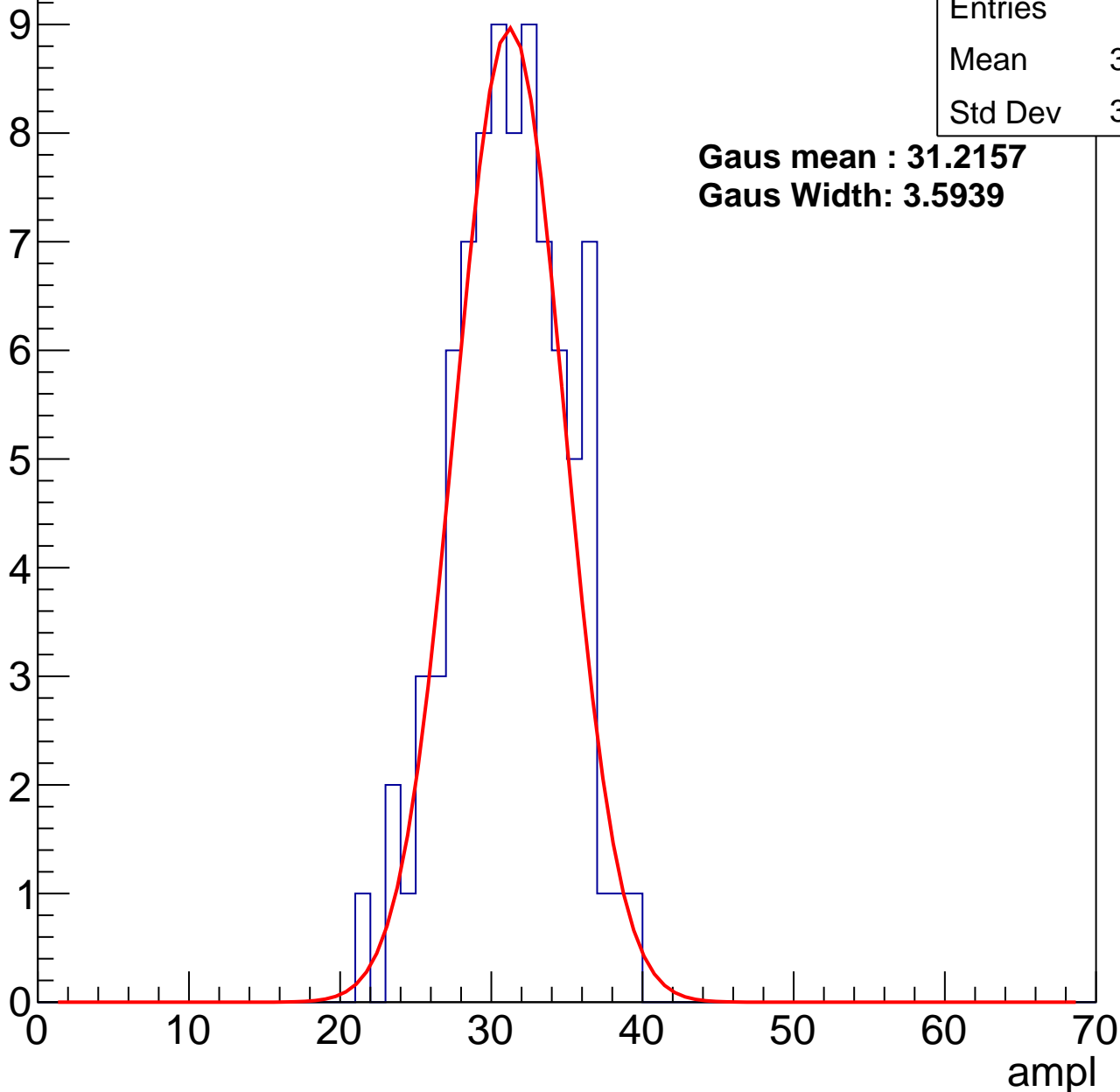
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	85
Mean	30.78
Std Dev	3.679

**Gaus mean : 31.2157**

**Gaus Width: 3.5939**



# B1L101S, U11-ch124, adc1

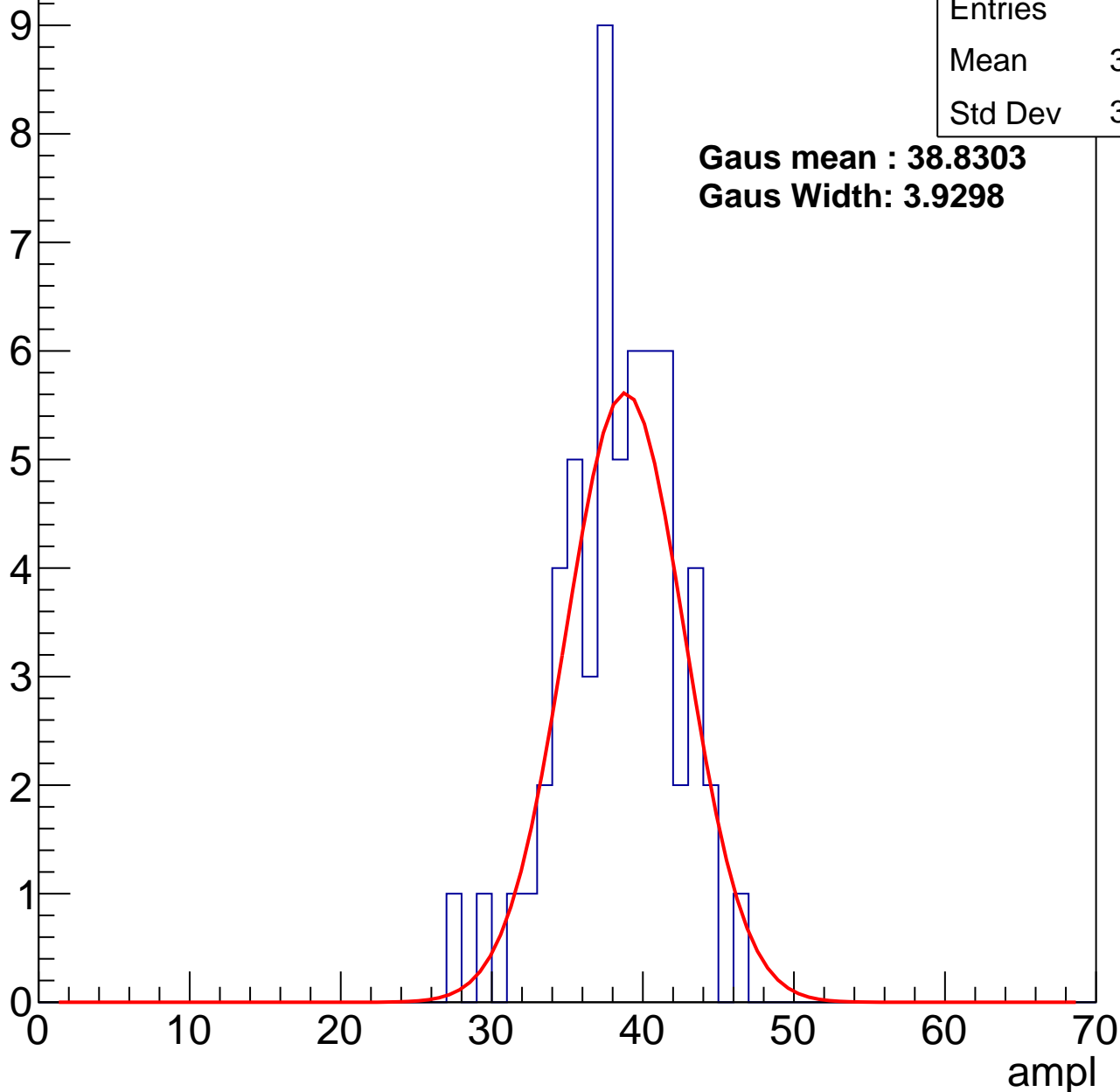
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	37.92
Std Dev	3.725

**Gaus mean : 38.8303**

**Gaus Width: 3.9298**



# B1L101S, U11-ch124, adc2

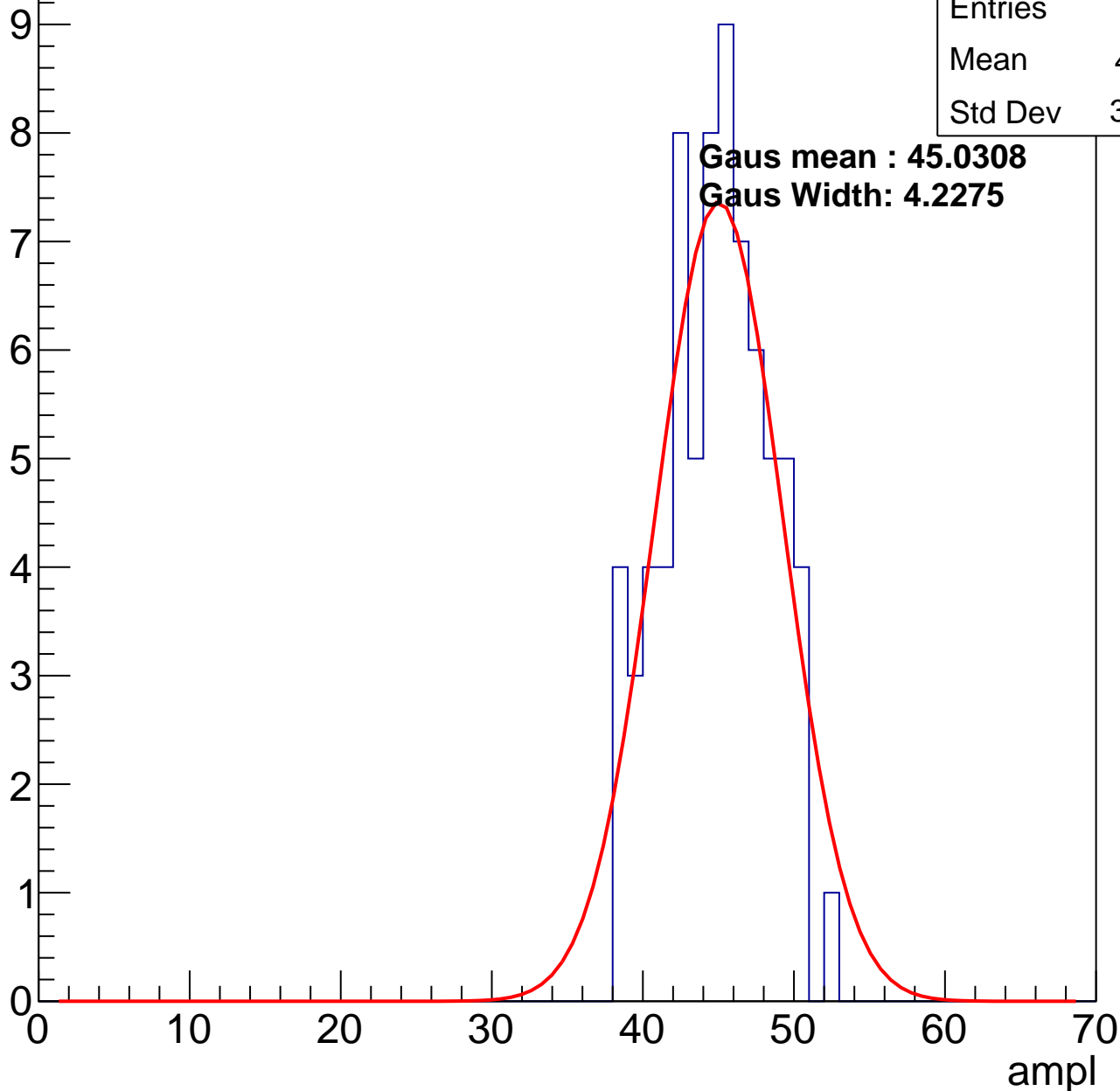
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	44.41
Std Dev	3.408

**Gaus mean : 45.0308**

**Gaus Width: 4.2275**



# B1L101S, U11-ch124, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

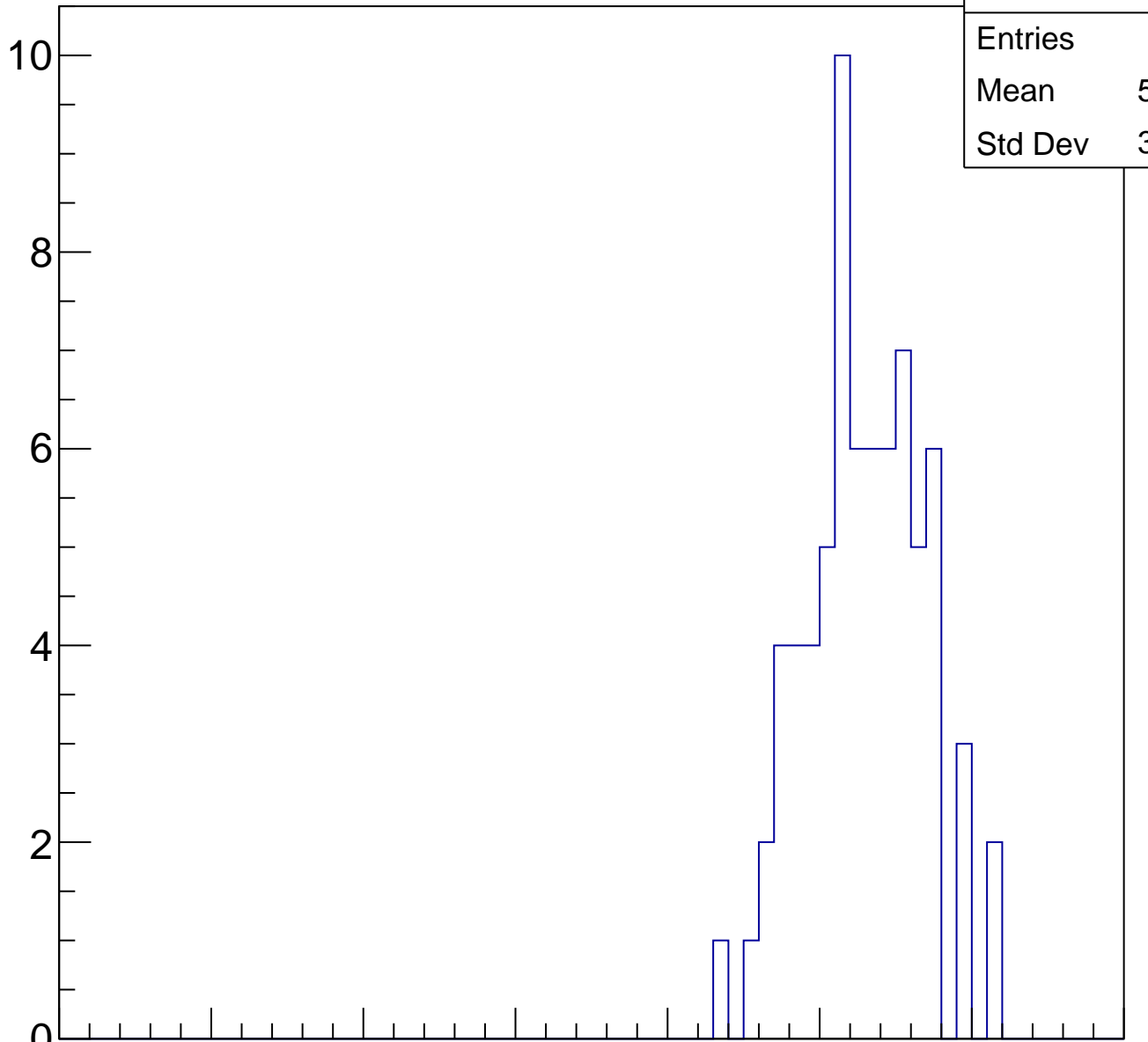
Entries	72
Mean	52.44
Std Dev	3.818

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

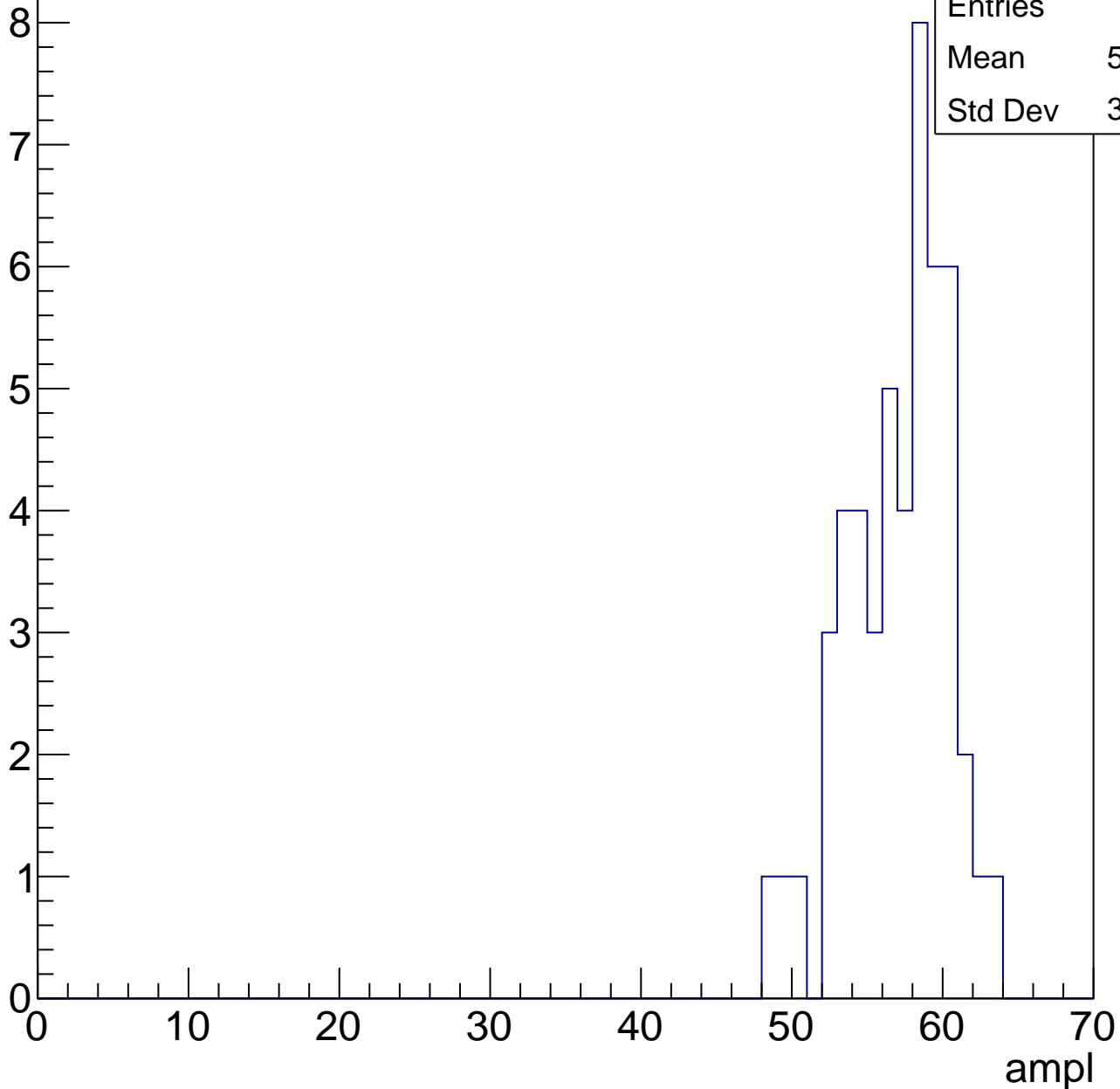


# B1L101S, U11-ch124, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	56.58
Std Dev	3.335

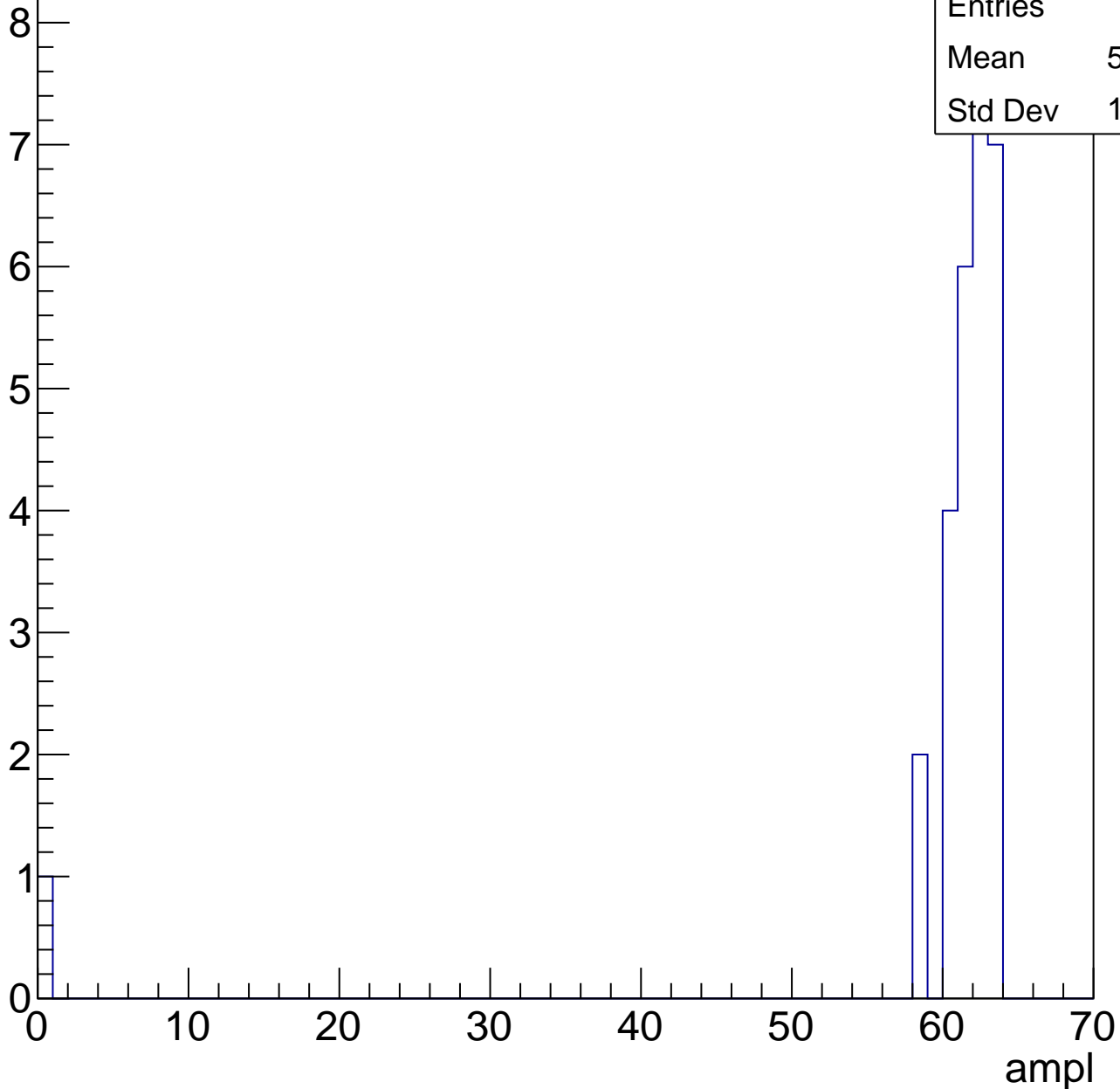


# B1L101S, U11-ch124, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

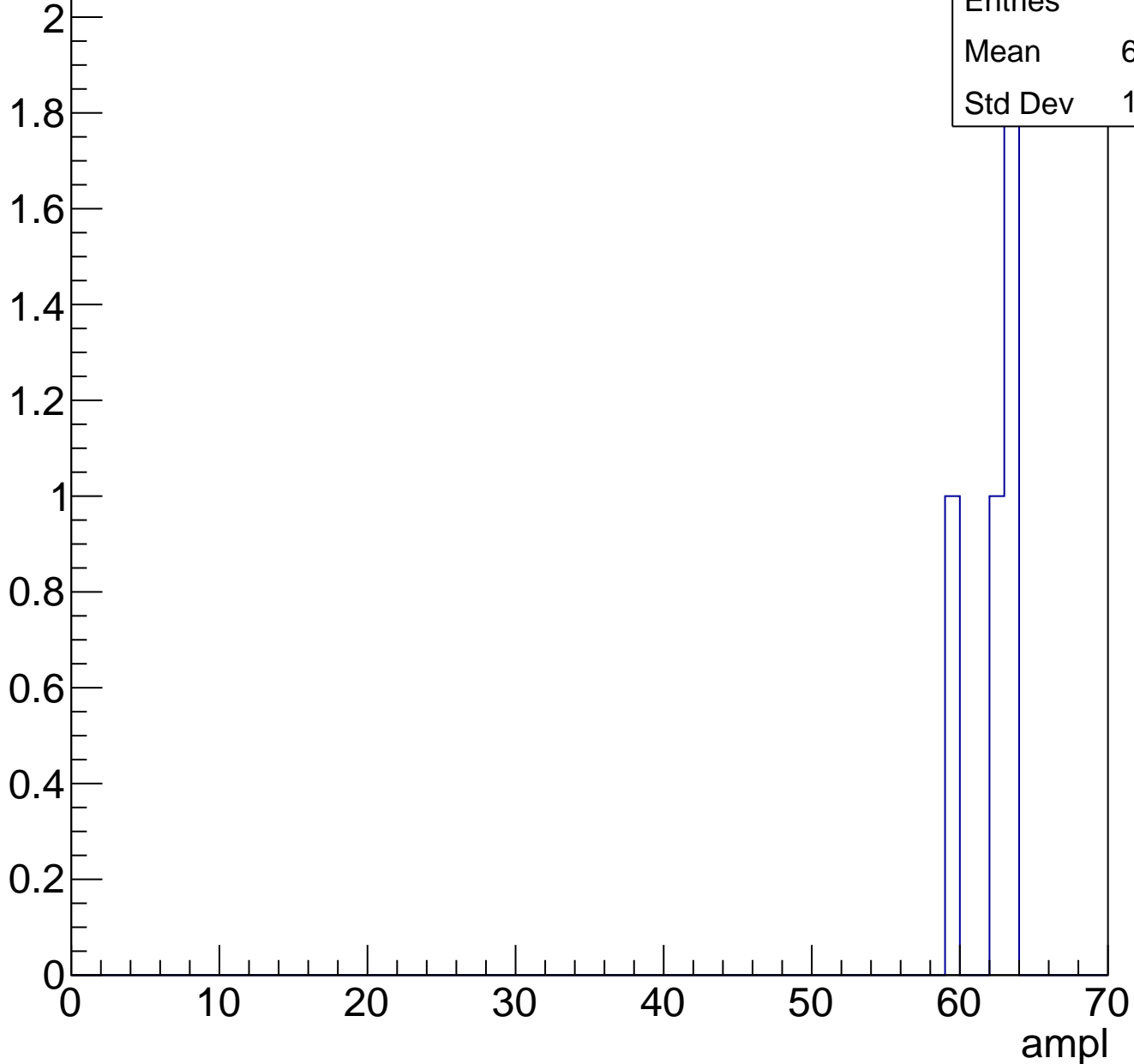
Entries	28
Mean	59.25
Std Dev	11.48



# B1L101S, U11-ch124, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

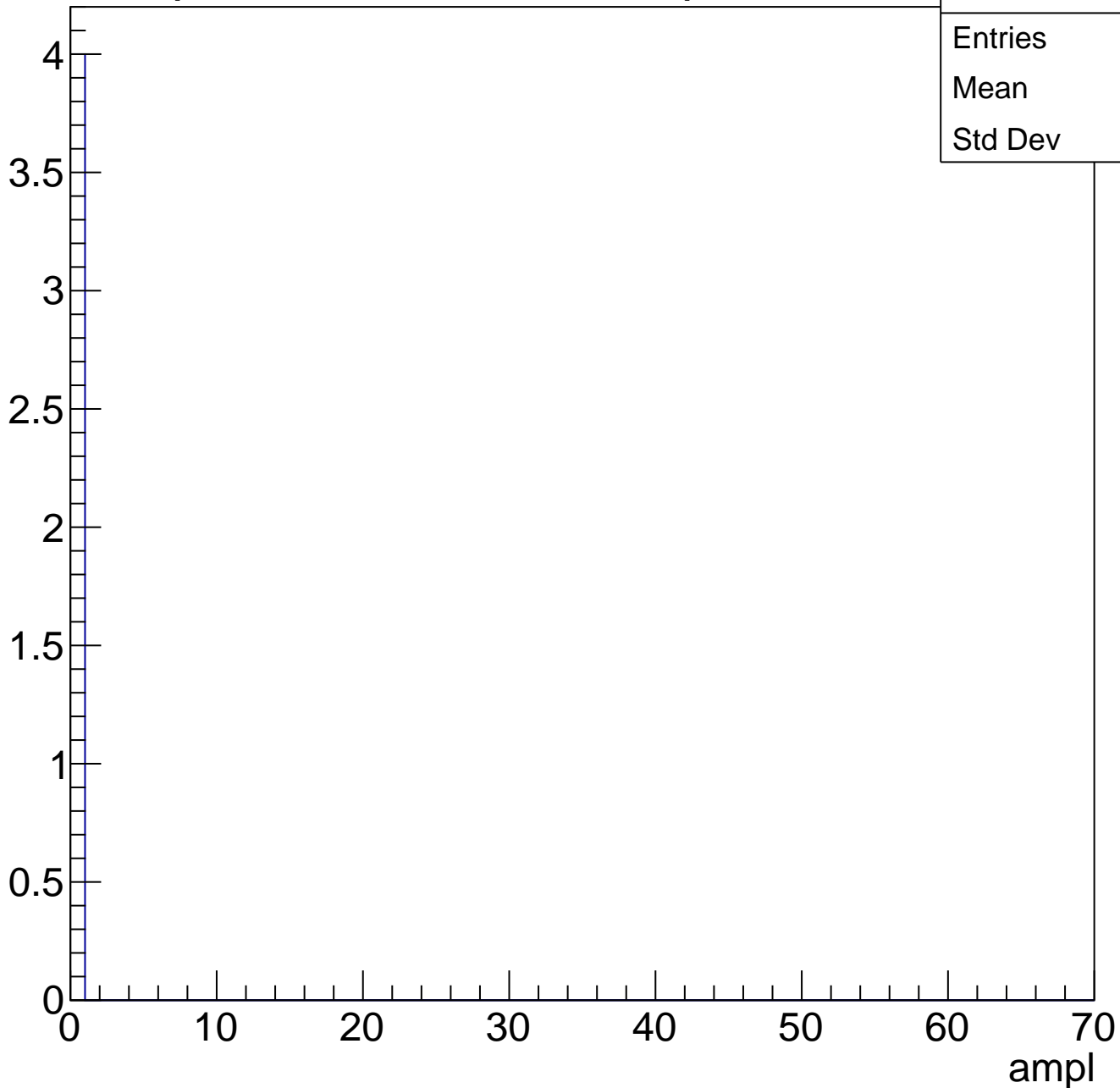




# B1L101S, U11-ch124, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	4
Mean	0
Std Dev	0

# B1L101S, U11-ch125, adc0

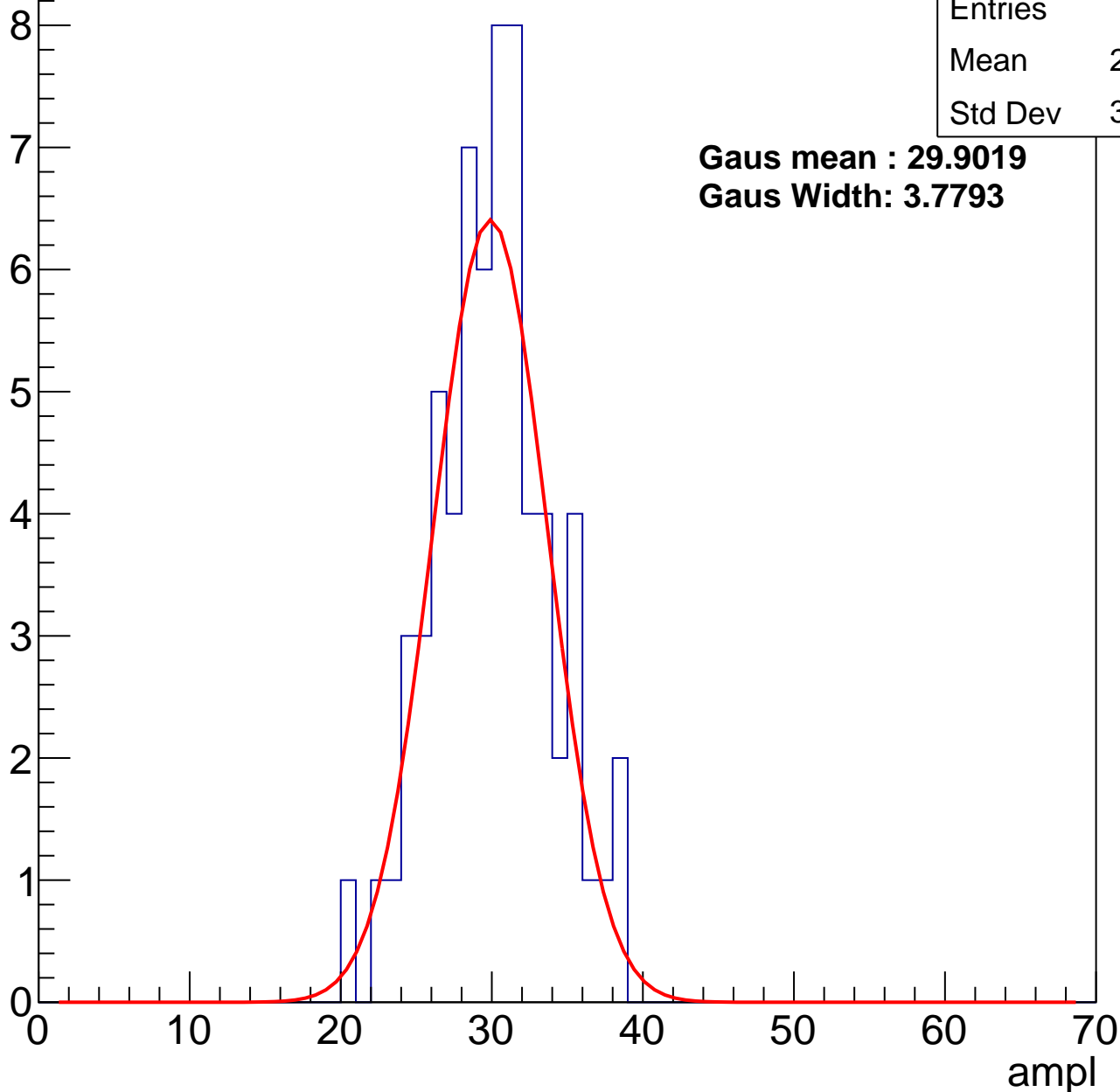
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	29.62
Std Dev	3.806

**Gaus mean : 29.9019**

**Gaus Width: 3.7793**



# B1L101S, U11-ch125, adc1

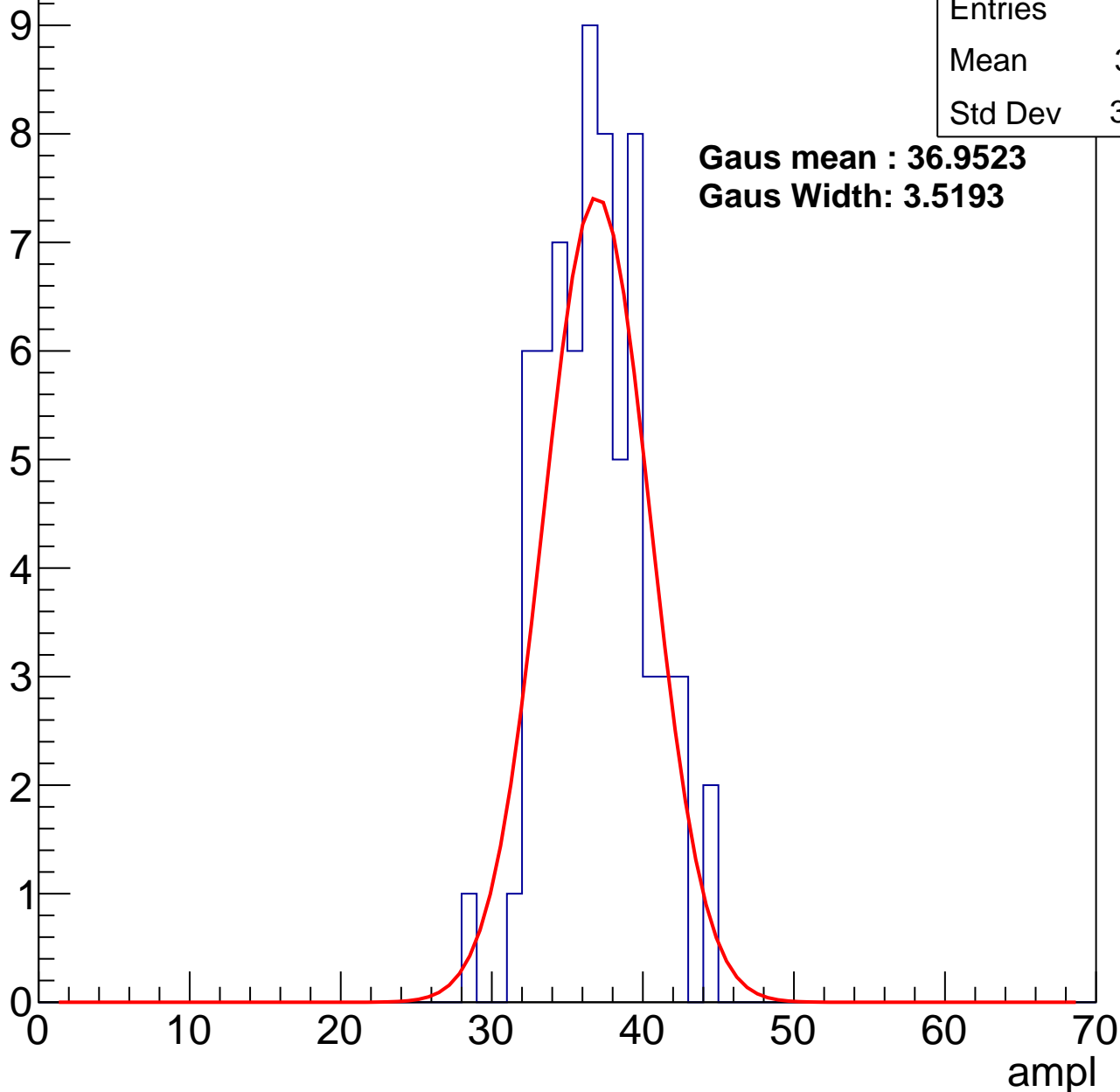
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	36.41
Std Dev	3.255

**Gaus mean : 36.9523**

**Gaus Width: 3.5193**



# B1L101S, U11-ch125, adc2

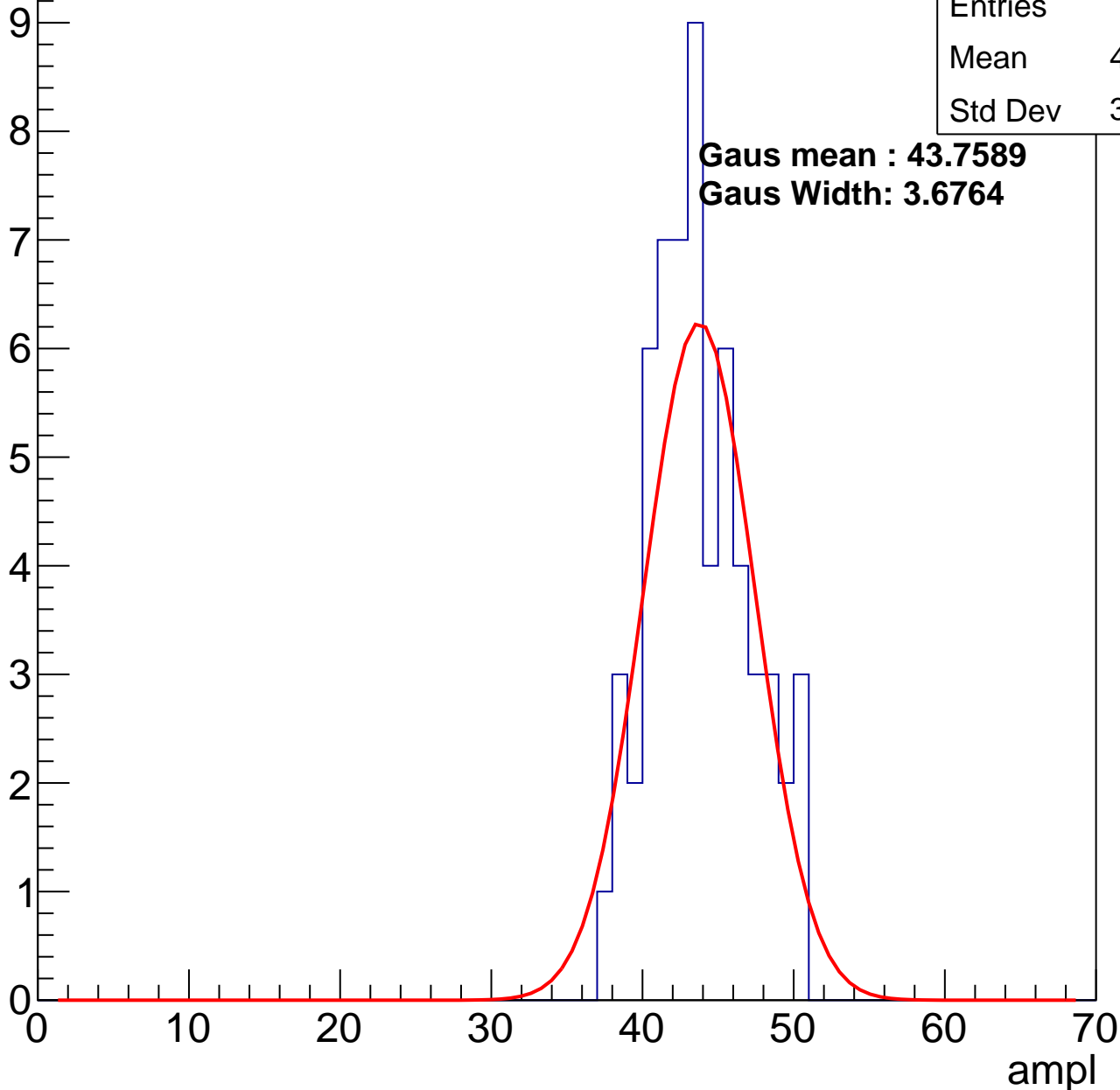
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	43.33
Std Dev	3.244

**Gaus mean : 43.7589**

**Gaus Width: 3.6764**

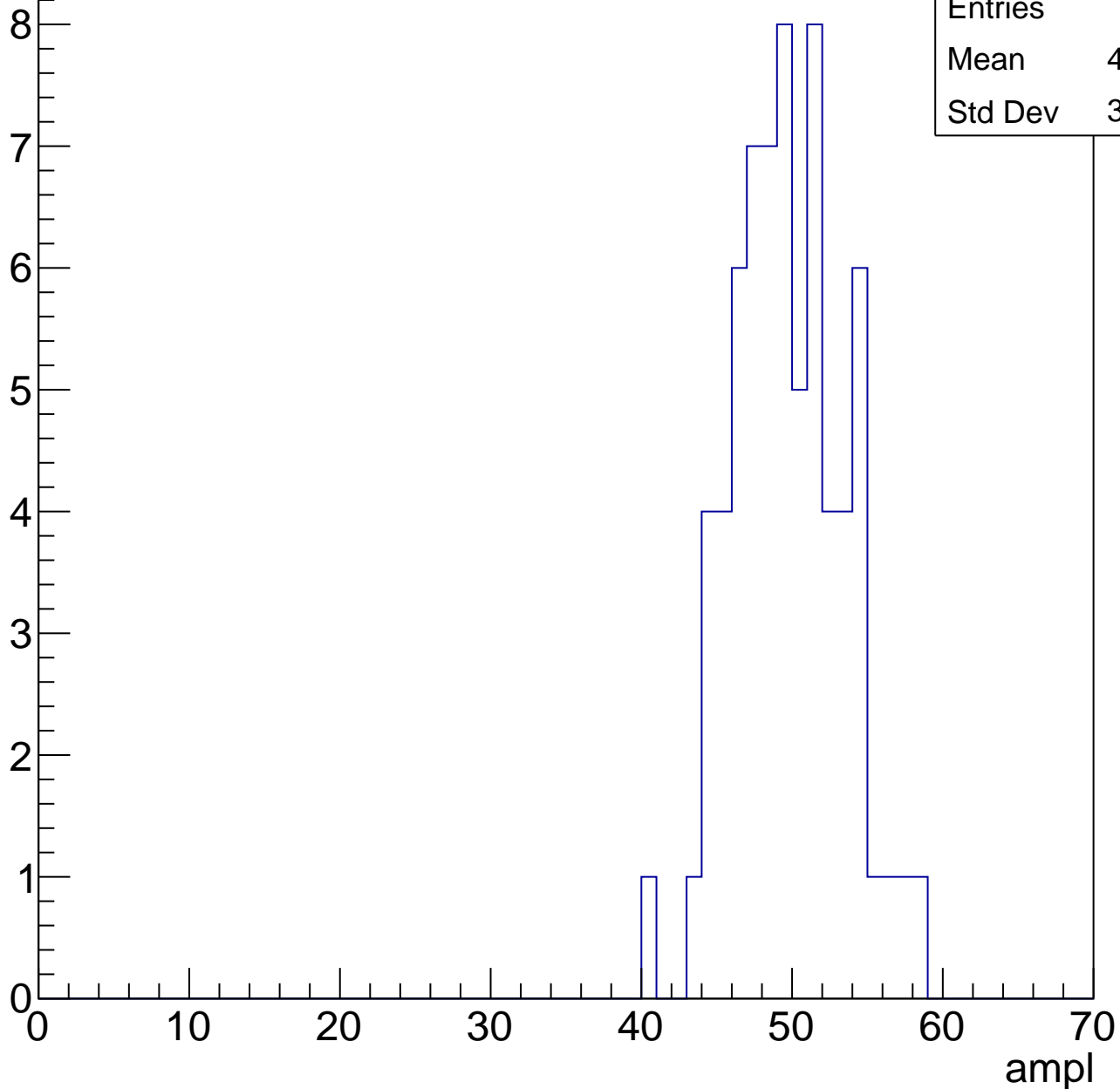


# B1L101S, U11-ch125, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	49.28
Std Dev	3.575

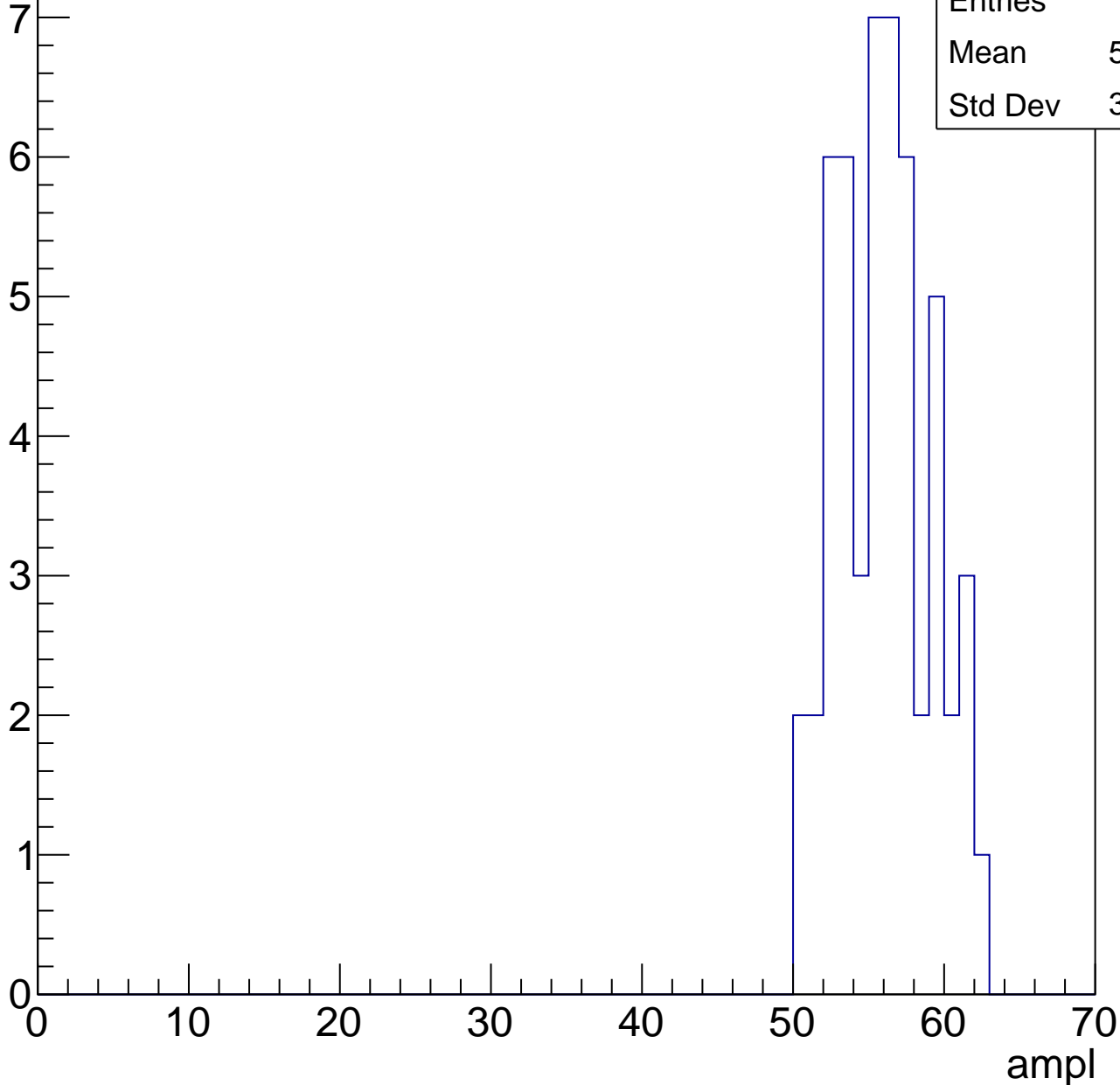


# B1L101S, U11-ch125, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	55.56
Std Dev	3.047

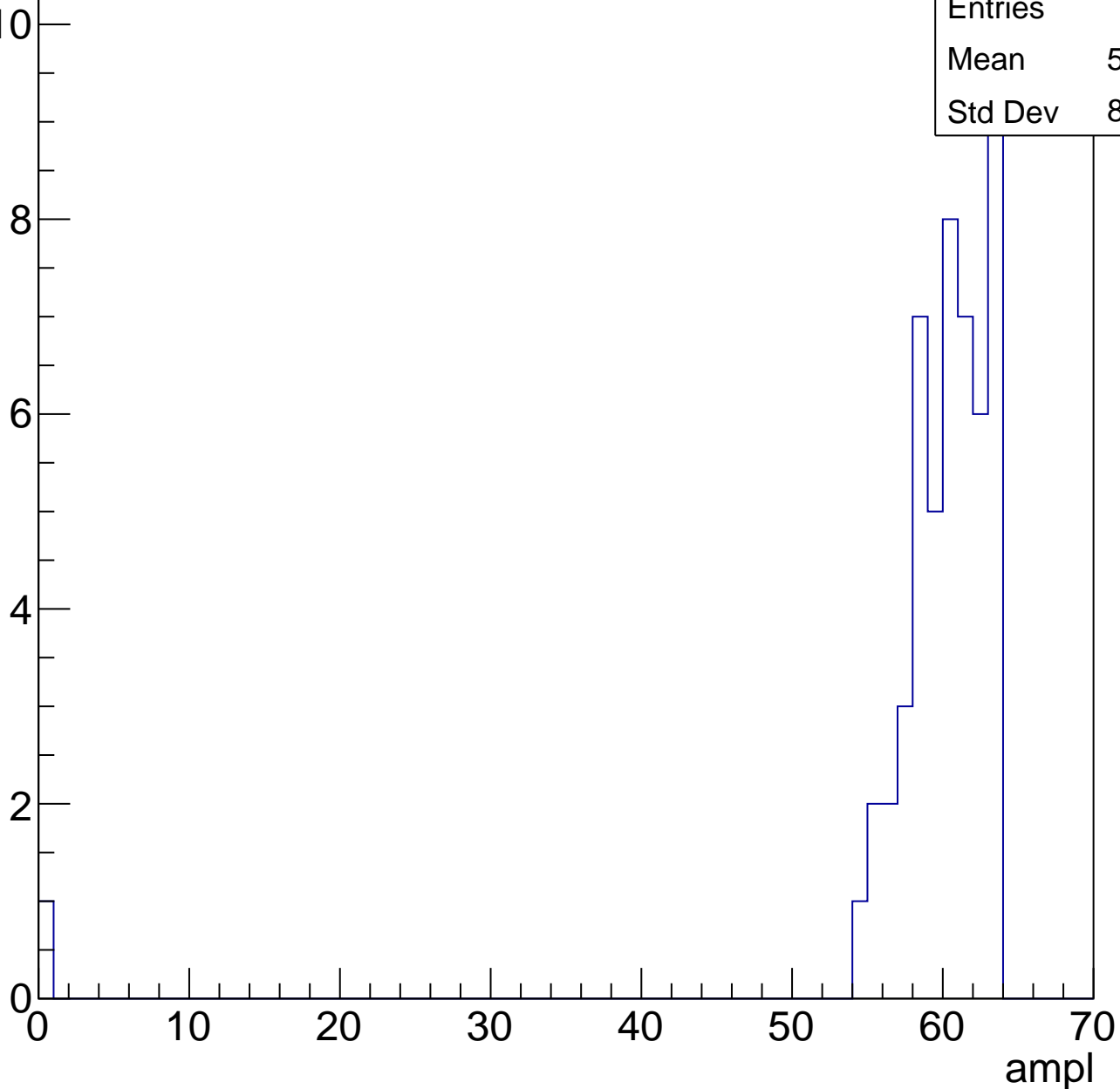


# B1L101S, U11-ch125, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

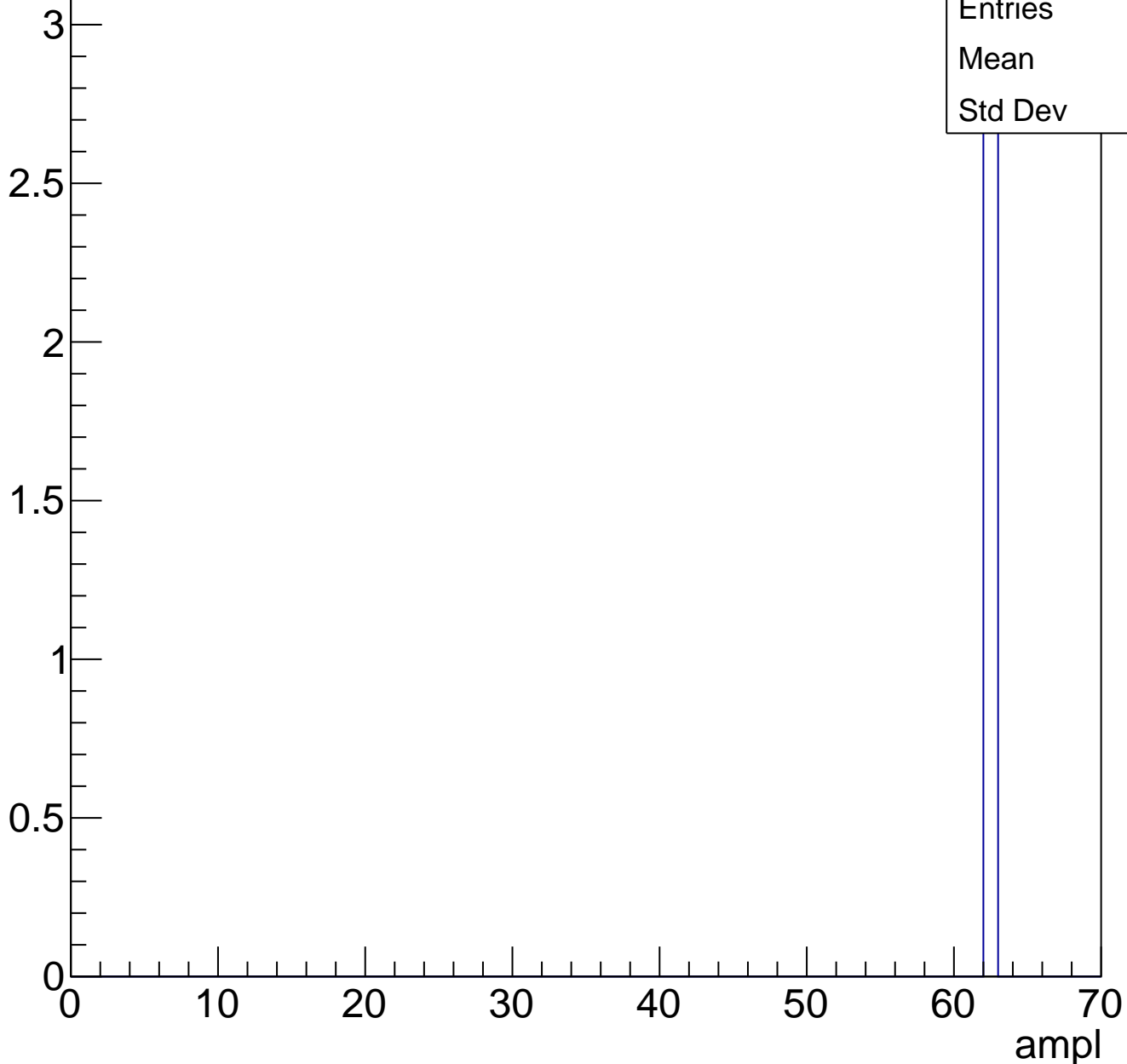
Entries	52
Mean	58.79
Std Dev	8.574



# B1L101S, U11-ch125, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U11-ch125, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U11-ch126, adc0

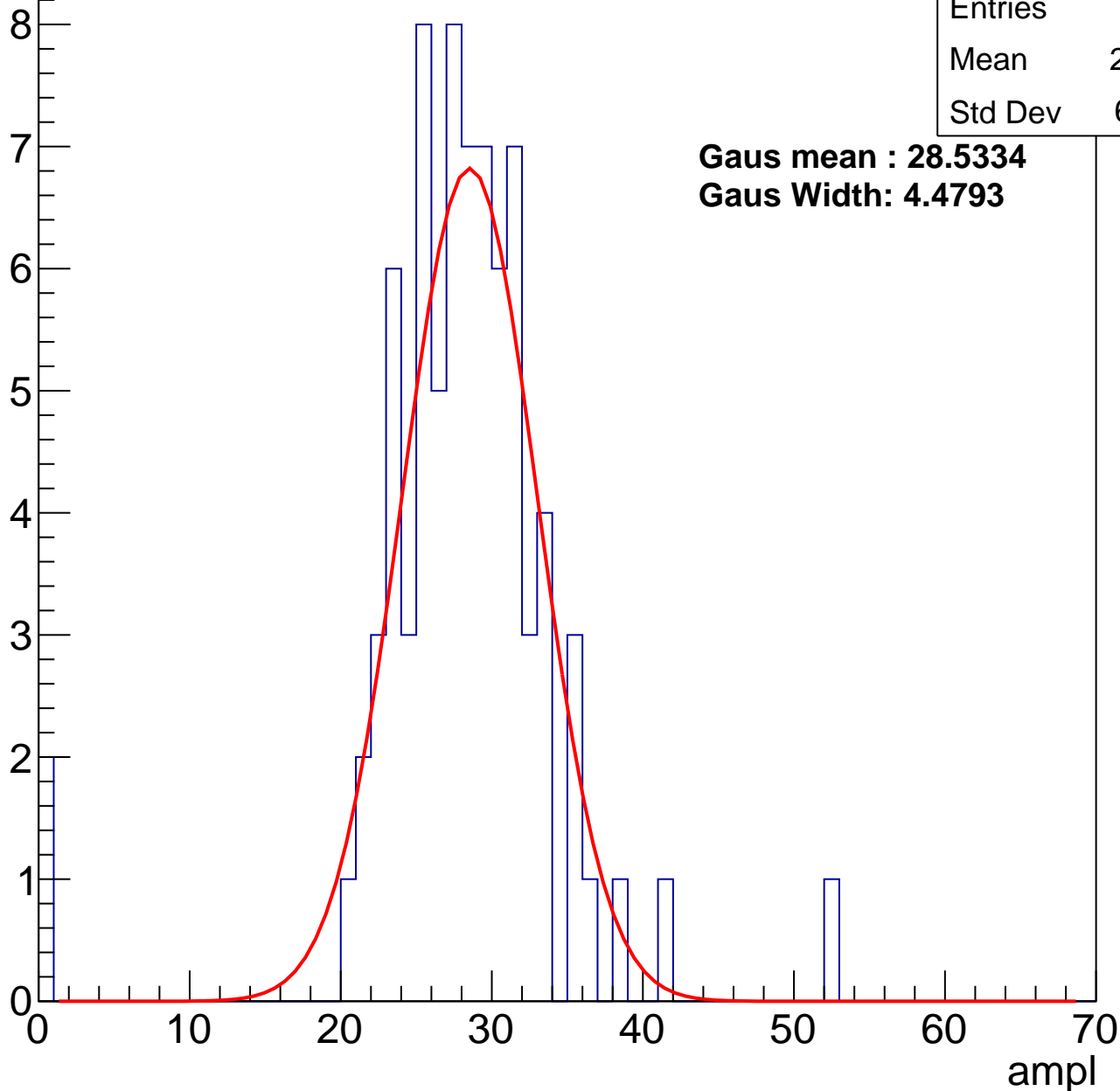
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	79
Mean	27.59
Std Dev	6.581

**Gaus mean : 28.5334**

**Gaus Width: 4.4793**



# B1L101S, U11-ch126, adc1

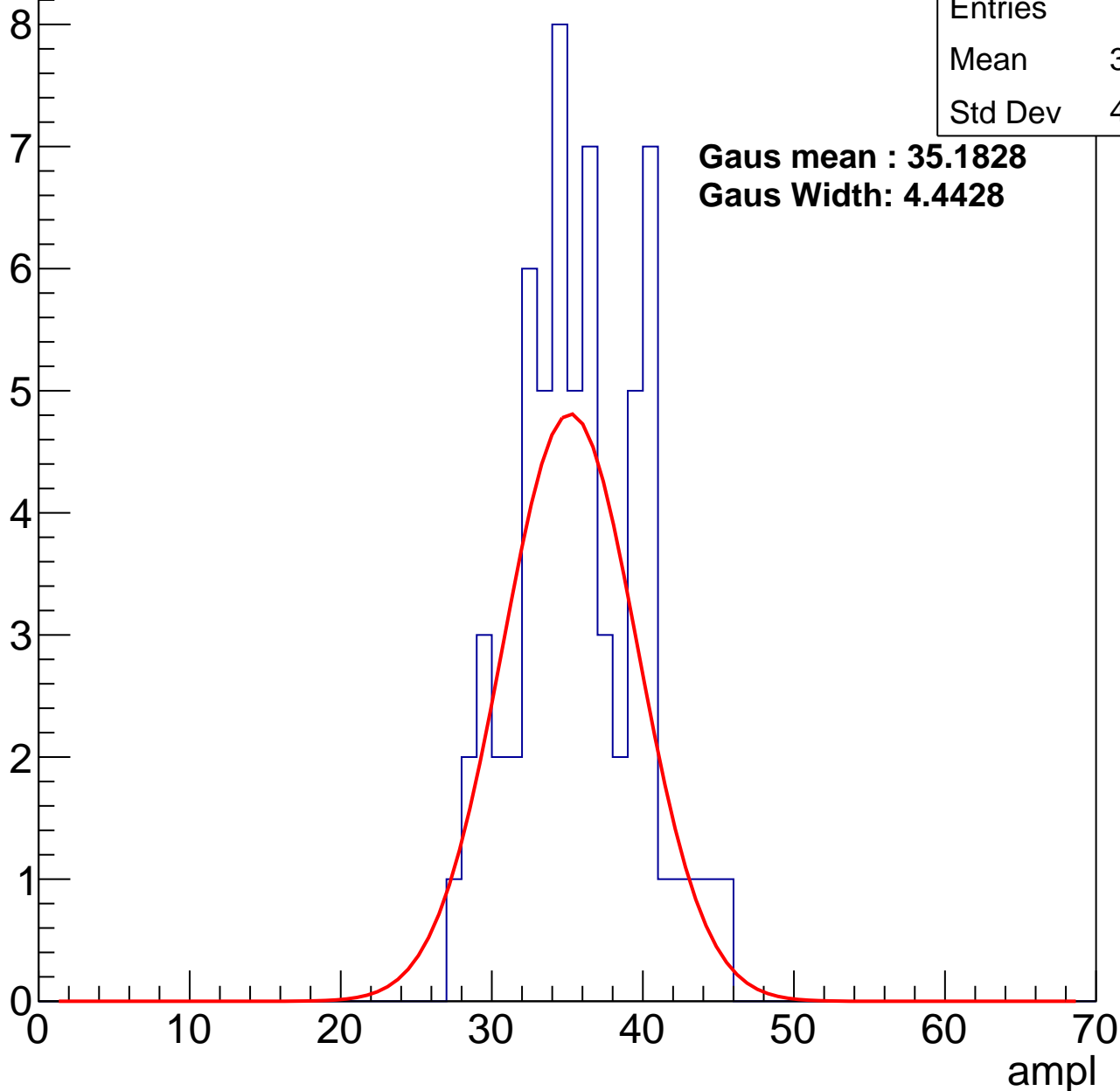
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	35.32
Std Dev	4.082

**Gaus mean : 35.1828**

**Gaus Width: 4.4428**



# B1L101S, U11-ch126, adc2

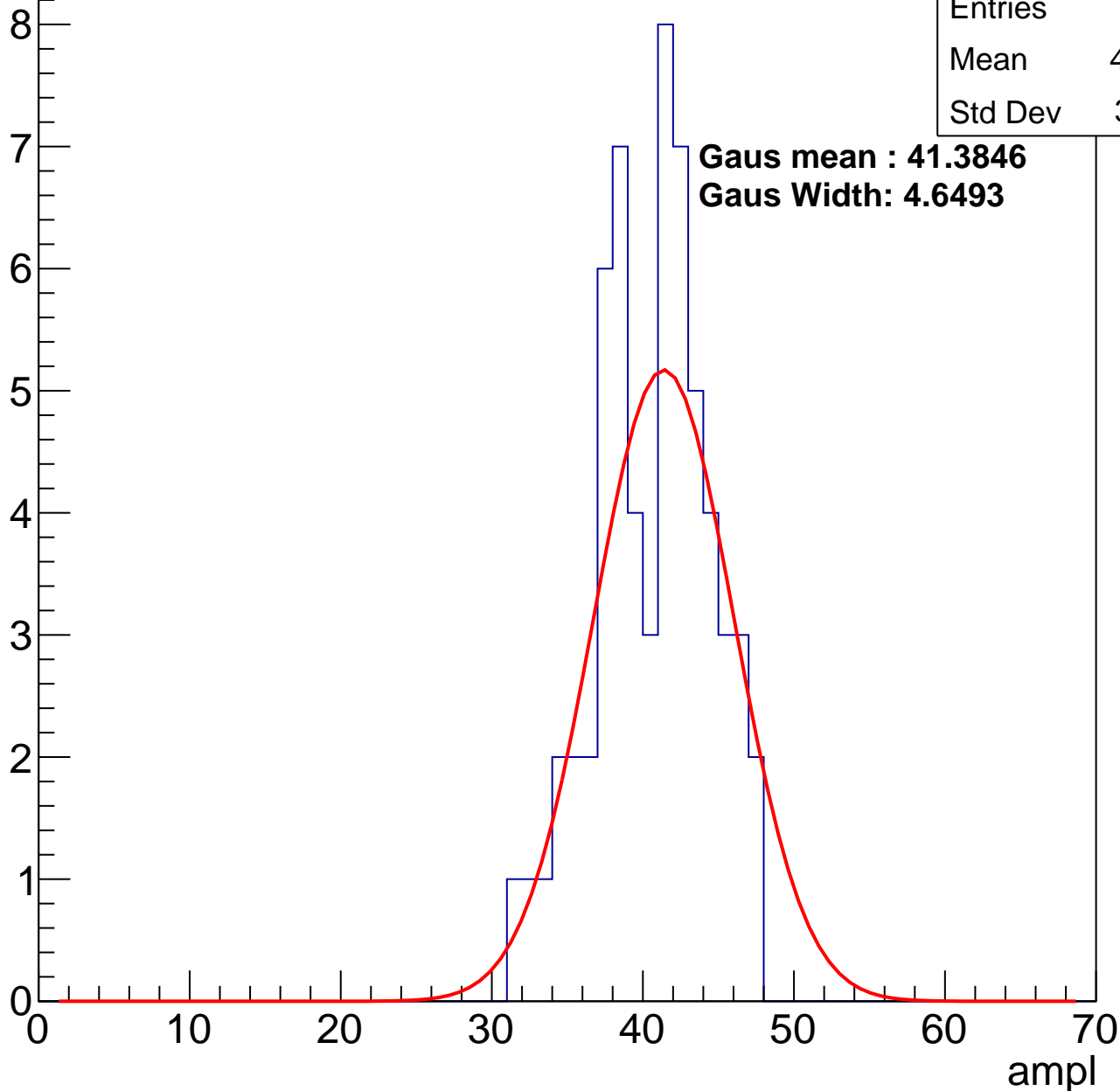
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	40.16
Std Dev	3.751

**Gaus mean : 41.3846**

**Gaus Width: 4.6493**

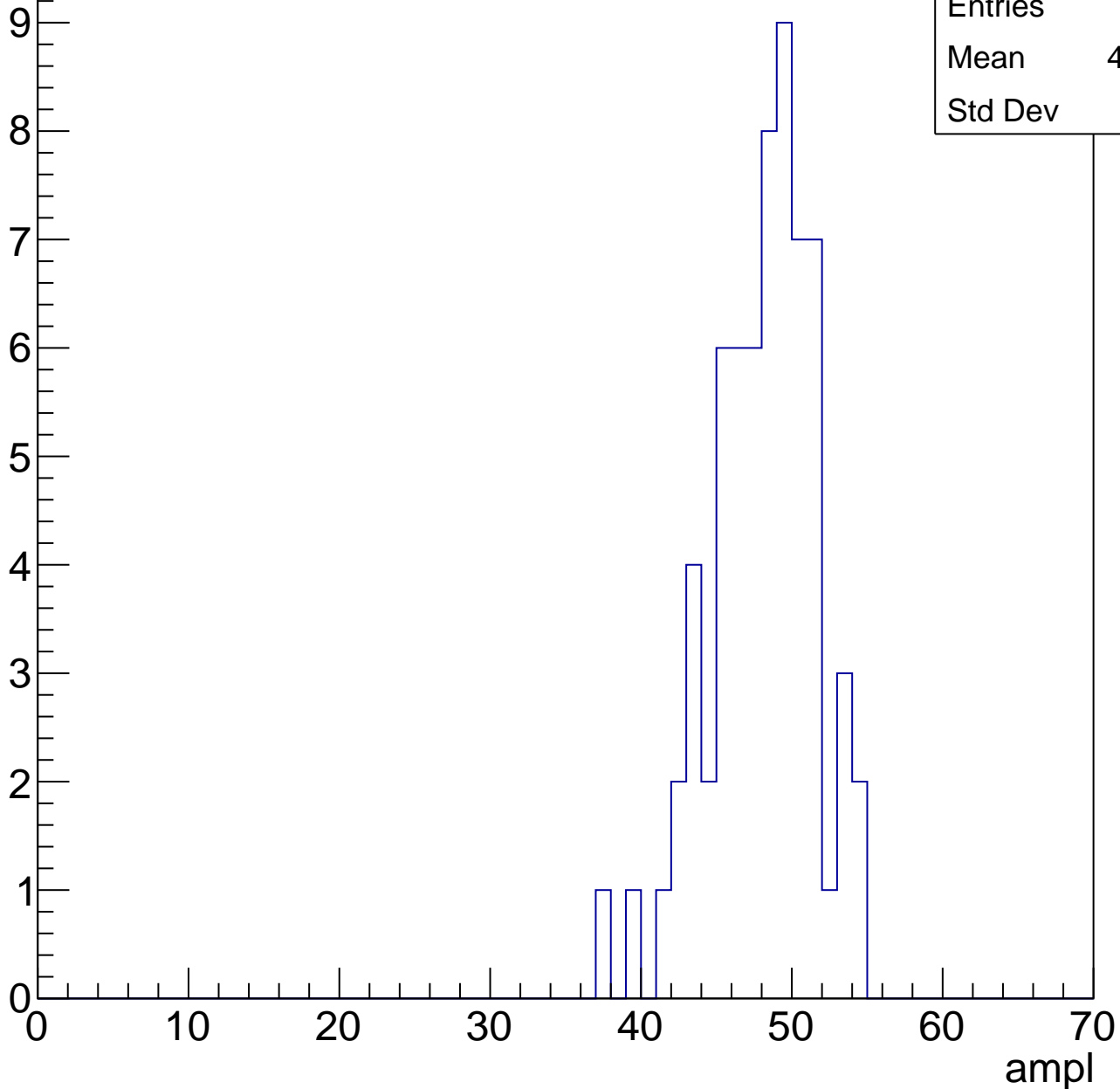


# B1L101S, U11-ch126, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	47.58
Std Dev	3.46

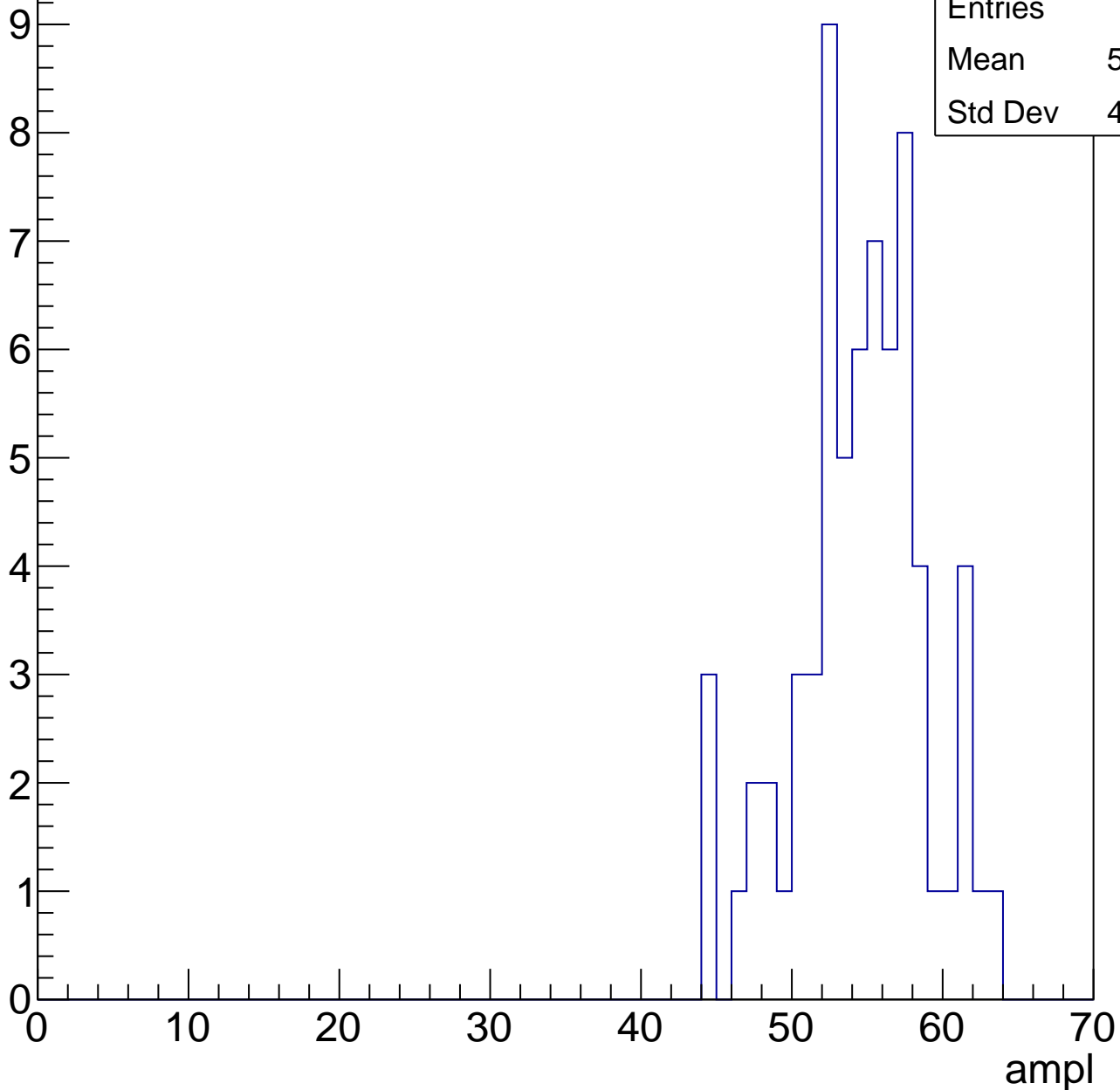


# B1L101S, U11-ch126, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

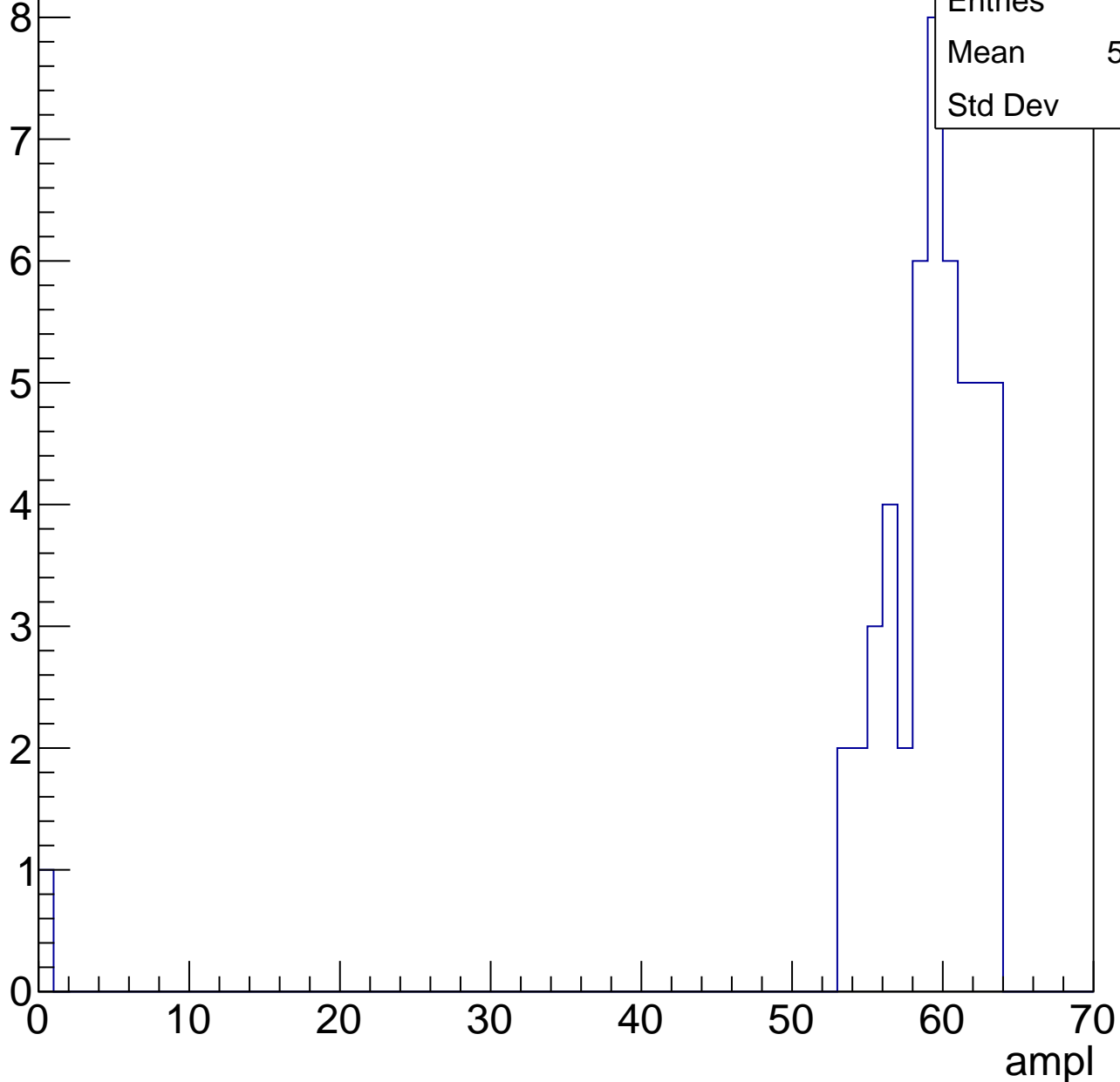
Entries	68
Mean	54.03
Std Dev	4.277



# B1L101S, U11-ch126, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

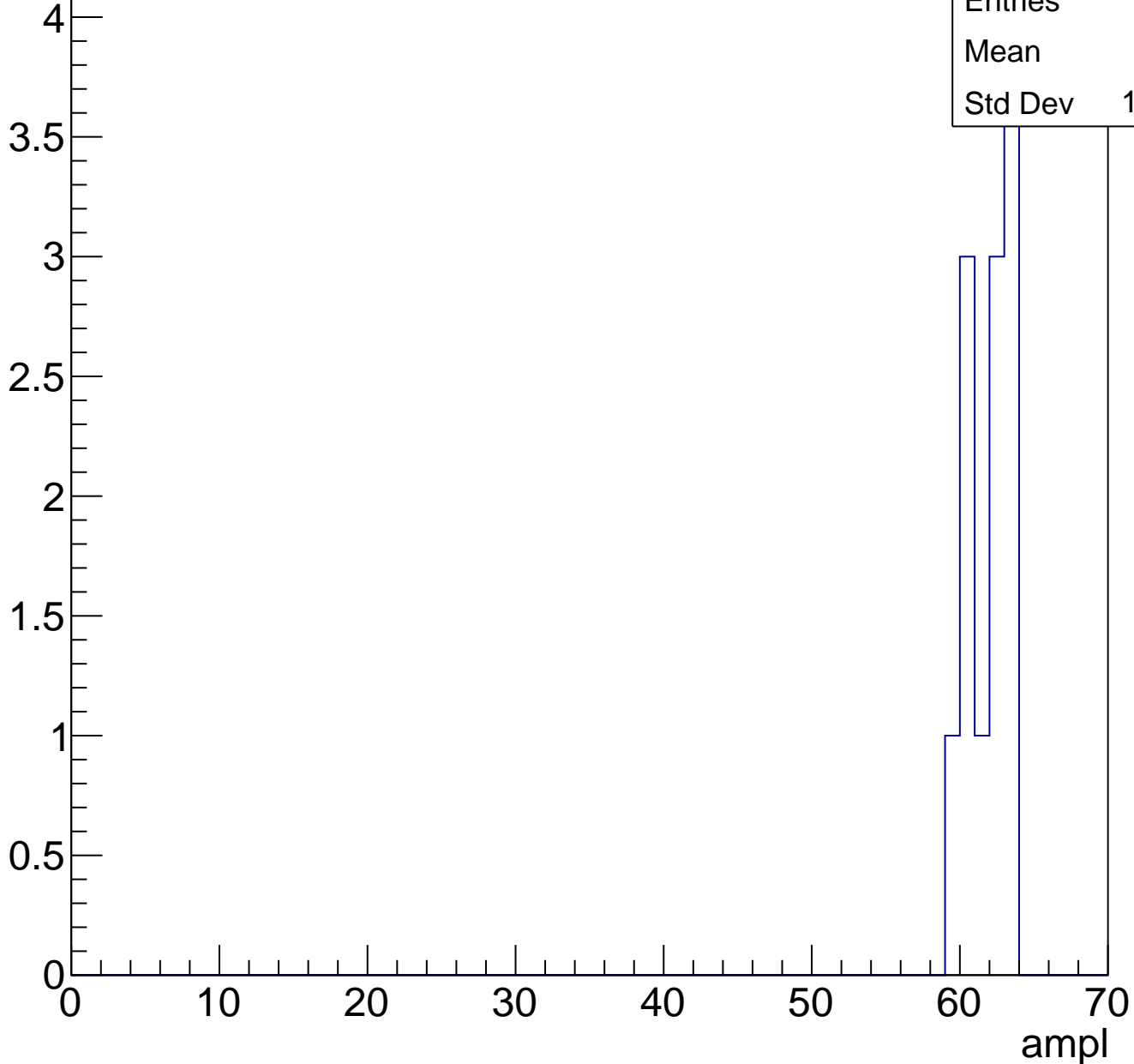
Entry



# B1L101S, U11-ch126, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	12
Mean	61.5
Std Dev	1.384



# B1L101S, U11-ch126, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U11-ch127, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	86
Mean	28.99
Std Dev	3.768

**Gaus mean : 29.4555**

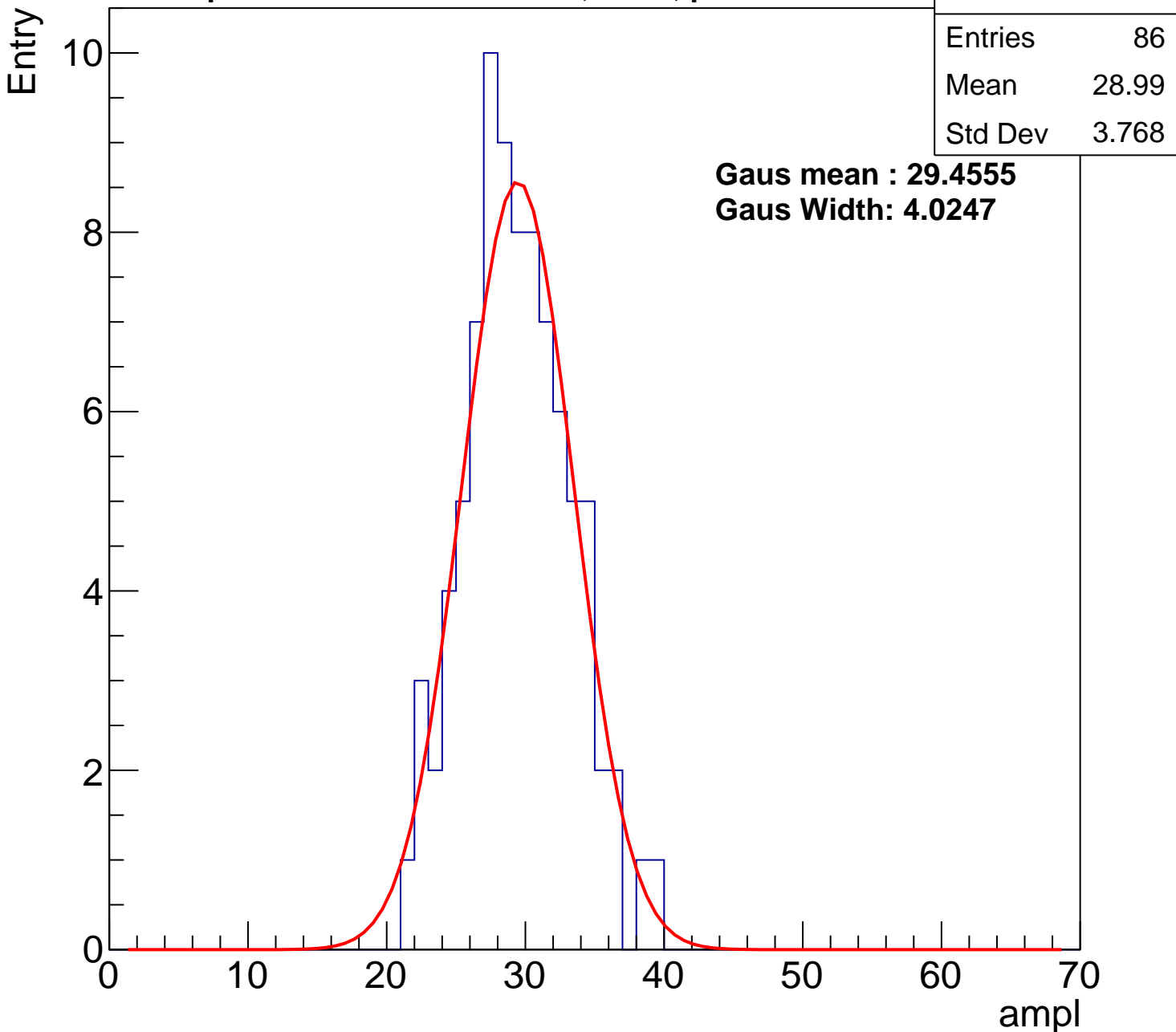
**Gaus Width: 4.0247**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U11-ch127, adc1

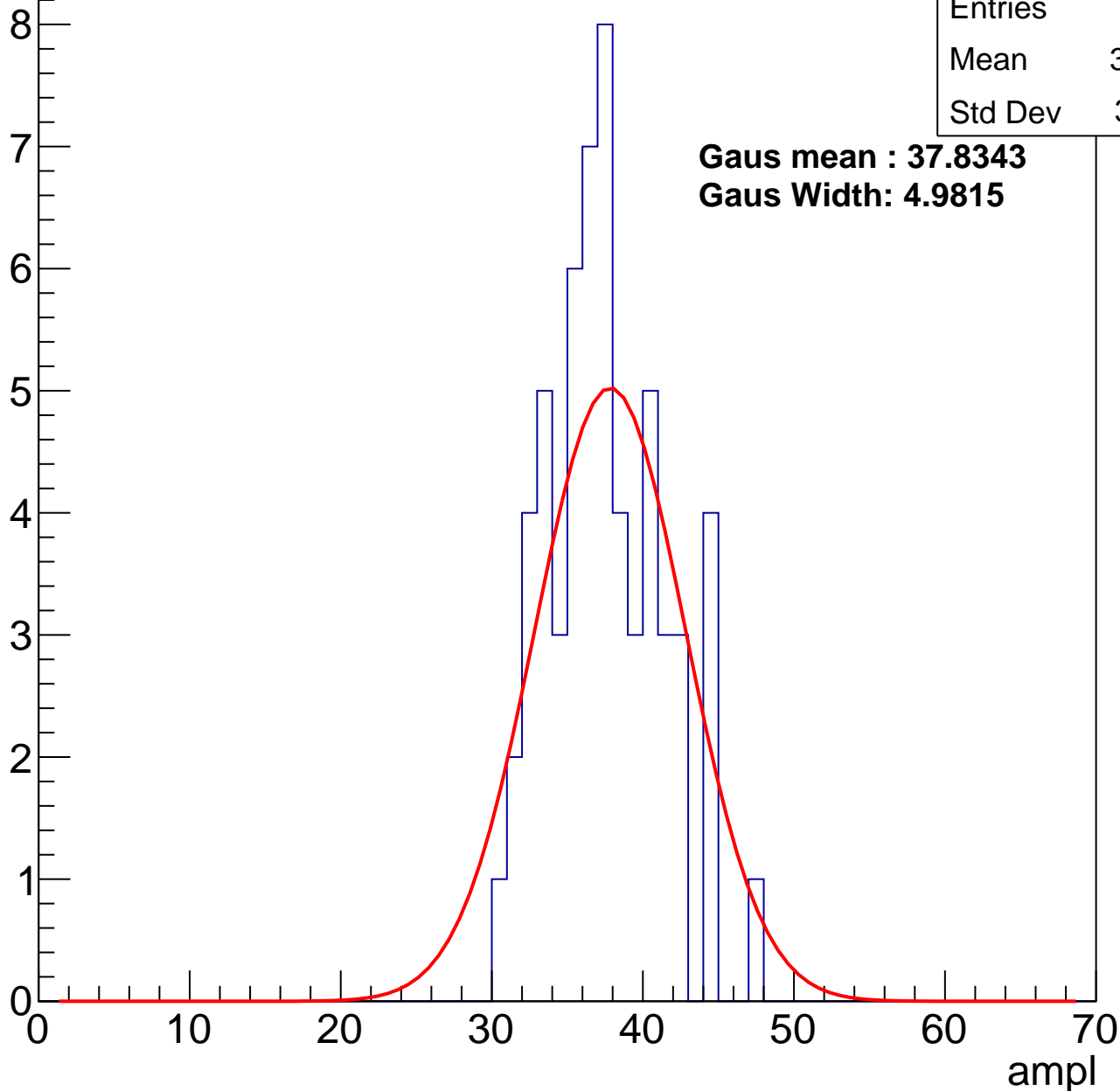
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	37.05
Std Dev	3.771

**Gaus mean : 37.8343**

**Gaus Width: 4.9815**



# B1L101S, U11-ch127, adc2

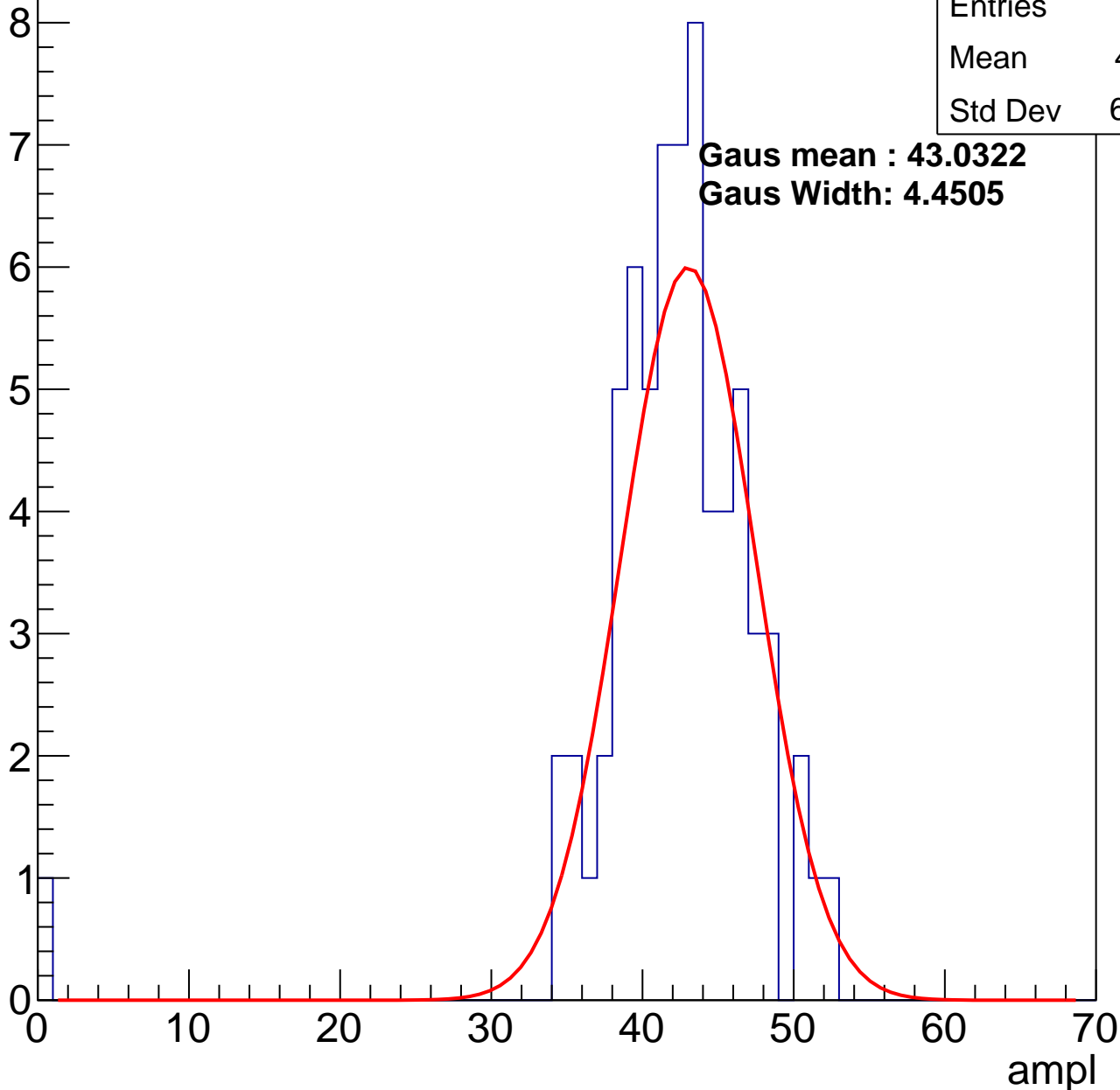
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	41.61
Std Dev	6.436

**Gaus mean : 43.0322**

**Gaus Width: 4.4505**

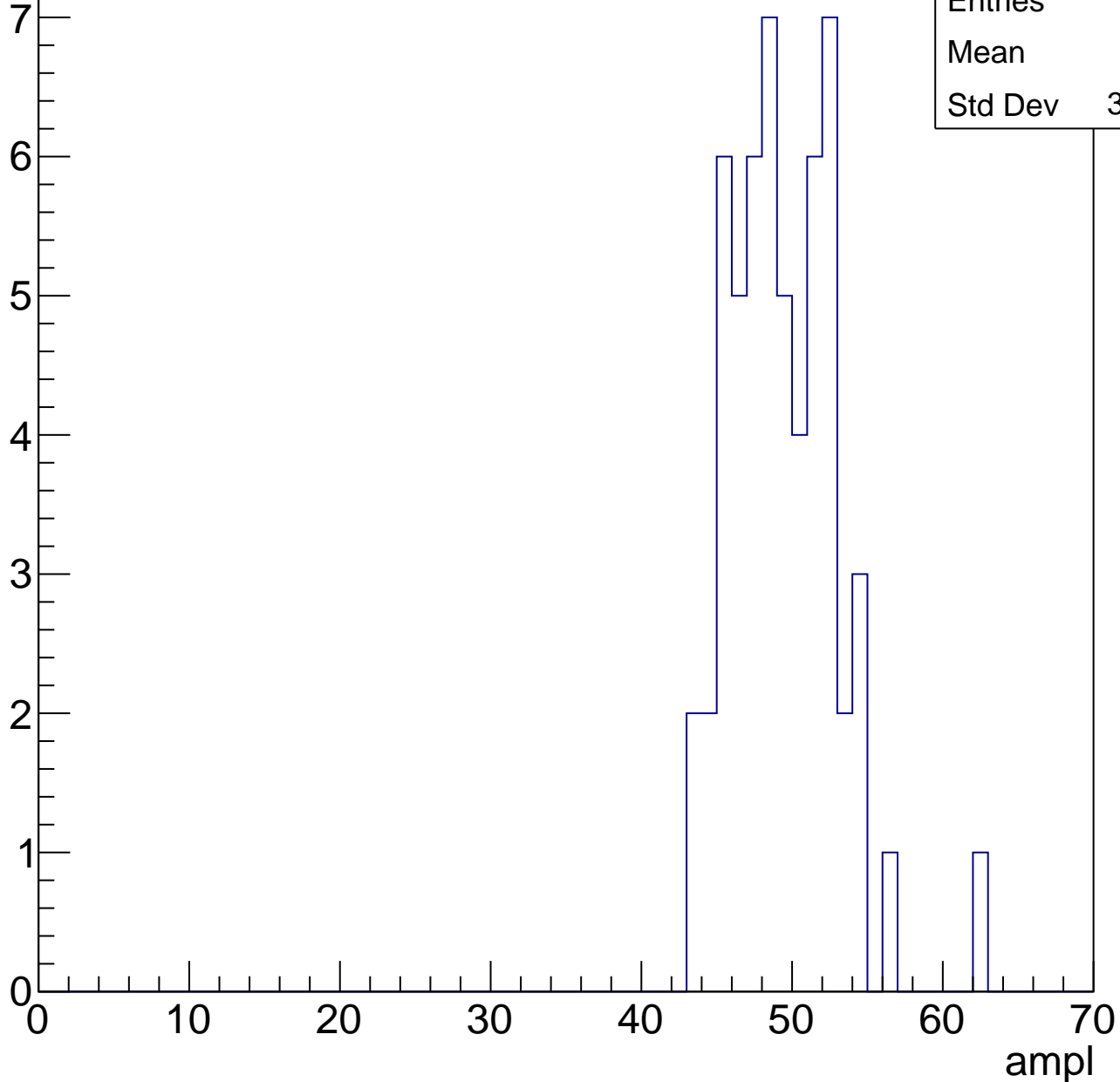


# B1L101S, U11-ch127, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	49
Std Dev	3.529

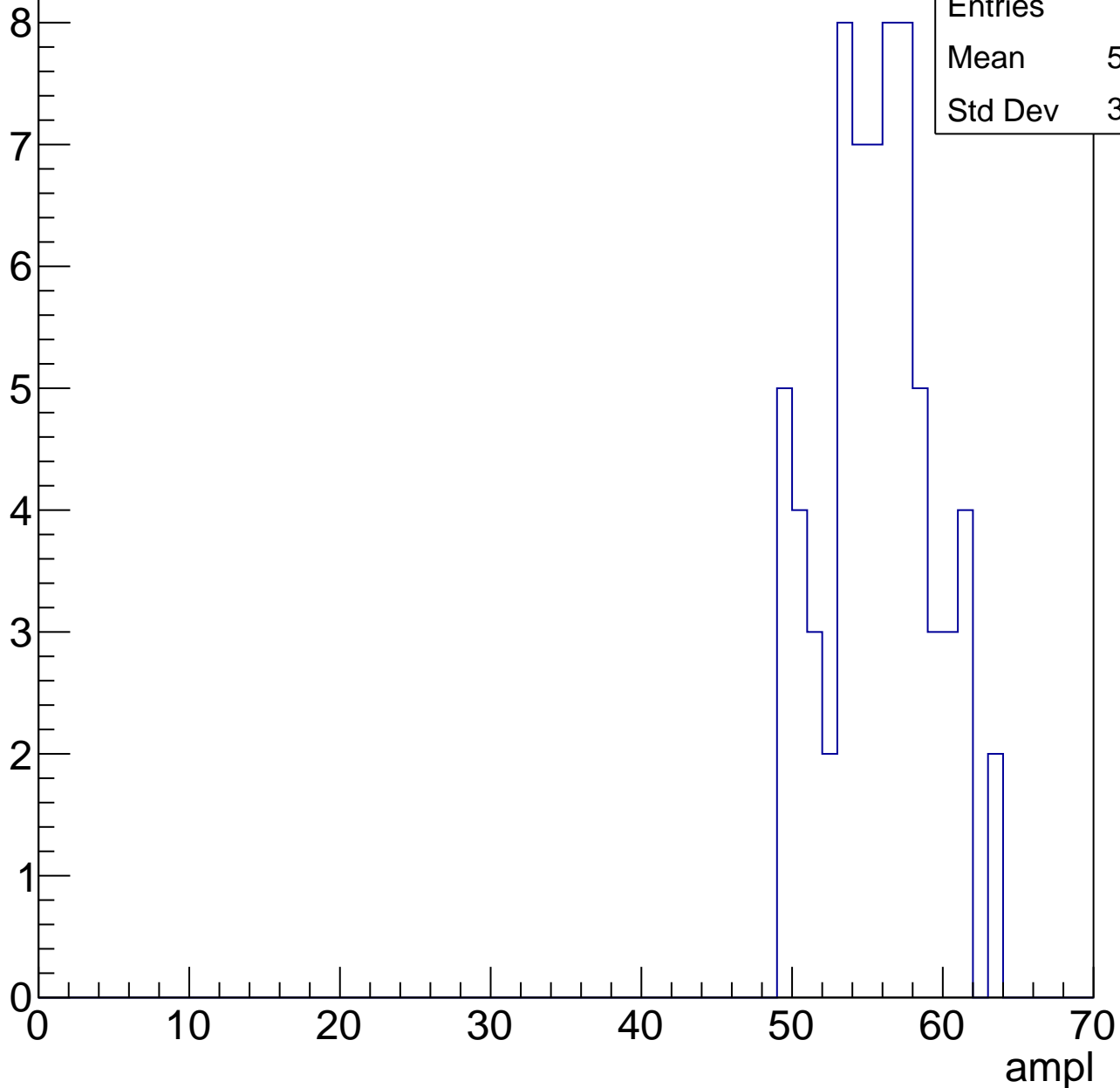


# B1L101S, U11-ch127, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	55.22
Std Dev	3.534

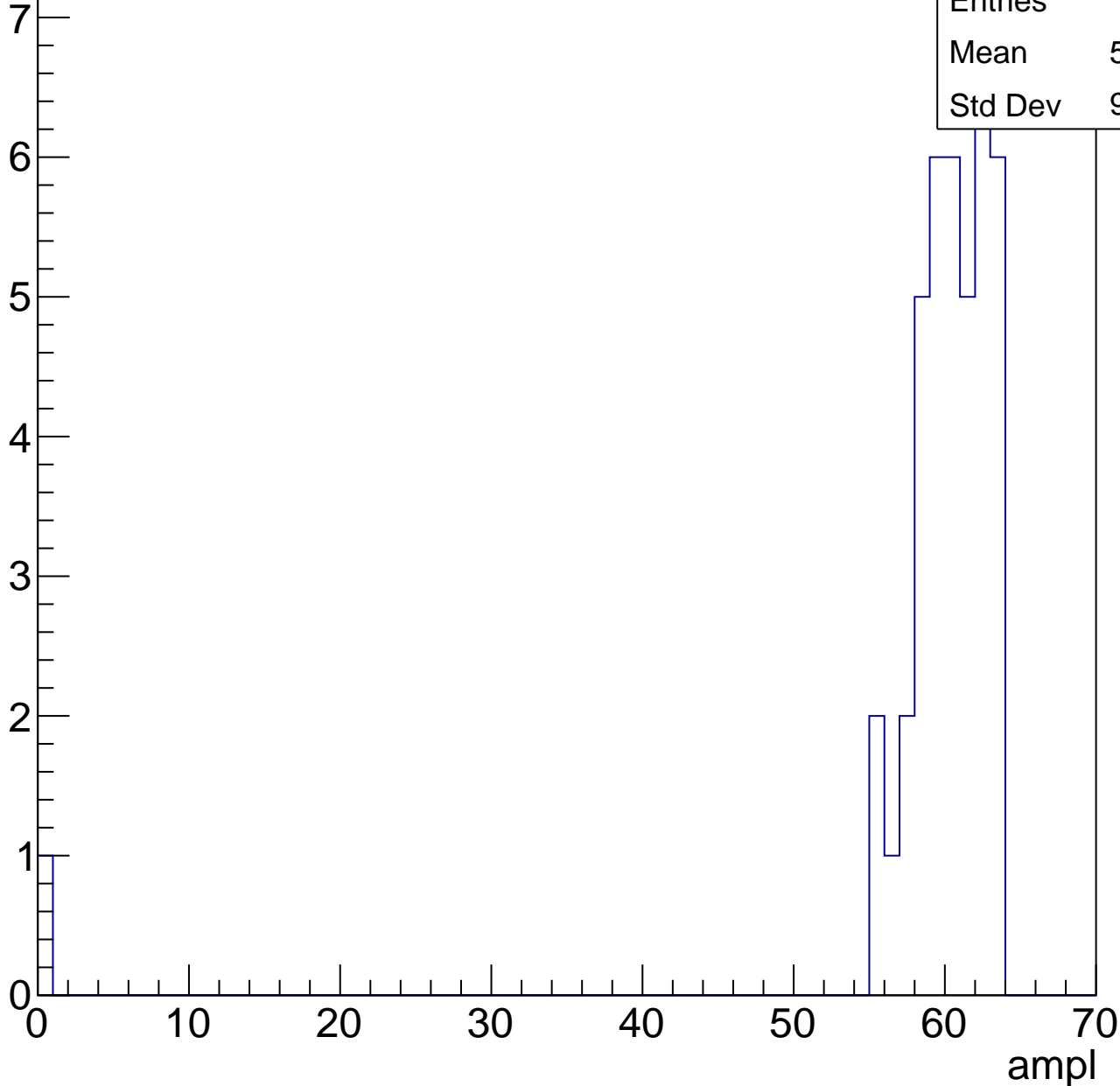


# B1L101S, U11-ch127, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	41
Mean	58.56
Std Dev	9.515



# B1L101S, U11-ch127, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

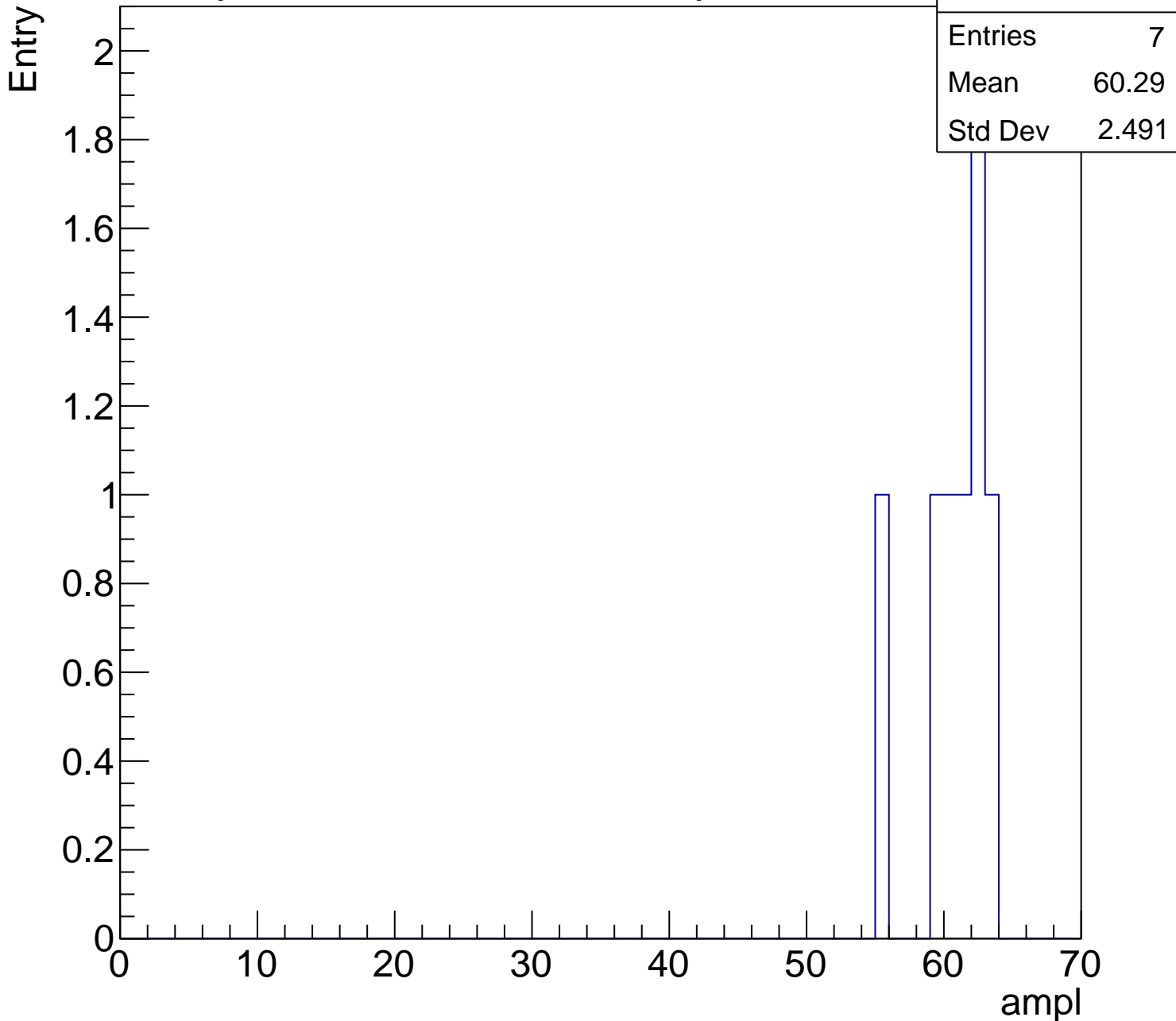
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	7
Mean	60.29
Std Dev	2.491

0 10 20 30 40 50 60 70

ampl

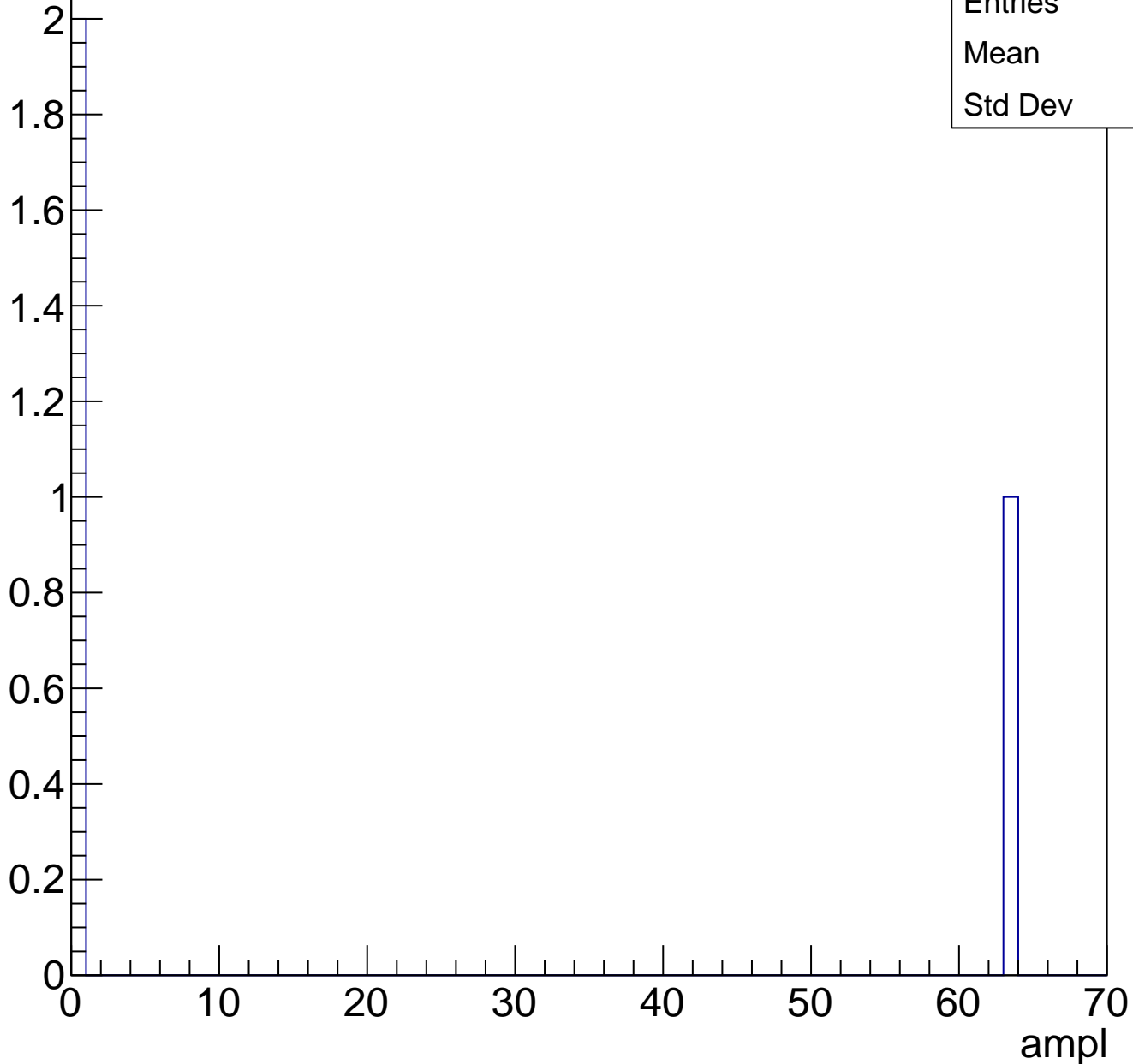




# B1L101S, U11-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

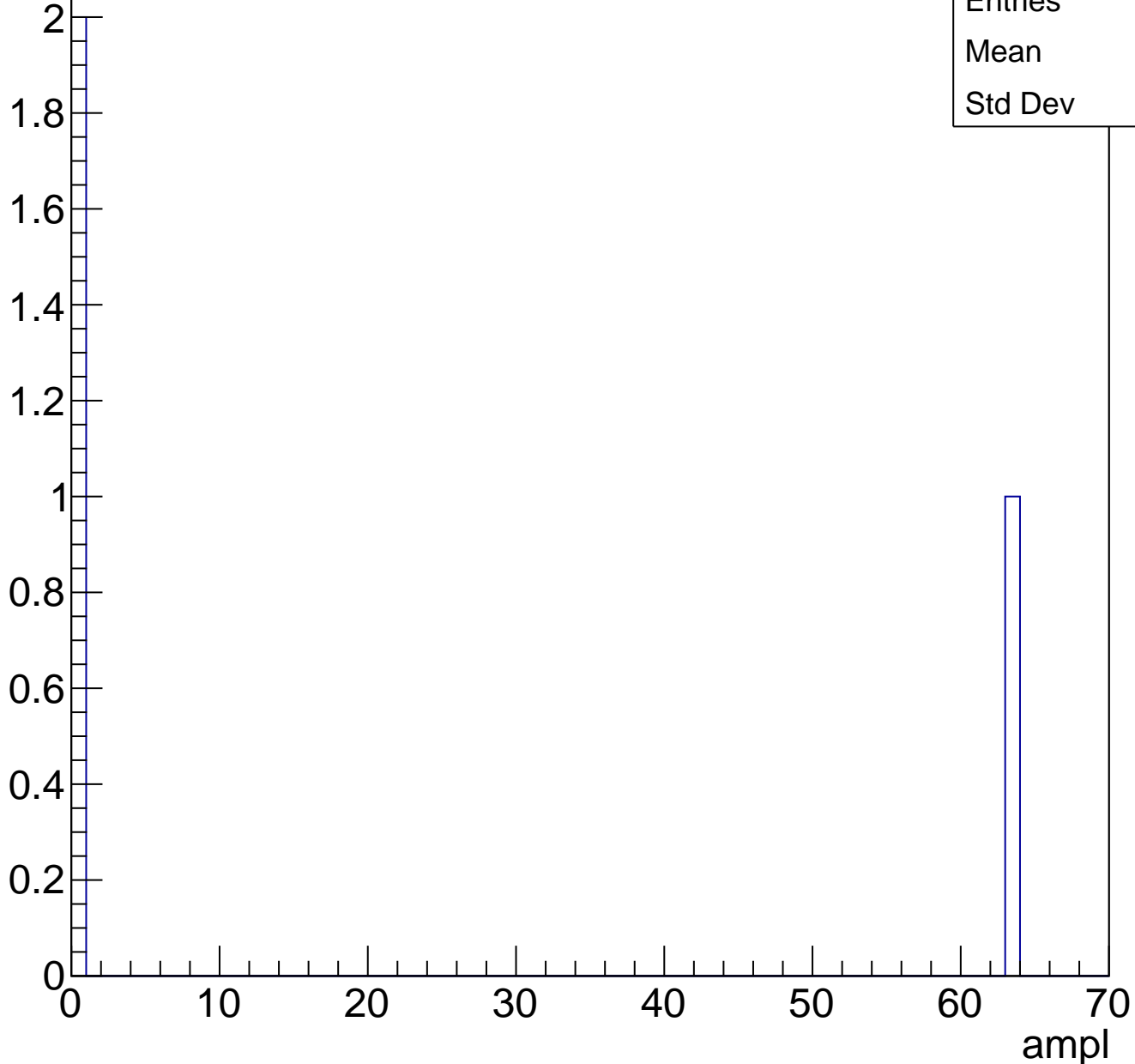
Entry



# B1L101S, U11-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	21
Std Dev	29.7