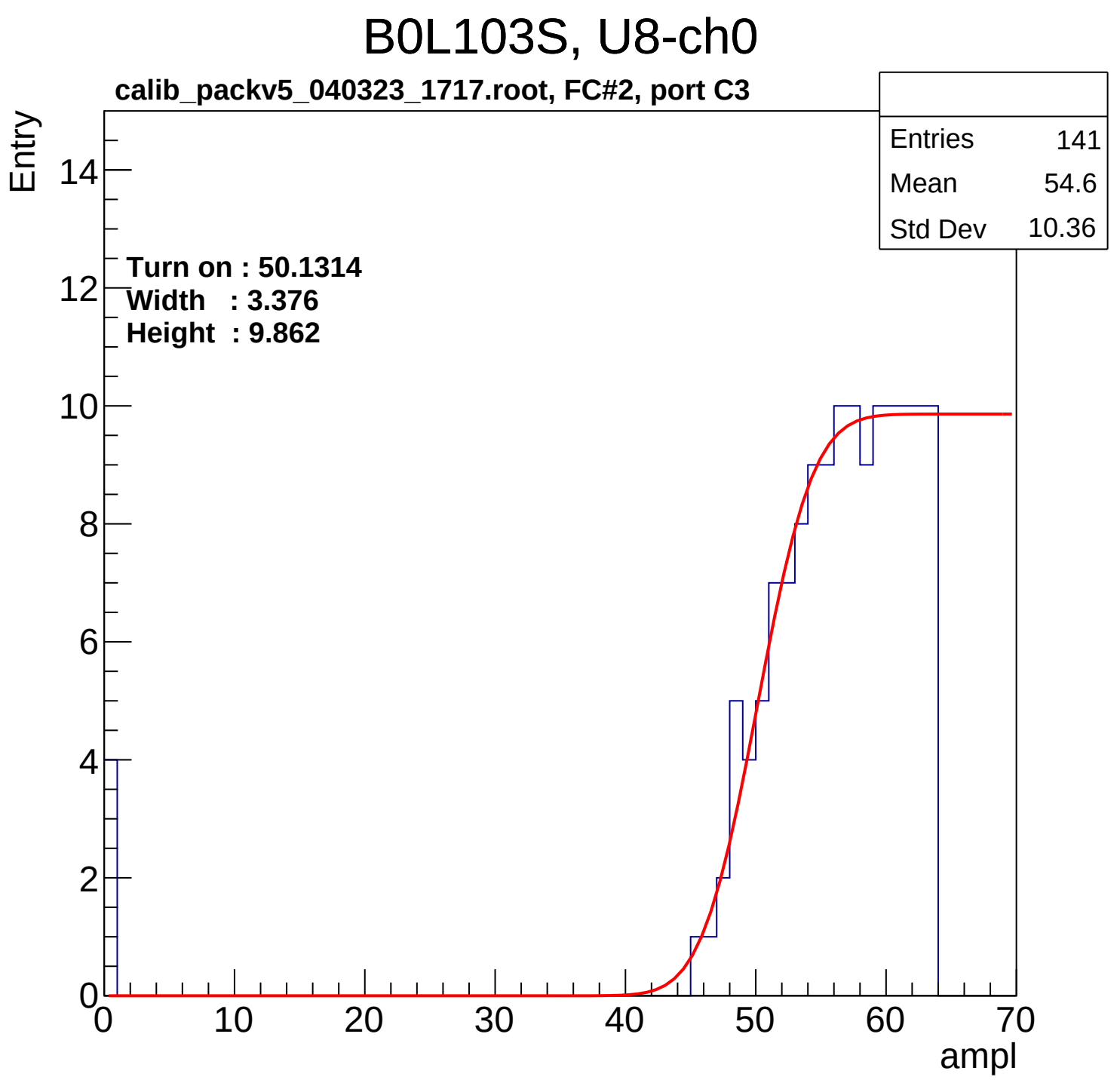
B0L103S, U8-ch0
calib_packv5_040323_1717.root, FC#2, port C3
Entries 141
Mean 54.6
Std Dev 10.36
Turn on : 50.1314
Width : 3.376
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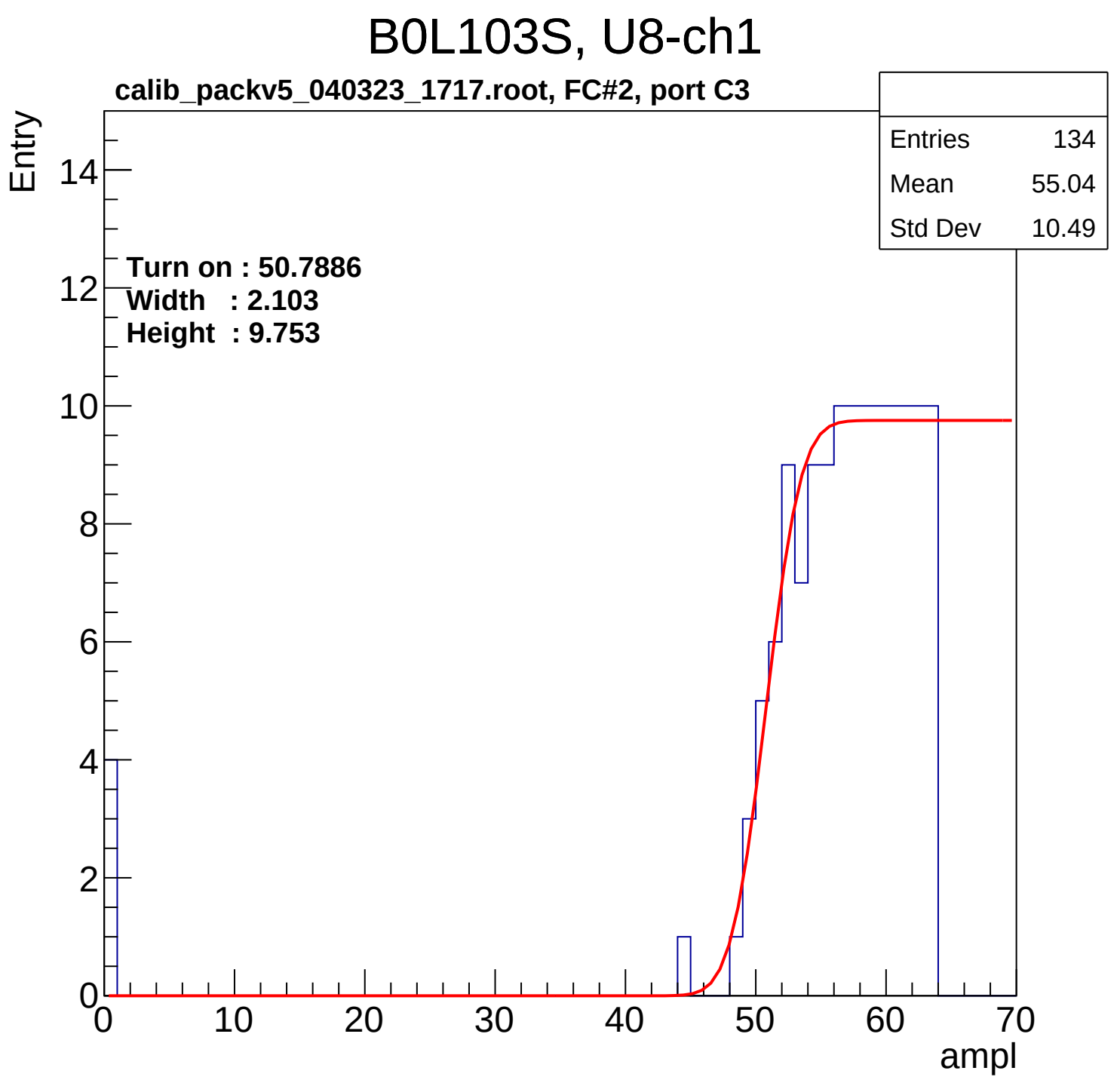
B0L103S, U8-ch1
calib_packv5_040323_1717.root, FC#2, port C3
Entries 134
Mean 55.04
Std Dev 10.49
Turn on : 50.7886
Width : 2.103
Height : 9.753
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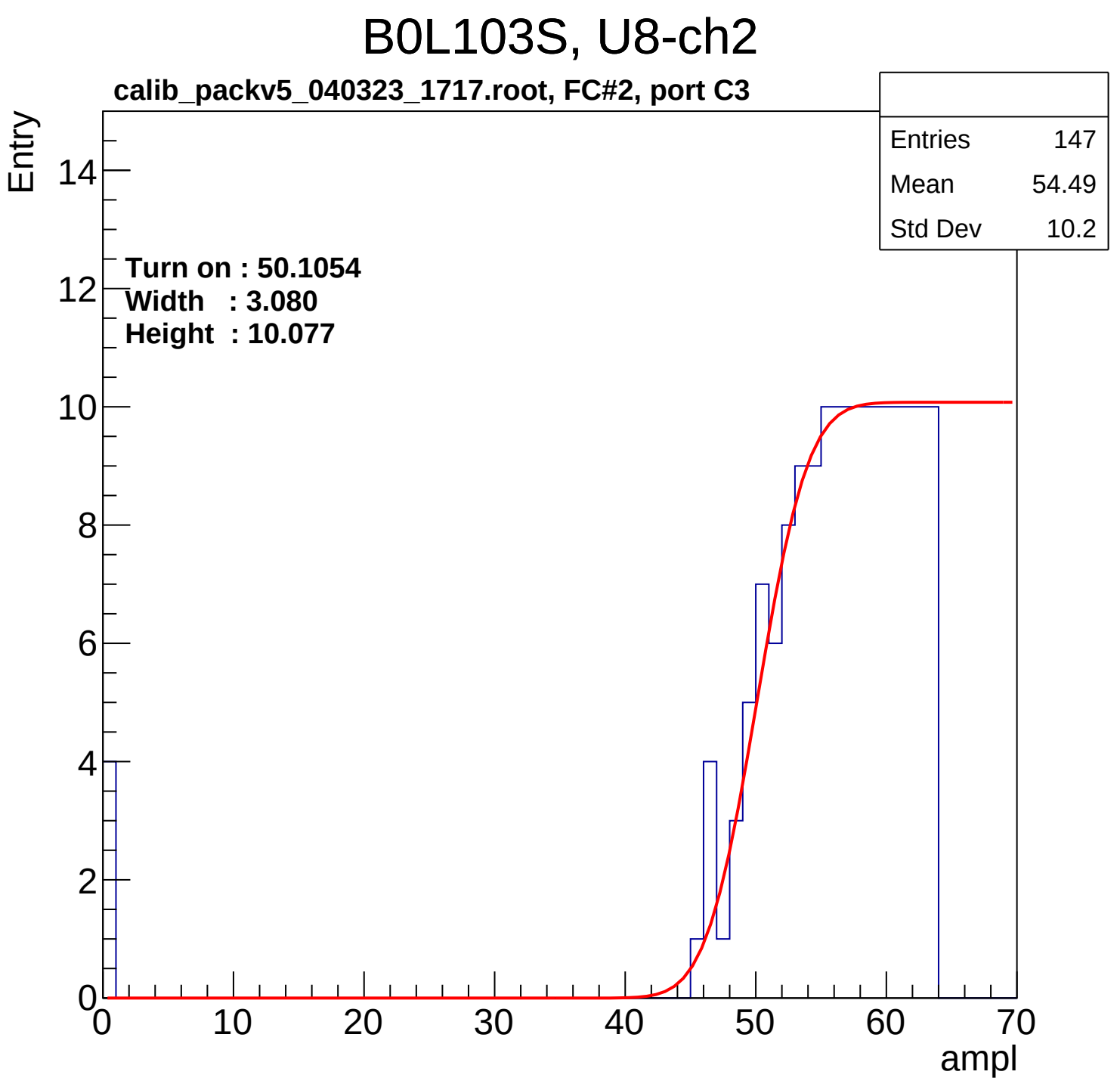
B0L103S, U8-ch2
calib_packv5_040323_1717.root, FC#2, port C3
Entries 147
Mean 54.49
Std Dev 10.2
Turn on : 50.1054
Width : 3.080
Height : 10.077
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ampl
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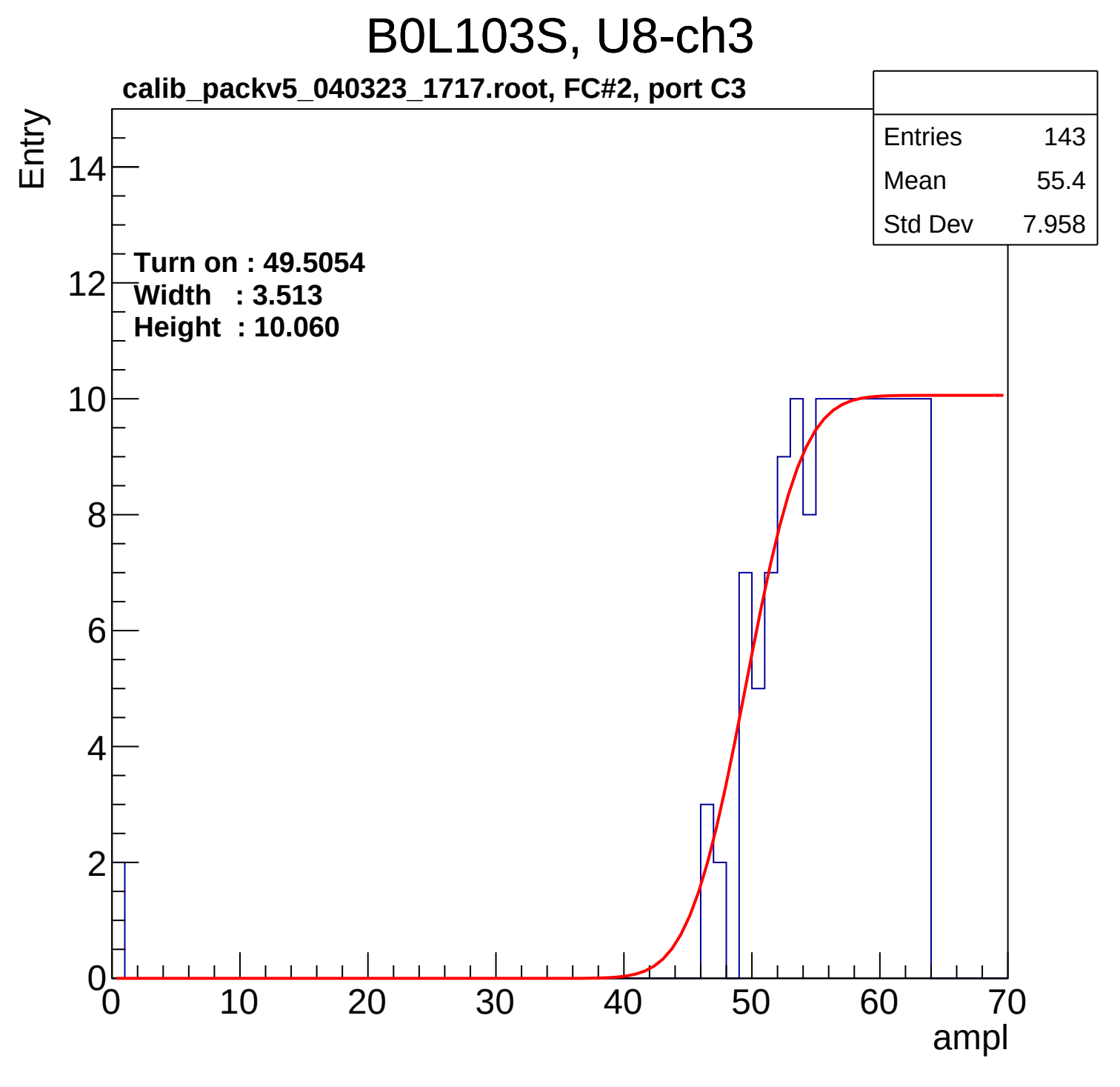
B0L103S, U8-ch3
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 55.4
Std Dev 7.958
Turn on : 49.5054
Width : 3.513
Height : 10.060
Entry
ampl
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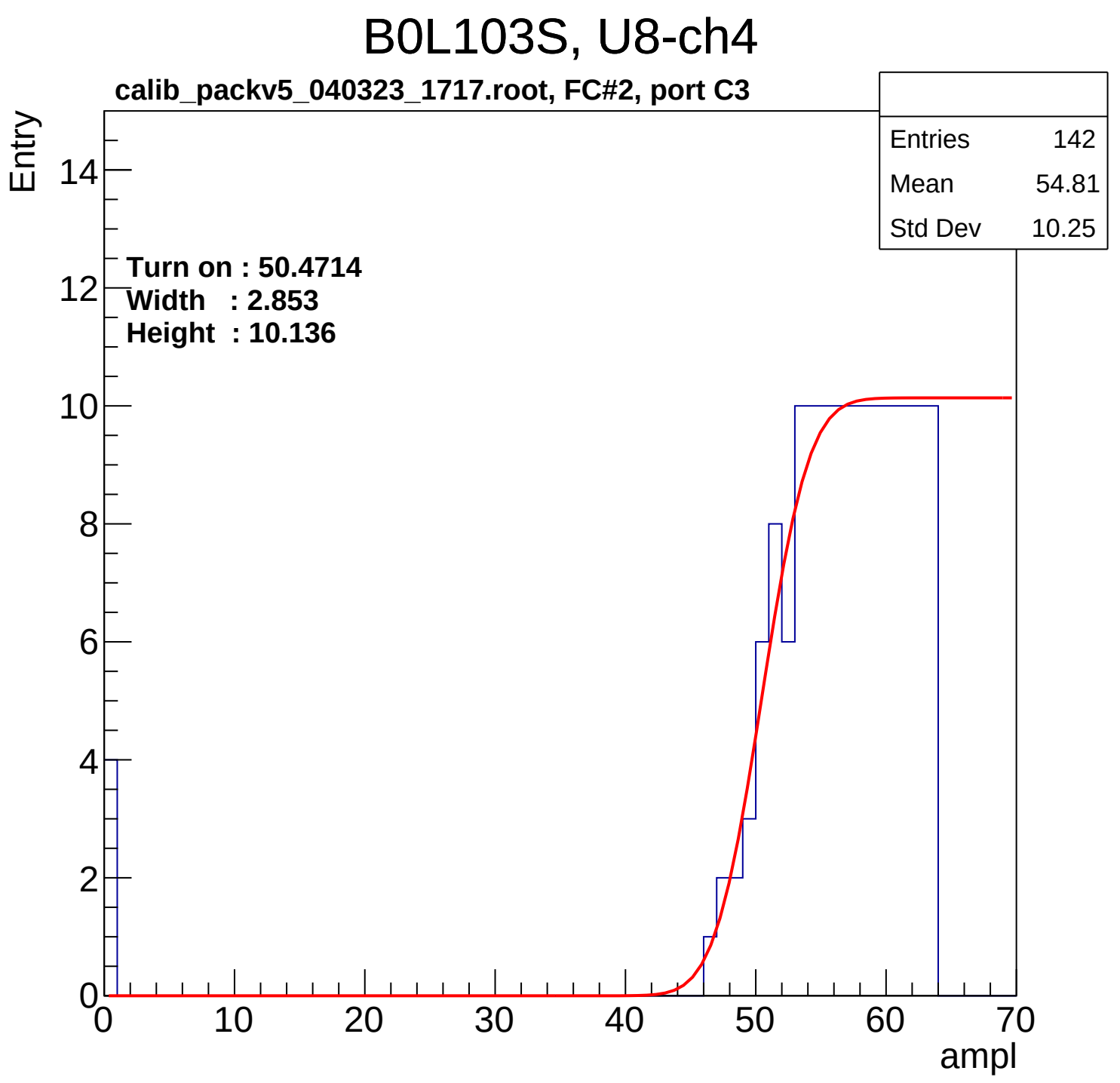
B0L103S, U8-ch4
calib_packv5_040323_1717.root, FC#2, port C3
Entries 142
Mean 54.81
Std Dev 10.25
Turn on : 50.4714
Width : 2.853
Height : 10.136
Entry
ampl
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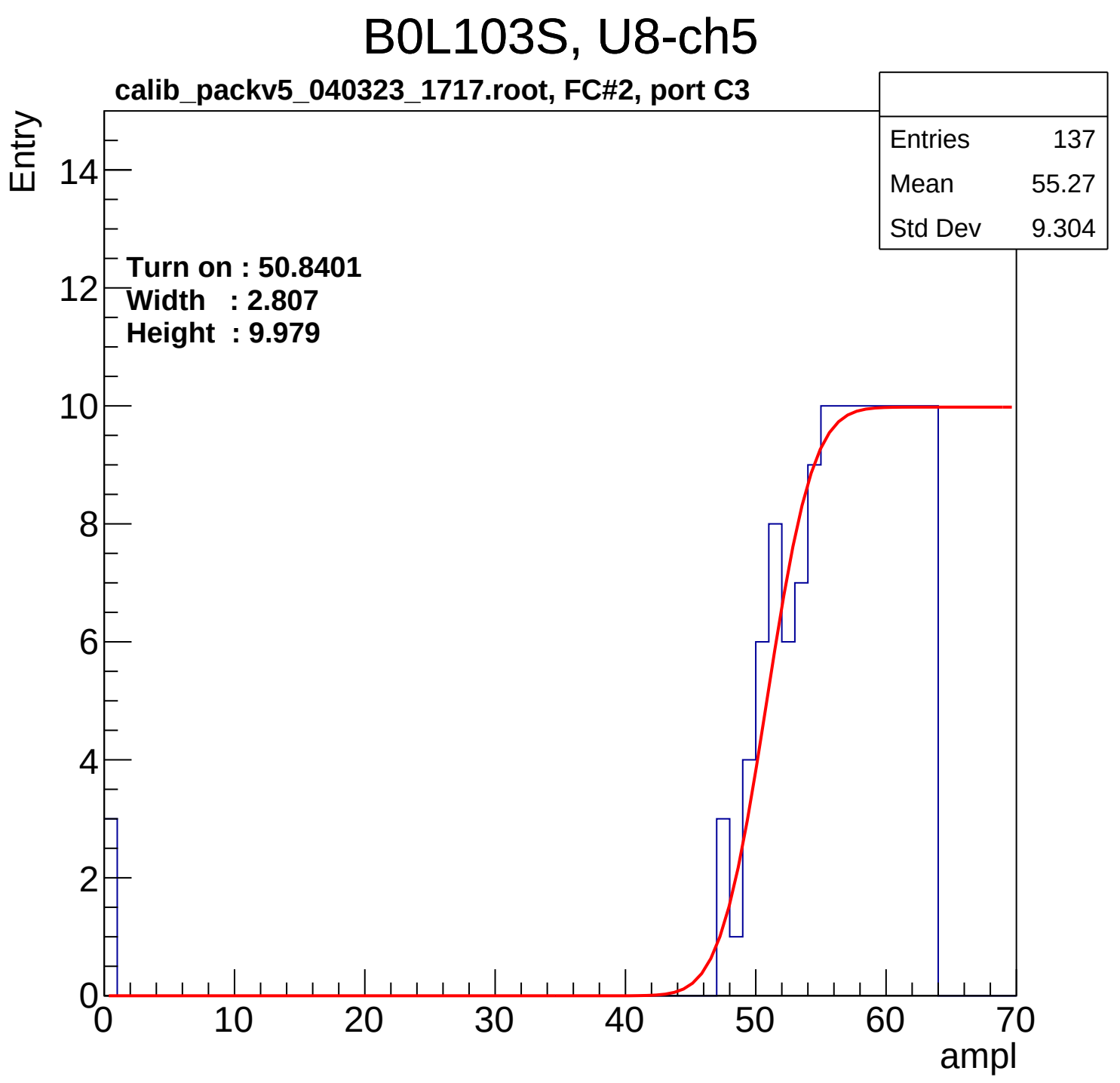
B0L103S, U8-ch5
calib_packv5_040323_1717.root, FC#2, port C3
Entries 137
Mean 55.27
Std Dev 9.304
Turn on : 50.8401
Width : 2.807
Height : 9.979
Entry
ampl
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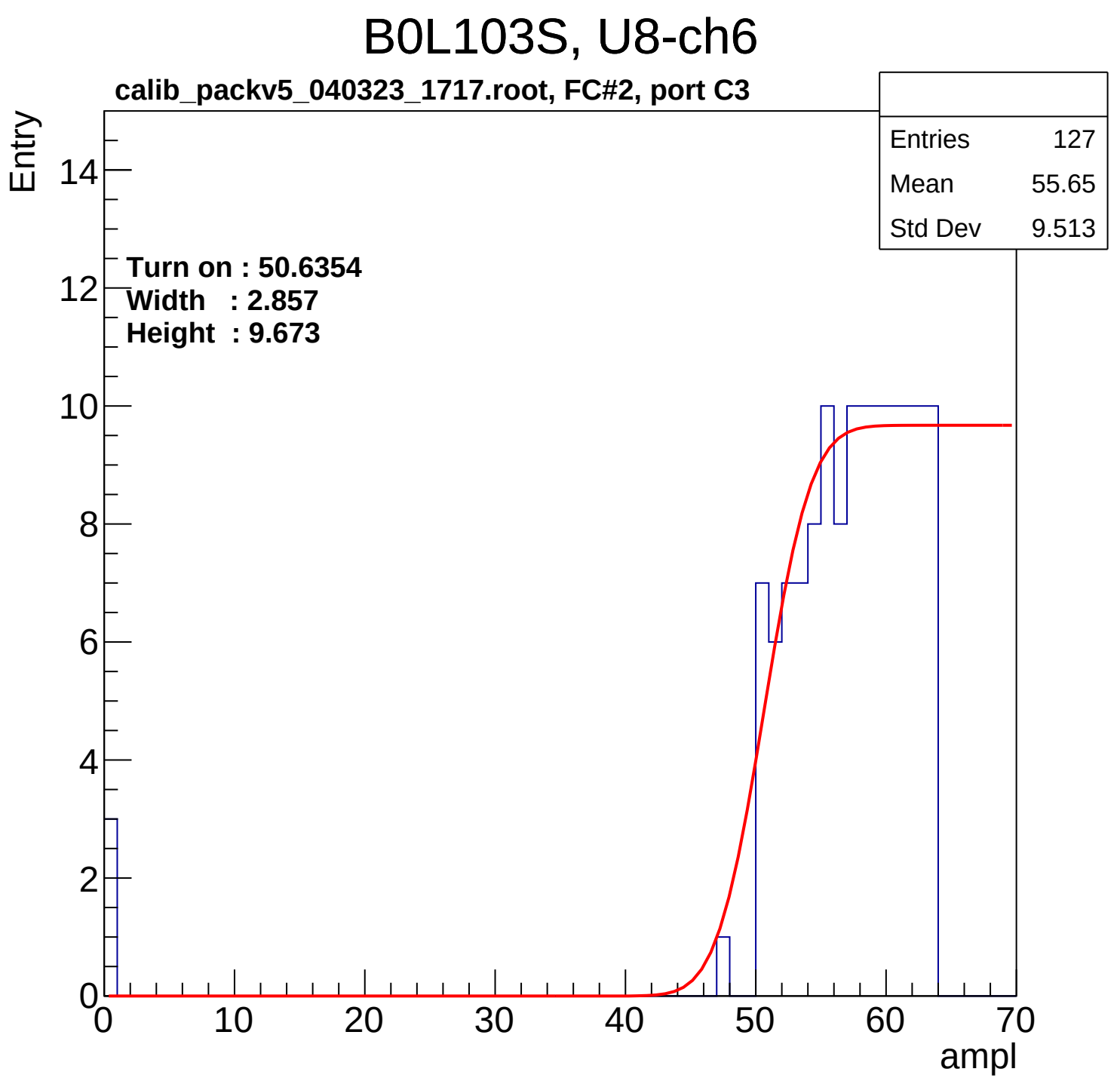
B0L103S, U8-ch6
calib_packv5_040323_1717.root, FC#2, port C3
Entries 127
Mean 55.65
Std Dev 9.513
Turn on : 50.6354
Width : 2.857
Height : 9.673
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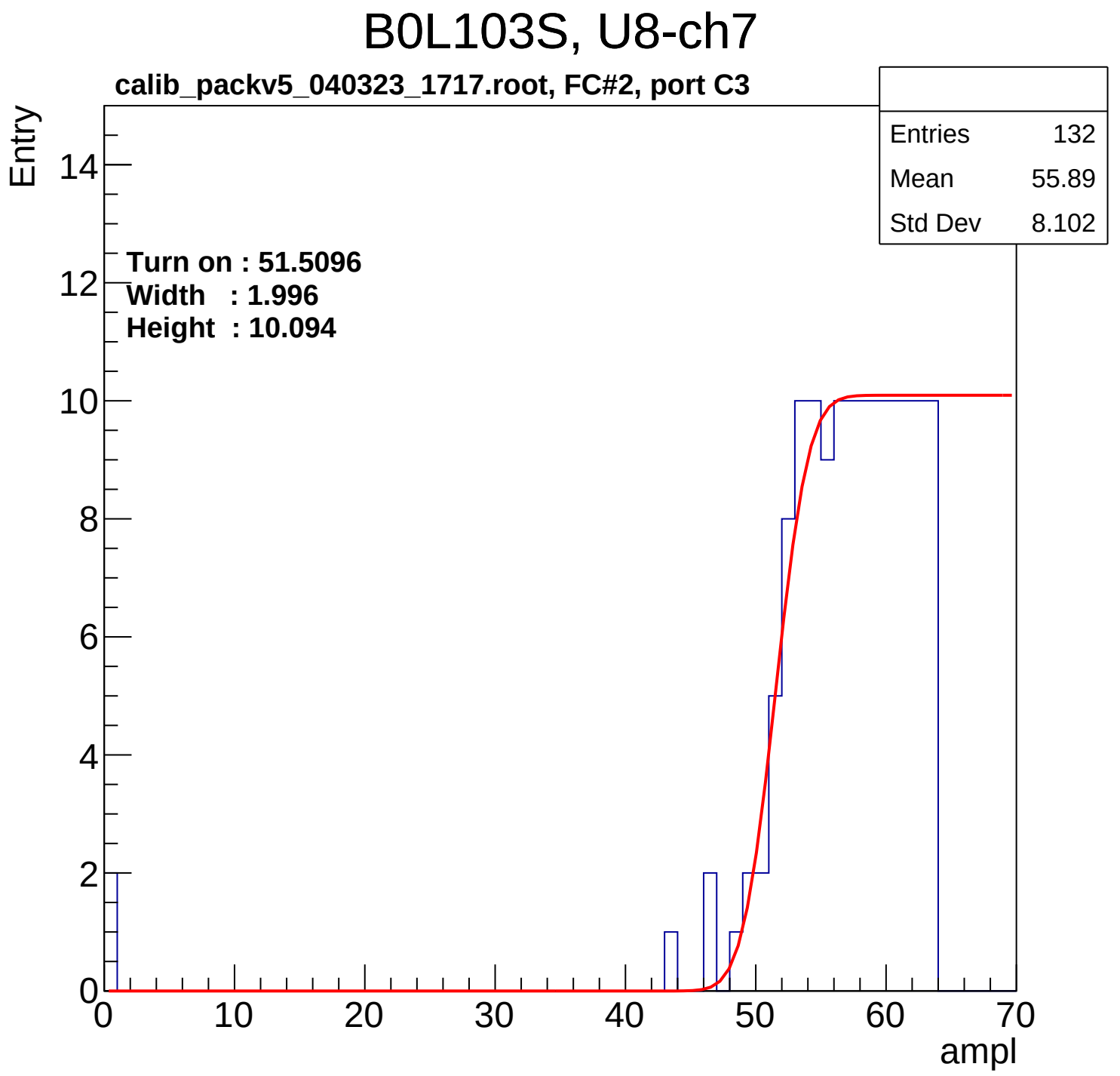
B0L103S, U8-ch7
calib_packv5_040323_1717.root, FC#2, port C3
Entries 132
Mean 55.89
Std Dev 8.102
Turn on : 51.5096
Width : 1.996
Height : 10.094
Entry
ampl
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6
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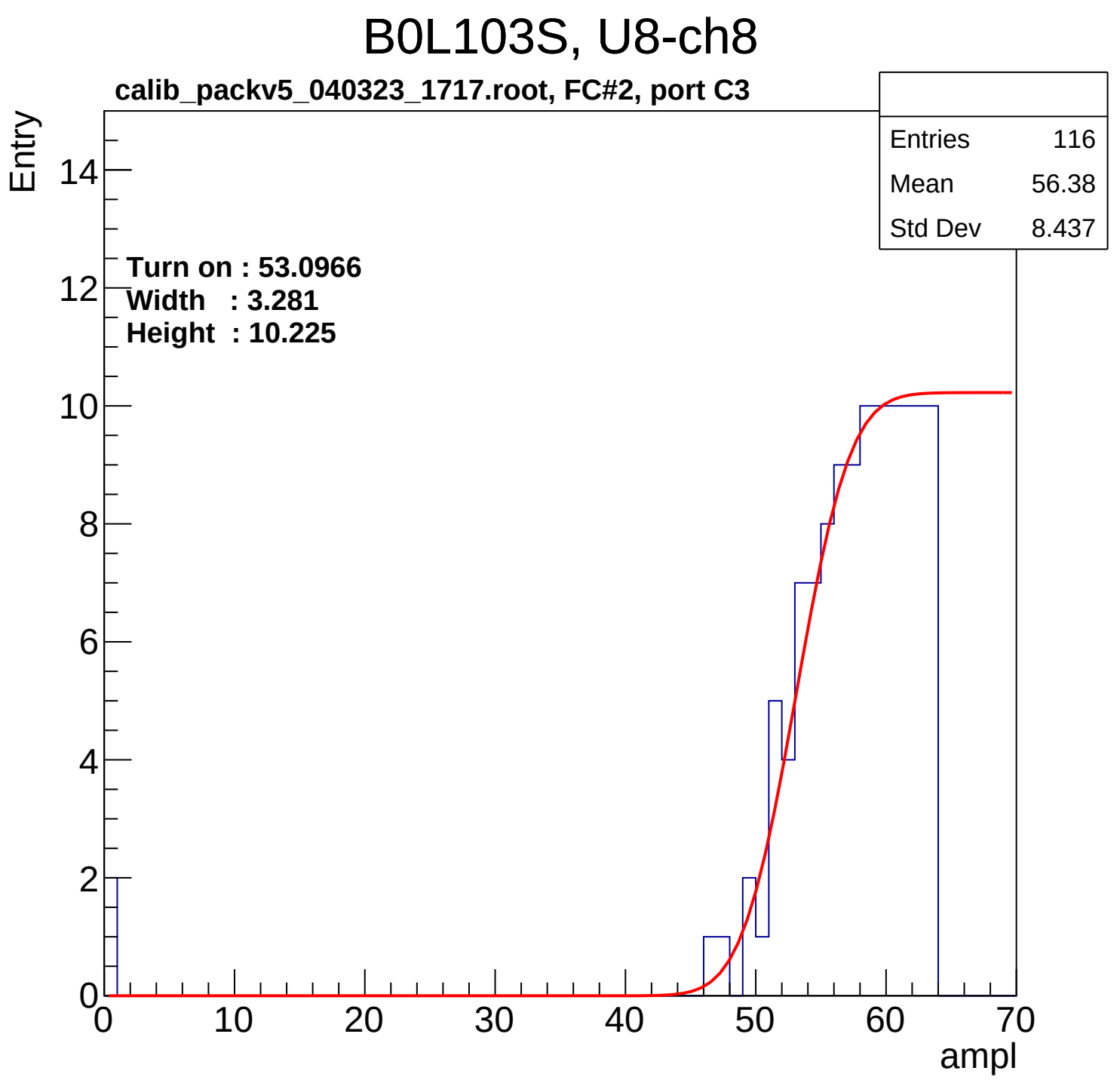
B0L103S, U8-ch8
calib_packv5_040323_1717.root, FC#2, port C3
Entries 116
Mean 56.38
Std Dev 8.437
Turn on : 53.0966
Width : 3.281
Height : 10.225
Entry
ampl
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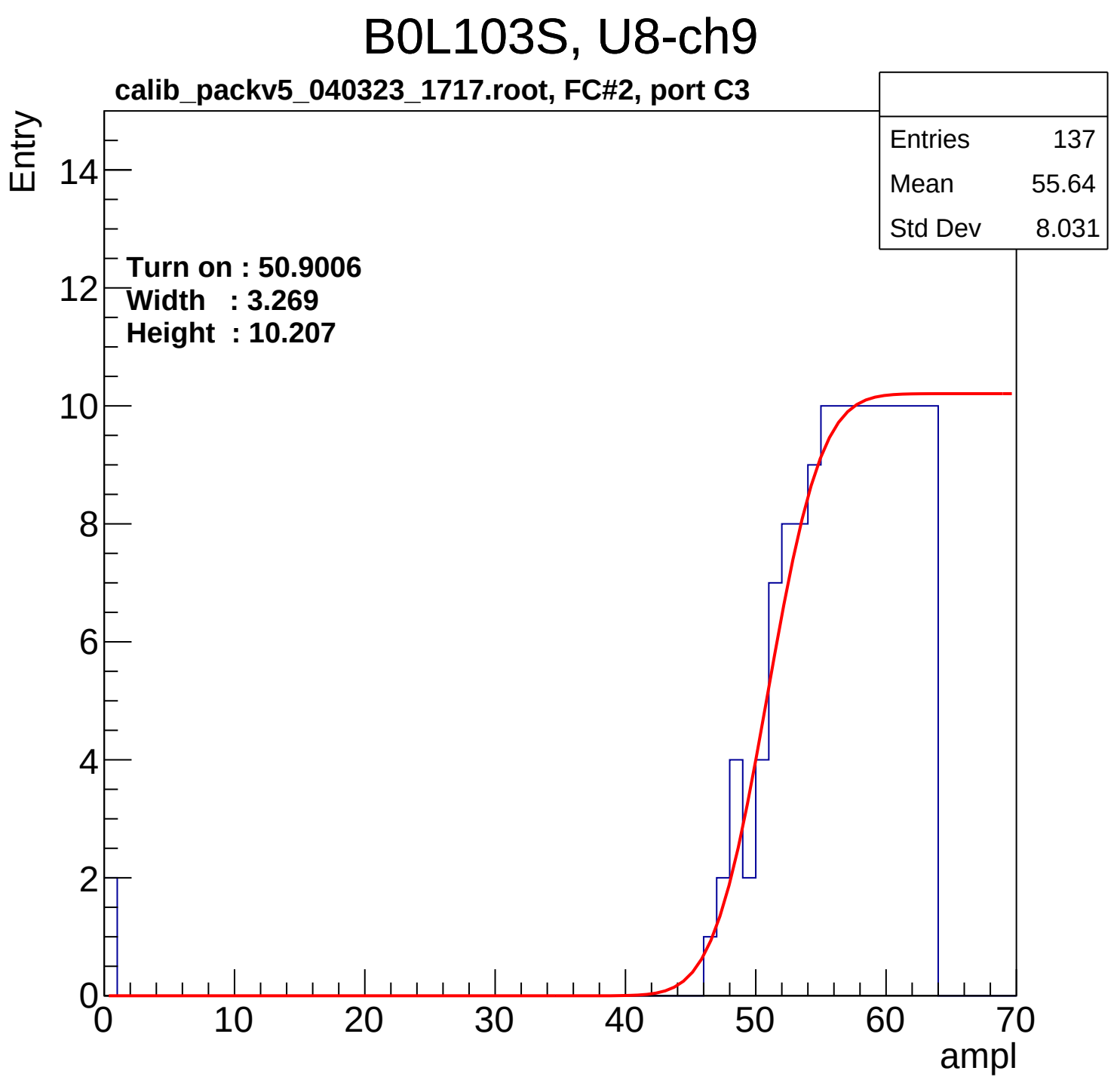
B0L103S, U8-ch9
calib_packv5_040323_1717.root, FC#2, port C3
Entries 137
Mean 55.64
Std Dev 8.031
Turn on : 50.9006
Width : 3.269
Height : 10.207
Entry
ampl
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8
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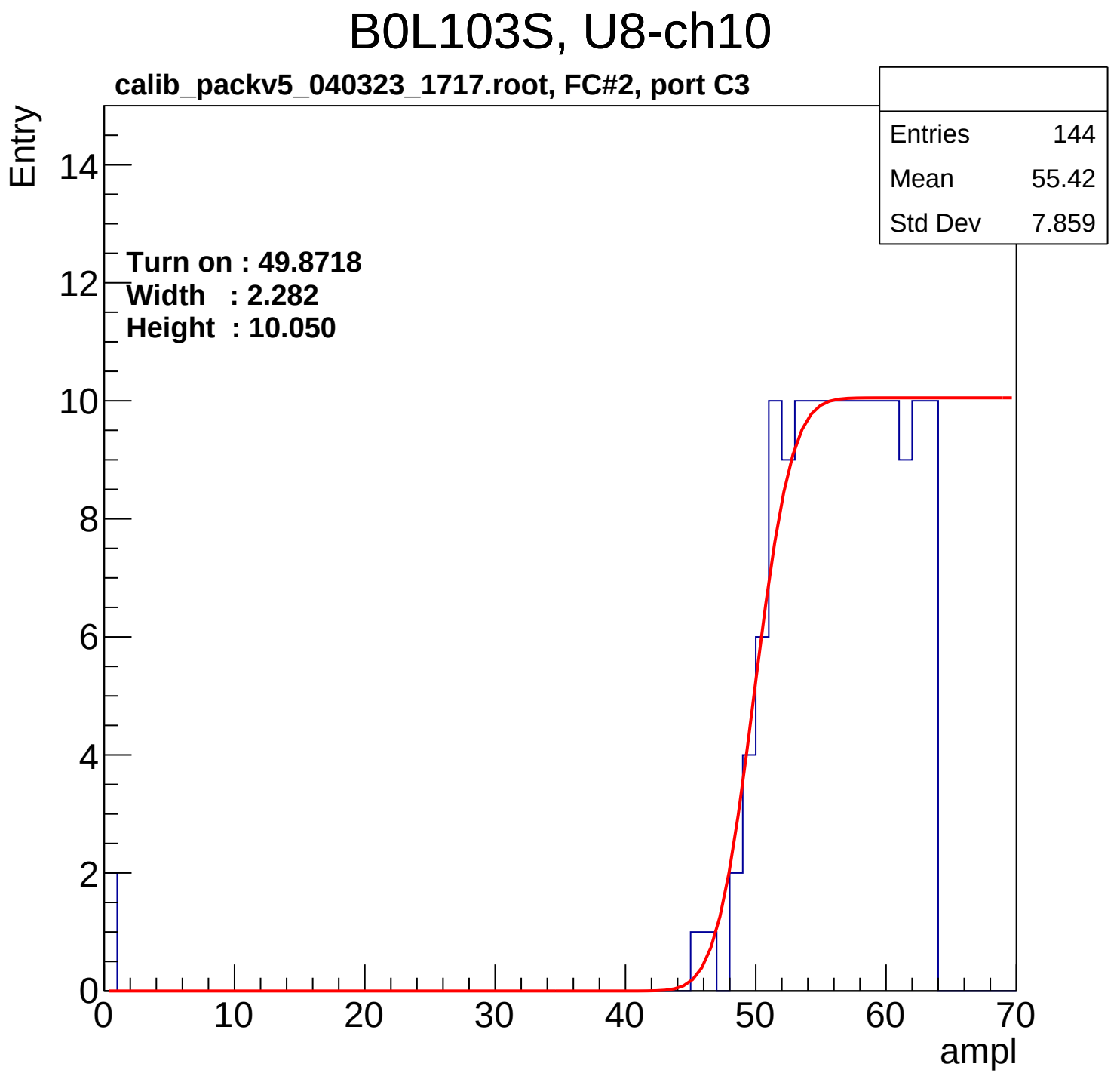
B0L103S, U8-ch10
calib_packv5_040323_1717.root, FC#2, port C3
Entries 144
Mean 55.42
Std Dev 7.859
Turn on : 49.8718
Width : 2.282
Height : 10.050
Entry
ampl
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6
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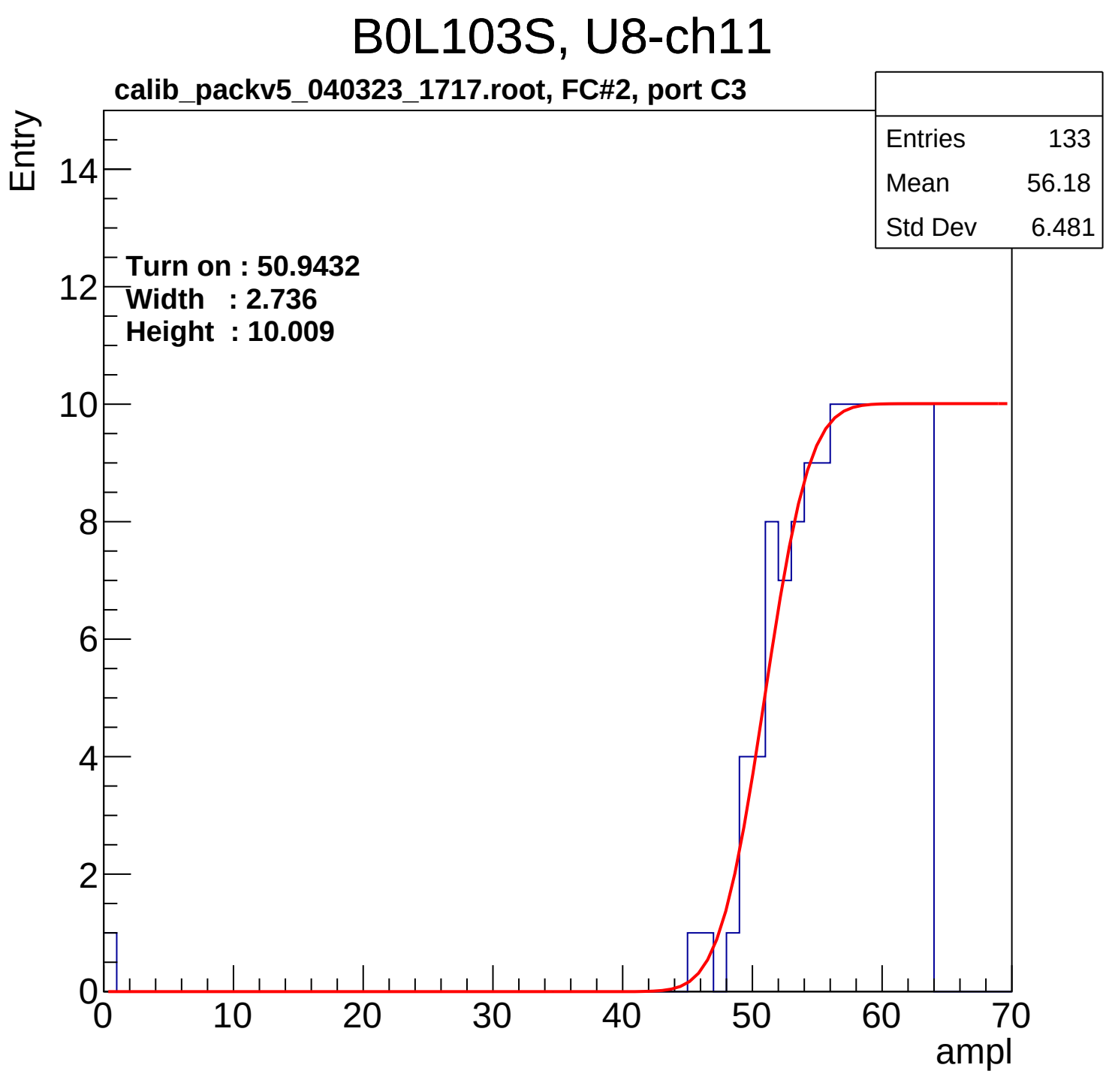
B0L103S, U8-ch11
calib_packv5_040323_1717.root, FC#2, port C3
Entries 133
Mean 56.18
Std Dev 6.481
Turn on : 50.9432
Width : 2.736
Height : 10.009
Entry
ampl
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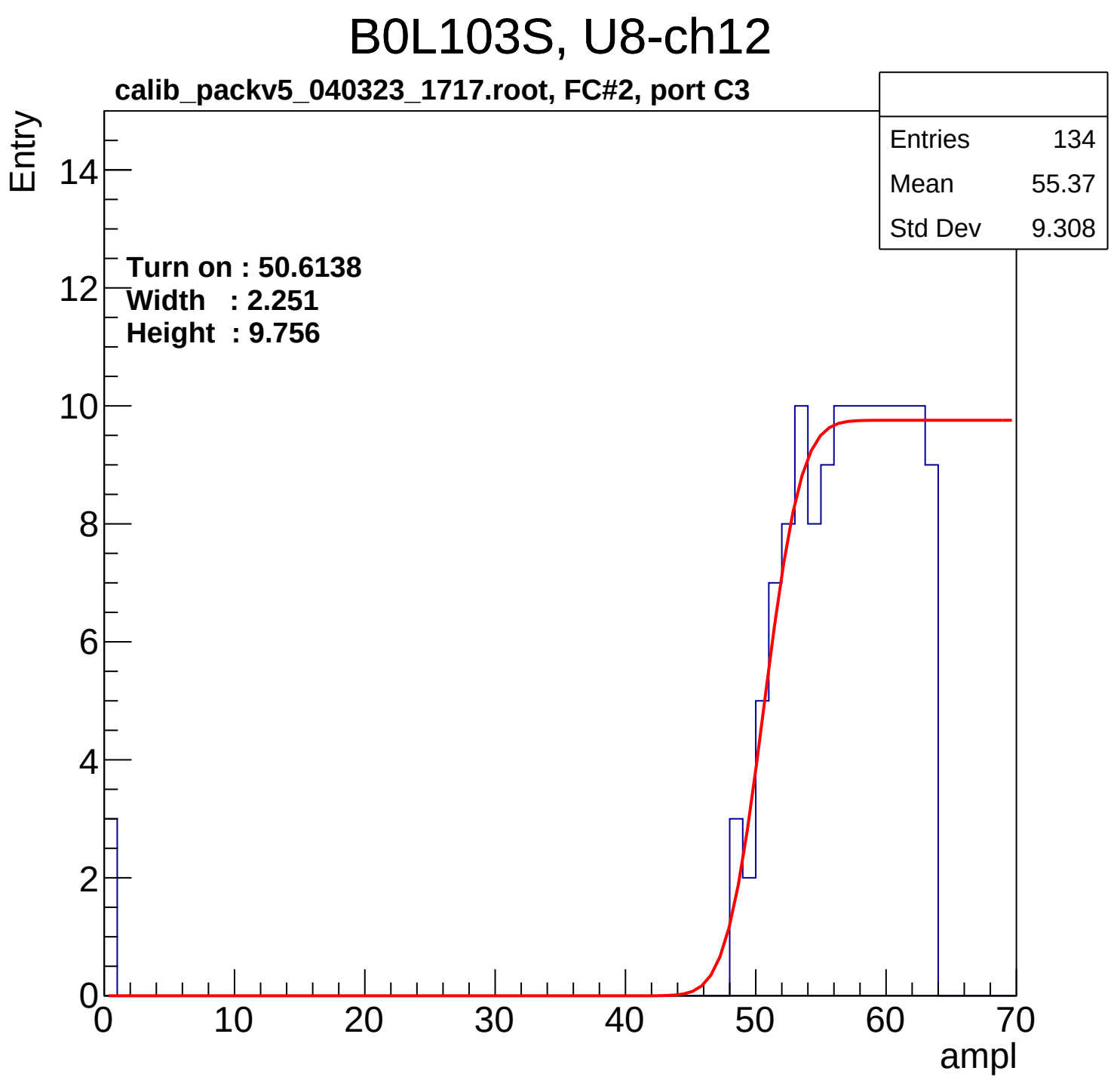
B0L103S, U8-ch12
calib_packv5_040323_1717.root, FC#2, port C3
Entries 134
Mean 55.37
Std Dev 9.308
Turn on : 50.6138
Width : 2.251
Height : 9.756
Entry
ampl
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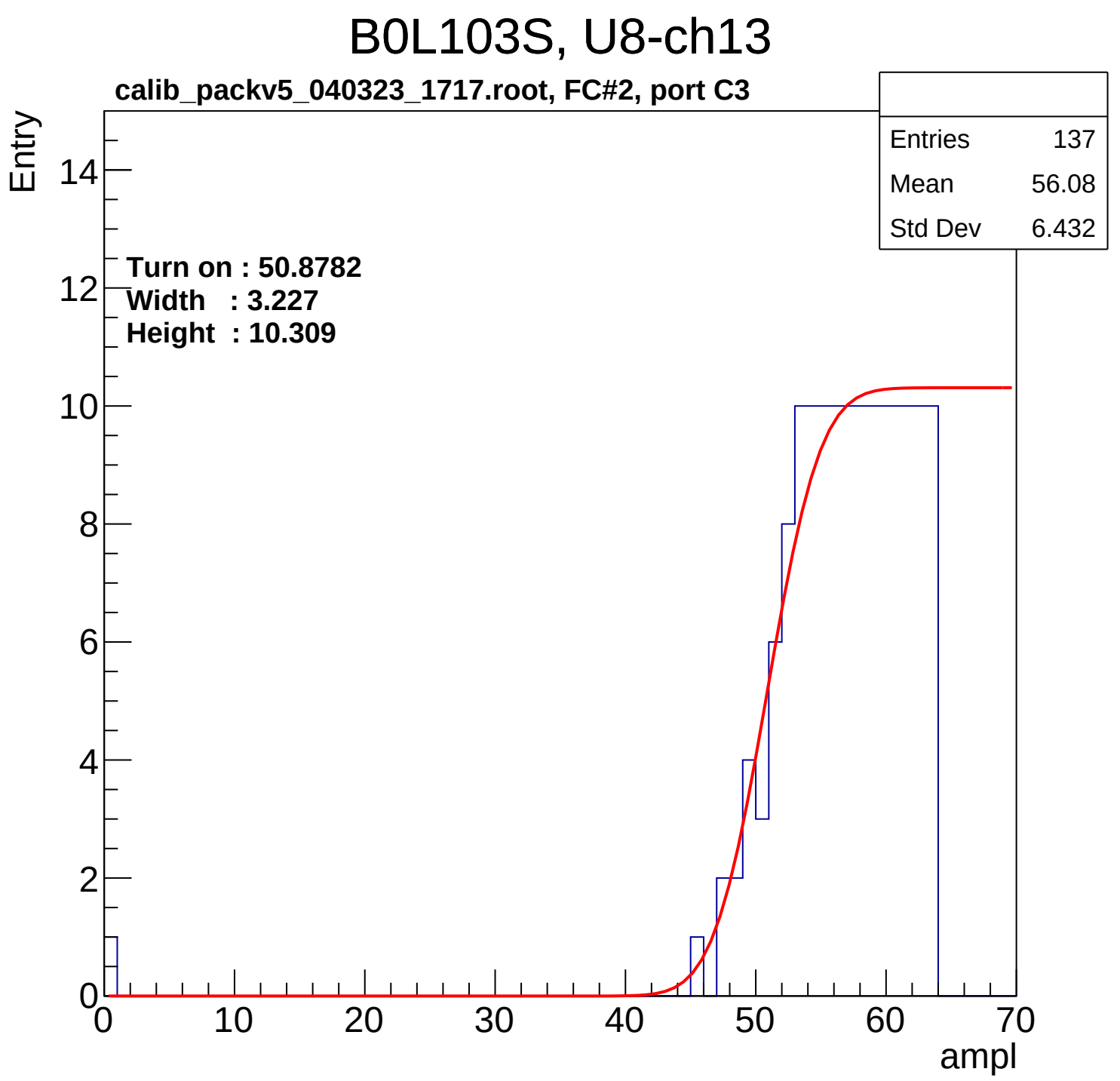
B0L103S, U8-ch13
calib_packv5_040323_1717.root, FC#2, port C3
Entries 137
Mean 56.08
Std Dev 6.432
Turn on : 50.8782
Width : 3.227
Height : 10.309
Entry
ampl
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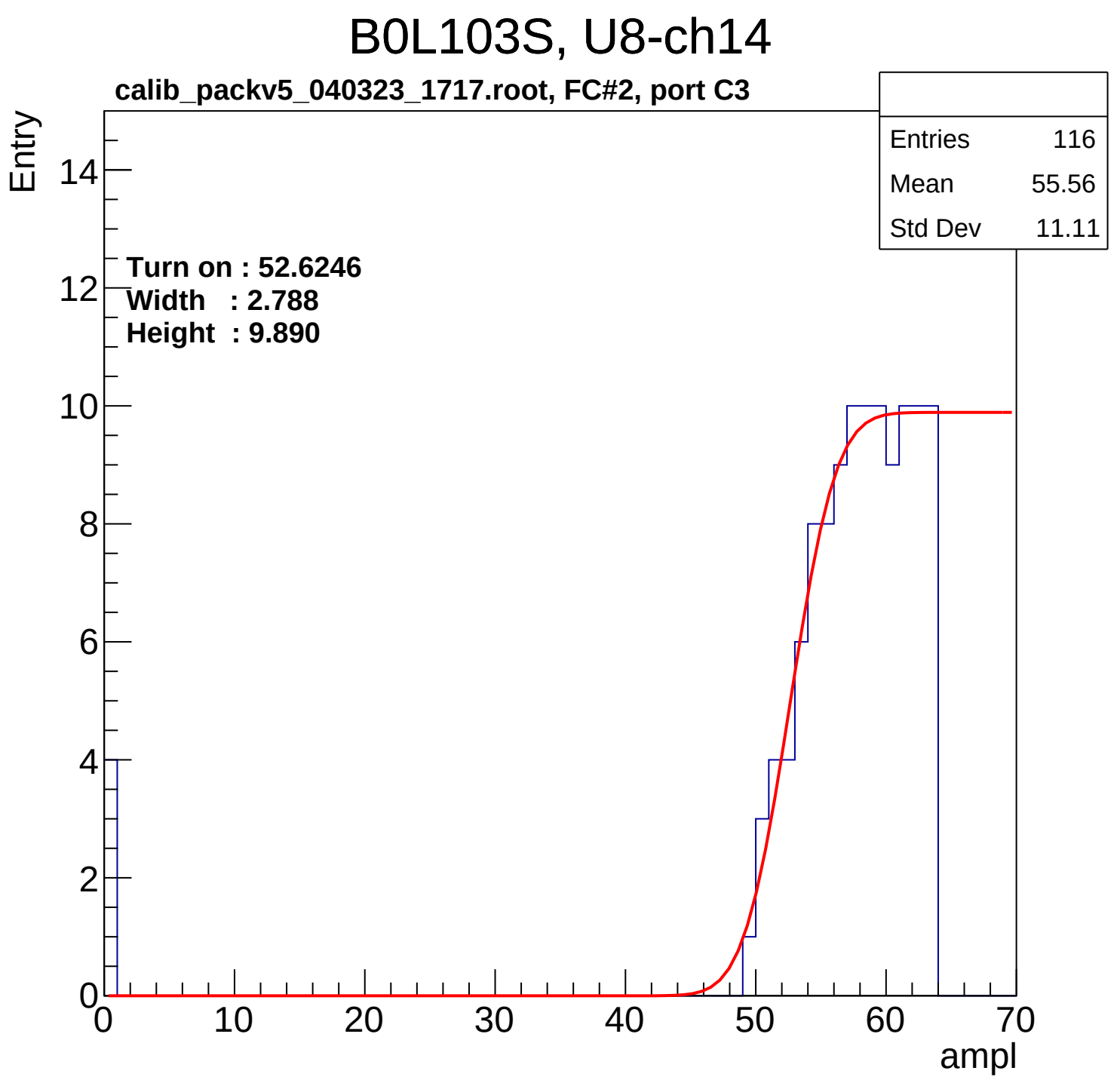
B0L103S, U8-ch14
calib_packv5_040323_1717.root, FC#2, port C3
Entries 116
Mean 55.56
Std Dev 11.11
Turn on : 52.6246
Width : 2.788
Height : 9.890
Entry
ampl
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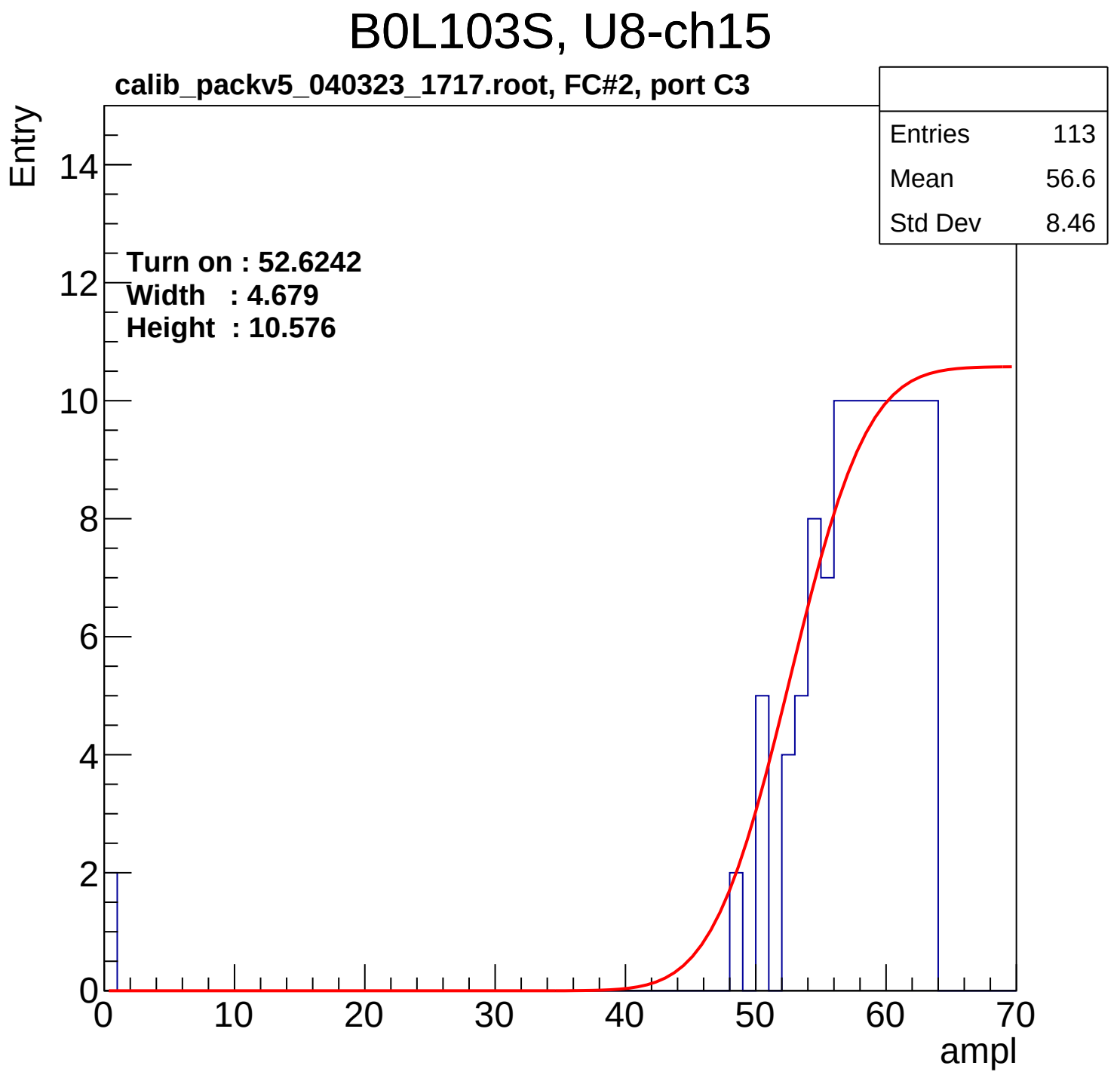
B0L103S, U8-ch15
calib_packv5_040323_1717.root, FC#2, port C3
Entries 113
Mean 56.6
Std Dev 8.46
Turn on : 52.6242
Width : 4.679
Height : 10.576
Entry
ampl
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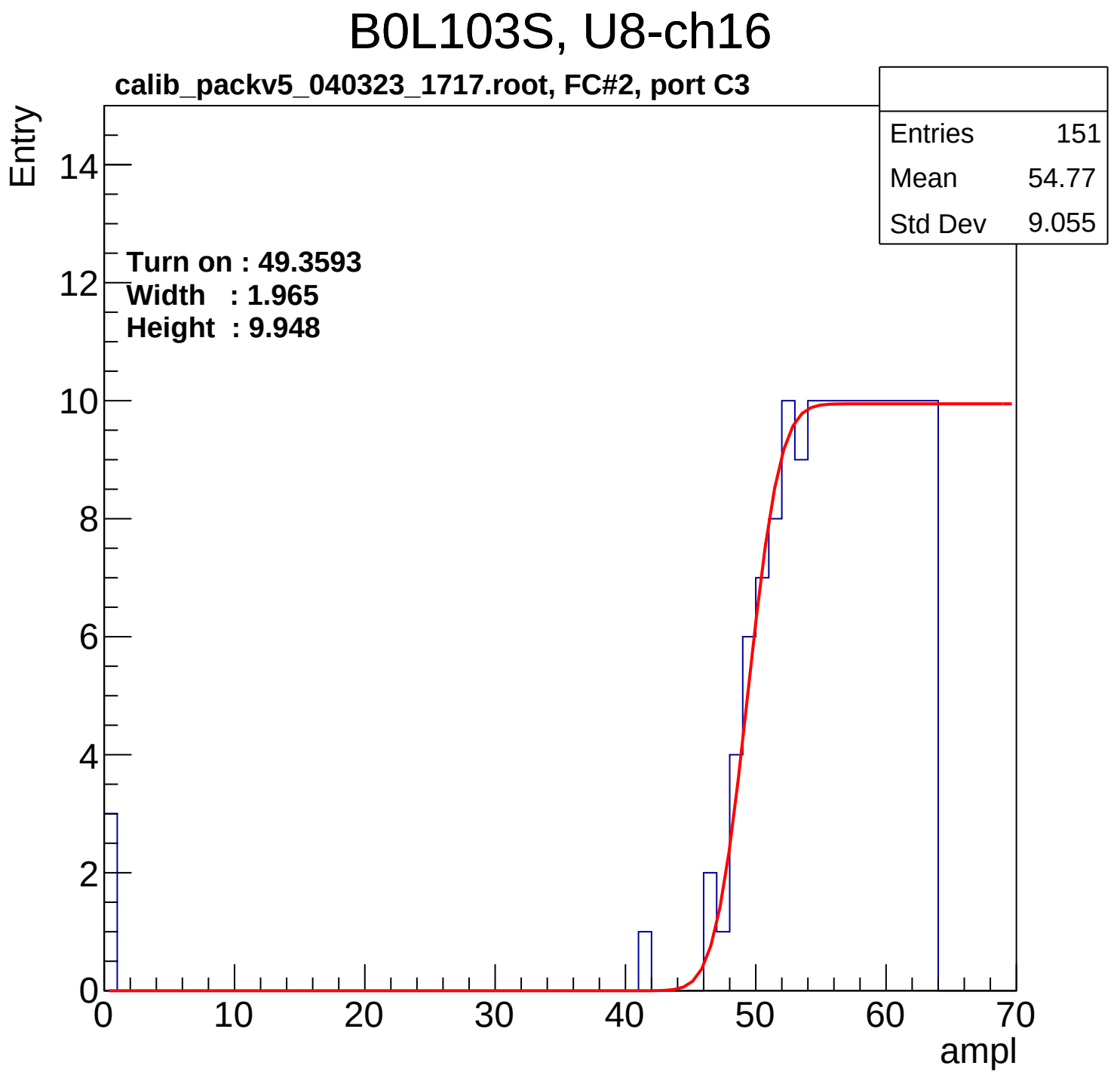
B0L103S, U8-ch16
calib_packv5_040323_1717.root, FC#2, port C3
Entries 151
Mean 54.77
Std Dev 9.055
Turn on : 49.3593
Width : 1.965
Height : 9.948
Entry
ampl
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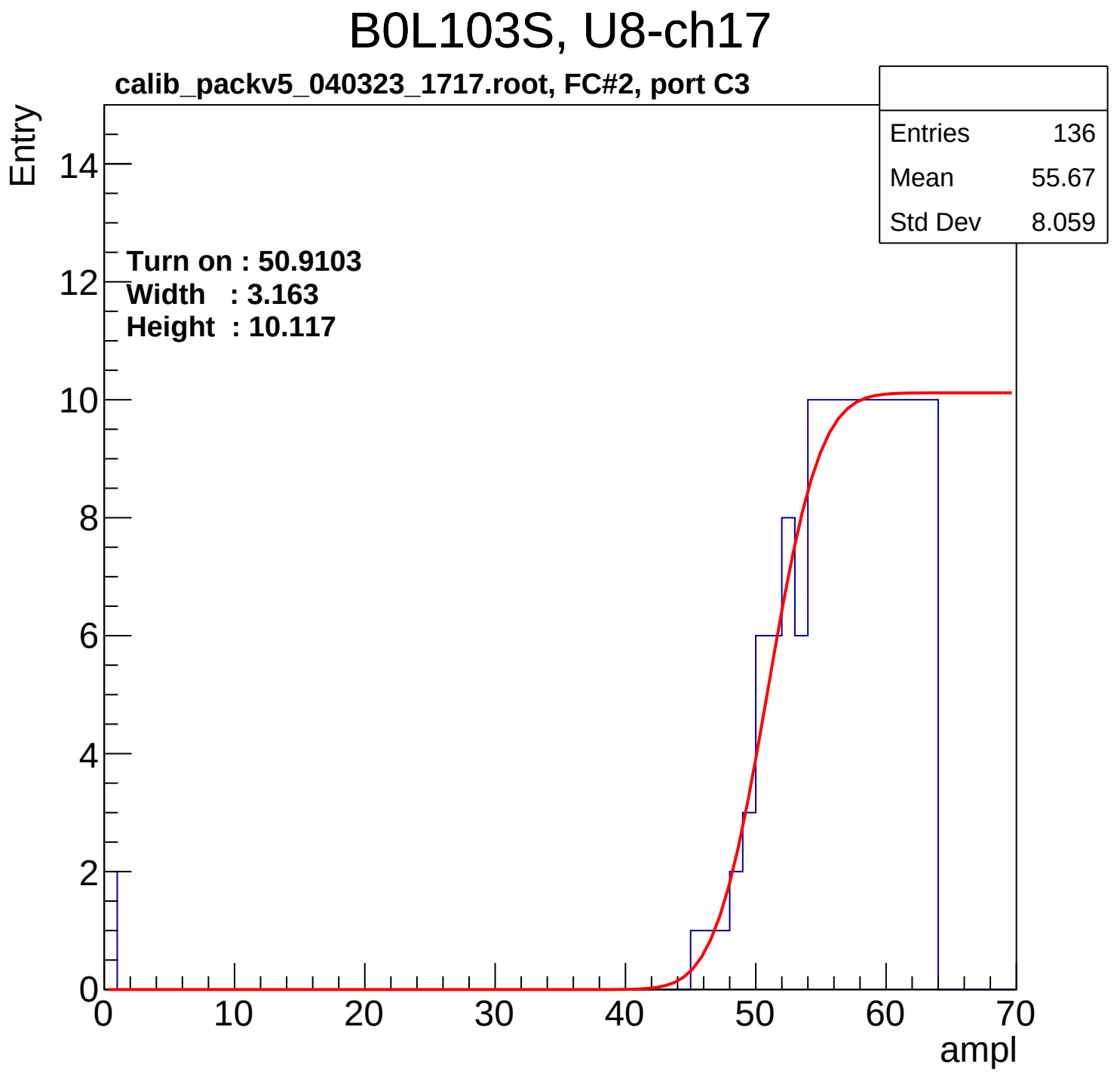
B0L103S, U8-ch17
calib_packv5_040323_1717.root, FC#2, port C3
Entries 136
Mean 55.67
Std Dev 8.059
Turn on : 50.9103
Width : 3.163
Height : 10.117
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ampl
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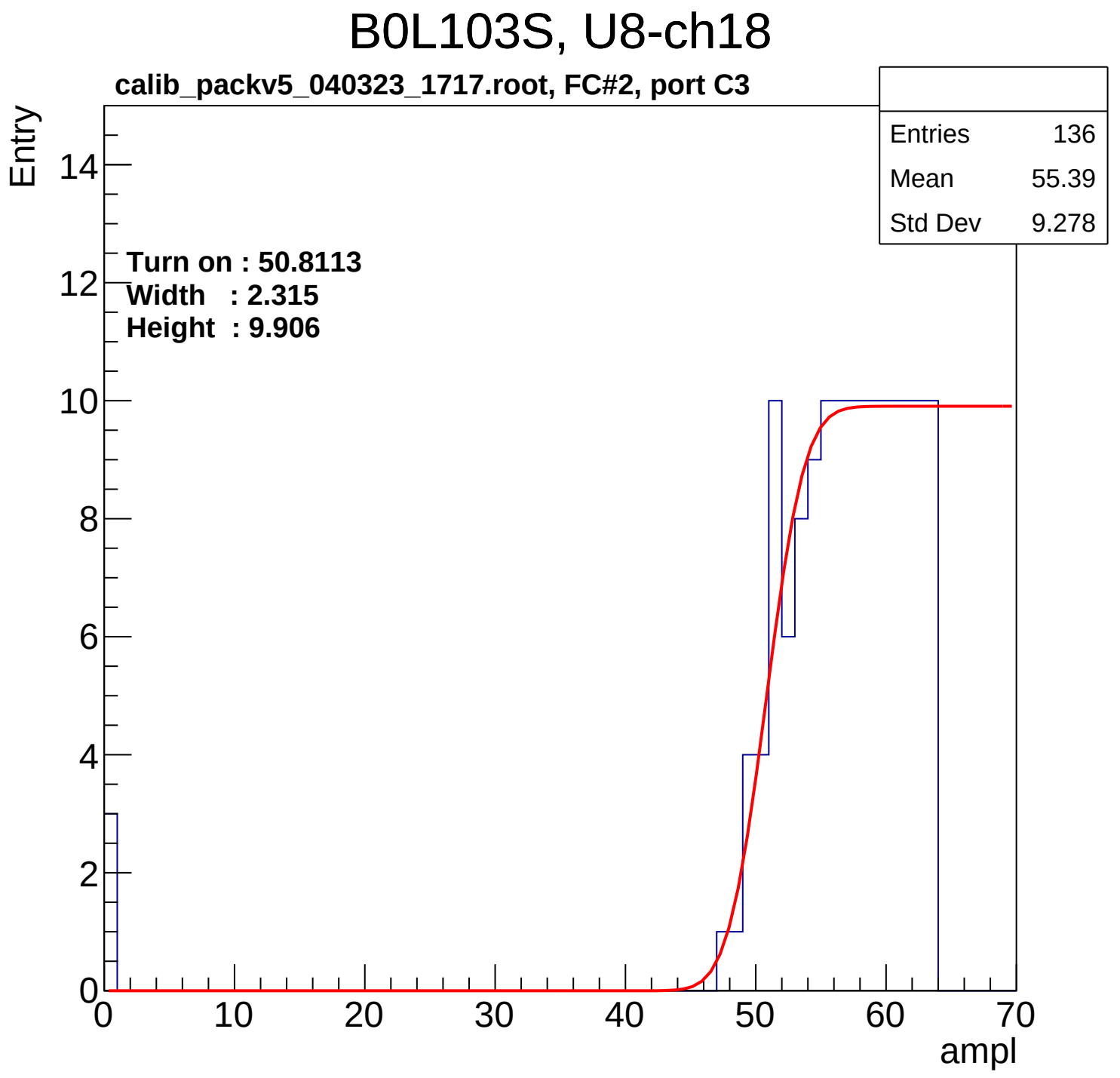
B0L103S, U8-ch18
calib_packv5_040323_1717.root, FC#2, port C3
Entries 136
Mean 55.39
Std Dev 9.278
Turn on : 50.8113
Width : 2.315
Height : 9.906
Entry
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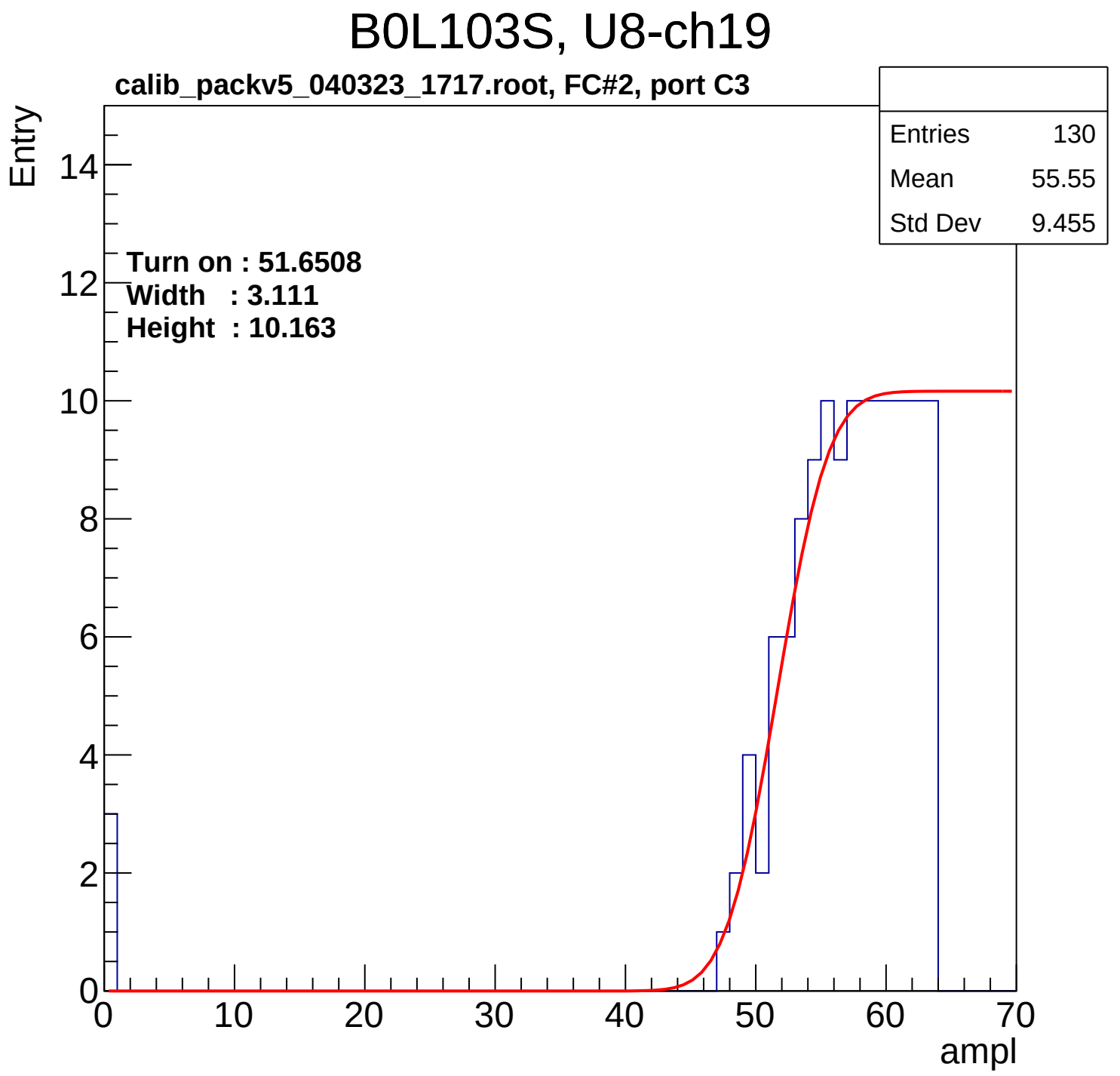
B0L103S, U8-ch19
calib_packv5_040323_1717.root, FC#2, port C3
Entries 130
Mean 55.55
Std Dev 9.455
Turn on : 51.6508
Width : 3.111
Height : 10.163
Entry
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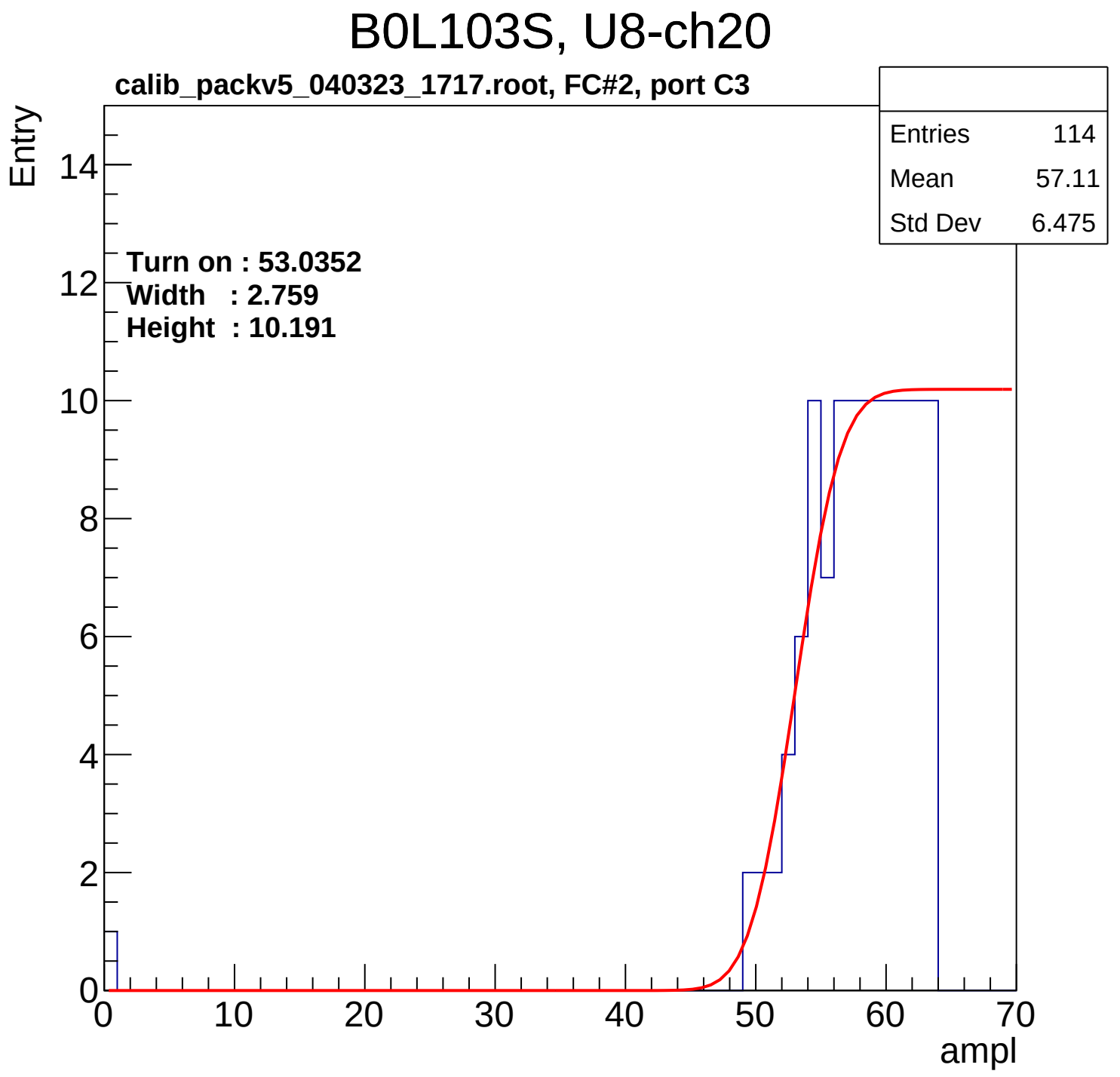
B0L103S, U8-ch20
calib_packv5_040323_1717.root, FC#2, port C3
Entries 114
Mean 57.11
Std Dev 6.475
Turn on : 53.0352
Width : 2.759
Height : 10.191
Entry
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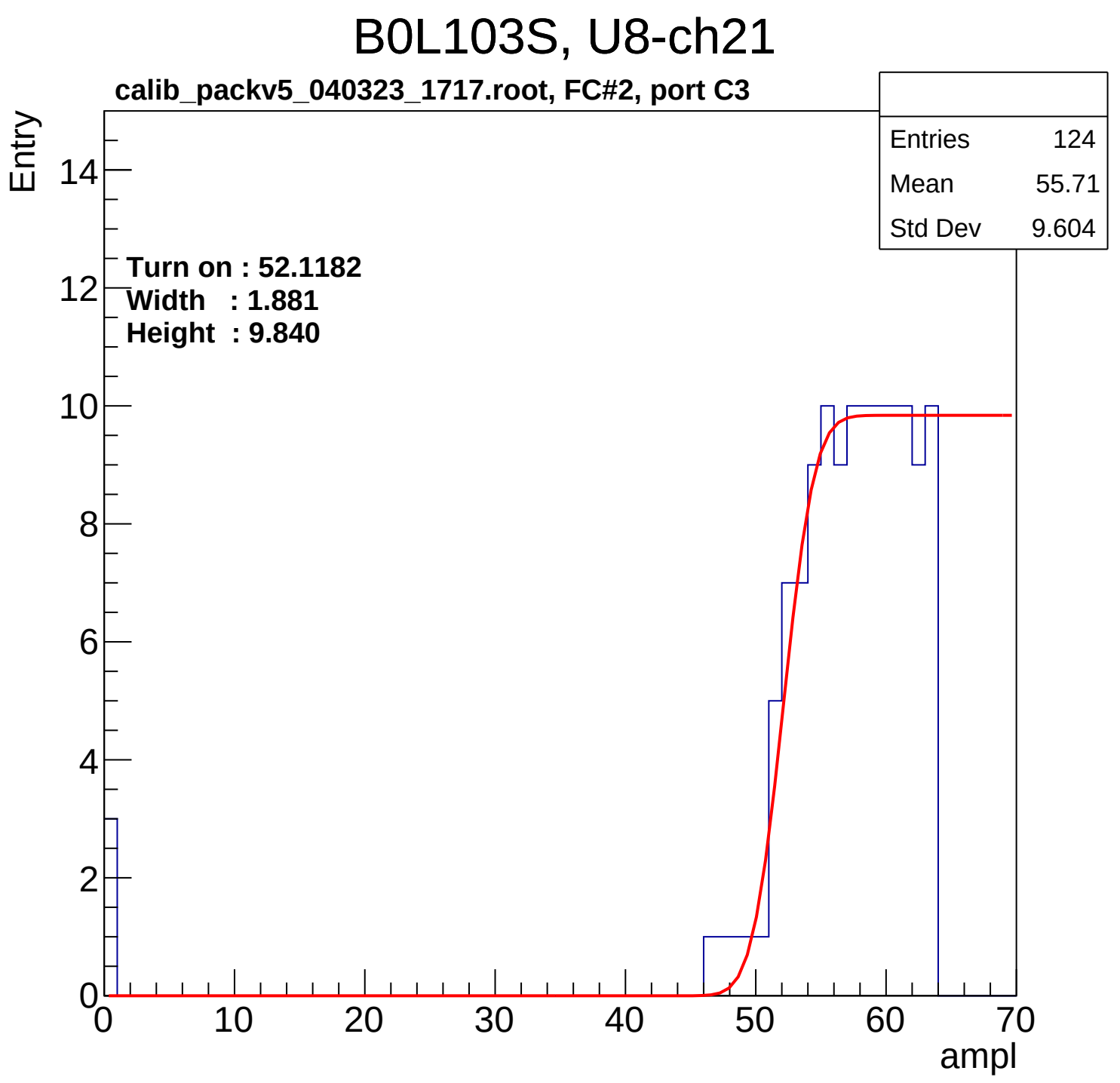
B0L103S, U8-ch21
calib_packv5_040323_1717.root, FC#2, port C3
Entries 124
Mean 55.71
Std Dev 9.604
Turn on : 52.1182
Width : 1.881
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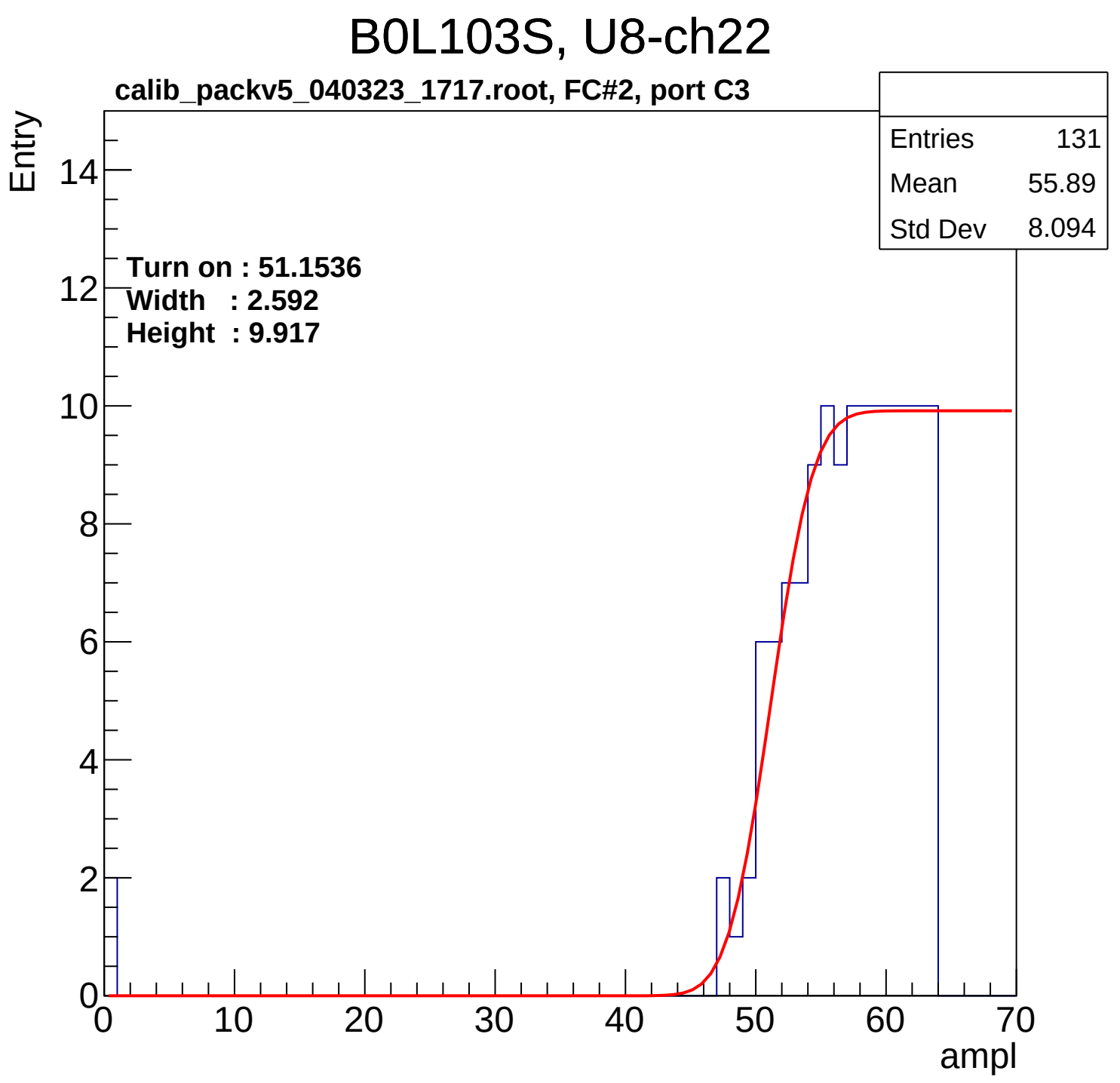
B0L103S, U8-ch22
calib_packv5_040323_1717.root, FC#2, port C3
Entries 131
Mean 55.89
Std Dev 8.094
Turn on : 51.1536
Width : 2.592
Height : 9.917
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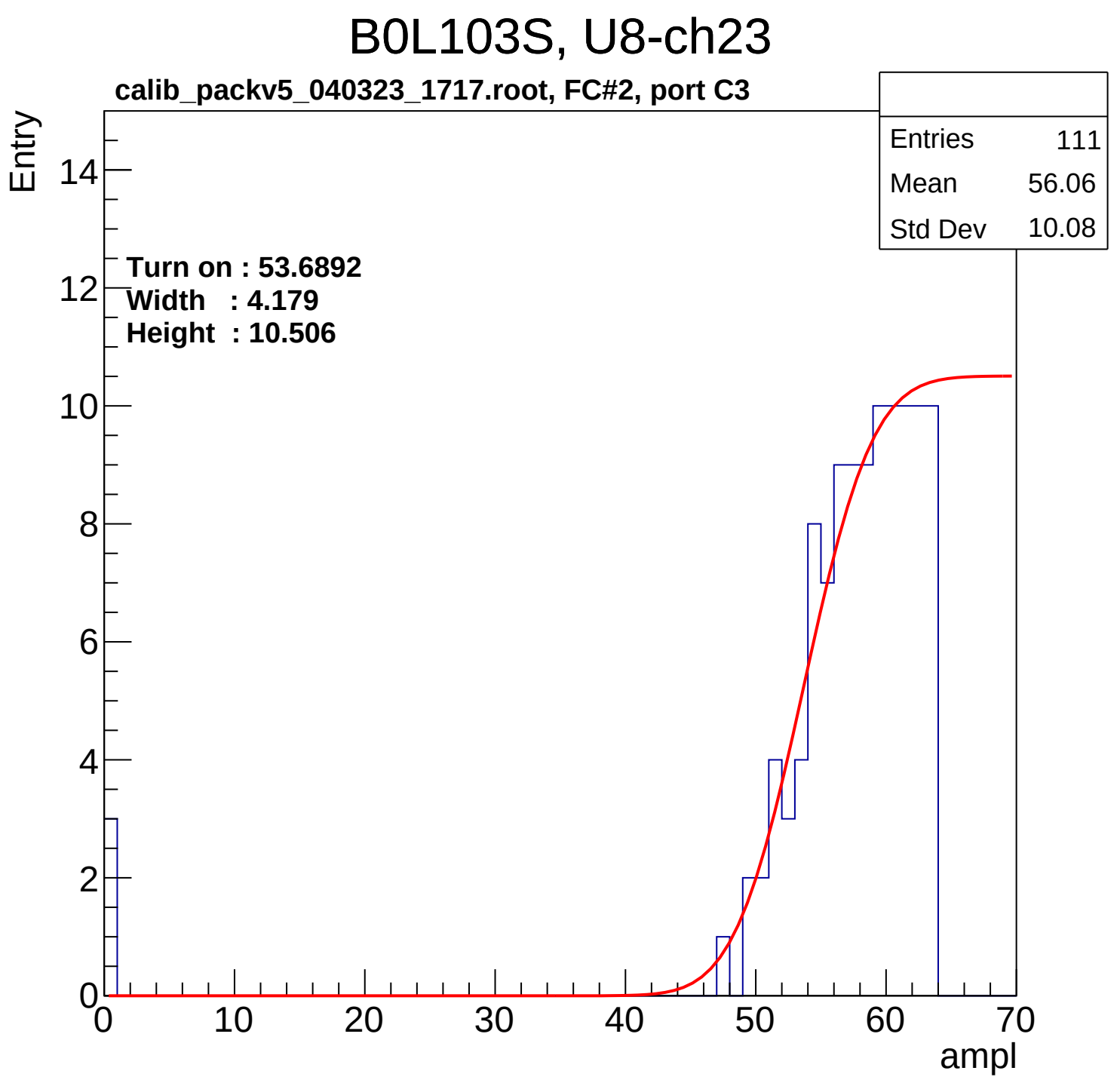
B0L103S, U8-ch23
calib_packv5_040323_1717.root, FC#2, port C3
Entries 111
Mean 56.06
Std Dev 10.08
Turn on : 53.6892
Width : 4.179
Height : 10.506
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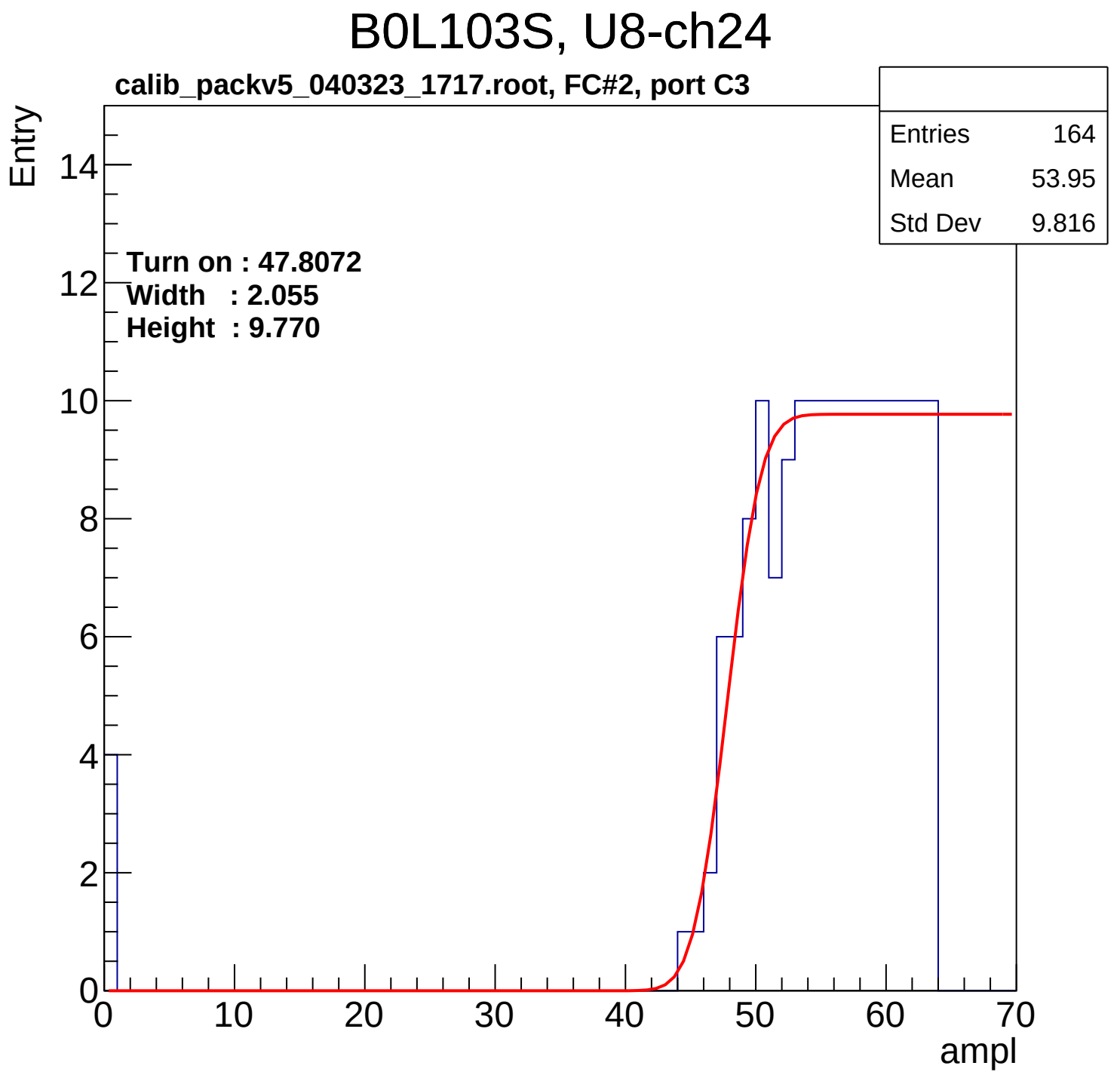
B0L103S, U8-ch24
calib_packv5_040323_1717.root, FC#2, port C3
Entries 164
Mean 53.95
Std Dev 9.816
Turn on : 47.8072
Width : 2.055
Height : 9.770
Entry
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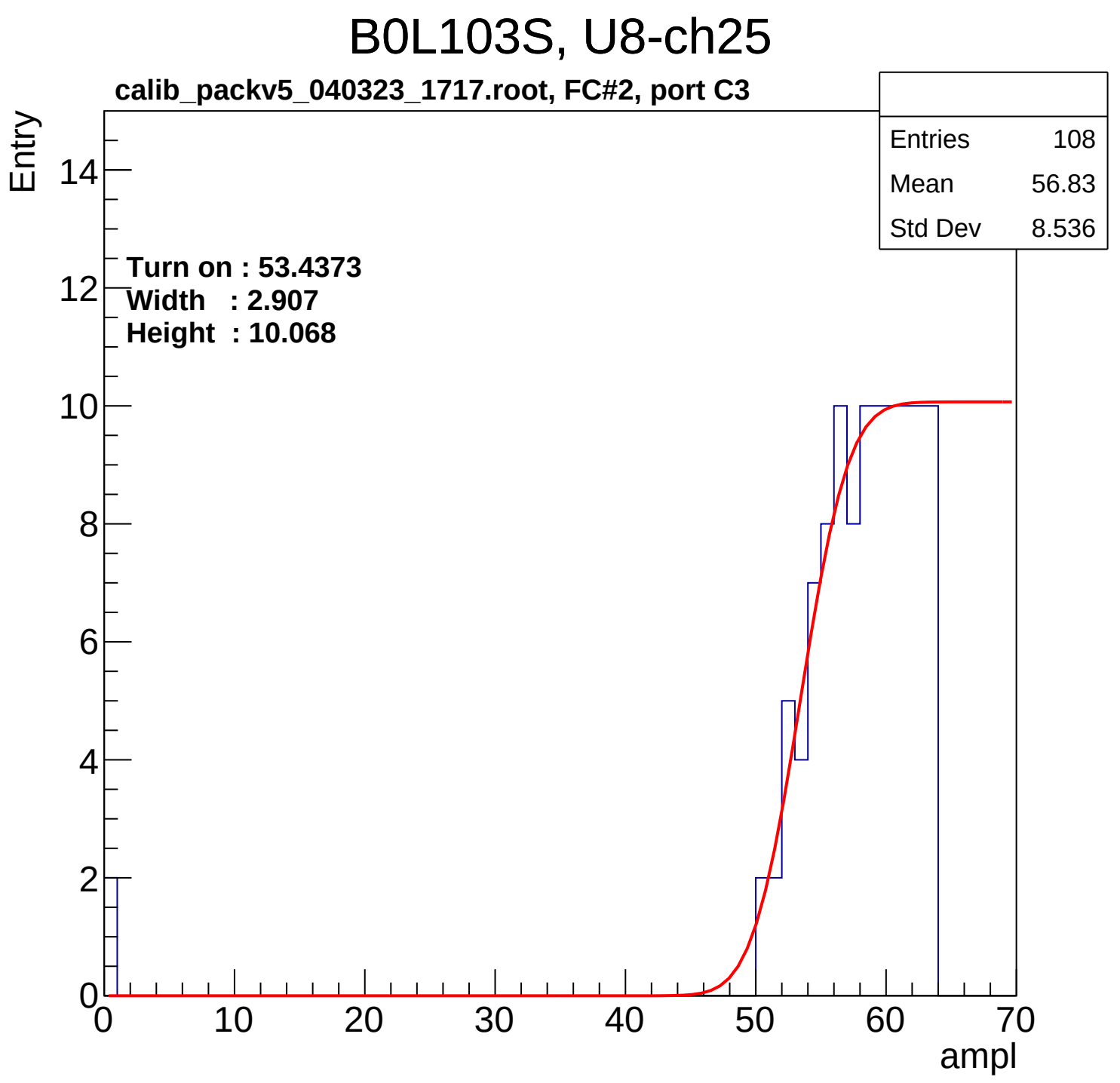
B0L103S, U8-ch25
calib_packv5_040323_1717.root, FC#2, port C3
Entries 108
Mean 56.83
Std Dev 8.536
Turn on : 53.4373
Width : 2.907
Height : 10.068
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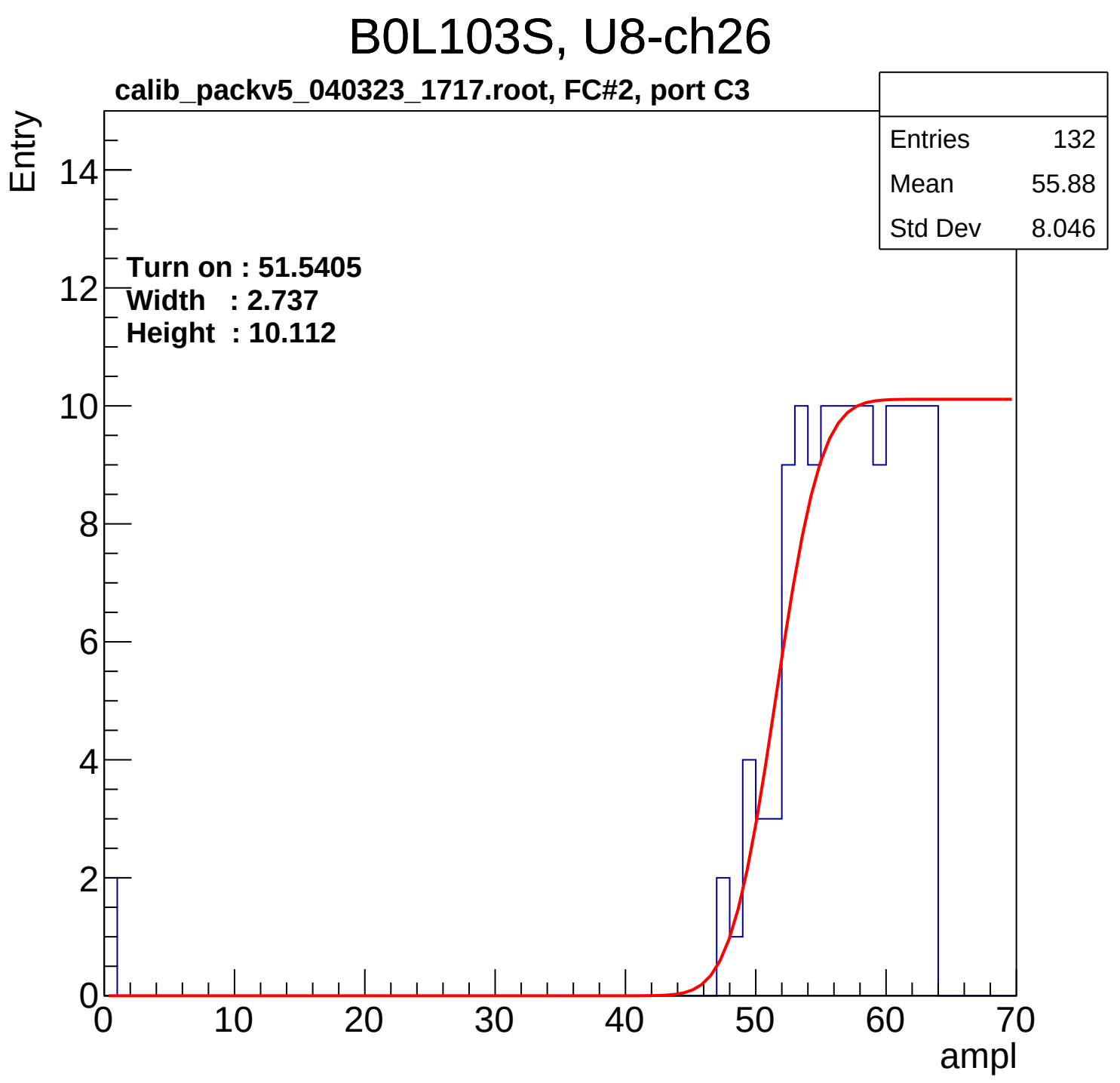
B0L103S, U8-ch26
calib_packv5_040323_1717.root, FC#2, port C3
Entries 132
Mean 55.88
Std Dev 8.046
Turn on : 51.5405
Width : 2.737
Height : 10.112
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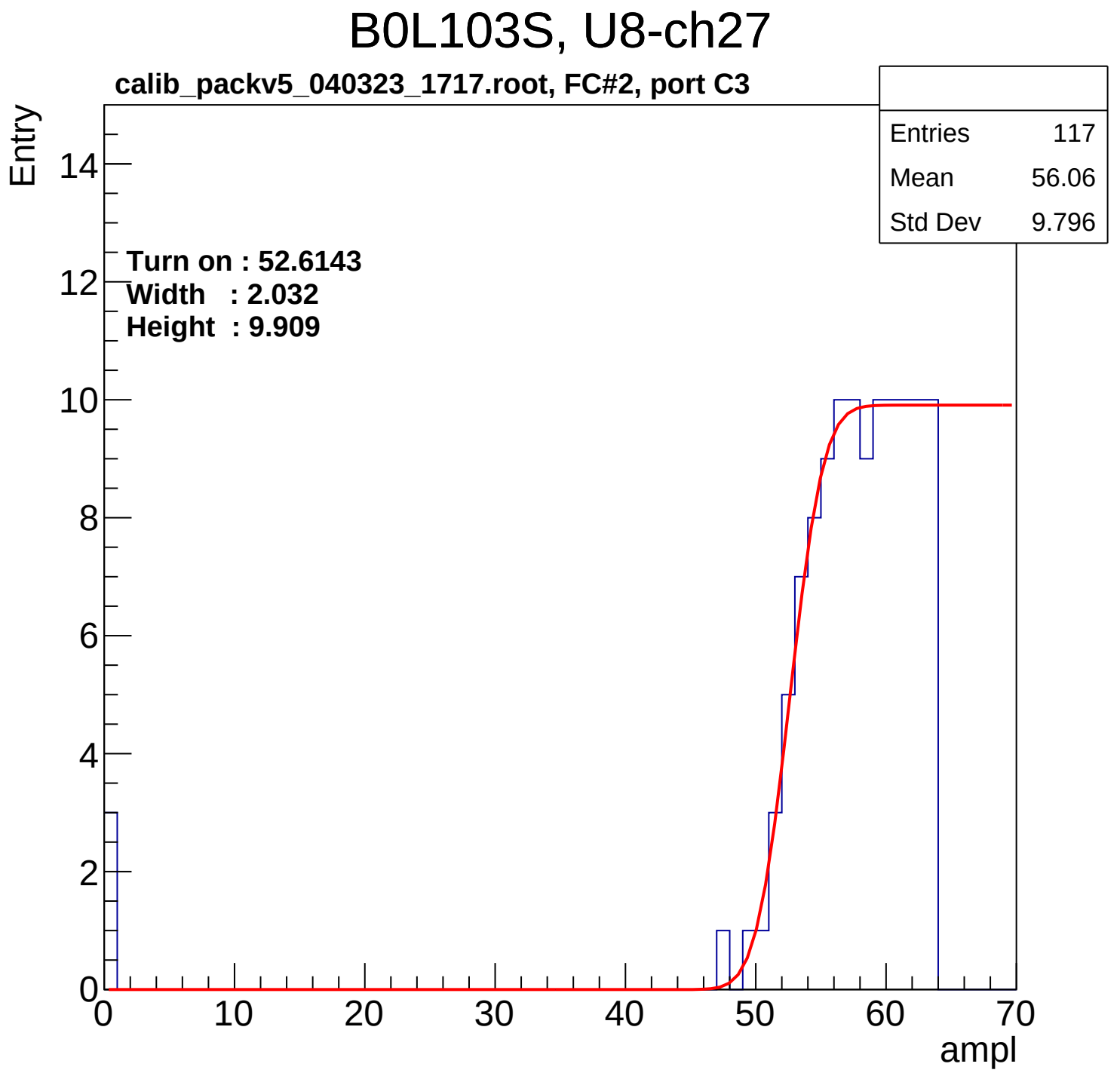
B0L103S, U8-ch27
calib_packv5_040323_1717.root, FC#2, port C3
Entries 117
Mean 56.06
Std Dev 9.796
Turn on : 52.6143
Width : 2.032
Height : 9.909
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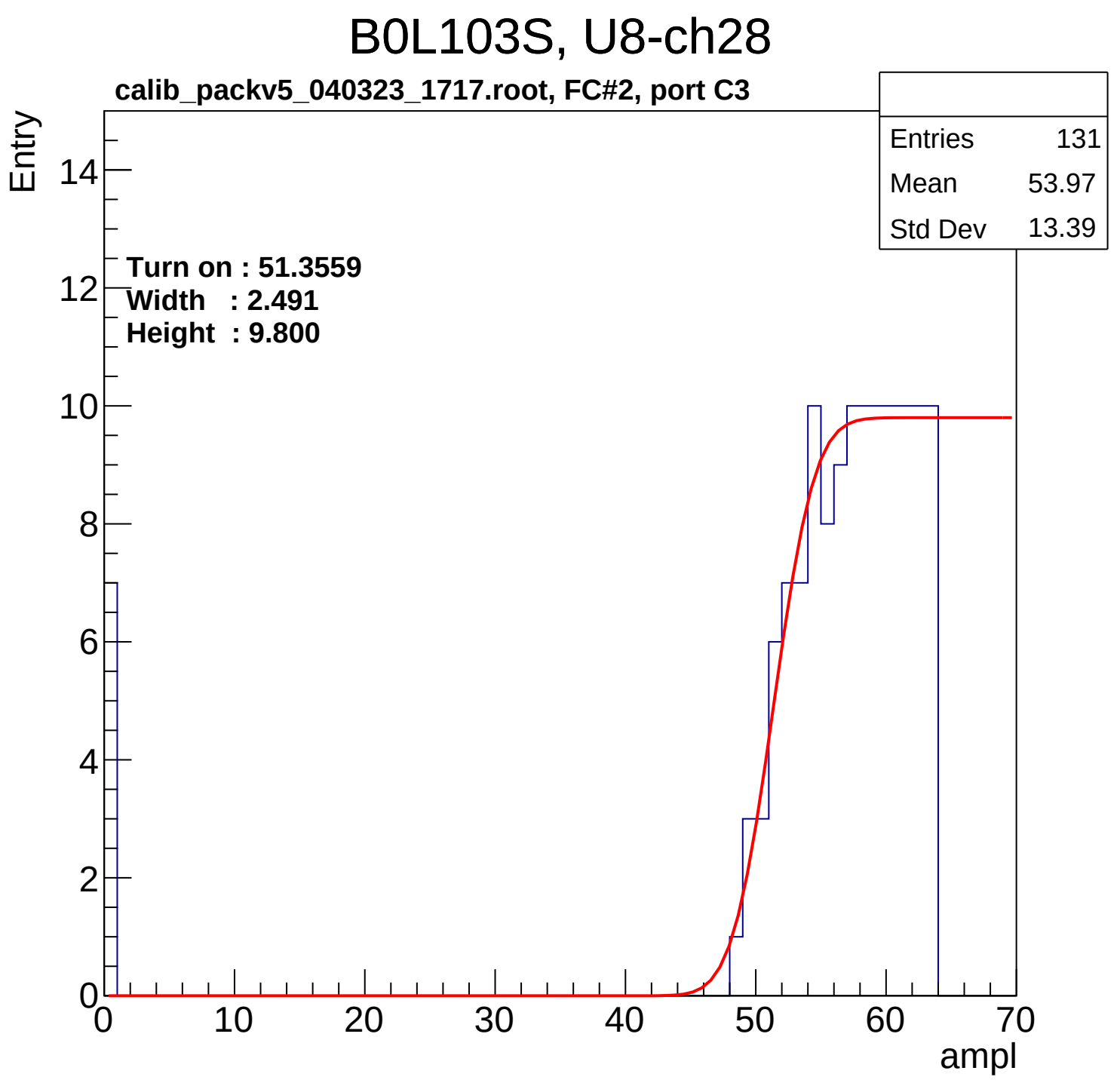
B0L103S, U8-ch28
calib_packv5_040323_1717.root, FC#2, port C3
Entries 131
Mean 53.97
Std Dev 13.39
Turn on : 51.3559
Width : 2.491
Height : 9.800
Entry
ampl
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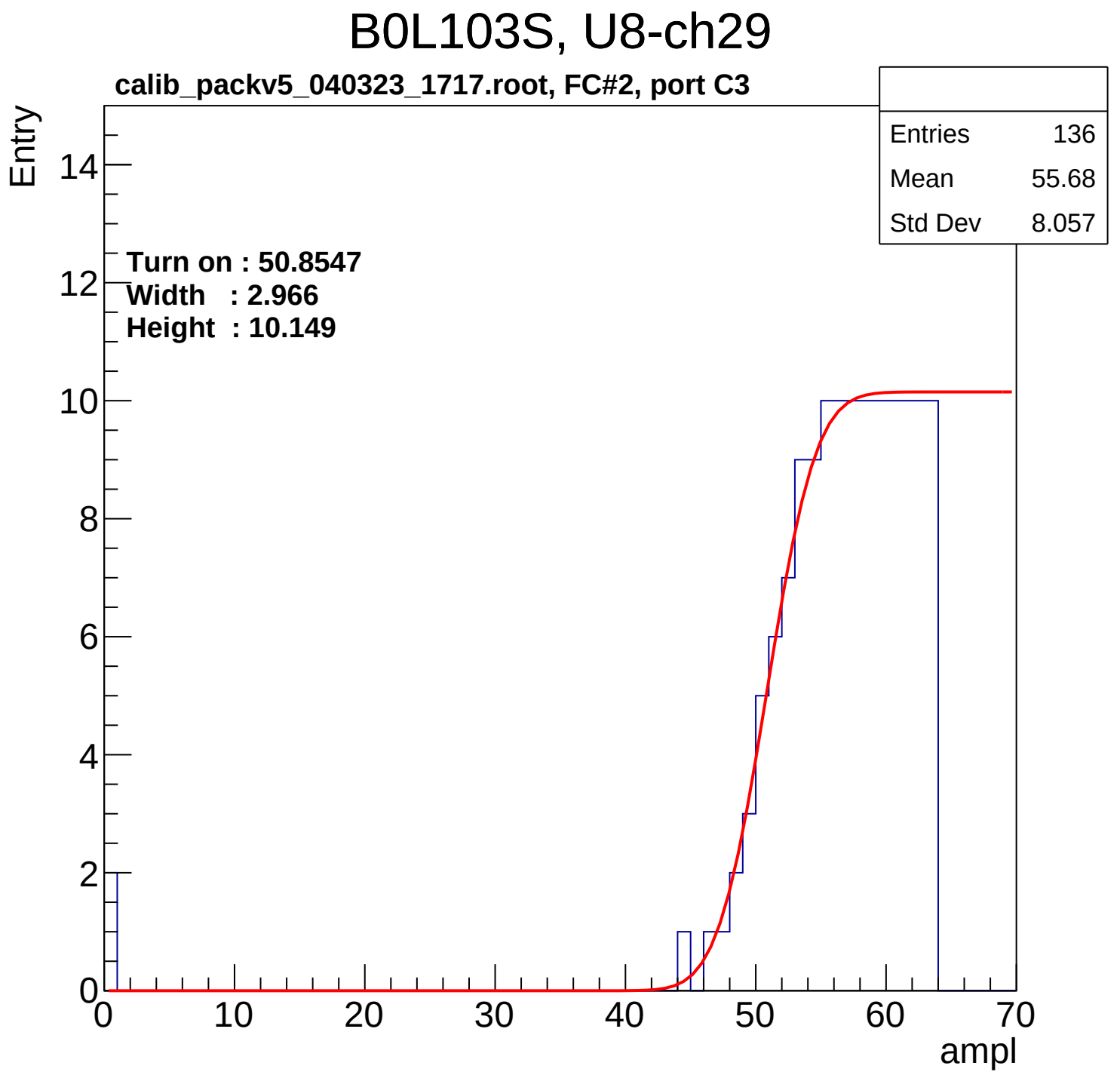
B0L103S, U8-ch29
calib_packv5_040323_1717.root, FC#2, port C3
Entries 136
Mean 55.68
Std Dev 8.057
Turn on : 50.8547
Width : 2.966
Height : 10.149
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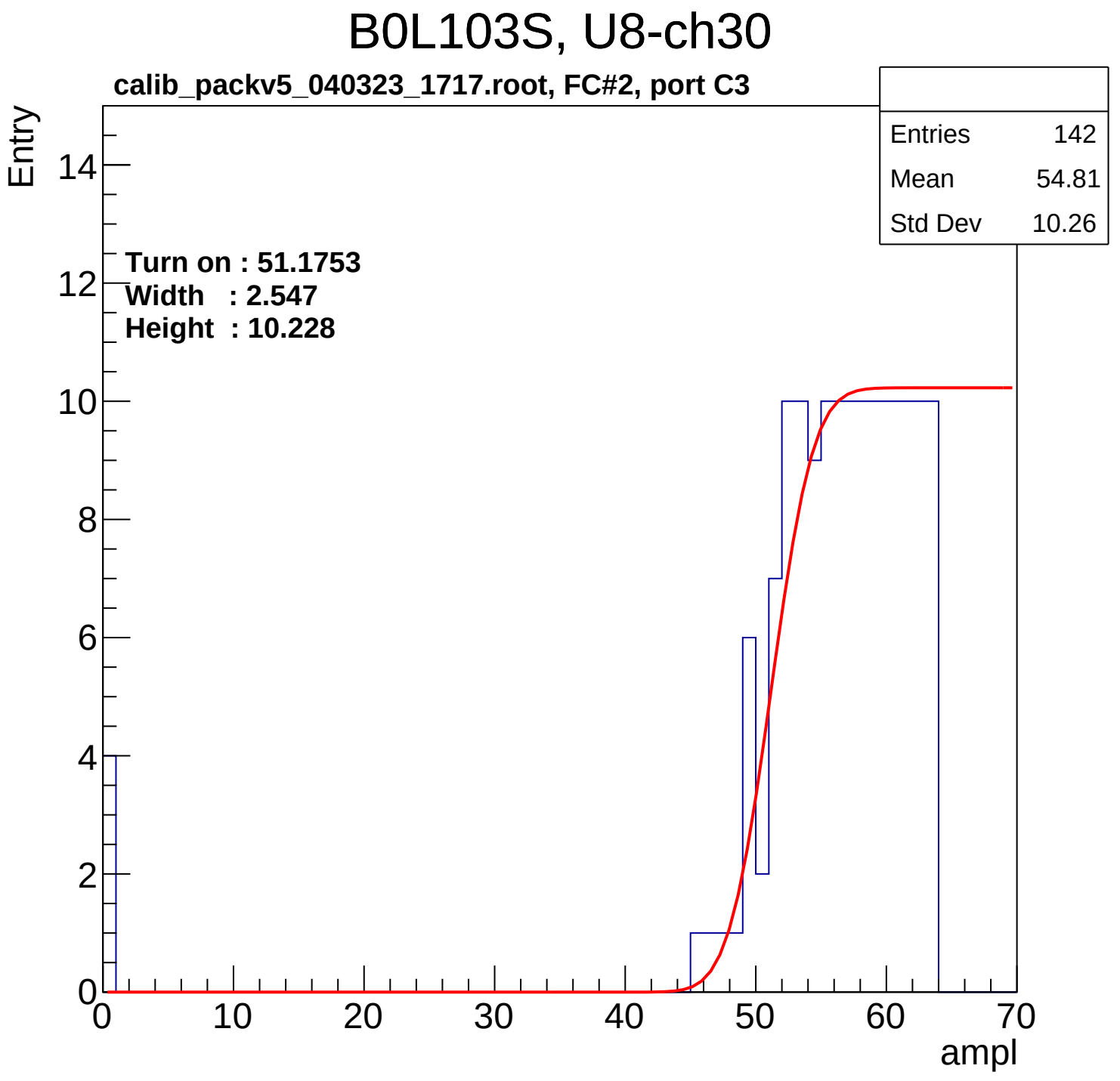
B0L103S, U8-ch30
calib_packv5_040323_1717.root, FC#2, port C3
Entries 142
Mean 54.81
Std Dev 10.26
Turn on : 51.1753
Width : 2.547
Height : 10.228
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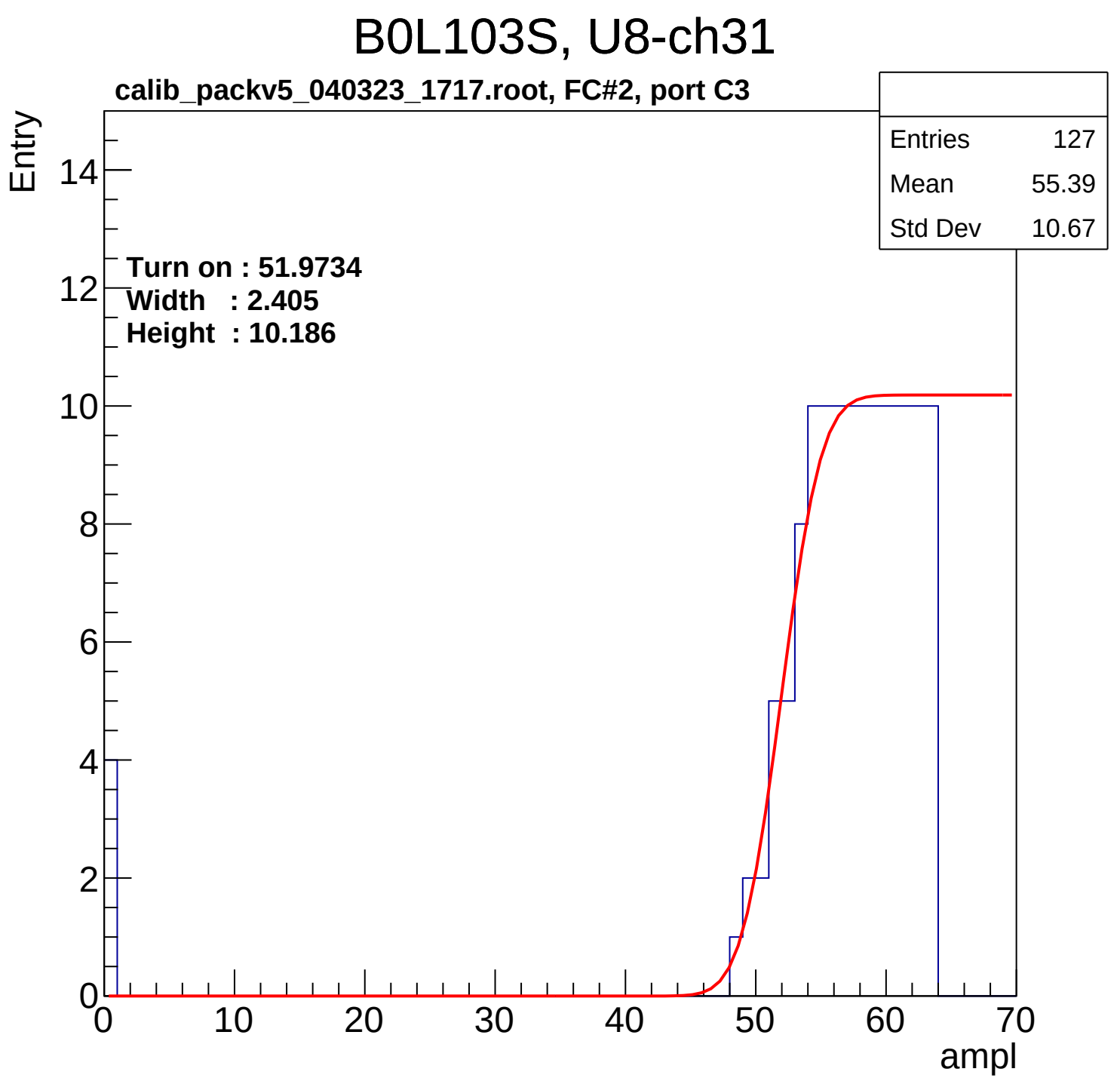
B0L103S, U8-ch31
calib_packv5_040323_1717.root, FC#2, port C3
Entries 127
Mean 55.39
Std Dev 10.67
Turn on : 51.9734
Width : 2.405
Height : 10.186
Entry
ampl
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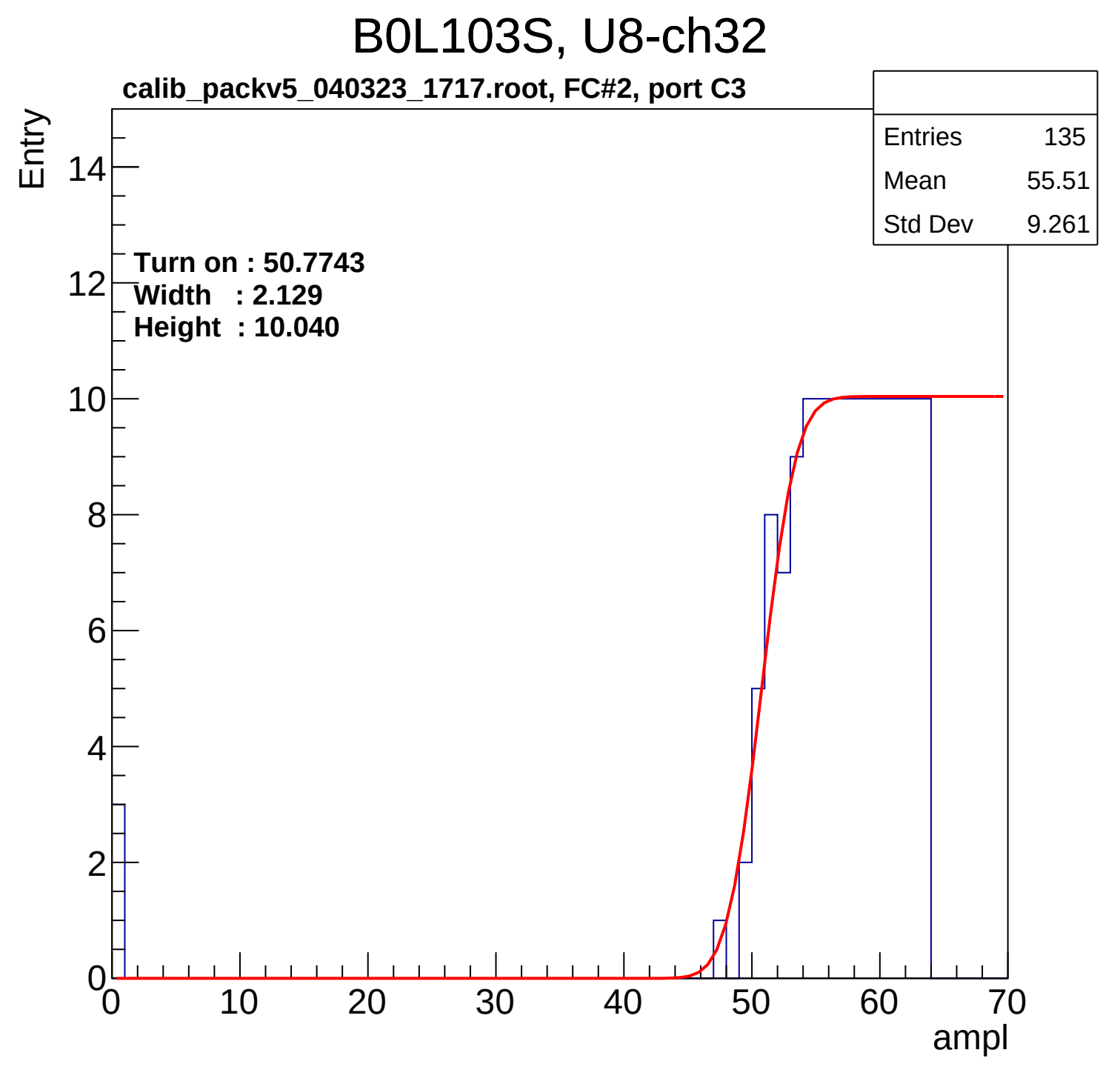
B0L103S, U8-ch32
calib_packv5_040323_1717.root, FC#2, port C3
Entries 135
Mean 55.51
Std Dev 9.261
Turn on : 50.7743
Width : 2.129
Height : 10.040
Entry
ampl
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8
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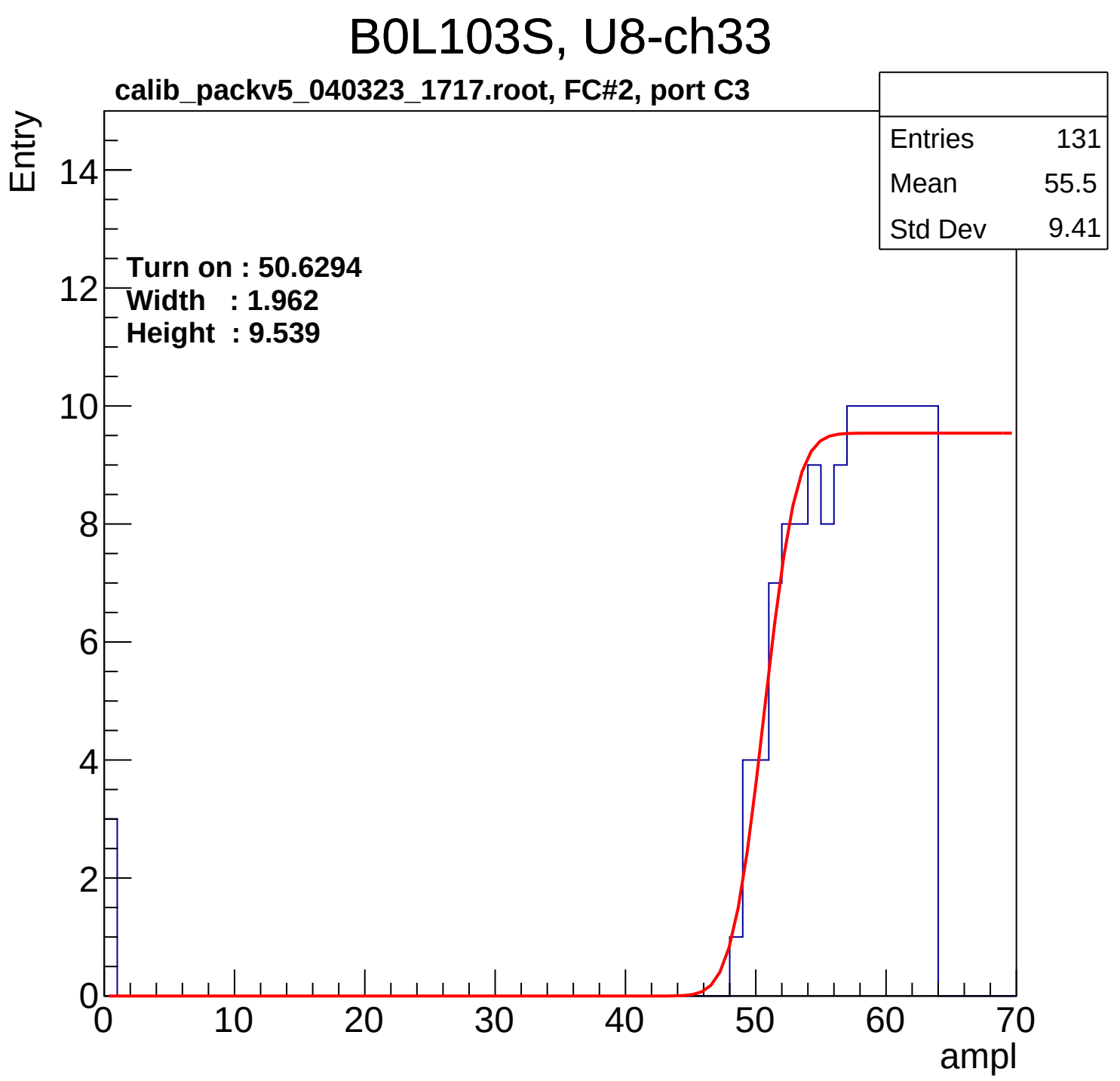
B0L103S, U8-ch33
calib_packv5_040323_1717.root, FC#2, port C3
Entries 131
Mean 55.5
Std Dev 9.41
Turn on : 50.6294
Width : 1.962
Height : 9.539
Entry
ampl
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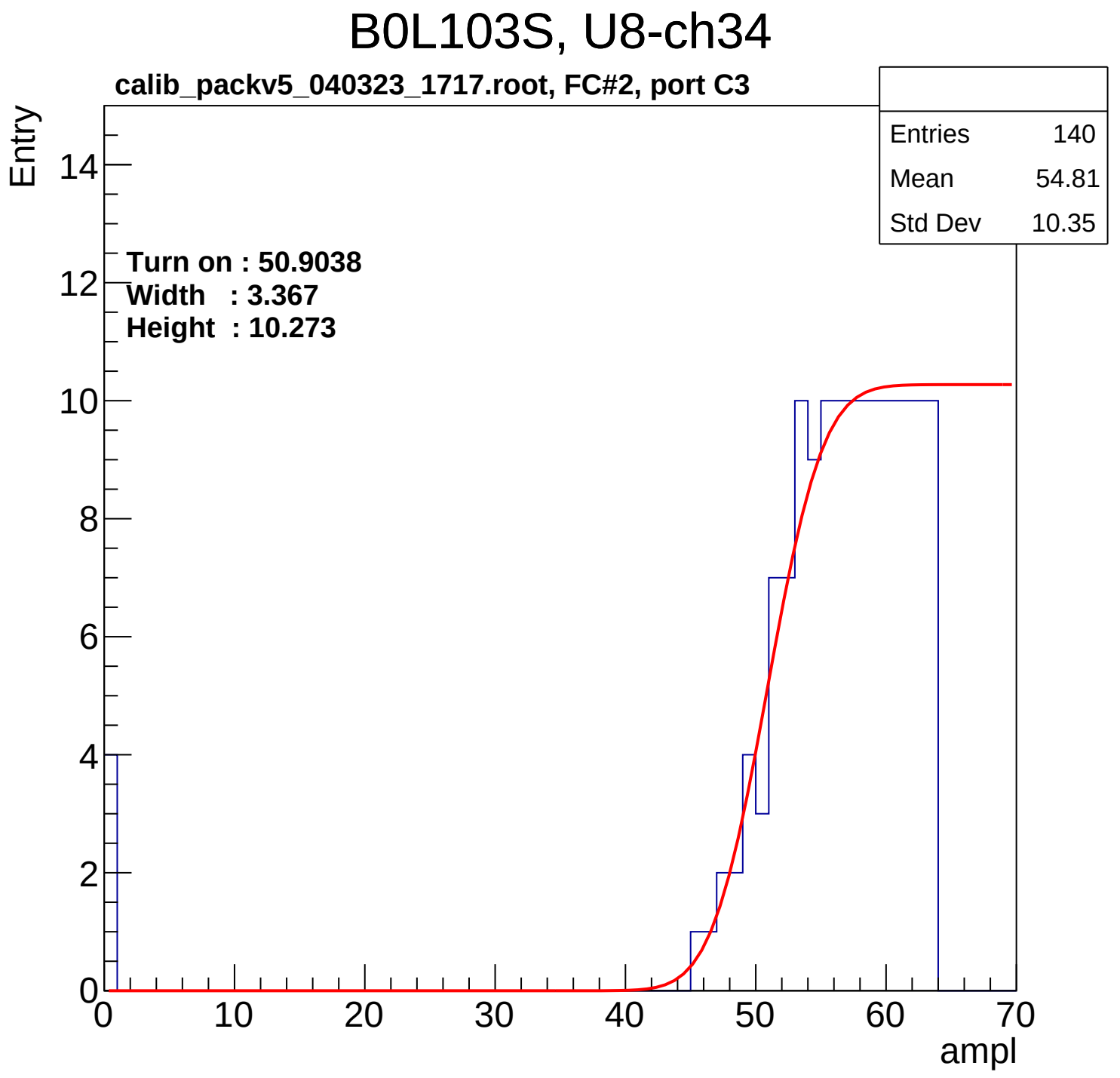
B0L103S, U8-ch34
calib_packv5_040323_1717.root, FC#2, port C3
Entries 140
Mean 54.81
Std Dev 10.35
Turn on : 50.9038
Width : 3.367
Height : 10.273
Entry
ampl
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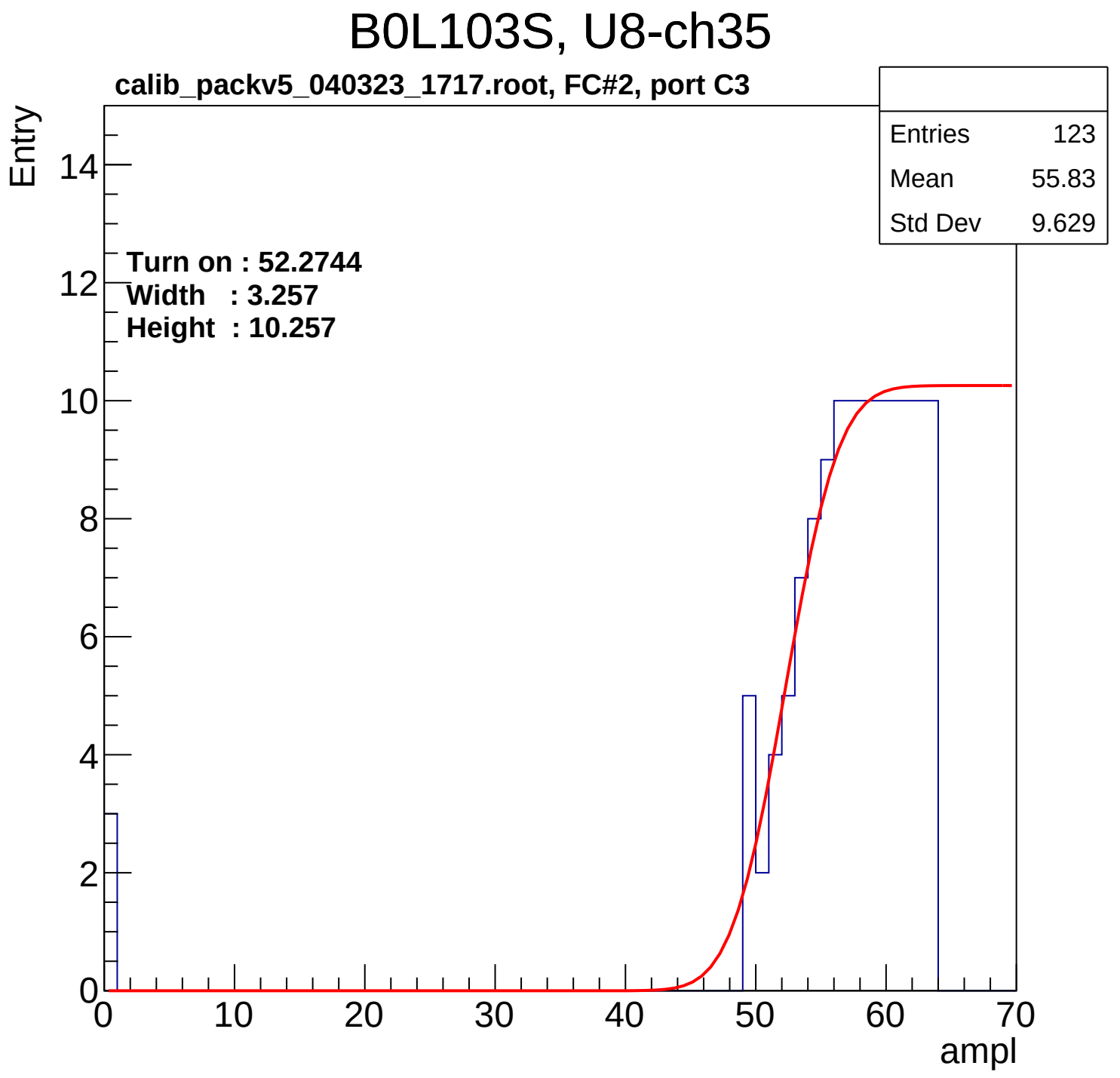
B0L103S, U8-ch35
calib_packv5_040323_1717.root, FC#2, port C3
Entries 123
Mean 55.83
Std Dev 9.629
Turn on : 52.2744
Width : 3.257
Height : 10.257
Entry
ampl
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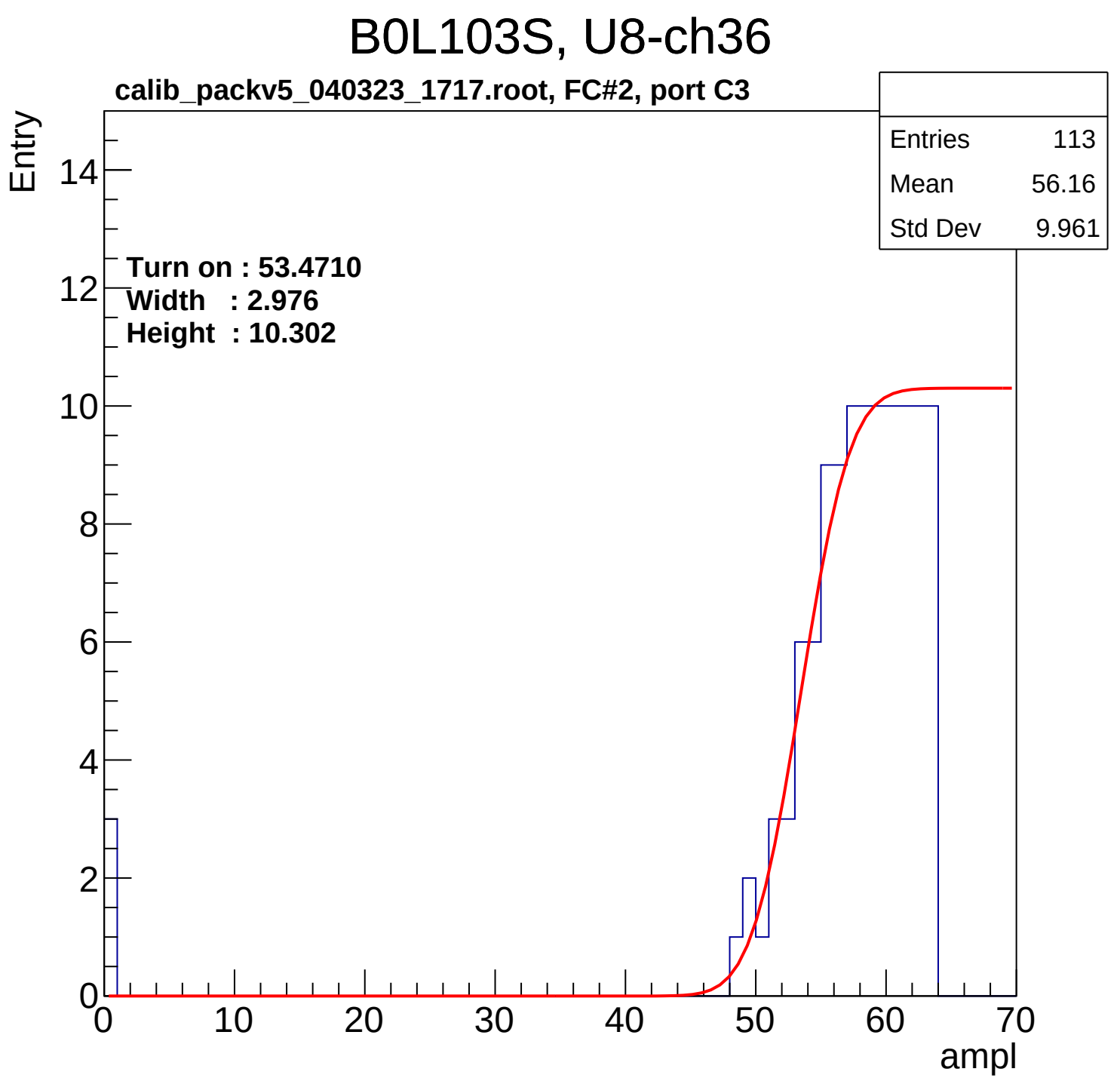
B0L103S, U8-ch36
calib_packv5_040323_1717.root, FC#2, port C3
Entries 113
Mean 56.16
Std Dev 9.961
Turn on : 53.4710
Width : 2.976
Height : 10.302
Entry
ampl
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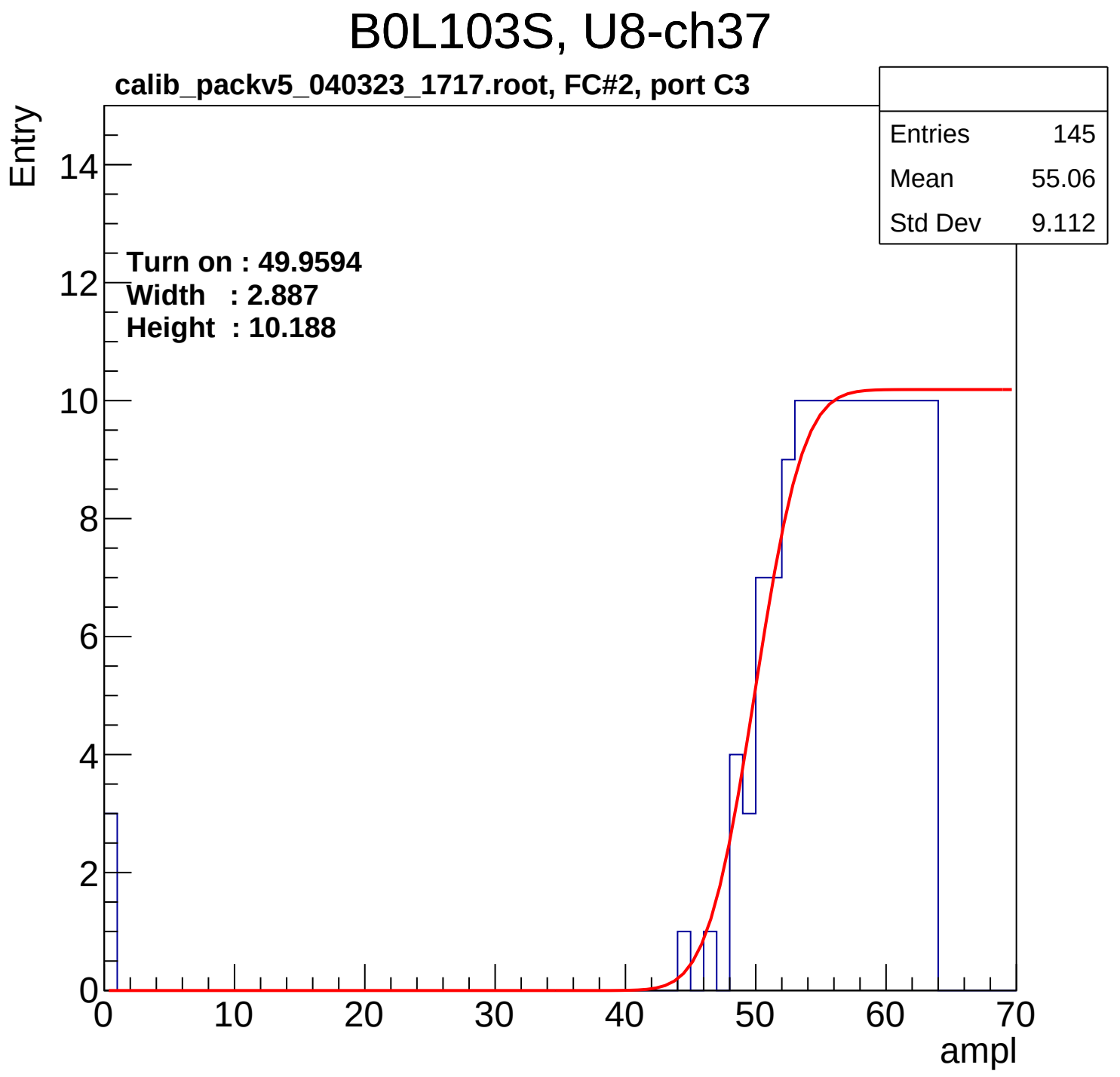
B0L103S, U8-ch37
calib_packv5_040323_1717.root, FC#2, port C3
Entries 145
Mean 55.06
Std Dev 9.112
Turn on : 49.9594
Width : 2.887
Height : 10.188
Entry
ampl
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8
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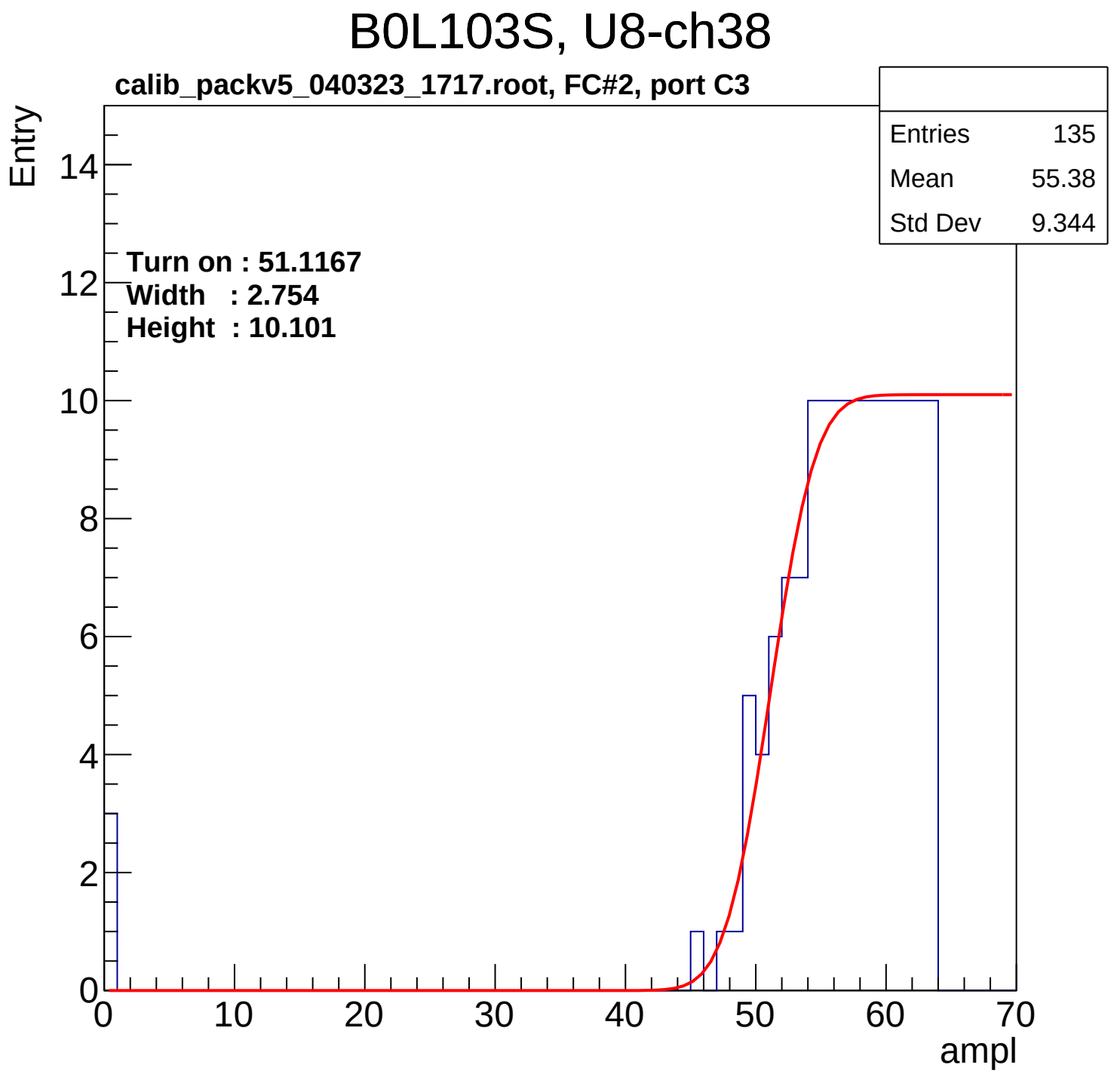
B0L103S, U8-ch38
calib_packv5_040323_1717.root, FC#2, port C3
Entries 135
Mean 55.38
Std Dev 9.344
Turn on : 51.1167
Width : 2.754
Height : 10.101
Entry
ampl
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6
8
10
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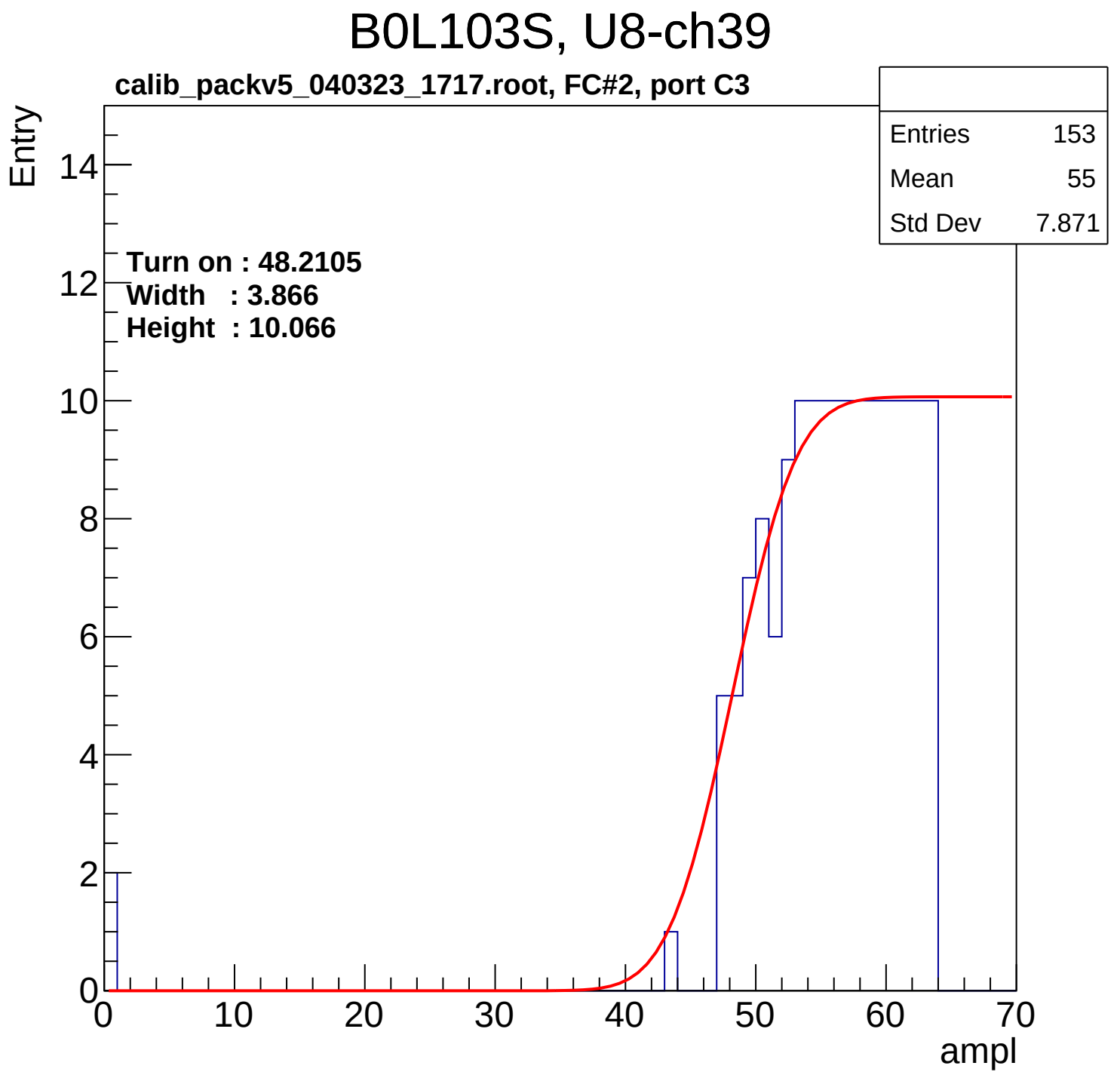
B0L103S, U8-ch39
calib_packv5_040323_1717.root, FC#2, port C3
Entries 153
Mean 55
Std Dev 7.871
Turn on : 48.2105
Width : 3.866
Height : 10.066
Entry
ampl
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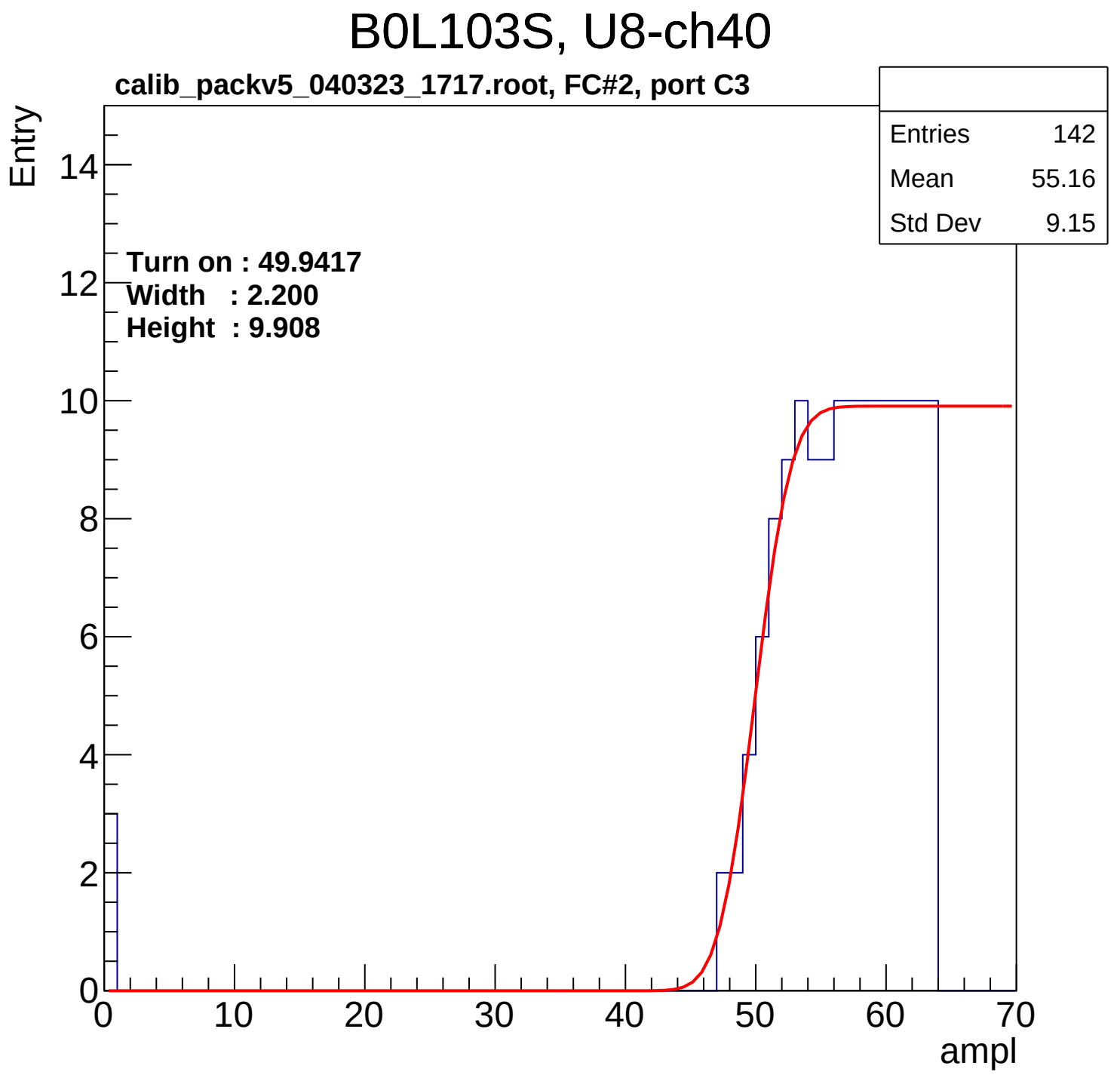
B0L103S, U8-ch40
calib_packv5_040323_1717.root, FC#2, port C3
Entries 142
Mean 55.16
Std Dev 9.15
Turn on : 49.9417
Width : 2.200
Height : 9.908
Entry
ampl
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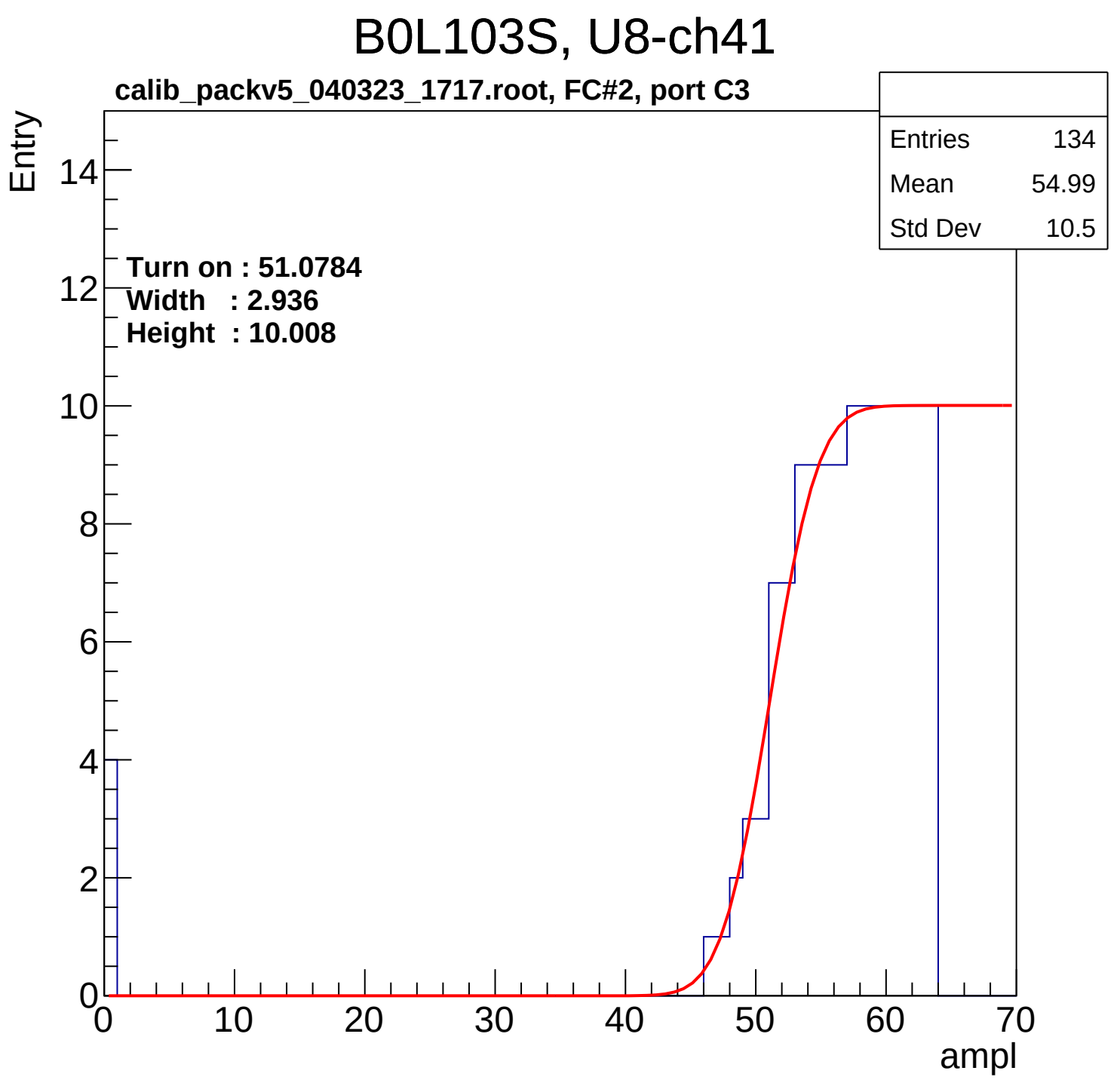
B0L103S, U8-ch41
calib_packv5_040323_1717.root, FC#2, port C3
Entries 134
Mean 54.99
Std Dev 10.5
Turn on : 51.0784
Width : 2.936
Height : 10.008
Entry
ampl
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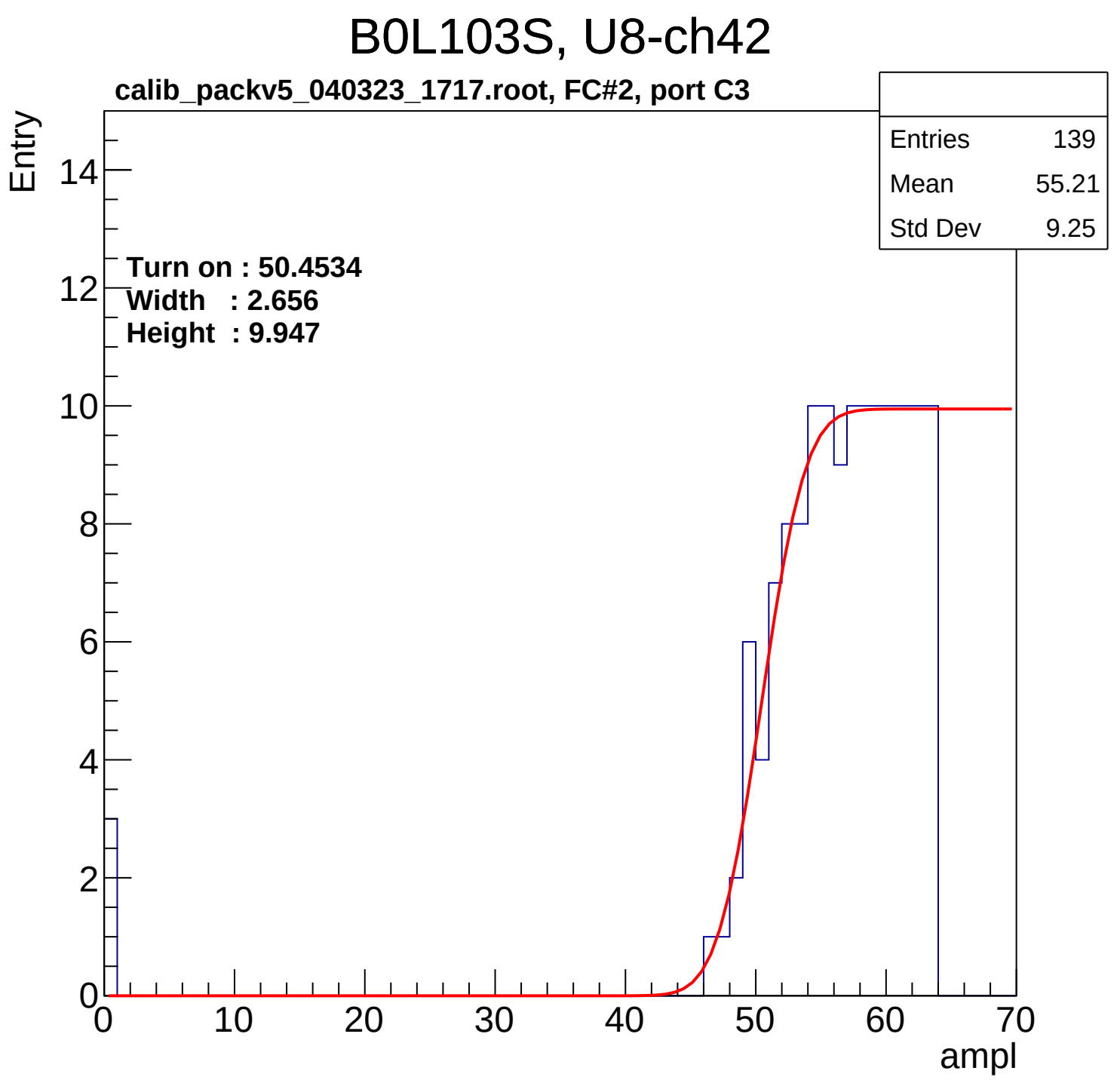
B0L103S, U8-ch42
calib_packv5_040323_1717.root, FC#2, port C3
Entries 139
Mean 55.21
Std Dev 9.25
Turn on : 50.4534
Width : 2.656
Height : 9.947
Entry
ampl
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6
8
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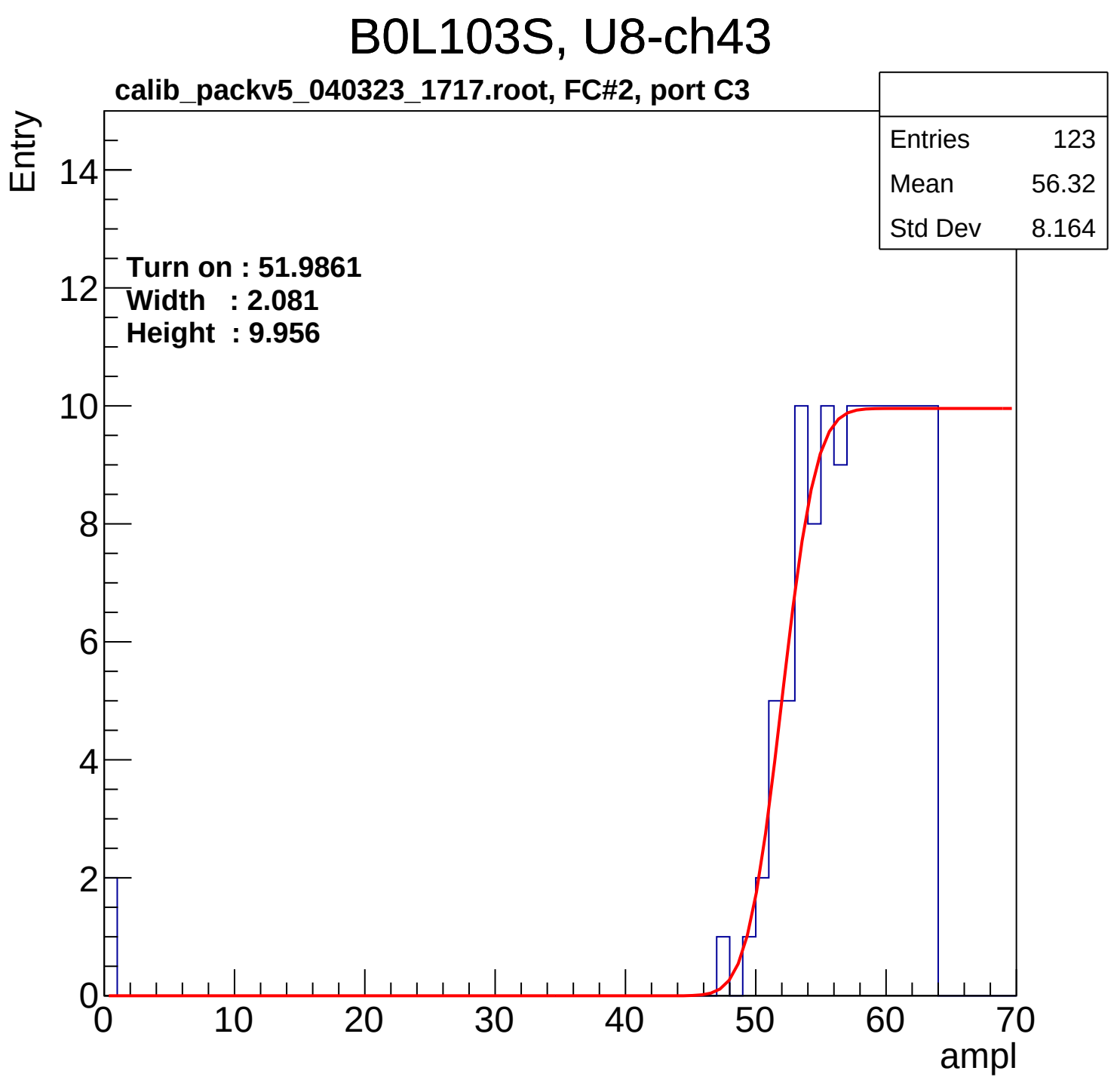
B0L103S, U8-ch43
calib_packv5_040323_1717.root, FC#2, port C3
Entries 123
Mean 56.32
Std Dev 8.164
Turn on : 51.9861
Width : 2.081
Height : 9.956
Entry
ampl
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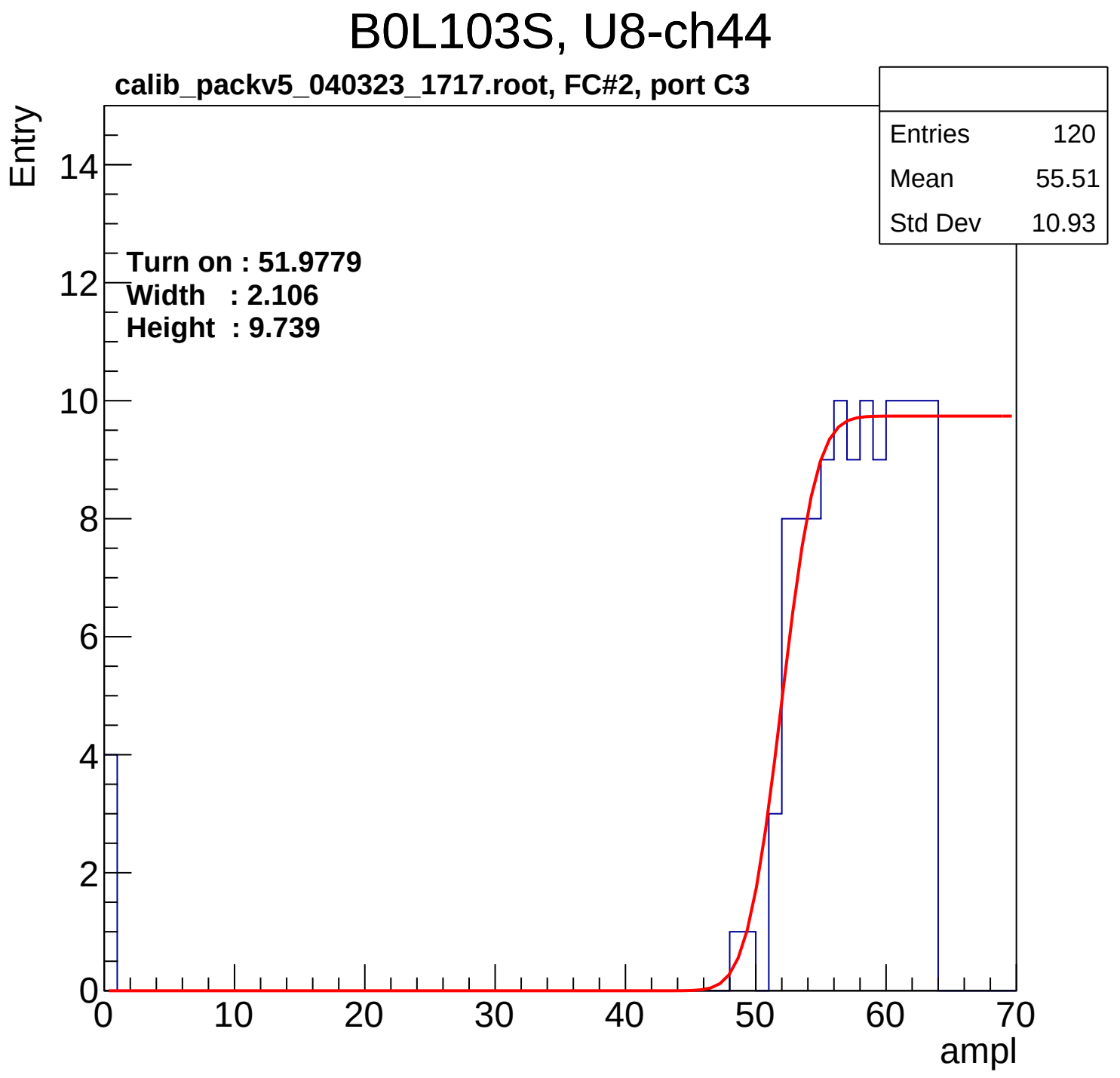
B0L103S, U8-ch44
calib_packv5_040323_1717.root, FC#2, port C3
Entries 120
Mean 55.51
Std Dev 10.93
Turn on : 51.9779
Width : 2.106
Height : 9.739
Entry
ampl
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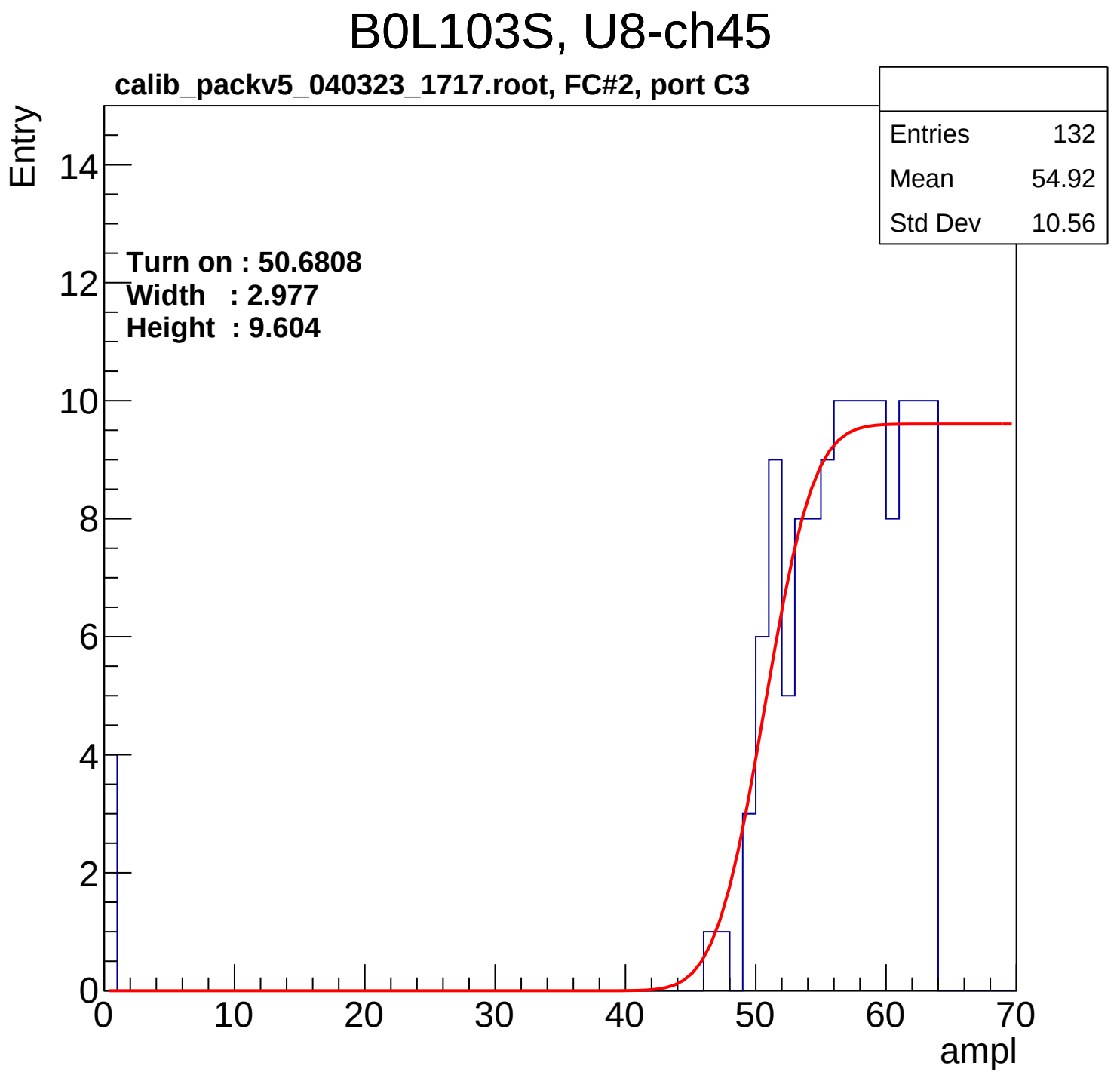
B0L103S, U8-ch45
calib_packv5_040323_1717.root, FC#2, port C3
Entries 132
Mean 54.92
Std Dev 10.56
Turn on : 50.6808
Width : 2.977
Height : 9.604
Entry
ampl
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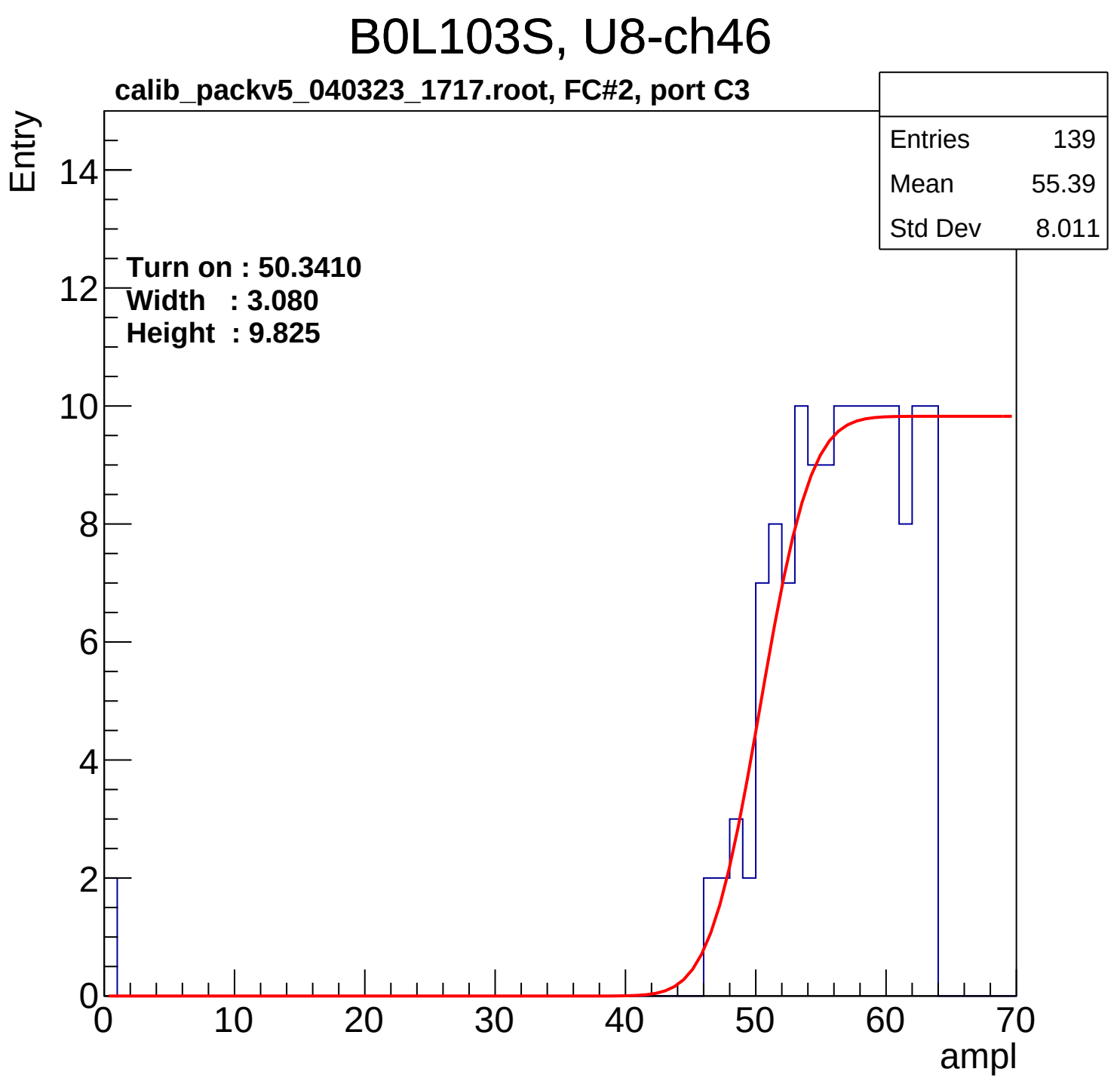
B0L103S, U8-ch46
calib_packv5_040323_1717.root, FC#2, port C3
Entries 139
Mean 55.39
Std Dev 8.011
Turn on : 50.3410
Width : 3.080
Height : 9.825
Entry
ampl
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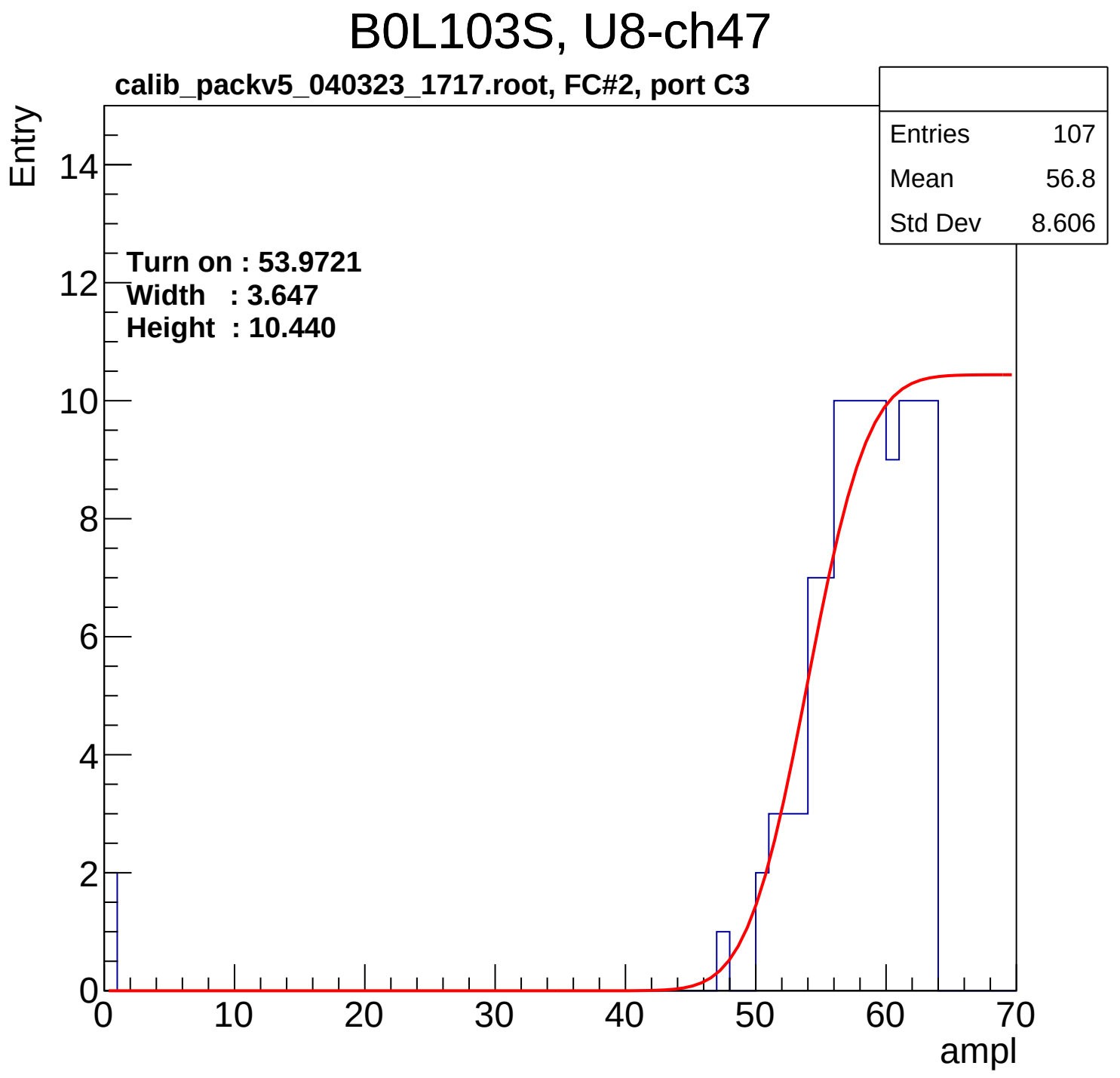
B0L103S, U8-ch47
calib_packv5_040323_1717.root, FC#2, port C3
Entries 107
Mean 56.8
Std Dev 8.606
Turn on : 53.9721
Width : 3.647
Height : 10.440
Entry
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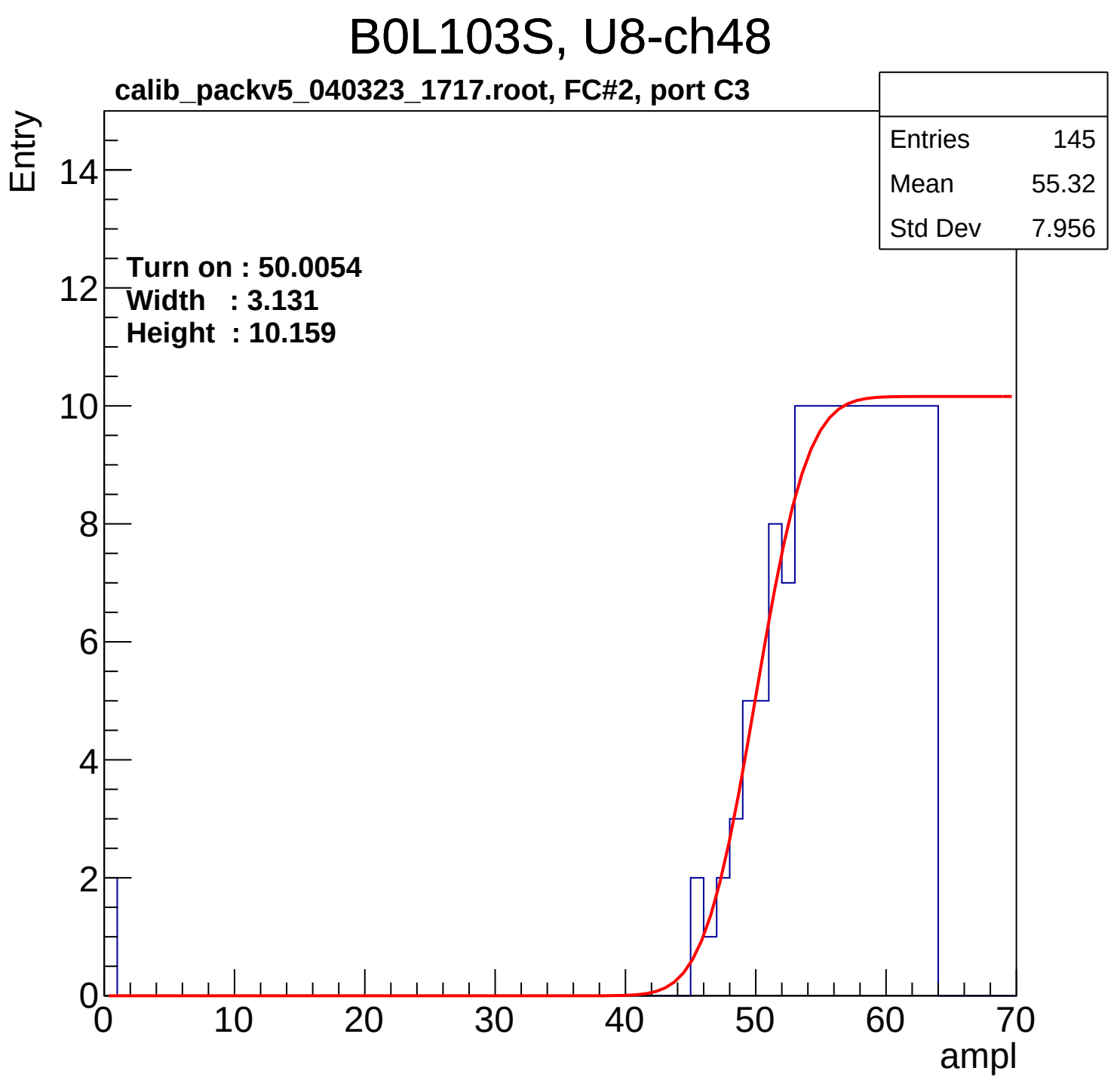
B0L103S, U8-ch48
calib_packv5_040323_1717.root, FC#2, port C3
Entries 145
Mean 55.32
Std Dev 7.956
Turn on : 50.0054
Width : 3.131
Height : 10.159
Entry
ampl
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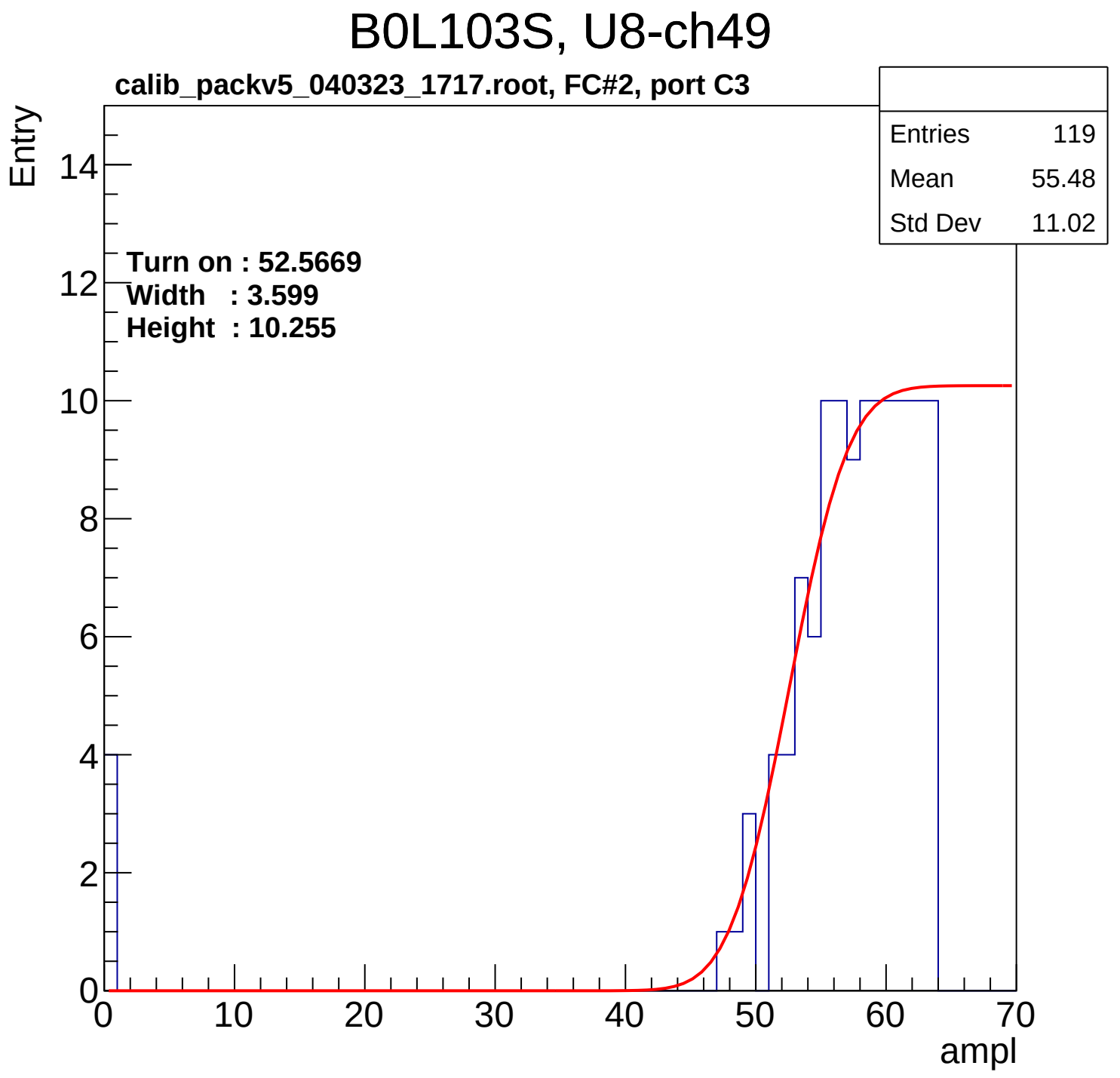
B0L103S, U8-ch49
calib_packv5_040323_1717.root, FC#2, port C3
Entries 119
Mean 55.48
Std Dev 11.02
Turn on : 52.5669
Width : 3.599
Height : 10.255
Entry
ampl
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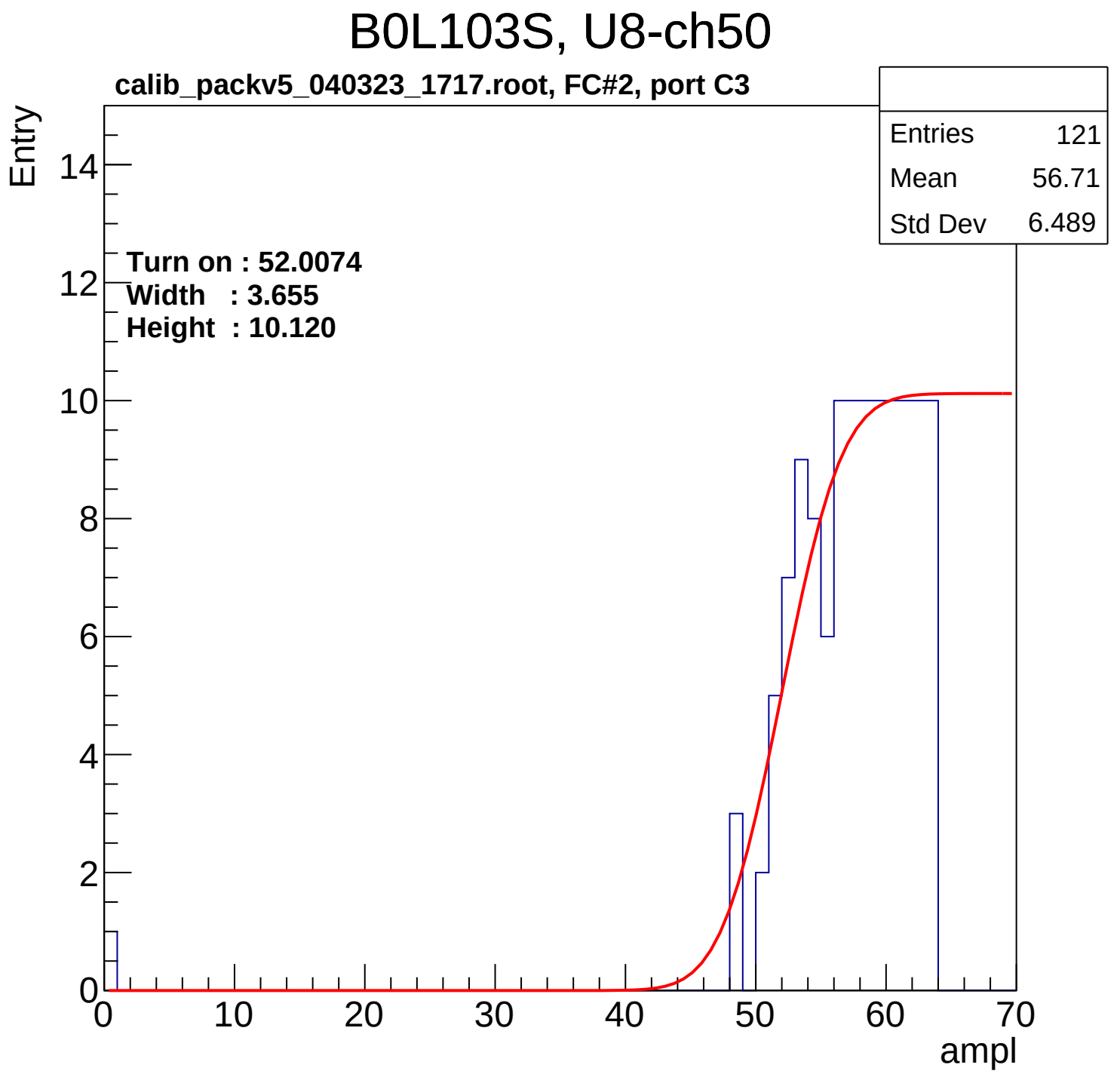
B0L103S, U8-ch50
calib_packv5_040323_1717.root, FC#2, port C3
Entries 121
Mean 56.71
Std Dev 6.489
Turn on : 52.0074
Width : 3.655
Height : 10.120
Entry
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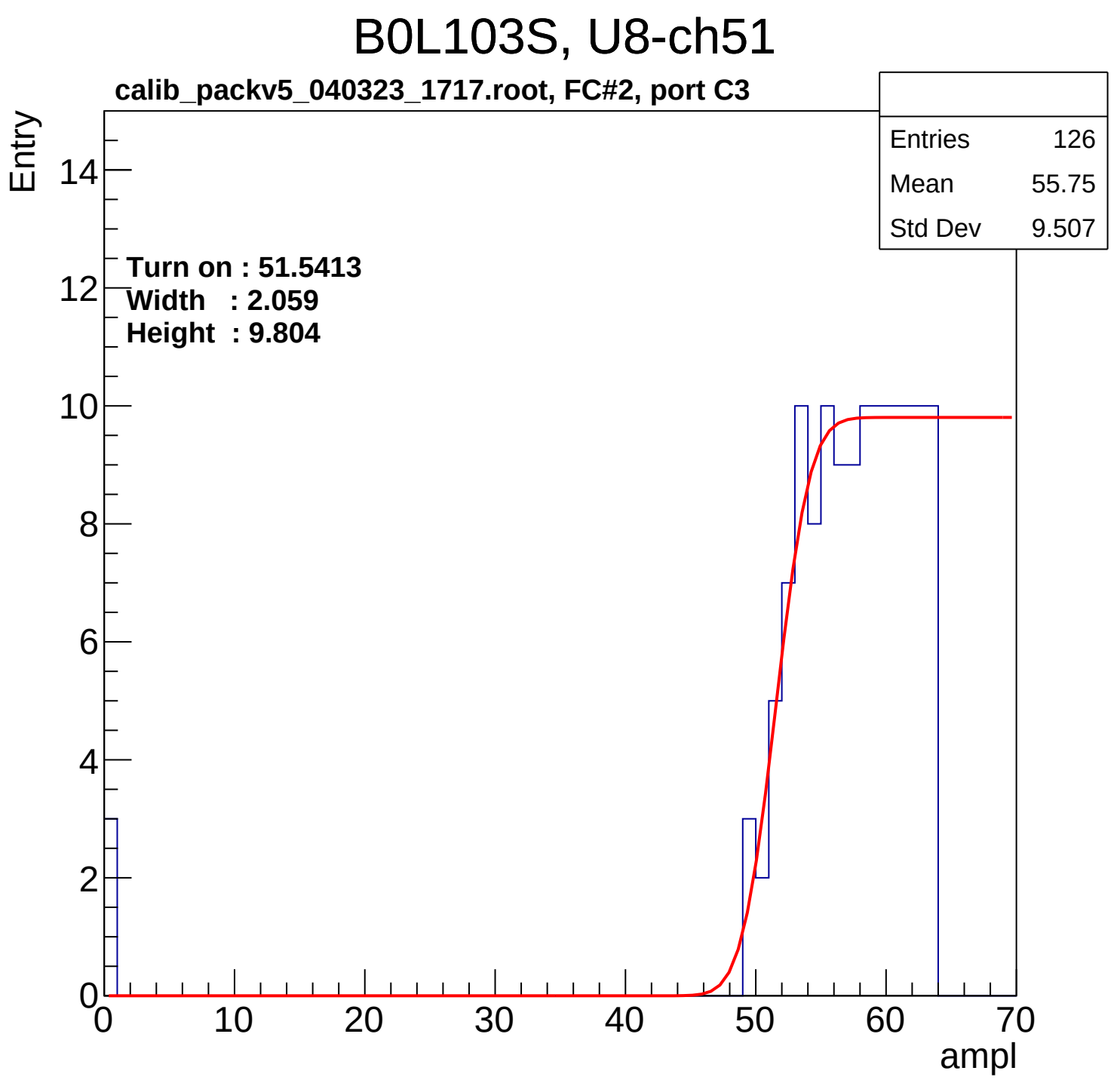
B0L103S, U8-ch51
calib_packv5_040323_1717.root, FC#2, port C3
Entries 126
Mean 55.75
Std Dev 9.507
Turn on : 51.5413
Width : 2.059
Height : 9.804
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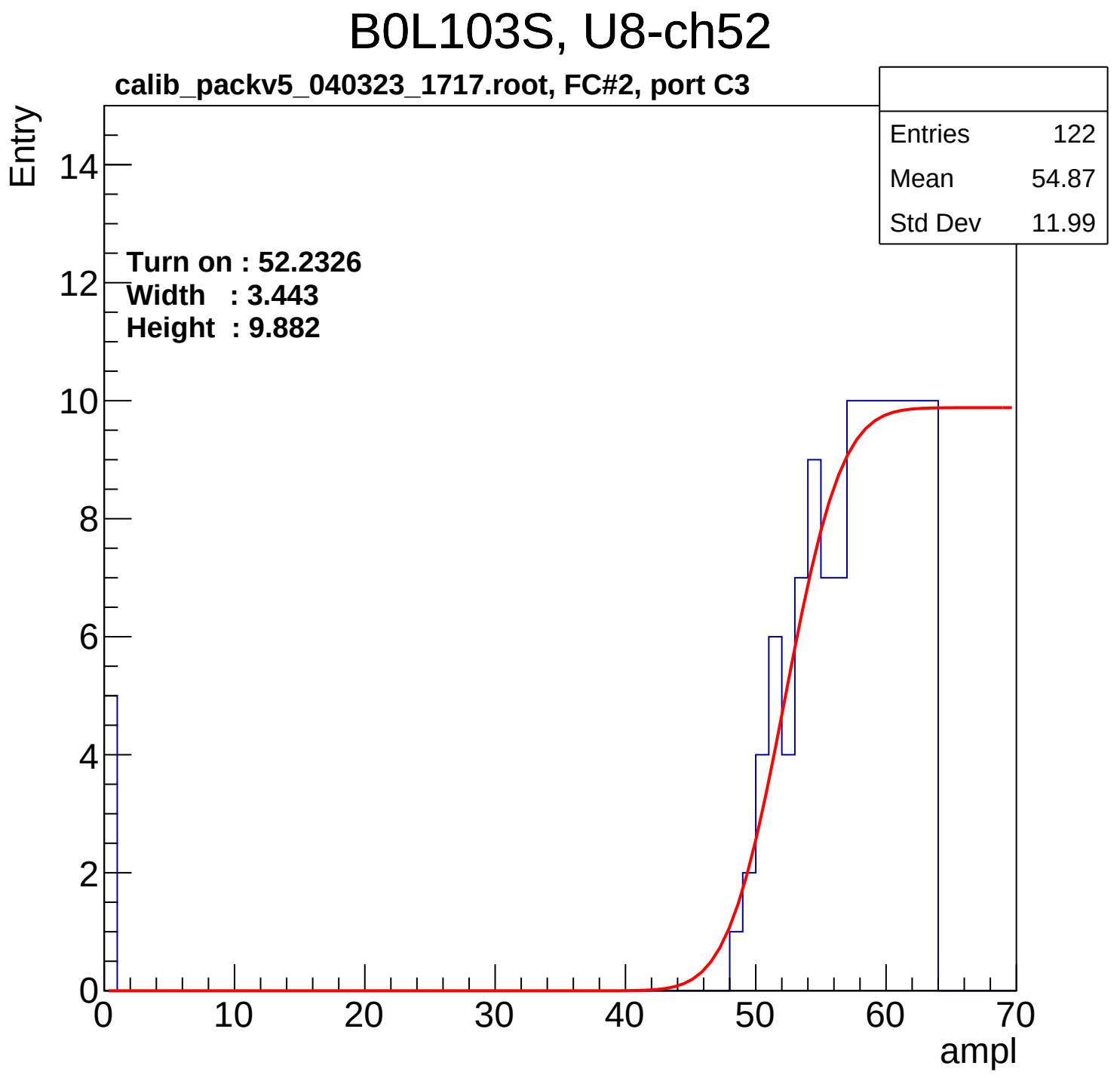
B0L103S, U8-ch52
calib_packv5_040323_1717.root, FC#2, port C3
Entries 122
Mean 54.87
Std Dev 11.99
Turn on : 52.2326
Width : 3.443
Height : 9.882
Entry
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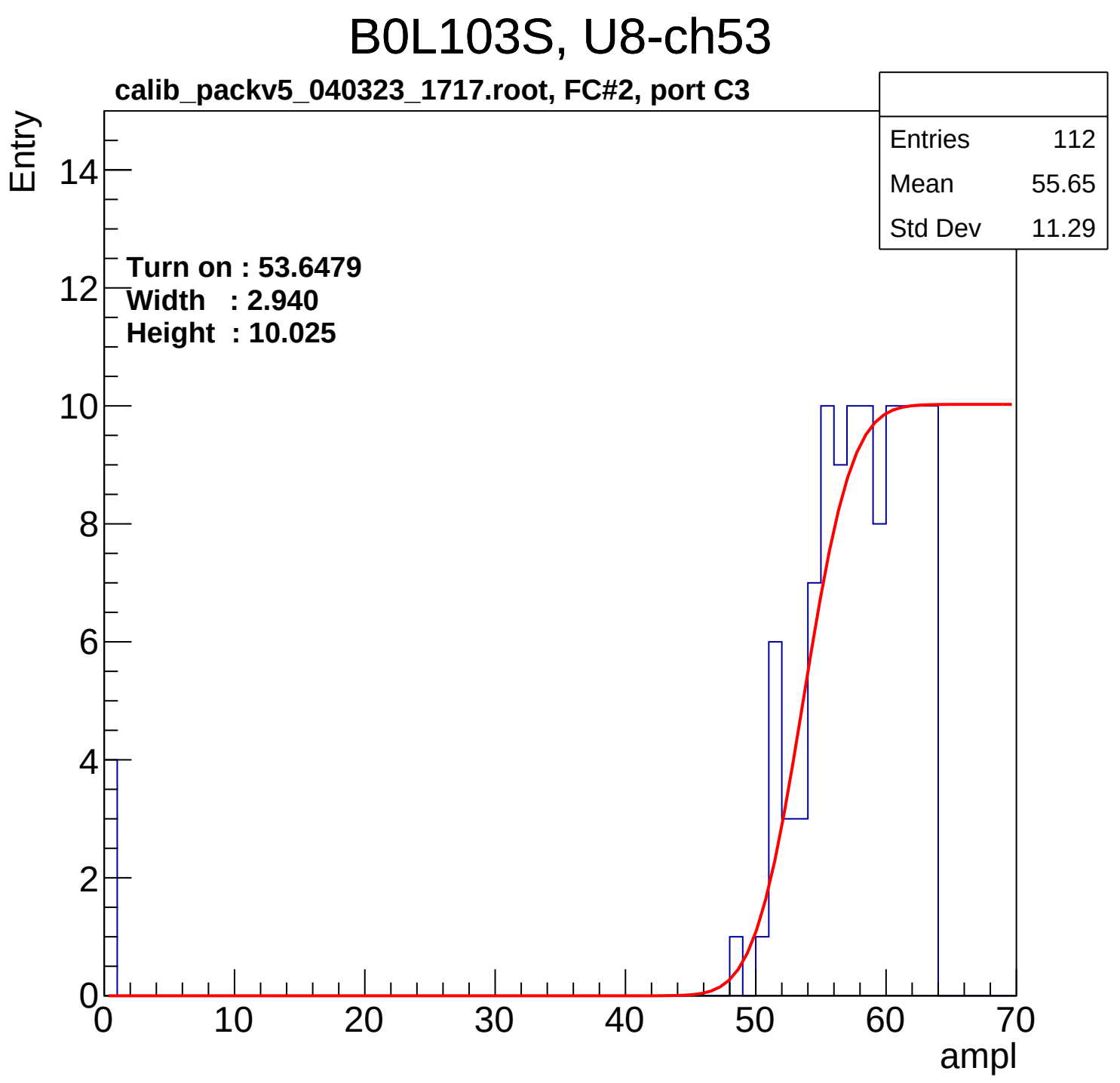
B0L103S, U8-ch53
calib_packv5_040323_1717.root, FC#2, port C3
Entries 112
Mean 55.65
Std Dev 11.29
Turn on : 53.6479
Width : 2.940
Height : 10.025
Entry
ampl
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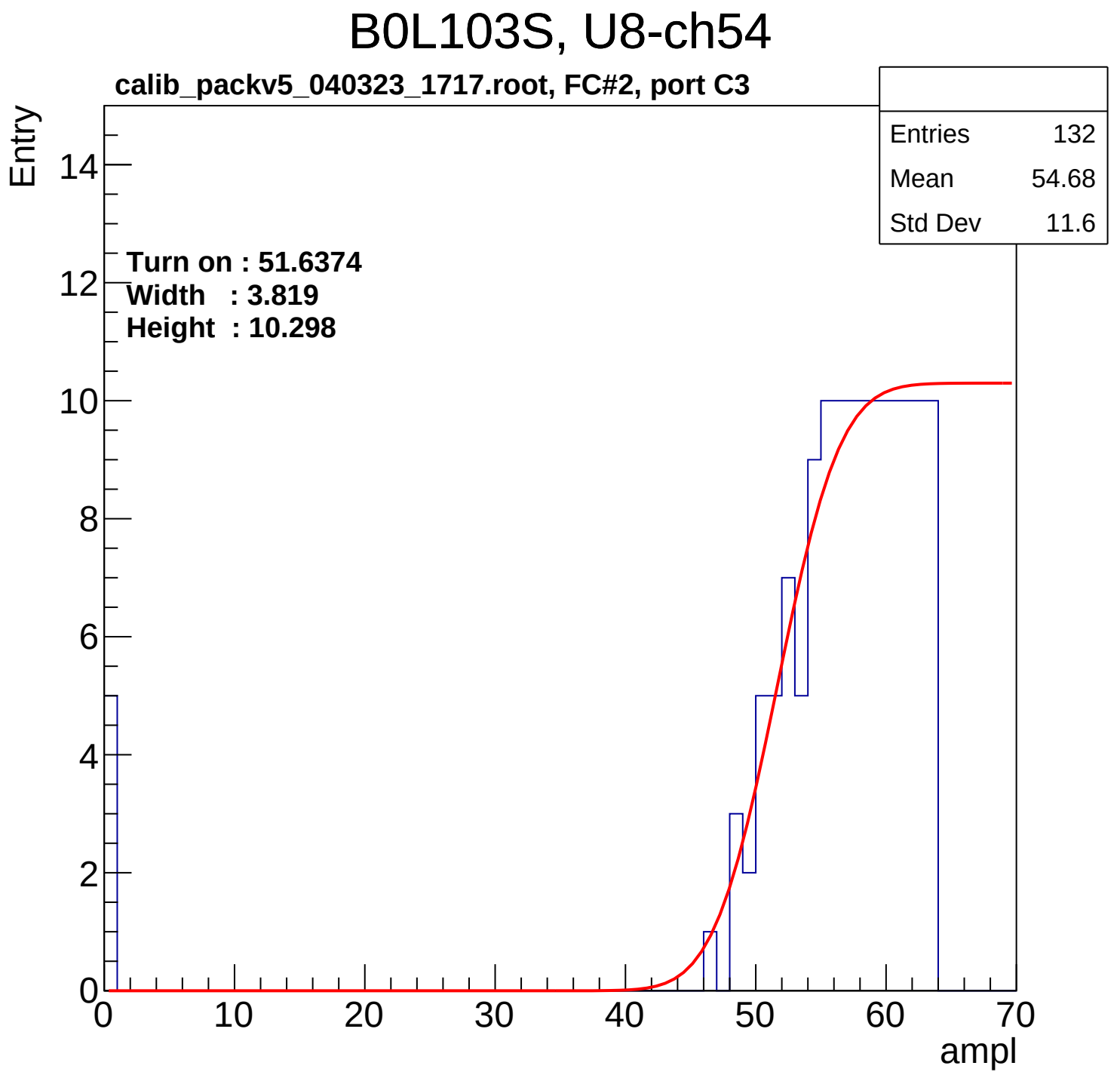
B0L103S, U8-ch54
calib_packv5_040323_1717.root, FC#2, port C3
Entries 132
Mean 54.68
Std Dev 11.6
Turn on : 51.6374
Width : 3.819
Height : 10.298
Entry
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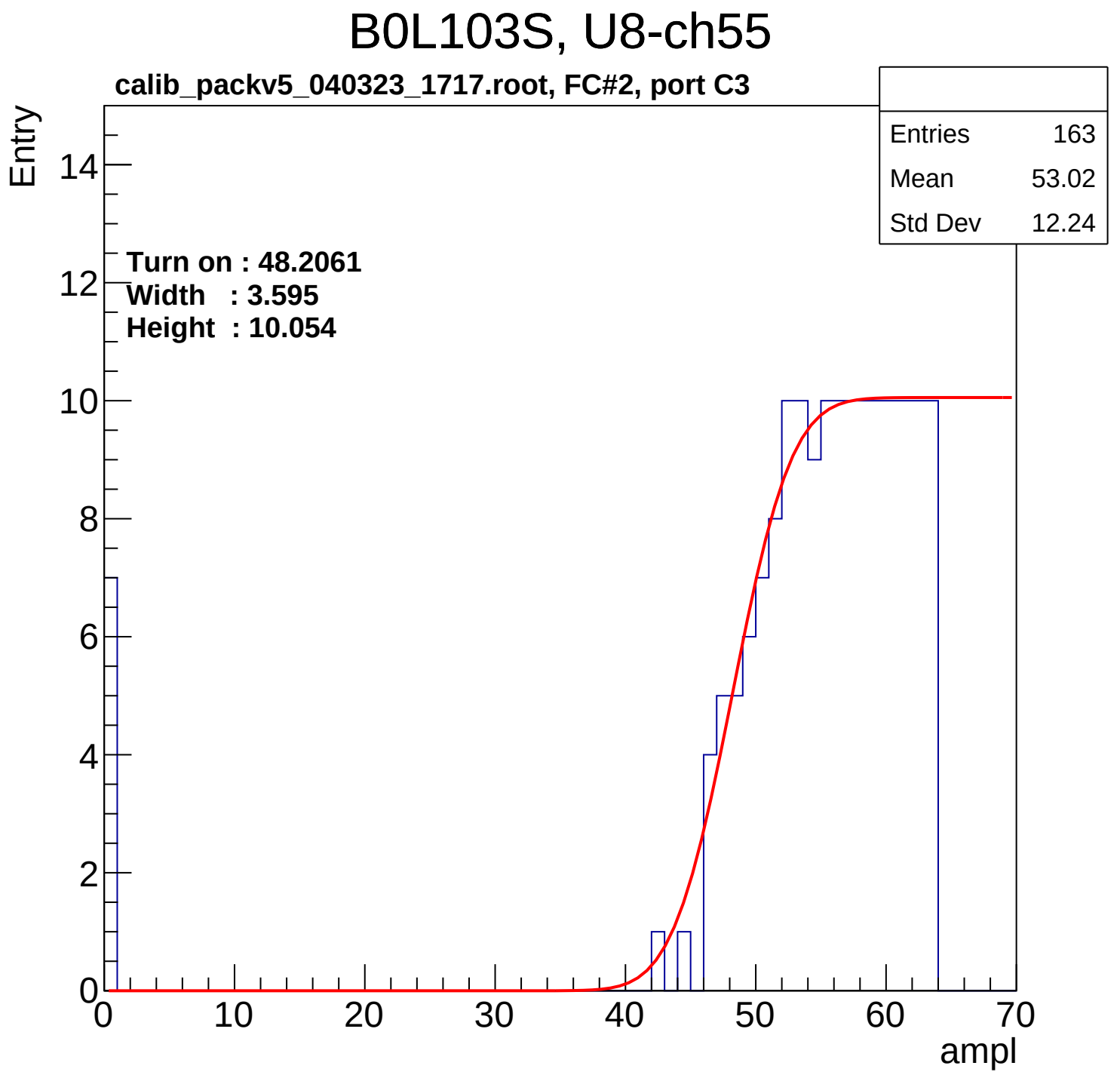
B0L103S, U8-ch55
calib_packv5_040323_1717.root, FC#2, port C3
Entries 163
Mean 53.02
Std Dev 12.24
Turn on : 48.2061
Width : 3.595
Height : 10.054
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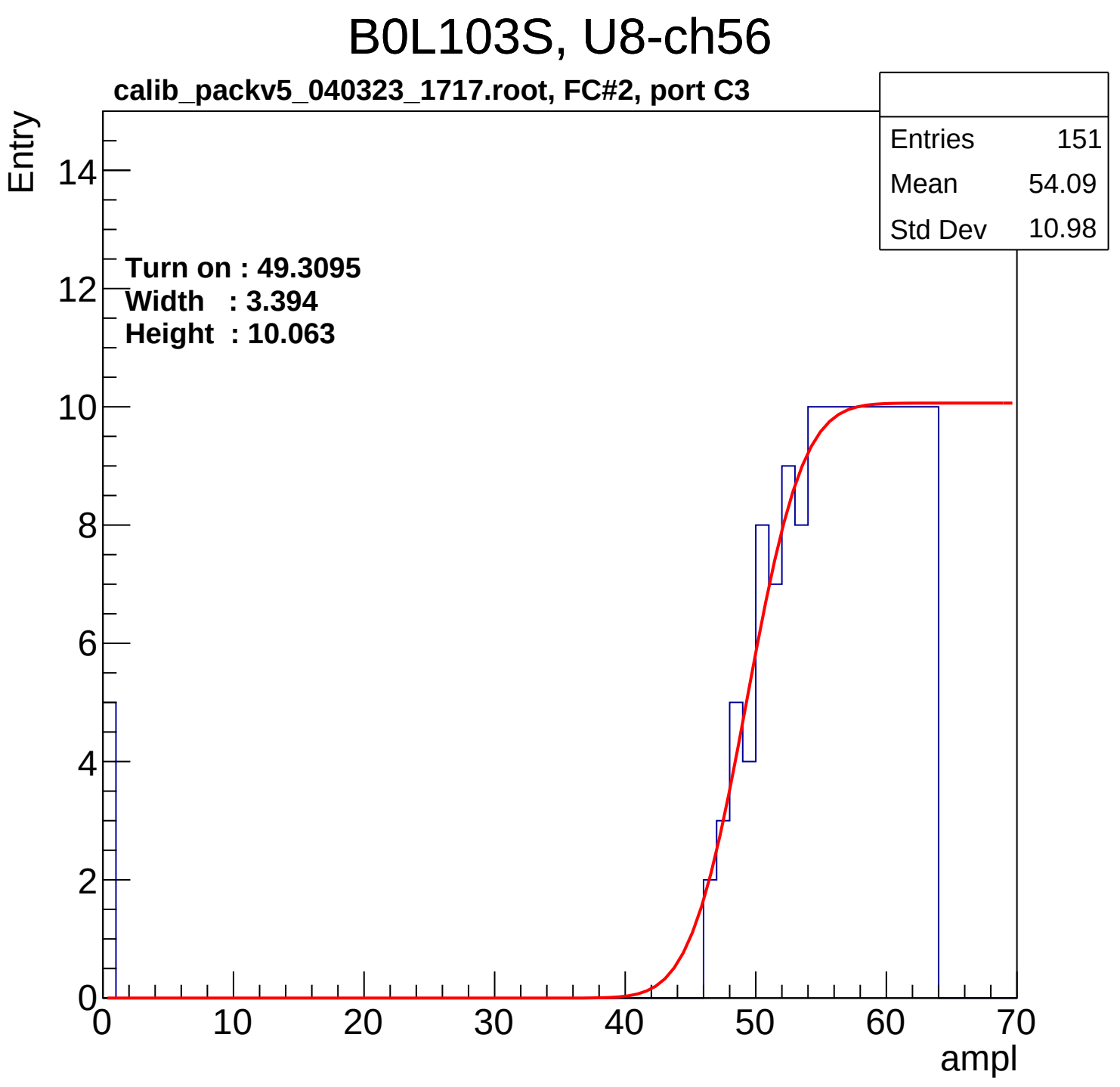
B0L103S, U8-ch56
calib_packv5_040323_1717.root, FC#2, port C3
Entries 151
Mean 54.09
Std Dev 10.98
Turn on : 49.3095
Width : 3.394
Height : 10.063
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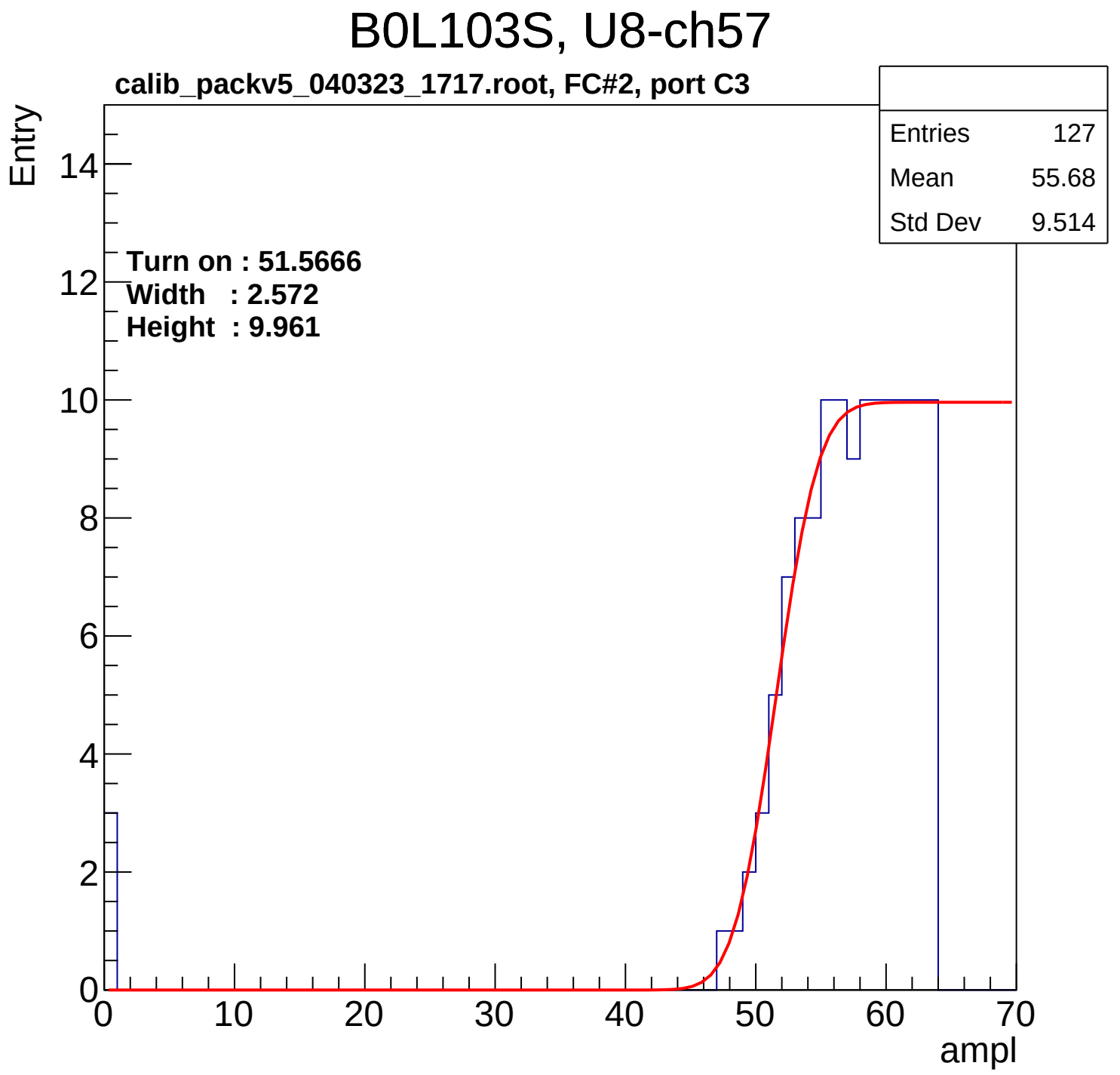
B0L103S, U8-ch57
calib_packv5_040323_1717.root, FC#2, port C3
Entries 127
Mean 55.68
Std Dev 9.514
Turn on : 51.5666
Width : 2.572
Height : 9.961
Entry
ampl
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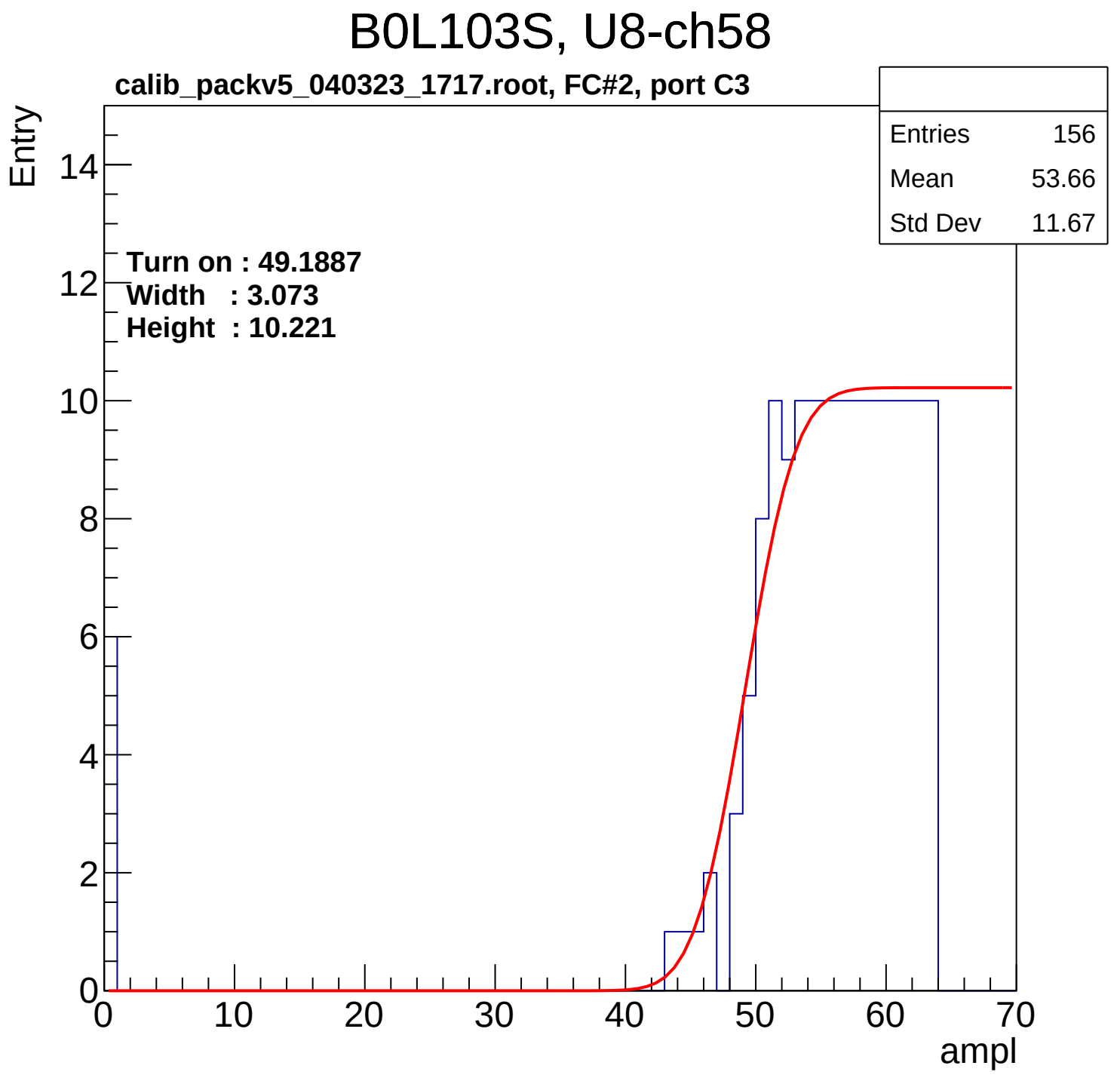
B0L103S, U8-ch58
calib_packv5_040323_1717.root, FC#2, port C3
Entries 156
Mean 53.66
Std Dev 11.67
Turn on : 49.1887
Width : 3.073
Height : 10.221
Entry
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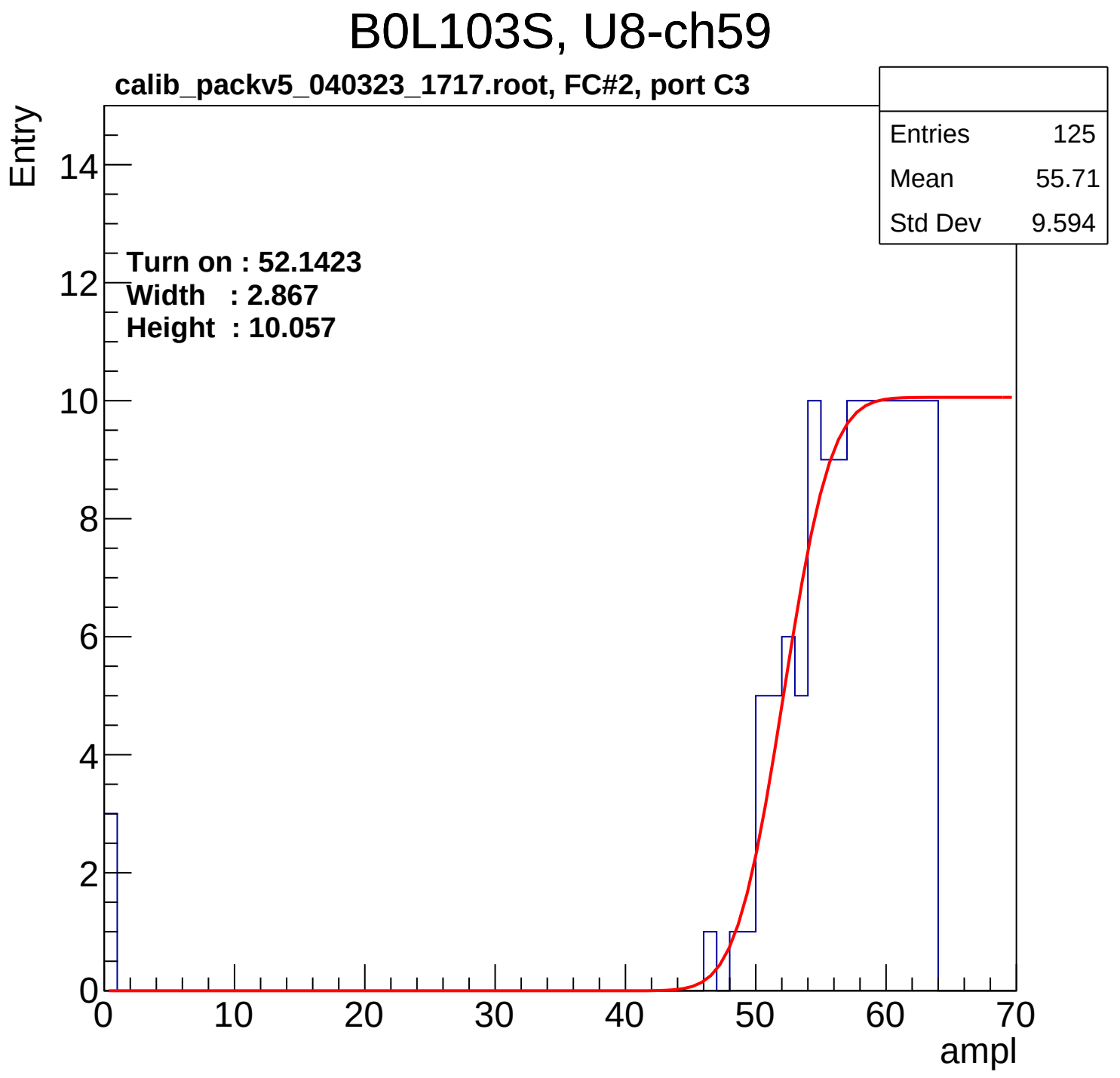
B0L103S, U8-ch59
calib_packv5_040323_1717.root, FC#2, port C3
Entries 125
Mean 55.71
Std Dev 9.594
Turn on : 52.1423
Width : 2.867
Height : 10.057
Entry
ampl
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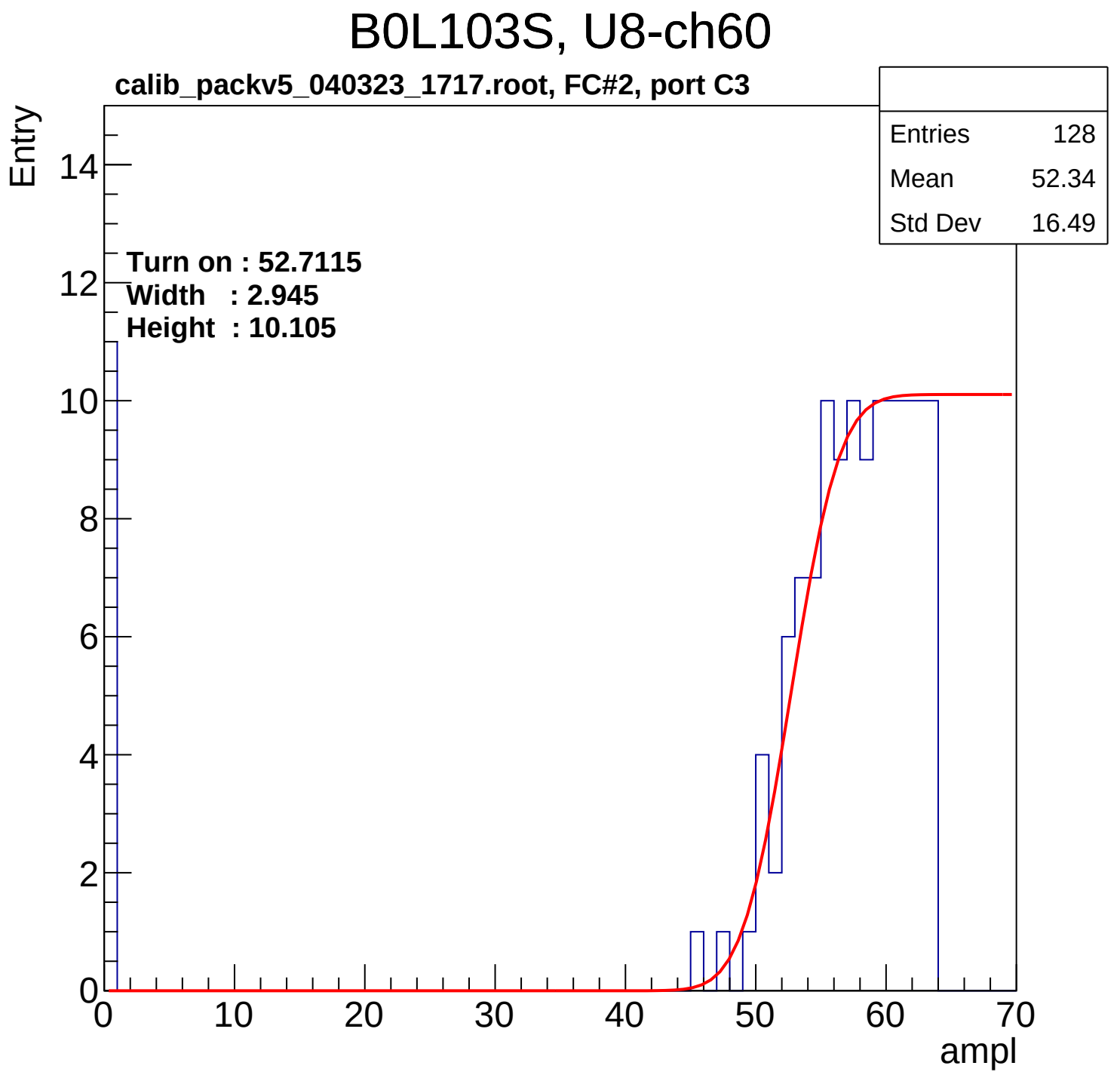
B0L103S, U8-ch60
calib_packv5_040323_1717.root, FC#2, port C3
Entries 128
Mean 52.34
Std Dev 16.49
Turn on : 52.7115
Width : 2.945
Height : 10.105
Entry
ampl
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2
4
6
8
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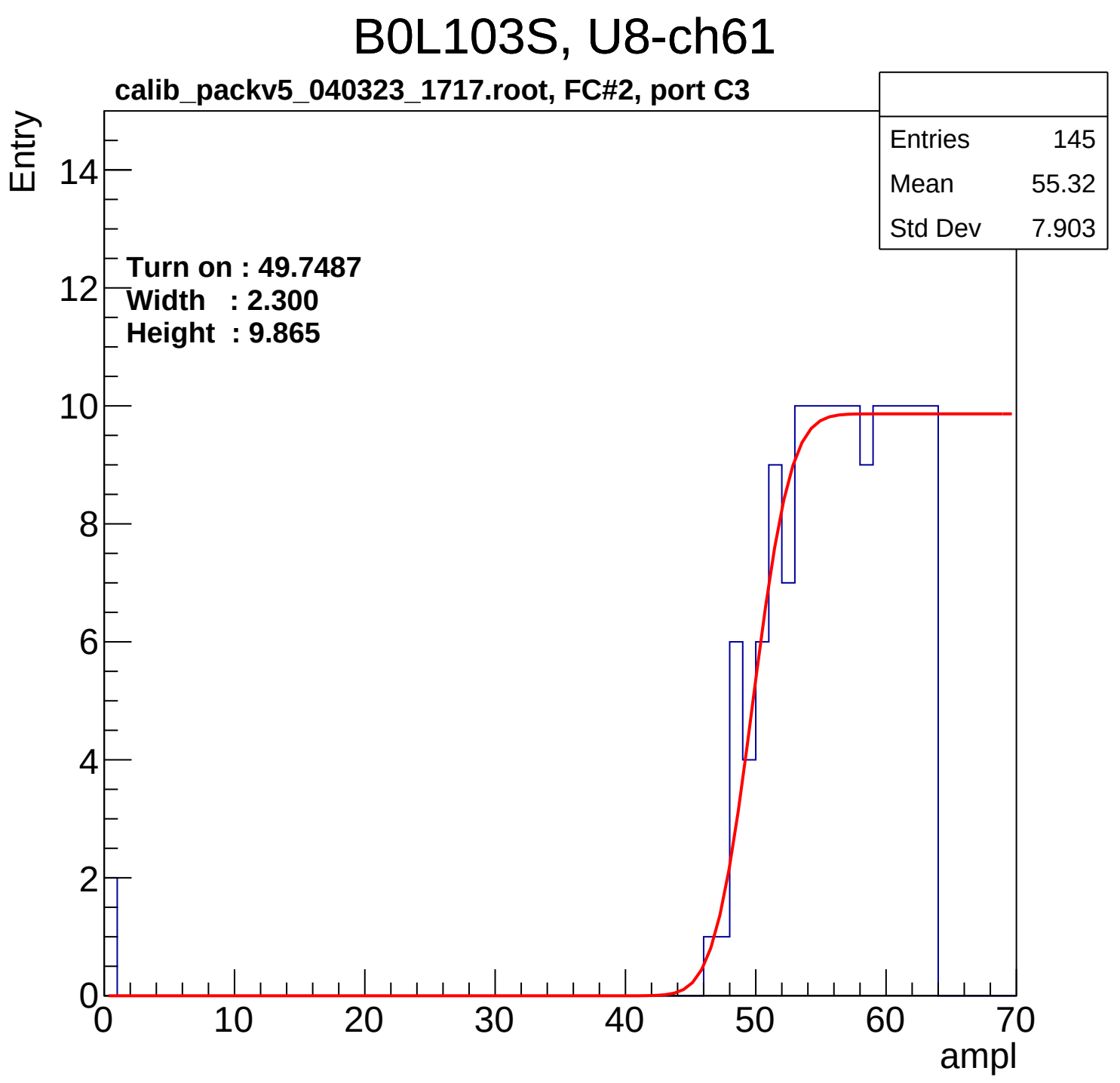
B0L103S, U8-ch61
calib_packv5_040323_1717.root, FC#2, port C3
Entries 145
Mean 55.32
Std Dev 7.903
Turn on : 49.7487
Width : 2.300
Height : 9.865
Entry
ampl
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2
4
6
8
10
12
14
0
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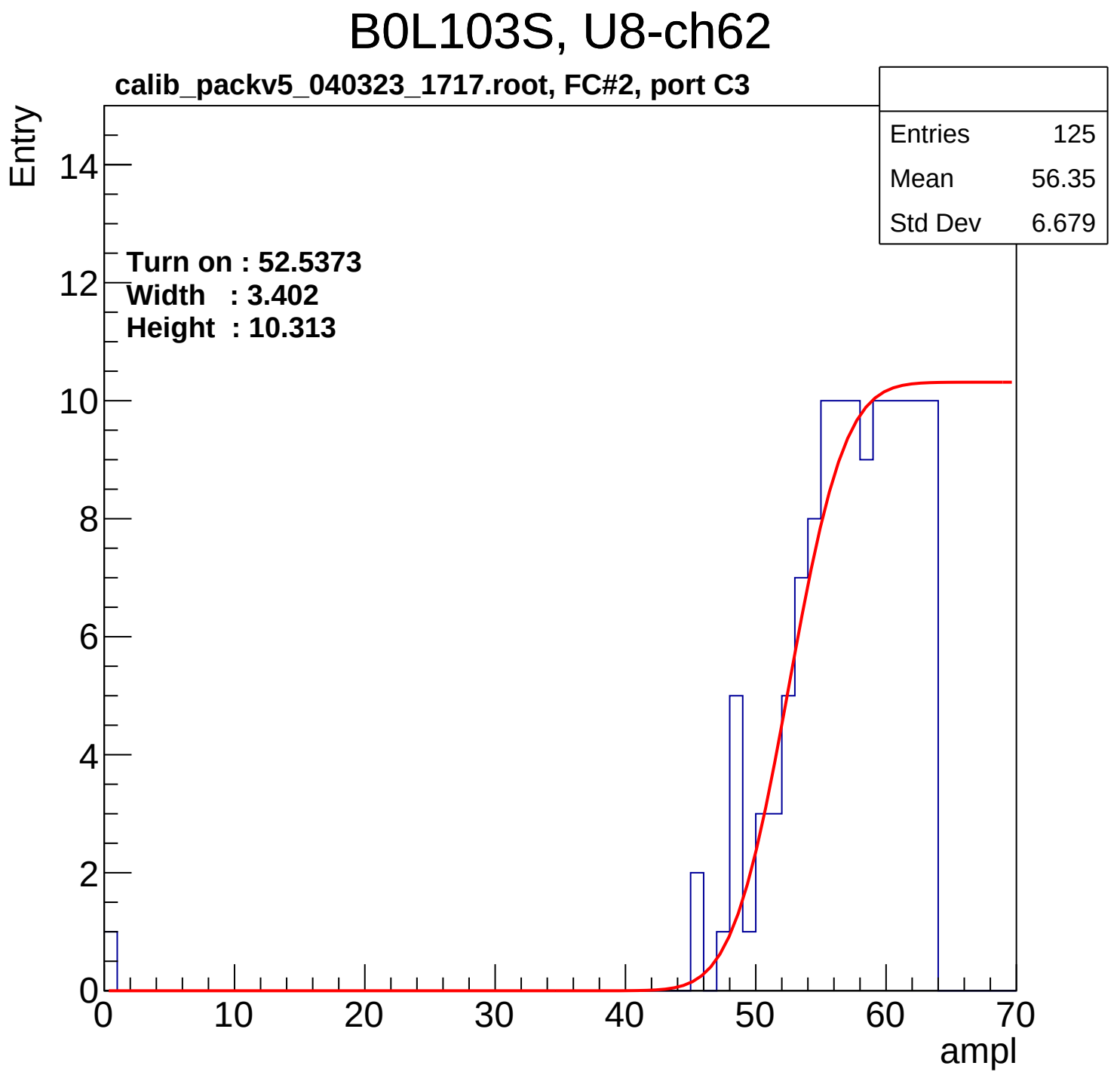
B0L103S, U8-ch62
calib_packv5_040323_1717.root, FC#2, port C3
Entries 125
Mean 56.35
Std Dev 6.679
Turn on : 52.5373
Width : 3.402
Height : 10.313
Entry
ampl
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6
8
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0
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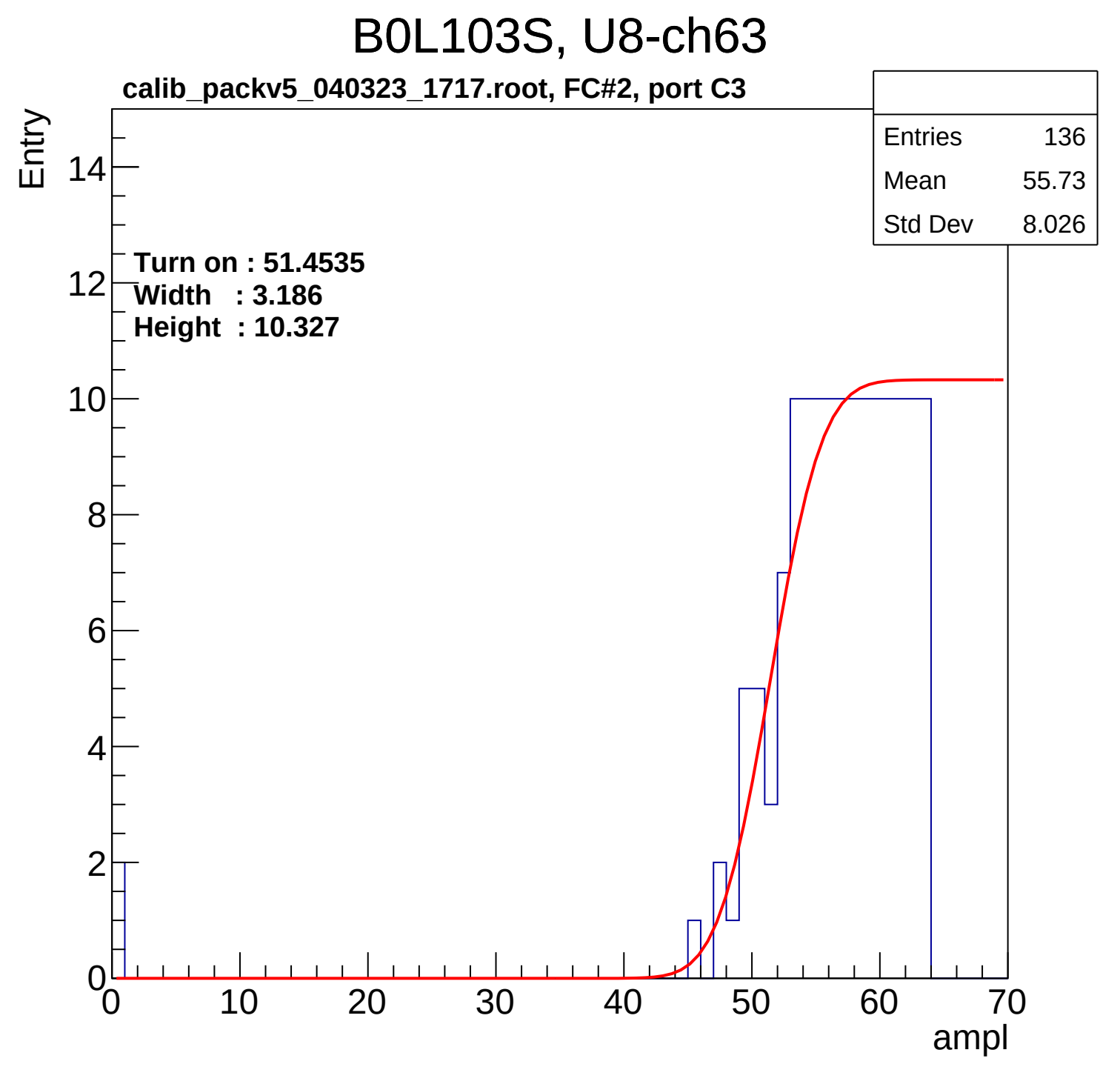
B0L103S, U8-ch63
calib_packv5_040323_1717.root, FC#2, port C3
Entries 136
Mean 55.73
Std Dev 8.026
Turn on : 51.4535
Width : 3.186
Height : 10.327
Entry
ampl
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2
4
6
8
10
12
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0
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20
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40
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60
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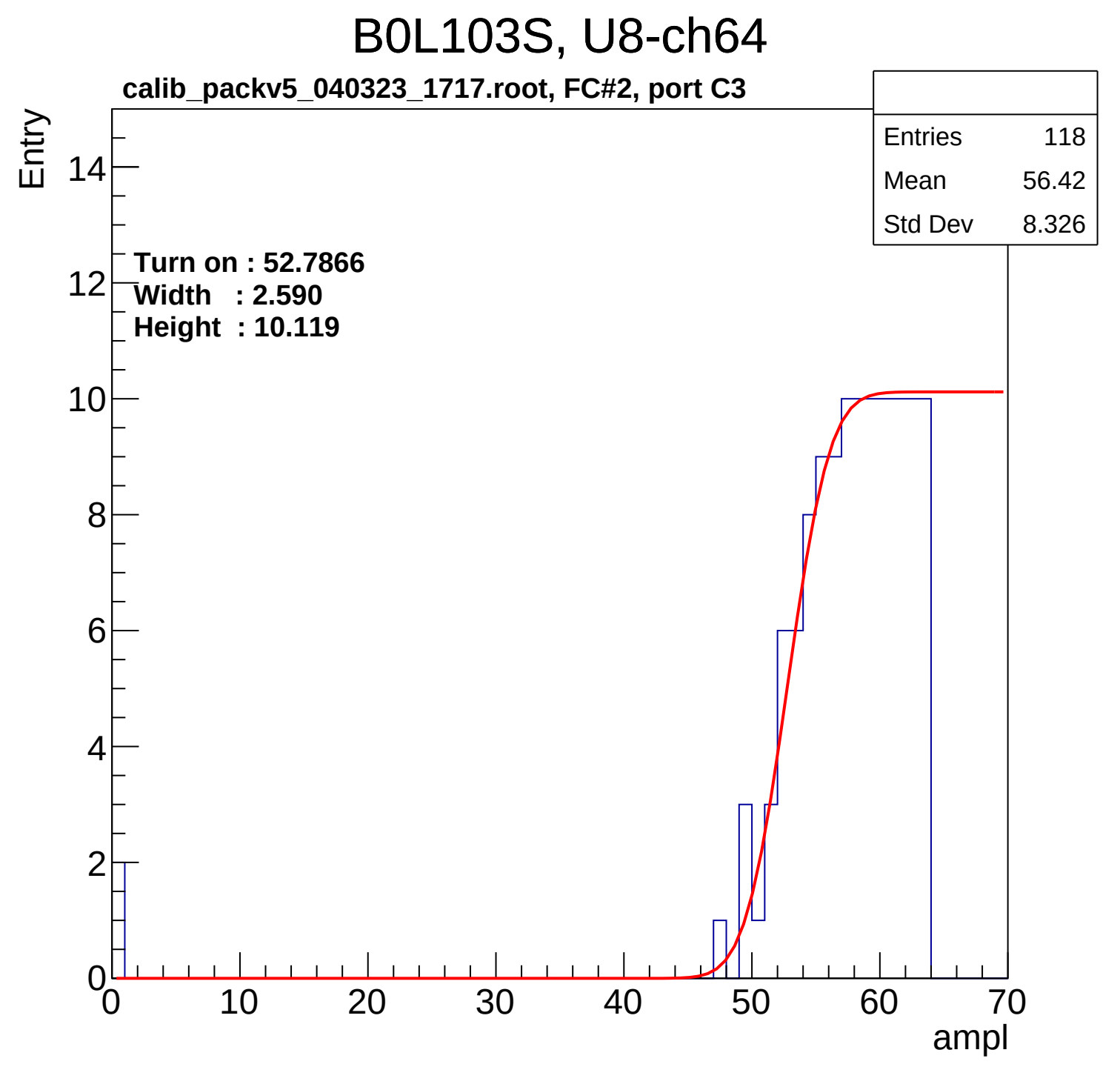
B0L103S, U8-ch64
calib_packv5_040323_1717.root, FC#2, port C3
Entries 118
Mean 56.42
Std Dev 8.326
Turn on : 52.7866
Width : 2.590
Height : 10.119
Entry
ampl
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4
6
8
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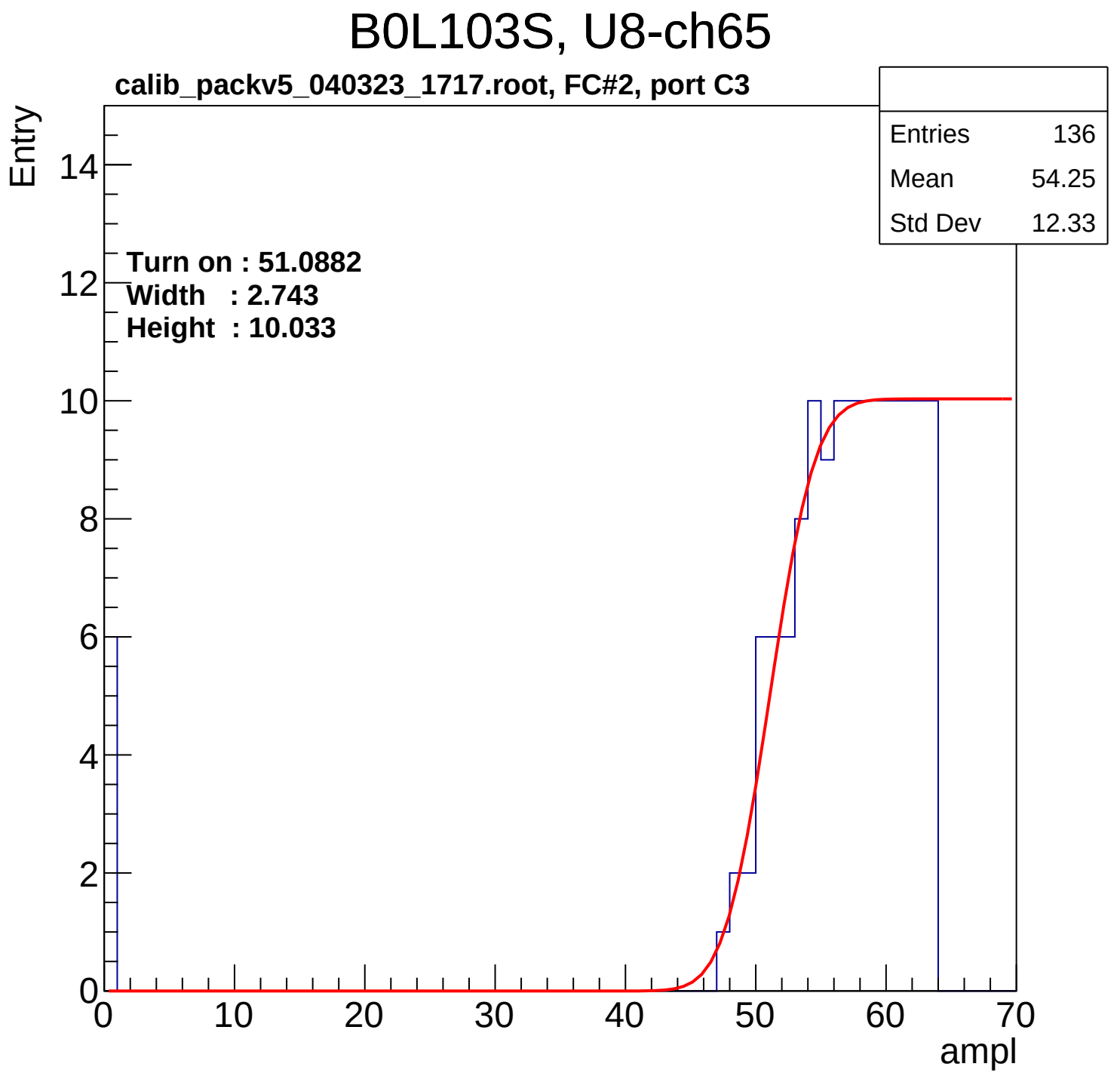
B0L103S, U8-ch65
calib_packv5_040323_1717.root, FC#2, port C3
Entries 136
Mean 54.25
Std Dev 12.33
Turn on : 51.0882
Width : 2.743
Height : 10.033
Entry
ampl
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2
4
6
8
10
12
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0
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60
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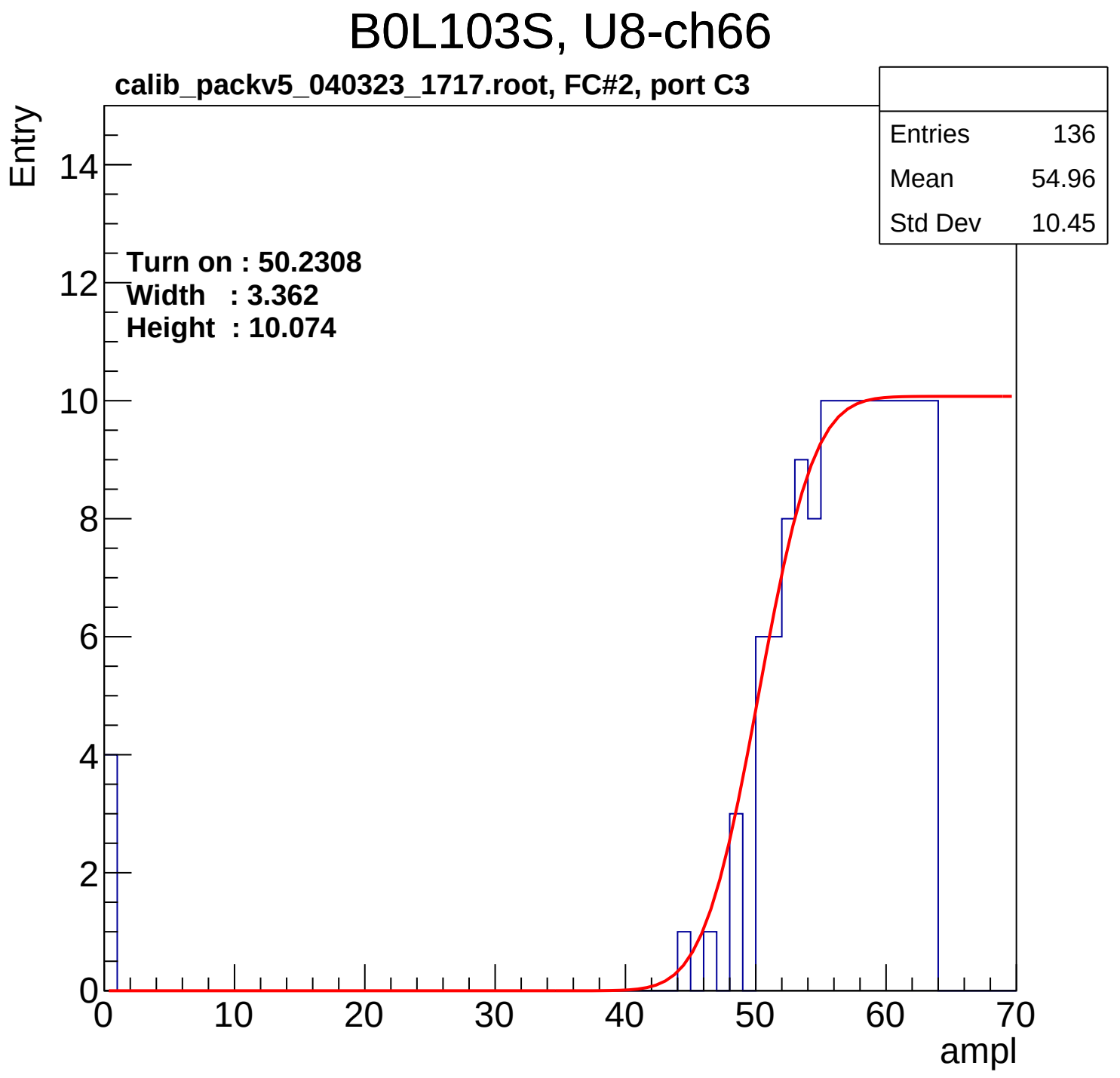
B0L103S, U8-ch66
calib_packv5_040323_1717.root, FC#2, port C3
Entries 136
Mean 54.96
Std Dev 10.45
Turn on : 50.2308
Width : 3.362
Height : 10.074
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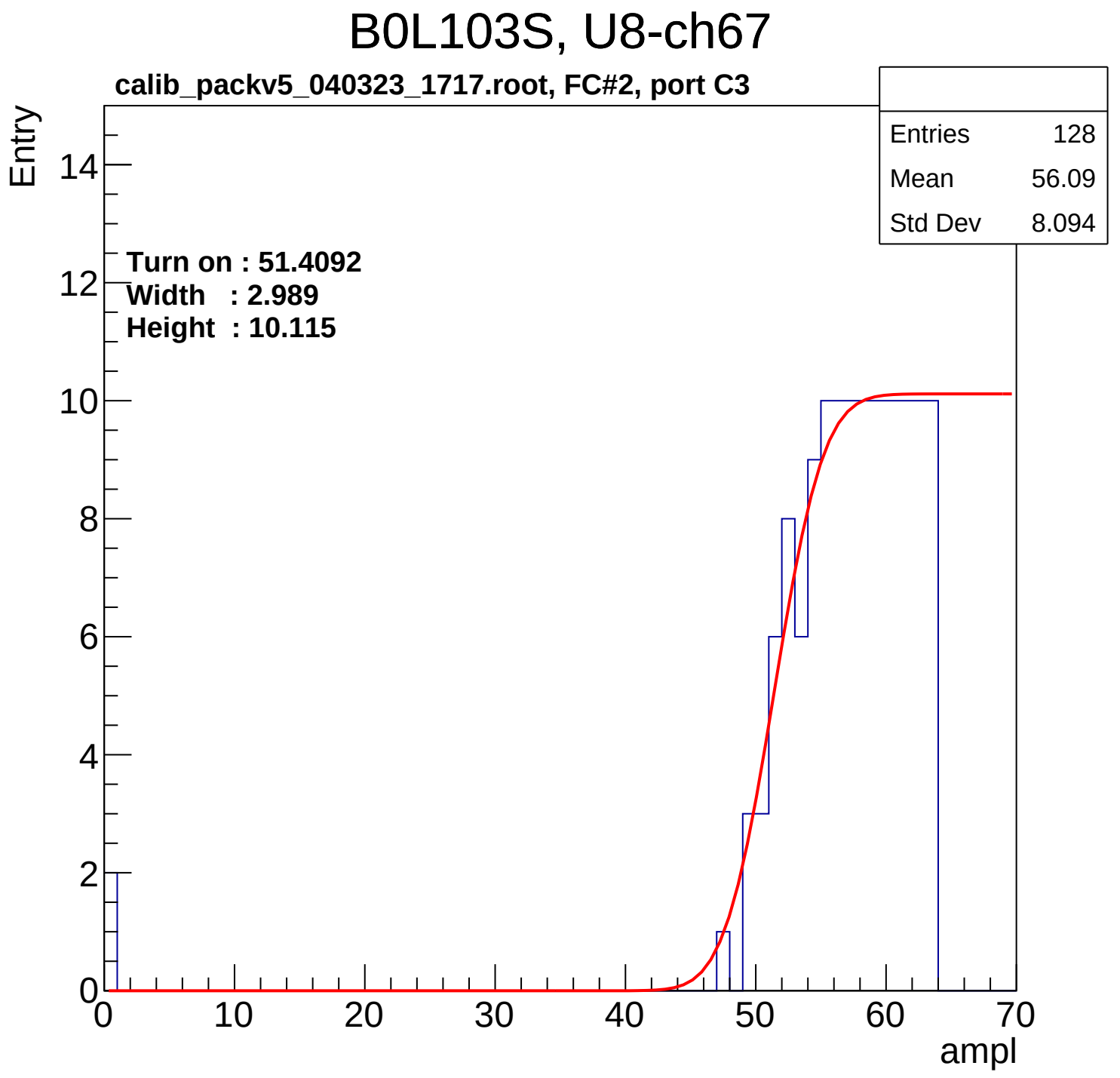
B0L103S, U8-ch67
calib_packv5_040323_1717.root, FC#2, port C3
Entries 128
Mean 56.09
Std Dev 8.094
Turn on : 51.4092
Width : 2.989
Height : 10.115
Entry
ampl
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4
6
8
10
12
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0
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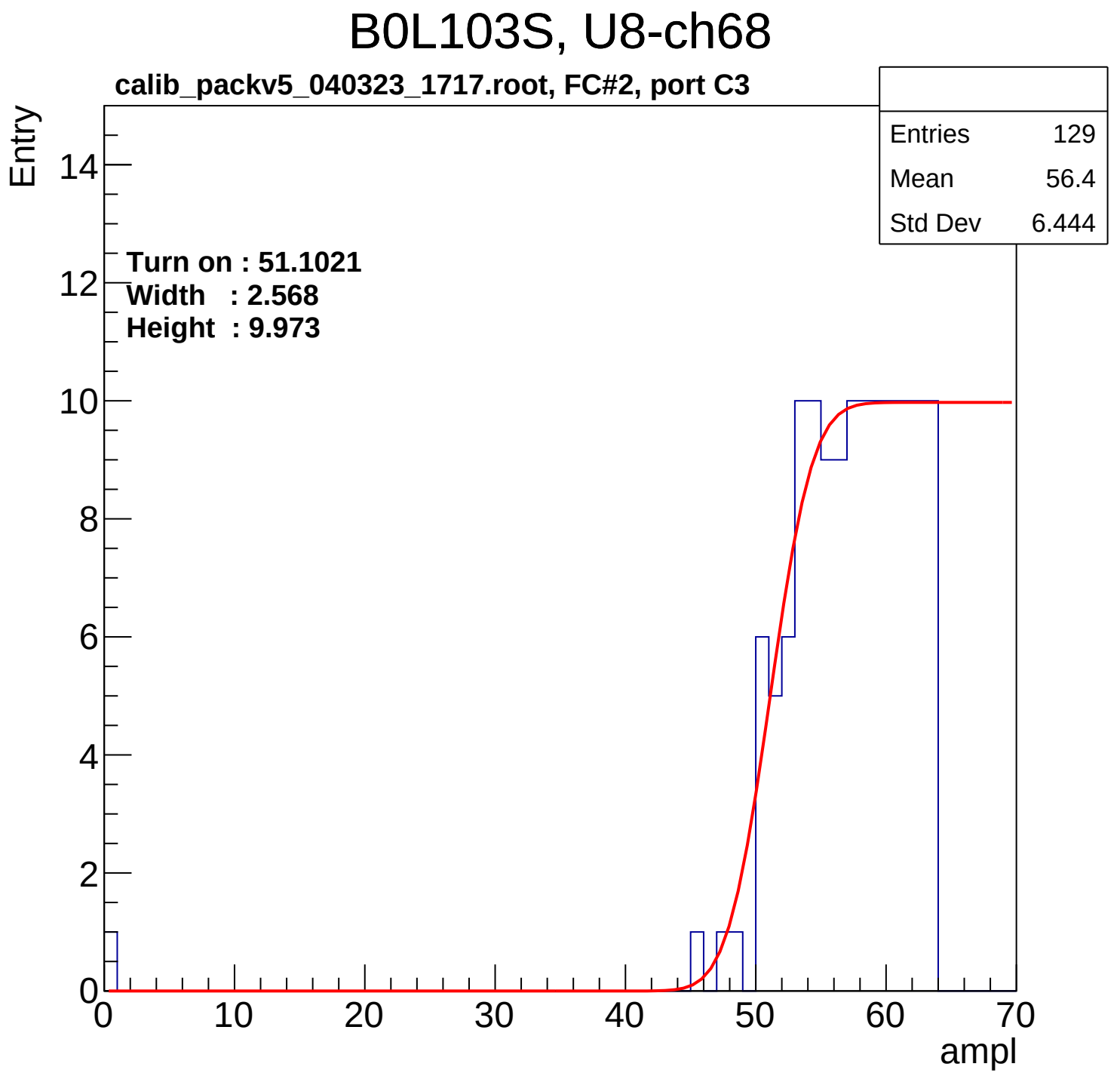
B0L103S, U8-ch68
calib_packv5_040323_1717.root, FC#2, port C3
Entries 129
Mean 56.4
Std Dev 6.444
Turn on : 51.1021
Width : 2.568
Height : 9.973
Entry
ampl
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6
8
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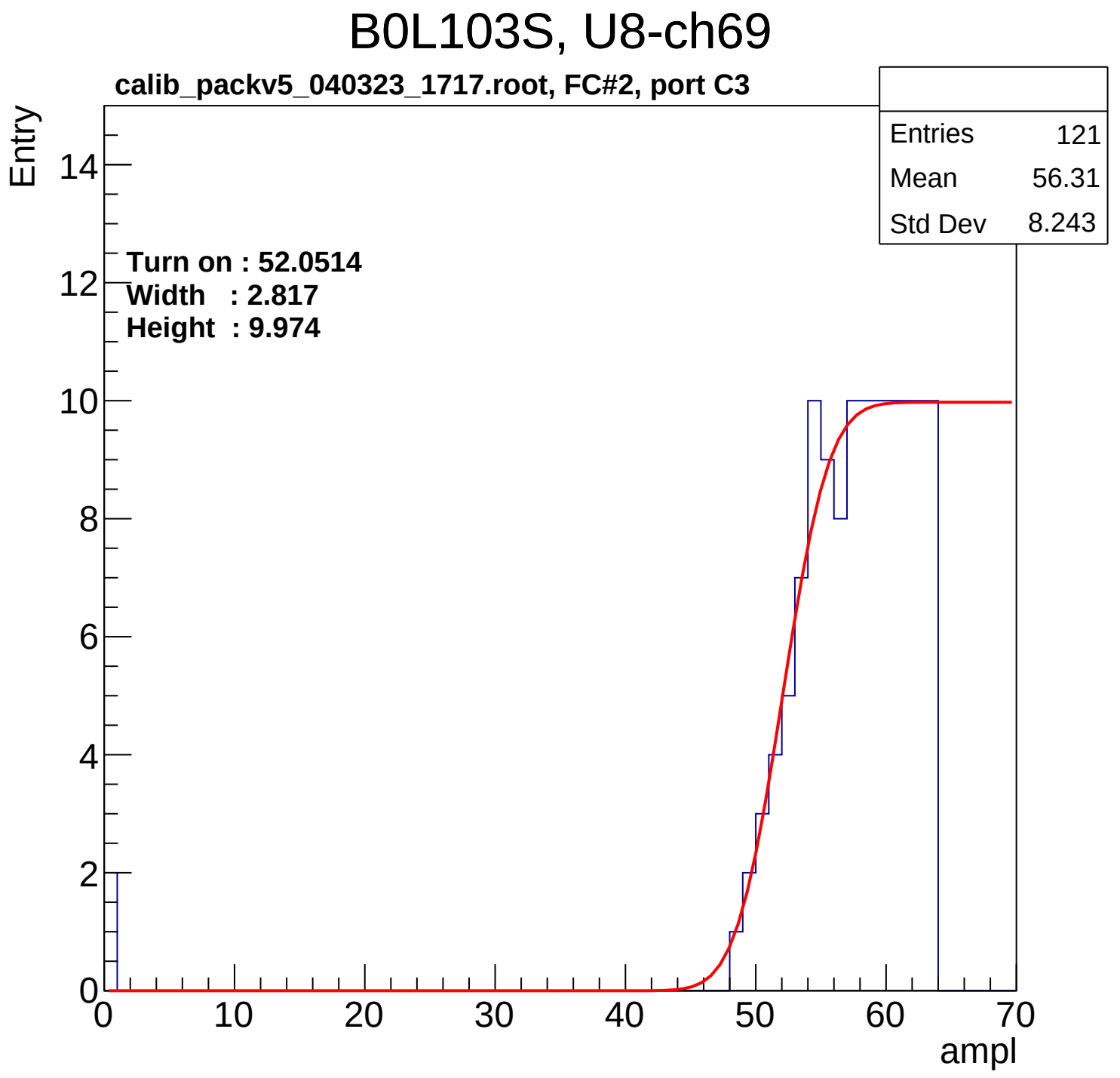
B0L103S, U8-ch69
calib_packv5_040323_1717.root, FC#2, port C3
Entries 121
Mean 56.31
Std Dev 8.243
Turn on : 52.0514
Width : 2.817
Height : 9.974
Entry
ampl
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6
8
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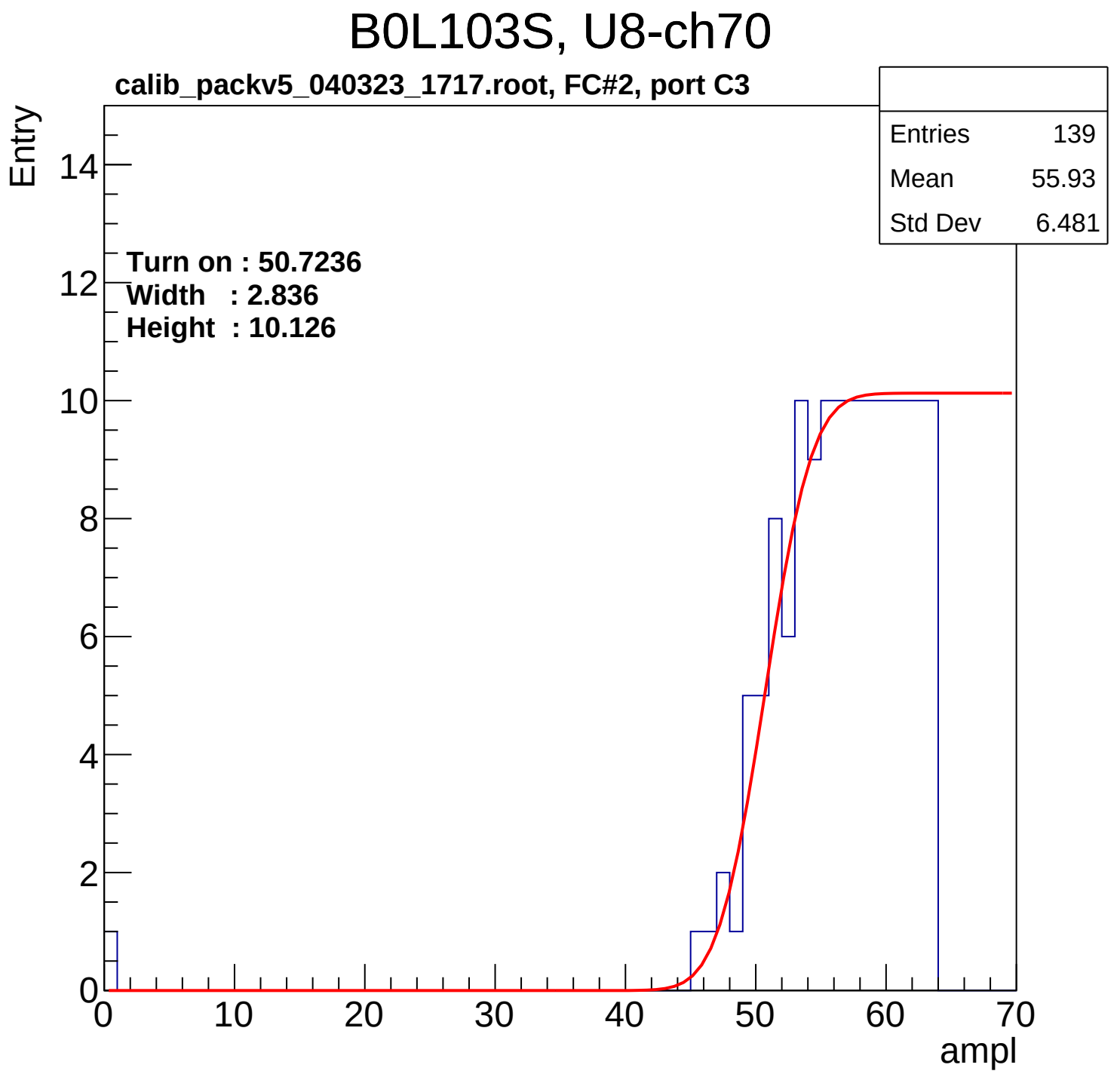
B0L103S, U8-ch70
calib_packv5_040323_1717.root, FC#2, port C3
Entries 139
Mean 55.93
Std Dev 6.481
Turn on : 50.7236
Width : 2.836
Height : 10.126
Entry
ampl
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6
8
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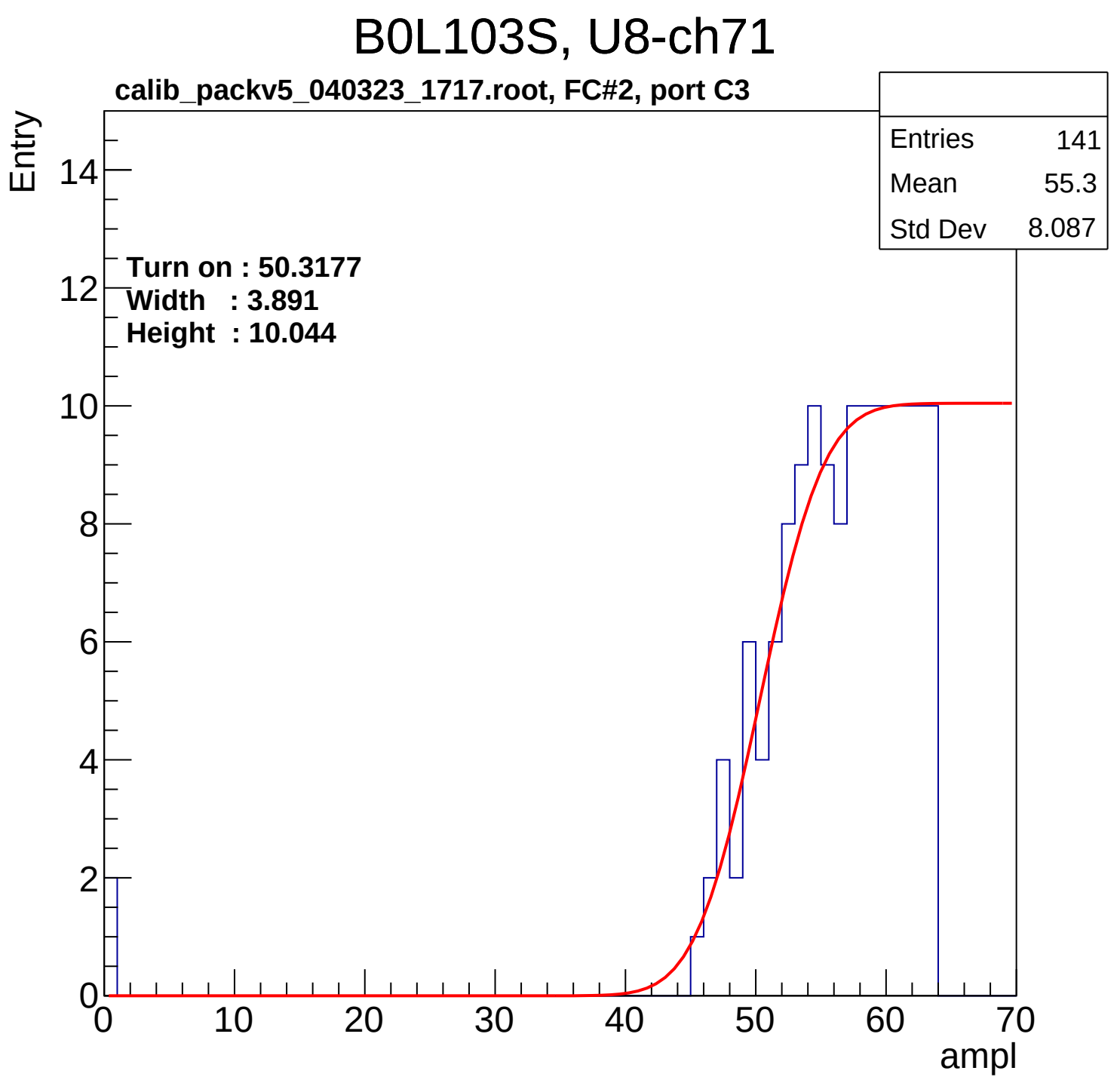
B0L103S, U8-ch71
calib_packv5_040323_1717.root, FC#2, port C3
Entries 141
Mean 55.3
Std Dev 8.087
Turn on : 50.3177
Width : 3.891
Height : 10.044
Entry
ampl
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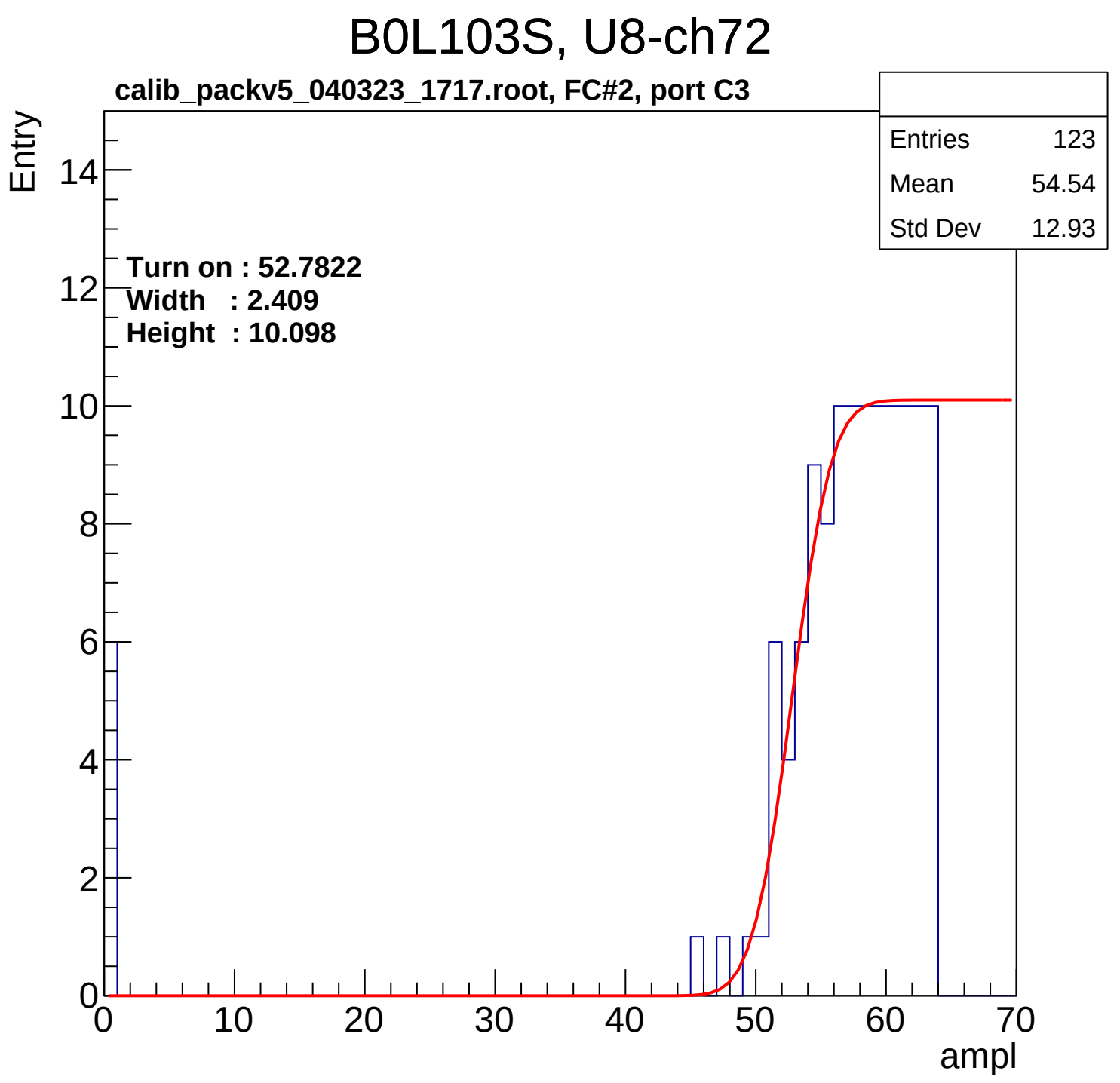
B0L103S, U8-ch72
calib_packv5_040323_1717.root, FC#2, port C3
Entries 123
Mean 54.54
Std Dev 12.93
Turn on : 52.7822
Width : 2.409
Height : 10.098
Entry
ampl
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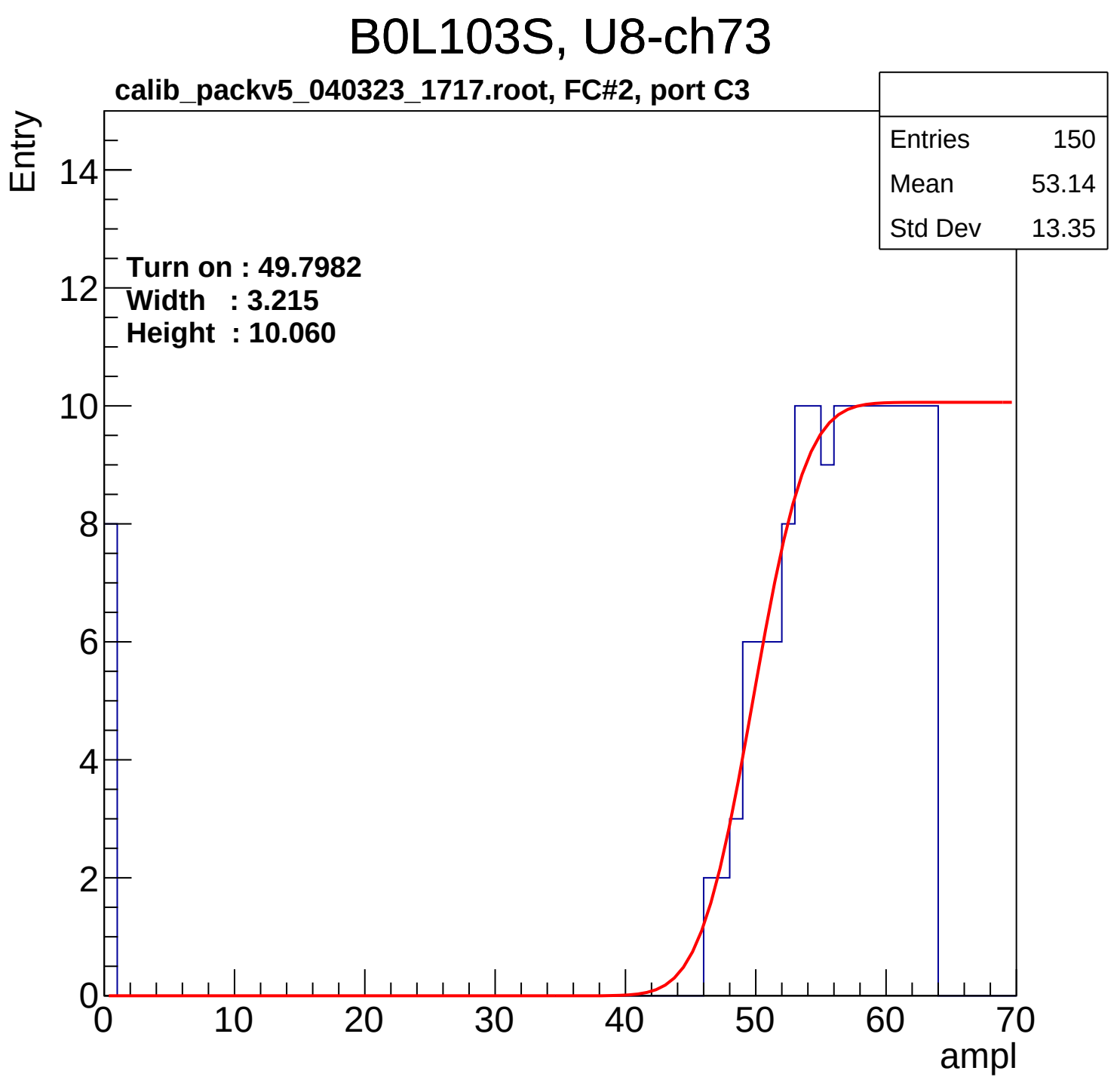
B0L103S, U8-ch73
calib_packv5_040323_1717.root, FC#2, port C3
Entries 150
Mean 53.14
Std Dev 13.35
Turn on : 49.7982
Width : 3.215
Height : 10.060
Entry
ampl
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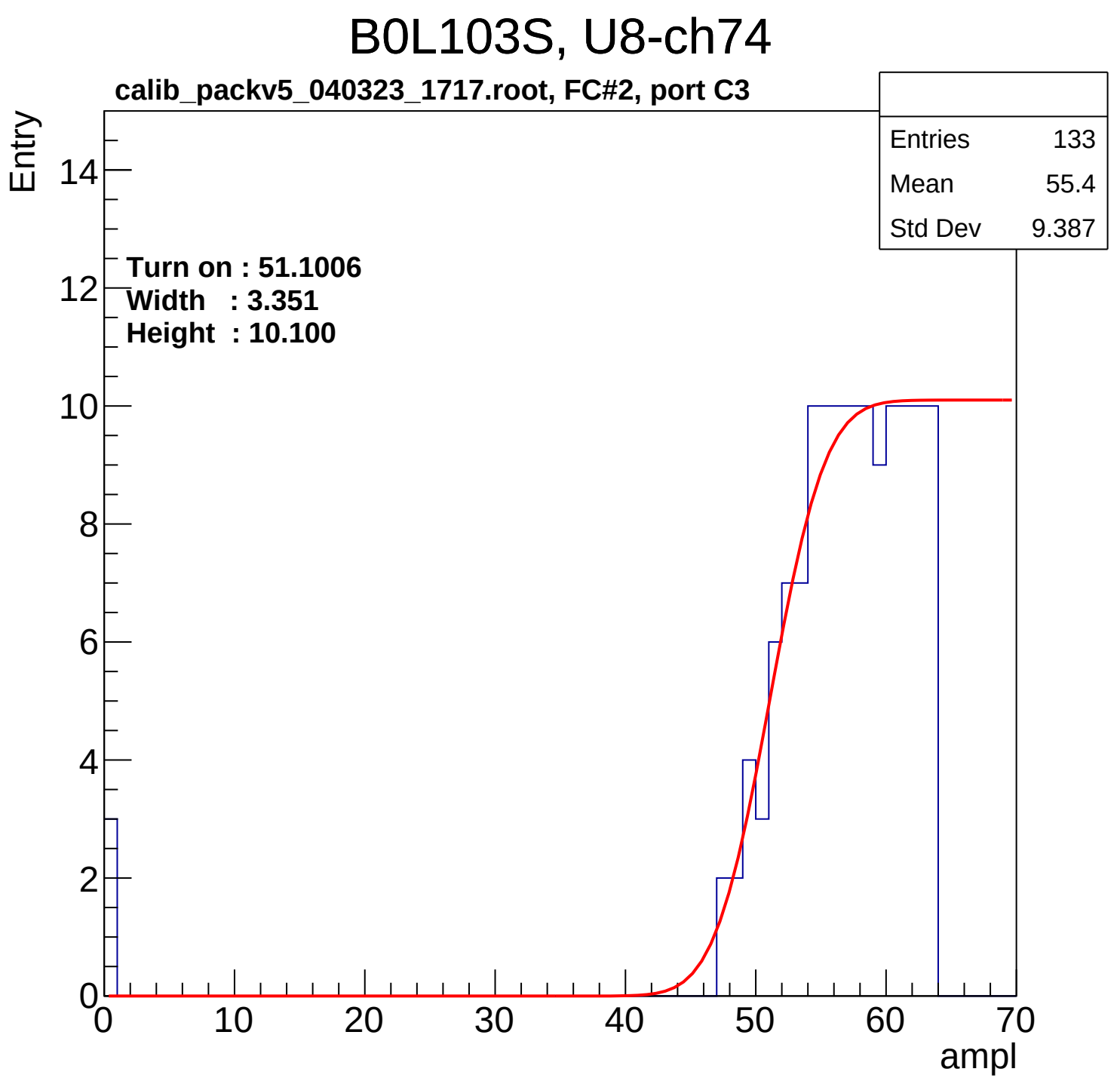
B0L103S, U8-ch74
calib_packv5_040323_1717.root, FC#2, port C3
Entries 133
Mean 55.4
Std Dev 9.387
Turn on : 51.1006
Width : 3.351
Height : 10.100
Entry
ampl
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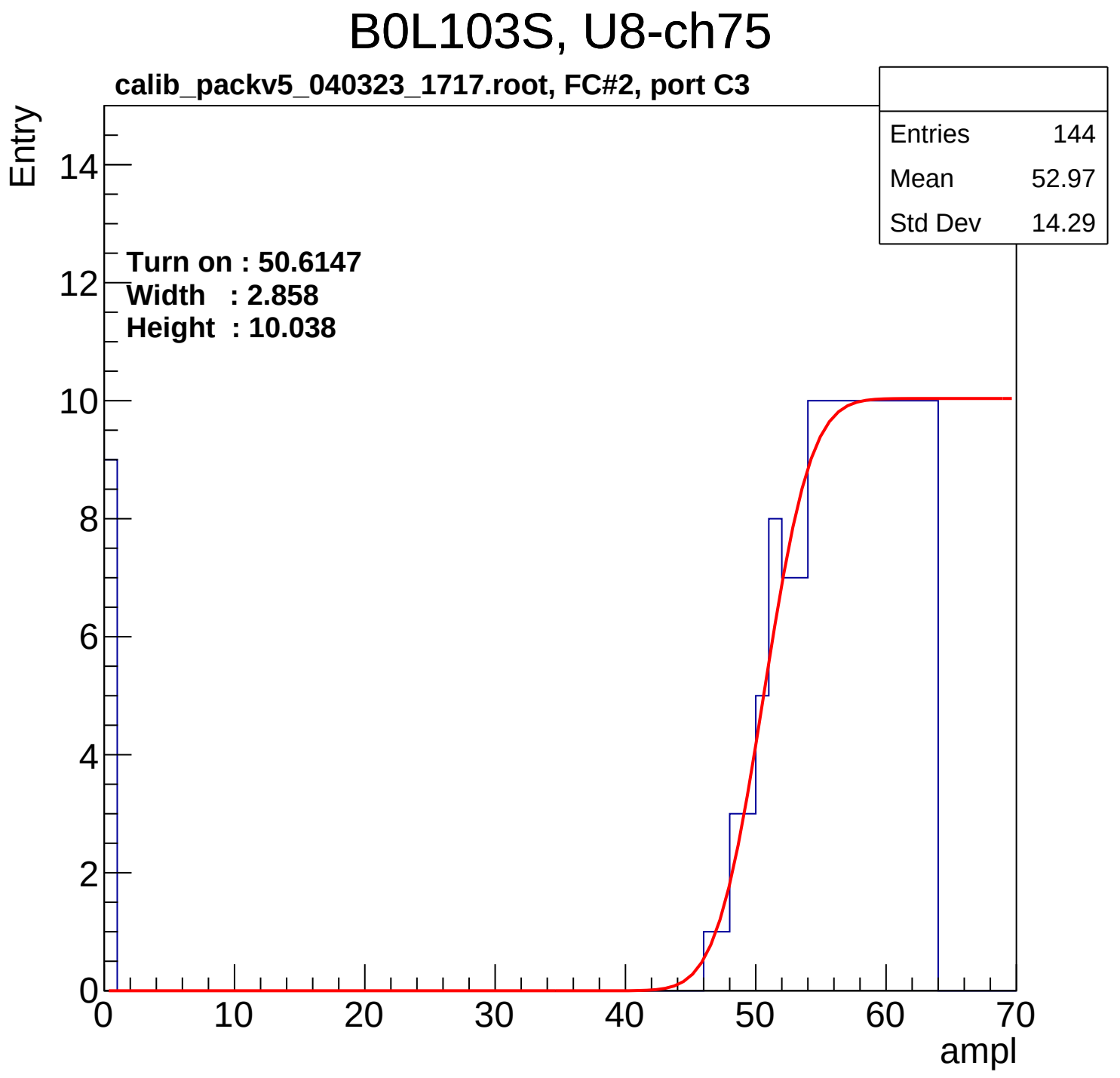
B0L103S, U8-ch75
calib_packv5_040323_1717.root, FC#2, port C3
Entries 144
Mean 52.97
Std Dev 14.29
Turn on : 50.6147
Width : 2.858
Height : 10.038
Entry
ampl
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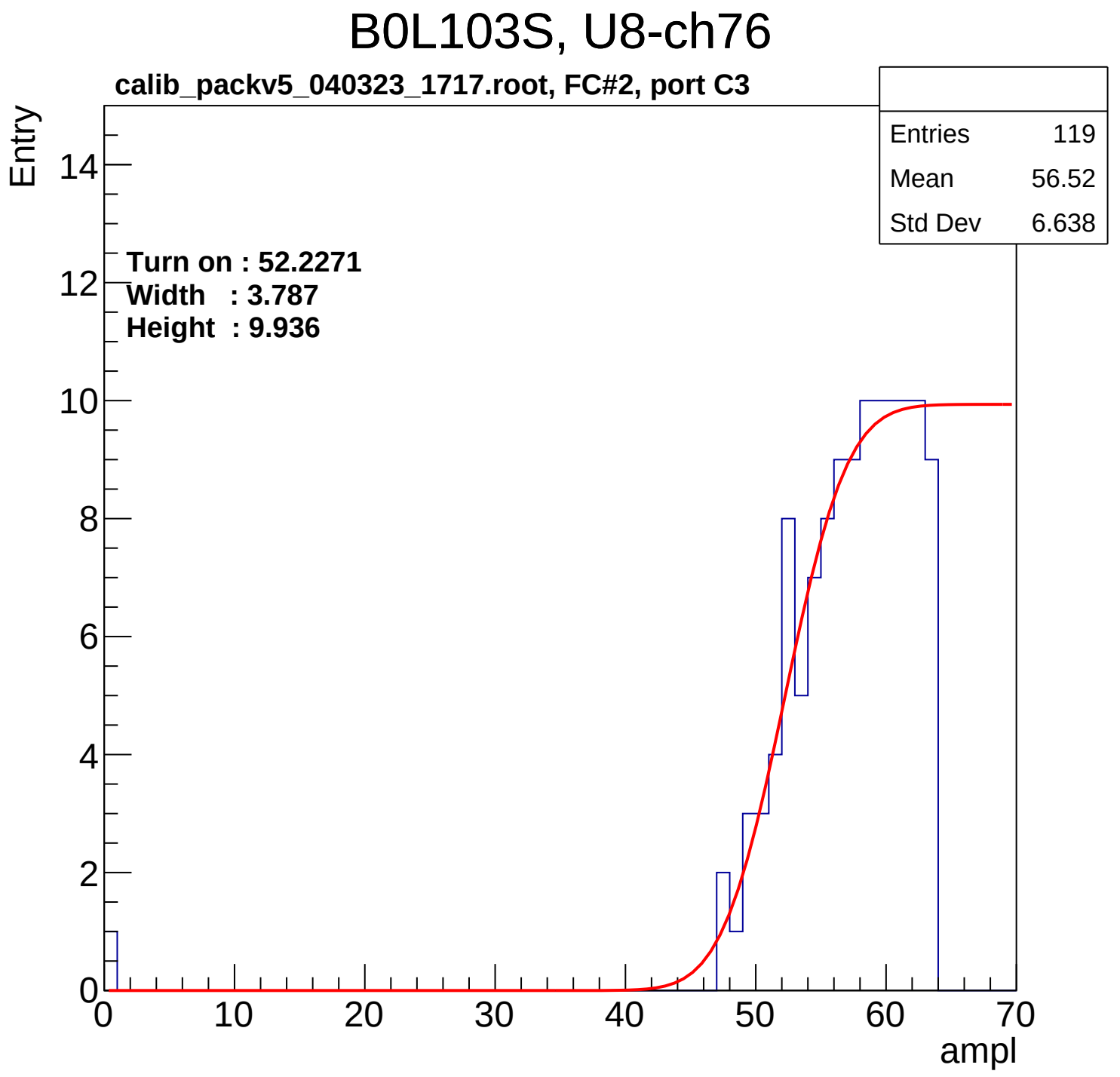
B0L103S, U8-ch76
calib_packv5_040323_1717.root, FC#2, port C3
Entries 119
Mean 56.52
Std Dev 6.638
Turn on : 52.2271
Width : 3.787
Height : 9.936
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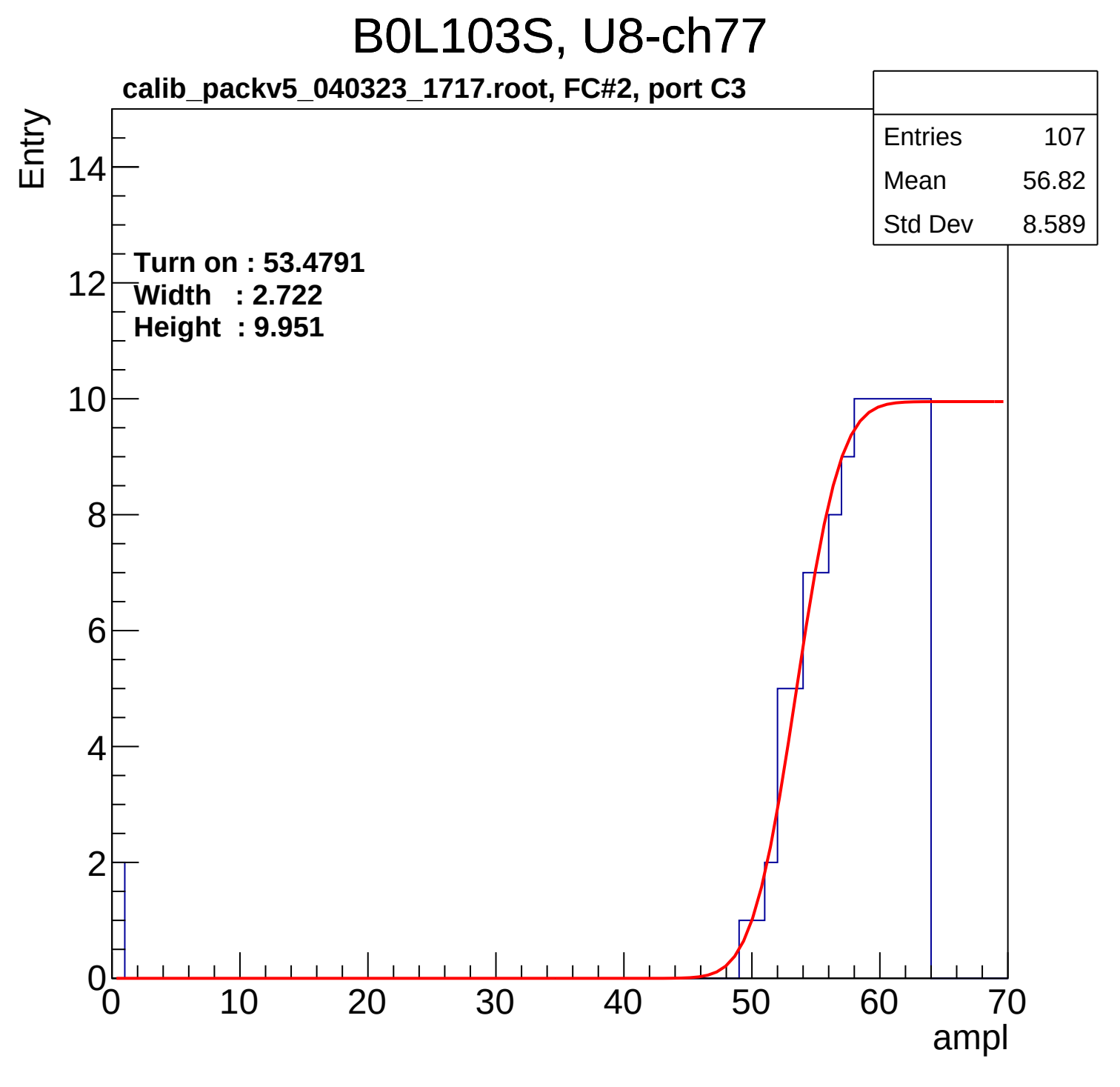
B0L103S, U8-ch77
calib_packv5_040323_1717.root, FC#2, port C3
Entries 107
Mean 56.82
Std Dev 8.589
Turn on : 53.4791
Width : 2.722
Height : 9.951
Entry
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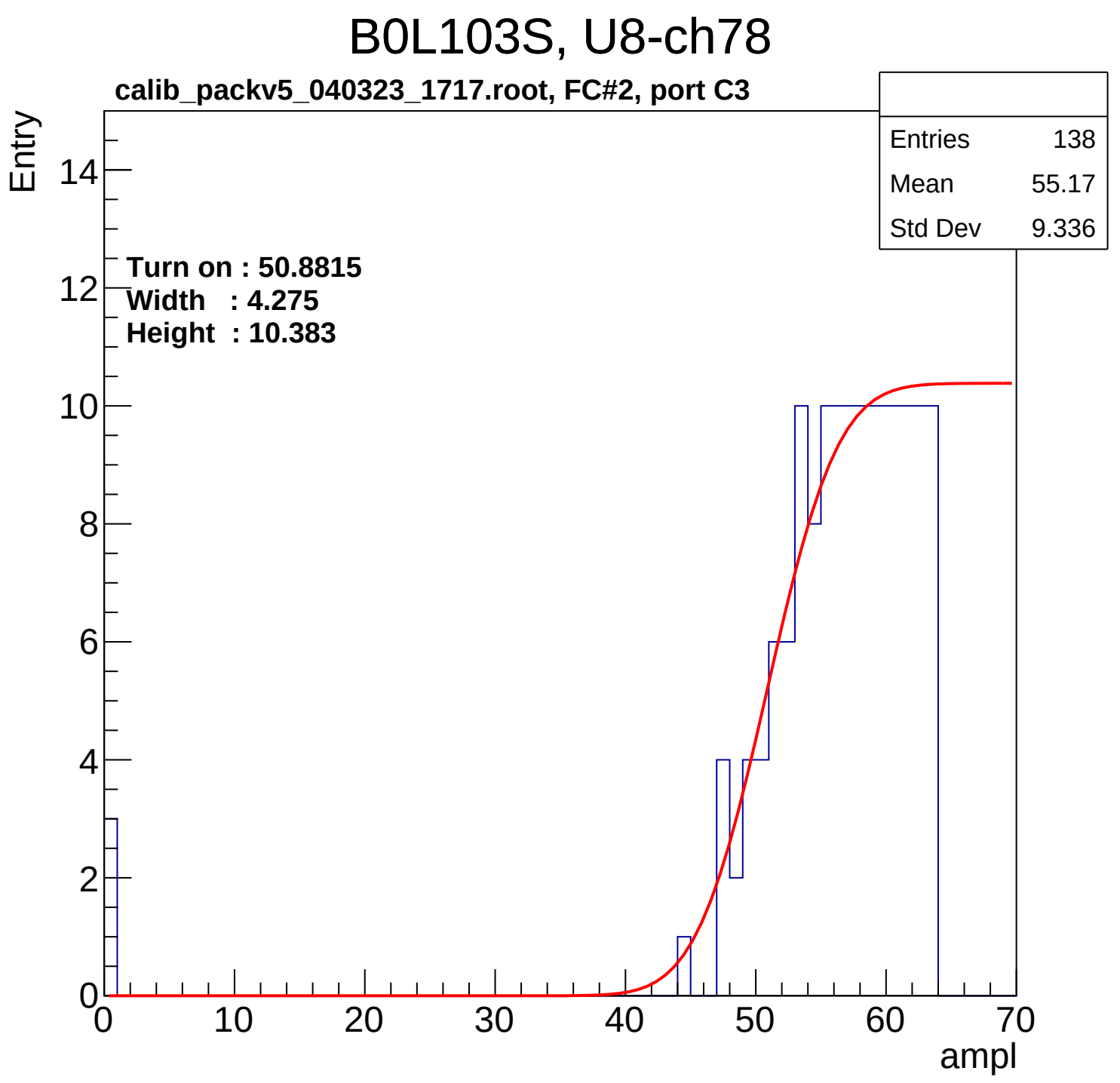
B0L103S, U8-ch78
calib_packv5_040323_1717.root, FC#2, port C3
Entries 138
Mean 55.17
Std Dev 9.336
Turn on : 50.8815
Width : 4.275
Height : 10.383
Entry
ampl
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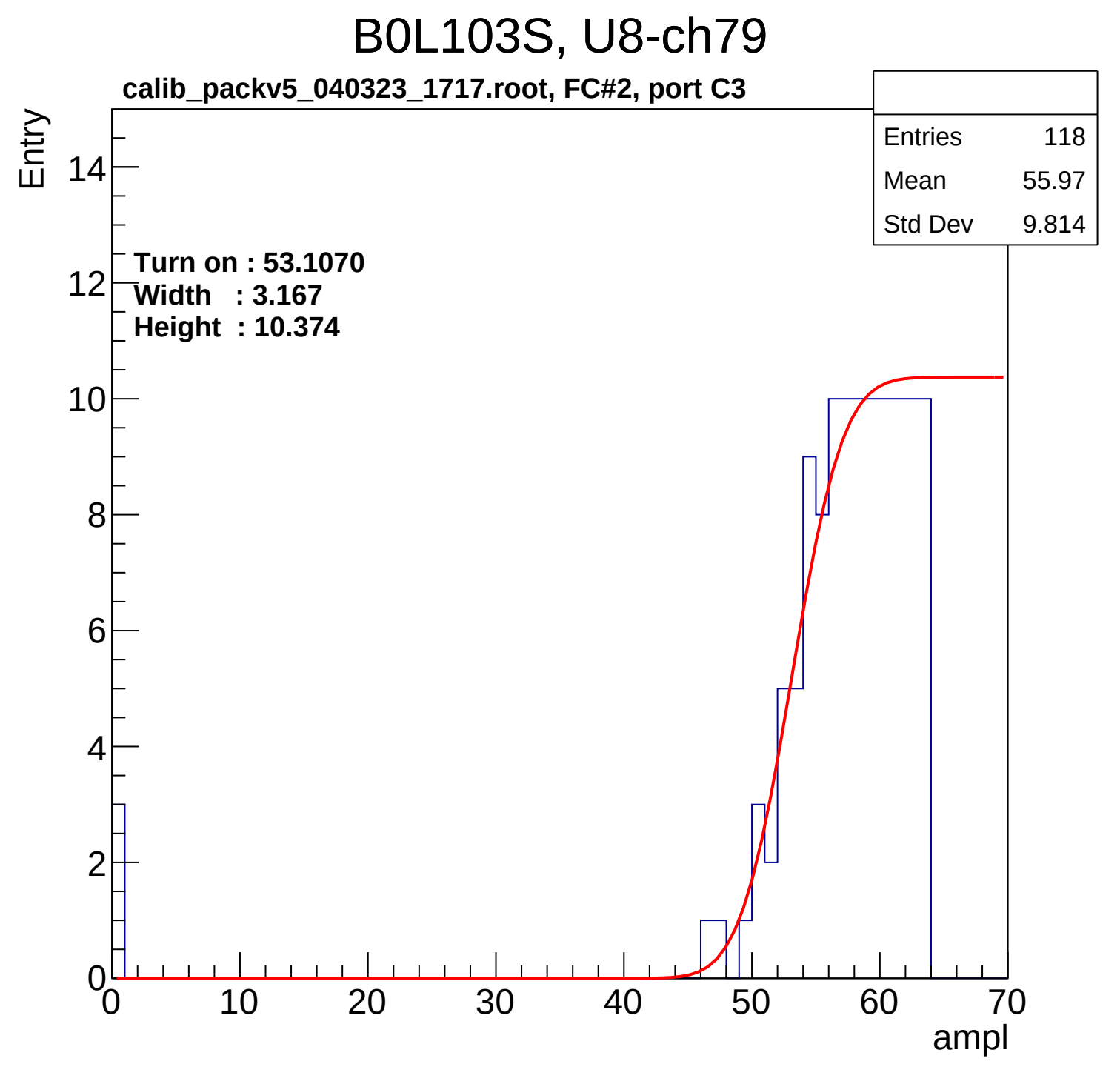
B0L103S, U8-ch79
calib_packv5_040323_1717.root, FC#2, port C3
Entries 118
Mean 55.97
Std Dev 9.814
Turn on : 53.1070
Width : 3.167
Height : 10.374
Entry
ampl
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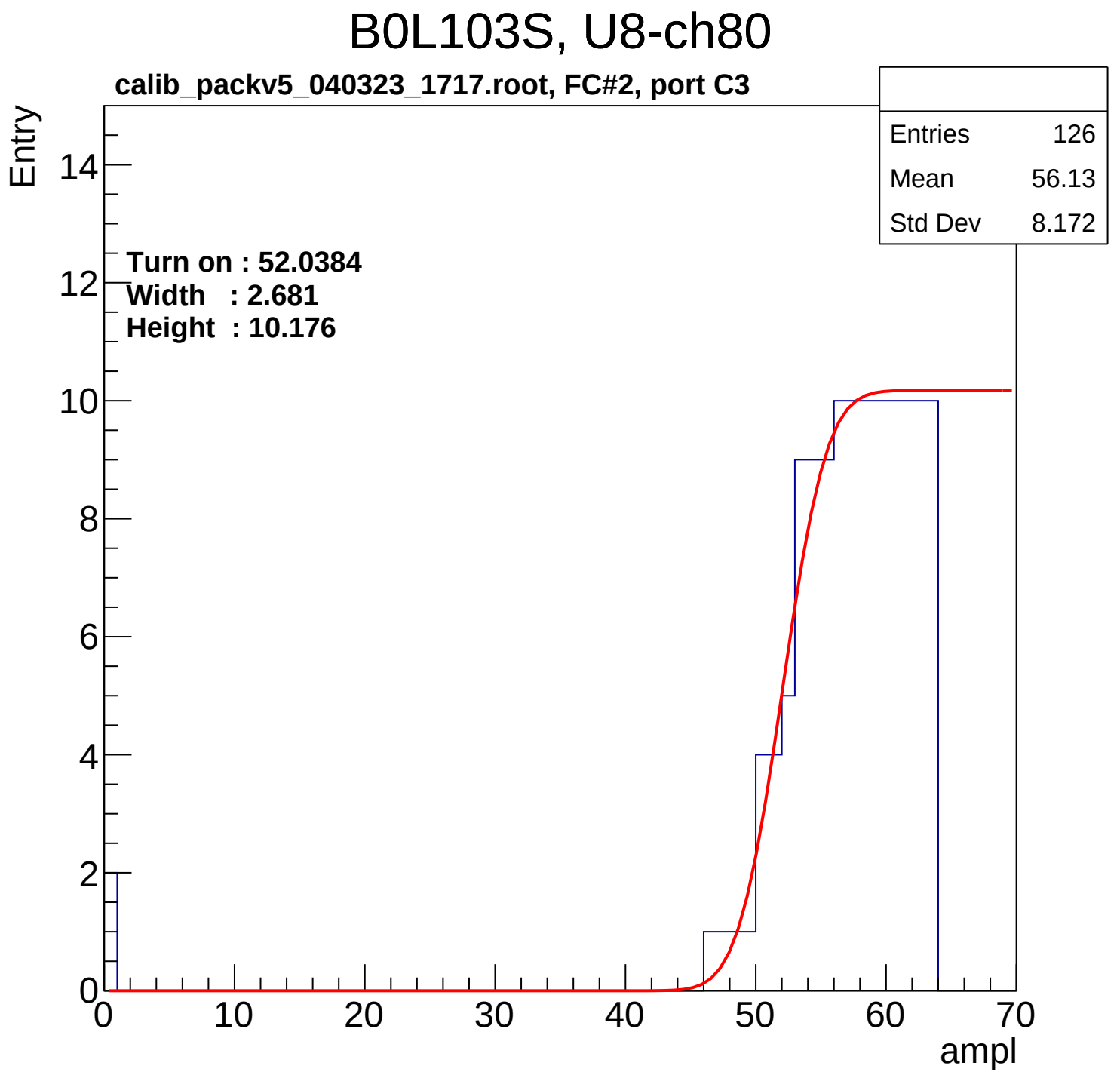
B0L103S, U8-ch80
calib_packv5_040323_1717.root, FC#2, port C3
Entries 126
Mean 56.13
Std Dev 8.172
Turn on : 52.0384
Width : 2.681
Height : 10.176
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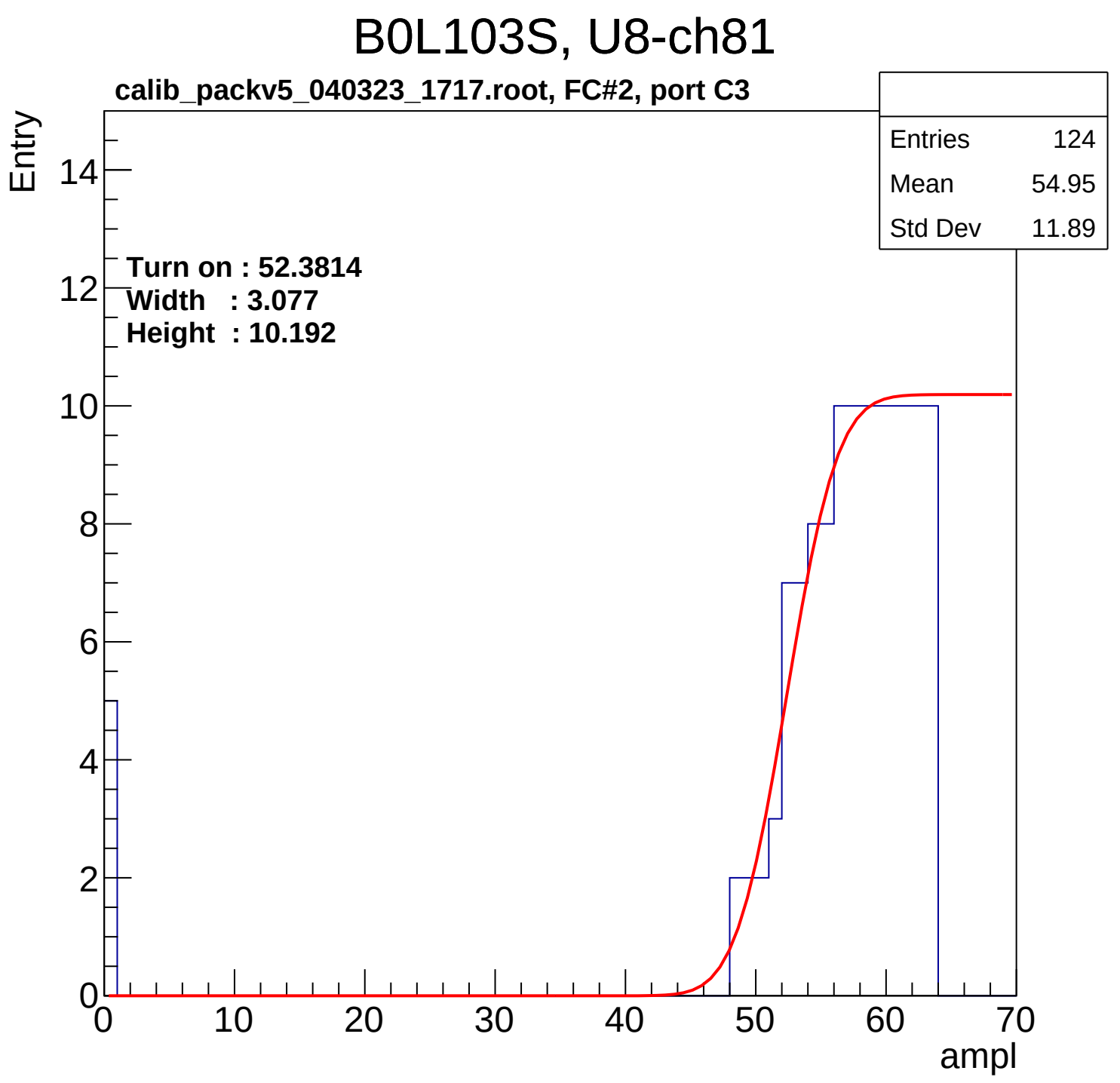
B0L103S, U8-ch81
calib_packv5_040323_1717.root, FC#2, port C3
Entries 124
Mean 54.95
Std Dev 11.89
Turn on : 52.3814
Width : 3.077
Height : 10.192
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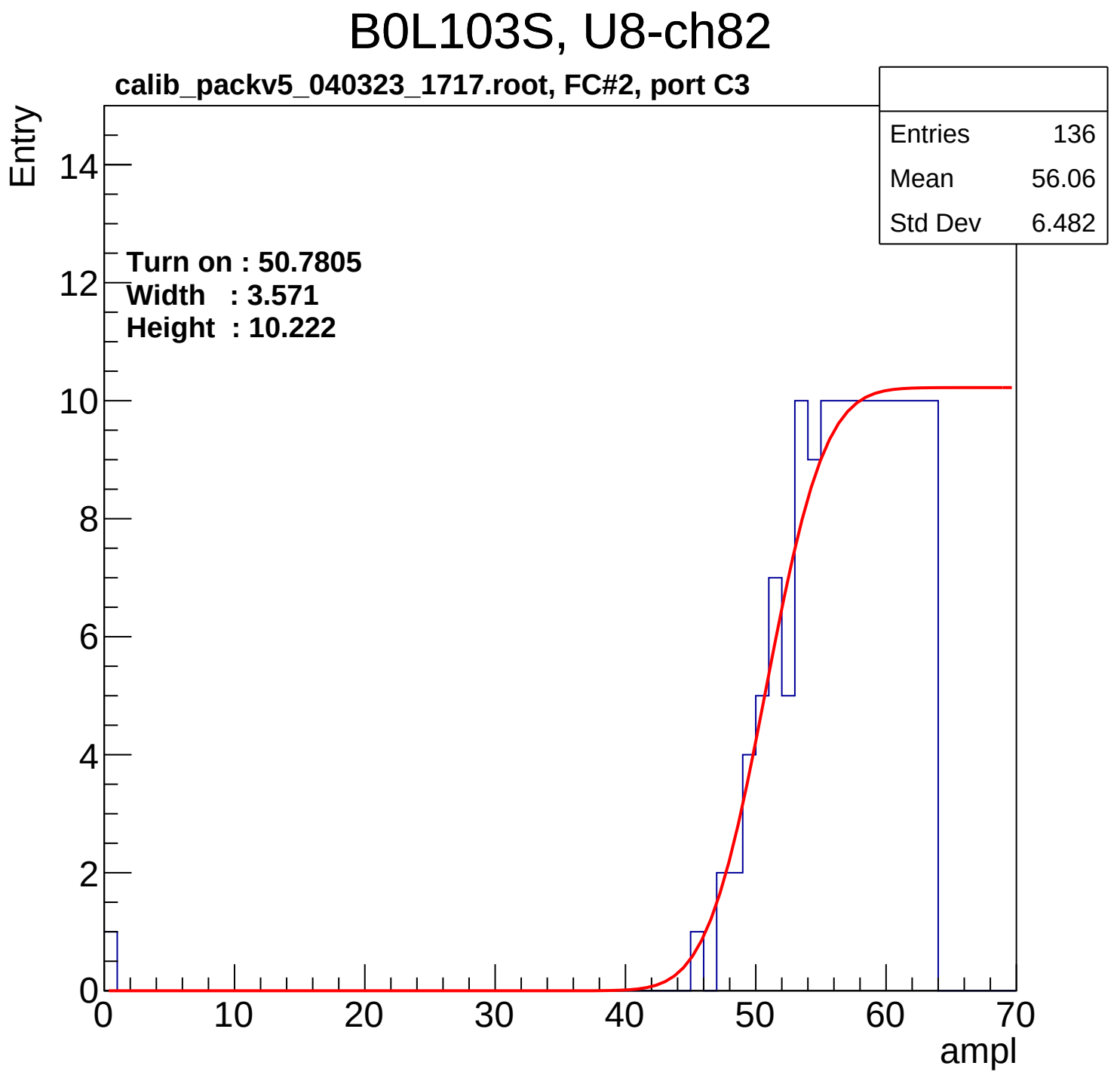
B0L103S, U8-ch82
calib_packv5_040323_1717.root, FC#2, port C3
Entries 136
Mean 56.06
Std Dev 6.482
Turn on : 50.7805
Width : 3.571
Height : 10.222
Entry
ampl
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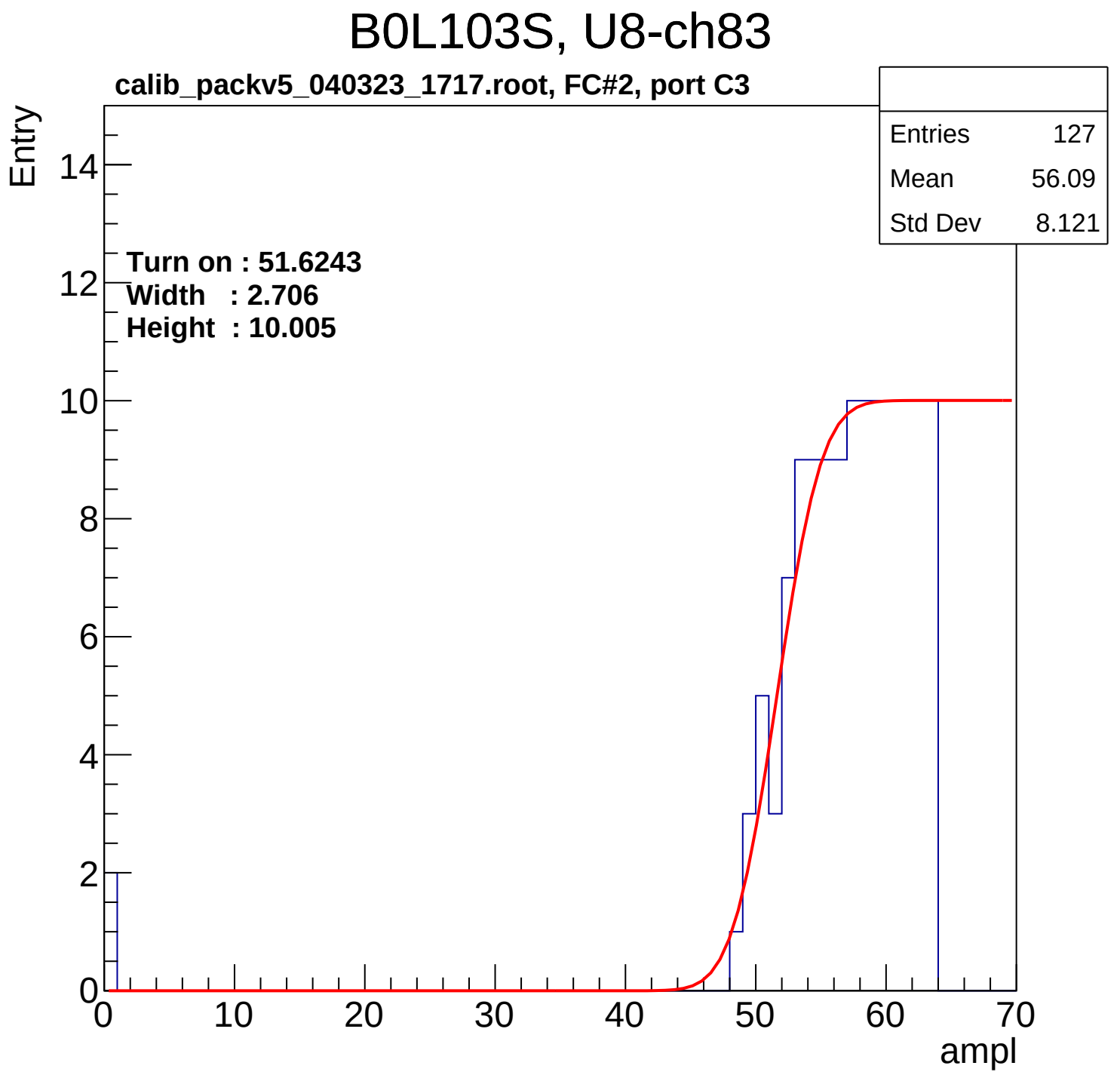
B0L103S, U8-ch83
calib_packv5_040323_1717.root, FC#2, port C3
Entries 127
Mean 56.09
Std Dev 8.121
Turn on : 51.6243
Width : 2.706
Height : 10.005
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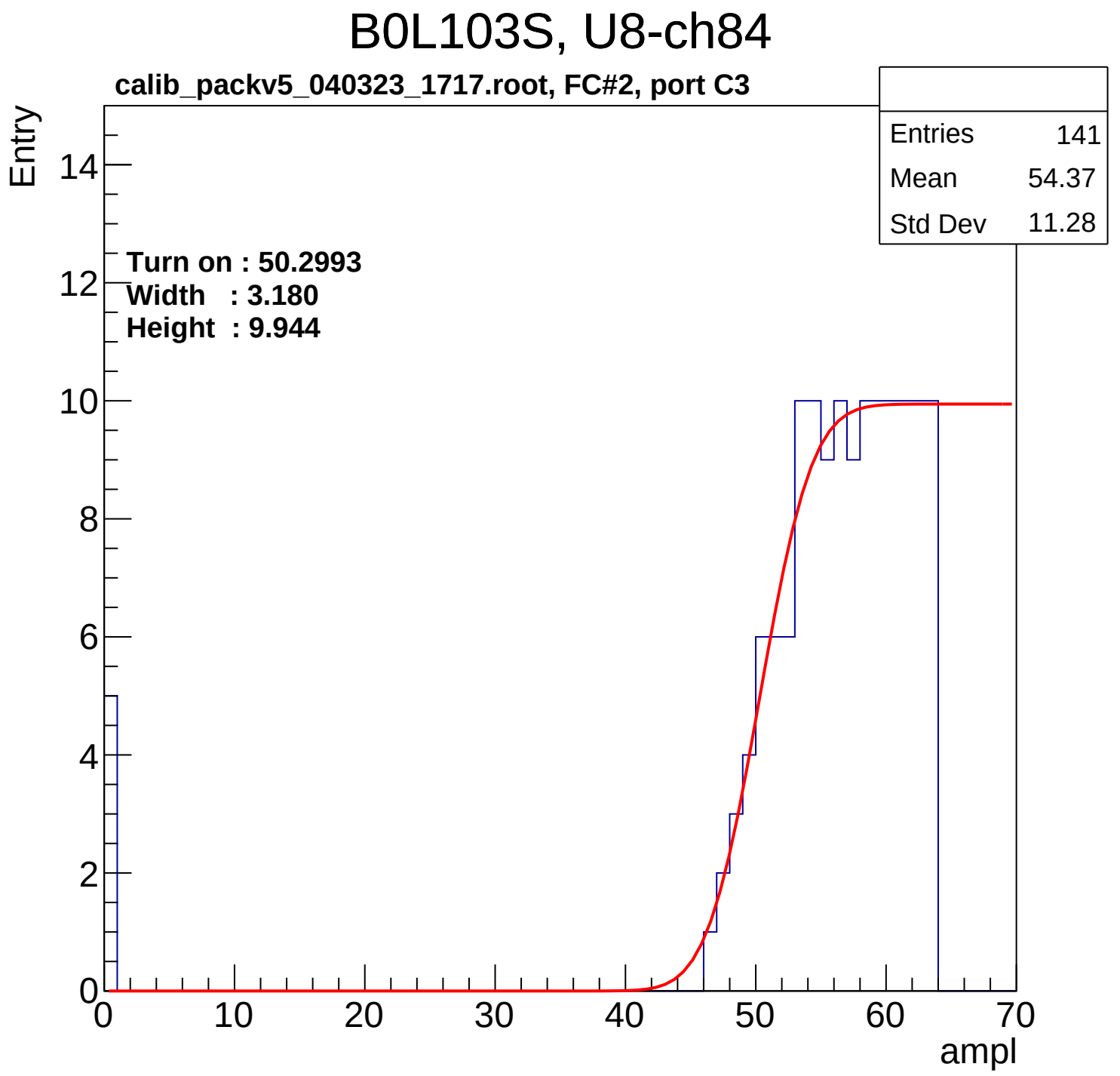
B0L103S, U8-ch84
calib_packv5_040323_1717.root, FC#2, port C3
Entries 141
Mean 54.37
Std Dev 11.28
Turn on : 50.2993
Width : 3.180
Height : 9.944
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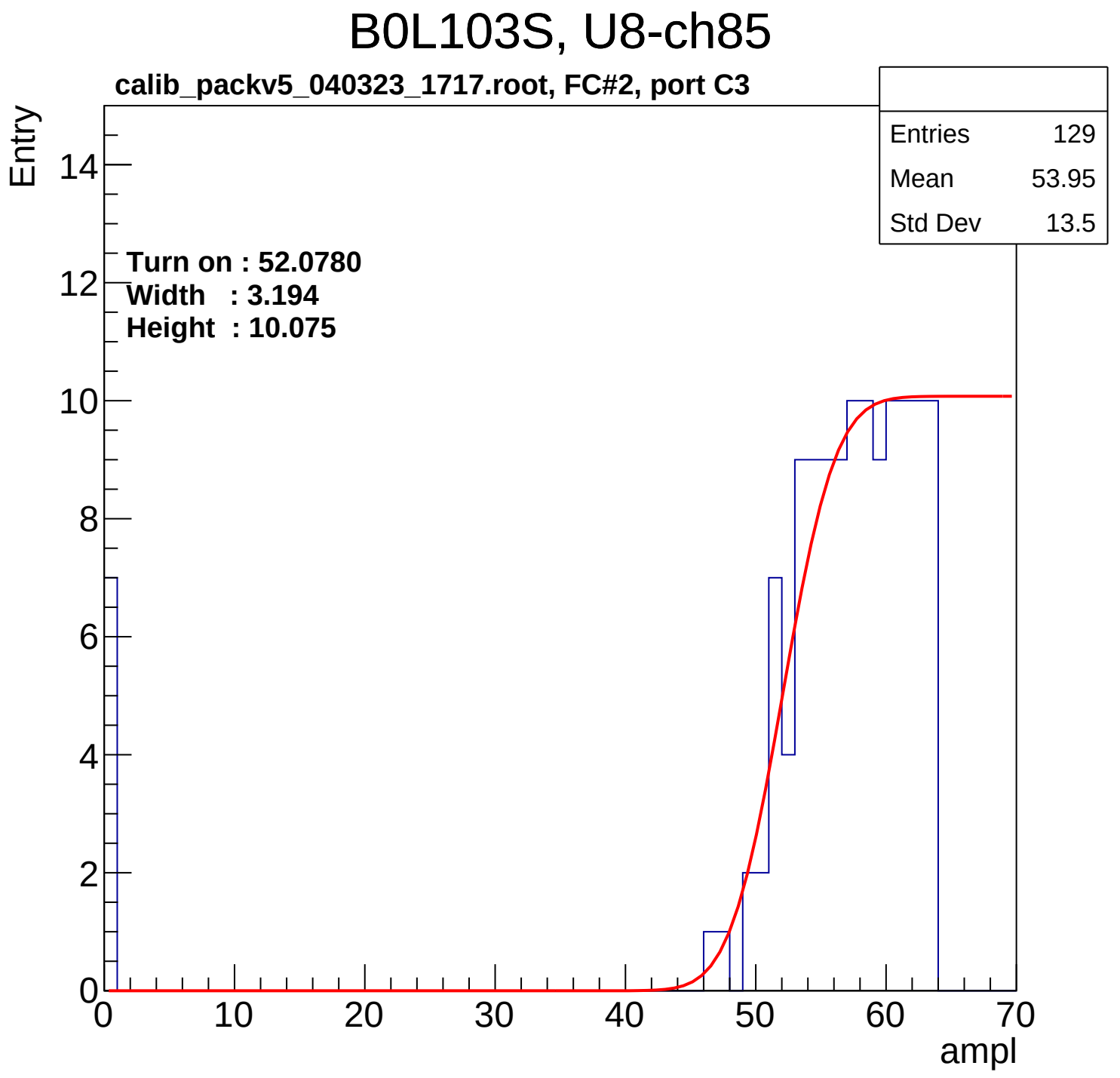
B0L103S, U8-ch85
calib_packv5_040323_1717.root, FC#2, port C3
Entries 129
Mean 53.95
Std Dev 13.5
Turn on : 52.0780
Width : 3.194
Height : 10.075
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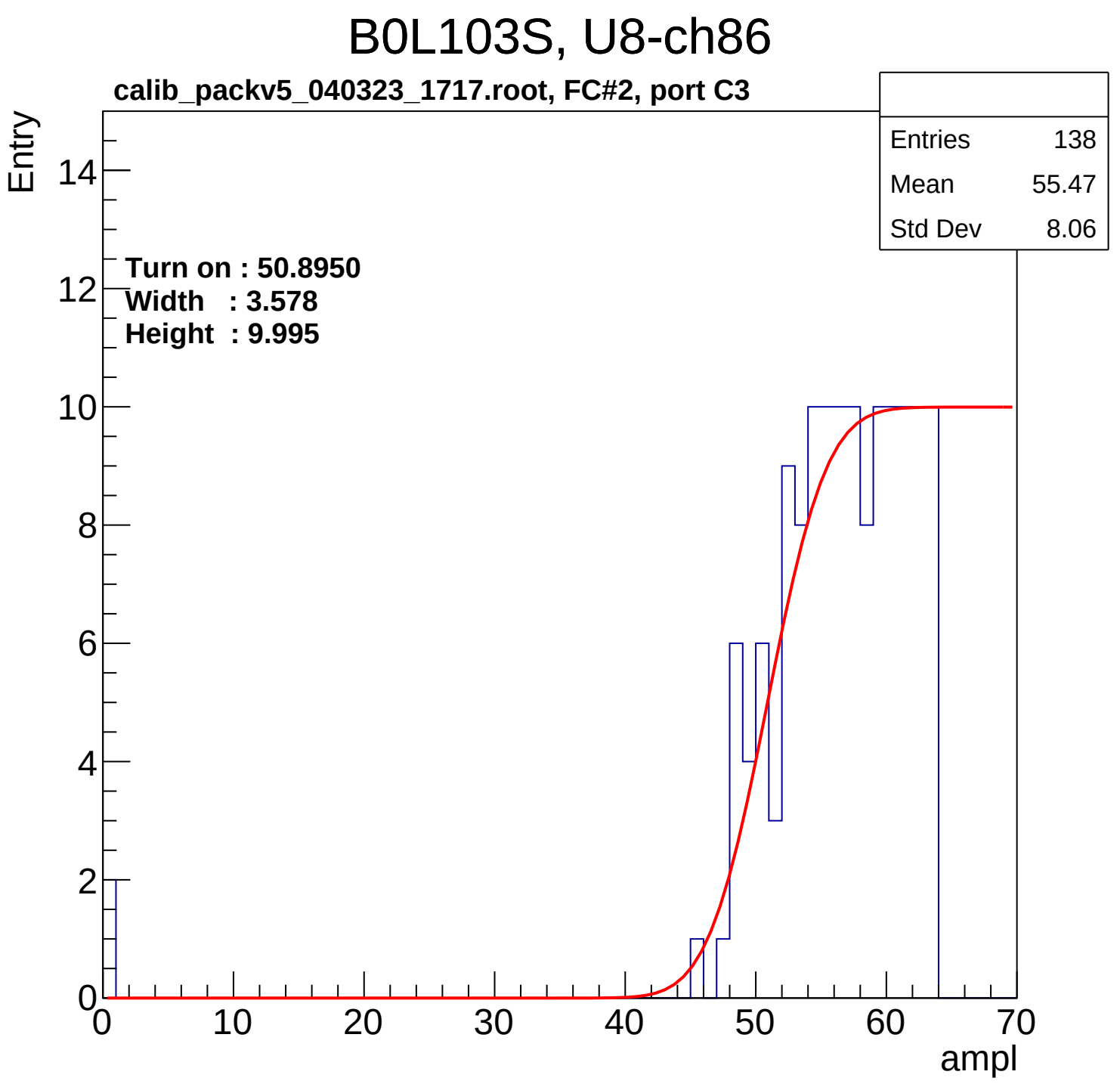
B0L103S, U8-ch86
calib_packv5_040323_1717.root, FC#2, port C3
Entries 138
Mean 55.47
Std Dev 8.06
Turn on : 50.8950
Width : 3.578
Height : 9.995
Entry
ampl
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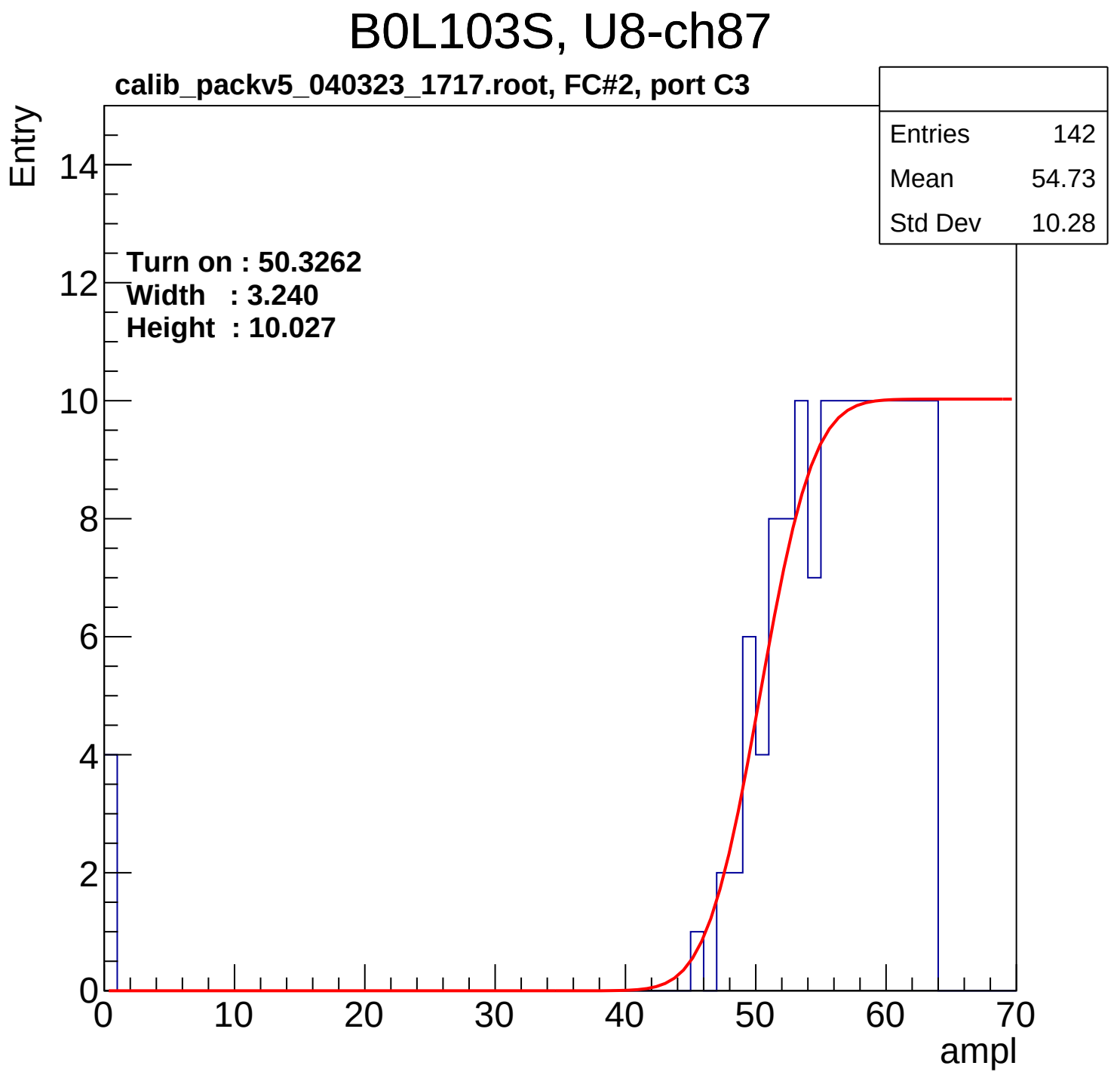
B0L103S, U8-ch87
calib_packv5_040323_1717.root, FC#2, port C3
Entries 142
Mean 54.73
Std Dev 10.28
Turn on : 50.3262
Width : 3.240
Height : 10.027
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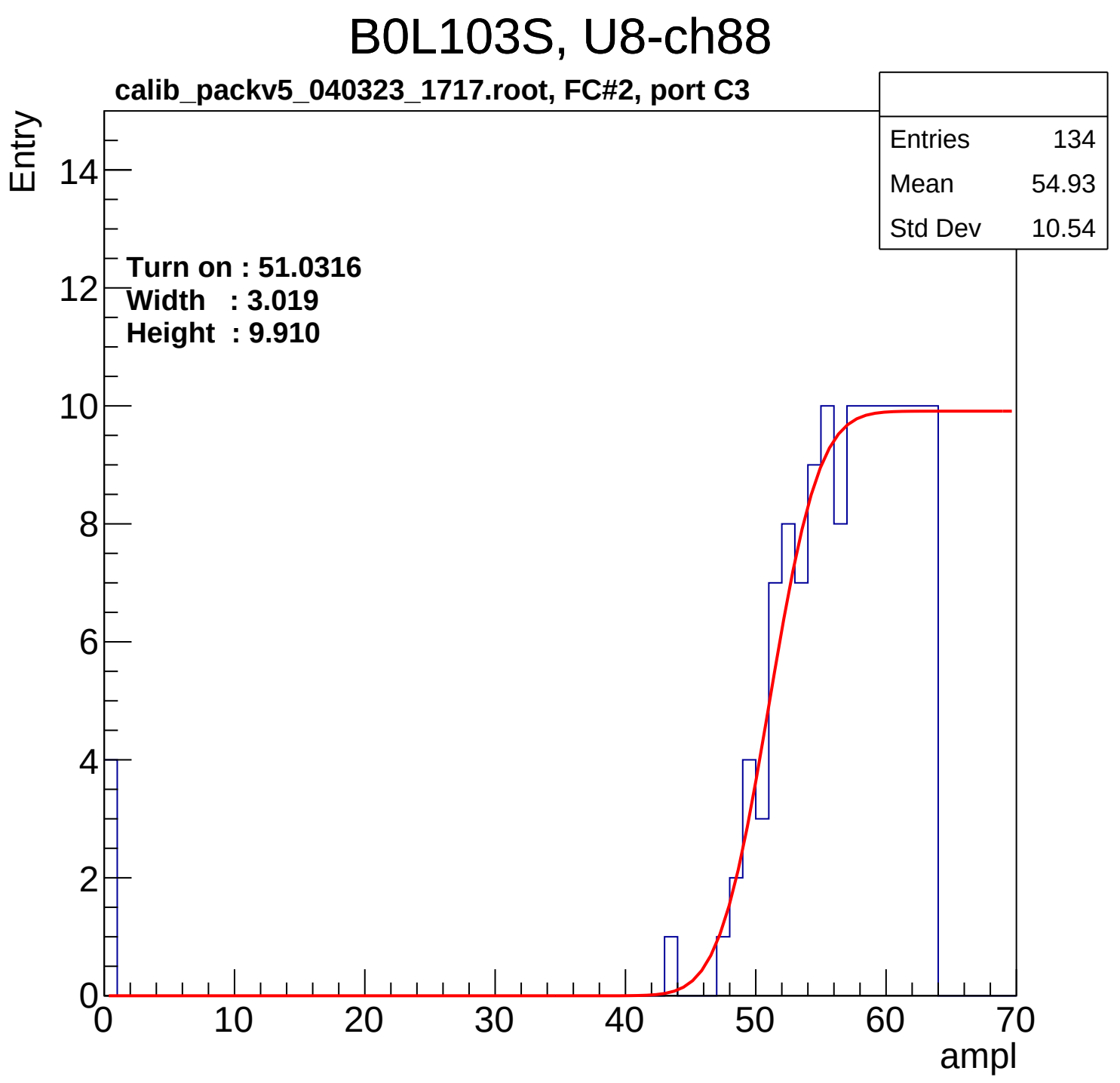
B0L103S, U8-ch88
calib_packv5_040323_1717.root, FC#2, port C3
Entries 134
Mean 54.93
Std Dev 10.54
Turn on : 51.0316
Width : 3.019
Height : 9.910
Entry
ampl
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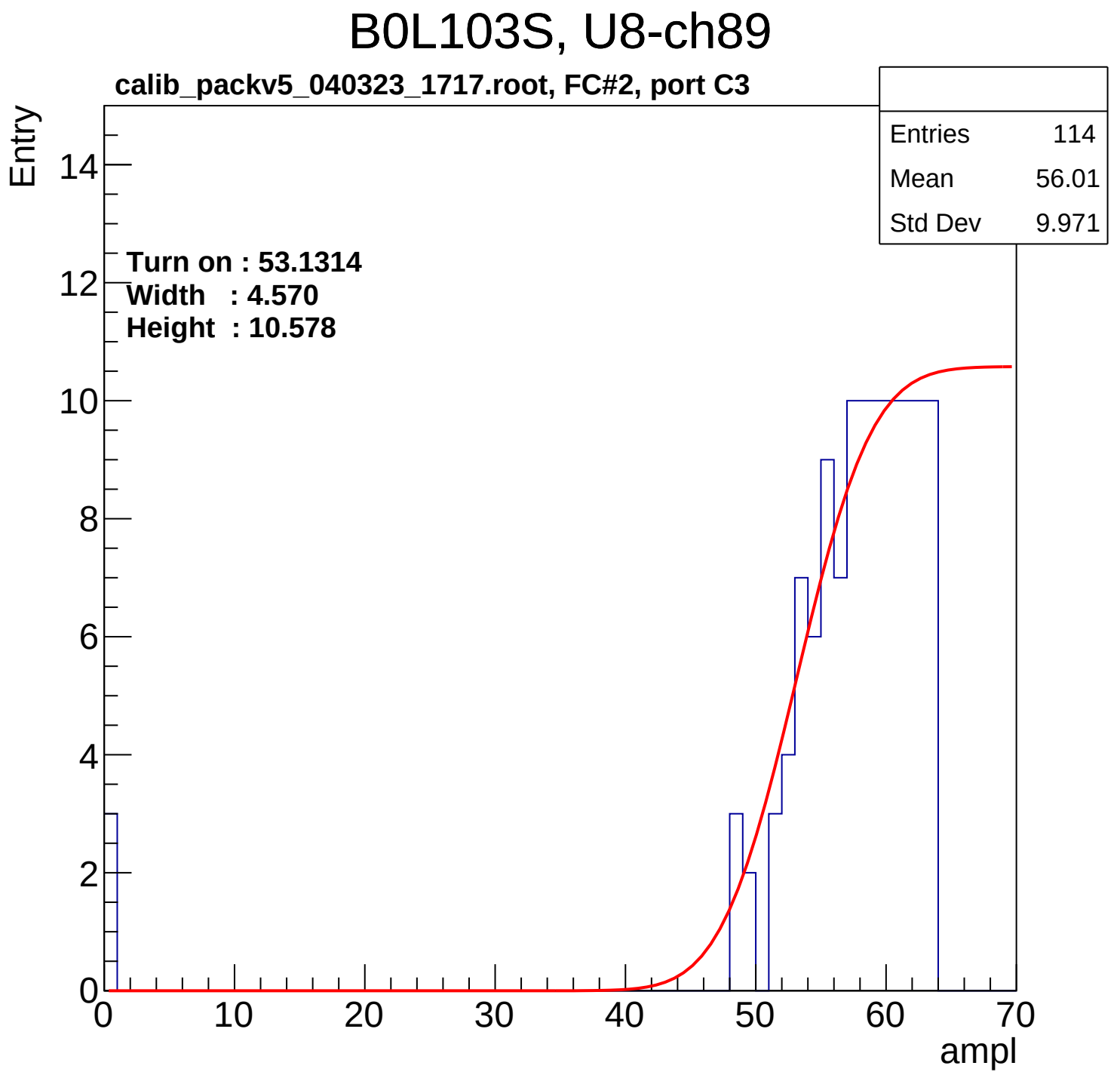
B0L103S, U8-ch89
calib_packv5_040323_1717.root, FC#2, port C3
Entries 114
Mean 56.01
Std Dev 9.971
Turn on : 53.1314
Width : 4.570
Height : 10.578
Entry
ampl
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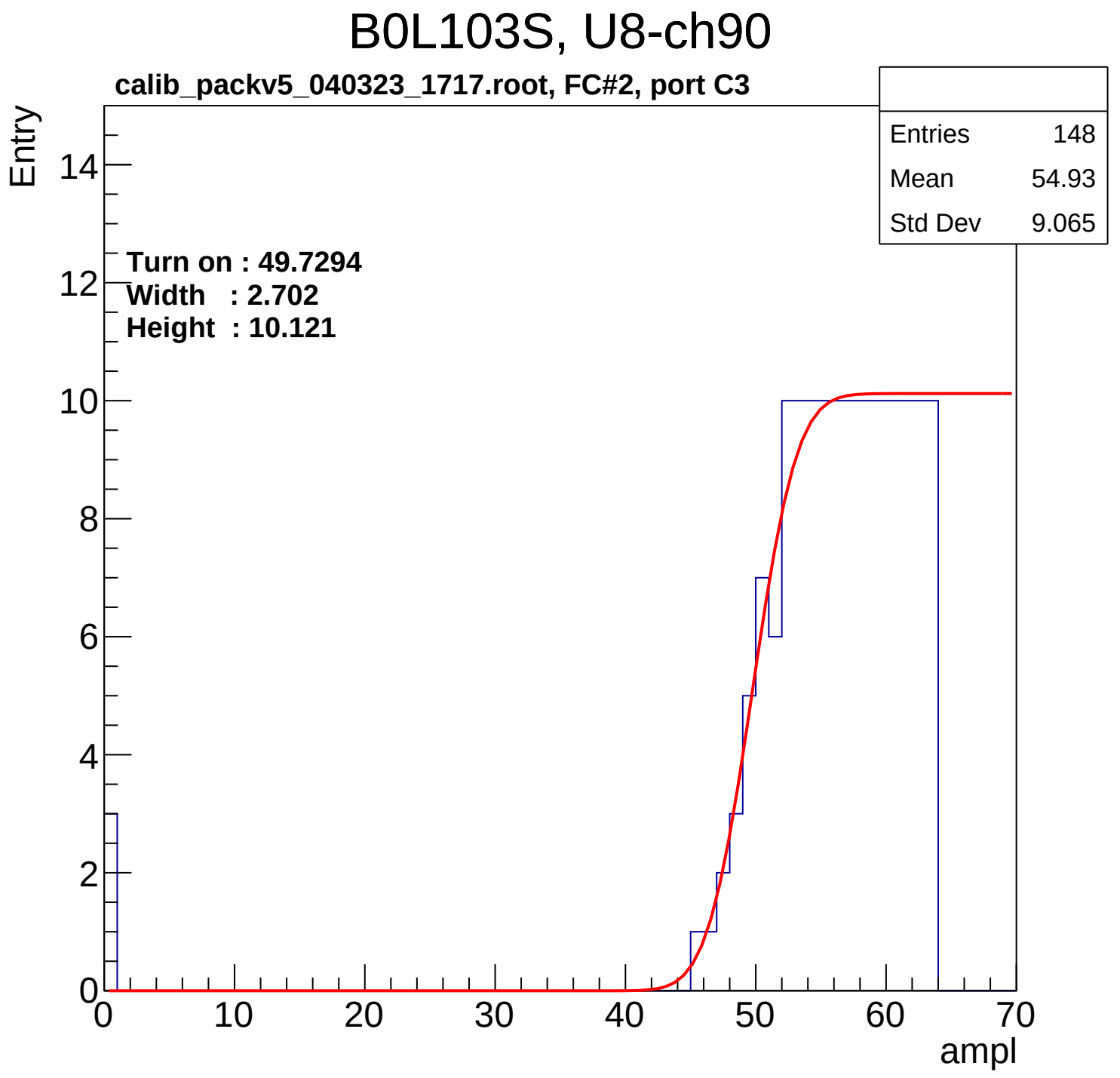
B0L103S, U8-ch90
calib_packv5_040323_1717.root, FC#2, port C3
Entries 148
Mean 54.93
Std Dev 9.065
Turn on : 49.7294
Width : 2.702
Height : 10.121
Entry
ampl
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2
4
6
8
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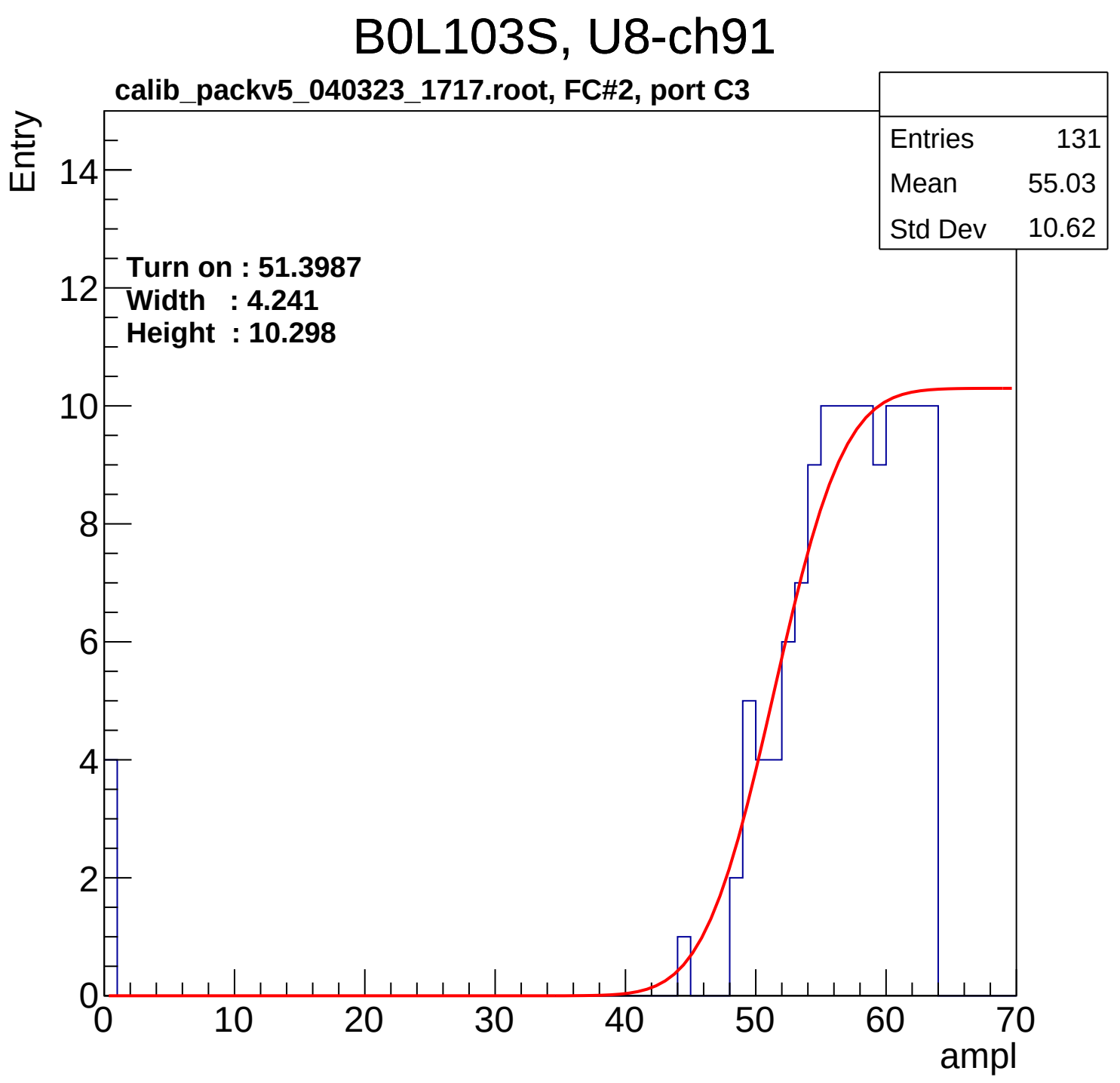
B0L103S, U8-ch91
calib_packv5_040323_1717.root, FC#2, port C3
Entries 131
Mean 55.03
Std Dev 10.62
Turn on : 51.3987
Width : 4.241
Height : 10.298
Entry
ampl
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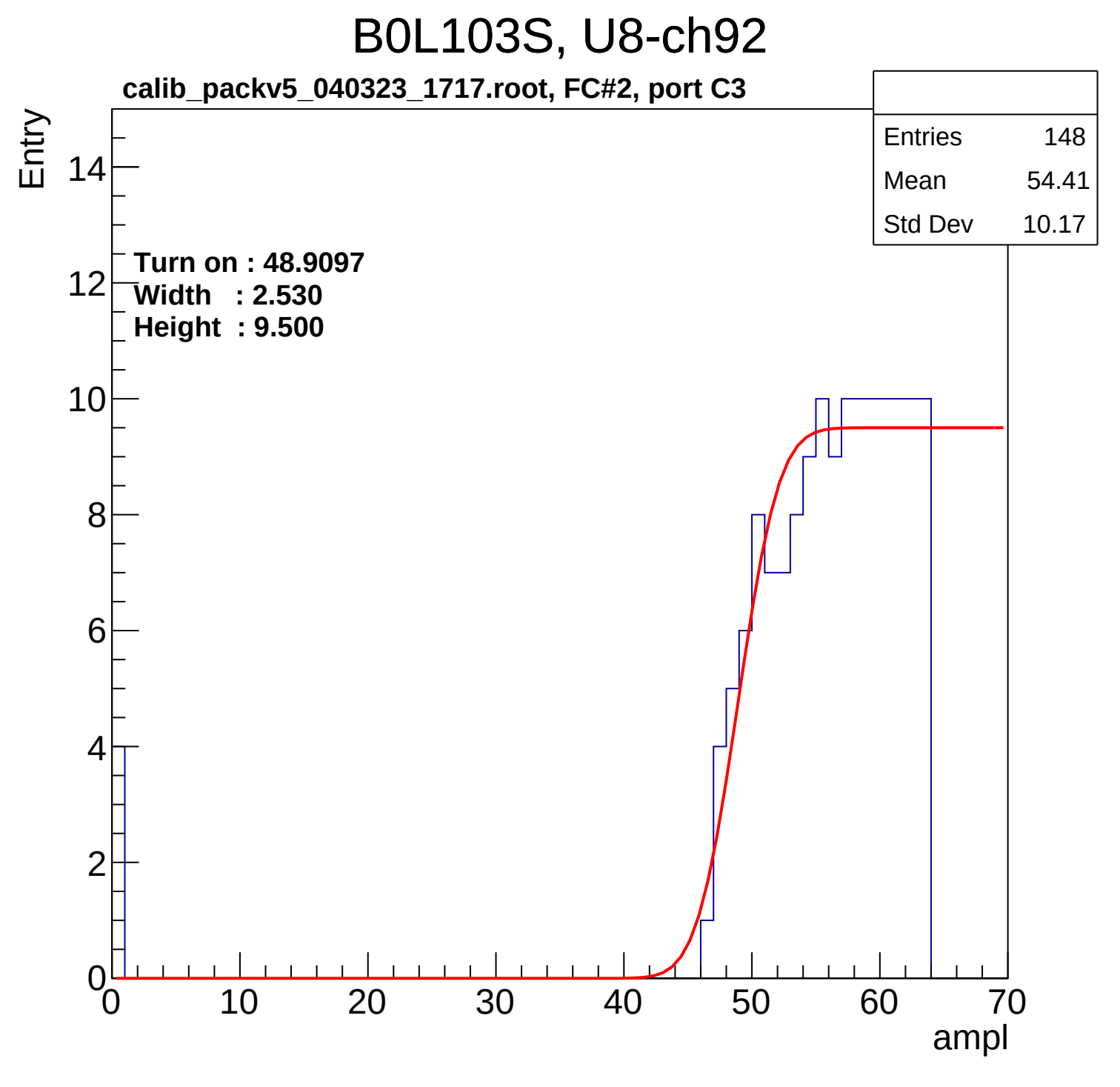
B0L103S, U8-ch92
calib_packv5_040323_1717.root, FC#2, port C3
Entries 148
Mean 54.41
Std Dev 10.17
Turn on : 48.9097
Width : 2.530
Height : 9.500
Entry
ampl
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2
4
6
8
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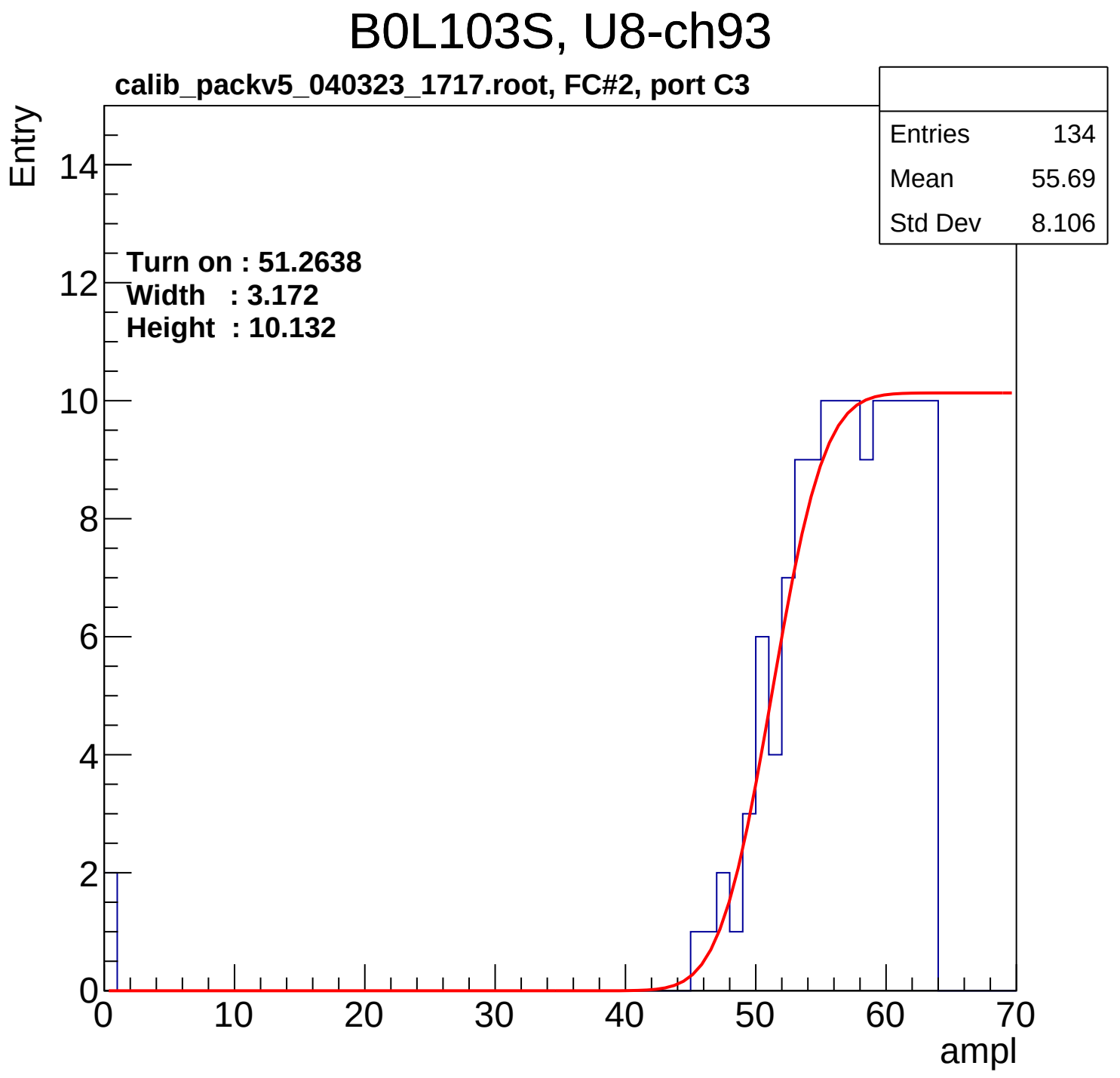
B0L103S, U8-ch93
calib_packv5_040323_1717.root, FC#2, port C3
Entries 134
Mean 55.69
Std Dev 8.106
Turn on : 51.2638
Width : 3.172
Height : 10.132
Entry
ampl
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8
10
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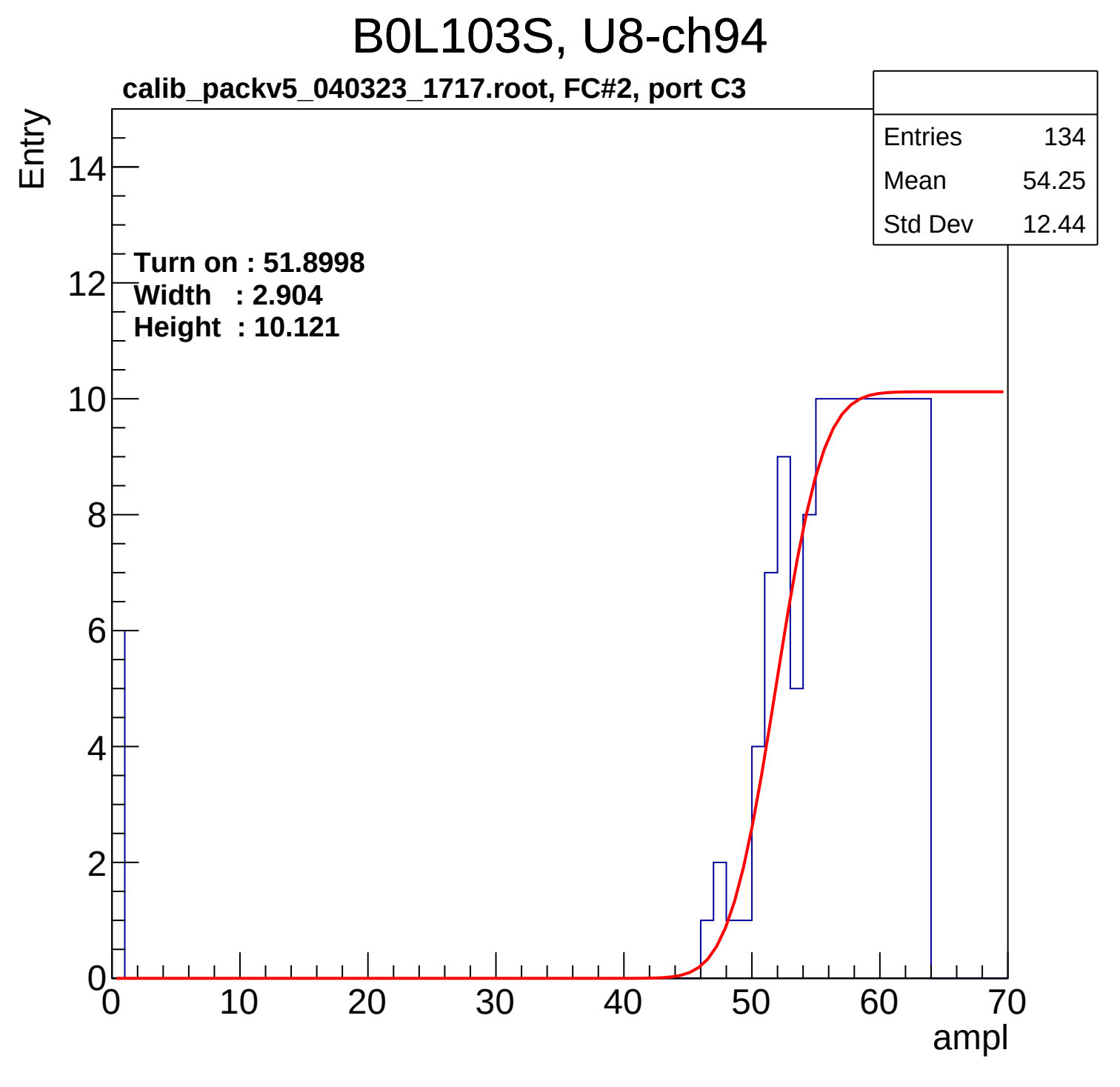
B0L103S, U8-ch94
calib_packv5_040323_1717.root, FC#2, port C3
Entries 134
Mean 54.25
Std Dev 12.44
Turn on : 51.8998
Width : 2.904
Height : 10.121
Entry
ampl
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2
4
6
8
10
12
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0
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60
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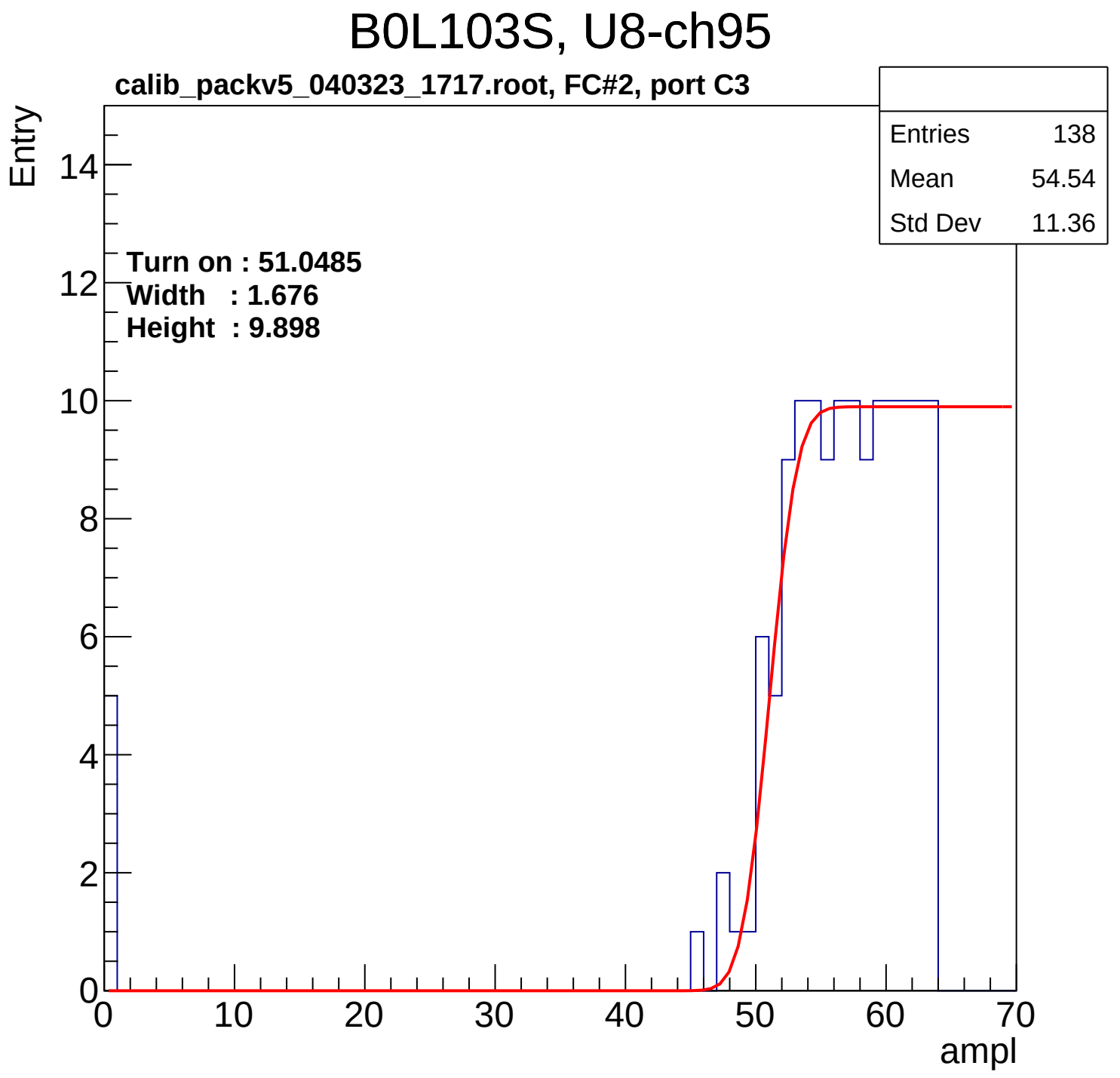
B0L103S, U8-ch95
calib_packv5_040323_1717.root, FC#2, port C3
Entries 138
Mean 54.54
Std Dev 11.36
Turn on : 51.0485
Width : 1.676
Height : 9.898
Entry
ampl
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4
6
8
10
12
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0
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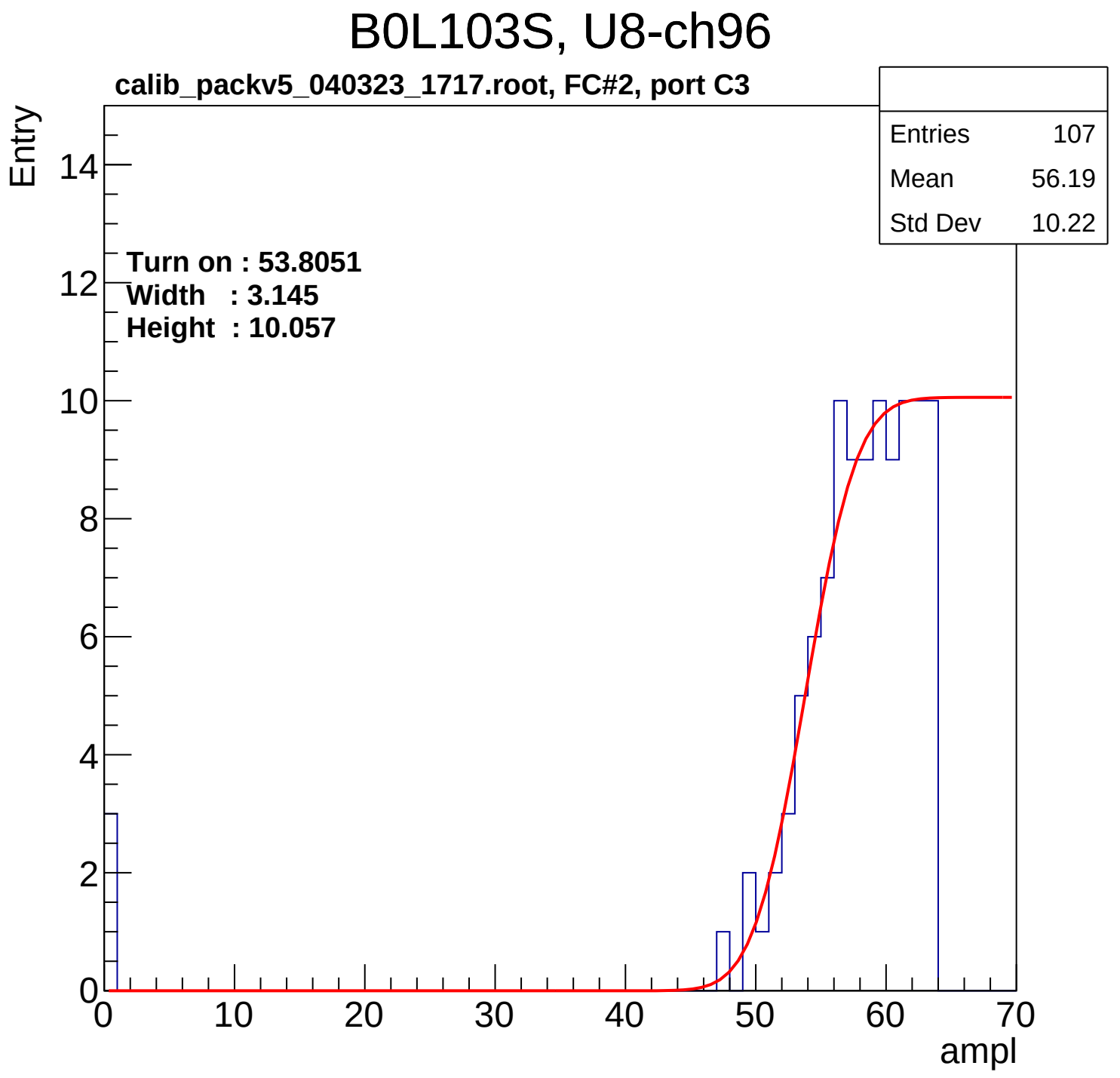
B0L103S, U8-ch96
calib_packv5_040323_1717.root, FC#2, port C3
Entries 107
Mean 56.19
Std Dev 10.22
Turn on : 53.8051
Width : 3.145
Height : 10.057
Entry
ampl
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4
6
8
10
12
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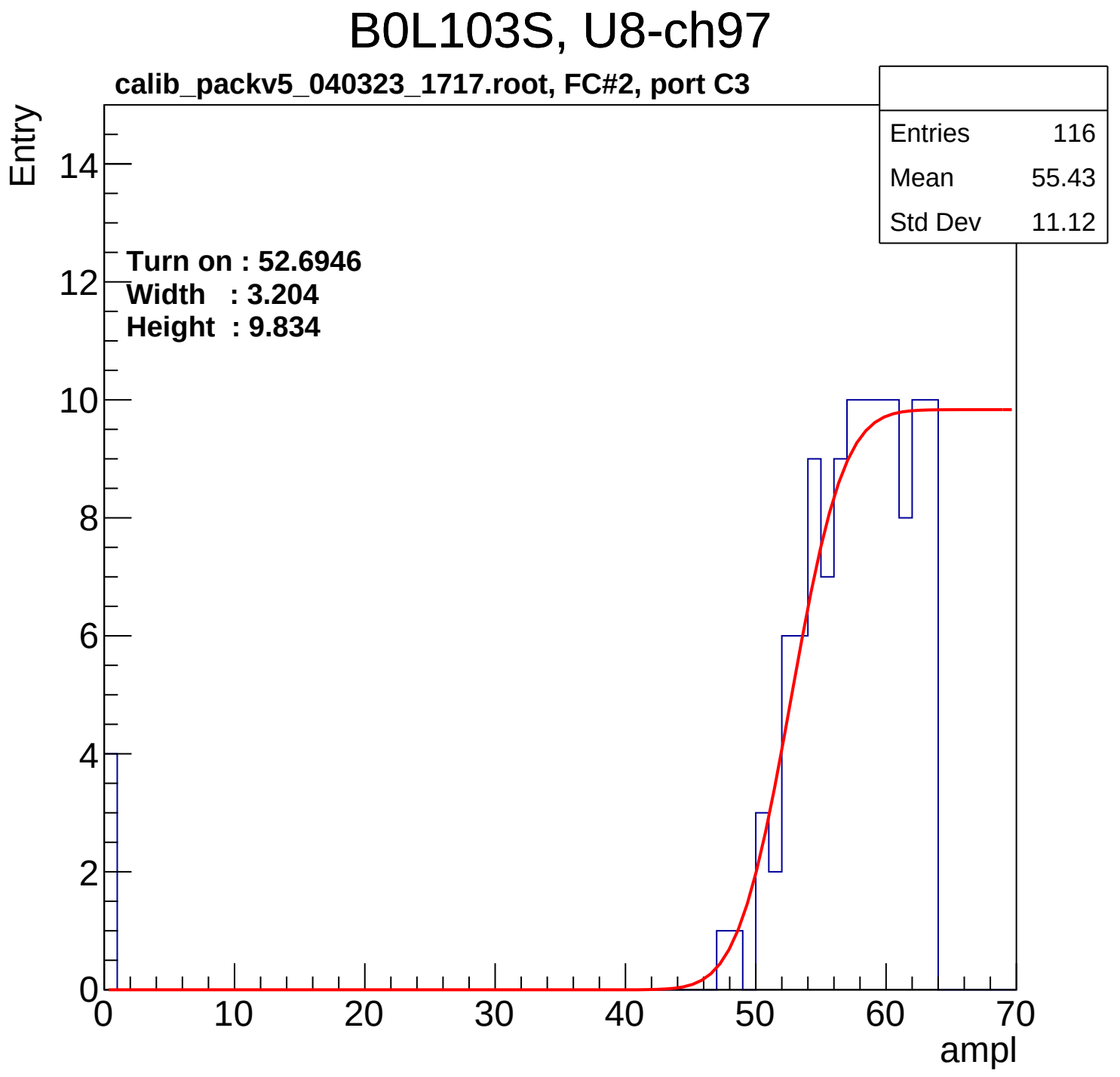
B0L103S, U8-ch97
calib_packv5_040323_1717.root, FC#2, port C3
Entries 116
Mean 55.43
Std Dev 11.12
Turn on : 52.6946
Width : 3.204
Height : 9.834
Entry
ampl
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6
8
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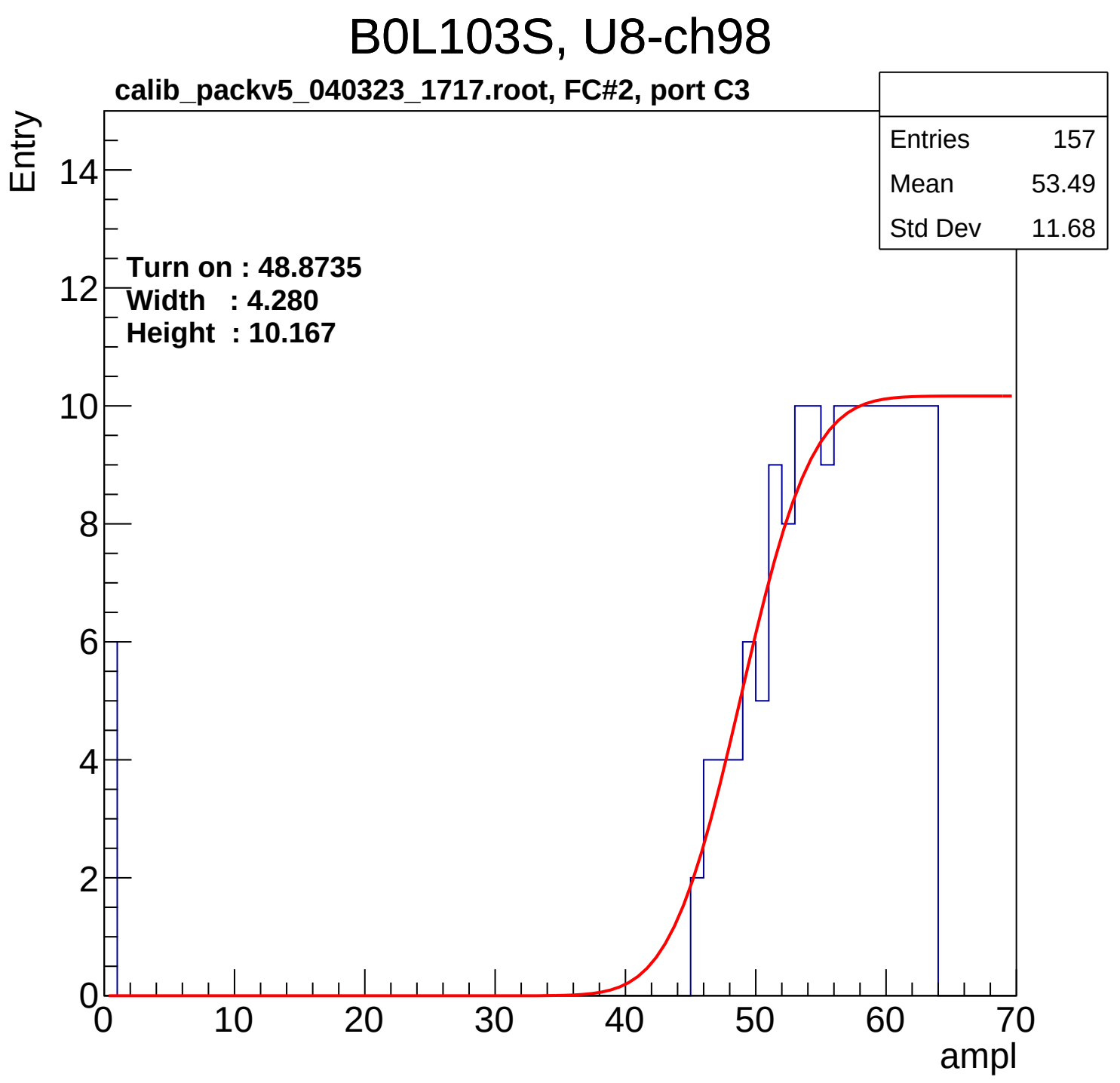
B0L103S, U8-ch98
calib_packv5_040323_1717.root, FC#2, port C3
Entries 157
Mean 53.49
Std Dev 11.68
Turn on : 48.8735
Width : 4.280
Height : 10.167
Entry
ampl
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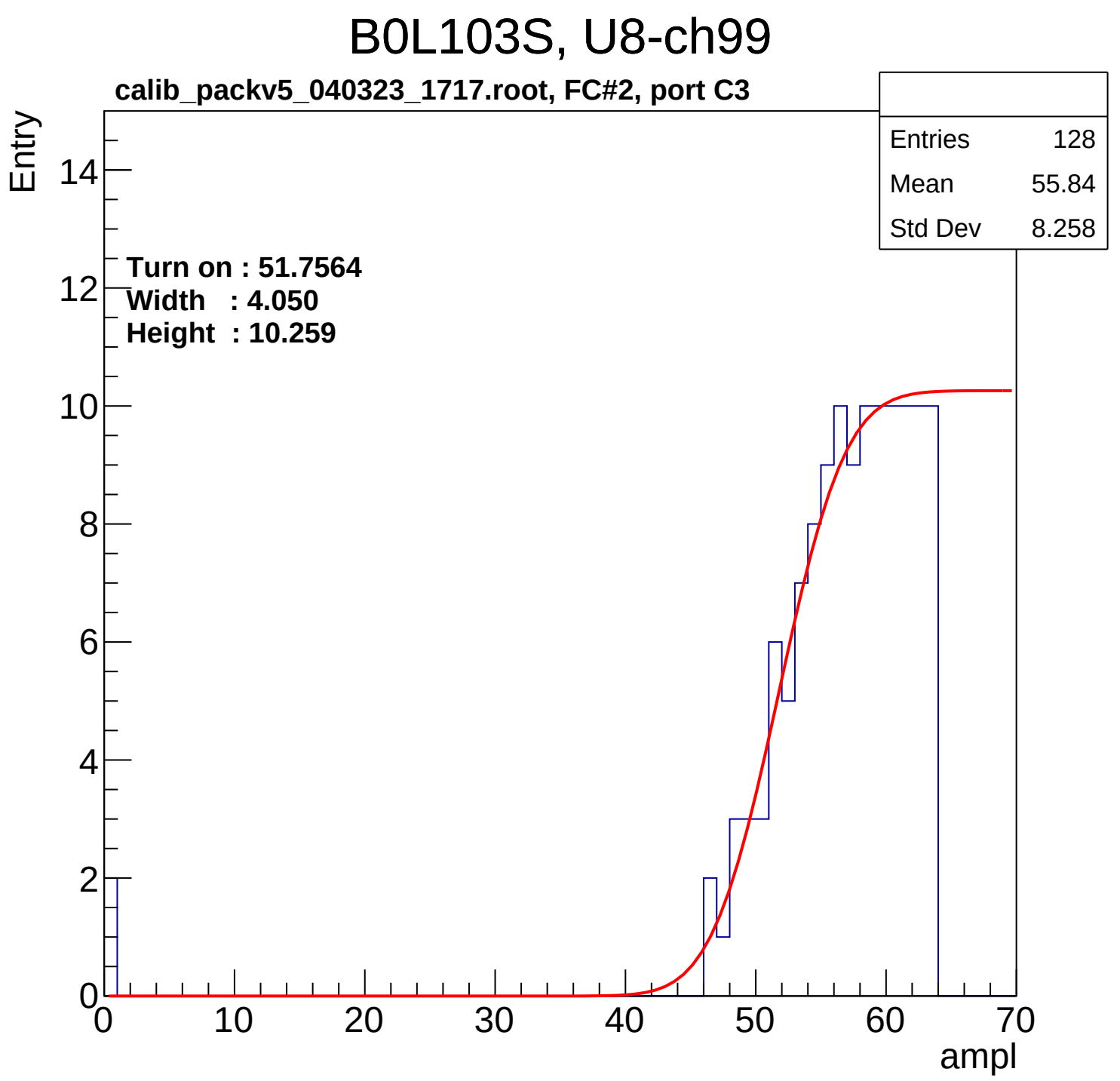
B0L103S, U8-ch99
calib_packv5_040323_1717.root, FC#2, port C3
Entries 128
Mean 55.84
Std Dev 8.258
Turn on : 51.7564
Width : 4.050
Height : 10.259
Entry
ampl
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8
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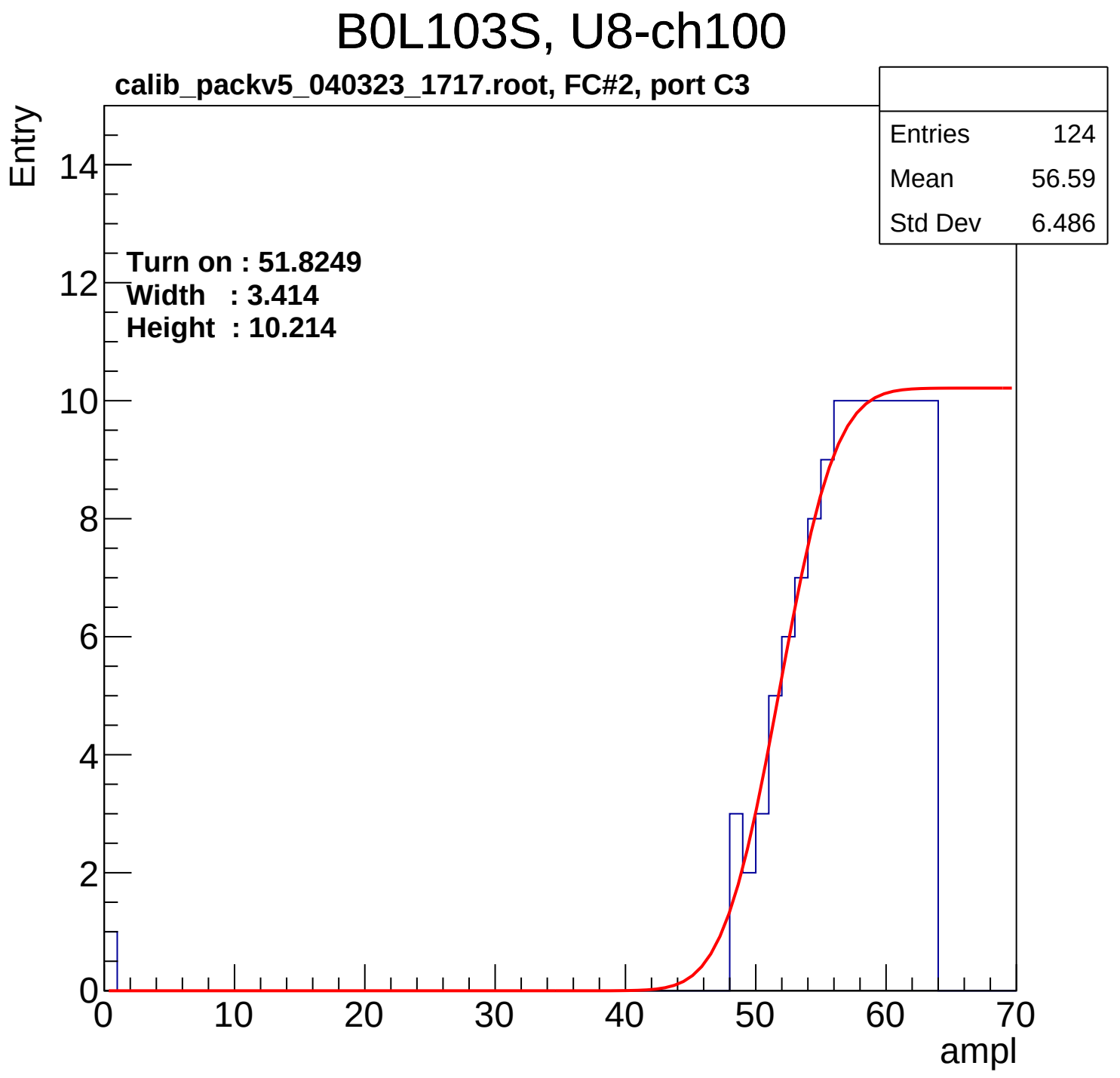
B0L103S, U8-ch100
calib_packv5_040323_1717.root, FC#2, port C3
Entries 124
Mean 56.59
Std Dev 6.486
Turn on : 51.8249
Width : 3.414
Height : 10.214
Entry
ampl
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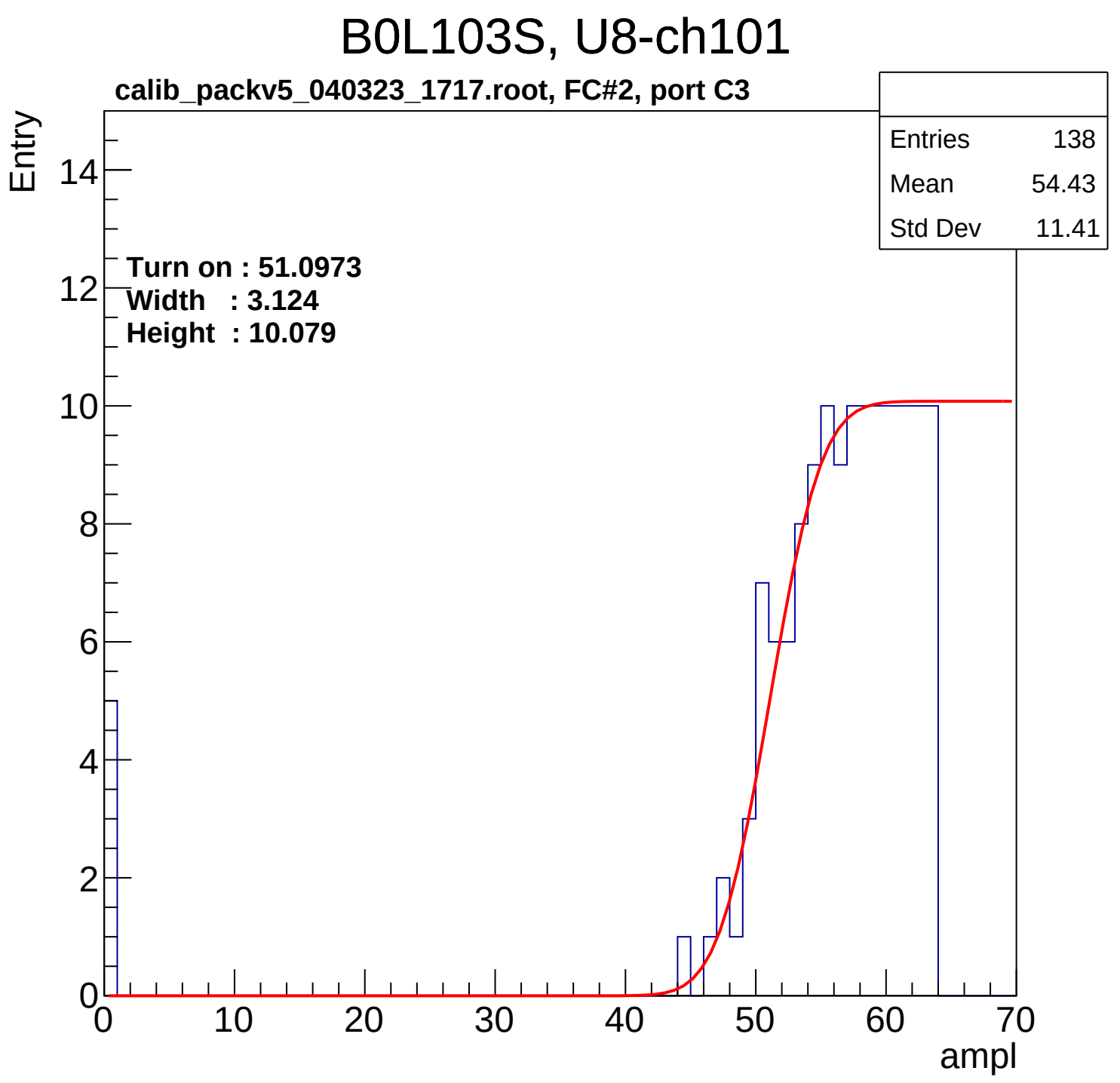
B0L103S, U8-ch101
calib_packv5_040323_1717.root, FC#2, port C3
Entries 138
Mean 54.43
Std Dev 11.41
Turn on : 51.0973
Width : 3.124
Height : 10.079
Entry
ampl
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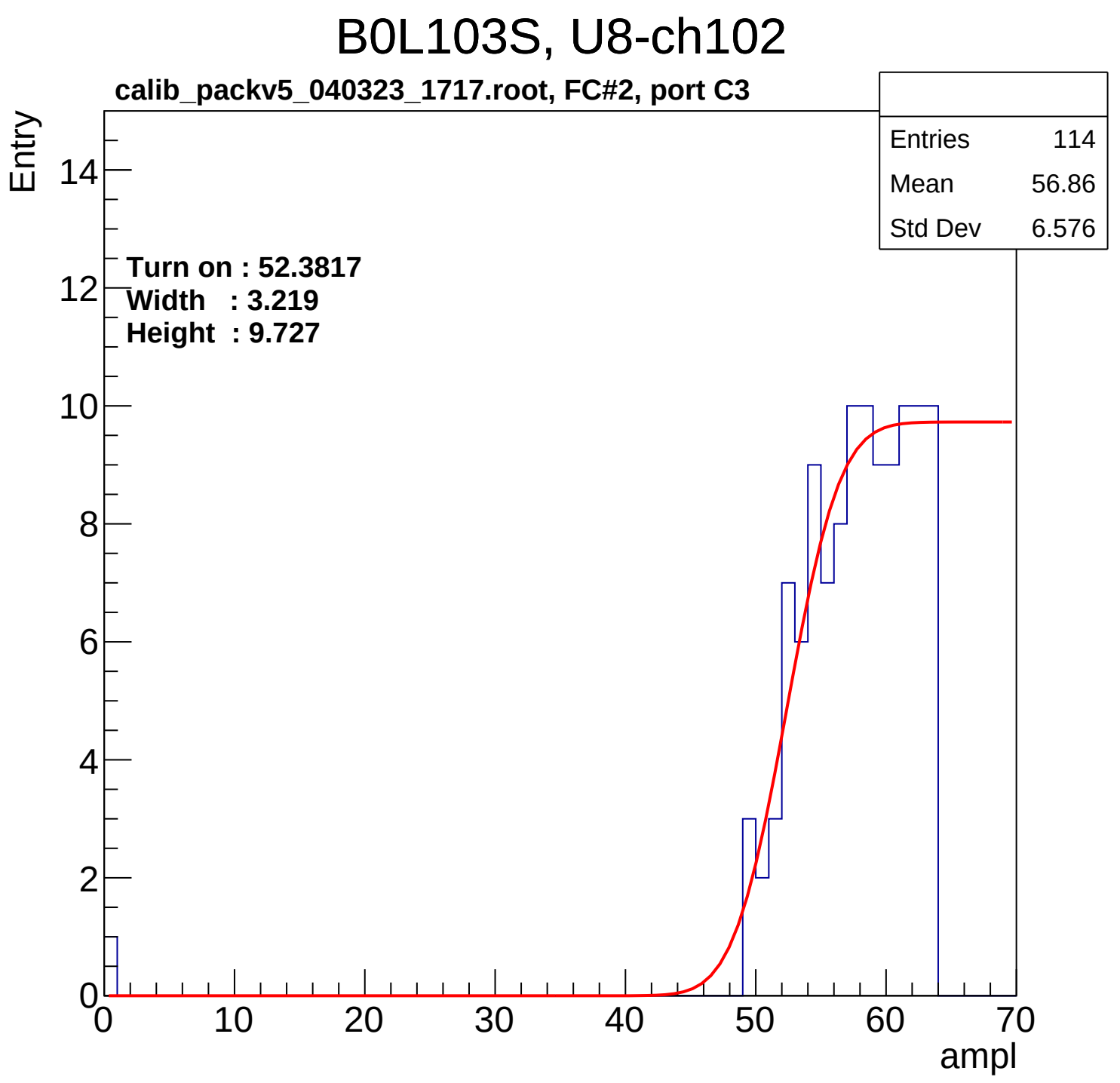
B0L103S, U8-ch102
calib_packv5_040323_1717.root, FC#2, port C3
Entries 114
Mean 56.86
Std Dev 6.576
Turn on : 52.3817
Width : 3.219
Height : 9.727
Entry
ampl
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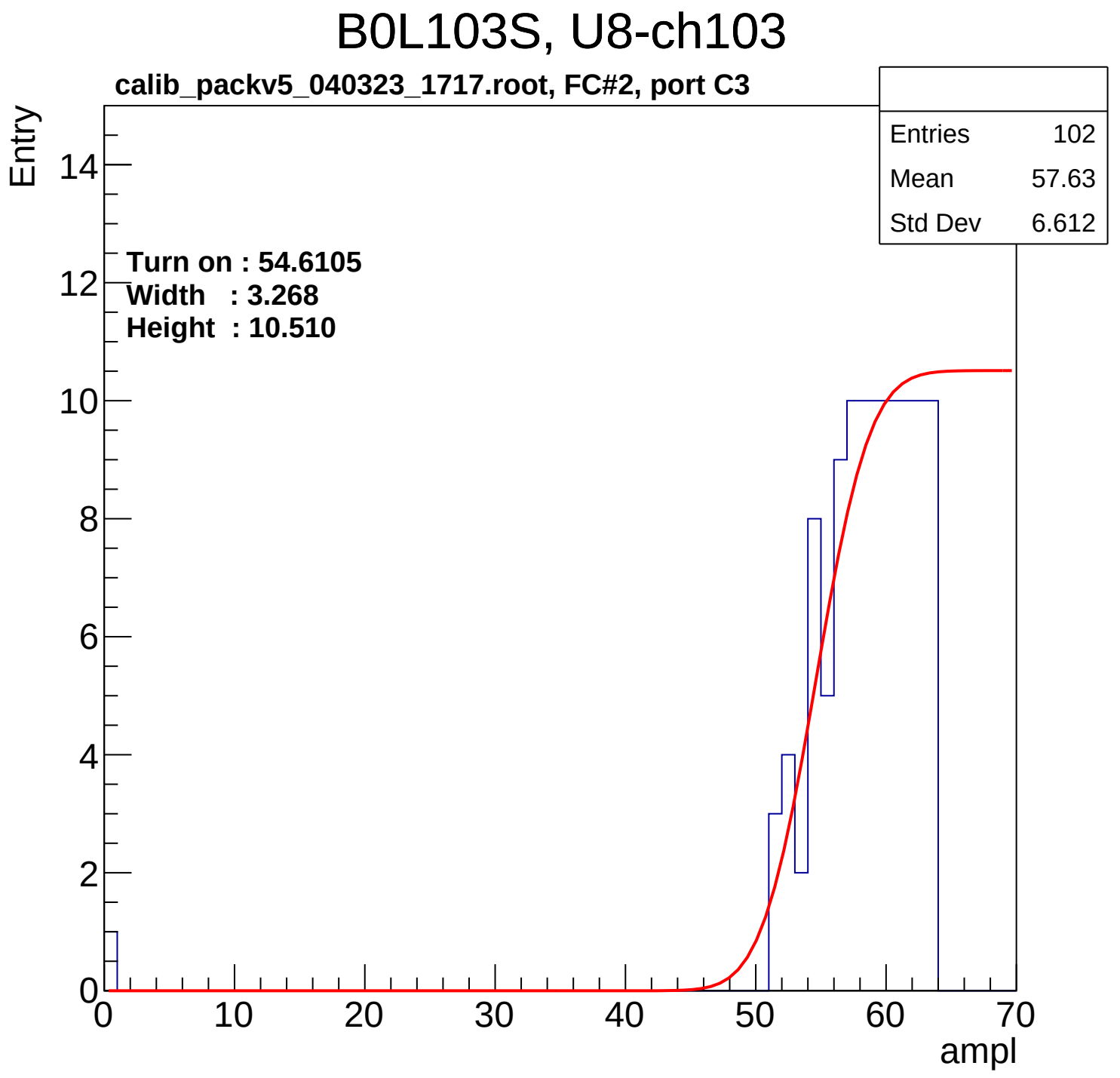
B0L103S, U8-ch103
calib_packv5_040323_1717.root, FC#2, port C3
Entries 102
Mean 57.63
Std Dev 6.612
Turn on : 54.6105
Width : 3.268
Height : 10.510
Entry
ampl
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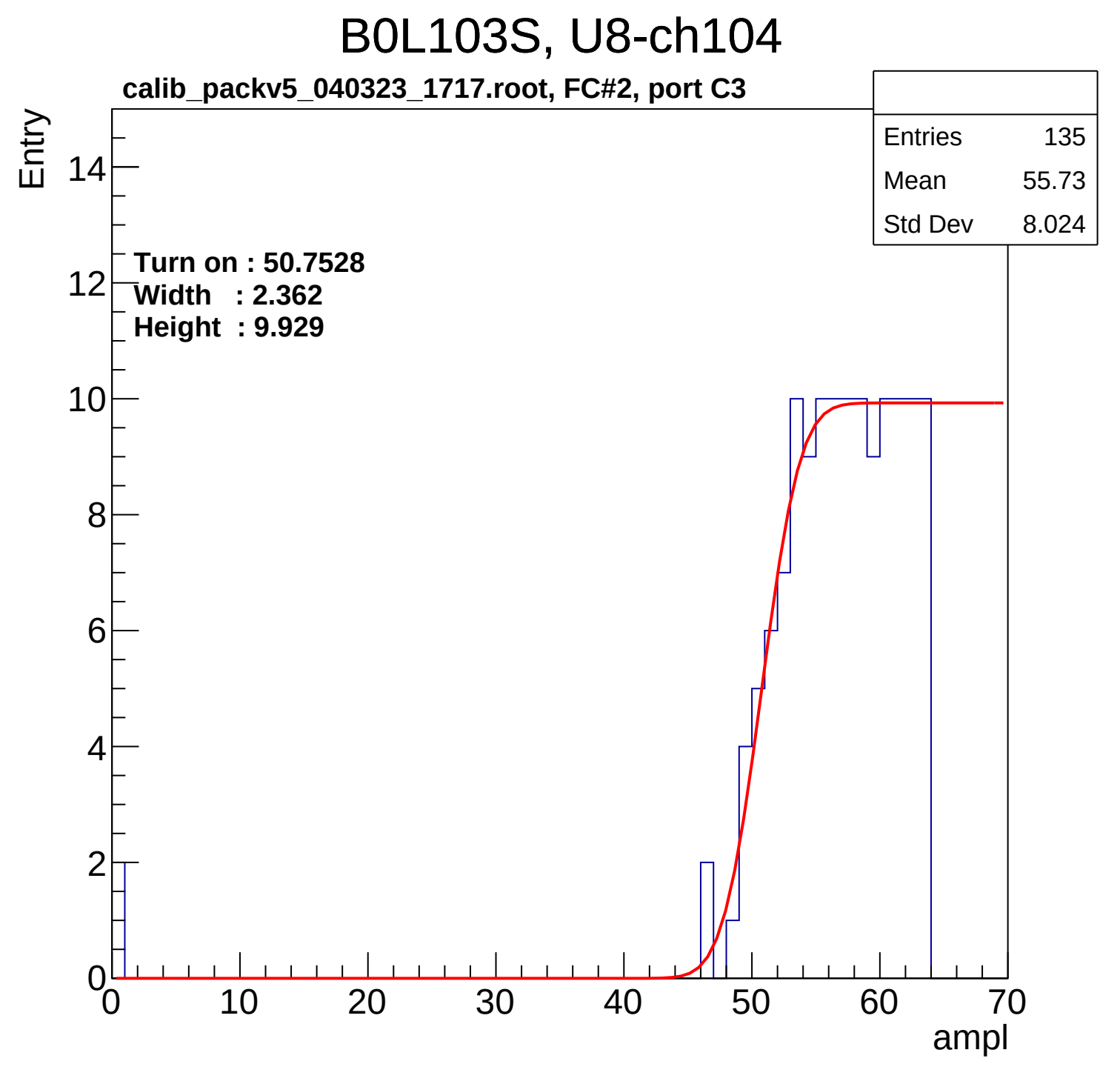
B0L103S, U8-ch104
calib_packv5_040323_1717.root, FC#2, port C3
Entries 135
Mean 55.73
Std Dev 8.024
Turn on : 50.7528
Width : 2.362
Height : 9.929
Entry
ampl
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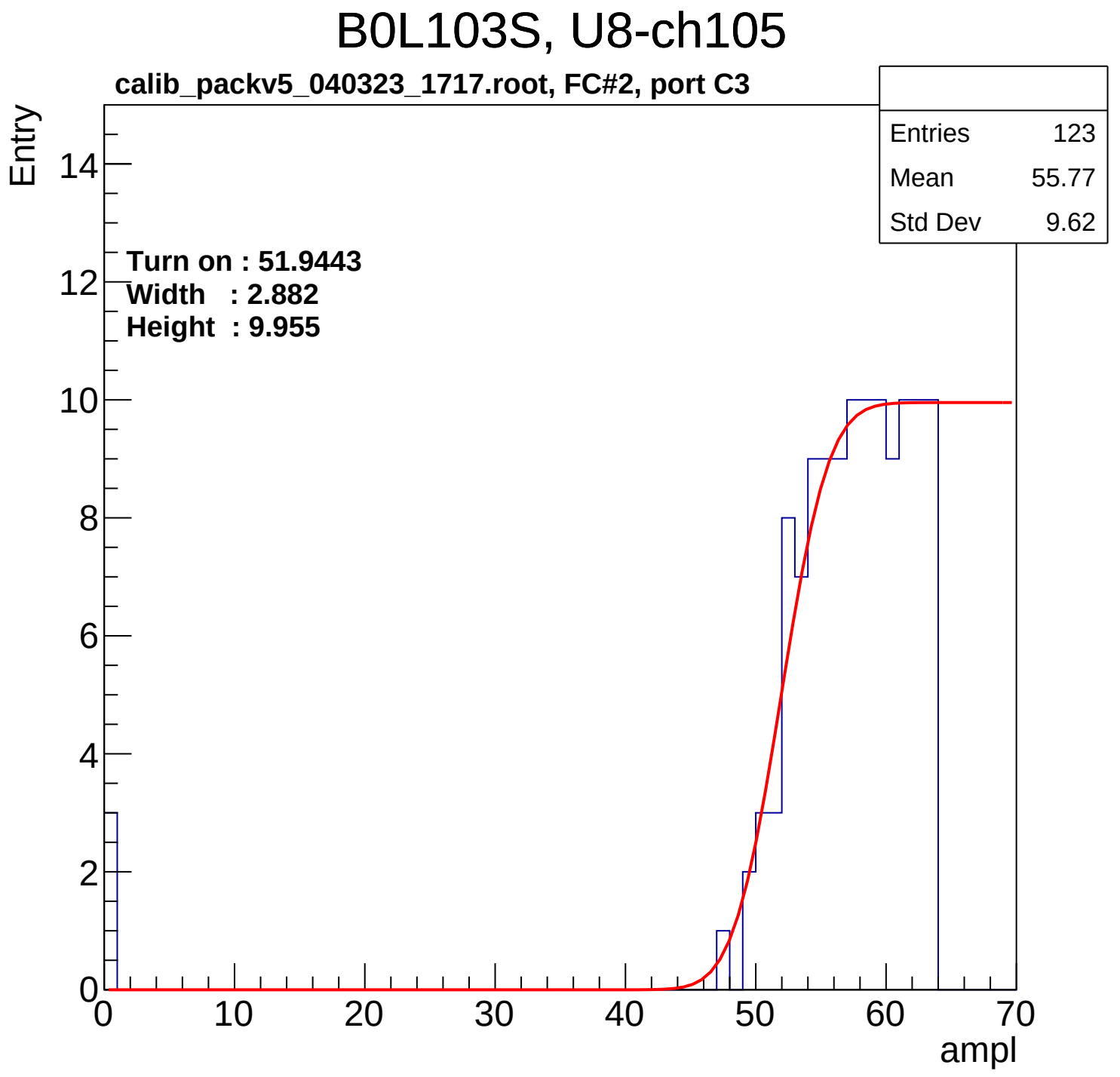
B0L103S, U8-ch105
calib_packv5_040323_1717.root, FC#2, port C3
Entries 123
Mean 55.77
Std Dev 9.62
Turn on : 51.9443
Width : 2.882
Height : 9.955
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ampl
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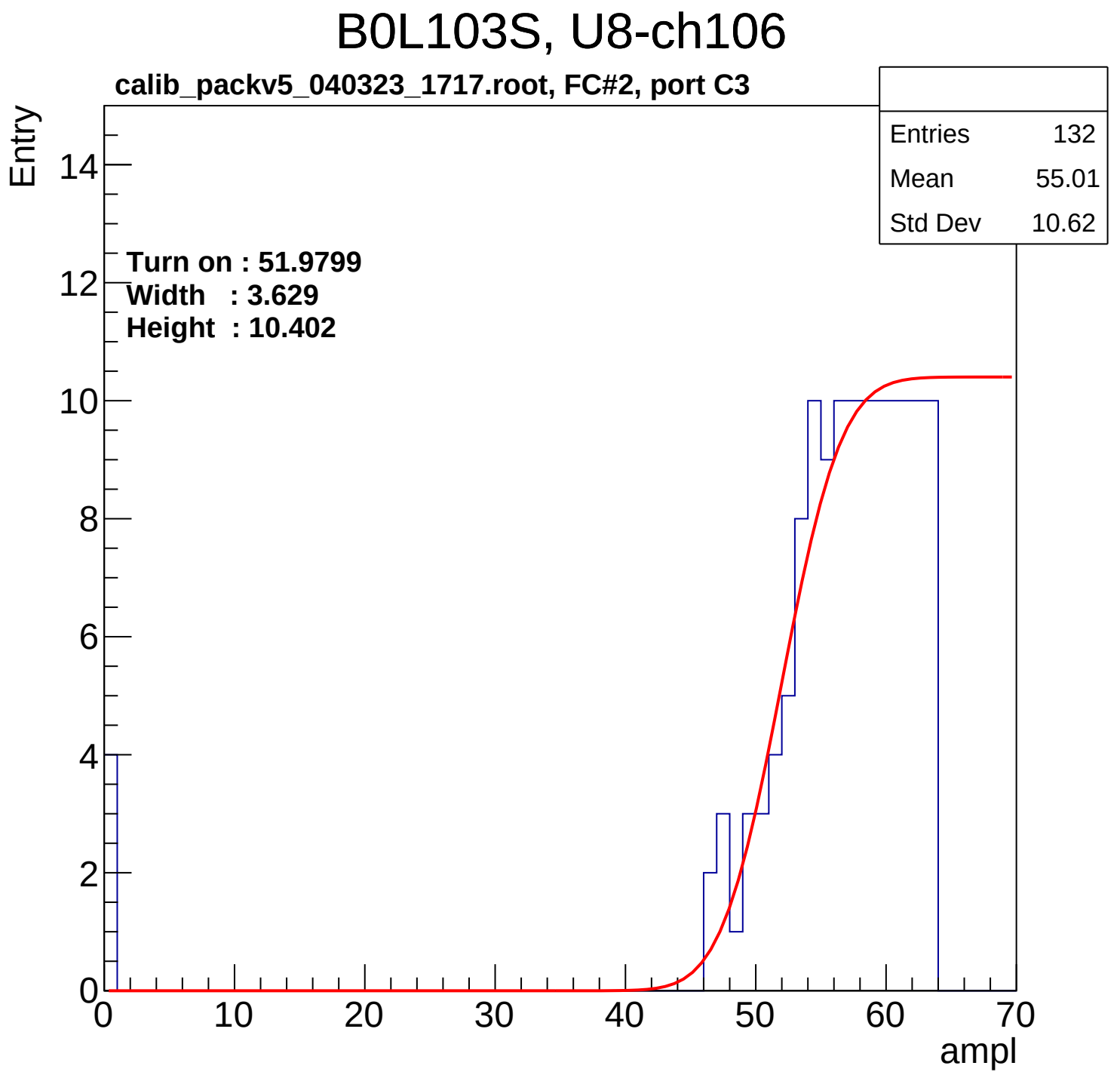
B0L103S, U8-ch106
calib_packv5_040323_1717.root, FC#2, port C3
Entries 132
Mean 55.01
Std Dev 10.62
Turn on : 51.9799
Width : 3.629
Height : 10.402
Entry
ampl
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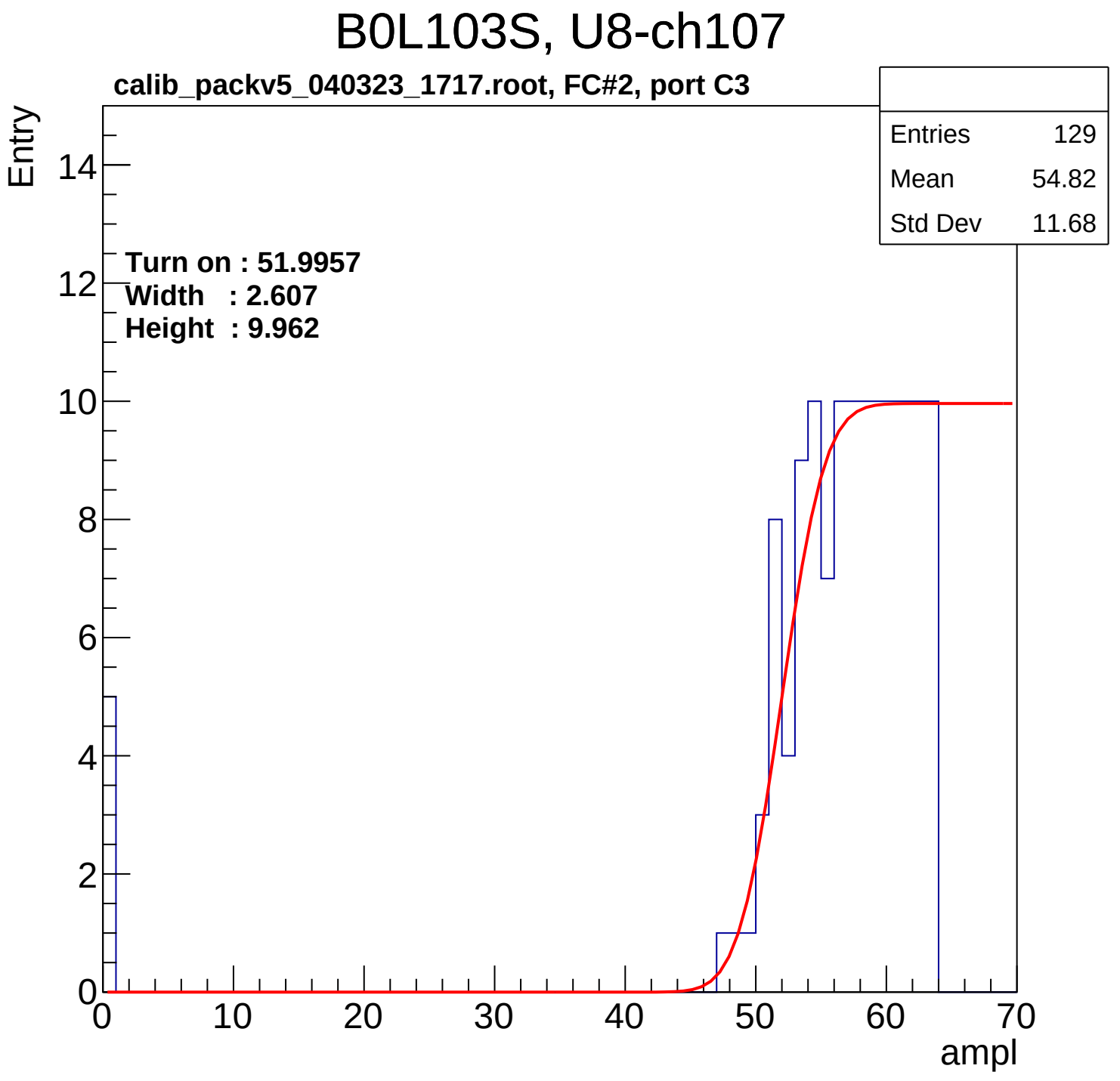
B0L103S, U8-ch107
calib_packv5_040323_1717.root, FC#2, port C3
Entries 129
Mean 54.82
Std Dev 11.68
Turn on : 51.9957
Width : 2.607
Height : 9.962
Entry
ampl
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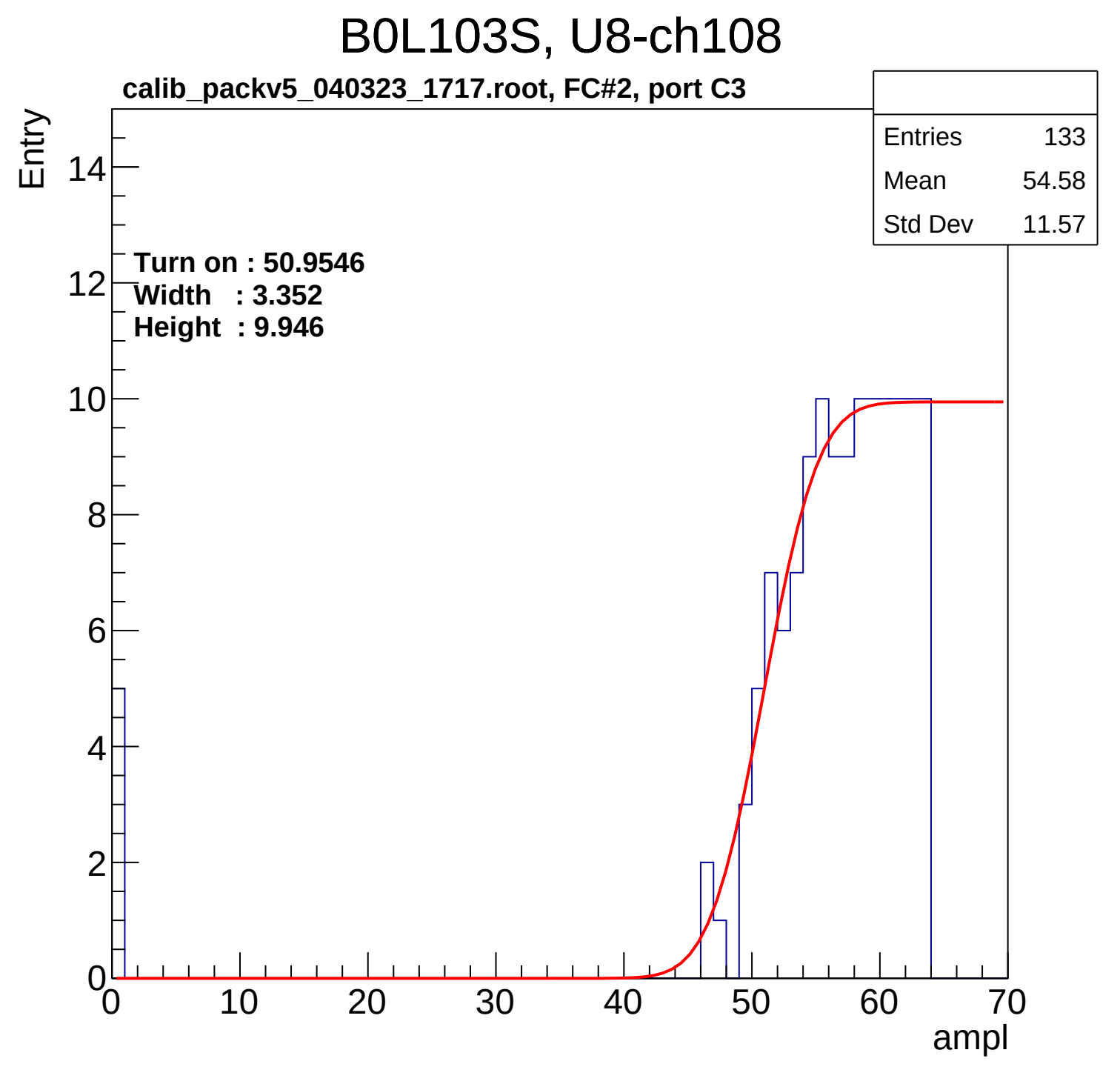
B0L103S, U8-ch108
calib_packv5_040323_1717.root, FC#2, port C3
Entries 133
Mean 54.58
Std Dev 11.57
Turn on : 50.9546
Width : 3.352
Height : 9.946
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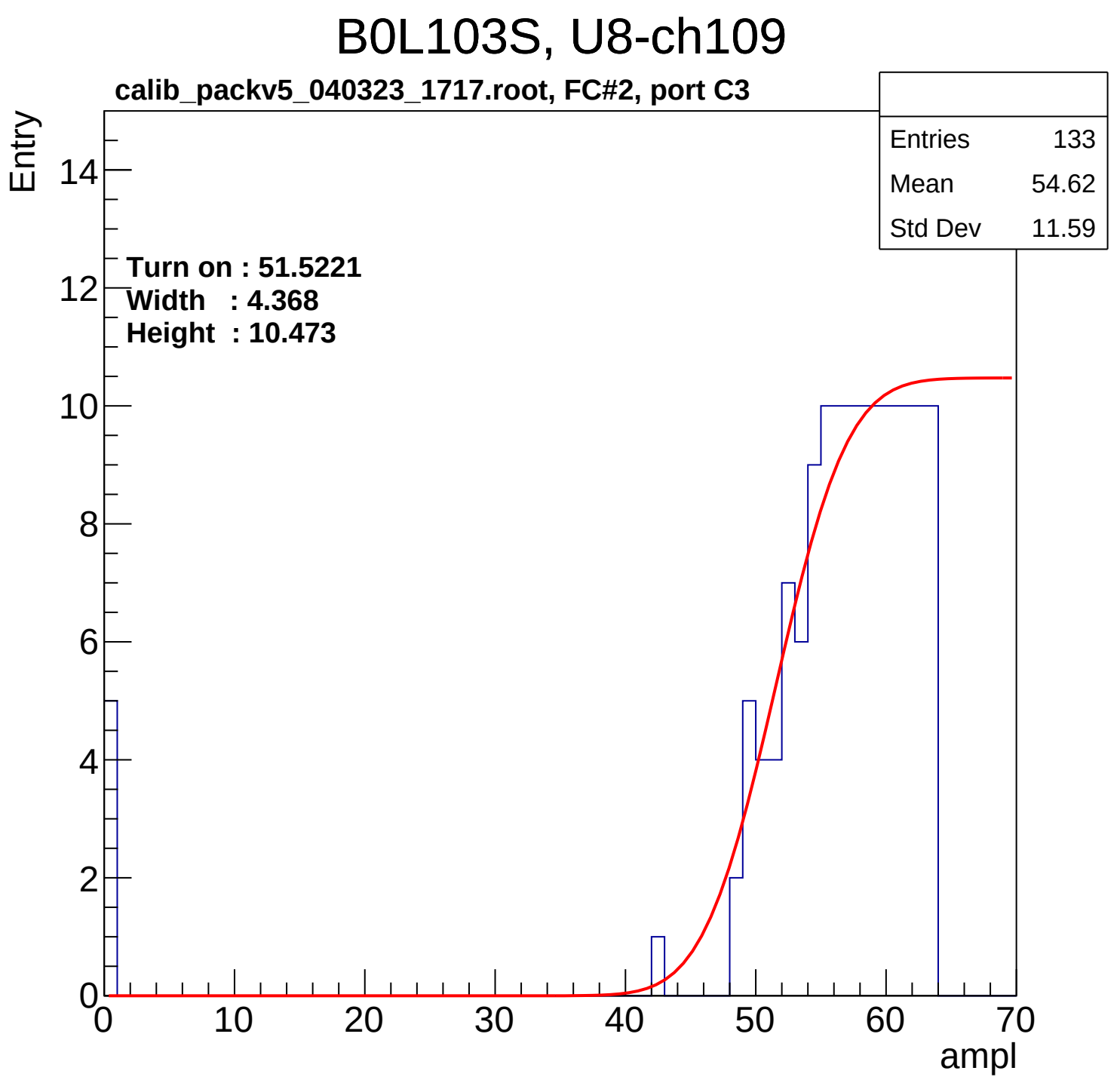
B0L103S, U8-ch109
calib_packv5_040323_1717.root, FC#2, port C3
Entries 133
Mean 54.62
Std Dev 11.59
Turn on : 51.5221
Width : 4.368
Height : 10.473
Entry
ampl
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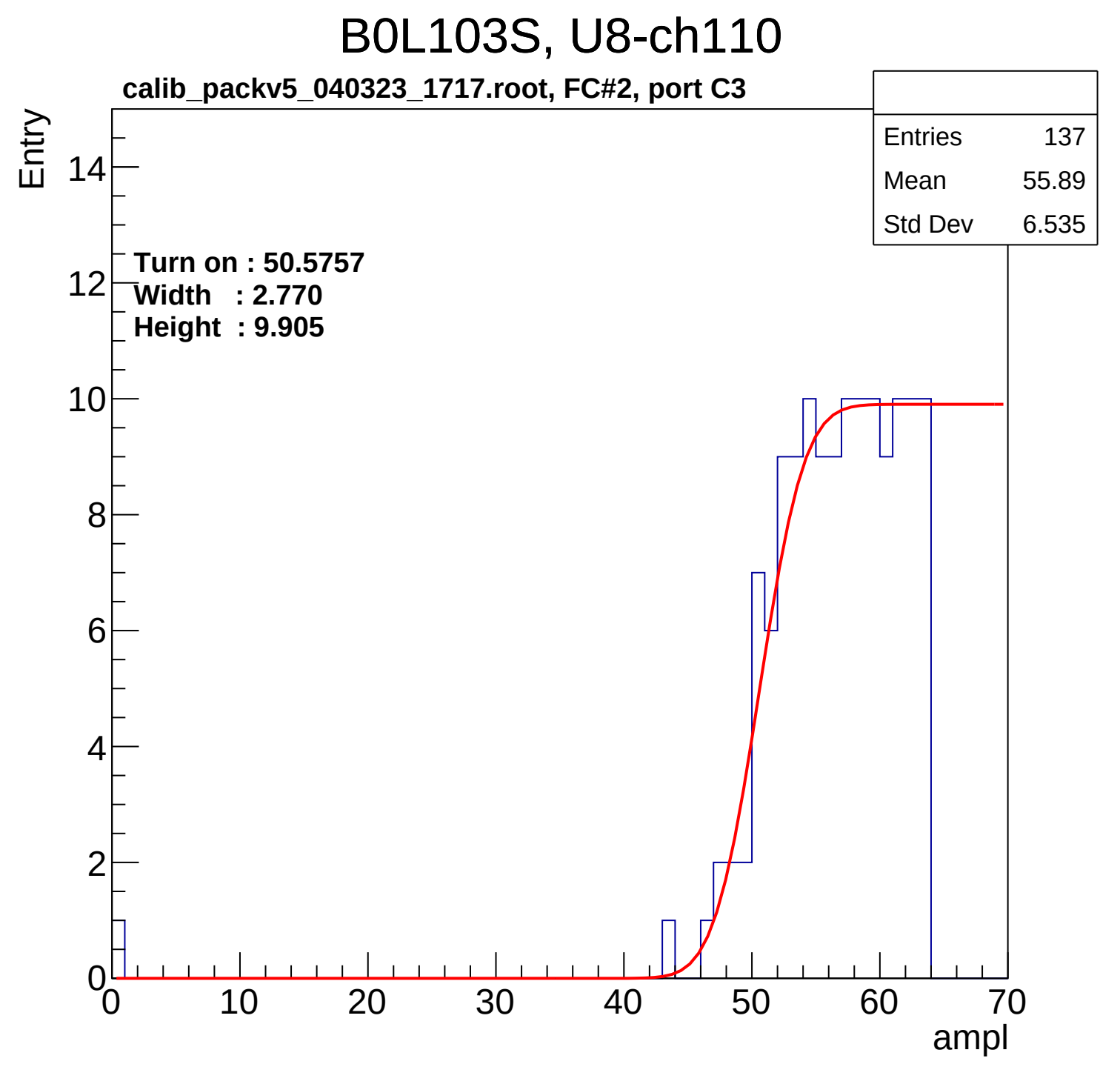
B0L103S, U8-ch110
calib_packv5_040323_1717.root, FC#2, port C3
Entries 137
Mean 55.89
Std Dev 6.535
Turn on : 50.5757
Width : 2.770
Height : 9.905
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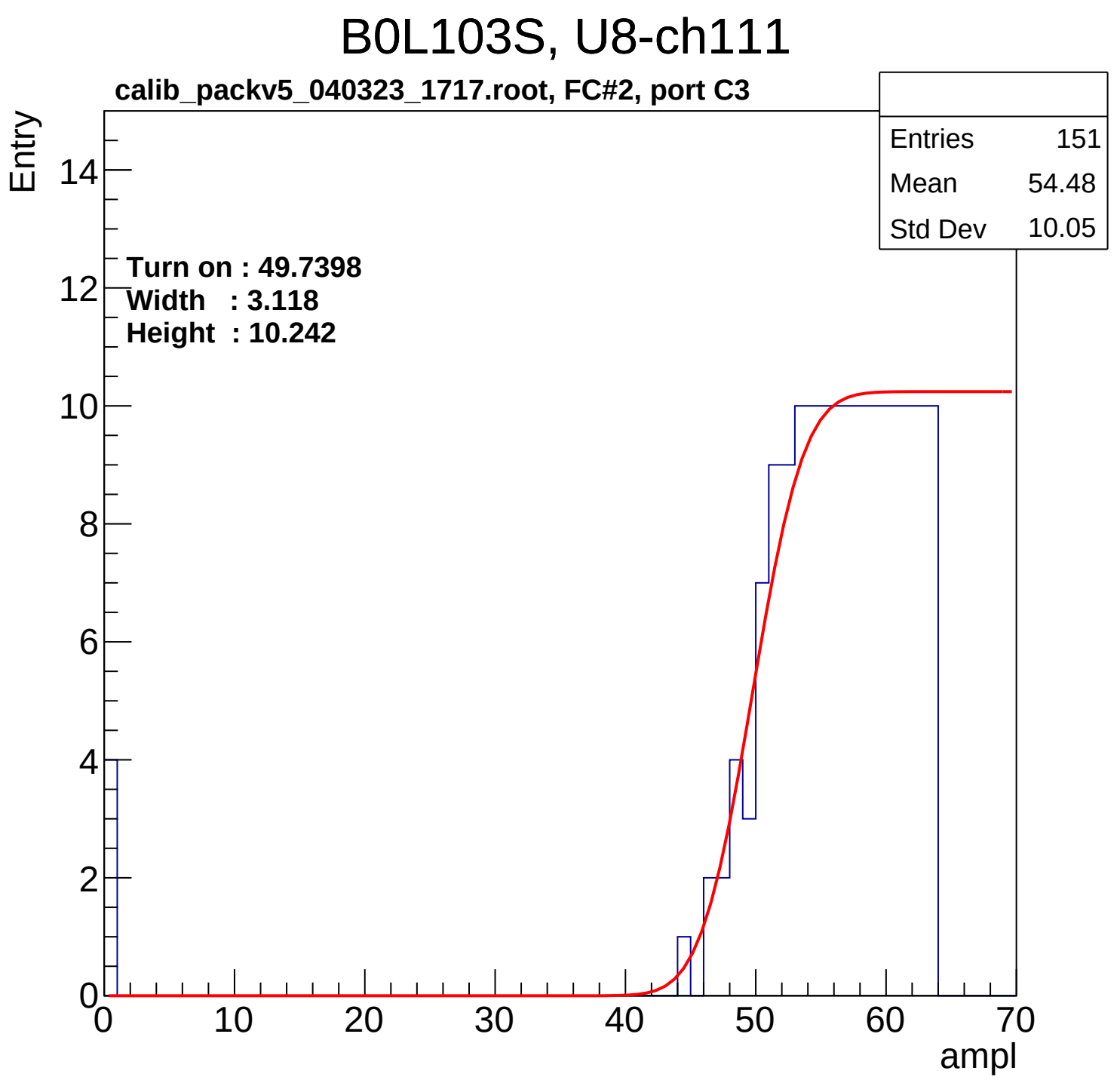
B0L103S, U8-ch111
calib_packv5_040323_1717.root, FC#2, port C3
Entries 151
Mean 54.48
Std Dev 10.05
Turn on : 49.7398
Width : 3.118
Height : 10.242
Entry
ampl
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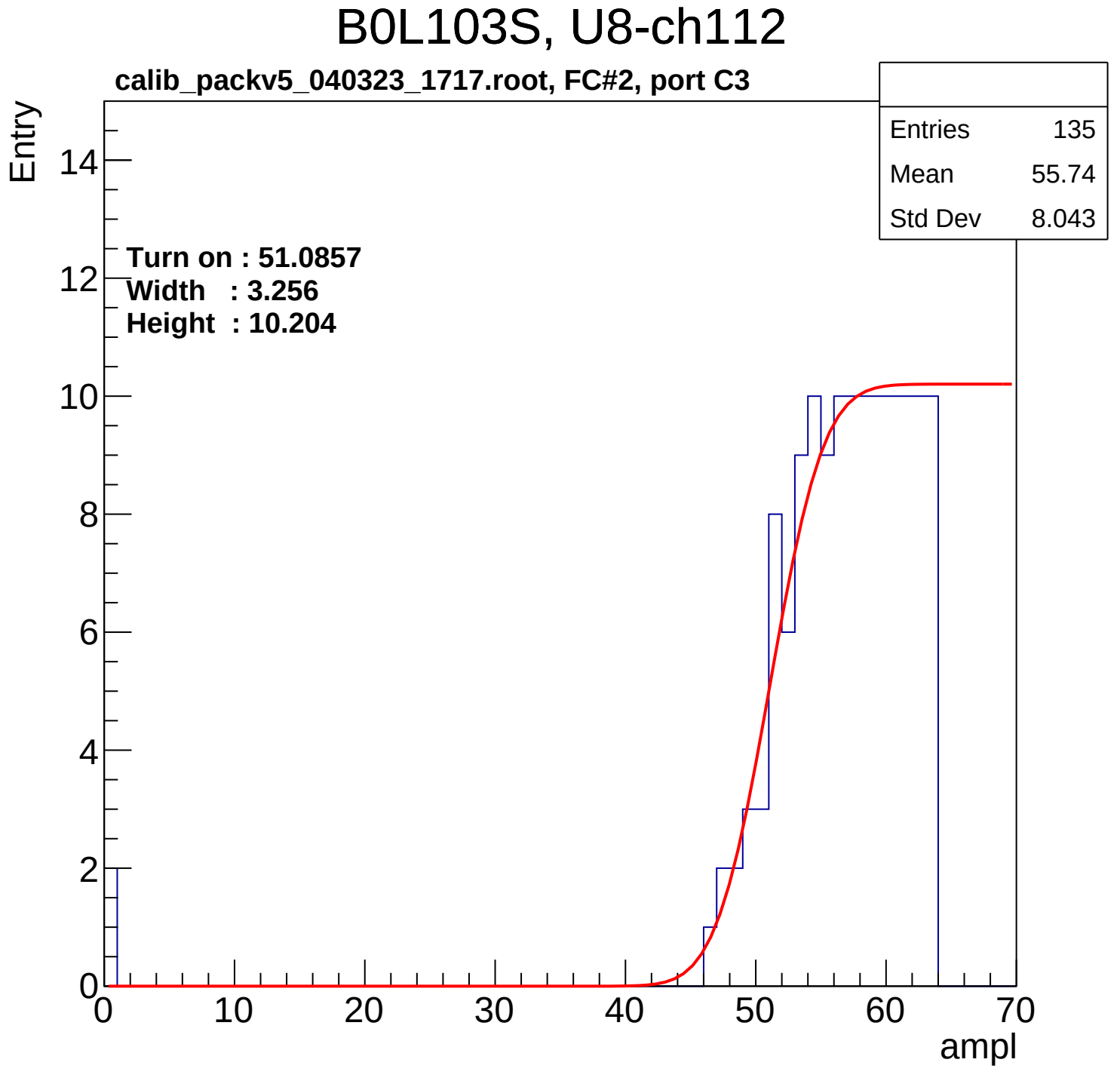
B0L103S, U8-ch112
calib_packv5_040323_1717.root, FC#2, port C3
Entries 135
Mean 55.74
Std Dev 8.043
Turn on : 51.0857
Width : 3.256
Height : 10.204
Entry
ampl
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6
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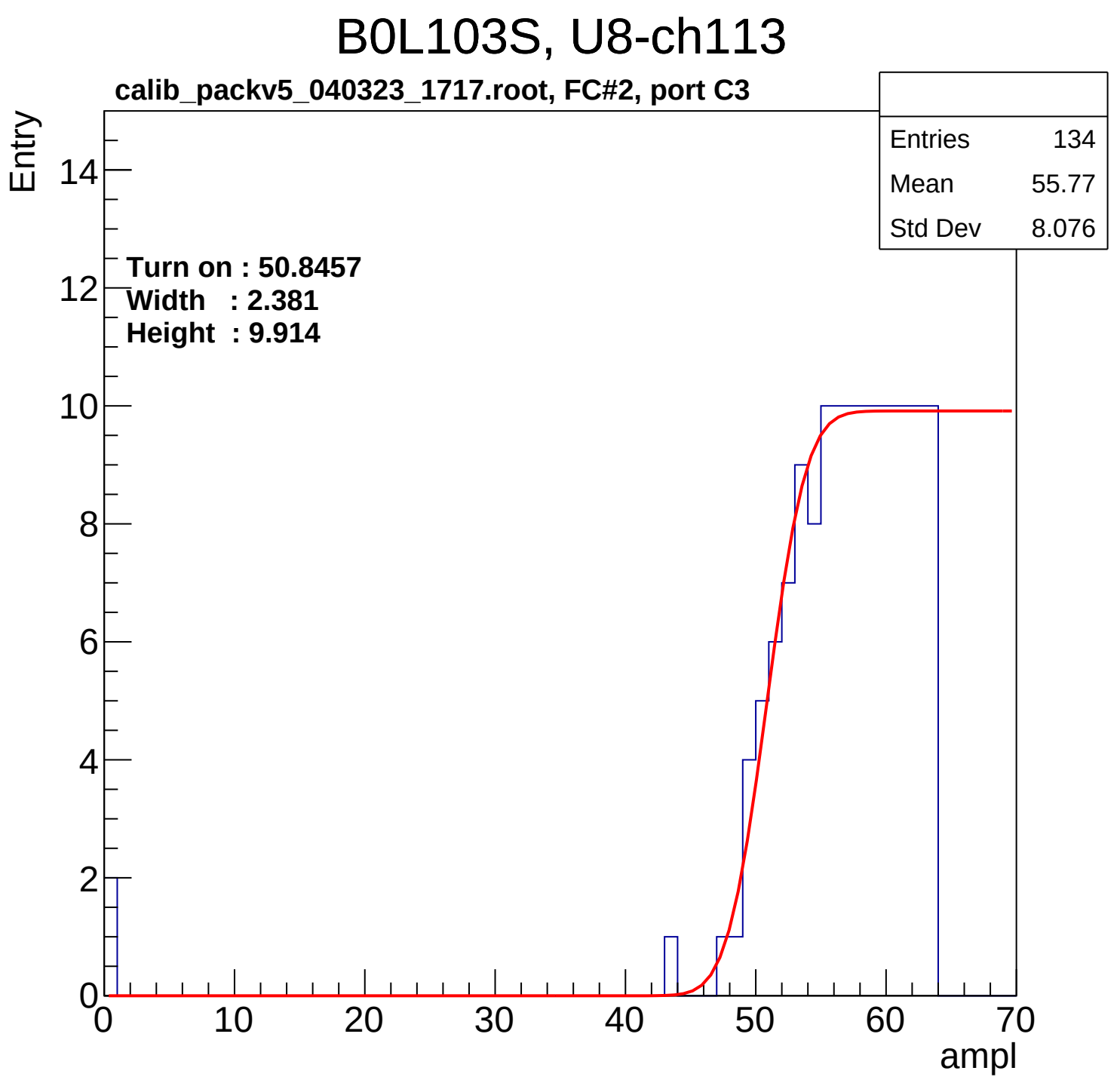
B0L103S, U8-ch113
calib_packv5_040323_1717.root, FC#2, port C3
Entries 134
Mean 55.77
Std Dev 8.076
Turn on : 50.8457
Width : 2.381
Height : 9.914
Entry
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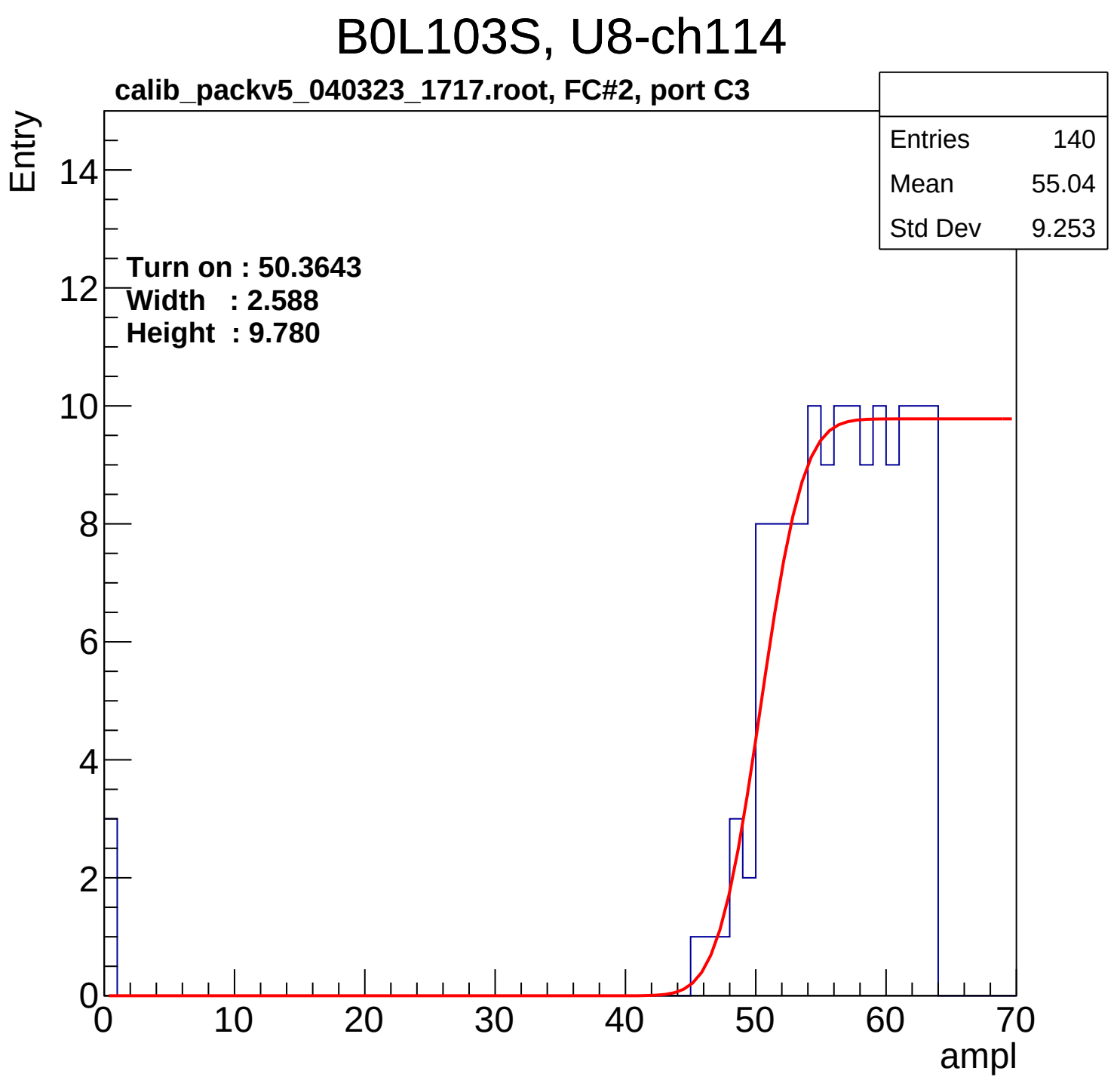
B0L103S, U8-ch114
calib_packv5_040323_1717.root, FC#2, port C3
Entries 140
Mean 55.04
Std Dev 9.253
Turn on : 50.3643
Width : 2.588
Height : 9.780
Entry
ampl
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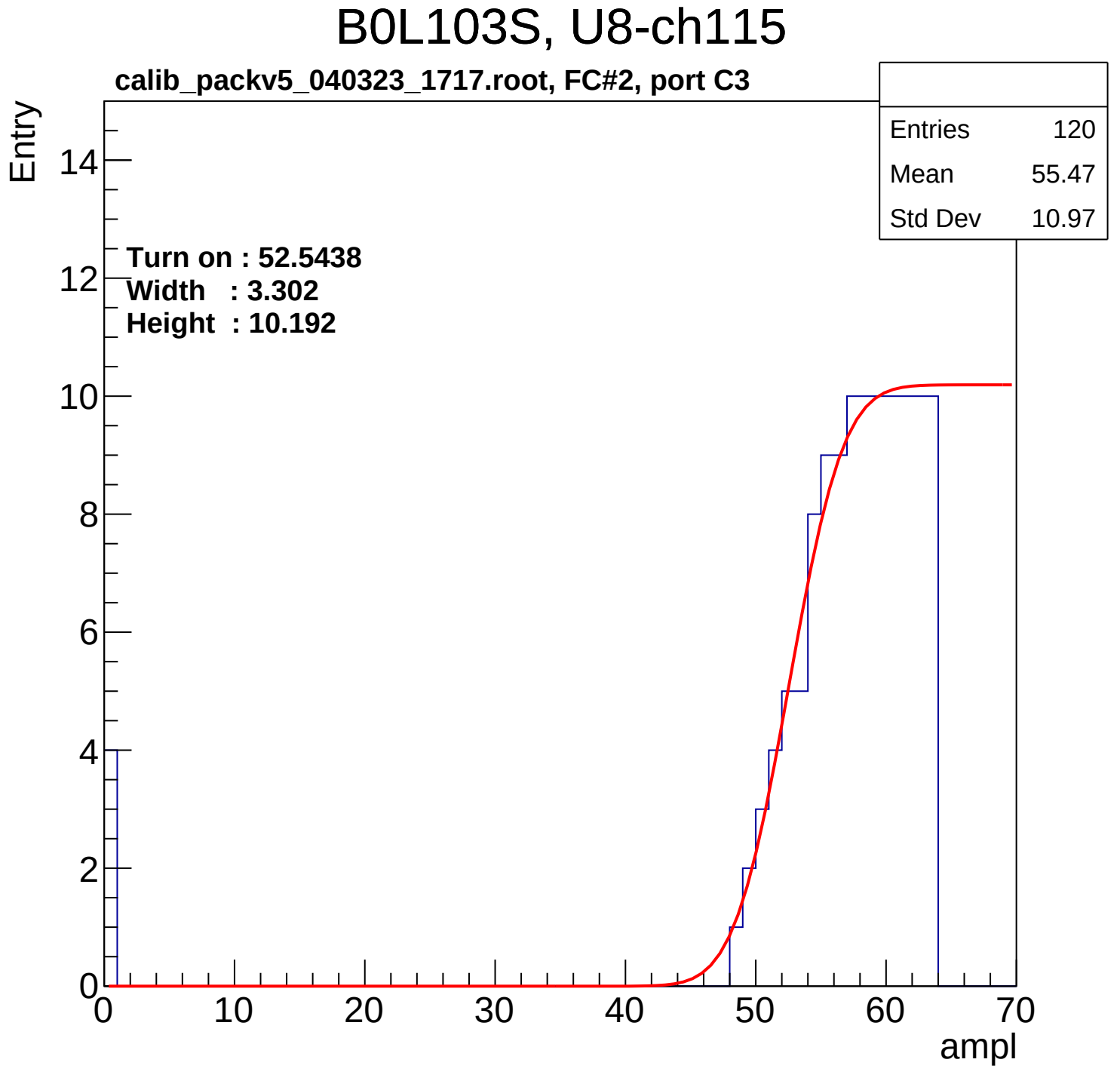
B0L103S, U8-ch115
calib_packv5_040323_1717.root, FC#2, port C3
Entries 120
Mean 55.47
Std Dev 10.97
Turn on : 52.5438
Width : 3.302
Height : 10.192
Entry
ampl
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2
4
6
8
10
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14
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10
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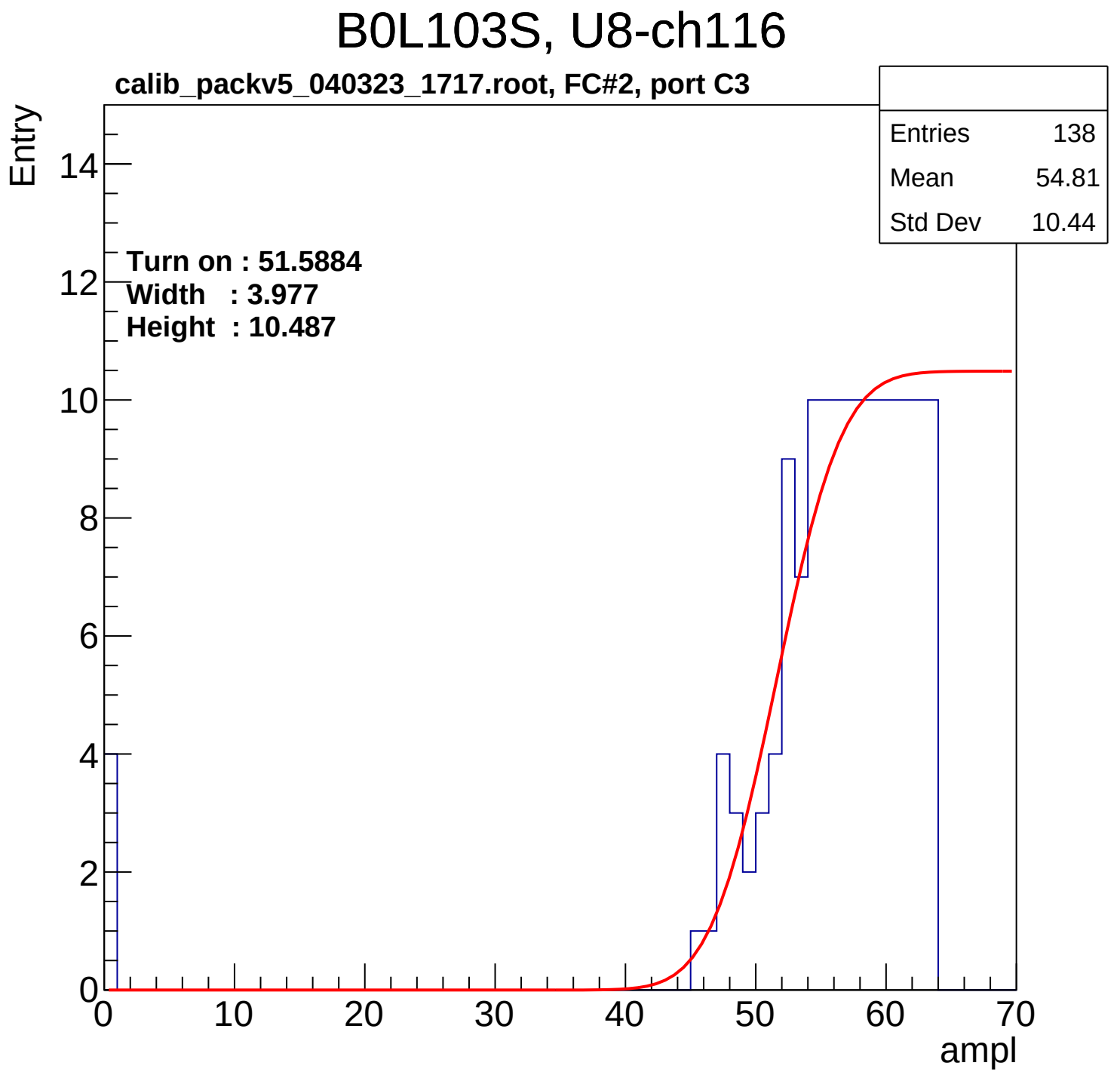
B0L103S, U8-ch116
calib_packv5_040323_1717.root, FC#2, port C3
Entries 138
Mean 54.81
Std Dev 10.44
Turn on : 51.5884
Width : 3.977
Height : 10.487
Entry
ampl
0
2
4
6
8
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12
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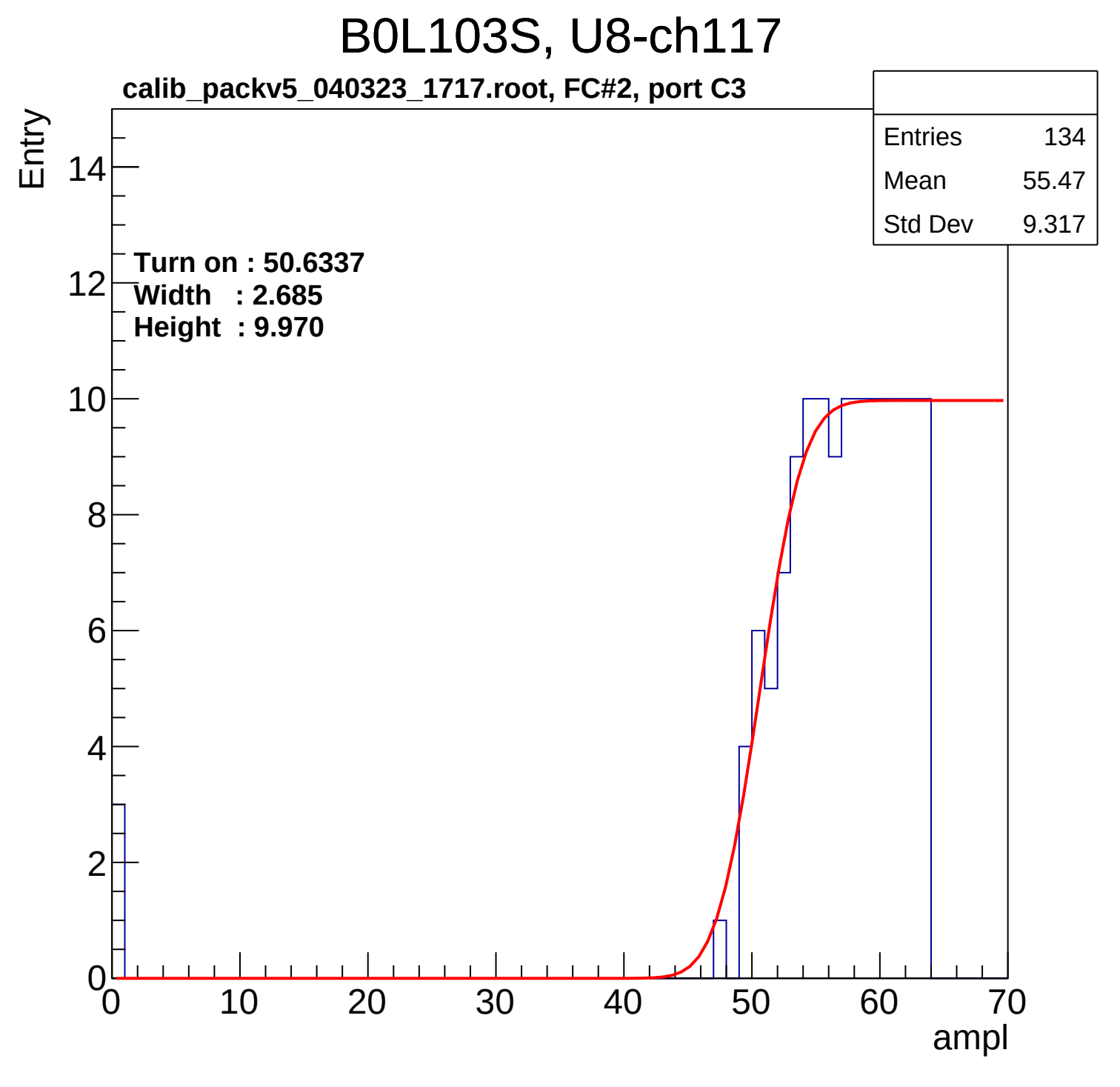
B0L103S, U8-ch117
calib_packv5_040323_1717.root, FC#2, port C3
Entries 134
Mean 55.47
Std Dev 9.317
Turn on : 50.6337
Width : 2.685
Height : 9.970
Entry
ampl
0
2
4
6
8
10
12
14
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10
20
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40
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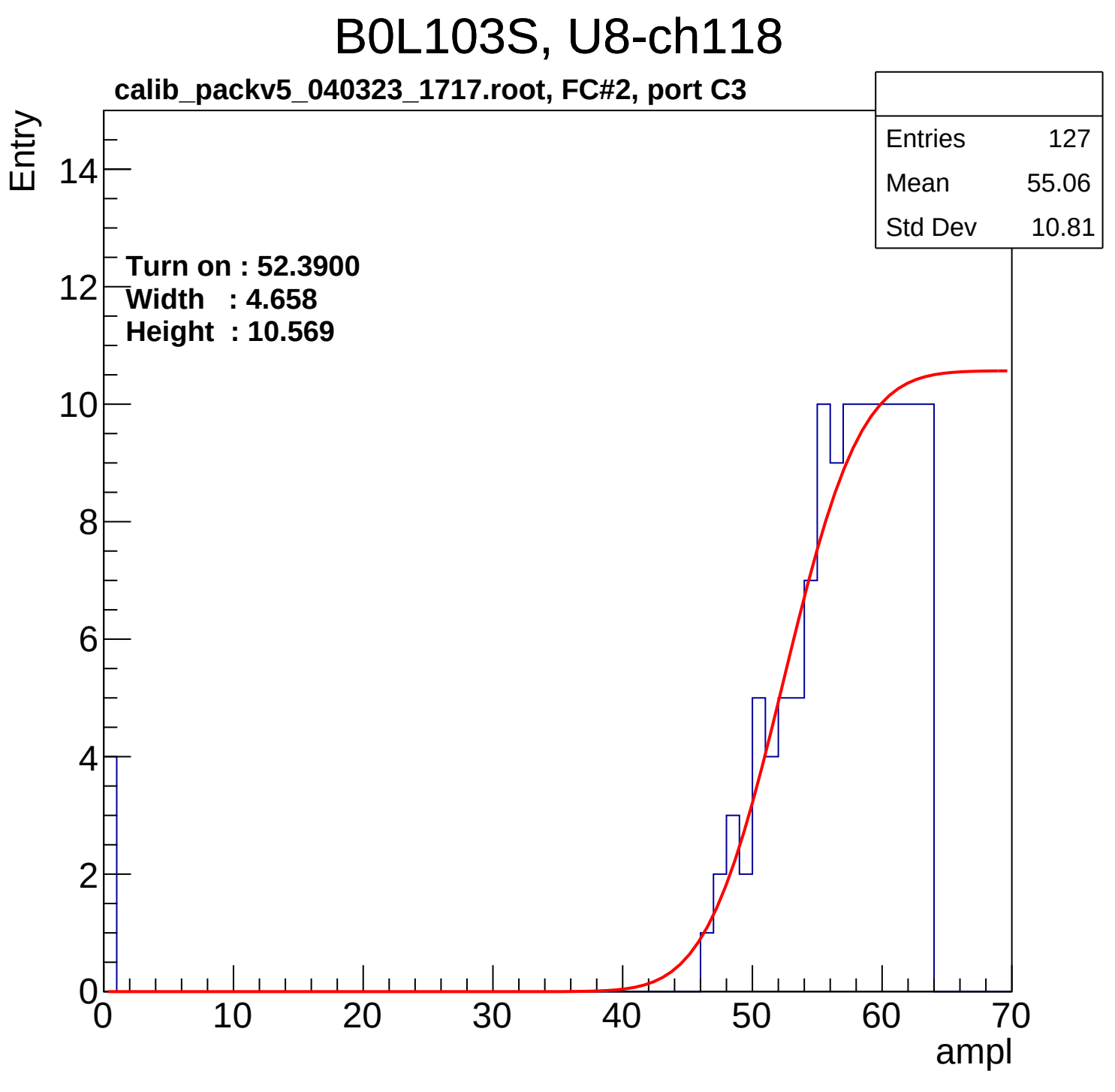
B0L103S, U8-ch118
calib_packv5_040323_1717.root, FC#2, port C3
Entries 127
Mean 55.06
Std Dev 10.81
Turn on : 52.3900
Width : 4.658
Height : 10.569
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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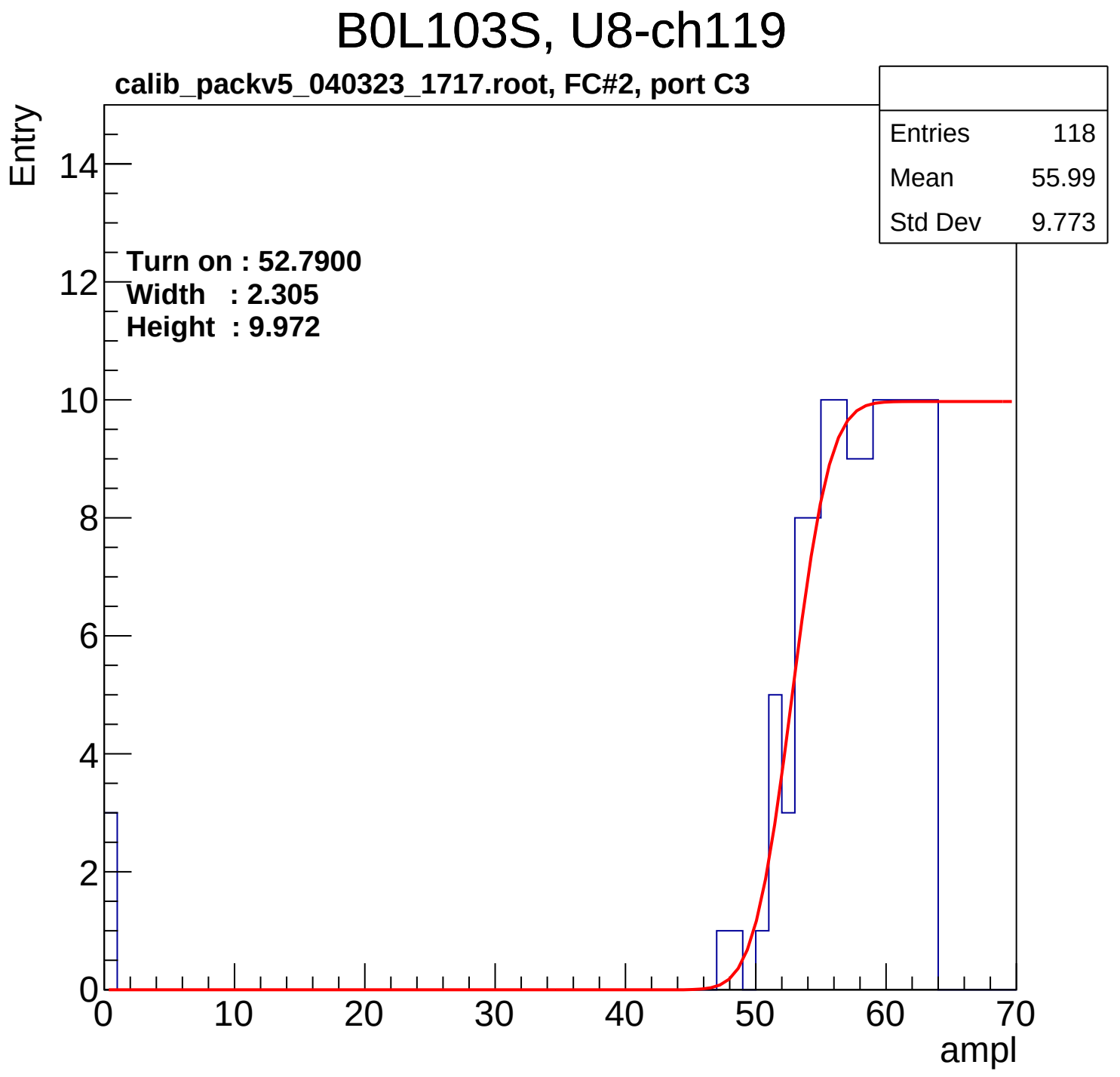
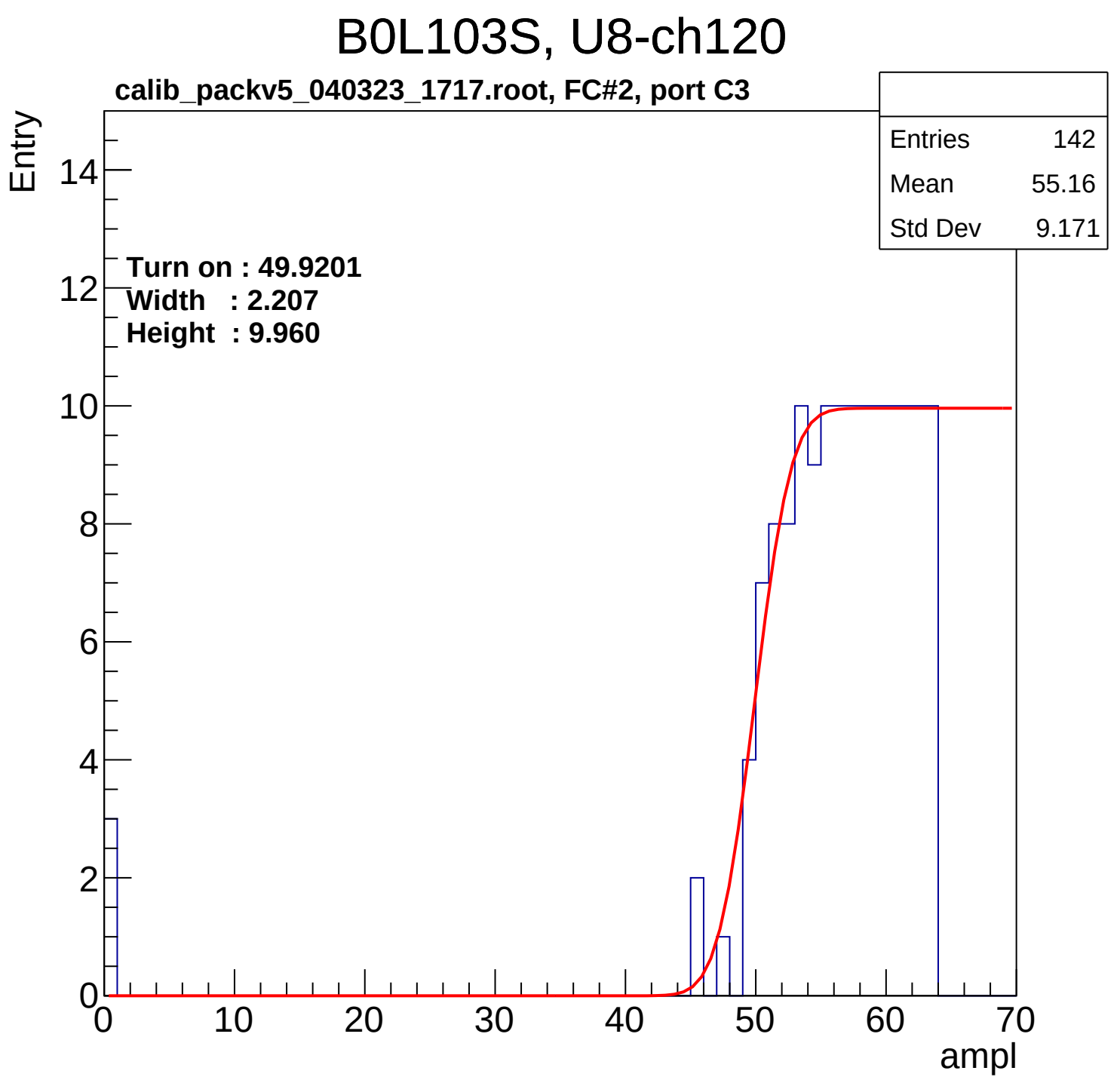

B0L103S, U8-ch119
calib_packv5_040323_1717.root, FC#2, port C3
Entries 118
Mean 55.99
Std Dev 9.773
Turn on : 52.7900
Width : 2.305
Height : 9.972
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L103S, U8-ch120
calib_packv5_040323_1717.root, FC#2, port C3
Entries 142
Mean 55.16
Std Dev 9.171
Turn on : 49.9201
Width : 2.207
Height : 9.960
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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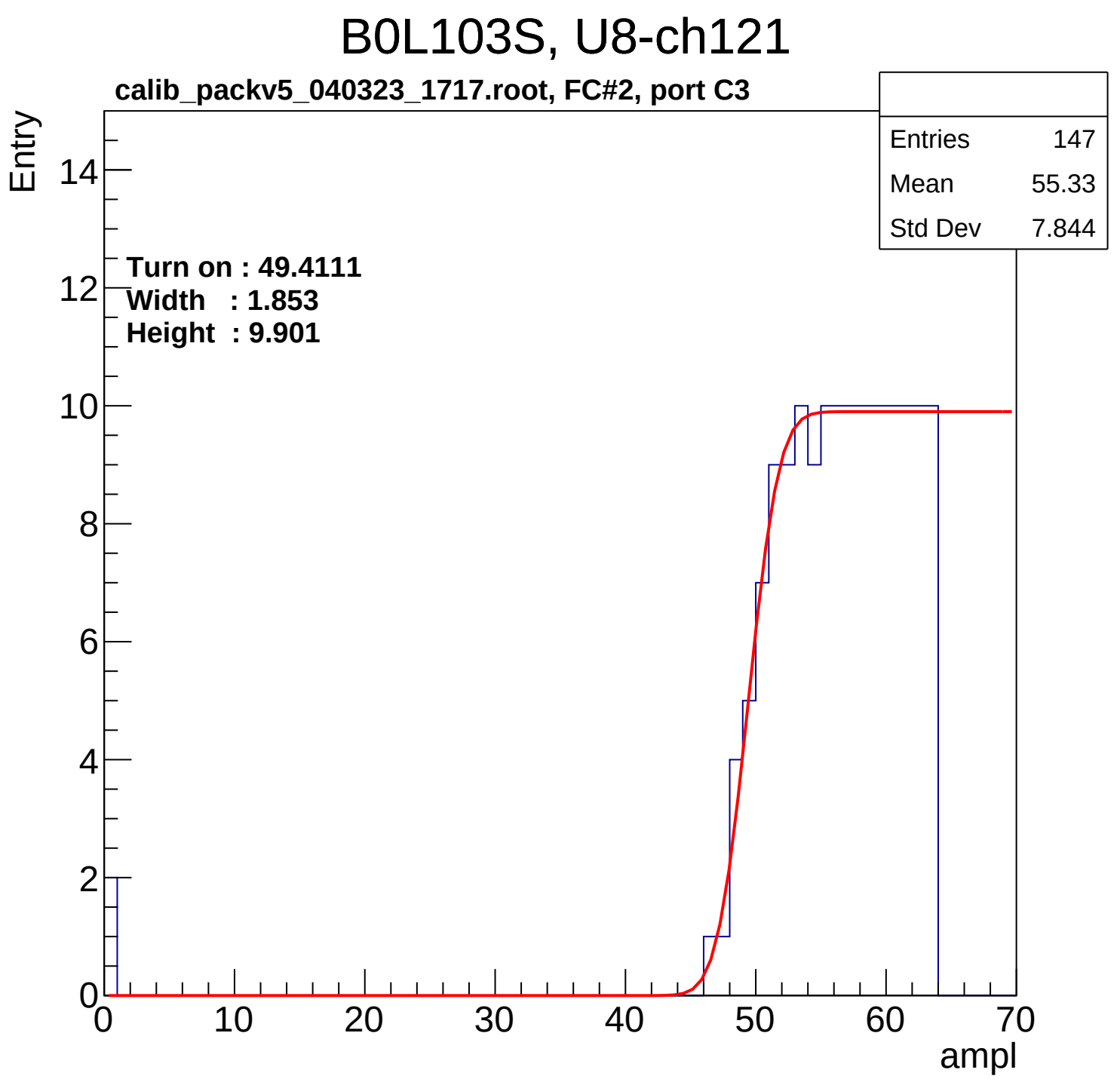
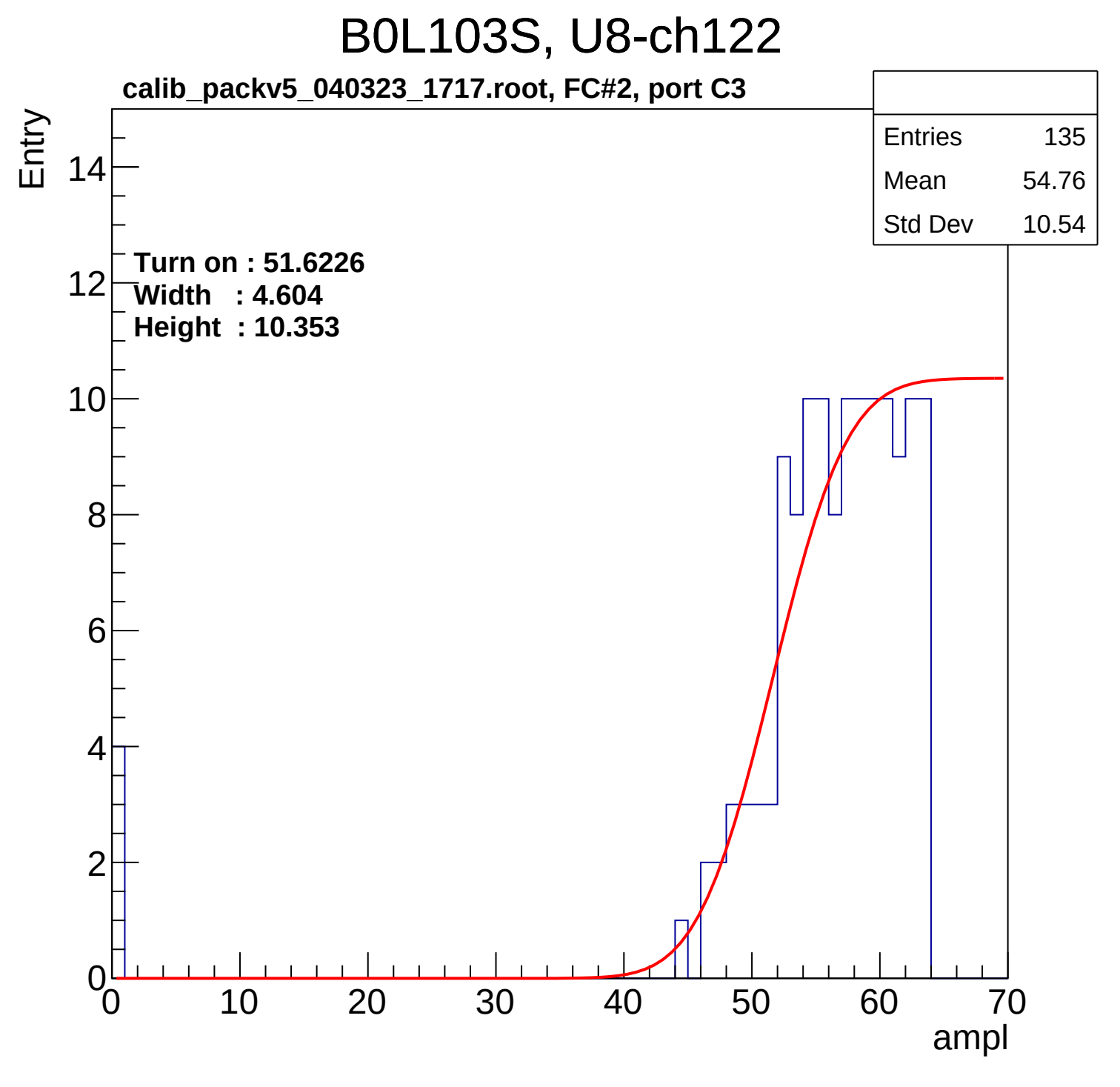

B0L103S, U8-ch121
calib_packv5_040323_1717.root, FC#2, port C3
Entries 147
Mean 55.33
Std Dev 7.844
Turn on : 49.4111
Width : 1.853
Height : 9.901
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L103S, U8-ch122
calib_packv5_040323_1717.root, FC#2, port C3
Entries 135
Mean 54.76
Std Dev 10.54
Turn on : 51.6226
Width : 4.604
Height : 10.353
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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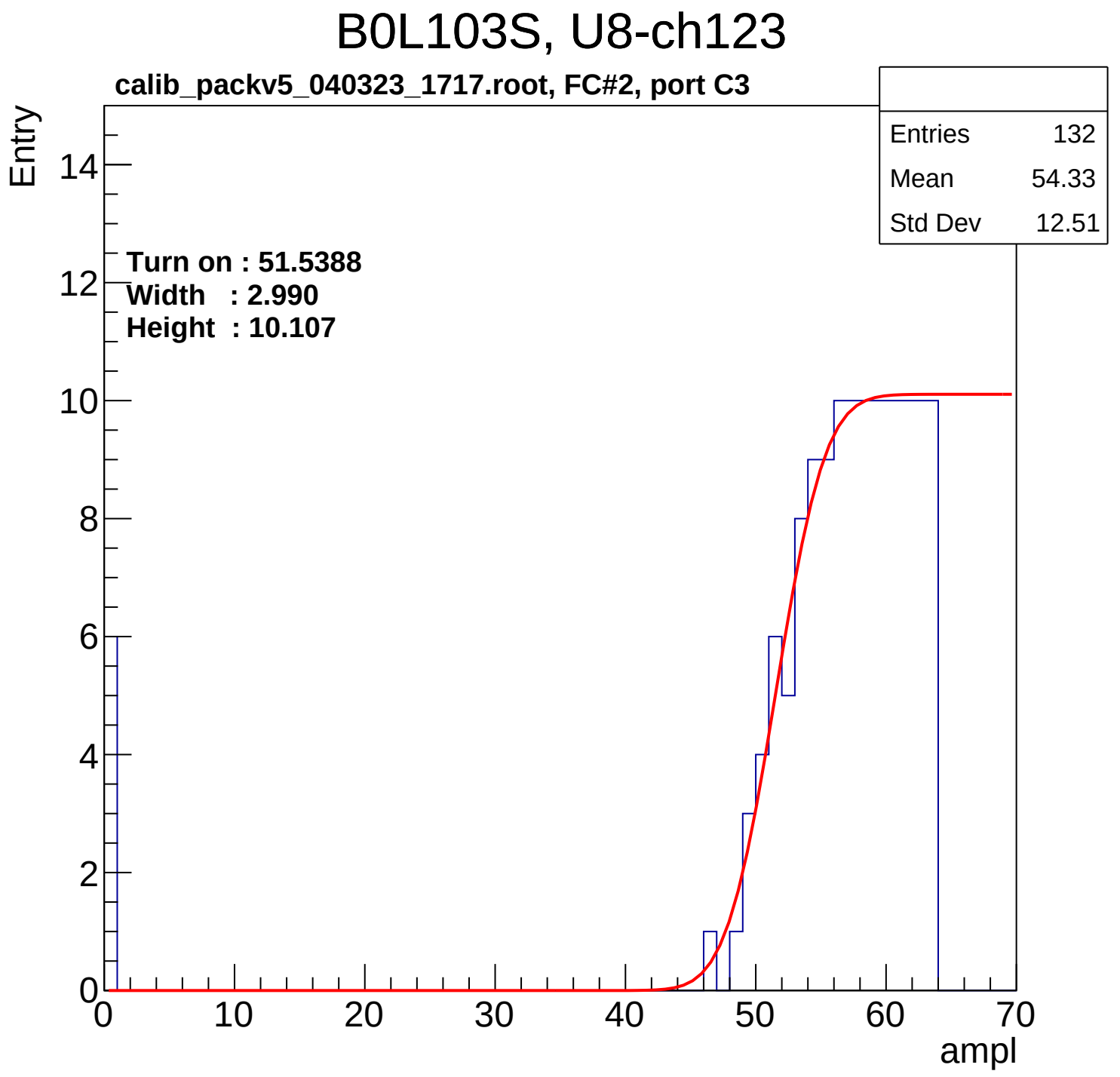
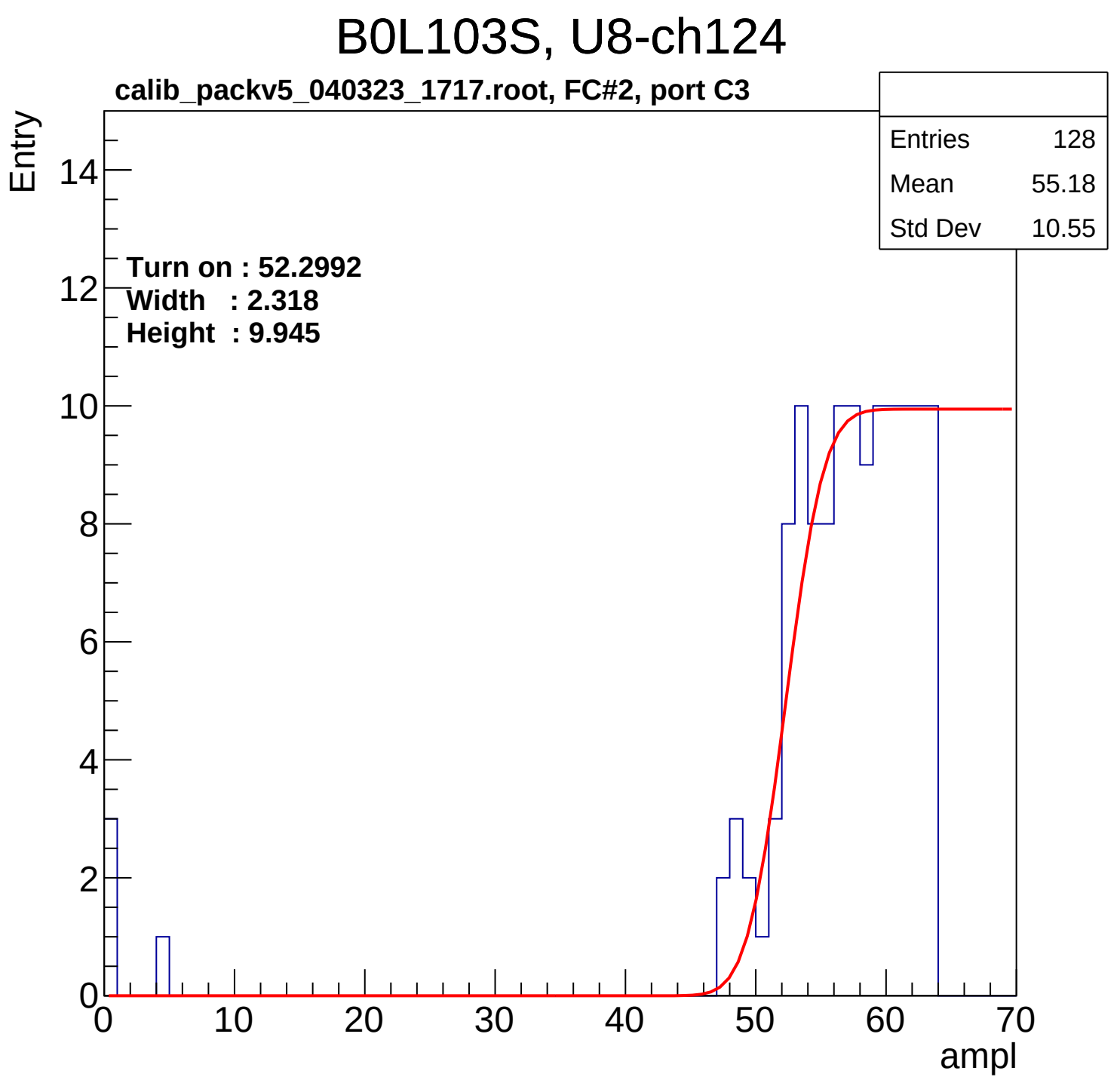
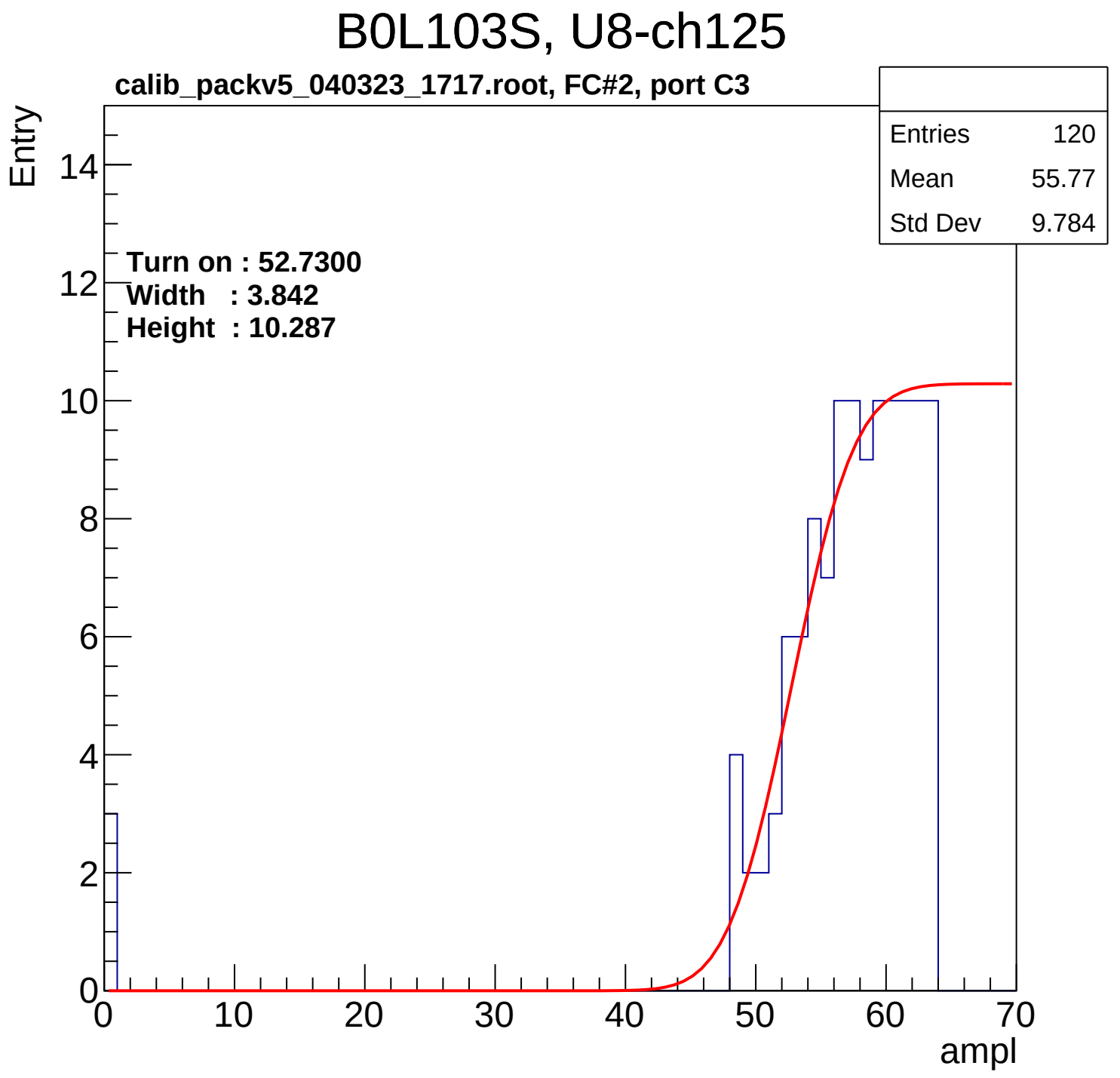

B0L103S, U8-ch123
calib_packv5_040323_1717.root, FC#2, port C3
Entries 132
Mean 54.33
Std Dev 12.51
Turn on : 51.5388
Width : 2.990
Height : 10.107
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L103S, U8-ch124
calib_packv5_040323_1717.root, FC#2, port C3
Entries 128
Mean 55.18
Std Dev 10.55
Turn on : 52.2992
Width : 2.318
Height : 9.945
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L103S, U8-ch125
calib_packv5_040323_1717.root, FC#2, port C3
Entries 120
Mean 55.77
Std Dev 9.784
Turn on : 52.7300
Width : 3.842
Height : 10.287
Entry
ampl
0
2
4
6
8
10
12
14
0
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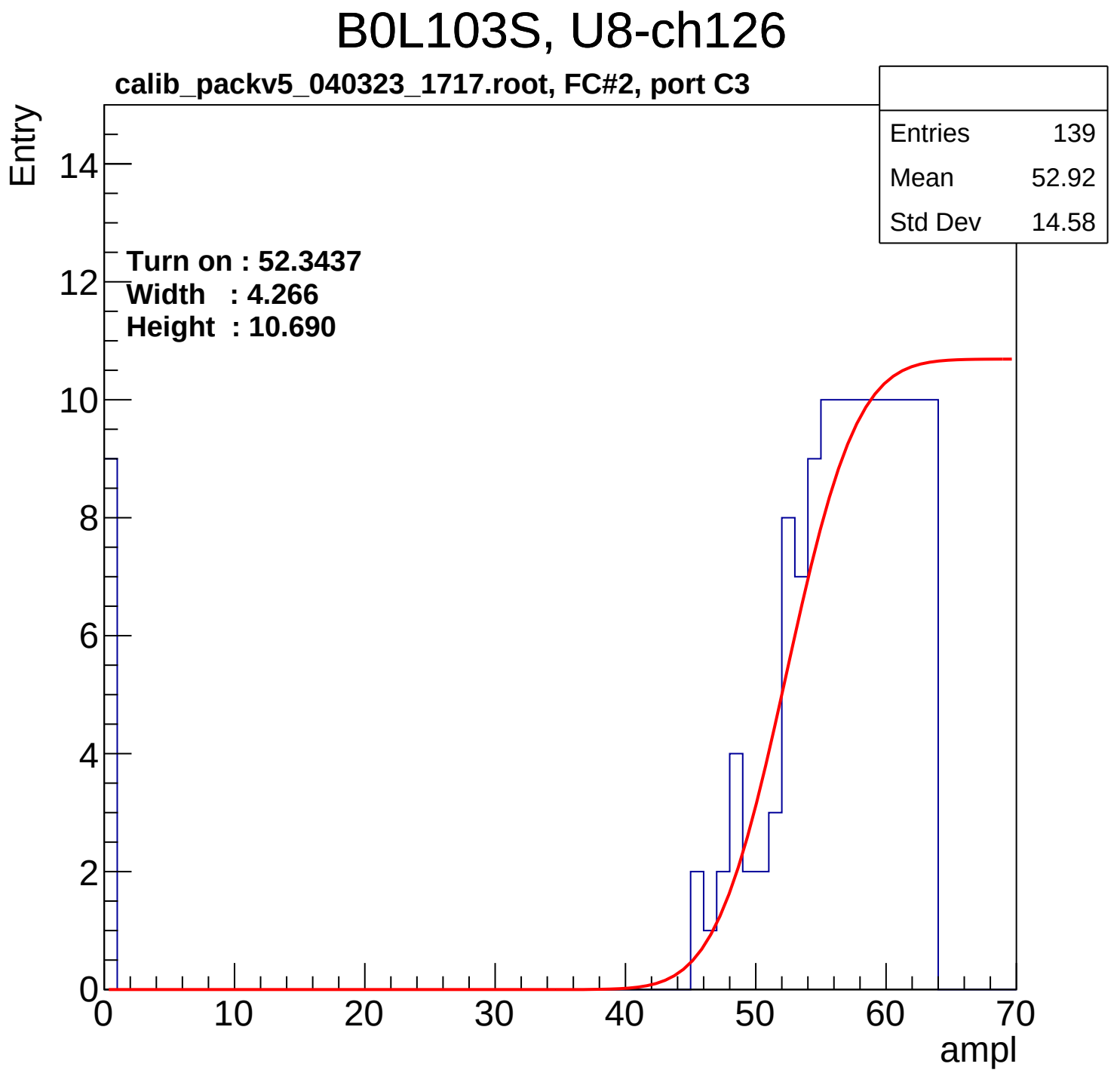
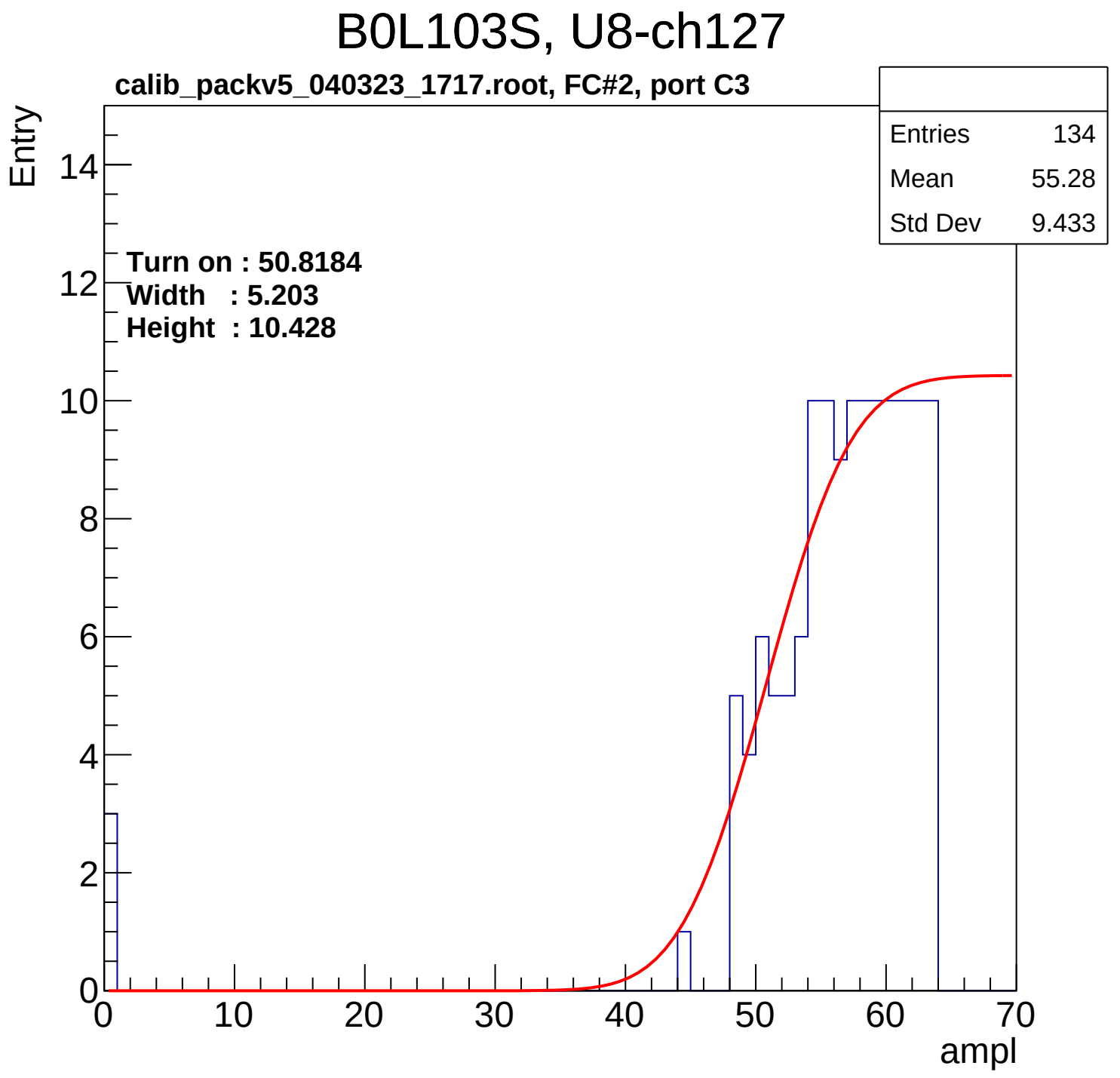
20
30
40
50
60
70


B0L103S, U8-ch126
calib_packv5_040323_1717.root, FC#2, port C3
Entries 139
Mean 52.92
Std Dev 14.58
Turn on : 52.3437
Width : 4.266
Height : 10.690
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L103S, U8-ch127
calib_packv5_040323_1717.root, FC#2, port C3
Entries 134
Mean 55.28
Std Dev 9.433
Turn on : 50.8184
Width : 5.203
Height : 10.428
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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60
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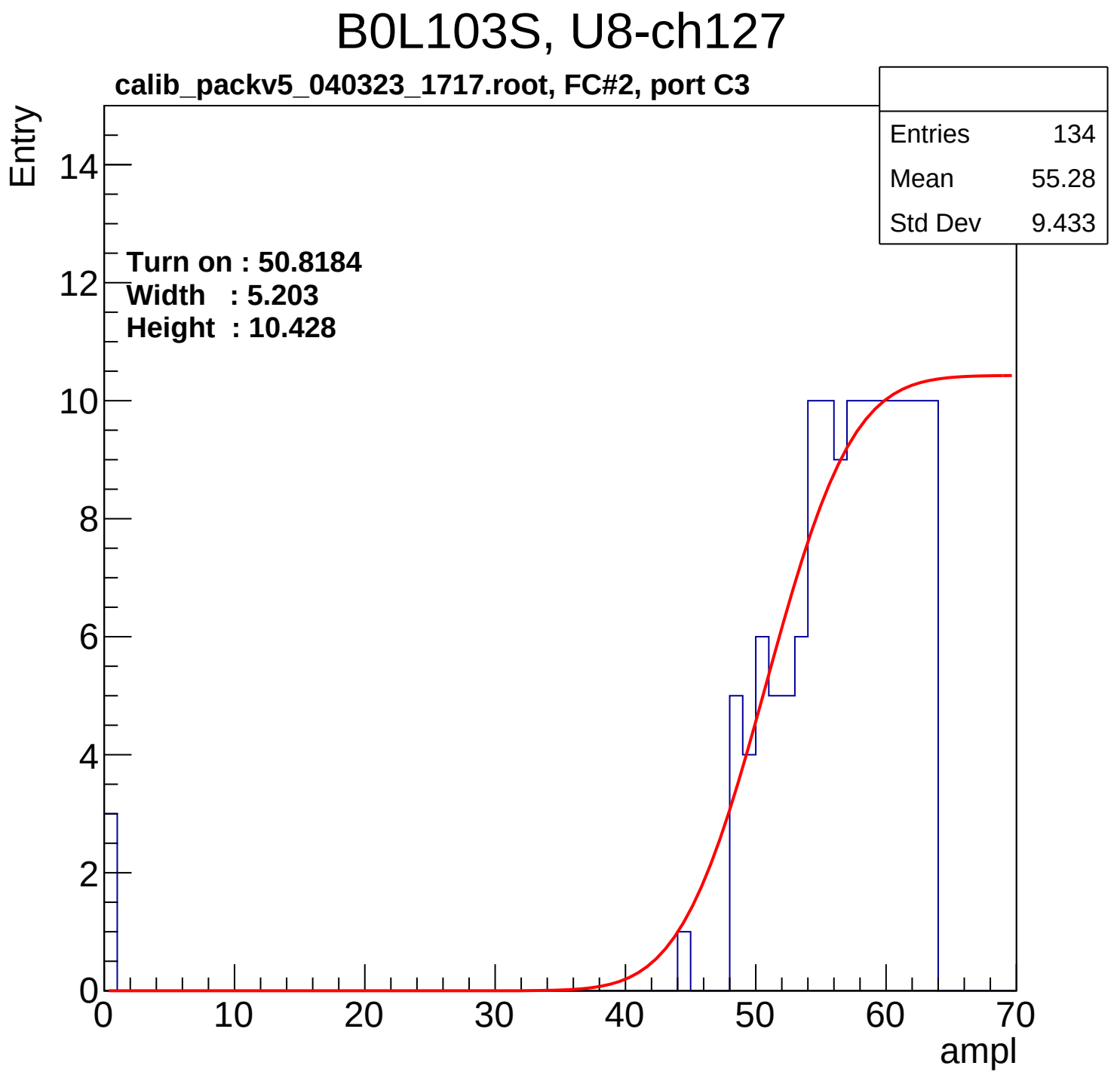
B0L103S, U8-ch127
calib_packv5_040323_1717.root, FC#2, port C3
Entries 134
Mean 55.28
Std Dev 9.433
Turn on : 50.8184
Width : 5.203
Height : 10.428
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70