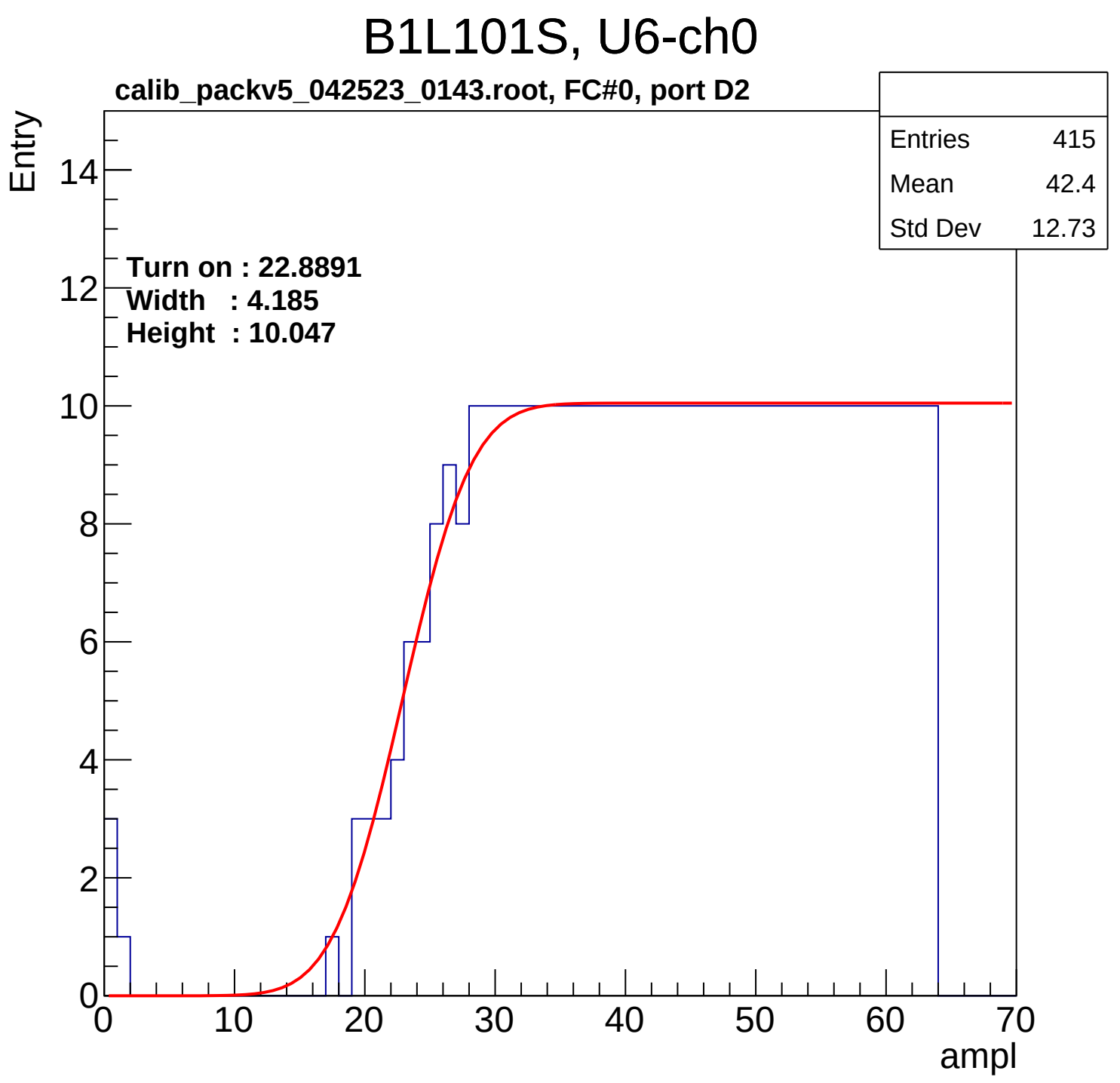
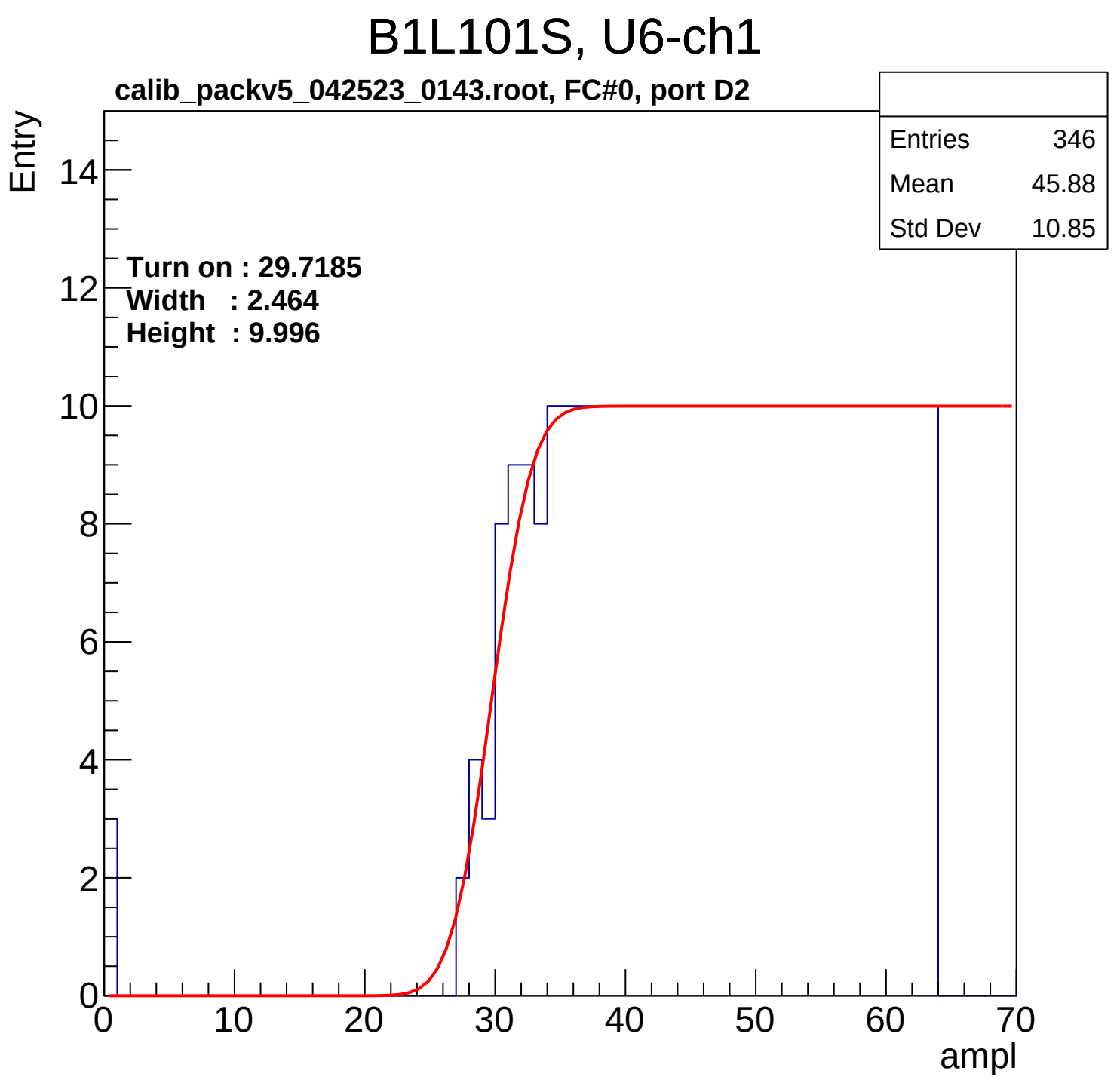
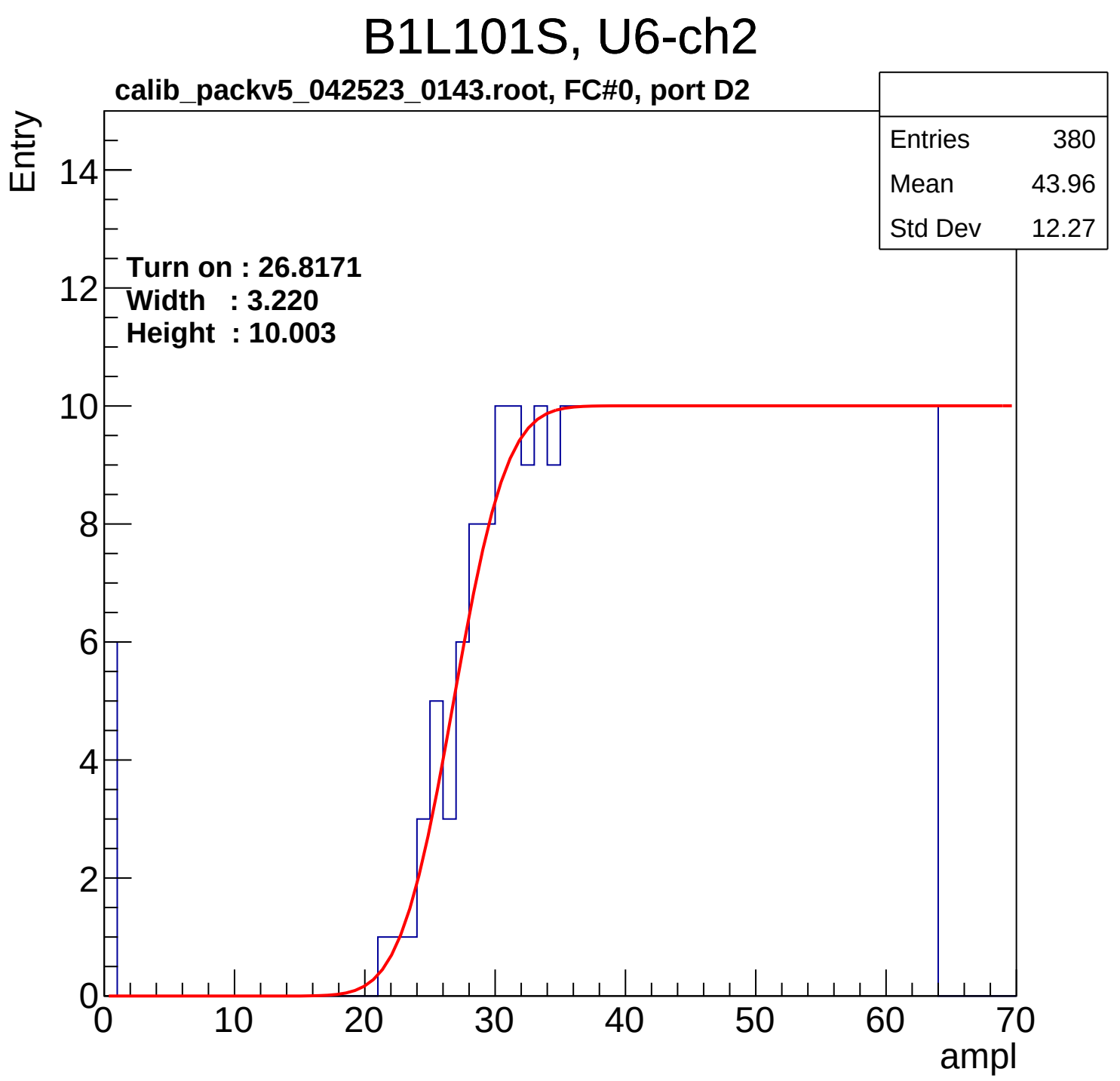
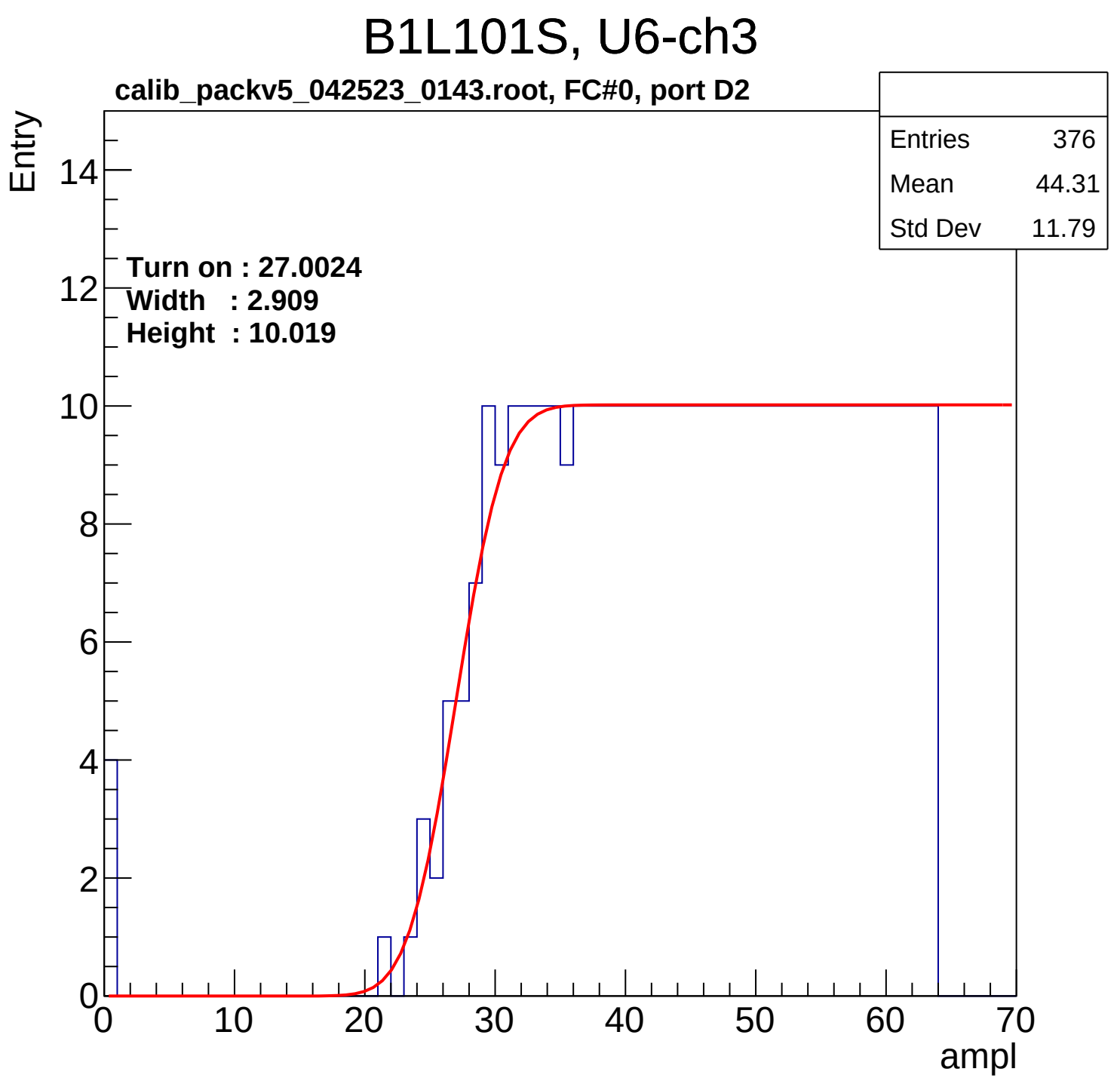
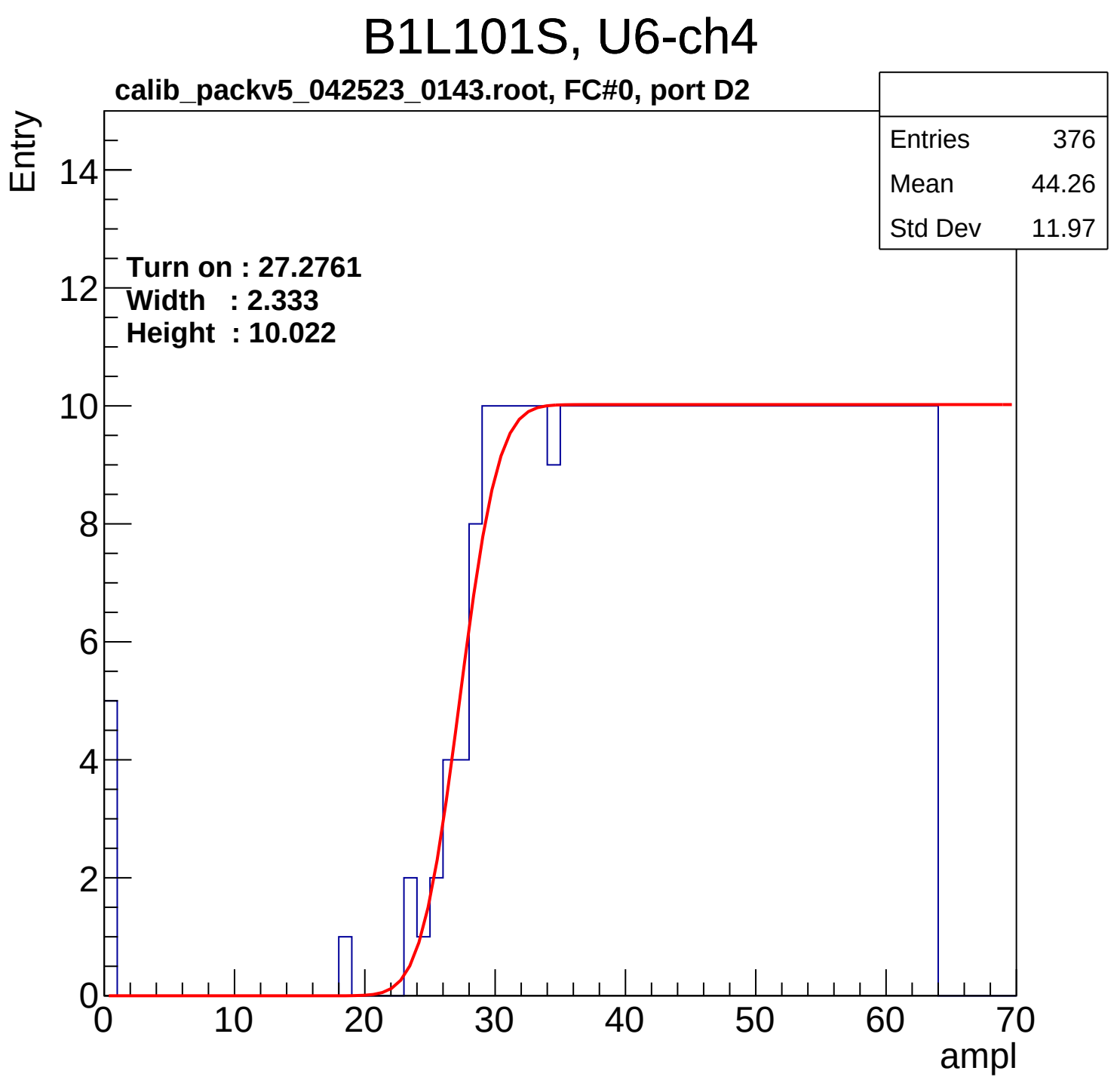
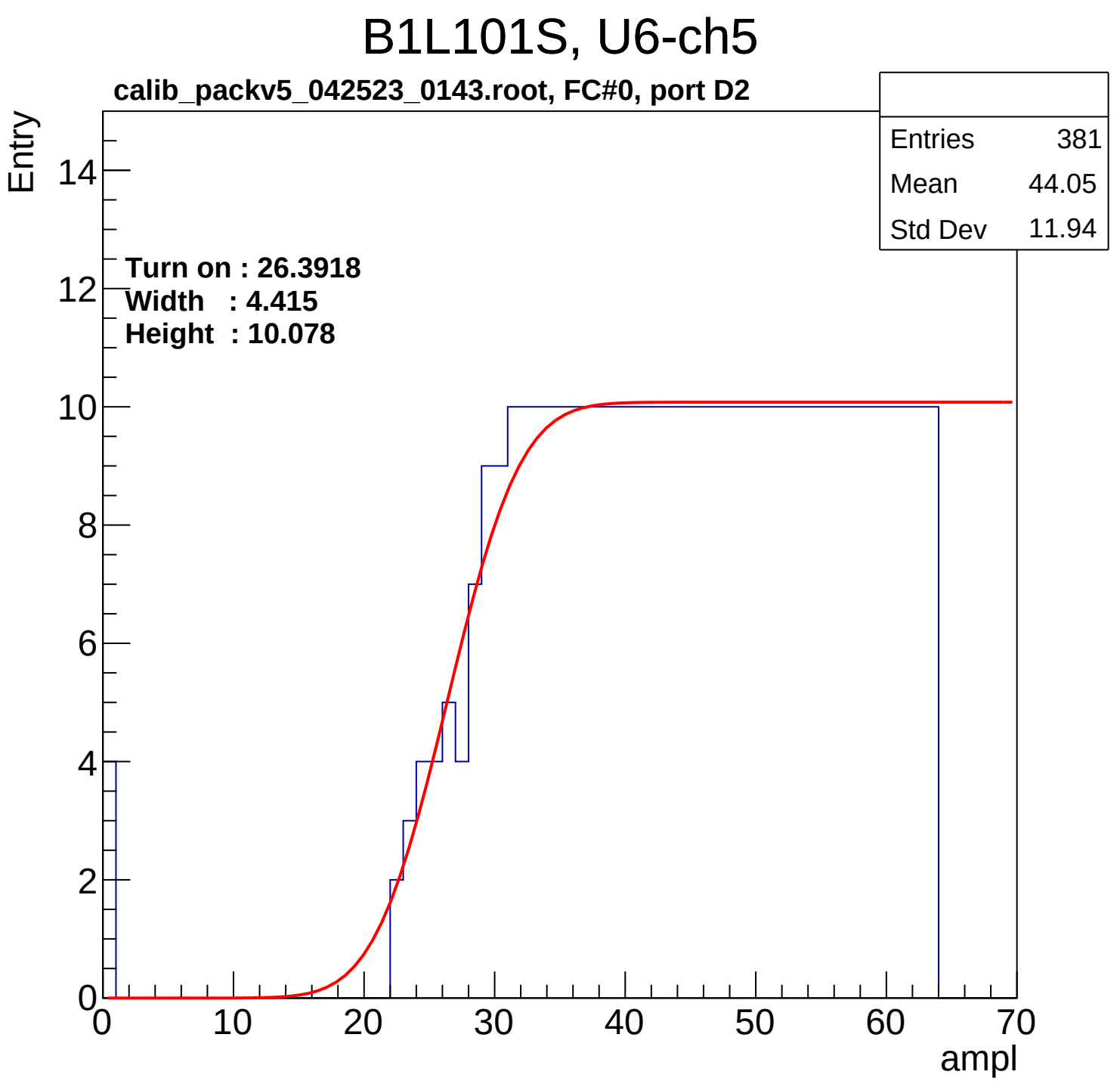

B1L101S, U6-ch0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 415
Mean 42.4
Std Dev 12.73
Turn on : 22.8891
Width : 4.185
Height : 10.047
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

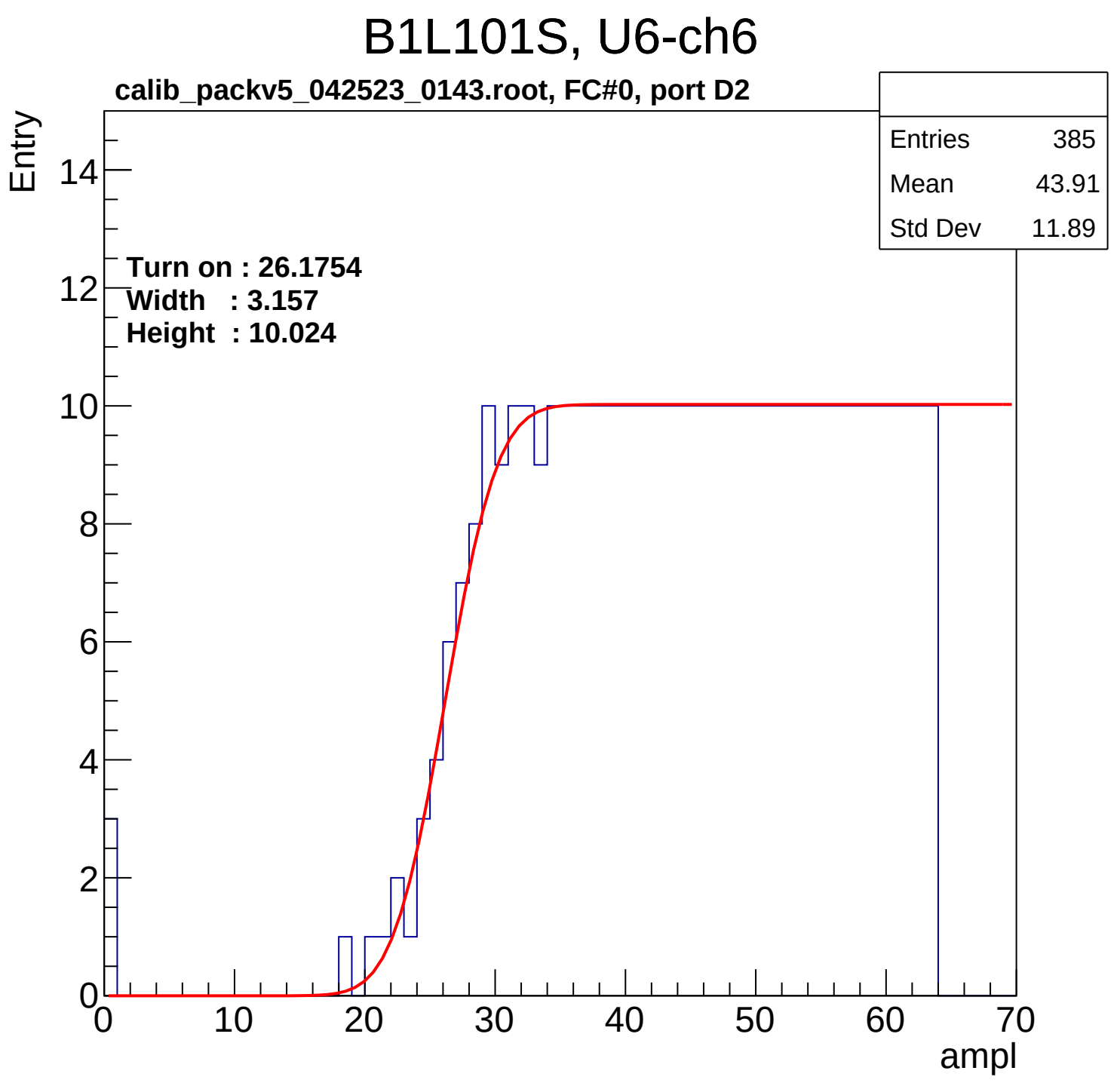

B1L101S, U6-ch1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 346
Mean 45.88
Std Dev 10.85
Turn on : 29.7185
Width : 2.464
Height : 9.996
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

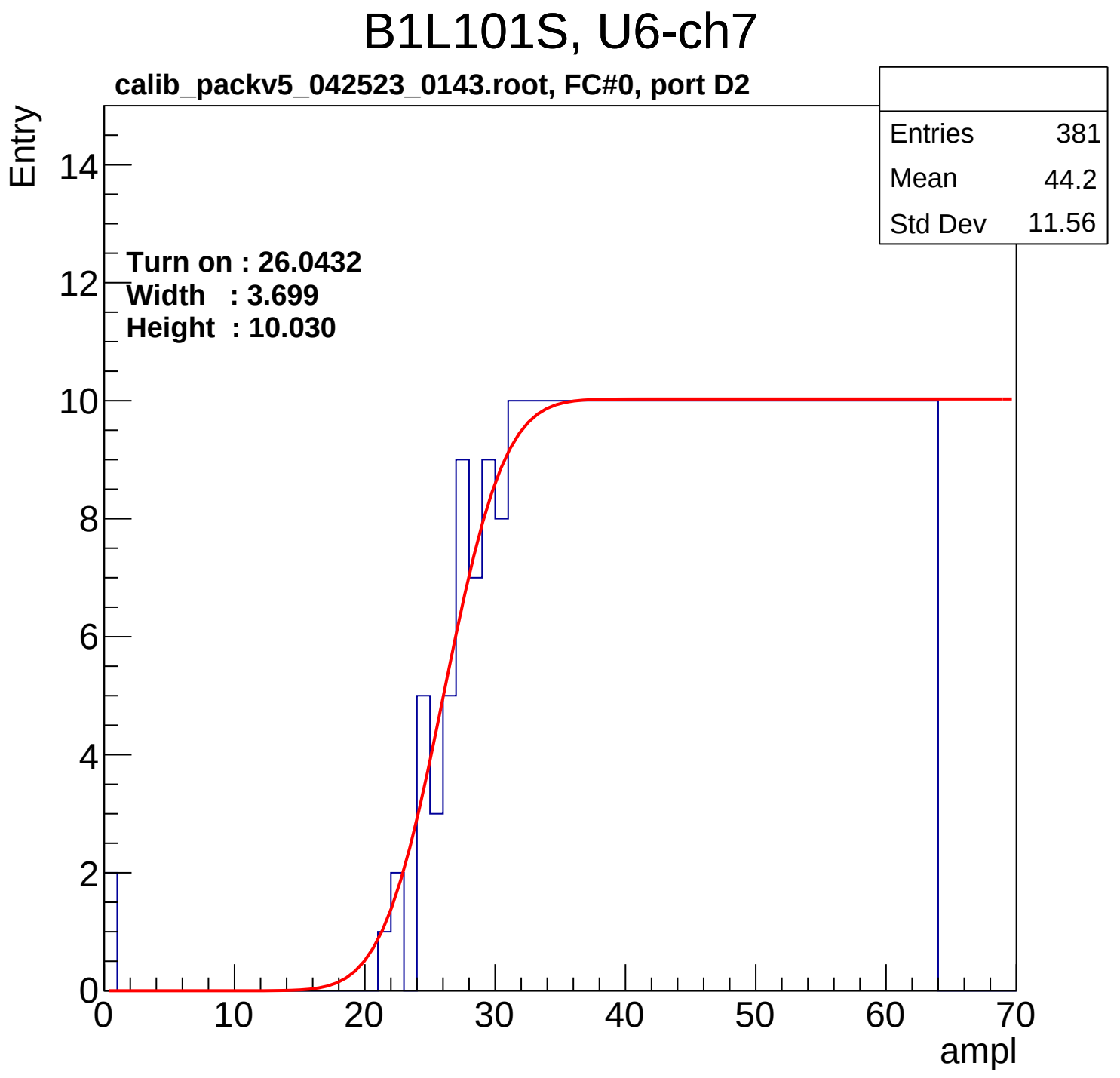

B1L101S, U6-ch2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 380
Mean 43.96
Std Dev 12.27
Turn on : 26.8171
Width : 3.220
Height : 10.003
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

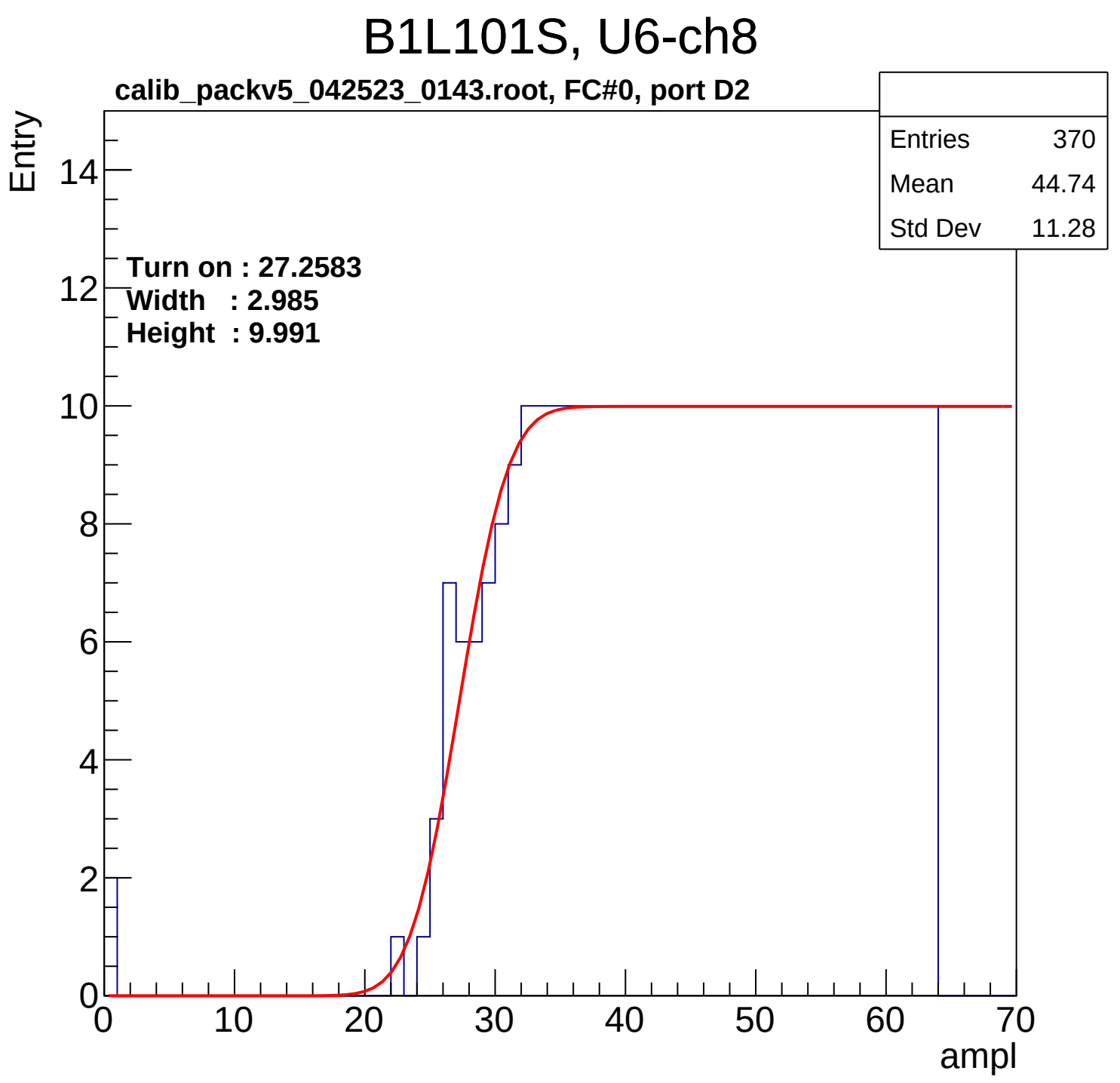

B1L101S, U6-ch3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 376
Mean 44.31
Std Dev 11.79
Turn on : 27.0024
Width : 2.909
Height : 10.019
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

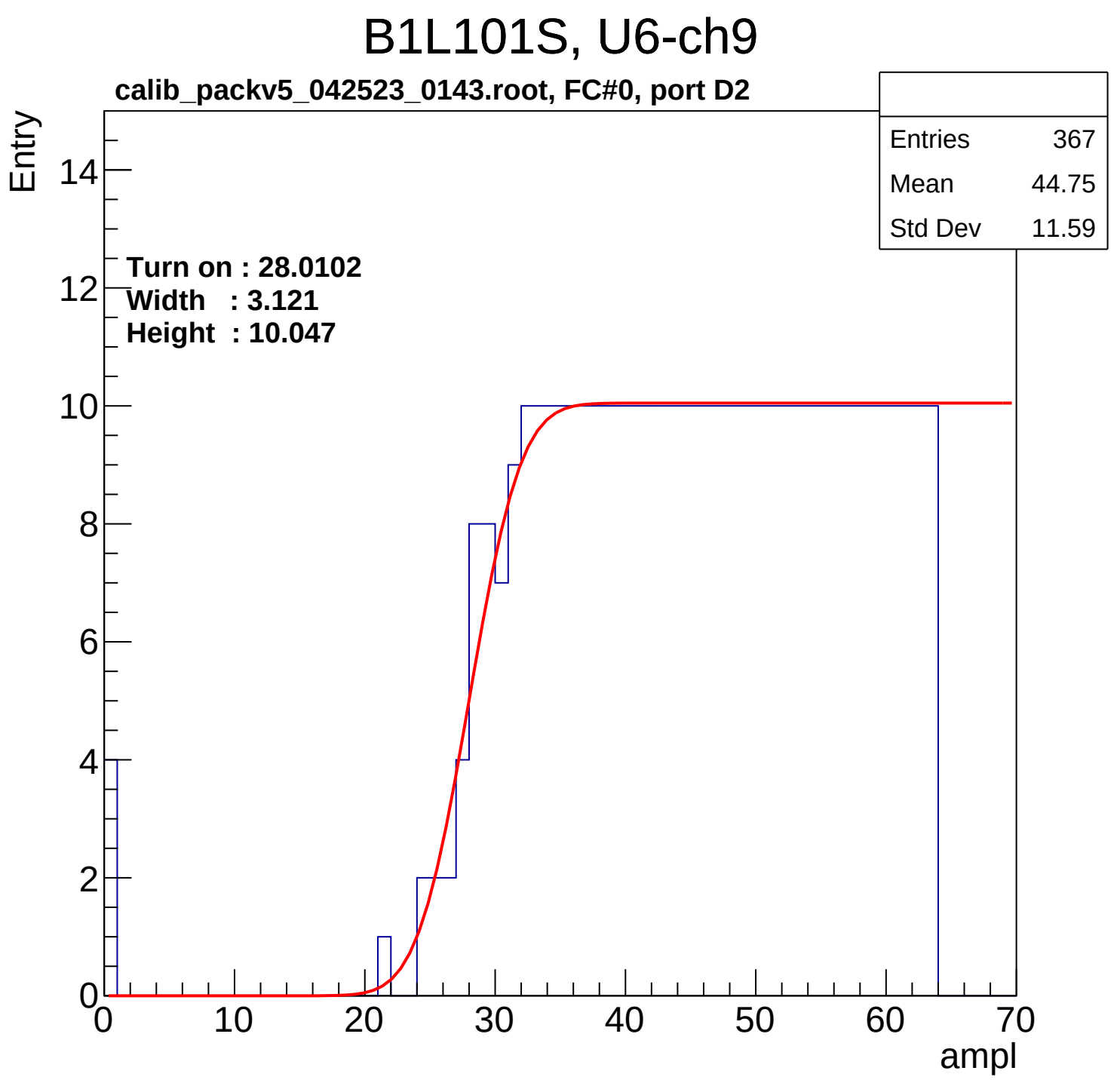

B1L101S, U6-ch4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 376
Mean 44.26
Std Dev 11.97
Turn on : 27.2761
Width : 2.333
Height : 10.022
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

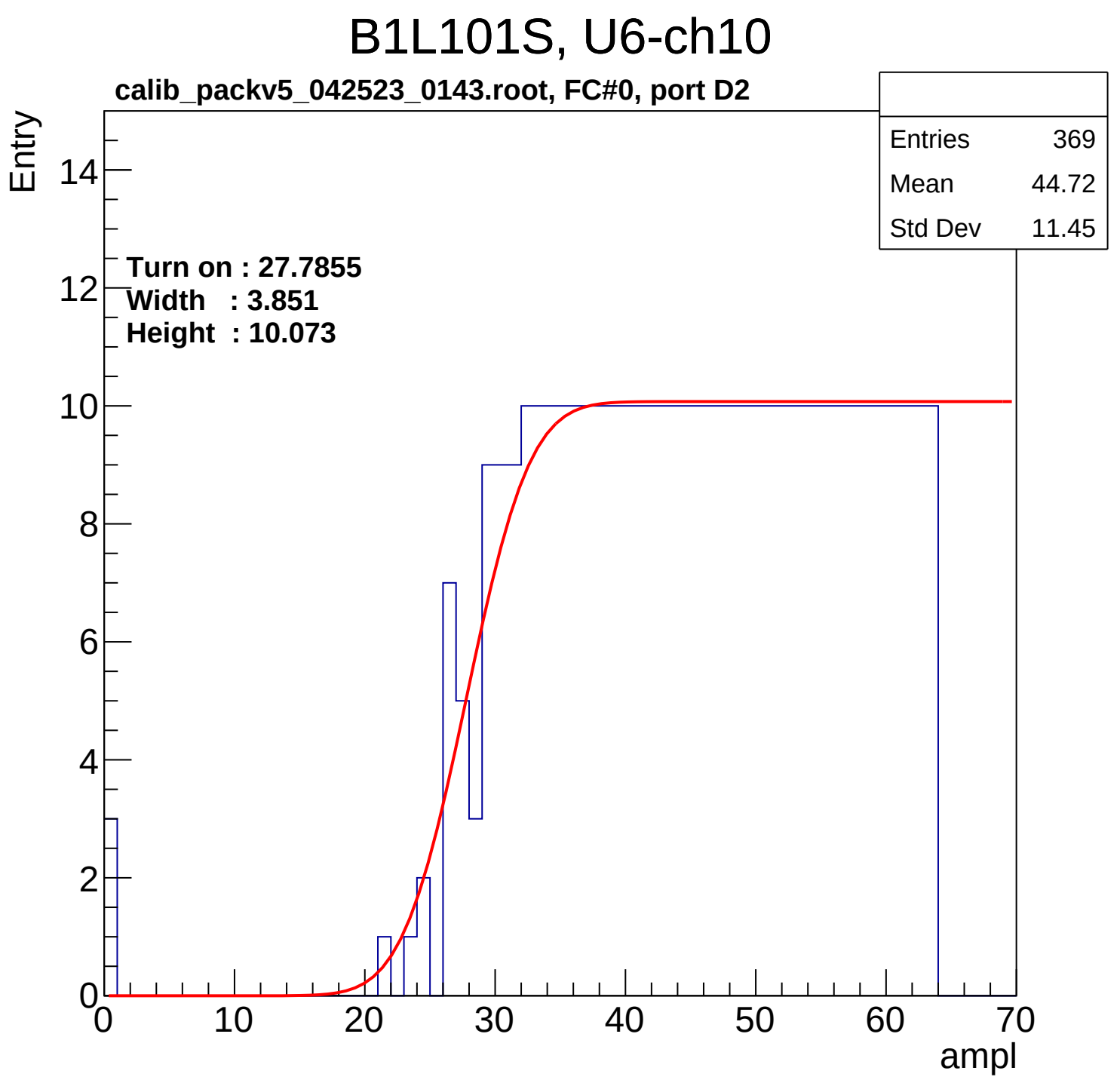

B1L101S, U6-ch5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 381
Mean 44.05
Std Dev 11.94
Turn on : 26.3918
Width : 4.415
Height : 10.078
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

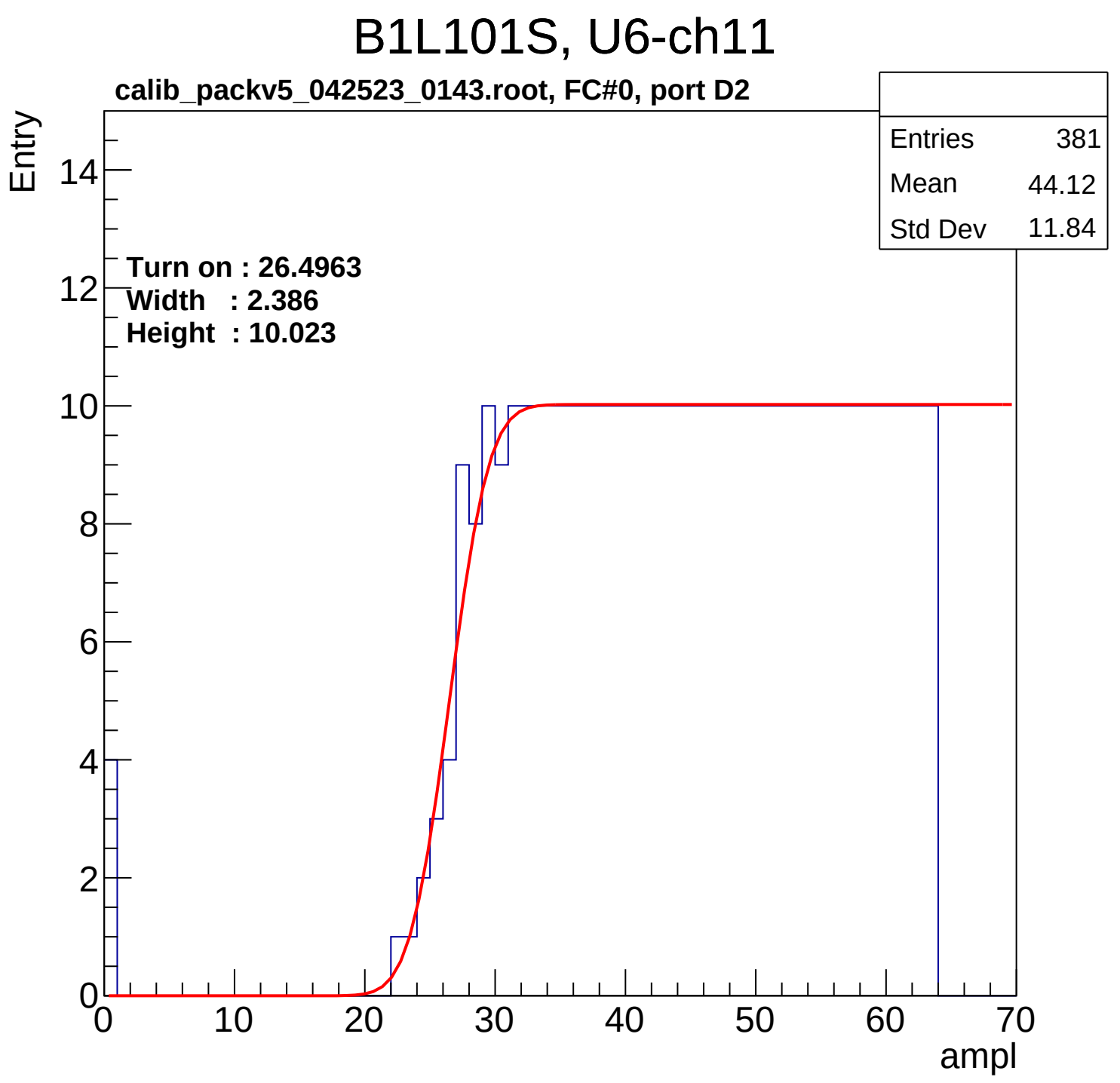

B1L101S, U6-ch6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 385
Mean 43.91
Std Dev 11.89
Turn on : 26.1754
Width : 3.157
Height : 10.024
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

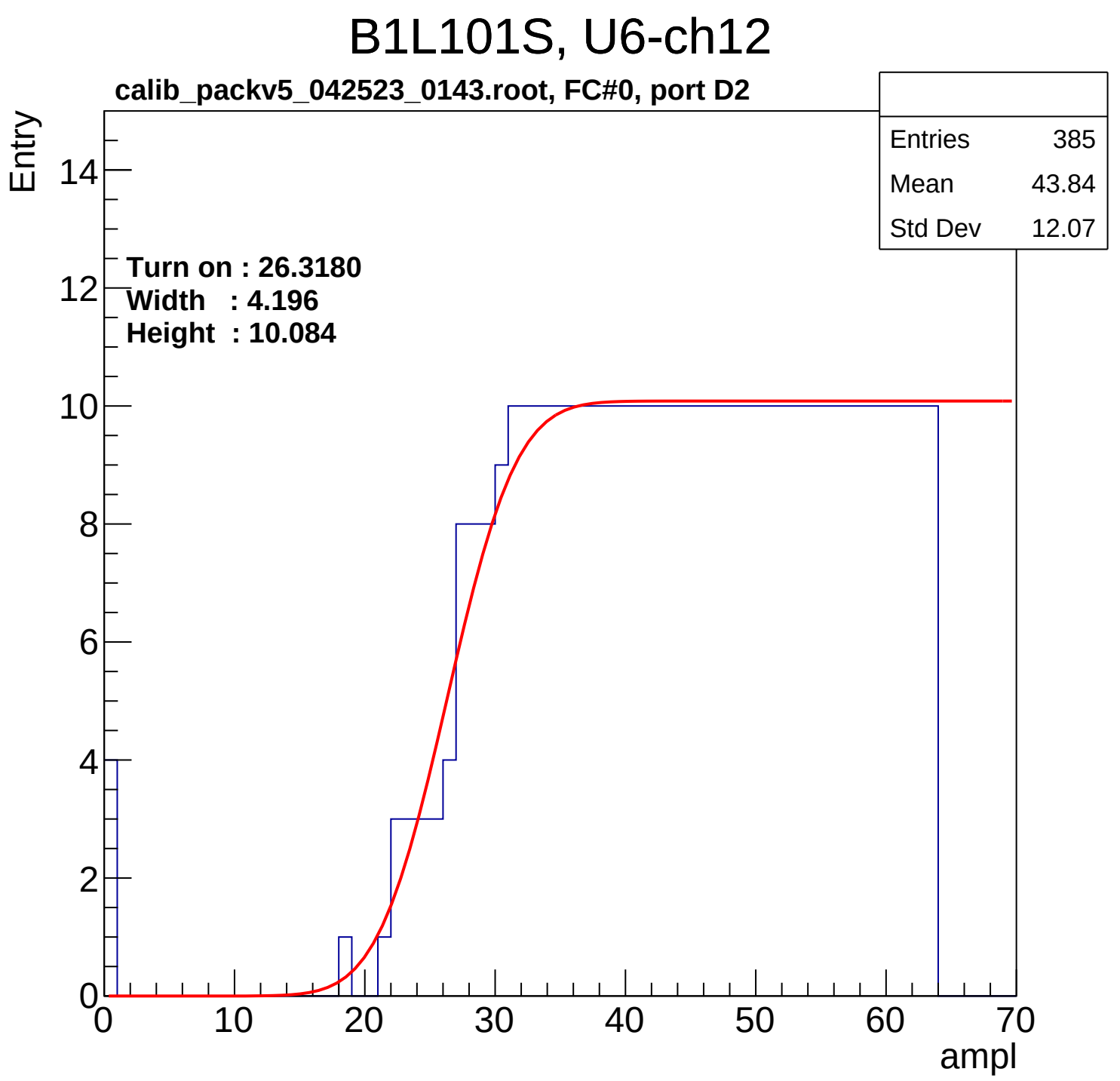

B1L101S, U6-ch7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 381
Mean 44.2
Std Dev 11.56
Turn on : 26.0432
Width : 3.699
Height : 10.030
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

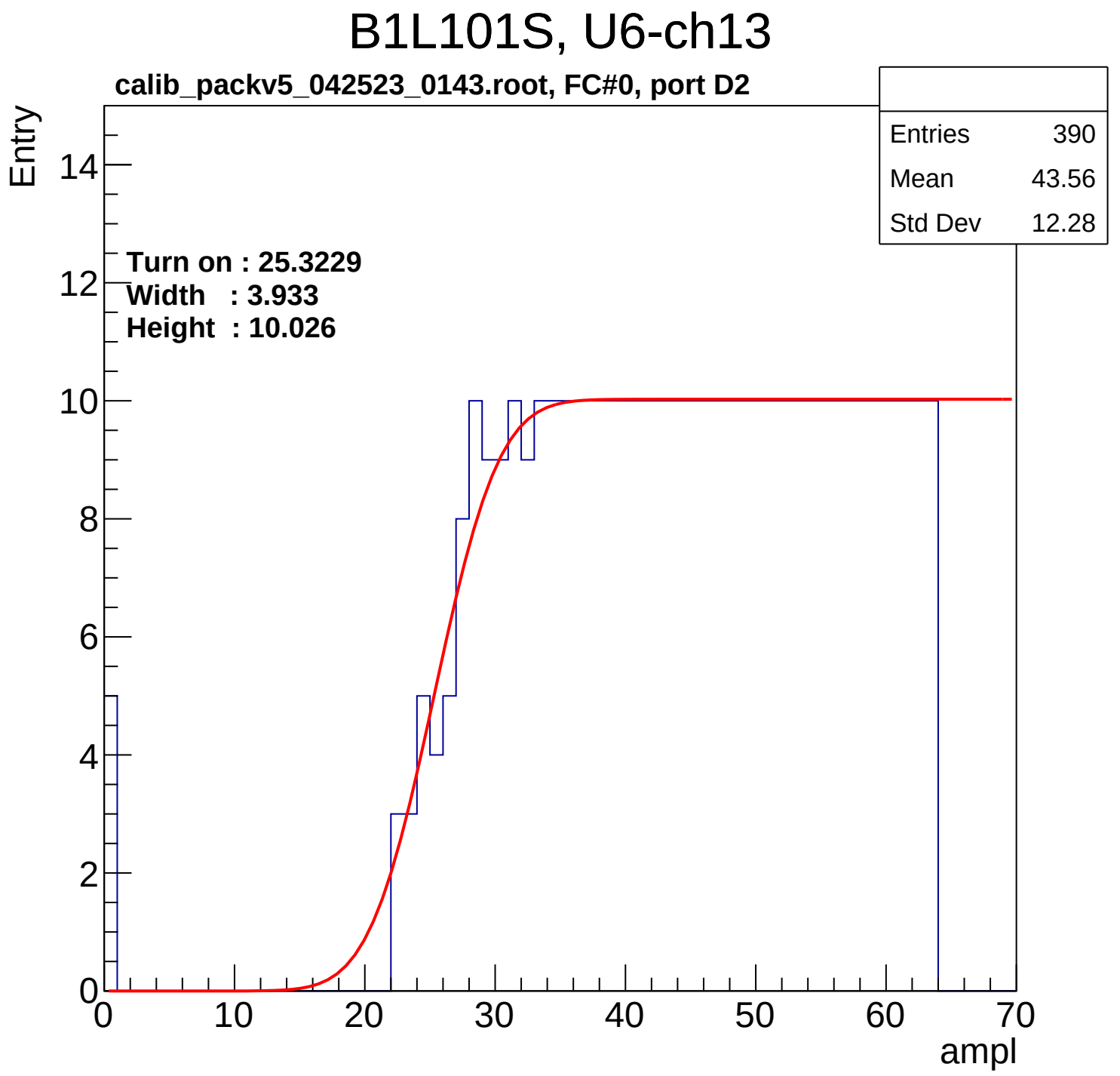

B1L101S, U6-ch8
calib_packv5_042523_0143.root, FC#0, port D2
Entries 370
Mean 44.74
Std Dev 11.28
Turn on : 27.2583
Width : 2.985
Height : 9.991
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

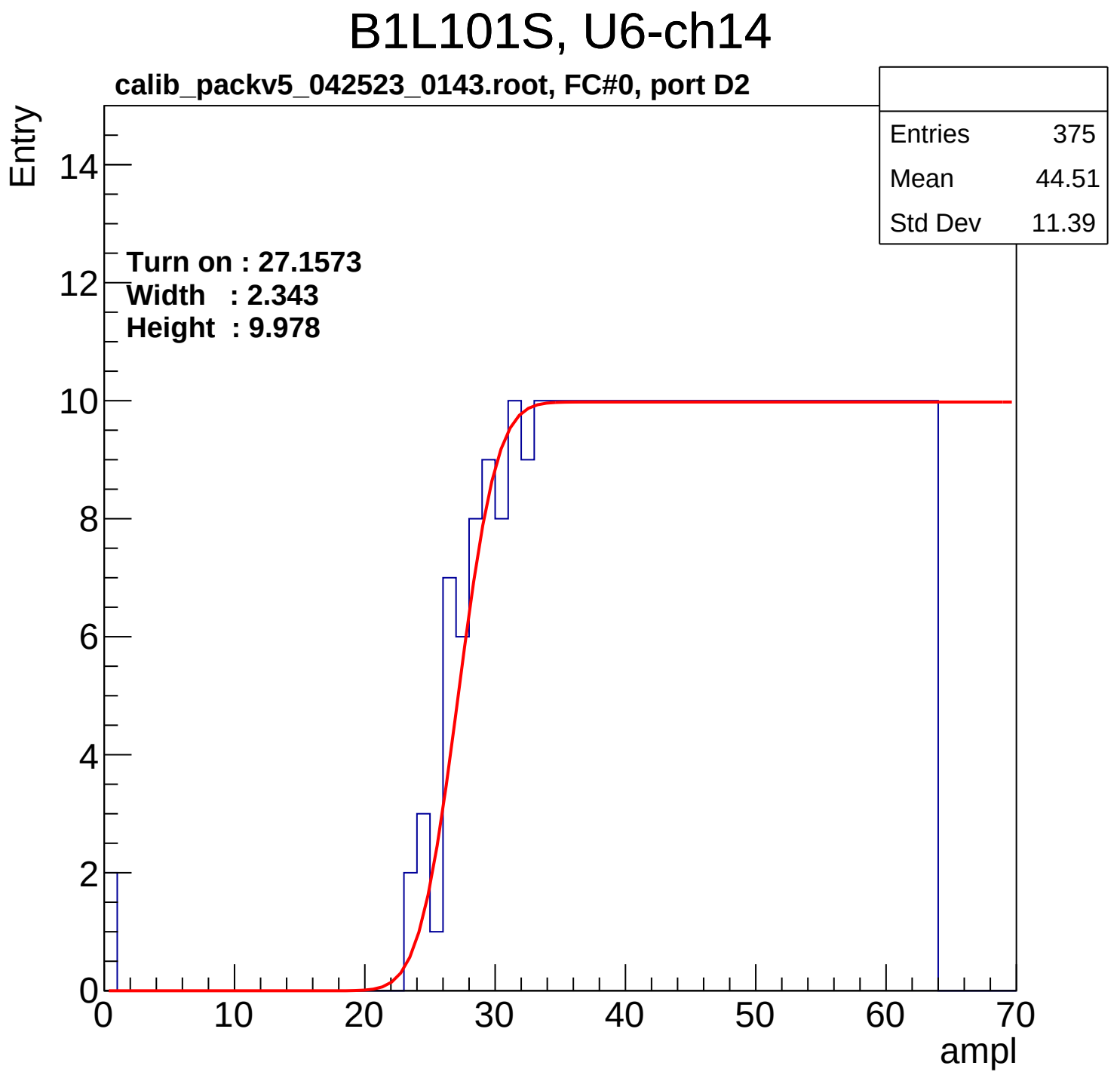

B1L101S, U6-ch9
calib_packv5_042523_0143.root, FC#0, port D2
Entries 367
Mean 44.75
Std Dev 11.59
Turn on : 28.0102
Width : 3.121
Height : 10.047
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

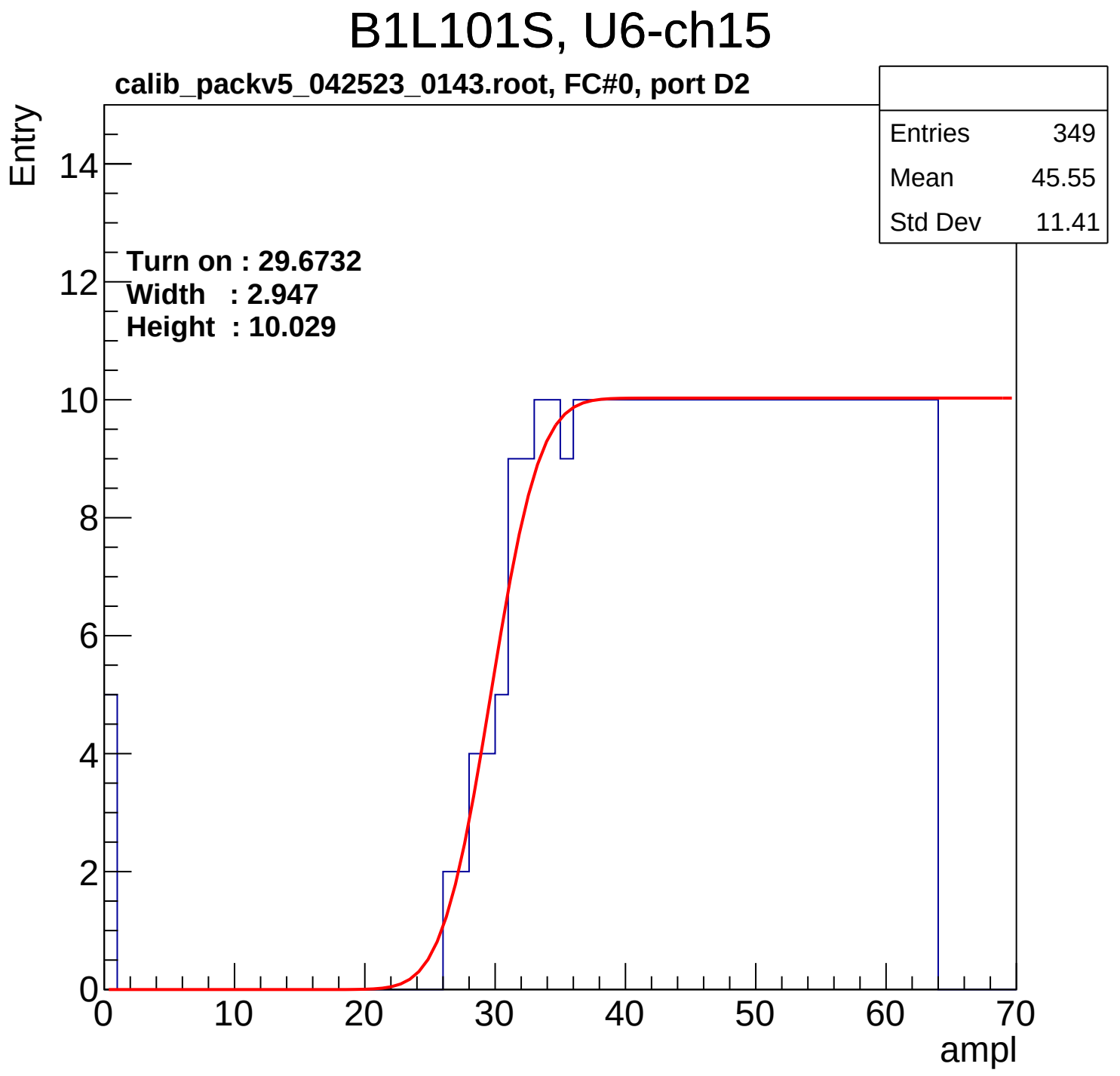

B1L101S, U6-ch10
calib_packv5_042523_0143.root, FC#0, port D2
Entries 369
Mean 44.72
Std Dev 11.45
Turn on : 27.7855
Width : 3.851
Height : 10.073
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

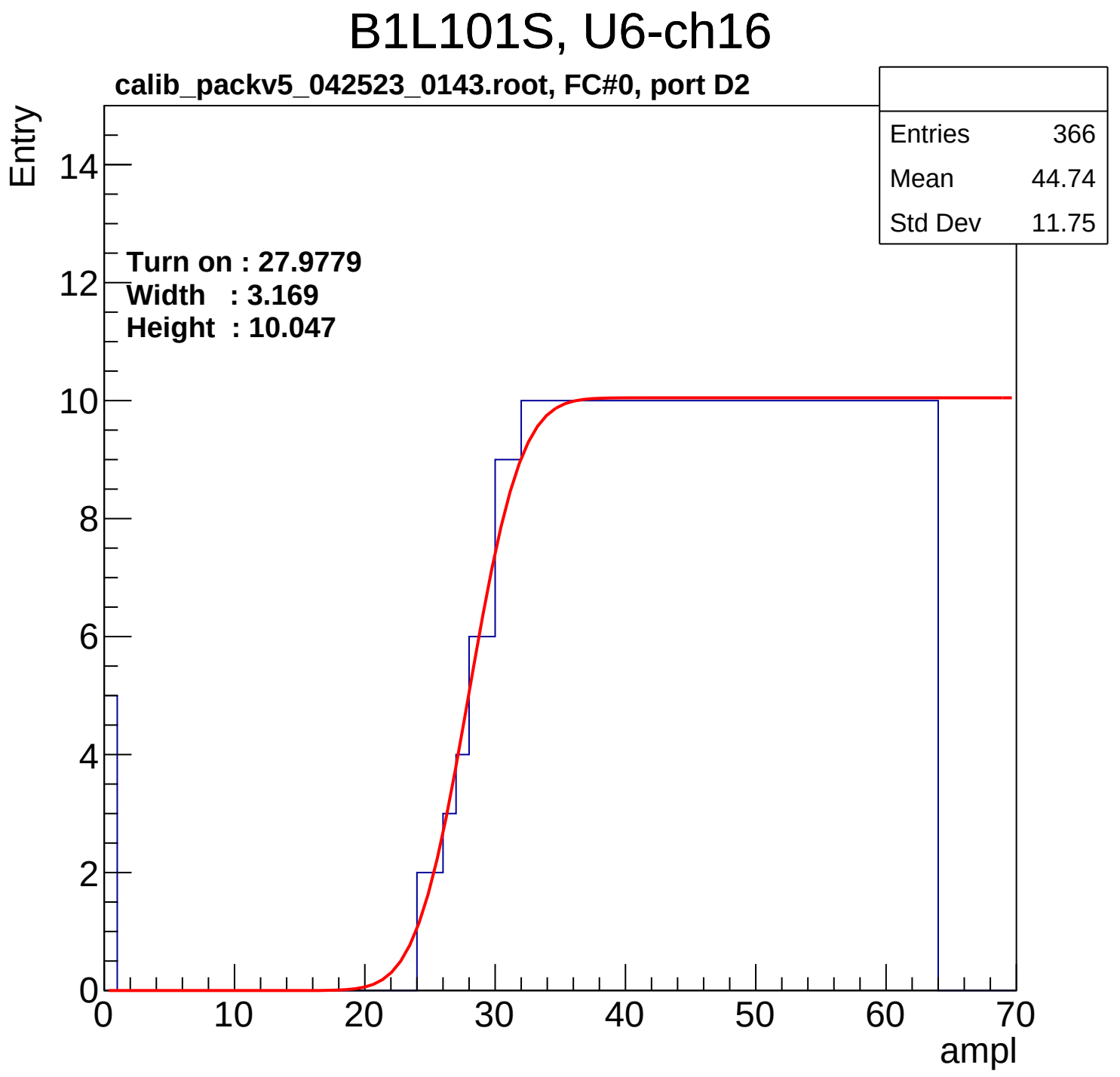

B1L101S, U6-ch11
calib_packv5_042523_0143.root, FC#0, port D2
Entries 381
Mean 44.12
Std Dev 11.84
Turn on : 26.4963
Width : 2.386
Height : 10.023
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

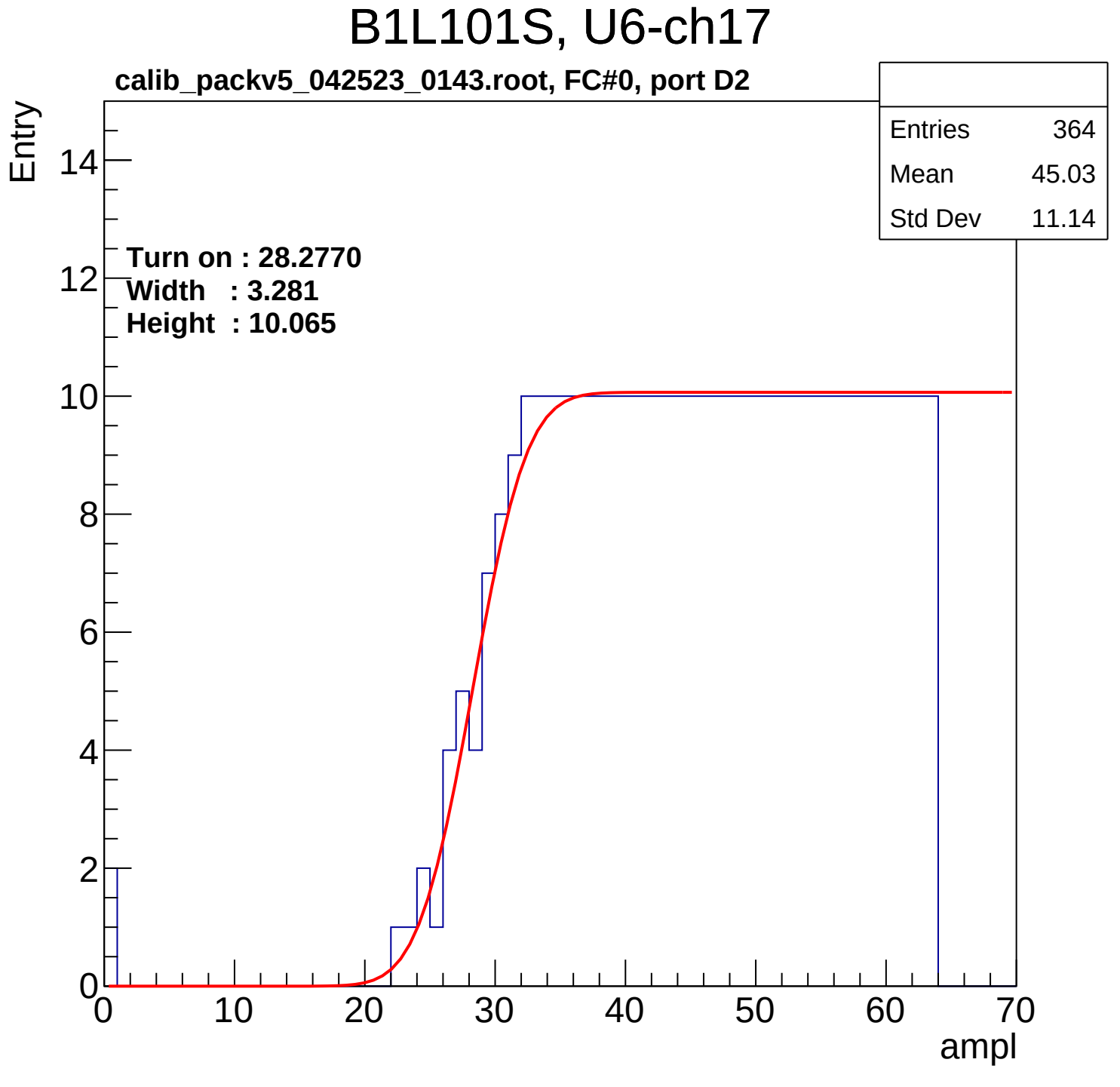

B1L101S, U6-ch12
calib_packv5_042523_0143.root, FC#0, port D2
Entries 385
Mean 43.84
Std Dev 12.07
Turn on : 26.3180
Width : 4.196
Height : 10.084
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

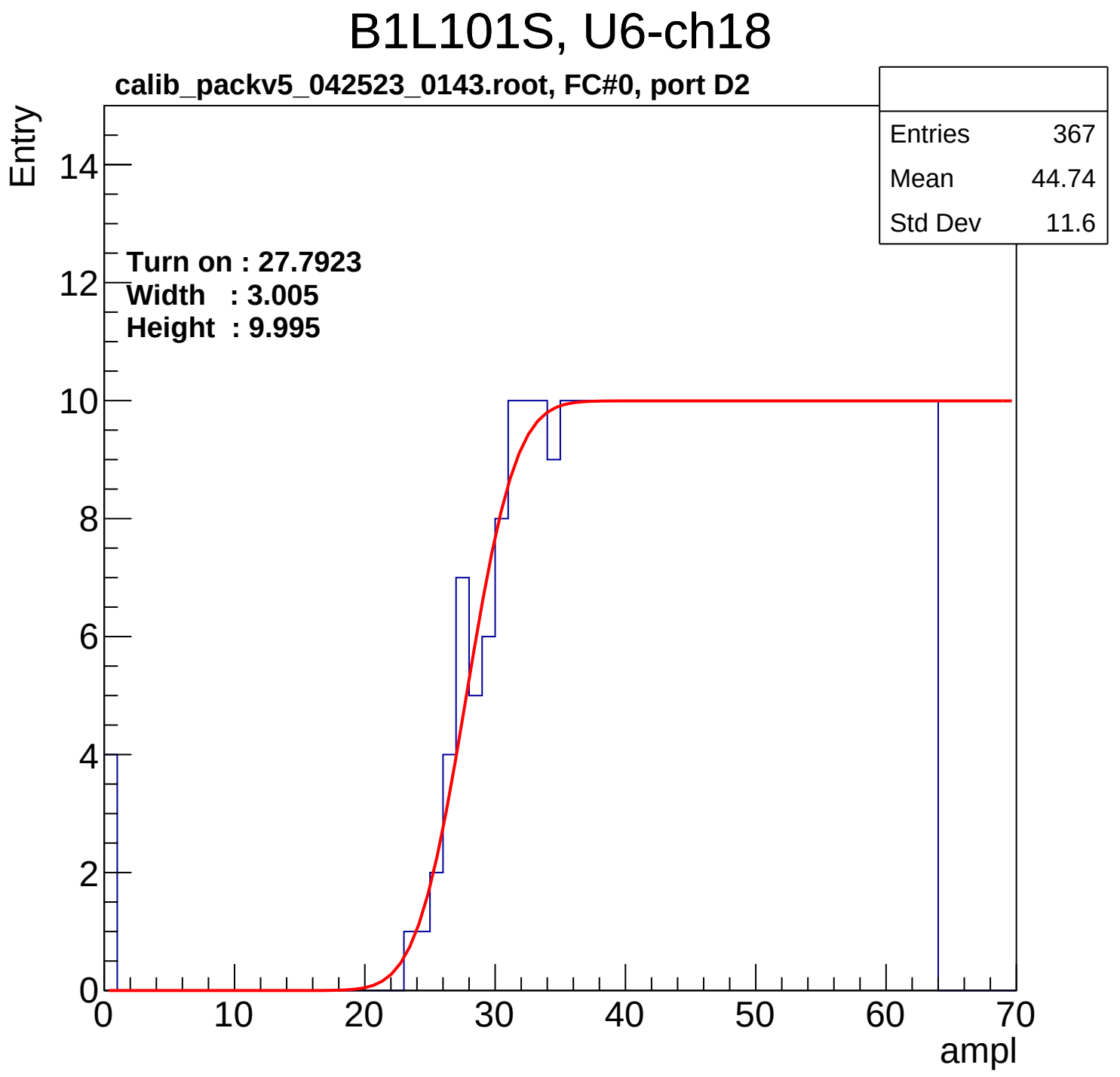

B1L101S, U6-ch13
calib_packv5_042523_0143.root, FC#0, port D2
Entries 390
Mean 43.56
Std Dev 12.28
Turn on : 25.3229
Width : 3.933
Height : 10.026
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

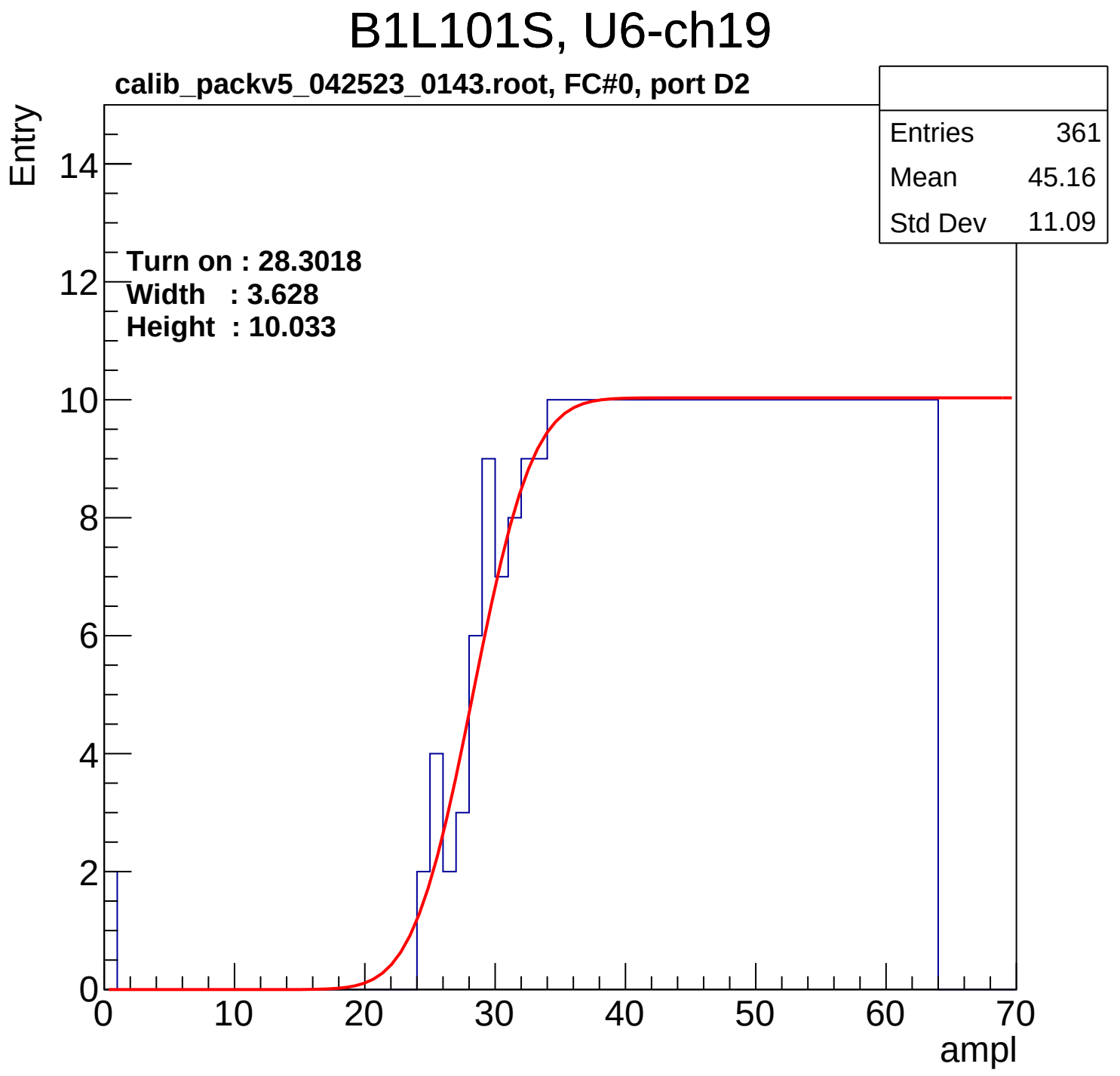

B1L101S, U6-ch14
calib_packv5_042523_0143.root, FC#0, port D2
Entries 375
Mean 44.51
Std Dev 11.39
Turn on : 27.1573
Width : 2.343
Height : 9.978
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

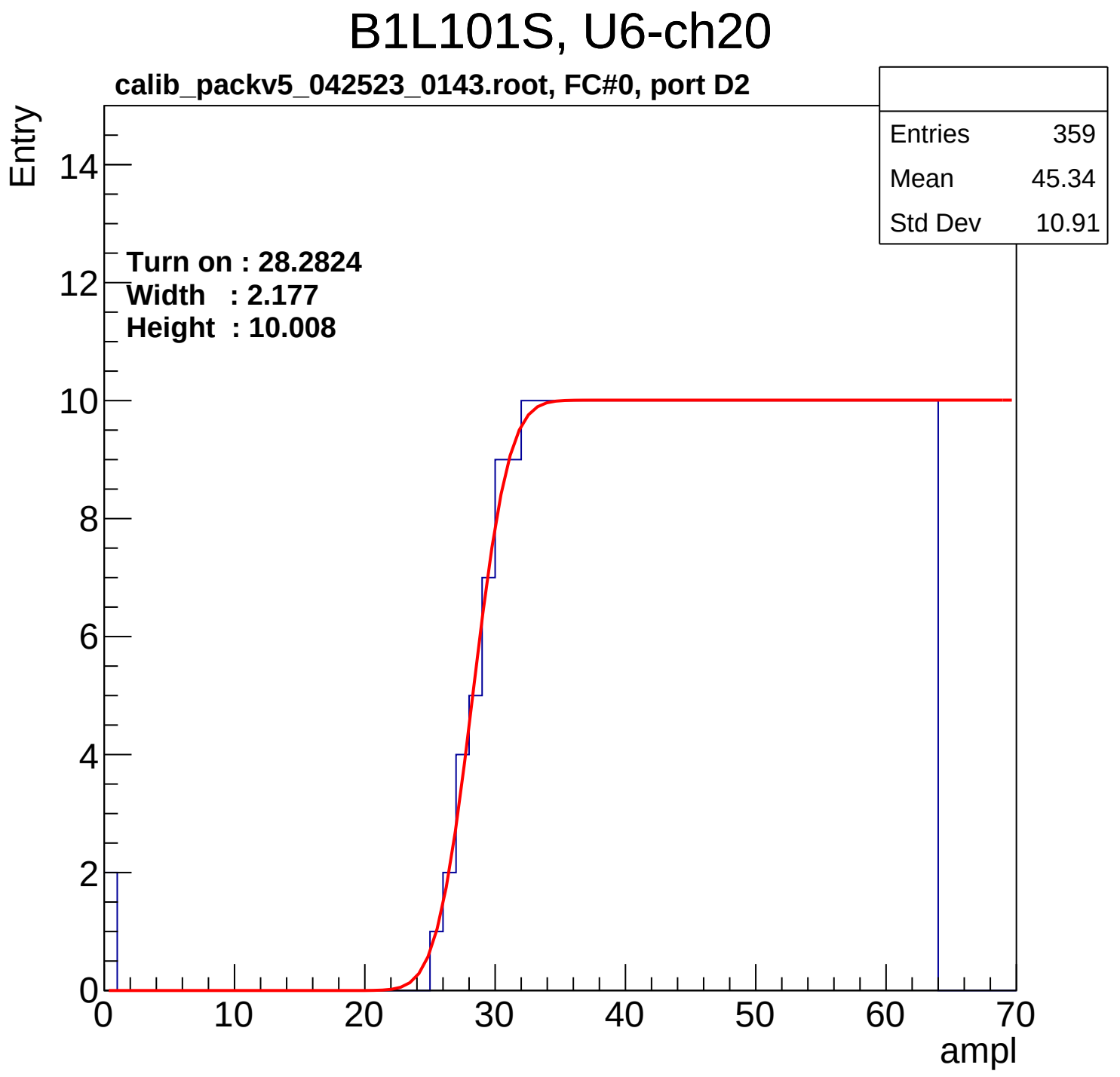

B1L101S, U6-ch15
calib_packv5_042523_0143.root, FC#0, port D2
Entries 349
Mean 45.55
Std Dev 11.41
Turn on : 29.6732
Width : 2.947
Height : 10.029
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

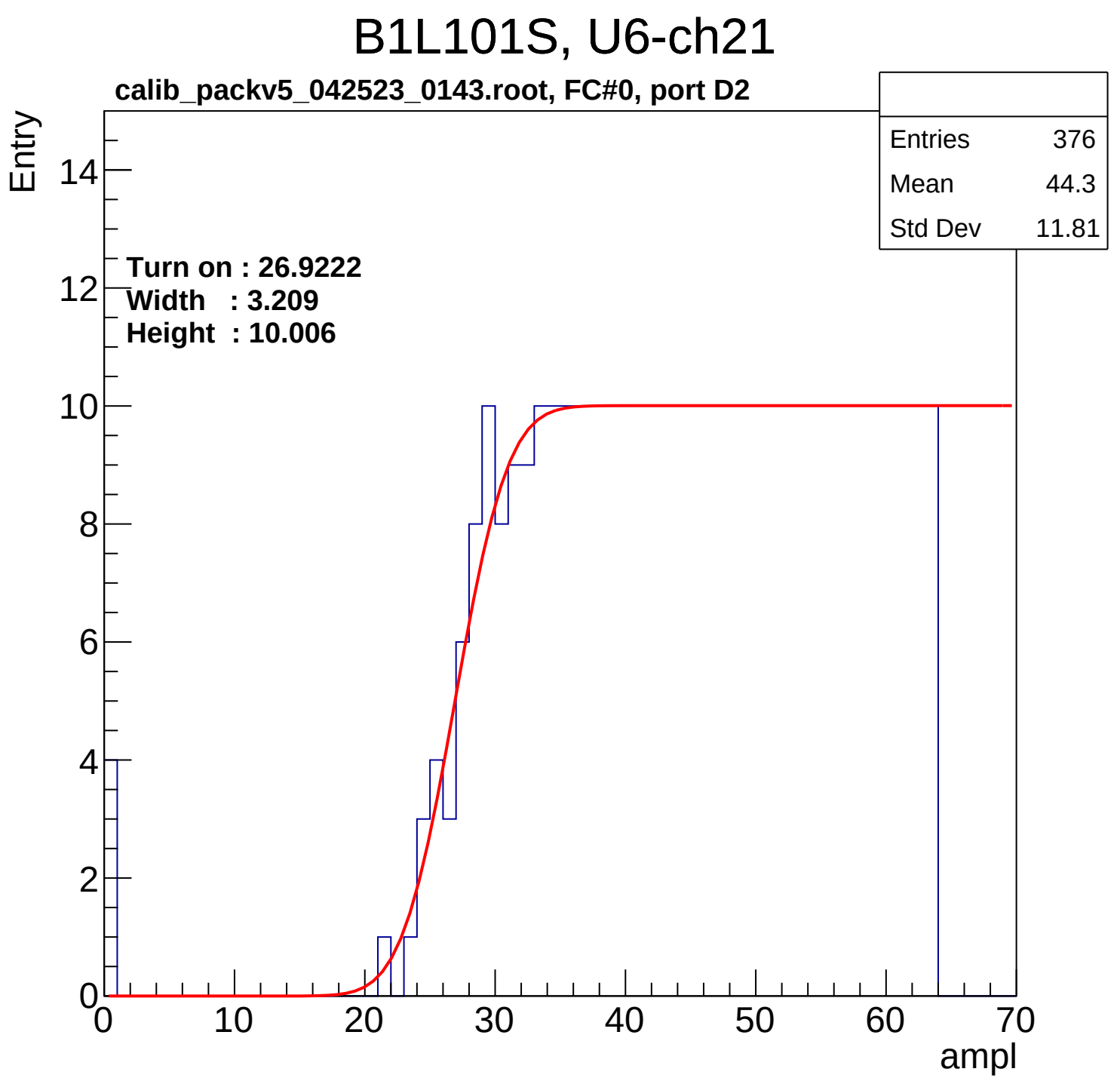

B1L101S, U6-ch16
calib_packv5_042523_0143.root, FC#0, port D2
Entries 366
Mean 44.74
Std Dev 11.75
Turn on : 27.9779
Width : 3.169
Height : 10.047
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

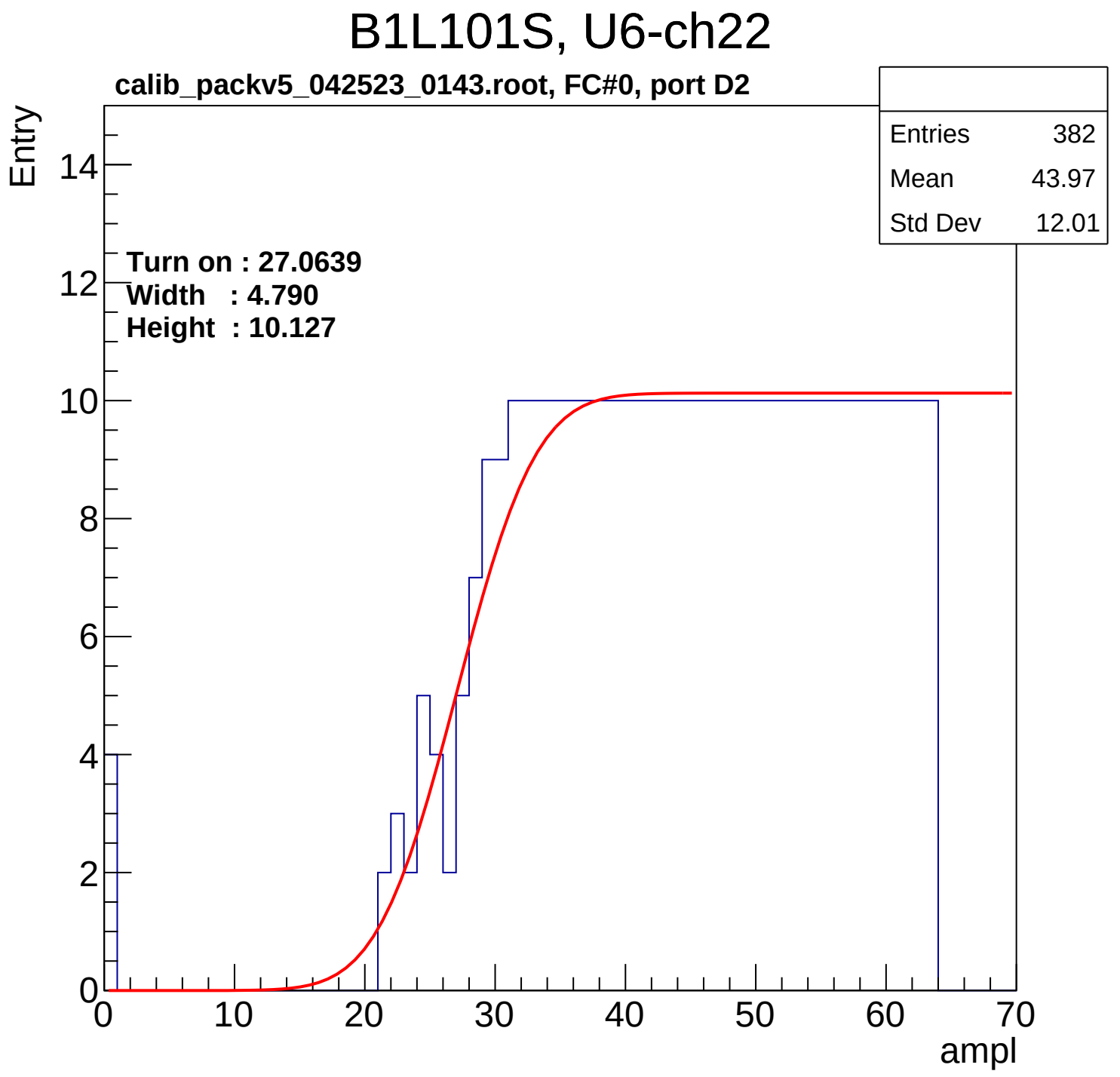

B1L101S, U6-ch17
calib_packv5_042523_0143.root, FC#0, port D2
Entries 364
Mean 45.03
Std Dev 11.14
Turn on : 28.2770
Width : 3.281
Height : 10.065
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

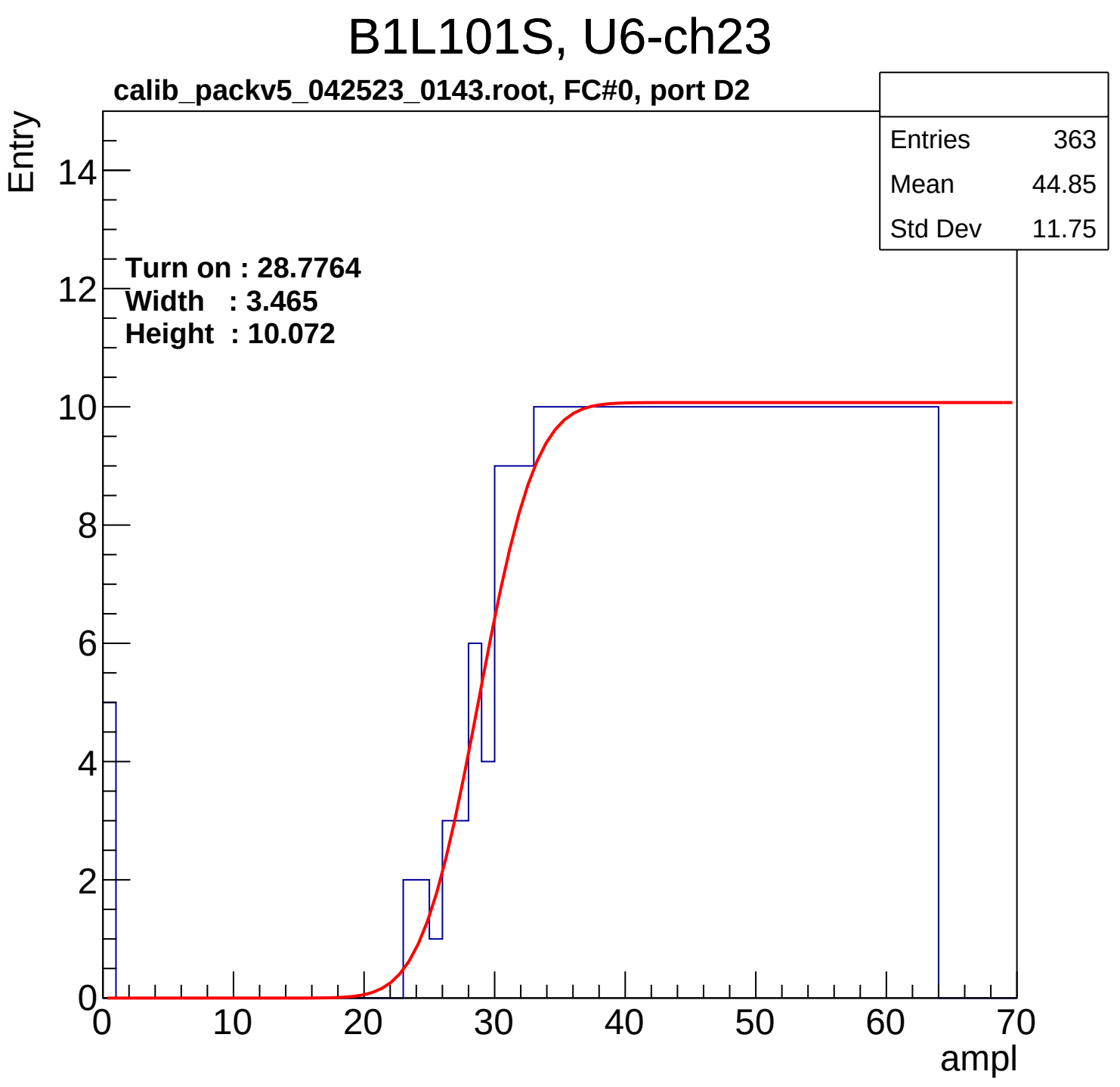

B1L101S, U6-ch18
calib_packv5_042523_0143.root, FC#0, port D2
Entries 367
Mean 44.74
Std Dev 11.6
Turn on : 27.7923
Width : 3.005
Height : 9.995
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

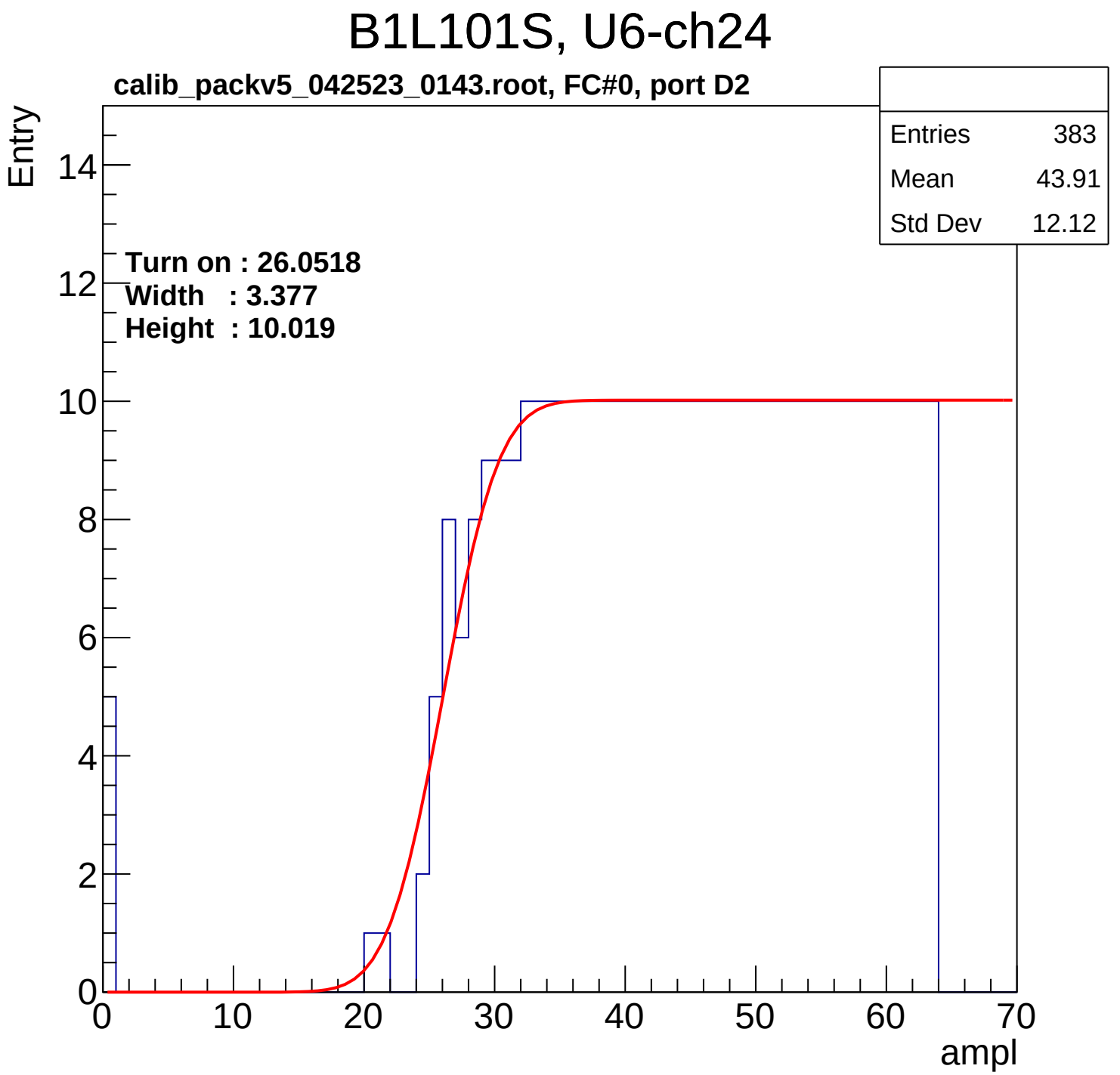

B1L101S, U6-ch19
calib_packv5_042523_0143.root, FC#0, port D2
Entries 361
Mean 45.16
Std Dev 11.09
Turn on : 28.3018
Width : 3.628
Height : 10.033
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

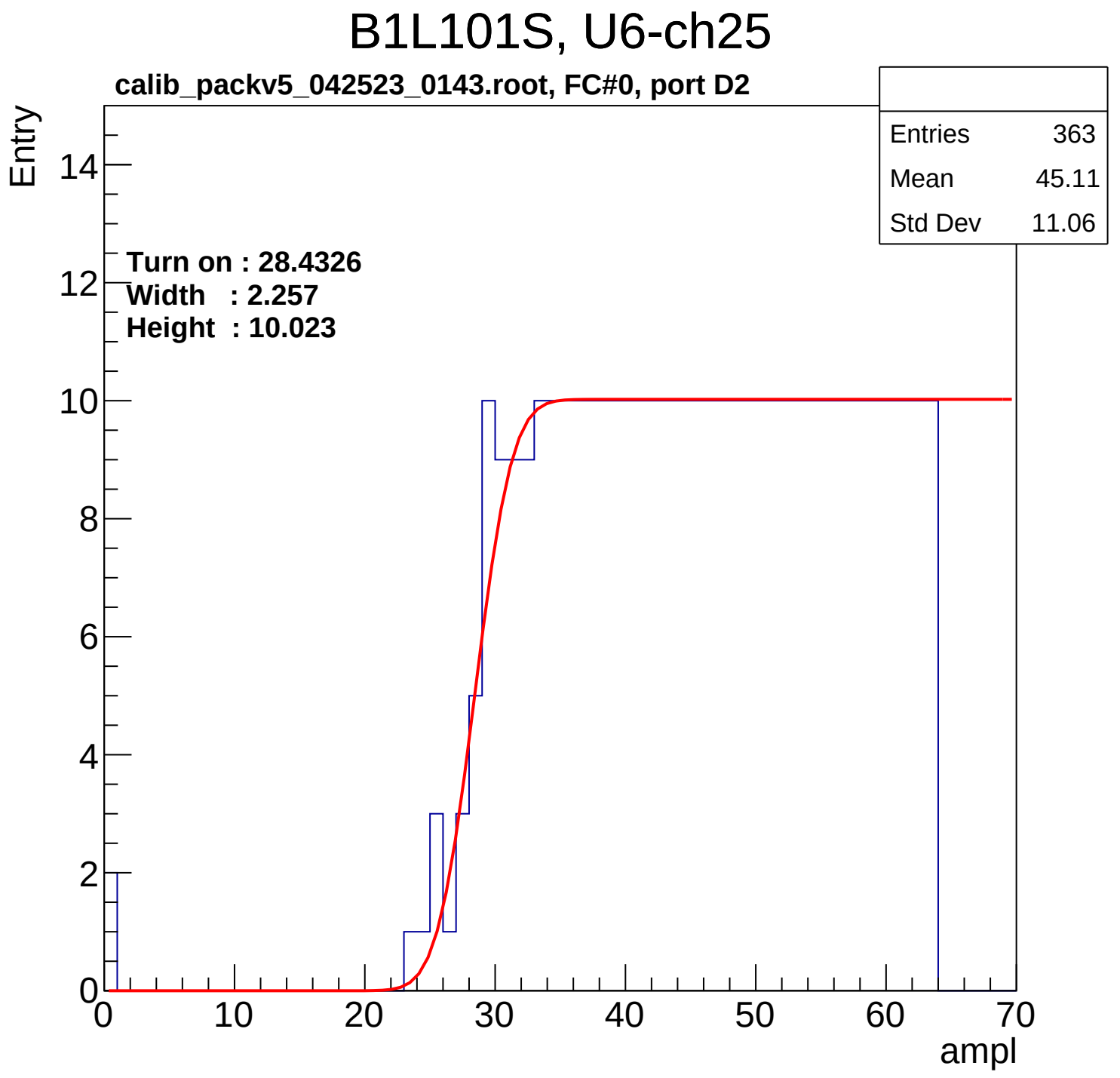

B1L101S, U6-ch20
calib_packv5_042523_0143.root, FC#0, port D2
Entries 359
Mean 45.34
Std Dev 10.91
Turn on : 28.2824
Width : 2.177
Height : 10.008
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

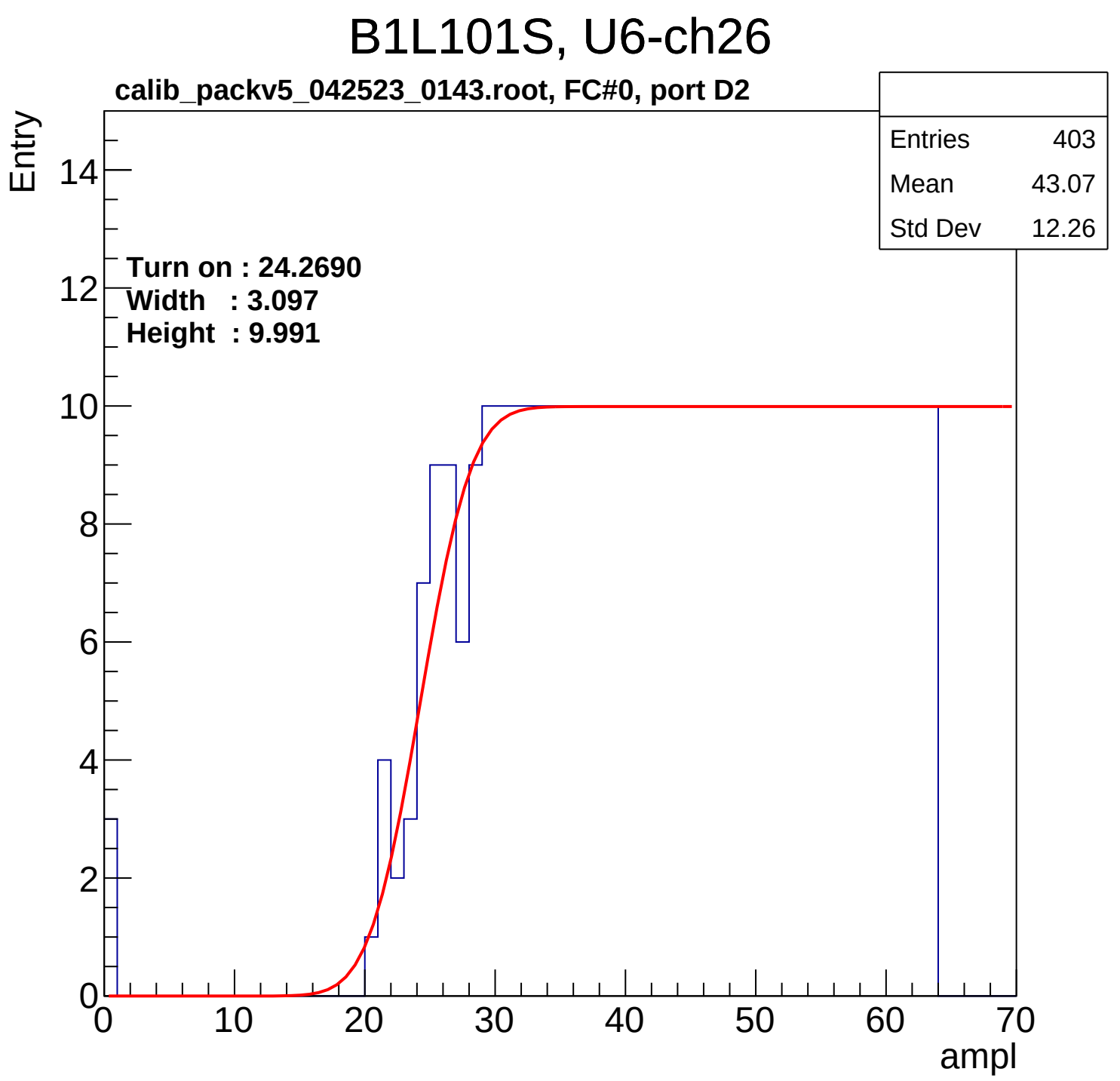

B1L101S, U6-ch21
calib_packv5_042523_0143.root, FC#0, port D2
Entries 376
Mean 44.3
Std Dev 11.81
Turn on : 26.9222
Width : 3.209
Height : 10.006
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

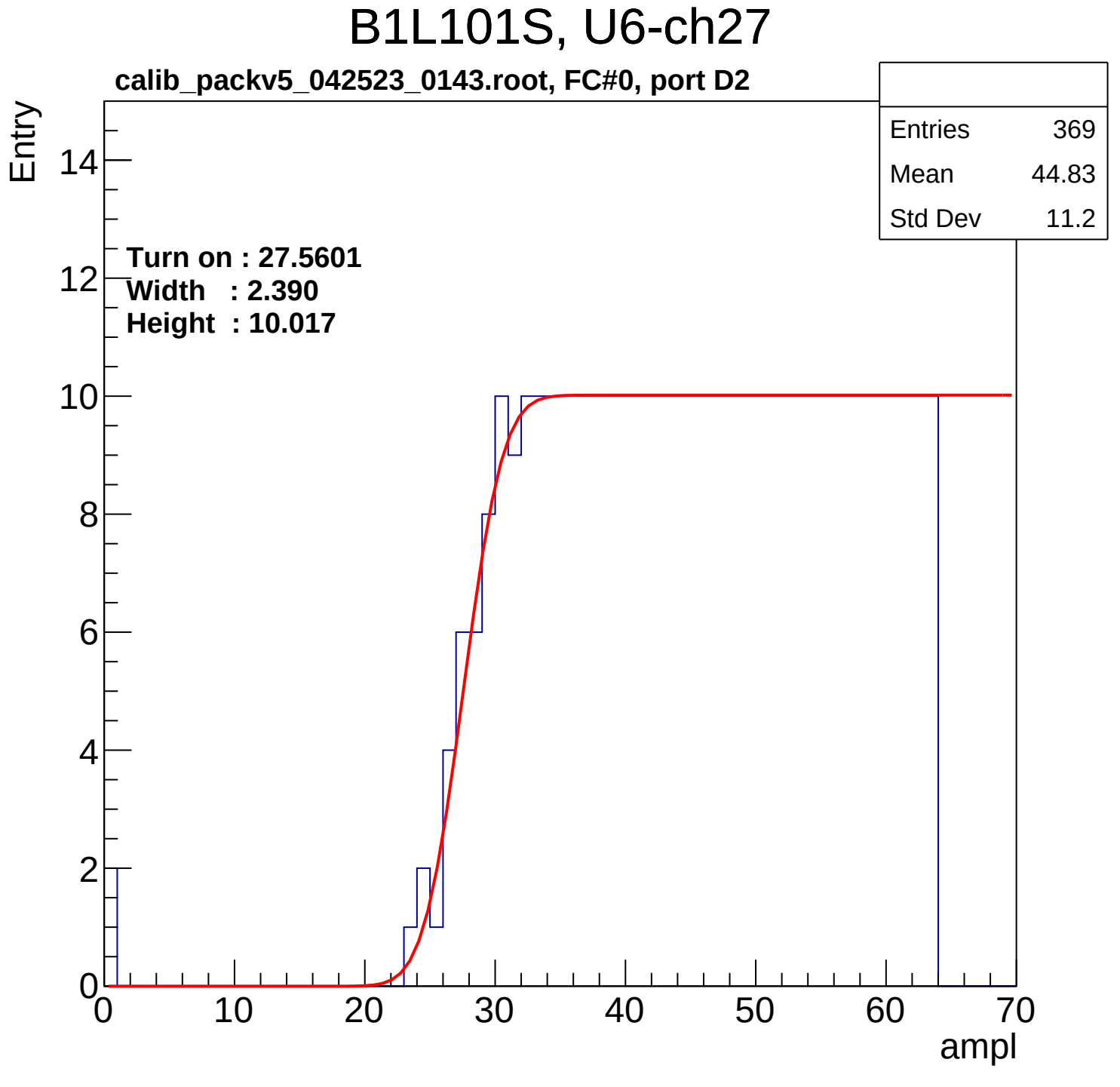

B1L101S, U6-ch22
calib_packv5_042523_0143.root, FC#0, port D2
Entries 382
Mean 43.97
Std Dev 12.01
Turn on : 27.0639
Width : 4.790
Height : 10.127
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

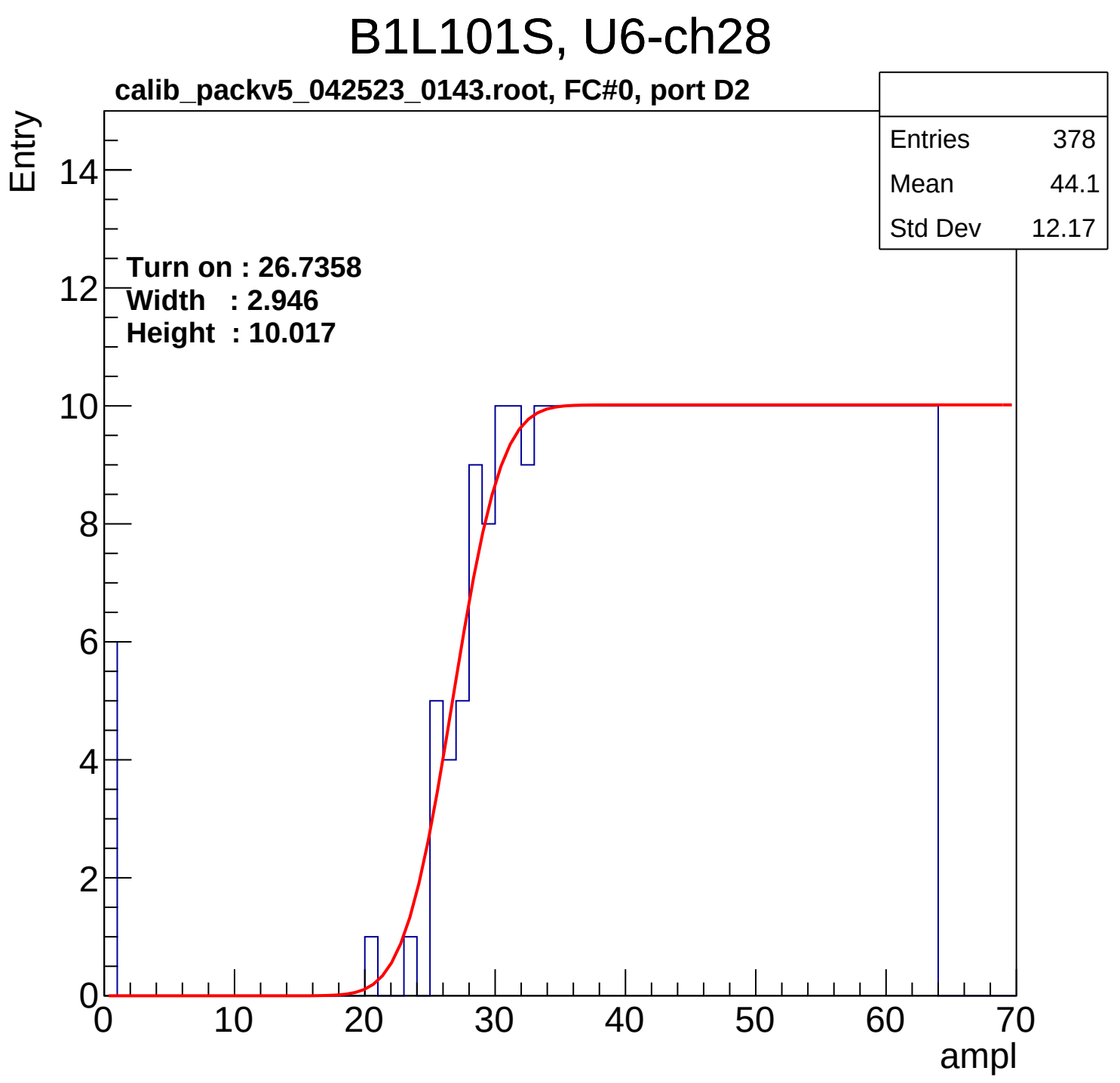

B1L101S, U6-ch23
calib_packv5_042523_0143.root, FC#0, port D2
Entries 363
Mean 44.85
Std Dev 11.75
Turn on : 28.7764
Width : 3.465
Height : 10.072
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

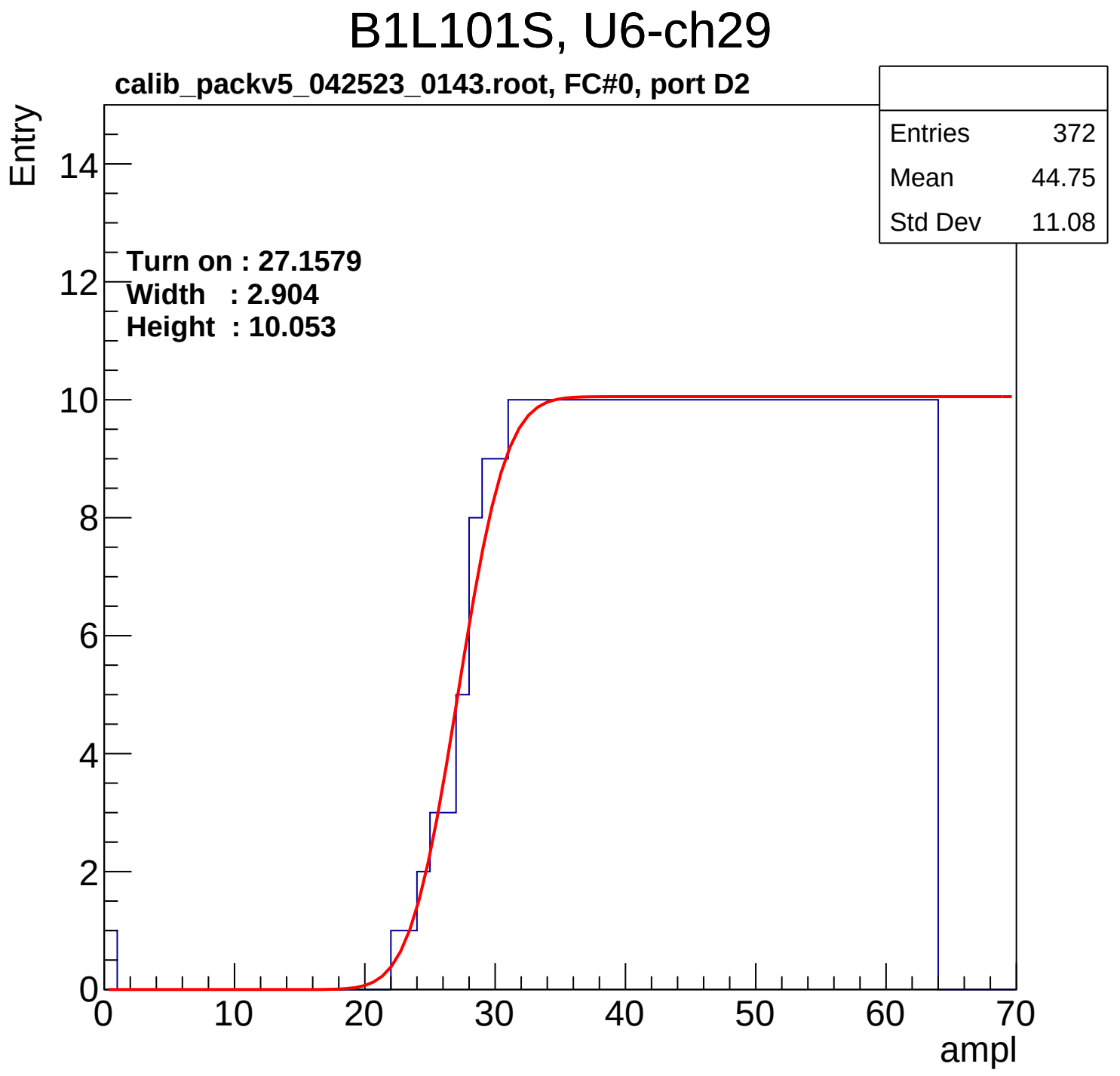

B1L101S, U6-ch24
calib_packv5_042523_0143.root, FC#0, port D2
Entries 383
Mean 43.91
Std Dev 12.12
Turn on : 26.0518
Width : 3.377
Height : 10.019
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

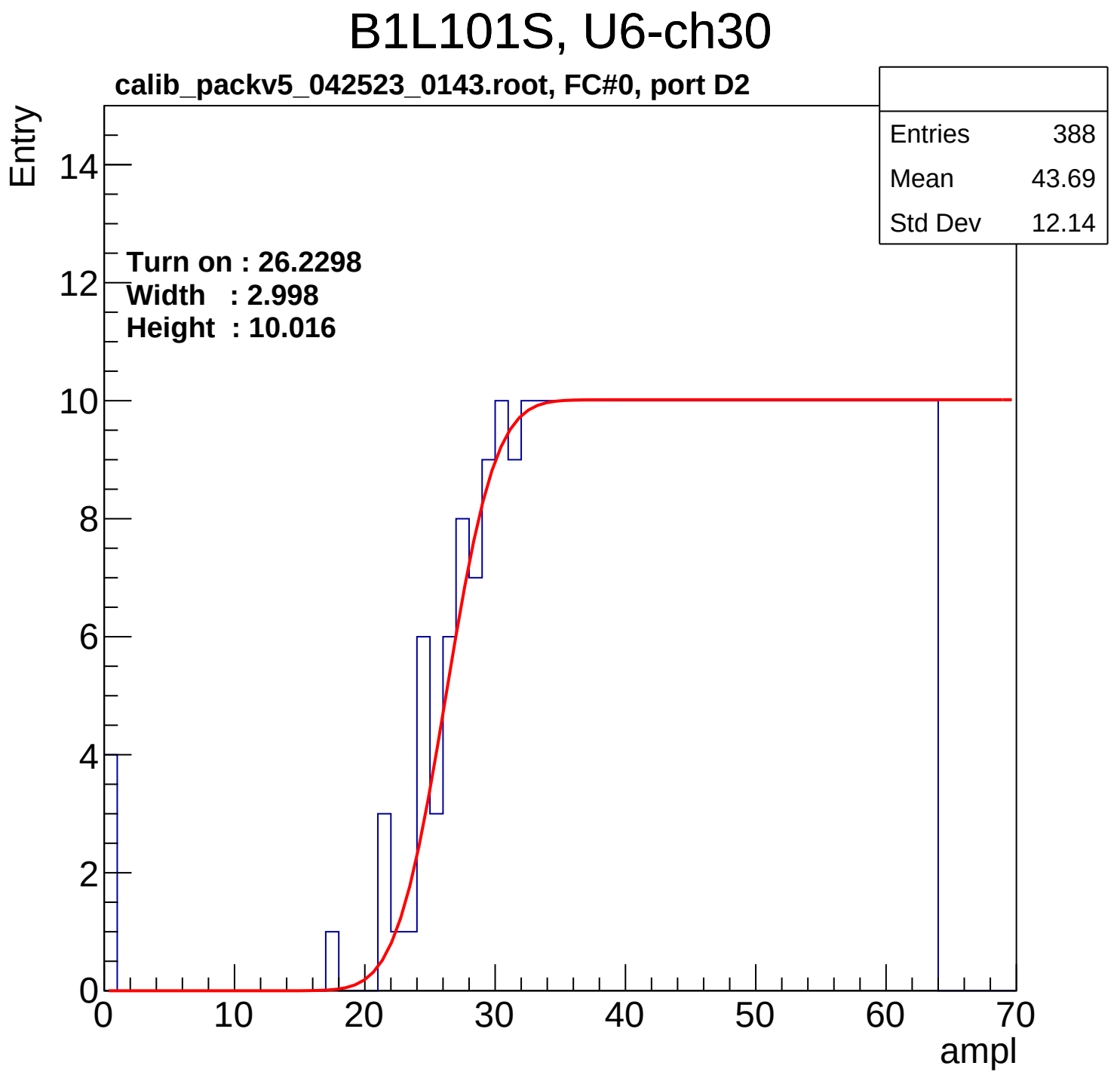

B1L101S, U6-ch25
calib_packv5_042523_0143.root, FC#0, port D2
Entries 363
Mean 45.11
Std Dev 11.06
Turn on : 28.4326
Width : 2.257
Height : 10.023
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

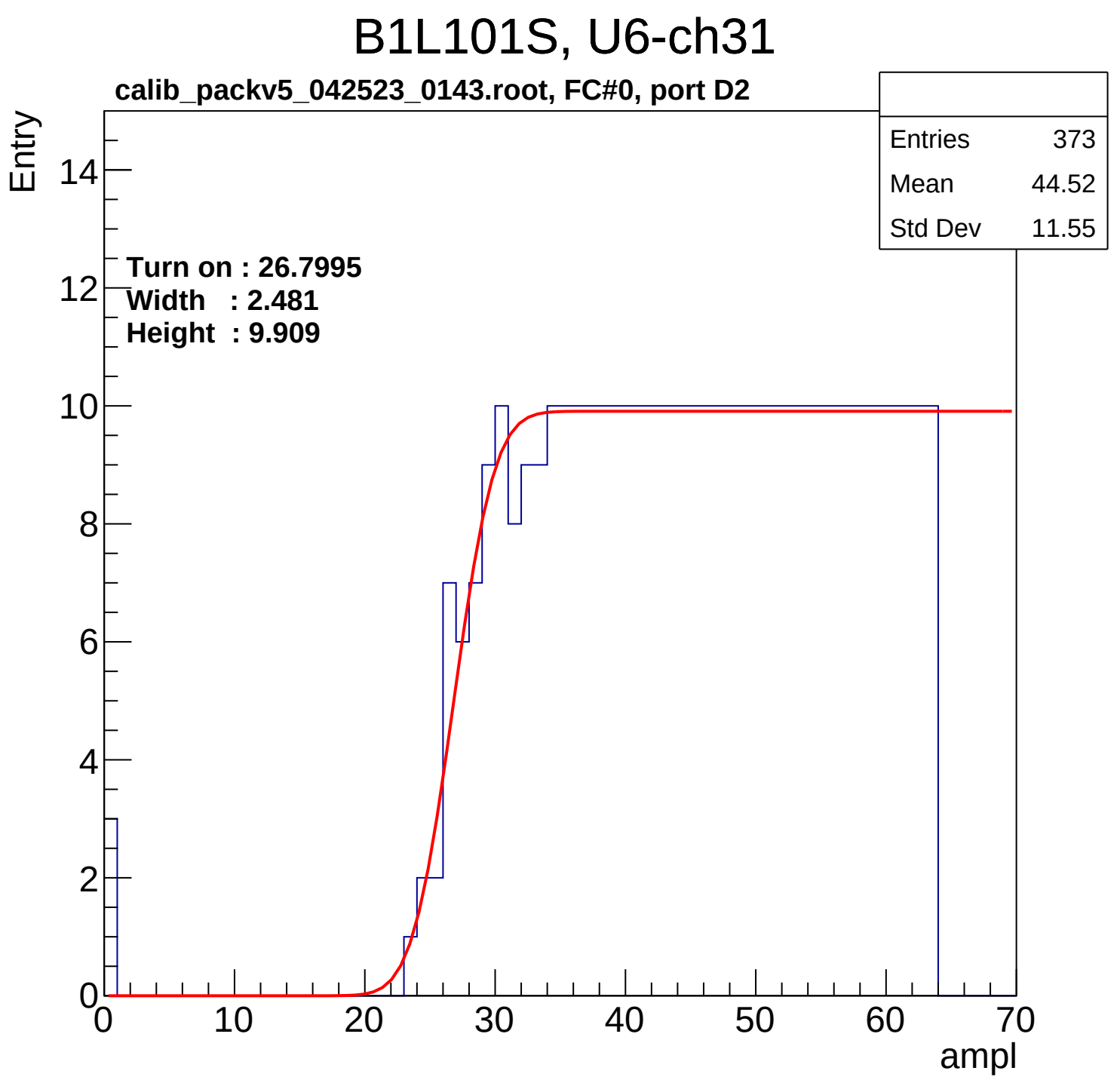

B1L101S, U6-ch26
calib_packv5_042523_0143.root, FC#0, port D2
Entries 403
Mean 43.07
Std Dev 12.26
Turn on : 24.2690
Width : 3.097
Height : 9.991
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

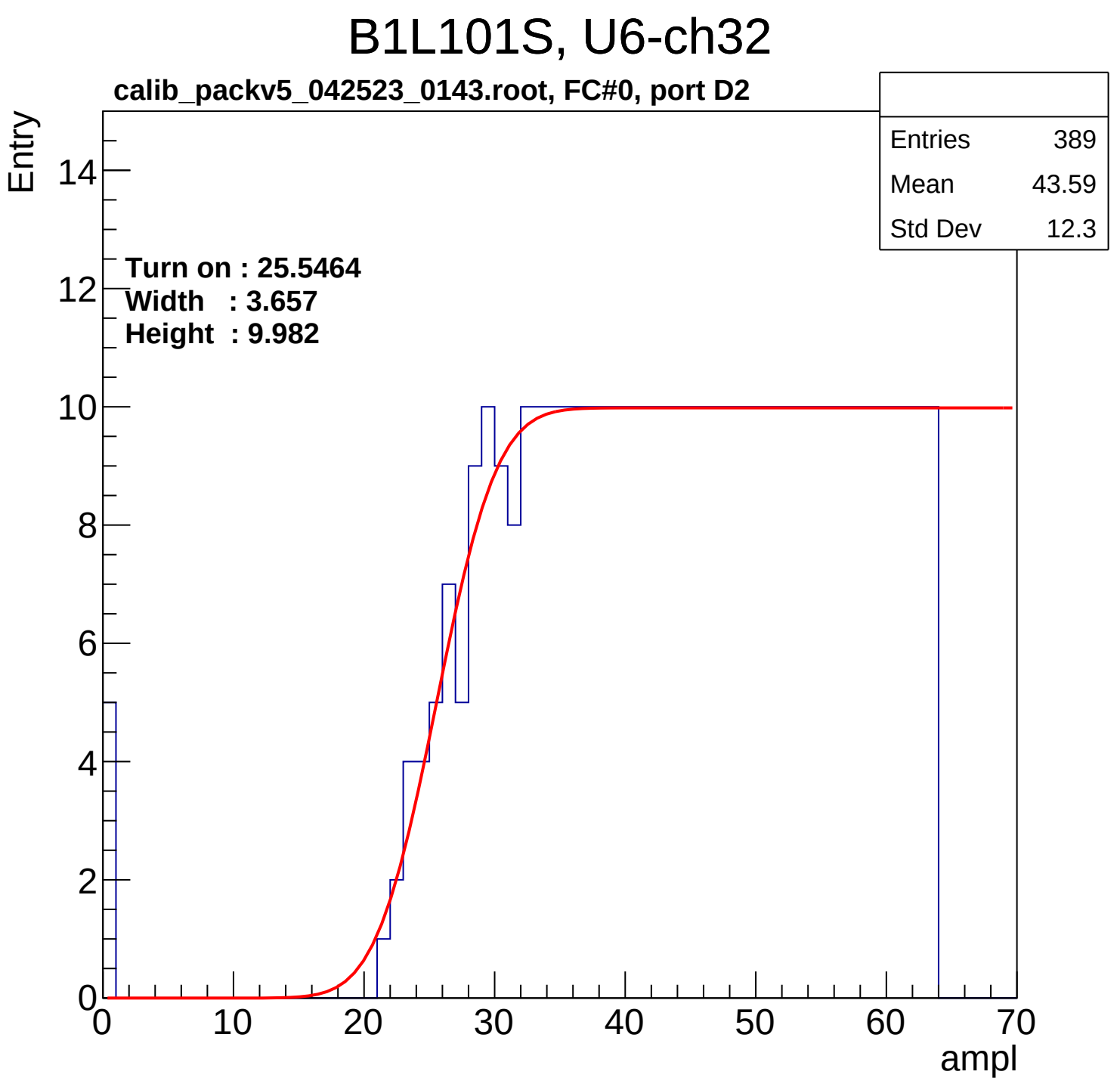

B1L101S, U6-ch27
calib_packv5_042523_0143.root, FC#0, port D2
Entries 369
Mean 44.83
Std Dev 11.2
Turn on : 27.5601
Width : 2.390
Height : 10.017
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

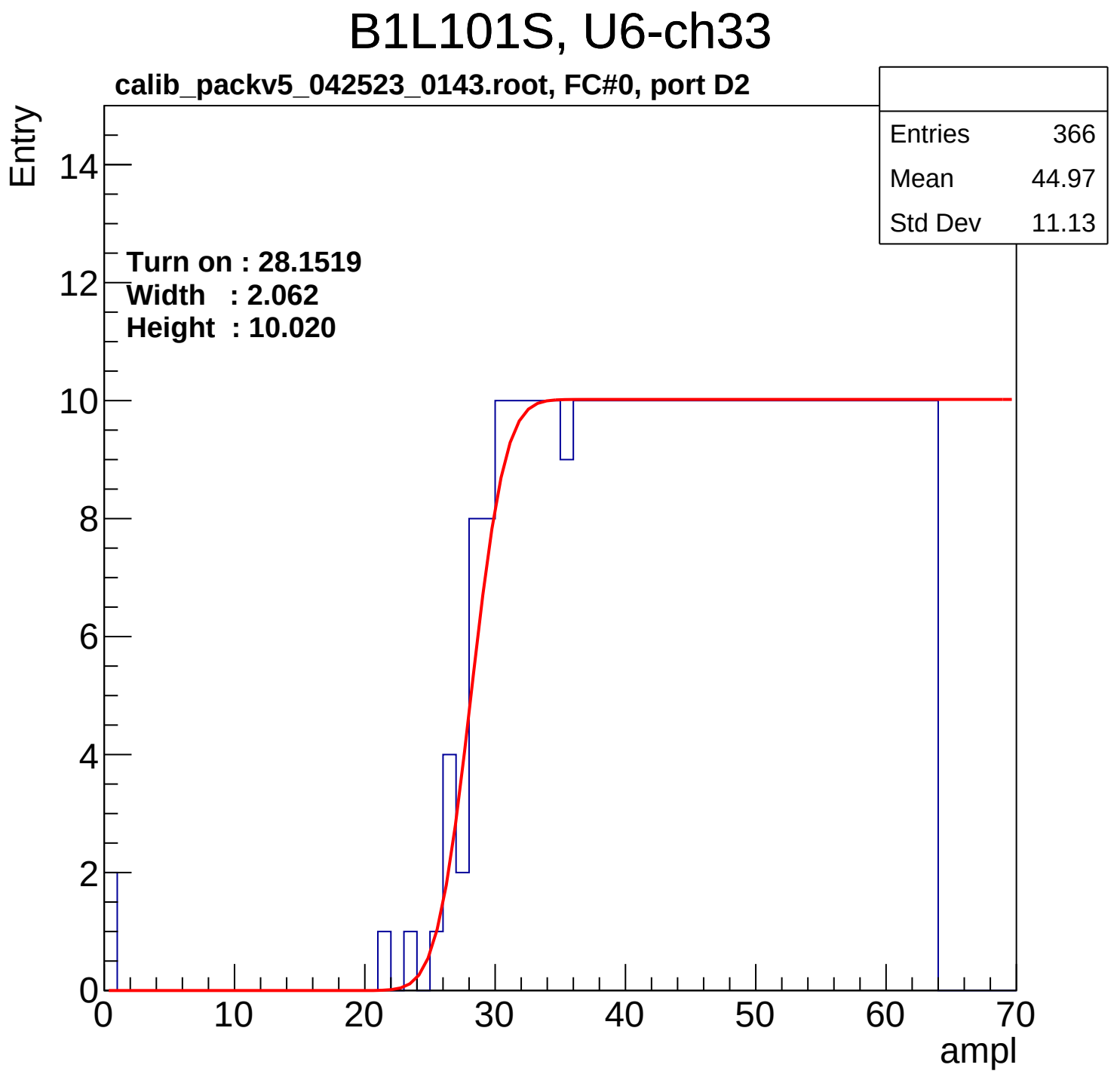

B1L101S, U6-ch28
calib_packv5_042523_0143.root, FC#0, port D2
Entries 378
Mean 44.1
Std Dev 12.17
Turn on : 26.7358
Width : 2.946
Height : 10.017
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

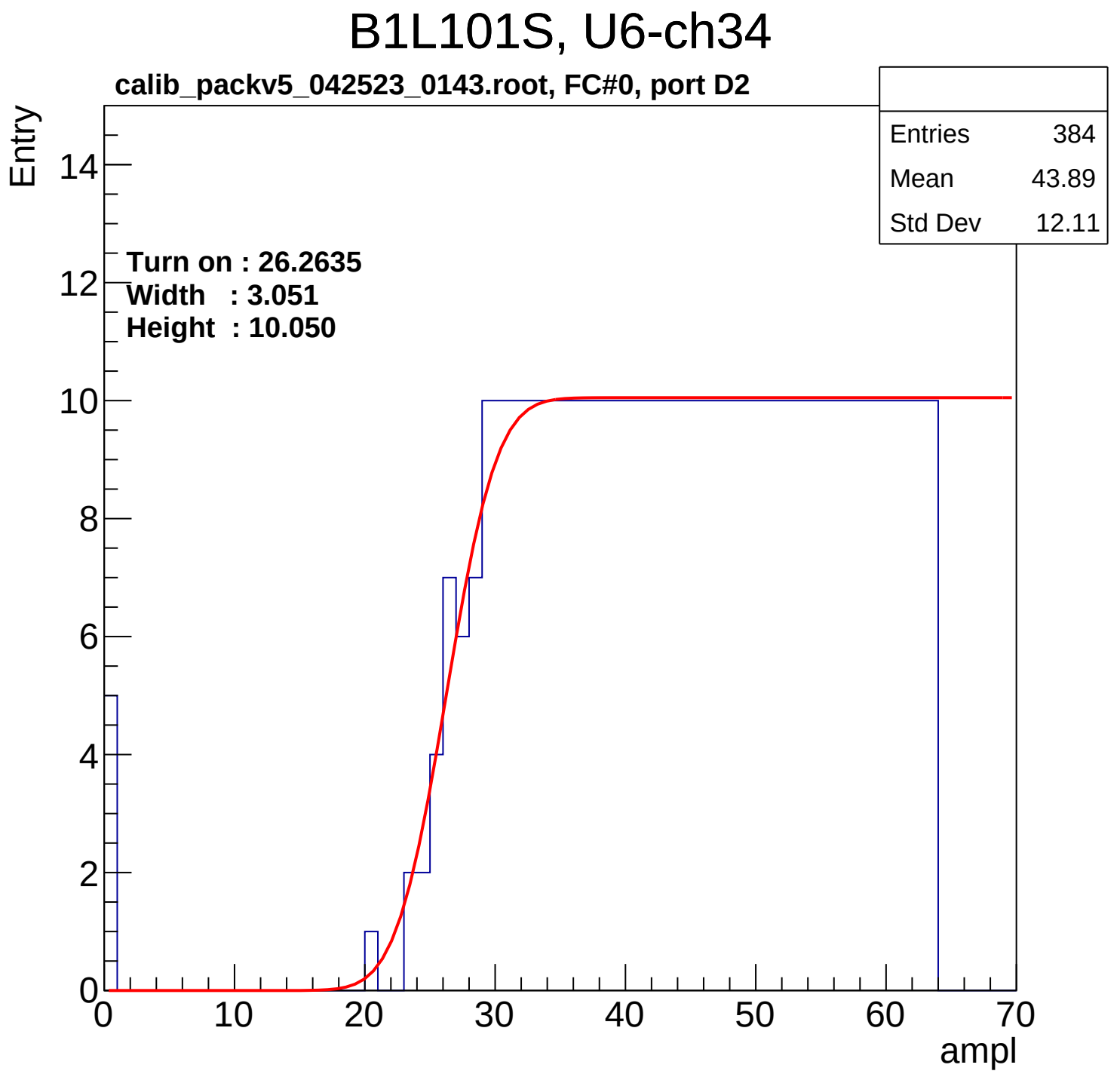

B1L101S, U6-ch29
calib_packv5_042523_0143.root, FC#0, port D2
Entries 372
Mean 44.75
Std Dev 11.08
Turn on : 27.1579
Width : 2.904
Height : 10.053
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

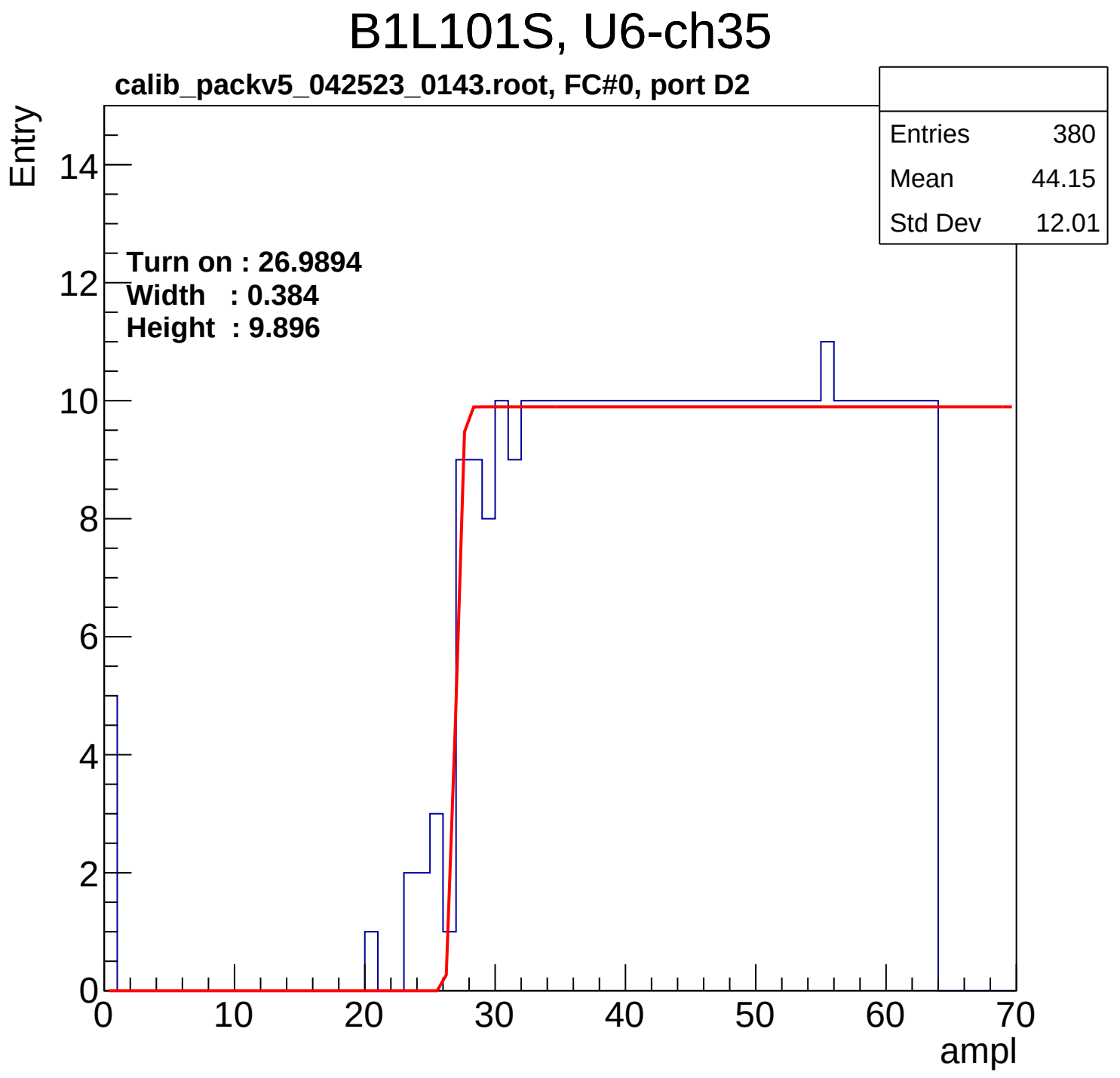

B1L101S, U6-ch30
calib_packv5_042523_0143.root, FC#0, port D2
Entries 388
Mean 43.69
Std Dev 12.14
Turn on : 26.2298
Width : 2.998
Height : 10.016
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

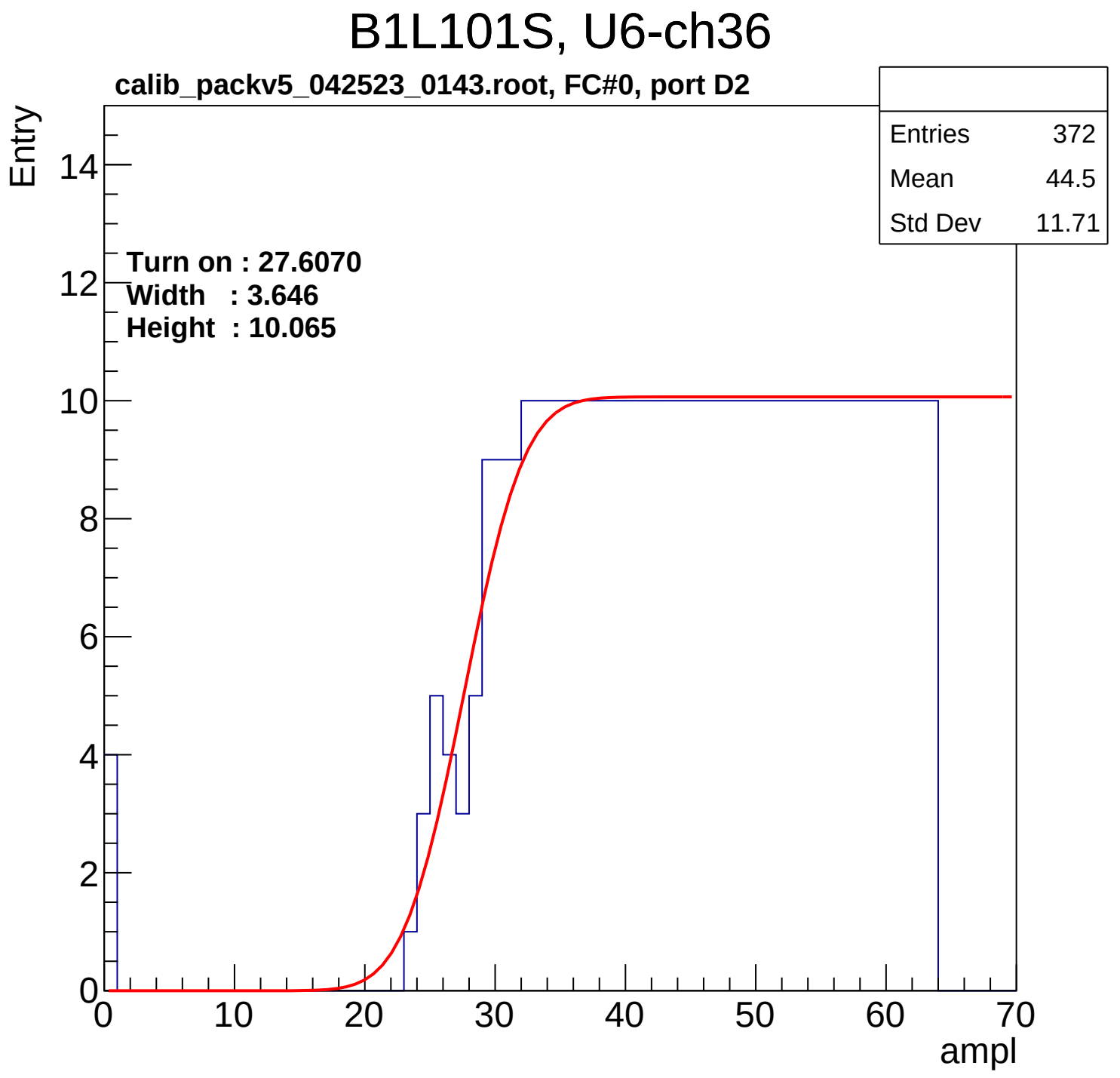

B1L101S, U6-ch31
calib_packv5_042523_0143.root, FC#0, port D2
Entries 373
Mean 44.52
Std Dev 11.55
Turn on : 26.7995
Width : 2.481
Height : 9.909
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

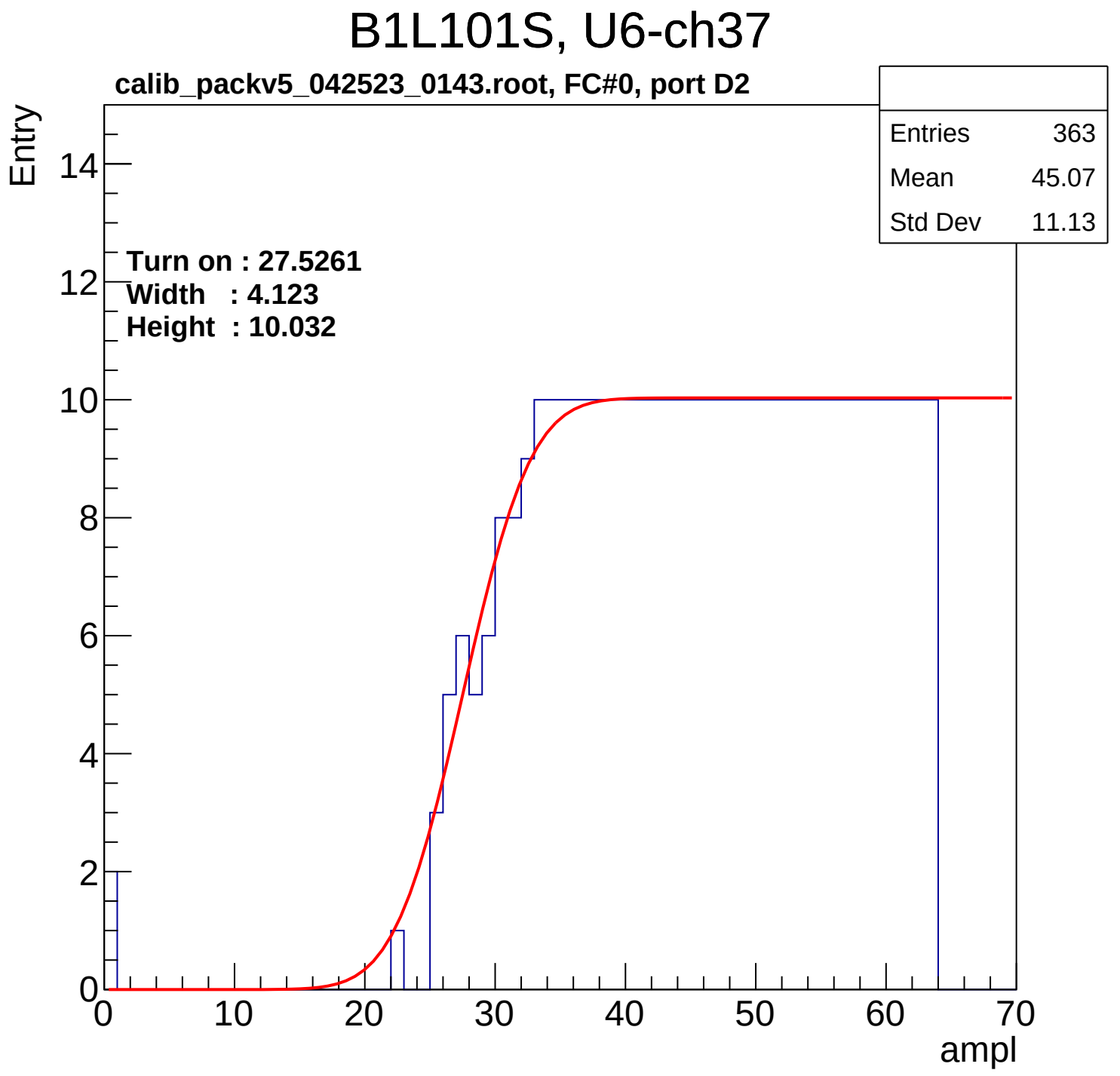

B1L101S, U6-ch32
calib_packv5_042523_0143.root, FC#0, port D2
Entries 389
Mean 43.59
Std Dev 12.3
Turn on : 25.5464
Width : 3.657
Height : 9.982
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

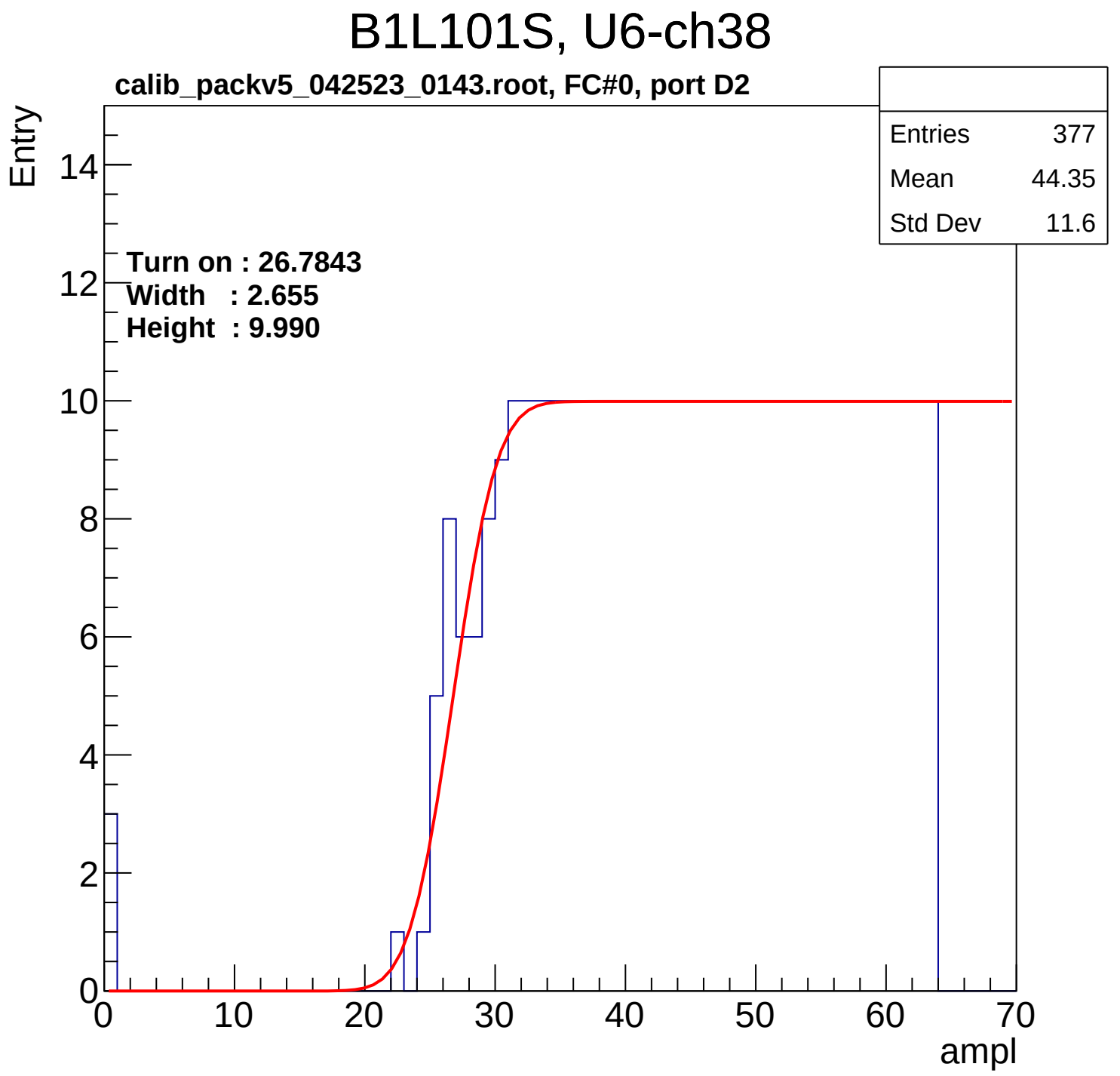

B1L101S, U6-ch33
calib_packv5_042523_0143.root, FC#0, port D2
Entries 366
Mean 44.97
Std Dev 11.13
Turn on : 28.1519
Width : 2.062
Height : 10.020
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

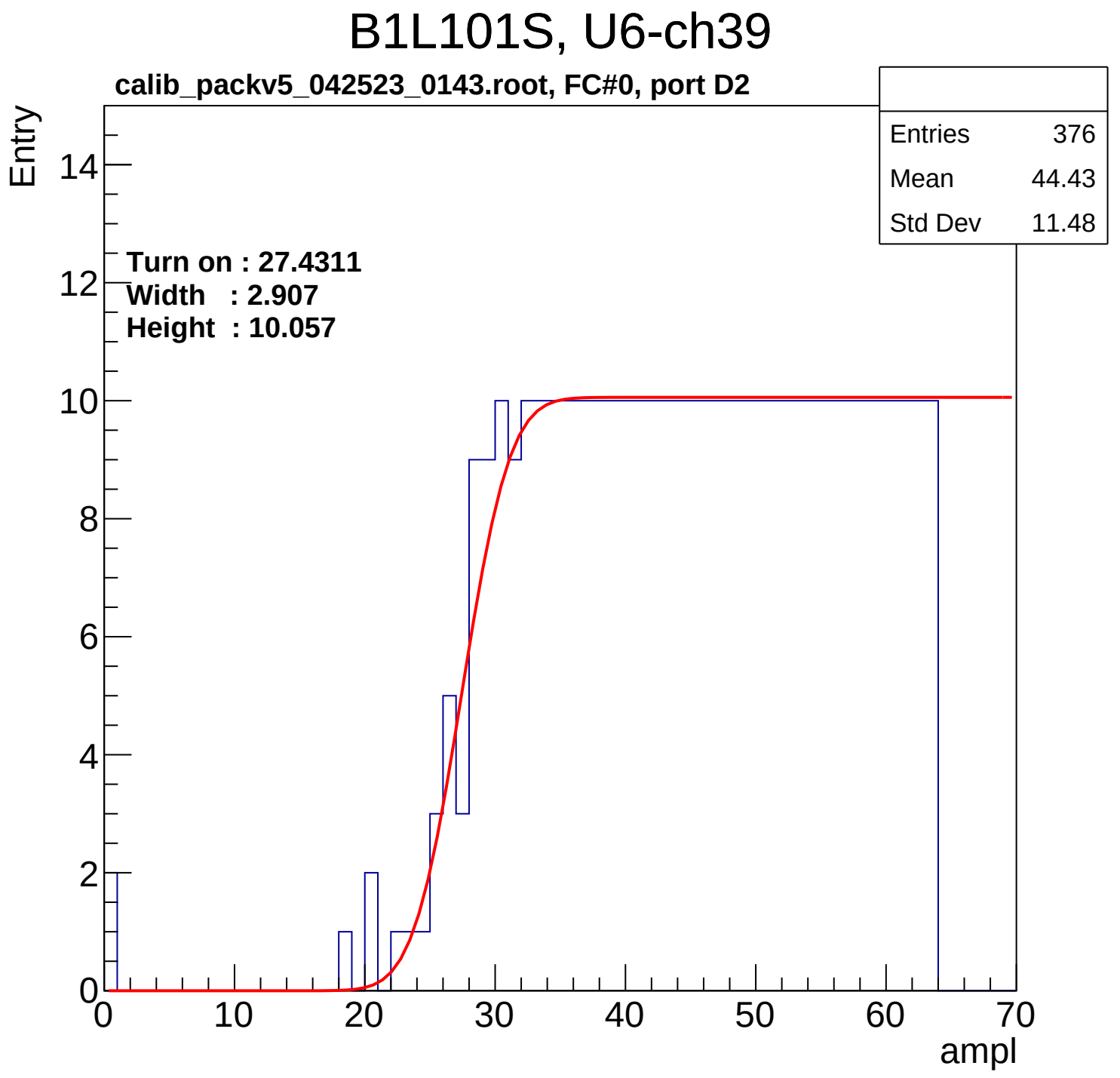

B1L101S, U6-ch34
calib_packv5_042523_0143.root, FC#0, port D2
Entries 384
Mean 43.89
Std Dev 12.11
Turn on : 26.2635
Width : 3.051
Height : 10.050
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

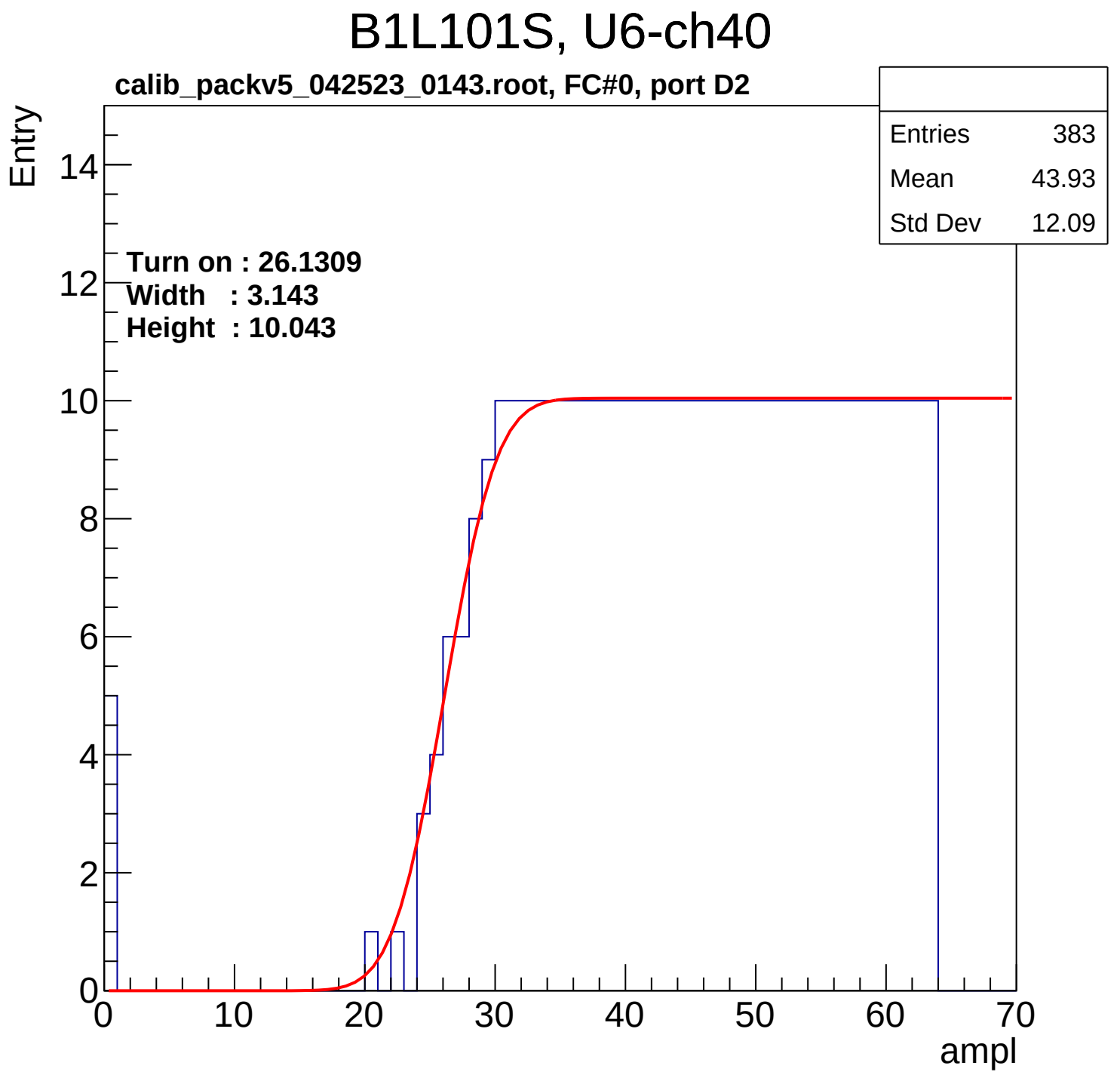

B1L101S, U6-ch35
calib_packv5_042523_0143.root, FC#0, port D2
Entries 380
Mean 44.15
Std Dev 12.01
Turn on : 26.9894
Width : 0.384
Height : 9.896
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

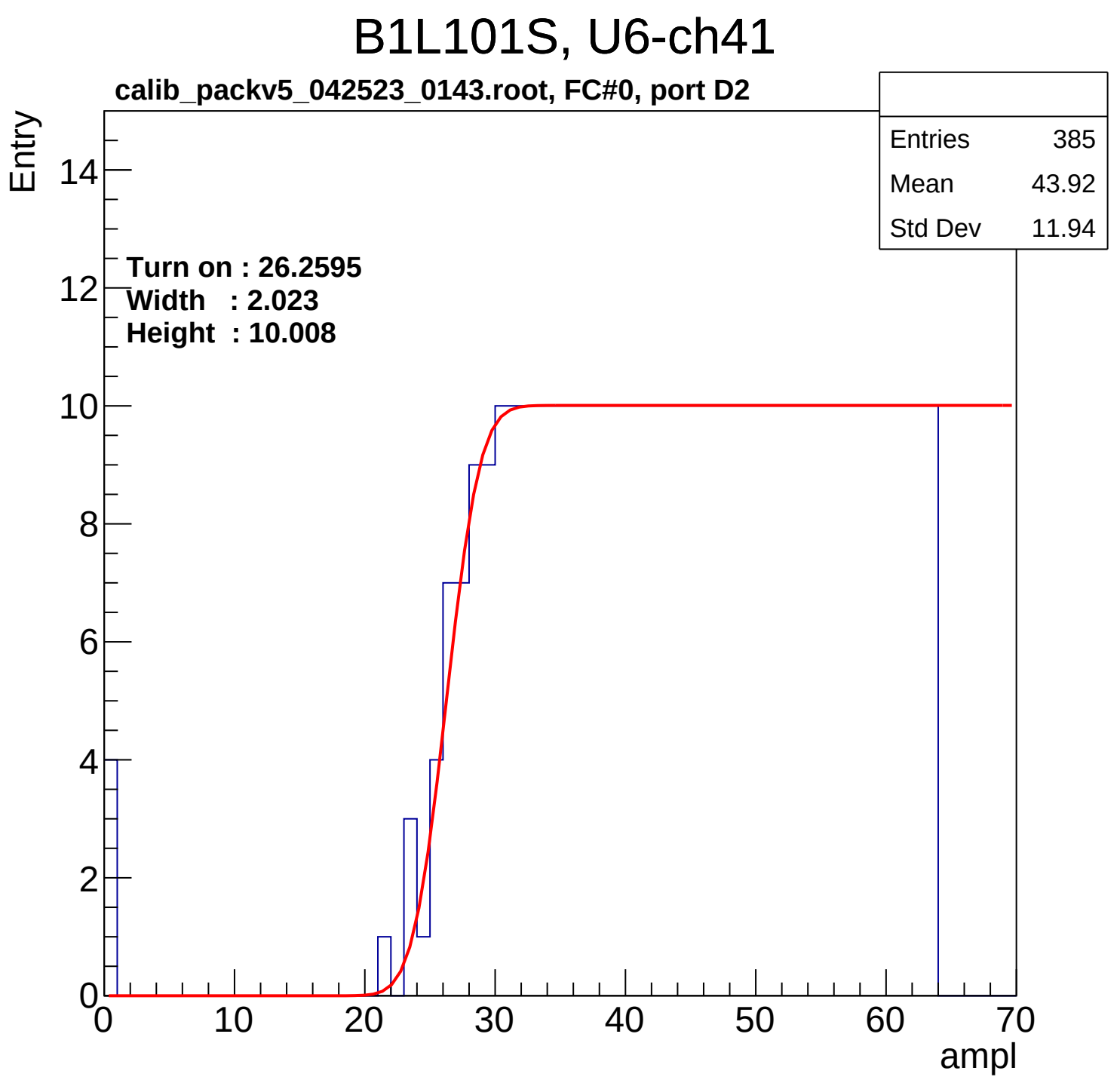

B1L101S, U6-ch36
calib_packv5_042523_0143.root, FC#0, port D2
Entries 372
Mean 44.5
Std Dev 11.71
Turn on : 27.6070
Width : 3.646
Height : 10.065
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

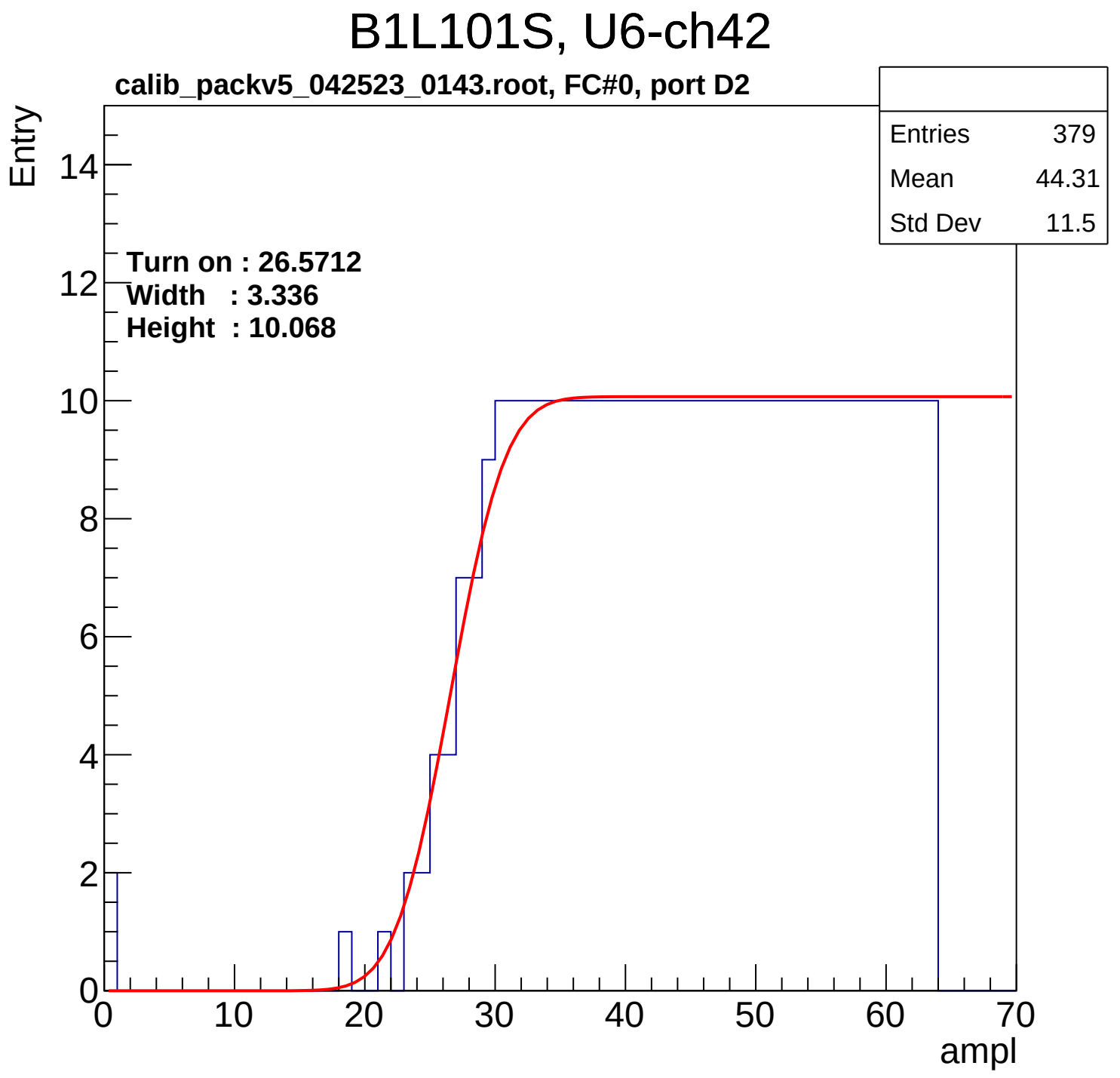

B1L101S, U6-ch37
calib_packv5_042523_0143.root, FC#0, port D2
Entries 363
Mean 45.07
Std Dev 11.13
Turn on : 27.5261
Width : 4.123
Height : 10.032
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

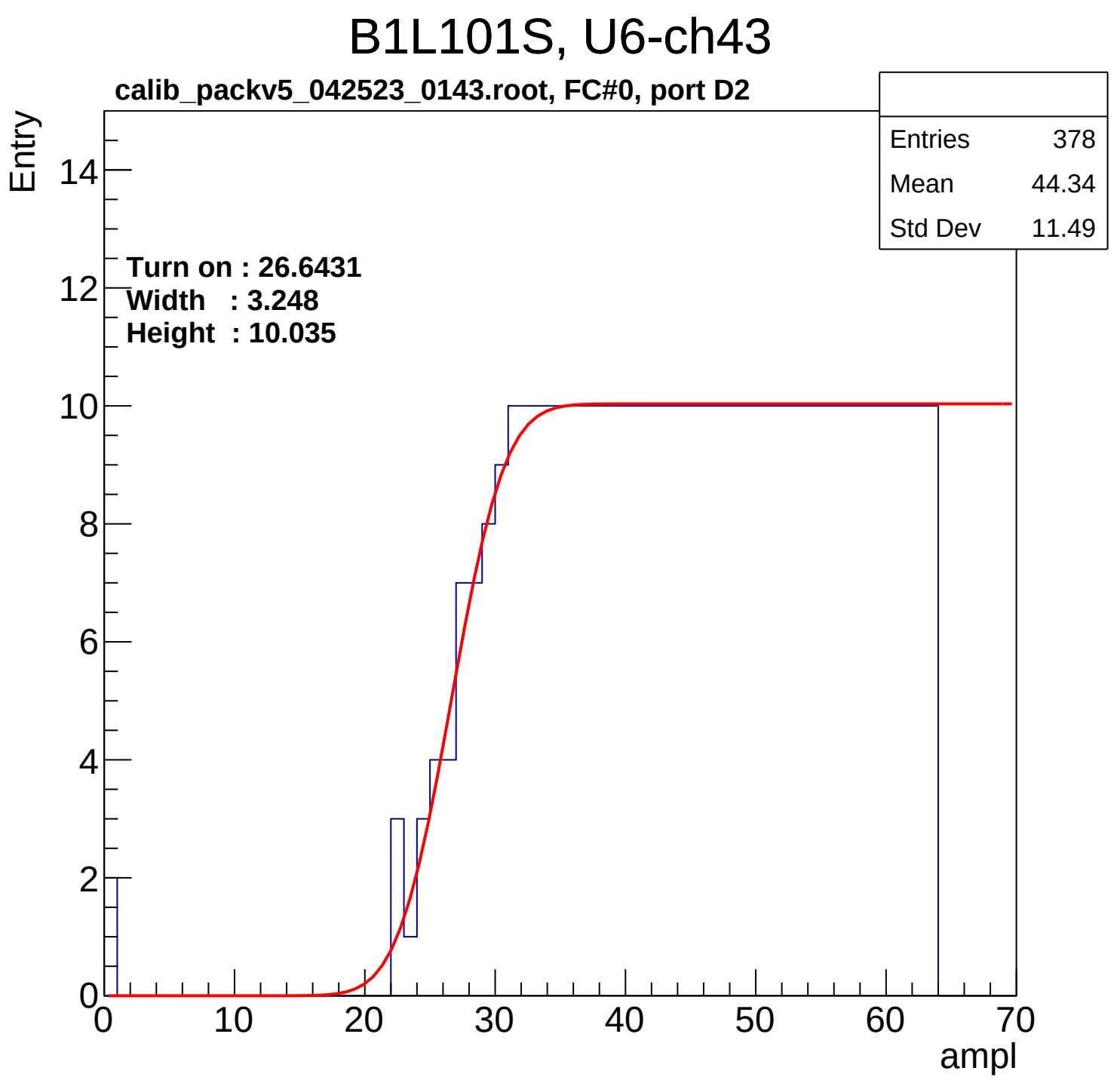

B1L101S, U6-ch38
calib_packv5_042523_0143.root, FC#0, port D2
Entries 377
Mean 44.35
Std Dev 11.6
Turn on : 26.7843
Width : 2.655
Height : 9.990
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

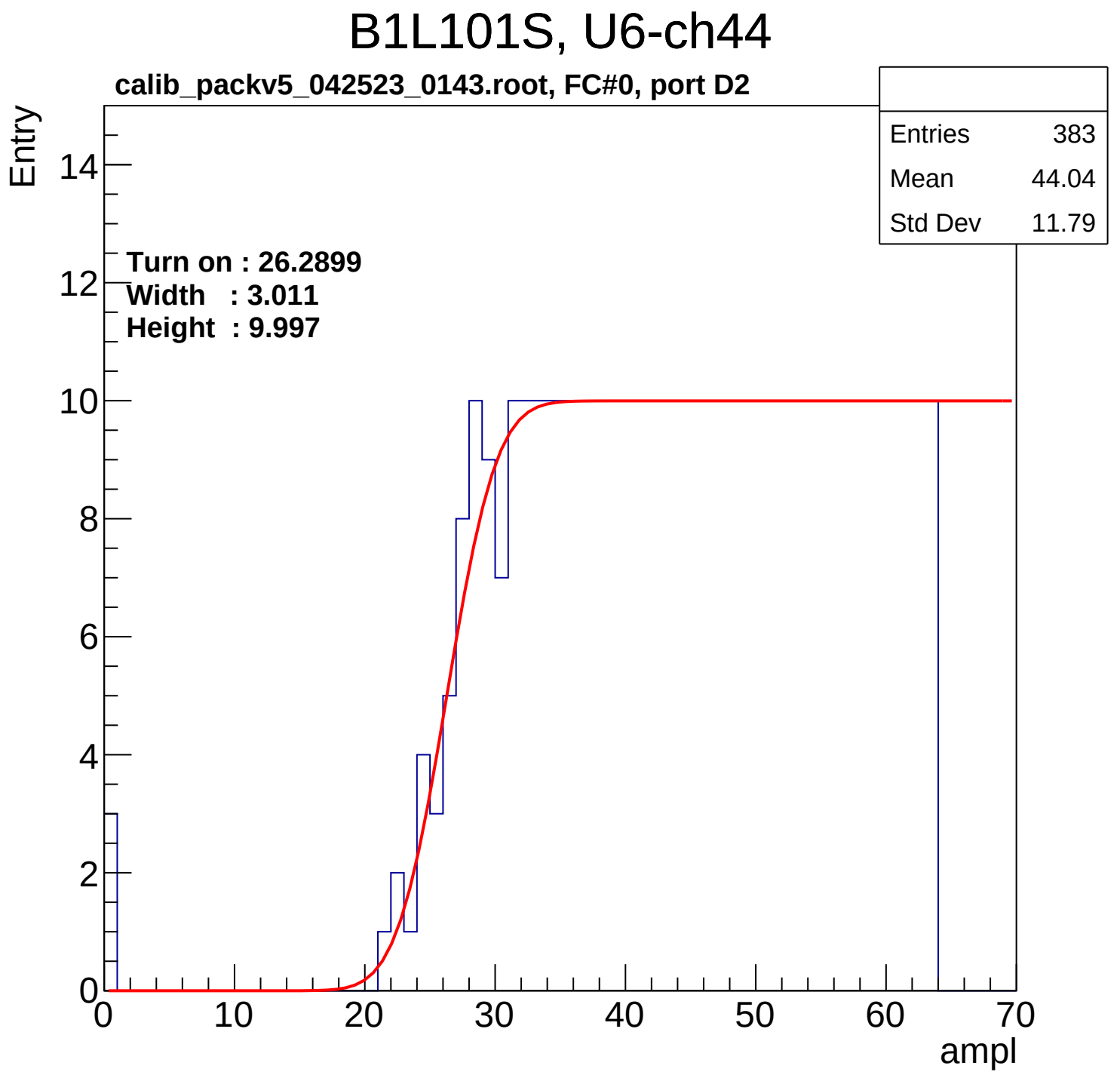

B1L101S, U6-ch39
calib_packv5_042523_0143.root, FC#0, port D2
Entries 376
Mean 44.43
Std Dev 11.48
Turn on : 27.4311
Width : 2.907
Height : 10.057
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

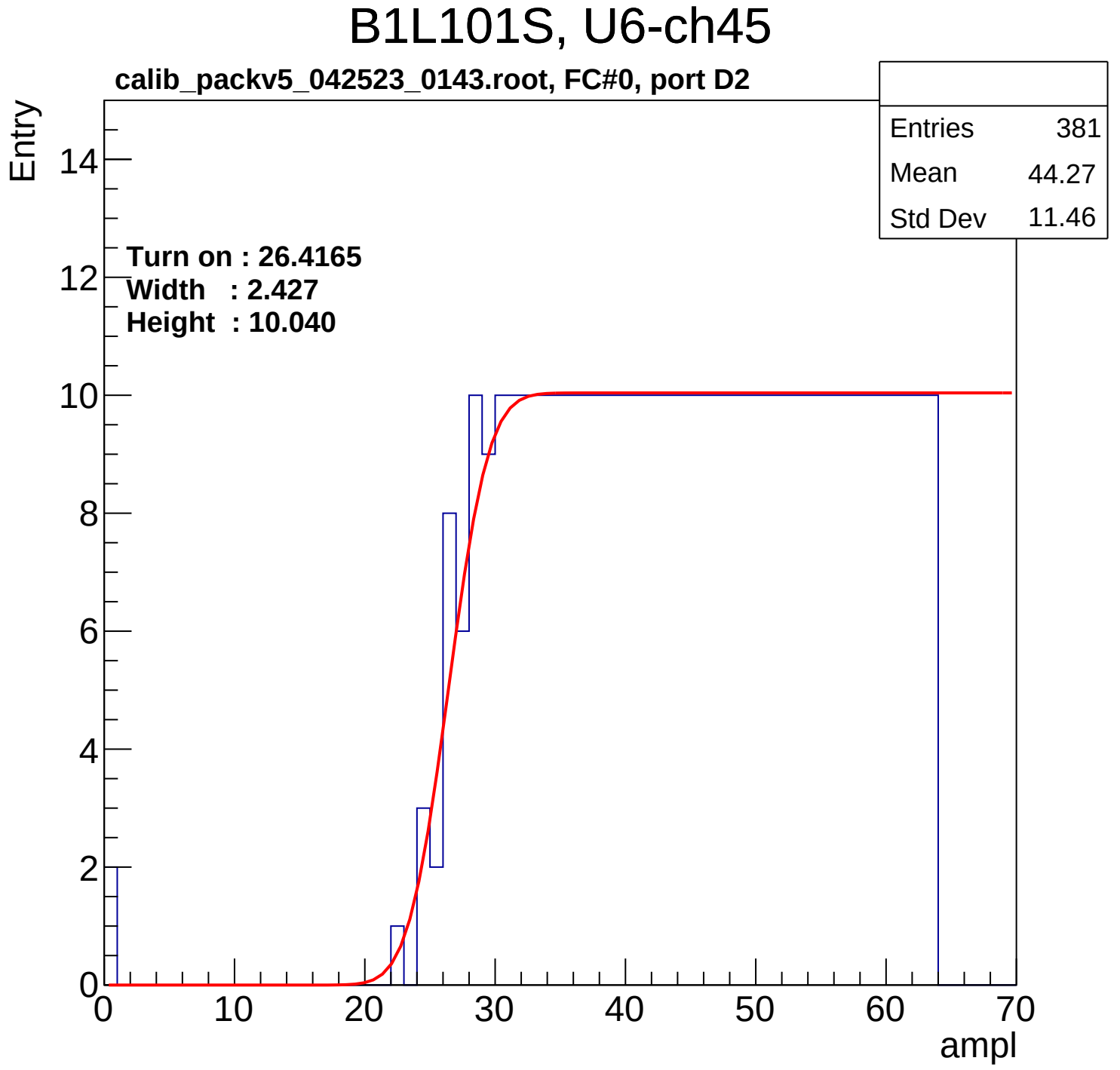

B1L101S, U6-ch40
calib_packv5_042523_0143.root, FC#0, port D2
Entries 383
Mean 43.93
Std Dev 12.09
Turn on : 26.1309
Width : 3.143
Height : 10.043
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

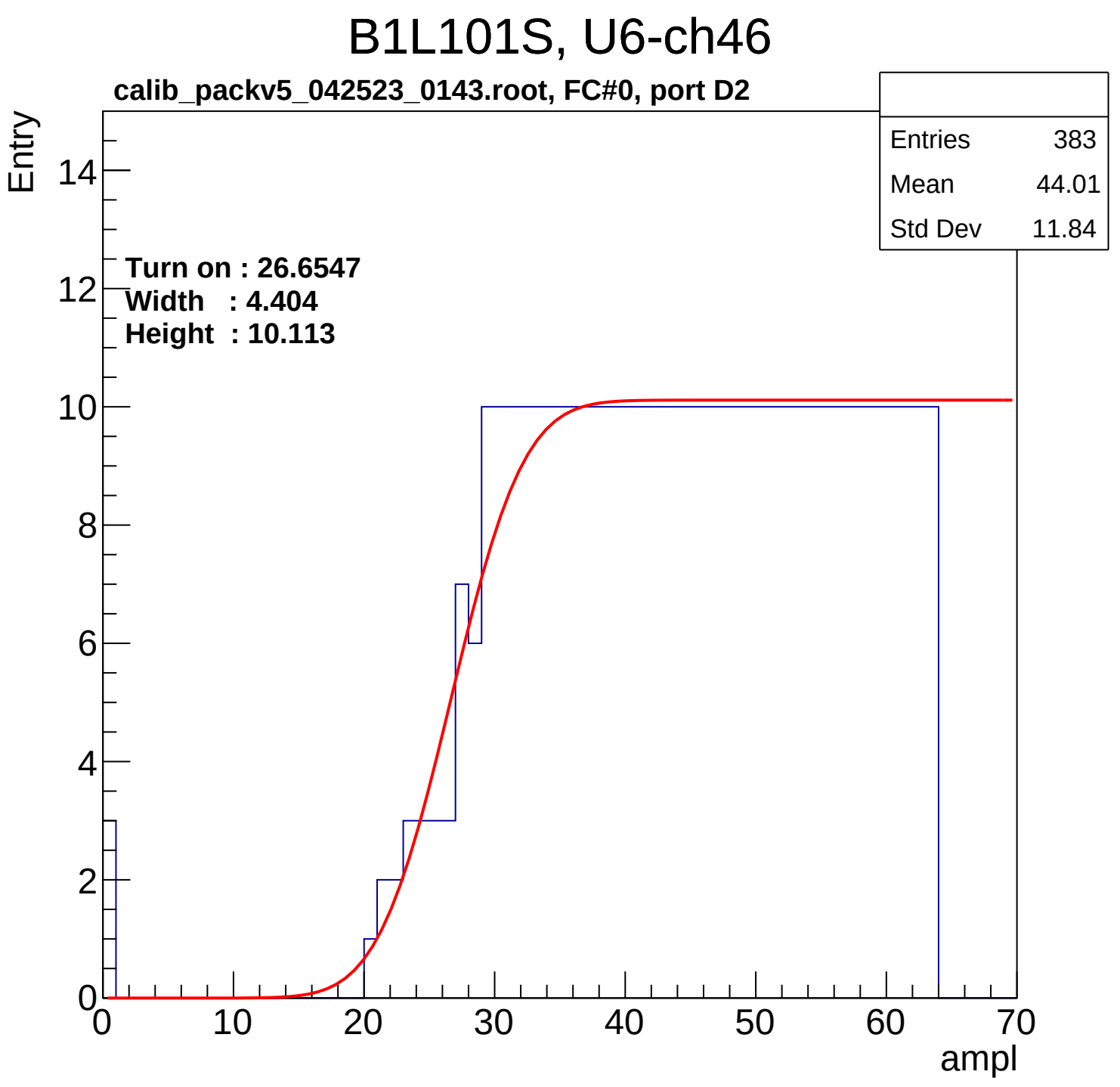

B1L101S, U6-ch41
calib_packv5_042523_0143.root, FC#0, port D2
Entries 385
Mean 43.92
Std Dev 11.94
Turn on : 26.2595
Width : 2.023
Height : 10.008
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

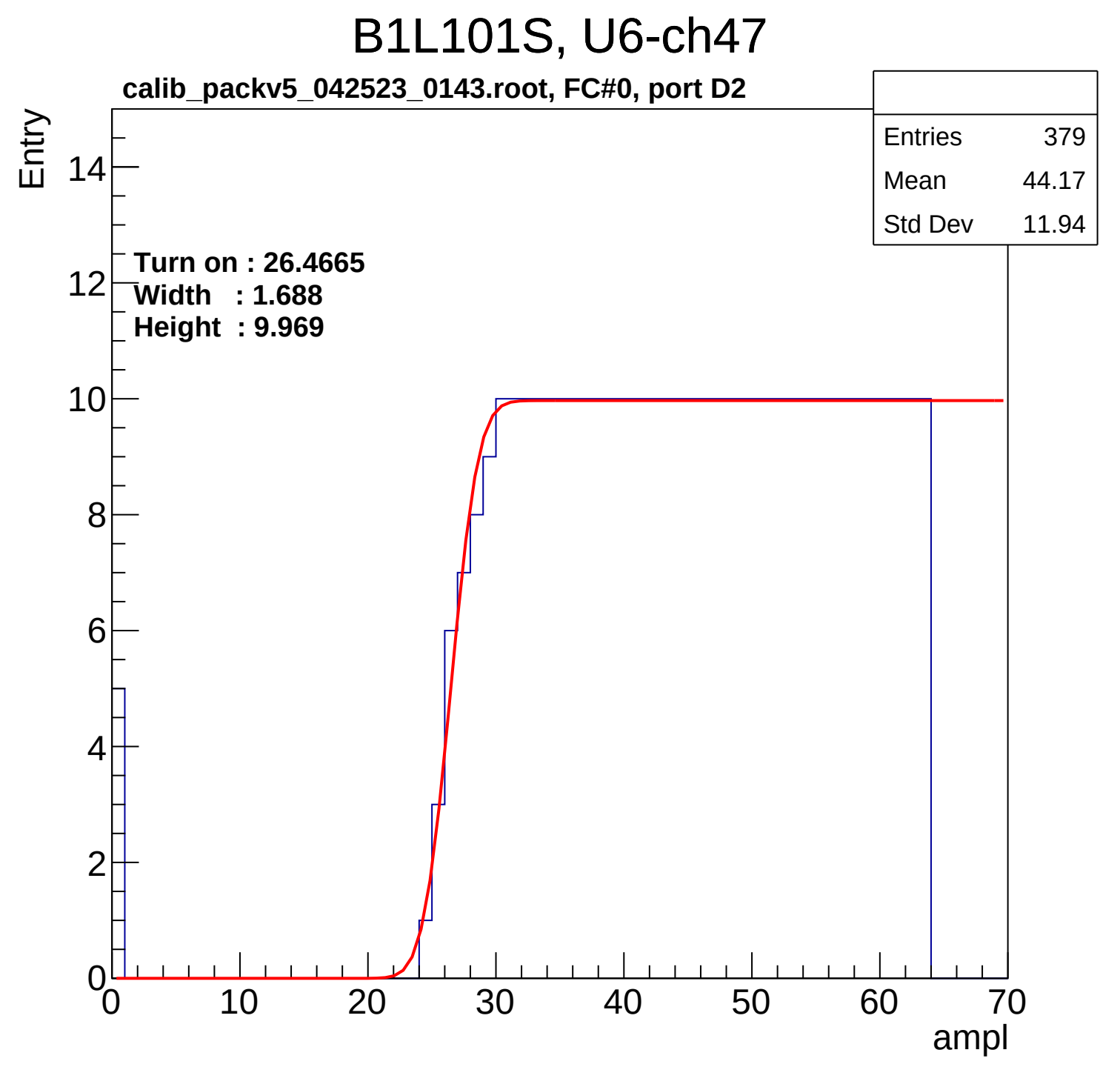

B1L101S, U6-ch42
calib_packv5_042523_0143.root, FC#0, port D2
Entries 379
Mean 44.31
Std Dev 11.5
Turn on : 26.5712
Width : 3.336
Height : 10.068
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

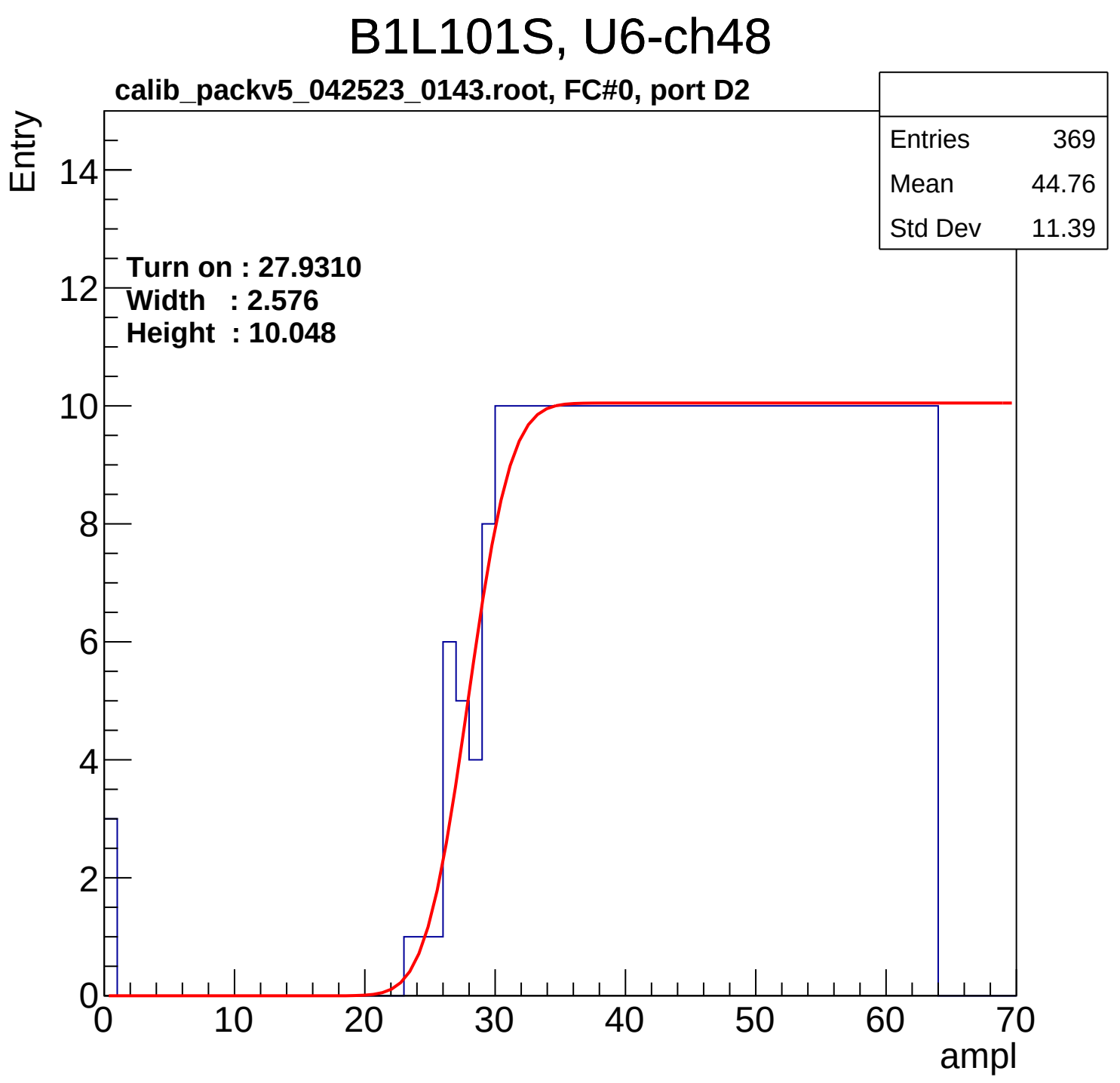

B1L101S, U6-ch43
calib_packv5_042523_0143.root, FC#0, port D2
Entries 378
Mean 44.34
Std Dev 11.49
Turn on : 26.6431
Width : 3.248
Height : 10.035
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

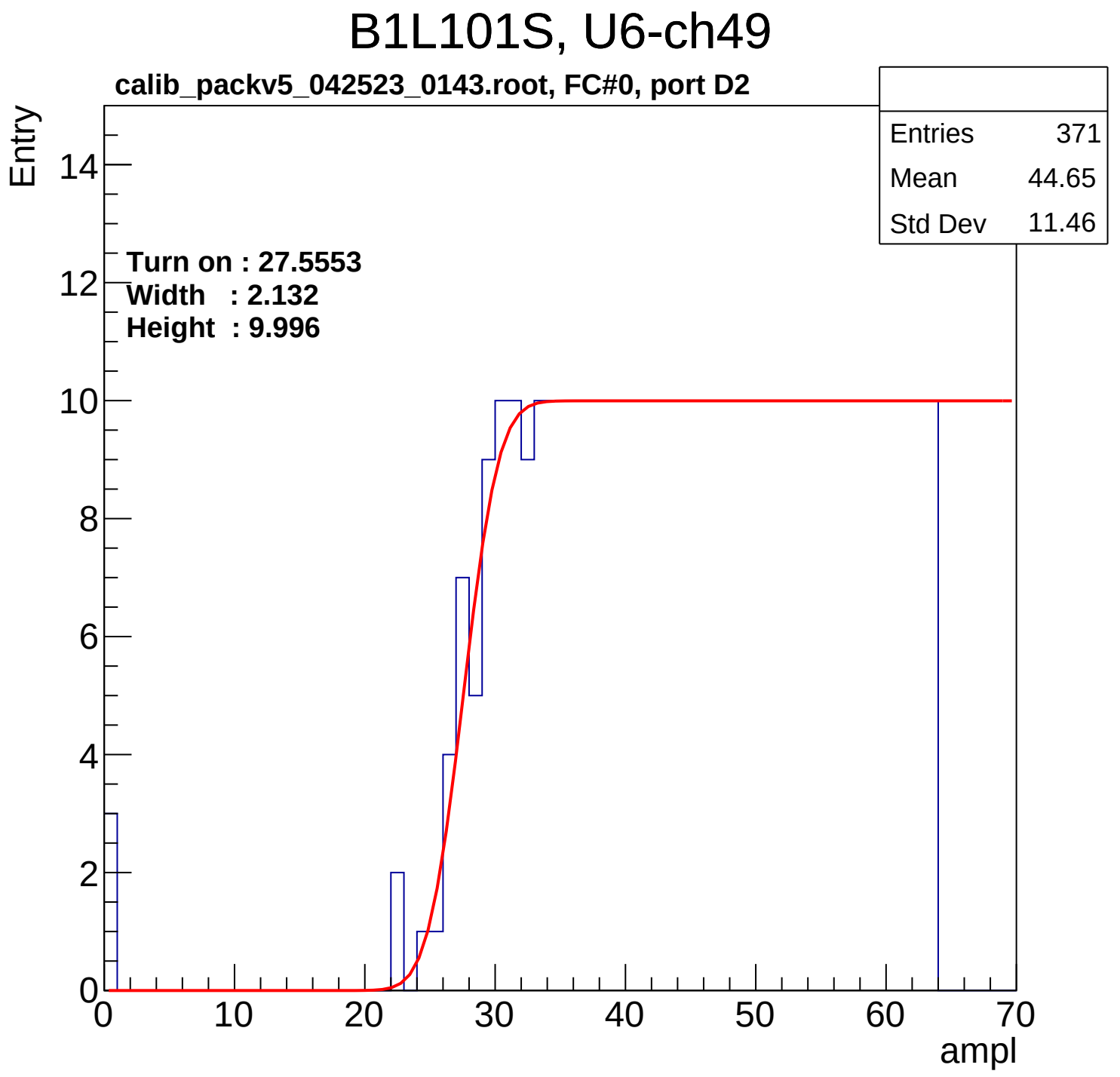

B1L101S, U6-ch44
calib_packv5_042523_0143.root, FC#0, port D2
Entries 383
Mean 44.04
Std Dev 11.79
Turn on : 26.2899
Width : 3.011
Height : 9.997
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

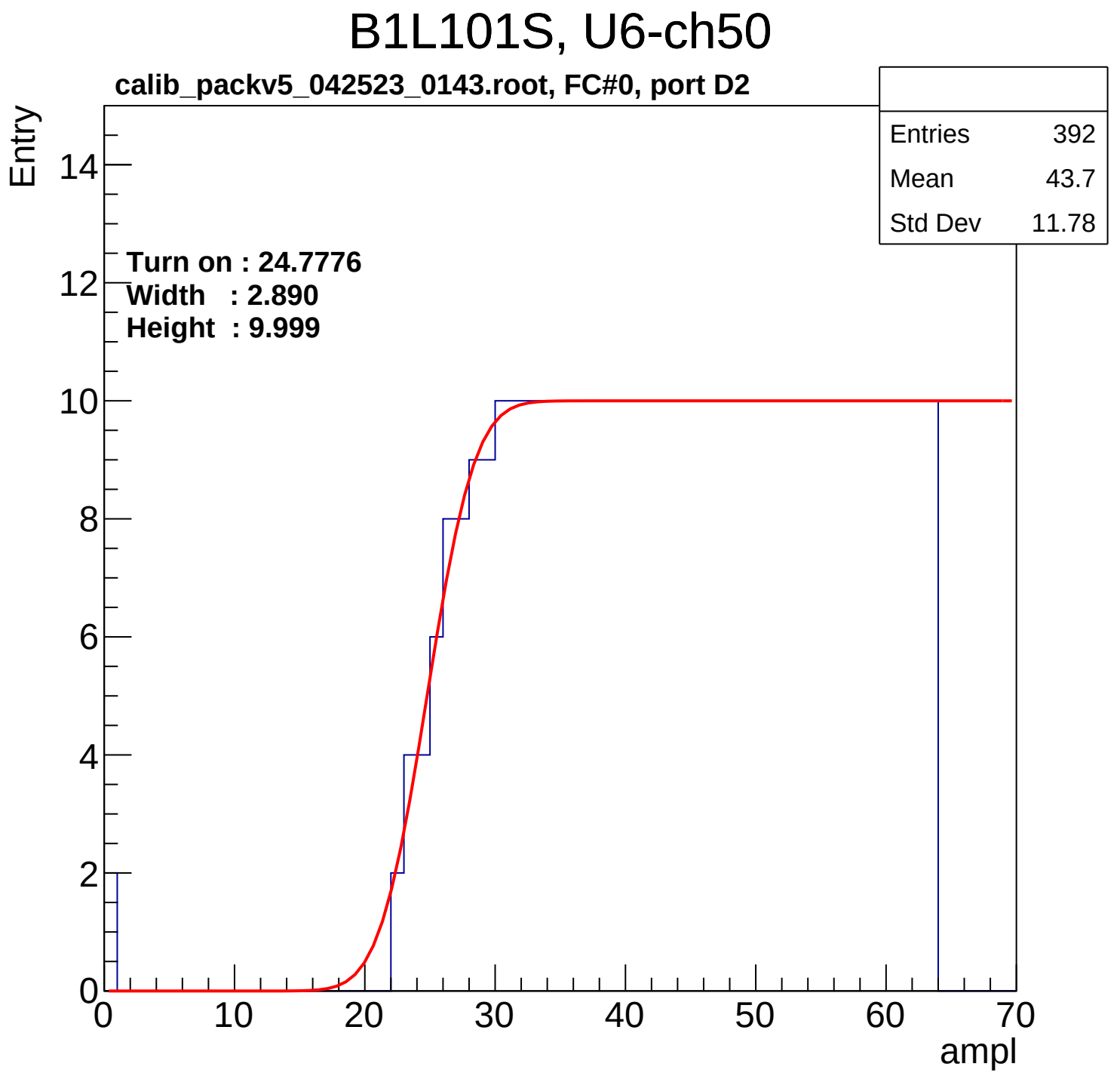

B1L101S, U6-ch45
calib_packv5_042523_0143.root, FC#0, port D2
Entries 381
Mean 44.27
Std Dev 11.46
Turn on : 26.4165
Width : 2.427
Height : 10.040
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

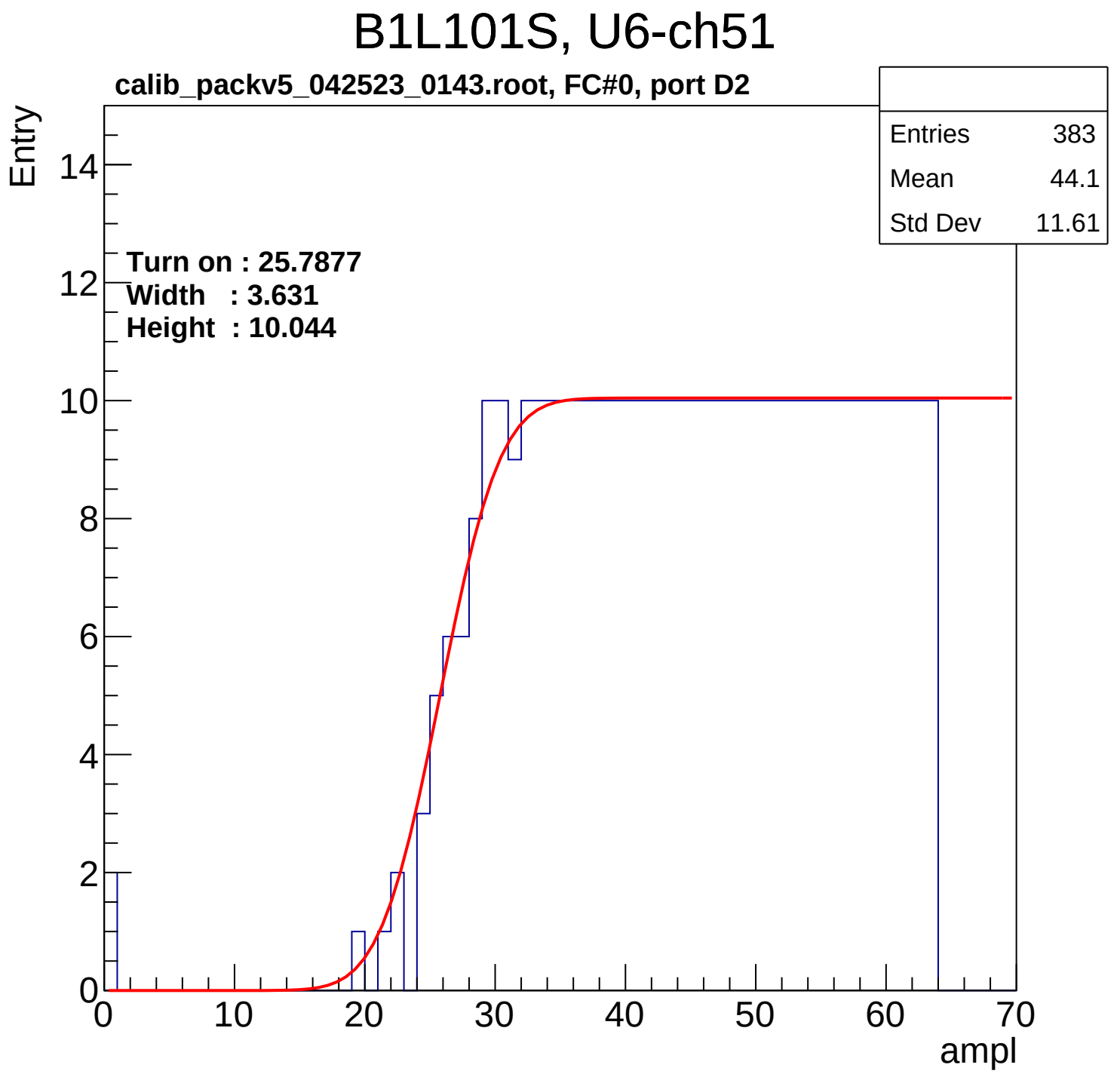

B1L101S, U6-ch46
calib_packv5_042523_0143.root, FC#0, port D2
Entries 383
Mean 44.01
Std Dev 11.84
Turn on : 26.6547
Width : 4.404
Height : 10.113
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

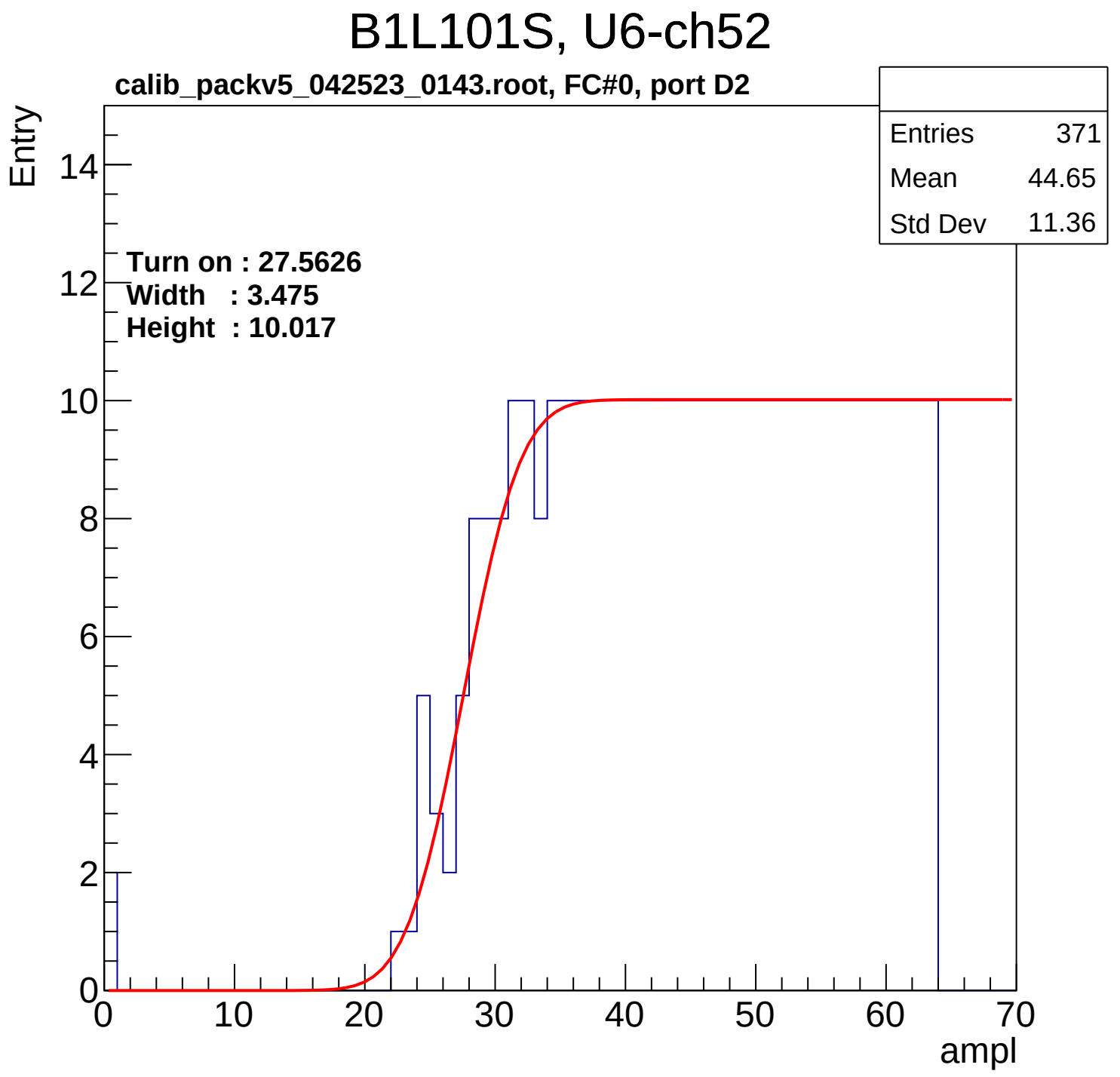

B1L101S, U6-ch47
calib_packv5_042523_0143.root, FC#0, port D2
Entries 379
Mean 44.17
Std Dev 11.94
Turn on : 26.4665
Width : 1.688
Height : 9.969
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

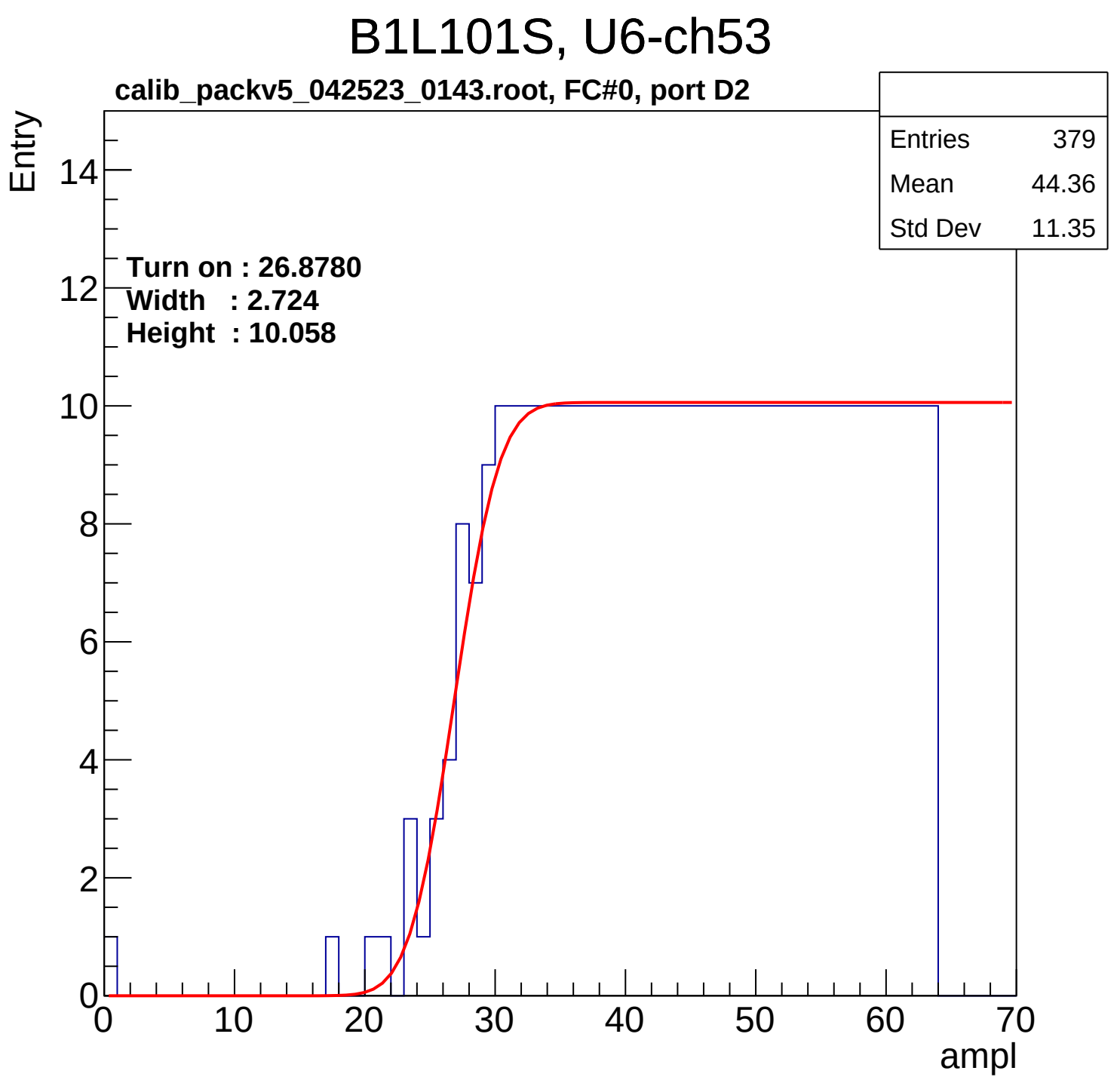

B1L101S, U6-ch48
calib_packv5_042523_0143.root, FC#0, port D2
Entries 369
Mean 44.76
Std Dev 11.39
Turn on : 27.9310
Width : 2.576
Height : 10.048
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

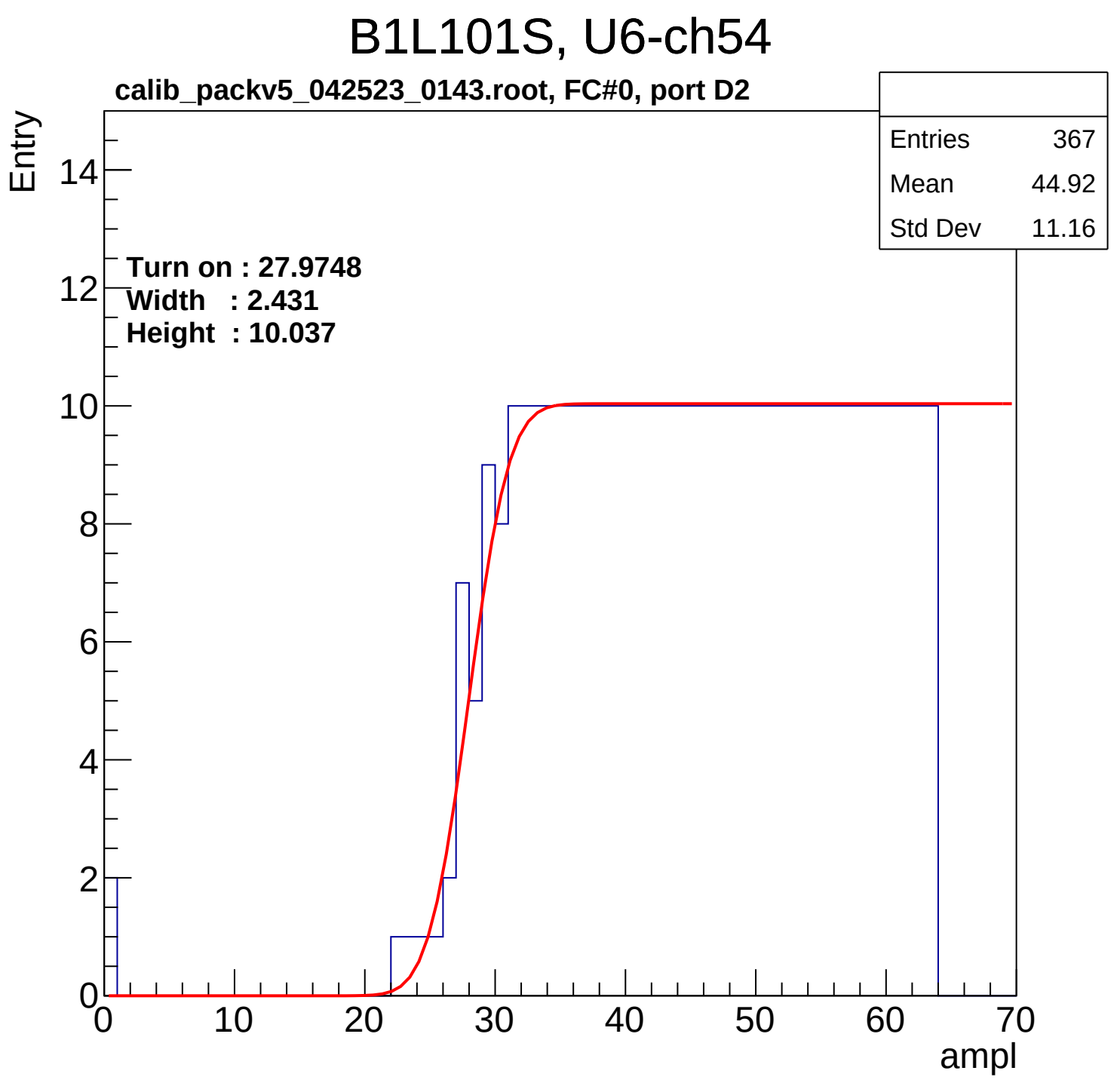

B1L101S, U6-ch49
calib_packv5_042523_0143.root, FC#0, port D2
Entries 371
Mean 44.65
Std Dev 11.46
Turn on : 27.5553
Width : 2.132
Height : 9.996
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

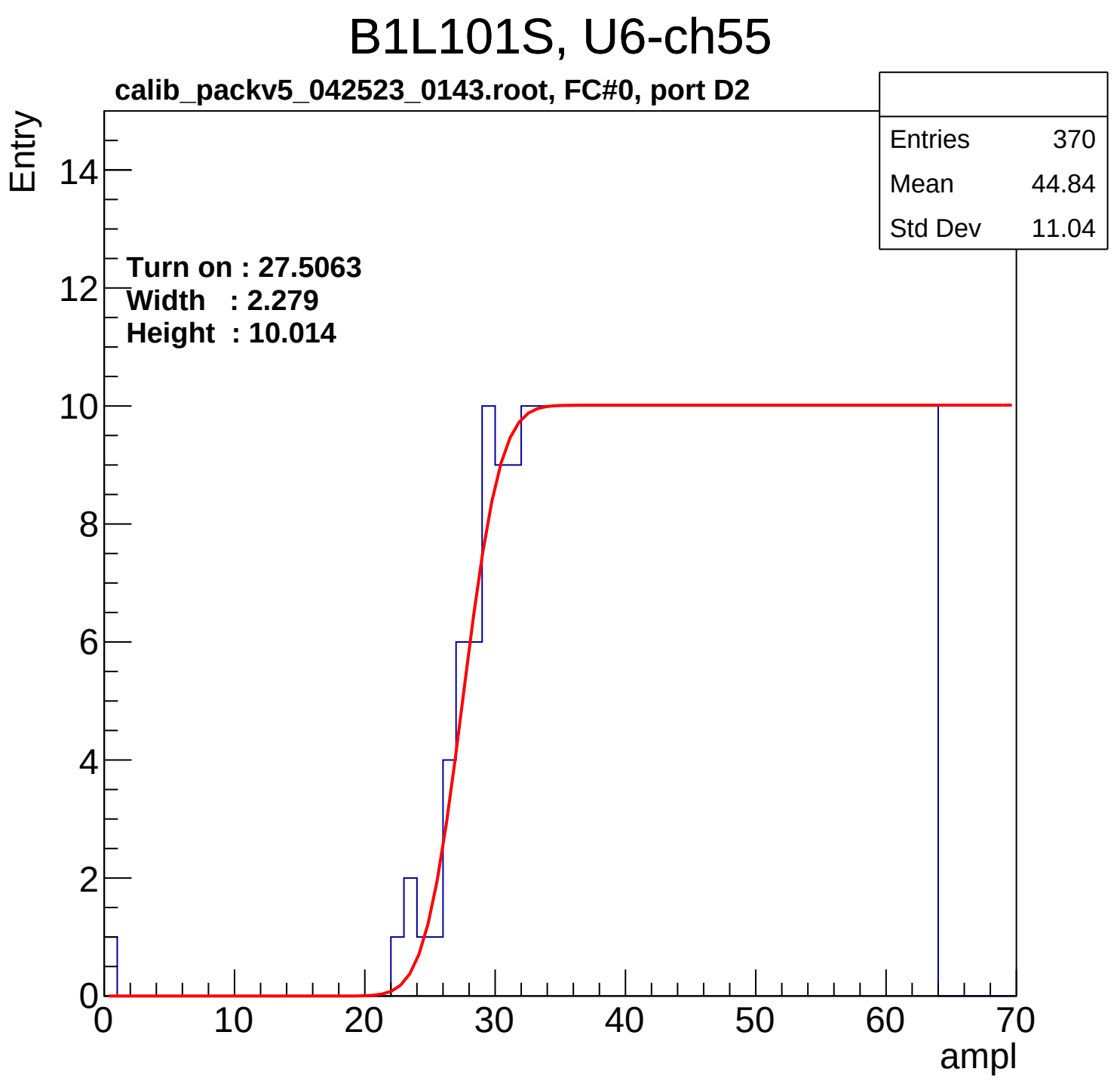

B1L101S, U6-ch50
calib_packv5_042523_0143.root, FC#0, port D2
Entries 392
Mean 43.7
Std Dev 11.78
Turn on : 24.7776
Width : 2.890
Height : 9.999
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

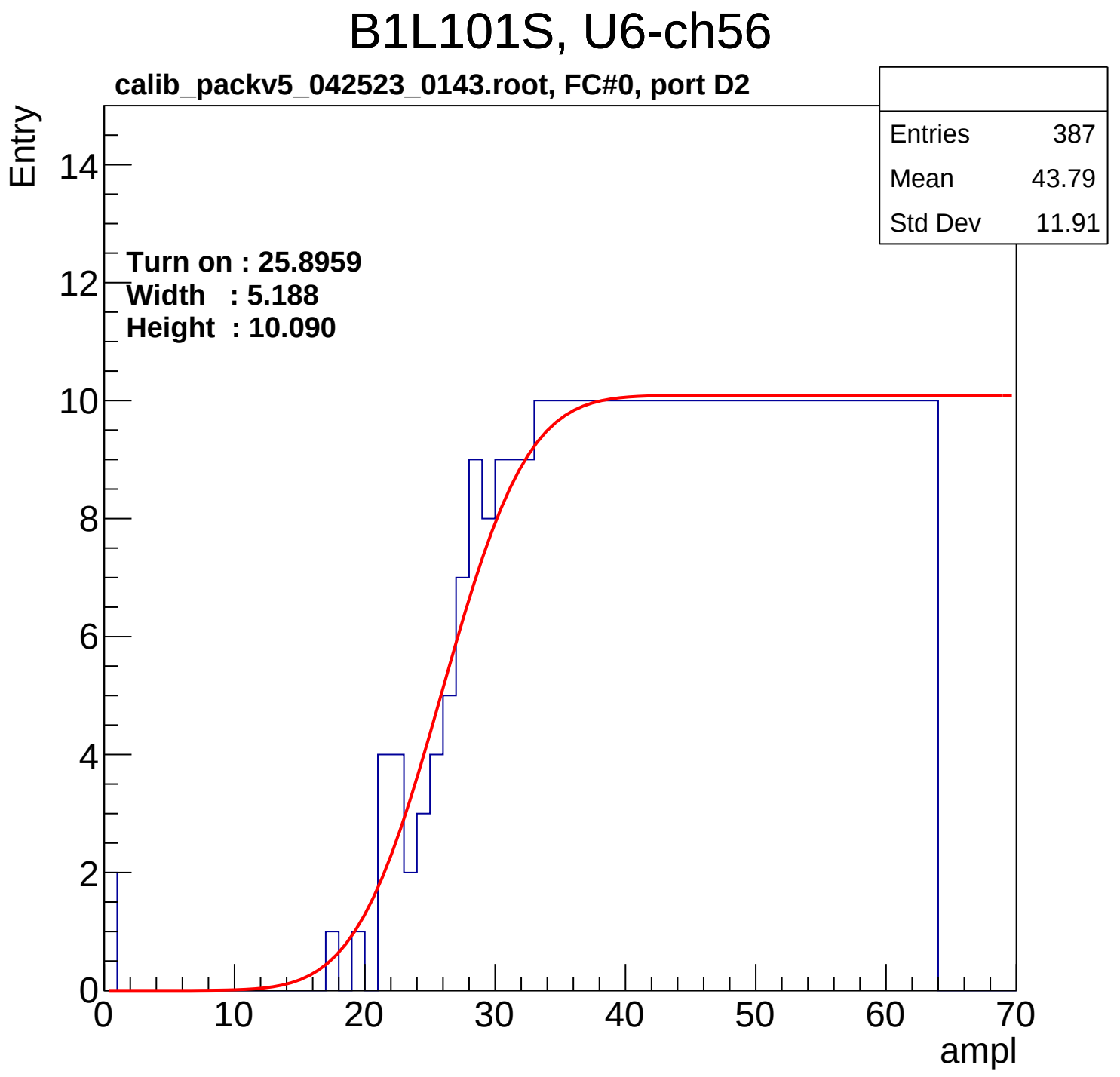

B1L101S, U6-ch51
calib_packv5_042523_0143.root, FC#0, port D2
Entries 383
Mean 44.1
Std Dev 11.61
Turn on : 25.7877
Width : 3.631
Height : 10.044
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

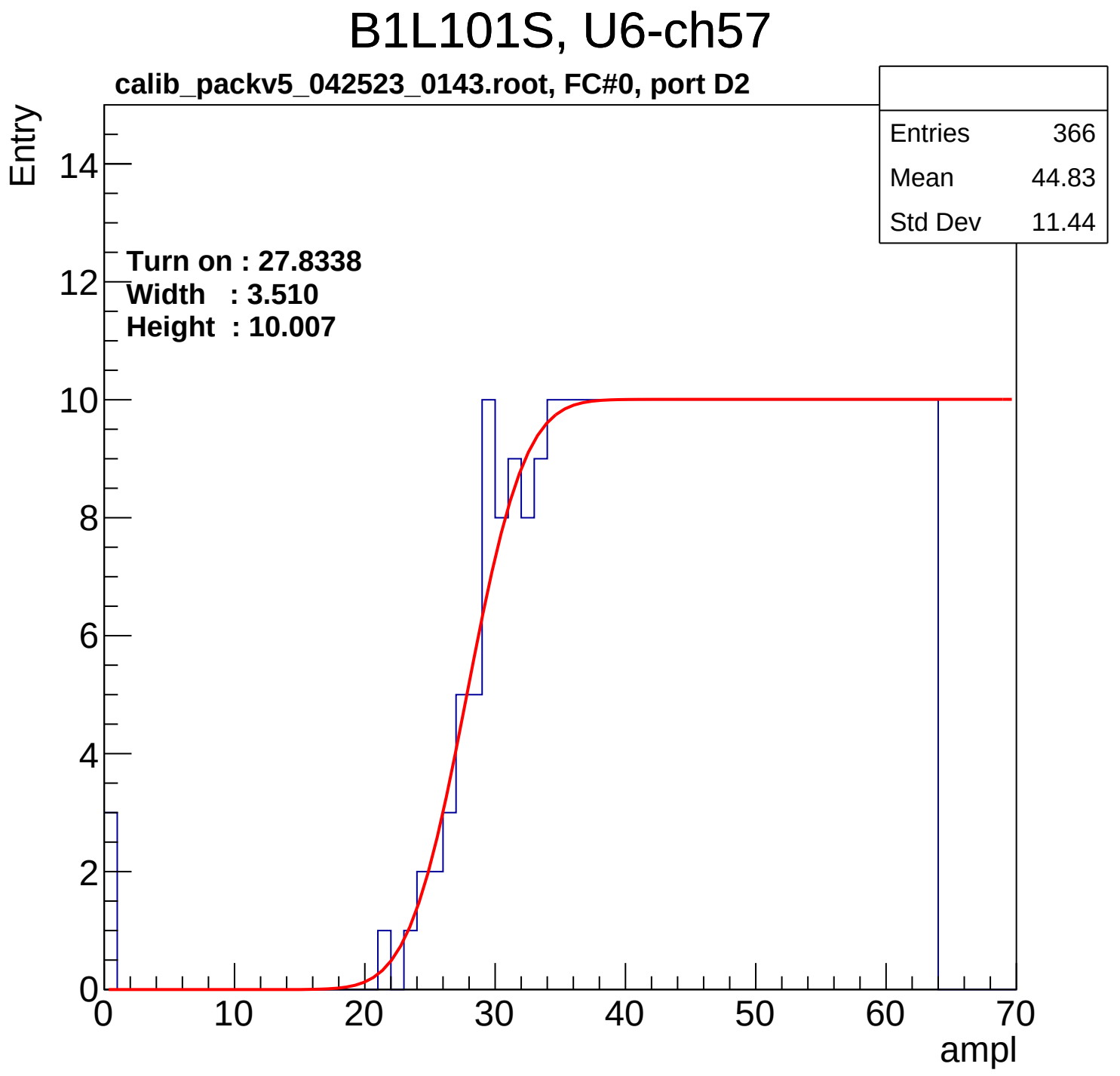

B1L101S, U6-ch52
calib_packv5_042523_0143.root, FC#0, port D2
Entries 371
Mean 44.65
Std Dev 11.36
Turn on : 27.5626
Width : 3.475
Height : 10.017
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

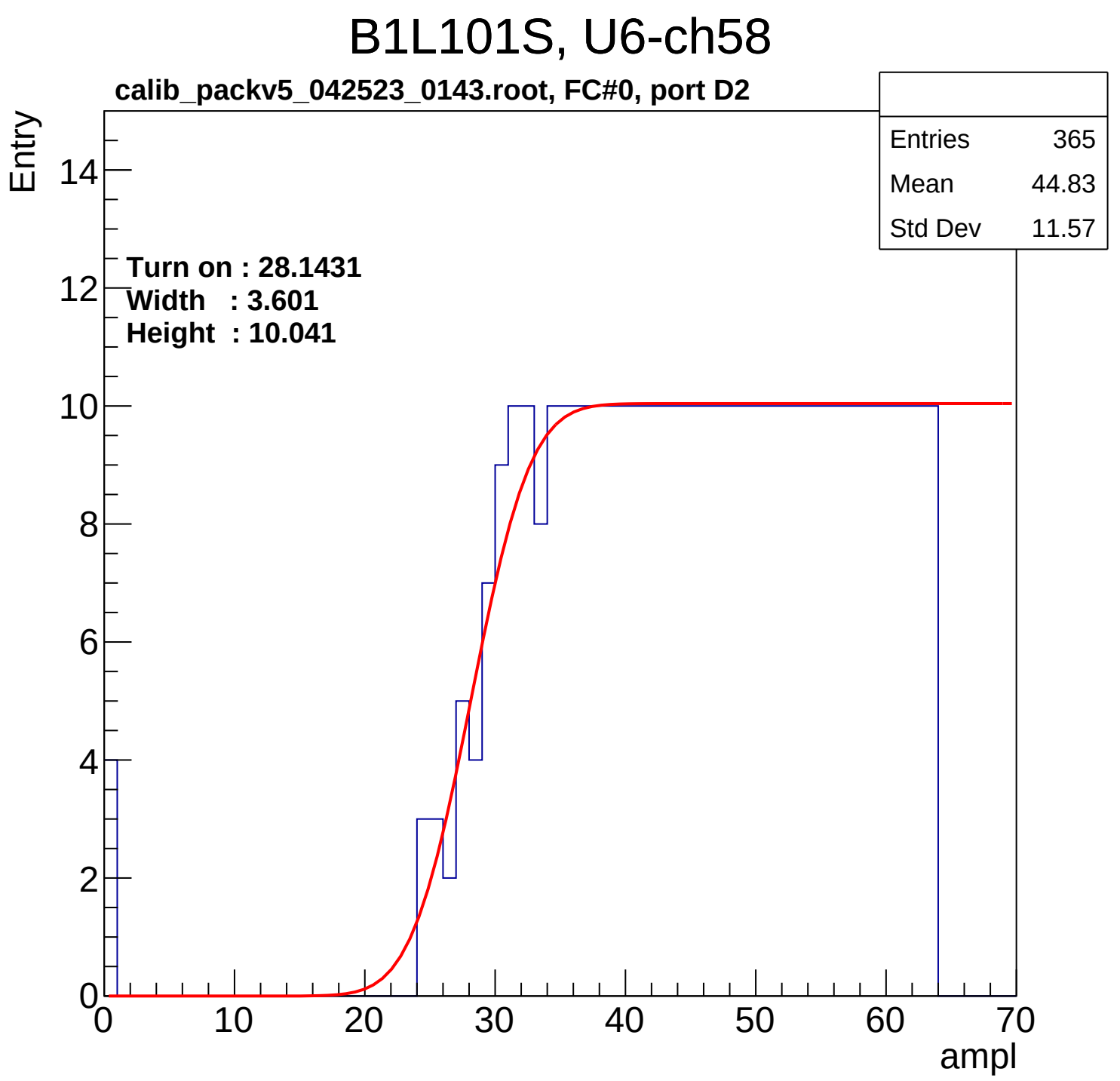

B1L101S, U6-ch53
calib_packv5_042523_0143.root, FC#0, port D2
Entries 379
Mean 44.36
Std Dev 11.35
Turn on : 26.8780
Width : 2.724
Height : 10.058
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

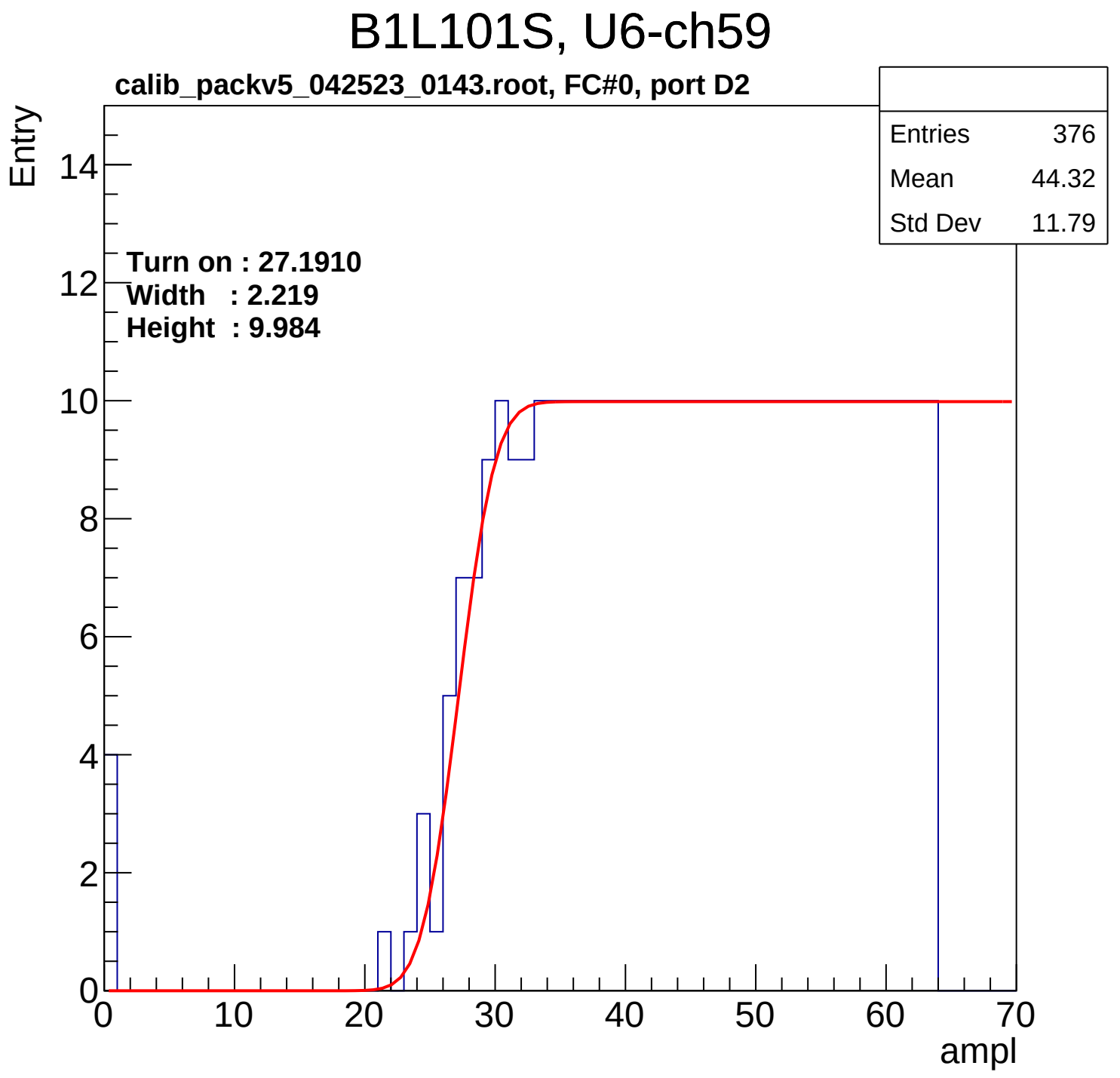

B1L101S, U6-ch54
calib_packv5_042523_0143.root, FC#0, port D2
Entries 367
Mean 44.92
Std Dev 11.16
Turn on : 27.9748
Width : 2.431
Height : 10.037
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

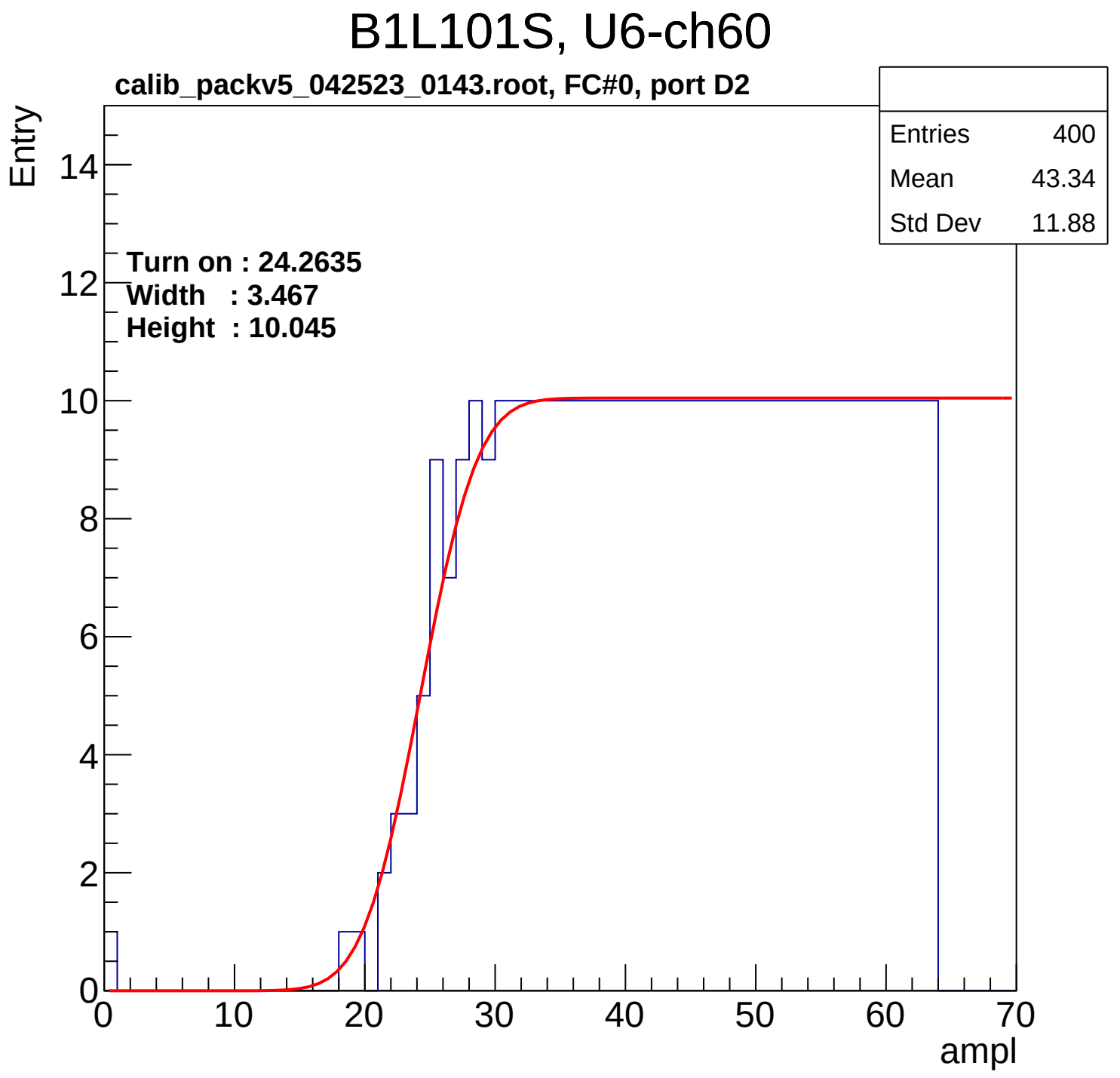

B1L101S, U6-ch55
calib_packv5_042523_0143.root, FC#0, port D2
Entries 370
Mean 44.84
Std Dev 11.04
Turn on : 27.5063
Width : 2.279
Height : 10.014
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

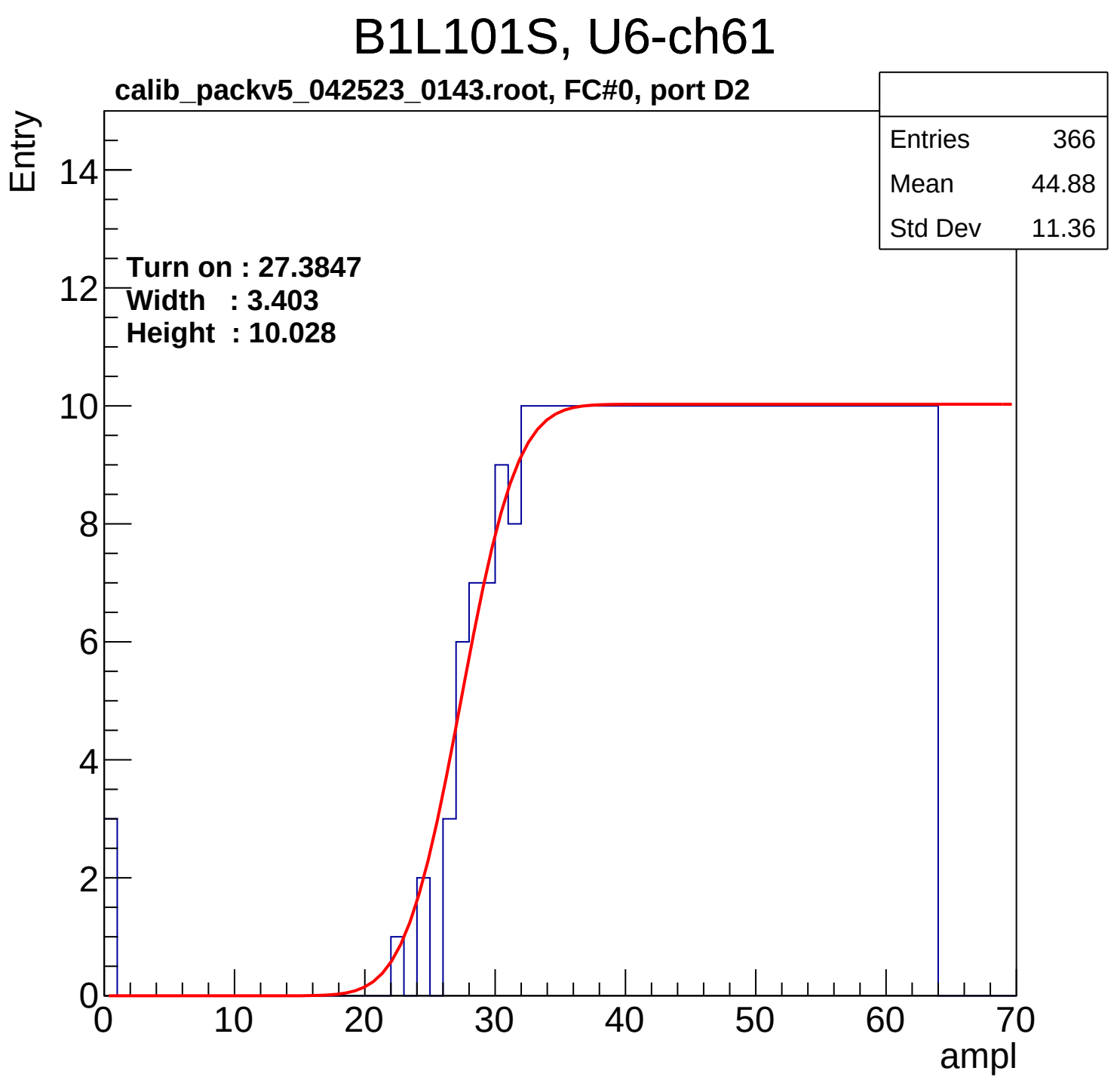

B1L101S, U6-ch56
calib_packv5_042523_0143.root, FC#0, port D2
Entries 387
Mean 43.79
Std Dev 11.91
Turn on : 25.8959
Width : 5.188
Height : 10.090
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

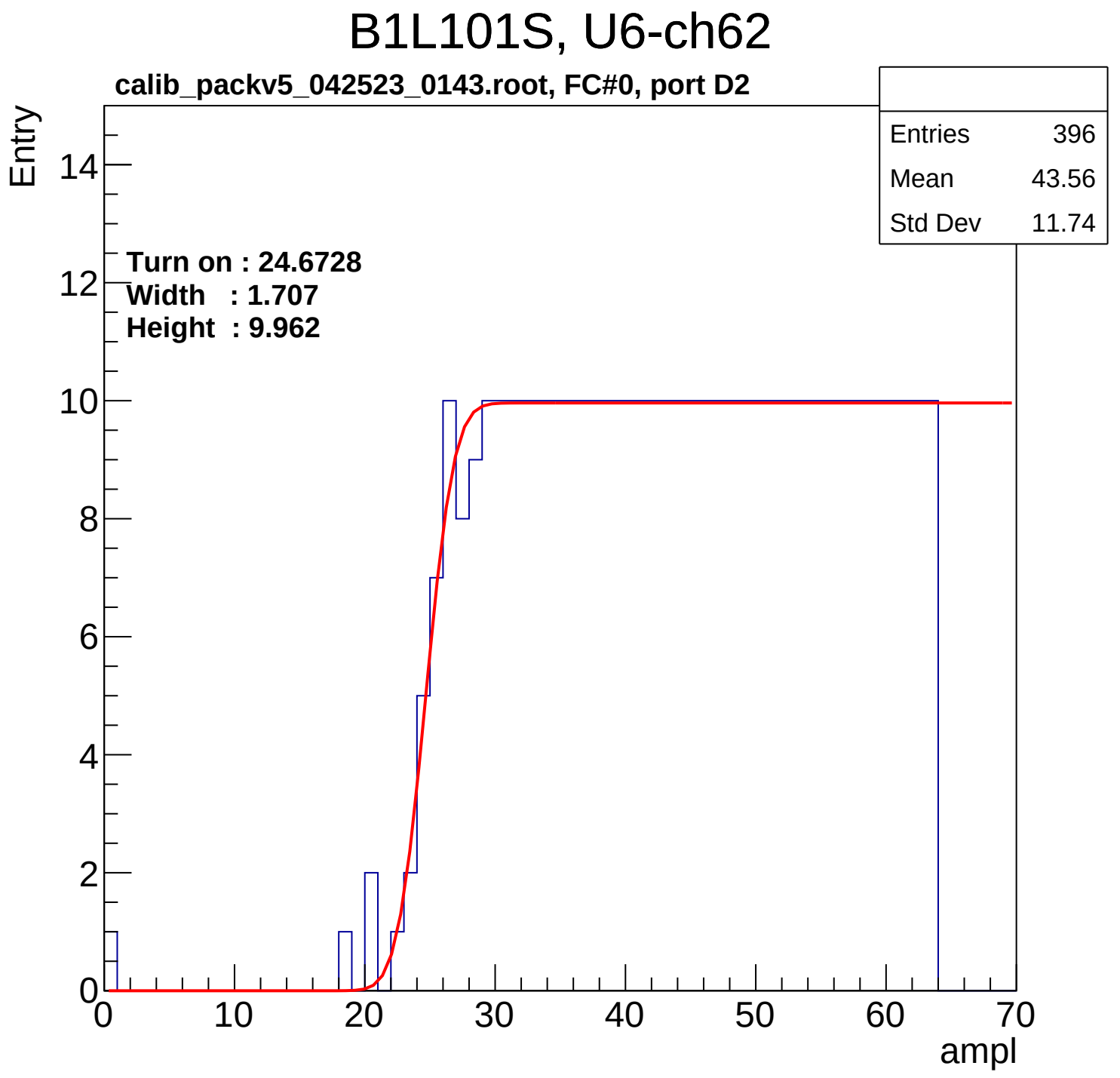

B1L101S, U6-ch57
calib_packv5_042523_0143.root, FC#0, port D2
Entries 366
Mean 44.83
Std Dev 11.44
Turn on : 27.8338
Width : 3.510
Height : 10.007
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

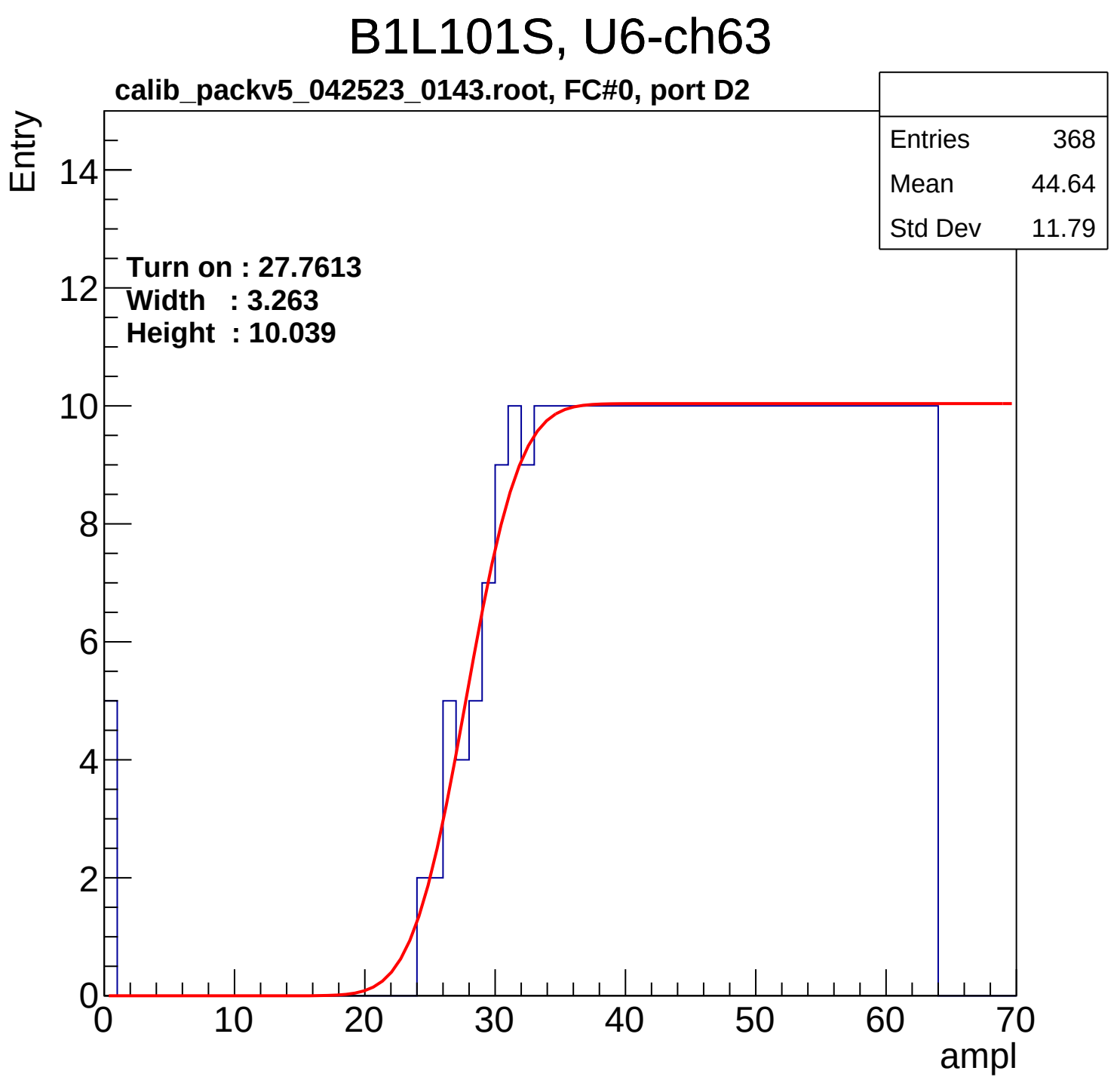

B1L101S, U6-ch58
calib_packv5_042523_0143.root, FC#0, port D2
Entries 365
Mean 44.83
Std Dev 11.57
Turn on : 28.1431
Width : 3.601
Height : 10.041
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

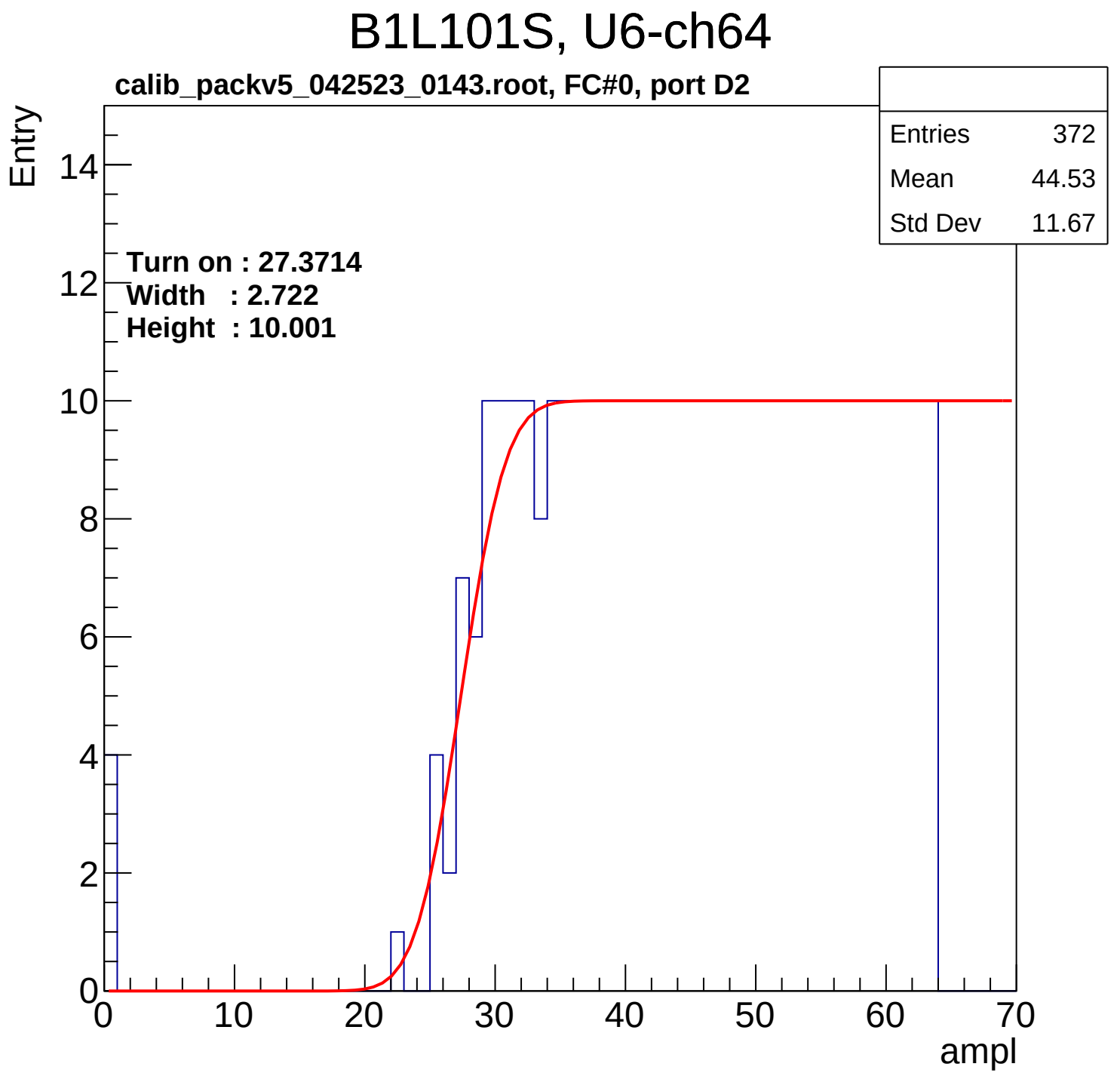

B1L101S, U6-ch59
calib_packv5_042523_0143.root, FC#0, port D2
Entries 376
Mean 44.32
Std Dev 11.79
Turn on : 27.1910
Width : 2.219
Height : 9.984
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

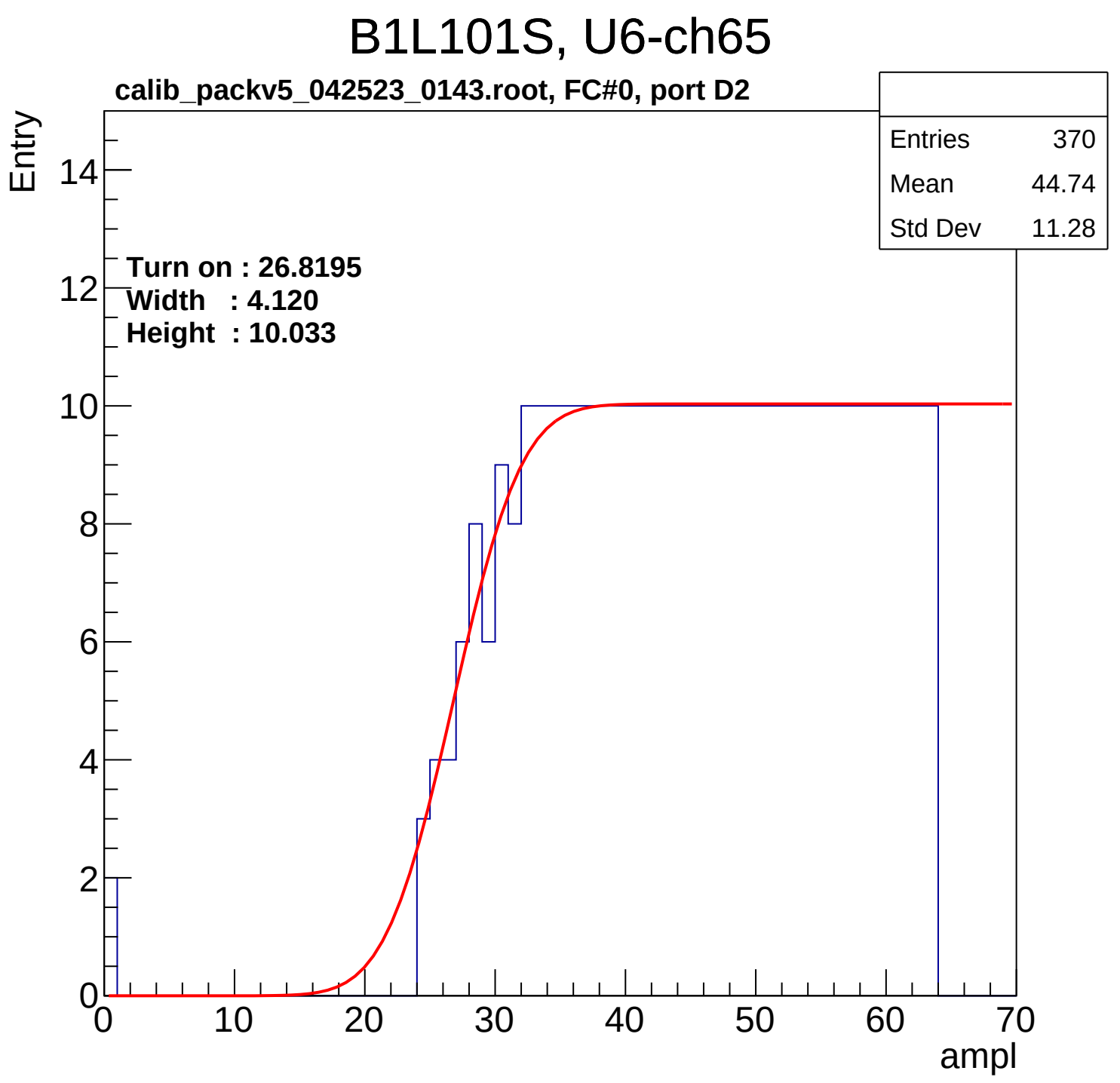

B1L101S, U6-ch60
calib_packv5_042523_0143.root, FC#0, port D2
Entries 400
Mean 43.34
Std Dev 11.88
Turn on : 24.2635
Width : 3.467
Height : 10.045
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

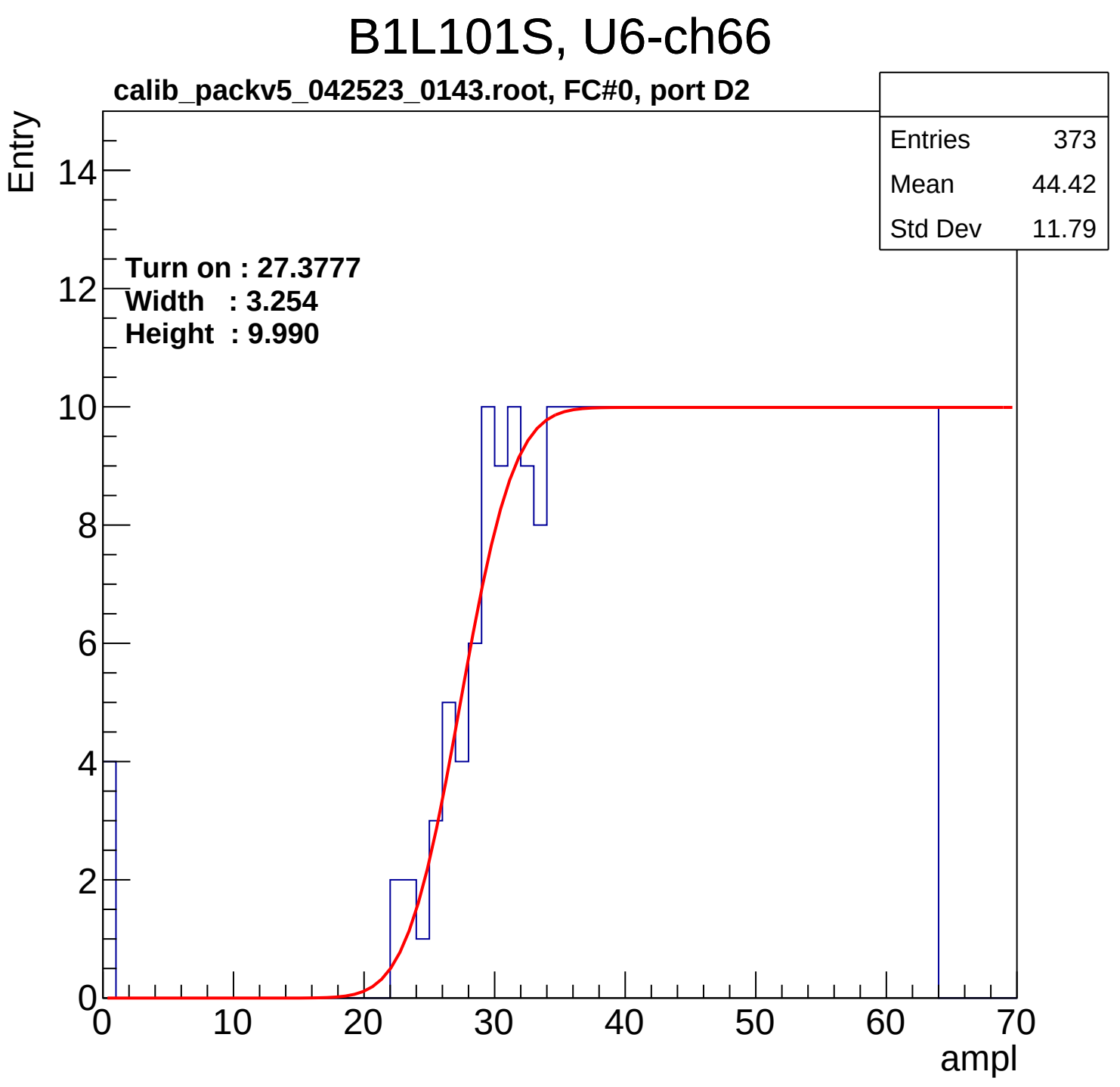

B1L101S, U6-ch61
calib_packv5_042523_0143.root, FC#0, port D2
Entries 366
Mean 44.88
Std Dev 11.36
Turn on : 27.3847
Width : 3.403
Height : 10.028
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

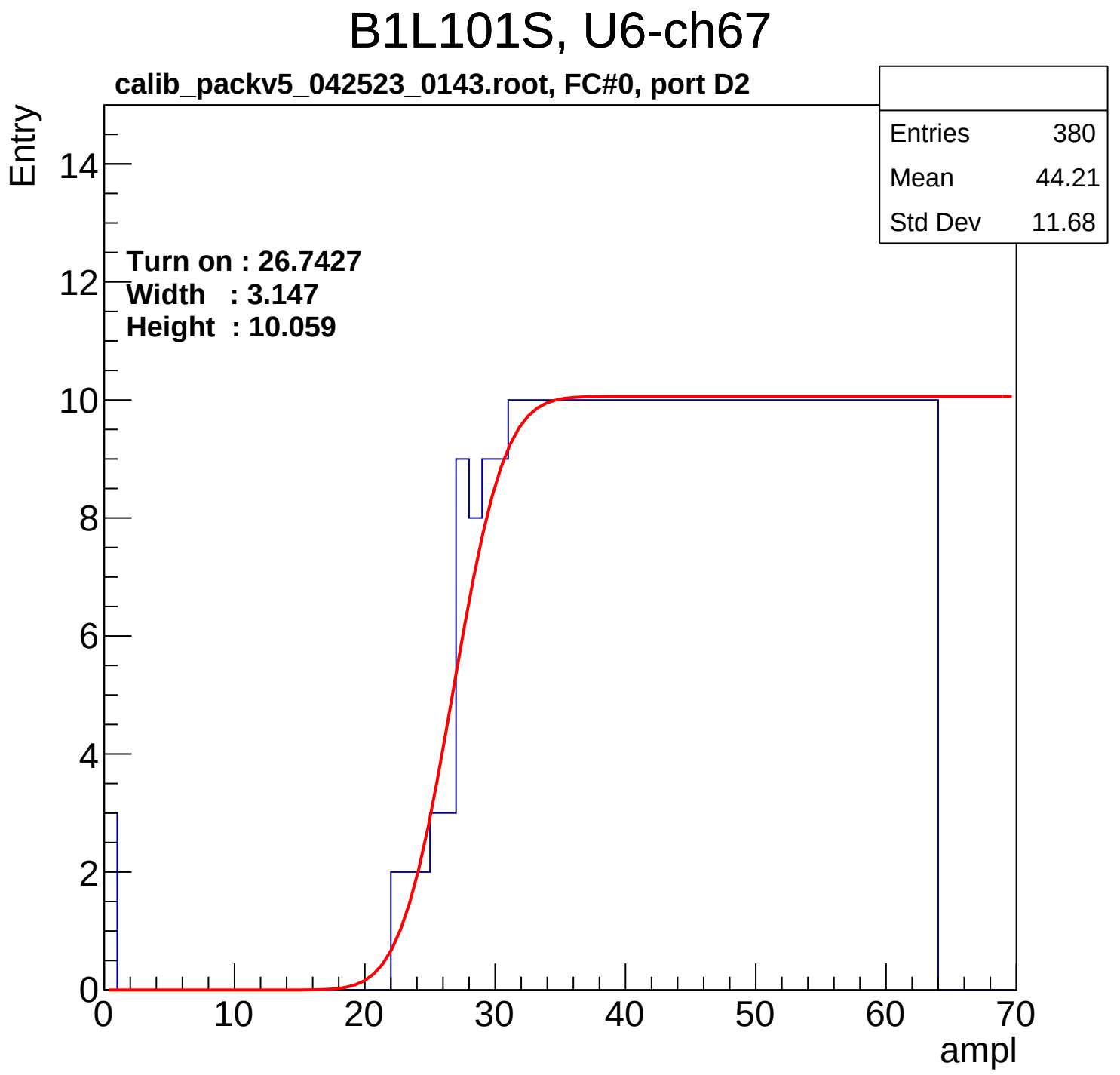

B1L101S, U6-ch62
calib_packv5_042523_0143.root, FC#0, port D2
Entries 396
Mean 43.56
Std Dev 11.74
Turn on : 24.6728
Width : 1.707
Height : 9.962
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

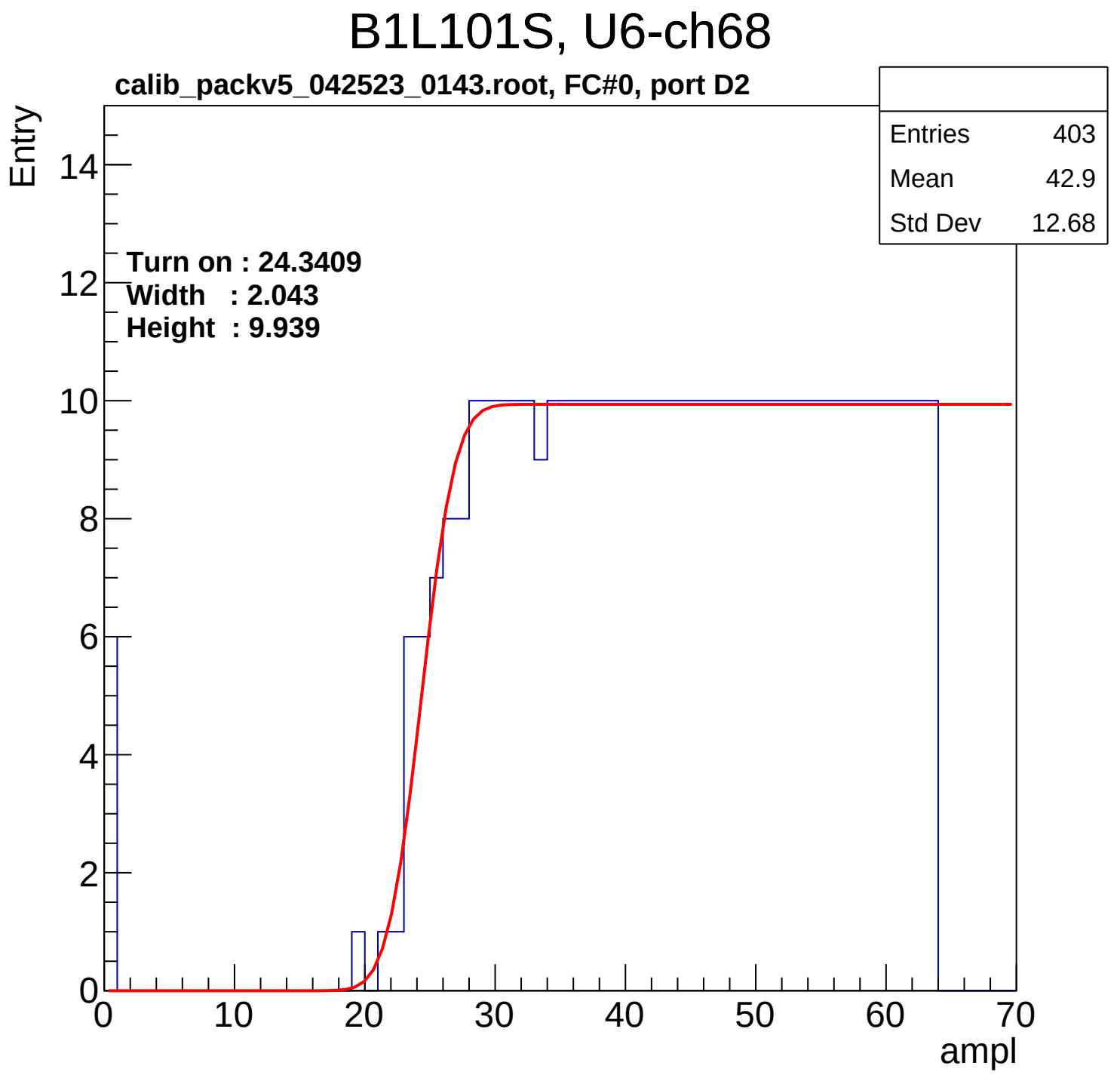

B1L101S, U6-ch63
calib_packv5_042523_0143.root, FC#0, port D2
Entries 368
Mean 44.64
Std Dev 11.79
Turn on : 27.7613
Width : 3.263
Height : 10.039
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

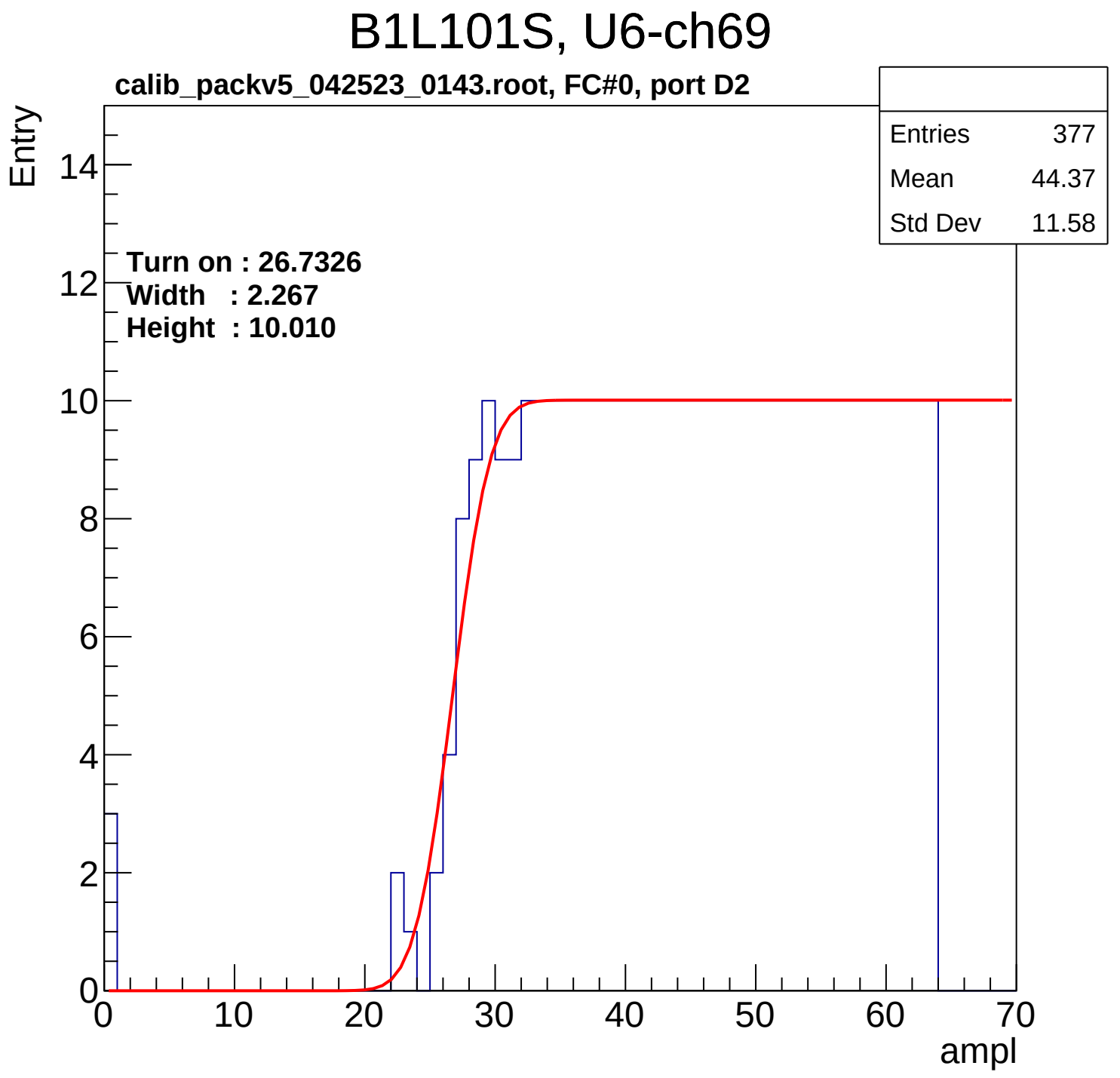

B1L101S, U6-ch64
calib_packv5_042523_0143.root, FC#0, port D2
Entries 372
Mean 44.53
Std Dev 11.67
Turn on : 27.3714
Width : 2.722
Height : 10.001
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

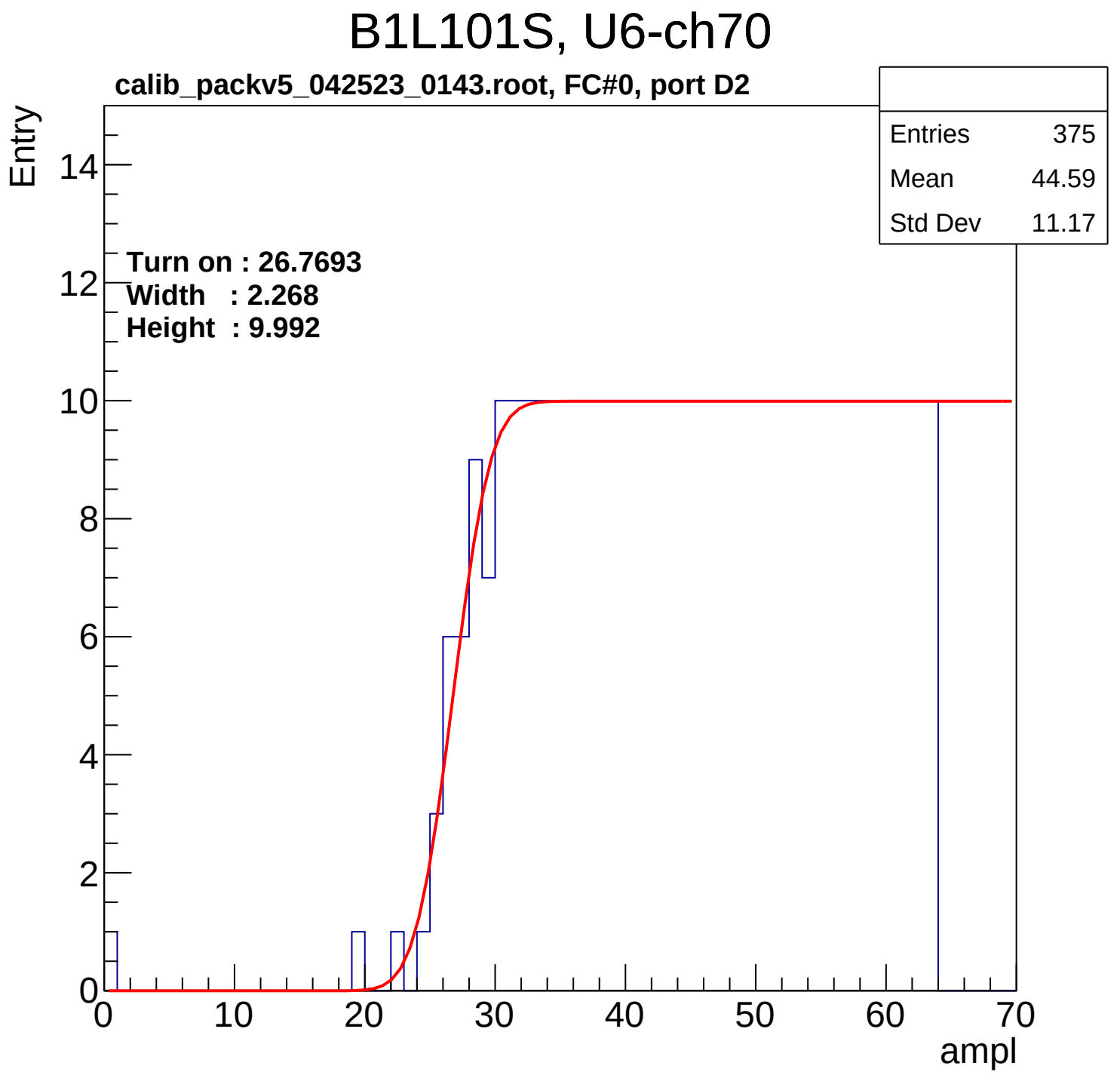

B1L101S, U6-ch65
calib_packv5_042523_0143.root, FC#0, port D2
Entries 370
Mean 44.74
Std Dev 11.28
Turn on : 26.8195
Width : 4.120
Height : 10.033
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

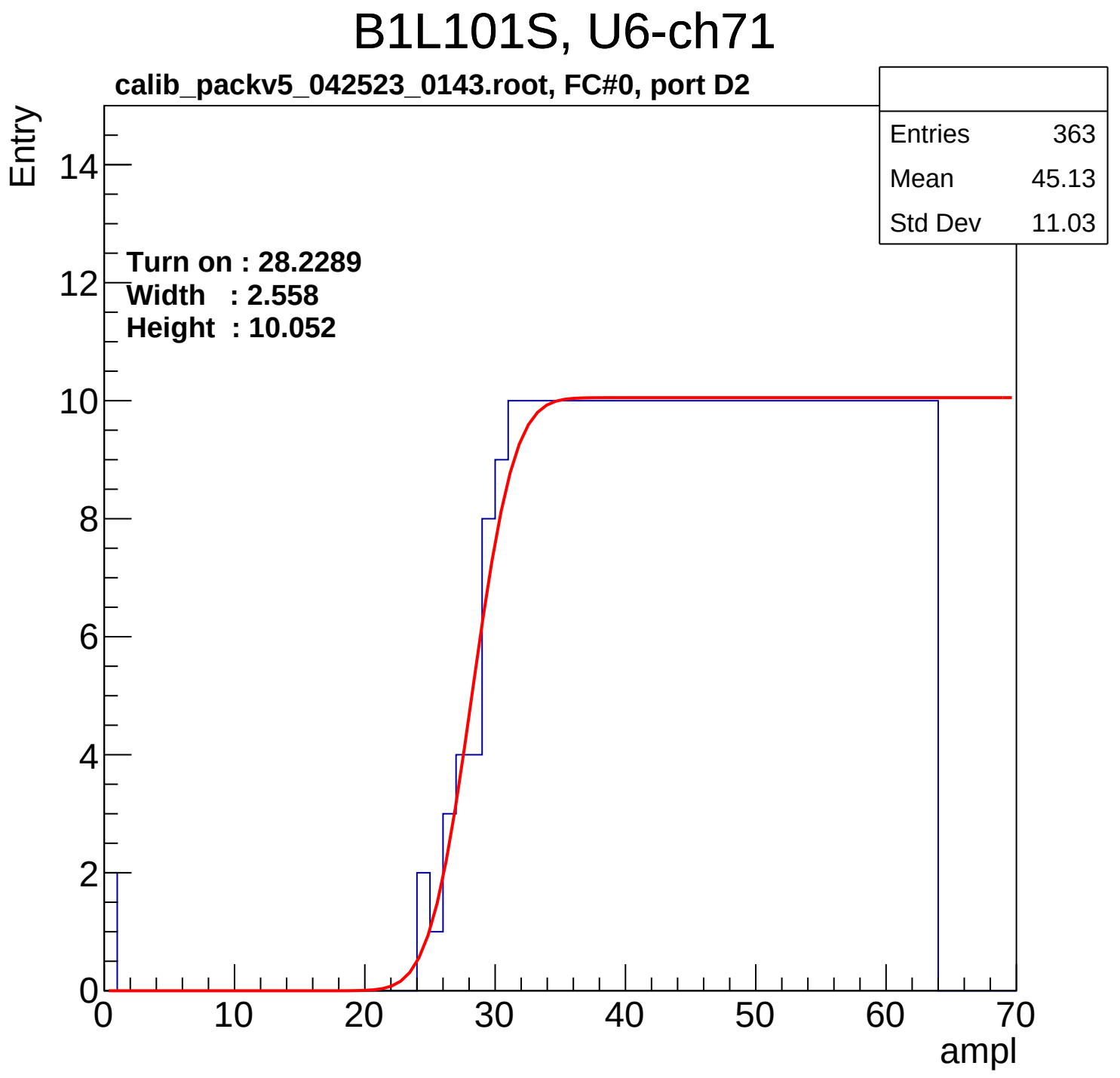

B1L101S, U6-ch66
calib_packv5_042523_0143.root, FC#0, port D2
Entries 373
Mean 44.42
Std Dev 11.79
Turn on : 27.3777
Width : 3.254
Height : 9.990
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

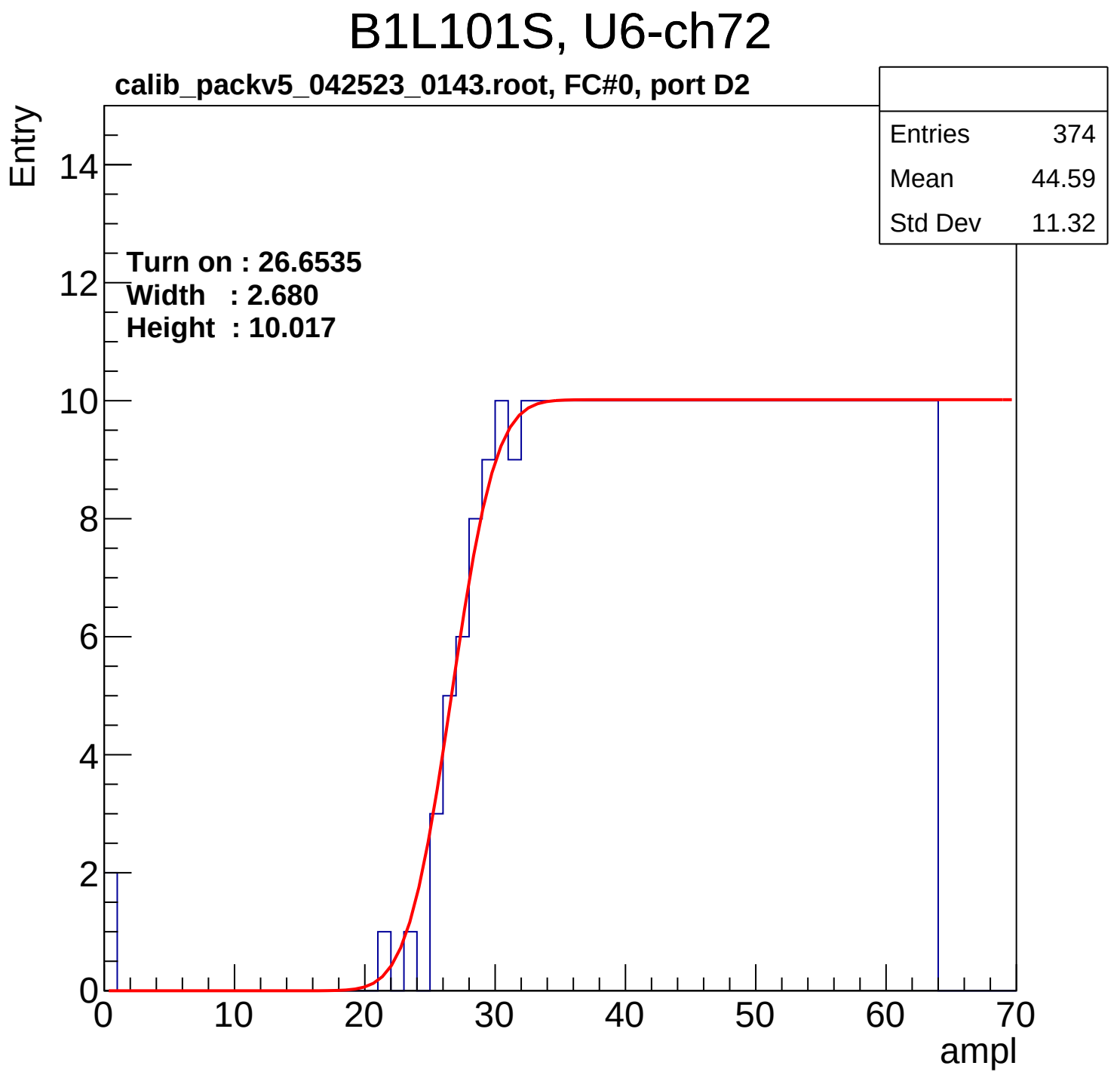

B1L101S, U6-ch67
calib_packv5_042523_0143.root, FC#0, port D2
Entries 380
Mean 44.21
Std Dev 11.68
Turn on : 26.7427
Width : 3.147
Height : 10.059
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

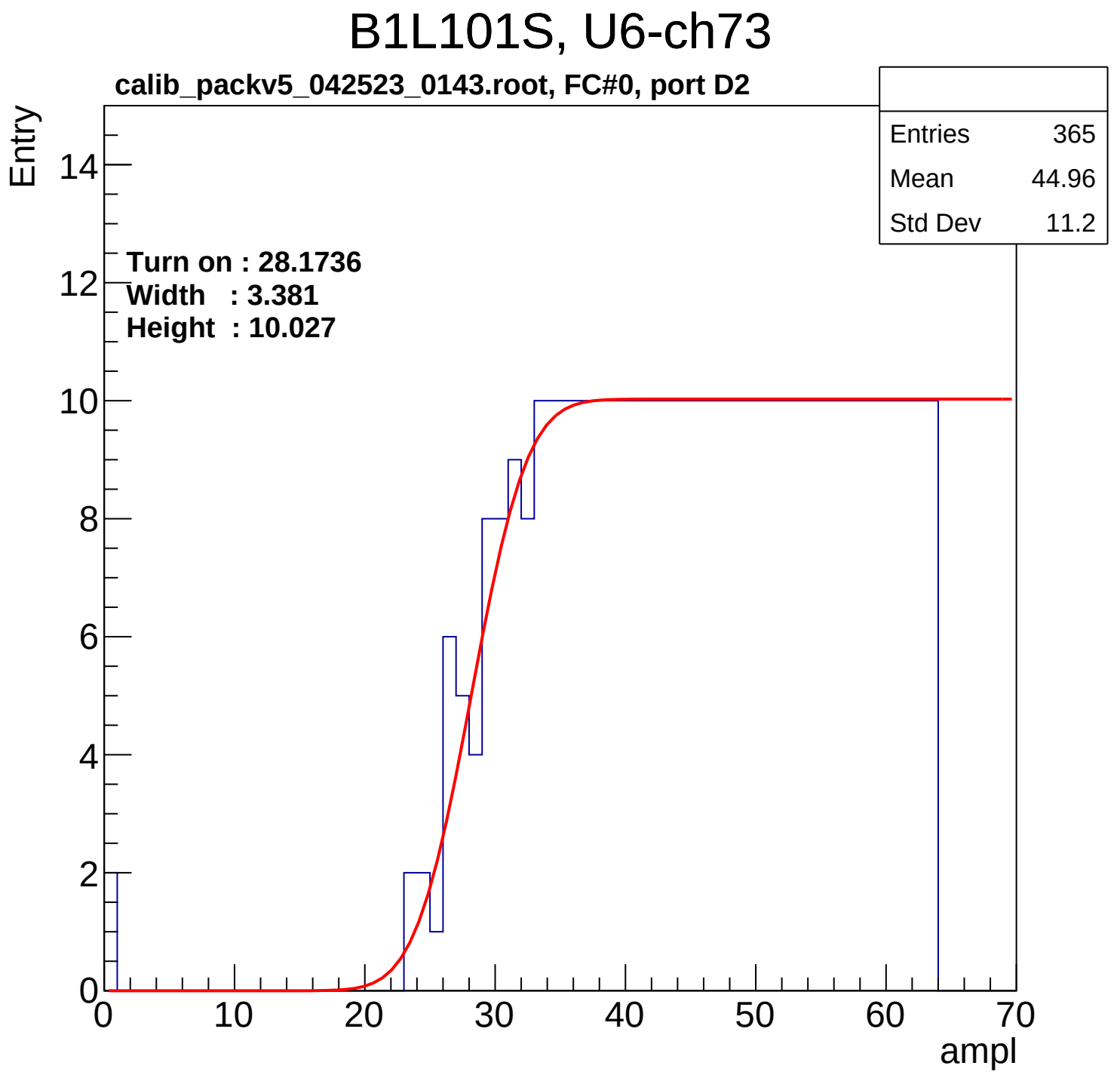

B1L101S, U6-ch68
calib_packv5_042523_0143.root, FC#0, port D2
Entries 403
Mean 42.9
Std Dev 12.68
Turn on : 24.3409
Width : 2.043
Height : 9.939
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

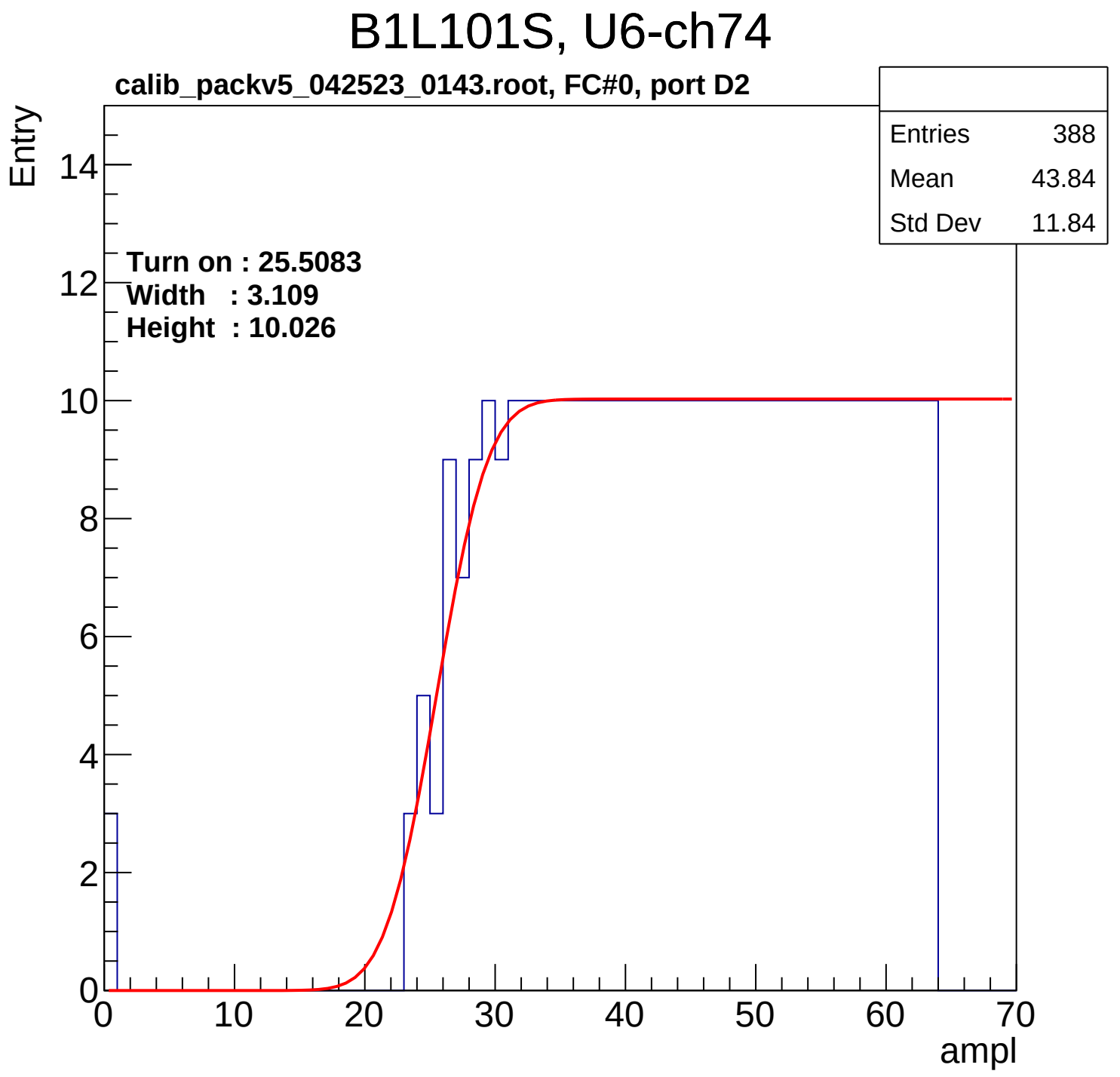

B1L101S, U6-ch69
calib_packv5_042523_0143.root, FC#0, port D2
Entries 377
Mean 44.37
Std Dev 11.58
Turn on : 26.7326
Width : 2.267
Height : 10.010
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

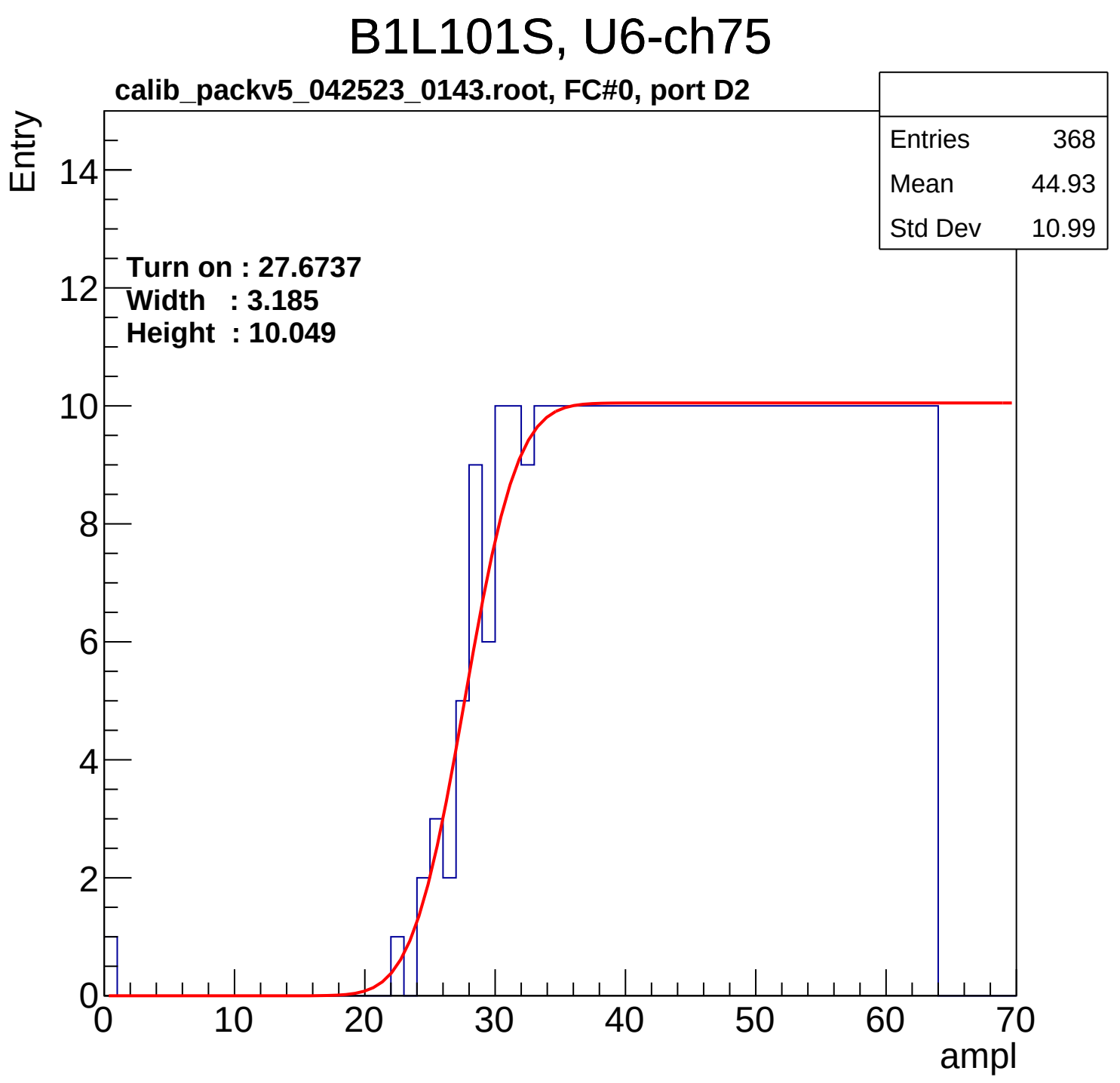

B1L101S, U6-ch70
calib_packv5_042523_0143.root, FC#0, port D2
Entries 375
Mean 44.59
Std Dev 11.17
Turn on : 26.7693
Width : 2.268
Height : 9.992
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

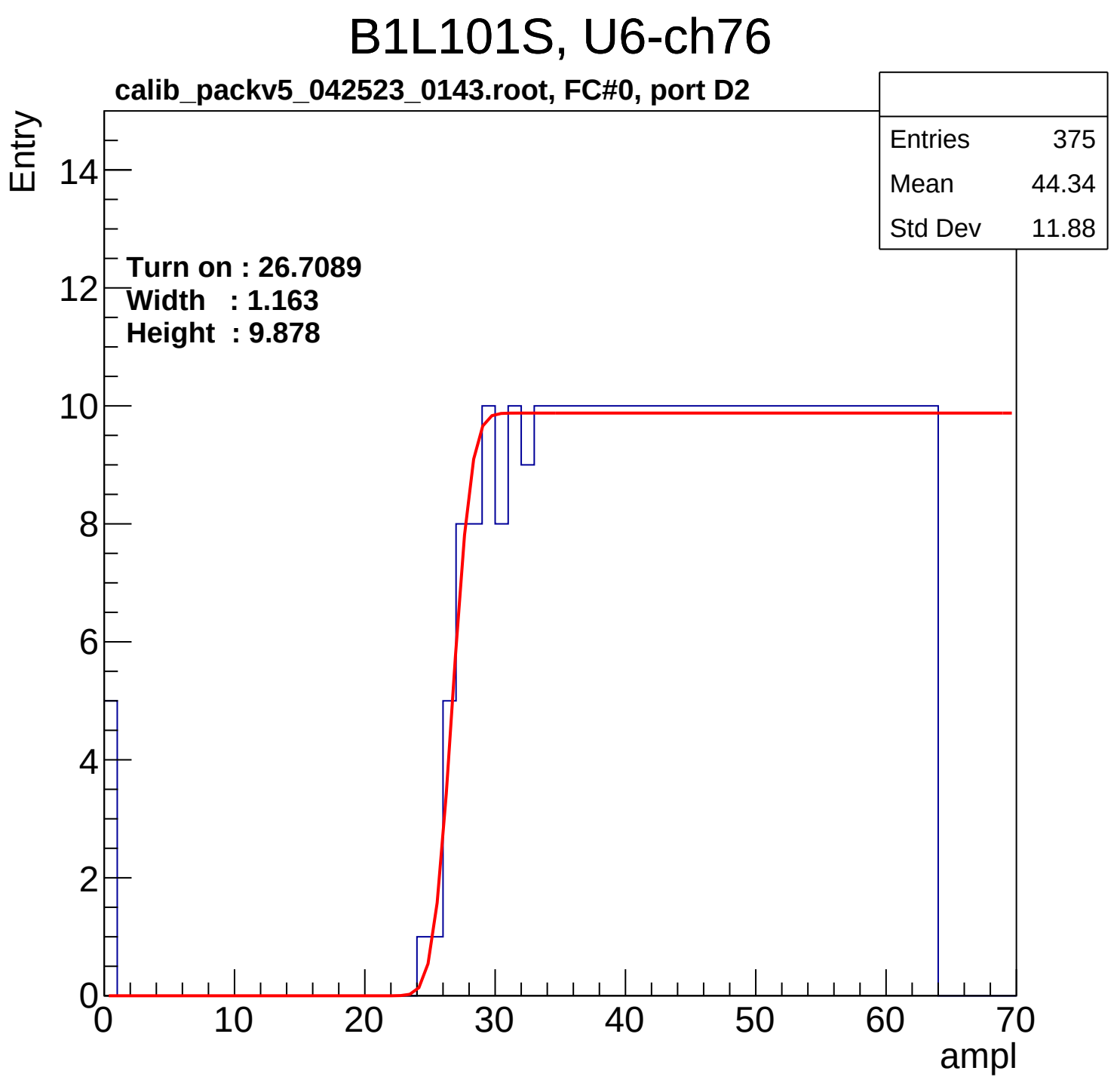

B1L101S, U6-ch71
calib_packv5_042523_0143.root, FC#0, port D2
Entries 363
Mean 45.13
Std Dev 11.03
Turn on : 28.2289
Width : 2.558
Height : 10.052
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

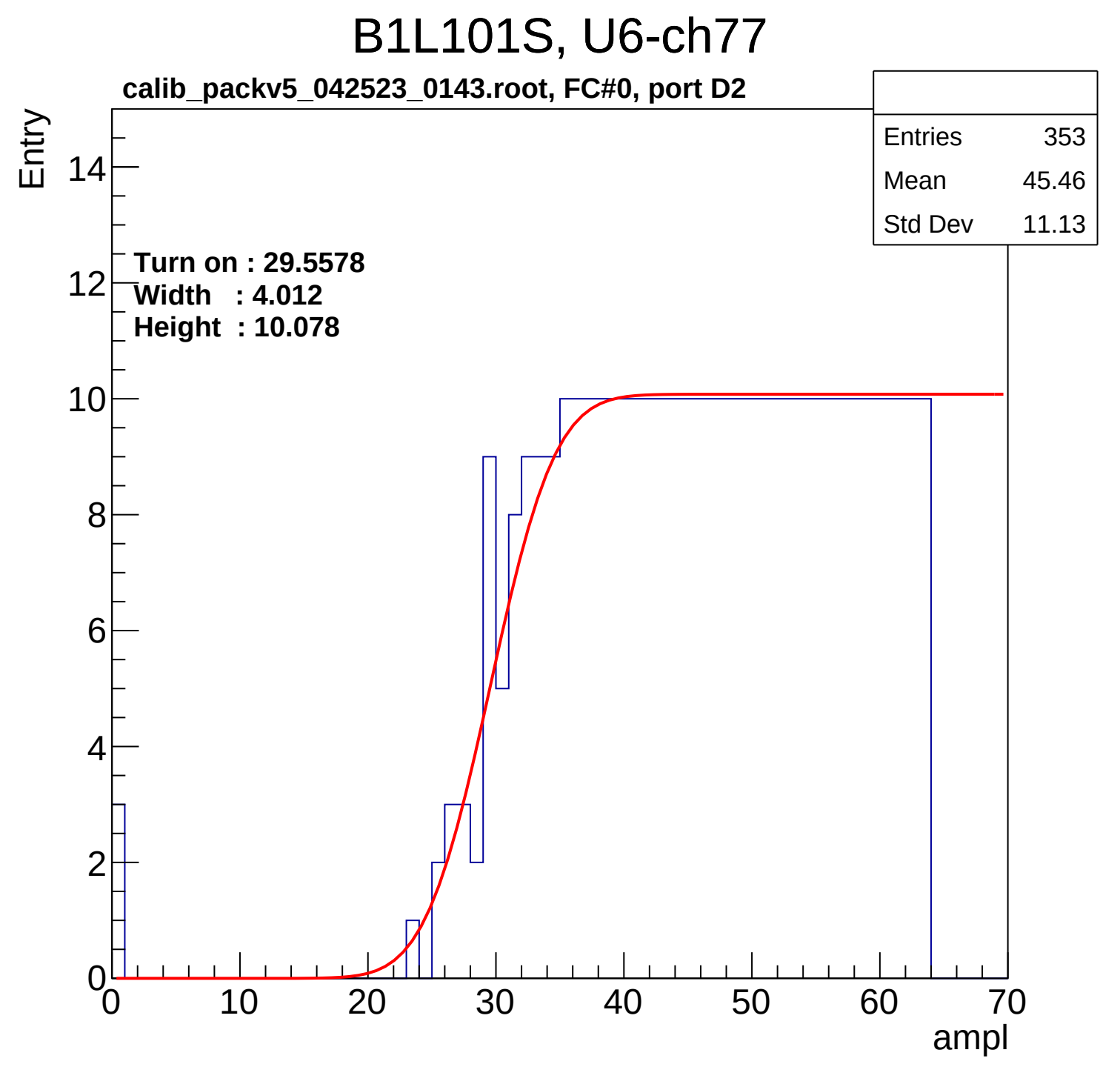

B1L101S, U6-ch72
calib_packv5_042523_0143.root, FC#0, port D2
Entries 374
Mean 44.59
Std Dev 11.32
Turn on : 26.6535
Width : 2.680
Height : 10.017
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

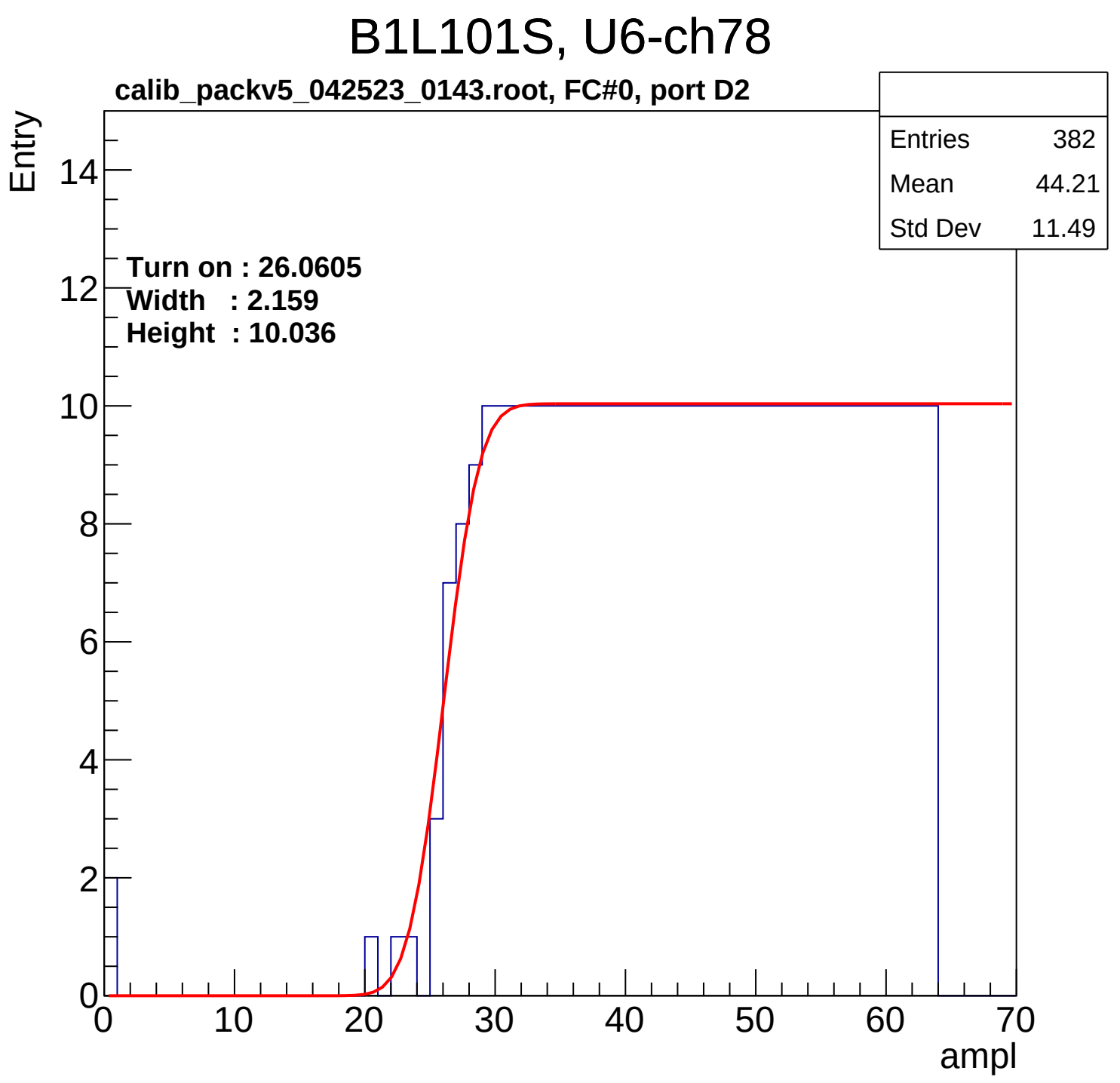

B1L101S, U6-ch73
calib_packv5_042523_0143.root, FC#0, port D2
Entries 365
Mean 44.96
Std Dev 11.2
Turn on : 28.1736
Width : 3.381
Height : 10.027
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

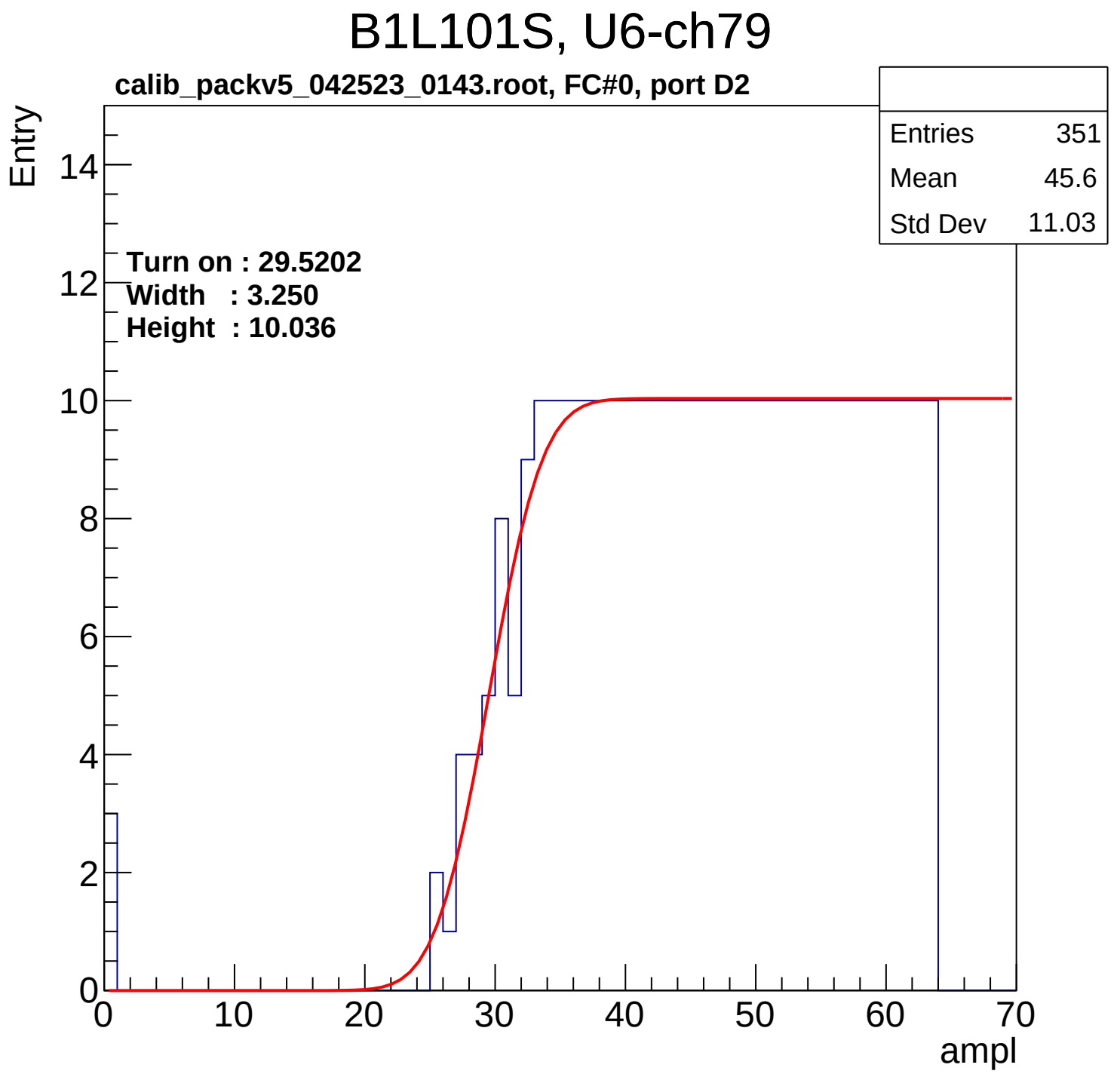

B1L101S, U6-ch74
calib_packv5_042523_0143.root, FC#0, port D2
Entries 388
Mean 43.84
Std Dev 11.84
Turn on : 25.5083
Width : 3.109
Height : 10.026
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

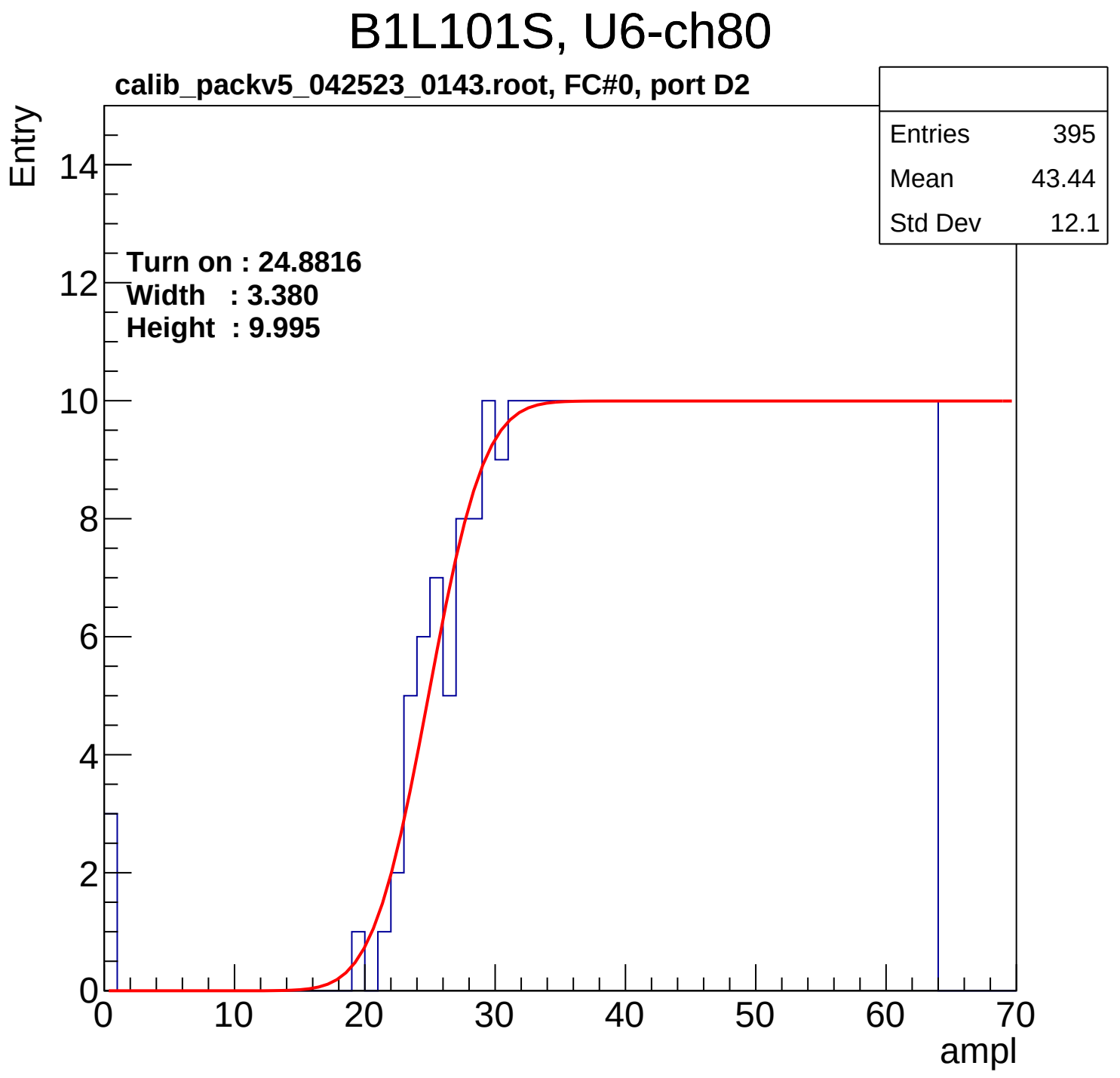

B1L101S, U6-ch75
calib_packv5_042523_0143.root, FC#0, port D2
Entries 368
Mean 44.93
Std Dev 10.99
Turn on : 27.6737
Width : 3.185
Height : 10.049
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

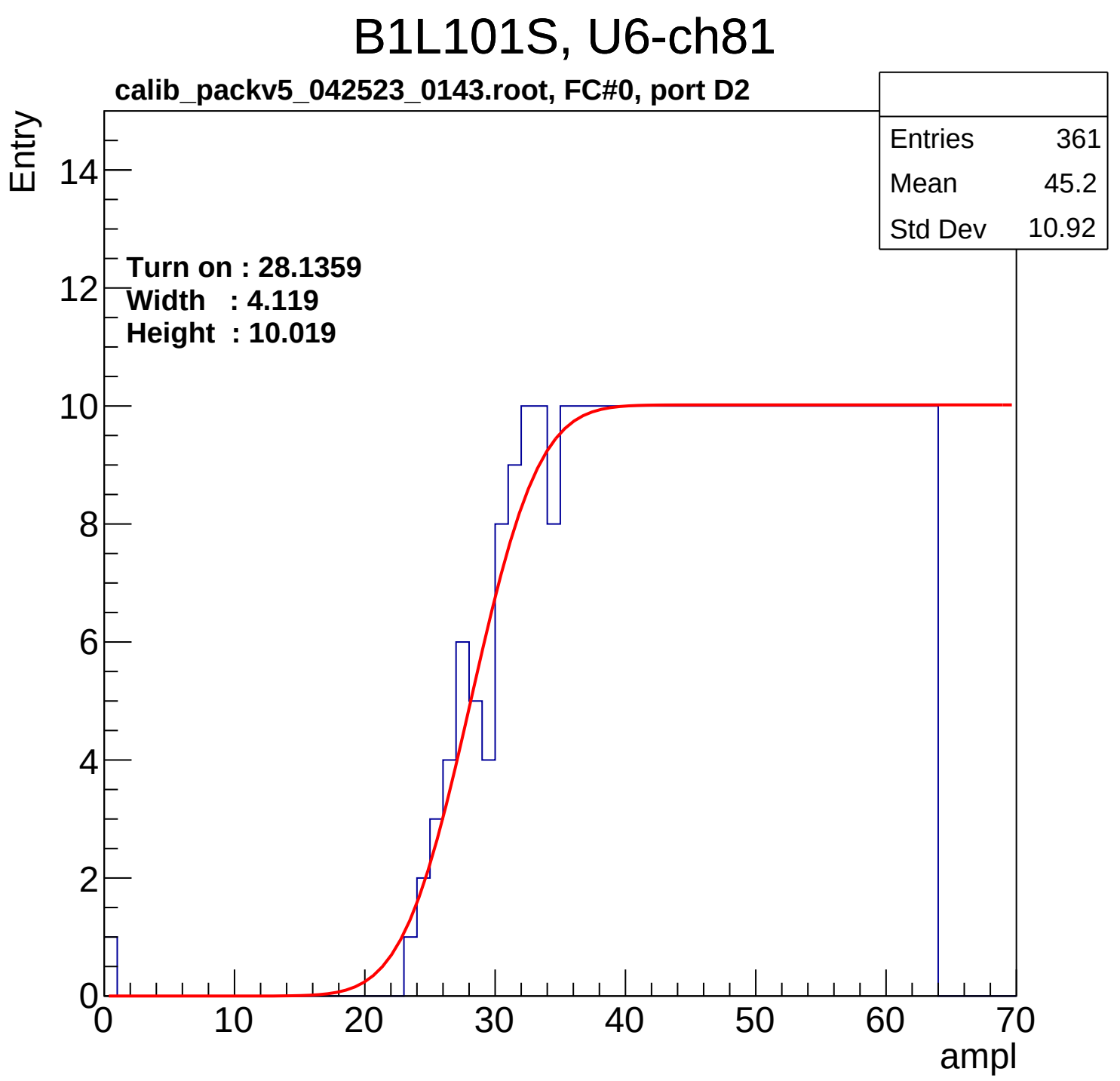

B1L101S, U6-ch76
calib_packv5_042523_0143.root, FC#0, port D2
Entries 375
Mean 44.34
Std Dev 11.88
Turn on : 26.7089
Width : 1.163
Height : 9.878
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

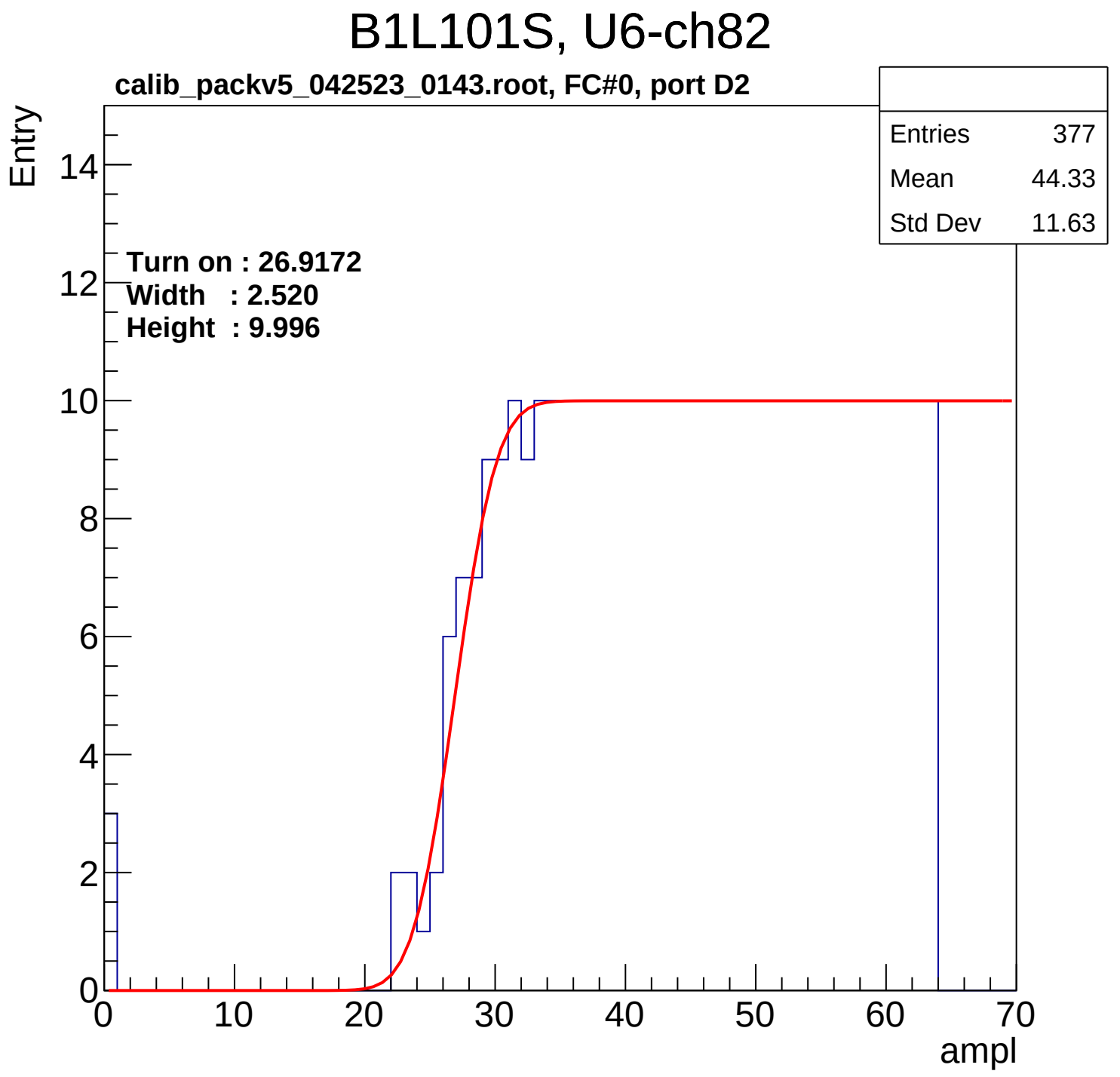

B1L101S, U6-ch77
calib_packv5_042523_0143.root, FC#0, port D2
Entries 353
Mean 45.46
Std Dev 11.13
Turn on : 29.5578
Width : 4.012
Height : 10.078
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

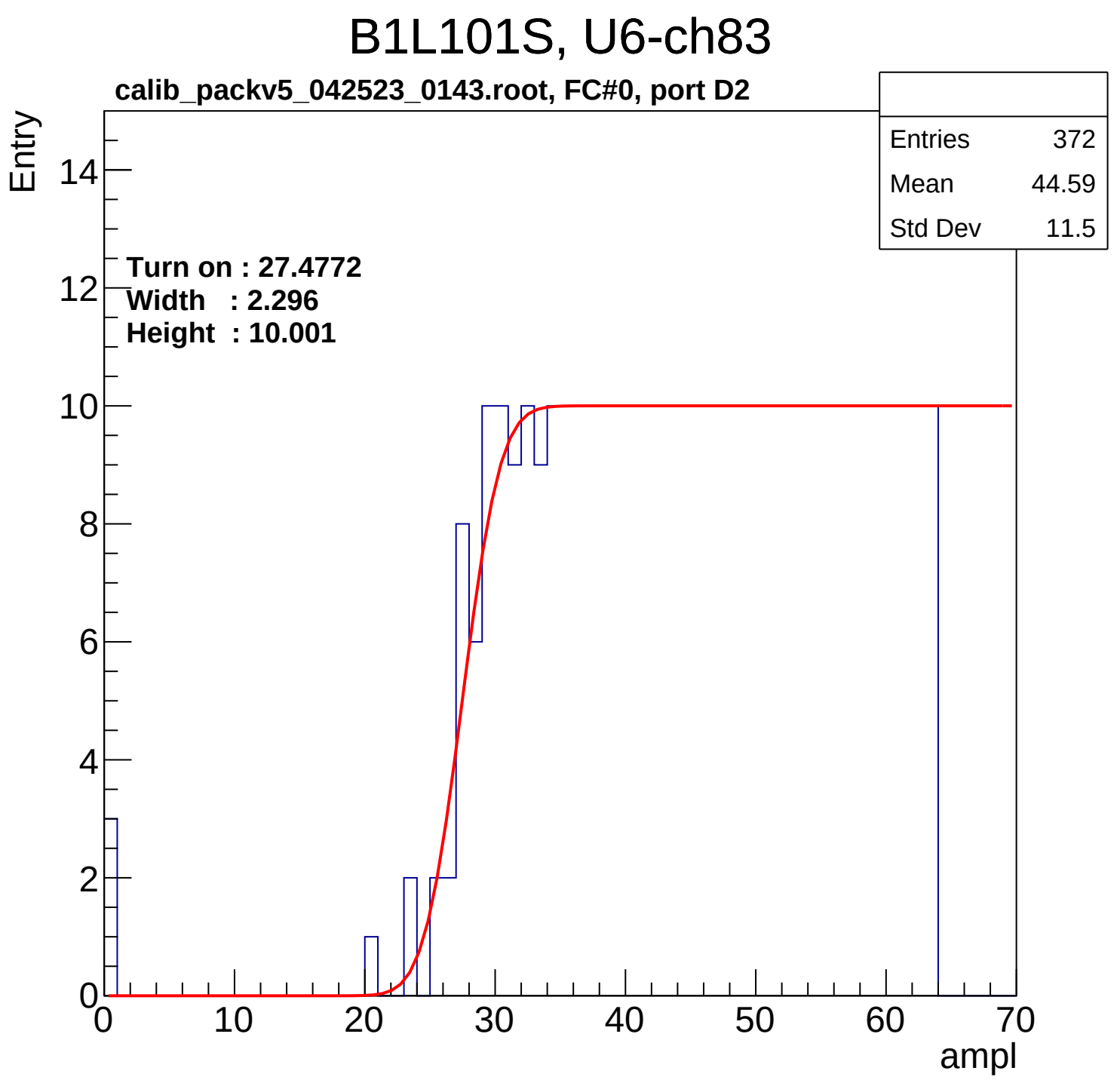

B1L101S, U6-ch78
calib_packv5_042523_0143.root, FC#0, port D2
Entries 382
Mean 44.21
Std Dev 11.49
Turn on : 26.0605
Width : 2.159
Height : 10.036
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

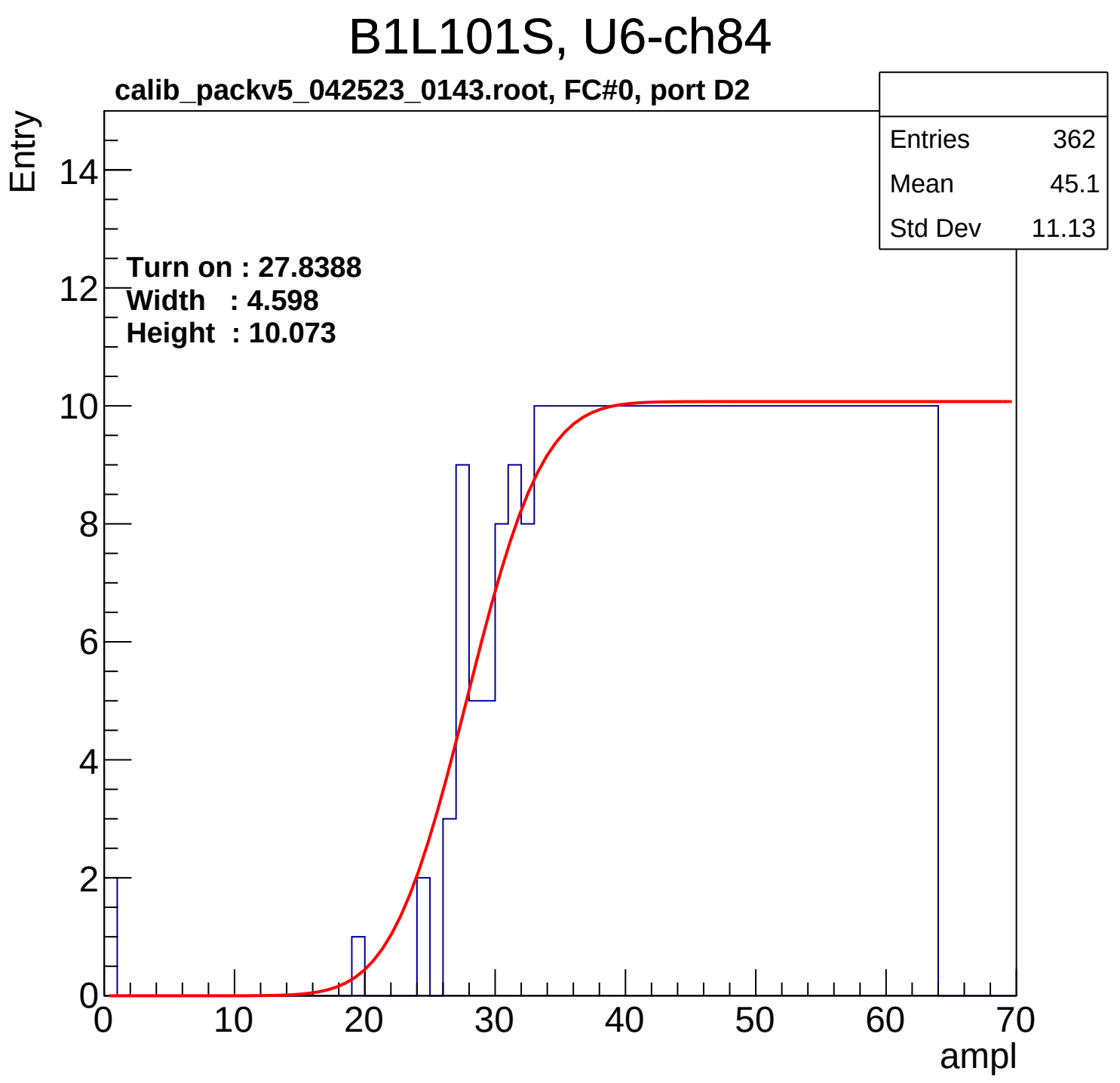

B1L101S, U6-ch79
calib_packv5_042523_0143.root, FC#0, port D2
Entries 351
Mean 45.6
Std Dev 11.03
Turn on : 29.5202
Width : 3.250
Height : 10.036
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

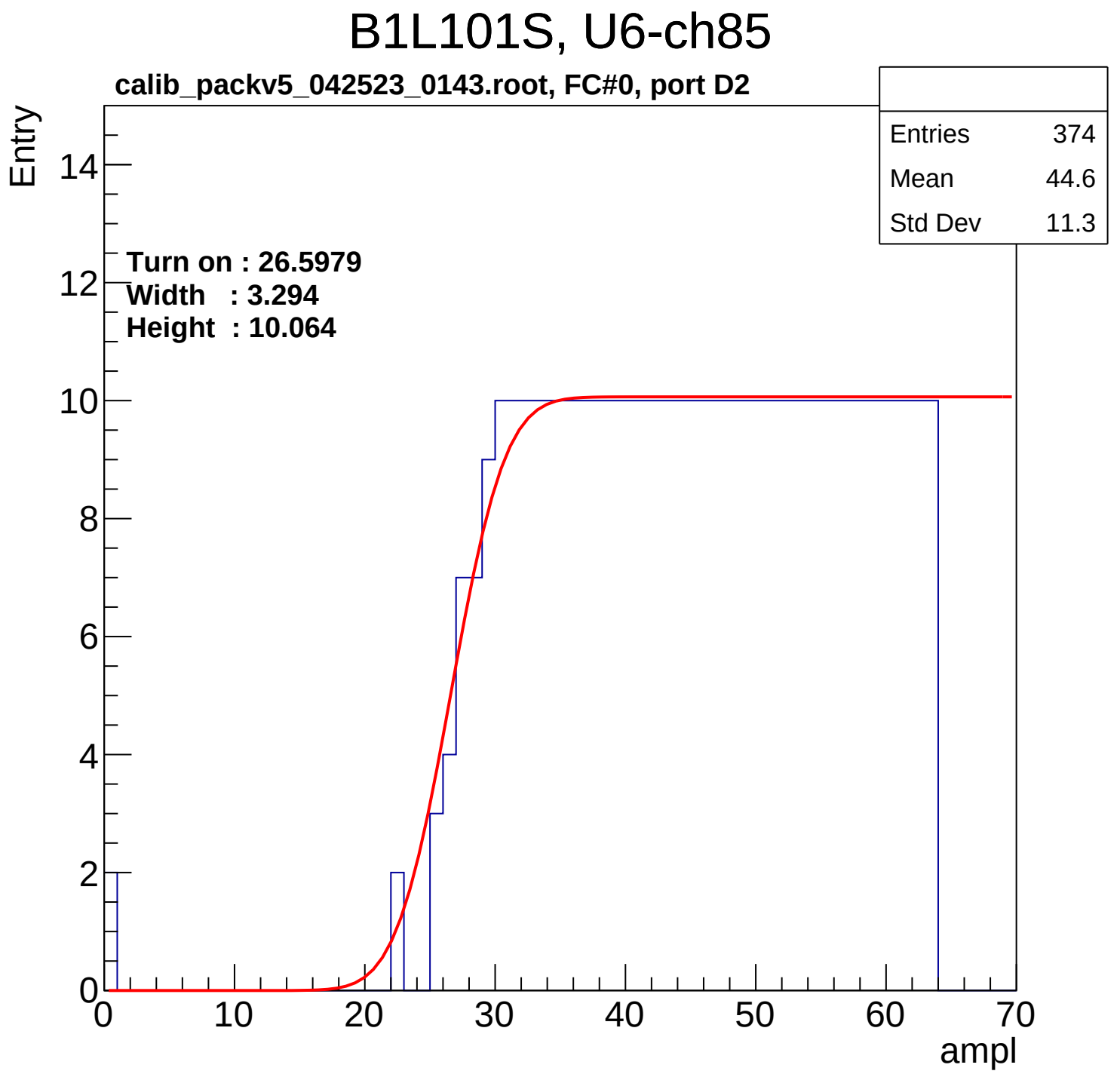

B1L101S, U6-ch80
calib_packv5_042523_0143.root, FC#0, port D2
Entries 395
Mean 43.44
Std Dev 12.1
Turn on : 24.8816
Width : 3.380
Height : 9.995
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

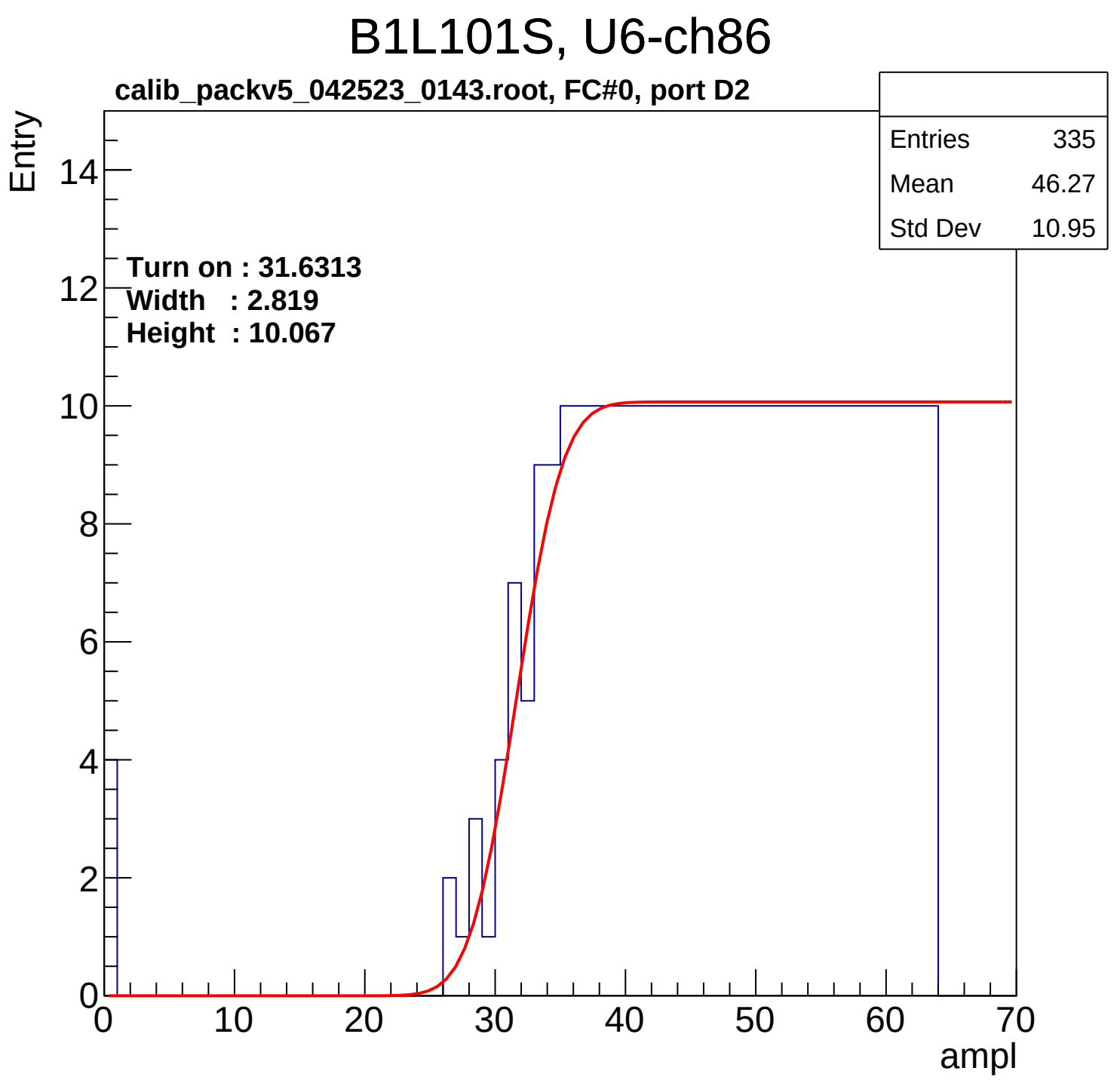

B1L101S, U6-ch81
calib_packv5_042523_0143.root, FC#0, port D2
Entries 361
Mean 45.2
Std Dev 10.92
Turn on : 28.1359
Width : 4.119
Height : 10.019
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

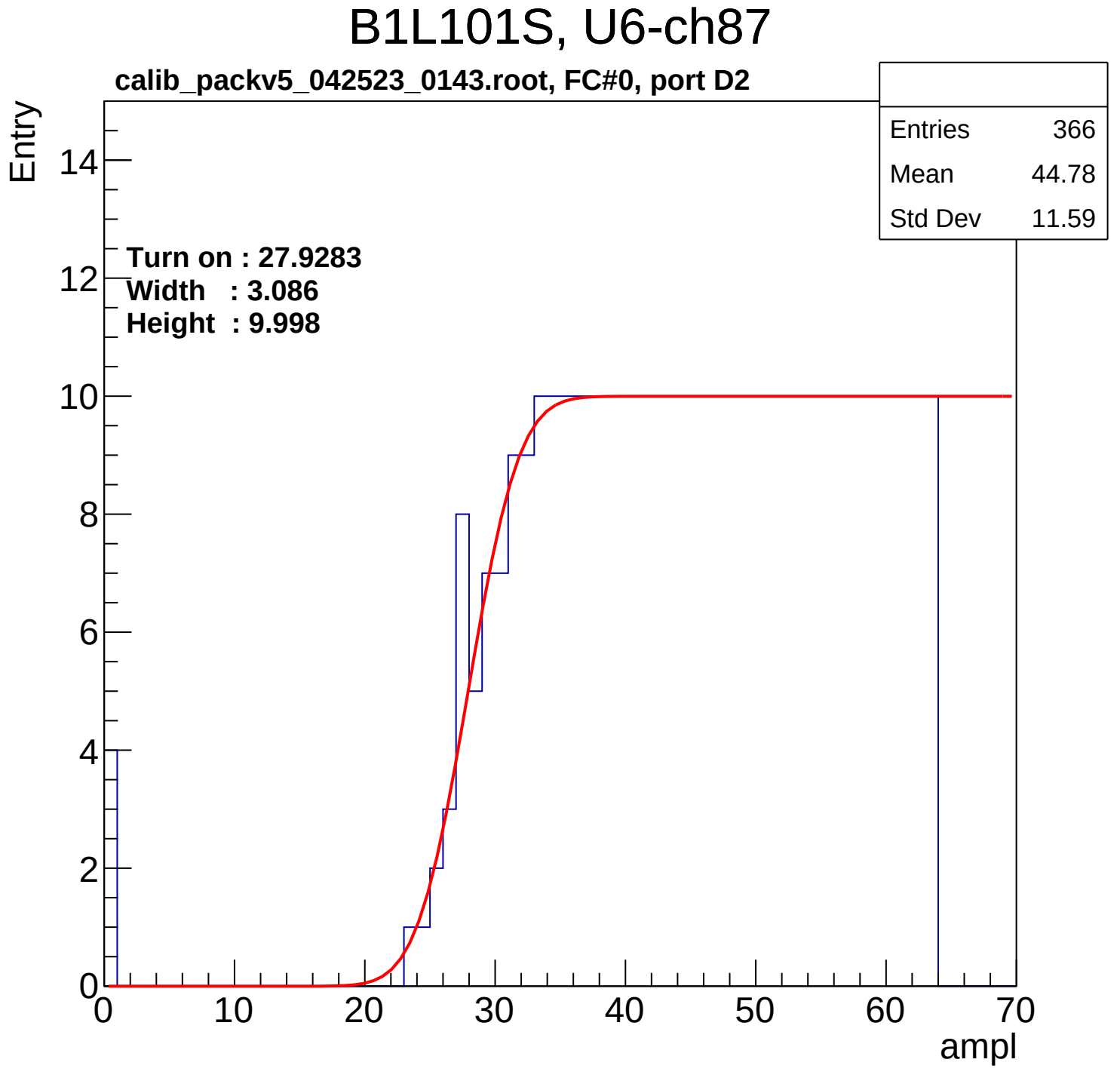

B1L101S, U6-ch82
calib_packv5_042523_0143.root, FC#0, port D2
Entries 377
Mean 44.33
Std Dev 11.63
Turn on : 26.9172
Width : 2.520
Height : 9.996
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

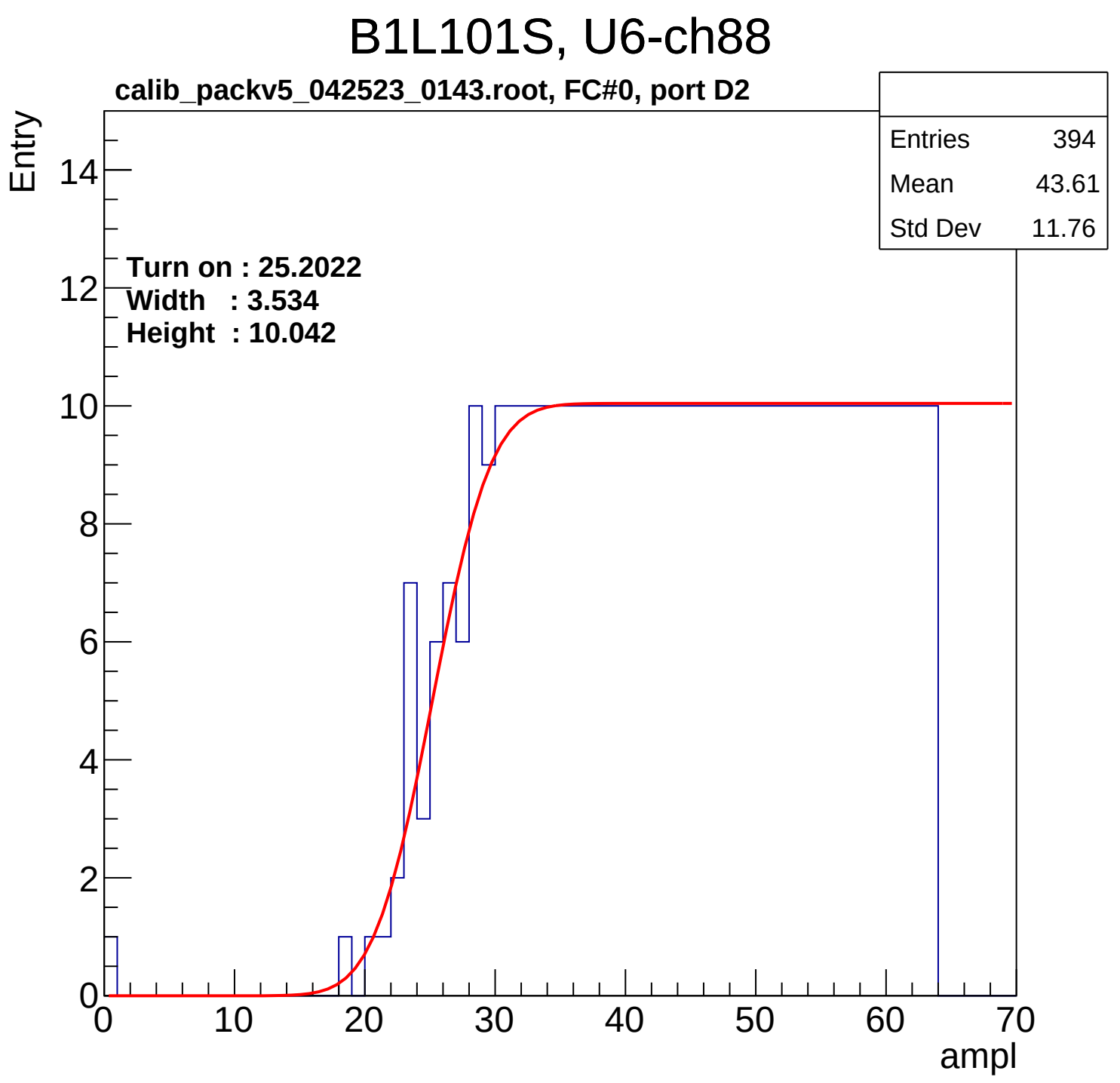

B1L101S, U6-ch83
calib_packv5_042523_0143.root, FC#0, port D2
Entries 372
Mean 44.59
Std Dev 11.5
Turn on : 27.4772
Width : 2.296
Height : 10.001
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

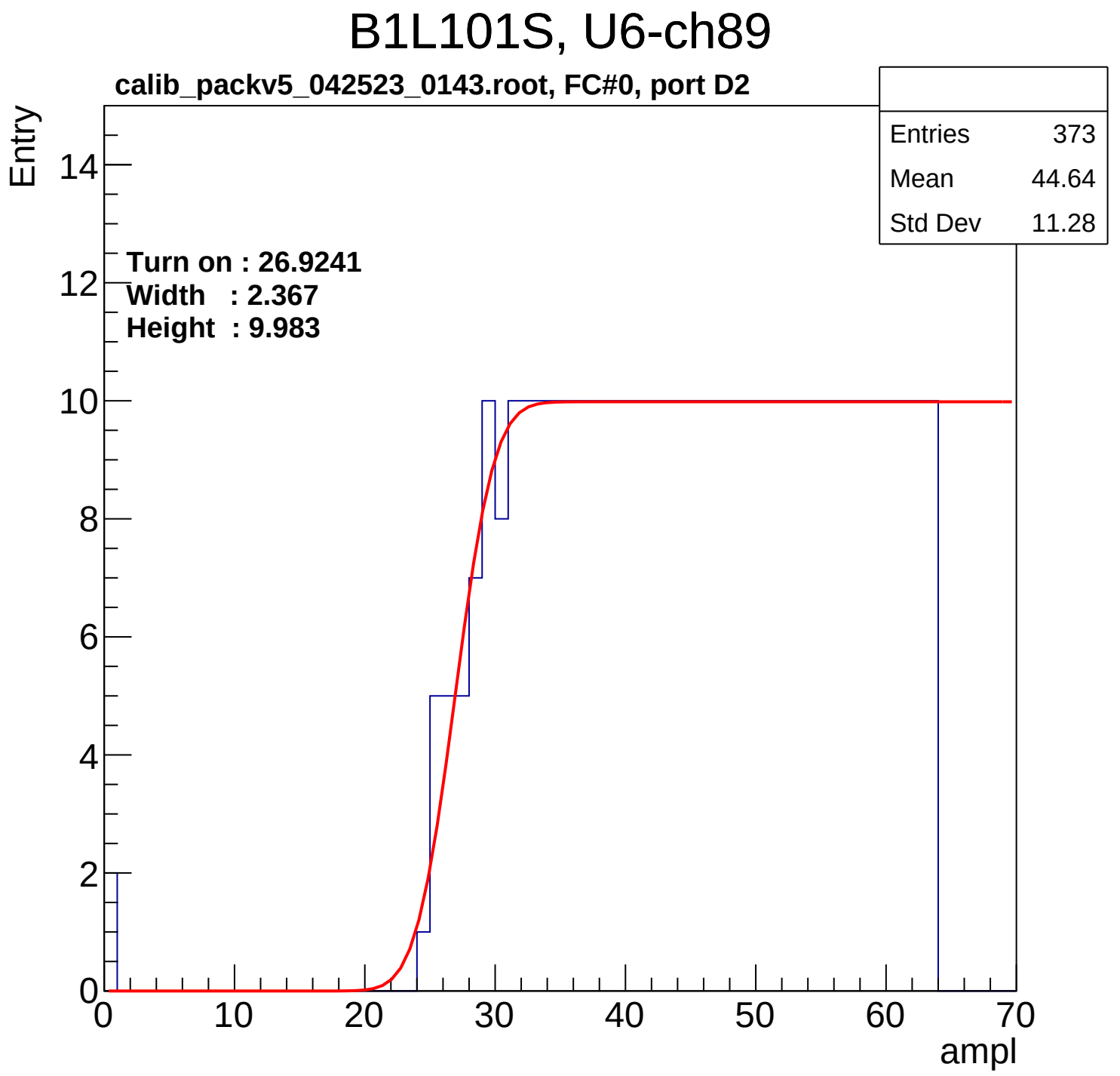

B1L101S, U6-ch84
calib_packv5_042523_0143.root, FC#0, port D2
Entries 362
Mean 45.1
Std Dev 11.13
Turn on : 27.8388
Width : 4.598
Height : 10.073
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

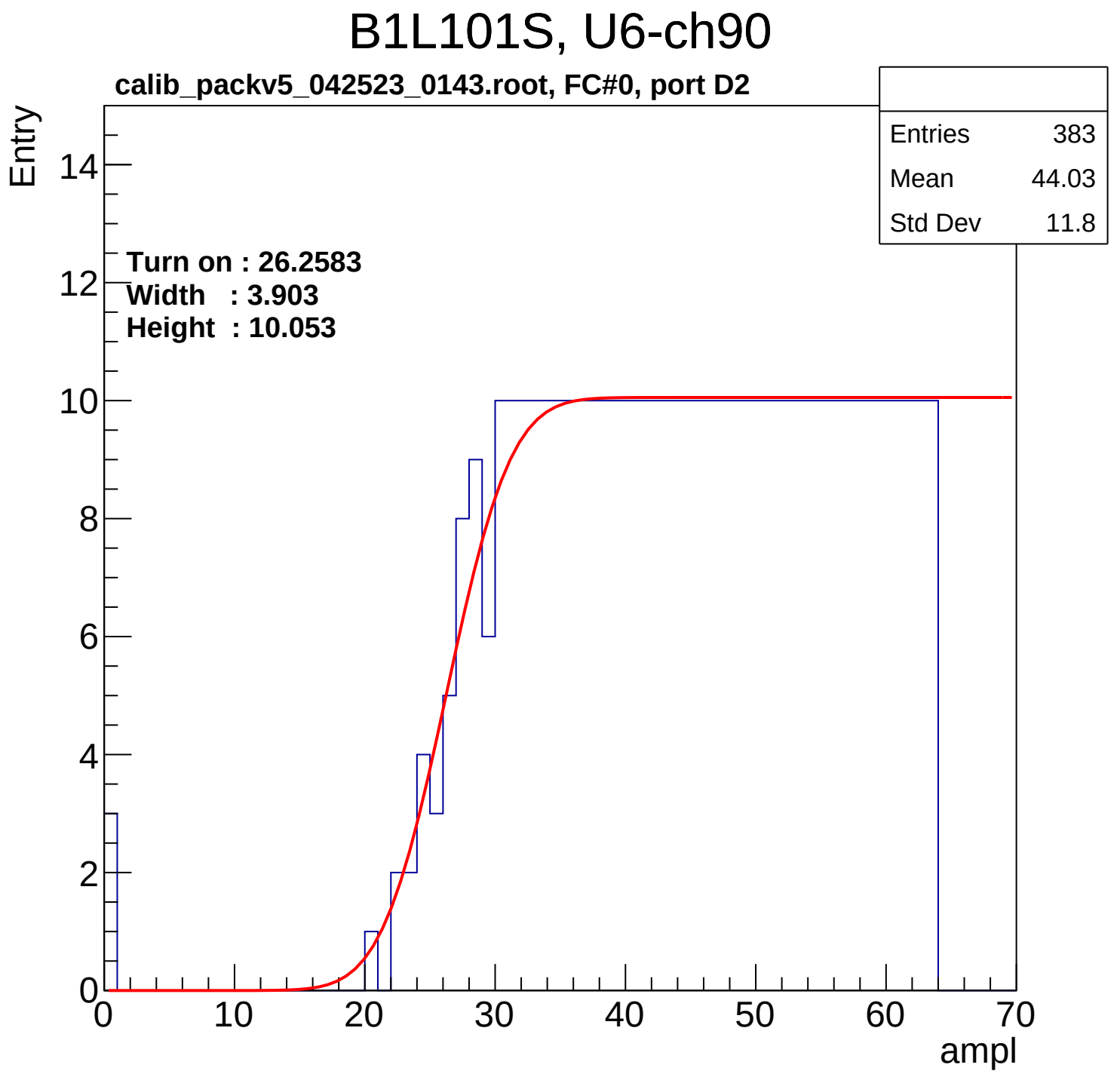

B1L101S, U6-ch85
calib_packv5_042523_0143.root, FC#0, port D2
Entries 374
Mean 44.6
Std Dev 11.3
Turn on : 26.5979
Width : 3.294
Height : 10.064
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

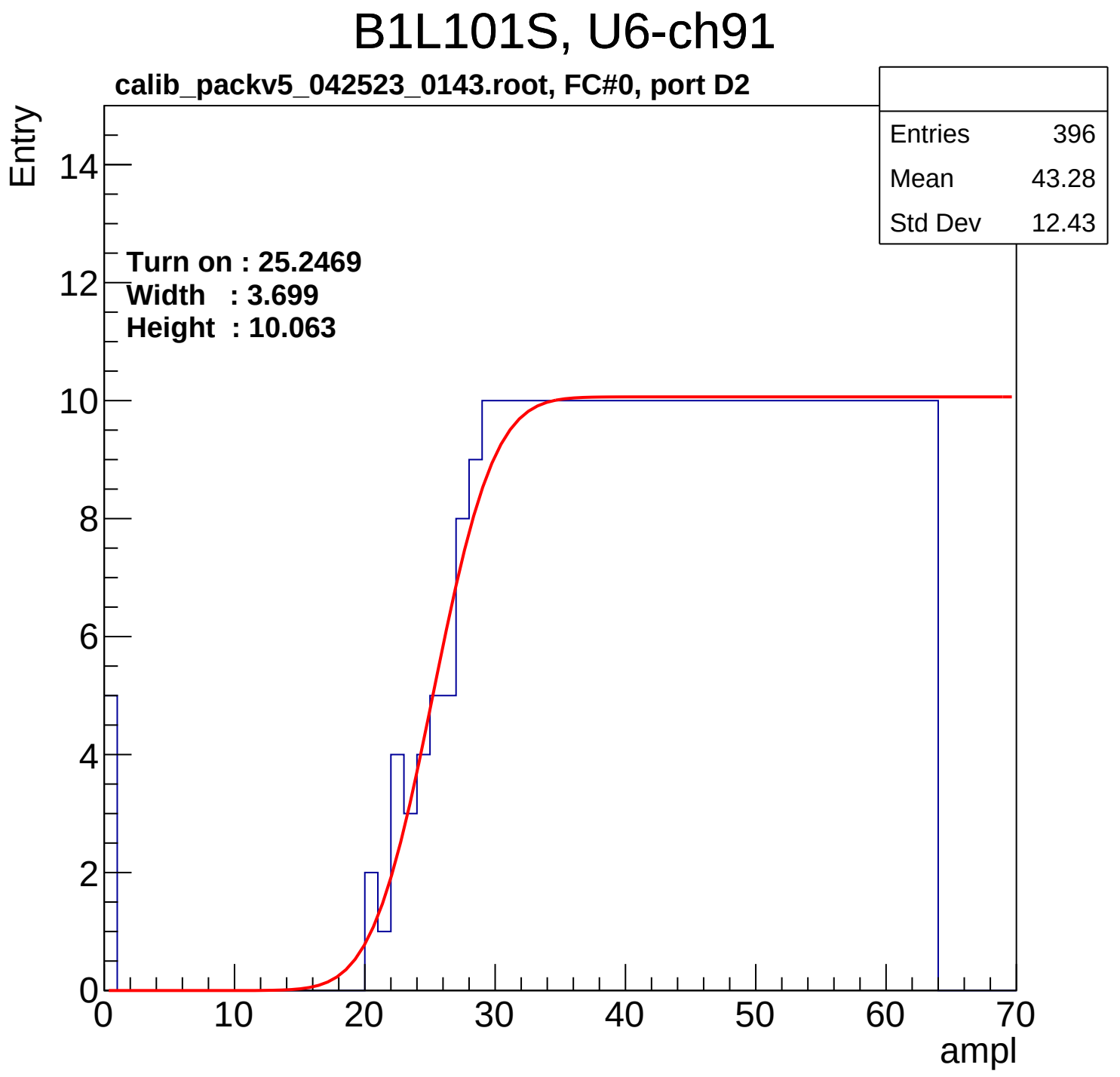

B1L101S, U6-ch86
calib_packv5_042523_0143.root, FC#0, port D2
Entries 335
Mean 46.27
Std Dev 10.95
Turn on : 31.6313
Width : 2.819
Height : 10.067
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

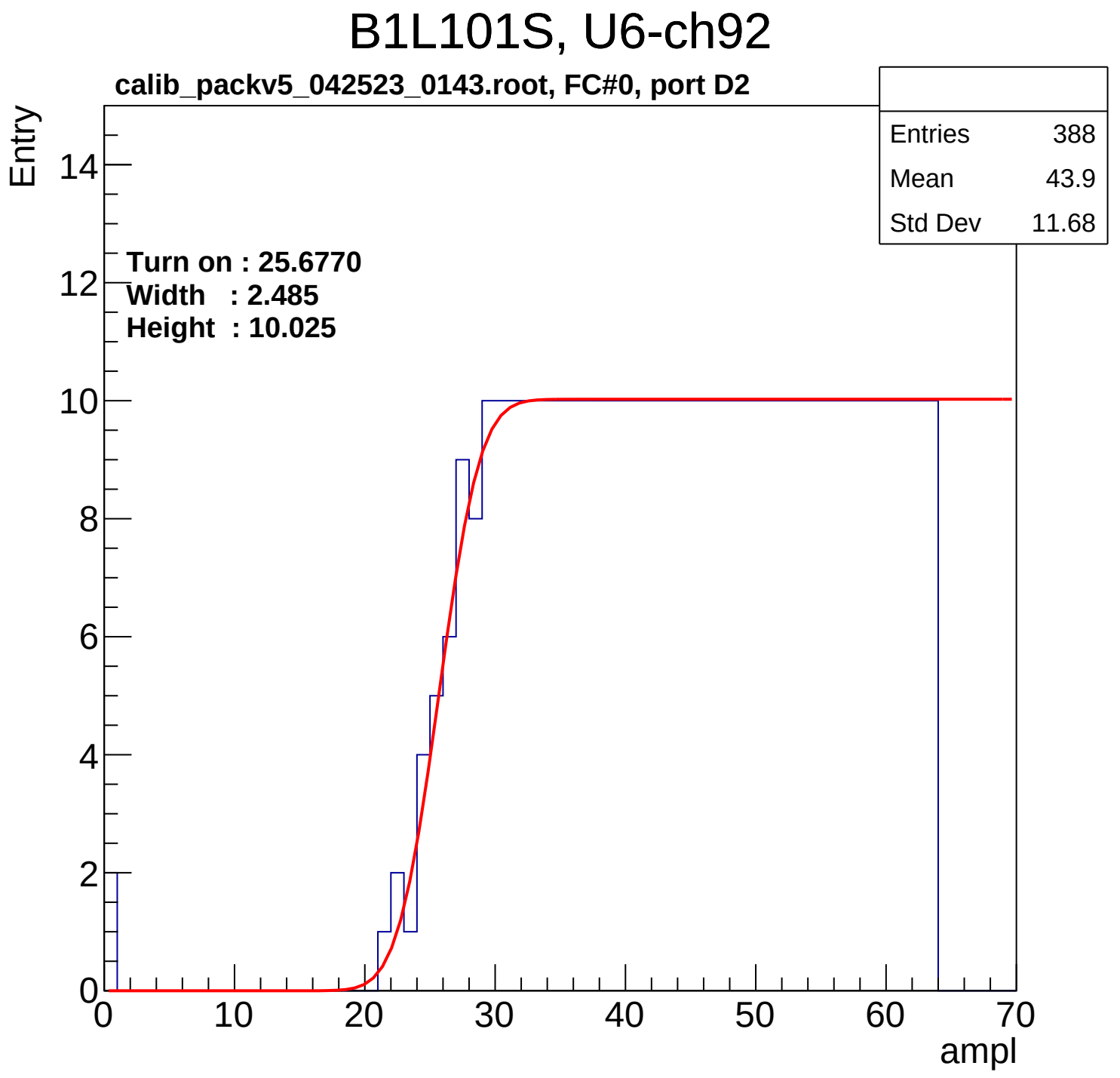

B1L101S, U6-ch87
calib_packv5_042523_0143.root, FC#0, port D2
Entries 366
Mean 44.78
Std Dev 11.59
Turn on : 27.9283
Width : 3.086
Height : 9.998
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

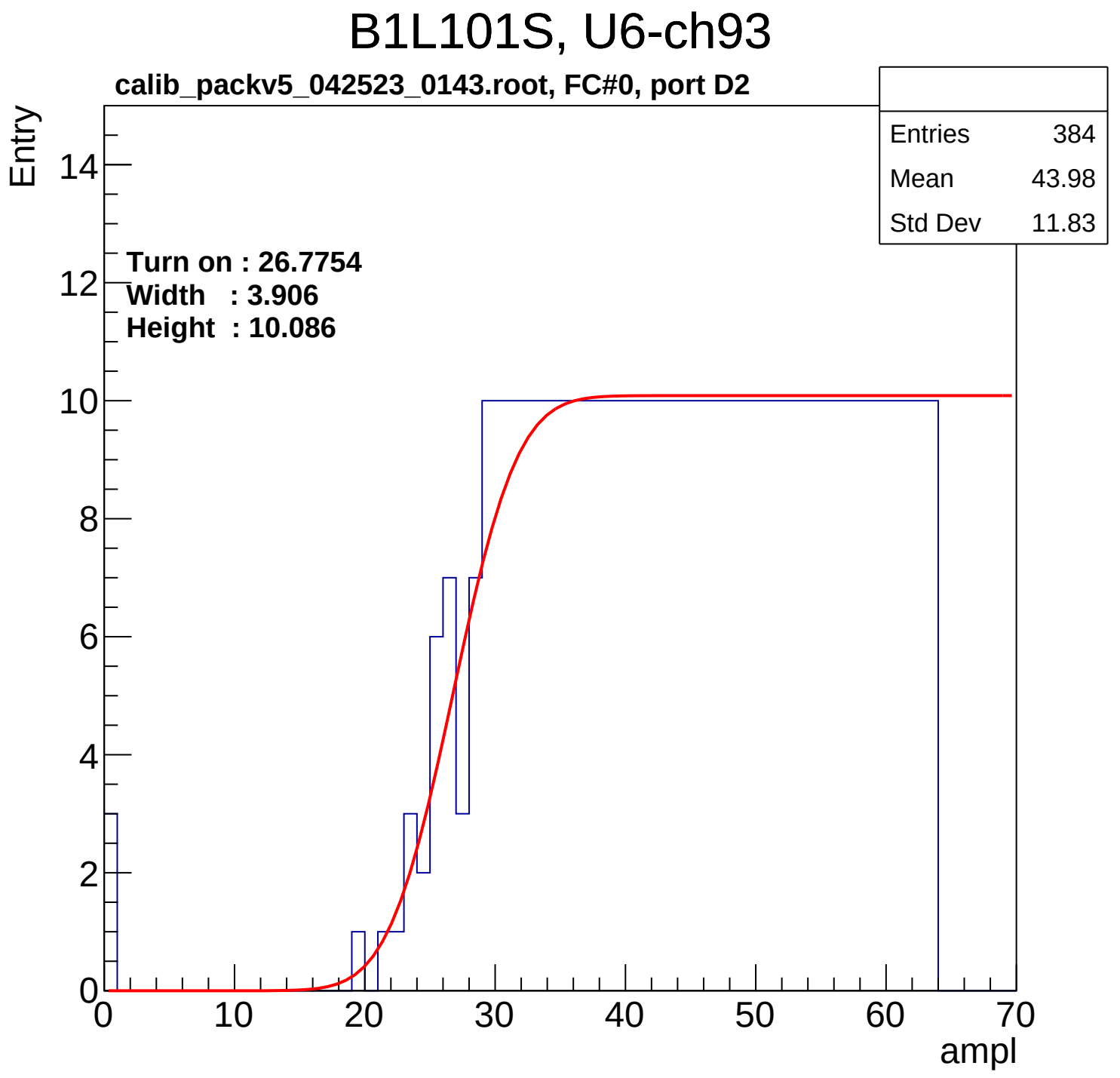

B1L101S, U6-ch88
calib_packv5_042523_0143.root, FC#0, port D2
Entries 394
Mean 43.61
Std Dev 11.76
Turn on : 25.2022
Width : 3.534
Height : 10.042
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

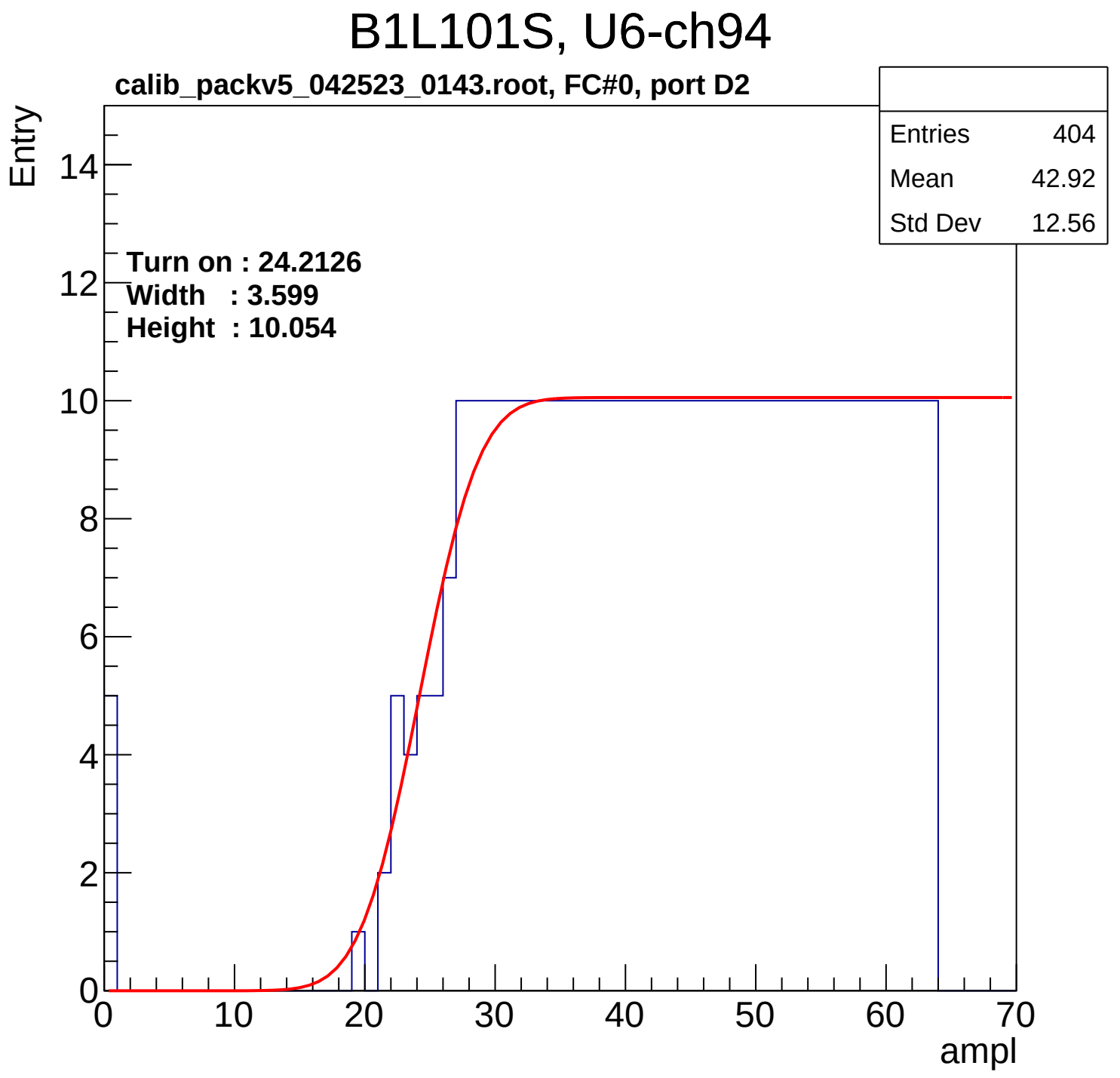

B1L101S, U6-ch89
calib_packv5_042523_0143.root, FC#0, port D2
Entries 373
Mean 44.64
Std Dev 11.28
Turn on : 26.9241
Width : 2.367
Height : 9.983
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

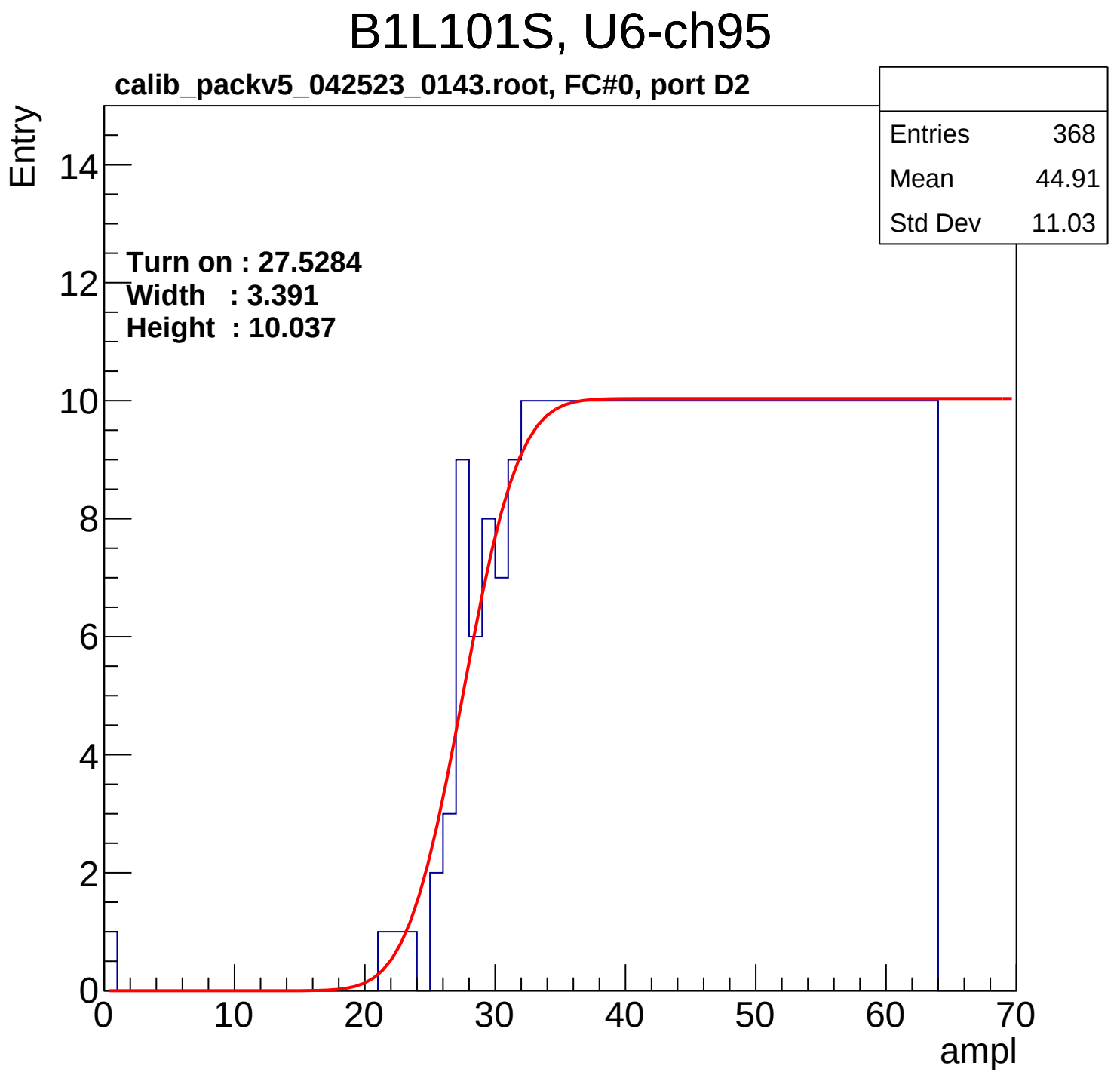

B1L101S, U6-ch90
calib_packv5_042523_0143.root, FC#0, port D2
Entries 383
Mean 44.03
Std Dev 11.8
Turn on : 26.2583
Width : 3.903
Height : 10.053
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

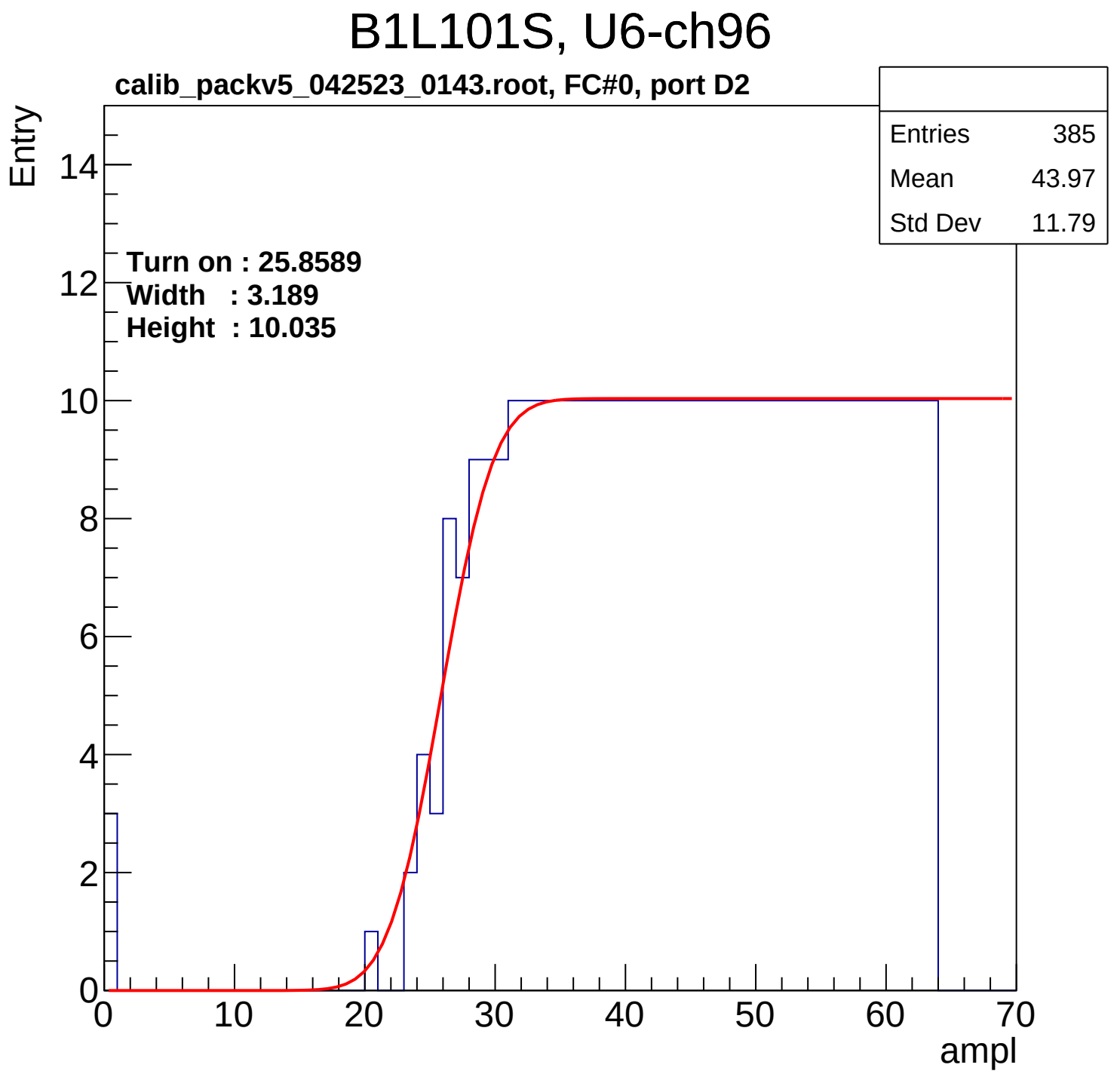

B1L101S, U6-ch91
calib_packv5_042523_0143.root, FC#0, port D2
Entries 396
Mean 43.28
Std Dev 12.43
Turn on : 25.2469
Width : 3.699
Height : 10.063
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

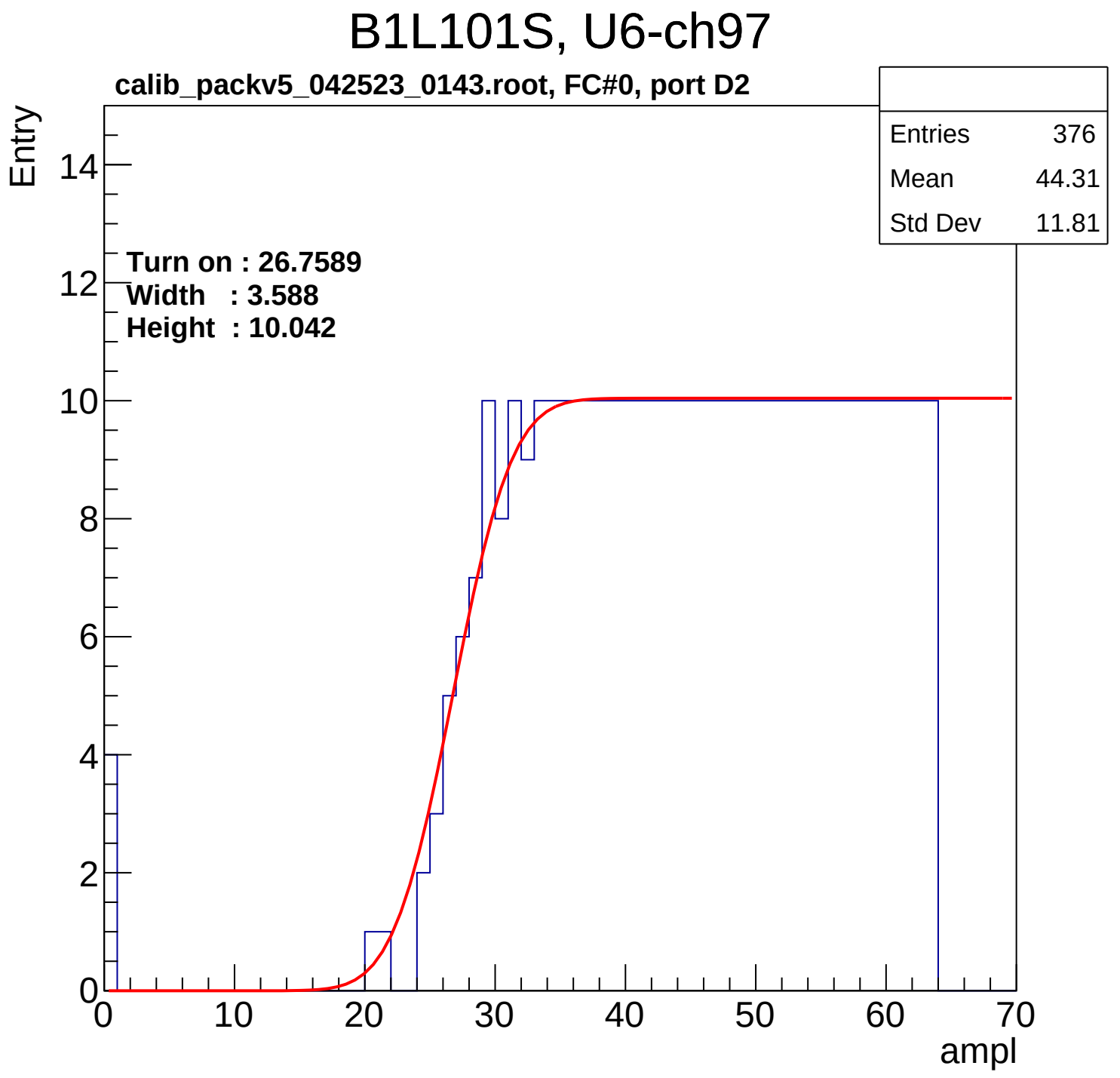

B1L101S, U6-ch92
calib_packv5_042523_0143.root, FC#0, port D2
Entries 388
Mean 43.9
Std Dev 11.68
Turn on : 25.6770
Width : 2.485
Height : 10.025
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

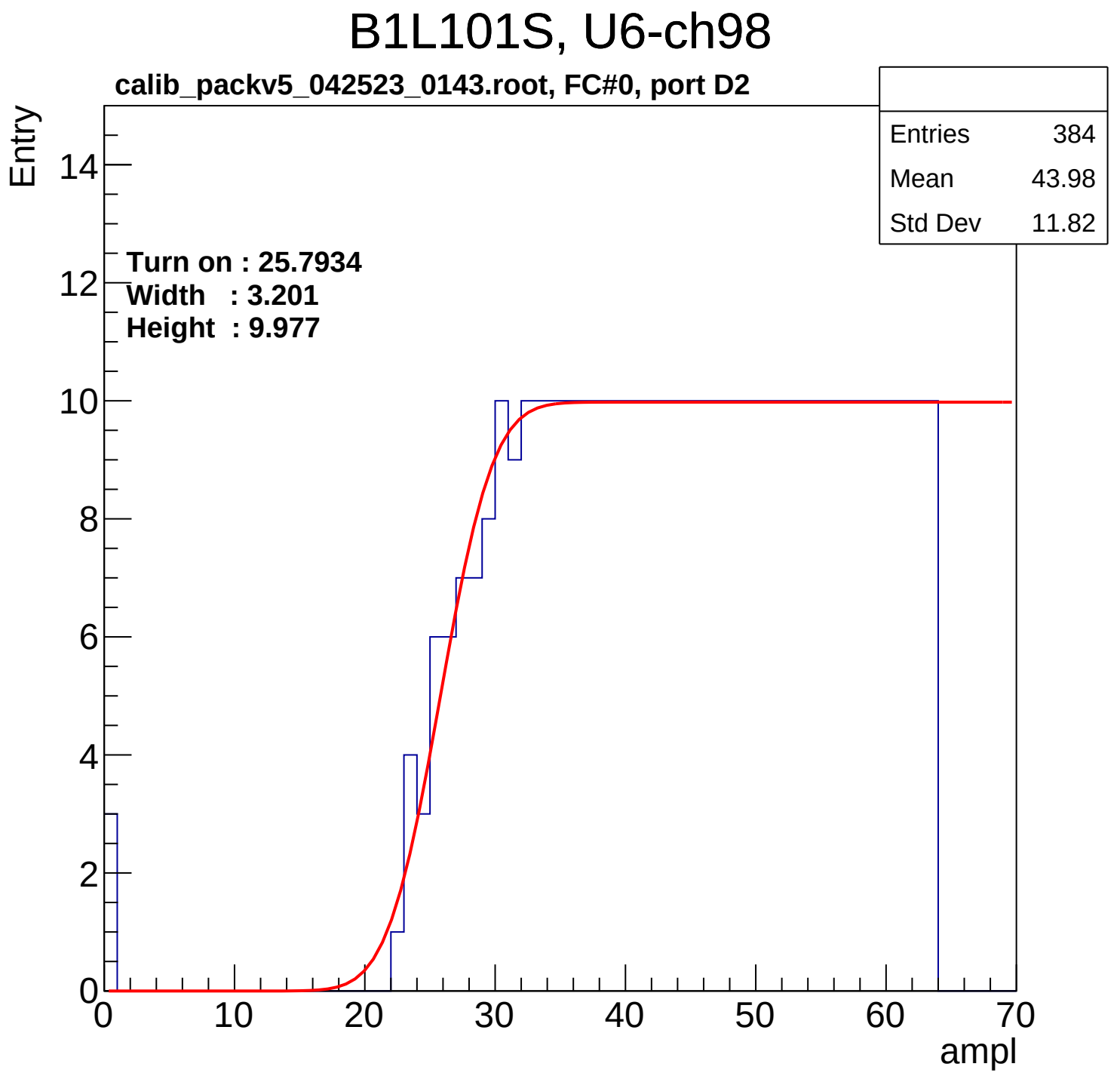

B1L101S, U6-ch93
calib_packv5_042523_0143.root, FC#0, port D2
Entries 384
Mean 43.98
Std Dev 11.83
Turn on : 26.7754
Width : 3.906
Height : 10.086
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

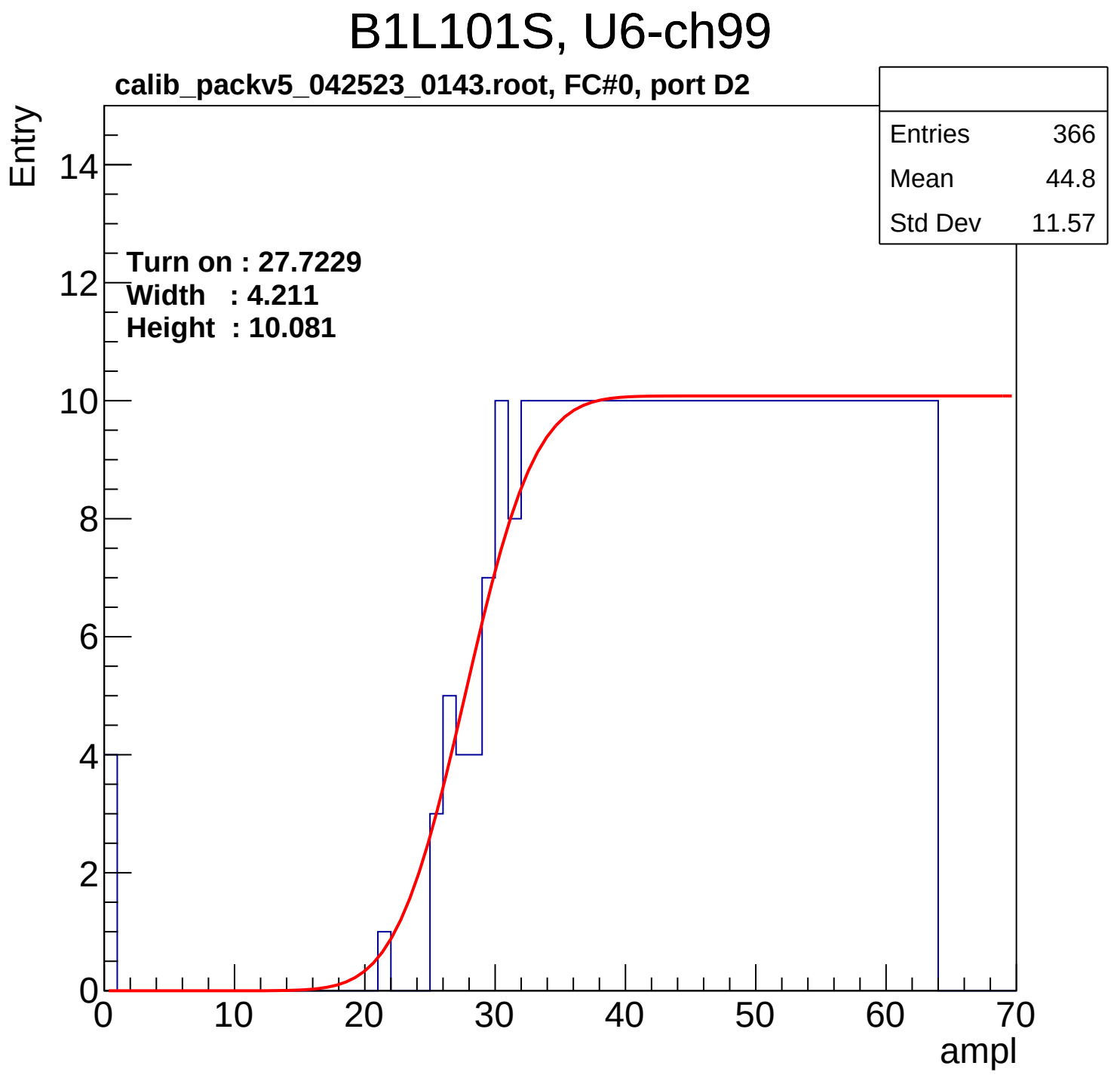

B1L101S, U6-ch94
calib_packv5_042523_0143.root, FC#0, port D2
Entries 404
Mean 42.92
Std Dev 12.56
Turn on : 24.2126
Width : 3.599
Height : 10.054
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

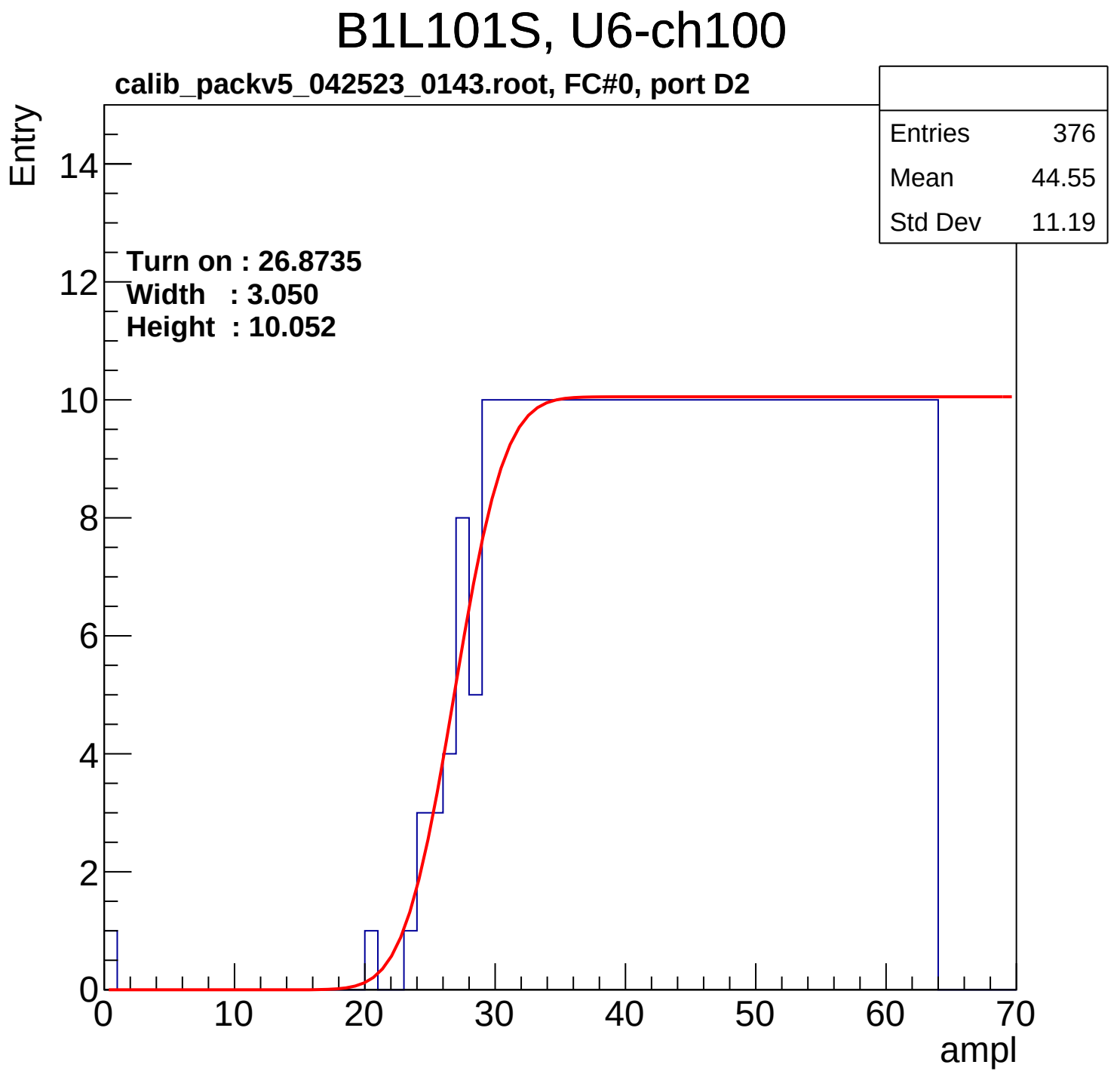

B1L101S, U6-ch95
calib_packv5_042523_0143.root, FC#0, port D2
Entries 368
Mean 44.91
Std Dev 11.03
Turn on : 27.5284
Width : 3.391
Height : 10.037
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

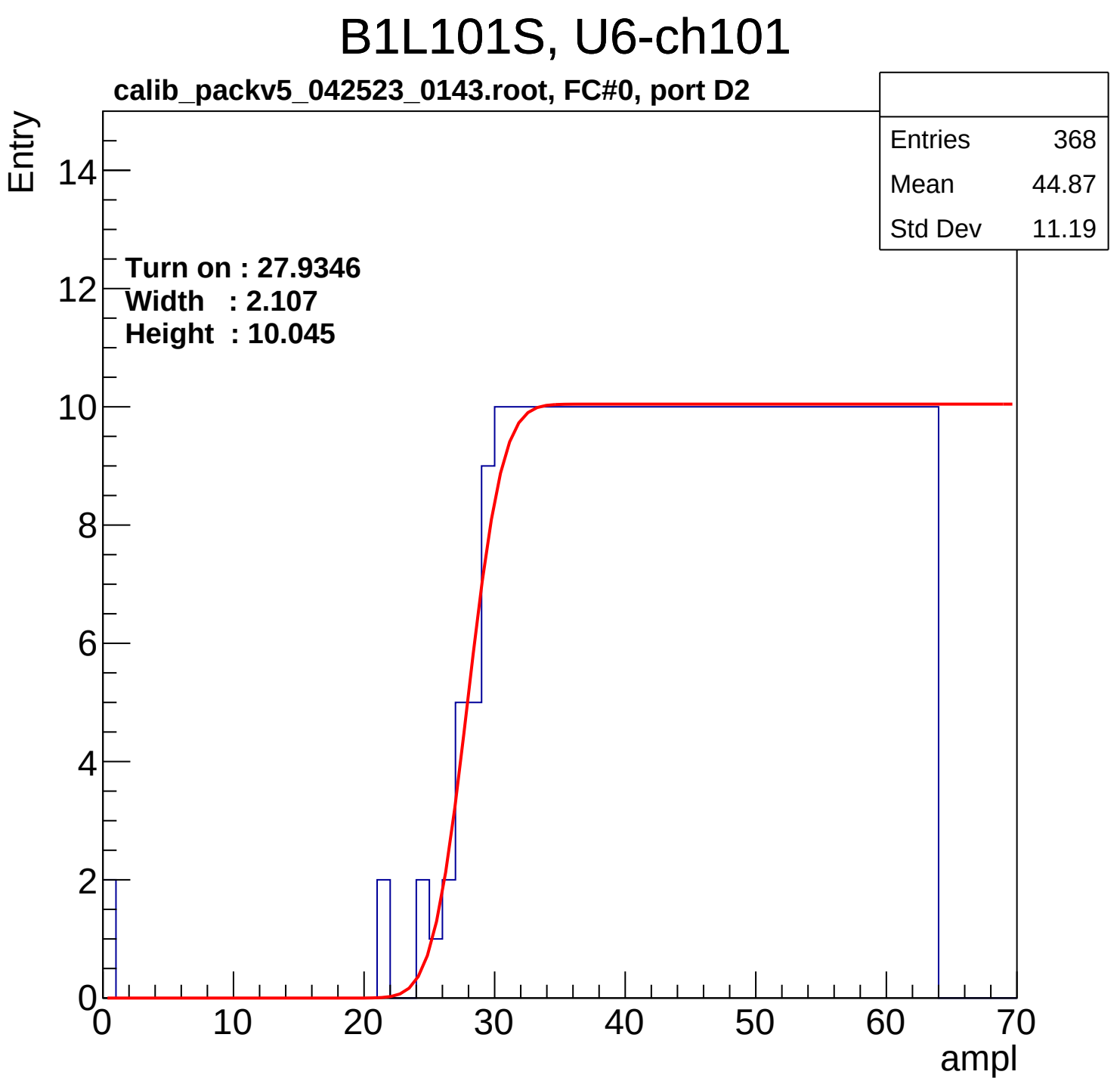

B1L101S, U6-ch96
calib_packv5_042523_0143.root, FC#0, port D2
Entries 385
Mean 43.97
Std Dev 11.79
Turn on : 25.8589
Width : 3.189
Height : 10.035
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

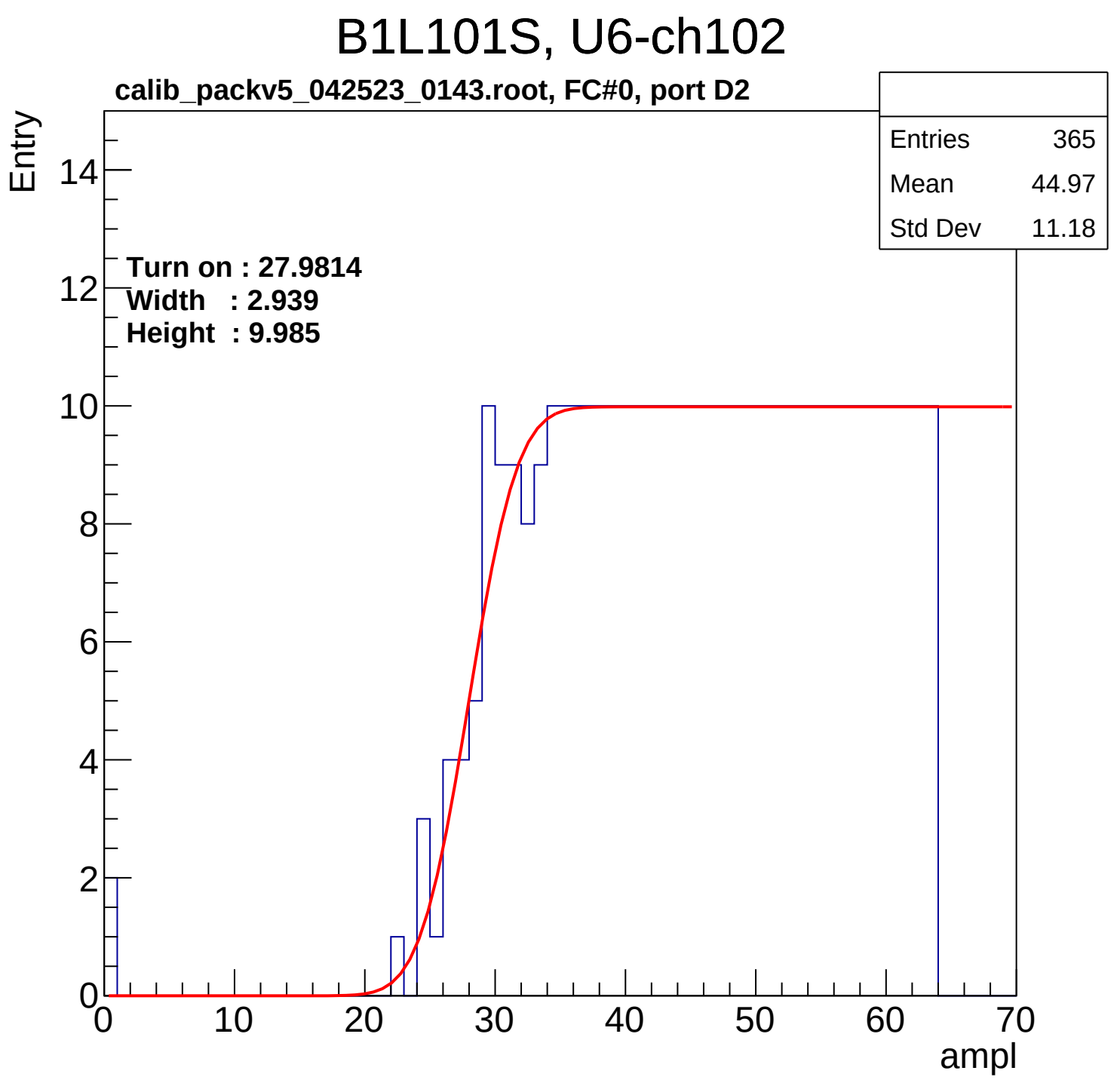

B1L101S, U6-ch97
calib_packv5_042523_0143.root, FC#0, port D2
Entries 376
Mean 44.31
Std Dev 11.81
Turn on : 26.7589
Width : 3.588
Height : 10.042
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

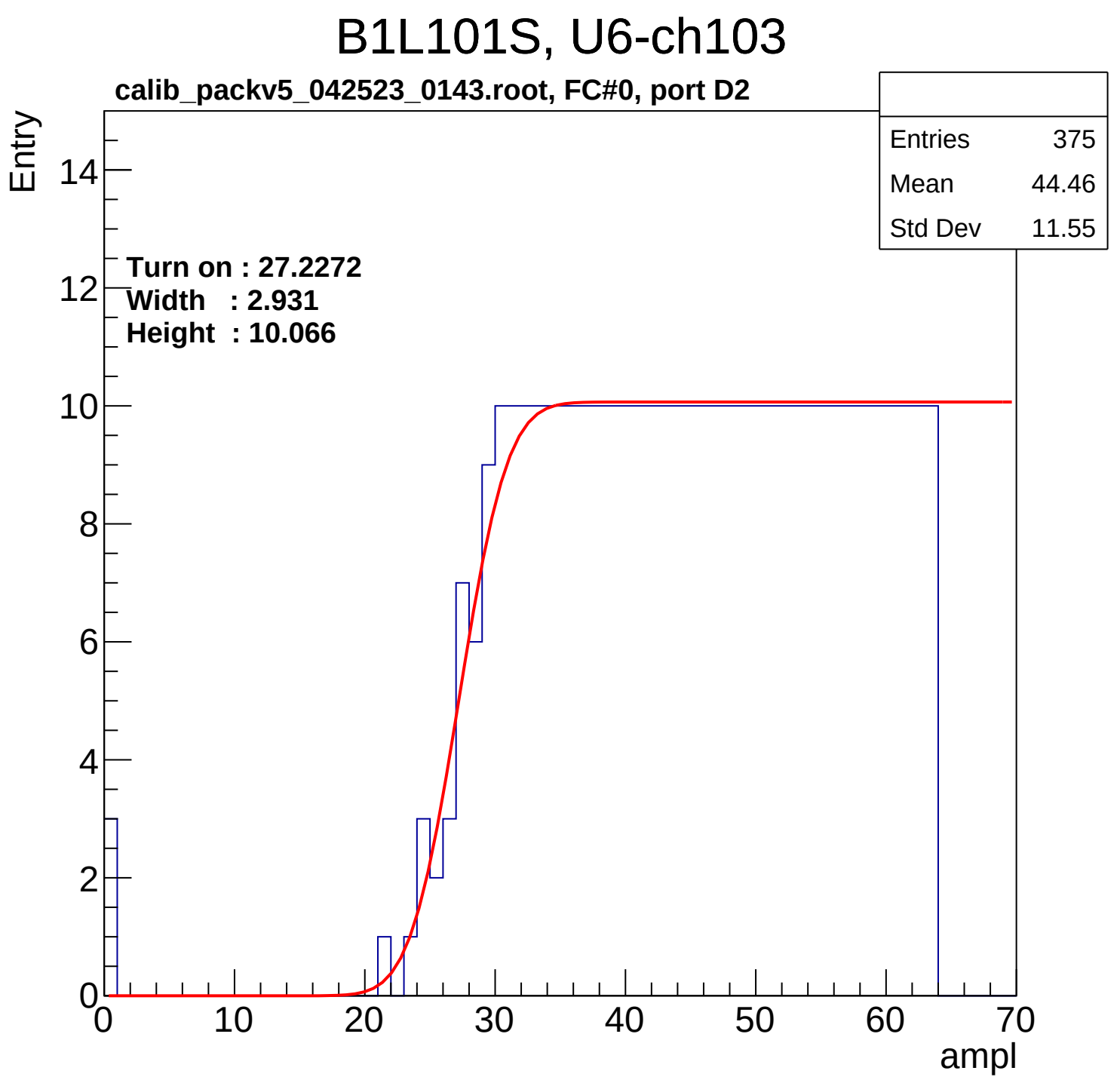

B1L101S, U6-ch98
calib_packv5_042523_0143.root, FC#0, port D2
Entries 384
Mean 43.98
Std Dev 11.82
Turn on : 25.7934
Width : 3.201
Height : 9.977
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

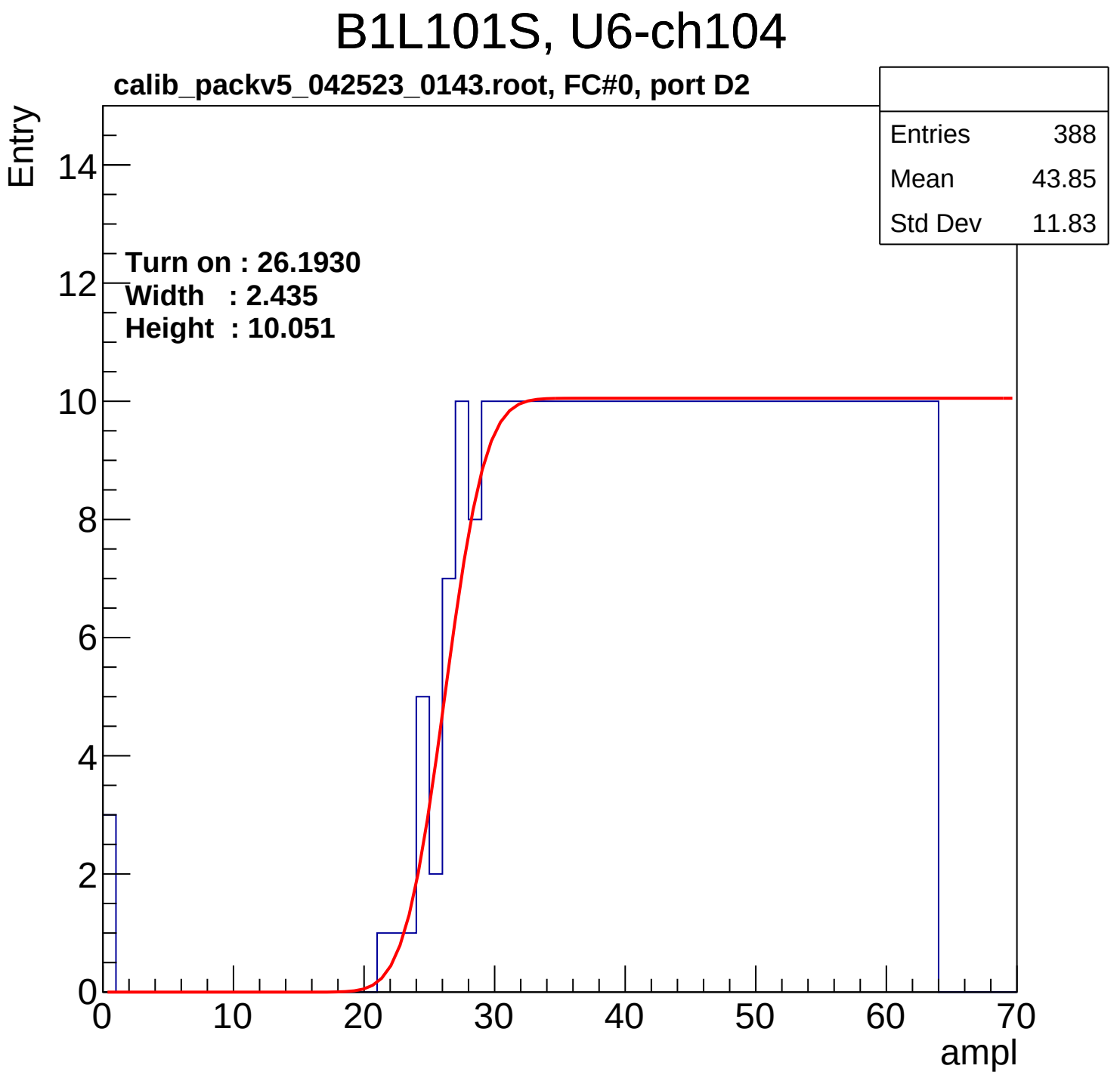

B1L101S, U6-ch99
calib_packv5_042523_0143.root, FC#0, port D2
Entries 366
Mean 44.8
Std Dev 11.57
Turn on : 27.7229
Width : 4.211
Height : 10.081
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

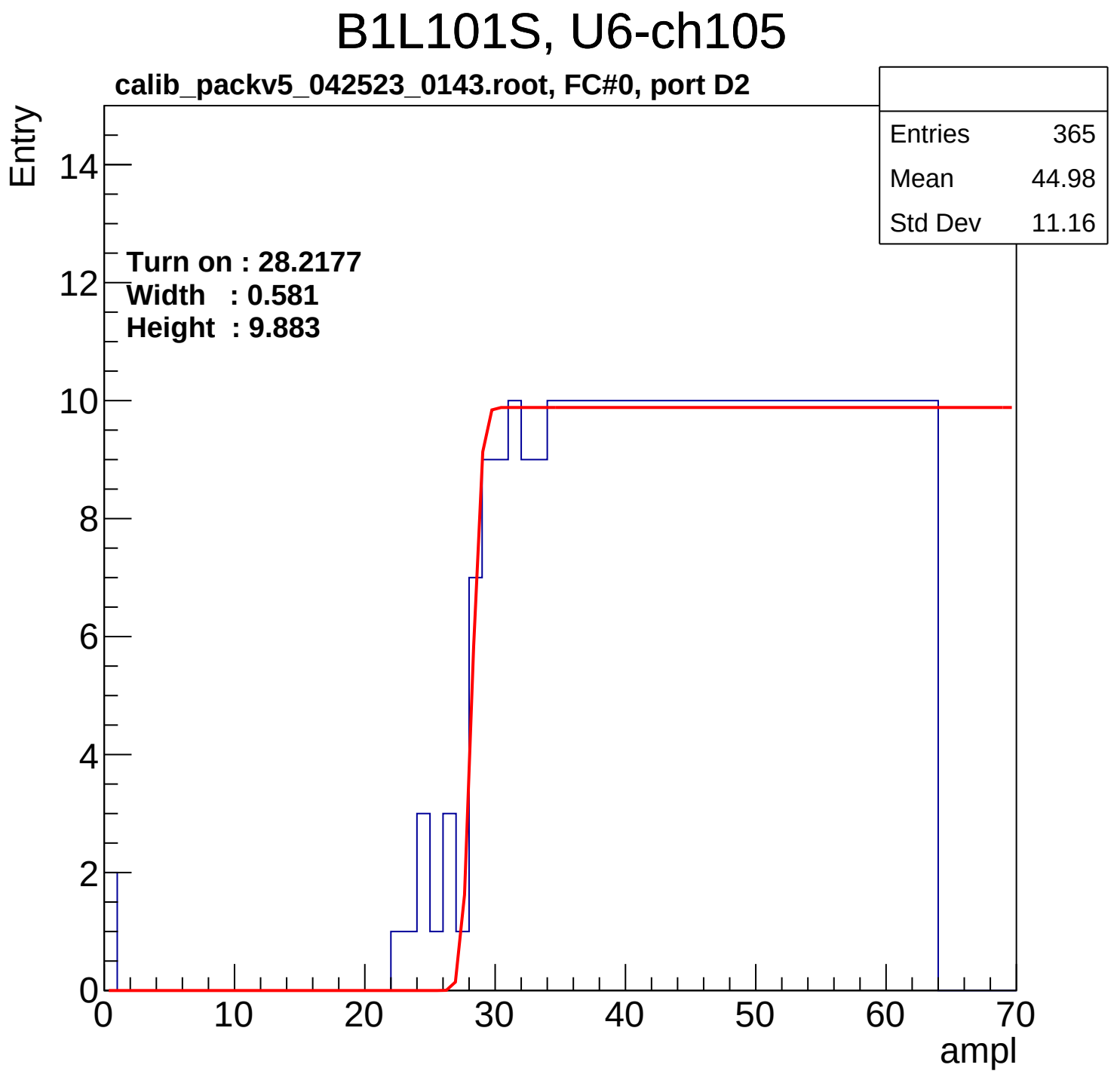

B1L101S, U6-ch100
calib_packv5_042523_0143.root, FC#0, port D2
Entries 376
Mean 44.55
Std Dev 11.19
Turn on : 26.8735
Width : 3.050
Height : 10.052
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

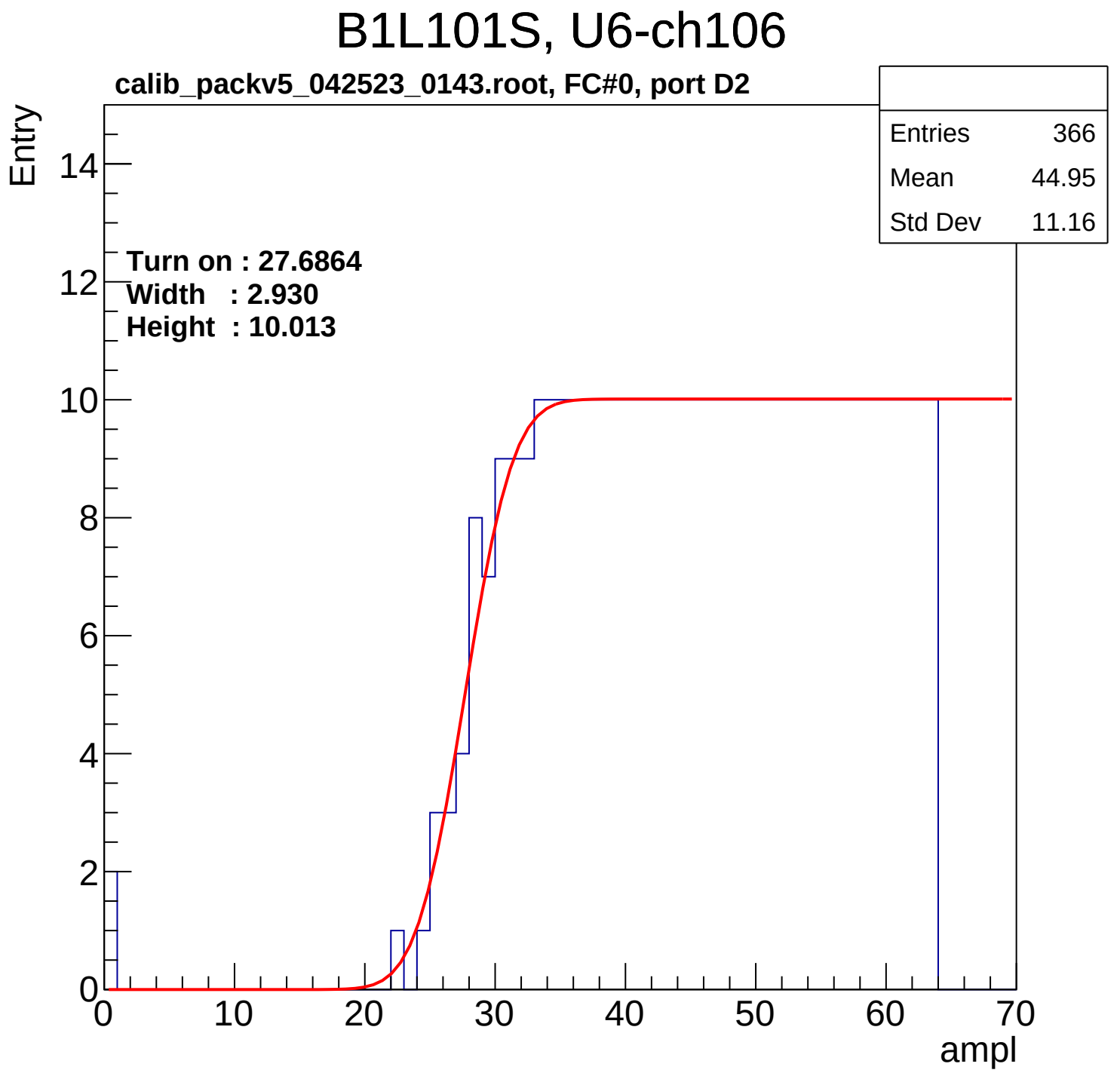

B1L101S, U6-ch101
calib_packv5_042523_0143.root, FC#0, port D2
Entries 368
Mean 44.87
Std Dev 11.19
Turn on : 27.9346
Width : 2.107
Height : 10.045
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

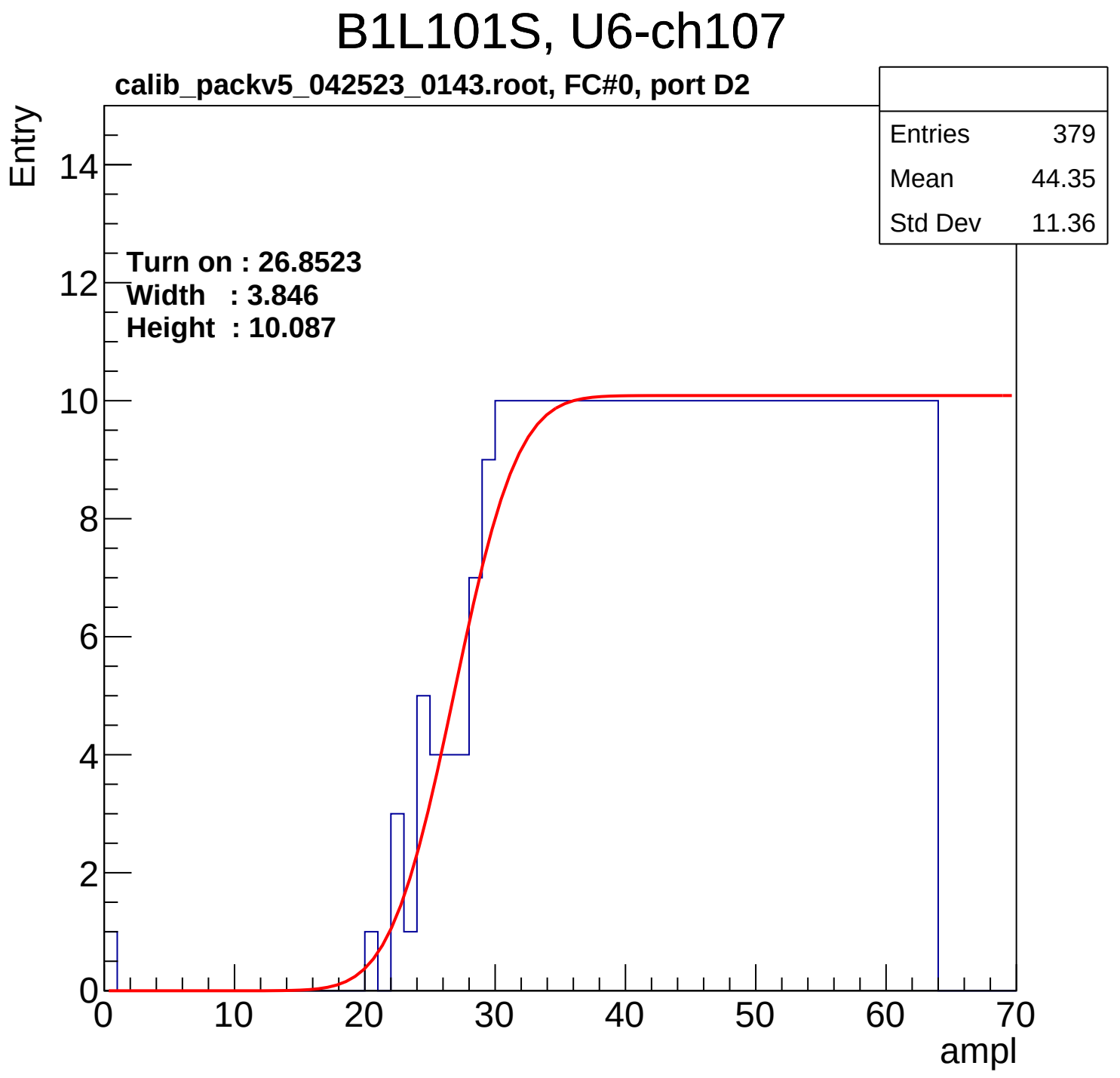

B1L101S, U6-ch102
calib_packv5_042523_0143.root, FC#0, port D2
Entries 365
Mean 44.97
Std Dev 11.18
Turn on : 27.9814
Width : 2.939
Height : 9.985
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

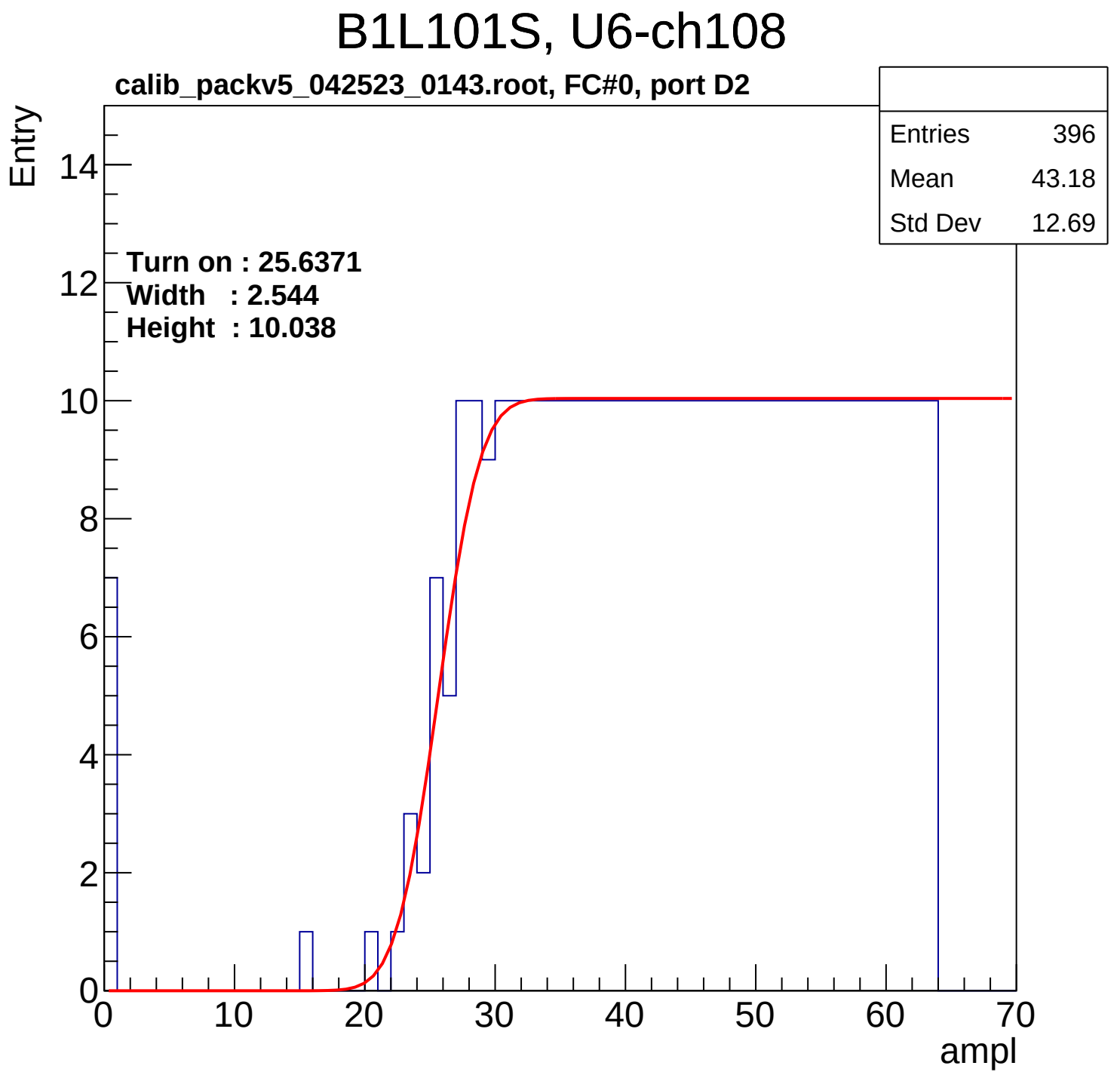

B1L101S, U6-ch103
calib_packv5_042523_0143.root, FC#0, port D2
Entries 375
Mean 44.46
Std Dev 11.55
Turn on : 27.2272
Width : 2.931
Height : 10.066
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

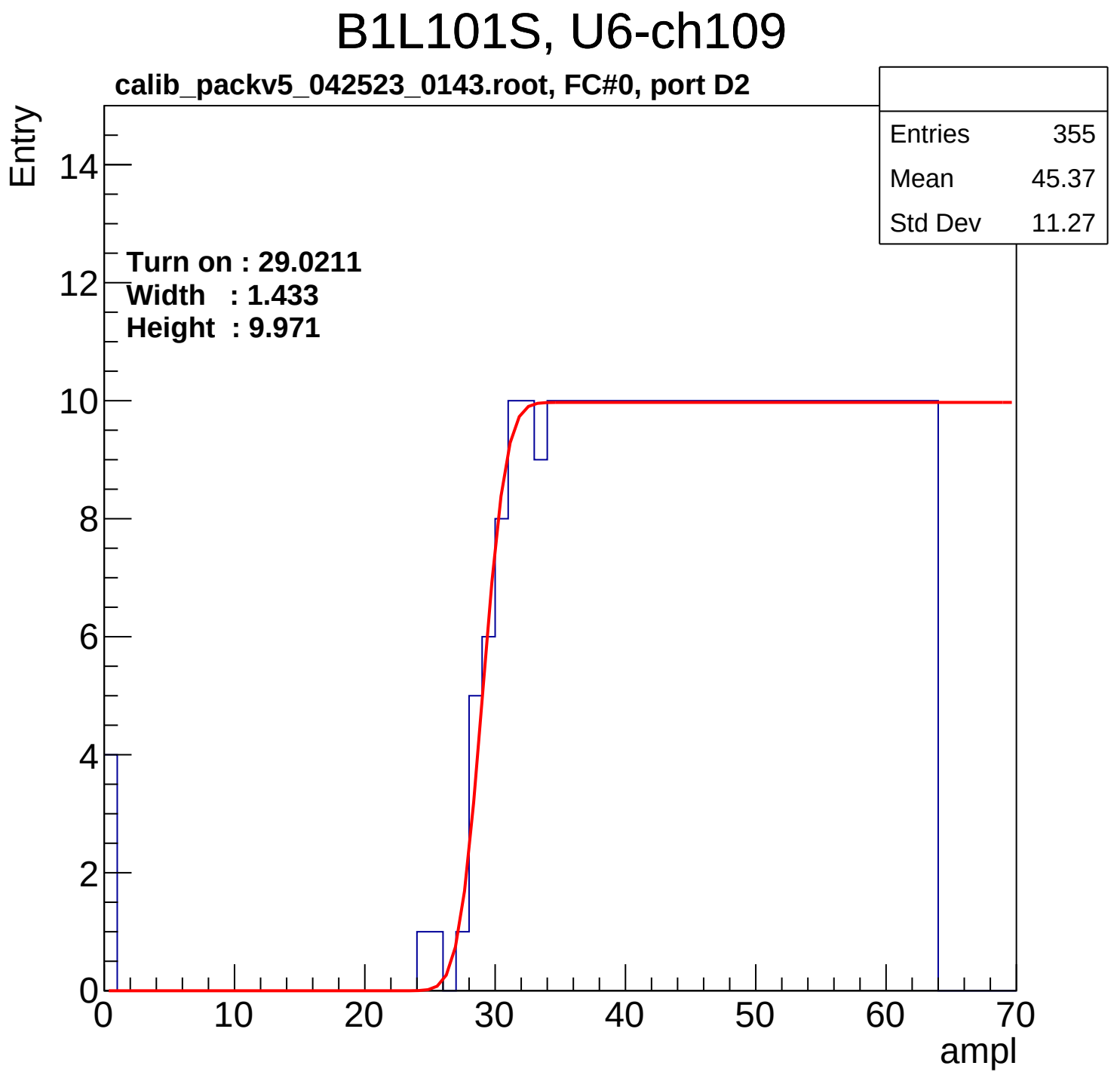

B1L101S, U6-ch104
calib_packv5_042523_0143.root, FC#0, port D2
Entries 388
Mean 43.85
Std Dev 11.83
Turn on : 26.1930
Width : 2.435
Height : 10.051
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

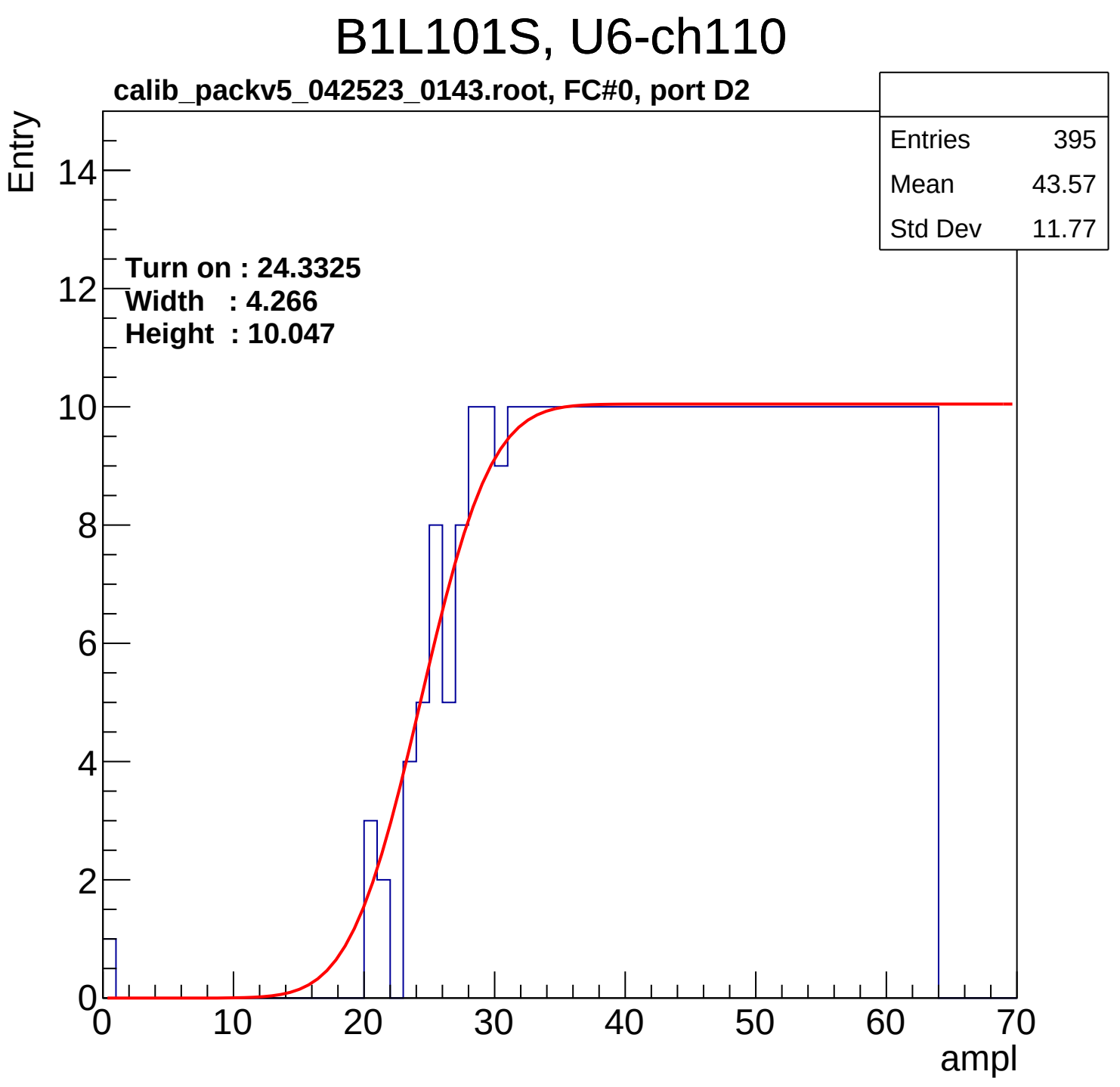

B1L101S, U6-ch105
calib_packv5_042523_0143.root, FC#0, port D2
Entries 365
Mean 44.98
Std Dev 11.16
Turn on : 28.2177
Width : 0.581
Height : 9.883
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

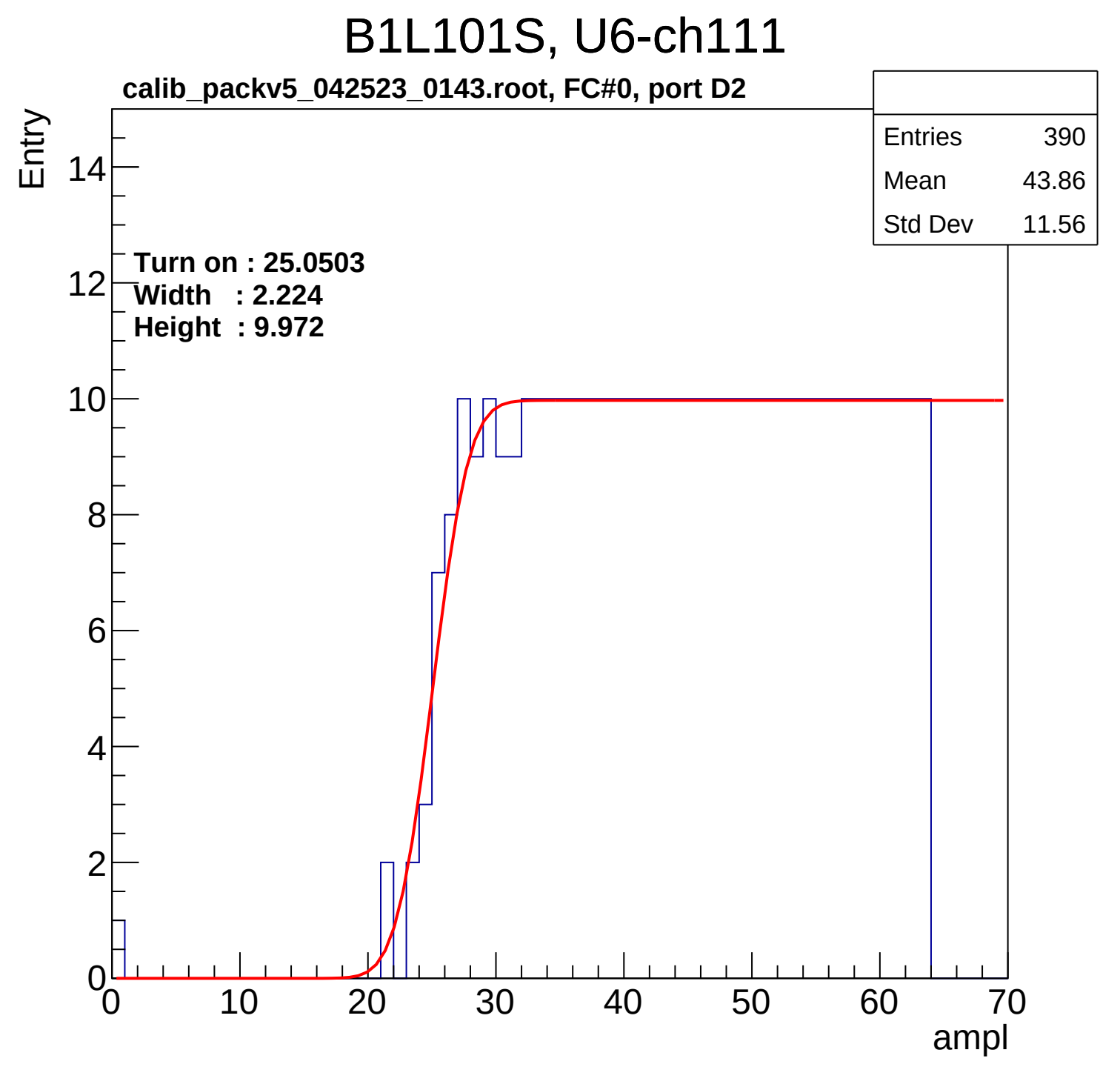

B1L101S, U6-ch106
calib_packv5_042523_0143.root, FC#0, port D2
Entries 366
Mean 44.95
Std Dev 11.16
Turn on : 27.6864
Width : 2.930
Height : 10.013
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

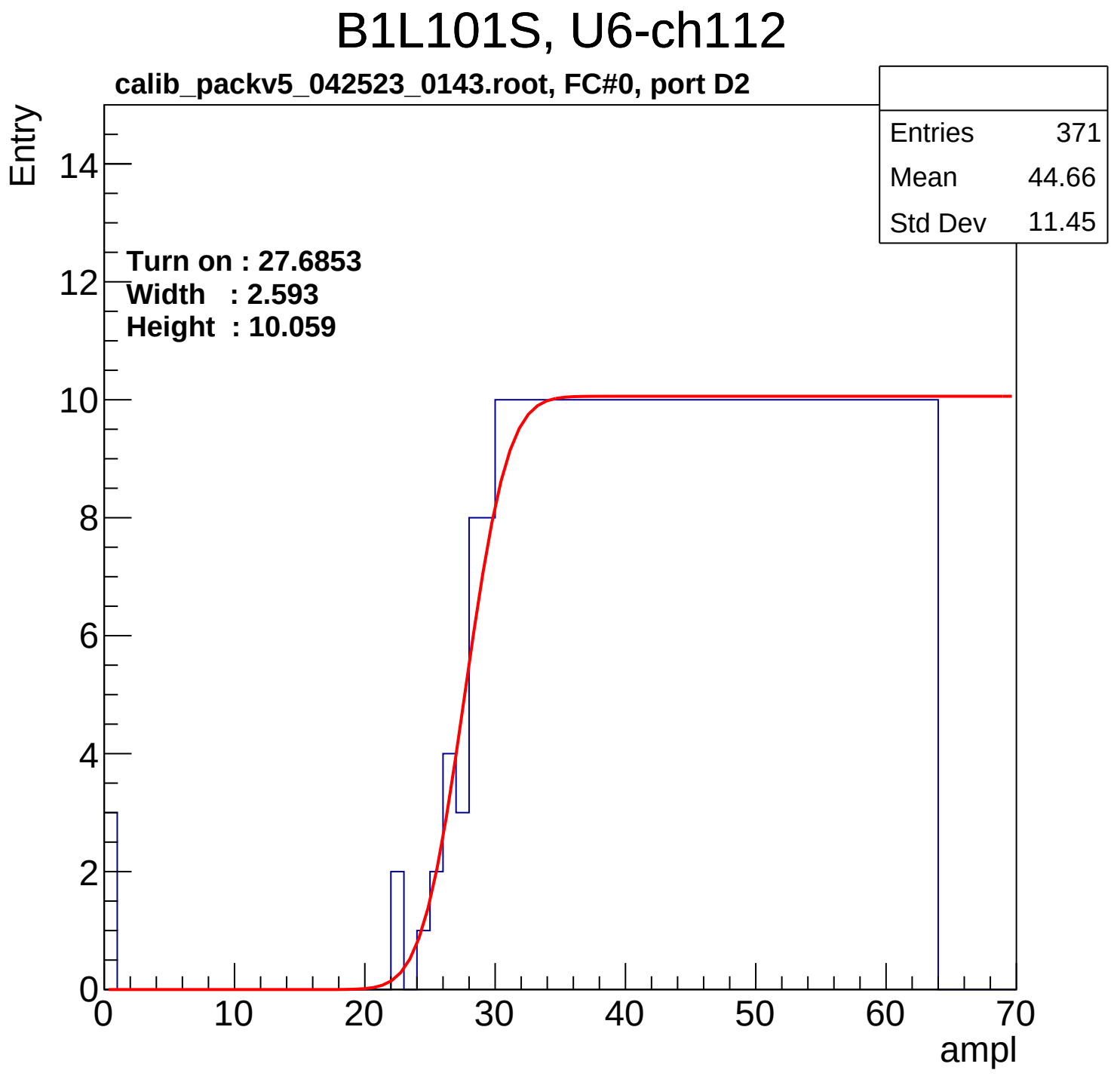

B1L101S, U6-ch107
calib_packv5_042523_0143.root, FC#0, port D2
Entries 379
Mean 44.35
Std Dev 11.36
Turn on : 26.8523
Width : 3.846
Height : 10.087
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

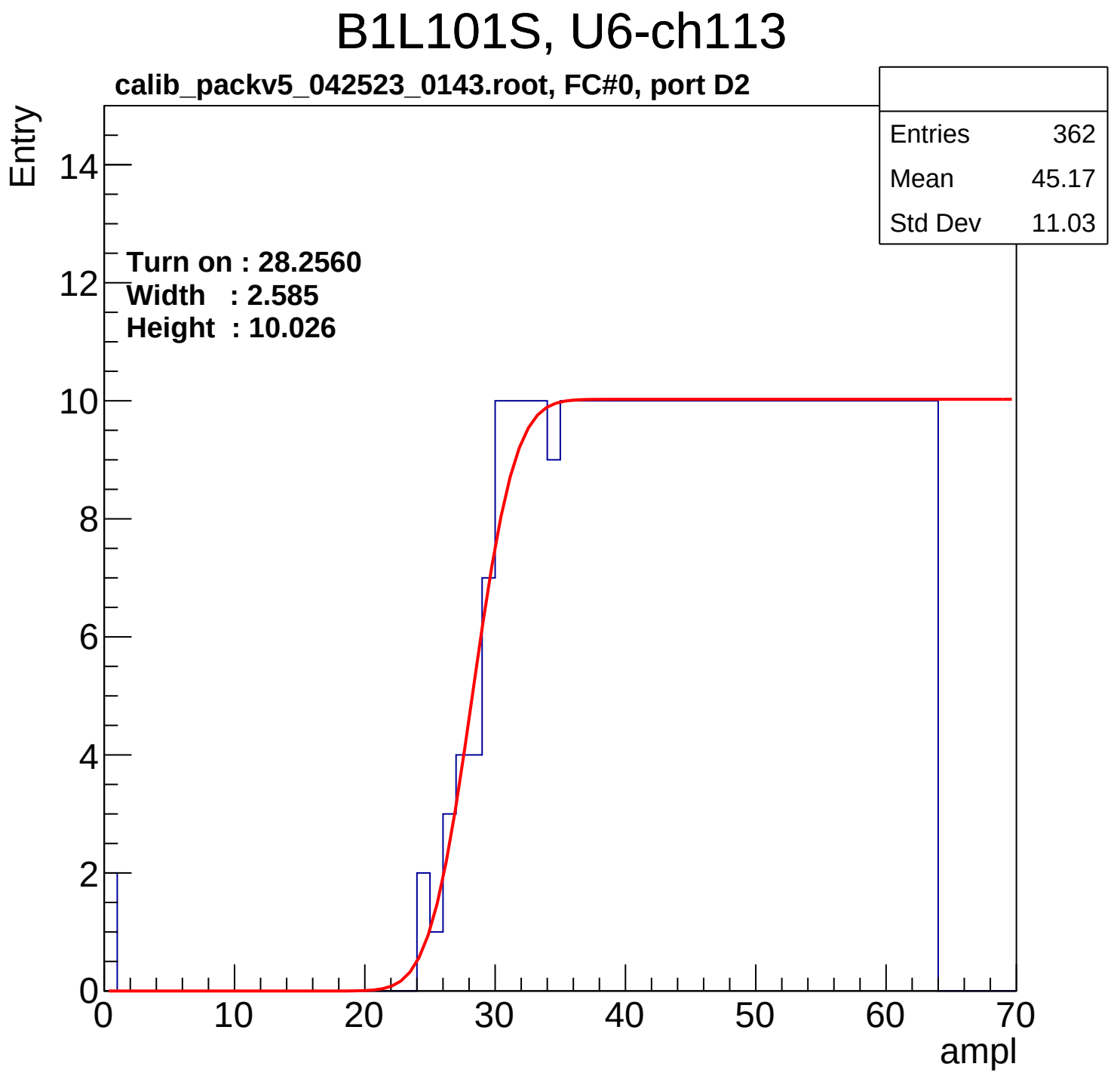

B1L101S, U6-ch108
calib_packv5_042523_0143.root, FC#0, port D2
Entries 396
Mean 43.18
Std Dev 12.69
Turn on : 25.6371
Width : 2.544
Height : 10.038
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

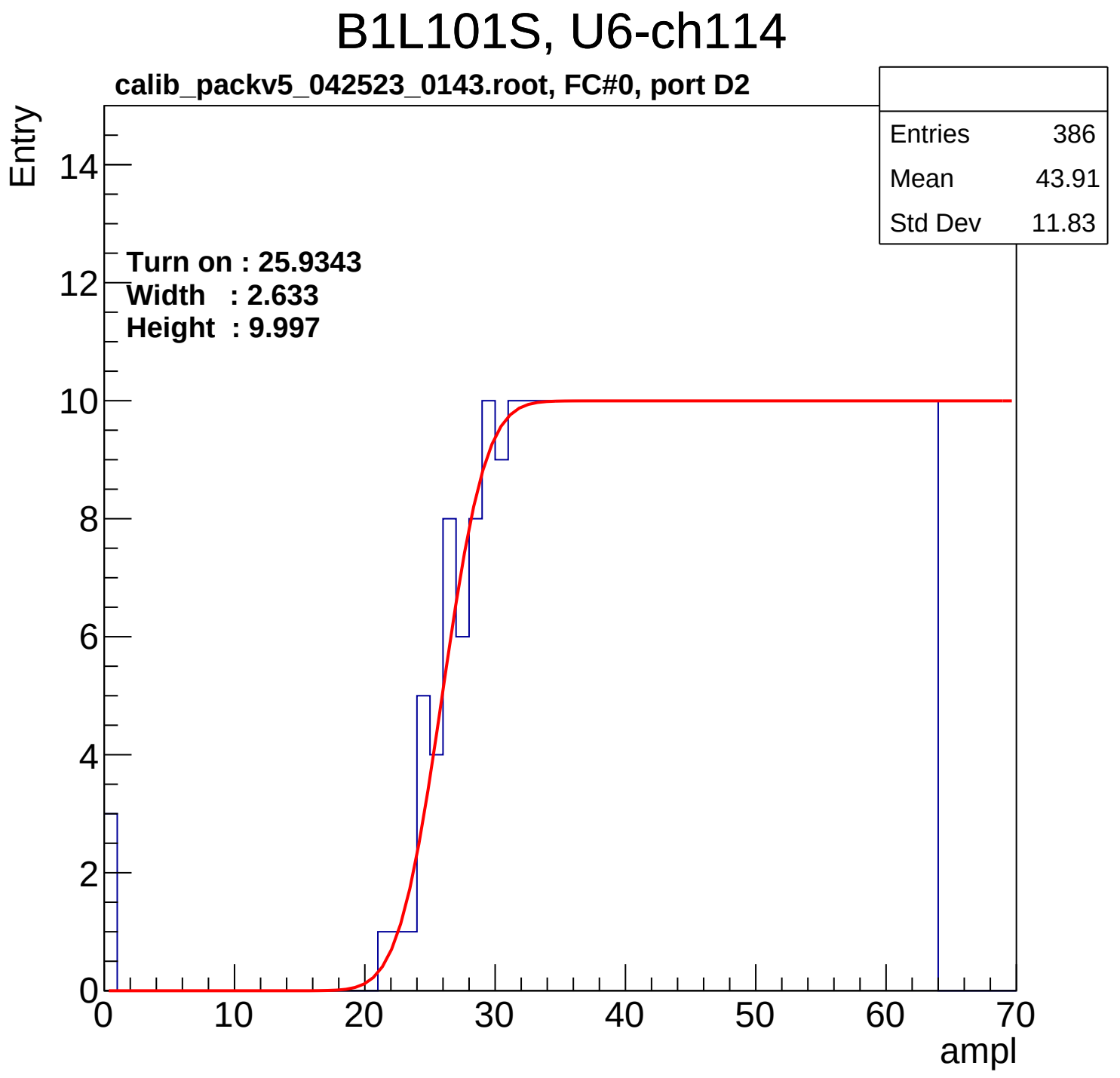

B1L101S, U6-ch109
calib_packv5_042523_0143.root, FC#0, port D2
Entries 355
Mean 45.37
Std Dev 11.27
Turn on : 29.0211
Width : 1.433
Height : 9.971
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

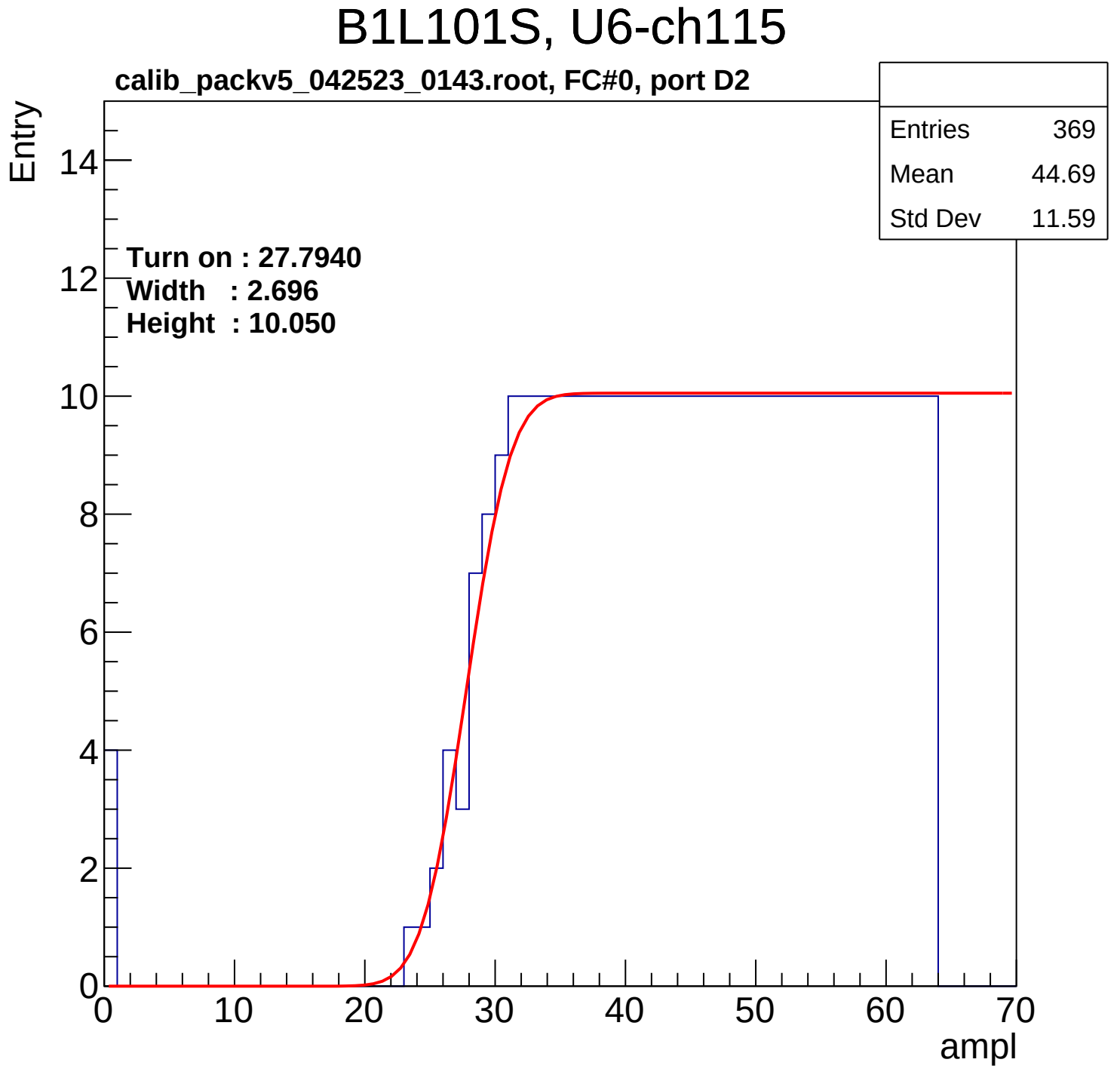

B1L101S, U6-ch110
calib_packv5_042523_0143.root, FC#0, port D2
Entries 395
Mean 43.57
Std Dev 11.77
Turn on : 24.3325
Width : 4.266
Height : 10.047
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

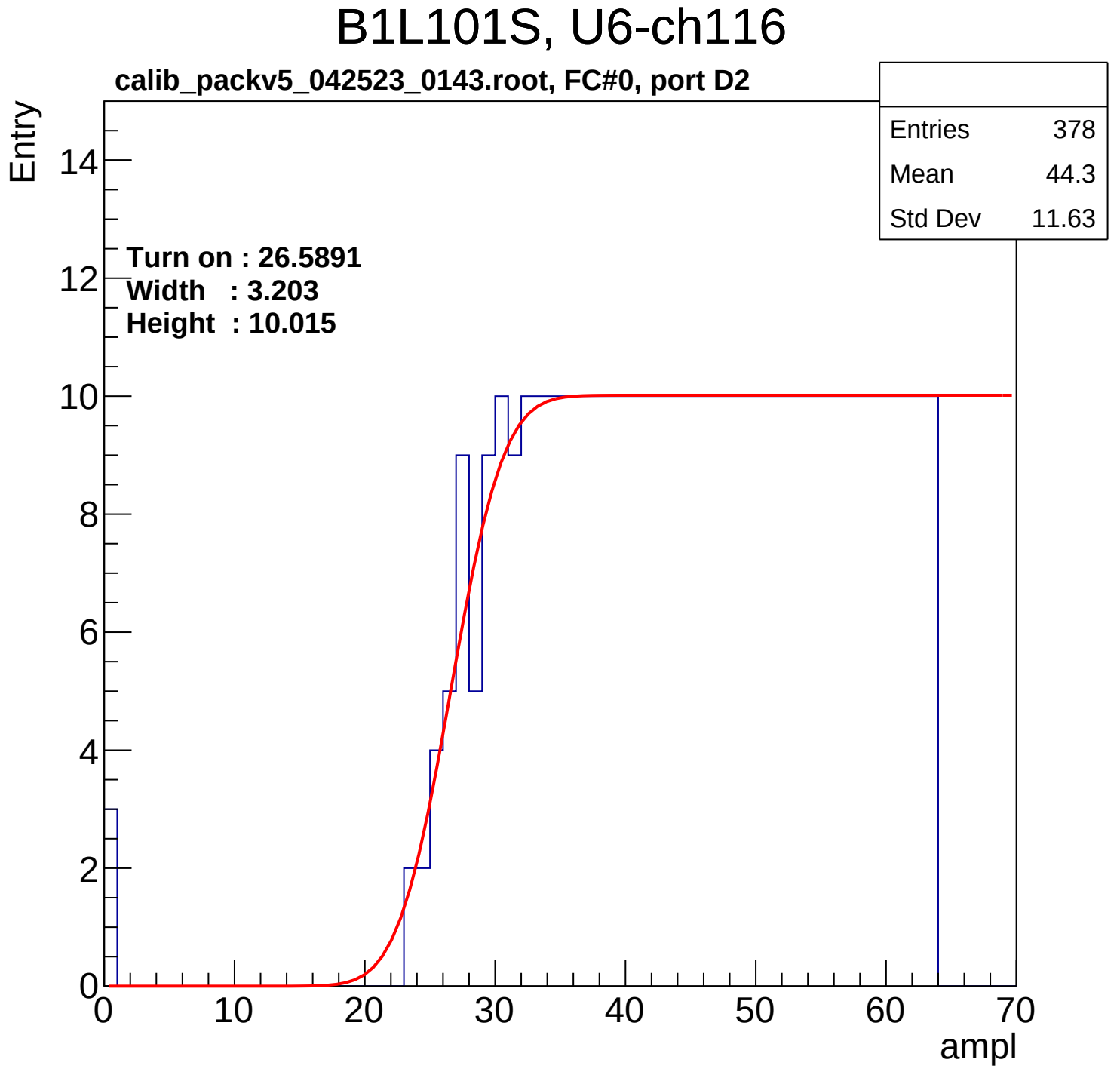

B1L101S, U6-ch111
calib_packv5_042523_0143.root, FC#0, port D2
Entries 390
Mean 43.86
Std Dev 11.56
Turn on : 25.0503
Width : 2.224
Height : 9.972
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

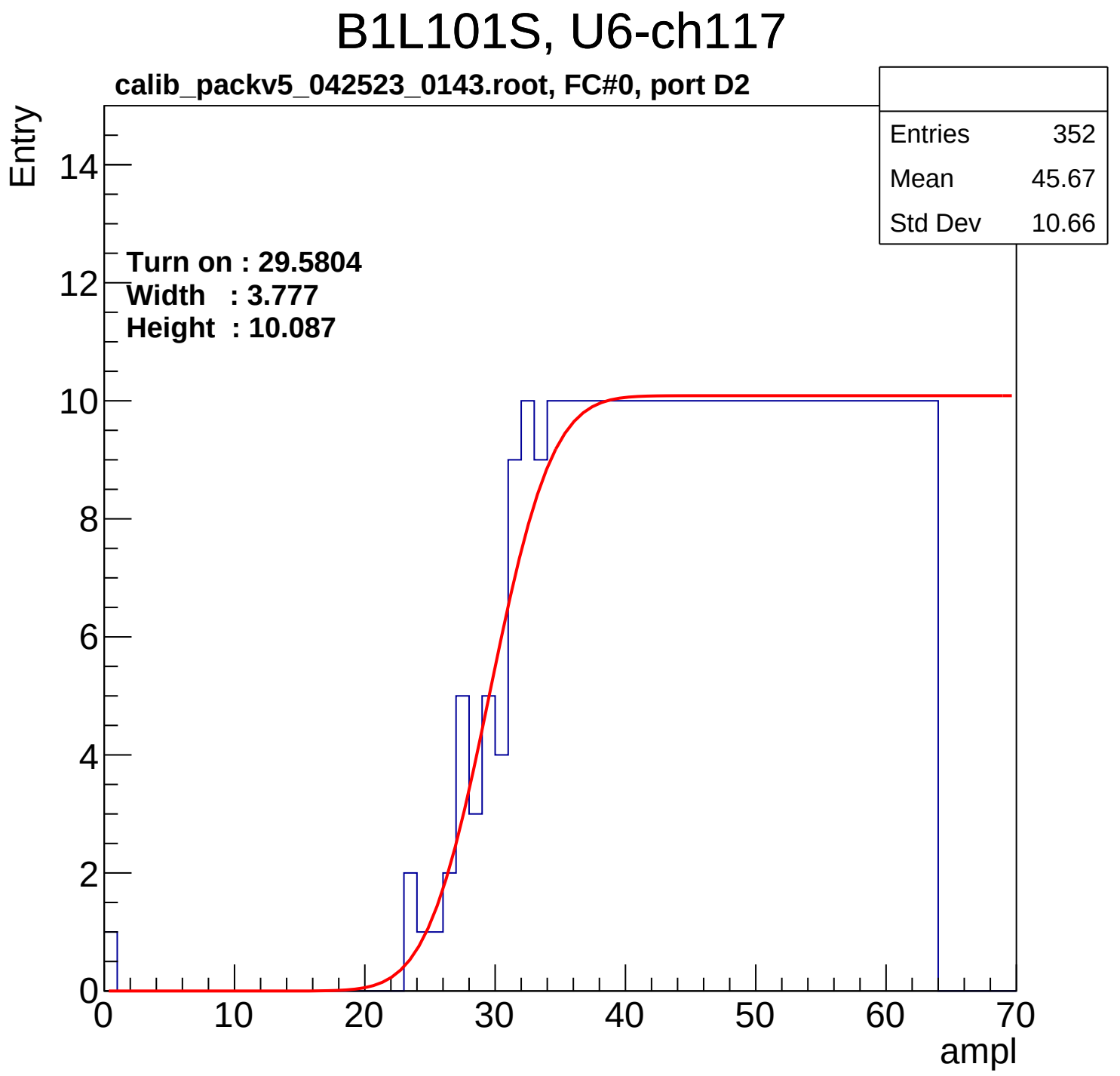

B1L101S, U6-ch112
calib_packv5_042523_0143.root, FC#0, port D2
Entries 371
Mean 44.66
Std Dev 11.45
Turn on : 27.6853
Width : 2.593
Height : 10.059
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

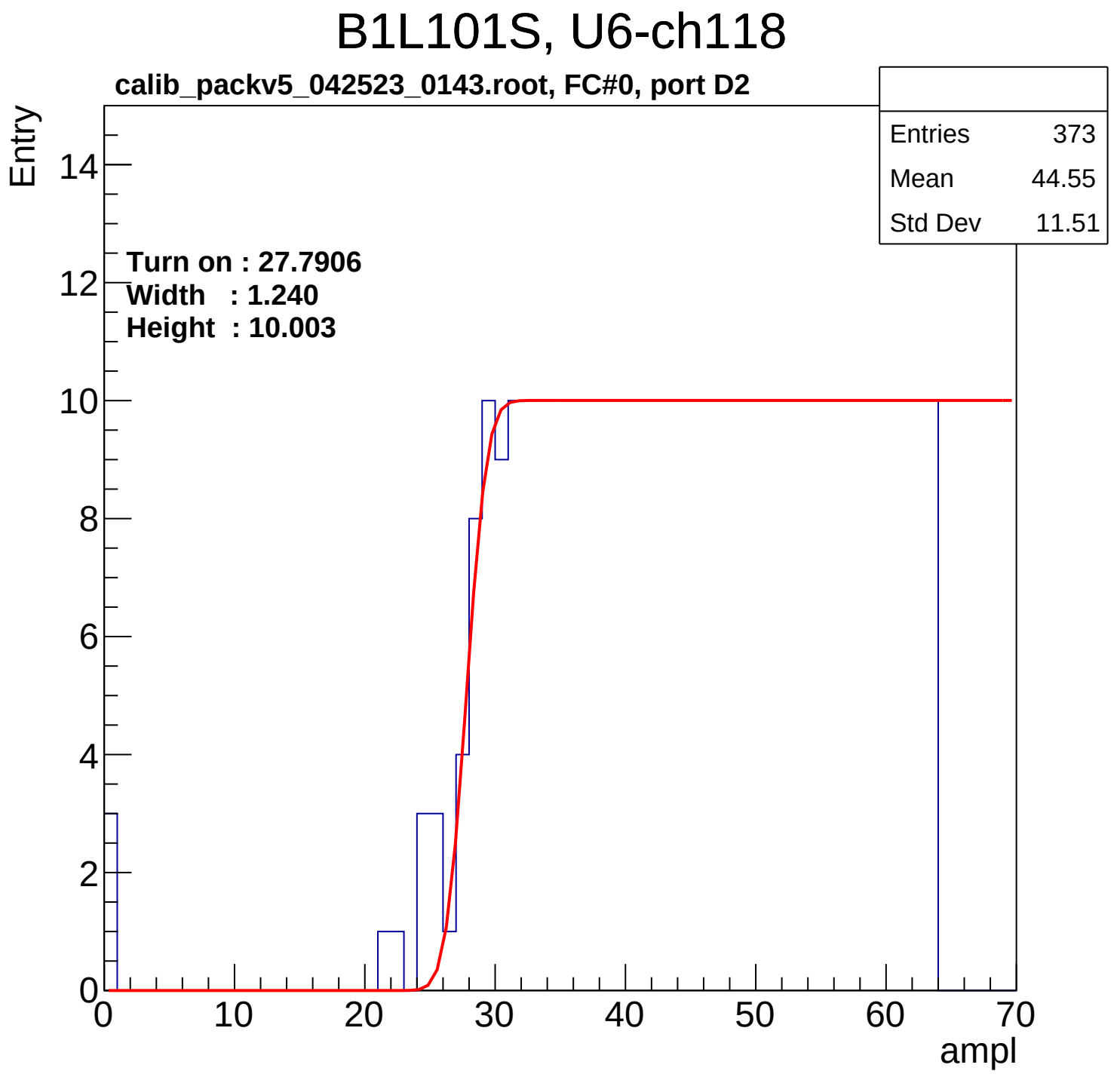

B1L101S, U6-ch113
calib_packv5_042523_0143.root, FC#0, port D2
Entries 362
Mean 45.17
Std Dev 11.03
Turn on : 28.2560
Width : 2.585
Height : 10.026
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

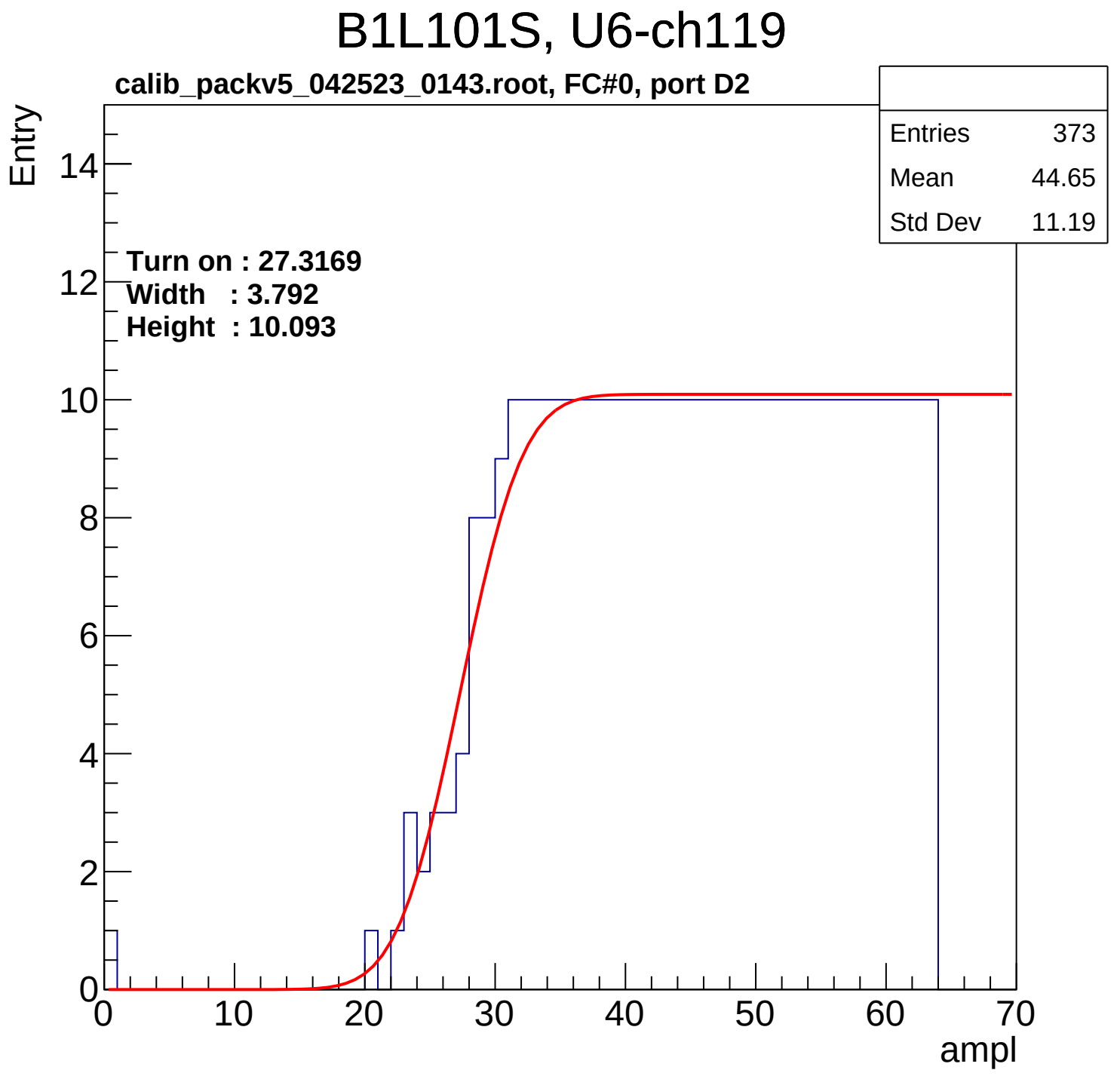

B1L101S, U6-ch114
calib_packv5_042523_0143.root, FC#0, port D2
Entries 386
Mean 43.91
Std Dev 11.83
Turn on : 25.9343
Width : 2.633
Height : 9.997
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

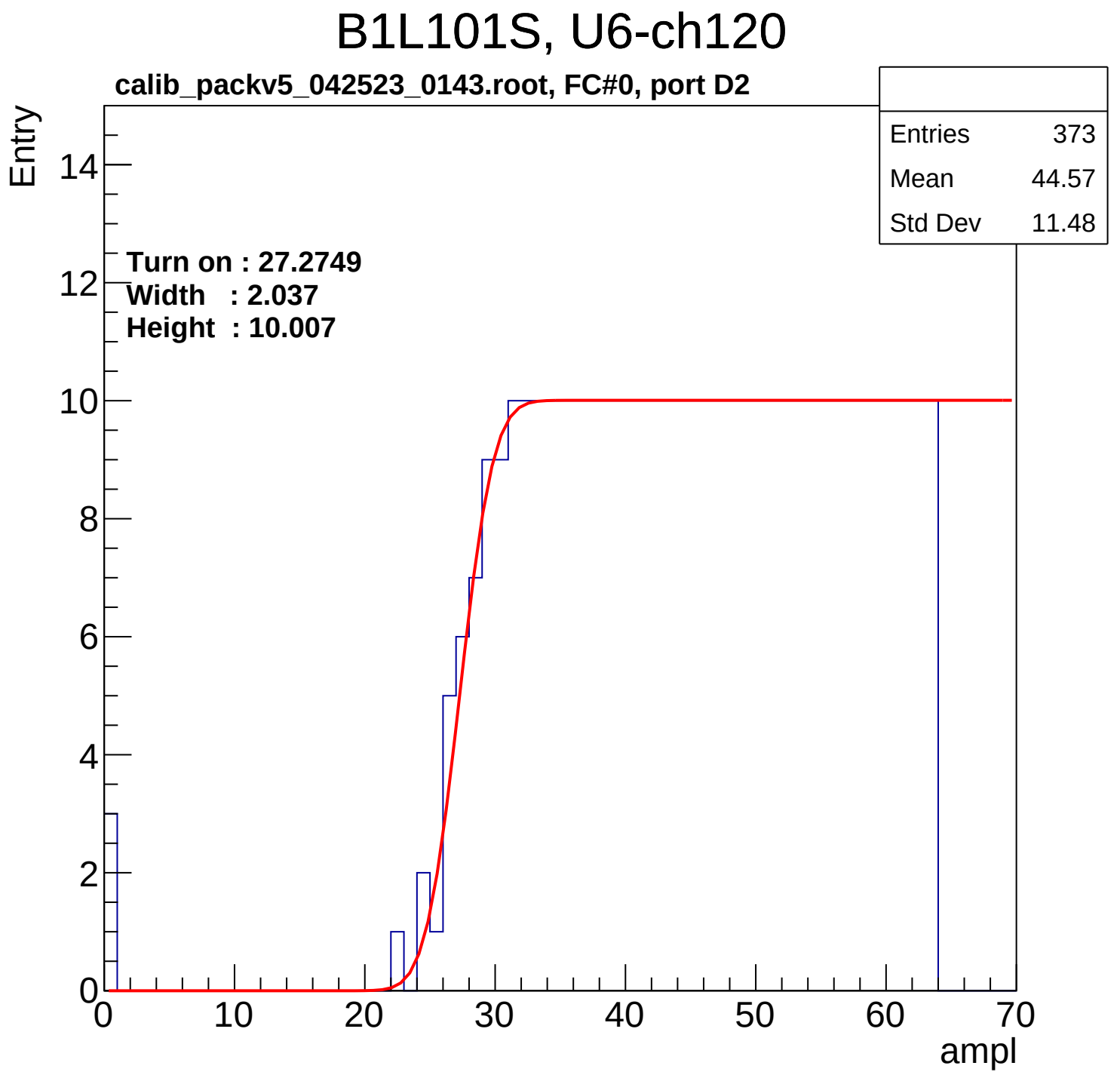

B1L101S, U6-ch115
calib_packv5_042523_0143.root, FC#0, port D2
Entries 369
Mean 44.69
Std Dev 11.59
Turn on : 27.7940
Width : 2.696
Height : 10.050
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

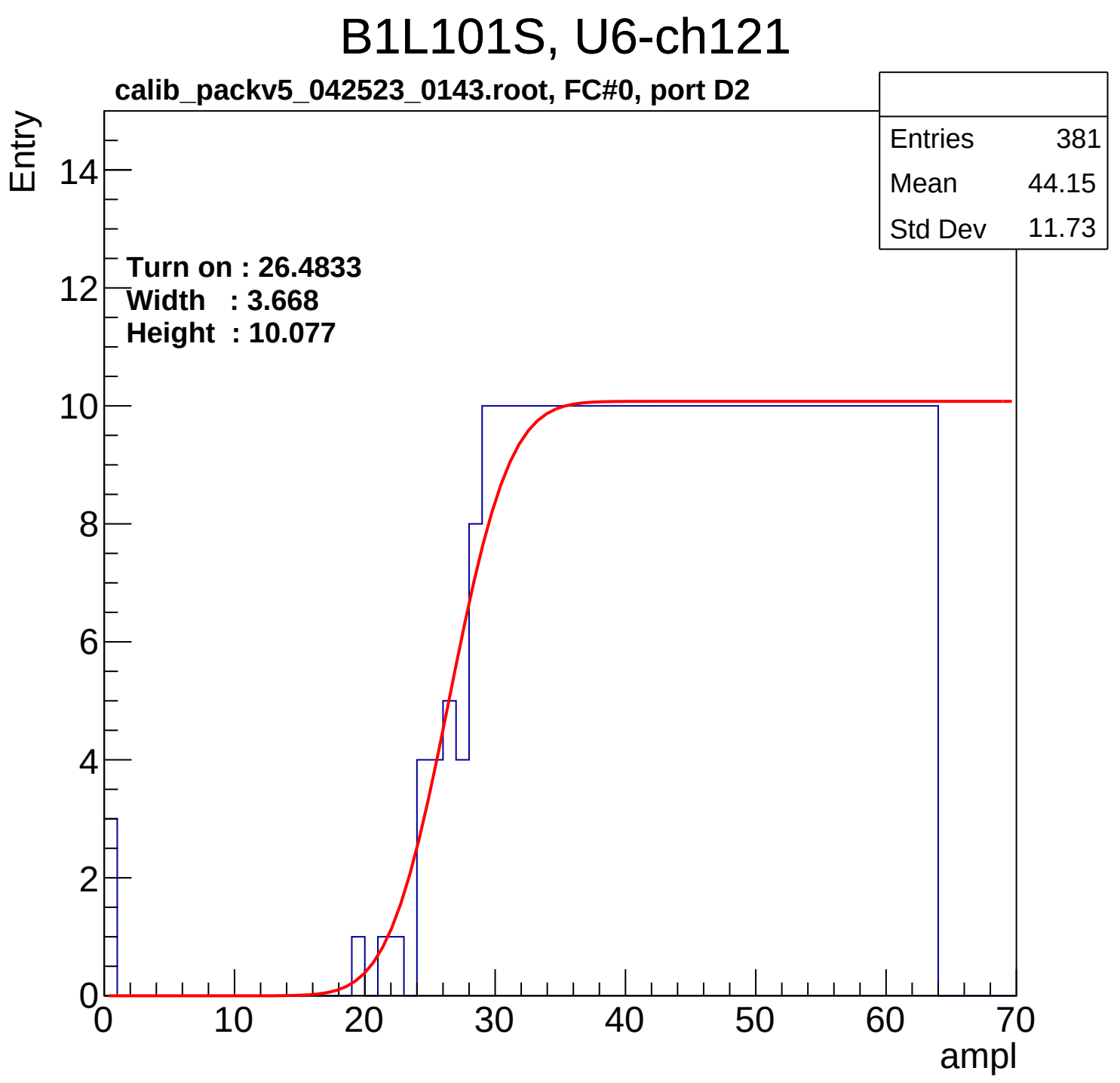

B1L101S, U6-ch116
calib_packv5_042523_0143.root, FC#0, port D2
Entries 378
Mean 44.3
Std Dev 11.63
Turn on : 26.5891
Width : 3.203
Height : 10.015
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

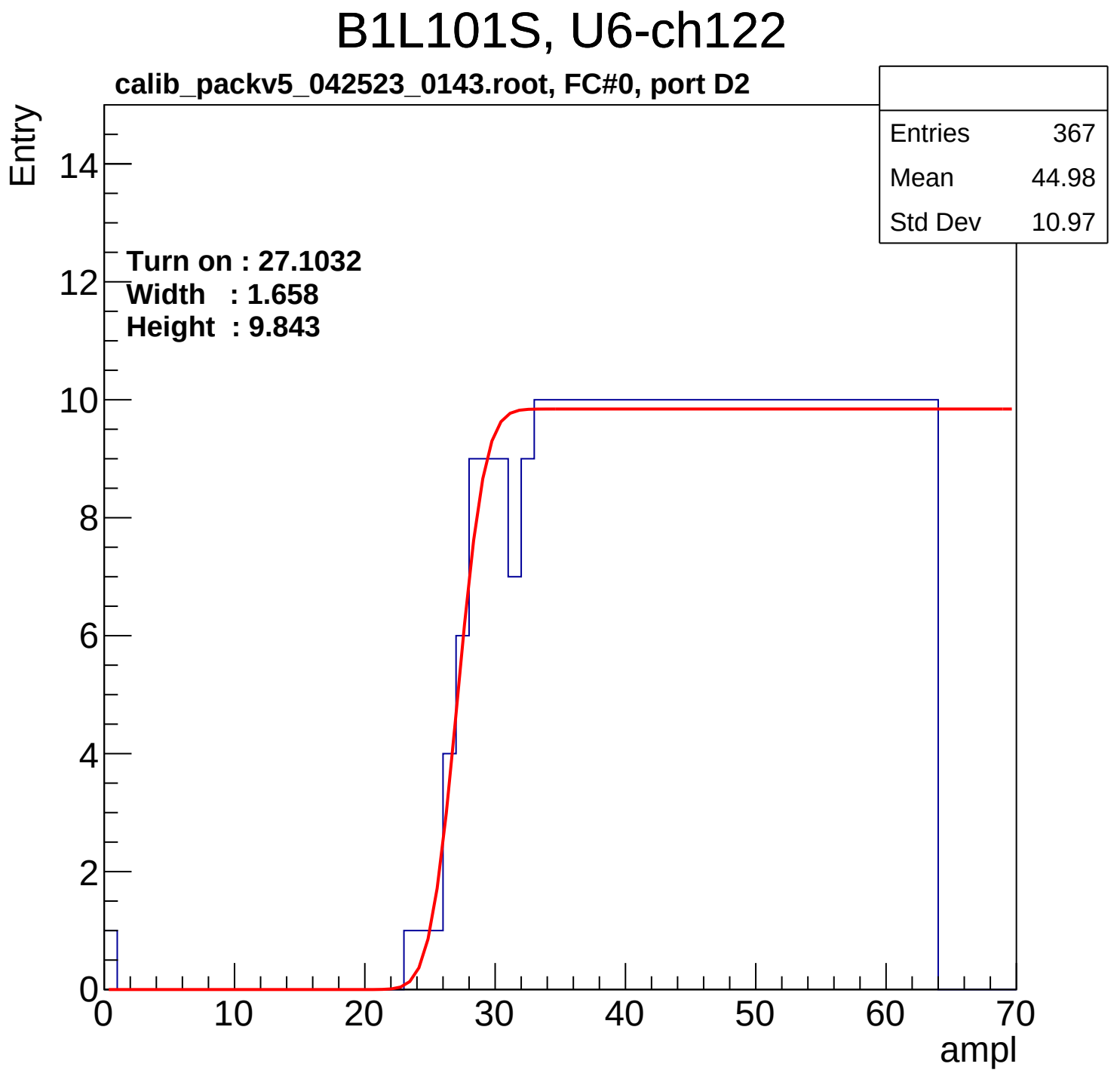

B1L101S, U6-ch117
calib_packv5_042523_0143.root, FC#0, port D2
Entries 352
Mean 45.67
Std Dev 10.66
Turn on : 29.5804
Width : 3.777
Height : 10.087
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

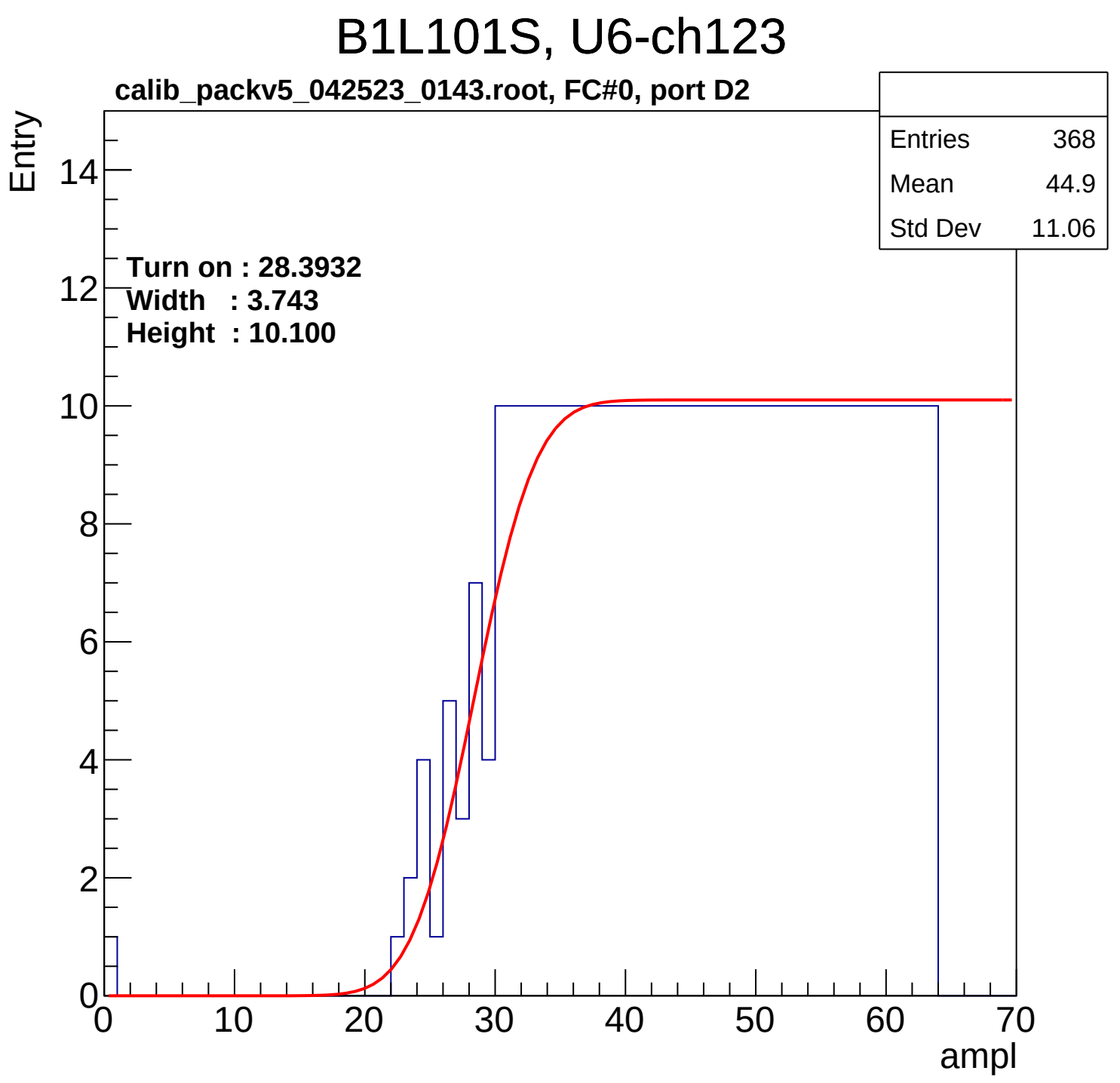

B1L101S, U6-ch118
calib_packv5_042523_0143.root, FC#0, port D2
Entries 373
Mean 44.55
Std Dev 11.51
Turn on : 27.7906
Width : 1.240
Height : 10.003
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

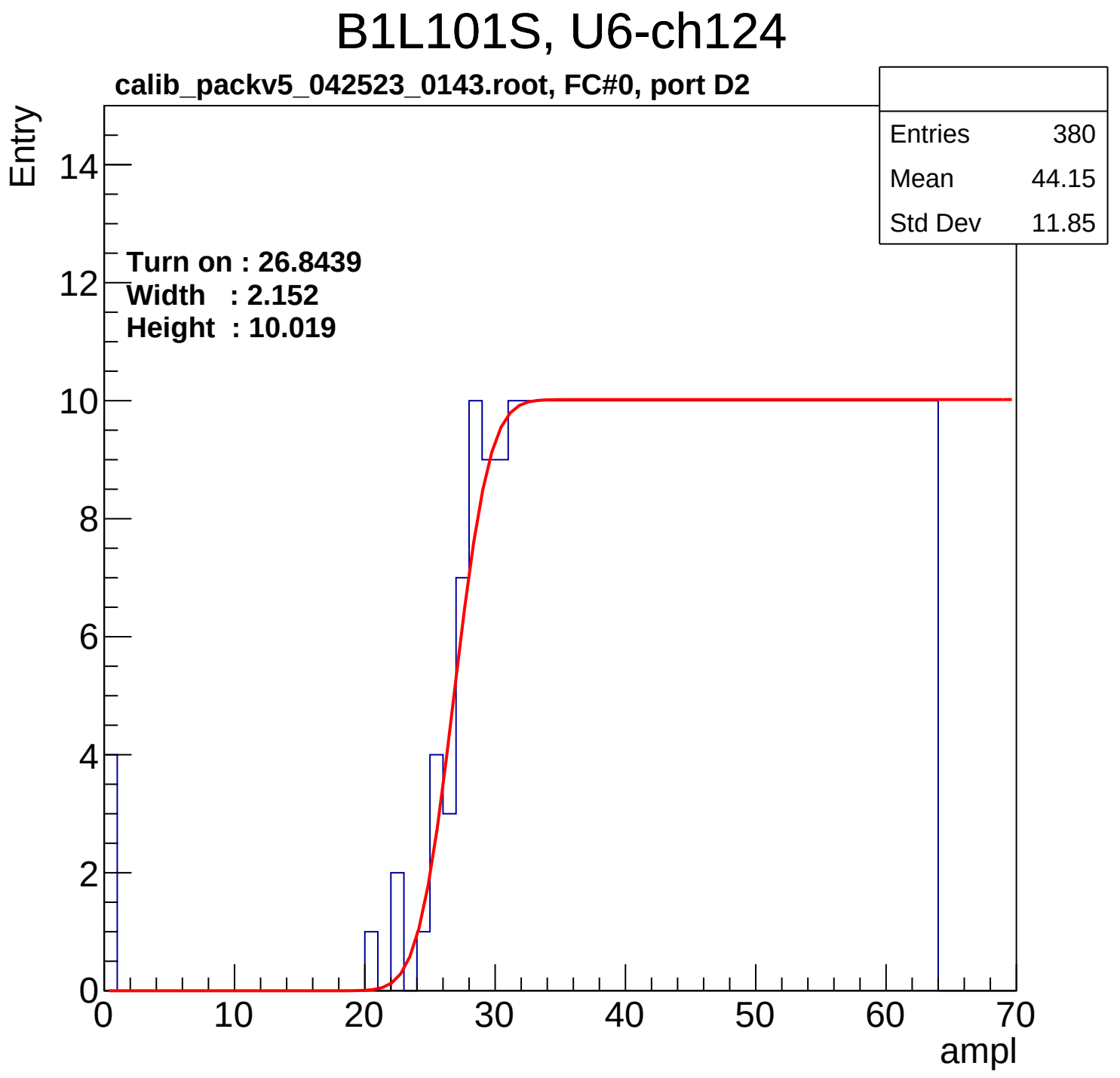

B1L101S, U6-ch119
calib_packv5_042523_0143.root, FC#0, port D2
Entries 373
Mean 44.65
Std Dev 11.19
Turn on : 27.3169
Width : 3.792
Height : 10.093
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

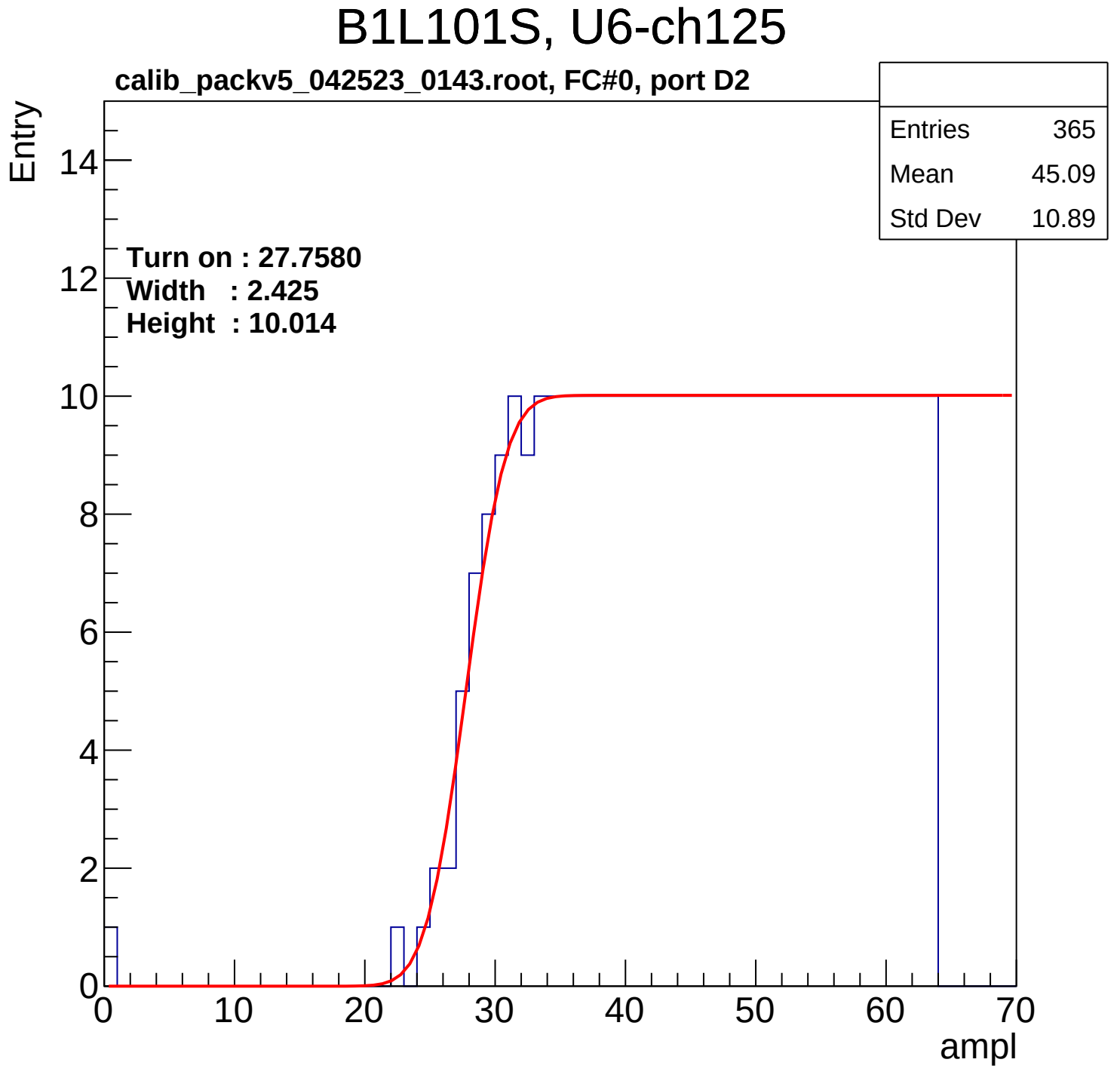

B1L101S, U6-ch120
calib_packv5_042523_0143.root, FC#0, port D2
Entries 373
Mean 44.57
Std Dev 11.48
Turn on : 27.2749
Width : 2.037
Height : 10.007
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

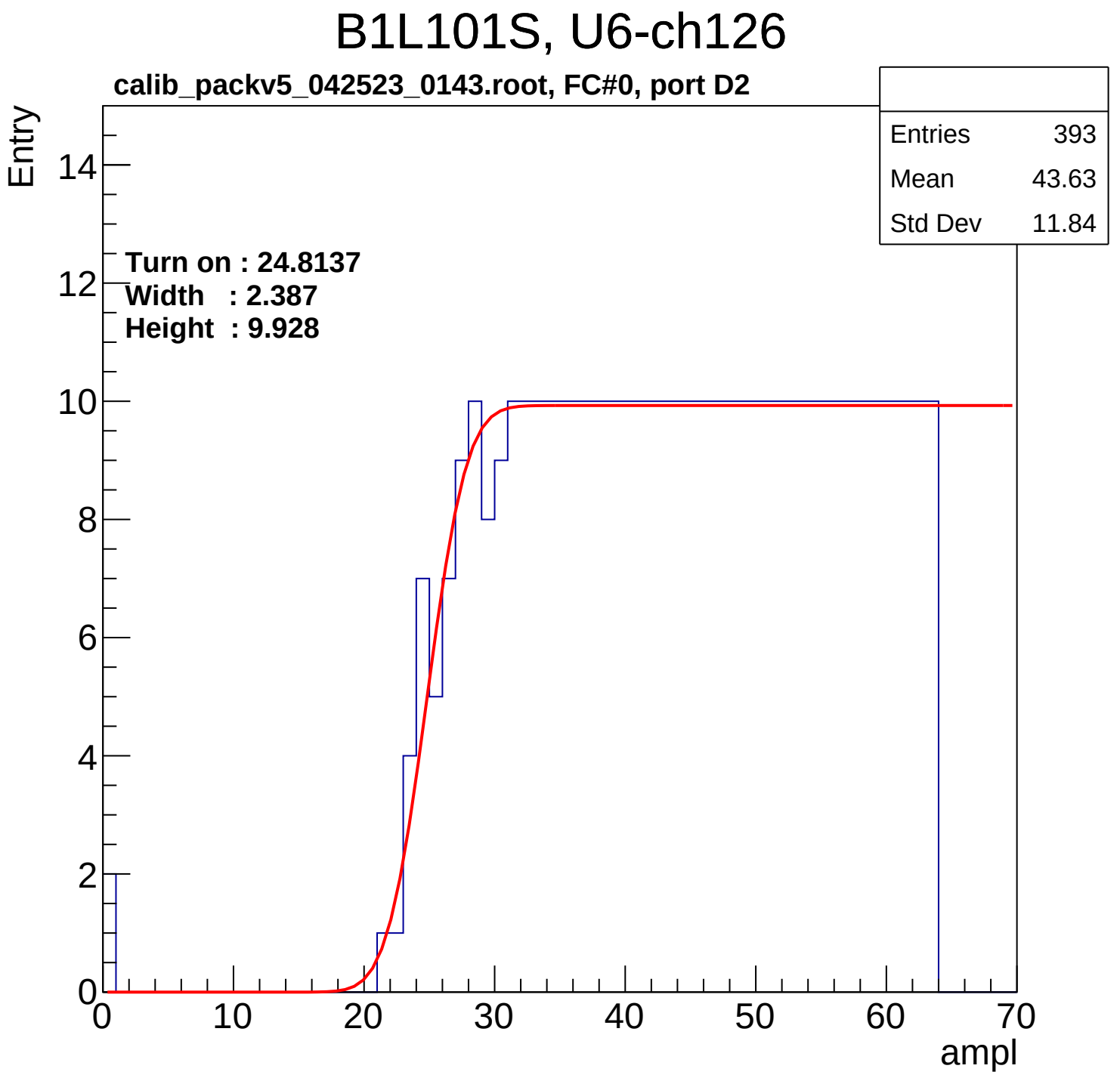

B1L101S, U6-ch121
calib_packv5_042523_0143.root, FC#0, port D2
Entries 381
Mean 44.15
Std Dev 11.73
Turn on : 26.4833
Width : 3.668
Height : 10.077
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

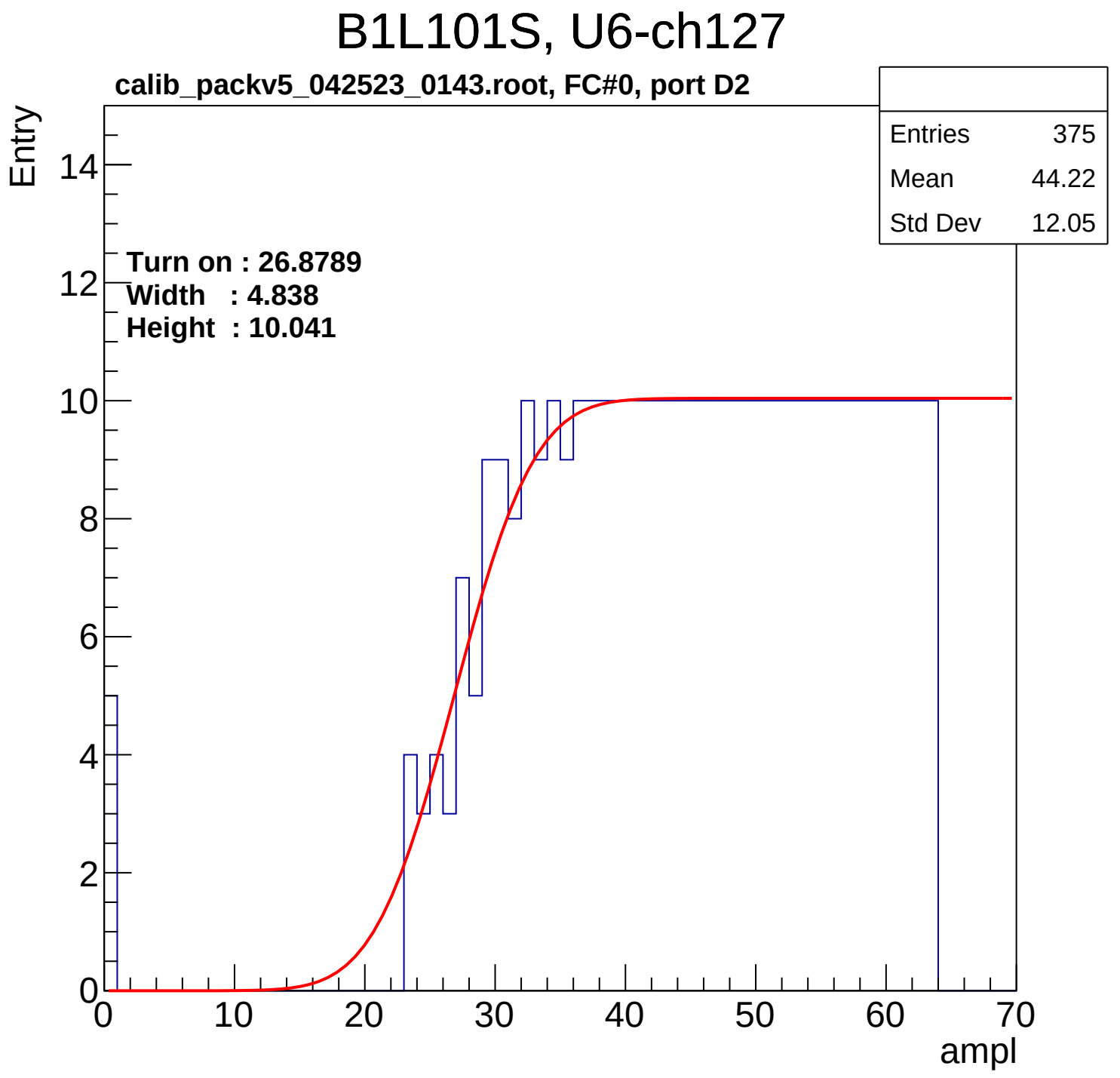

B1L101S, U6-ch122
calib_packv5_042523_0143.root, FC#0, port D2
Entries 367
Mean 44.98
Std Dev 10.97
Turn on : 27.1032
Width : 1.658
Height : 9.843
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

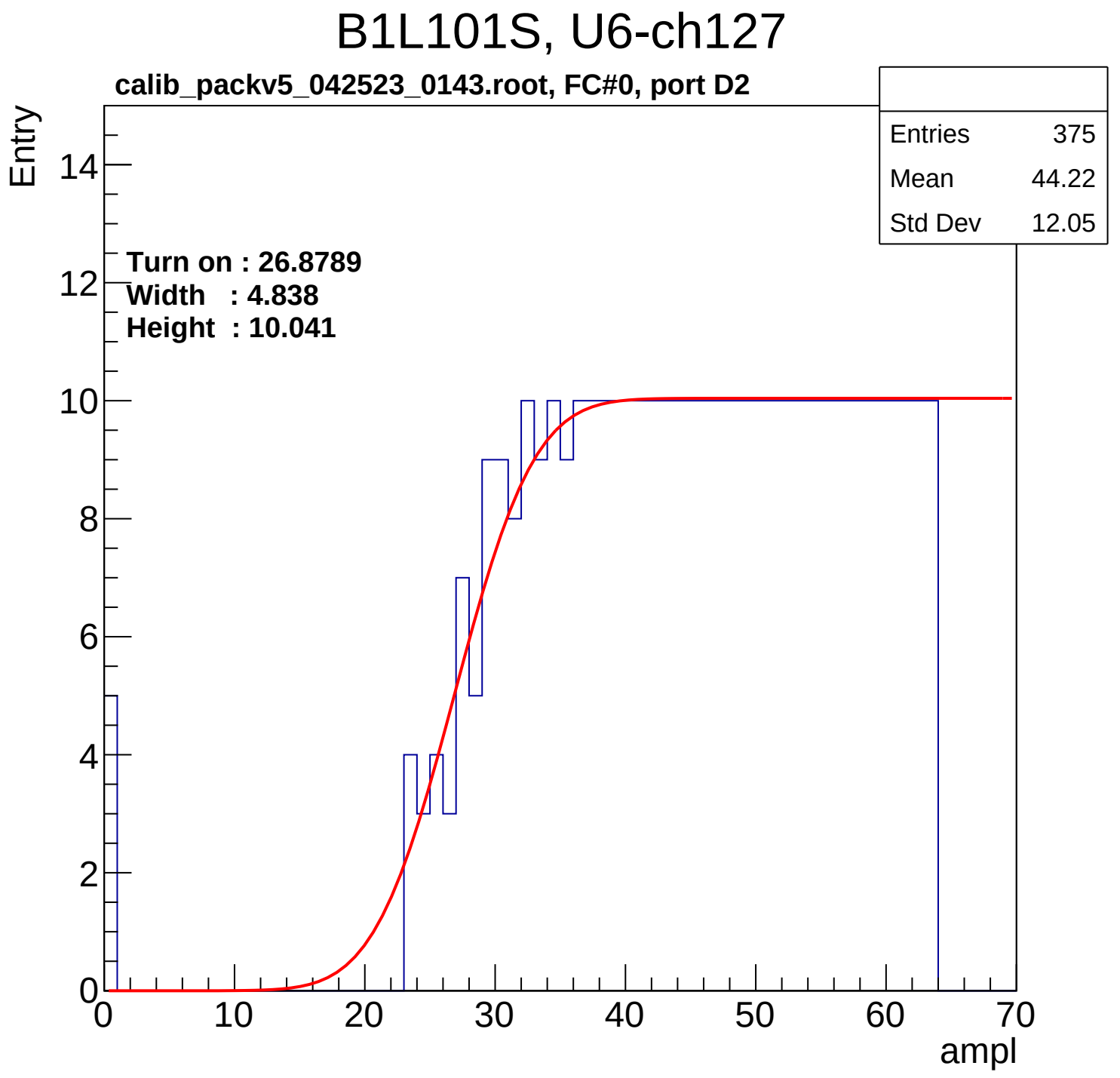

B1L101S, U6-ch123
calib_packv5_042523_0143.root, FC#0, port D2
Entries 368
Mean 44.9
Std Dev 11.06
Turn on : 28.3932
Width : 3.743
Height : 10.100
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L101S, U6-ch124
calib_packv5_042523_0143.root, FC#0, port D2
Entries 380
Mean 44.15
Std Dev 11.85
Turn on : 26.8439
Width : 2.152
Height : 10.019
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L101S, U6-ch125
calib_packv5_042523_0143.root, FC#0, port D2
Entries 365
Mean 45.09
Std Dev 10.89
Turn on : 27.7580
Width : 2.425
Height : 10.014
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L101S, U6-ch126
calib_packv5_042523_0143.root, FC#0, port D2
Entries 393
Mean 43.63
Std Dev 11.84
Turn on : 24.8137
Width : 2.387
Height : 9.928
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L101S, U6-ch127
calib_packv5_042523_0143.root, FC#0, port D2
Entries 375
Mean 44.22
Std Dev 12.05
Turn on : 26.8789
Width : 4.838
Height : 10.041
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L101S, U6-ch127
calib_packv5_042523_0143.root, FC#0, port D2
Entries 375
Mean 44.22
Std Dev 12.05
Turn on : 26.8789
Width : 4.838
Height : 10.041
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70