



# B0L001S, U20-ch0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	354
Mean	45.43
Std Dev	11.13

Turn on : 29.2770

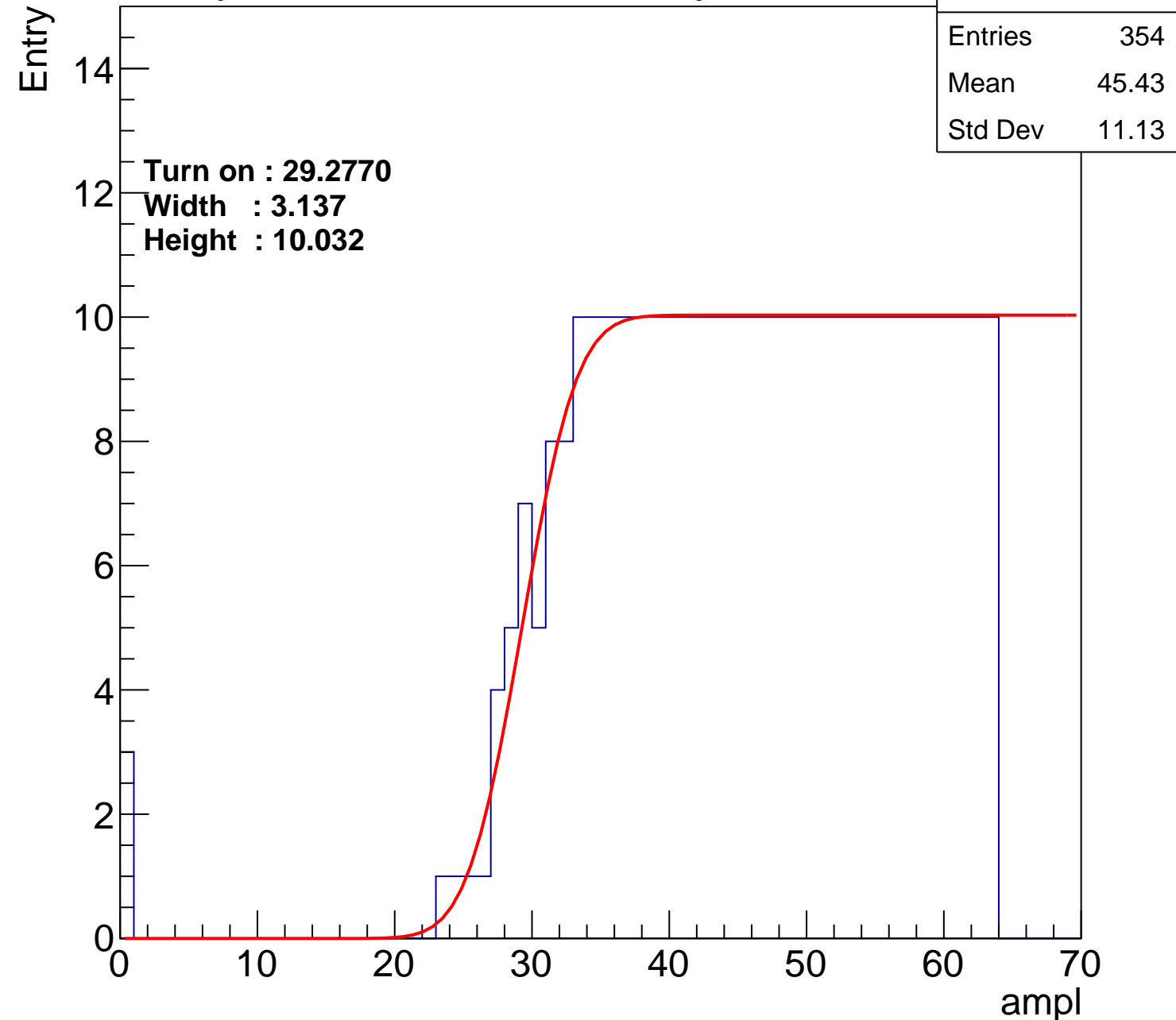
Width : 3.137

Height : 10.032

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	356
Mean	45.41
Std Dev	11.06

**Turn on : 29.1643**

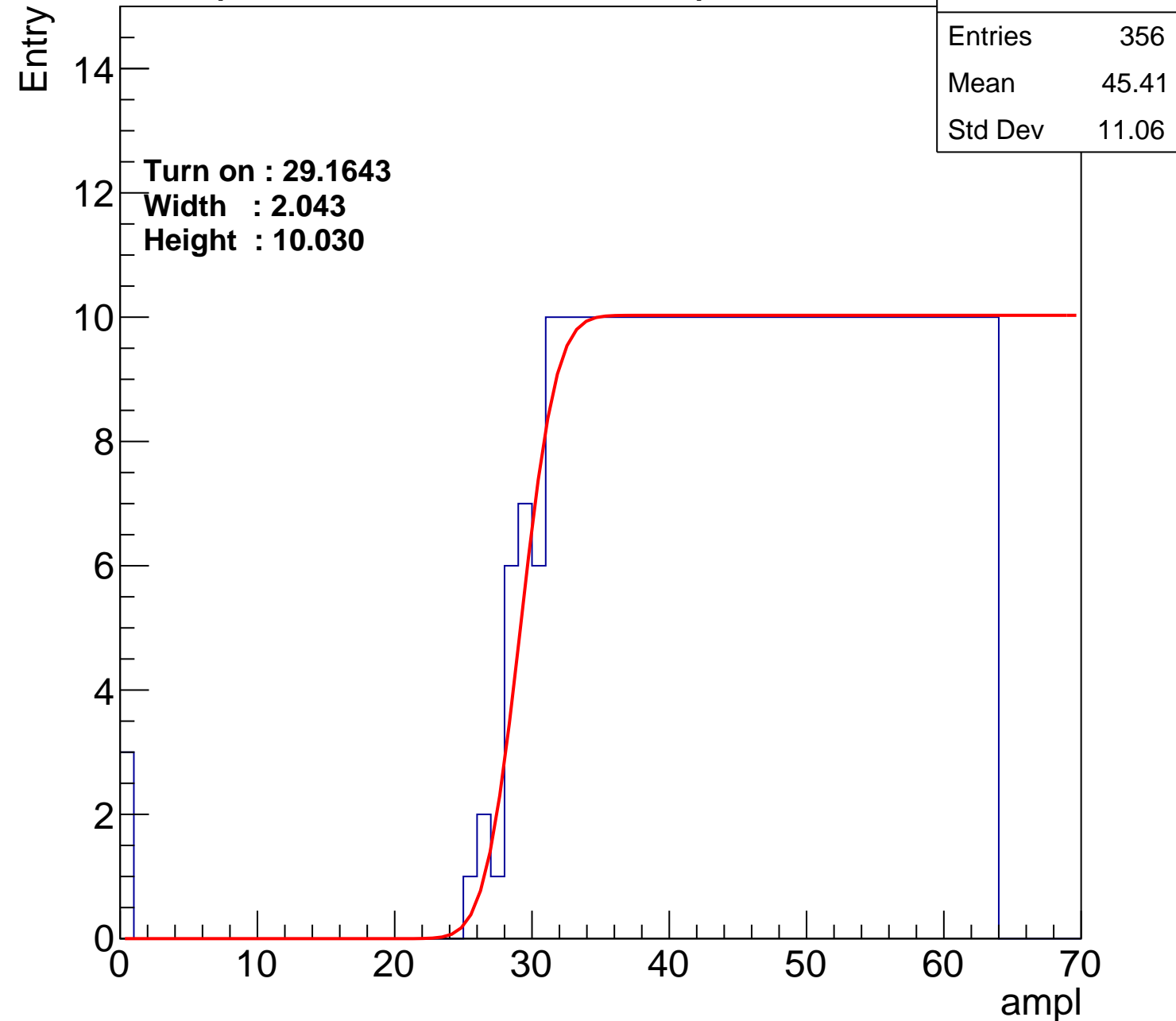
**Width : 2.043**

**Height : 10.030**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	362
Mean	45.1
Std Dev	11.23

**Turn on : 28.1777**

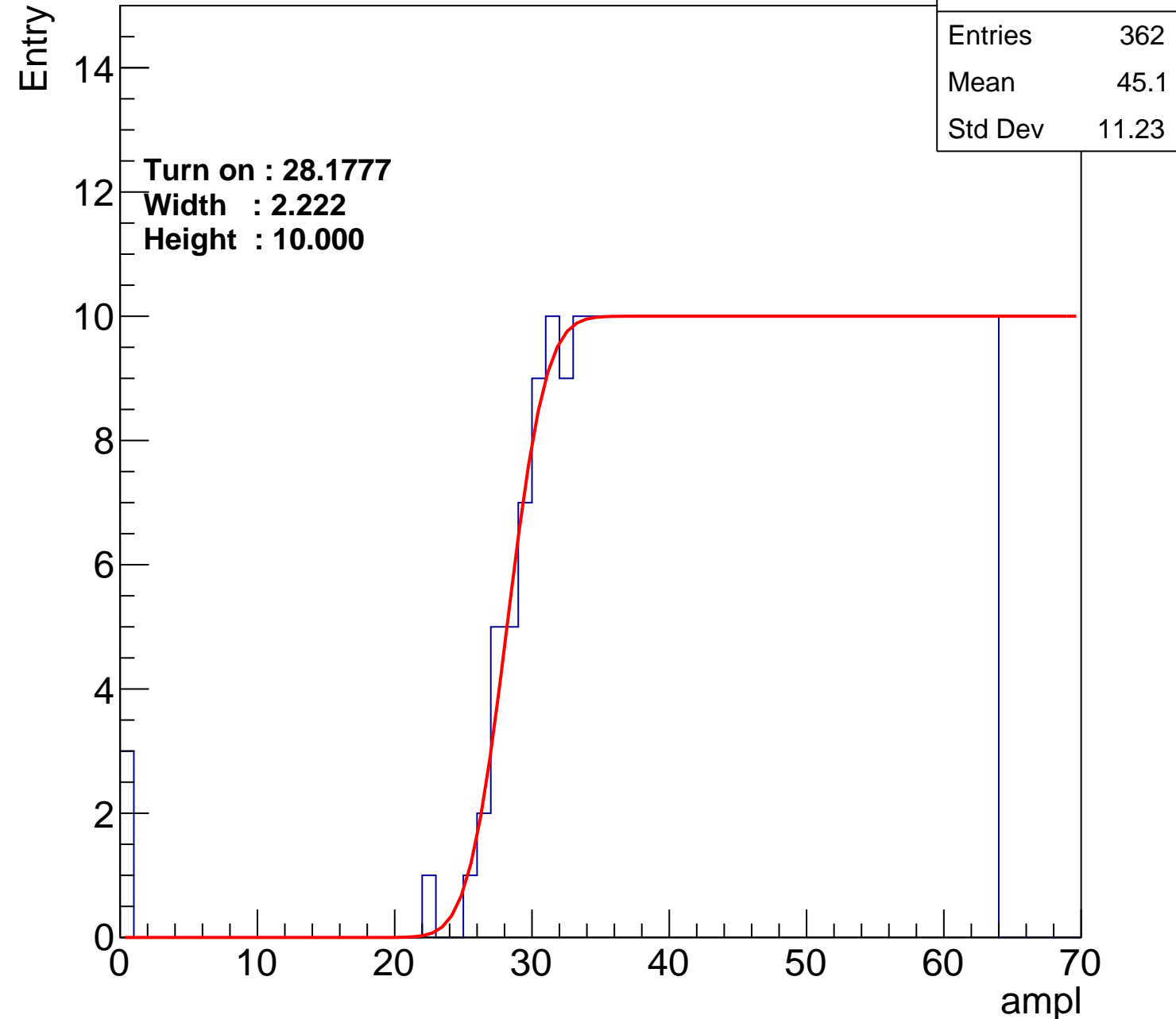
**Width : 2.222**

**Height : 10.000**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch3

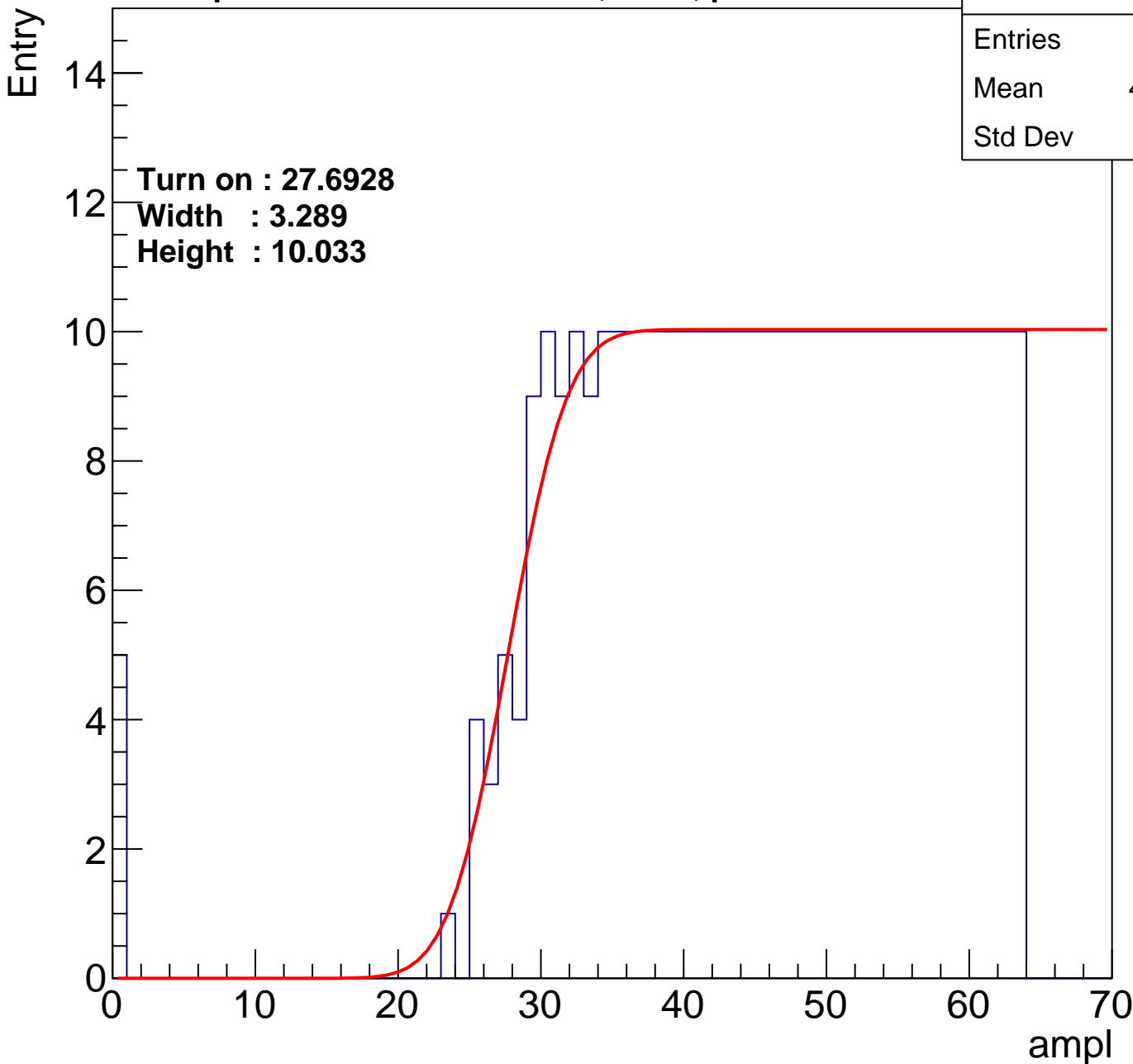
**calib\_packv5\_042523\_0143.root, FC#9, port A1**

Entries	369
Mean	44.59
Std Dev	11.81

**Turn on : 27.6928**

**Width : 3.289**

**Height : 10.033**



# B0L001S, U20-ch4

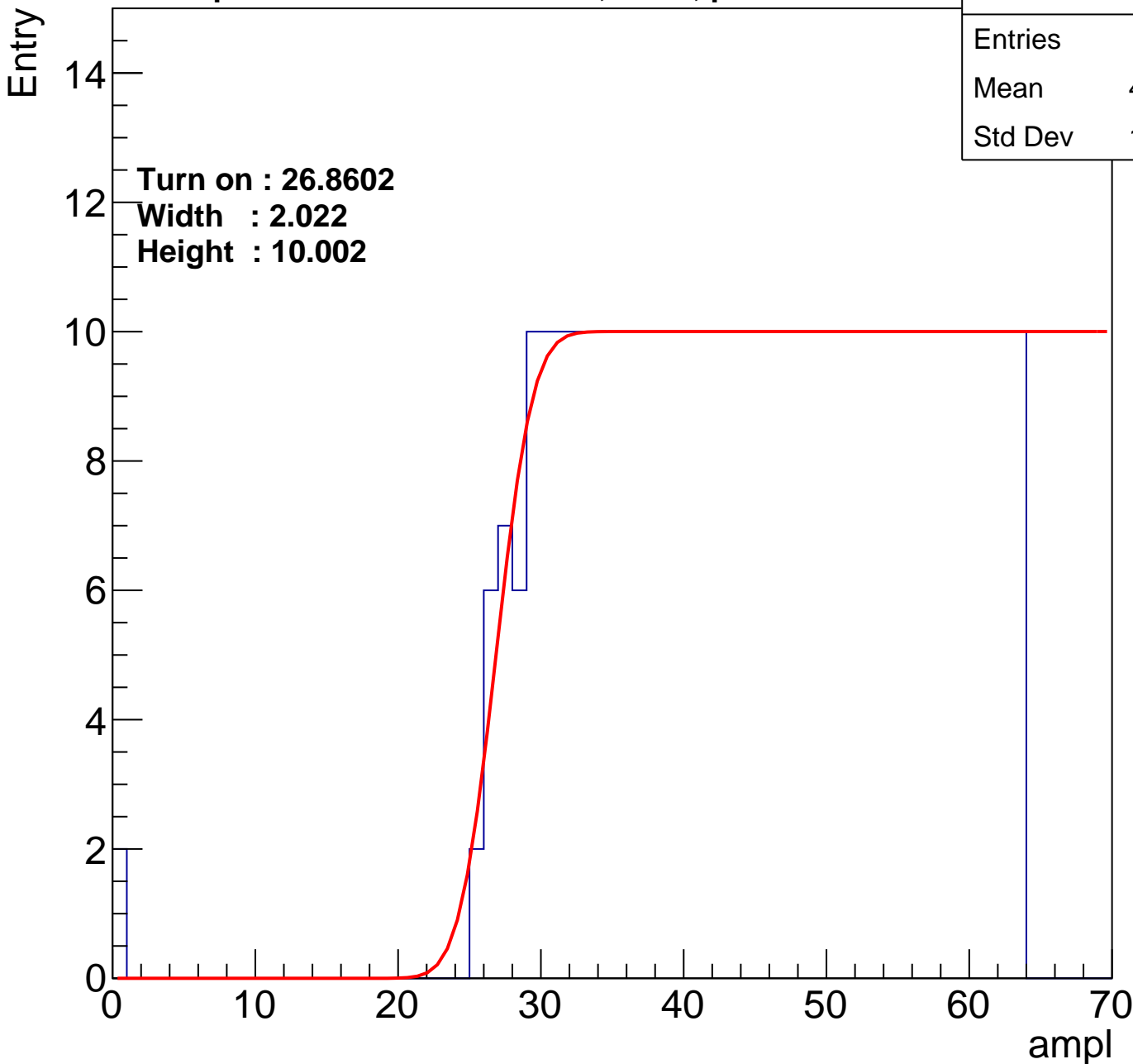
**calib\_packv5\_042523\_0143.root, FC#9, port A1**

Entries	373
Mean	44.67
Std Dev	11.23

**Turn on : 26.8602**

**Width : 2.022**

**Height : 10.002**



# B0L001S, U20-ch5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	337
Mean	46.39
Std Dev	10.42

**Turn on : 30.8988**

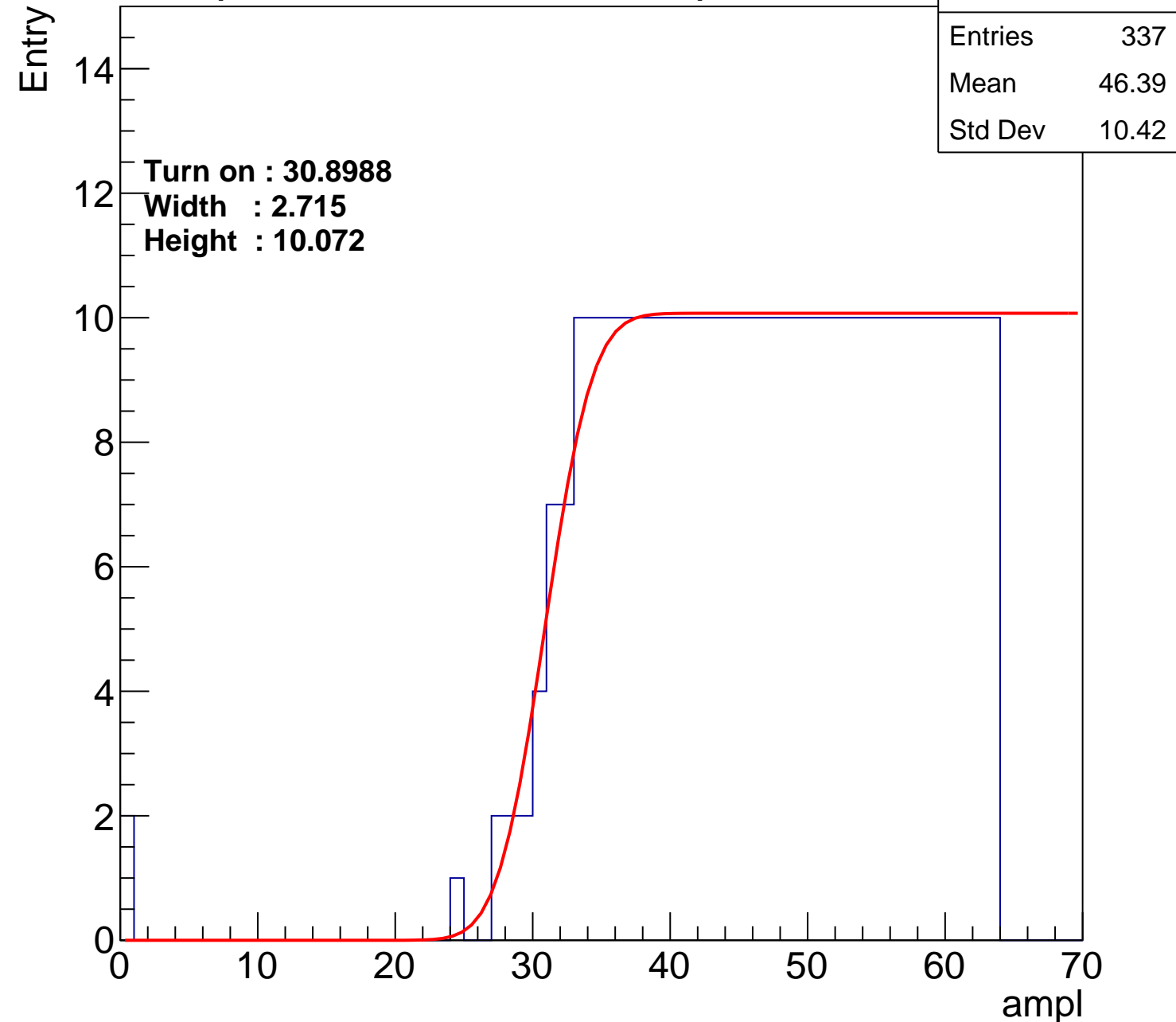
**Width : 2.715**

**Height : 10.072**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch6

**calib\_packv5\_042523\_0143.root, FC#9, port A1**

Entries	359
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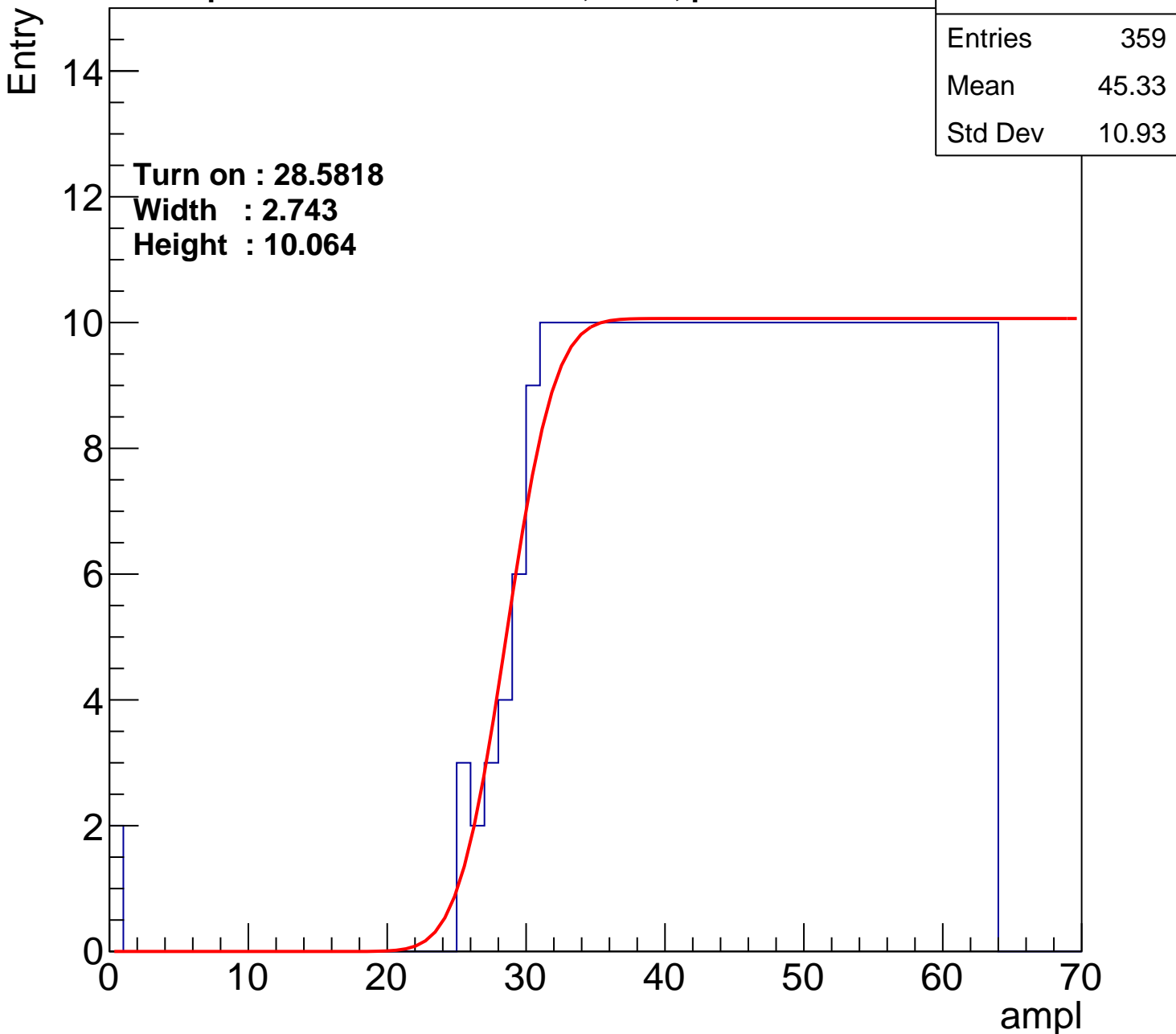
Mean	45.33
------	-------

Std Dev	10.93
---------	-------

**Turn on : 28.5818**

**Width : 2.743**

**Height : 10.064**





# B0L001S, U20-ch7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	362
Mean	45.21
Std Dev	11.04

Turn on : 28.0172

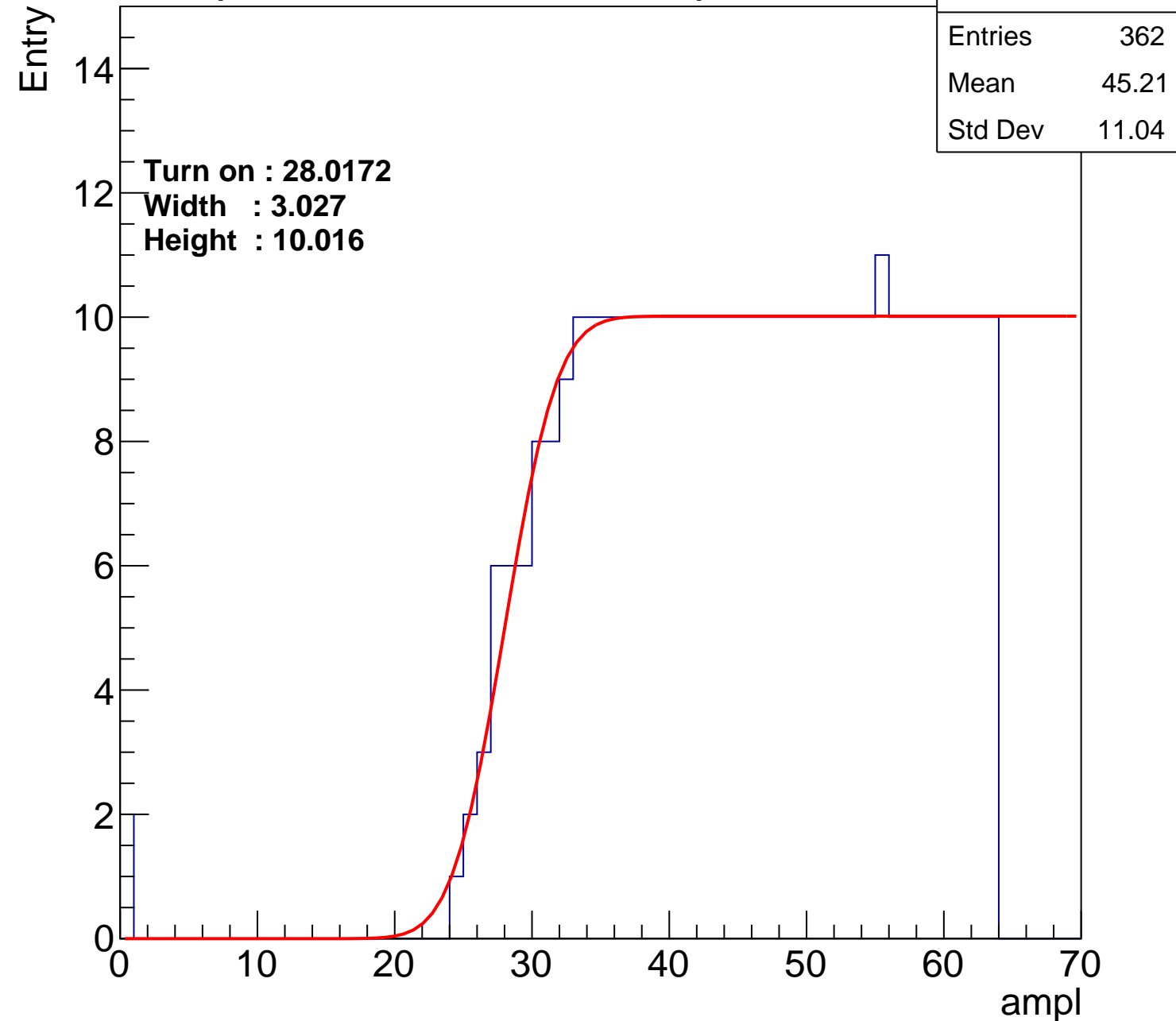
Width : 3.027

Height : 10.016

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch8

calib\_packv5\_042523\_0143.root, FC#9, port A1

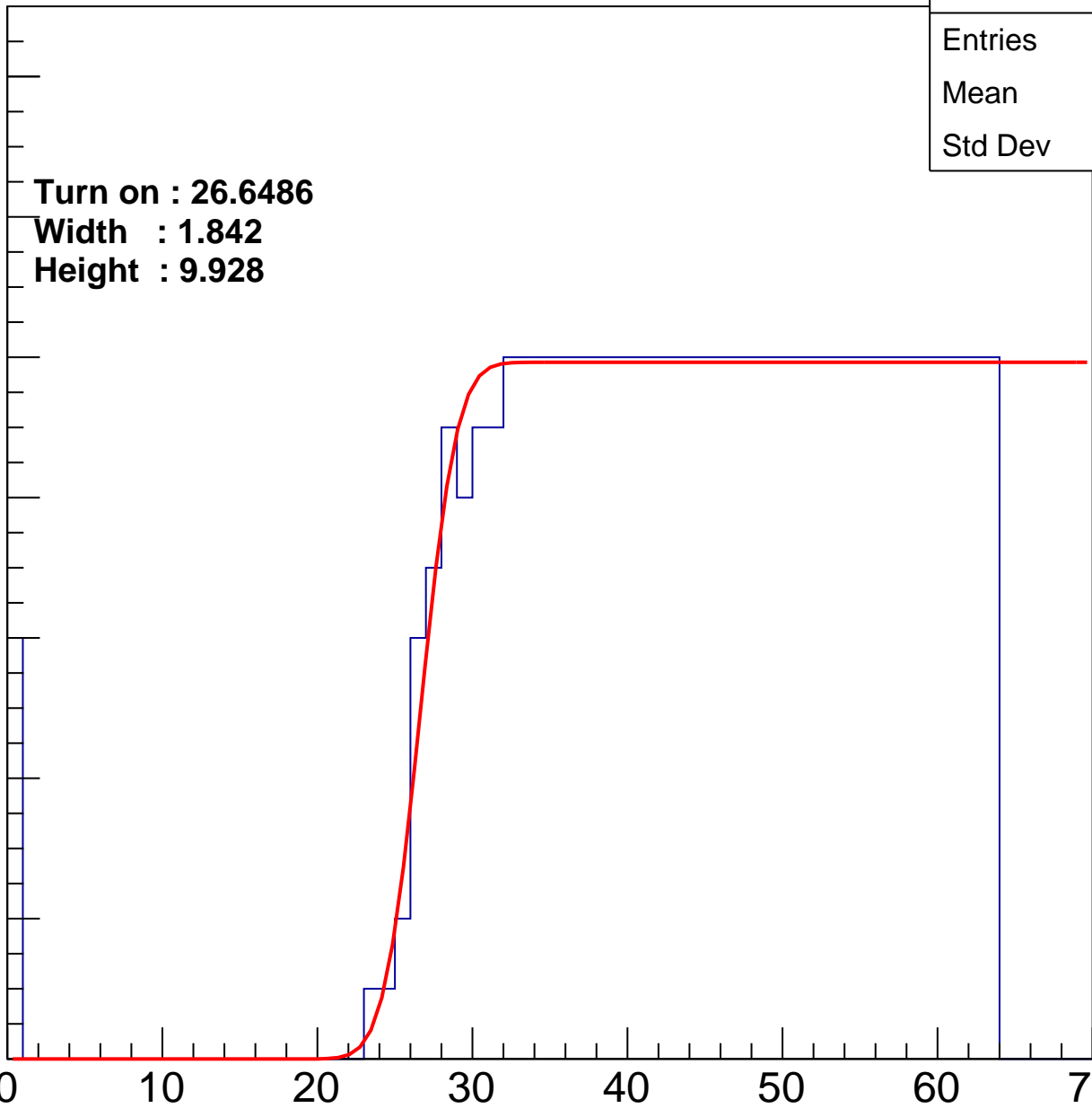
Entry

14  
12  
10  
8  
6  
4  
2  
0

Turn on : 26.6486  
Width : 1.842  
Height : 9.928

Entries	378
Mean	44.11
Std Dev	12.14

ampl



# B0L001S, U20-ch9

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	379
Mean	44.37
Std Dev	11.6

Turn on : 27.0224

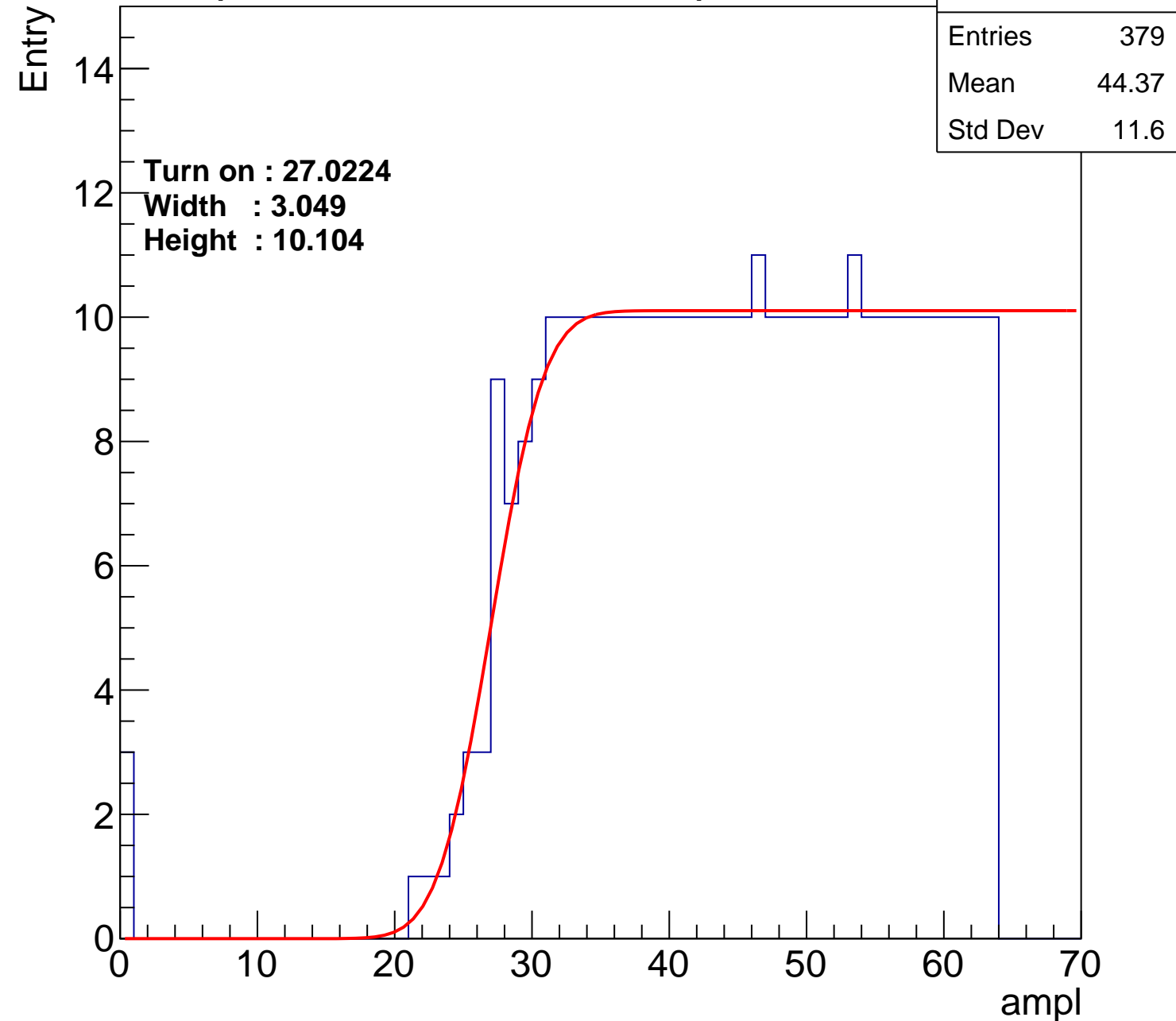
Width : 3.049

Height : 10.104

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch10

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	346
Mean	45.94
Std Dev	10.65

Turn on : 29.1699

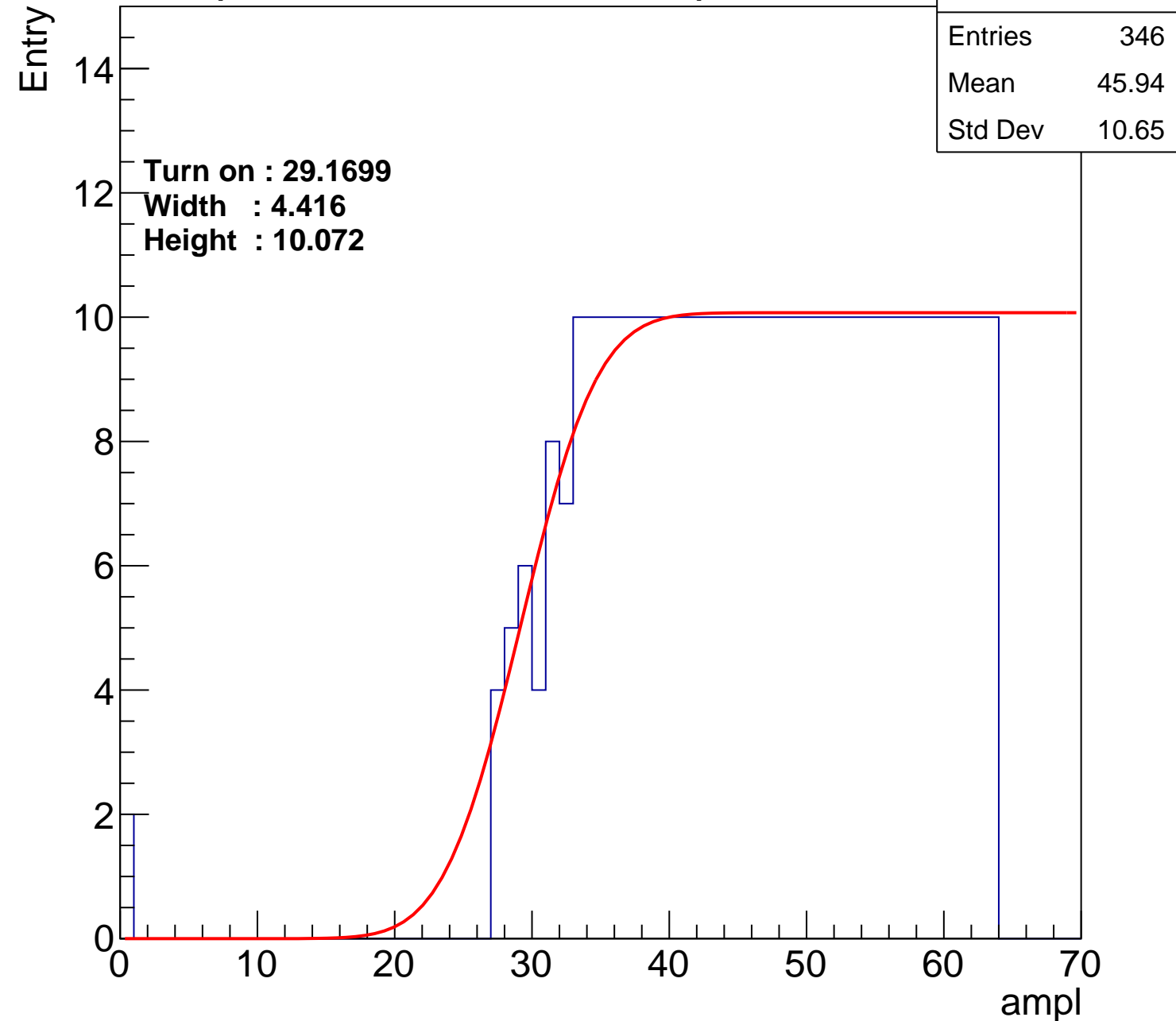
Width : 4.416

Height : 10.072

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch11

calib\_packv5\_042523\_0143.root, FC#9, port A1

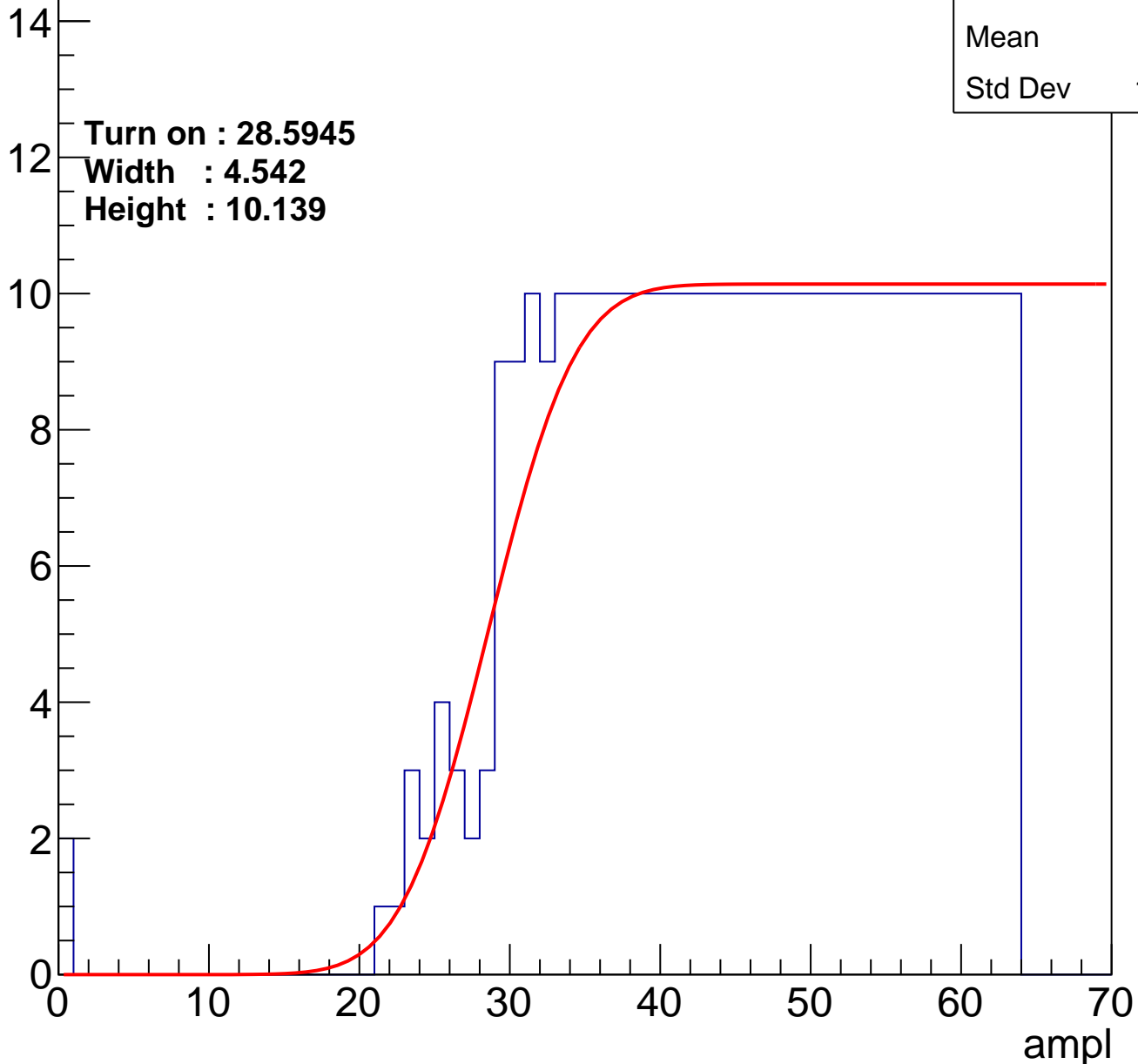
Entries	368
Mean	44.8
Std Dev	11.31

Turn on : 28.5945

Width : 4.542

Height : 10.139

Entry



# B0L001S, U20-ch12

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	374
Mean	44.53
Std Dev	11.41

Turn on : 27.4177

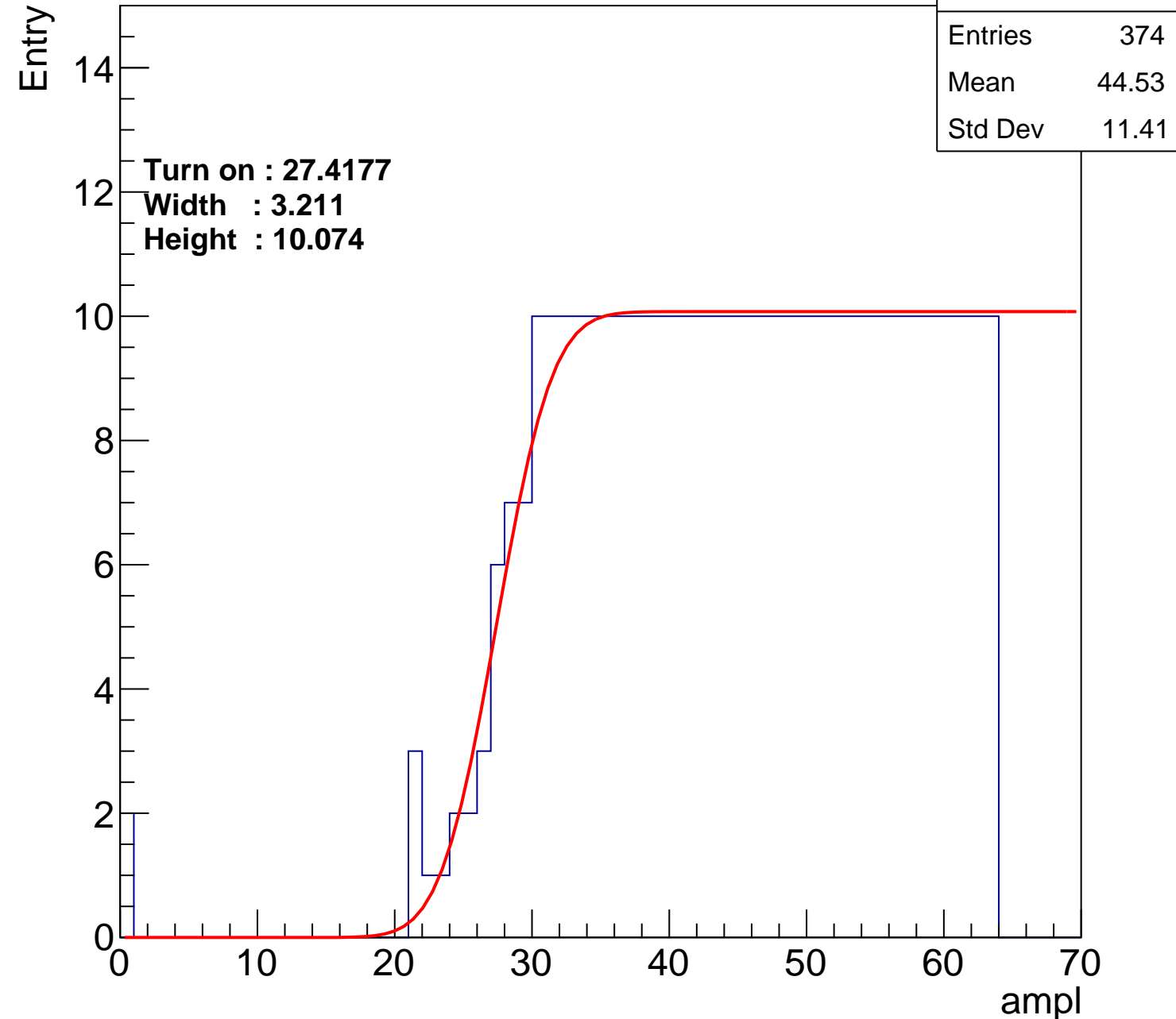
Width : 3.211

Height : 10.074

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch13

calib\_packv5\_042523\_0143.root, FC#9, port A1

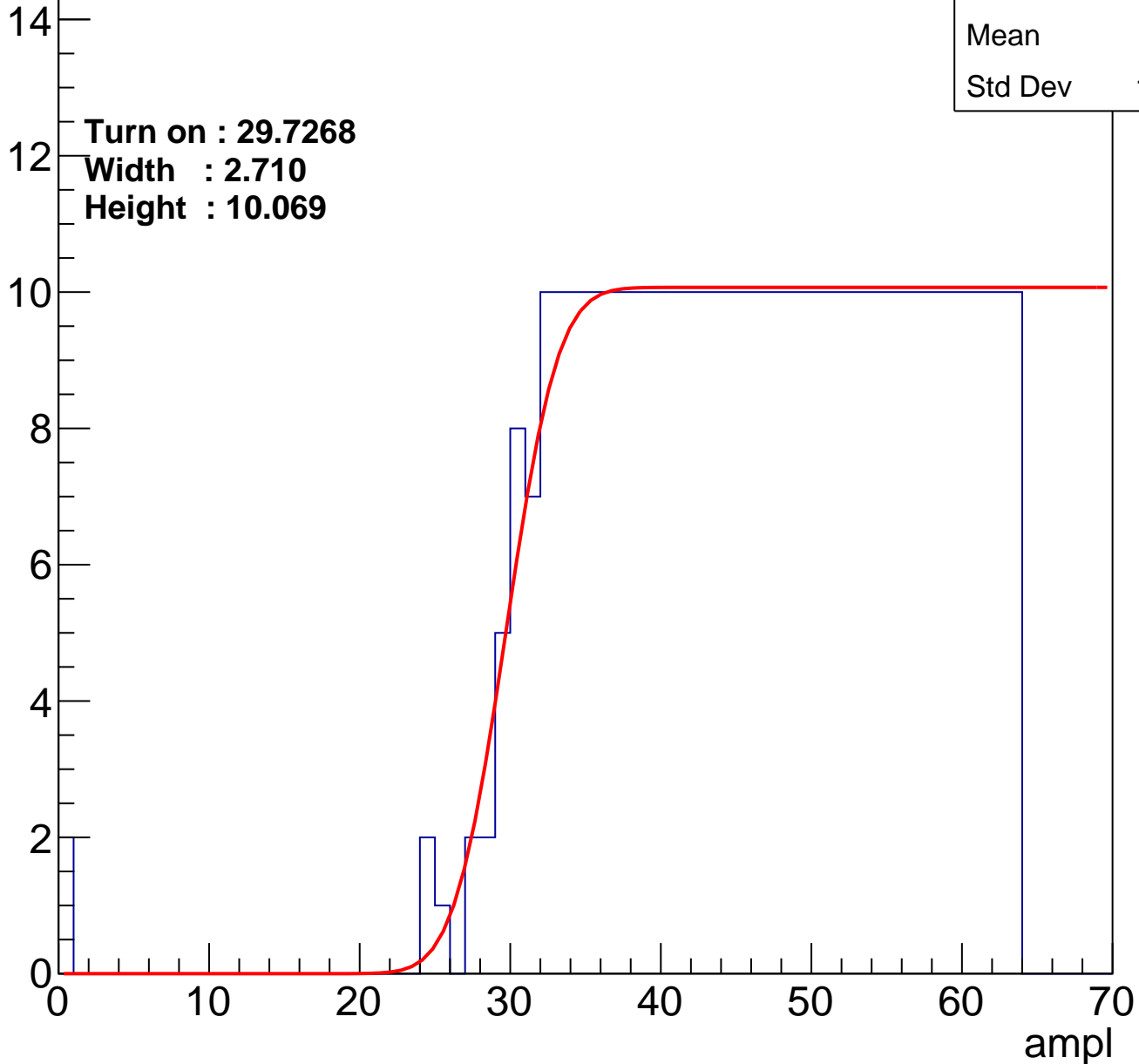
Entries	349
Mean	45.8
Std Dev	10.71

**Turn on : 29.7268**

**Width : 2.710**

**Height : 10.069**

Entry



# B0L001S, U20-ch14

calib\_packv5\_042523\_0143.root, FC#9, port A1

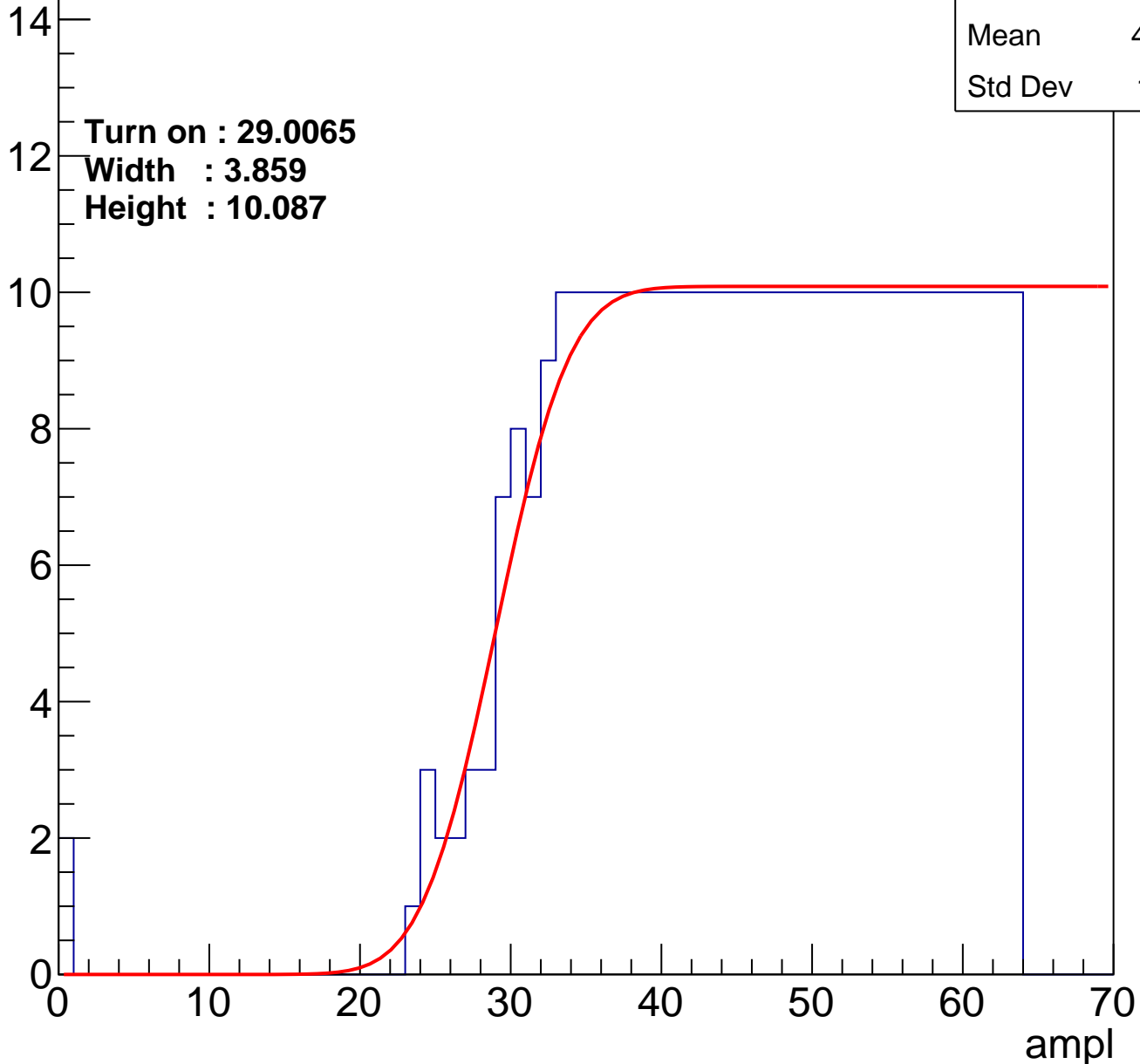
Entries	357
Mean	45.35
Std Dev	11.01

Turn on : 29.0065

Width : 3.859

Height : 10.087

Entry





# B0L001S, U20-ch15

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	376
Mean	44.51
Std Dev	11.25

**Turn on : 26.4855**

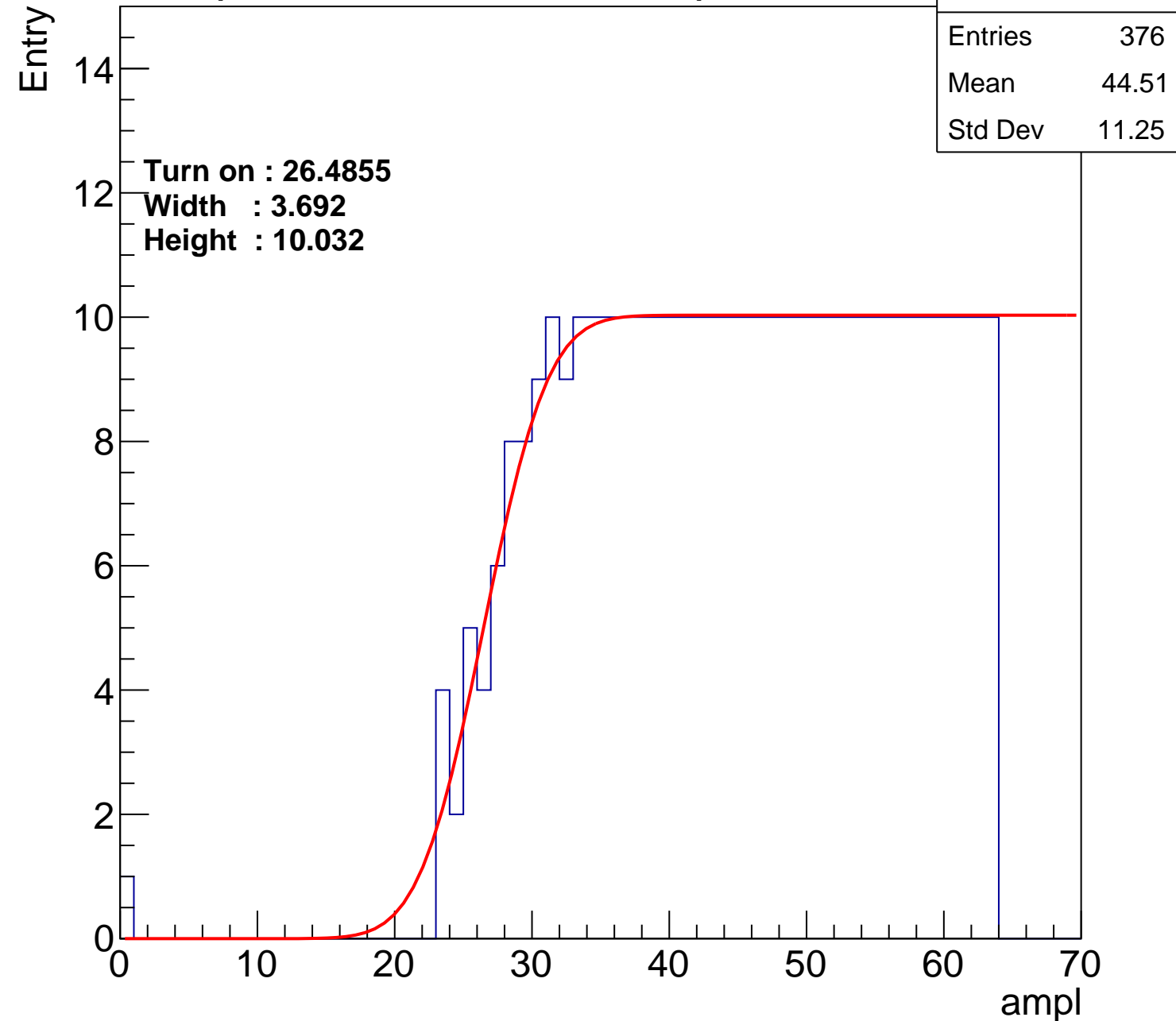
**Width : 3.692**

**Height : 10.032**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch16

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	344
Mean	46.06
Std Dev	10.44

Turn on : 30.1333

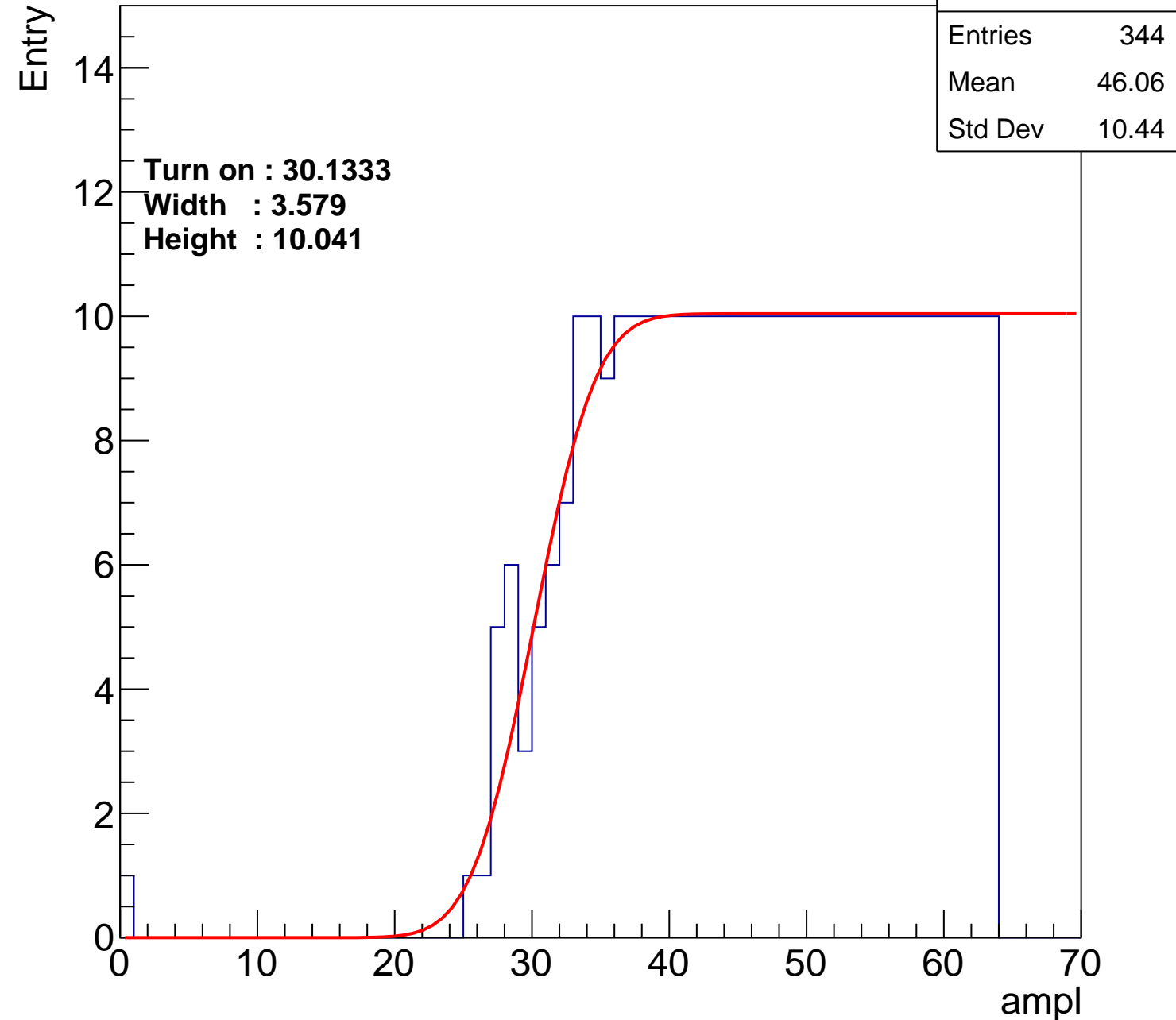
Width : 3.579

Height : 10.041

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch17

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	356
Mean	45.22
Std Dev	11.45

Turn on : 28.9114

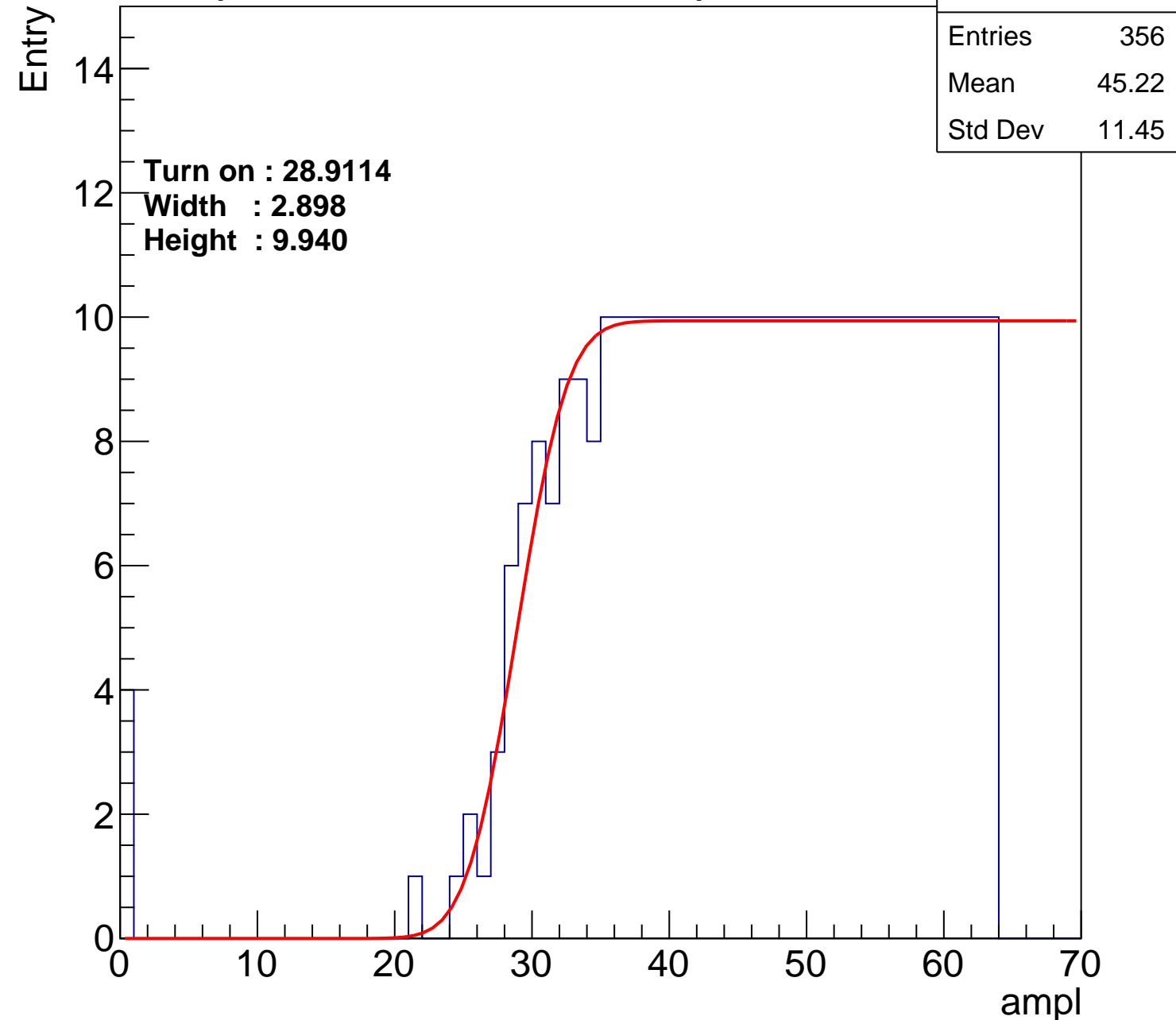
Width : 2.898

Height : 9.940

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch18

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	360
Mean	45.18
Std Dev	11.21

**Turn on : 28.7263**

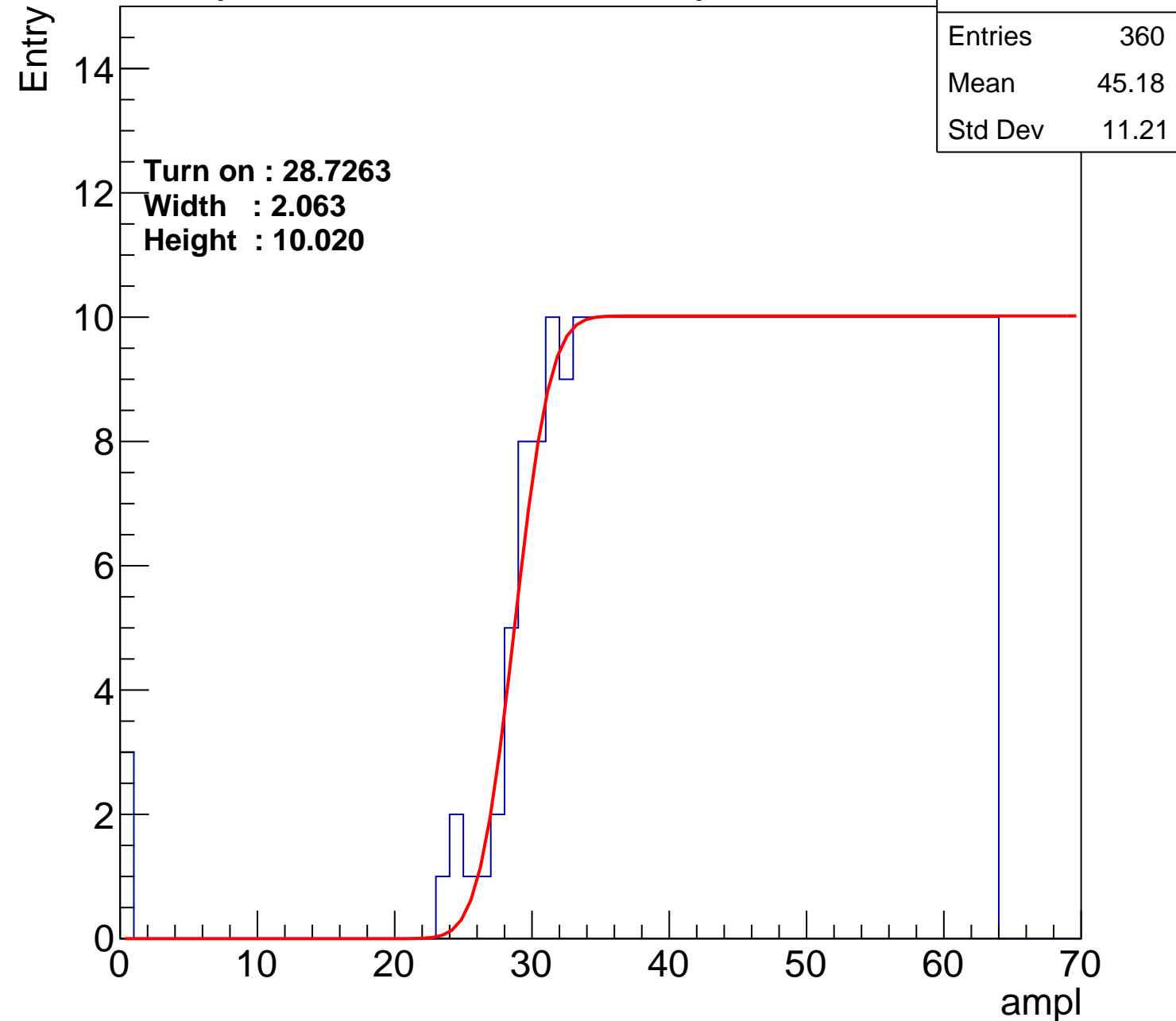
**Width : 2.063**

**Height : 10.020**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch19

calib\_packv5\_042523\_0143.root, FC#9, port A1

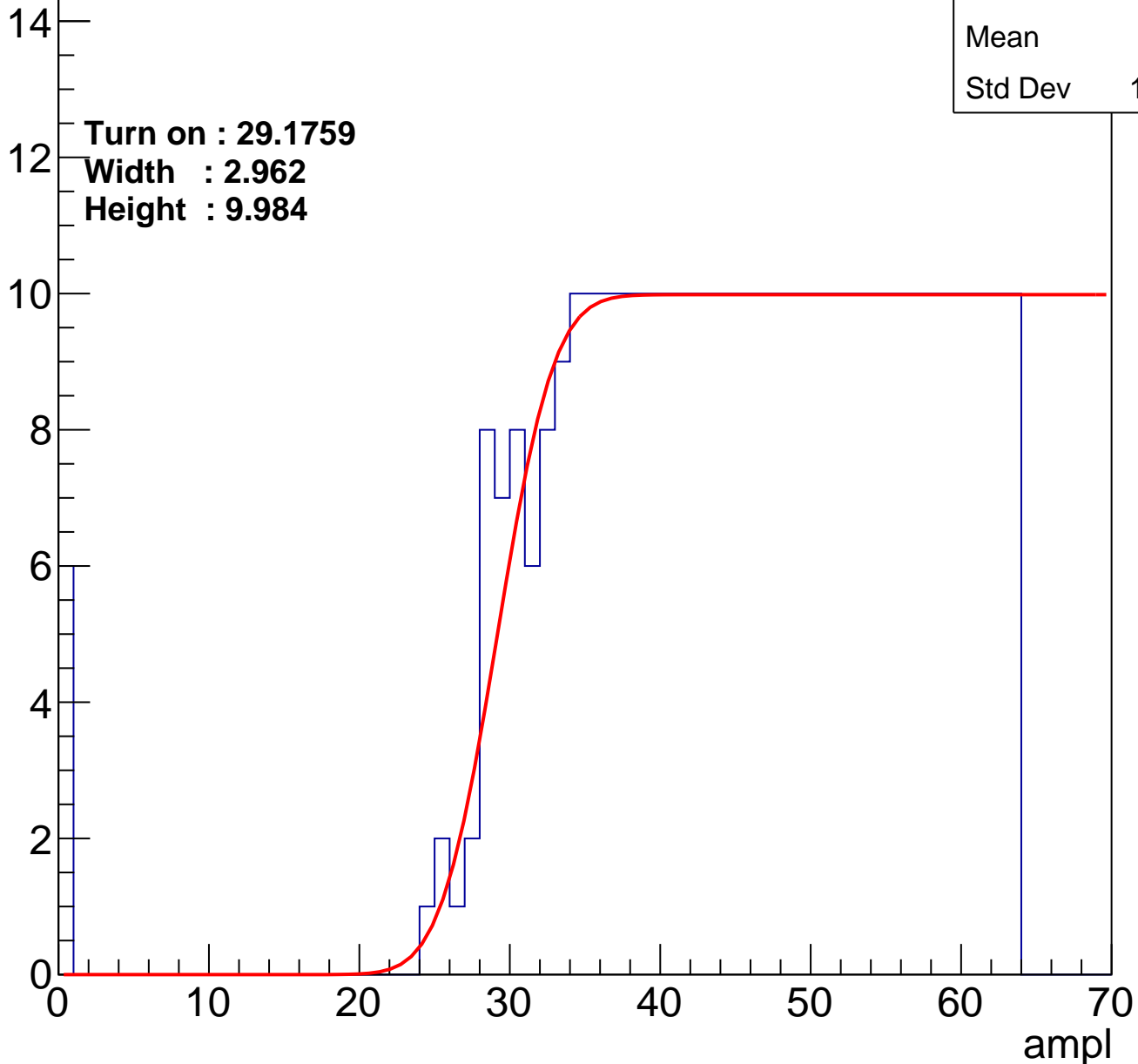
Entries	358
Mean	45
Std Dev	11.85

Turn on : 29.1759

Width : 2.962

Height : 9.984

Entry



# B0L001S, U20-ch20

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	360
Mean	45.21
Std Dev	11.06

Turn on : 28.4820

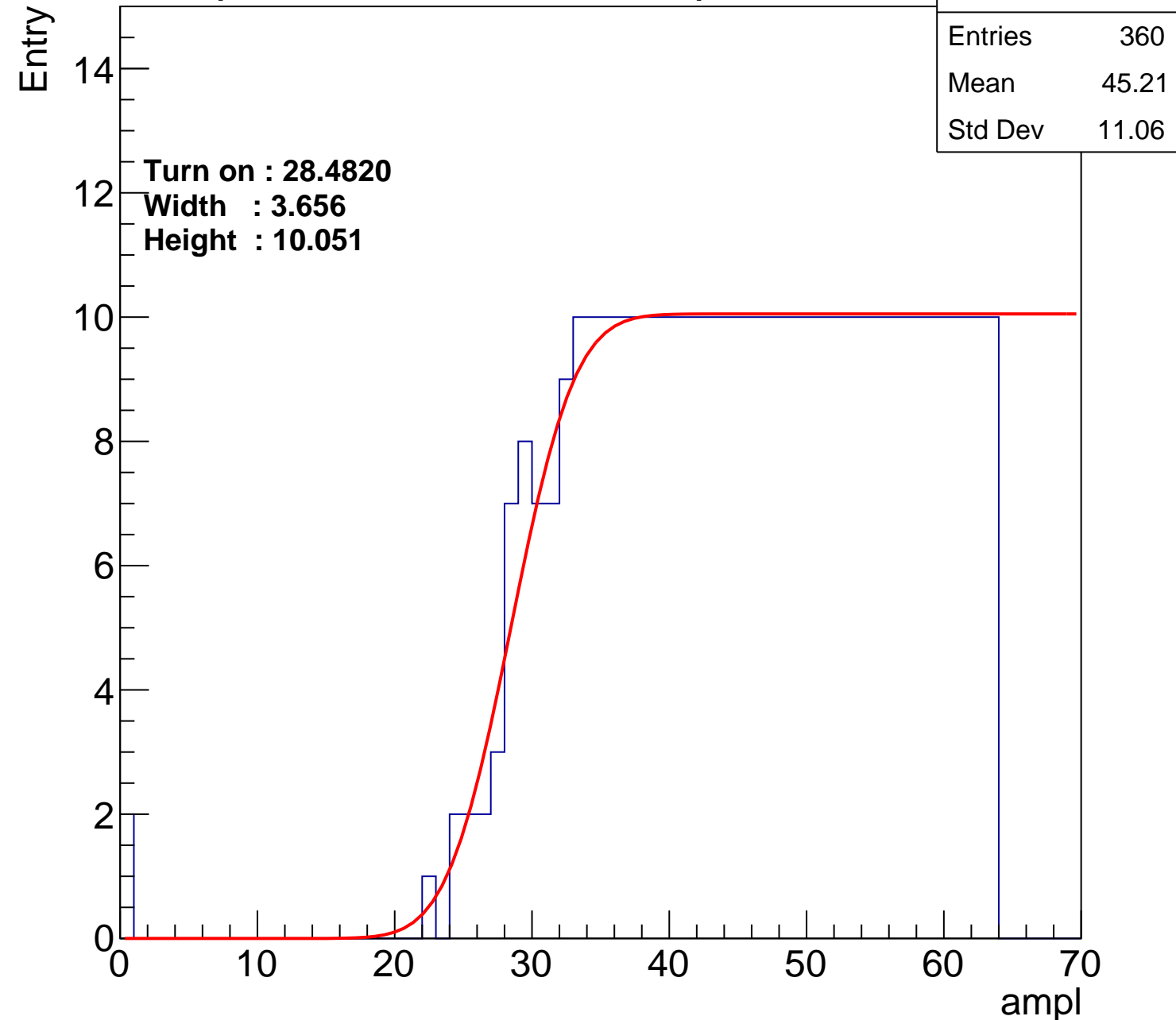
Width : 3.656

Height : 10.051

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch21

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	375
Mean	44.52
Std Dev	11.55

Turn on : 27.2436

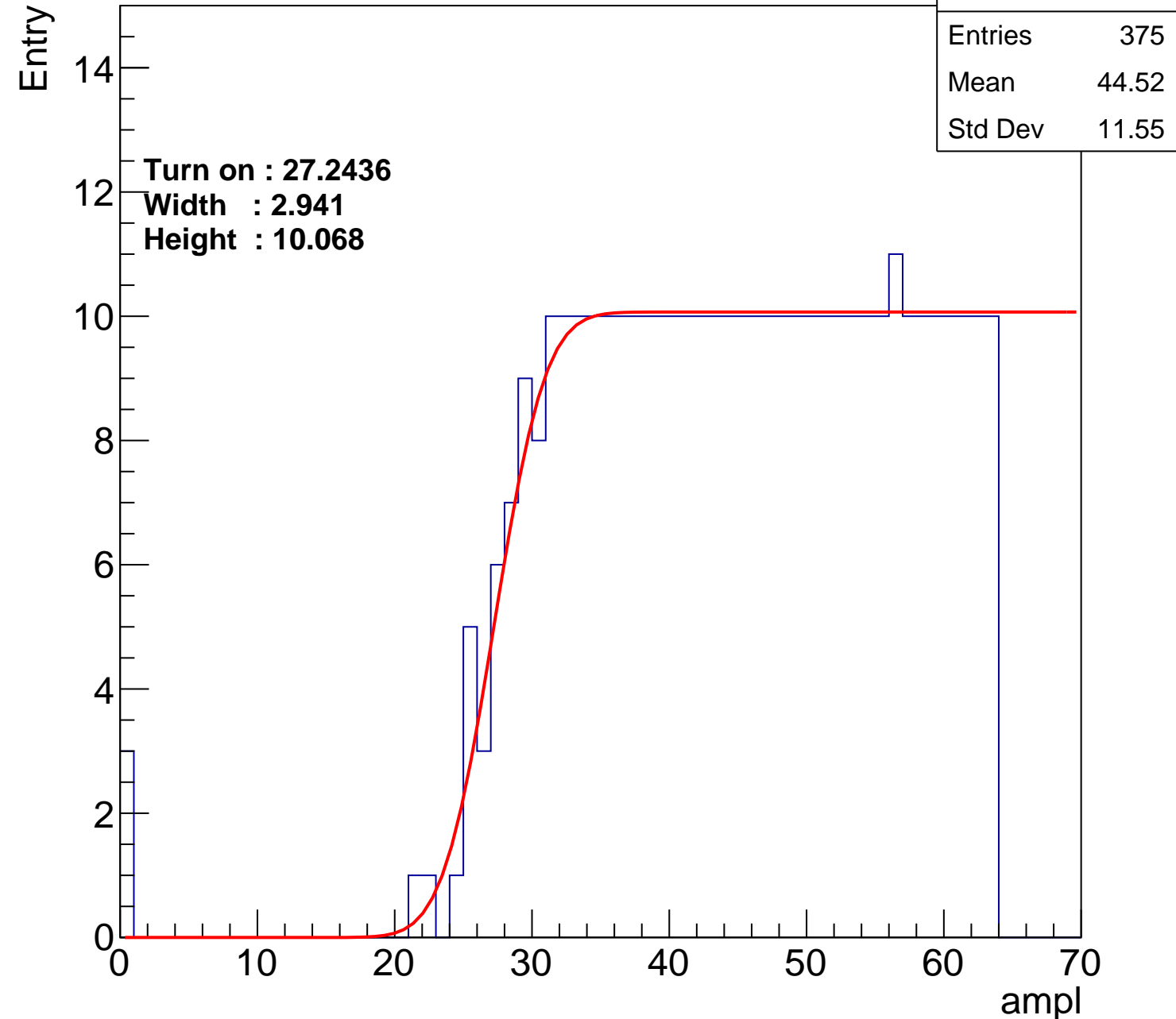
Width : 2.941

Height : 10.068

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch22

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	373
Mean	44.61
Std Dev	11.33

**Turn on : 26.7393**

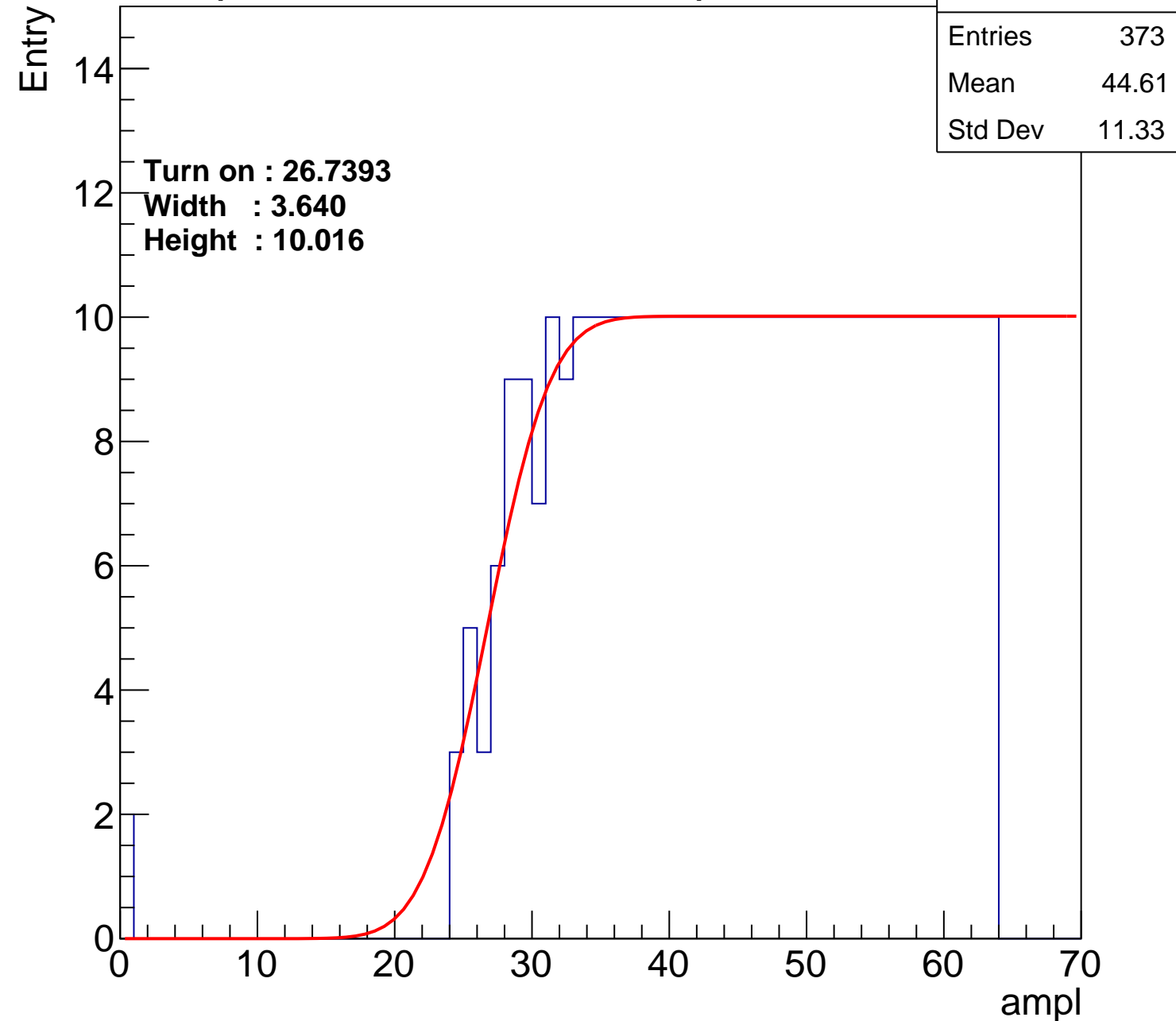
**Width : 3.640**

**Height : 10.016**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L001S, U20-ch23

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	363
Mean	45.02
Std Dev	11.29

**Turn on : 28.1693**

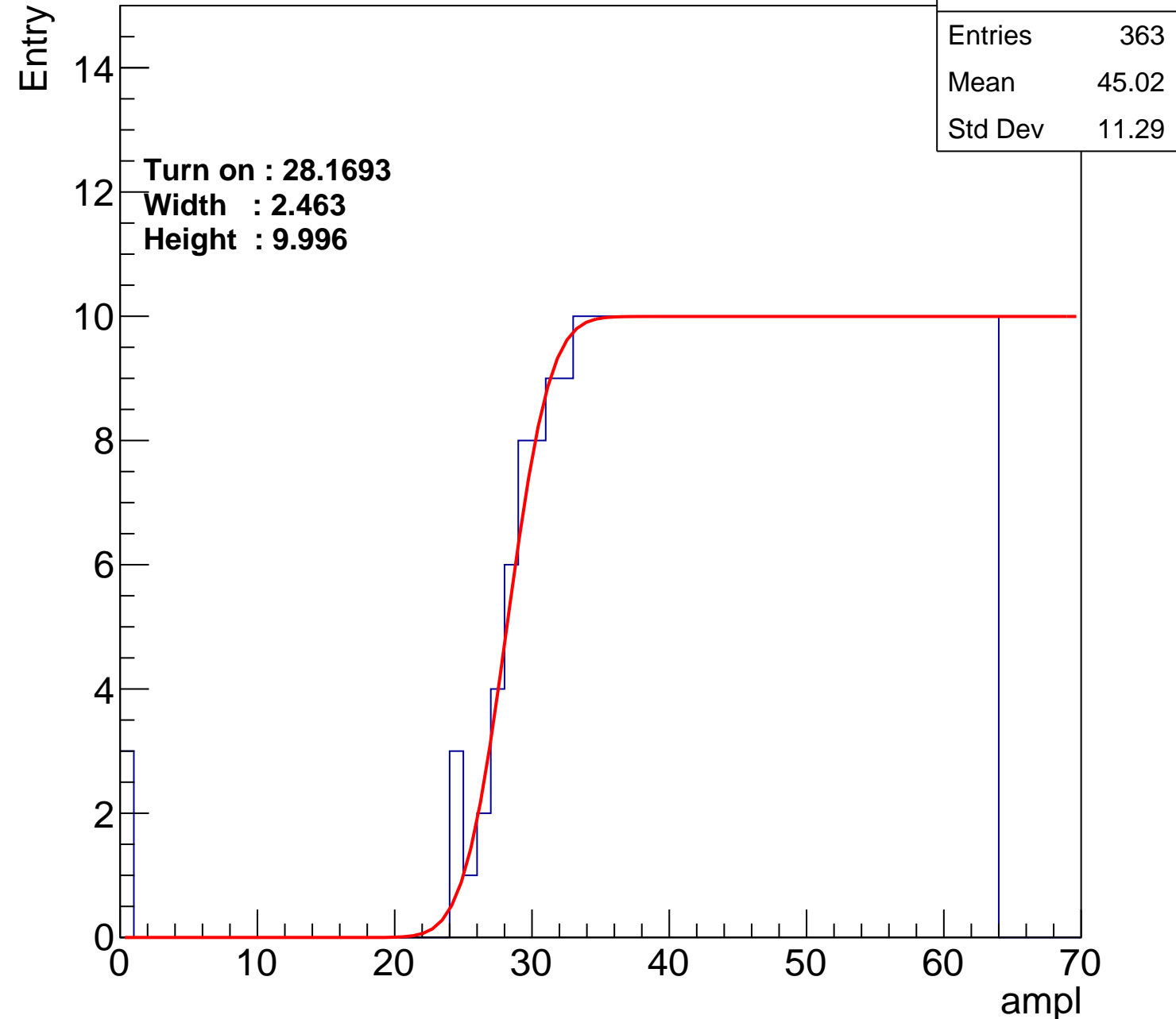
**Width : 2.463**

**Height : 9.996**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch24

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	387
Mean	43.85
Std Dev	11.87

Turn on : 25.7528

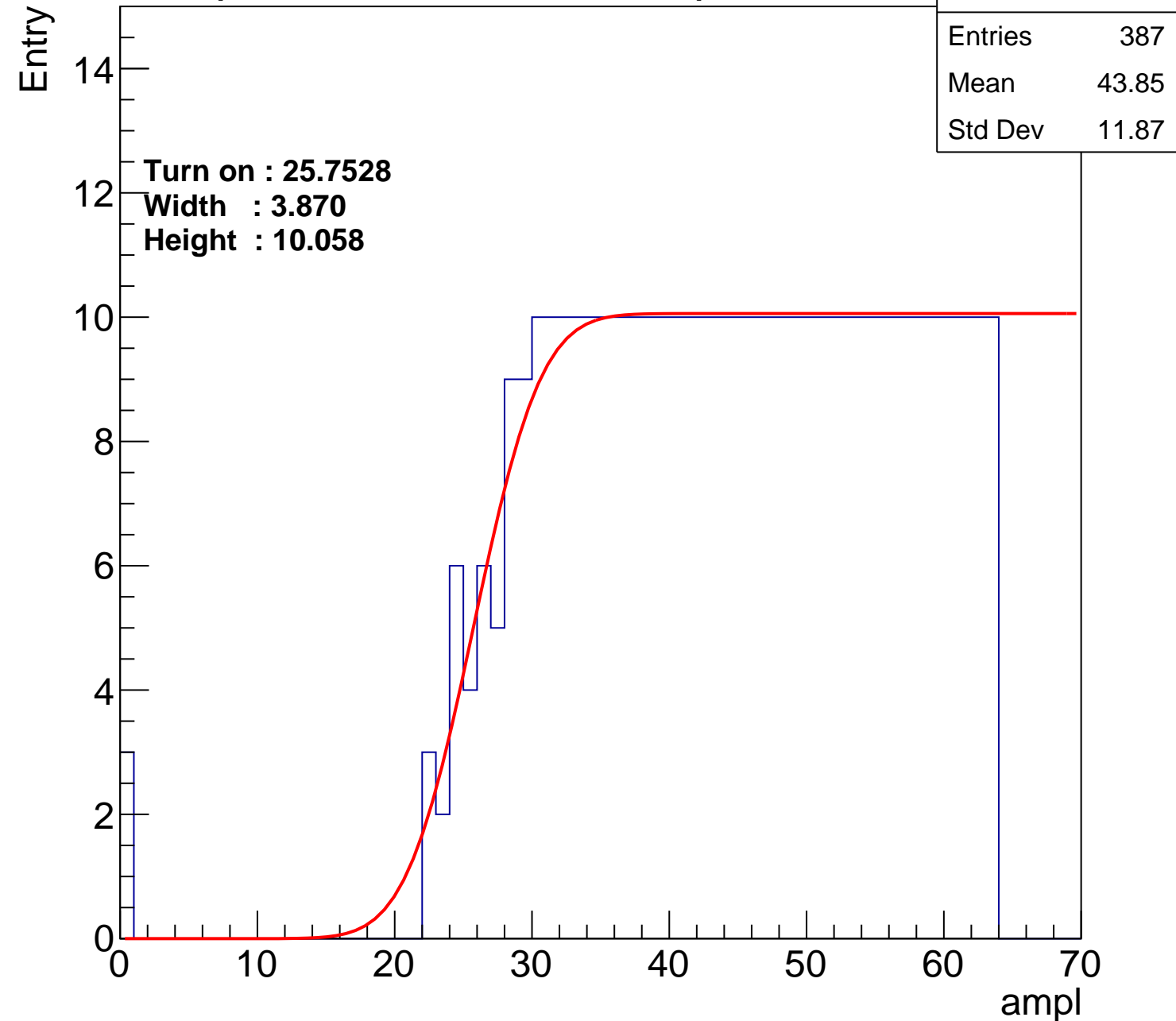
Width : 3.870

Height : 10.058

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch25

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	353
Mean	45.59
Std Dev	10.83

Turn on : 28.8599

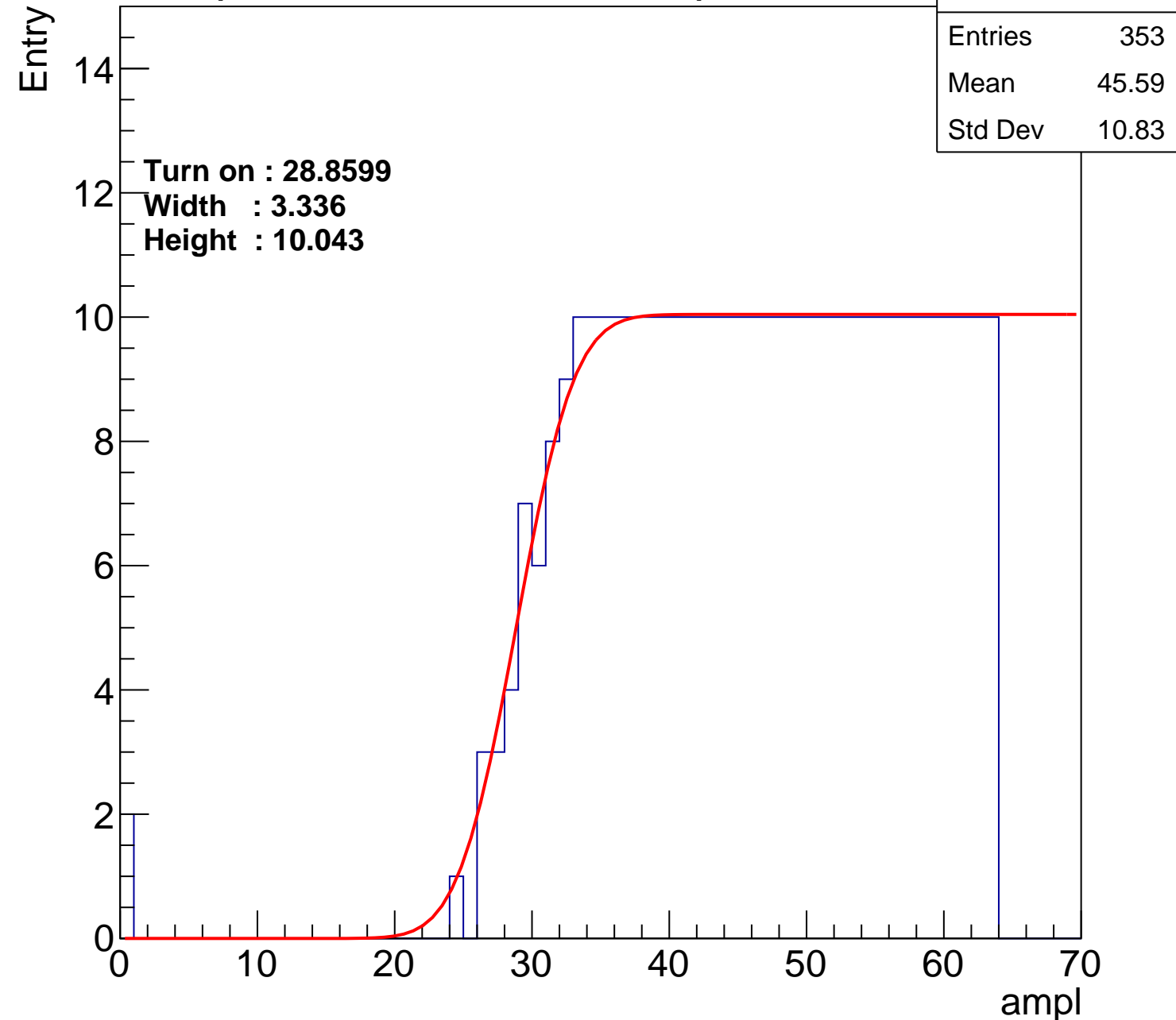
Width : 3.336

Height : 10.043

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch26

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	369
Mean	44.86
Std Dev	11.06

Turn on : 27.3808

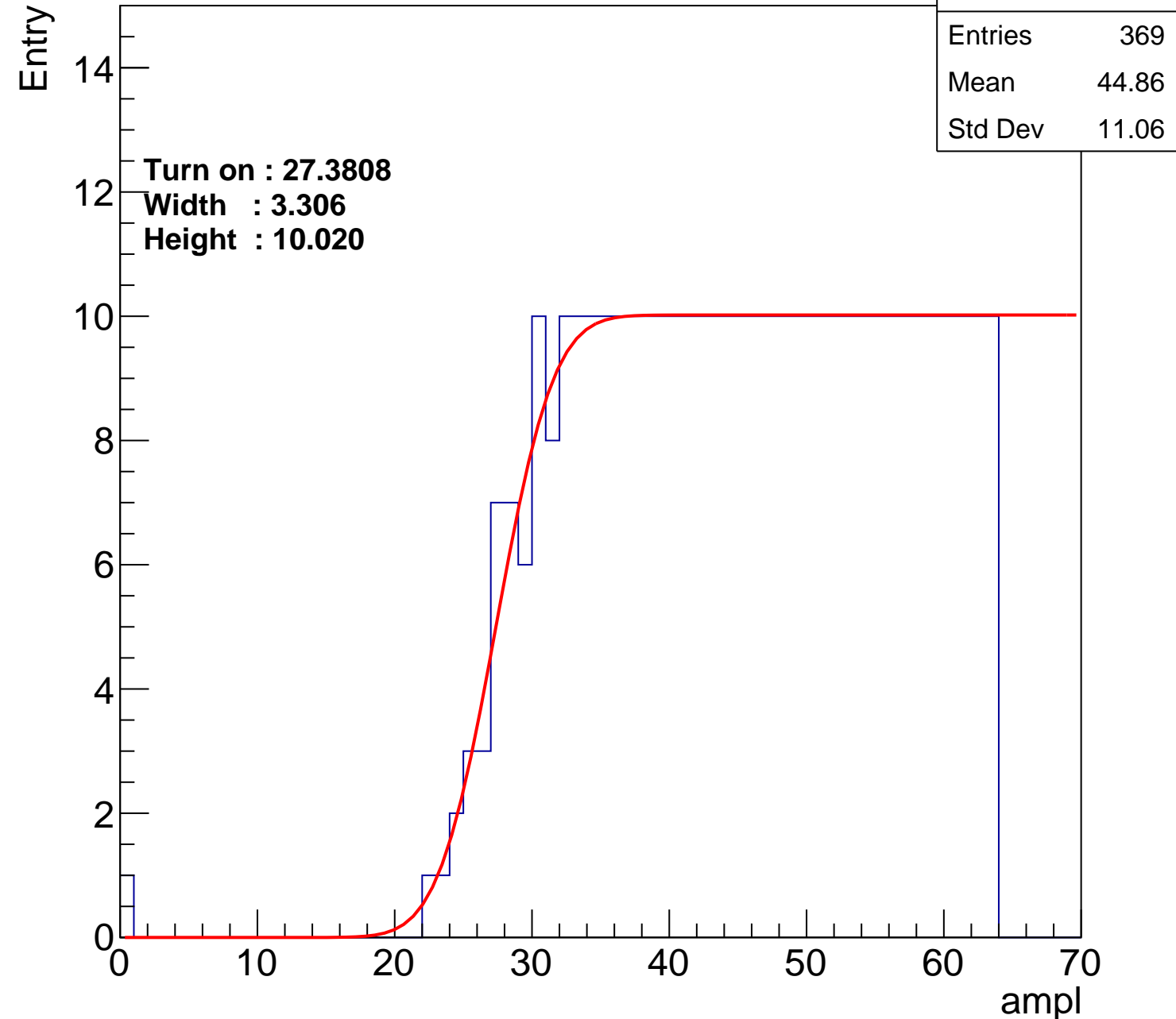
Width : 3.306

Height : 10.020

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch27

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	371
Mean	44.78
Std Dev	11.09

Turn on : 27.1877

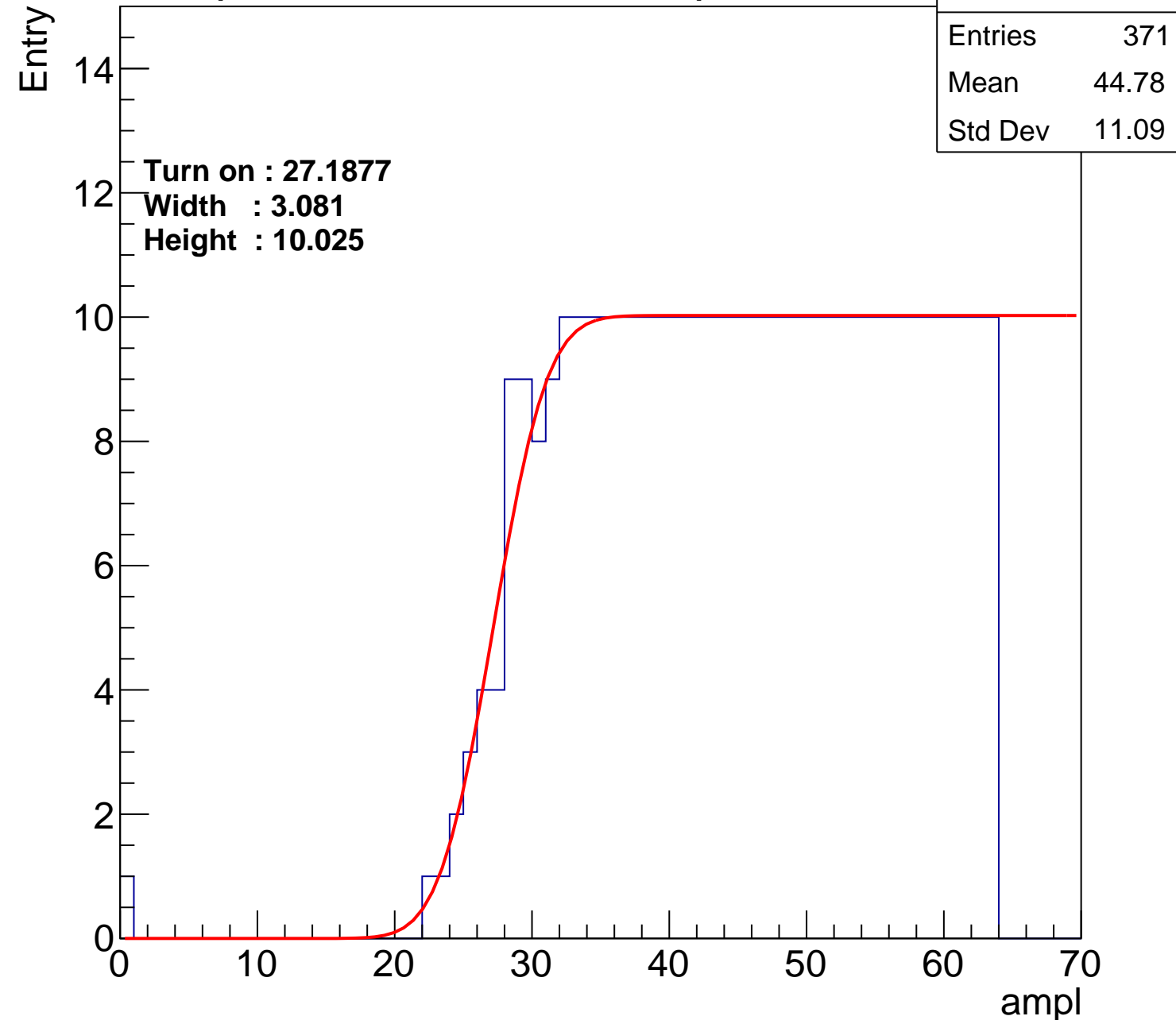
Width : 3.081

Height : 10.025

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch28

calib\_packv5\_042523\_0143.root, FC#9, port A1

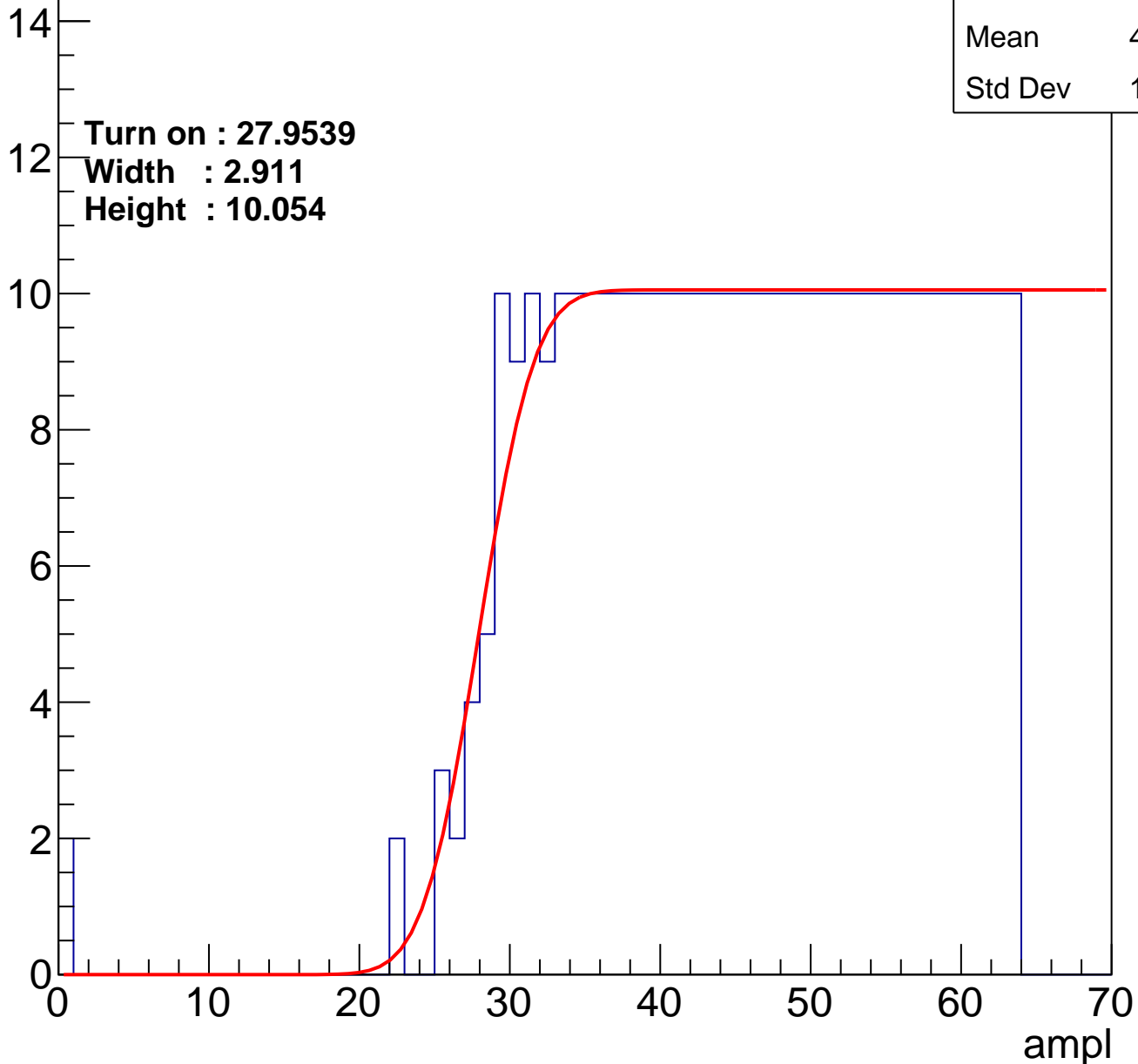
Entries	366
Mean	44.96
Std Dev	11.14

Turn on : 27.9539

Width : 2.911

Height : 10.054

Entry



# B0L001S, U20-ch29

calib\_packv5\_042523\_0143.root, FC#9, port A1

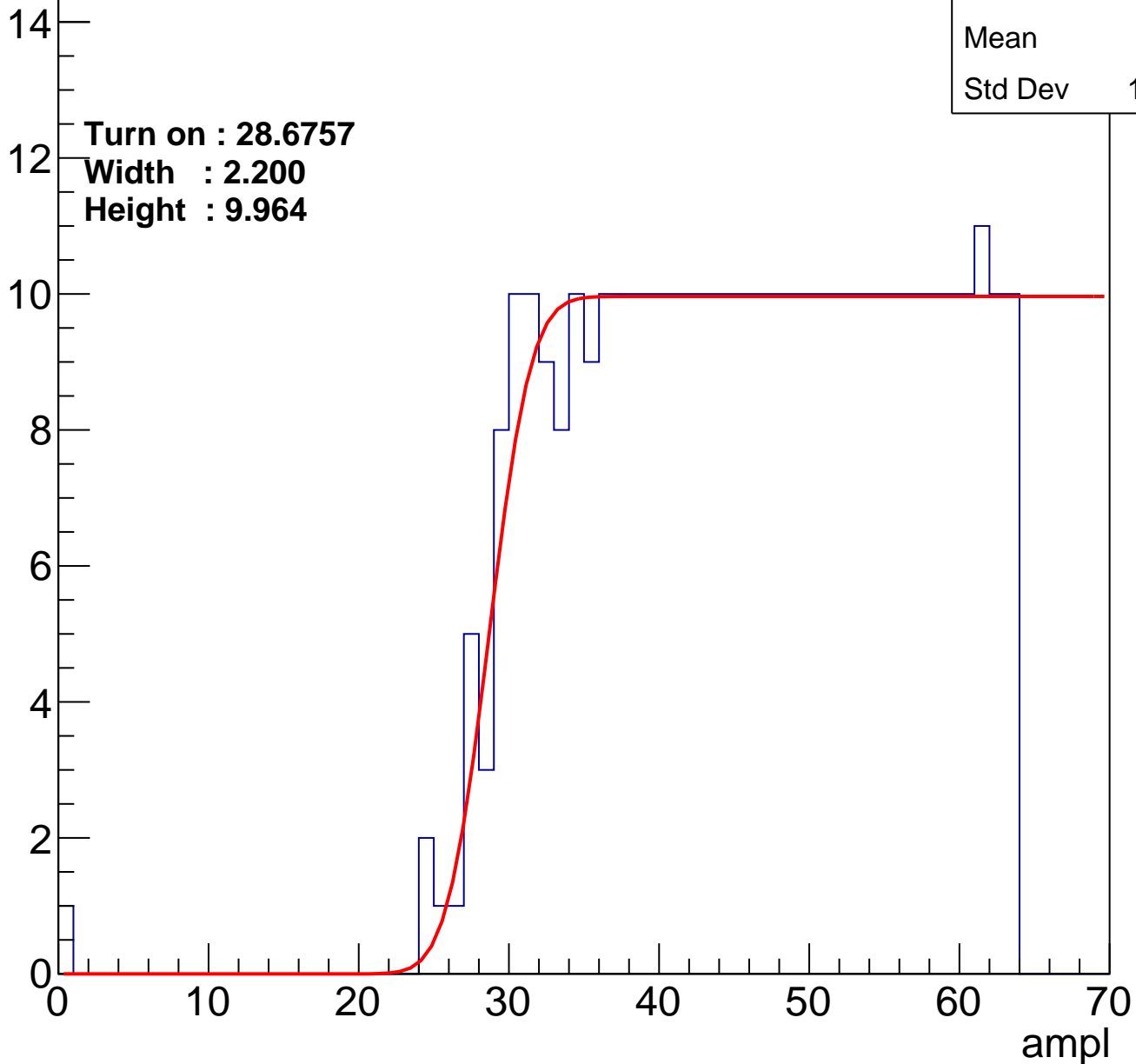
Entries	358
Mean	45.5
Std Dev	10.74

**Turn on : 28.6757**

**Width : 2.200**

**Height : 9.964**

Entry



# B0L001S, U20-ch30

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	327
Mean	46.87
Std Dev	10.2

Turn on : 31.5505

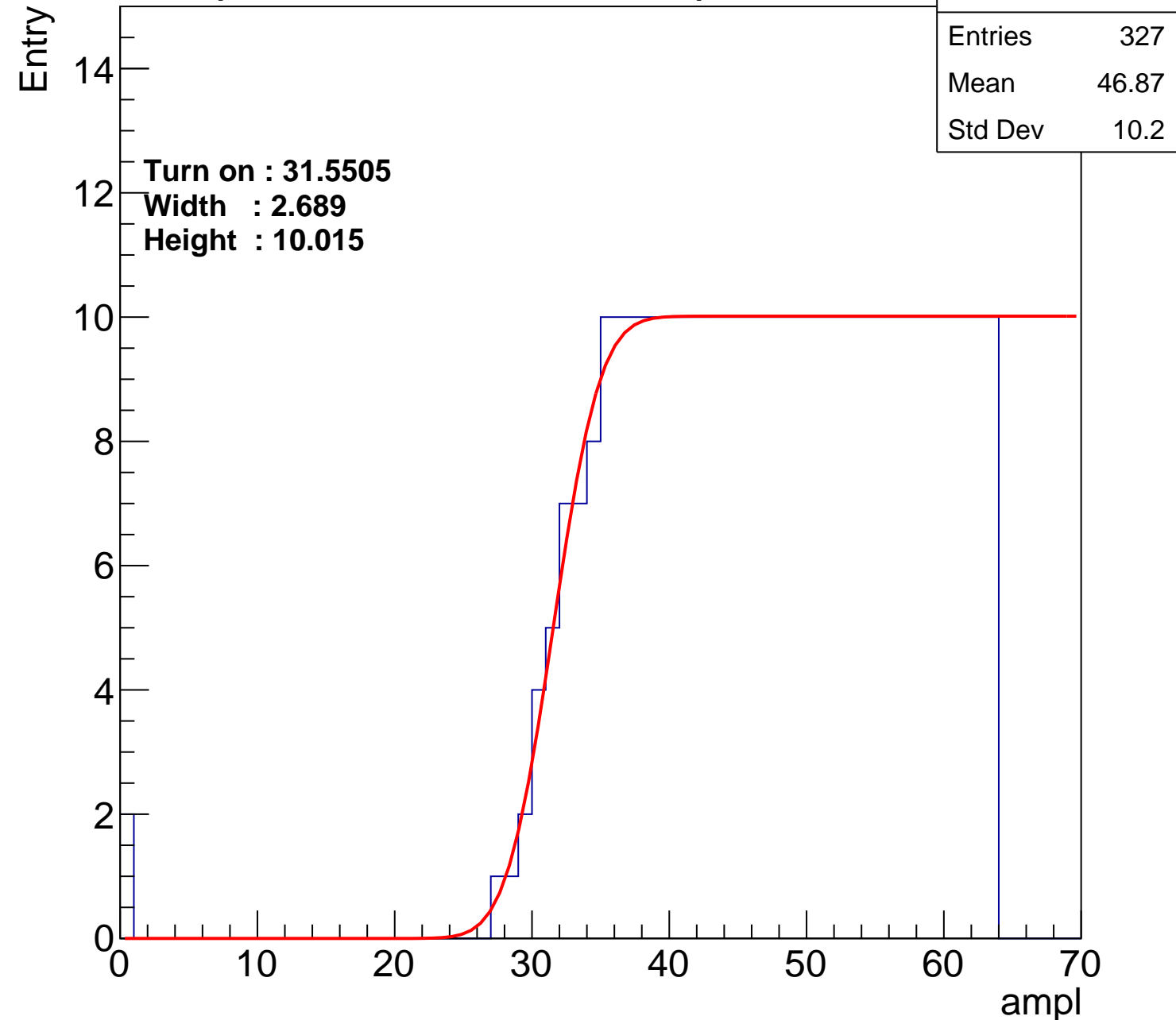
Width : 2.689

Height : 10.015

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L001S, U20-ch31

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	344
Mean	46.06
Std Dev	10.57

Turn on : 29.6315

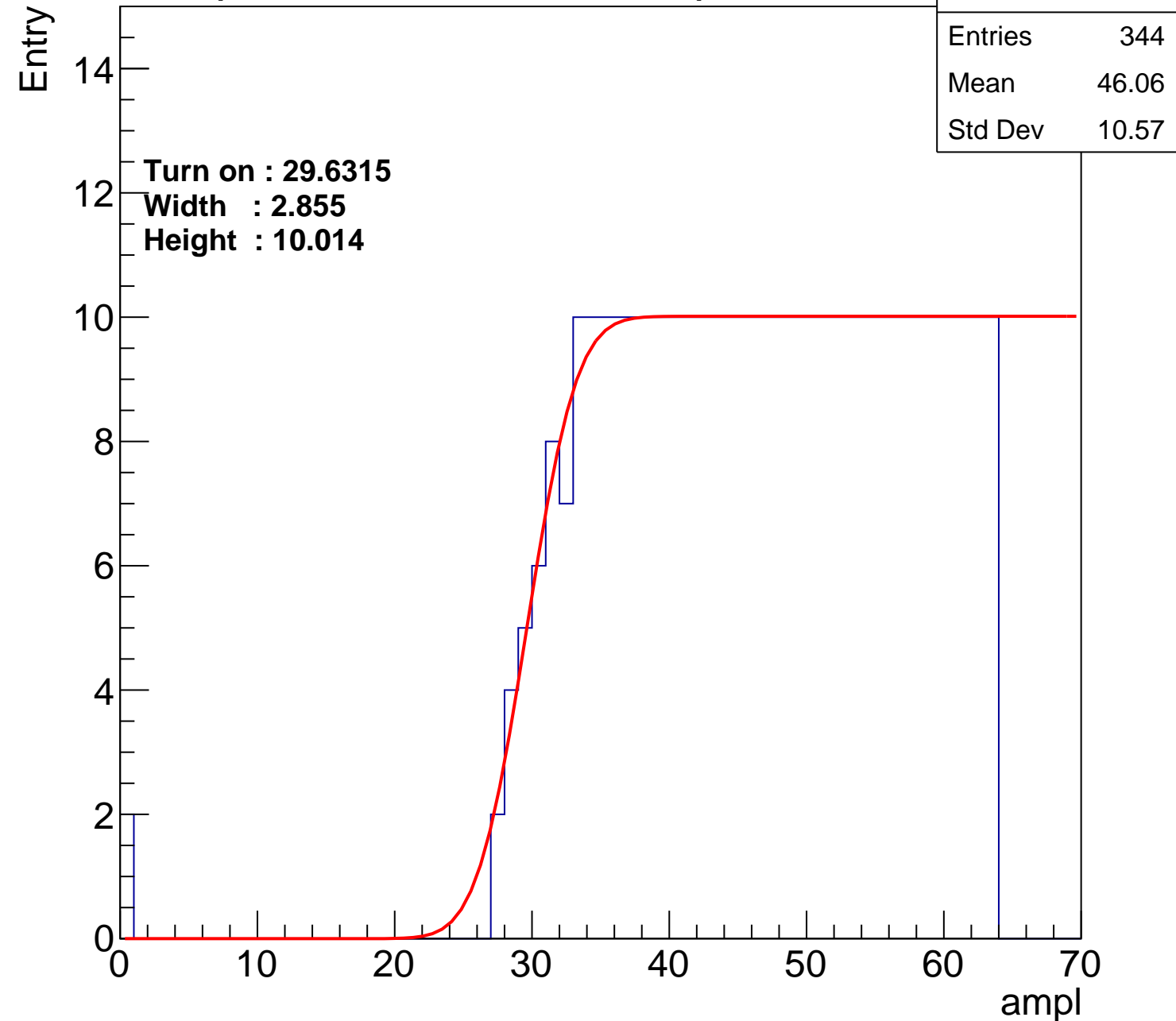
Width : 2.855

Height : 10.014

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch32

calib\_packv5\_042523\_0143.root, FC#9, port A1

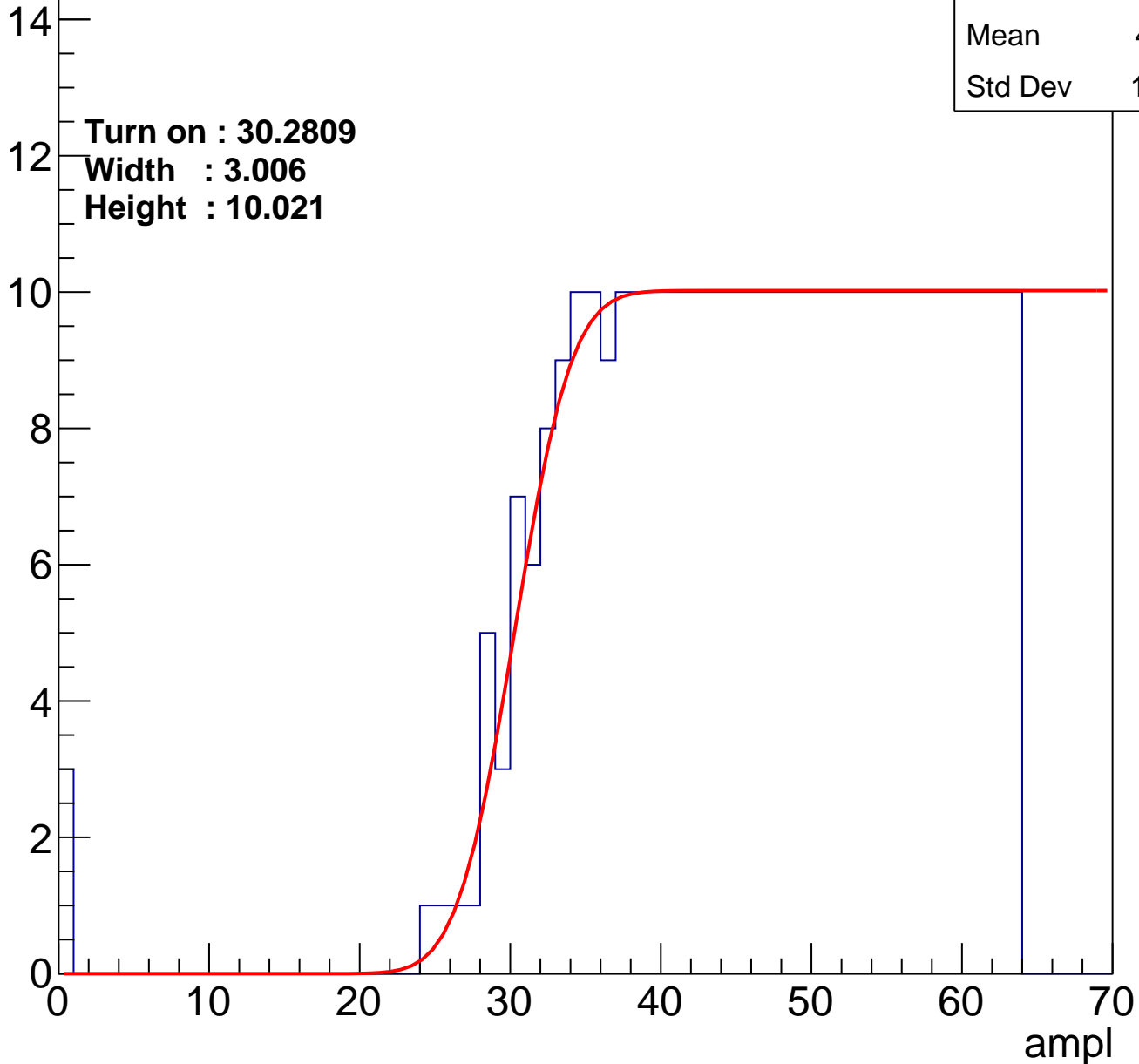
Entries	344
Mean	45.91
Std Dev	10.92

Turn on : 30.2809

Width : 3.006

Height : 10.021

Entry



# B0L001S, U20-ch33

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	356
Mean	45.38
Std Dev	11.1

**Turn on : 28.7007**

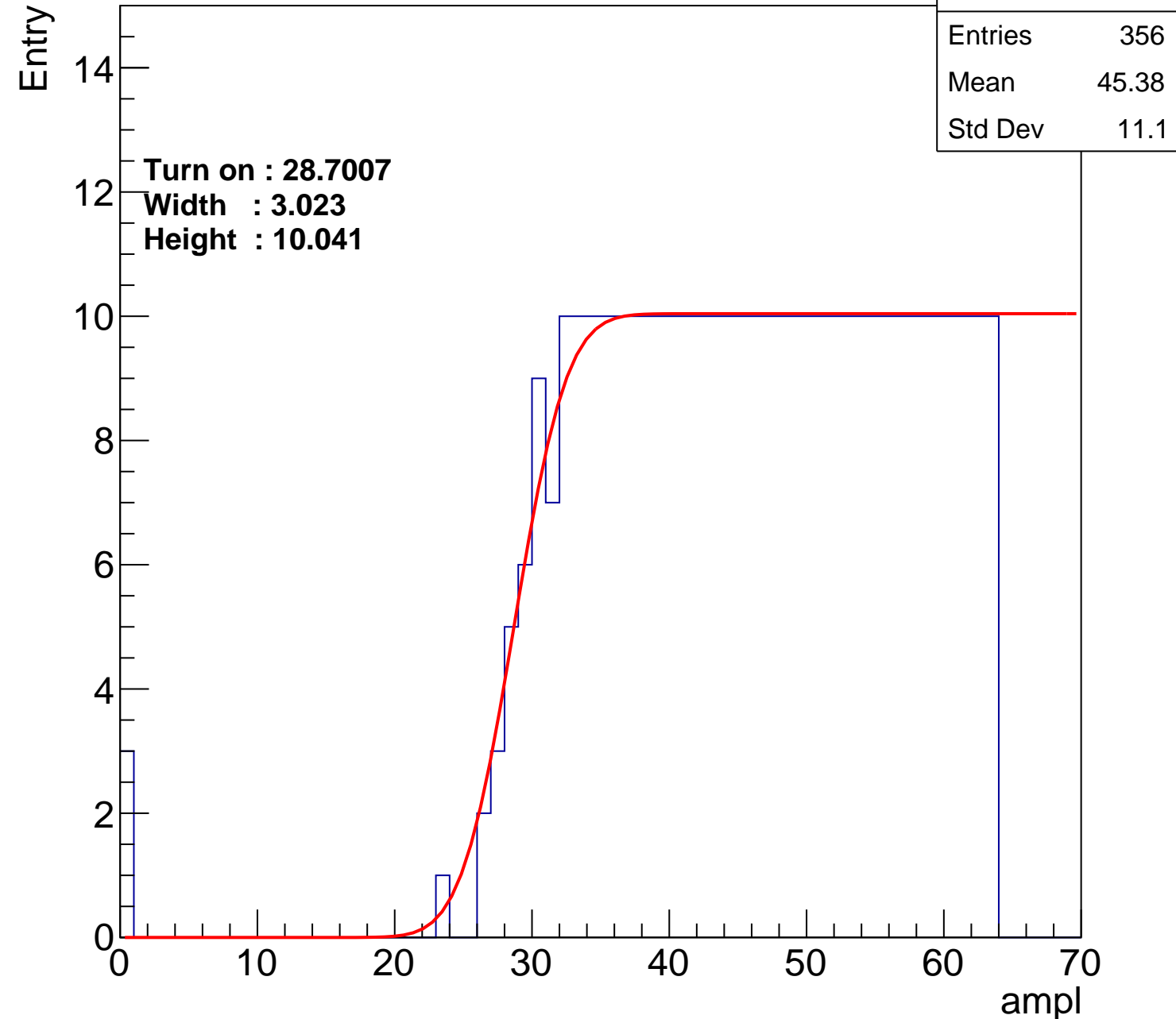
**Width : 3.023**

**Height : 10.041**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch34

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	360
Mean	45.16
Std Dev	11.25

**Turn on : 28.9401**

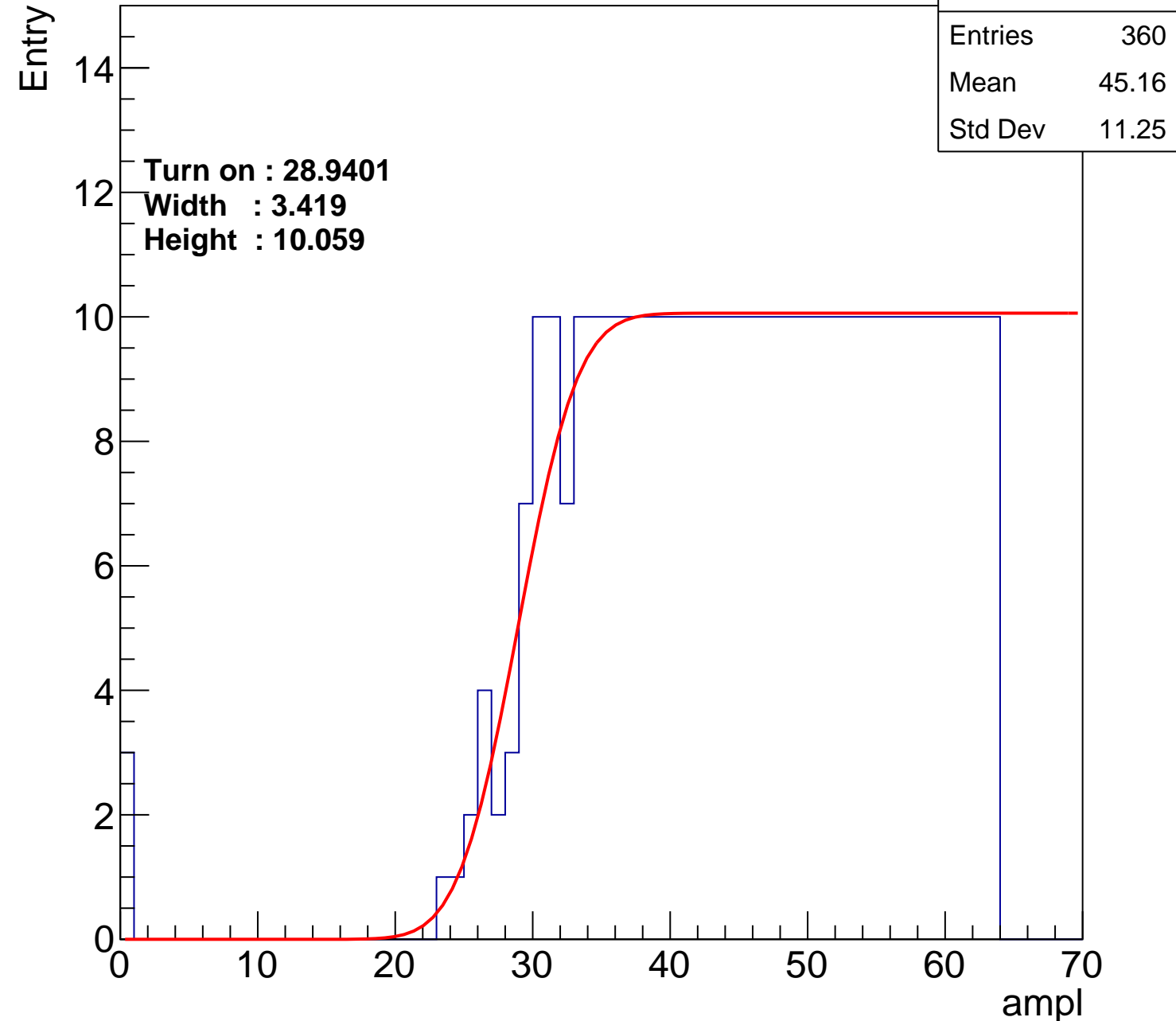
**Width : 3.419**

**Height : 10.059**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch35

calib\_packv5\_042523\_0143.root, FC#9, port A1

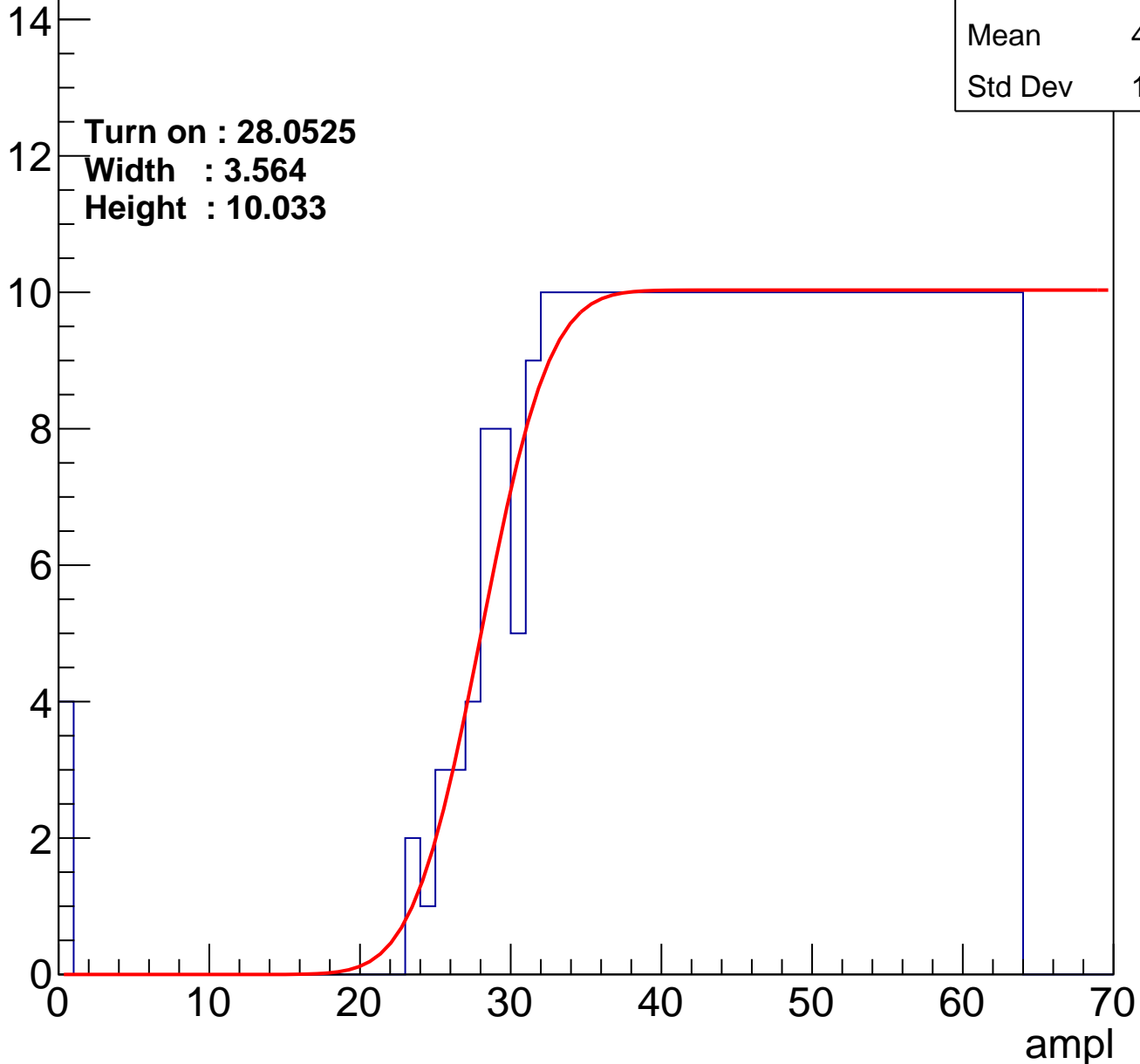
Entries	367
Mean	44.73
Std Dev	11.62

Turn on : 28.0525

Width : 3.564

Height : 10.033

Entry



# B0L001S, U20-ch36

calib\_packv5\_042523\_0143.root, FC#9, port A1

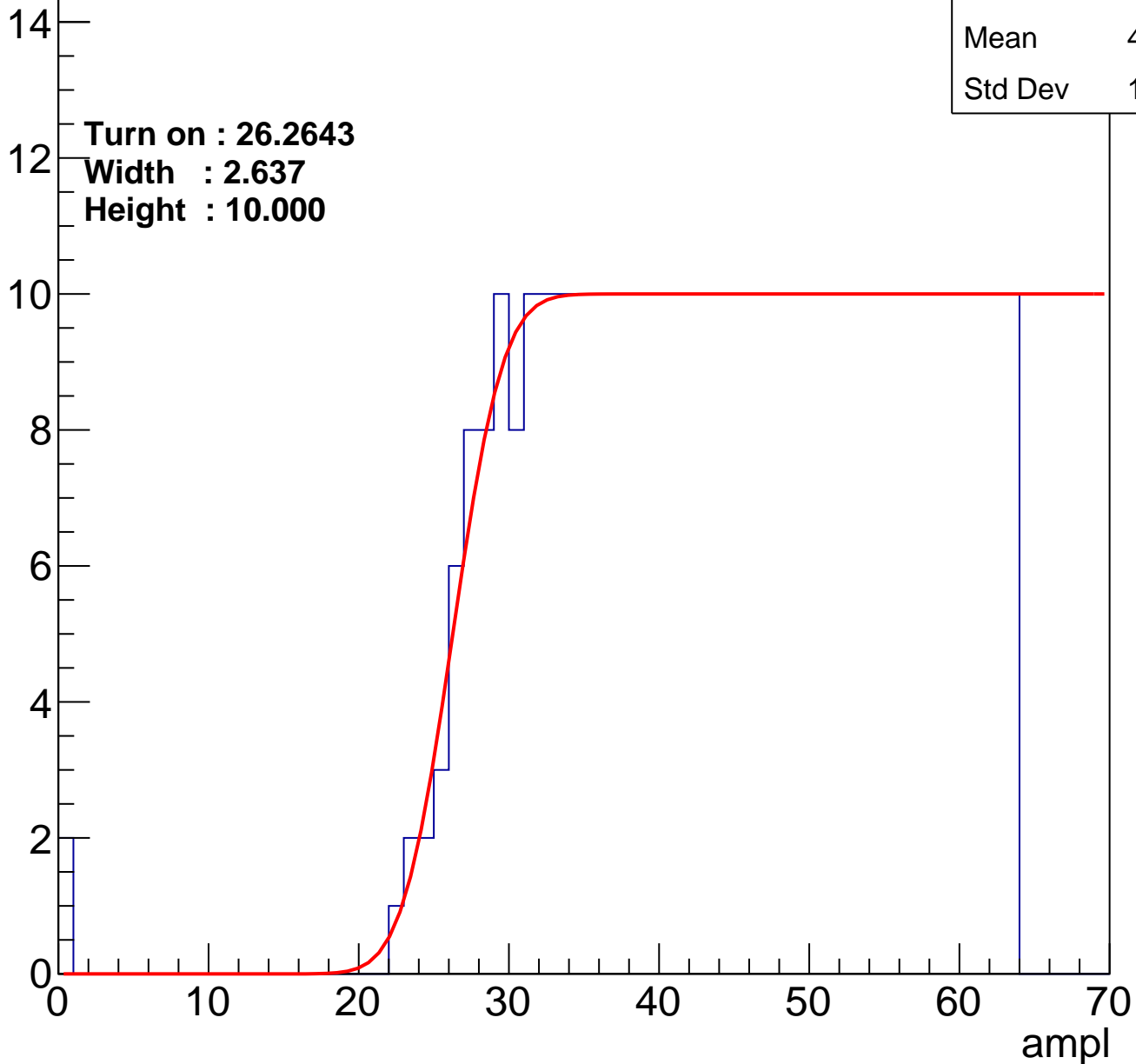
Entries	380
Mean	44.28
Std Dev	11.48

**Turn on : 26.2643**

**Width : 2.637**

**Height : 10.000**

Entry



# B0L001S, U20-ch37

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	357
Mean	45.35
Std Dev	10.99

**Turn on : 28.4479**

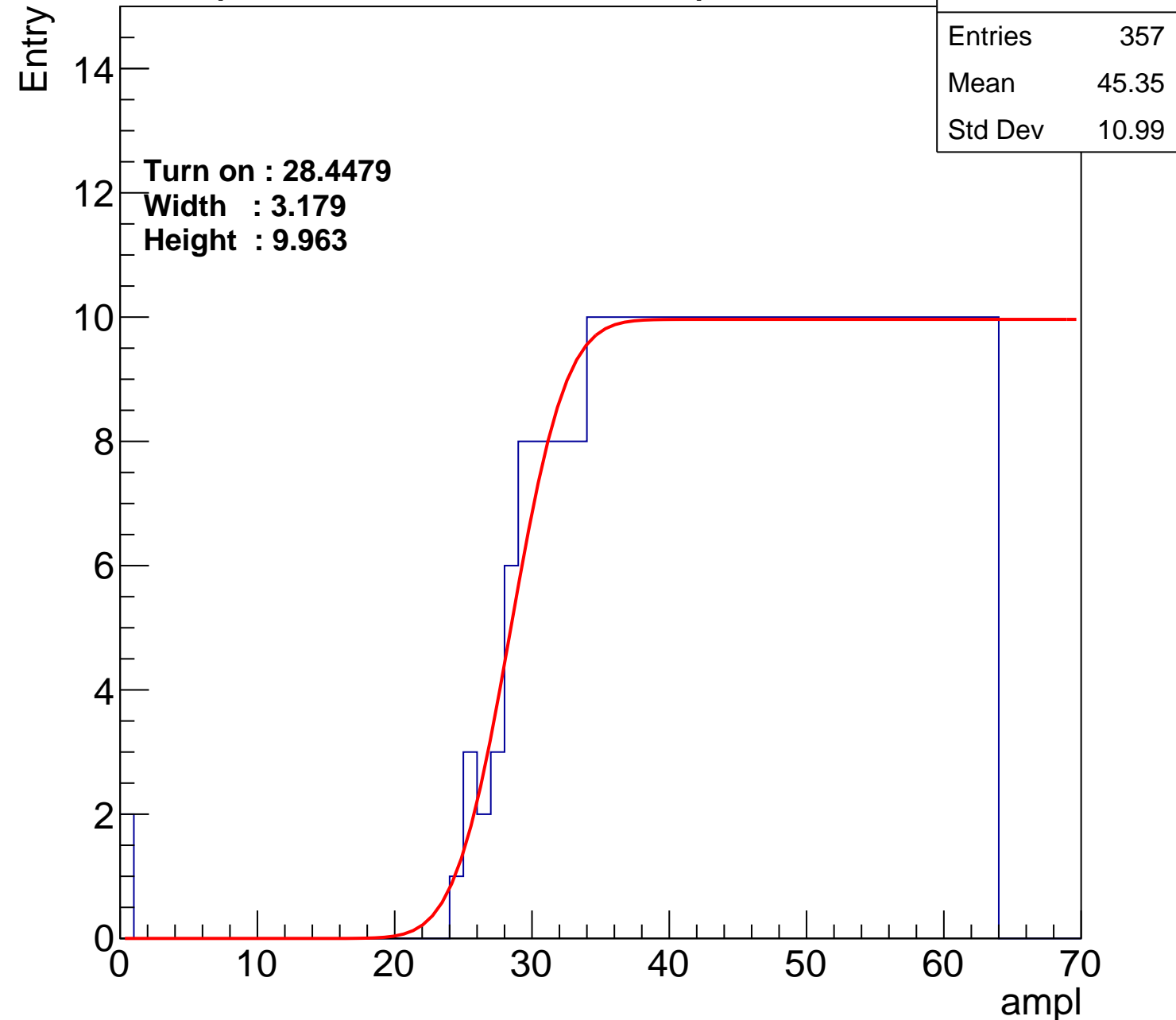
**Width : 3.179**

**Height : 9.963**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch38

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	350
Mean	45.61
Std Dev	11.06

**Turn on : 29.2747**

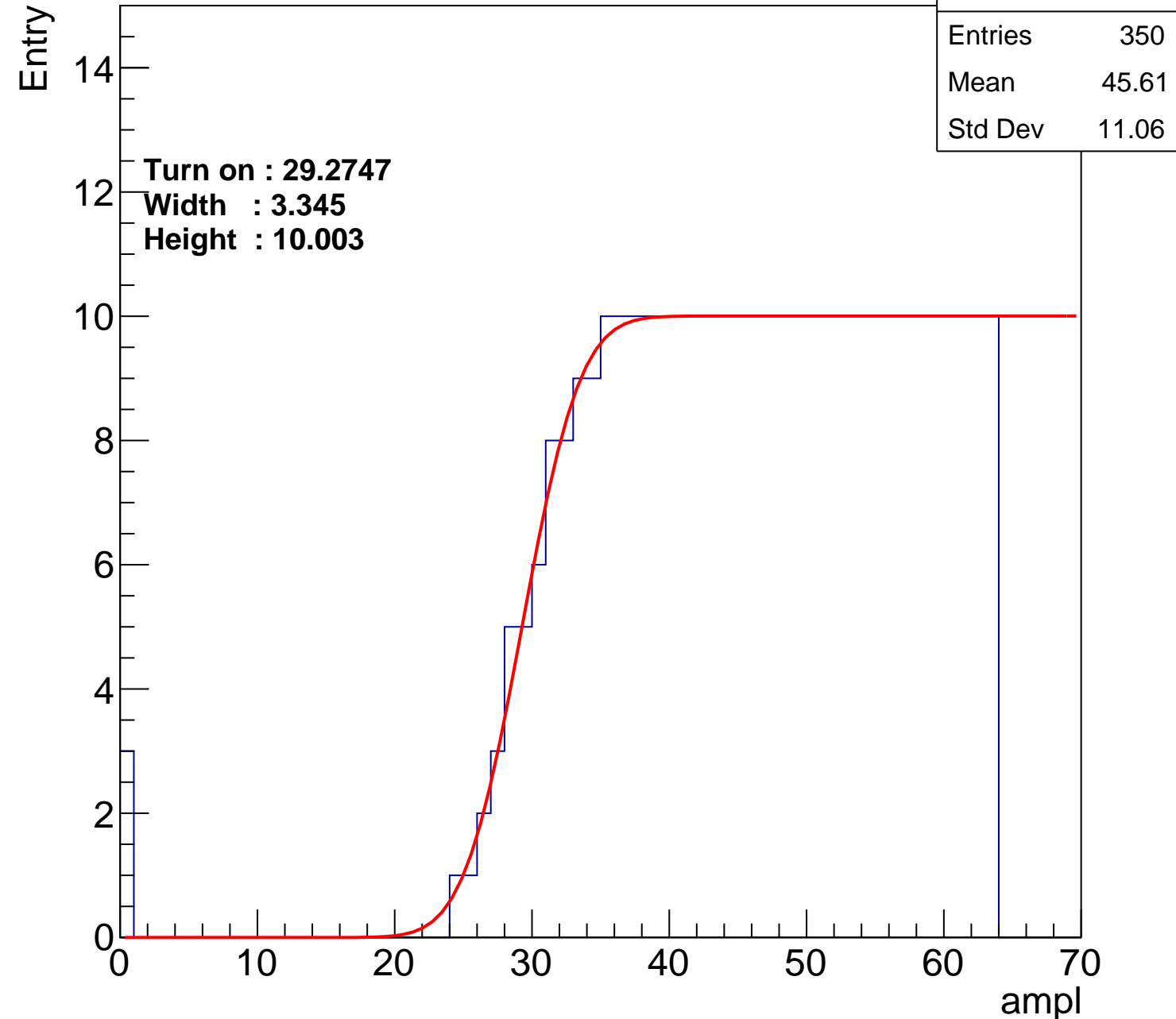
**Width : 3.345**

**Height : 10.003**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L001S, U20-ch39

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	345
Mean	45.88
Std Dev	10.9

Turn on : 29.9912

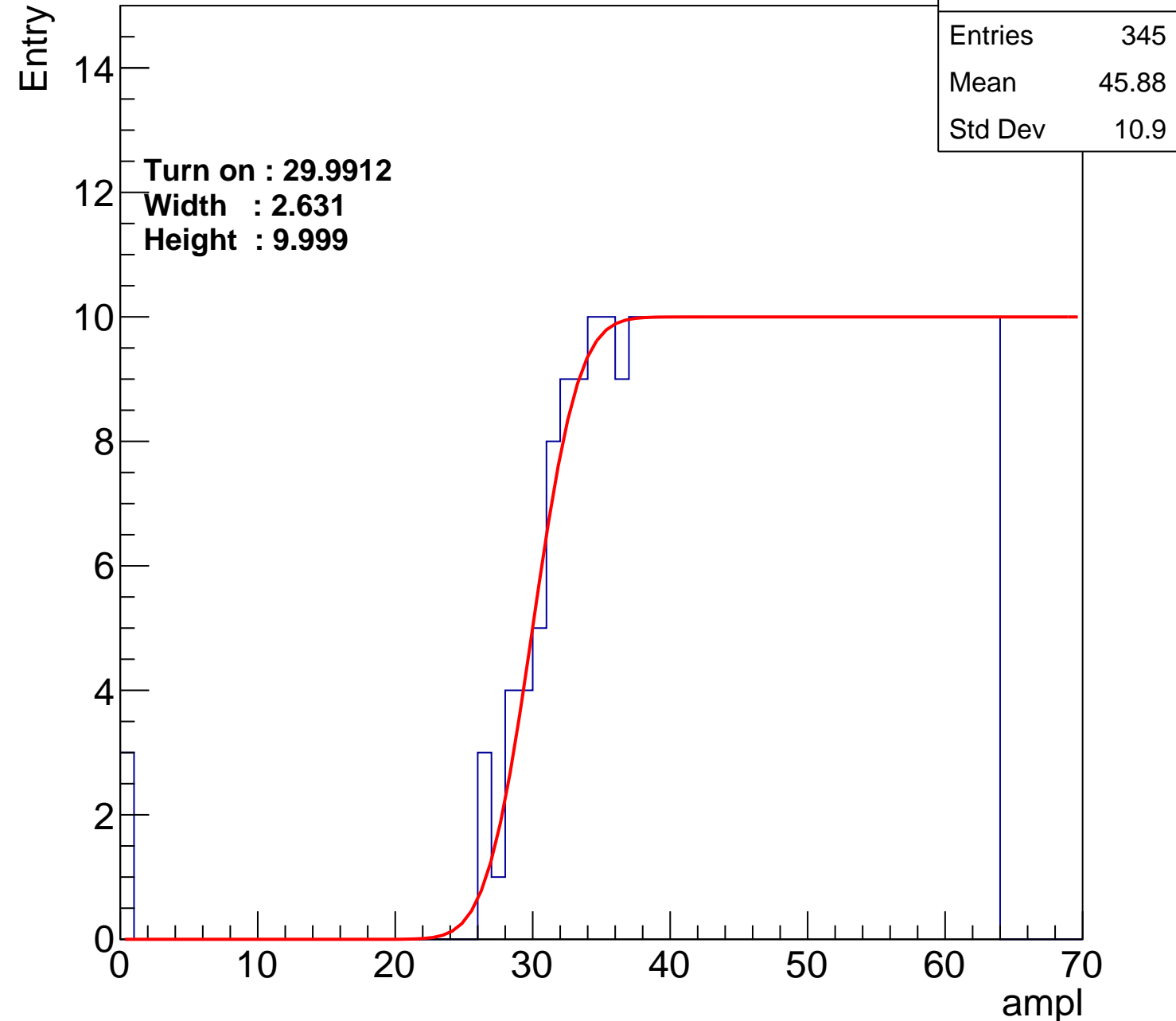
Width : 2.631

Height : 9.999

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch40

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	362
Mean	45.12
Std Dev	11.12

Turn on : 28.5241

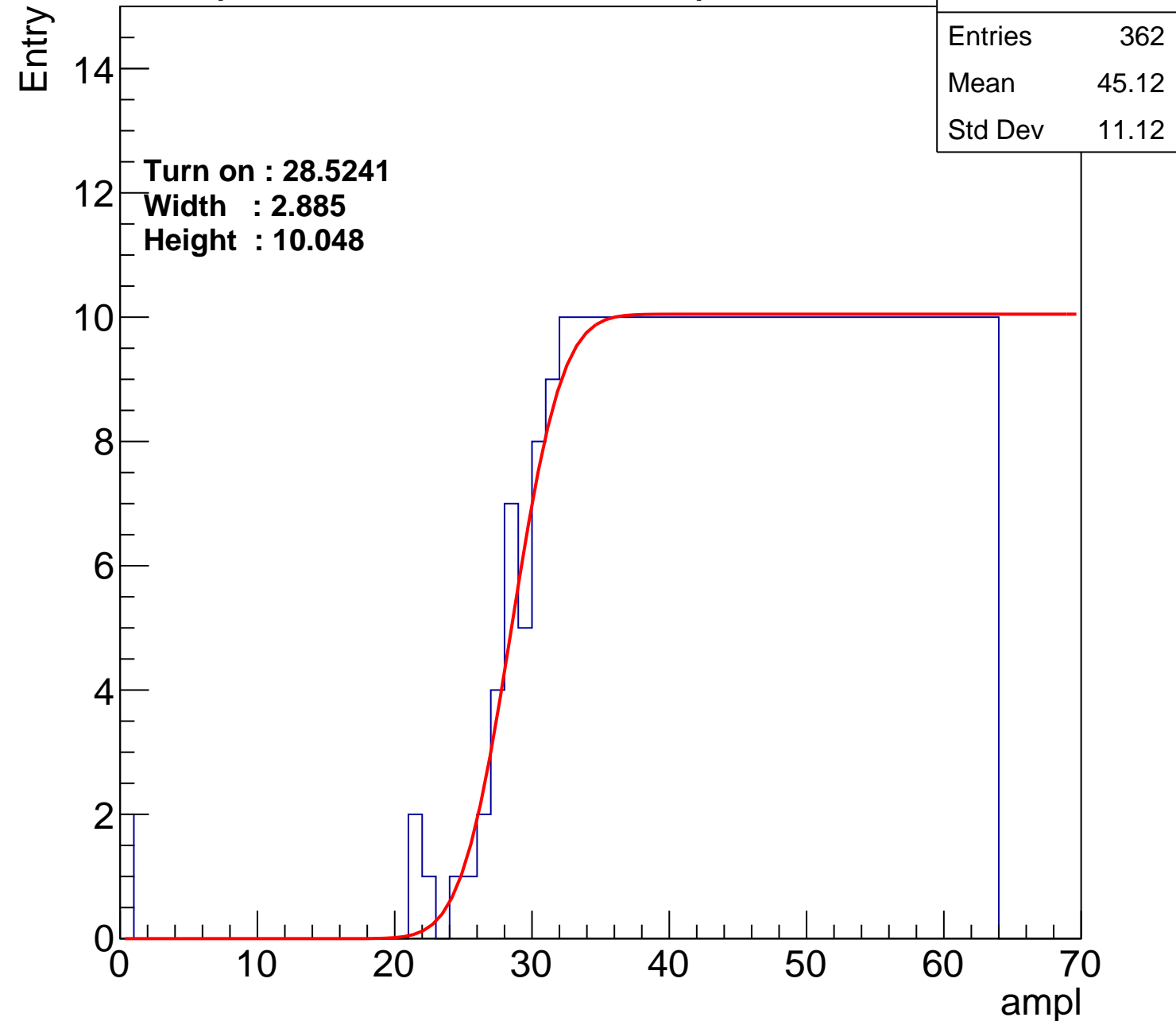
Width : 2.885

Height : 10.048

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch41

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	360
Mean	45.27
Std Dev	10.87

Turn on : 28.1226

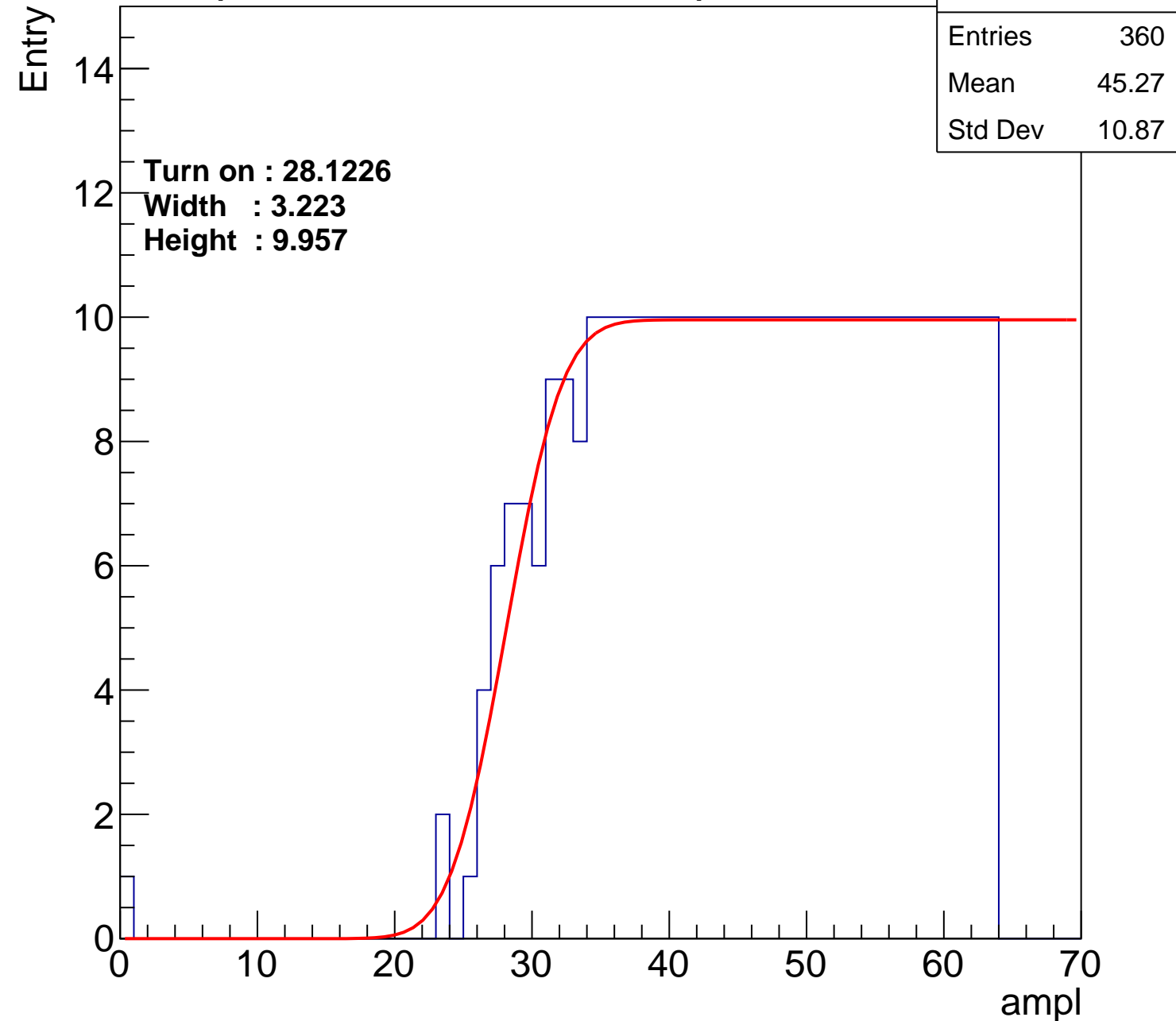
Width : 3.223

Height : 9.957

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch42

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	341
Mean	46.24
Std Dev	10.31

**Turn on : 30.3060**

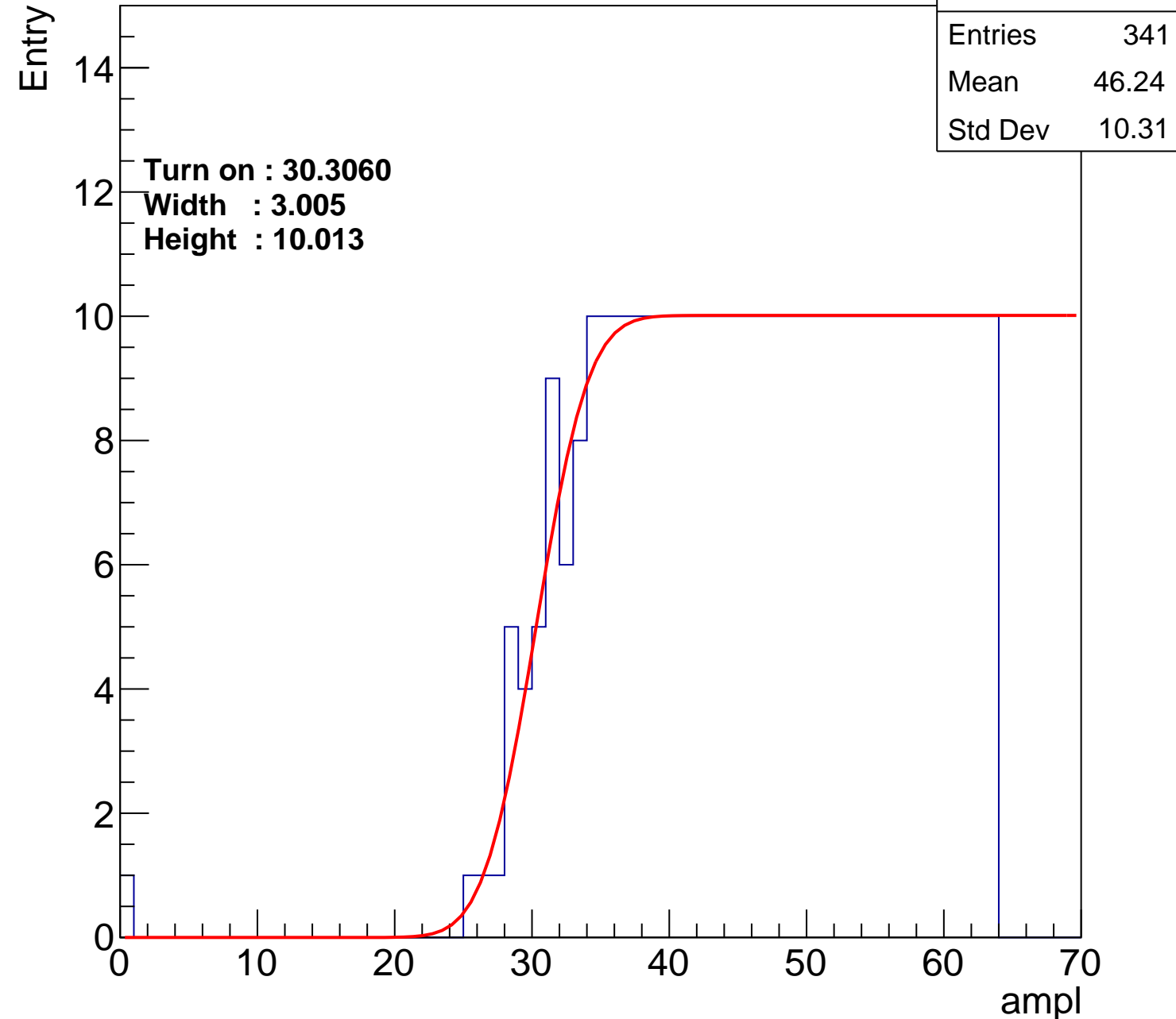
**Width : 3.005**

**Height : 10.013**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch43

calib\_packv5\_042523\_0143.root, FC#9, port A1

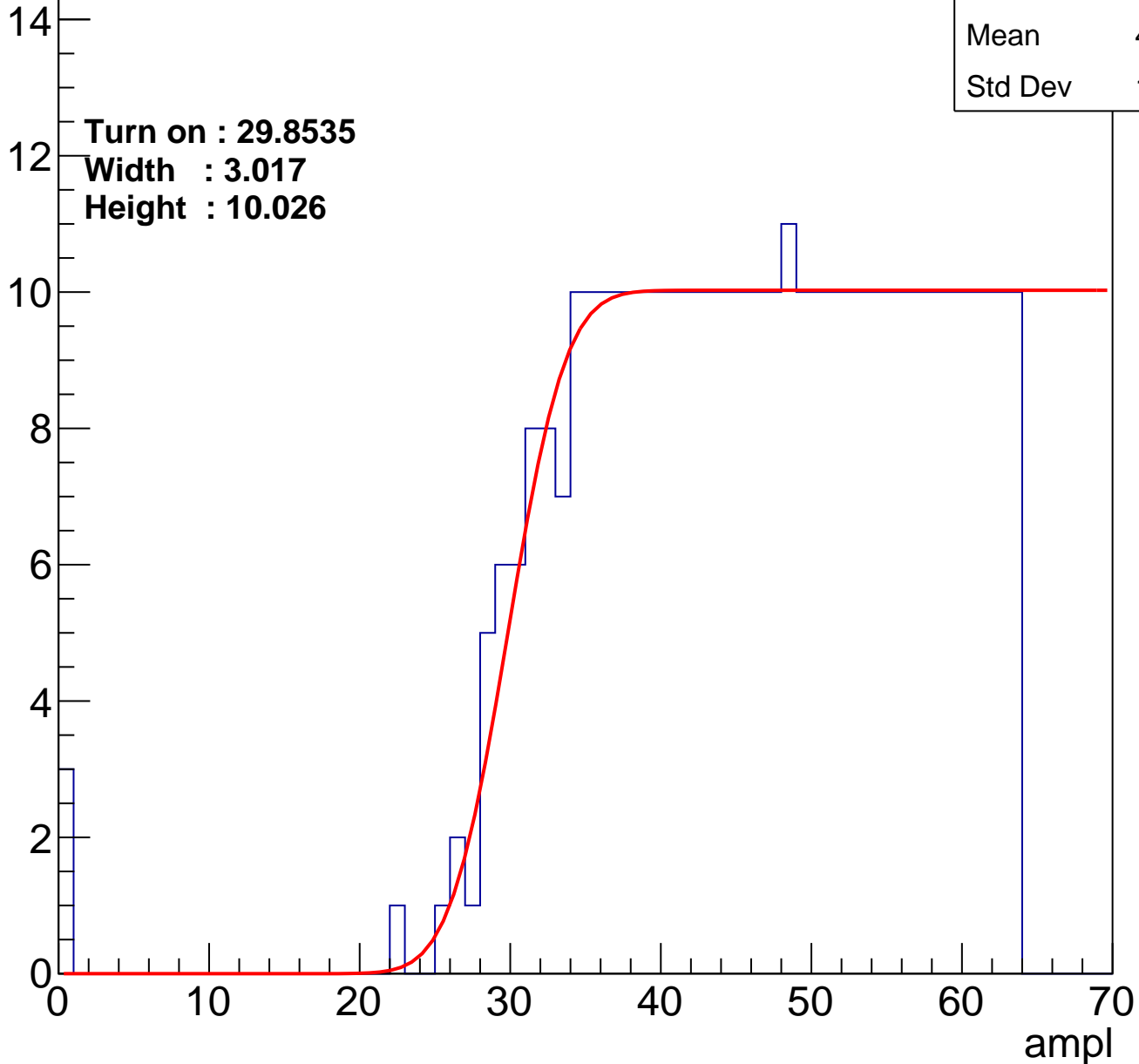
Entries	349
Mean	45.71
Std Dev	11.01

Turn on : 29.8535

Width : 3.017

Height : 10.026

Entry



# B0L001S, U20-ch44

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	372
Mean	44.6
Std Dev	11.49

Turn on : 27.0861

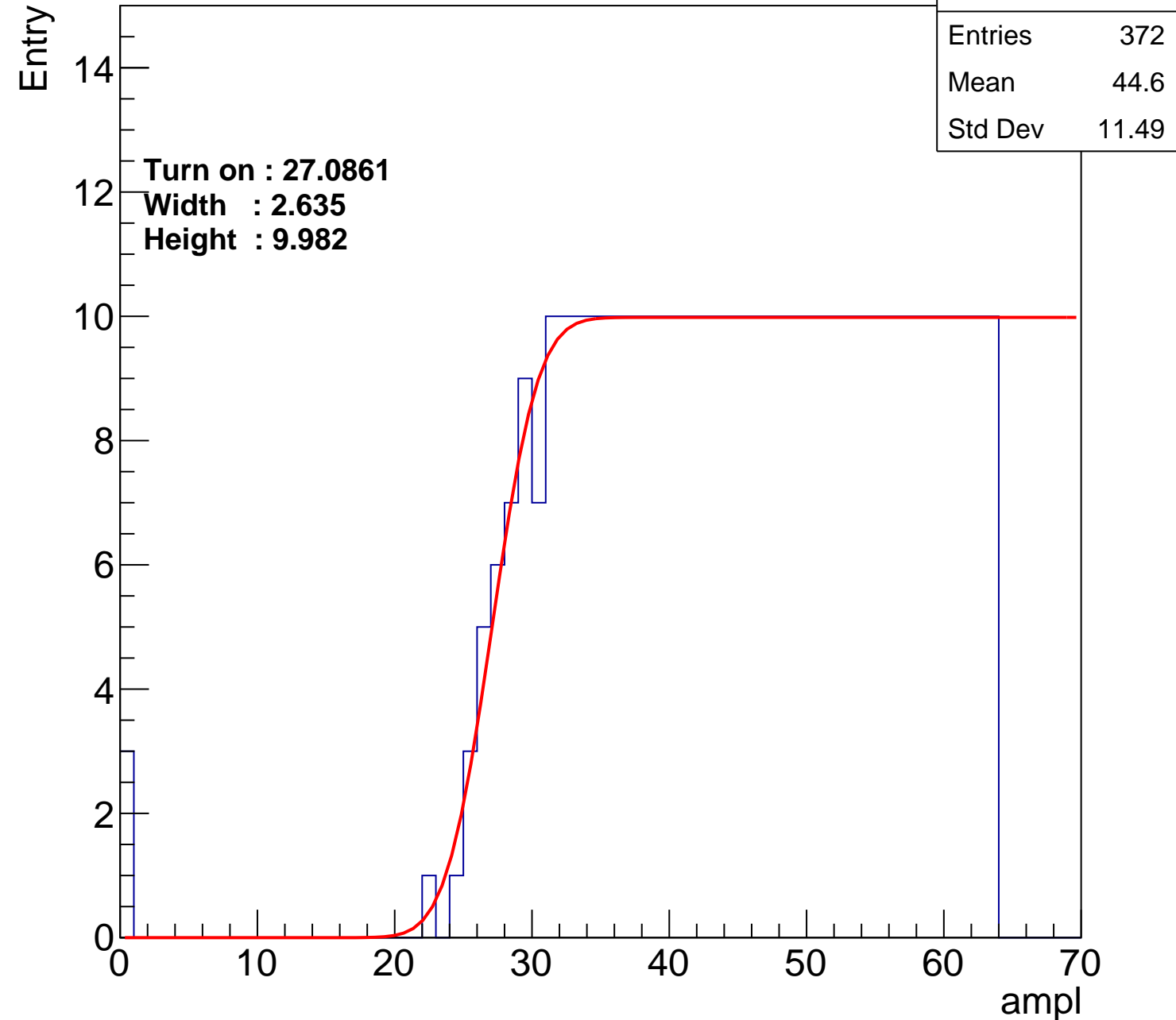
Width : 2.635

Height : 9.982

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch45

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	351
Mean	45.74
Std Dev	10.58

**Turn on : 28.9737**

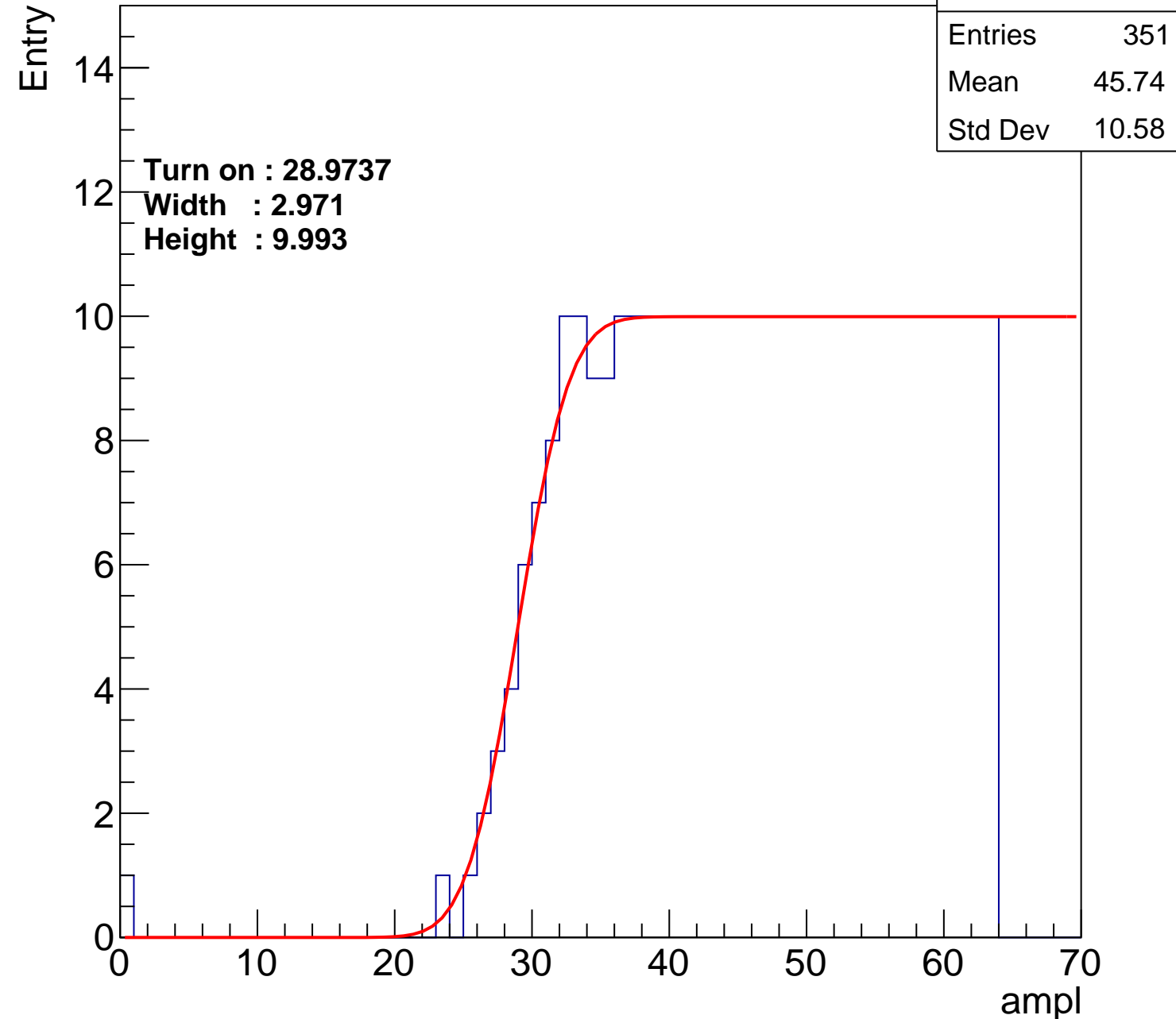
**Width : 2.971**

**Height : 9.993**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch46

calib\_packv5\_042523\_0143.root, FC#9, port A1

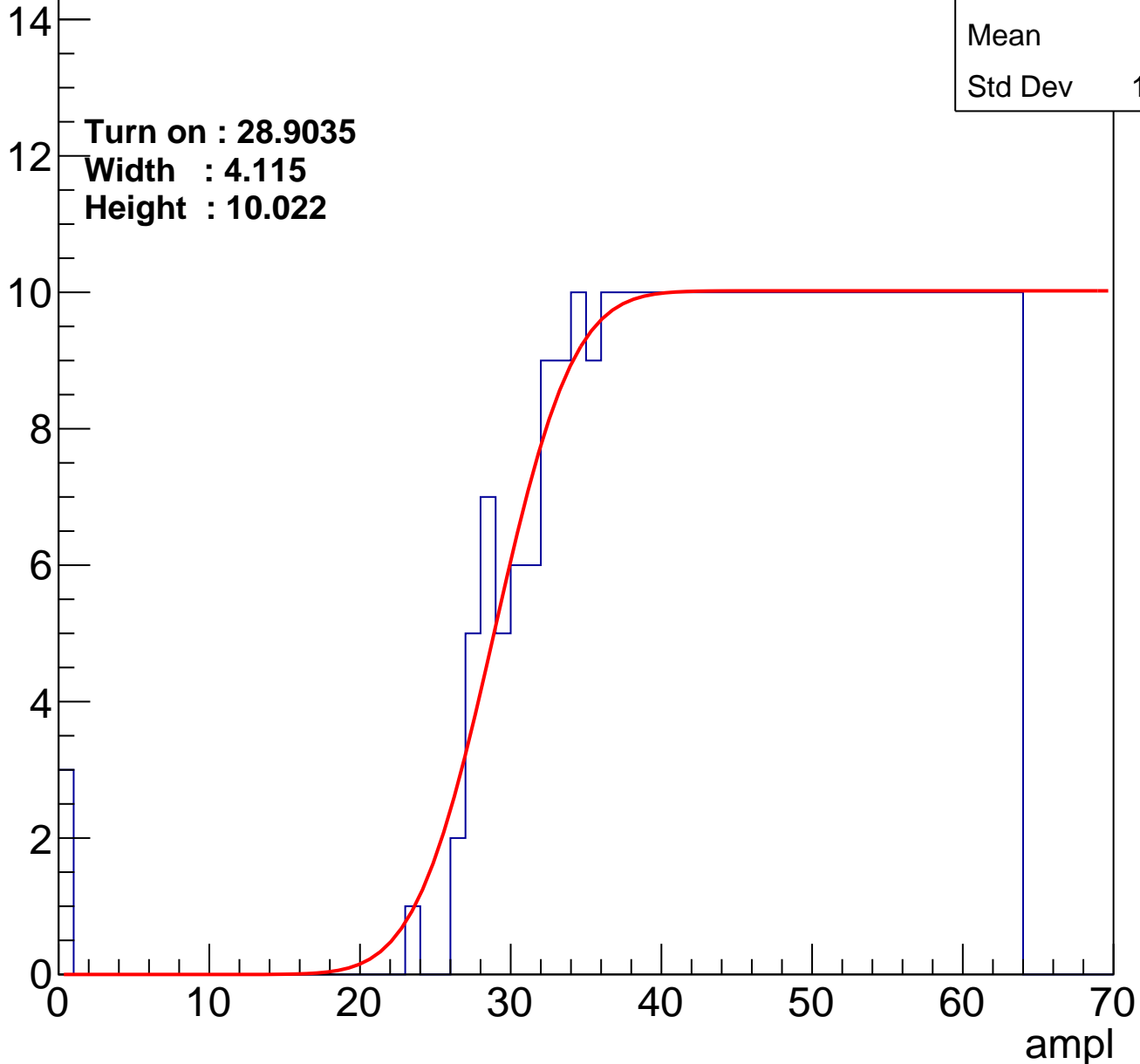
Entries	352
Mean	45.5
Std Dev	11.12

Turn on : 28.9035

Width : 4.115

Height : 10.022

Entry





# B0L001S, U20-ch47

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	370
Mean	44.67
Std Dev	11.47

Turn on : 27.2443

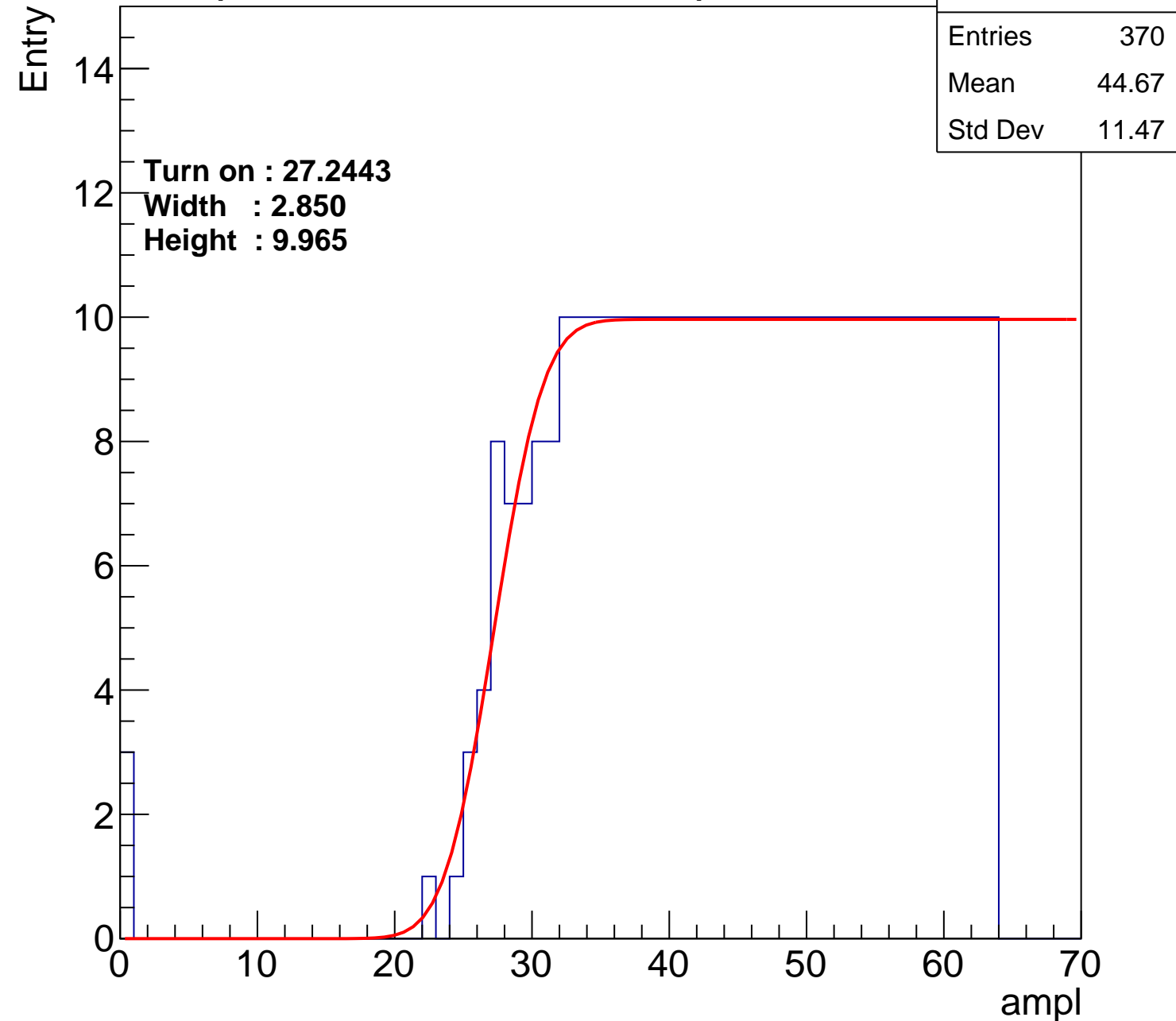
Width : 2.850

Height : 9.965

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch48

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	371
Mean	44.55
Std Dev	11.69

Turn on : 27.2630

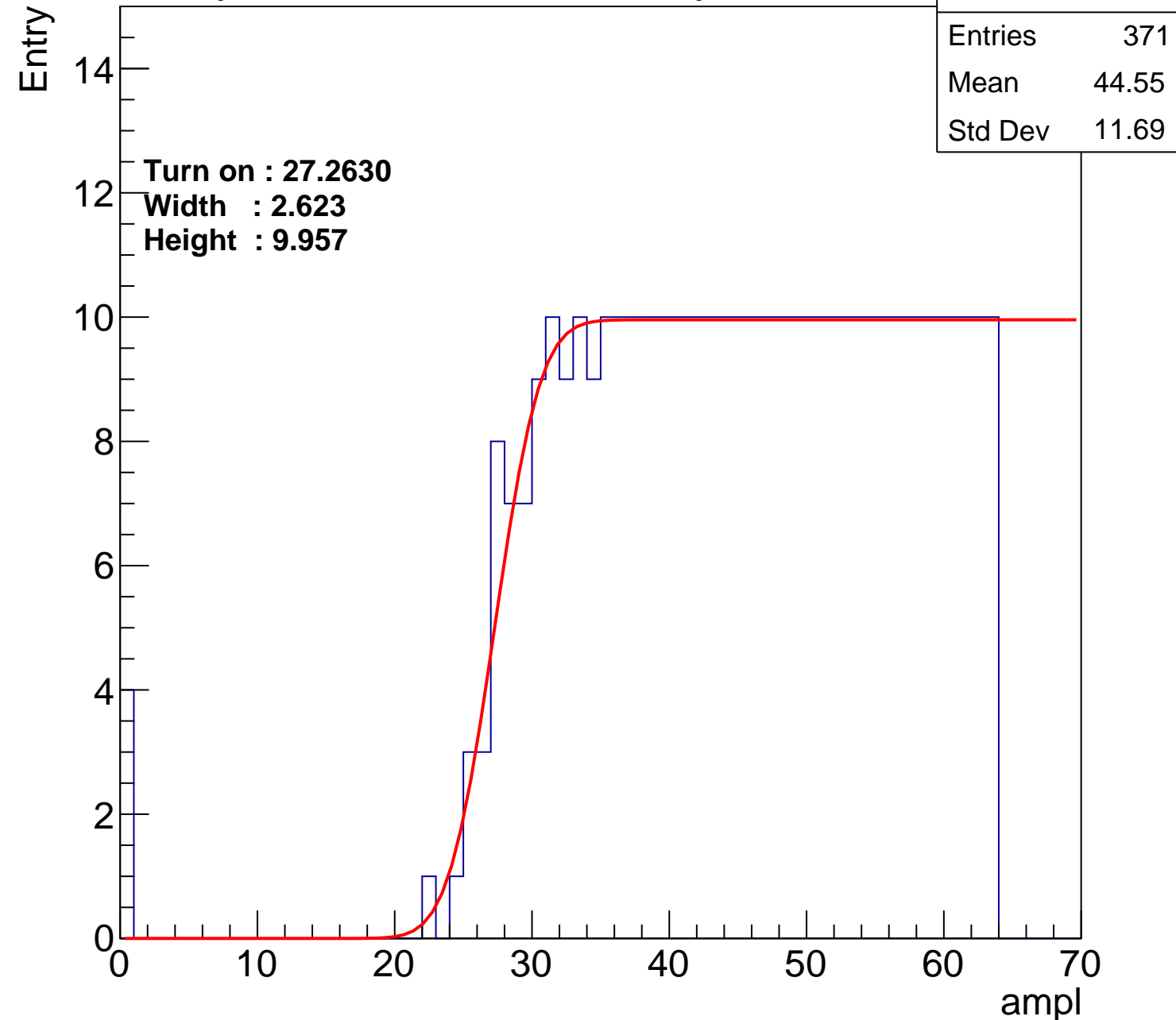
Width : 2.623

Height : 9.957

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch49

calib\_packv5\_042523\_0143.root, FC#9, port A1

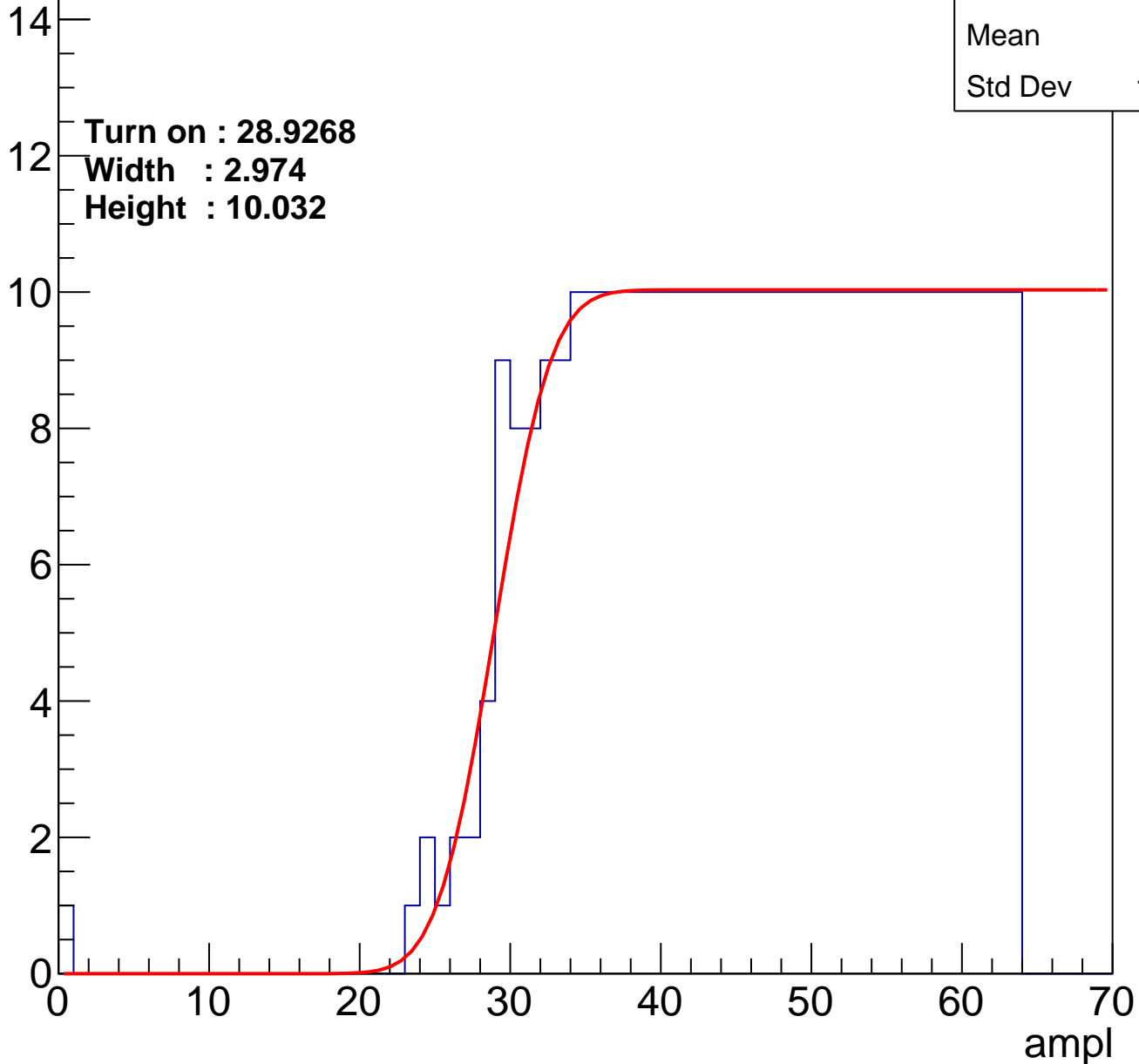
Entries	356
Mean	45.5
Std Dev	10.71

**Turn on : 28.9268**

**Width : 2.974**

**Height : 10.032**

Entry



# B0L001S, U20-ch50

calib\_packv5\_042523\_0143.root, FC#9, port A1

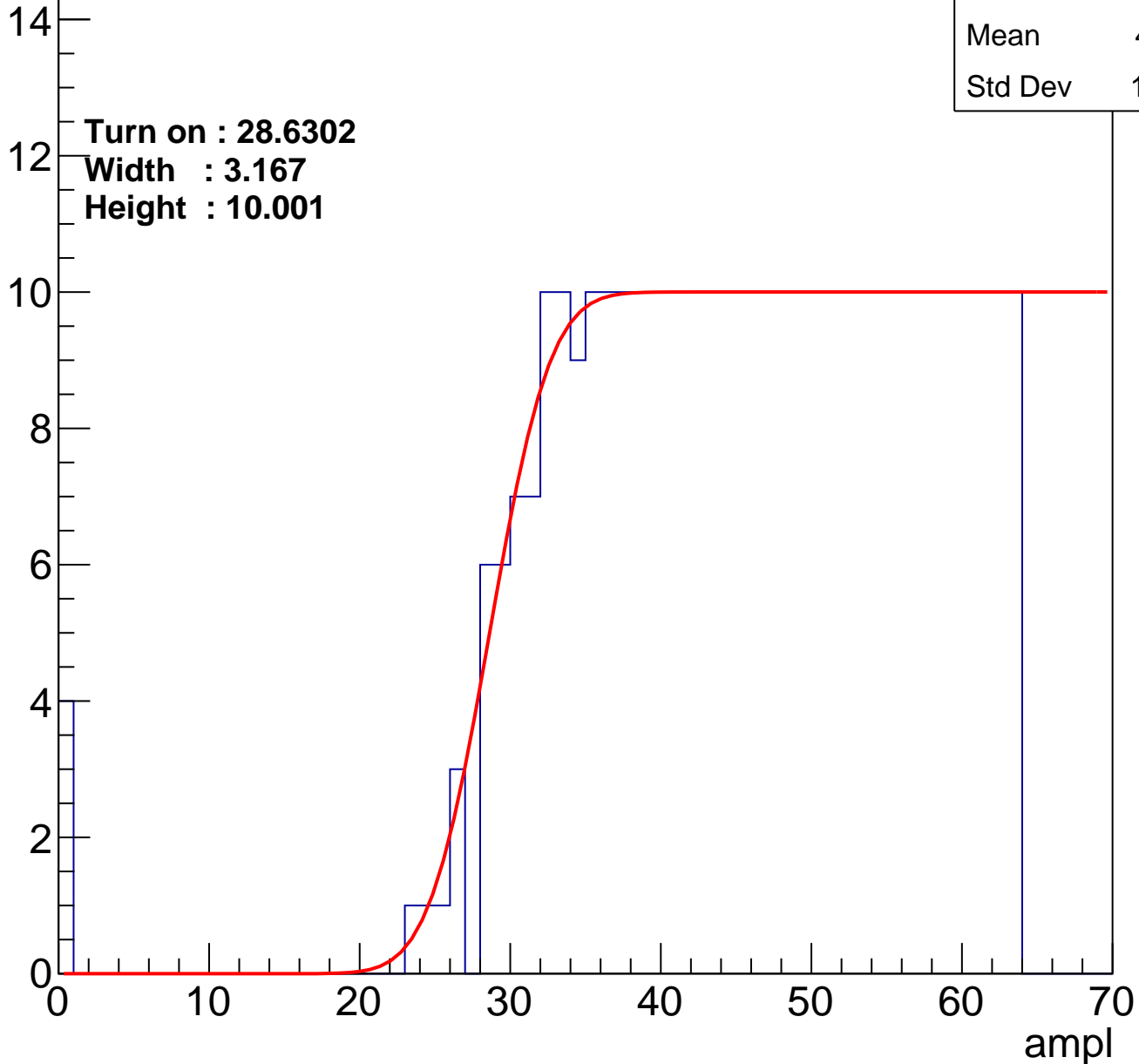
Entries	355
Mean	45.31
Std Dev	11.36

**Turn on : 28.6302**

**Width : 3.167**

**Height : 10.001**

Entry



# B0L001S, U20-ch51

calib\_packv5\_042523\_0143.root, FC#9, port A1

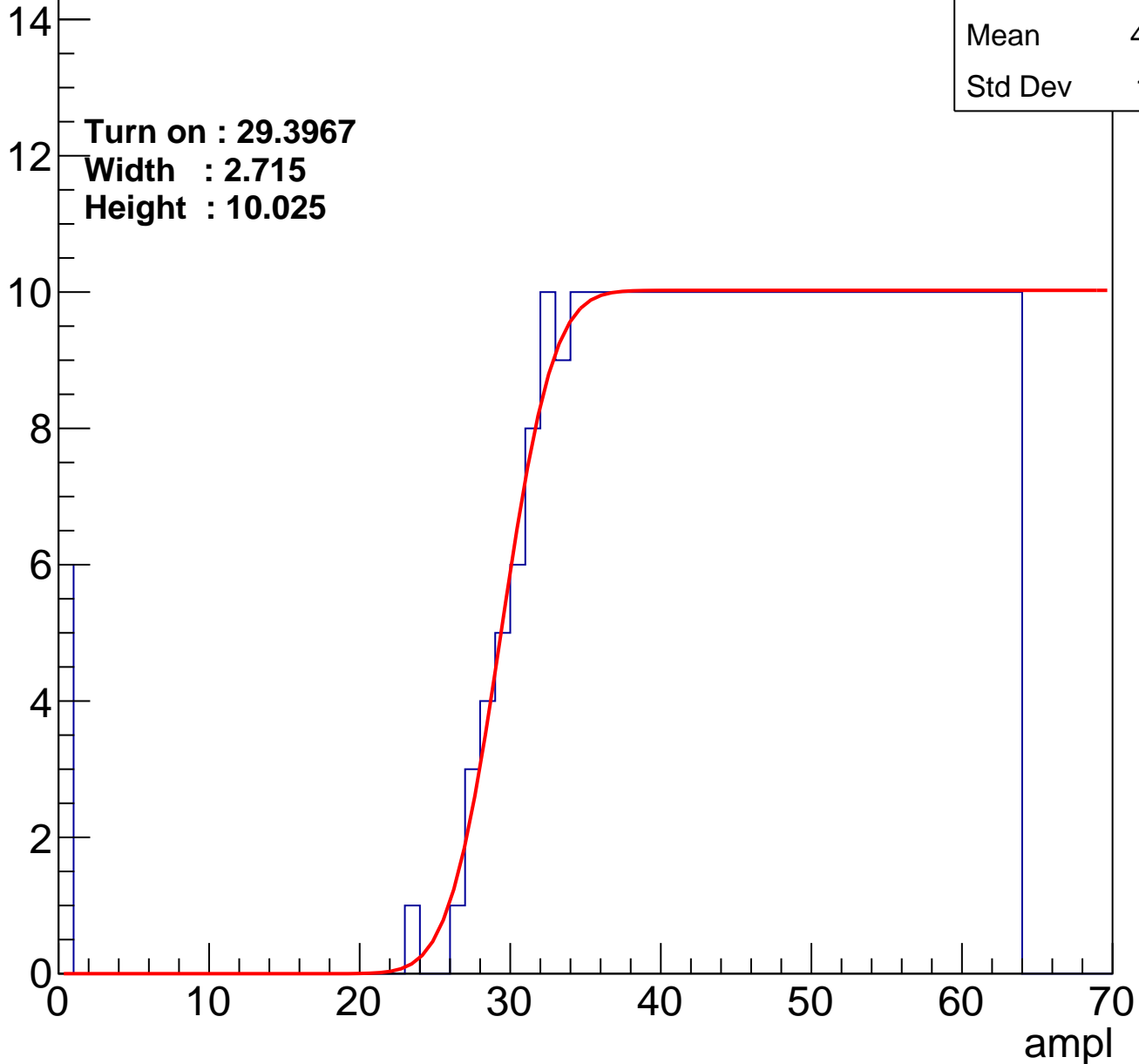
Entries	353
Mean	45.27
Std Dev	11.71

**Turn on : 29.3967**

**Width : 2.715**

**Height : 10.025**

Entry



# B0L001S, U20-ch52

calib\_packv5\_042523\_0143.root, FC#9, port A1

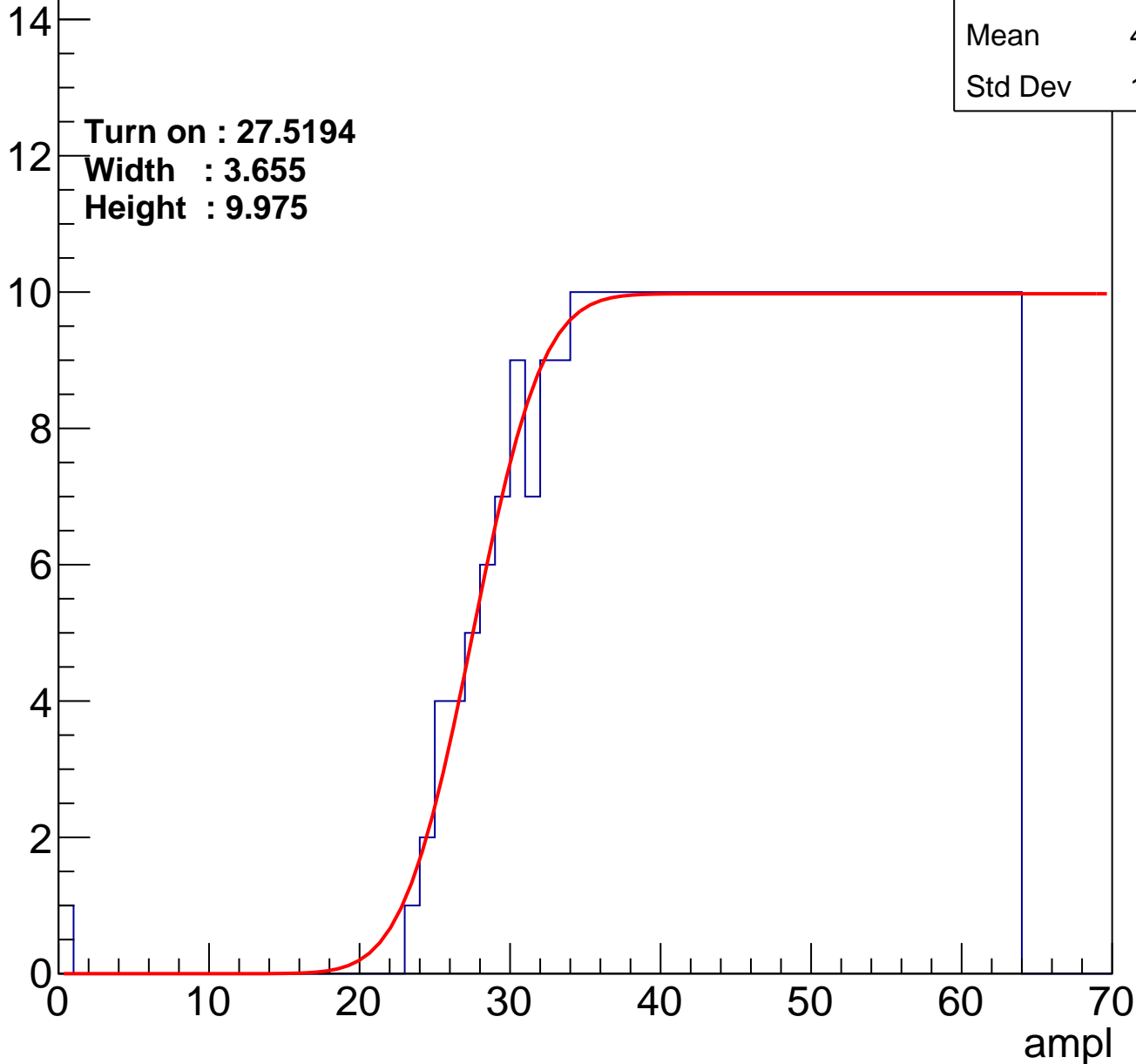
Entries	364
Mean	45.06
Std Dev	10.99

Turn on : 27.5194

Width : 3.655

Height : 9.975

Entry



# B0L001S, U20-ch53

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	350
Mean	45.77
Std Dev	10.6

Turn on : 29.5245

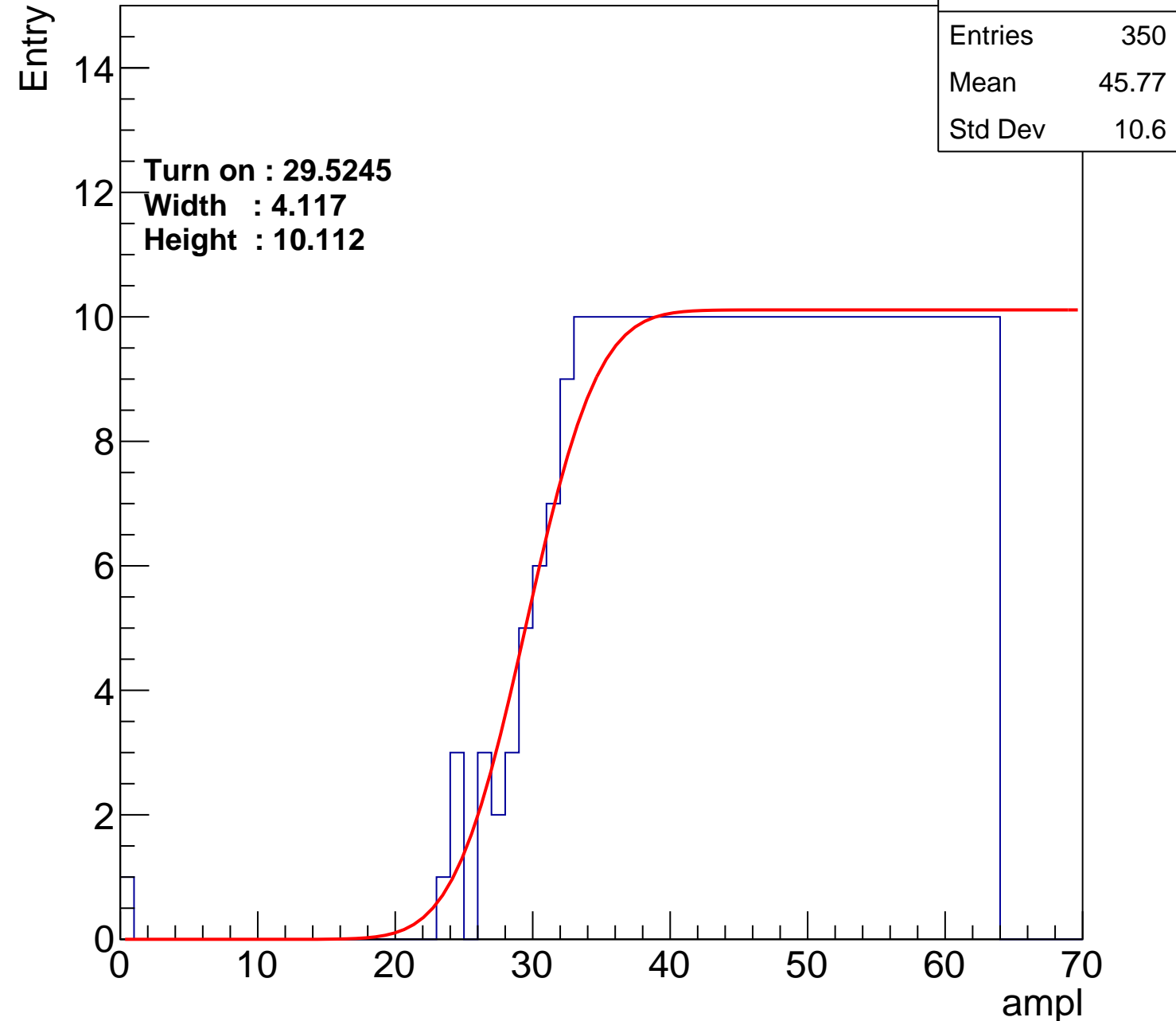
Width : 4.117

Height : 10.112

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch54

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	364
Mean	45.03
Std Dev	11.13

Turn on : 27.9223

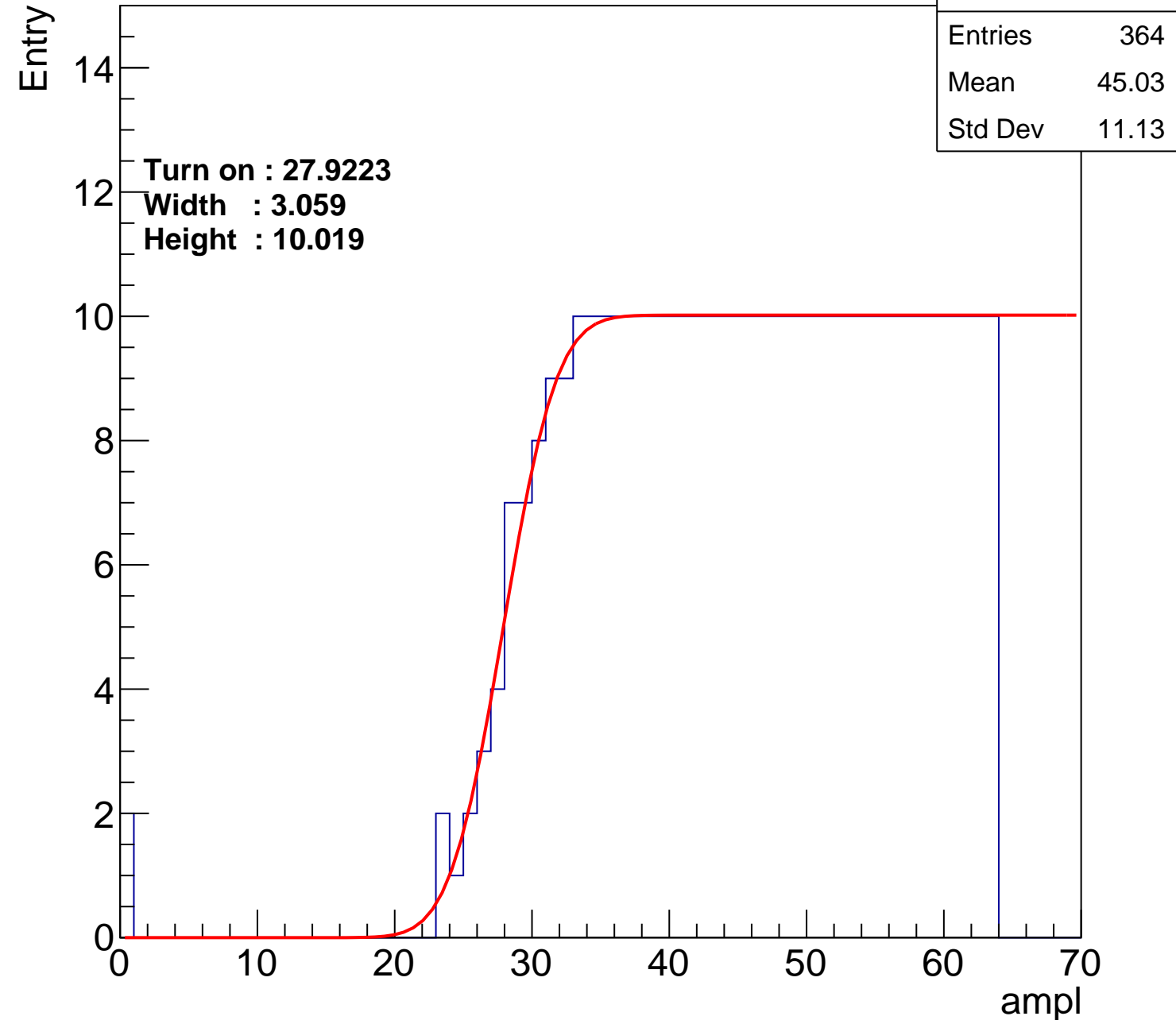
Width : 3.059

Height : 10.019

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L001S, U20-ch55

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	351
Mean	45.63
Std Dev	10.98

**Turn on : 29.3400**

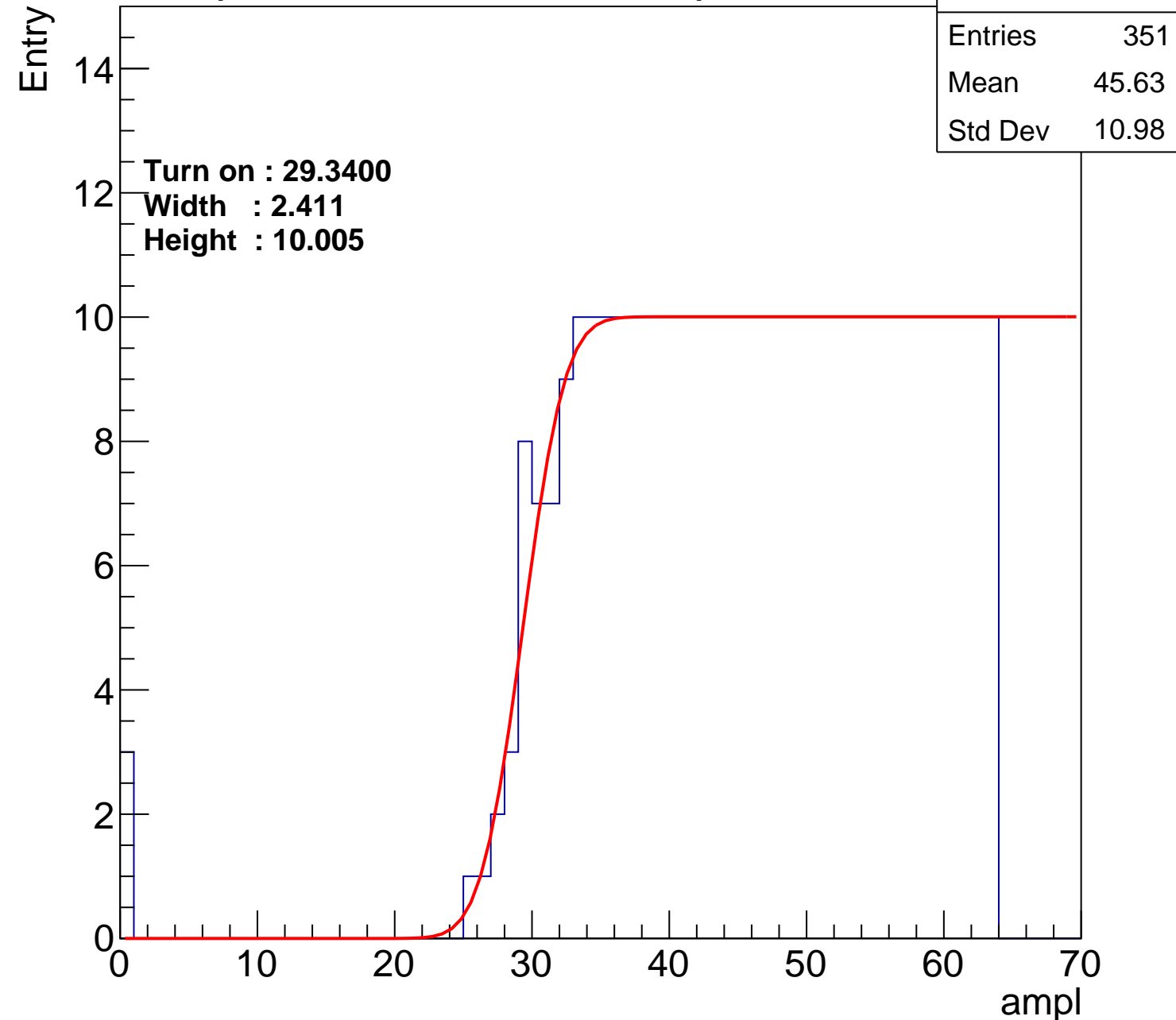
**Width : 2.411**

**Height : 10.005**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch56

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	366
Mean	44.69
Std Dev	11.83

Turn on : 28.7086

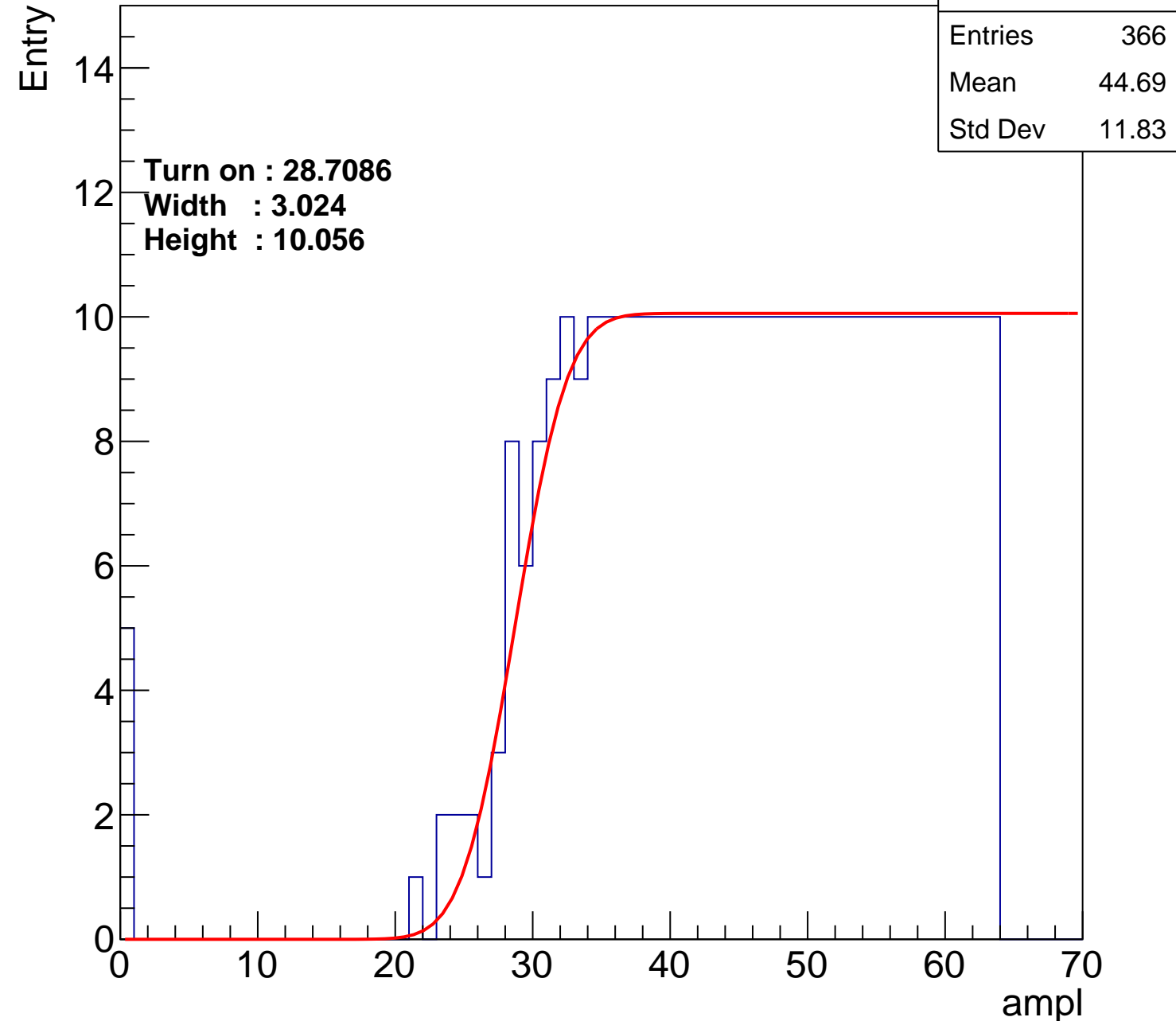
Width : 3.024

Height : 10.056

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch57

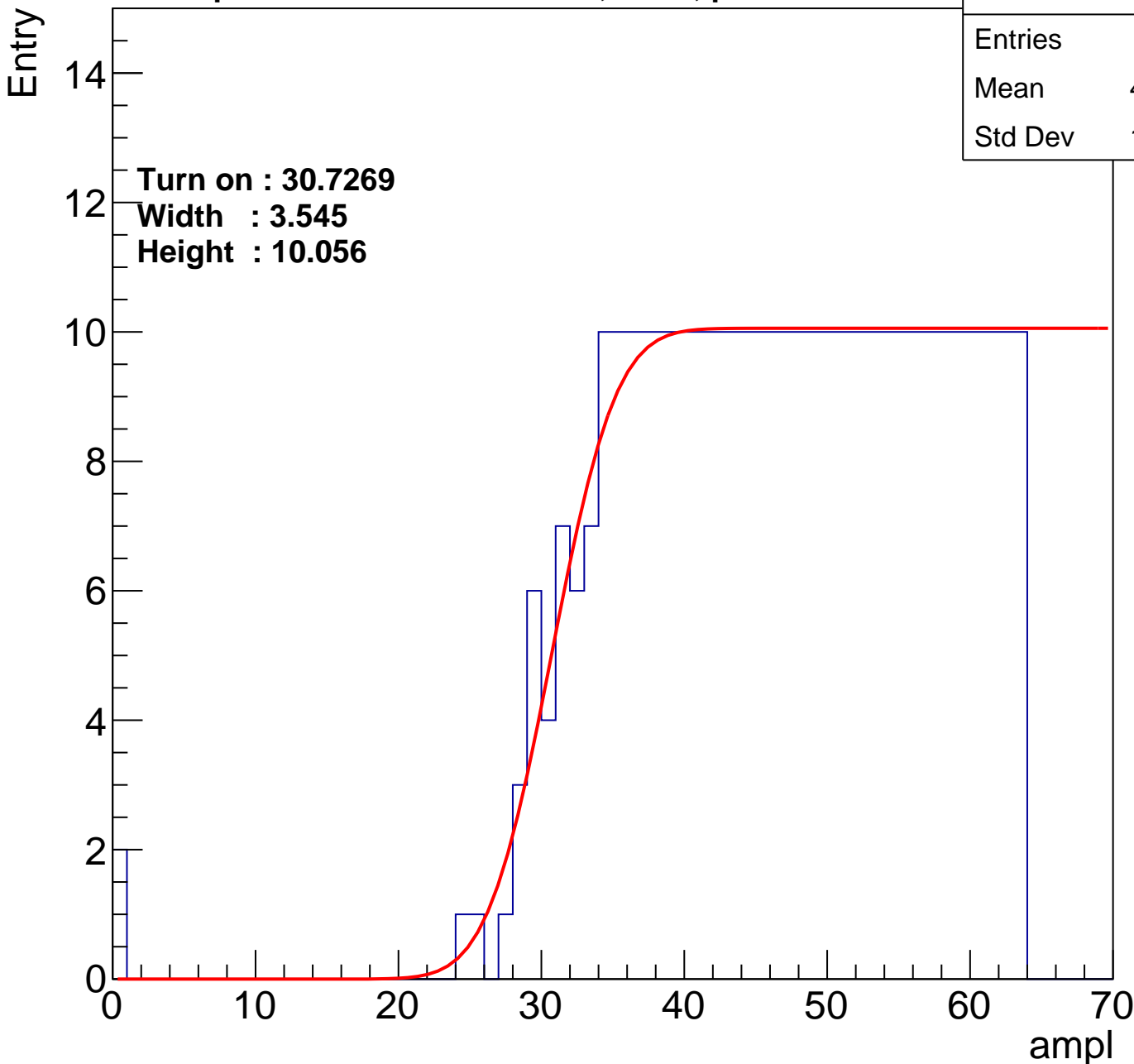
**calib\_packv5\_042523\_0143.root, FC#9, port A1**

Entries	338
Mean	46.28
Std Dev	10.53

**Turn on : 30.7269**

**Width : 3.545**

**Height : 10.056**



# B0L001S, U20-ch58

calib\_packv5\_042523\_0143.root, FC#9, port A1

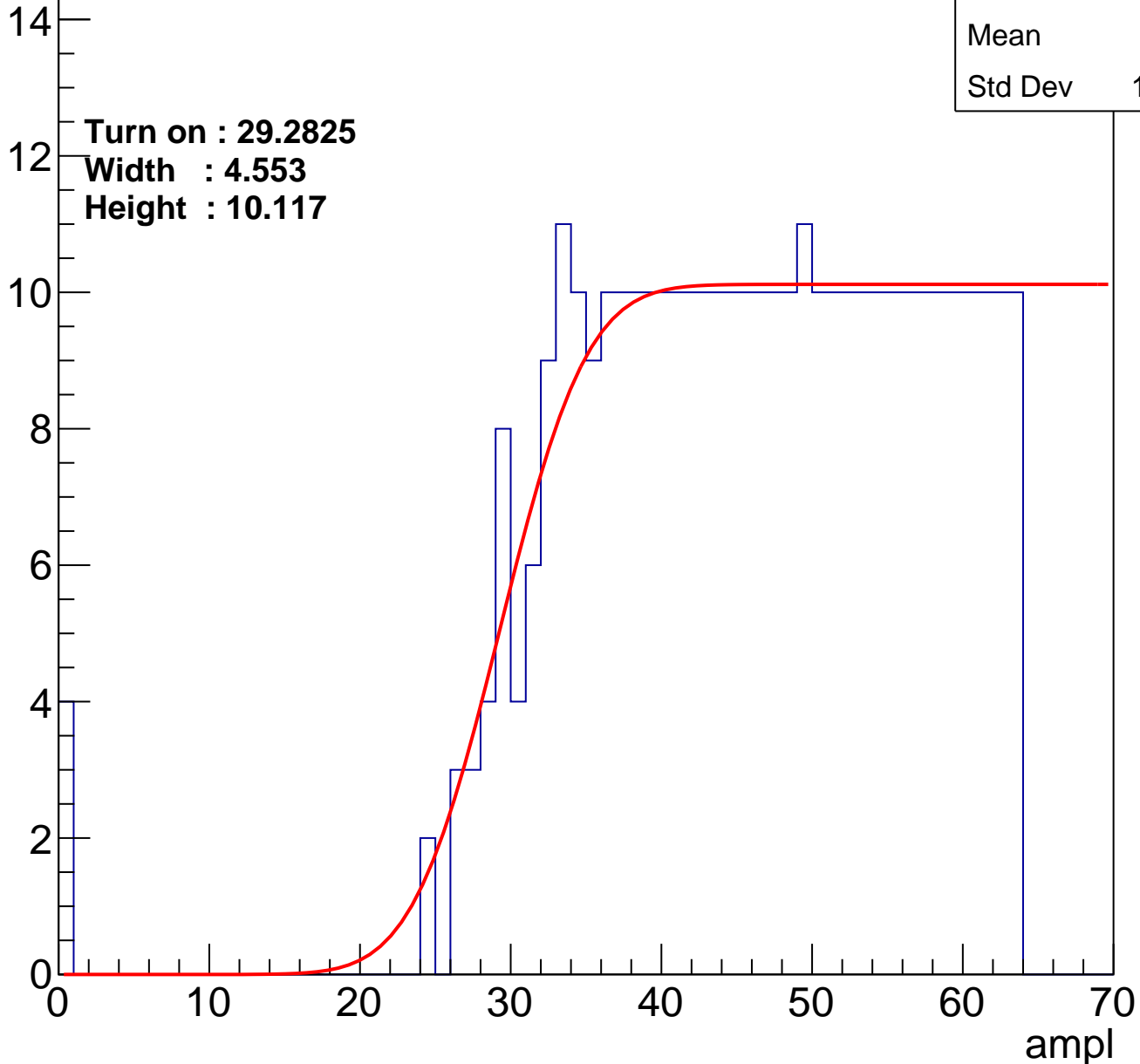
Entries	354
Mean	45.4
Std Dev	11.33

Turn on : 29.2825

Width : 4.553

Height : 10.117

Entry



# B0L001S, U20-ch59

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	366
Mean	44.88
Std Dev	11.36

Turn on : 27.8232

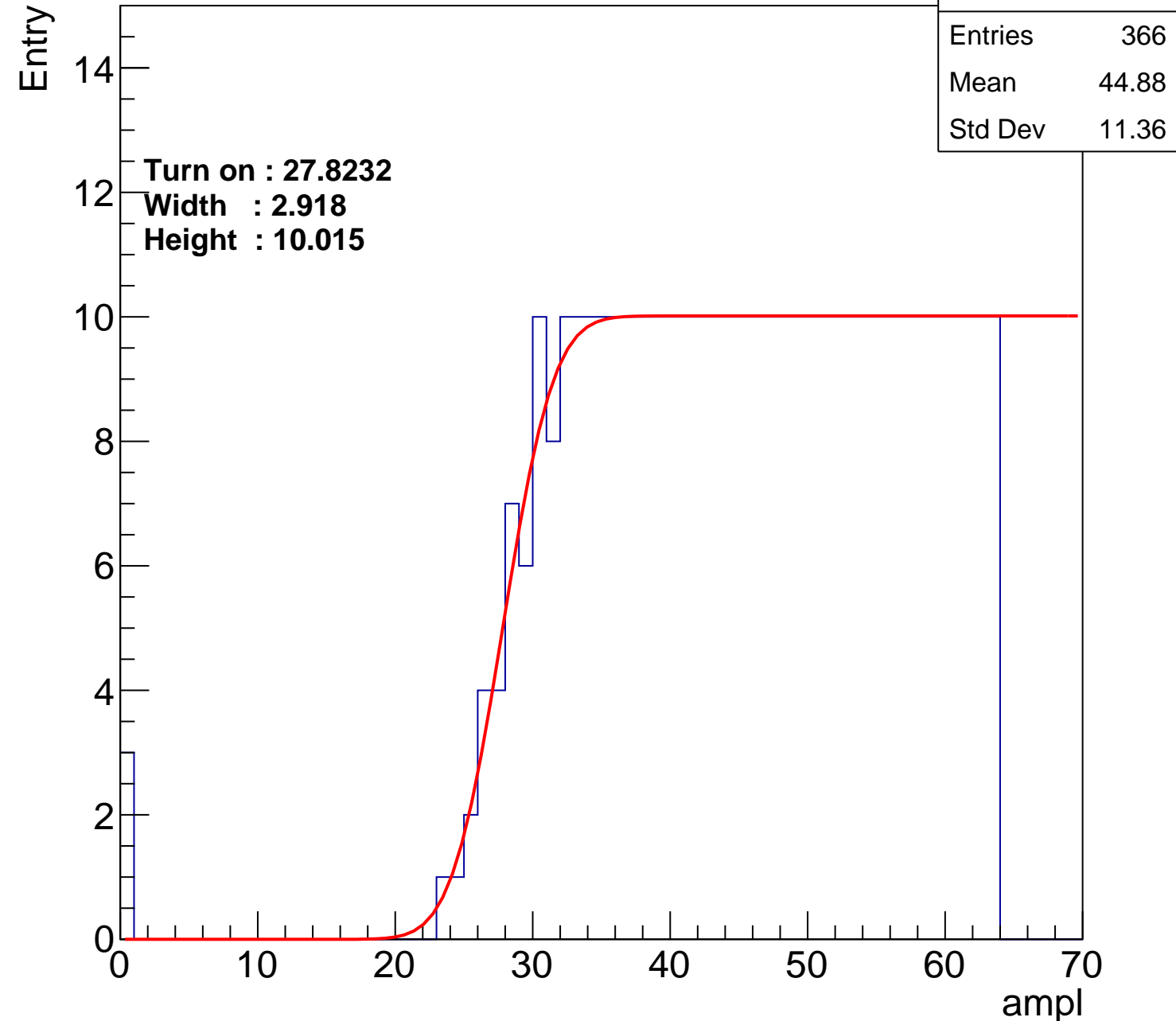
Width : 2.918

Height : 10.015

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch60

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	363
Mean	44.94
Std Dev	11.51

**Turn on : 28.5443**

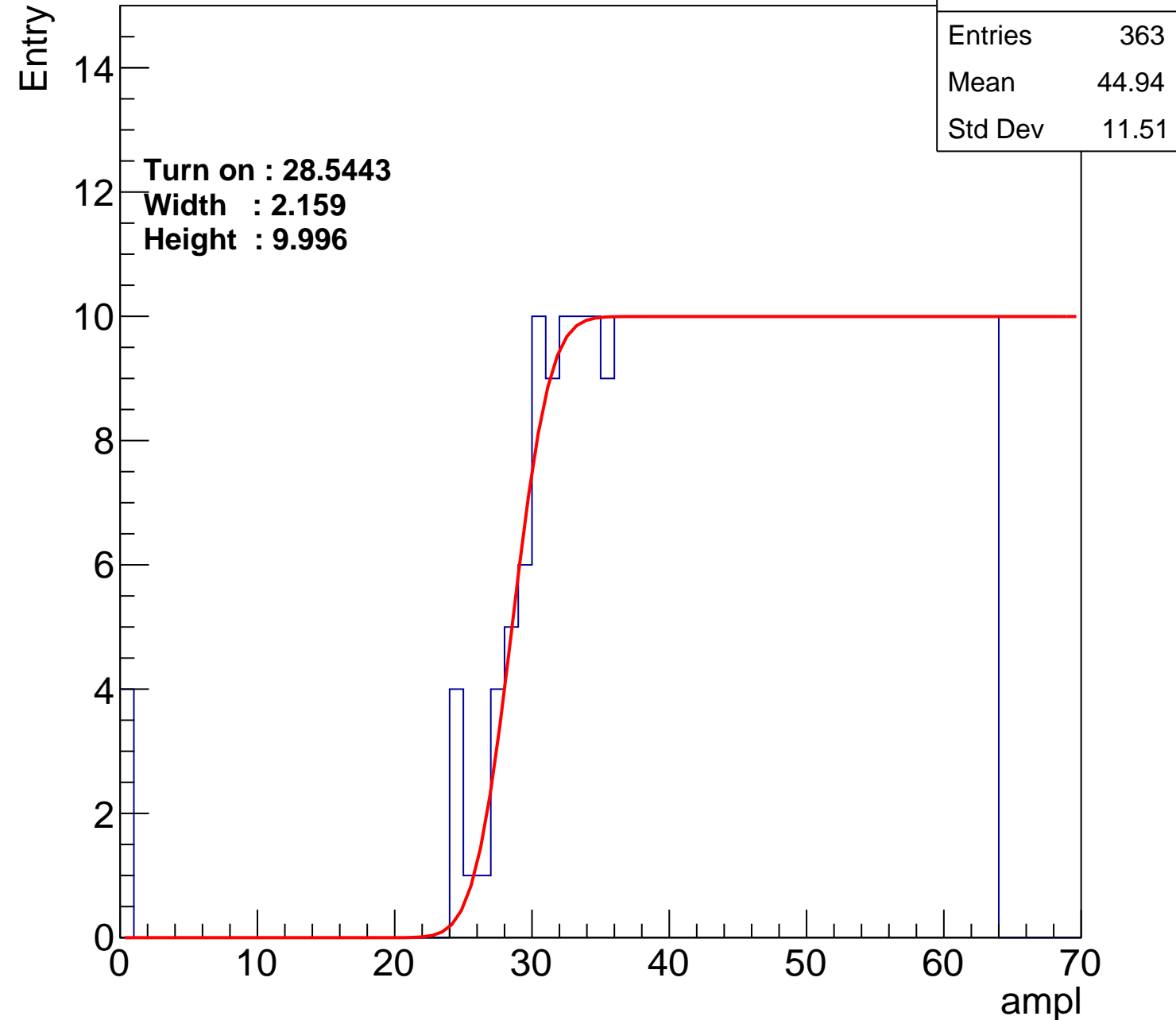
**Width : 2.159**

**Height : 9.996**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch61

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	368
Mean	44.72
Std Dev	11.58

Turn on : 27.2049

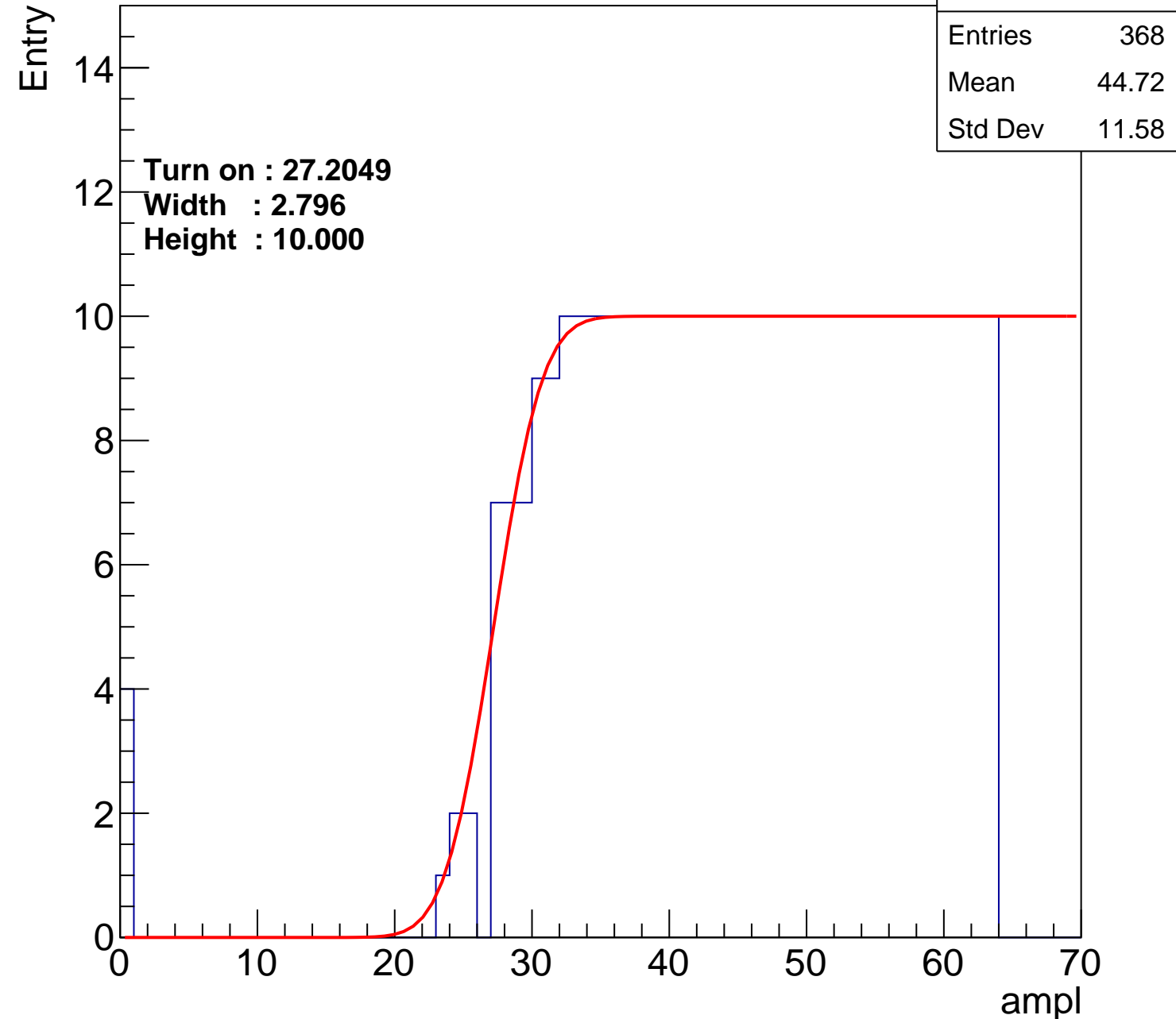
Width : 2.796

Height : 10.000

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch62

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	365
Mean	45
Std Dev	11.14

Turn on : 28.1513

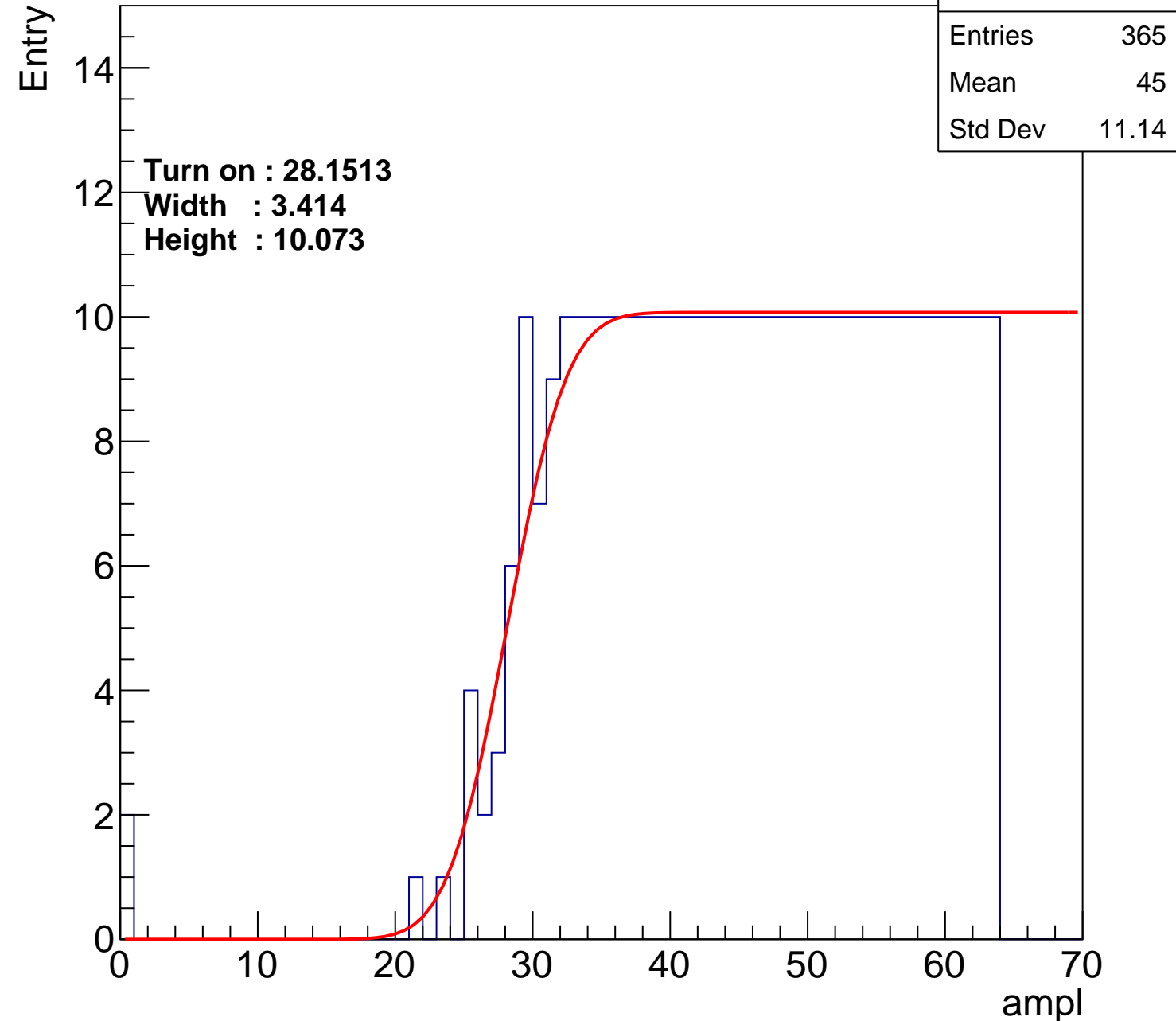
Width : 3.414

Height : 10.073

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L001S, U20-ch63

calib\_packv5\_042523\_0143.root, FC#9, port A1

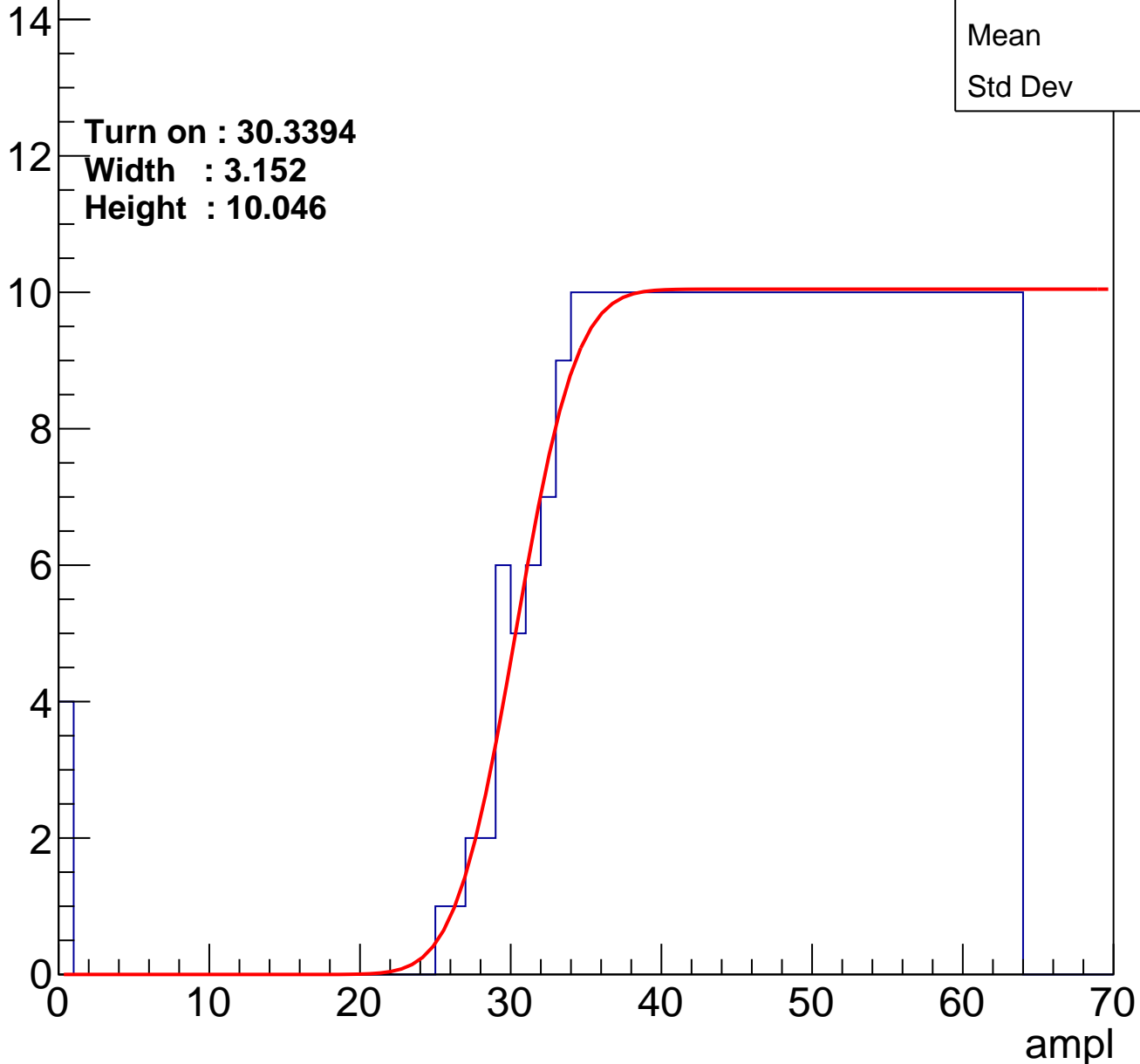
Entries	343
Mean	45.9
Std Dev	11.1

Turn on : 30.3394

Width : 3.152

Height : 10.046

Entry



# B0L001S, U20-ch64

calib\_packv5\_042523\_0143.root, FC#9, port A1

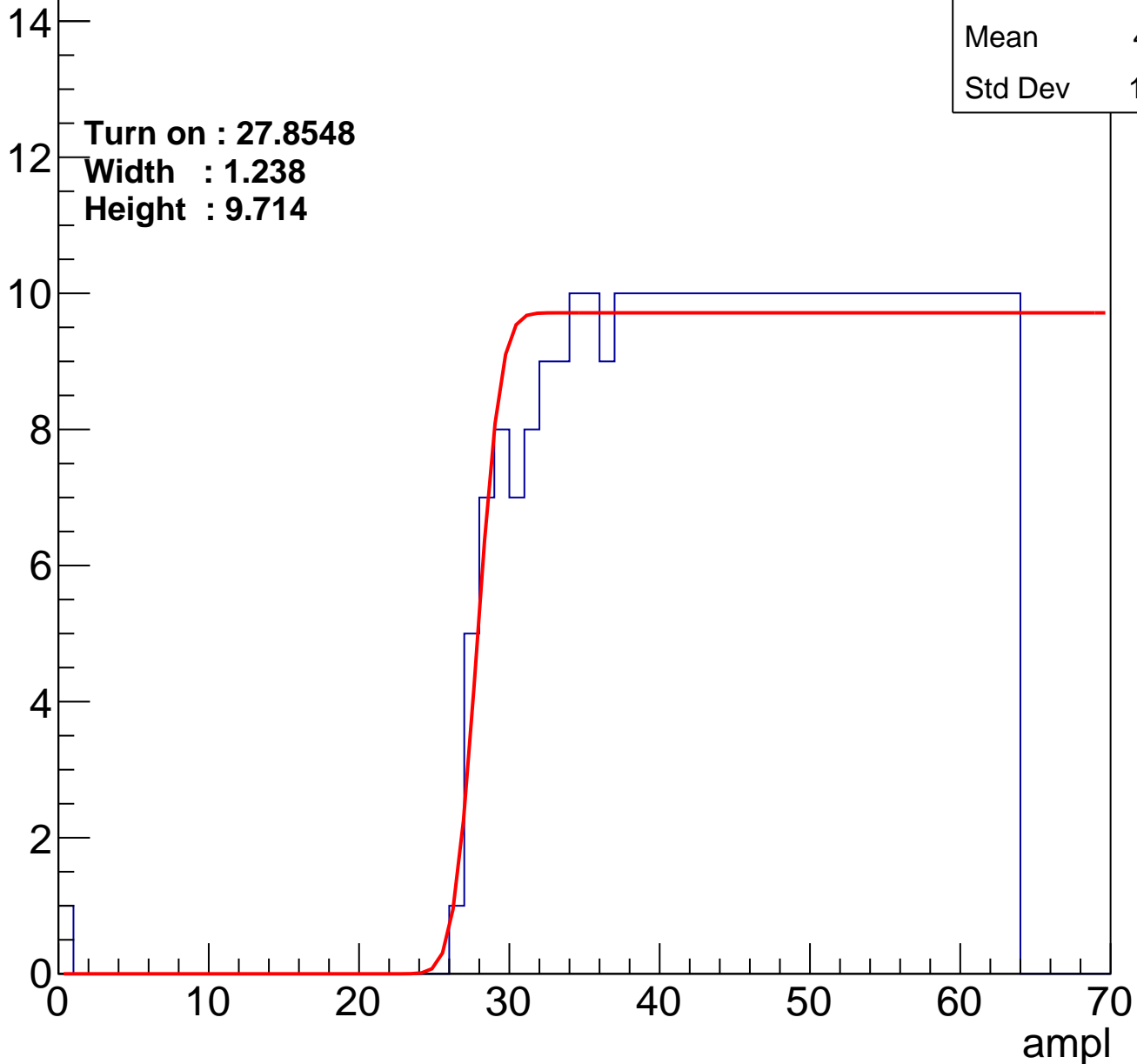
Entries	354
Mean	45.61
Std Dev	10.63

Turn on : 27.8548

Width : 1.238

Height : 9.714

Entry



# B0L001S, U20-ch65

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	378
Mean	44.41
Std Dev	11.31

Turn on : 26.7047

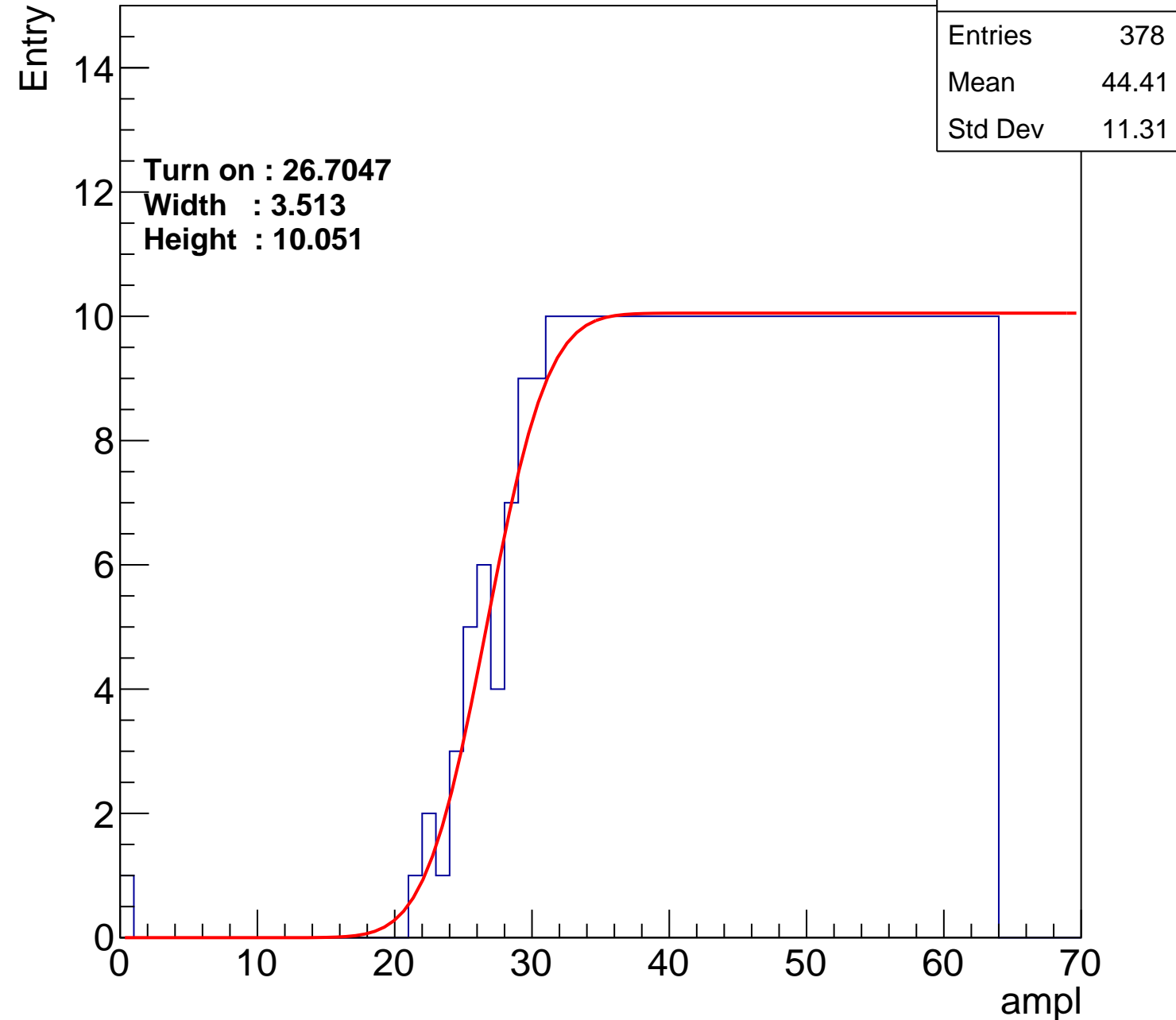
Width : 3.513

Height : 10.051

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch66

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	376
Mean	44.48
Std Dev	11.61

Turn on : 27.2724

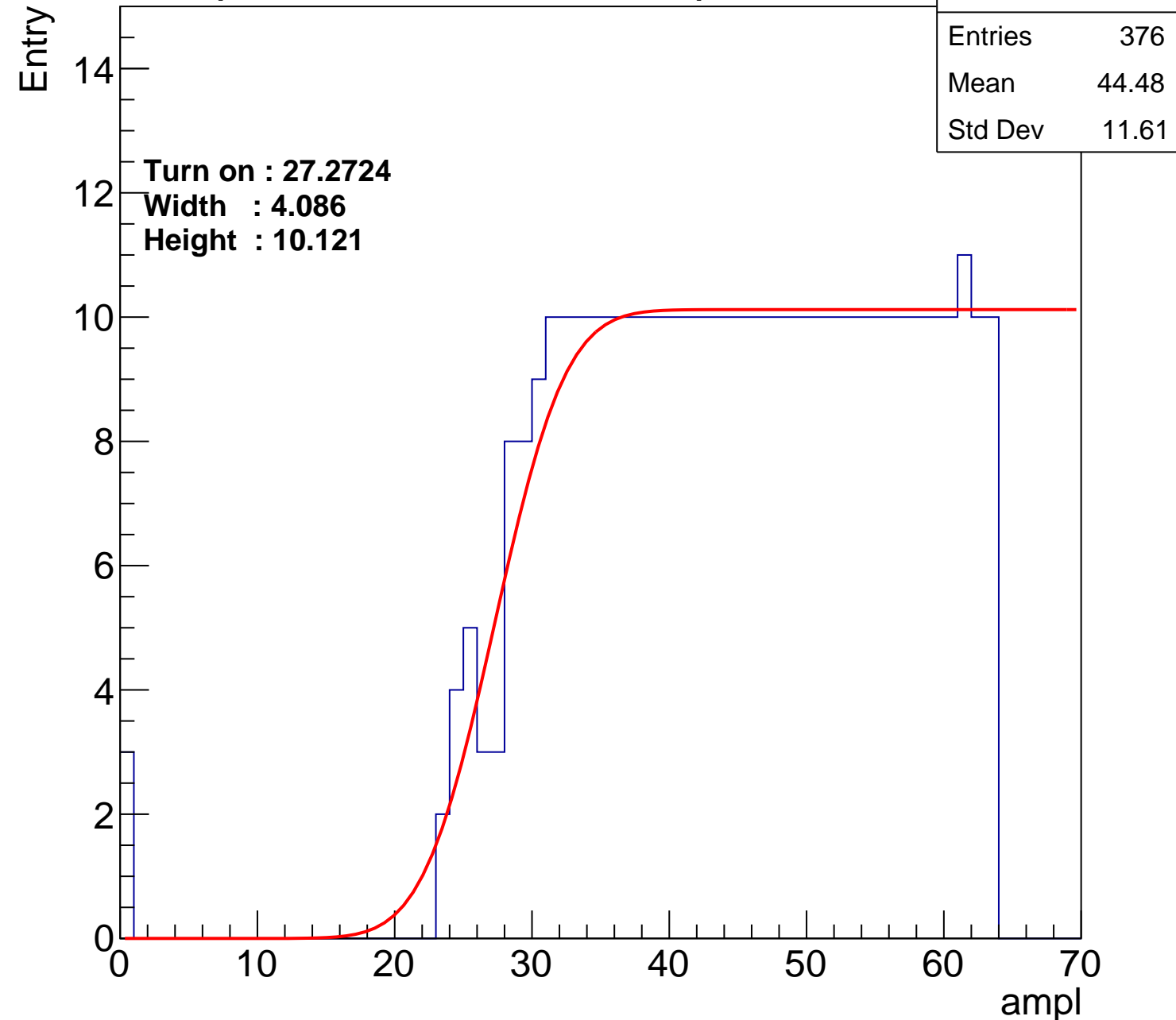
Width : 4.086

Height : 10.121

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch67

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	380
Mean	44.11
Std Dev	12.03

Turn on : 26.4511

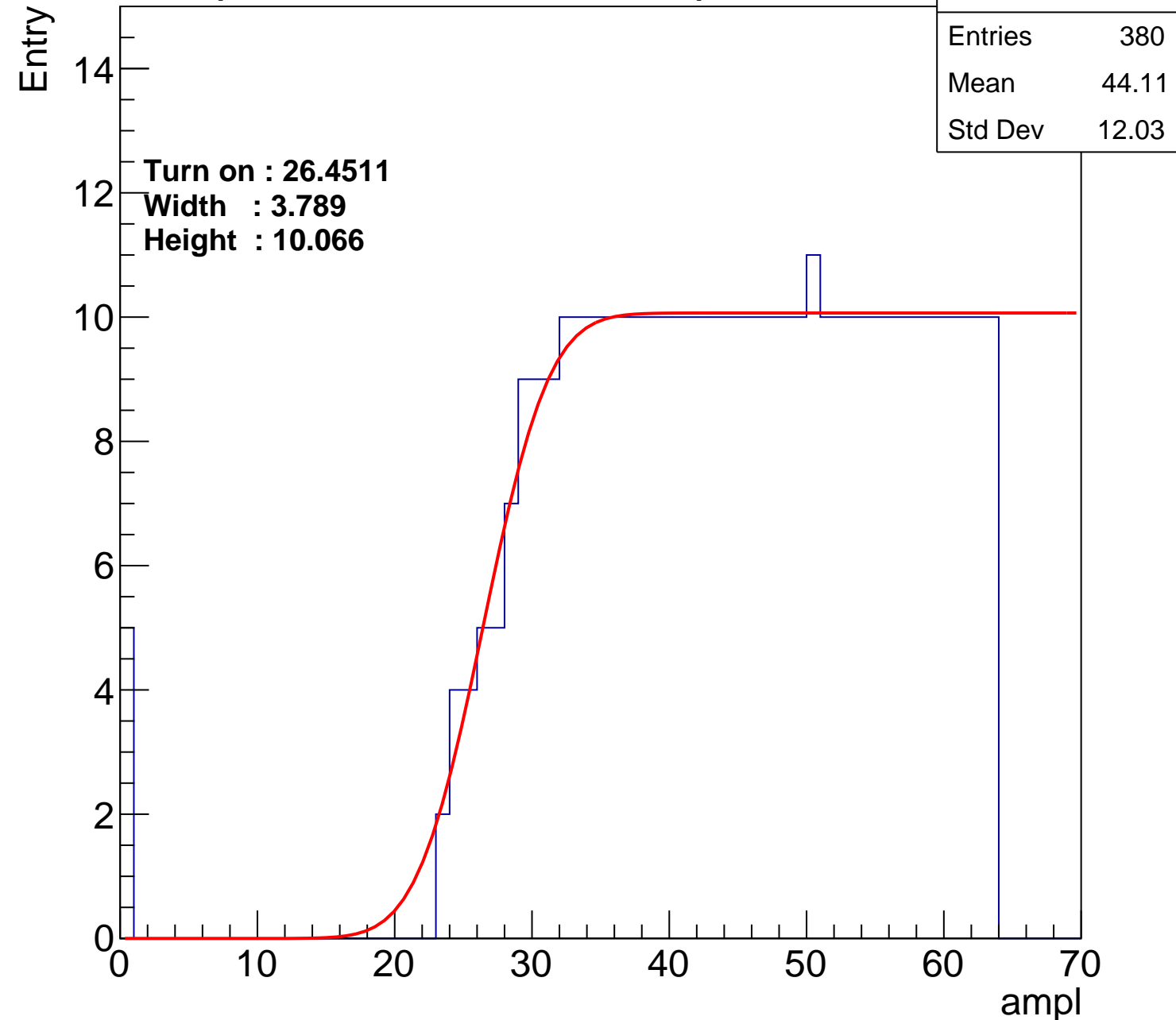
Width : 3.789

Height : 10.066

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch68

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	389
Mean	43.67
Std Dev	12.11

Turn on : 25.5779

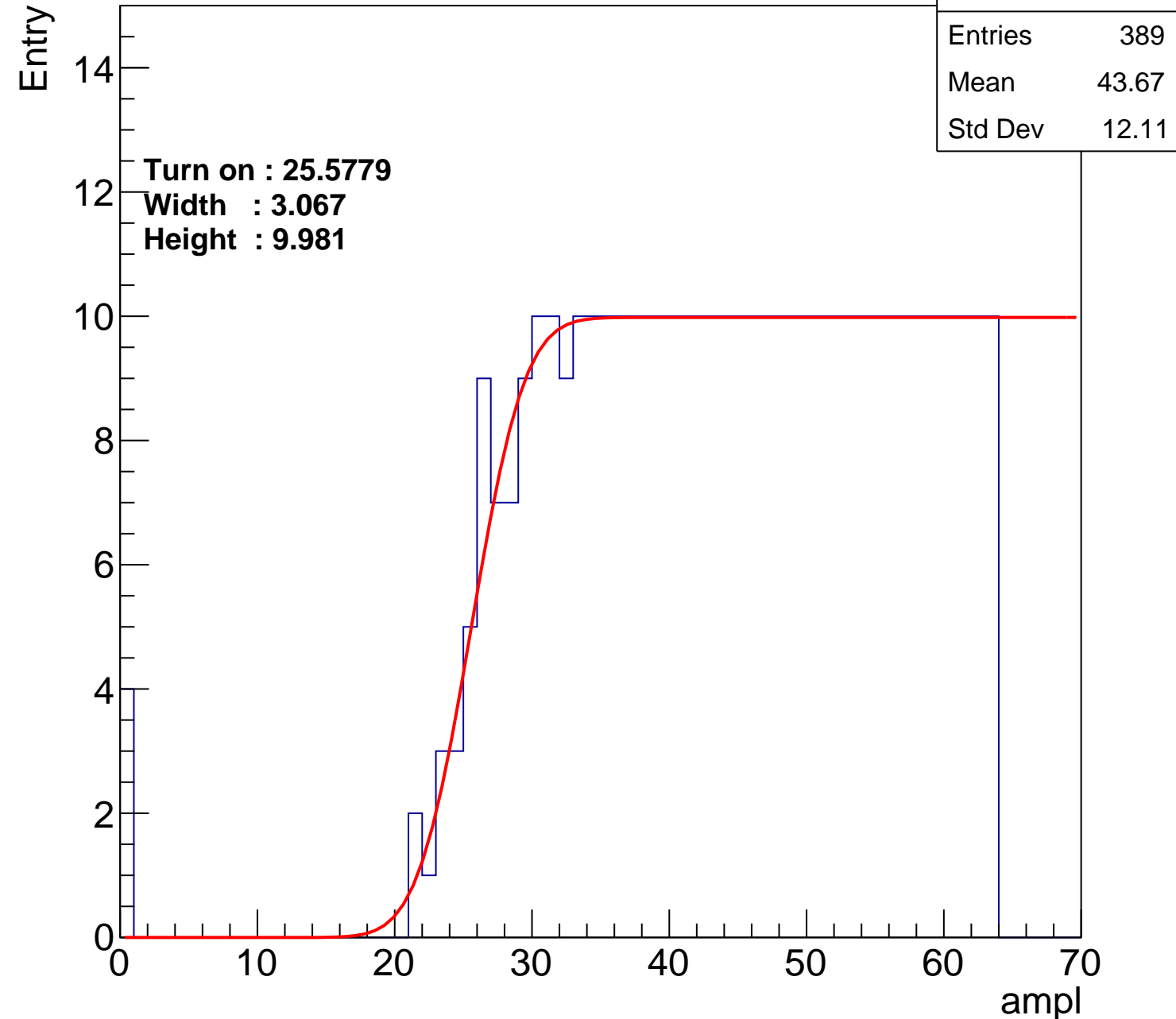
Width : 3.067

Height : 9.981

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch69

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	352
Mean	45.62
Std Dev	10.84

Turn on : 29.4836

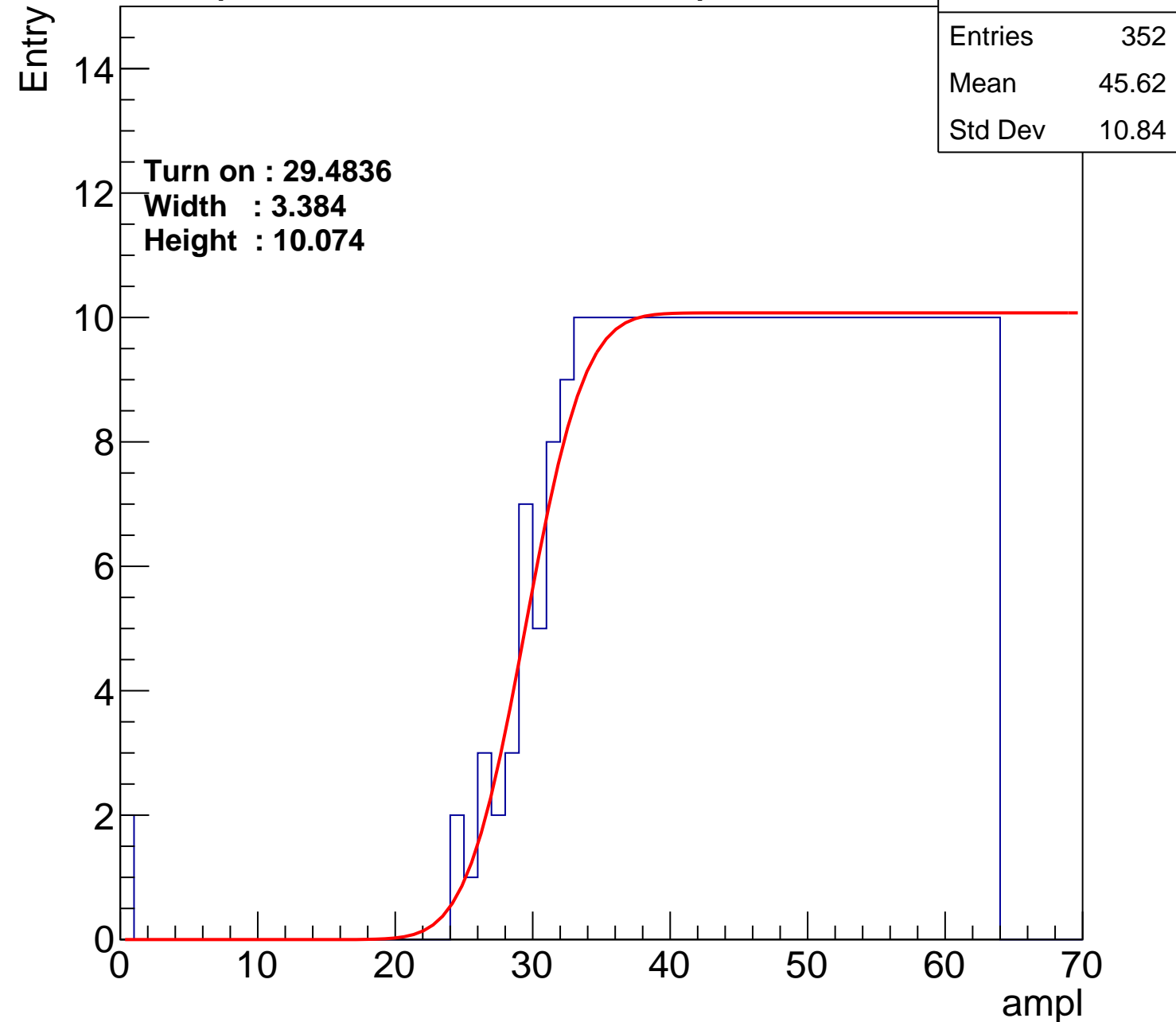
Width : 3.384

Height : 10.074

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch70

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	366
Mean	44.89
Std Dev	11.34

Turn on : 27.2832

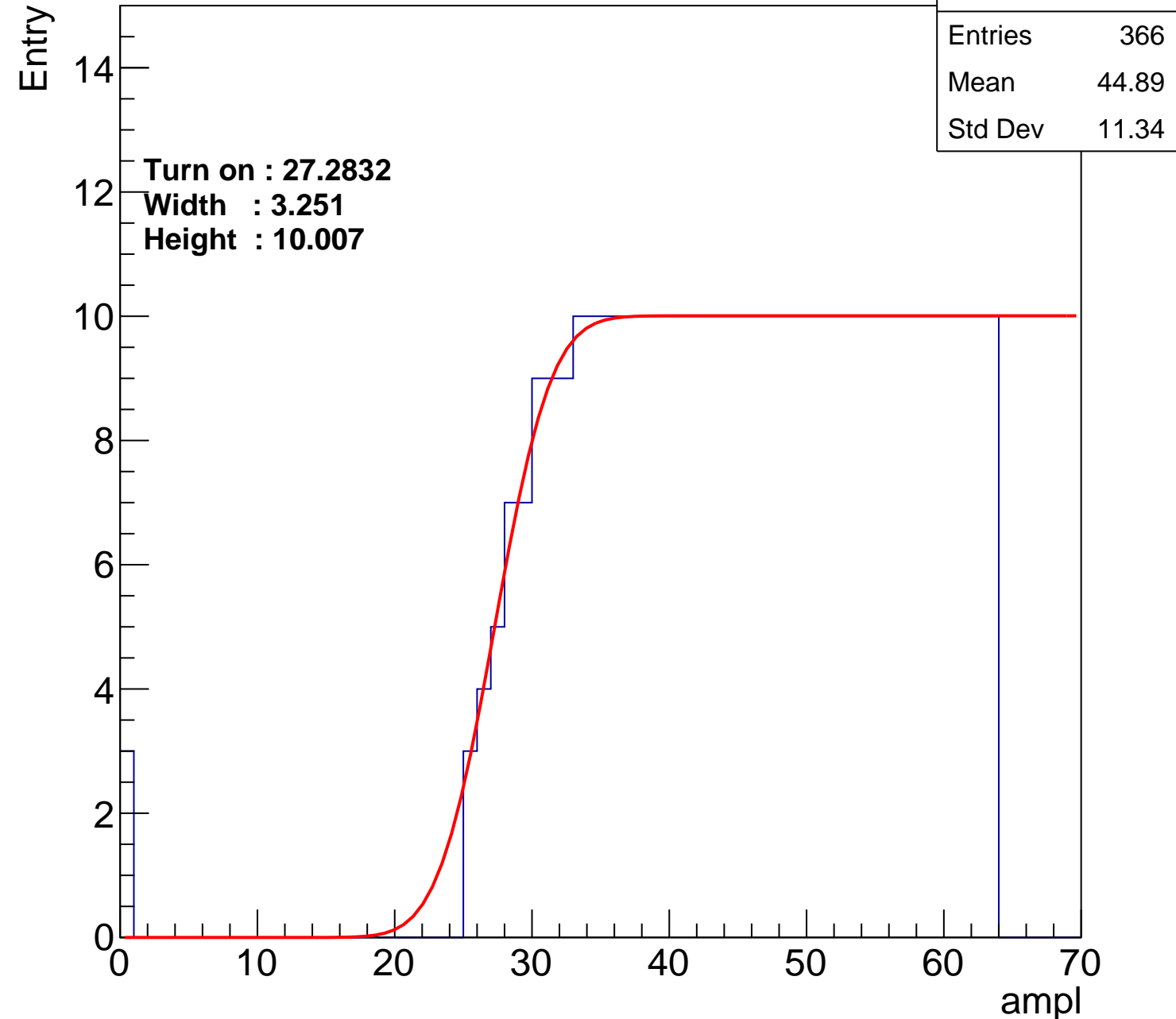
Width : 3.251

Height : 10.007

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L001S, U20-ch71

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	351
Mean	45.54
Std Dev	11.13

**Turn on : 29.8774**

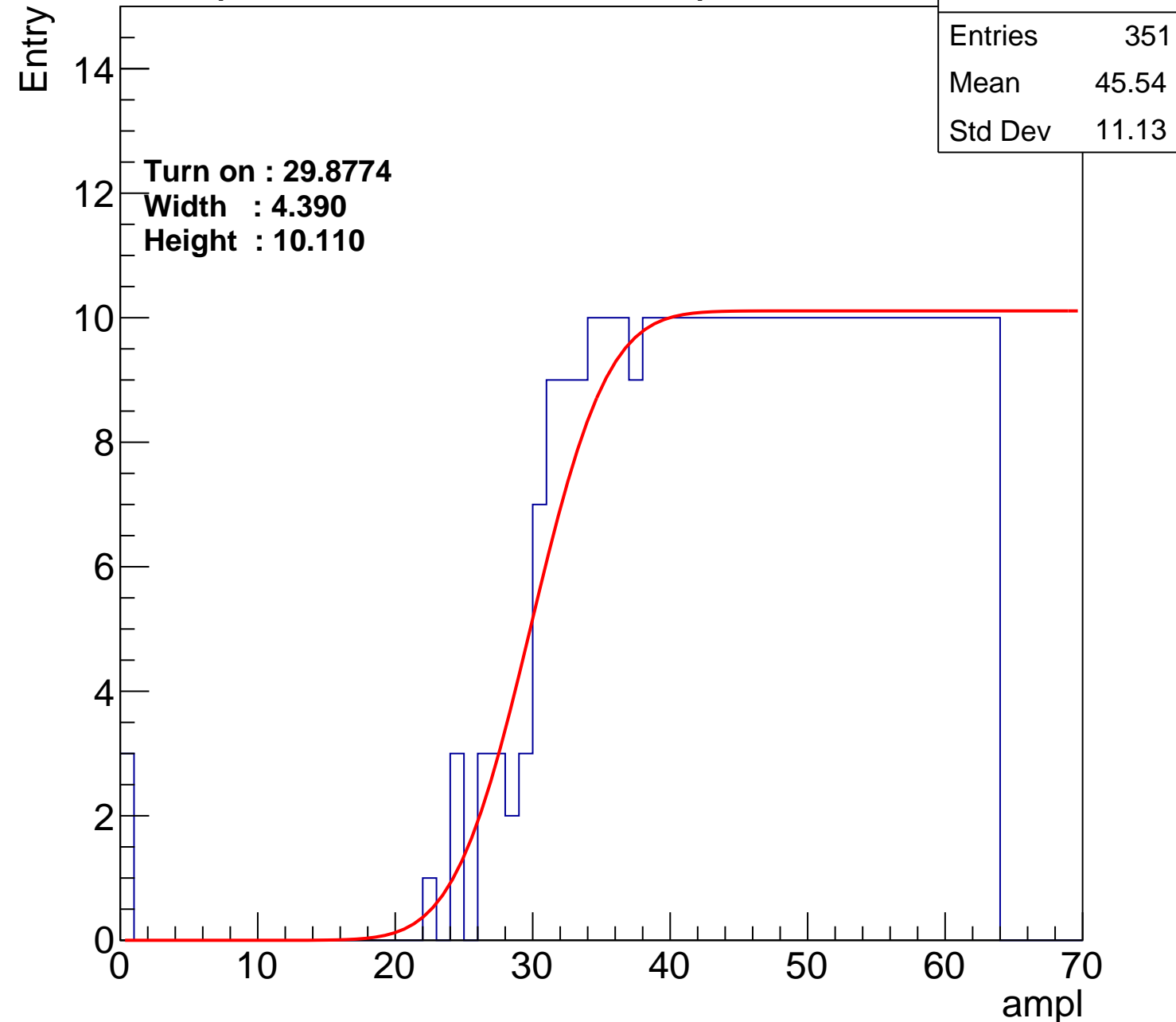
**Width : 4.390**

**Height : 10.110**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch72

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	357
Mean	45.22
Std Dev	11.4

**Turn on : 29.4046**

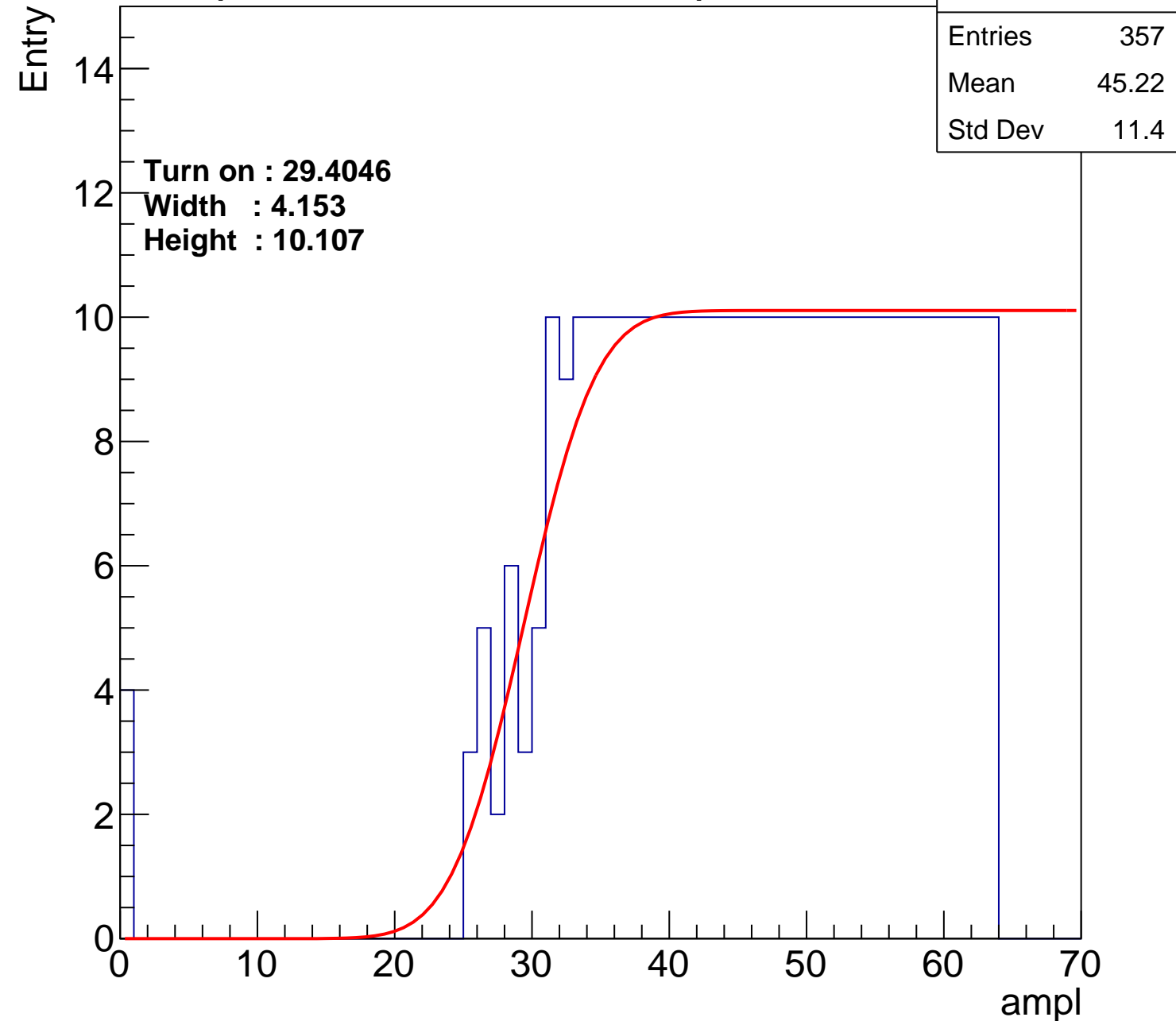
**Width : 4.153**

**Height : 10.107**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch73

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	372
Mean	44.59
Std Dev	11.49

Turn on : 27.2521

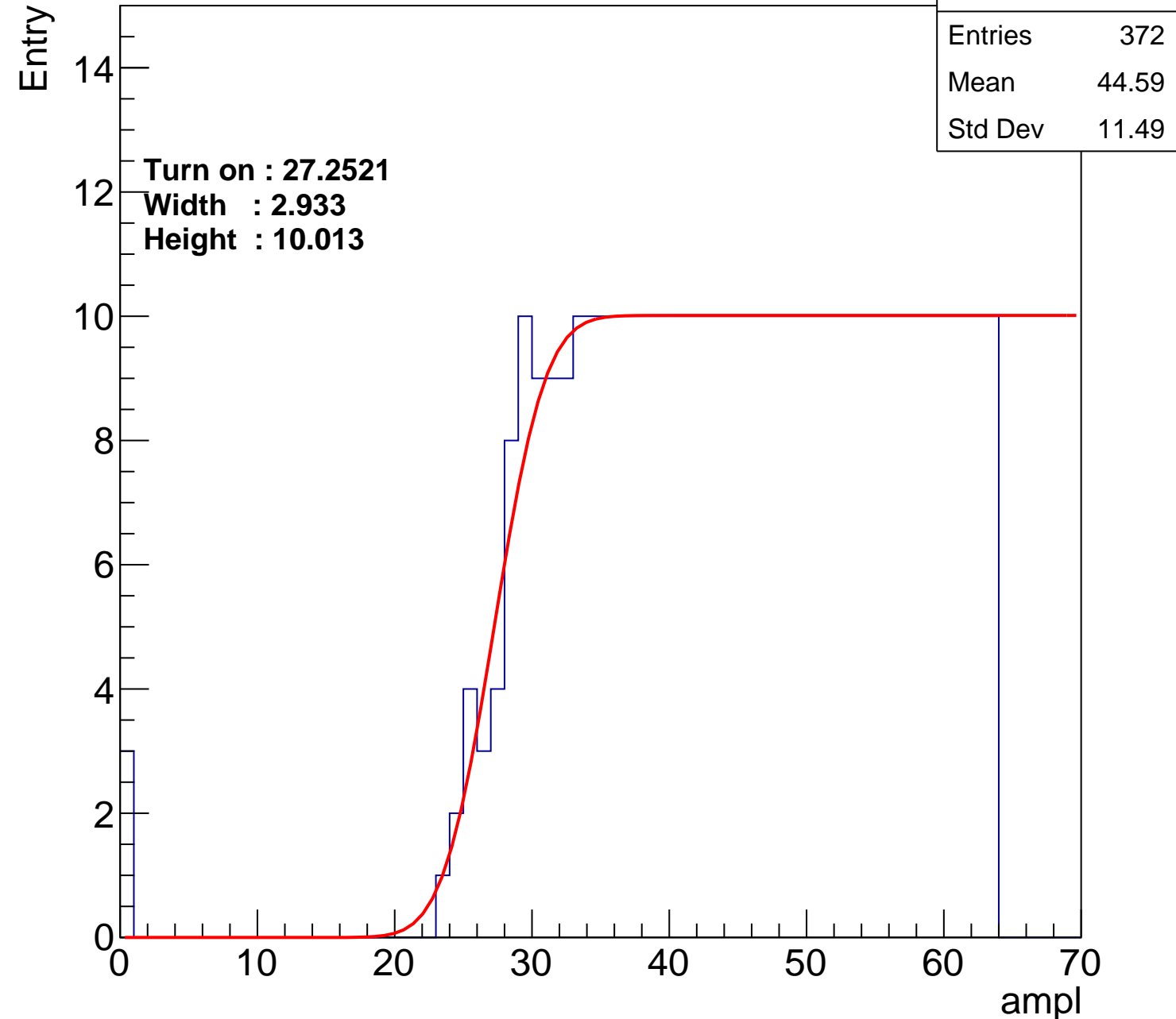
Width : 2.933

Height : 10.013

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch74

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	370
Mean	44.68
Std Dev	11.46

Turn on : 27.5636

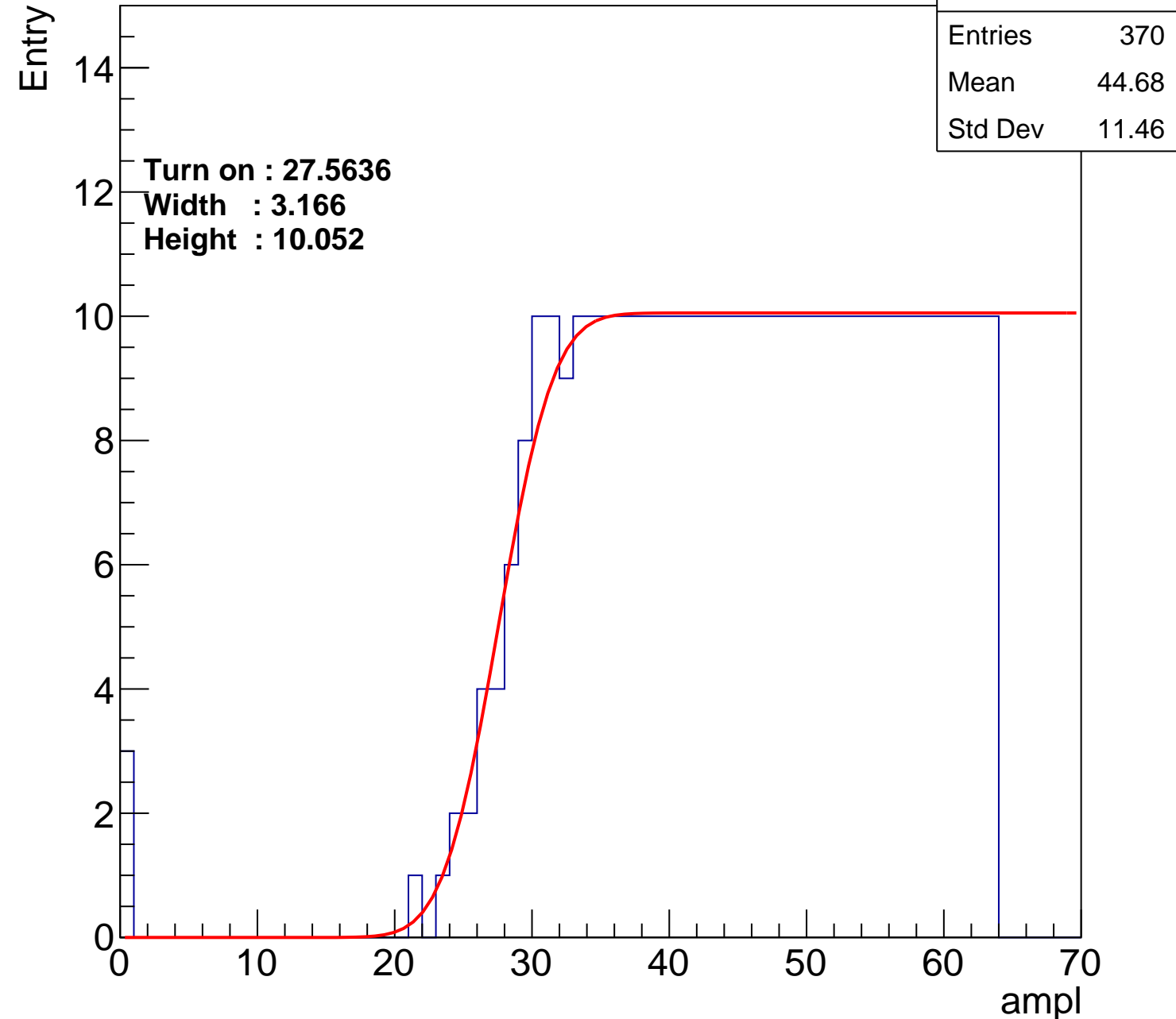
Width : 3.166

Height : 10.052

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch75

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	384
Mean	43.99
Std Dev	11.81

Turn on : 26.0522

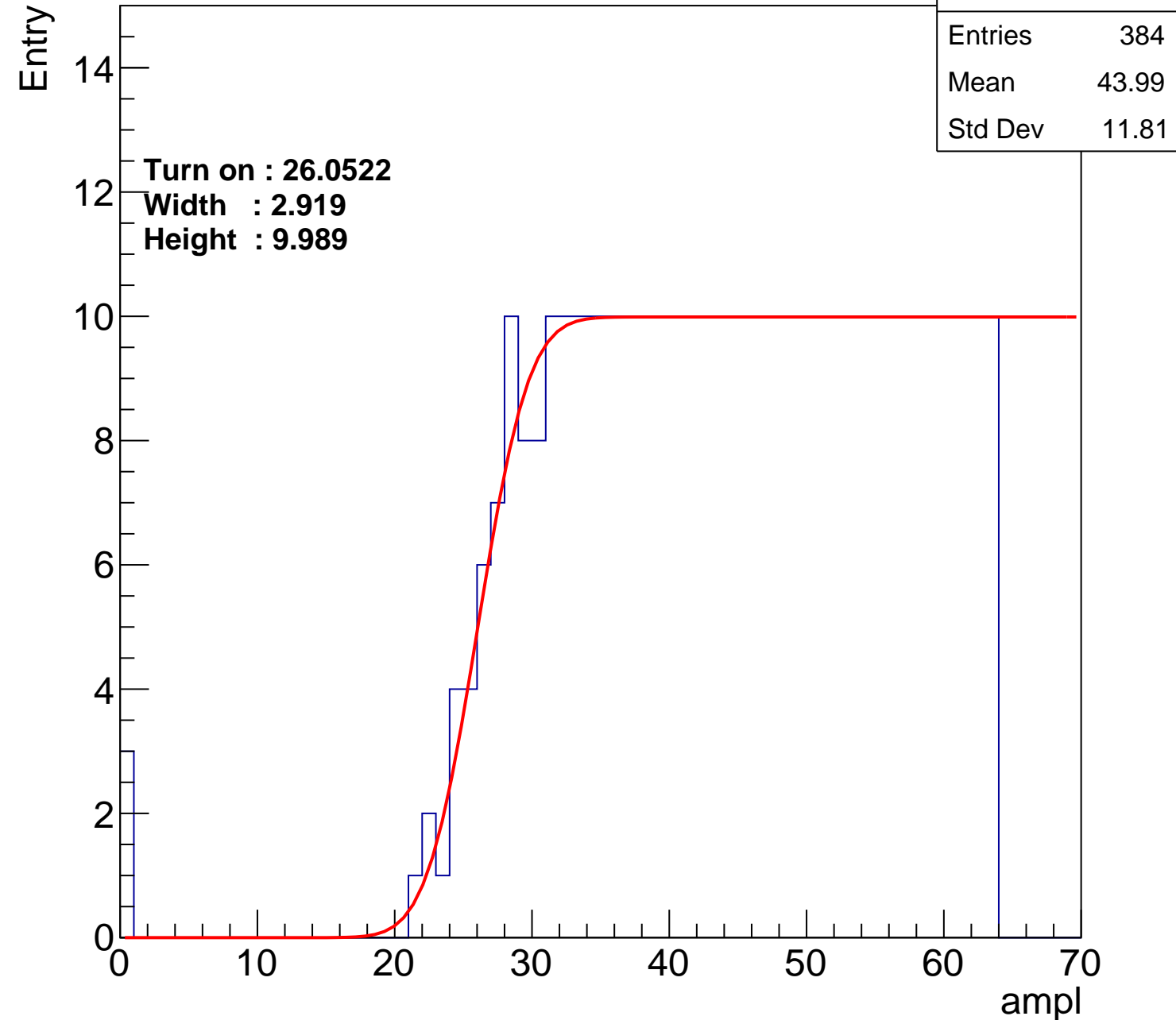
Width : 2.919

Height : 9.989

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch76

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	353
Mean	45.39
Std Dev	11.25

**Turn on : 29.5155**

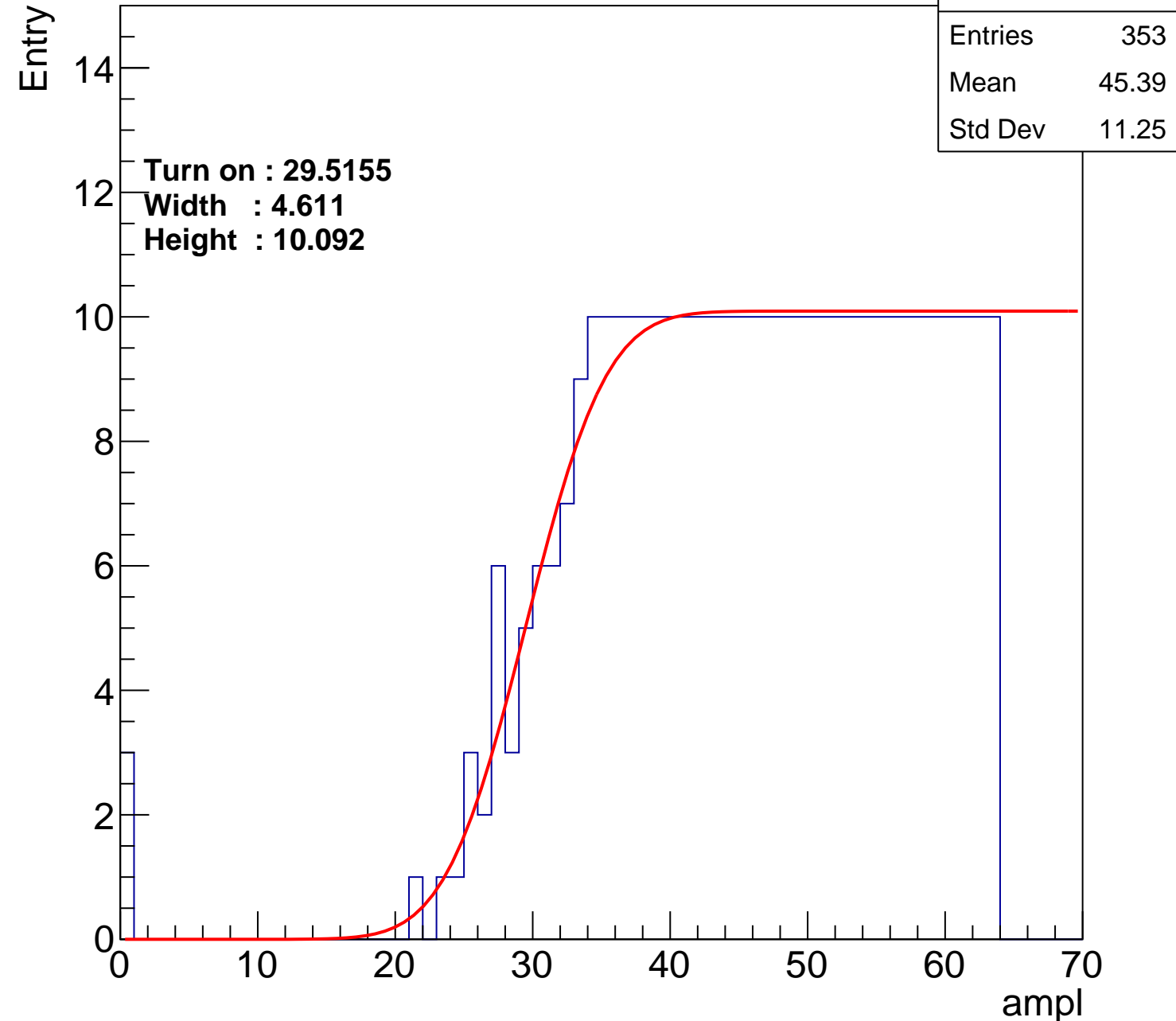
**Width : 4.611**

**Height : 10.092**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch77

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	352
Mean	45.65
Std Dev	10.69

Turn on : 29.5100

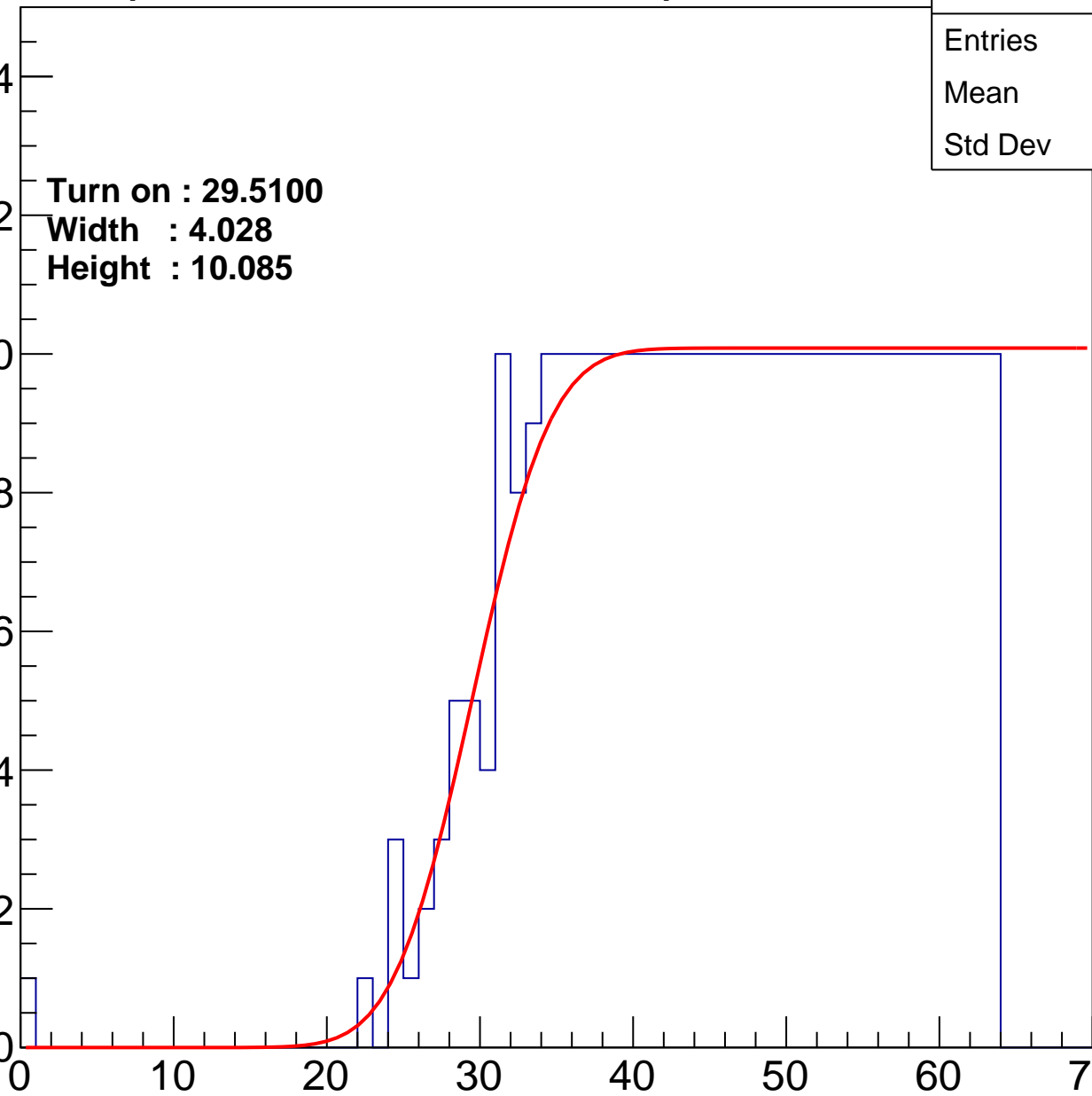
Width : 4.028

Height : 10.085

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch78

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	377
Mean	44.42
Std Dev	11.88

Turn on : 27.0125

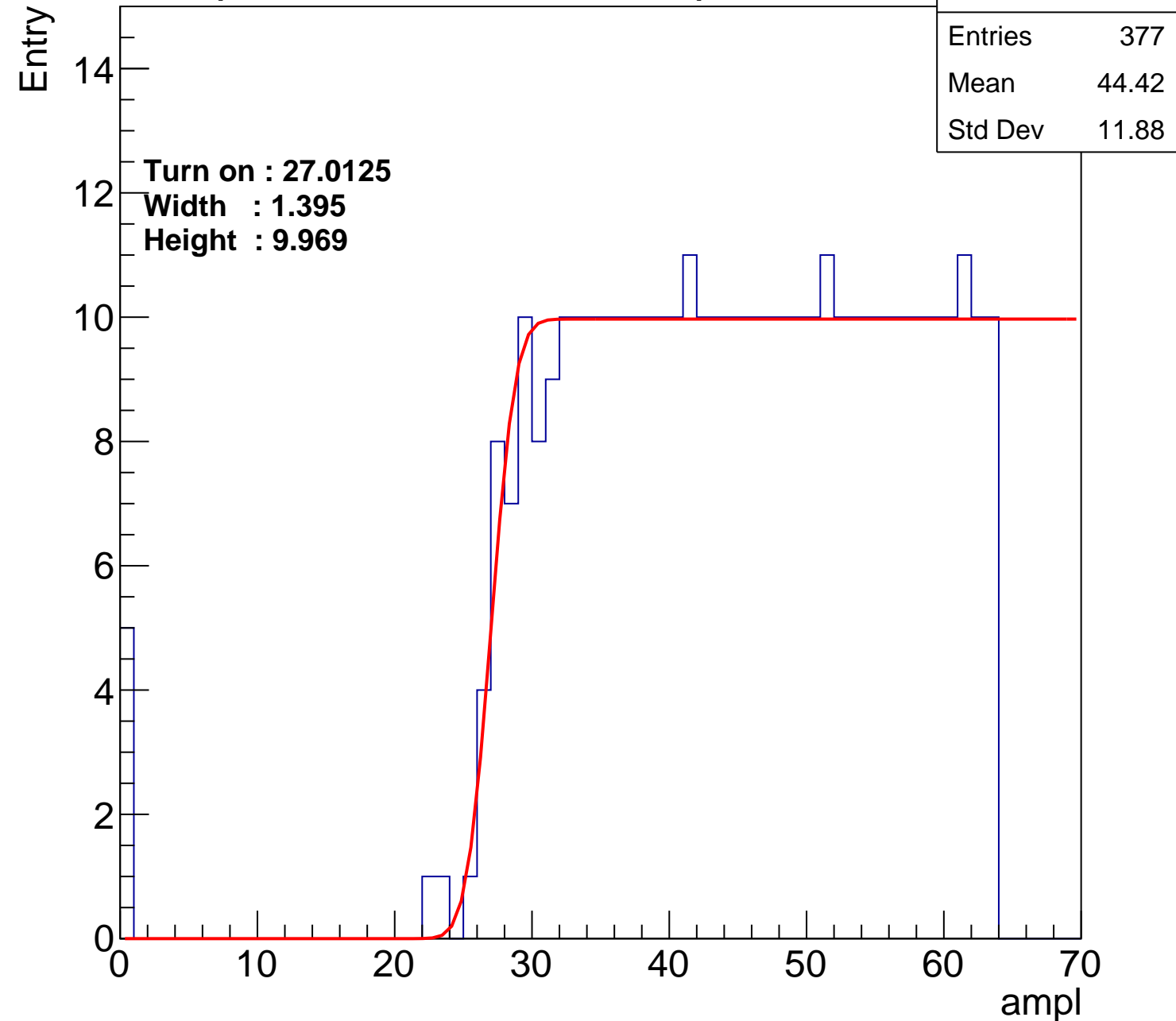
Width : 1.395

Height : 9.969

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L001S, U20-ch79

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	352
Mean	45.51
Std Dev	11.11

**Turn on : 29.0038**

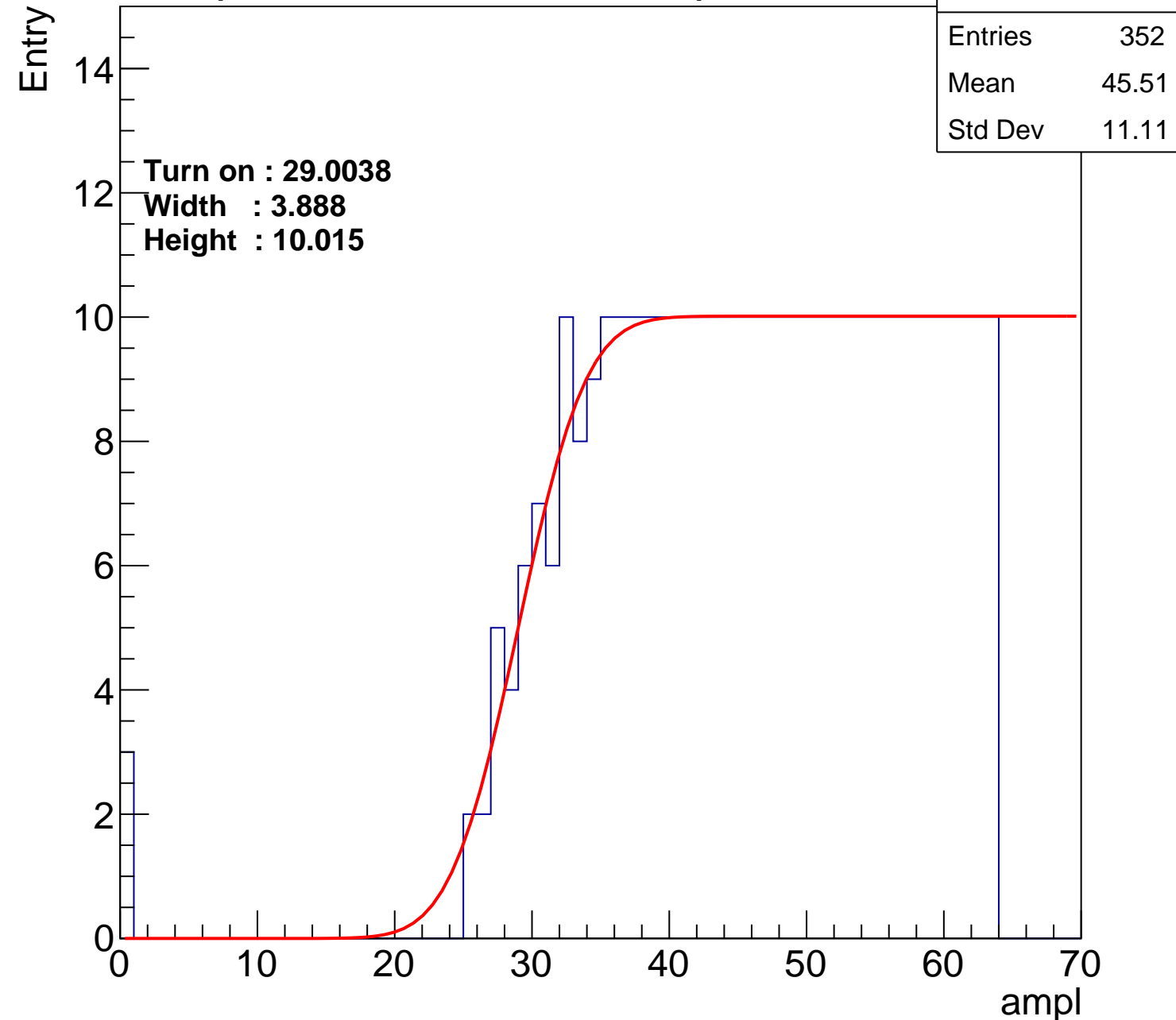
**Width : 3.888**

**Height : 10.015**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch80

calib\_packv5\_042523\_0143.root, FC#9, port A1

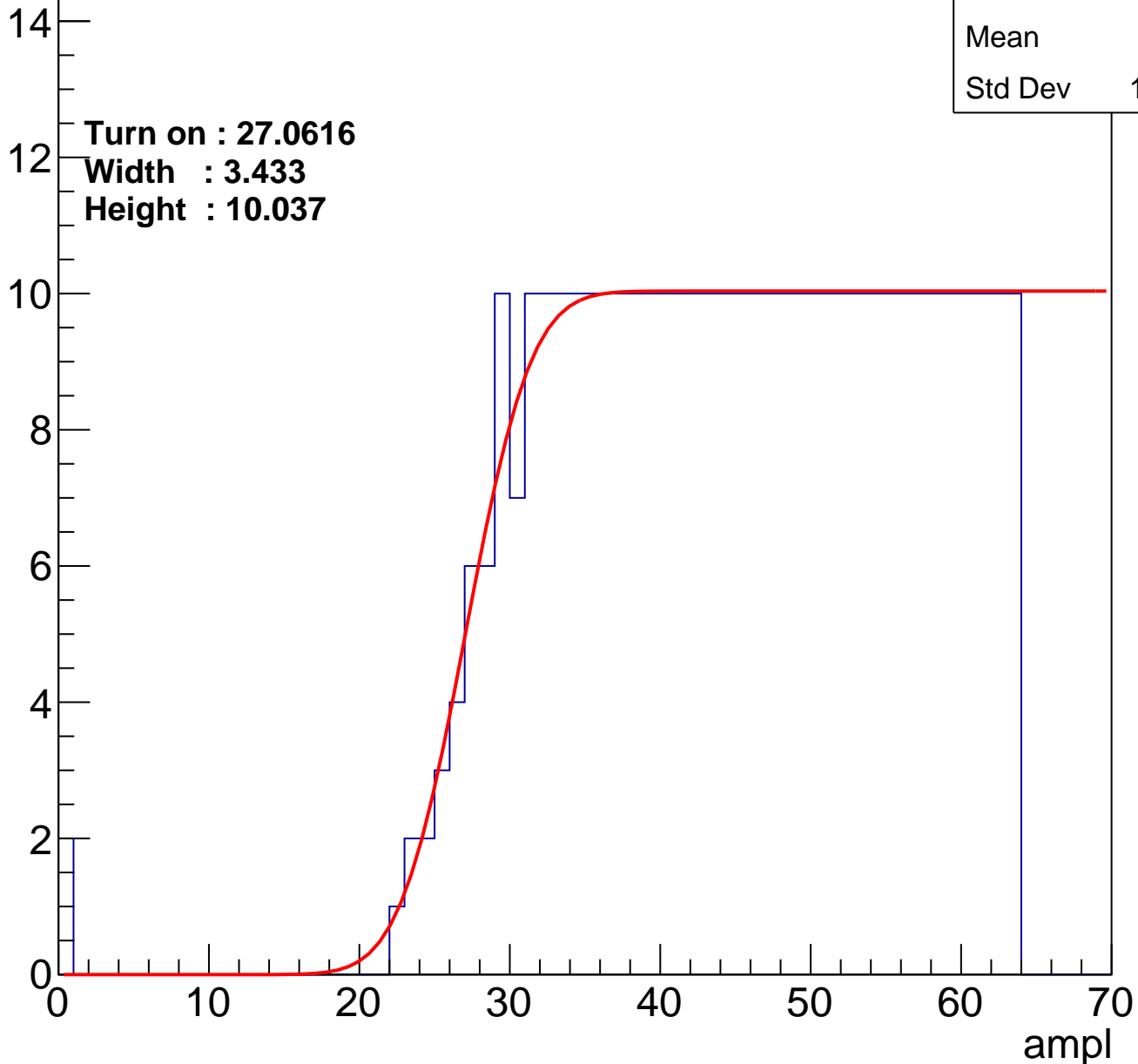
Entries	373
Mean	44.6
Std Dev	11.35

Turn on : 27.0616

Width : 3.433

Height : 10.037

Entry



# B0L001S, U20-ch81

calib\_packv5\_042523\_0143.root, FC#9, port A1

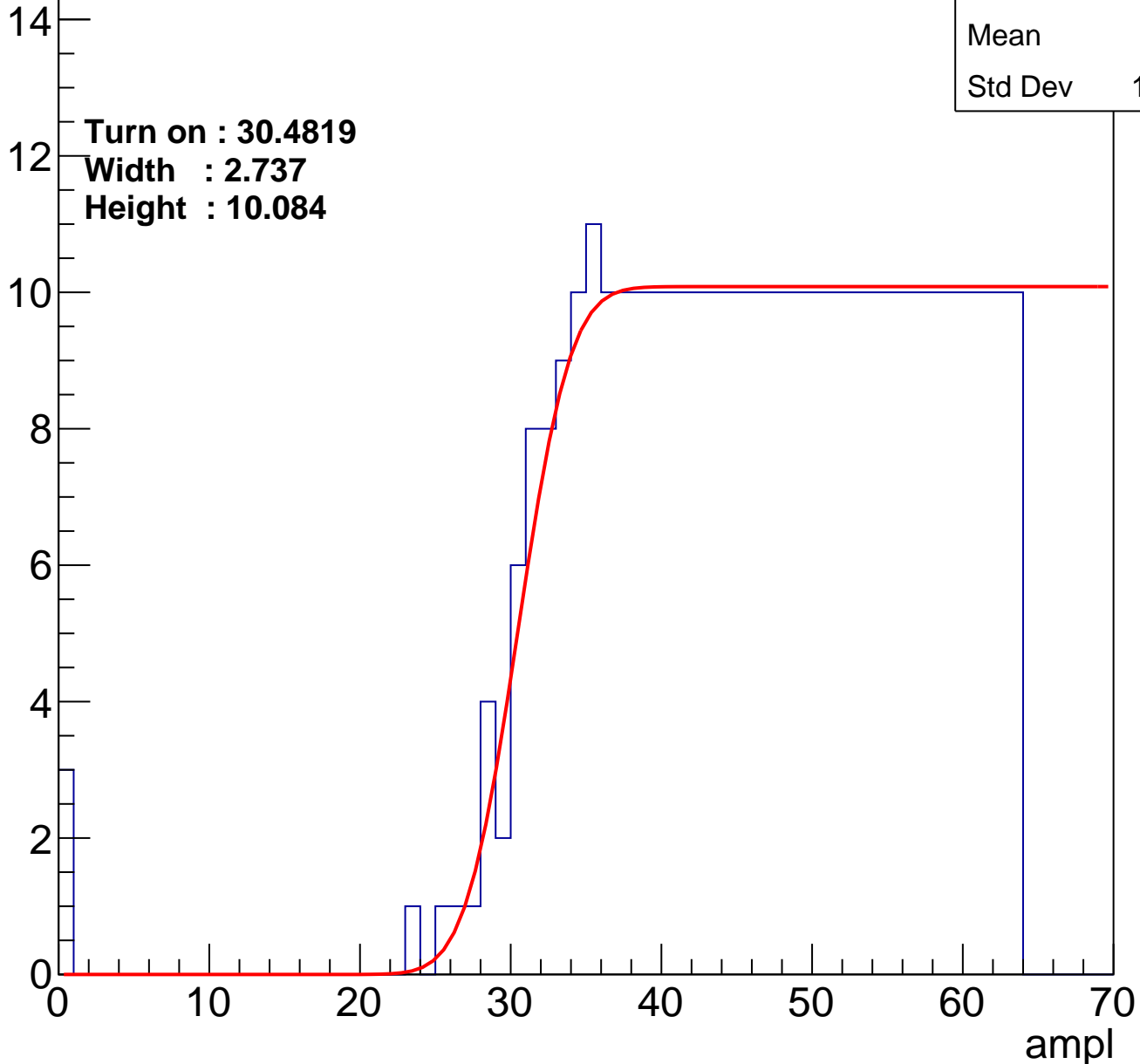
Entries	345
Mean	45.9
Std Dev	10.88

Turn on : 30.4819

Width : 2.737

Height : 10.084

Entry



# B0L001S, U20-ch82

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	351
Mean	45.65
Std Dev	10.86

Turn on : 29.7316

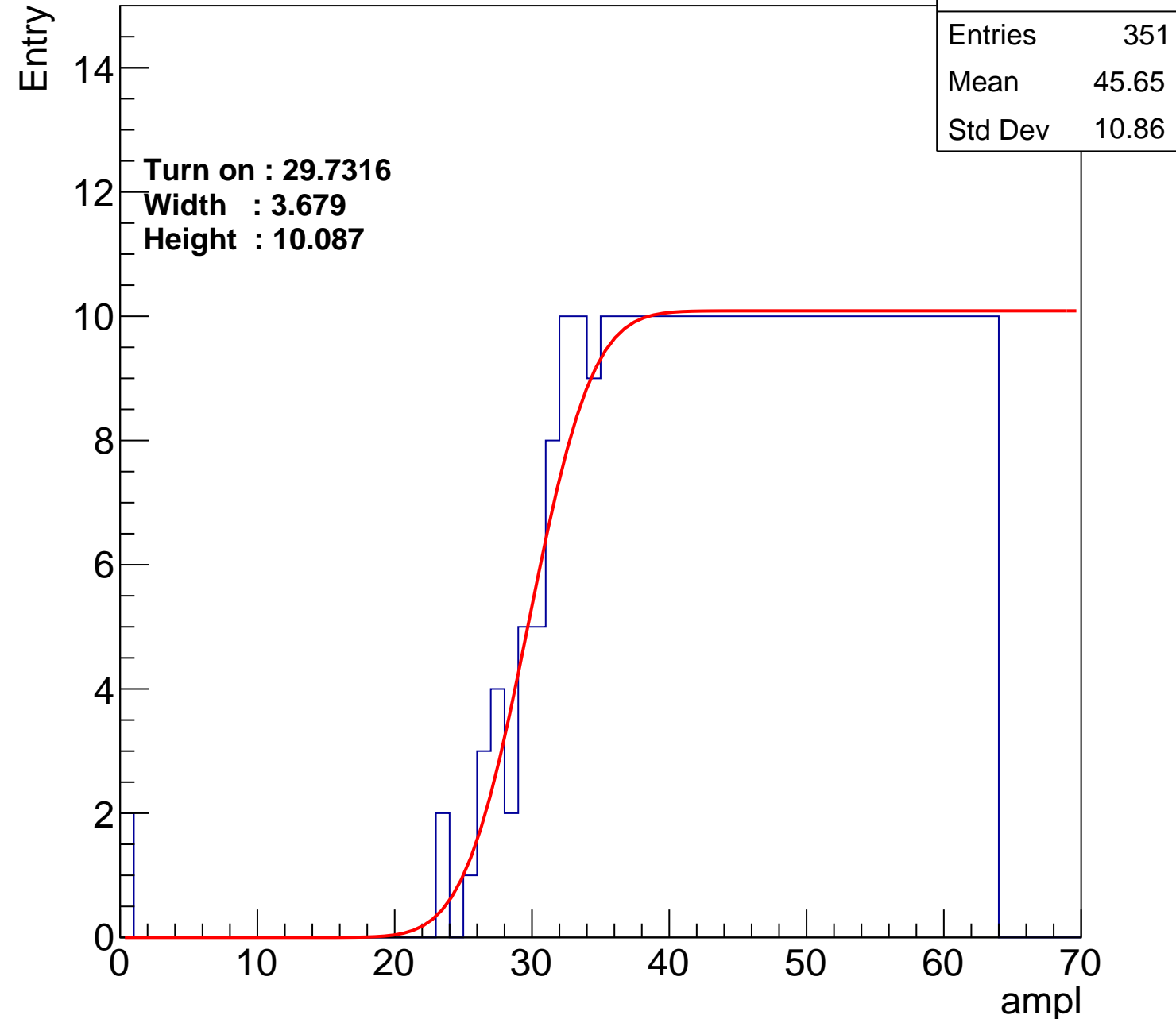
Width : 3.679

Height : 10.087

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch83

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	358
Mean	45.35
Std Dev	10.85

**Turn on : 28.5925**

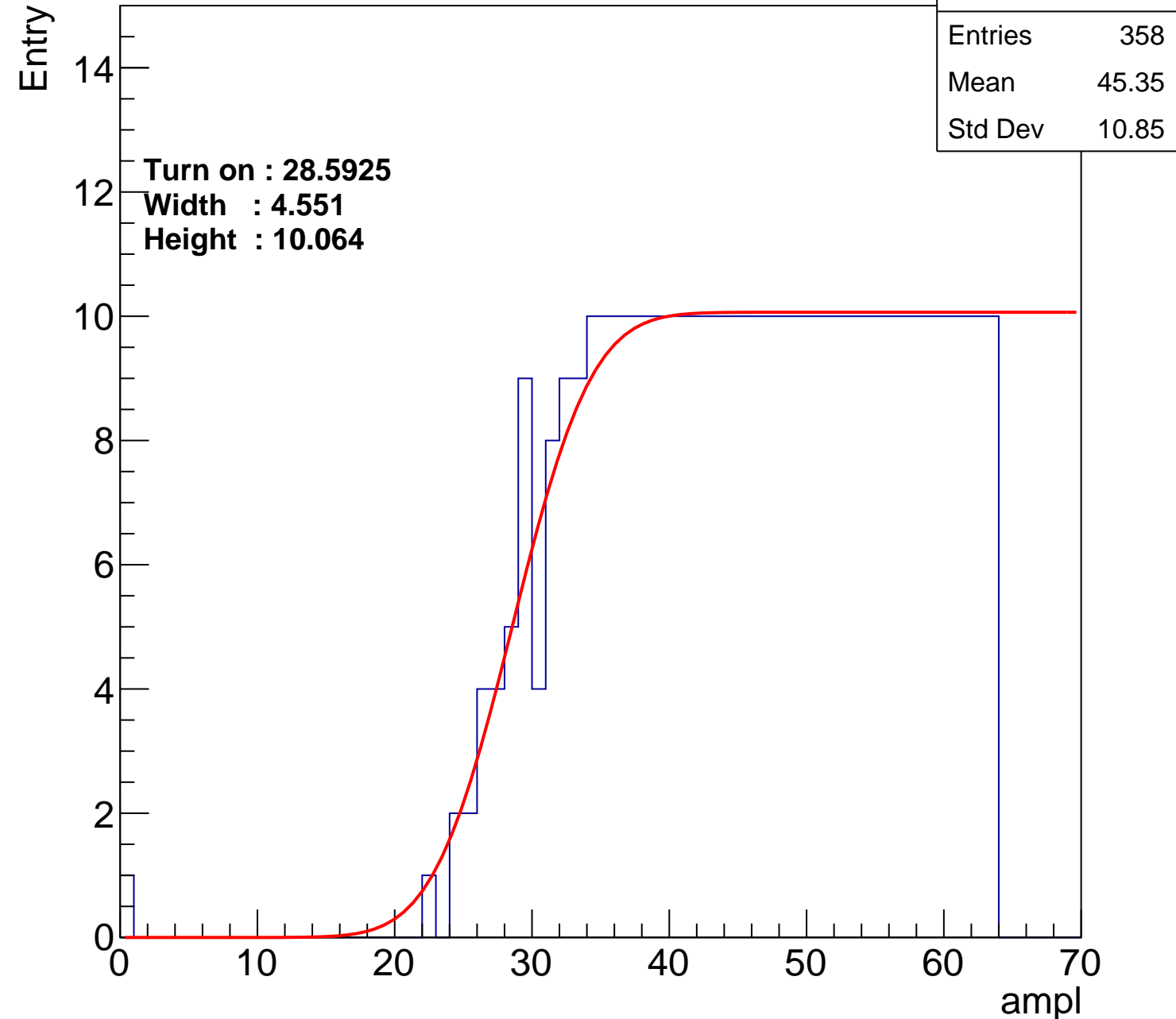
**Width : 4.551**

**Height : 10.064**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch84

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	356
Mean	45.24
Std Dev	11.52

**Turn on : 29.4543**

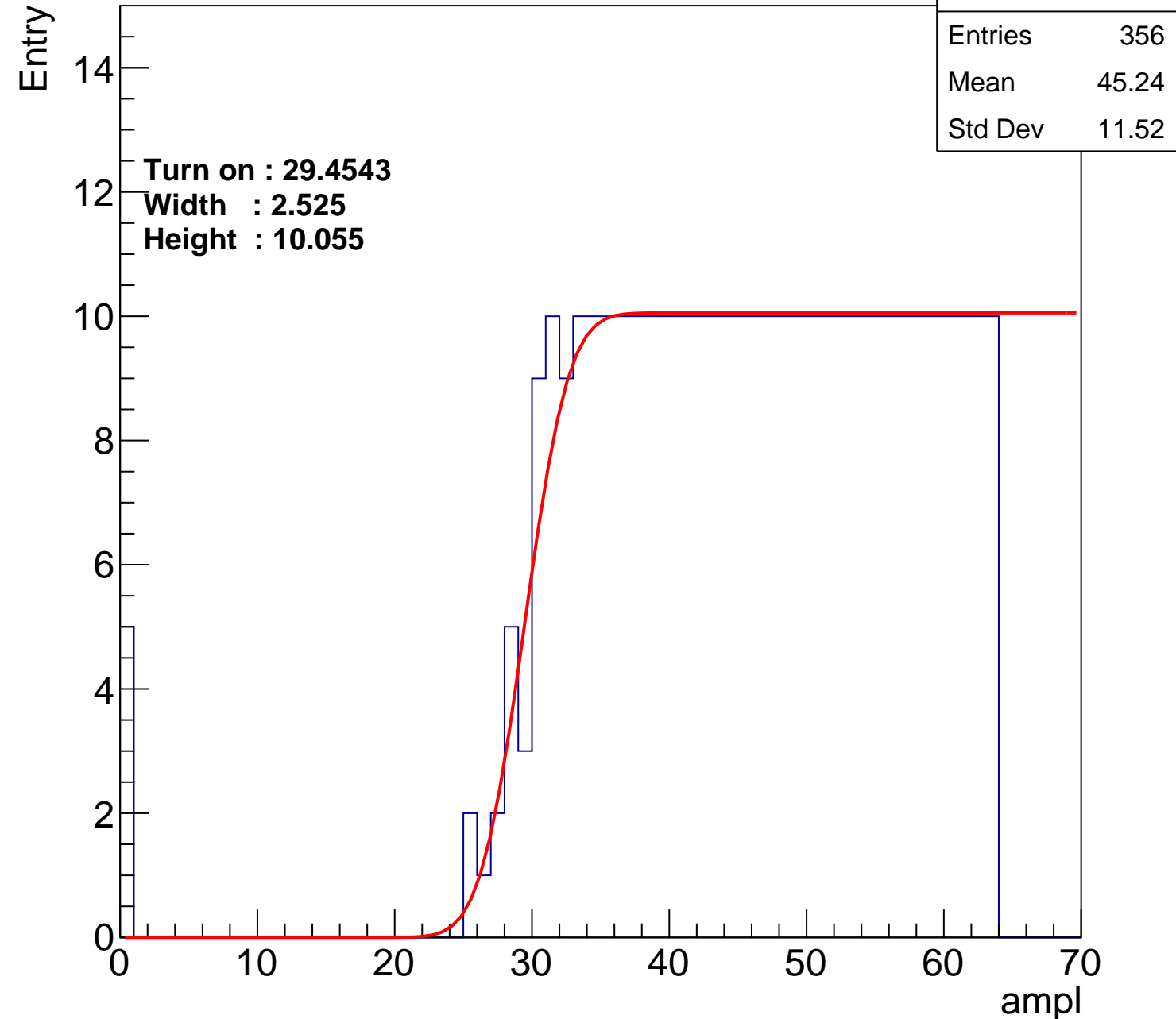
**Width : 2.525**

**Height : 10.055**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch85

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	355
Mean	45.32
Std Dev	11.36

Turn on : 27.6741

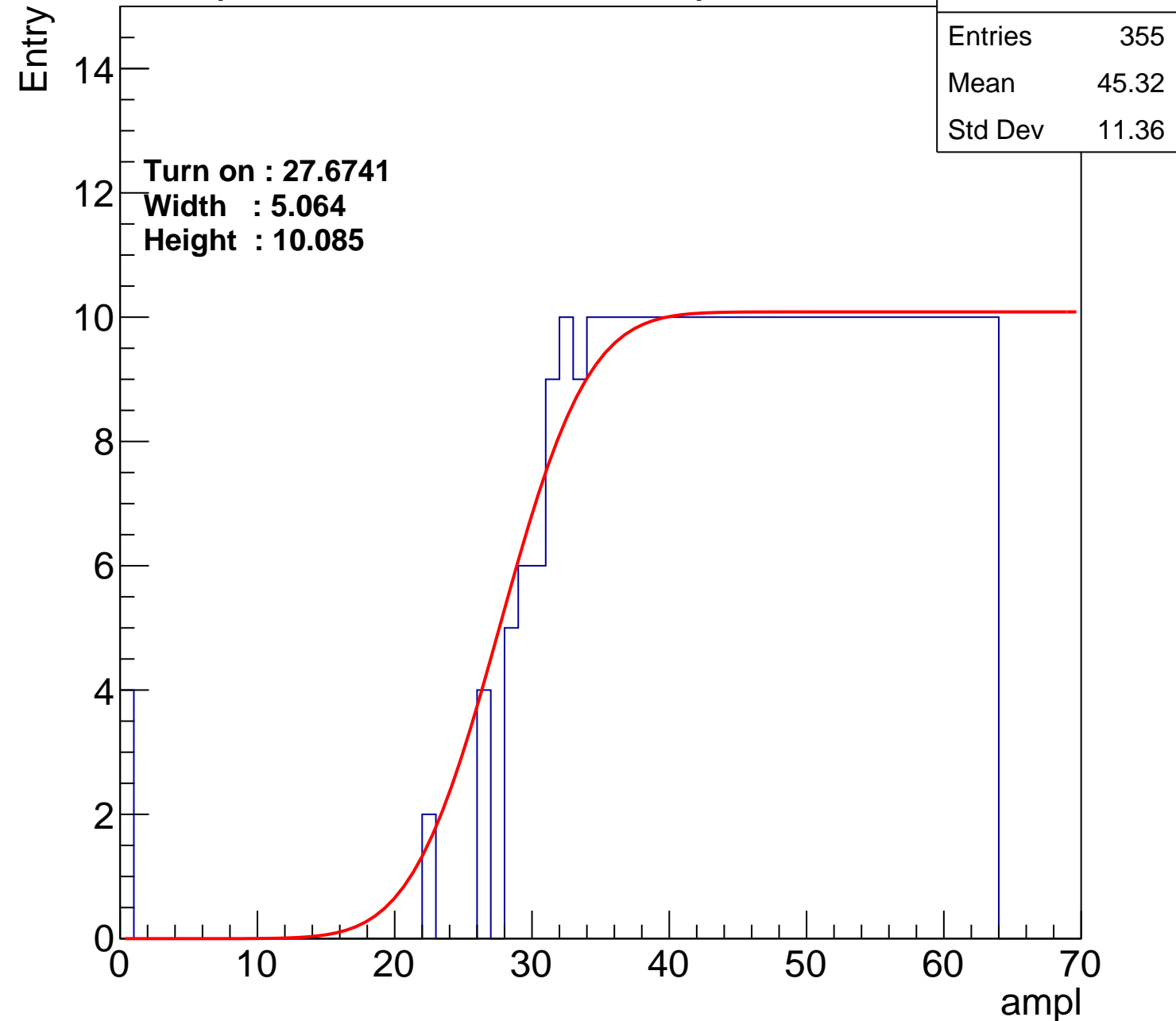
Width : 5.064

Height : 10.085

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch86

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	328
Mean	46.85
Std Dev	10.18

Turn on : 31.1427

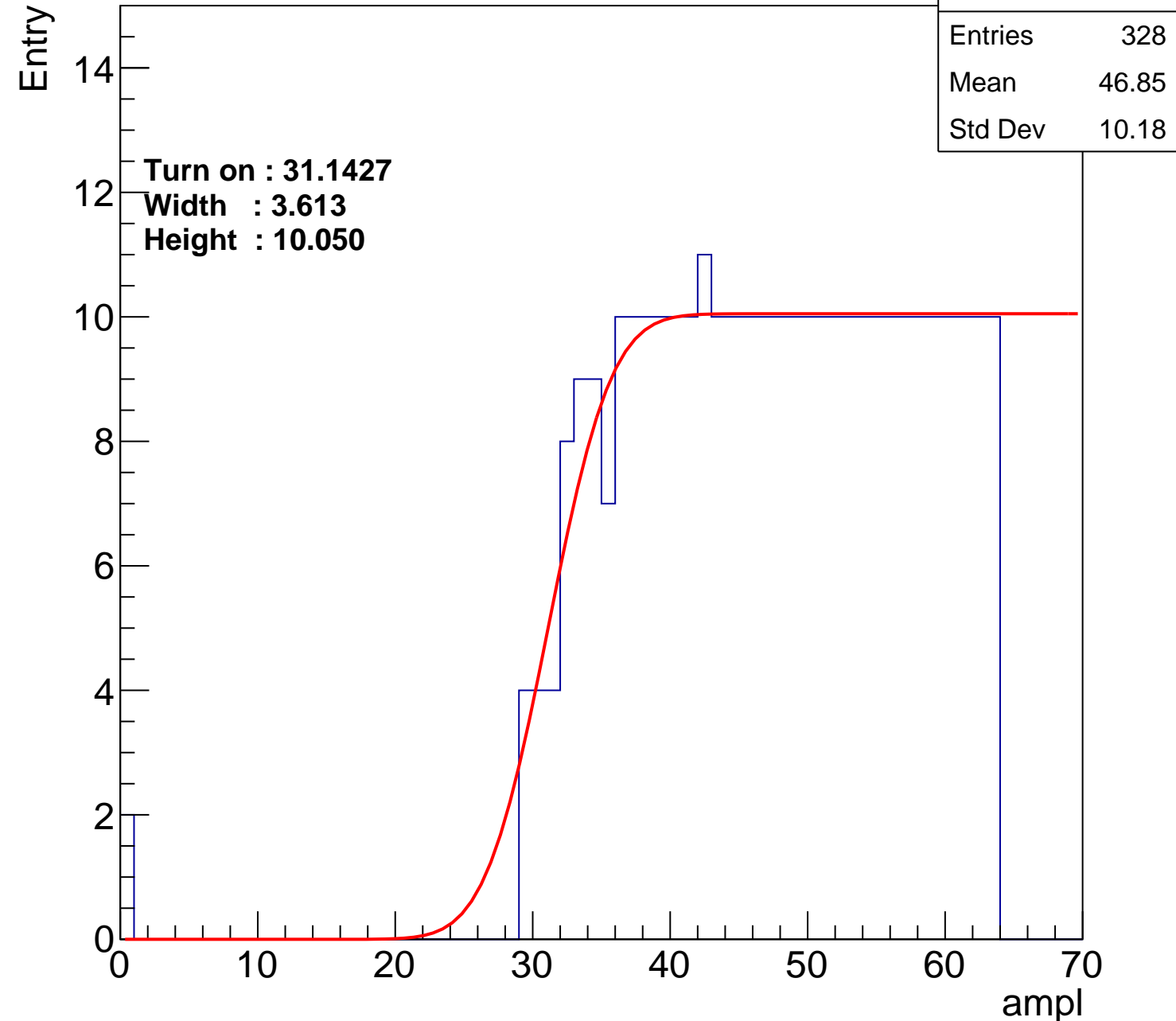
Width : 3.613

Height : 10.050

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





**calib\_packv5\_042523\_0143.root, FC#9, port A1**

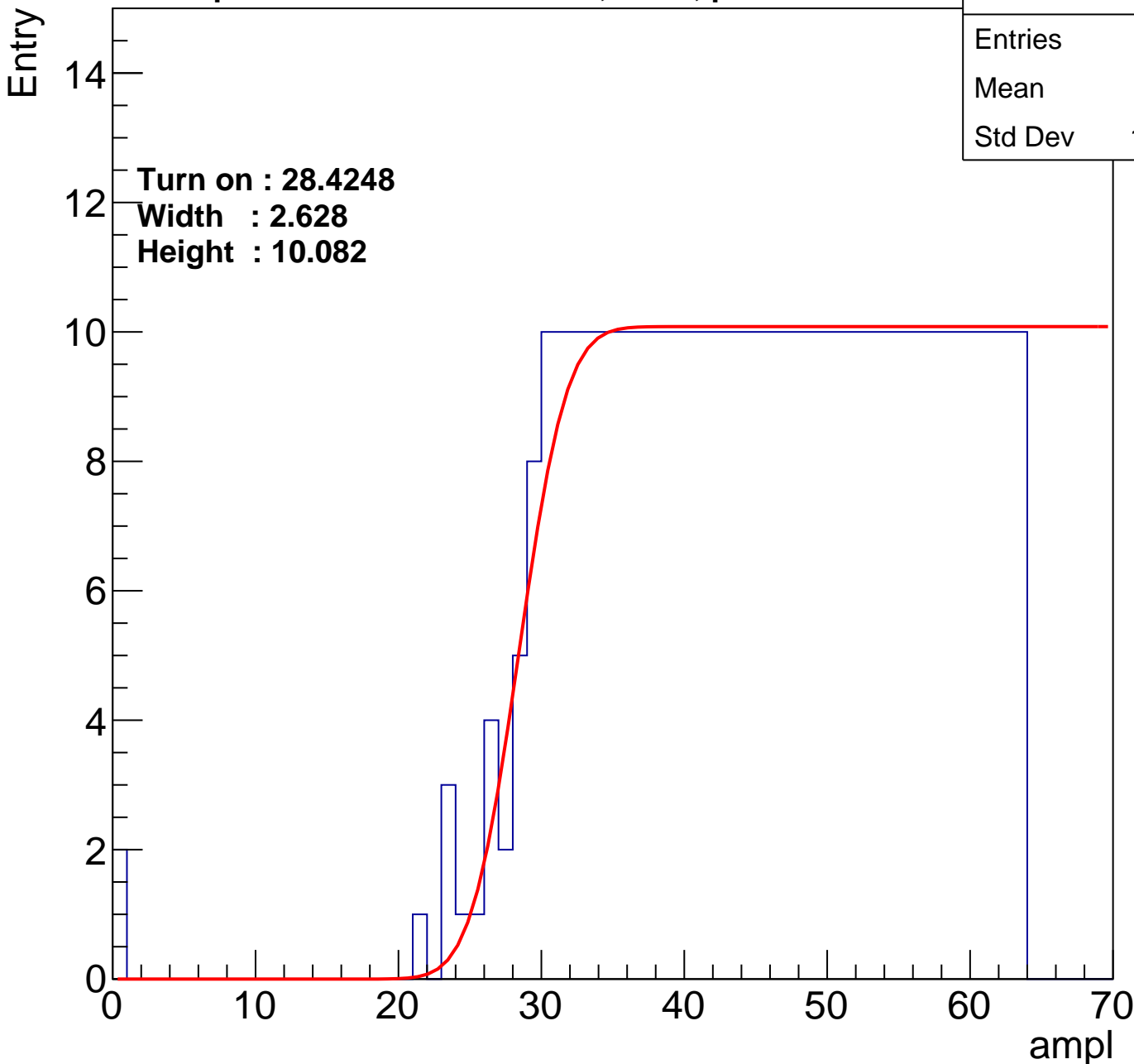
Entries	367
Mean	44.9
Std Dev	11.19

Mean	44.9
------	------

Std Dev	11.19
---------	-------

**Width : 2.628**

**Height : 10.082**



# B0L001S, U20-ch88

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	370
Mean	44.61
Std Dev	11.67

Turn on : 27.5936

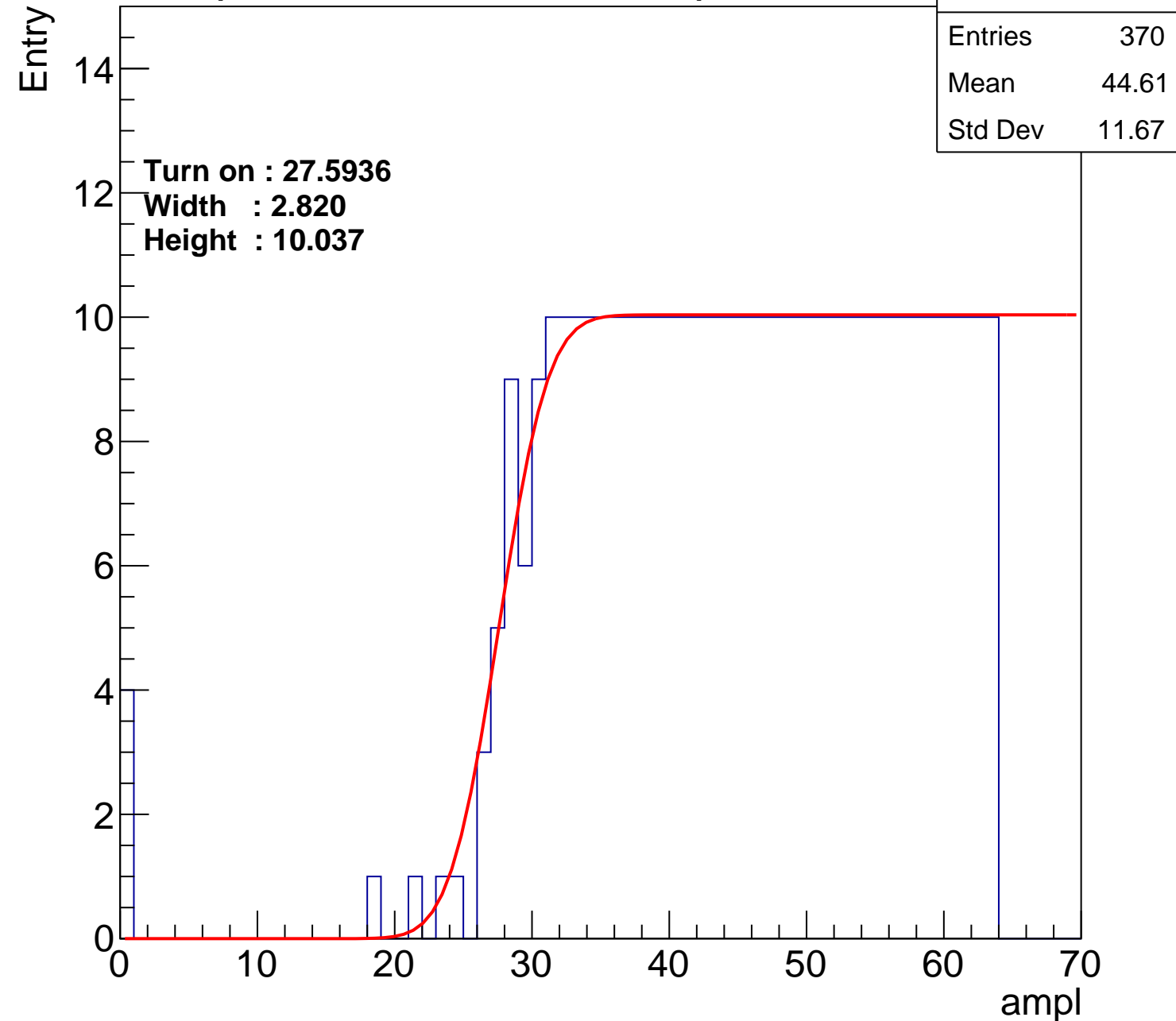
Width : 2.820

Height : 10.037

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch89

calib\_packv5\_042523\_0143.root, FC#9, port A1

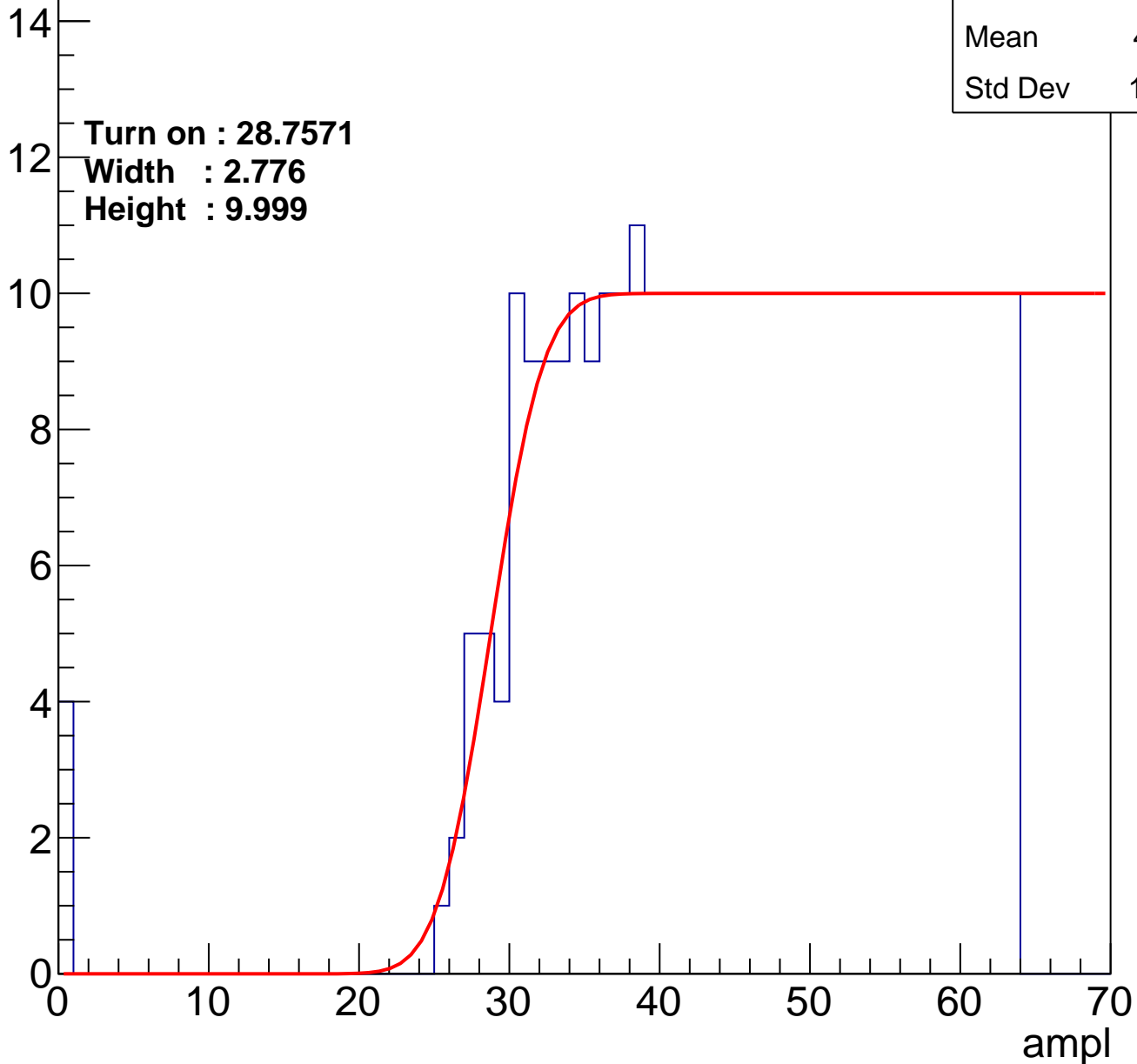
Entries	358
Mean	45.21
Std Dev	11.36

Turn on : 28.7571

Width : 2.776

Height : 9.999

Entry



# B0L001S, U20-ch90

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	380
Mean	43.99
Std Dev	12.23

Turn on : 26.9551

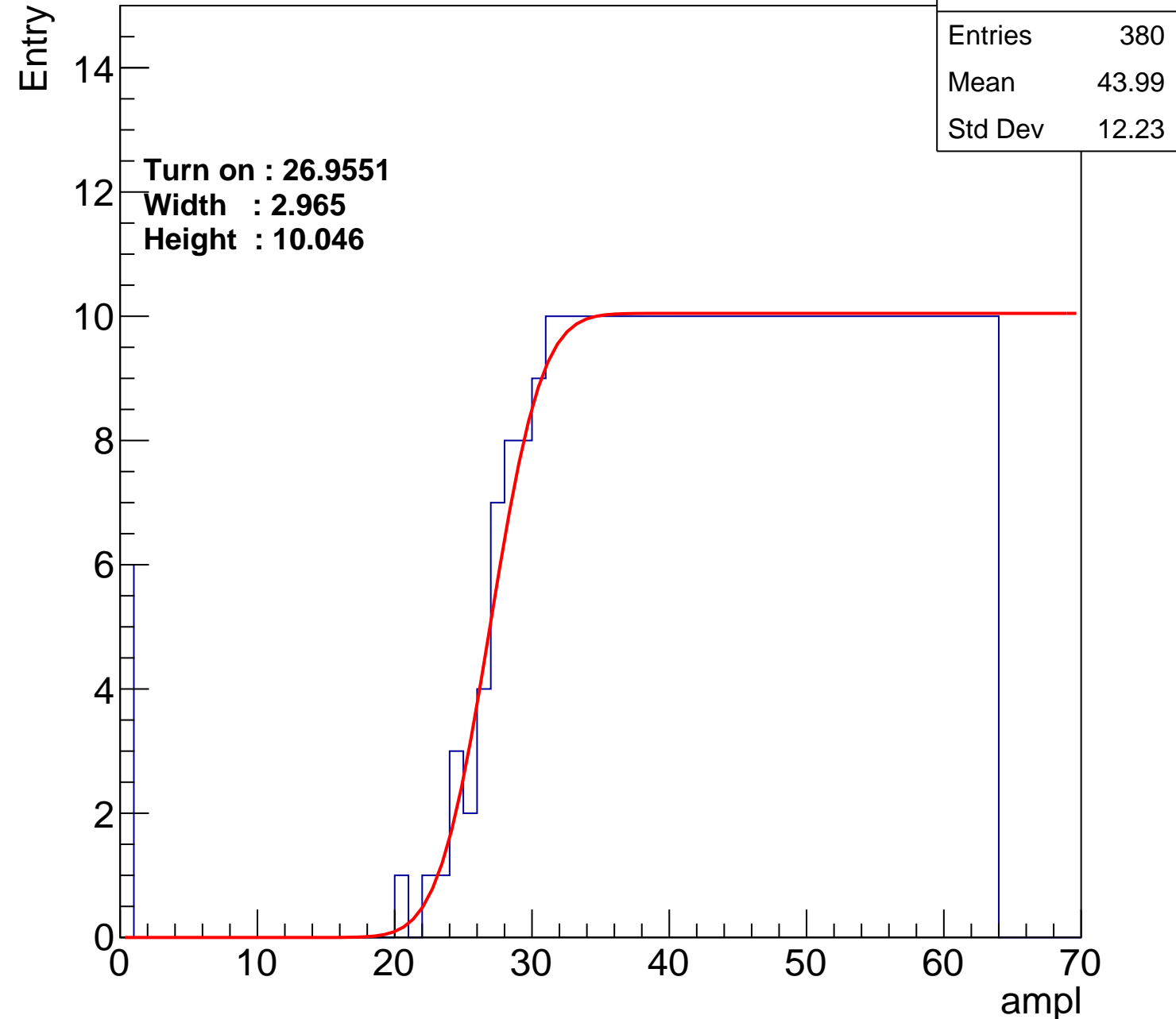
Width : 2.965

Height : 10.046

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch91

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	367
Mean	44.99
Std Dev	10.95

Turn on : 27.6092

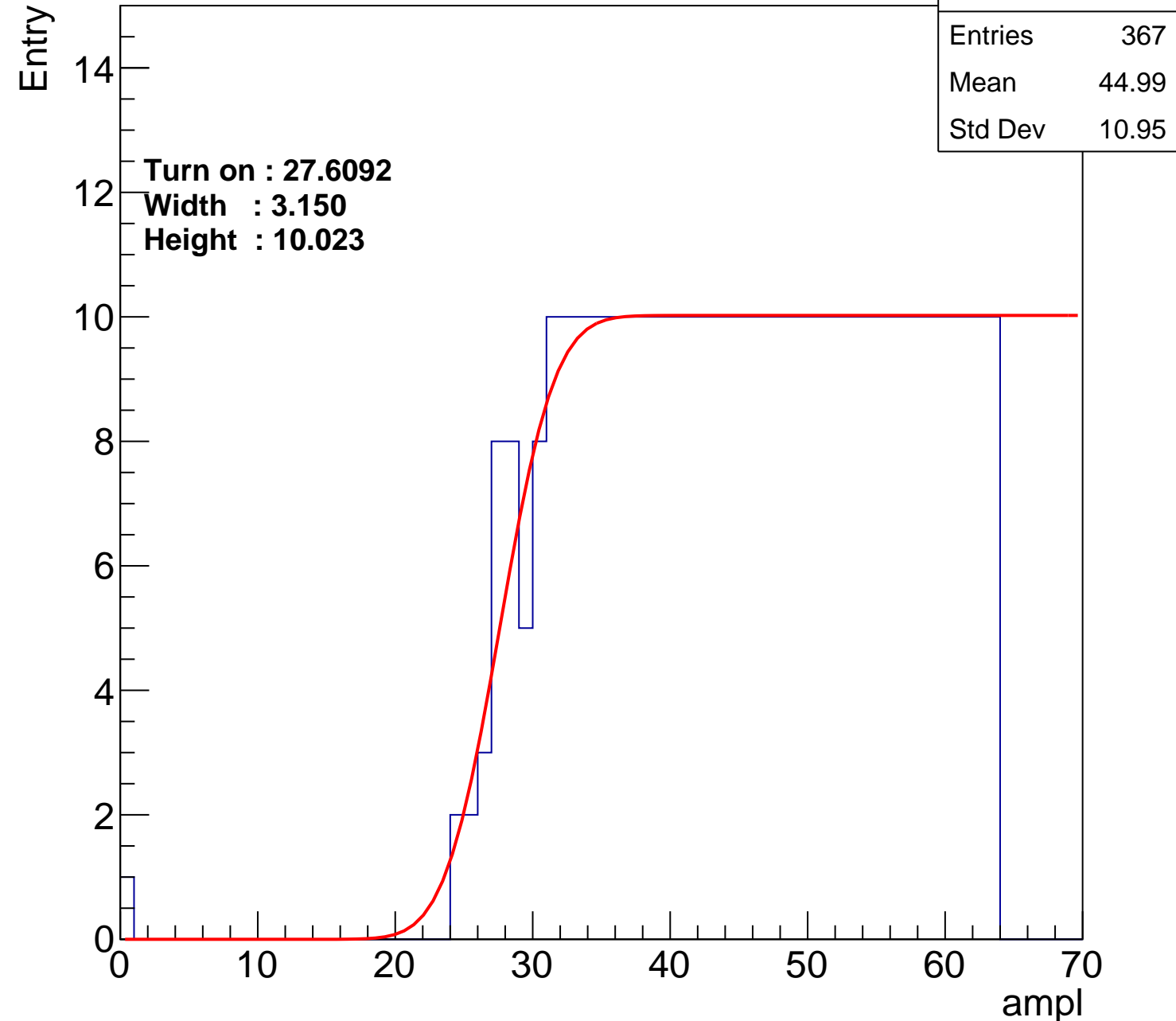
Width : 3.150

Height : 10.023

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch92

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	352
Mean	45.39
Std Dev	11.54

Turn on : 30.3092

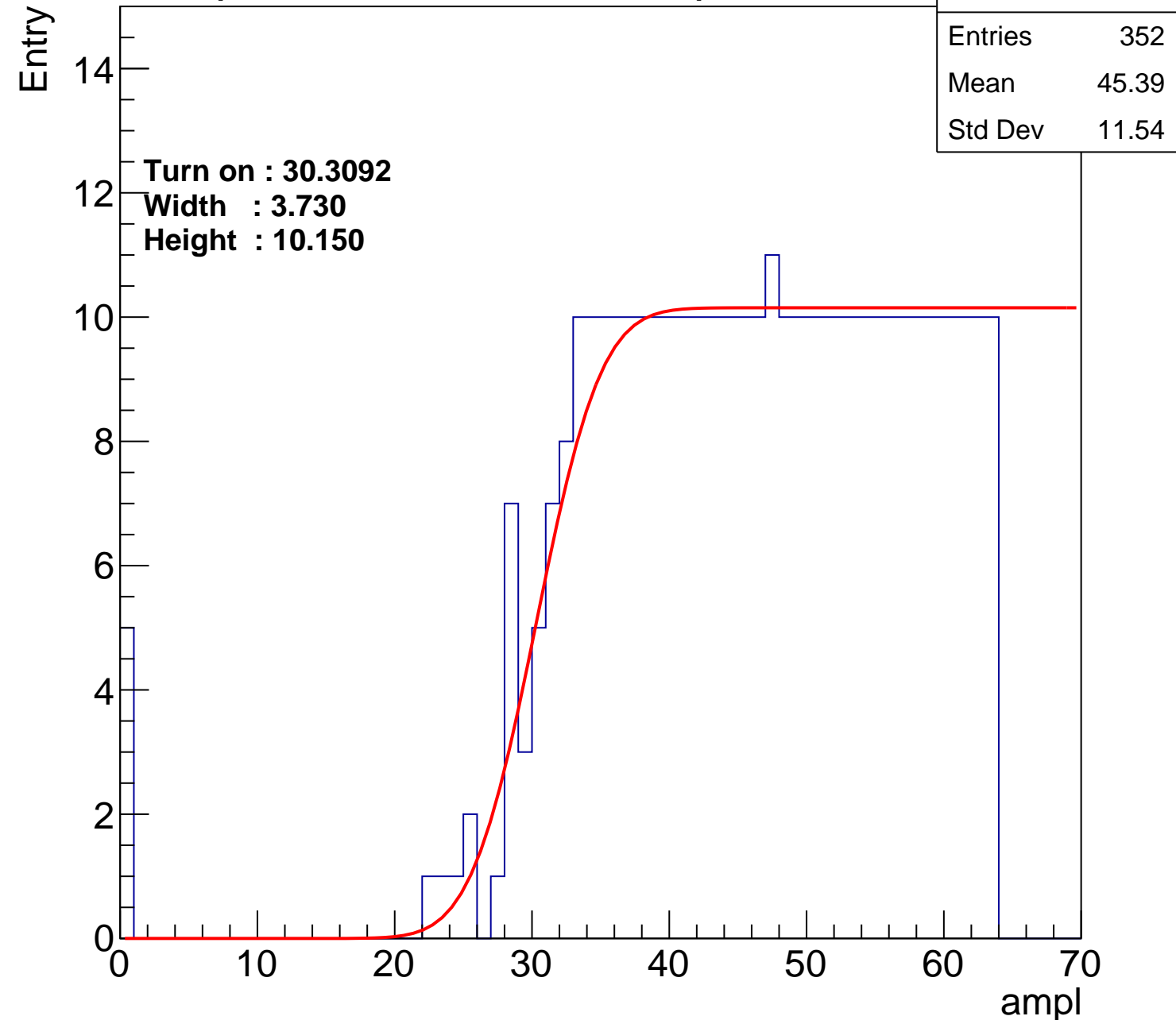
Width : 3.730

Height : 10.150

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch93

calib\_packv5\_042523\_0143.root, FC#9, port A1

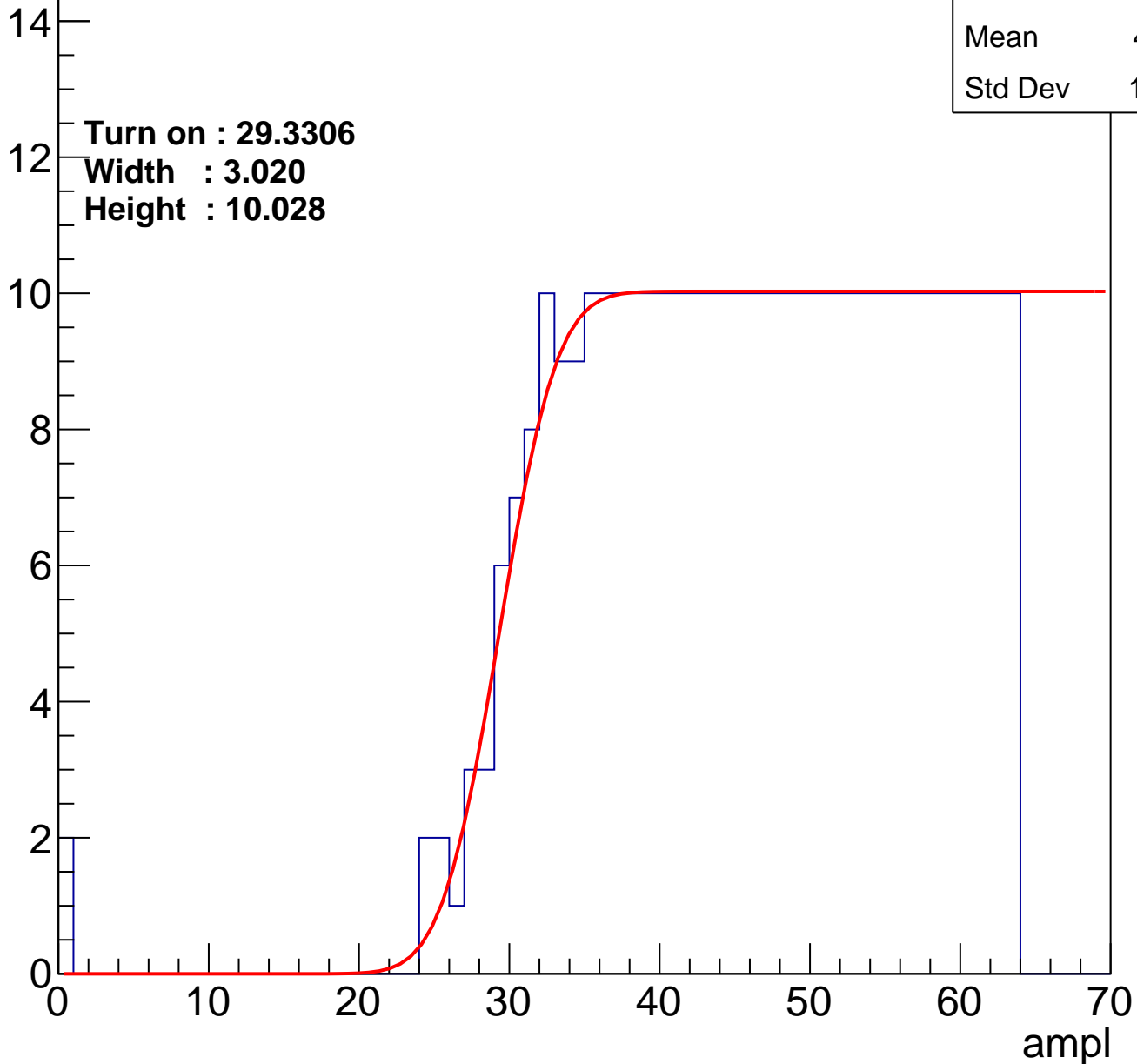
Entries	352
Mean	45.61
Std Dev	10.86

**Turn on : 29.3306**

**Width : 3.020**

**Height : 10.028**

Entry



# B0L001S, U20-ch94

calib\_packv5\_042523\_0143.root, FC#9, port A1

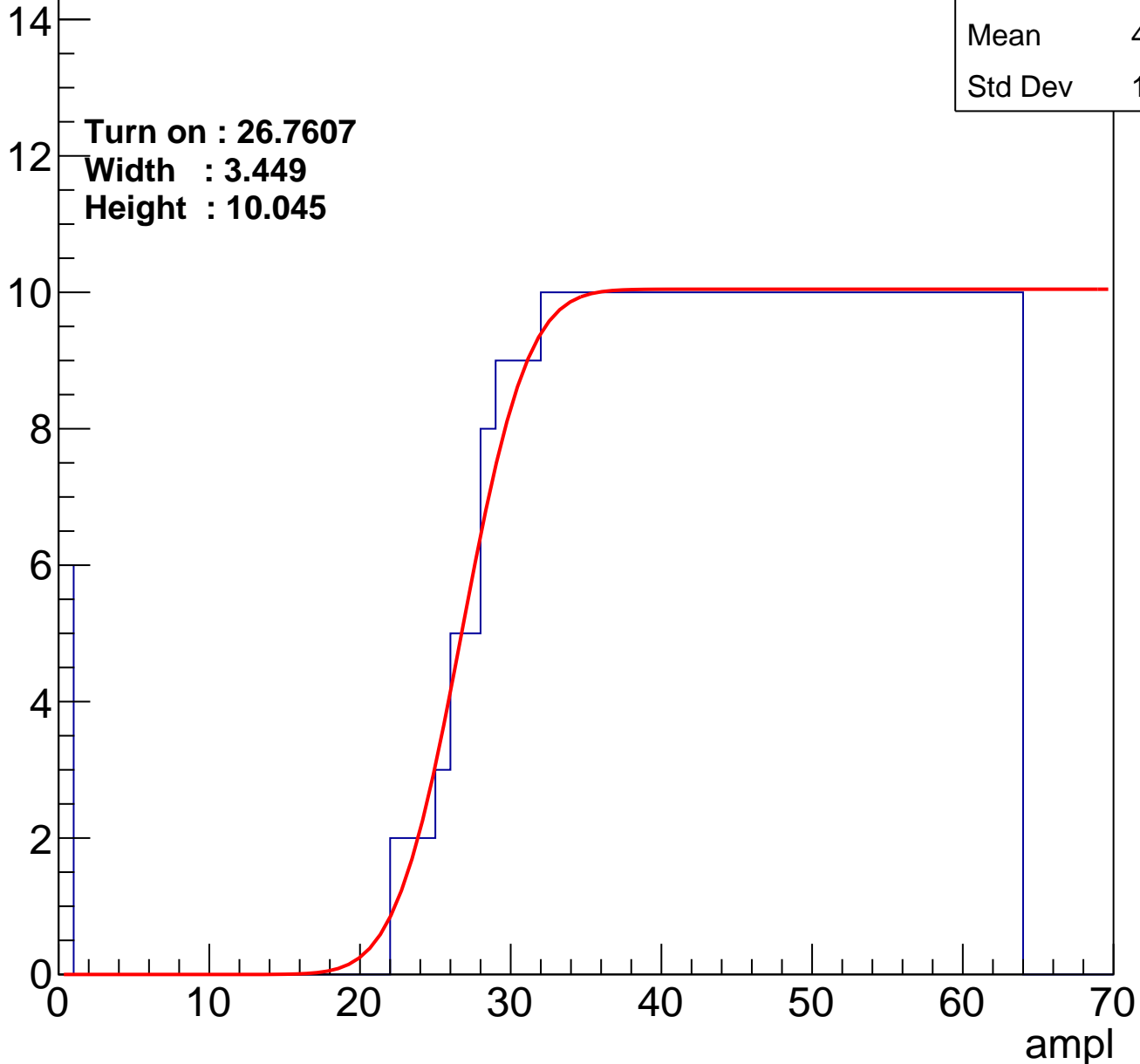
Entries	380
Mean	43.98
Std Dev	12.24

**Turn on : 26.7607**

**Width : 3.449**

**Height : 10.045**

Entry





# B0L001S, U20-ch95

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	359
Mean	45.09
Std Dev	11.49

**Turn on : 28.8280**

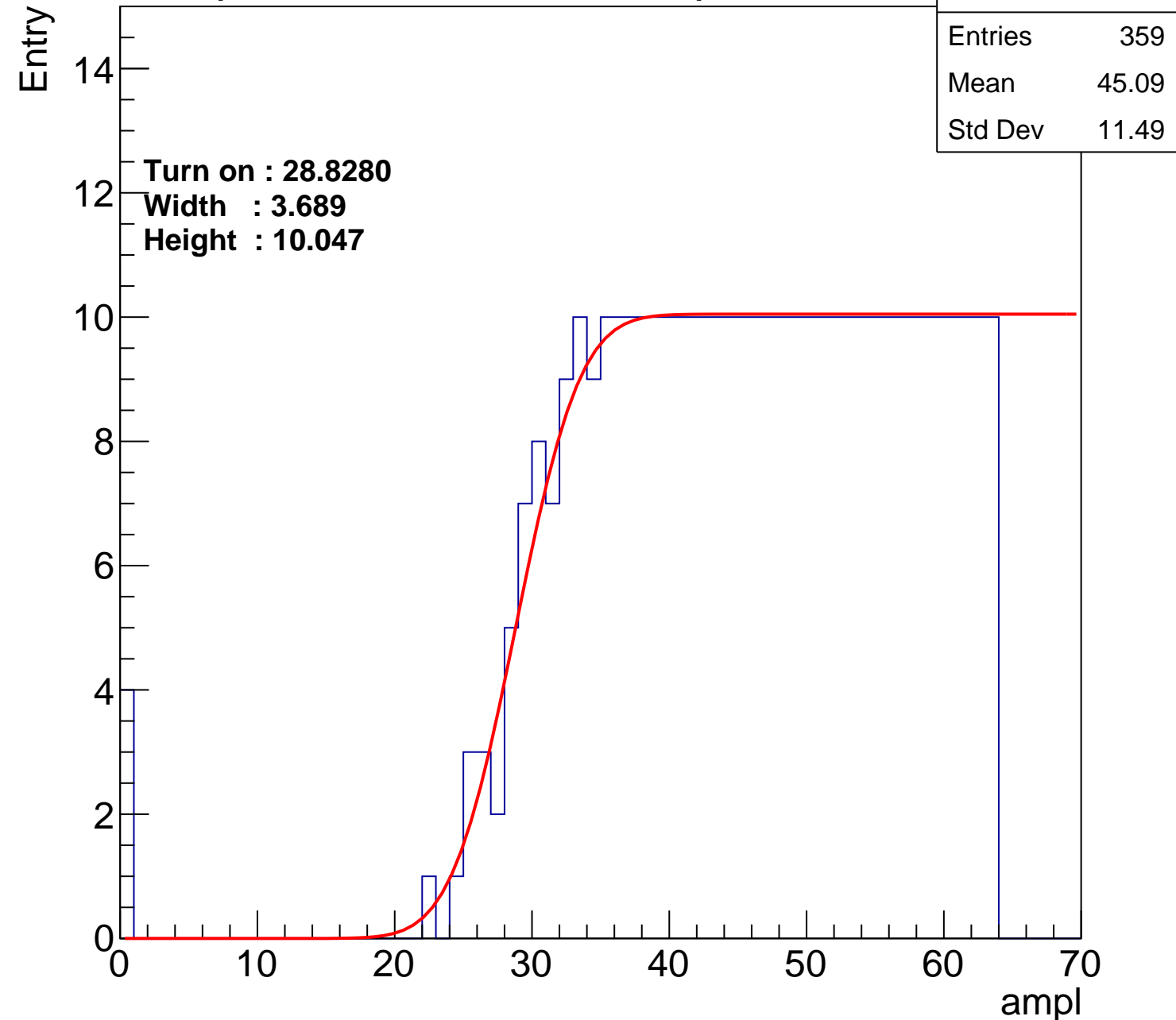
**Width : 3.689**

**Height : 10.047**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch96

calib\_packv5\_042523\_0143.root, FC#9, port A1

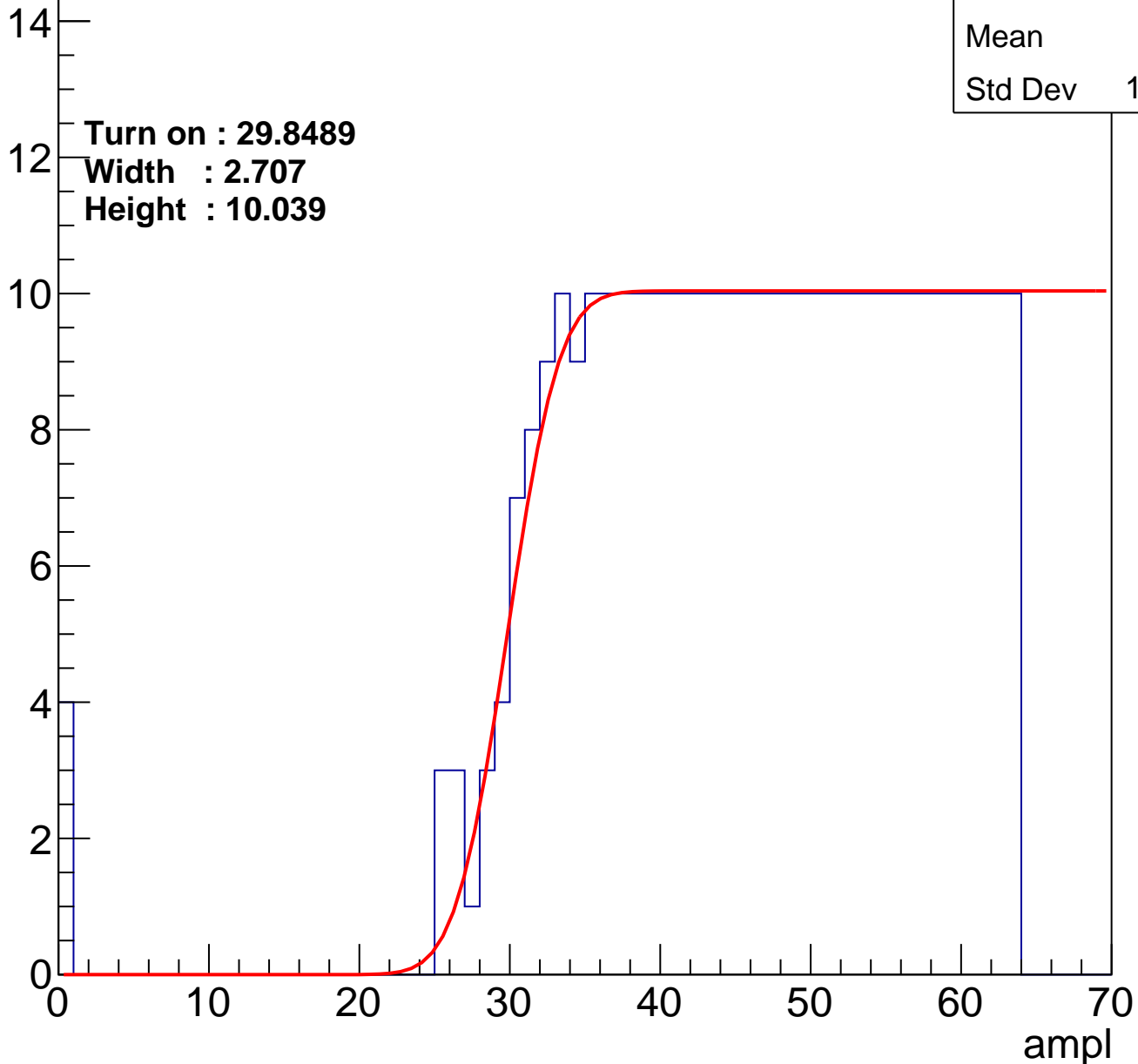
Entries	351
Mean	45.5
Std Dev	11.28

Turn on : 29.8489

Width : 2.707

Height : 10.039

Entry



# B0L001S, U20-ch97

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	369
Mean	44.87
Std Dev	11.04

Turn on : 27.2422

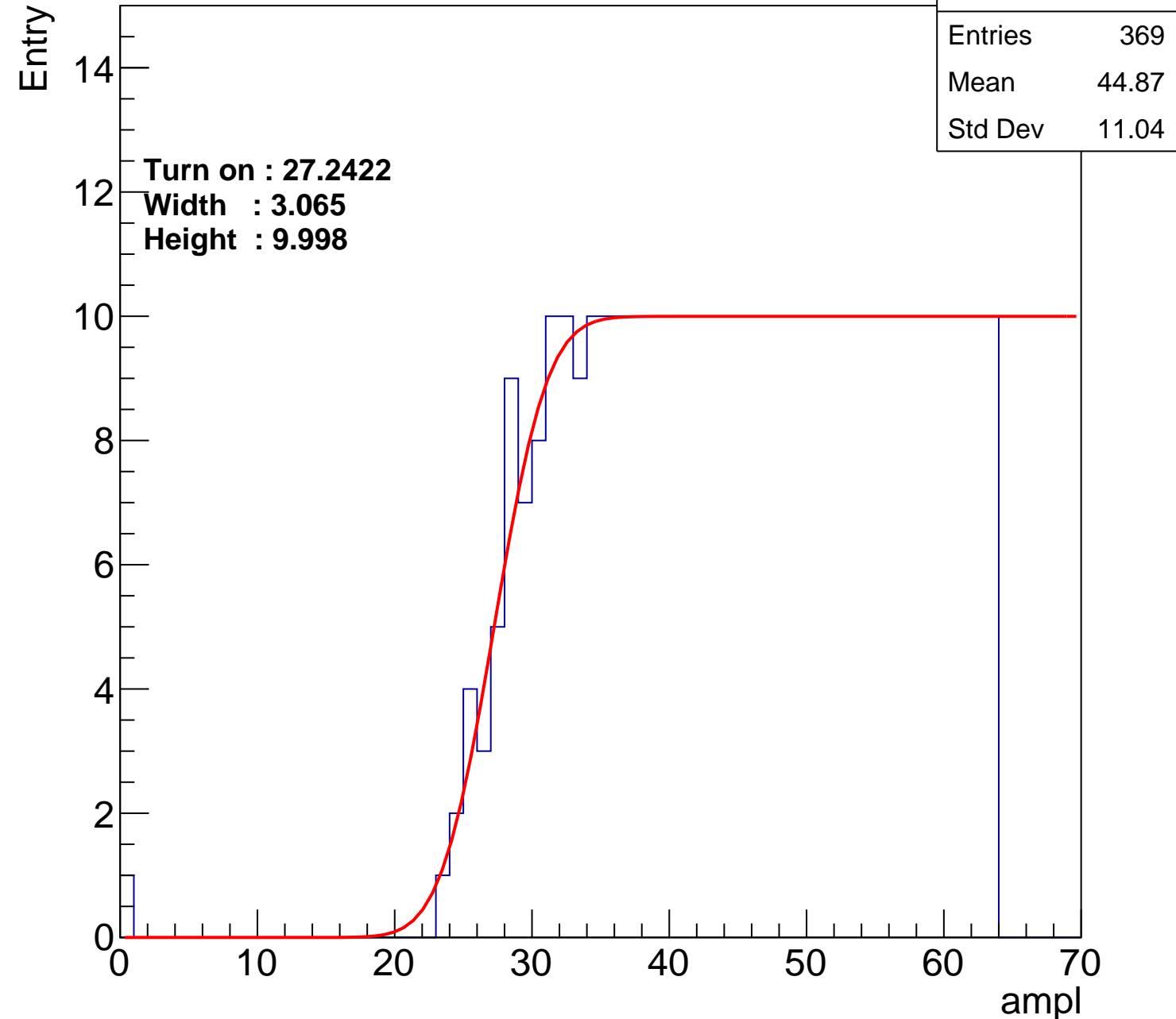
Width : 3.065

Height : 9.998

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch98

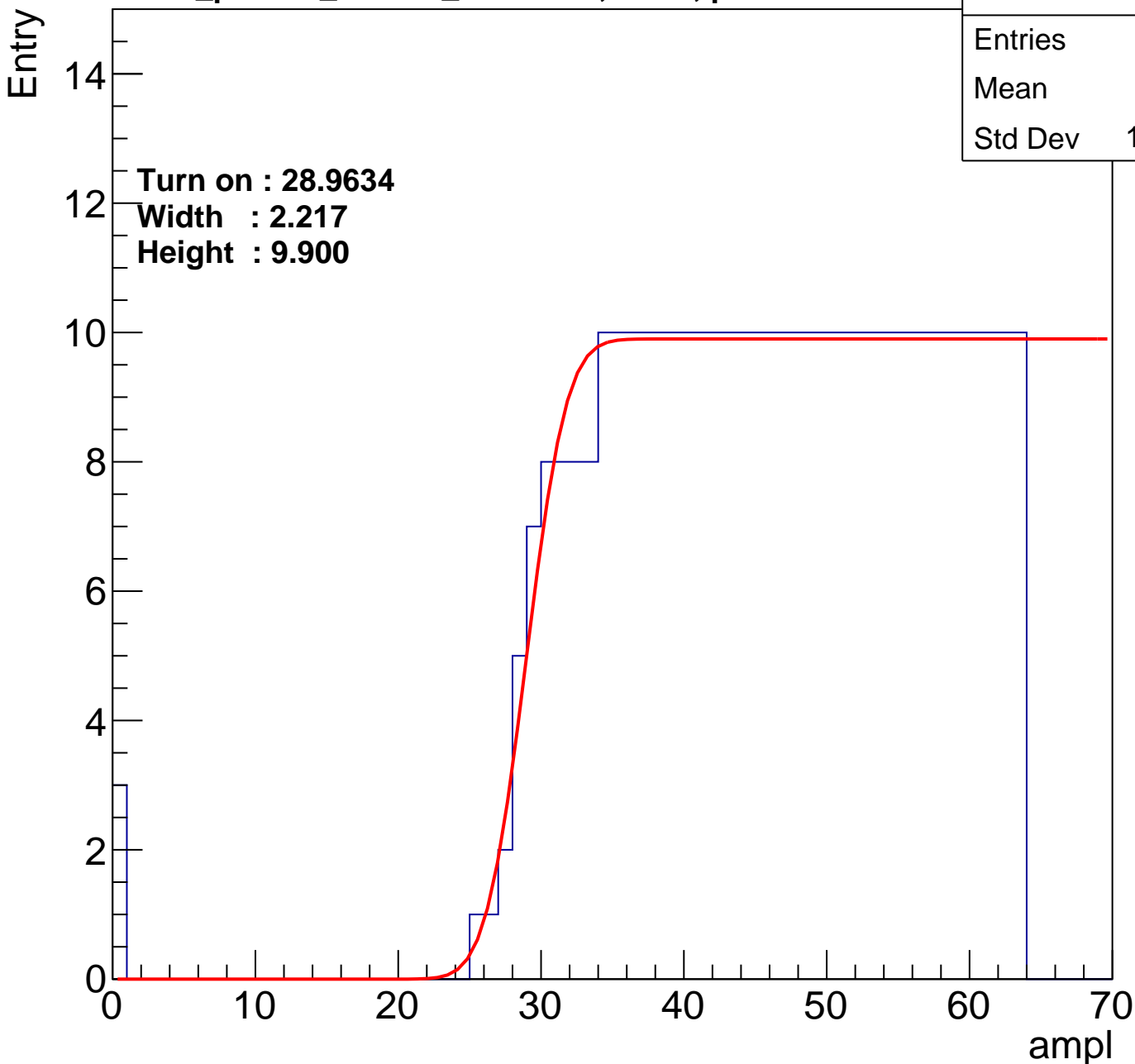
**calib\_packv5\_042523\_0143.root, FC#9, port A1**

Entries	351
Mean	45.6
Std Dev	11.02

**Turn on : 28.9634**

**Width : 2.217**

**Height : 9.900**



# B0L001S, U20-ch99

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	377
Mean	44.38
Std Dev	11.48

Turn on : 26.4402

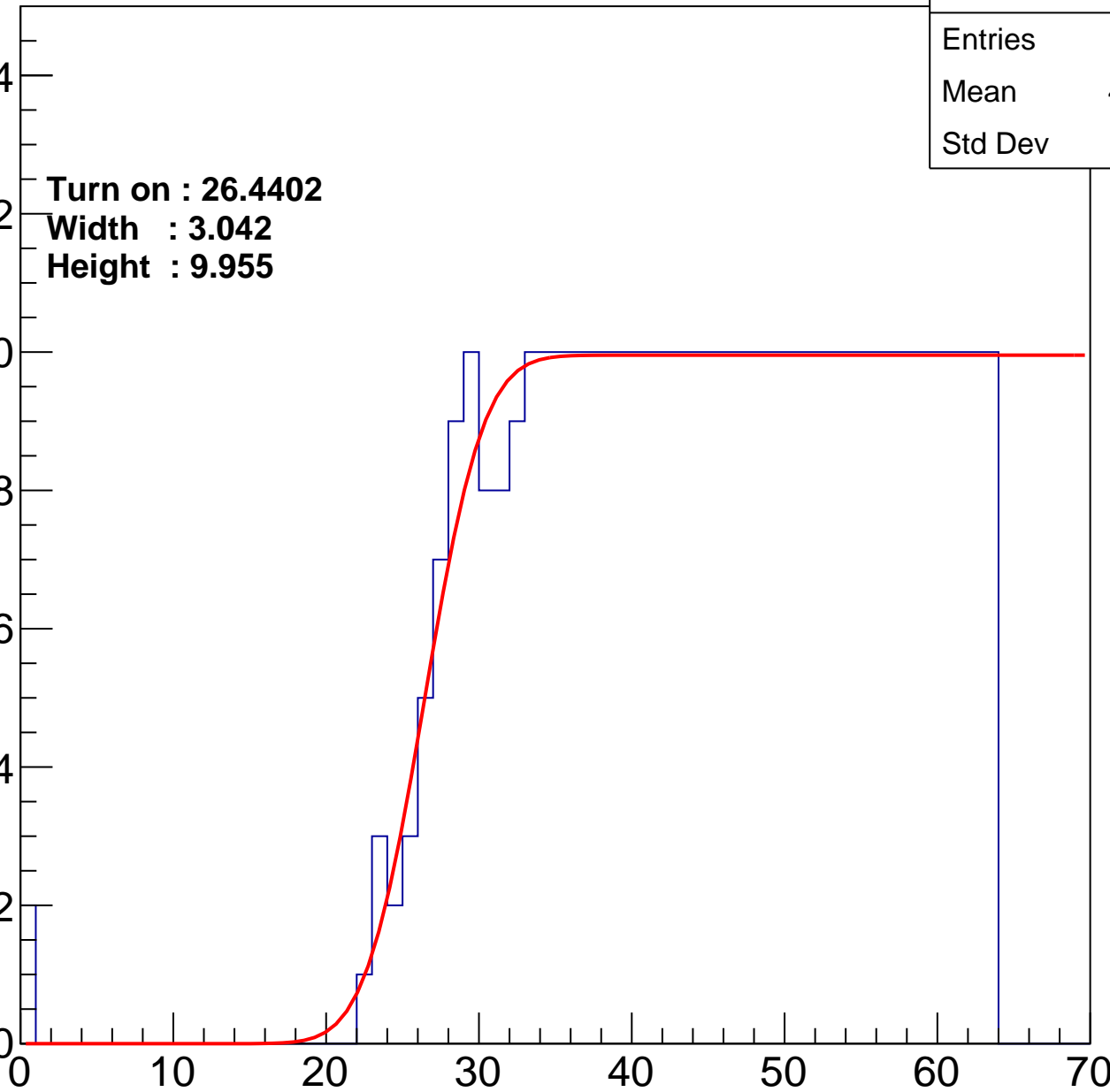
Width : 3.042

Height : 9.955

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch100

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	344
Mean	45.96
Std Dev	10.84

Turn on : 30.3223

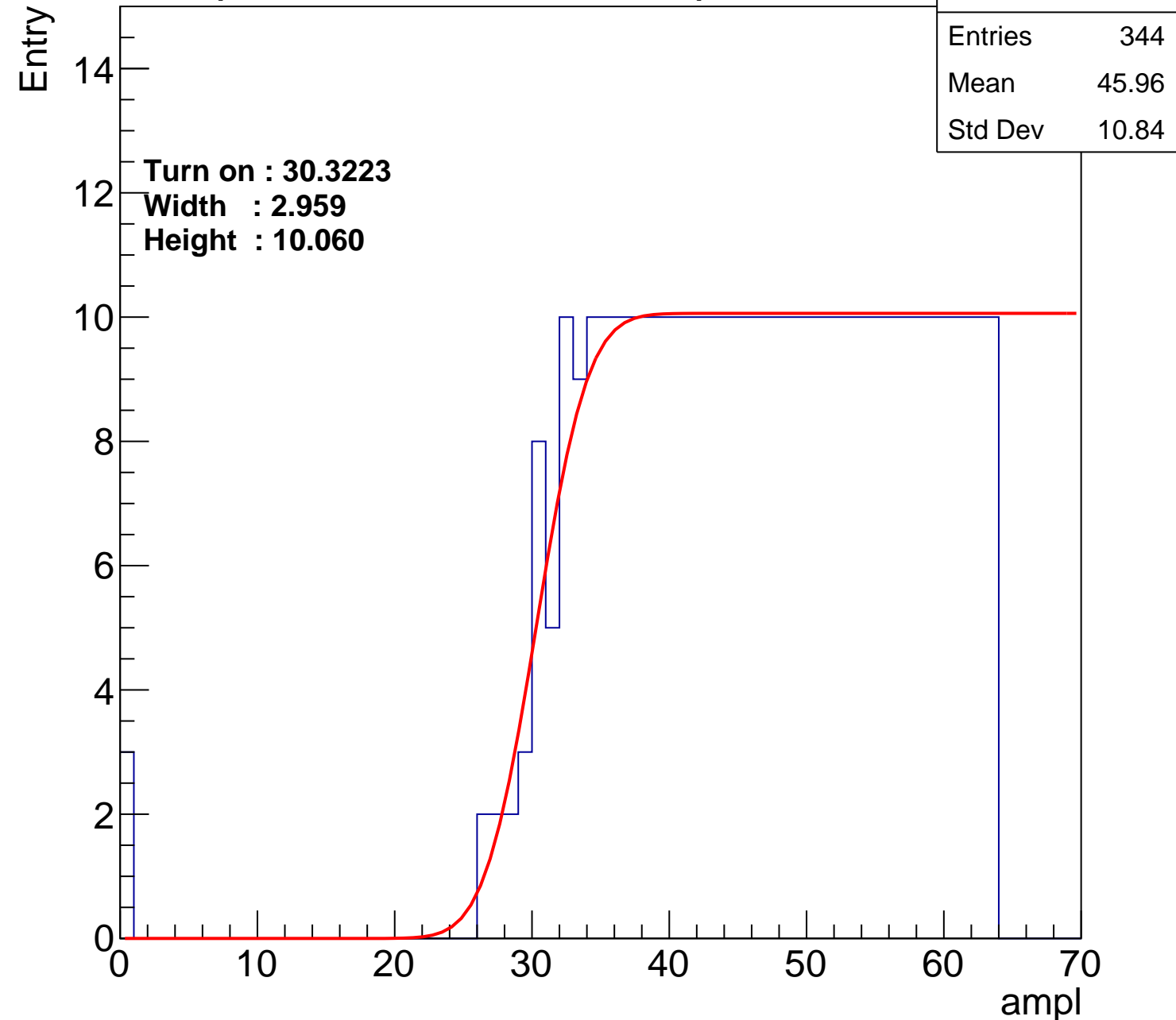
Width : 2.959

Height : 10.060

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch101

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	353
Mean	45.5
Std Dev	11.08

**Turn on : 28.9770**

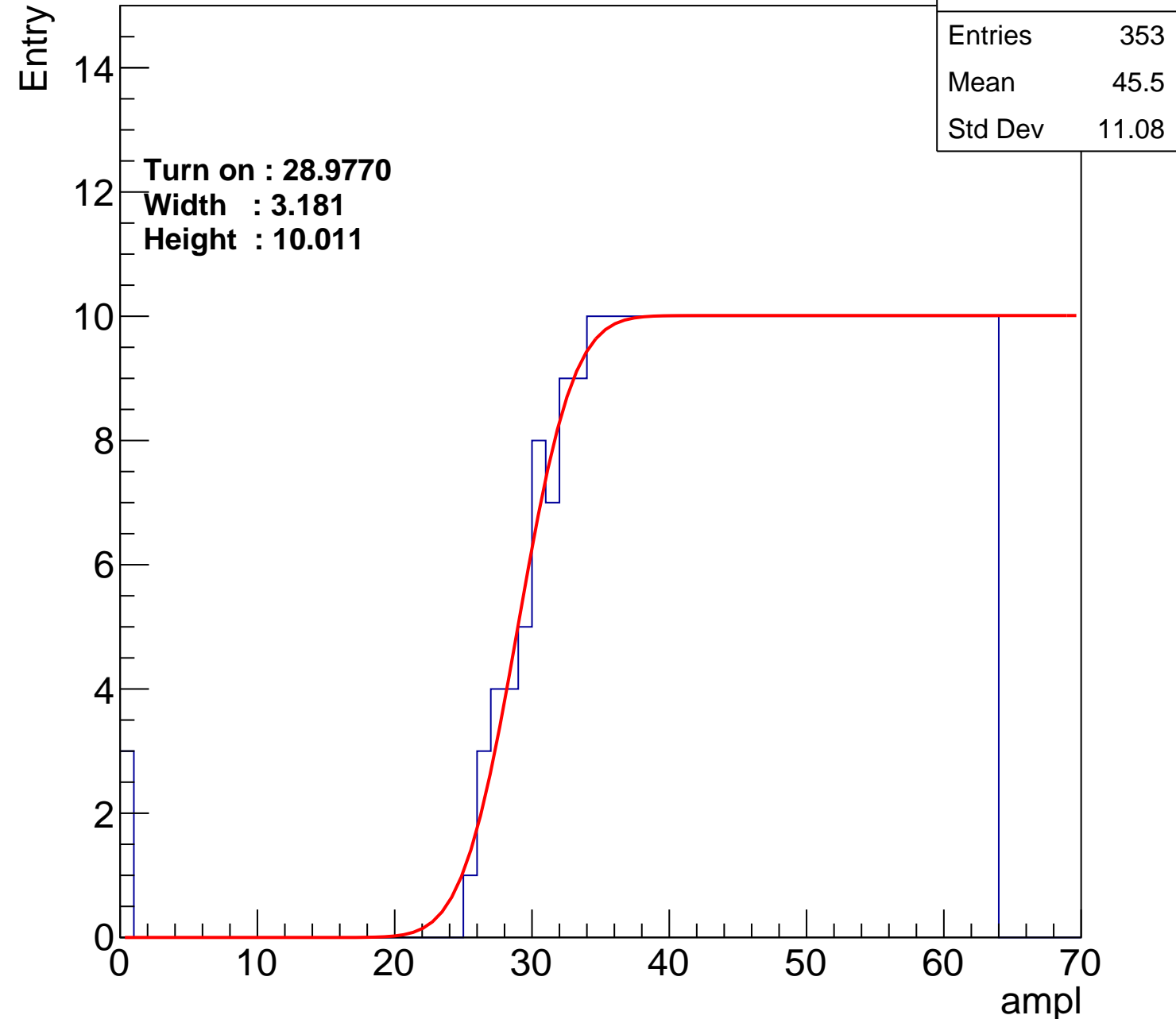
**Width : 3.181**

**Height : 10.011**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch102

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	371
Mean	44.56
Std Dev	11.68

Turn on : 27.9510

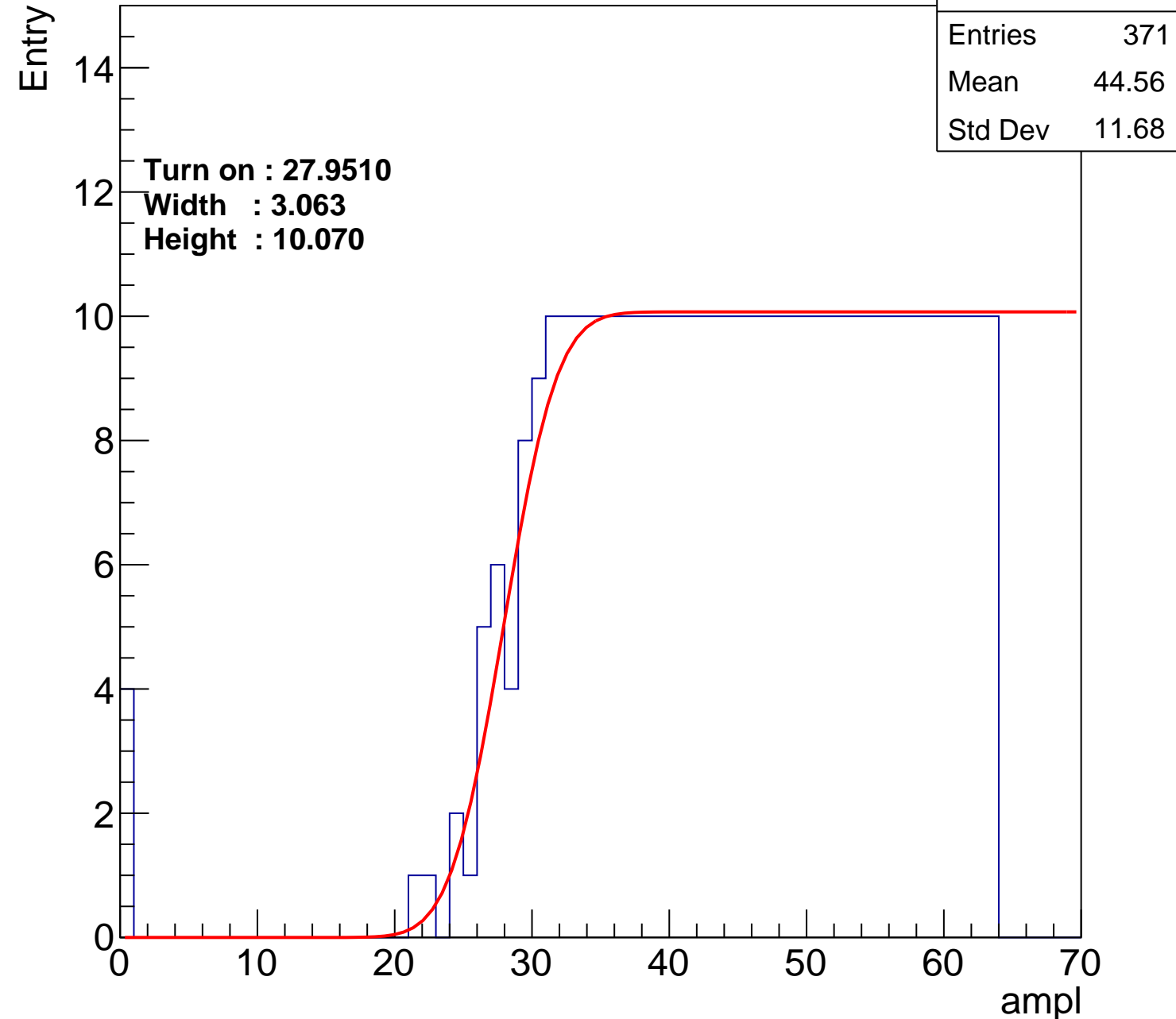
Width : 3.063

Height : 10.070

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L001S, U20-ch103

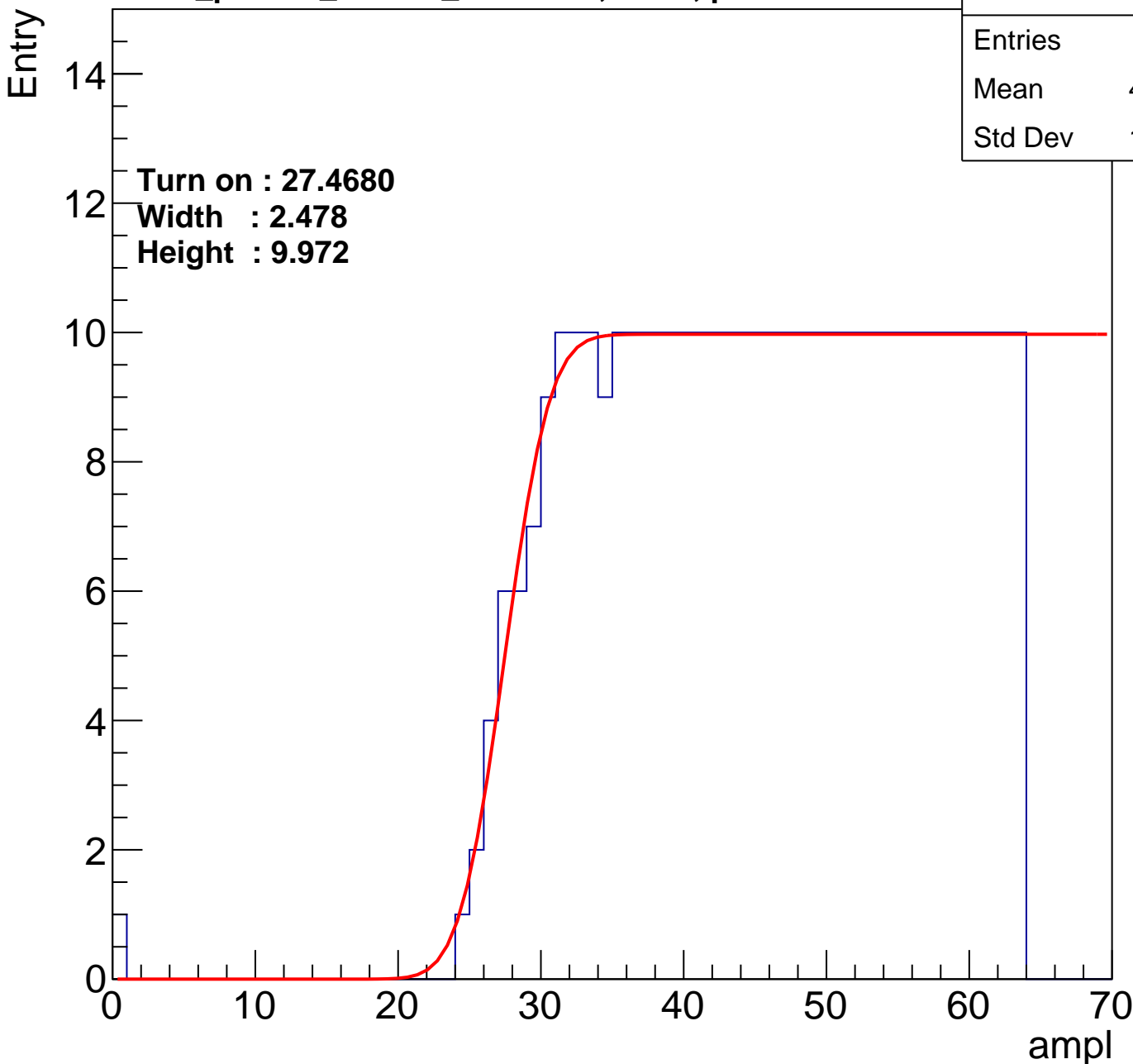
**calib\_packv5\_042523\_0143.root, FC#9, port A1**

Entries	365
Mean	45.09
Std Dev	10.89

**Turn on : 27.4680**

**Width : 2.478**

**Height : 9.972**



# B0L001S, U20-ch104

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	376
Mean	44.42
Std Dev	11.56

Turn on : 27.3553

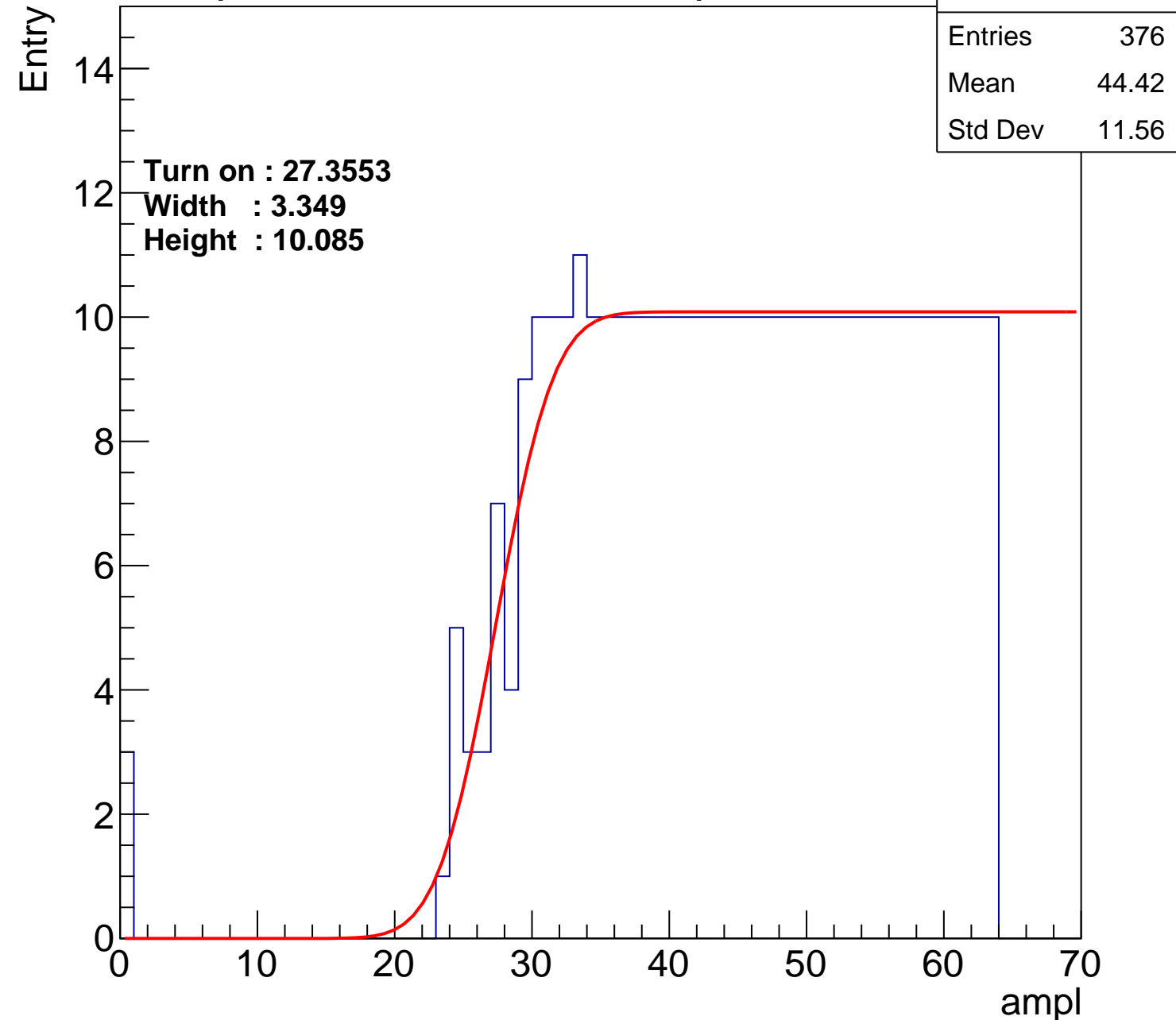
Width : 3.349

Height : 10.085

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch105

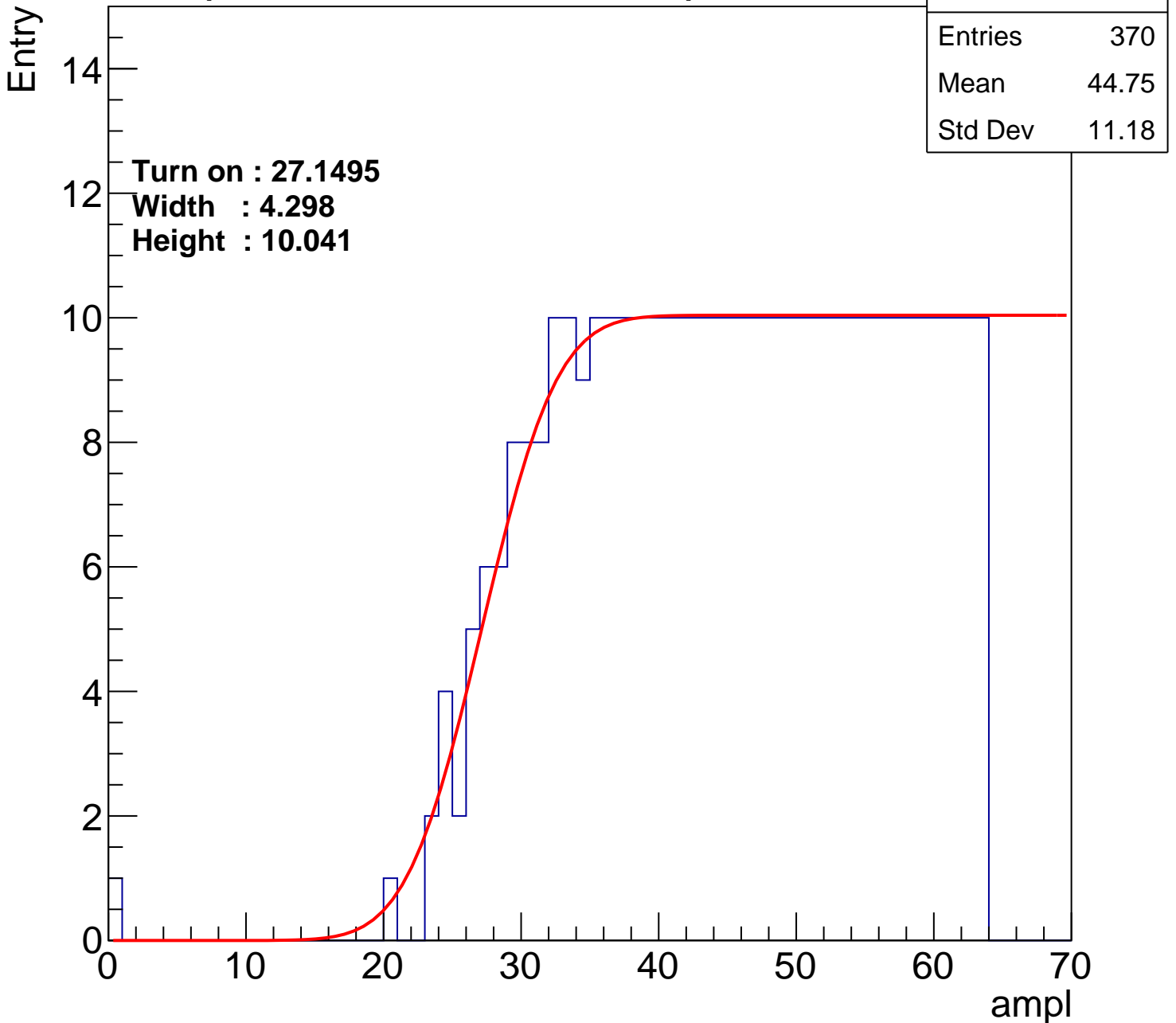
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	370
Mean	44.75
Std Dev	11.18

Turn on : 27.1495

Width : 4.298

Height : 10.041



# B0L001S, U20-ch106

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	370
Mean	44.38
Std Dev	12.22

Turn on : 27.8995

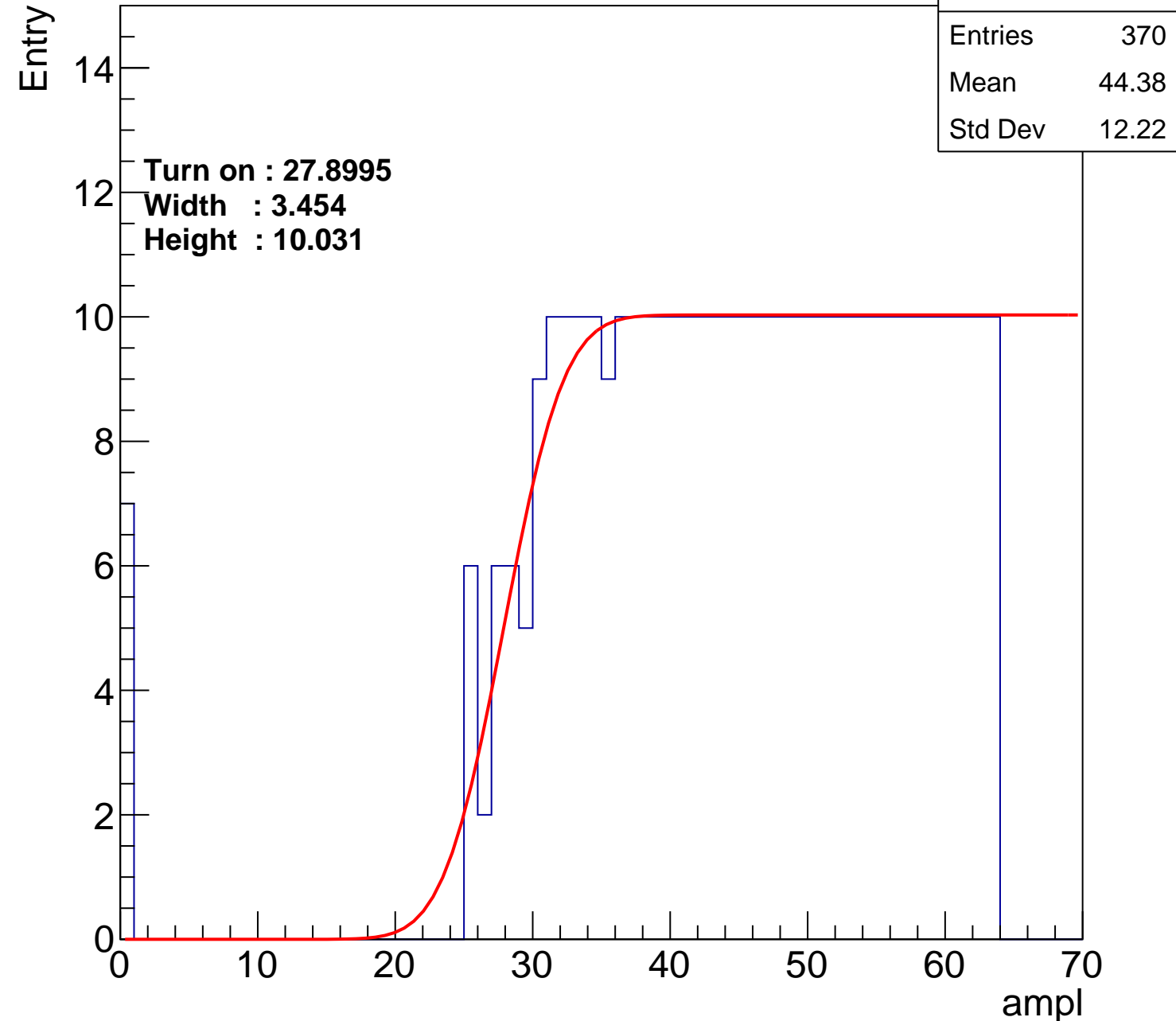
Width : 3.454

Height : 10.031

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch107

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	375
Mean	44.44
Std Dev	11.57

Turn on : 26.8625

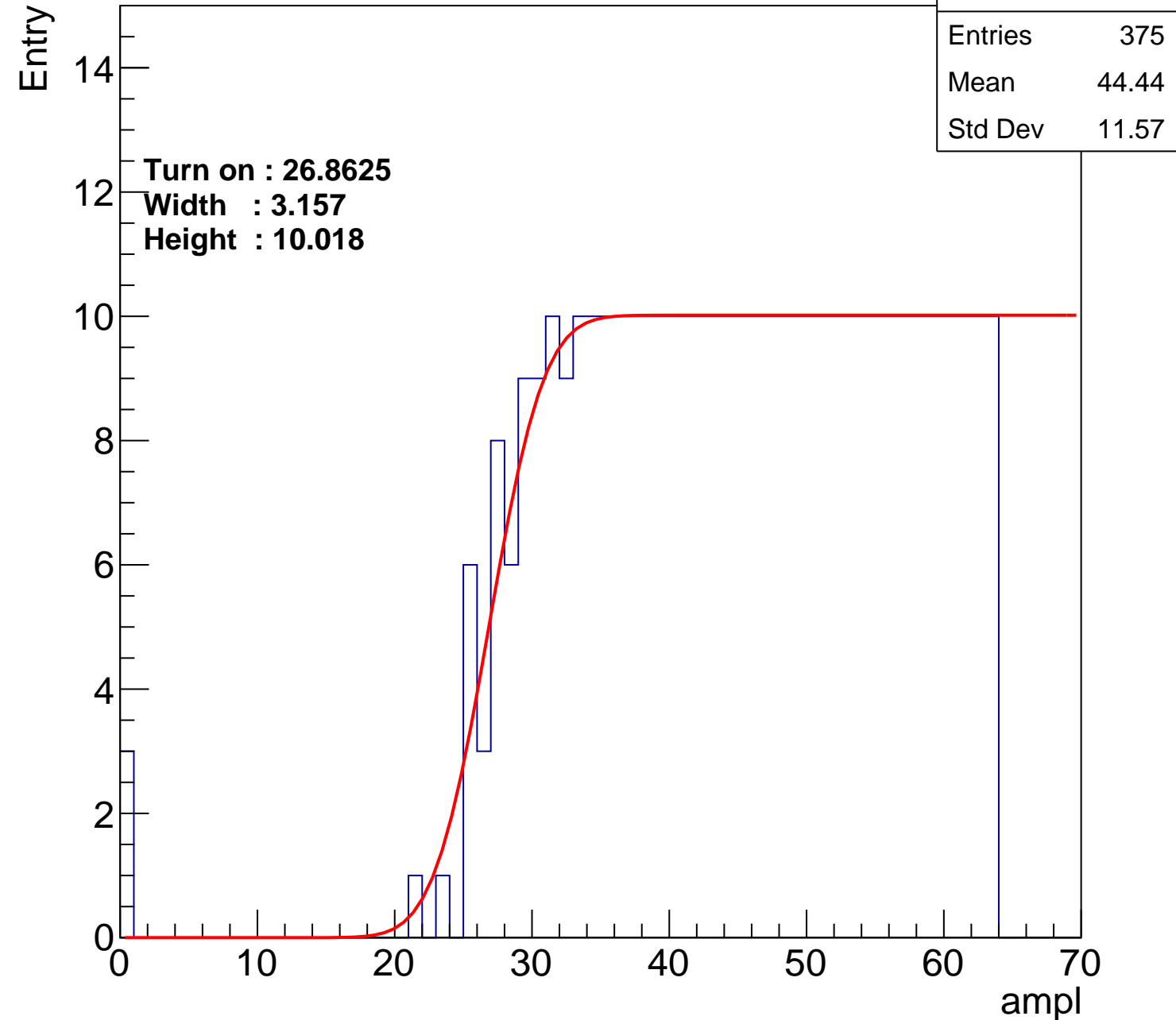
Width : 3.157

Height : 10.018

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch108

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	372
Mean	44.69
Std Dev	11.18

**Turn on : 27.1547**

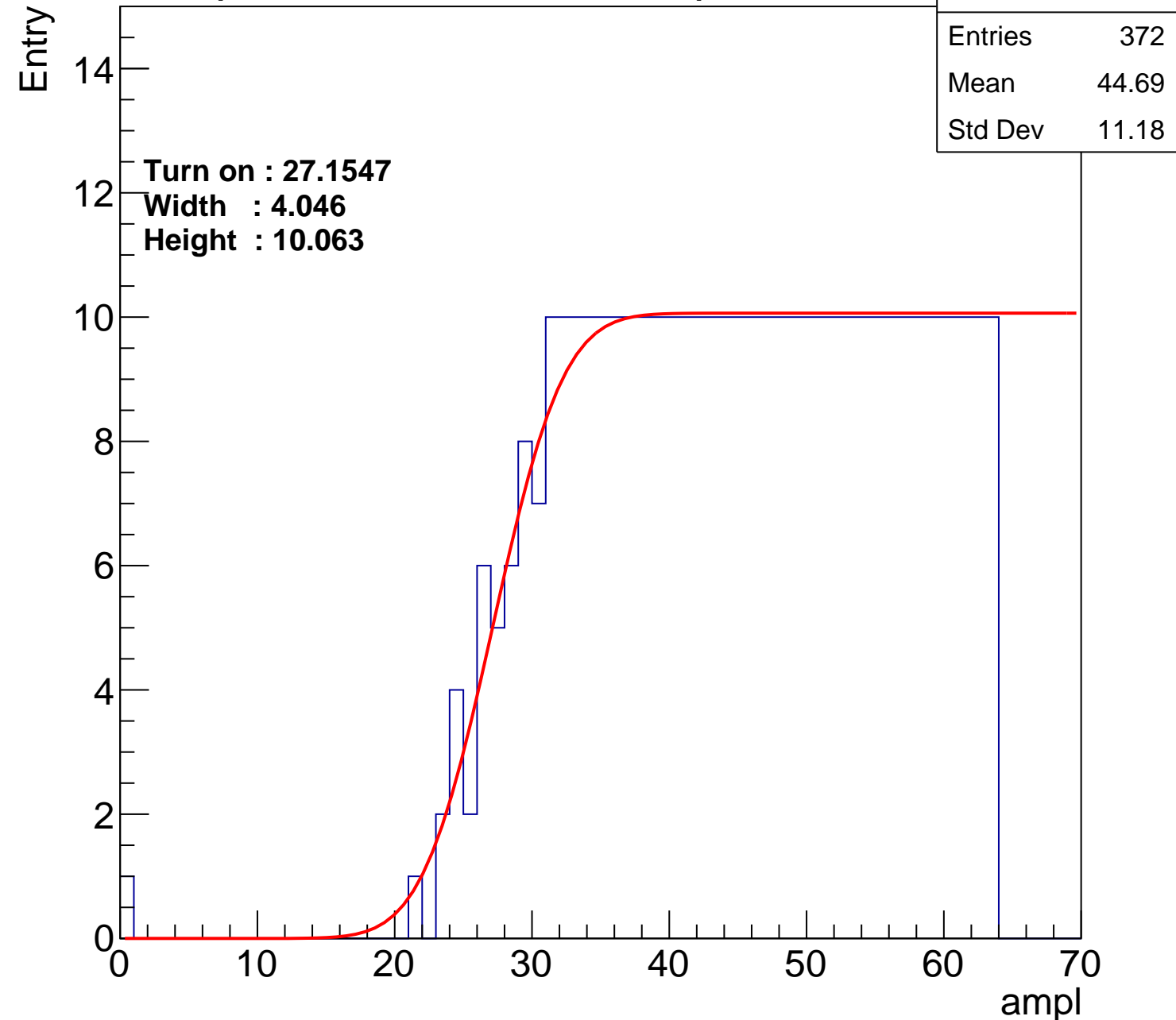
**Width : 4.046**

**Height : 10.063**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch109

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	339
Mean	46.19
Std Dev	10.74

Turn on : 30.5489

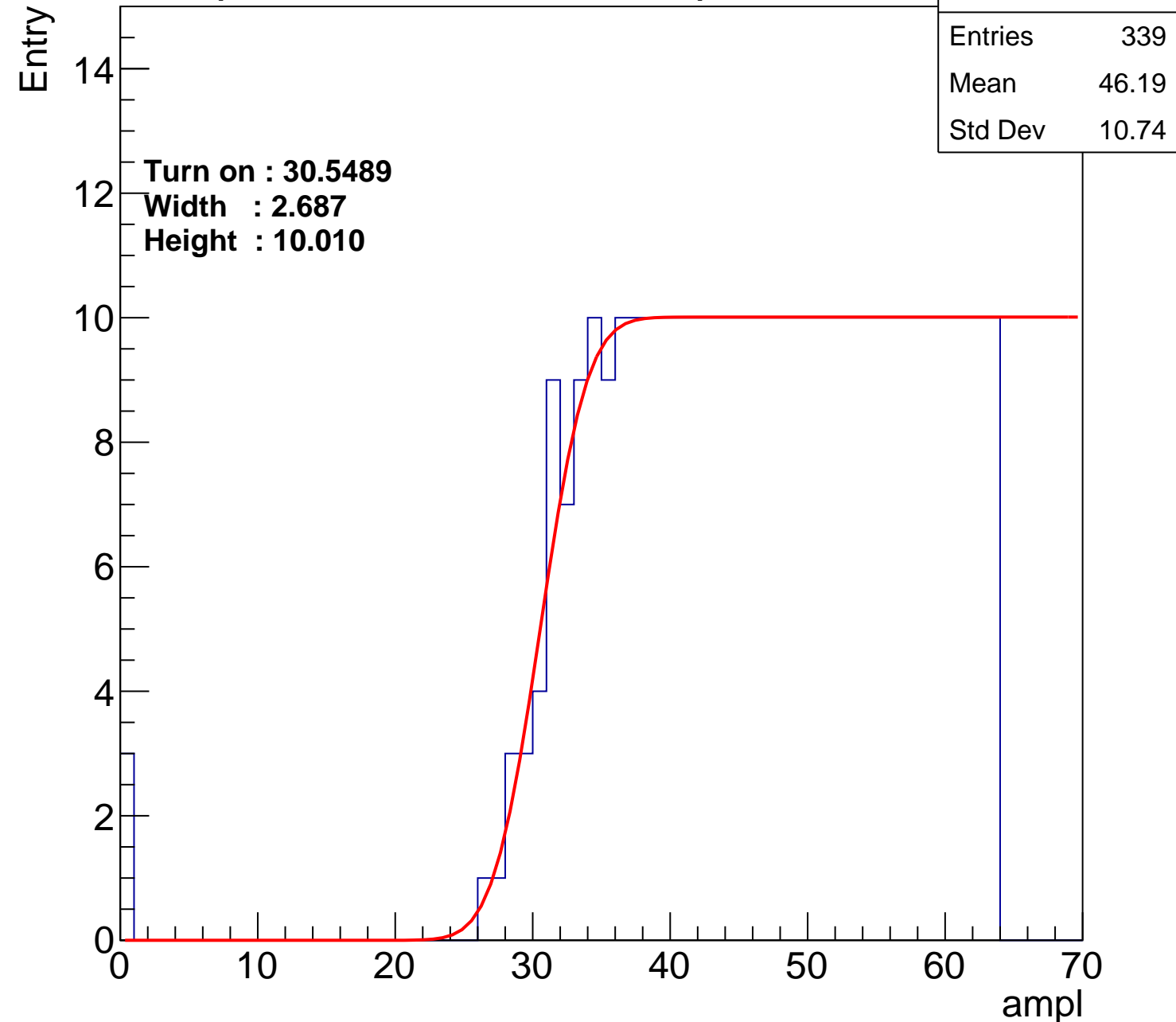
Width : 2.687

Height : 10.010

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch110

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	368
Mean	44.73
Std Dev	11.49

Turn on : 28.0203

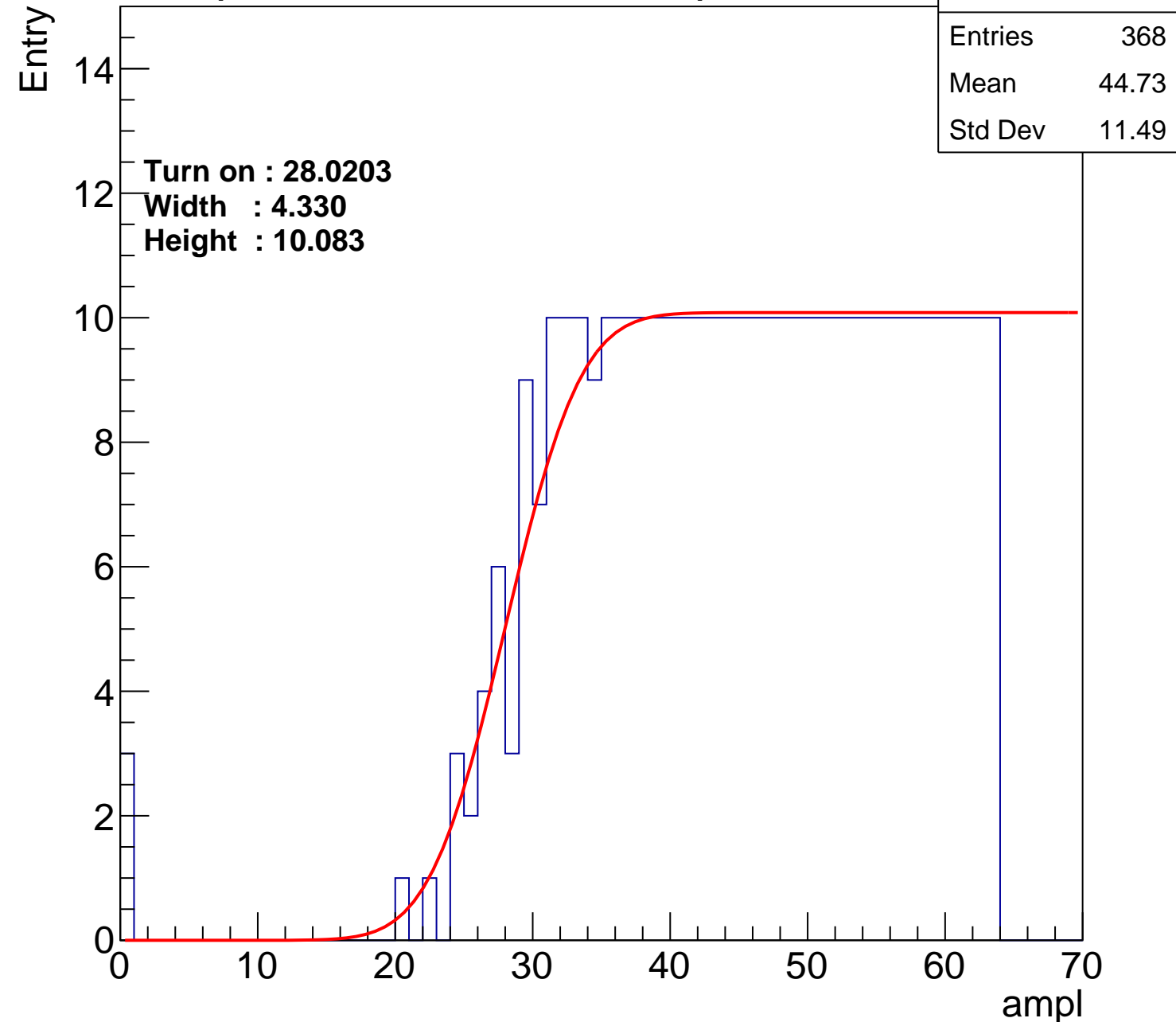
Width : 4.330

Height : 10.083

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L001S, U20-ch111

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	358
Mean	45.11
Std Dev	11.61

**Turn on : 29.0383**

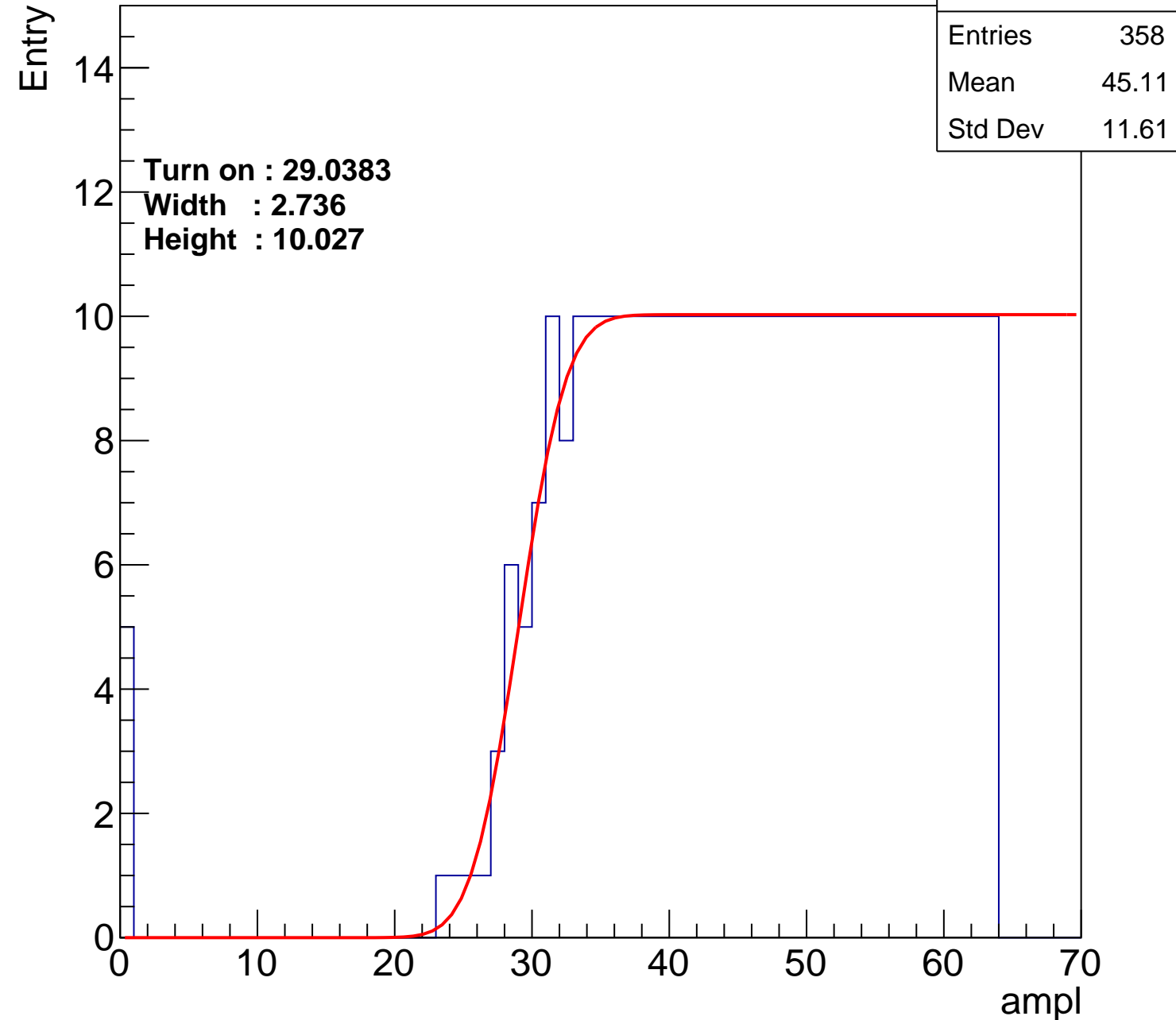
**Width : 2.736**

**Height : 10.027**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch112

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	355
Mean	45.14
Std Dev	11.81

**Turn on : 29.6306**

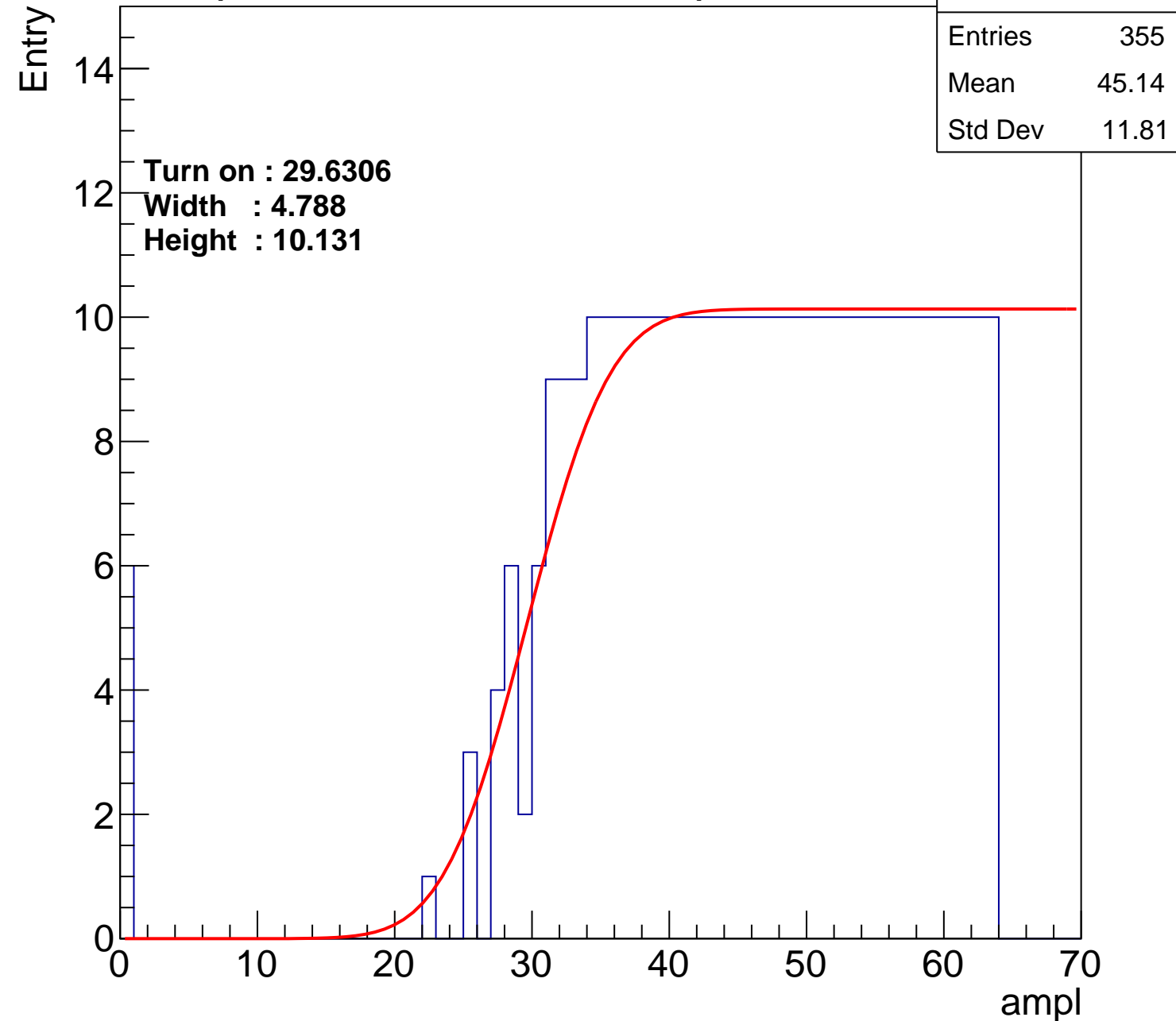
**Width : 4.788**

**Height : 10.131**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch113

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	385
Mean	44.03
Std Dev	11.63

Turn on : 26.0950

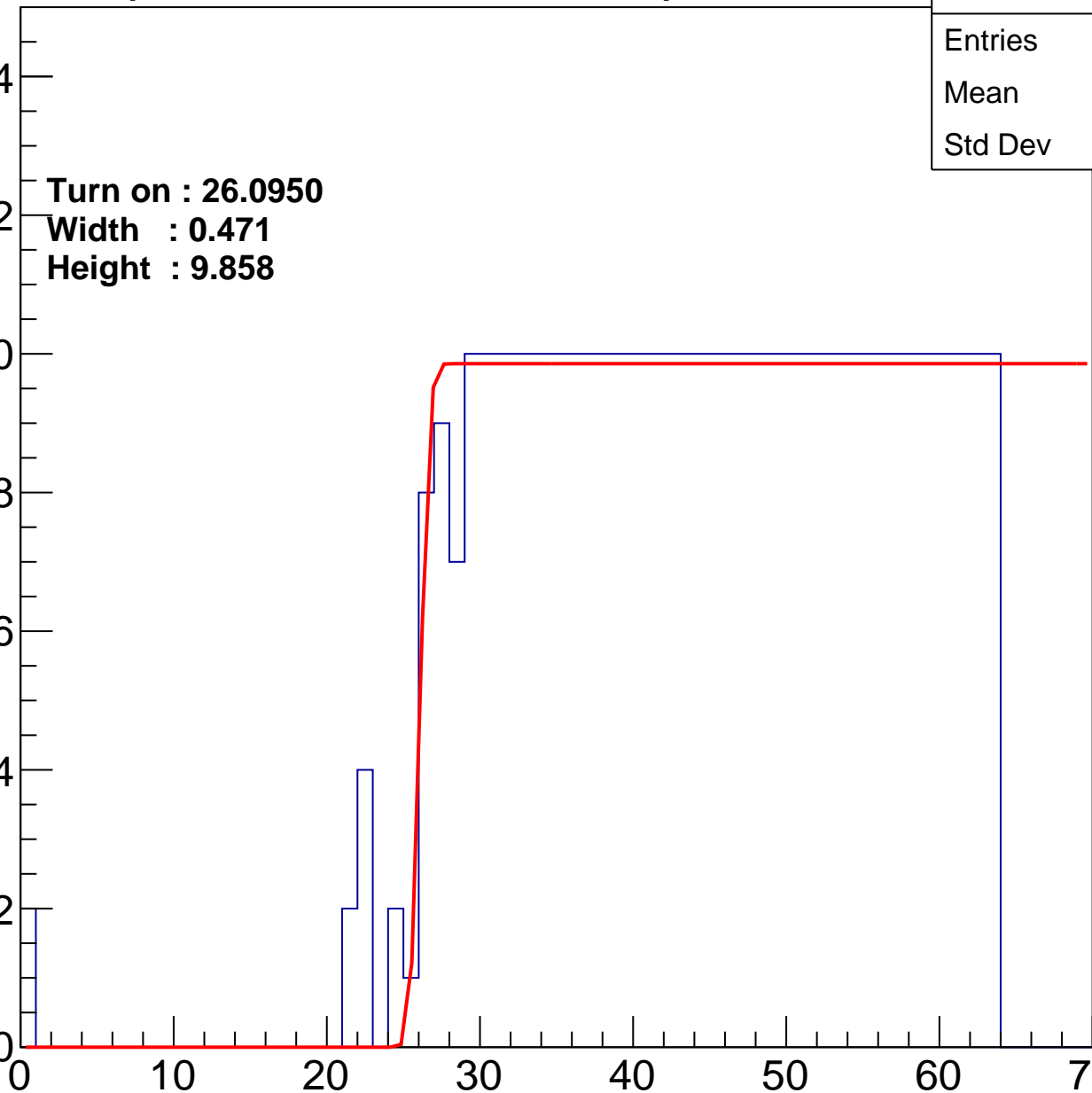
Width : 0.471

Height : 9.858

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch114

calib\_packv5\_042523\_0143.root, FC#9, port A1

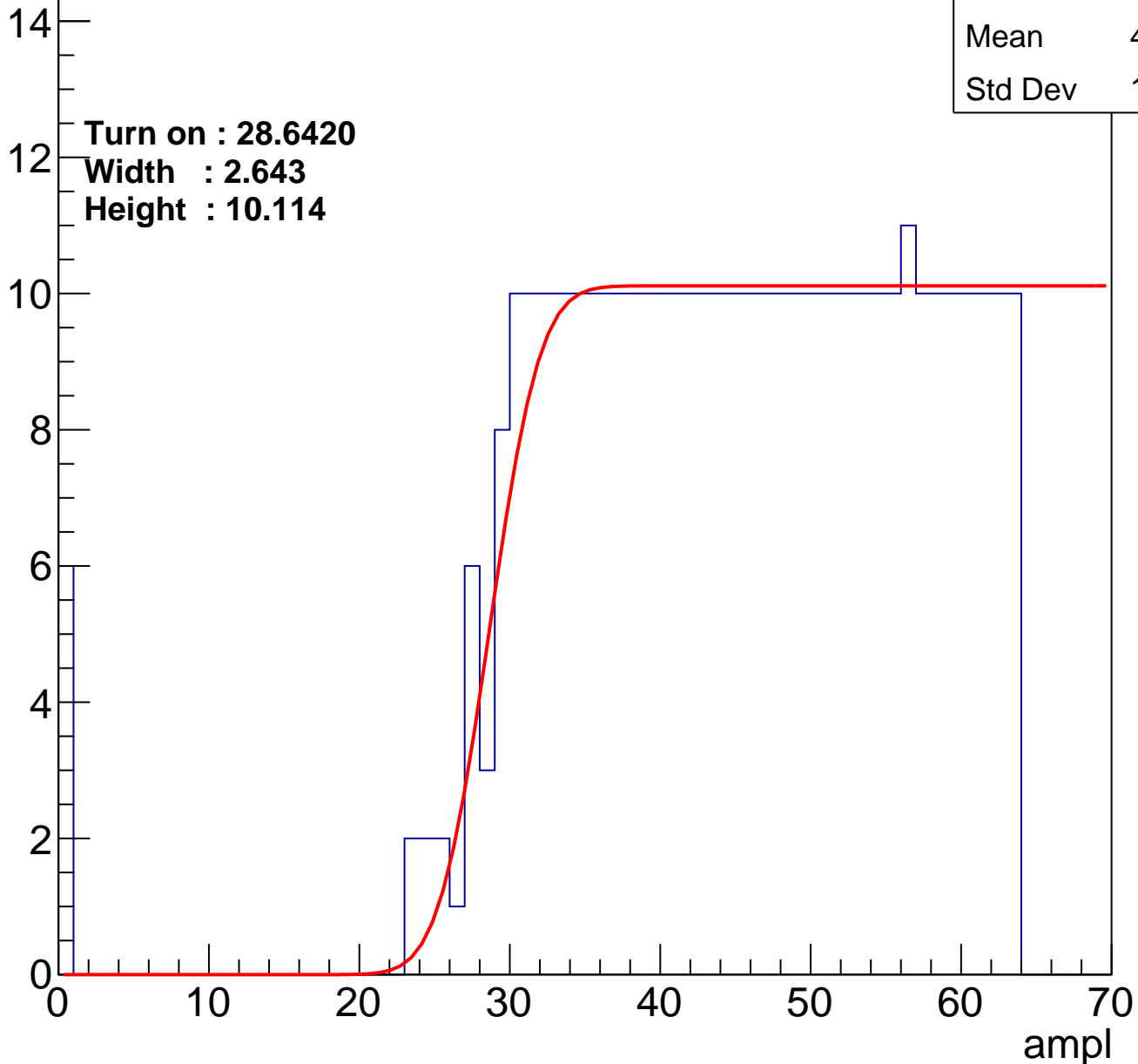
Entries	371
Mean	44.51
Std Dev	12.01

Turn on : 28.6420

Width : 2.643

Height : 10.114

Entry



# B0L001S, U20-ch115

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	373
Mean	44.39
Std Dev	11.91

Turn on : 28.2172

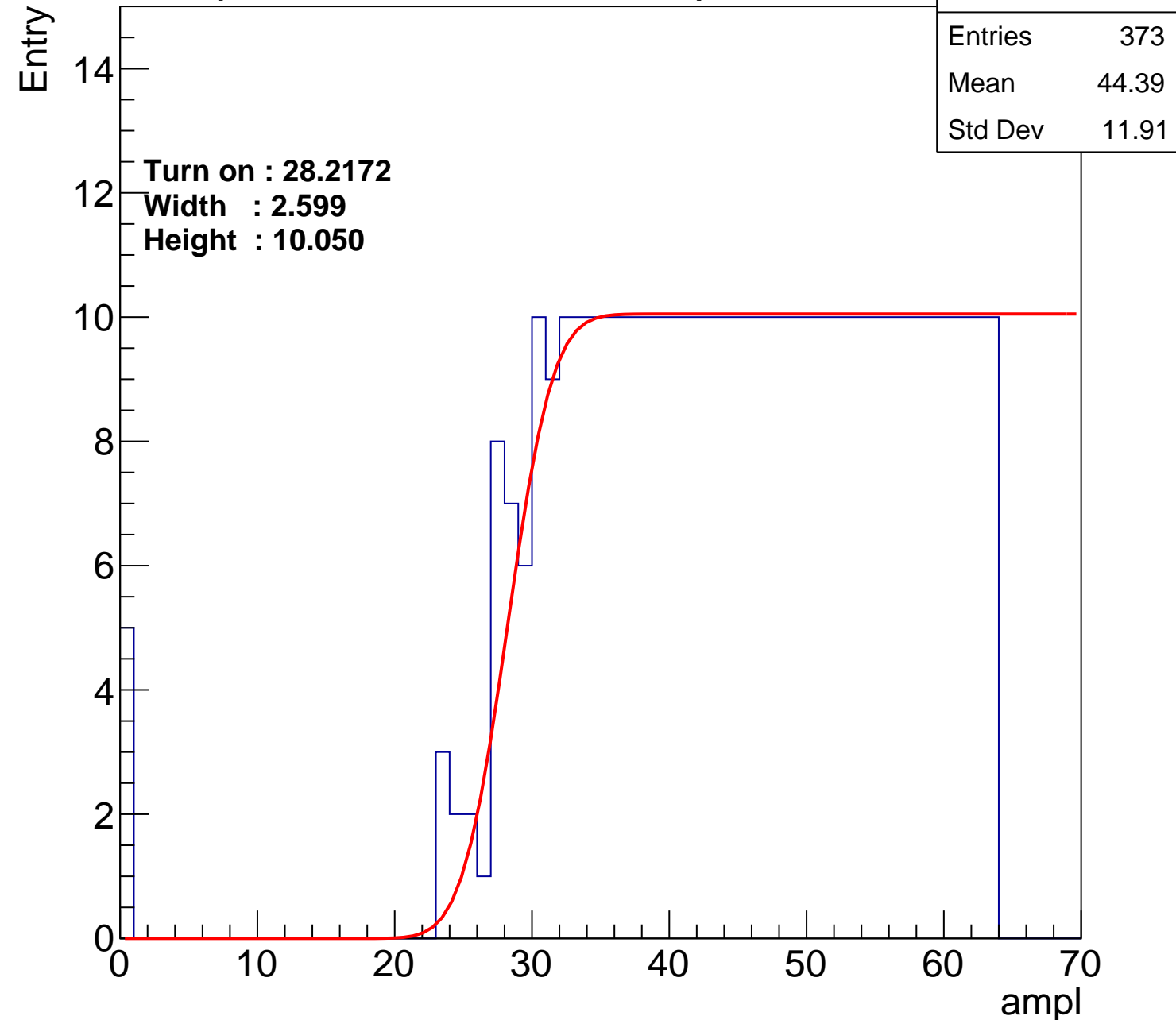
Width : 2.599

Height : 10.050

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch116

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	366
Mean	44.61
Std Dev	12.11

**Turn on : 28.1746**

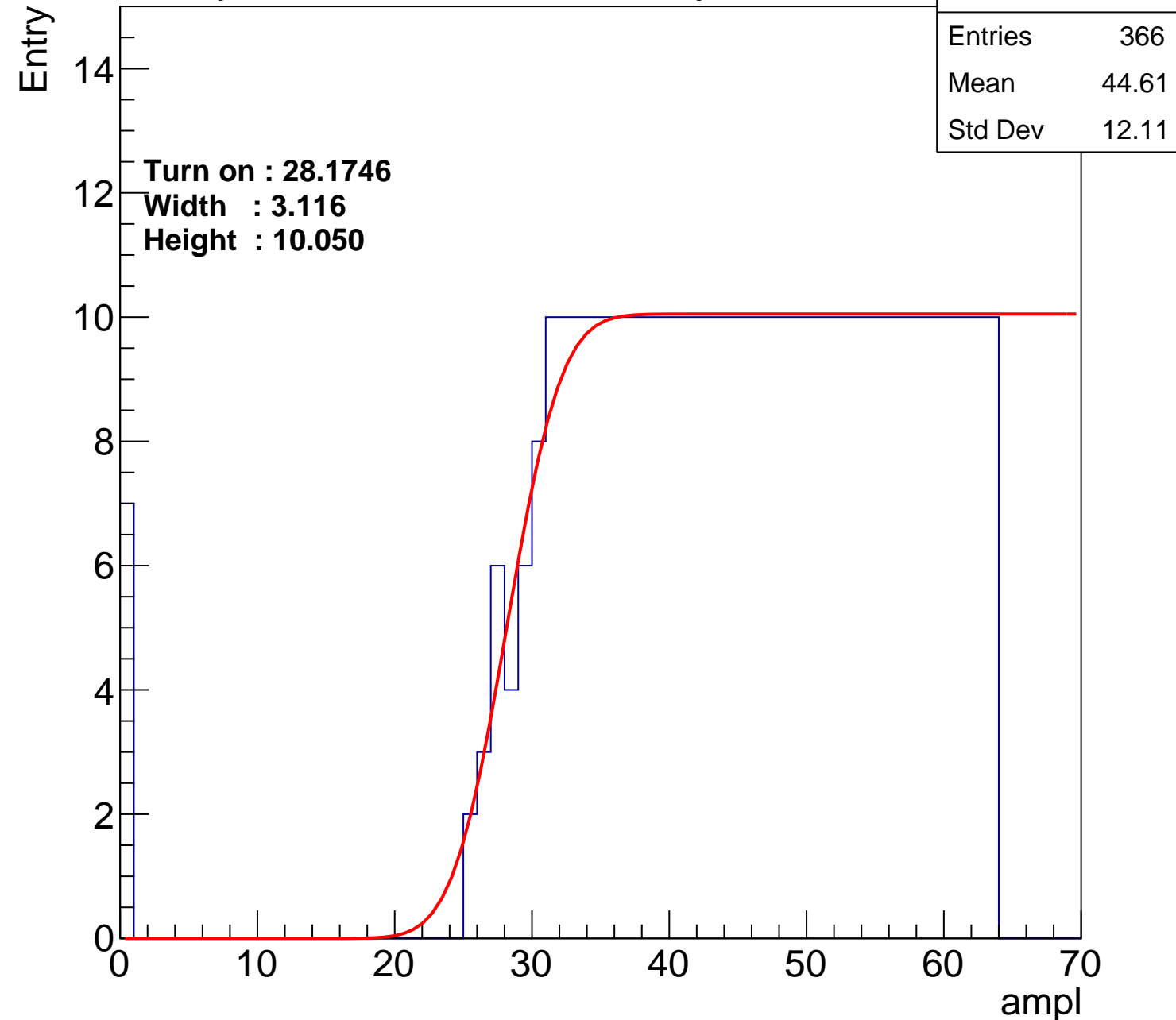
**Width : 3.116**

**Height : 10.050**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch117

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	379
Mean	44.06
Std Dev	12.11

Turn on : 27.3234

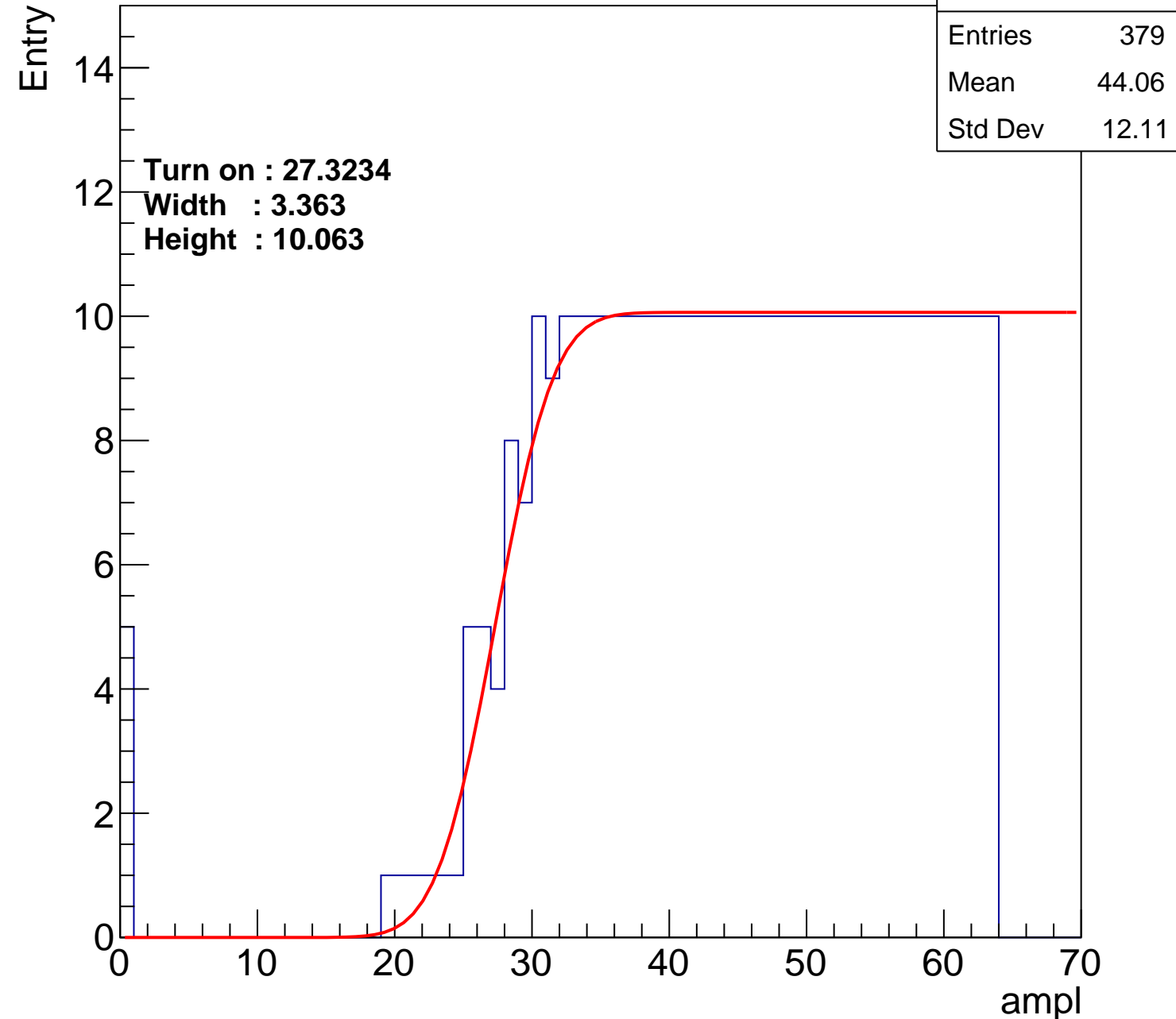
Width : 3.363

Height : 10.063

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch118

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	372
Mean	44.7
Std Dev	11.26

Turn on : 27.5672

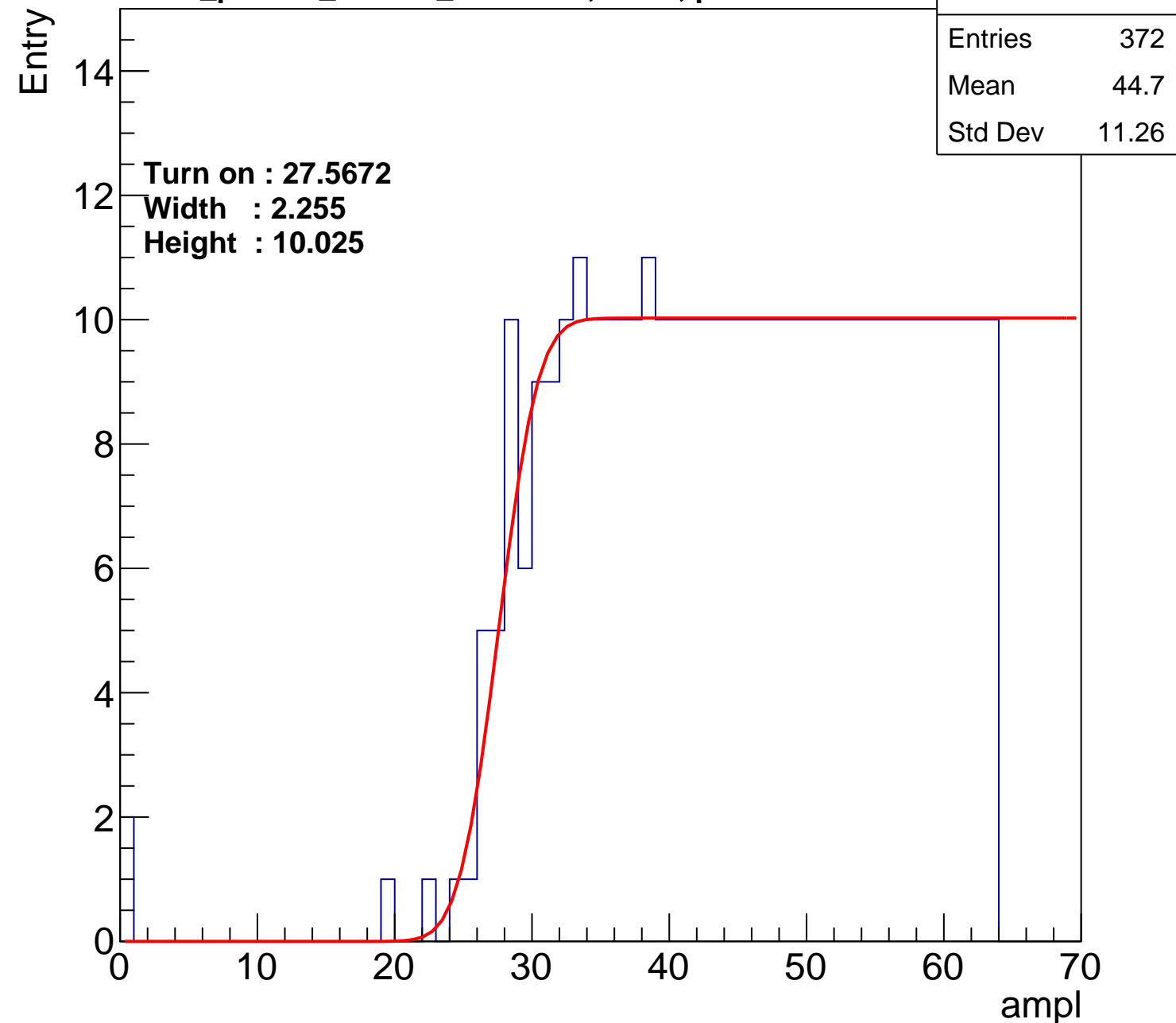
Width : 2.255

Height : 10.025

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L001S, U20-ch119

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	361
Mean	45.19
Std Dev	11.24

**Turn on : 28.6255**

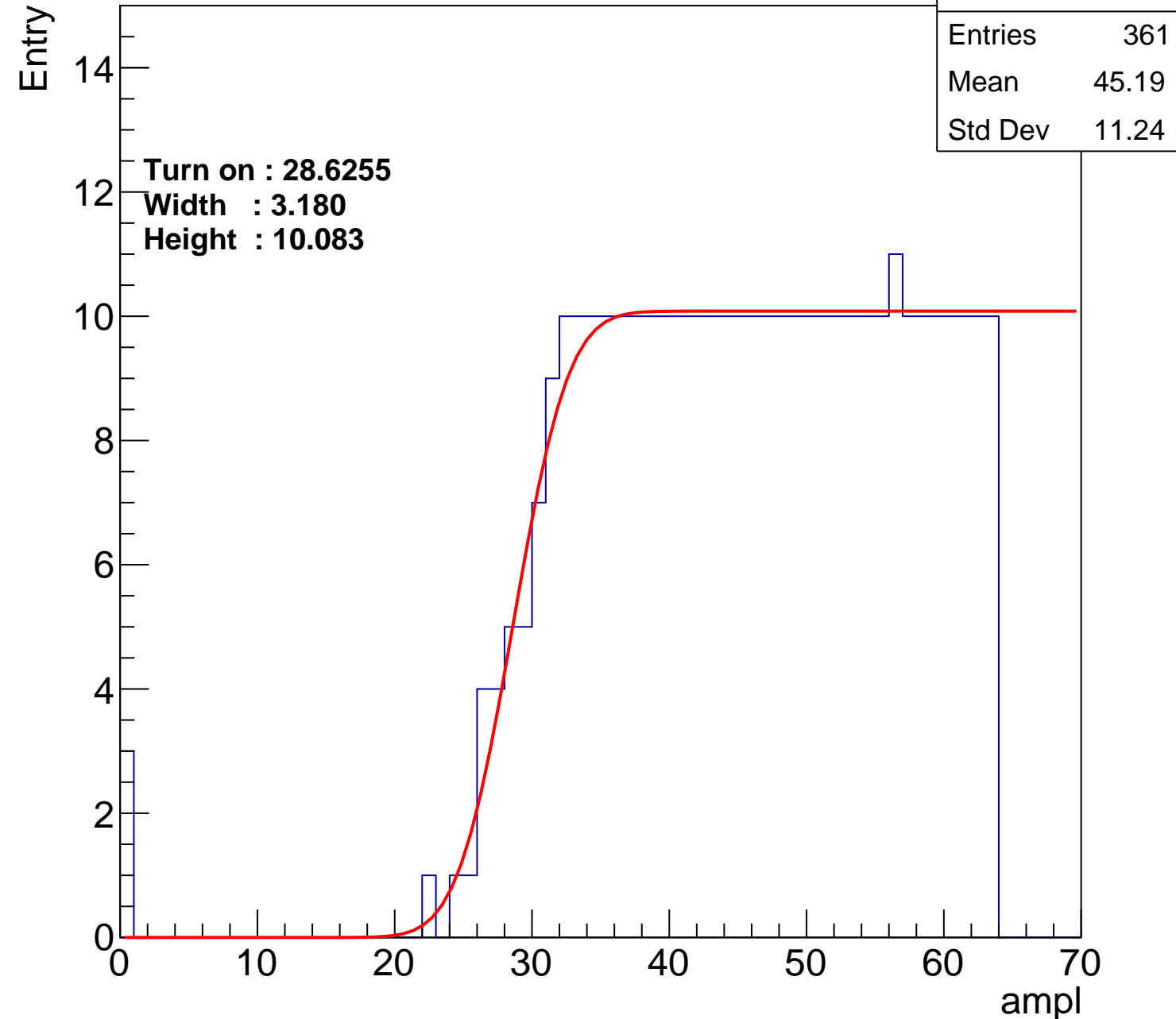
**Width : 3.180**

**Height : 10.083**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch120

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	358
Mean	45.47
Std Dev	10.65

**Turn on : 28.4900**

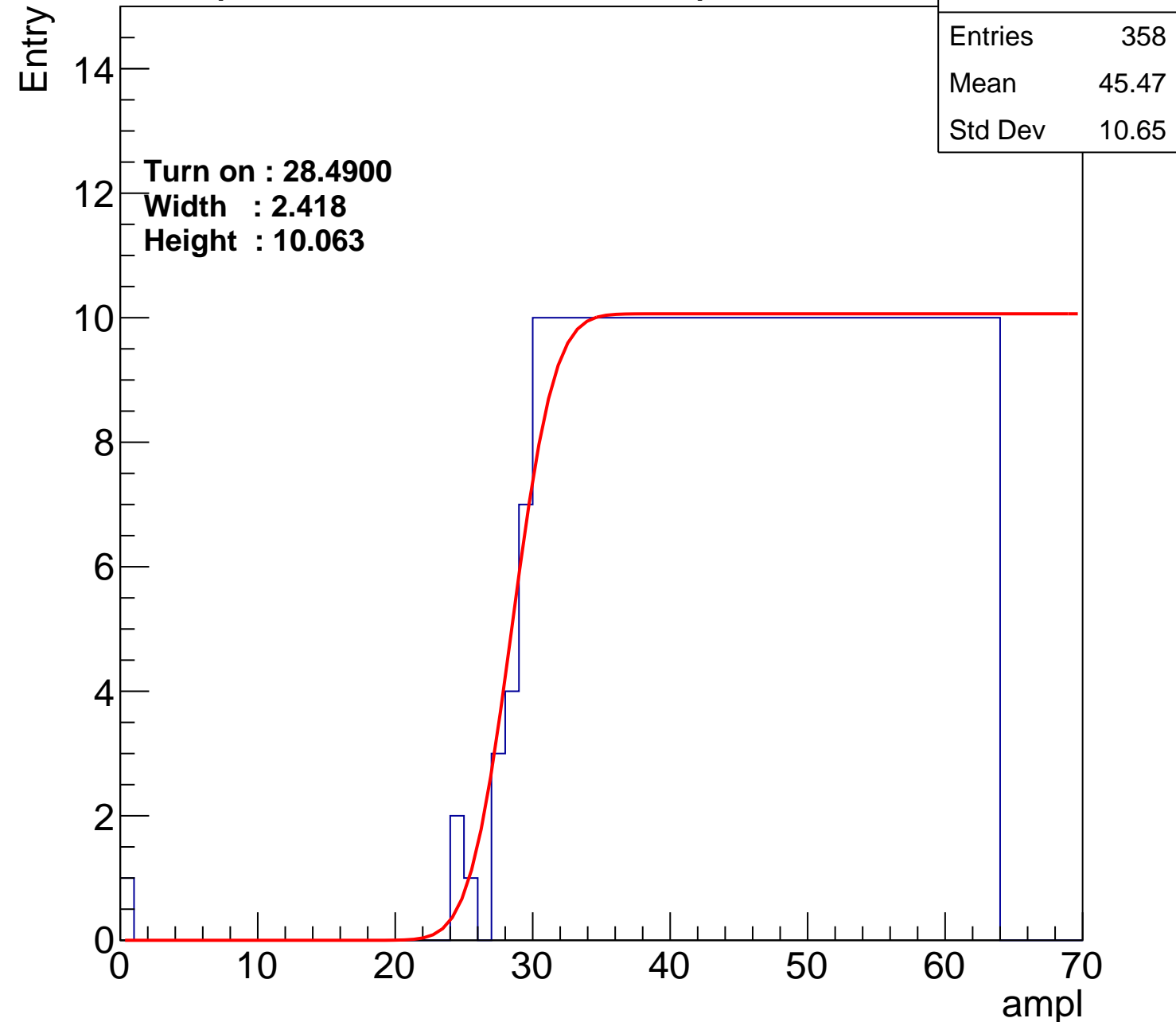
**Width : 2.418**

**Height : 10.063**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch121

calib\_packv5\_042523\_0143.root, FC#9, port A1

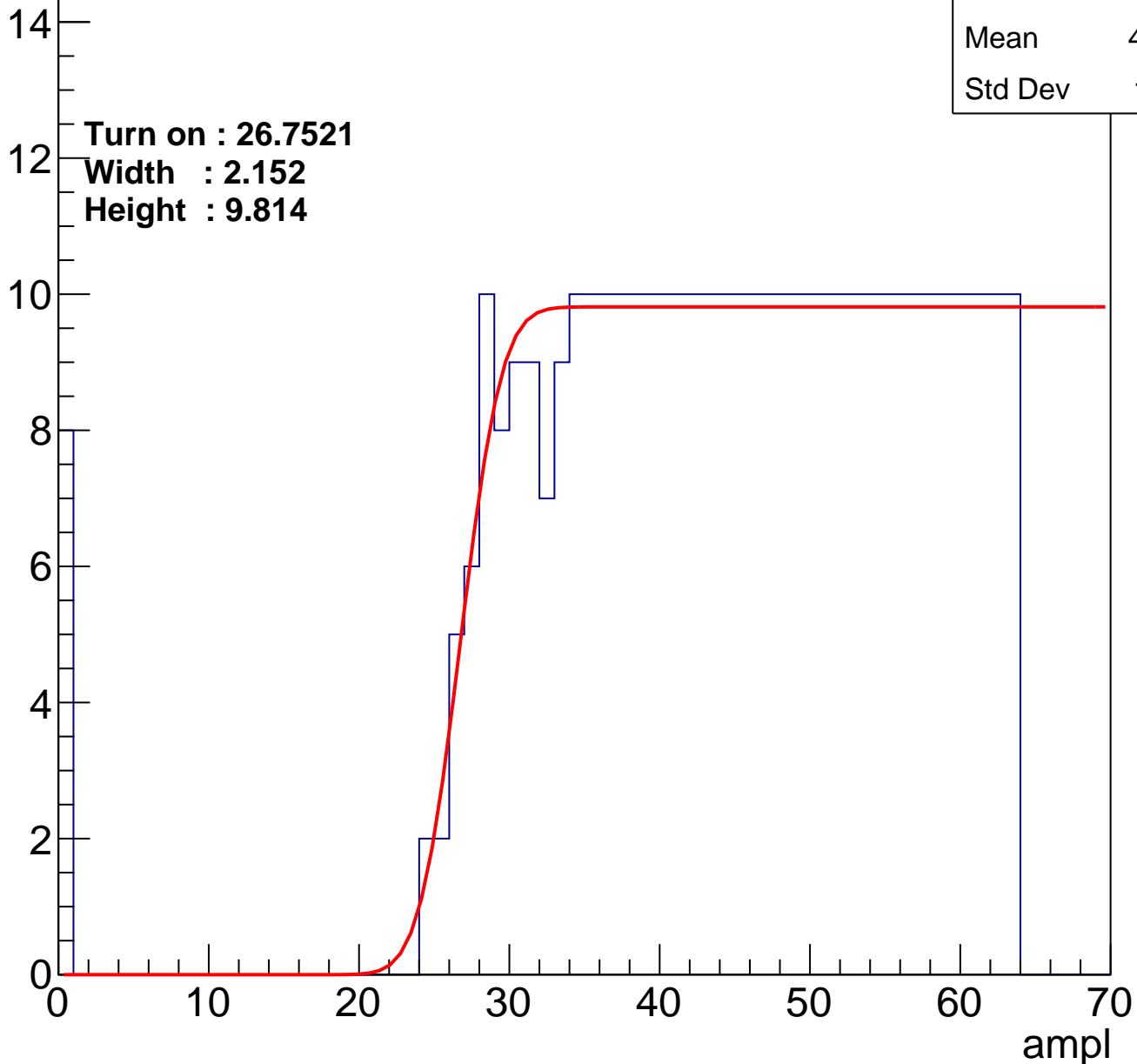
Entries	375
Mean	44.06
Std Dev	12.51

Turn on : 26.7521

Width : 2.152

Height : 9.814

Entry



# B0L001S, U20-ch122

calib\_packv5\_042523\_0143.root, FC#9, port A1

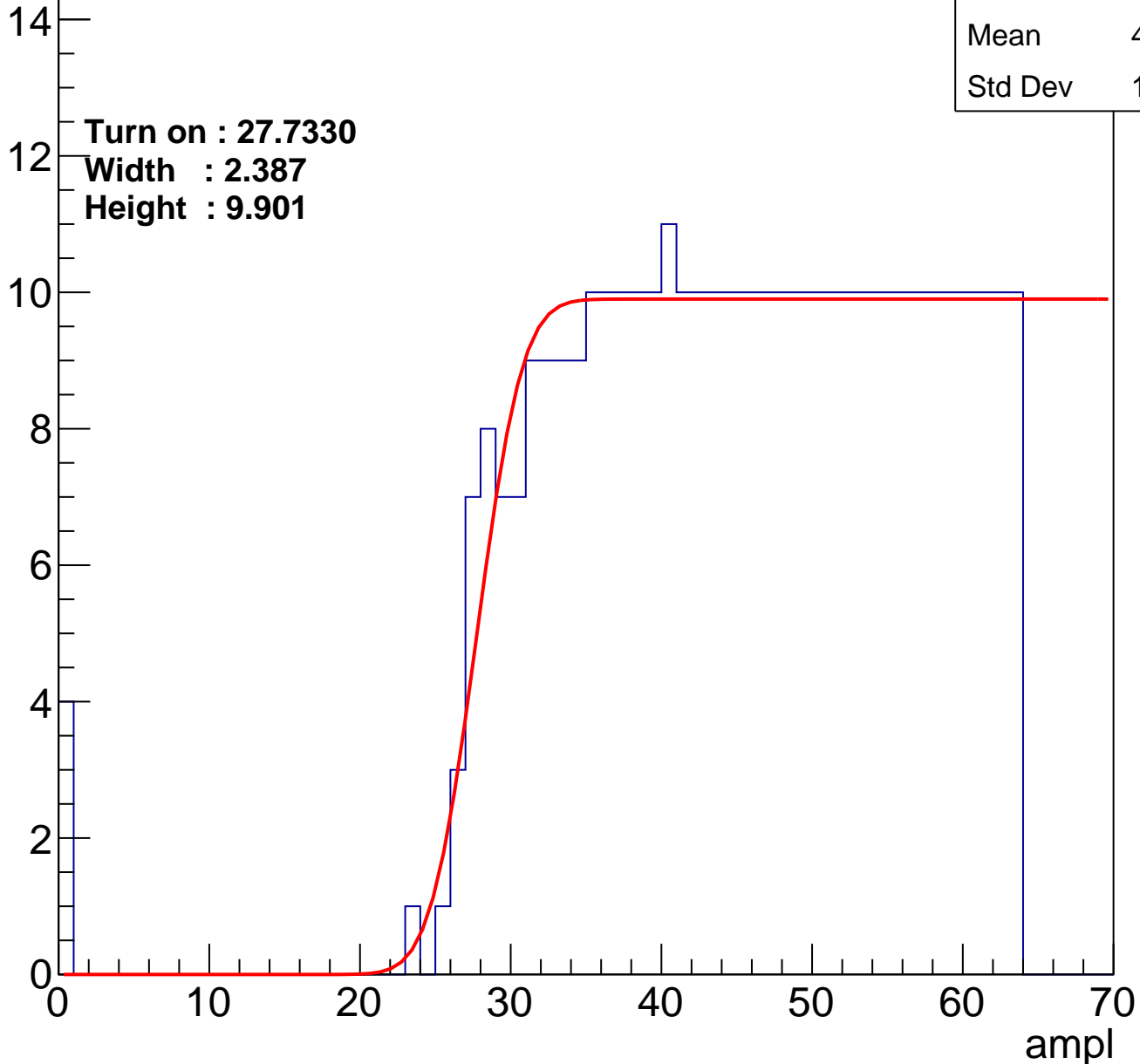
Entries	365
Mean	44.85
Std Dev	11.54

Turn on : 27.7330

Width : 2.387

Height : 9.901

Entry



# B0L001S, U20-ch123

calib\_packv5\_042523\_0143.root, FC#9, port A1

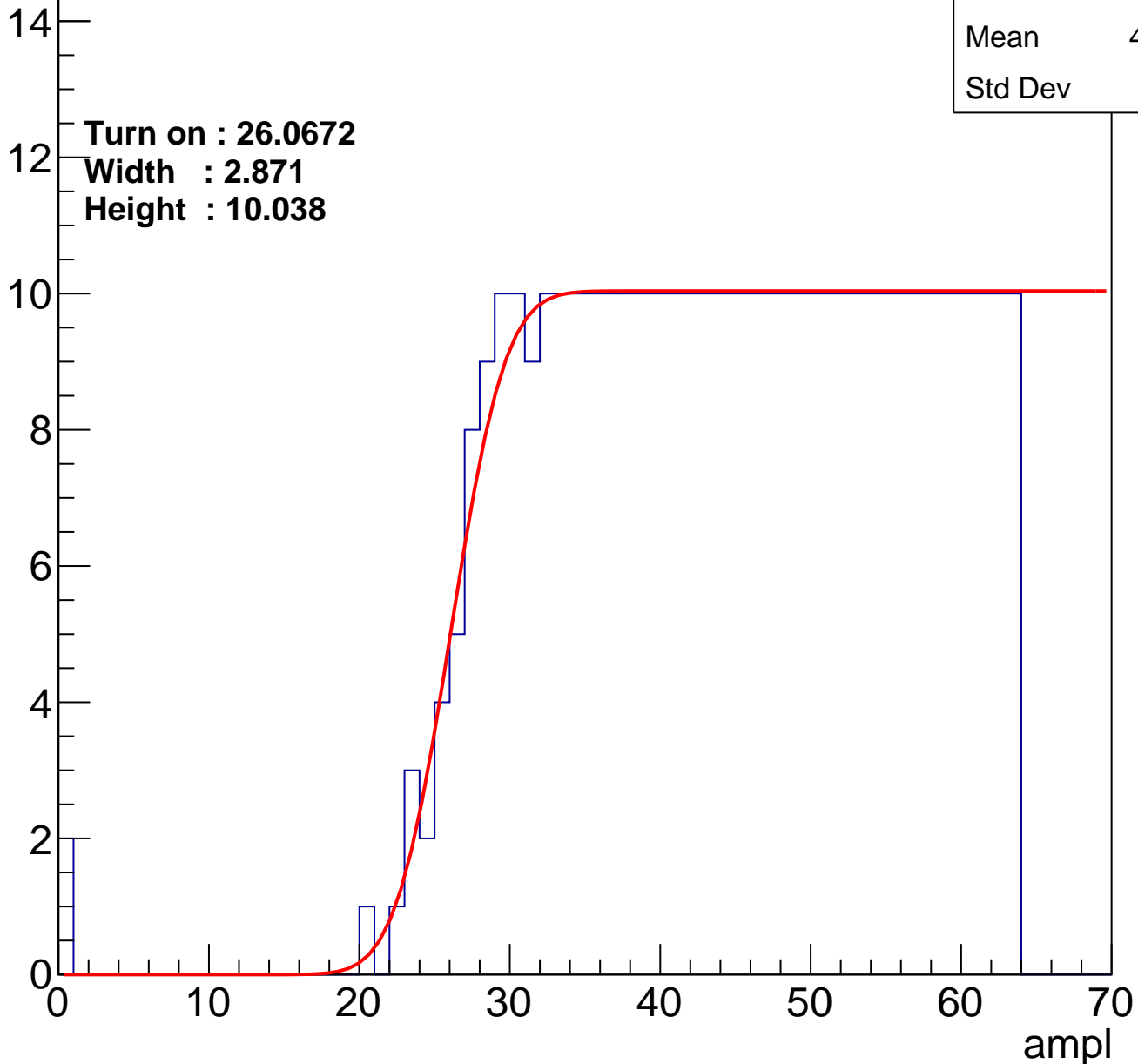
Entries	384
Mean	44.08
Std Dev	11.6

Turn on : 26.0672

Width : 2.871

Height : 10.038

Entry



# B0L001S, U20-ch124

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	370
Mean	44.61
Std Dev	11.66

**Turn on : 27.6703**

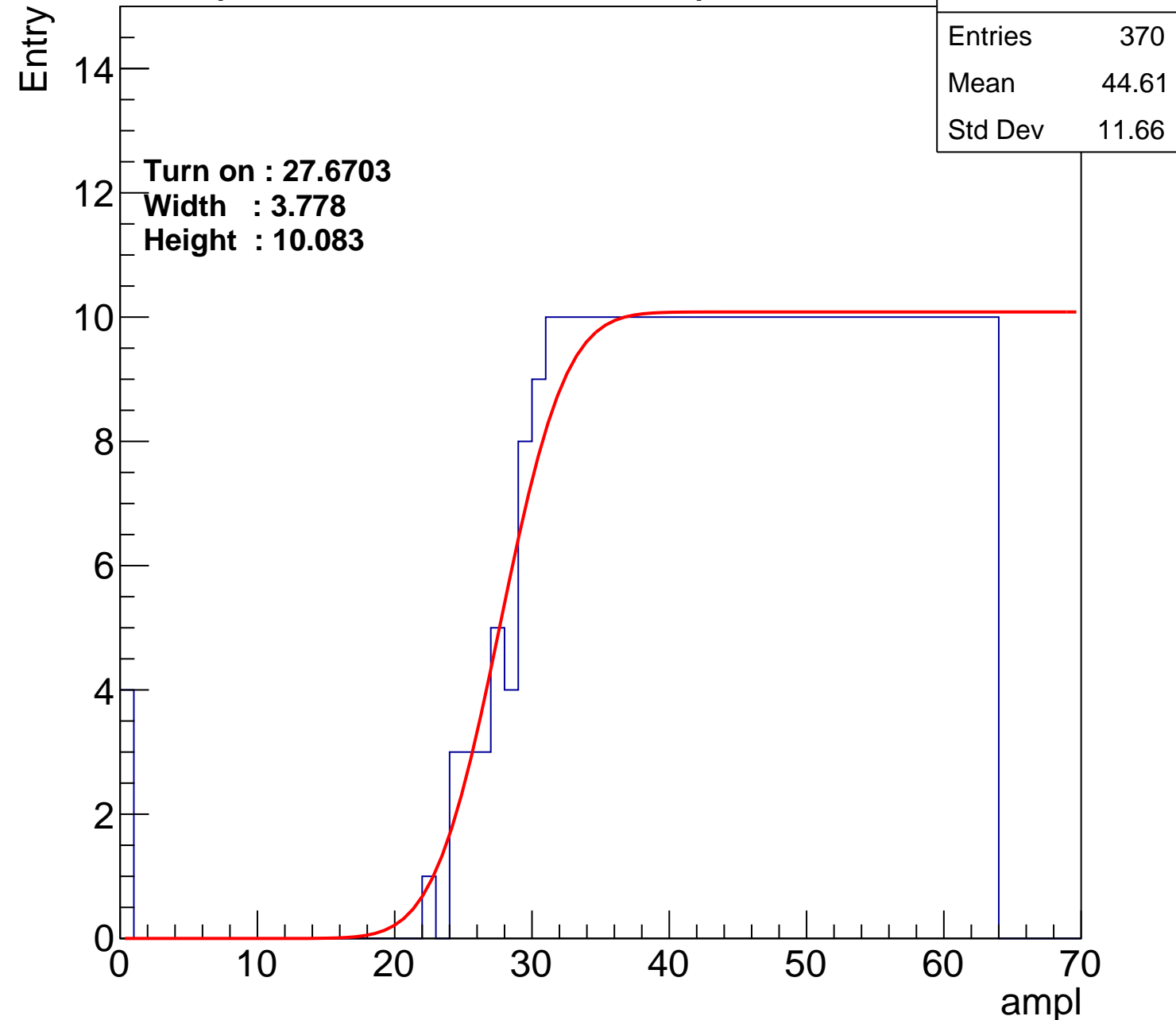
**Width : 3.778**

**Height : 10.083**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch125

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	365
Mean	44.96
Std Dev	11.36

Turn on : 27.6926

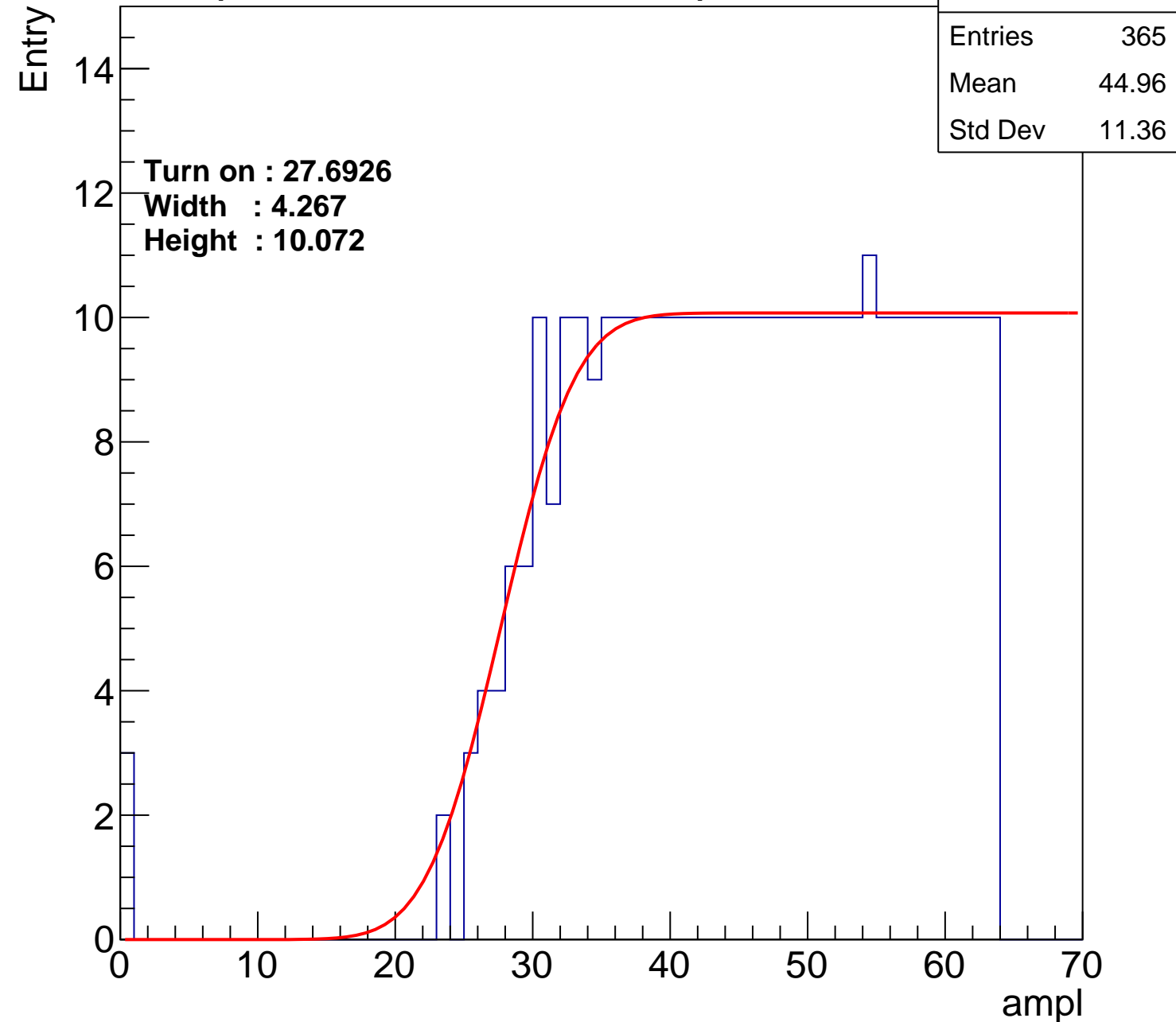
Width : 4.267

Height : 10.072

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch126

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	362
Mean	45.06
Std Dev	11.29

Turn on : 28.8491

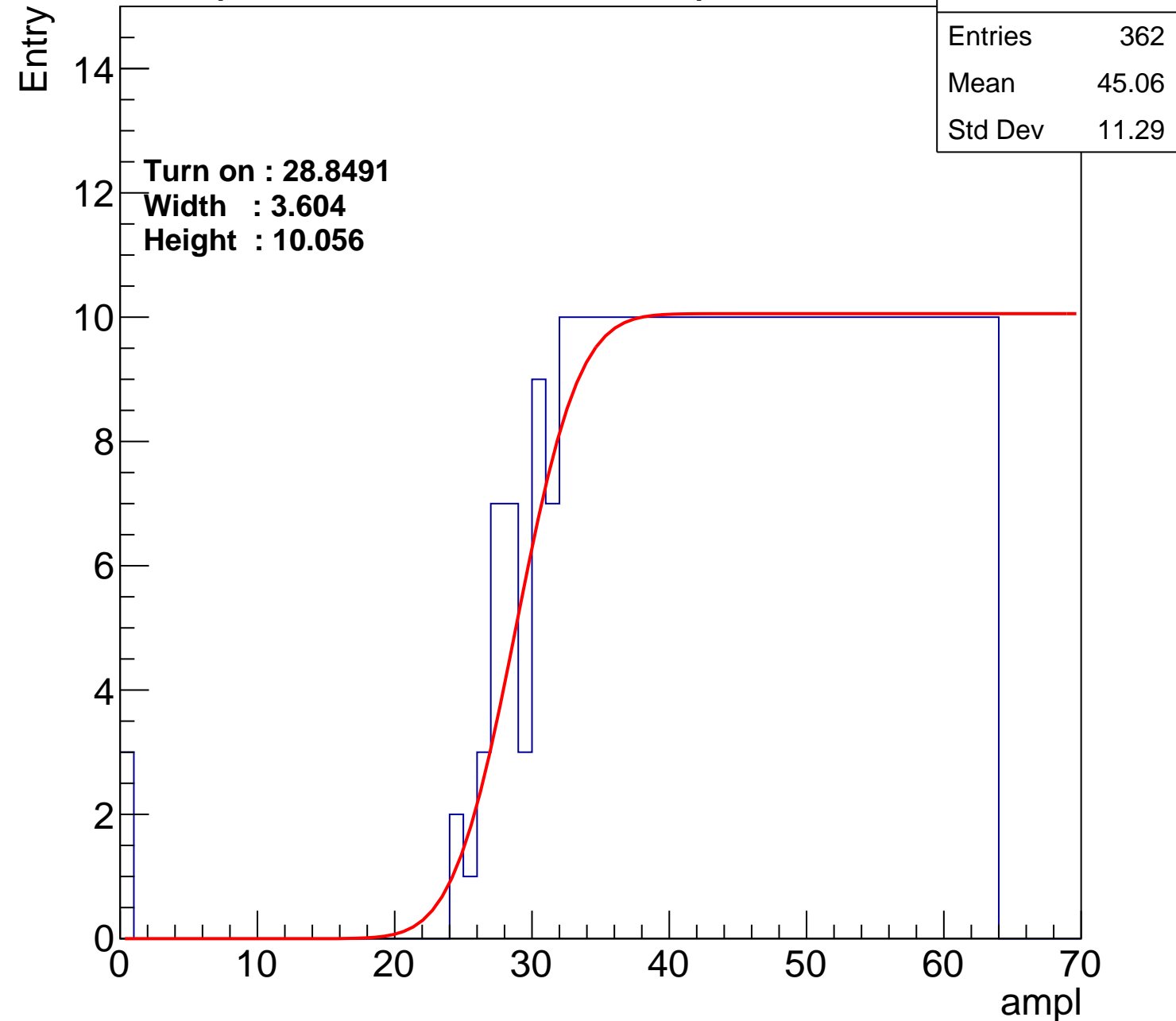
Width : 3.604

Height : 10.056

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L001S, U20-ch127

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	352
Mean	45.6
Std Dev	11.2

Turn on : 29.7080

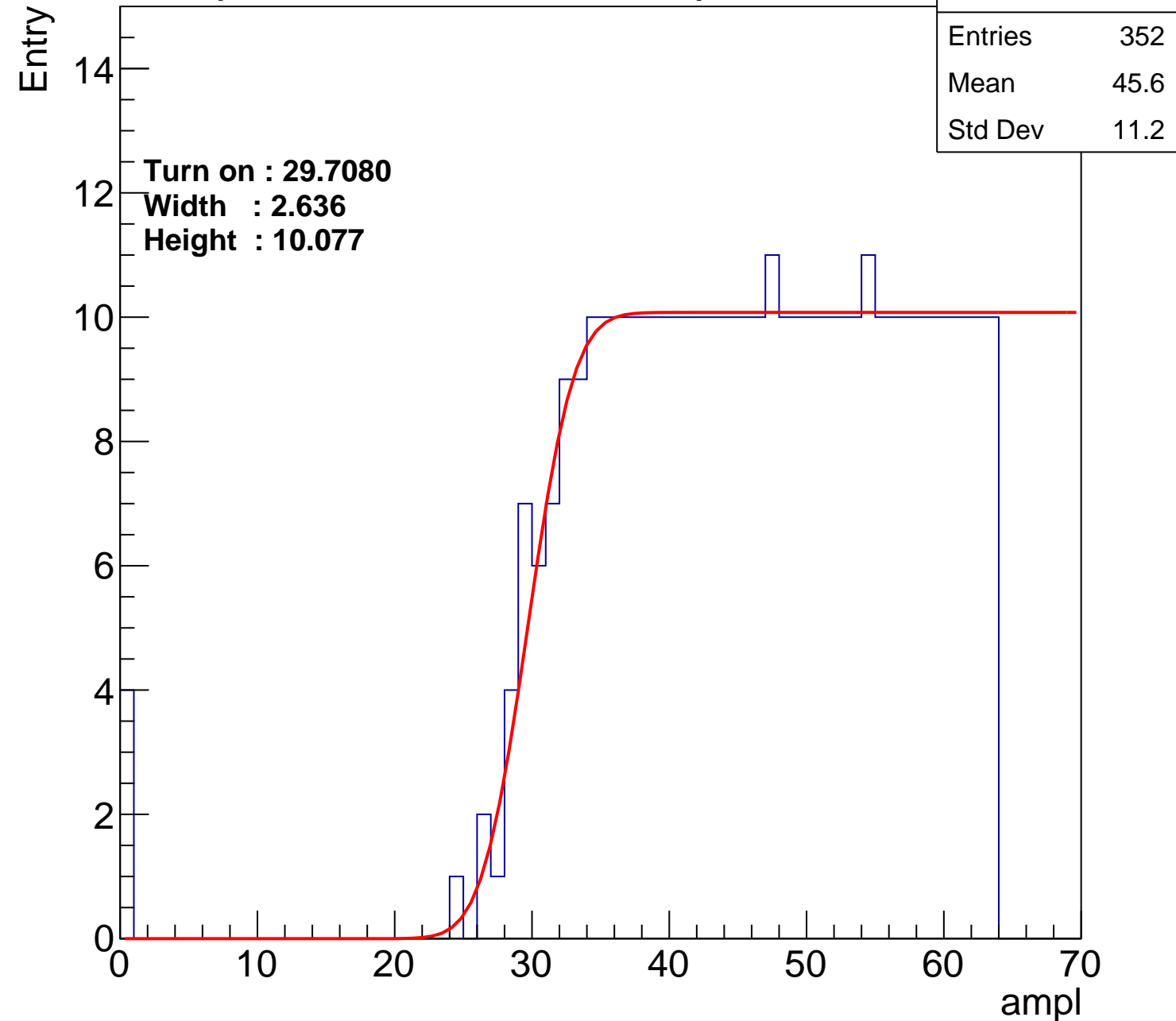
Width : 2.636

Height : 10.077

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U20-ch127

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	352
Mean	45.6
Std Dev	11.2

**Turn on : 29.7080**

**Width : 2.636**

**Height : 10.077**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl

