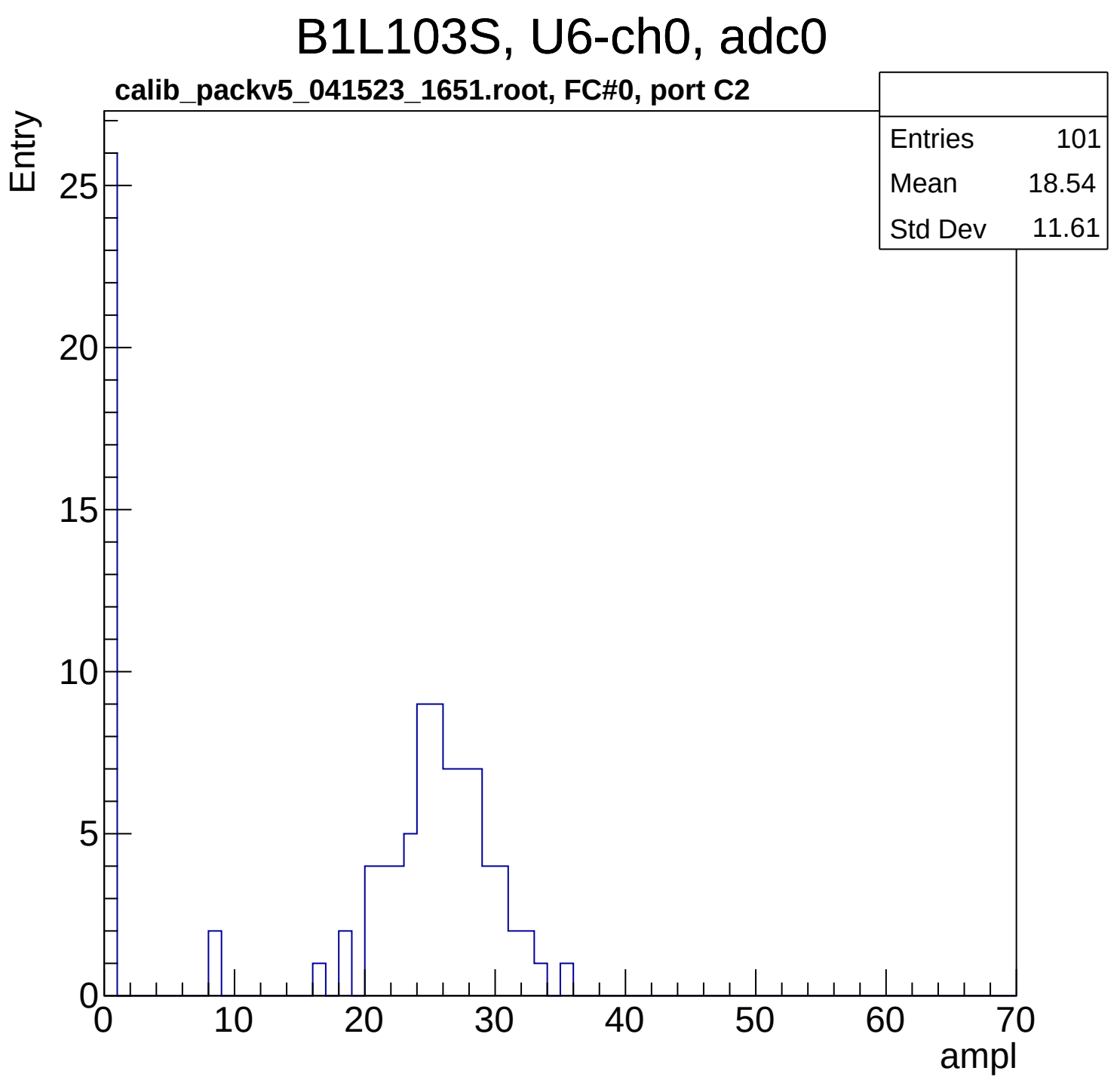
B1L103S, U6-ch0, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 101
Mean 18.54
Std Dev 11.61
Entry
0
5
10
15
20
25
0
10
20
30
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50
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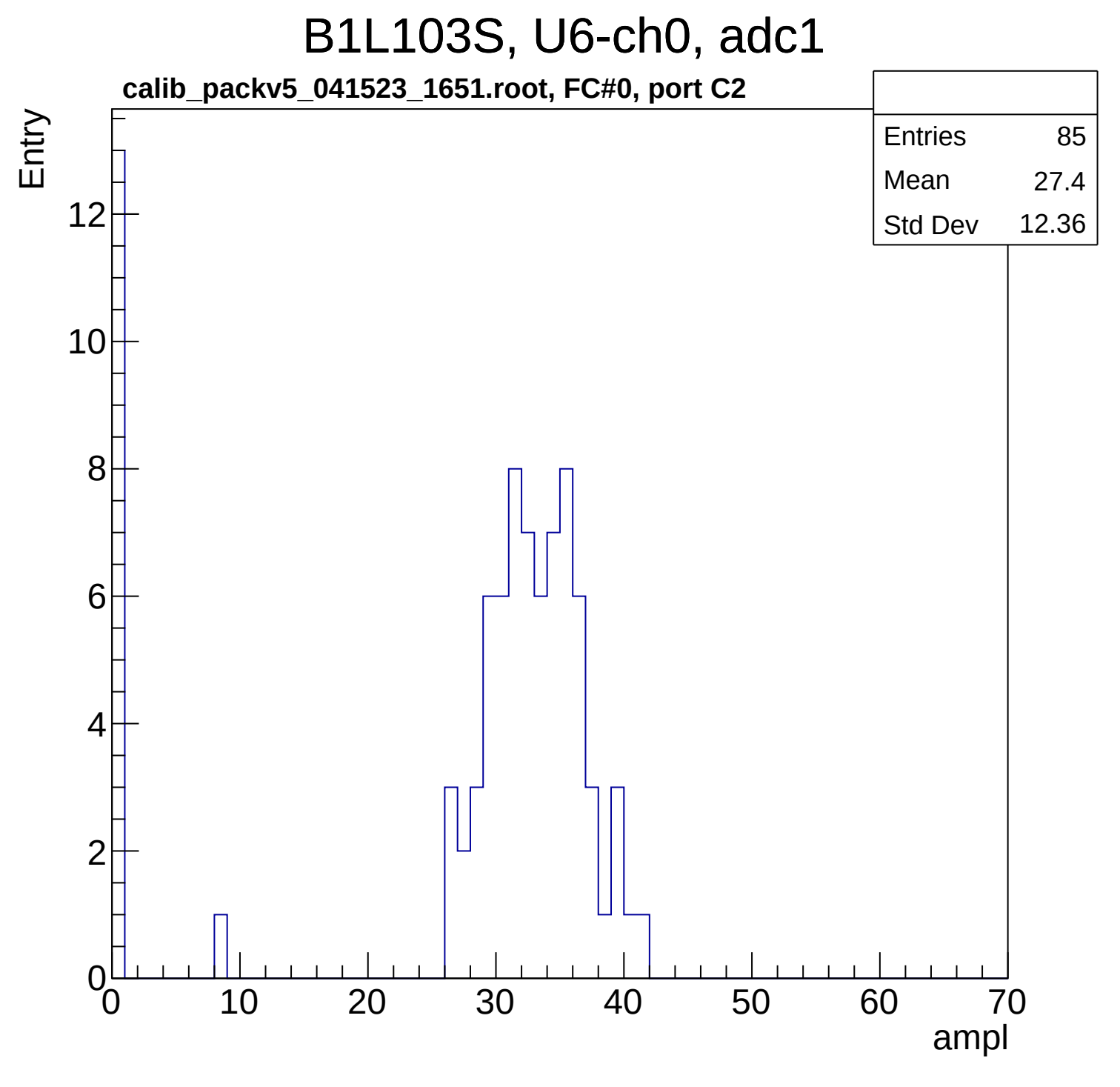
70
ampl


B1L103S, U6-ch0, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 27.4
Std Dev 12.36
Entry
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2
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8
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12
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10
20
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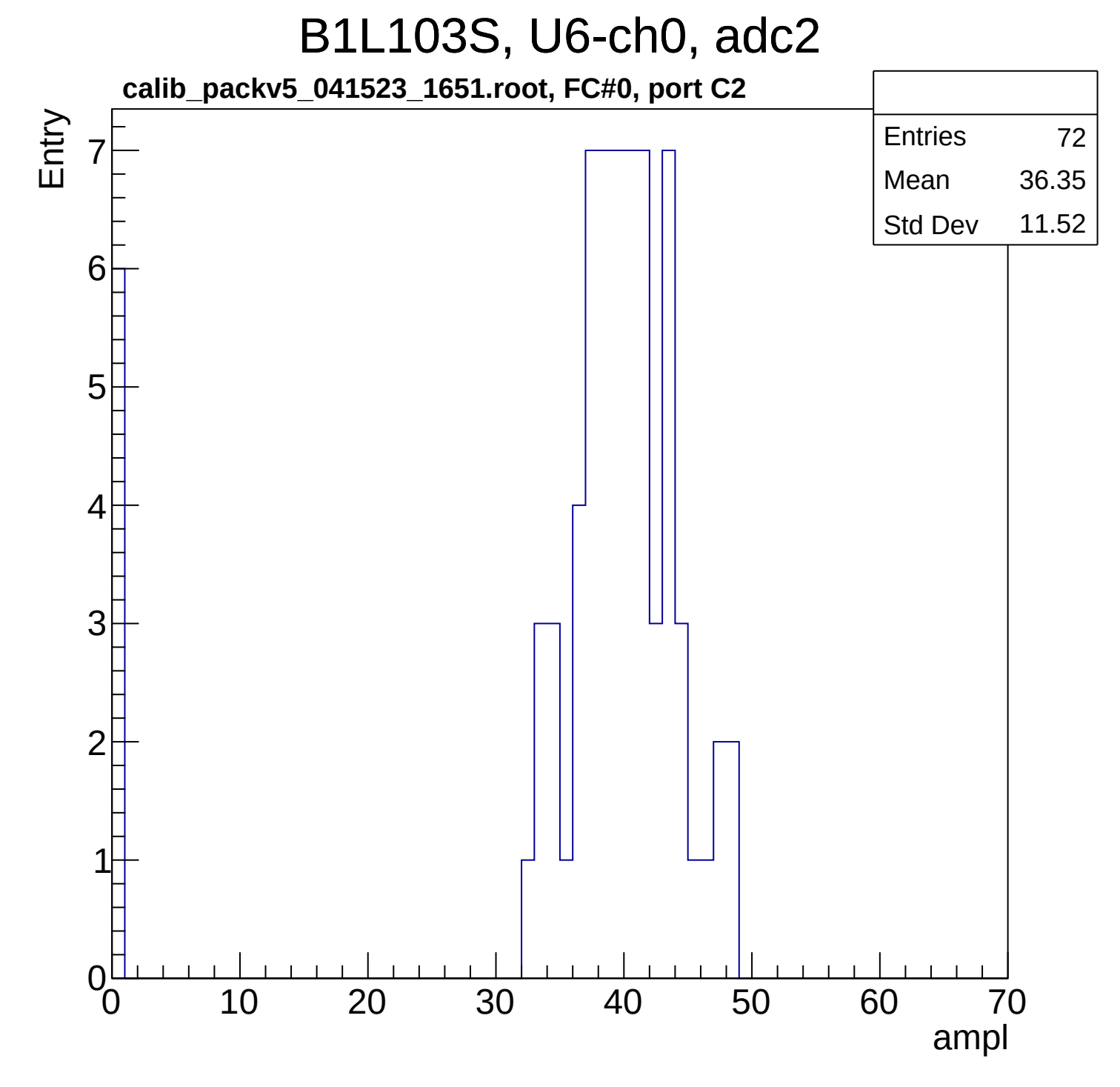
70
ampl


B1L103S, U6-ch0, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 36.35
Std Dev 11.52
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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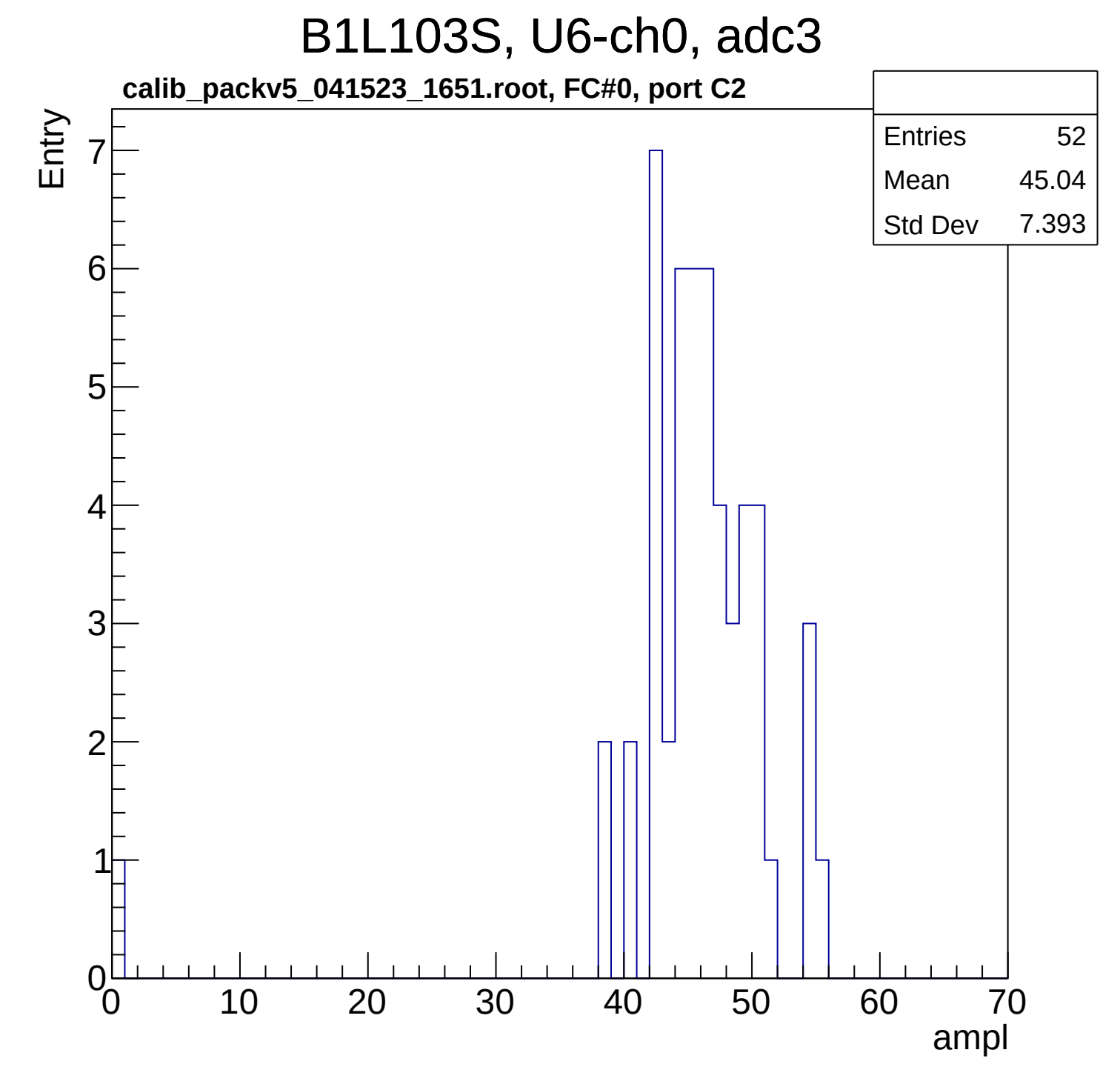
B1L103S, U6-ch0, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 45.04
Std Dev 7.393
Entry
ampl
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7
0
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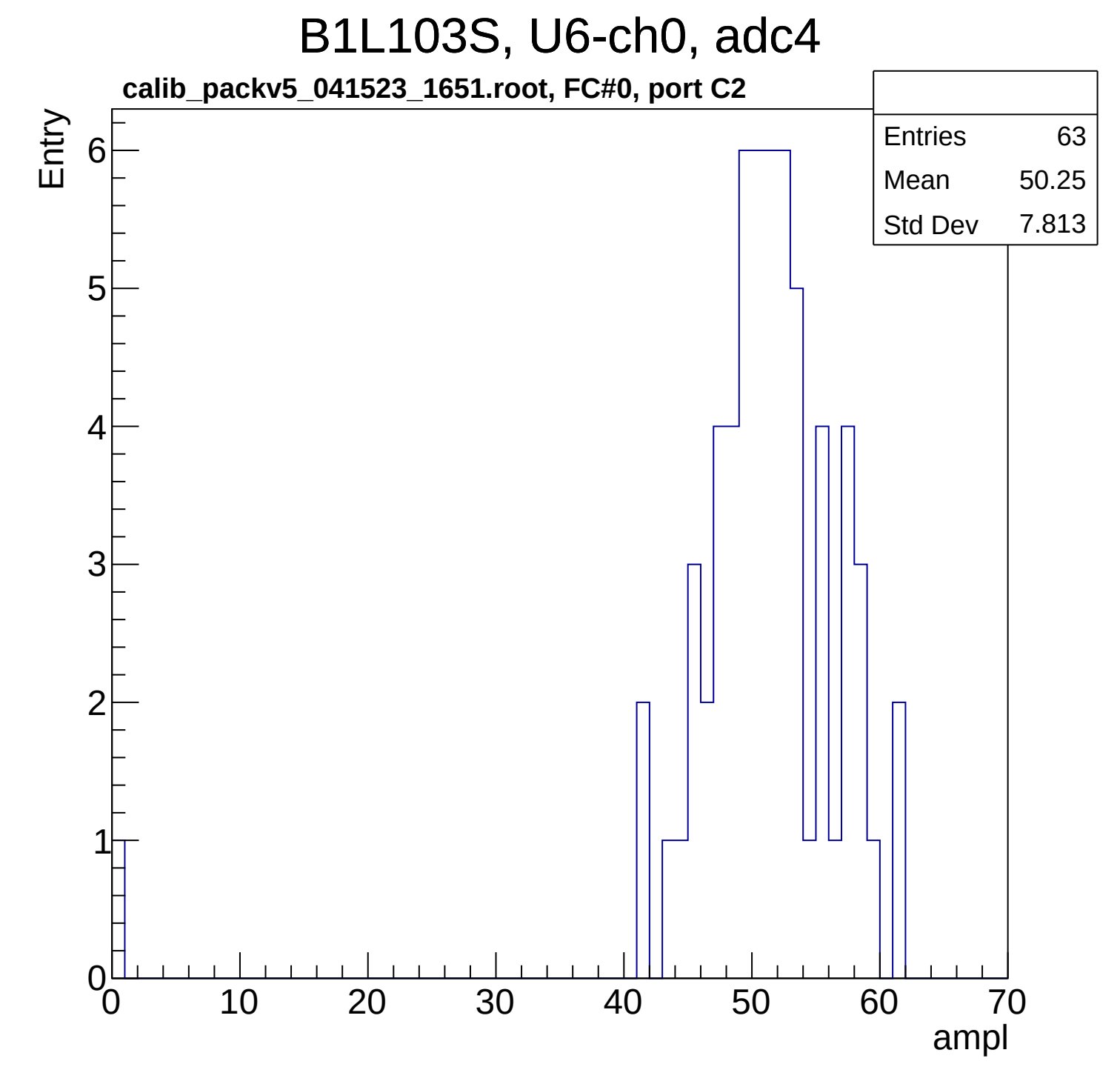
B1L103S, U6-ch0, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 50.25
Std Dev 7.813
Entry
ampl
0
1
2
3
4
5
6
0
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20
30
40
50
60
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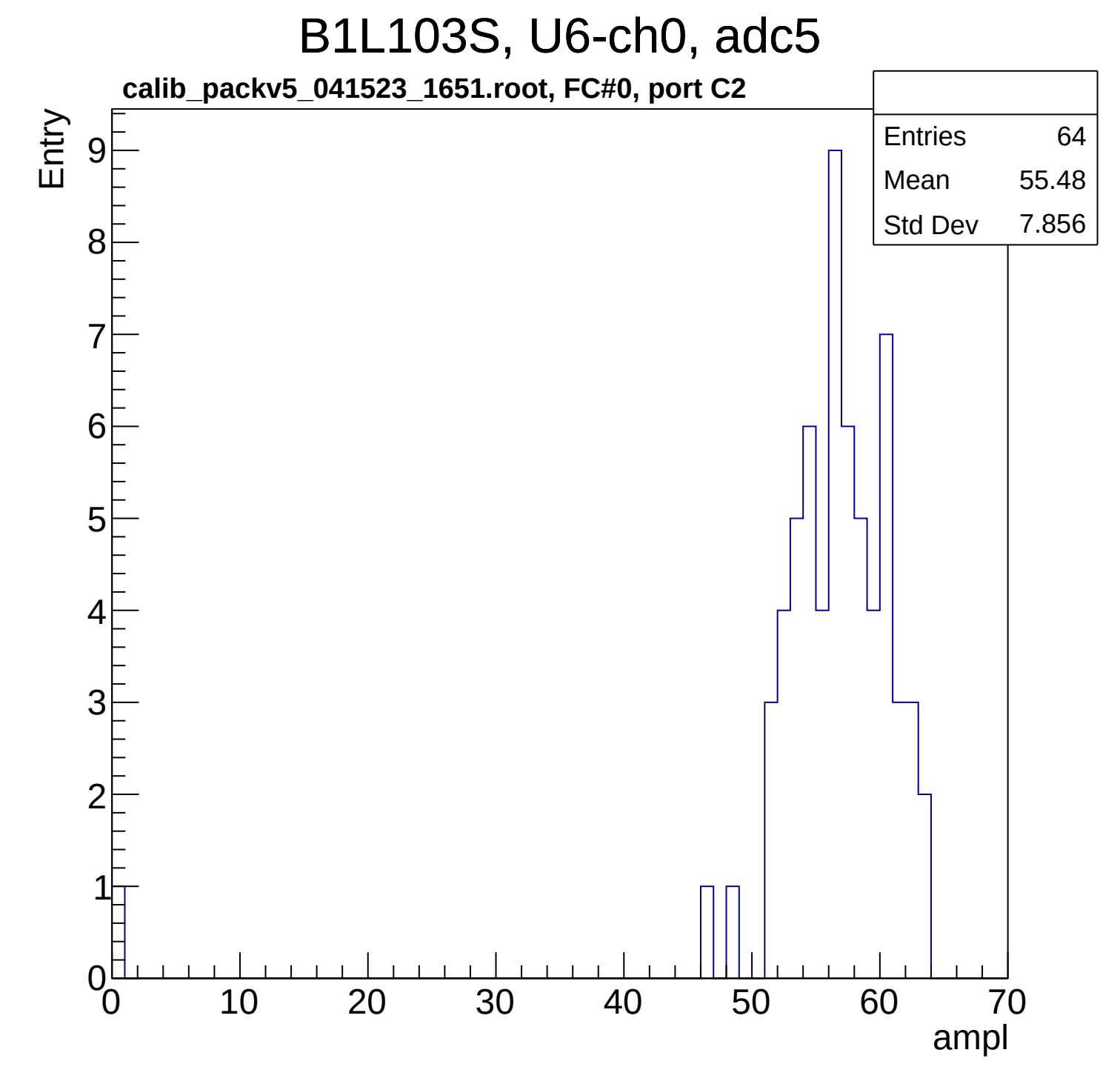
B1L103S, U6-ch0, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 55.48
Std Dev 7.856
Entry
ampl
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2
3
4
5
6
7
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0
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40
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60
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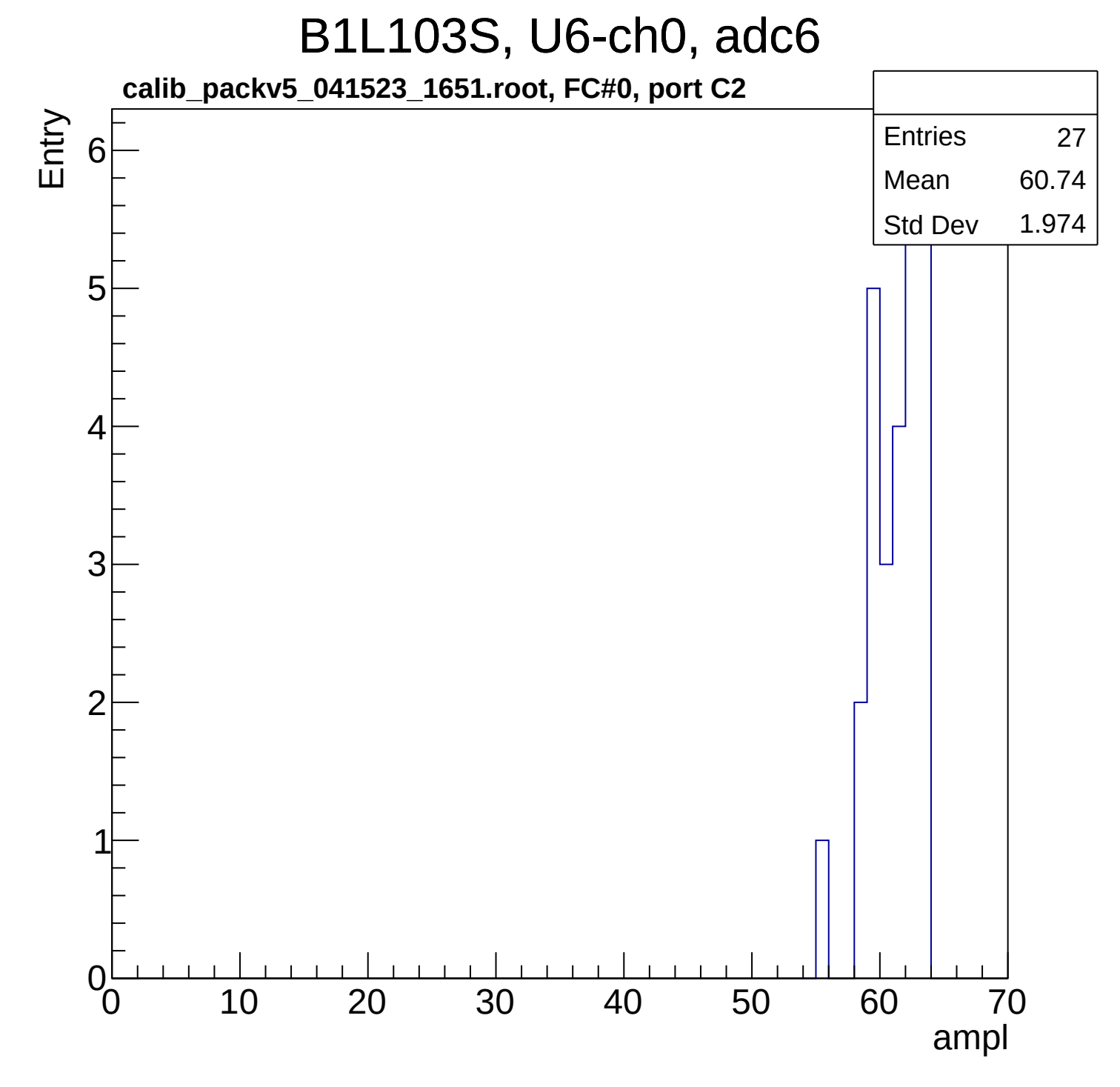
B1L103S, U6-ch0, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 60.74
Std Dev 1.974
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
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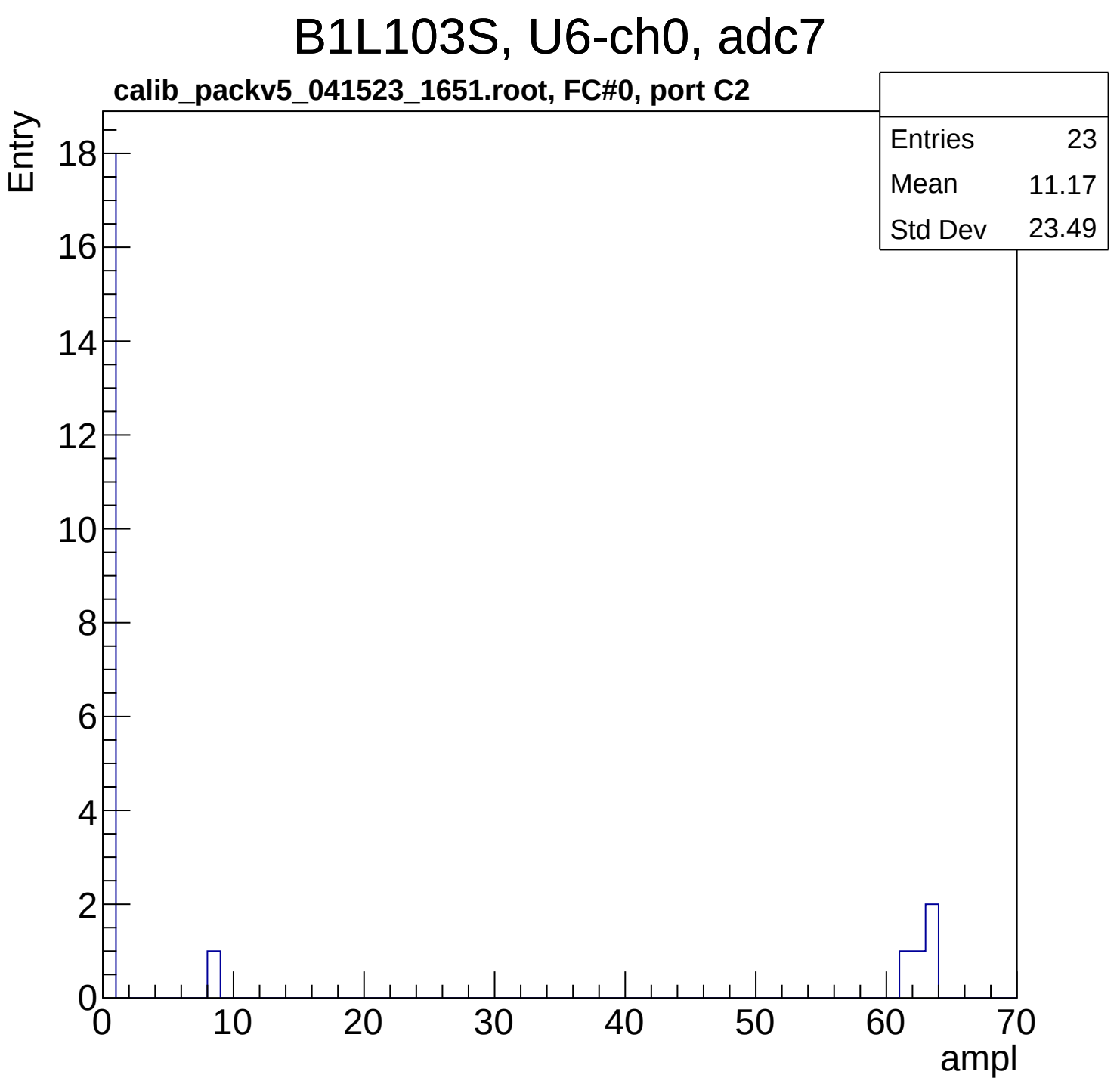
B1L103S, U6-ch0, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 11.17
Std Dev 23.49
Entry
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6
8
10
12
14
16
18
0
10
20
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50
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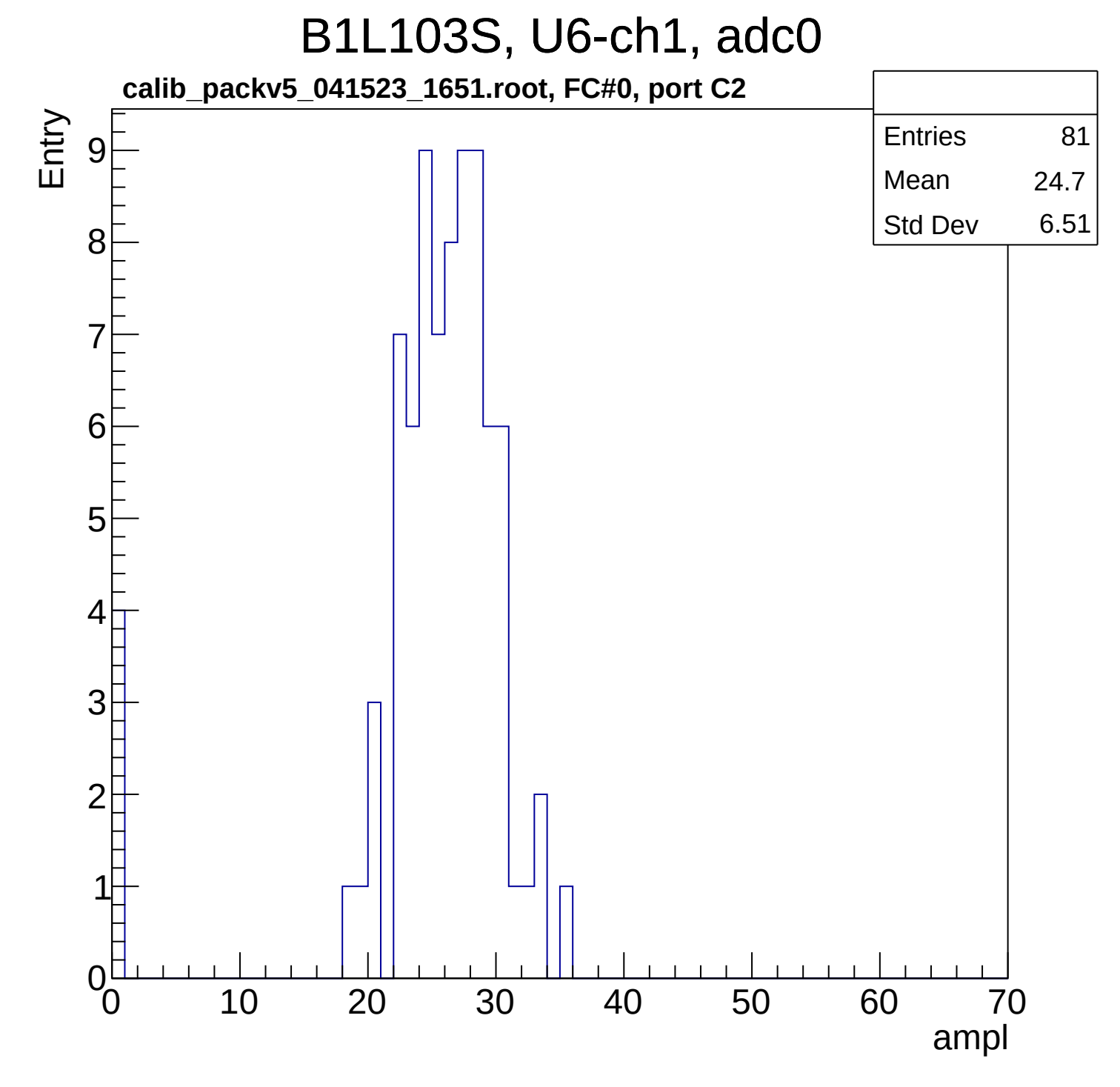
70
ampl


B1L103S, U6-ch1, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 24.7
Std Dev 6.51
Entry
ampl
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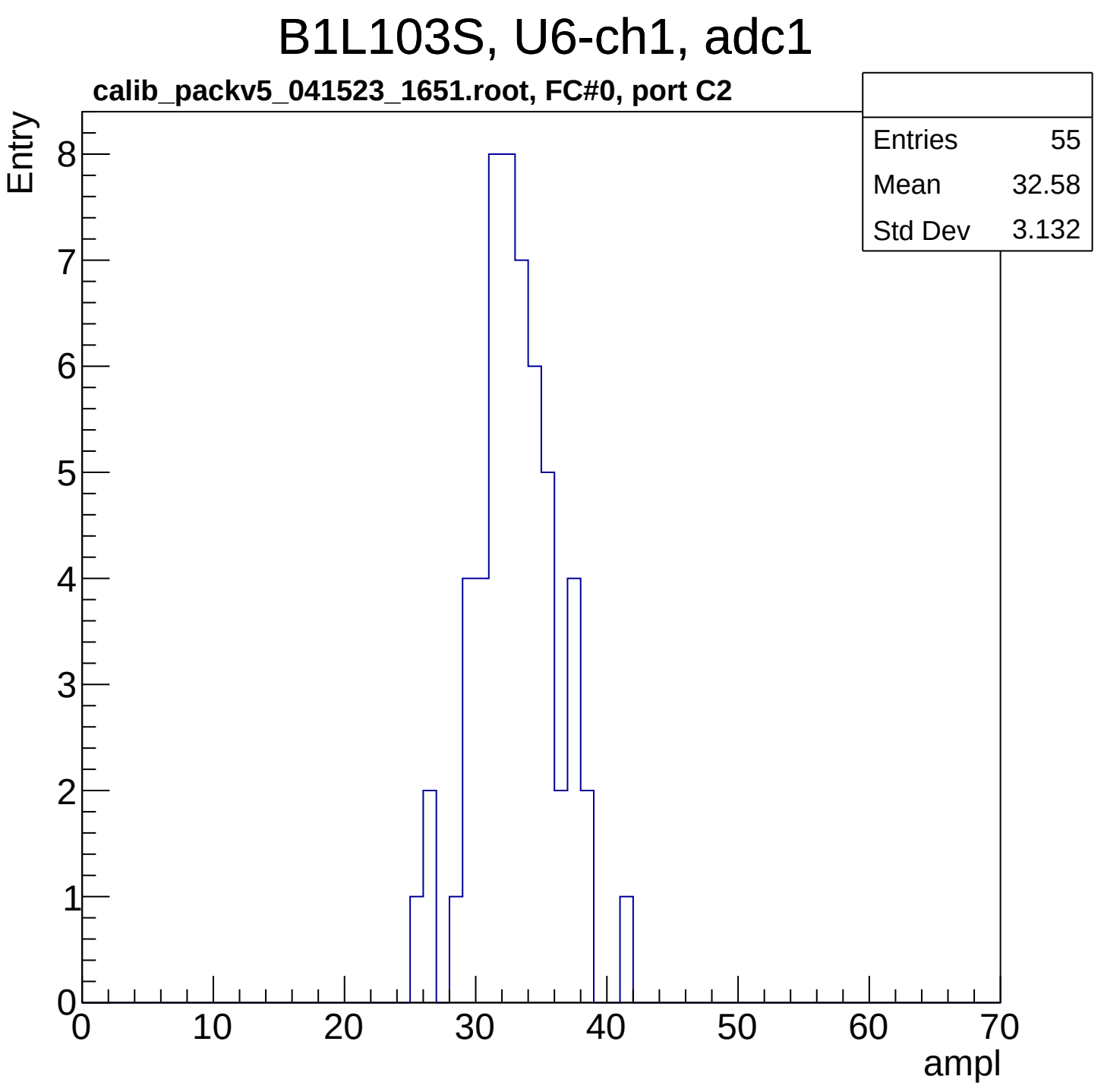
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch1, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 32.58
Std Dev 3.132
Entry
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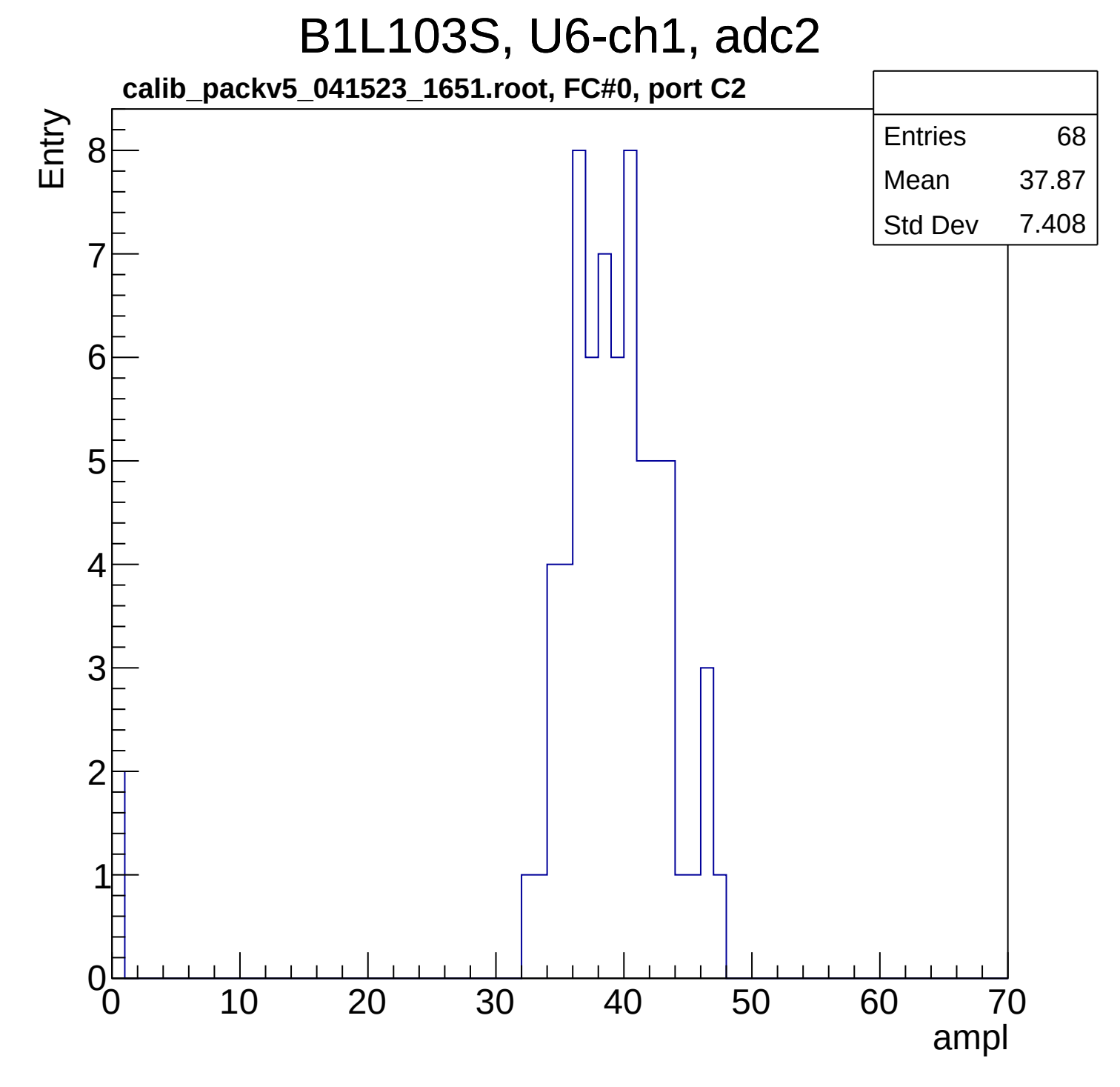
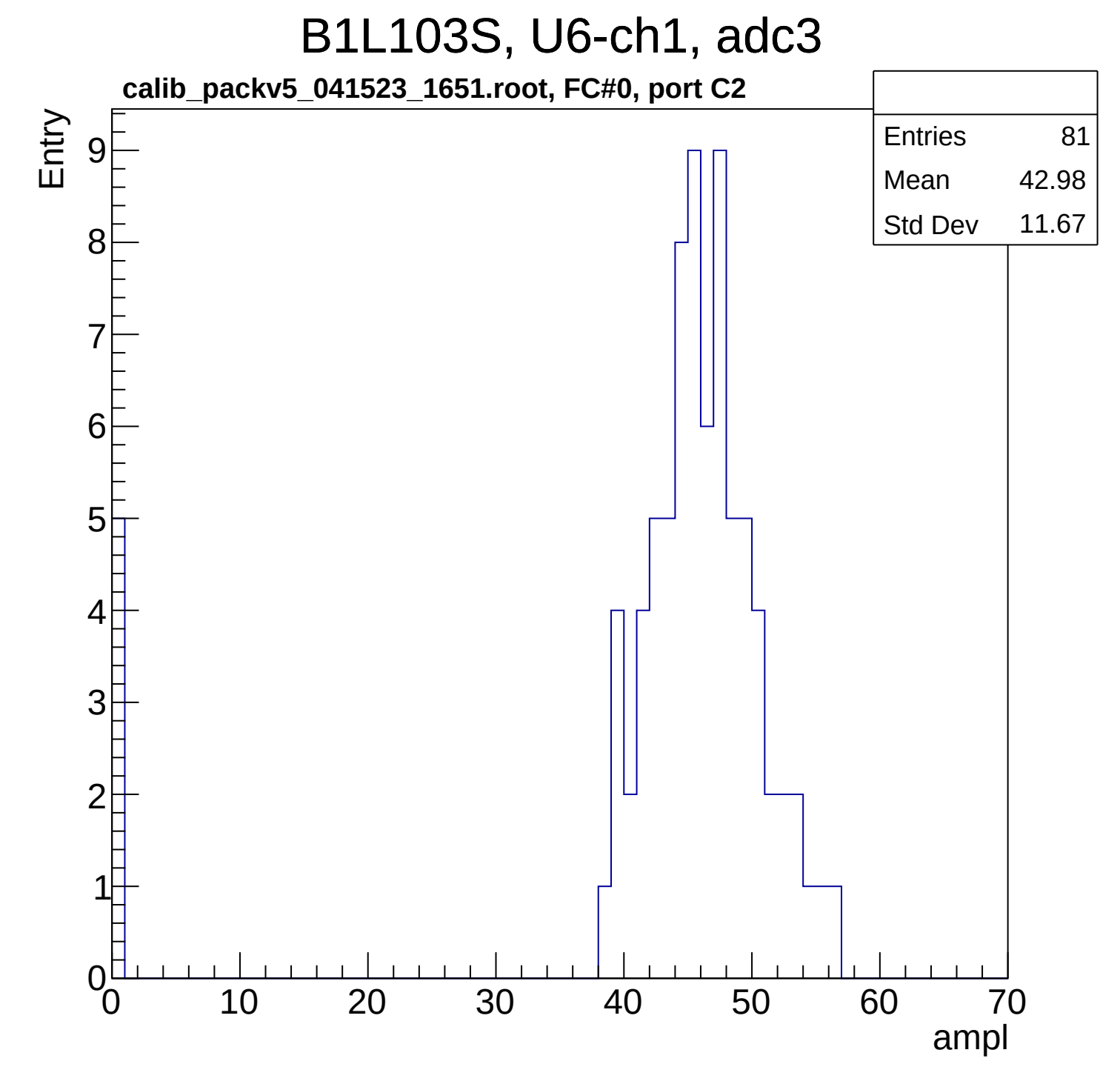
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch1, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 37.87
Std Dev 7.408
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch1, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 42.98
Std Dev 11.67
Entry
ampl
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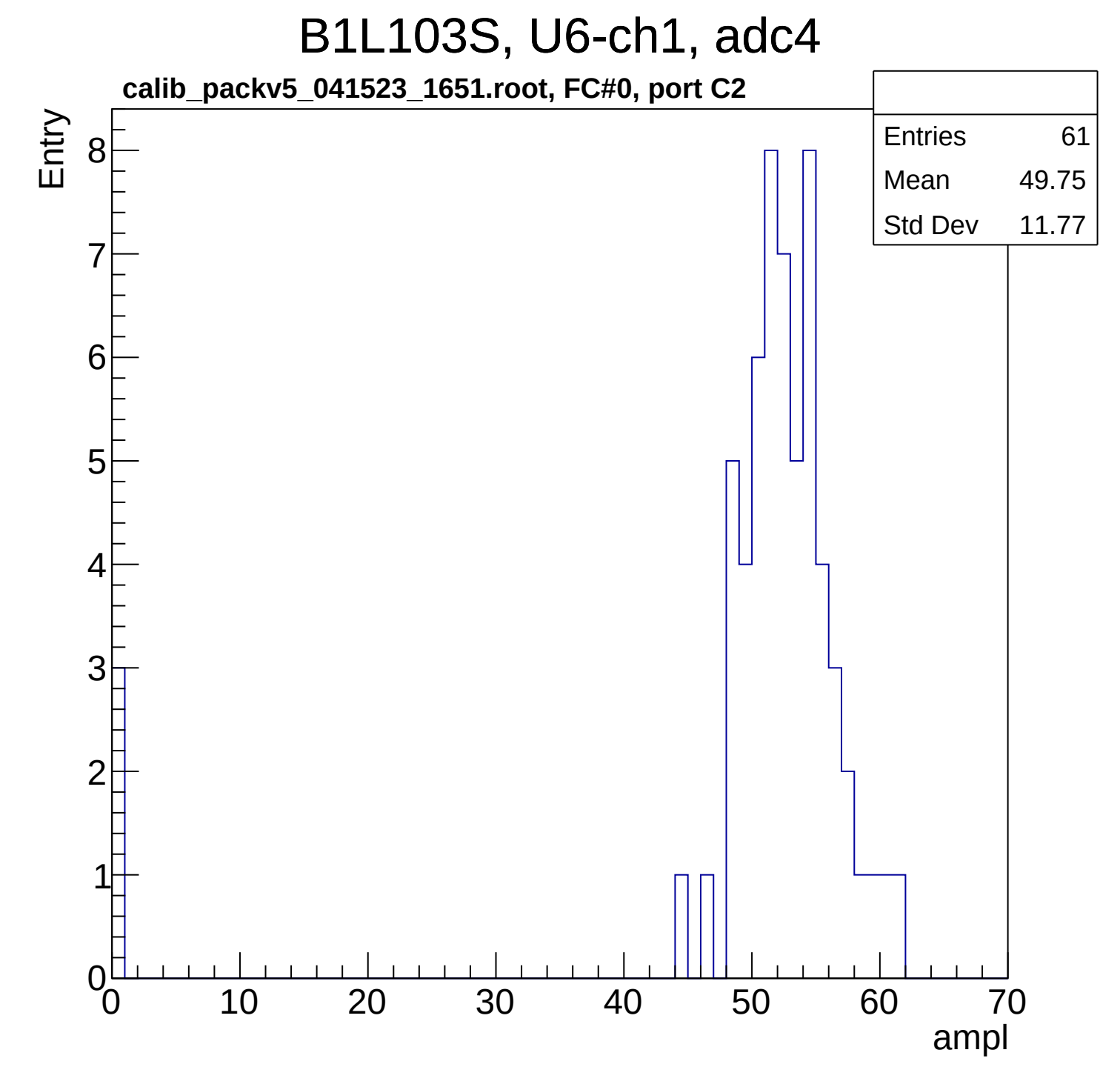
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch1, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 49.75
Std Dev 11.77
Entry
ampl
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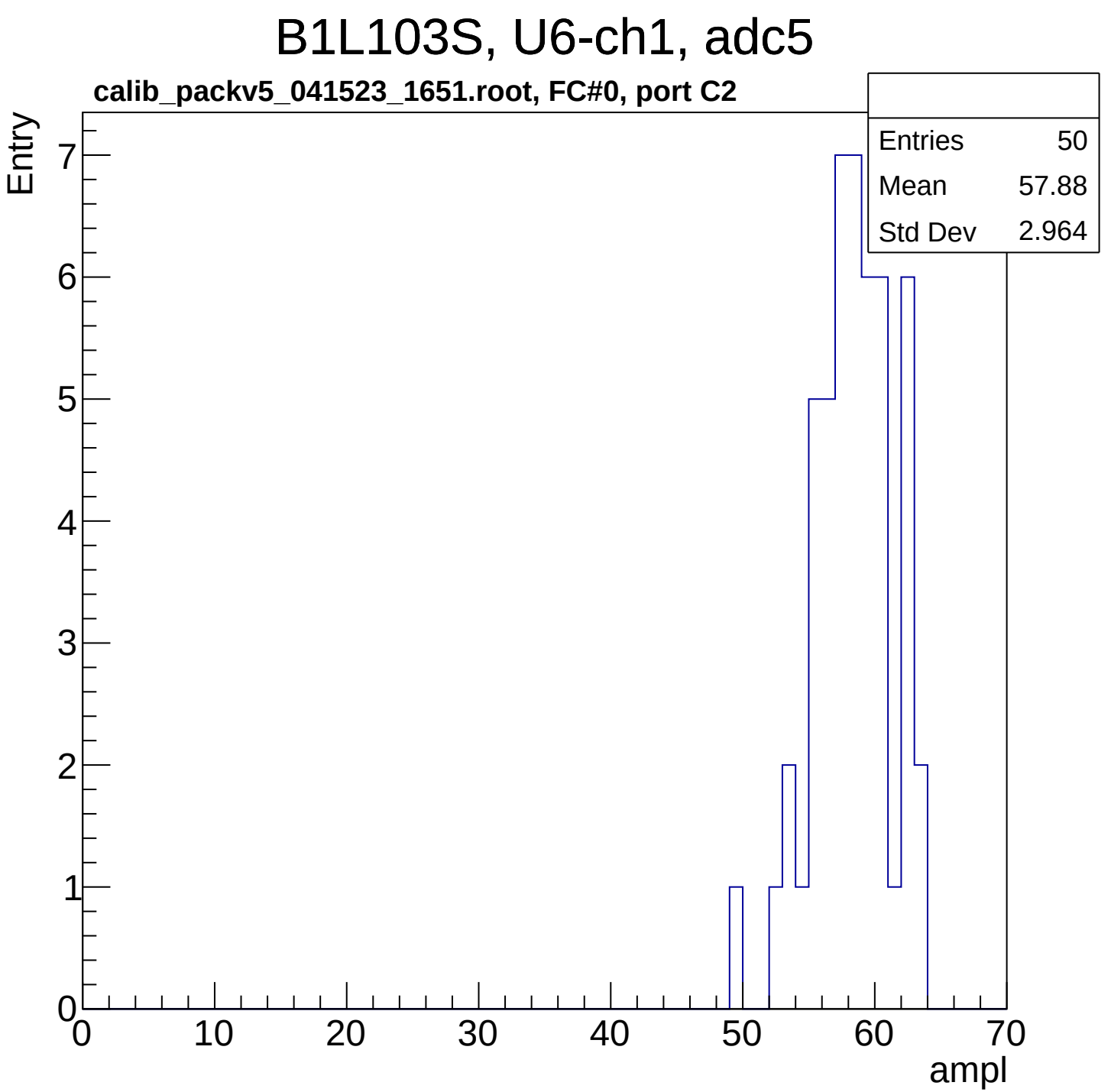
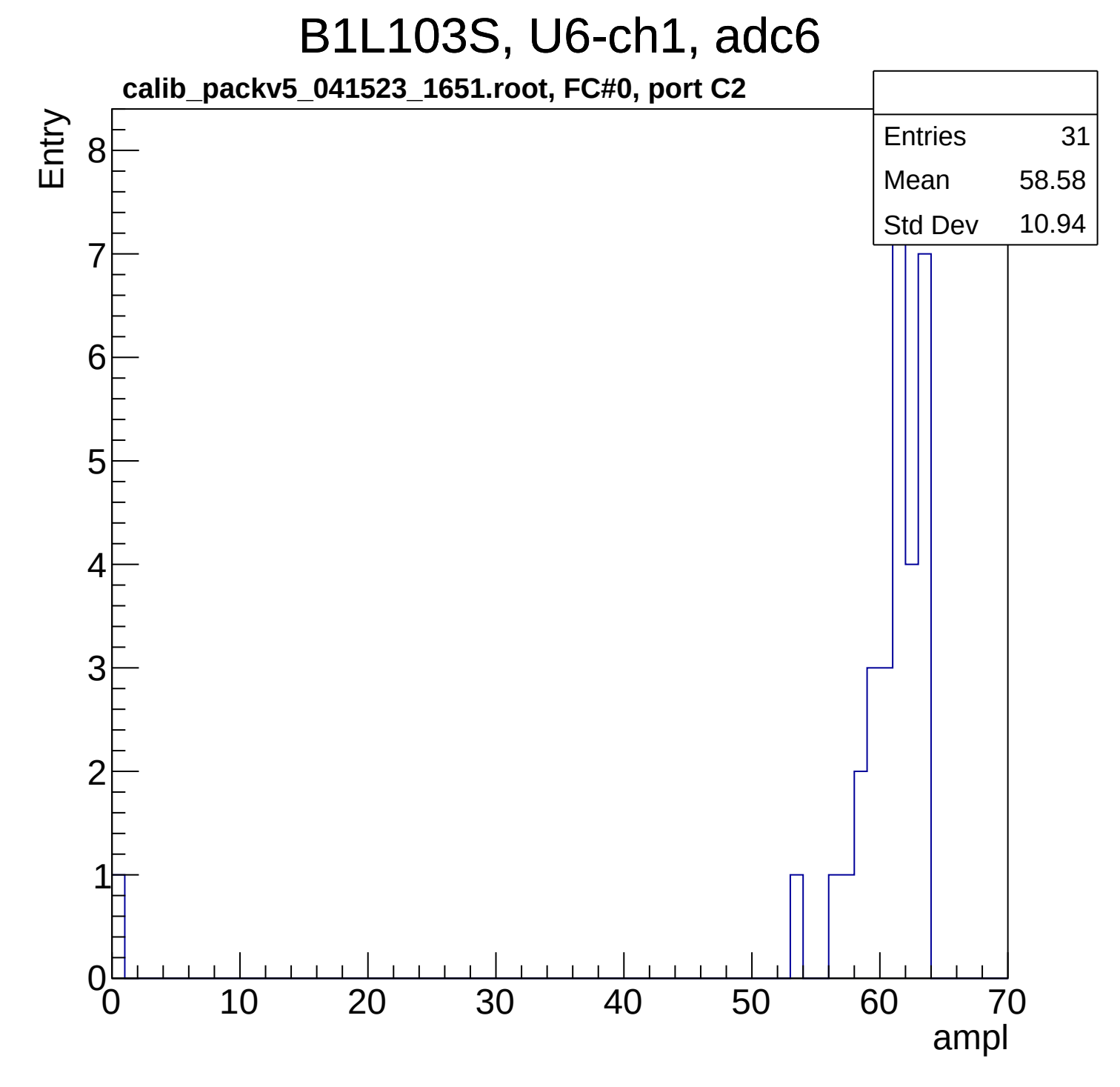
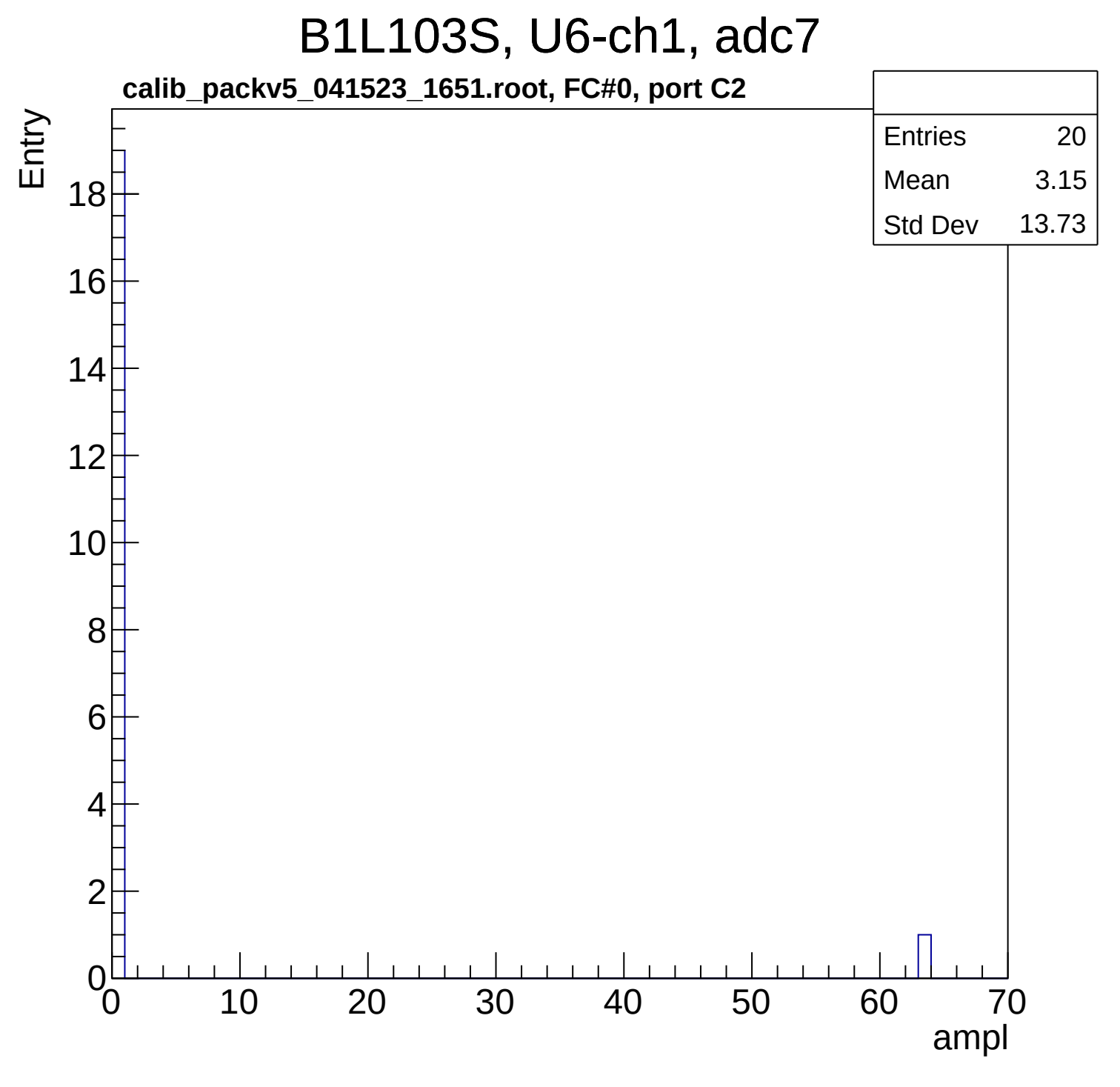
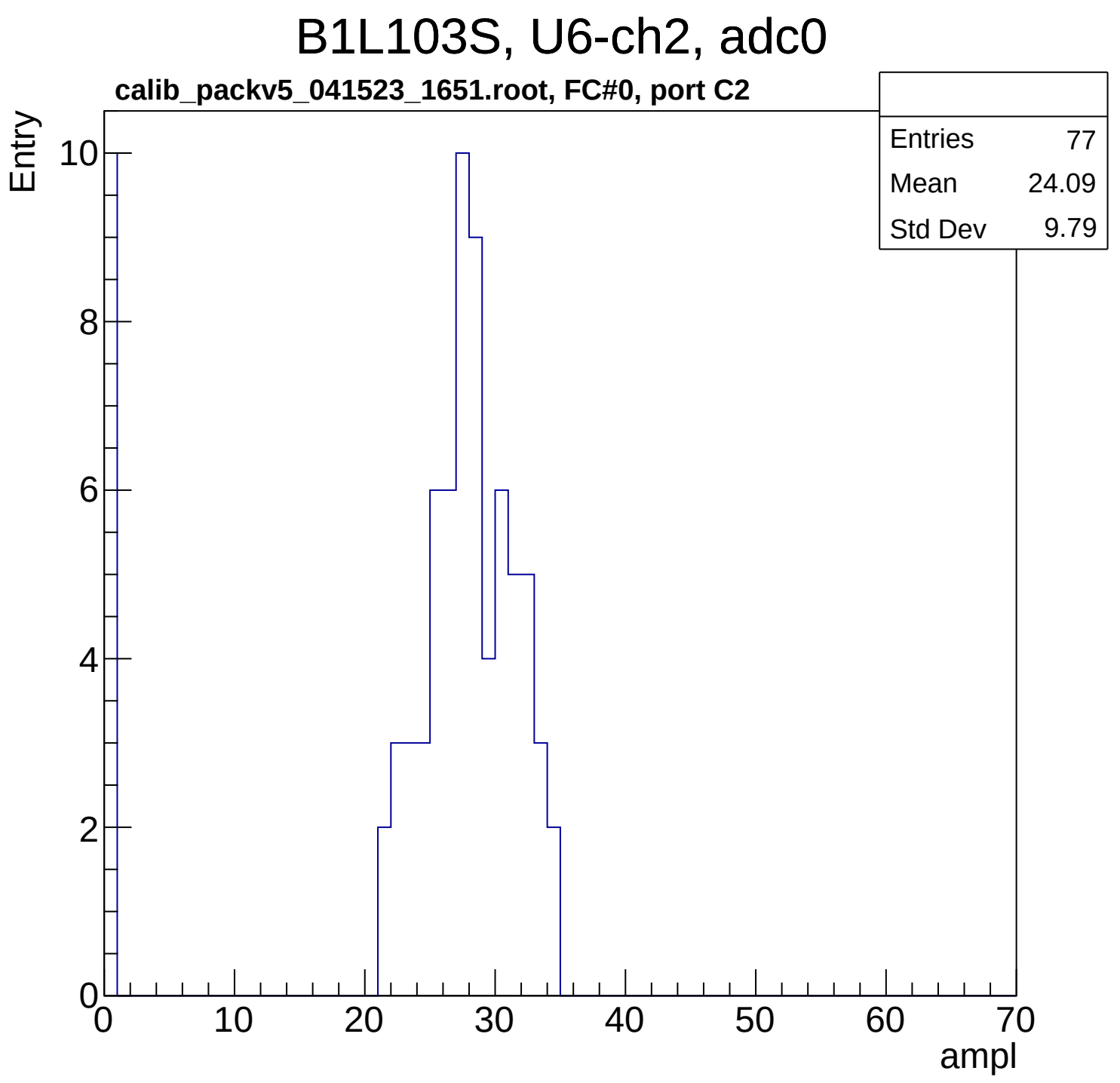
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch1, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 57.88
Std Dev 2.964
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U6-ch1, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 58.58
Std Dev 10.94
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch1, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch2, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 24.09
Std Dev 9.79
Entry
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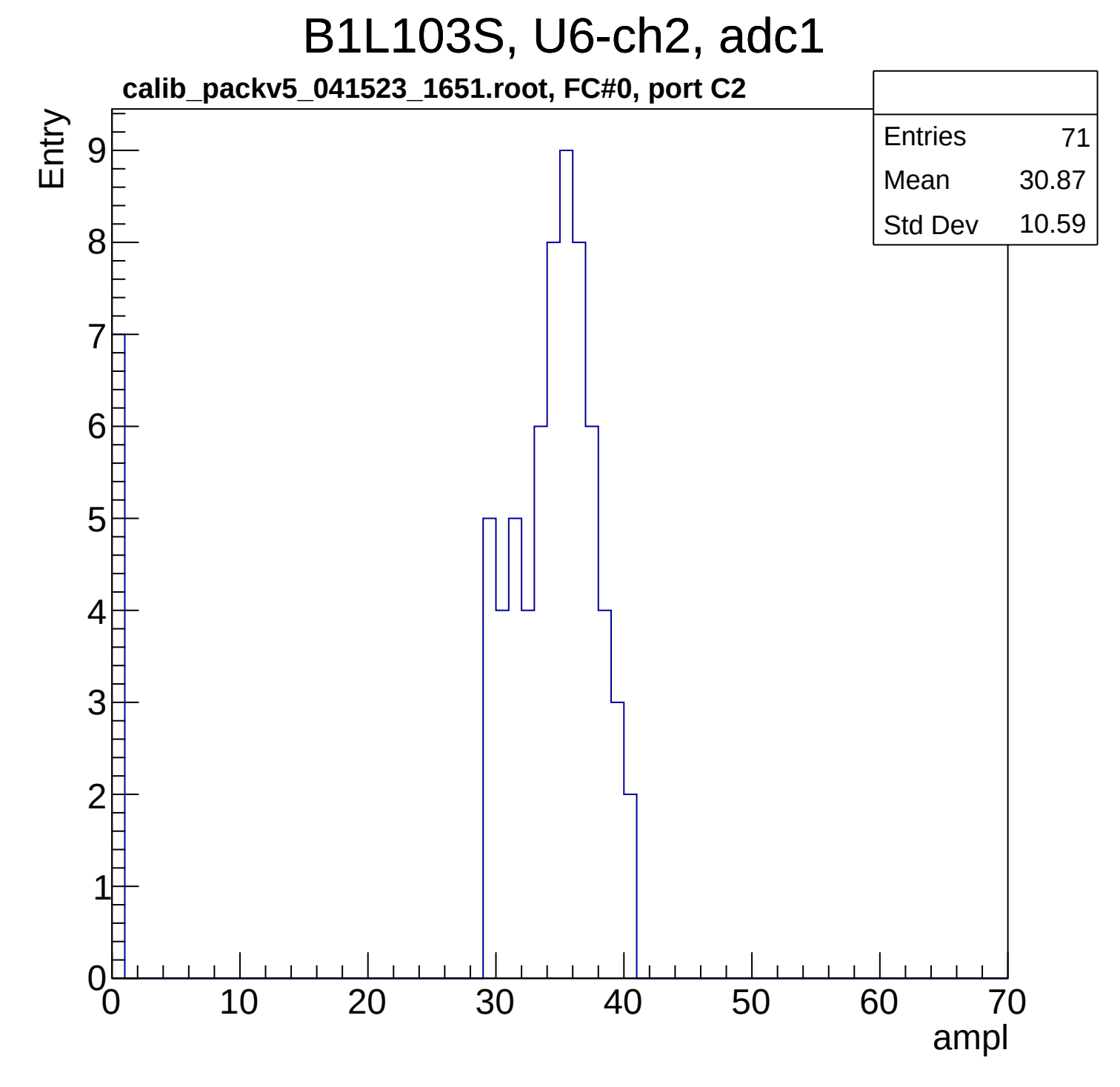
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch2, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 30.87
Std Dev 10.59
Entry
ampl
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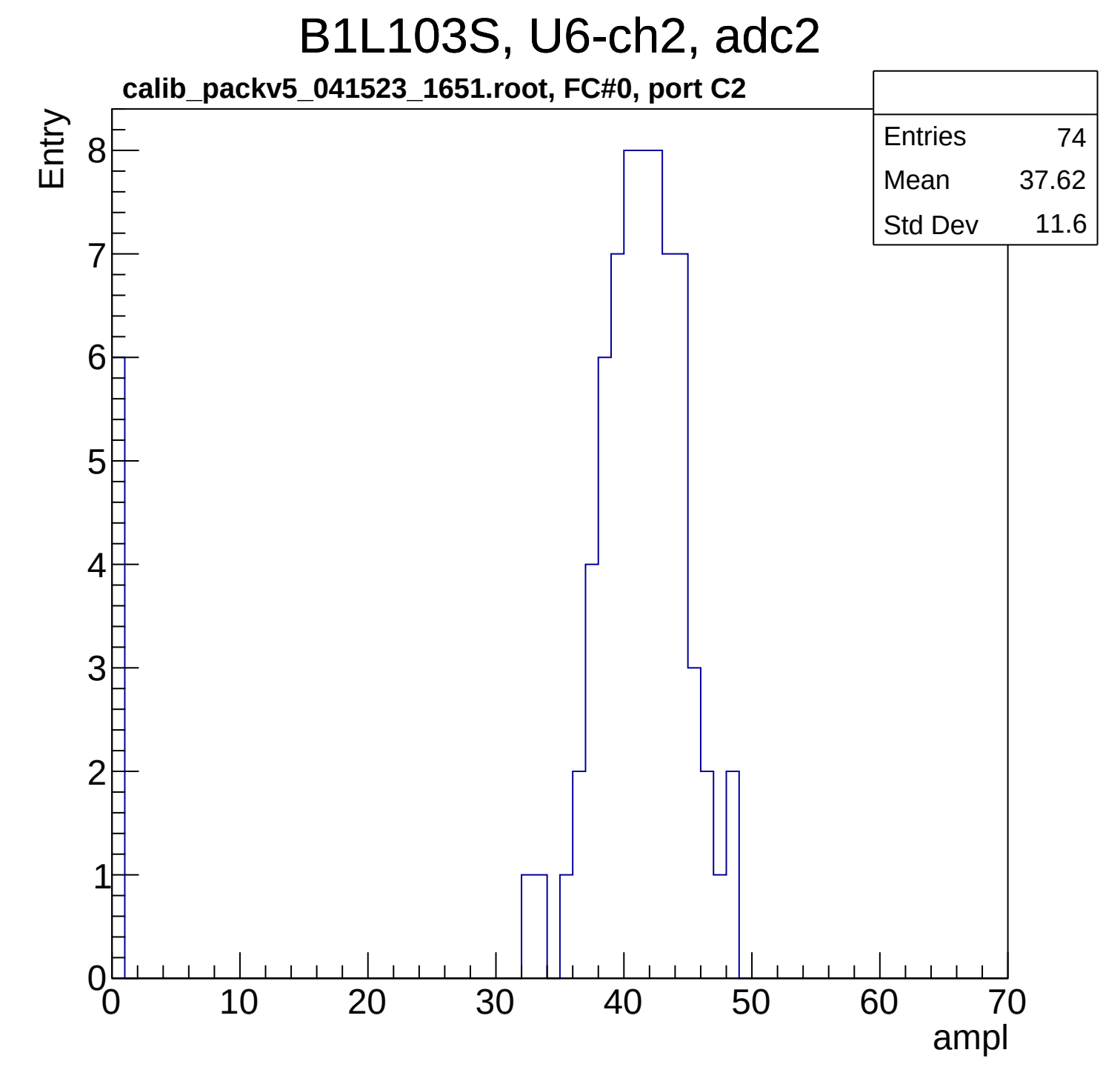
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch2, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 37.62
Std Dev 11.6
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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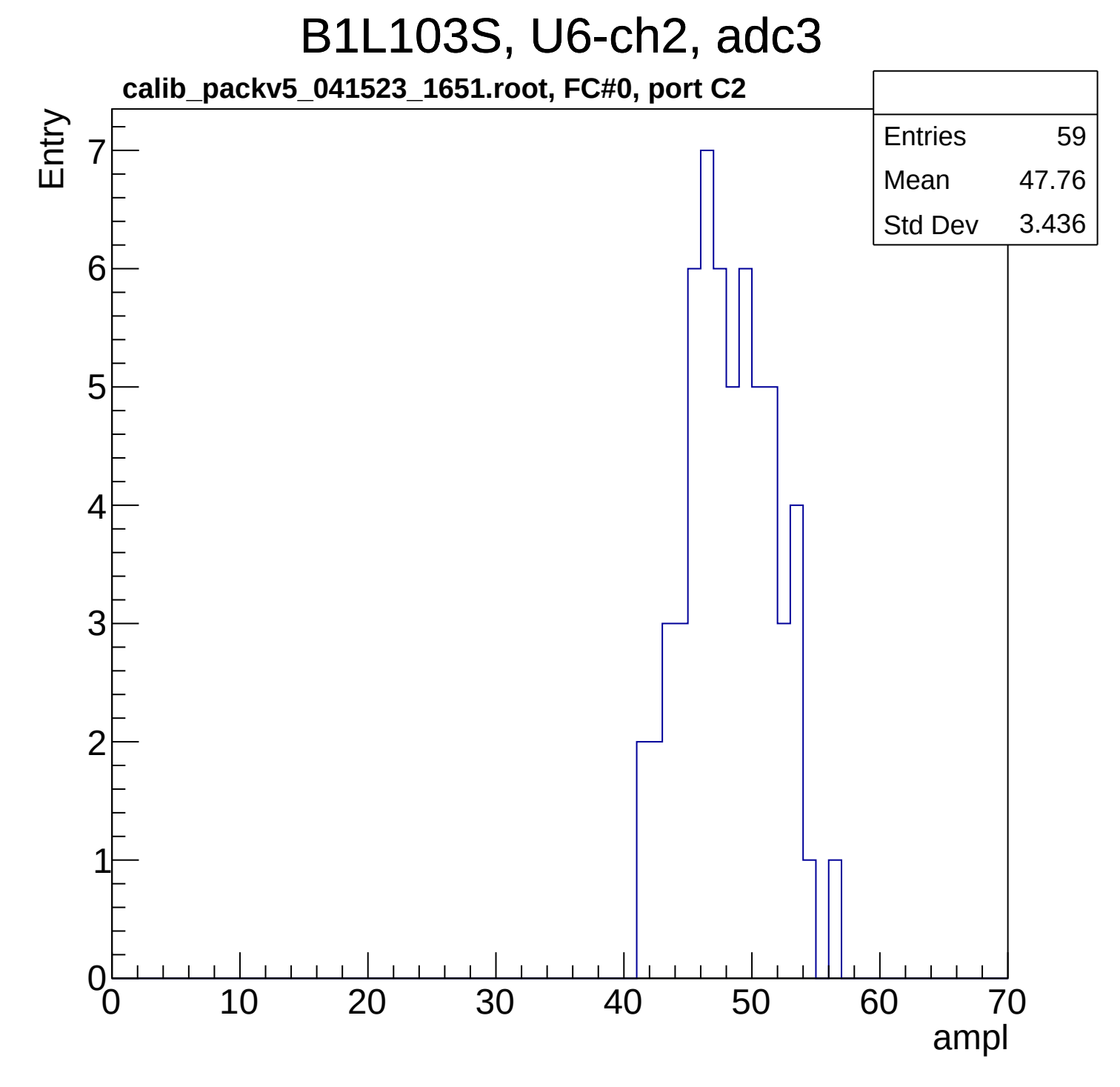
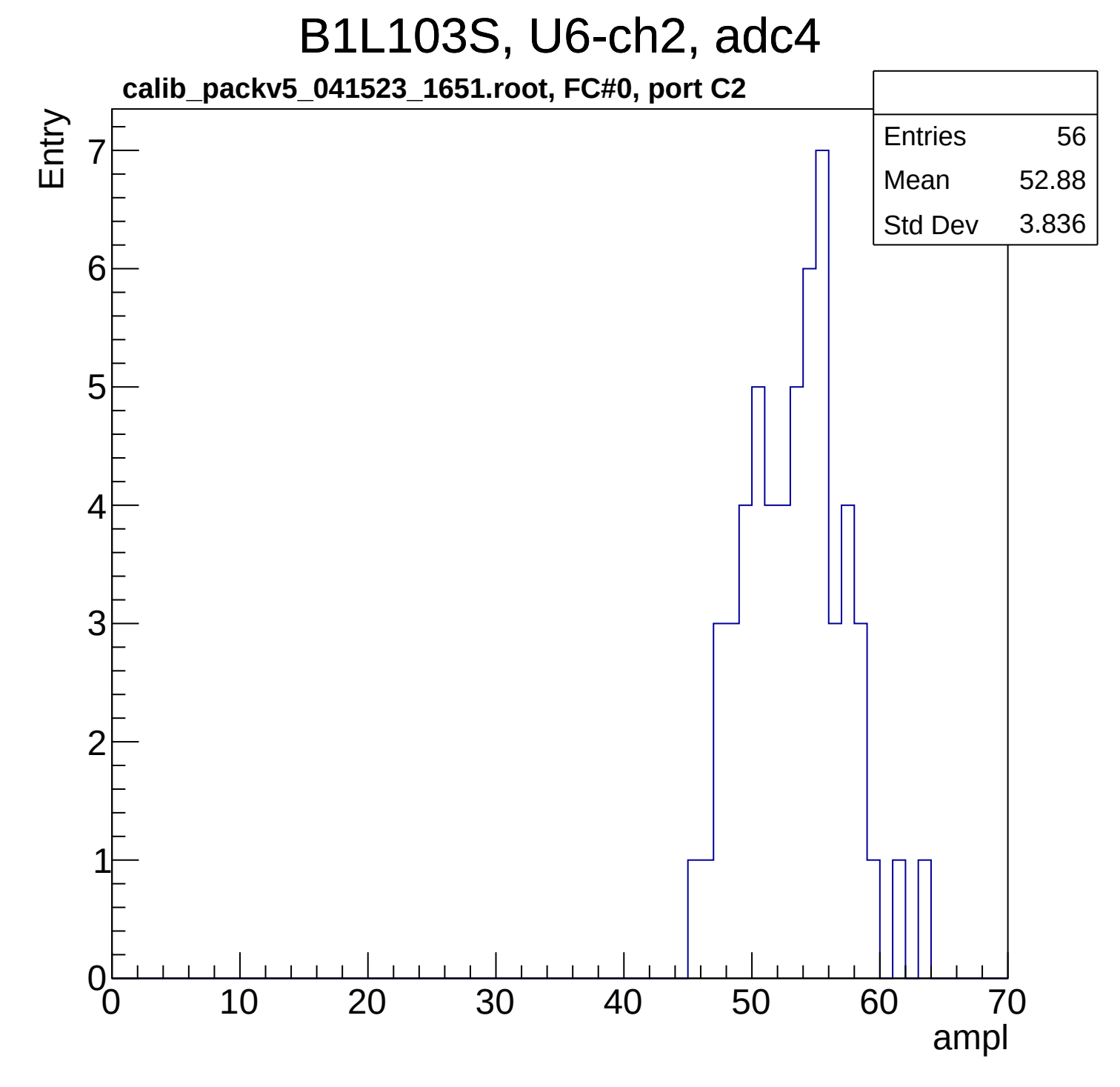

B1L103S, U6-ch2, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 47.76
Std Dev 3.436
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U6-ch2, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 52.88
Std Dev 3.836
Entry
ampl
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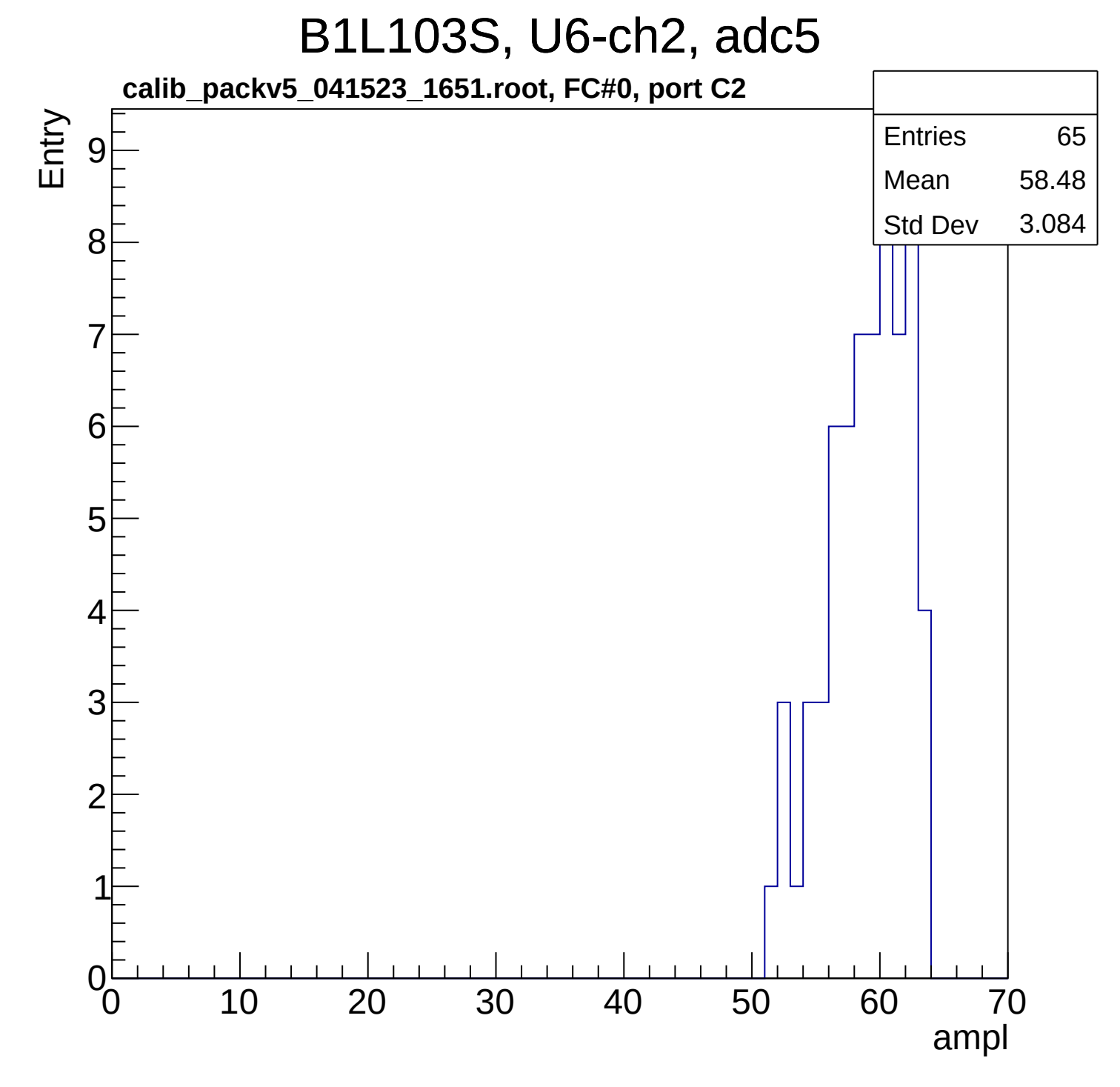
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U6-ch2, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 58.48
Std Dev 3.084
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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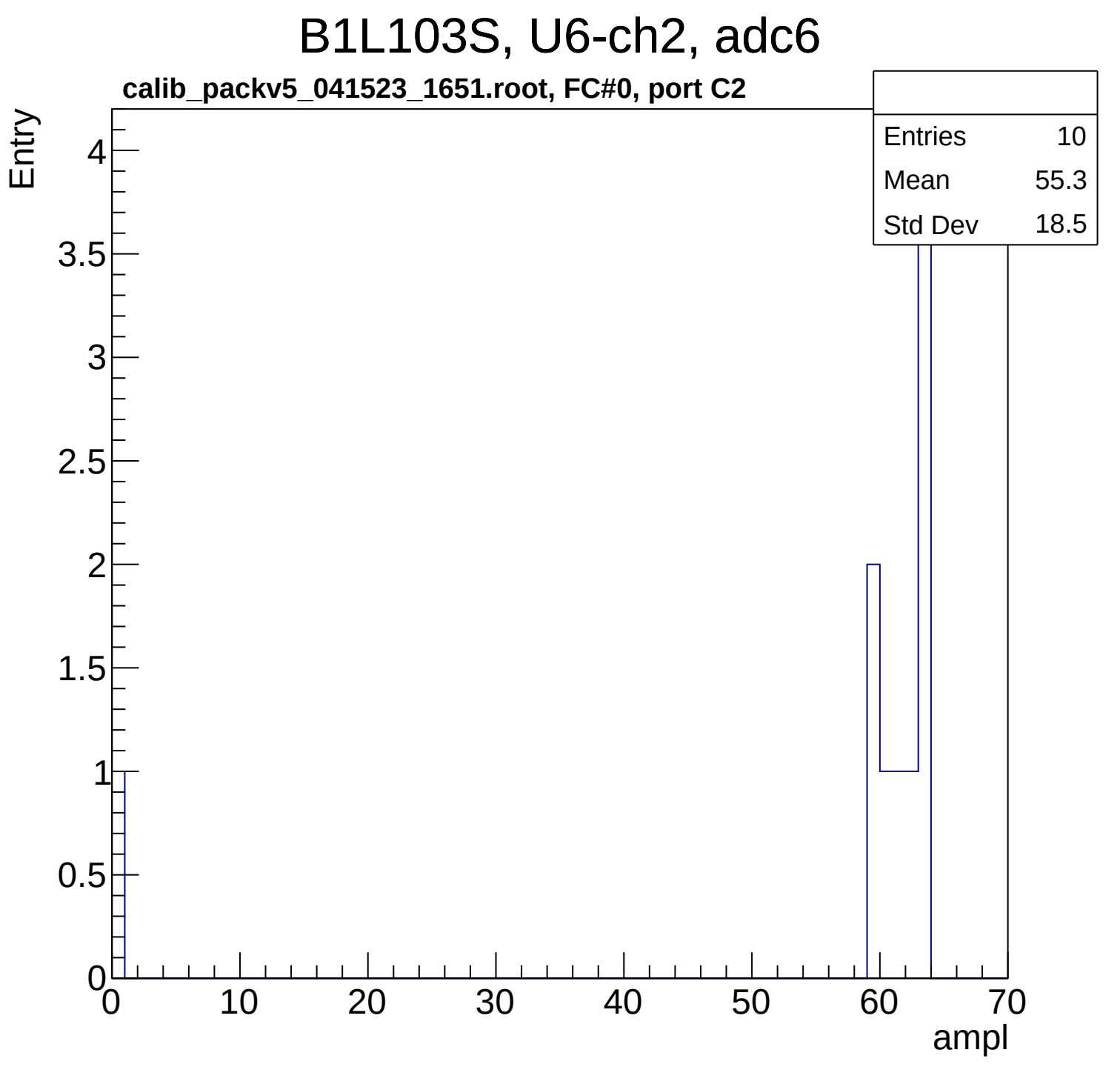
40
50
60
70


B1L103S, U6-ch2, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 55.3
Std Dev 18.5
Entry
ampl
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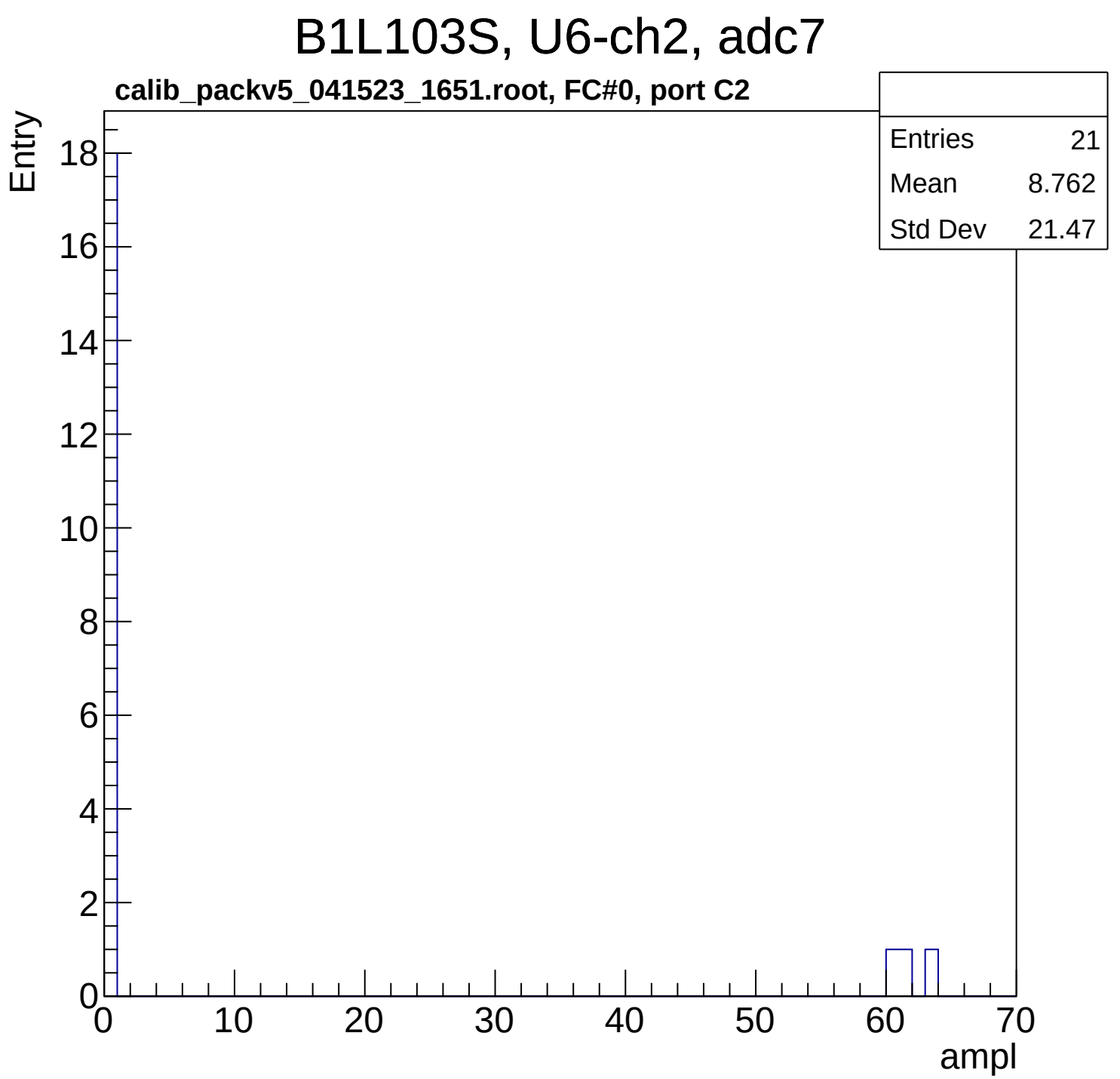
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U6-ch2, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 8.762
Std Dev 21.47
Entry
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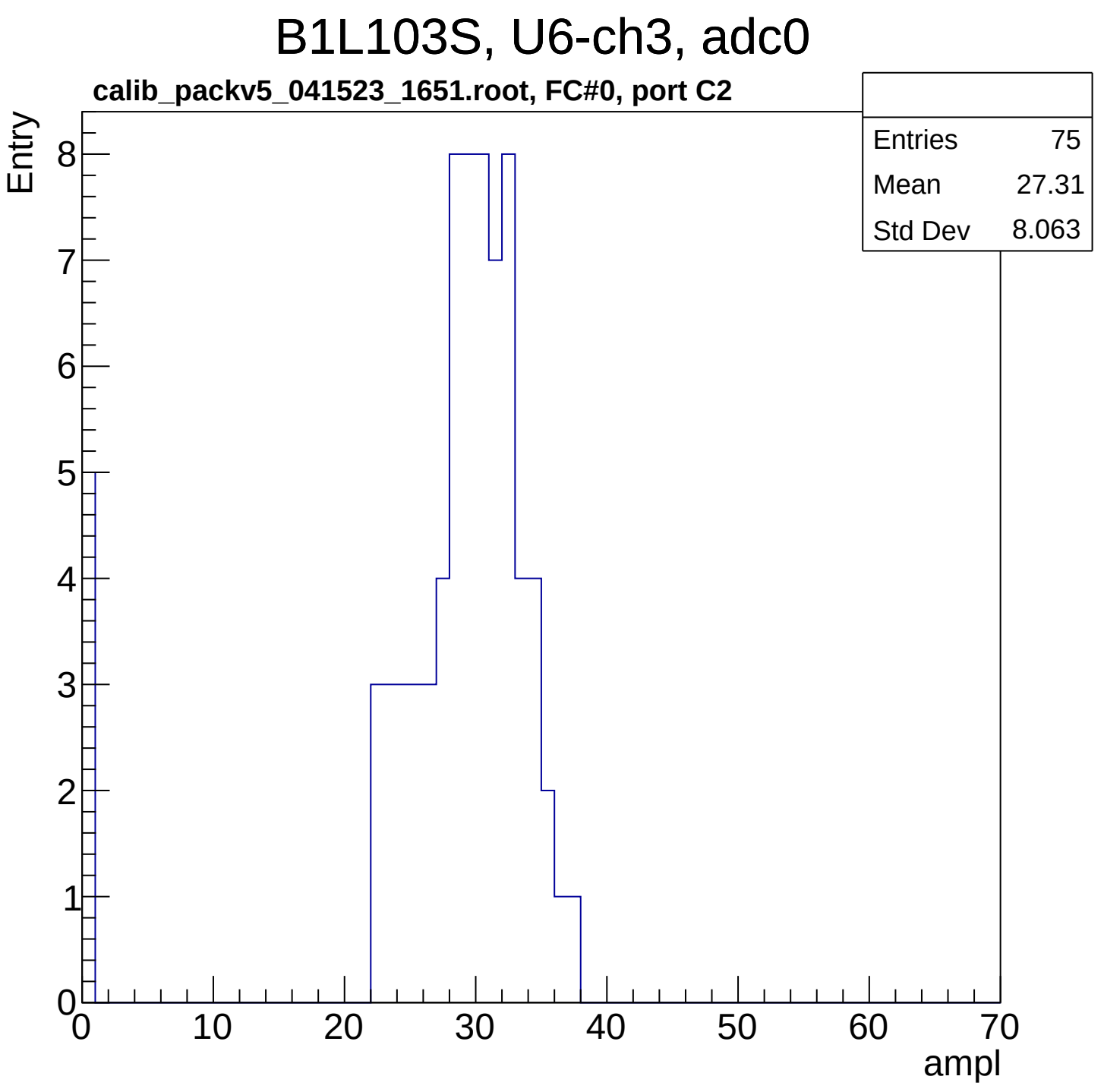
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch3, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 27.31
Std Dev 8.063
Entry
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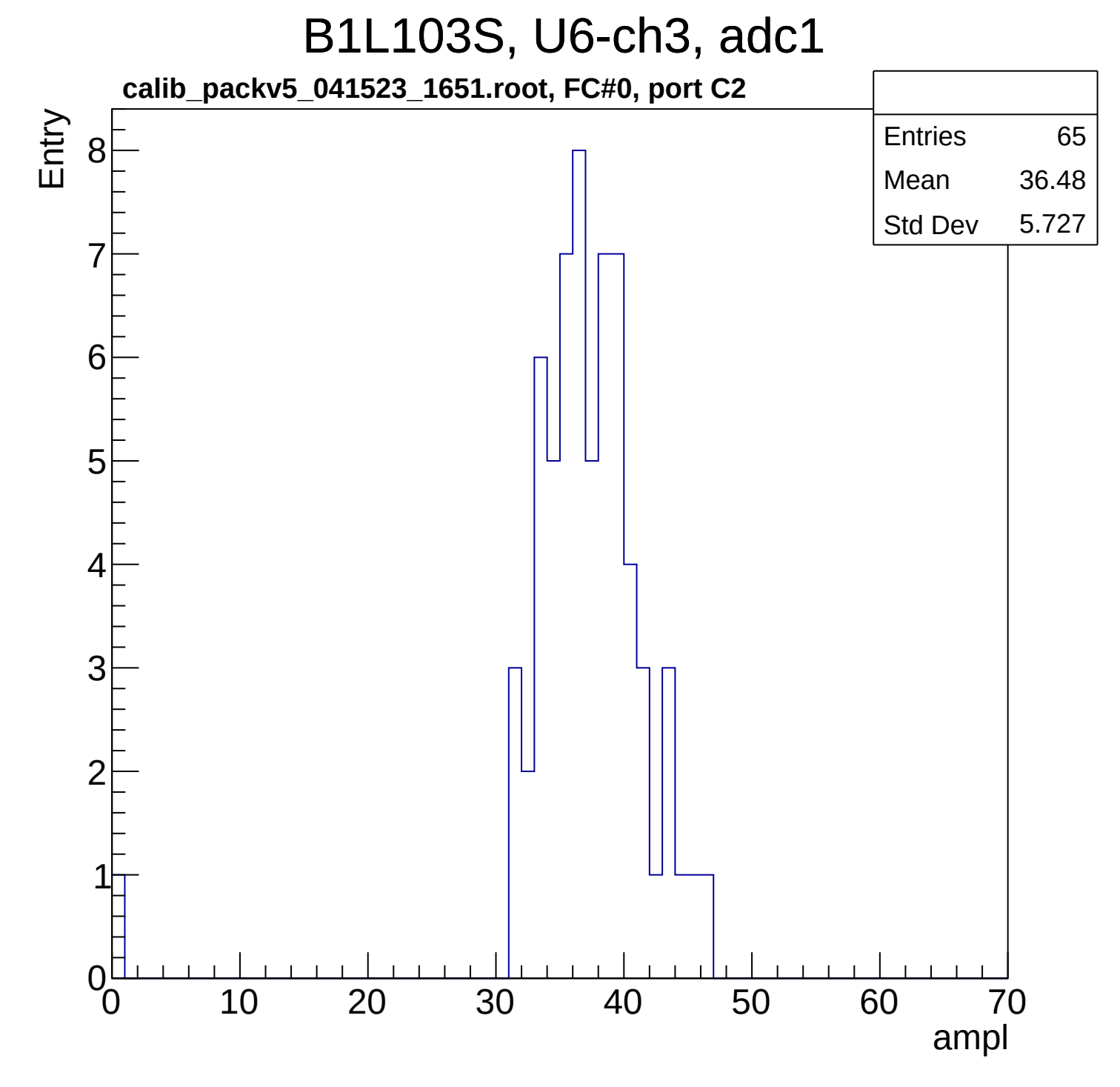
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch3, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 36.48
Std Dev 5.727
Entry
ampl
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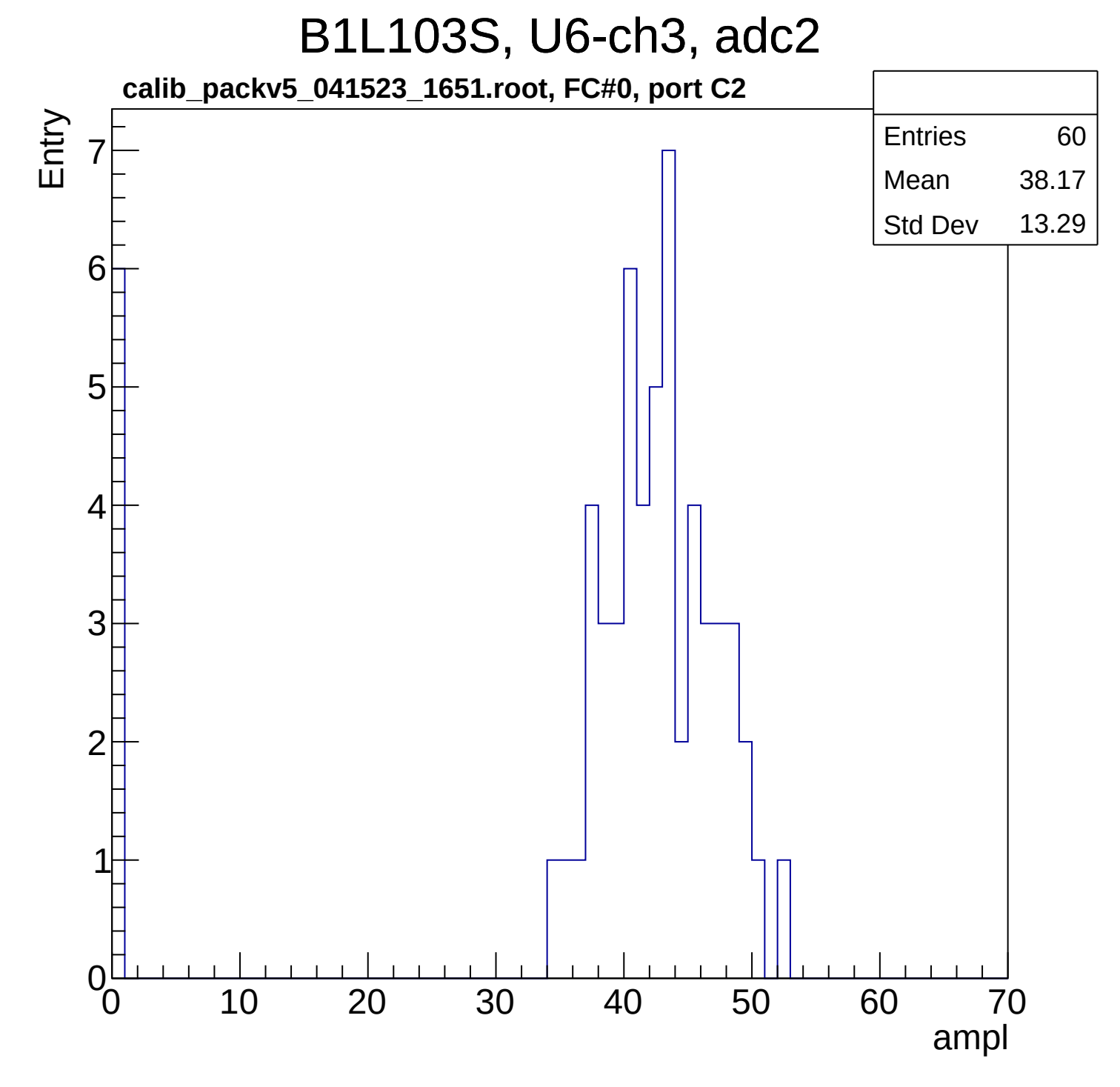
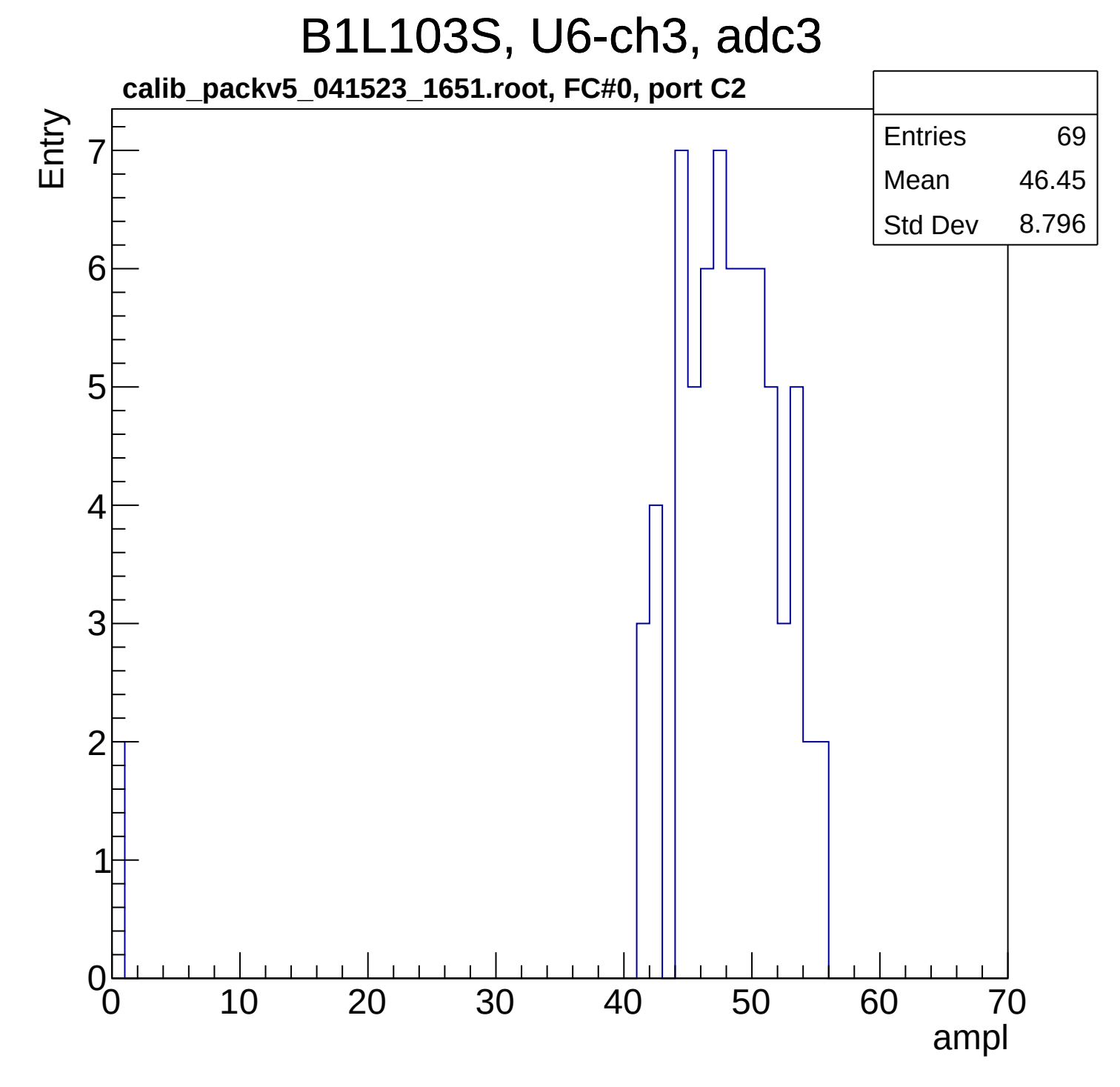
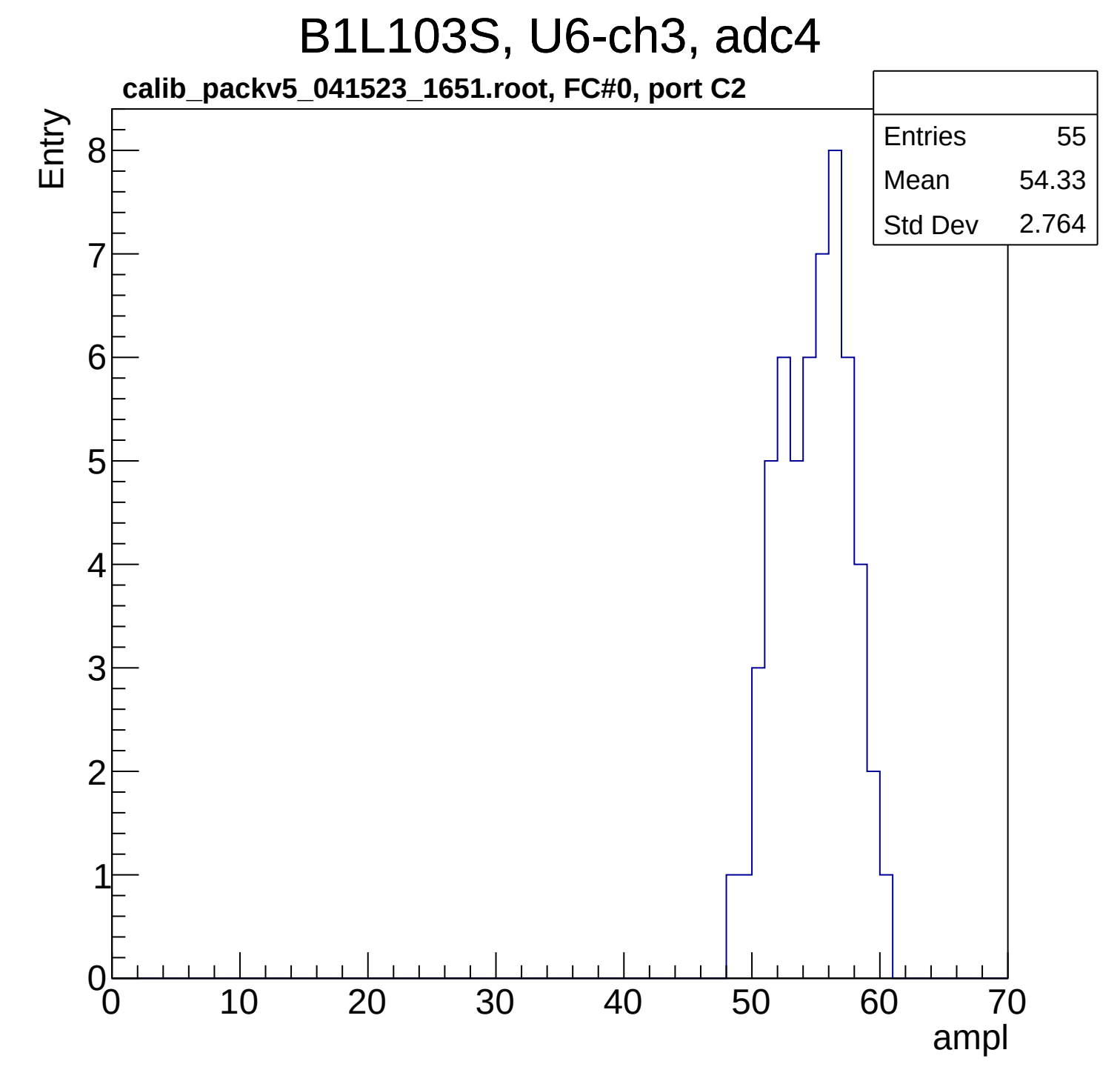
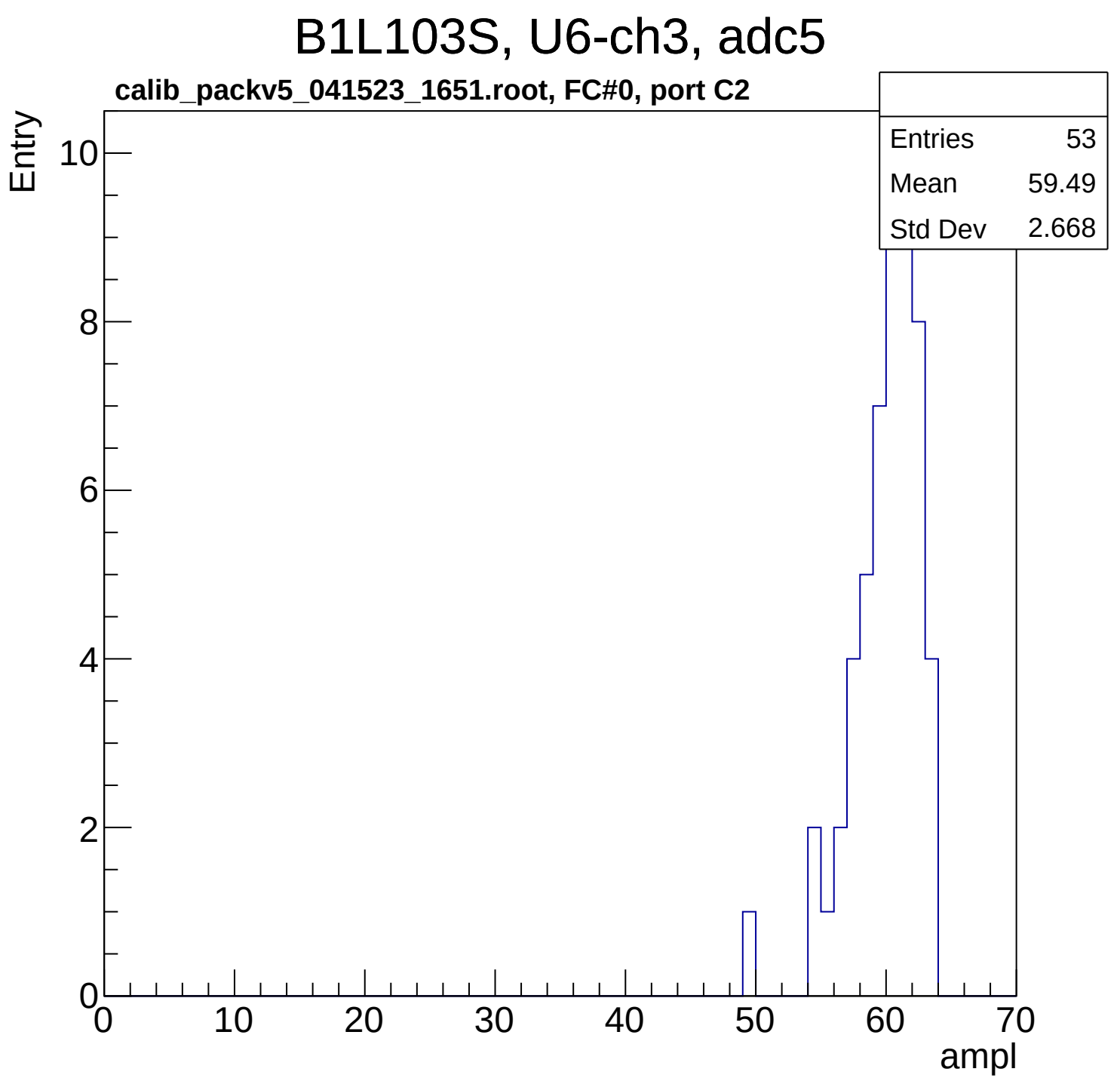
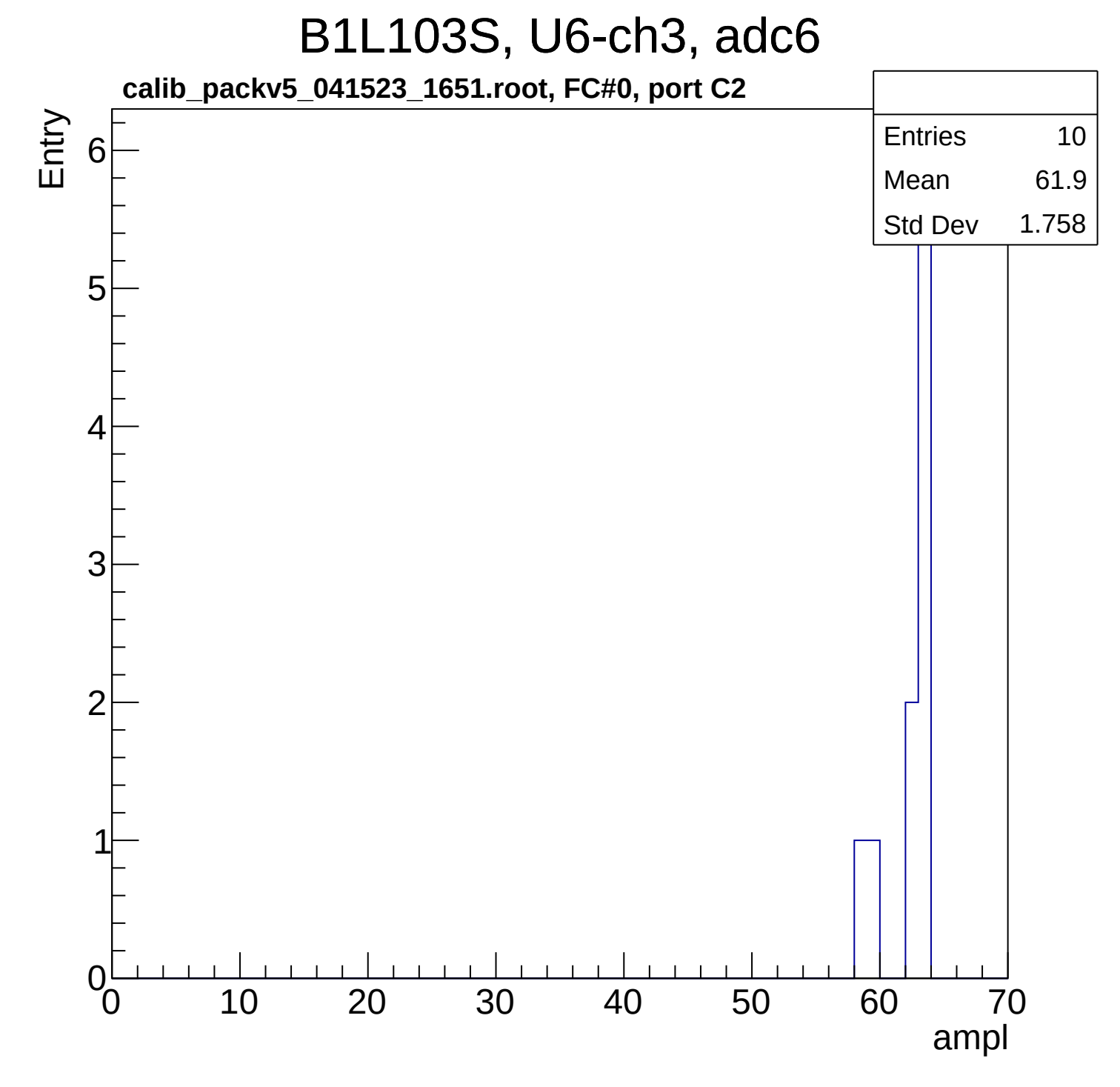
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

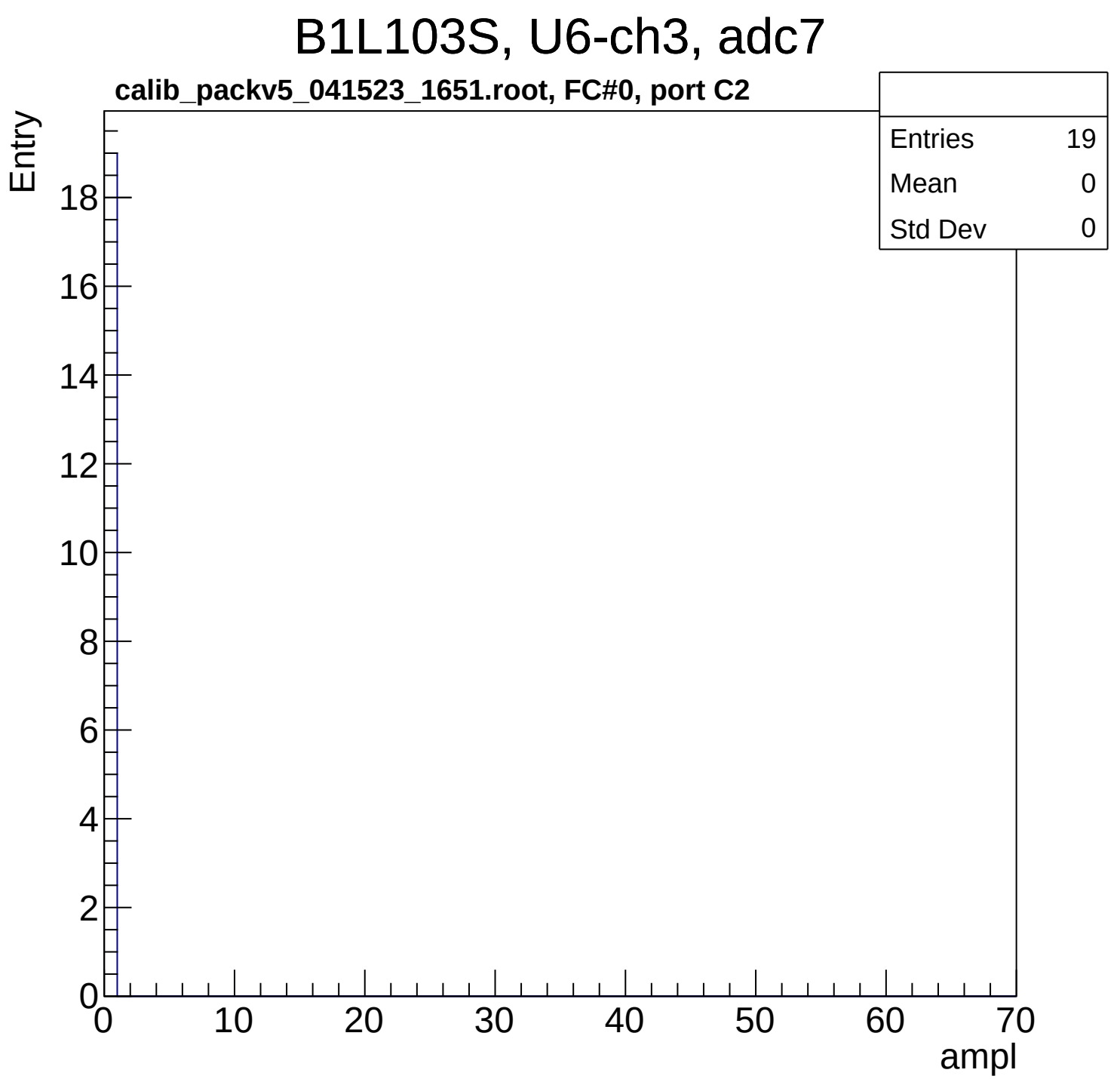

B1L103S, U6-ch3, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 38.17
Std Dev 13.29
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U6-ch3, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 46.45
Std Dev 8.796
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U6-ch3, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 54.33
Std Dev 2.764
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch3, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 59.49
Std Dev 2.668
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch3, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61.9
Std Dev 1.758
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch3, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
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10
20
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50
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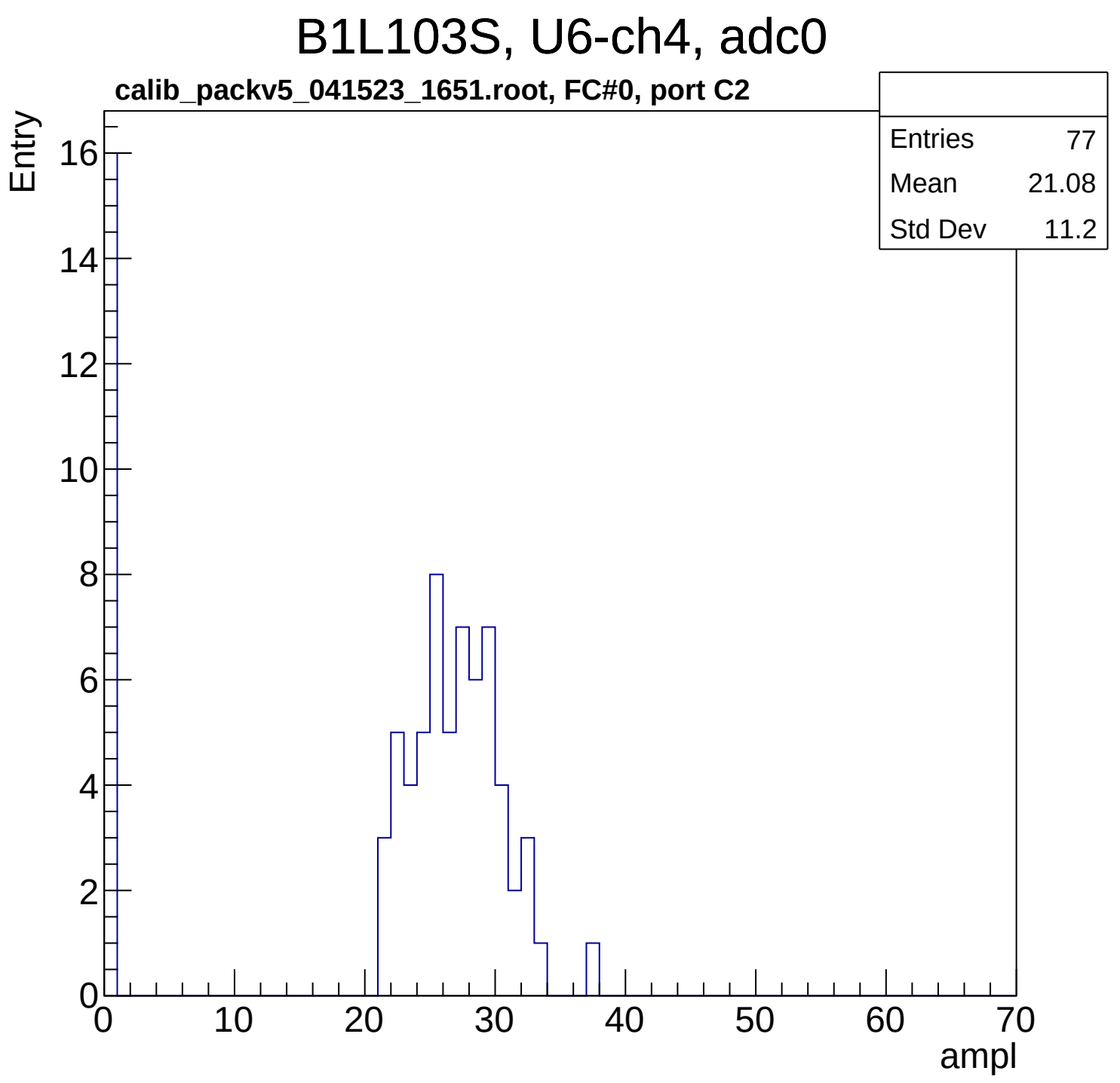
70
ampl


B1L103S, U6-ch4, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 21.08
Std Dev 11.2
Entry
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4
6
8
10
12
14
16
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10
20
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50
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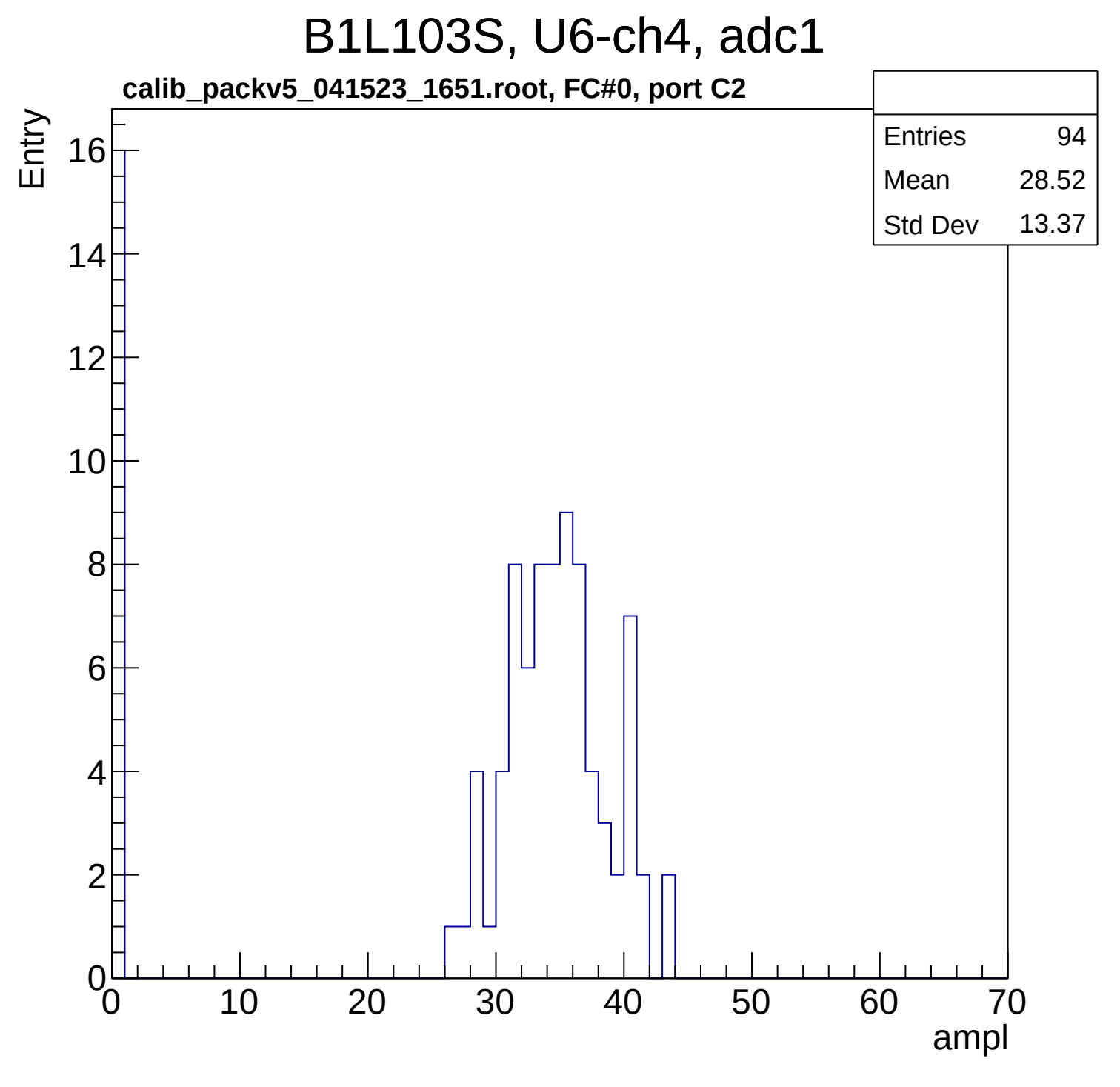
70
ampl


B1L103S, U6-ch4, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 28.52
Std Dev 13.37
Entry
ampl
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4
6
8
10
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14
16
0
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60
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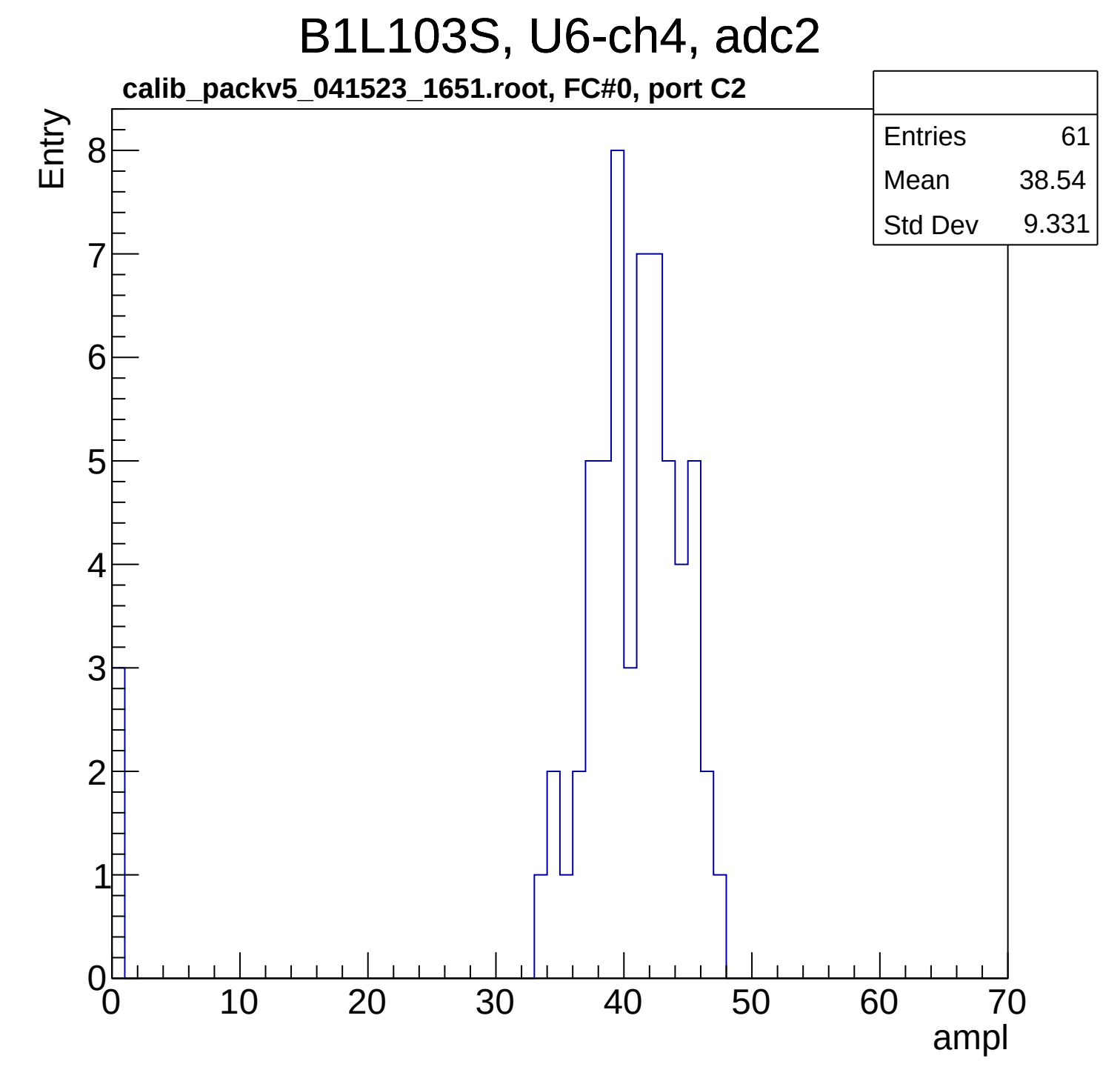
B1L103S, U6-ch4, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 38.54
Std Dev 9.331
Entry
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2
3
4
5
6
7
8
0
10
20
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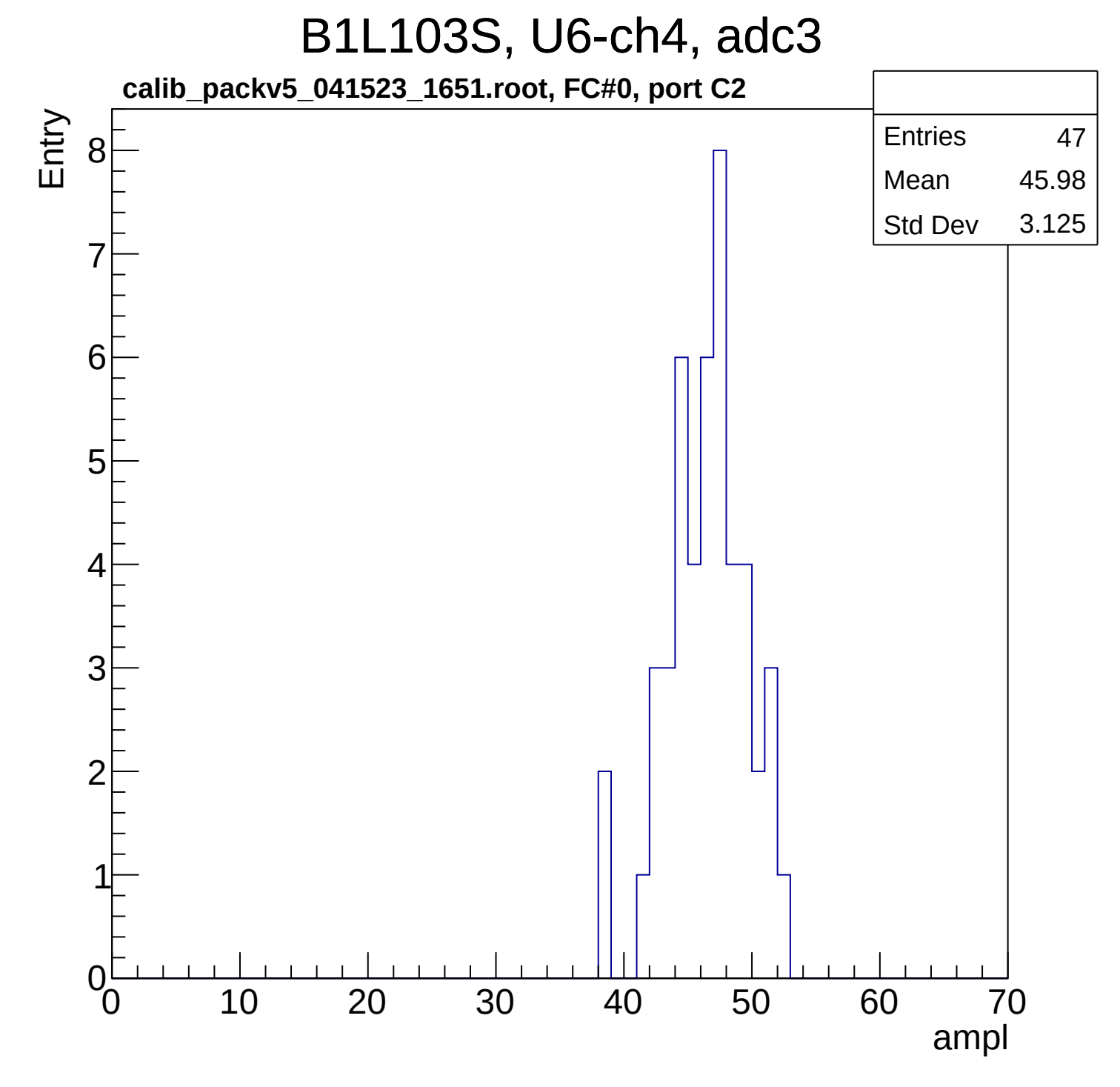
40
50
60
70
ampl


B1L103S, U6-ch4, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 45.98
Std Dev 3.125
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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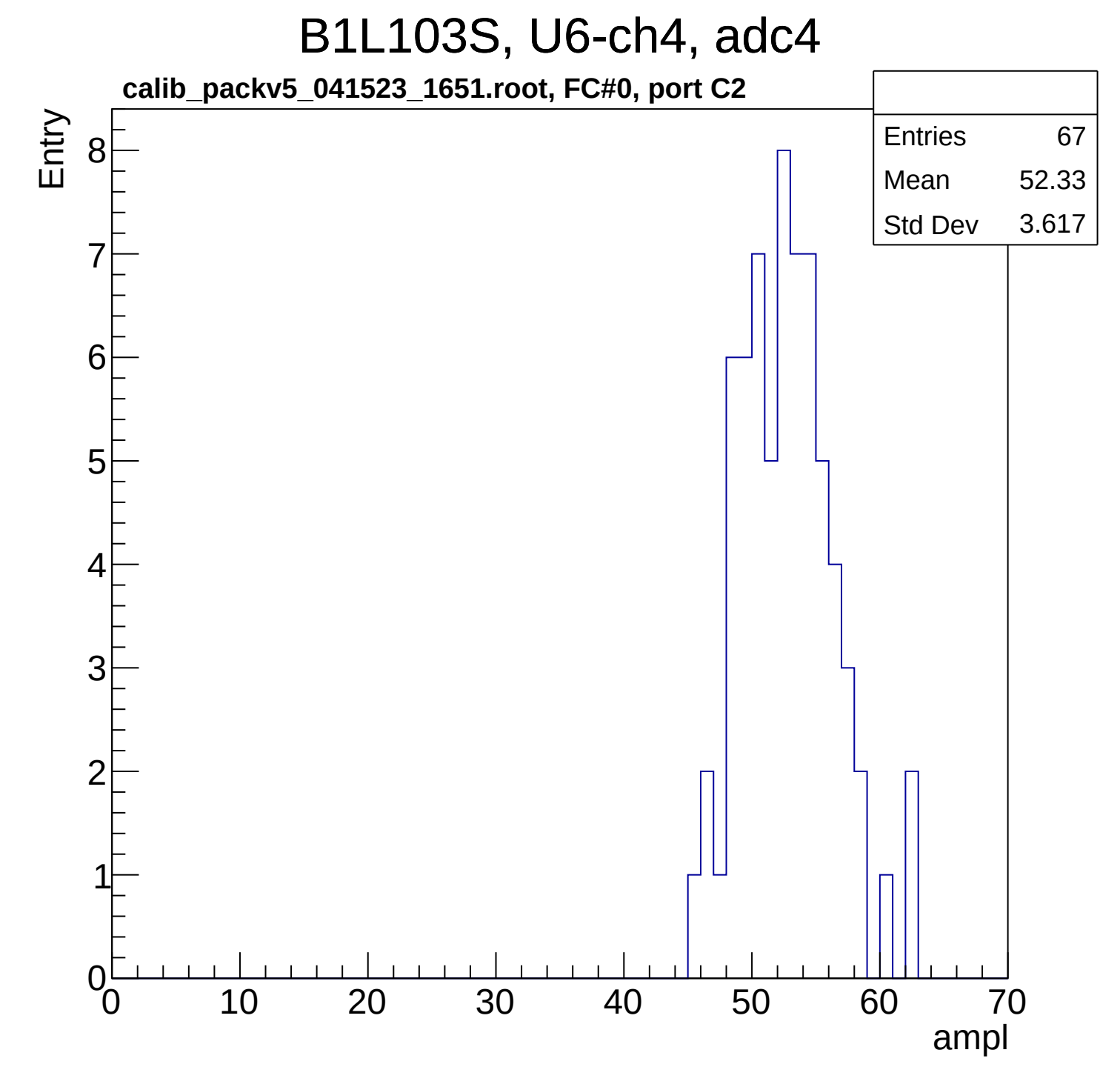
B1L103S, U6-ch4, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 52.33
Std Dev 3.617
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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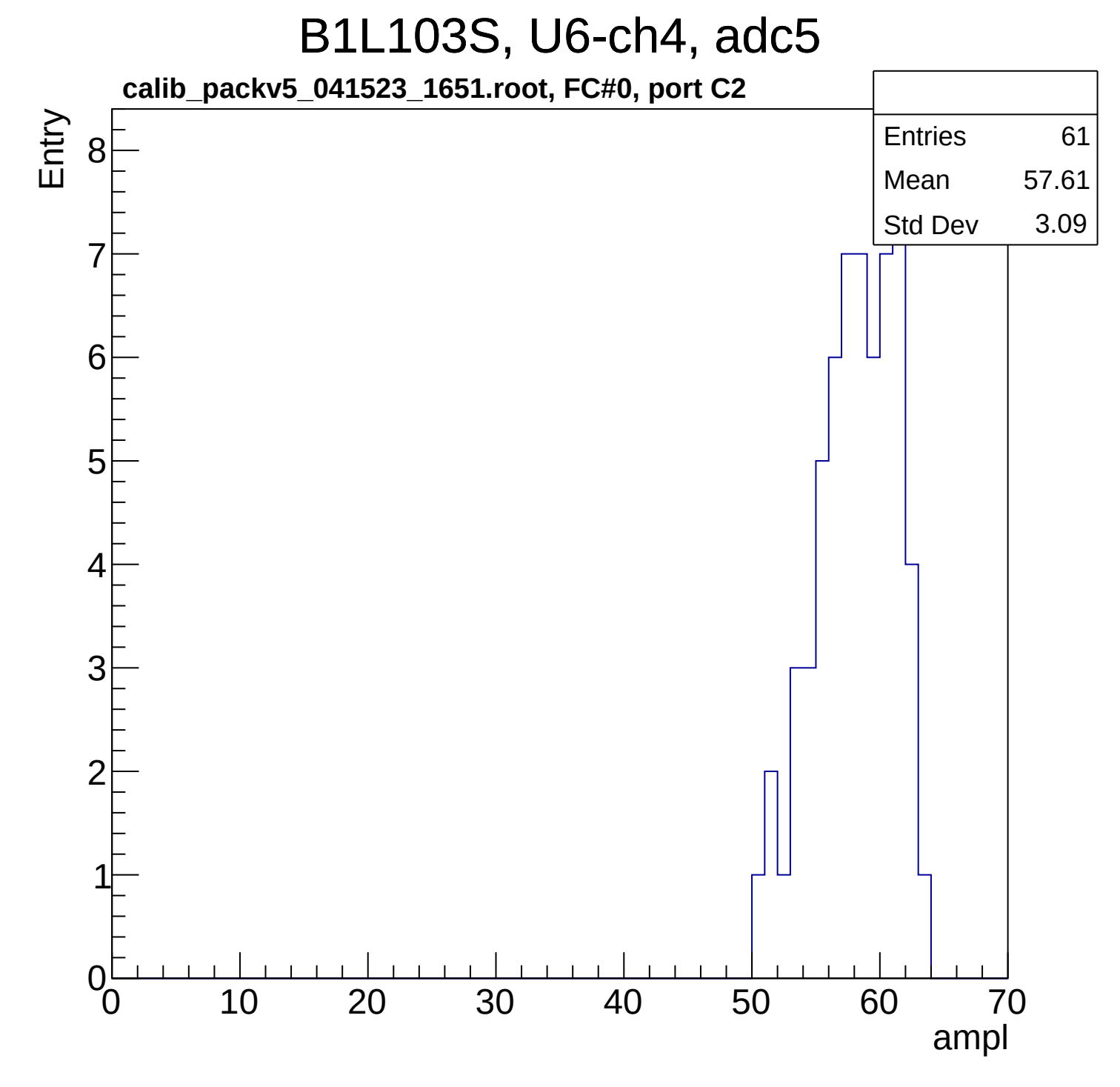
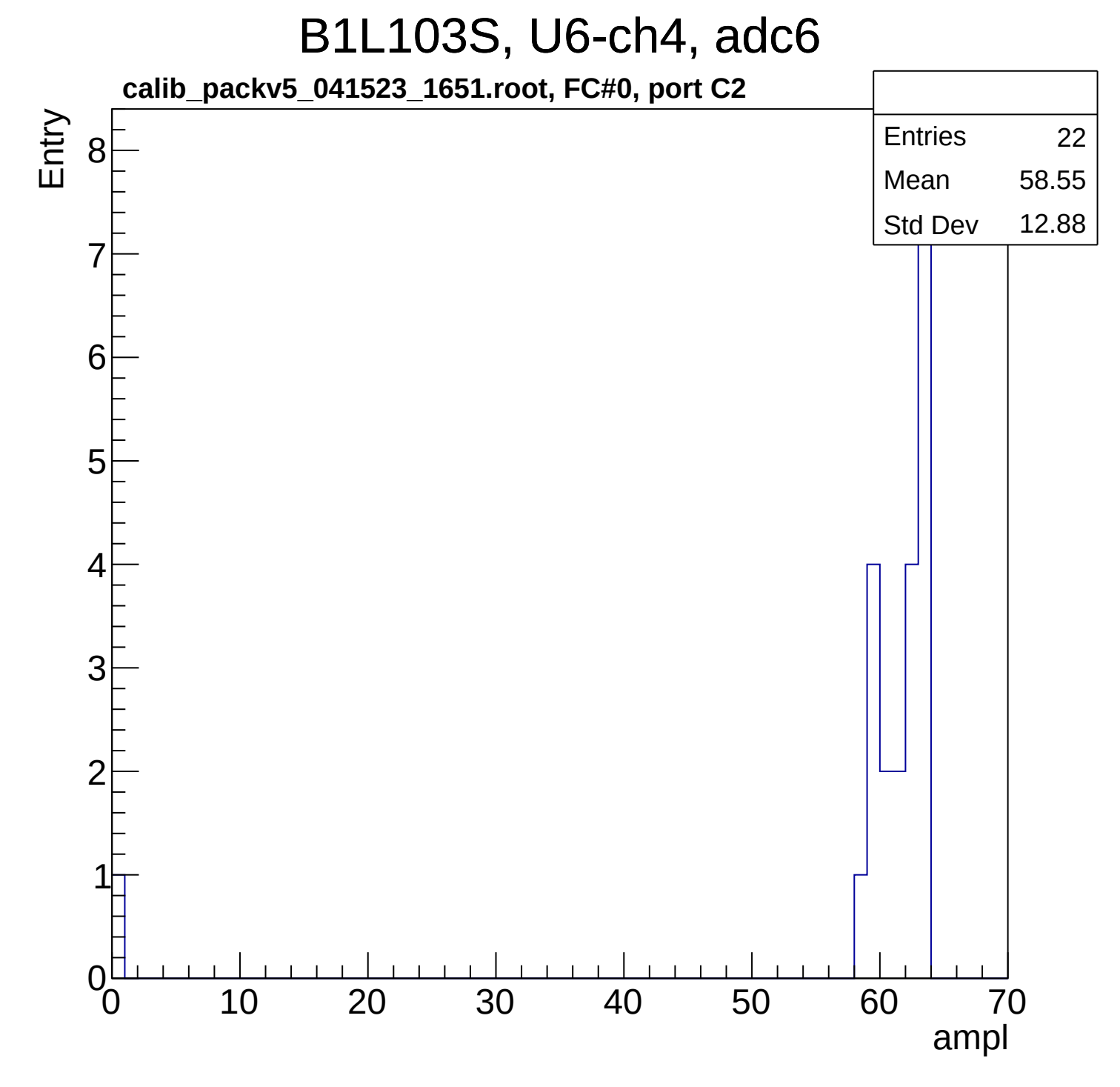

B1L103S, U6-ch4, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 57.61
Std Dev 3.09
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch4, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 58.55
Std Dev 12.88
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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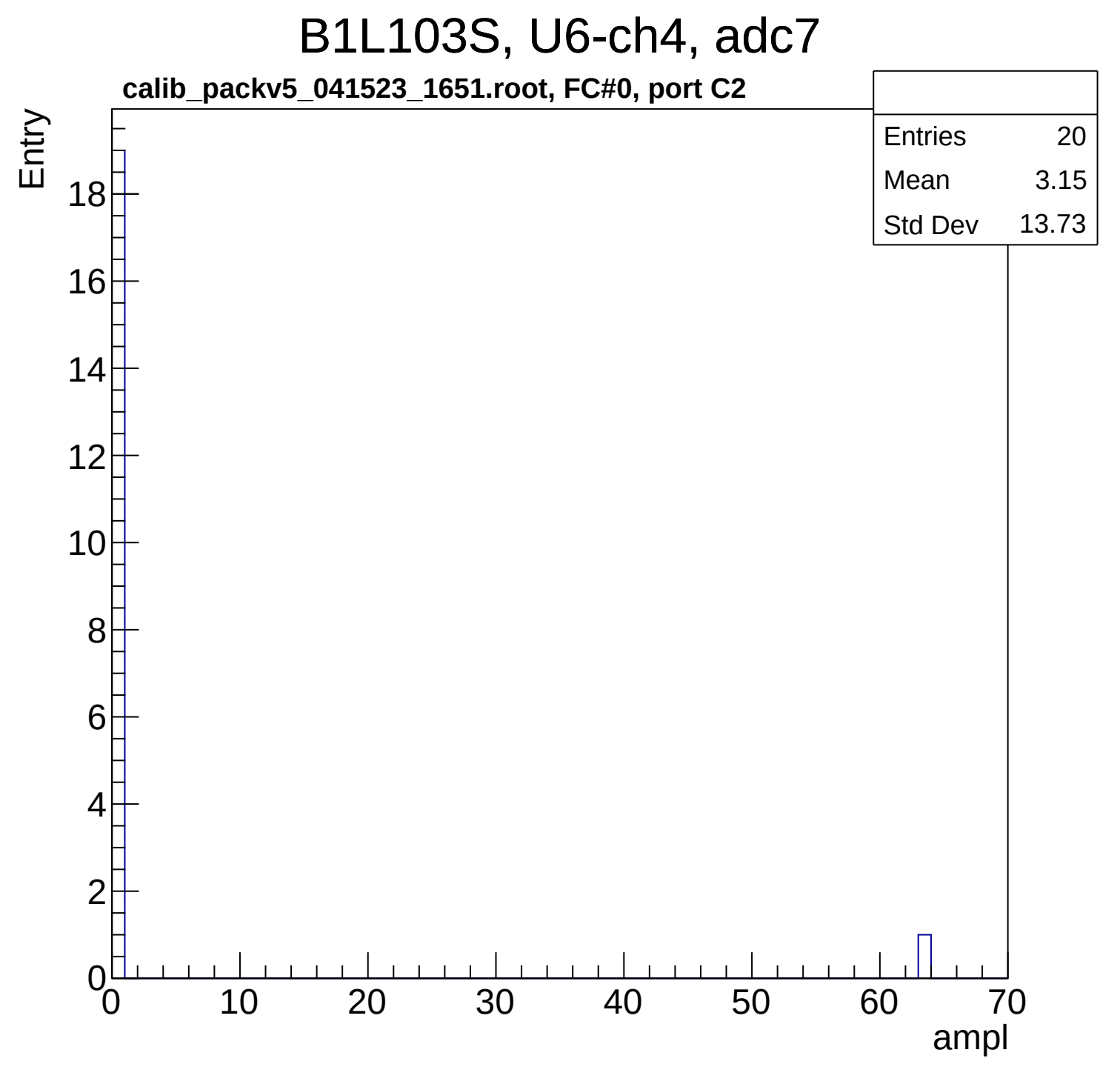
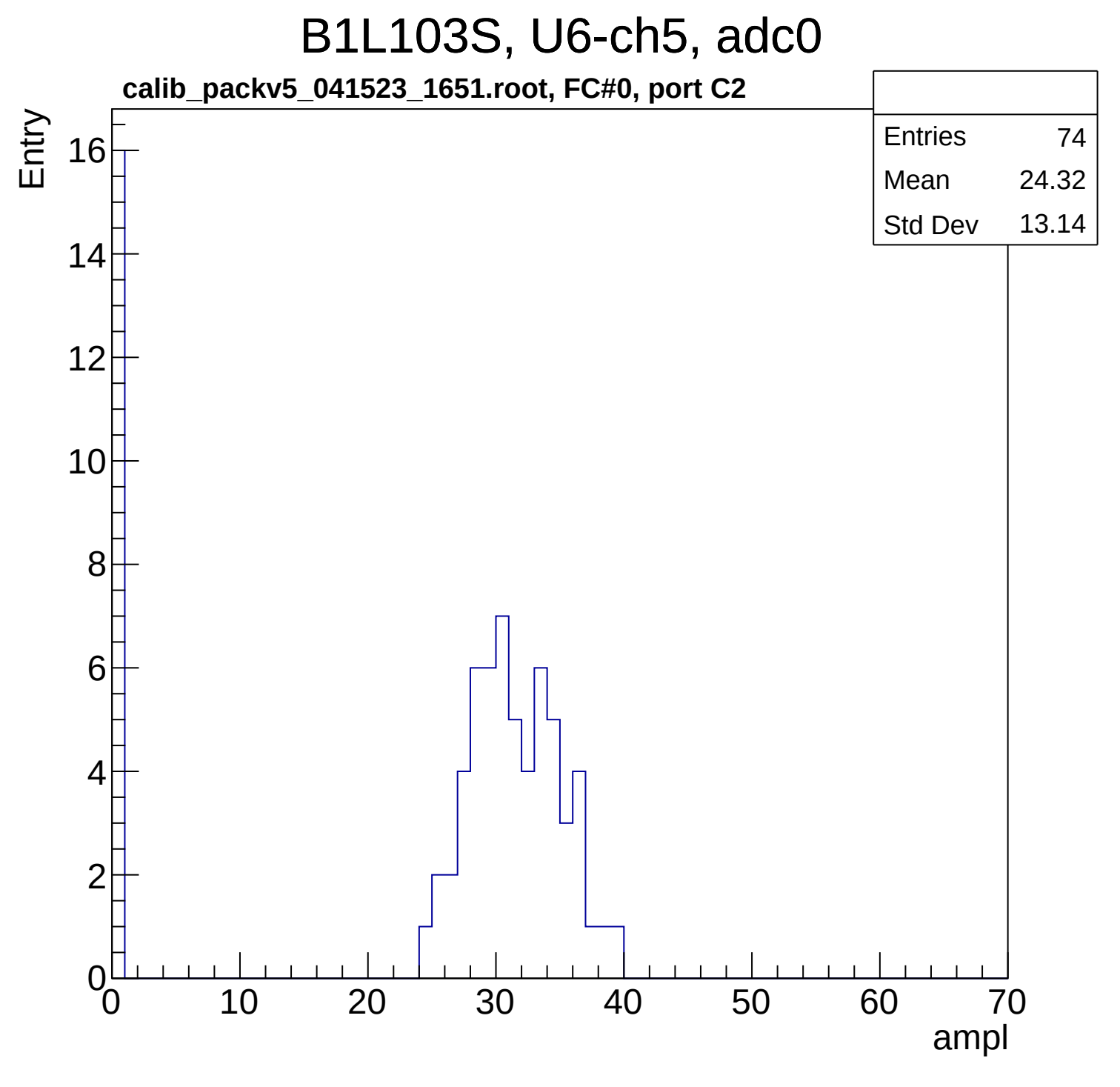
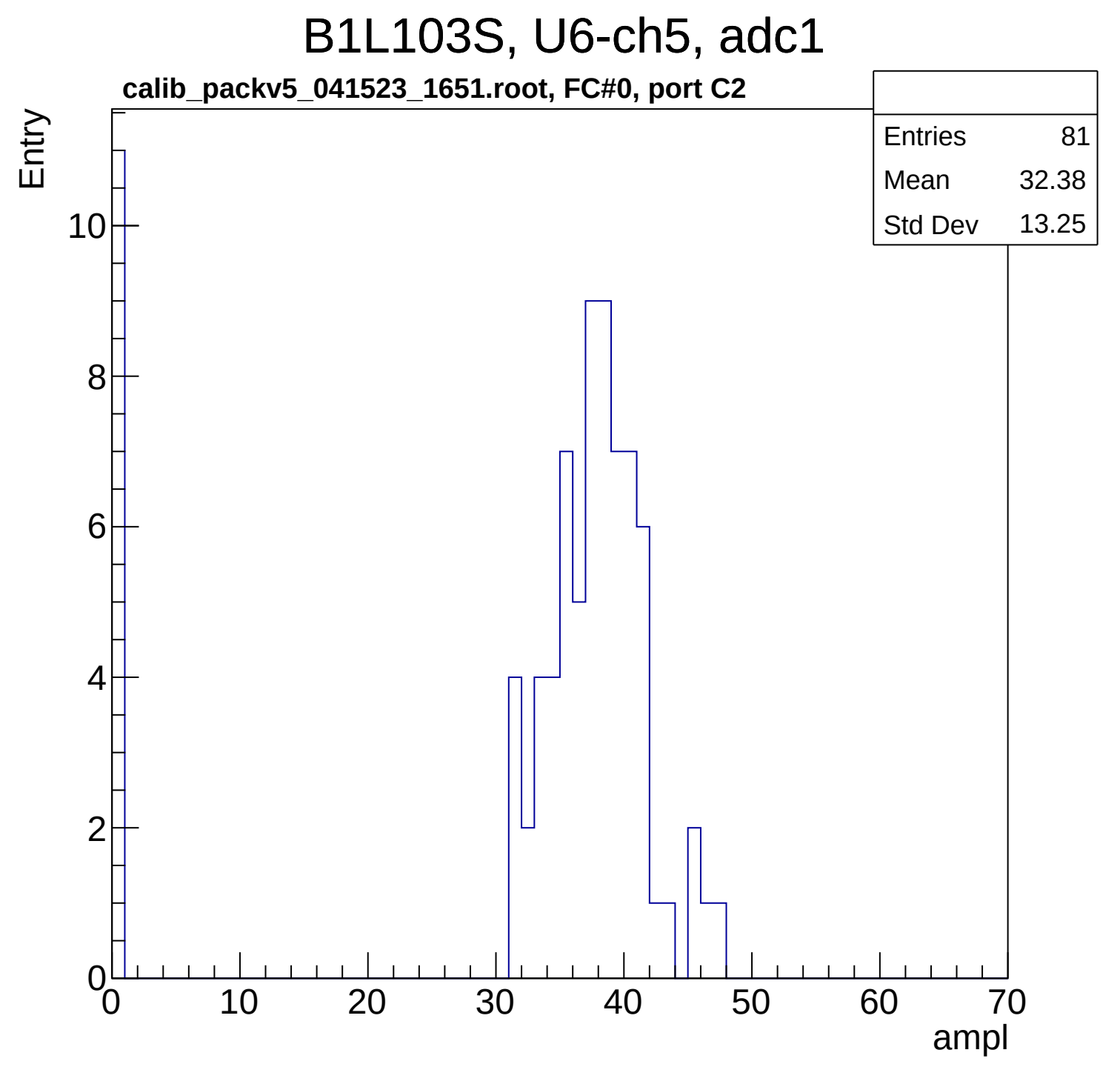
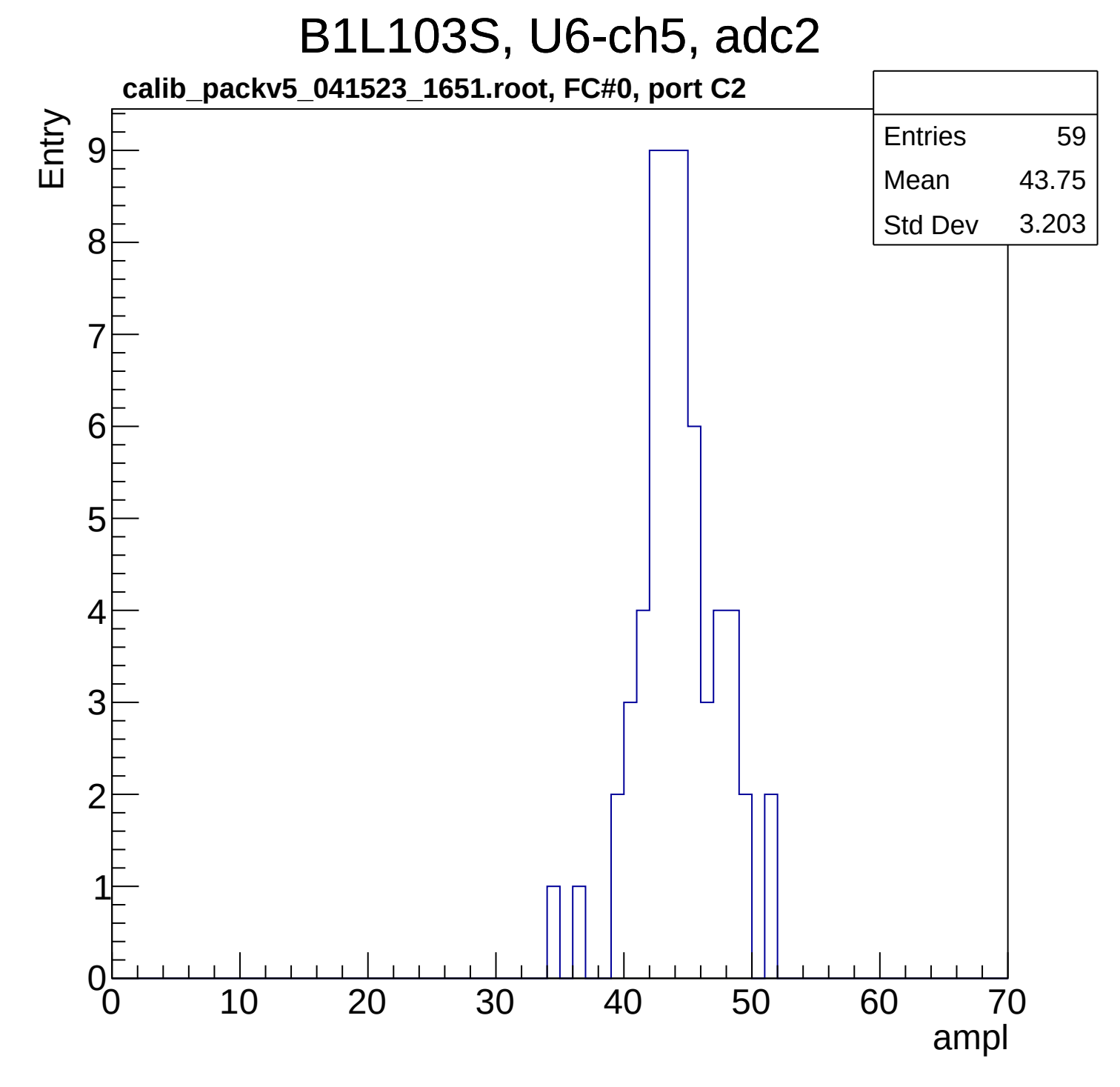
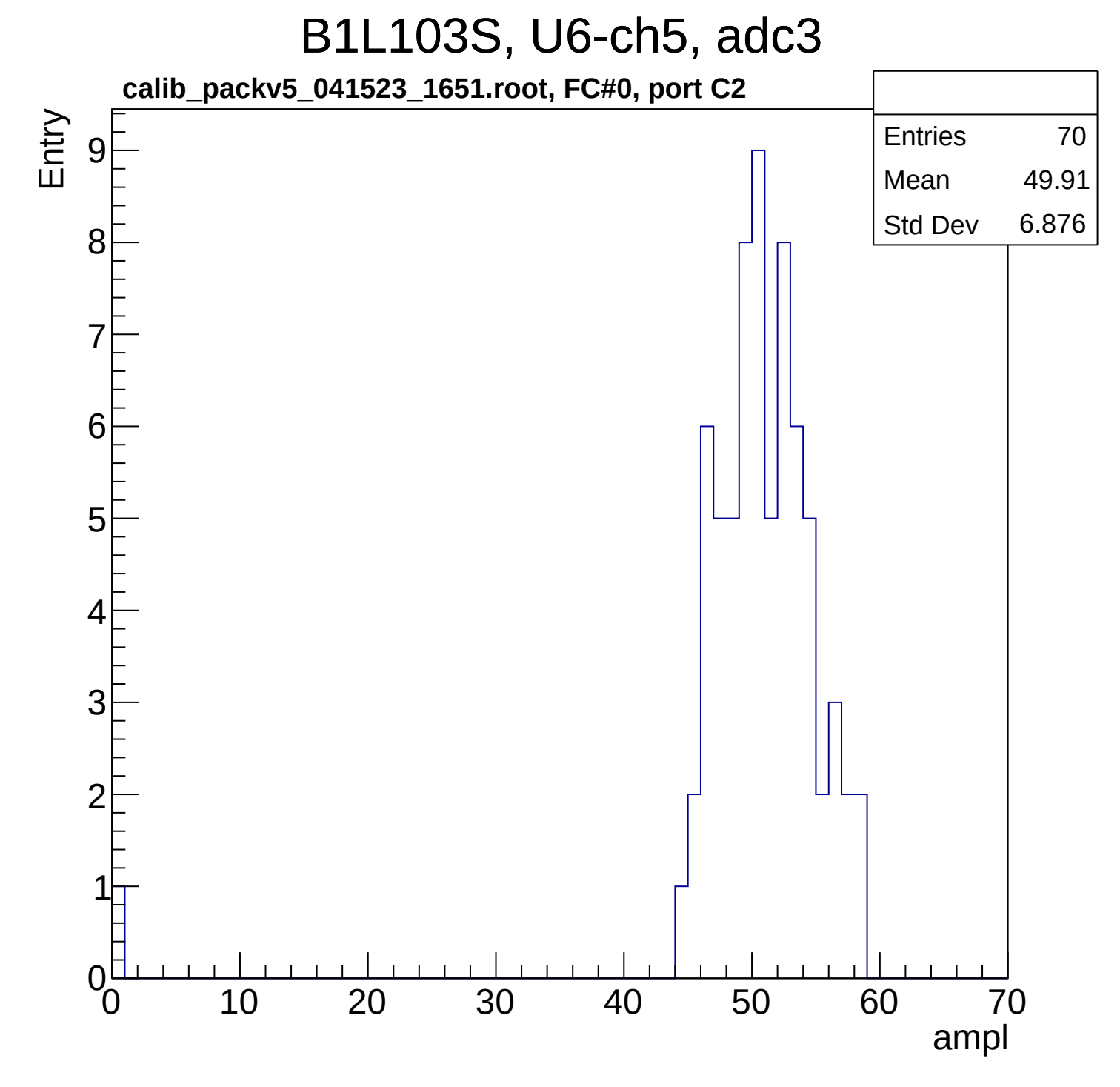
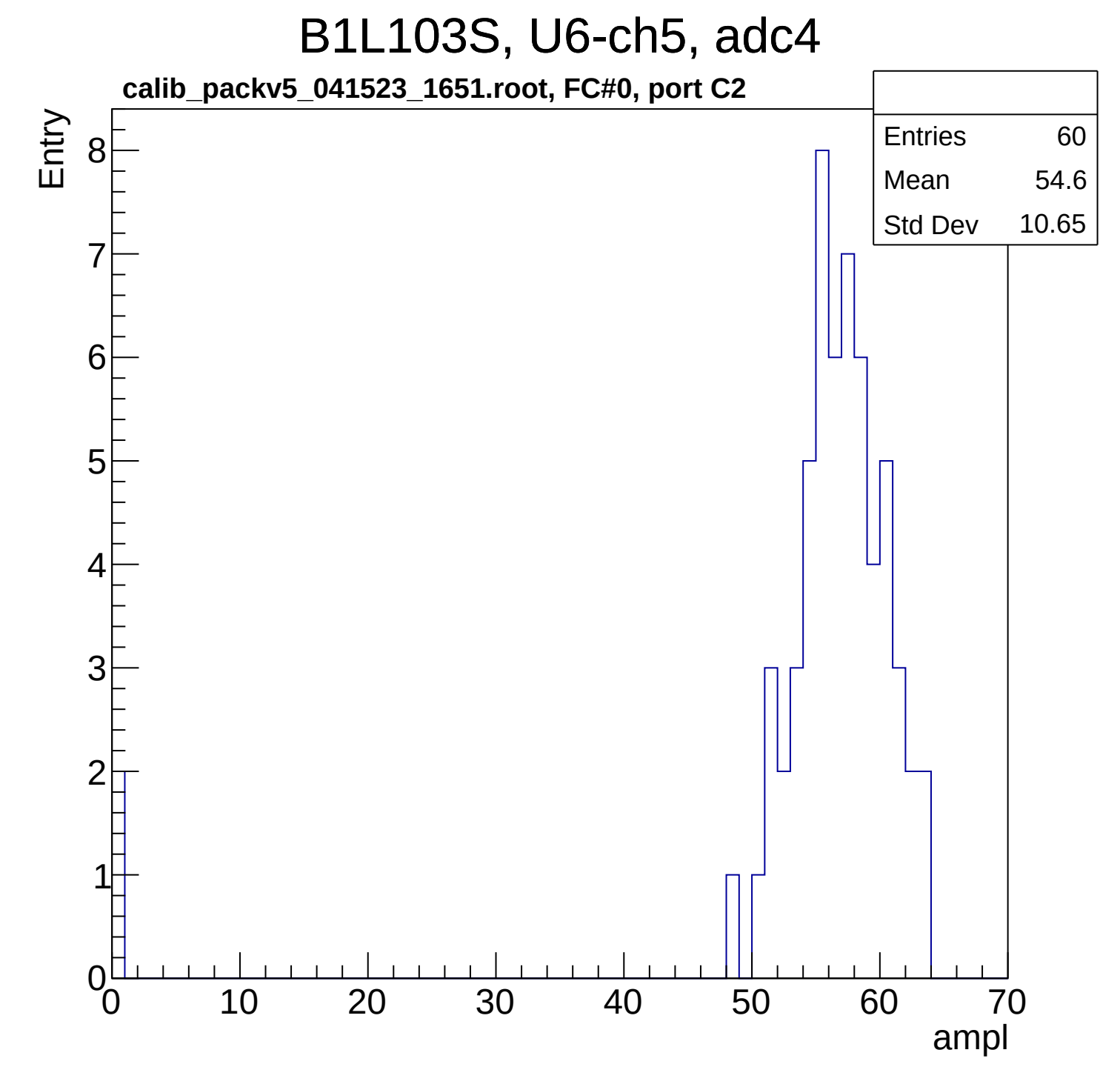

B1L103S, U6-ch4, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

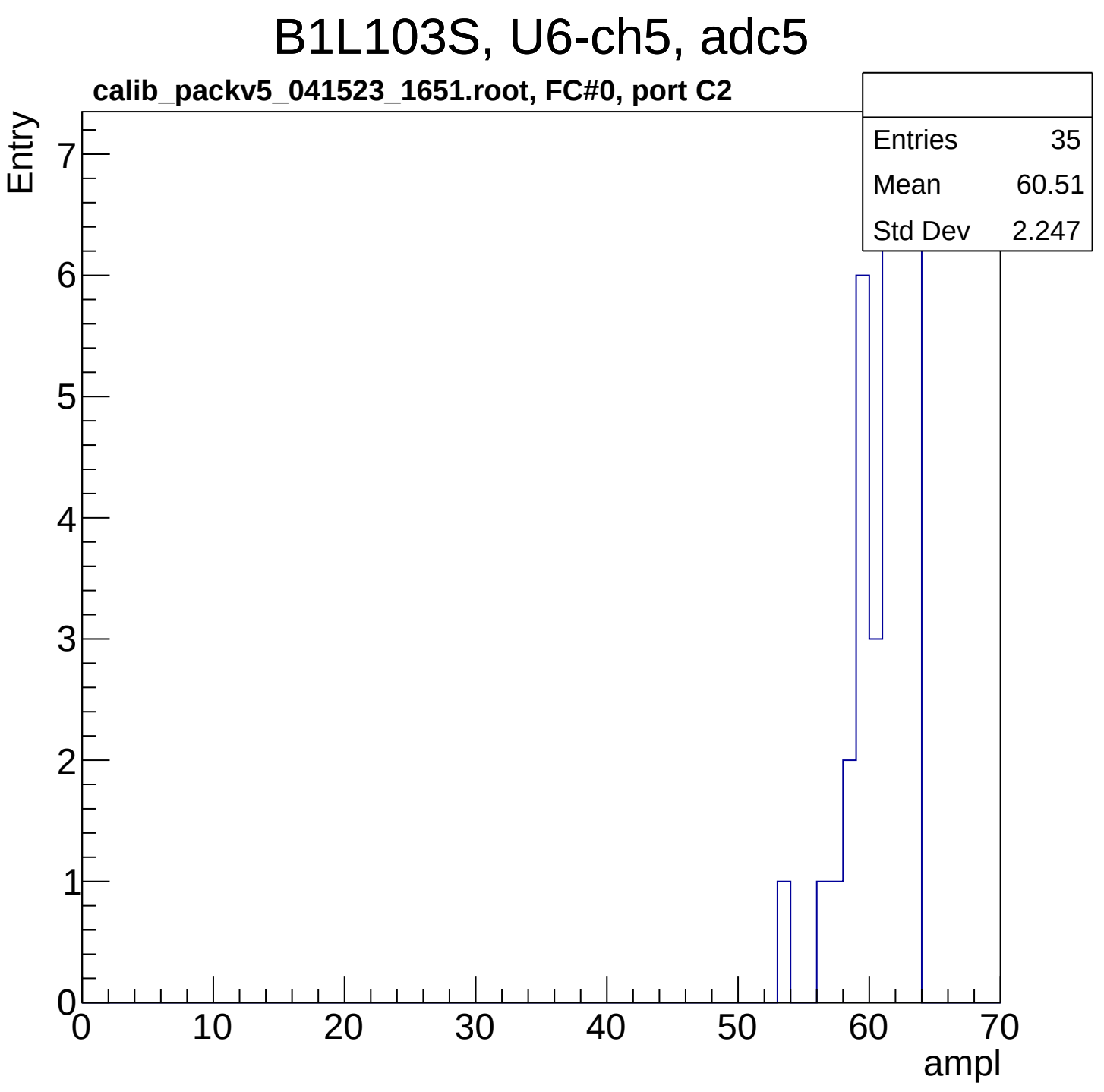

B1L103S, U6-ch5, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 24.32
Std Dev 13.14
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

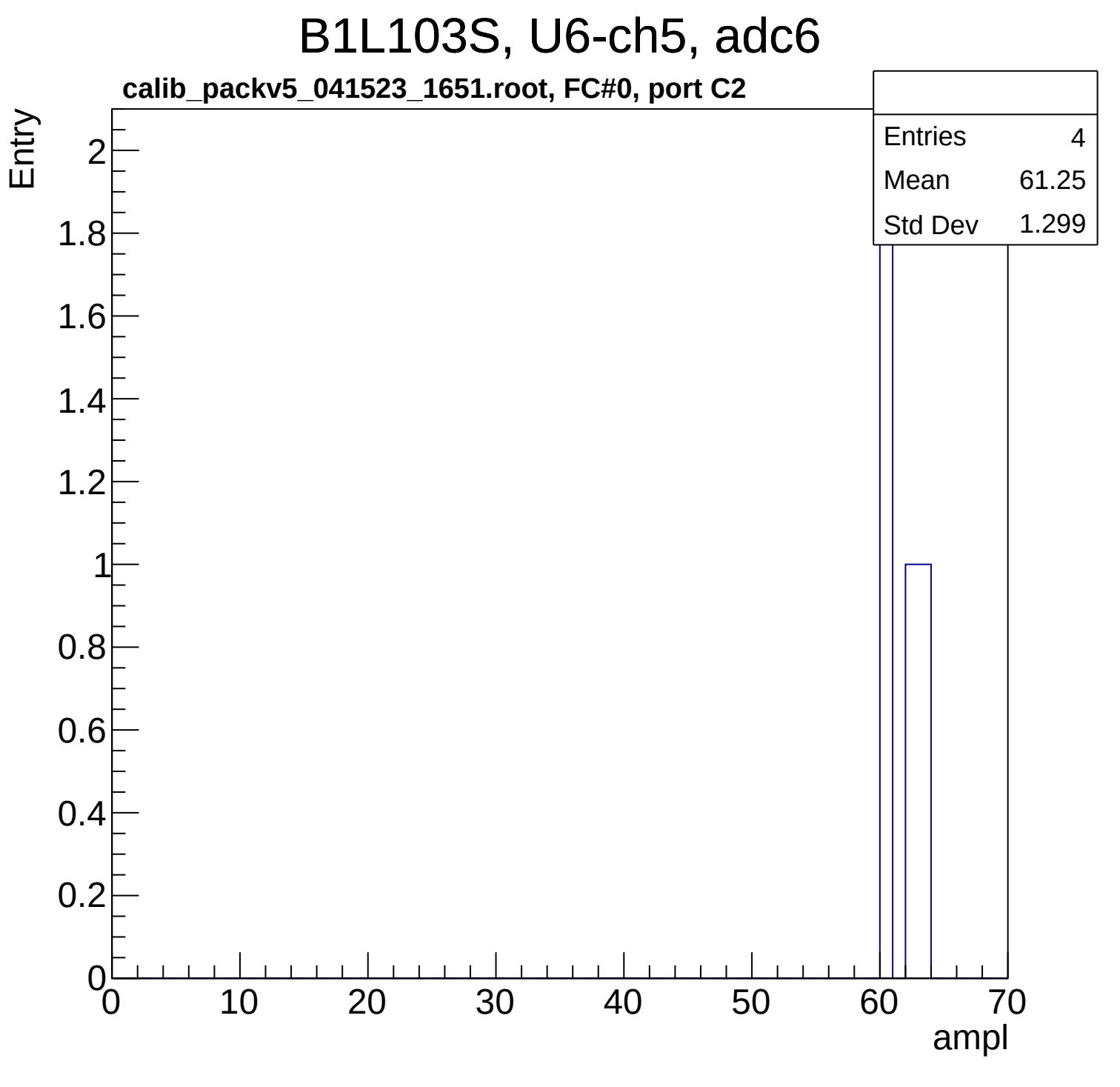

B1L103S, U6-ch5, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 32.38
Std Dev 13.25
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

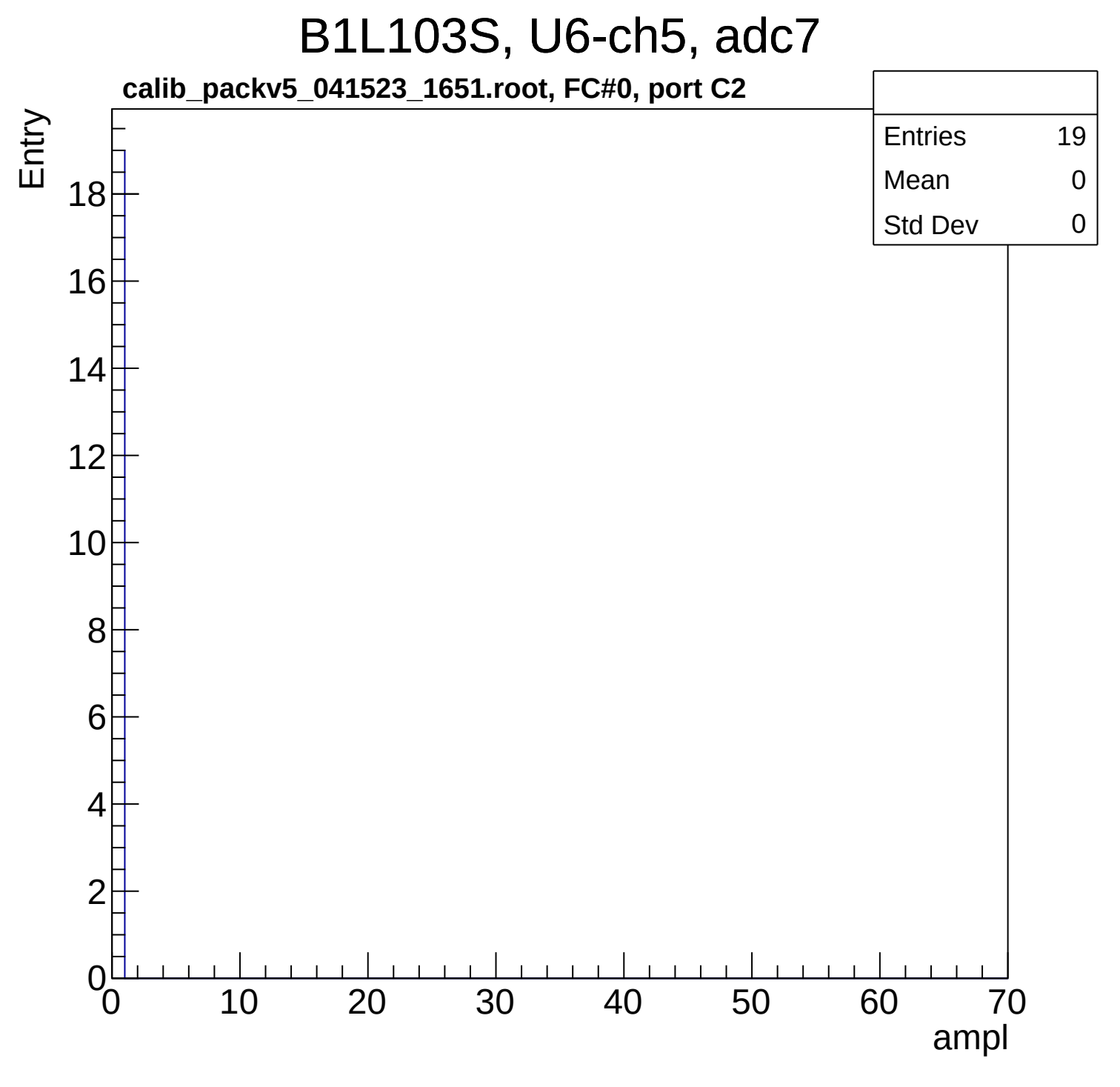

B1L103S, U6-ch5, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 43.75
Std Dev 3.203
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

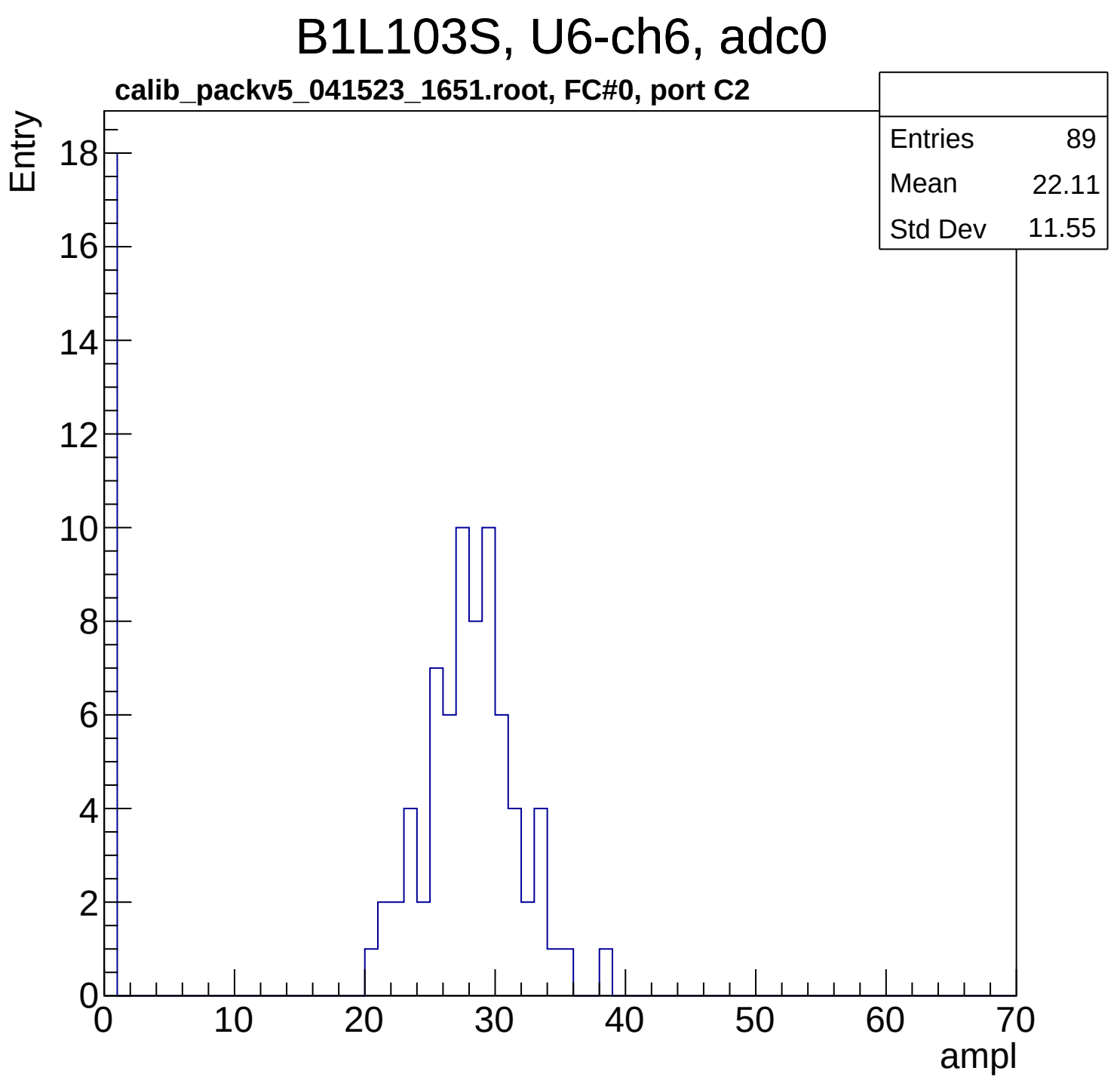

B1L103S, U6-ch5, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 49.91
Std Dev 6.876
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch5, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 54.6
Std Dev 10.65
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch5, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 60.51
Std Dev 2.247
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U6-ch5, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 61.25
Std Dev 1.299
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U6-ch5, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch6, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 22.11
Std Dev 11.55
Entry
0
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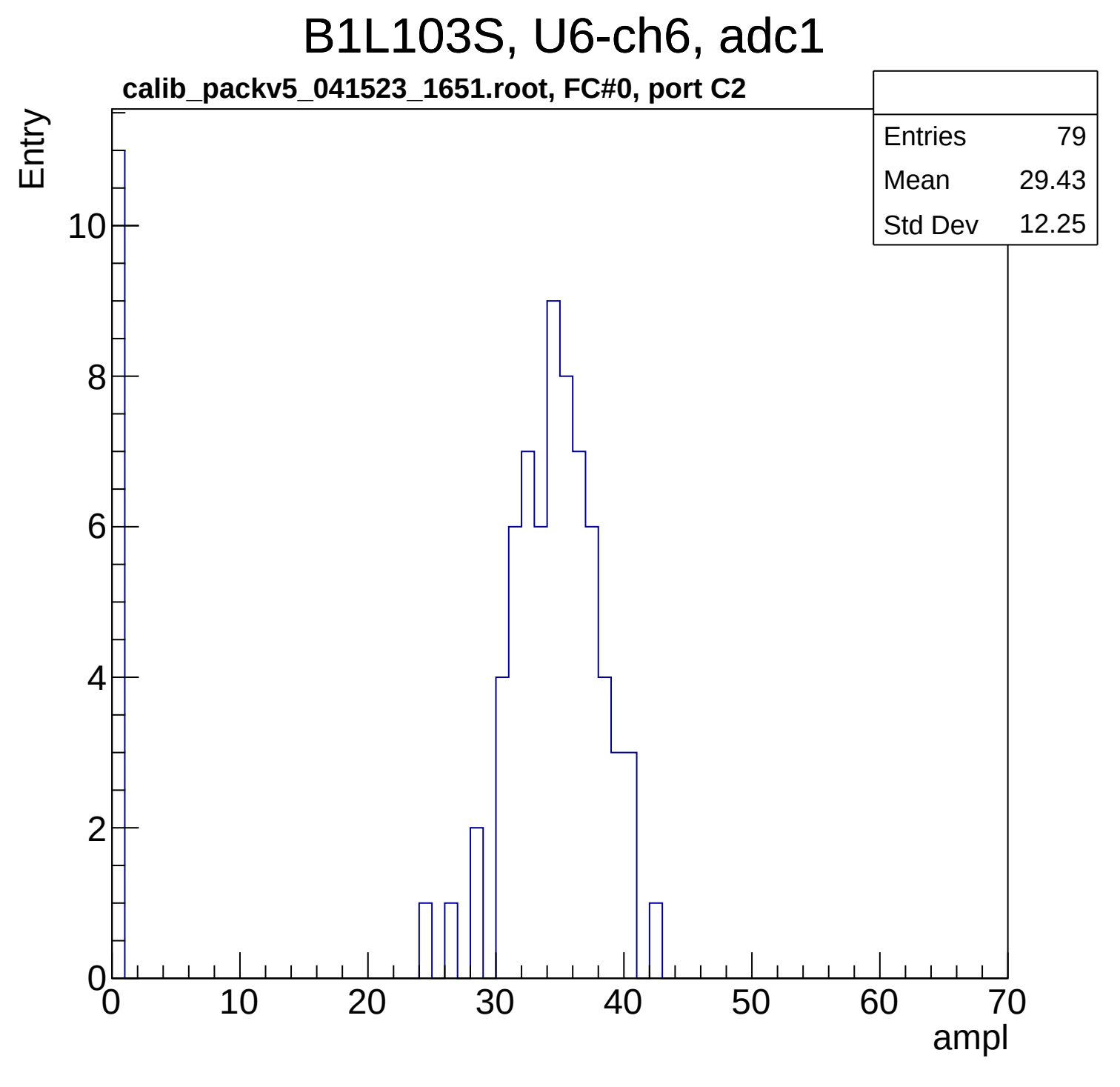
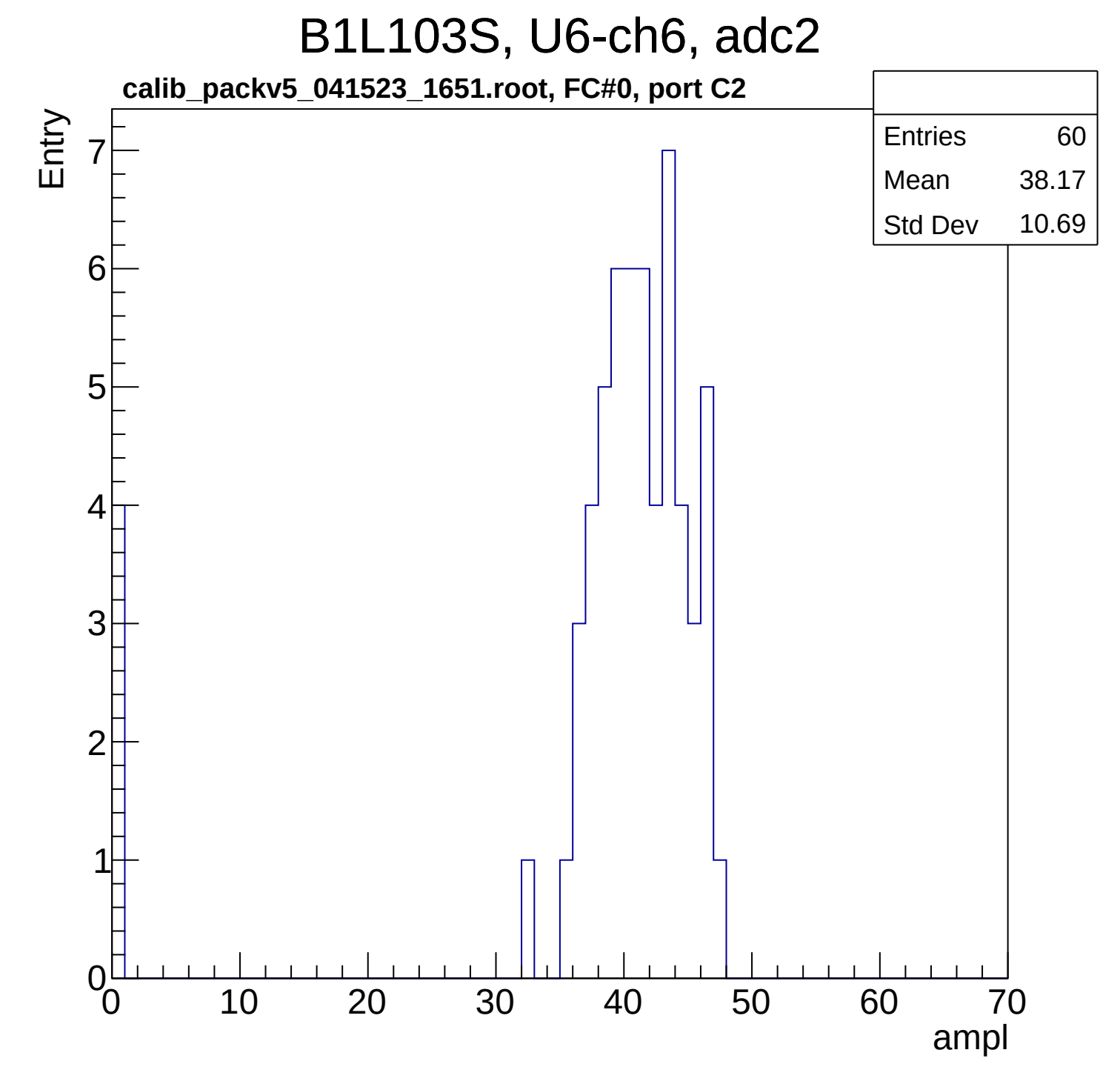
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch6, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 29.43
Std Dev 12.25
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch6, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 38.17
Std Dev 10.69
Entry
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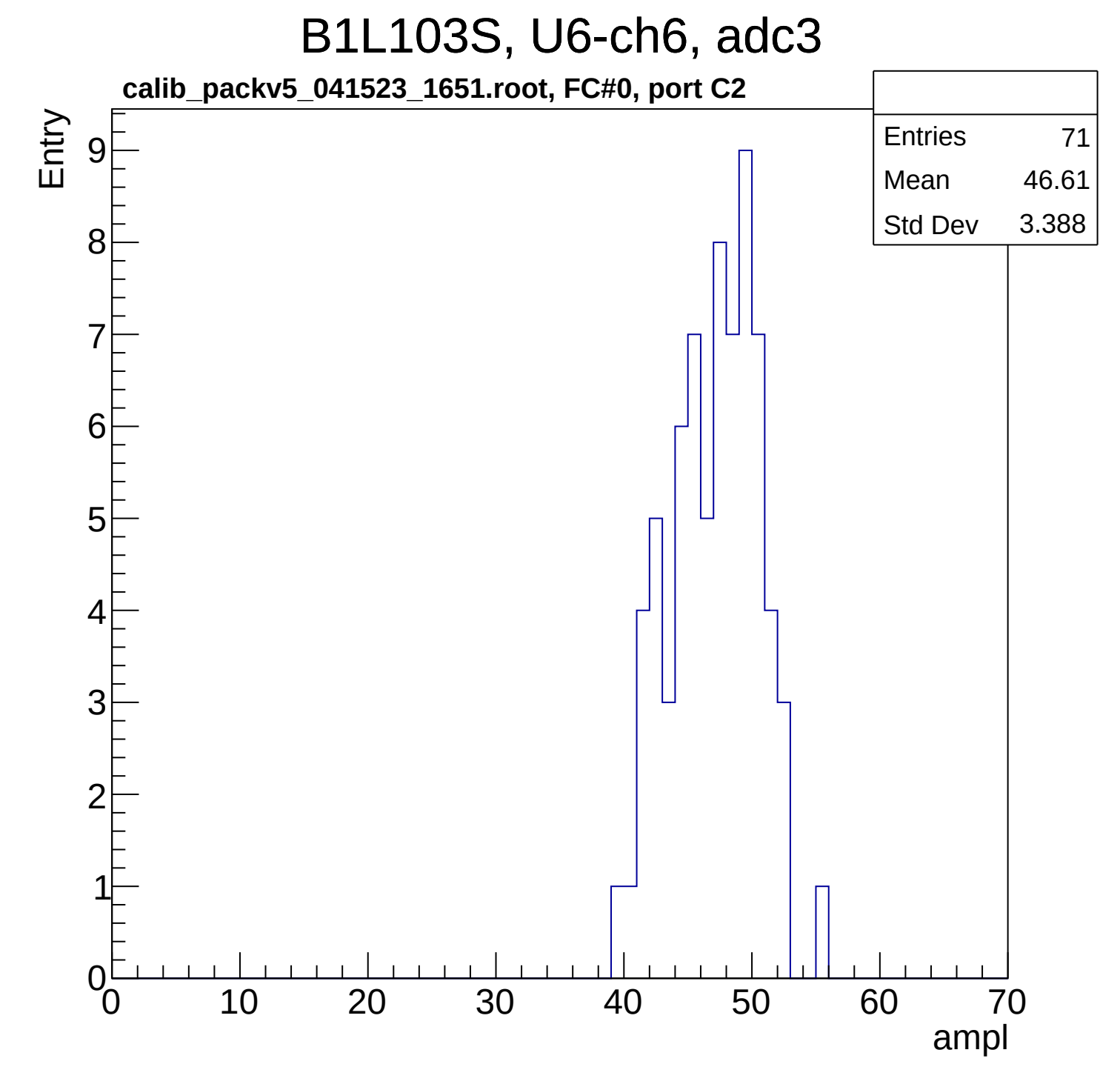
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch6, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 46.61
Std Dev 3.388
Entry
ampl
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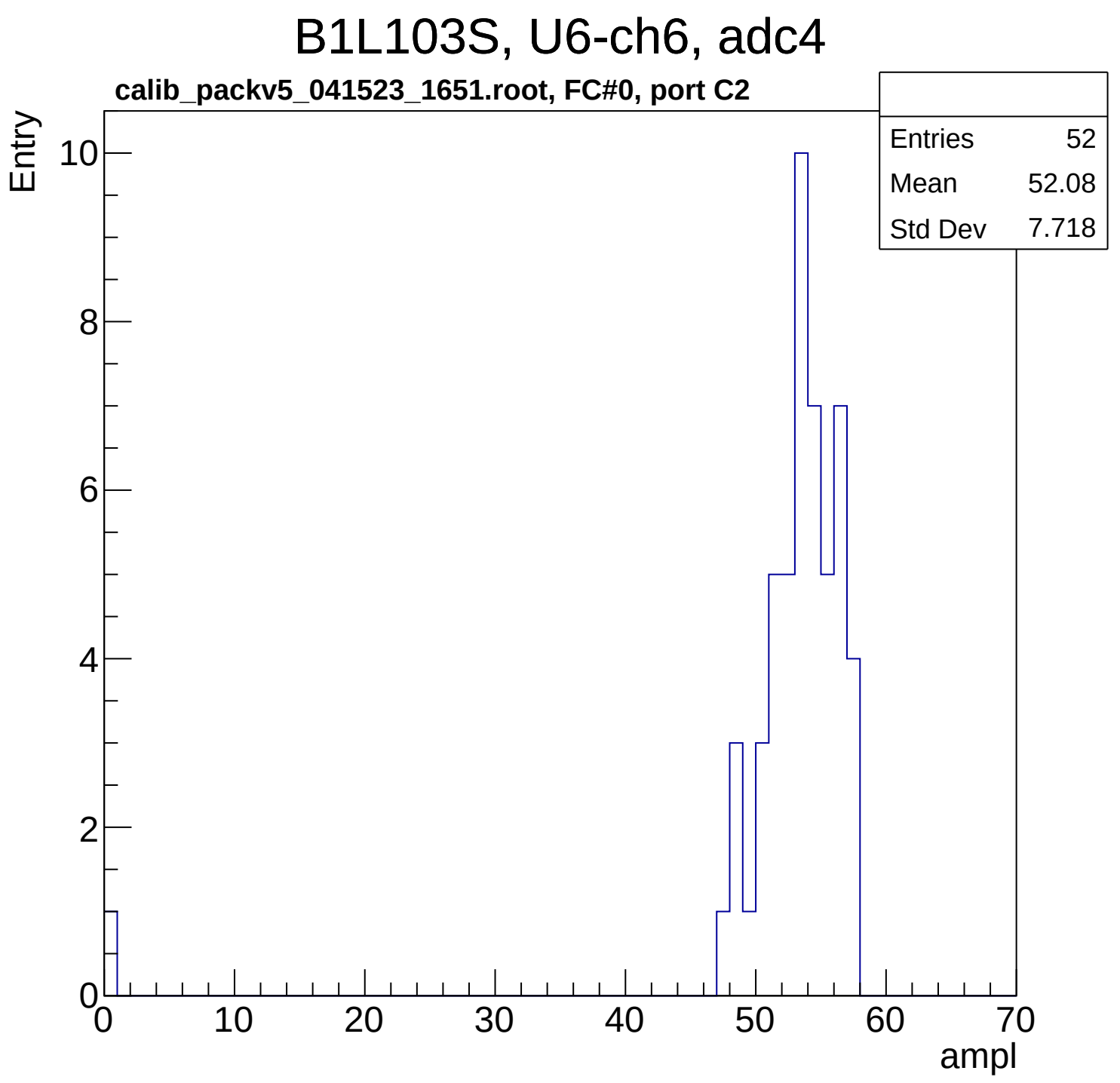
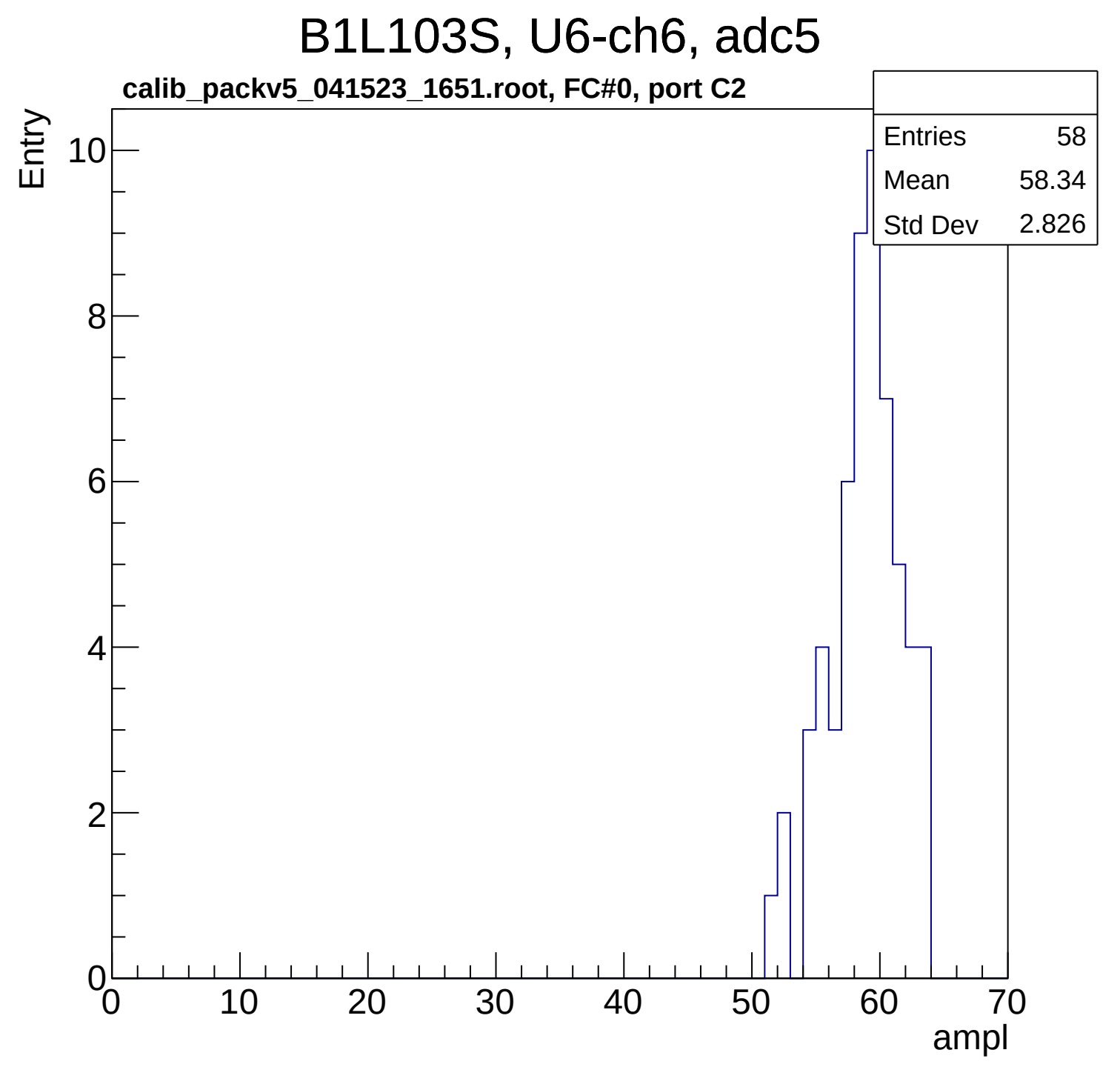
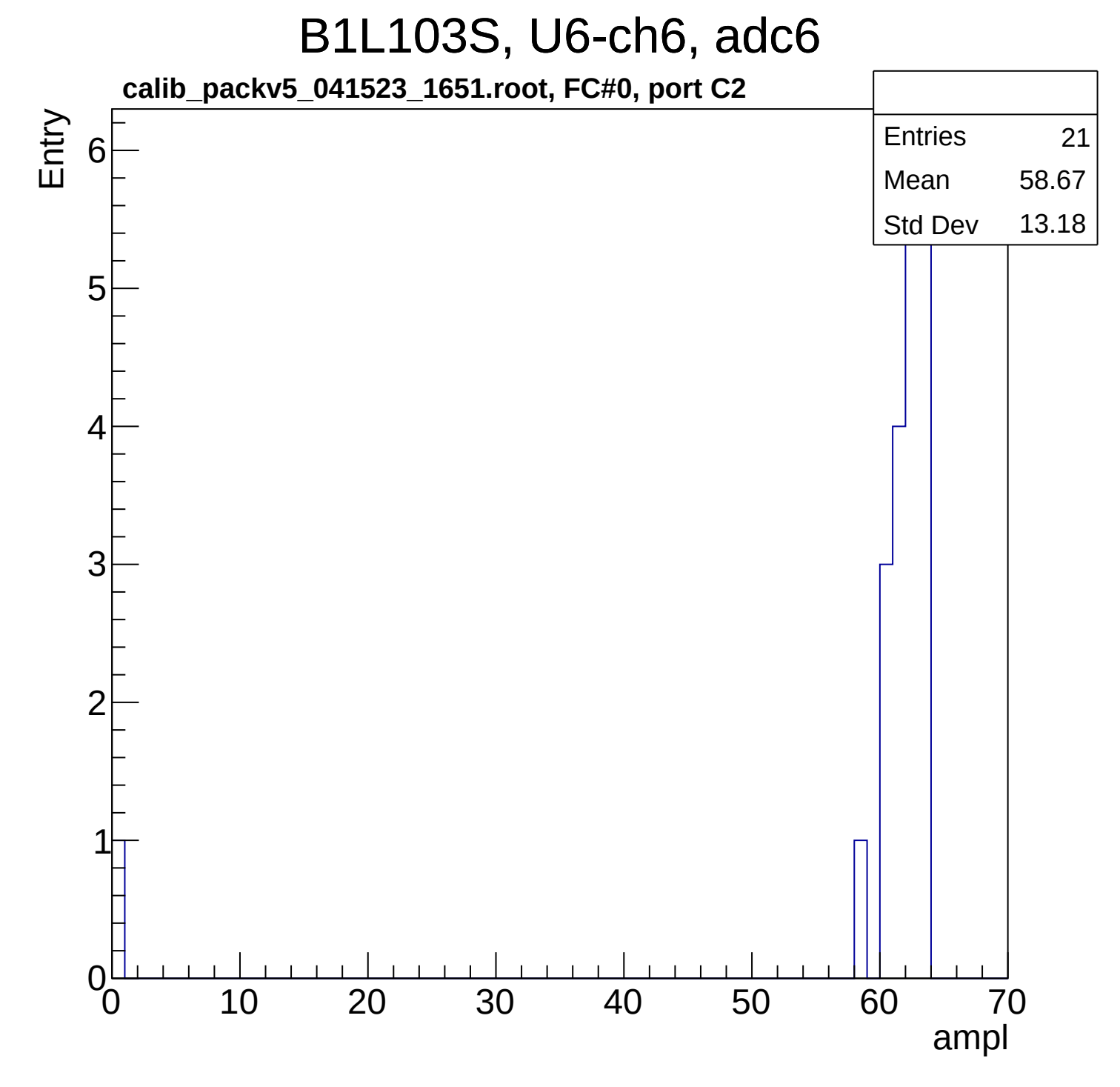
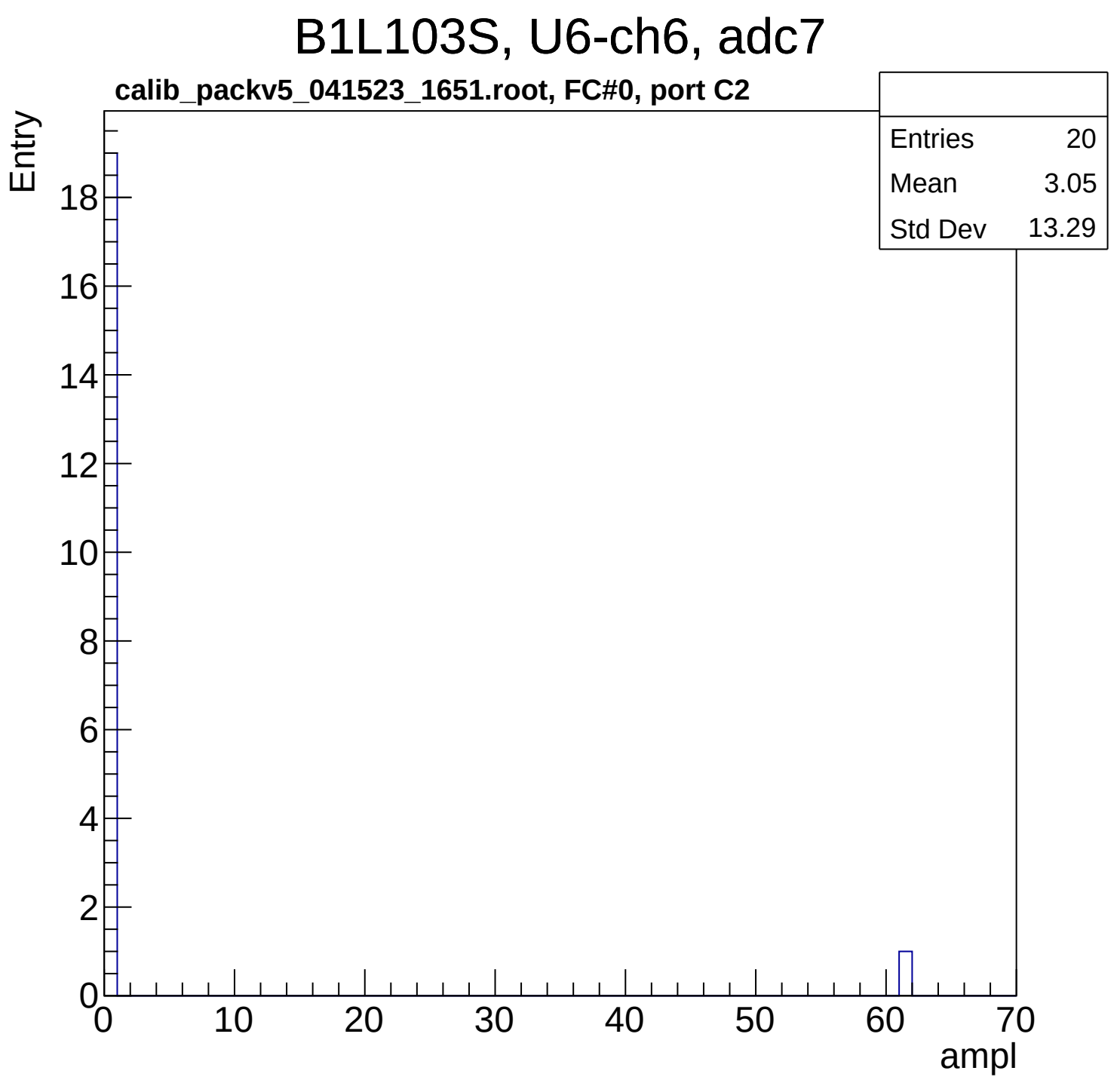
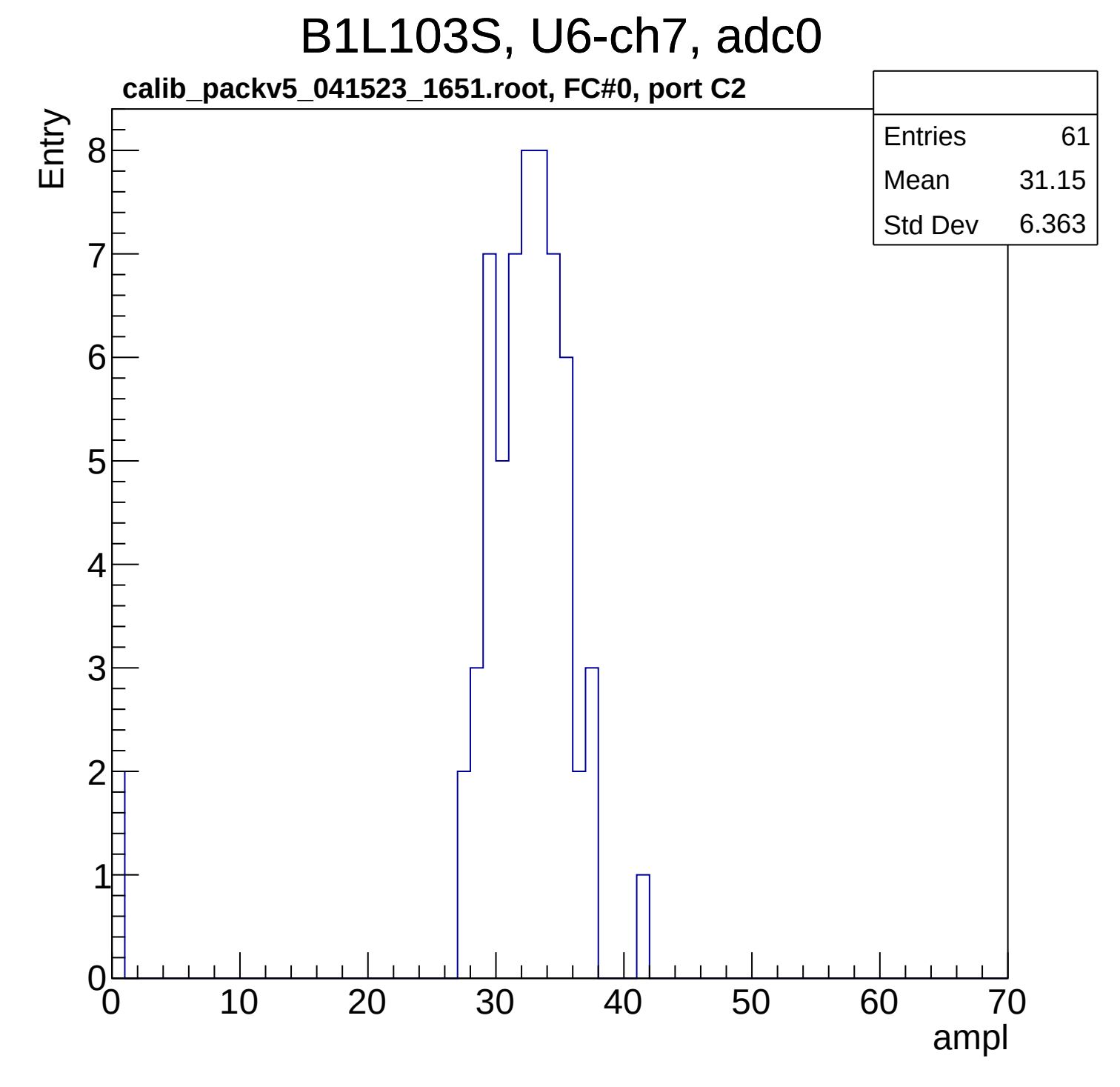
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

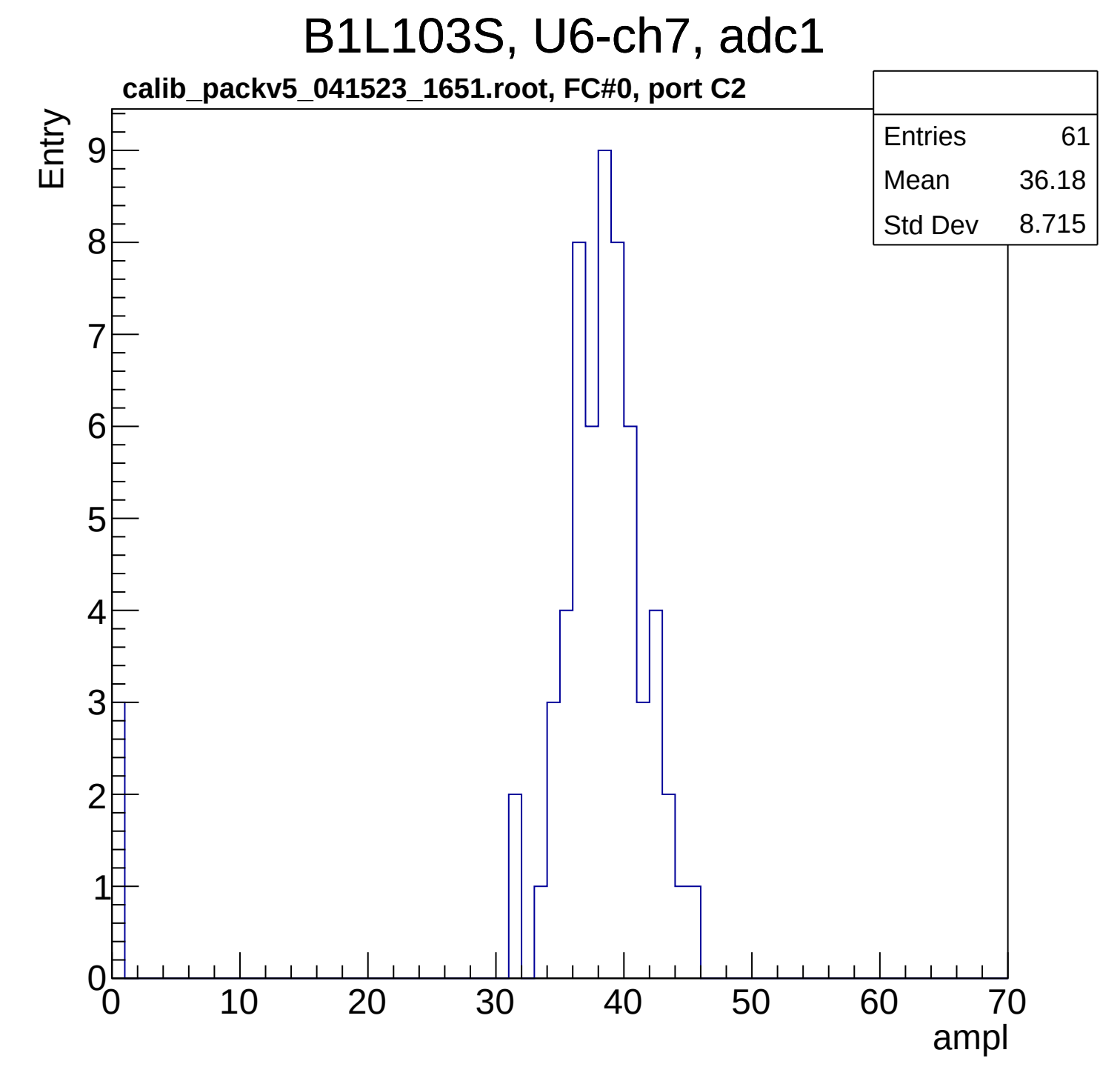

B1L103S, U6-ch6, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 52.08
Std Dev 7.718
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U6-ch6, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 58.34
Std Dev 2.826
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U6-ch6, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 58.67
Std Dev 13.18
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch6, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.05
Std Dev 13.29
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch7, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 31.15
Std Dev 6.363
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch7, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 36.18
Std Dev 8.715
Entry
ampl
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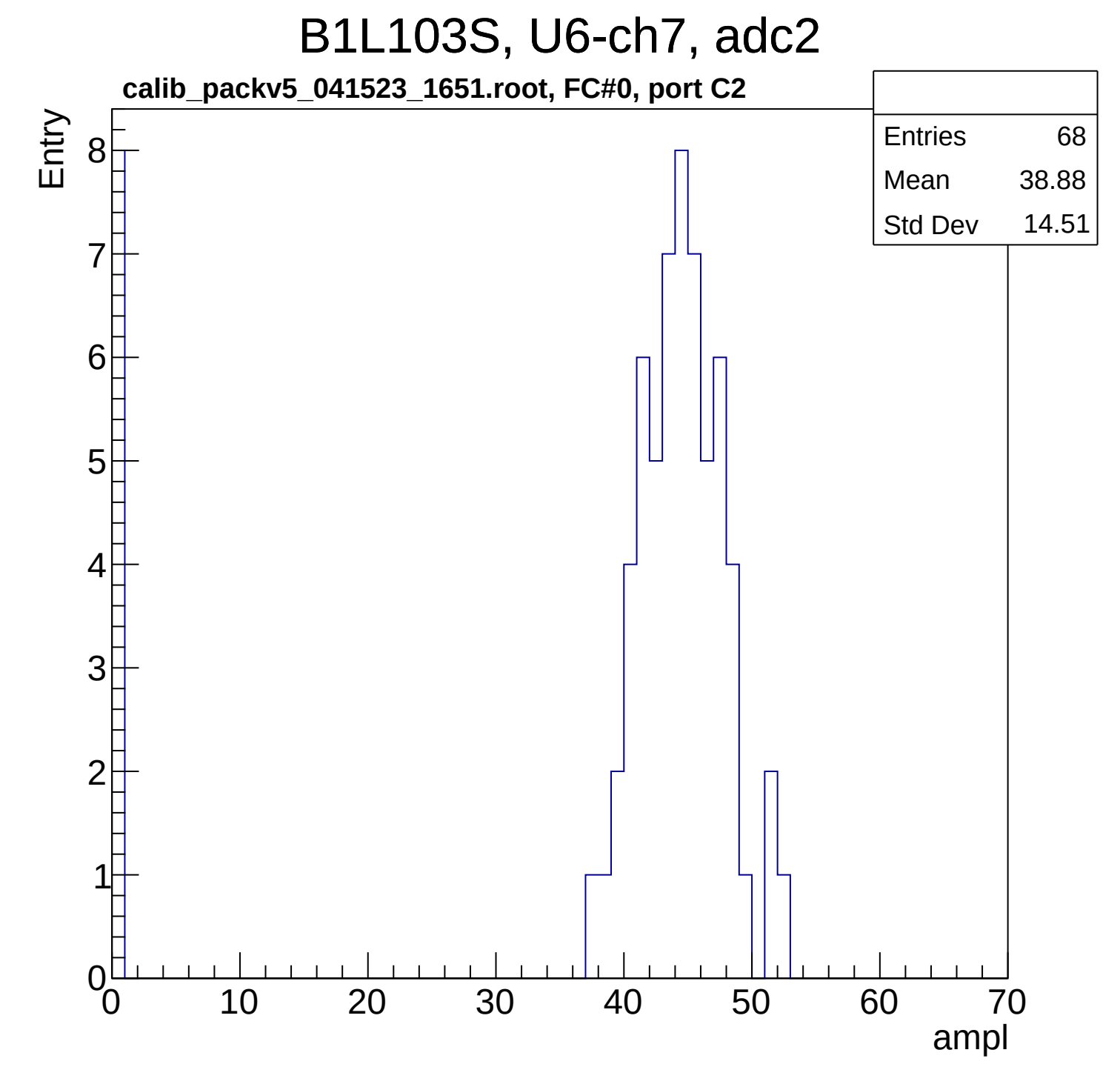
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch7, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 38.88
Std Dev 14.51
Entry
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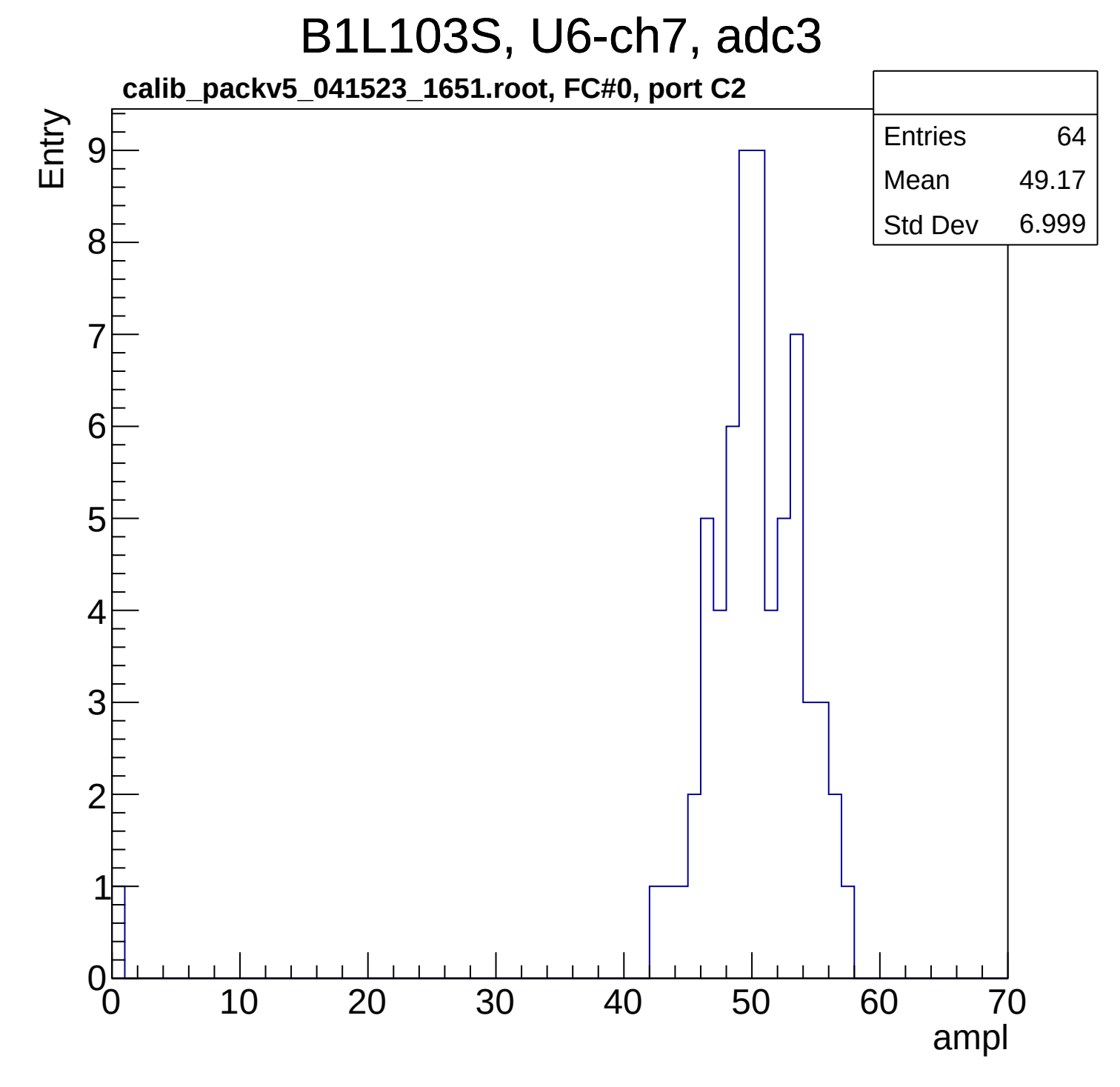
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch7, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 49.17
Std Dev 6.999
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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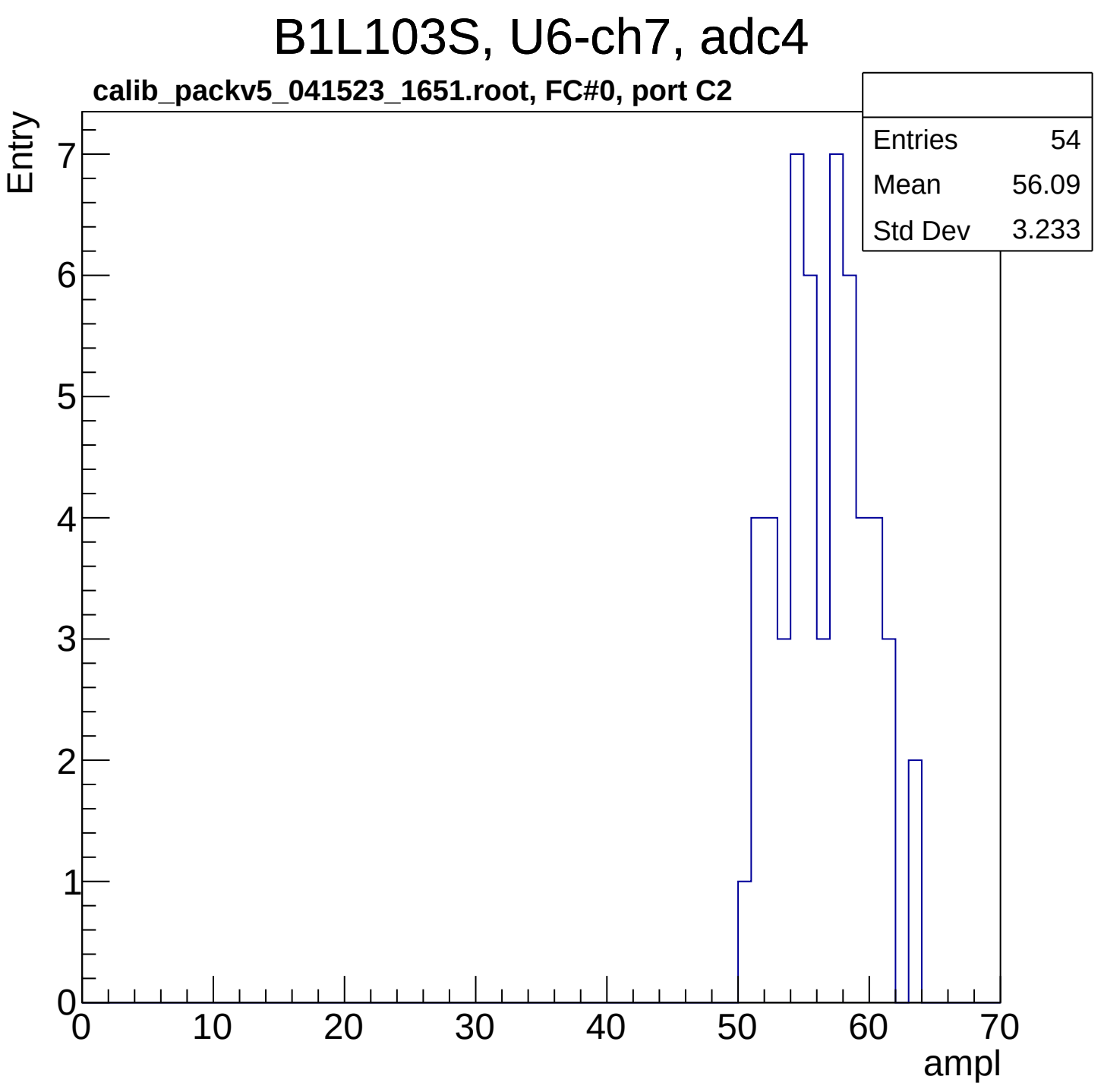
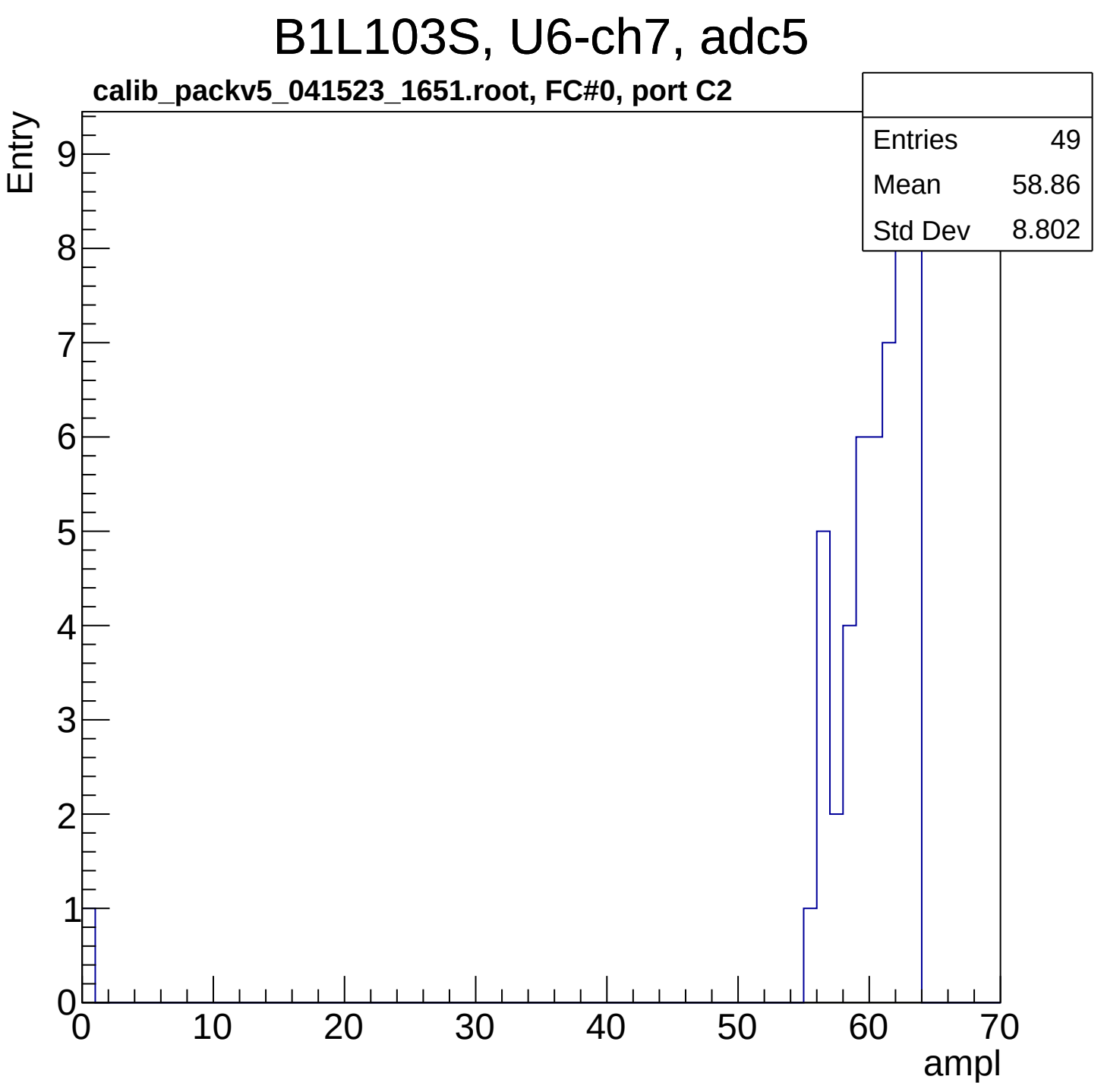
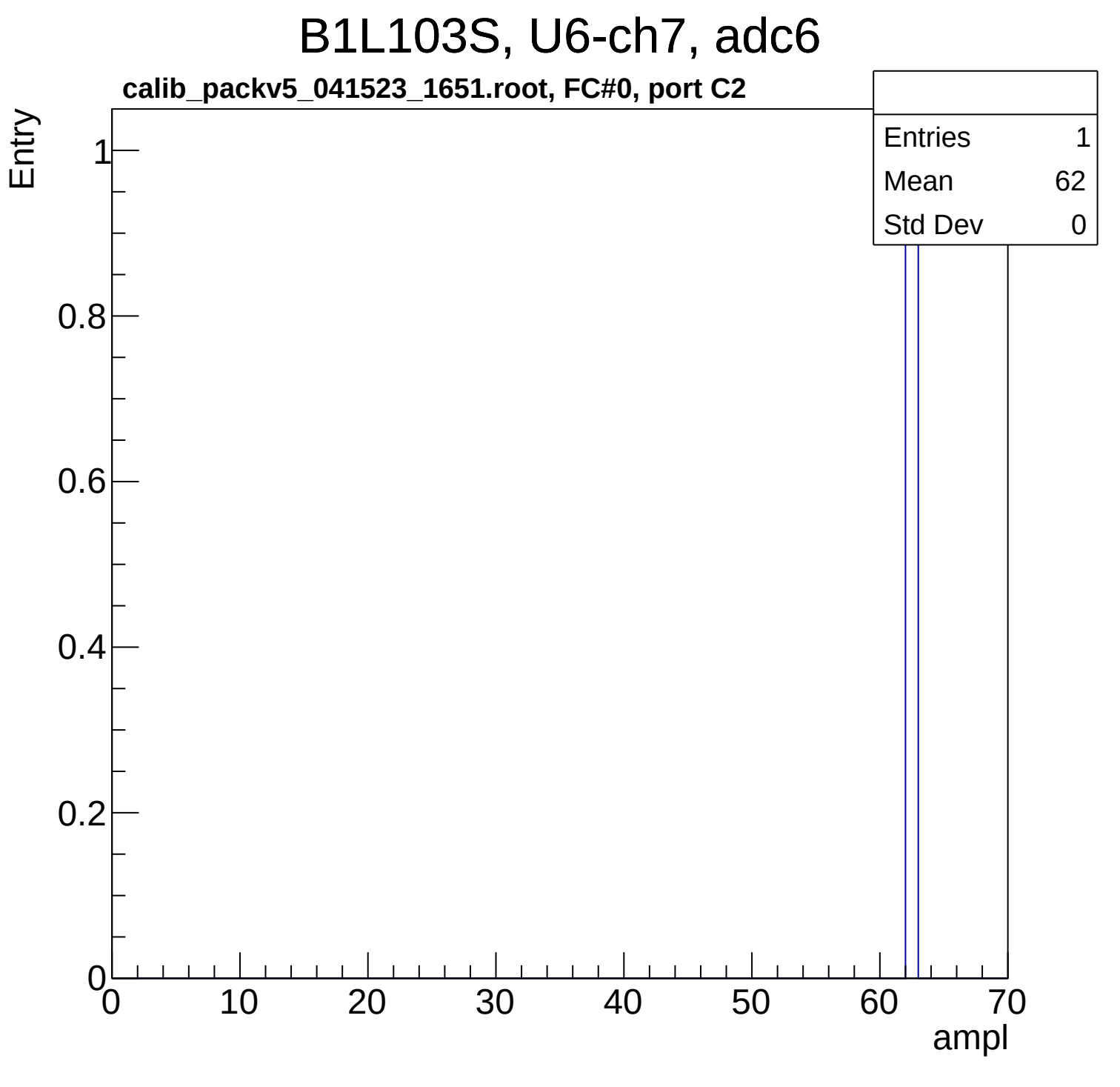
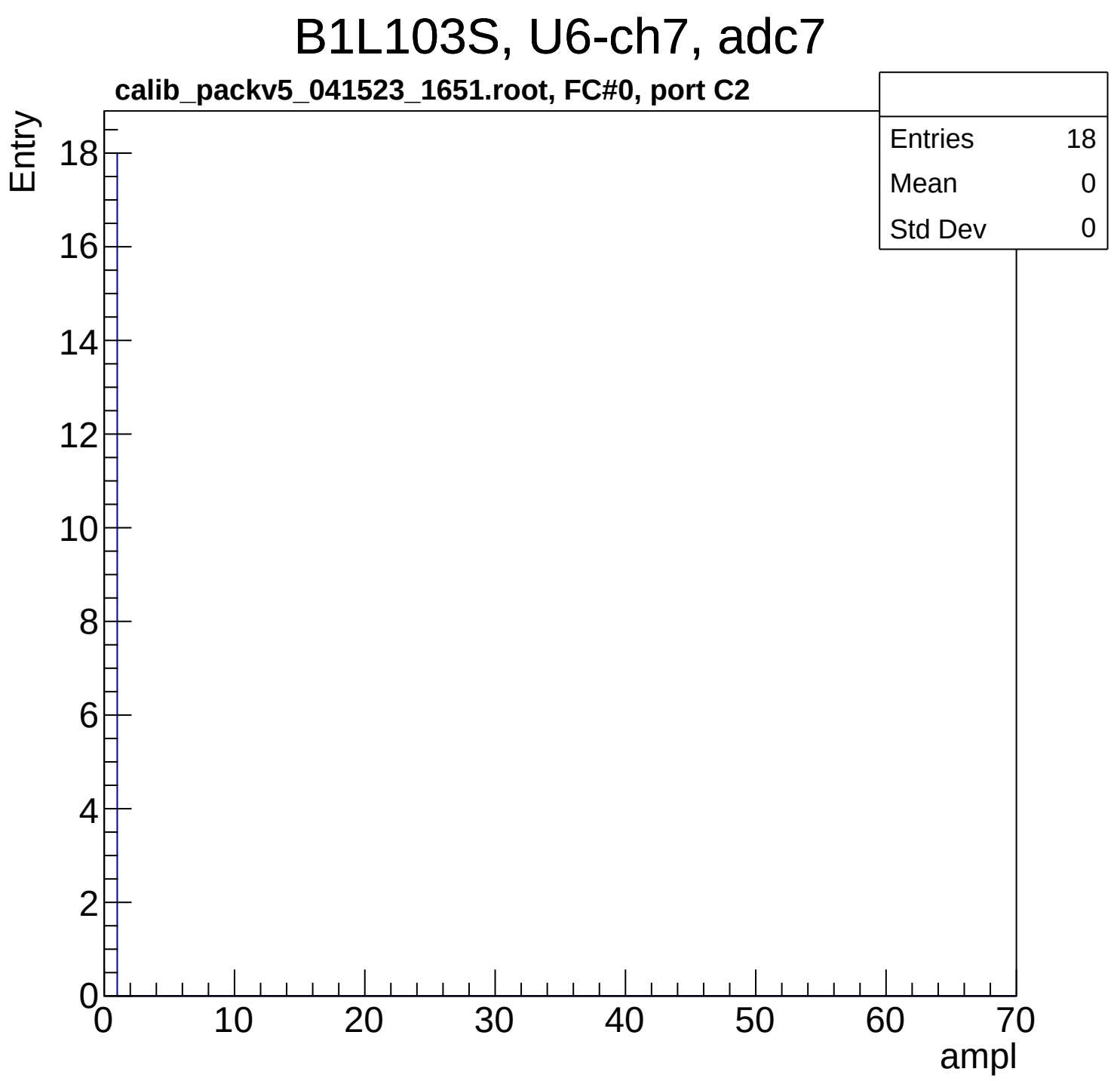

B1L103S, U6-ch7, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 56.09
Std Dev 3.233
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U6-ch7, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 58.86
Std Dev 8.802
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch7, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 1
Mean 62
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch7, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
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2
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6
8
10
12
14
16
18
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10
20
30
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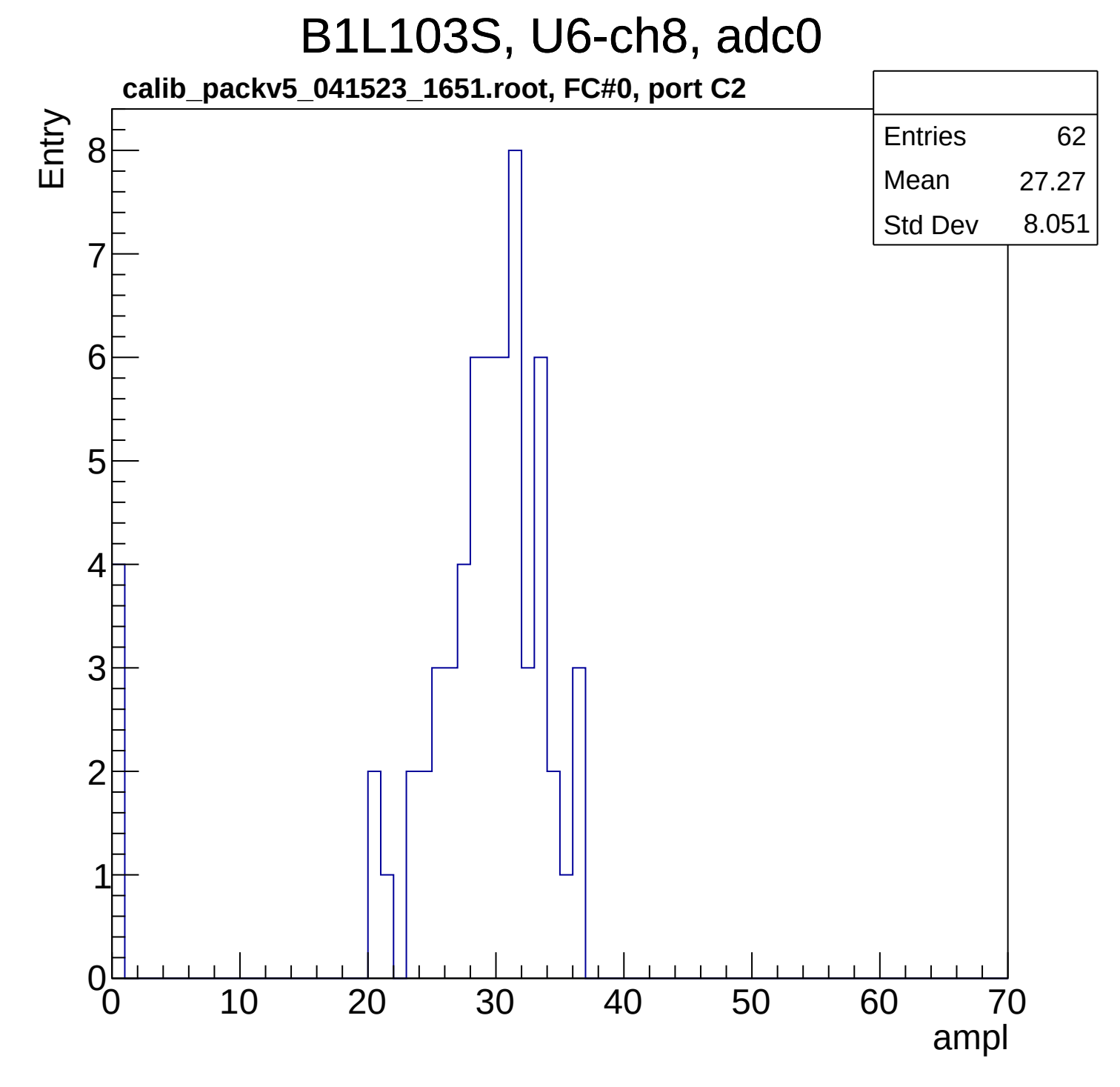
50
60
70
ampl


B1L103S, U6-ch8, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 27.27
Std Dev 8.051
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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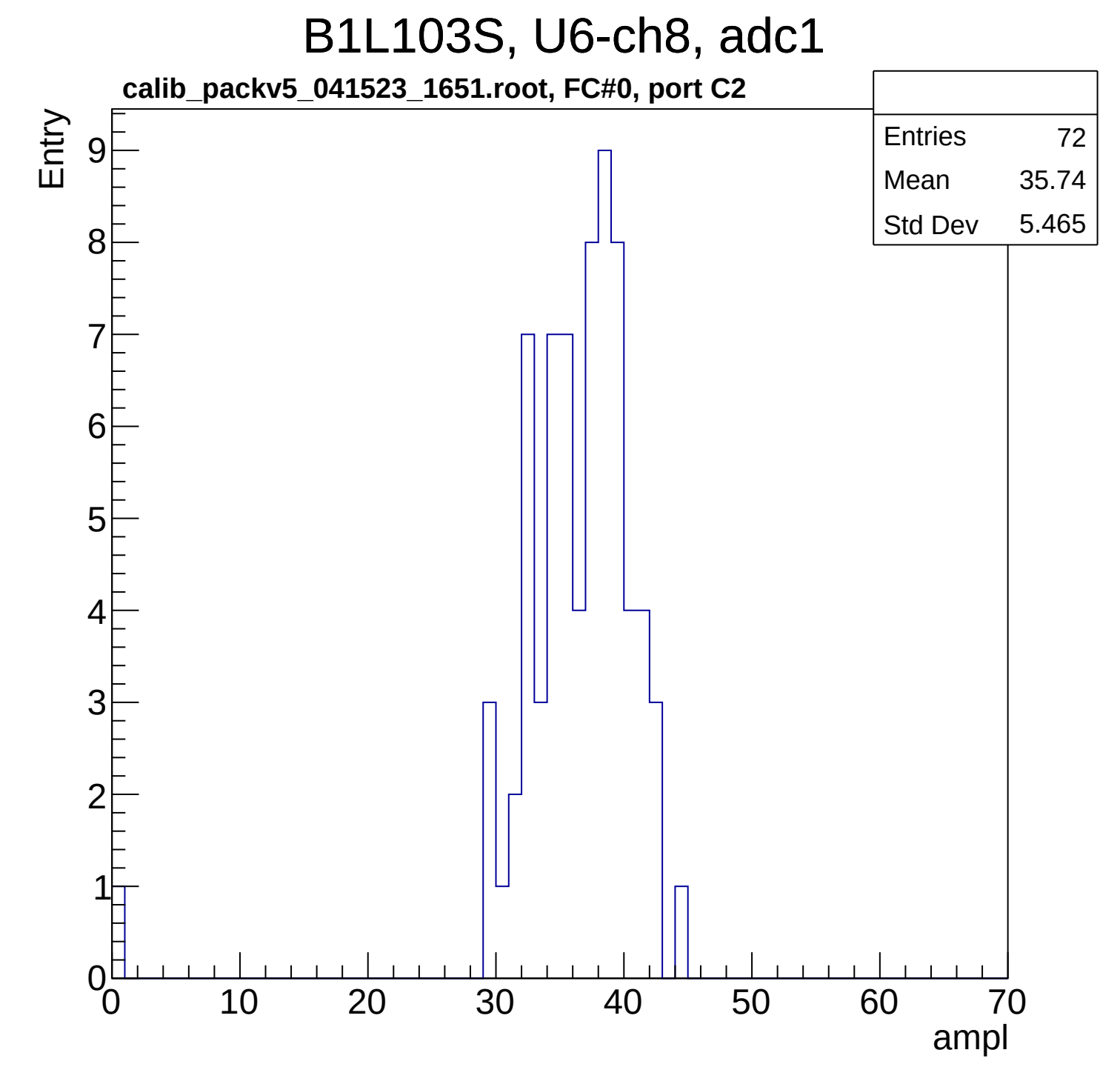
B1L103S, U6-ch8, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 35.74
Std Dev 5.465
Entry
ampl
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2
3
4
5
6
7
8
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0
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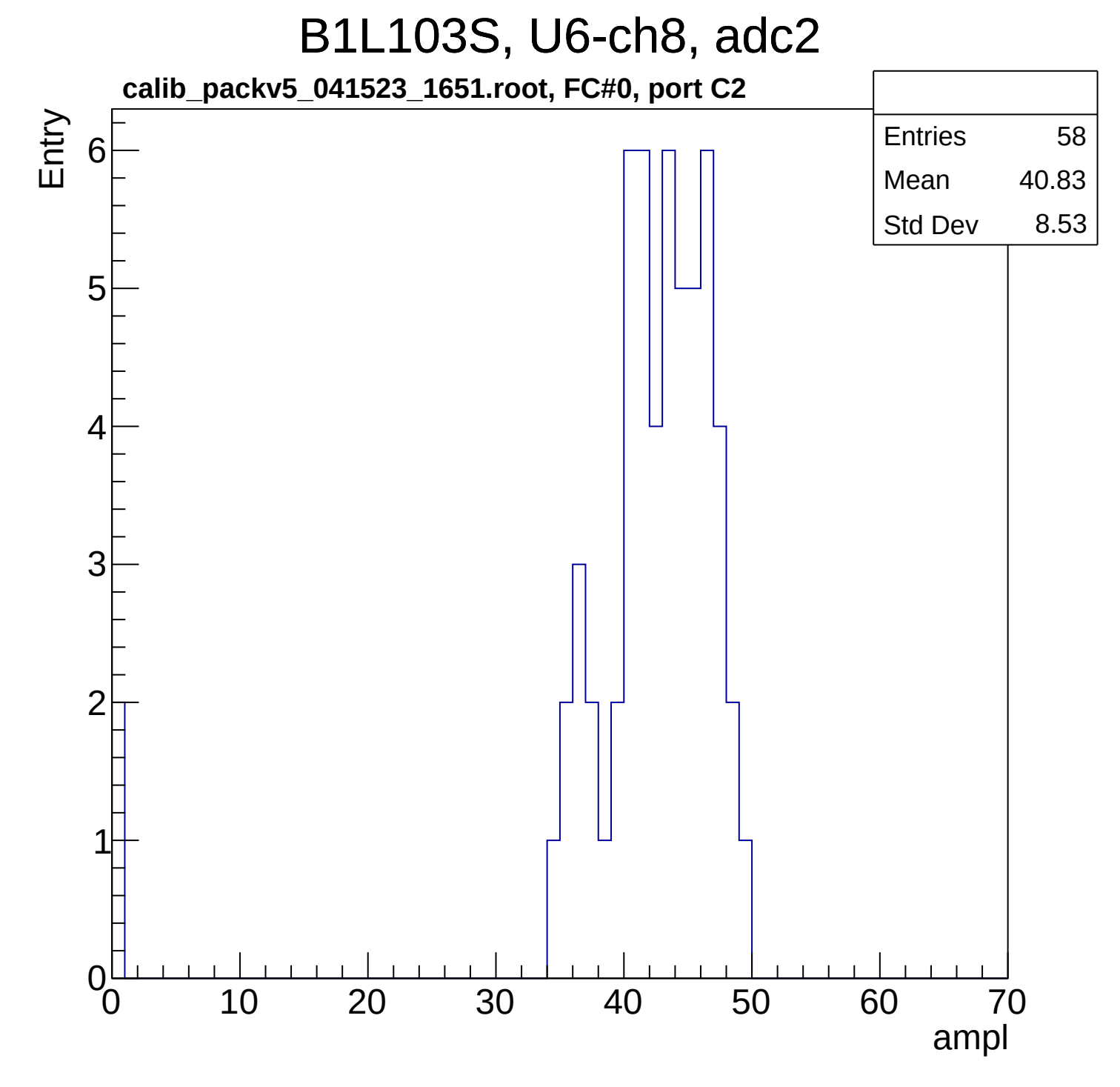
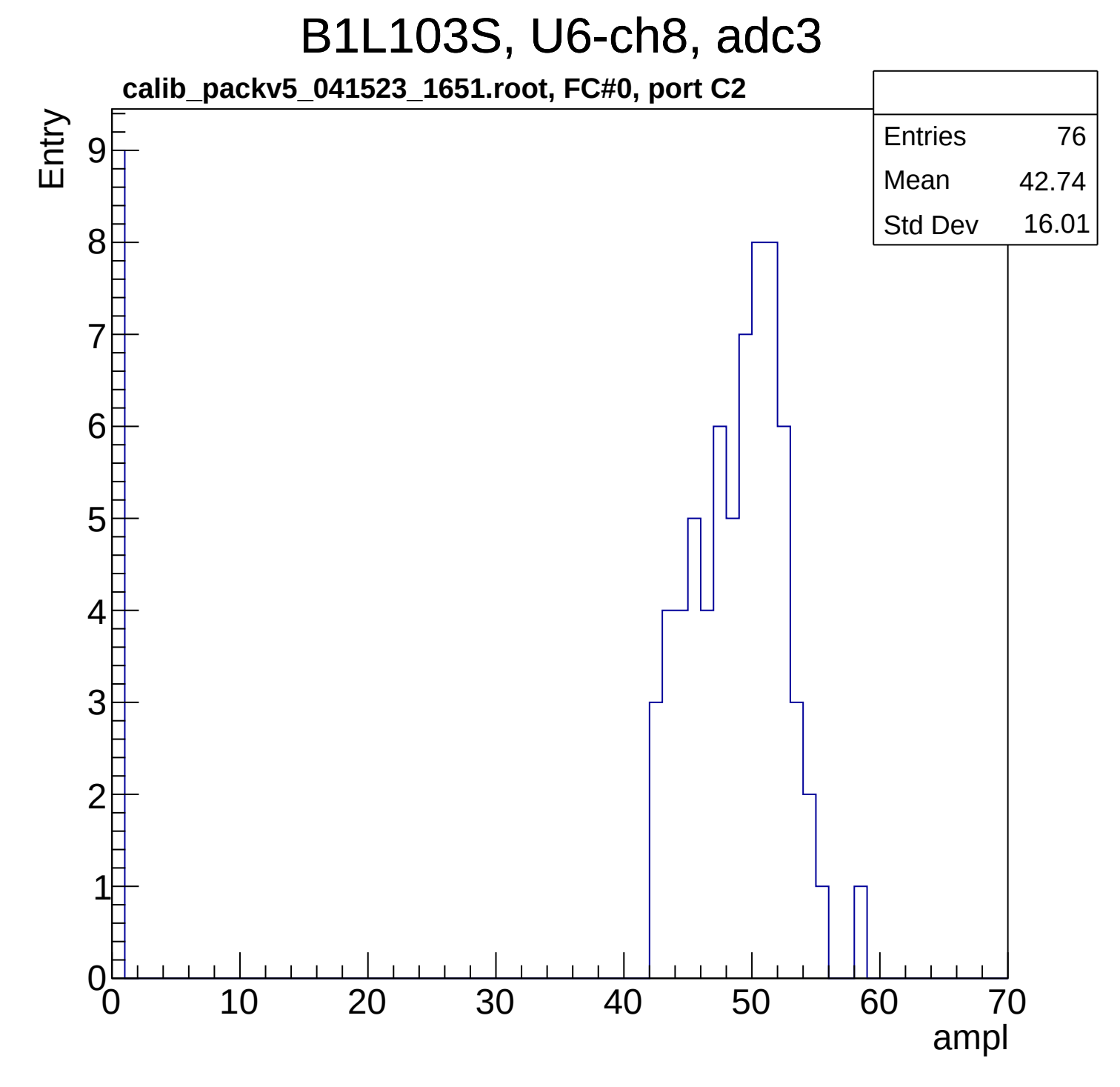

B1L103S, U6-ch8, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 40.83
Std Dev 8.53
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch8, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 42.74
Std Dev 16.01
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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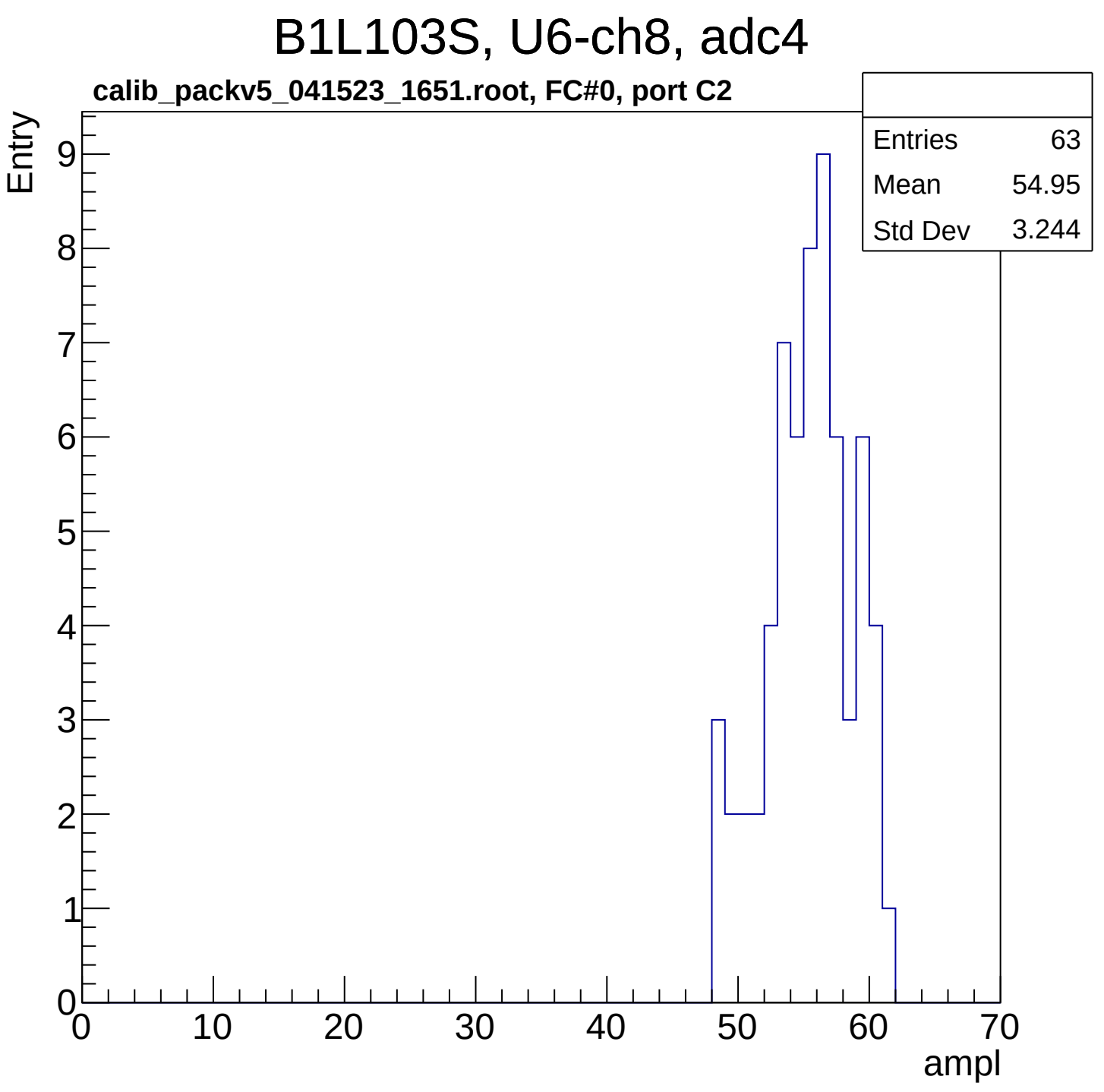
B1L103S, U6-ch8, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 54.95
Std Dev 3.244
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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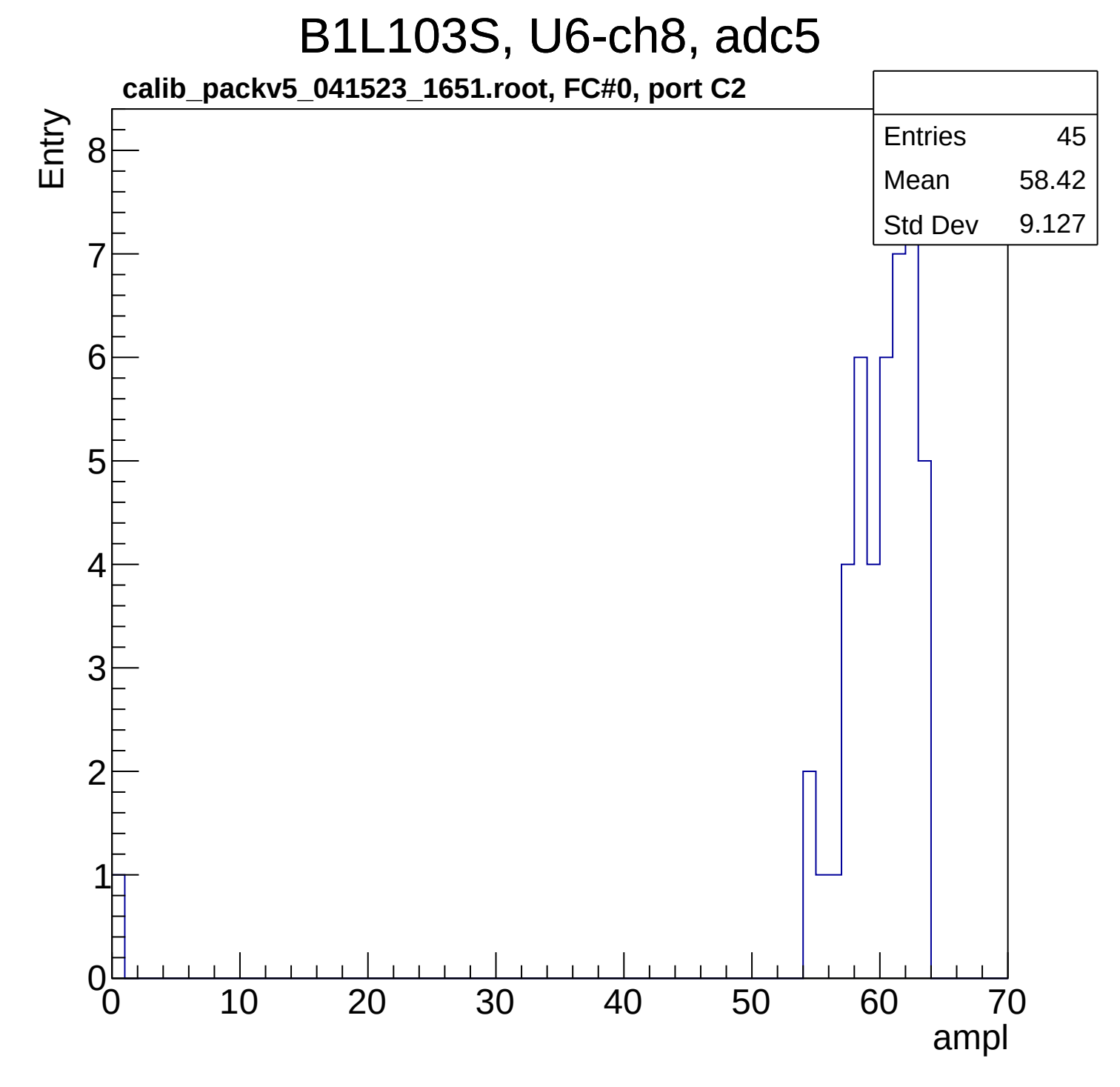
B1L103S, U6-ch8, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 58.42
Std Dev 9.127
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
50
60
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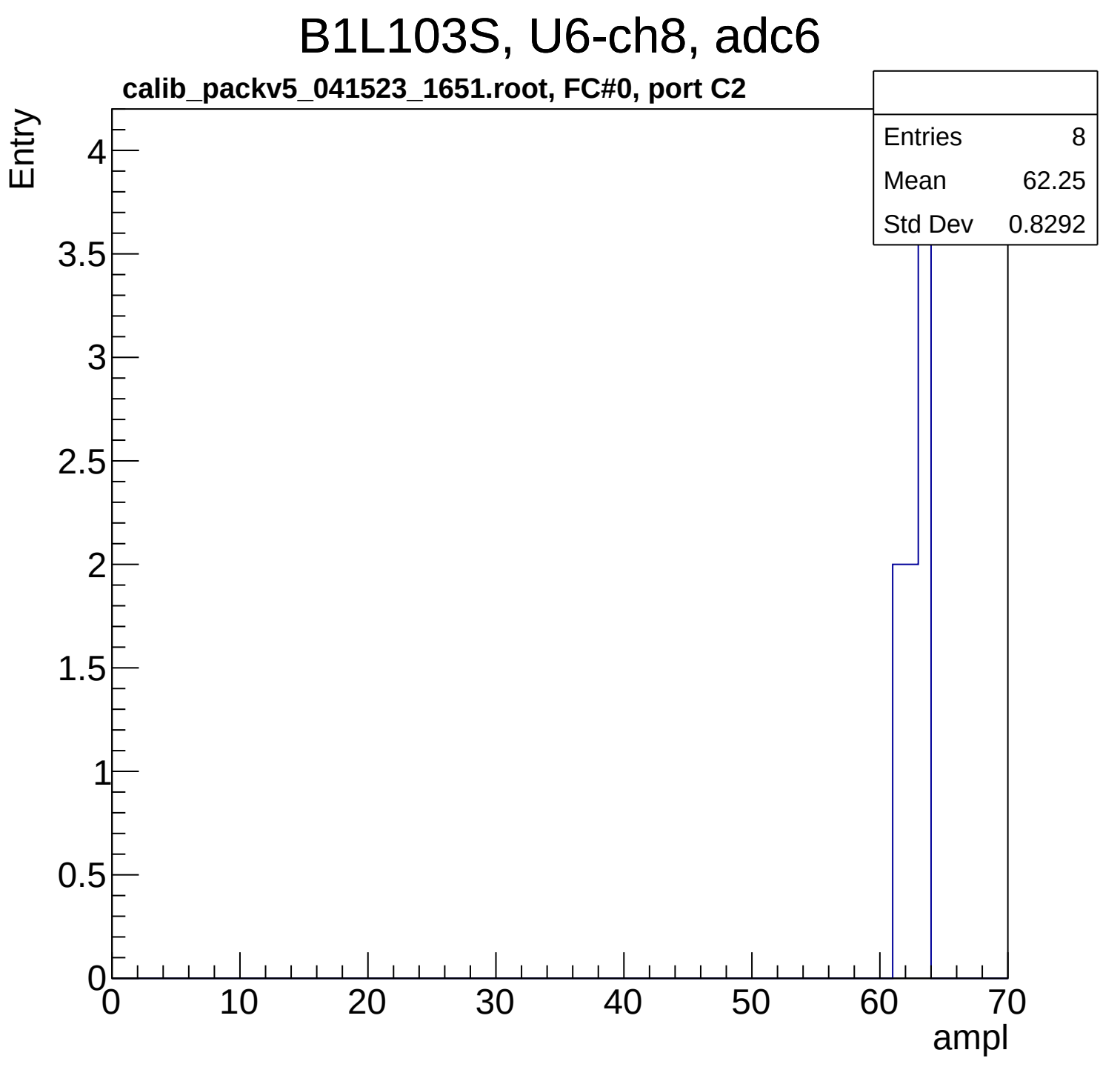
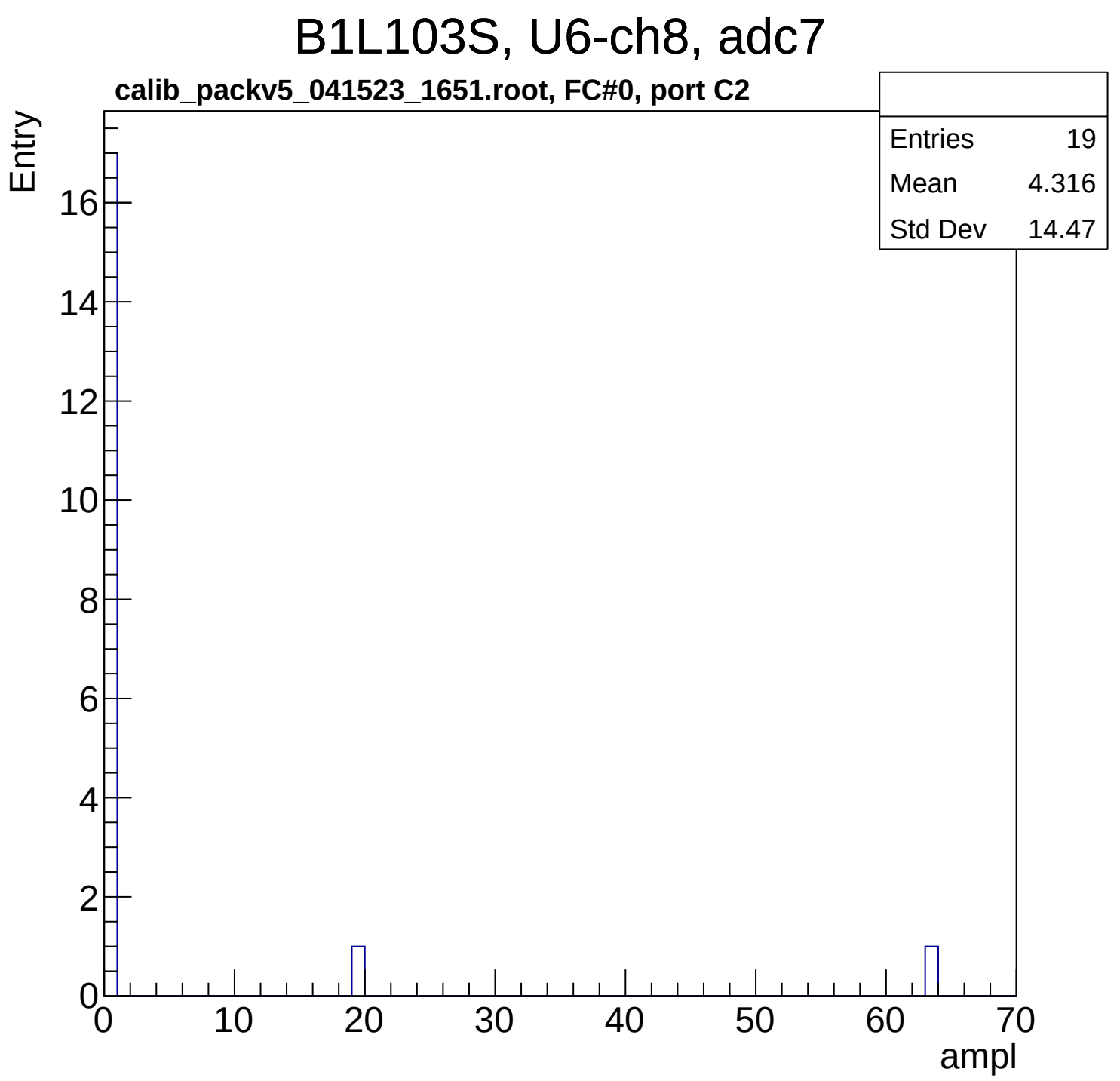
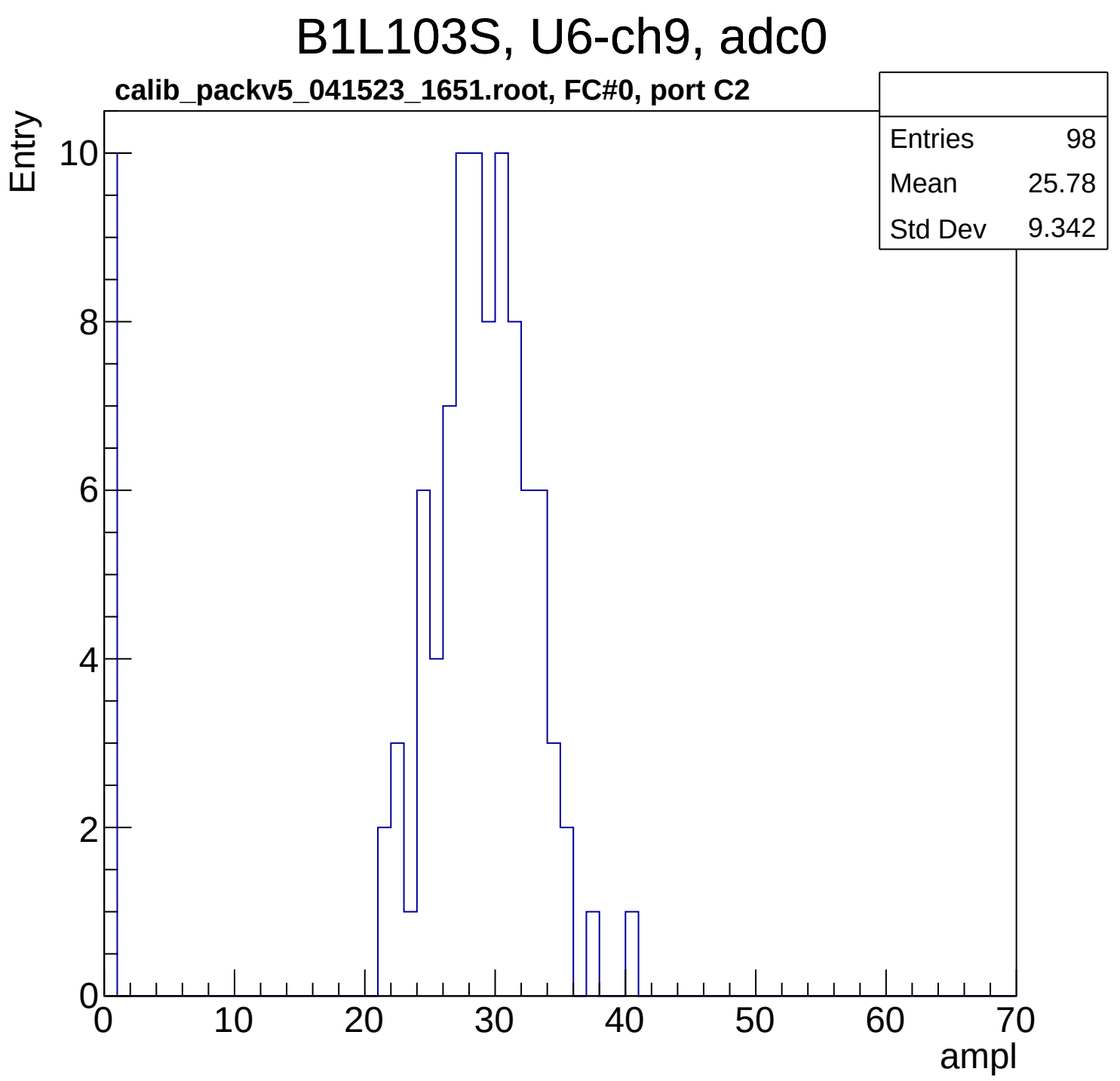
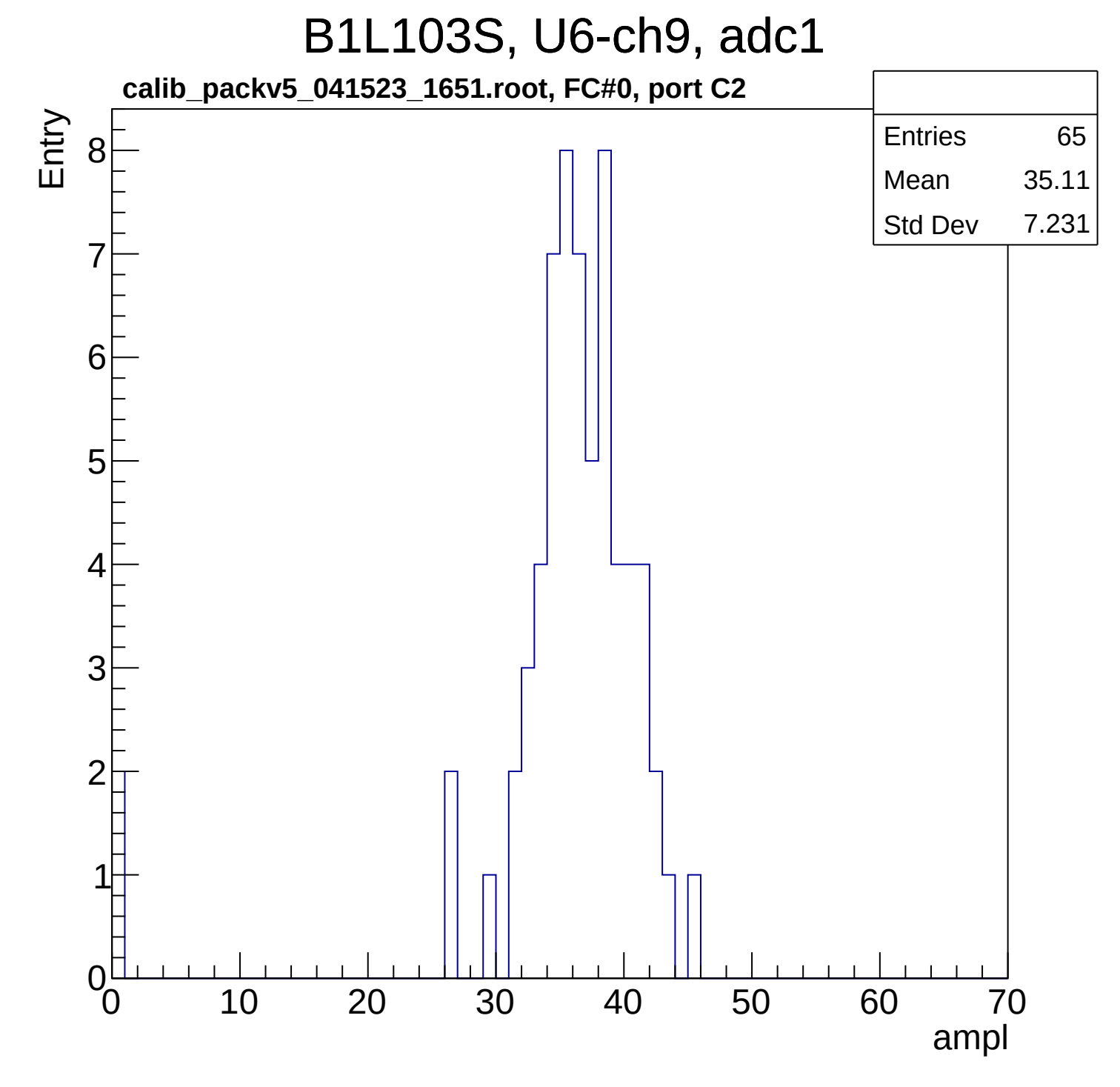

B1L103S, U6-ch8, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 62.25
Std Dev 0.8292
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U6-ch8, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 4.316
Std Dev 14.47
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch9, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 98
Mean 25.78
Std Dev 9.342
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch9, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 35.11
Std Dev 7.231
Entry
ampl
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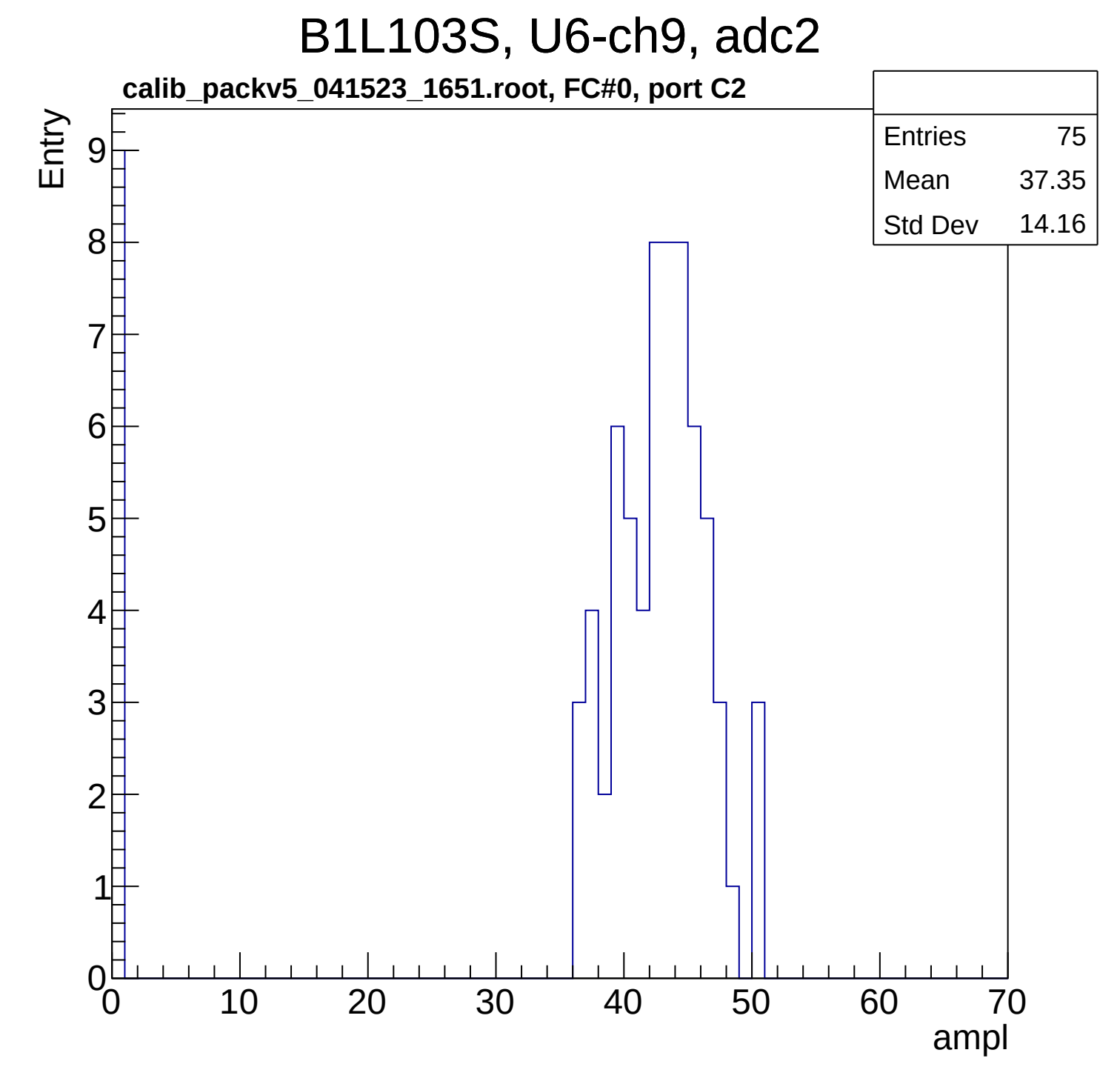
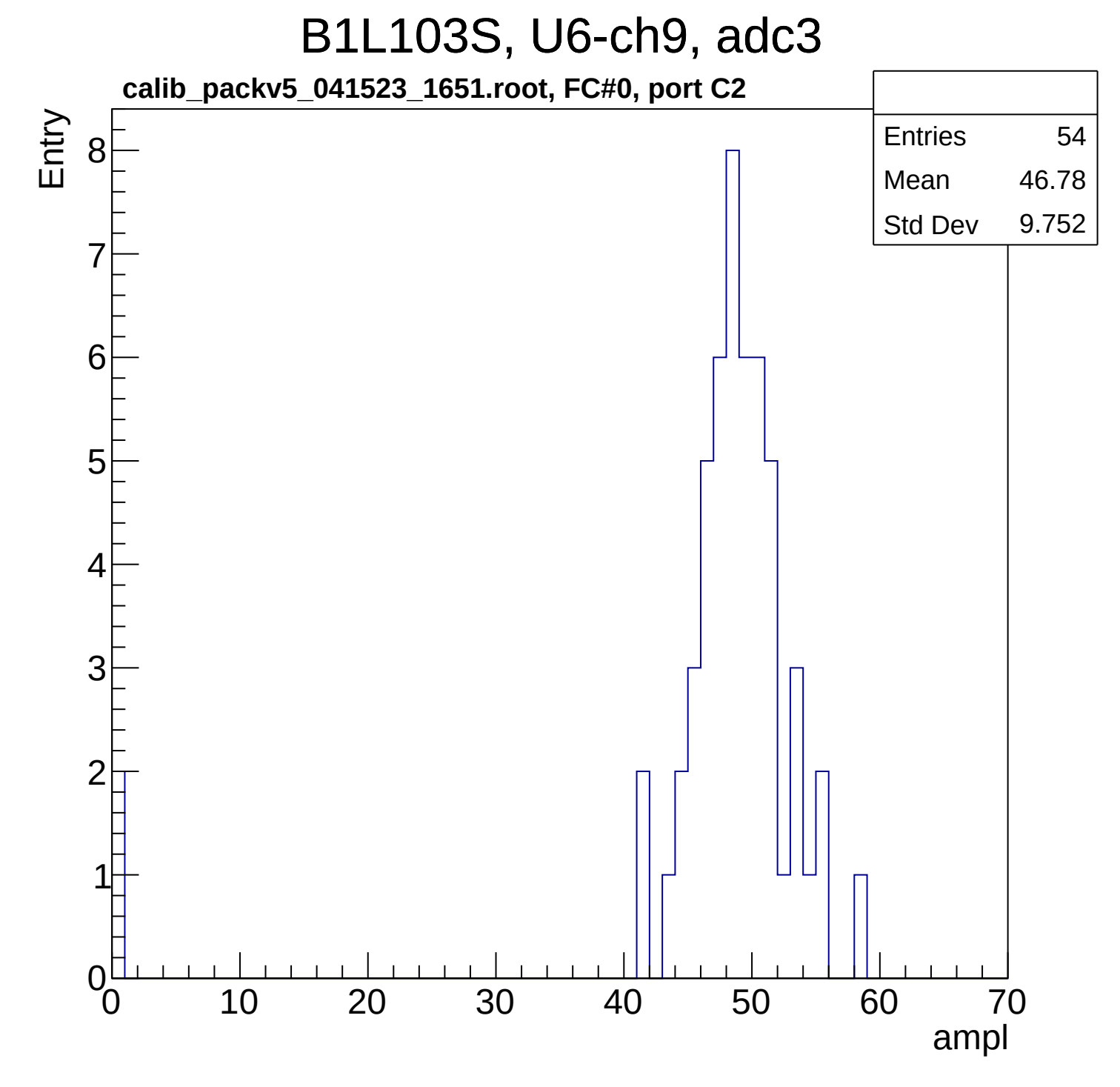
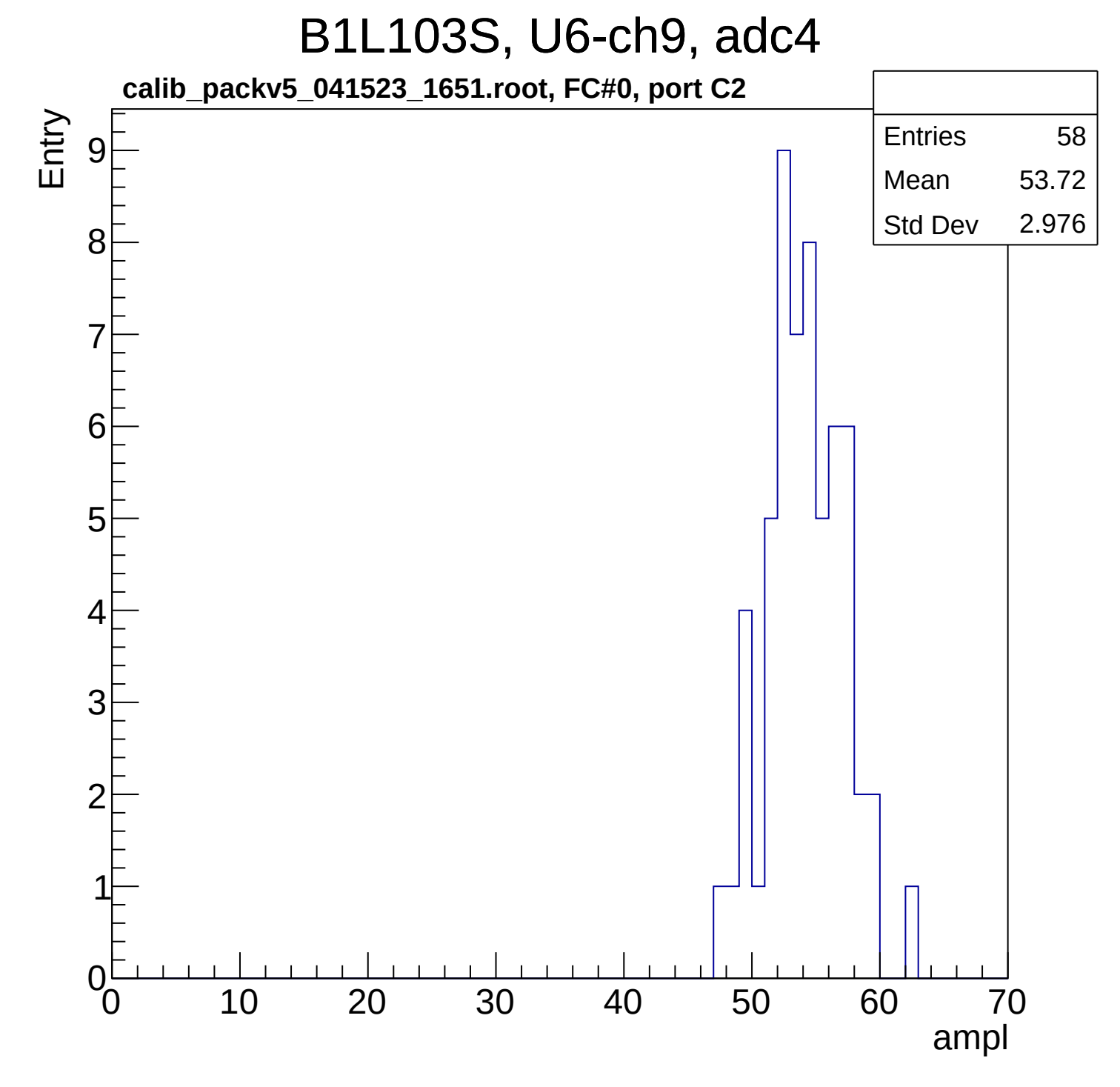
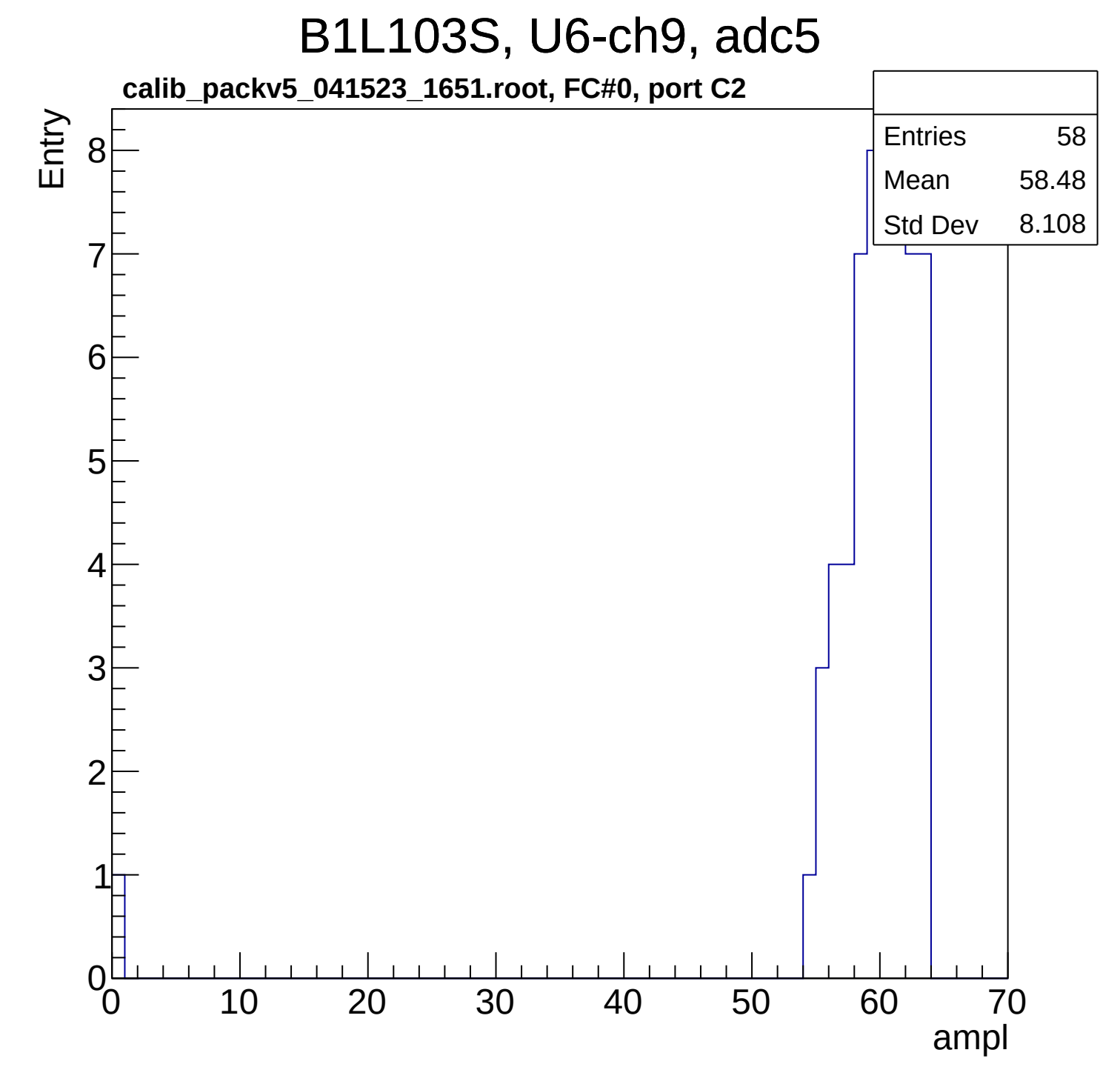
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch9, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 37.35
Std Dev 14.16
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch9, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 46.78
Std Dev 9.752
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch9, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 53.72
Std Dev 2.976
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch9, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 58.48
Std Dev 8.108
Entry
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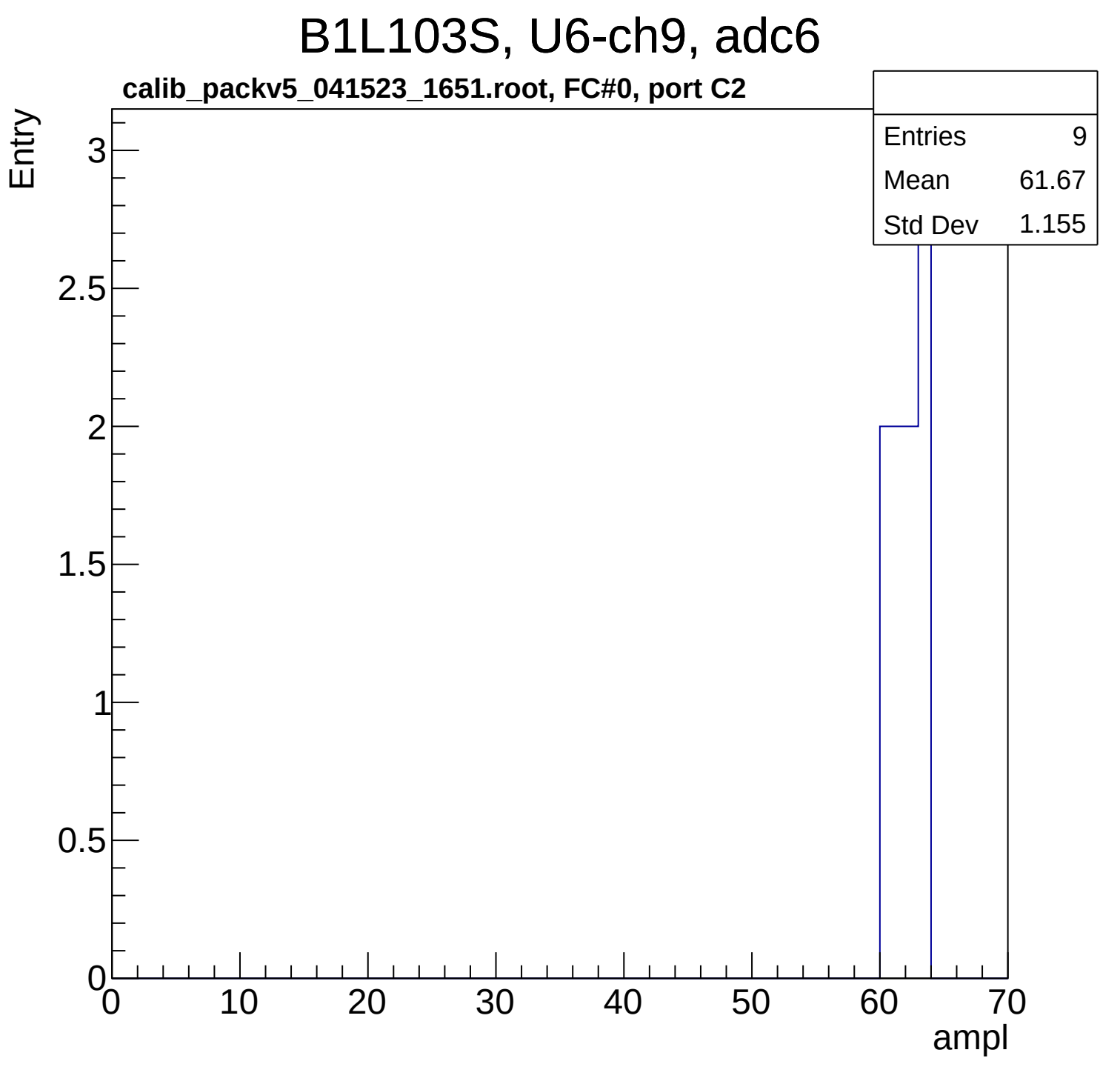
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch9, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 61.67
Std Dev 1.155
Entry
ampl
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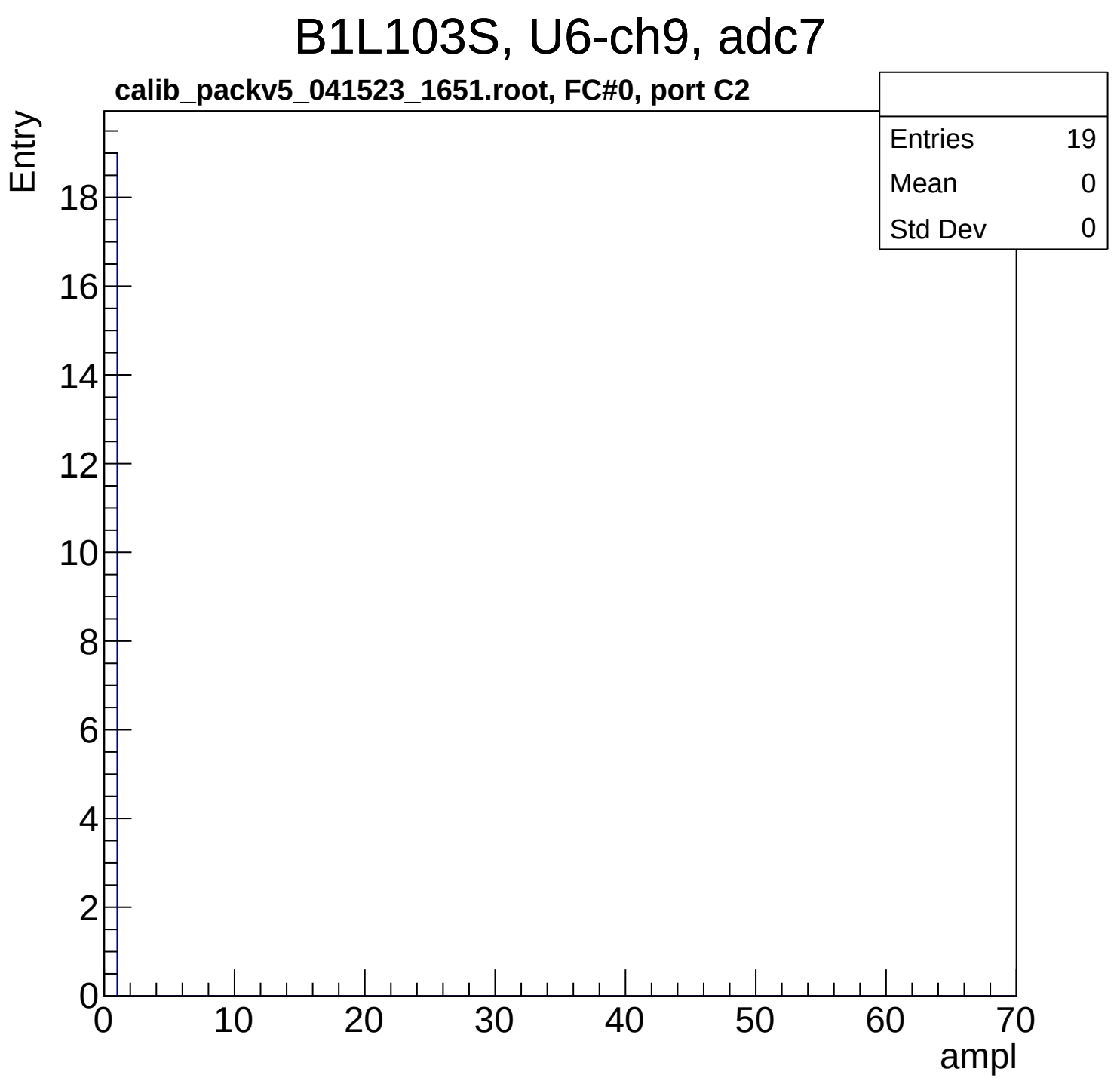
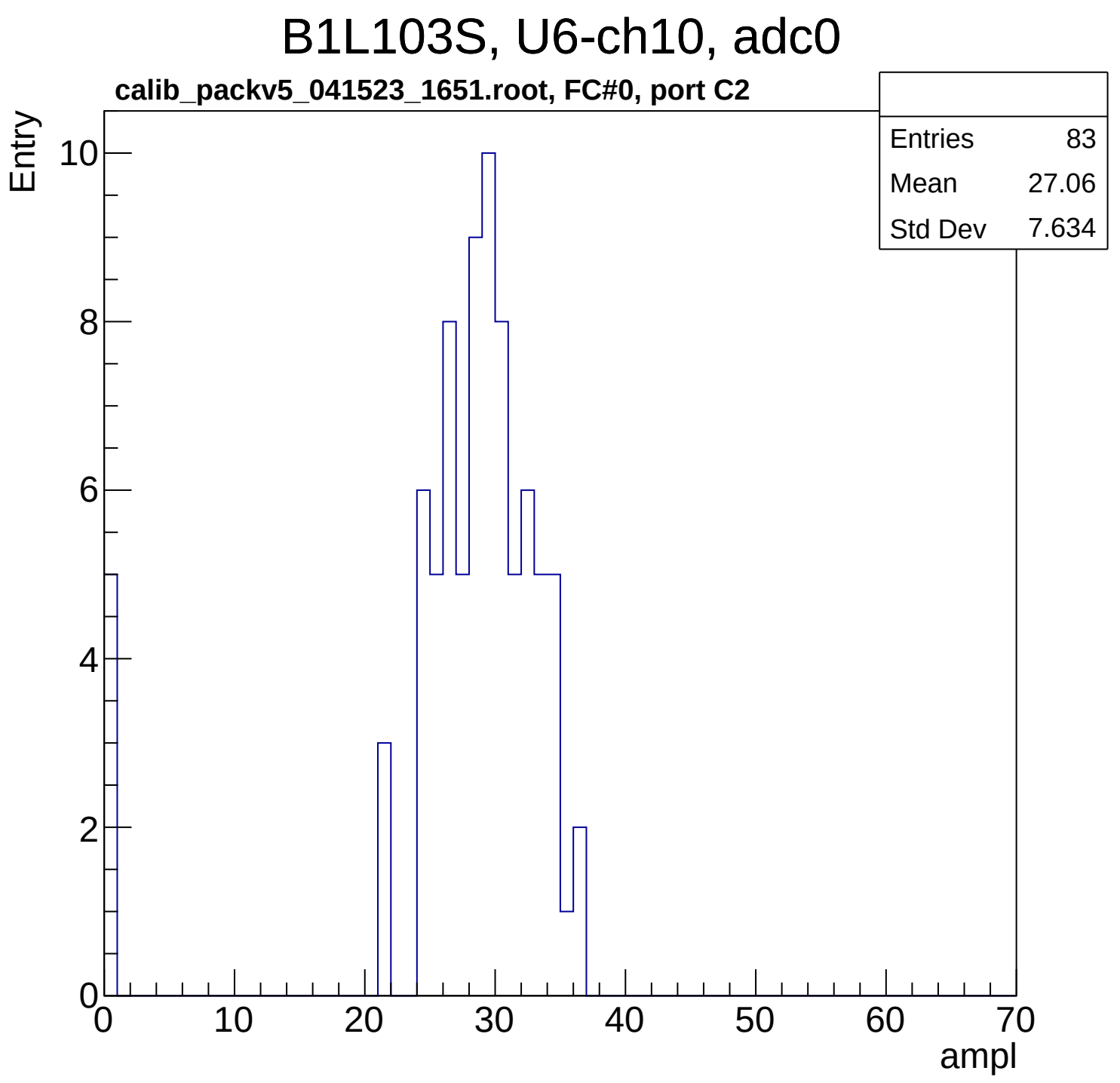
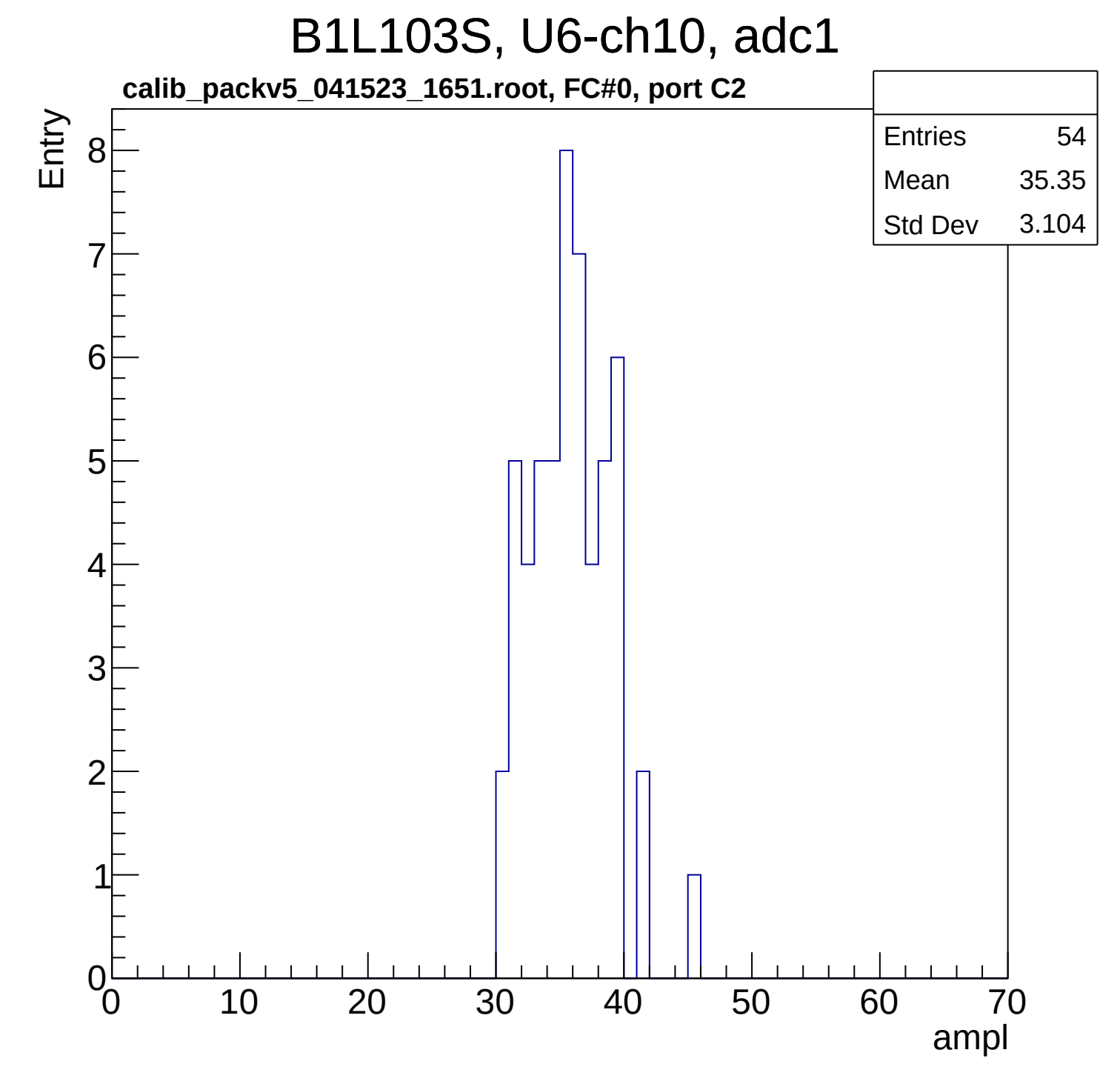
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U6-ch9, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch10, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 27.06
Std Dev 7.634
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U6-ch10, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 35.35
Std Dev 3.104
Entry
ampl
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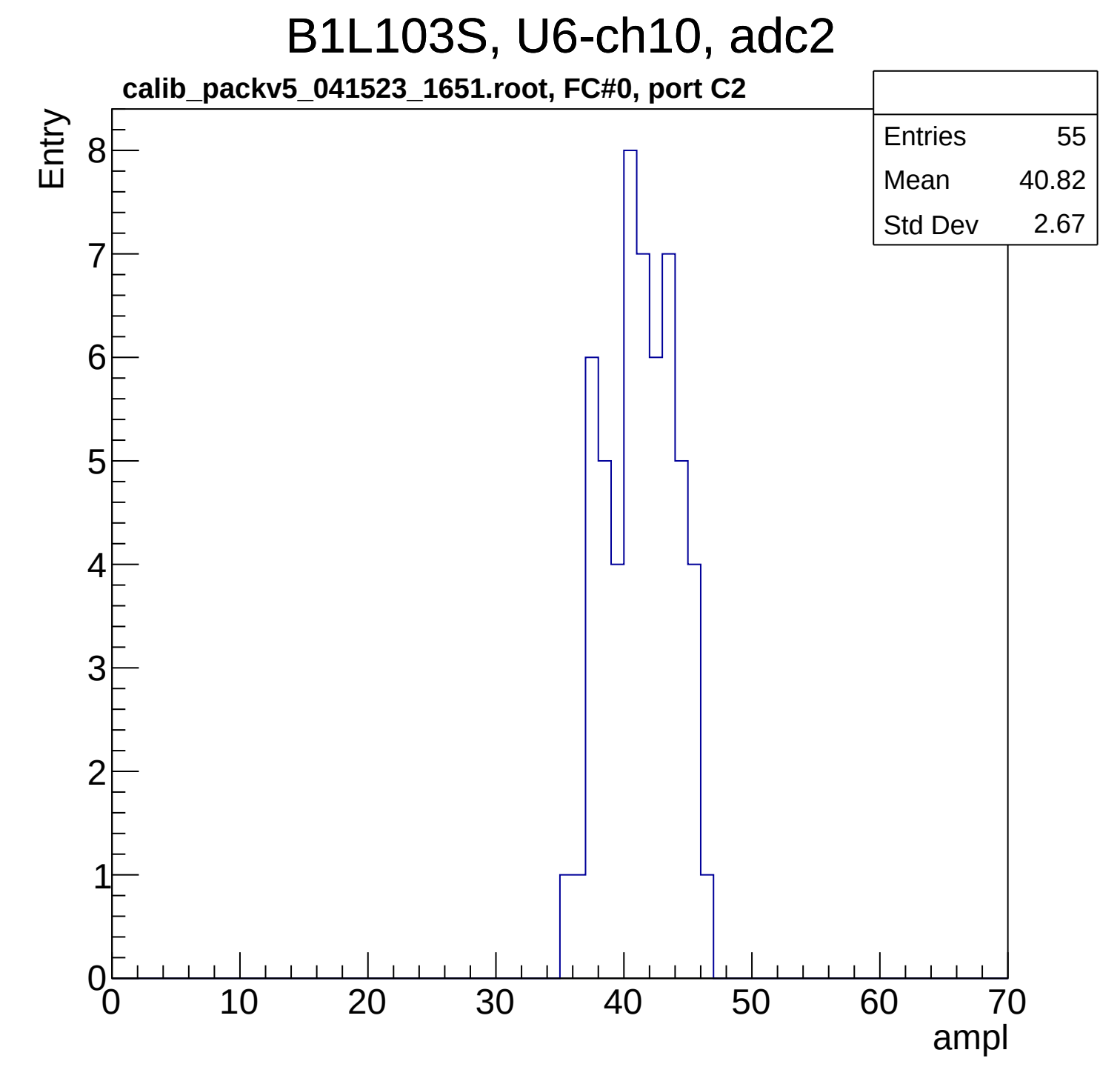
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch10, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 40.82
Std Dev 2.67
Entry
ampl
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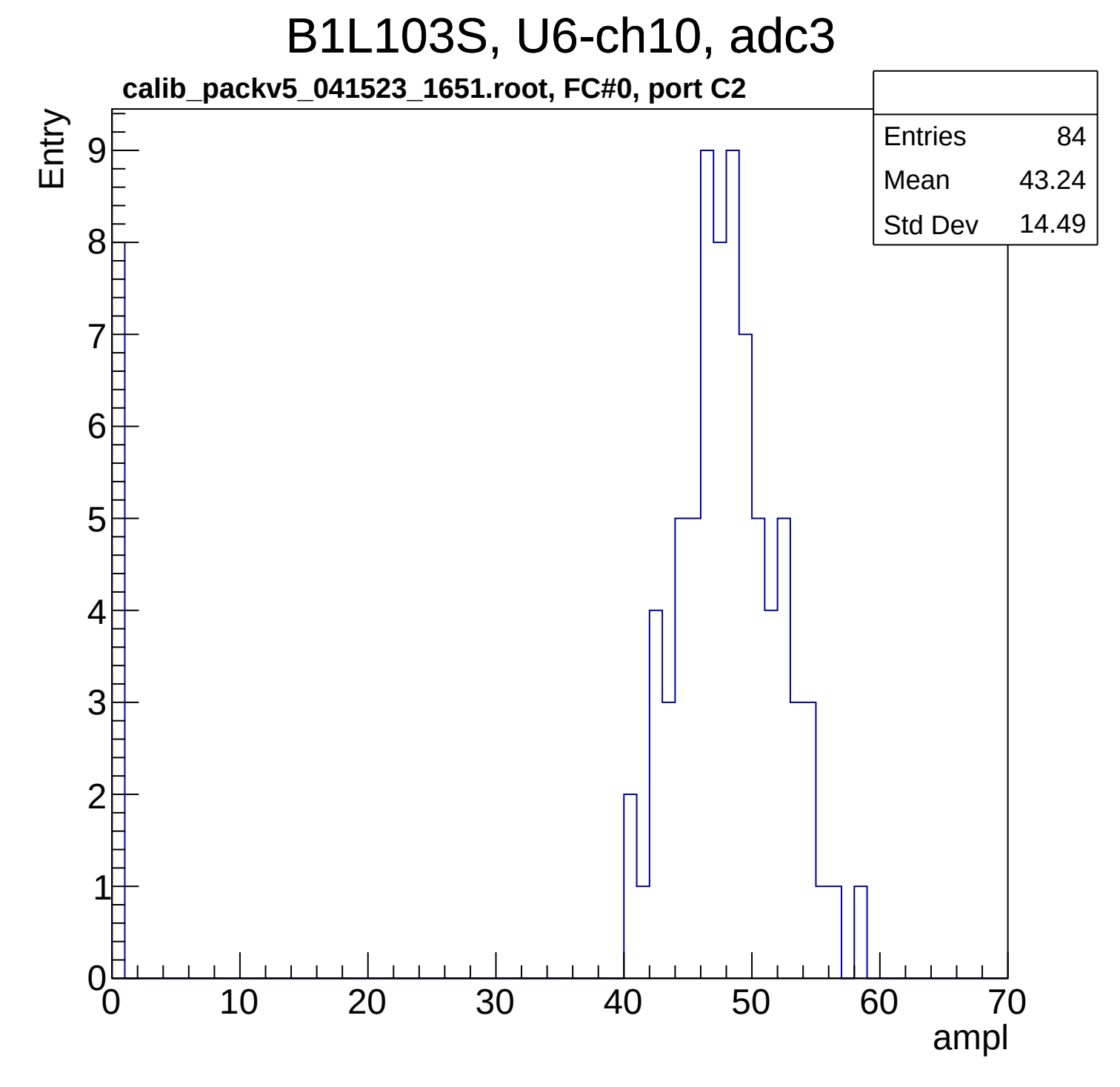
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch10, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 43.24
Std Dev 14.49
Entry
ampl
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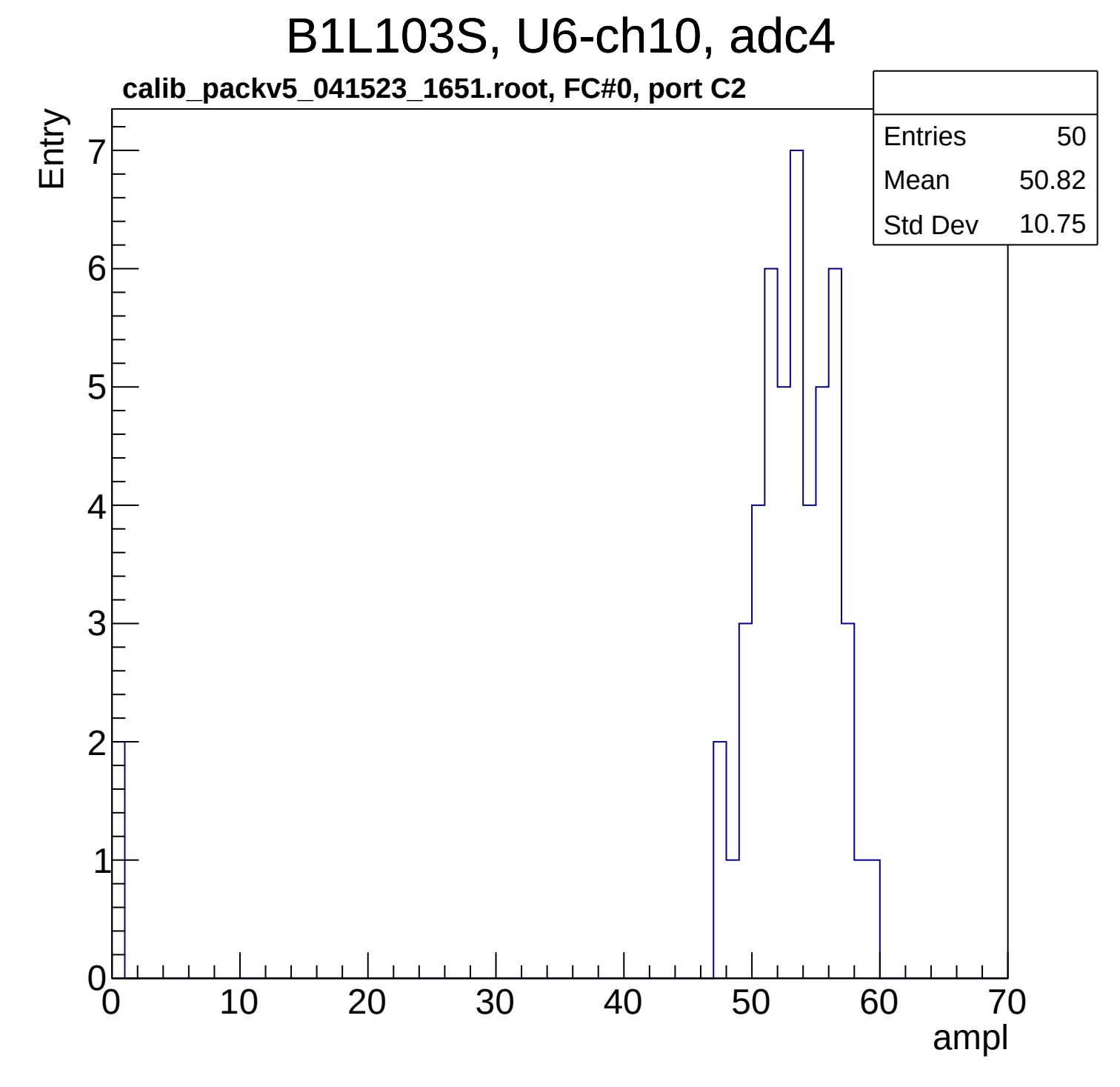
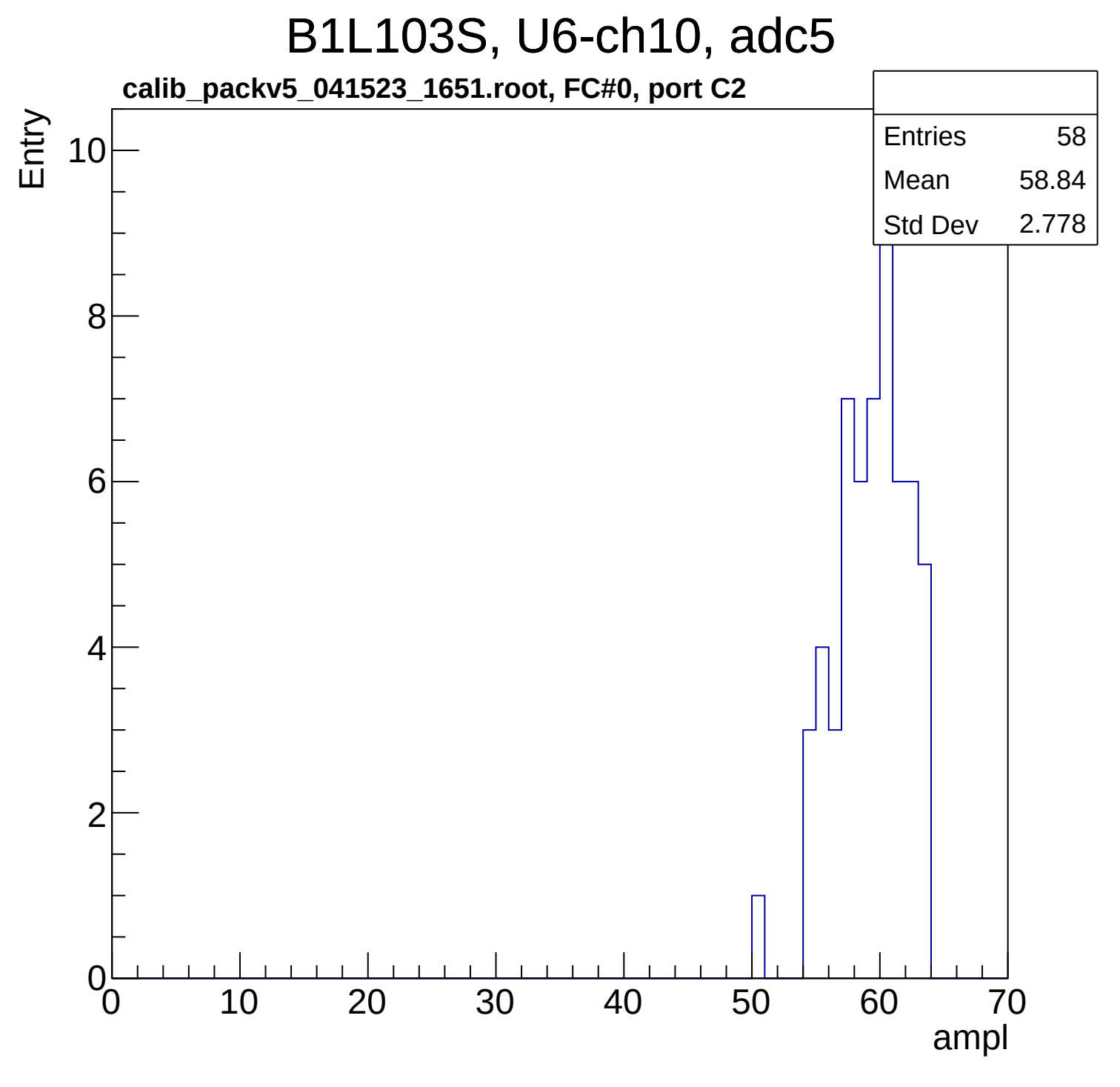
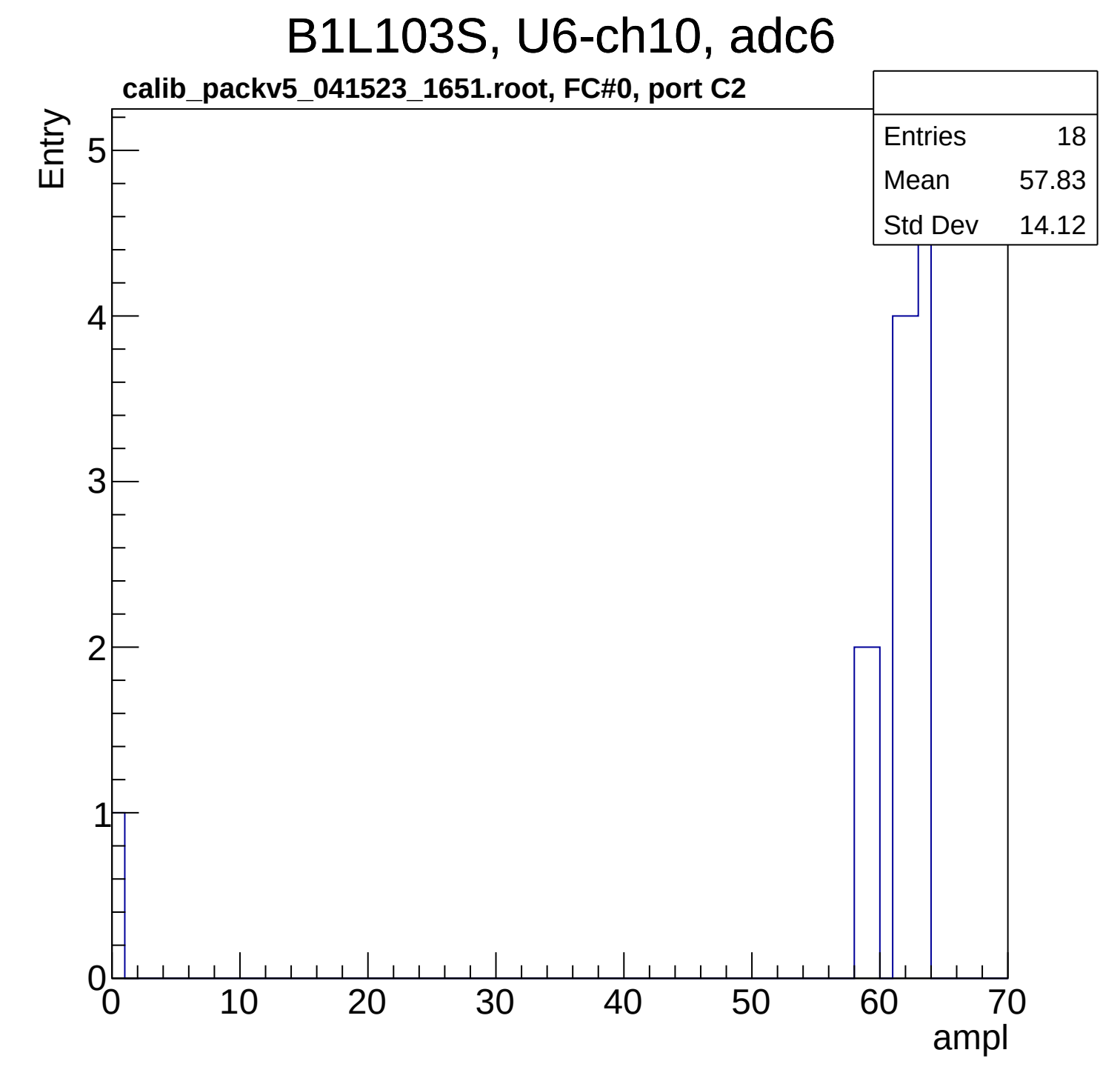
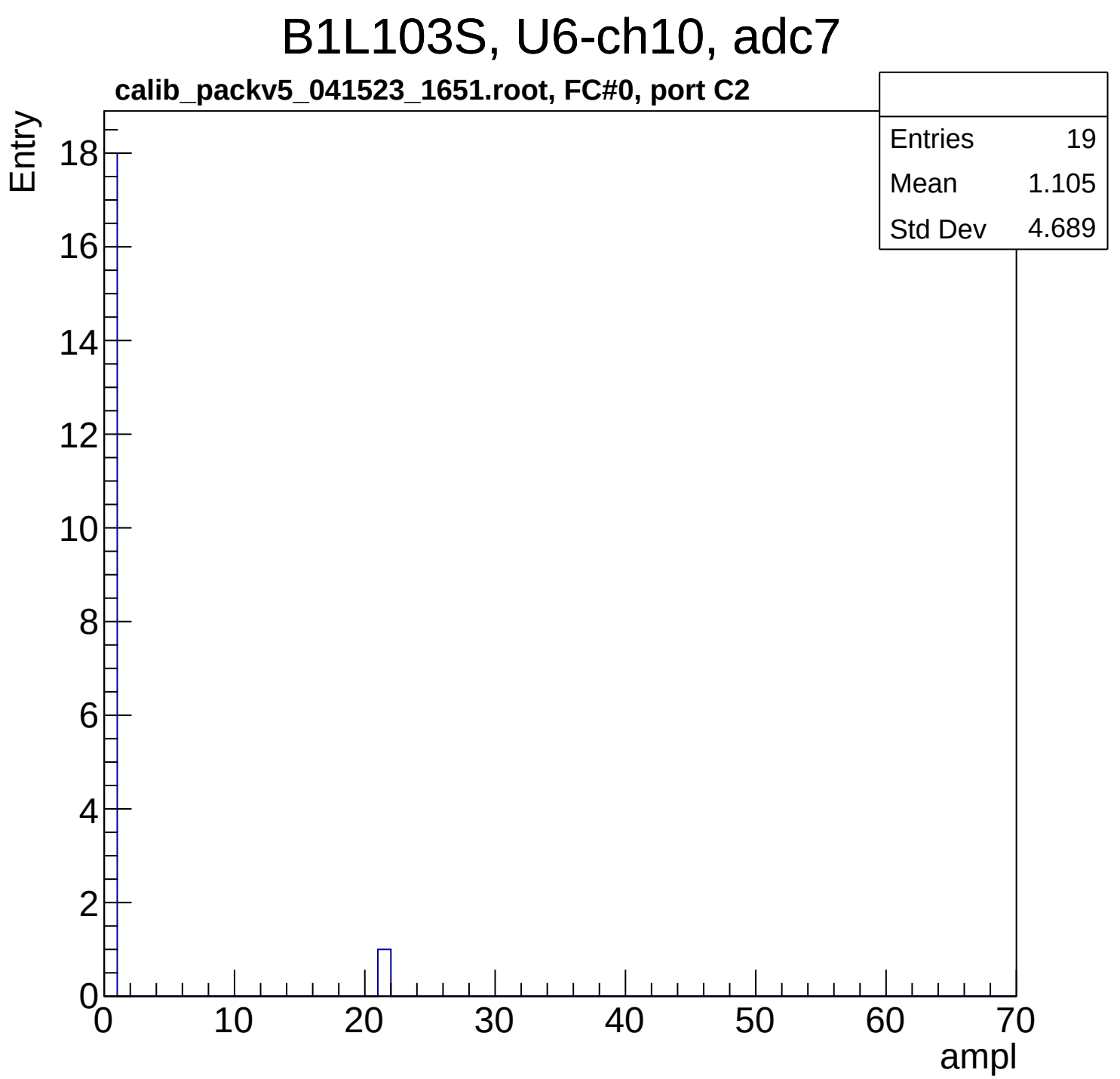
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch10, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 50.82
Std Dev 10.75
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U6-ch10, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 58.84
Std Dev 2.778
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U6-ch10, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 57.83
Std Dev 14.12
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U6-ch10, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.105
Std Dev 4.689
Entry
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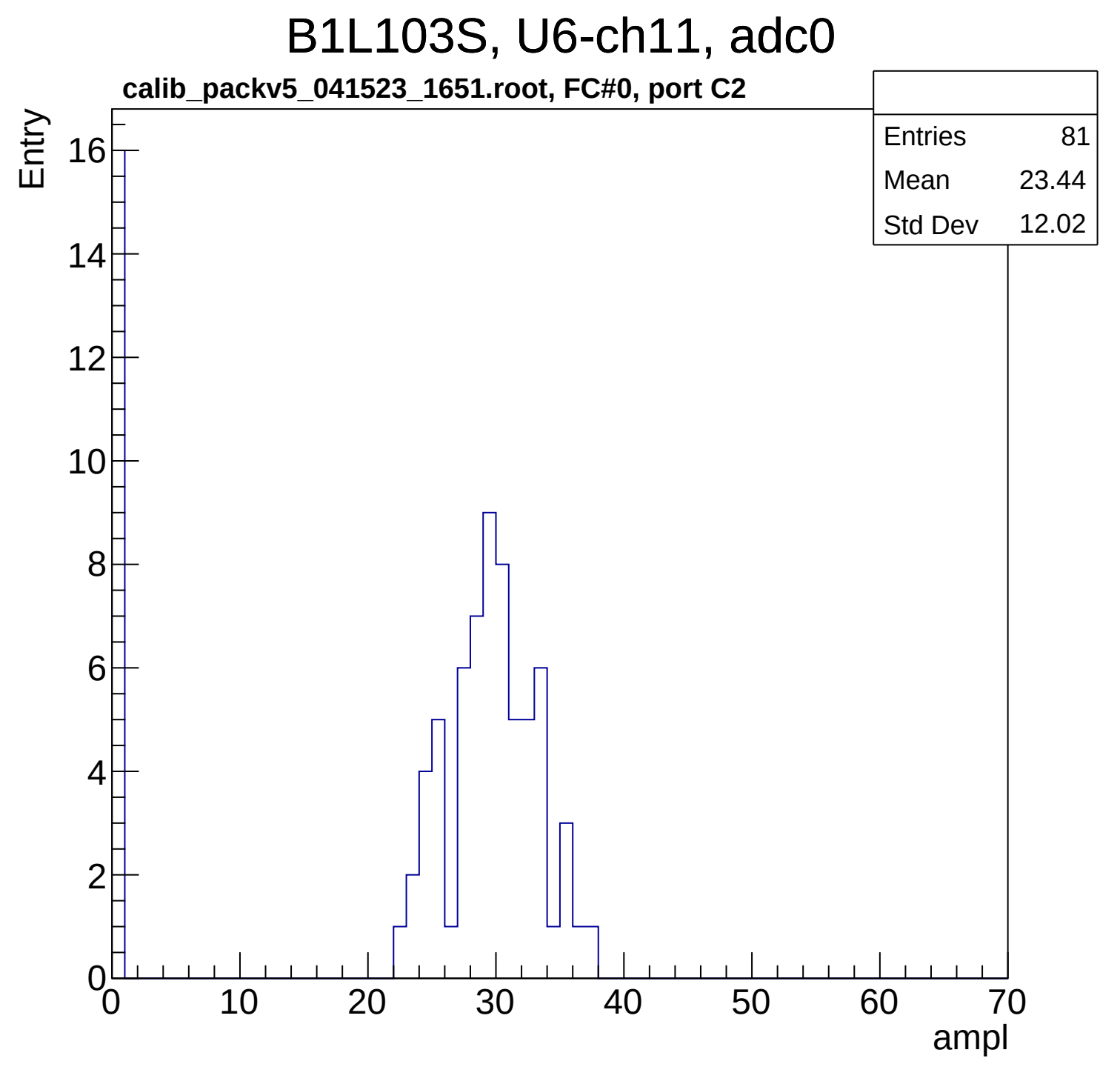
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch11, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 23.44
Std Dev 12.02
Entry
ampl
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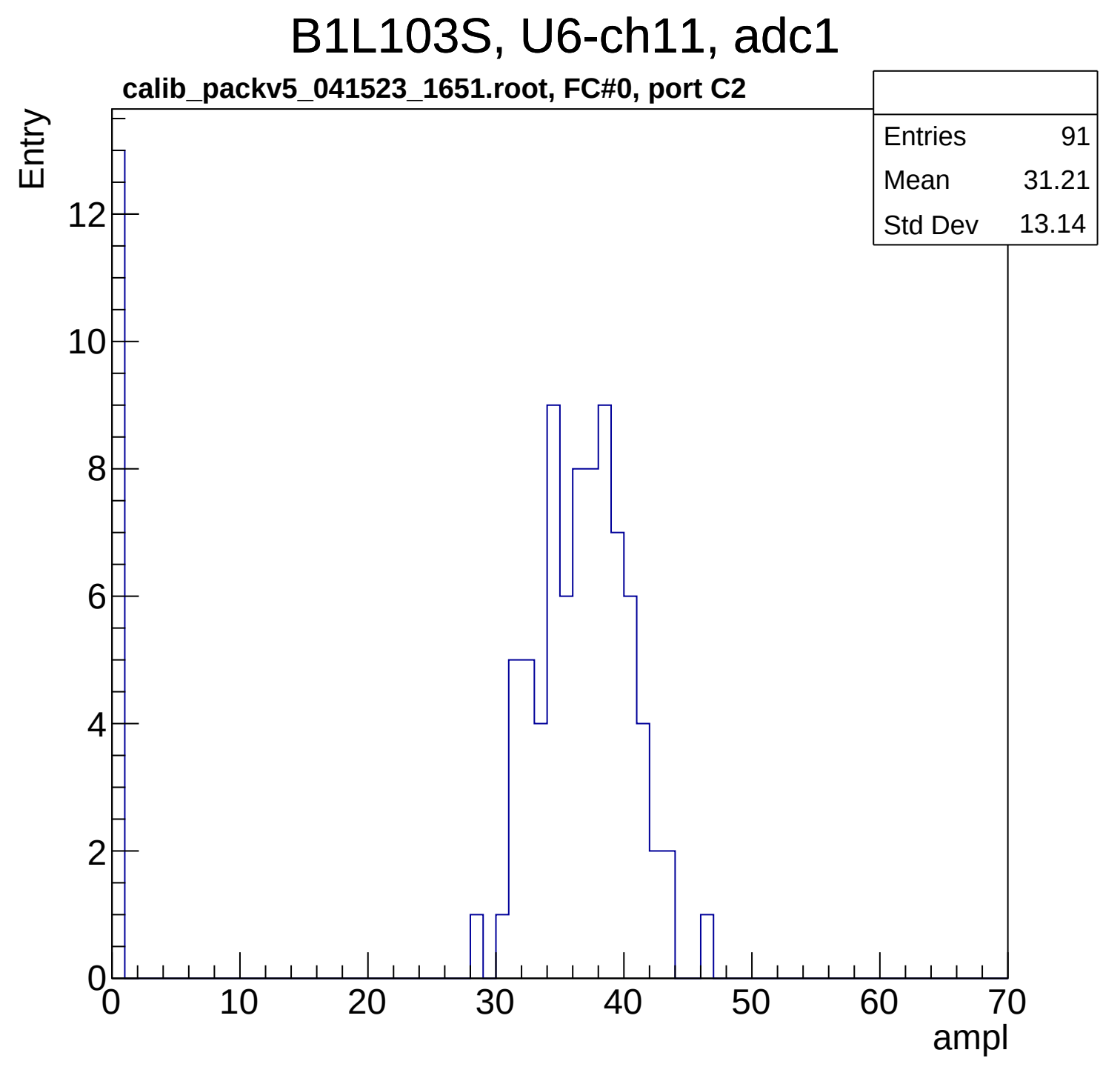
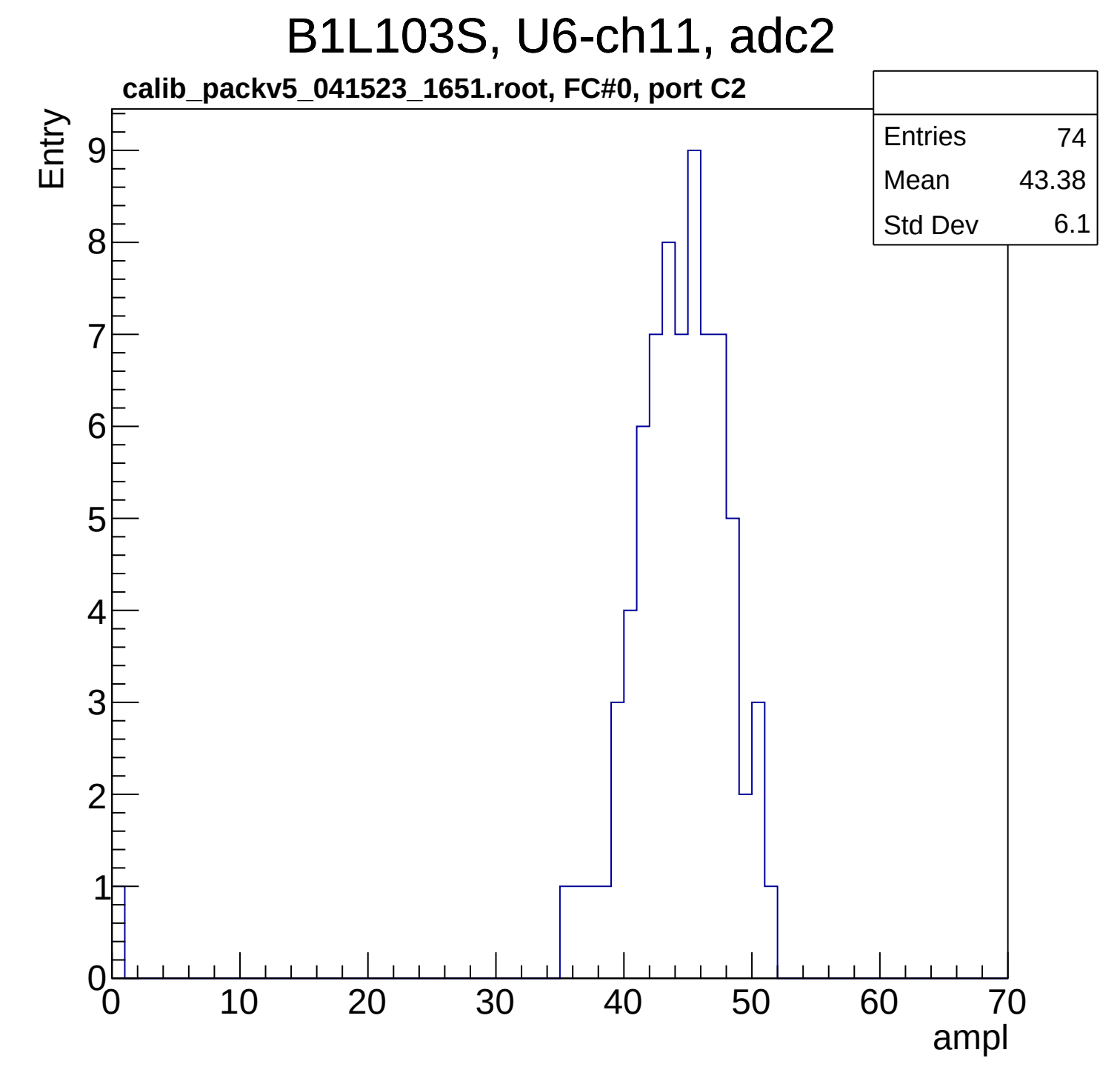
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L103S, U6-ch11, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 31.21
Std Dev 13.14
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch11, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 43.38
Std Dev 6.1
Entry
ampl
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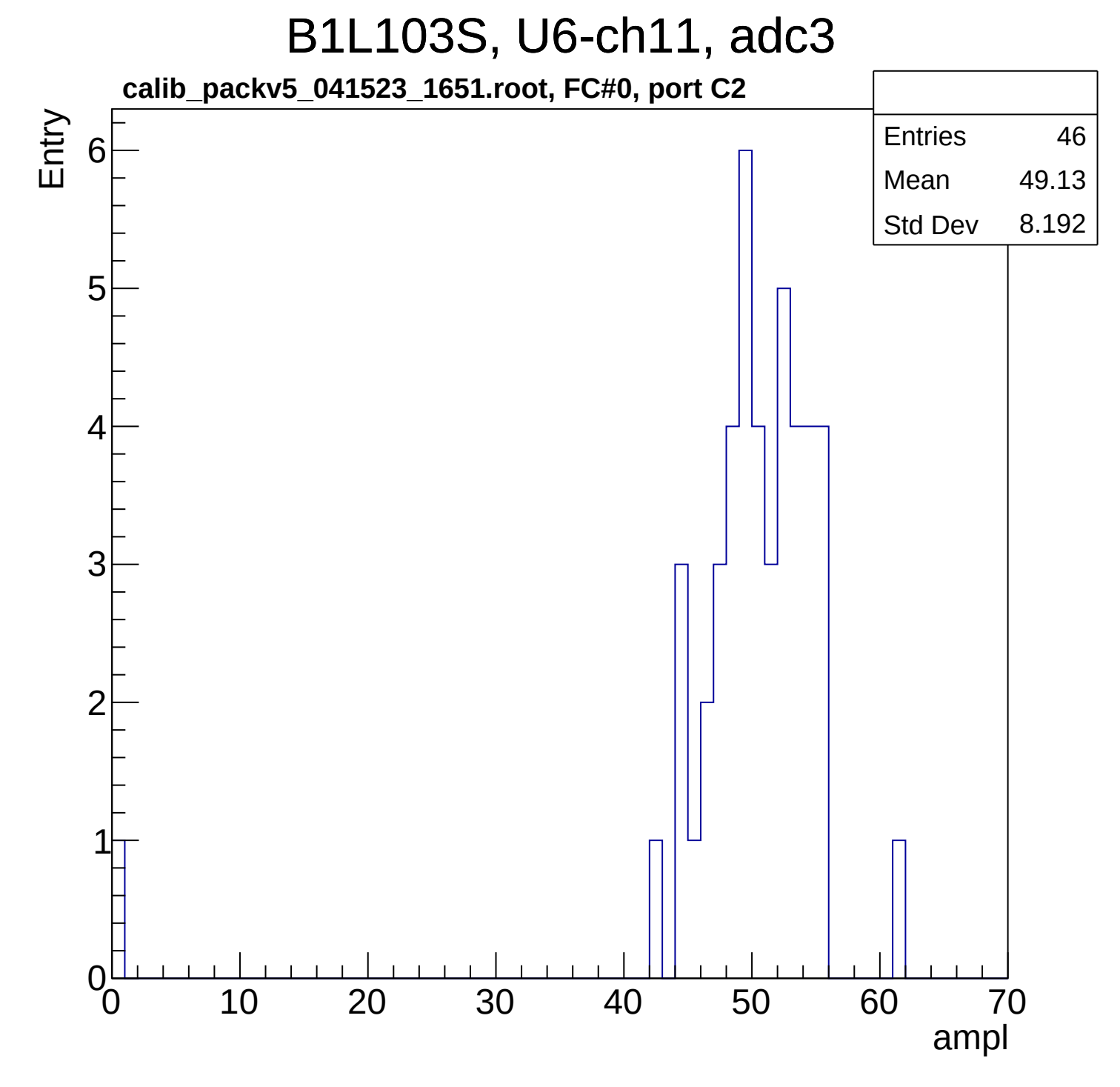
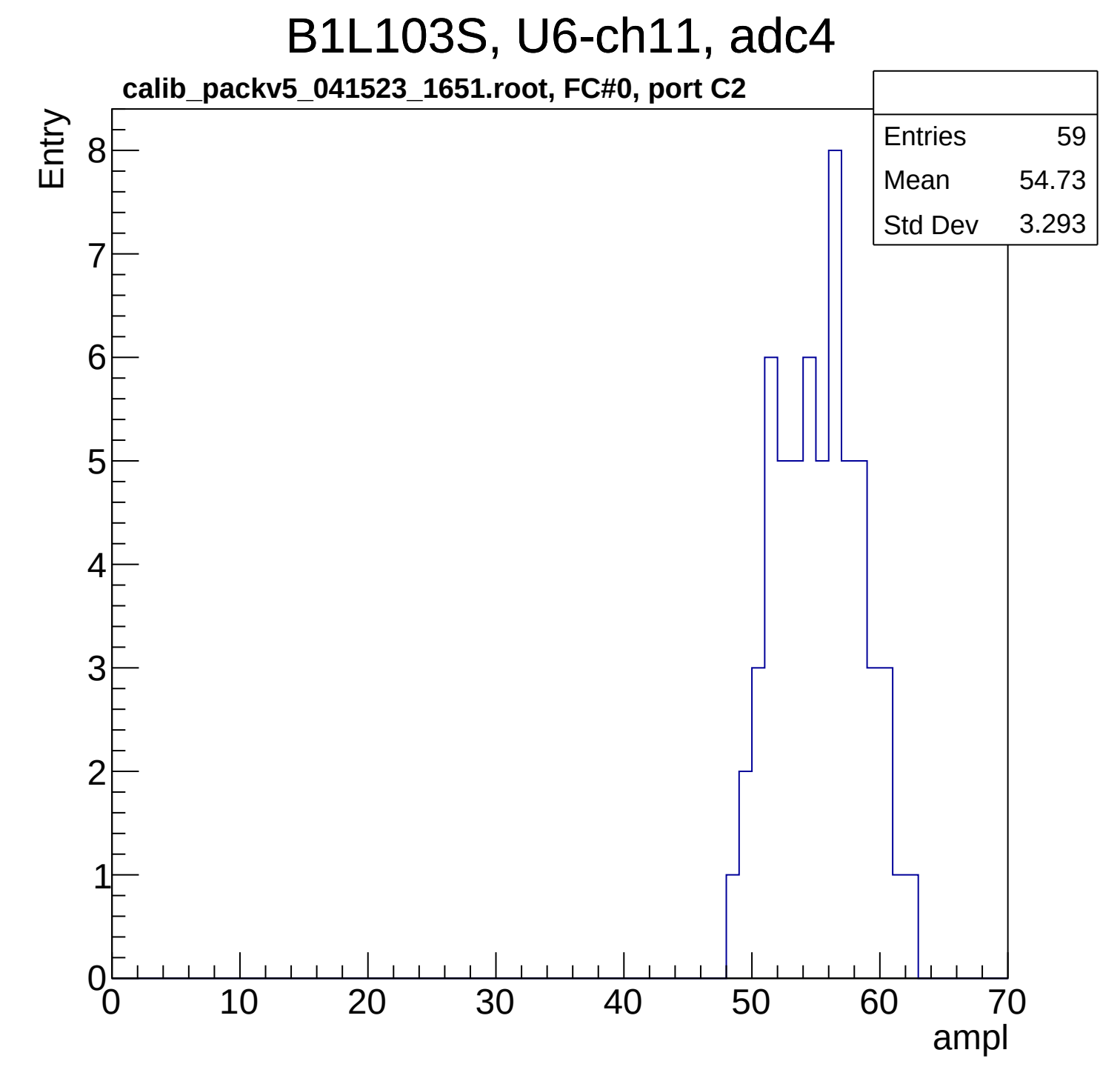
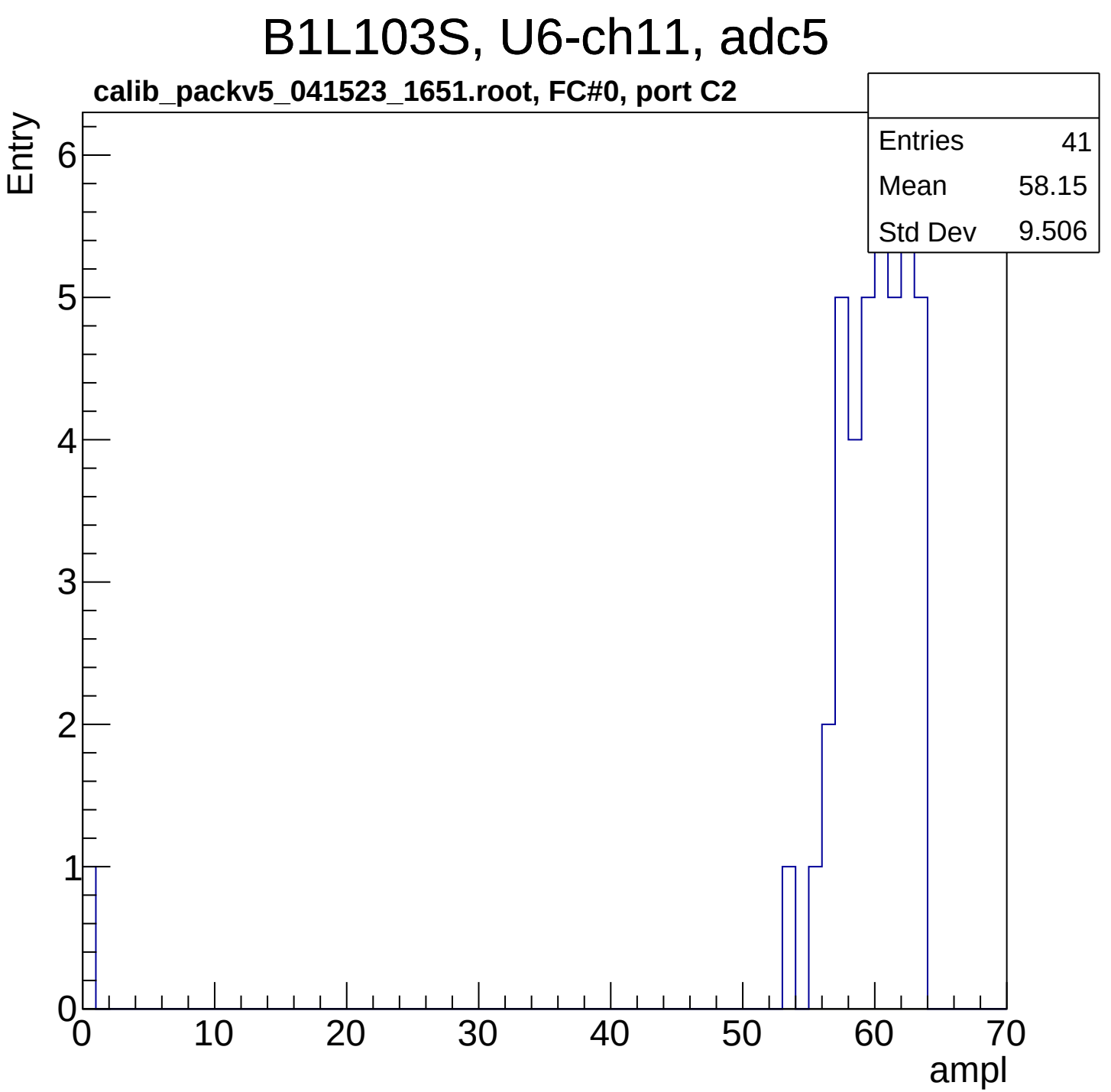
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch11, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 49.13
Std Dev 8.192
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch11, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 54.73
Std Dev 3.293
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch11, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 58.15
Std Dev 9.506
Entry
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4
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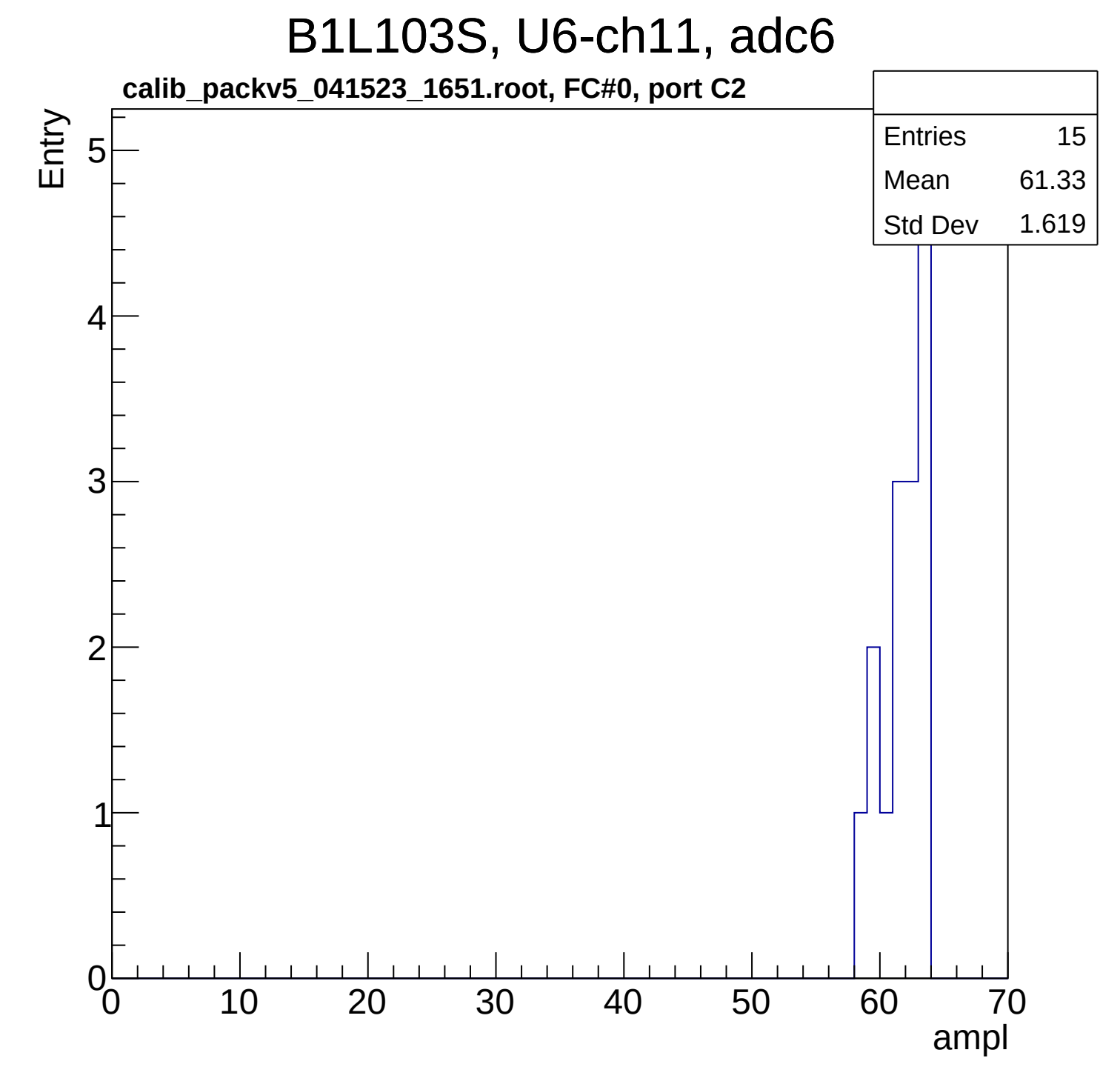
ampl


B1L103S, U6-ch11, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 61.33
Std Dev 1.619
Entry
ampl
0
1
2
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0
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40
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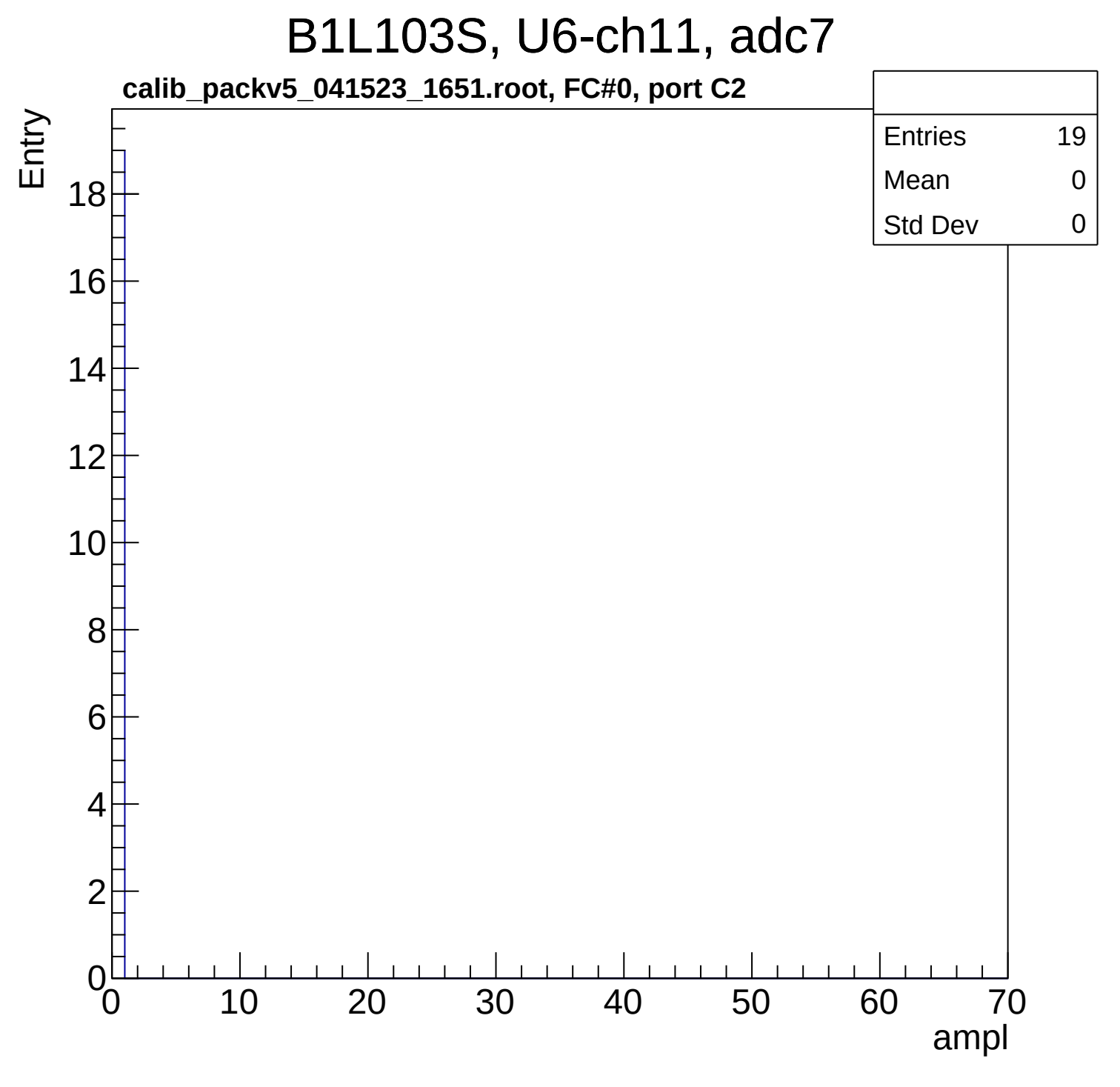
B1L103S, U6-ch11, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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2
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6
8
10
12
14
16
18
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50
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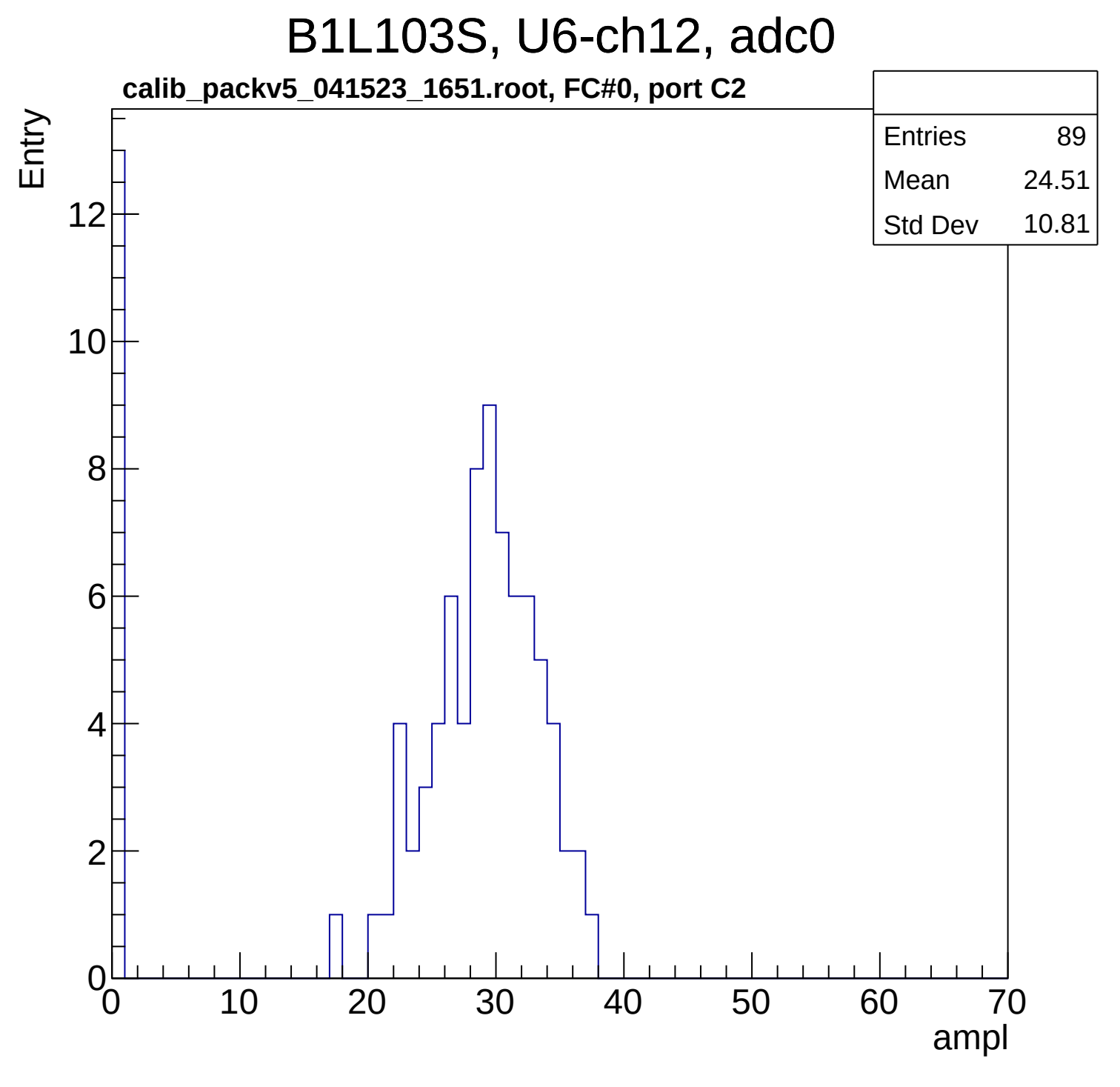
ampl


B1L103S, U6-ch12, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 24.51
Std Dev 10.81
Entry
ampl
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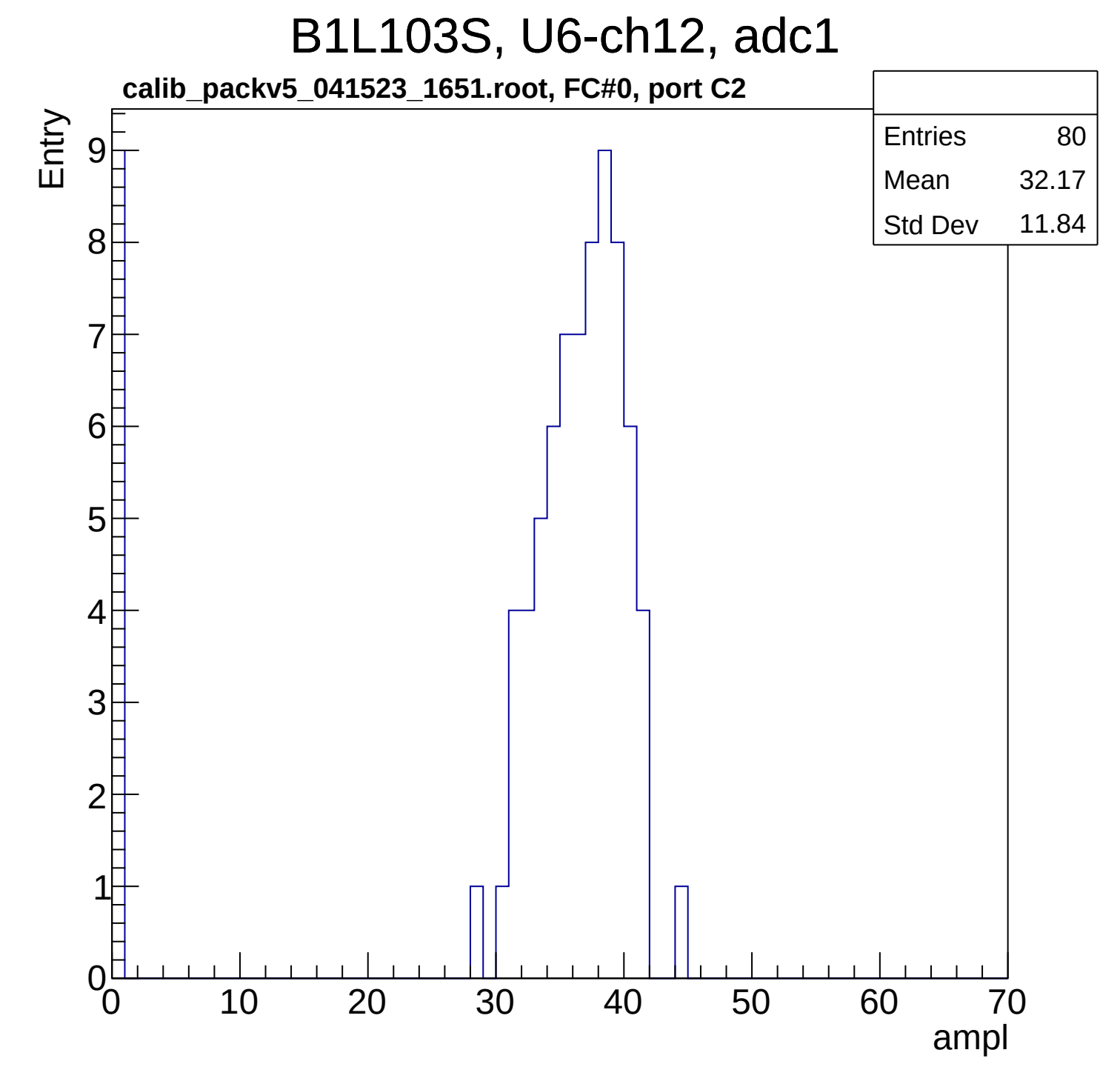
B1L103S, U6-ch12, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 32.17
Std Dev 11.84
Entry
ampl
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4
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7
8
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0
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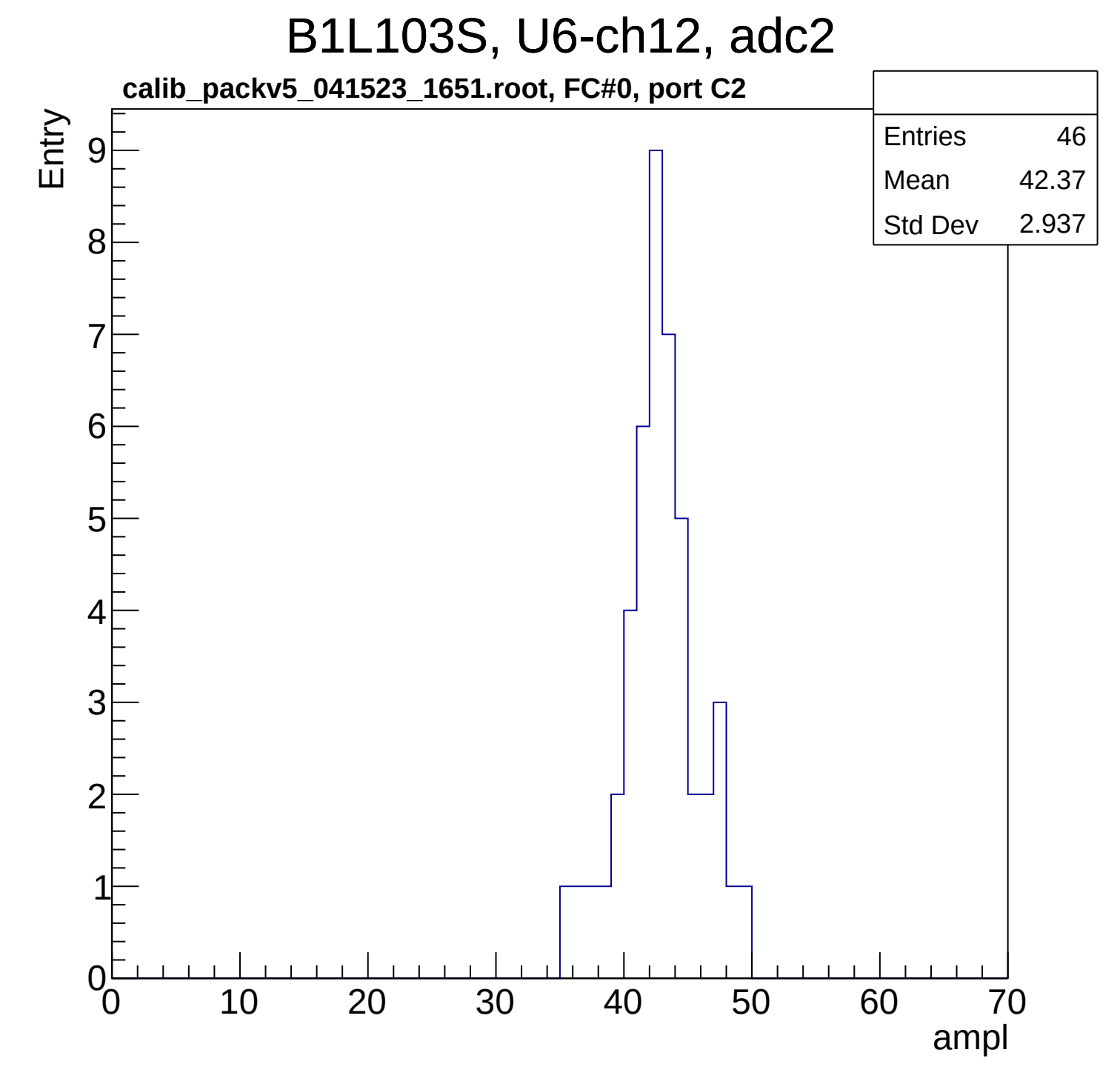
B1L103S, U6-ch12, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 42.37
Std Dev 2.937
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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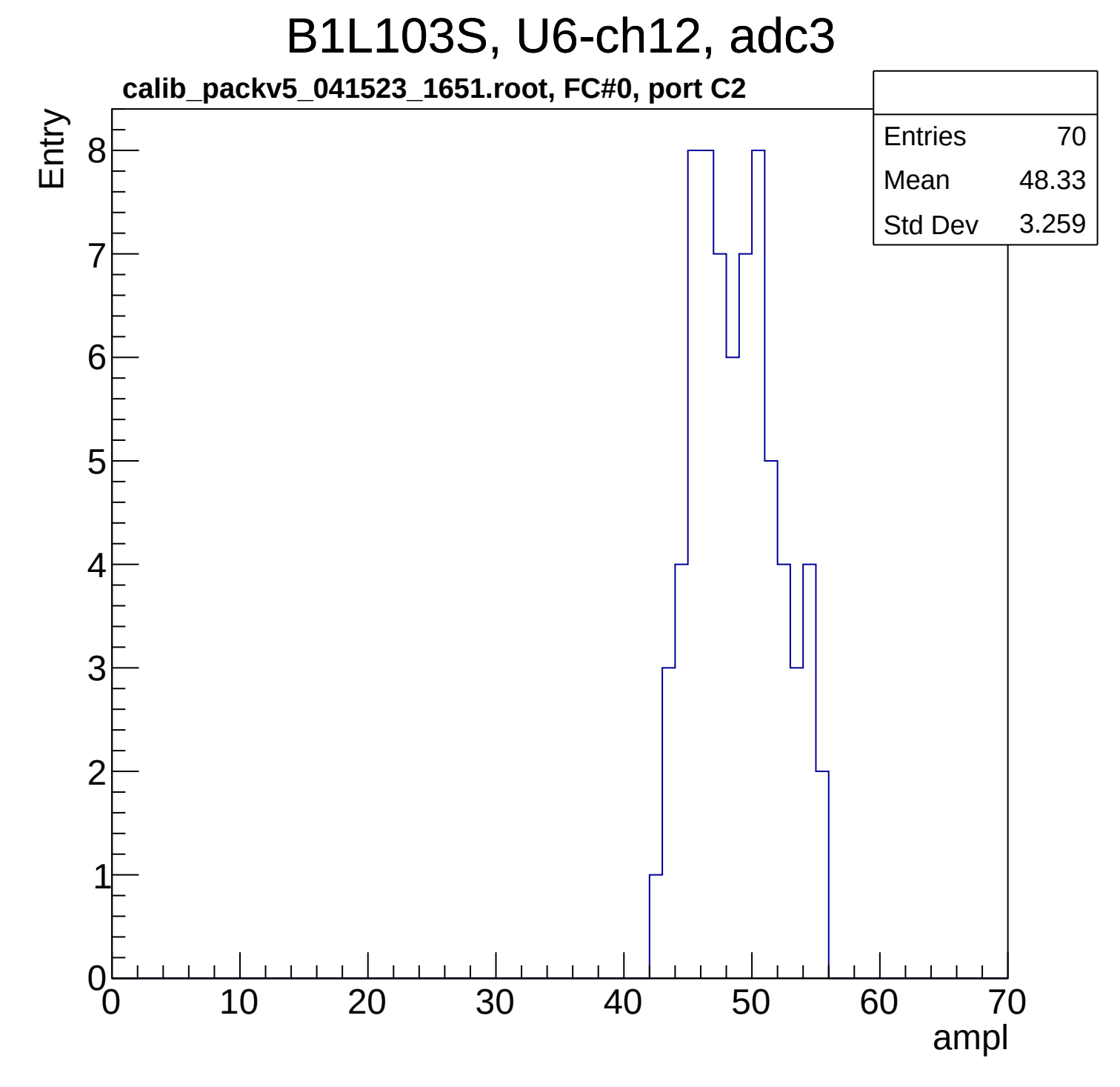
B1L103S, U6-ch12, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 48.33
Std Dev 3.259
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
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60
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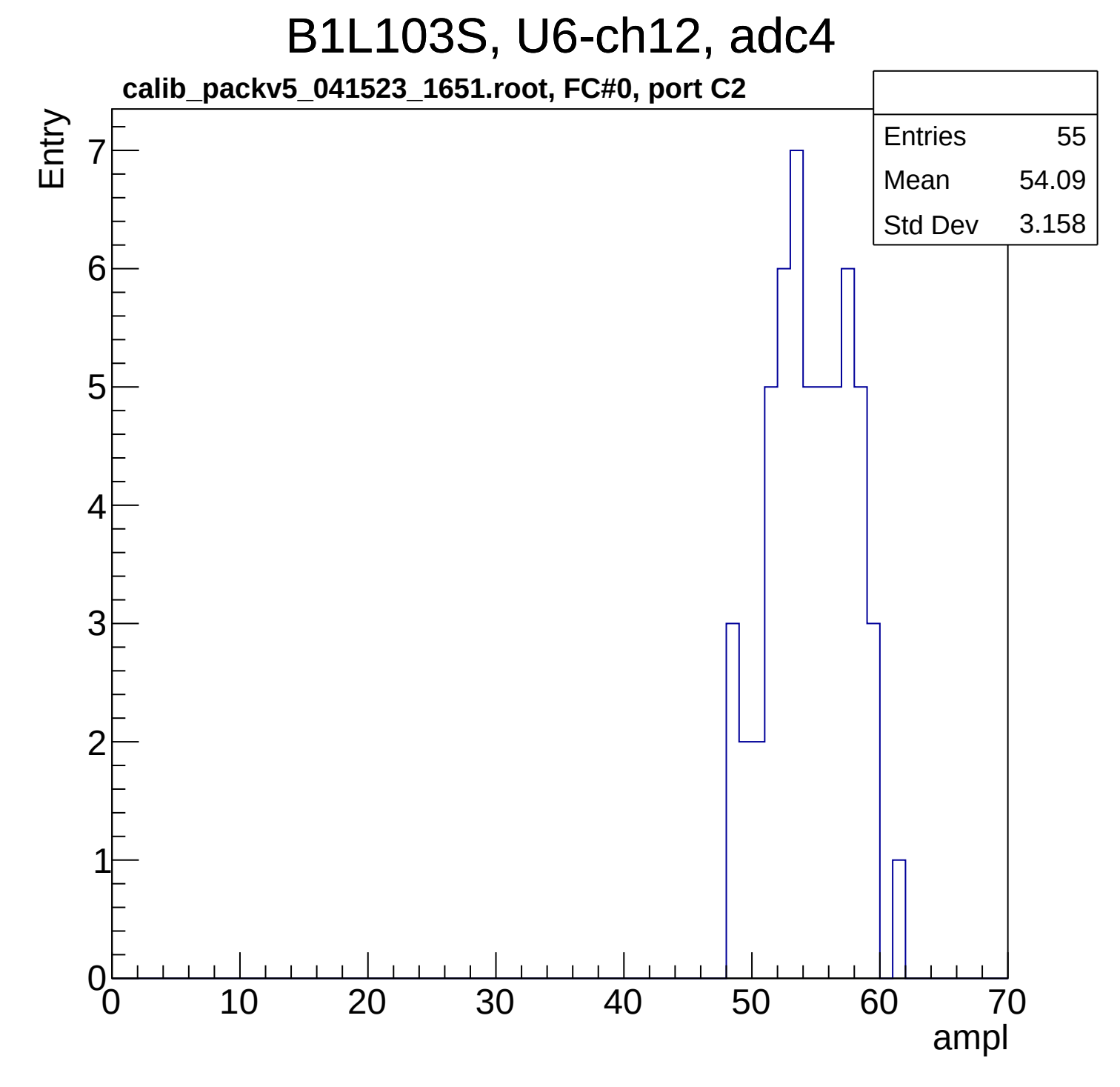
B1L103S, U6-ch12, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 54.09
Std Dev 3.158
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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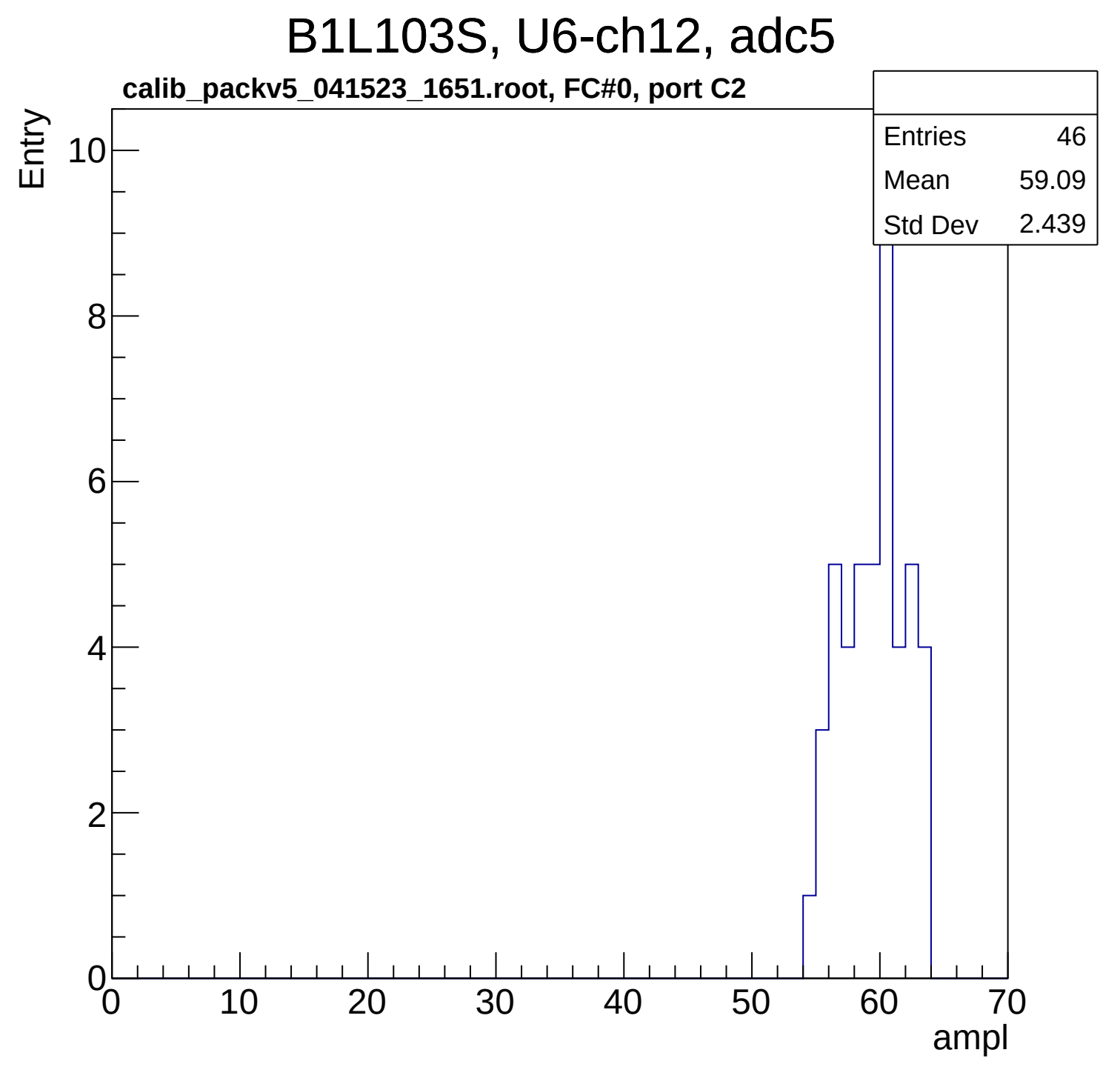
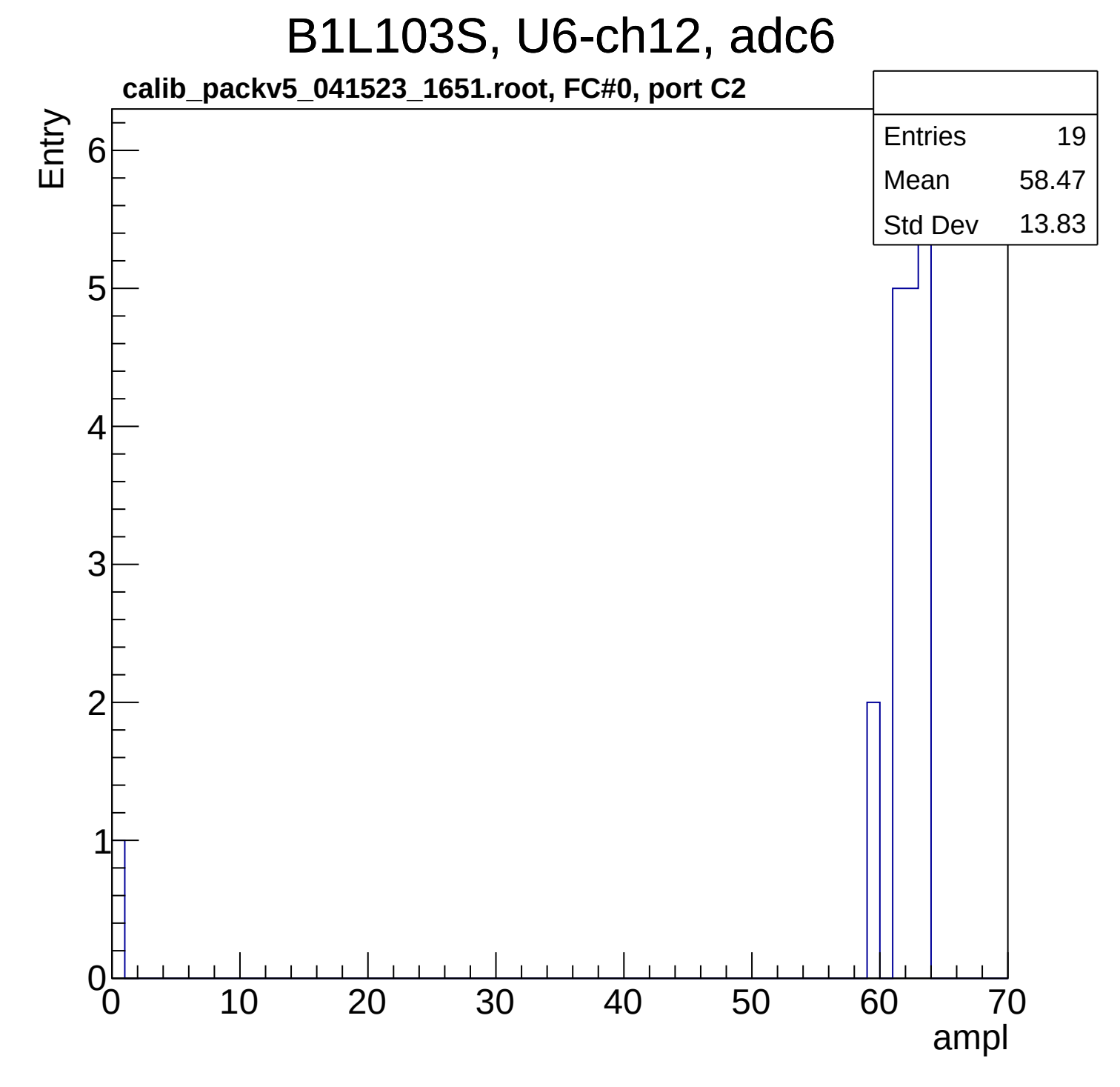
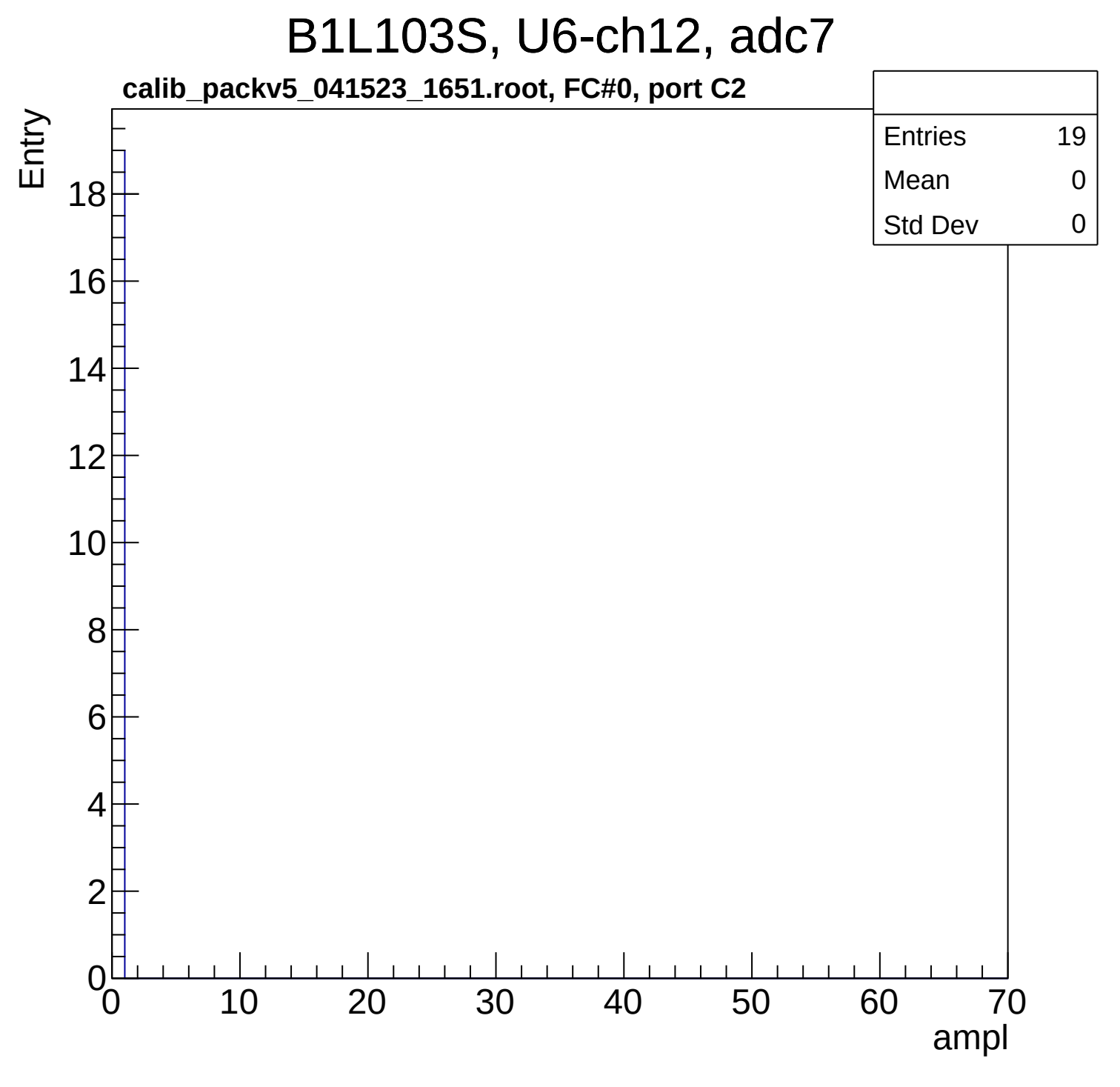
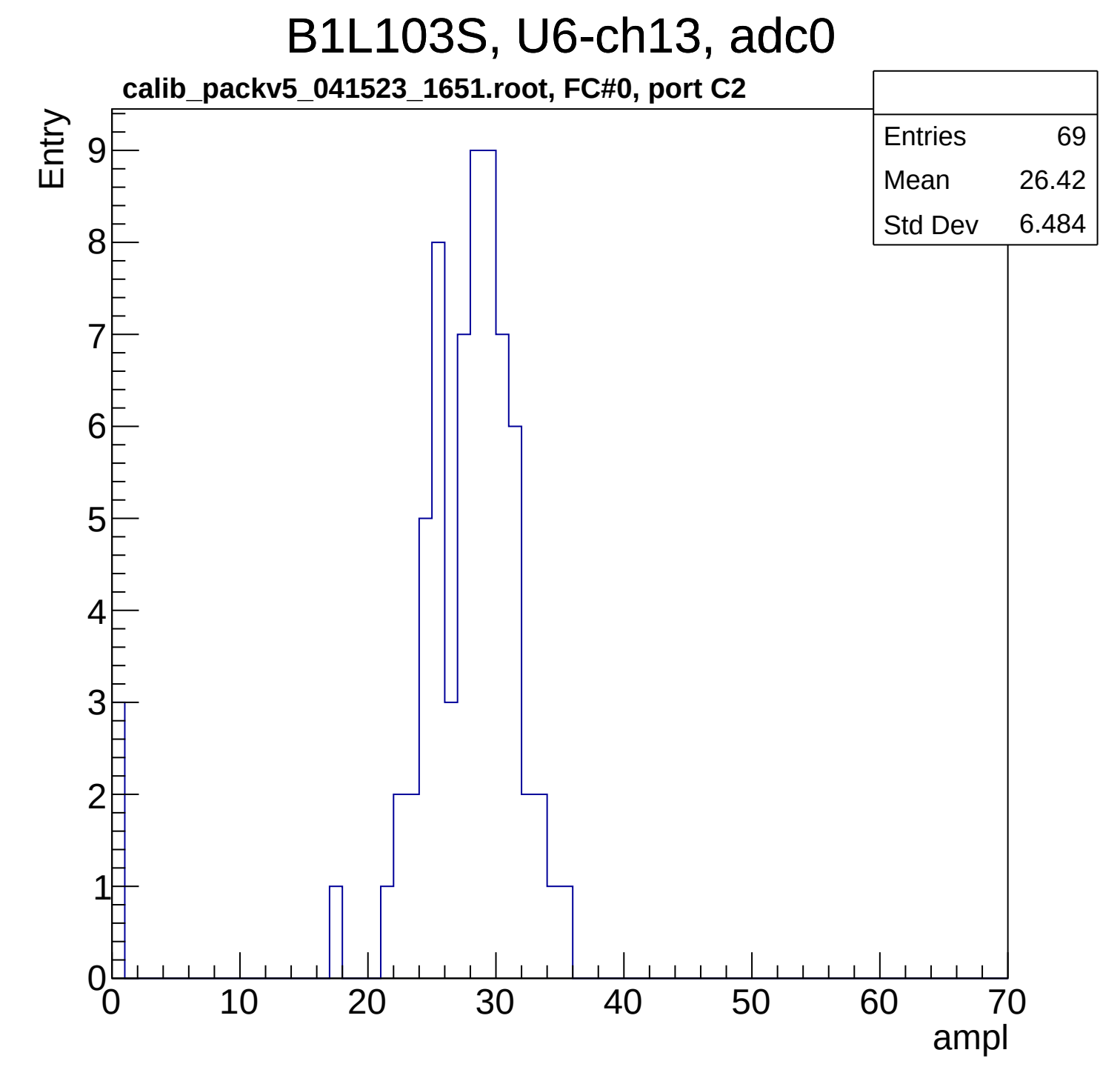

B1L103S, U6-ch12, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 59.09
Std Dev 2.439
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U6-ch12, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 58.47
Std Dev 13.83
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U6-ch12, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch13, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 26.42
Std Dev 6.484
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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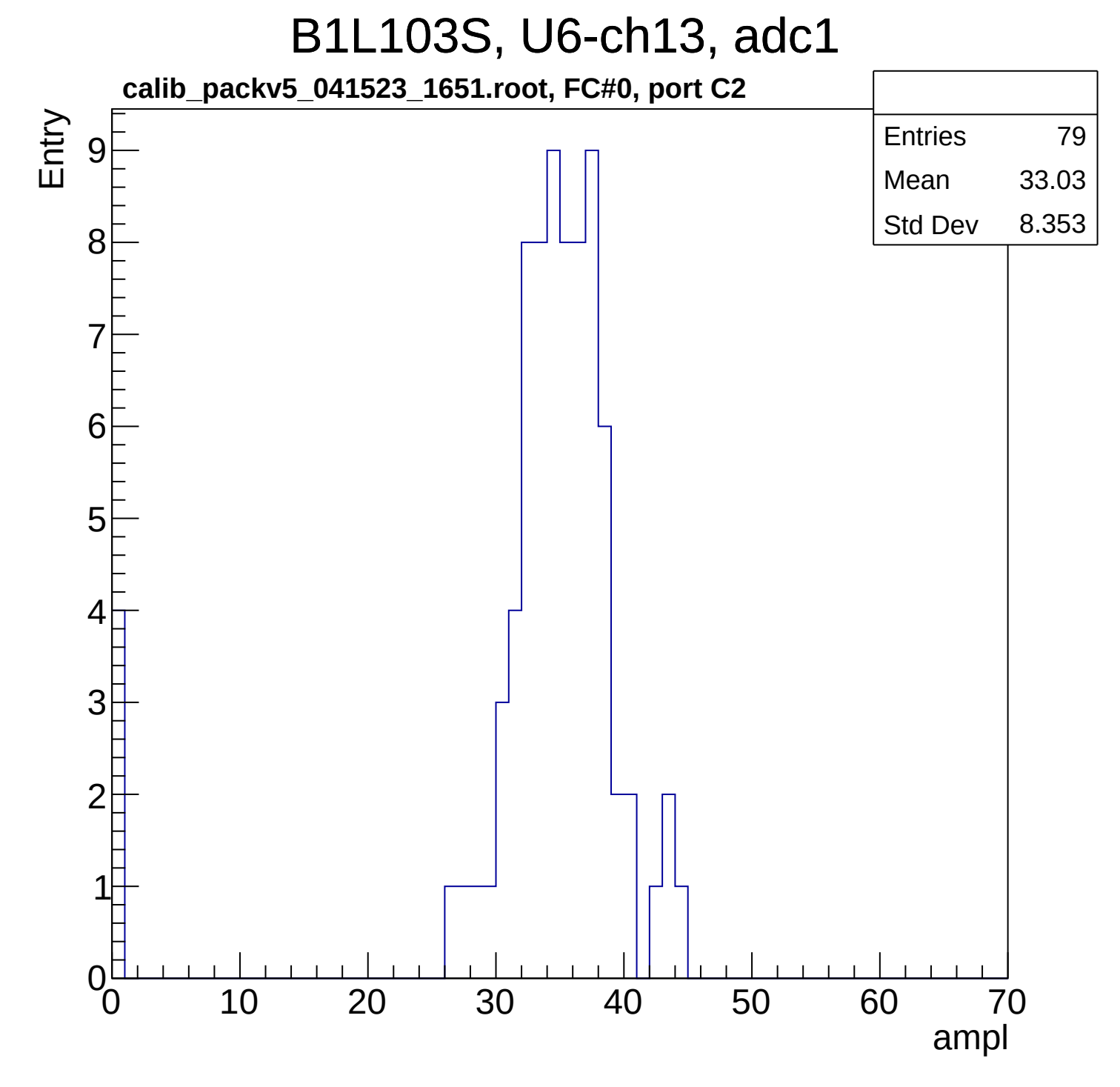
B1L103S, U6-ch13, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 33.03
Std Dev 8.353
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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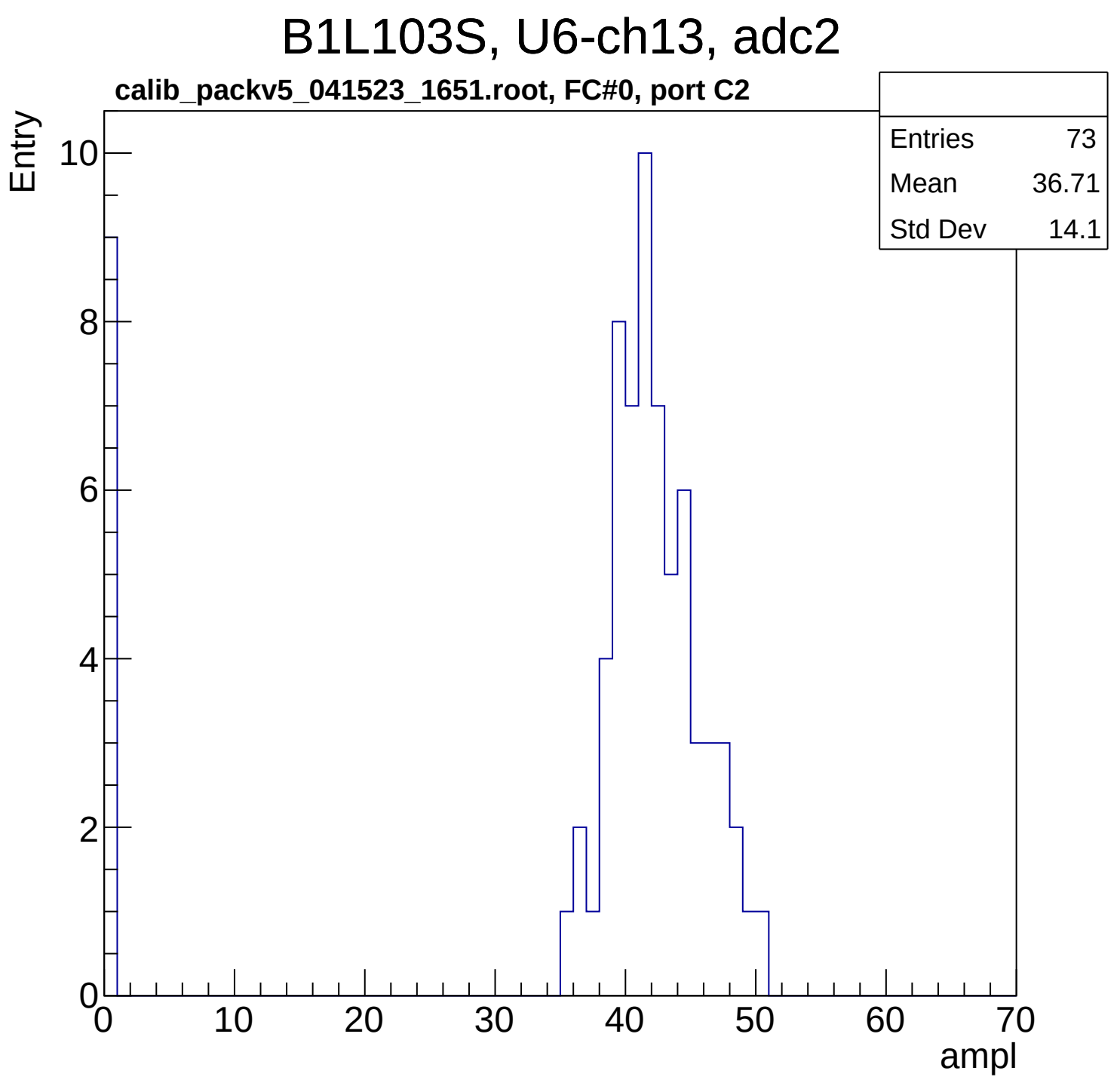
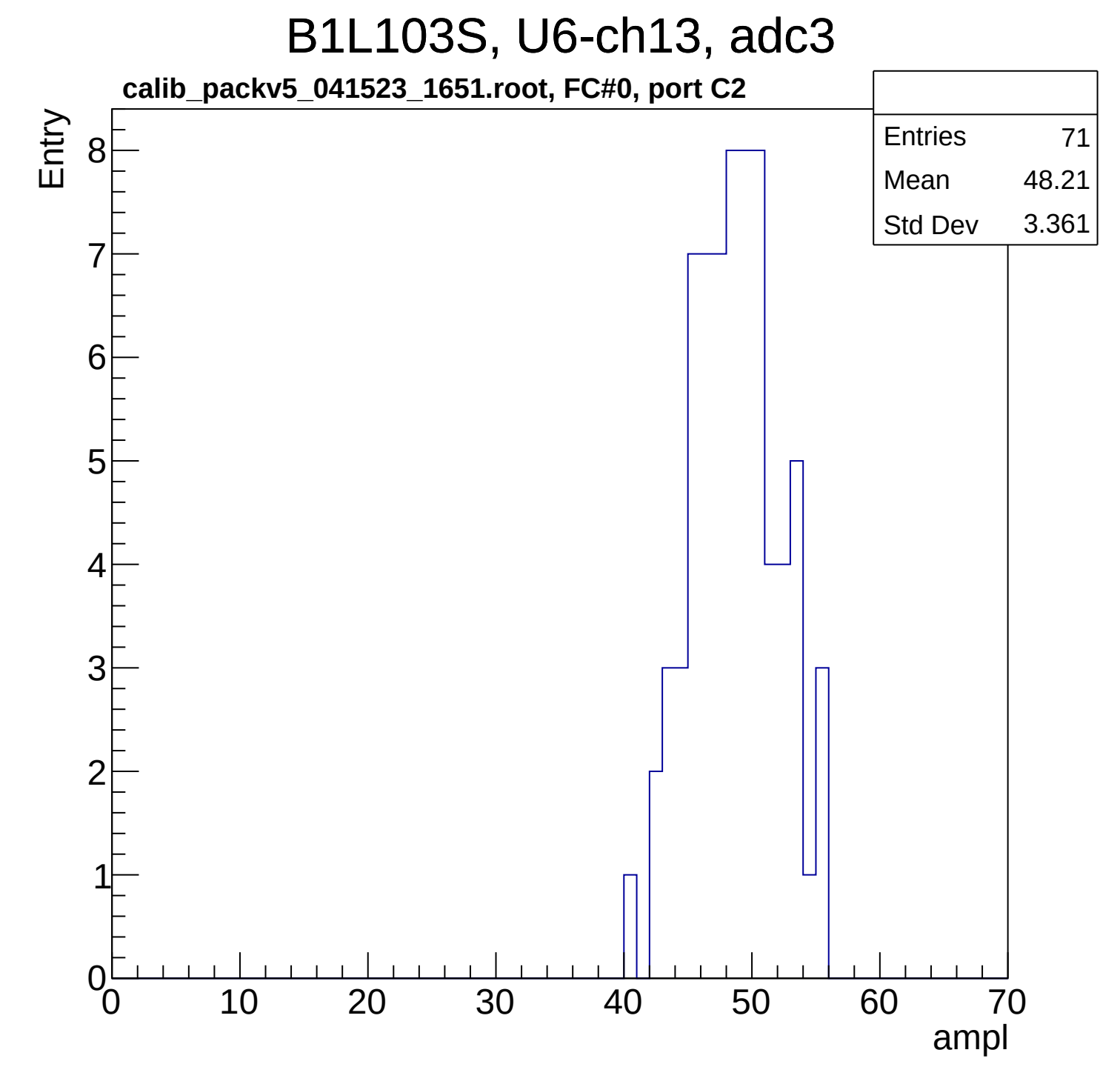
40
50
60
70


B1L103S, U6-ch13, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 36.71
Std Dev 14.1
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch13, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 48.21
Std Dev 3.361
Entry
ampl
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2
3
4
5
6
7
8
0
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60
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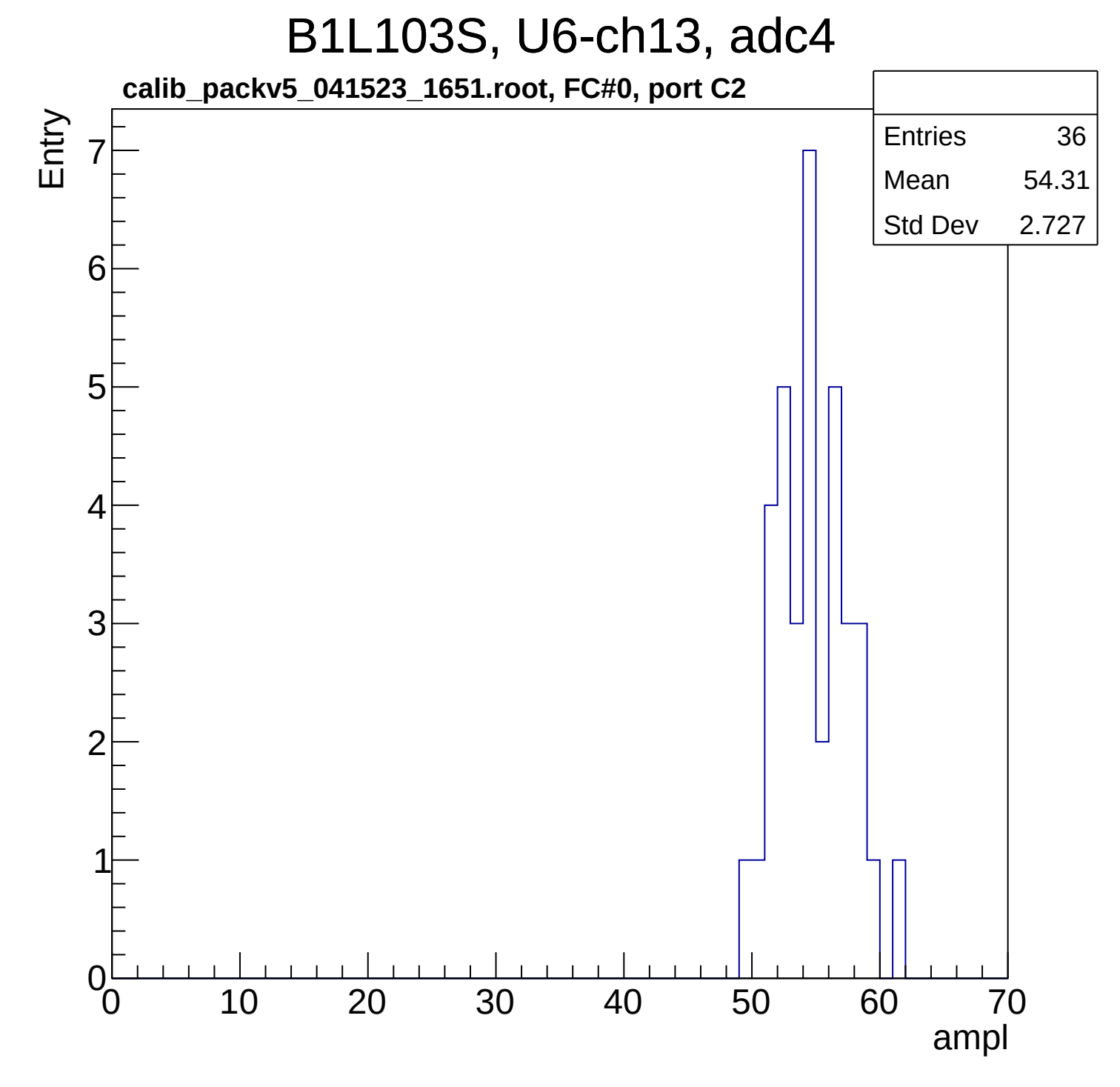
B1L103S, U6-ch13, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 54.31
Std Dev 2.727
Entry
ampl
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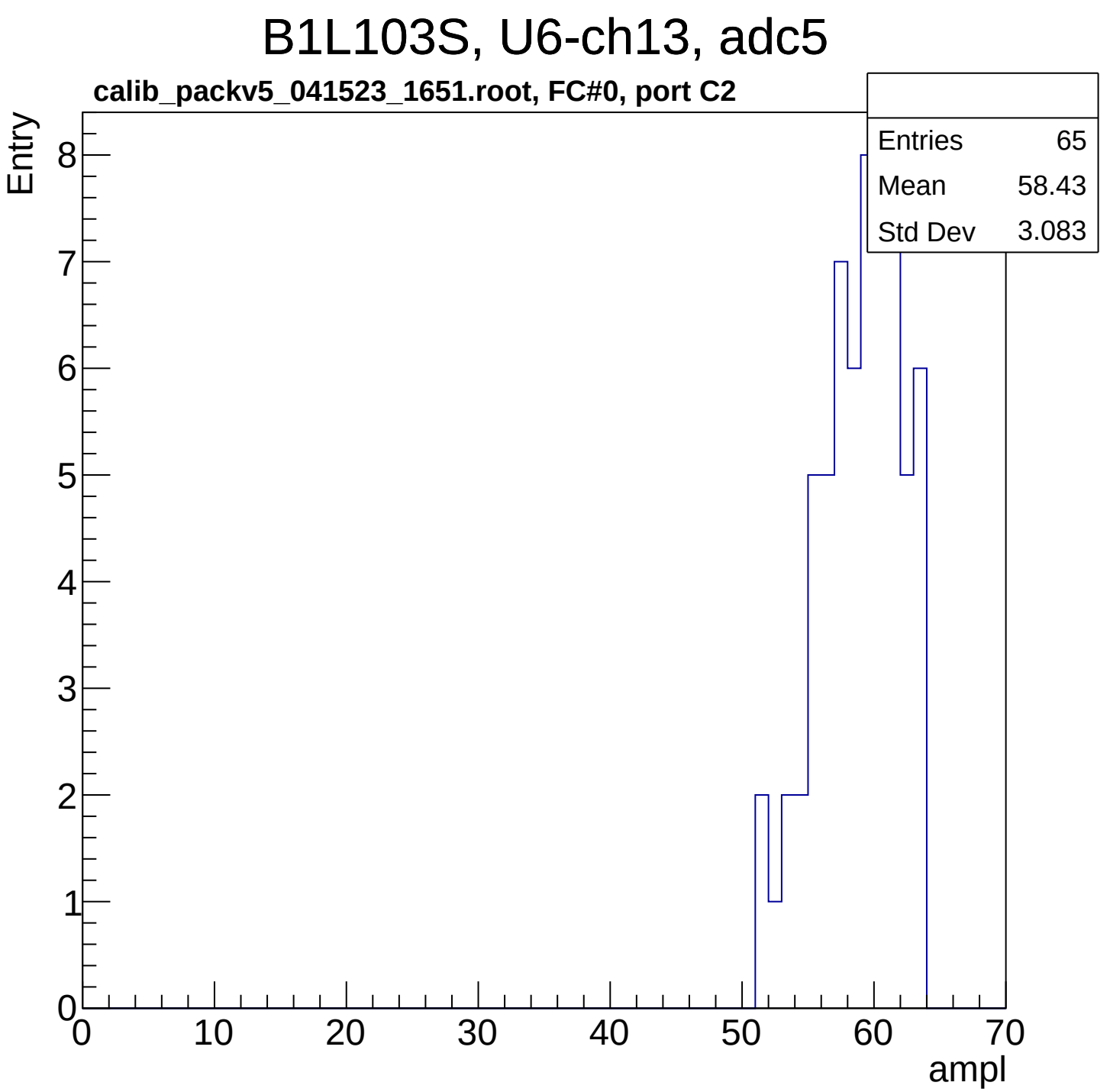
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U6-ch13, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 58.43
Std Dev 3.083
Entry
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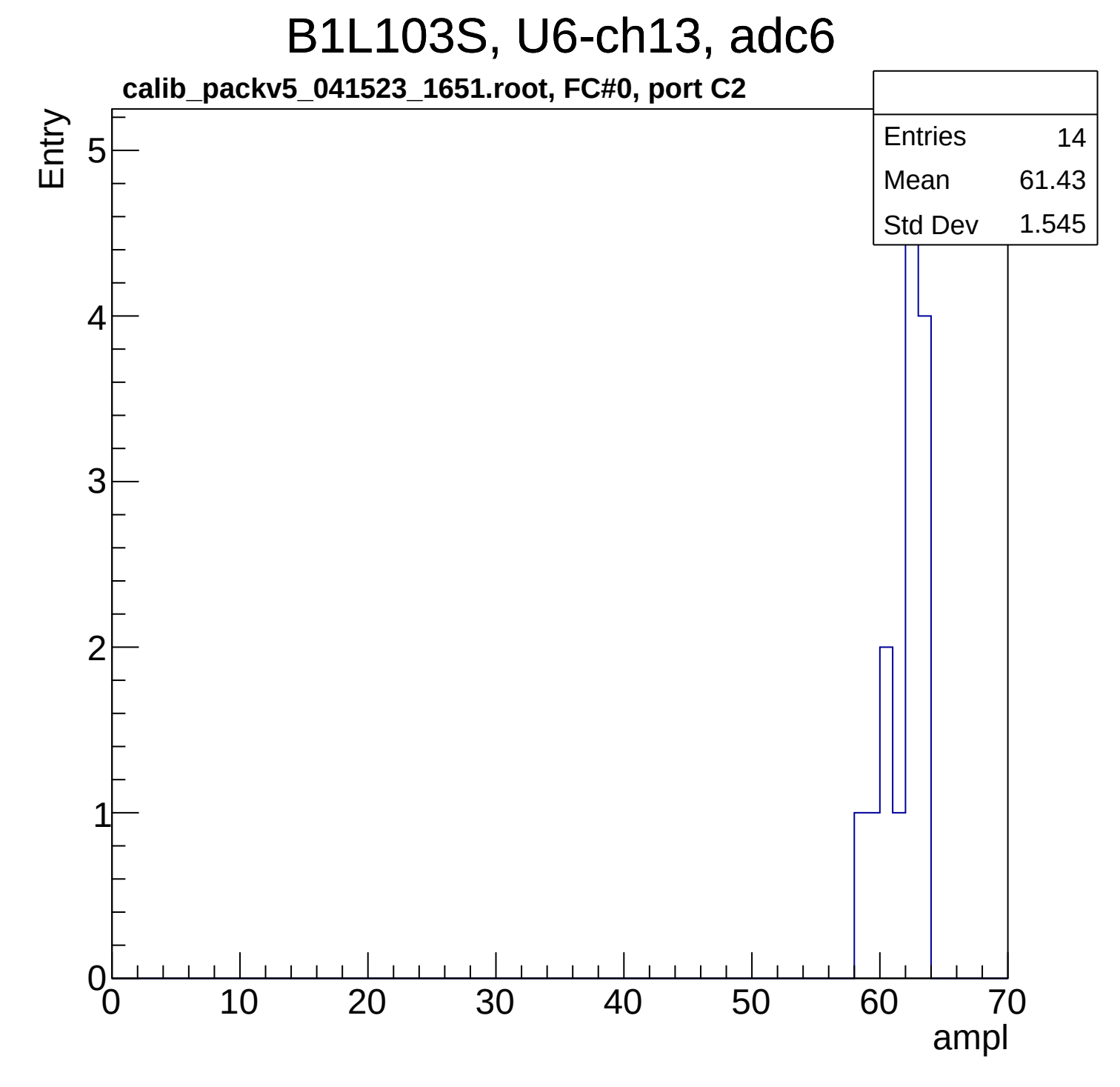
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch13, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 61.43
Std Dev 1.545
Entry
ampl
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1
2
3
4
5
0
10
20
30
40
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60
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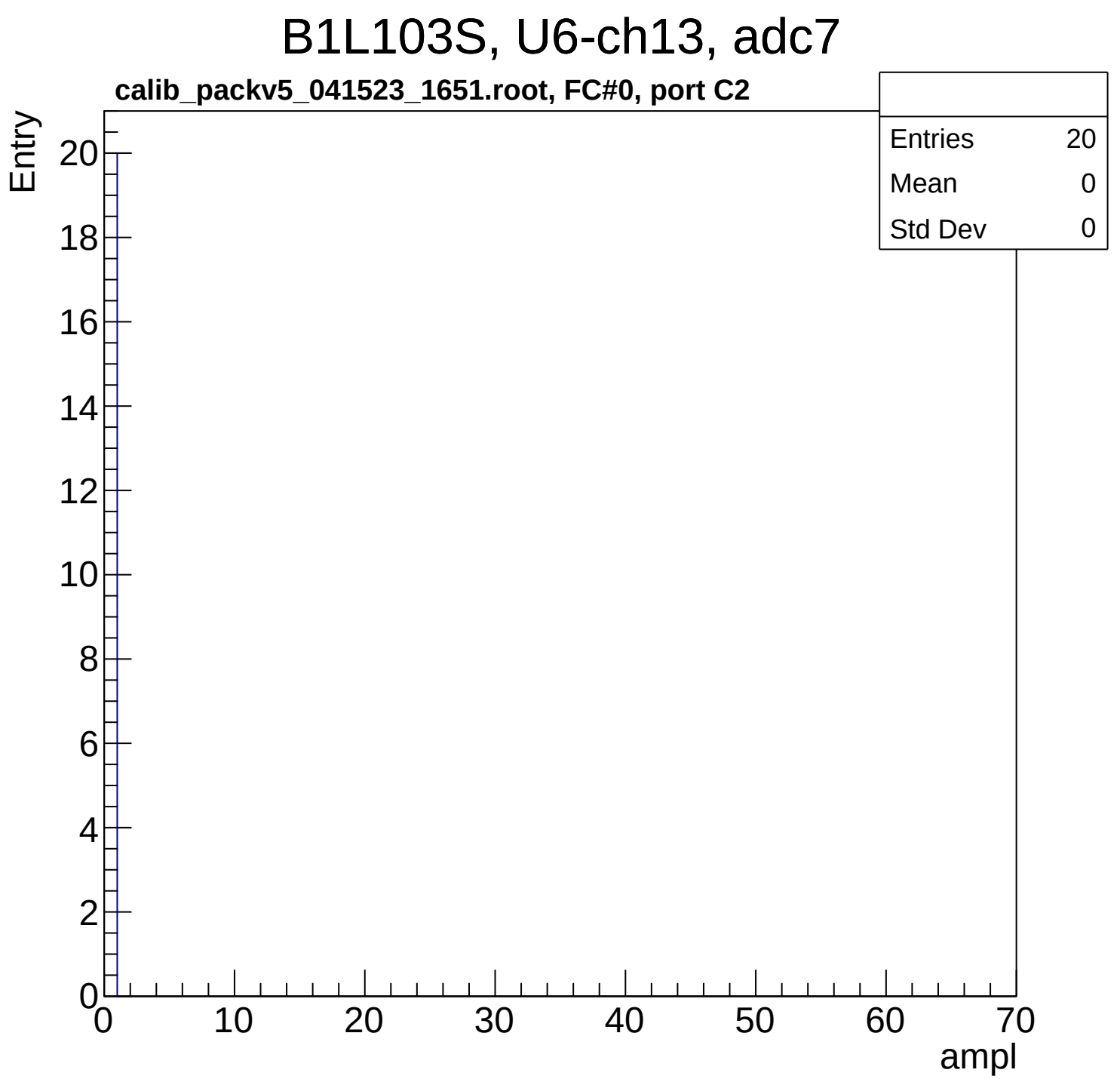
B1L103S, U6-ch13, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 0
Std Dev 0
Entry
0
2
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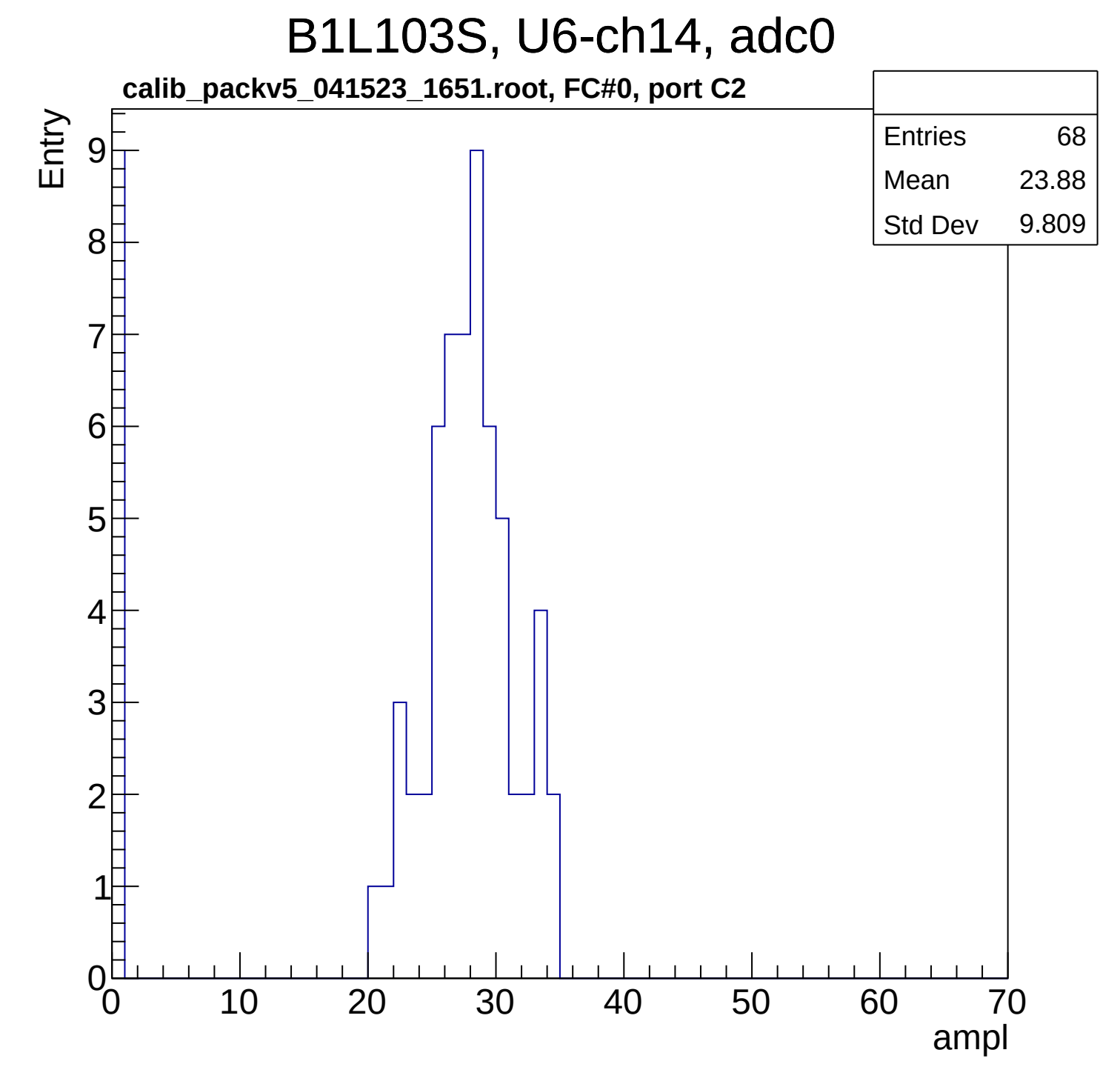
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch14, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 23.88
Std Dev 9.809
Entry
ampl
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2
3
4
5
6
7
8
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0
10
20
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60
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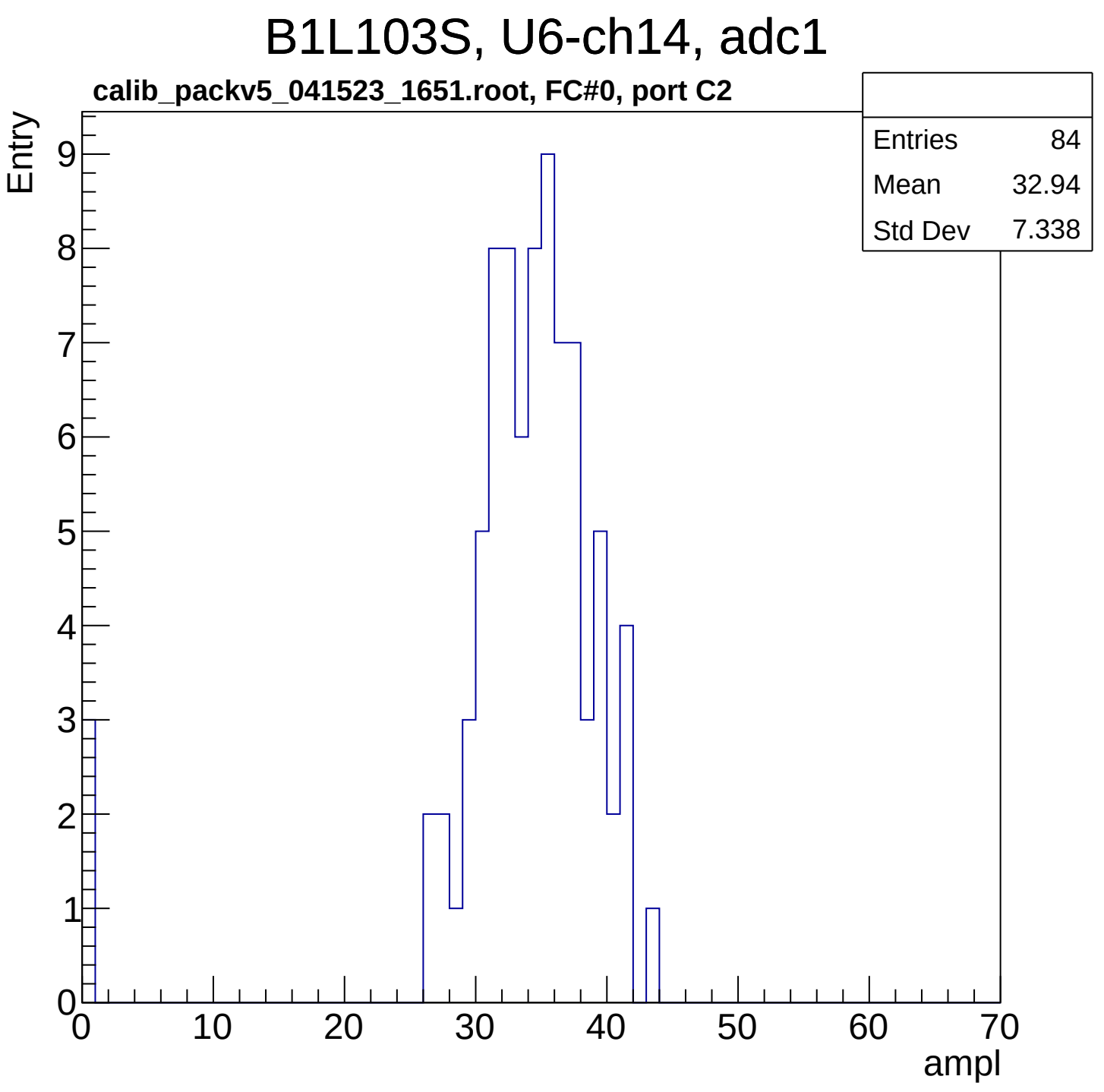
B1L103S, U6-ch14, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 32.94
Std Dev 7.338
Entry
ampl
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2
3
4
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6
7
8
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0
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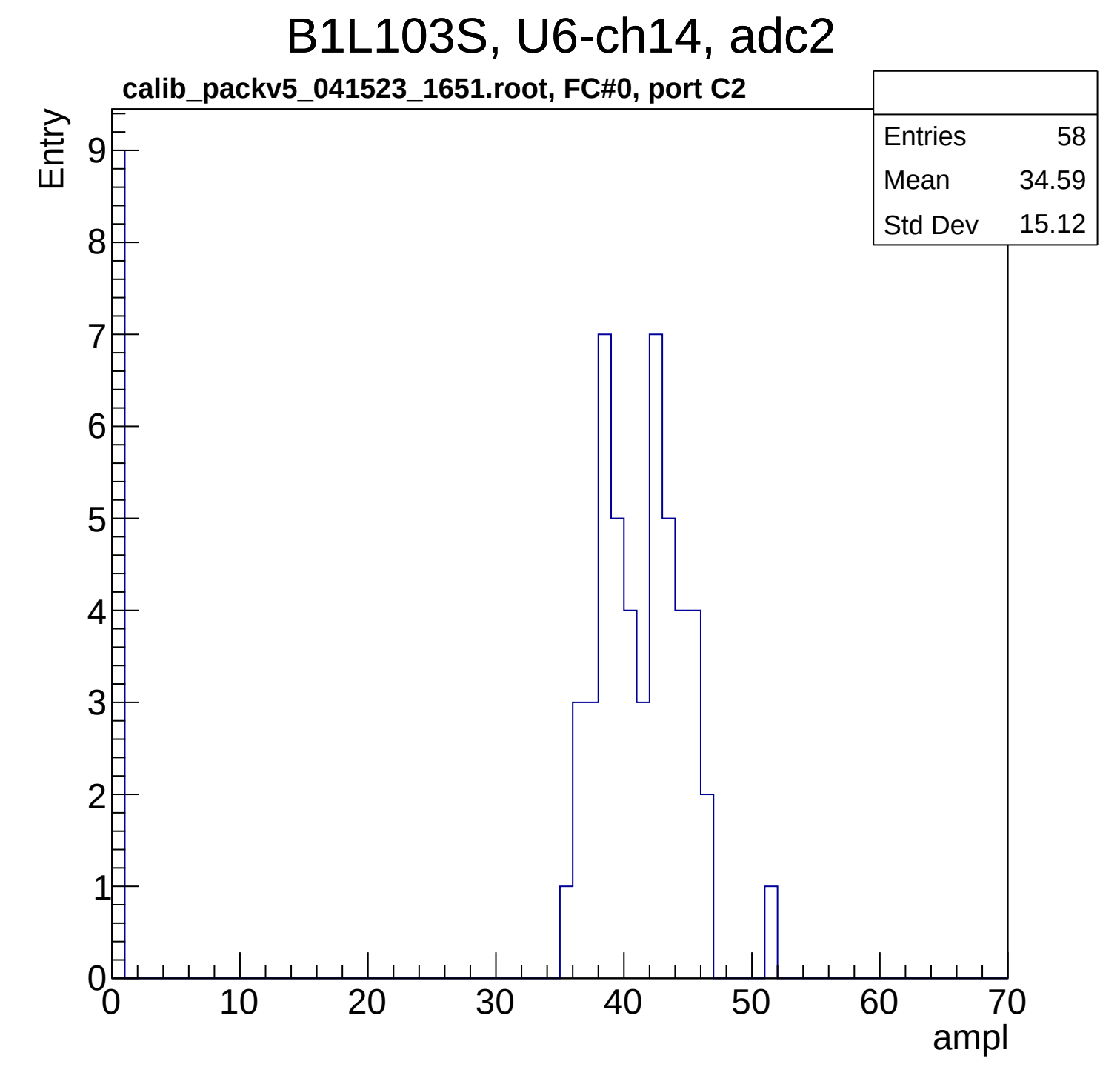
B1L103S, U6-ch14, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 34.59
Std Dev 15.12
Entry
ampl
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2
3
4
5
6
7
8
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0
10
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60
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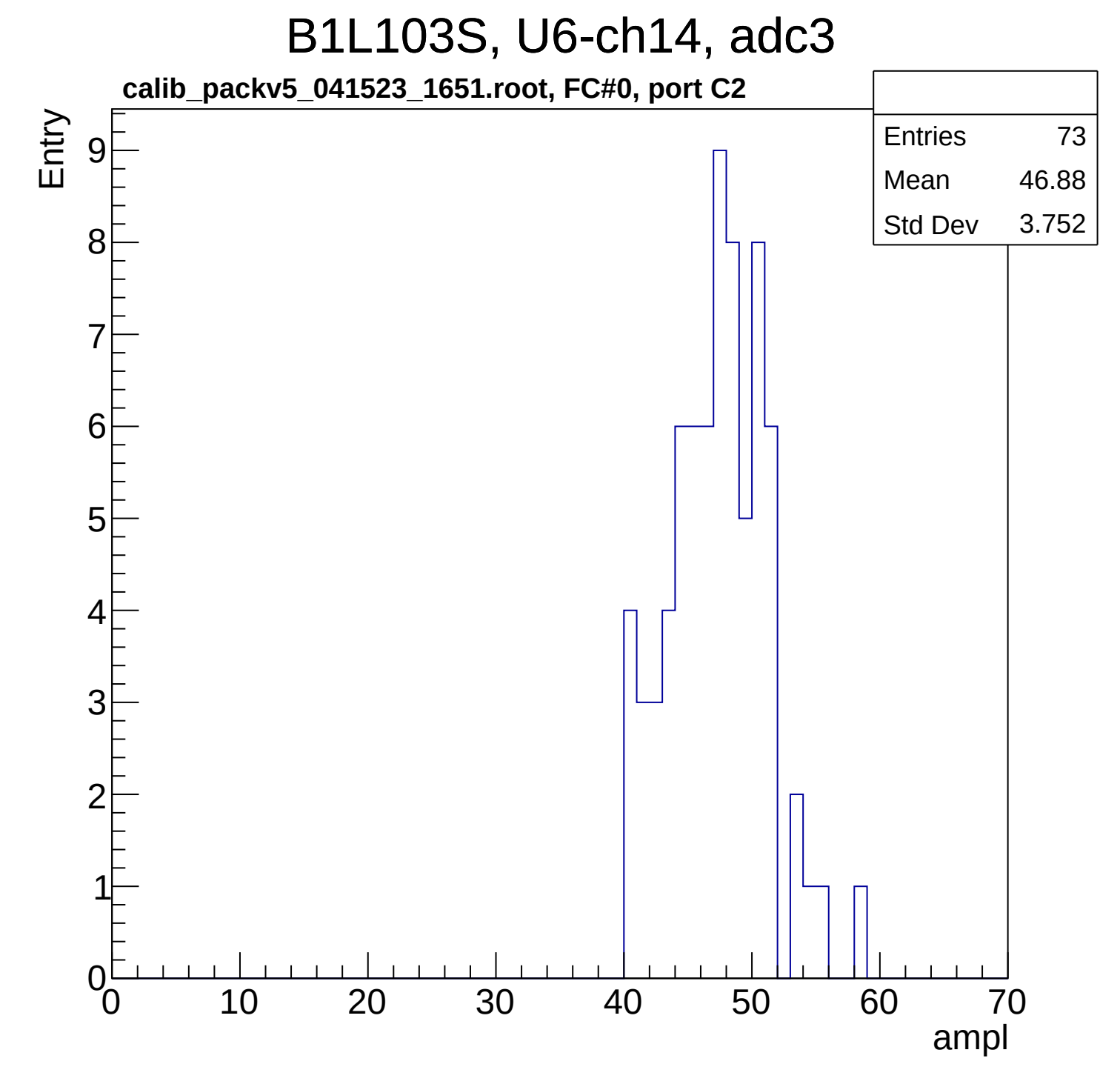
B1L103S, U6-ch14, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 46.88
Std Dev 3.752
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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60
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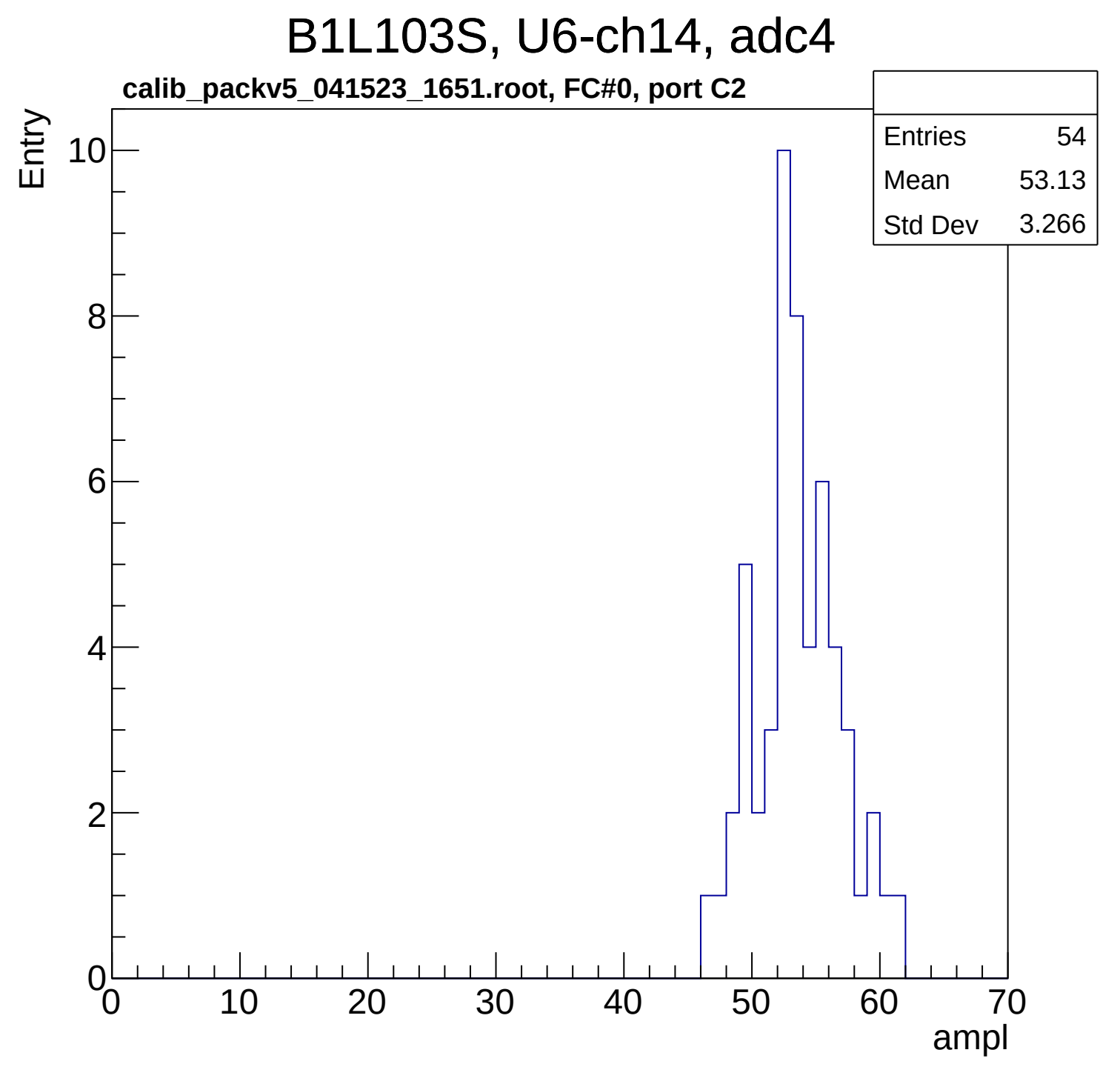
B1L103S, U6-ch14, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 53.13
Std Dev 3.266
Entry
ampl
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2
4
6
8
10
0
10
20
30
40
50
60
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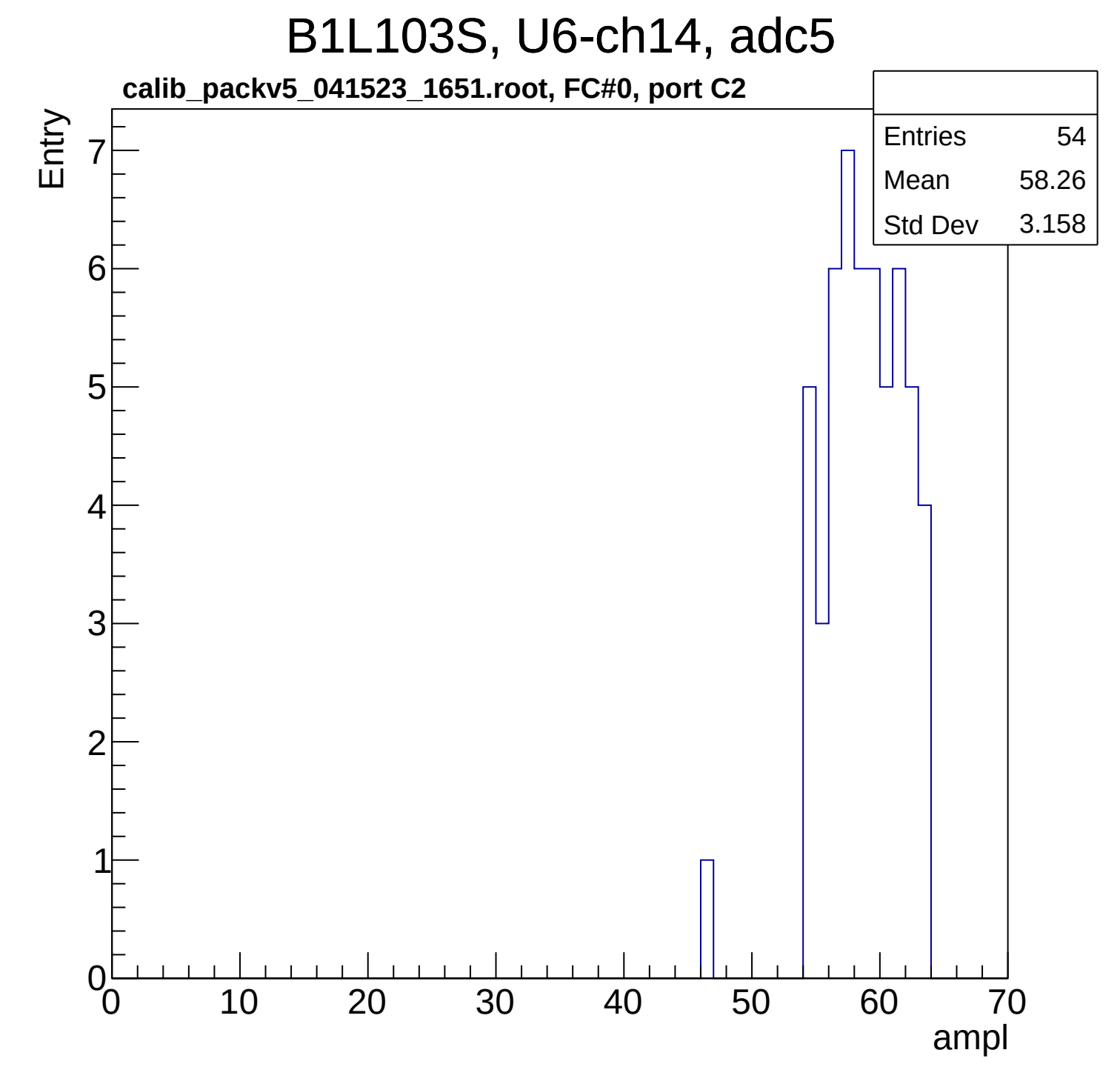
B1L103S, U6-ch14, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 58.26
Std Dev 3.158
Entry
ampl
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2
3
4
5
6
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0
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40
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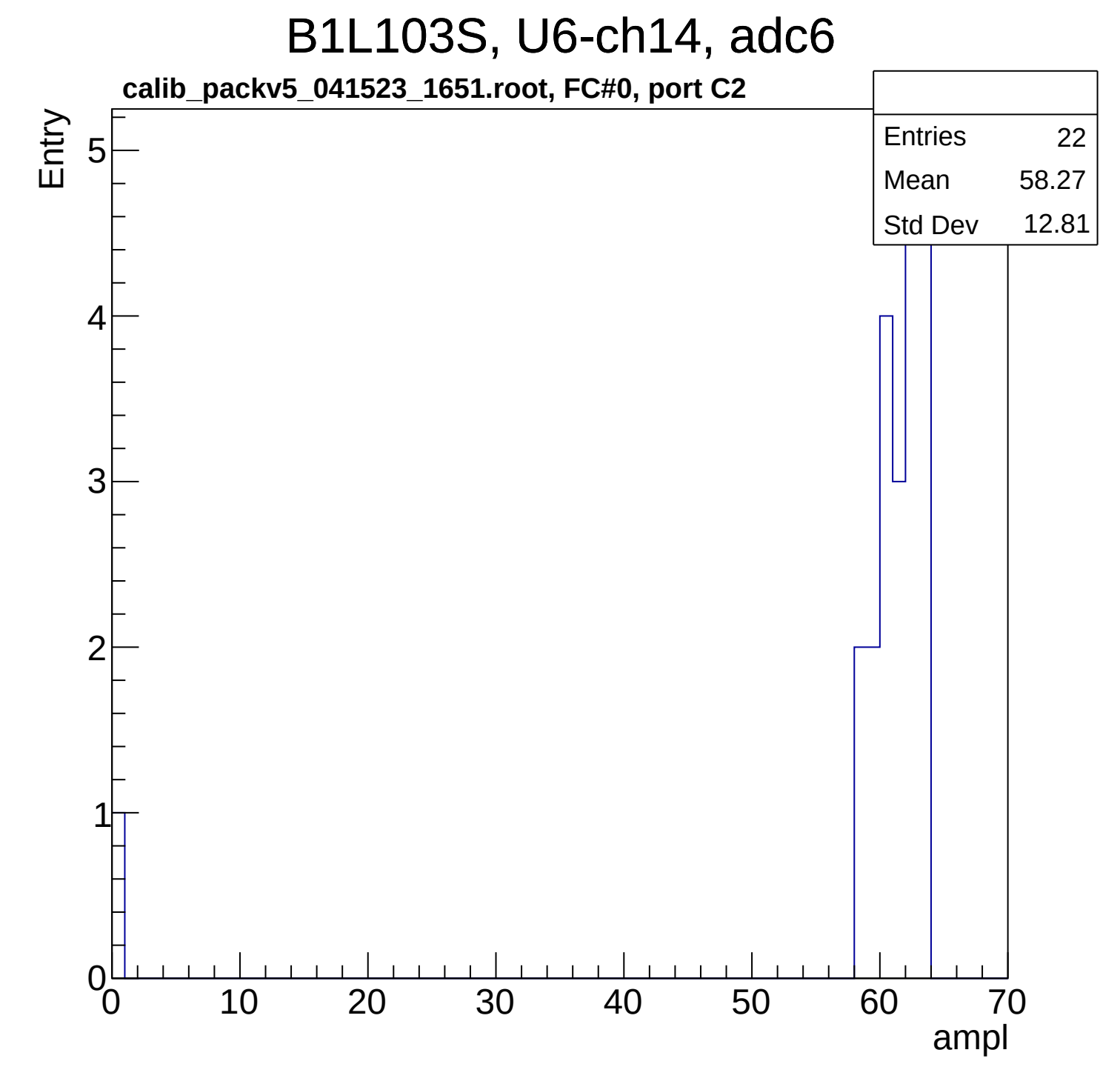
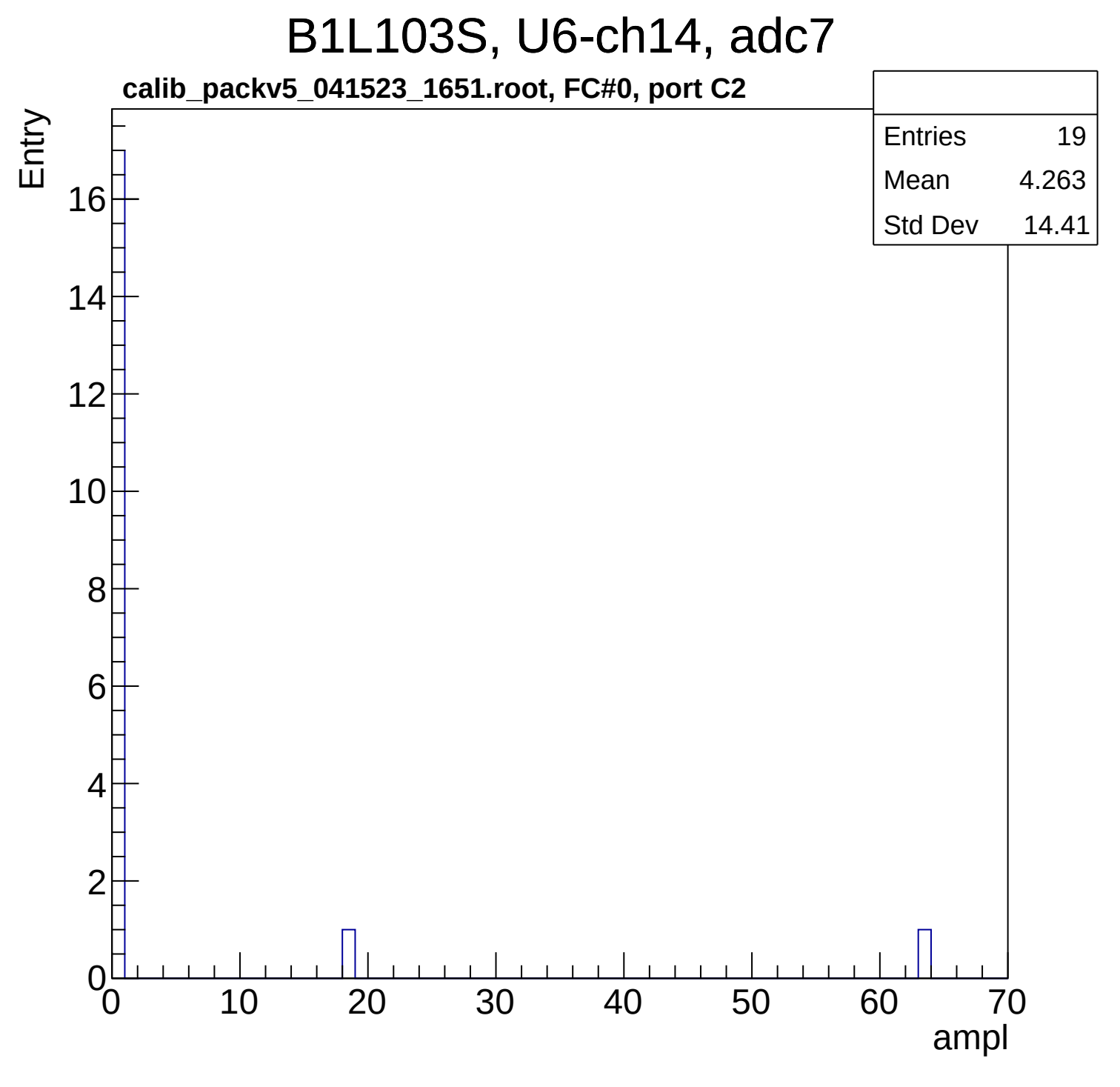

B1L103S, U6-ch14, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 58.27
Std Dev 12.81
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch14, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 4.263
Std Dev 14.41
Entry
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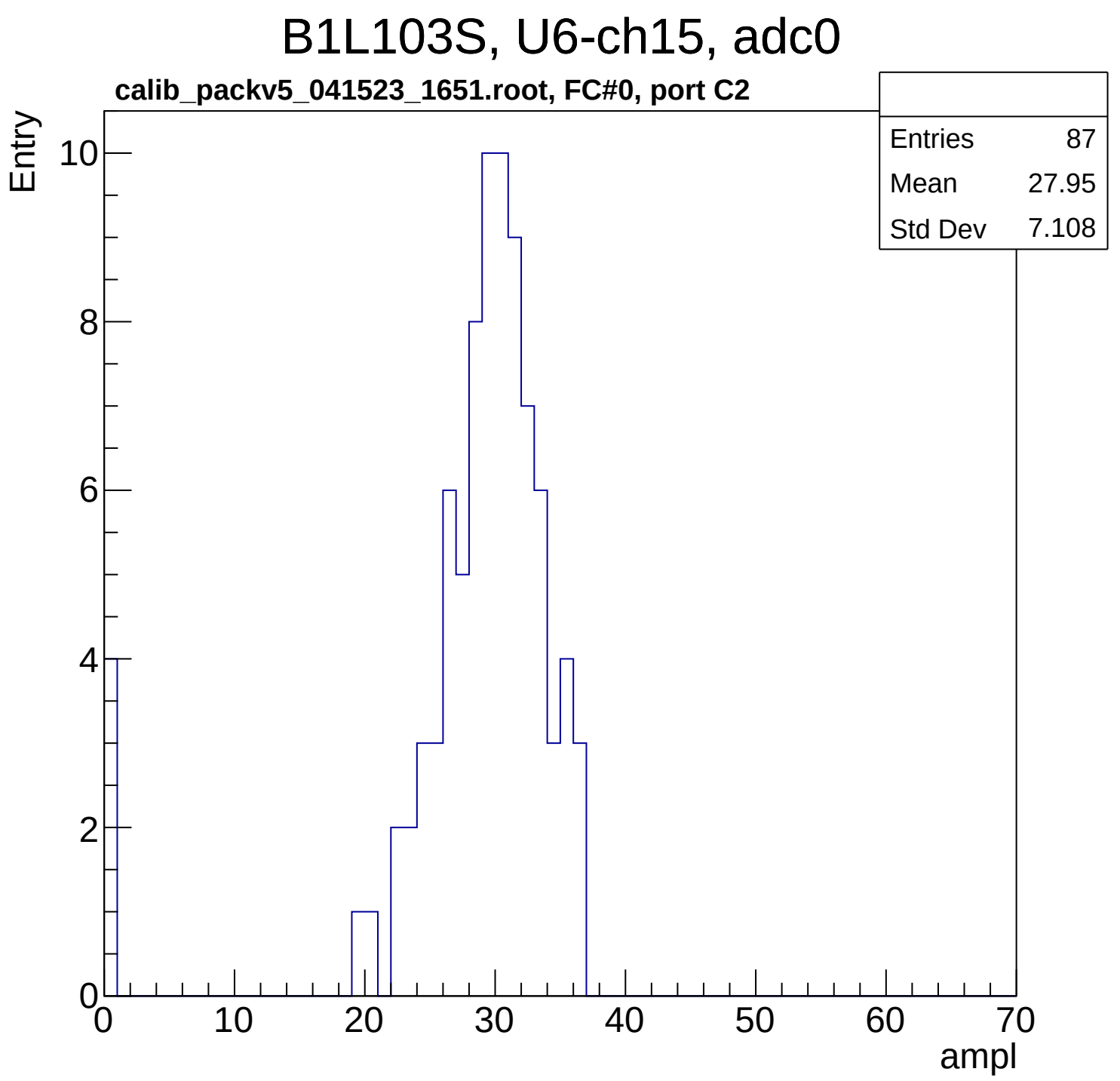
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch15, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 27.95
Std Dev 7.108
Entry
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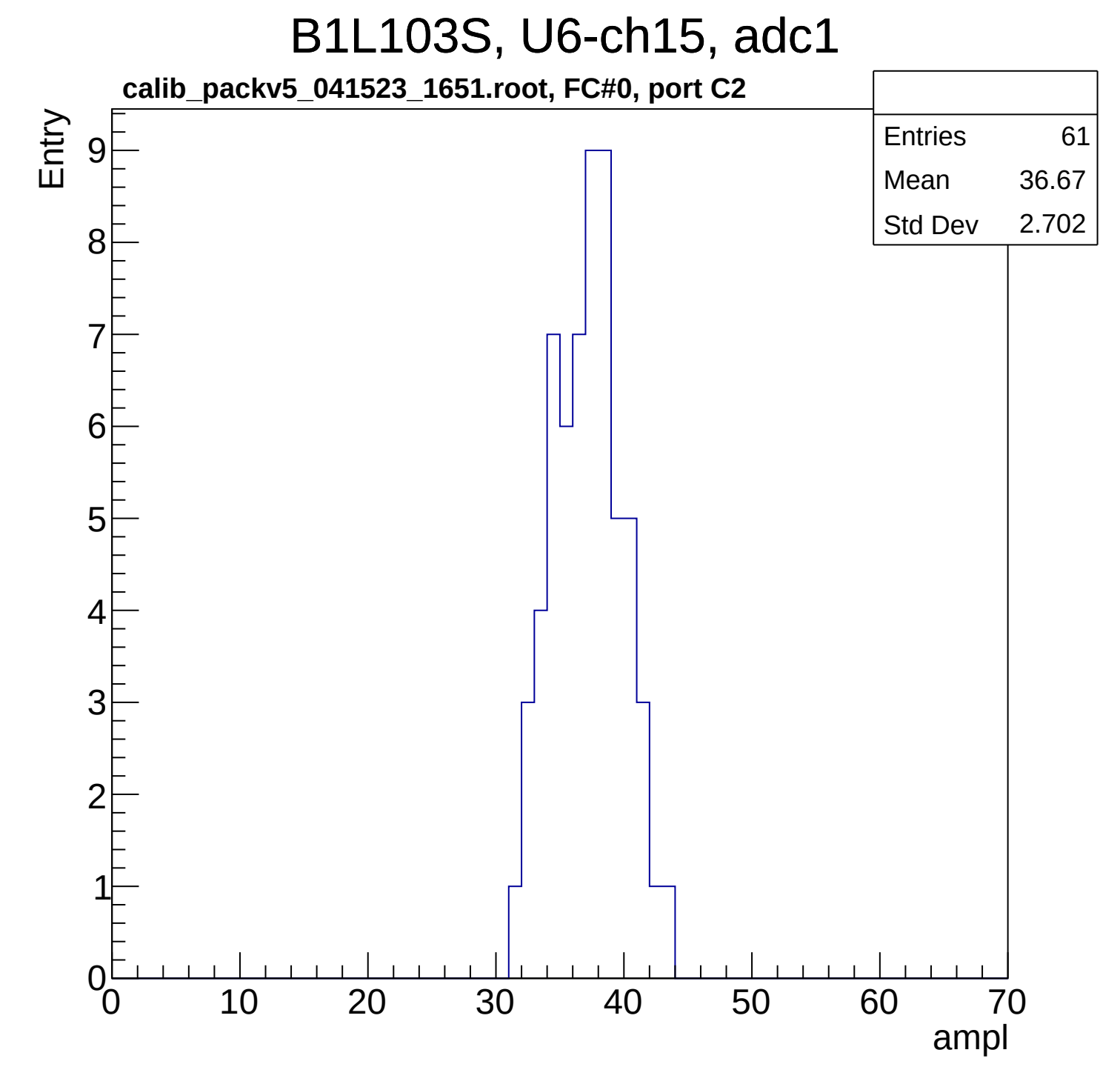
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch15, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 36.67
Std Dev 2.702
Entry
ampl
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2
3
4
5
6
7
8
9
0
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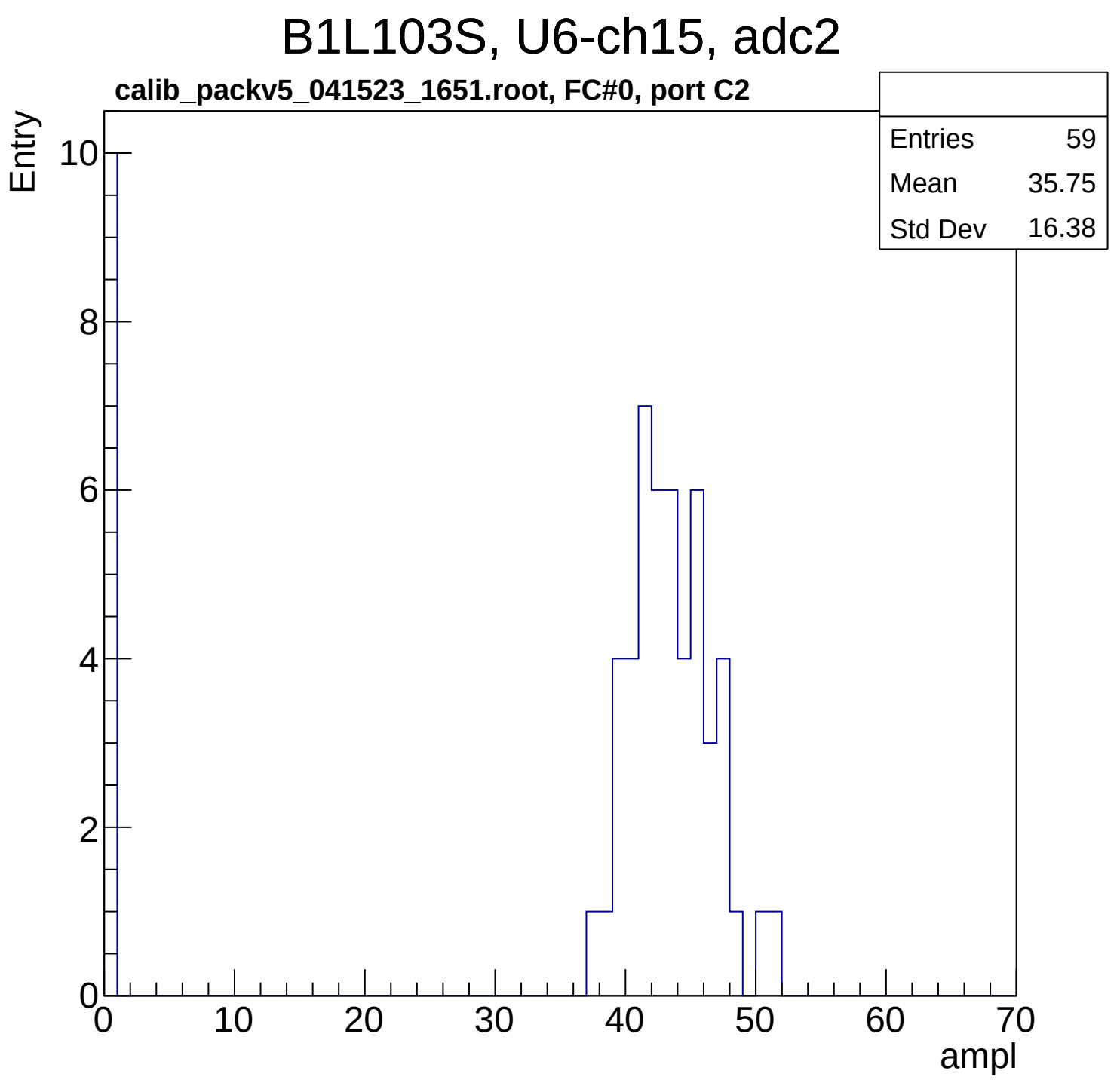
B1L103S, U6-ch15, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 35.75
Std Dev 16.38
Entry
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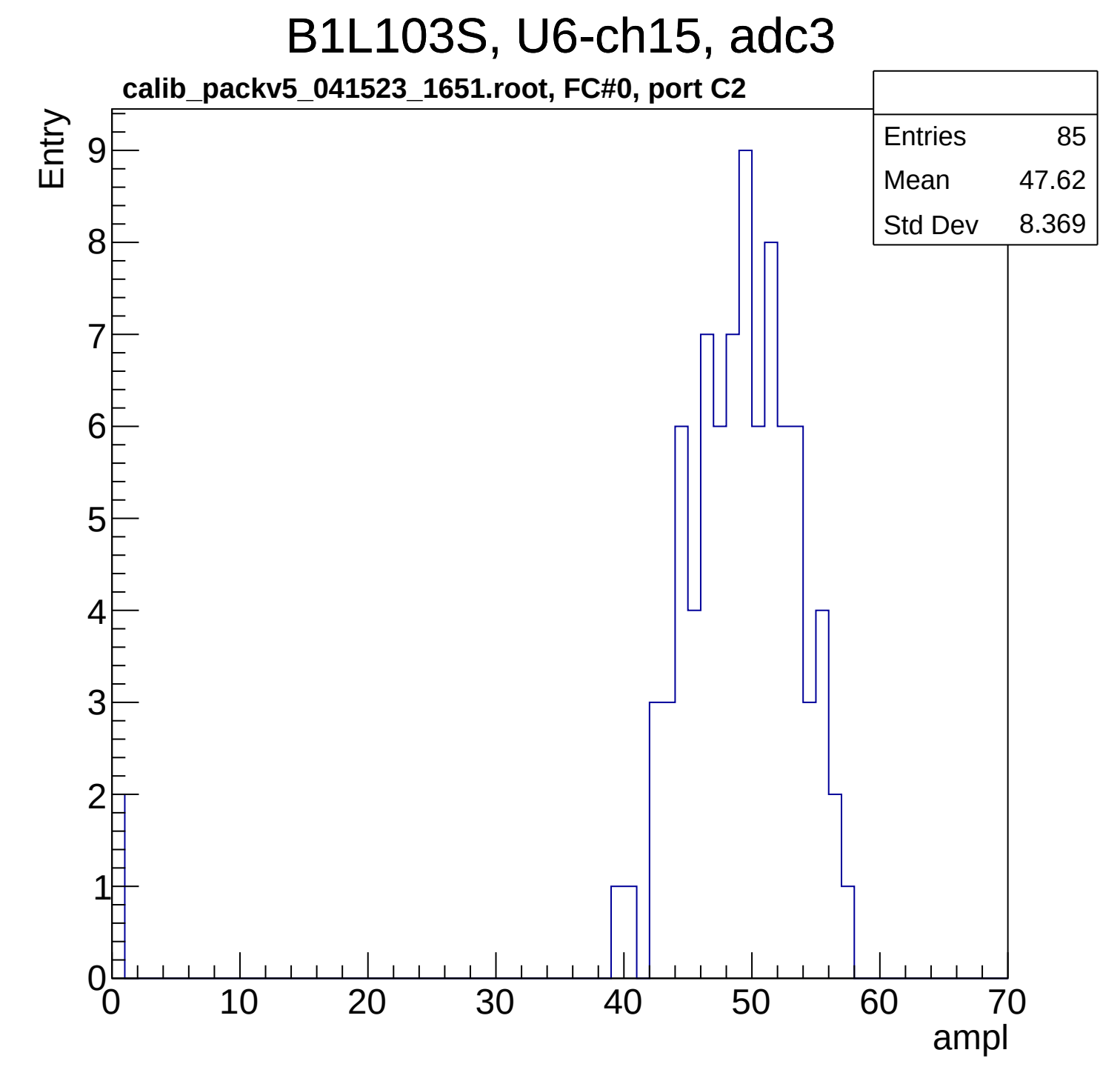
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch15, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 47.62
Std Dev 8.369
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
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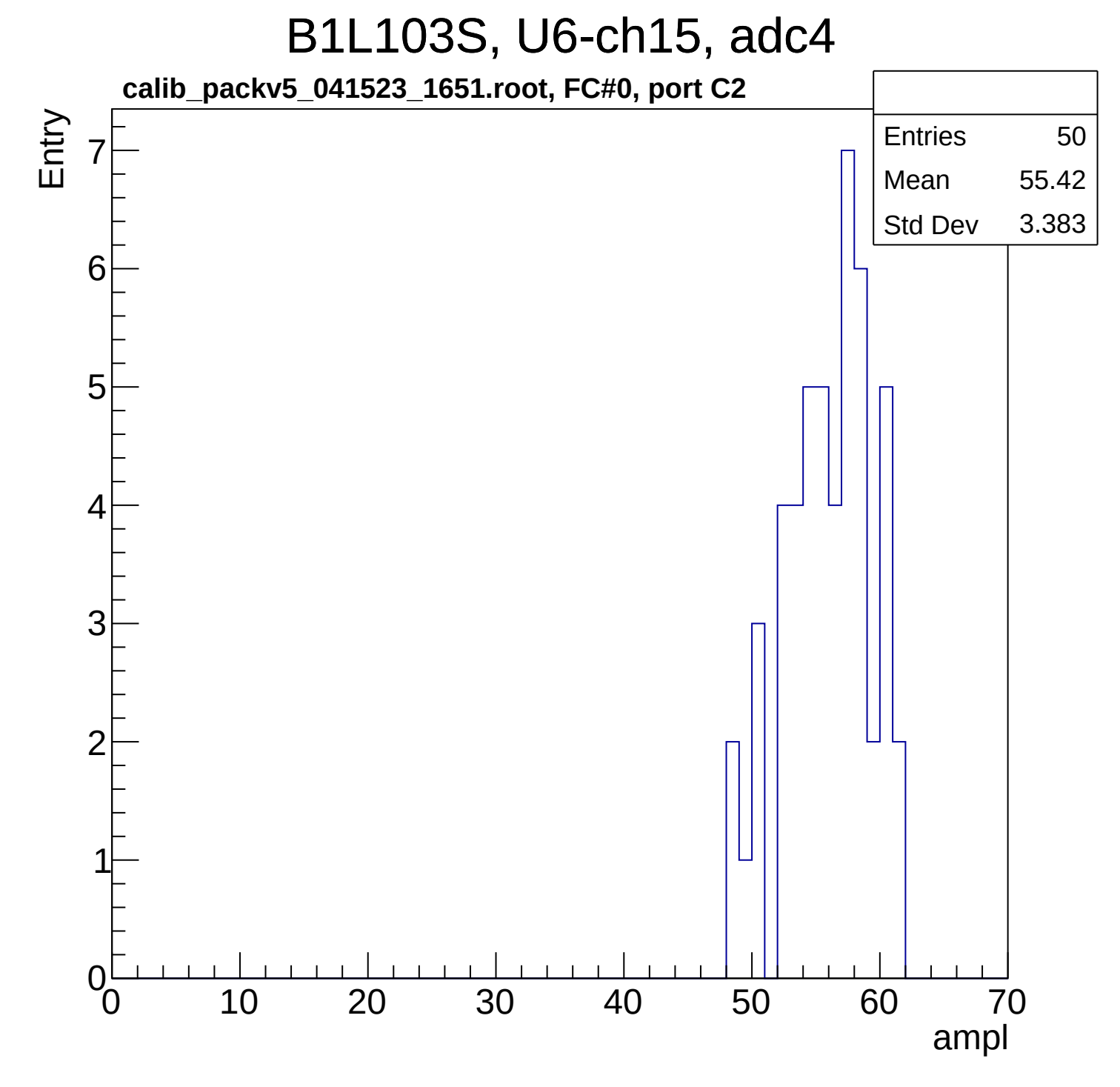
60
70


B1L103S, U6-ch15, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 55.42
Std Dev 3.383
Entry
ampl
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2
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4
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0
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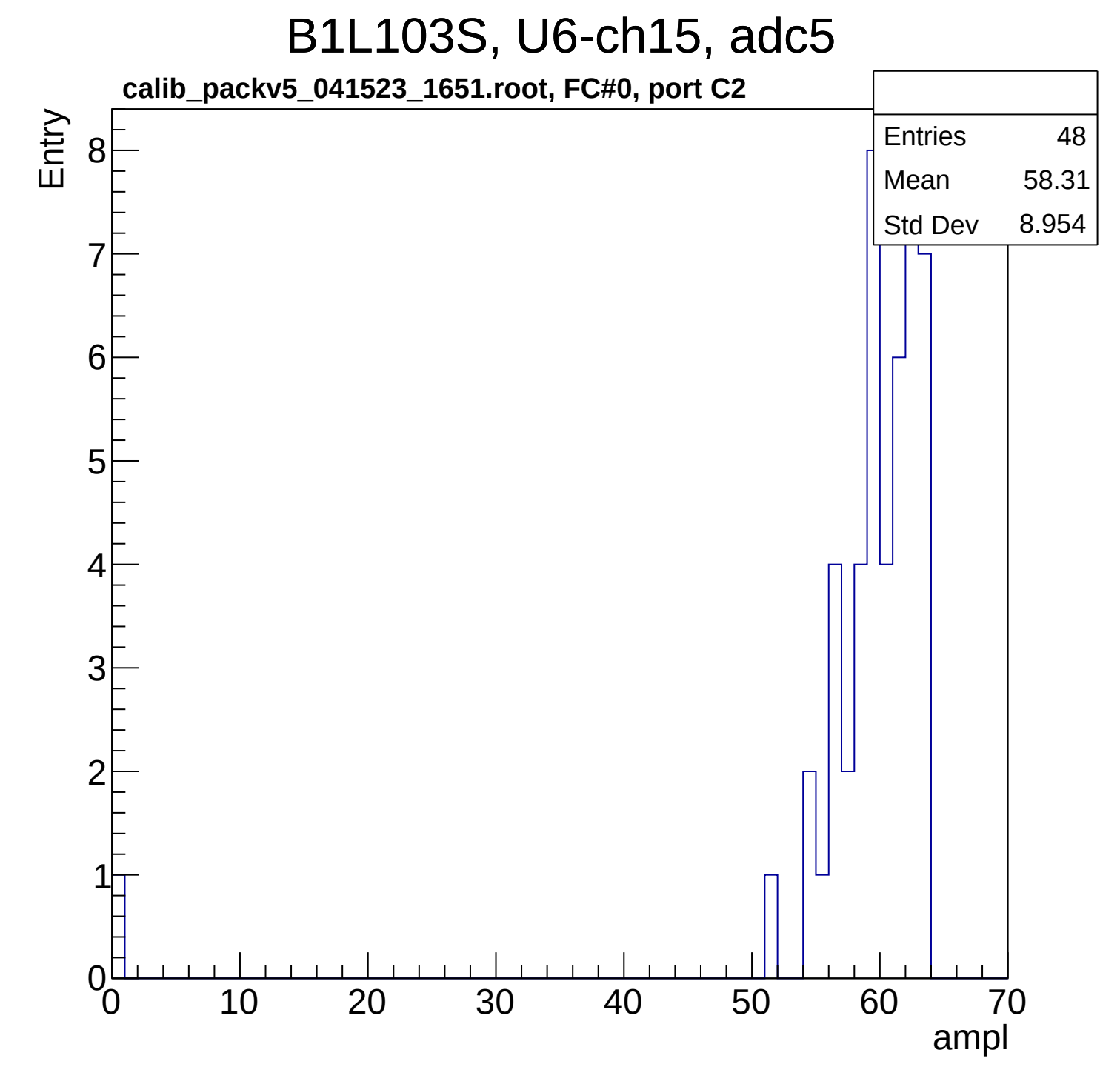
B1L103S, U6-ch15, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 58.31
Std Dev 8.954
Entry
ampl
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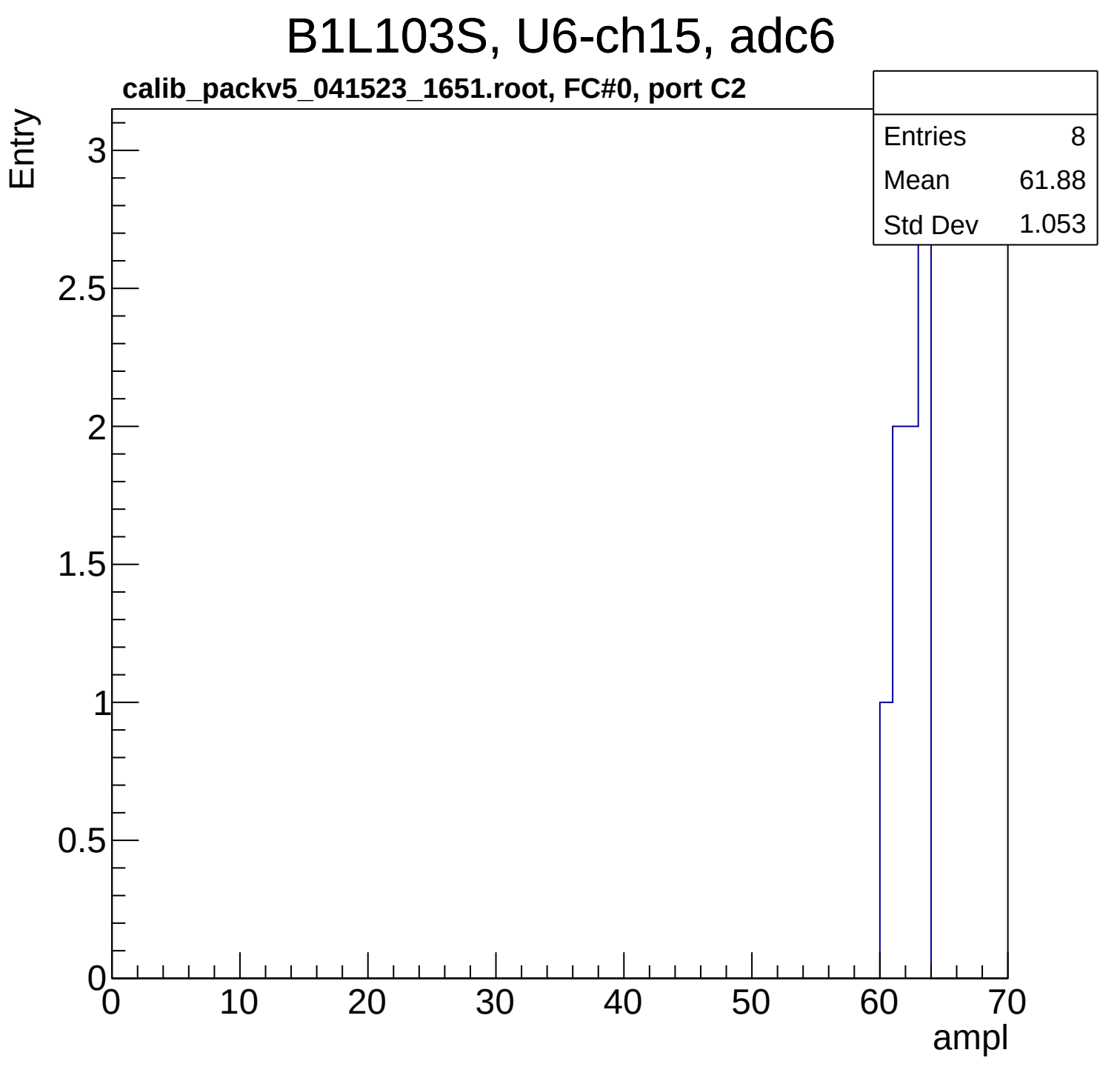
B1L103S, U6-ch15, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 61.88
Std Dev 1.053
Entry
ampl
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0.5
1
1.5
2
2.5
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0
10
20
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40
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60
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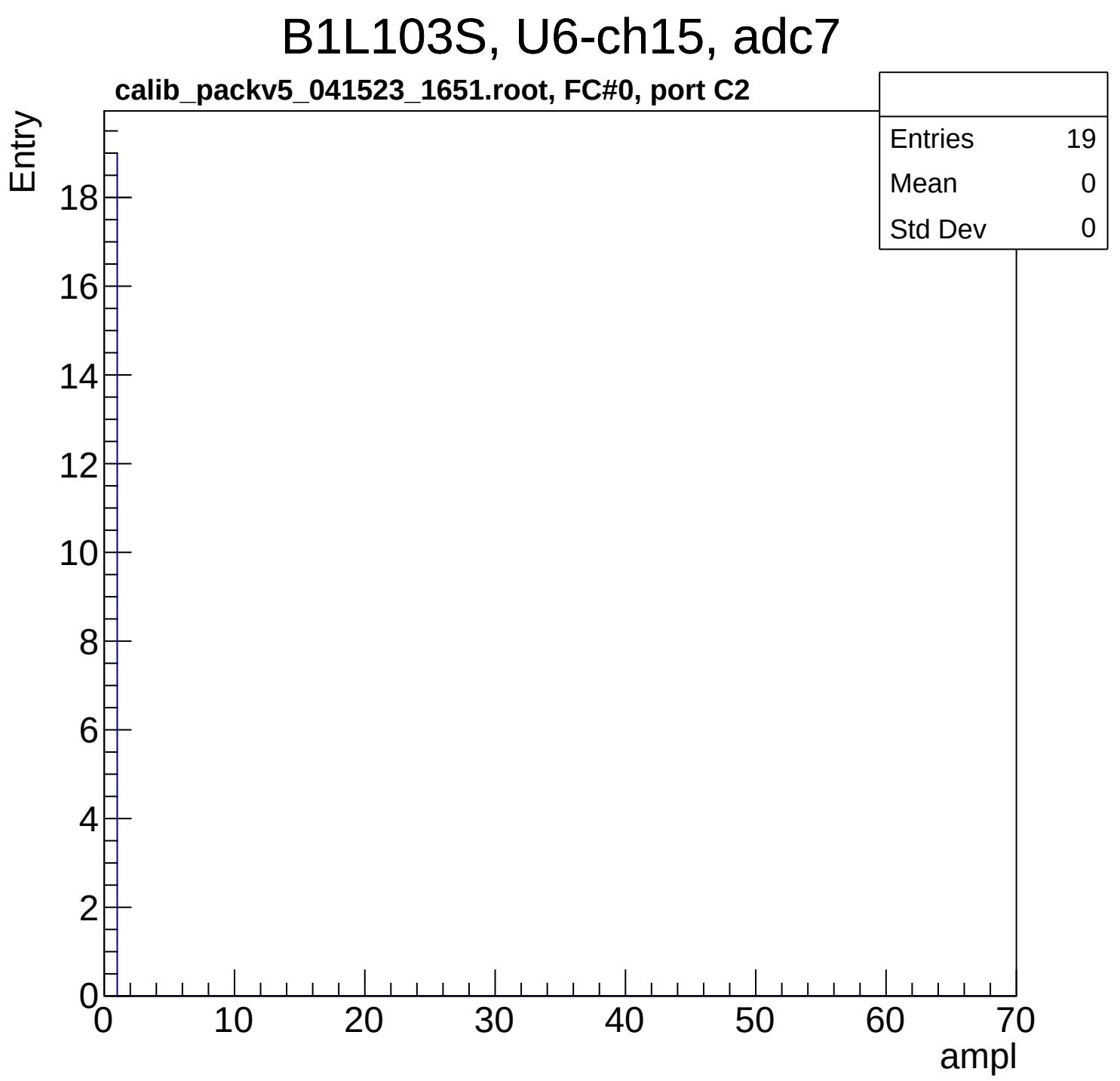
B1L103S, U6-ch15, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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2
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6
8
10
12
14
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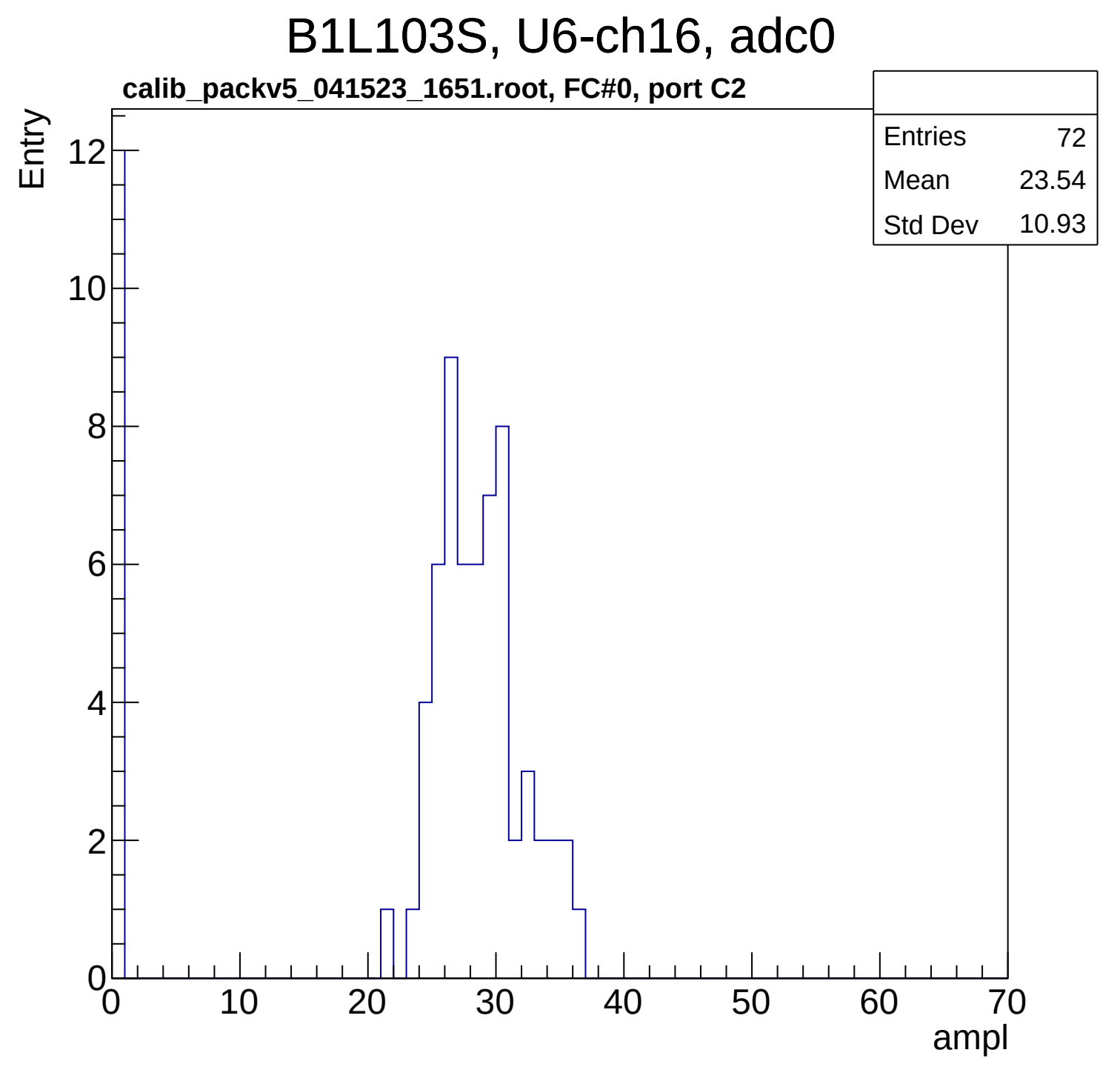
ampl


B1L103S, U6-ch16, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 23.54
Std Dev 10.93
Entry
0
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4
6
8
10
12
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10
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50
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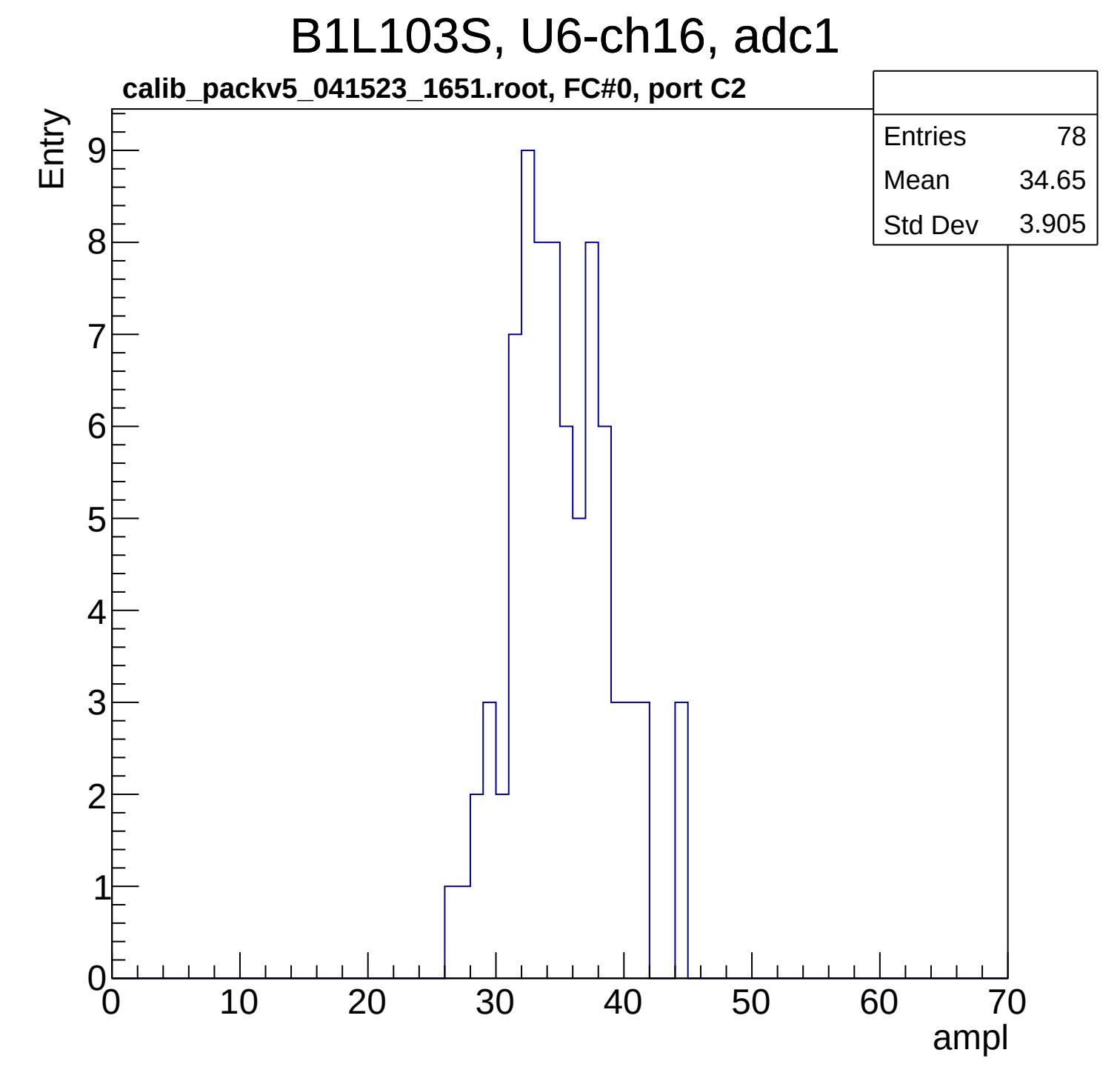
70
ampl


B1L103S, U6-ch16, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 34.65
Std Dev 3.905
Entry
ampl
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0
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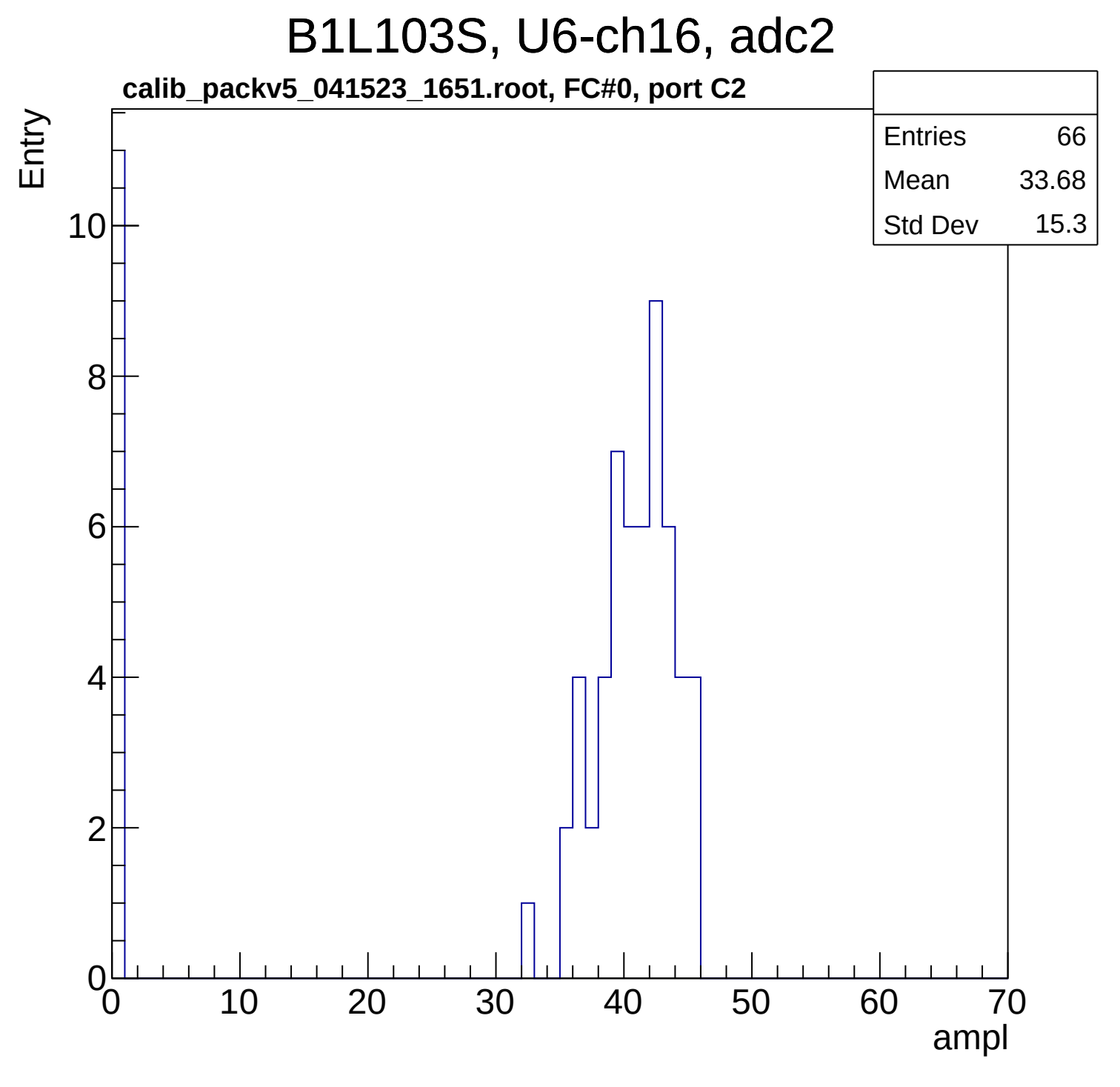
B1L103S, U6-ch16, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 33.68
Std Dev 15.3
Entry
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4
6
8
10
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10
20
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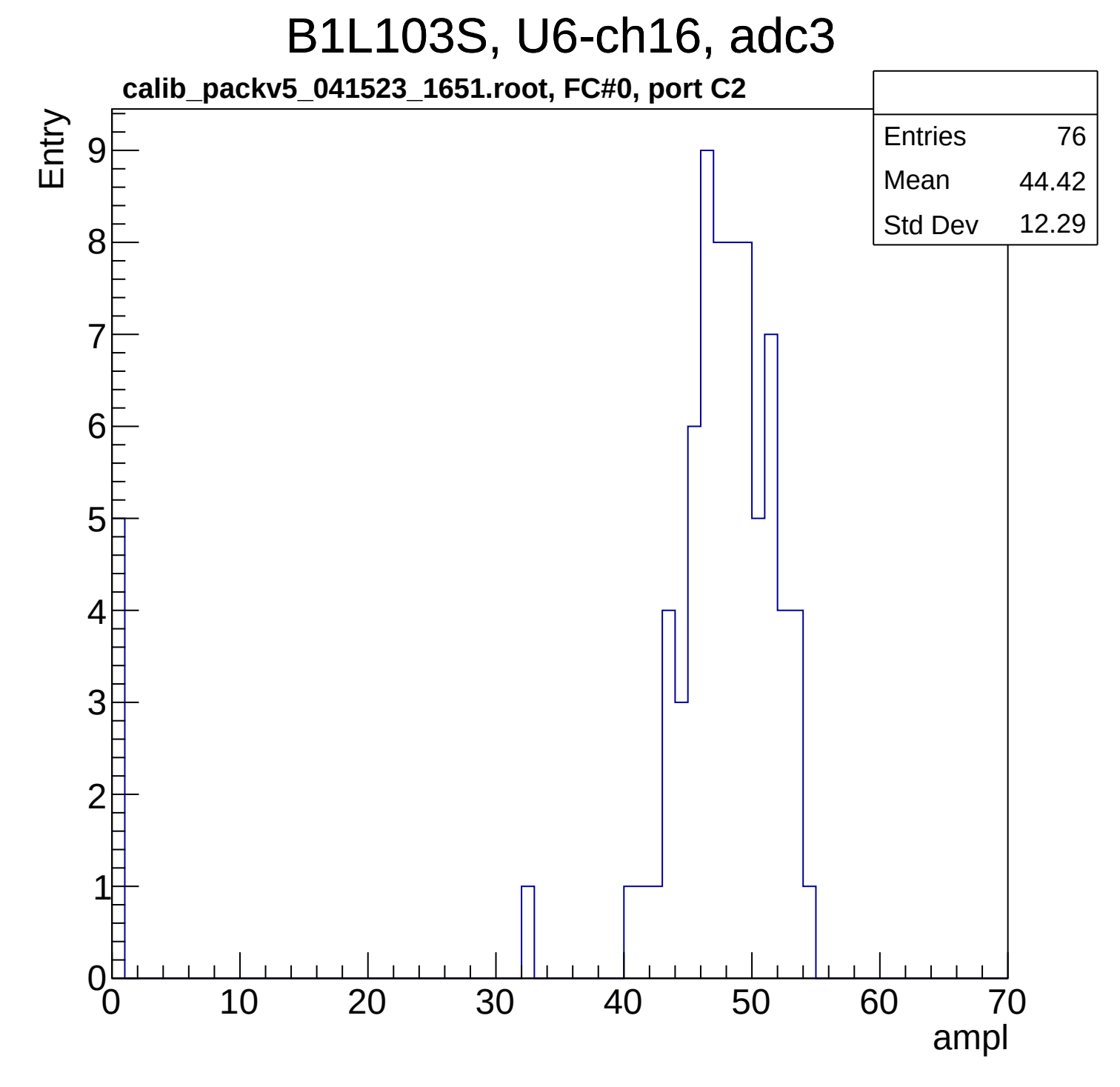
50
60
70
ampl


B1L103S, U6-ch16, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 44.42
Std Dev 12.29
Entry
ampl
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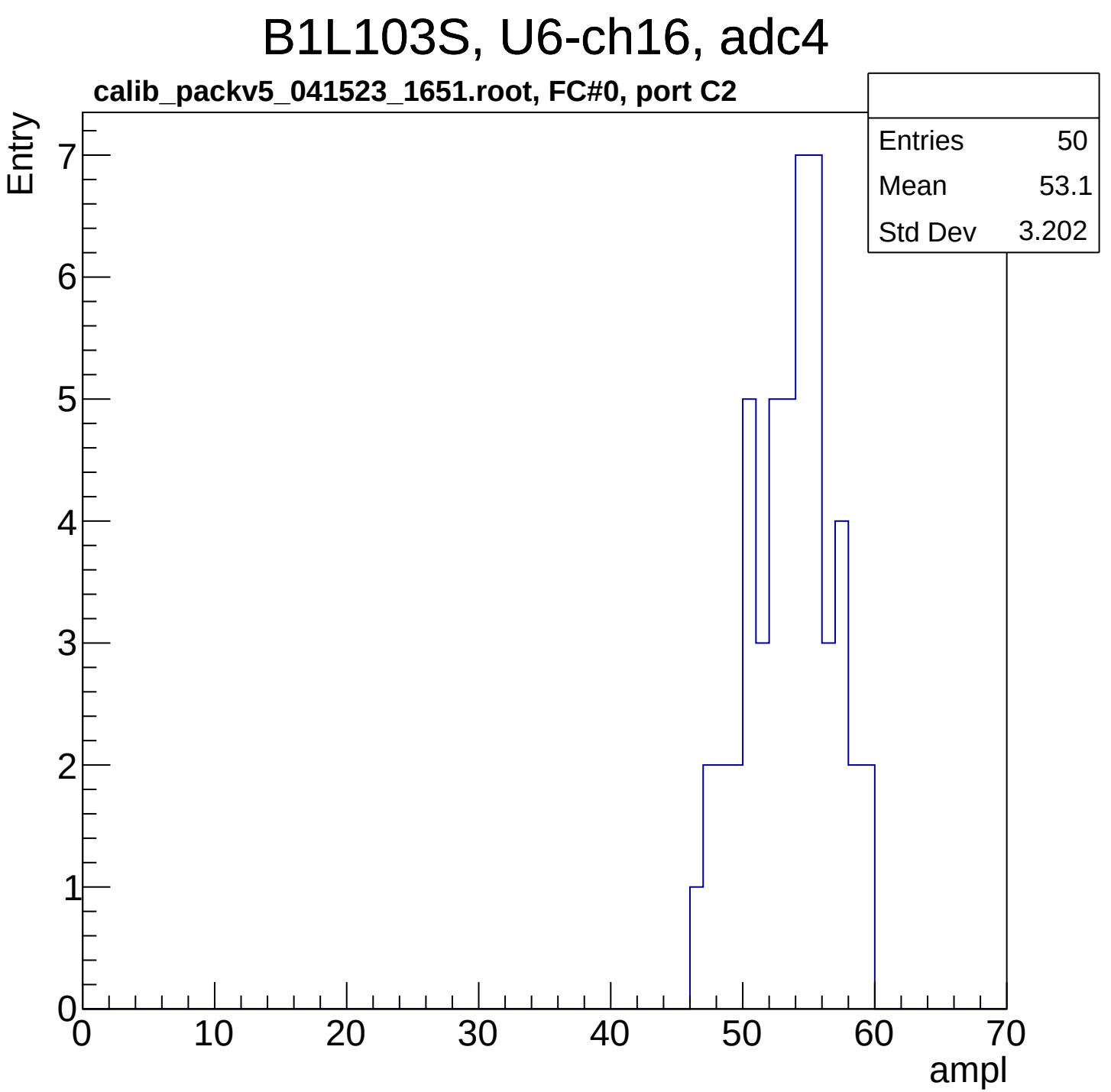
B1L103S, U6-ch16, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 53.1
Std Dev 3.202
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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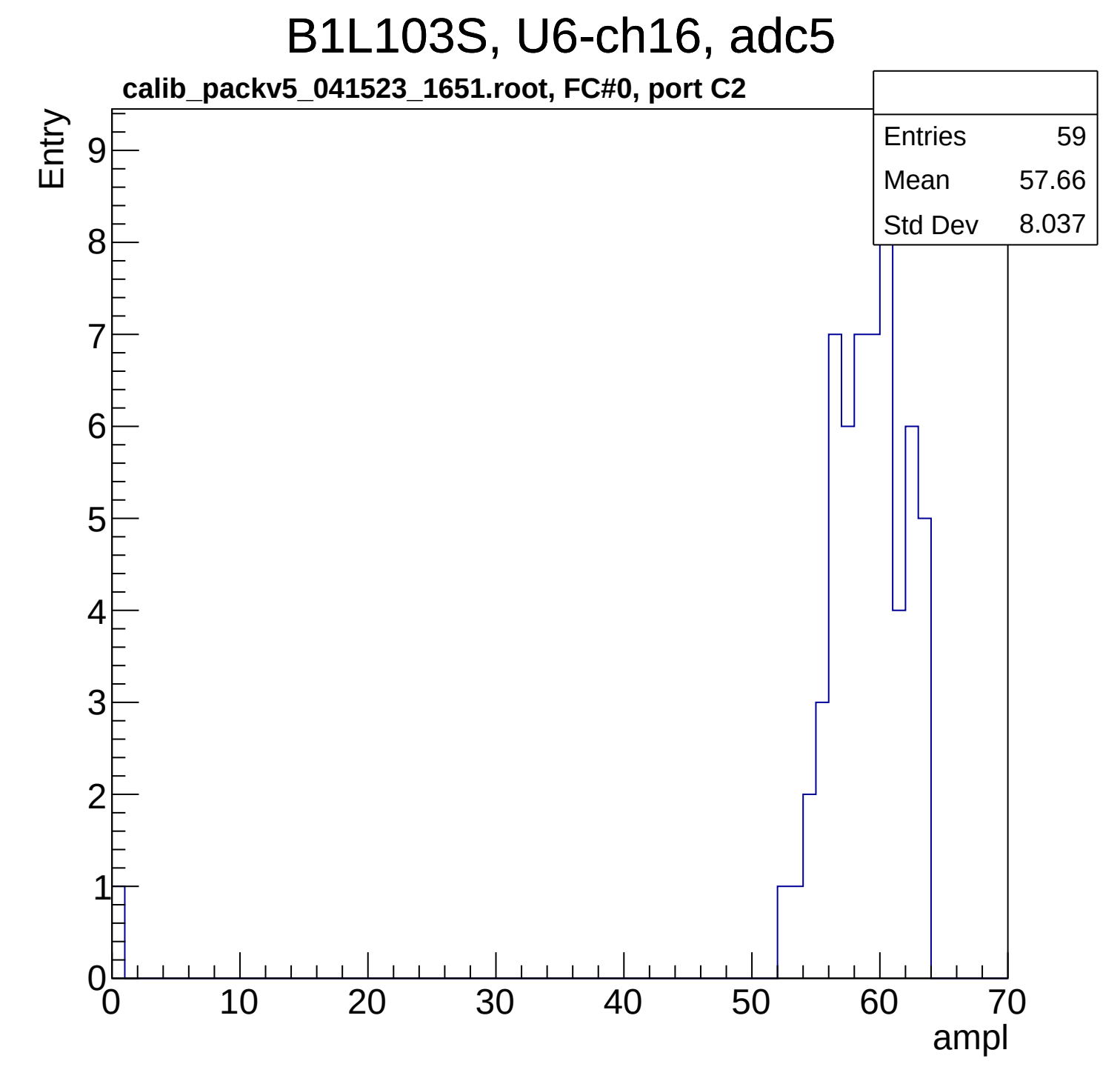
B1L103S, U6-ch16, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 57.66
Std Dev 8.037
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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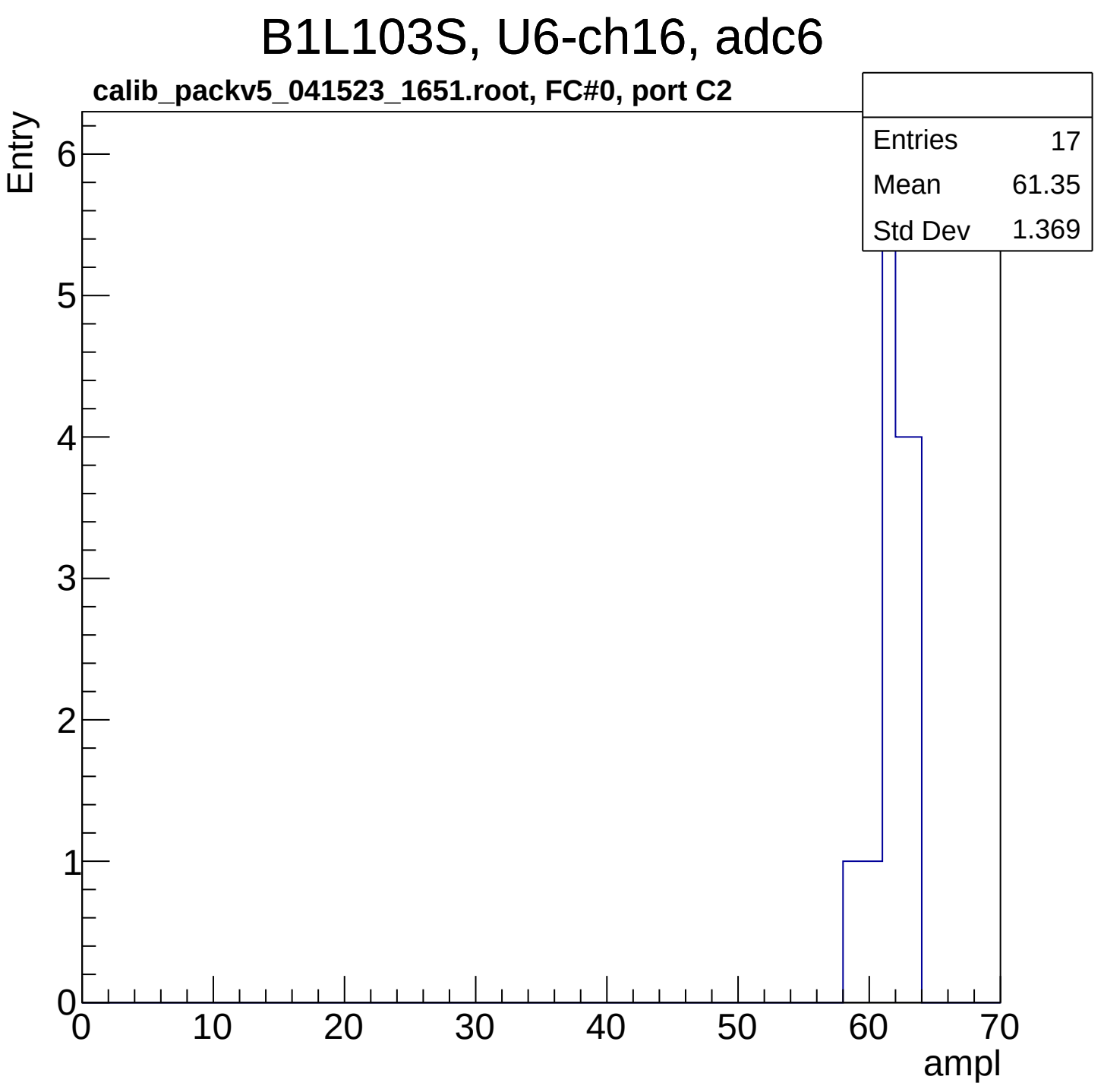
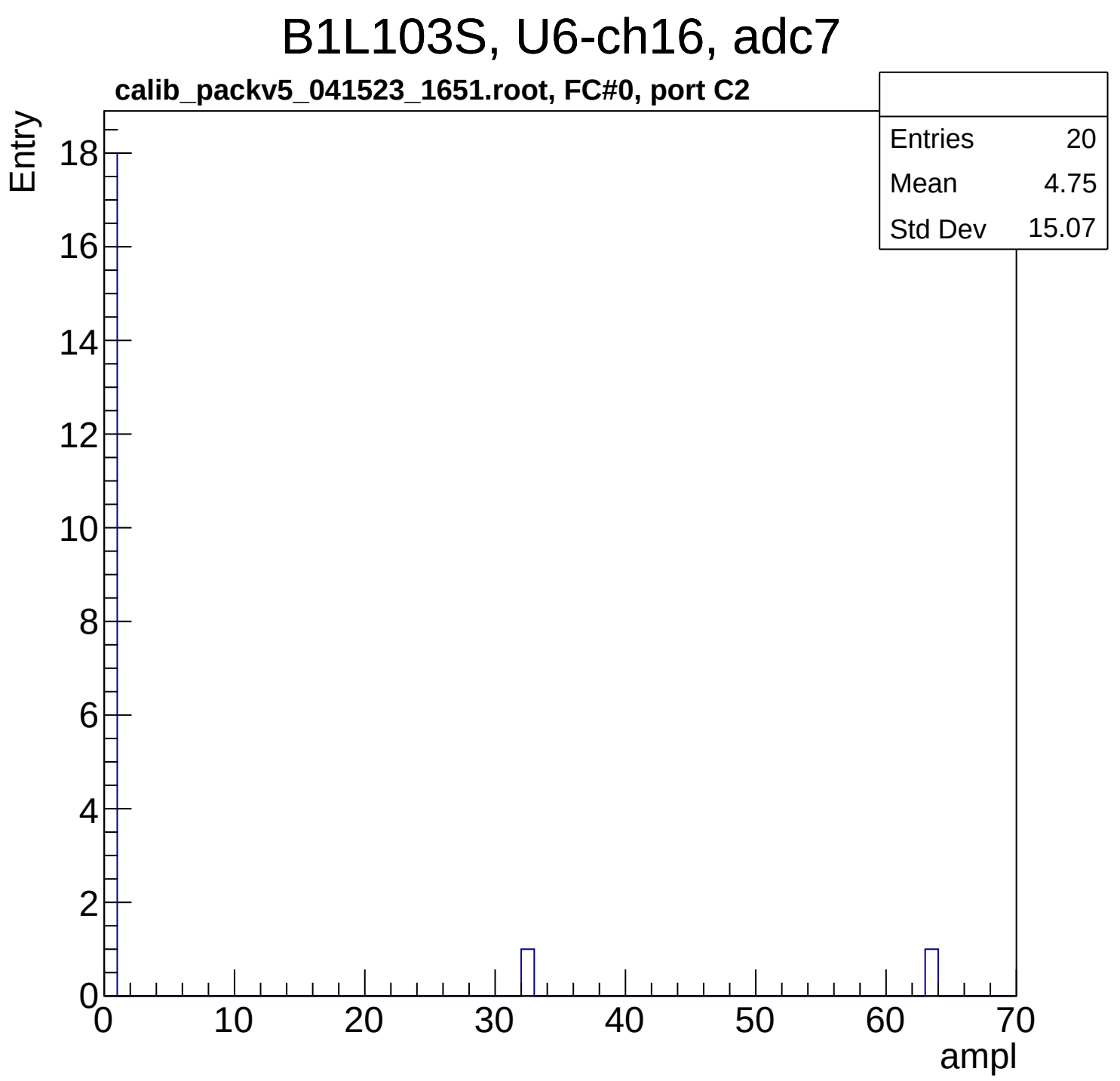

B1L103S, U6-ch16, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 61.35
Std Dev 1.369
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch16, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4.75
Std Dev 15.07
Entry
0
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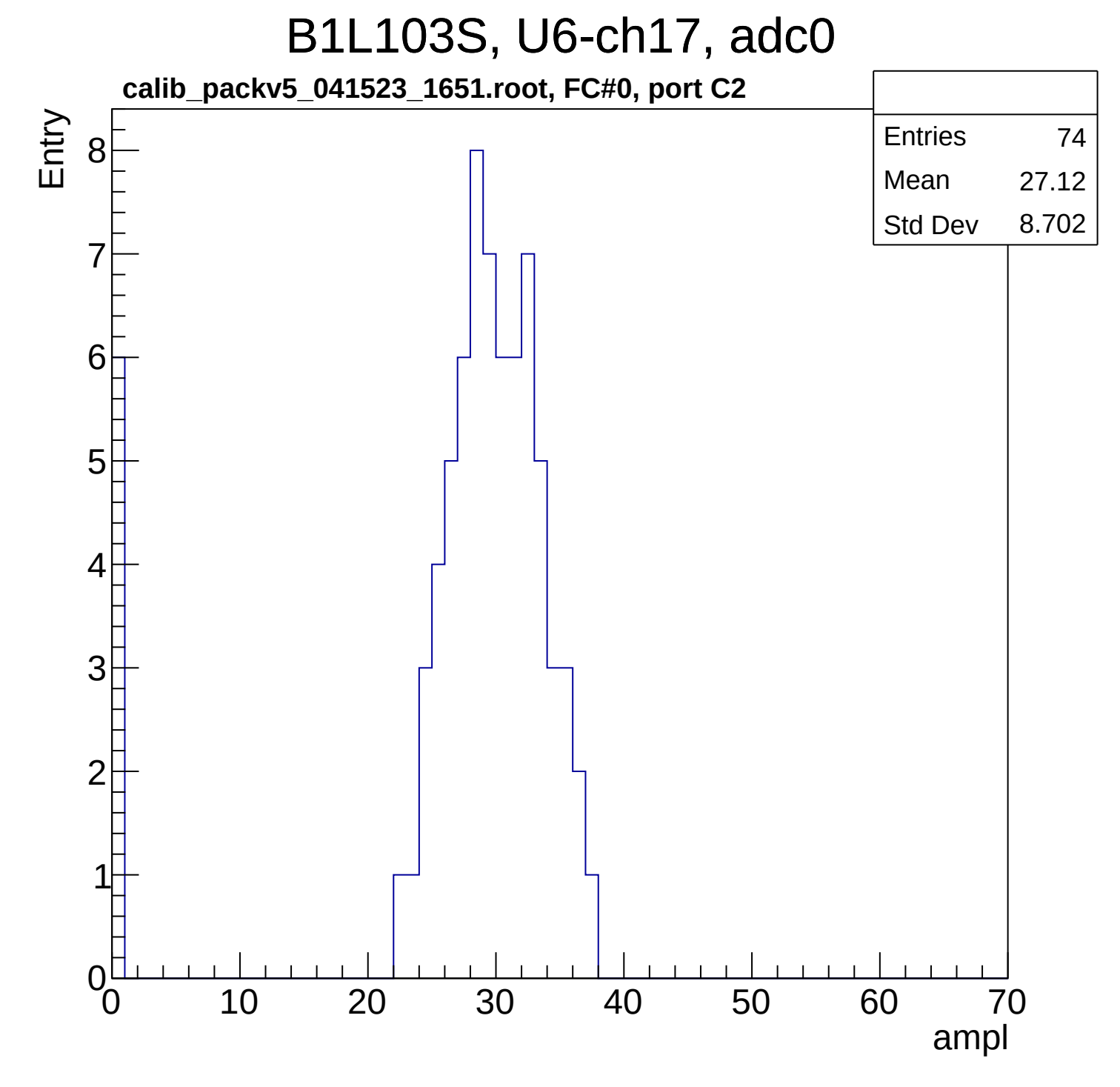
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch17, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 27.12
Std Dev 8.702
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
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40
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60
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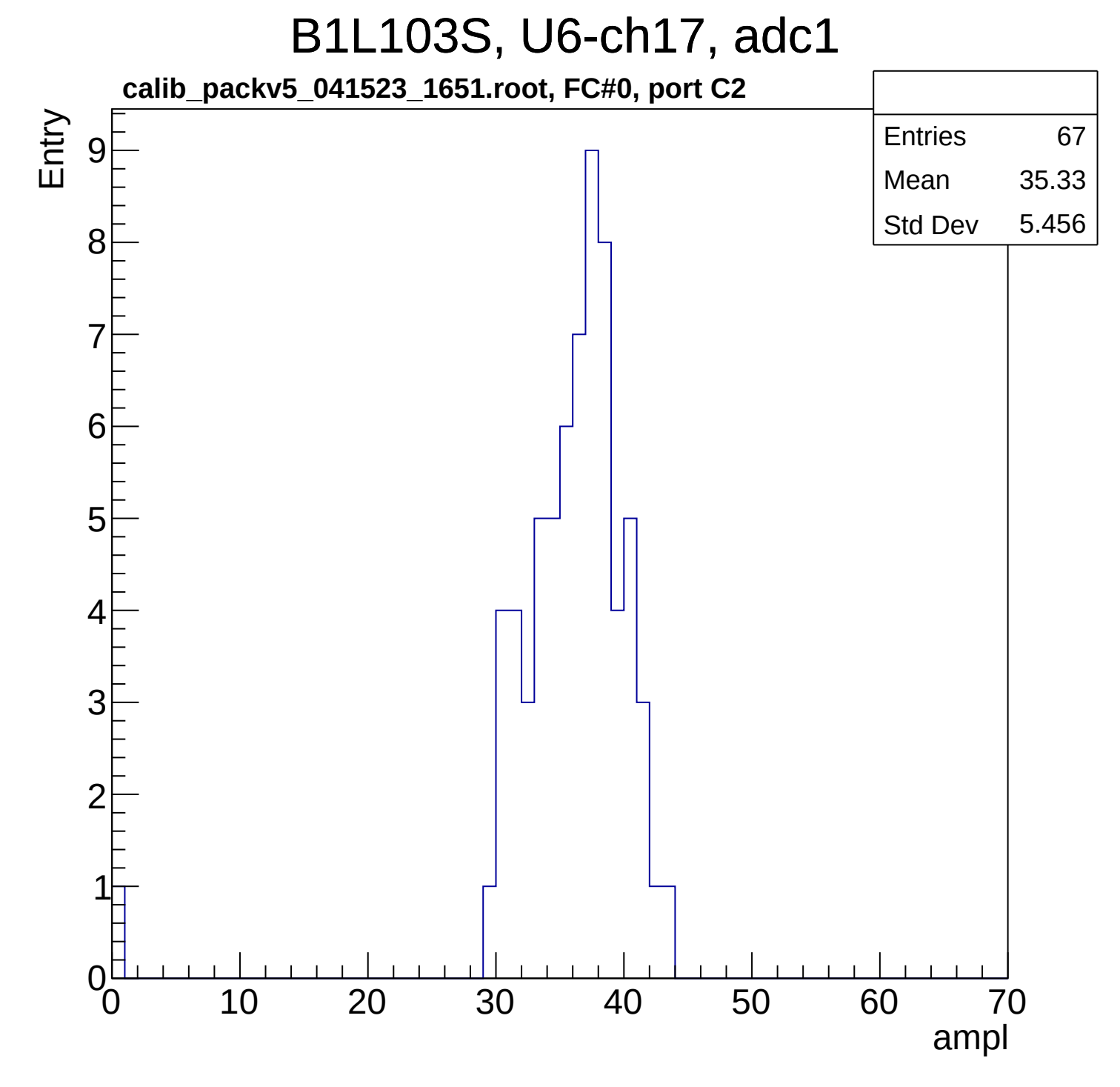
B1L103S, U6-ch17, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 35.33
Std Dev 5.456
Entry
ampl
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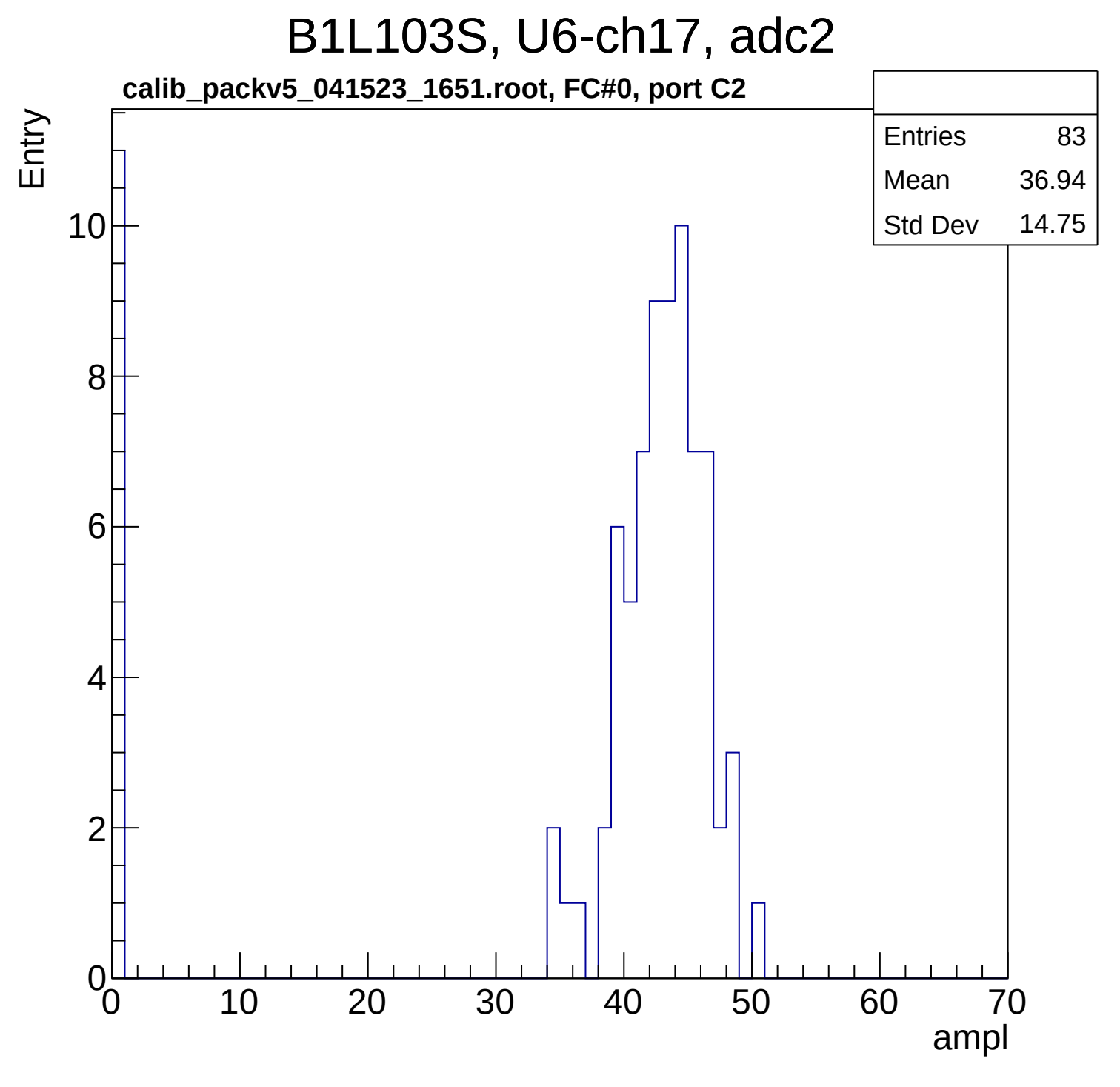
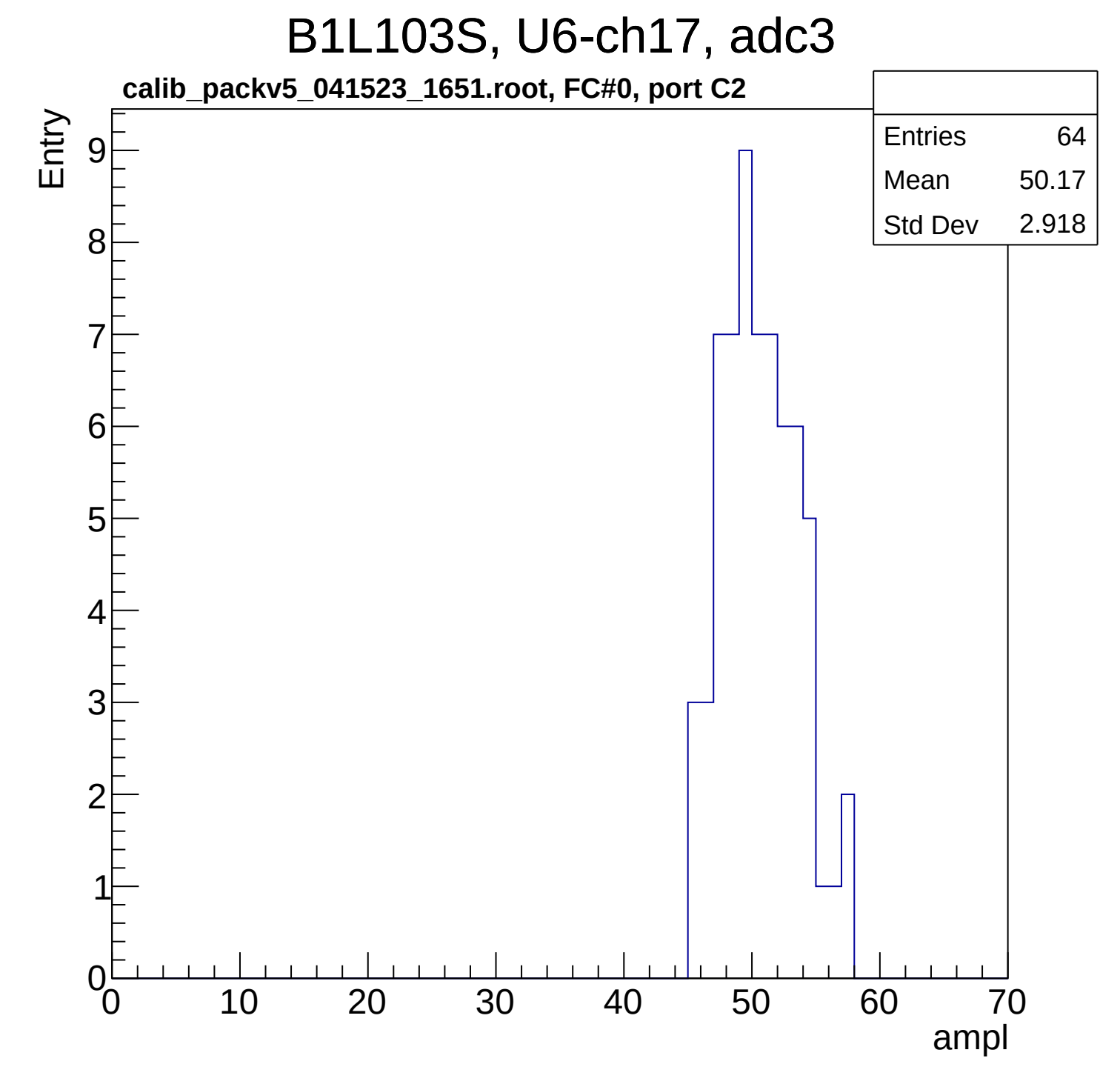
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch17, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 36.94
Std Dev 14.75
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch17, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 50.17
Std Dev 2.918
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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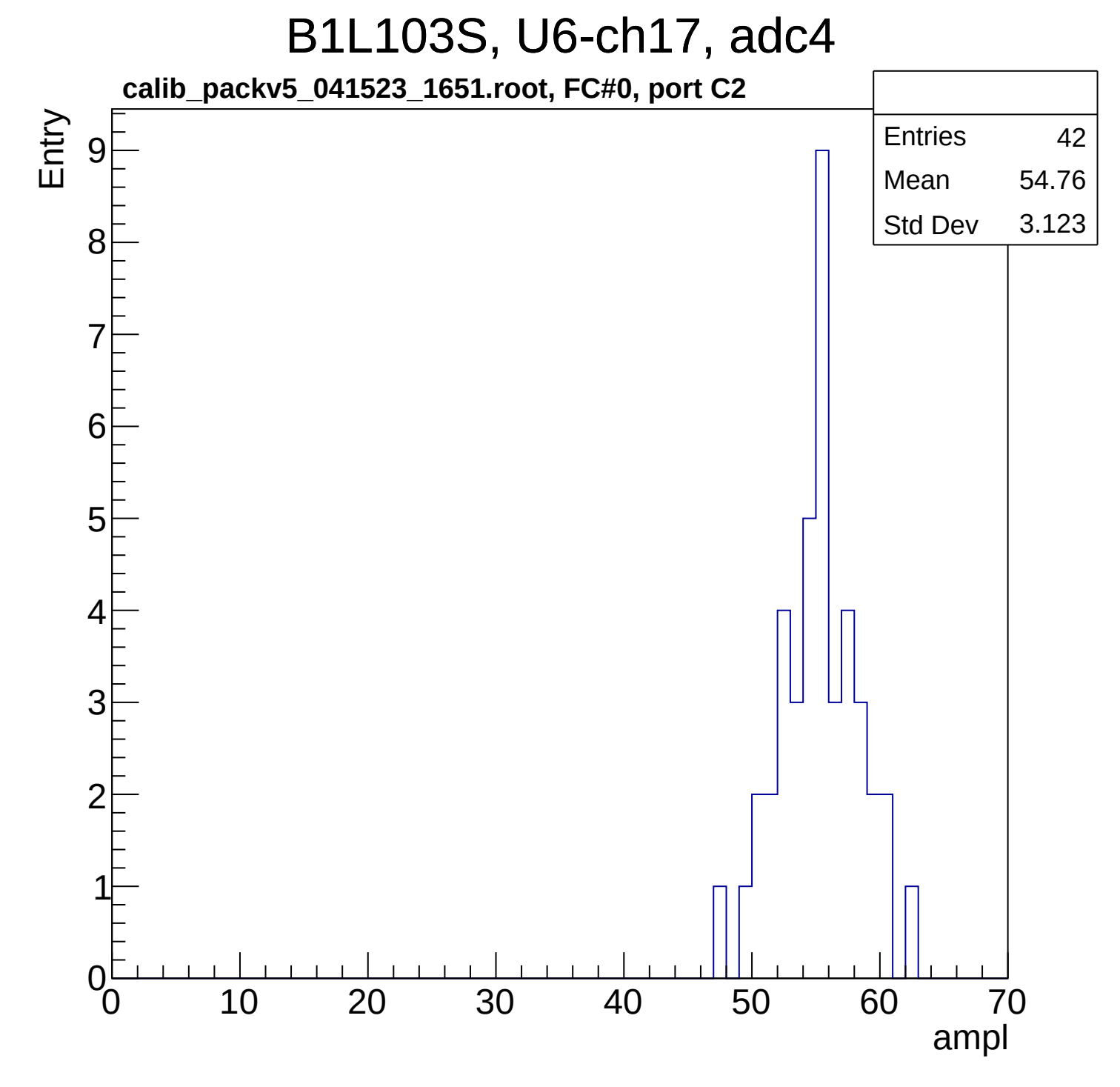
B1L103S, U6-ch17, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 54.76
Std Dev 3.123
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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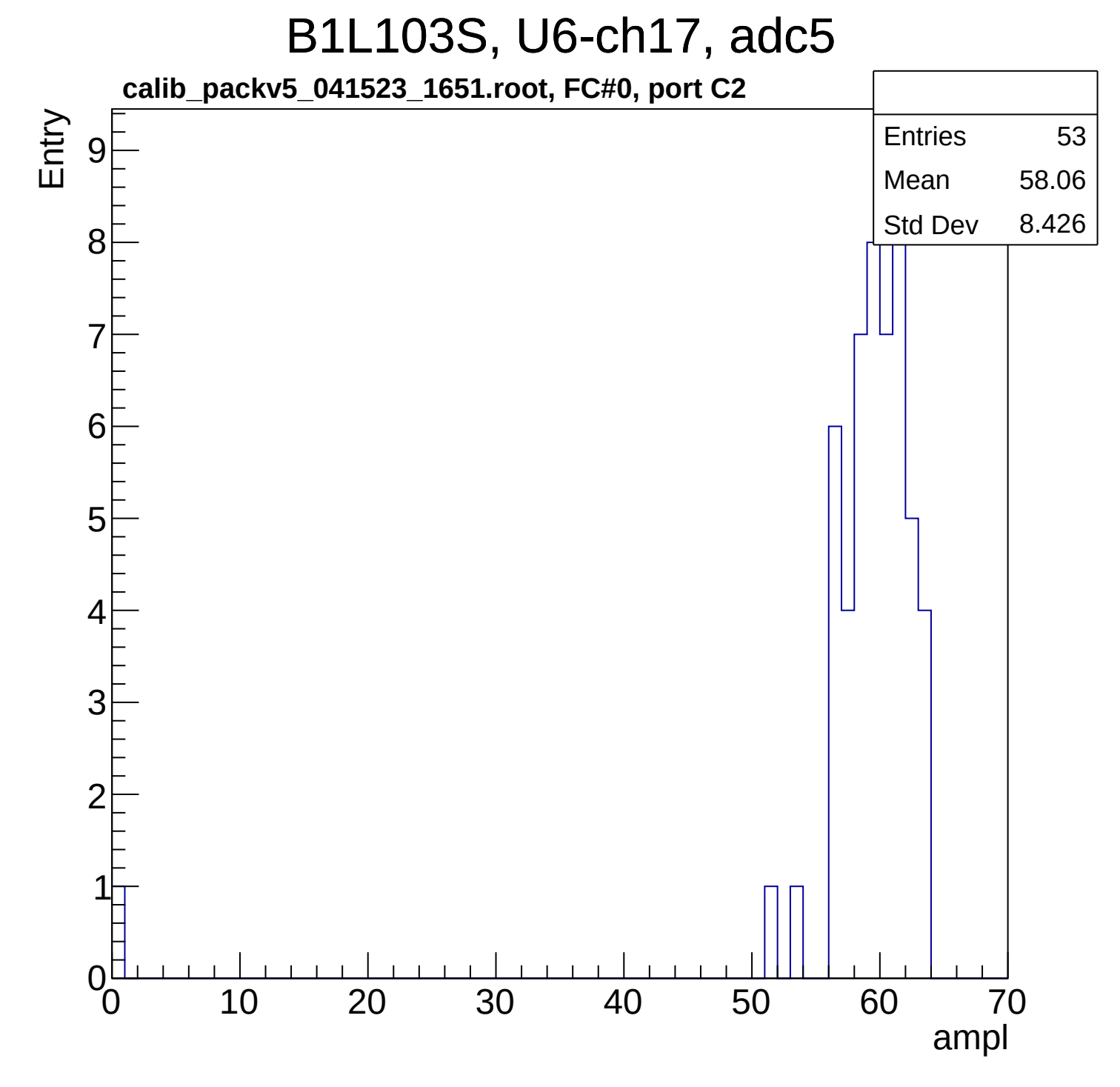
B1L103S, U6-ch17, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 58.06
Std Dev 8.426
Entry
ampl
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3
4
5
6
7
8
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0
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40
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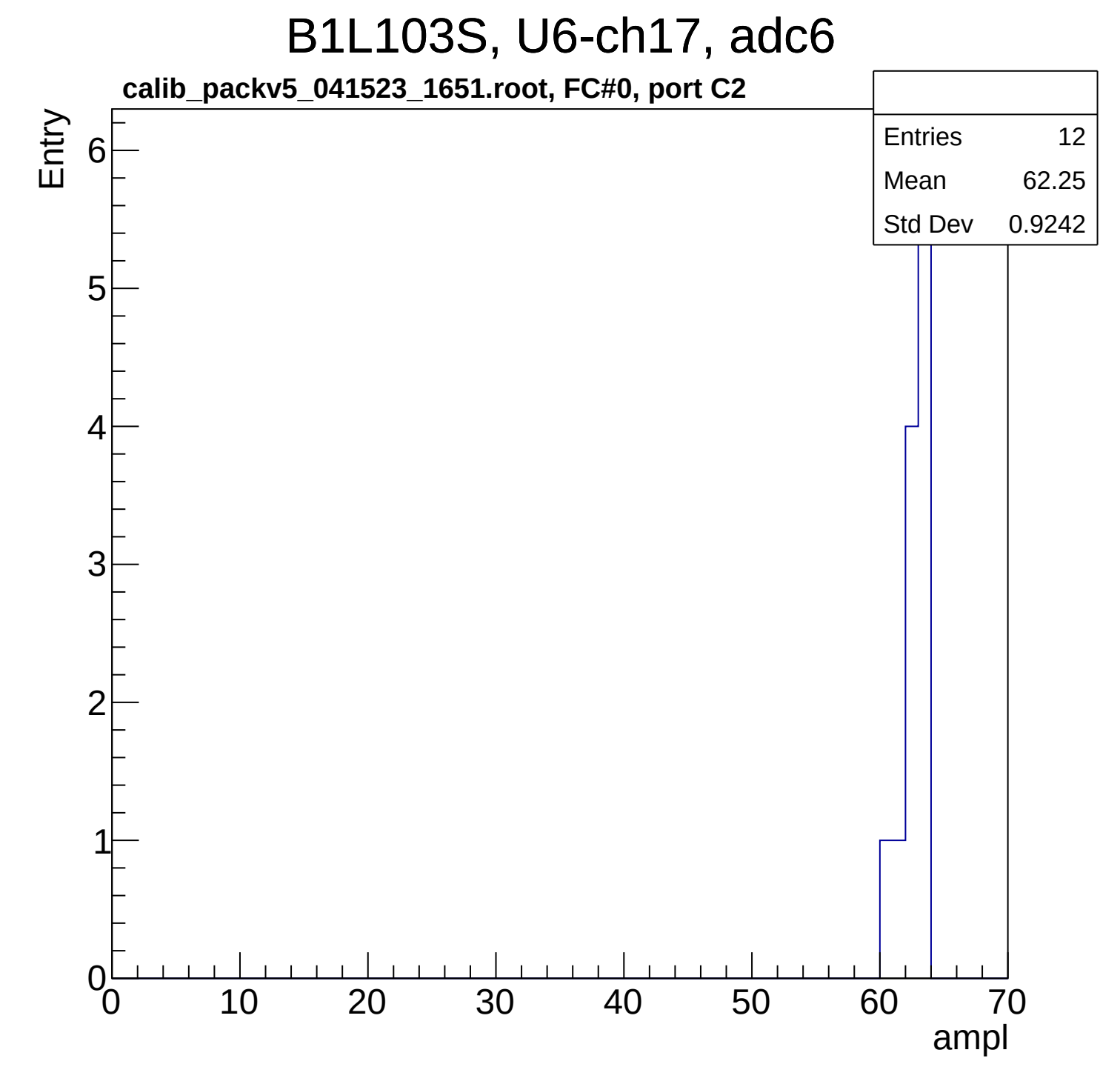
B1L103S, U6-ch17, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 62.25
Std Dev 0.9242
Entry
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2
3
4
5
6
0
10
20
30
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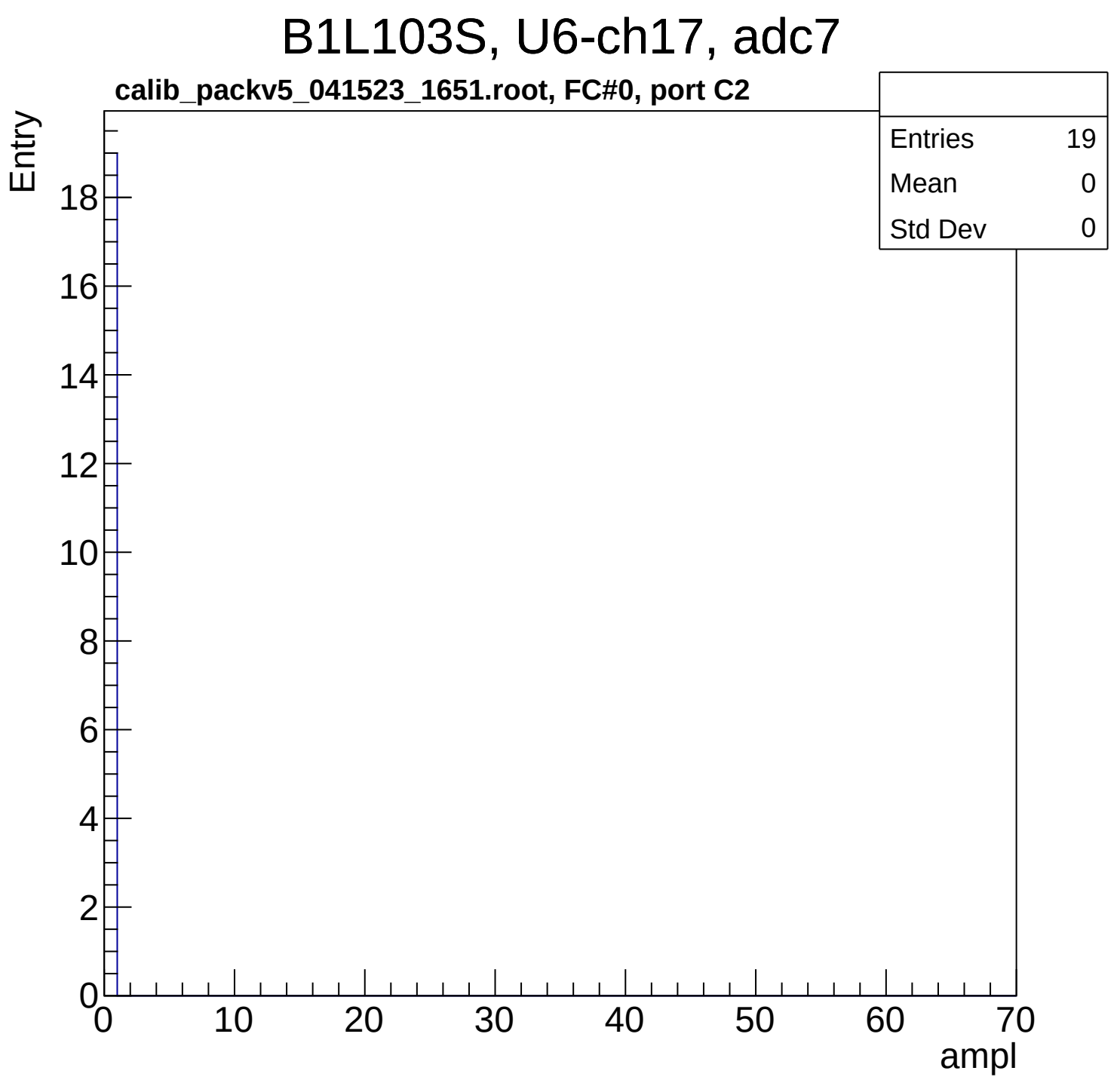
50
60
70
ampl


B1L103S, U6-ch17, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
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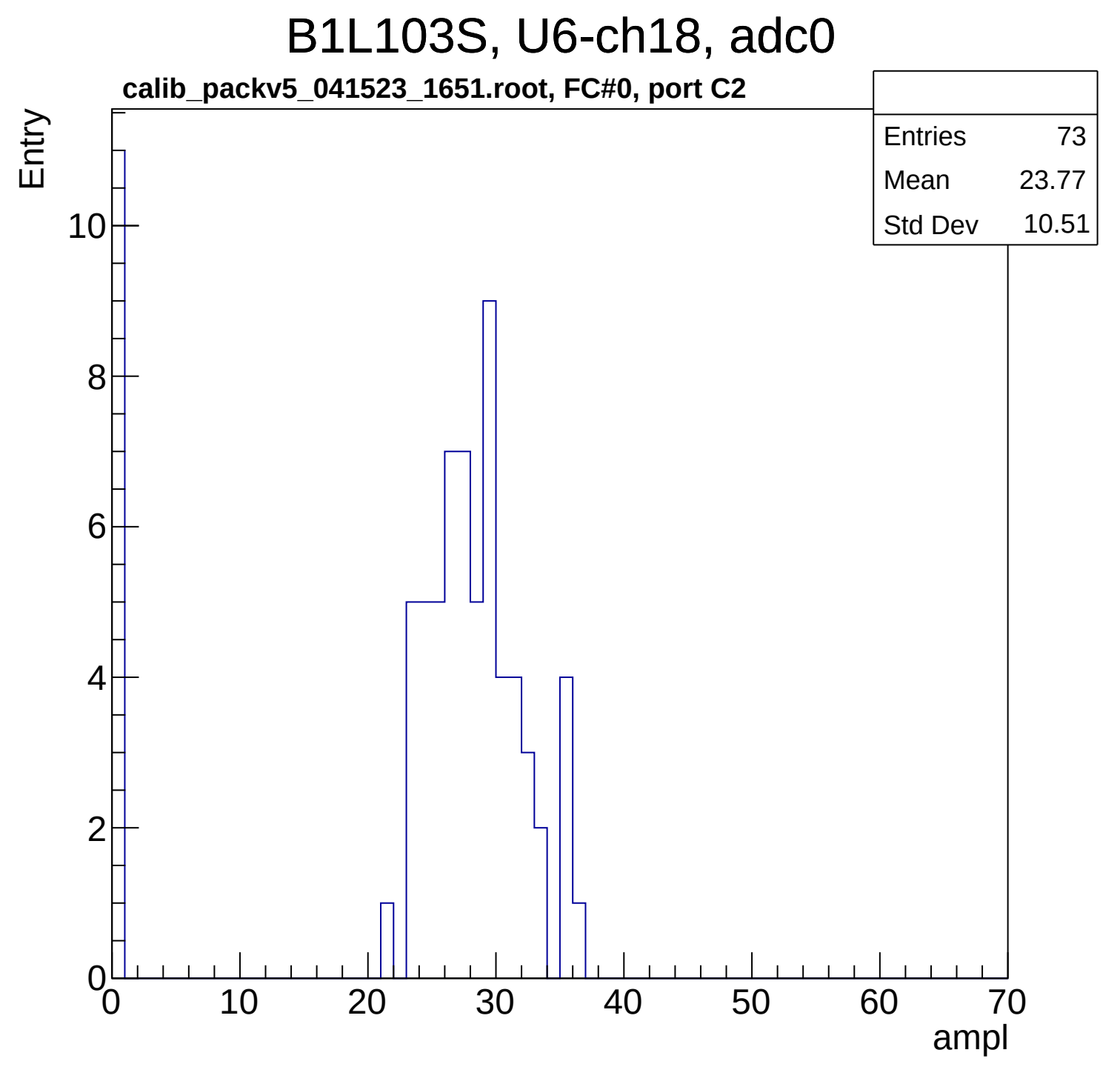
50
60
70
ampl


B1L103S, U6-ch18, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 23.77
Std Dev 10.51
Entry
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4
6
8
10
0
10
20
30
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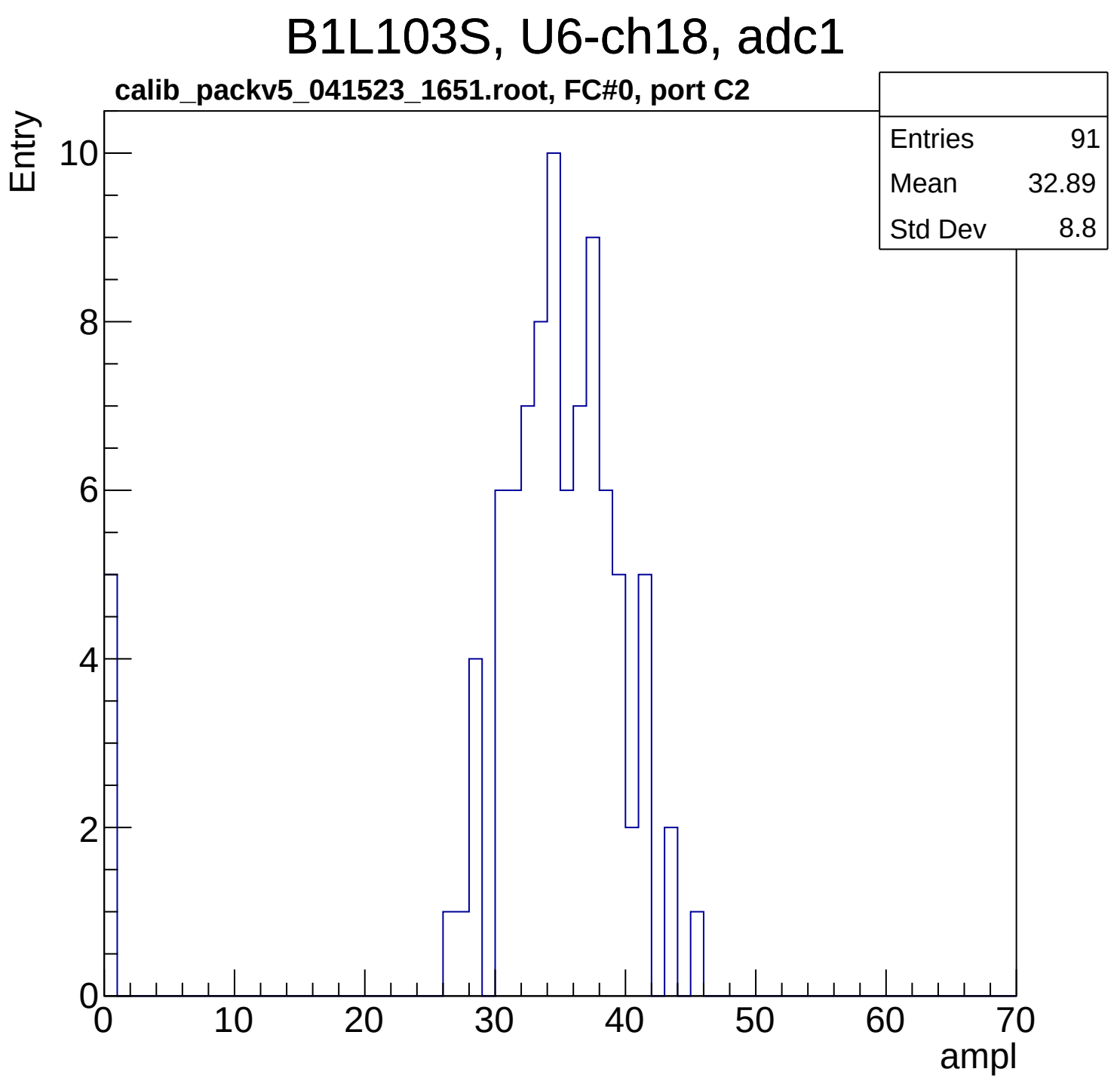
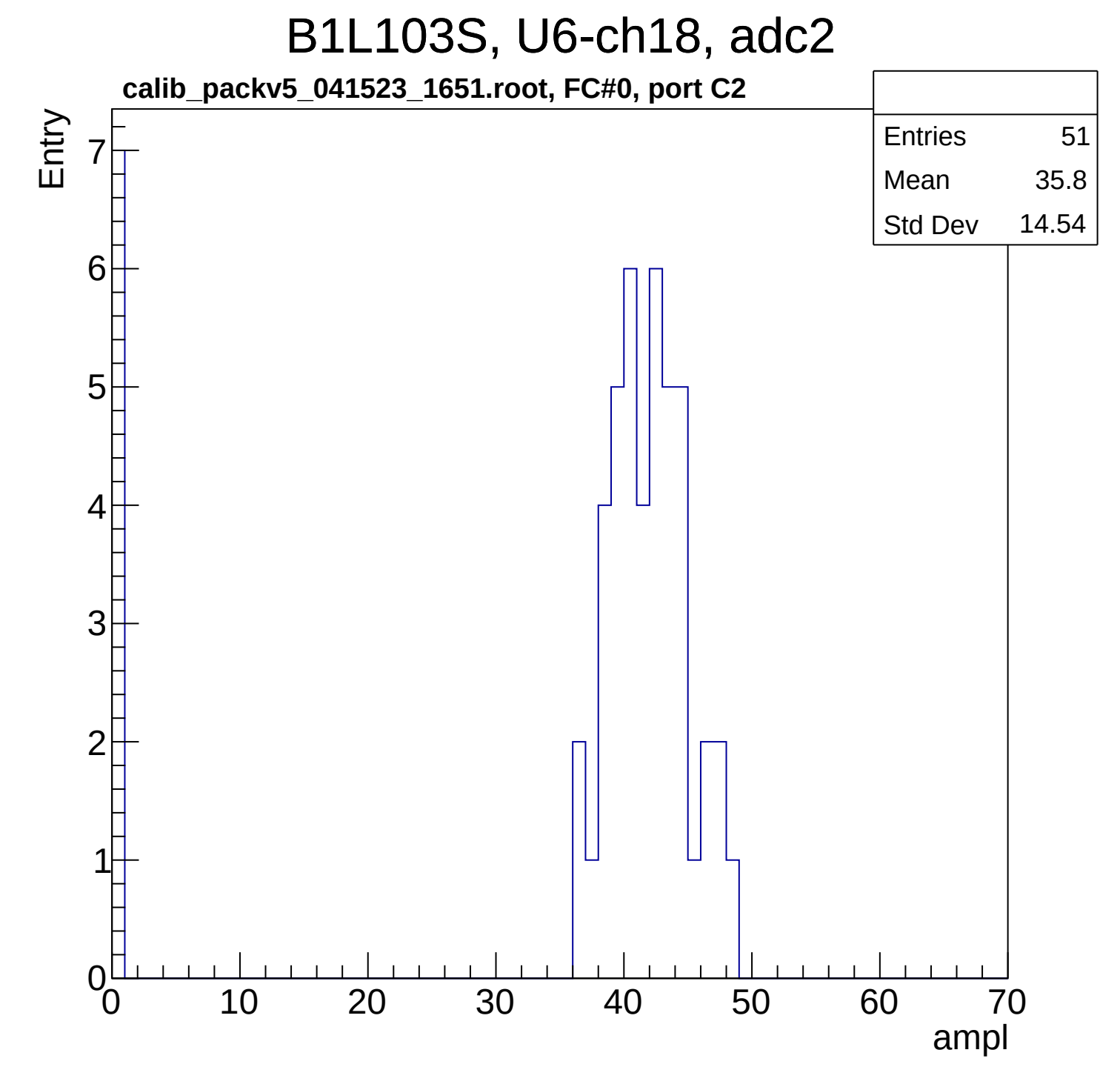
50
60
70
ampl


B1L103S, U6-ch18, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 32.89
Std Dev 8.8
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U6-ch18, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 35.8
Std Dev 14.54
Entry
ampl
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4
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6
7
0
10
20
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40
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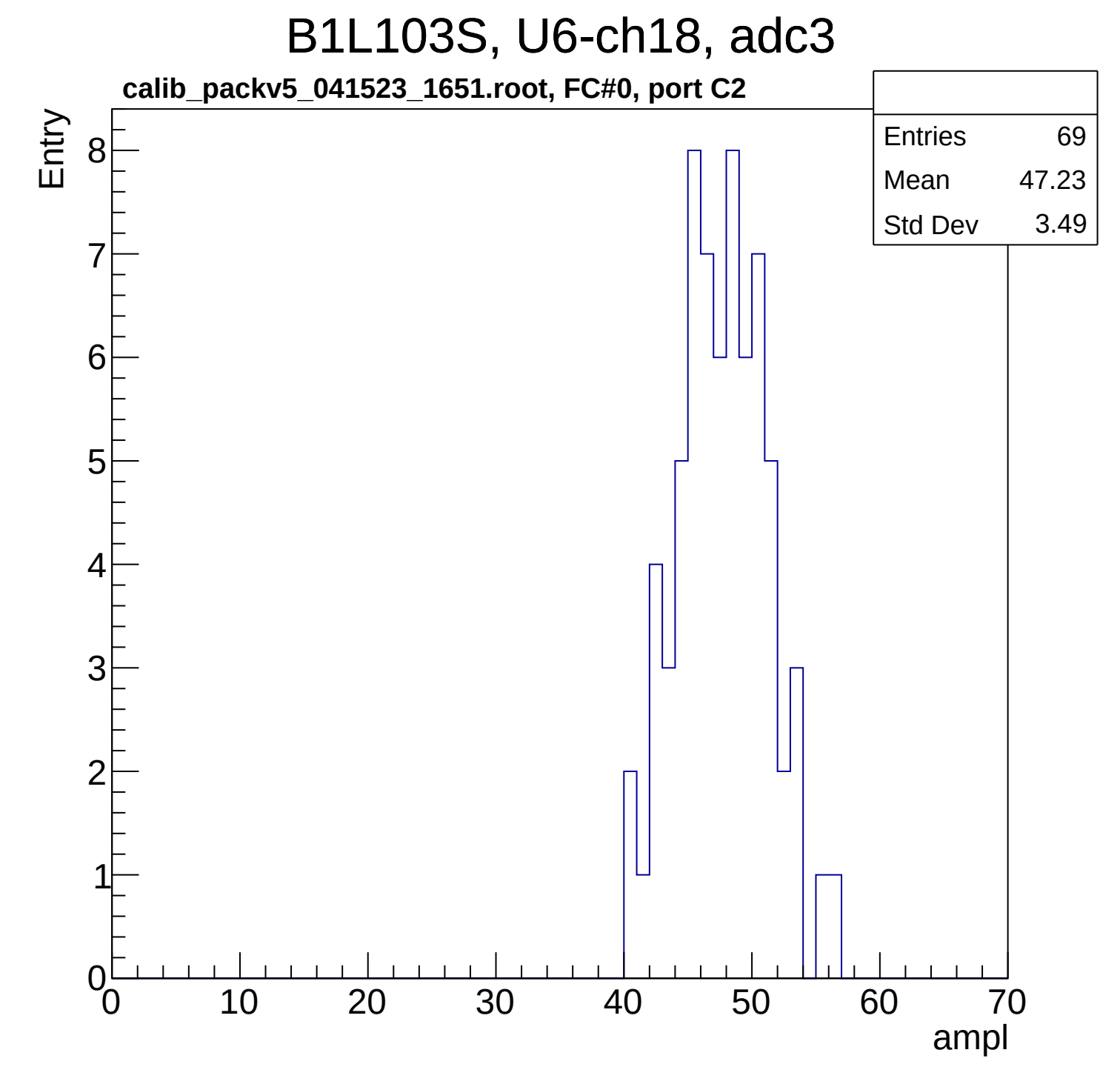
60
70


B1L103S, U6-ch18, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 47.23
Std Dev 3.49
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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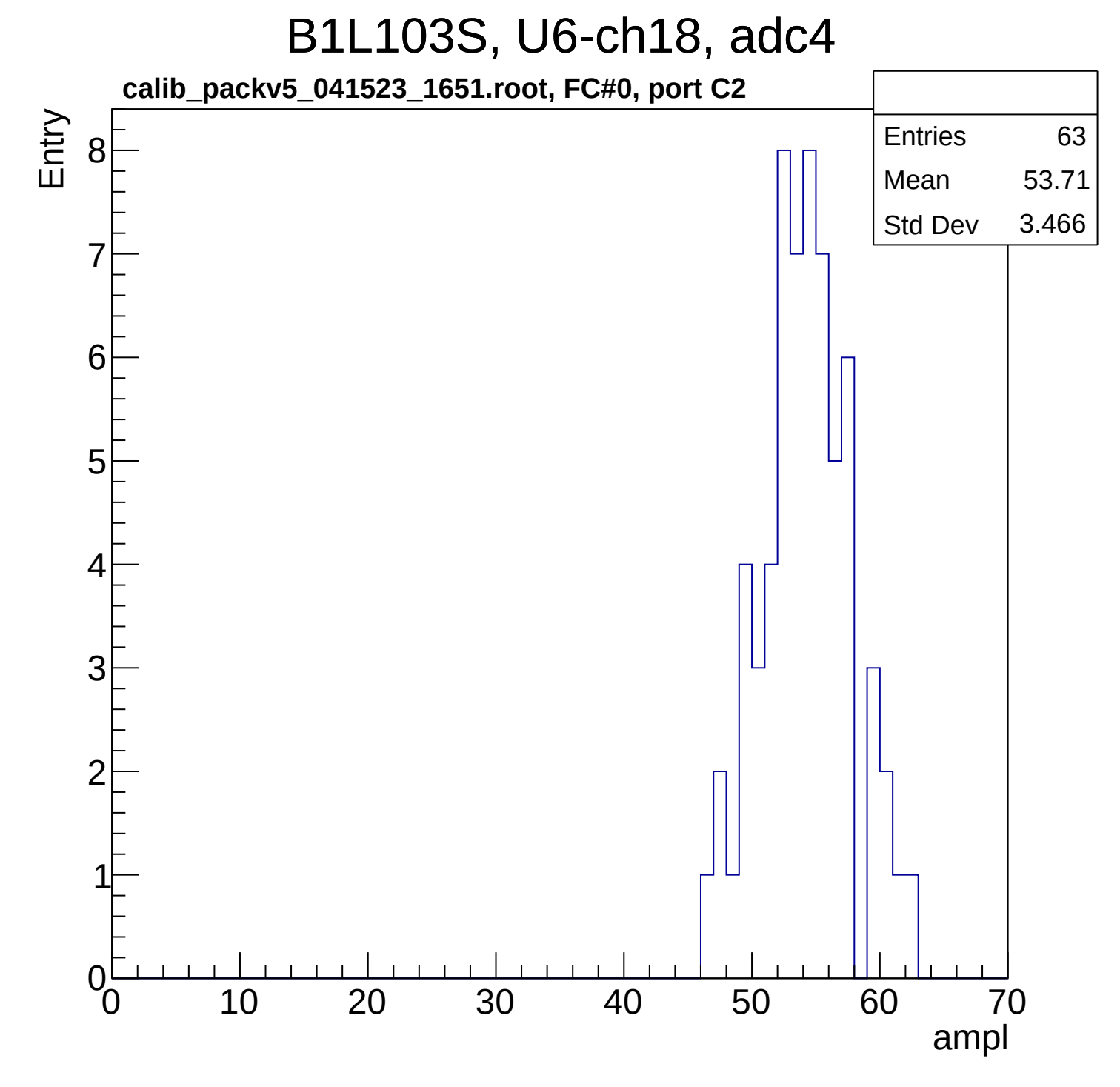
B1L103S, U6-ch18, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 53.71
Std Dev 3.466
Entry
ampl
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2
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5
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0
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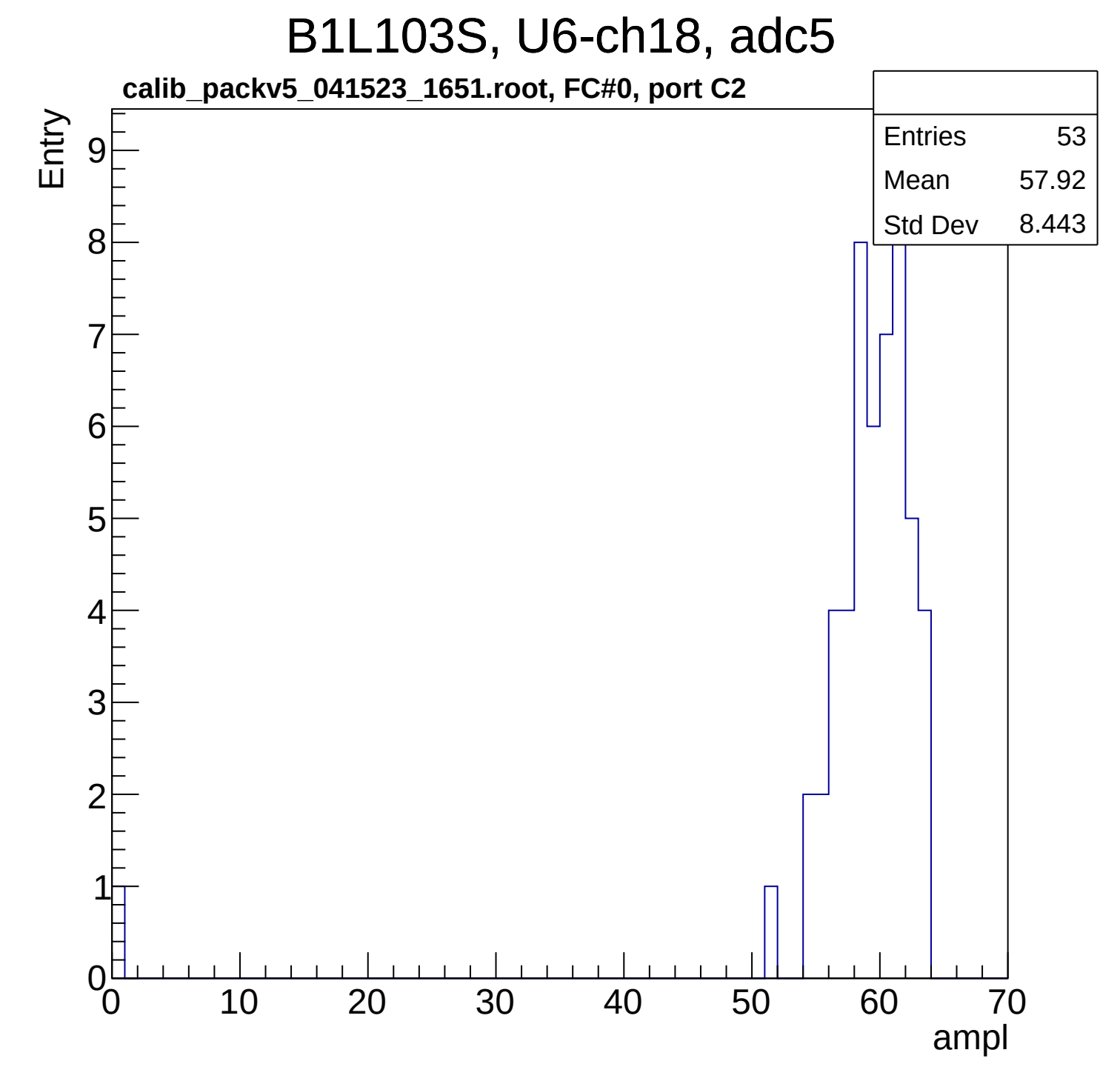
B1L103S, U6-ch18, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 57.92
Std Dev 8.443
Entry
ampl
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2
3
4
5
6
7
8
9
0
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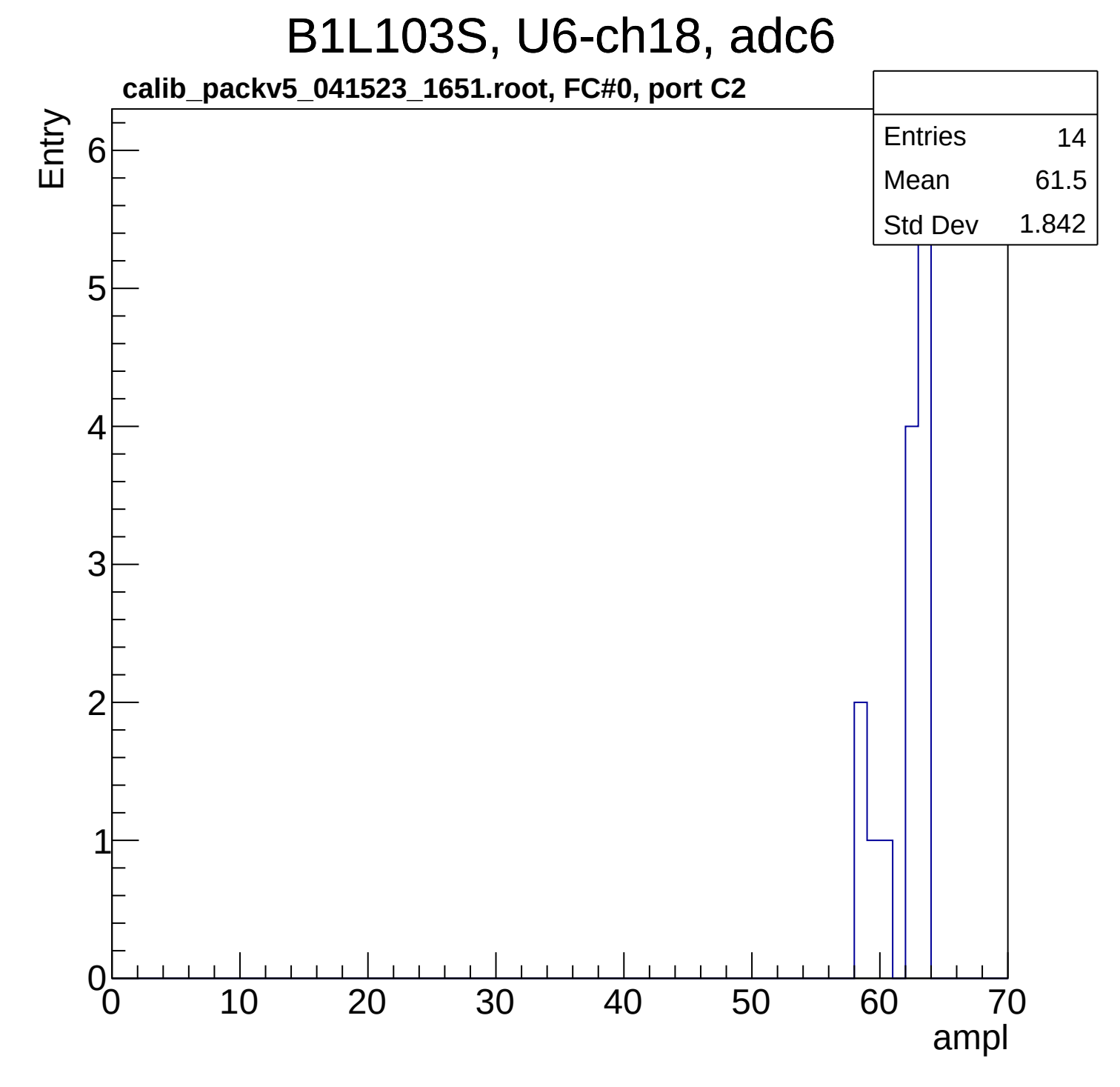
B1L103S, U6-ch18, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 61.5
Std Dev 1.842
Entry
0
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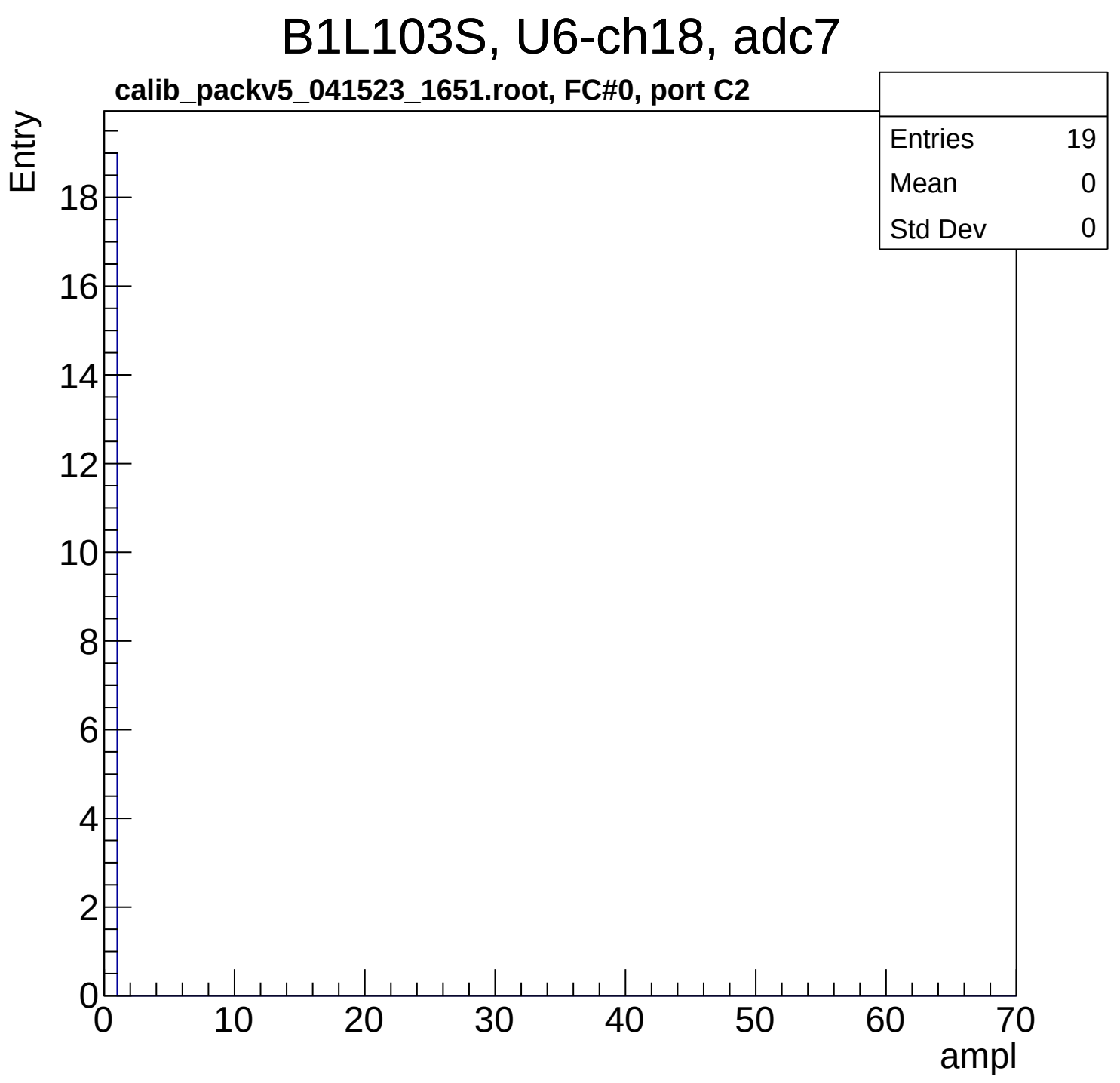
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch18, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
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50
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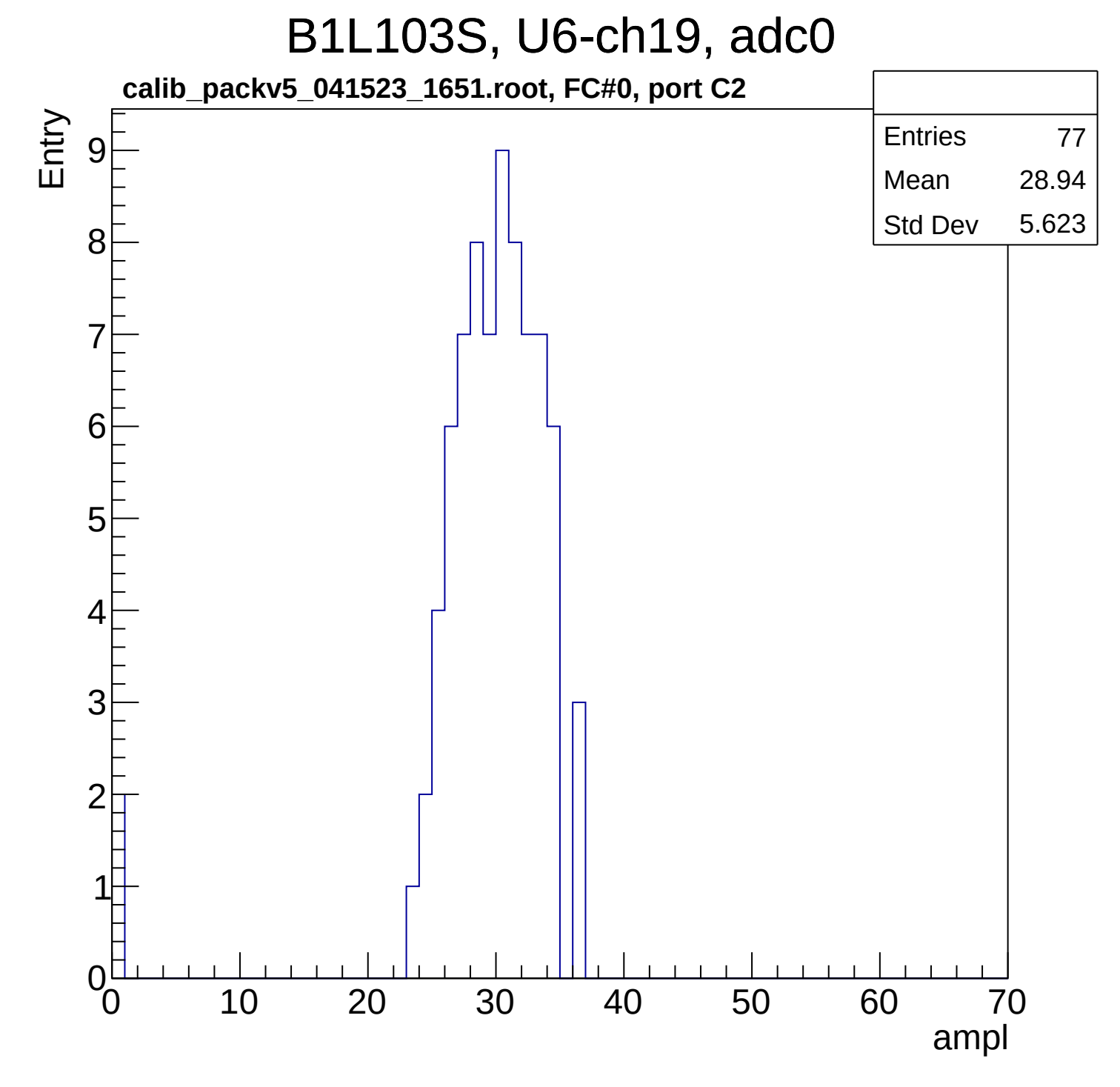
70
ampl


B1L103S, U6-ch19, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 28.94
Std Dev 5.623
Entry
ampl
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2
3
4
5
6
7
8
9
0
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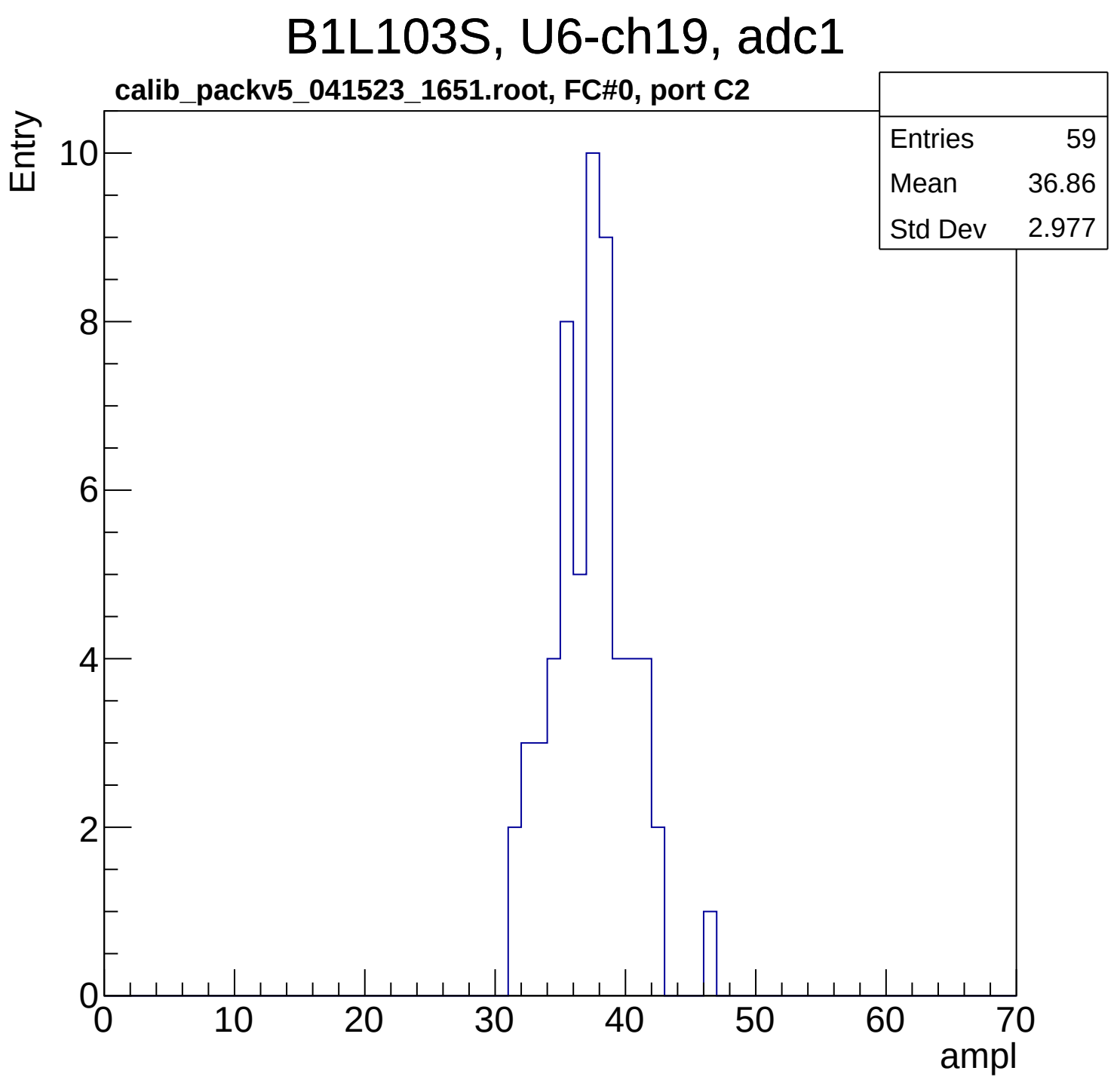
B1L103S, U6-ch19, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 36.86
Std Dev 2.977
Entry
ampl
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6
8
10
0
10
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40
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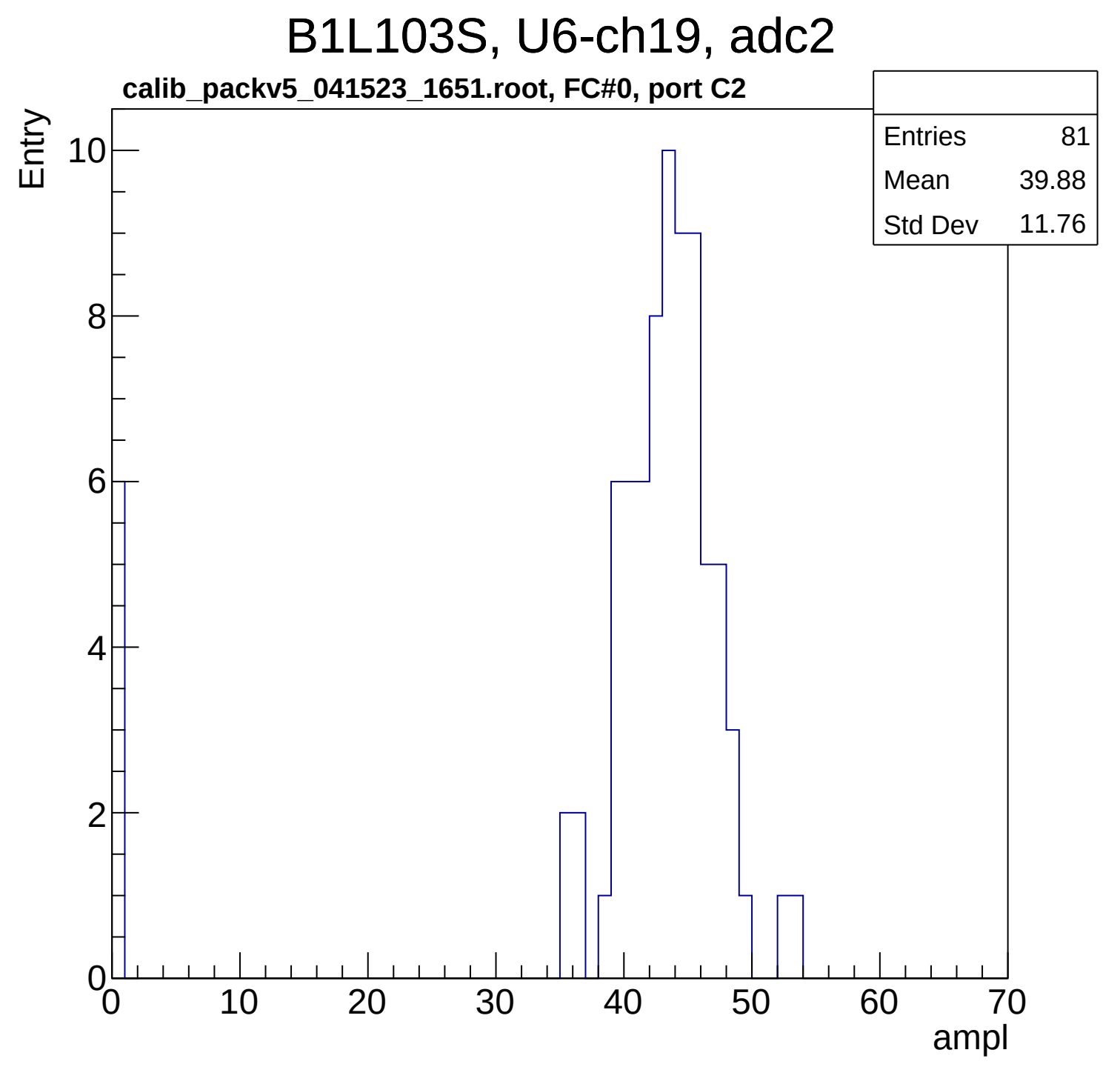
70


B1L103S, U6-ch19, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 39.88
Std Dev 11.76
Entry
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6
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10
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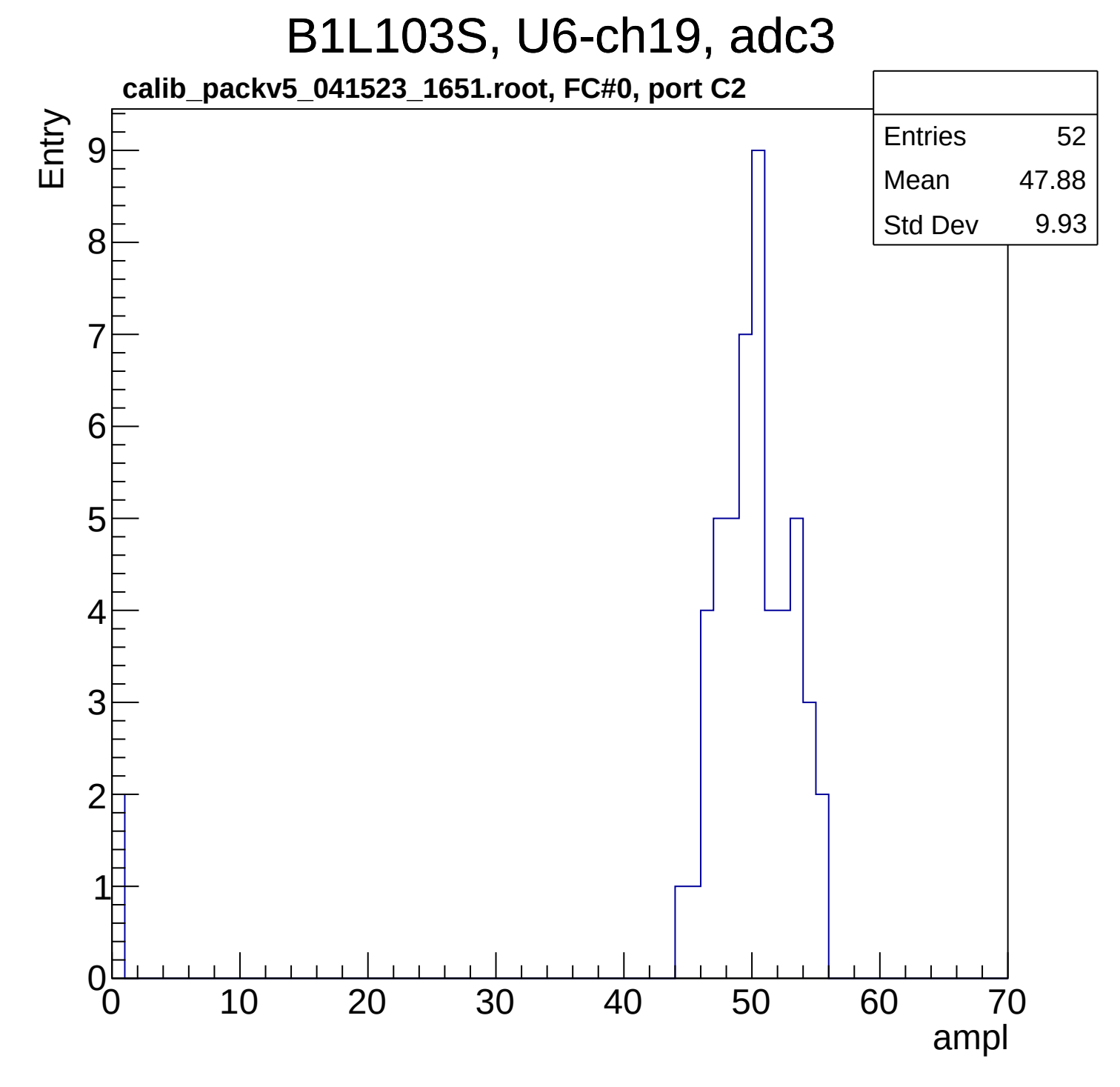
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch19, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 47.88
Std Dev 9.93
Entry
ampl
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2
3
4
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6
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8
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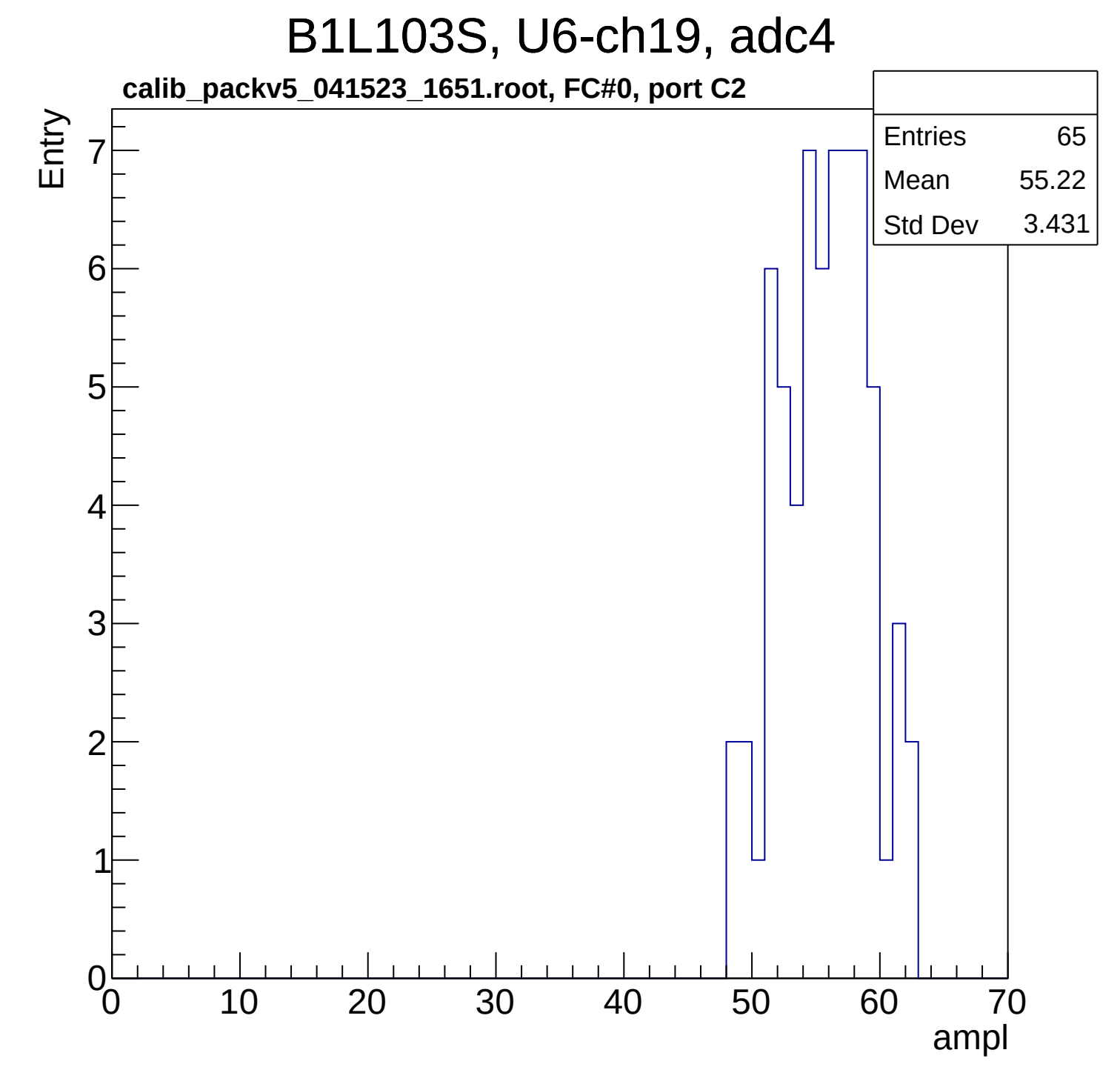
B1L103S, U6-ch19, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 55.22
Std Dev 3.431
Entry
ampl
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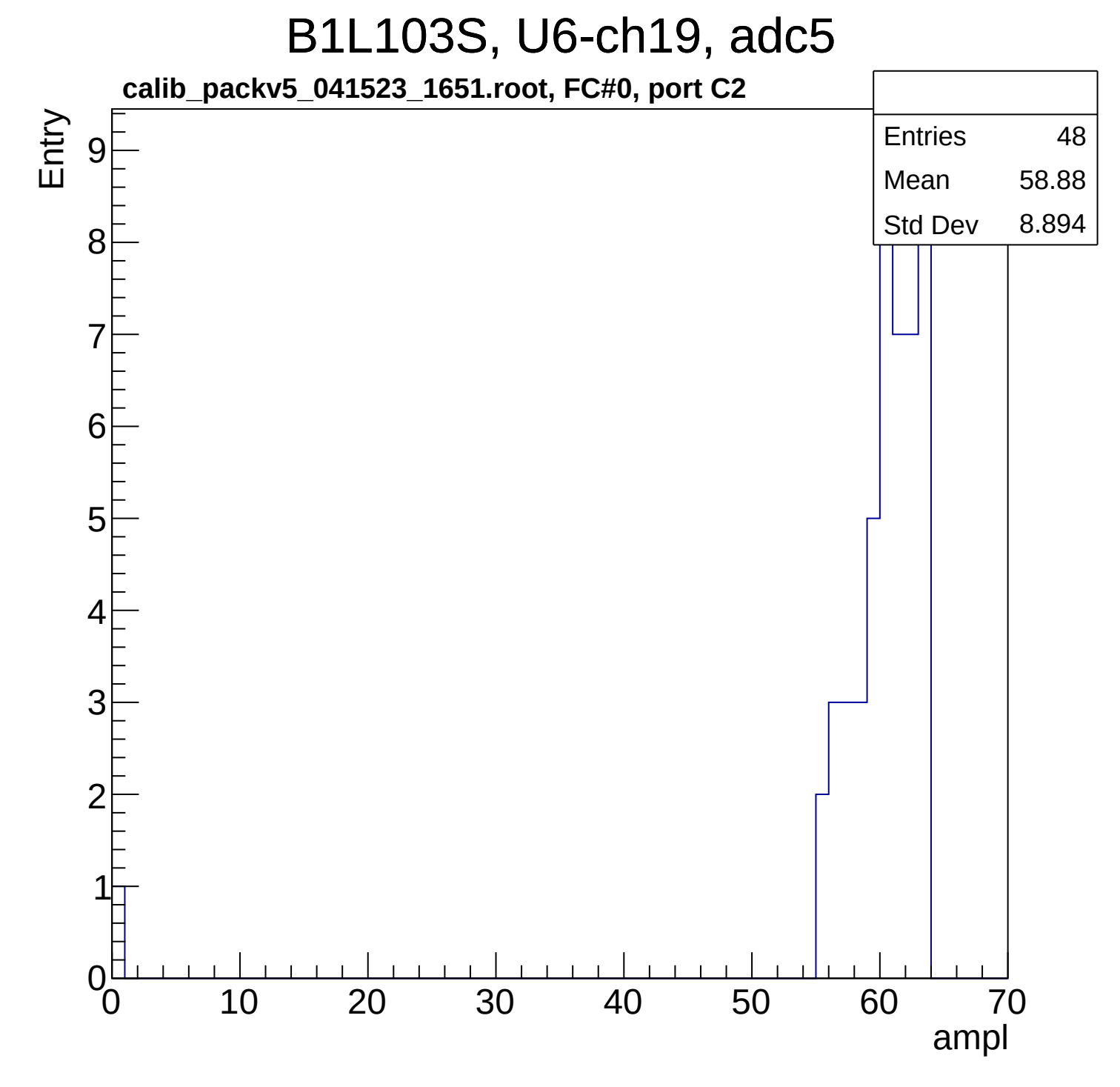
B1L103S, U6-ch19, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 58.88
Std Dev 8.894
Entry
ampl
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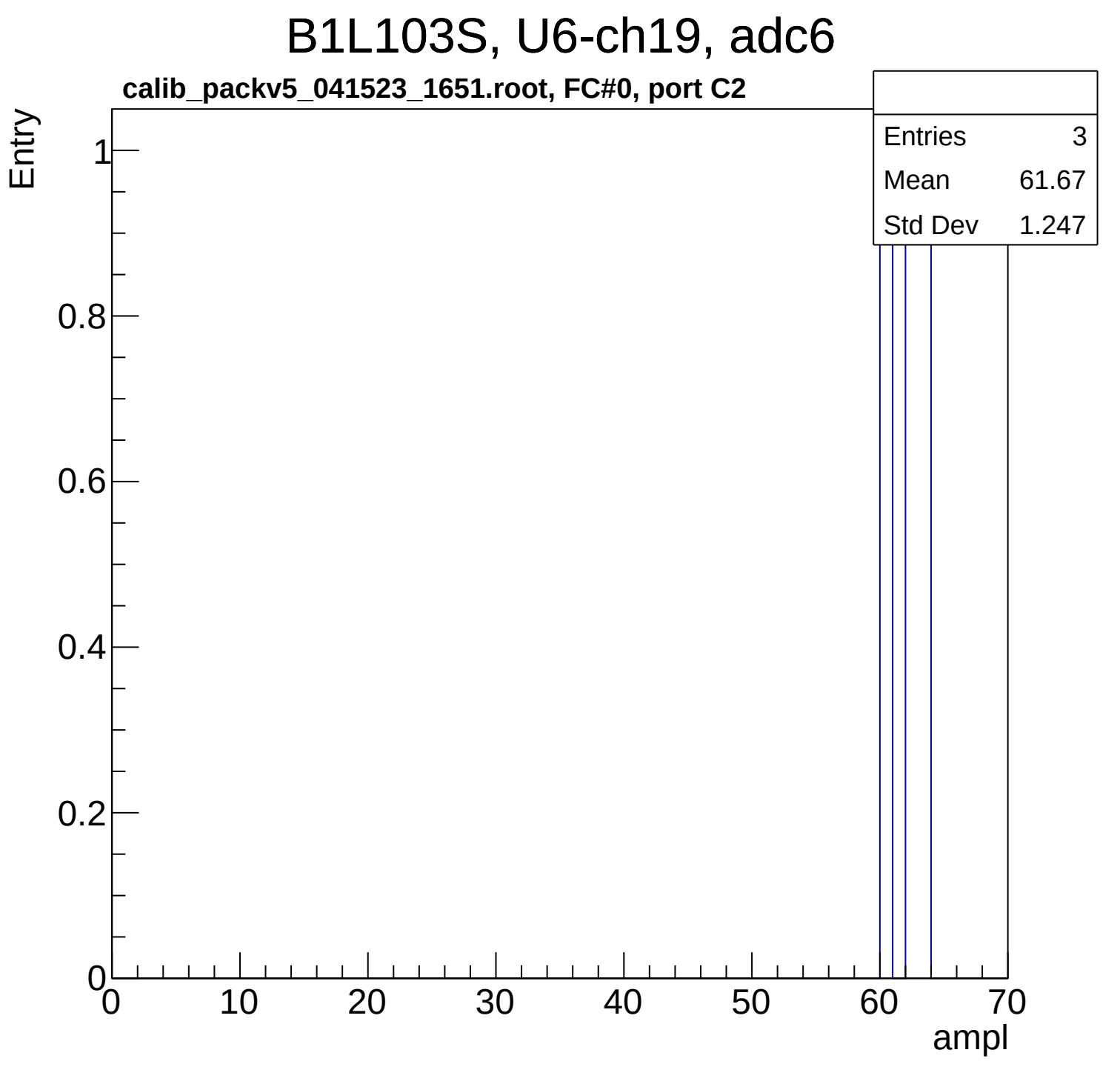
B1L103S, U6-ch19, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 61.67
Std Dev 1.247
Entry
ampl
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0.2
0.4
0.6
0.8
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0
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40
50
60
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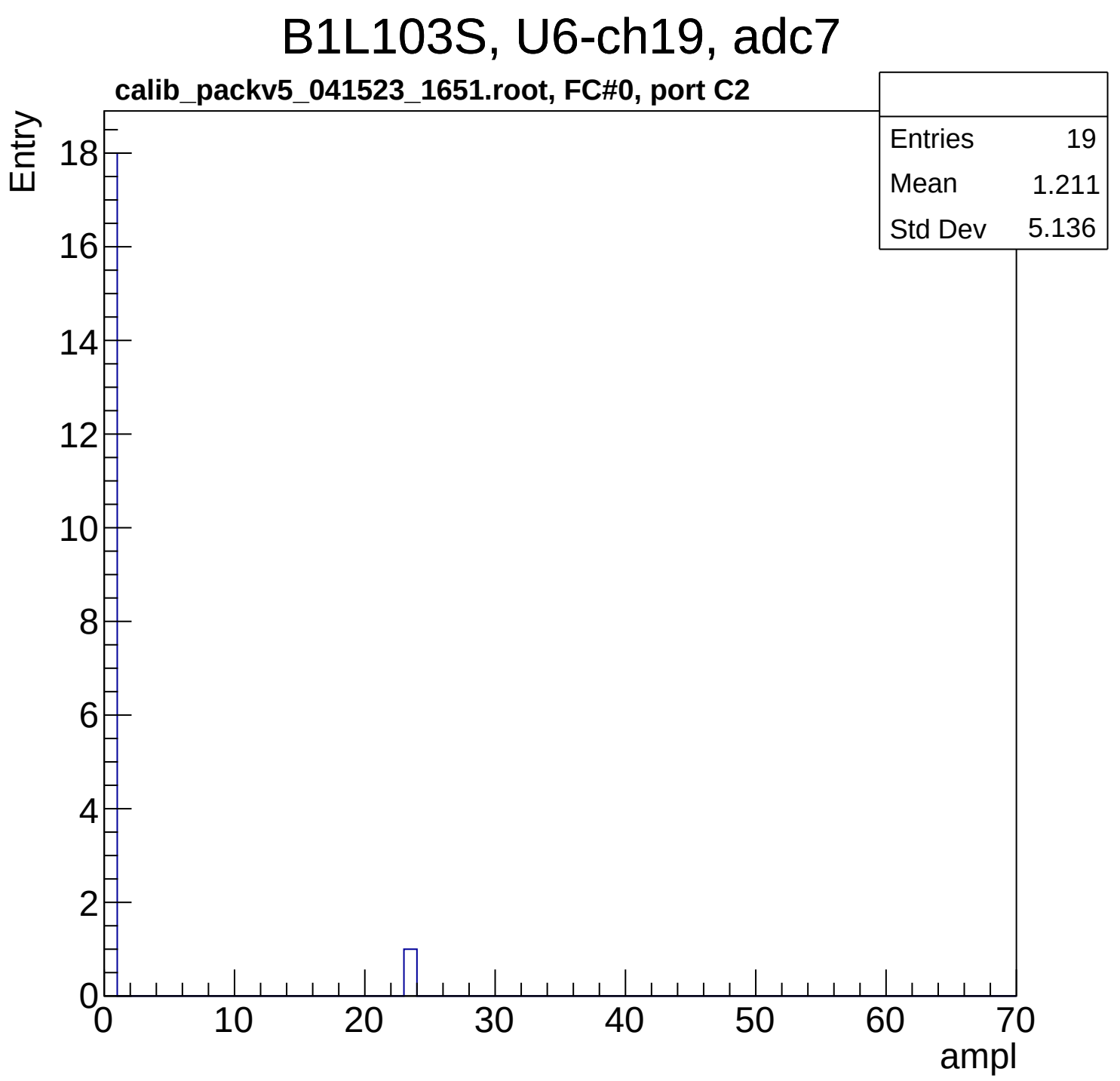
B1L103S, U6-ch19, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.211
Std Dev 5.136
Entry
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6
8
10
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14
16
18
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20
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50
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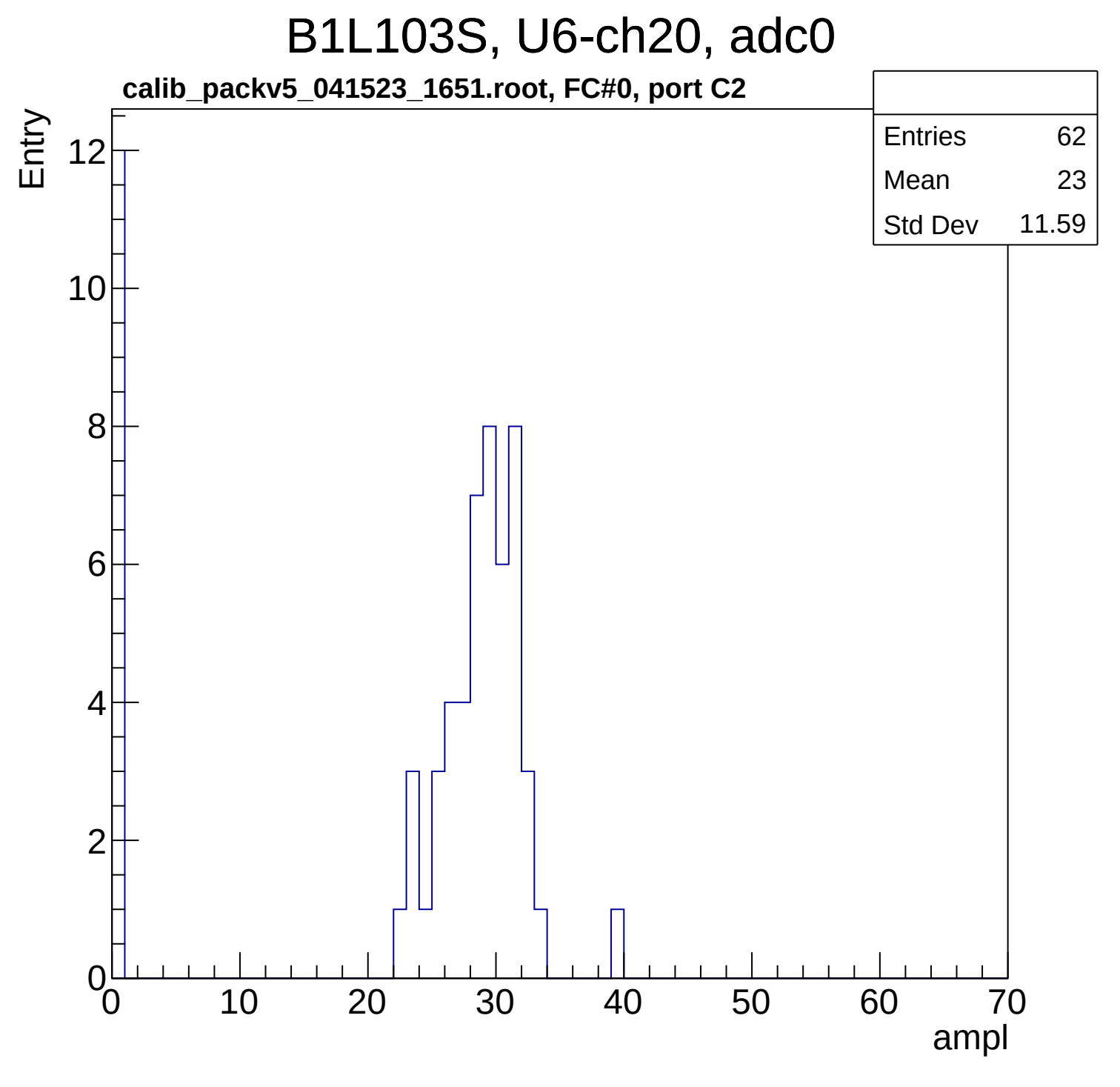
70
ampl


B1L103S, U6-ch20, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 23
Std Dev 11.59
Entry
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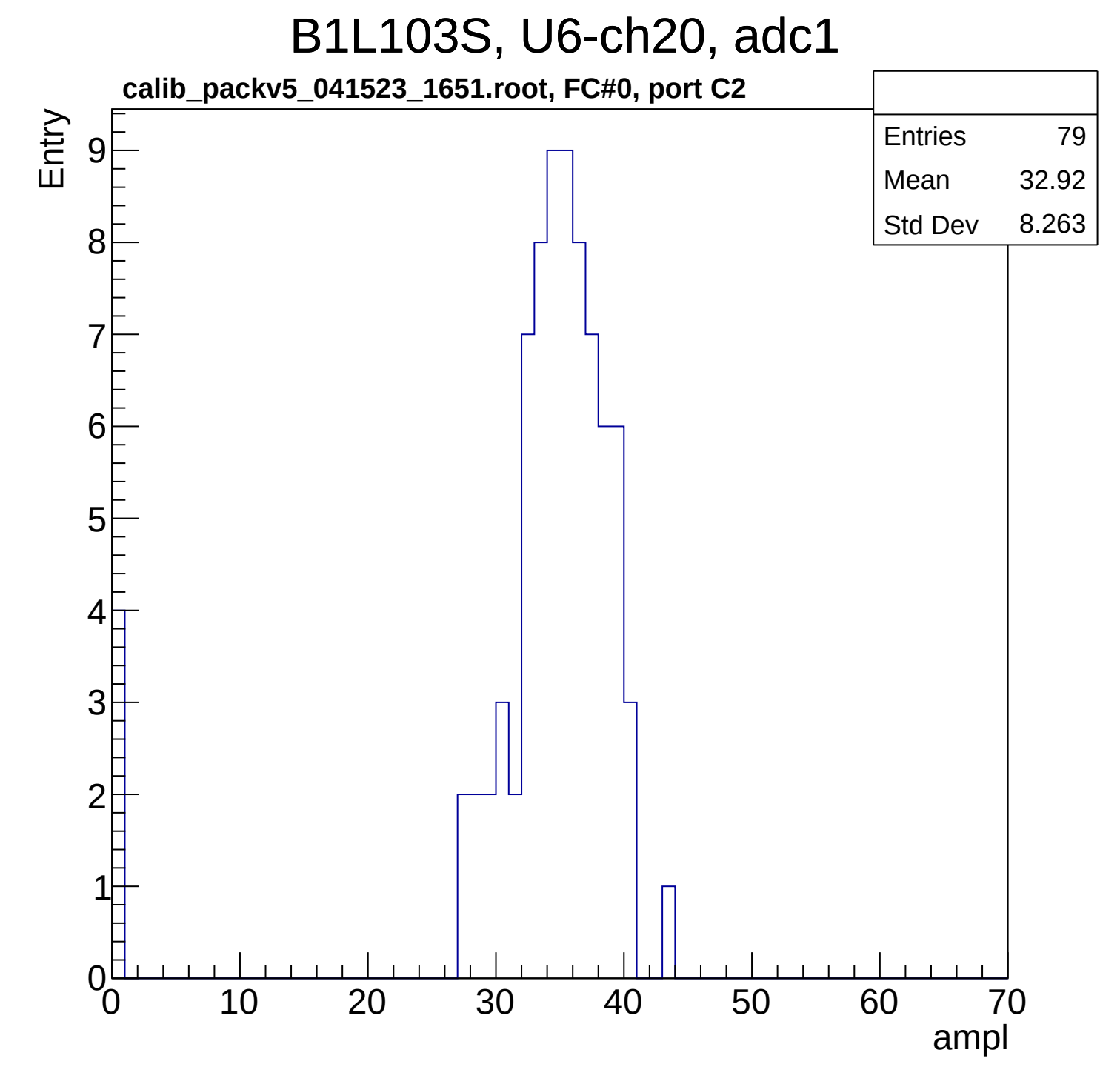
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch20, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 32.92
Std Dev 8.263
Entry
ampl
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4
5
6
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8
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0
10
20
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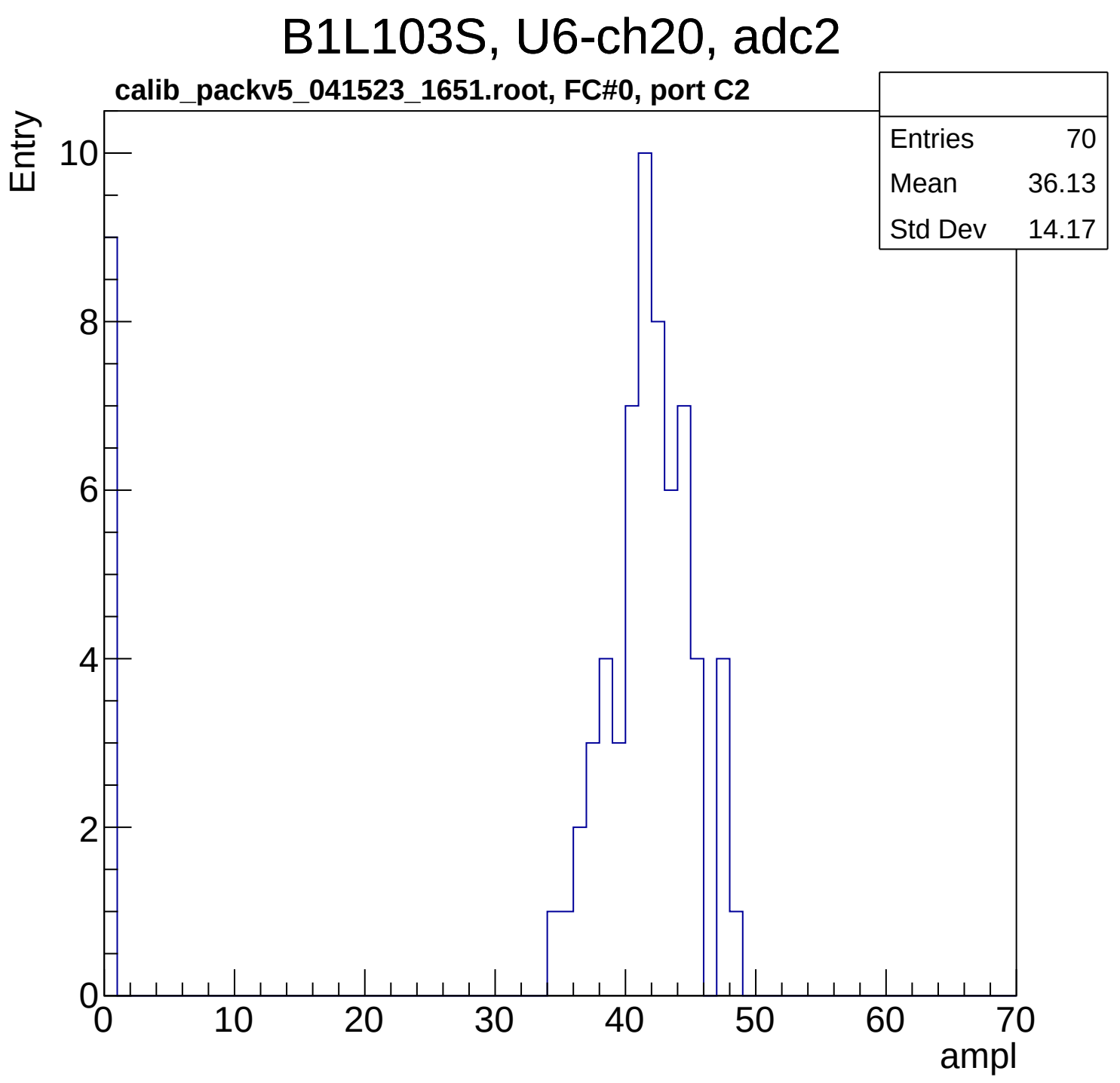
B1L103S, U6-ch20, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 36.13
Std Dev 14.17
Entry
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6
8
10
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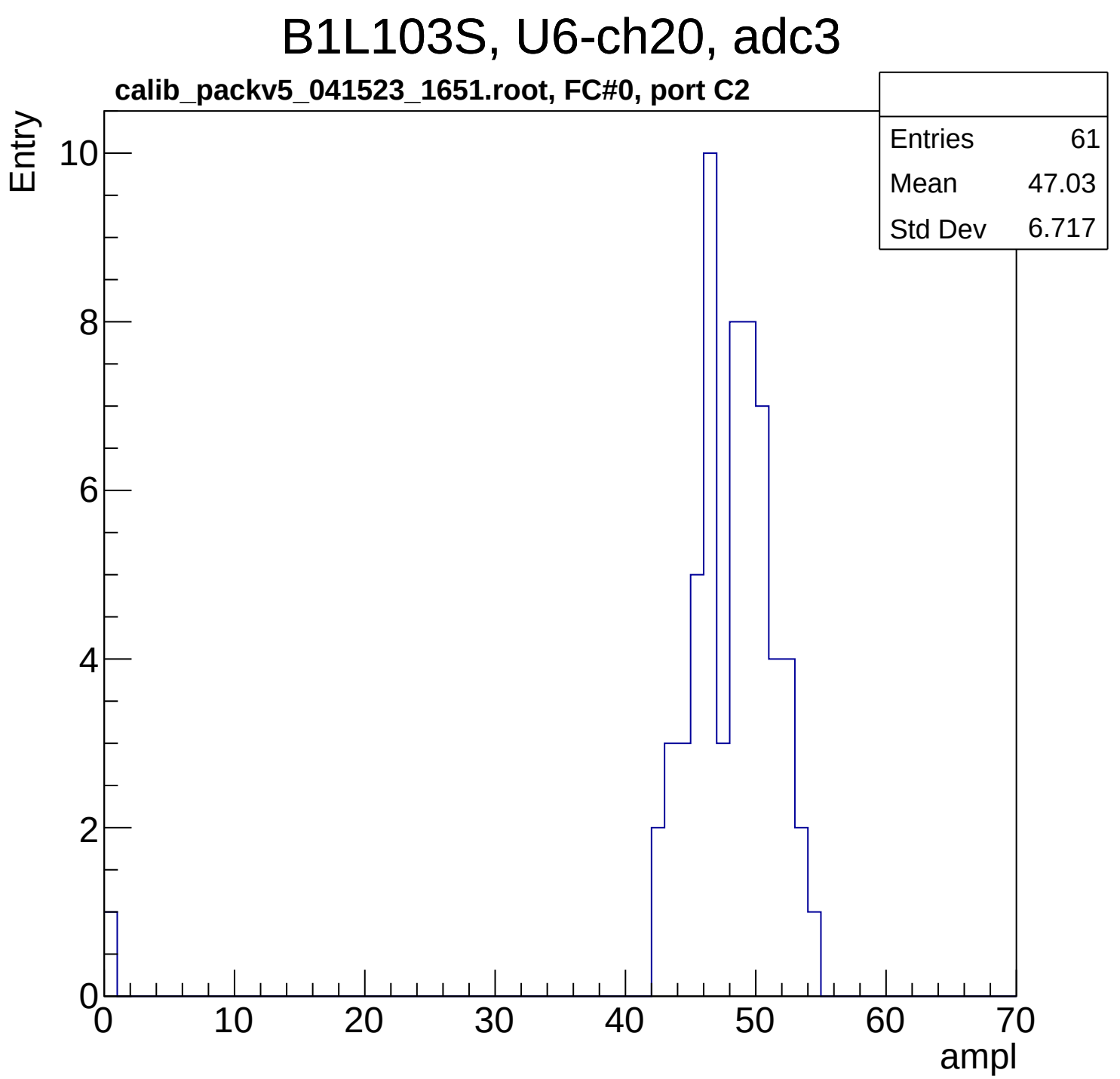
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch20, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 47.03
Std Dev 6.717
Entry
0
2
4
6
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10
0
10
20
30
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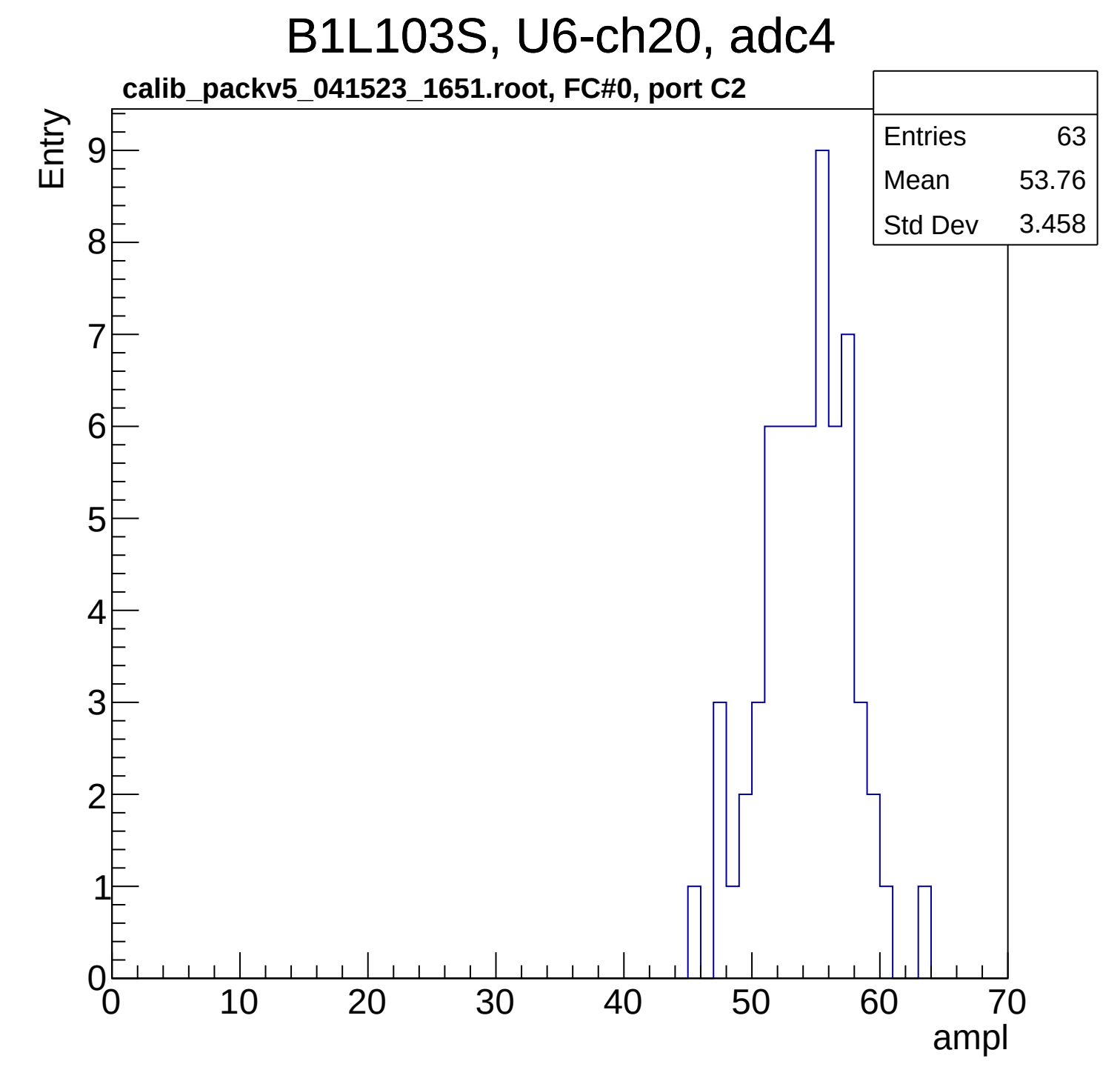
50
60
70
ampl


B1L103S, U6-ch20, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 53.76
Std Dev 3.458
Entry
ampl
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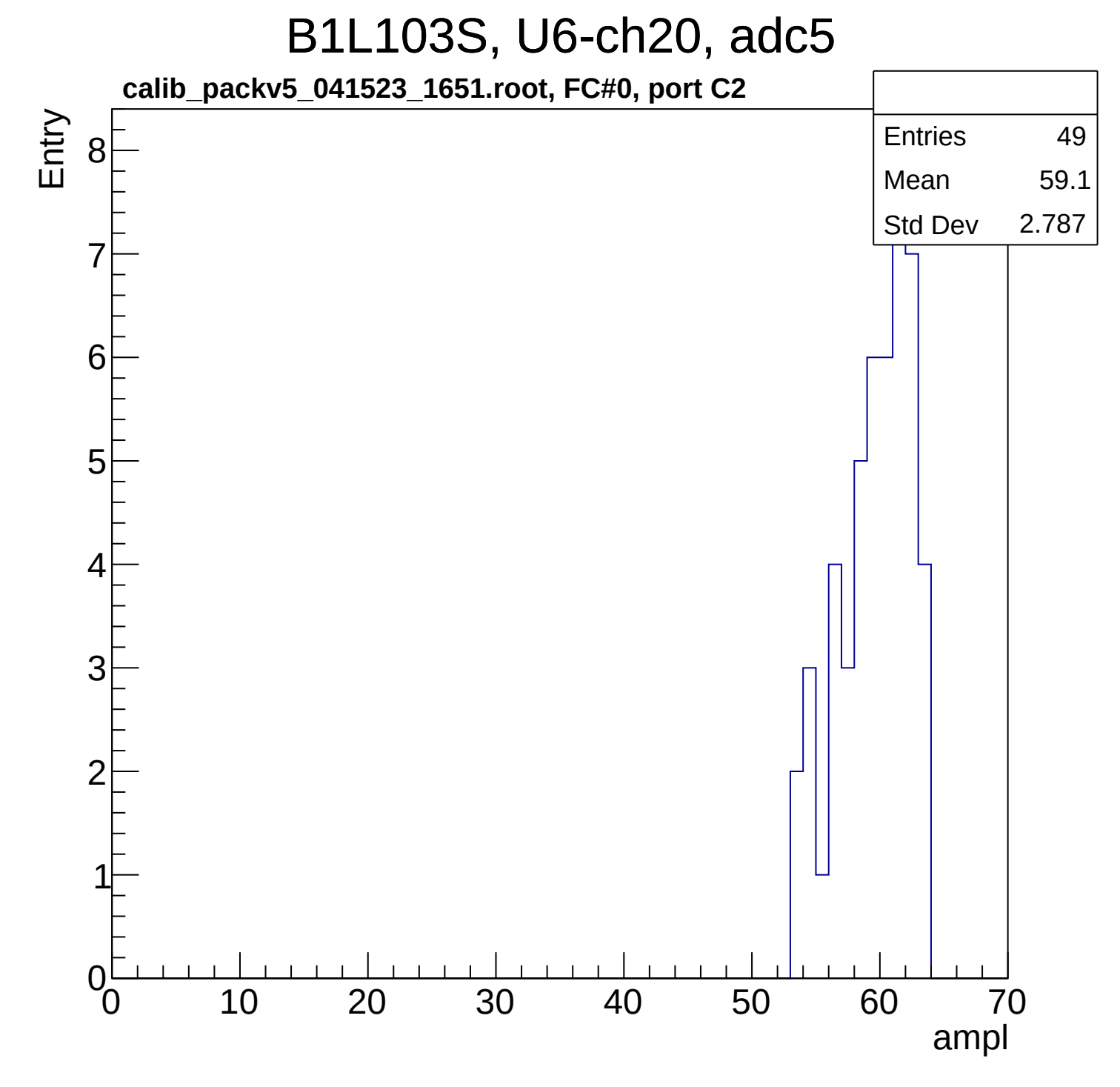
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch20, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 59.1
Std Dev 2.787
Entry
ampl
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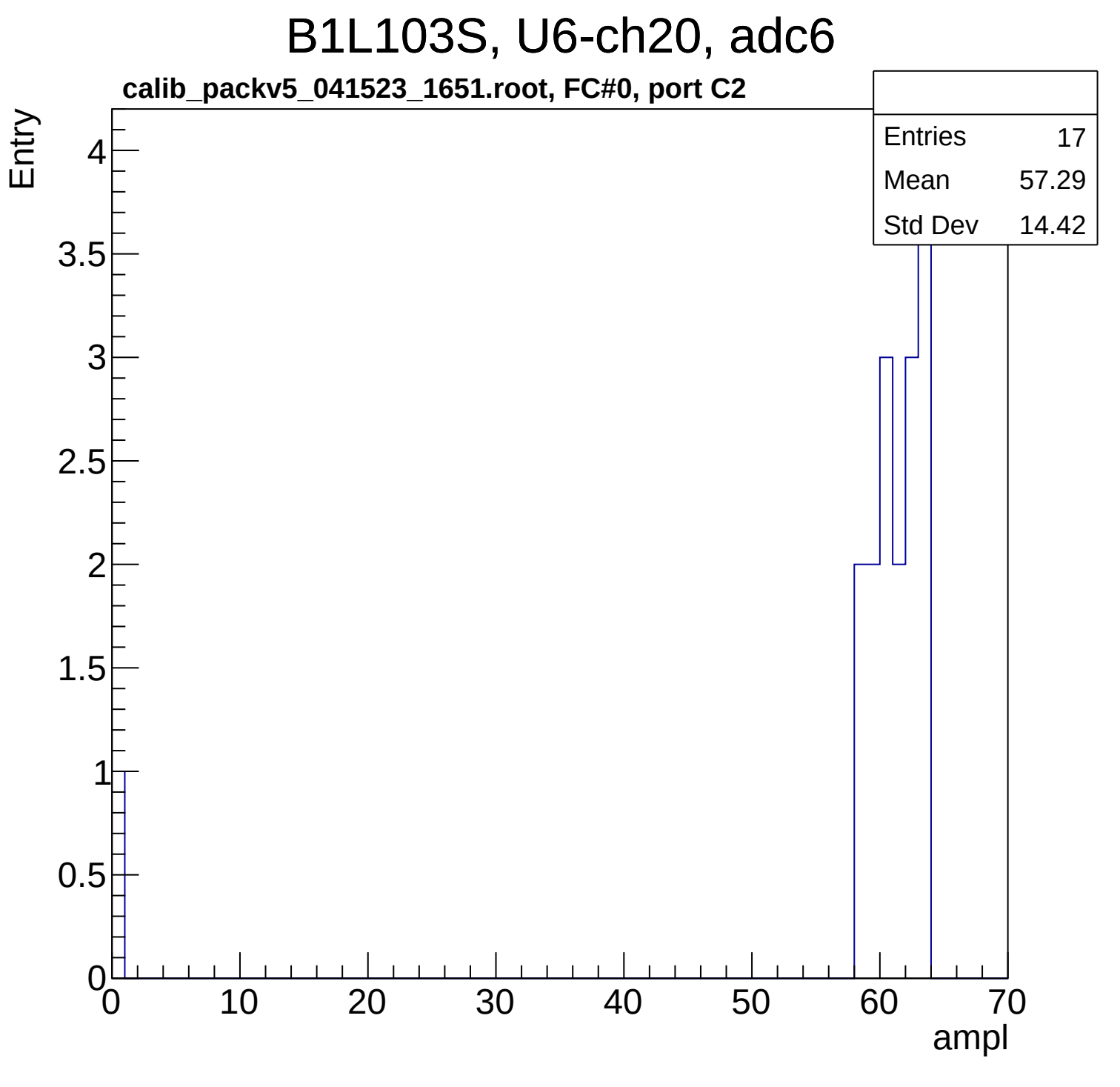
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch20, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 57.29
Std Dev 14.42
Entry
ampl
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1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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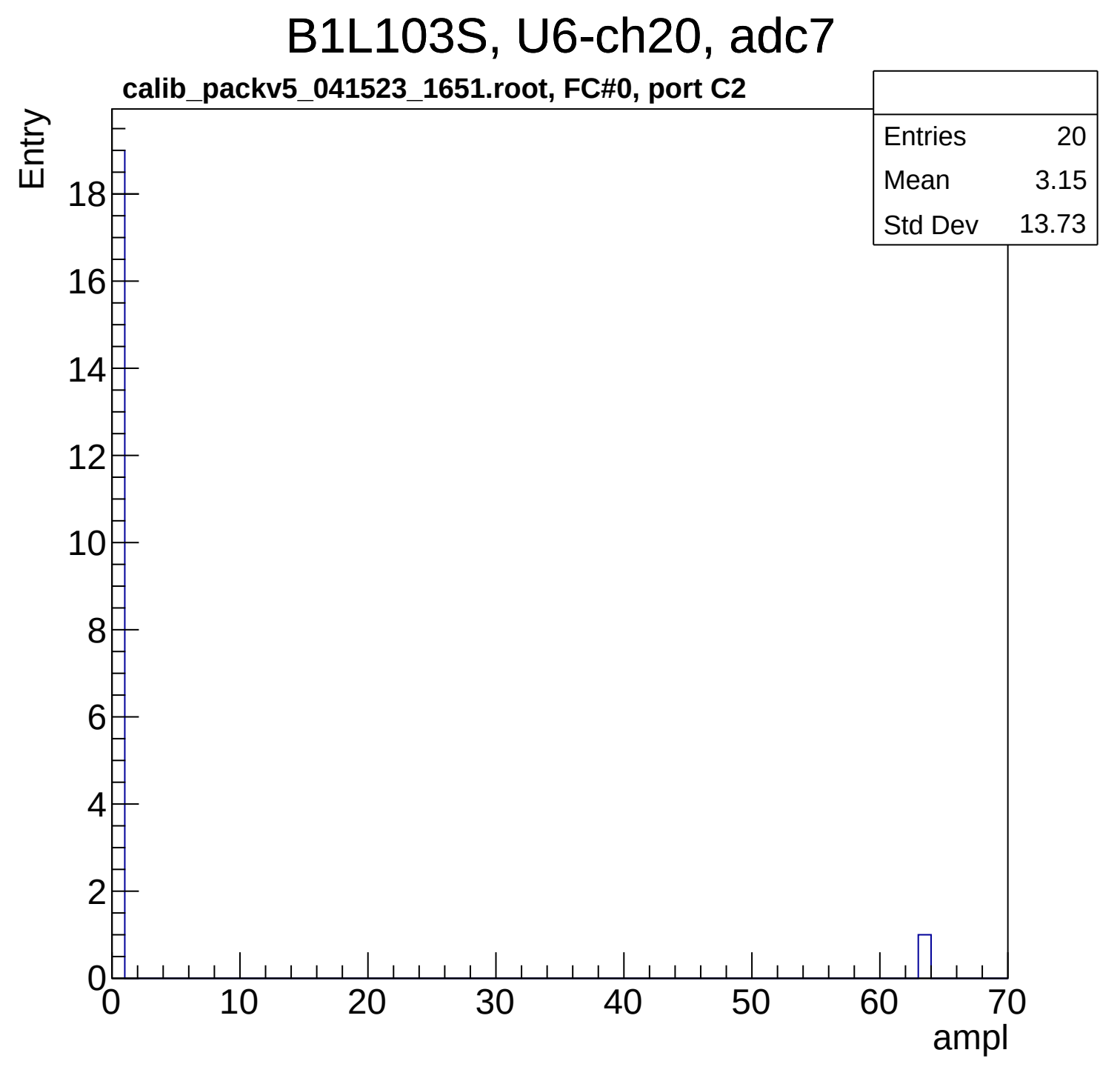
B1L103S, U6-ch20, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
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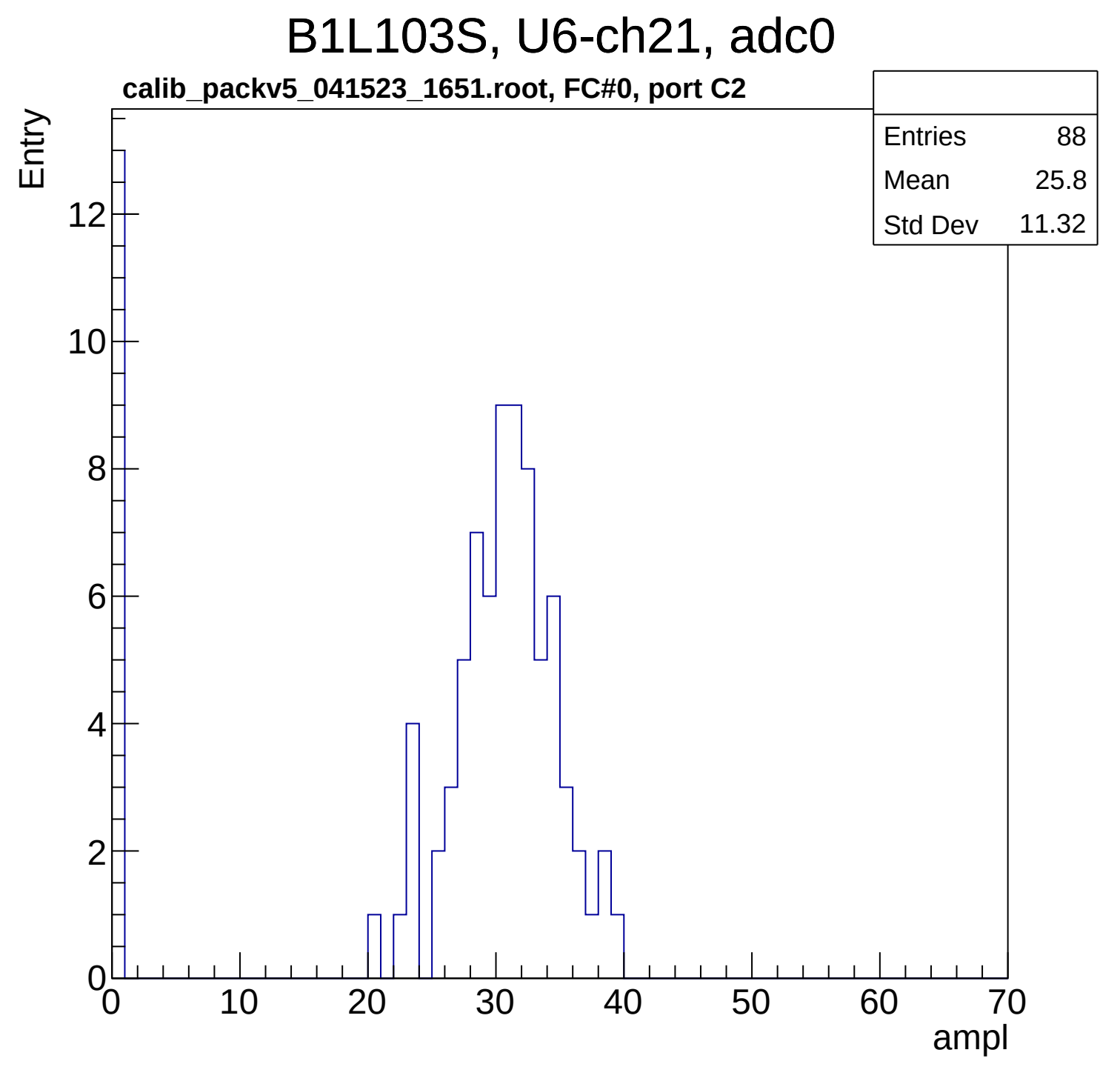
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch21, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 25.8
Std Dev 11.32
Entry
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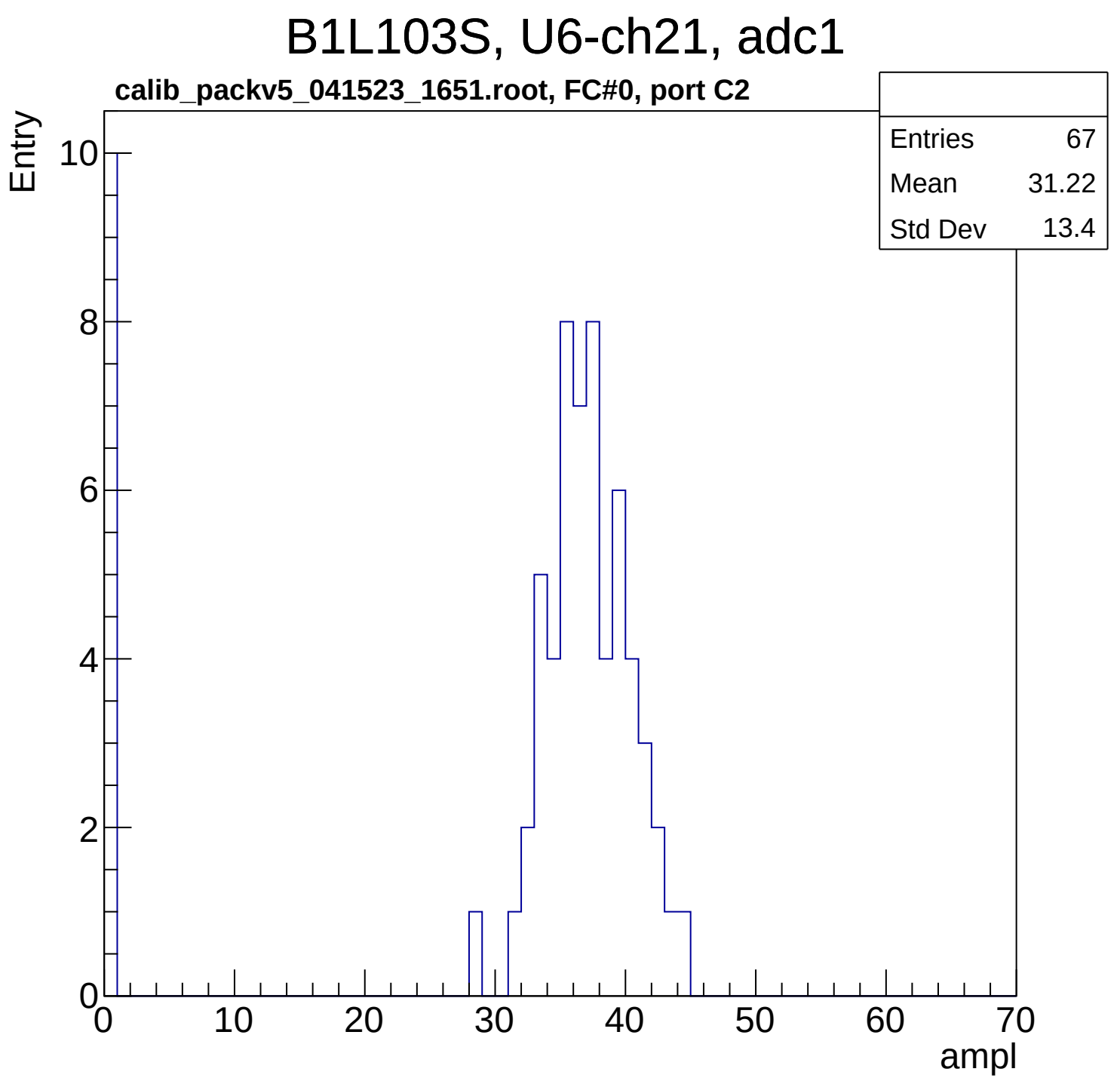
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch21, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 31.22
Std Dev 13.4
Entry
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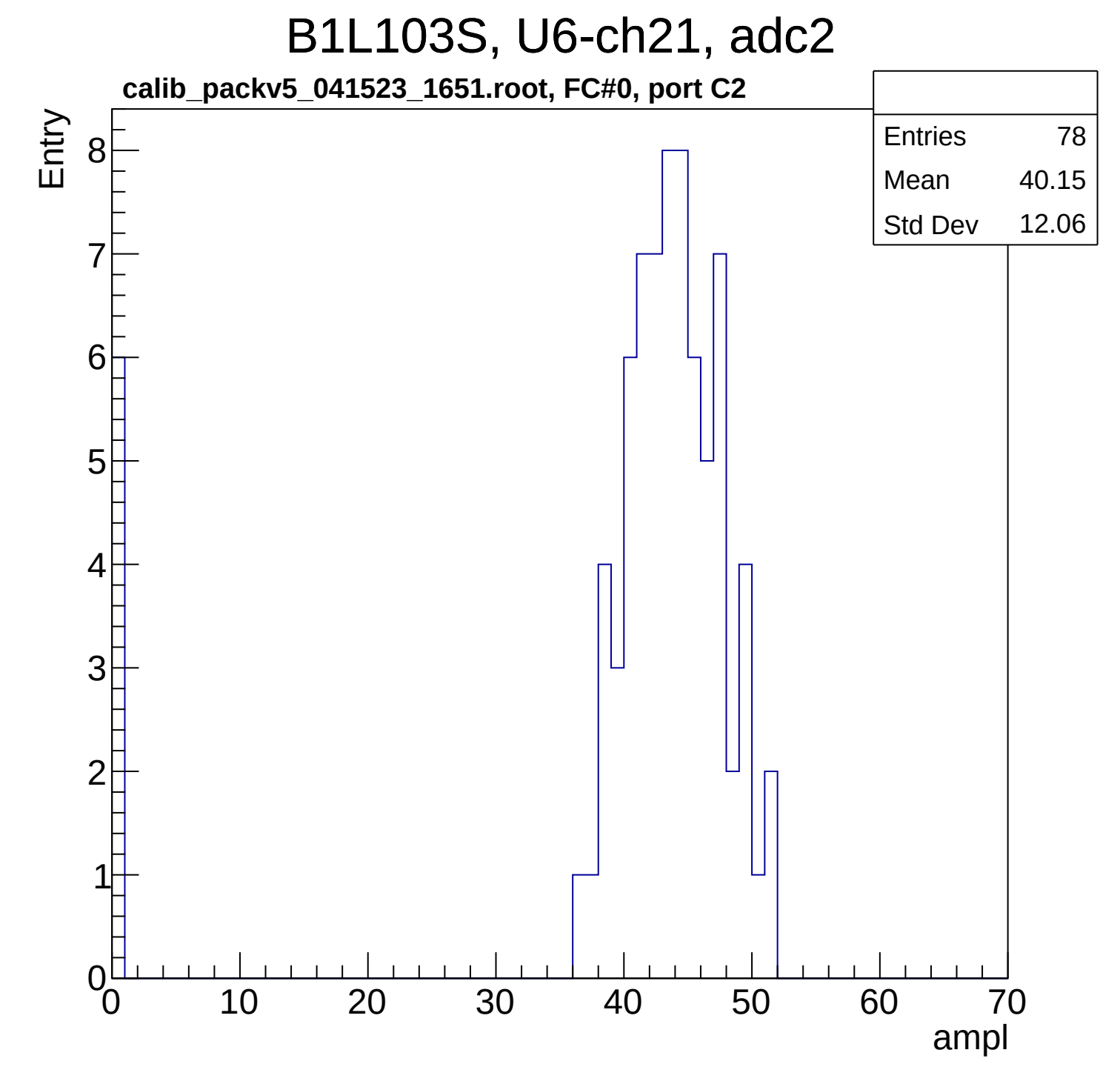
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch21, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 40.15
Std Dev 12.06
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
50
60
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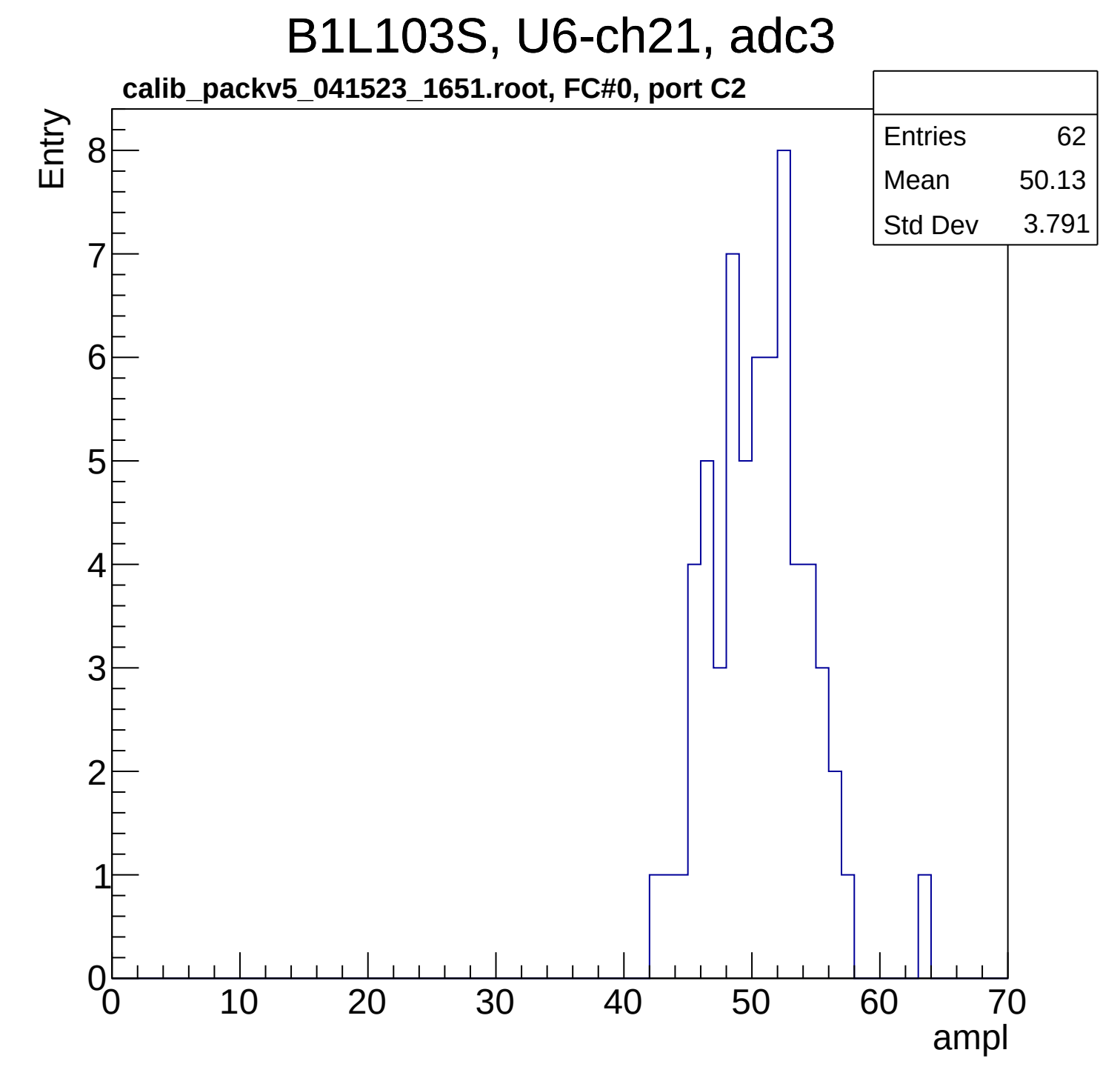
B1L103S, U6-ch21, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 50.13
Std Dev 3.791
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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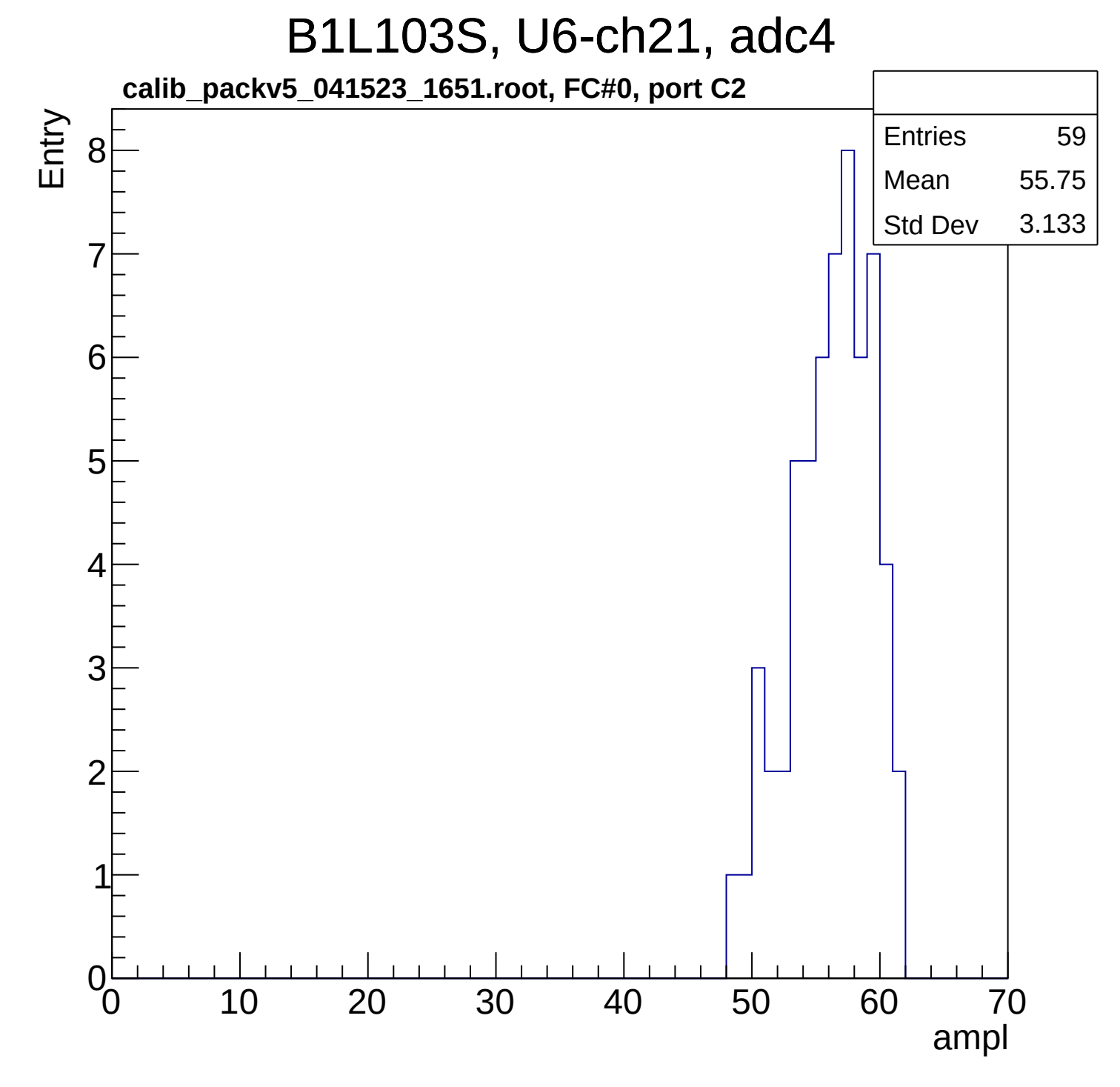
B1L103S, U6-ch21, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 55.75
Std Dev 3.133
Entry
ampl
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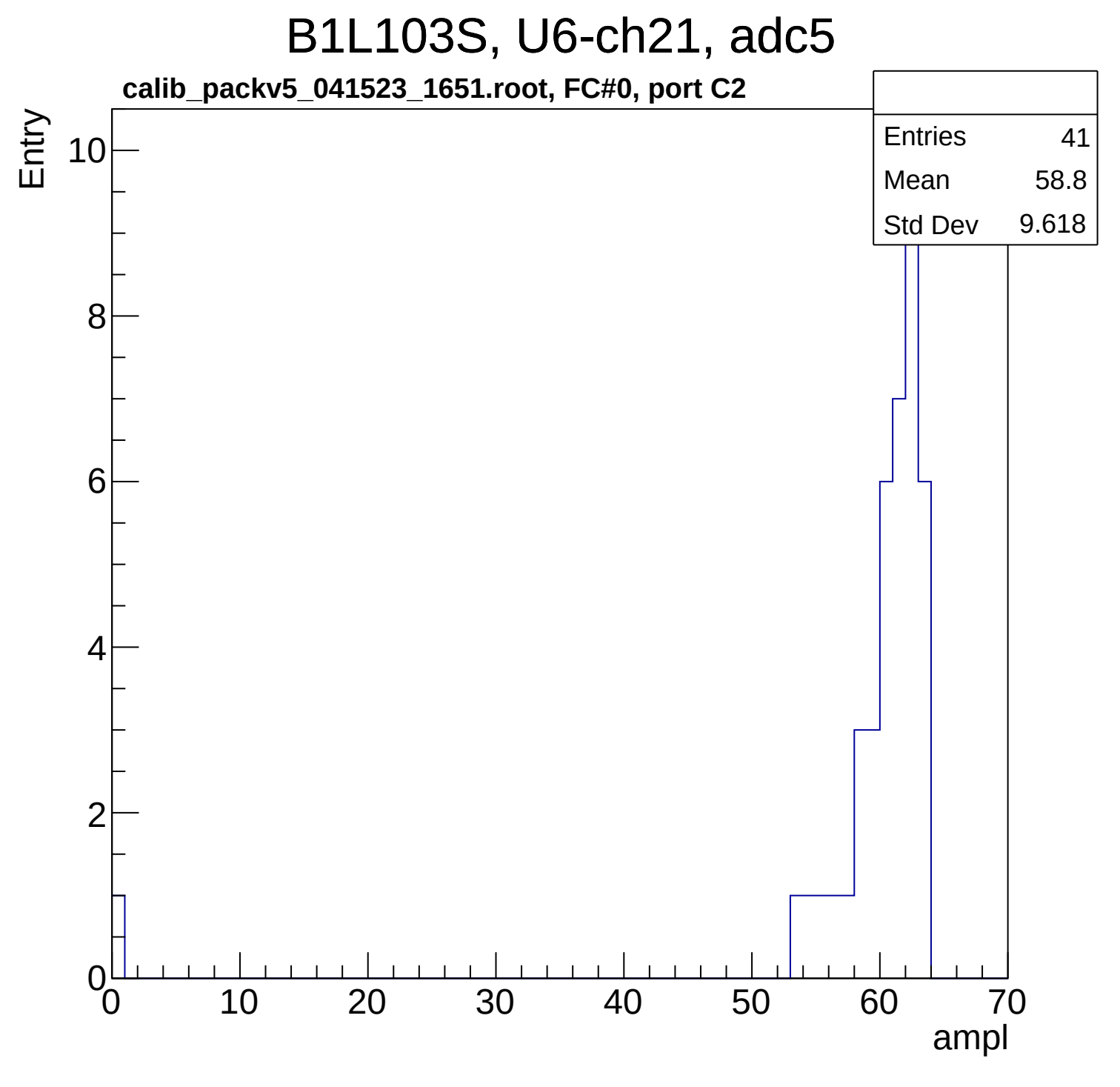
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch21, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 58.8
Std Dev 9.618
Entry
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4
6
8
10
0
10
20
30
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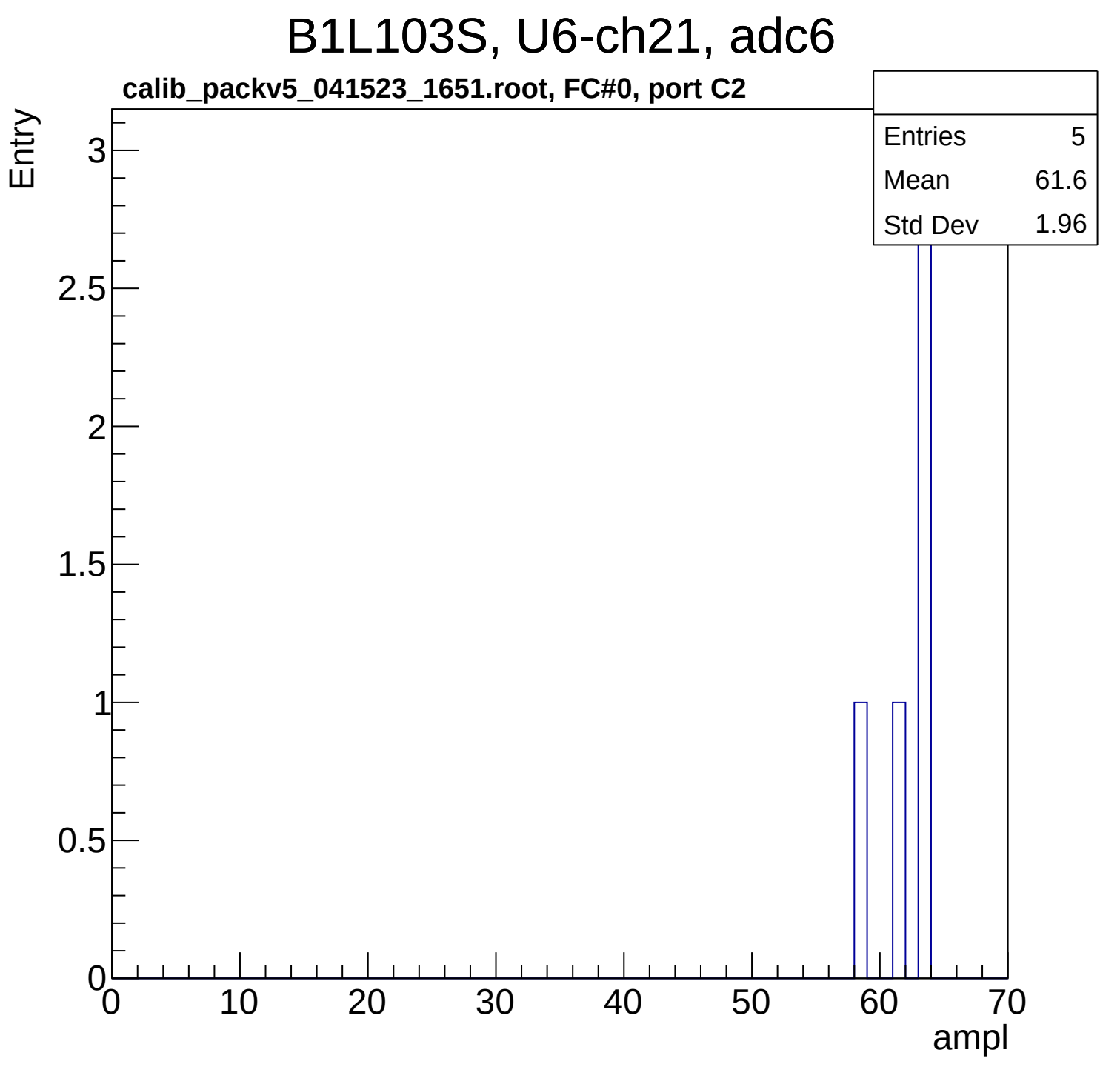
50
60
70
ampl


B1L103S, U6-ch21, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 61.6
Std Dev 1.96
Entry
ampl
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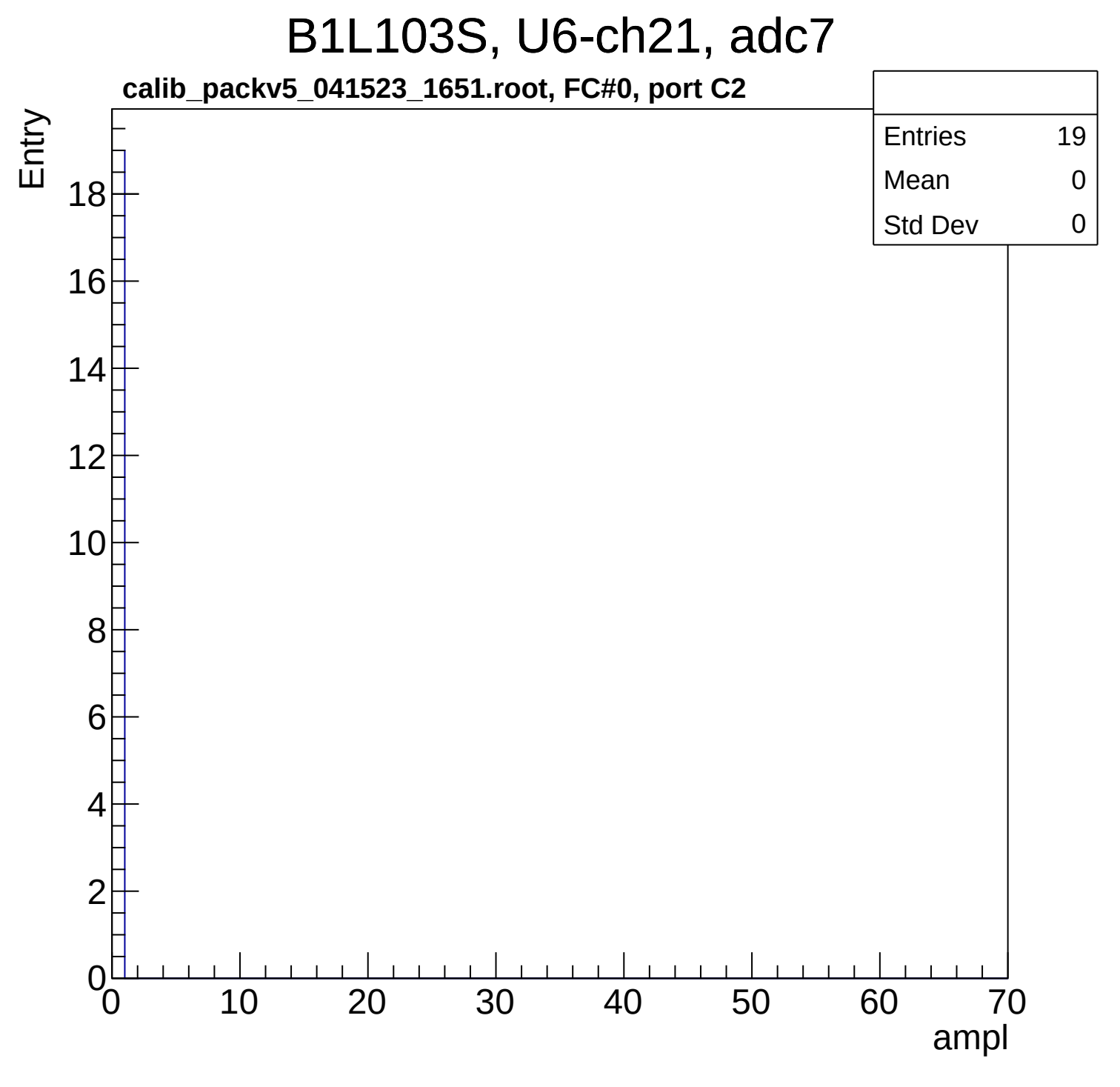
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U6-ch21, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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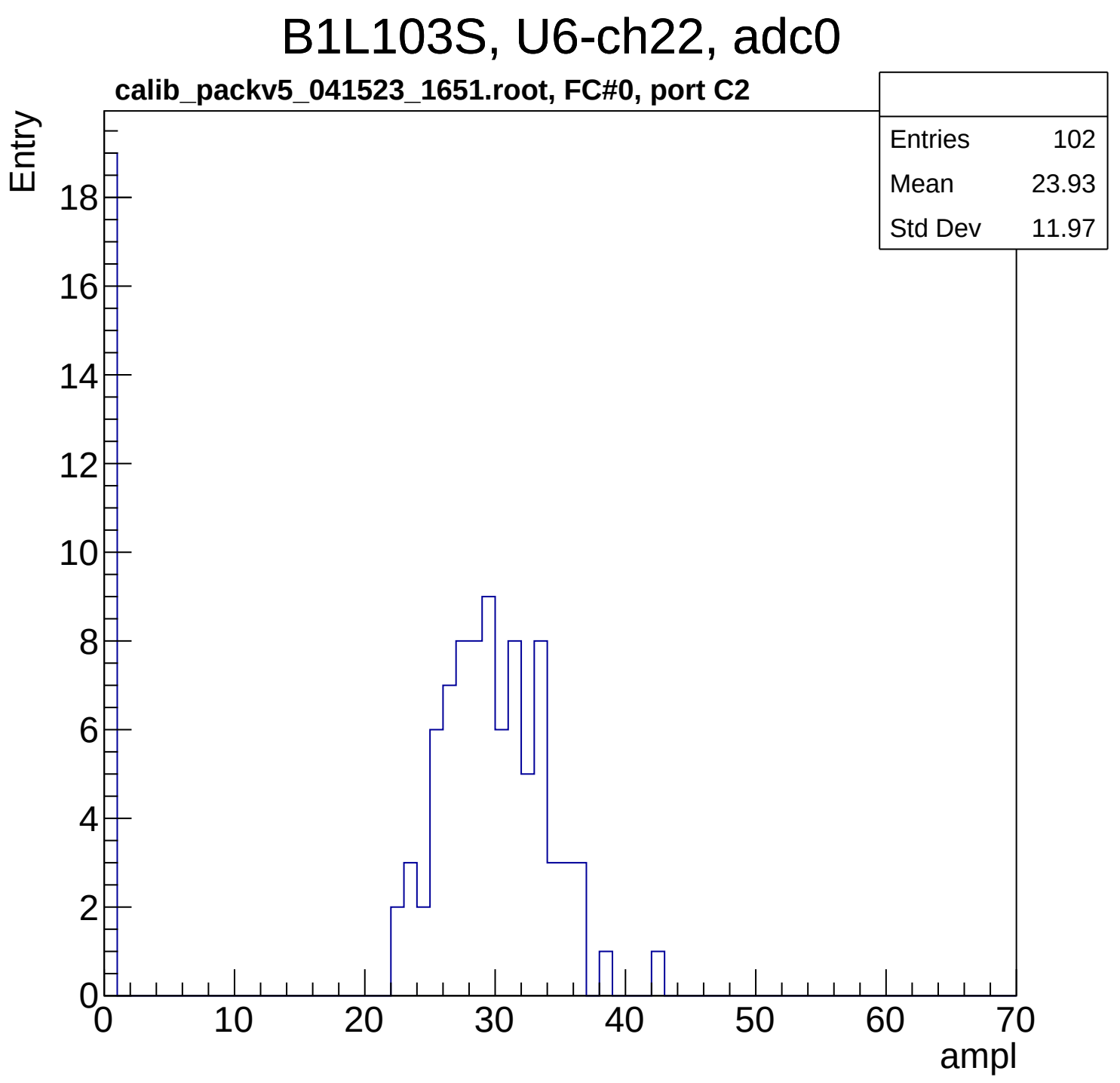
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch22, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 102
Mean 23.93
Std Dev 11.97
Entry
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6
8
10
12
14
16
18
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10
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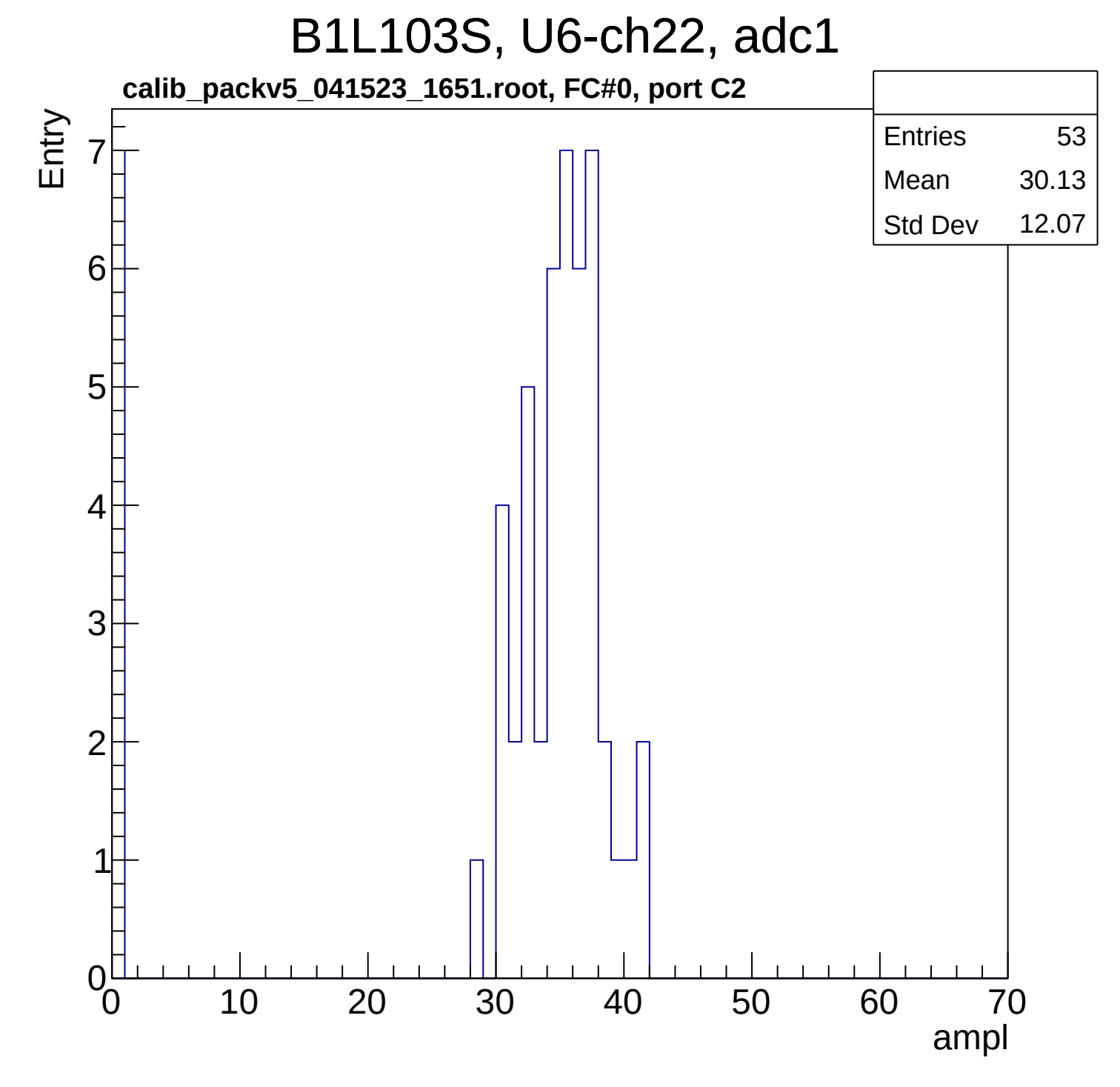
50
60
70
ampl


B1L103S, U6-ch22, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 30.13
Std Dev 12.07
Entry
ampl
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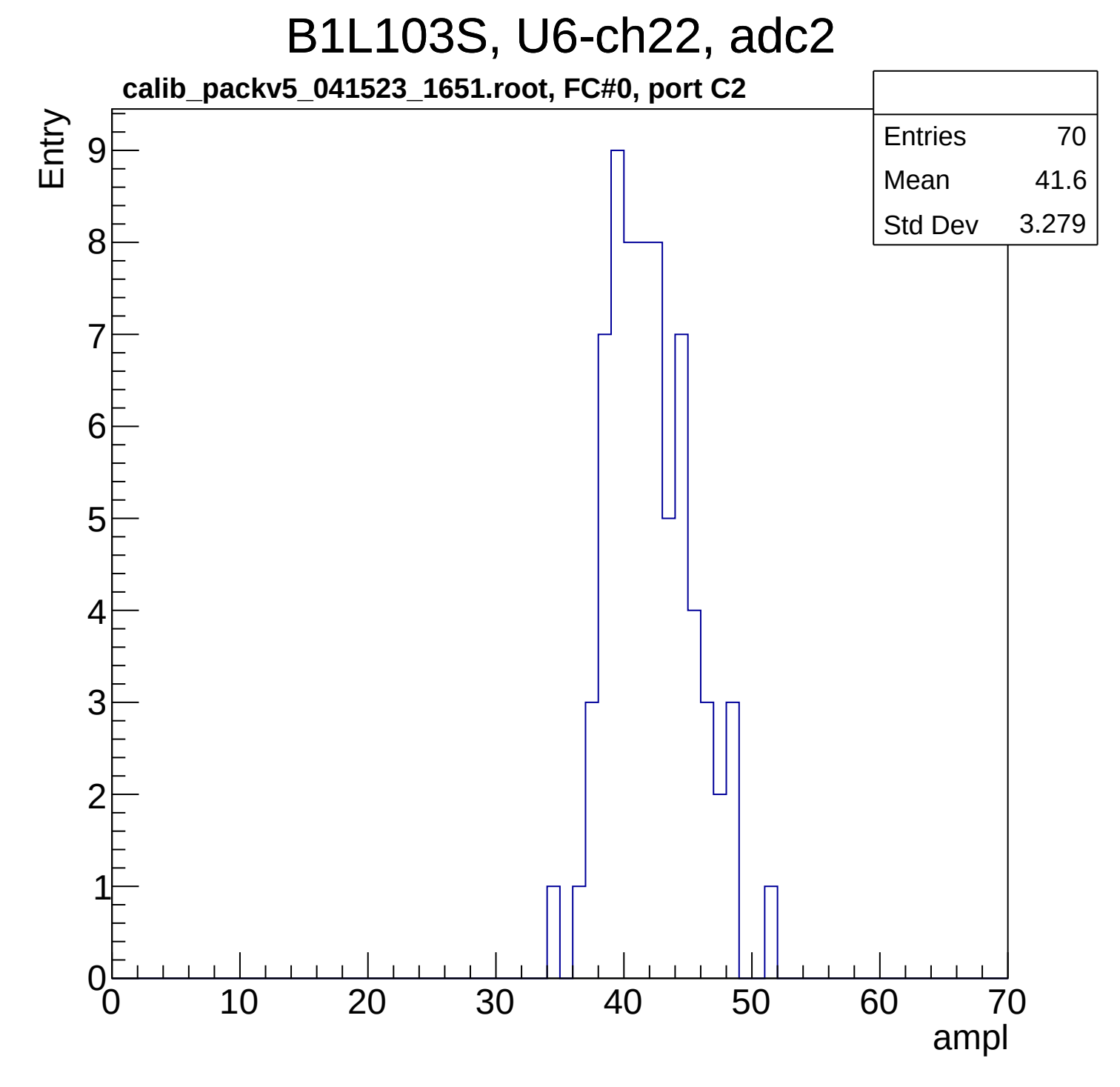
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U6-ch22, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 41.6
Std Dev 3.279
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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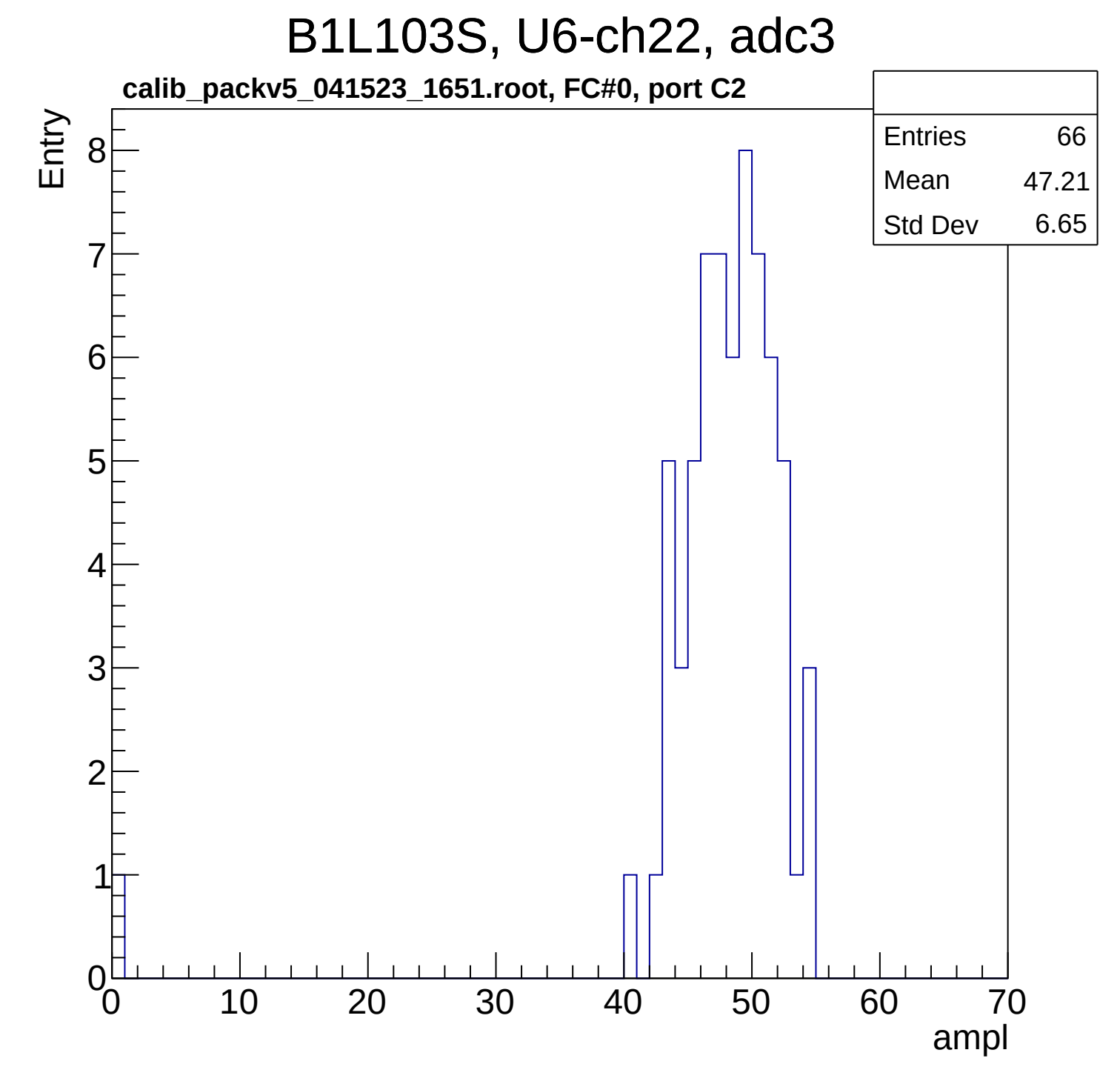
60
70


B1L103S, U6-ch22, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 47.21
Std Dev 6.65
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
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40
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60
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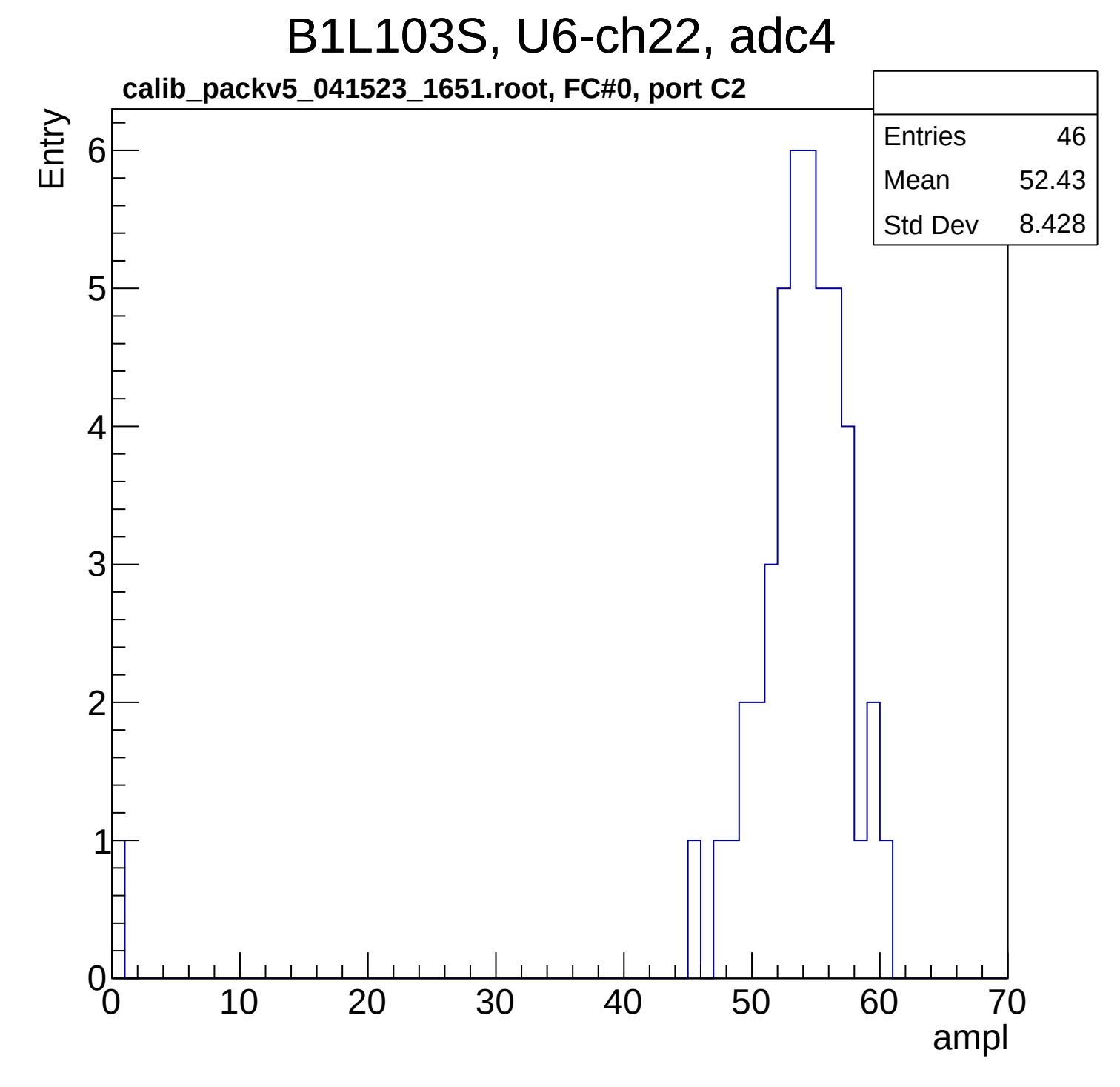
B1L103S, U6-ch22, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 52.43
Std Dev 8.428
Entry
ampl
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1
2
3
4
5
6
0
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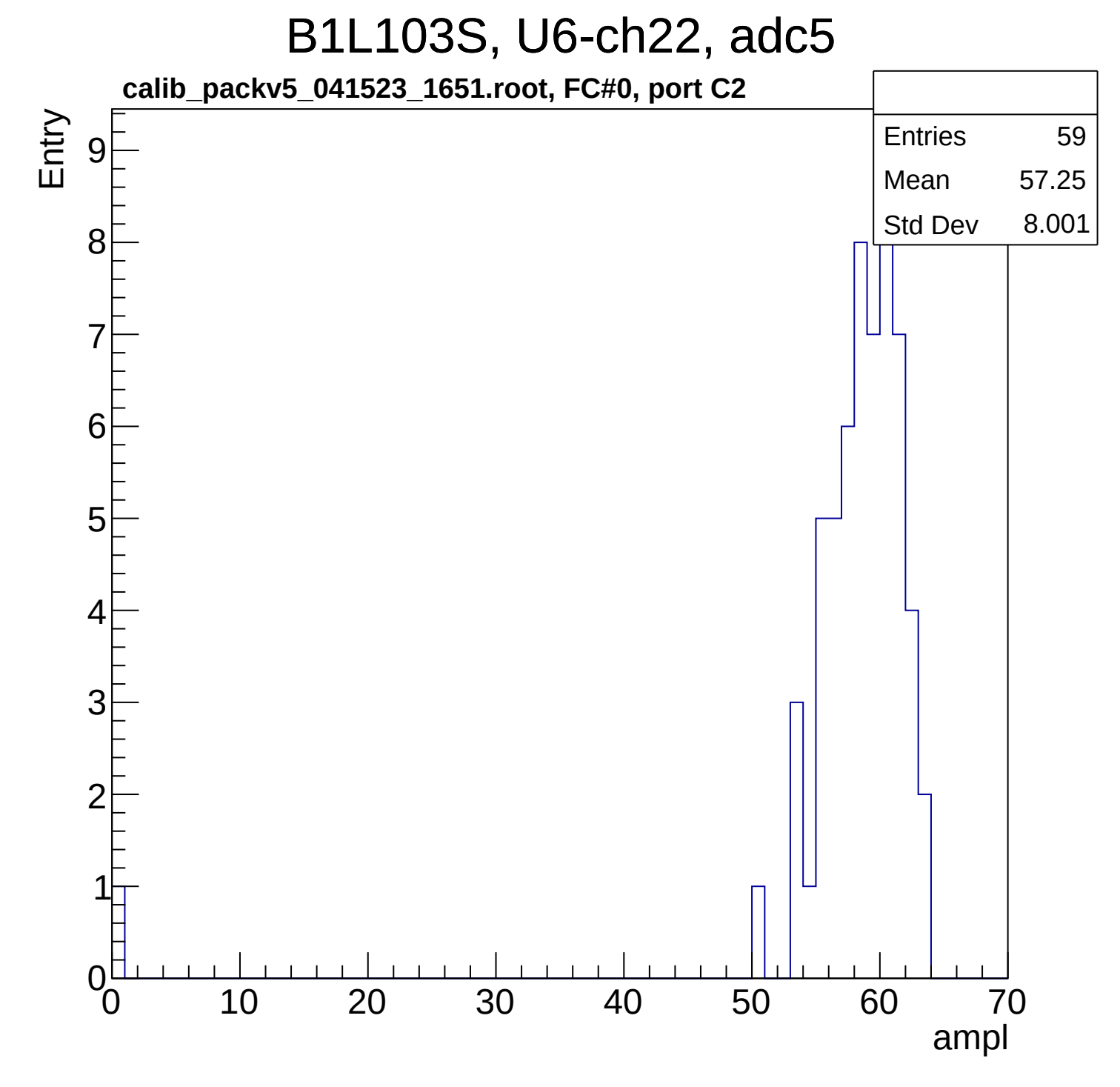
20
30
40
50
60
70


B1L103S, U6-ch22, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 57.25
Std Dev 8.001
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
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60
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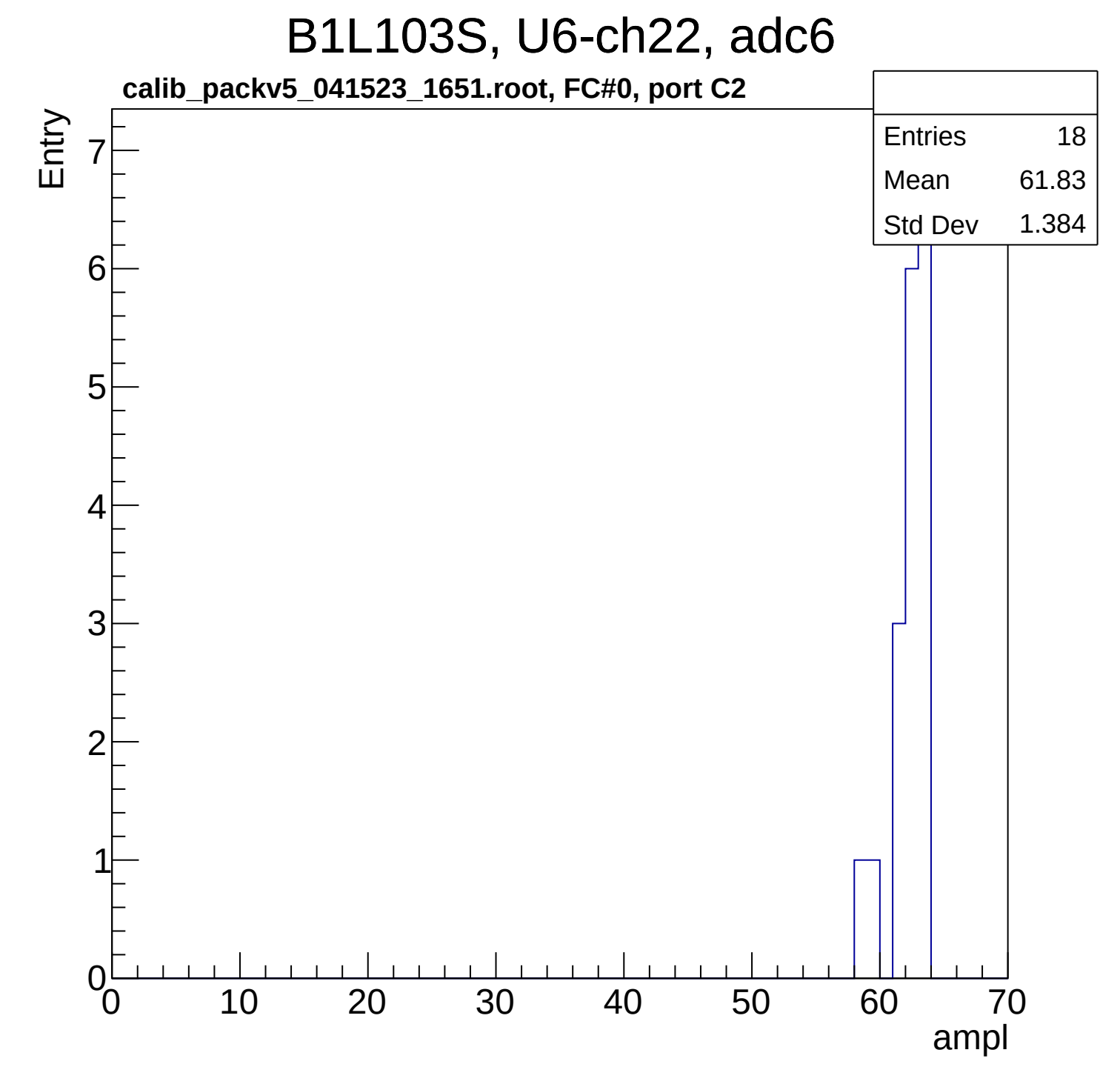
B1L103S, U6-ch22, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 61.83
Std Dev 1.384
Entry
ampl
0
1
2
3
4
5
6
7
0
10
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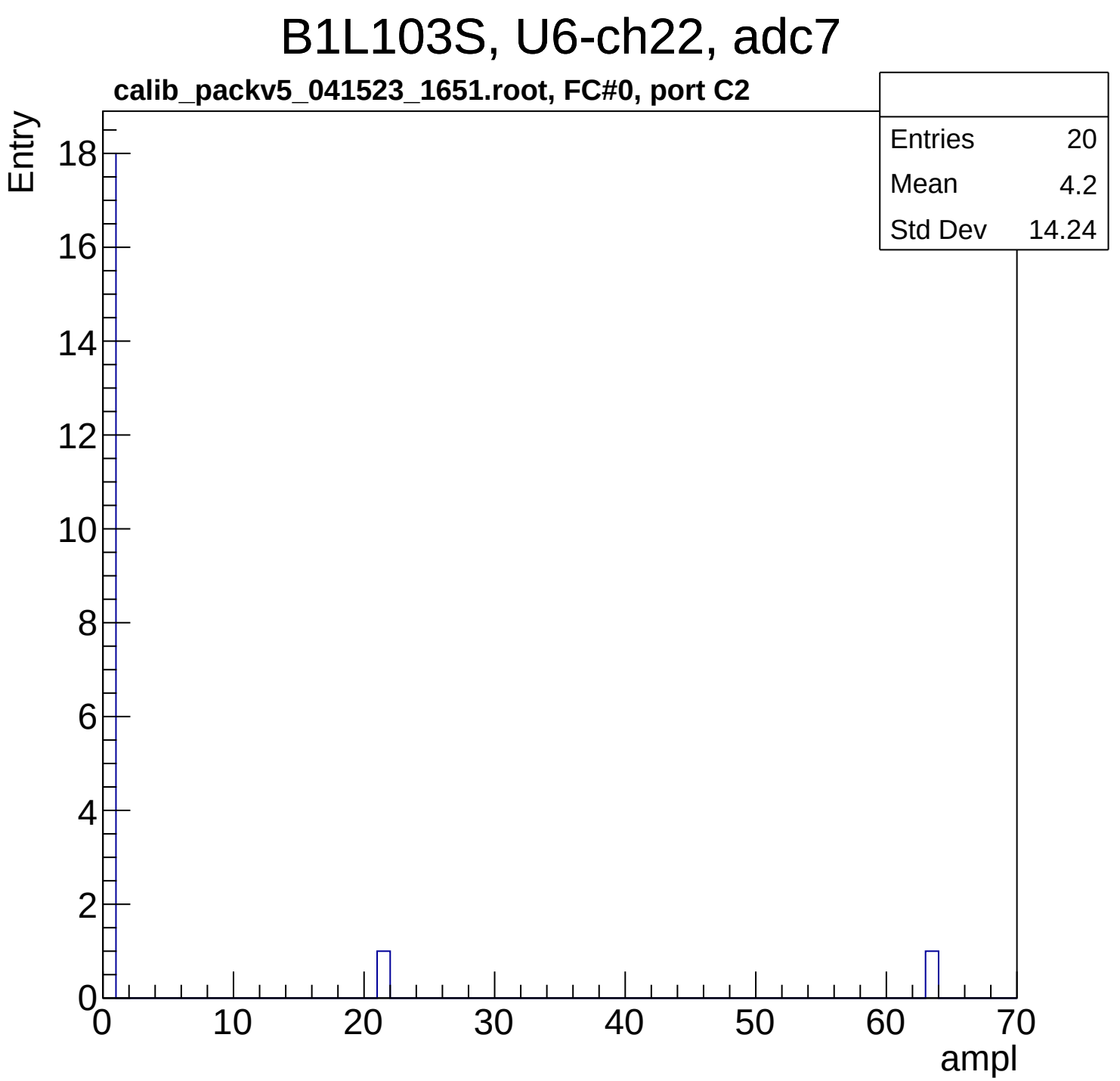
30
40
50
60
70


B1L103S, U6-ch22, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4.2
Std Dev 14.24
Entry
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8
10
12
14
16
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10
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50
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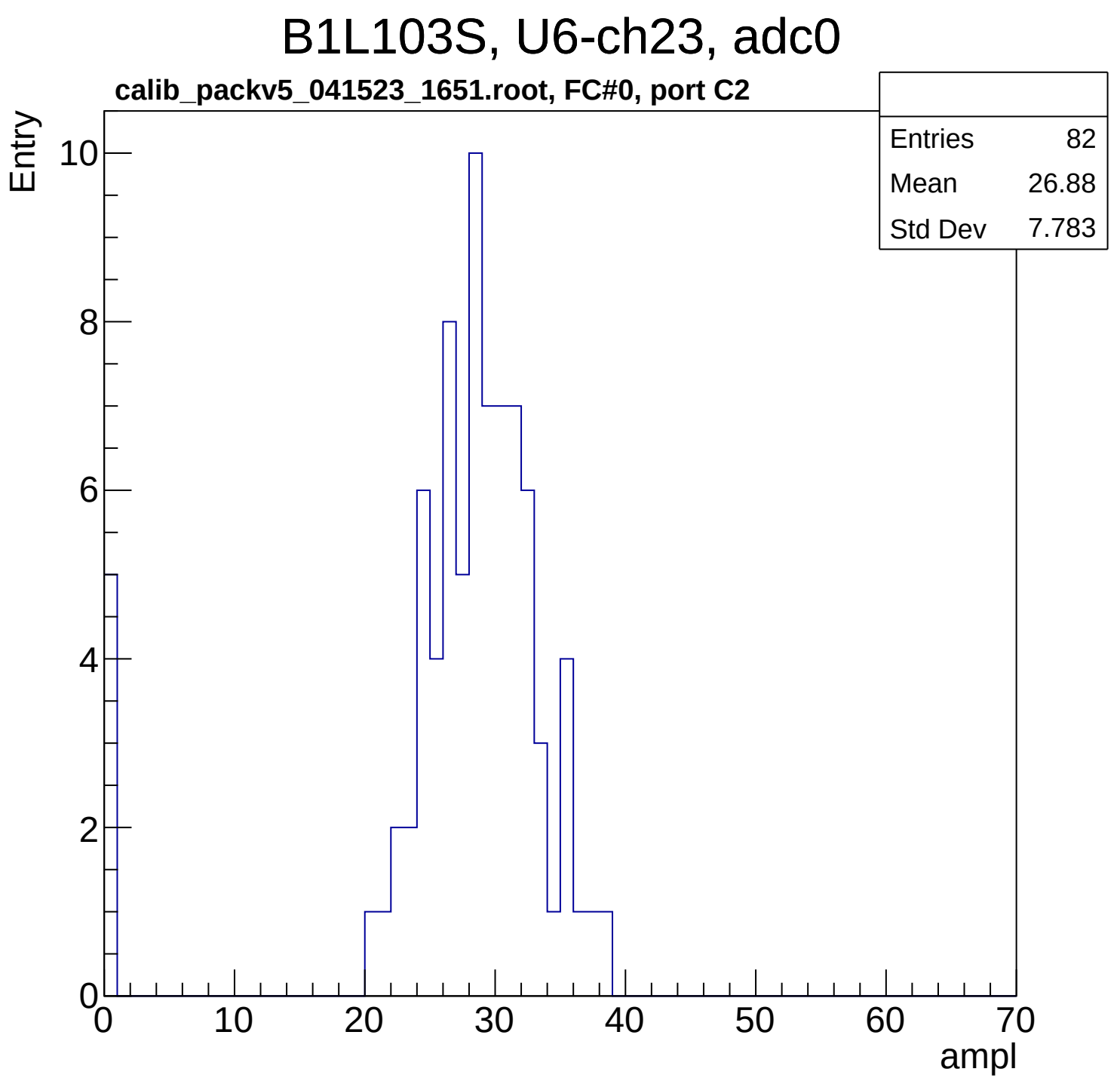
70
ampl


B1L103S, U6-ch23, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 26.88
Std Dev 7.783
Entry
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10
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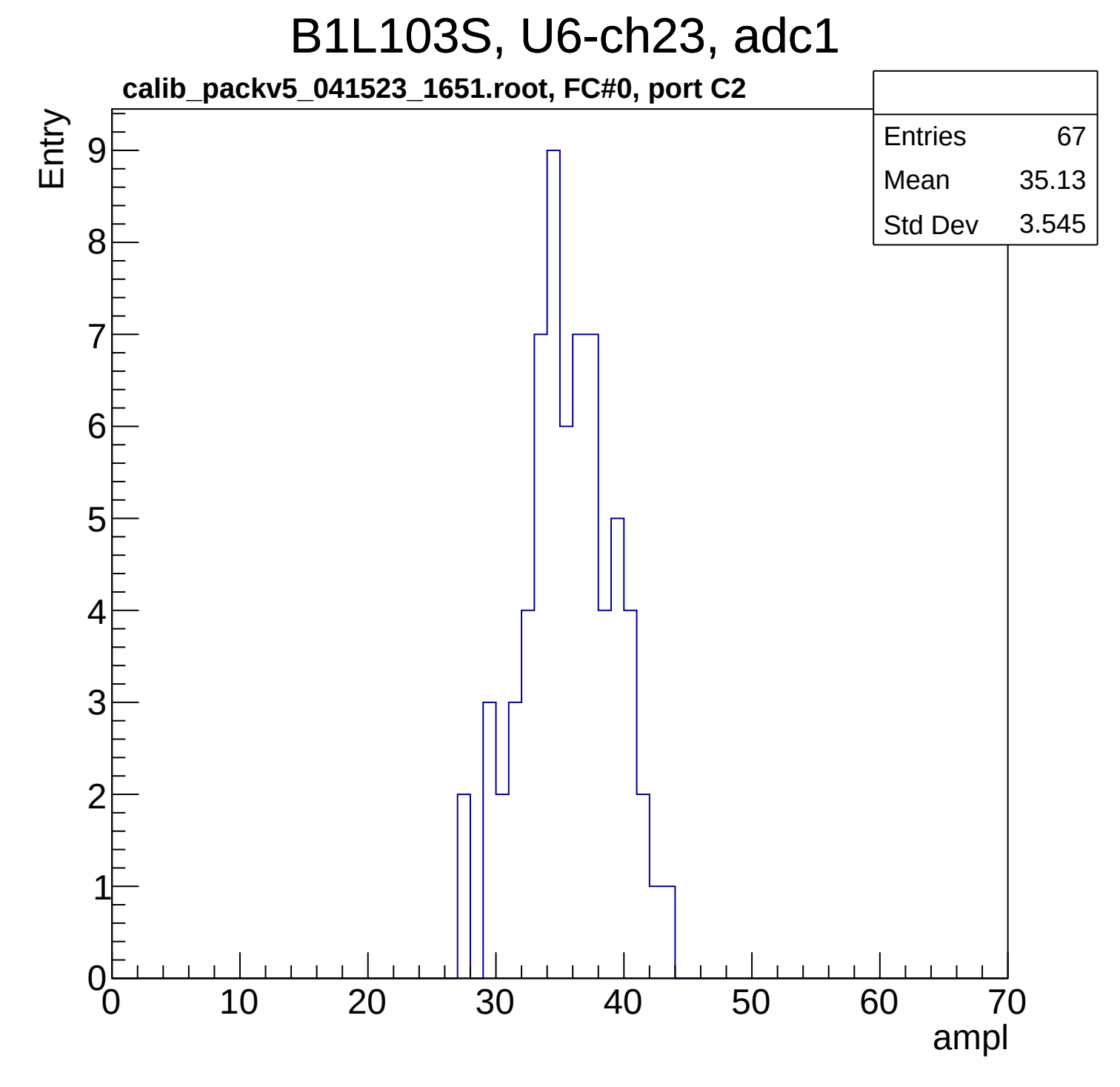
50
60
70
ampl


B1L103S, U6-ch23, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 35.13
Std Dev 3.545
Entry
ampl
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3
4
5
6
7
8
9
0
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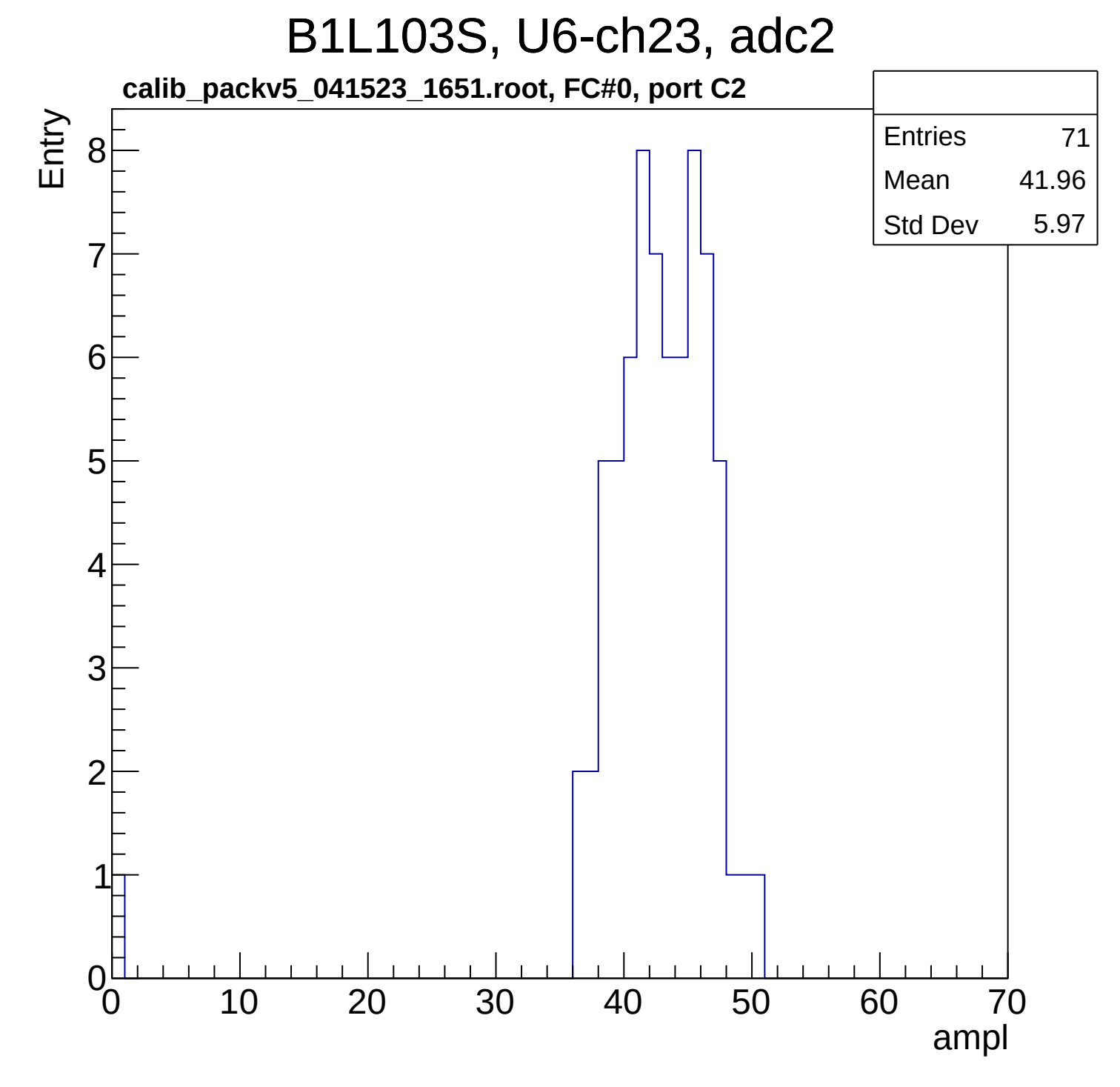
40
50
60
70


B1L103S, U6-ch23, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 41.96
Std Dev 5.97
Entry
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2
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4
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6
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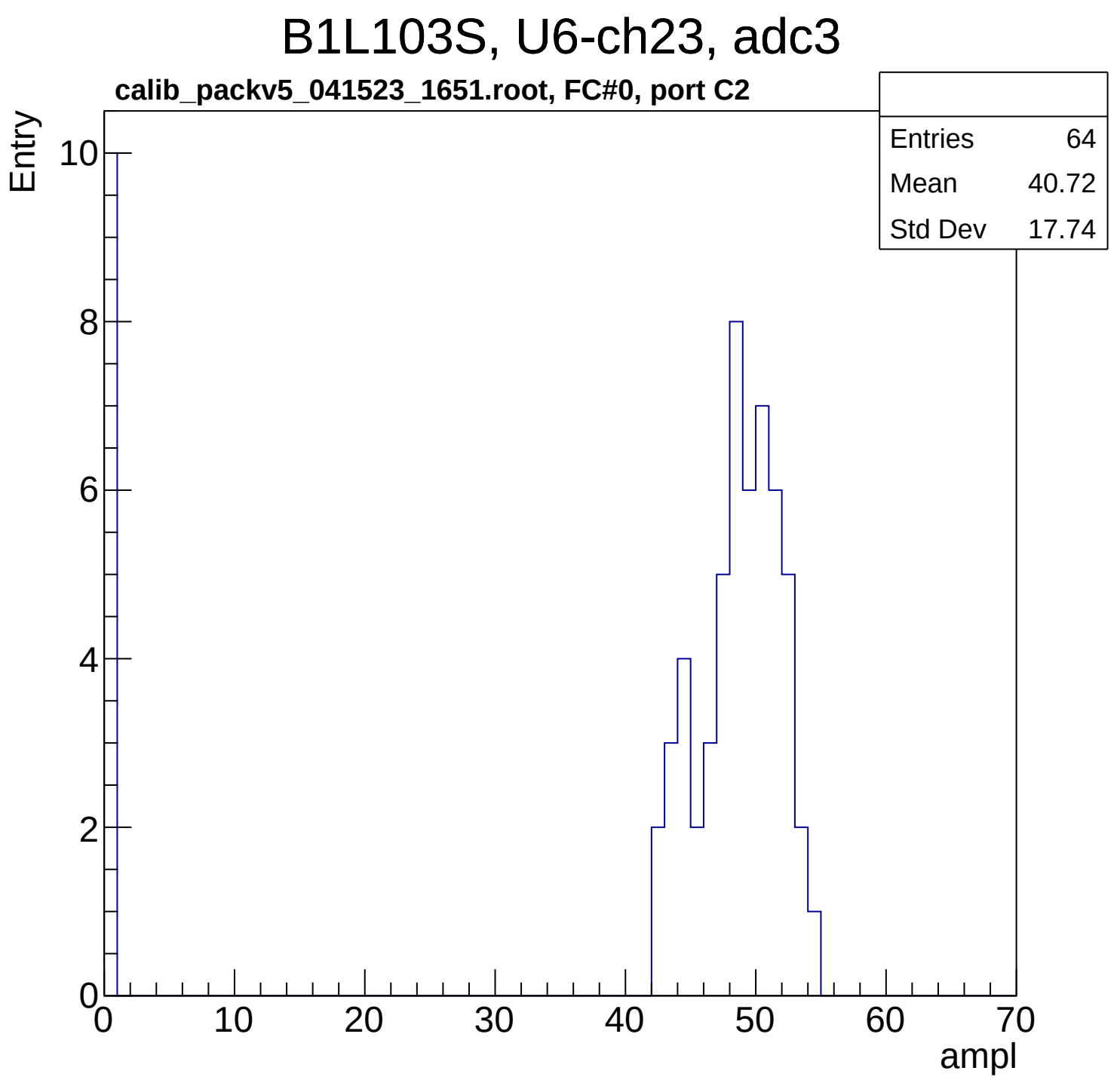
ampl


B1L103S, U6-ch23, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 40.72
Std Dev 17.74
Entry
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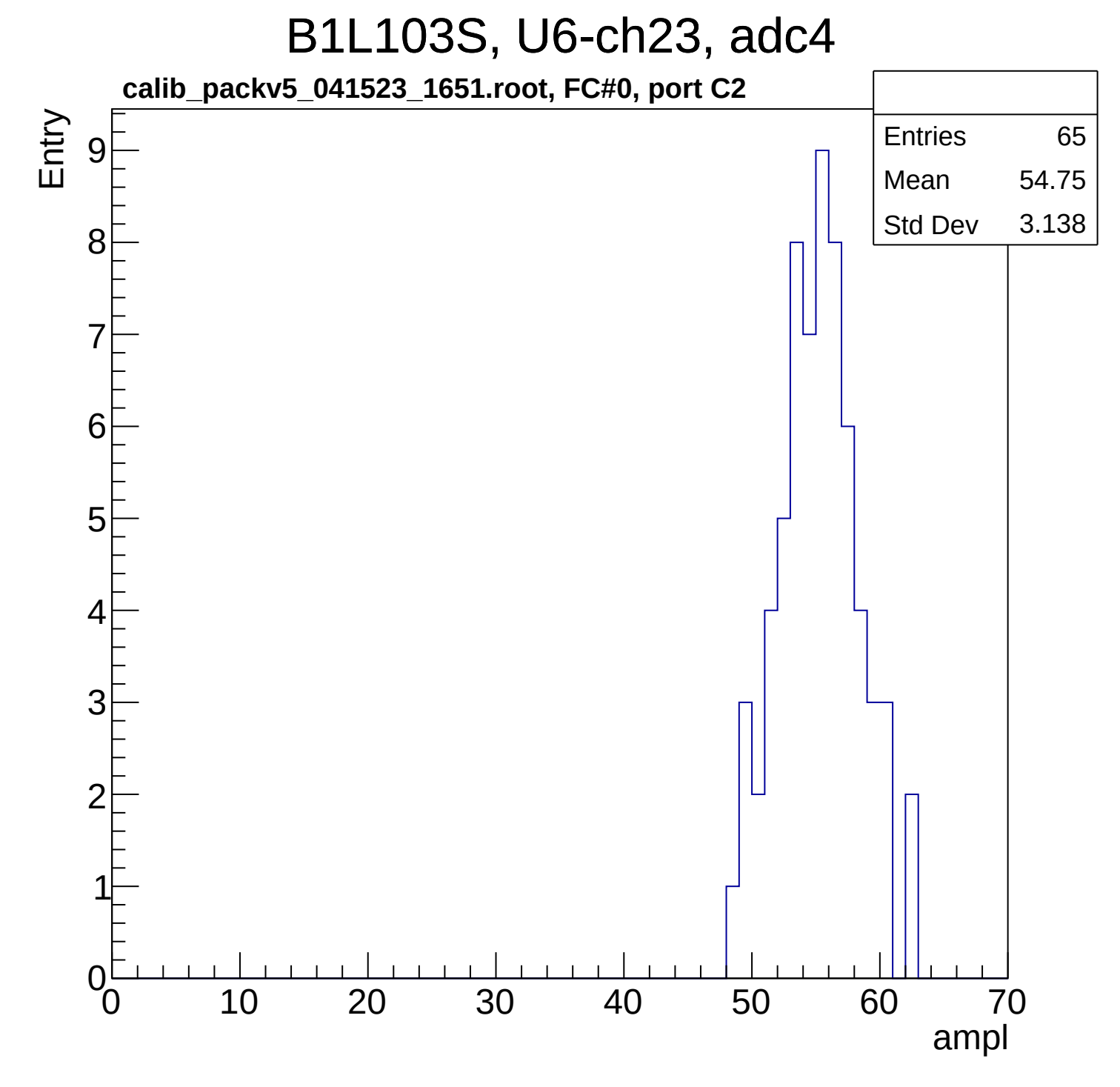
70
ampl


B1L103S, U6-ch23, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 54.75
Std Dev 3.138
Entry
ampl
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0
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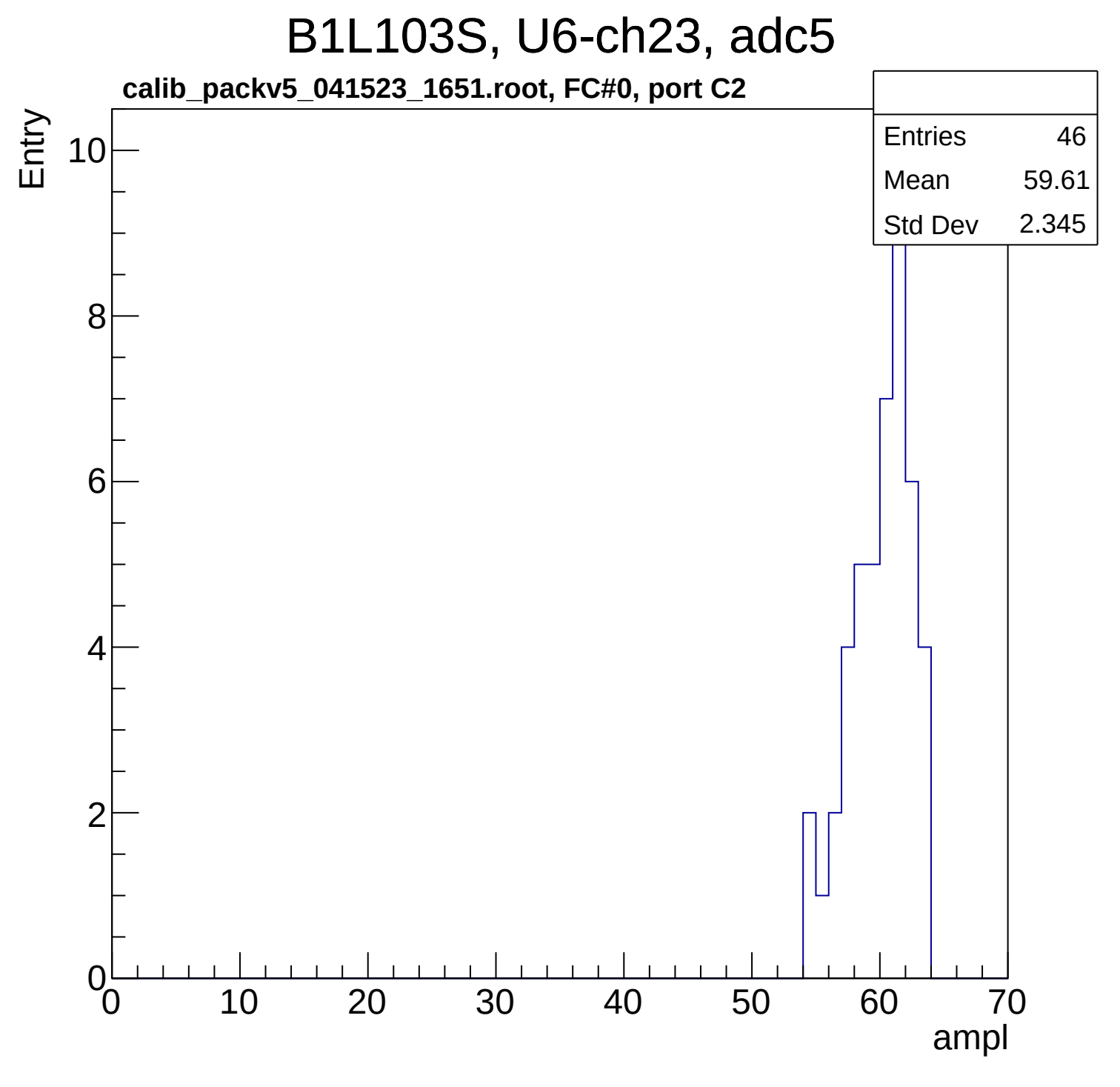
B1L103S, U6-ch23, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 59.61
Std Dev 2.345
Entry
ampl
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40
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60
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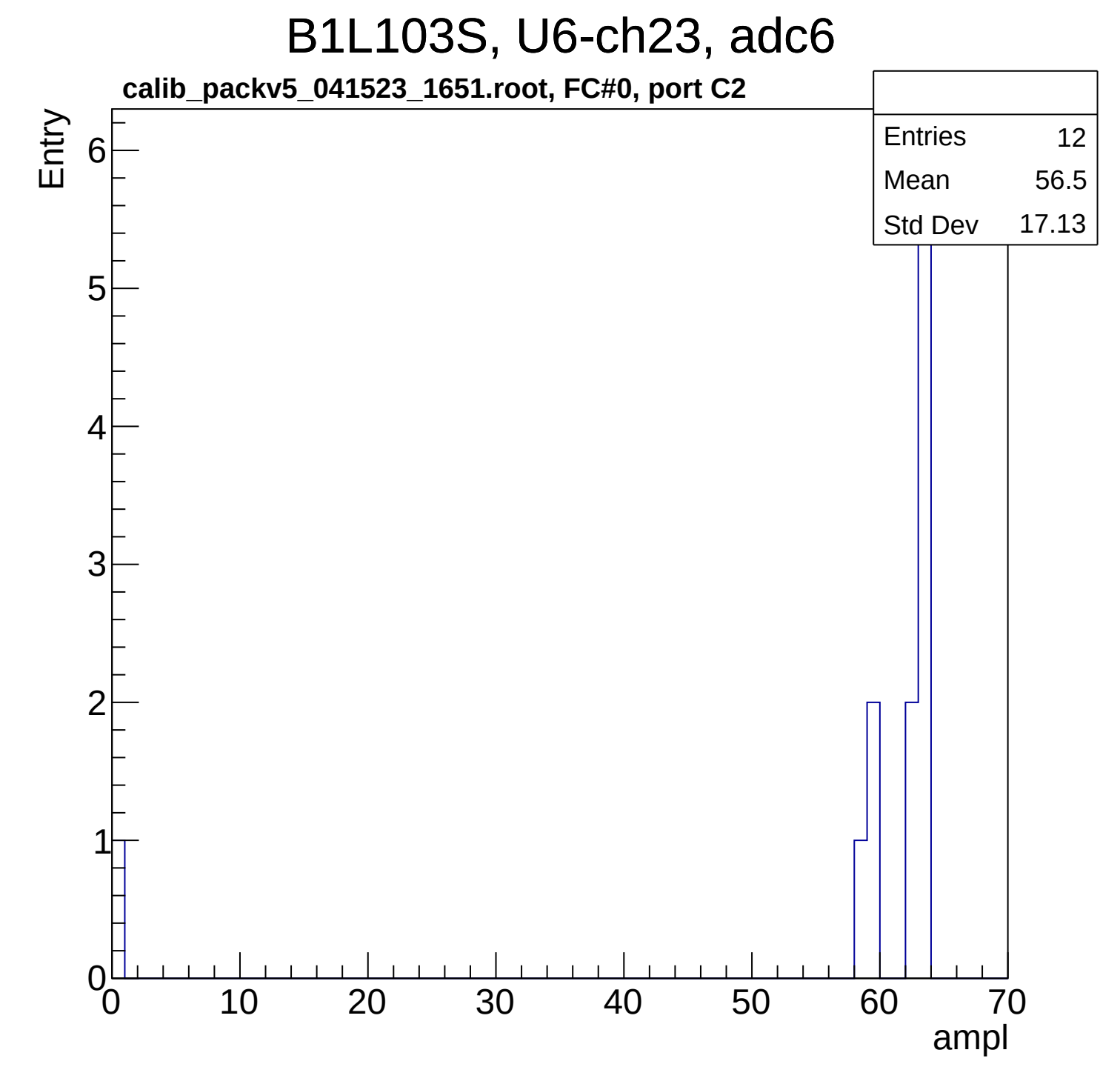
B1L103S, U6-ch23, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 56.5
Std Dev 17.13
Entry
0
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2
3
4
5
6
0
10
20
30
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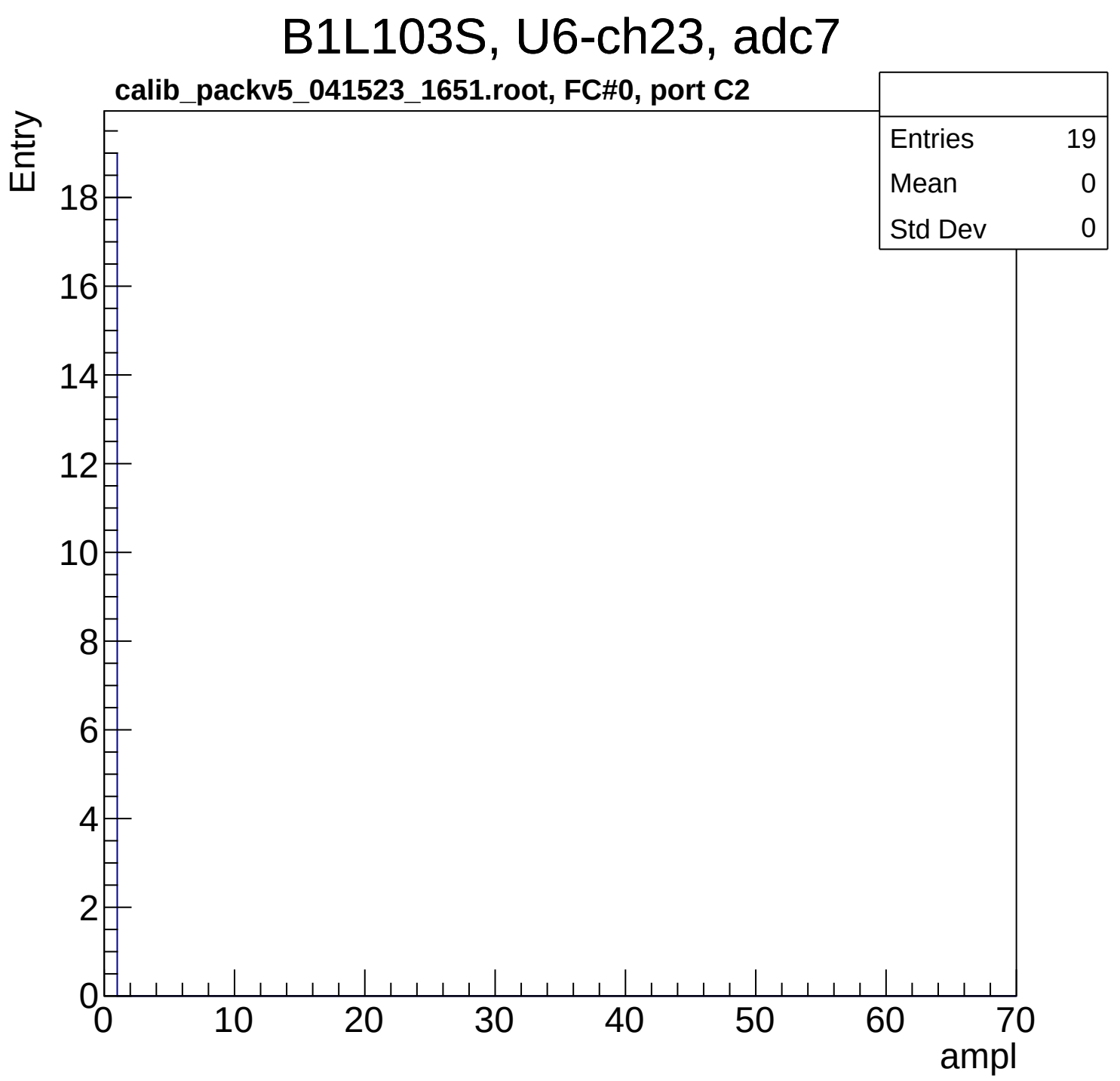
50
60
70
ampl


B1L103S, U6-ch23, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
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10
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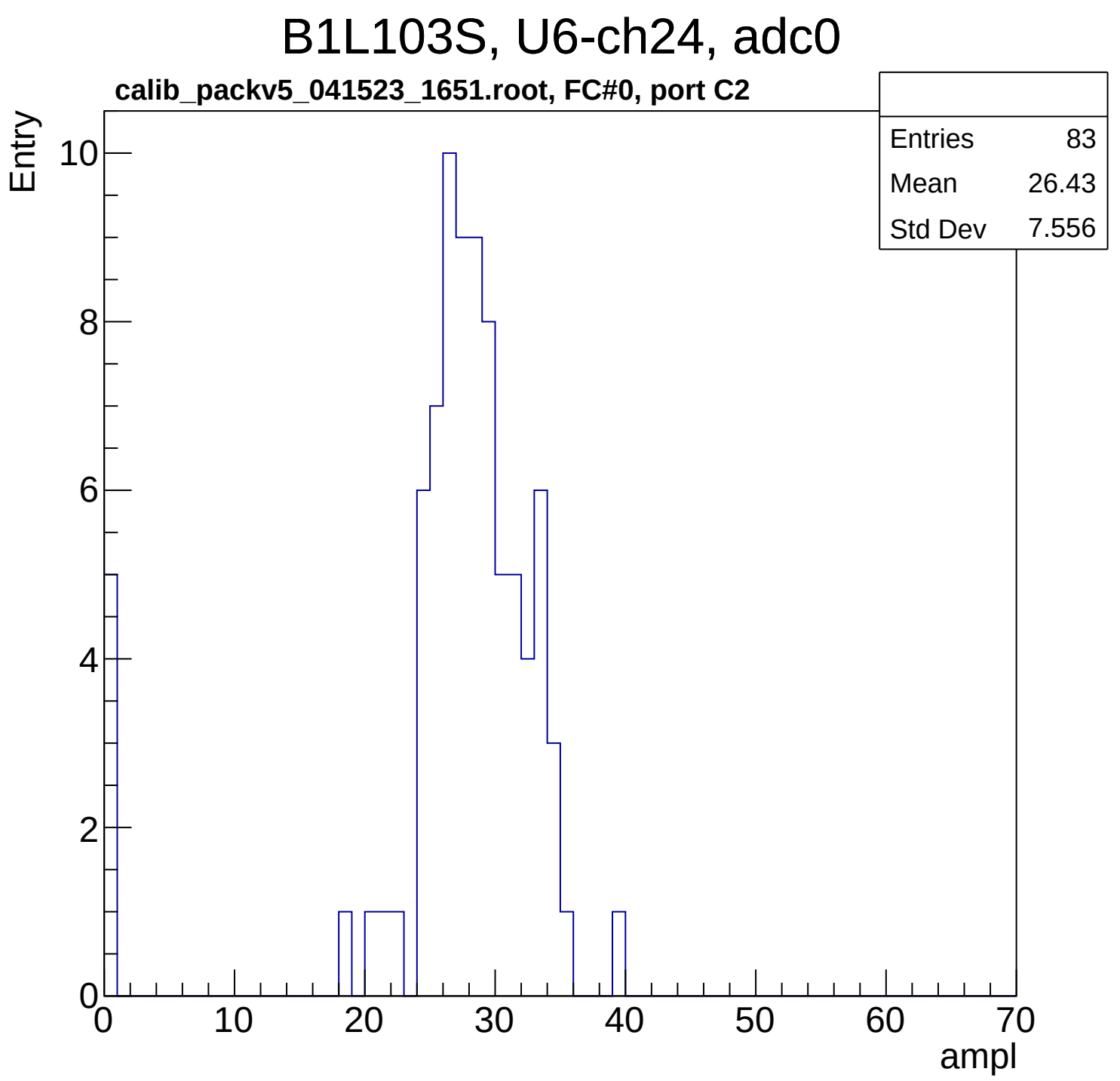
50
60
70
ampl


B1L103S, U6-ch24, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 26.43
Std Dev 7.556
Entry
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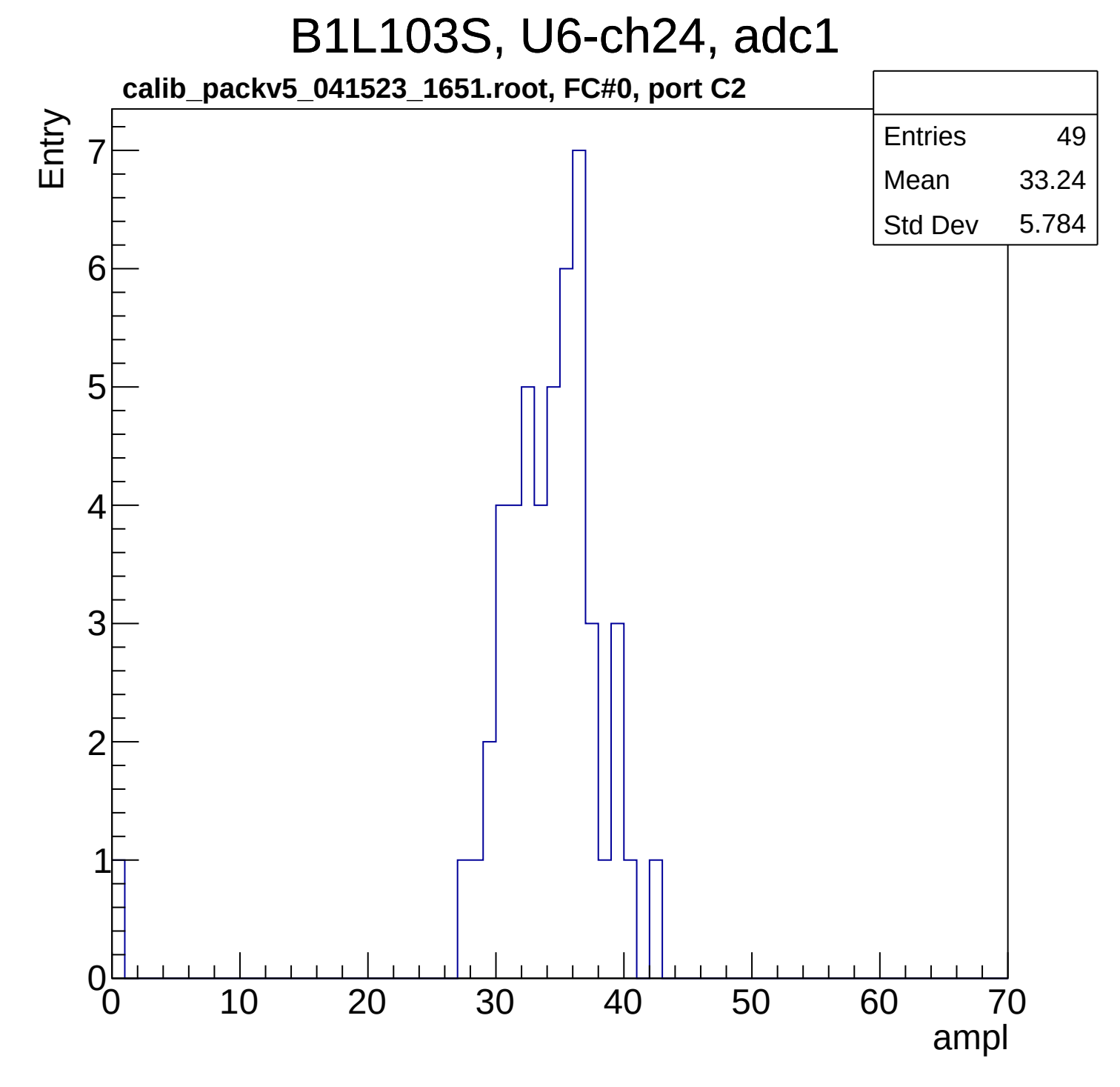
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch24, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 33.24
Std Dev 5.784
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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40
50
60
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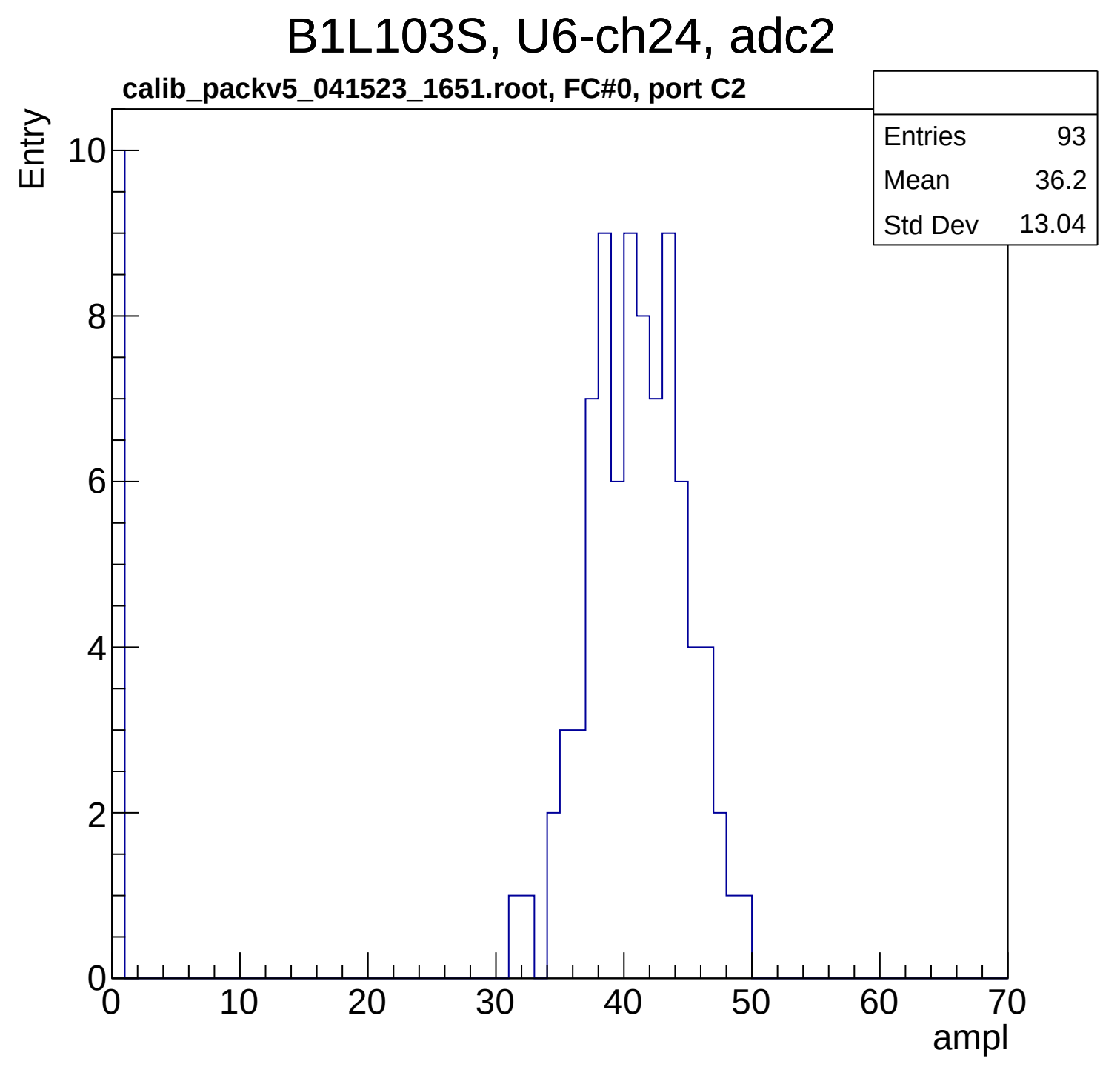
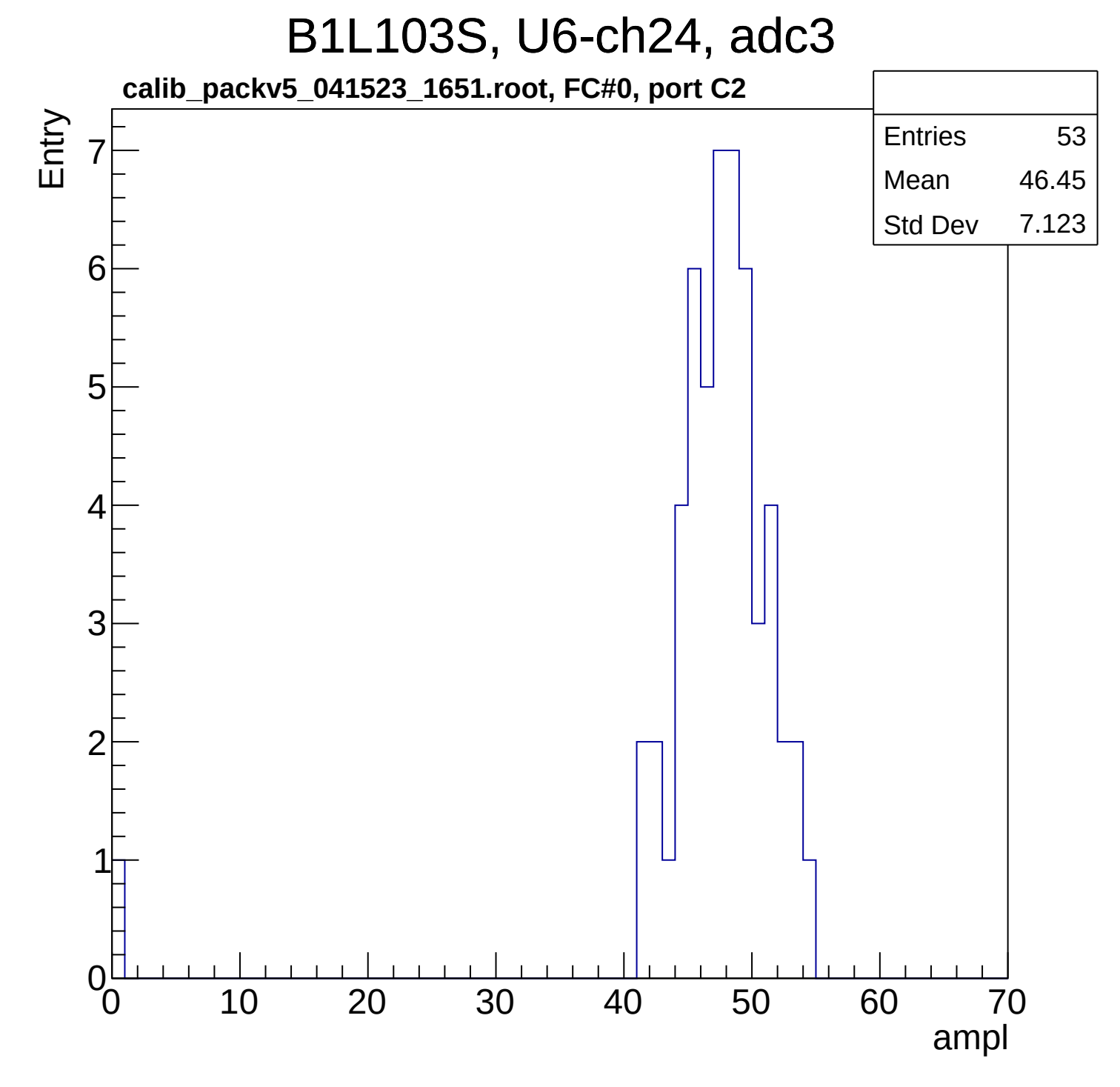
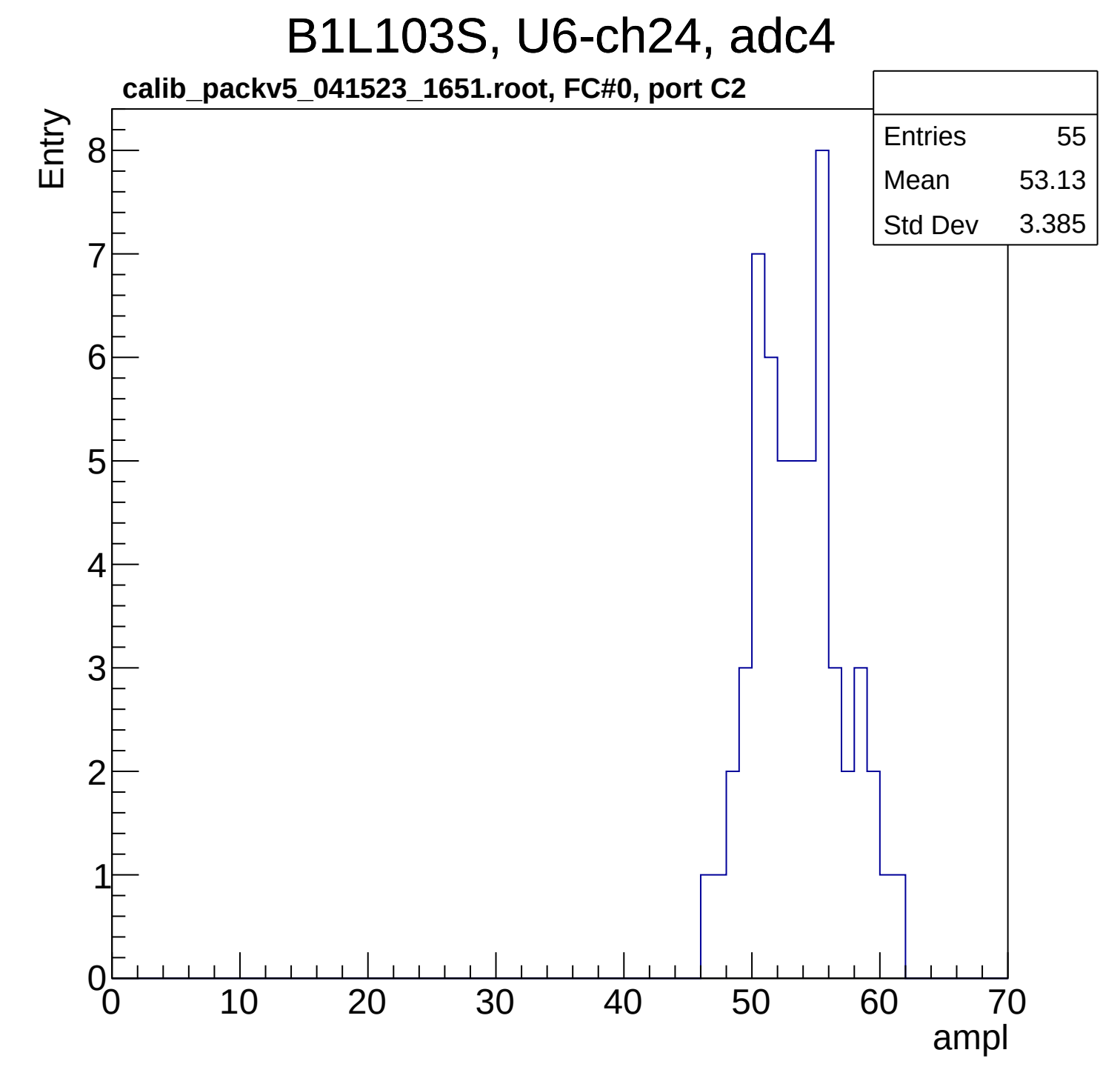

B1L103S, U6-ch24, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 36.2
Std Dev 13.04
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch24, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 46.45
Std Dev 7.123
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U6-ch24, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 53.13
Std Dev 3.385
Entry
ampl
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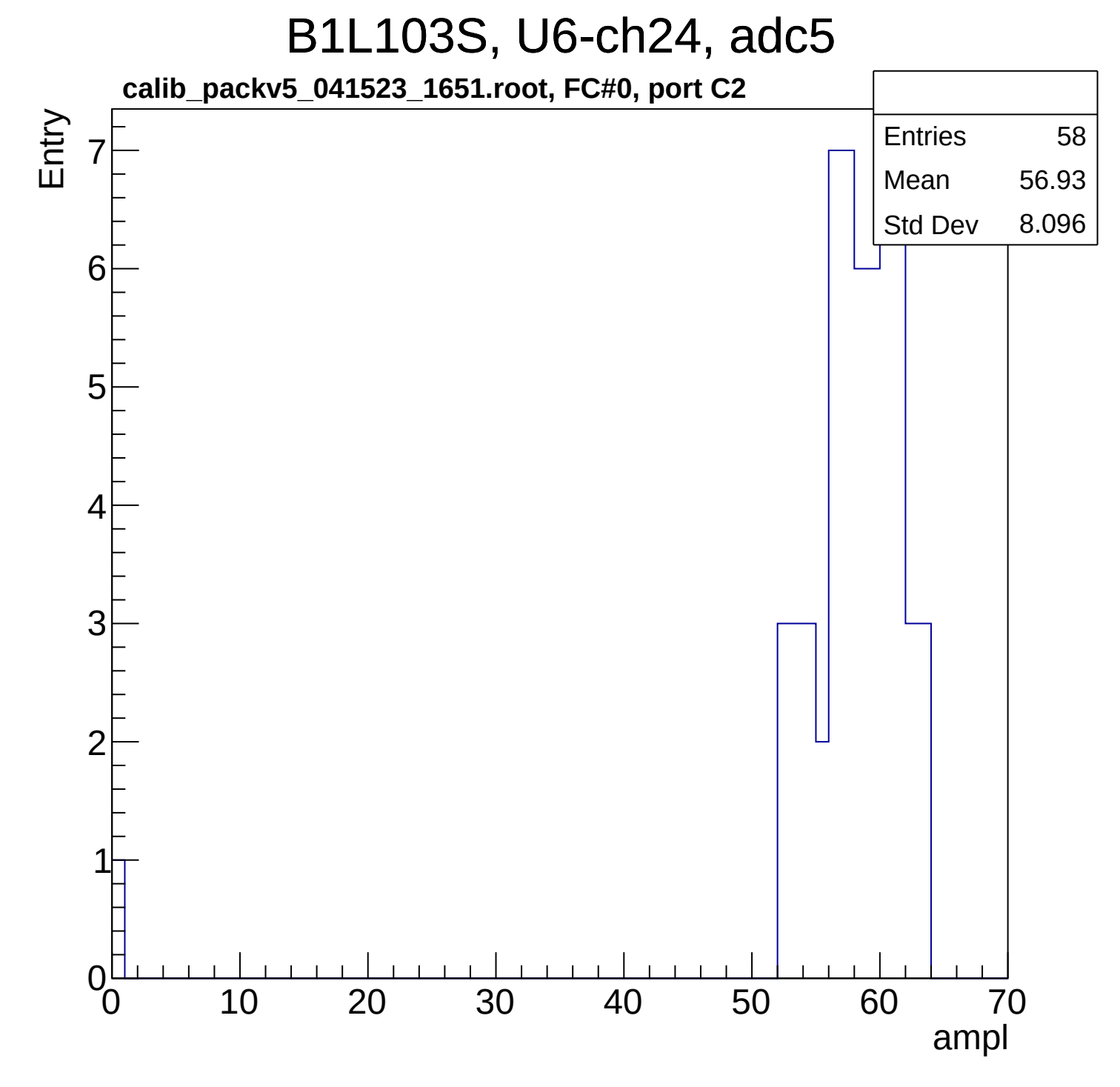
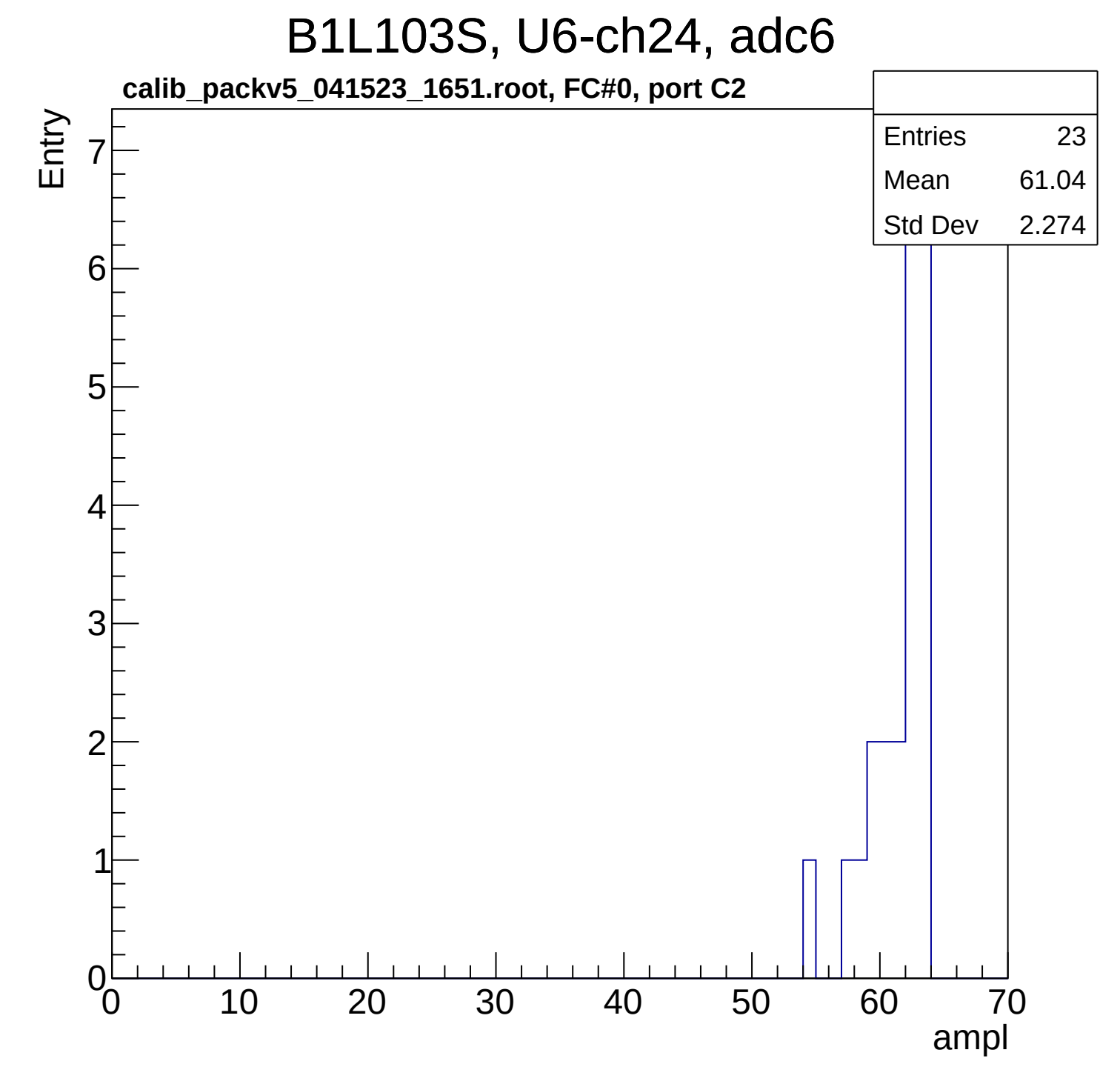
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch24, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 56.93
Std Dev 8.096
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U6-ch24, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 61.04
Std Dev 2.274
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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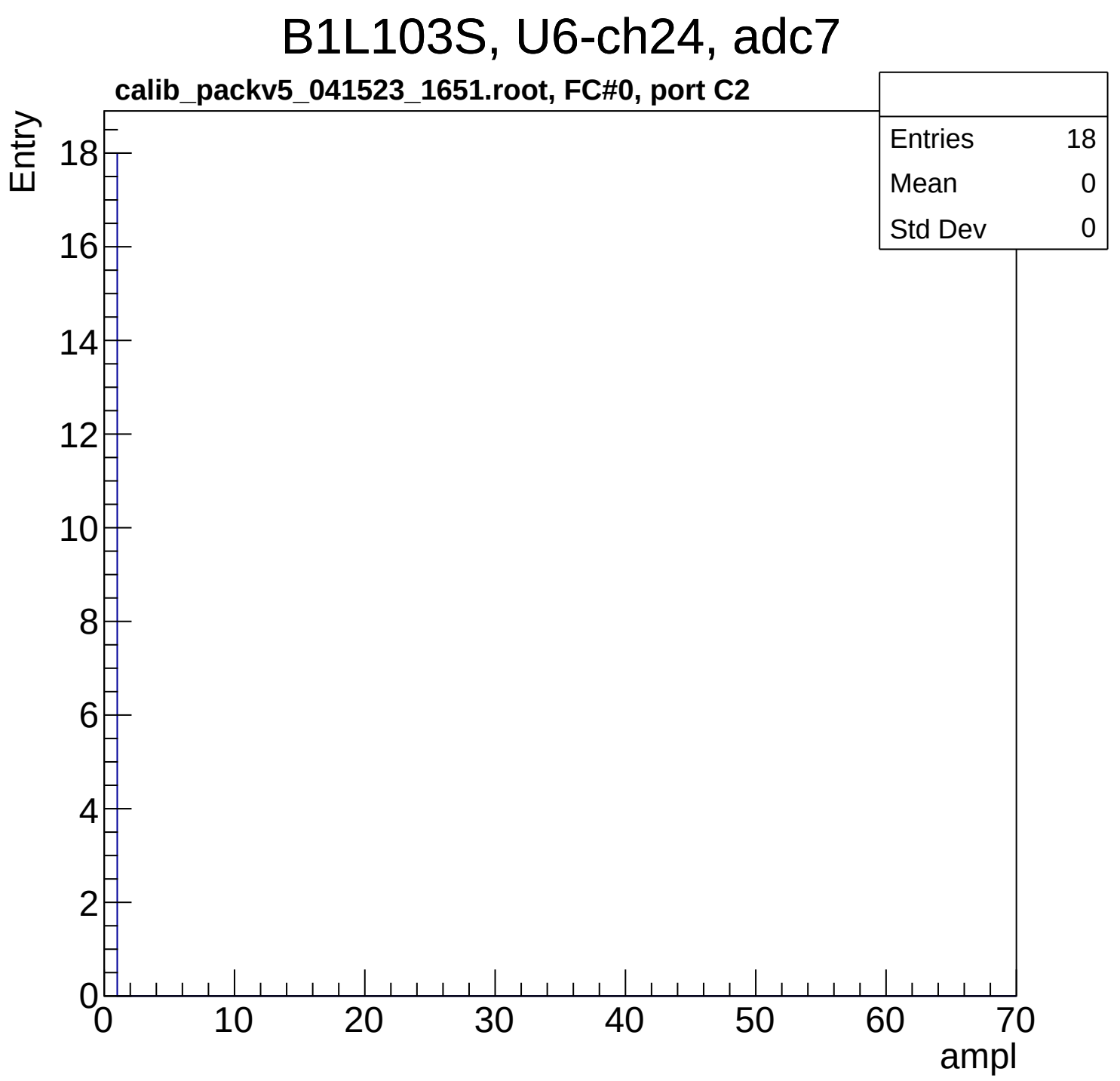
B1L103S, U6-ch24, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
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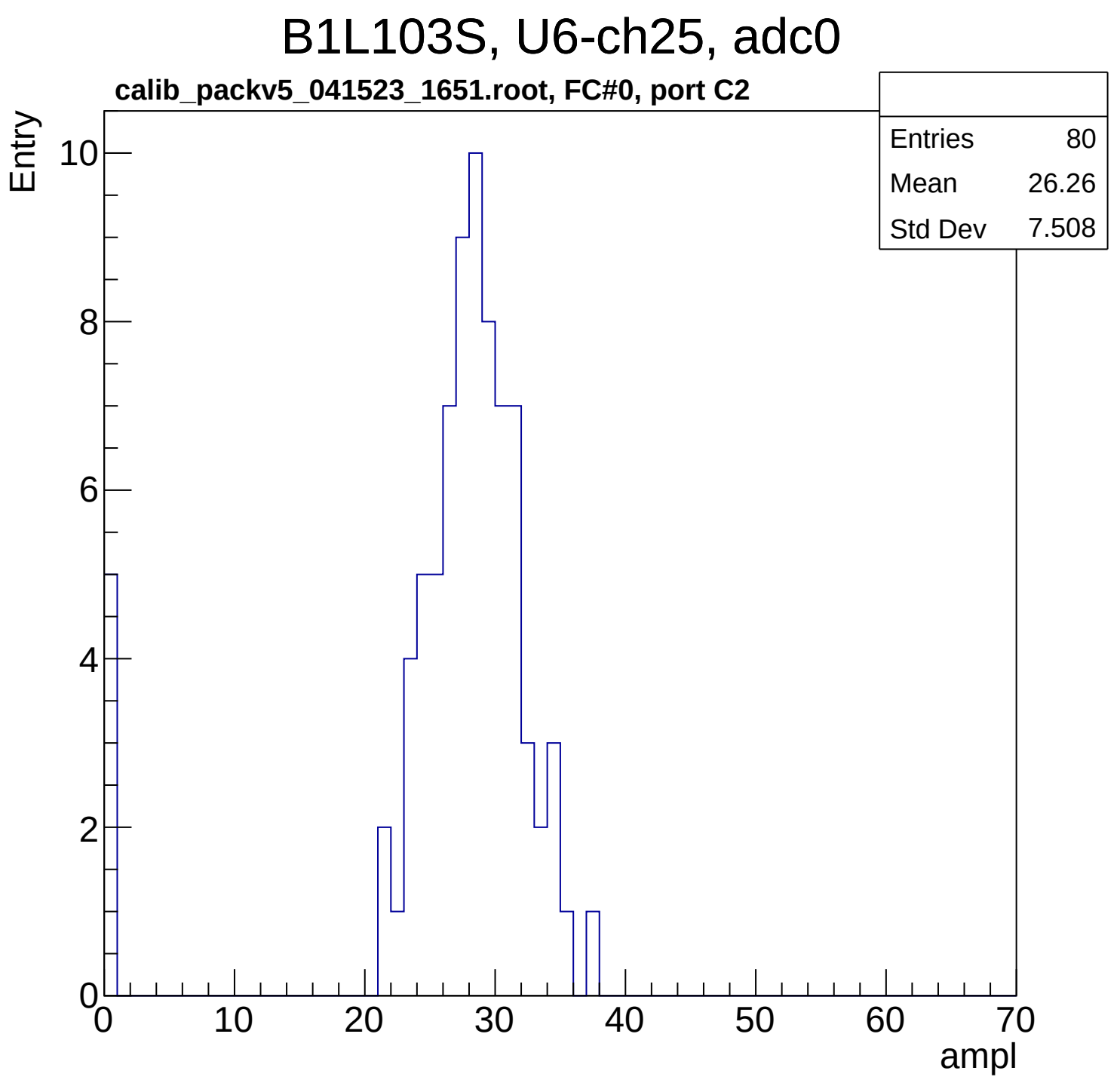
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch25, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 26.26
Std Dev 7.508
Entry
ampl
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2
4
6
8
10
0
10
20
30
40
50
60
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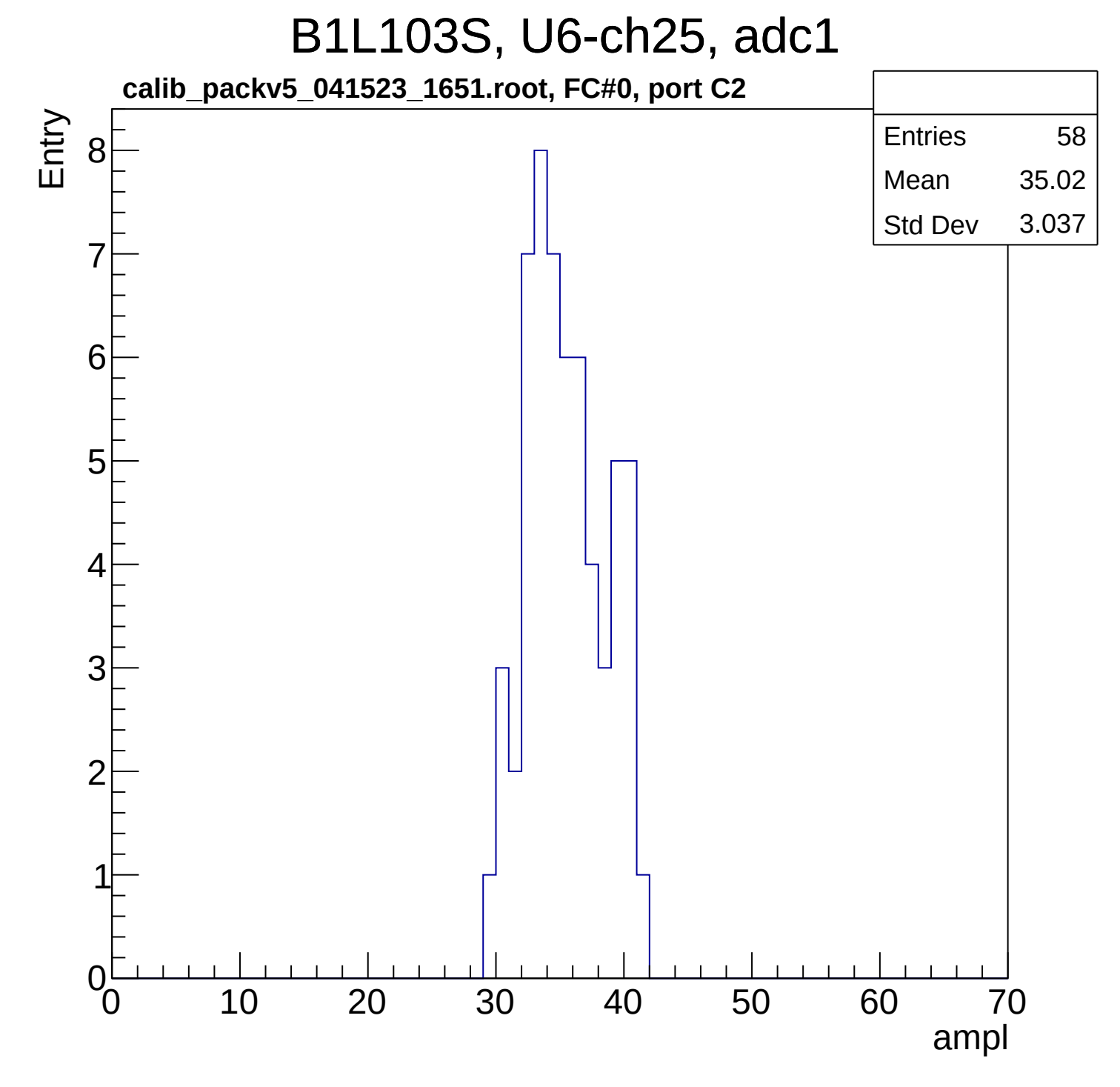
B1L103S, U6-ch25, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 35.02
Std Dev 3.037
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
50
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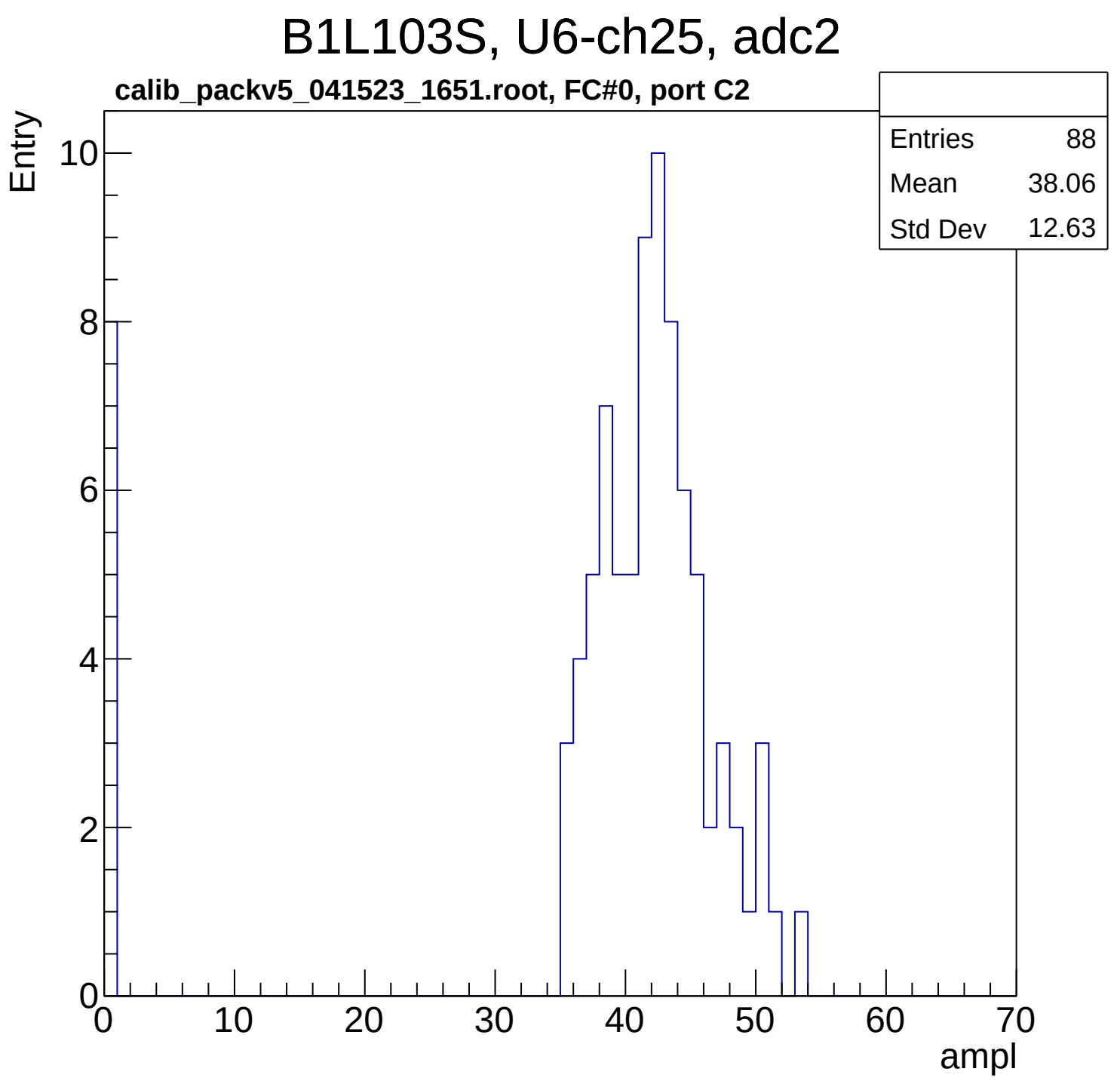
B1L103S, U6-ch25, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 38.06
Std Dev 12.63
Entry
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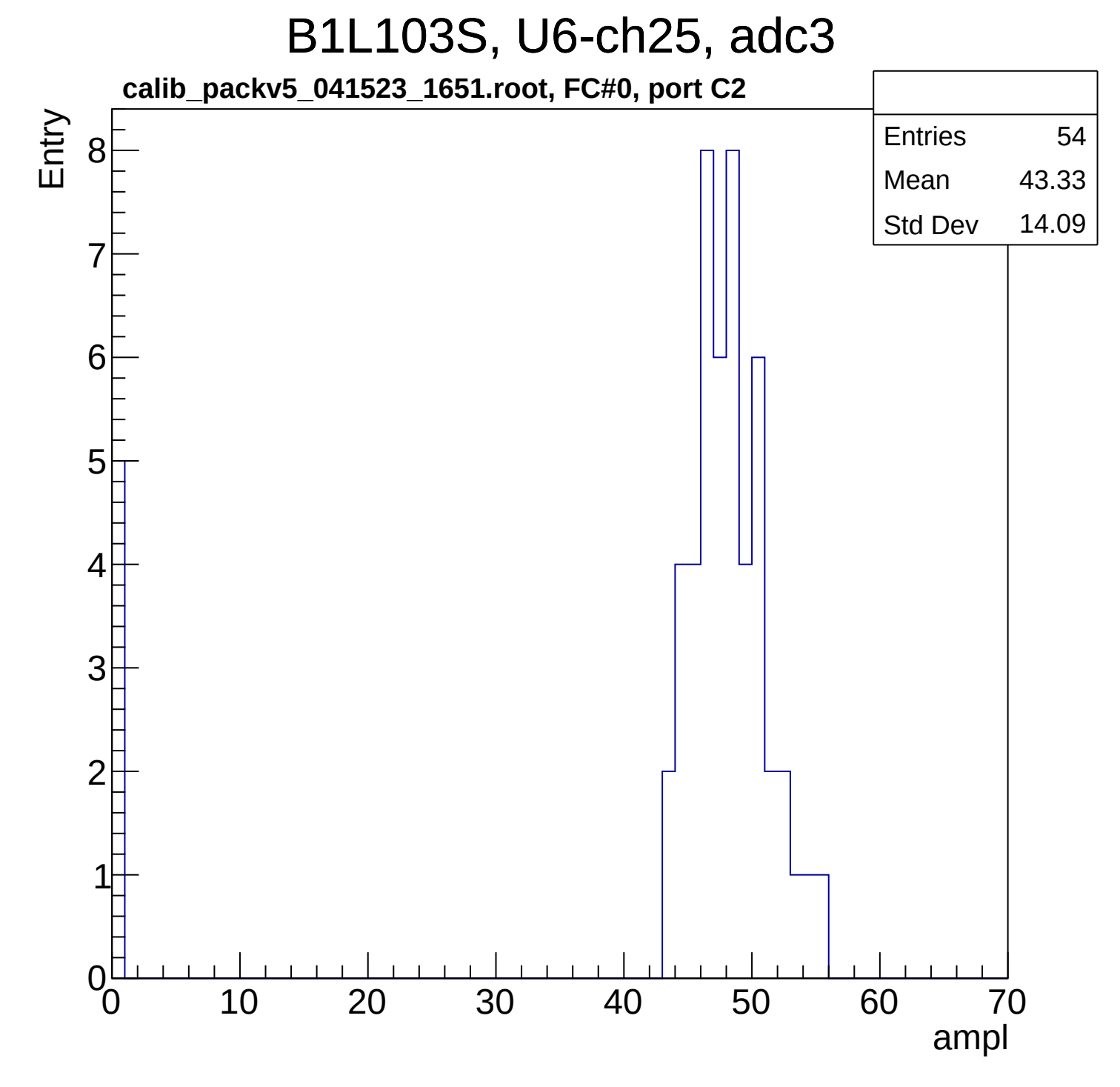
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch25, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 43.33
Std Dev 14.09
Entry
ampl
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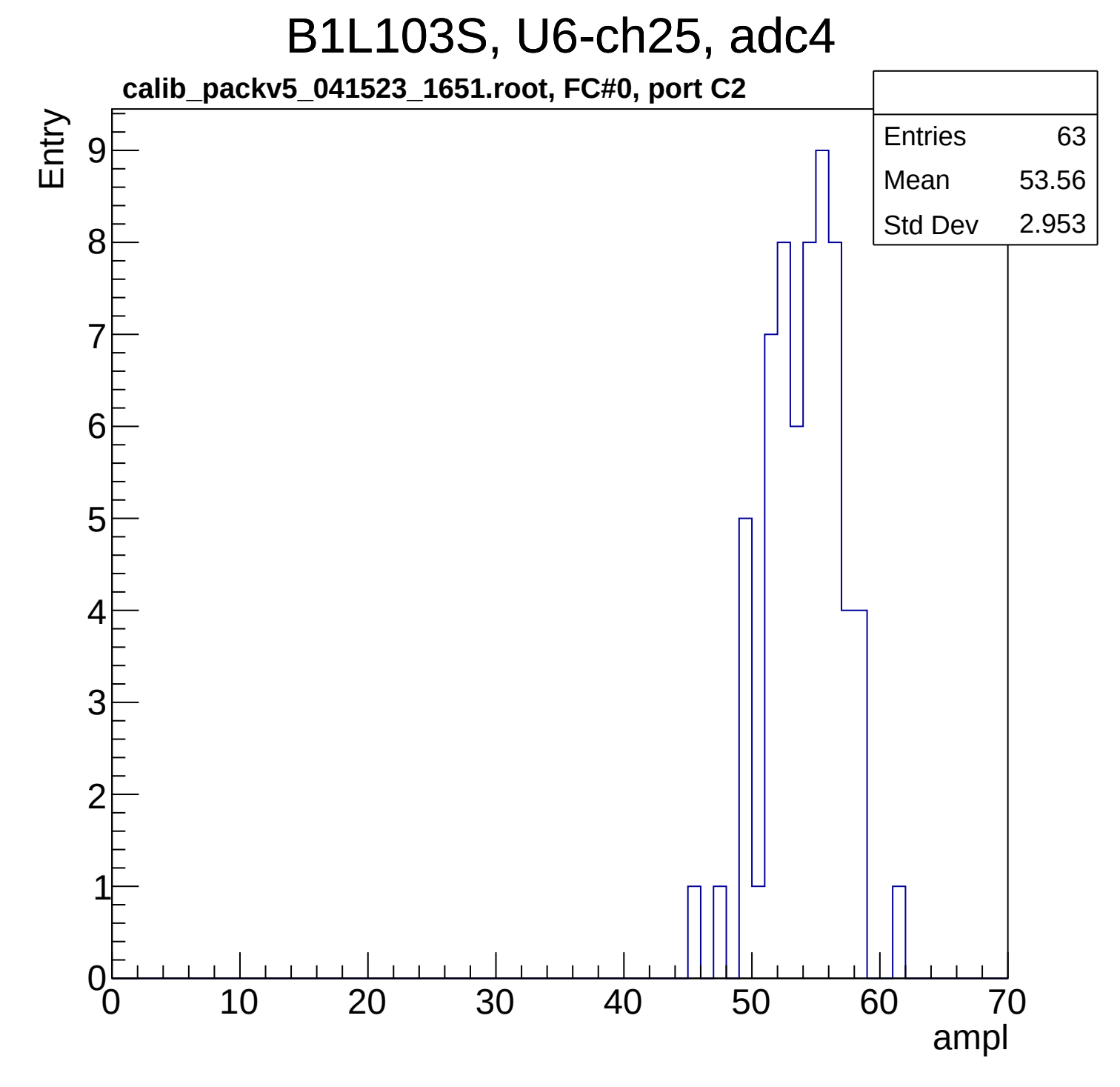
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch25, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 53.56
Std Dev 2.953
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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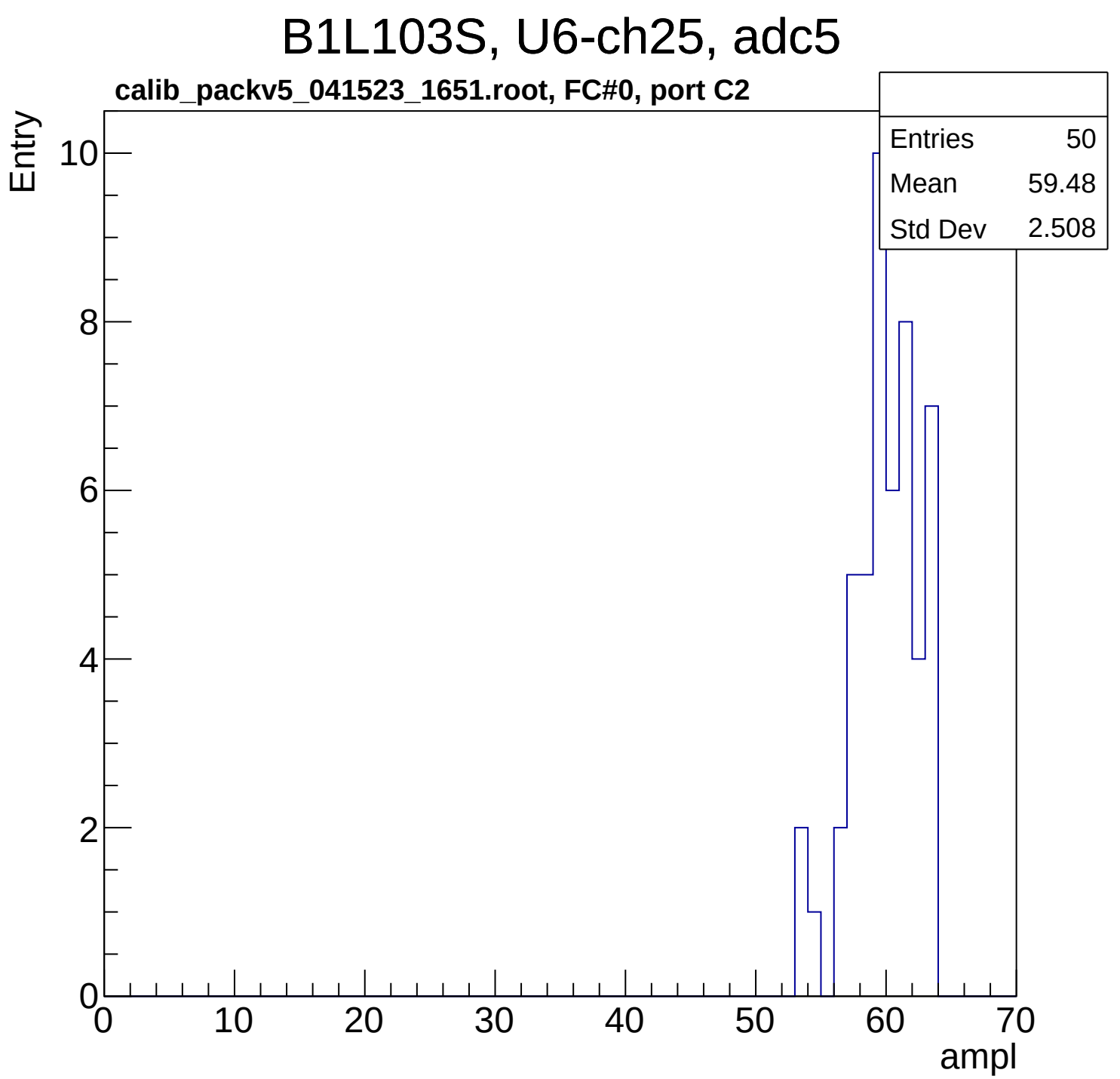
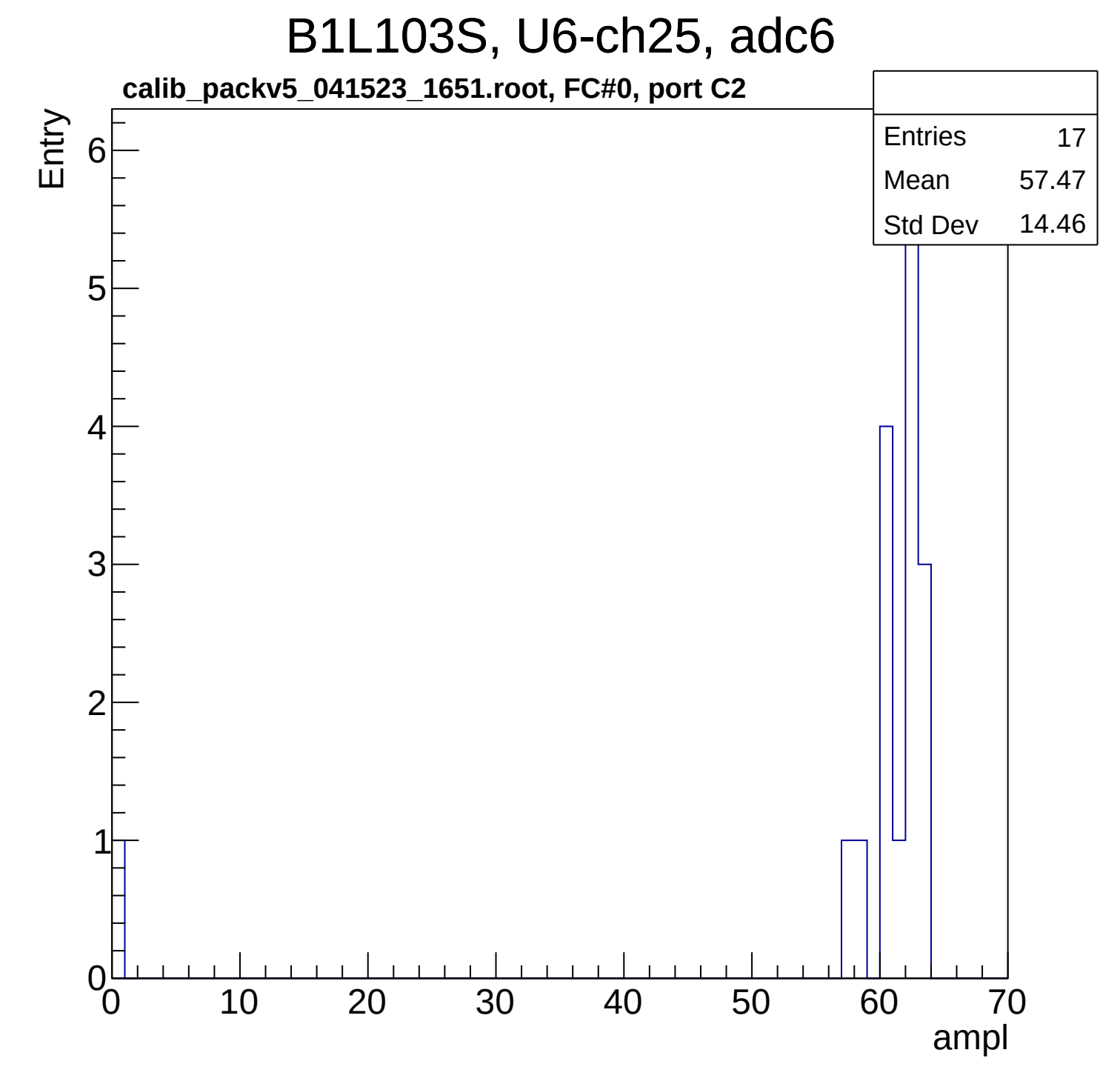
40
50
60
70


B1L103S, U6-ch25, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 59.48
Std Dev 2.508
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch25, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 57.47
Std Dev 14.46
Entry
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2
3
4
5
6
0
10
20
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50
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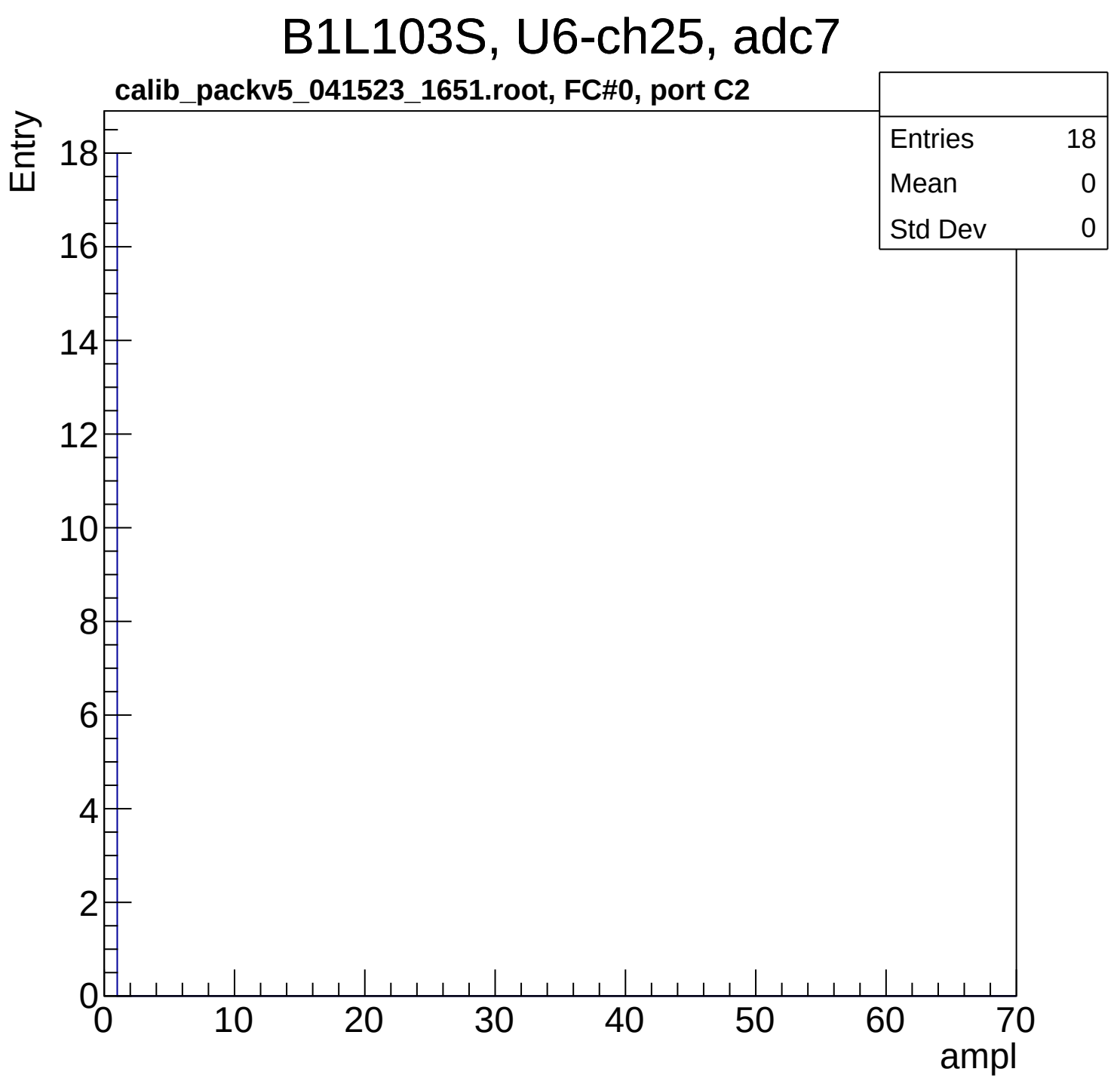
70
ampl


B1L103S, U6-ch25, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
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6
8
10
12
14
16
18
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10
20
30
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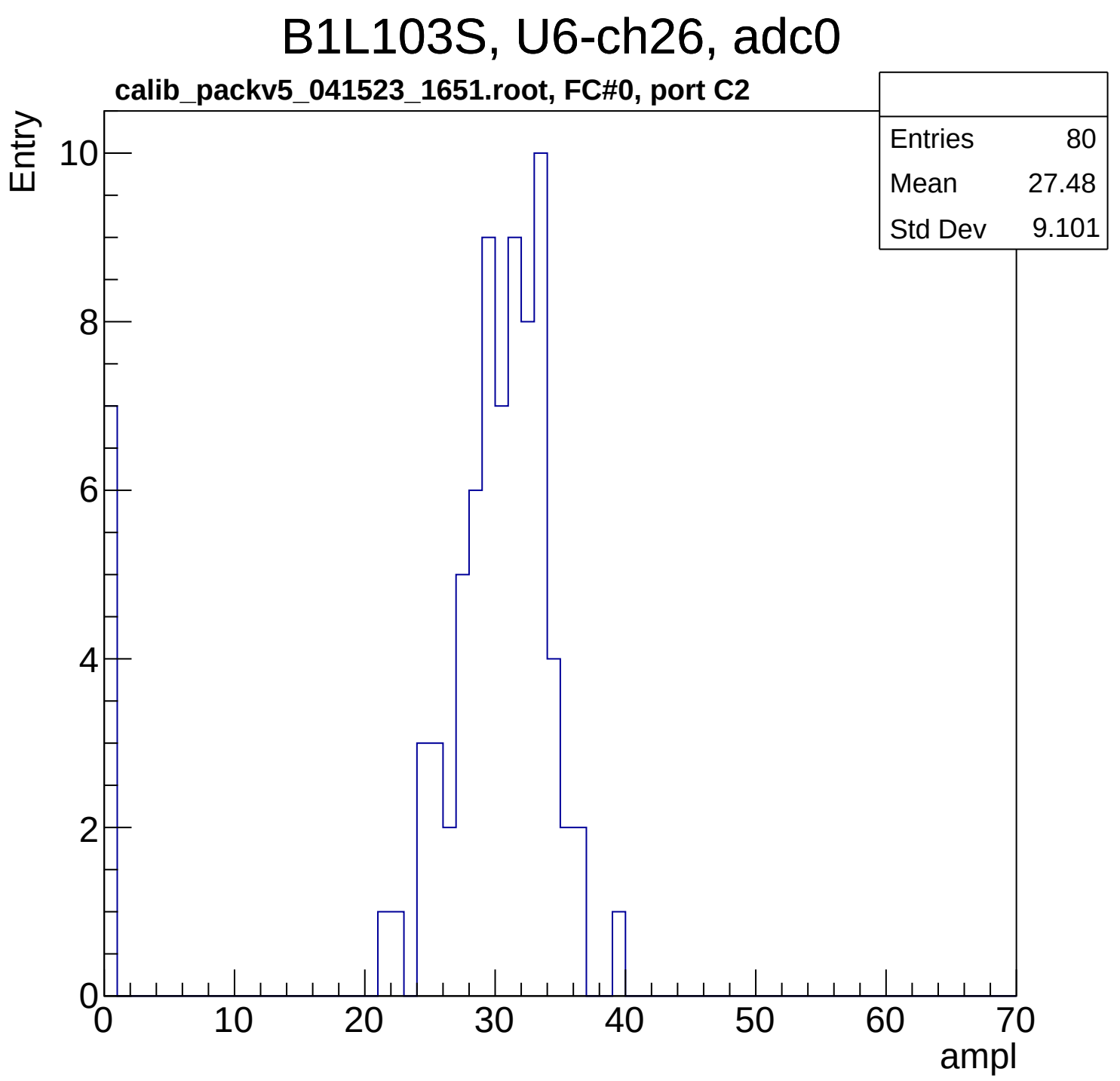
50
60
70
ampl


B1L103S, U6-ch26, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 27.48
Std Dev 9.101
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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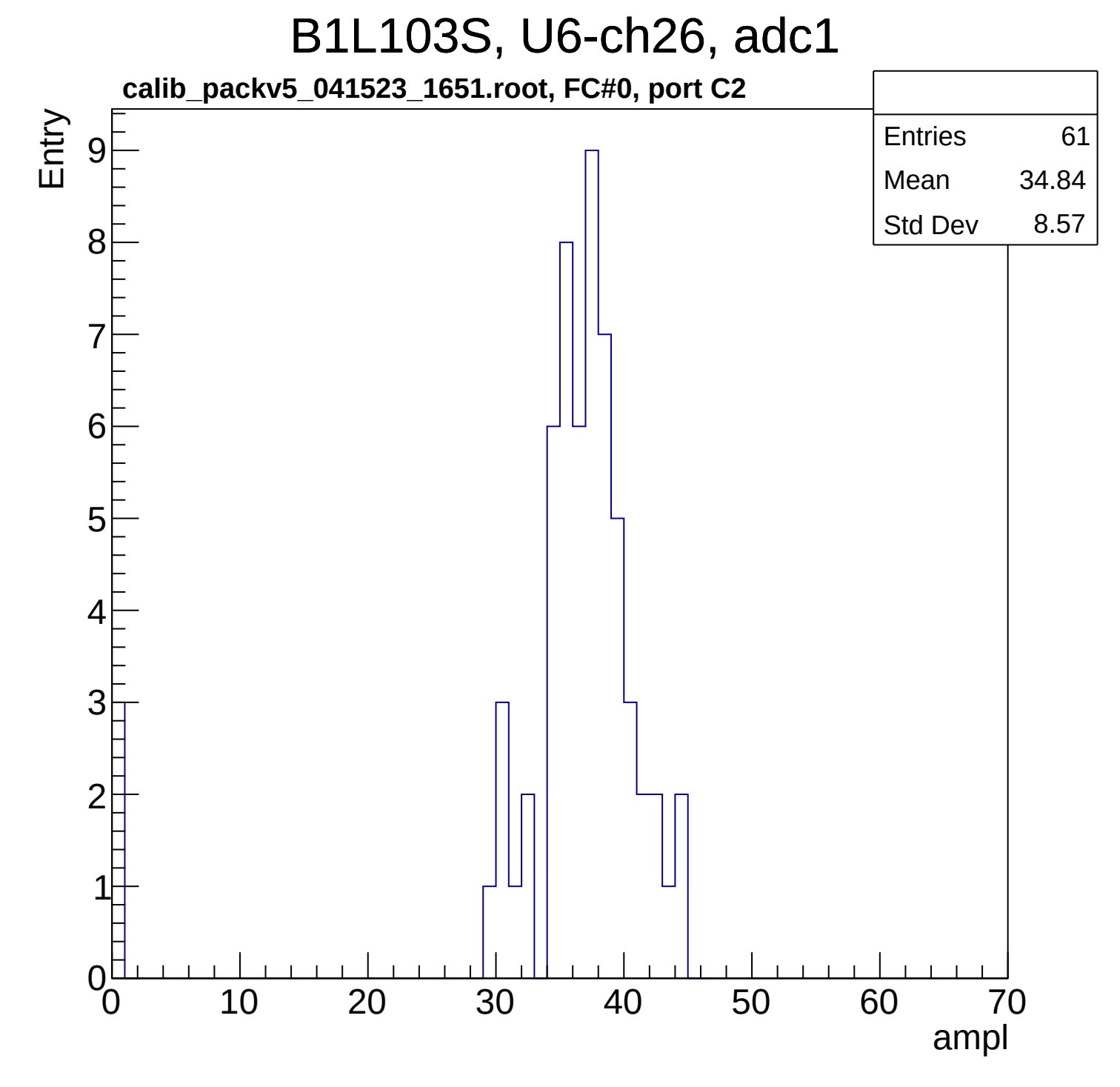
B1L103S, U6-ch26, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 34.84
Std Dev 8.57
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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60
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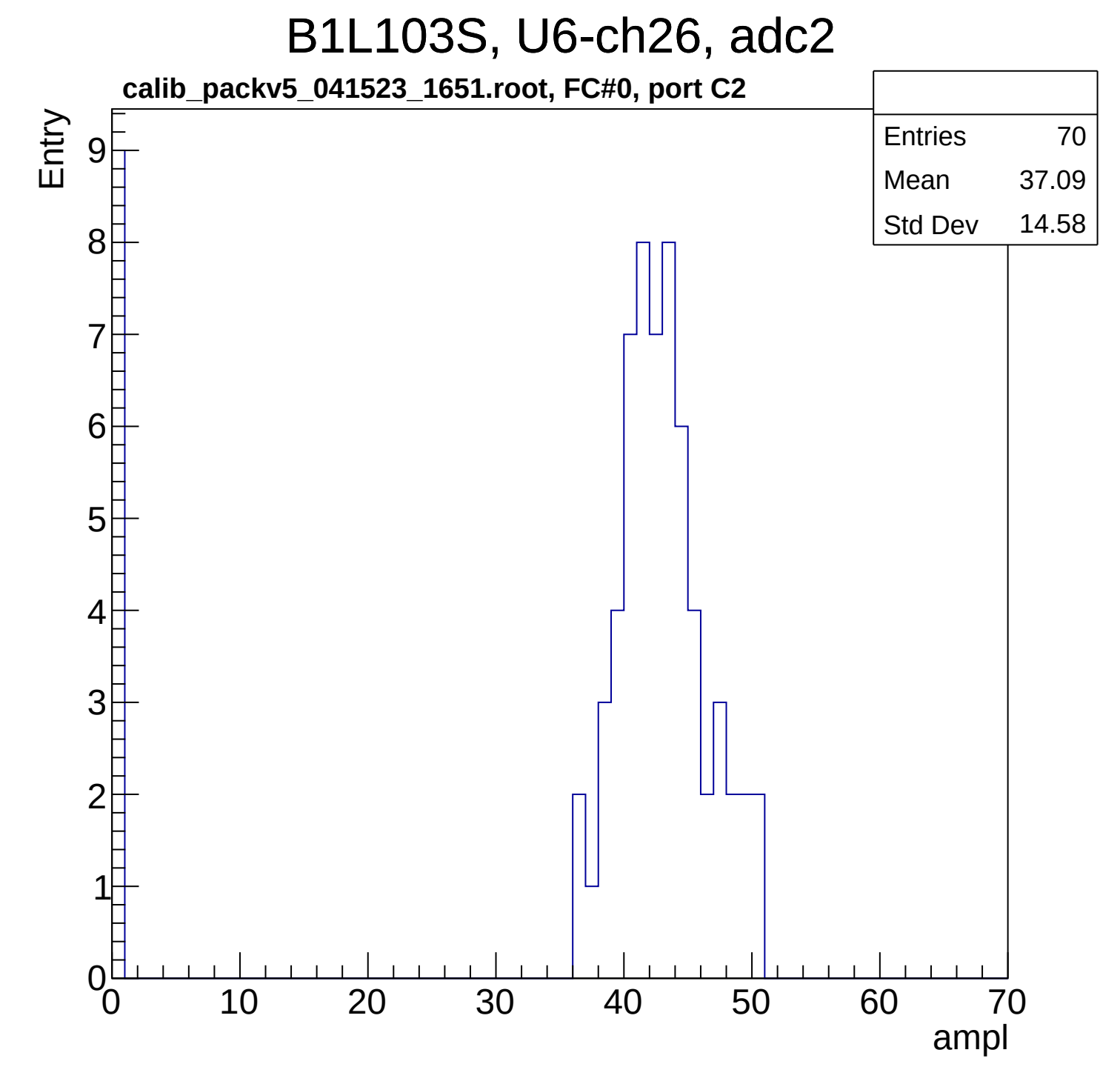
B1L103S, U6-ch26, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 37.09
Std Dev 14.58
Entry
ampl
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2
3
4
5
6
7
8
9
0
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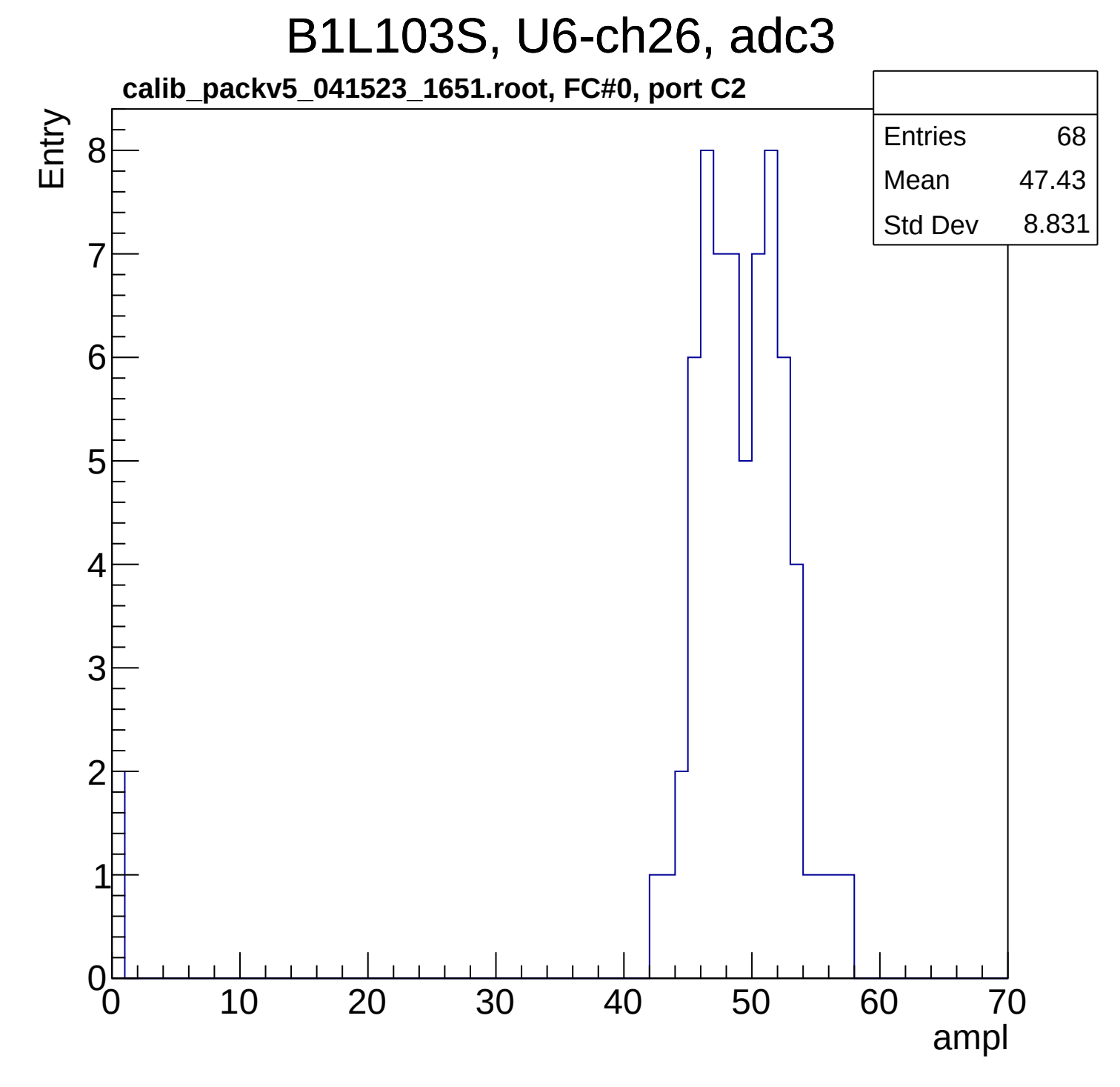
B1L103S, U6-ch26, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 47.43
Std Dev 8.831
Entry
ampl
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2
3
4
5
6
7
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0
10
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40
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60
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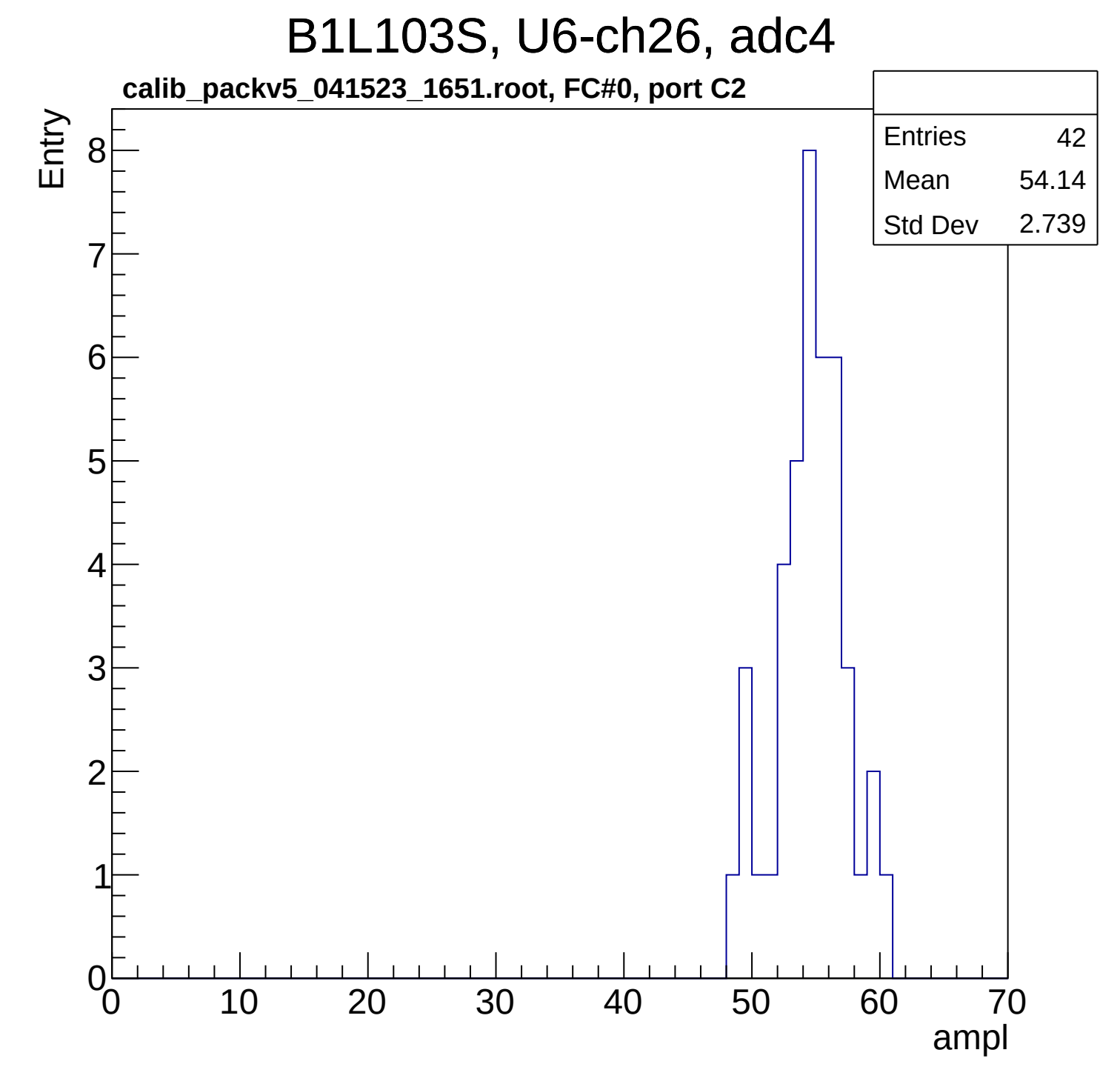
B1L103S, U6-ch26, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 54.14
Std Dev 2.739
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
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60
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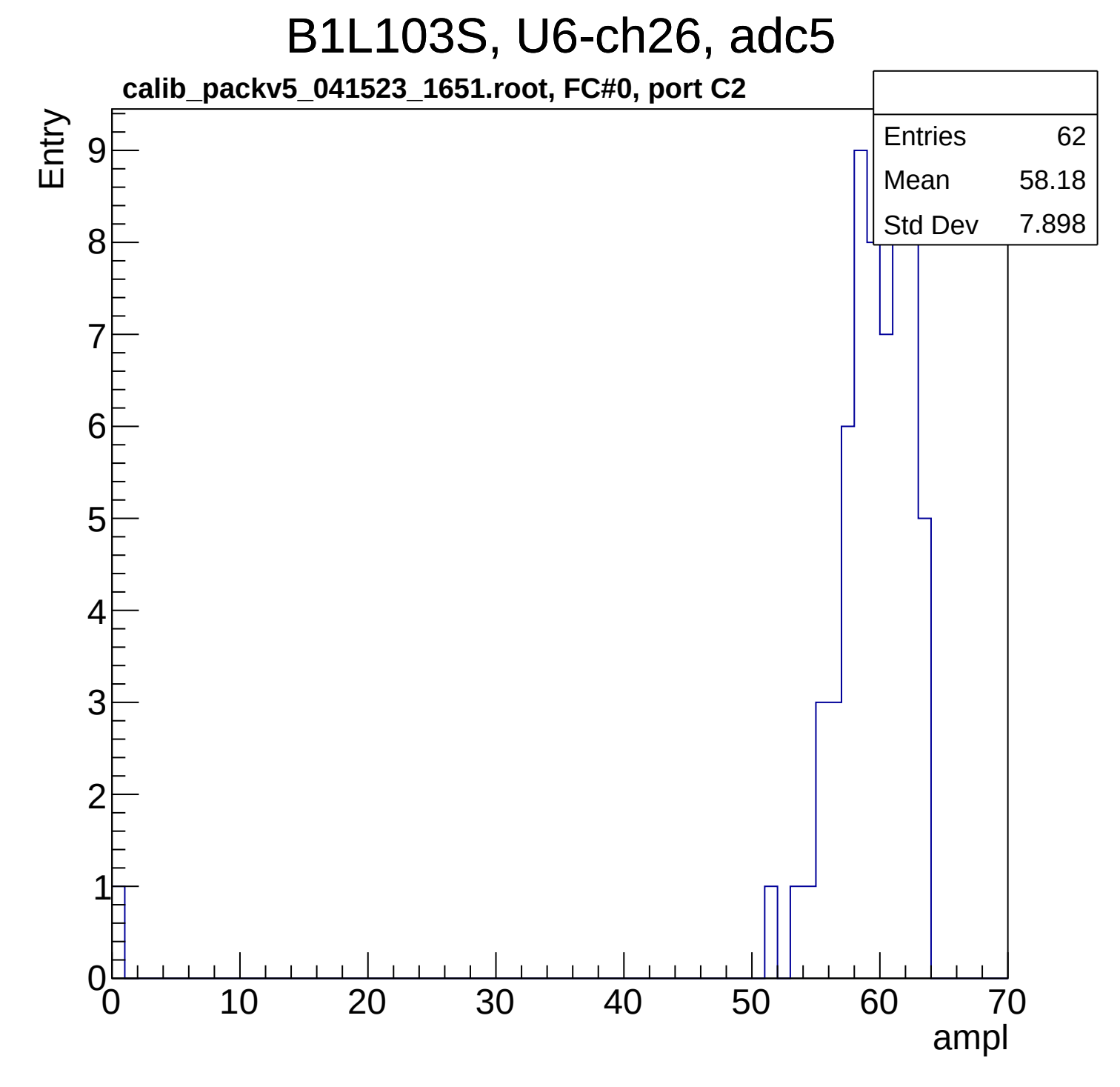
B1L103S, U6-ch26, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 58.18
Std Dev 7.898
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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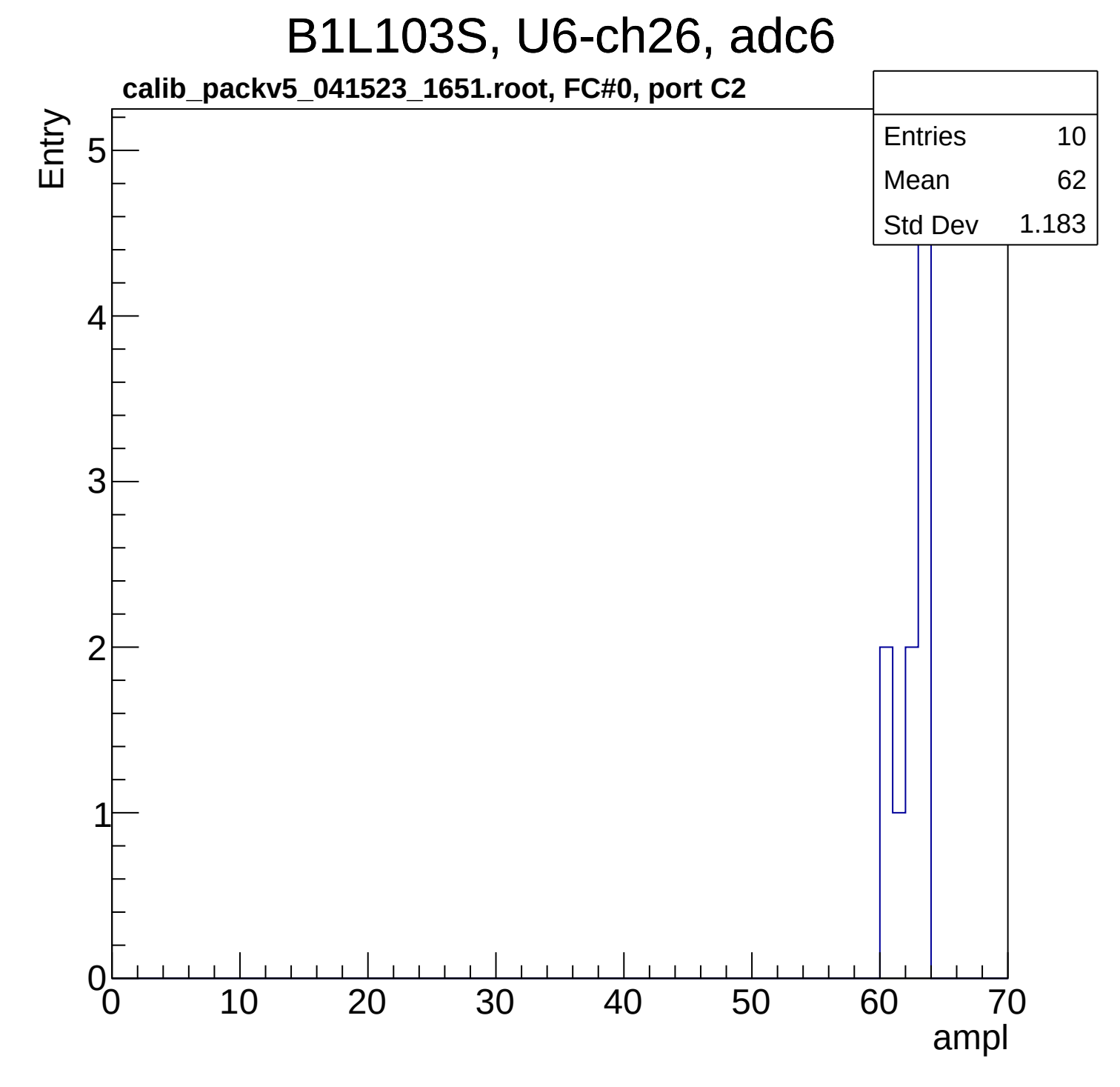
60
70


B1L103S, U6-ch26, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 62
Std Dev 1.183
Entry
ampl
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1
2
3
4
5
0
10
20
30
40
50
60
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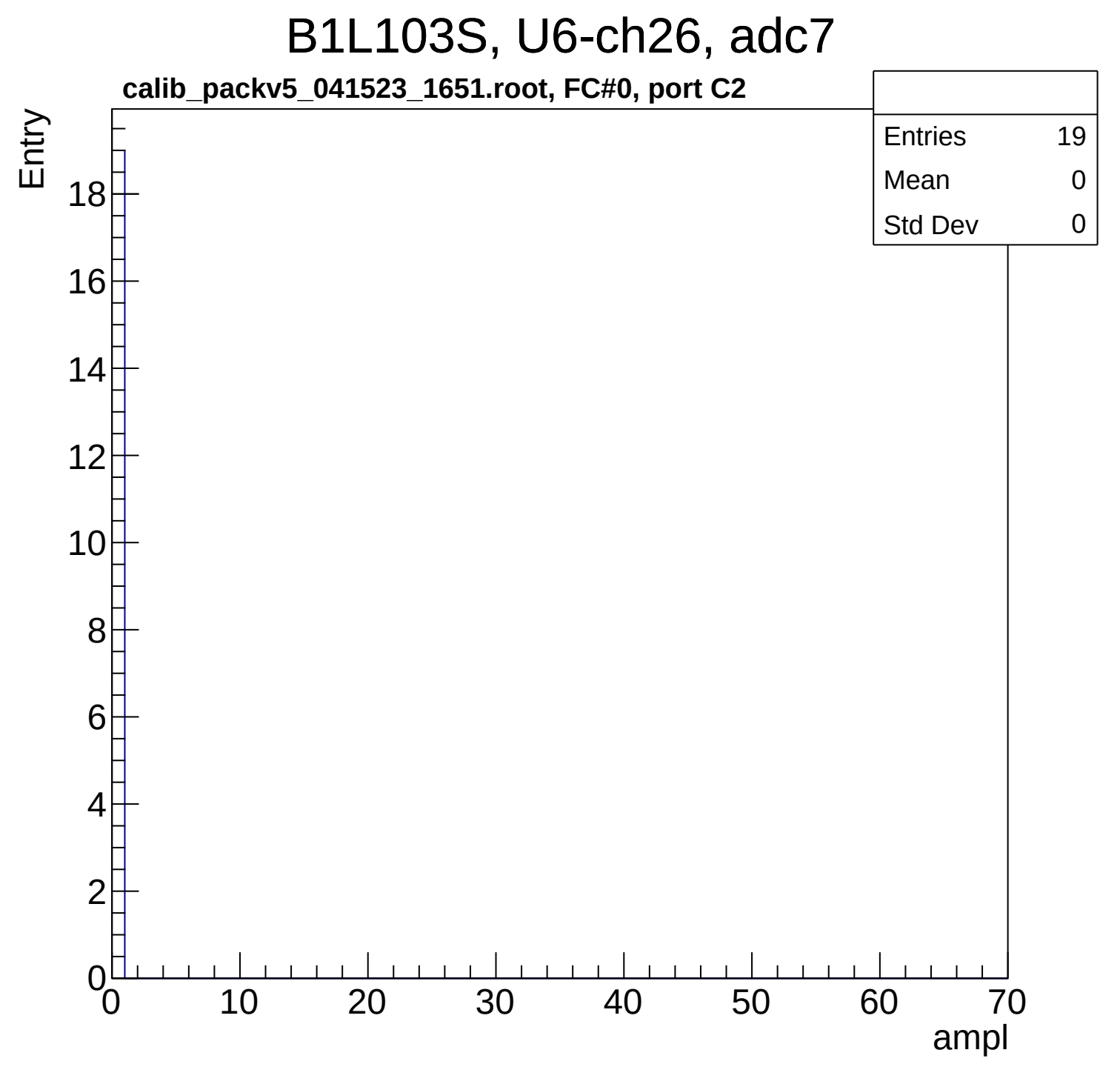
B1L103S, U6-ch26, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
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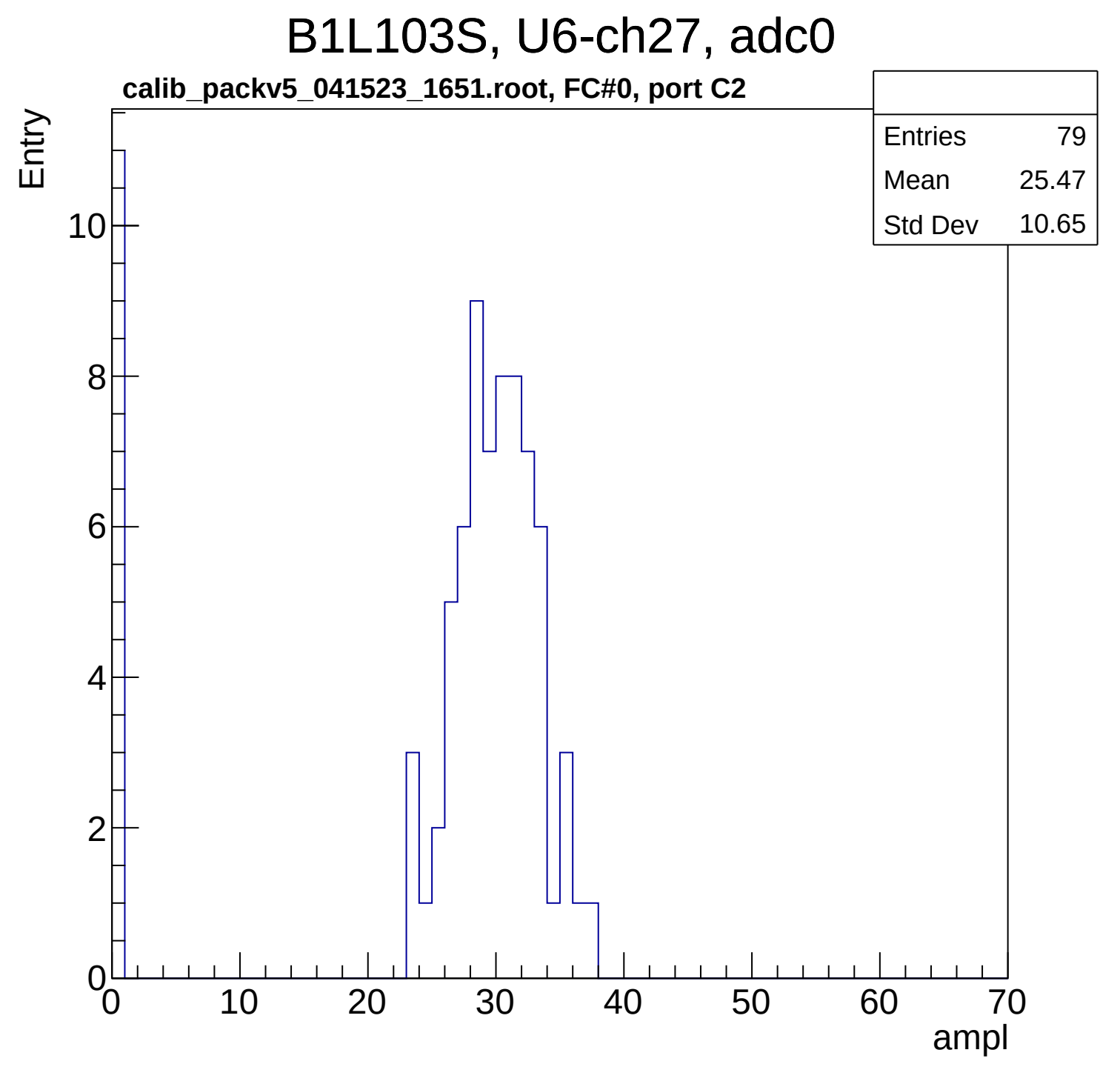
70
ampl


B1L103S, U6-ch27, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 25.47
Std Dev 10.65
Entry
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10
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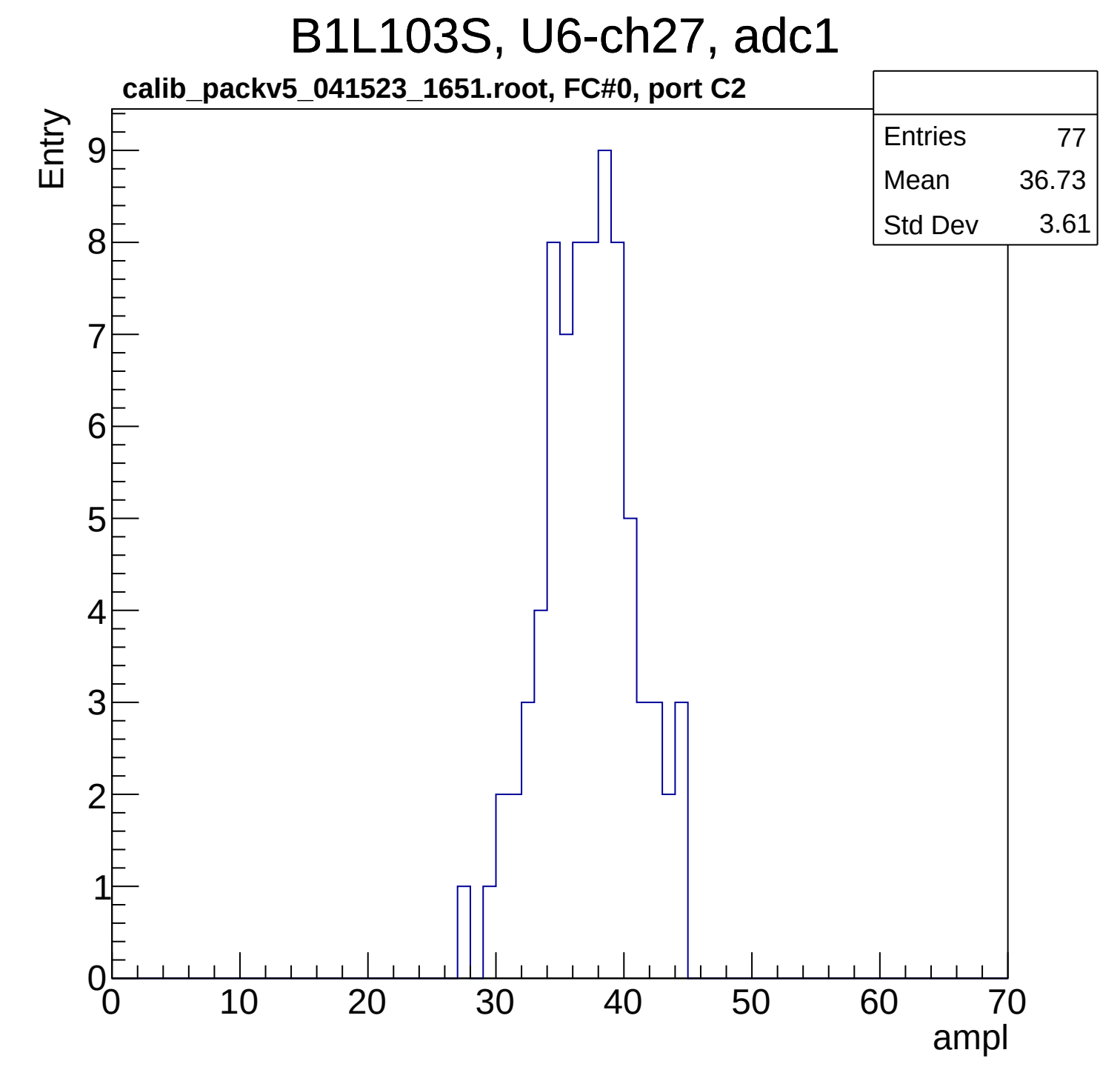
20
30
40
50
60
70
ampl


B1L103S, U6-ch27, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 36.73
Std Dev 3.61
Entry
ampl
0
1
2
3
4
5
6
7
8
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0
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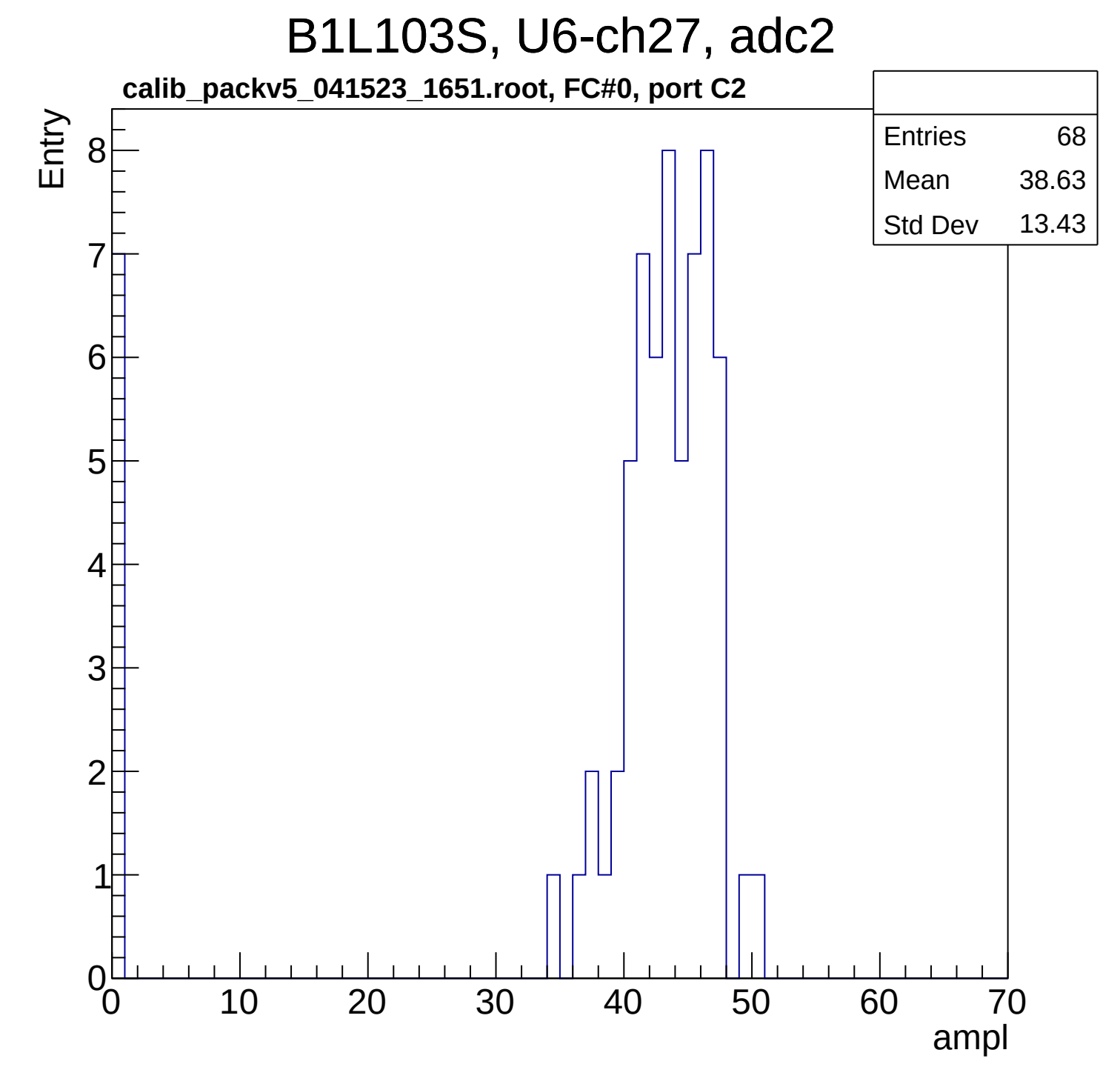
40
50
60
70


B1L103S, U6-ch27, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 38.63
Std Dev 13.43
Entry
ampl
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2
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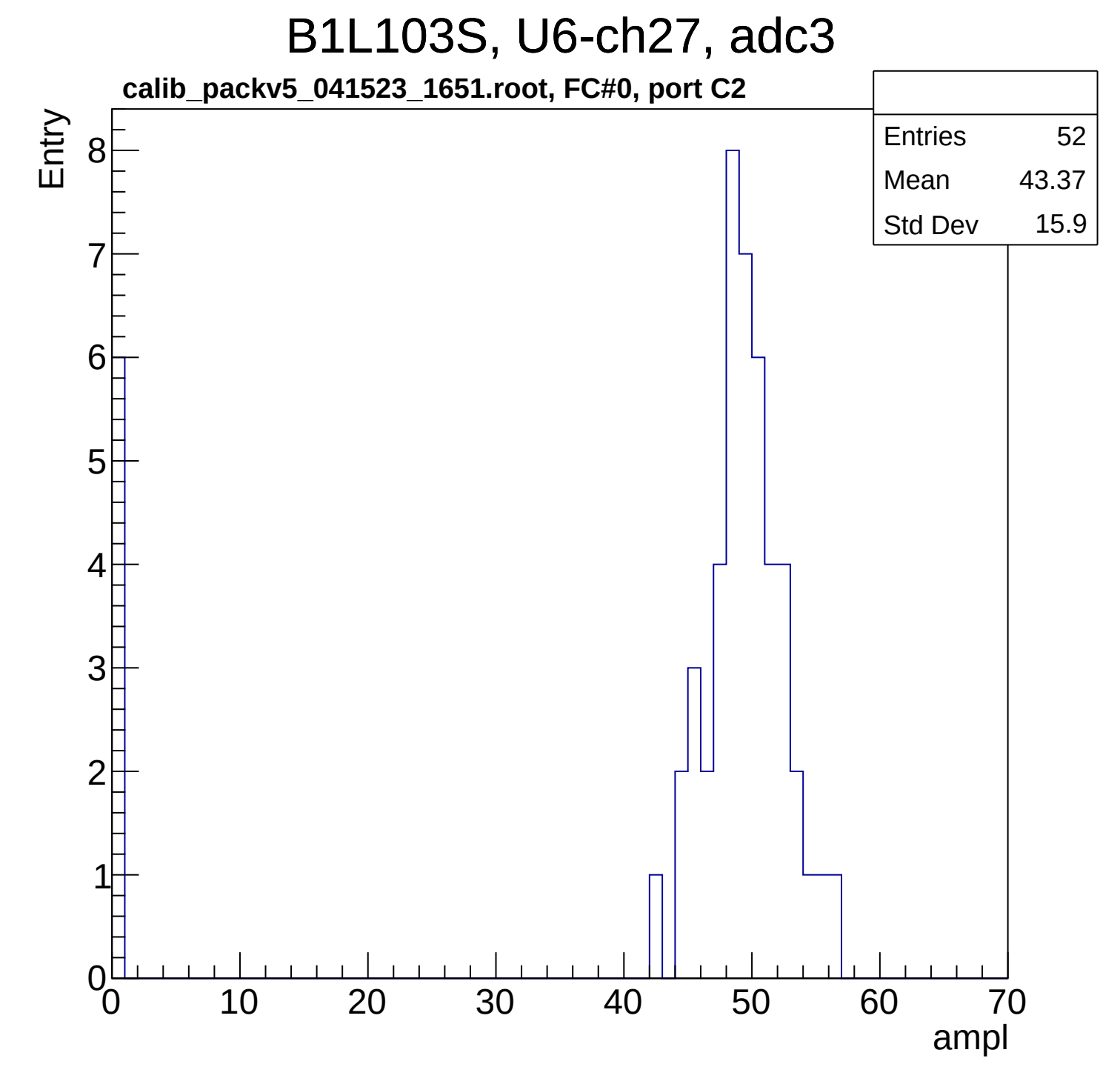
B1L103S, U6-ch27, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 43.37
Std Dev 15.9
Entry
ampl
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2
3
4
5
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7
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0
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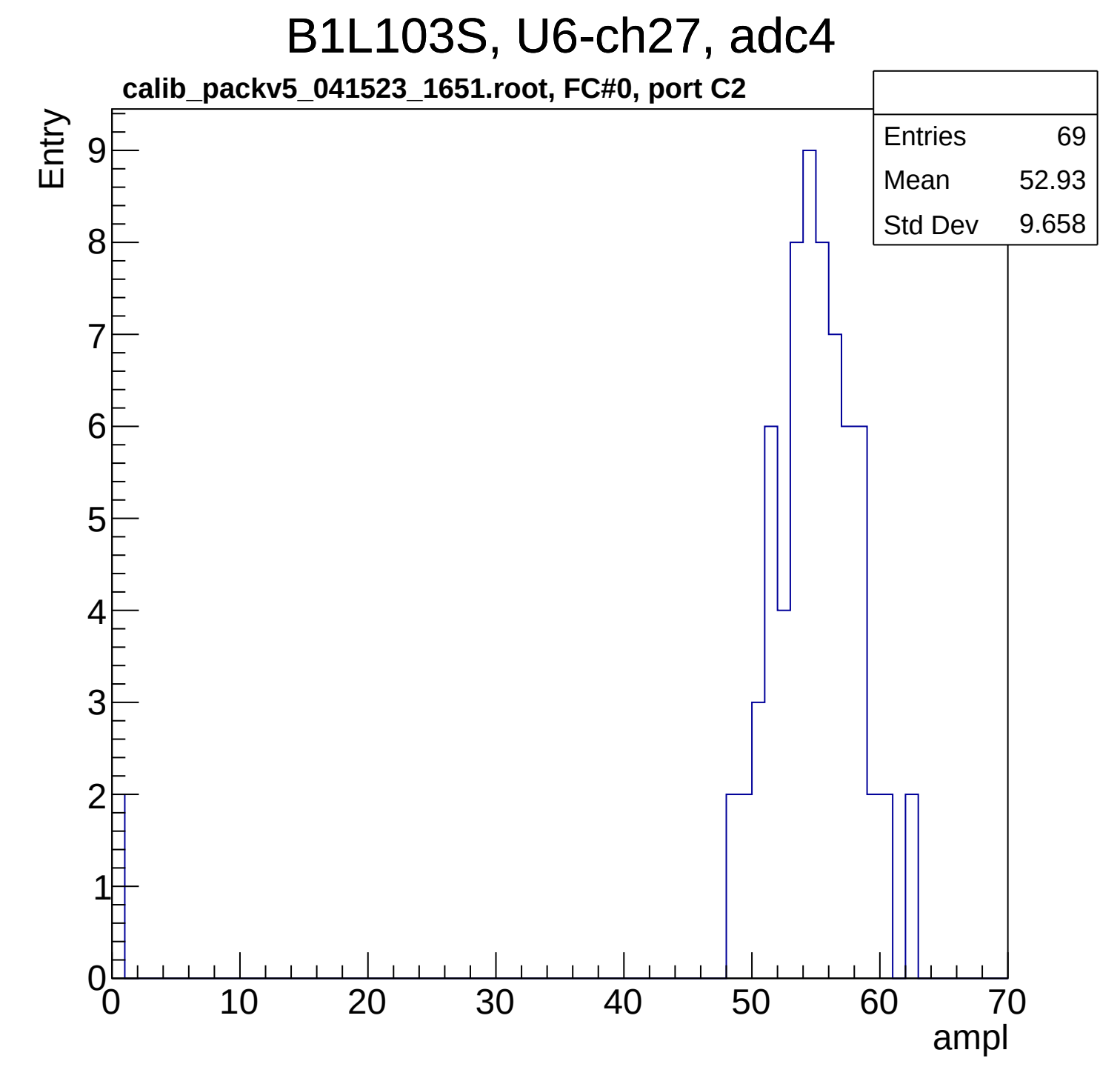
B1L103S, U6-ch27, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 52.93
Std Dev 9.658
Entry
ampl
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2
3
4
5
6
7
8
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0
10
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40
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60
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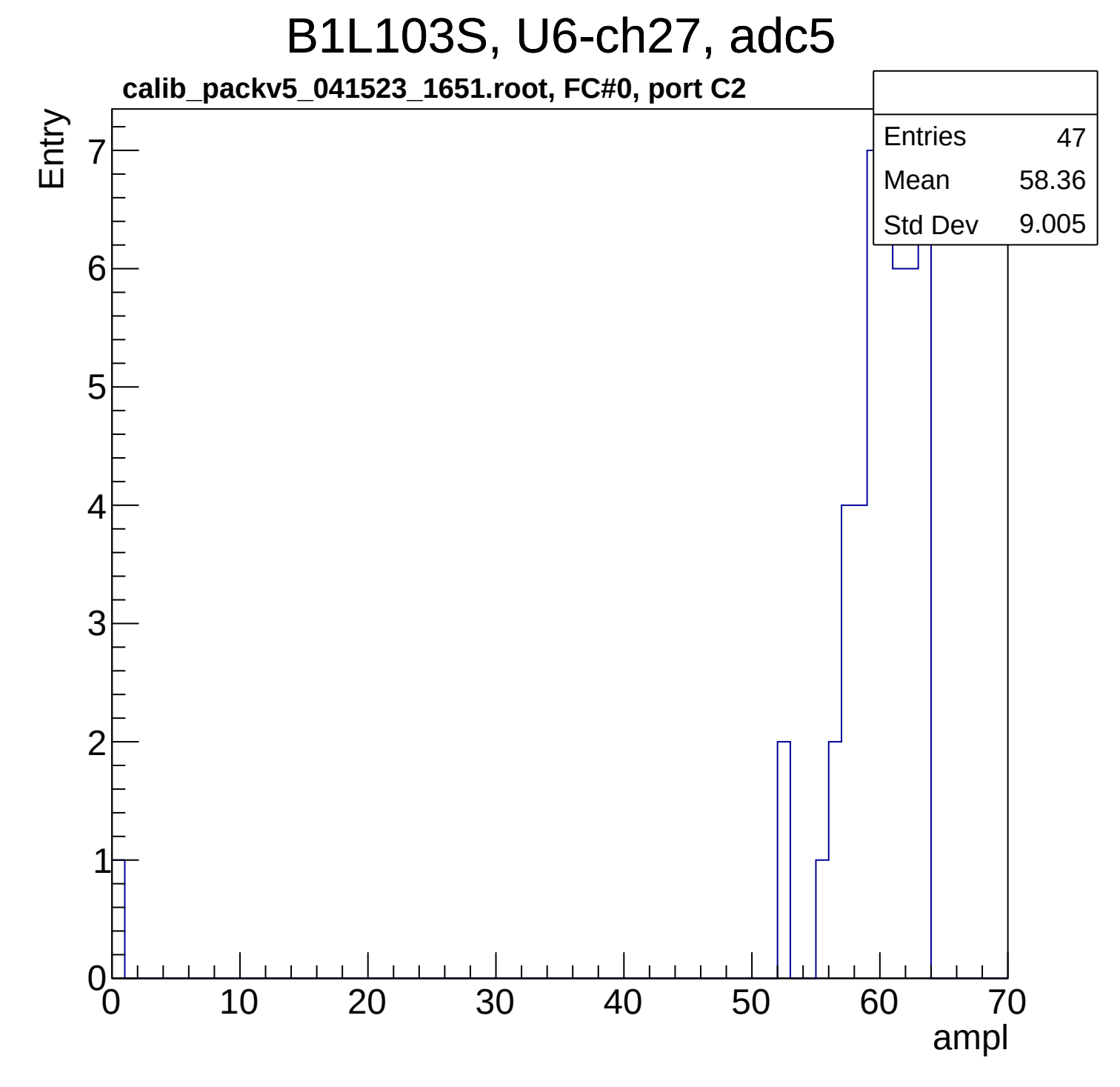
B1L103S, U6-ch27, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 58.36
Std Dev 9.005
Entry
ampl
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1
2
3
4
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6
7
0
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40
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60
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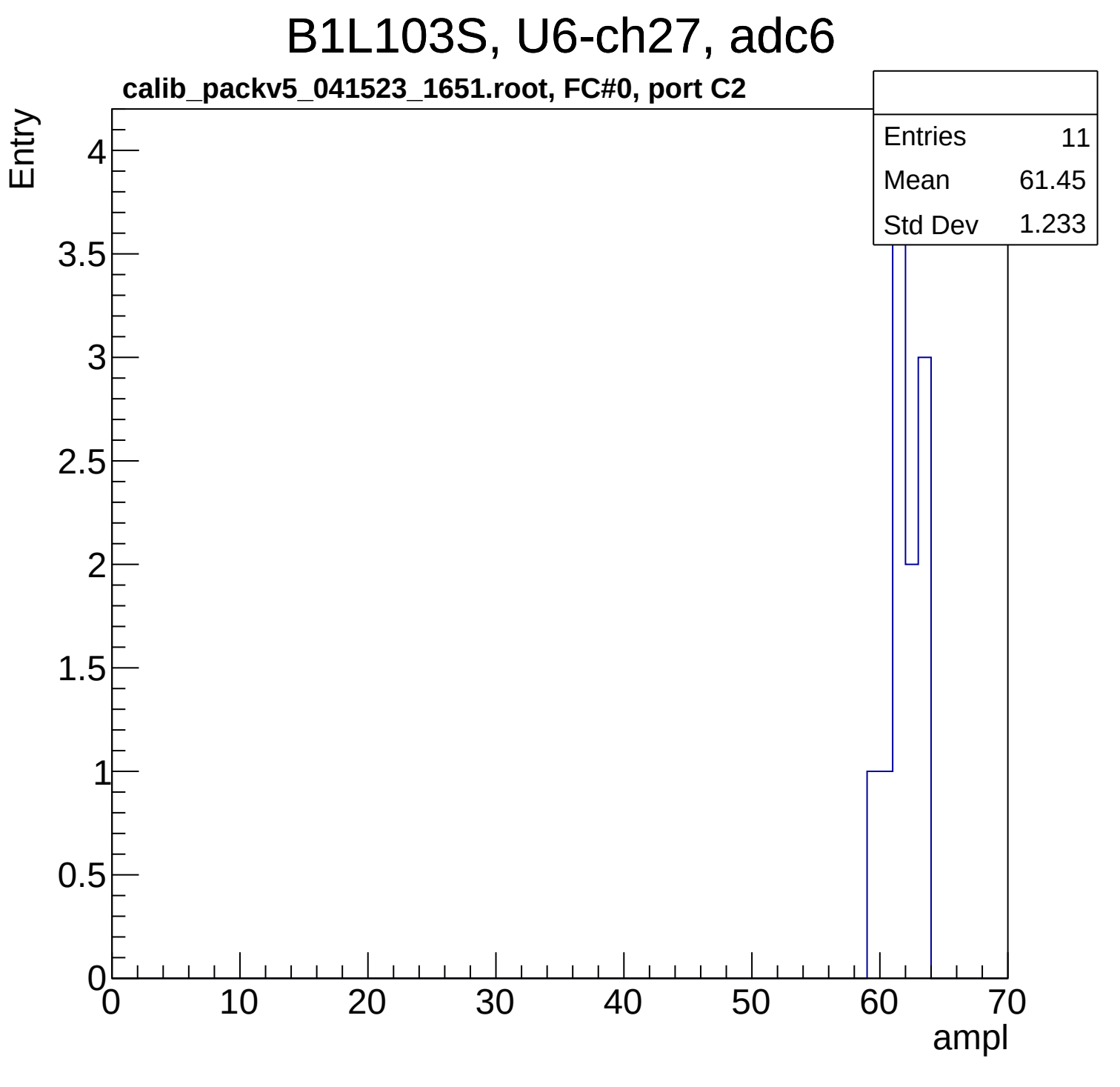
B1L103S, U6-ch27, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 61.45
Std Dev 1.233
Entry
ampl
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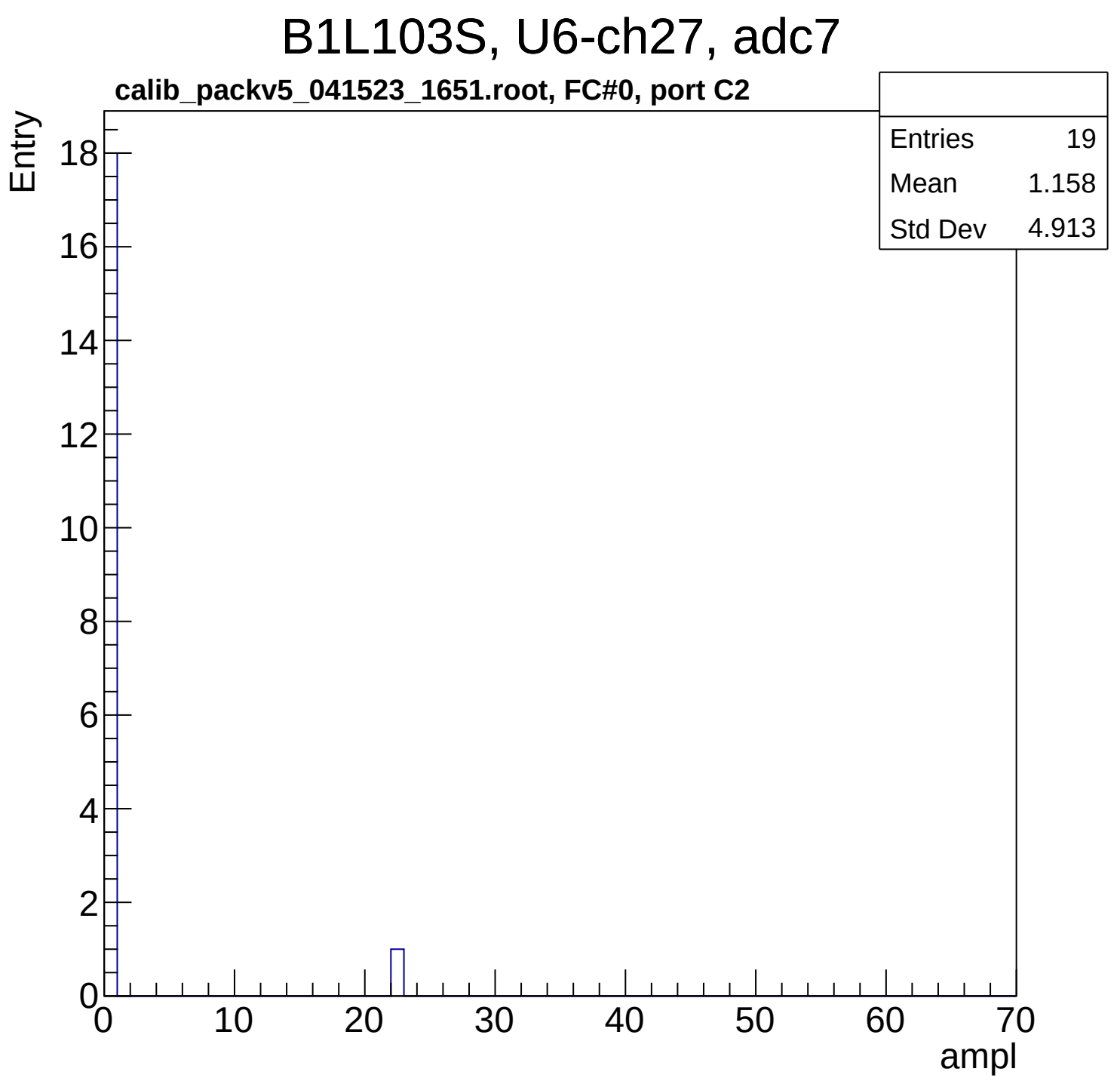
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U6-ch27, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.158
Std Dev 4.913
Entry
0
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6
8
10
12
14
16
18
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10
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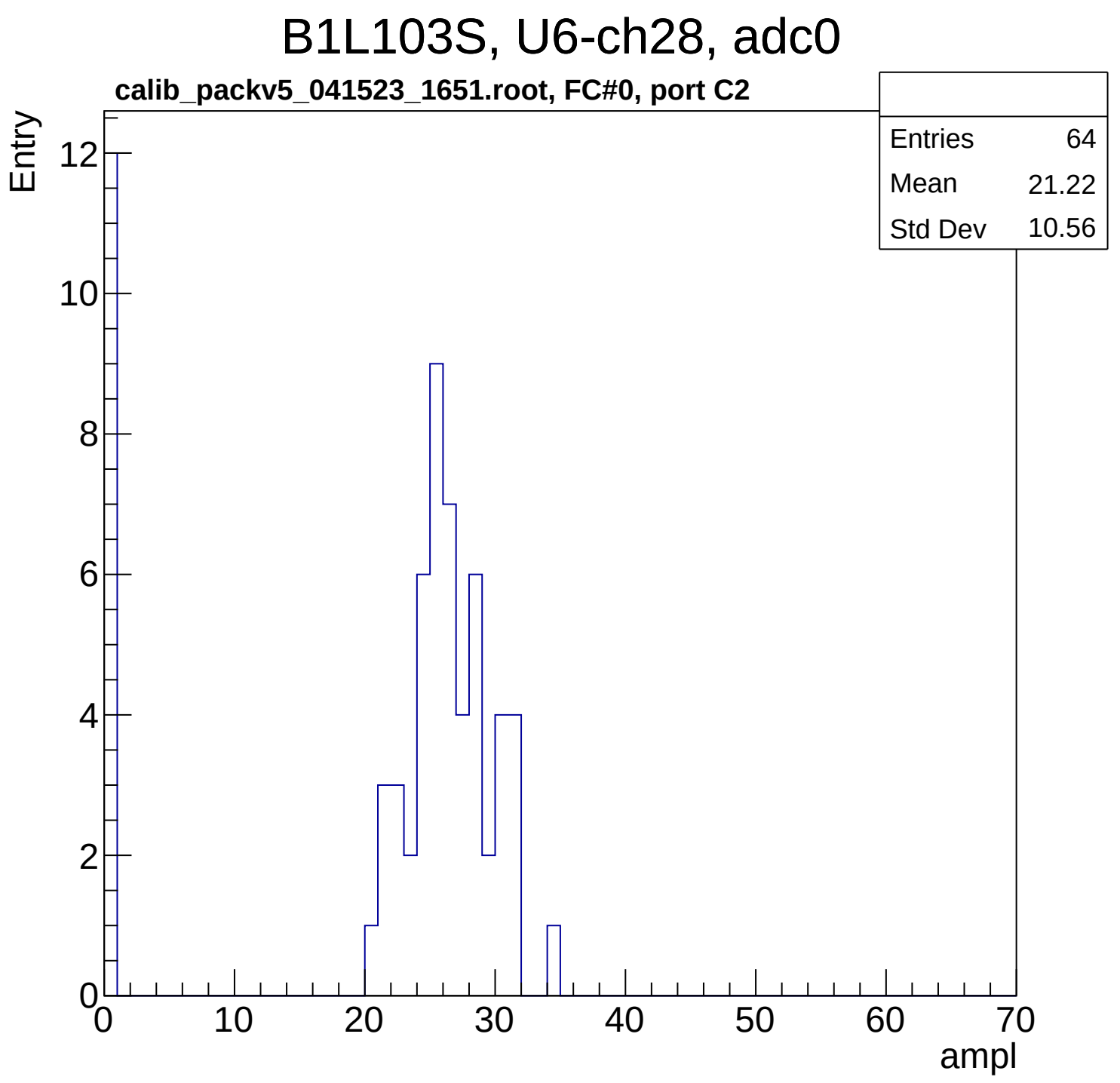
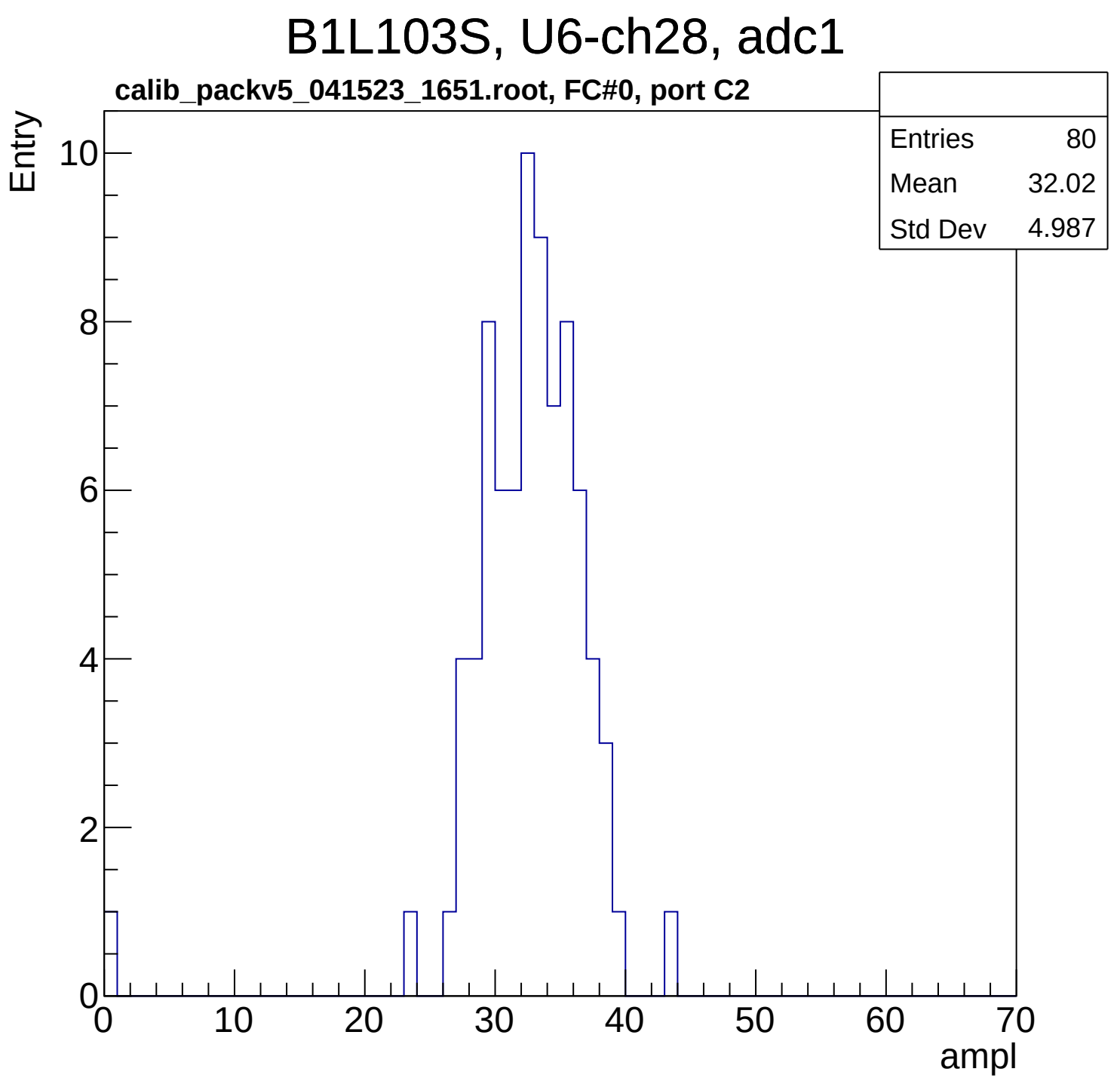
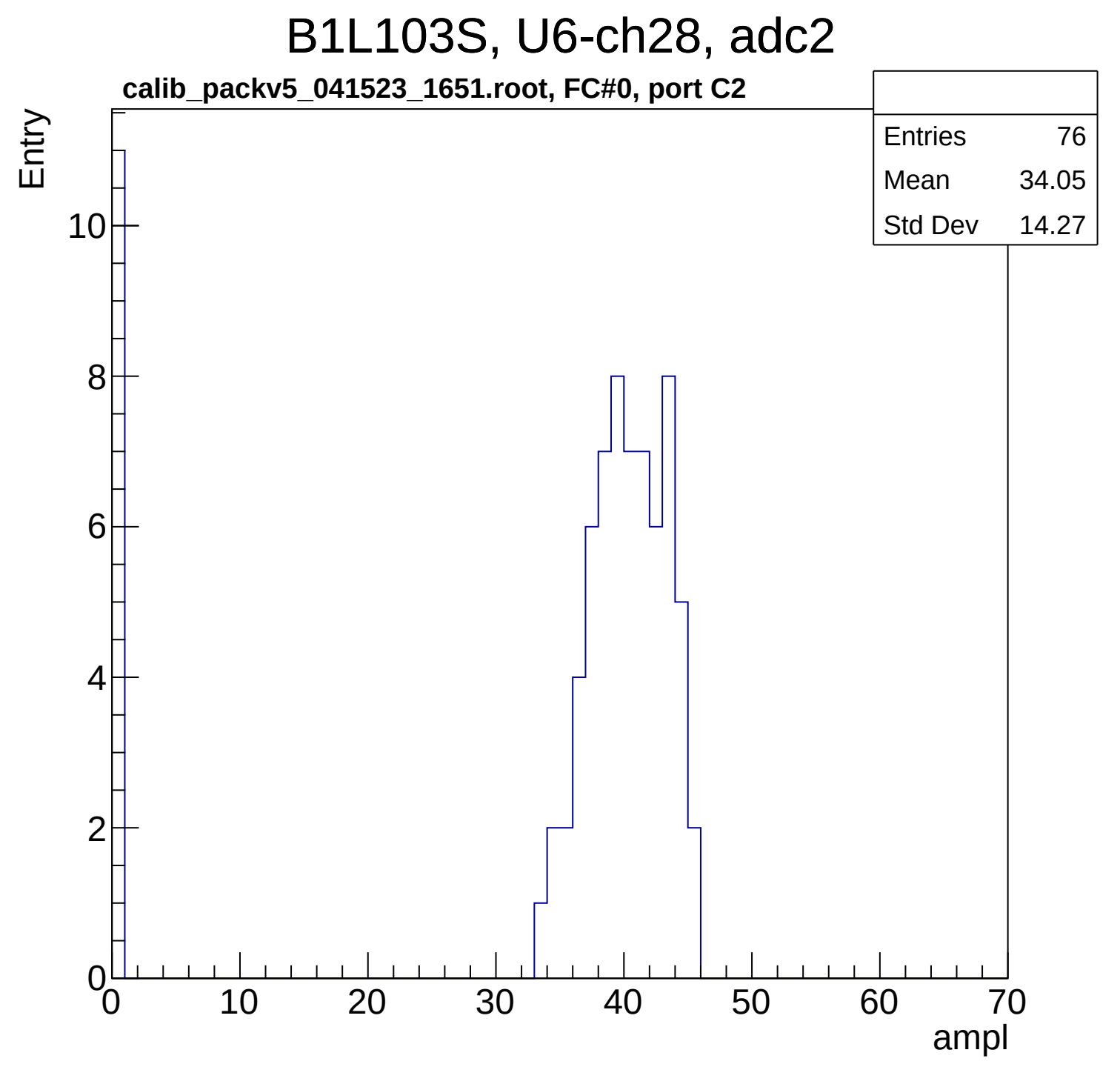
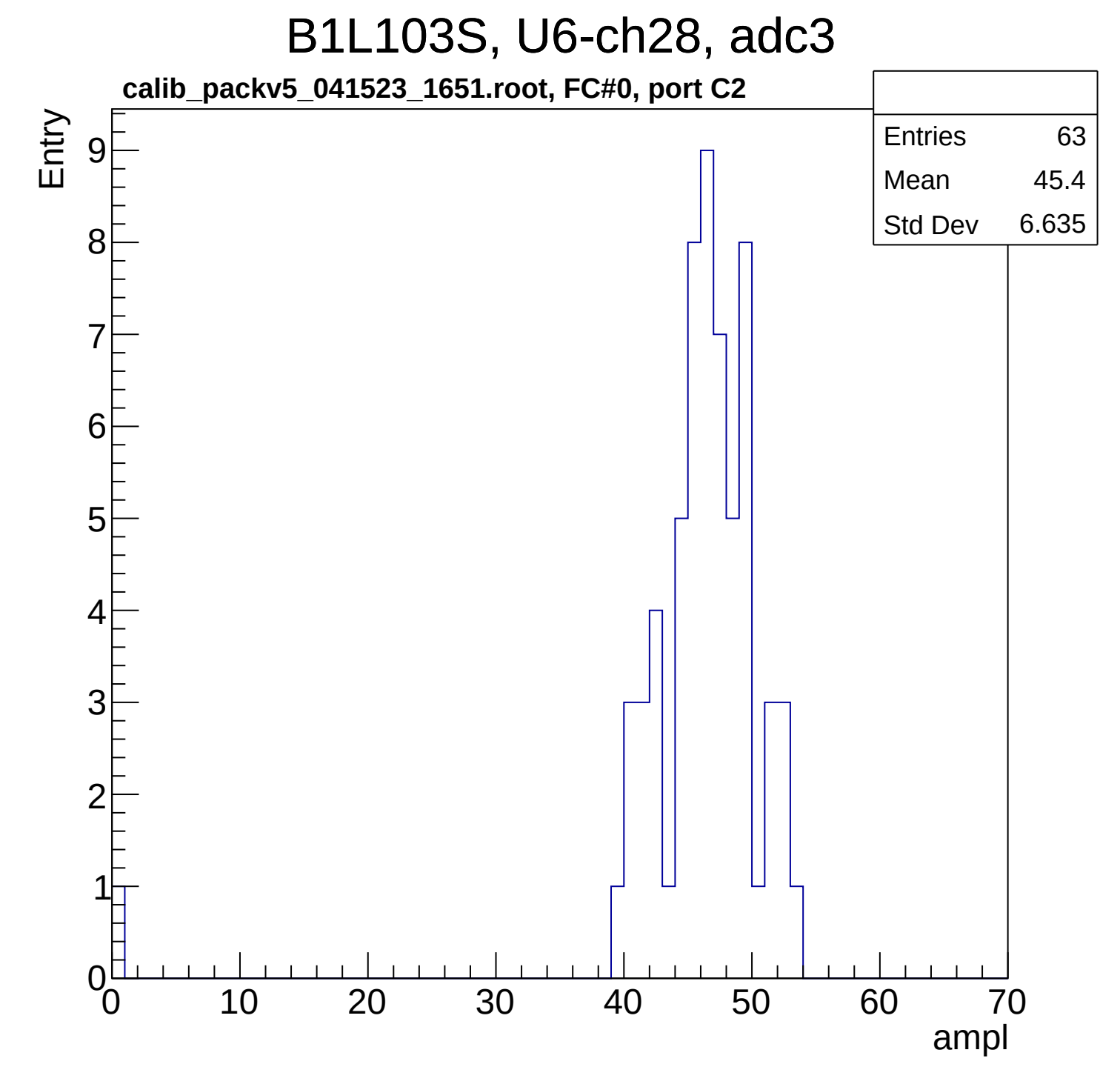
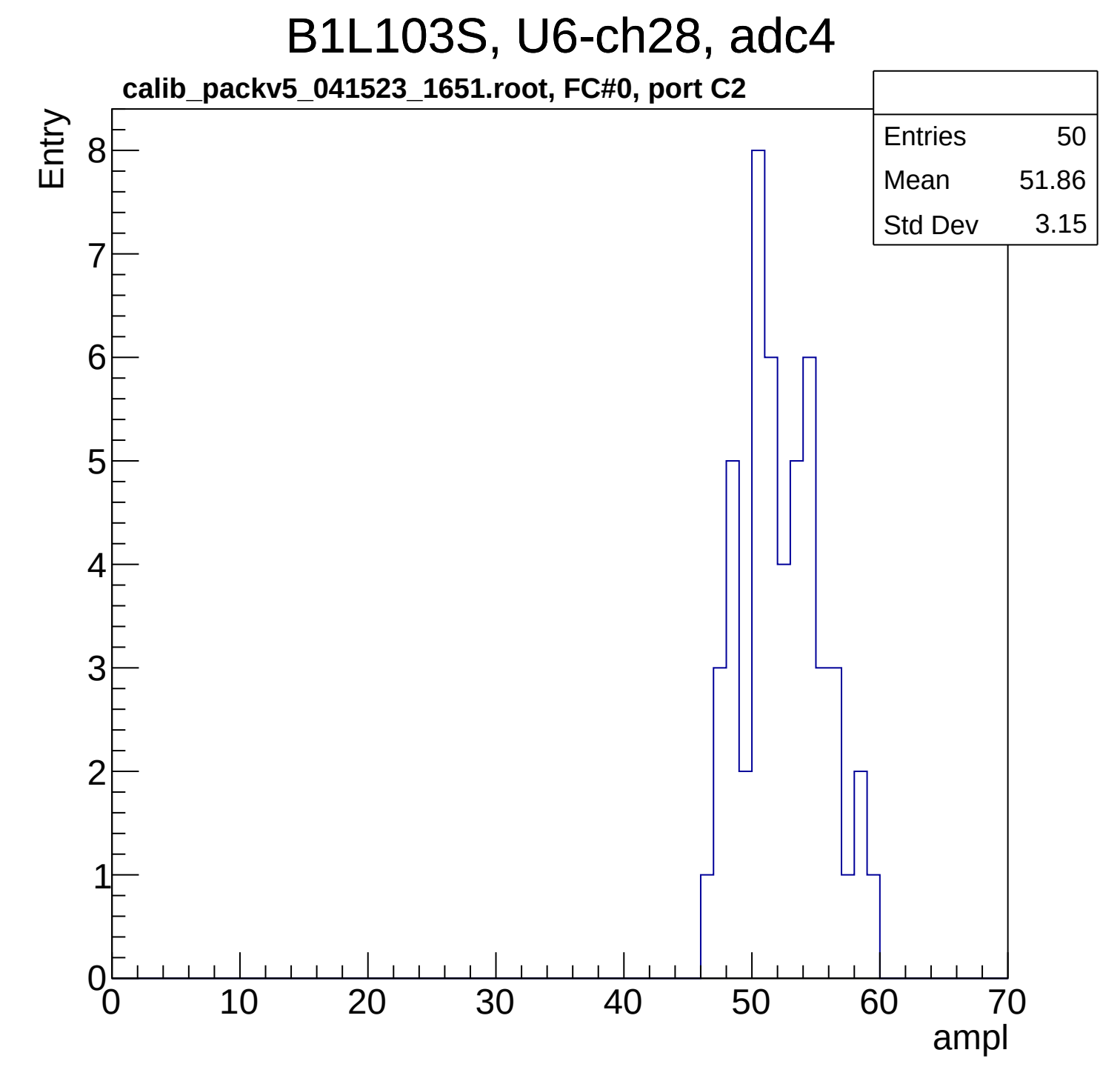
40
50
60
70
ampl

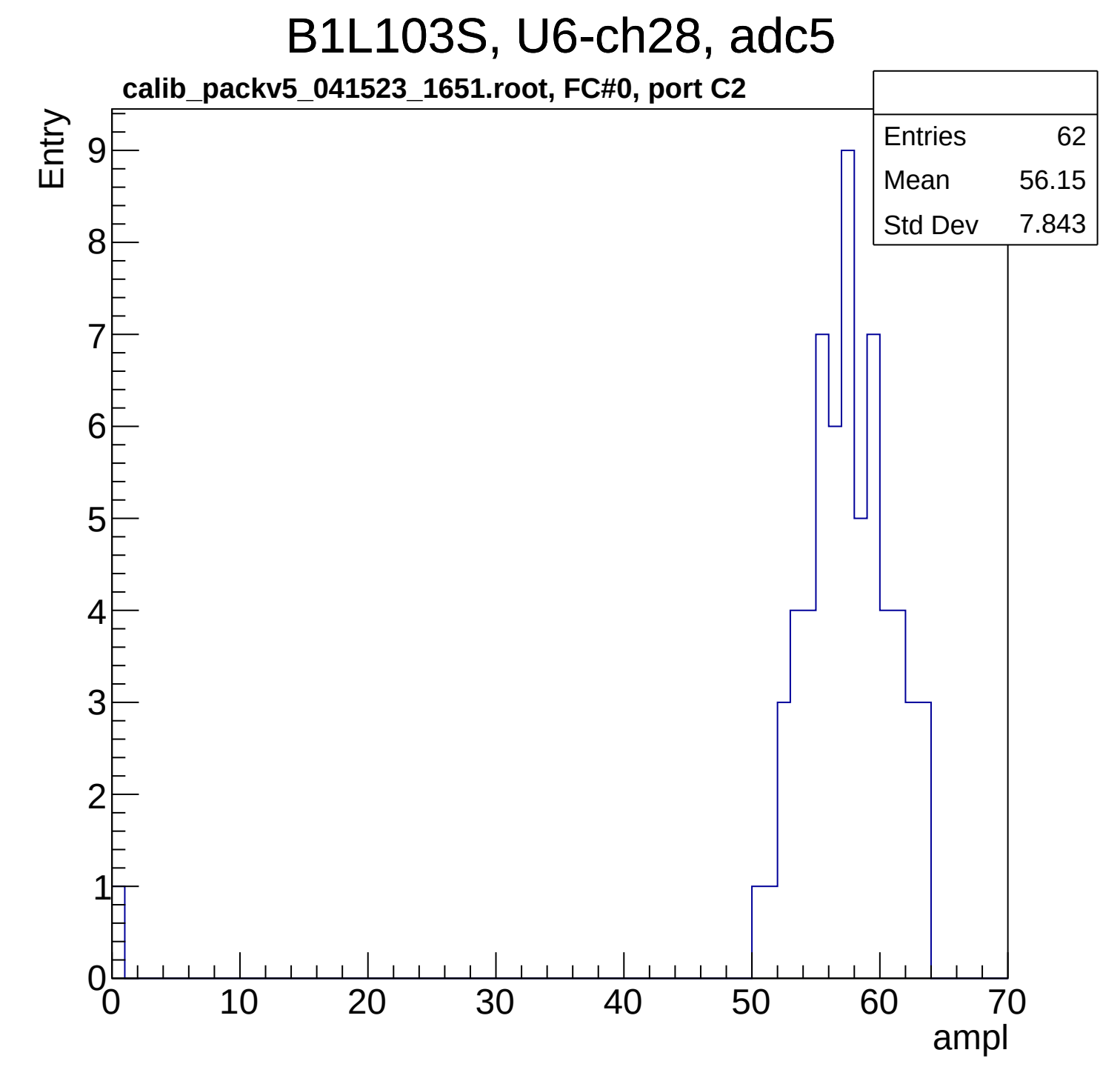

B1L103S, U6-ch28, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 21.22
Std Dev 10.56
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

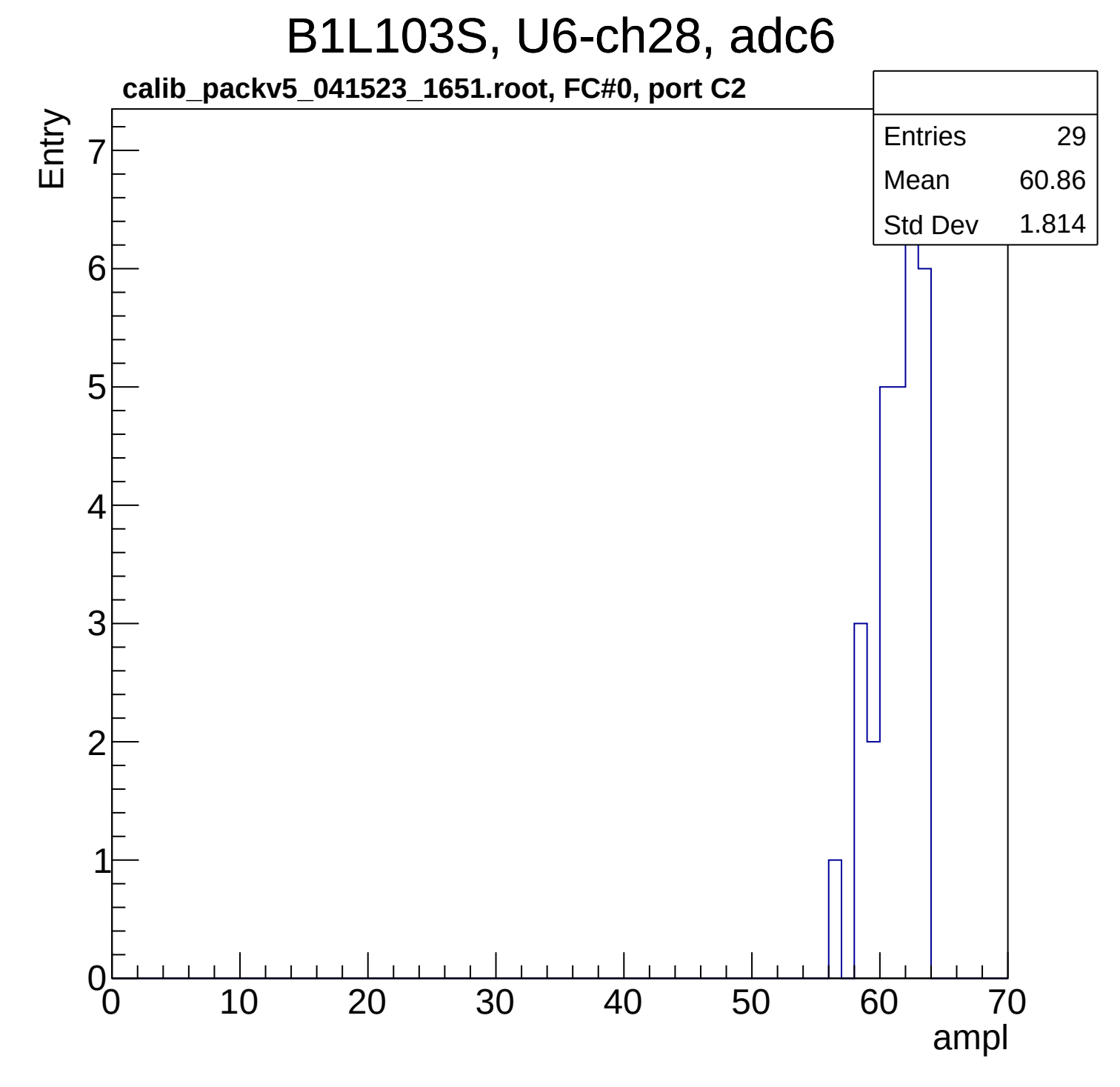

B1L103S, U6-ch28, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 32.02
Std Dev 4.987
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

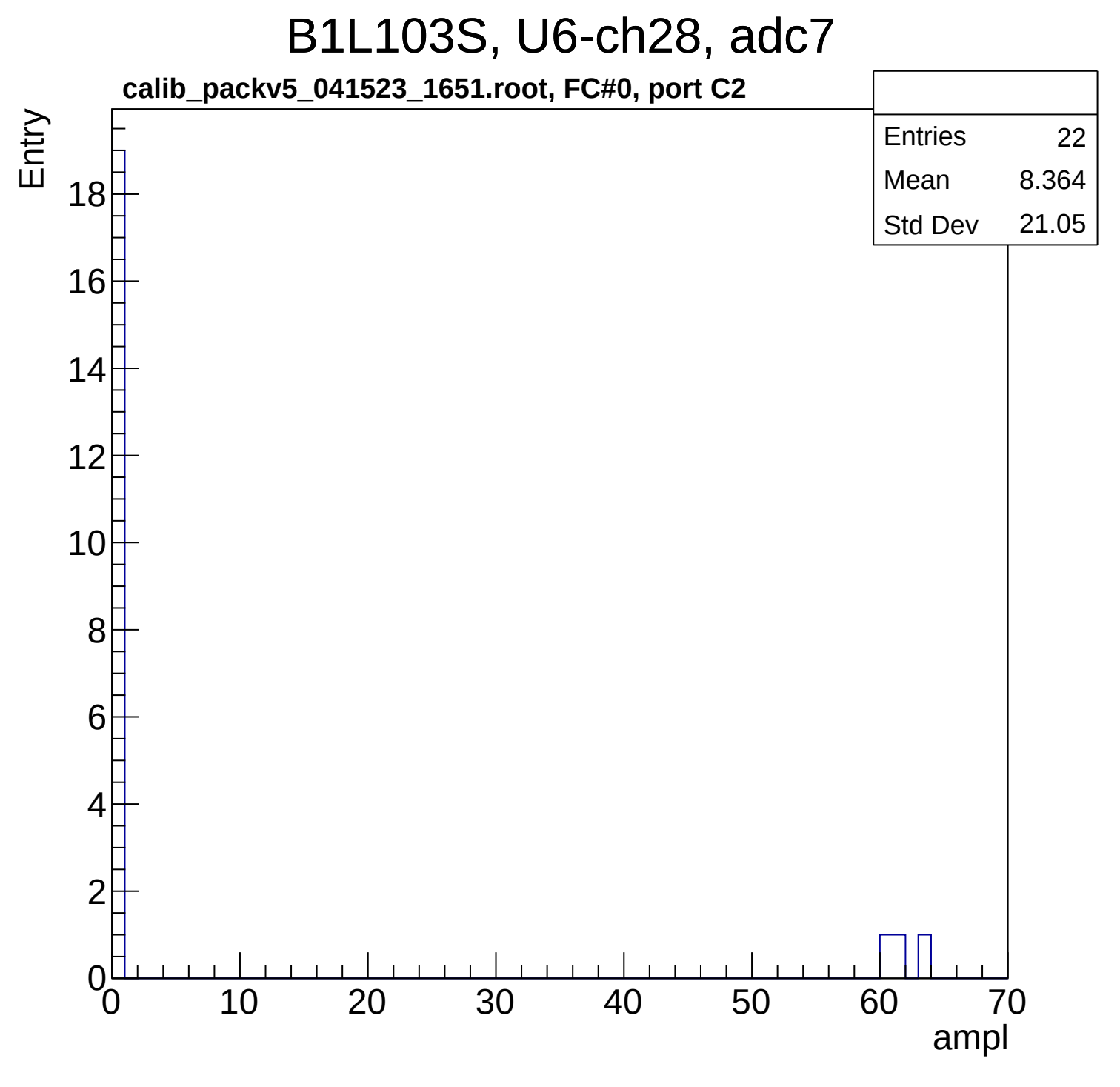

B1L103S, U6-ch28, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 34.05
Std Dev 14.27
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

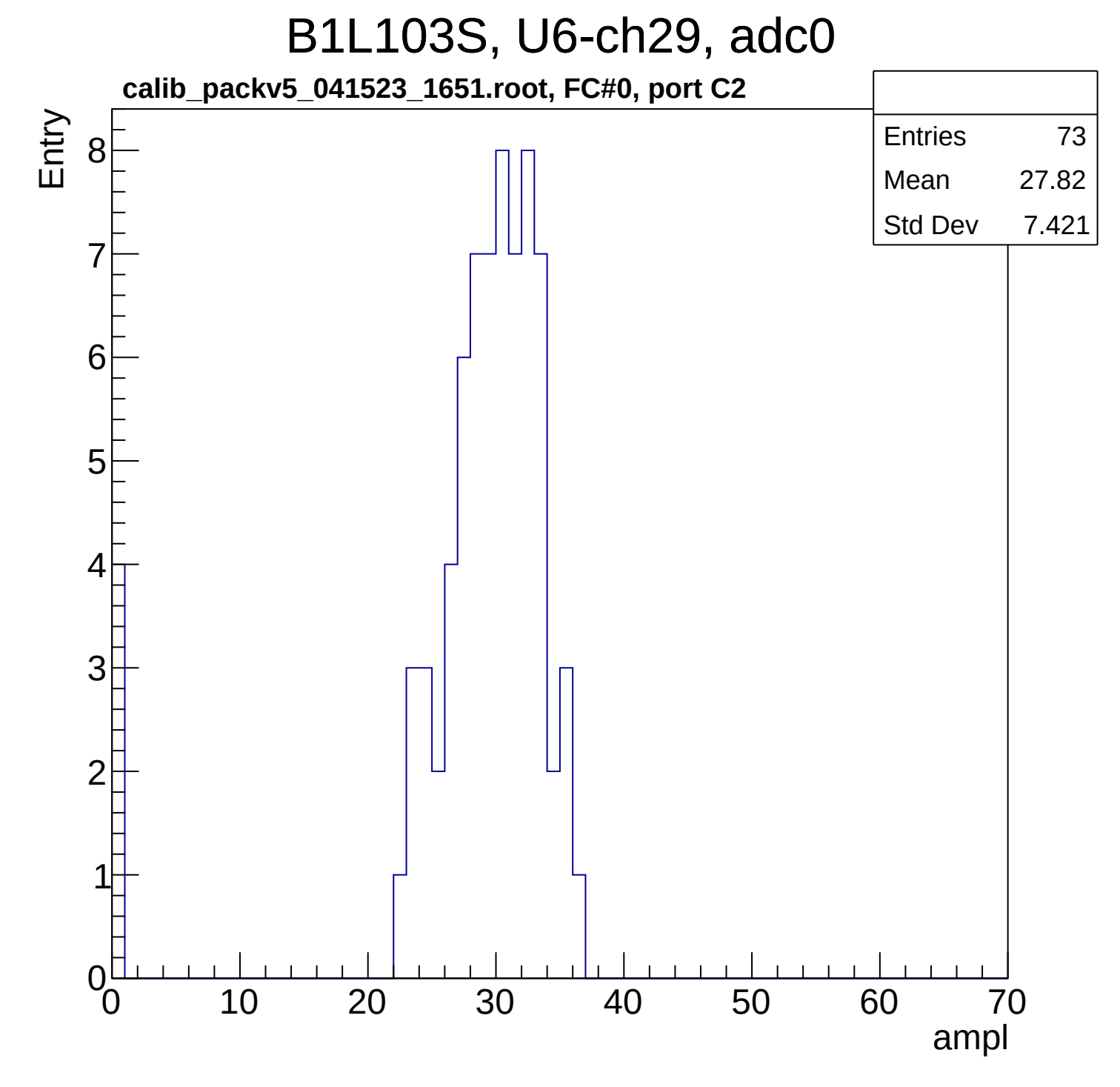

B1L103S, U6-ch28, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 45.4
Std Dev 6.635
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch28, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 51.86
Std Dev 3.15
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch28, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 56.15
Std Dev 7.843
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch28, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 60.86
Std Dev 1.814
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U6-ch28, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.364
Std Dev 21.05
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch29, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 27.82
Std Dev 7.421
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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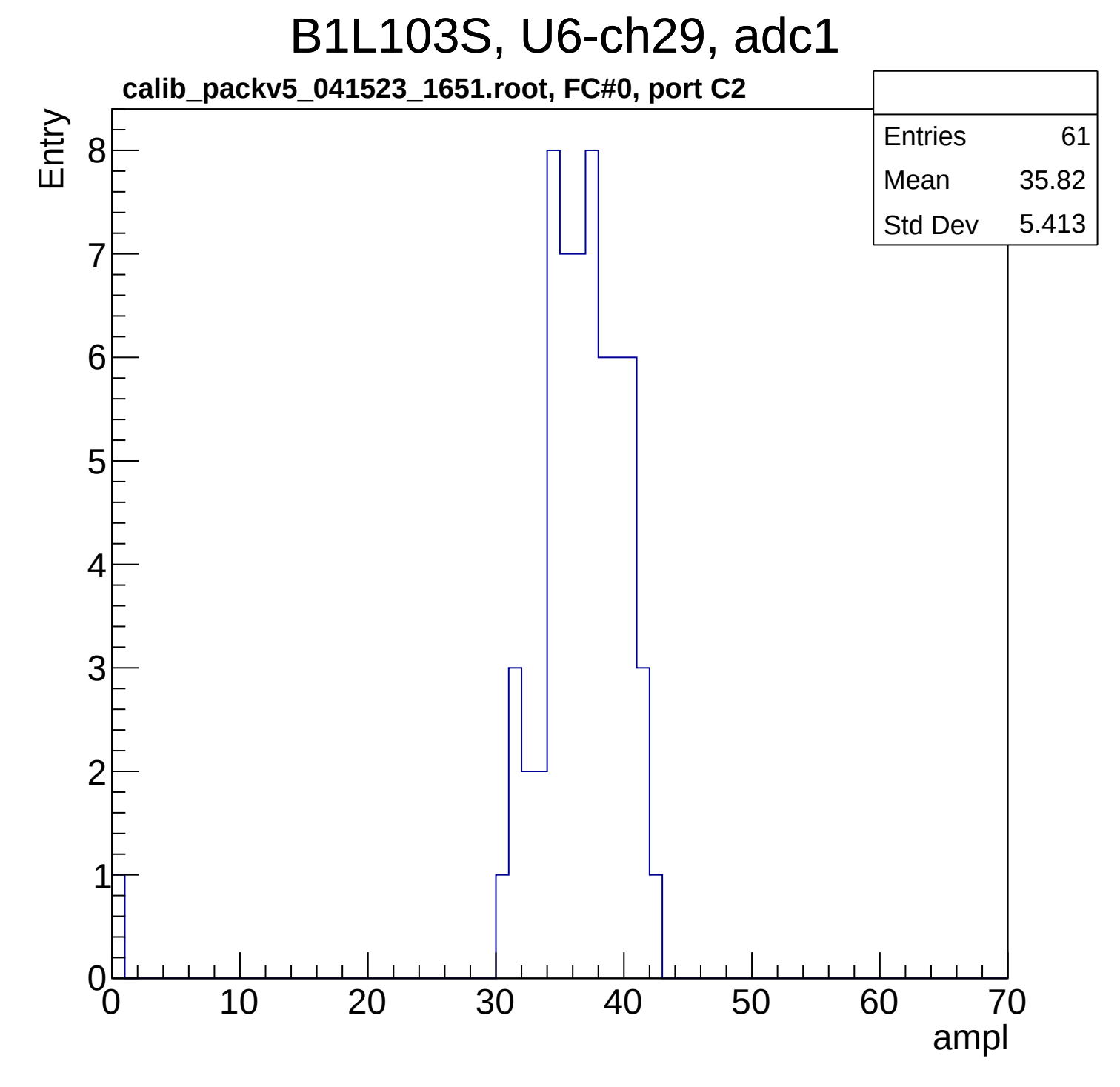
40
50
60
70


B1L103S, U6-ch29, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 35.82
Std Dev 5.413
Entry
ampl
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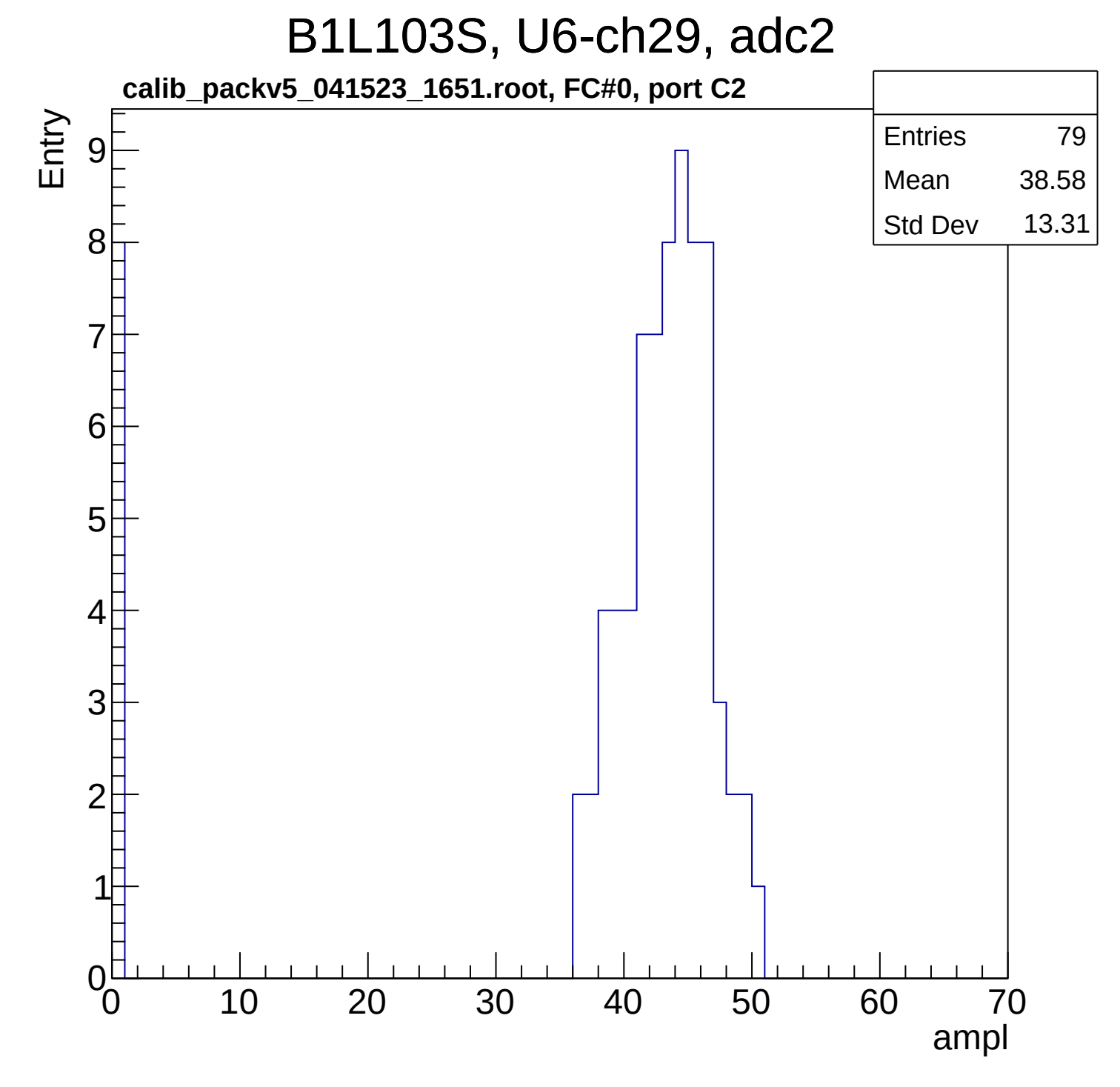
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch29, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 38.58
Std Dev 13.31
Entry
ampl
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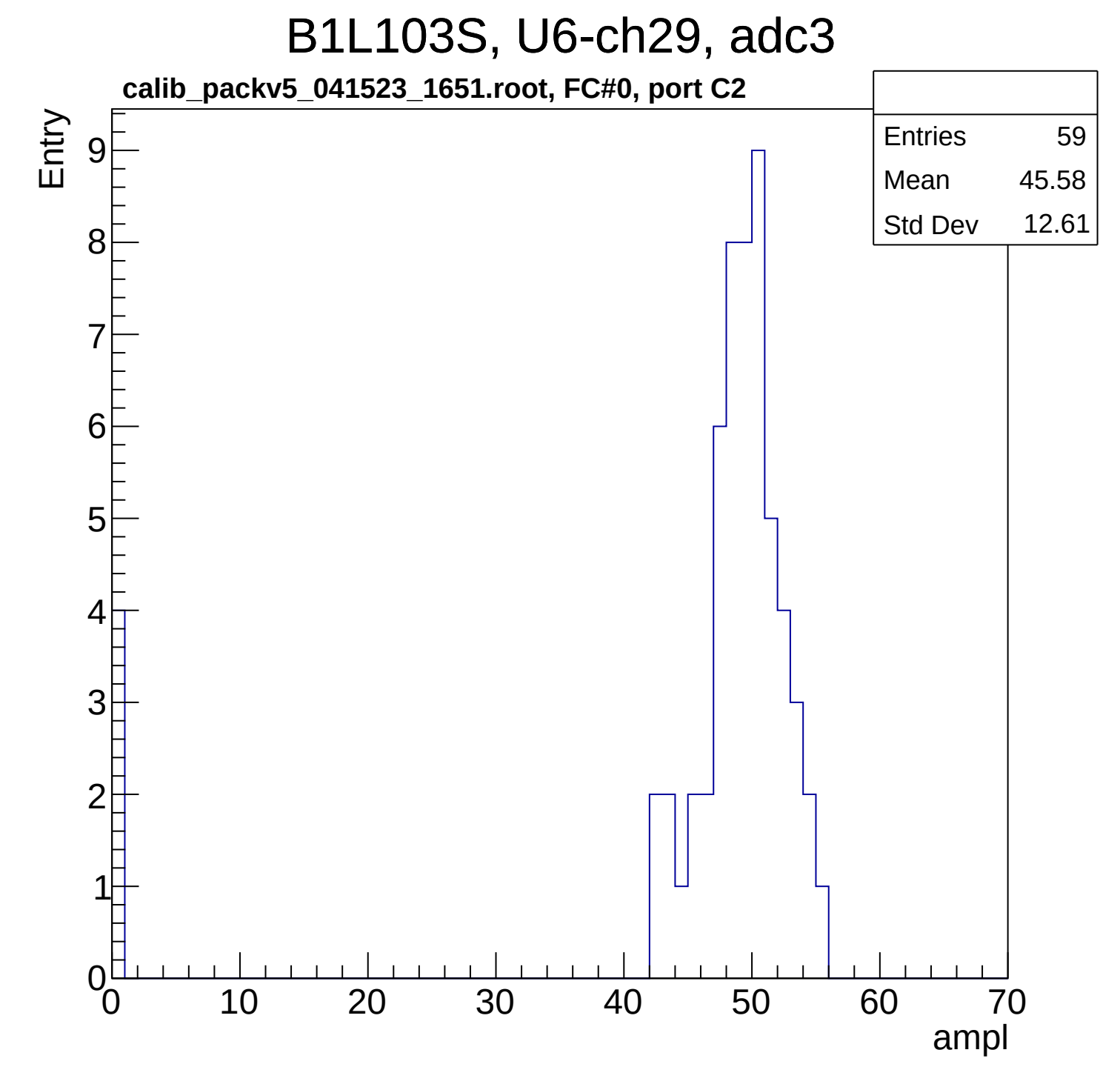
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch29, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 45.58
Std Dev 12.61
Entry
ampl
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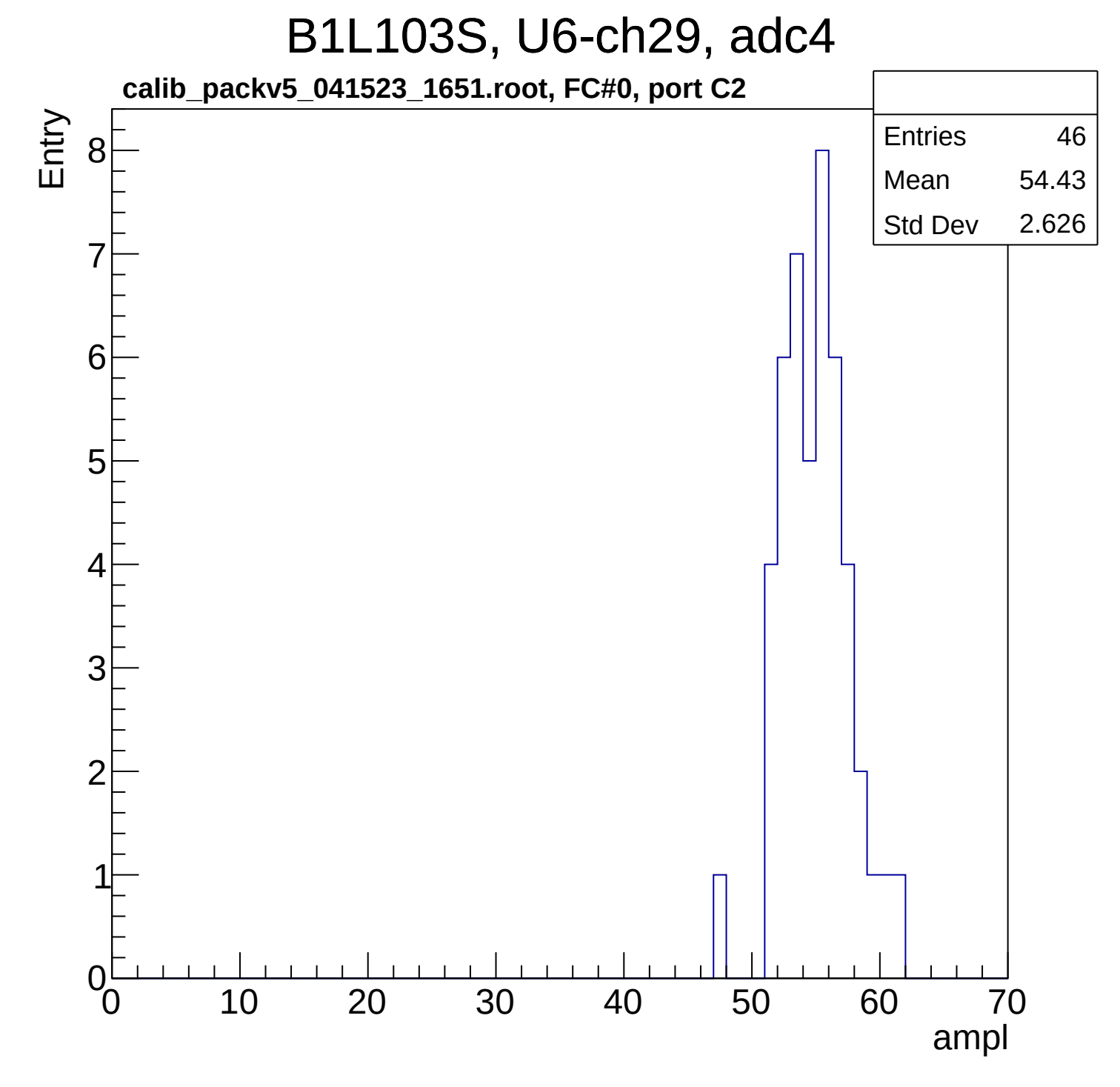
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch29, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 54.43
Std Dev 2.626
Entry
ampl
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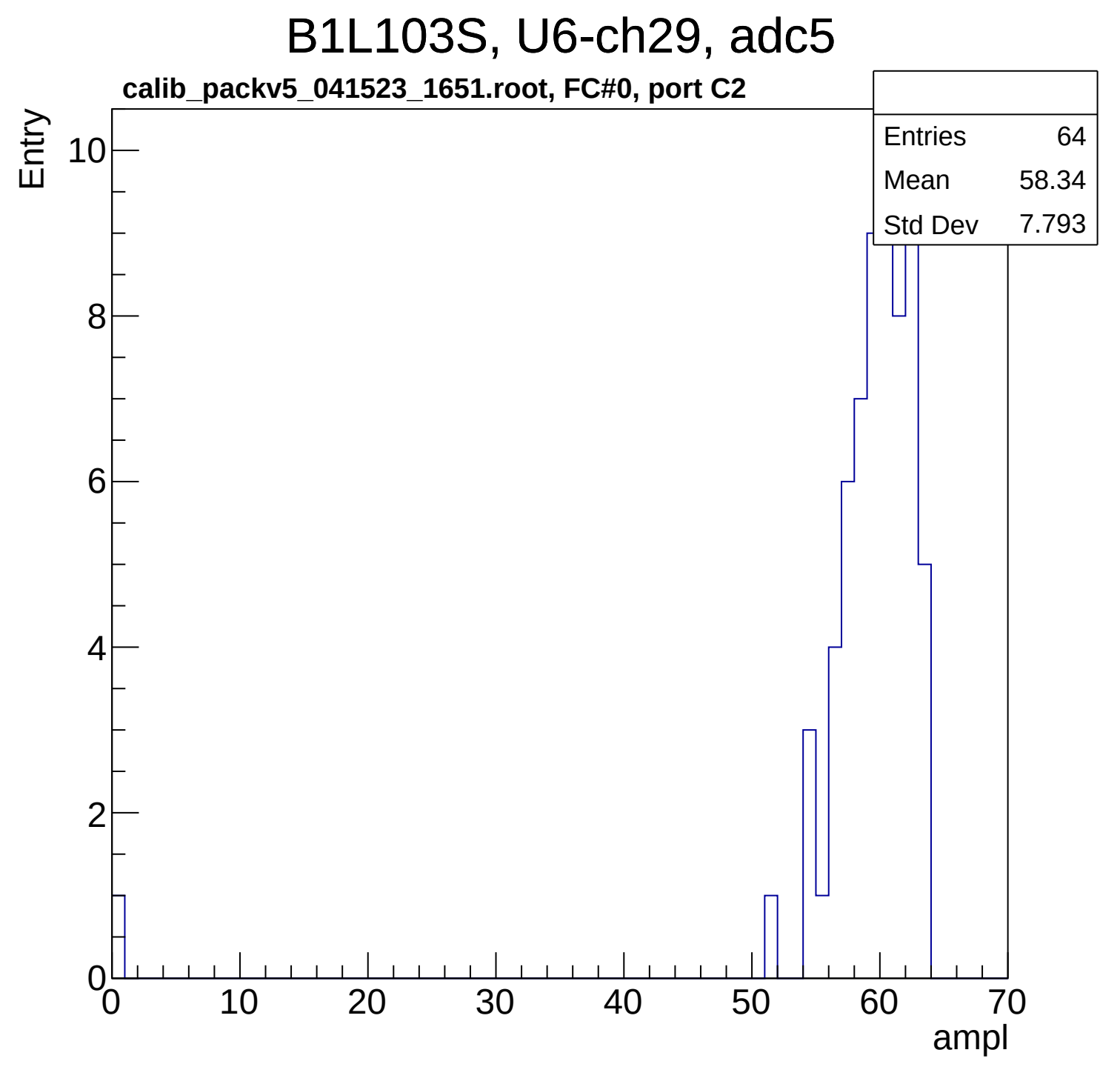
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch29, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 58.34
Std Dev 7.793
Entry
ampl
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8
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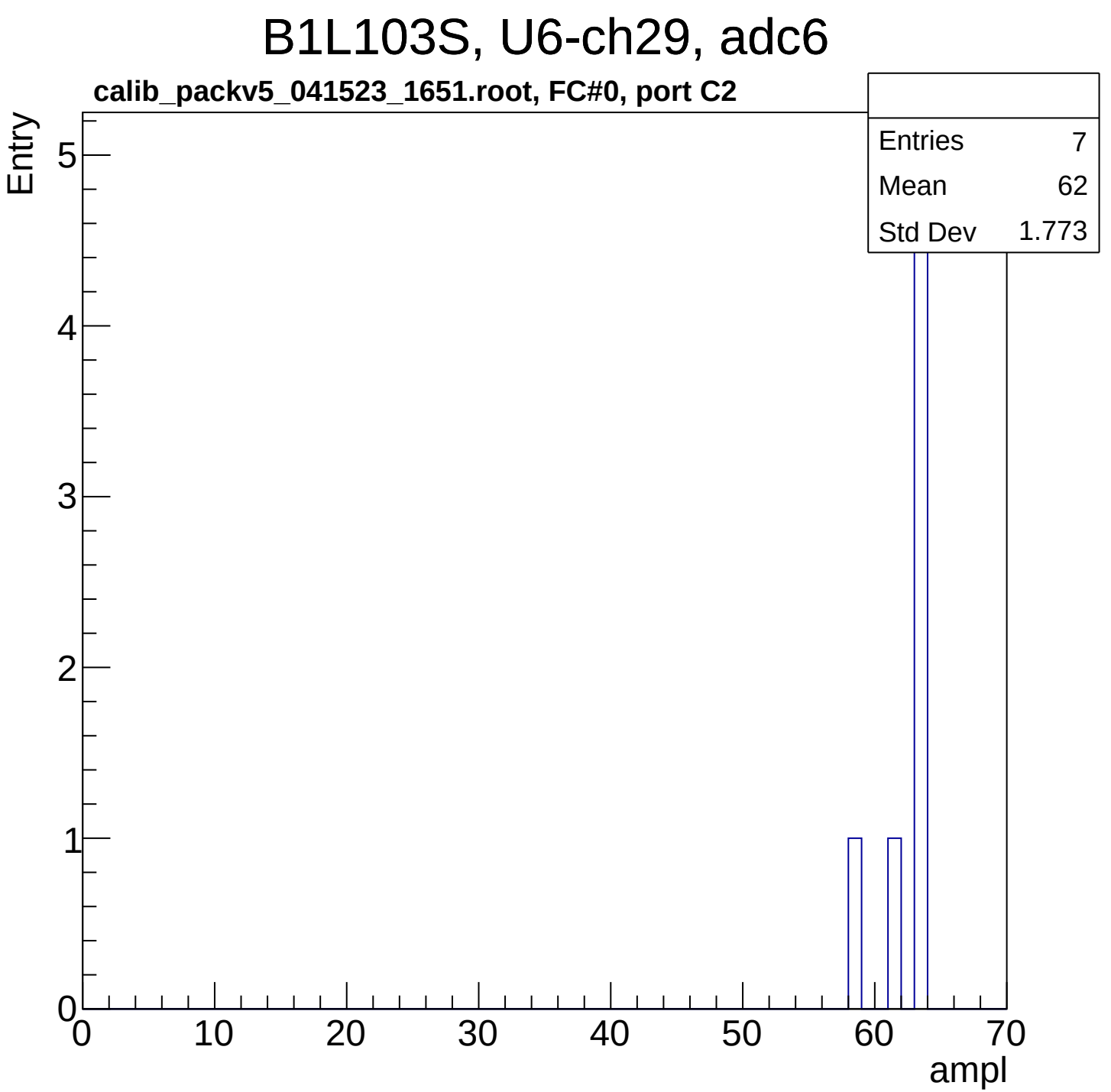
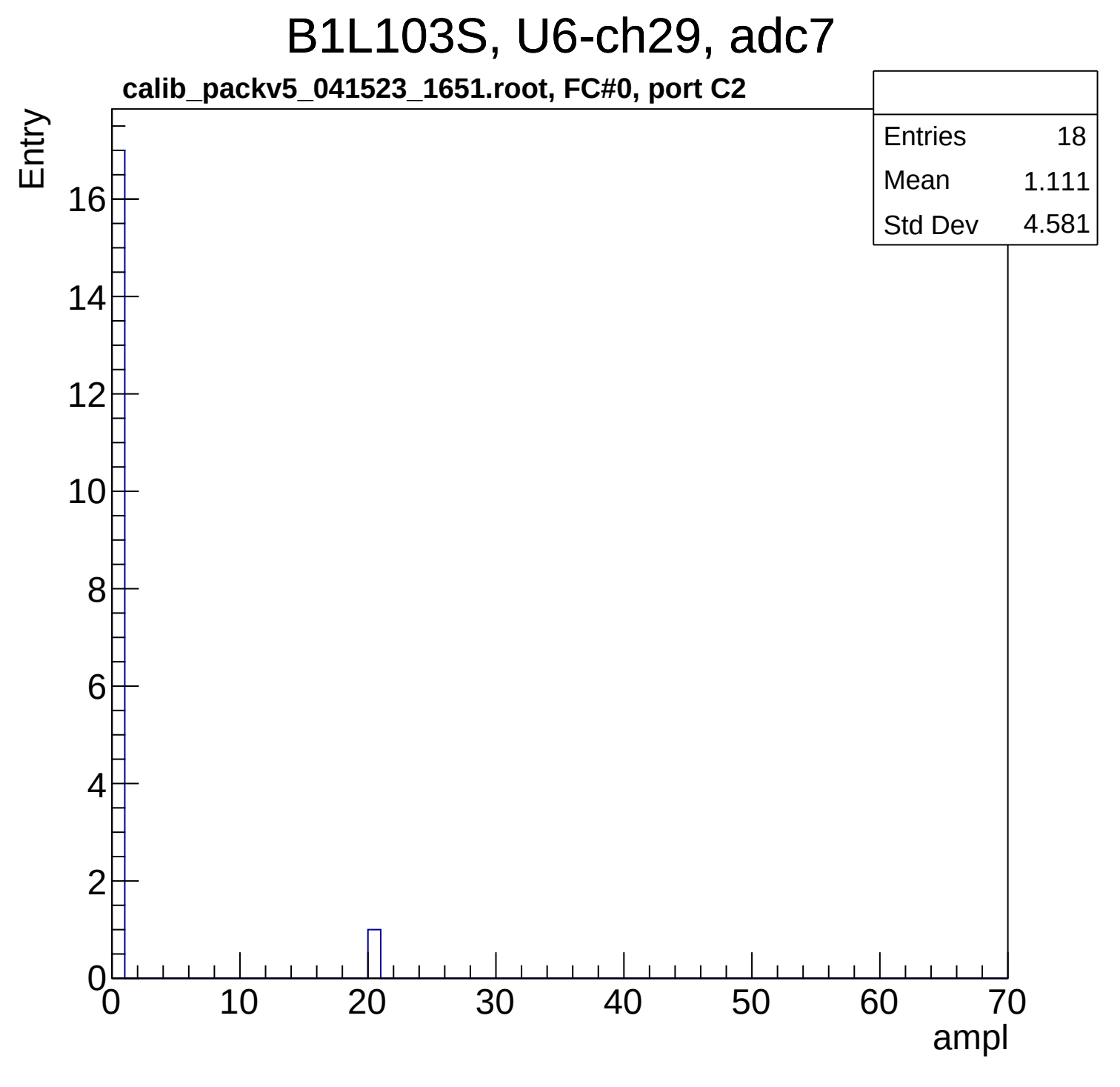
0
10
20
30
40
50
60
70


B1L103S, U6-ch29, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 62
Std Dev 1.773
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch29, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.111
Std Dev 4.581
Entry
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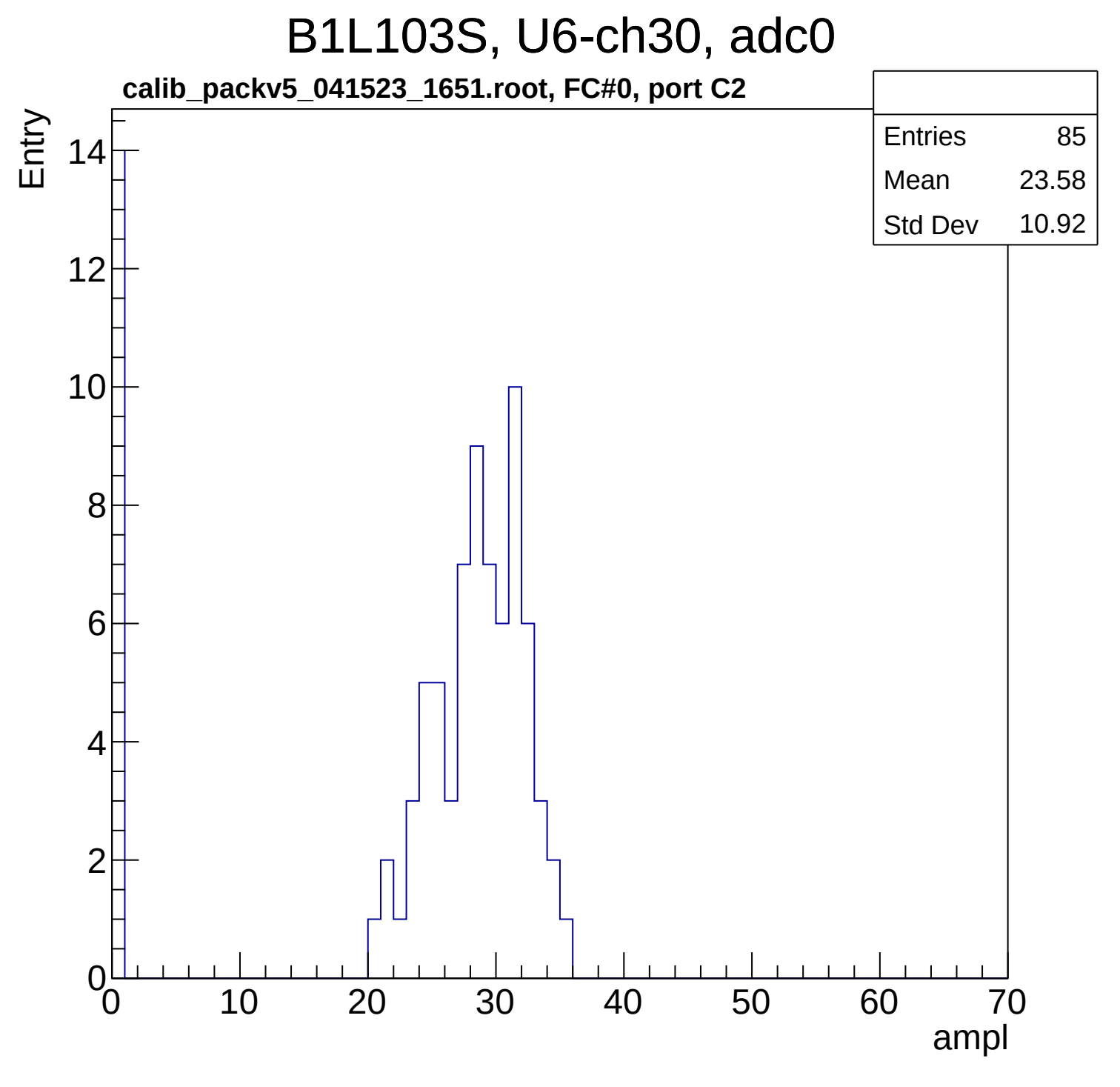
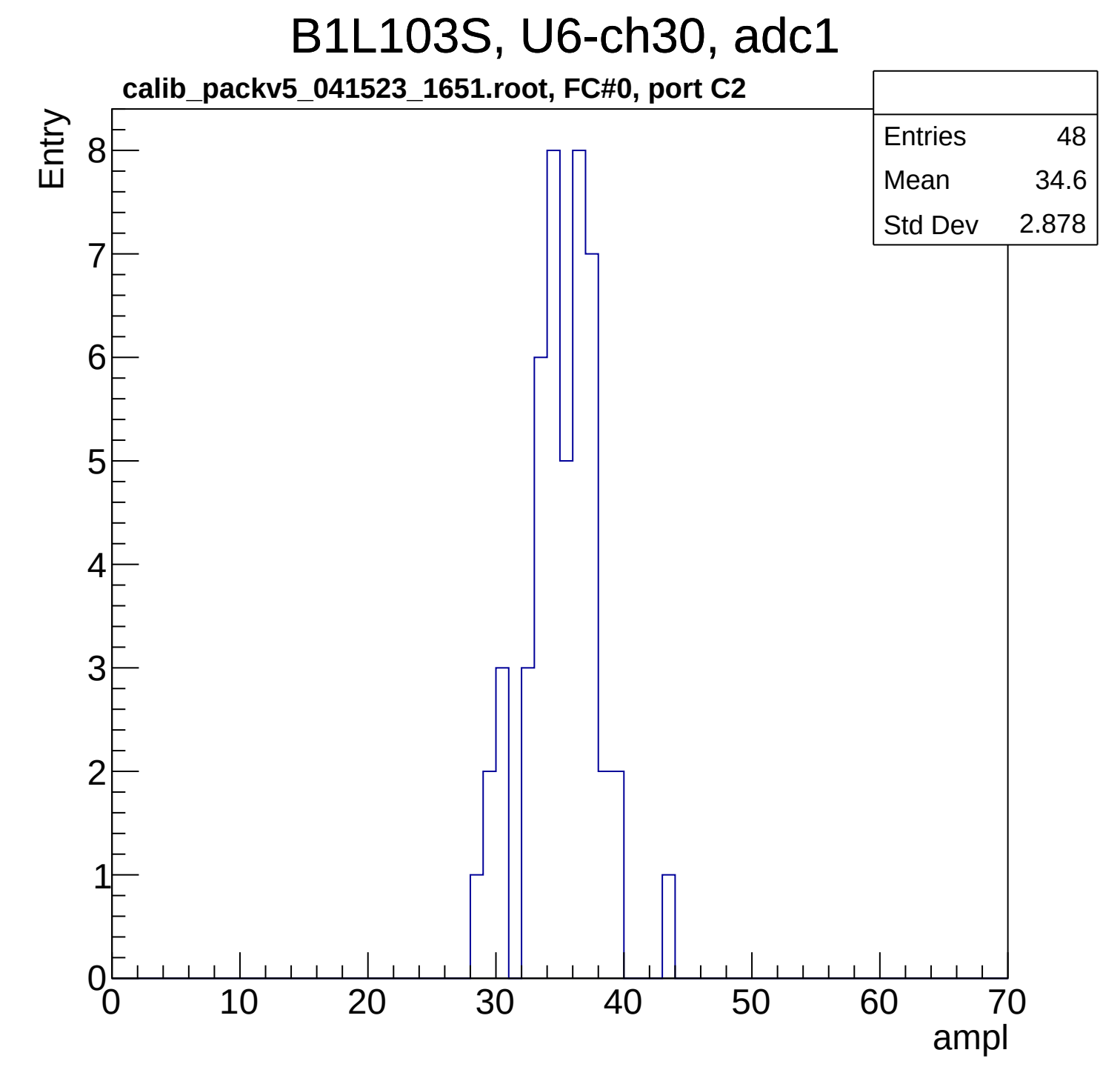
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch30, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 23.58
Std Dev 10.92
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U6-ch30, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 34.6
Std Dev 2.878
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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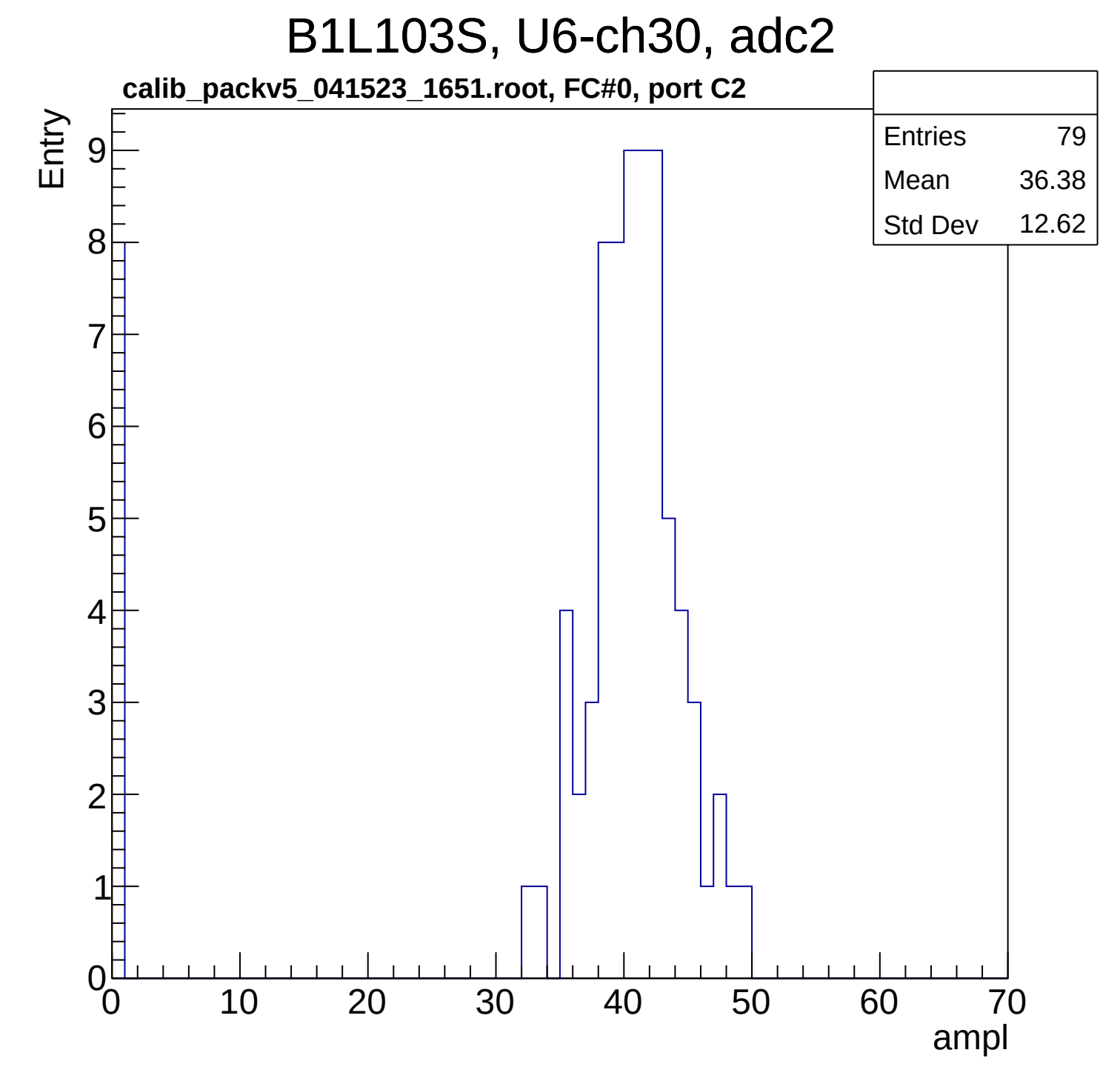
60
70


B1L103S, U6-ch30, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 36.38
Std Dev 12.62
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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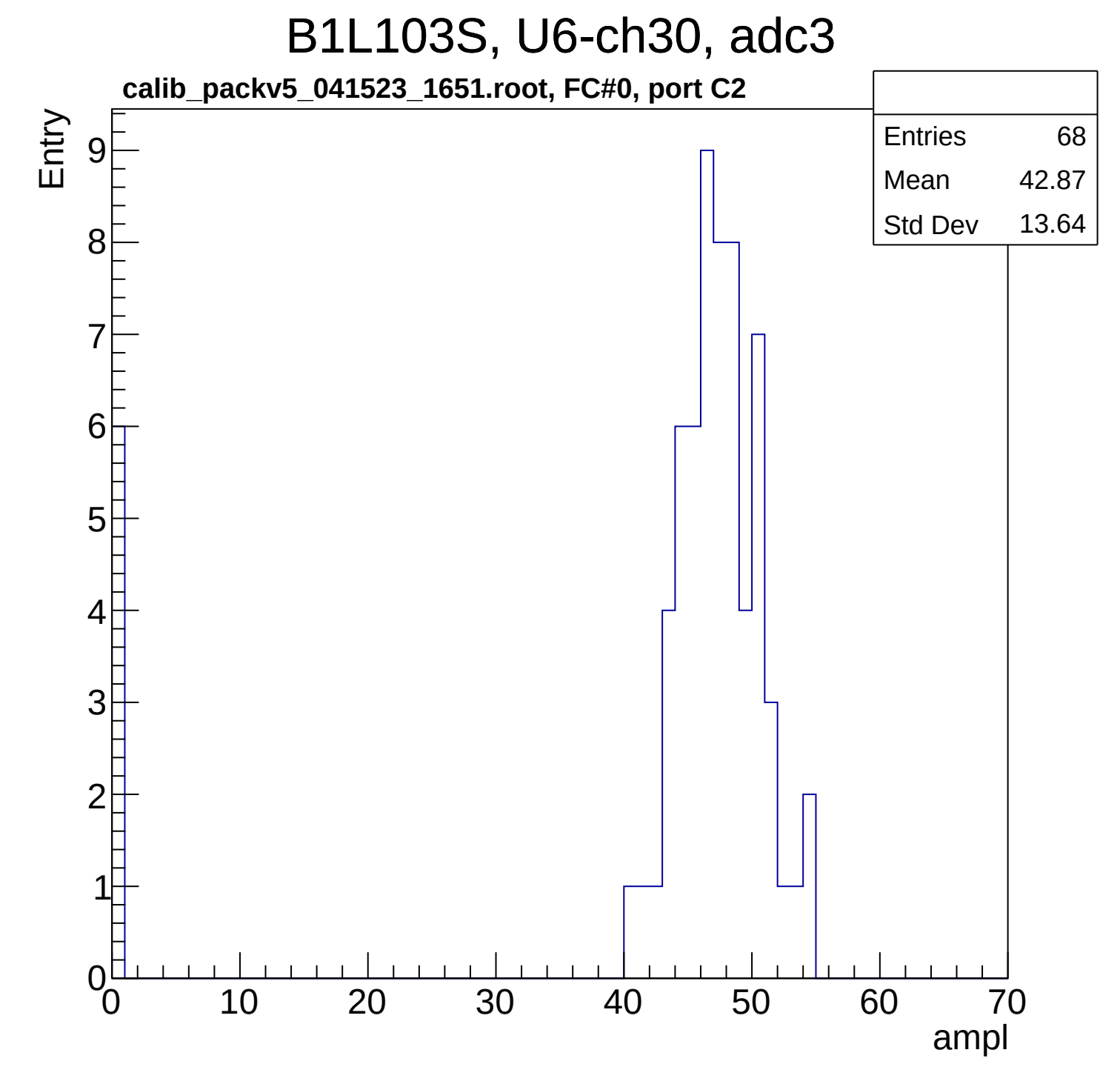
60
70


B1L103S, U6-ch30, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 42.87
Std Dev 13.64
Entry
ampl
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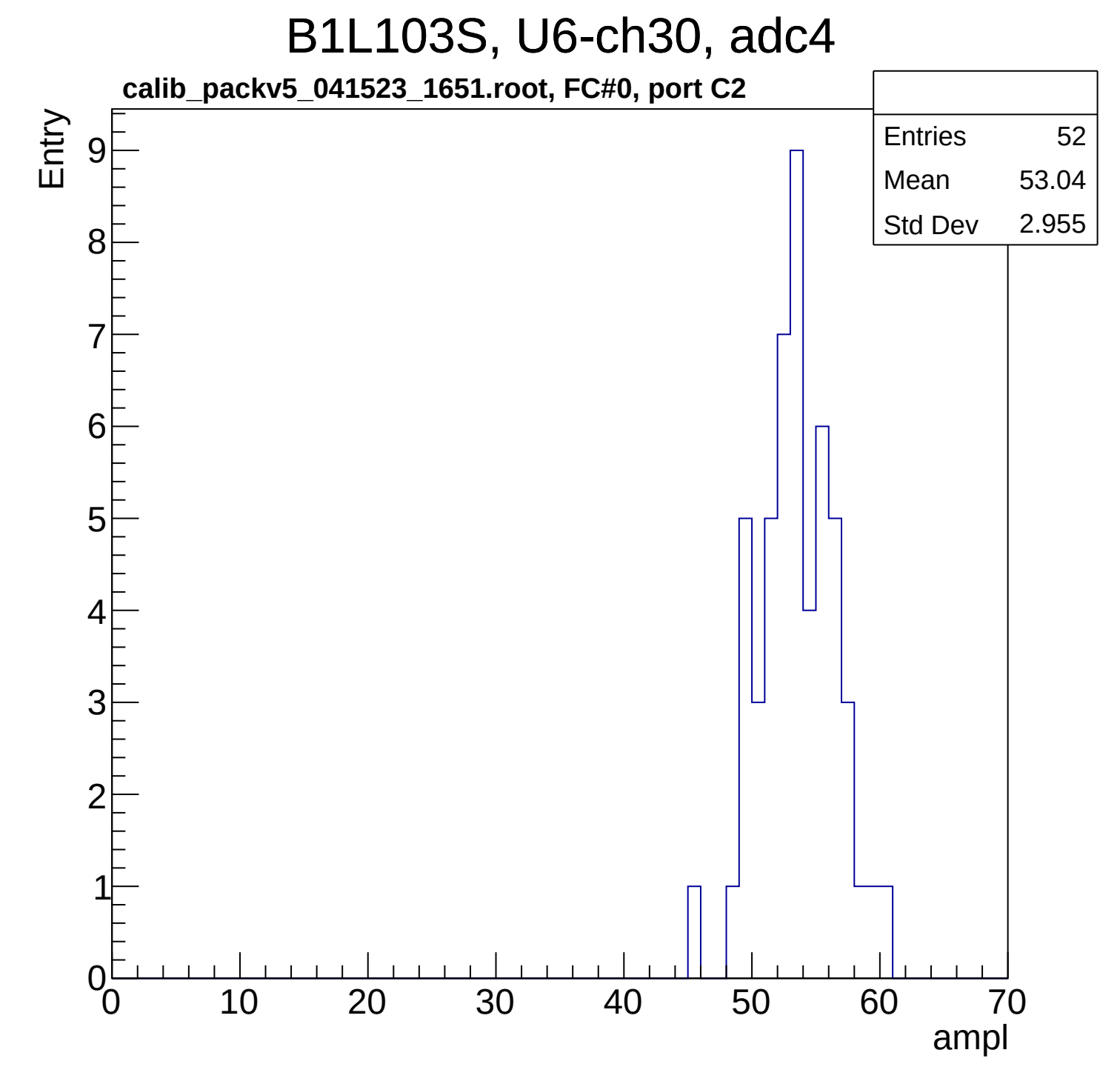
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch30, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 53.04
Std Dev 2.955
Entry
ampl
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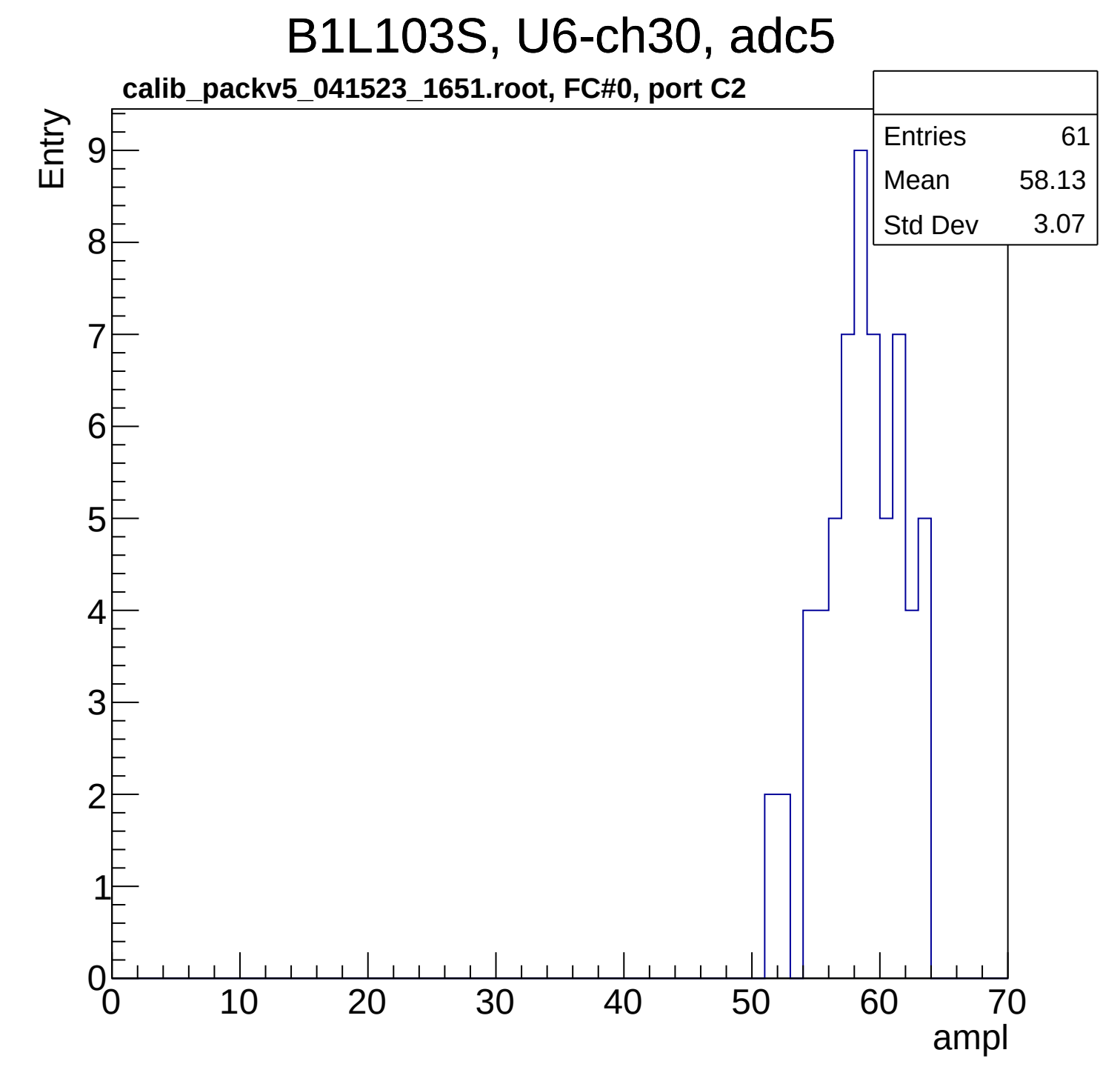
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch30, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 58.13
Std Dev 3.07
Entry
ampl
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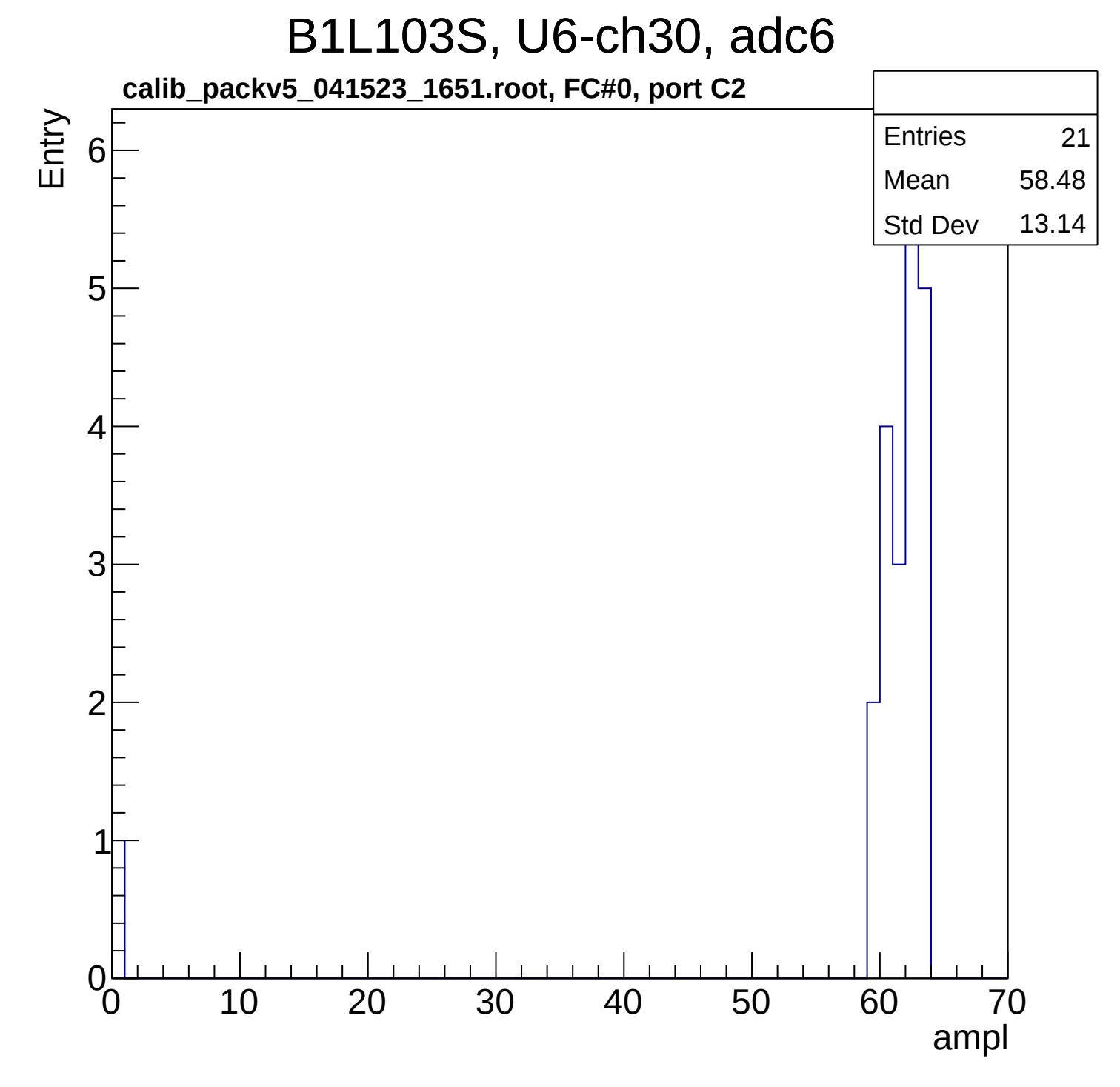
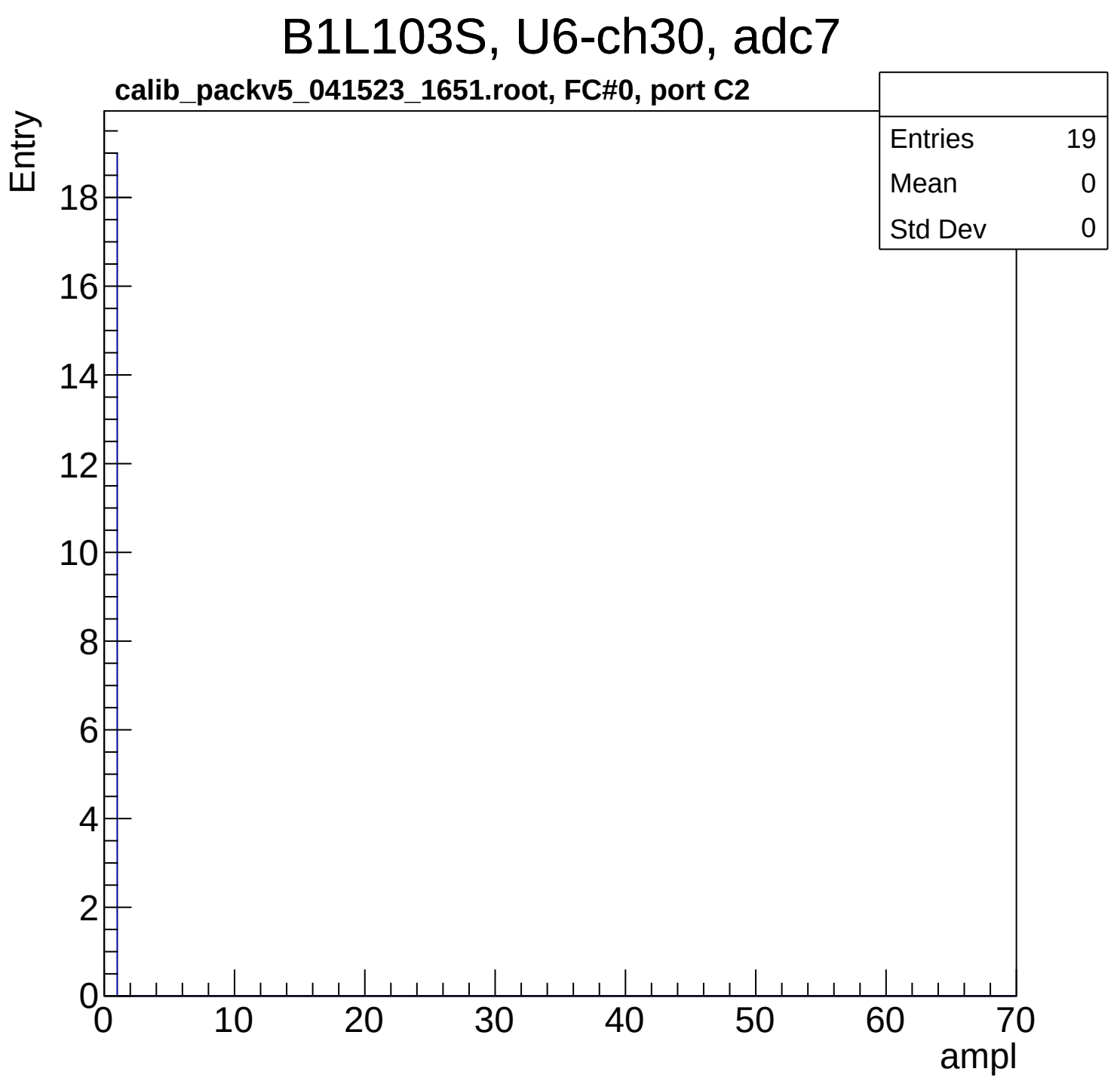
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch30, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 58.48
Std Dev 13.14
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch30, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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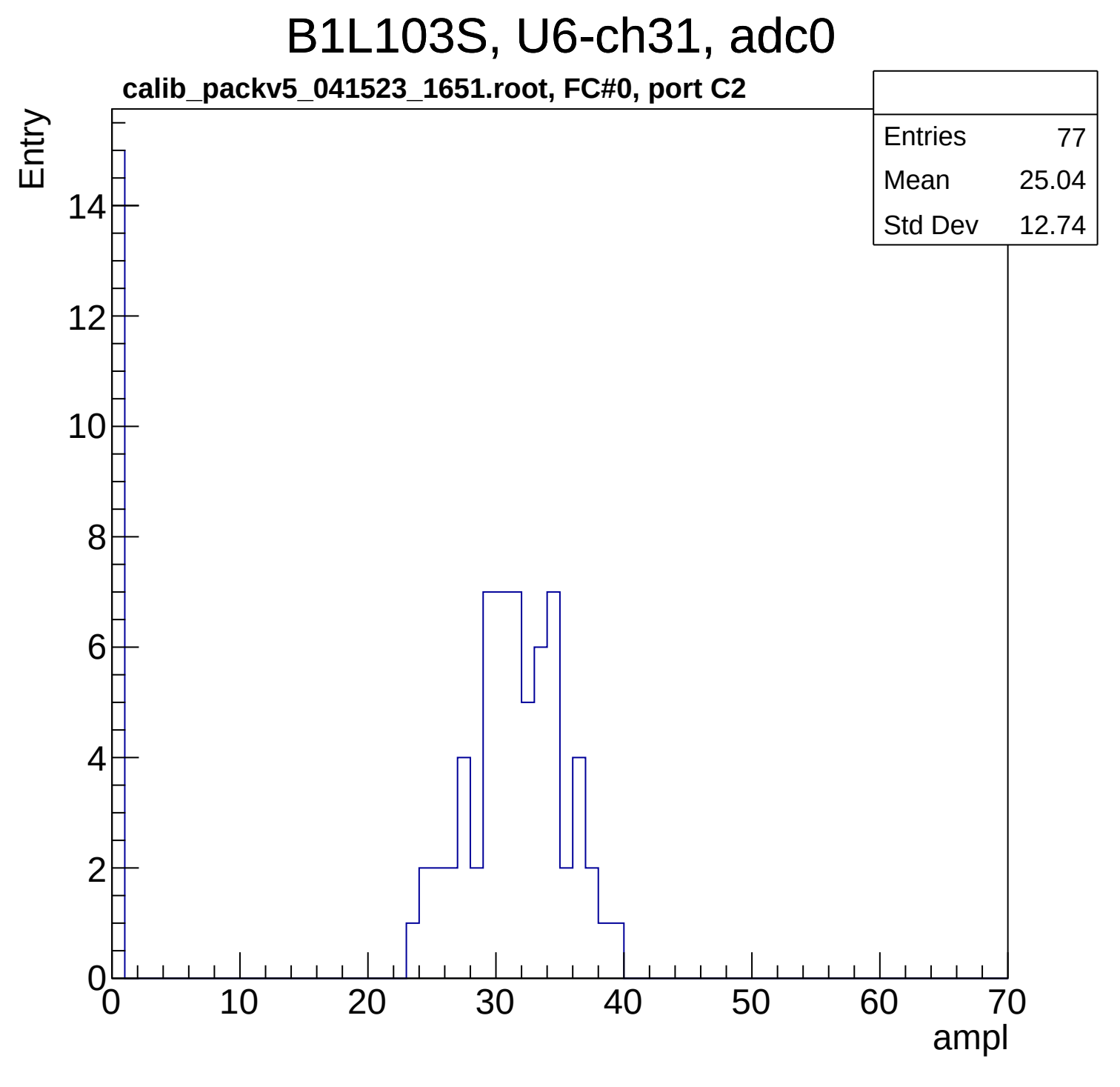
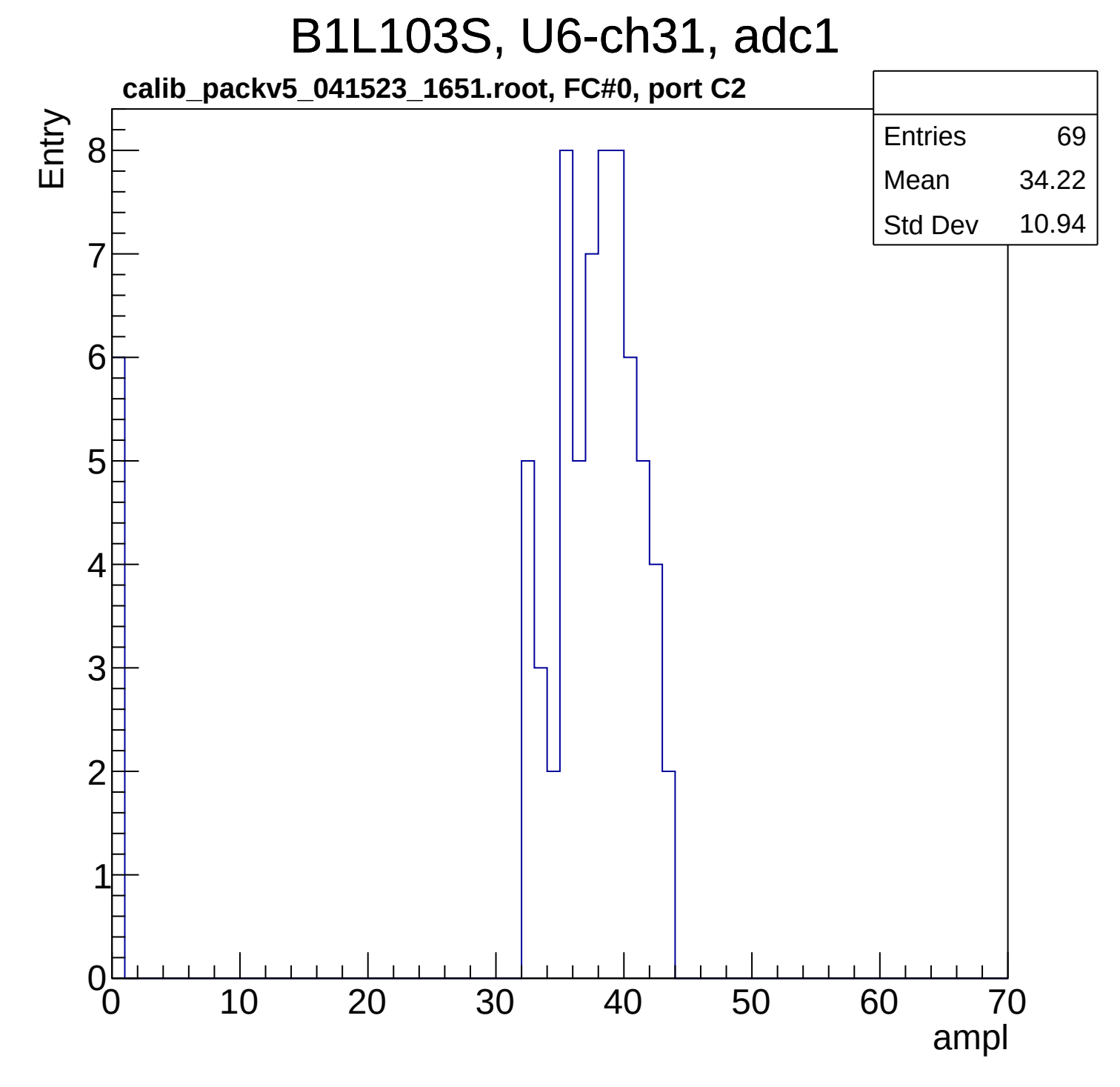
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch31, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 25.04
Std Dev 12.74
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch31, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 34.22
Std Dev 10.94
Entry
ampl
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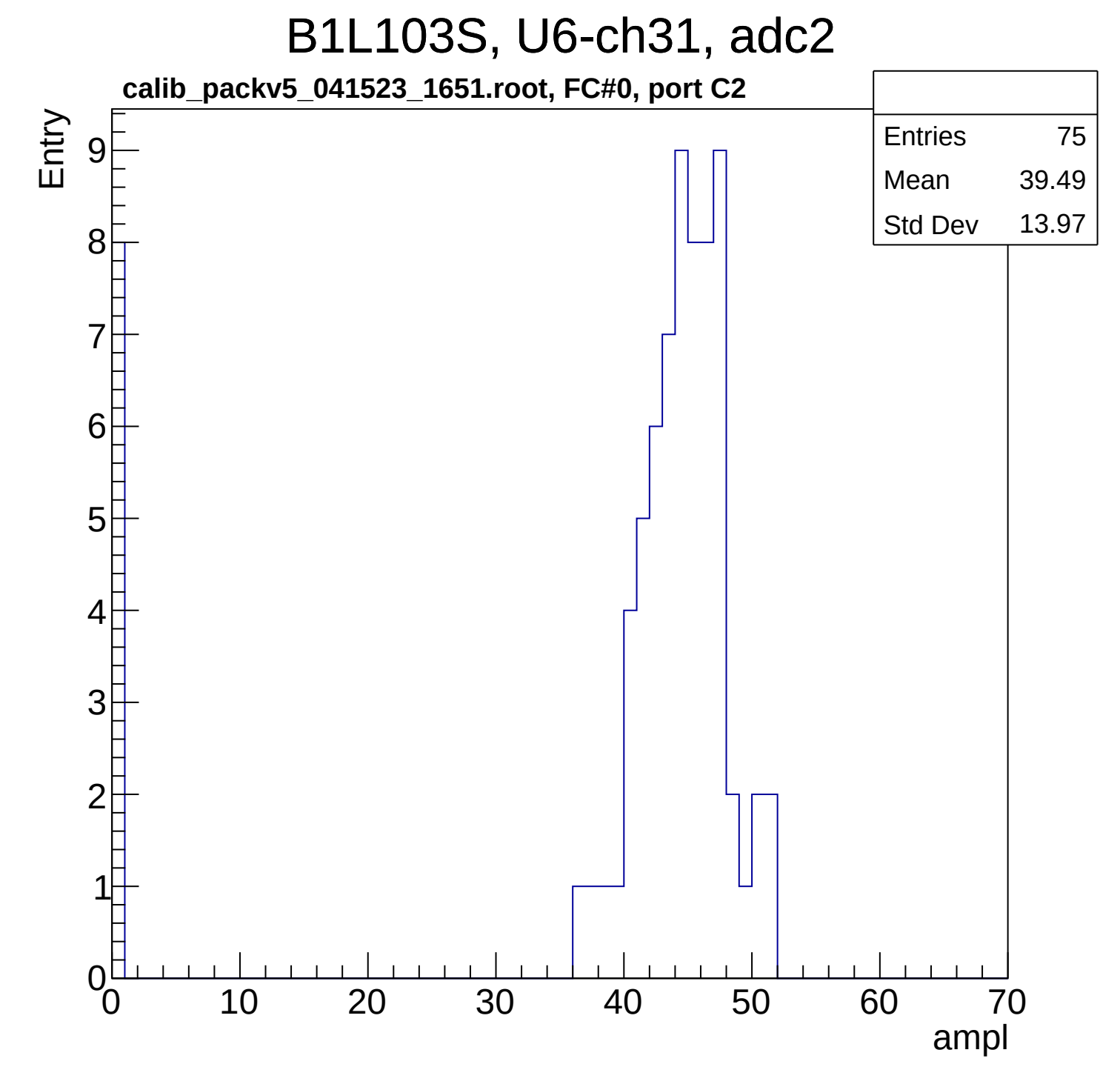
B1L103S, U6-ch31, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 39.49
Std Dev 13.97
Entry
ampl
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0
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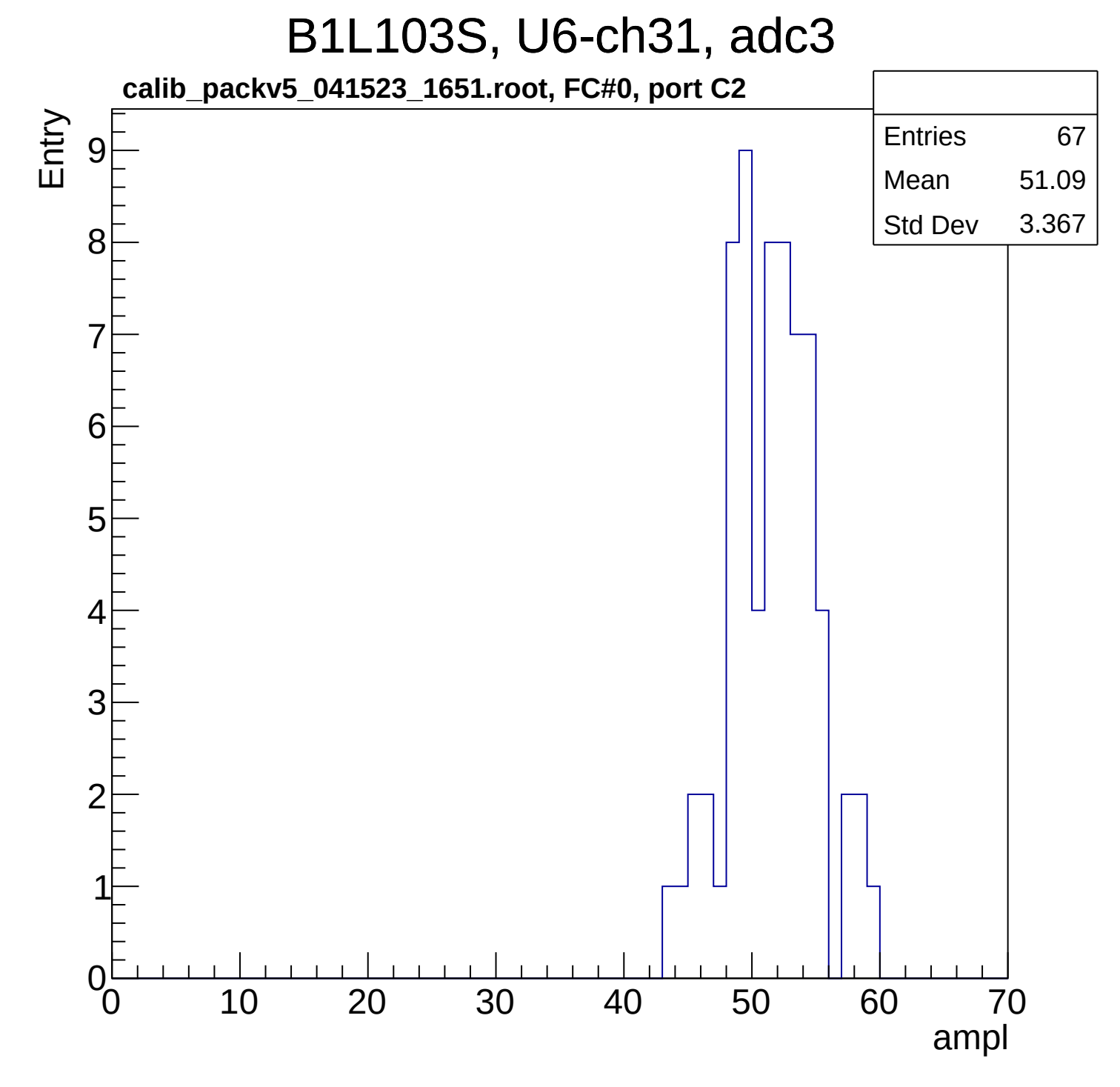
B1L103S, U6-ch31, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 51.09
Std Dev 3.367
Entry
ampl
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3
4
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6
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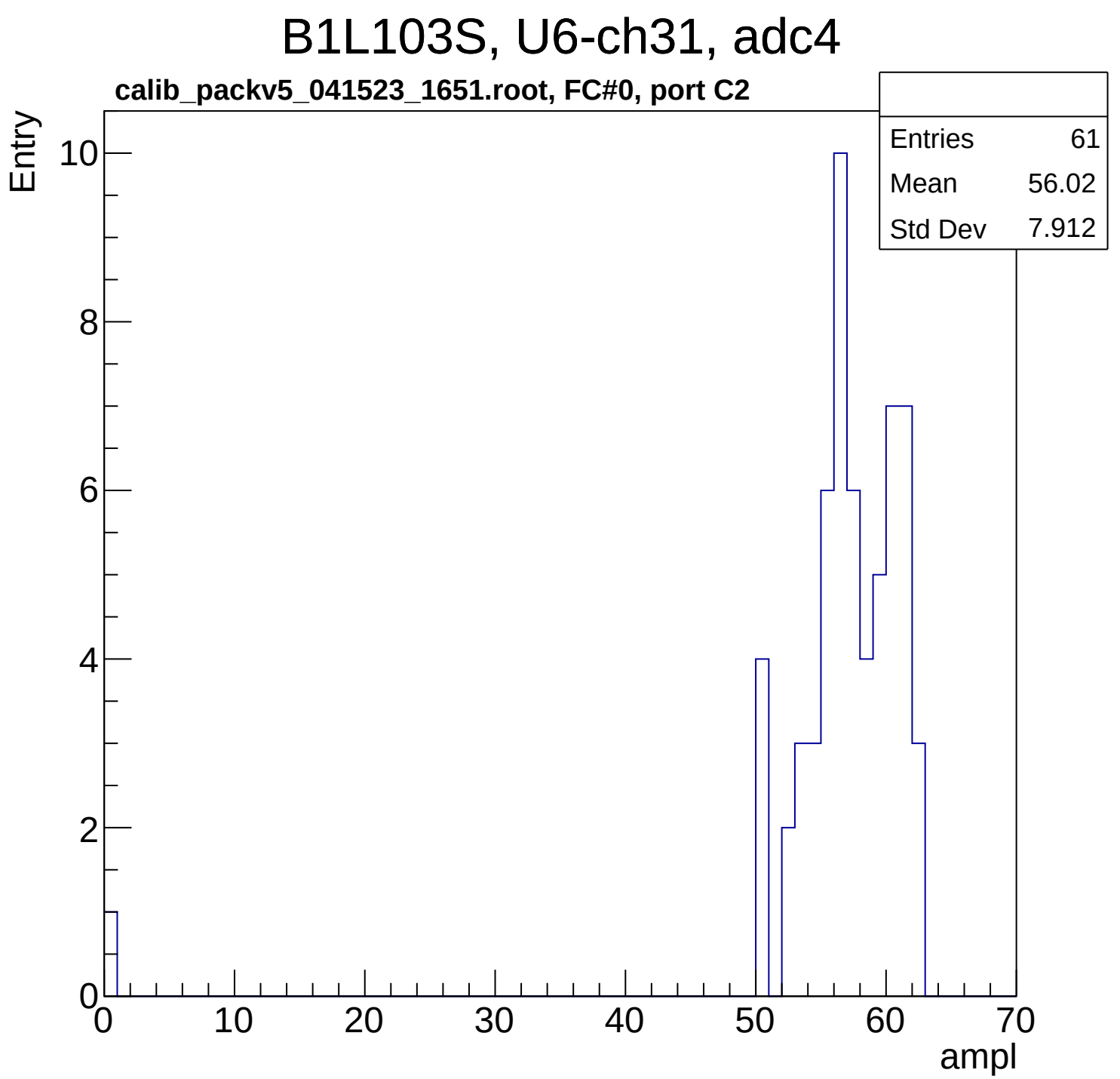
B1L103S, U6-ch31, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 56.02
Std Dev 7.912
Entry
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50
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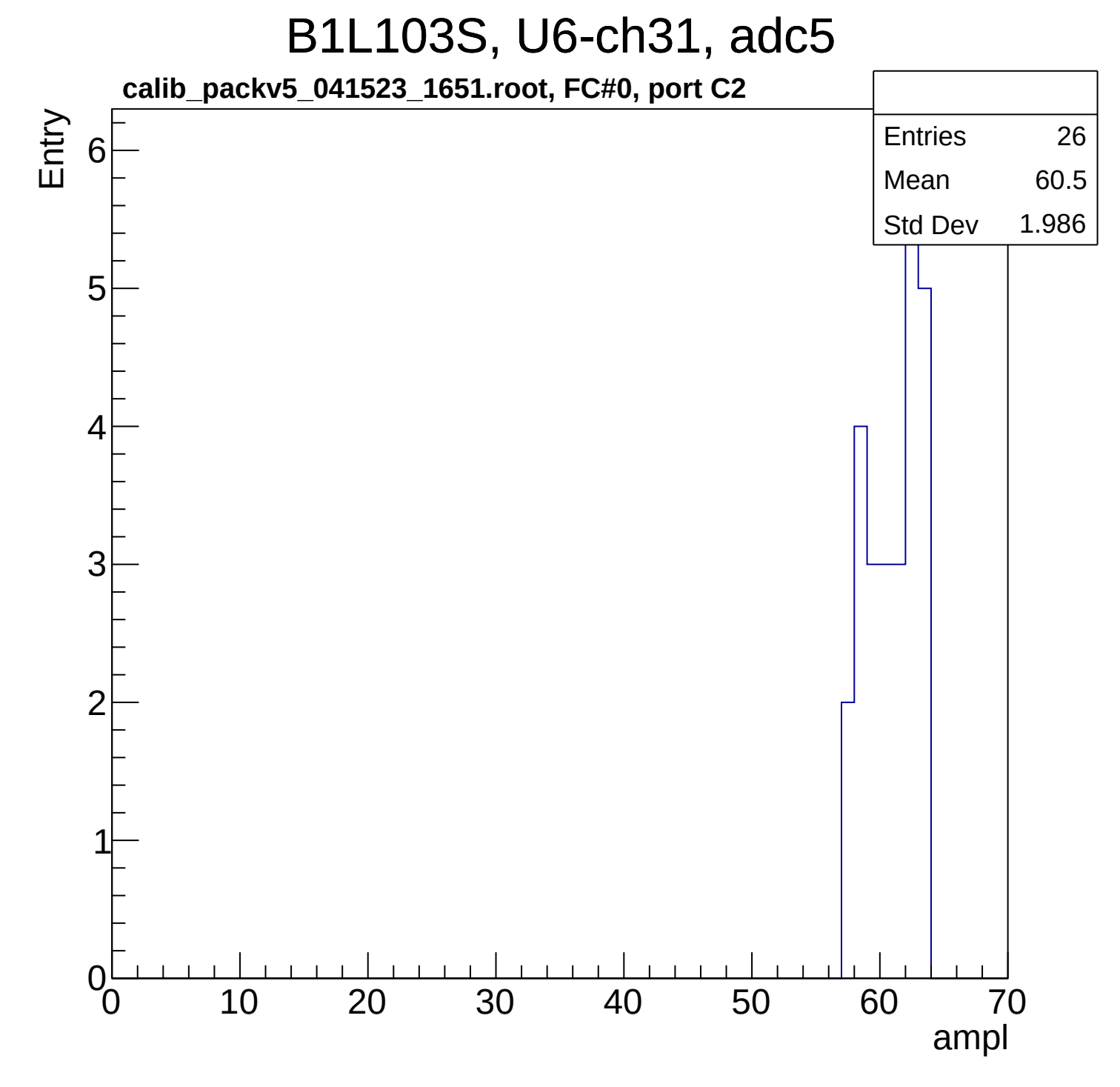
70
ampl


B1L103S, U6-ch31, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 60.5
Std Dev 1.986
Entry
ampl
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1
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0
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40
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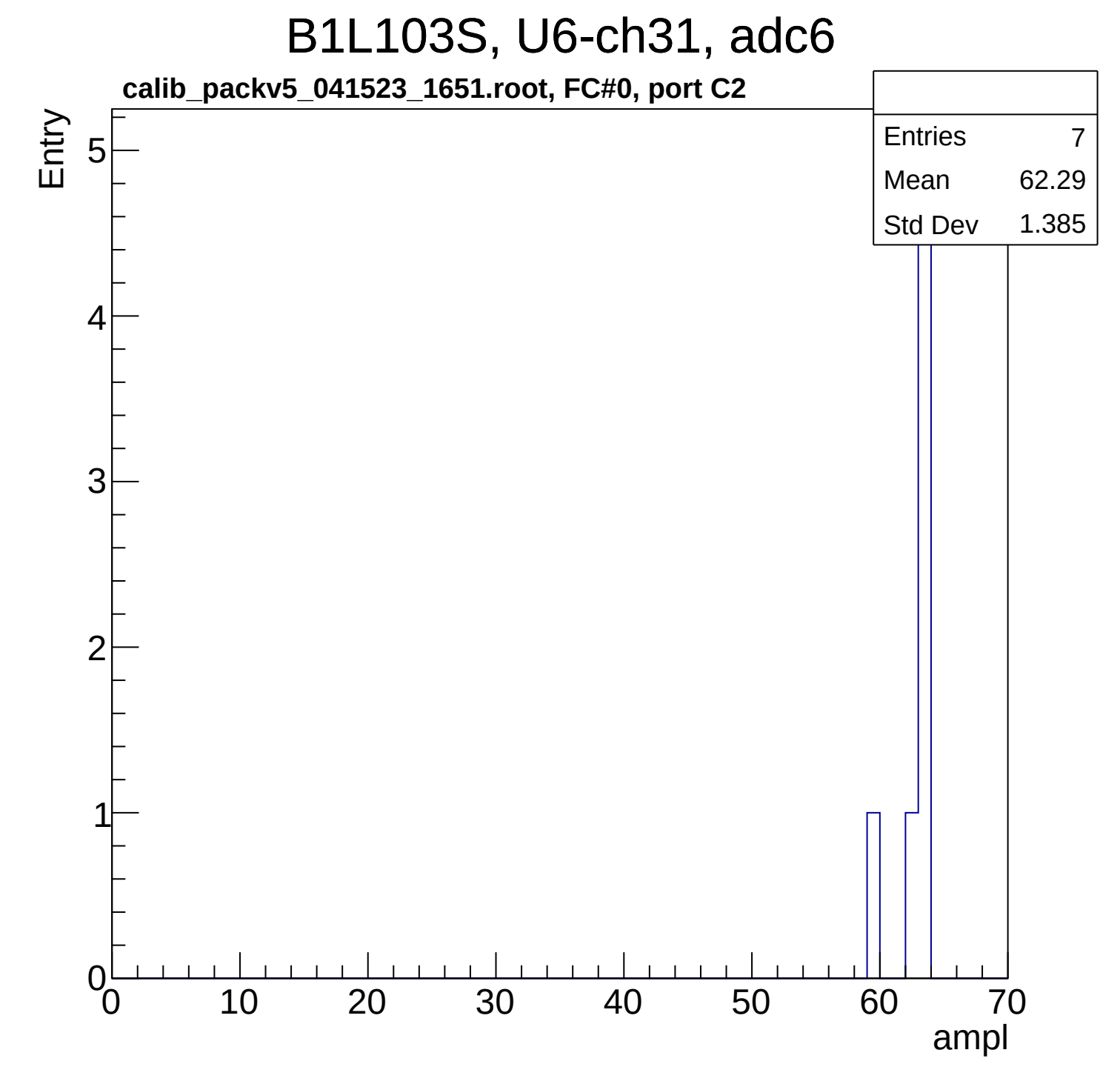
B1L103S, U6-ch31, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 62.29
Std Dev 1.385
Entry
ampl
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2
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0
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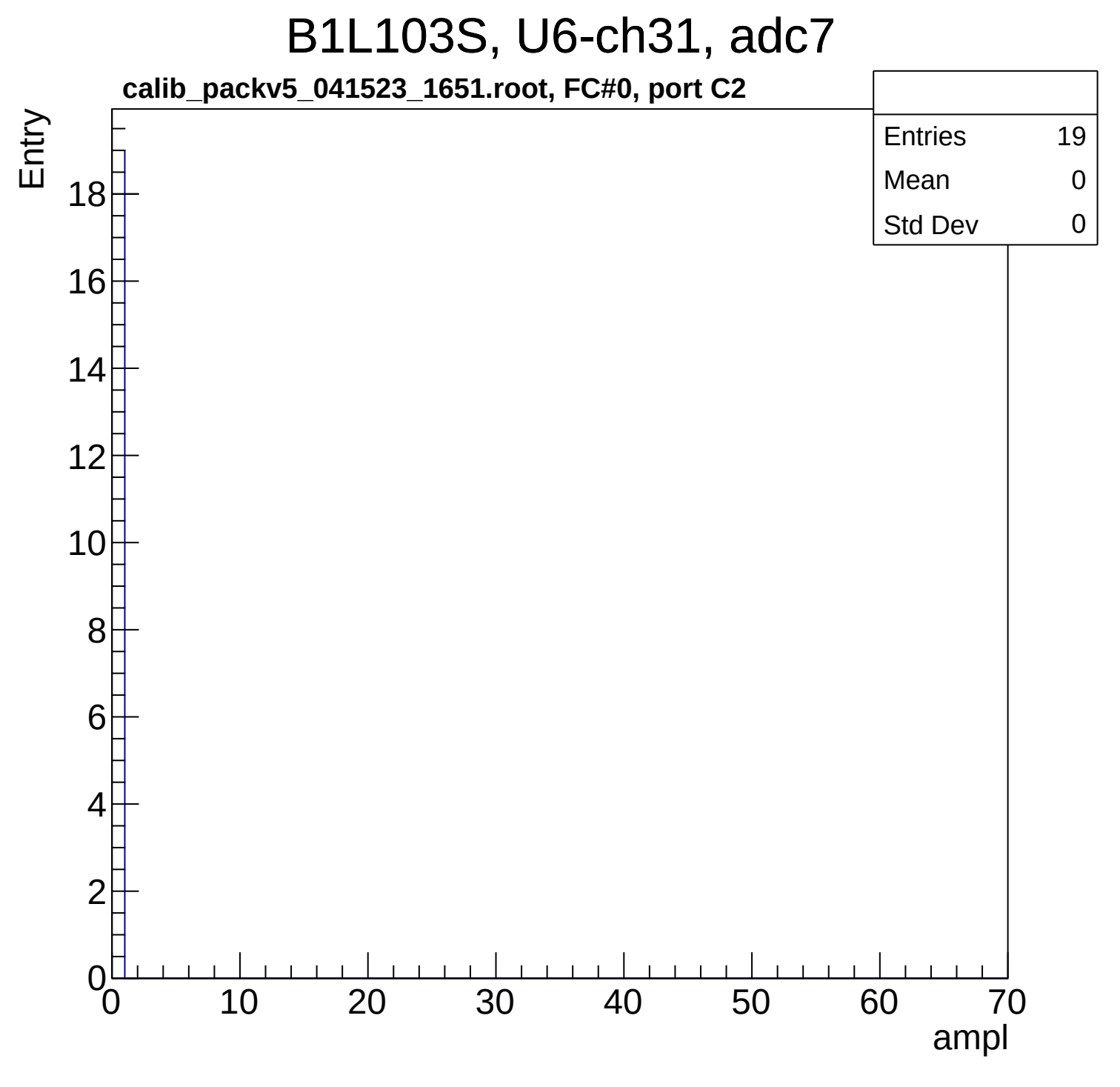
B1L103S, U6-ch31, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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8
10
12
14
16
18
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10
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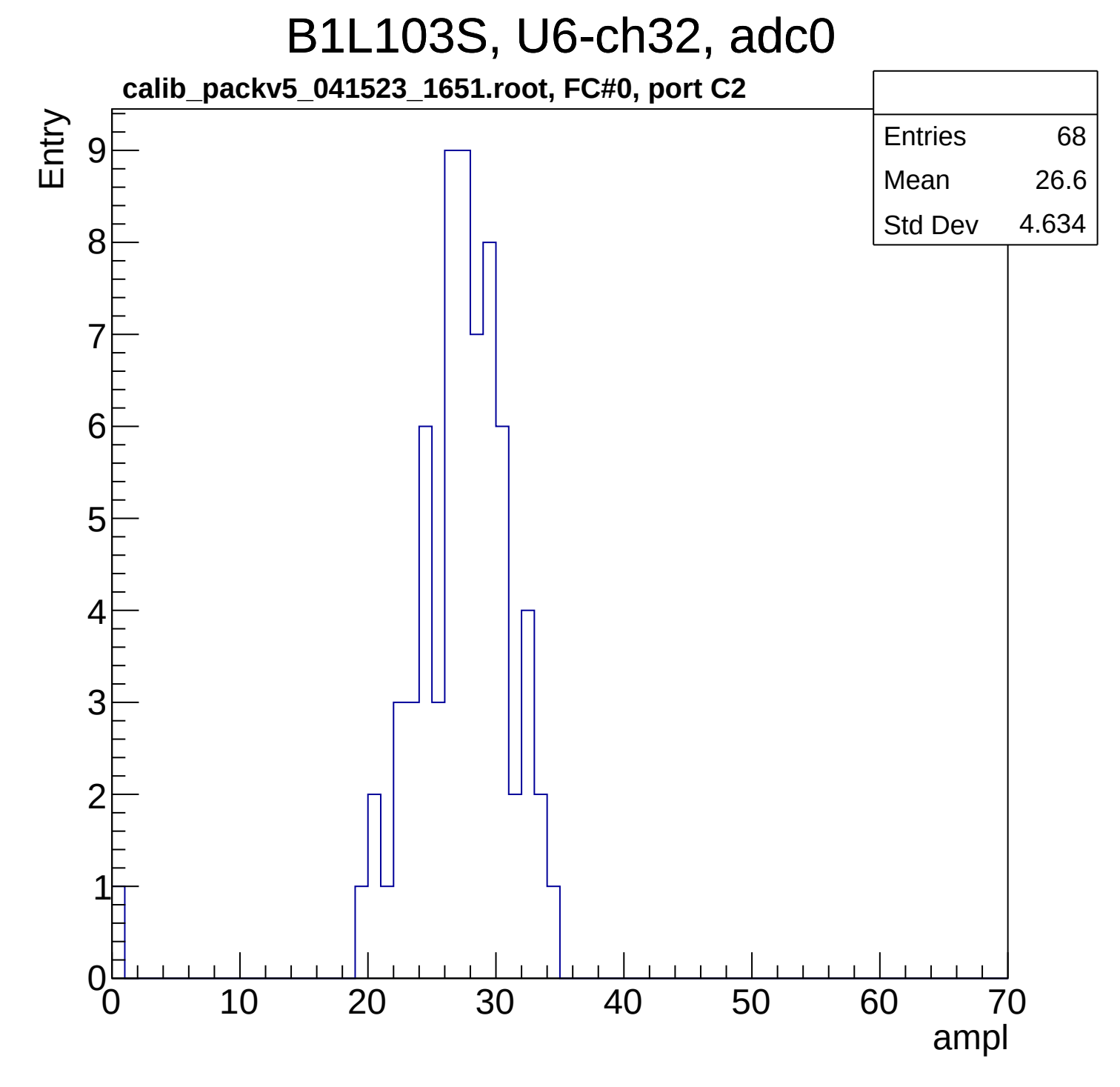
40
50
60
70
ampl


B1L103S, U6-ch32, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 26.6
Std Dev 4.634
Entry
ampl
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4
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6
7
8
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0
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60
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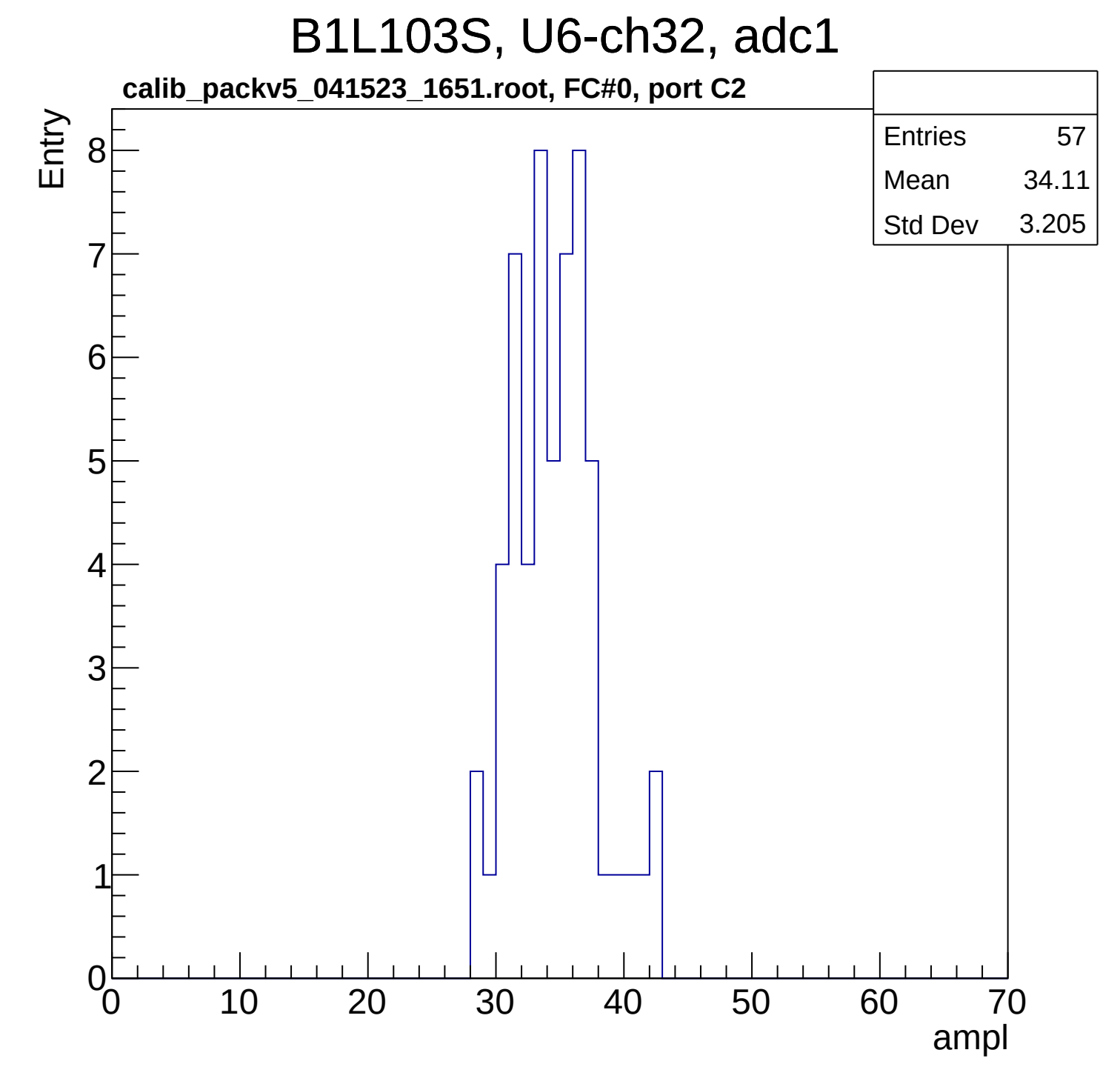
B1L103S, U6-ch32, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 34.11
Std Dev 3.205
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
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60
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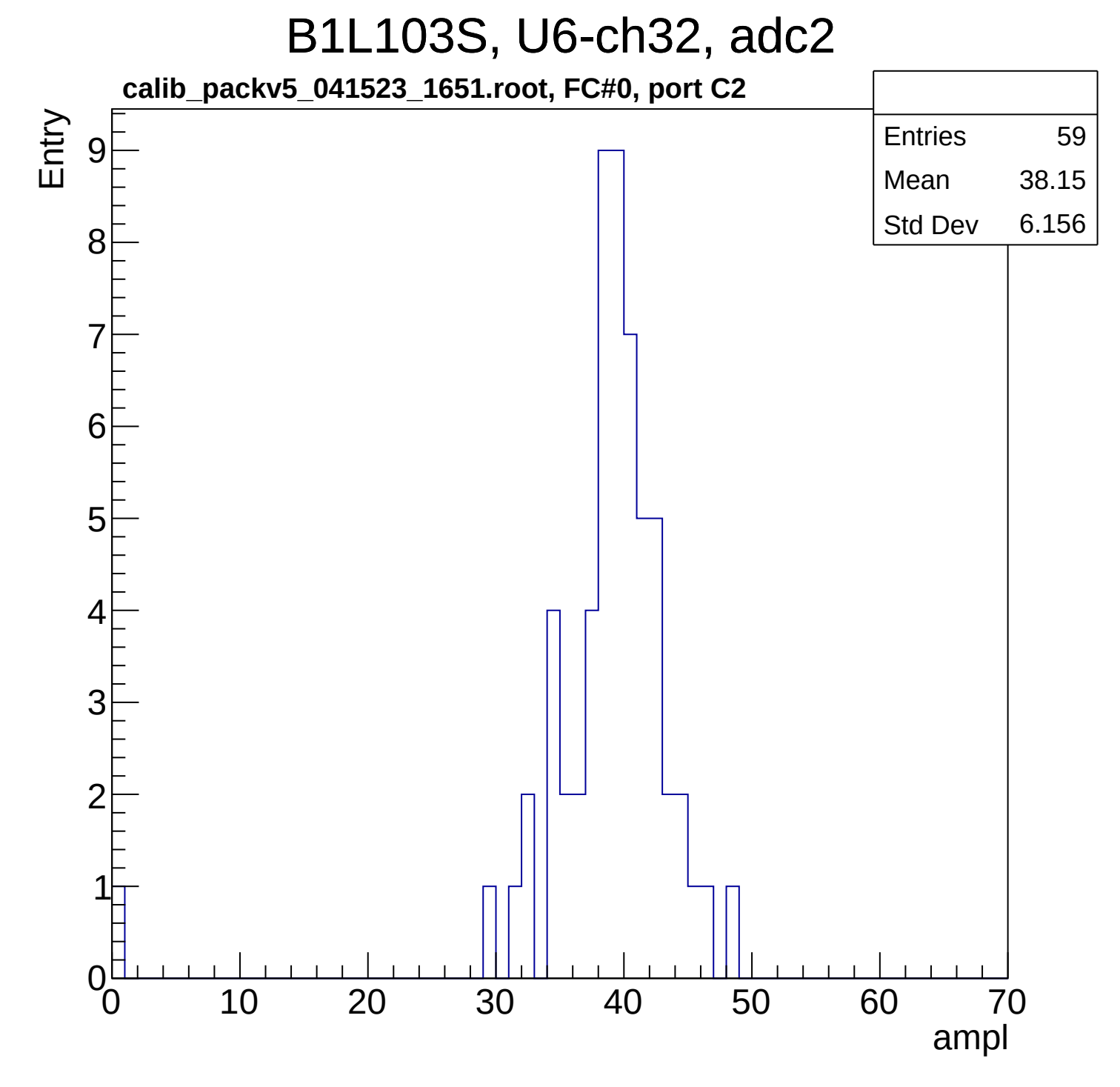
B1L103S, U6-ch32, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 38.15
Std Dev 6.156
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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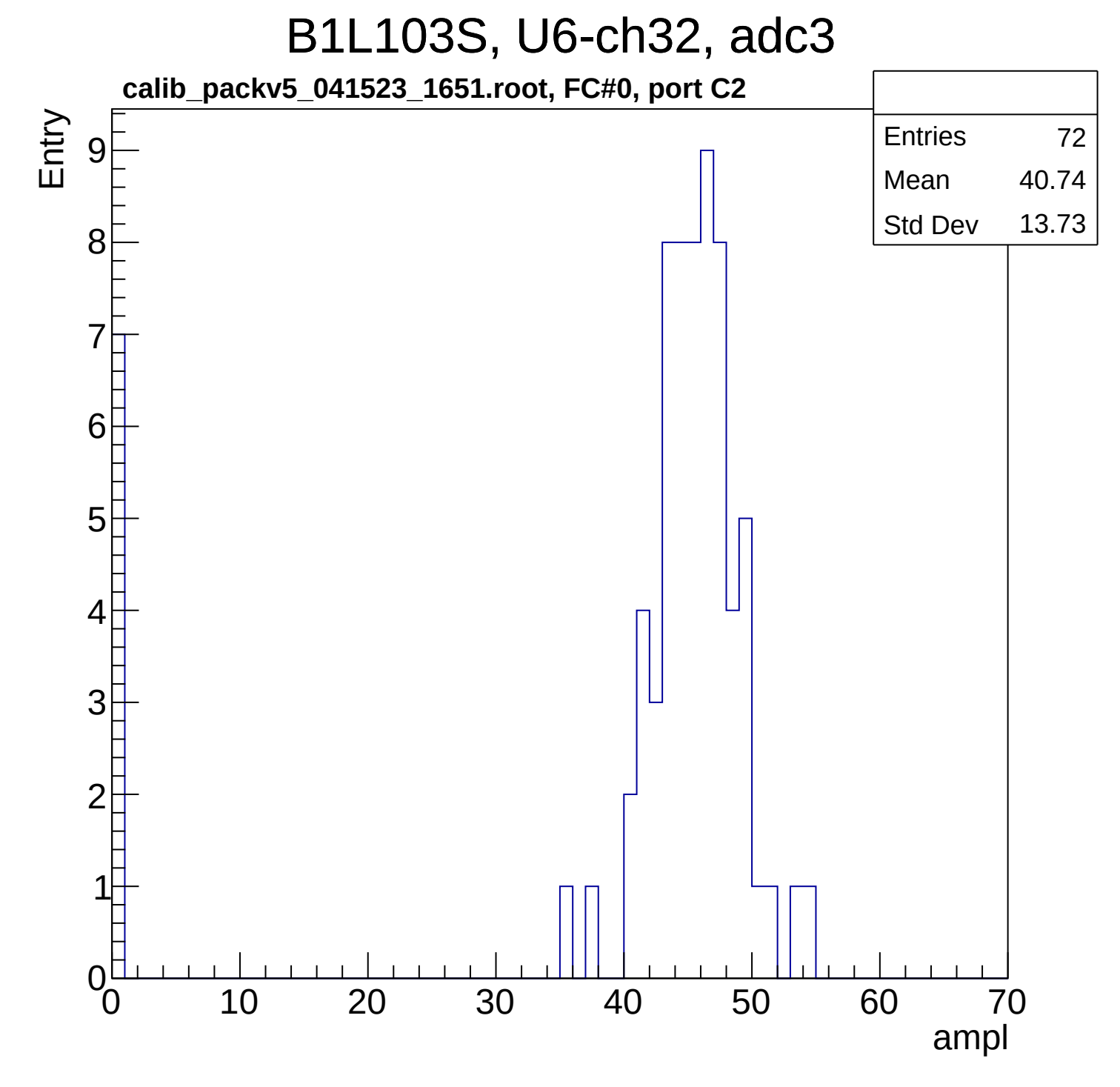
B1L103S, U6-ch32, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 40.74
Std Dev 13.73
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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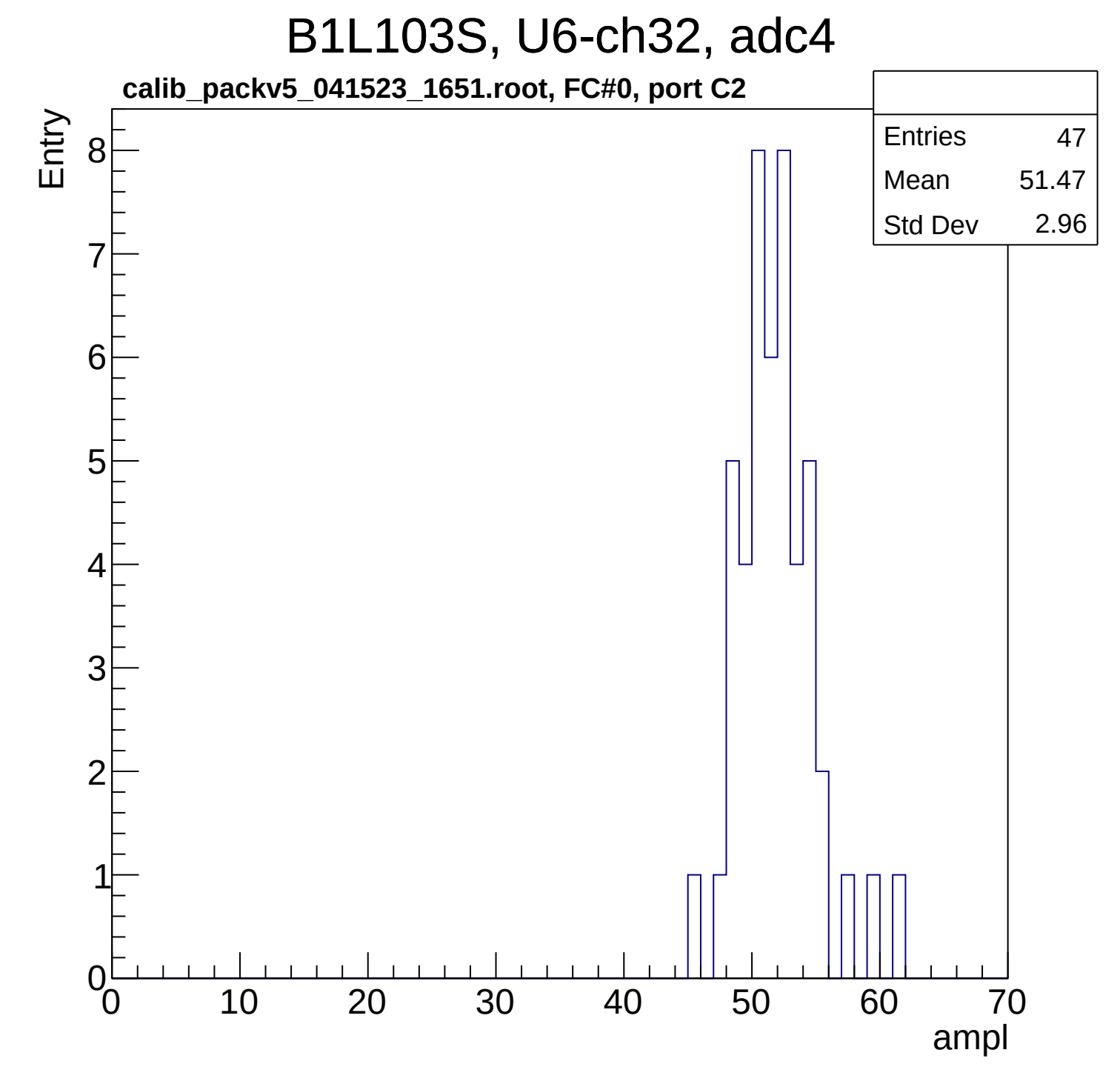
B1L103S, U6-ch32, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 51.47
Std Dev 2.96
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
50
60
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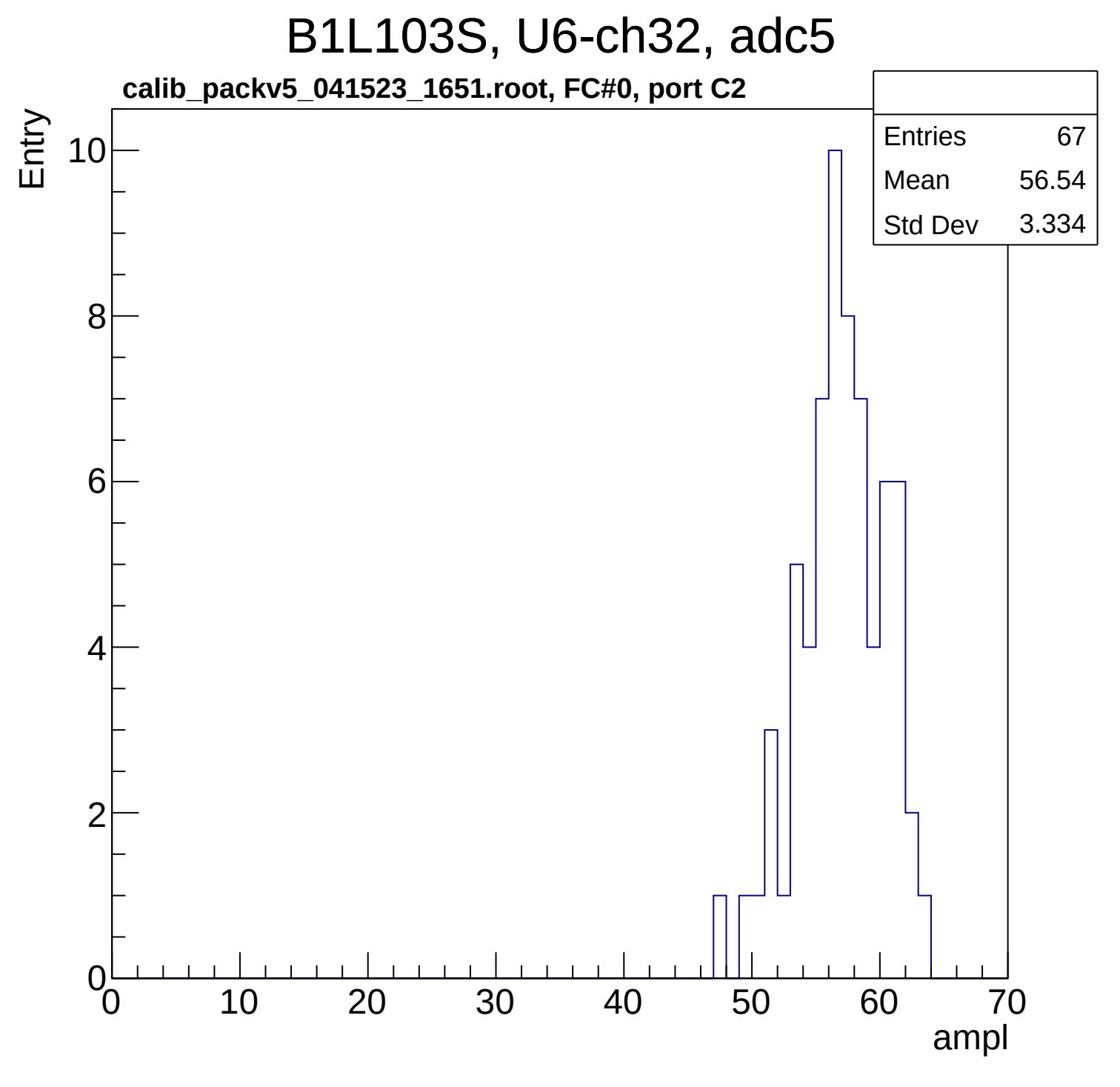
B1L103S, U6-ch32, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 56.54
Std Dev 3.334
Entry
ampl
0
2
4
6
8
10
0
10
20
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40
50
60
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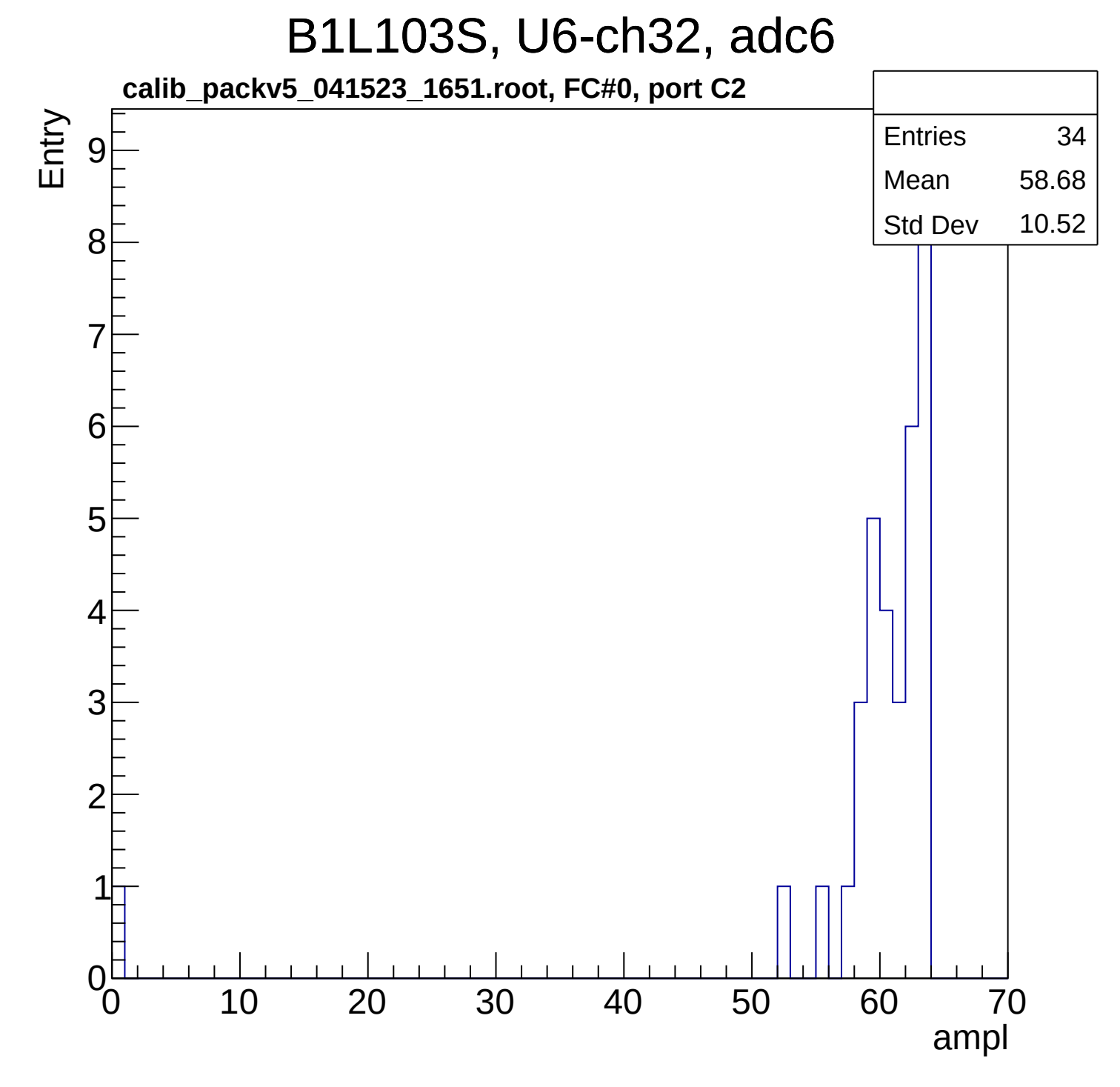
B1L103S, U6-ch32, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 58.68
Std Dev 10.52
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
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60
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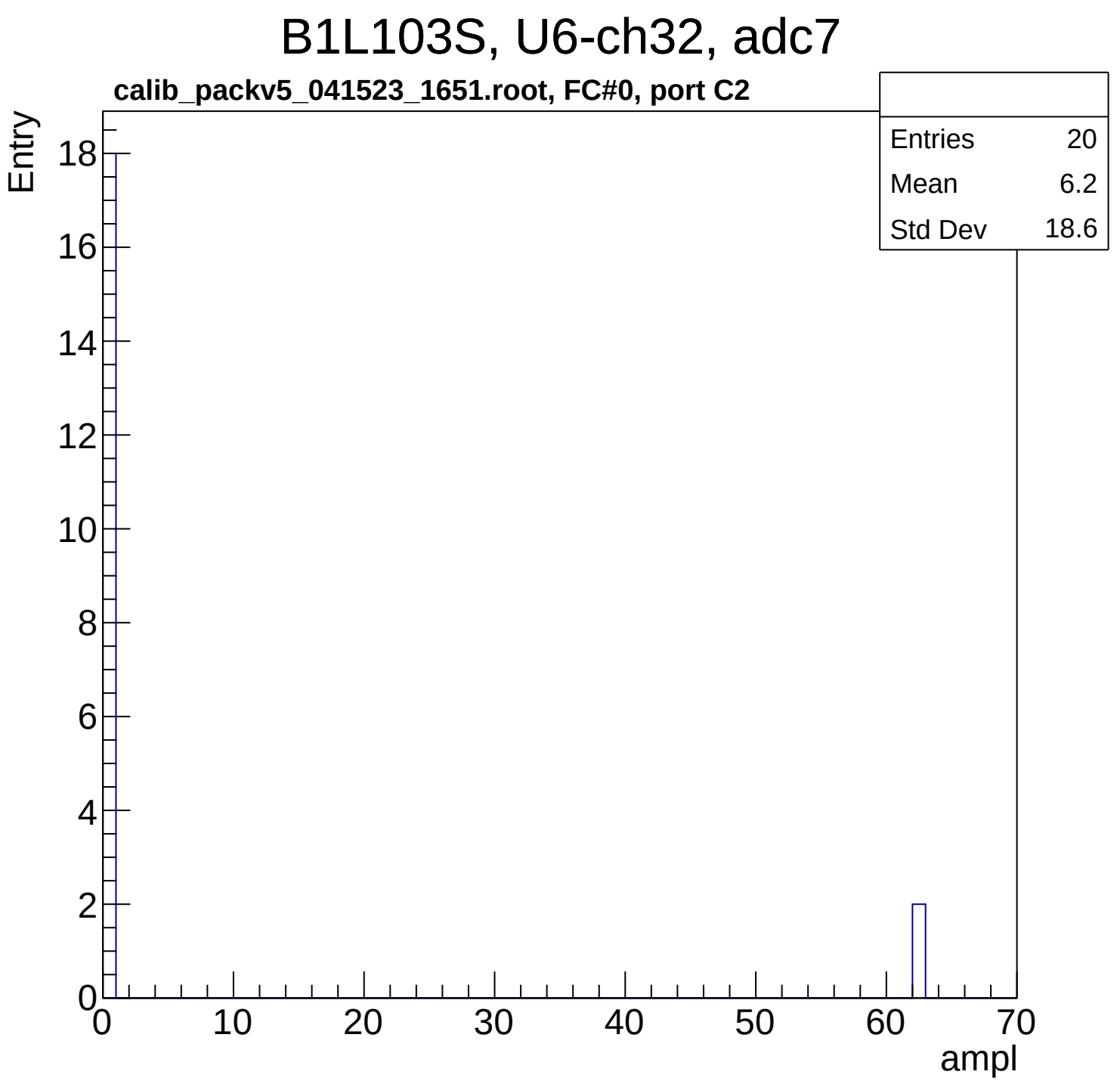
B1L103S, U6-ch32, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 6.2
Std Dev 18.6
Entry
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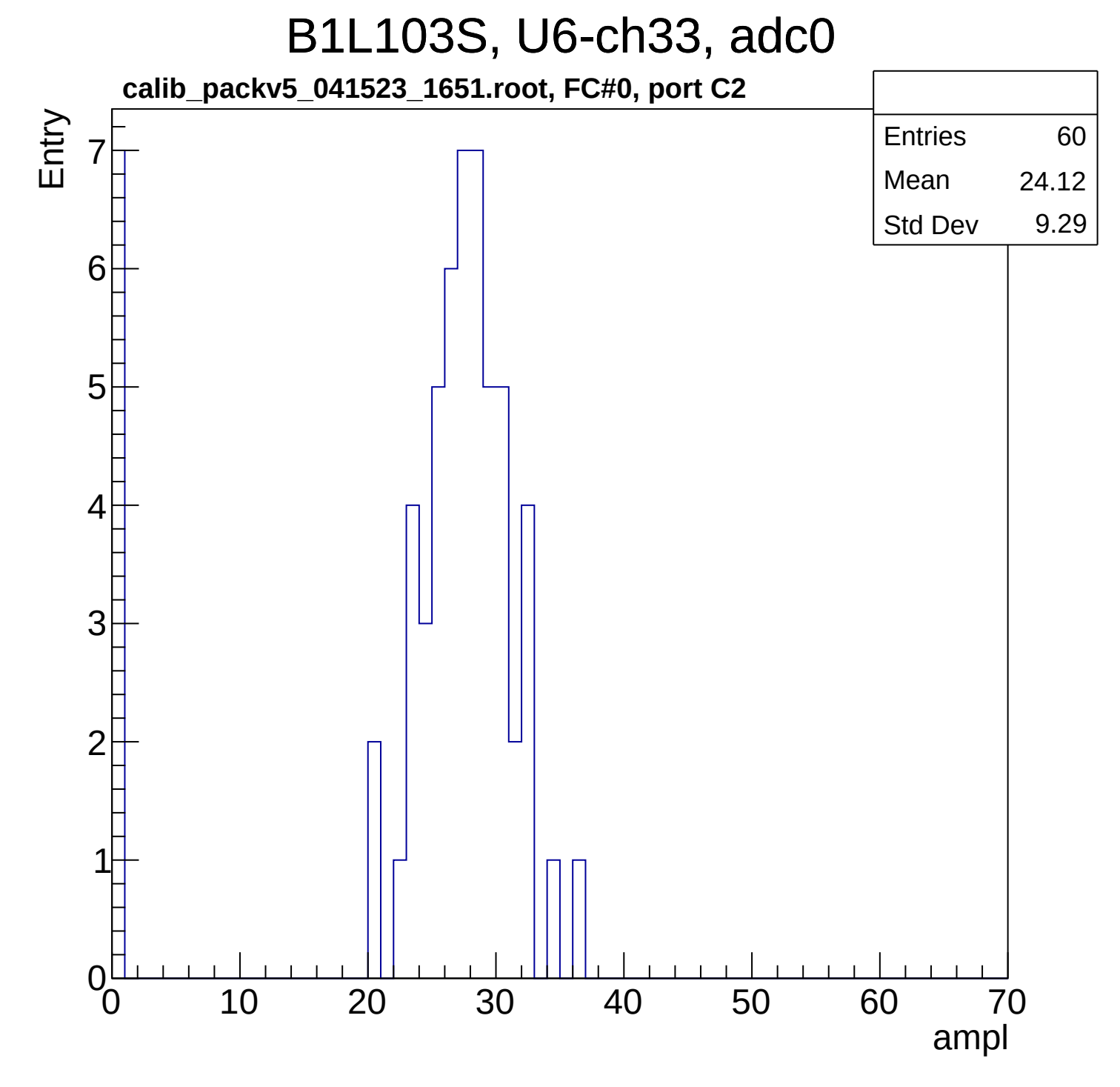
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch33, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 24.12
Std Dev 9.29
Entry
ampl
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2
3
4
5
6
7
0
10
20
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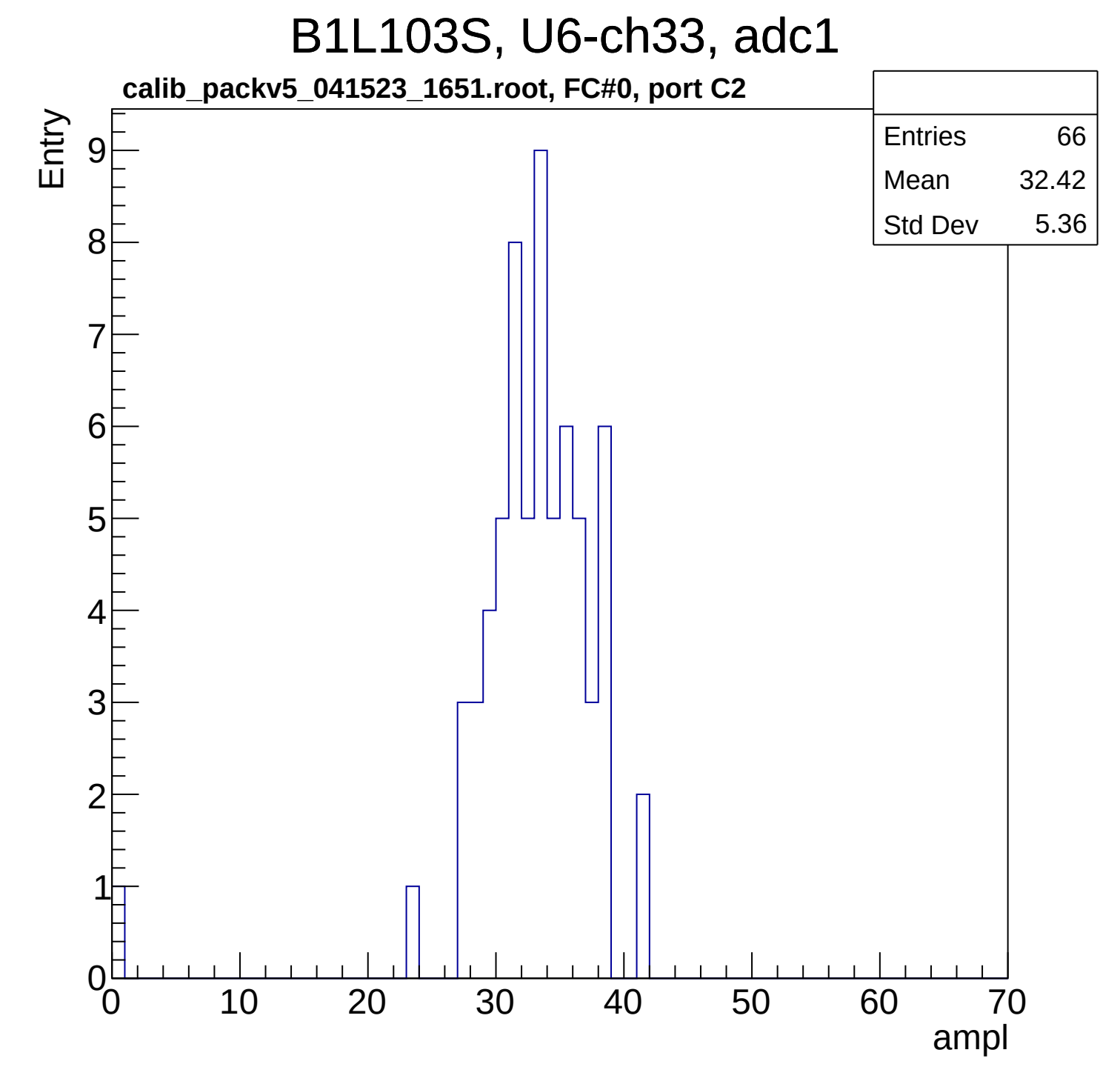
40
50
60
70


B1L103S, U6-ch33, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 32.42
Std Dev 5.36
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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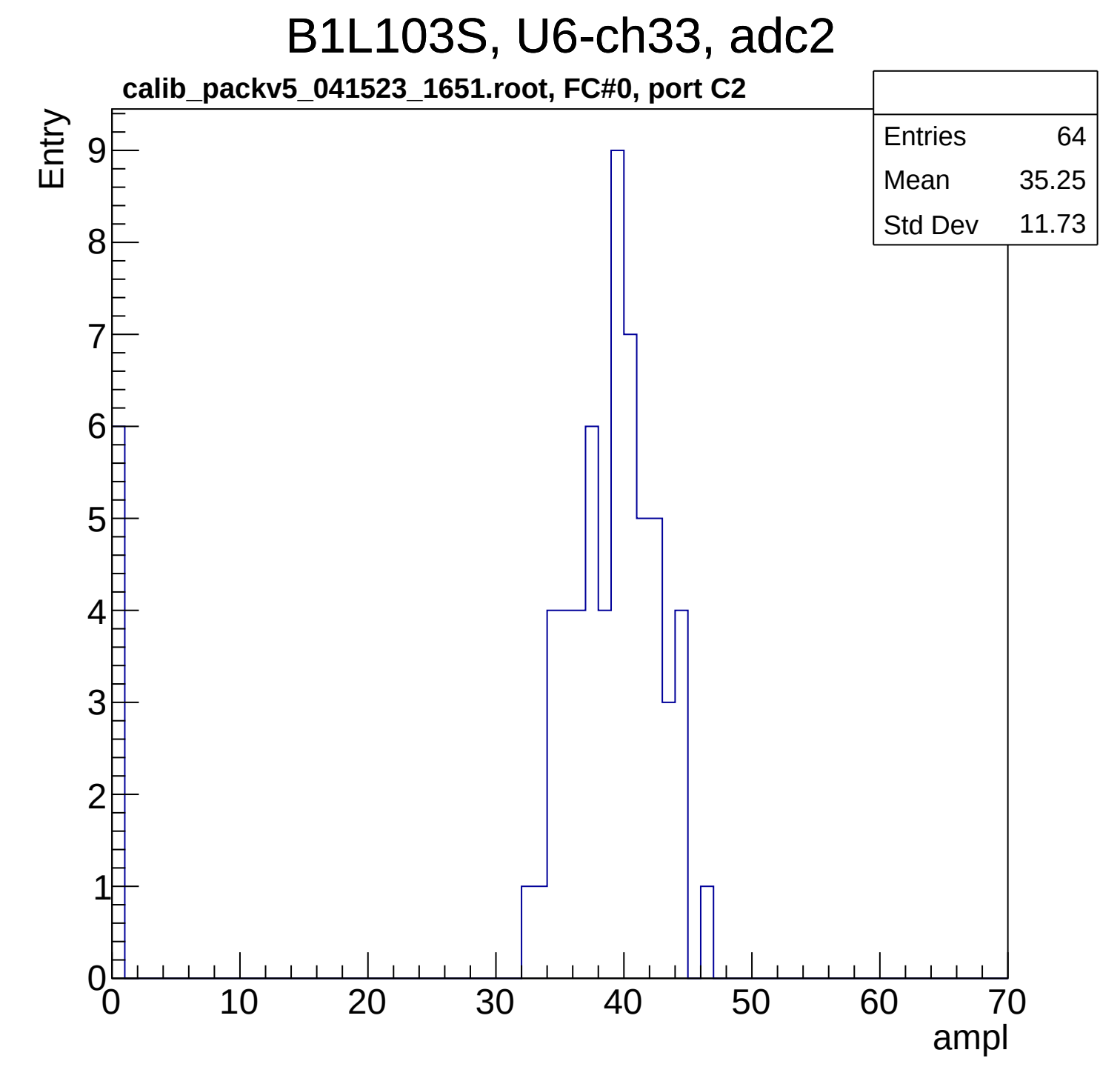
B1L103S, U6-ch33, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 35.25
Std Dev 11.73
Entry
ampl
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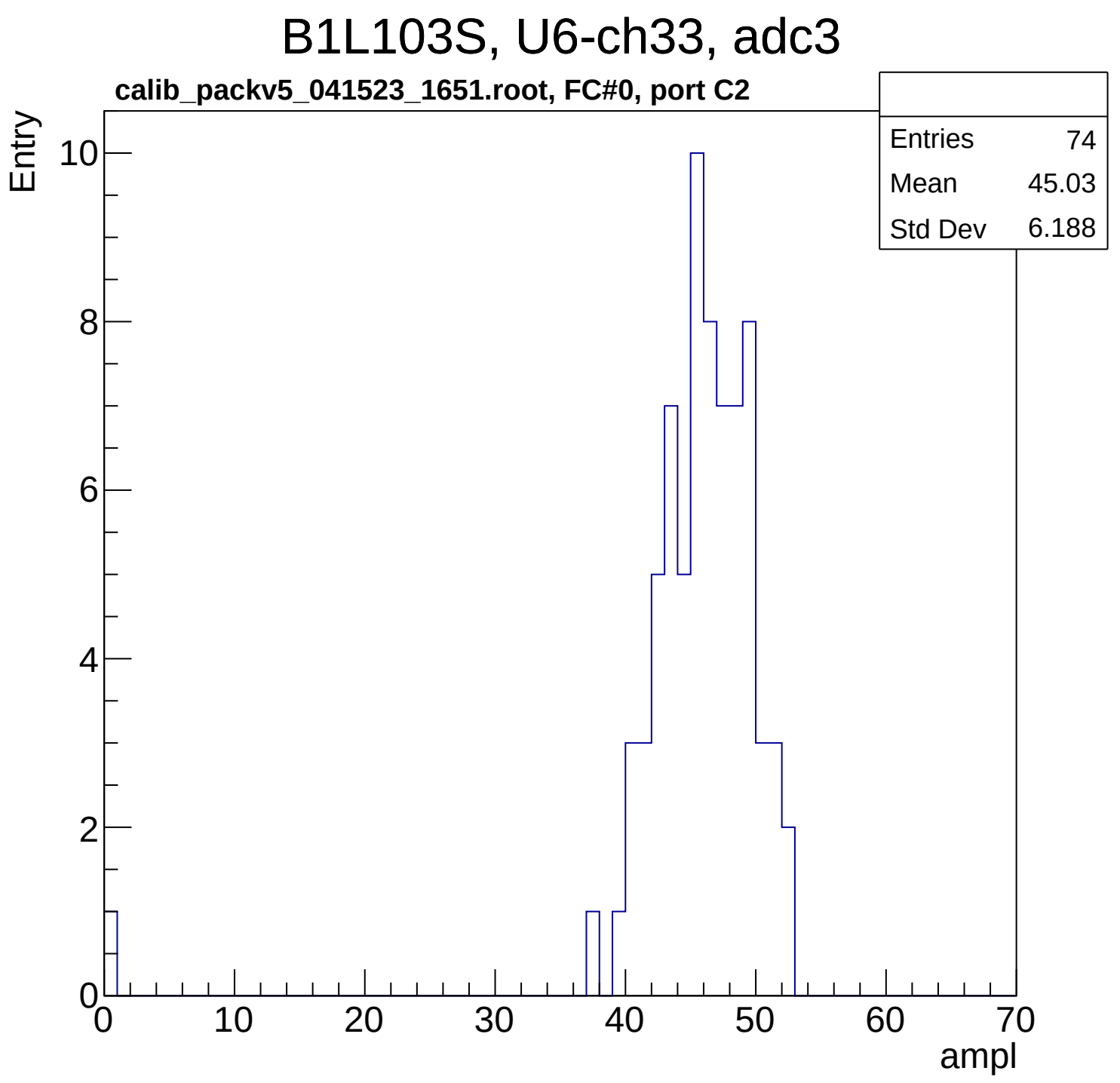
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch33, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 45.03
Std Dev 6.188
Entry
ampl
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4
6
8
10
0
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20
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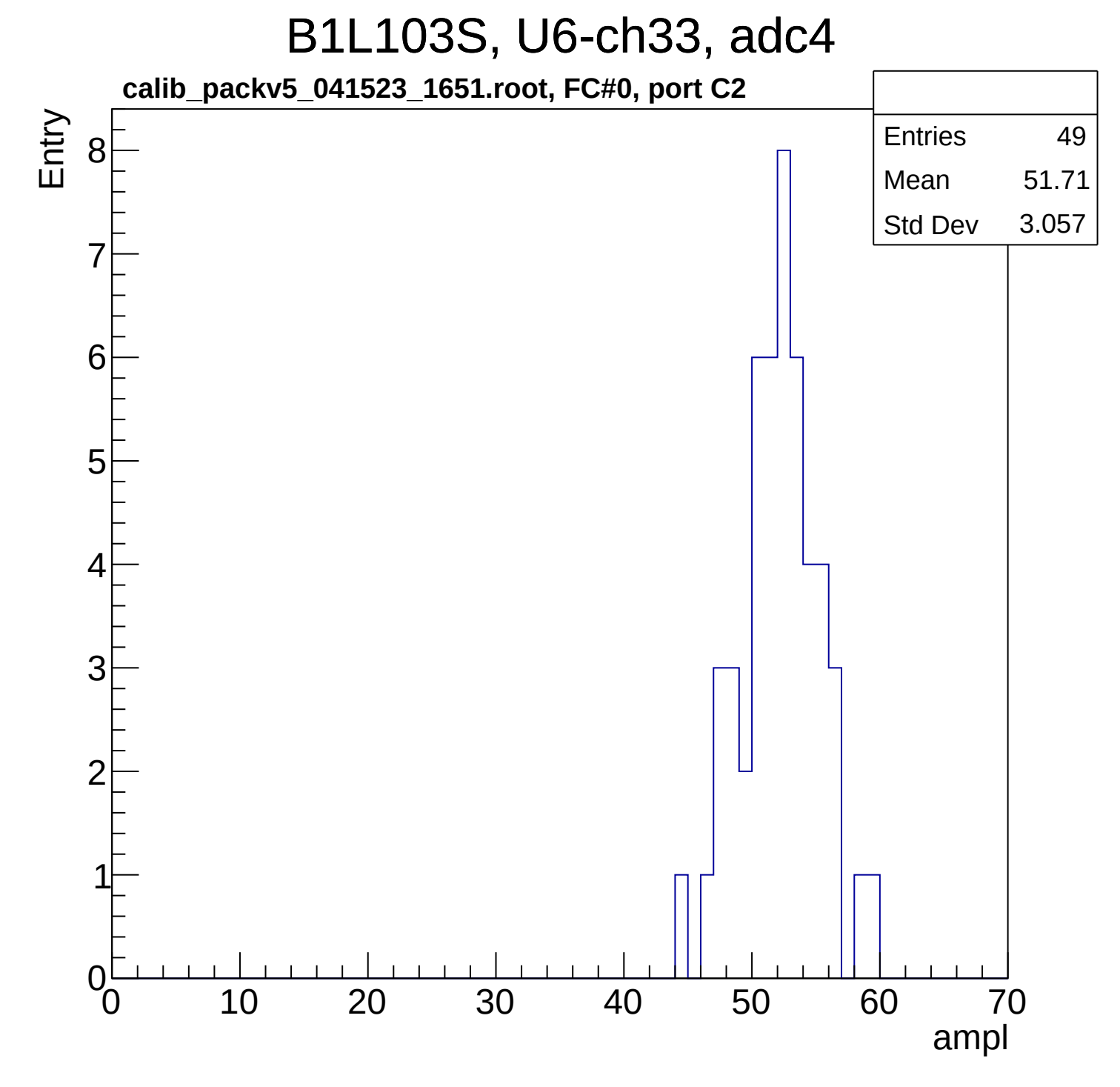
B1L103S, U6-ch33, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 51.71
Std Dev 3.057
Entry
ampl
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2
3
4
5
6
7
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0
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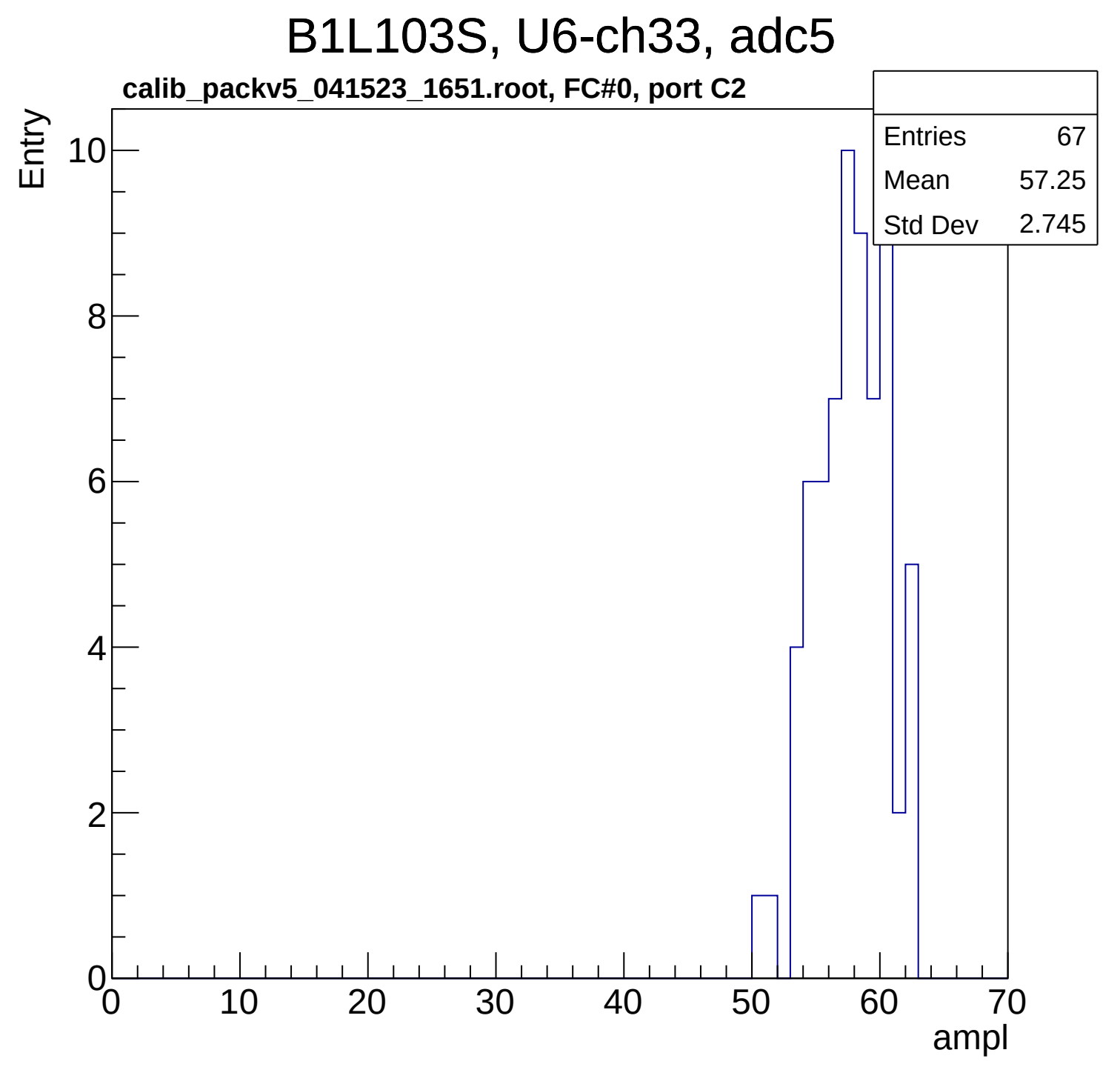
B1L103S, U6-ch33, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 57.25
Std Dev 2.745
Entry
ampl
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2
4
6
8
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0
10
20
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40
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60
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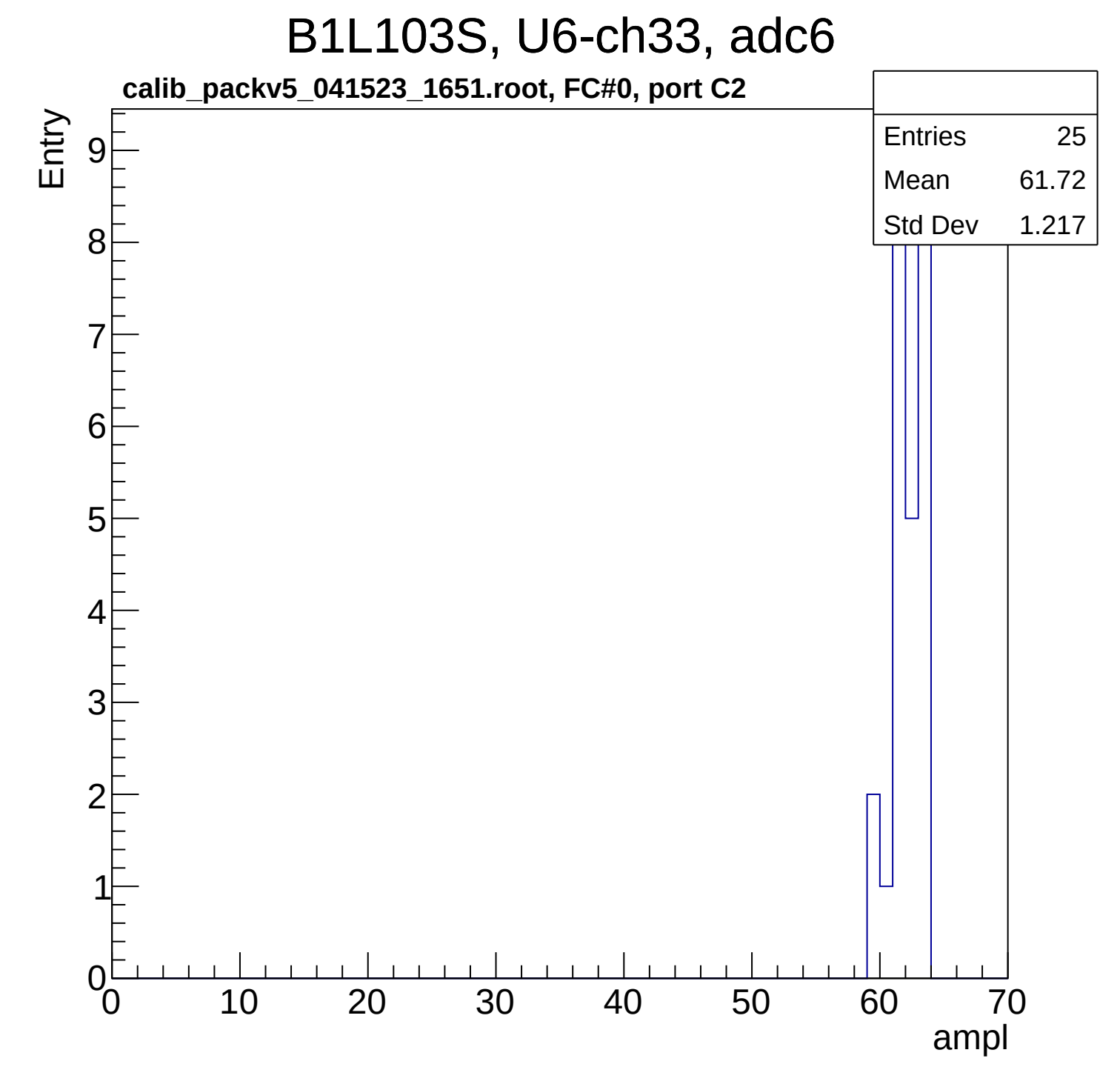
B1L103S, U6-ch33, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 61.72
Std Dev 1.217
Entry
ampl
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2
3
4
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6
7
8
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0
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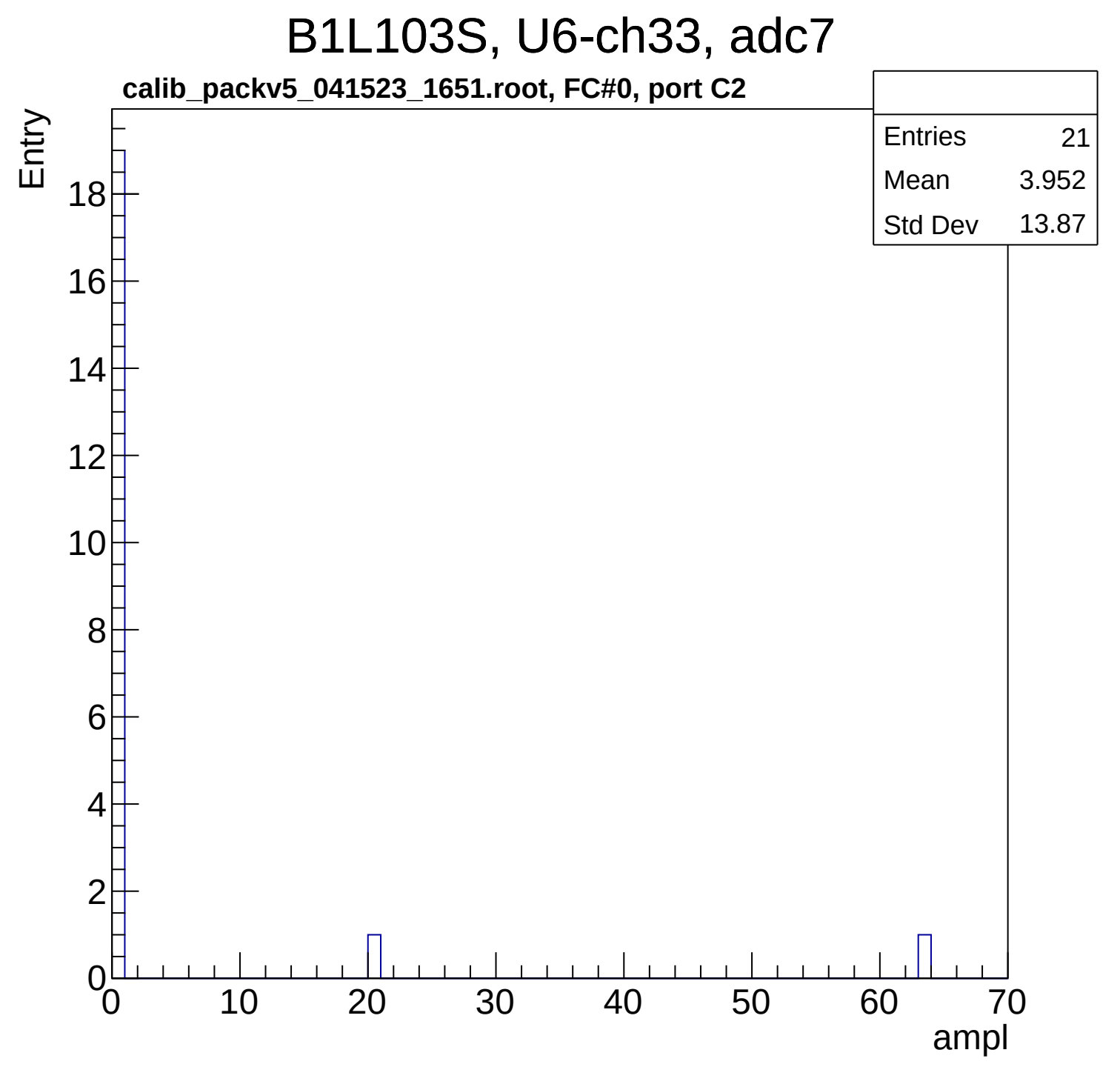
B1L103S, U6-ch33, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 3.952
Std Dev 13.87
Entry
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6
8
10
12
14
16
18
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10
20
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50
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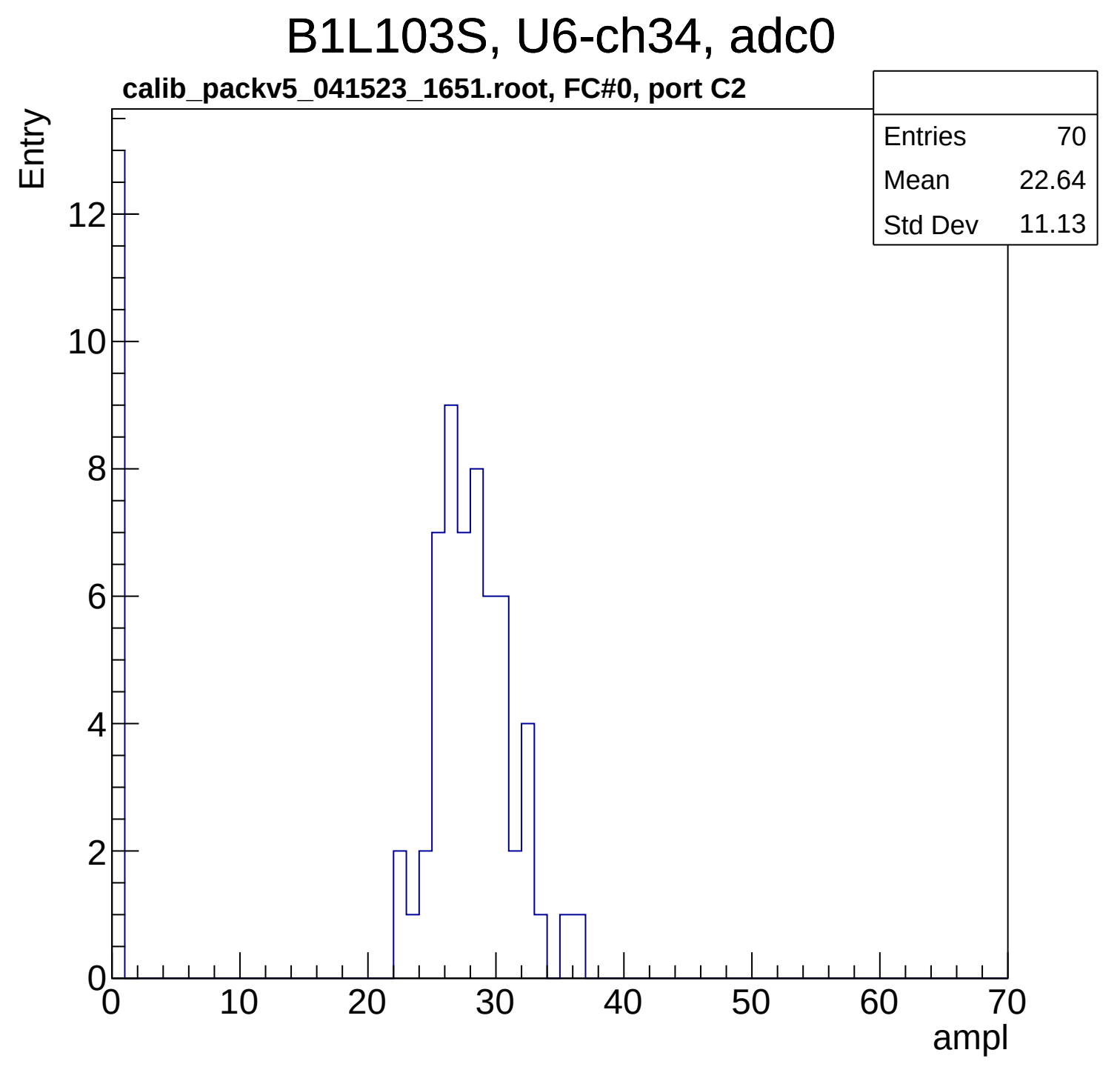
70
ampl


B1L103S, U6-ch34, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 22.64
Std Dev 11.13
Entry
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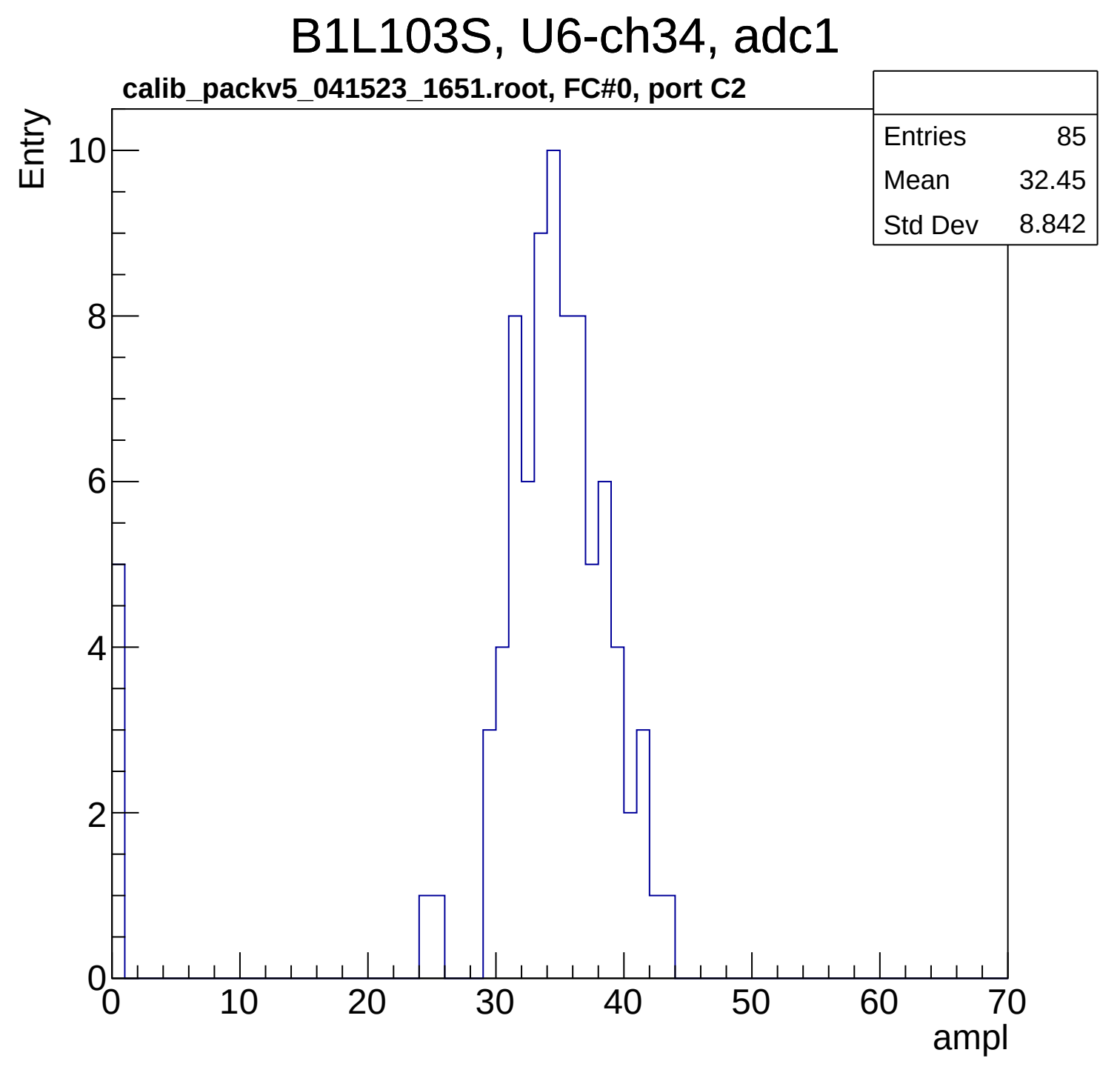
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch34, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 32.45
Std Dev 8.842
Entry
ampl
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0
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60
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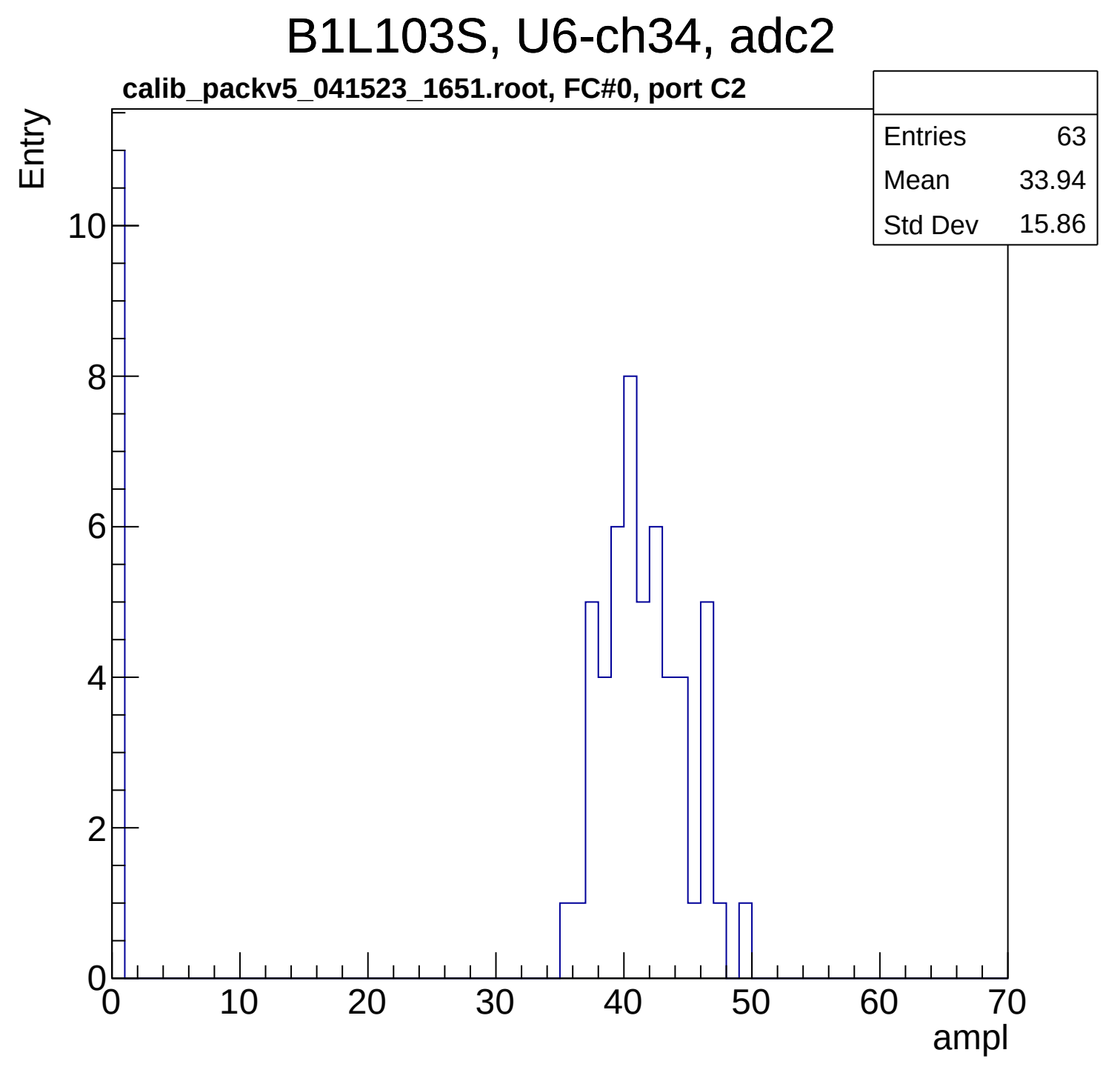
B1L103S, U6-ch34, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 33.94
Std Dev 15.86
Entry
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10
0
10
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30
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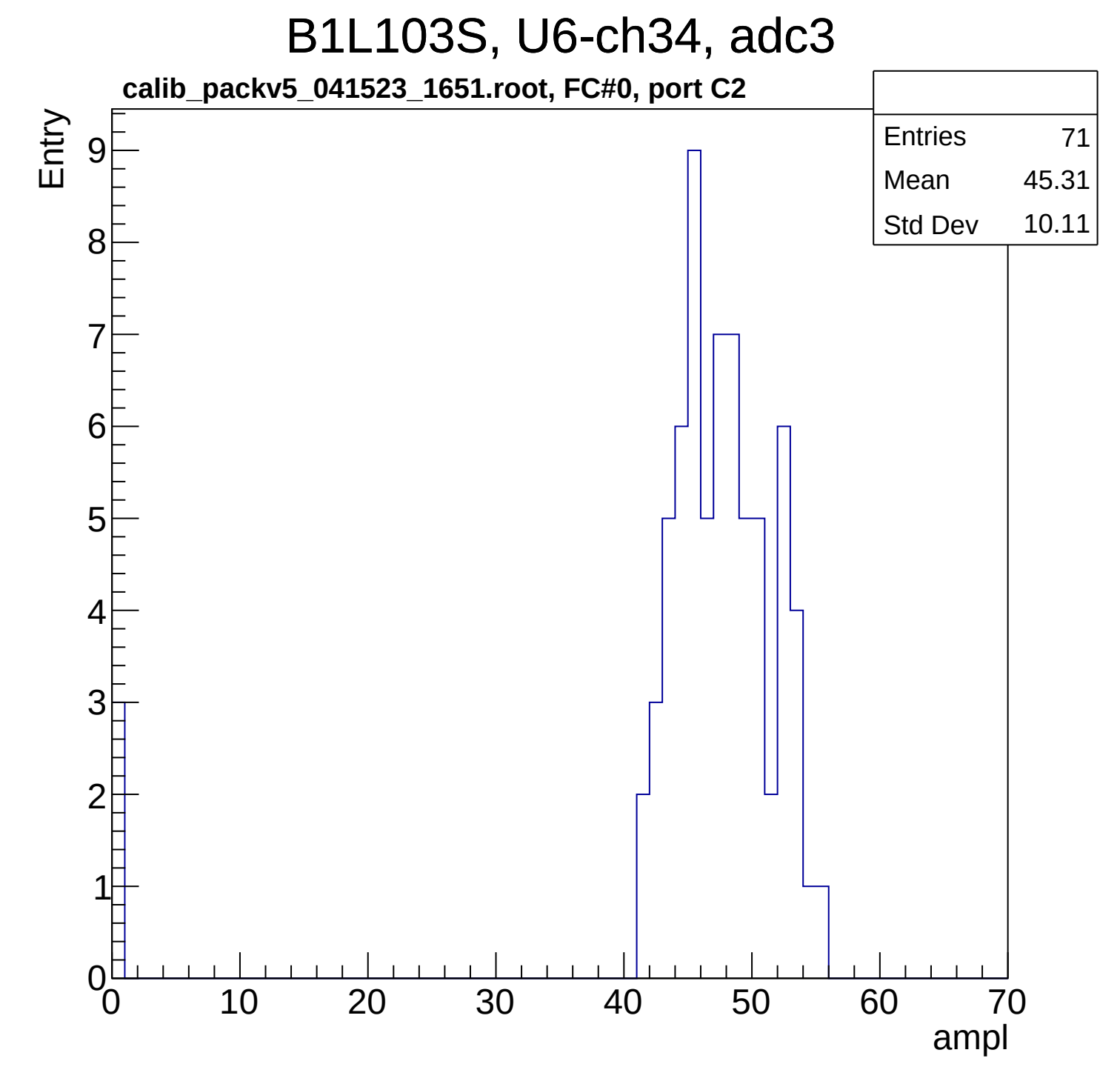
50
60
70
ampl


B1L103S, U6-ch34, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 45.31
Std Dev 10.11
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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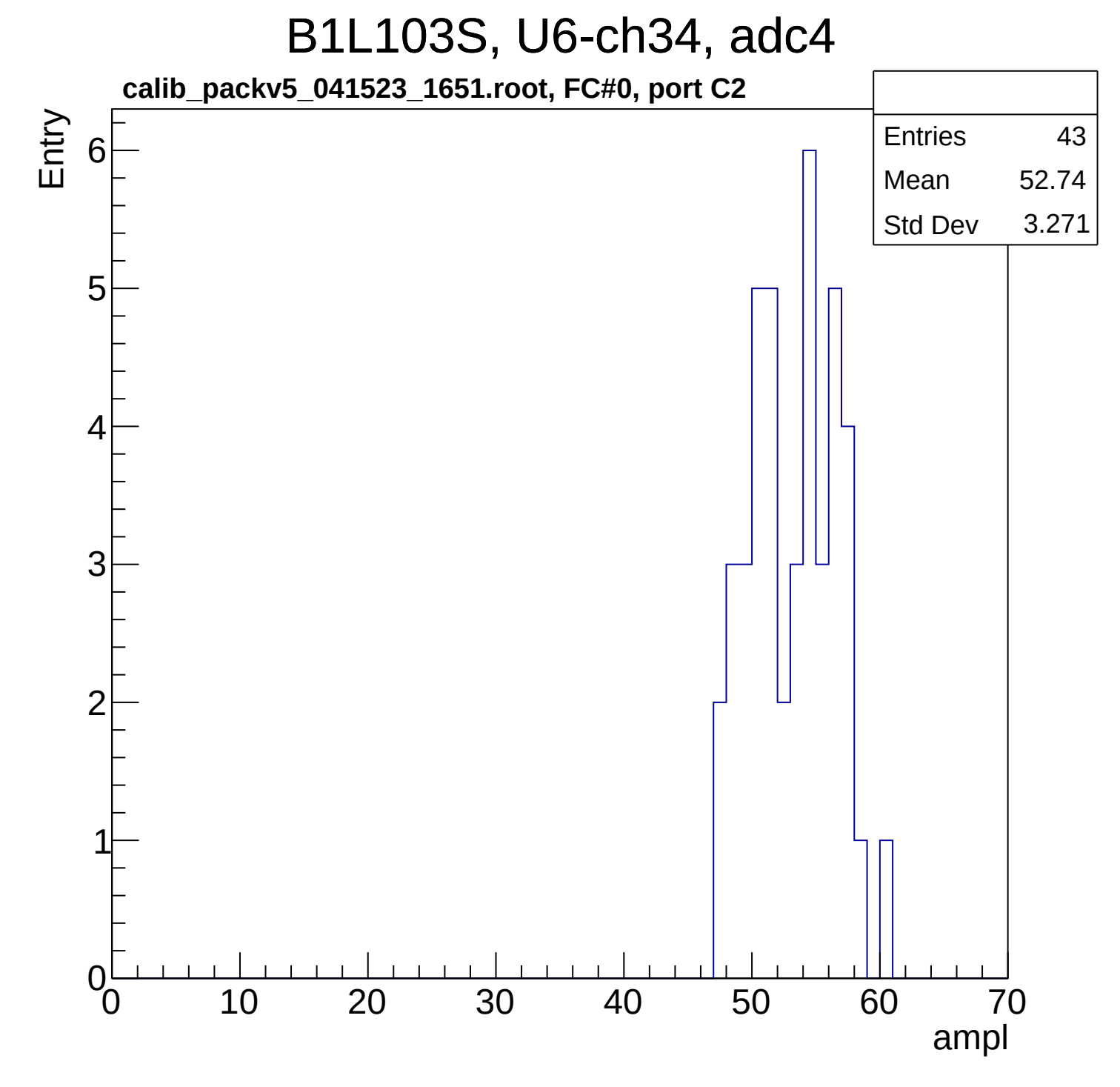
B1L103S, U6-ch34, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 52.74
Std Dev 3.271
Entry
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2
3
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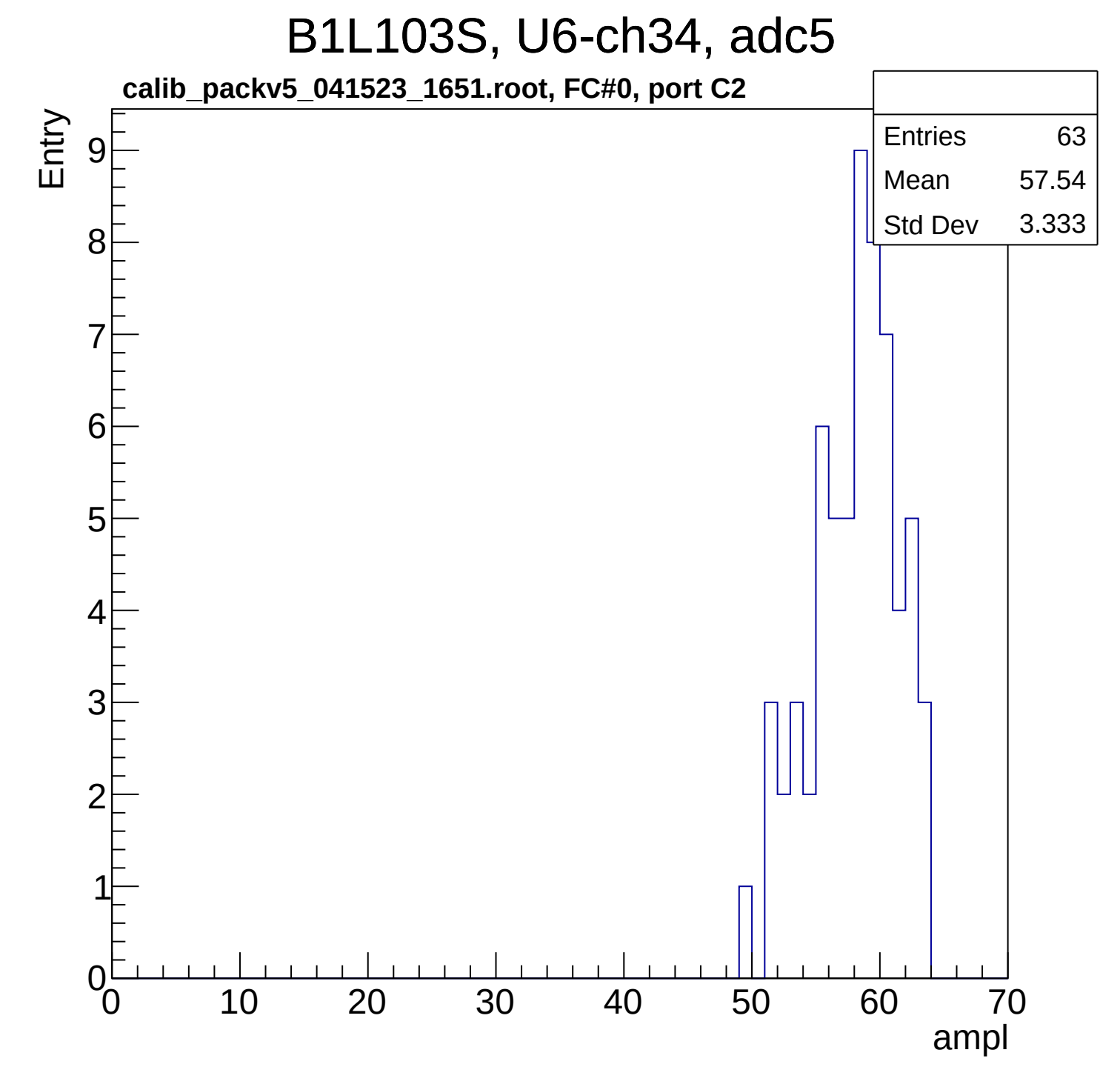
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch34, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 57.54
Std Dev 3.333
Entry
ampl
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2
3
4
5
6
7
8
9
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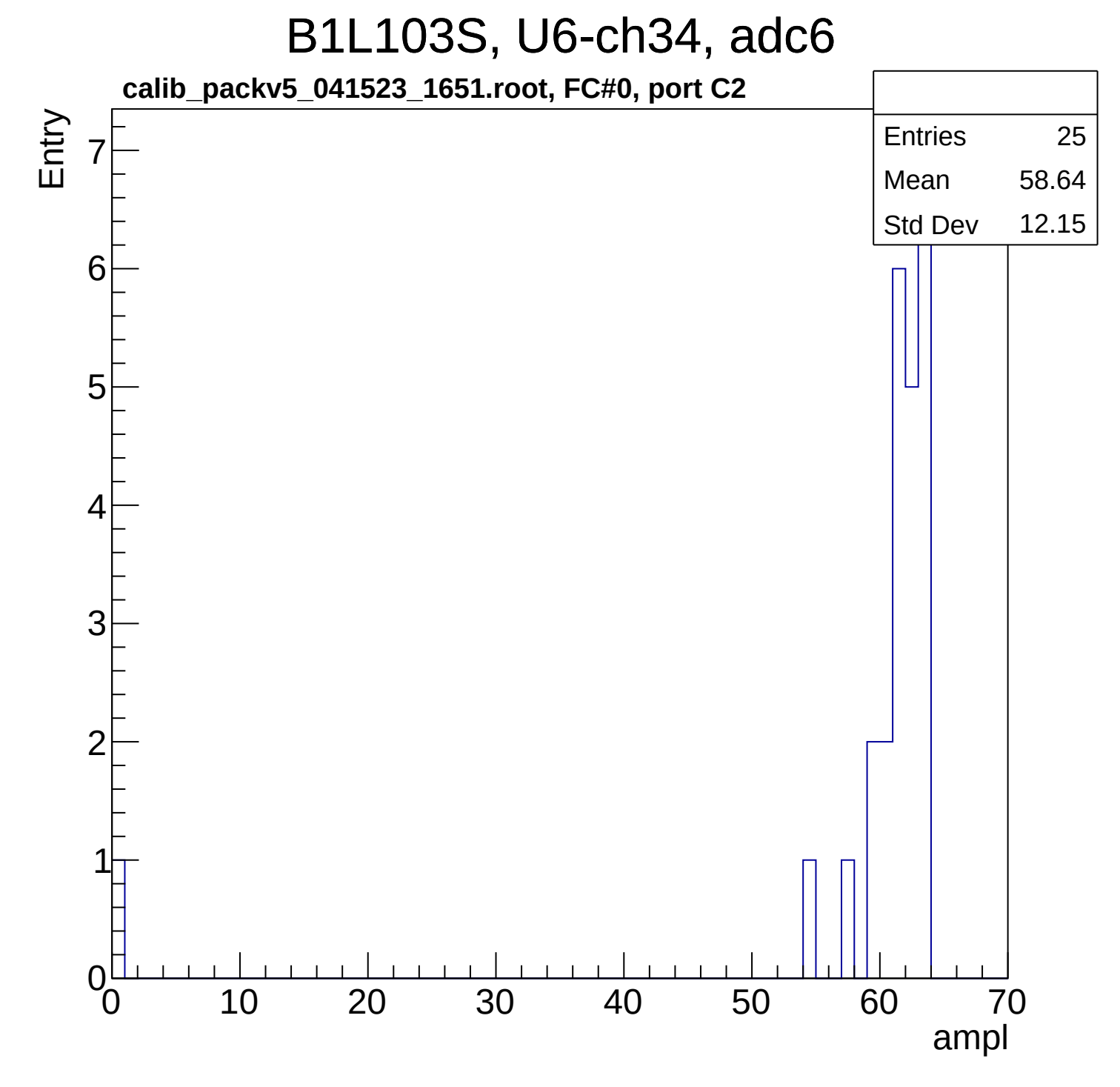
B1L103S, U6-ch34, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 58.64
Std Dev 12.15
Entry
ampl
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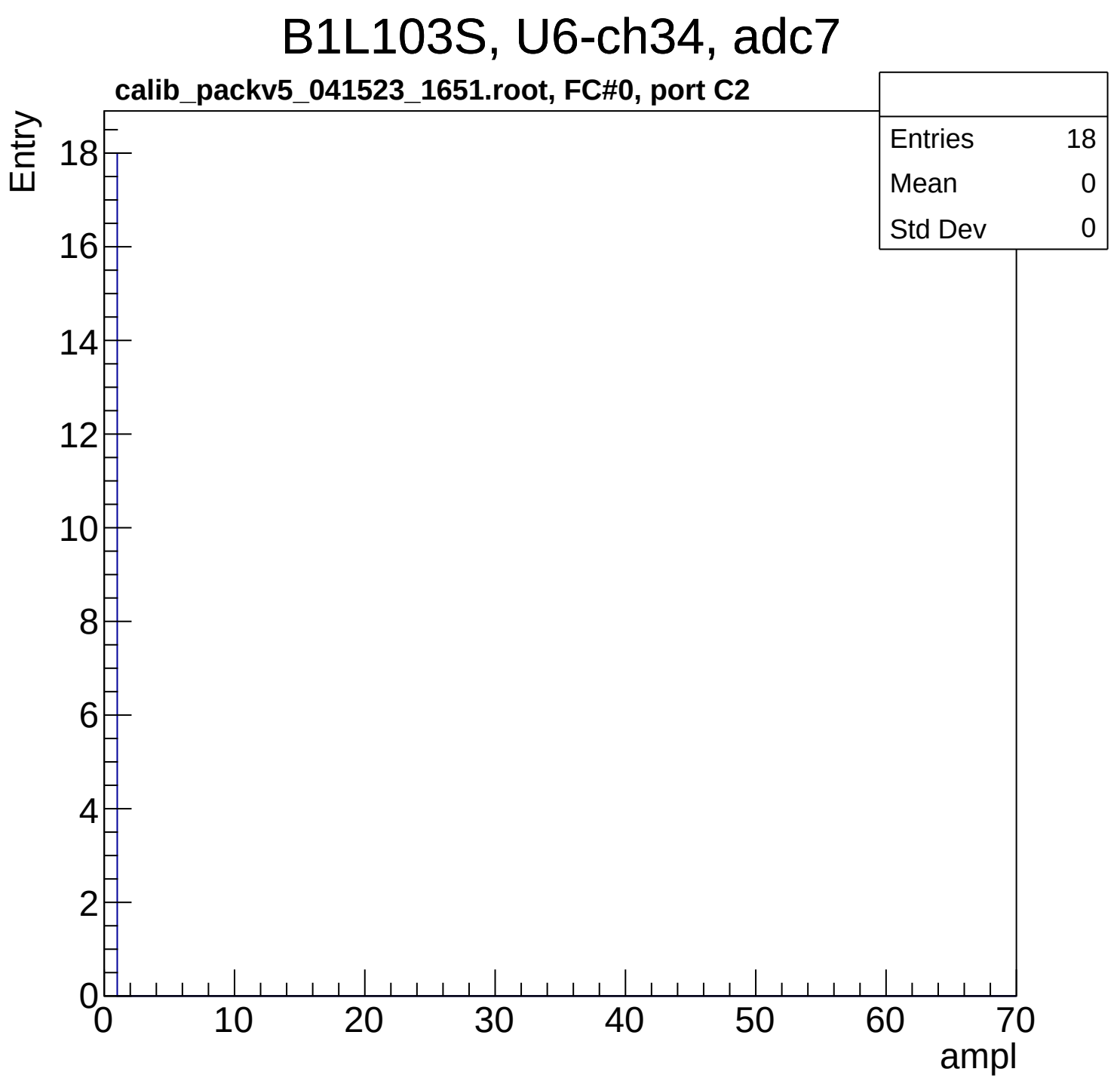
B1L103S, U6-ch34, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
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10
12
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30
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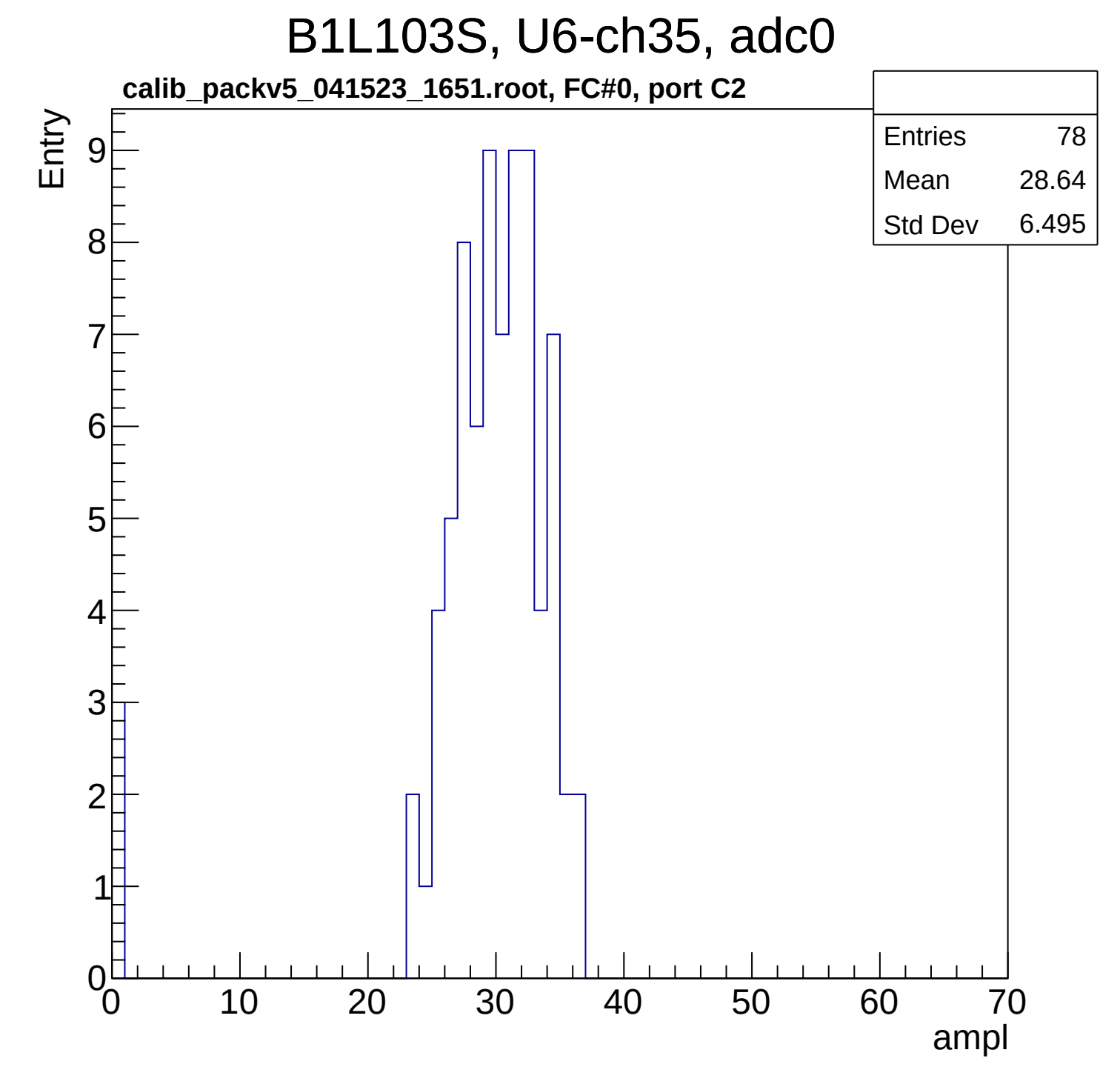
50
60
70
ampl


B1L103S, U6-ch35, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 28.64
Std Dev 6.495
Entry
ampl
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2
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4
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6
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0
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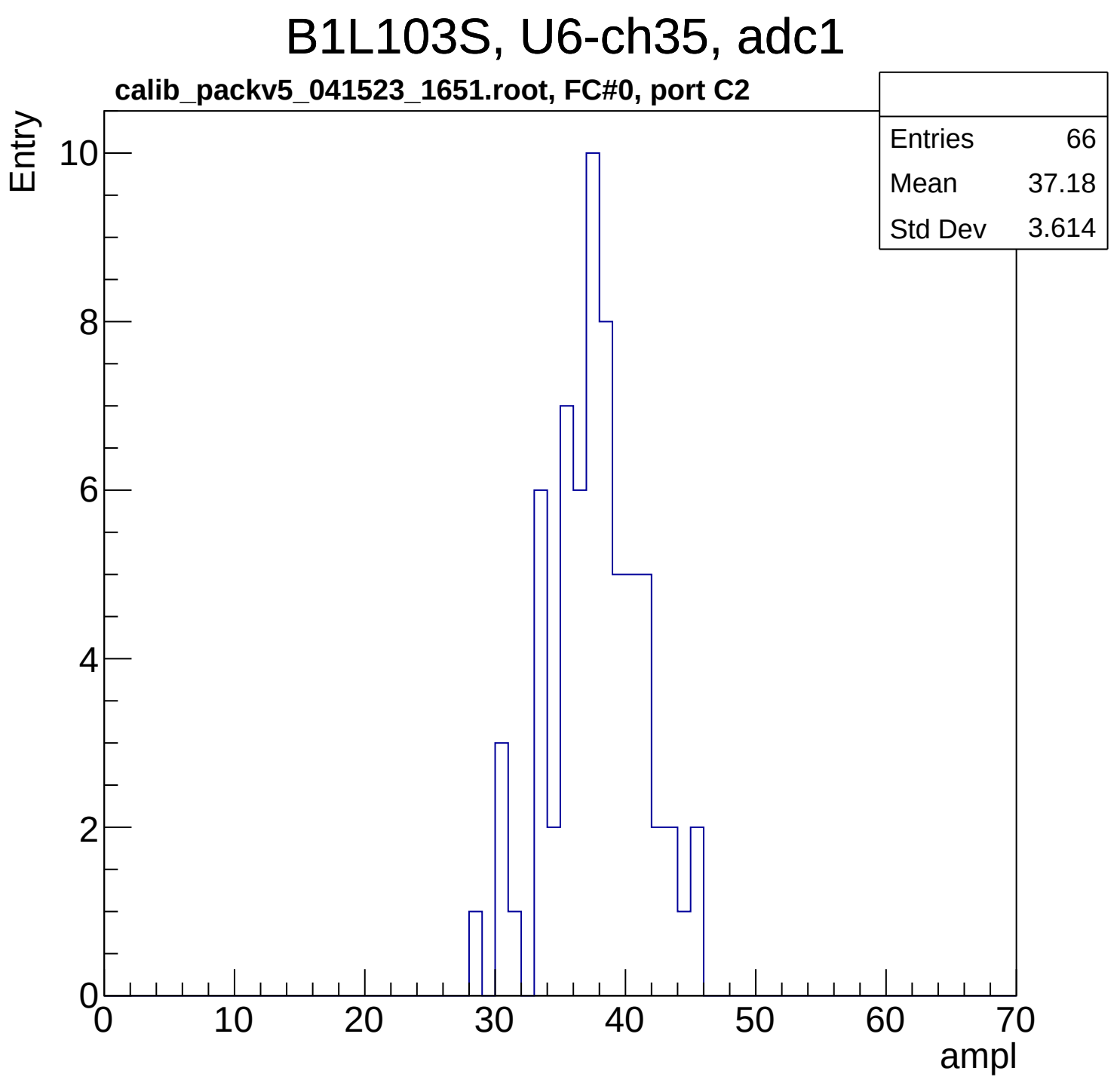
B1L103S, U6-ch35, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 37.18
Std Dev 3.614
Entry
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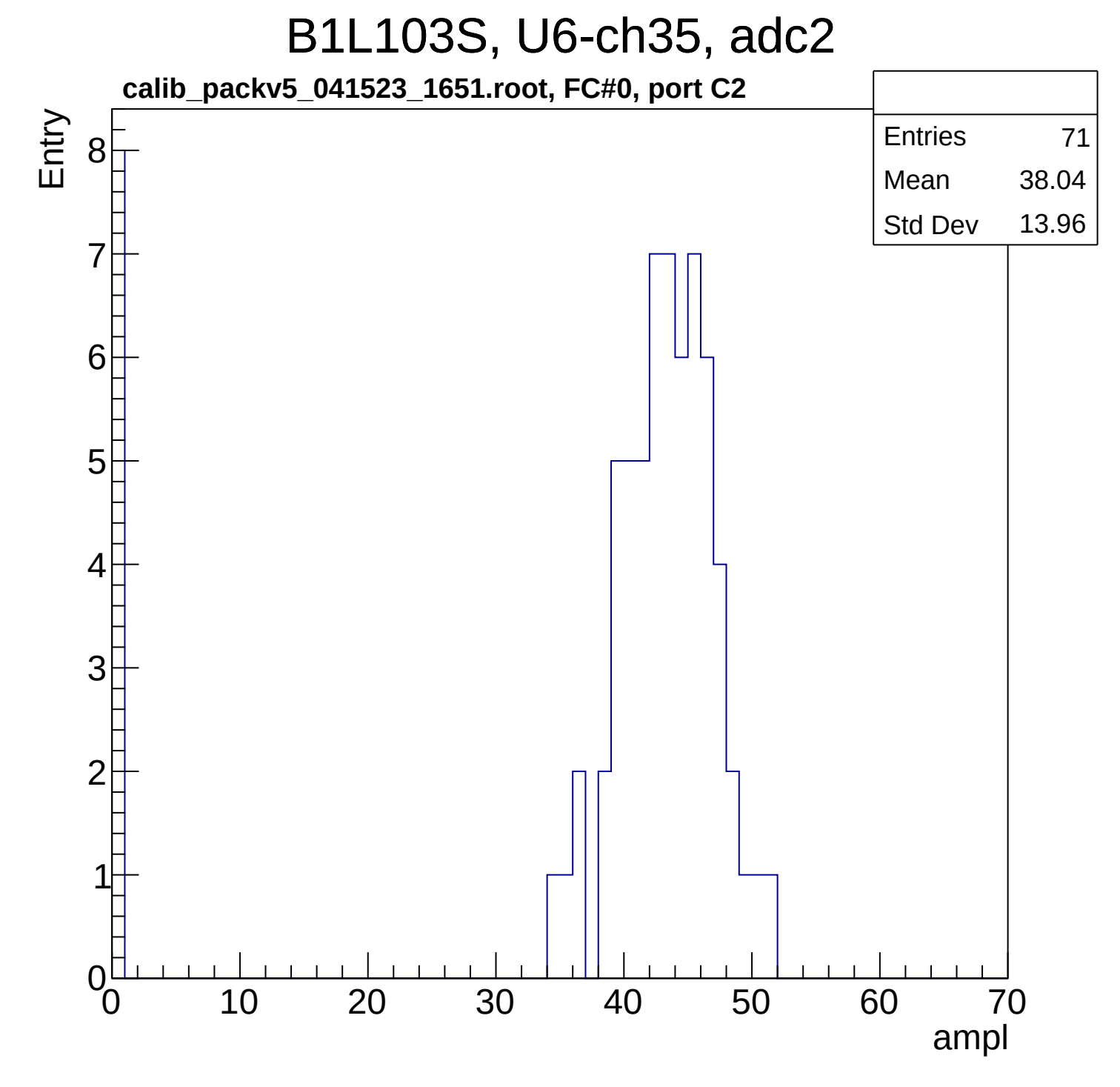
ampl


B1L103S, U6-ch35, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 38.04
Std Dev 13.96
Entry
ampl
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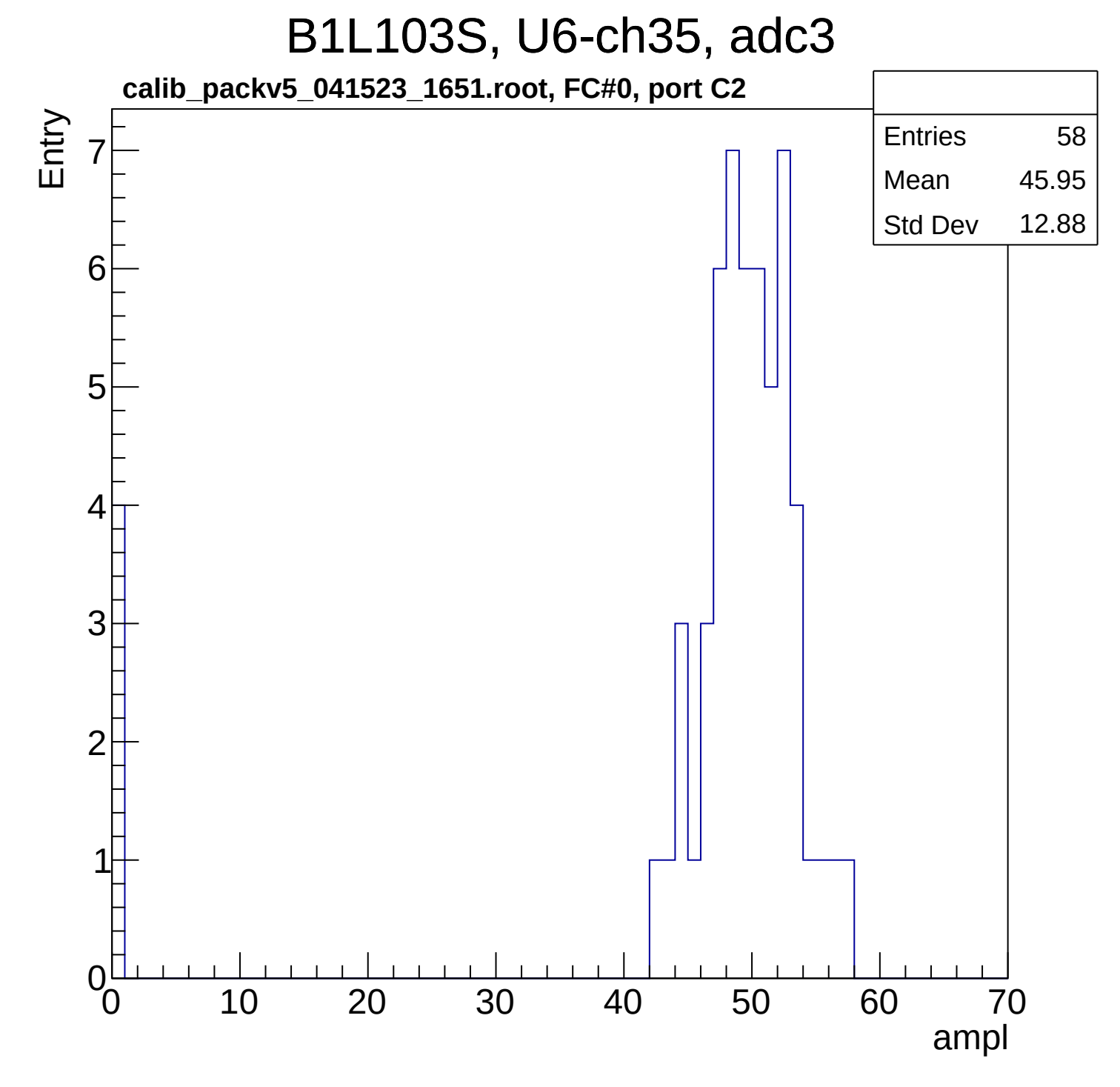
B1L103S, U6-ch35, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 45.95
Std Dev 12.88
Entry
ampl
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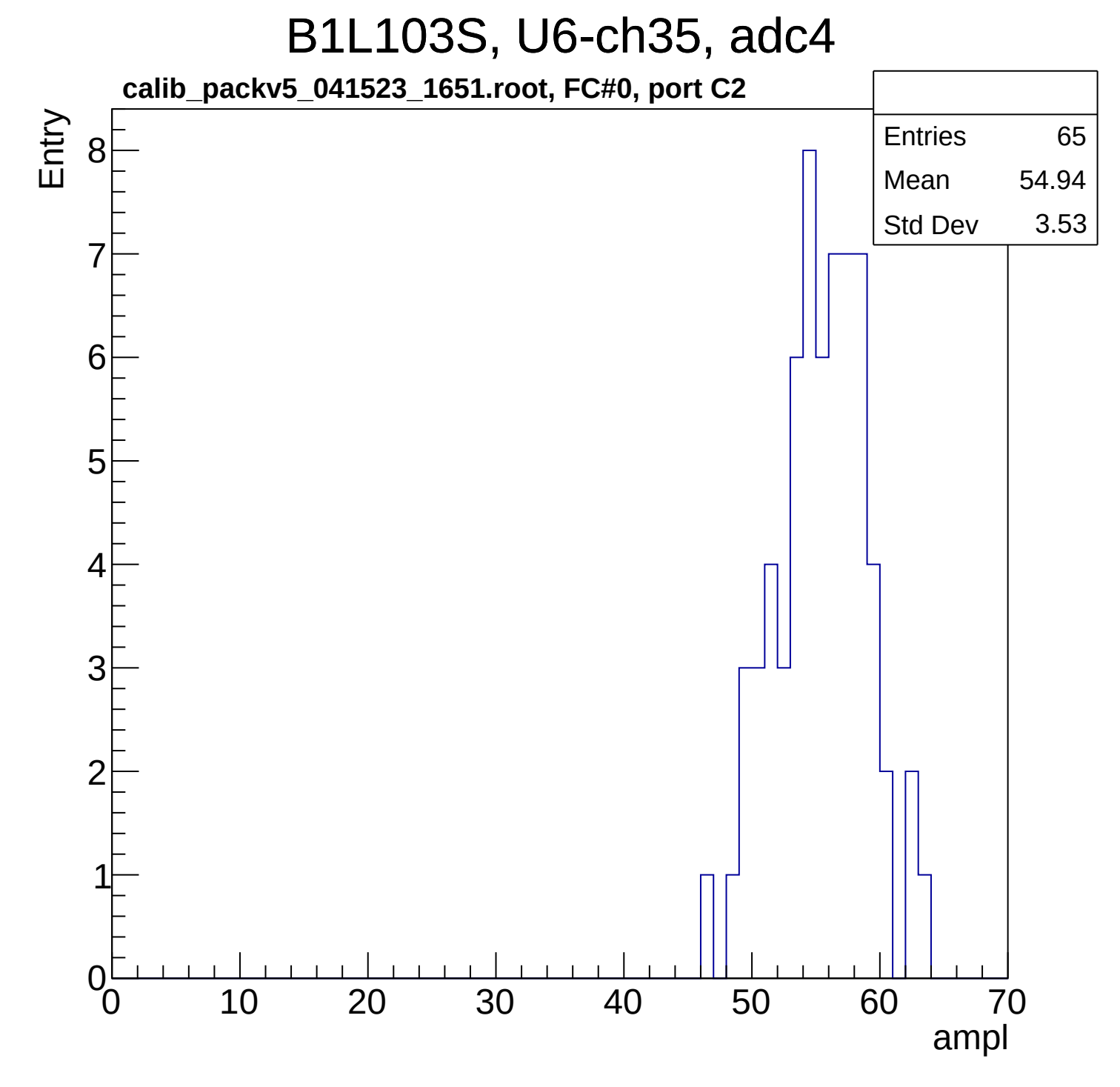
B1L103S, U6-ch35, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 54.94
Std Dev 3.53
Entry
ampl
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0
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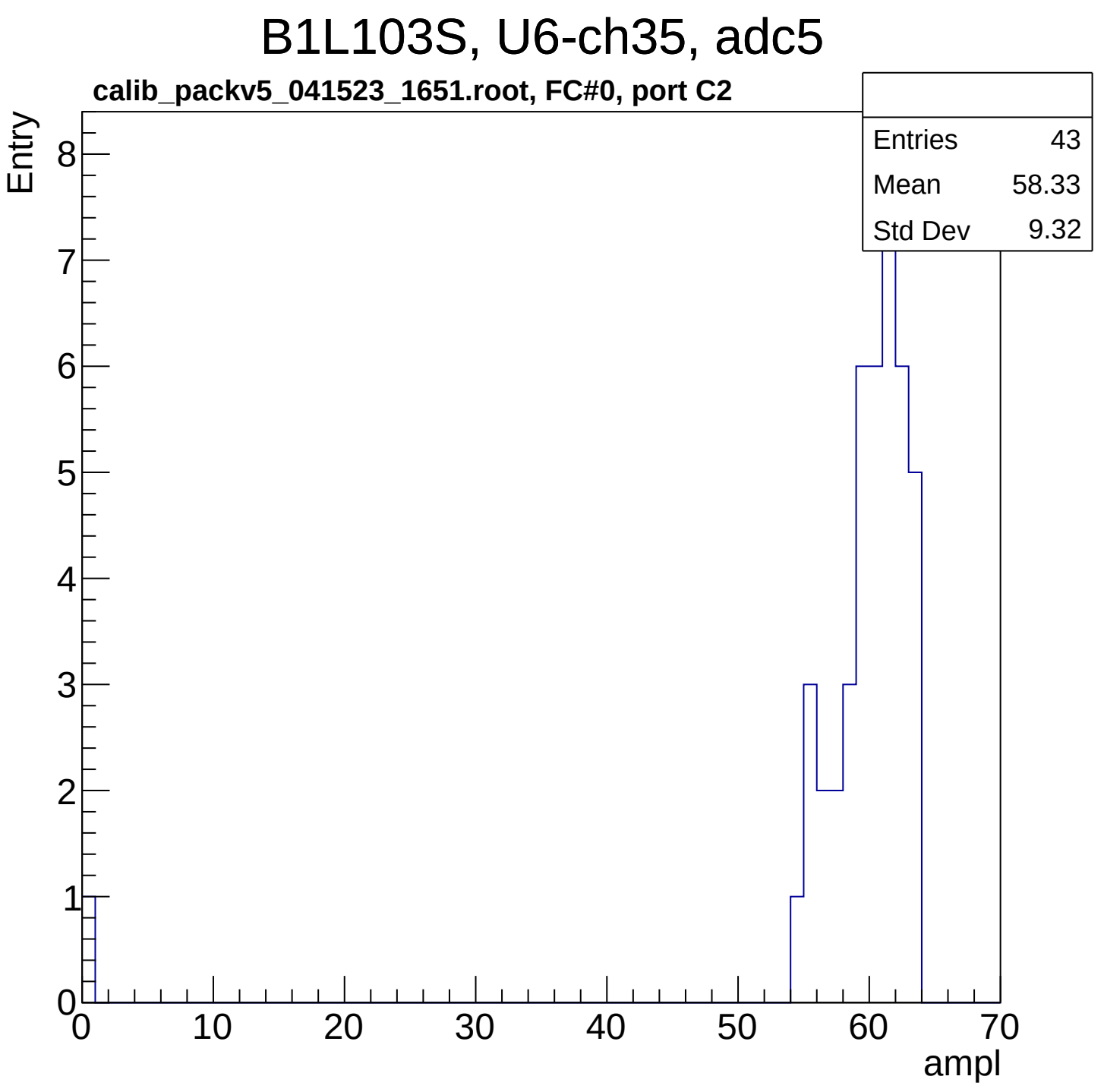
B1L103S, U6-ch35, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 58.33
Std Dev 9.32
Entry
ampl
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7
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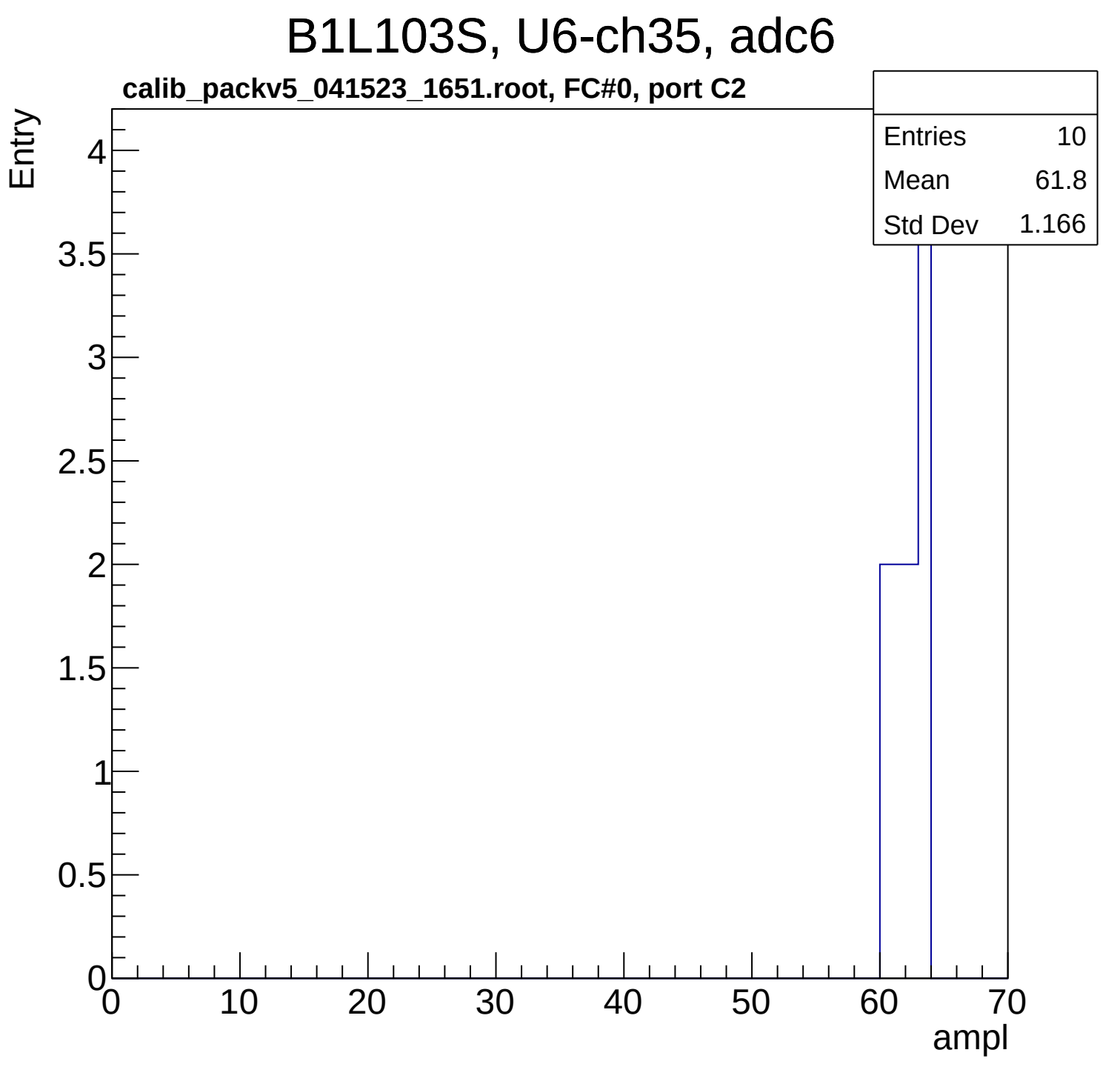
B1L103S, U6-ch35, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61.8
Std Dev 1.166
Entry
ampl
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1.5
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3.5
4
0
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40
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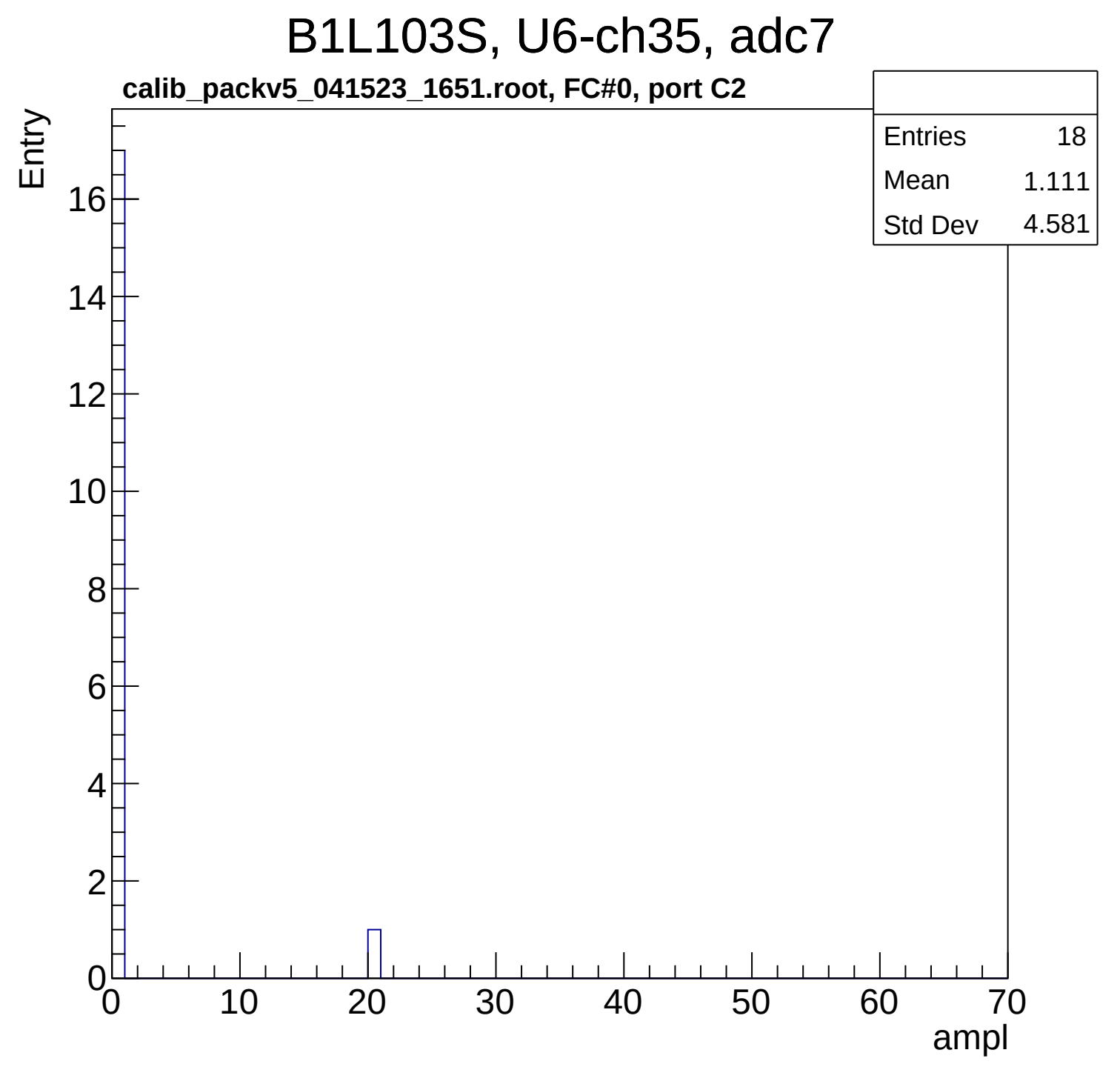
B1L103S, U6-ch35, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.111
Std Dev 4.581
Entry
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16
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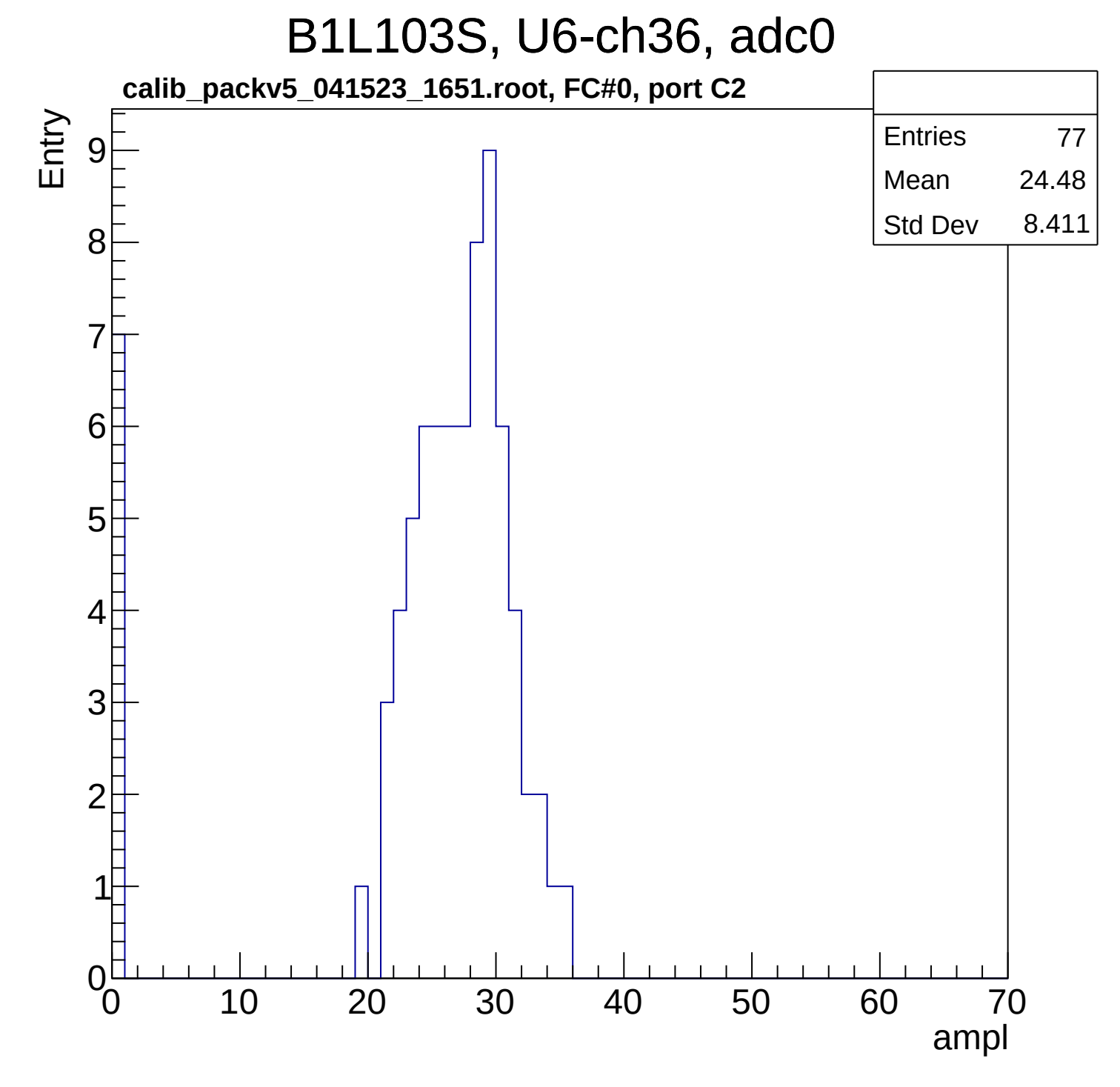
50
60
70
ampl


B1L103S, U6-ch36, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 24.48
Std Dev 8.411
Entry
ampl
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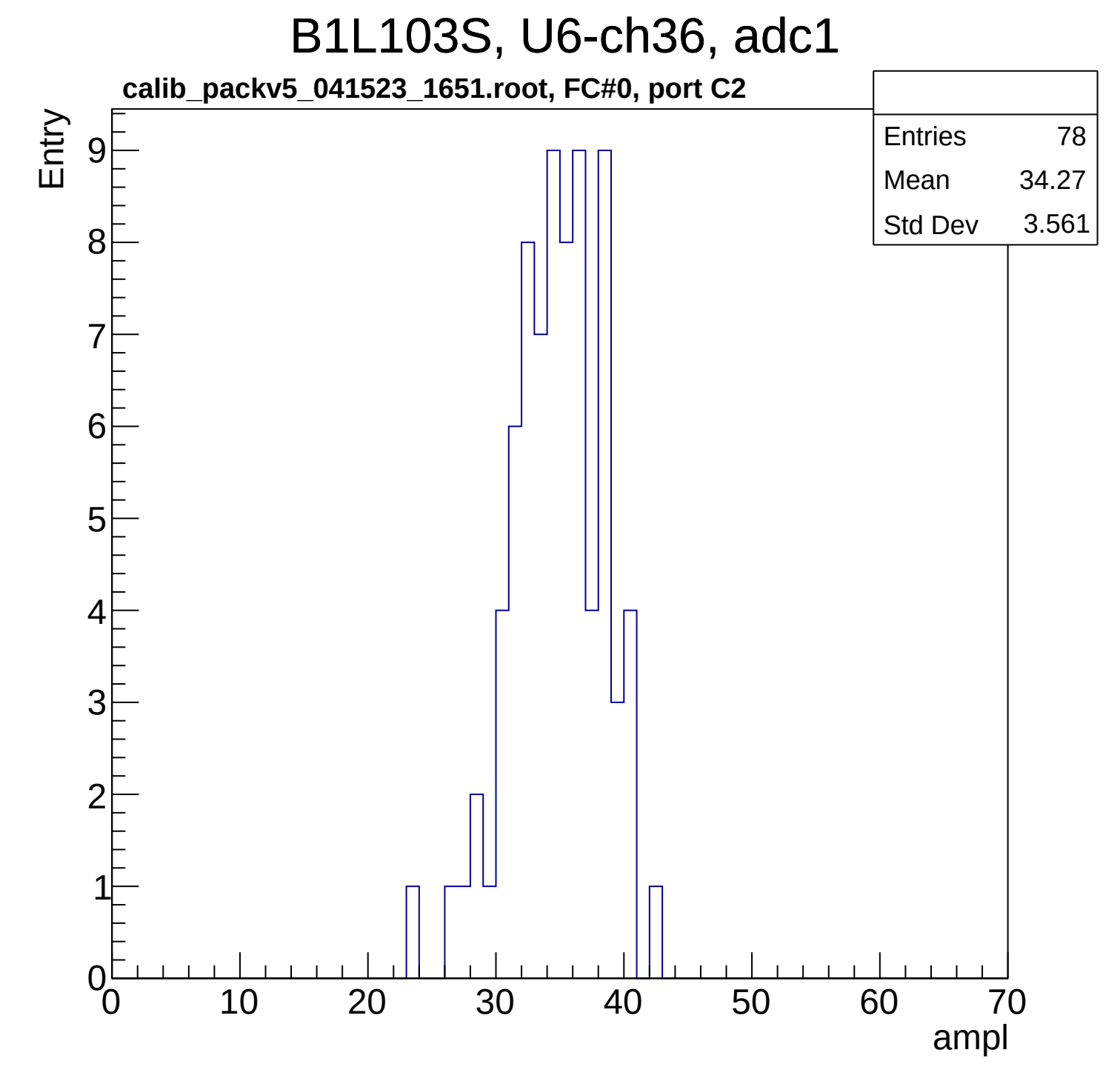
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch36, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 34.27
Std Dev 3.561
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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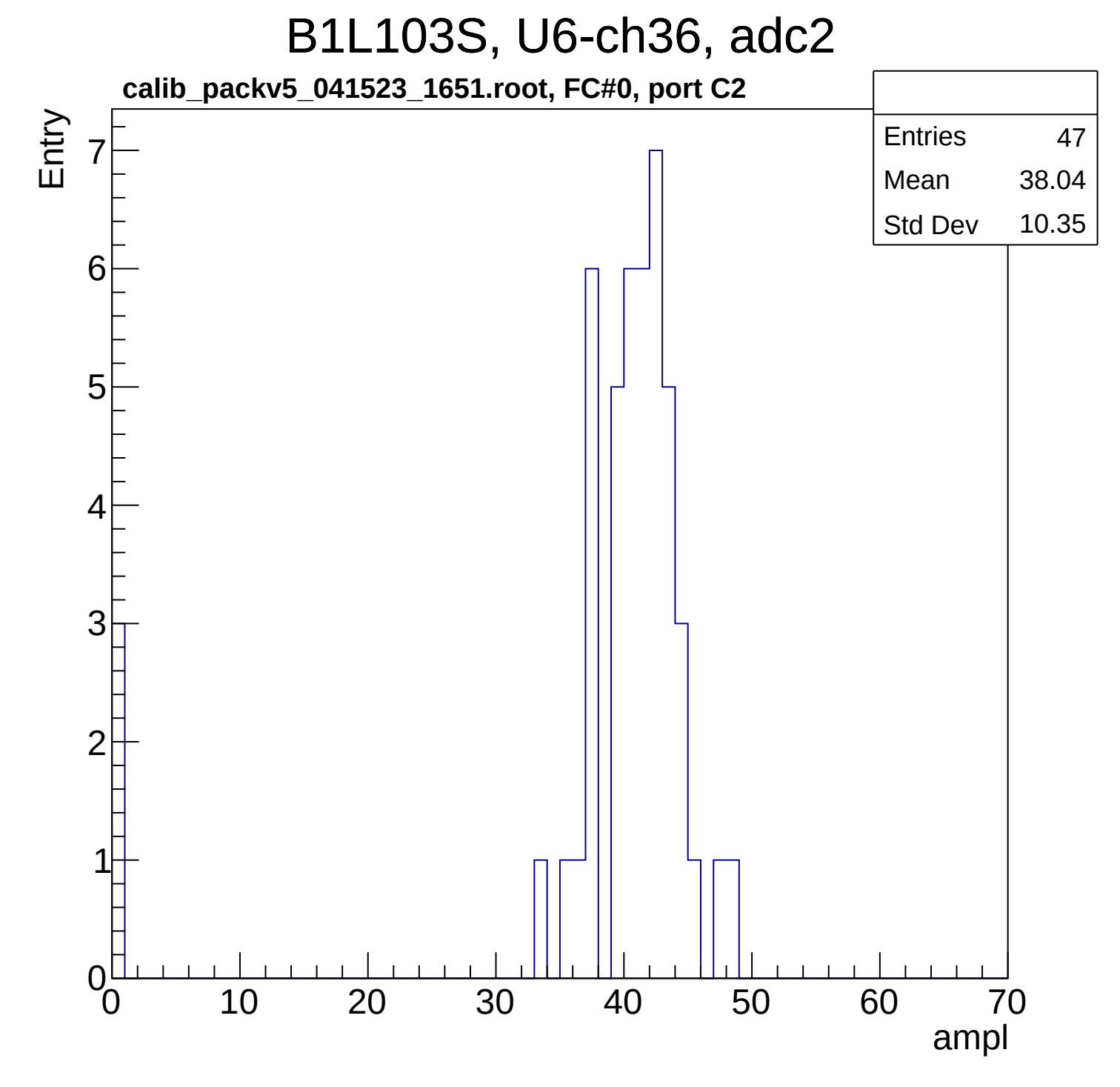
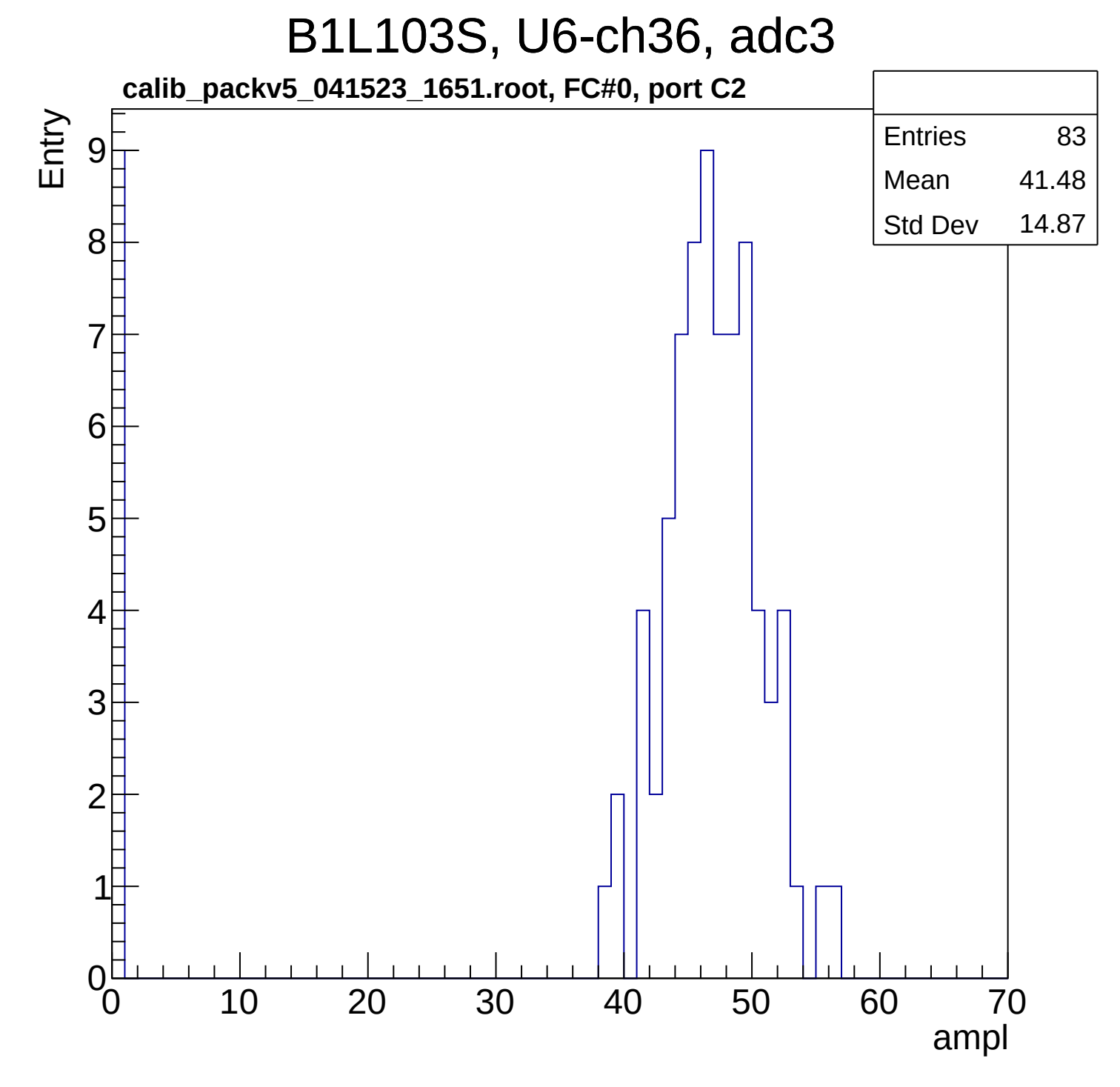
40
50
60
70


B1L103S, U6-ch36, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 38.04
Std Dev 10.35
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U6-ch36, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 41.48
Std Dev 14.87
Entry
ampl
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2
3
4
5
6
7
8
9
0
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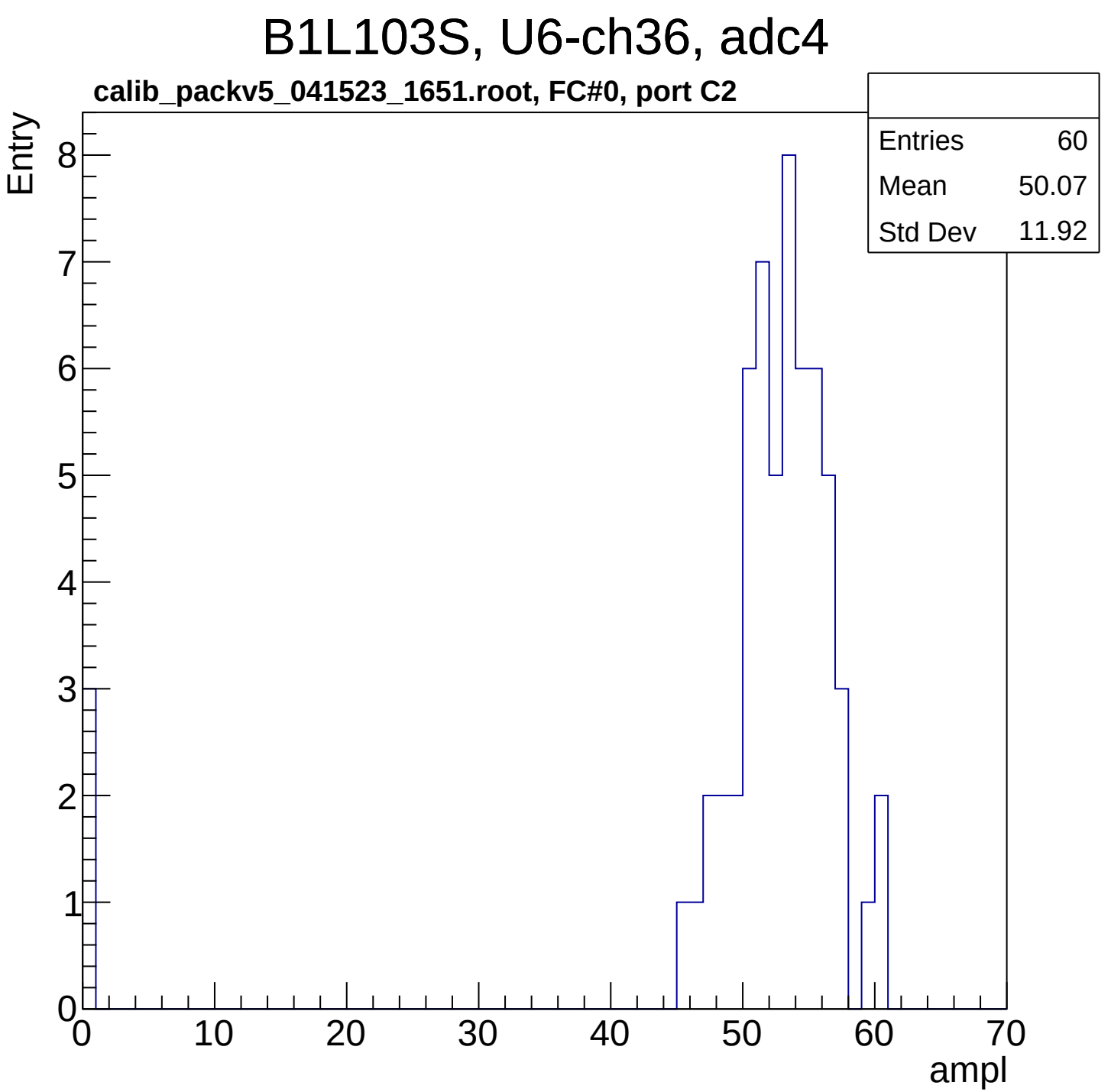
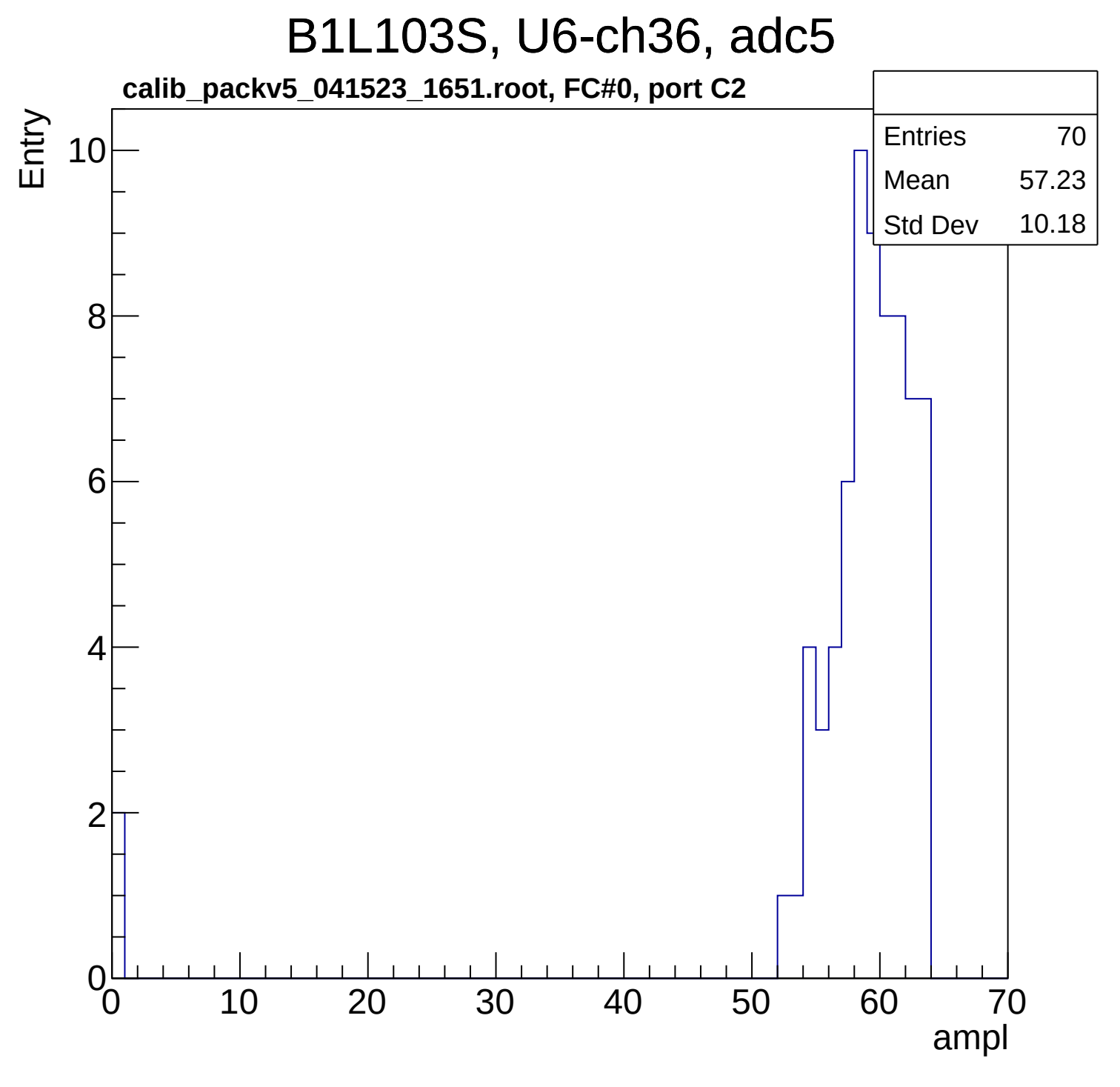
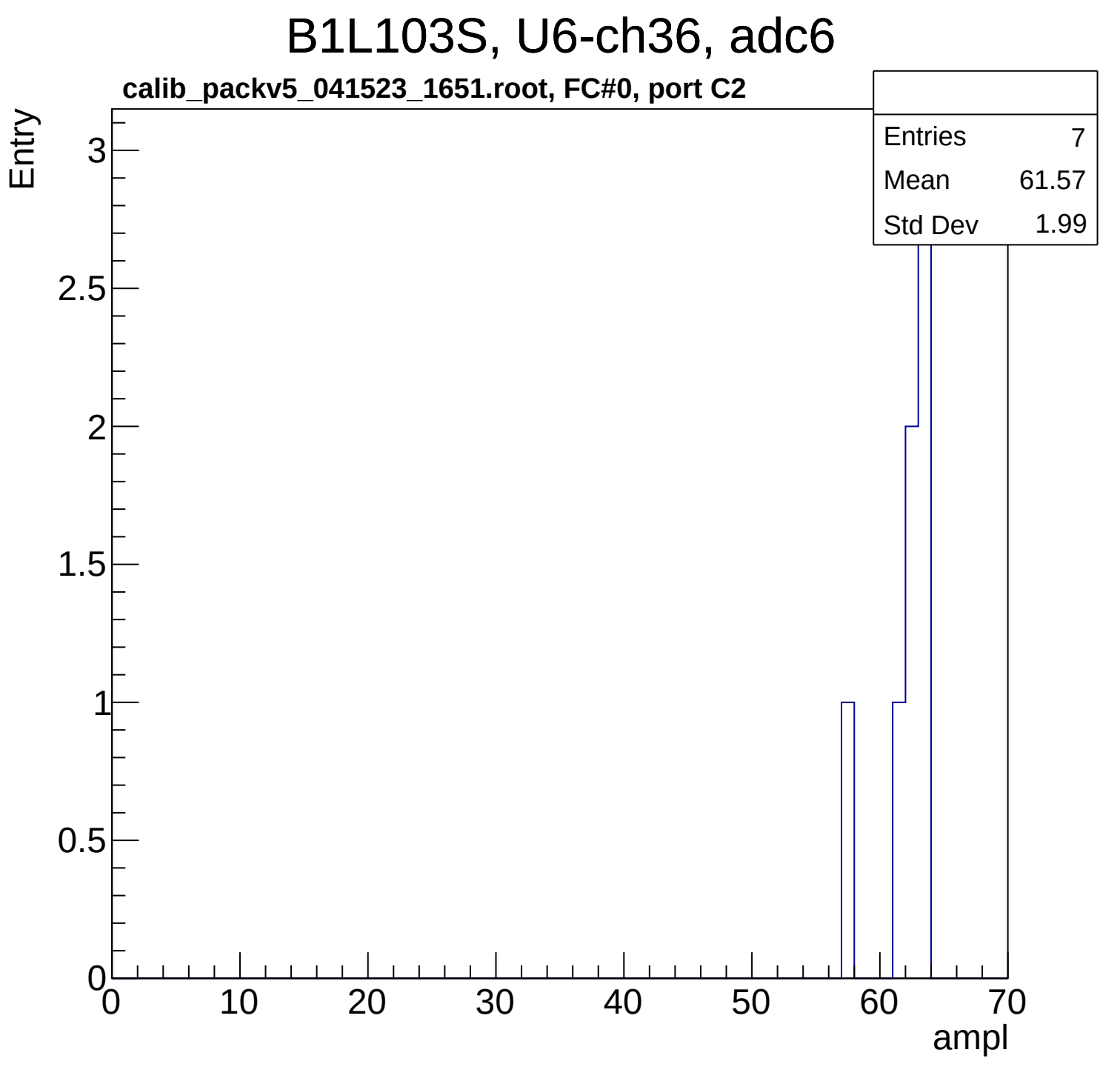
20
30
40
50
60
70


B1L103S, U6-ch36, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 50.07
Std Dev 11.92
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch36, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 57.23
Std Dev 10.18
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch36, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 61.57
Std Dev 1.99
Entry
ampl
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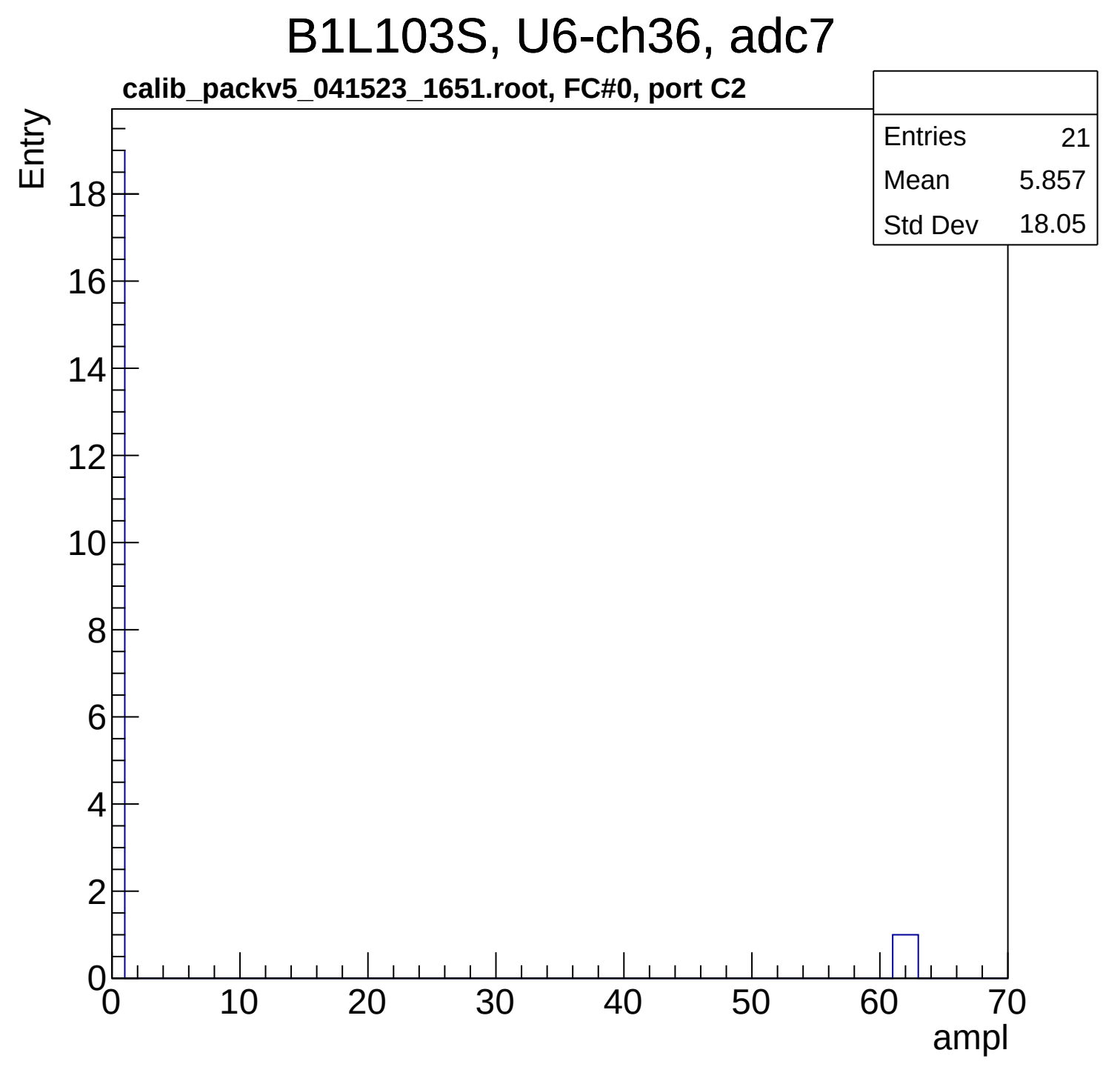
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U6-ch36, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.857
Std Dev 18.05
Entry
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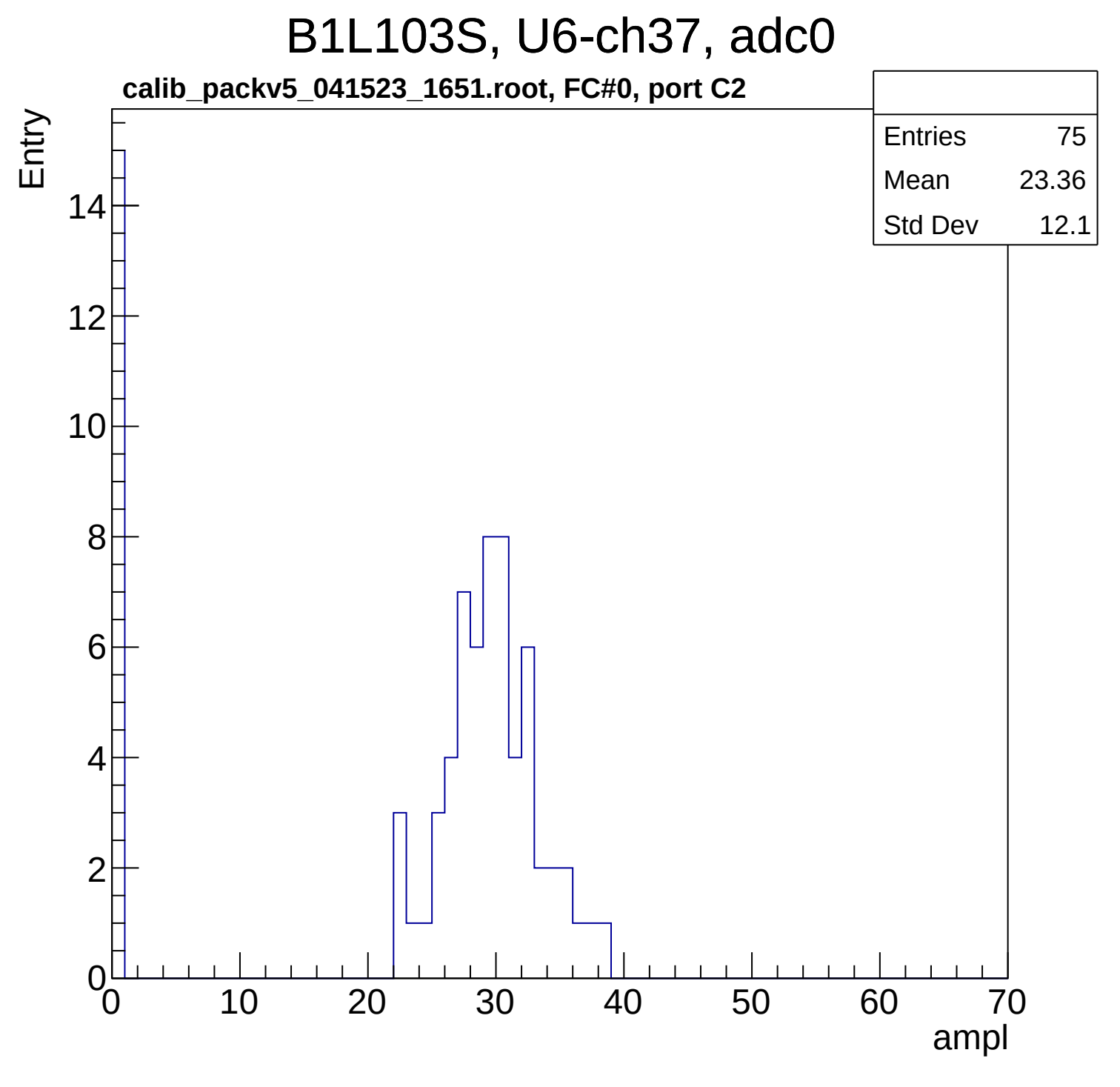
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch37, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 23.36
Std Dev 12.1
Entry
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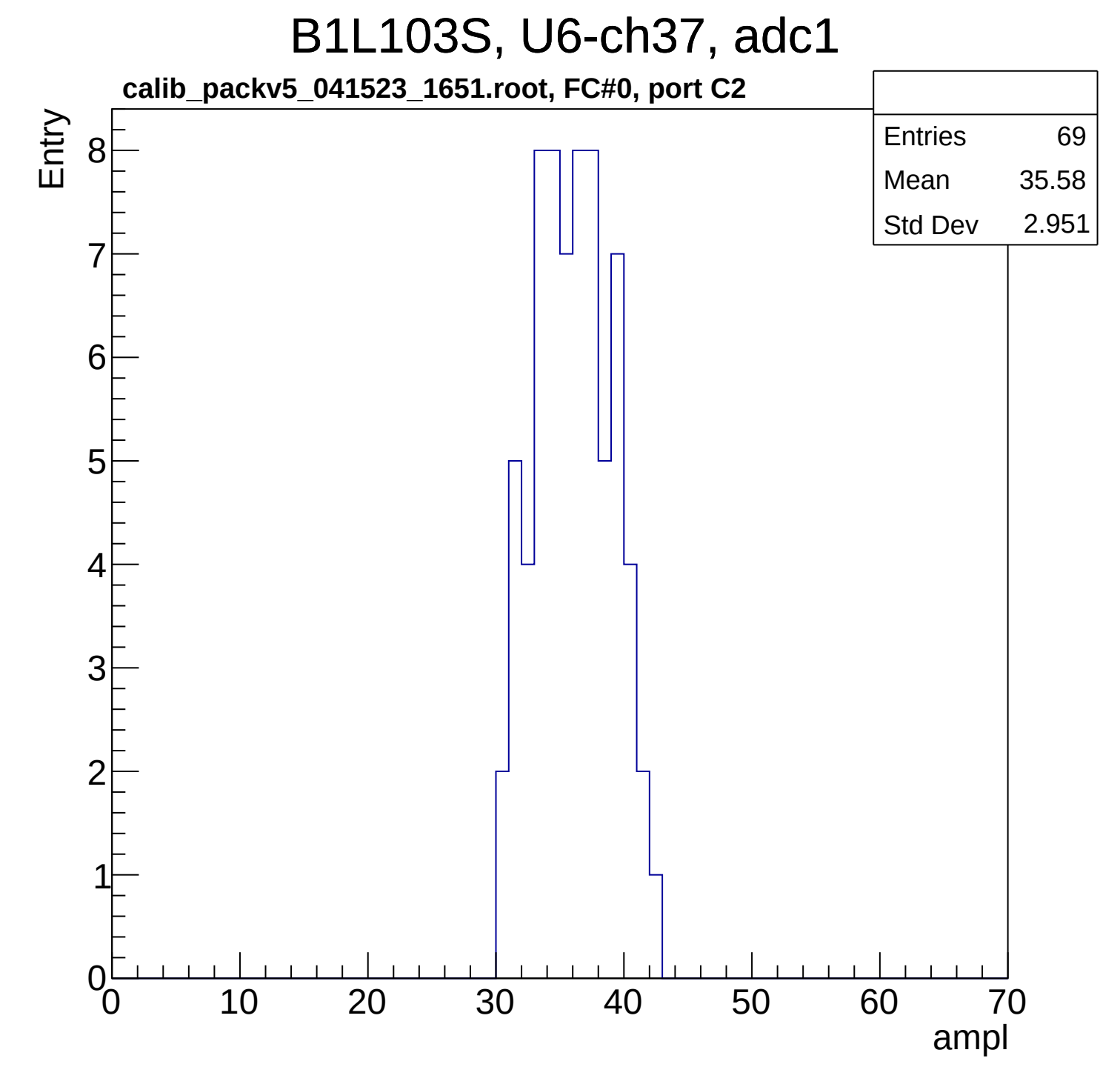
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch37, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 35.58
Std Dev 2.951
Entry
ampl
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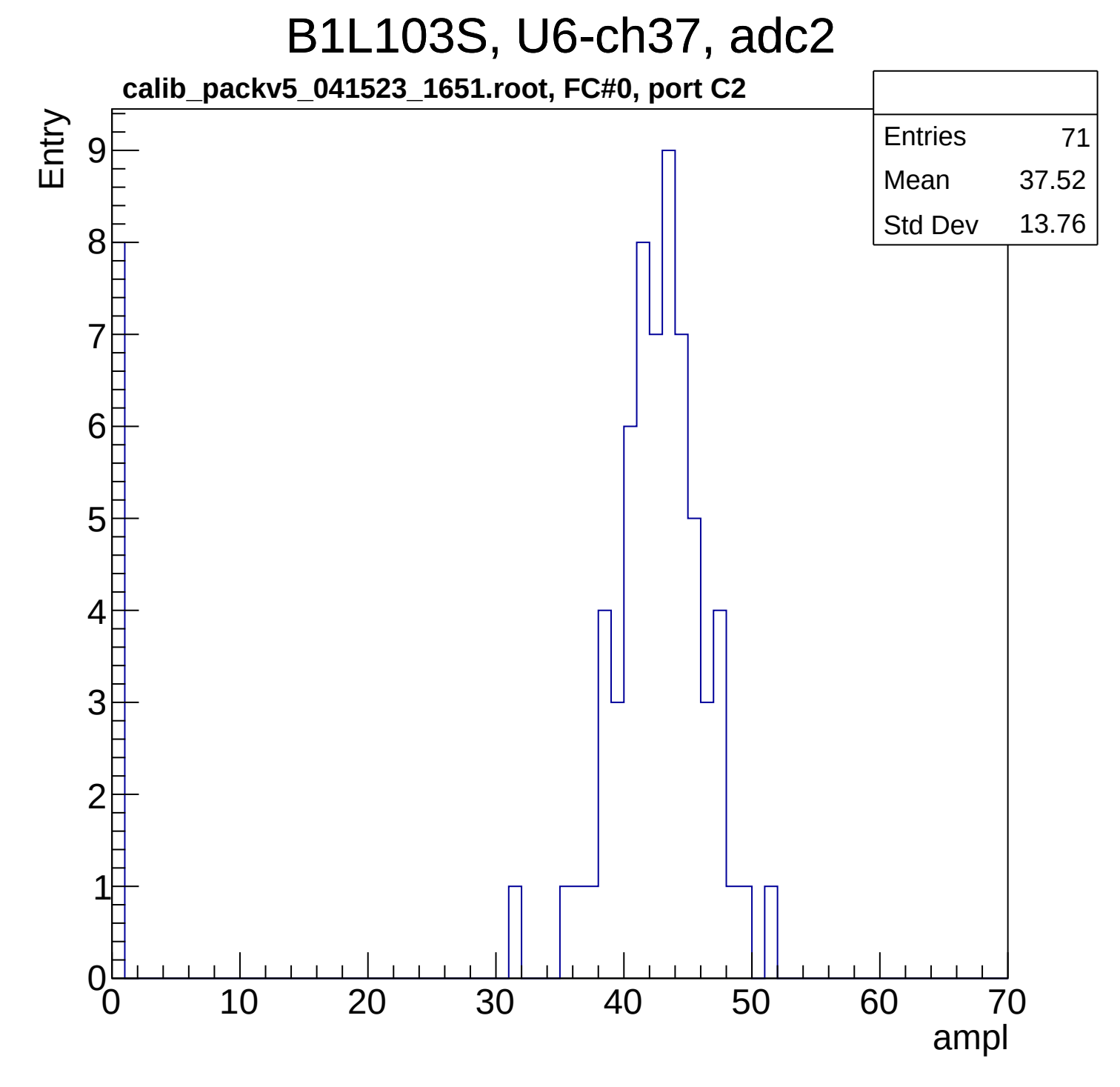
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch37, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 37.52
Std Dev 13.76
Entry
ampl
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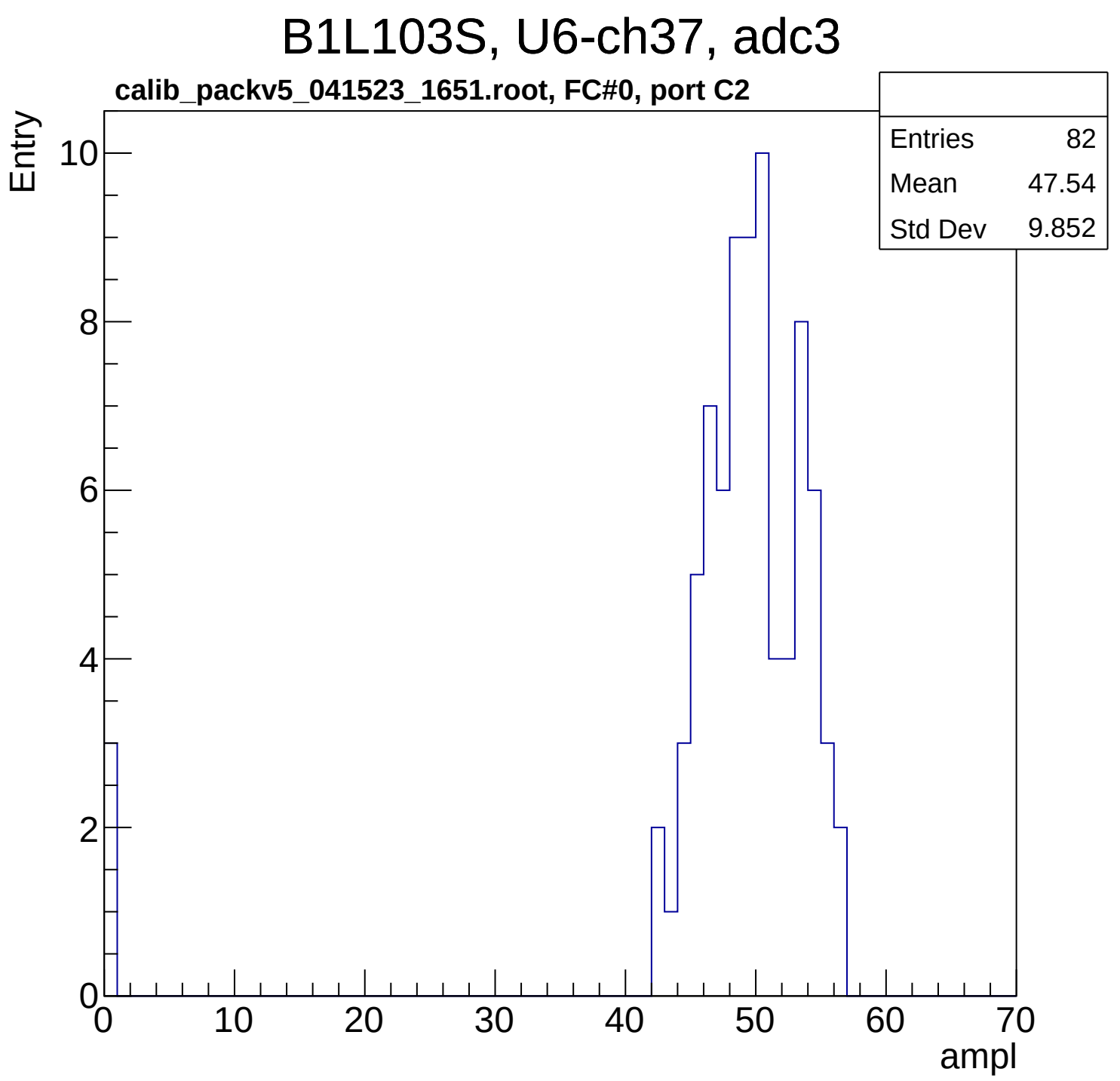
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch37, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 47.54
Std Dev 9.852
Entry
0
2
4
6
8
10
0
10
20
30
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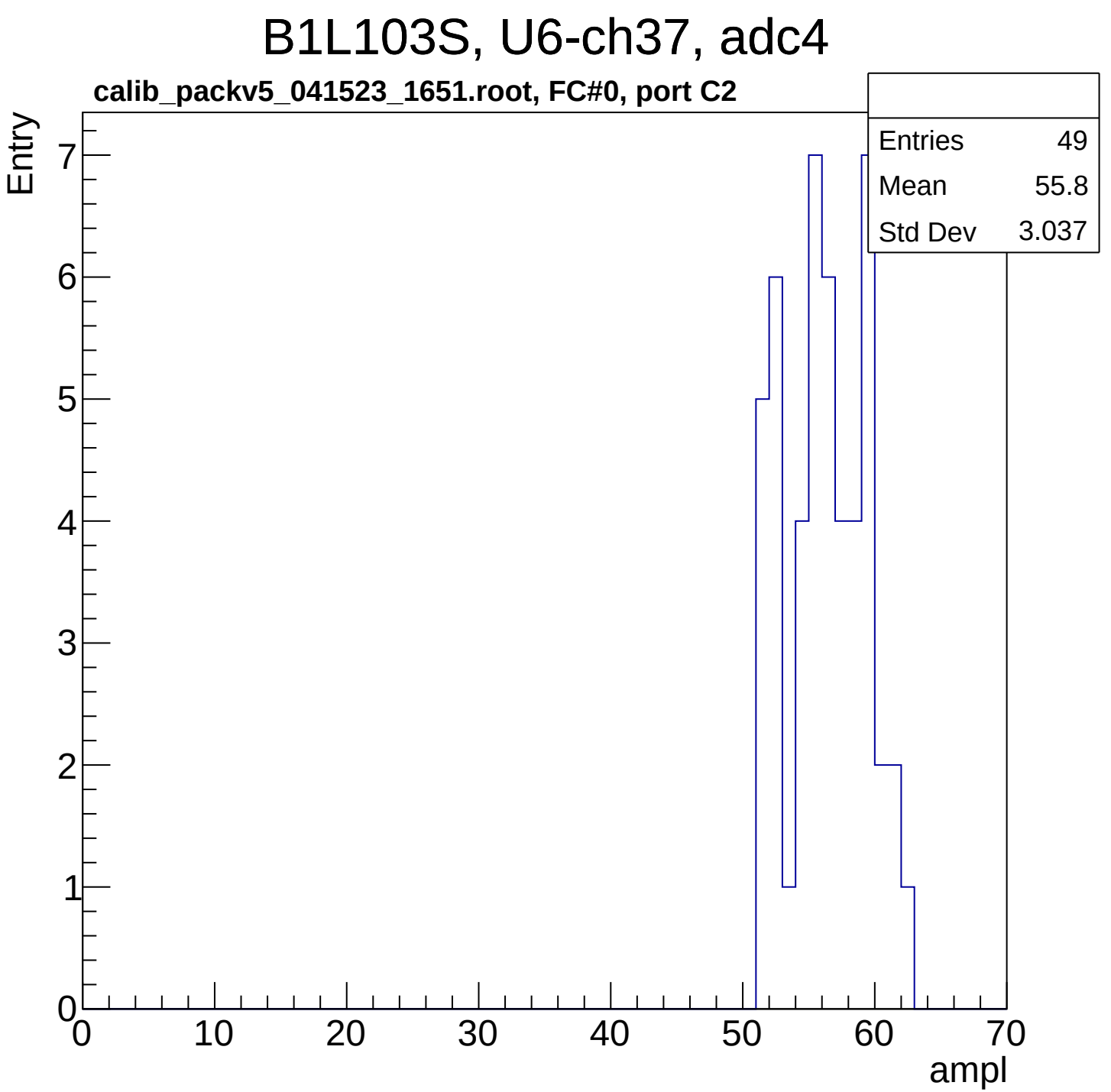
50
60
70
ampl


B1L103S, U6-ch37, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 55.8
Std Dev 3.037
Entry
ampl
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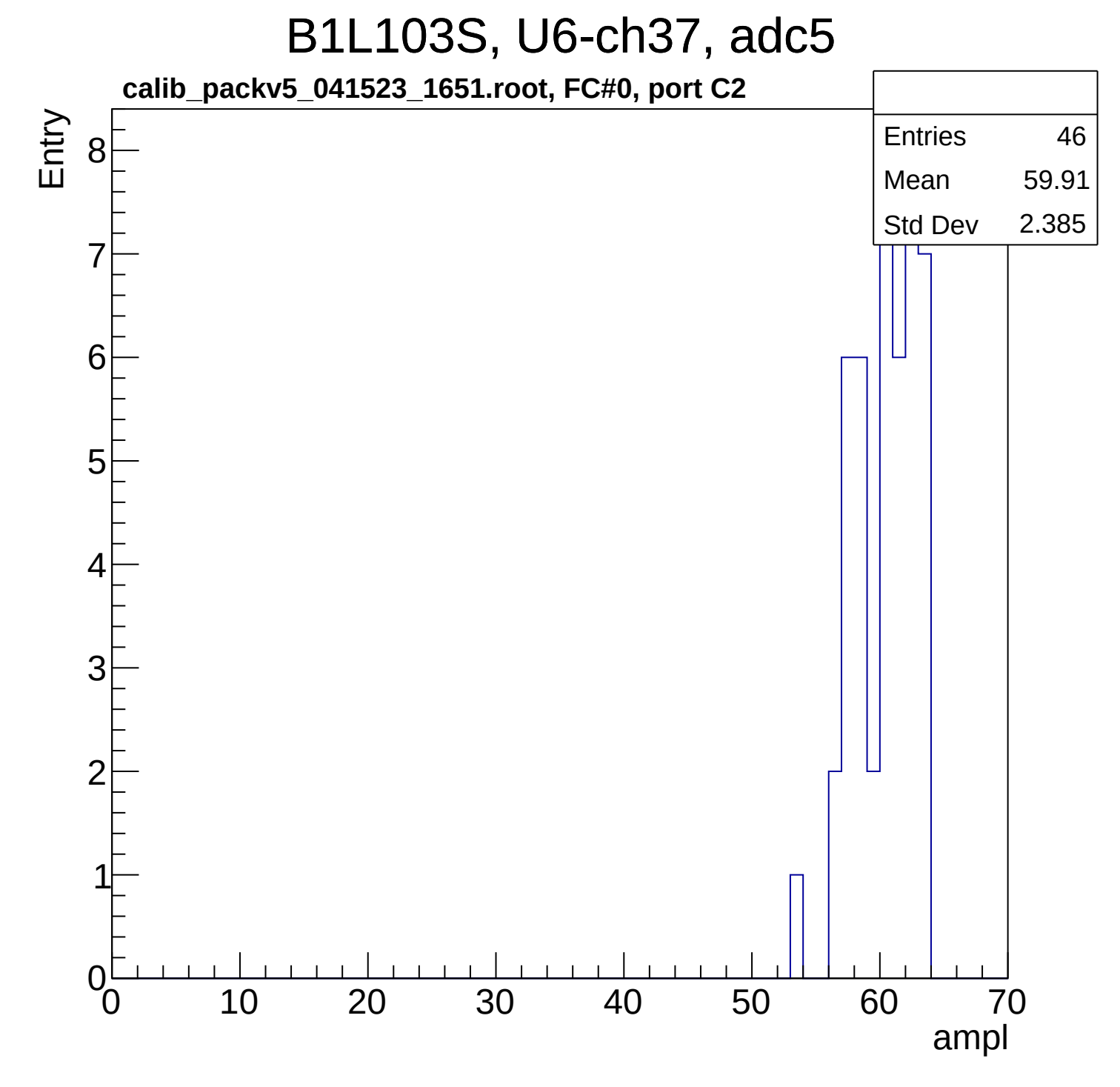
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U6-ch37, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 59.91
Std Dev 2.385
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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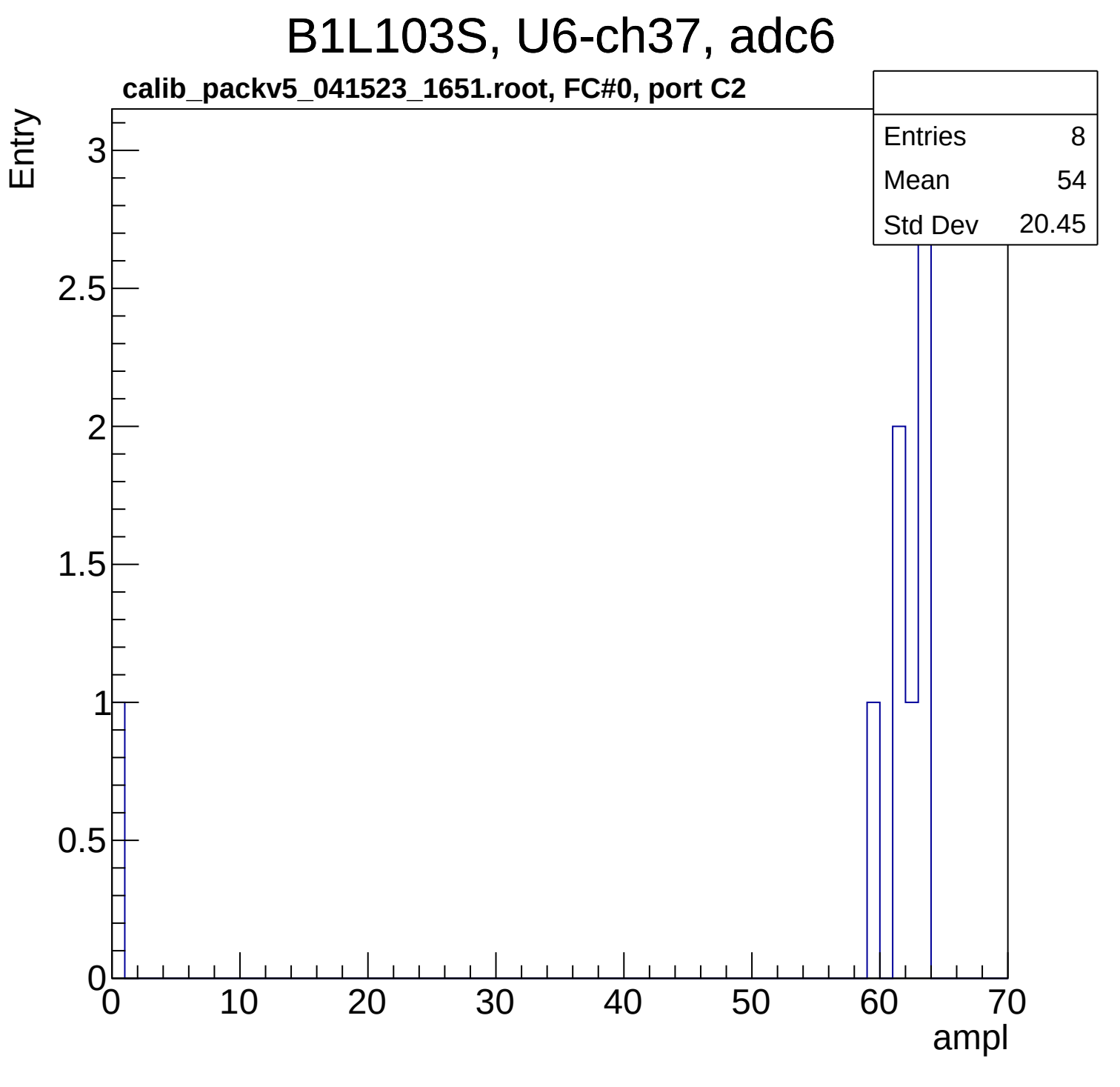
40
50
60
70


B1L103S, U6-ch37, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 54
Std Dev 20.45
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
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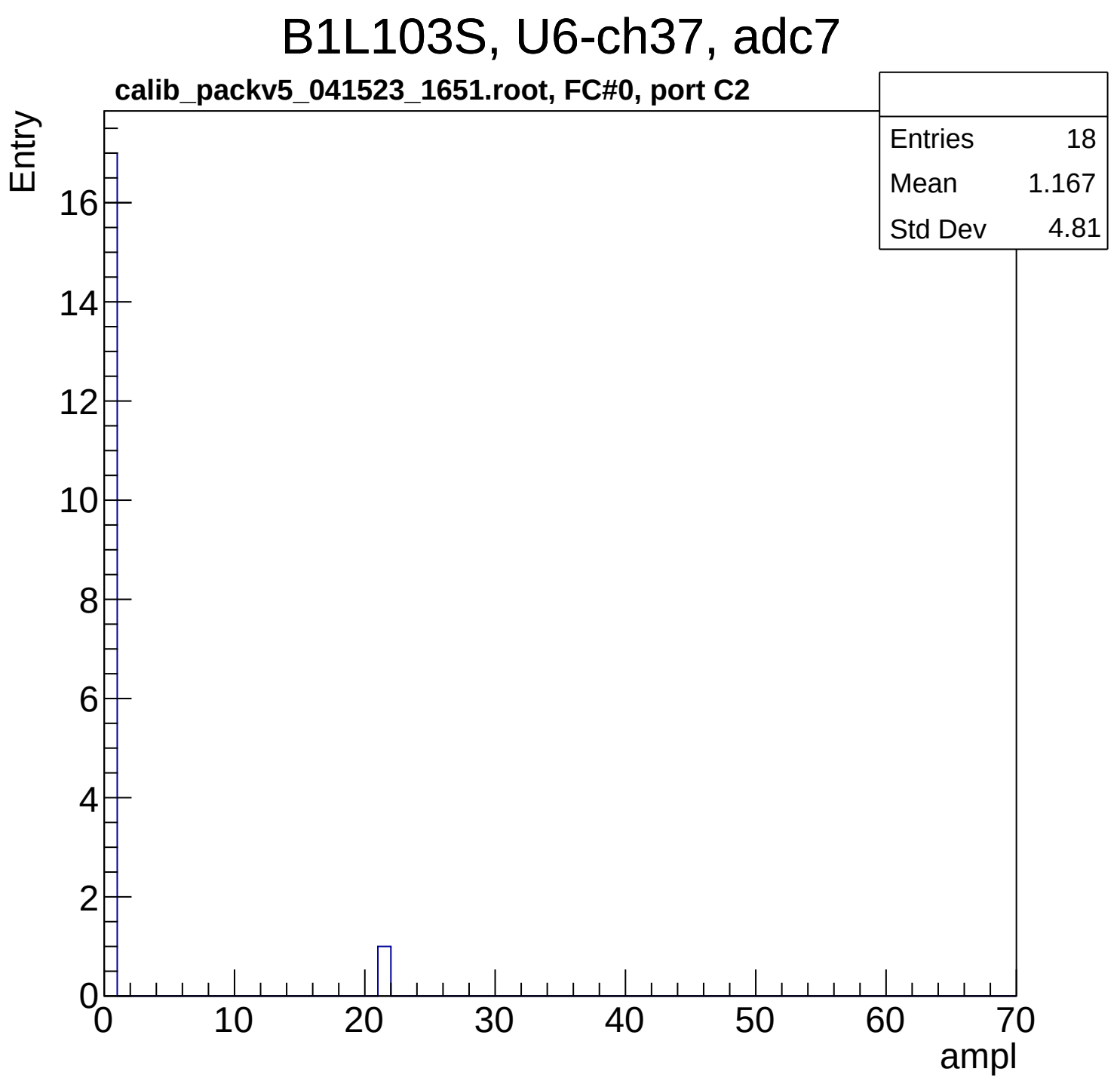
40
50
60
70


B1L103S, U6-ch37, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.167
Std Dev 4.81
Entry
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4
6
8
10
12
14
16
0
10
20
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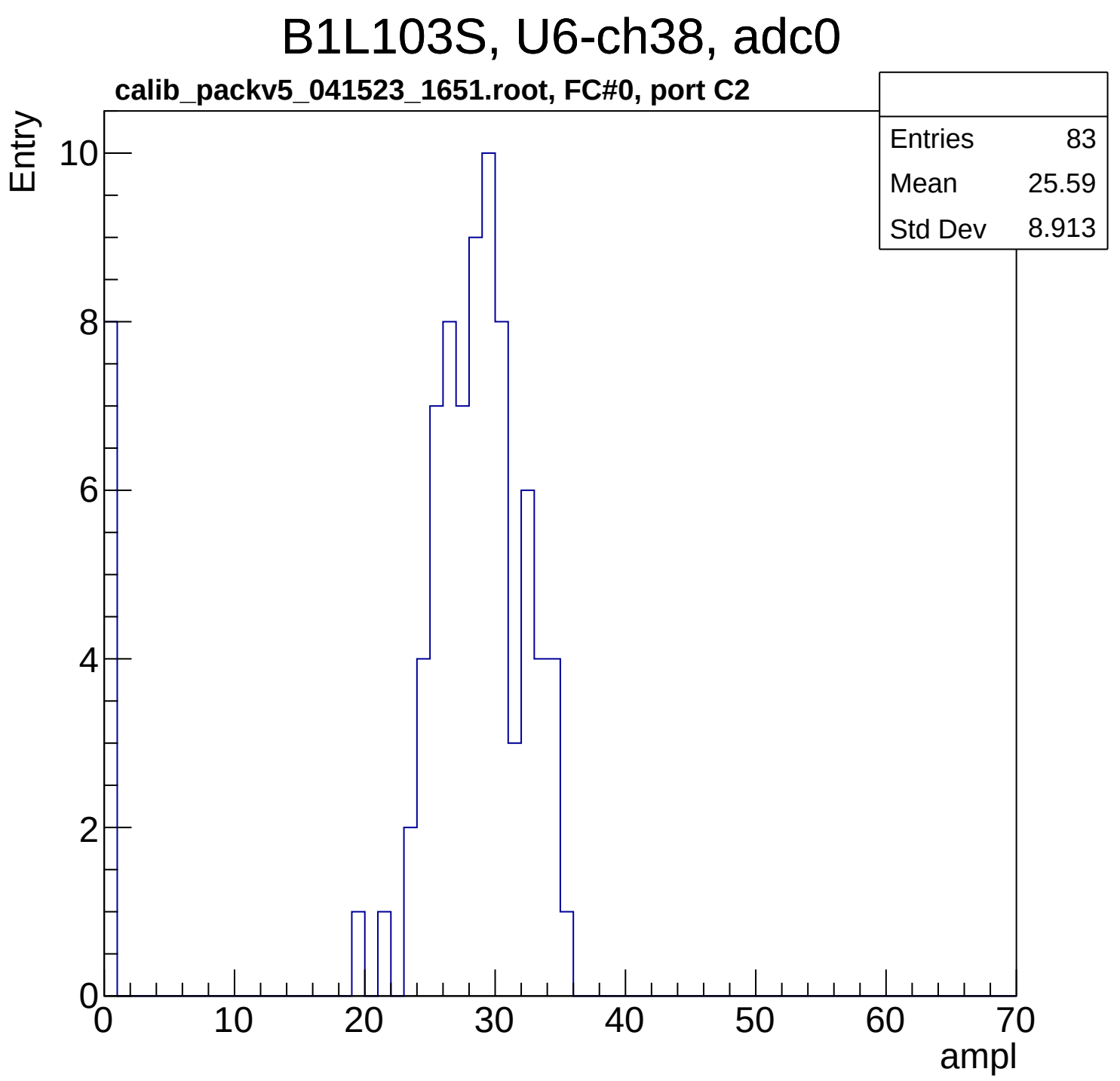
50
60
70
ampl


B1L103S, U6-ch38, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 25.59
Std Dev 8.913
Entry
ampl
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8
10
0
10
20
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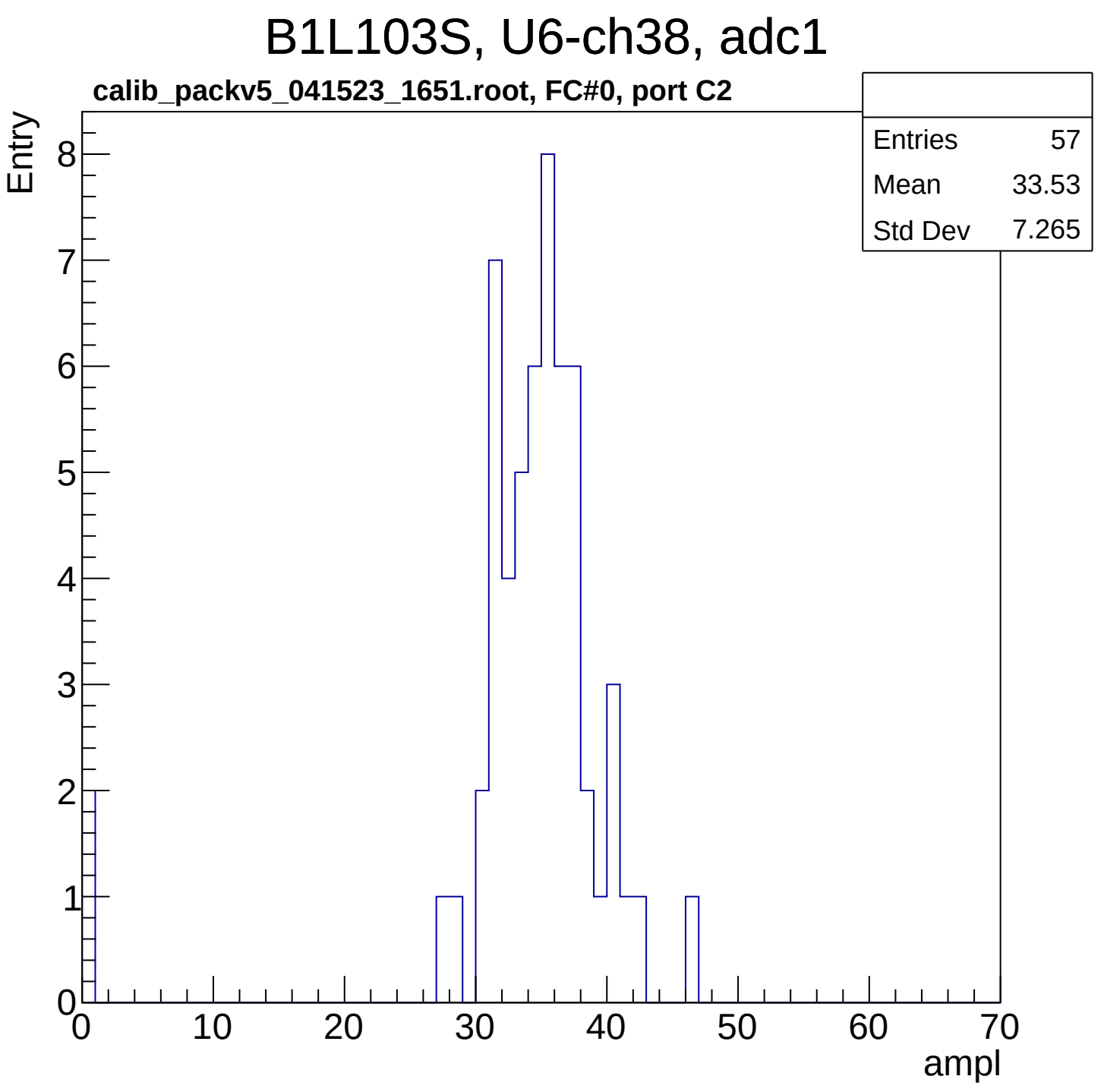
40
50
60
70


B1L103S, U6-ch38, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 33.53
Std Dev 7.265
Entry
ampl
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2
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4
5
6
7
8
0
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60
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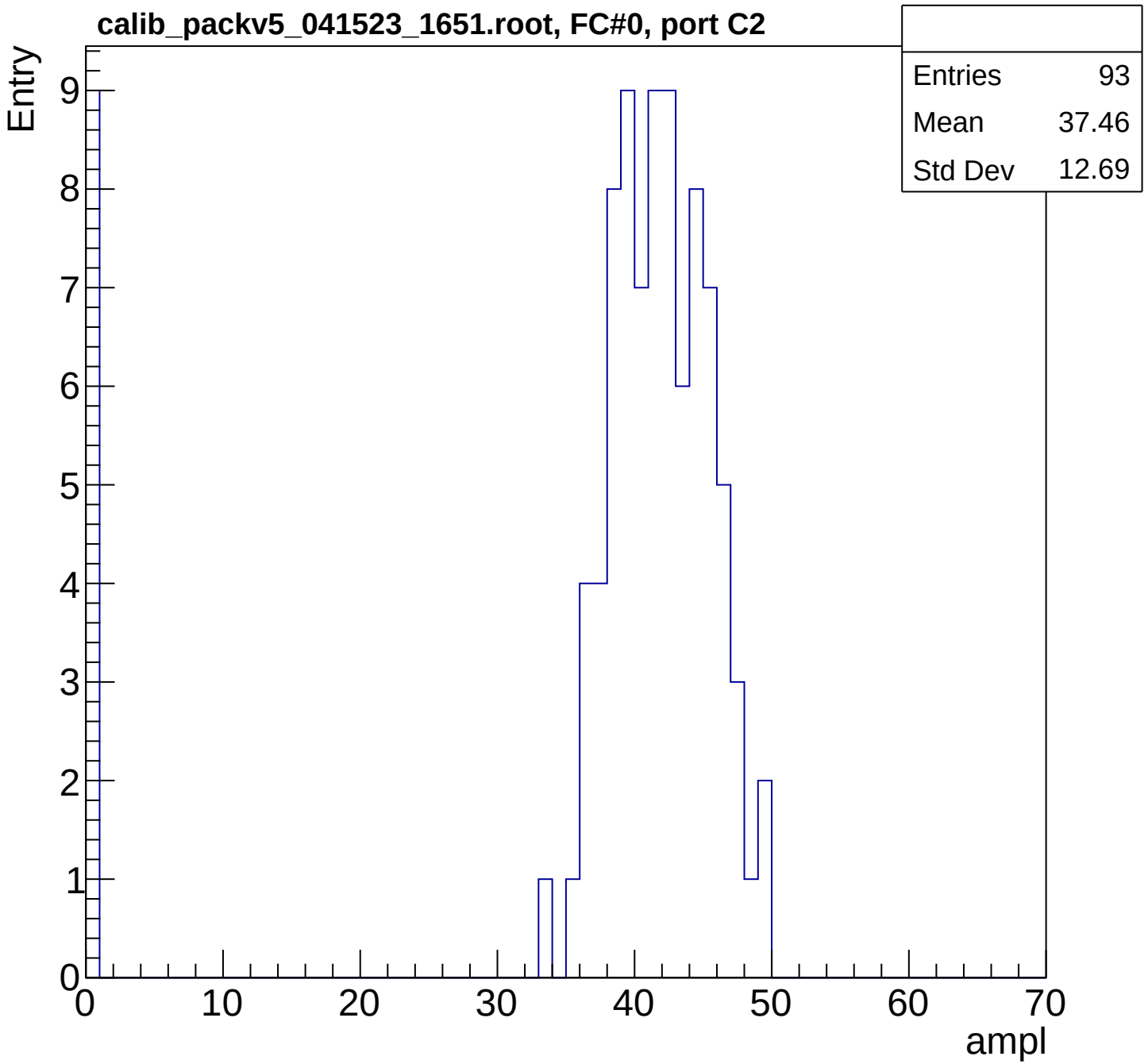
B1L103S, U6-ch38, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 37.46
Std Dev 12.69
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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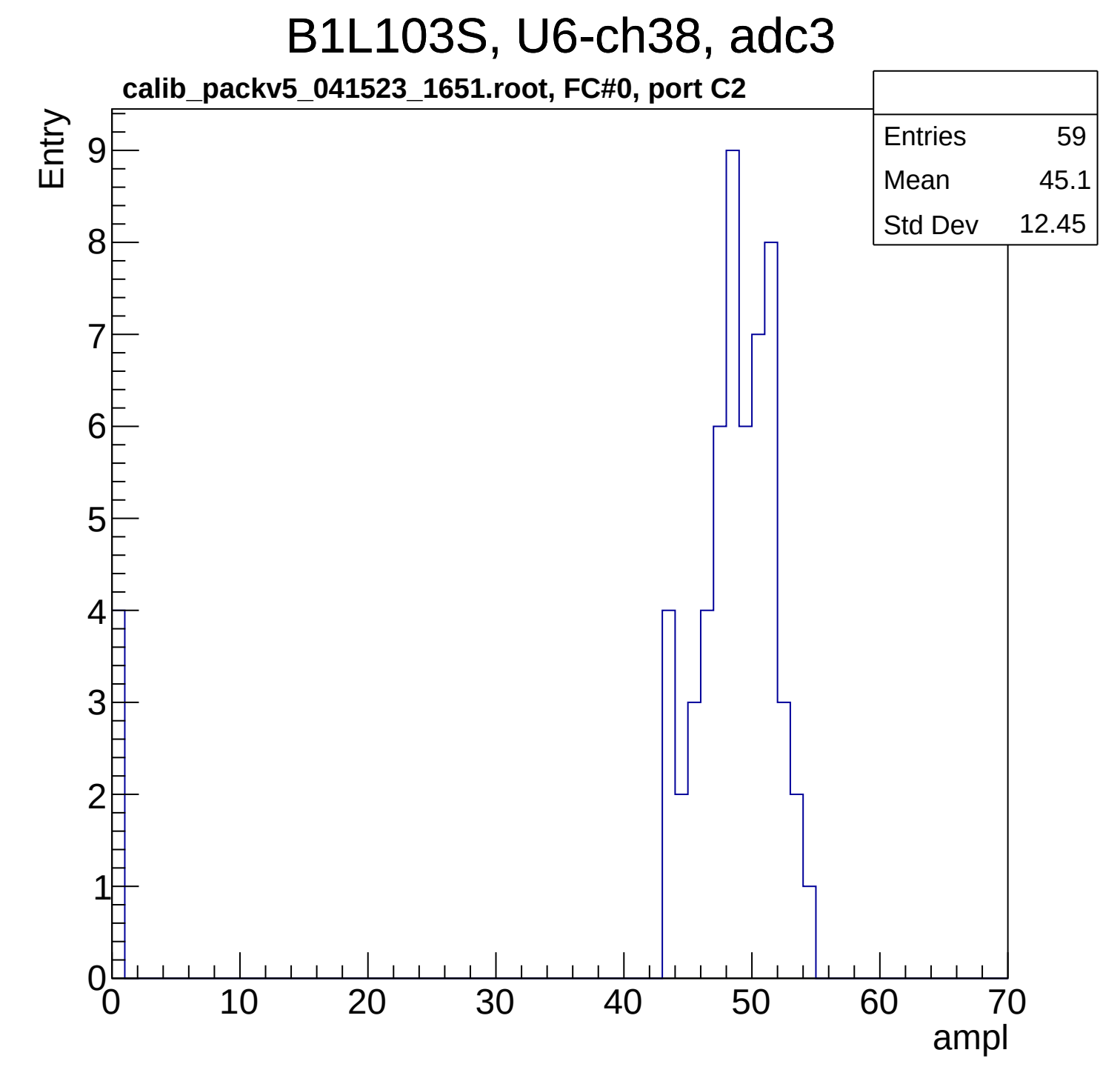
B1L103S, U6-ch38, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 45.1
Std Dev 12.45
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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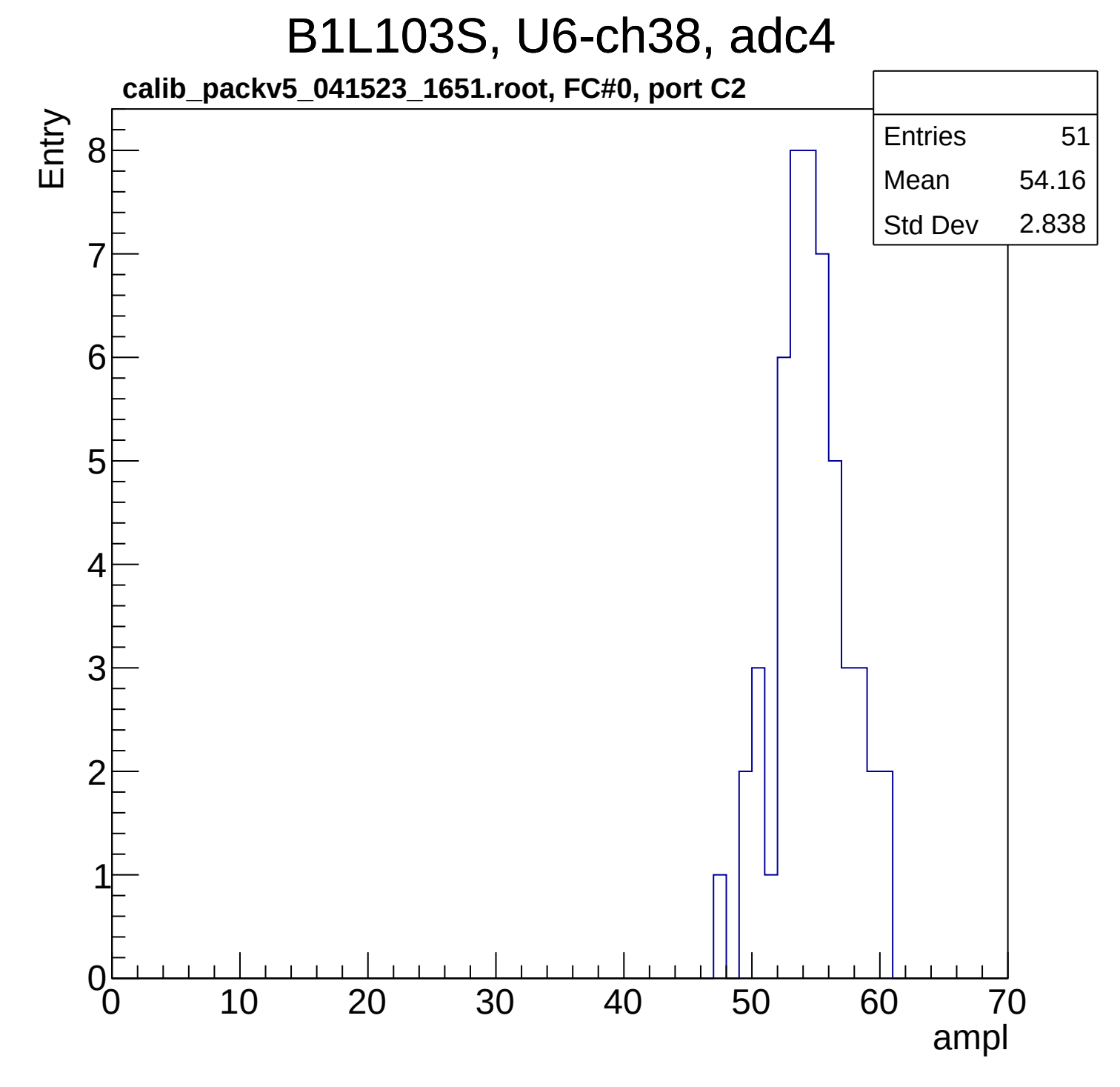
B1L103S, U6-ch38, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 54.16
Std Dev 2.838
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
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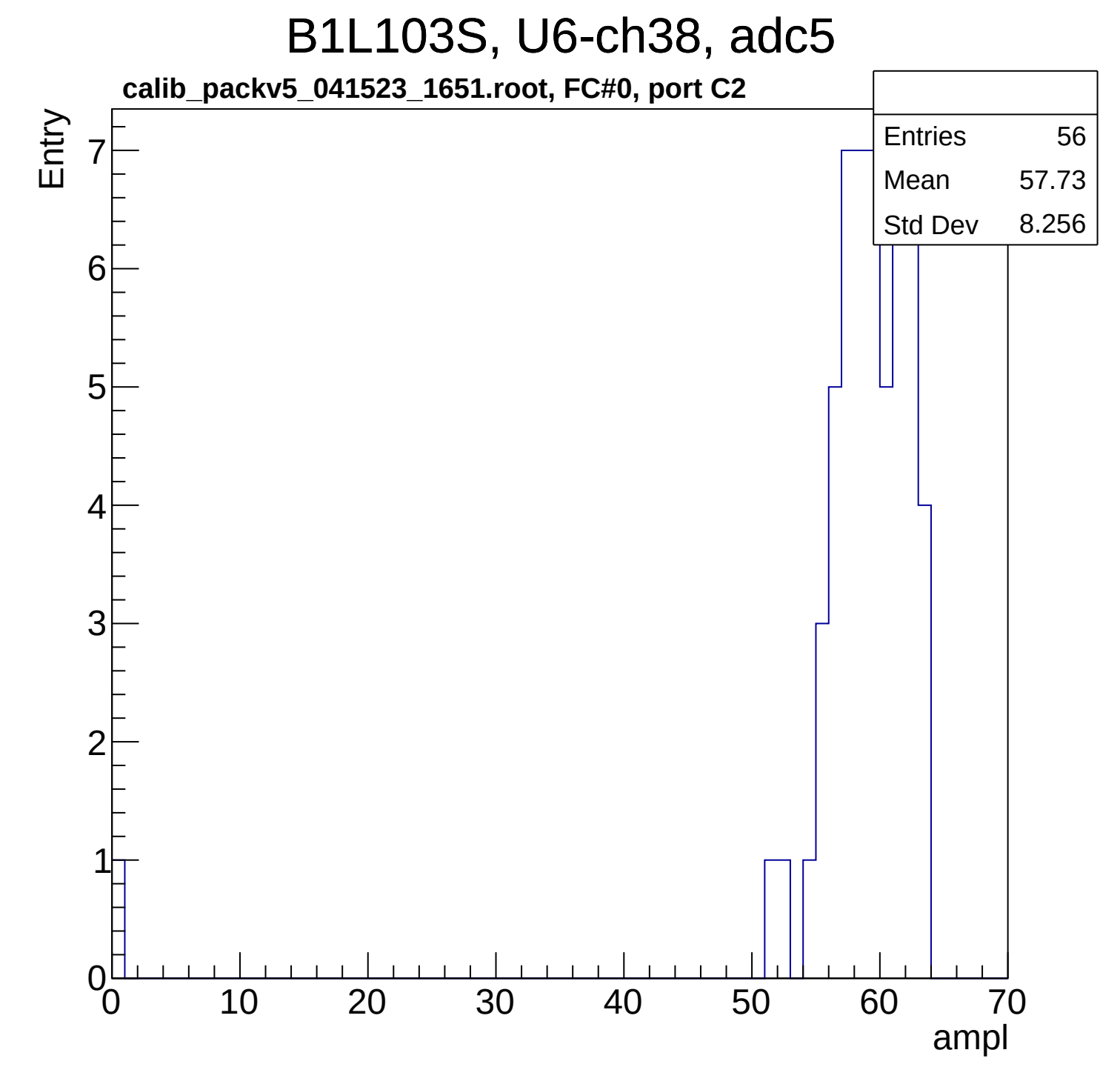
60
70


B1L103S, U6-ch38, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 57.73
Std Dev 8.256
Entry
ampl
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3
4
5
6
7
0
10
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40
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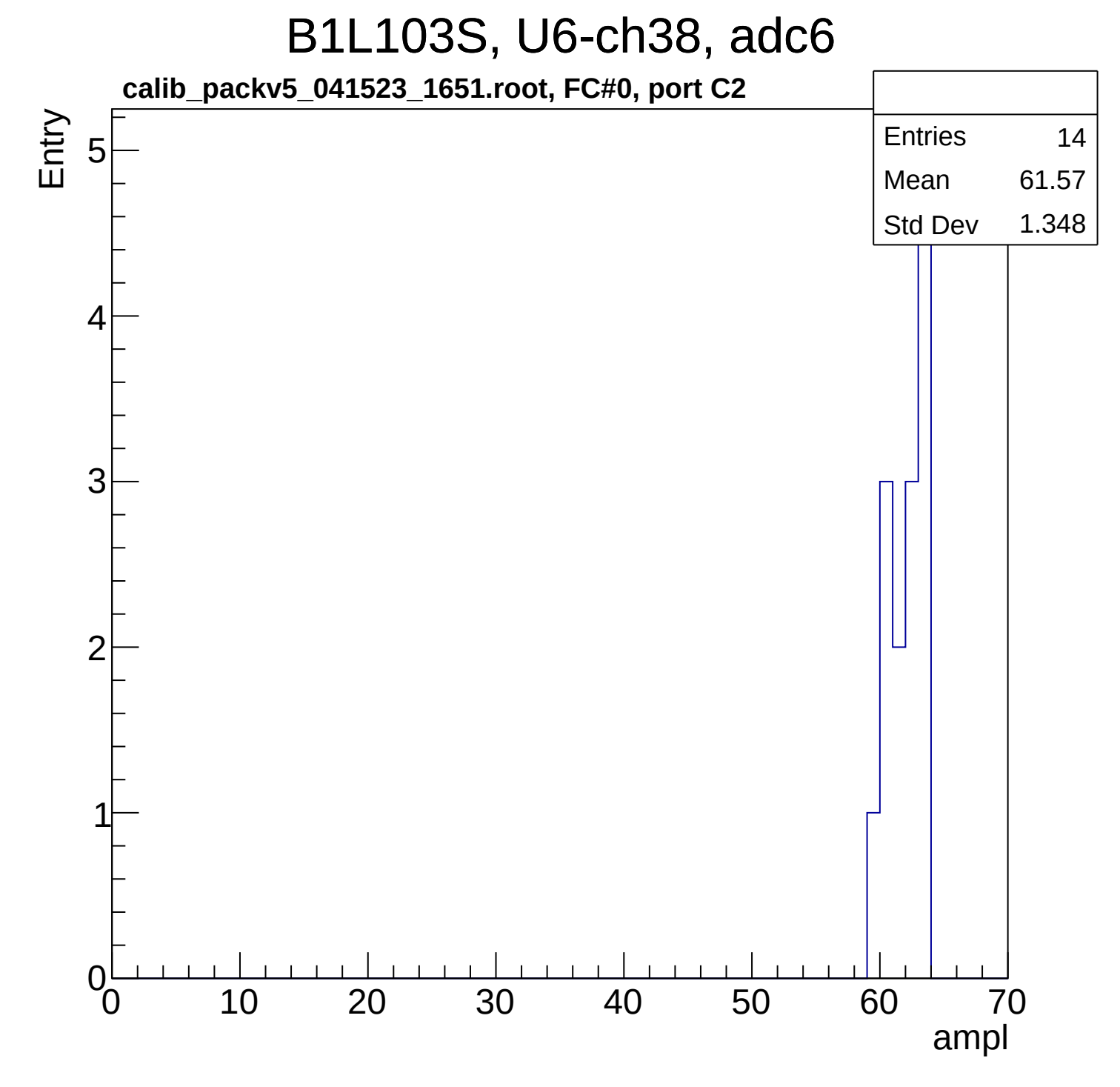
60
70


B1L103S, U6-ch38, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 61.57
Std Dev 1.348
Entry
ampl
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5
0
10
20
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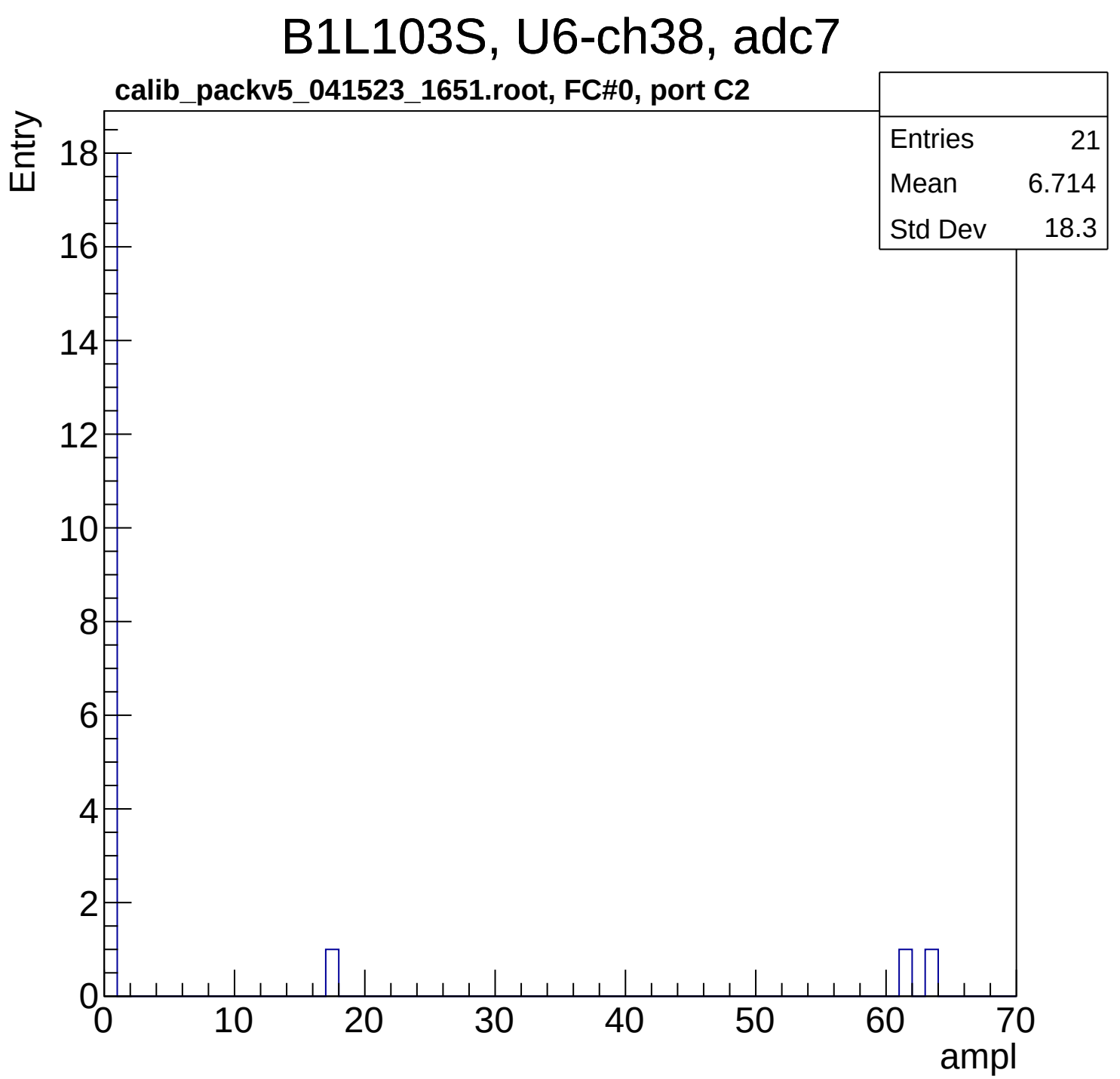
40
50
60
70


B1L103S, U6-ch38, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 6.714
Std Dev 18.3
Entry
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8
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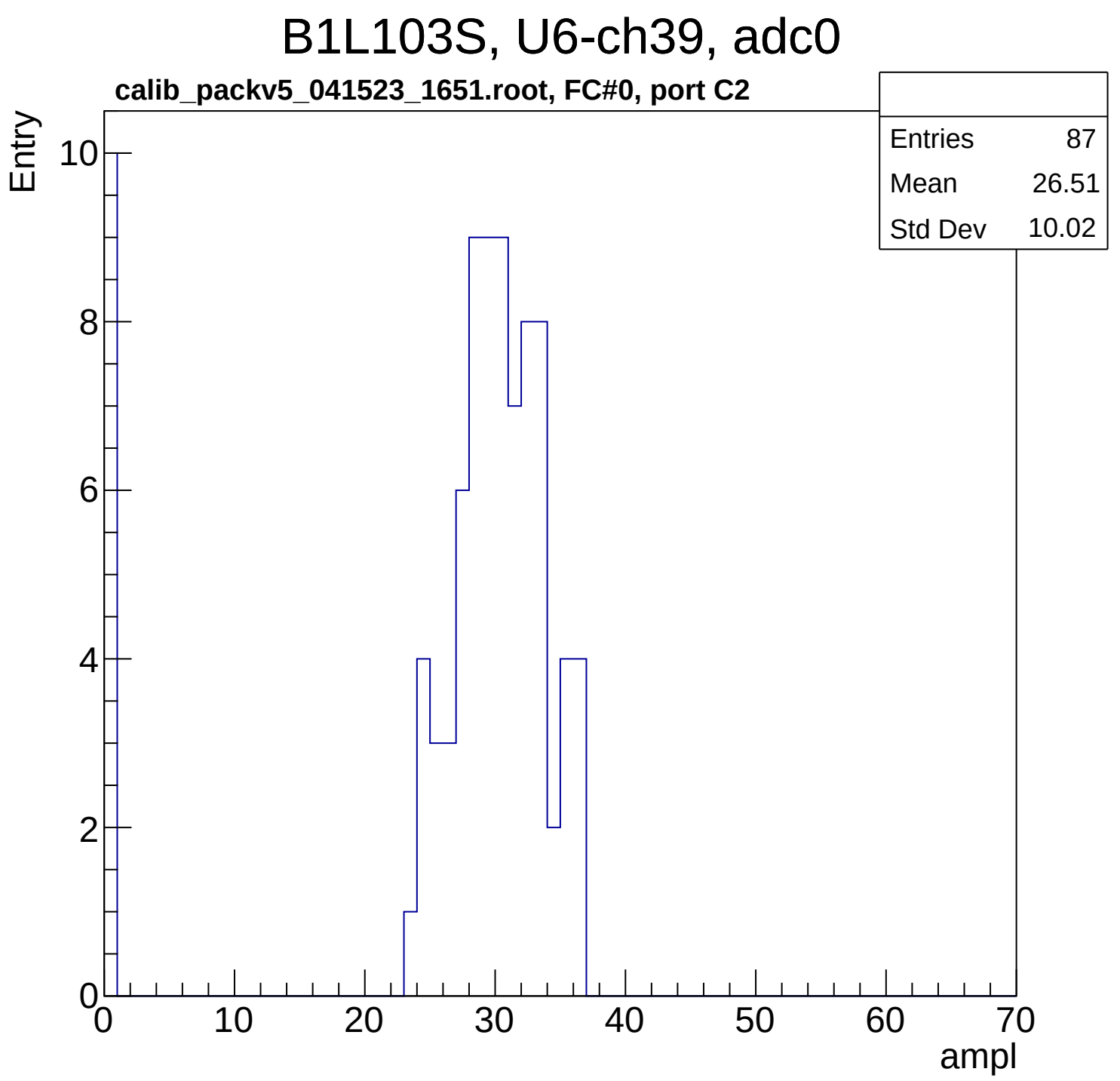
ampl


B1L103S, U6-ch39, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 26.51
Std Dev 10.02
Entry
ampl
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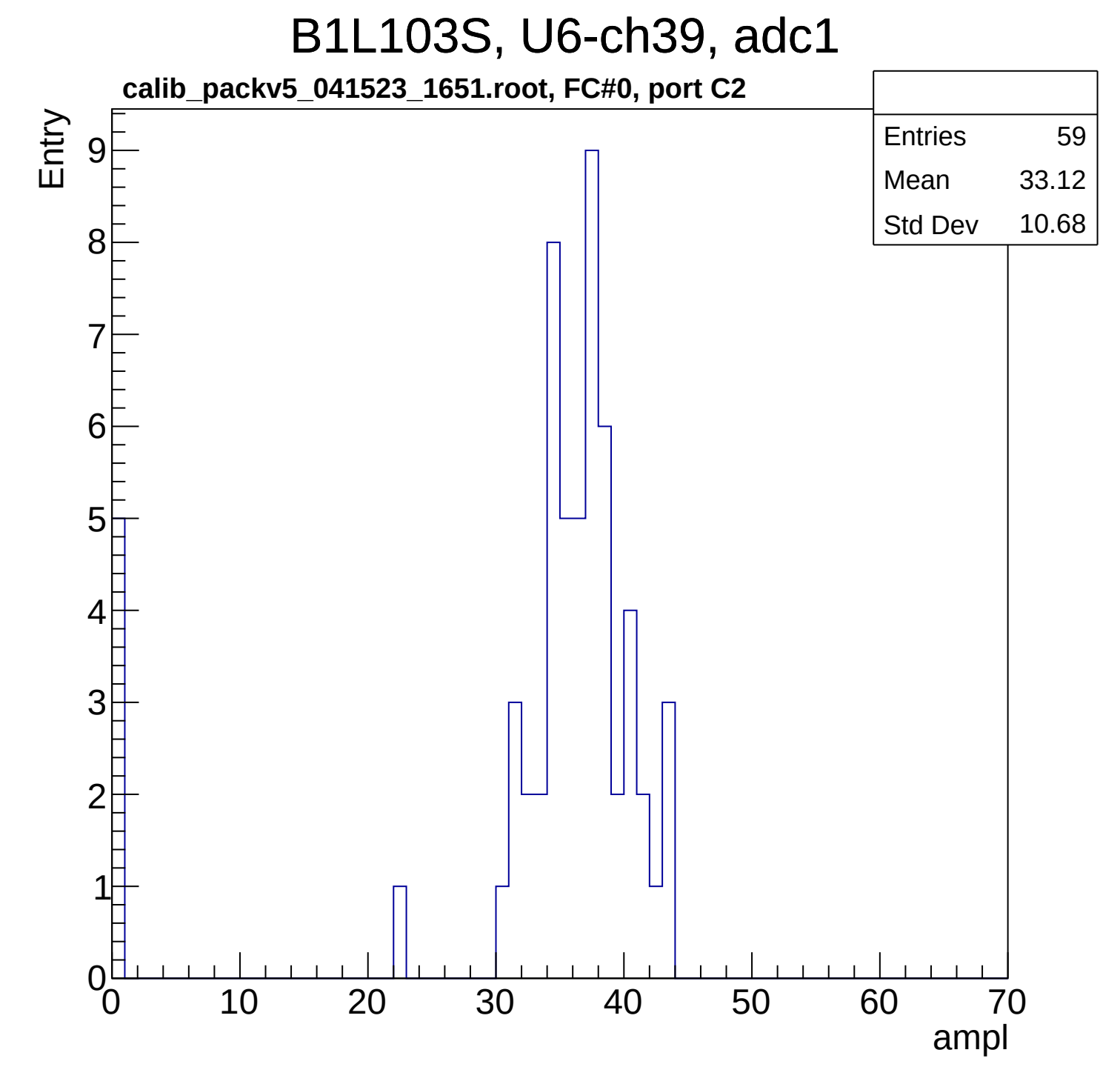
B1L103S, U6-ch39, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 33.12
Std Dev 10.68
Entry
ampl
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0
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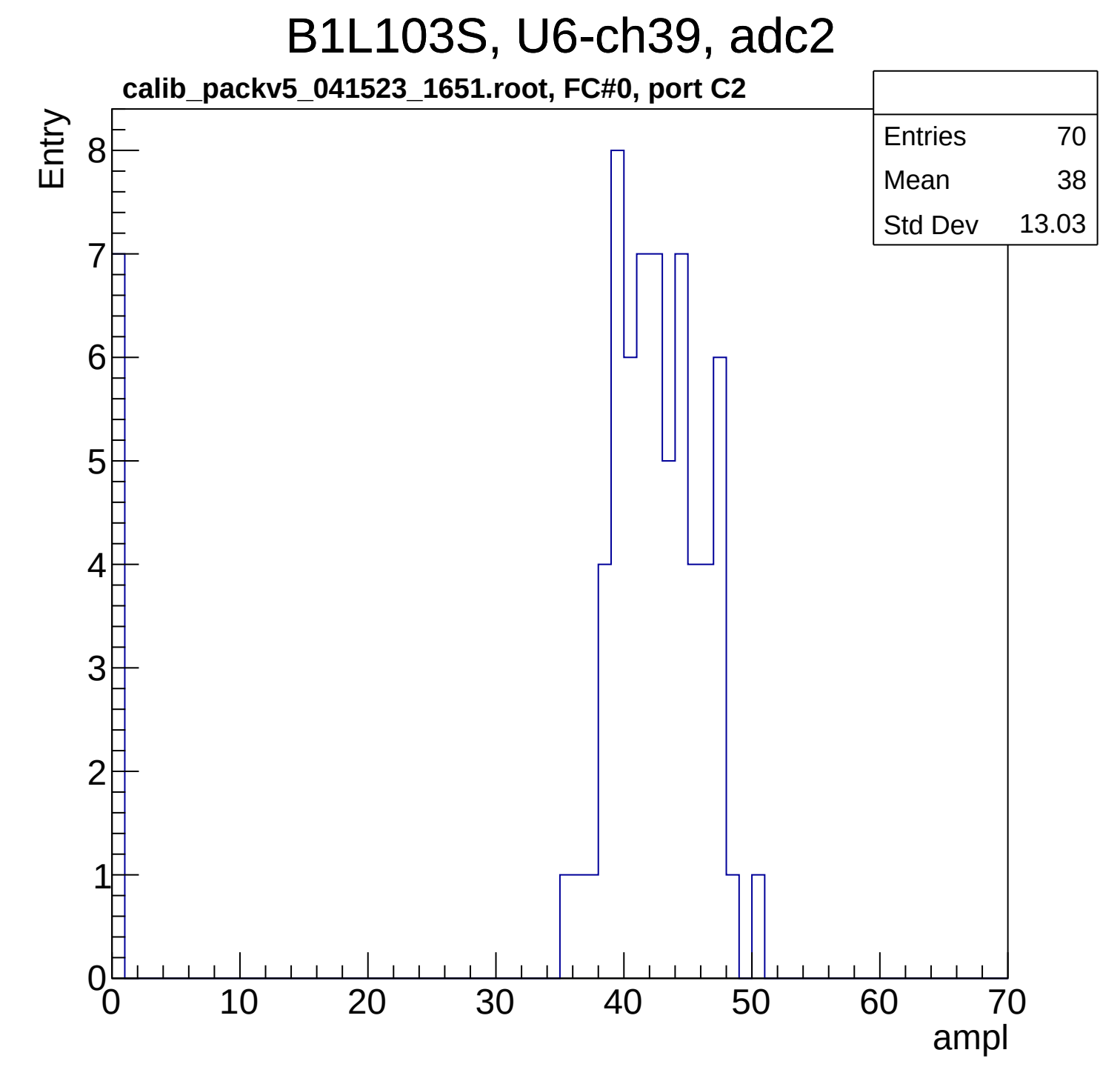
B1L103S, U6-ch39, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 38
Std Dev 13.03
Entry
ampl
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5
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7
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0
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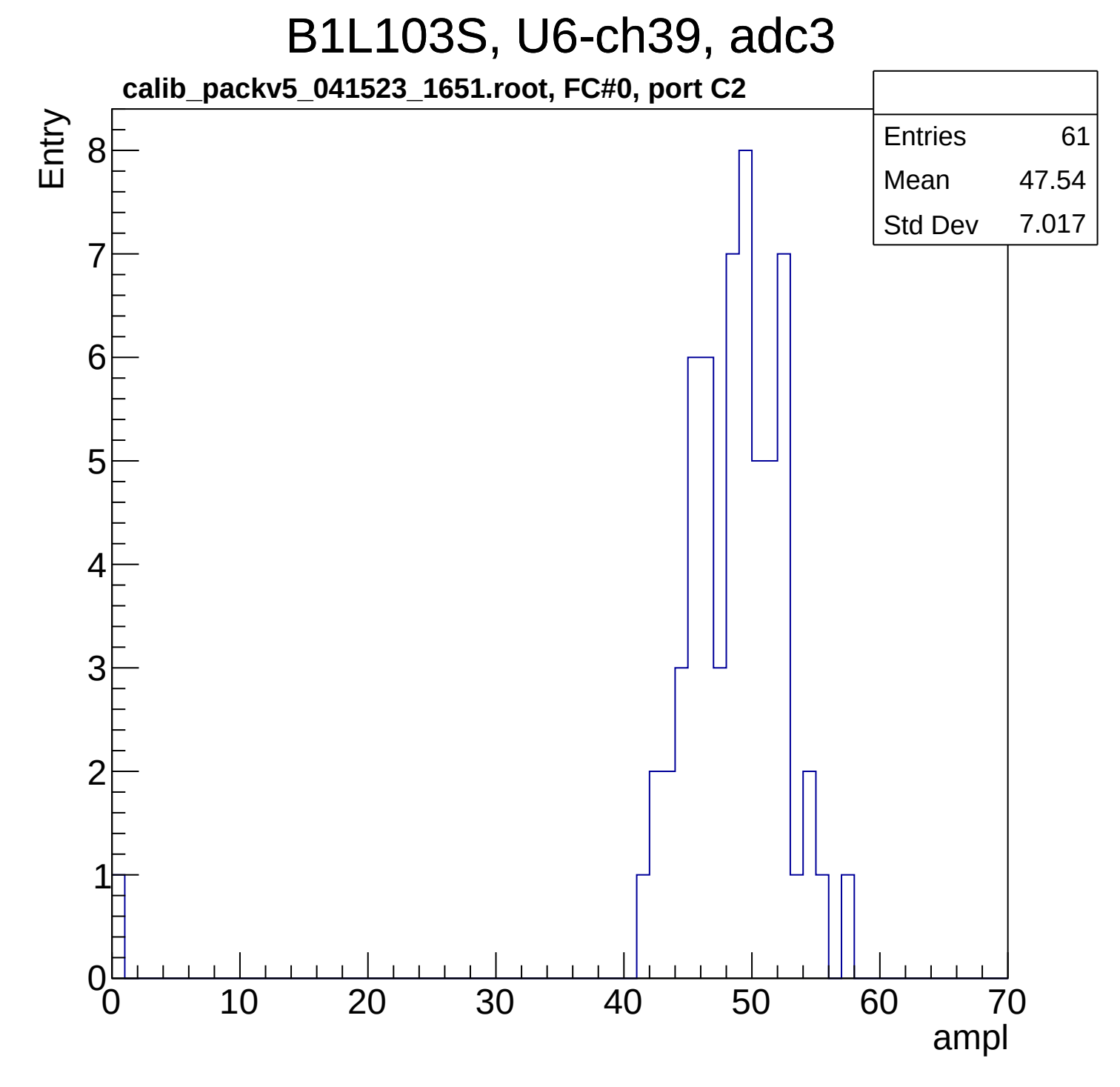
B1L103S, U6-ch39, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 47.54
Std Dev 7.017
Entry
ampl
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4
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0
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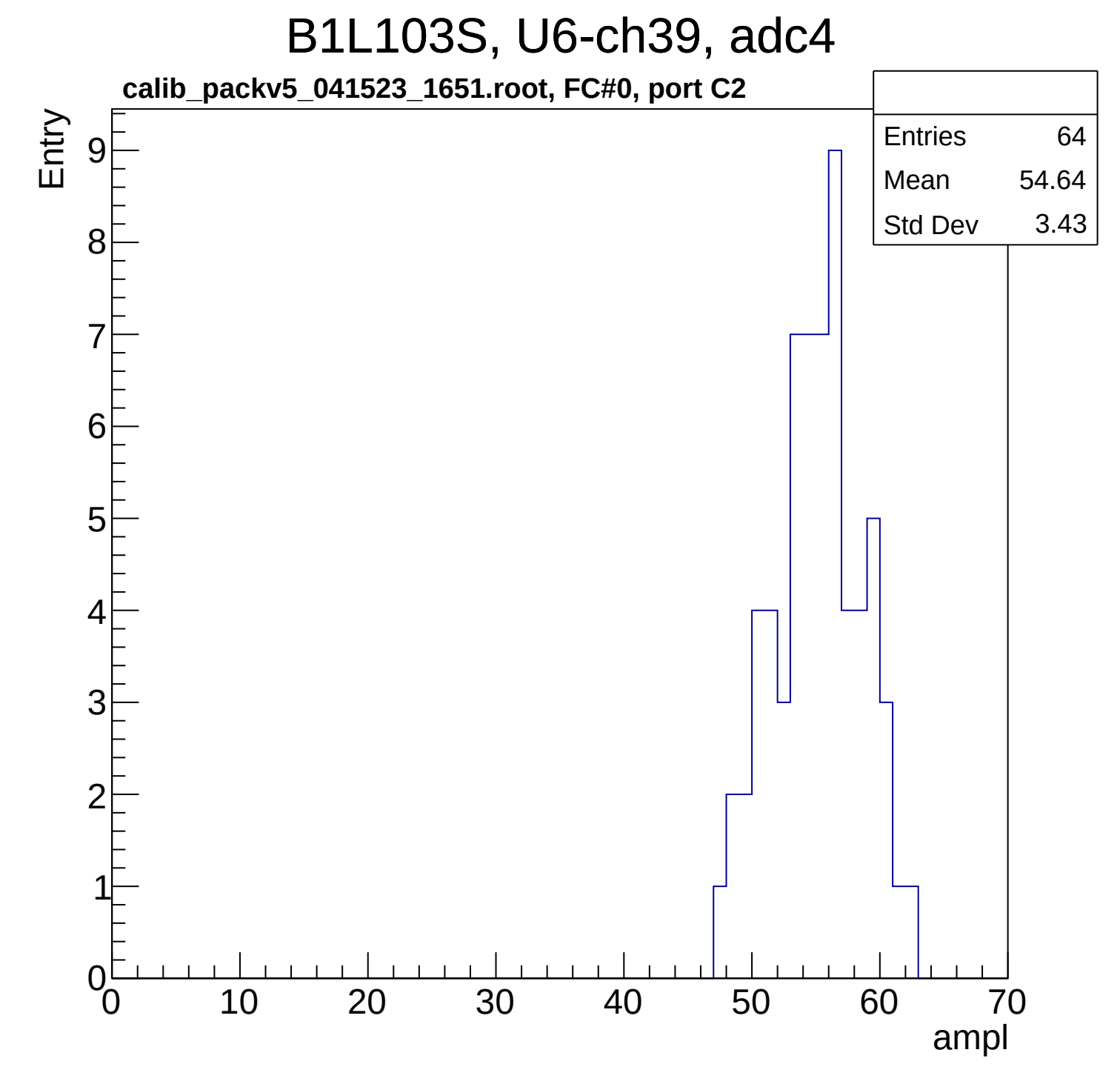
B1L103S, U6-ch39, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 54.64
Std Dev 3.43
Entry
ampl
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2
3
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6
7
8
9
0
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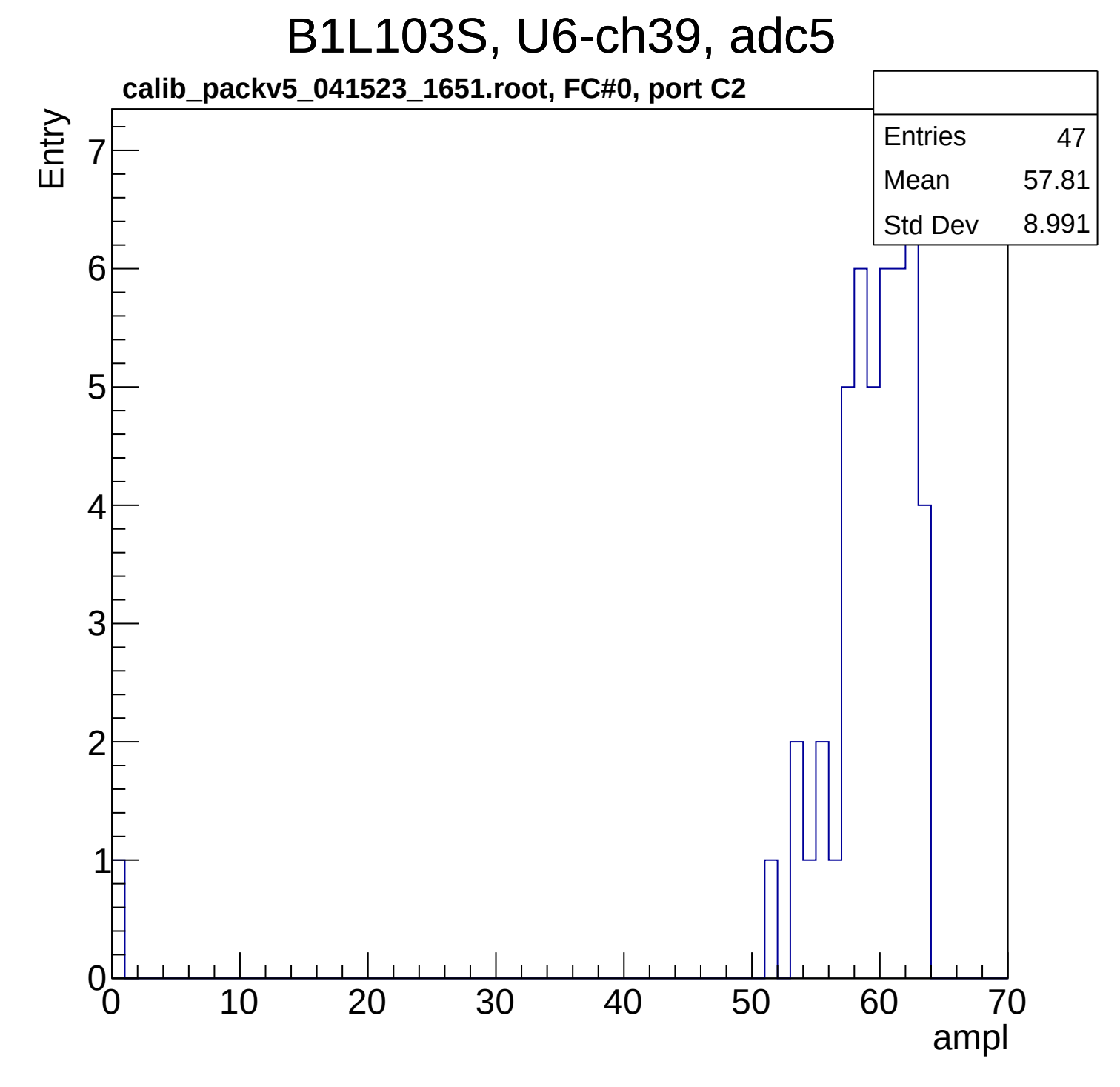
B1L103S, U6-ch39, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 57.81
Std Dev 8.991
Entry
ampl
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4
5
6
7
0
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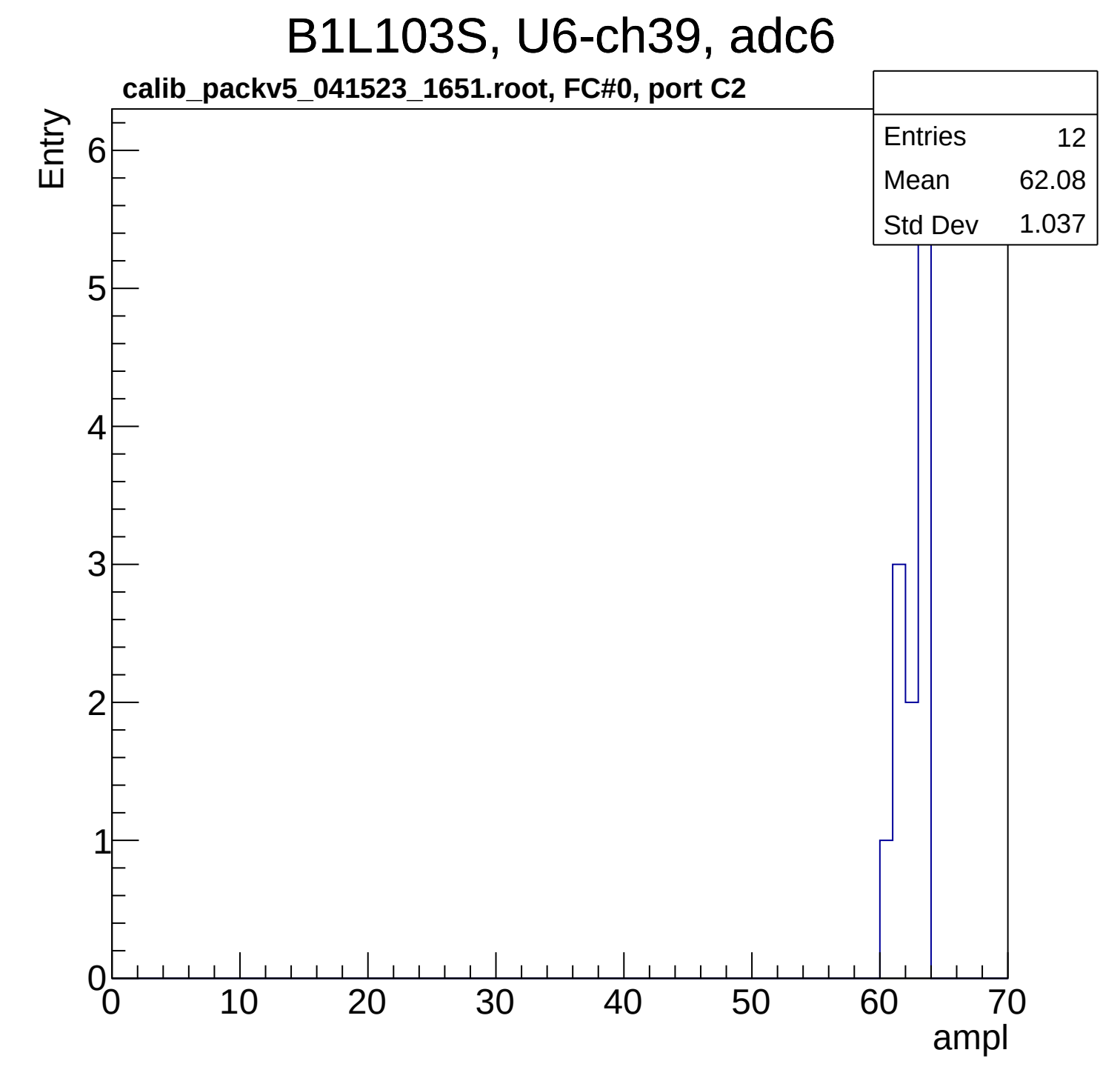
B1L103S, U6-ch39, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 62.08
Std Dev 1.037
Entry
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3
4
5
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10
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50
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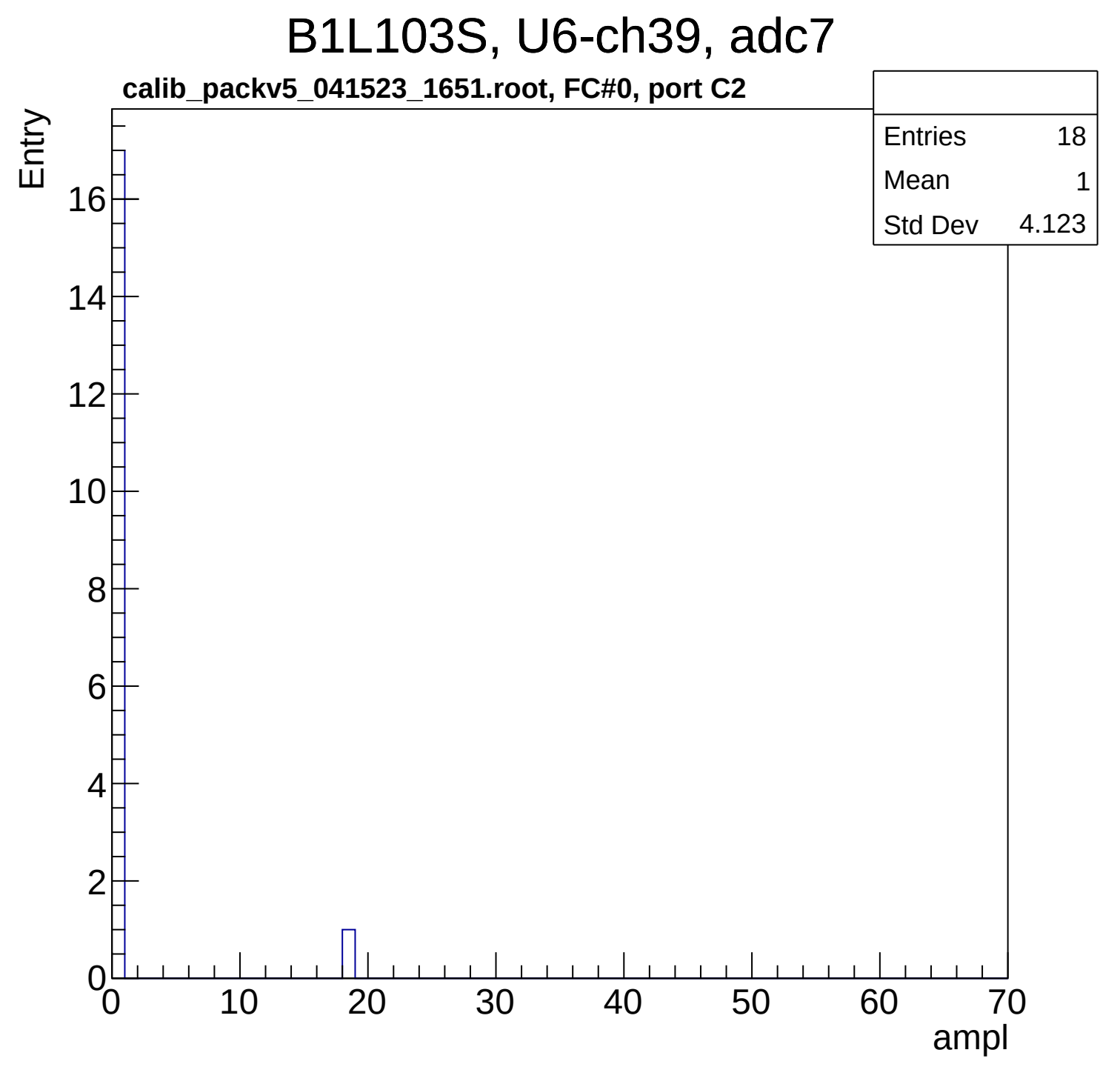
70
ampl


B1L103S, U6-ch39, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1
Std Dev 4.123
Entry
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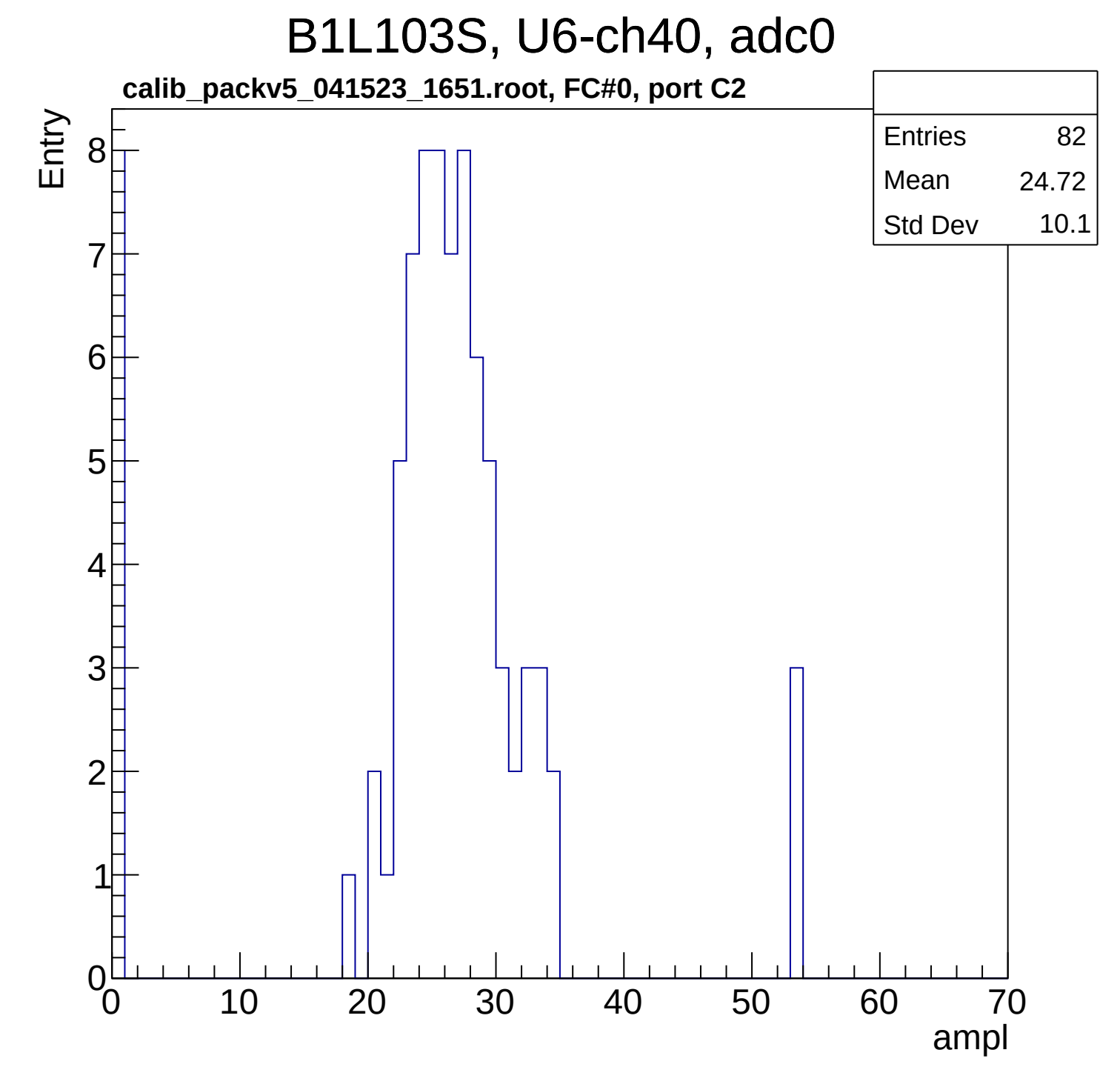
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch40, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 24.72
Std Dev 10.1
Entry
ampl
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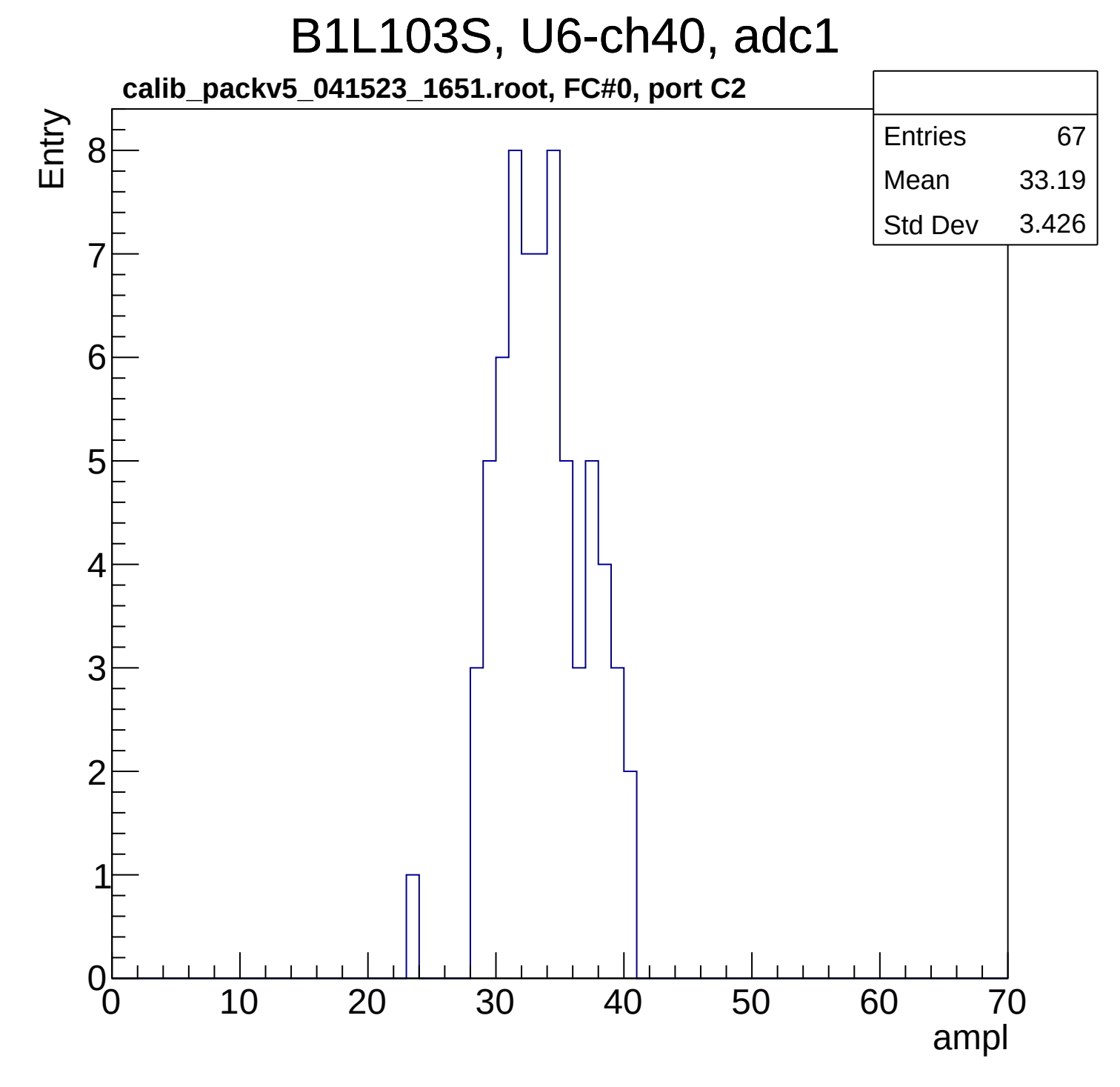
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch40, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 33.19
Std Dev 3.426
Entry
ampl
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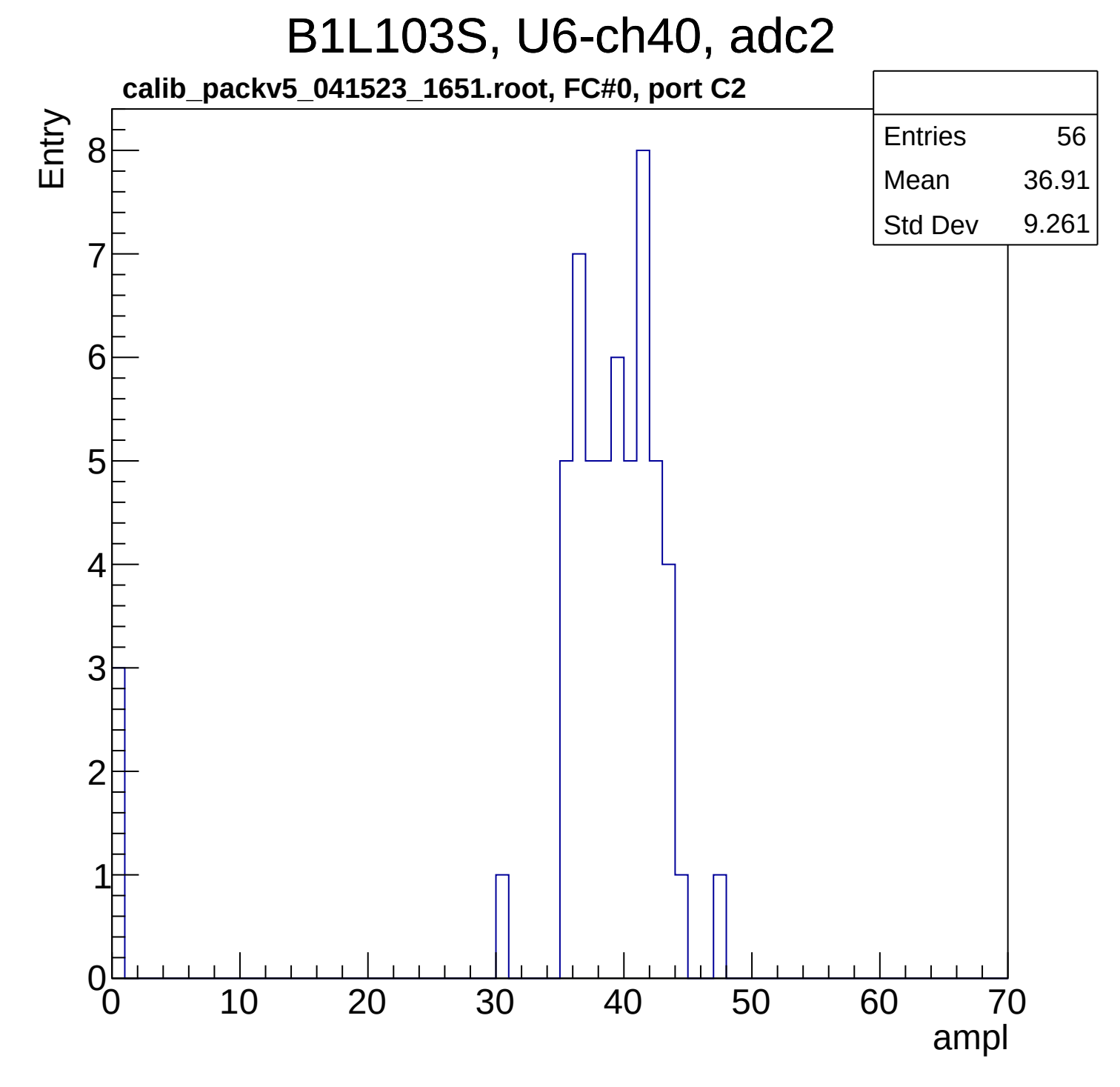
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch40, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 36.91
Std Dev 9.261
Entry
ampl
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2
3
4
5
6
7
8
0
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60
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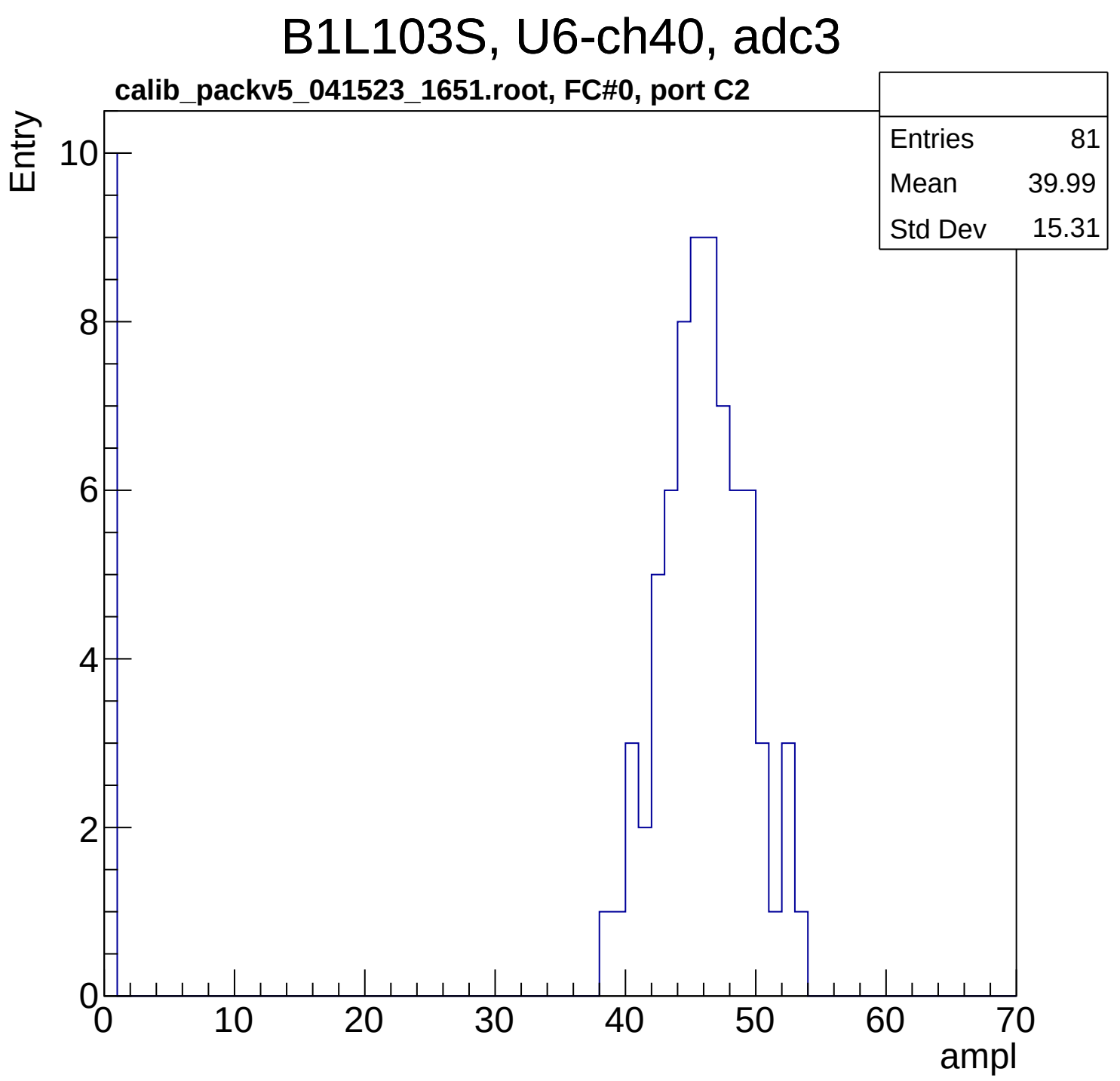
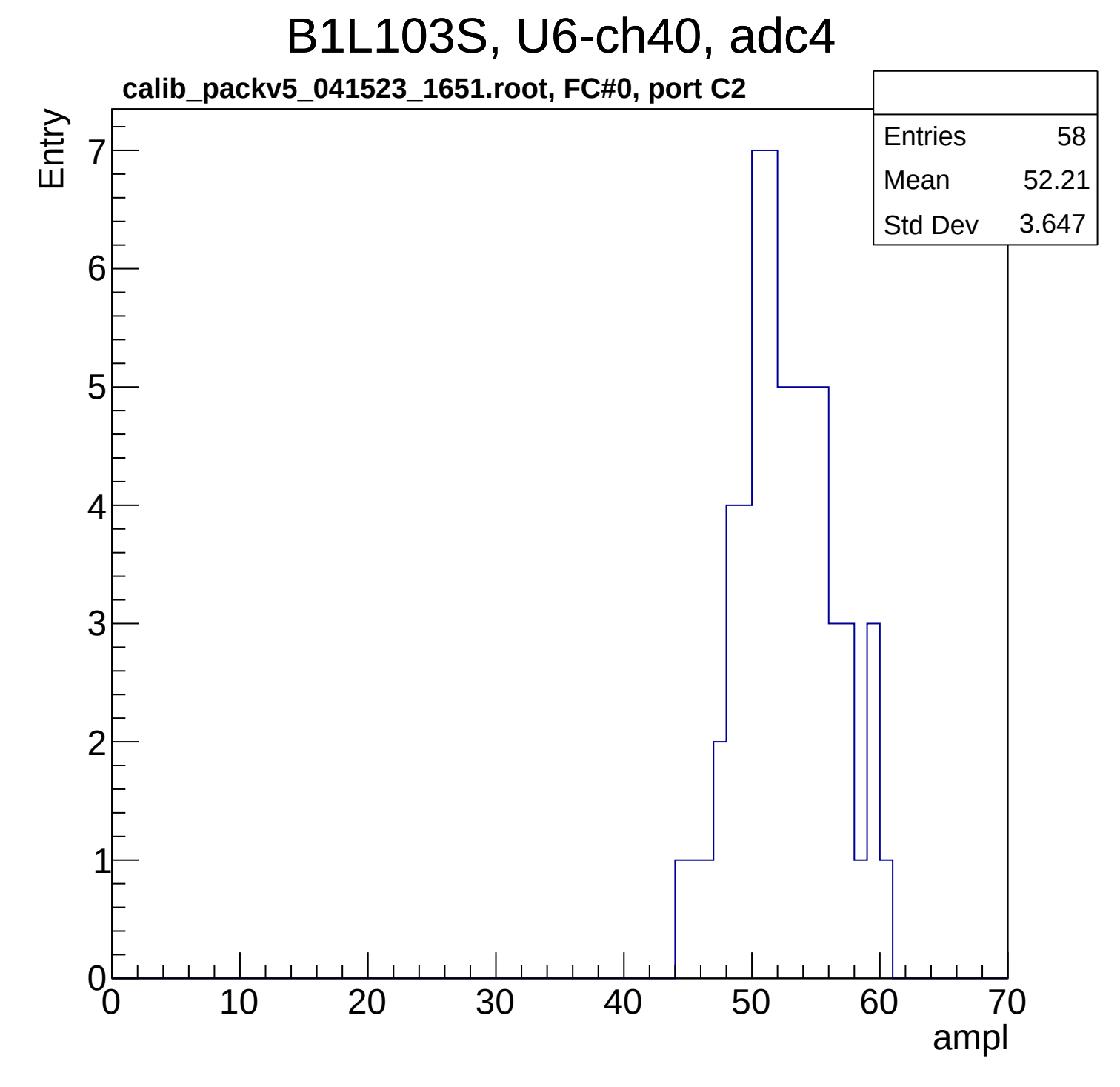
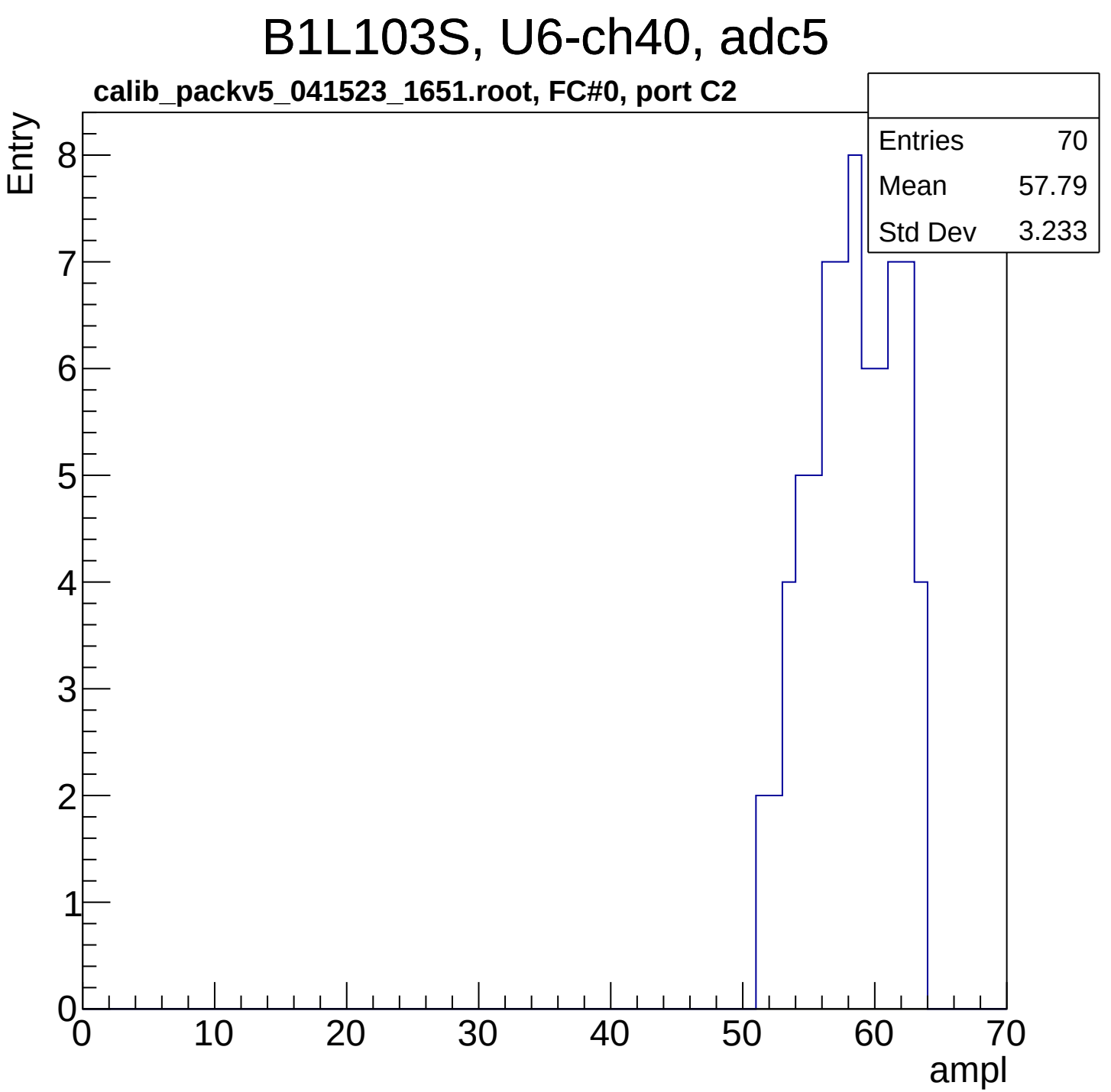

B1L103S, U6-ch40, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 39.99
Std Dev 15.31
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch40, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 52.21
Std Dev 3.647
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U6-ch40, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 57.79
Std Dev 3.233
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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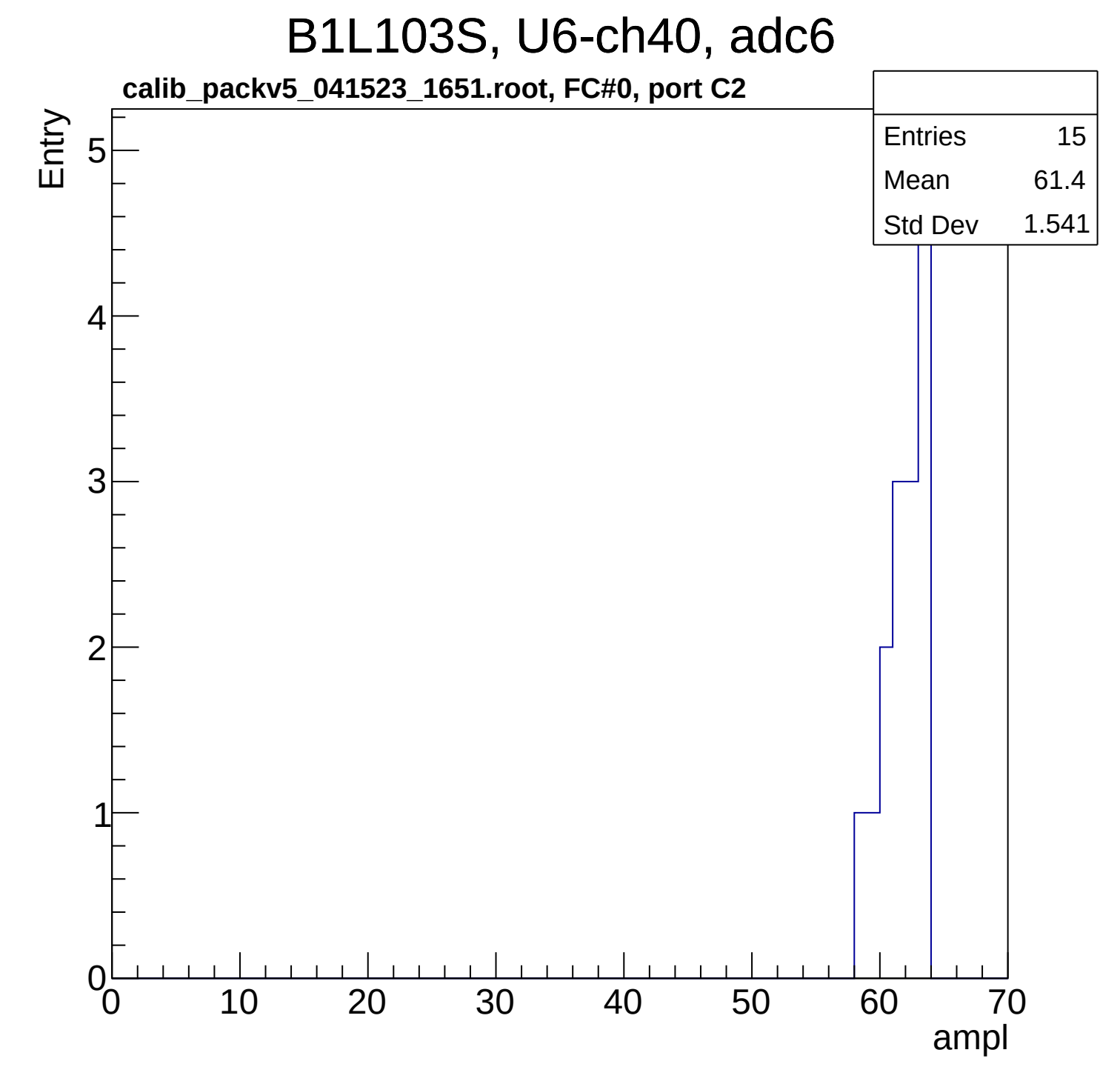
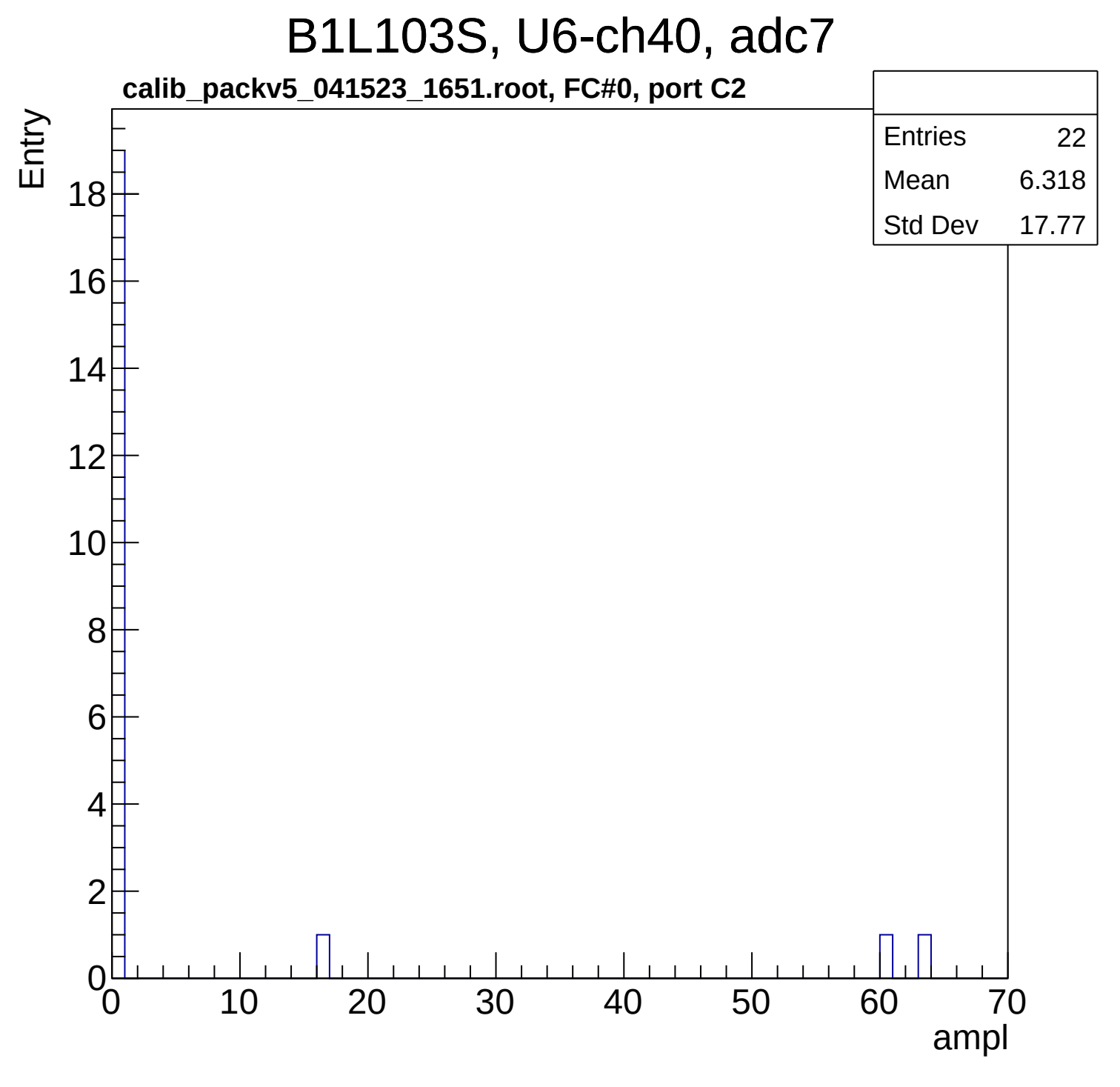

B1L103S, U6-ch40, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 61.4
Std Dev 1.541
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U6-ch40, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 6.318
Std Dev 17.77
Entry
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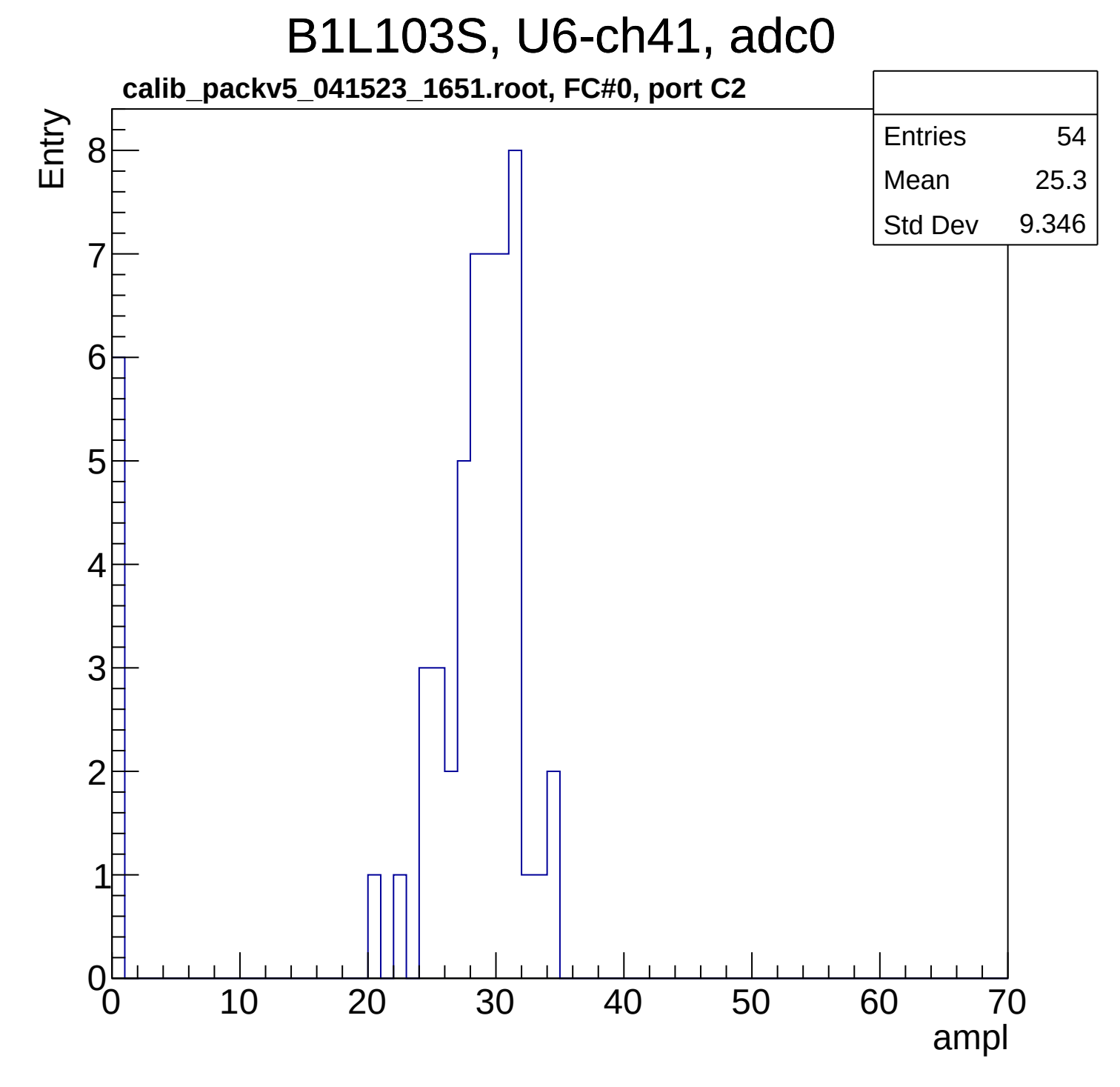
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch41, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 25.3
Std Dev 9.346
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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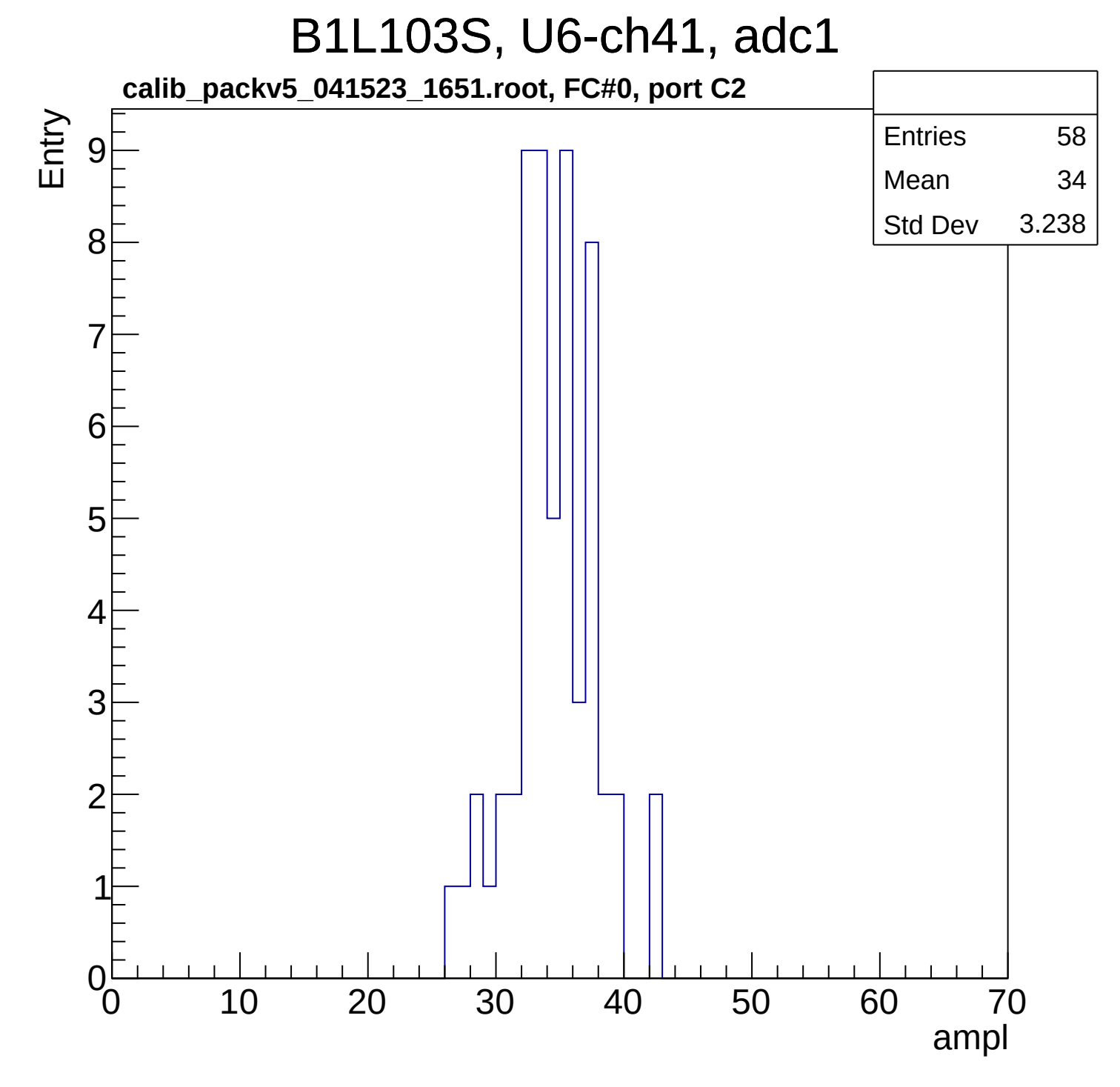
40
50
60
70


B1L103S, U6-ch41, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 34
Std Dev 3.238
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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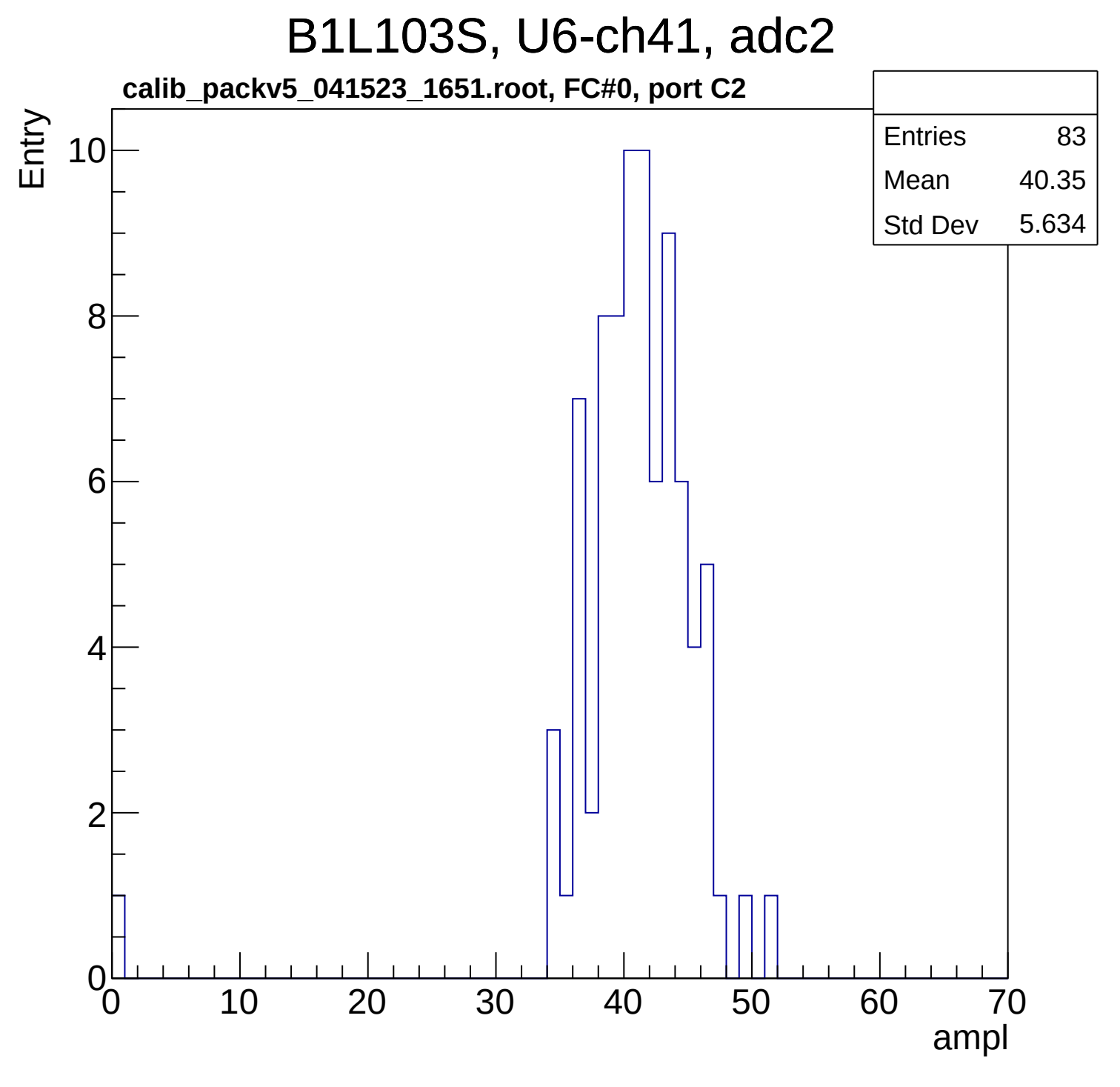
60
70


B1L103S, U6-ch41, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 40.35
Std Dev 5.634
Entry
ampl
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2
4
6
8
10
0
10
20
30
40
50
60
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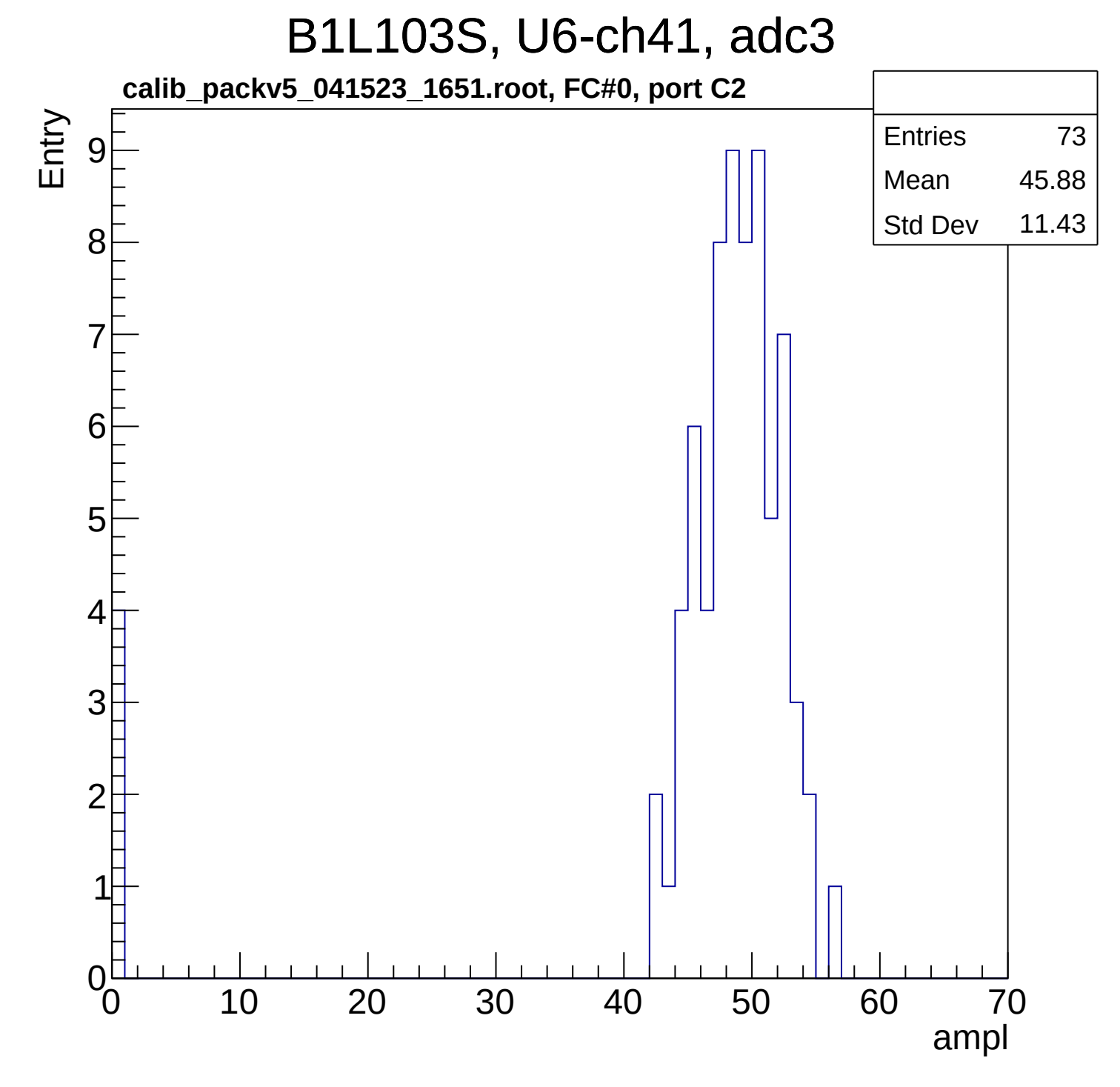
B1L103S, U6-ch41, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 45.88
Std Dev 11.43
Entry
ampl
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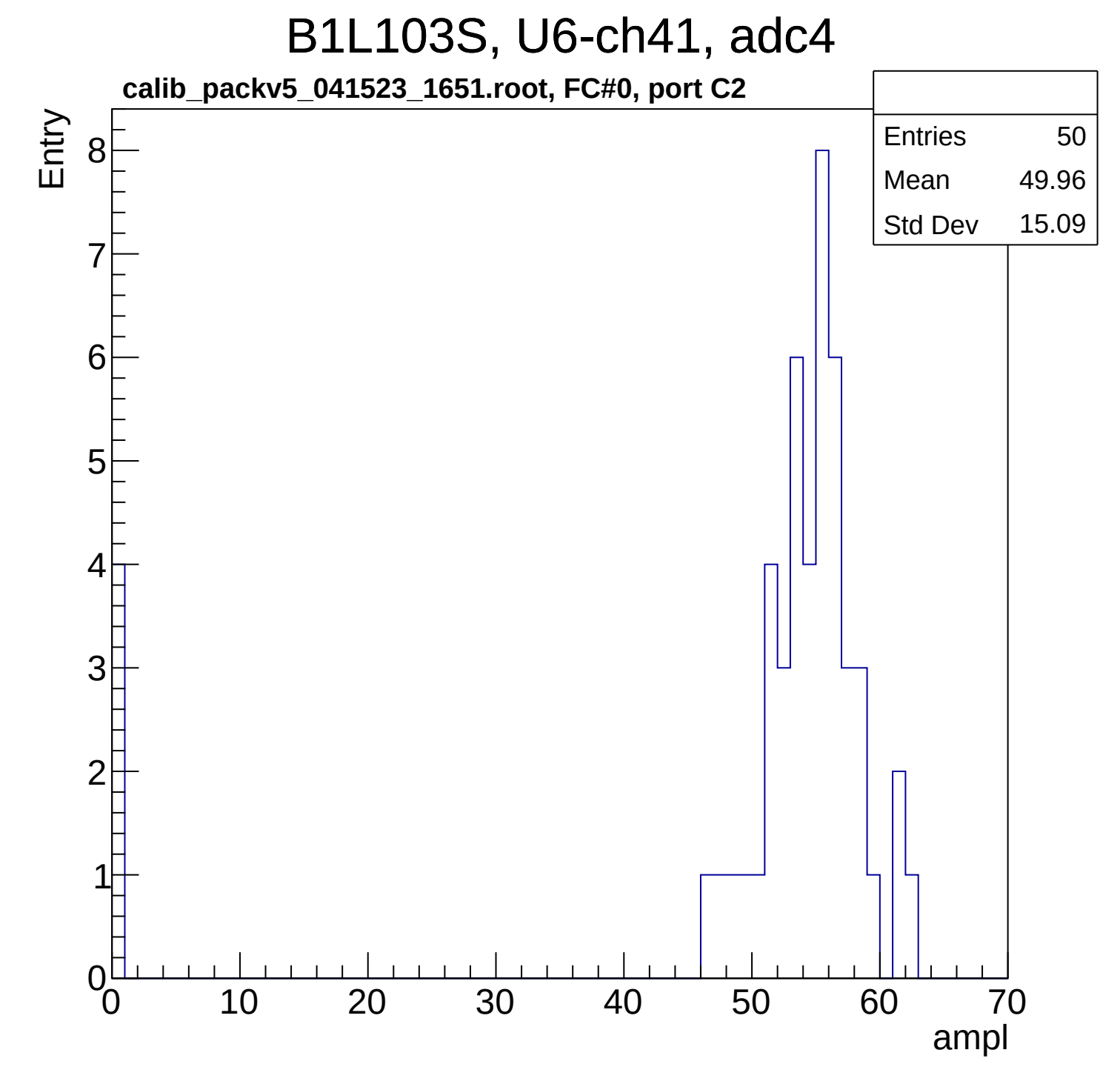
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch41, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 49.96
Std Dev 15.09
Entry
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2
3
4
5
6
7
8
0
10
20
30
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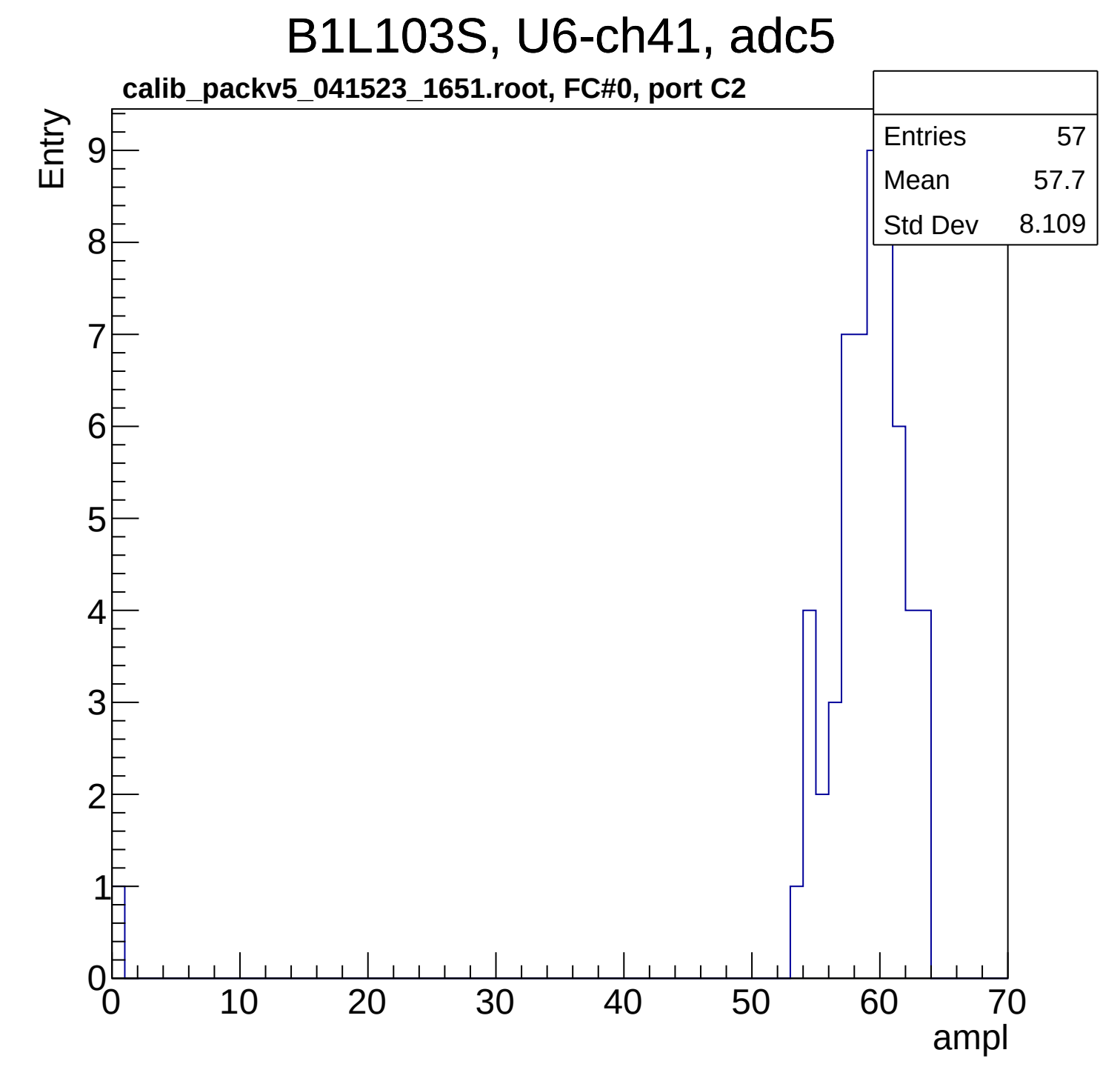
50
60
70
ampl


B1L103S, U6-ch41, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 57.7
Std Dev 8.109
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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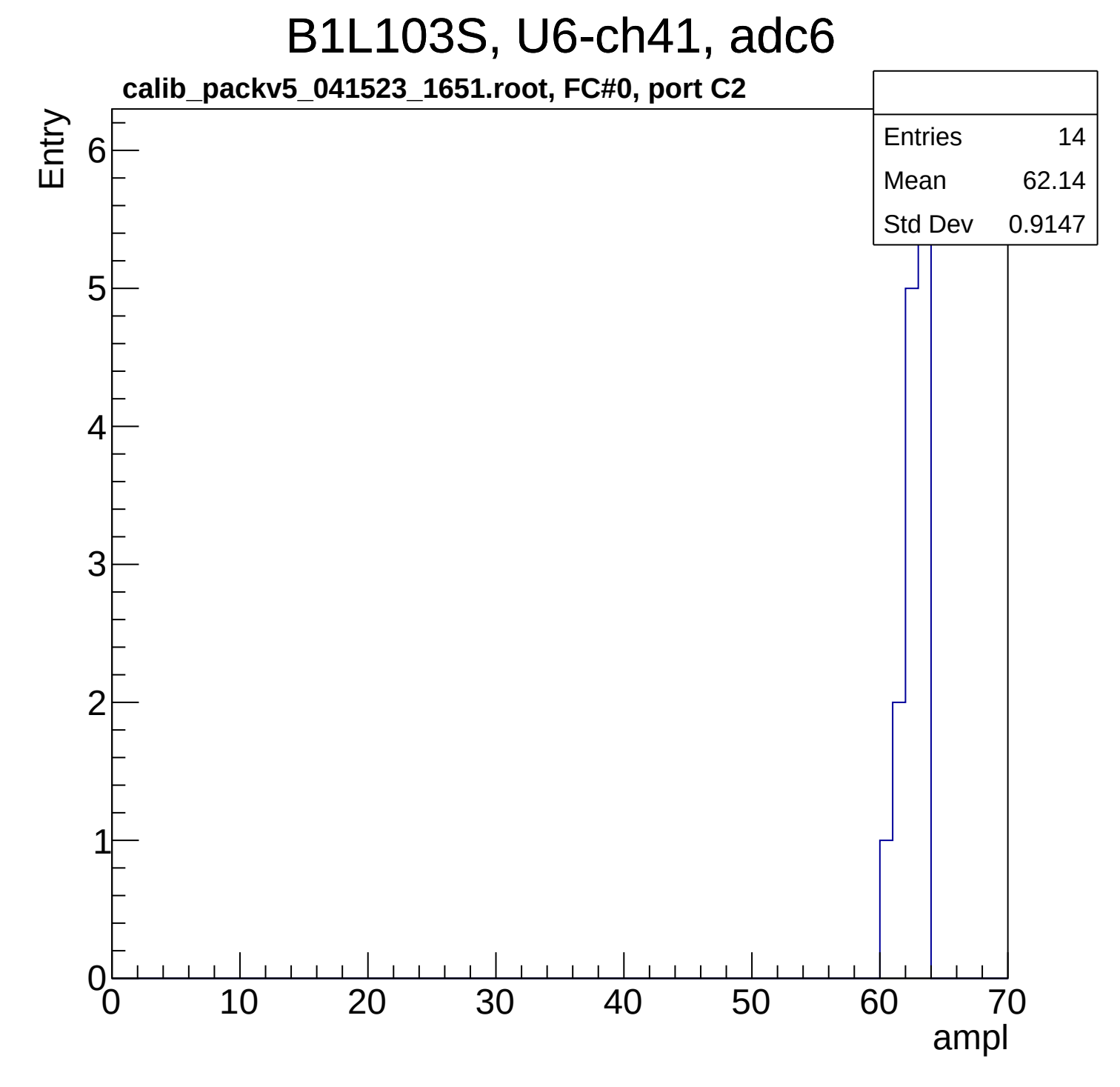
40
50
60
70


B1L103S, U6-ch41, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 62.14
Std Dev 0.9147
Entry
ampl
0
1
2
3
4
5
6
0
10
20
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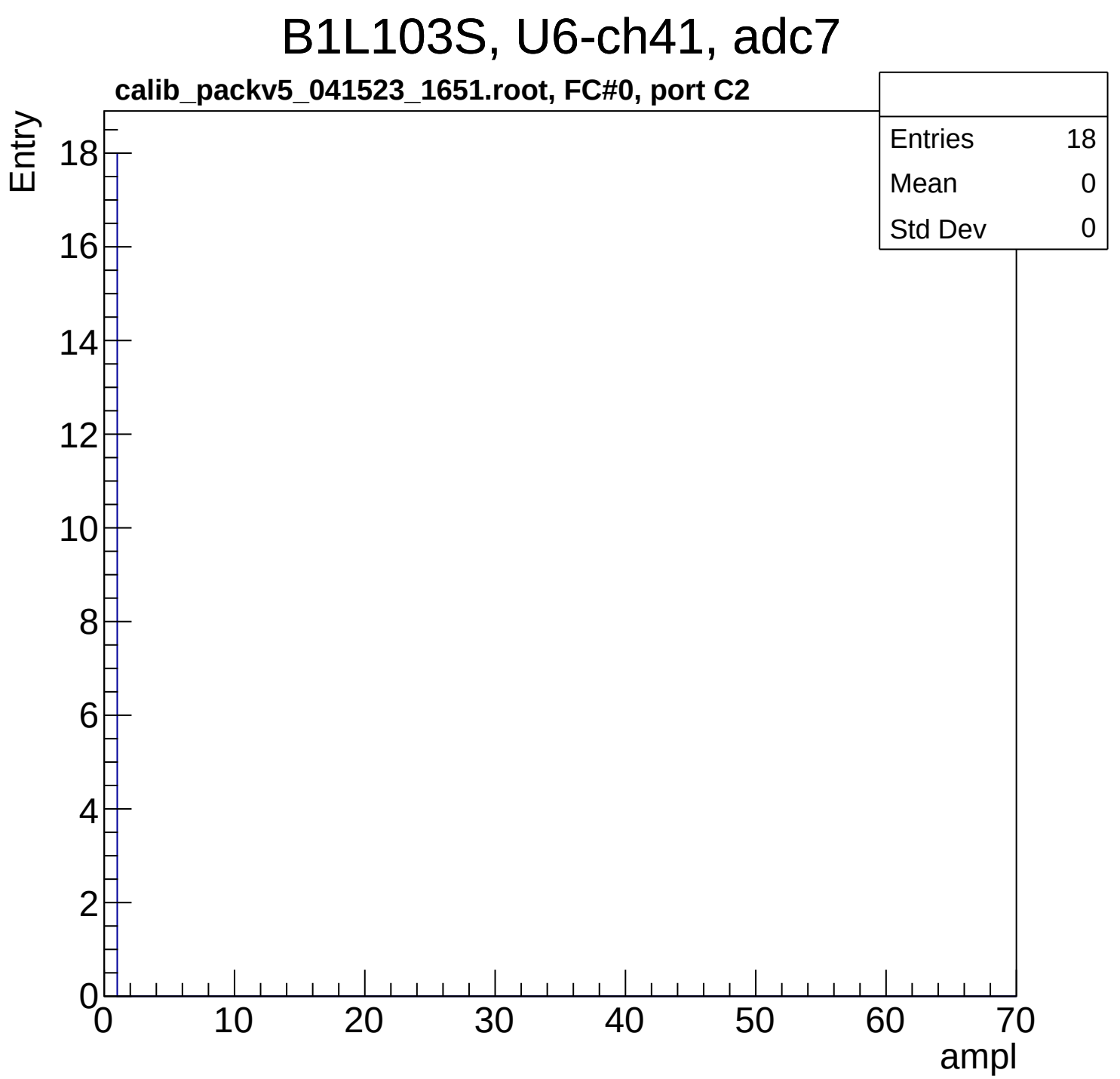
40
50
60
70


B1L103S, U6-ch41, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
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6
8
10
12
14
16
18
0
10
20
30
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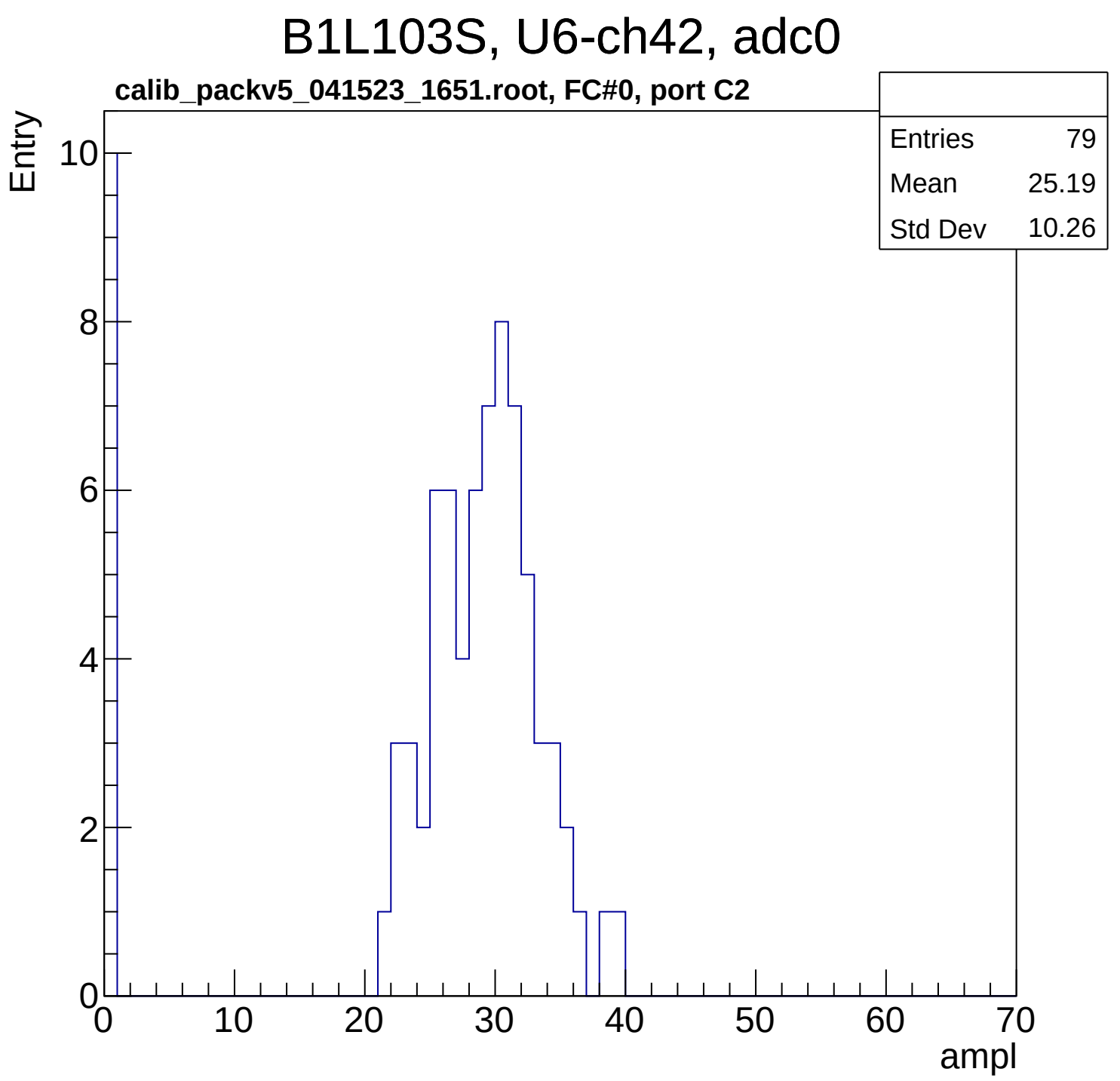
50
60
70
ampl


B1L103S, U6-ch42, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 25.19
Std Dev 10.26
Entry
0
2
4
6
8
10
0
10
20
30
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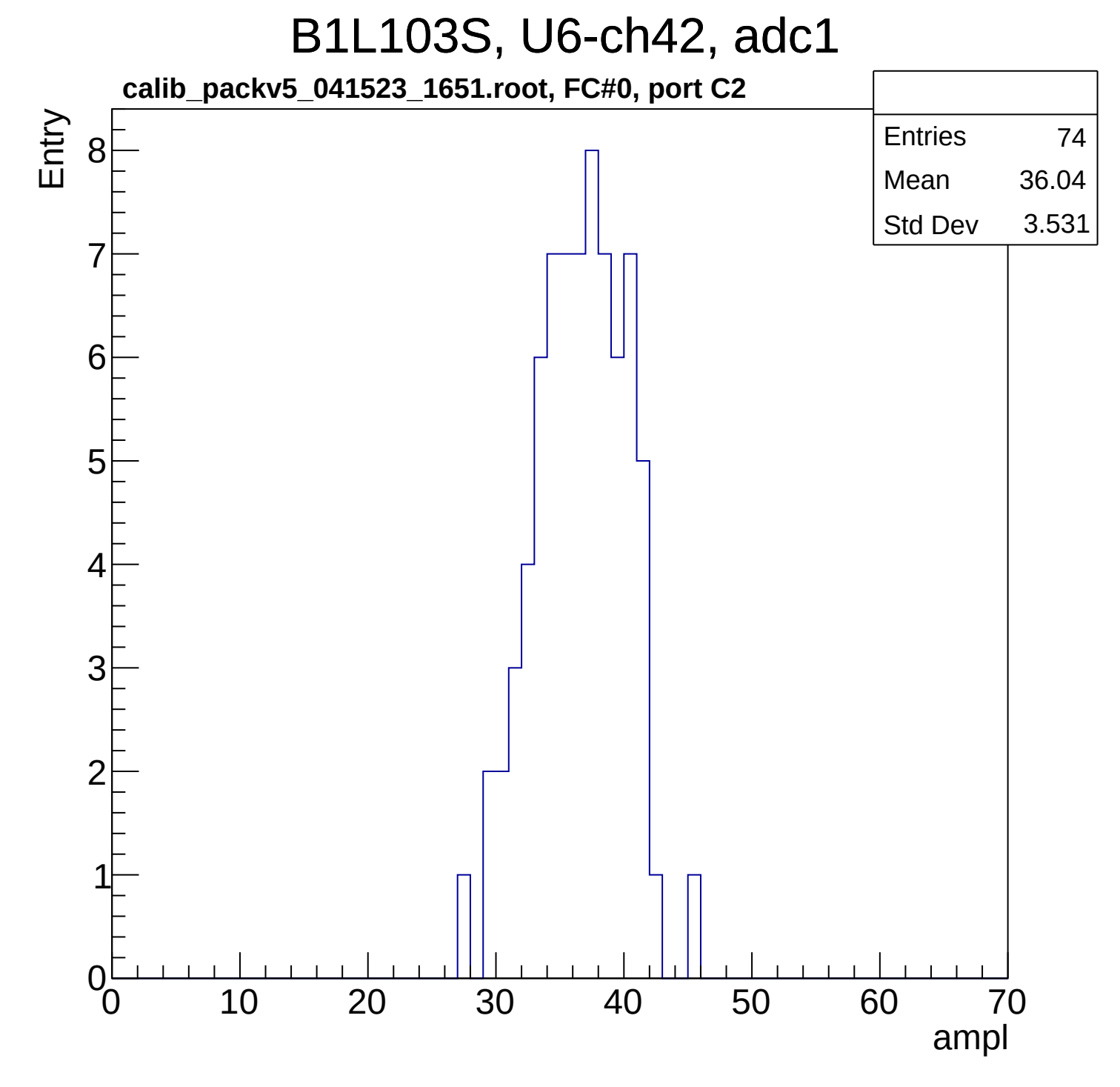
50
60
70
ampl


B1L103S, U6-ch42, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 36.04
Std Dev 3.531
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
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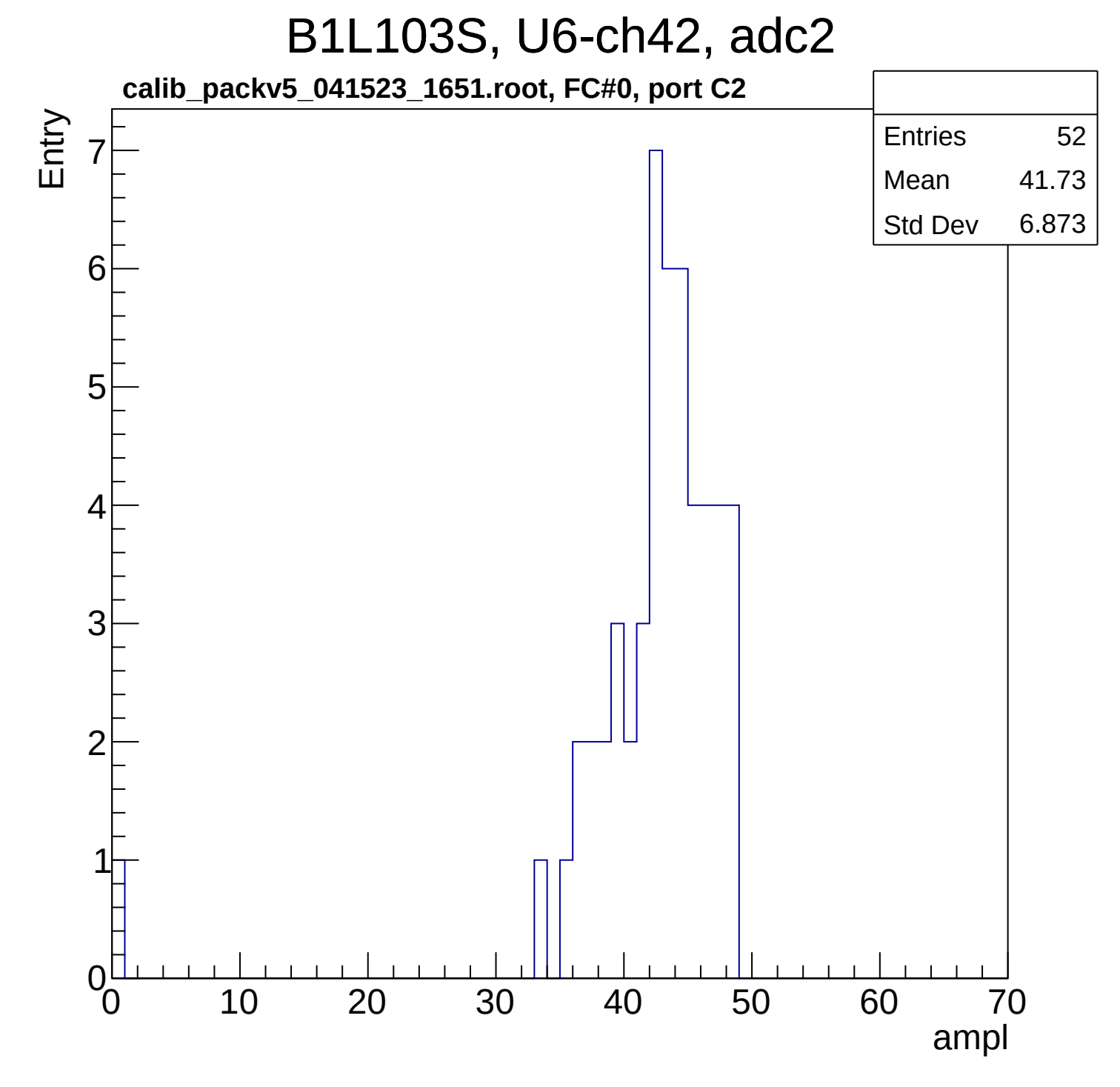
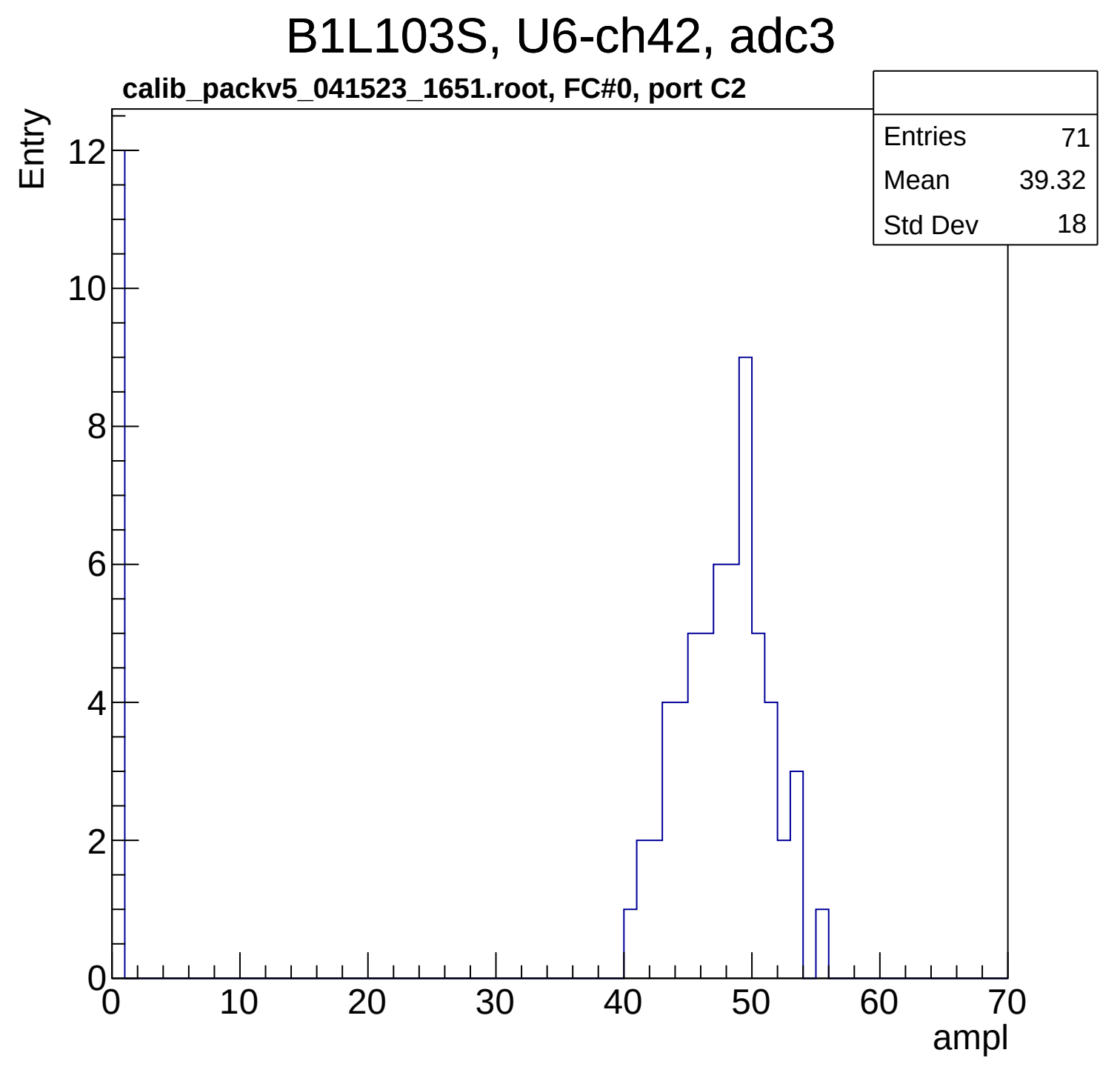
60
70


B1L103S, U6-ch42, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 41.73
Std Dev 6.873
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U6-ch42, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 39.32
Std Dev 18
Entry
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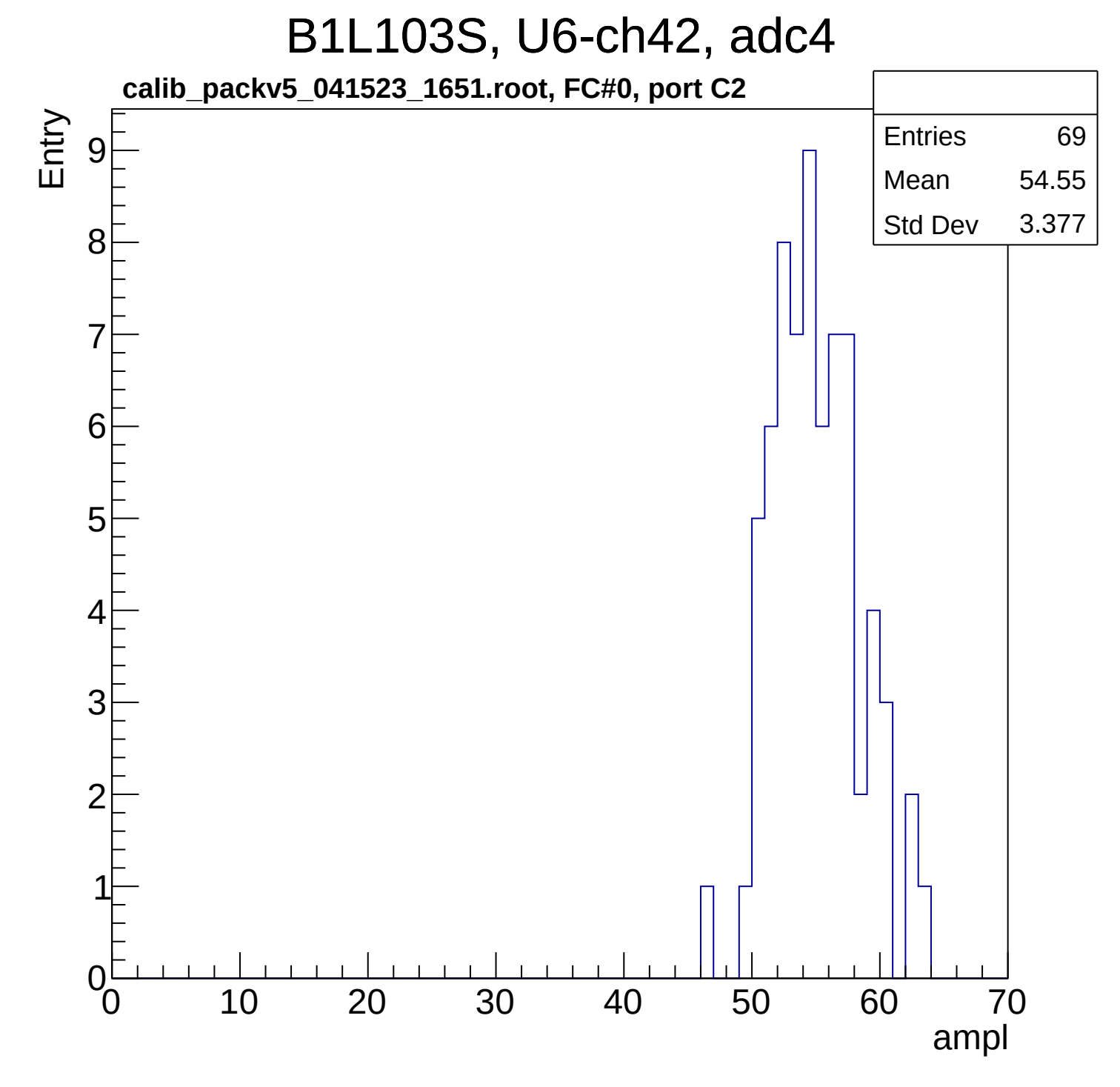
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch42, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 54.55
Std Dev 3.377
Entry
ampl
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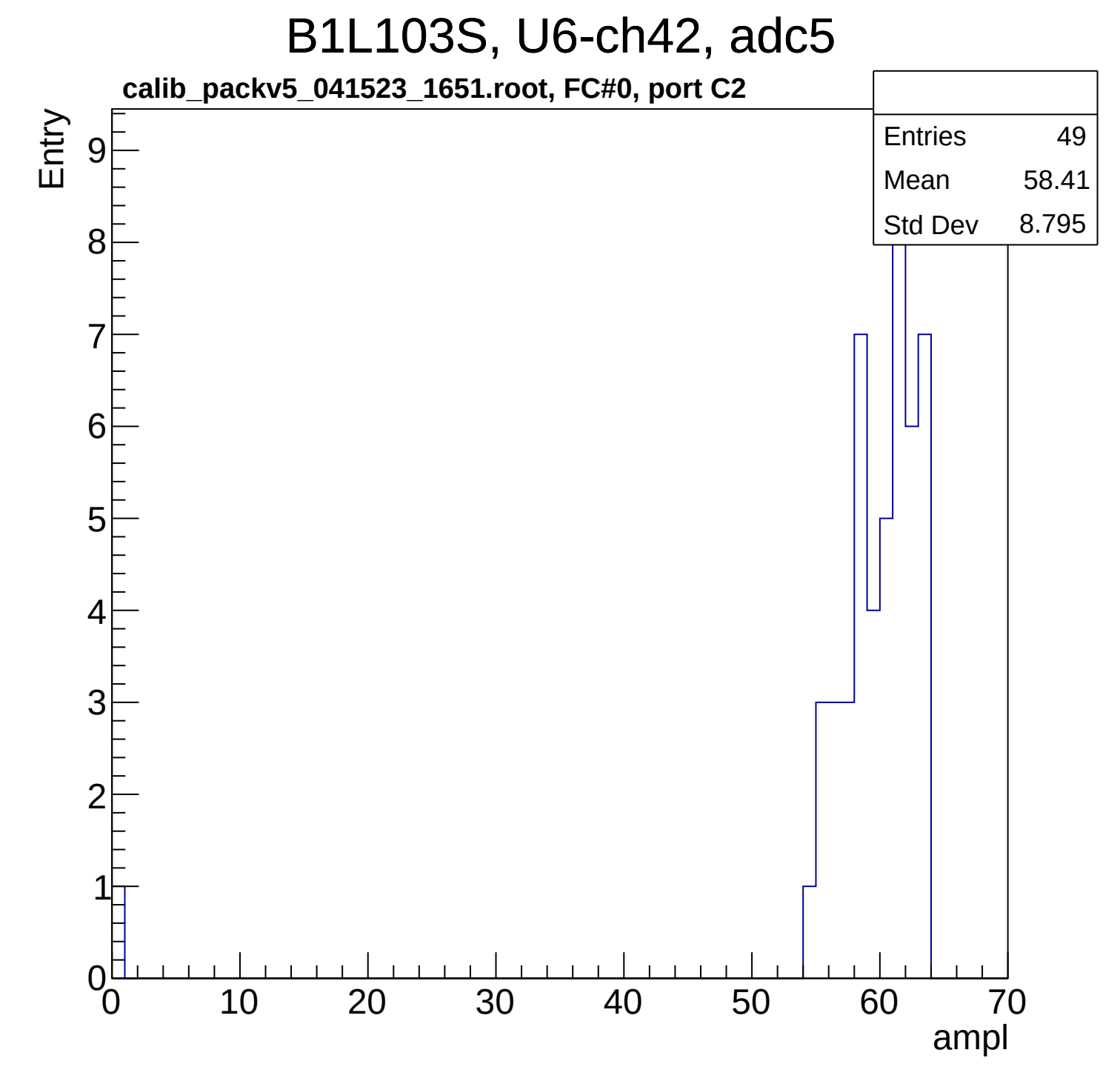
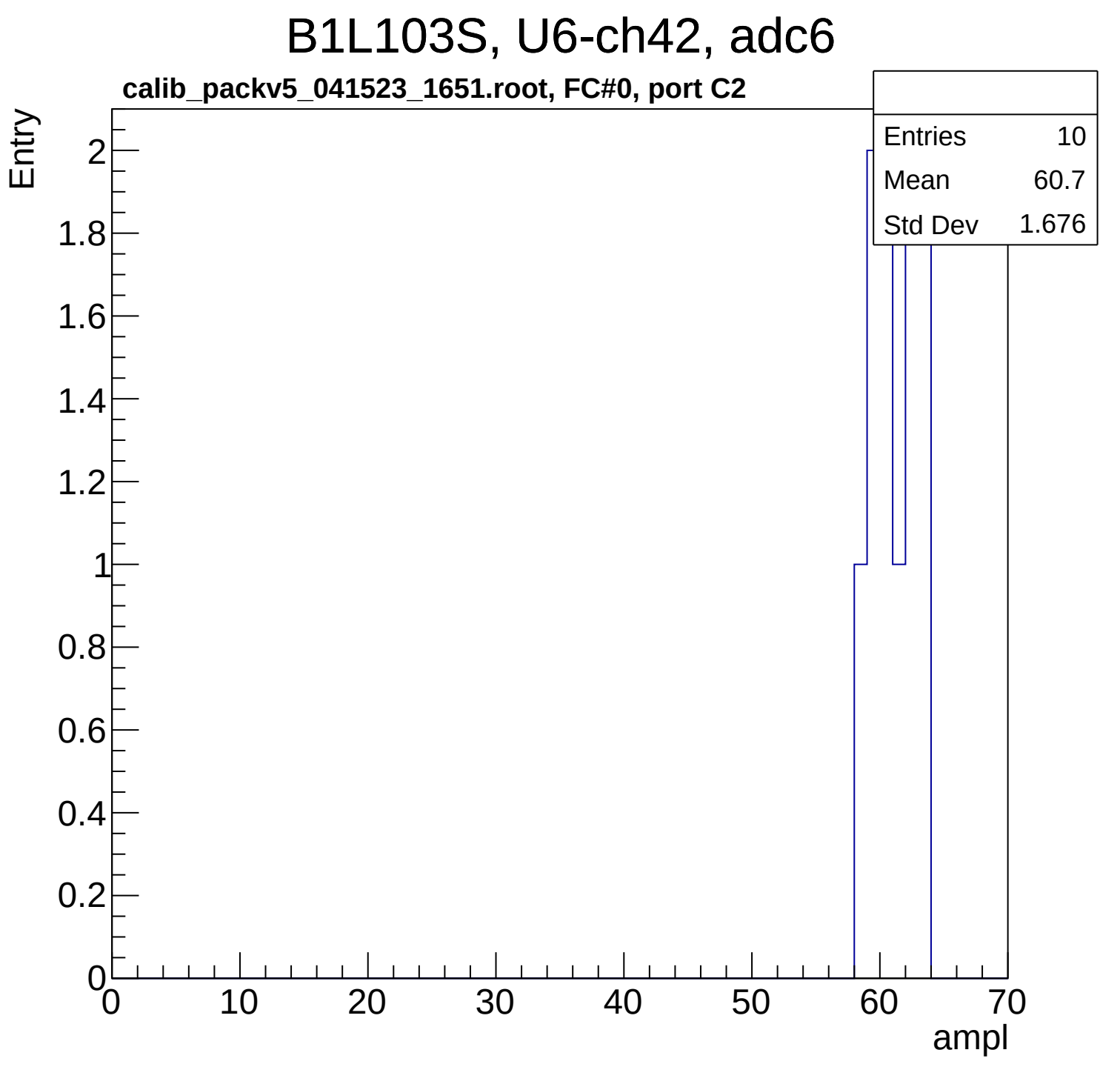
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch42, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 58.41
Std Dev 8.795
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch42, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 60.7
Std Dev 1.676
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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60
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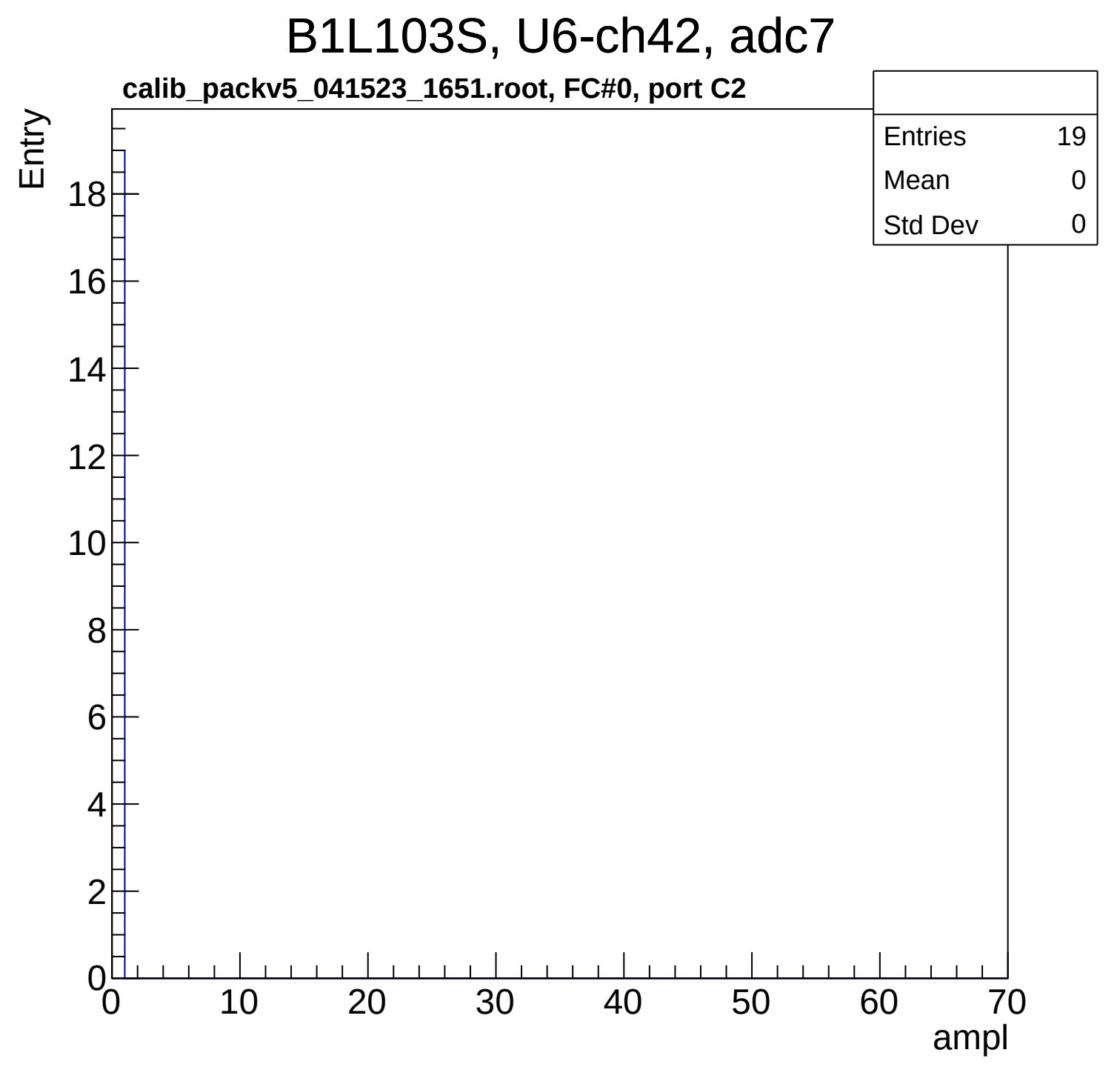
B1L103S, U6-ch42, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
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10
20
30
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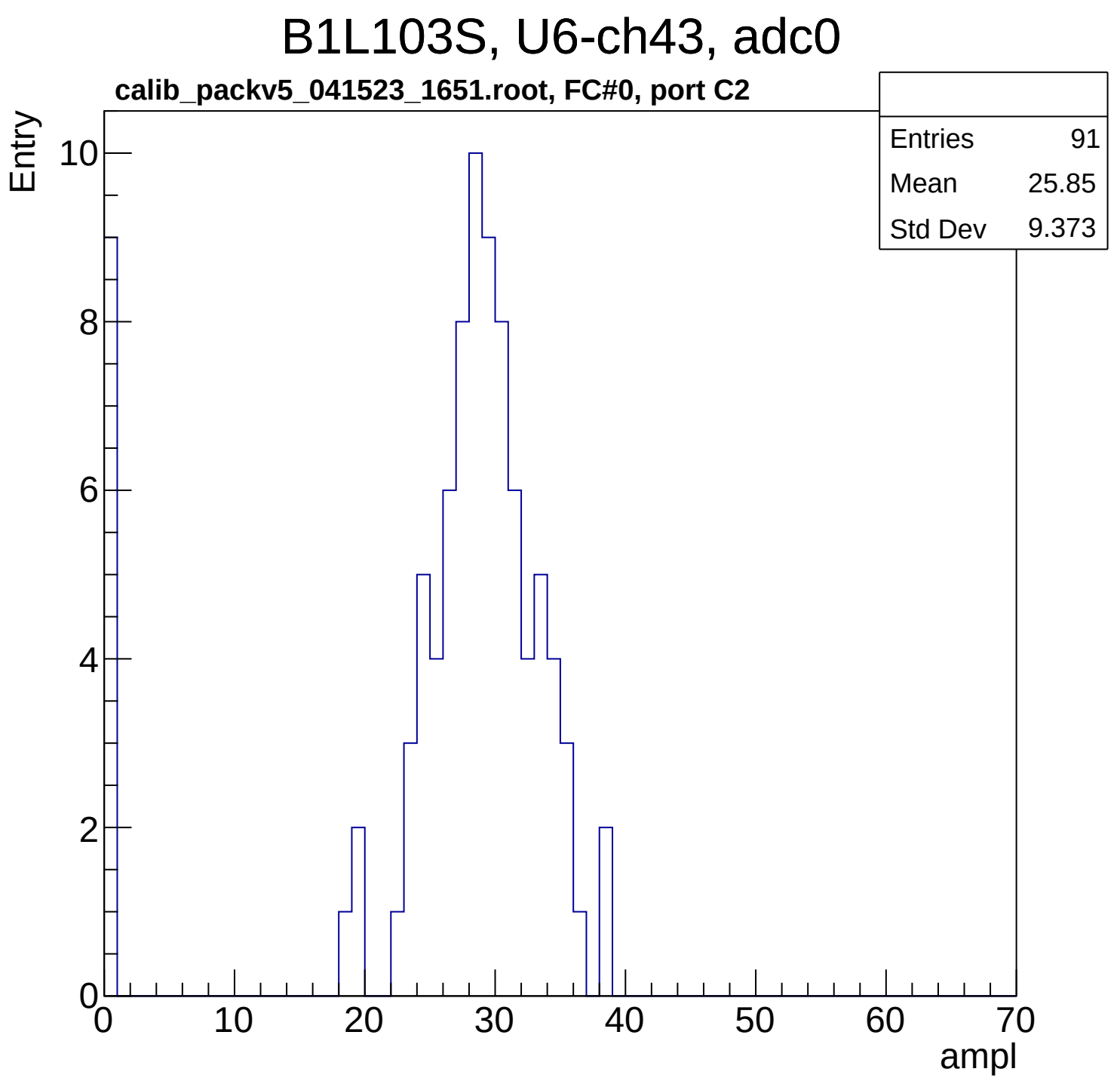
50
60
70
ampl


B1L103S, U6-ch43, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 25.85
Std Dev 9.373
Entry
0
2
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6
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10
0
10
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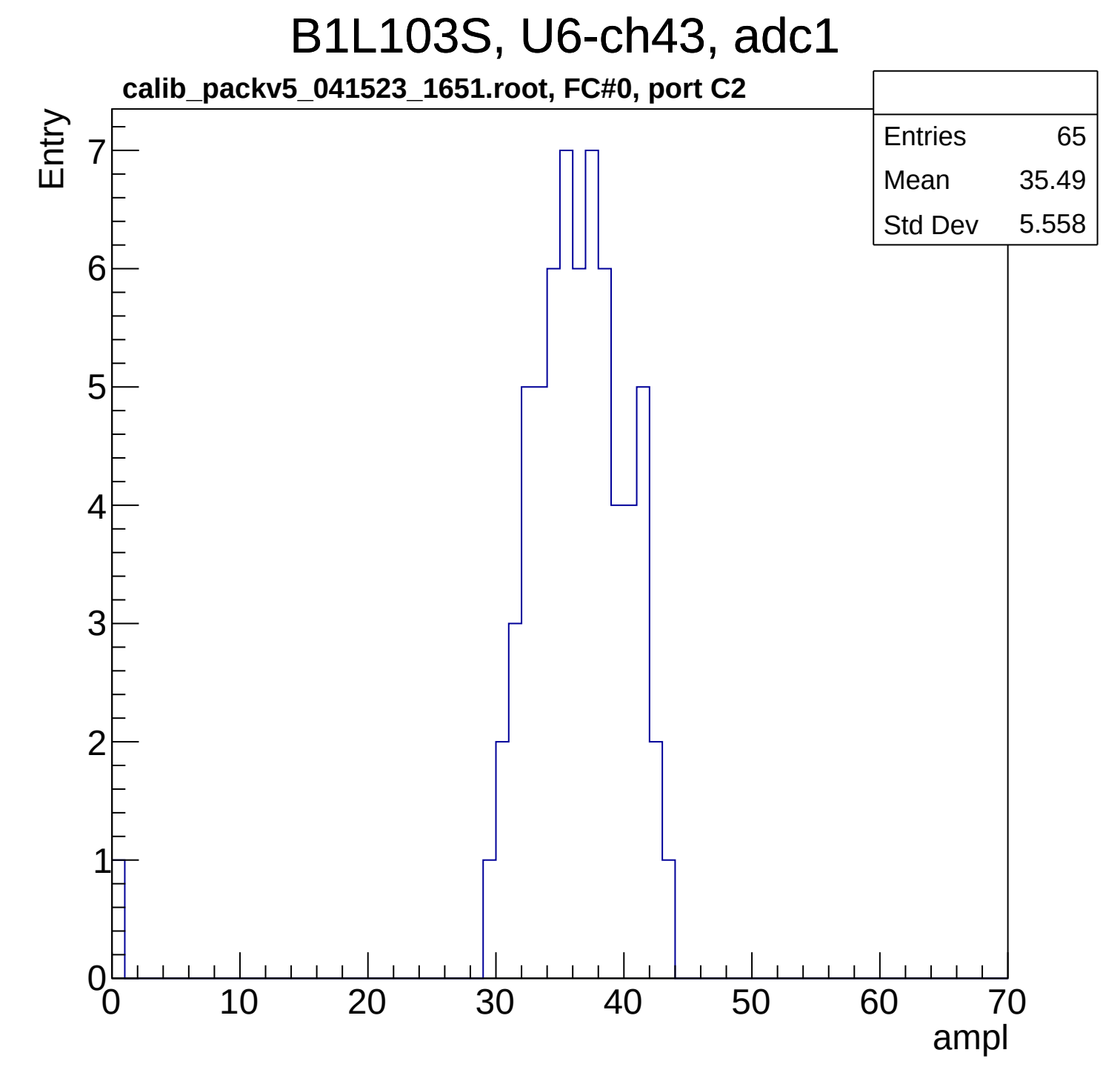
50
60
70
ampl


B1L103S, U6-ch43, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 35.49
Std Dev 5.558
Entry
ampl
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1
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4
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0
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40
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60
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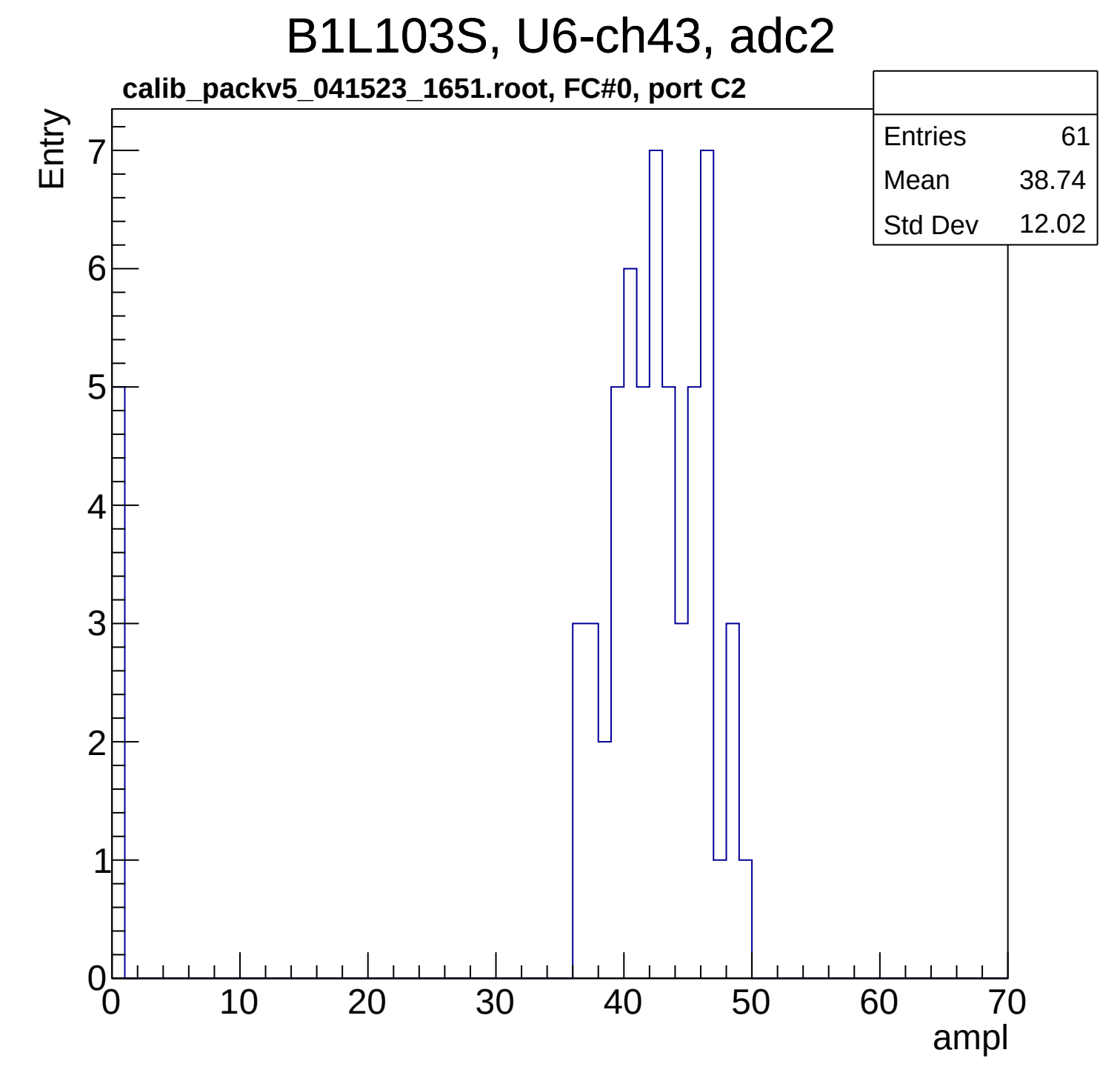
B1L103S, U6-ch43, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 38.74
Std Dev 12.02
Entry
ampl
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2
3
4
5
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0
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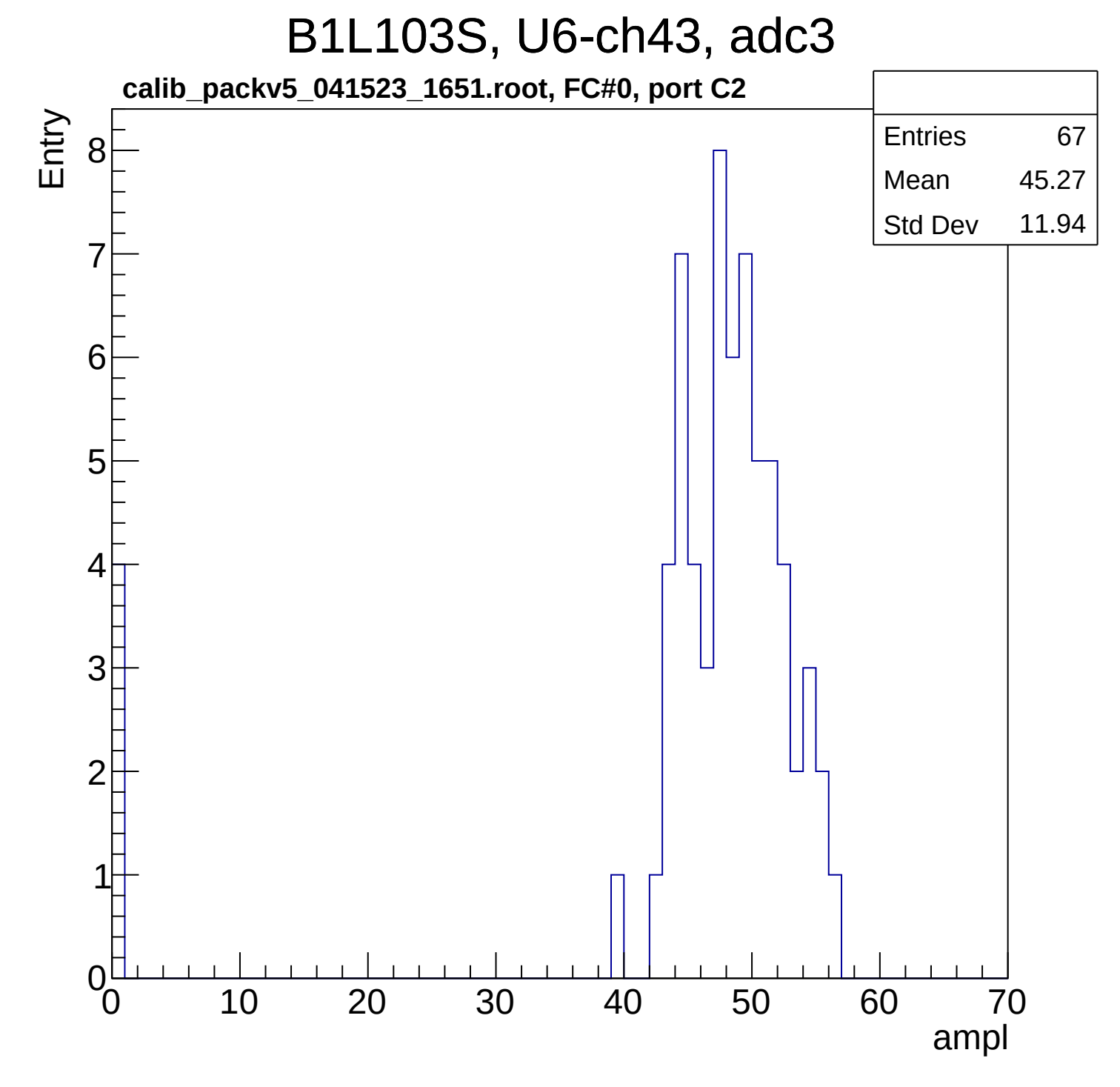
B1L103S, U6-ch43, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 45.27
Std Dev 11.94
Entry
ampl
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2
3
4
5
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7
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0
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40
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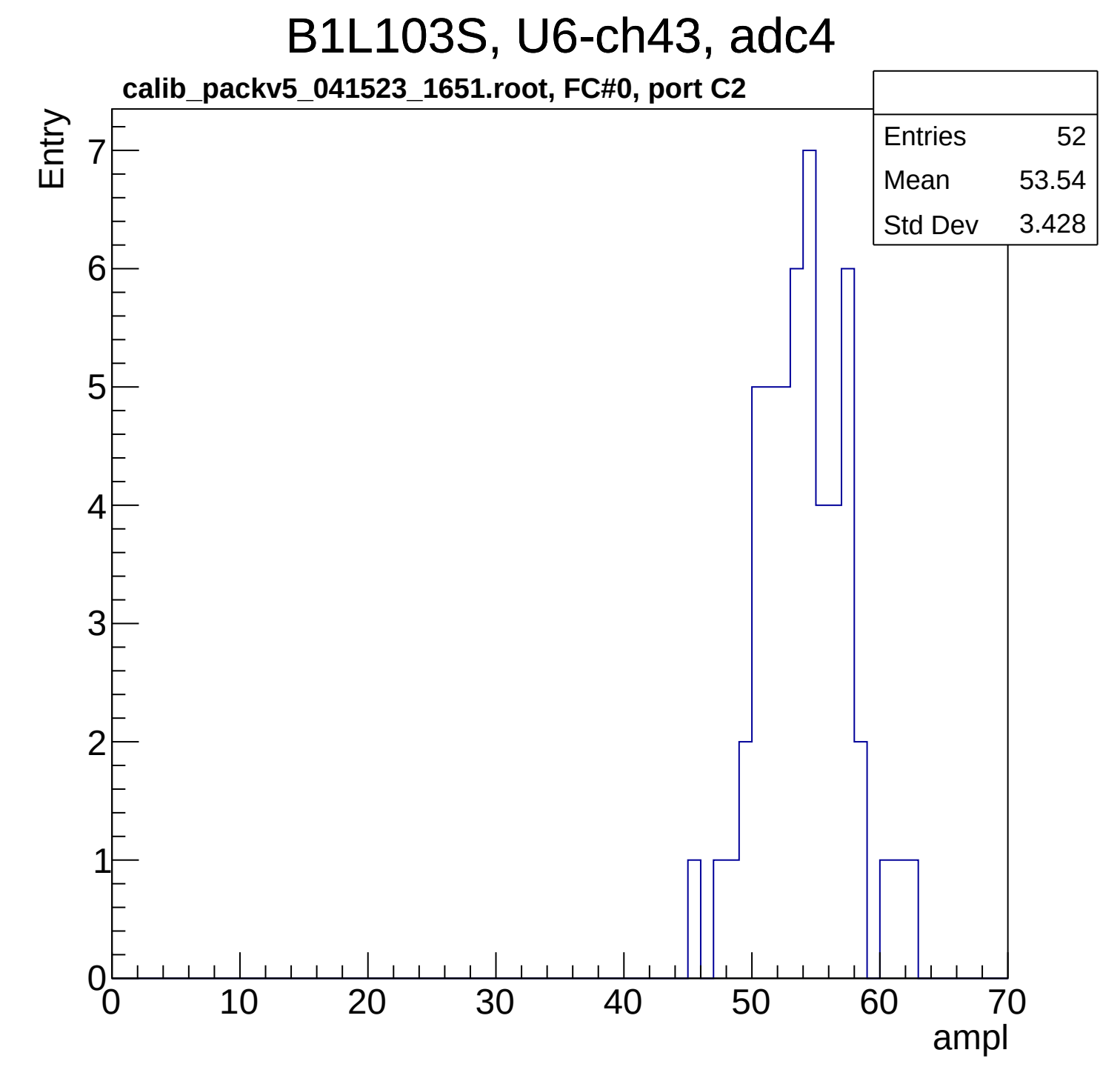
B1L103S, U6-ch43, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 53.54
Std Dev 3.428
Entry
ampl
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2
3
4
5
6
7
0
10
20
30
40
50
60
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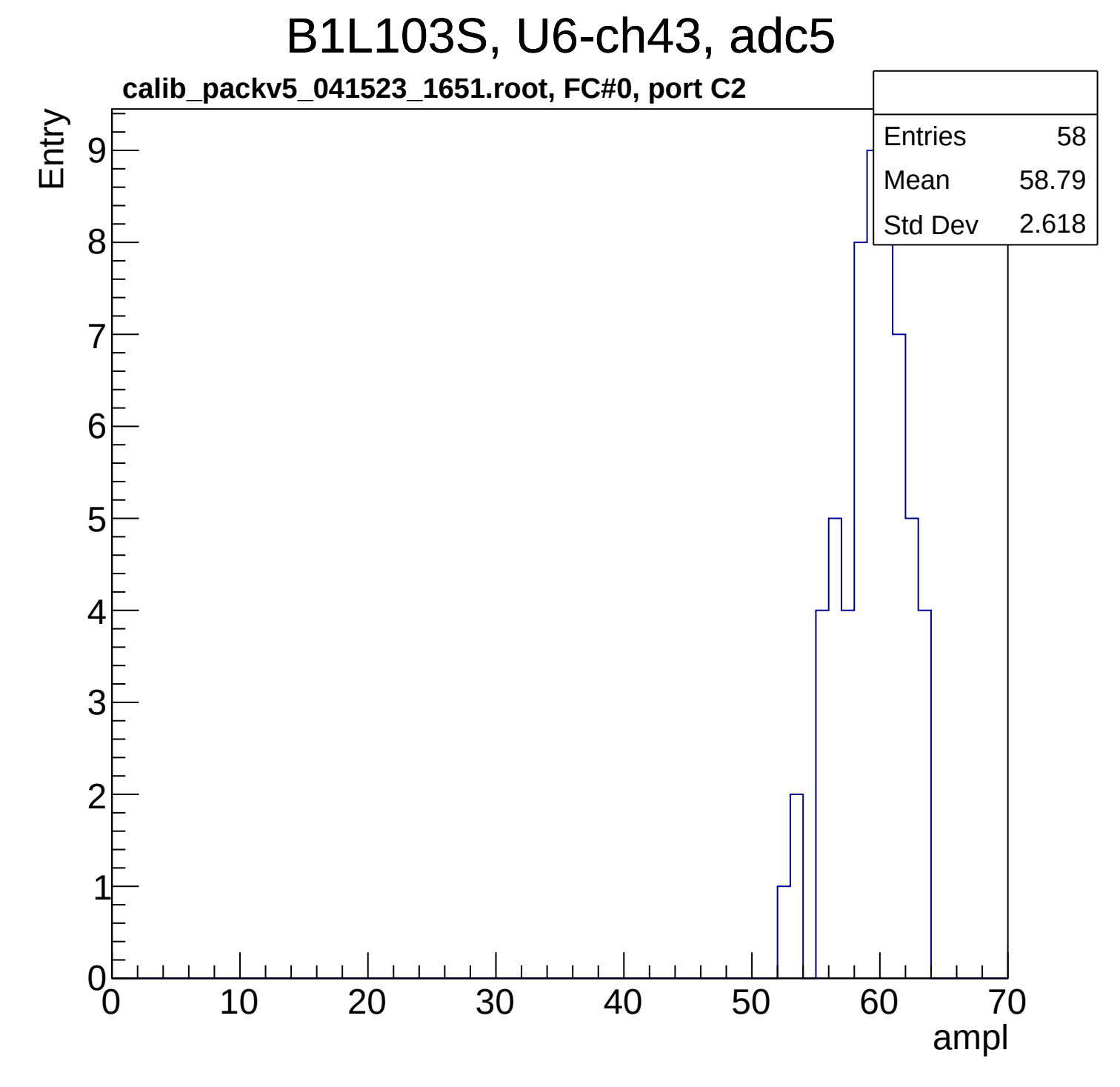
B1L103S, U6-ch43, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 58.79
Std Dev 2.618
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
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60
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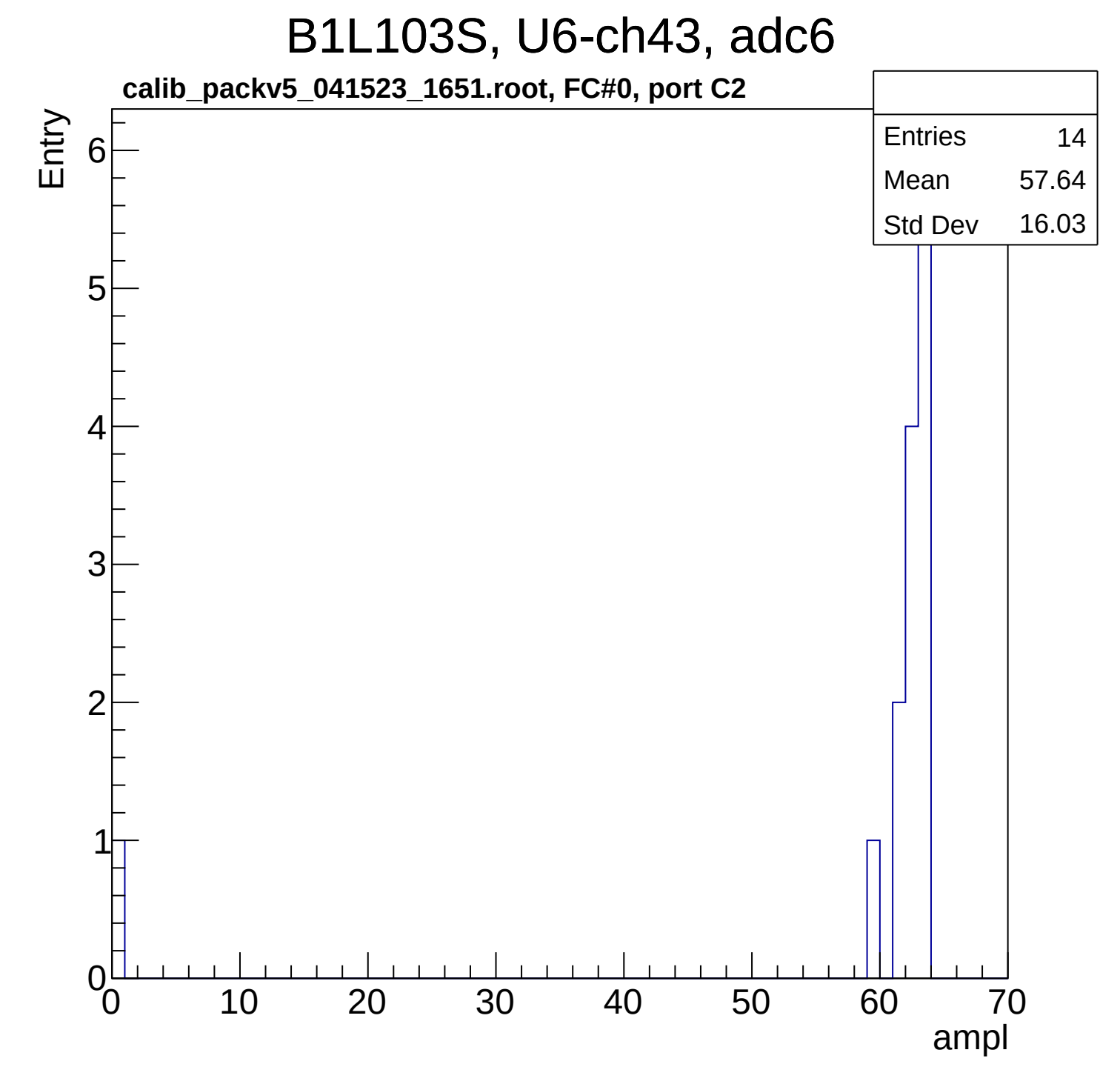
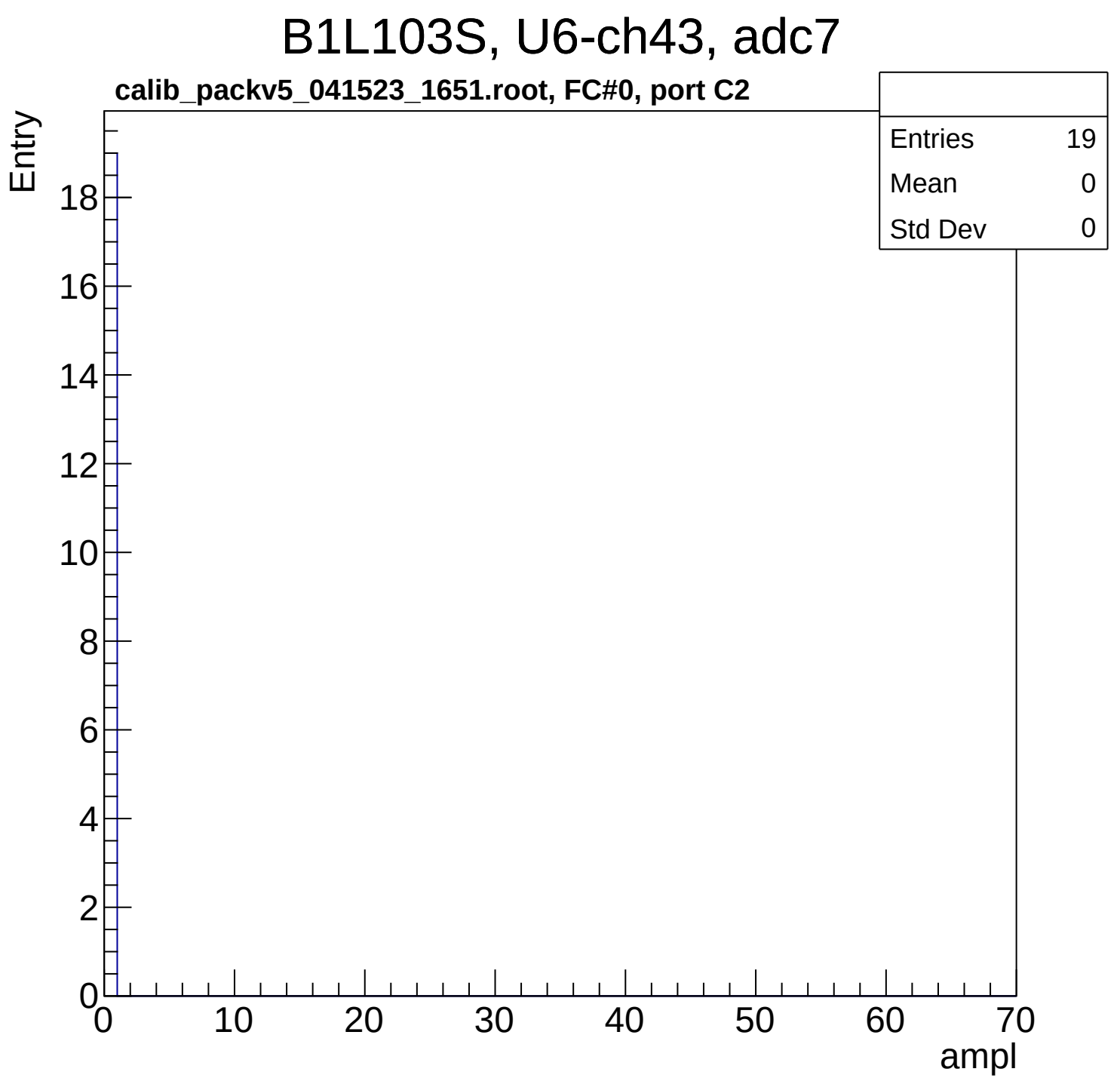
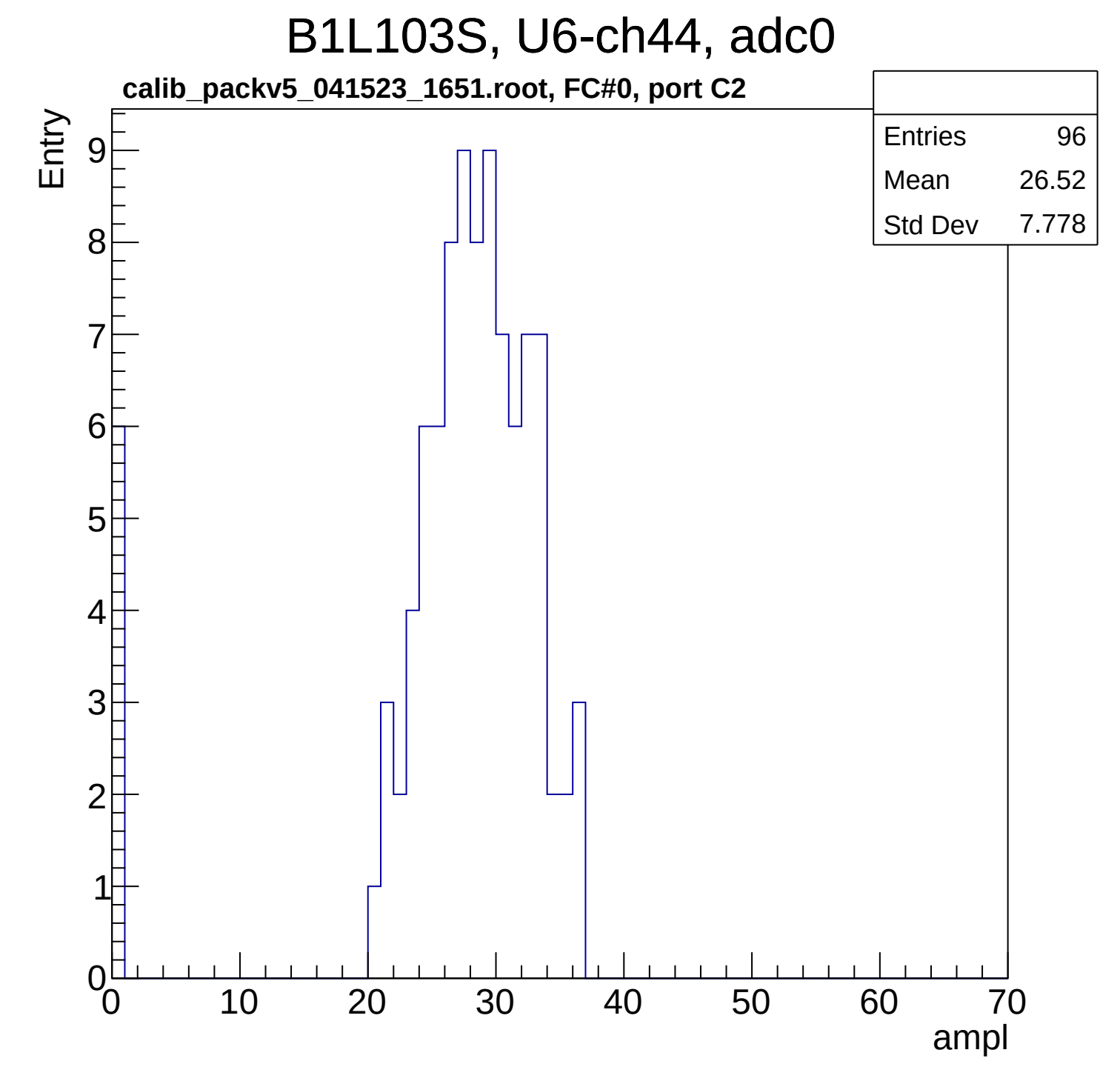

B1L103S, U6-ch43, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 57.64
Std Dev 16.03
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch43, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch44, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 96
Mean 26.52
Std Dev 7.778
Entry
ampl
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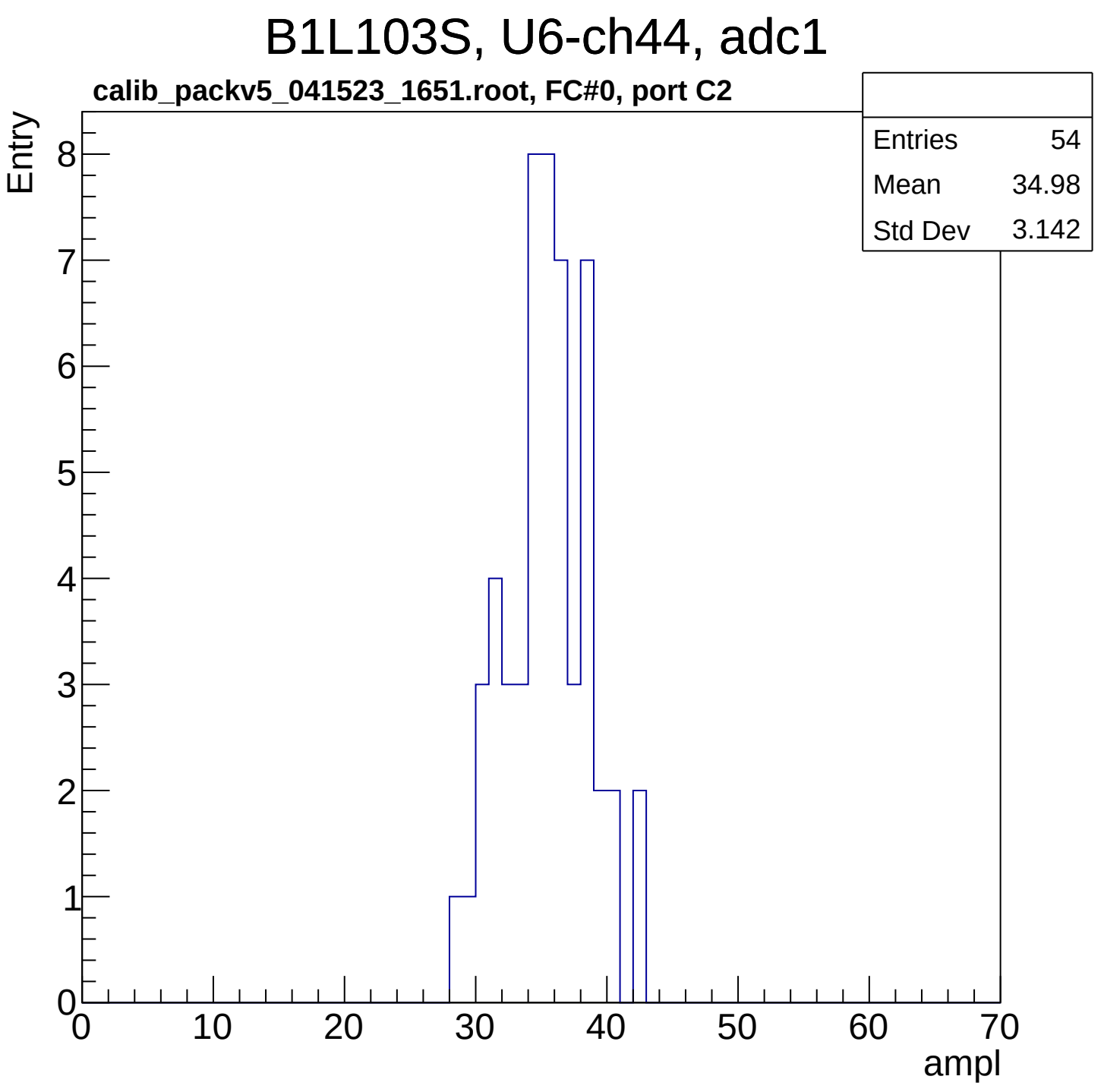
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch44, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 34.98
Std Dev 3.142
Entry
ampl
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2
3
4
5
6
7
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0
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40
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60
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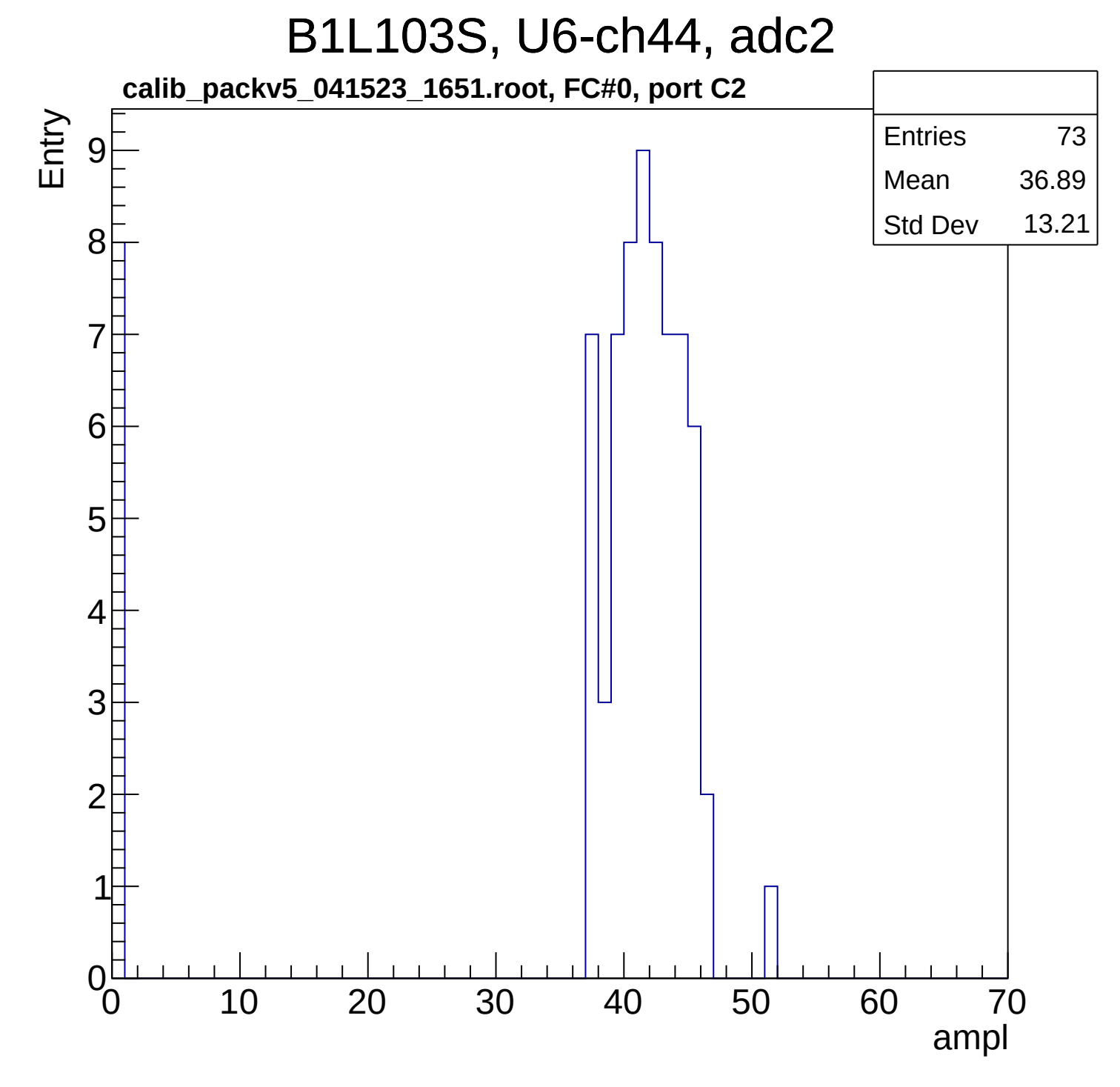
B1L103S, U6-ch44, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 36.89
Std Dev 13.21
Entry
ampl
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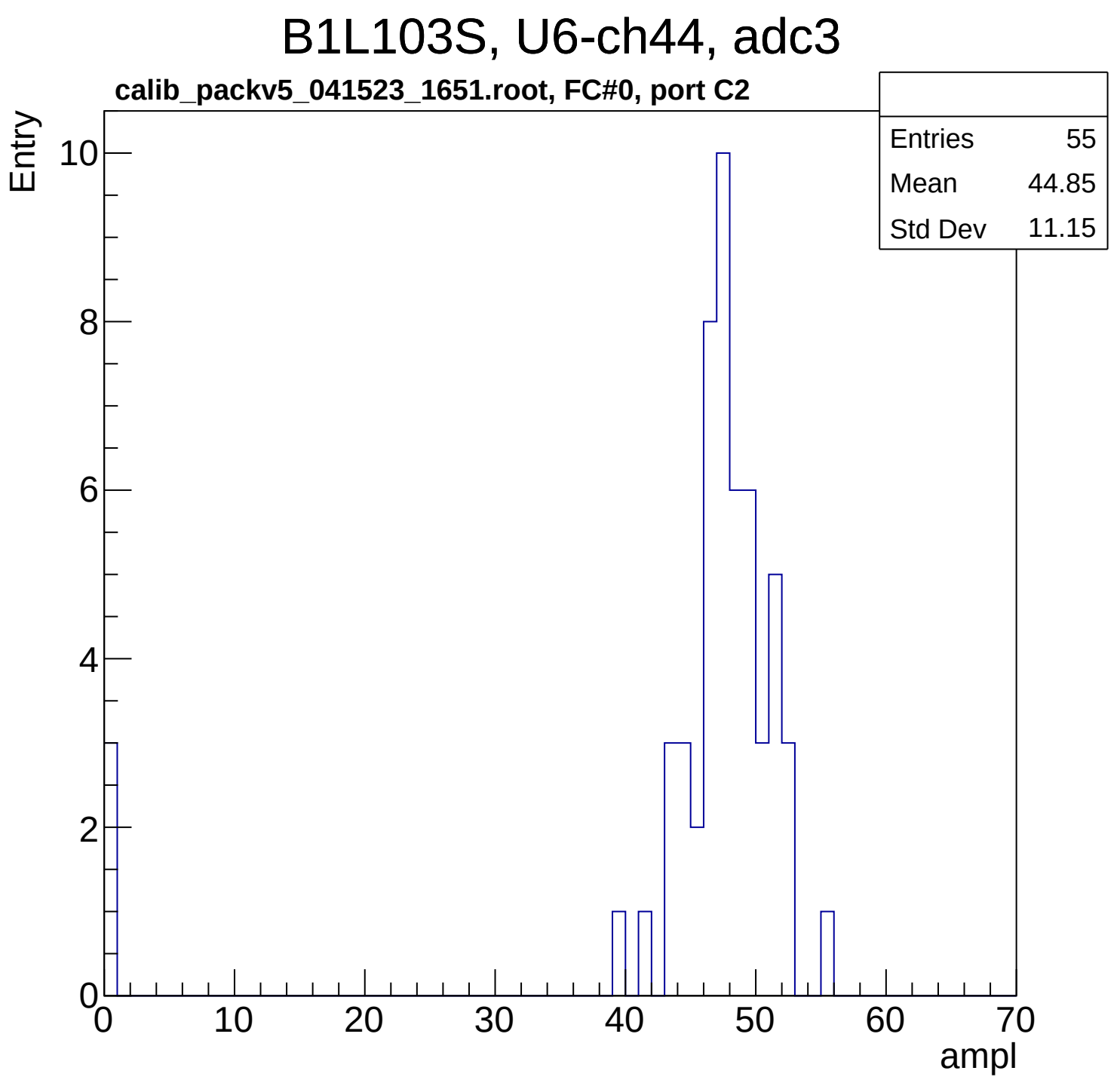
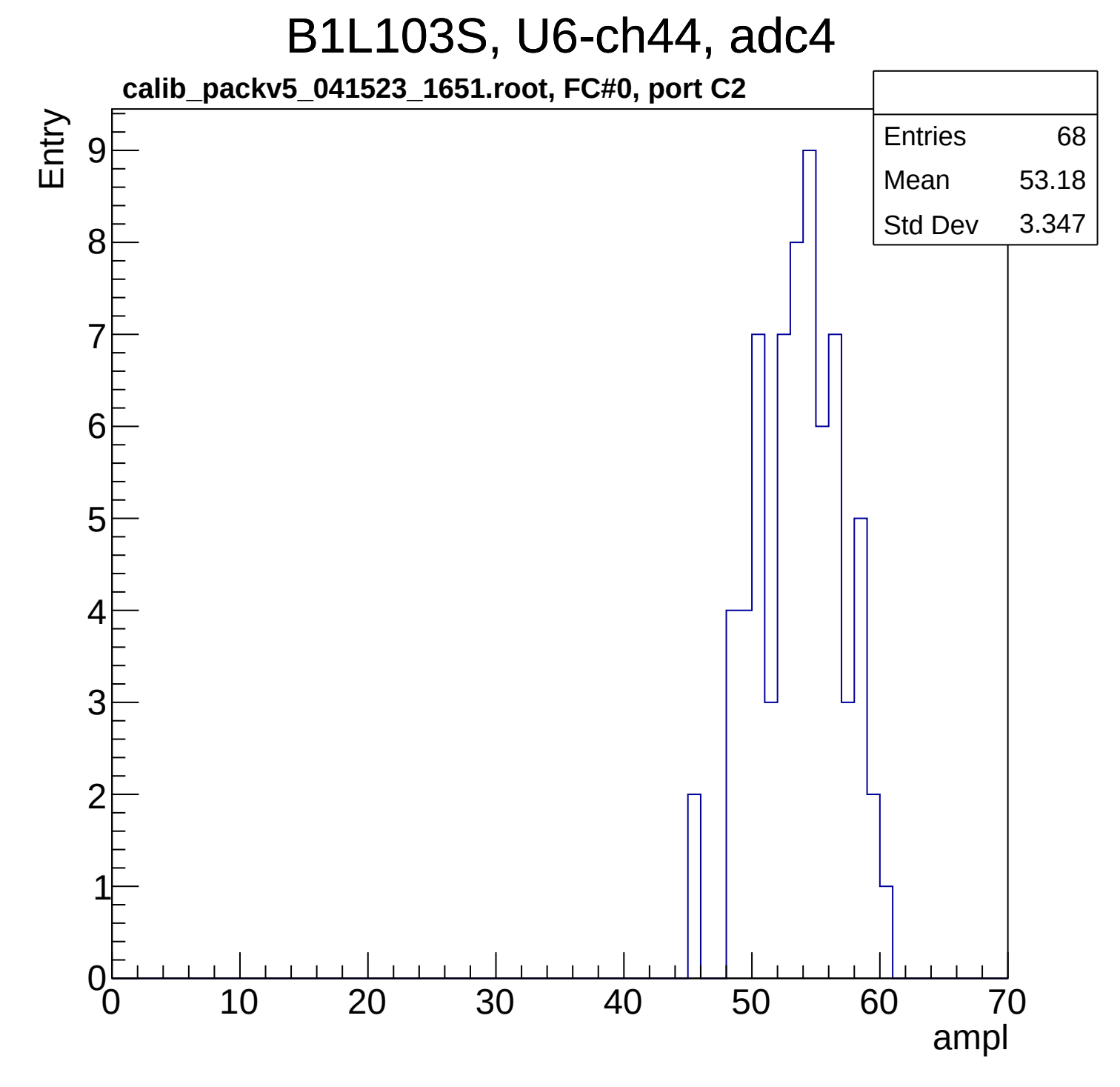
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch44, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 44.85
Std Dev 11.15
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch44, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 53.18
Std Dev 3.347
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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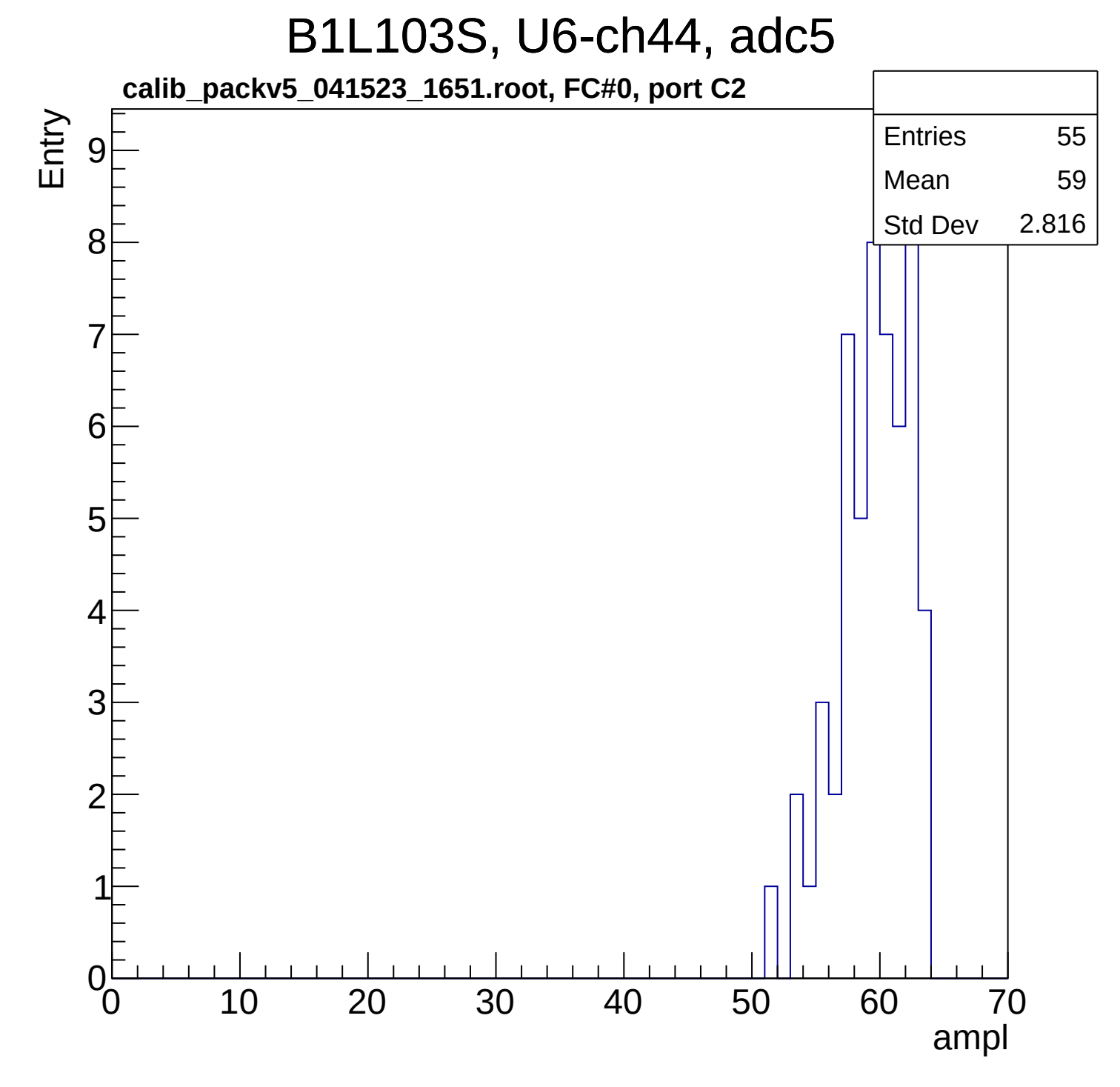
B1L103S, U6-ch44, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 59
Std Dev 2.816
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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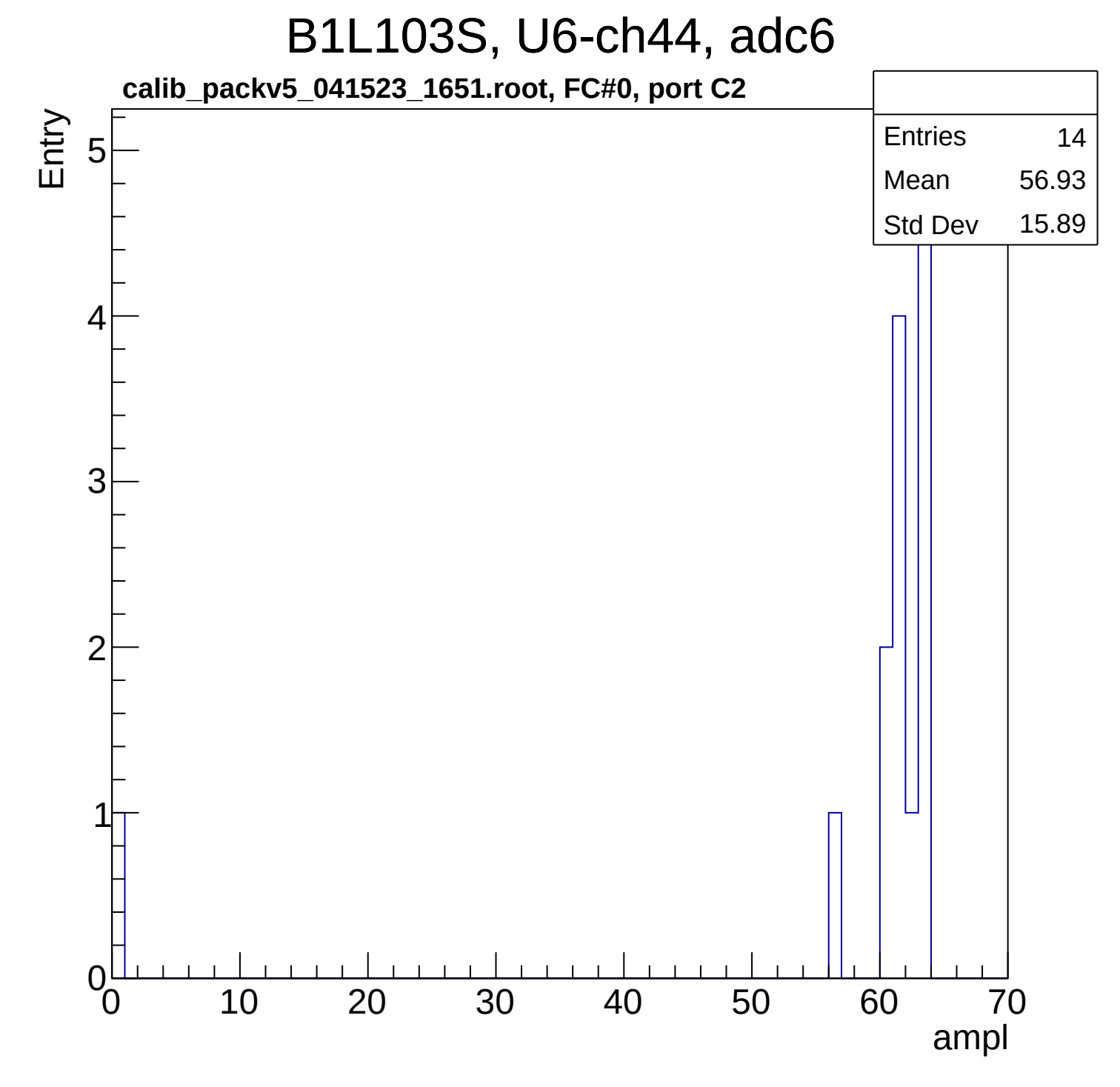
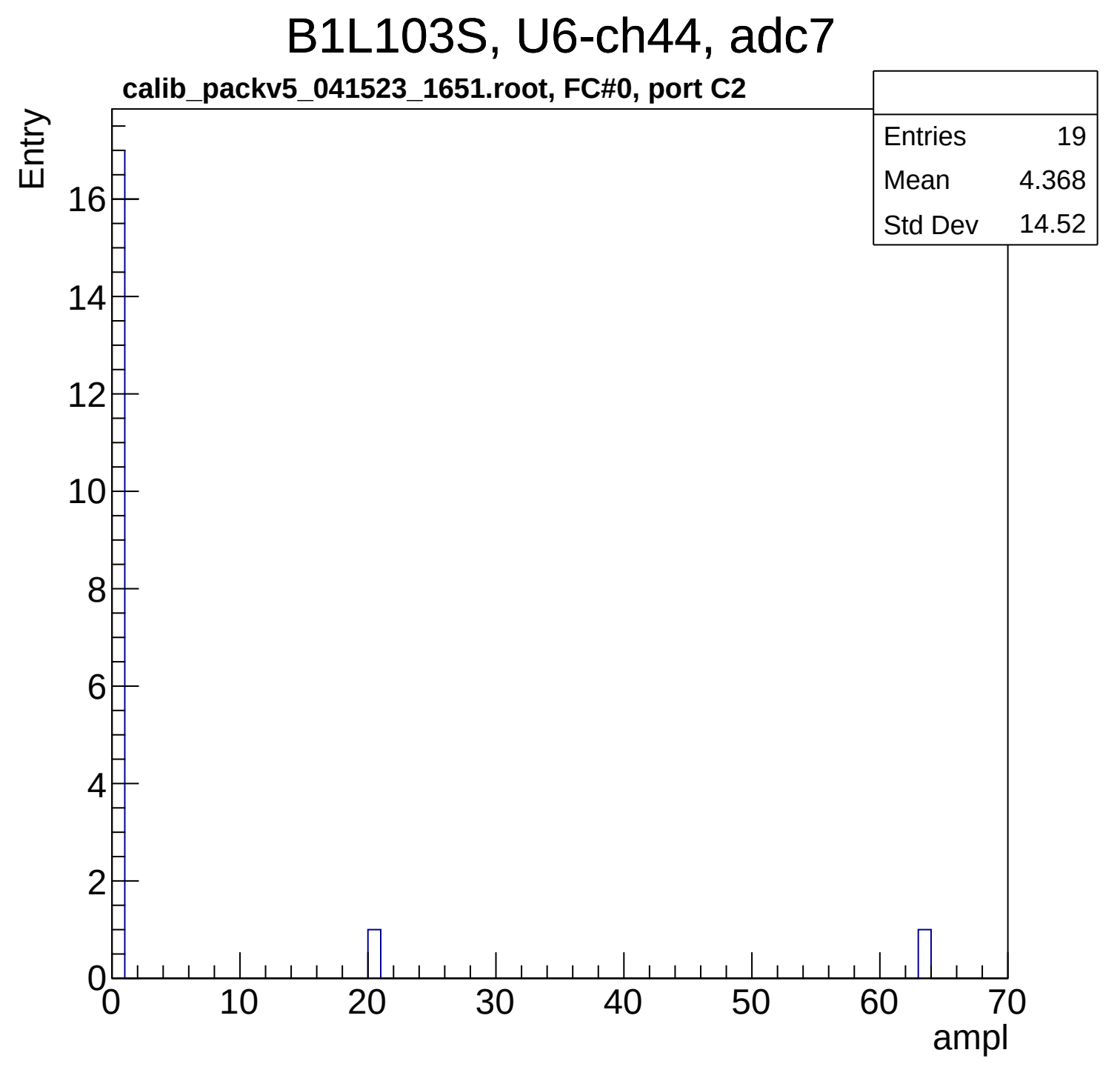

B1L103S, U6-ch44, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 56.93
Std Dev 15.89
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch44, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 4.368
Std Dev 14.52
Entry
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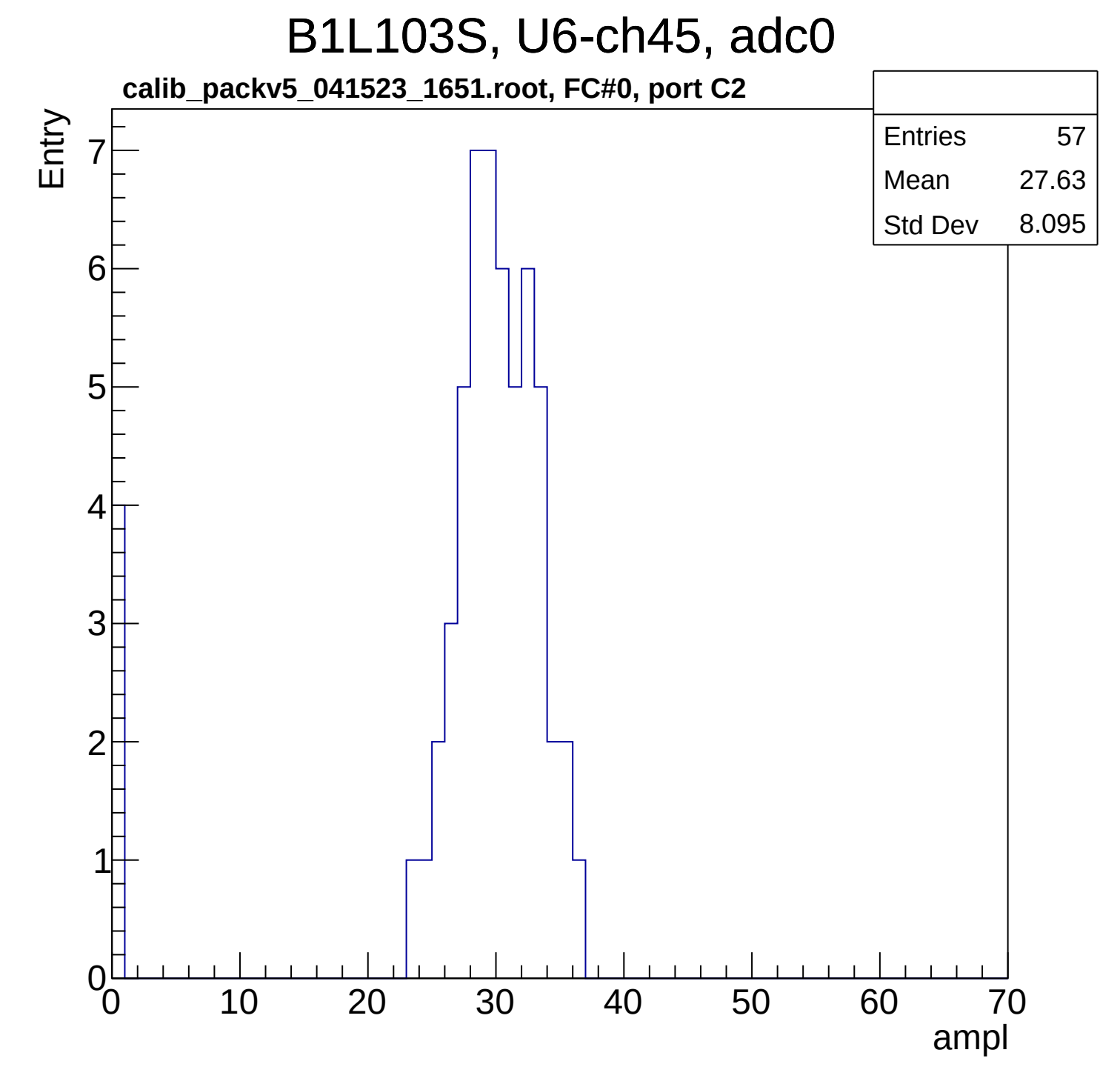
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch45, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 27.63
Std Dev 8.095
Entry
ampl
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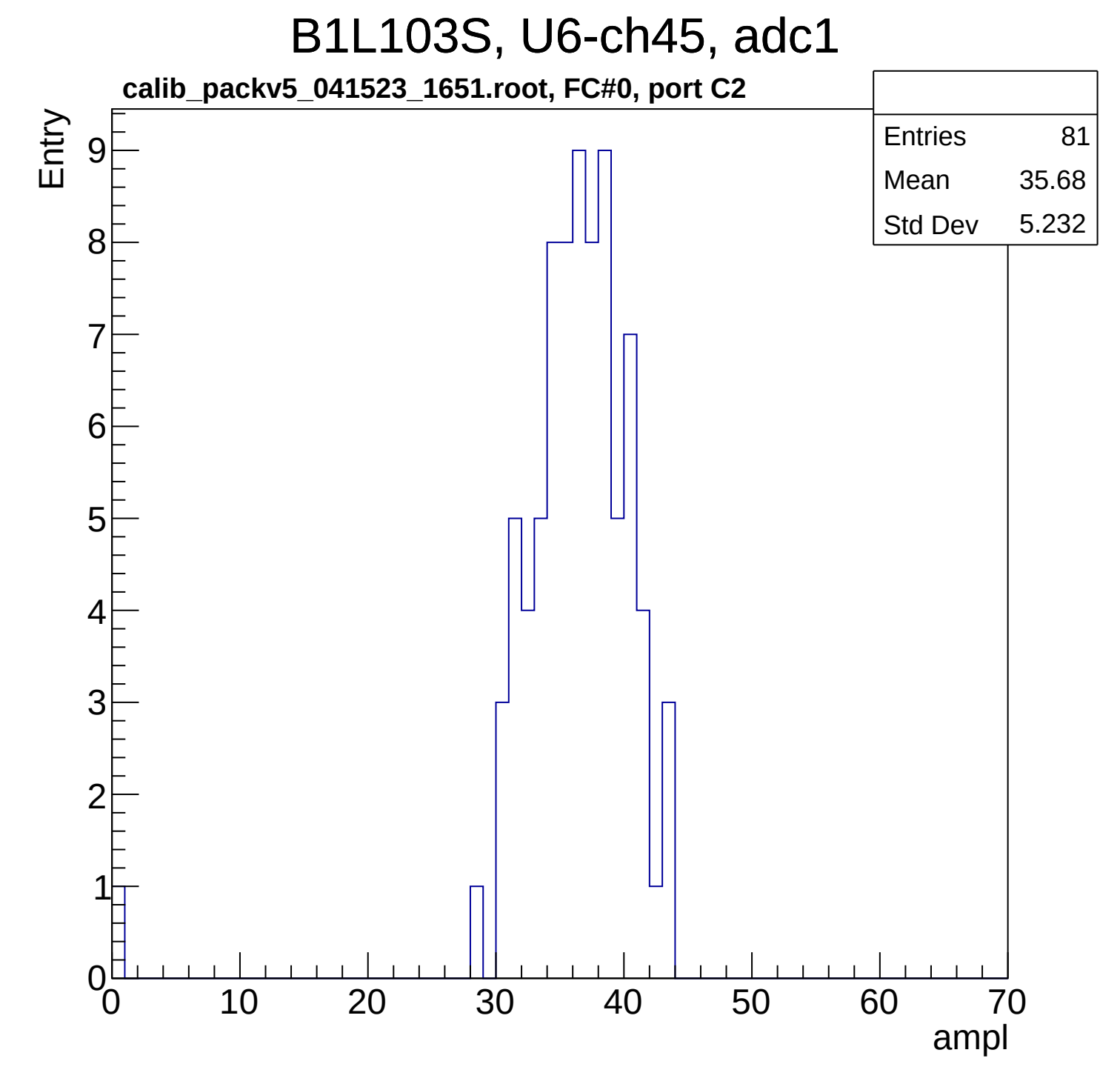
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U6-ch45, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 35.68
Std Dev 5.232
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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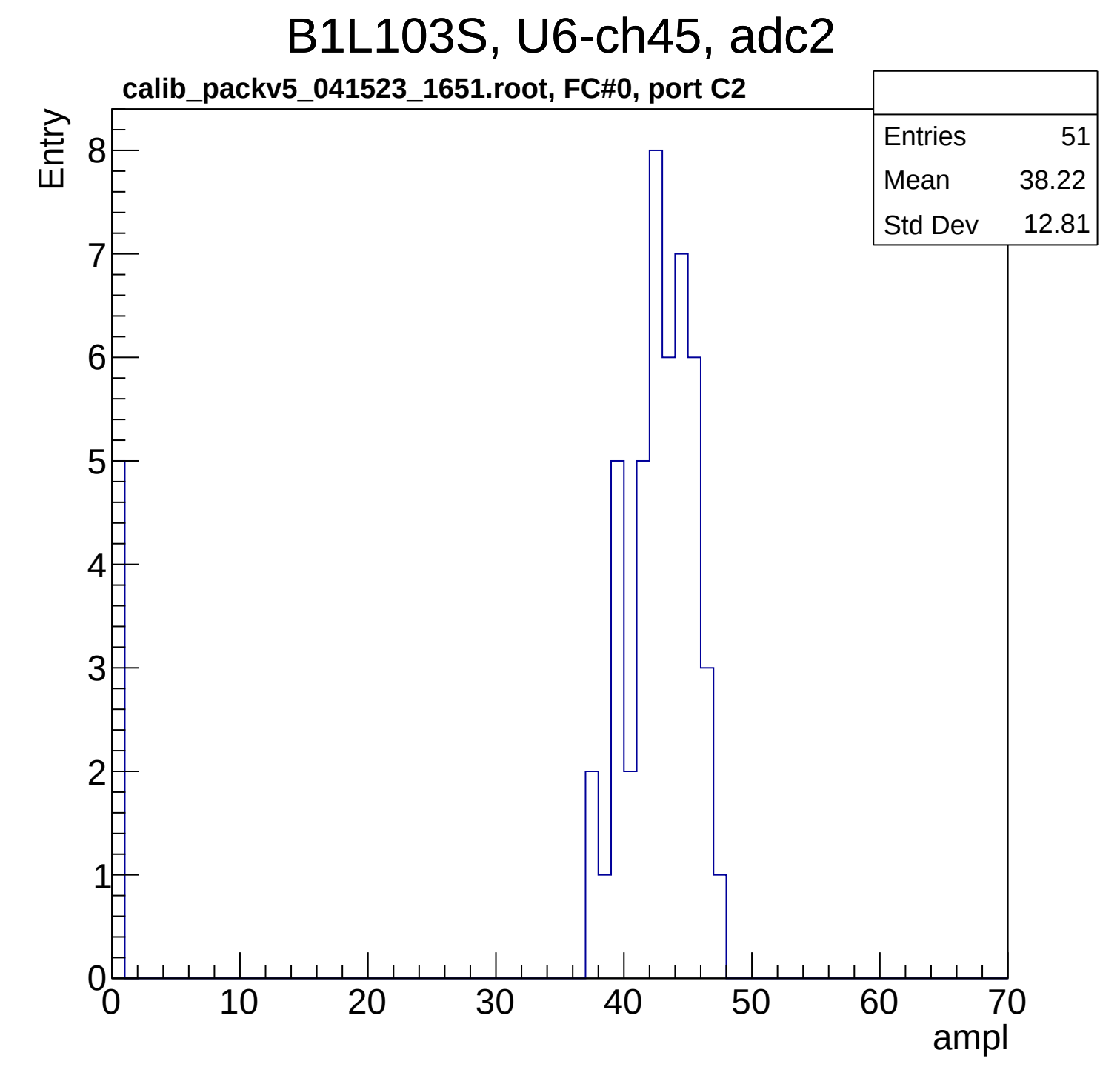
60
70


B1L103S, U6-ch45, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 38.22
Std Dev 12.81
Entry
ampl
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1
2
3
4
5
6
7
8
0
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40
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60
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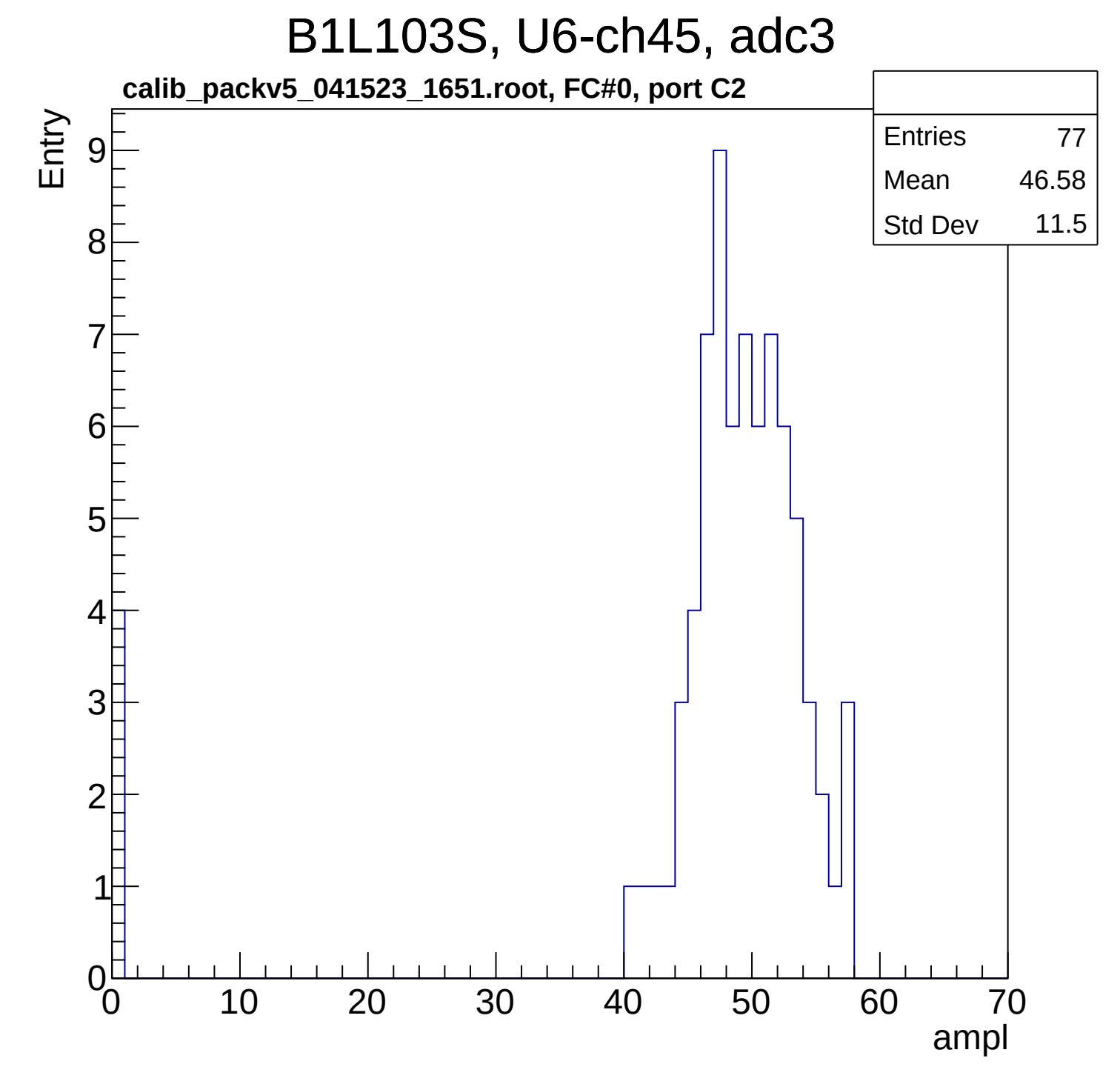
B1L103S, U6-ch45, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 46.58
Std Dev 11.5
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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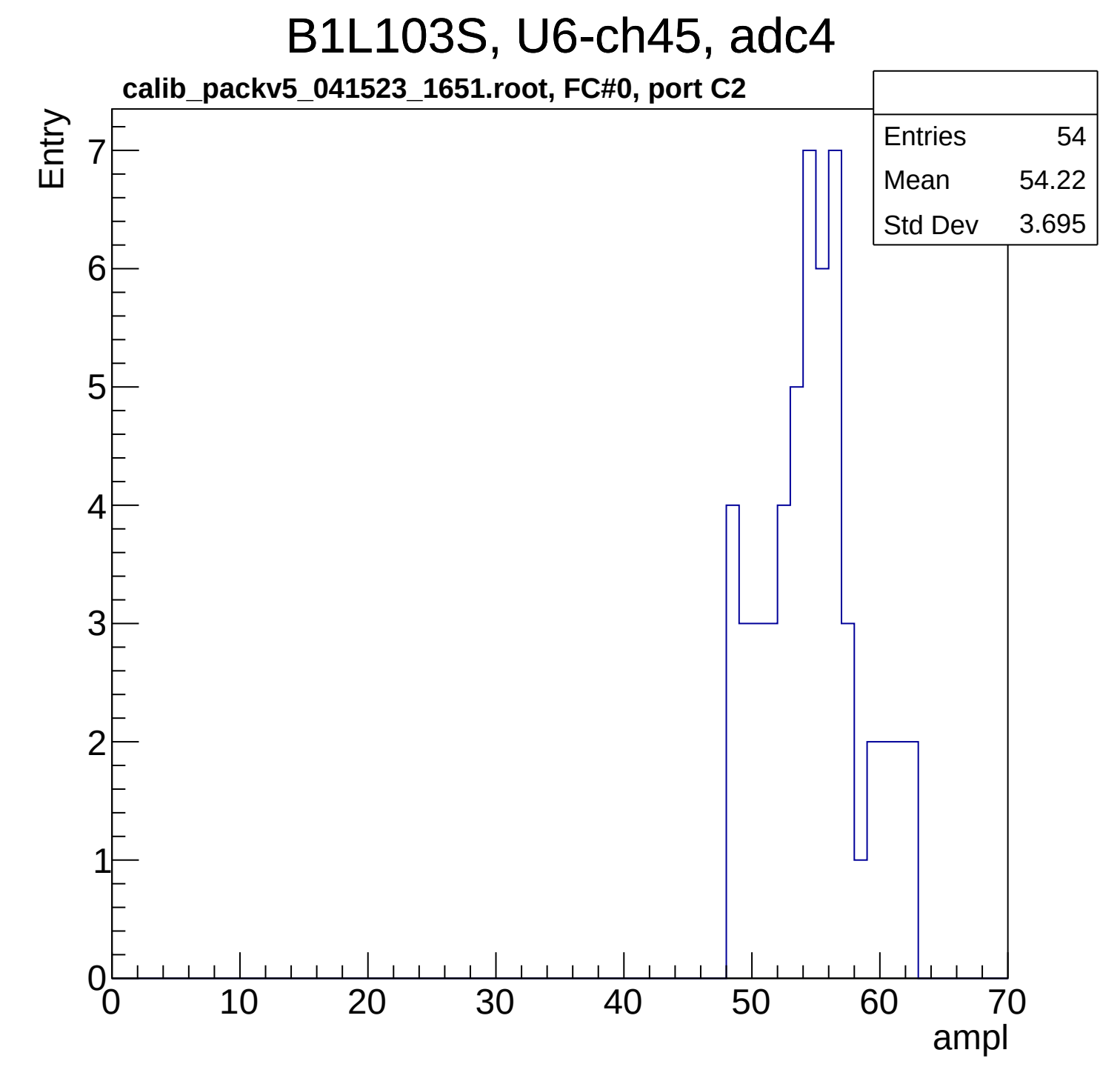
B1L103S, U6-ch45, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 54.22
Std Dev 3.695
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
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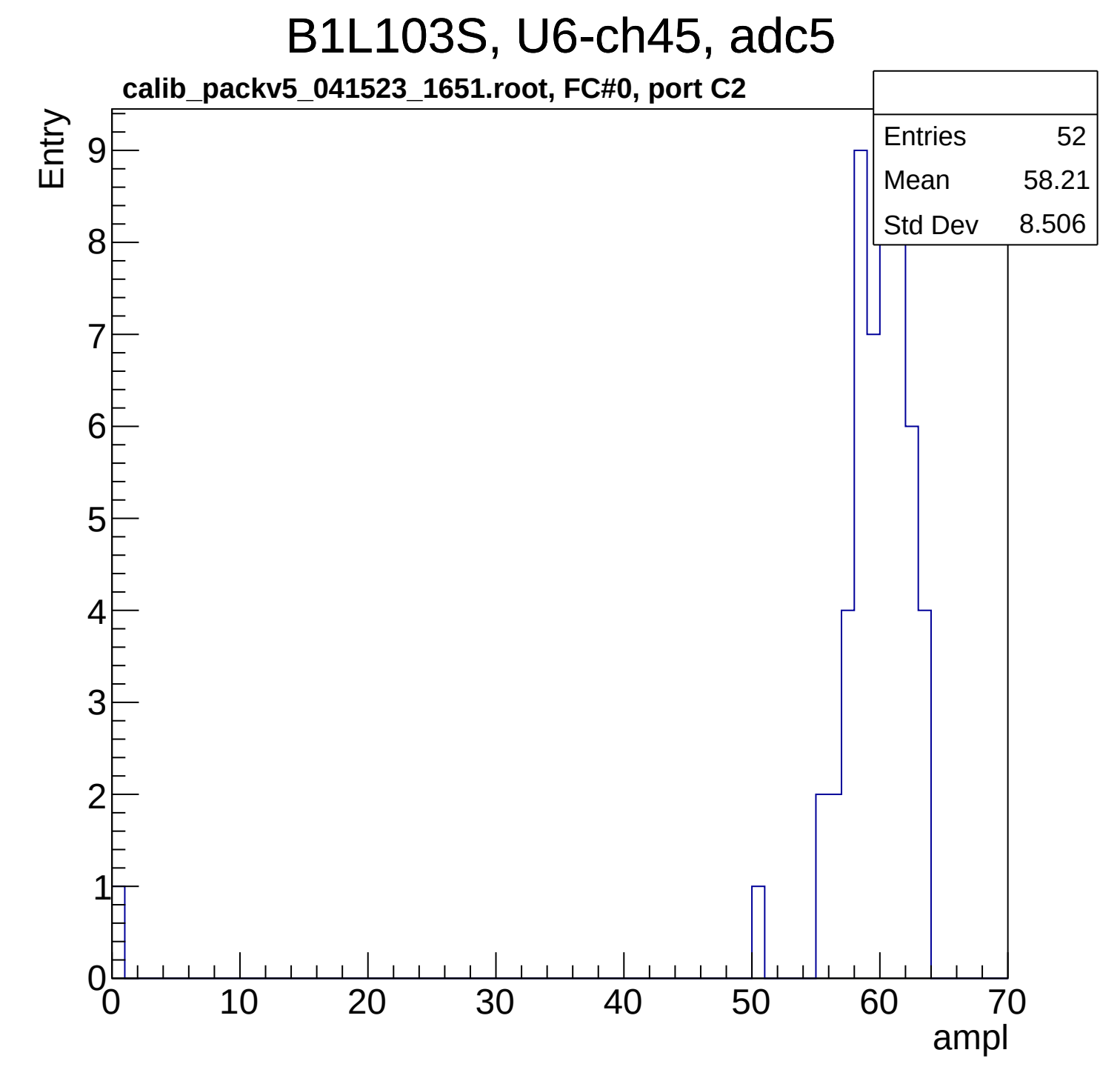
60
70


B1L103S, U6-ch45, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 58.21
Std Dev 8.506
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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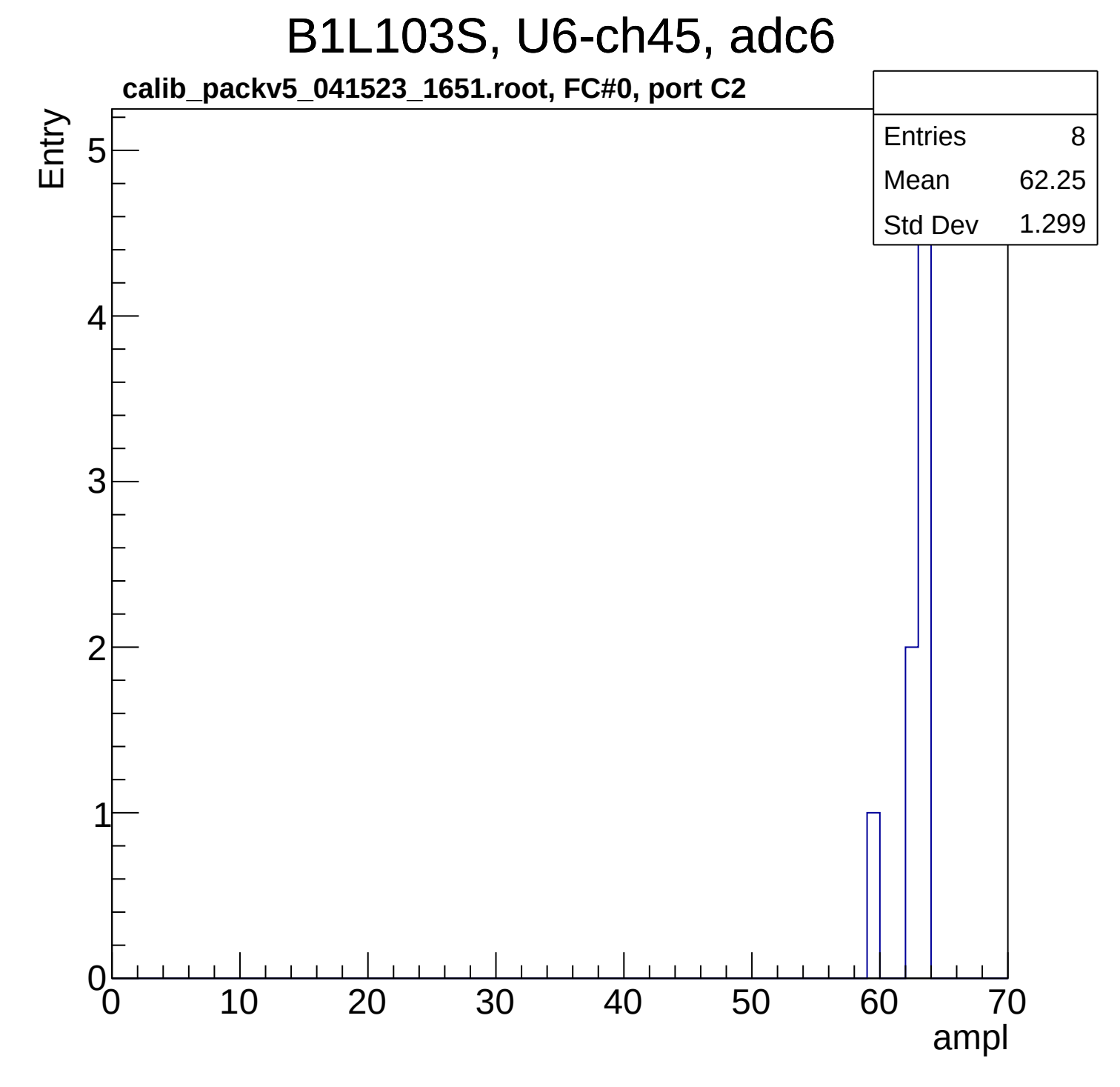
B1L103S, U6-ch45, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 62.25
Std Dev 1.299
Entry
ampl
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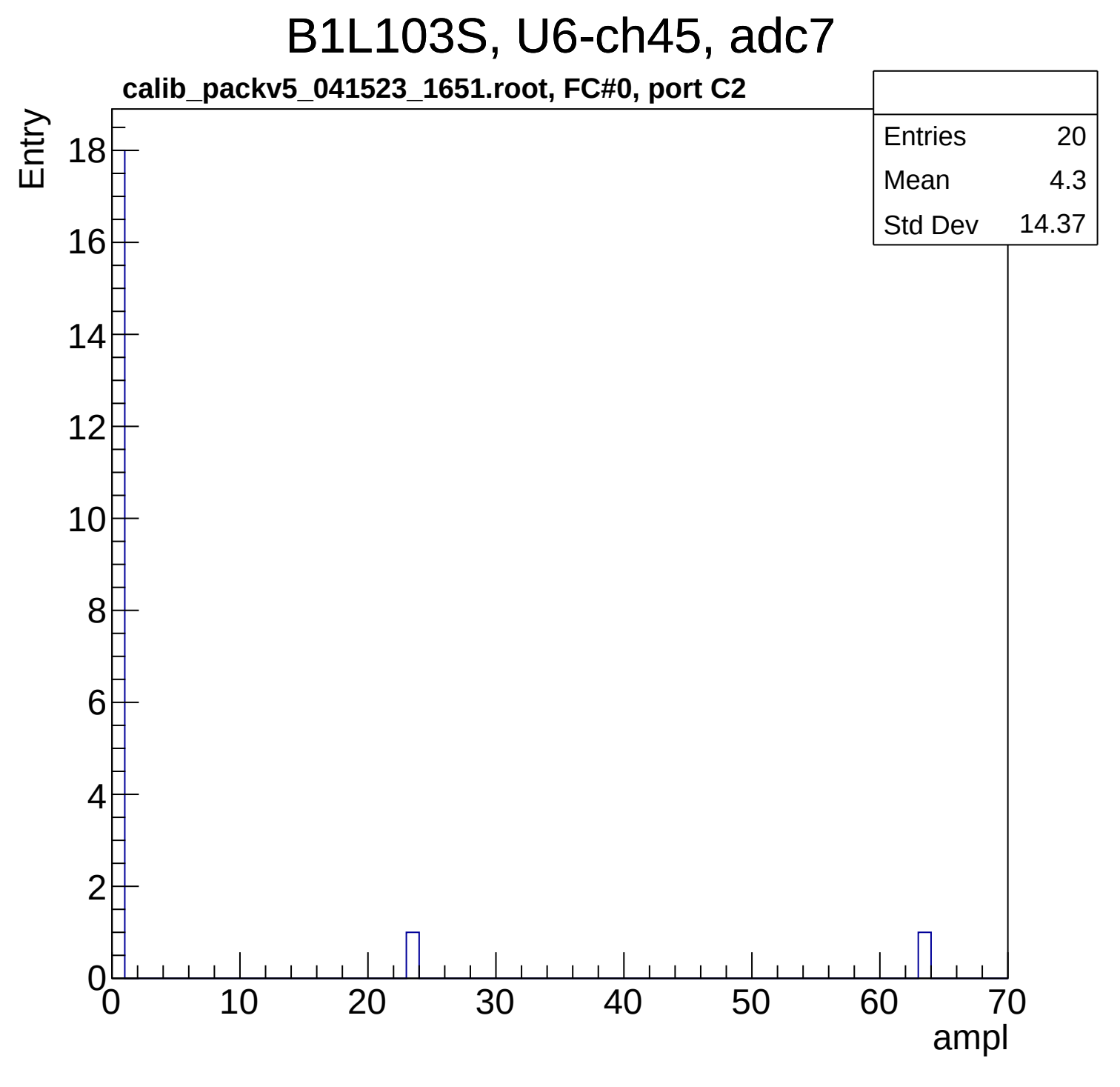
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U6-ch45, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4.3
Std Dev 14.37
Entry
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6
8
10
12
14
16
18
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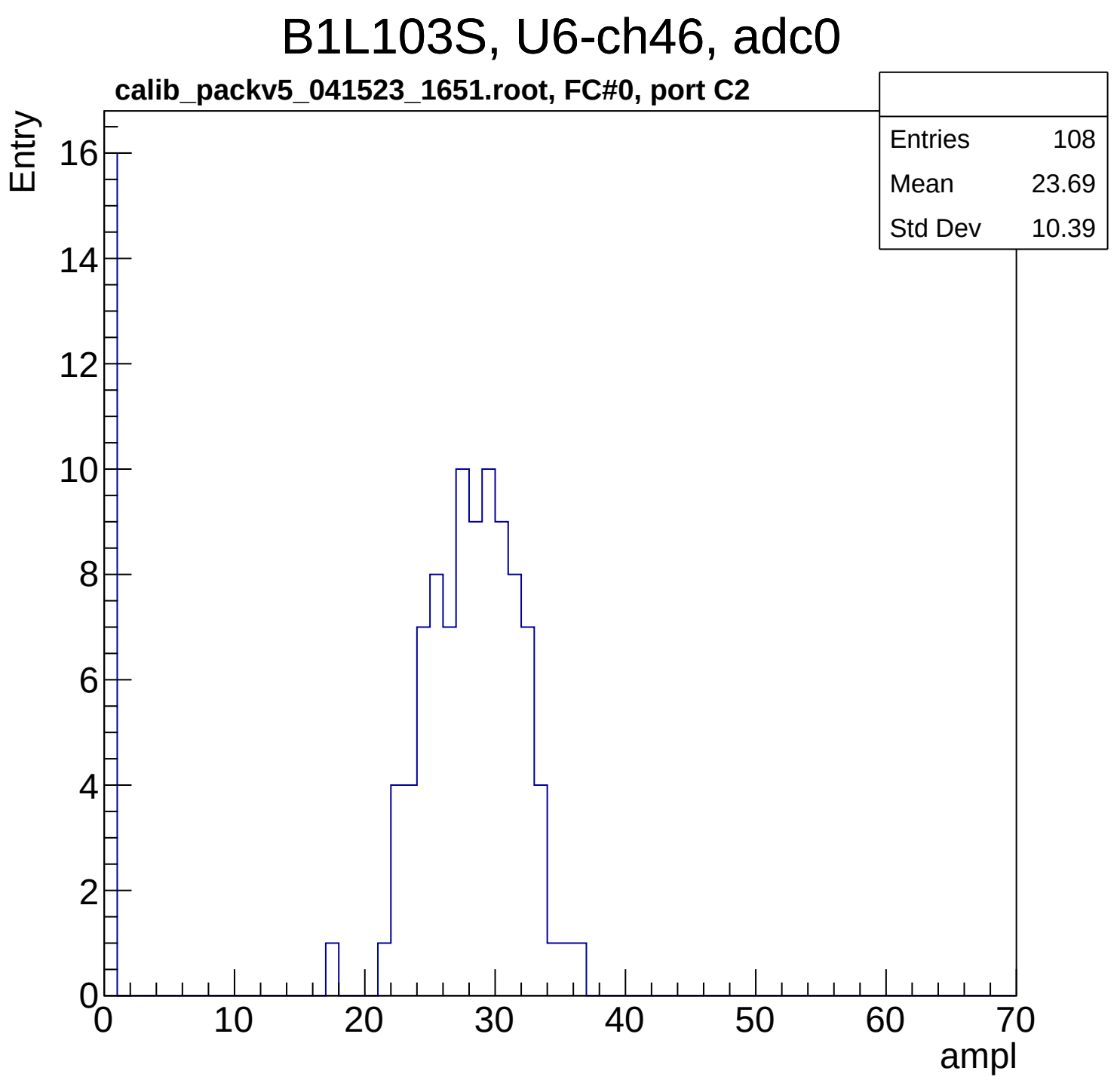
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch46, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 108
Mean 23.69
Std Dev 10.39
Entry
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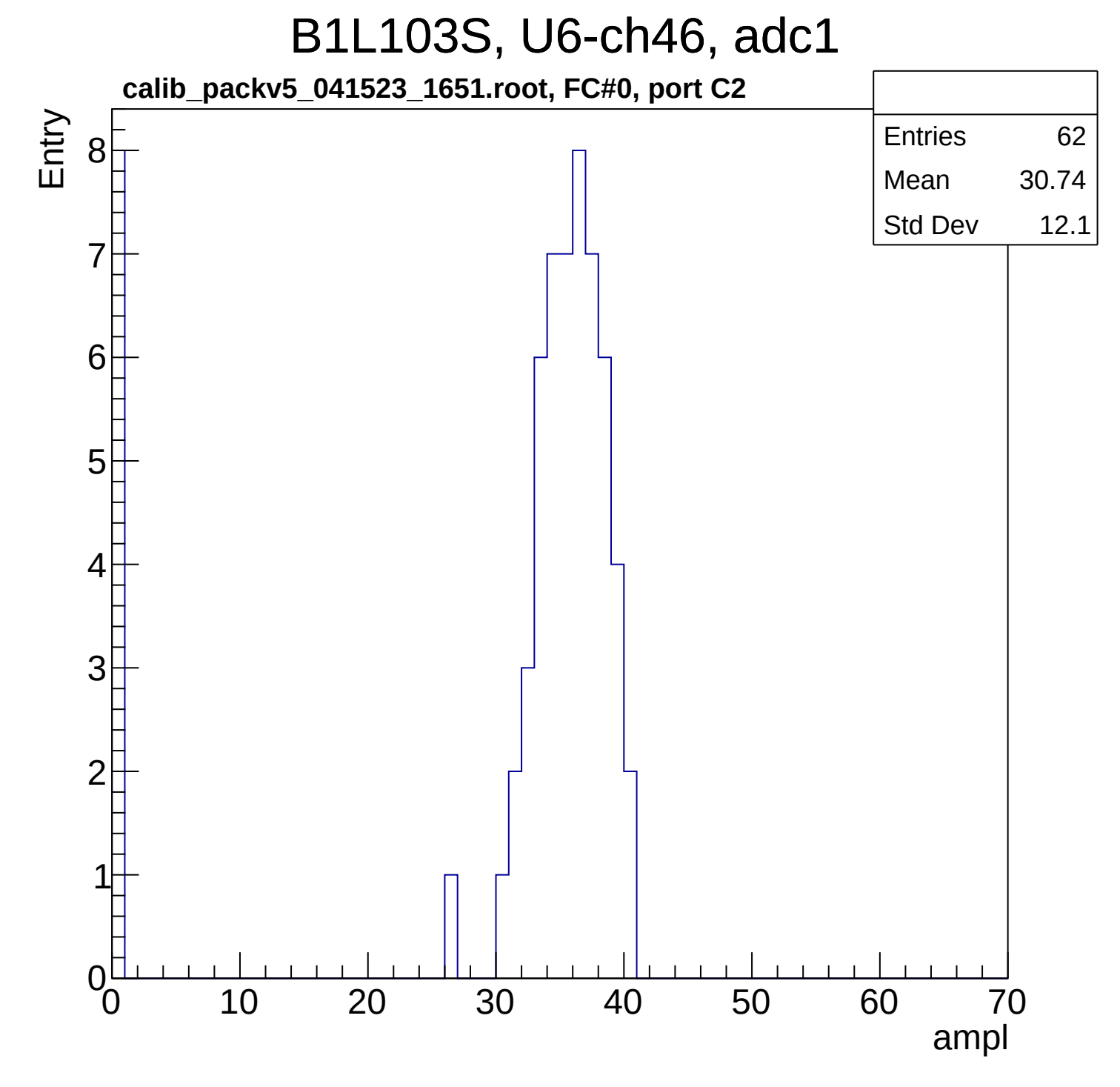
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch46, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 30.74
Std Dev 12.1
Entry
ampl
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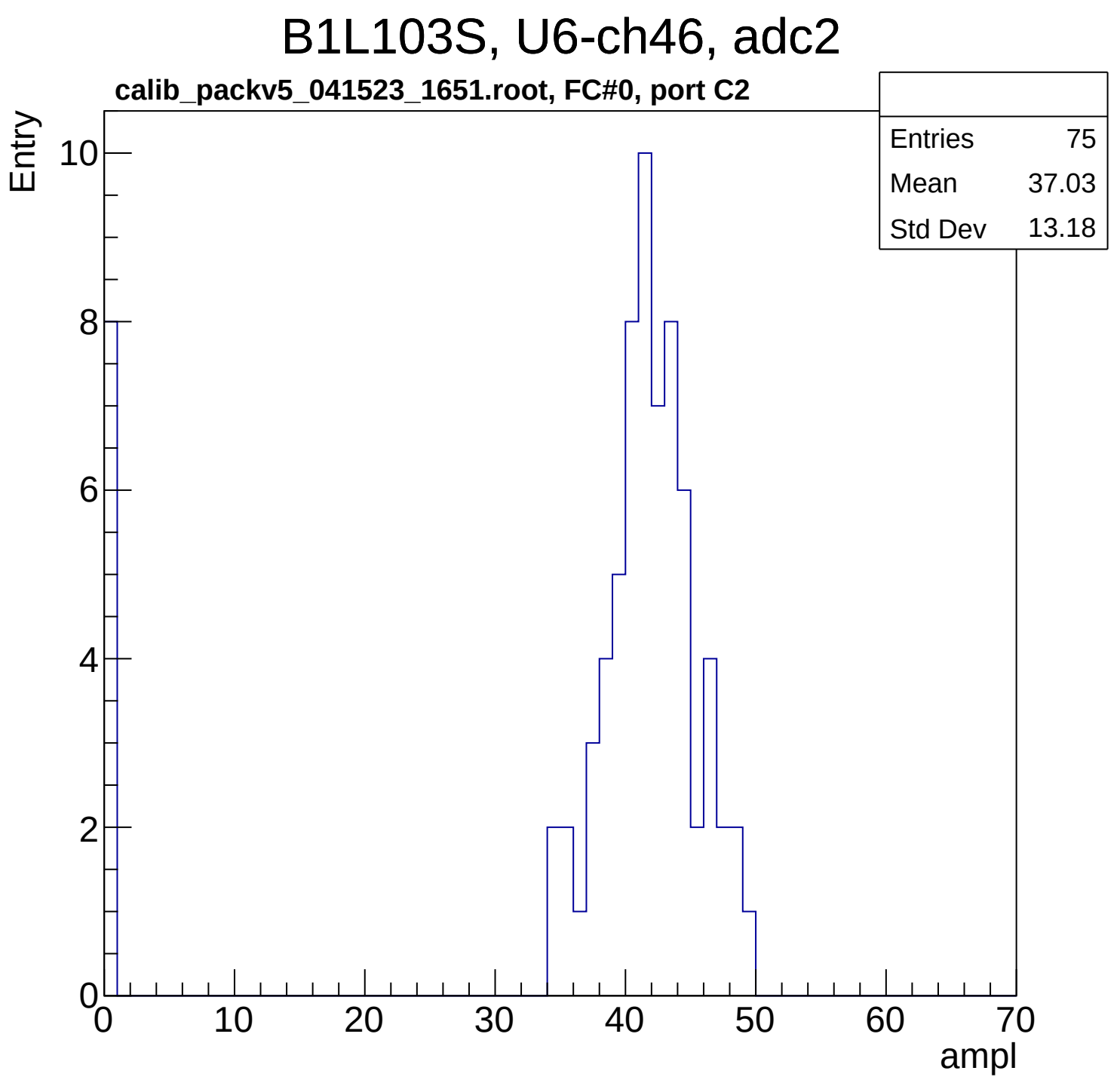
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch46, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 37.03
Std Dev 13.18
Entry
ampl
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2
4
6
8
10
0
10
20
30
40
50
60
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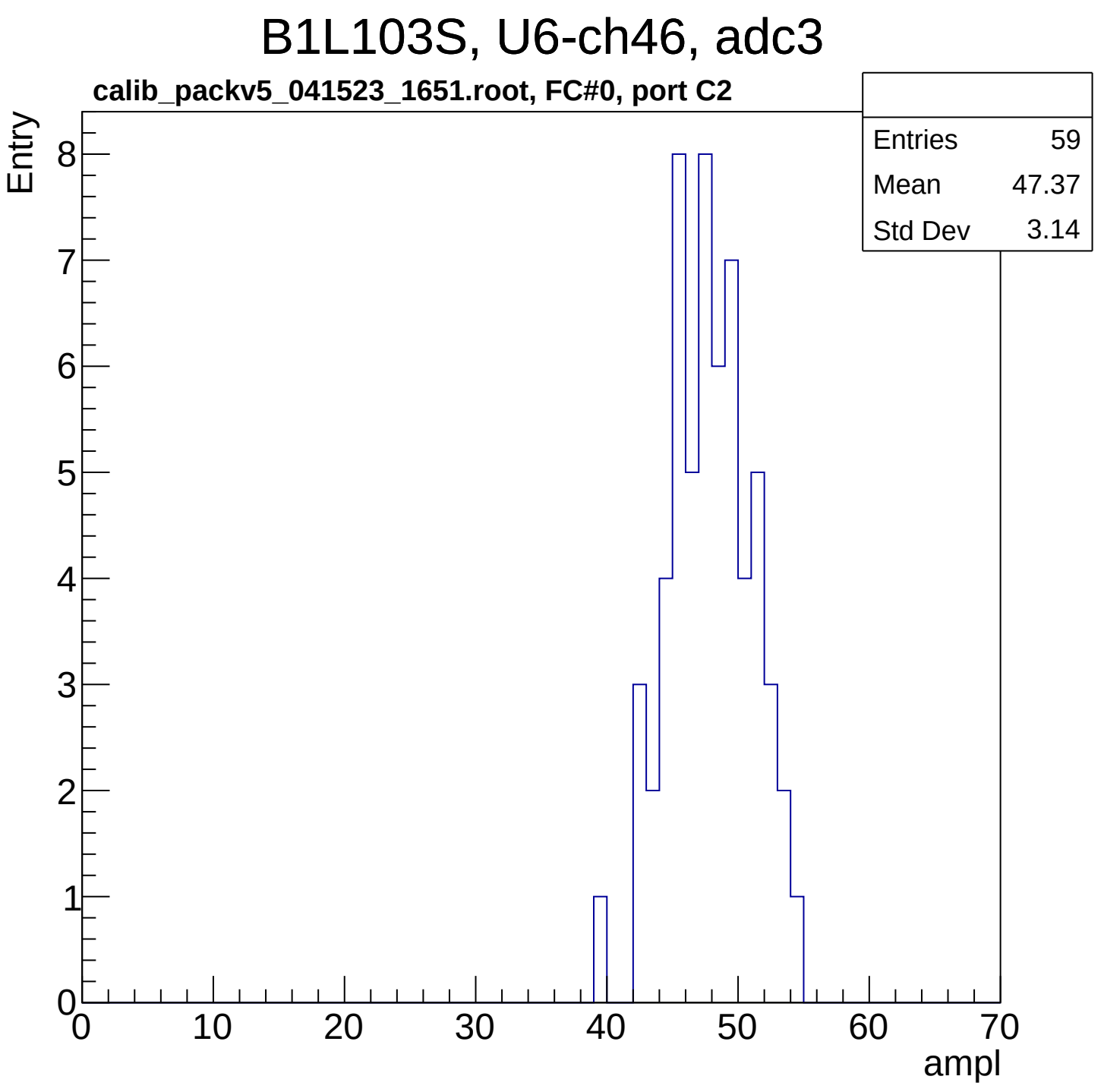
B1L103S, U6-ch46, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 47.37
Std Dev 3.14
Entry
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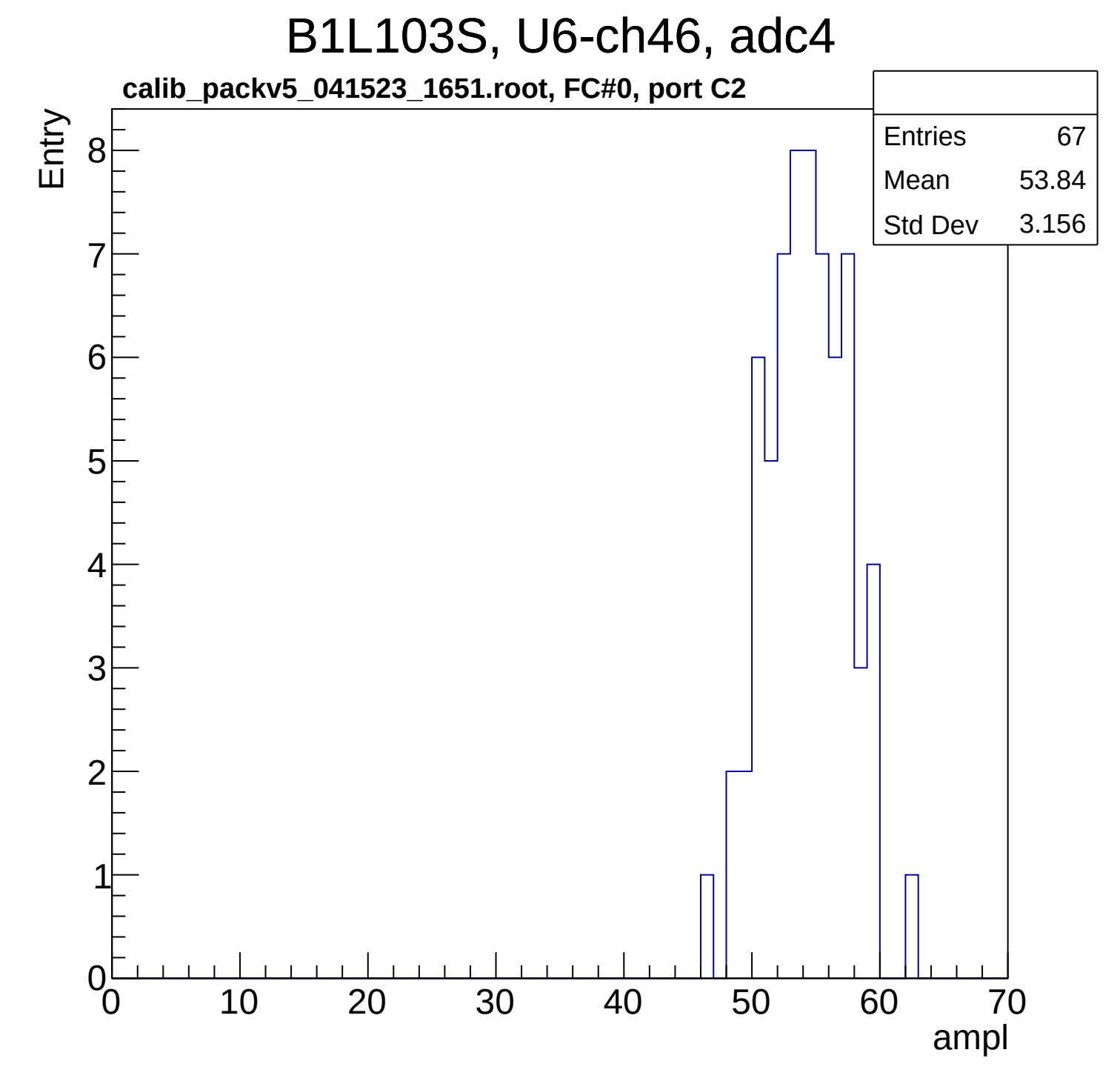
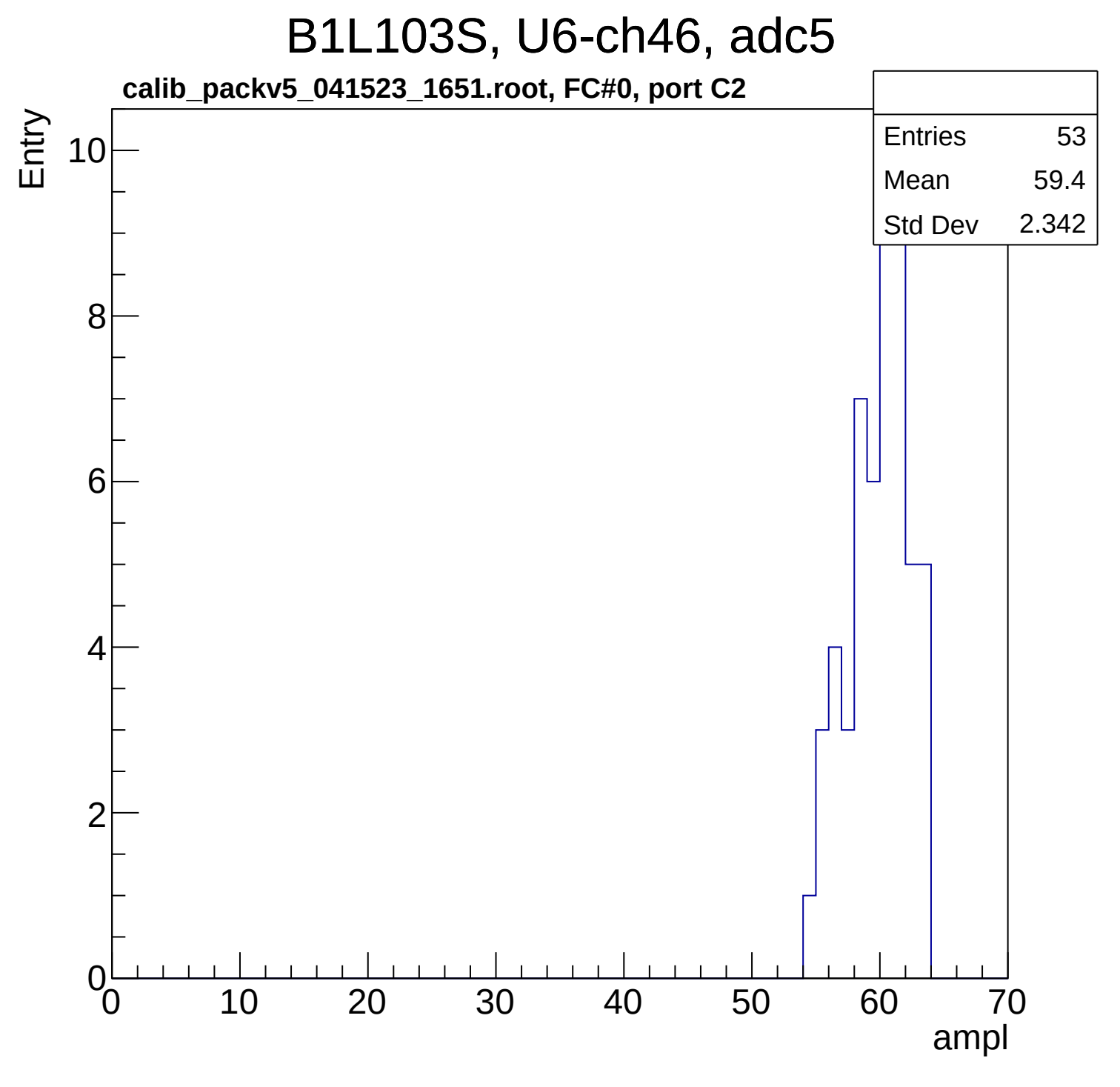
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch46, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 53.84
Std Dev 3.156
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch46, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 59.4
Std Dev 2.342
Entry
0
2
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6
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10
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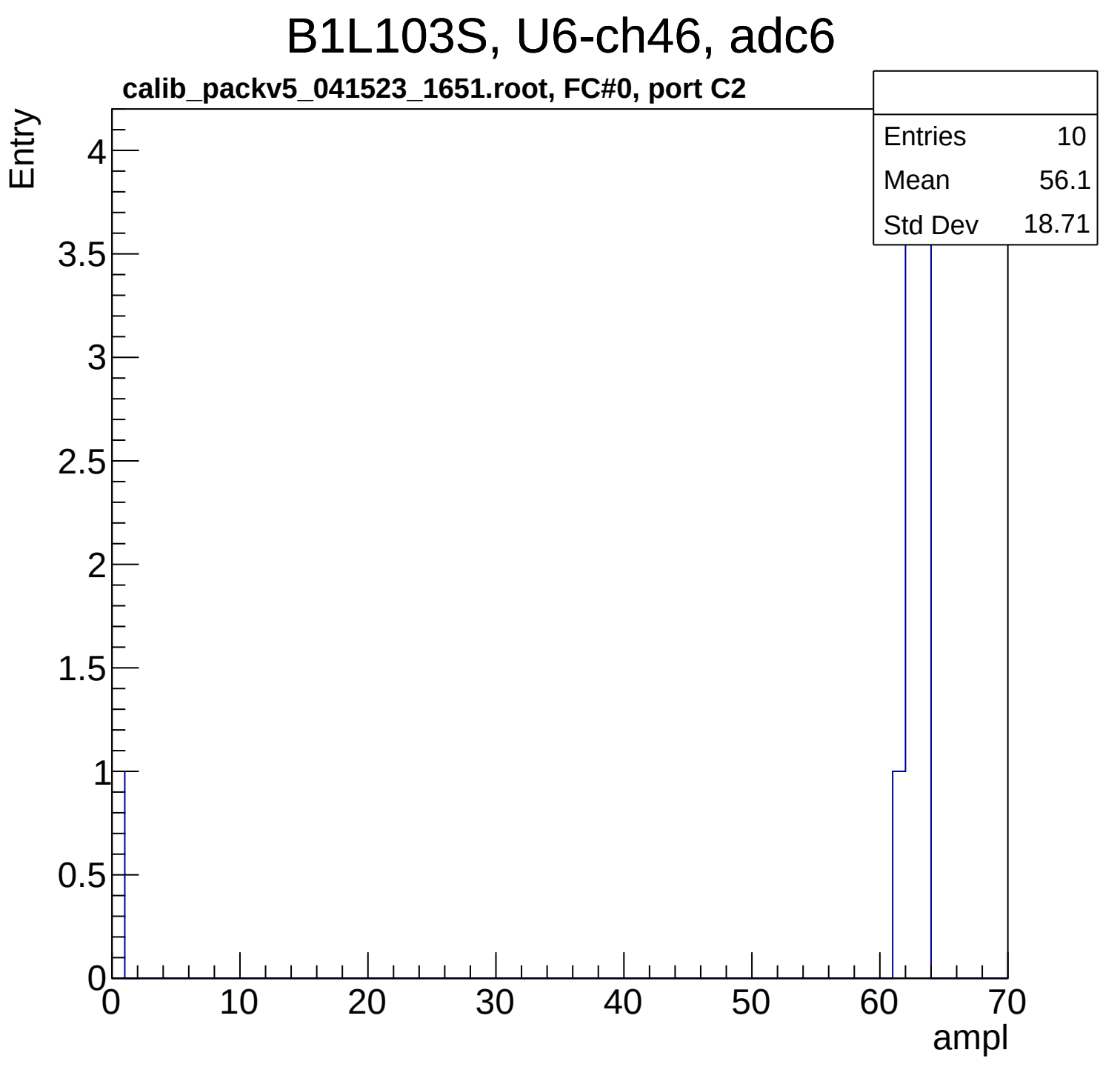
ampl


B1L103S, U6-ch46, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 56.1
Std Dev 18.71
Entry
ampl
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1.5
2
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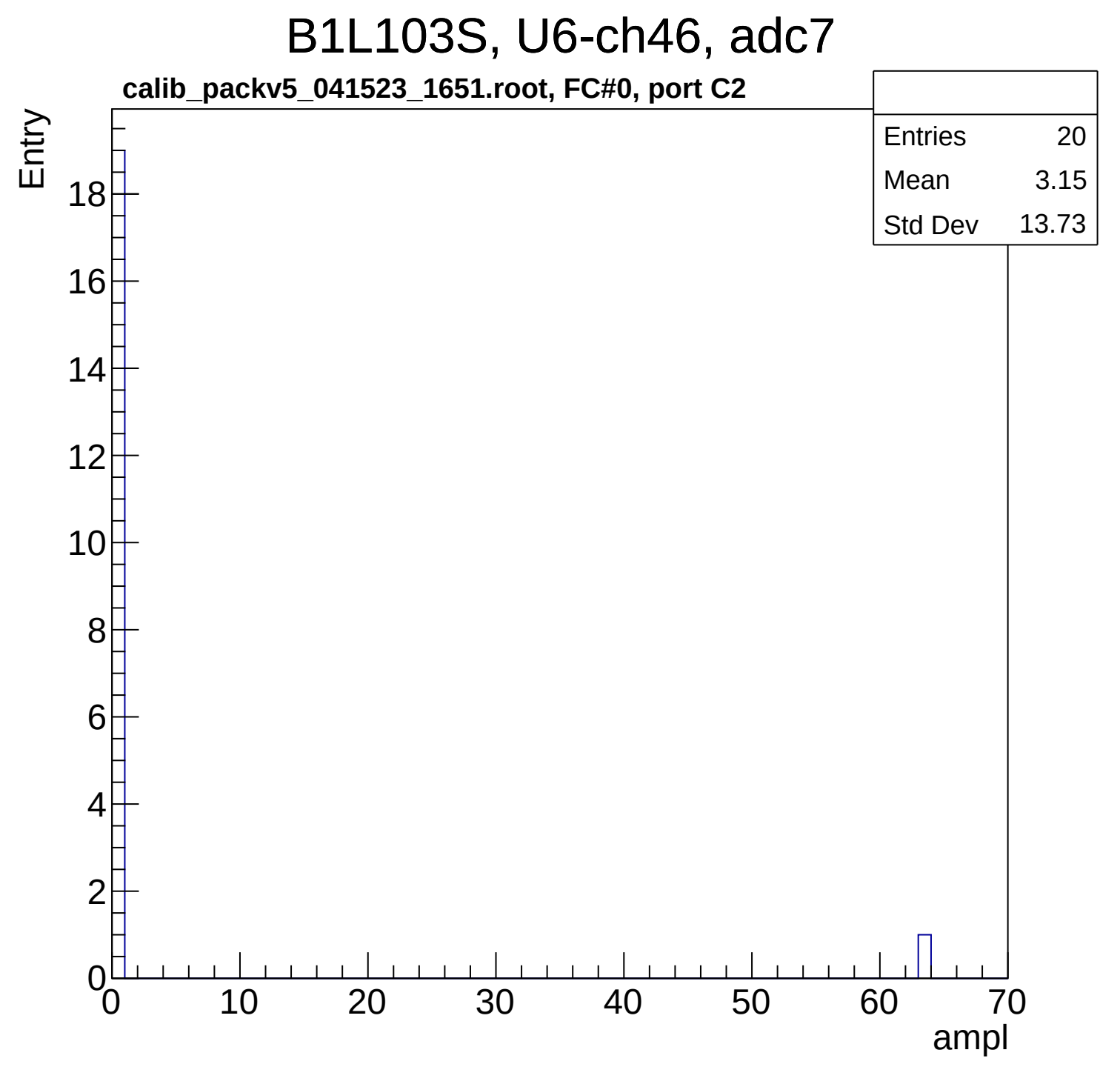
B1L103S, U6-ch46, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
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6
8
10
12
14
16
18
0
10
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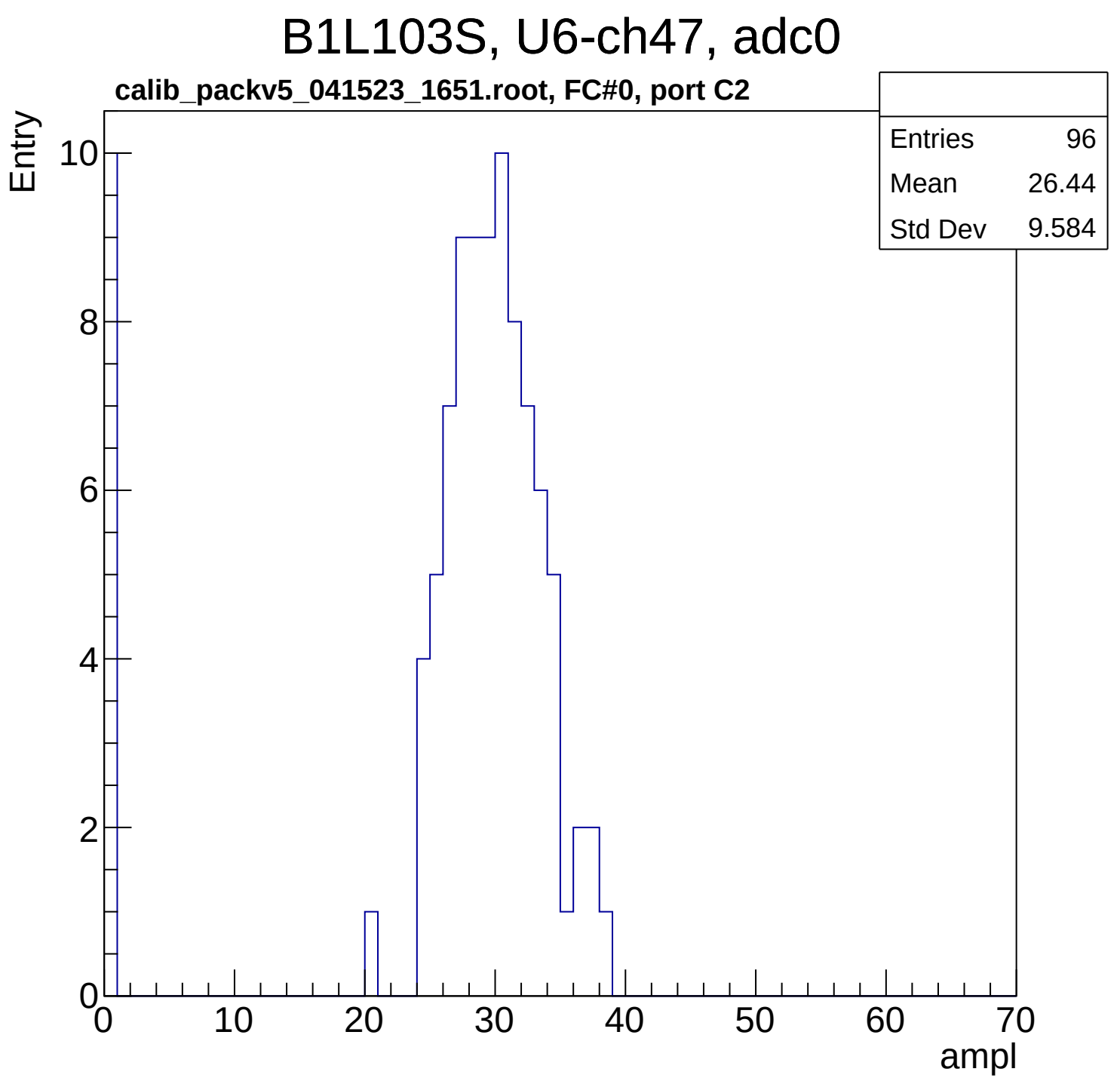
50
60
70
ampl


B1L103S, U6-ch47, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 96
Mean 26.44
Std Dev 9.584
Entry
ampl
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4
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8
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0
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40
50
60
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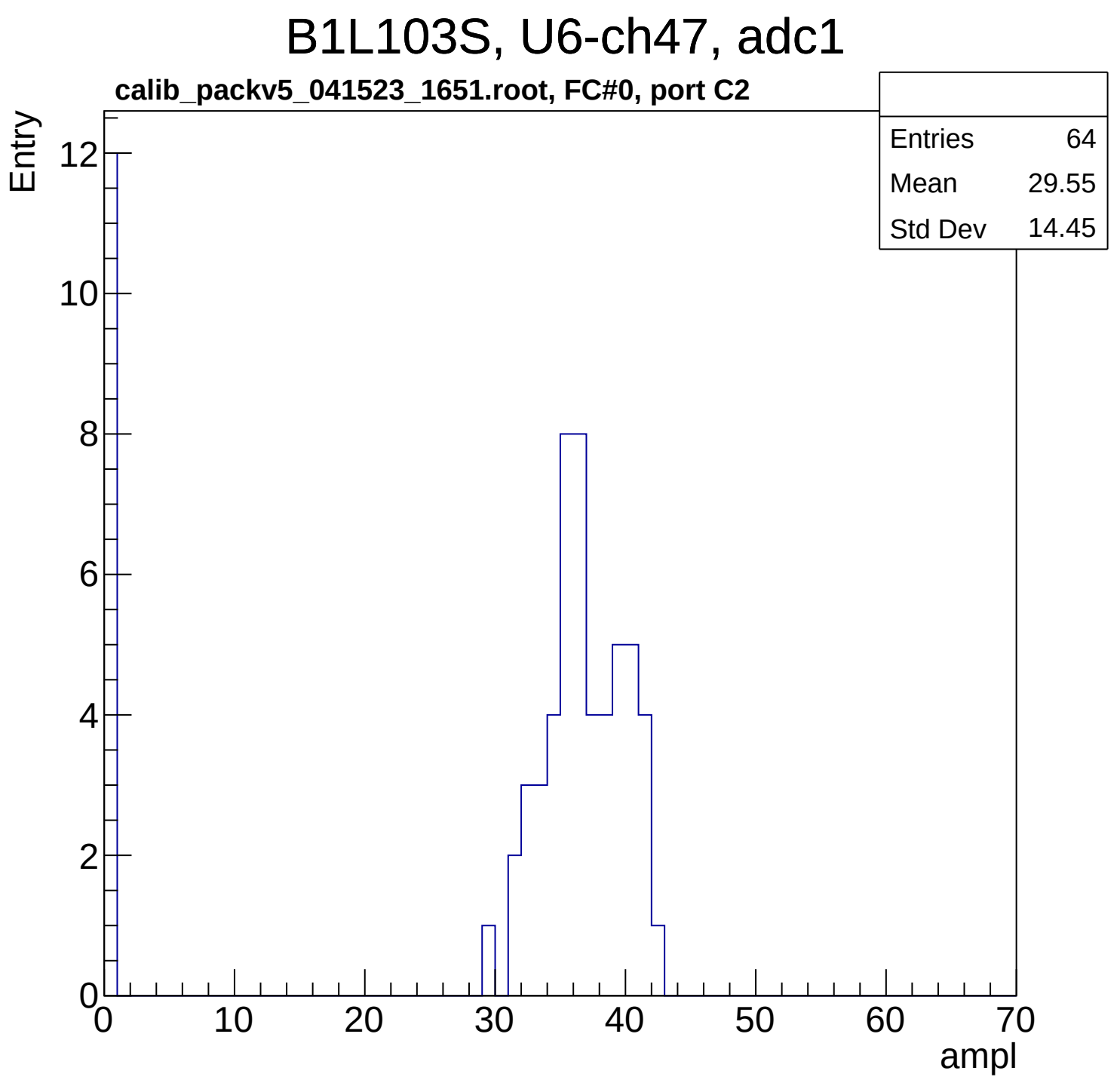
B1L103S, U6-ch47, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 29.55
Std Dev 14.45
Entry
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8
10
12
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50
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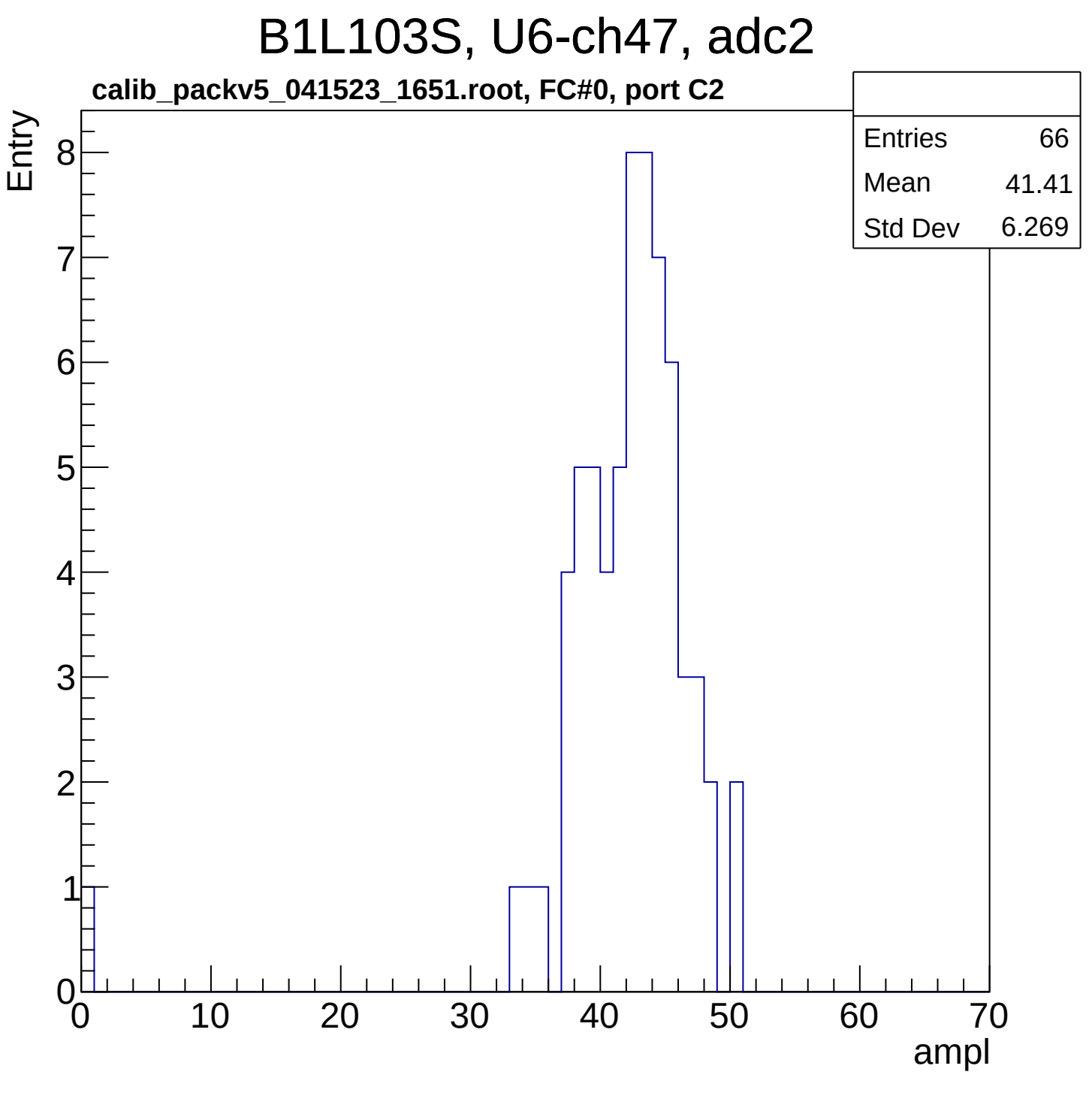
70
ampl


B1L103S, U6-ch47, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 41.41
Std Dev 6.269
Entry
ampl
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7
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0
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40
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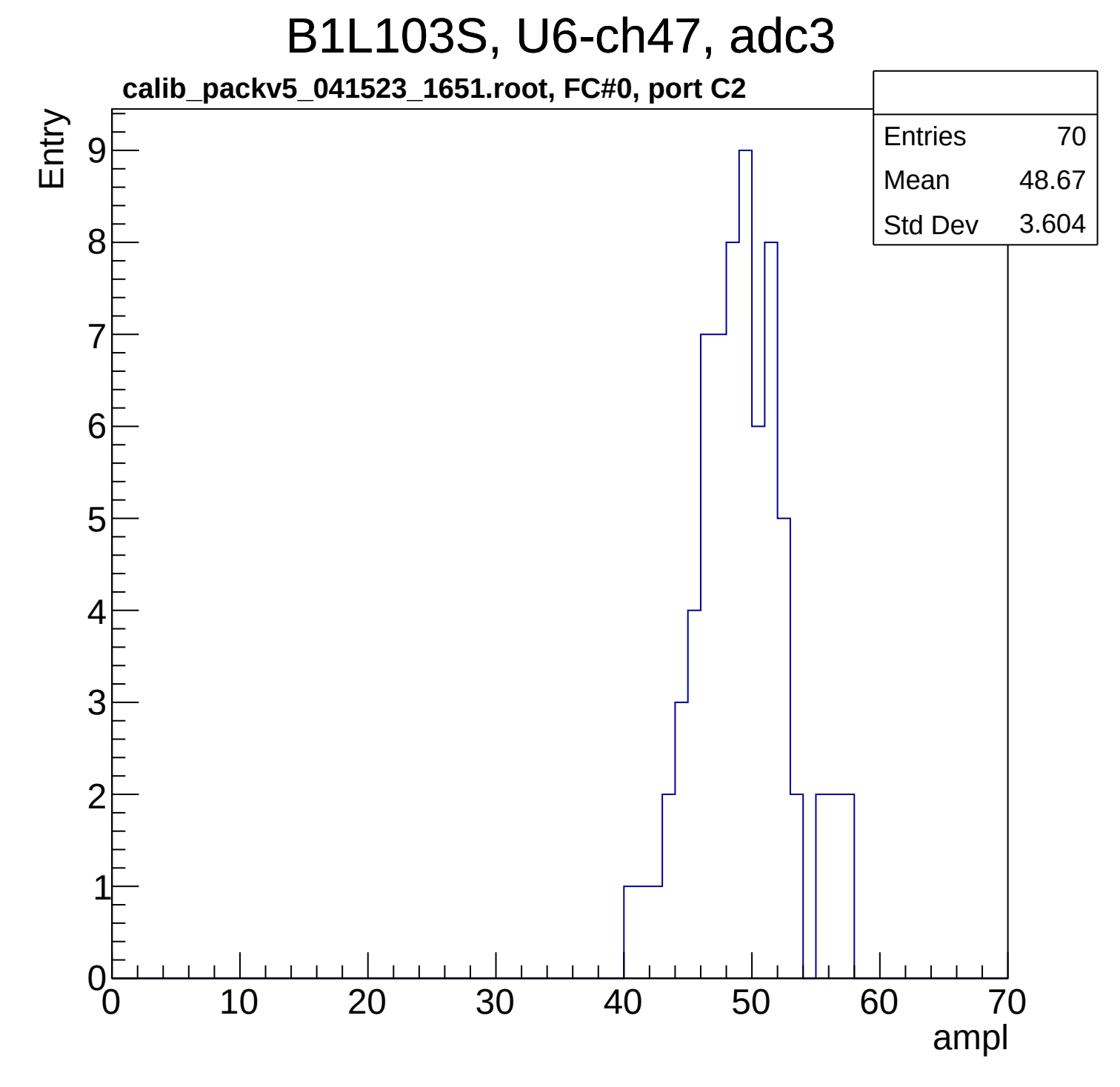
B1L103S, U6-ch47, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 48.67
Std Dev 3.604
Entry
ampl
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3
4
5
6
7
8
9
0
10
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40
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60
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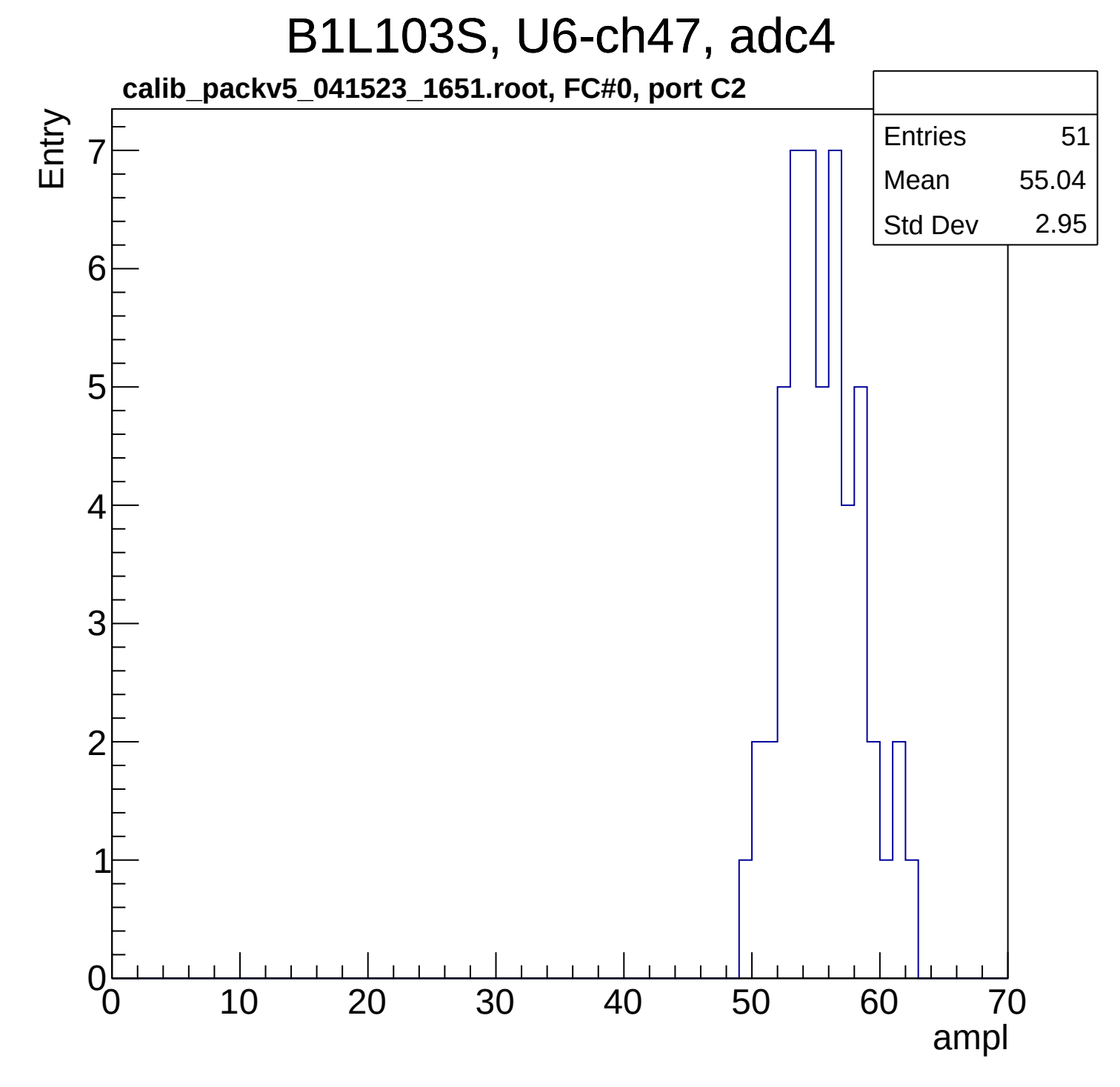
B1L103S, U6-ch47, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 55.04
Std Dev 2.95
Entry
ampl
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1
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3
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6
7
0
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40
50
60
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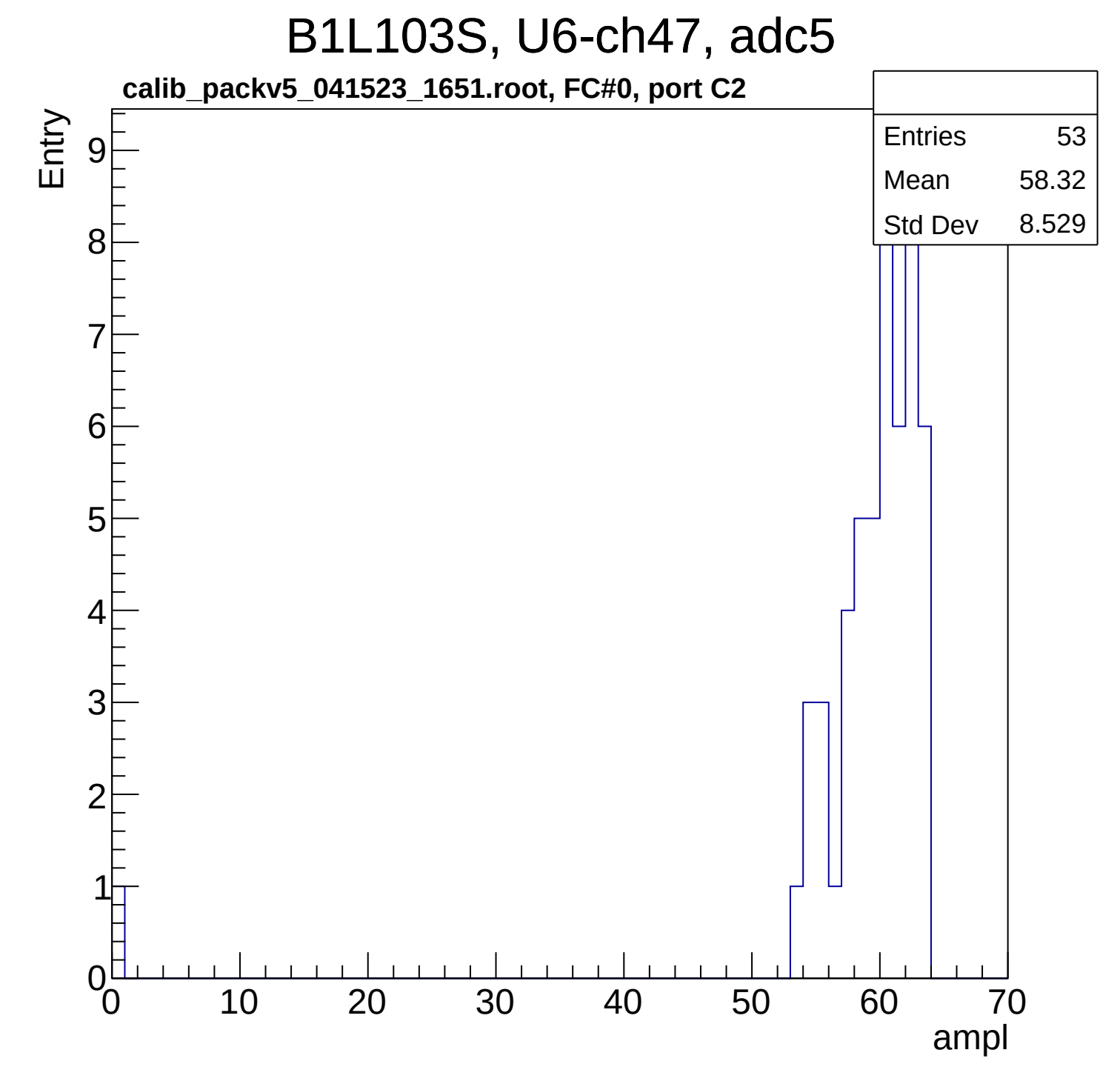
B1L103S, U6-ch47, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 58.32
Std Dev 8.529
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
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60
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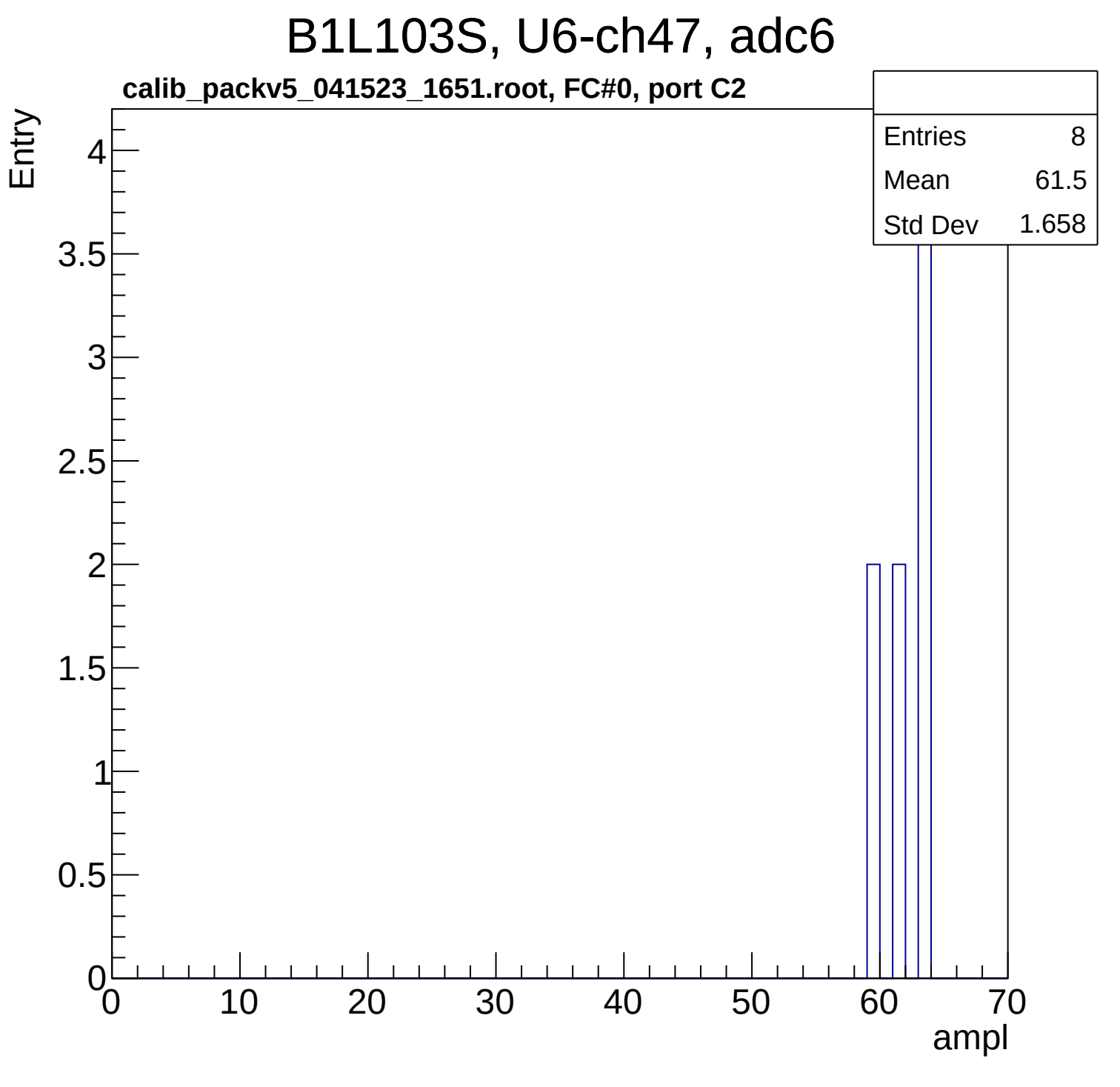
B1L103S, U6-ch47, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 61.5
Std Dev 1.658
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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40
50
60
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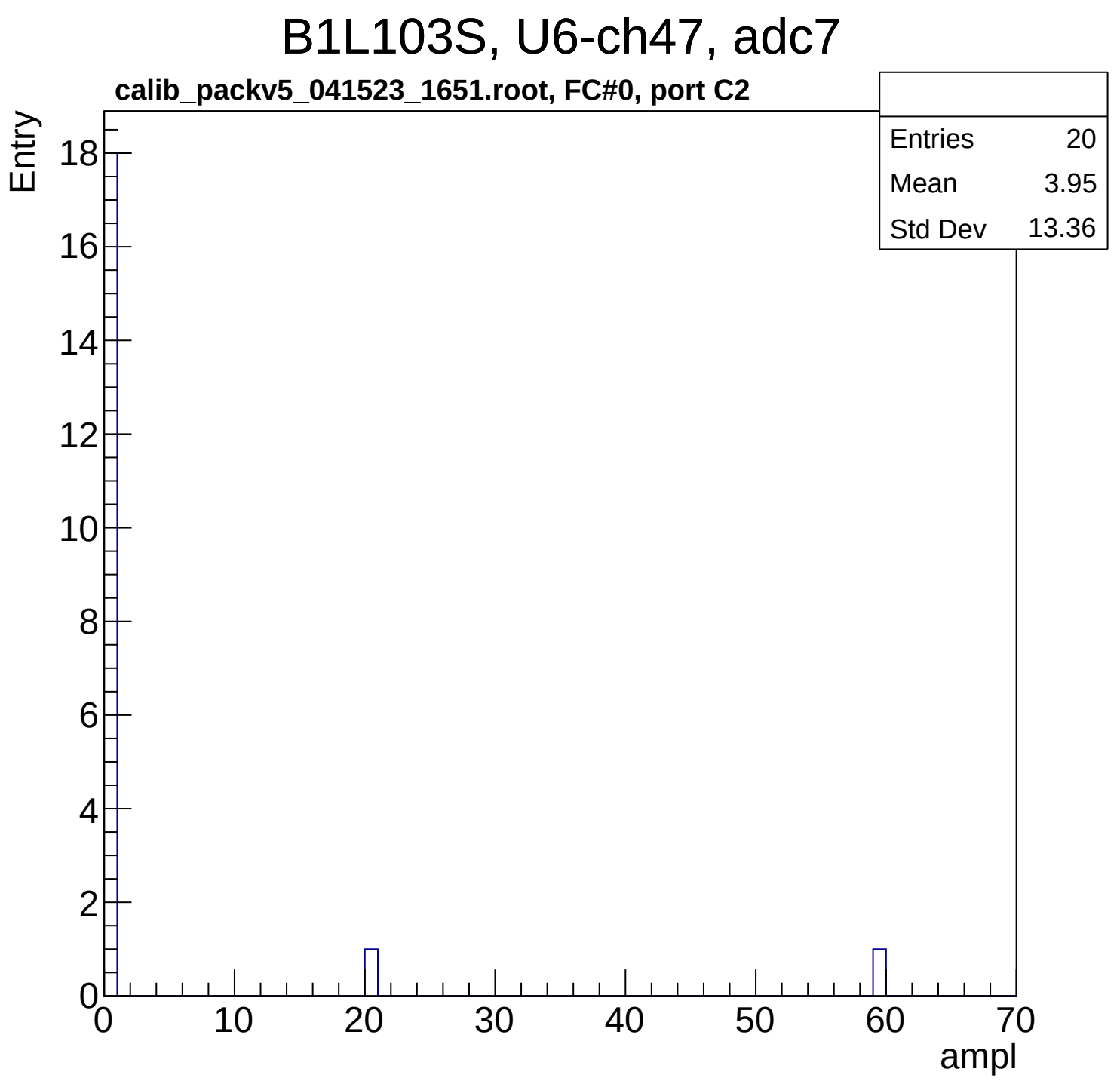
B1L103S, U6-ch47, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.95
Std Dev 13.36
Entry
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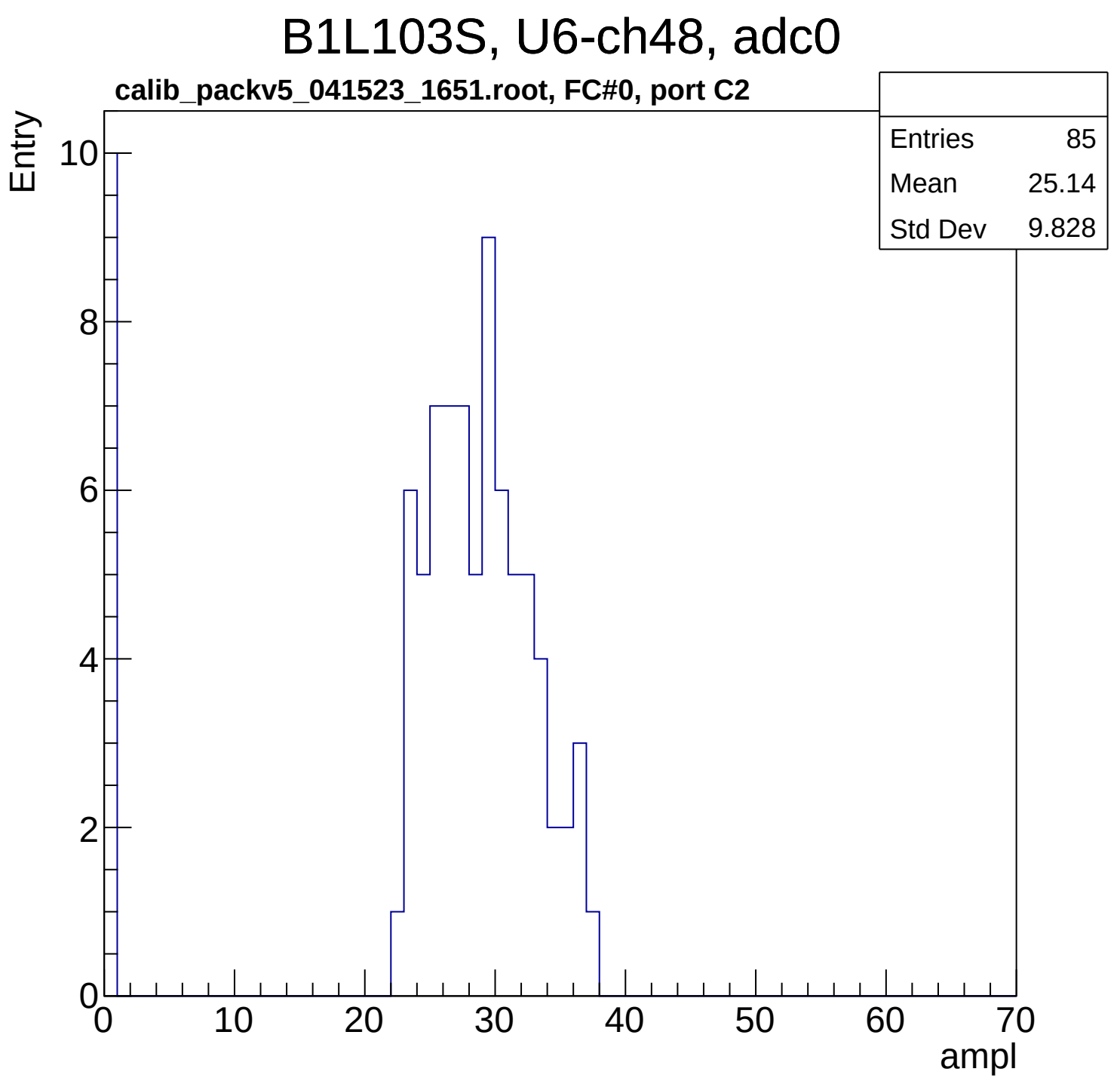
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch48, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 25.14
Std Dev 9.828
Entry
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2
4
6
8
10
0
10
20
30
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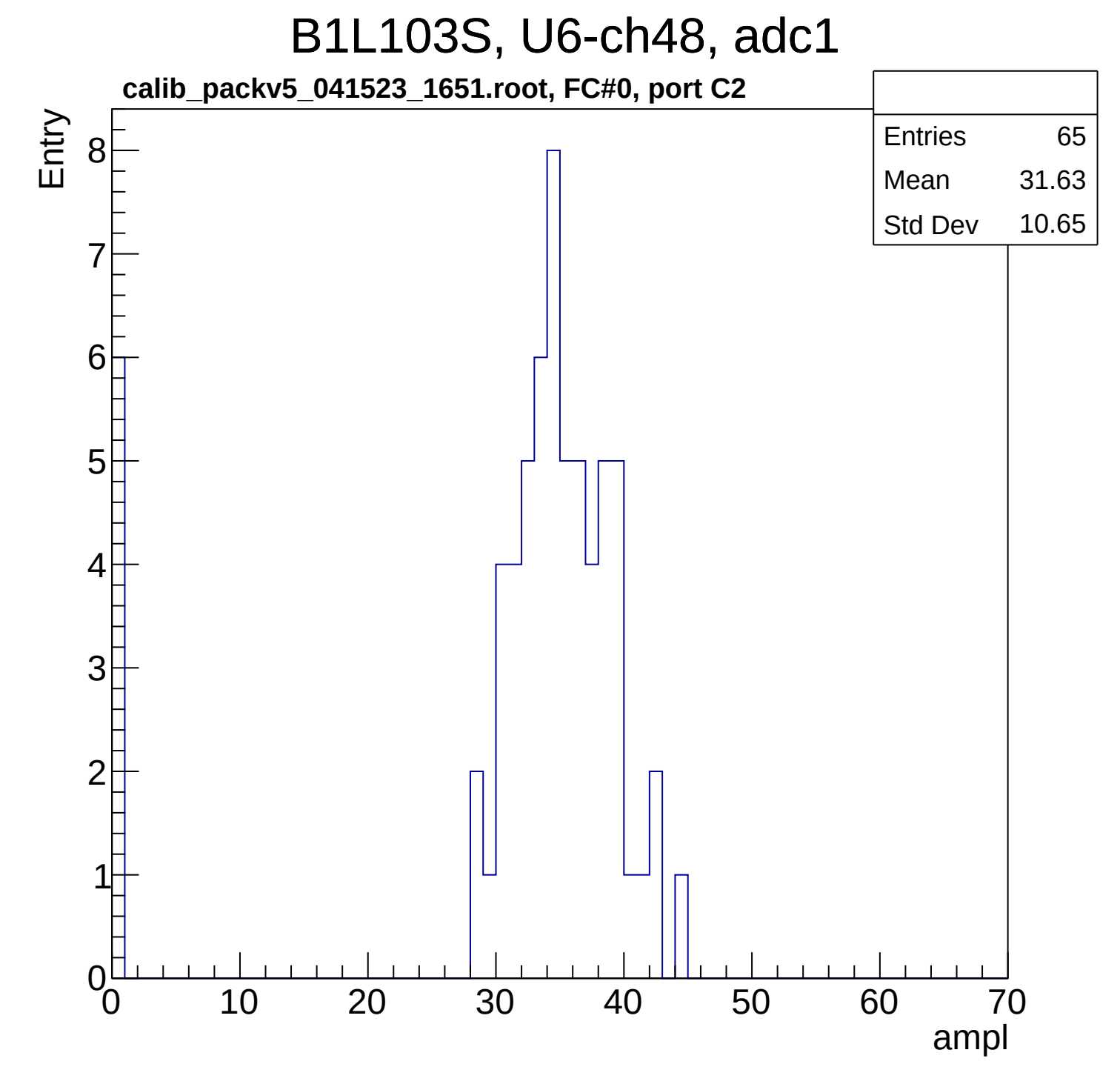
50
60
70
ampl


B1L103S, U6-ch48, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 31.63
Std Dev 10.65
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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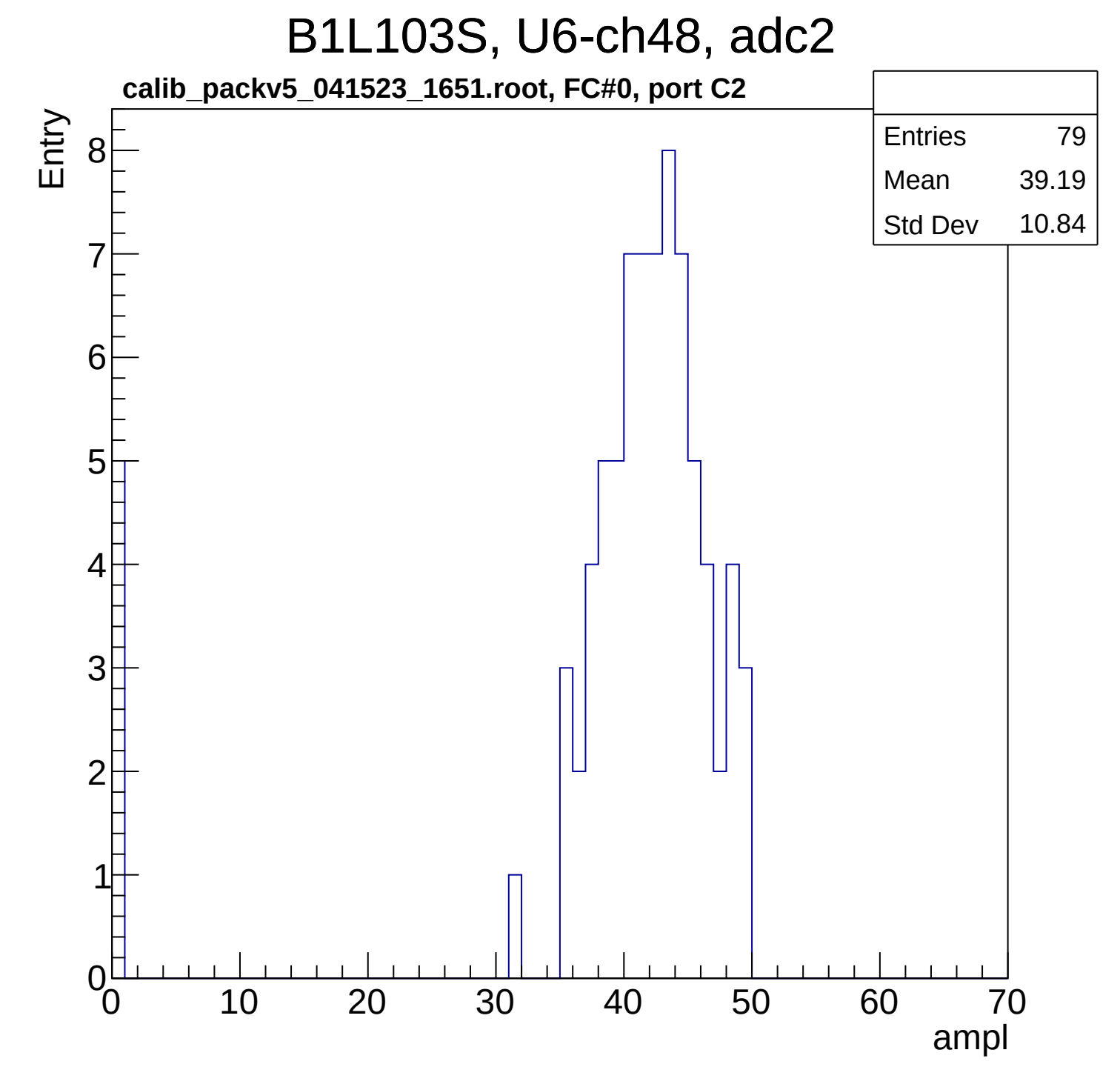
B1L103S, U6-ch48, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 39.19
Std Dev 10.84
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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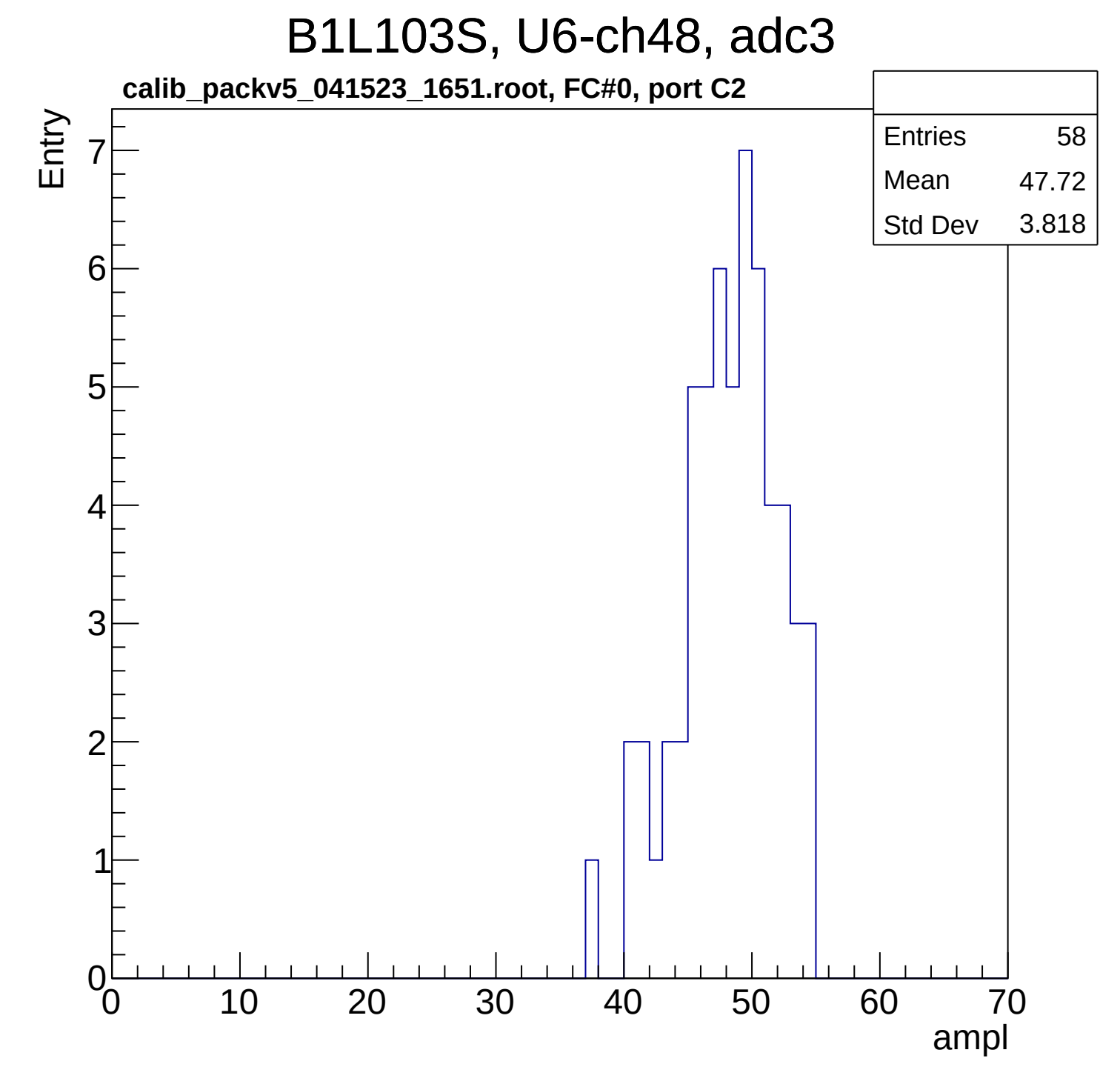
40
50
60
70


B1L103S, U6-ch48, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 47.72
Std Dev 3.818
Entry
ampl
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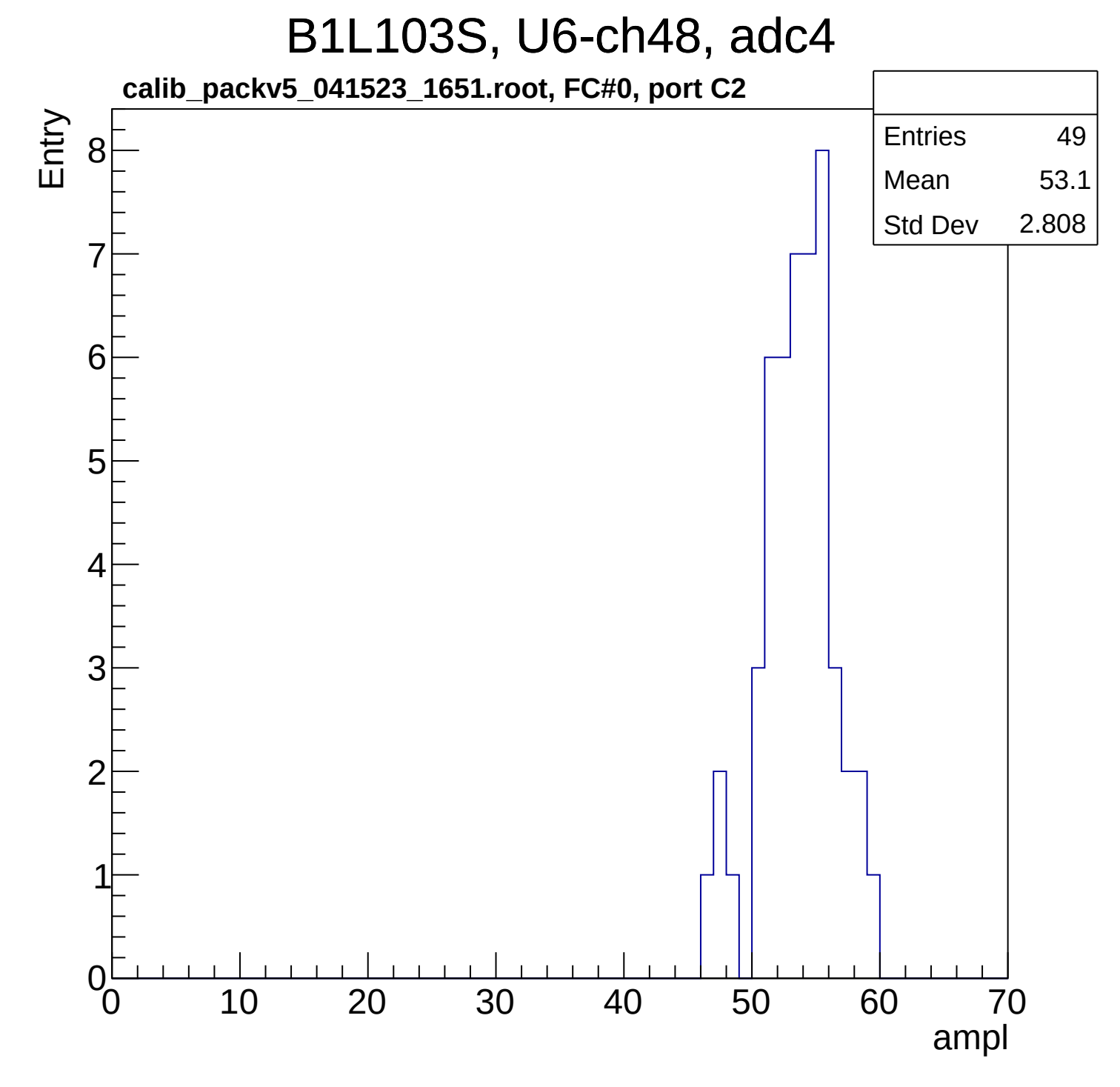
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U6-ch48, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 53.1
Std Dev 2.808
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
50
60
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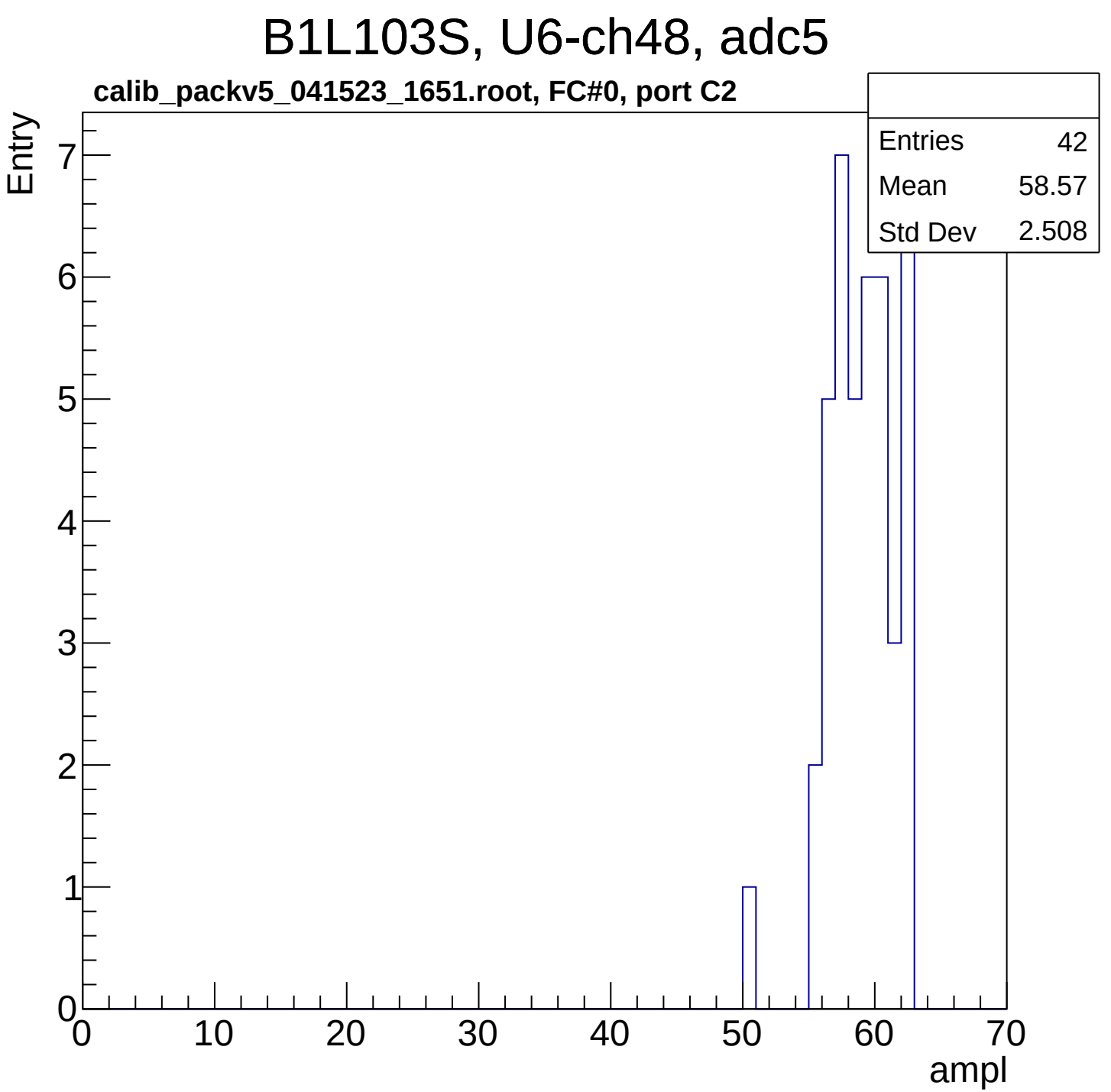
B1L103S, U6-ch48, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 58.57
Std Dev 2.508
Entry
ampl
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3
4
5
6
7
0
10
20
30
40
50
60
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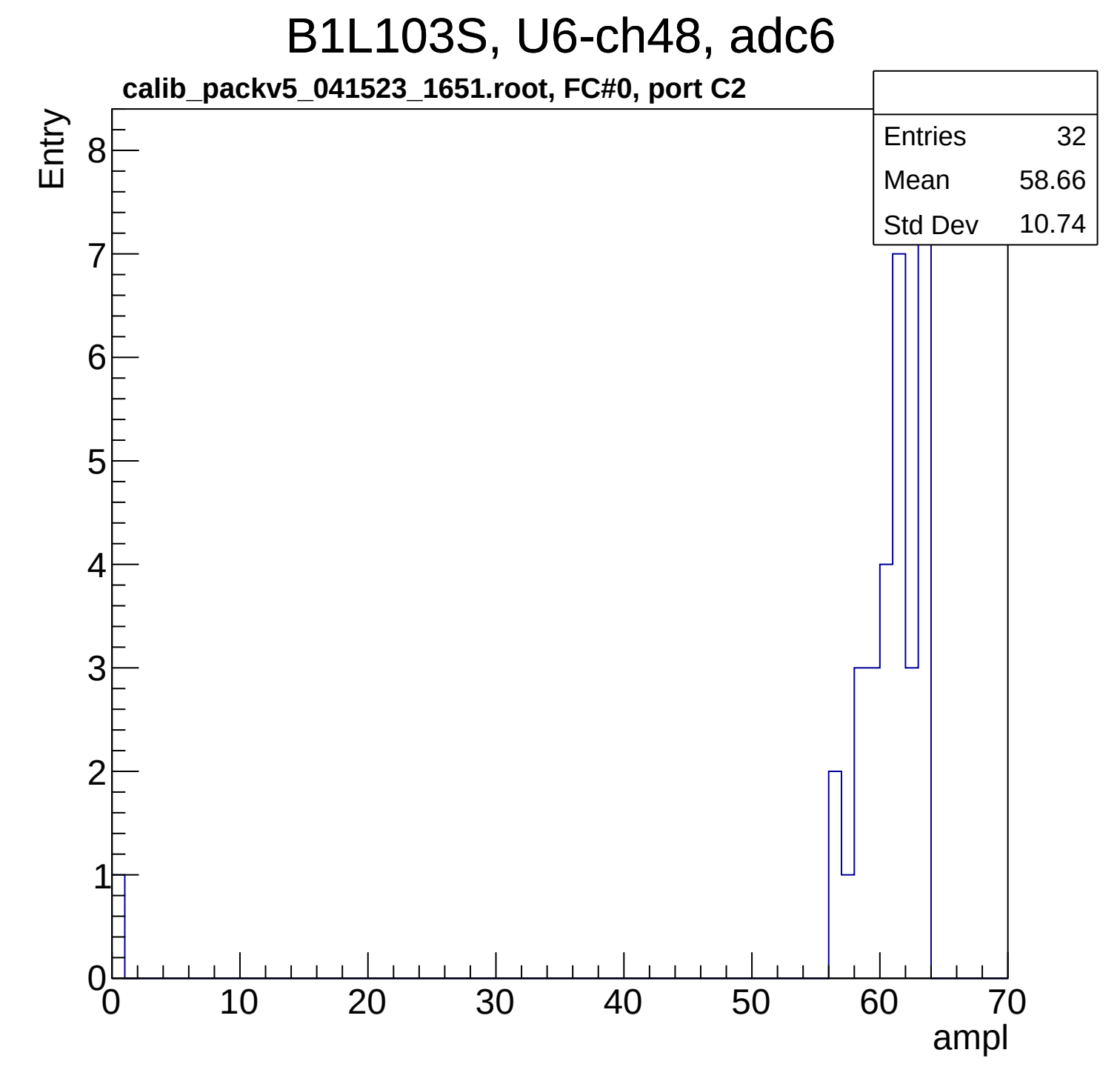
B1L103S, U6-ch48, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 58.66
Std Dev 10.74
Entry
ampl
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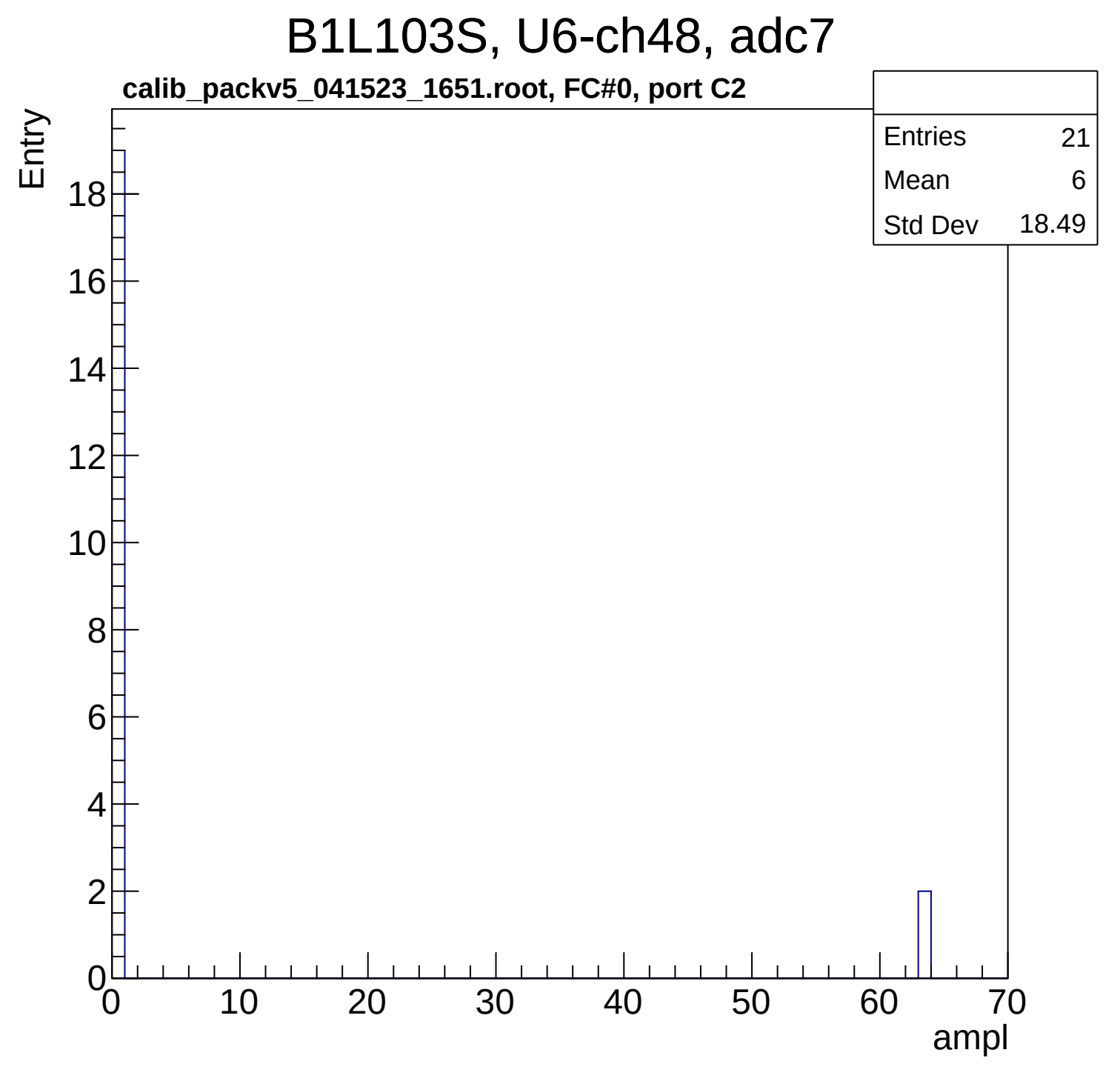
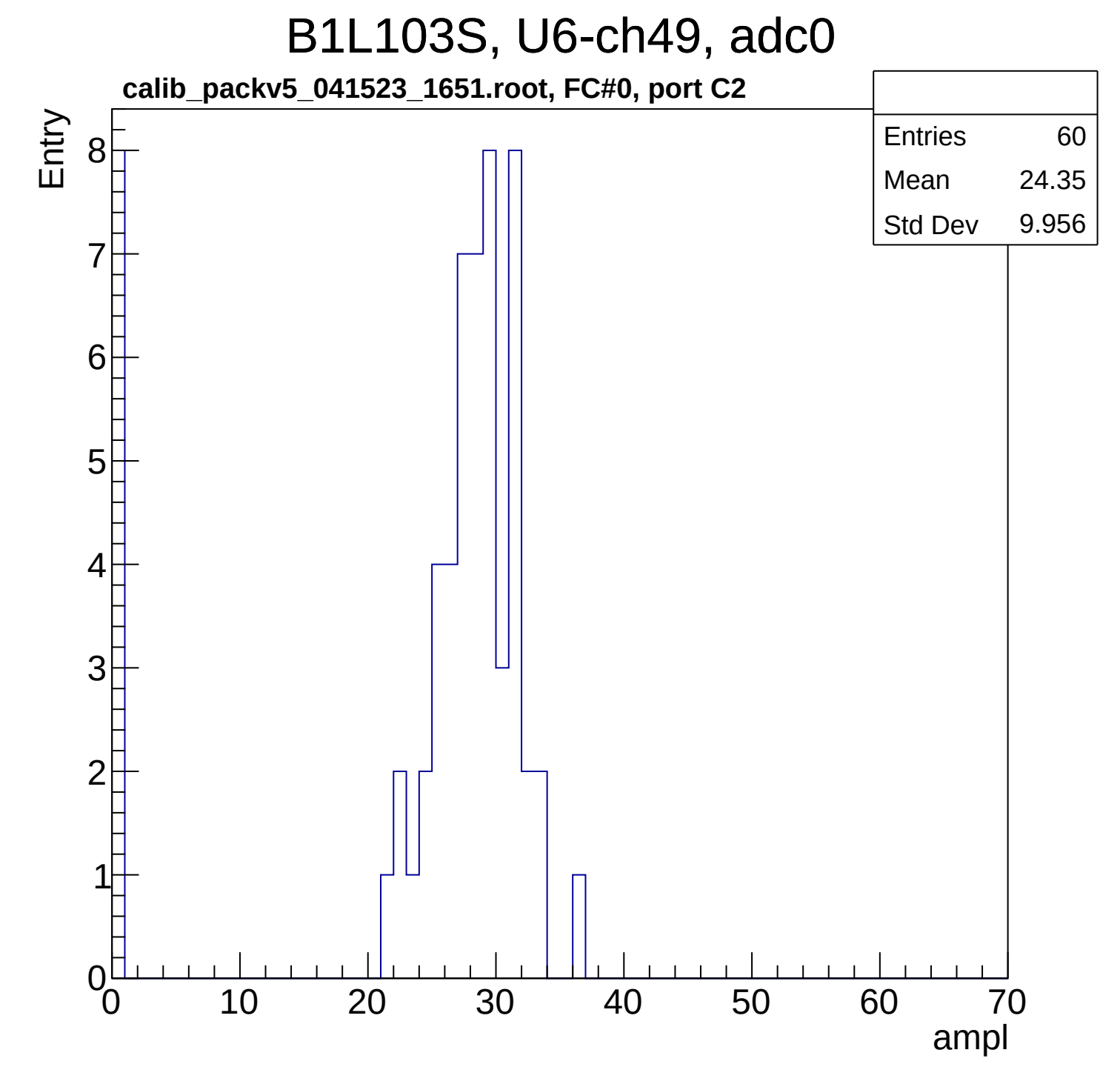
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch48, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 6
Std Dev 18.49
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch49, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 24.35
Std Dev 9.956
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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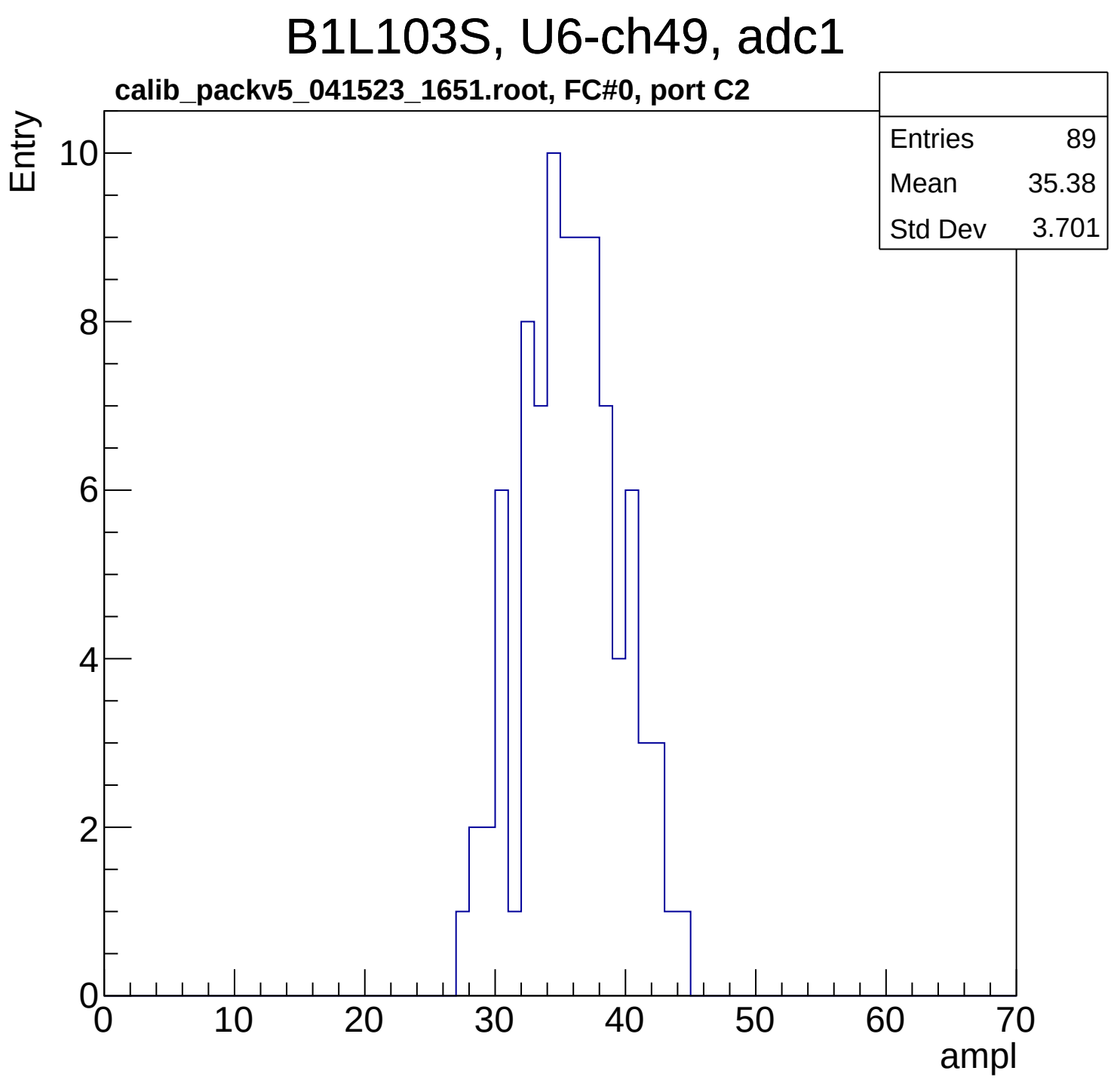
40
50
60
70


B1L103S, U6-ch49, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 35.38
Std Dev 3.701
Entry
ampl
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4
6
8
10
0
10
20
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40
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60
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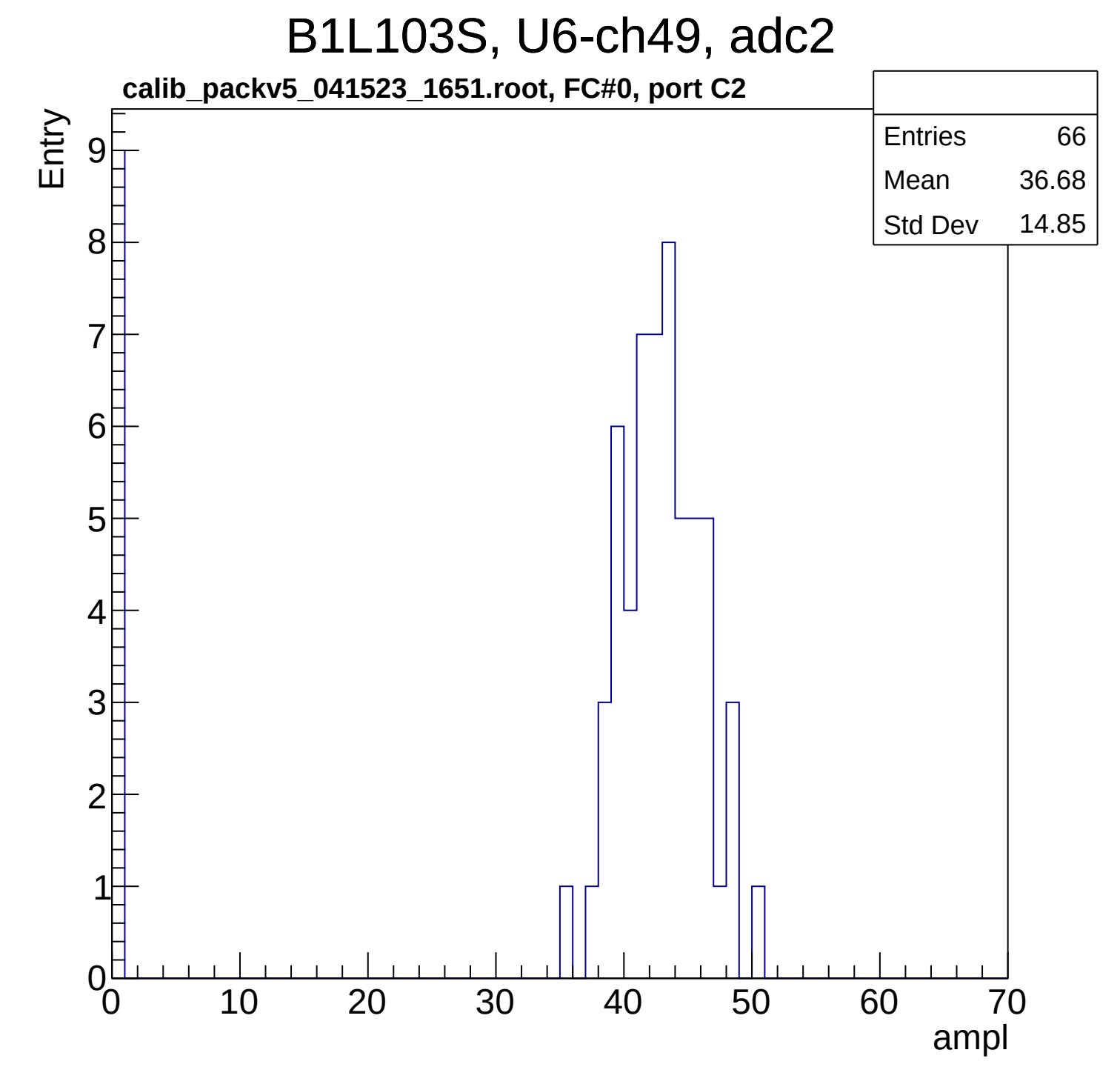
B1L103S, U6-ch49, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 36.68
Std Dev 14.85
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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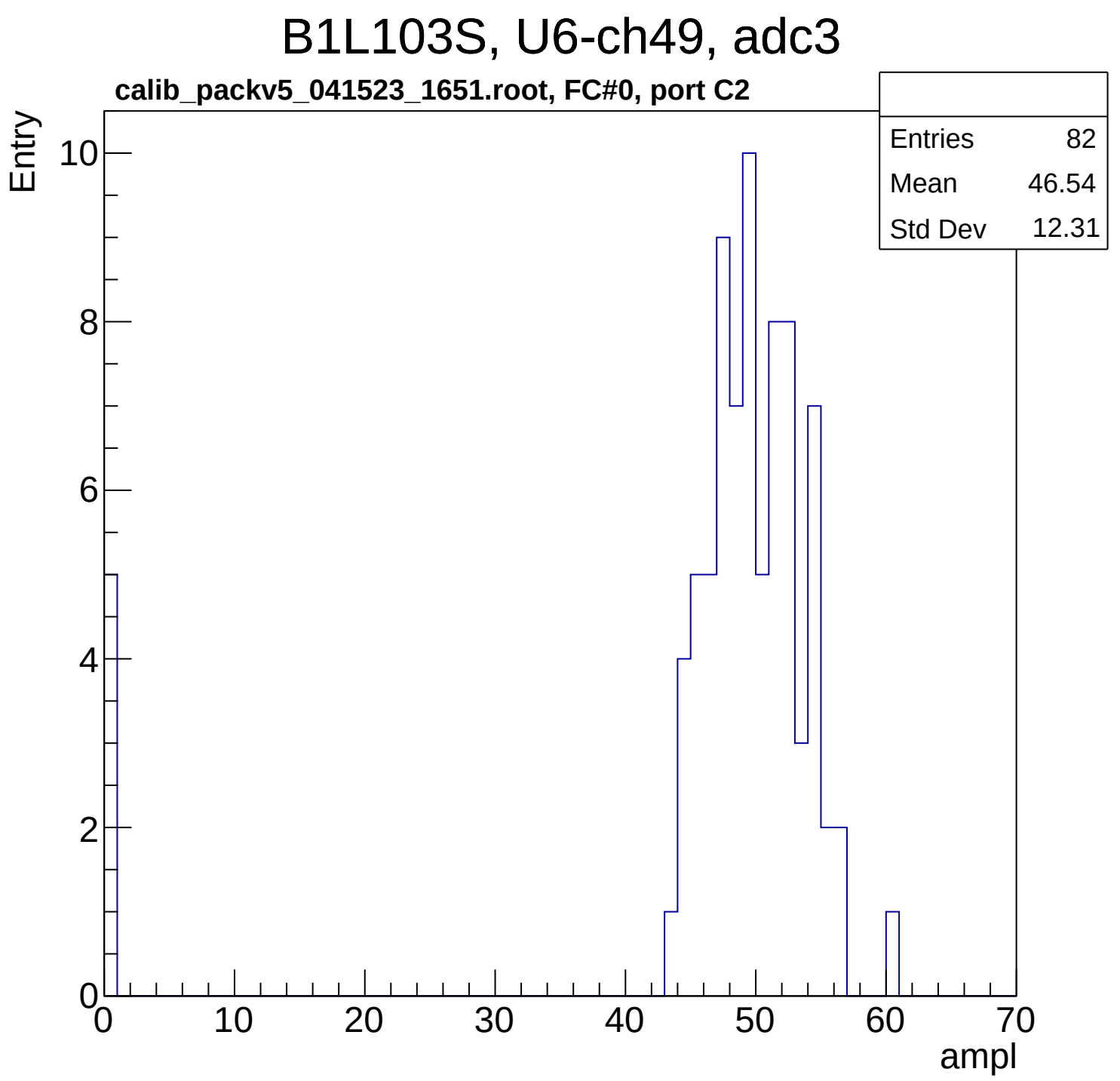
B1L103S, U6-ch49, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 46.54
Std Dev 12.31
Entry
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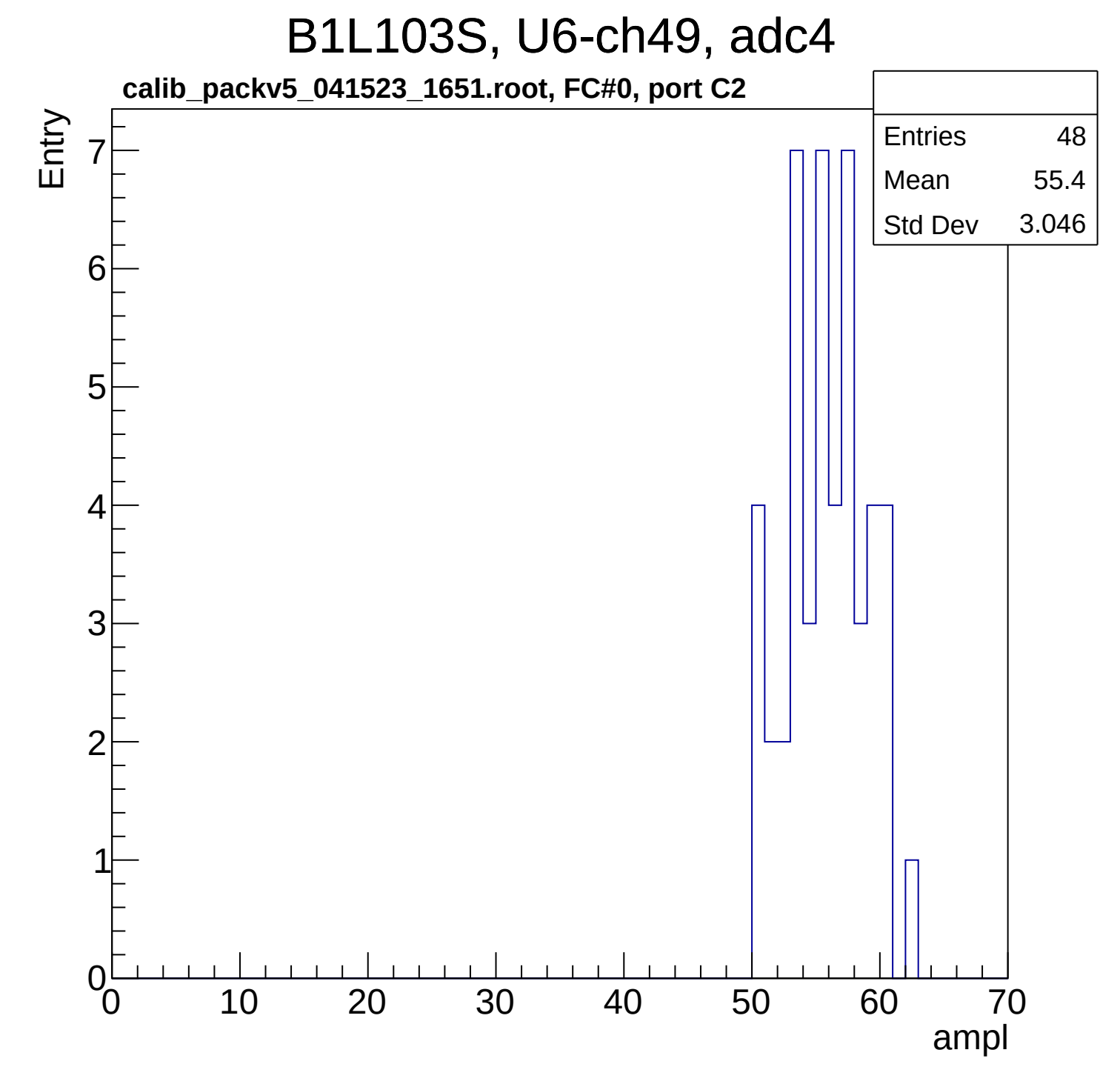
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch49, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 55.4
Std Dev 3.046
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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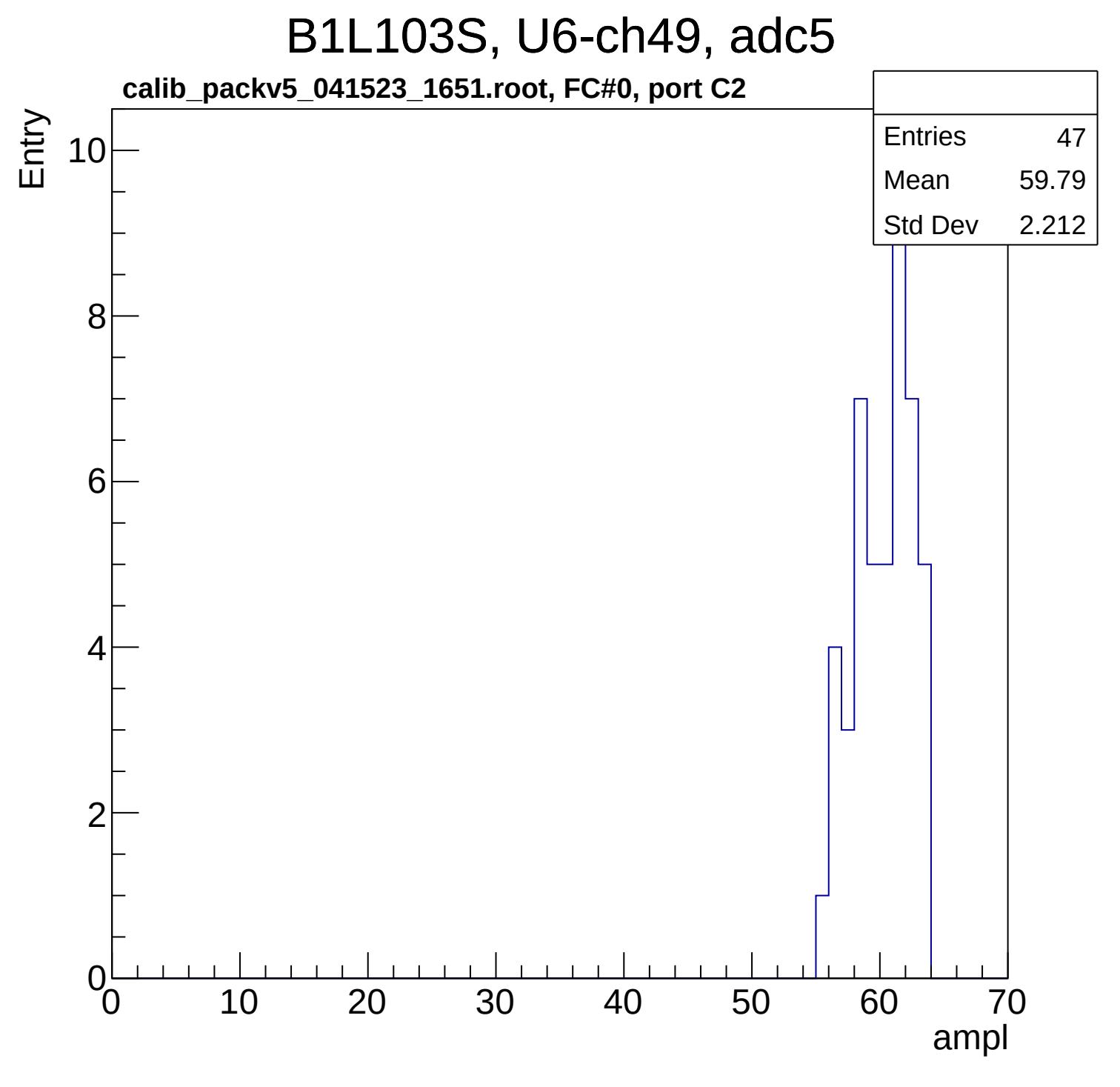
60
70


B1L103S, U6-ch49, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 59.79
Std Dev 2.212
Entry
ampl
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4
6
8
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0
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60
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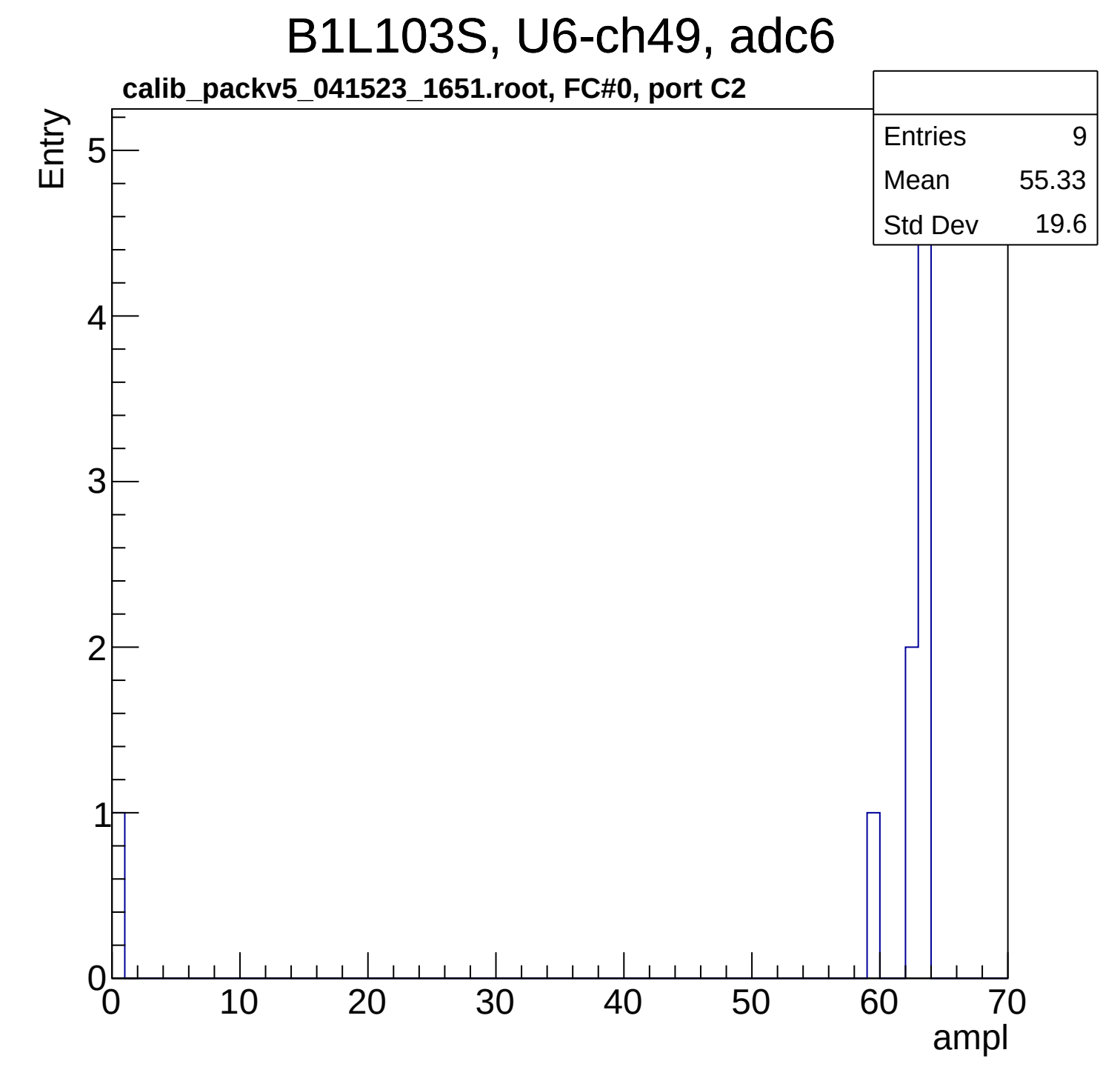
B1L103S, U6-ch49, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 55.33
Std Dev 19.6
Entry
ampl
0
1
2
3
4
5
0
10
20
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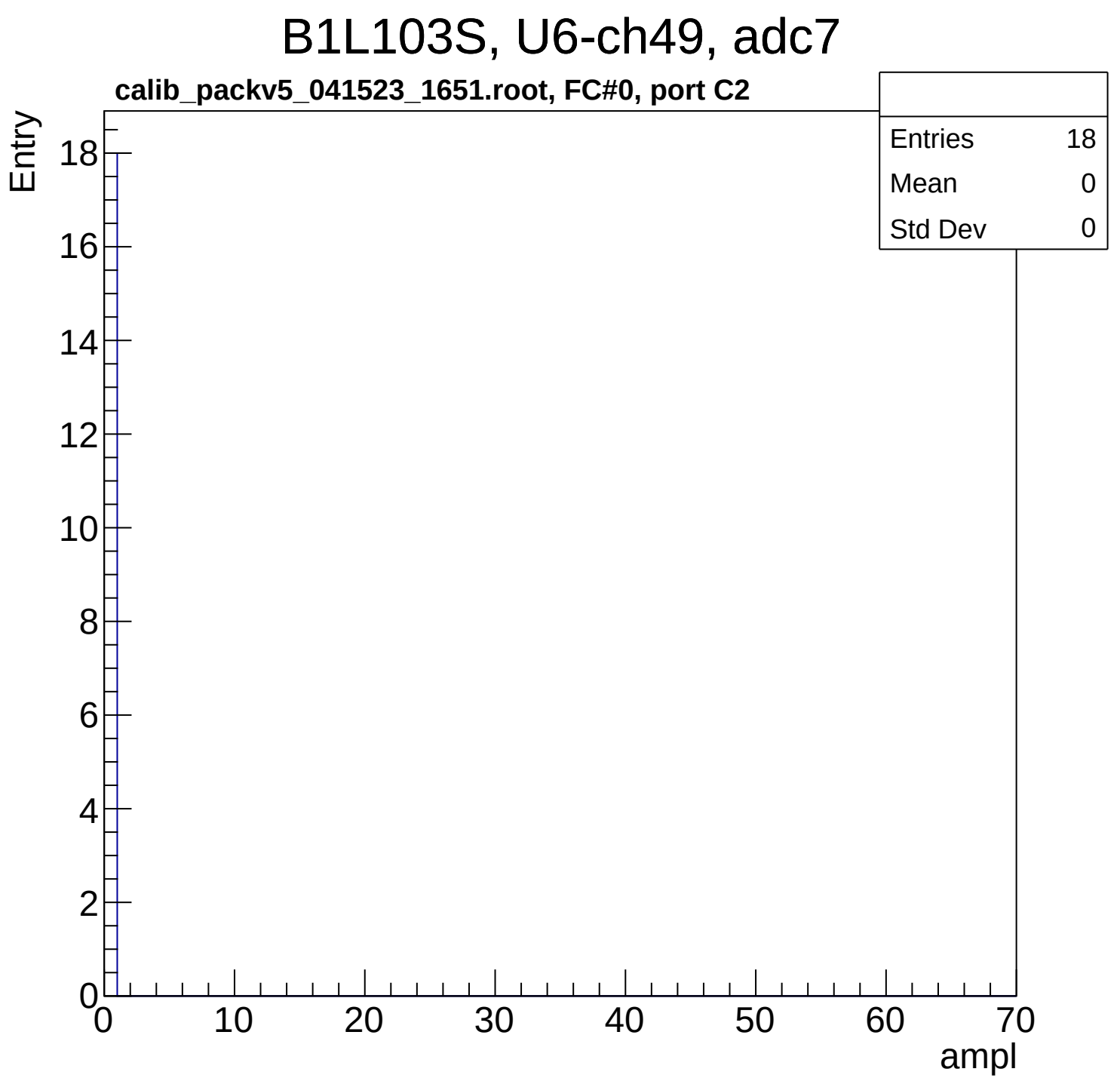
40
50
60
70


B1L103S, U6-ch49, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
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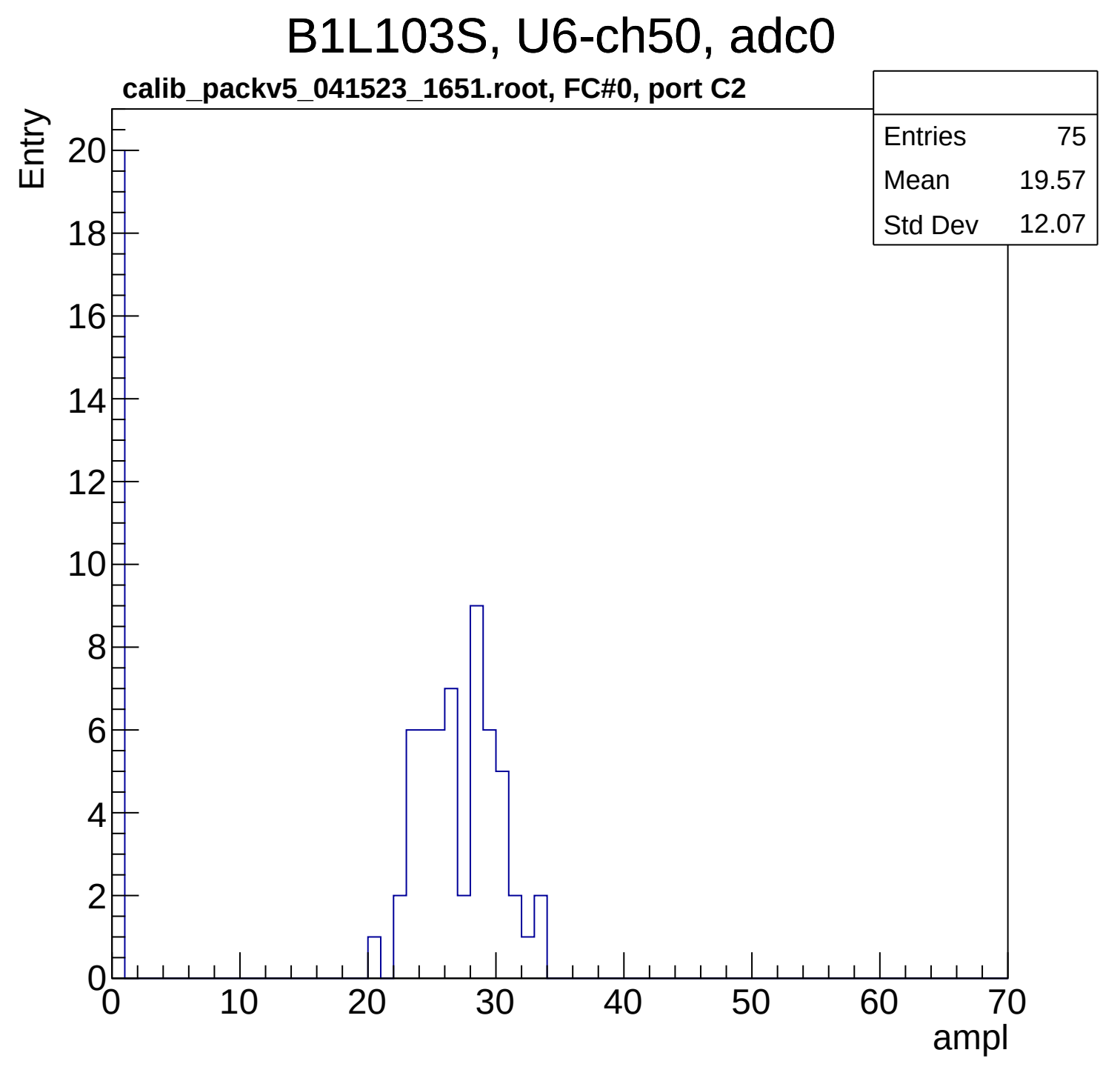
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch50, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 19.57
Std Dev 12.07
Entry
0
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8
10
12
14
16
18
20
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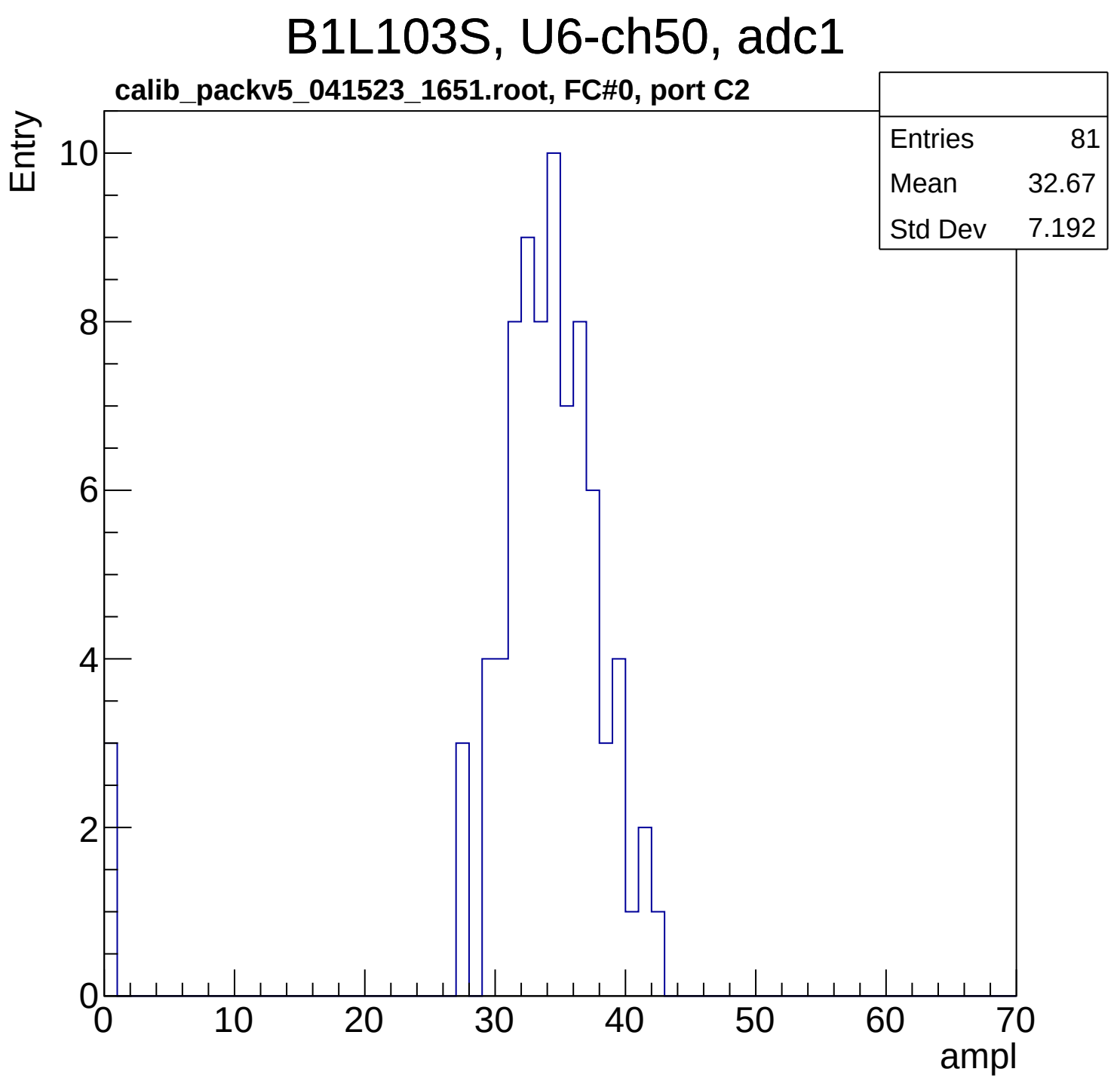
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch50, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 32.67
Std Dev 7.192
Entry
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10
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20
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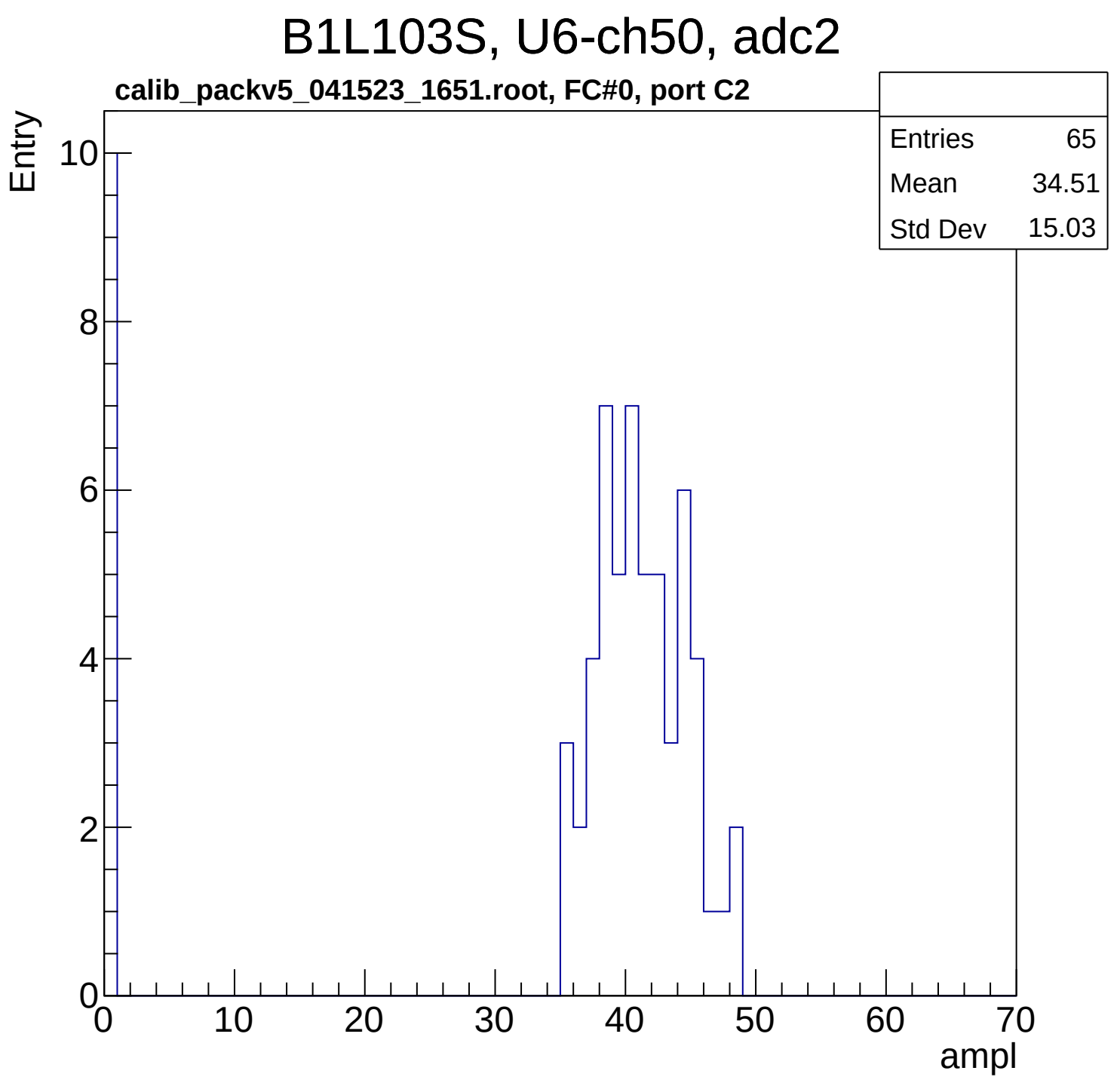
50
60
70
ampl


B1L103S, U6-ch50, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 34.51
Std Dev 15.03
Entry
ampl
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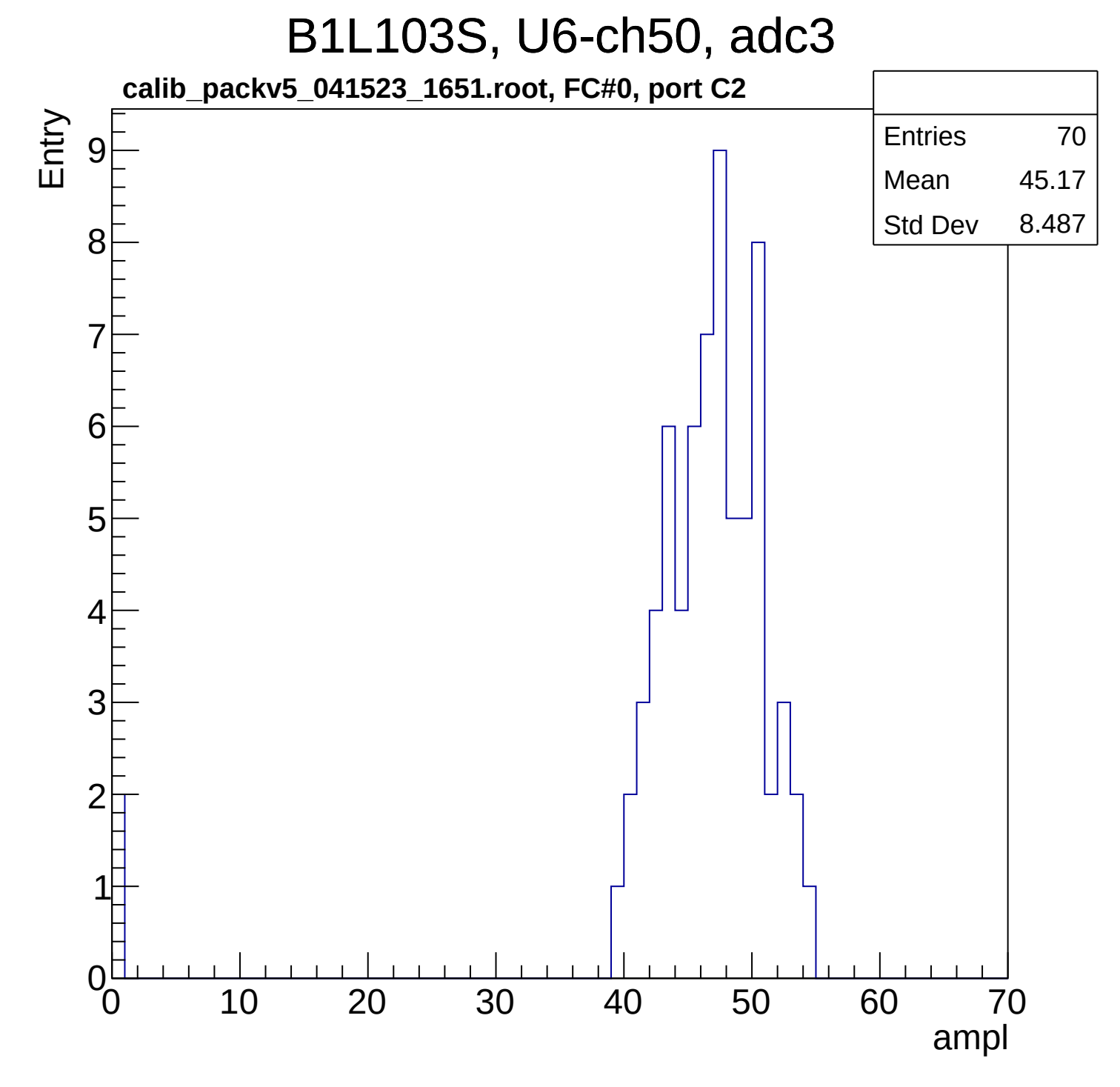
40
50
60
70


B1L103S, U6-ch50, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 45.17
Std Dev 8.487
Entry
ampl
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3
4
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6
7
8
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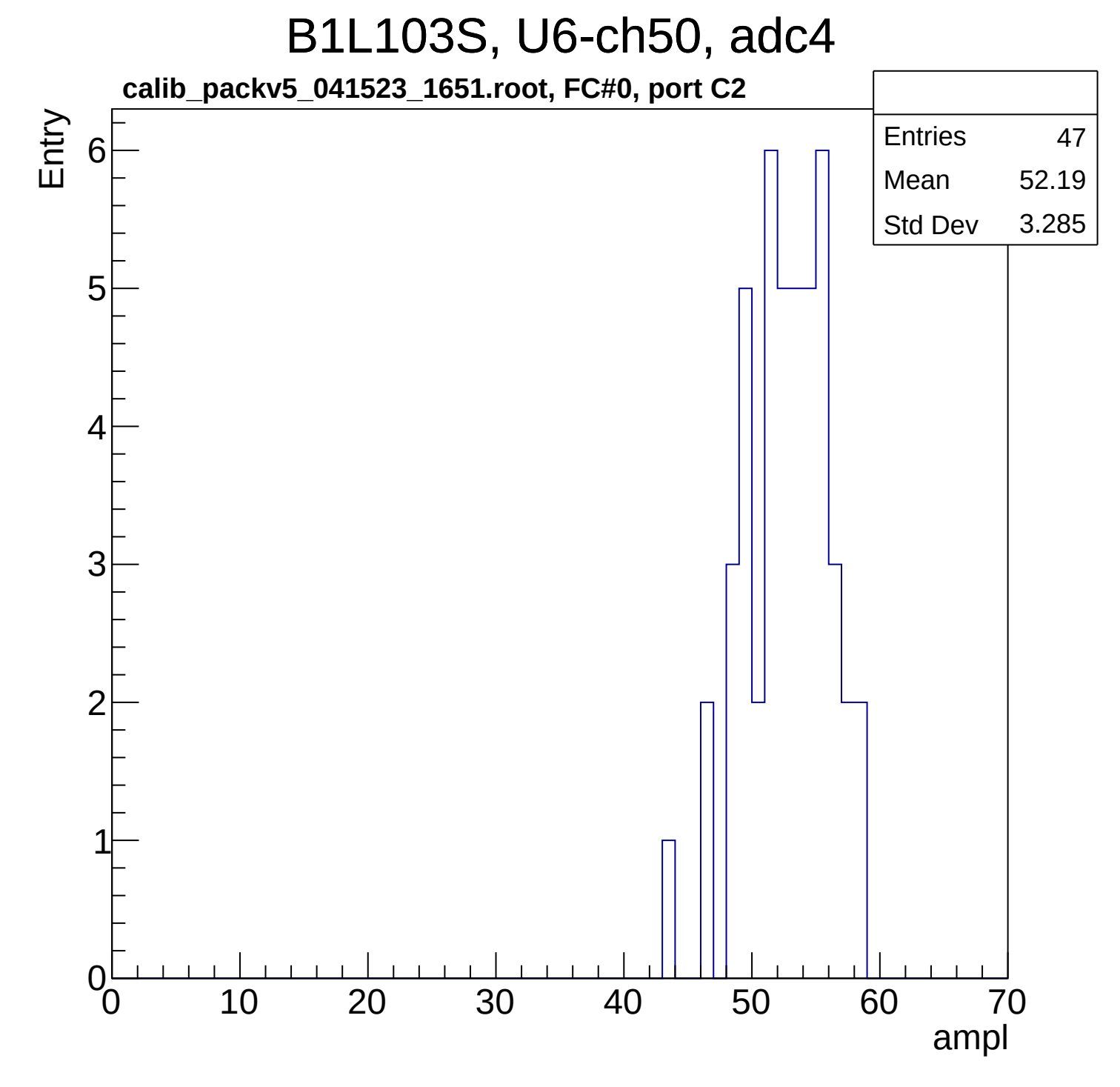
70


B1L103S, U6-ch50, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 52.19
Std Dev 3.285
Entry
ampl
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3
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0
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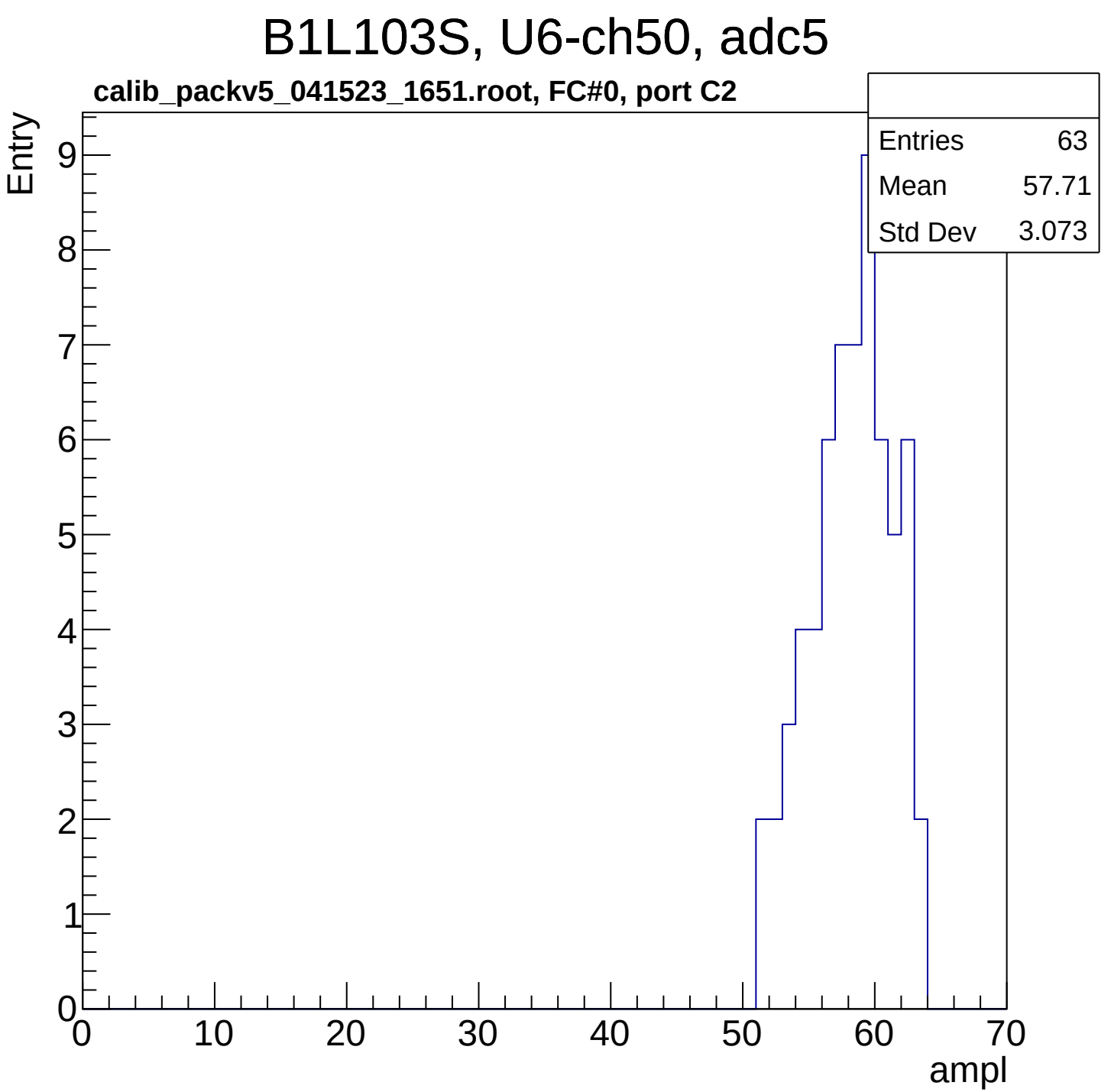
B1L103S, U6-ch50, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 57.71
Std Dev 3.073
Entry
ampl
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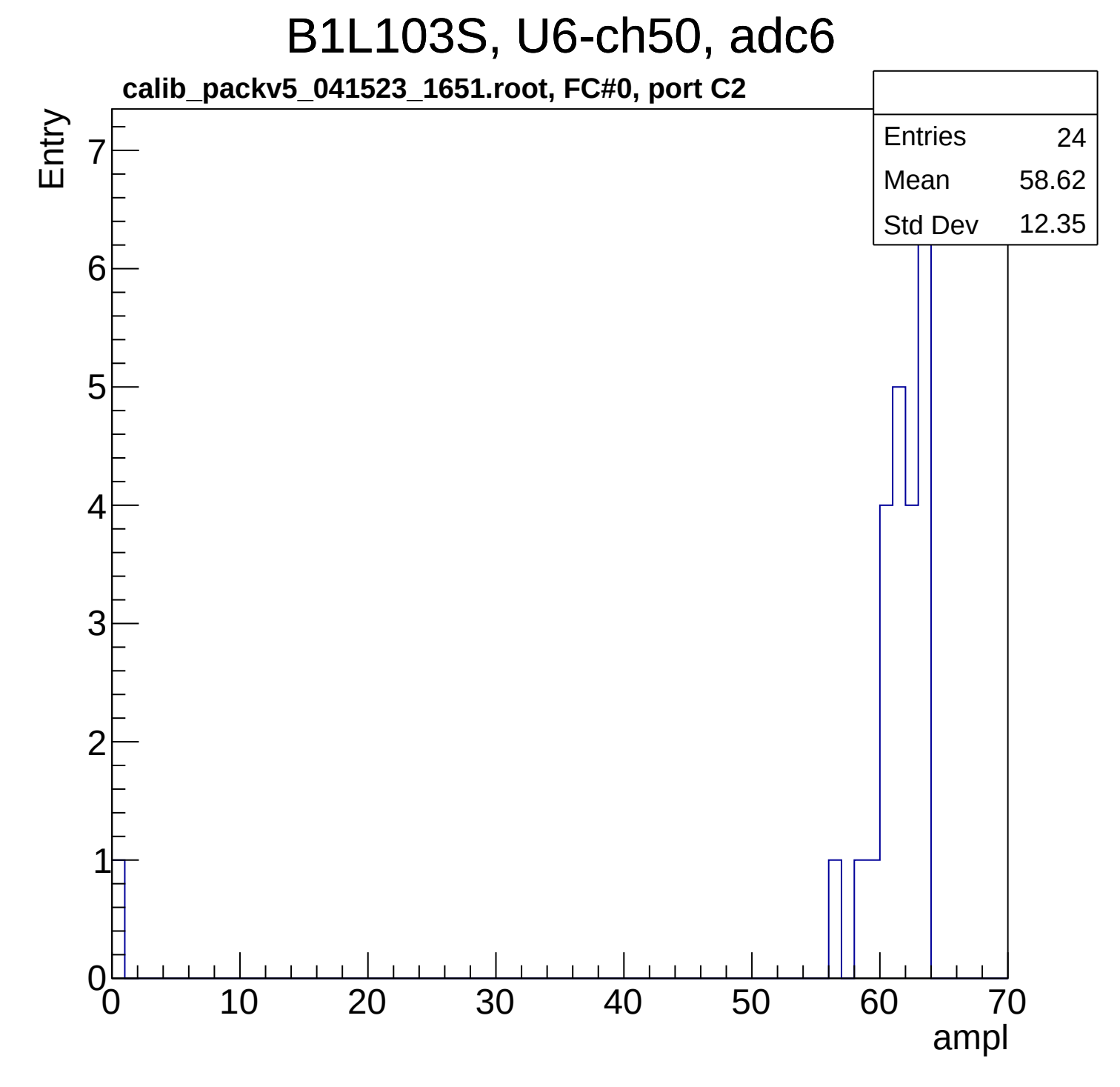
B1L103S, U6-ch50, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 58.62
Std Dev 12.35
Entry
ampl
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2
3
4
5
6
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0
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40
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60
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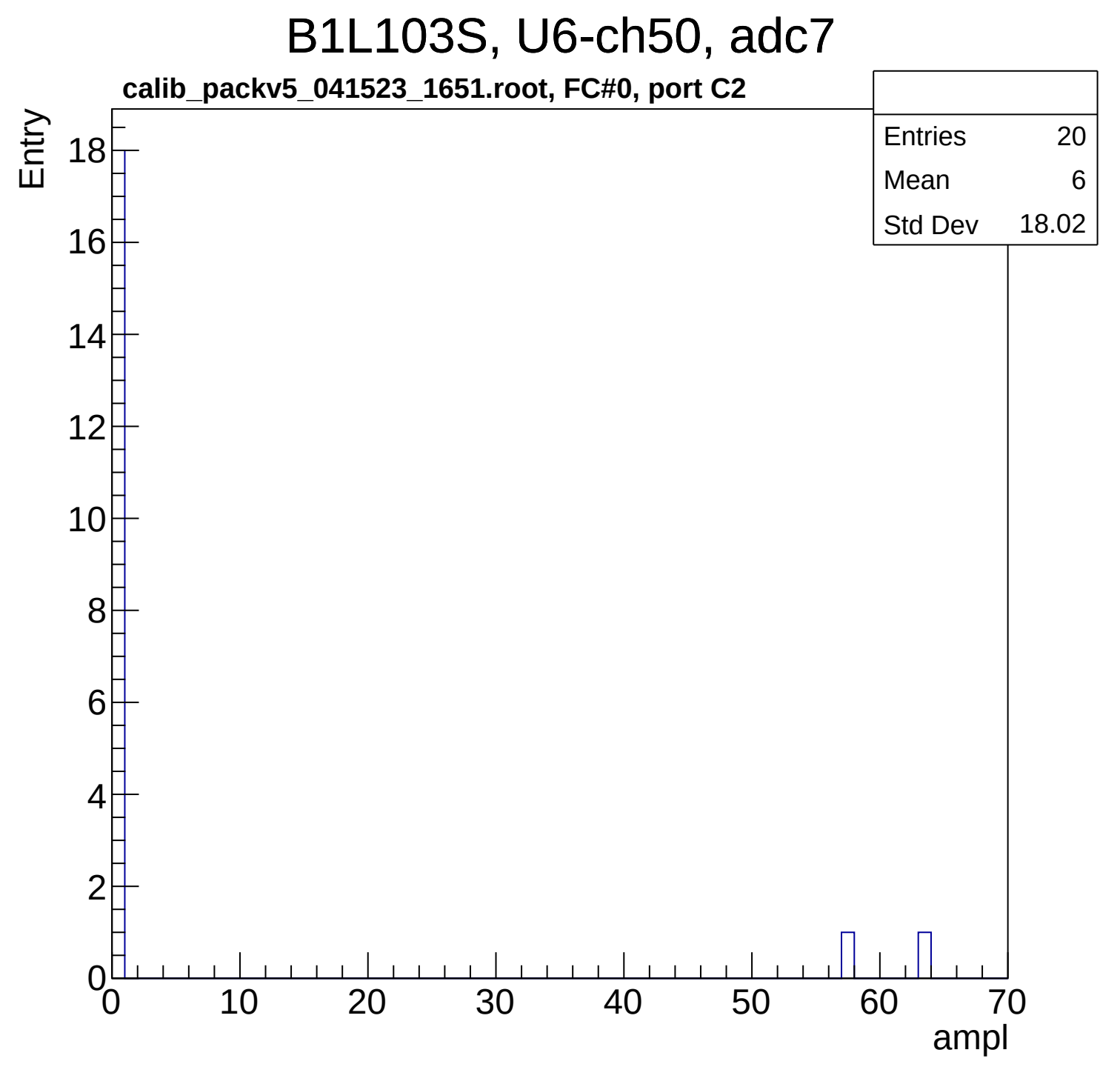
B1L103S, U6-ch50, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 6
Std Dev 18.02
Entry
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6
8
10
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14
16
18
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50
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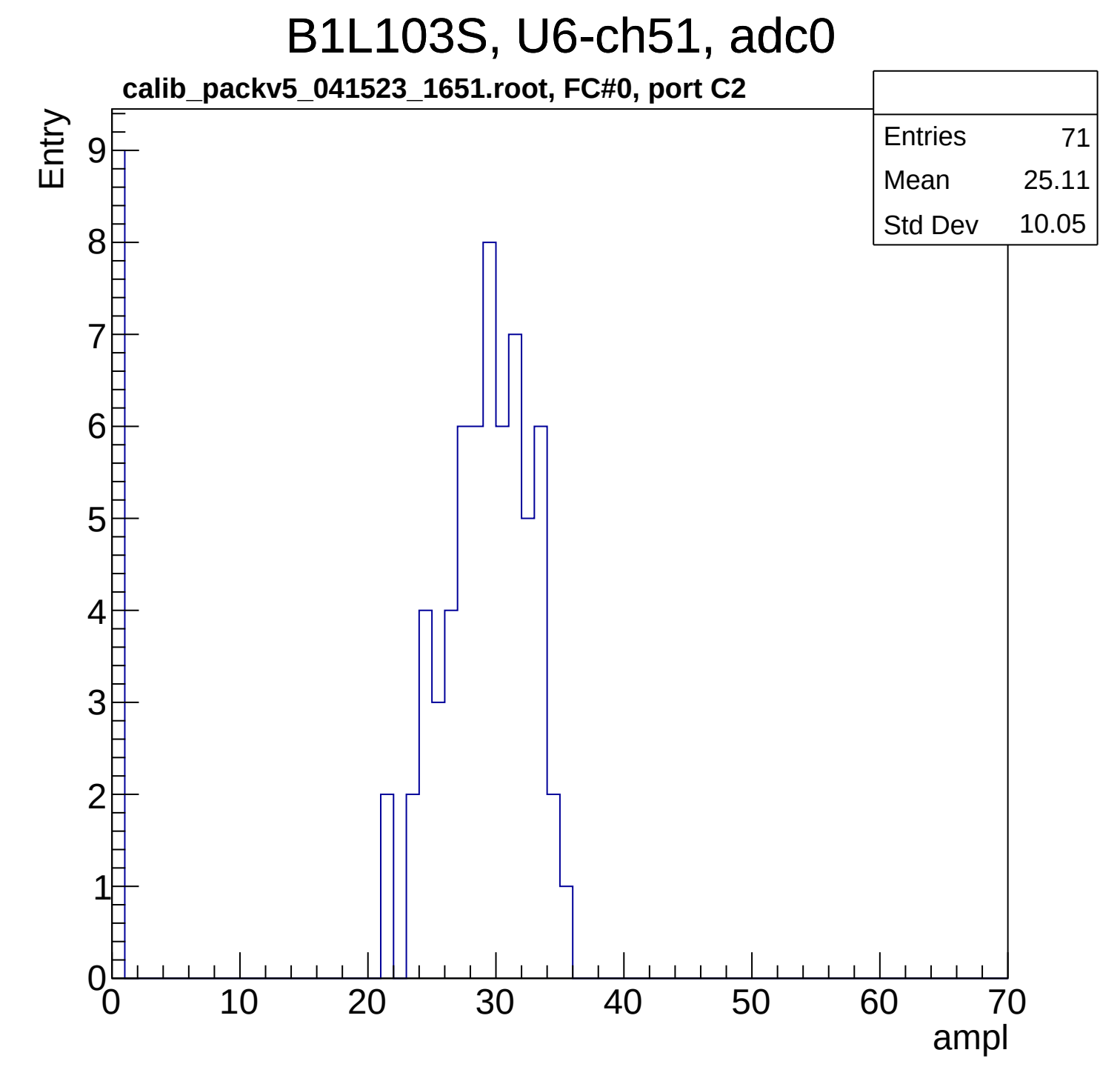
70
ampl


B1L103S, U6-ch51, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 25.11
Std Dev 10.05
Entry
ampl
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2
3
4
5
6
7
8
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0
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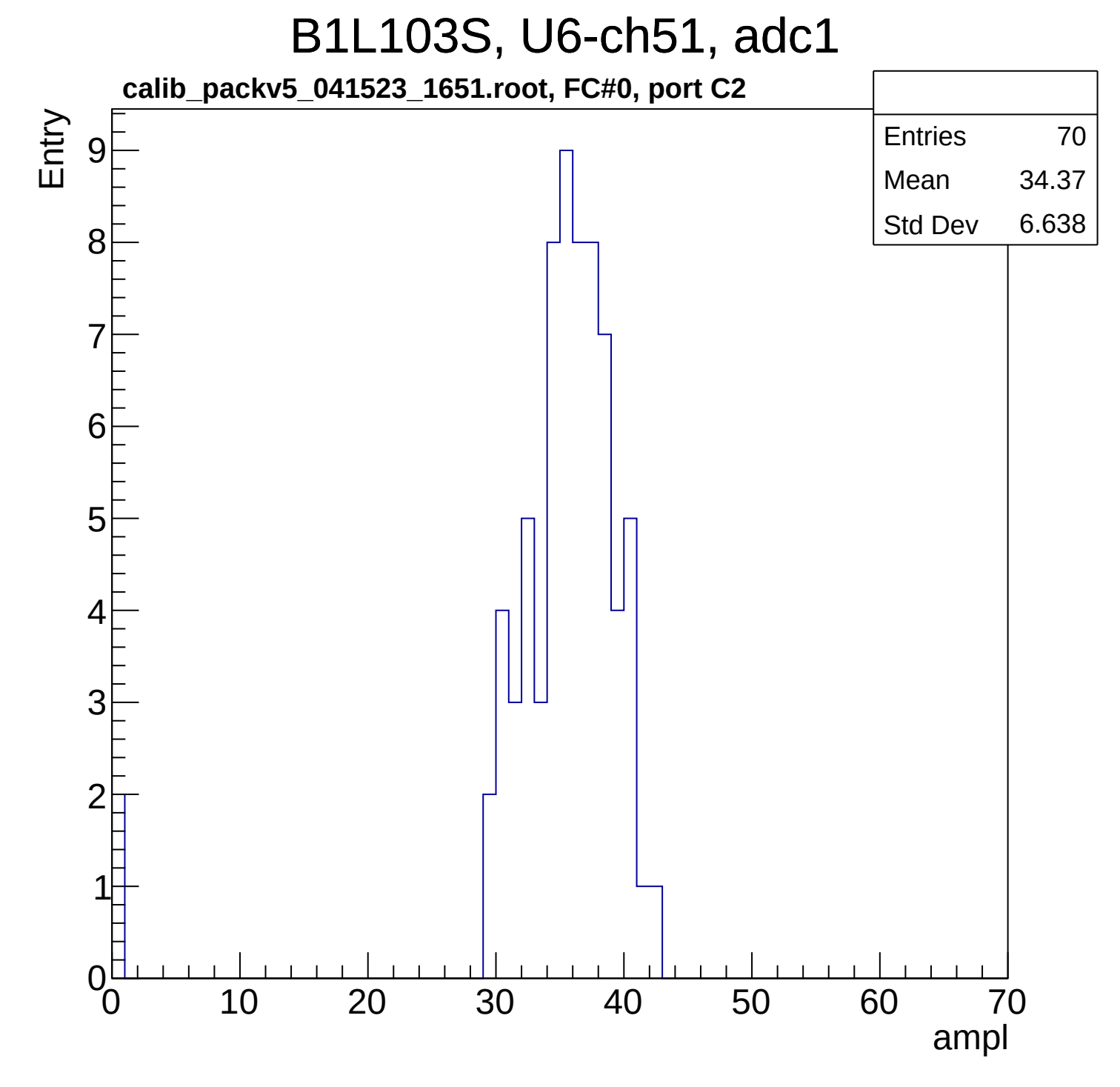
B1L103S, U6-ch51, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 34.37
Std Dev 6.638
Entry
ampl
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2
3
4
5
6
7
8
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0
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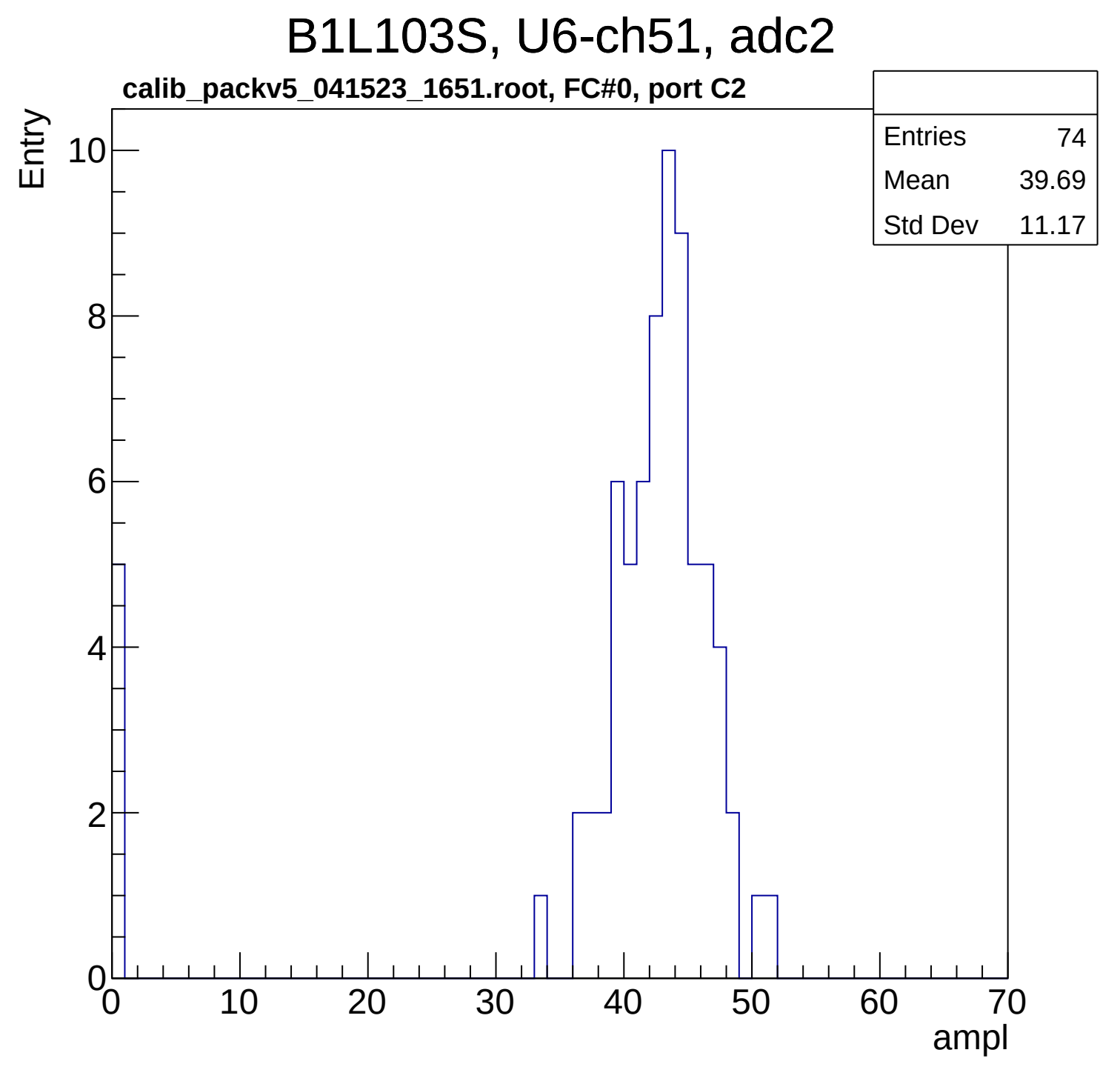
B1L103S, U6-ch51, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 39.69
Std Dev 11.17
Entry
ampl
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4
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8
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0
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60
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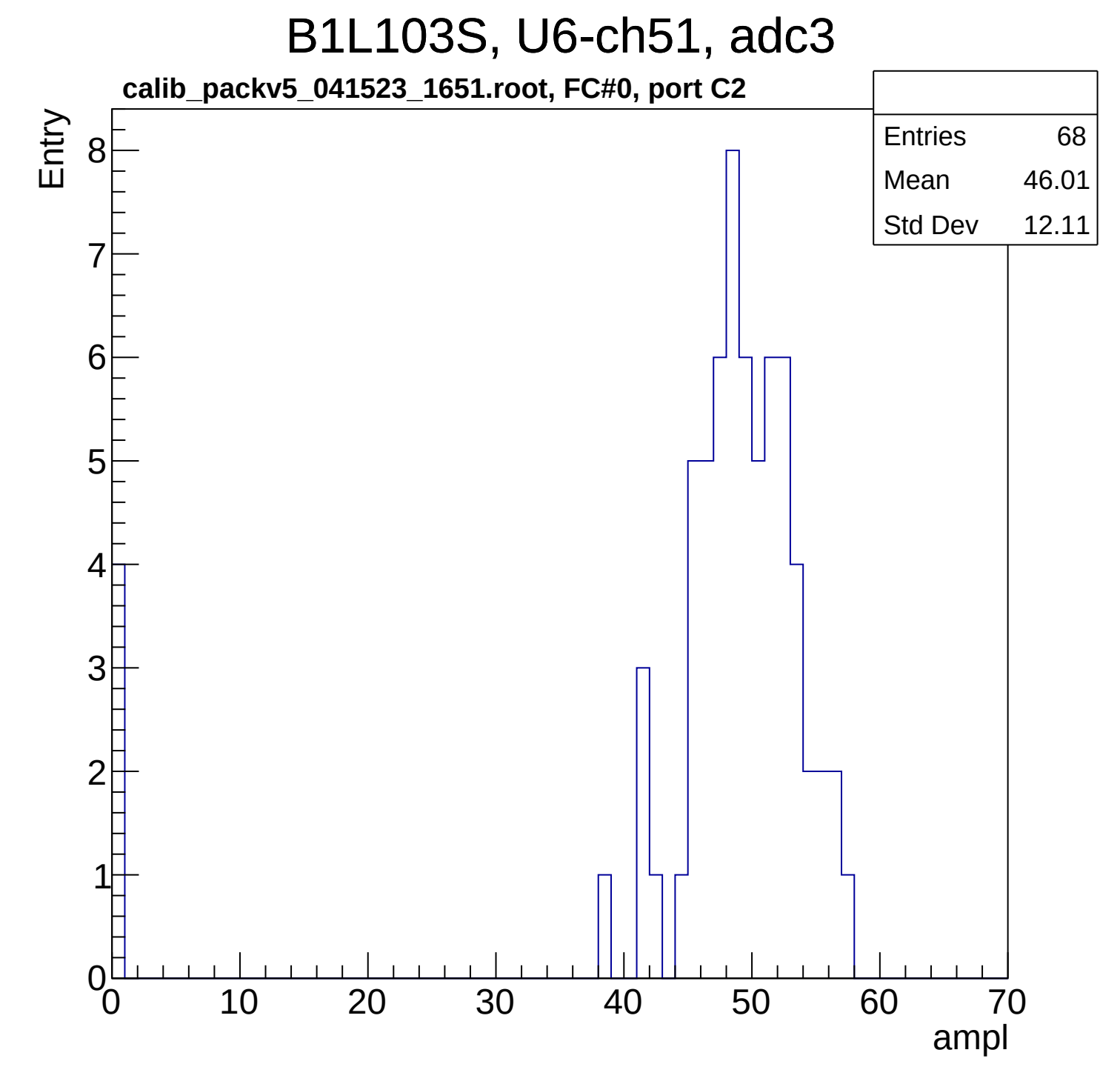
B1L103S, U6-ch51, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 46.01
Std Dev 12.11
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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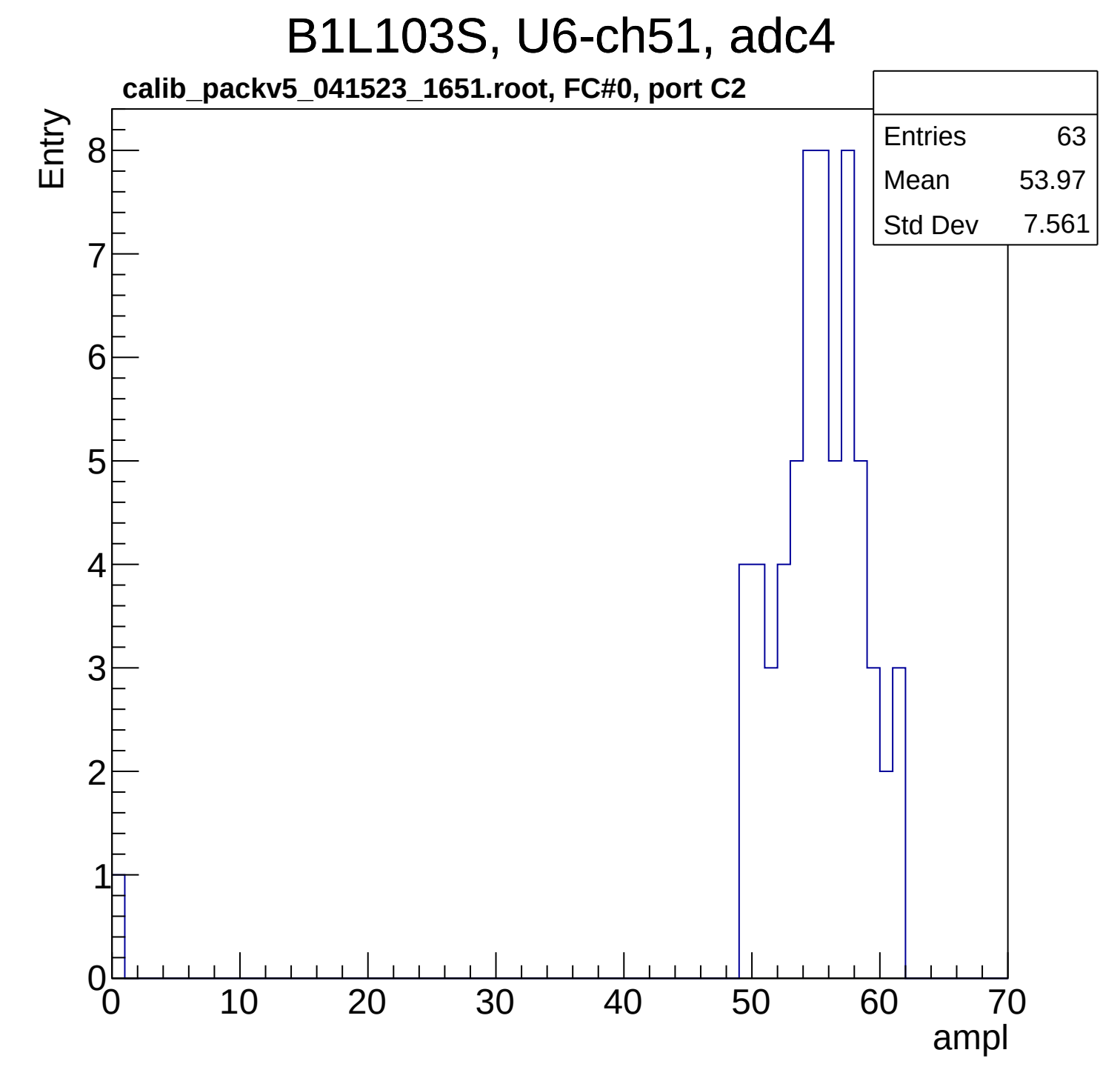
B1L103S, U6-ch51, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 53.97
Std Dev 7.561
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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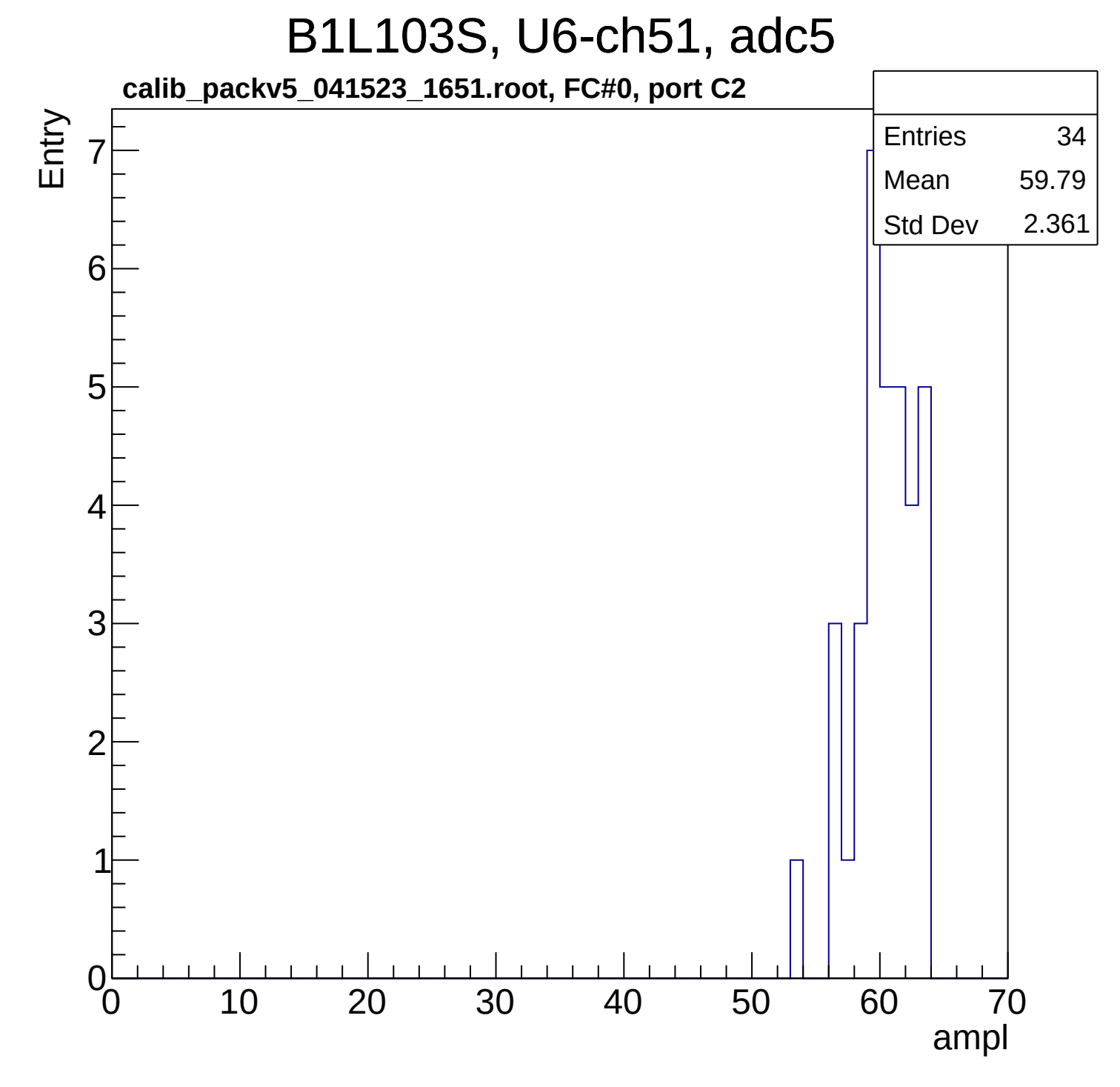
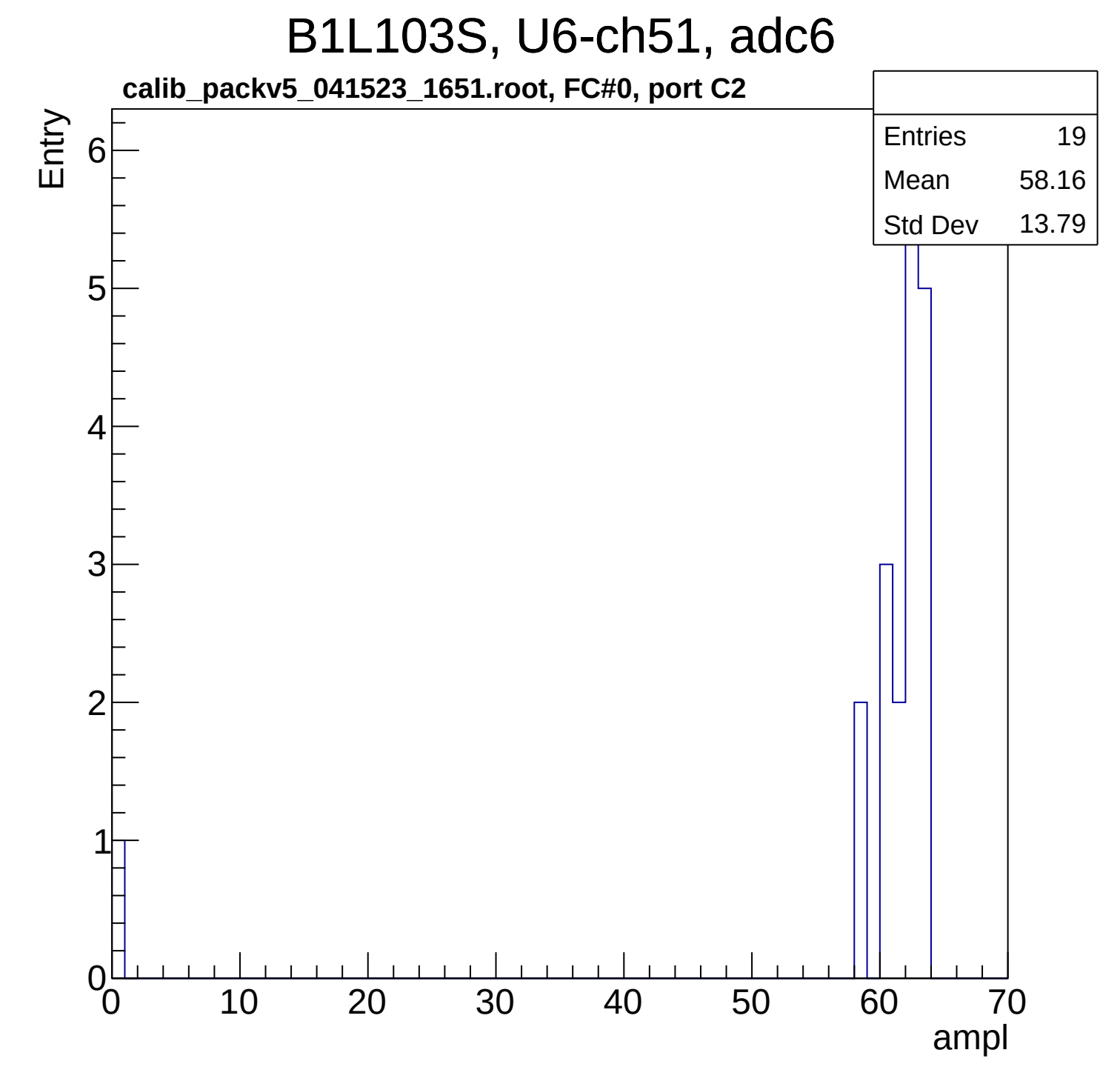
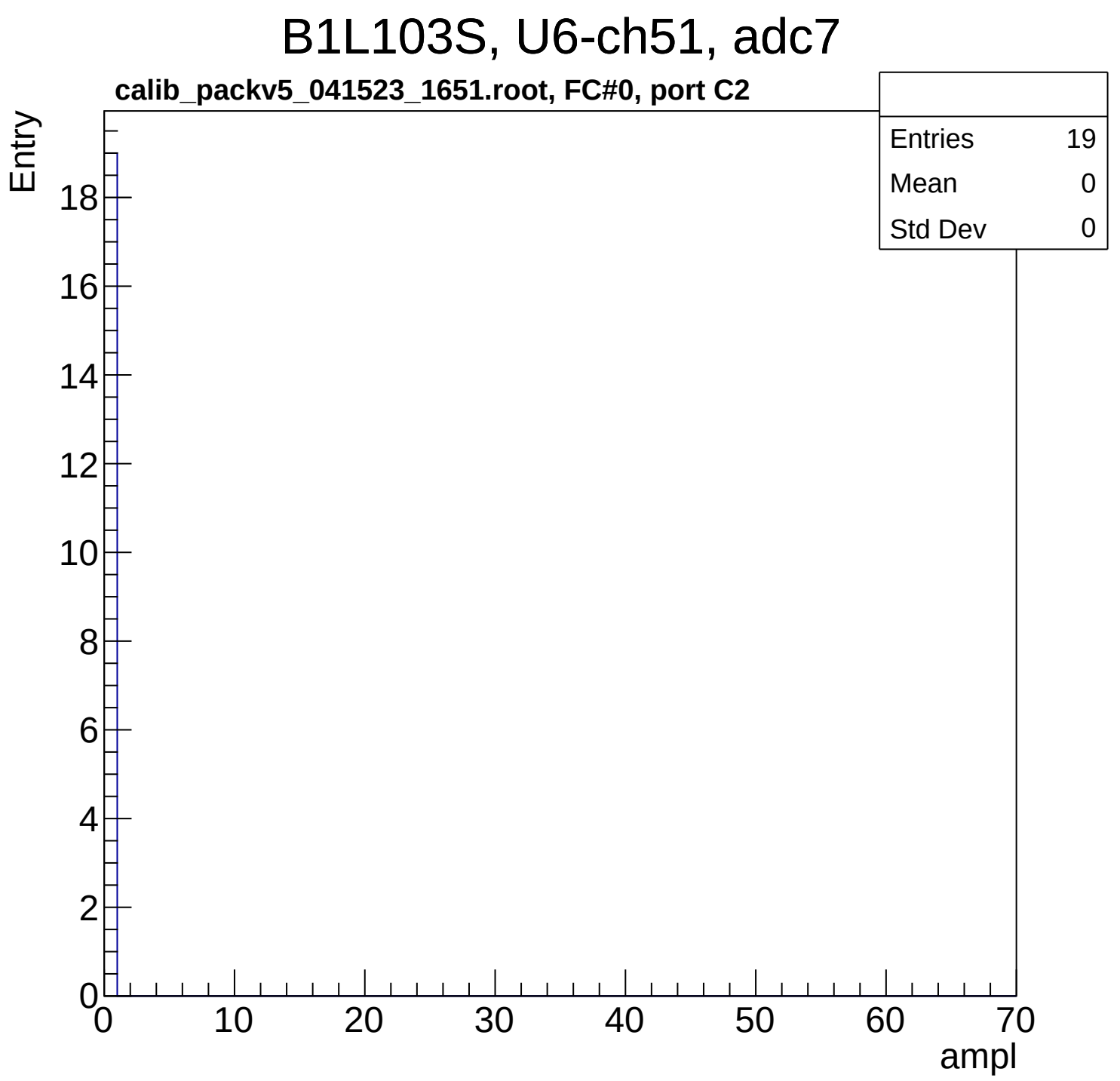
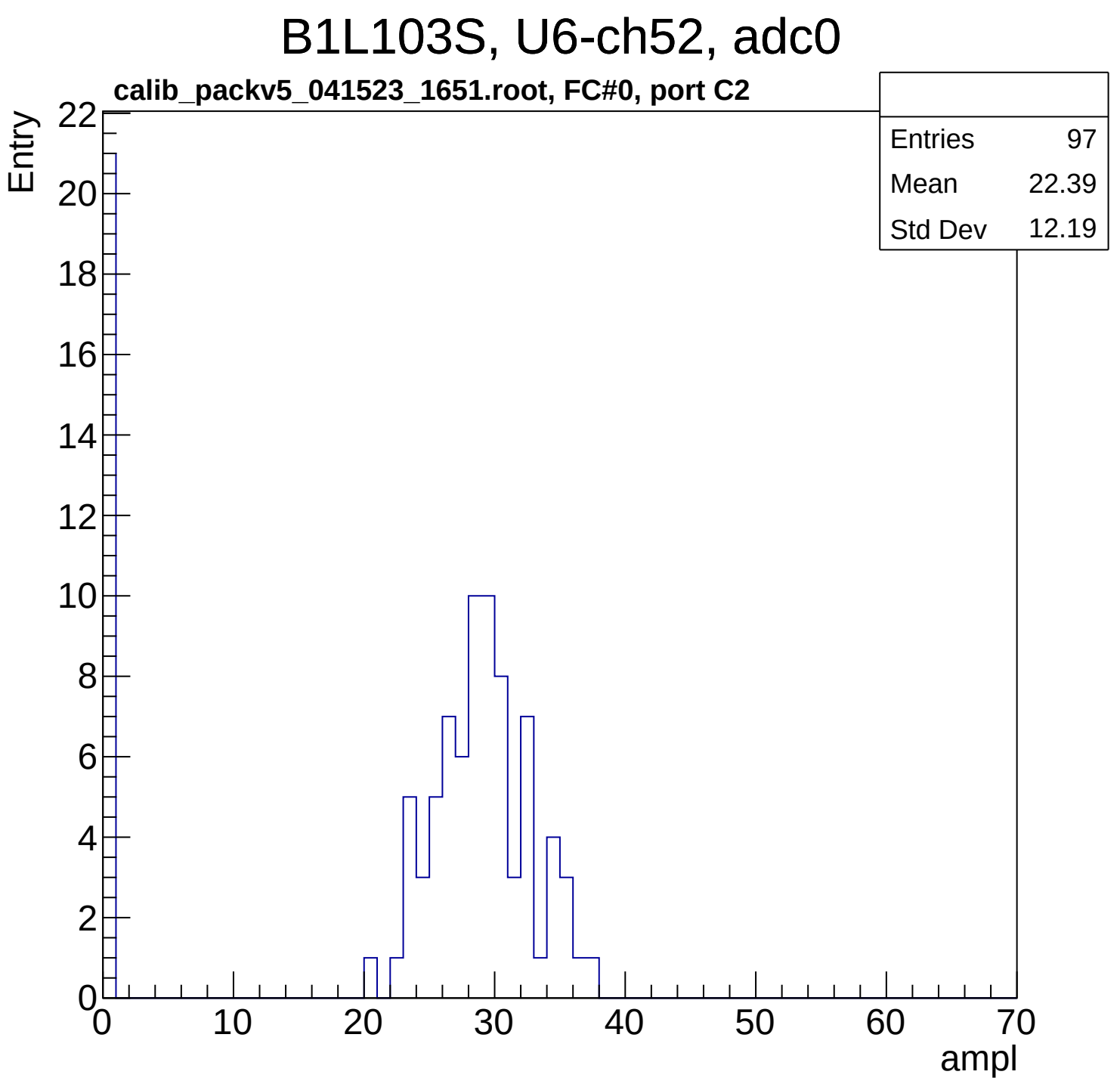
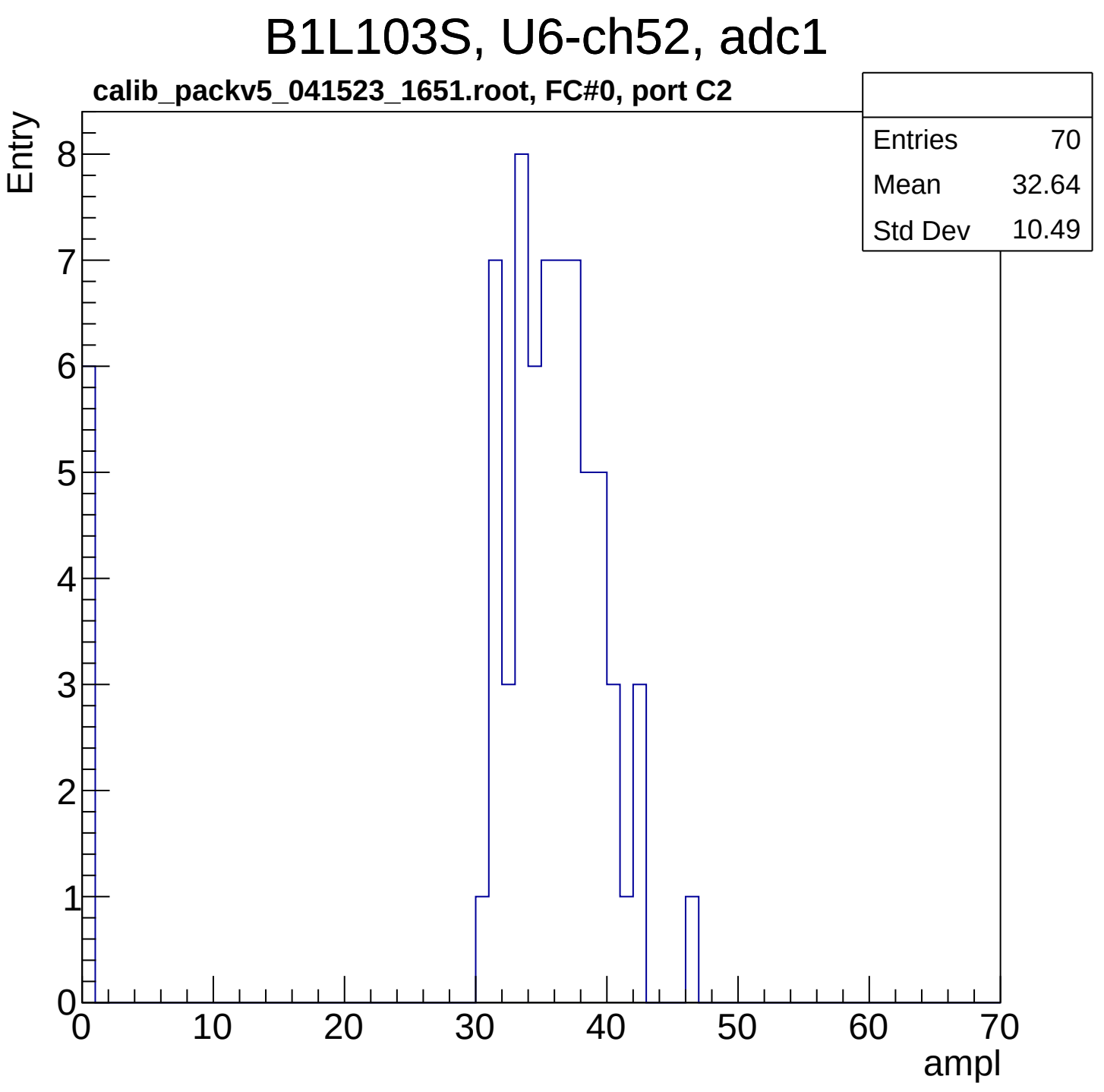

B1L103S, U6-ch51, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 59.79
Std Dev 2.361
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U6-ch51, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 58.16
Std Dev 13.79
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch51, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch52, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 22.39
Std Dev 12.19
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70


B1L103S, U6-ch52, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 32.64
Std Dev 10.49
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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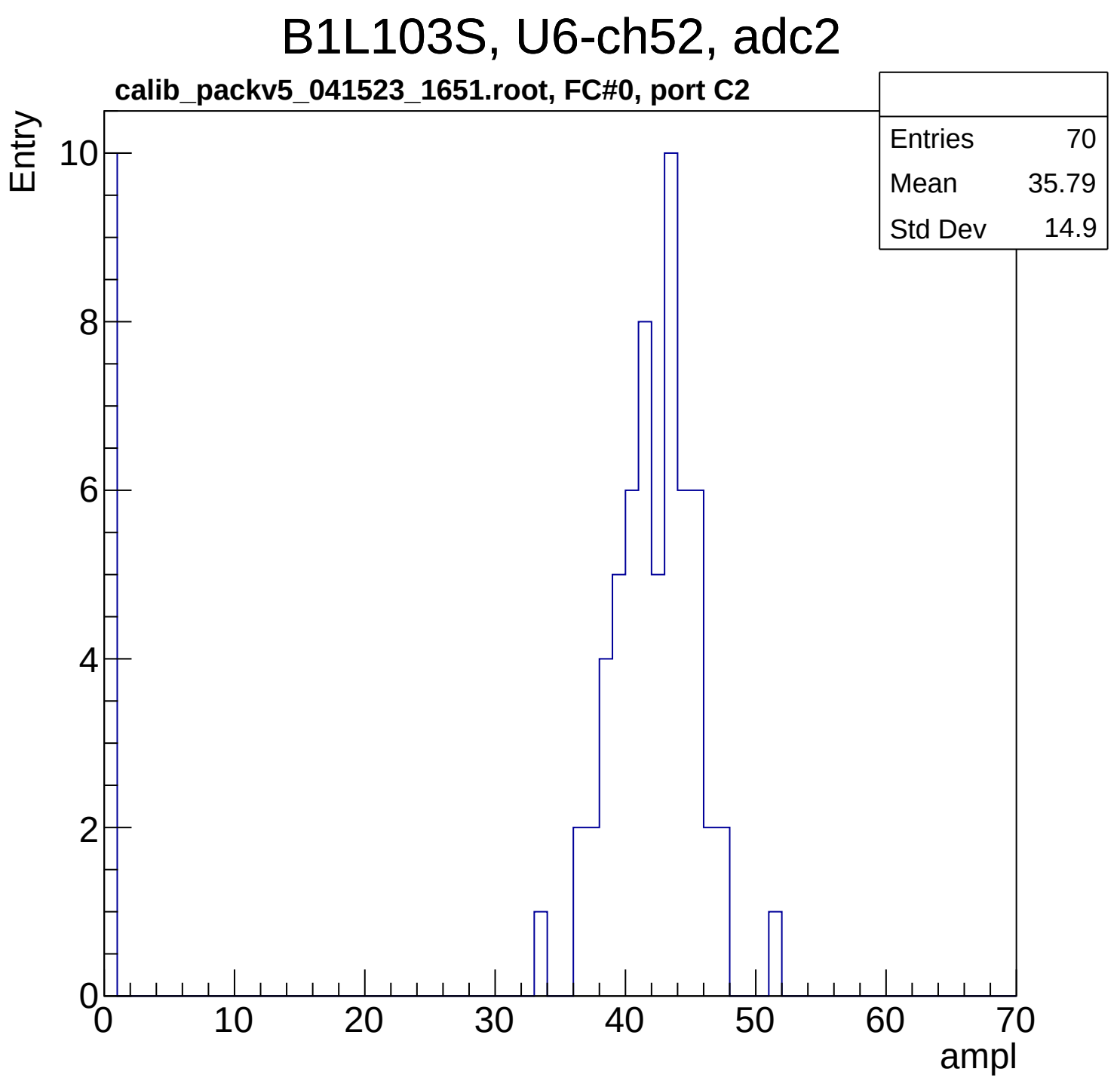
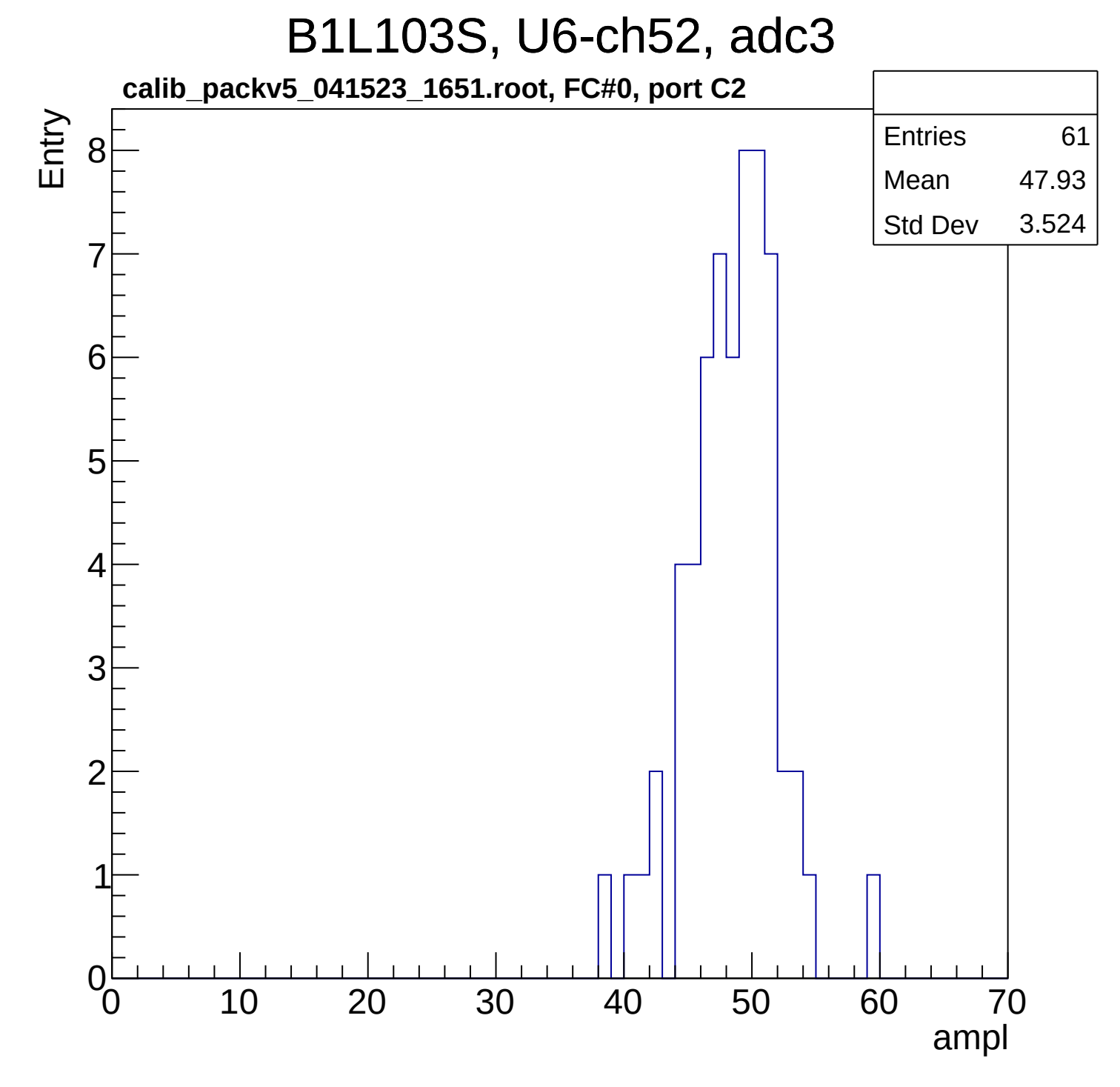

B1L103S, U6-ch52, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 35.79
Std Dev 14.9
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U6-ch52, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 47.93
Std Dev 3.524
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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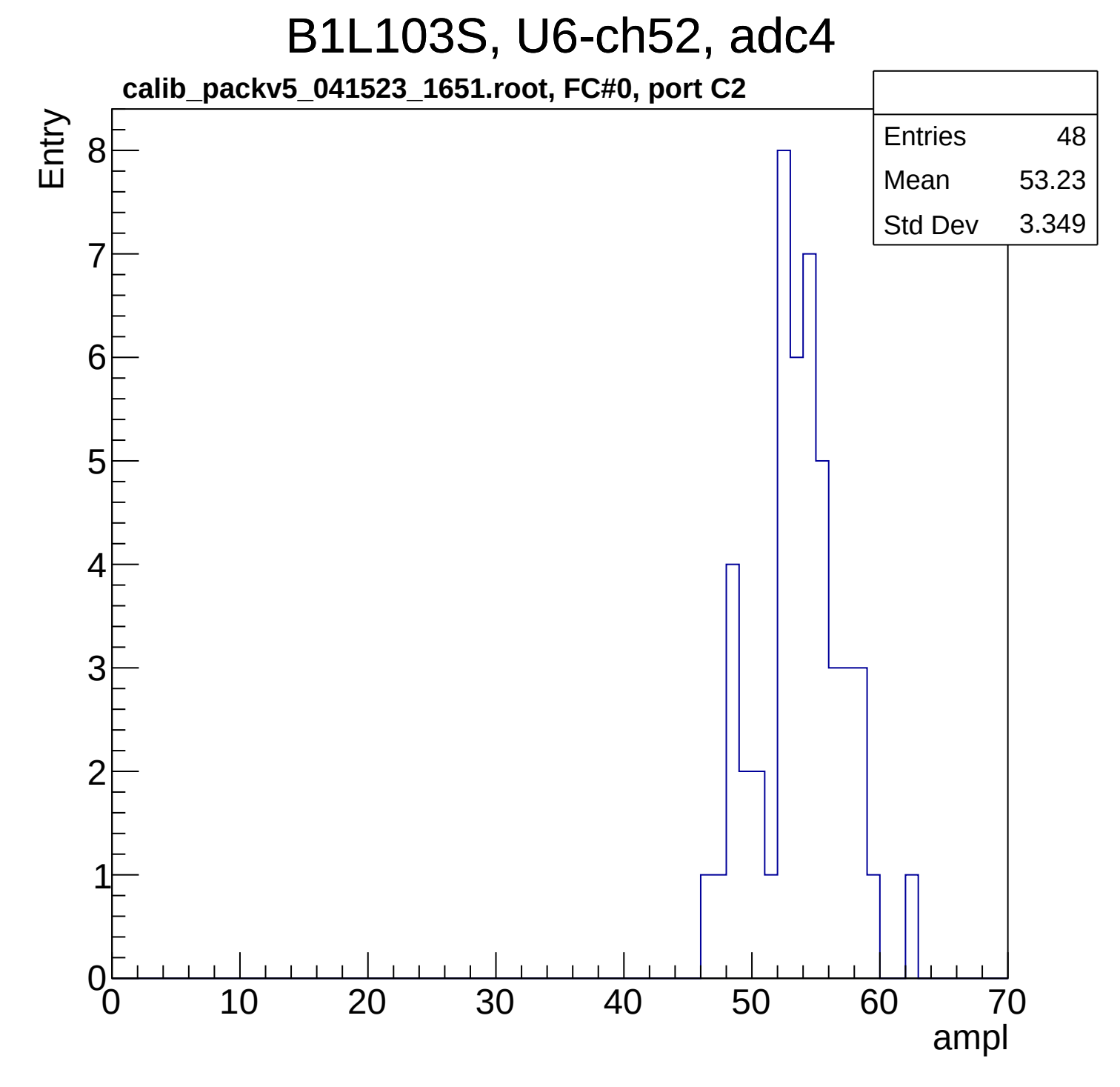
B1L103S, U6-ch52, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 53.23
Std Dev 3.349
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
50
60
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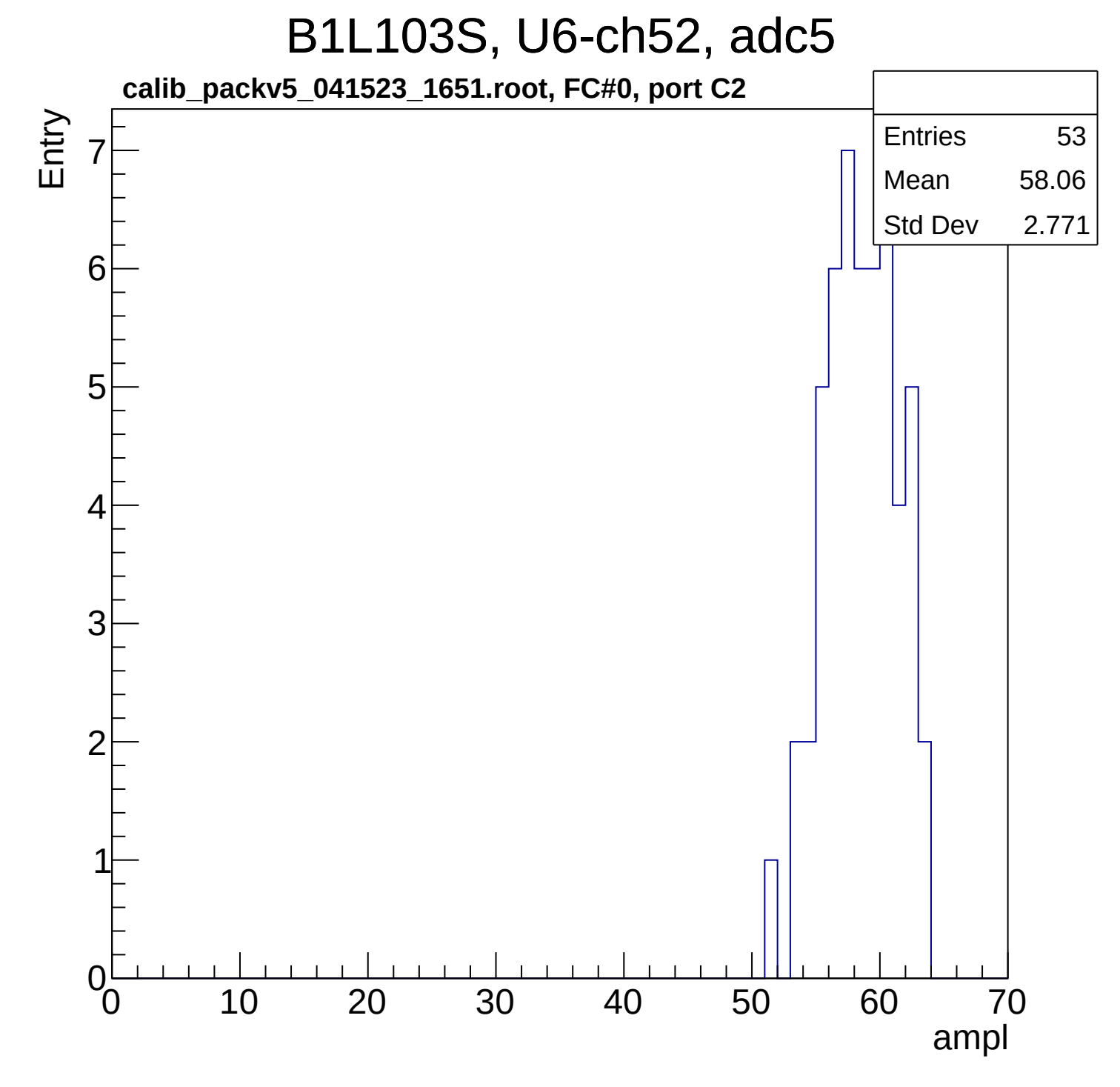
B1L103S, U6-ch52, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 58.06
Std Dev 2.771
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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40
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60
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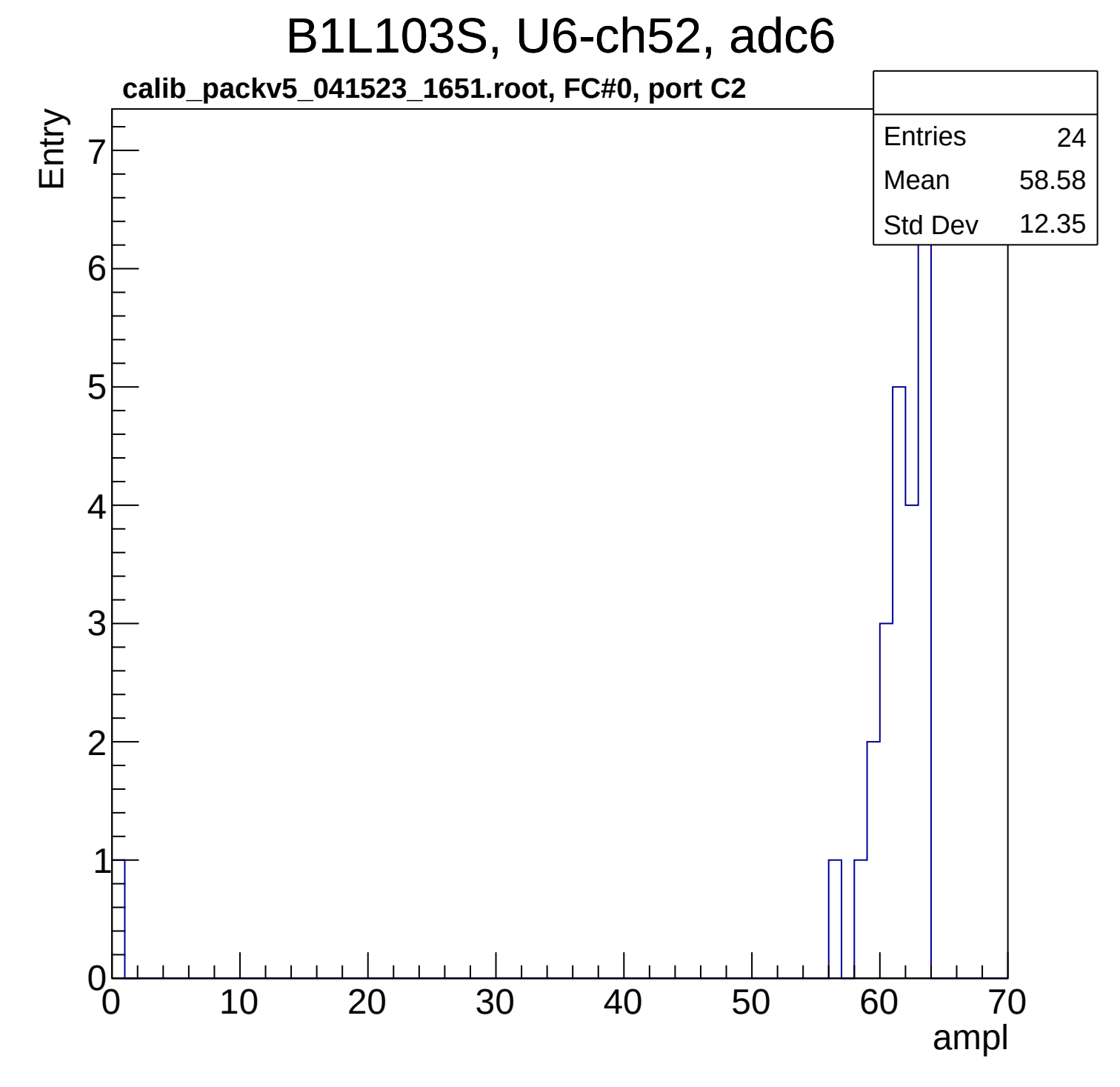
B1L103S, U6-ch52, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 58.58
Std Dev 12.35
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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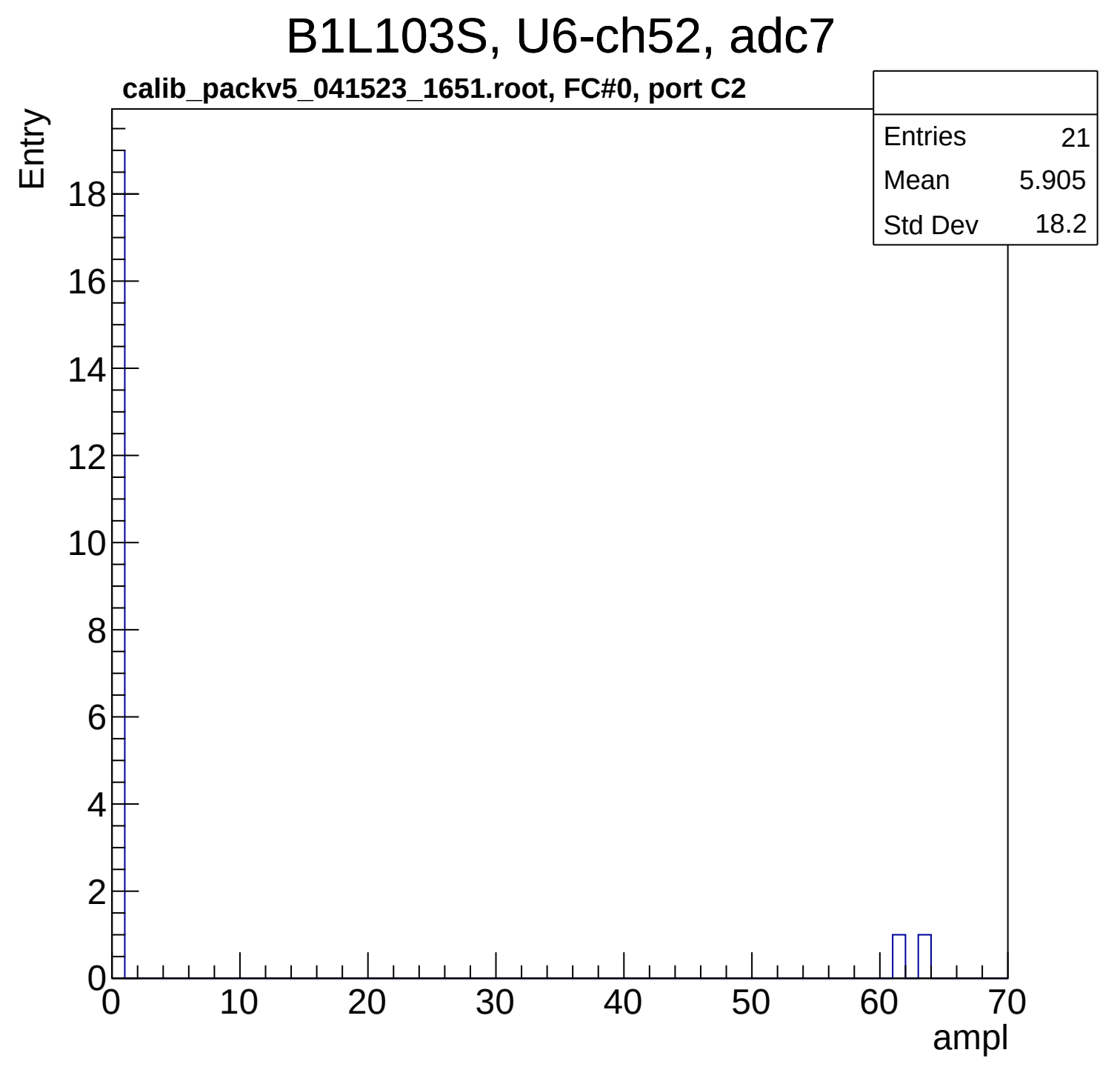
B1L103S, U6-ch52, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.905
Std Dev 18.2
Entry
0
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6
8
10
12
14
16
18
0
10
20
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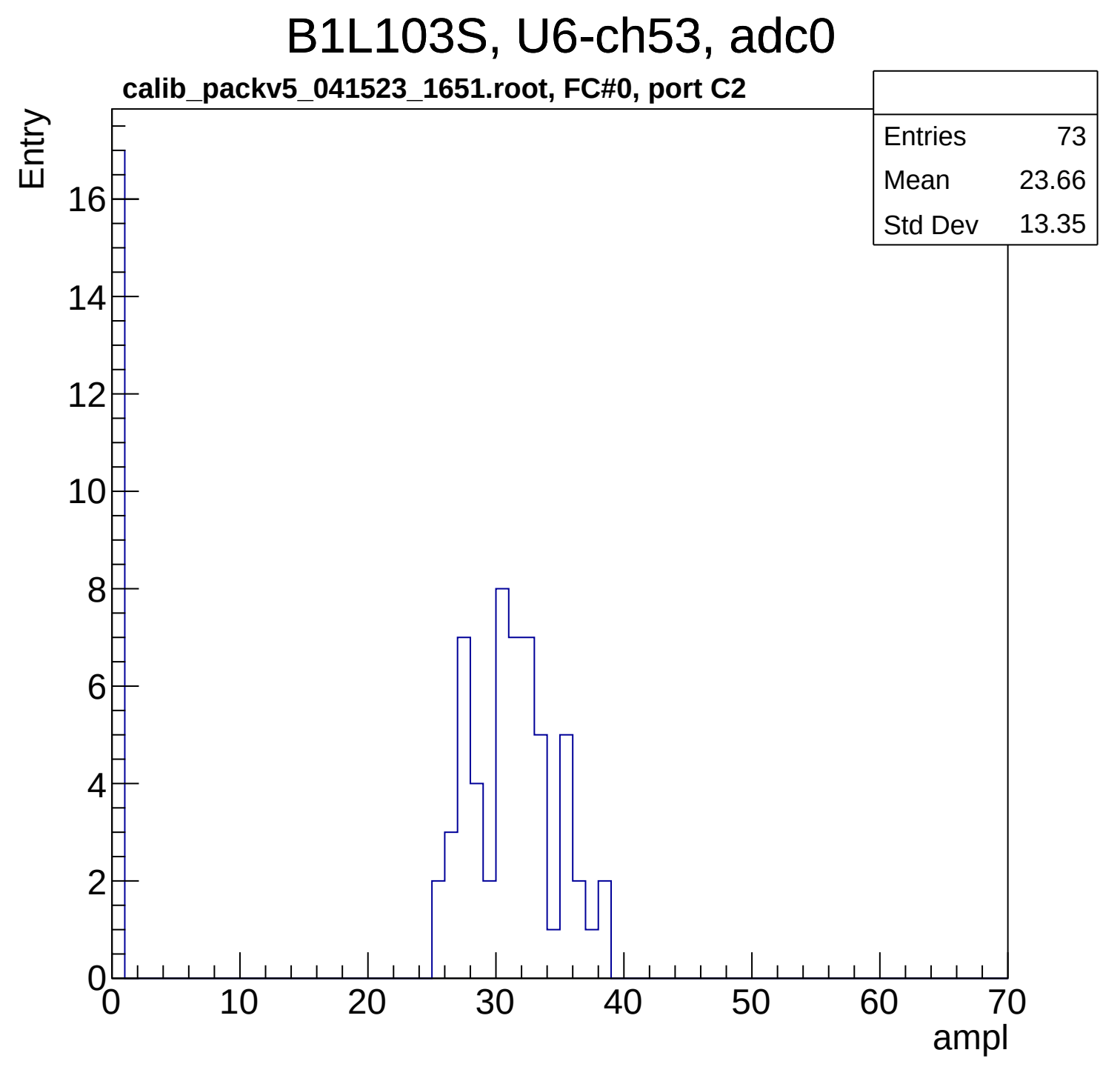
50
60
70
ampl


B1L103S, U6-ch53, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 23.66
Std Dev 13.35
Entry
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6
8
10
12
14
16
0
10
20
30
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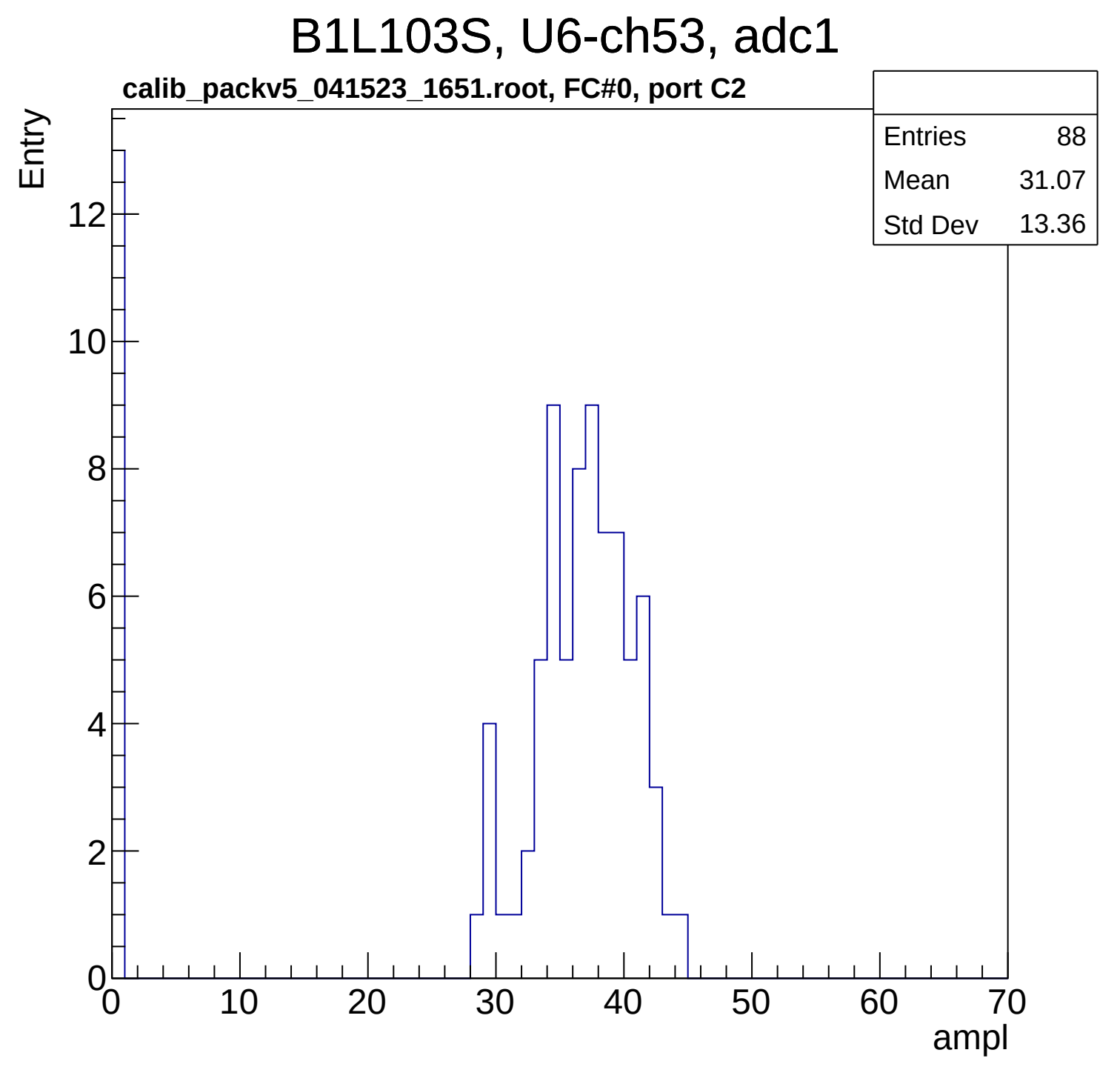
50
60
70
ampl


B1L103S, U6-ch53, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 31.07
Std Dev 13.36
Entry
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2
4
6
8
10
12
0
10
20
30
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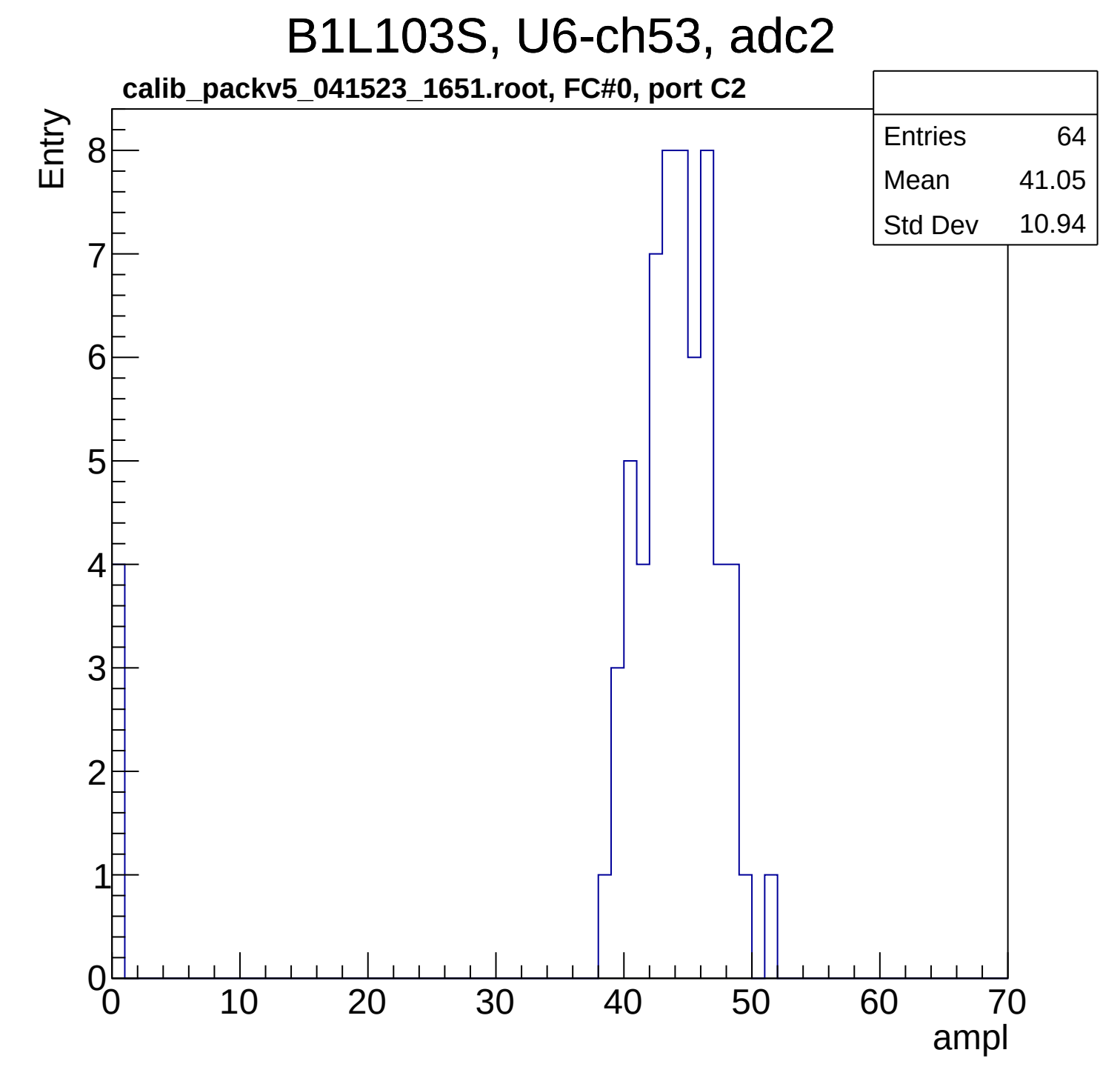
50
60
70
ampl


B1L103S, U6-ch53, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 41.05
Std Dev 10.94
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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60
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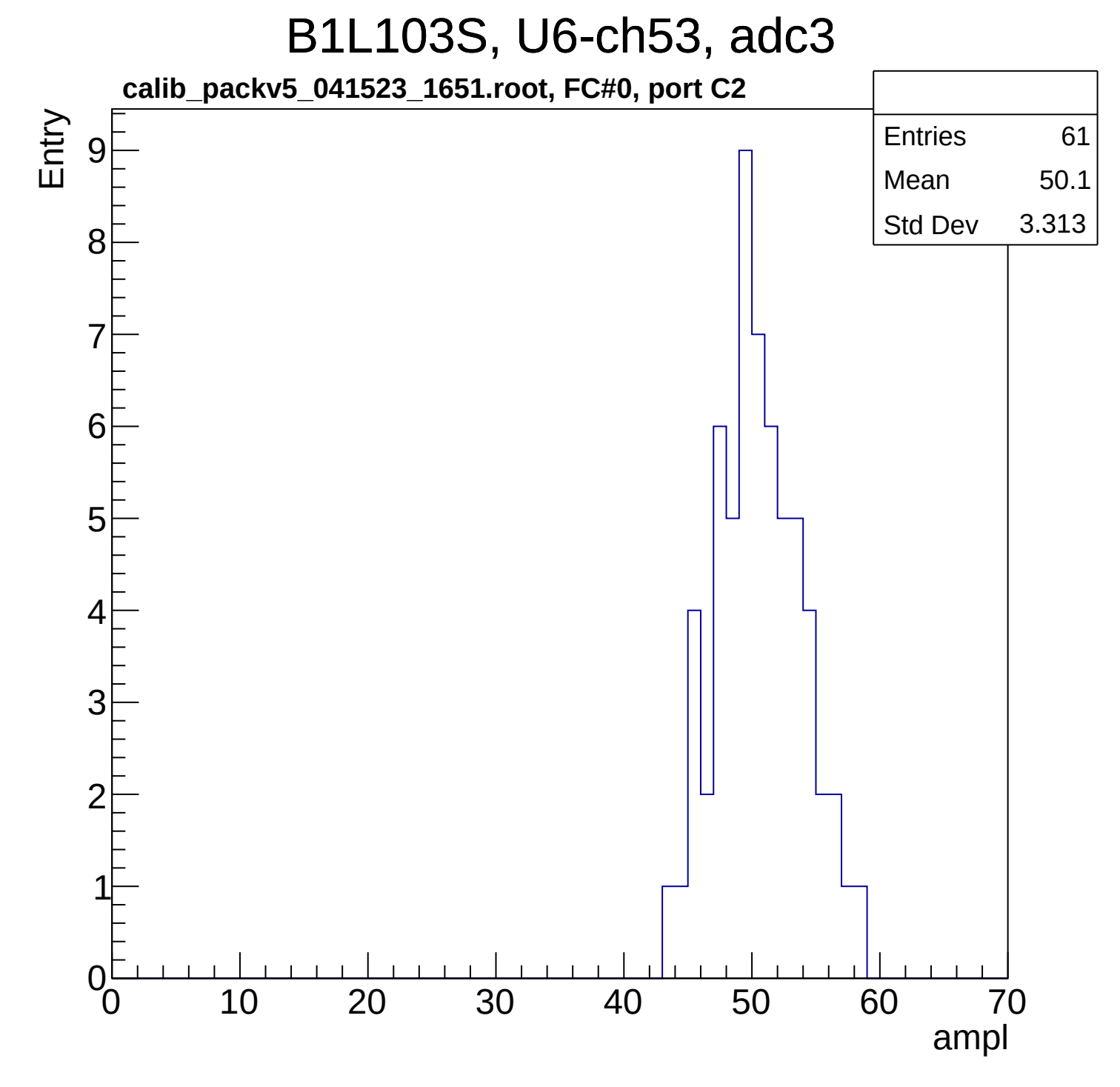
B1L103S, U6-ch53, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 50.1
Std Dev 3.313
Entry
ampl
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2
3
4
5
6
7
8
9
0
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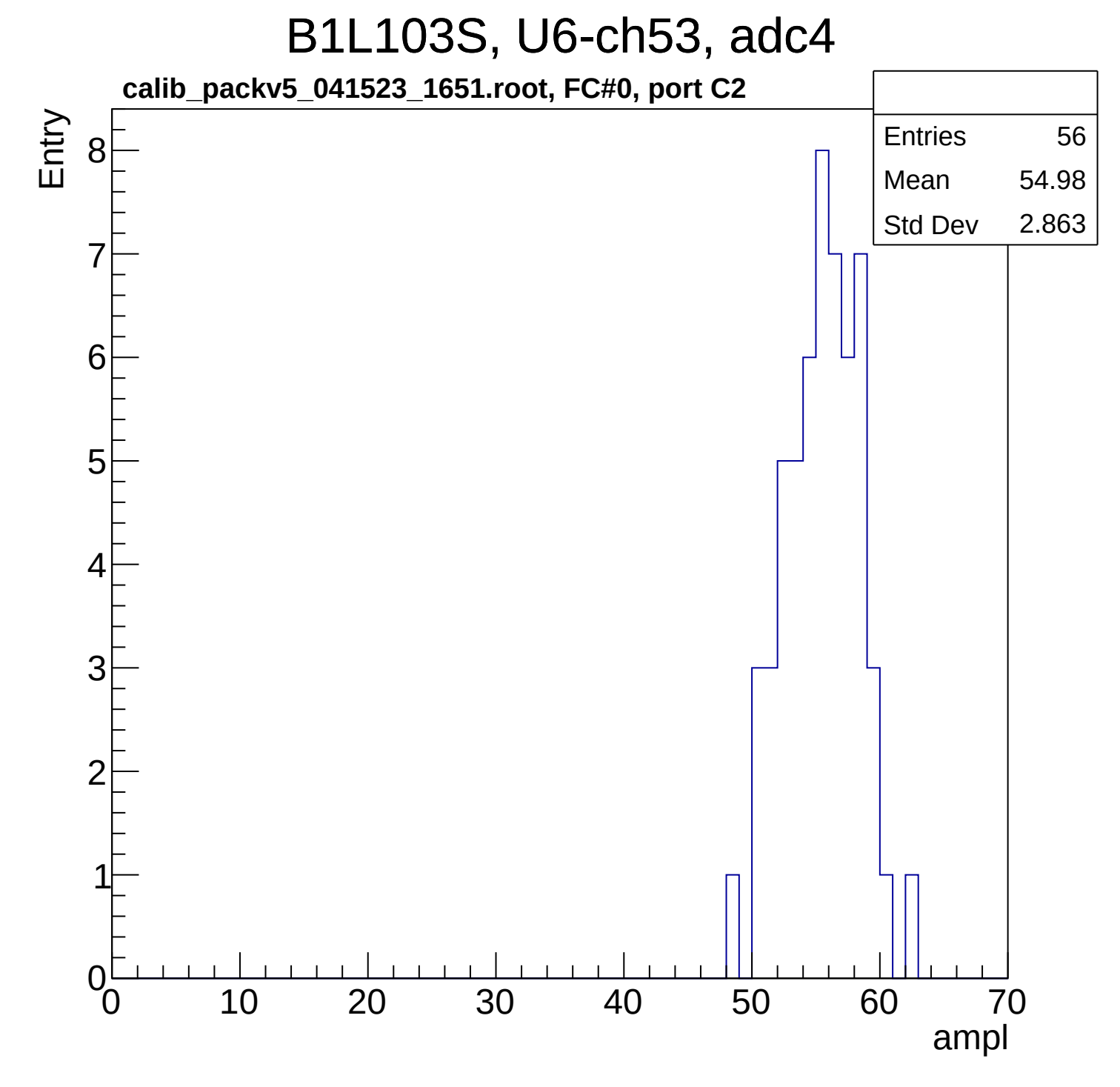
60
70


B1L103S, U6-ch53, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 54.98
Std Dev 2.863
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
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60
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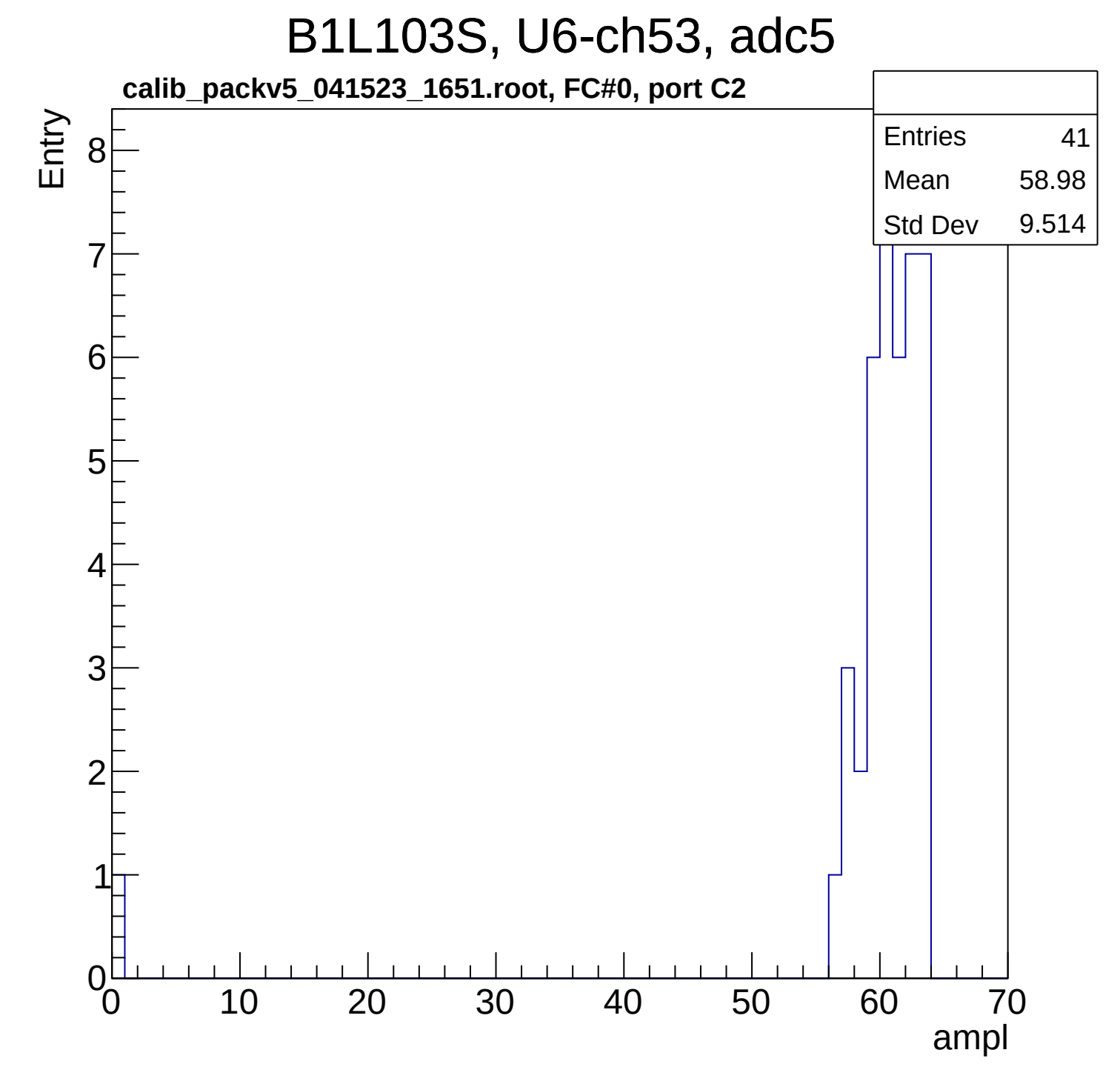
B1L103S, U6-ch53, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 58.98
Std Dev 9.514
Entry
ampl
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4
5
6
7
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0
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60
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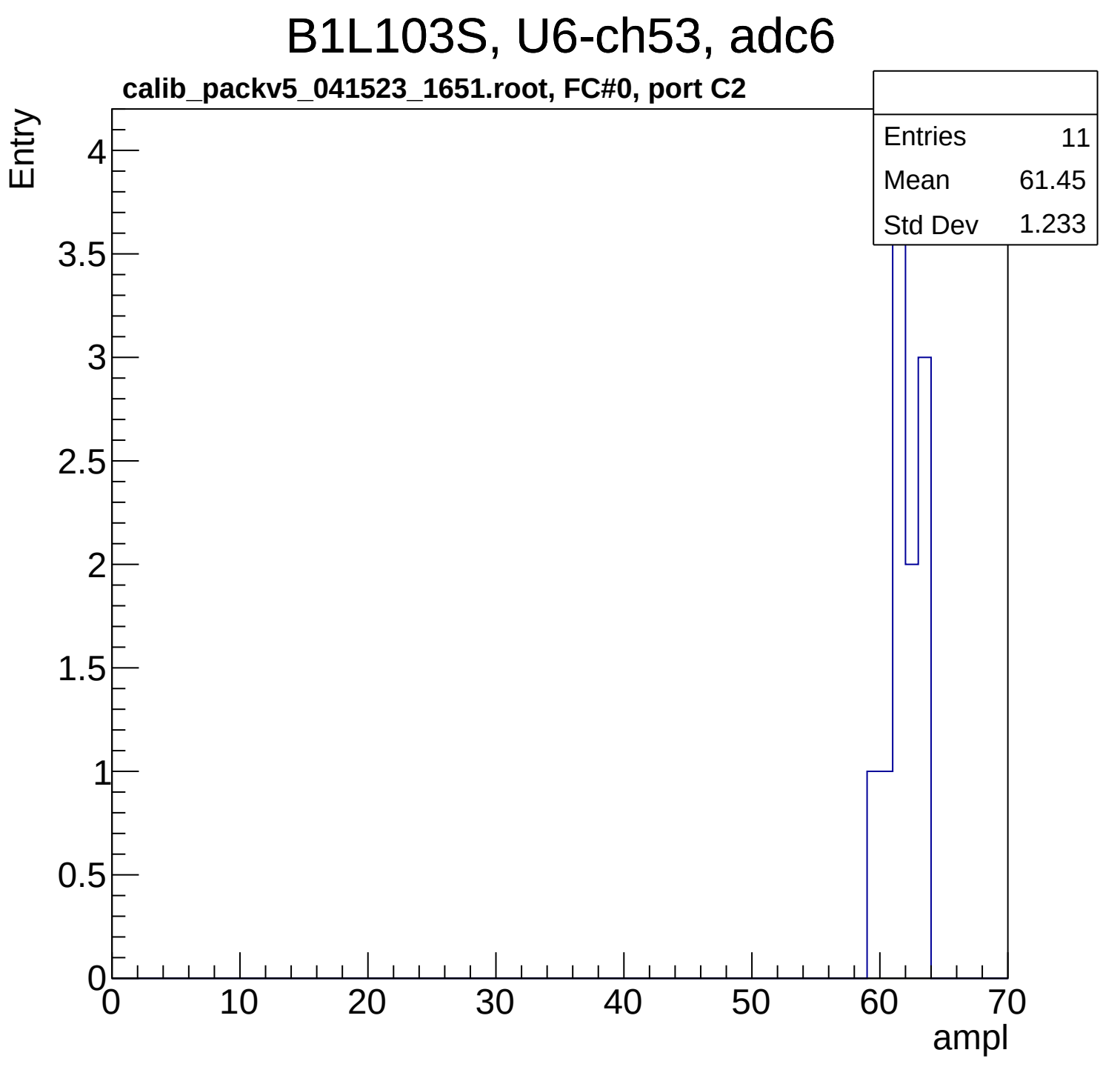
B1L103S, U6-ch53, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 61.45
Std Dev 1.233
Entry
ampl
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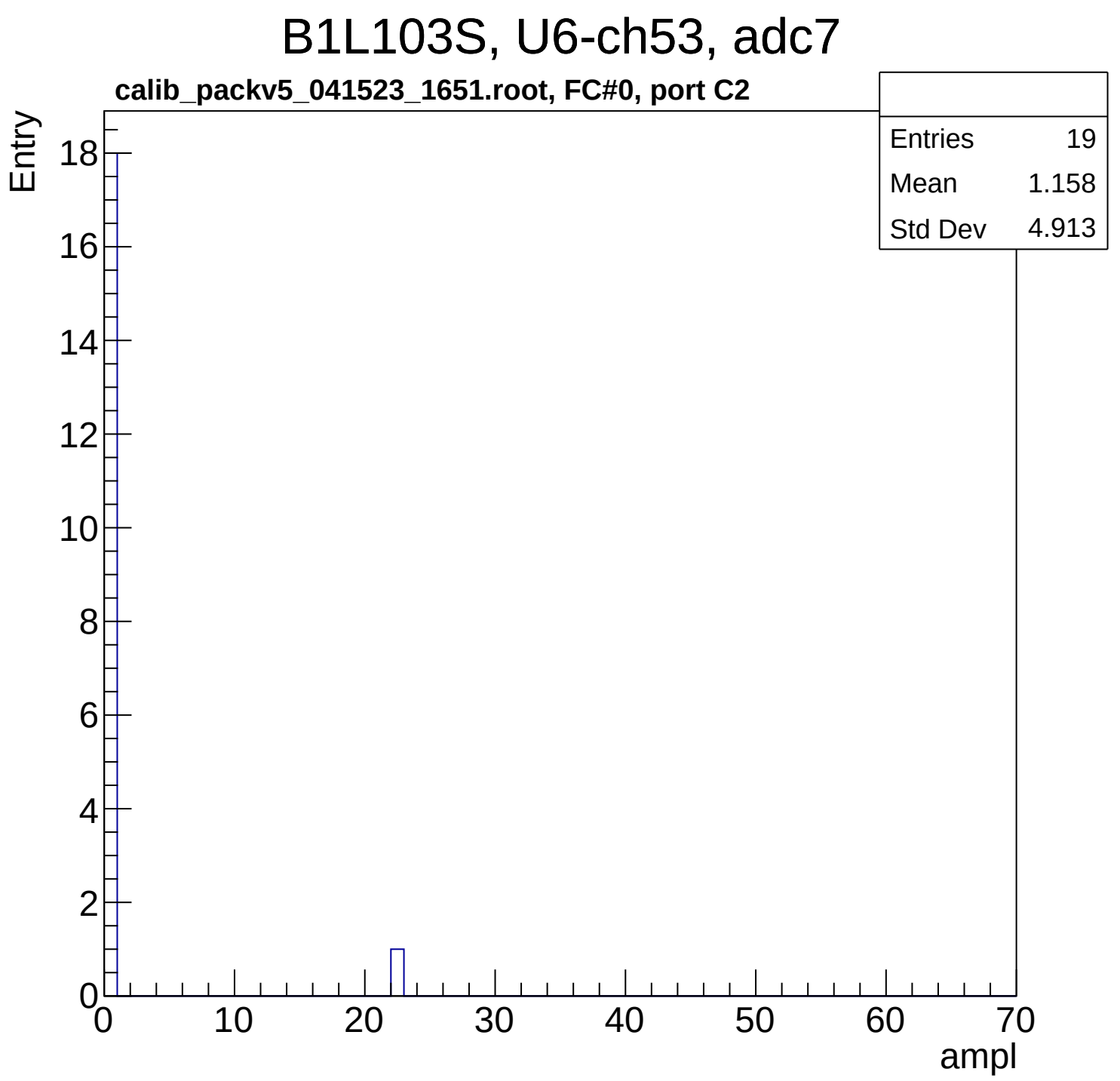
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U6-ch53, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.158
Std Dev 4.913
Entry
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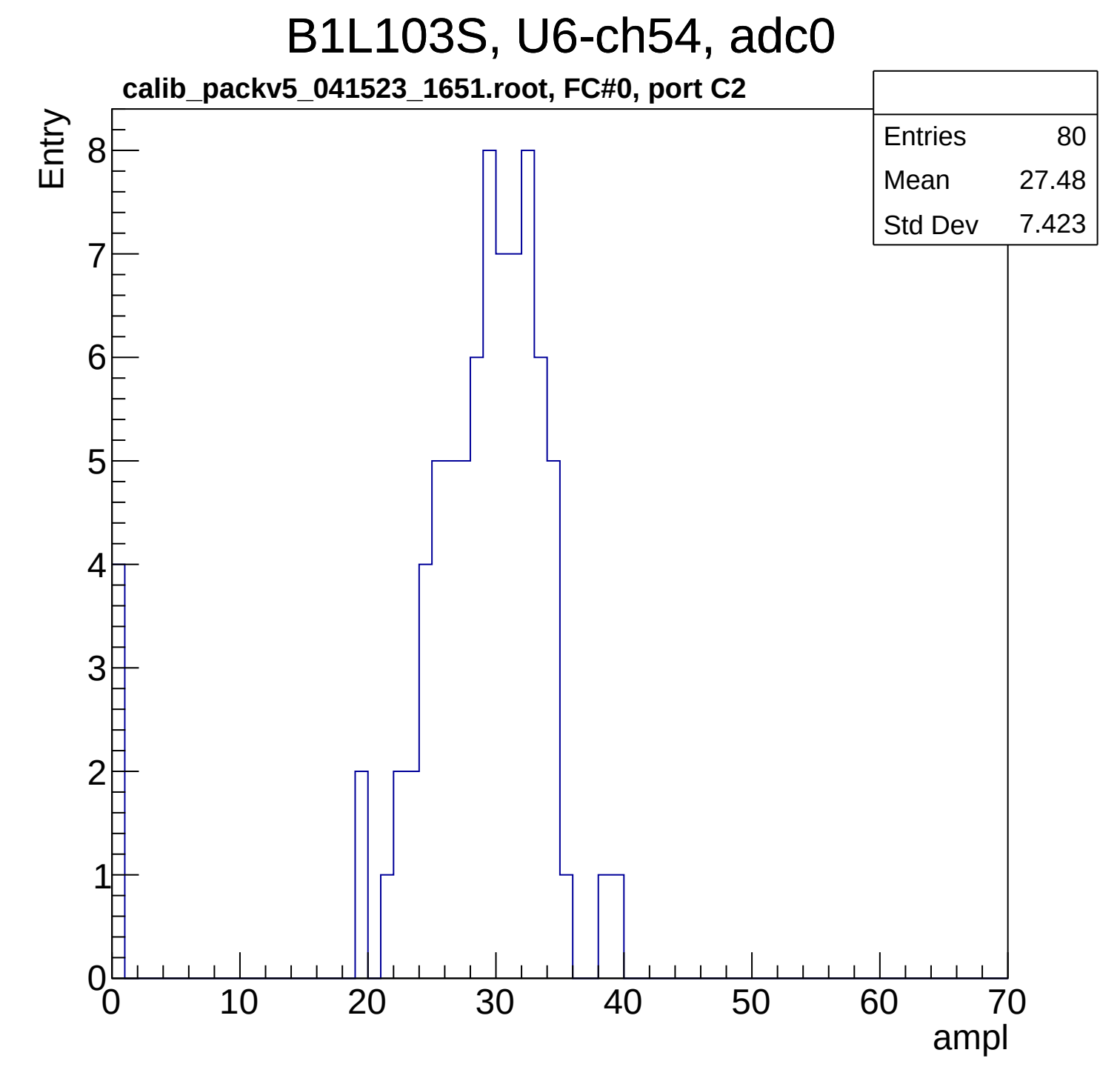
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch54, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 27.48
Std Dev 7.423
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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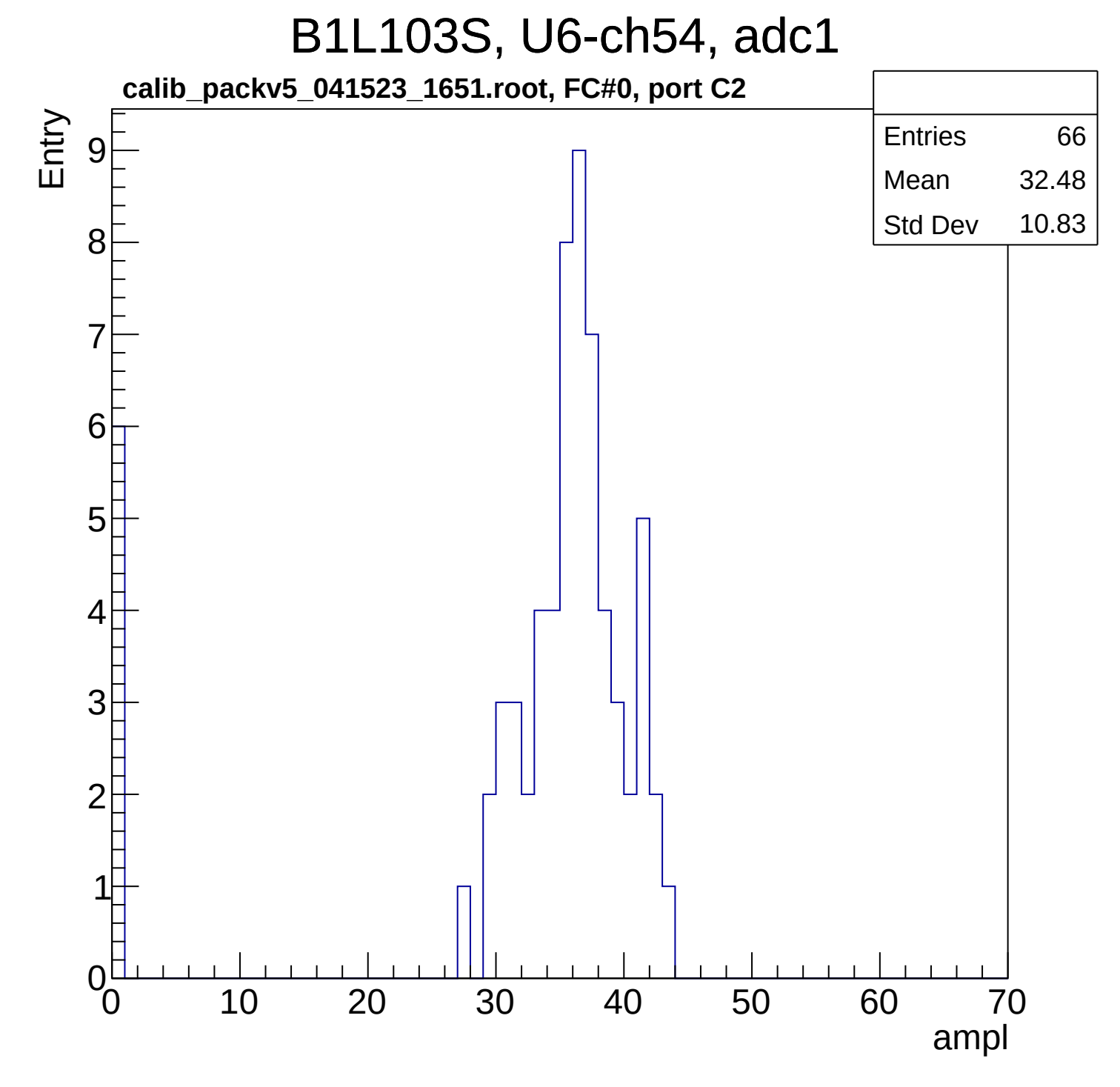
40
50
60
70


B1L103S, U6-ch54, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 32.48
Std Dev 10.83
Entry
ampl
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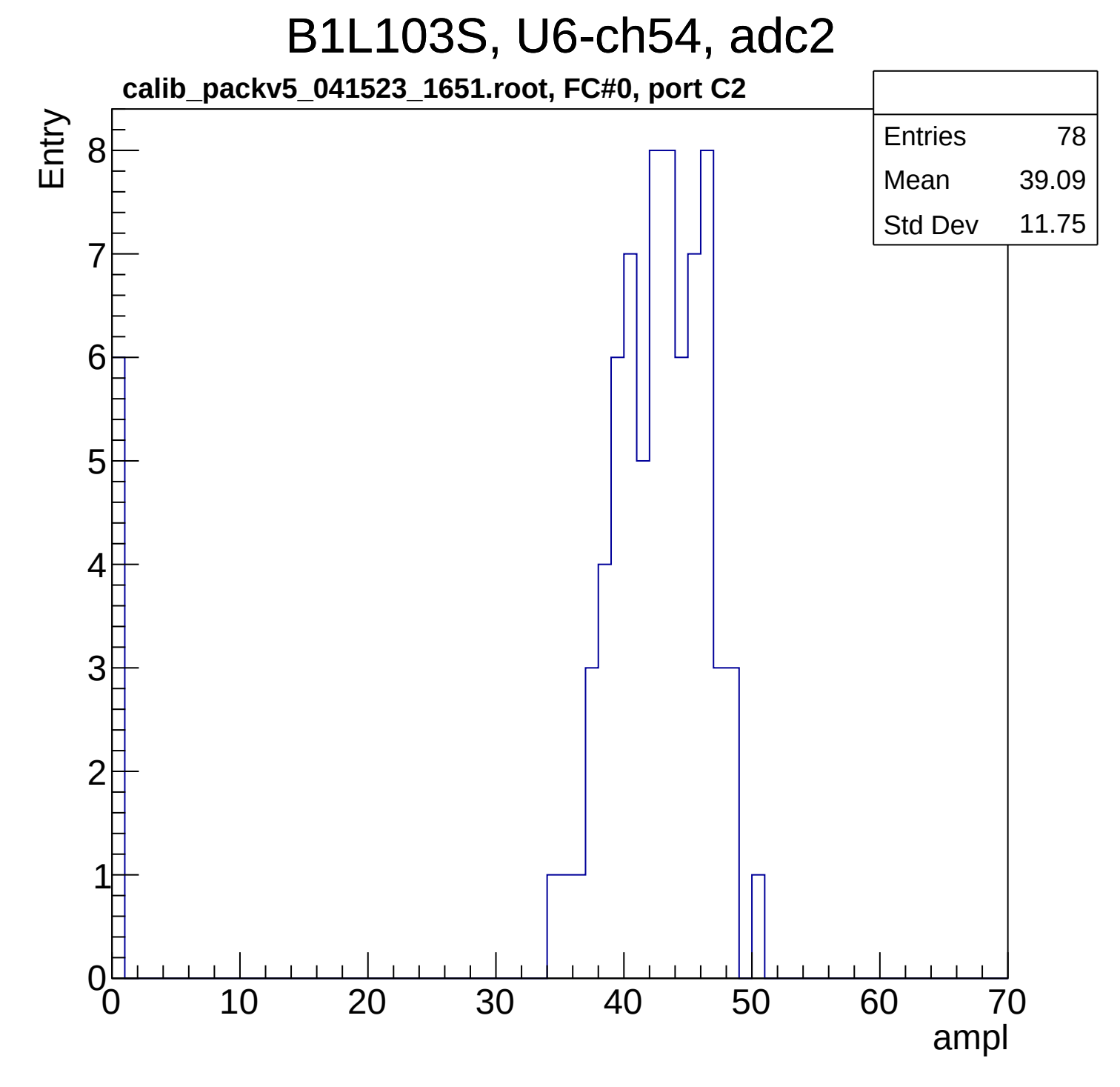
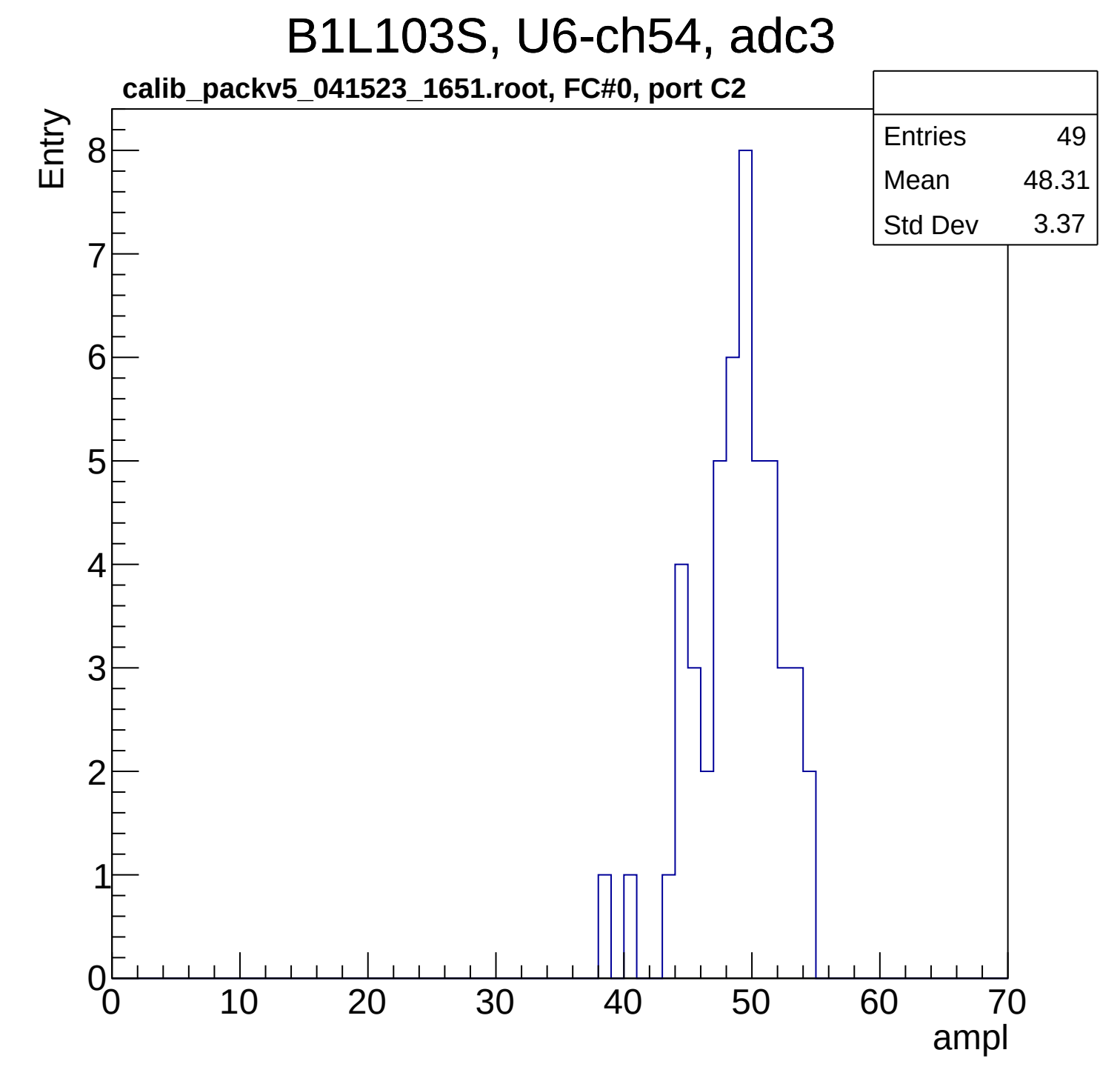
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch54, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 39.09
Std Dev 11.75
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch54, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 48.31
Std Dev 3.37
Entry
ampl
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2
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4
5
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7
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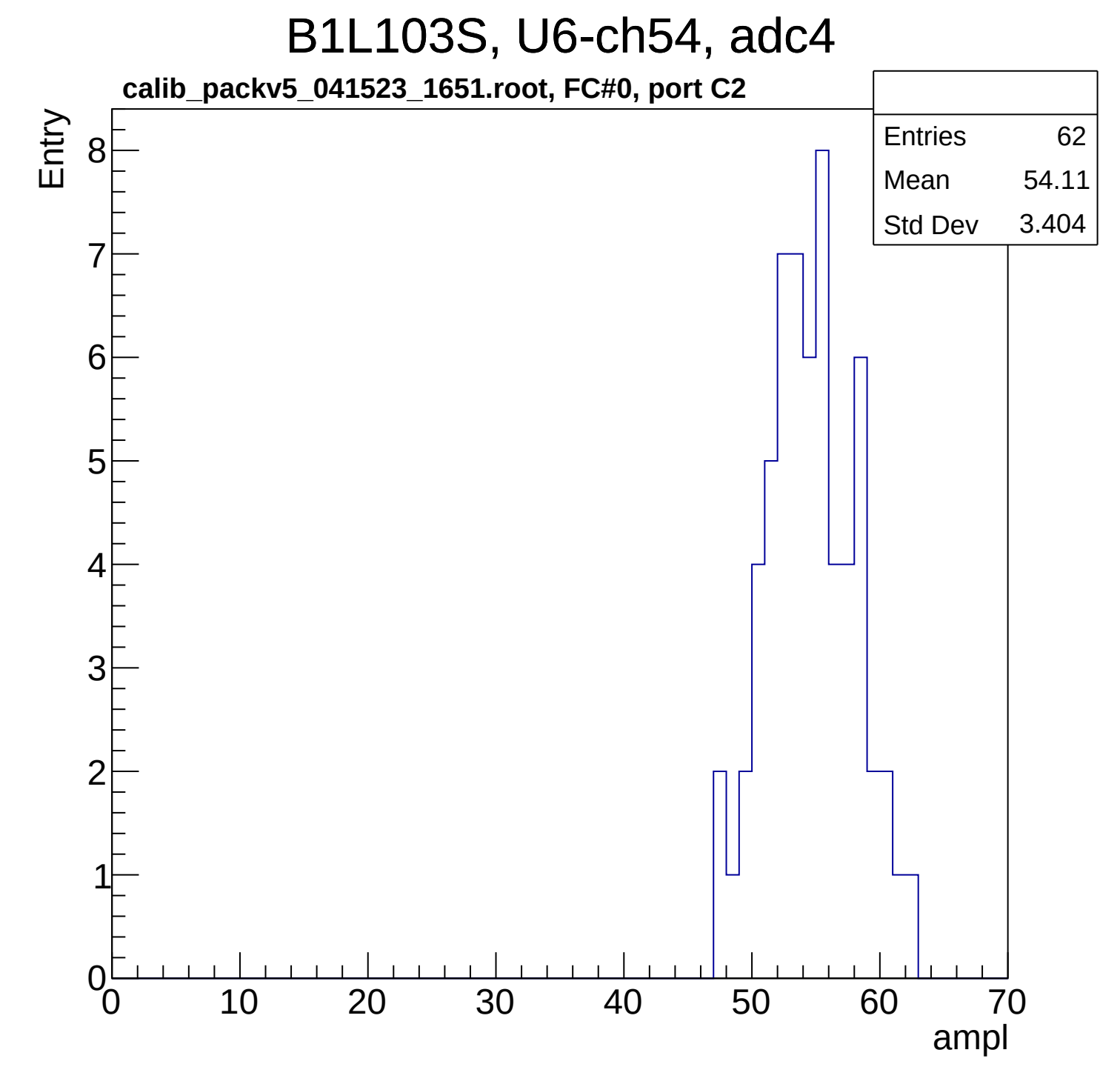
B1L103S, U6-ch54, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 54.11
Std Dev 3.404
Entry
ampl
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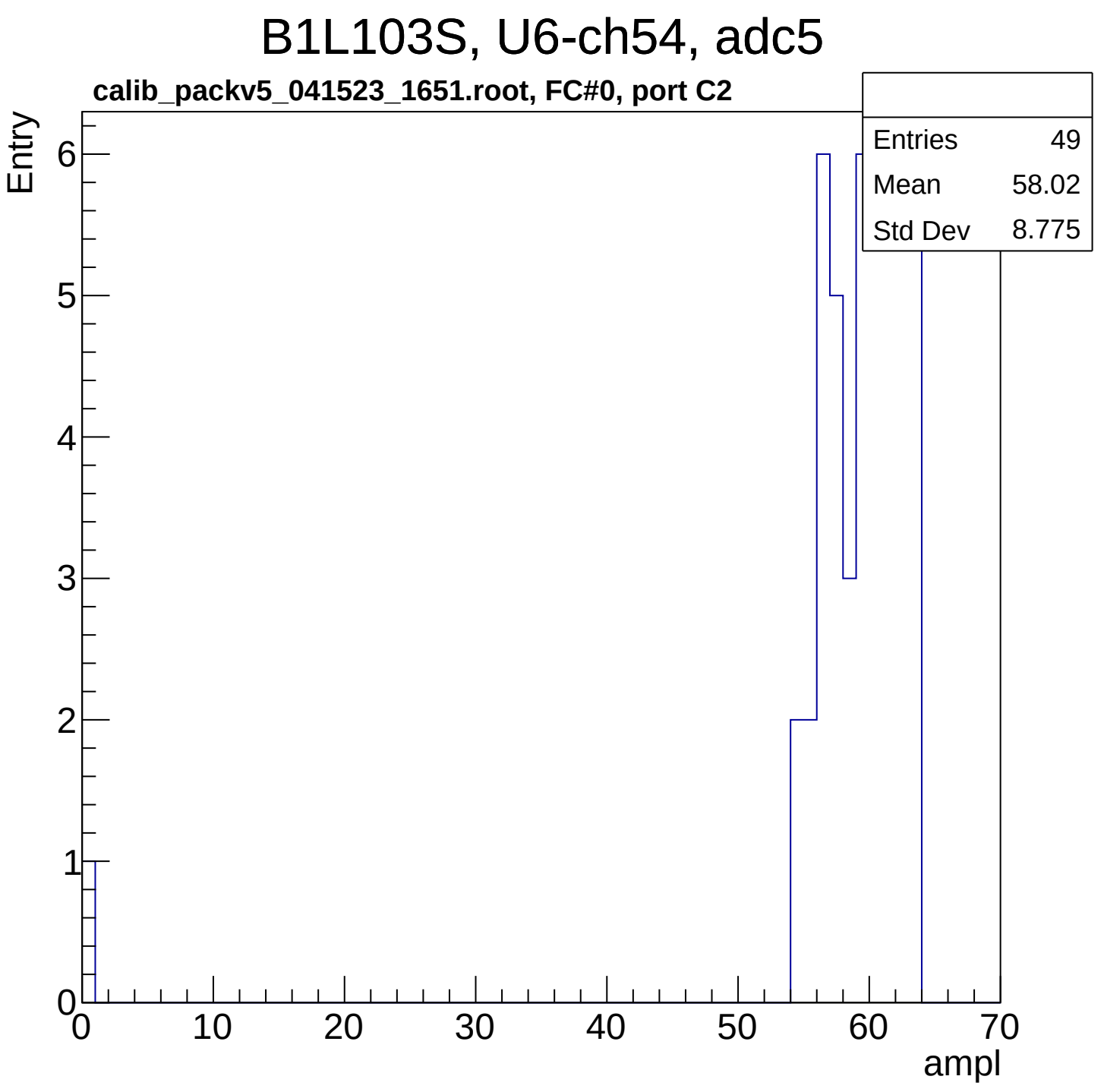
B1L103S, U6-ch54, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 58.02
Std Dev 8.775
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6
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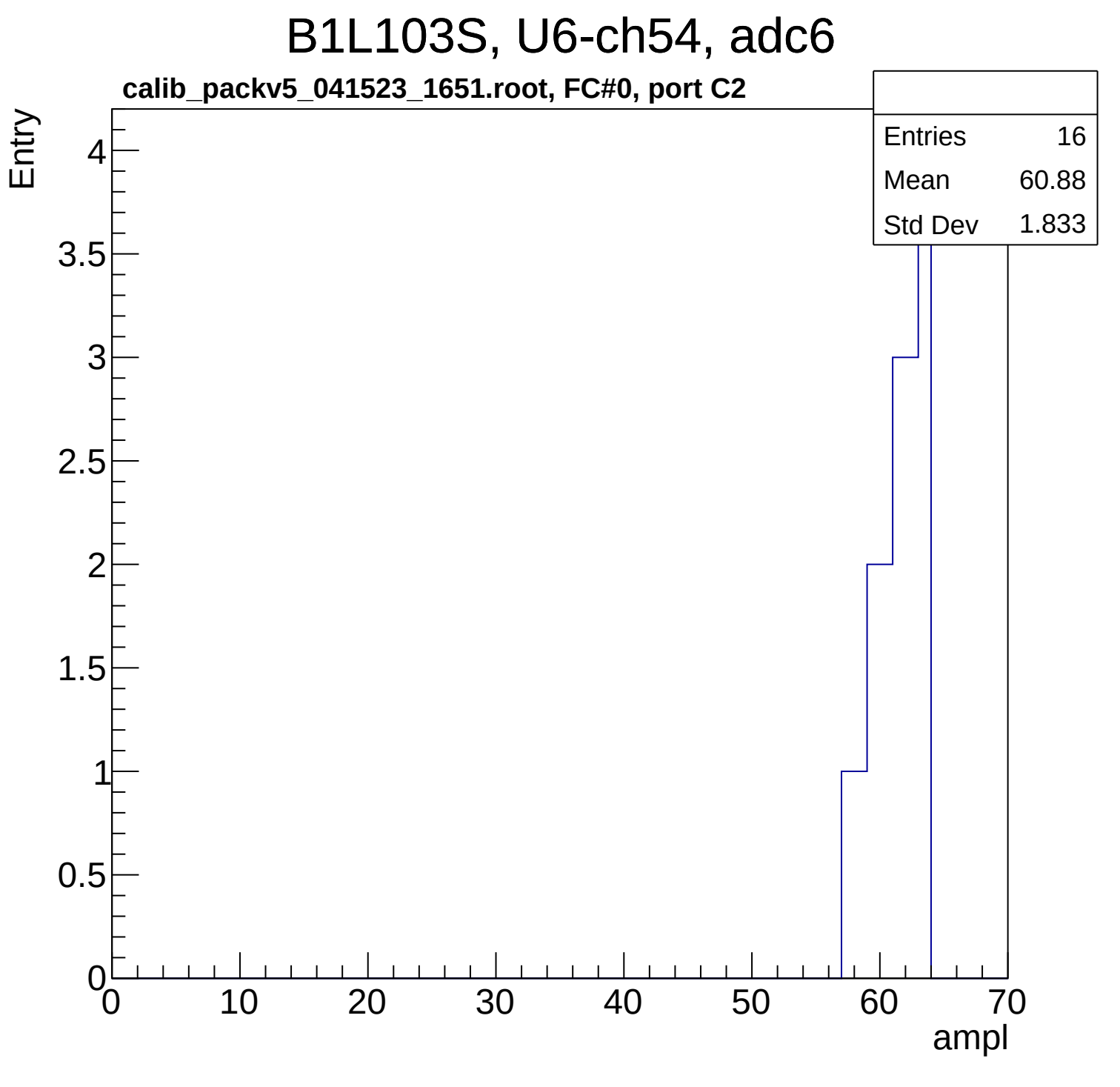
70
ampl


B1L103S, U6-ch54, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 60.88
Std Dev 1.833
Entry
ampl
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1.5
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3
3.5
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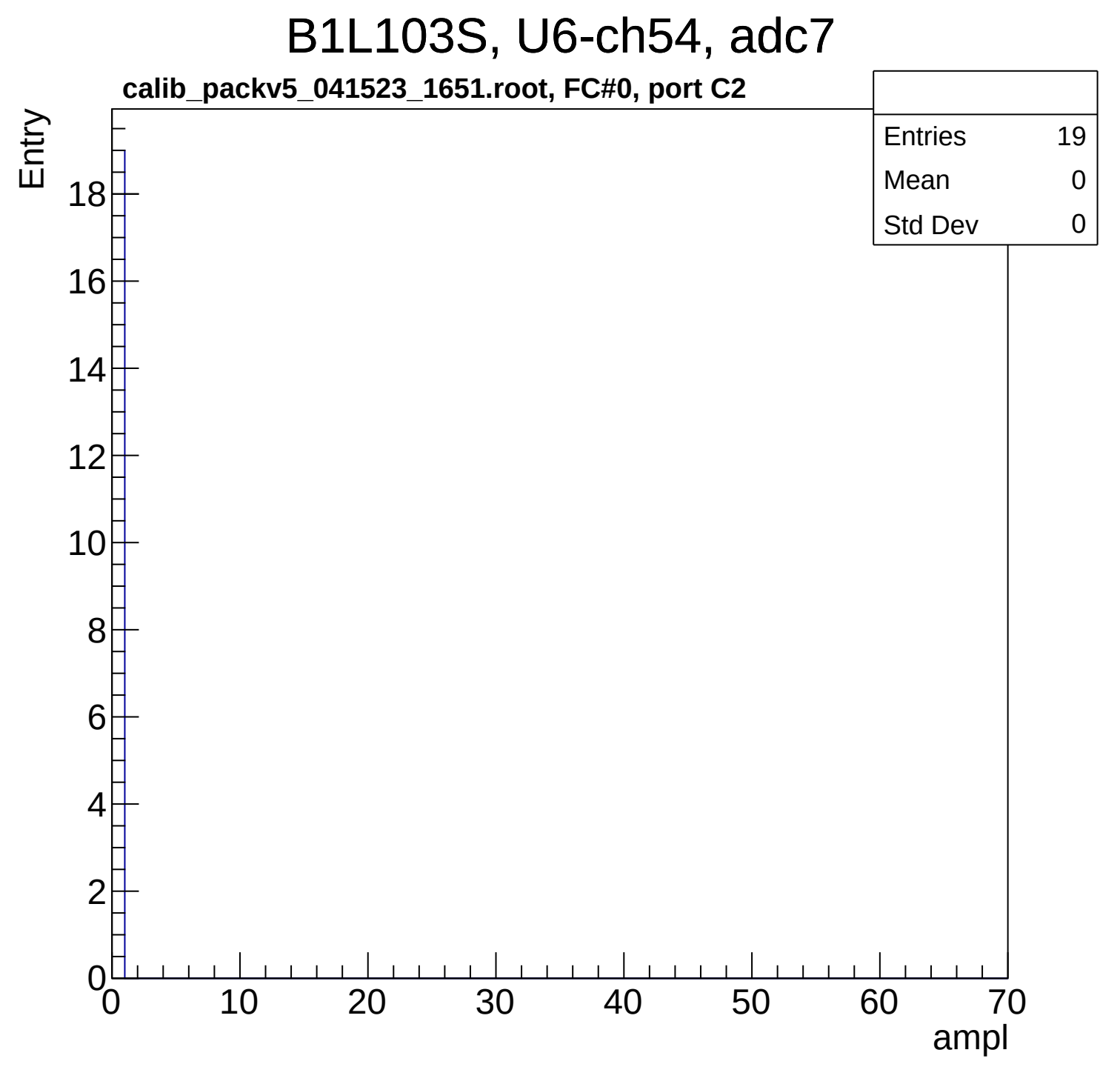
B1L103S, U6-ch54, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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6
8
10
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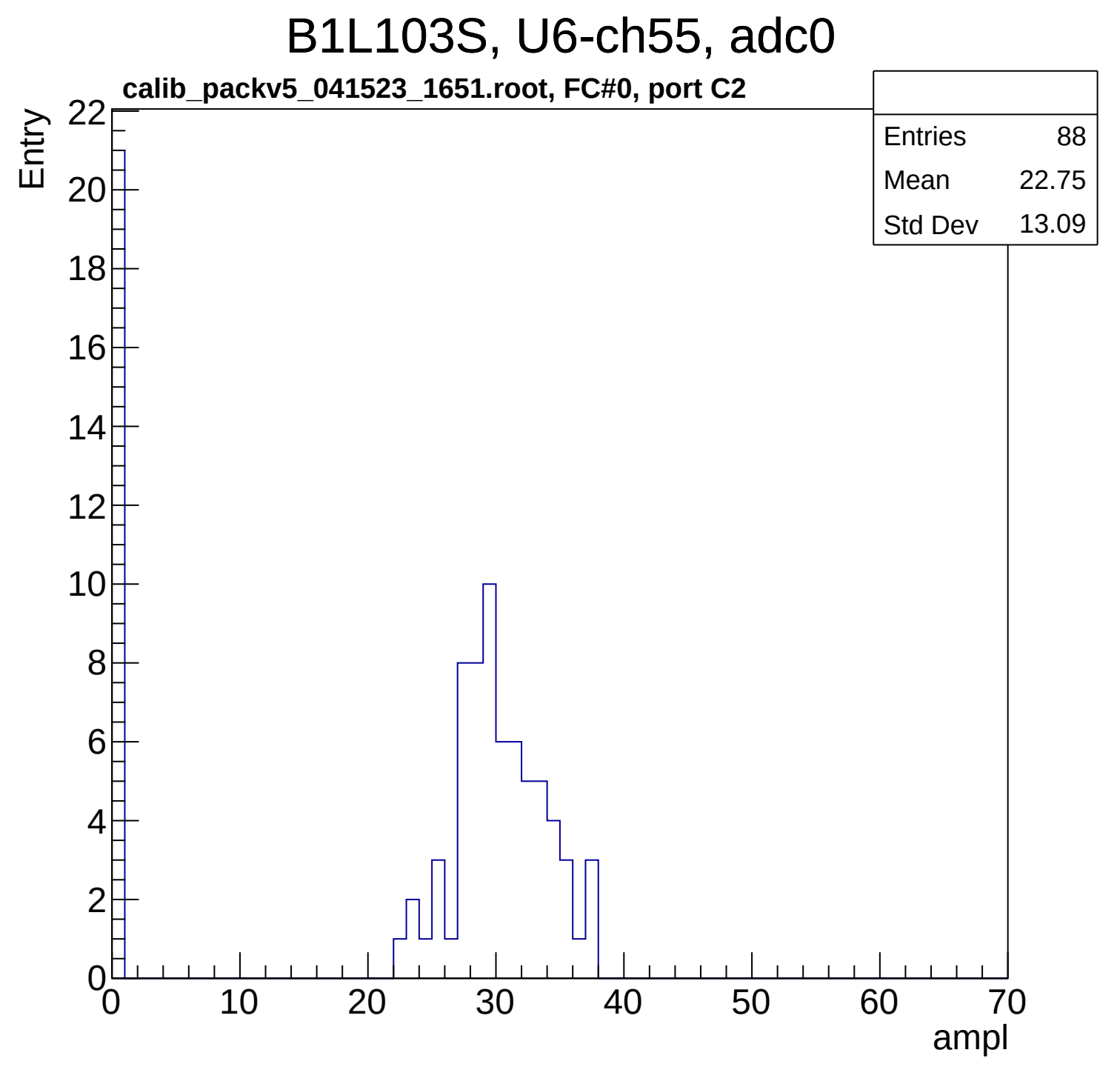
ampl


B1L103S, U6-ch55, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 22.75
Std Dev 13.09
Entry
ampl
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10
12
14
16
18
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22
0
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60
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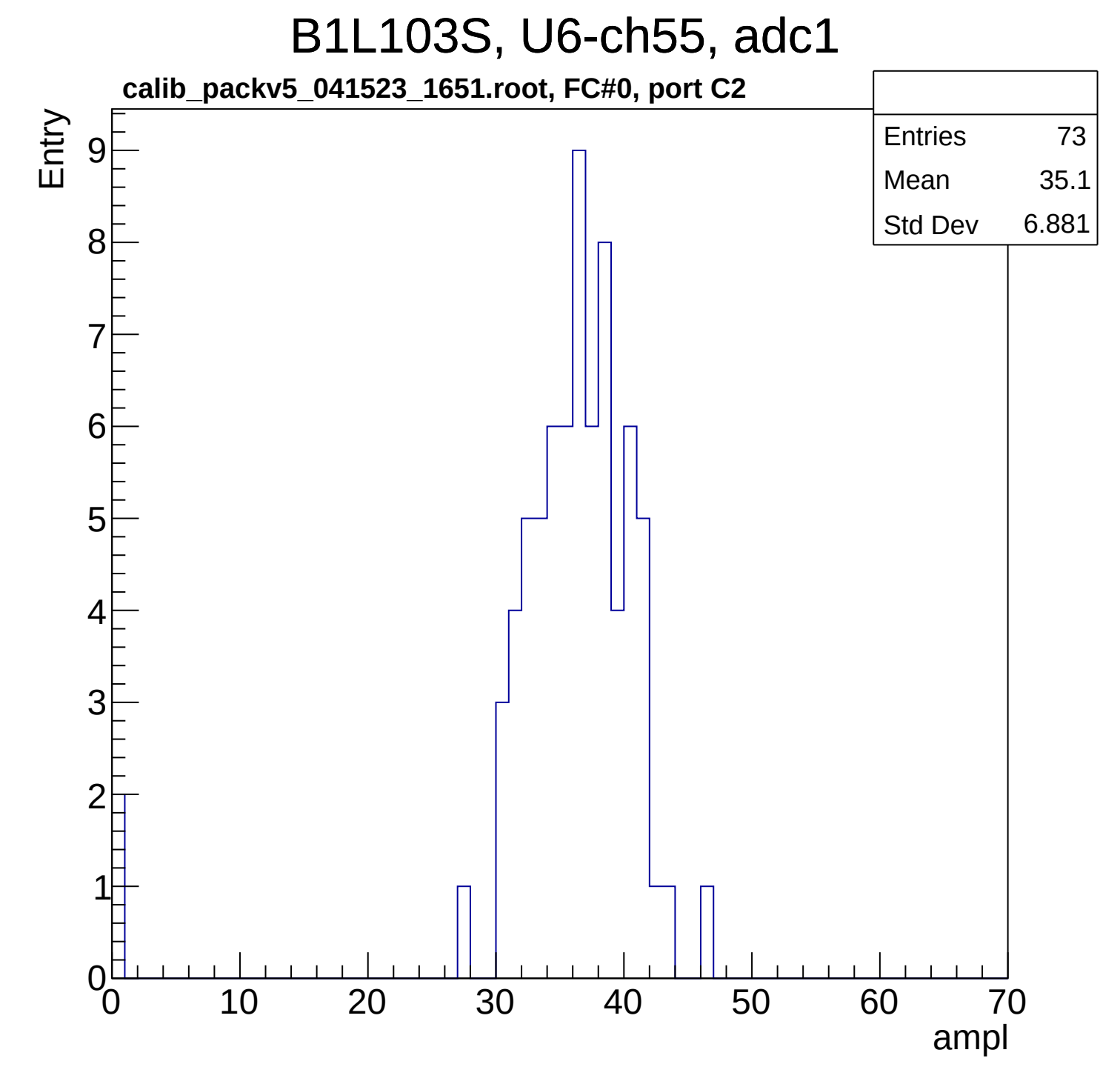
B1L103S, U6-ch55, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 35.1
Std Dev 6.881
Entry
ampl
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4
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8
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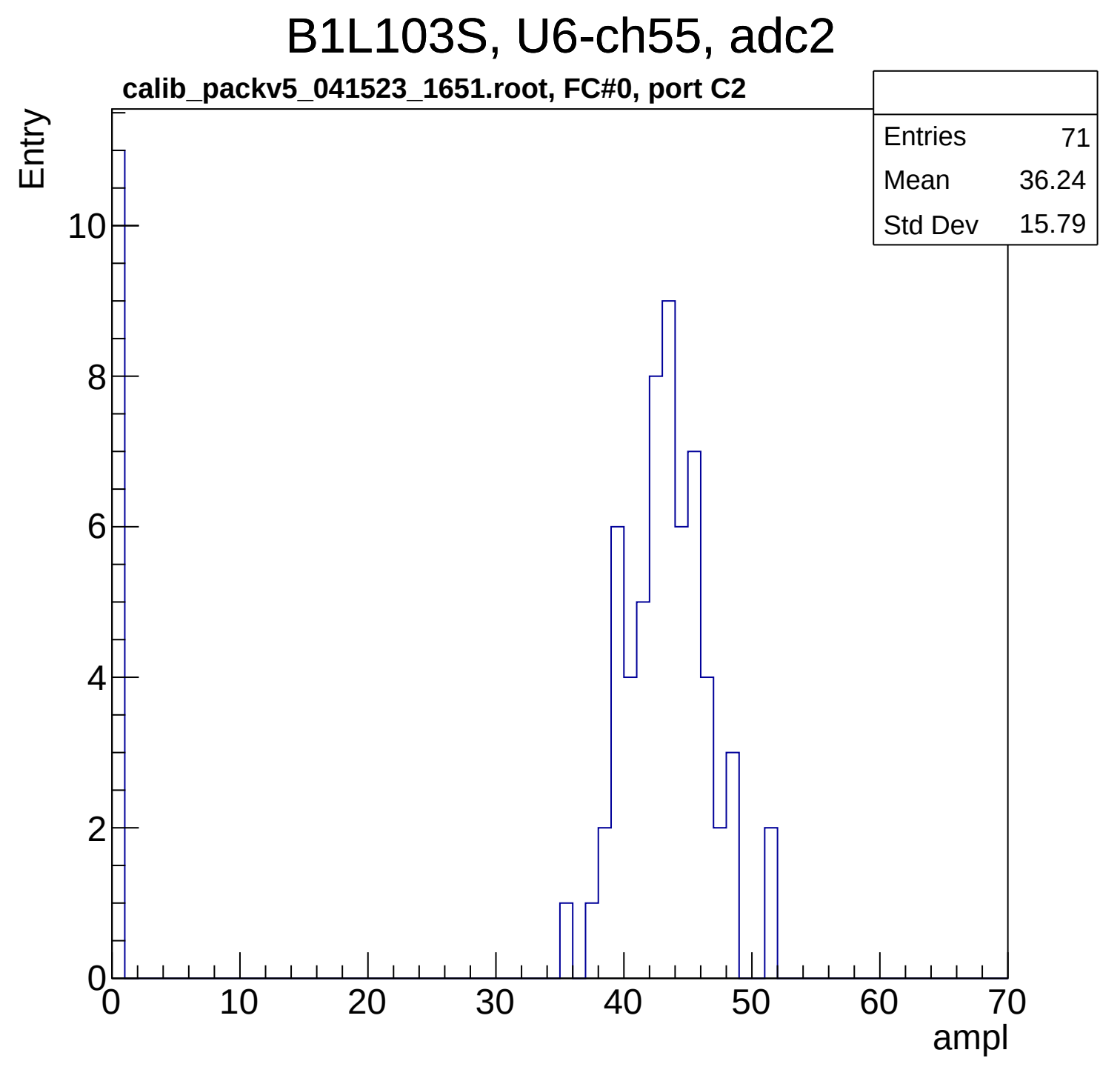
B1L103S, U6-ch55, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 36.24
Std Dev 15.79
Entry
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8
10
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10
20
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50
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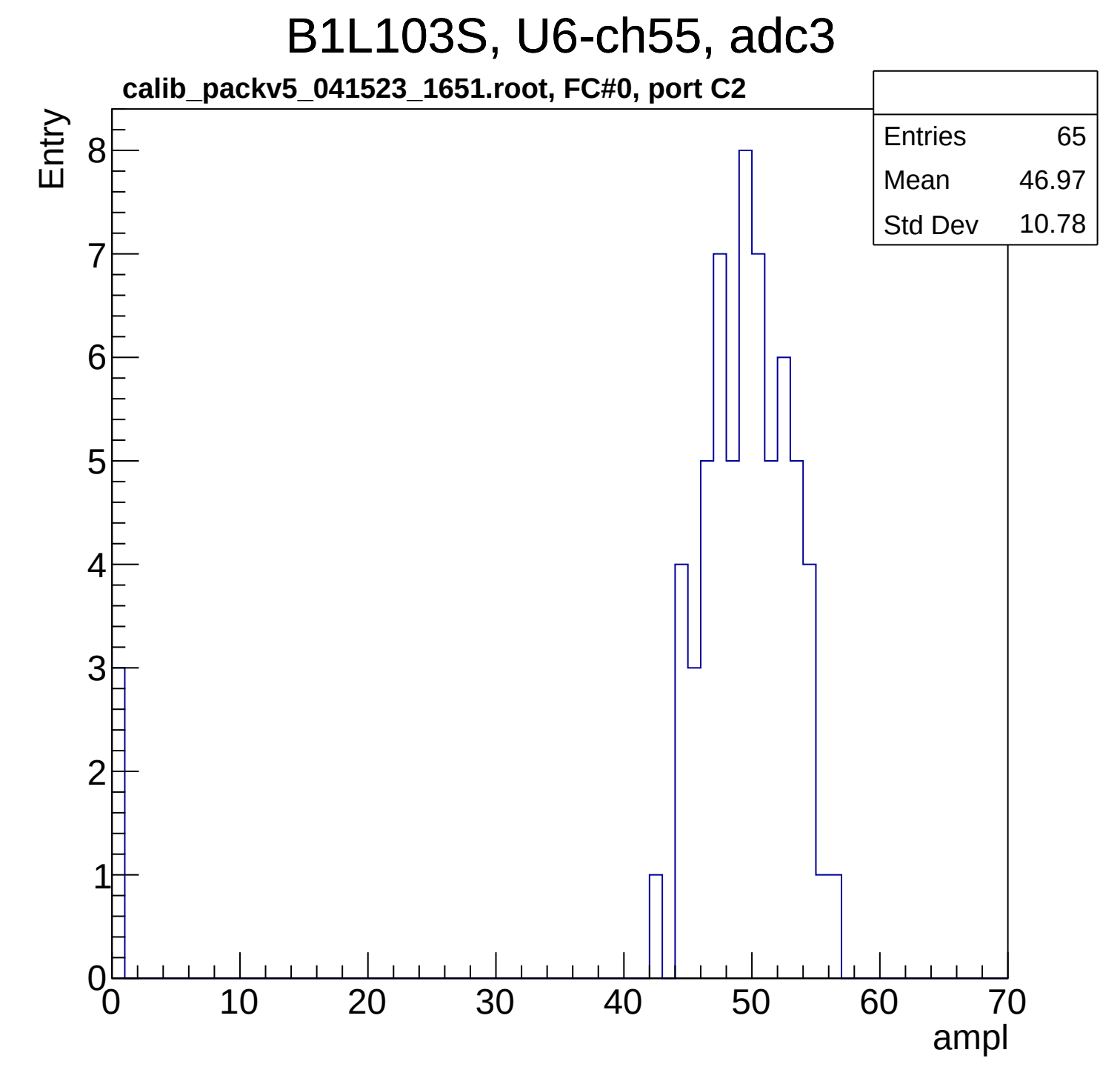
70
ampl


B1L103S, U6-ch55, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 46.97
Std Dev 10.78
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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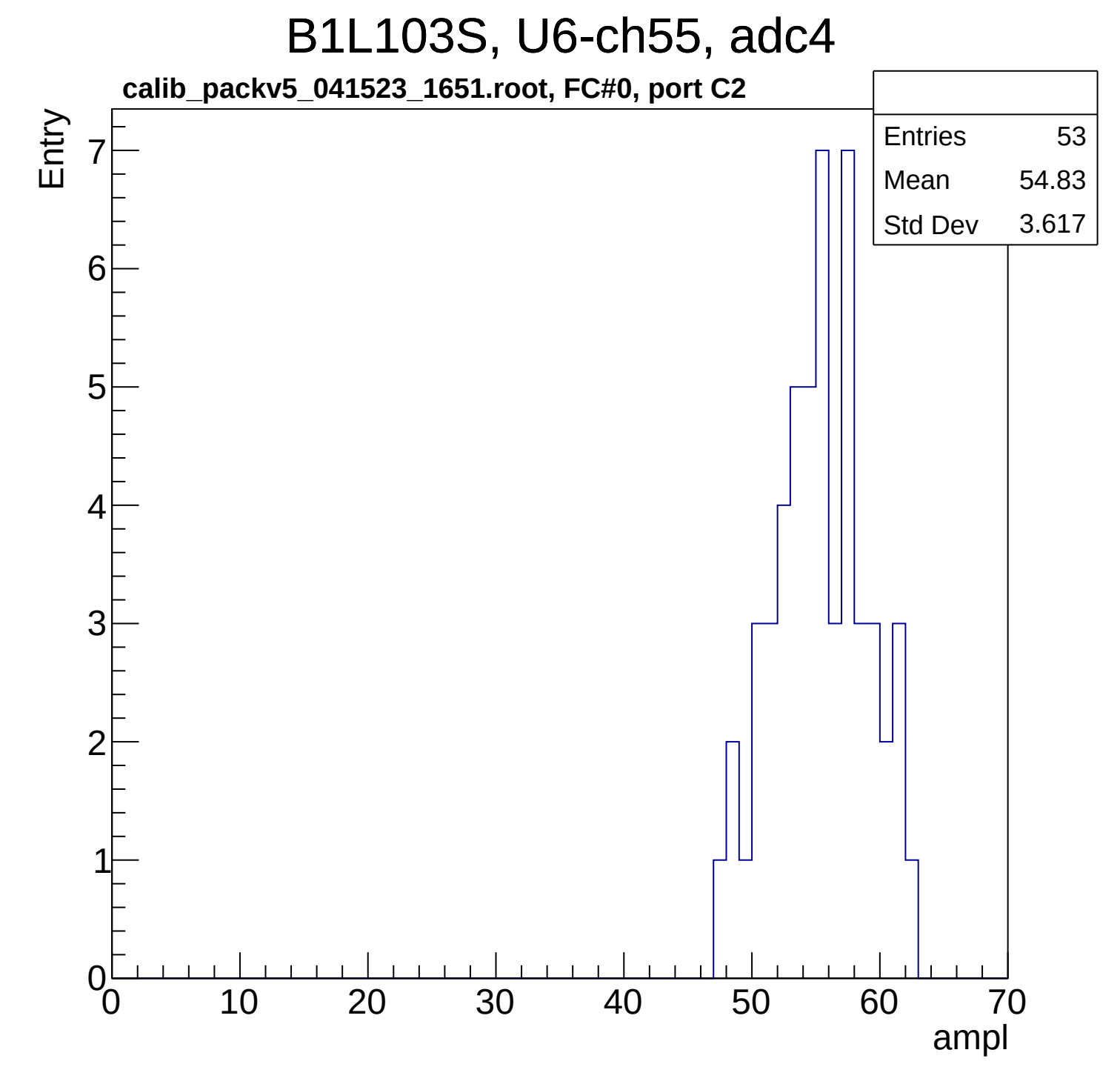
B1L103S, U6-ch55, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 54.83
Std Dev 3.617
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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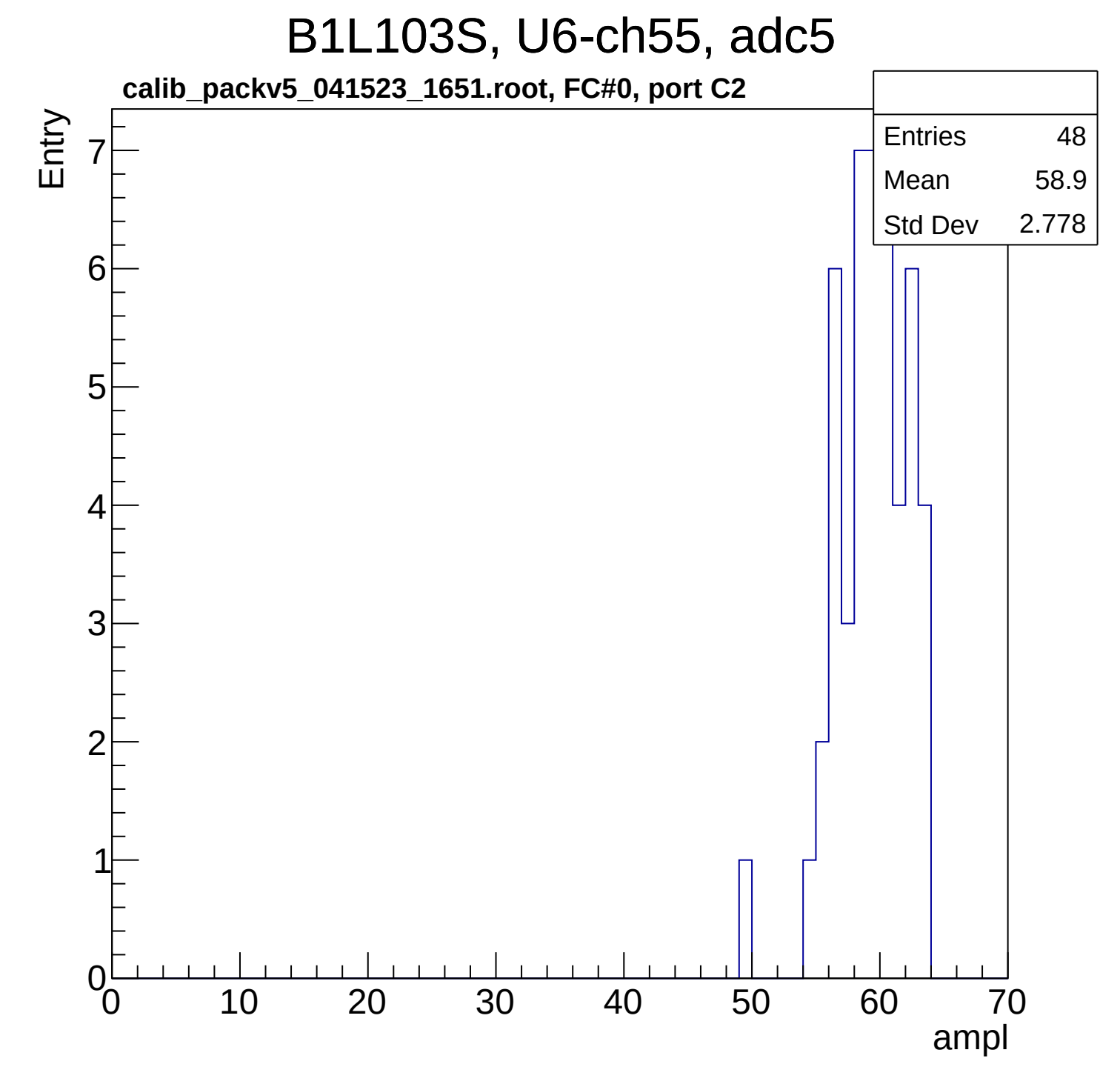
B1L103S, U6-ch55, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 58.9
Std Dev 2.778
Entry
ampl
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2
3
4
5
6
7
0
10
20
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40
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60
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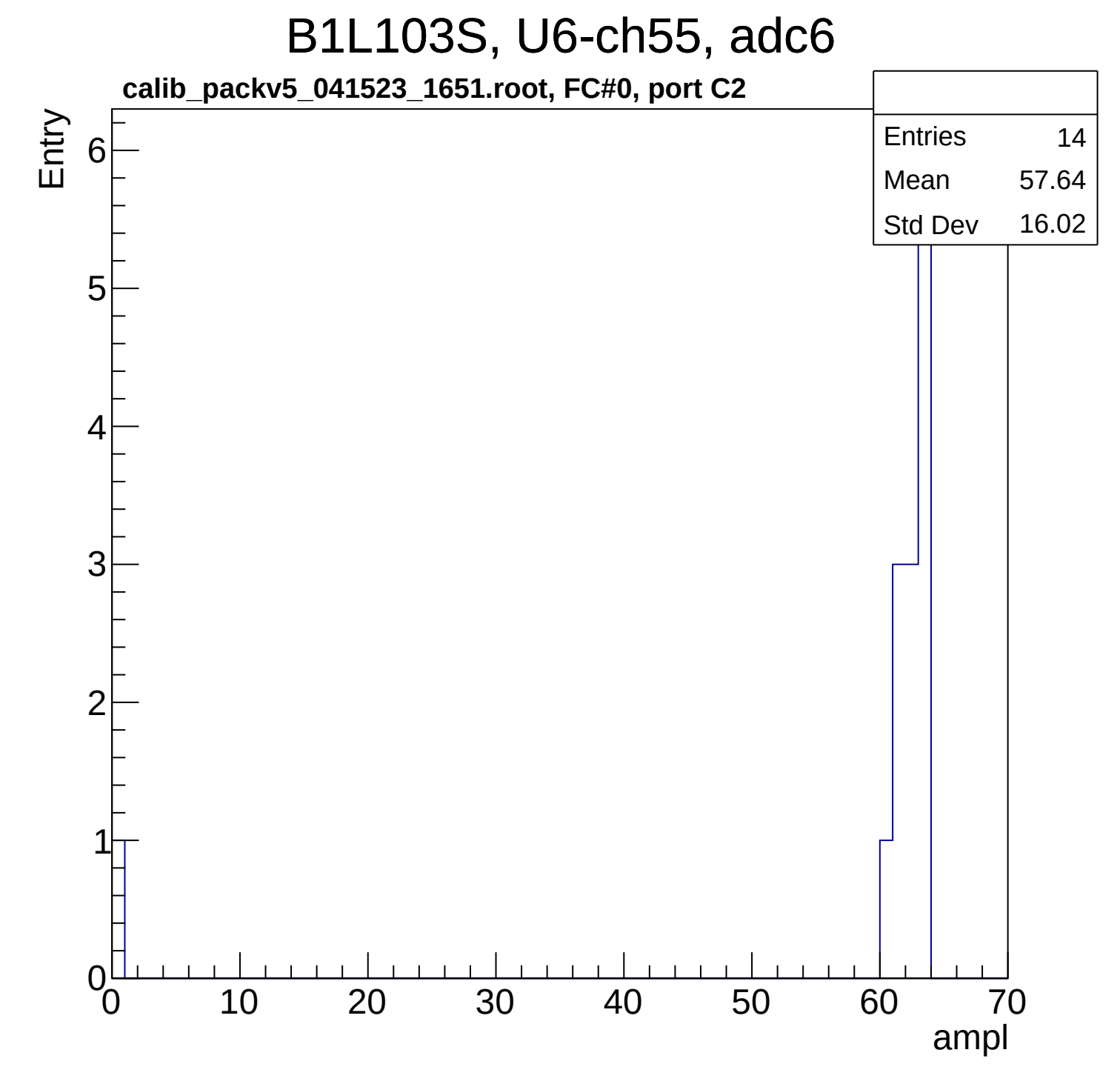
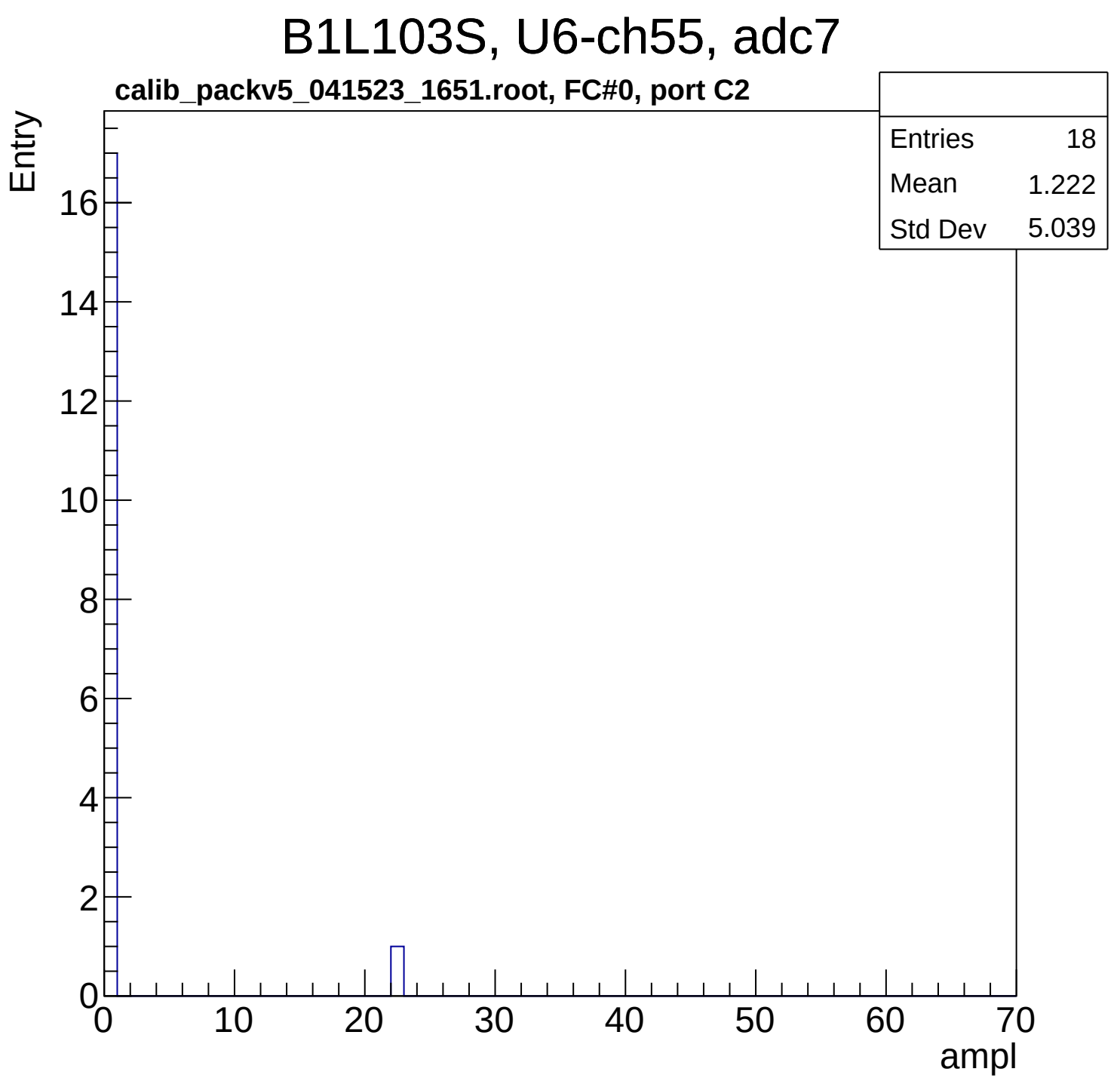

B1L103S, U6-ch55, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 57.64
Std Dev 16.02
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch55, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.222
Std Dev 5.039
Entry
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4
6
8
10
12
14
16
0
10
20
30
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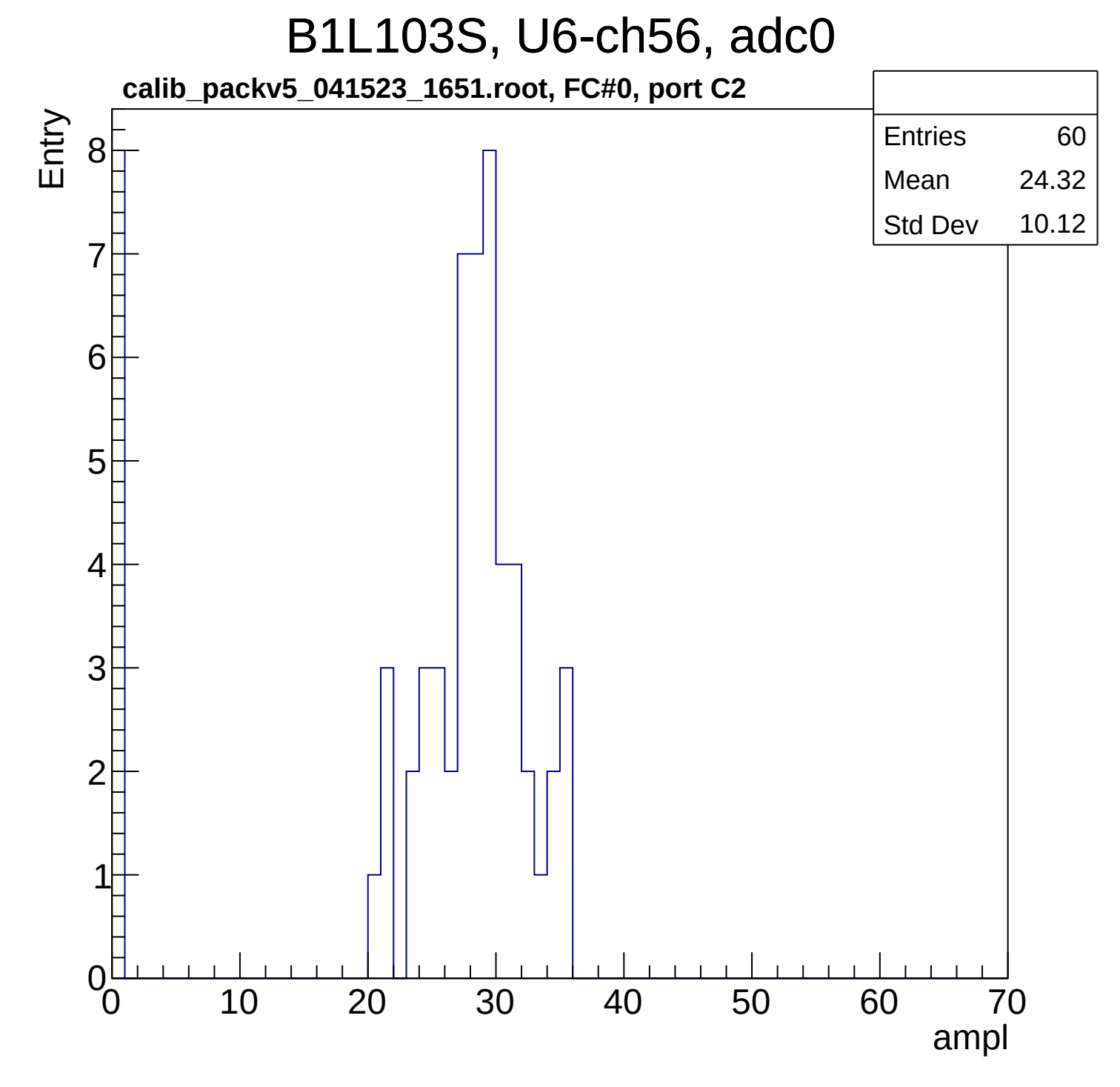
50
60
70
ampl


B1L103S, U6-ch56, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 24.32
Std Dev 10.12
Entry
ampl
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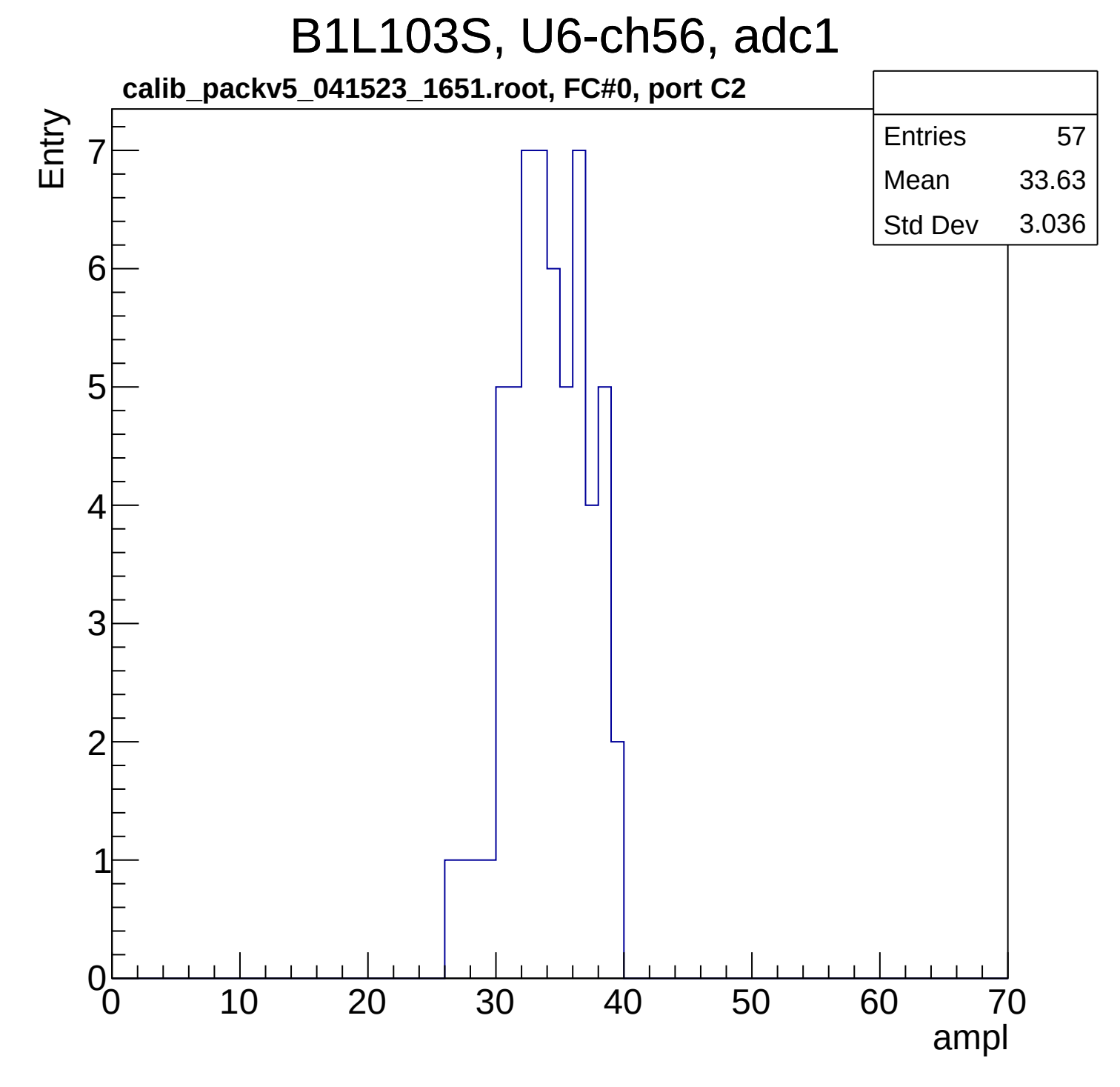
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch56, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 33.63
Std Dev 3.036
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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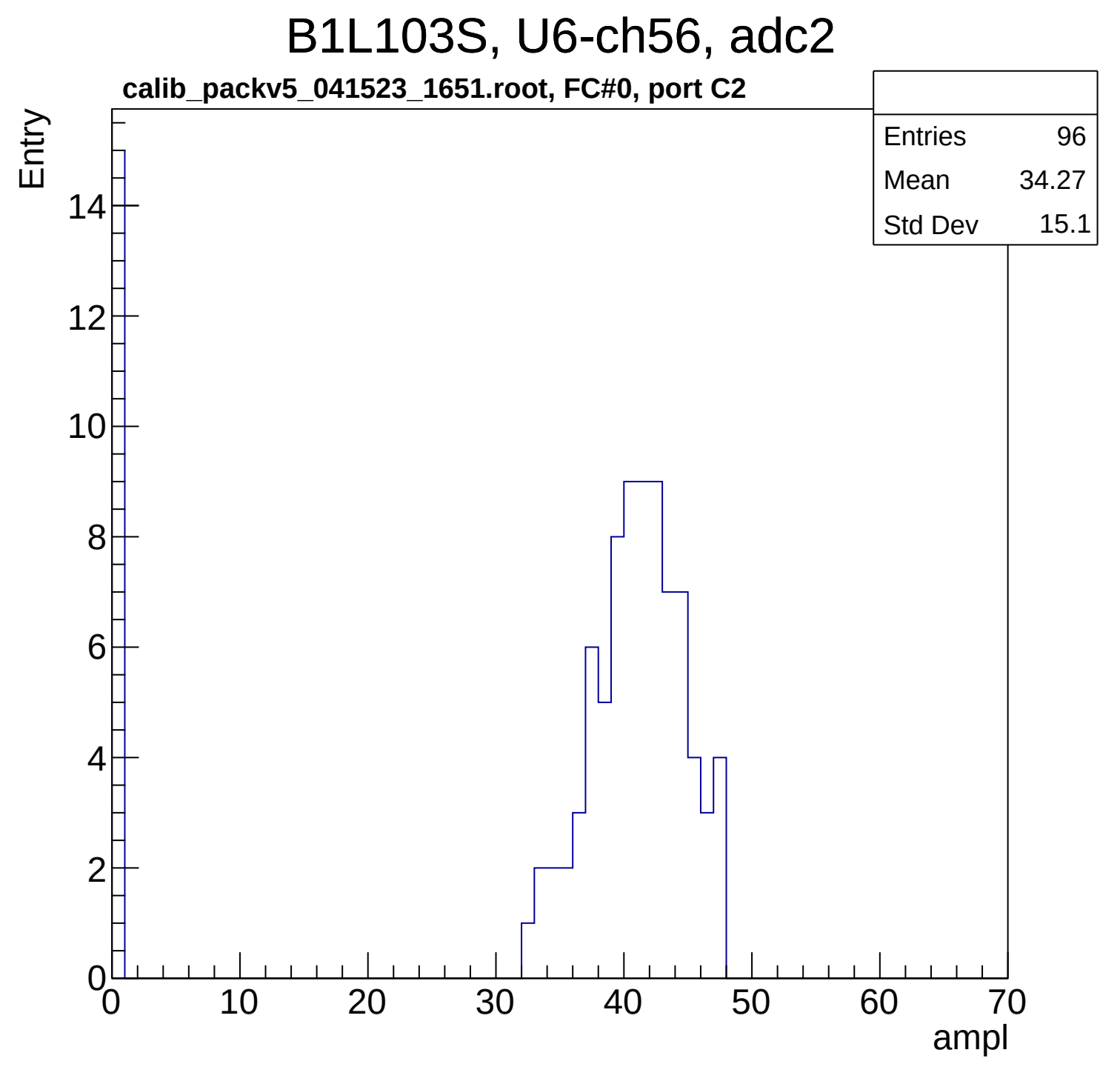
B1L103S, U6-ch56, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 96
Mean 34.27
Std Dev 15.1
Entry
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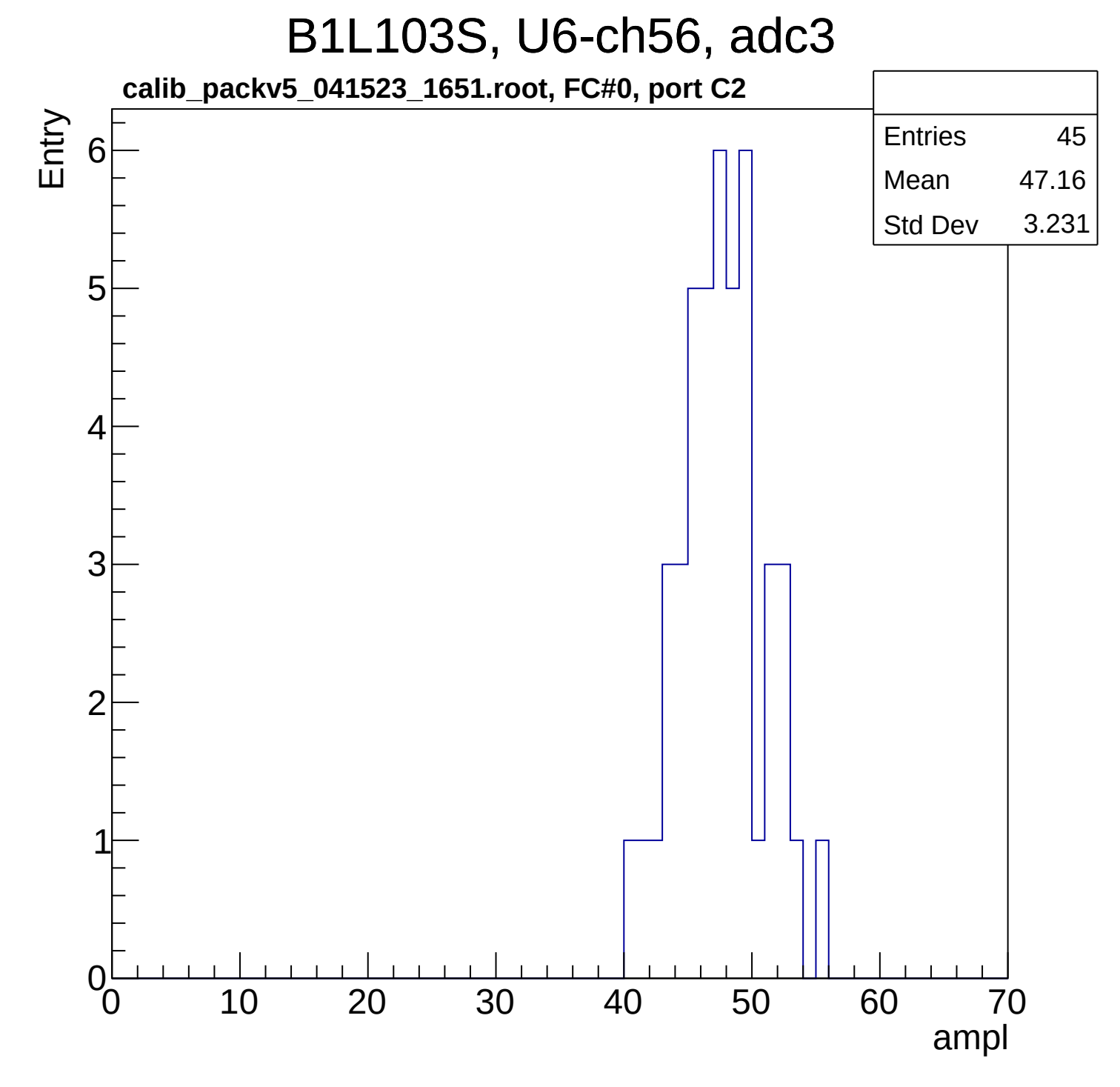
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch56, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 47.16
Std Dev 3.231
Entry
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2
3
4
5
6
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10
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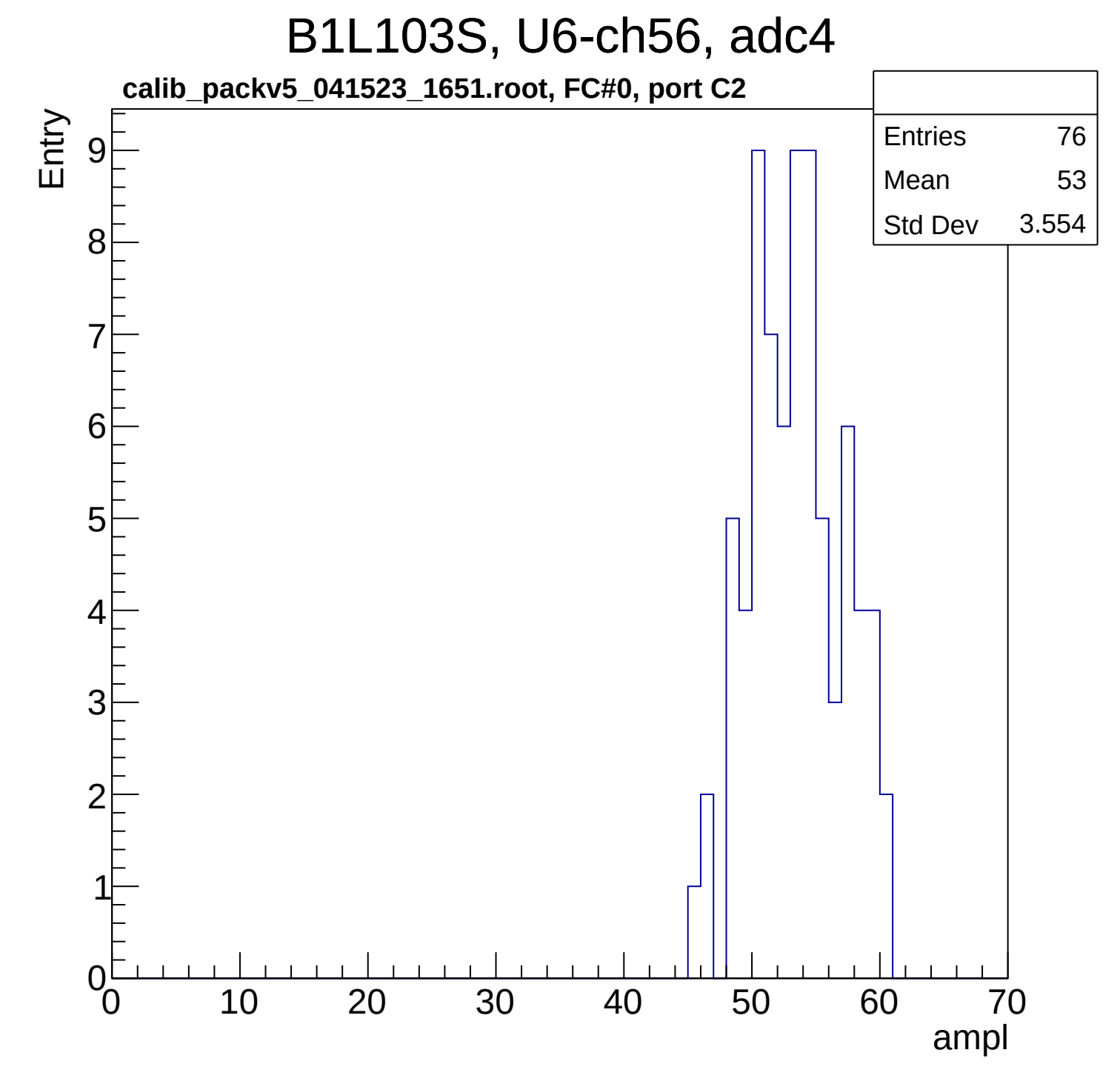
50
60
70
ampl


B1L103S, U6-ch56, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 53
Std Dev 3.554
Entry
ampl
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3
4
5
6
7
8
9
0
10
20
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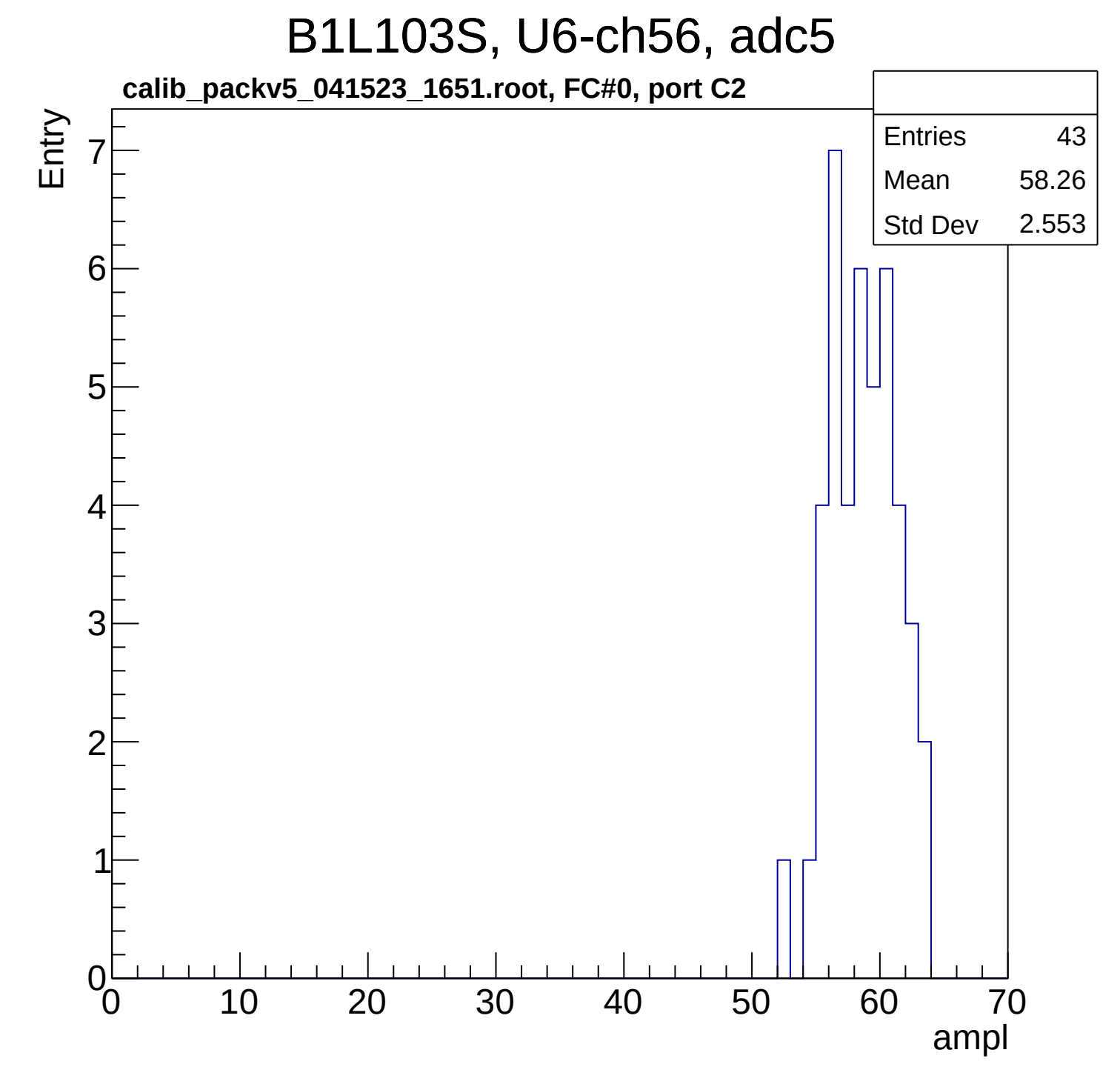
40
50
60
70


B1L103S, U6-ch56, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 58.26
Std Dev 2.553
Entry
ampl
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1
2
3
4
5
6
7
0
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40
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60
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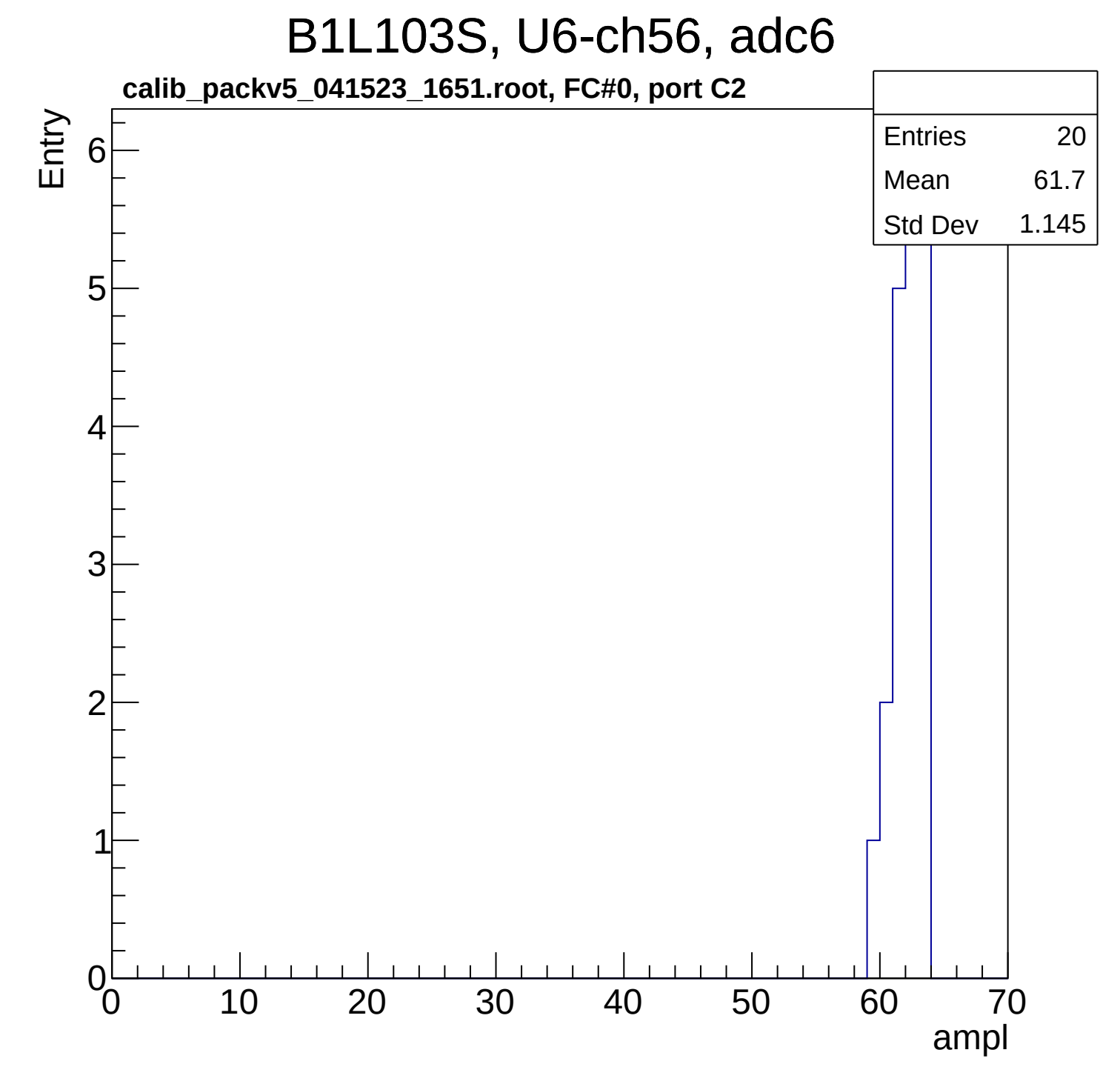
B1L103S, U6-ch56, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 61.7
Std Dev 1.145
Entry
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2
3
4
5
6
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10
20
30
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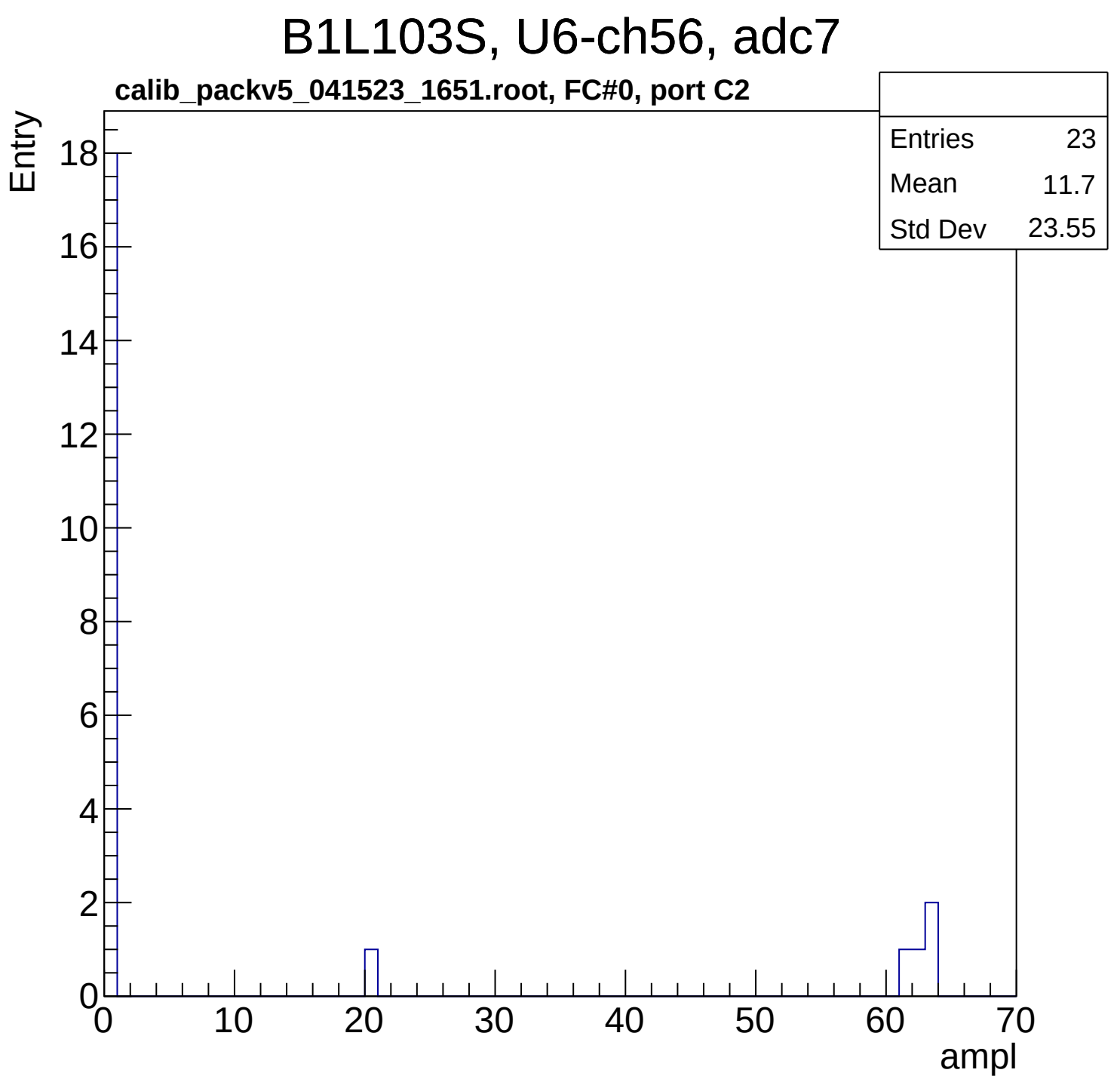
50
60
70
ampl


B1L103S, U6-ch56, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 11.7
Std Dev 23.55
Entry
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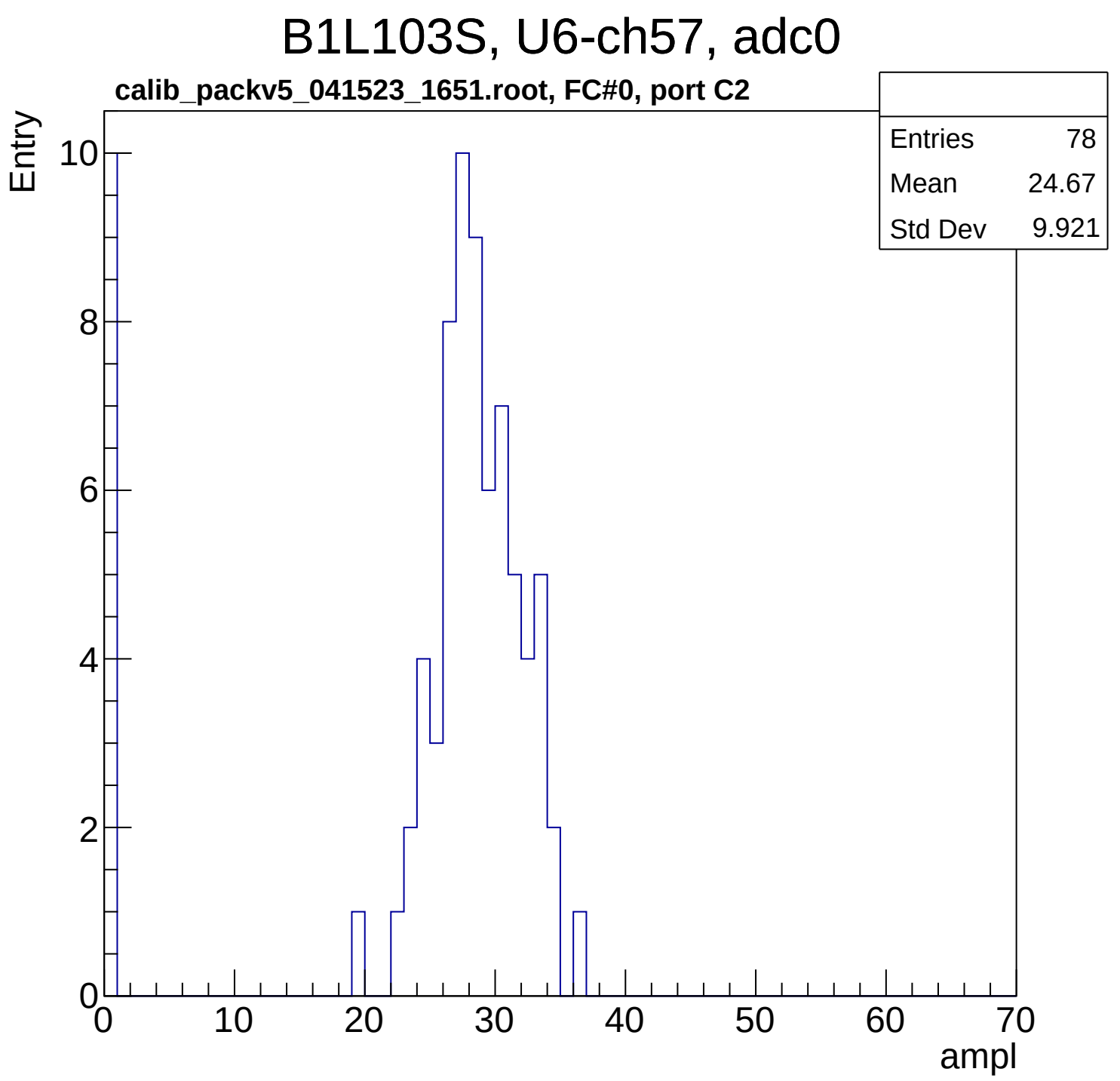
60
70
ampl


B1L103S, U6-ch57, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 24.67
Std Dev 9.921
Entry
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8
10
0
10
20
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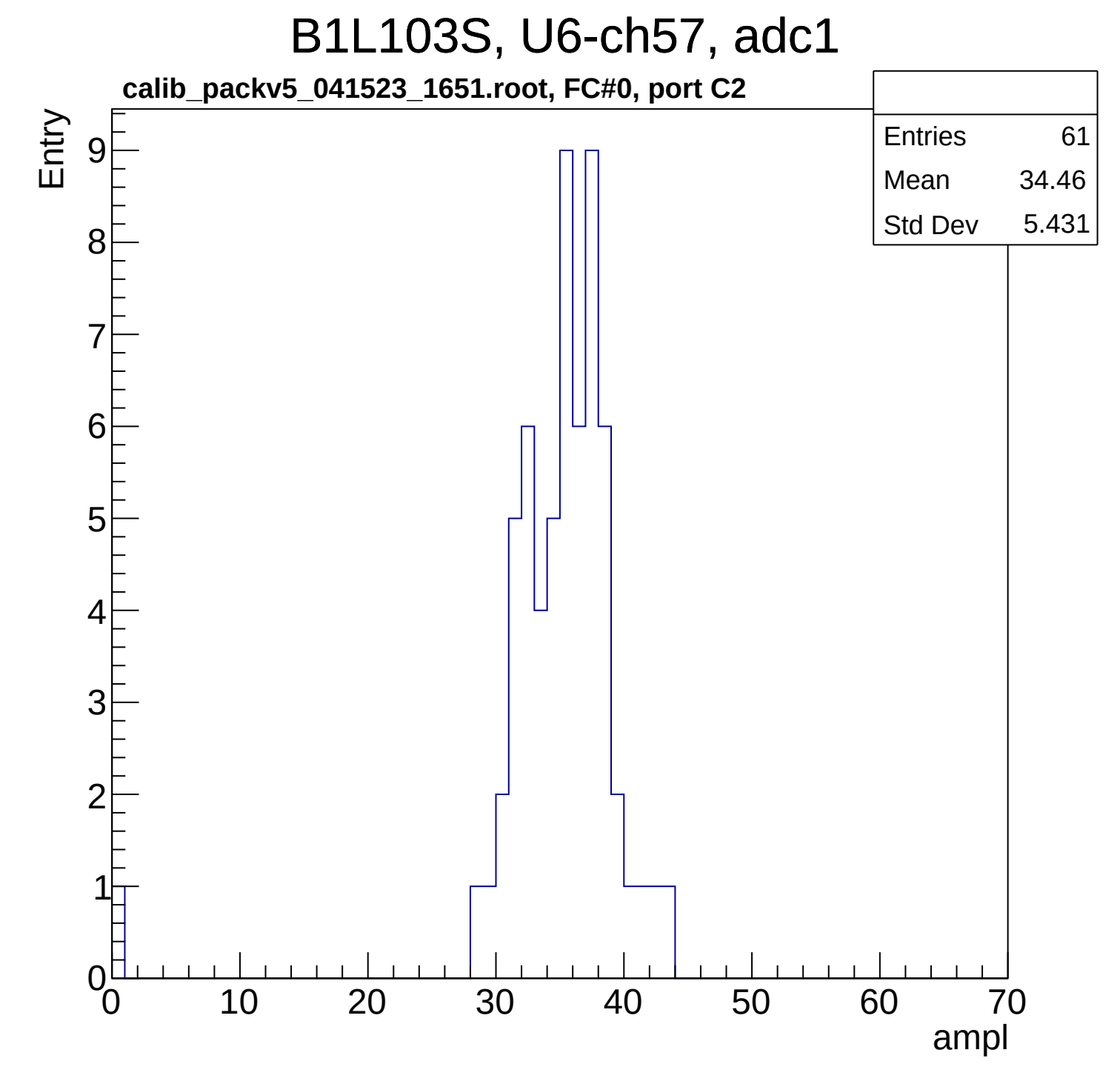
50
60
70
ampl


B1L103S, U6-ch57, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 34.46
Std Dev 5.431
Entry
ampl
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4
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6
7
8
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0
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60
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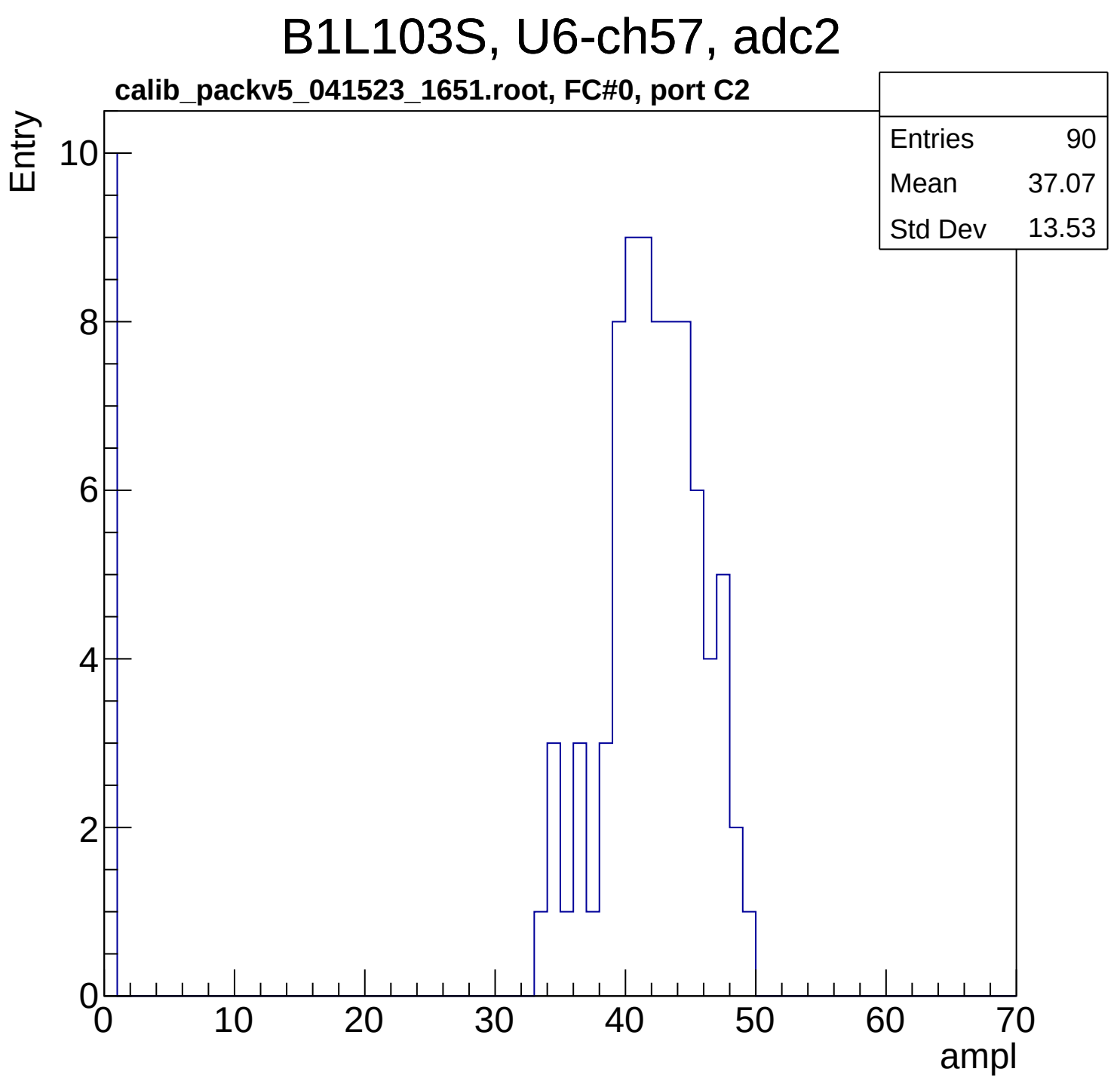
B1L103S, U6-ch57, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 37.07
Std Dev 13.53
Entry
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6
8
10
0
10
20
30
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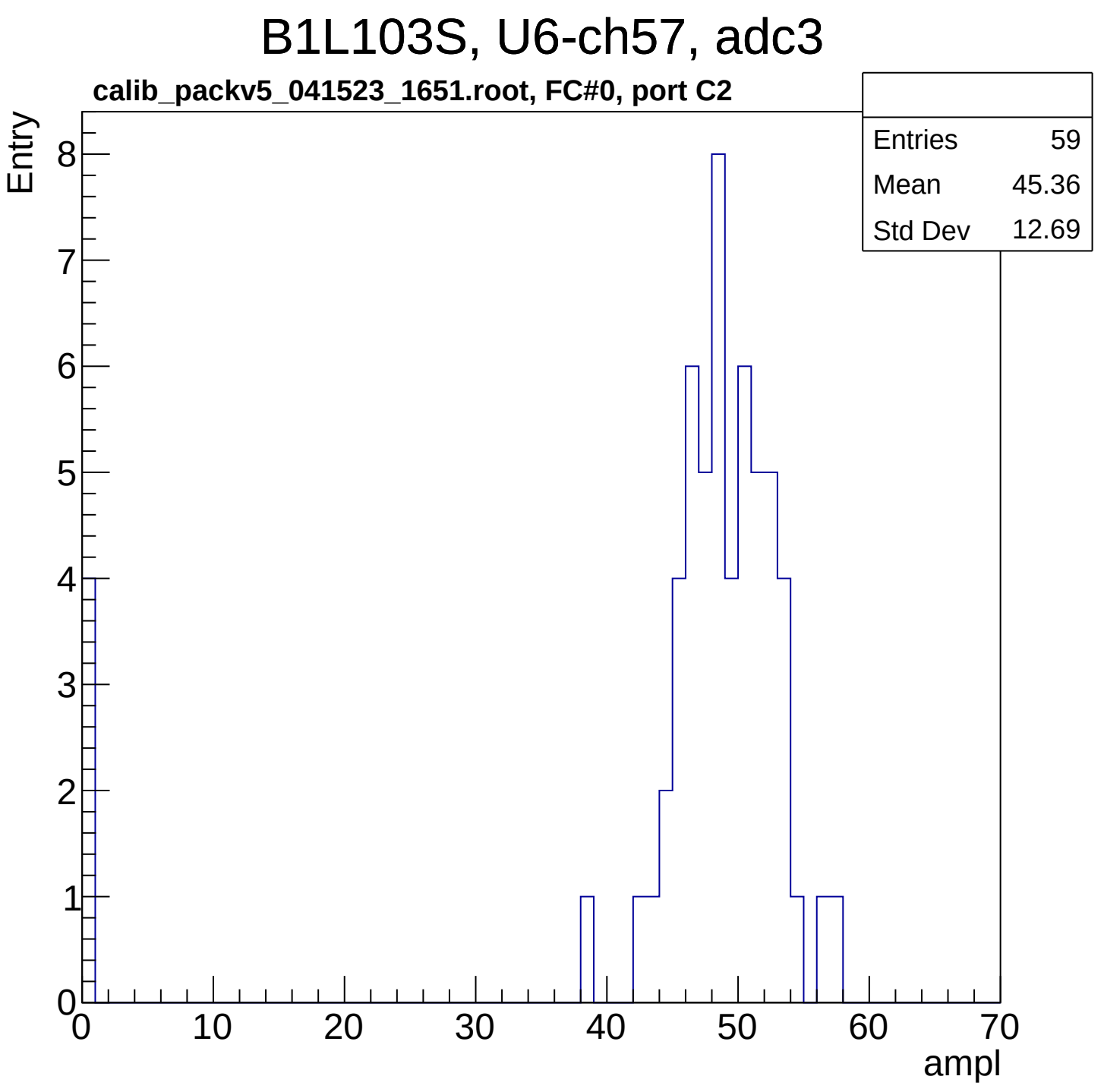
50
60
70
ampl


B1L103S, U6-ch57, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 45.36
Std Dev 12.69
Entry
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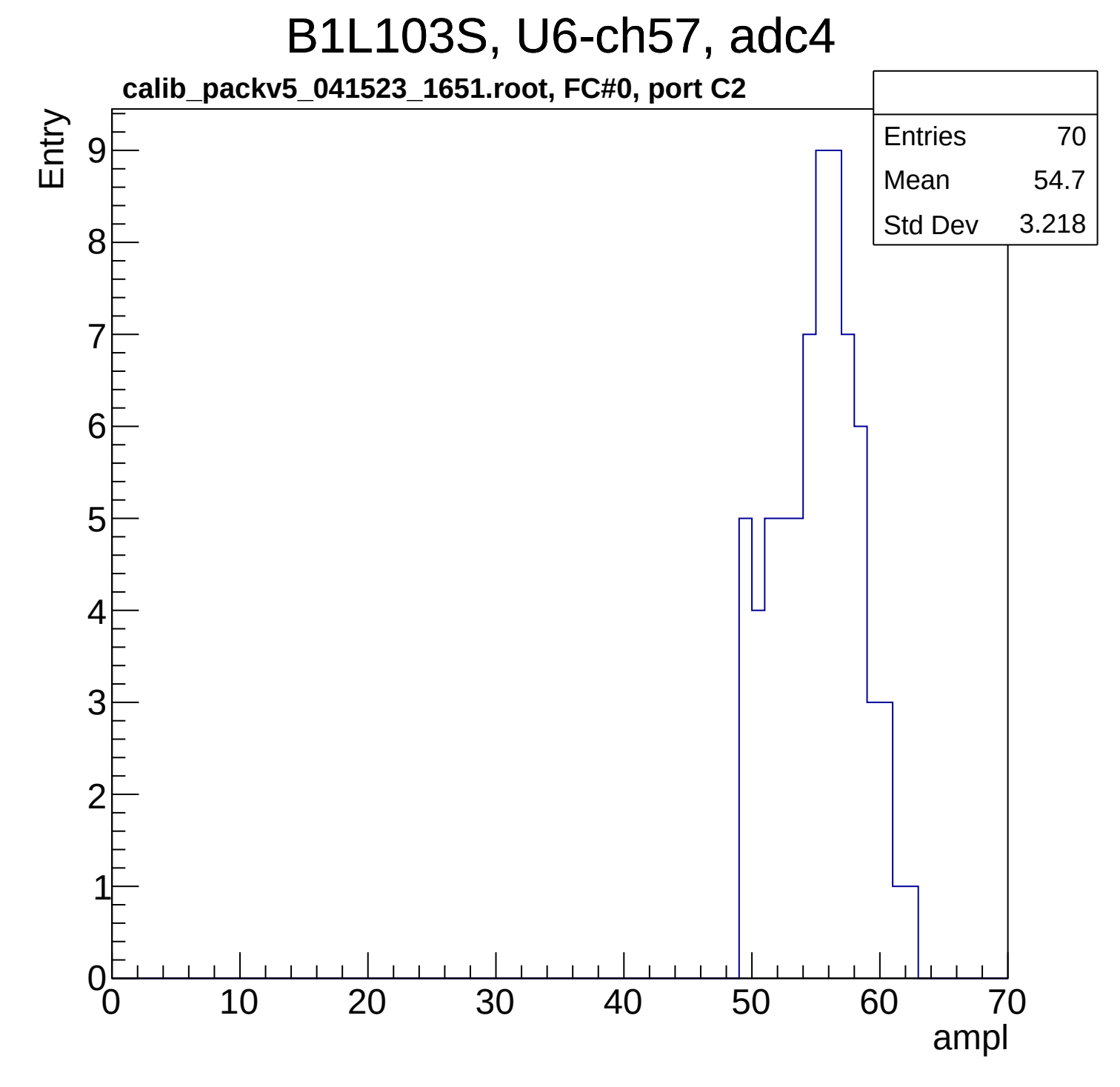
B1L103S, U6-ch57, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 54.7
Std Dev 3.218
Entry
ampl
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3
4
5
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7
8
9
0
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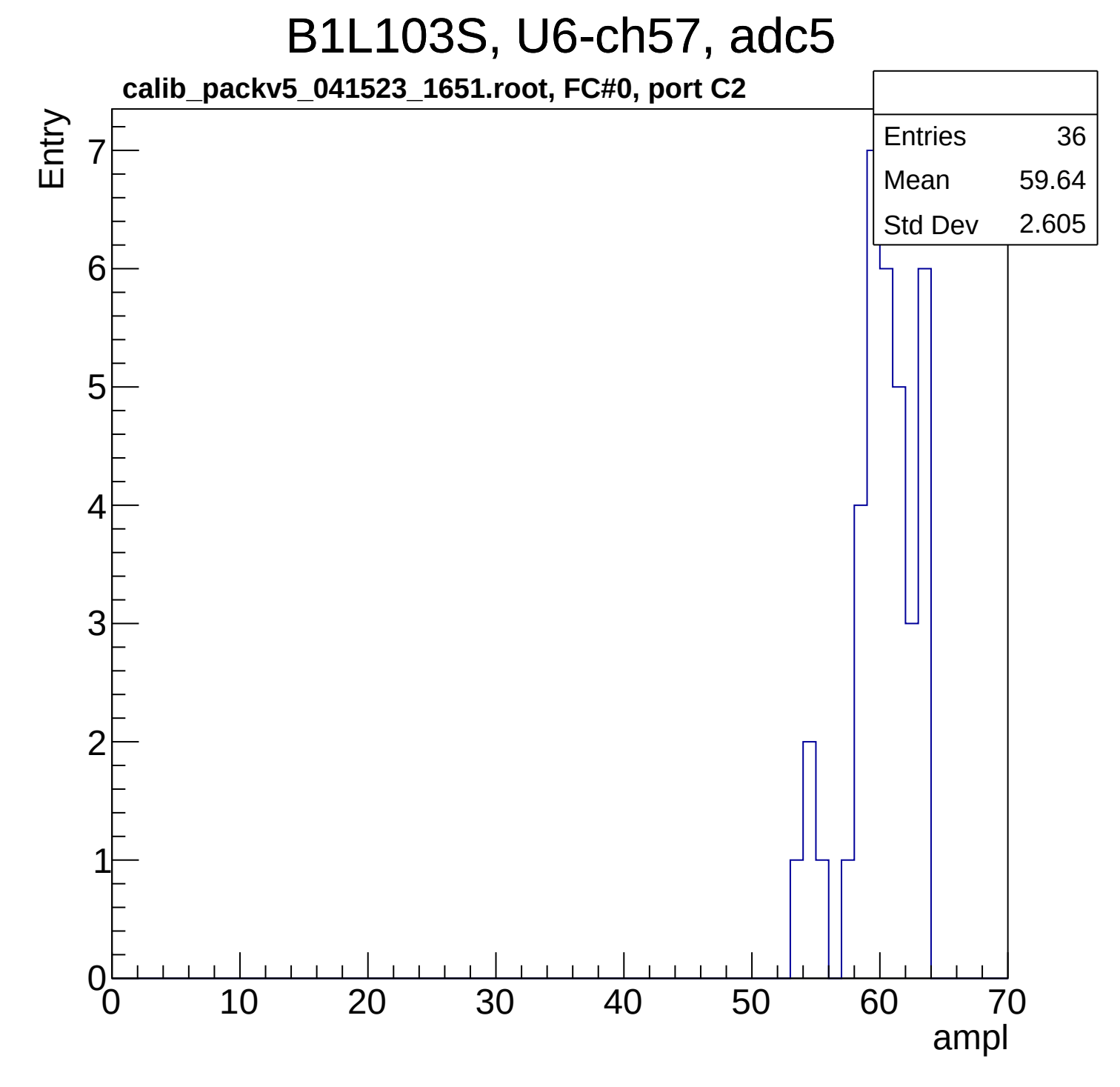
B1L103S, U6-ch57, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 59.64
Std Dev 2.605
Entry
ampl
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1
2
3
4
5
6
7
0
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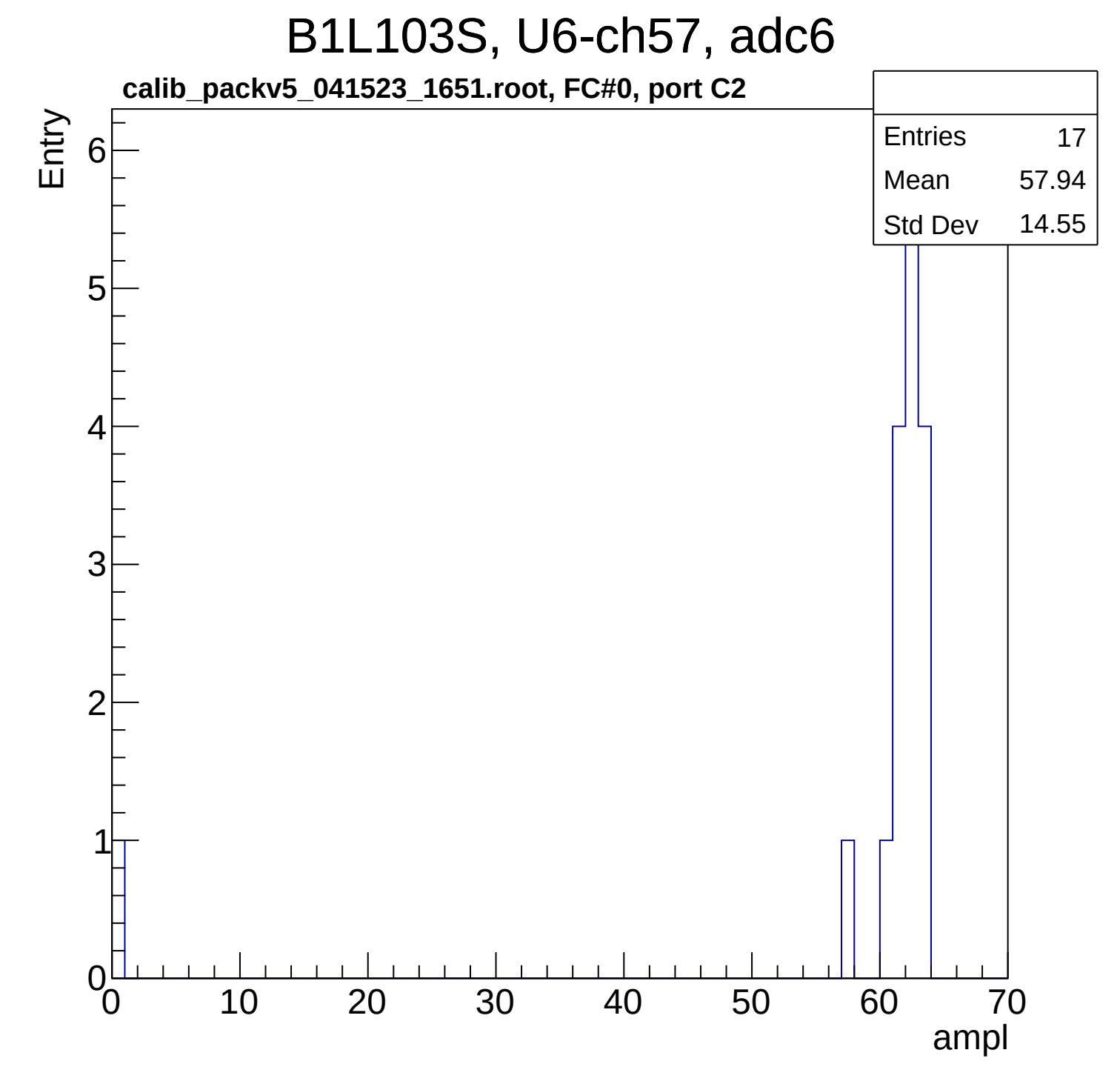
B1L103S, U6-ch57, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 57.94
Std Dev 14.55
Entry
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2
3
4
5
6
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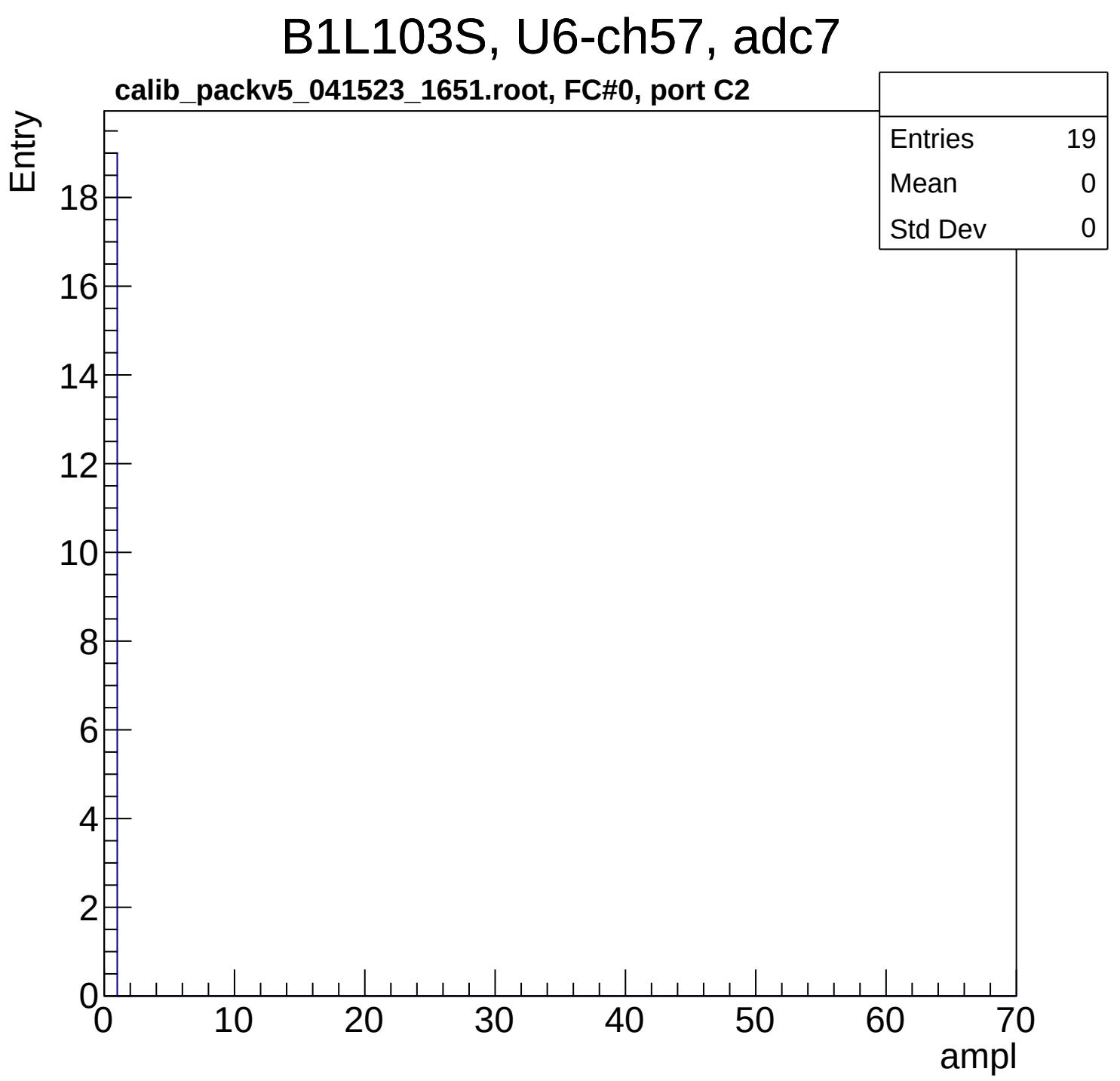
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch57, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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4
6
8
10
12
14
16
18
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10
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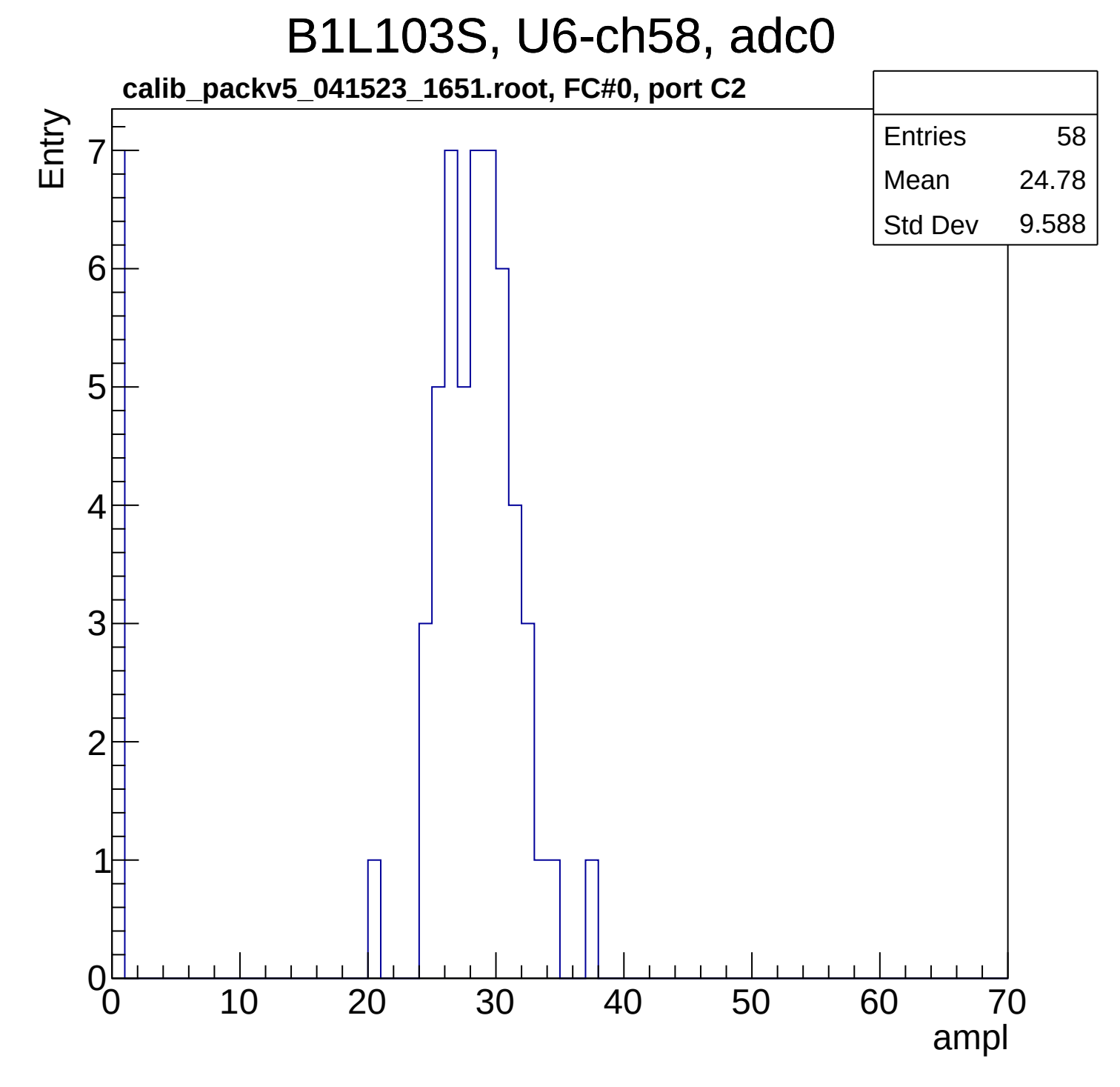
50
60
70
ampl


B1L103S, U6-ch58, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 24.78
Std Dev 9.588
Entry
ampl
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2
3
4
5
6
7
0
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60
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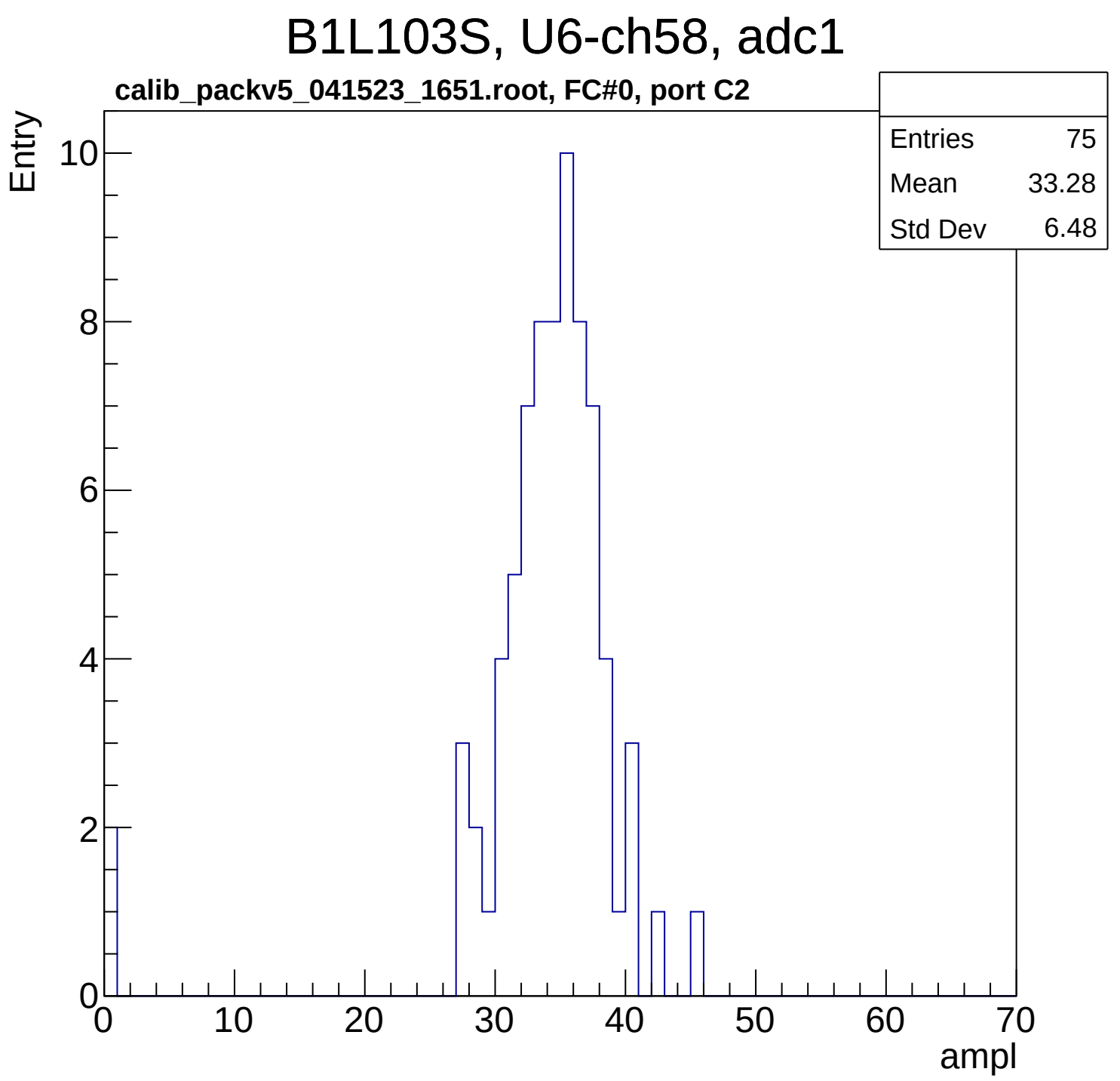
B1L103S, U6-ch58, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 33.28
Std Dev 6.48
Entry
ampl
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8
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0
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20
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40
50
60
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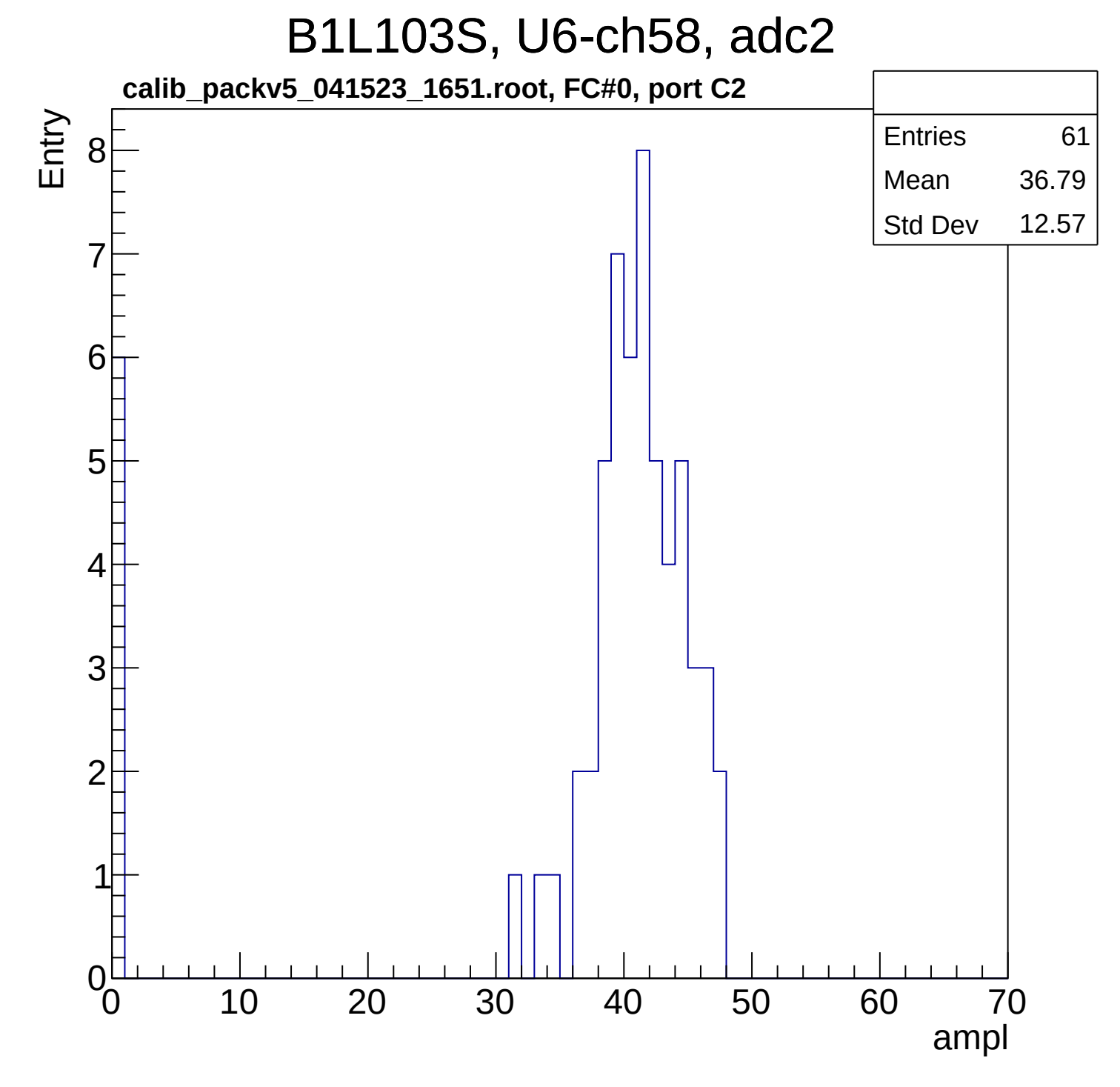
B1L103S, U6-ch58, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 36.79
Std Dev 12.57
Entry
ampl
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2
3
4
5
6
7
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0
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60
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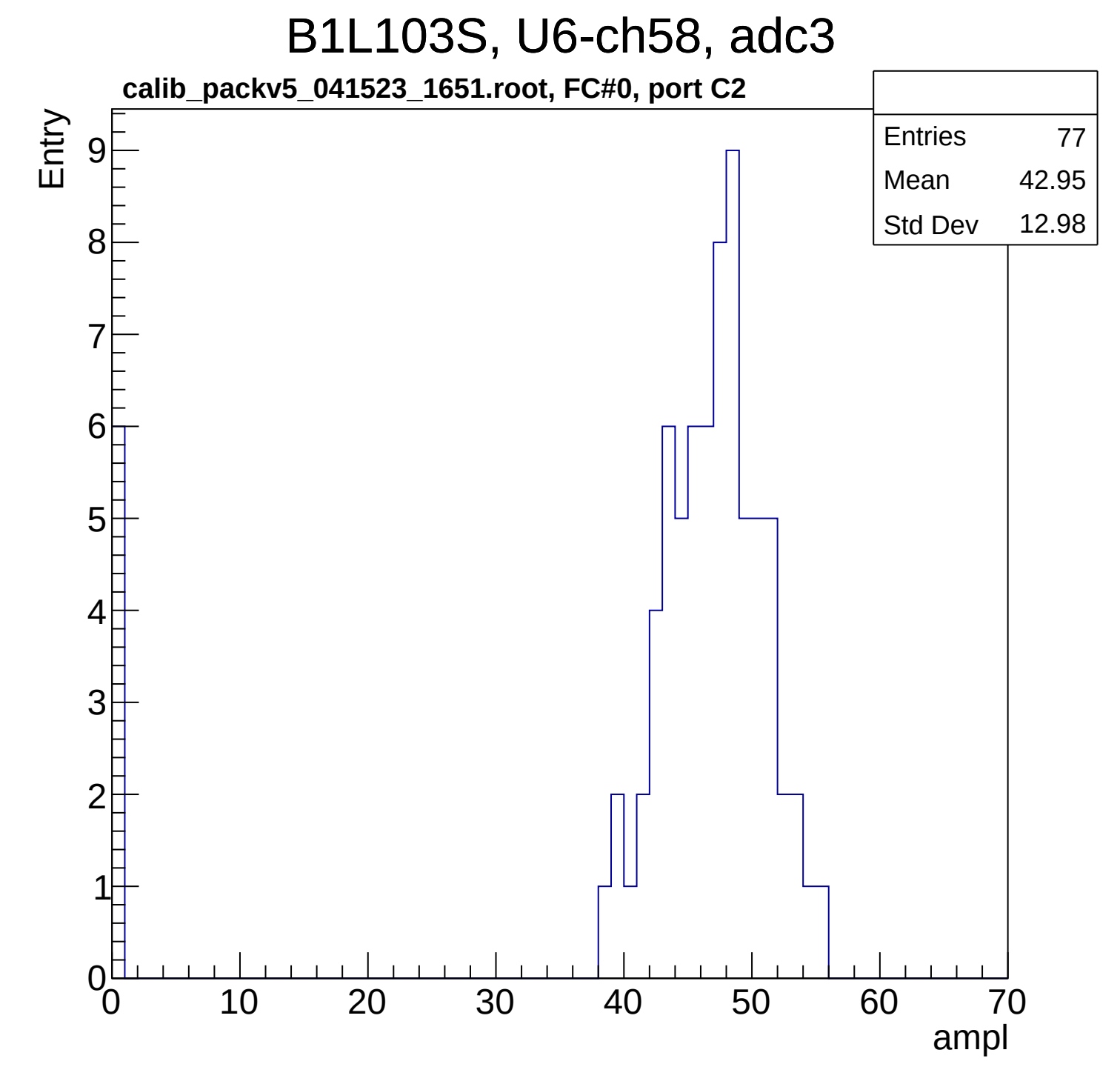
B1L103S, U6-ch58, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 42.95
Std Dev 12.98
Entry
ampl
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6
7
8
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0
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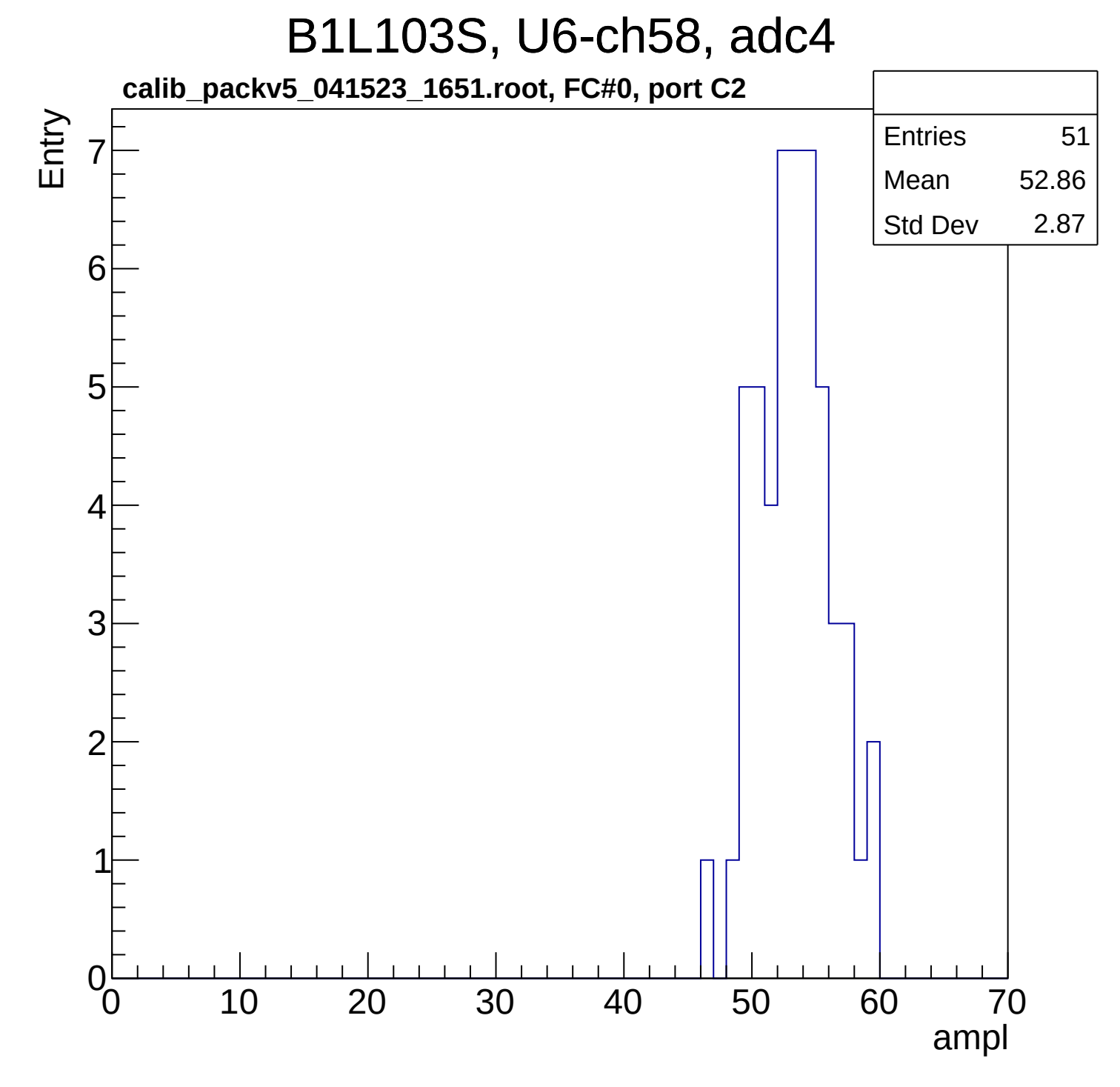
B1L103S, U6-ch58, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 52.86
Std Dev 2.87
Entry
ampl
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2
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4
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6
7
0
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40
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60
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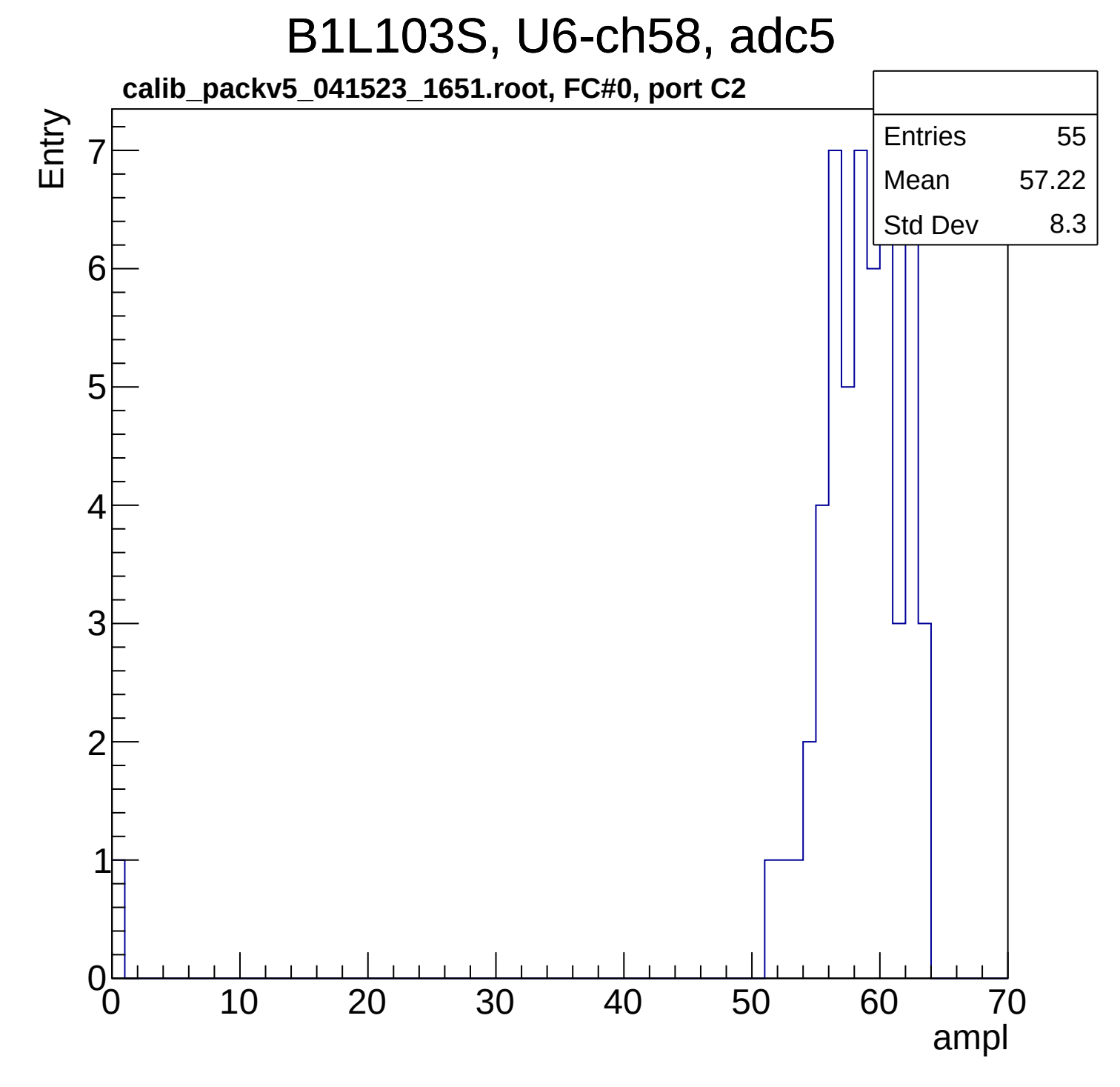
B1L103S, U6-ch58, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 57.22
Std Dev 8.3
Entry
ampl
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4
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60
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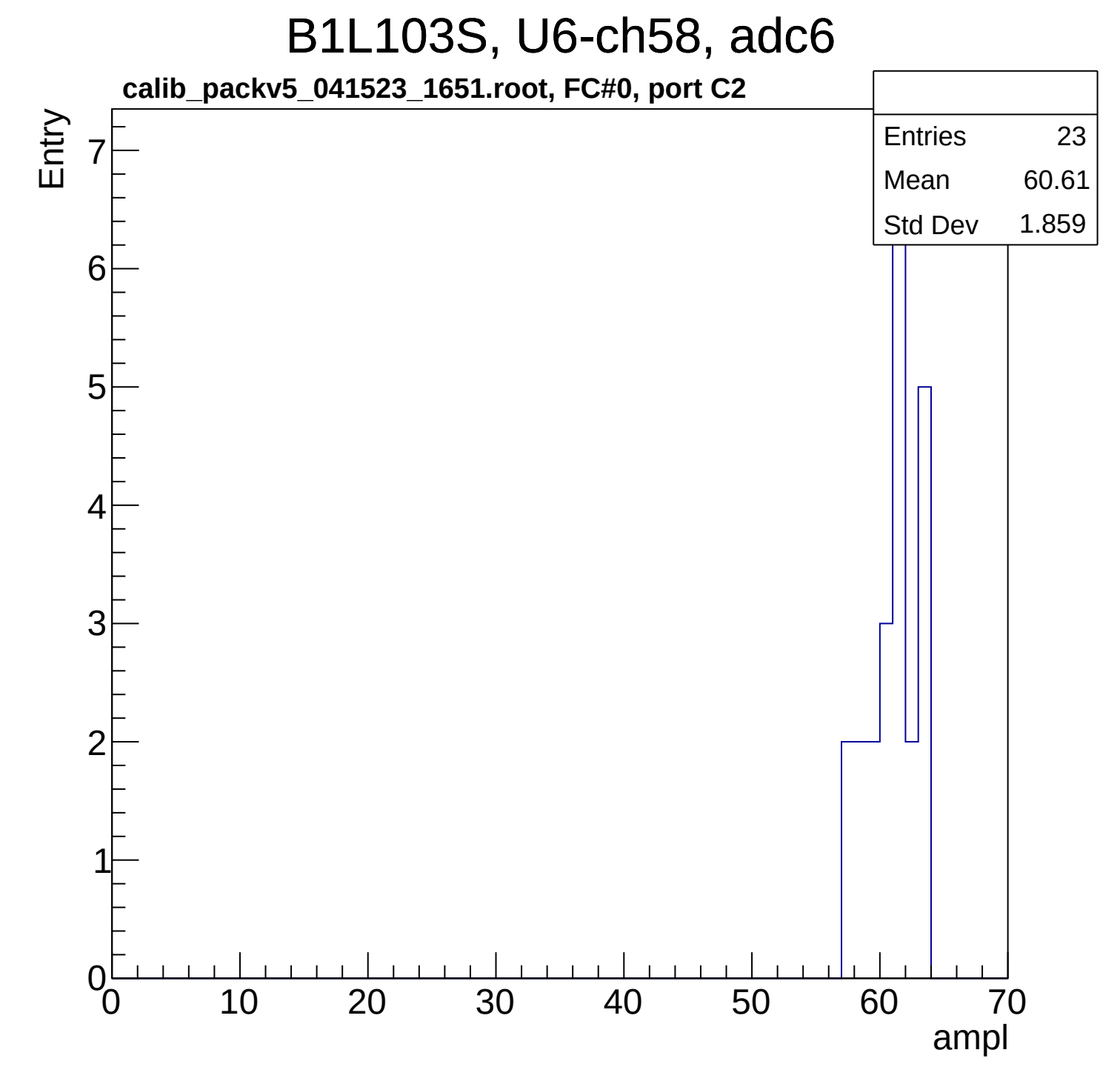
B1L103S, U6-ch58, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 60.61
Std Dev 1.859
Entry
ampl
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6
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0
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40
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60
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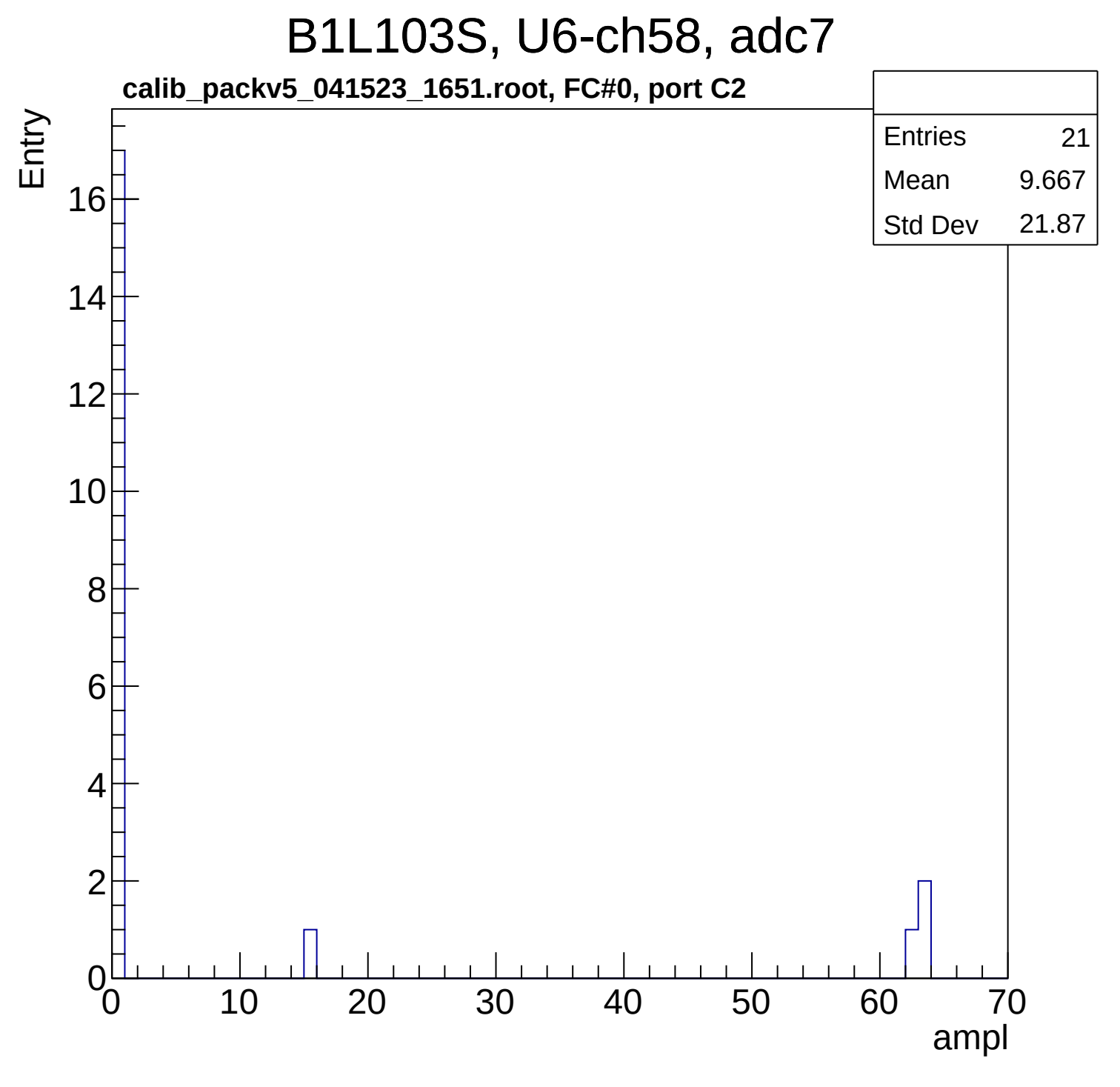
B1L103S, U6-ch58, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 9.667
Std Dev 21.87
Entry
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4
6
8
10
12
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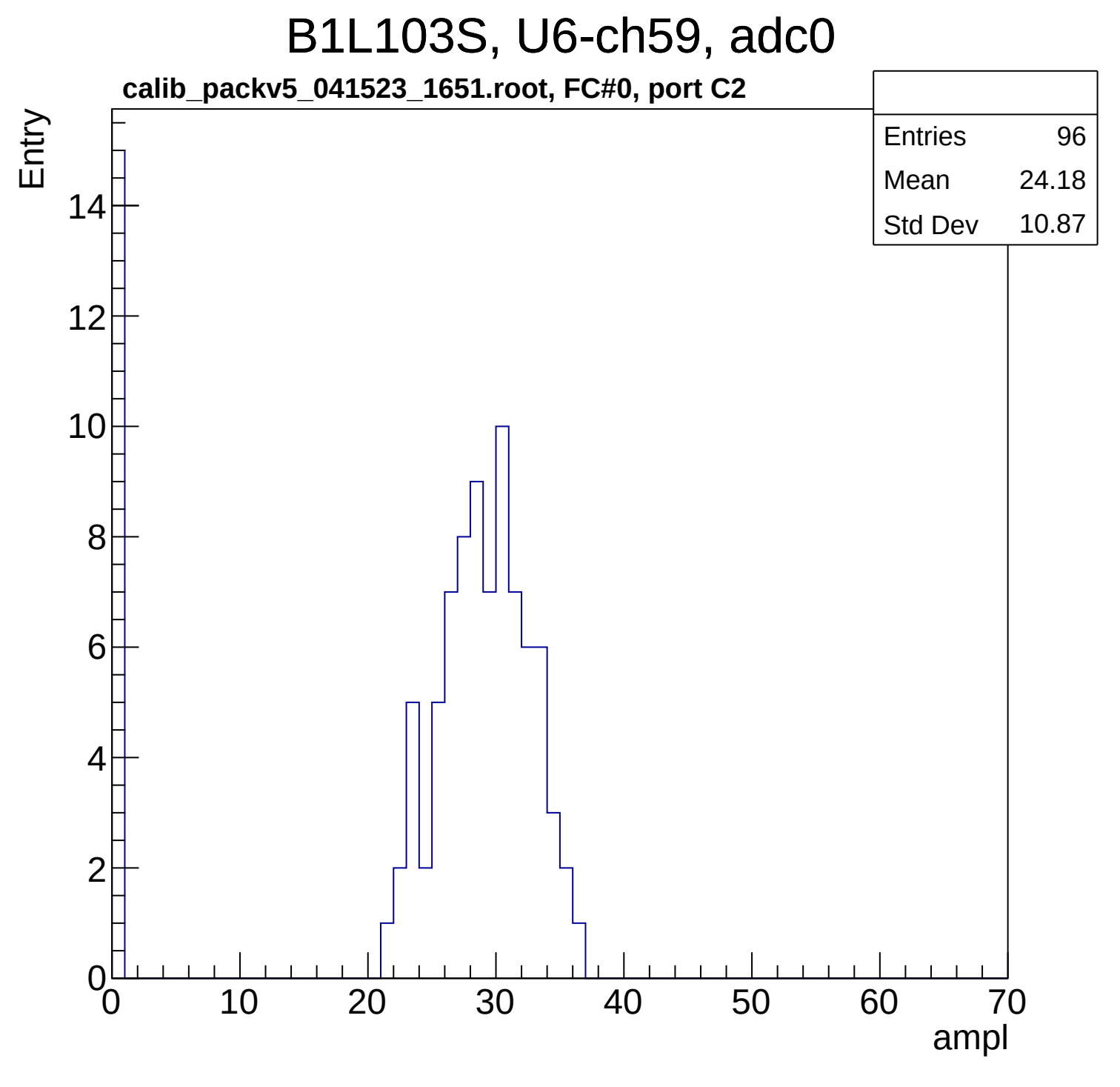
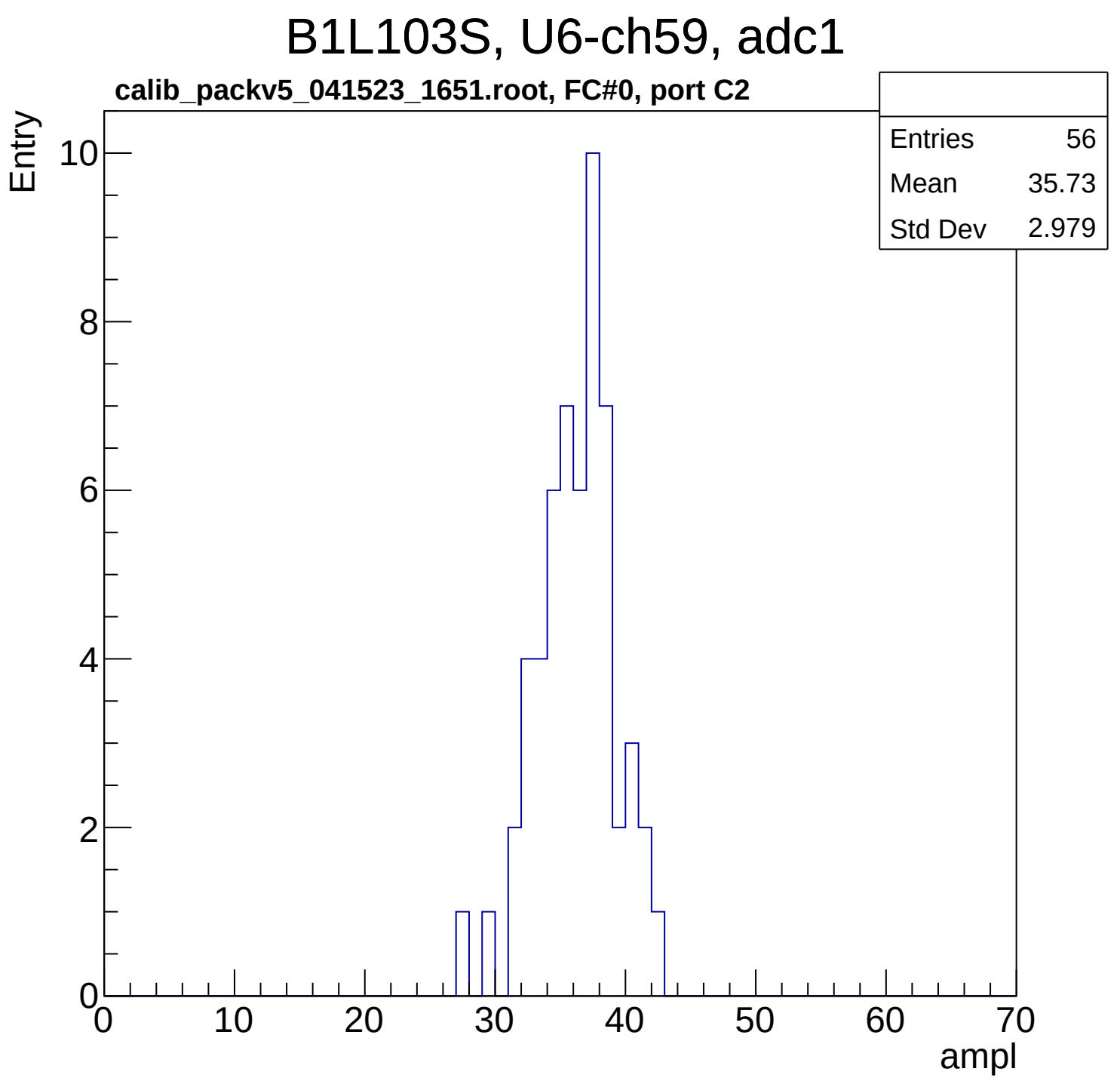
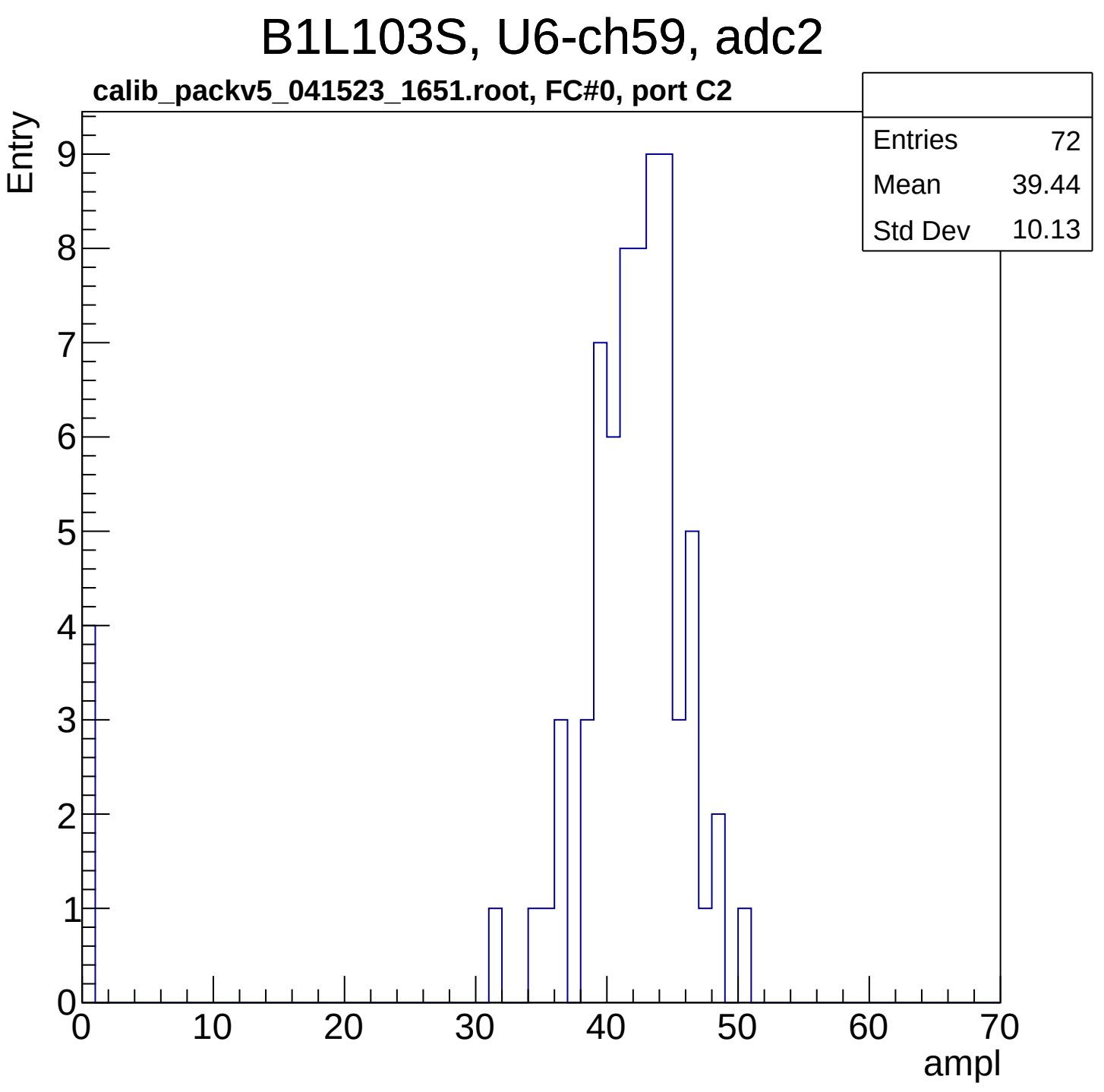
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch59, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 96
Mean 24.18
Std Dev 10.87
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch59, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 35.73
Std Dev 2.979
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U6-ch59, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 39.44
Std Dev 10.13
Entry
ampl
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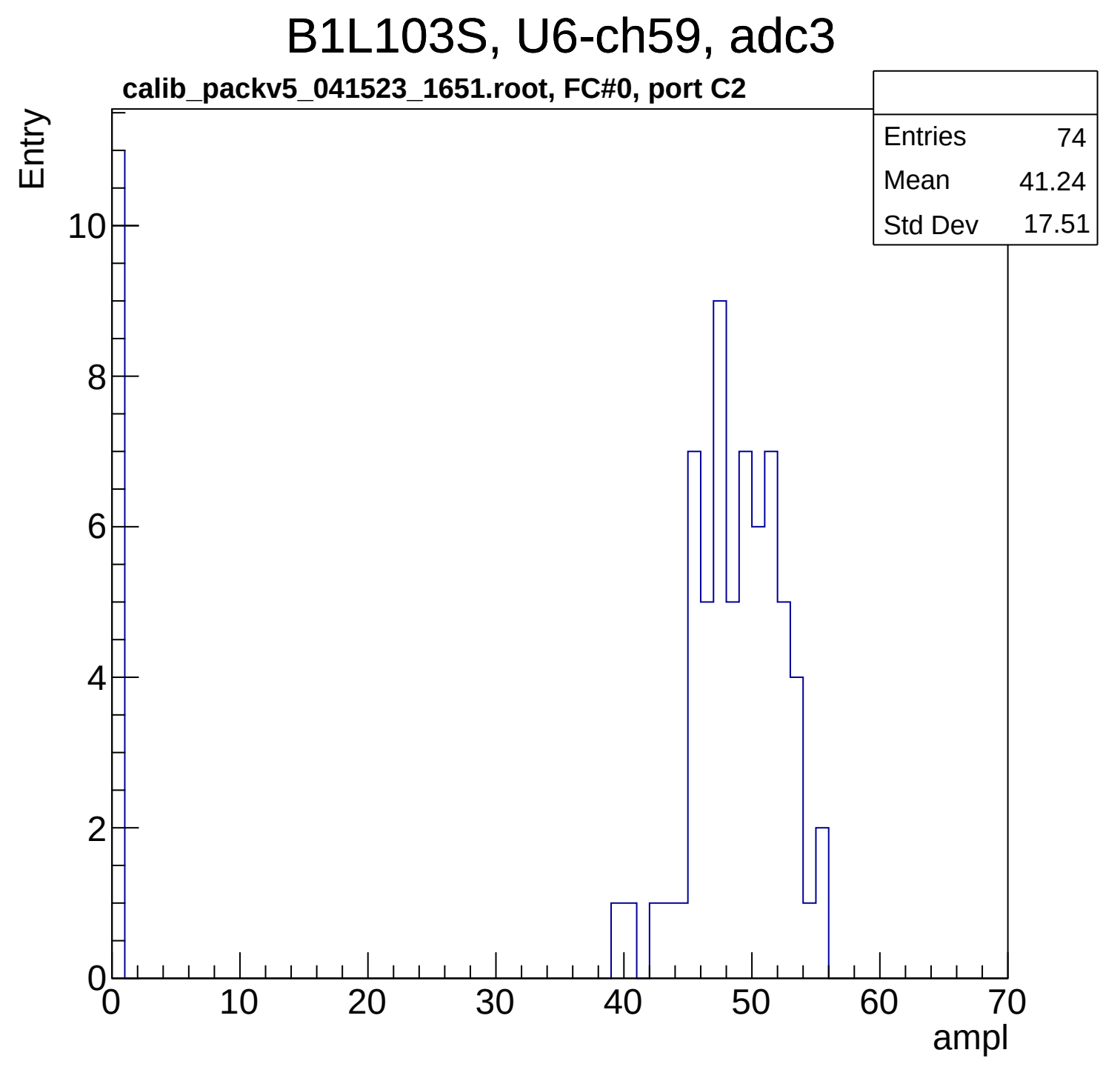
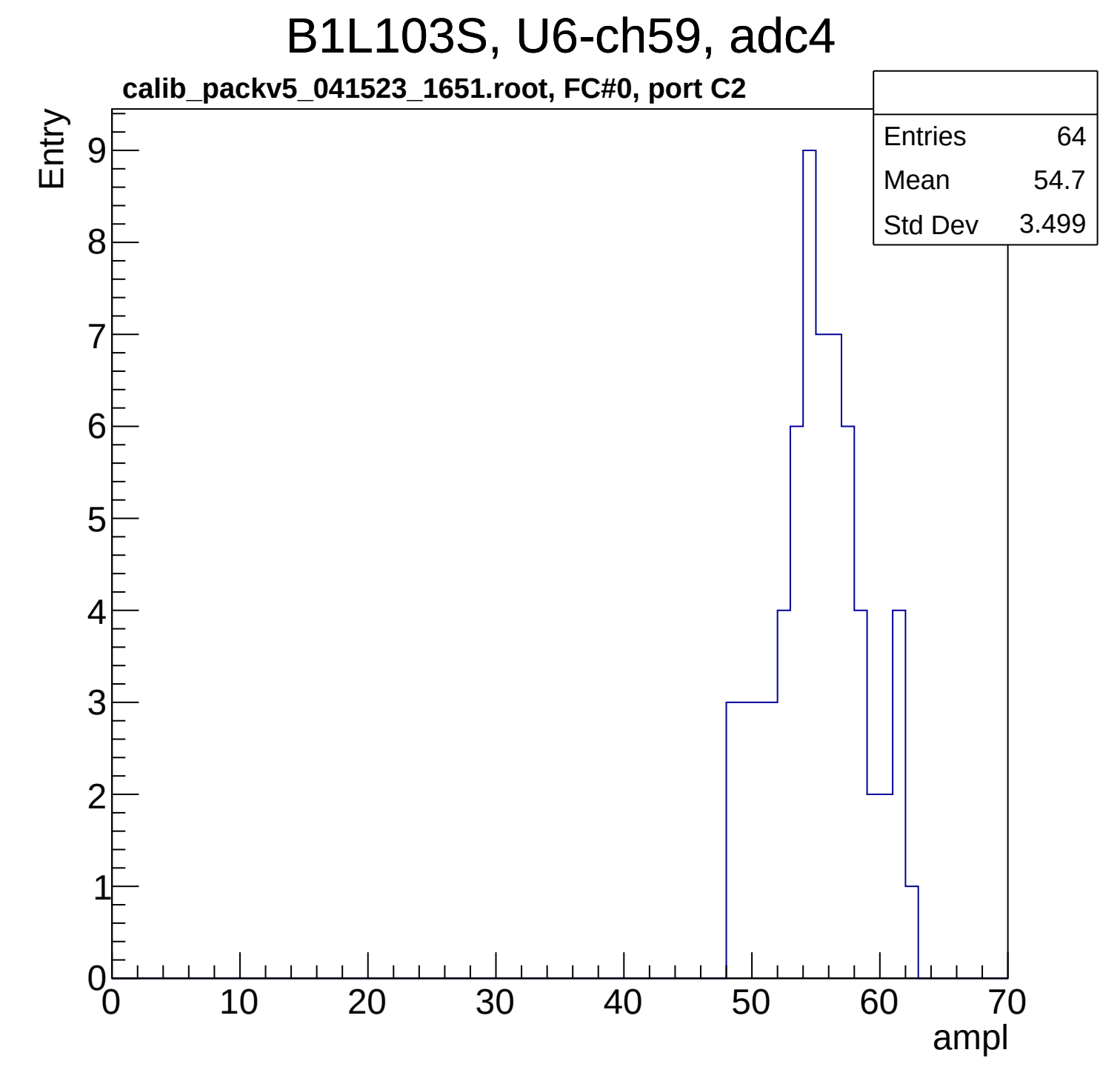
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch59, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 41.24
Std Dev 17.51
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch59, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 54.7
Std Dev 3.499
Entry
ampl
0
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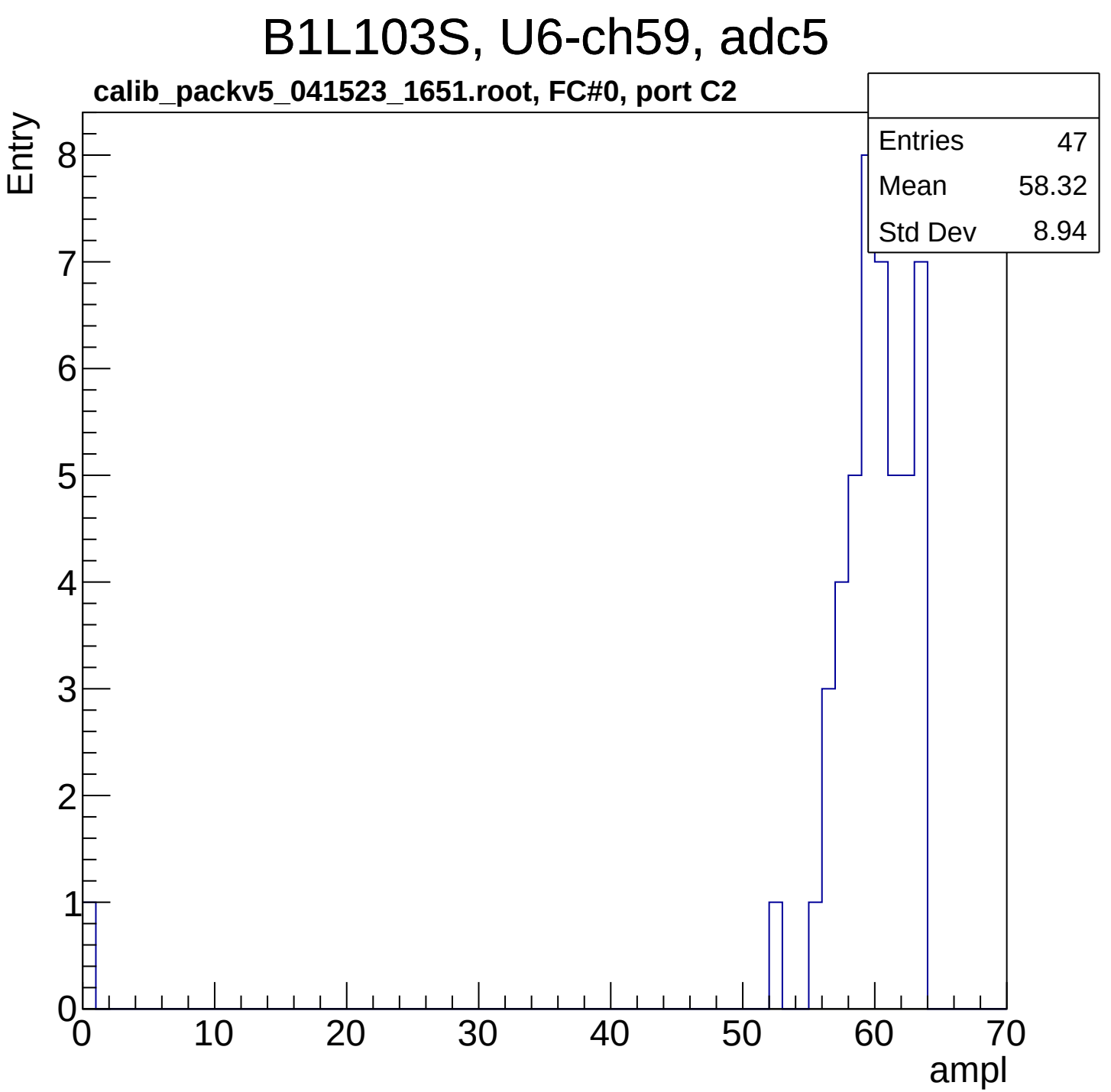
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch59, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 58.32
Std Dev 8.94
Entry
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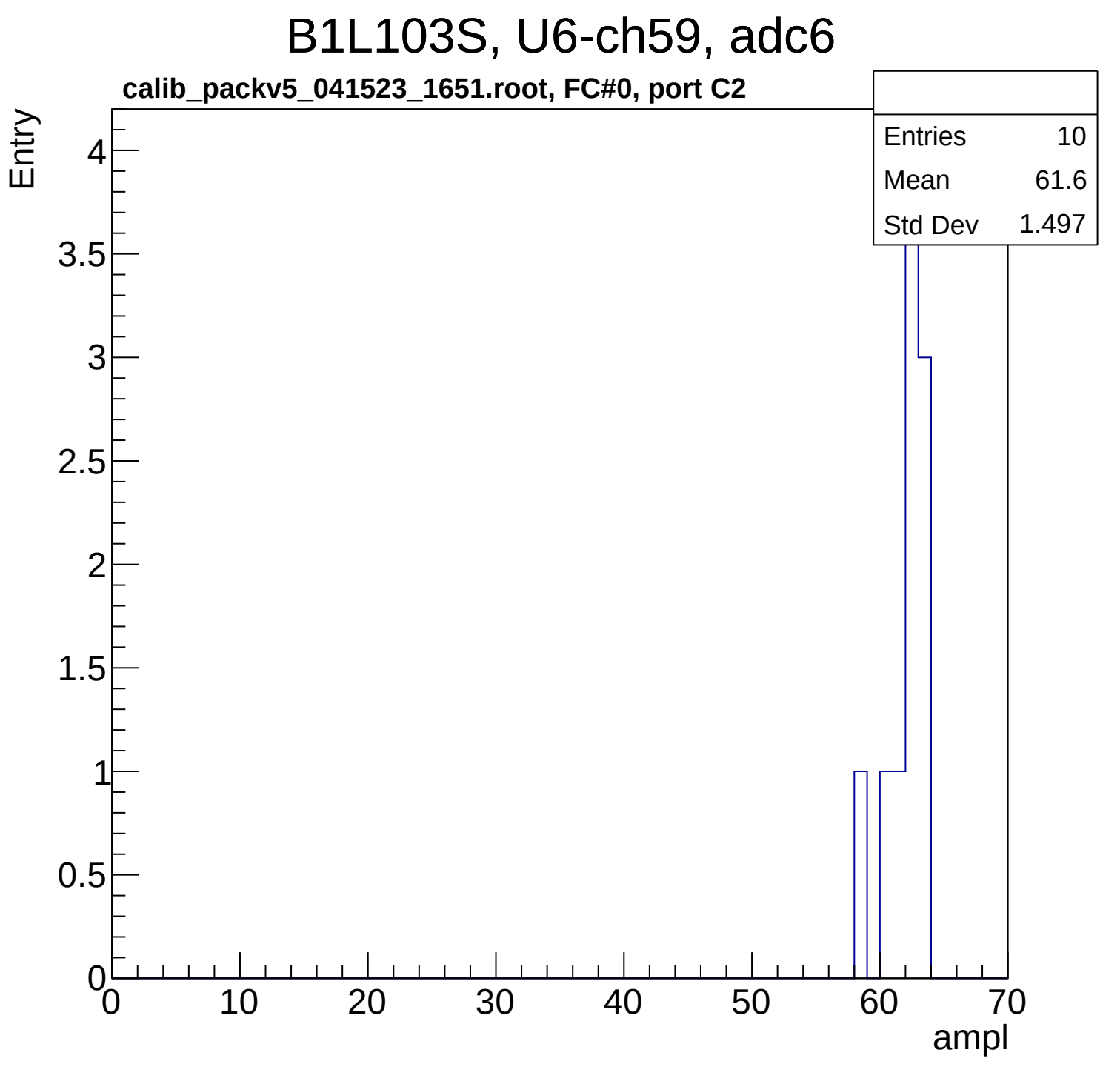
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch59, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61.6
Std Dev 1.497
Entry
ampl
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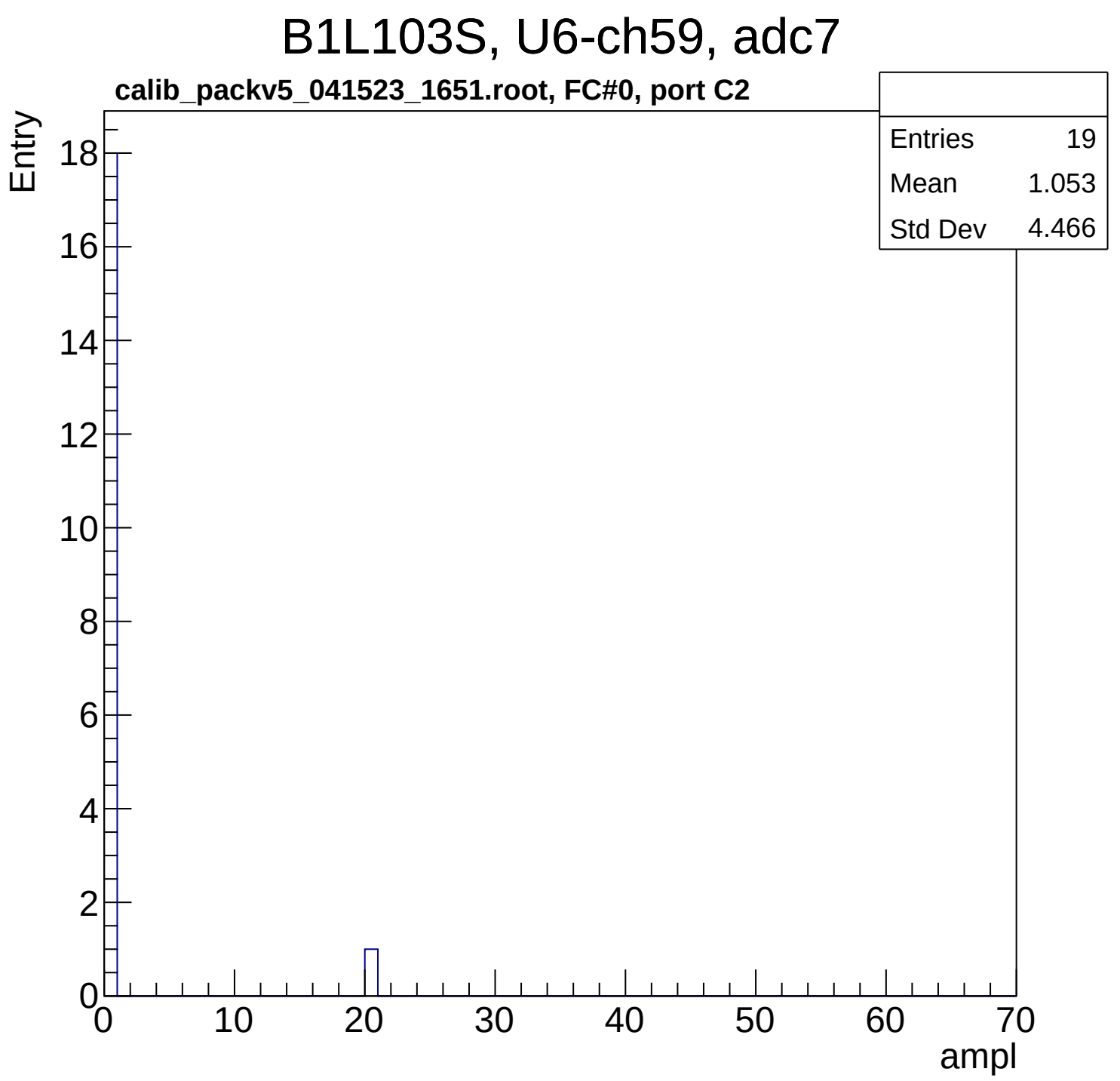
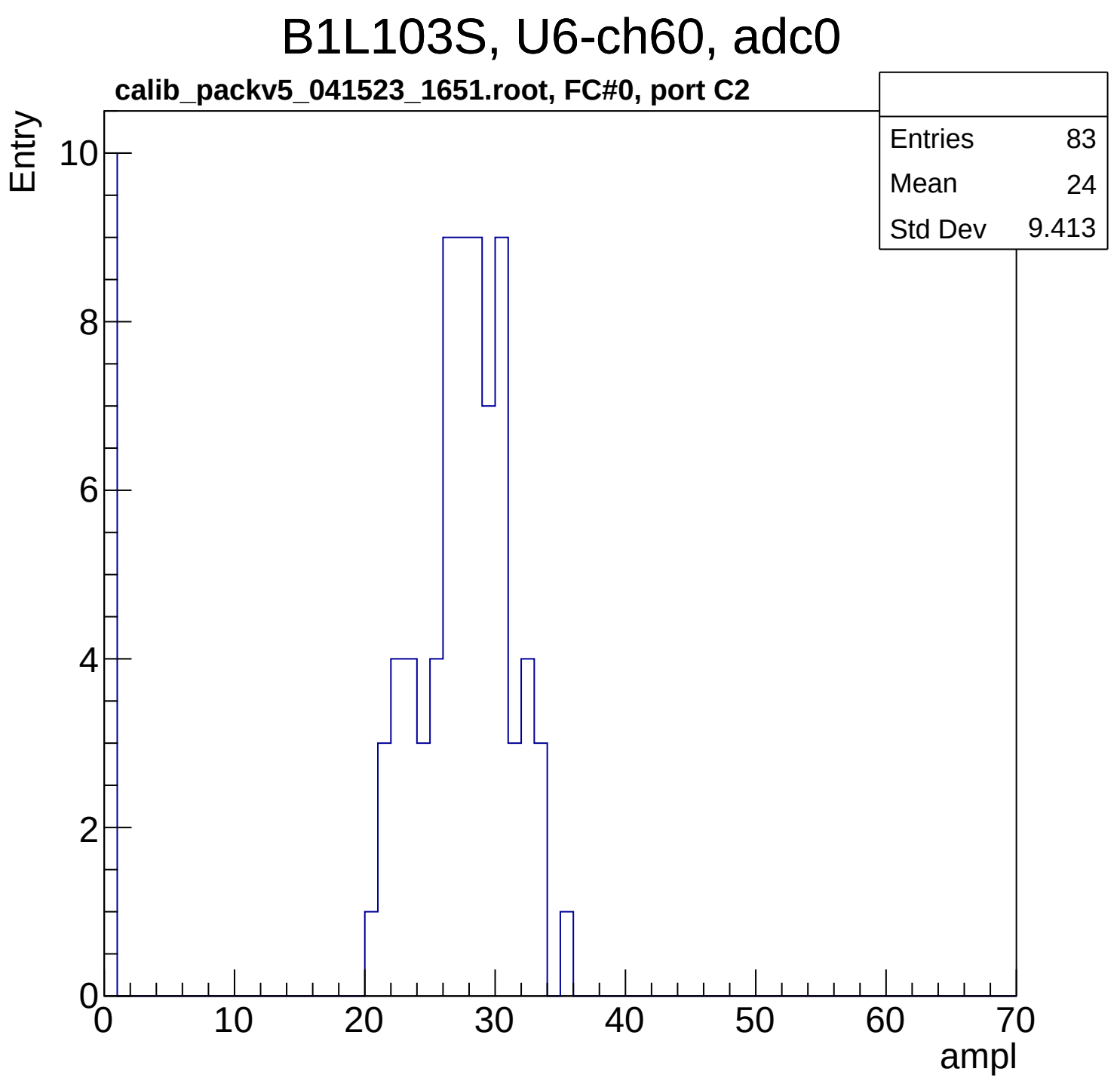
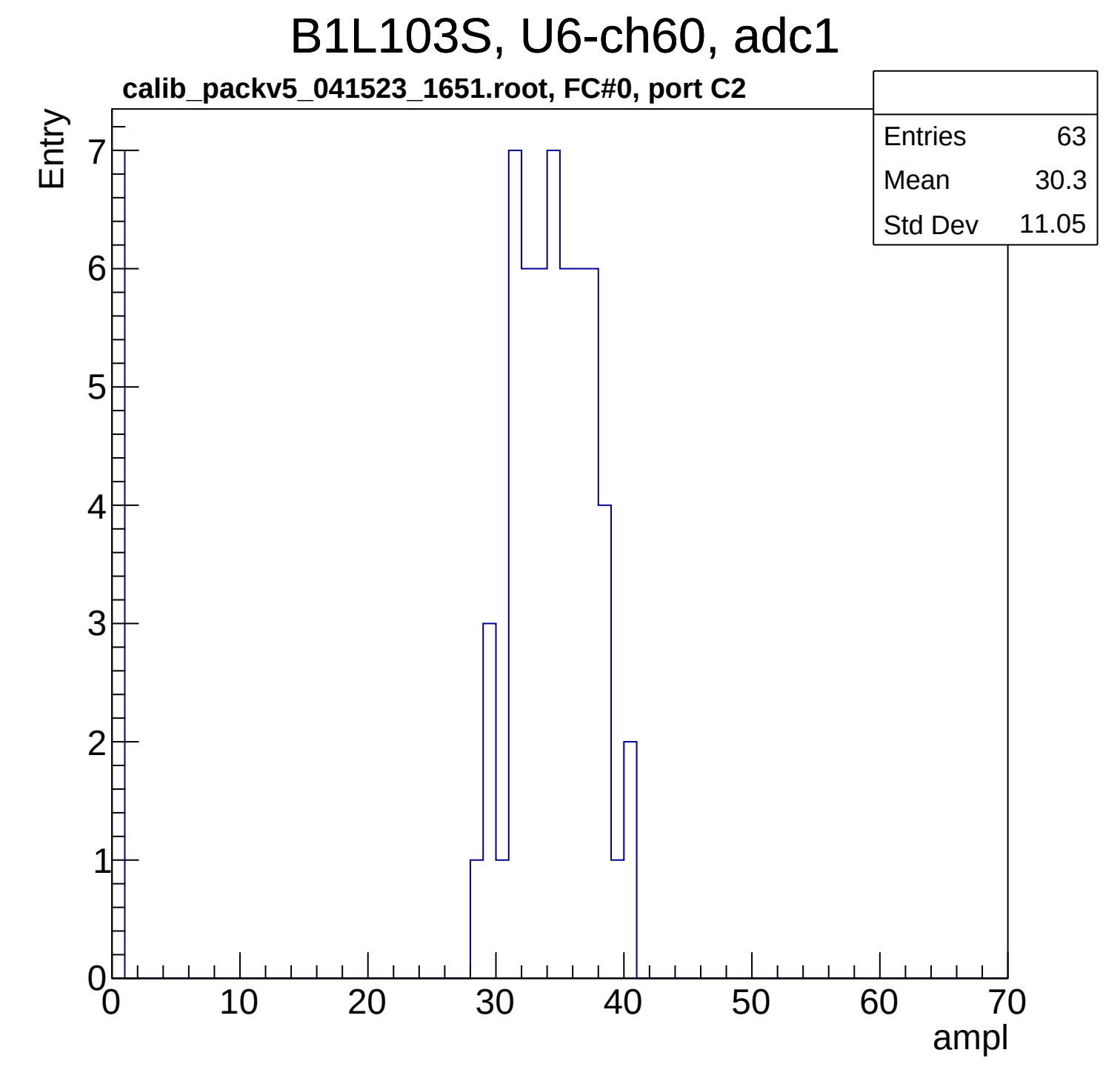
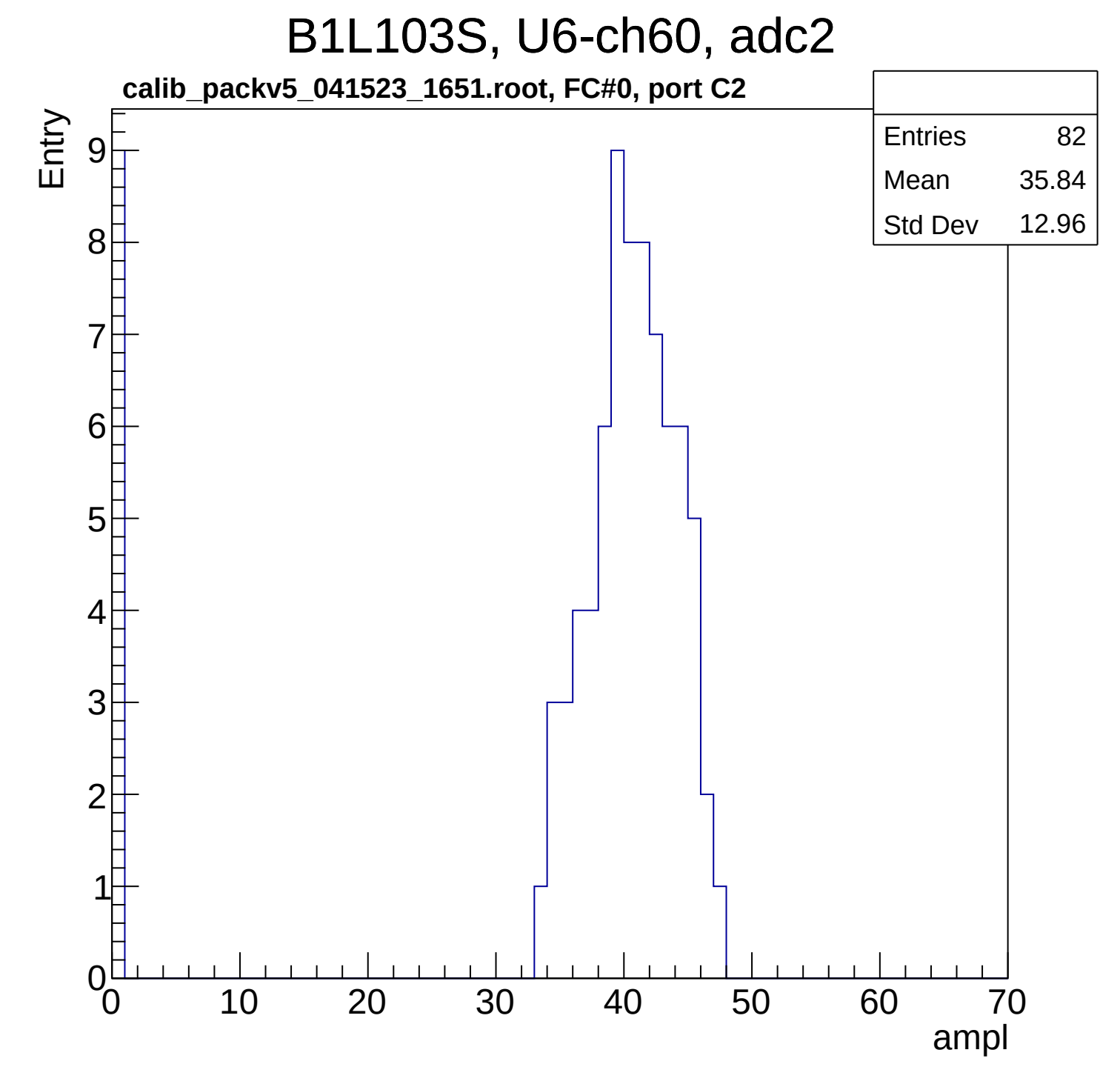
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U6-ch59, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.053
Std Dev 4.466
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch60, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 24
Std Dev 9.413
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U6-ch60, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 30.3
Std Dev 11.05
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U6-ch60, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 35.84
Std Dev 12.96
Entry
ampl
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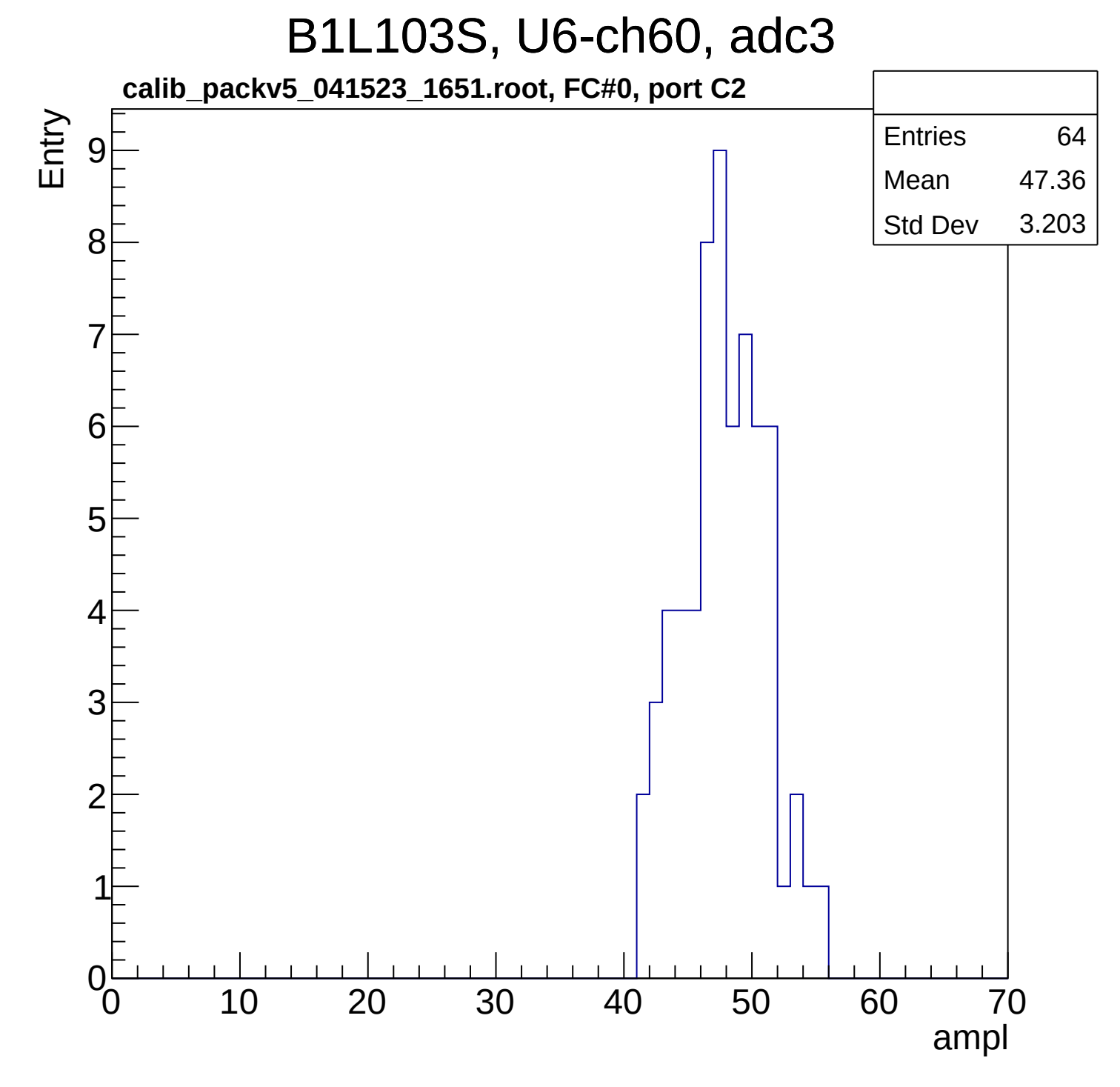
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch60, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 47.36
Std Dev 3.203
Entry
ampl
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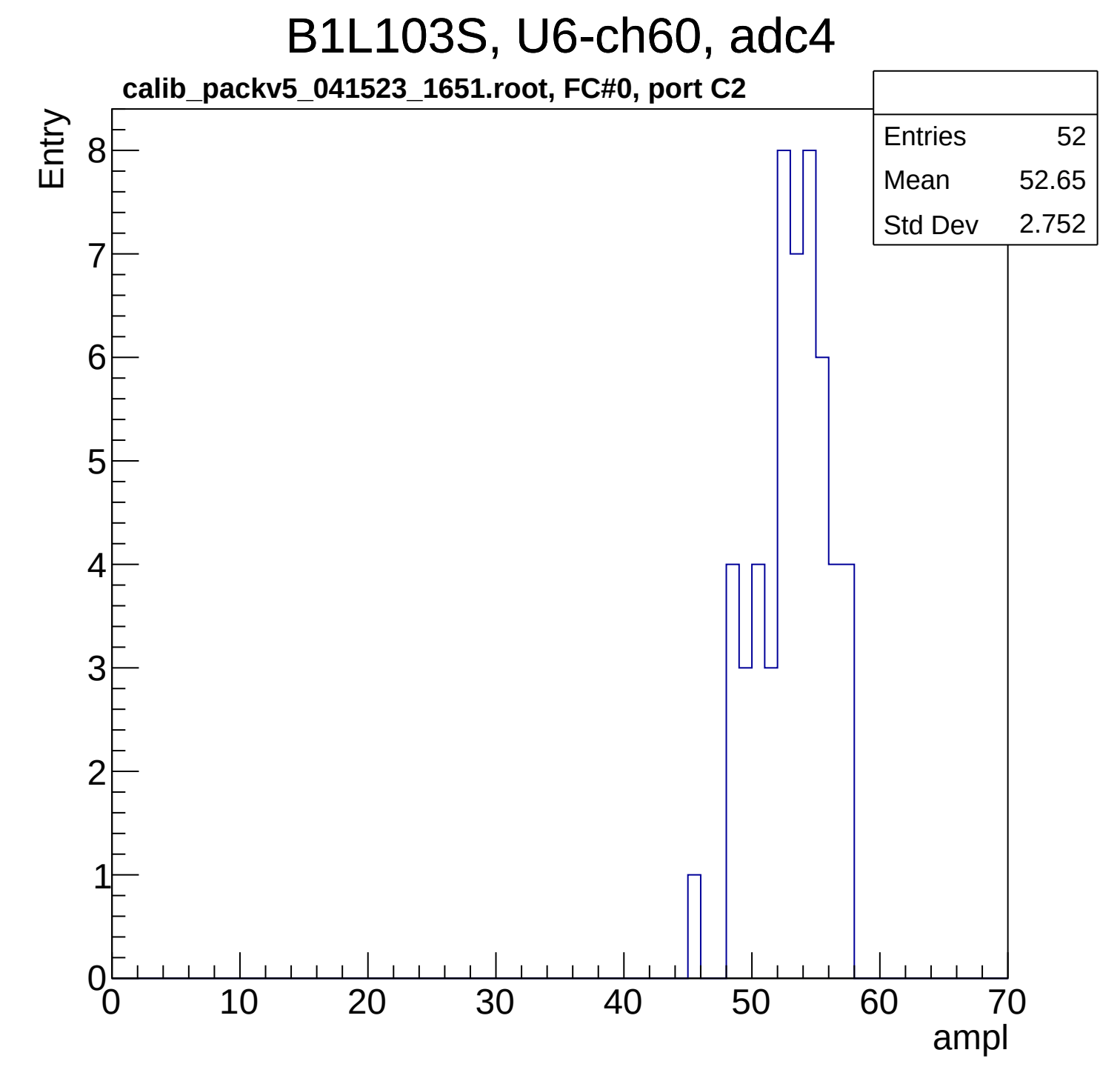
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch60, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 52.65
Std Dev 2.752
Entry
ampl
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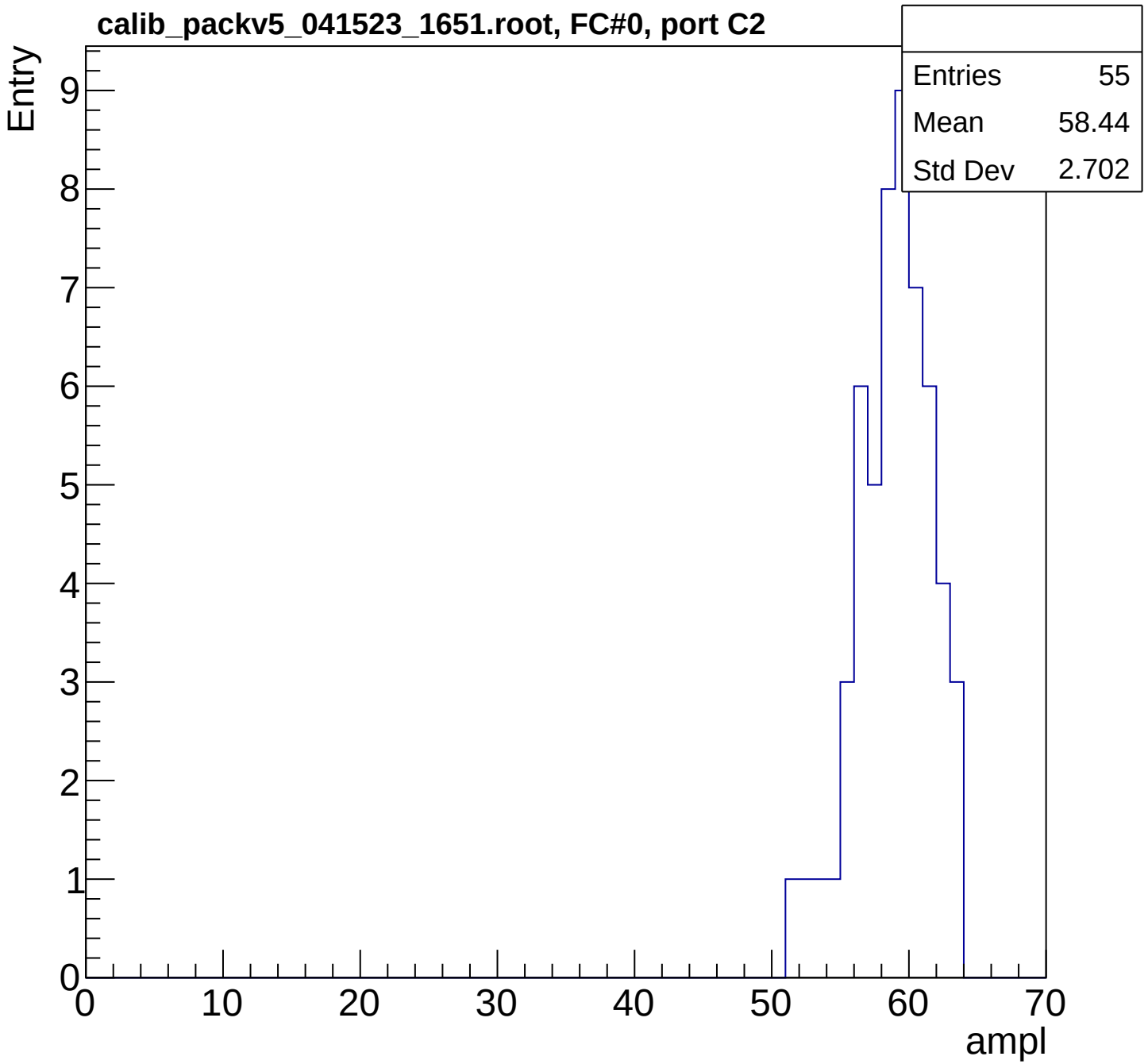
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch60, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 58.44
Std Dev 2.702
Entry
ampl
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2
3
4
5
6
7
8
9
0
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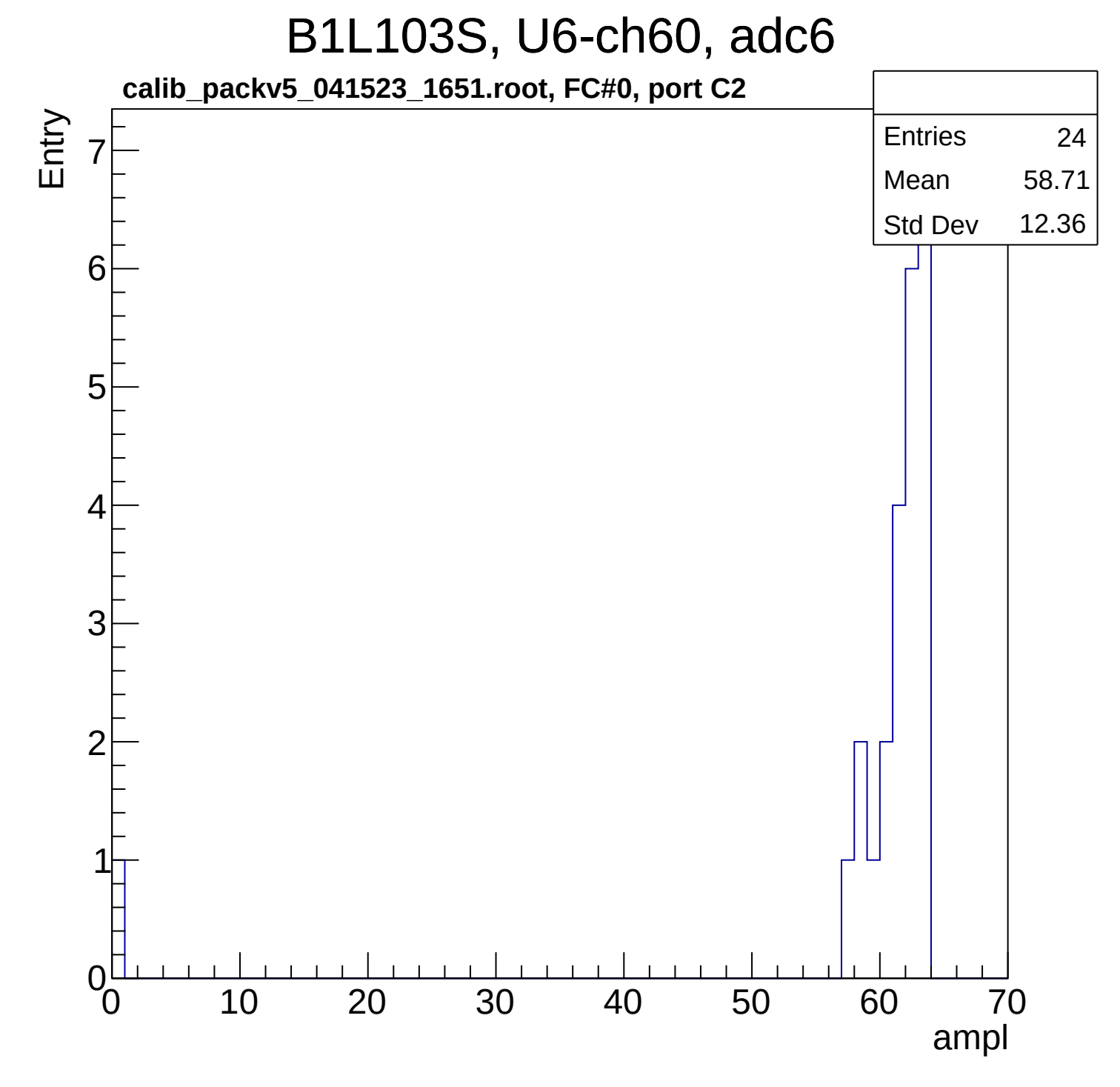
B1L103S, U6-ch60, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 58.71
Std Dev 12.36
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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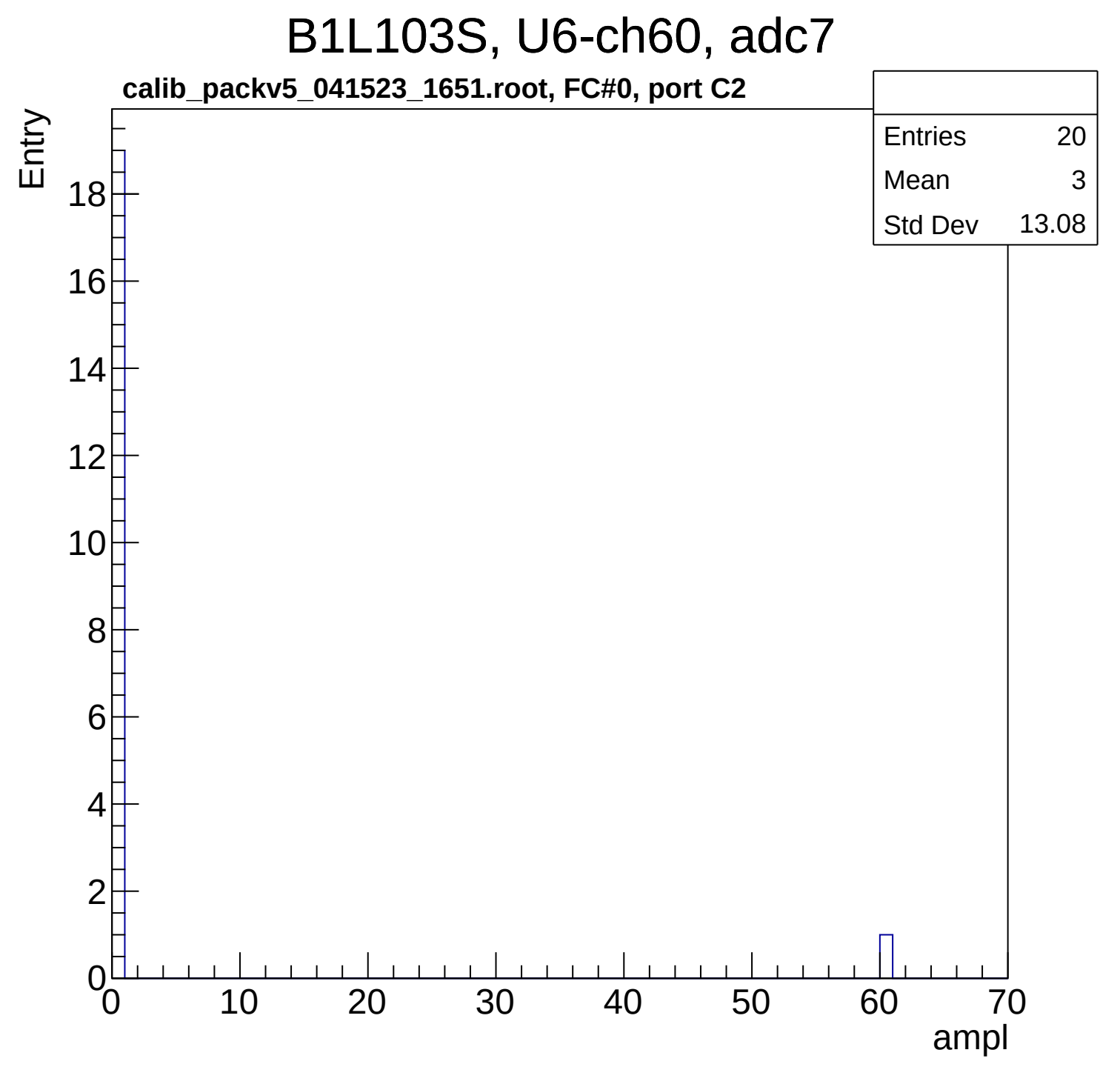
B1L103S, U6-ch60, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3
Std Dev 13.08
Entry
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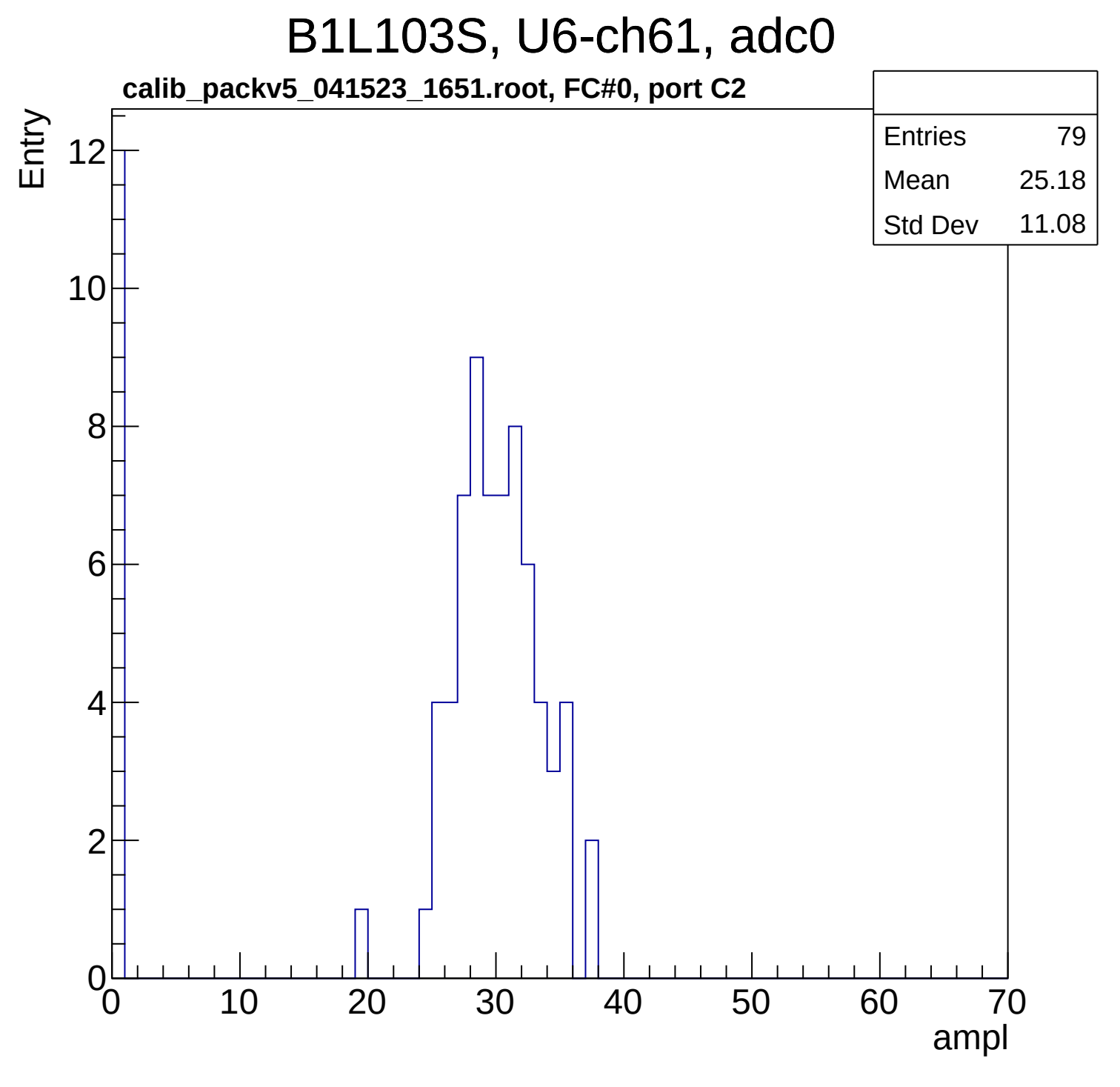
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch61, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 25.18
Std Dev 11.08
Entry
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4
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8
10
12
0
10
20
30
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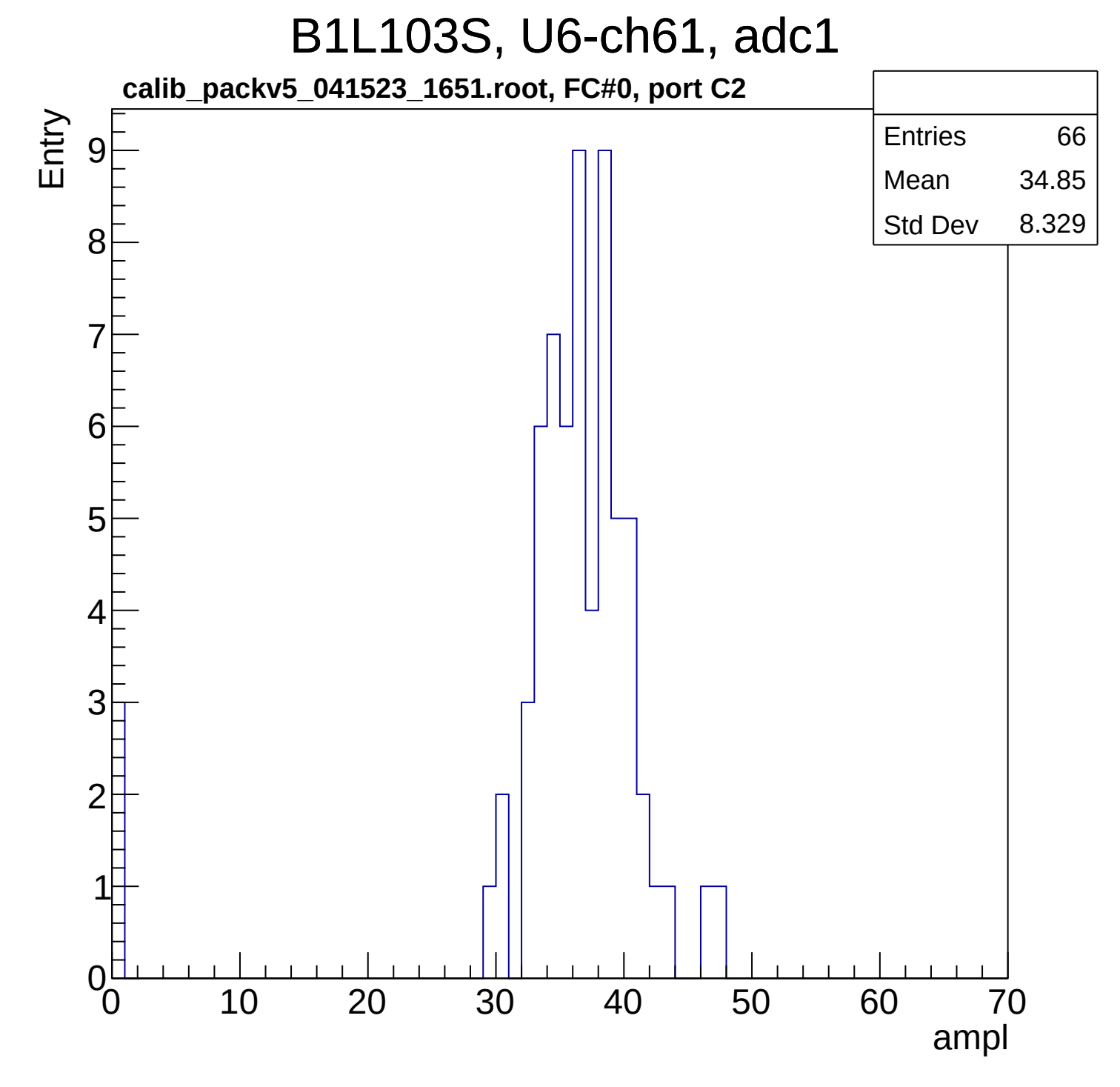
50
60
70
ampl


B1L103S, U6-ch61, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 34.85
Std Dev 8.329
Entry
ampl
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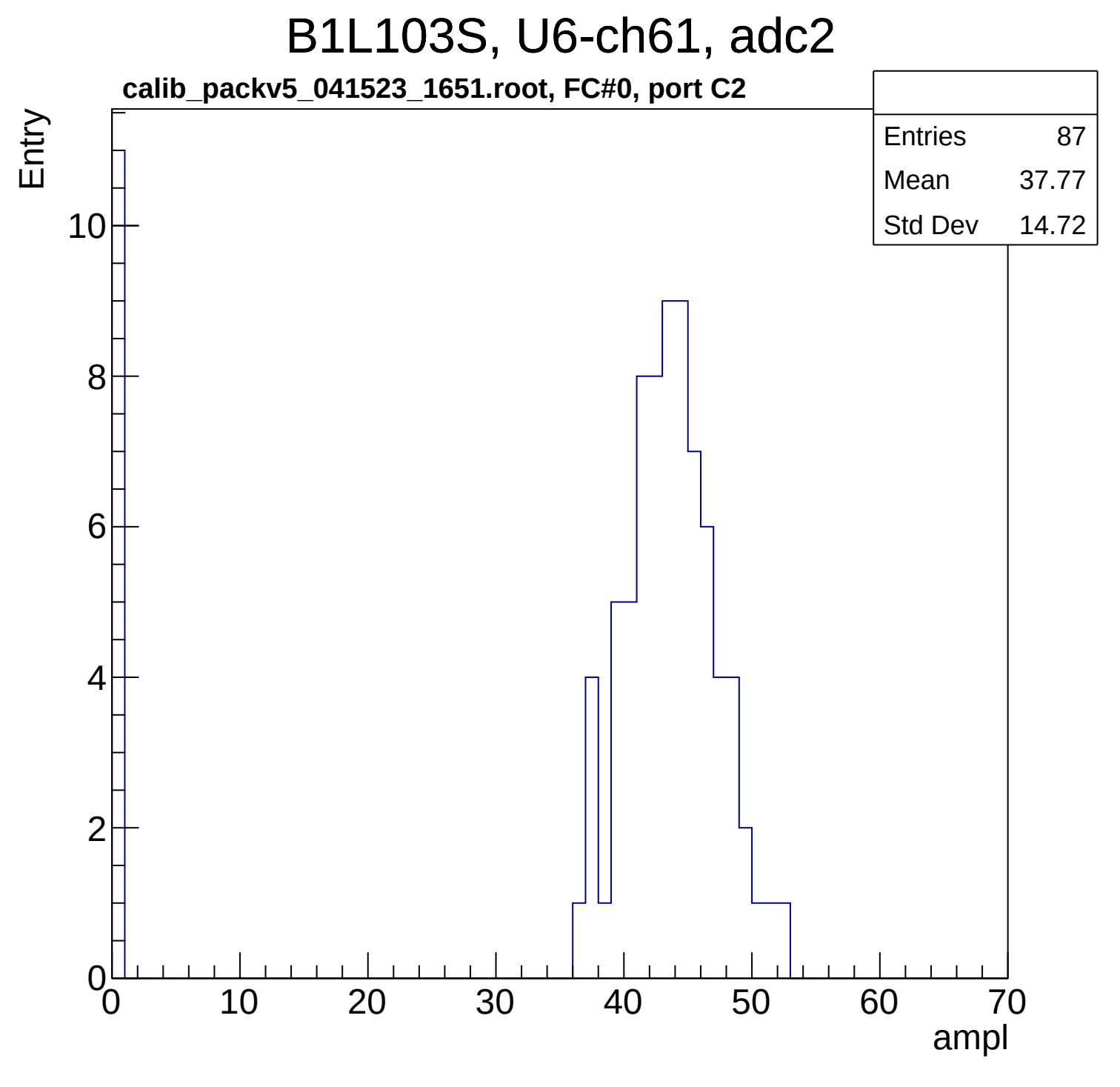
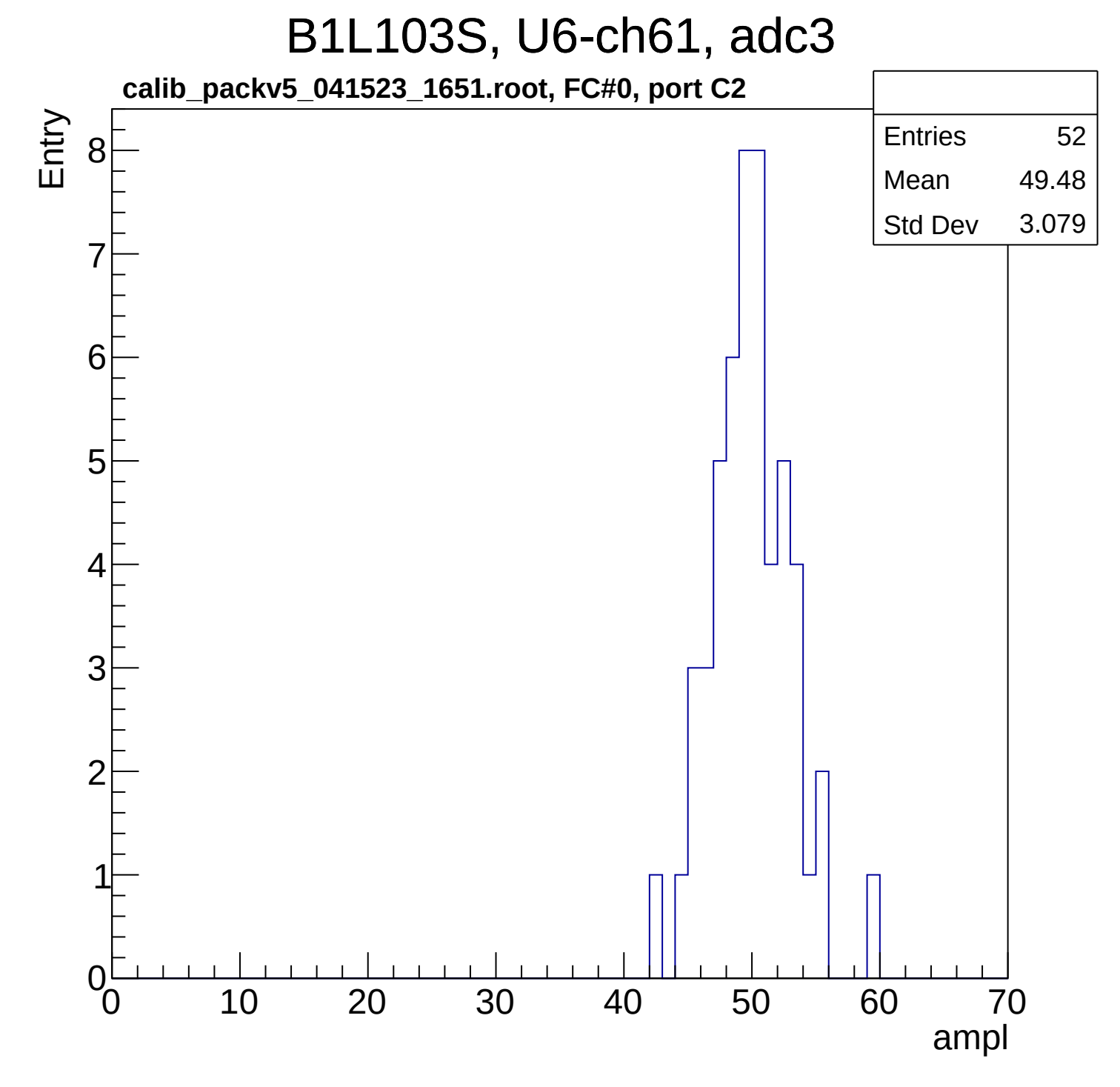
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch61, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 37.77
Std Dev 14.72
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch61, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 49.48
Std Dev 3.079
Entry
ampl
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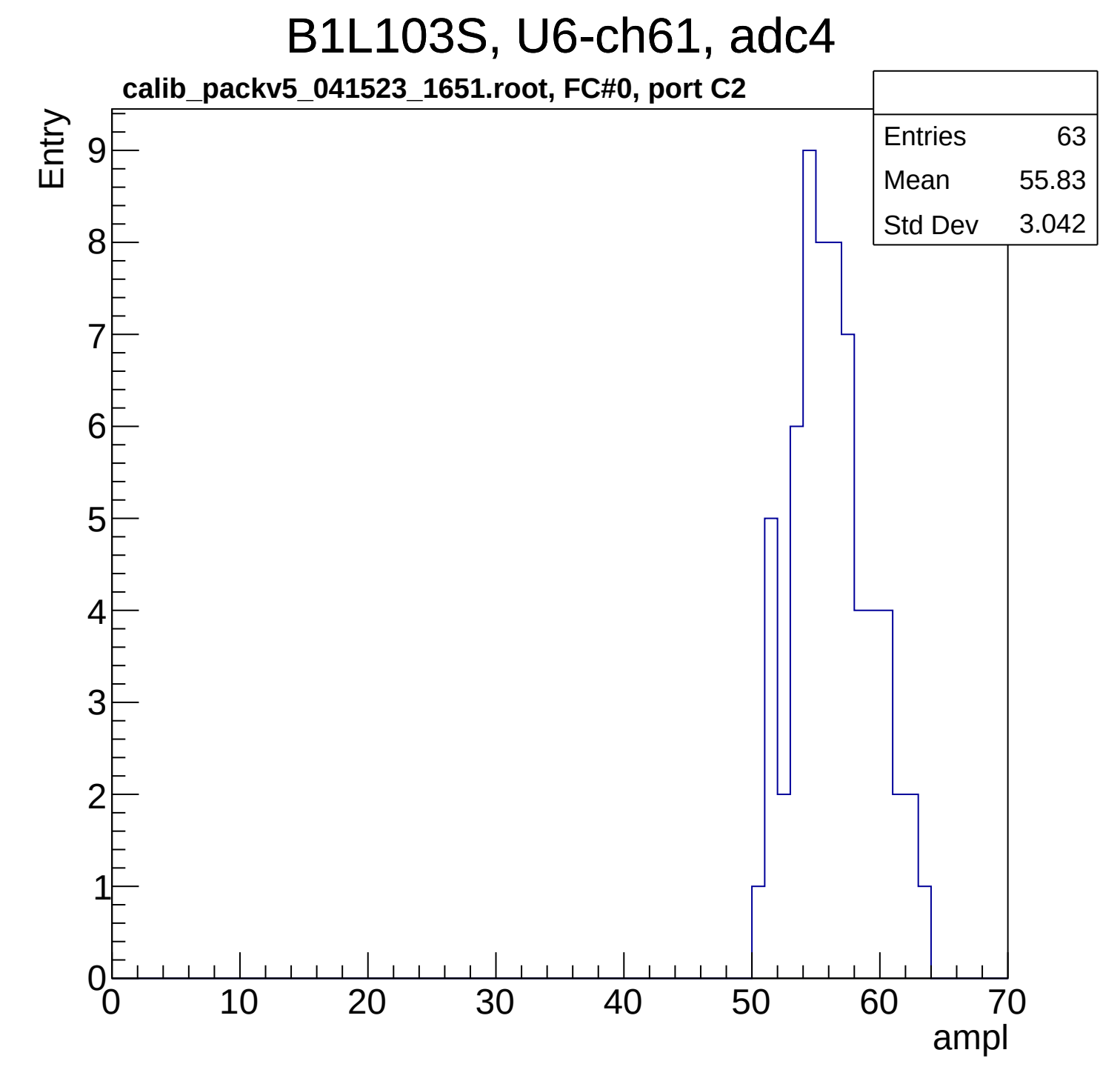
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch61, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 55.83
Std Dev 3.042
Entry
ampl
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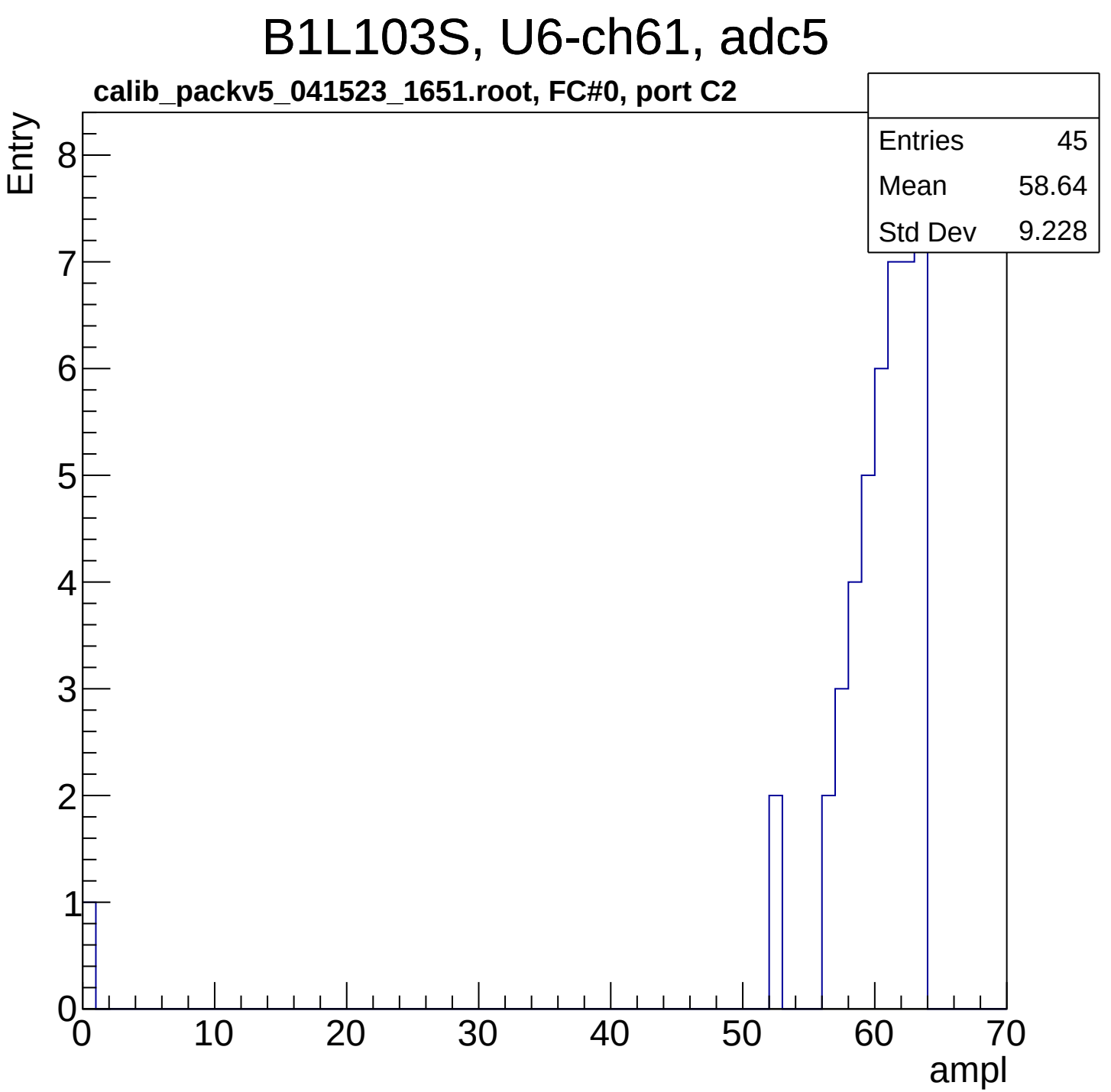
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch61, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 58.64
Std Dev 9.228
Entry
ampl
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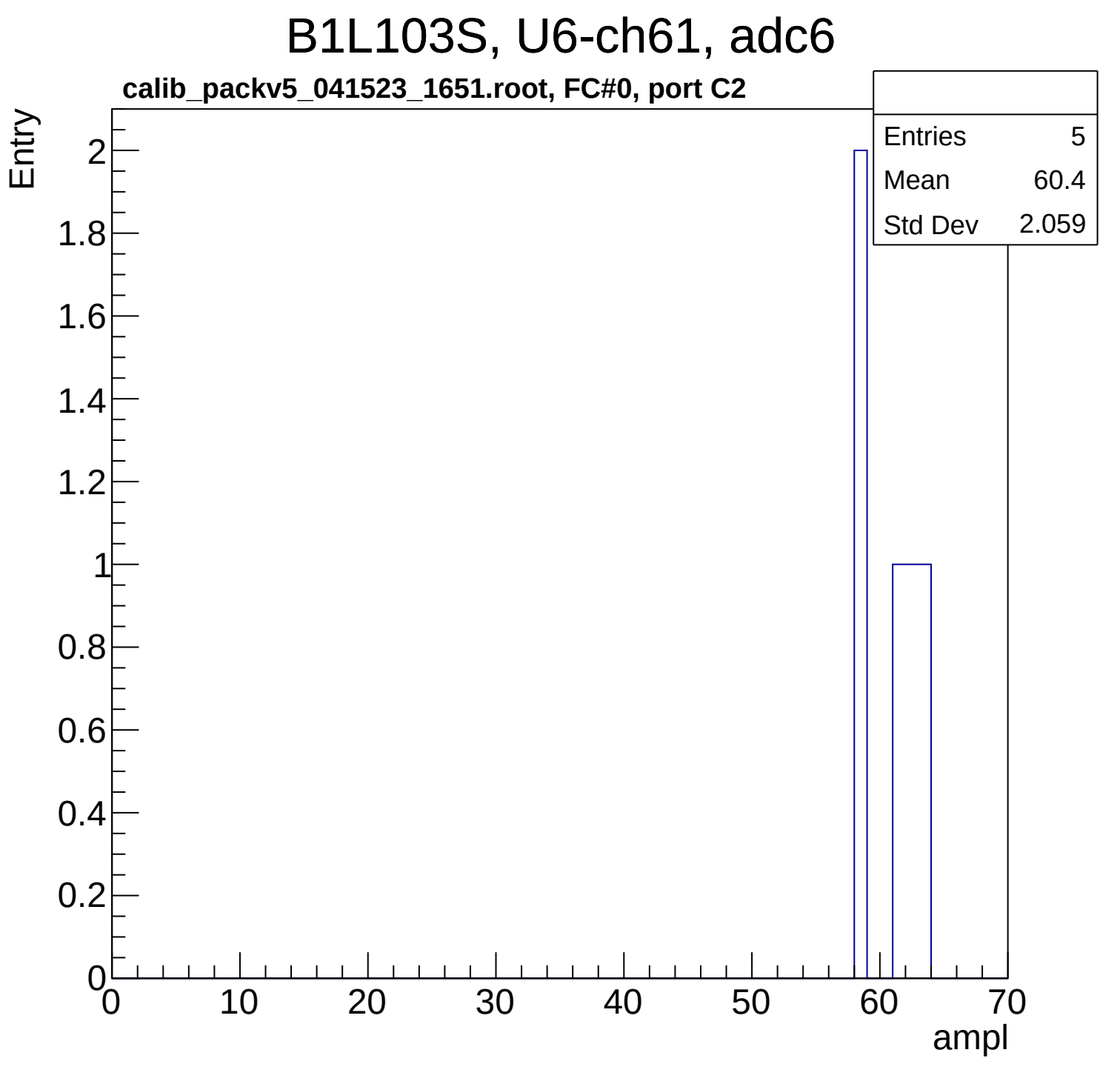
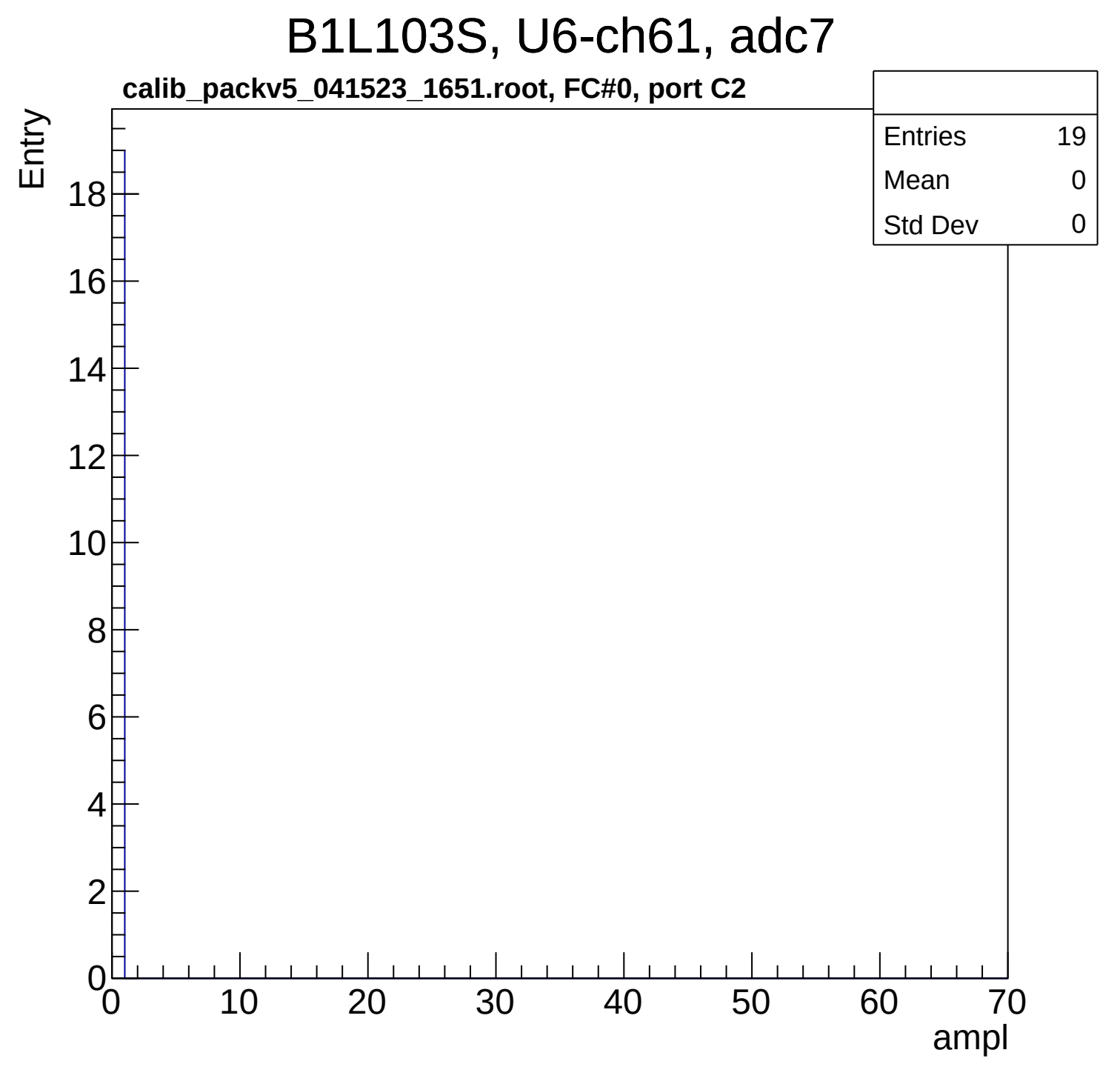
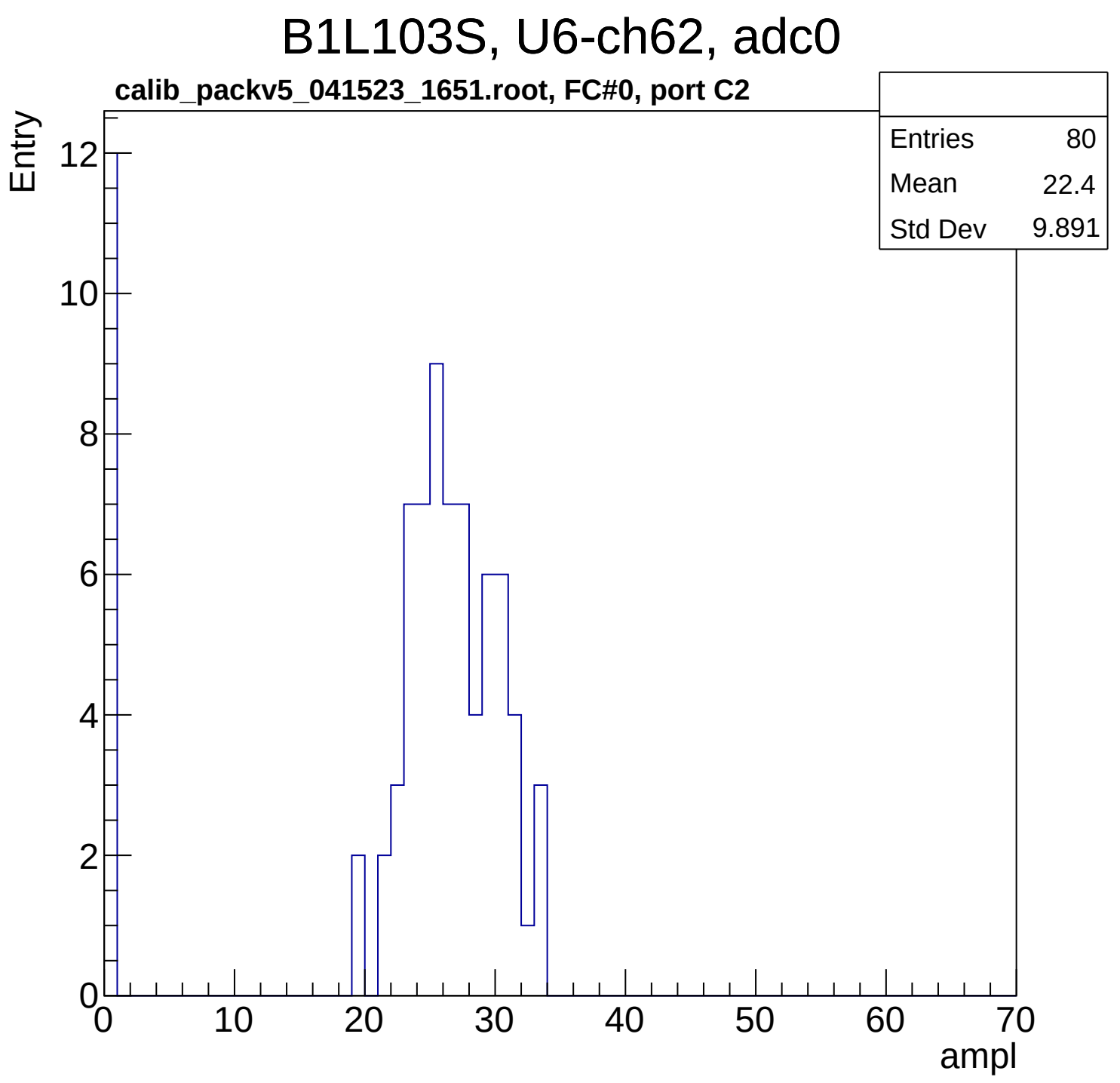
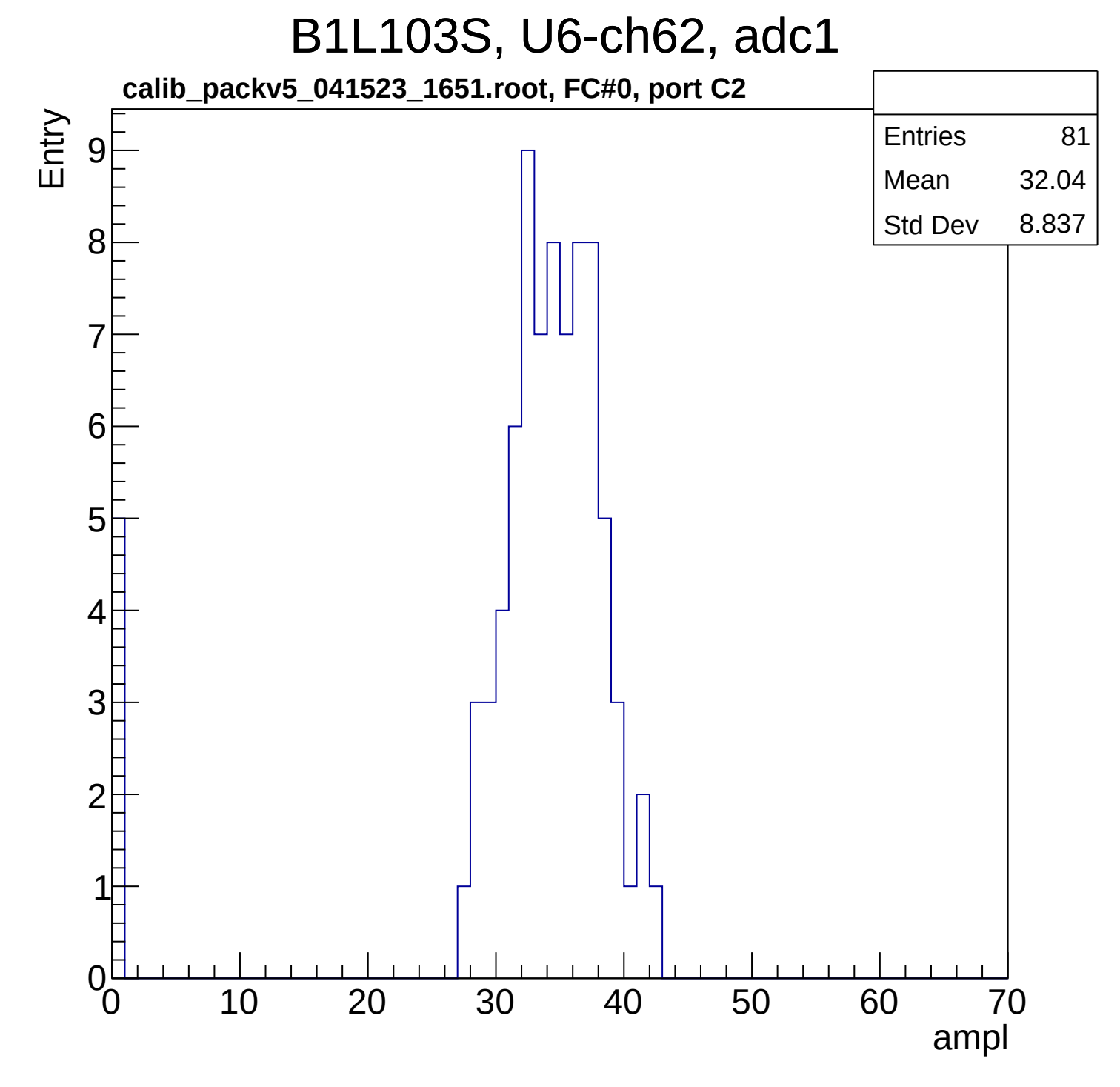
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch61, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 60.4
Std Dev 2.059
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U6-ch61, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch62, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 22.4
Std Dev 9.891
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch62, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 32.04
Std Dev 8.837
Entry
ampl
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2
3
4
5
6
7
8
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0
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60
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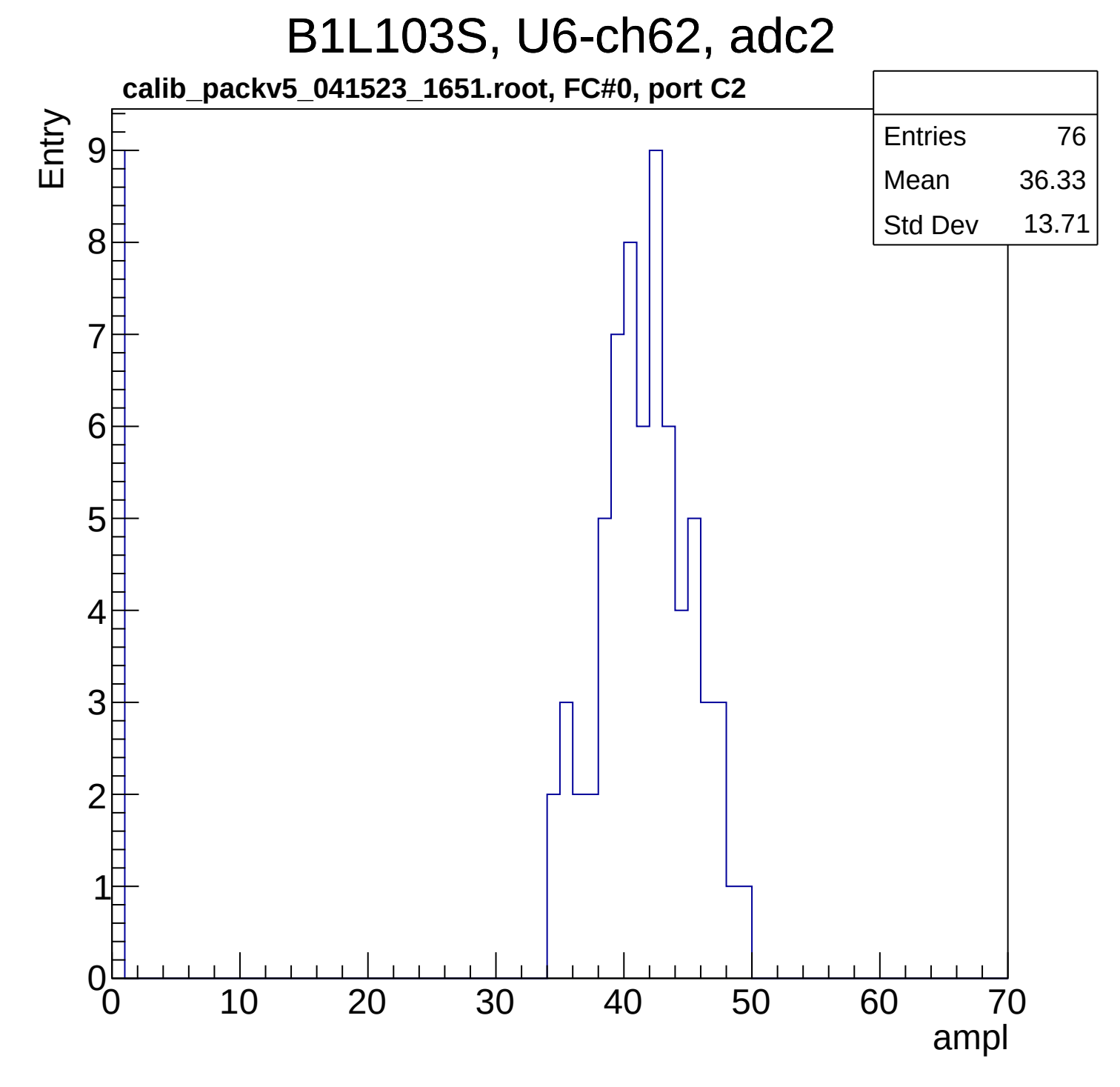
B1L103S, U6-ch62, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 36.33
Std Dev 13.71
Entry
ampl
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2
3
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5
6
7
8
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0
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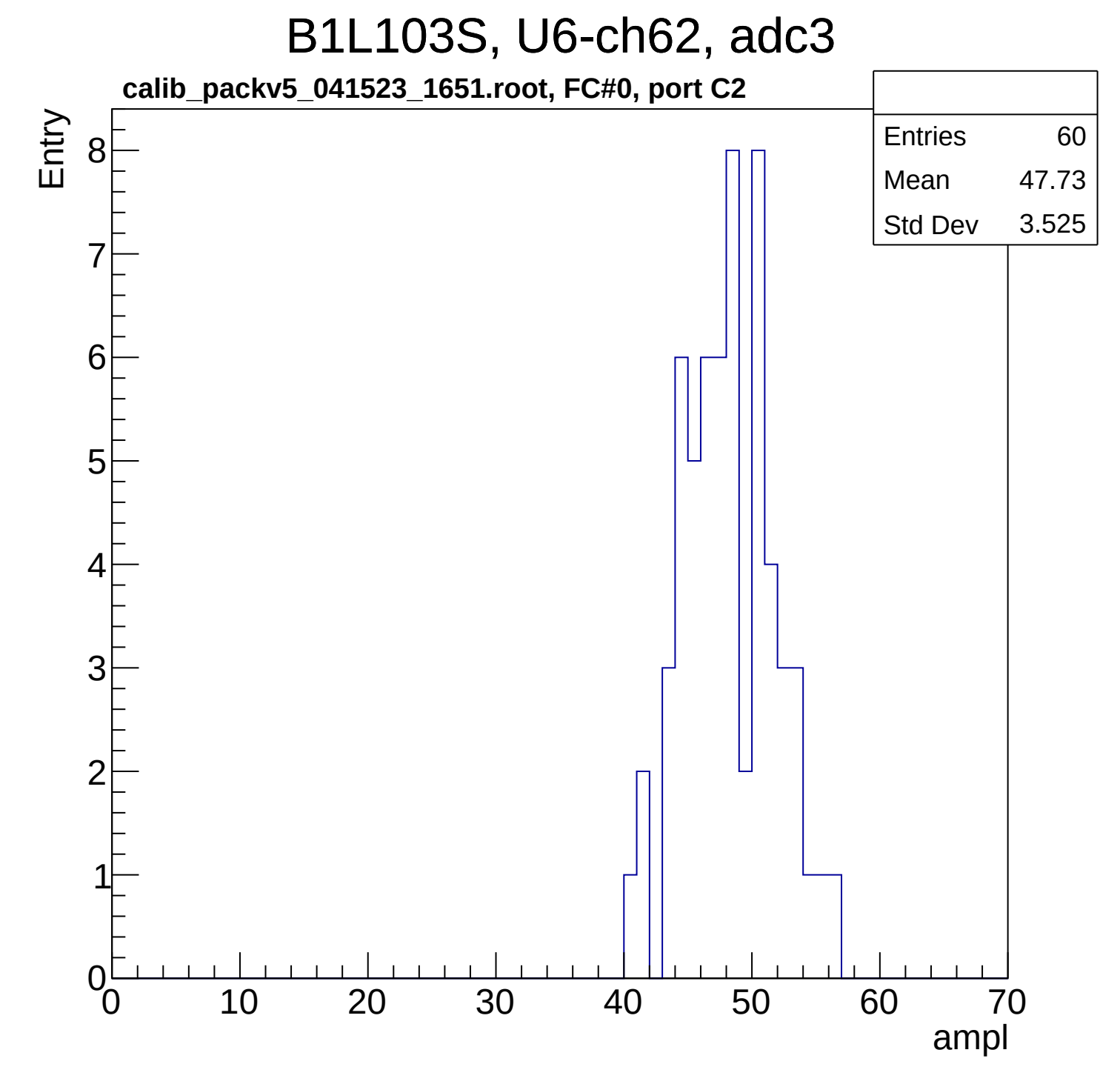
B1L103S, U6-ch62, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 47.73
Std Dev 3.525
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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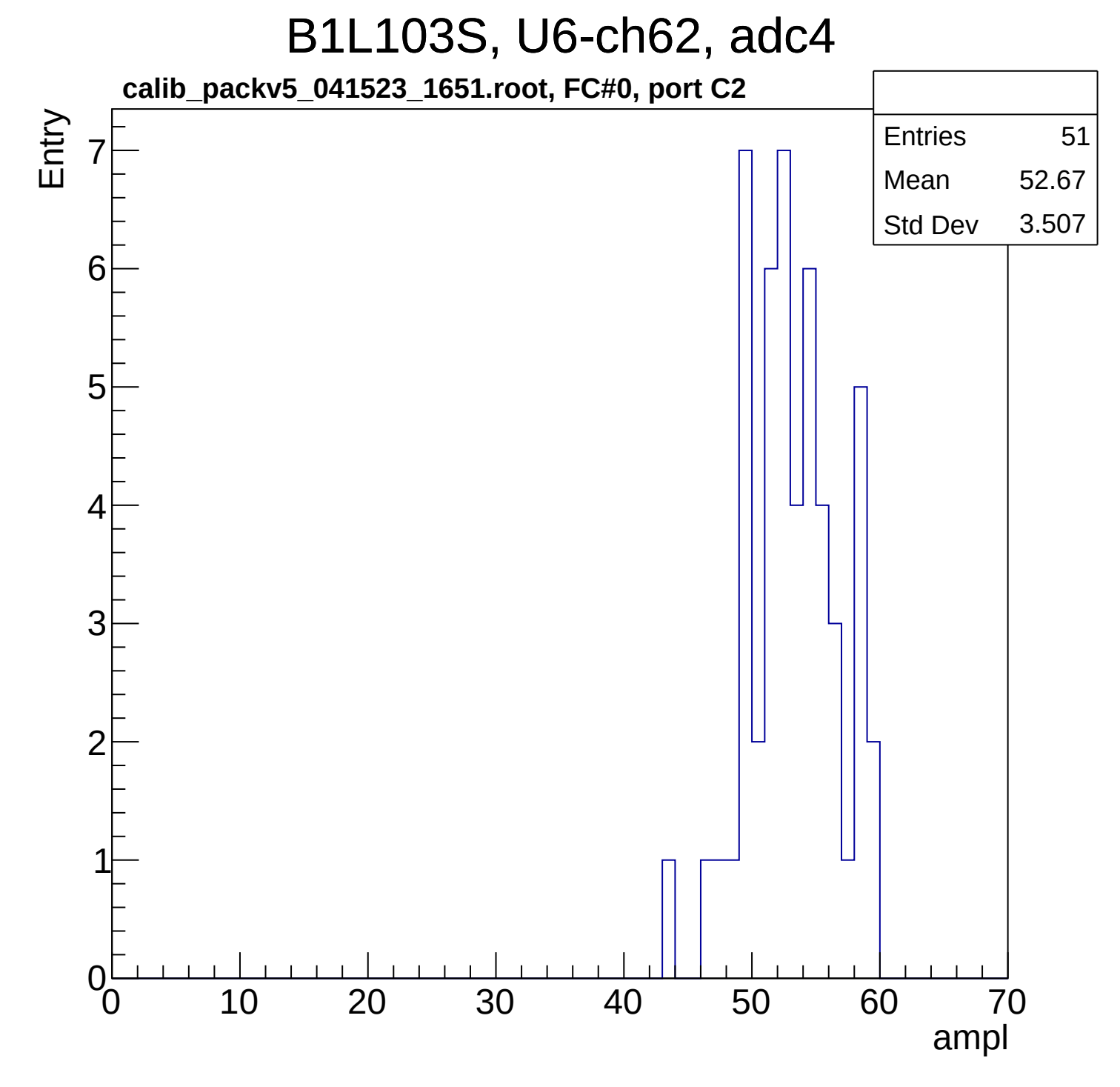
B1L103S, U6-ch62, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 52.67
Std Dev 3.507
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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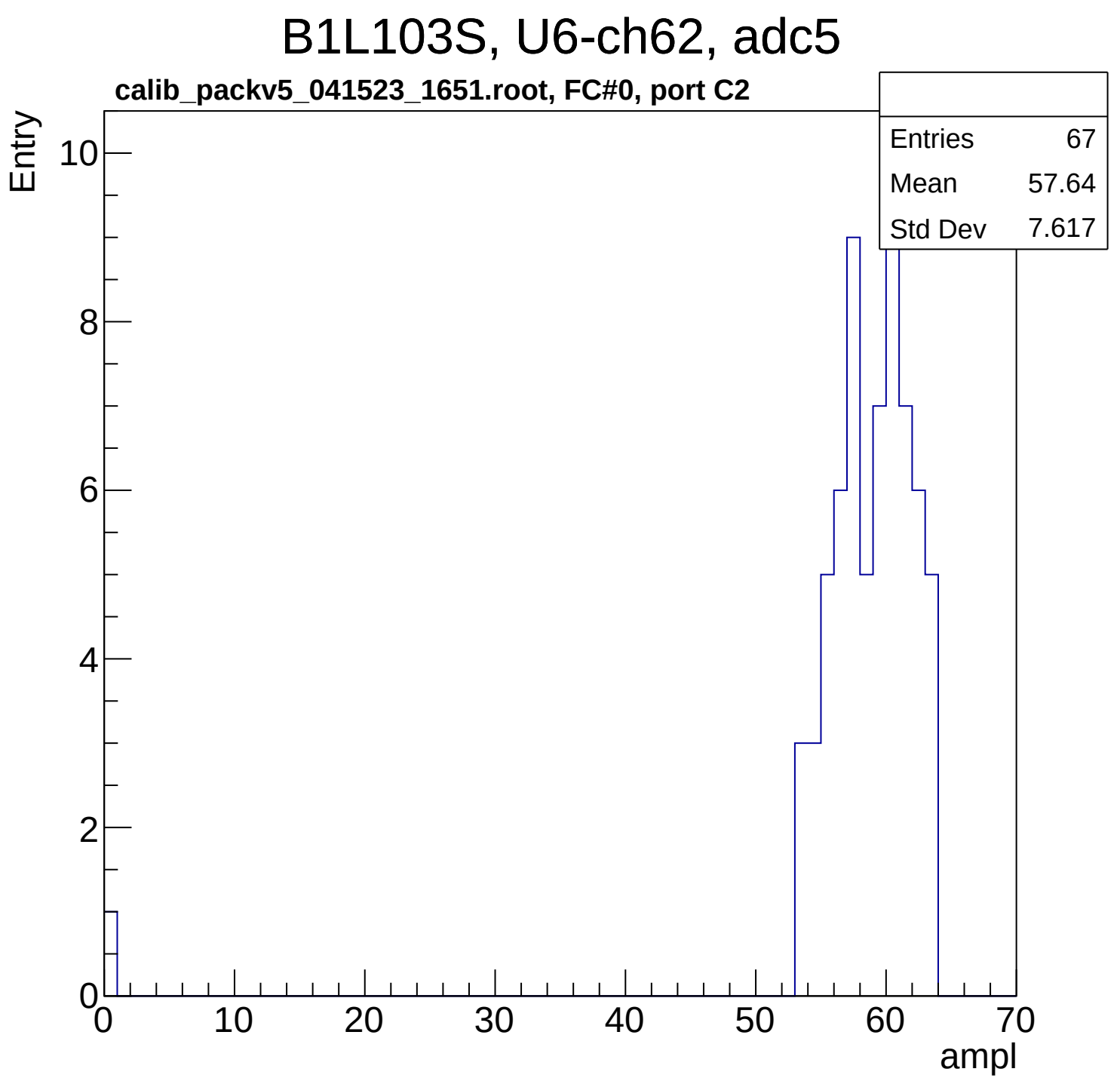
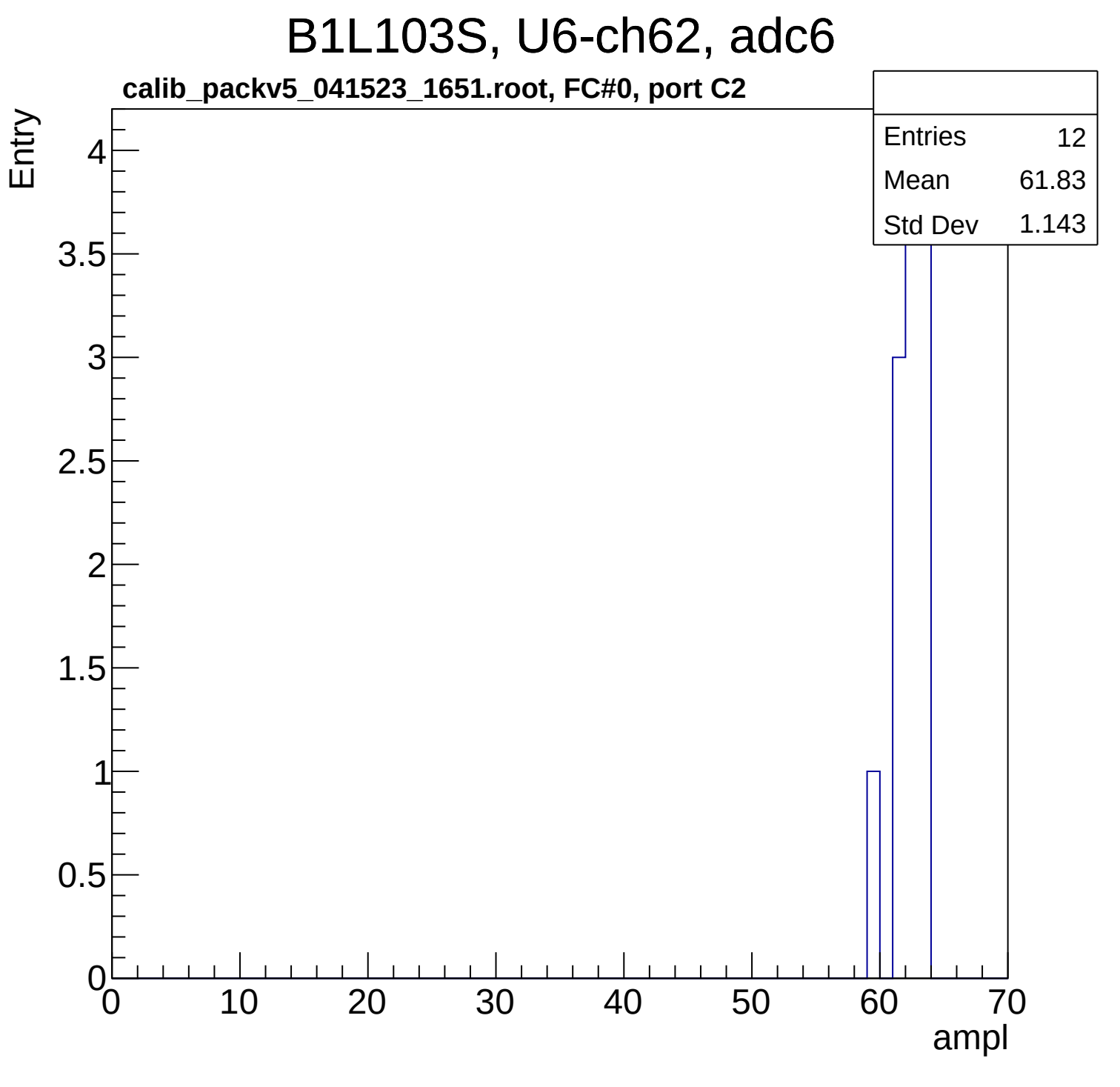

B1L103S, U6-ch62, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 57.64
Std Dev 7.617
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch62, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.83
Std Dev 1.143
Entry
ampl
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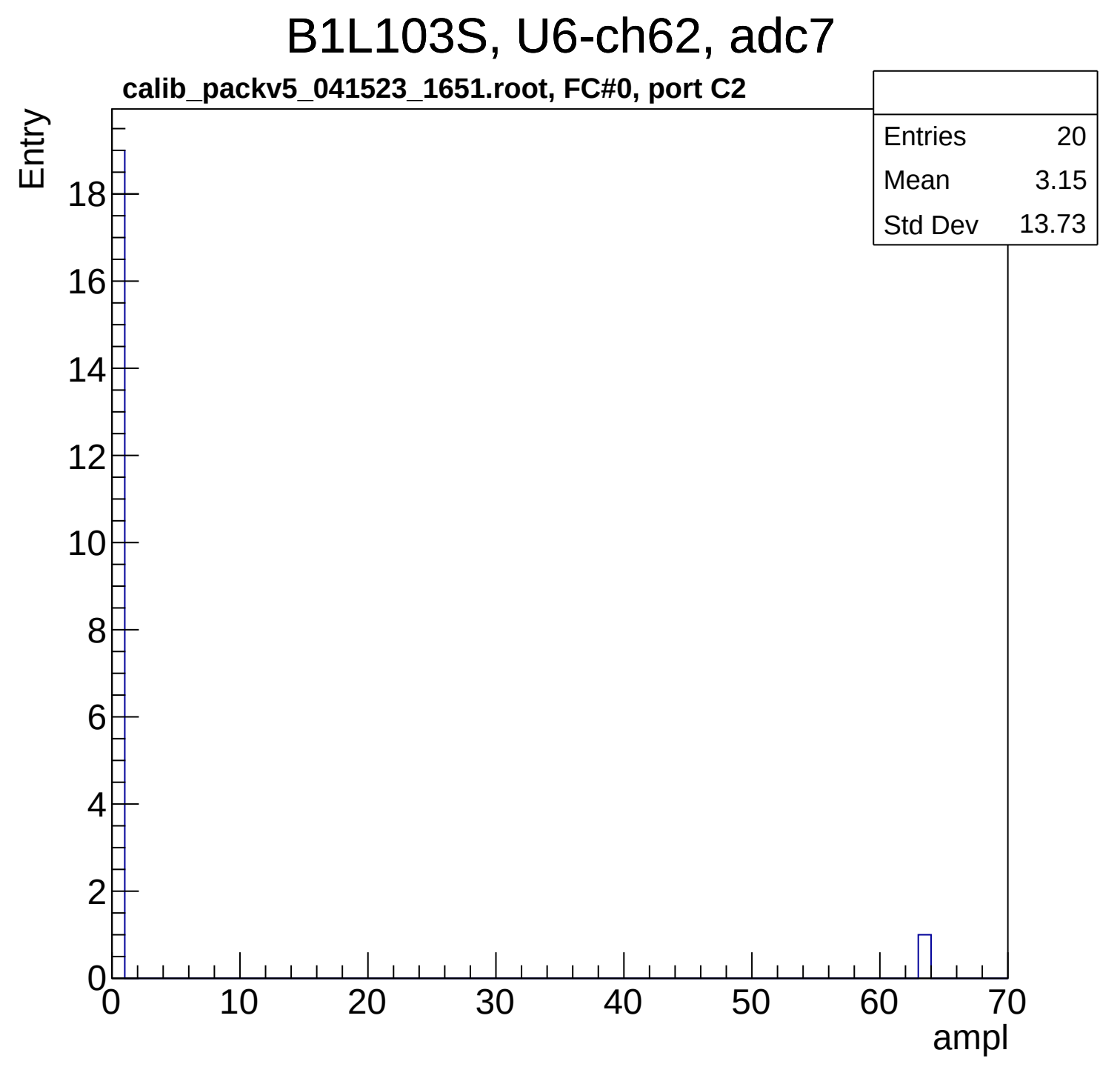
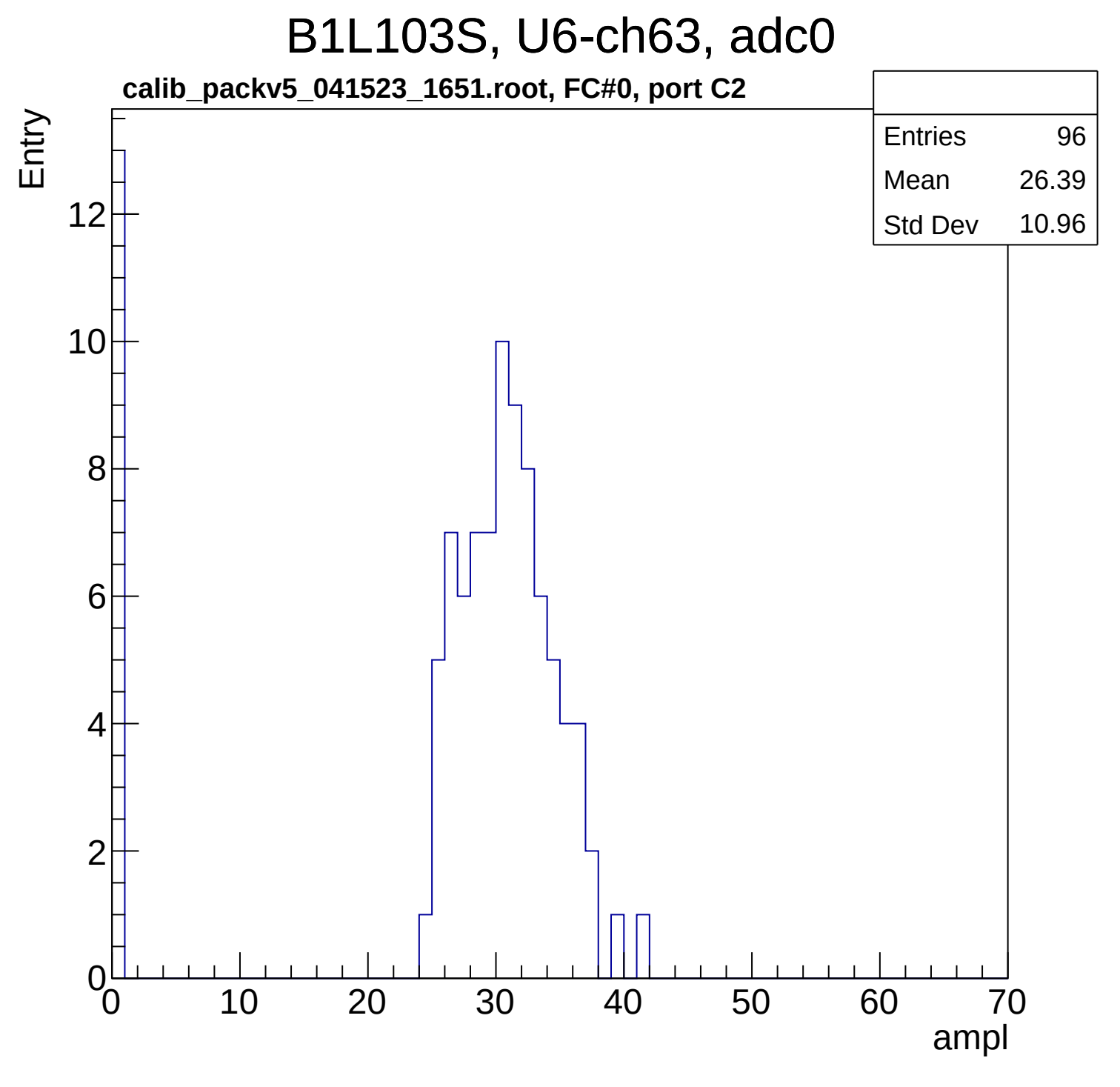
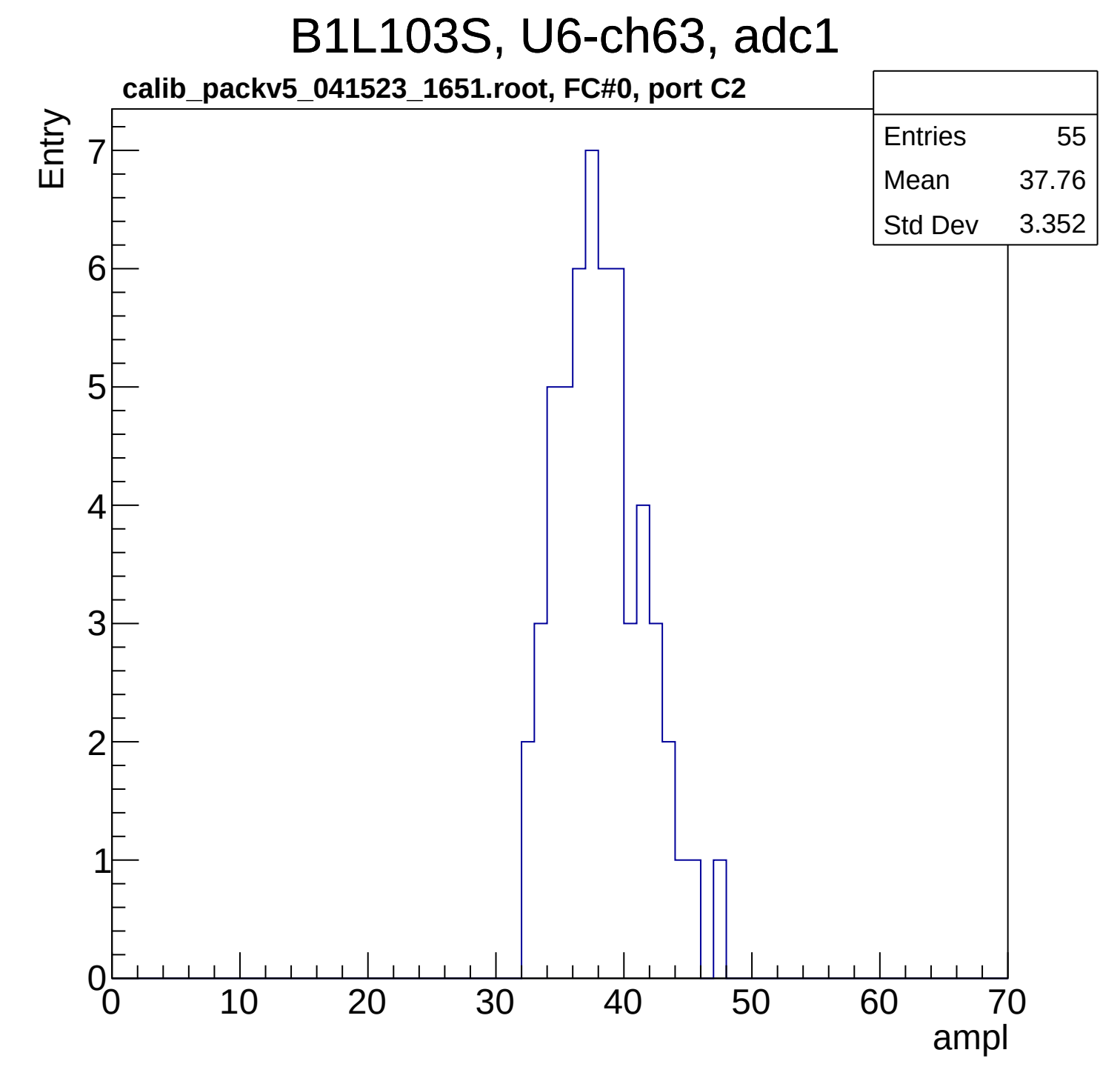
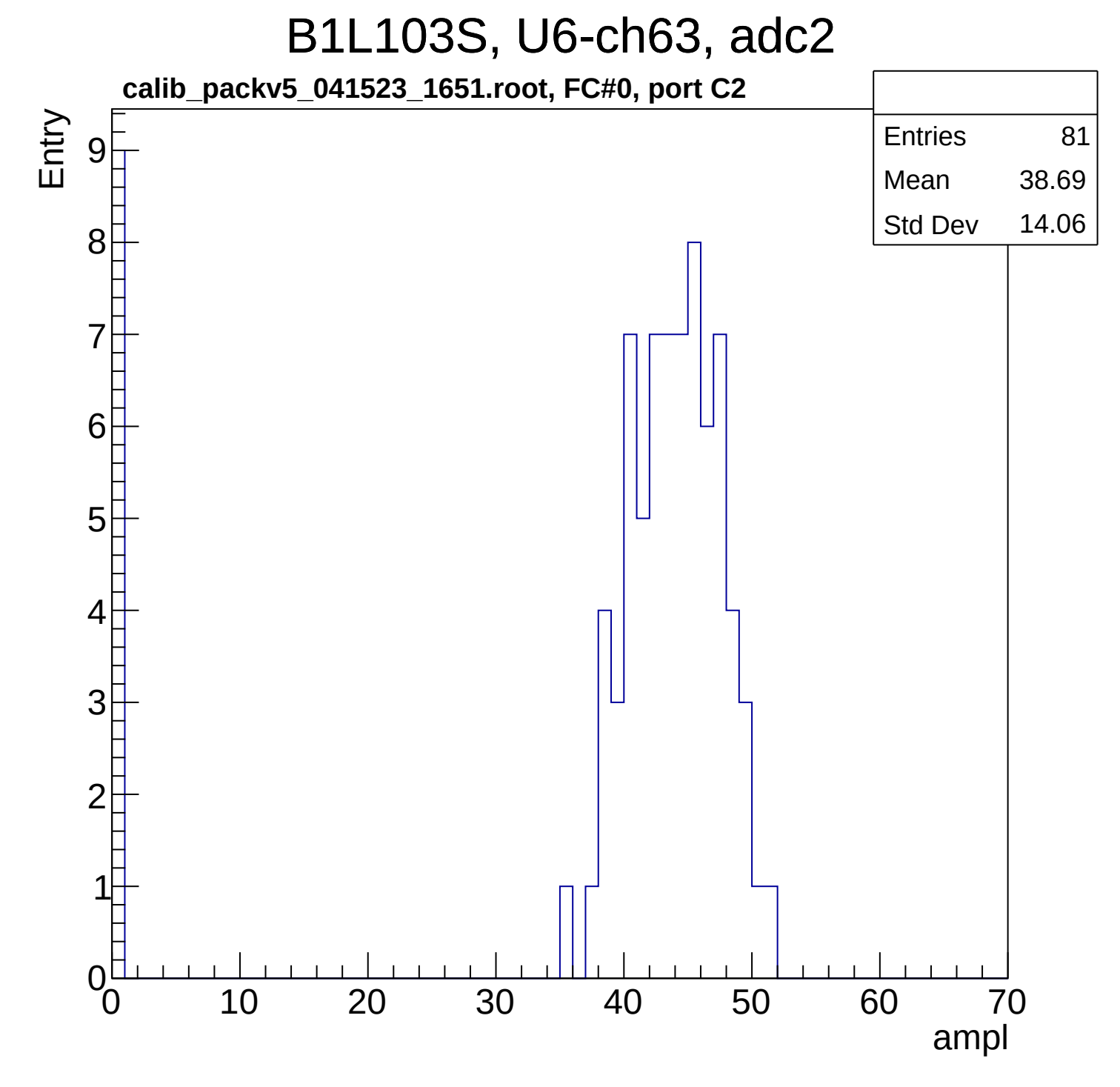
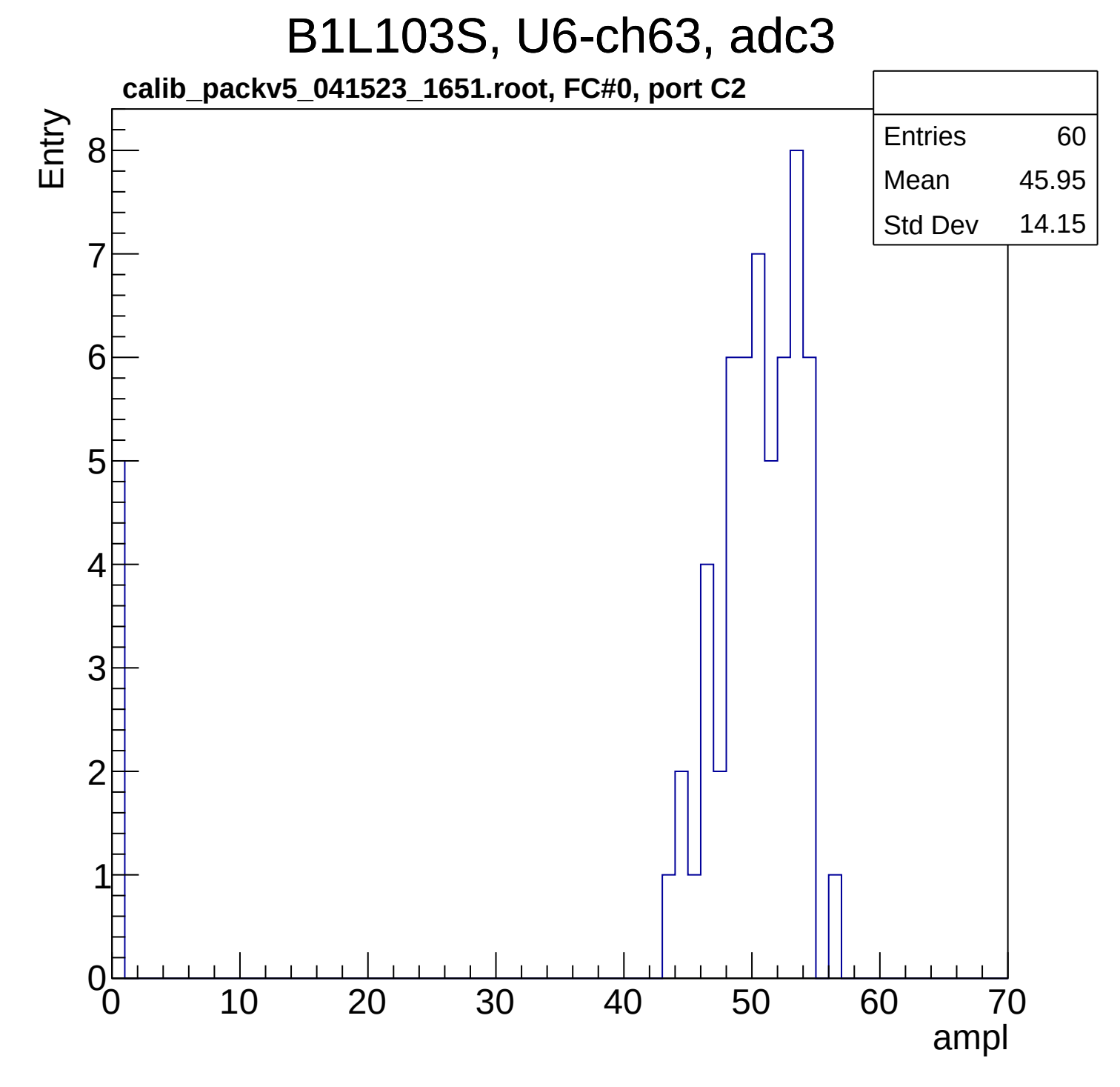
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

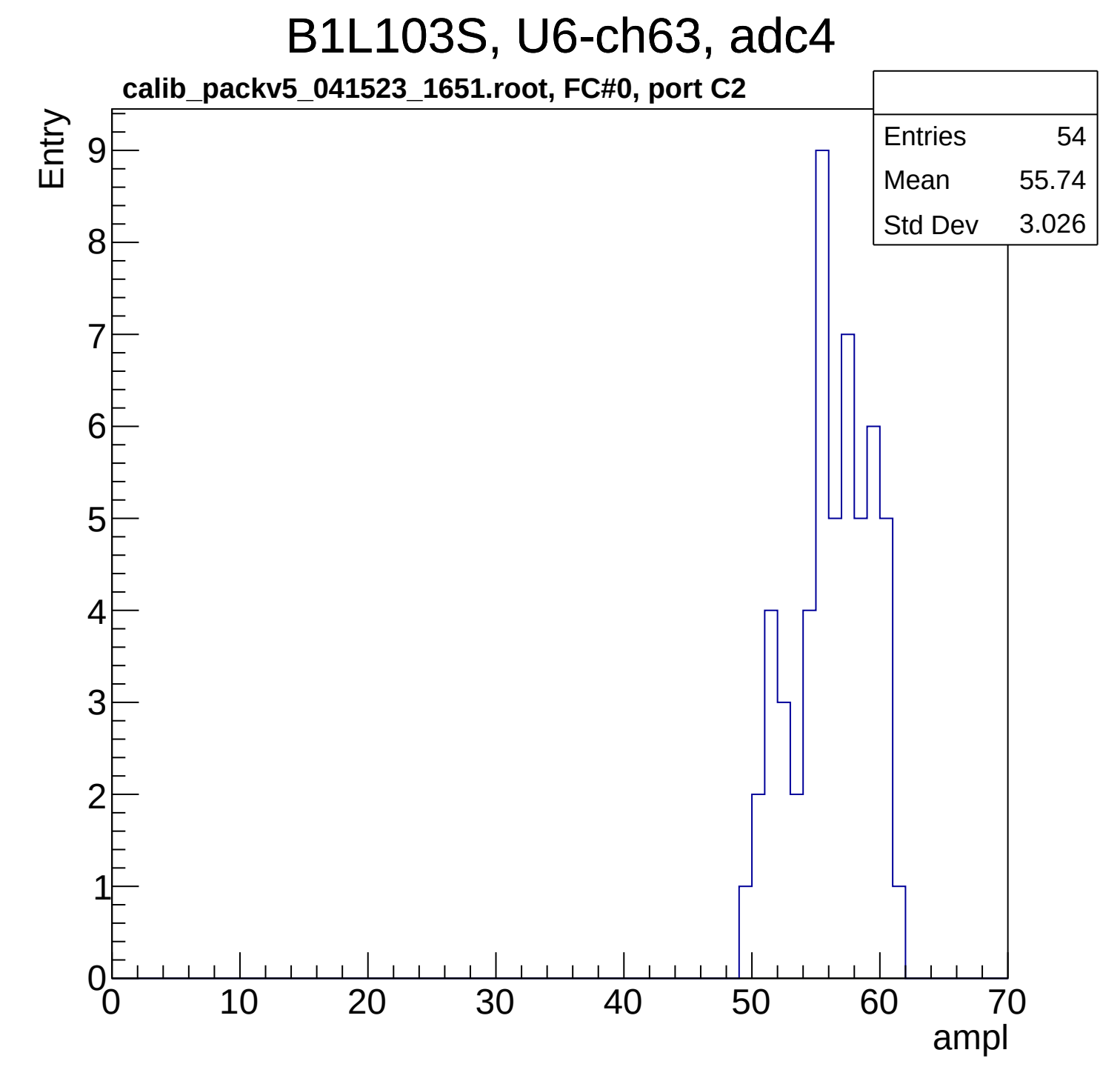

B1L103S, U6-ch62, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

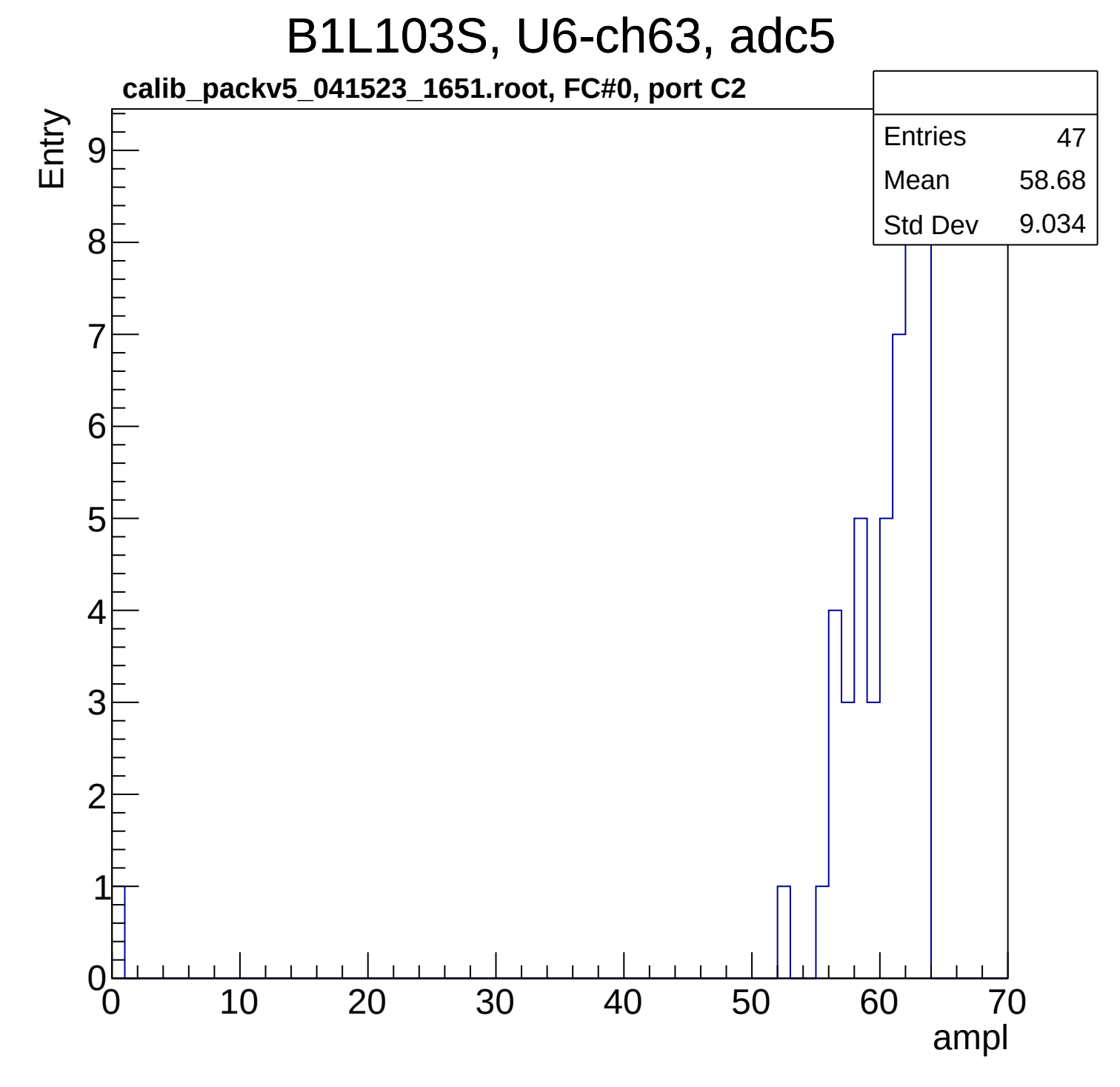

B1L103S, U6-ch63, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 96
Mean 26.39
Std Dev 10.96
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch63, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 37.76
Std Dev 3.352
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U6-ch63, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 38.69
Std Dev 14.06
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch63, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 45.95
Std Dev 14.15
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch63, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 55.74
Std Dev 3.026
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch63, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 58.68
Std Dev 9.034
Entry
ampl
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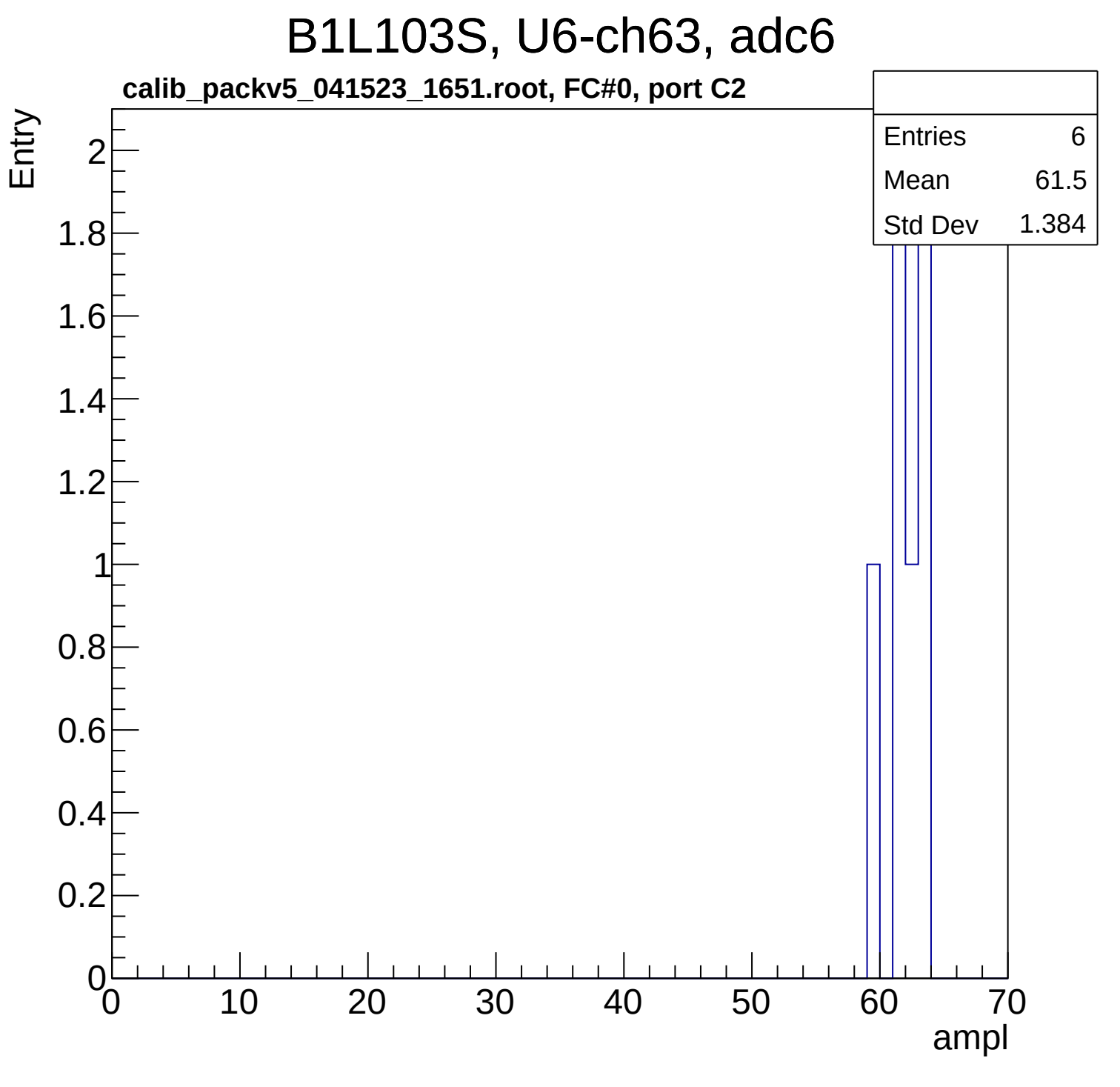
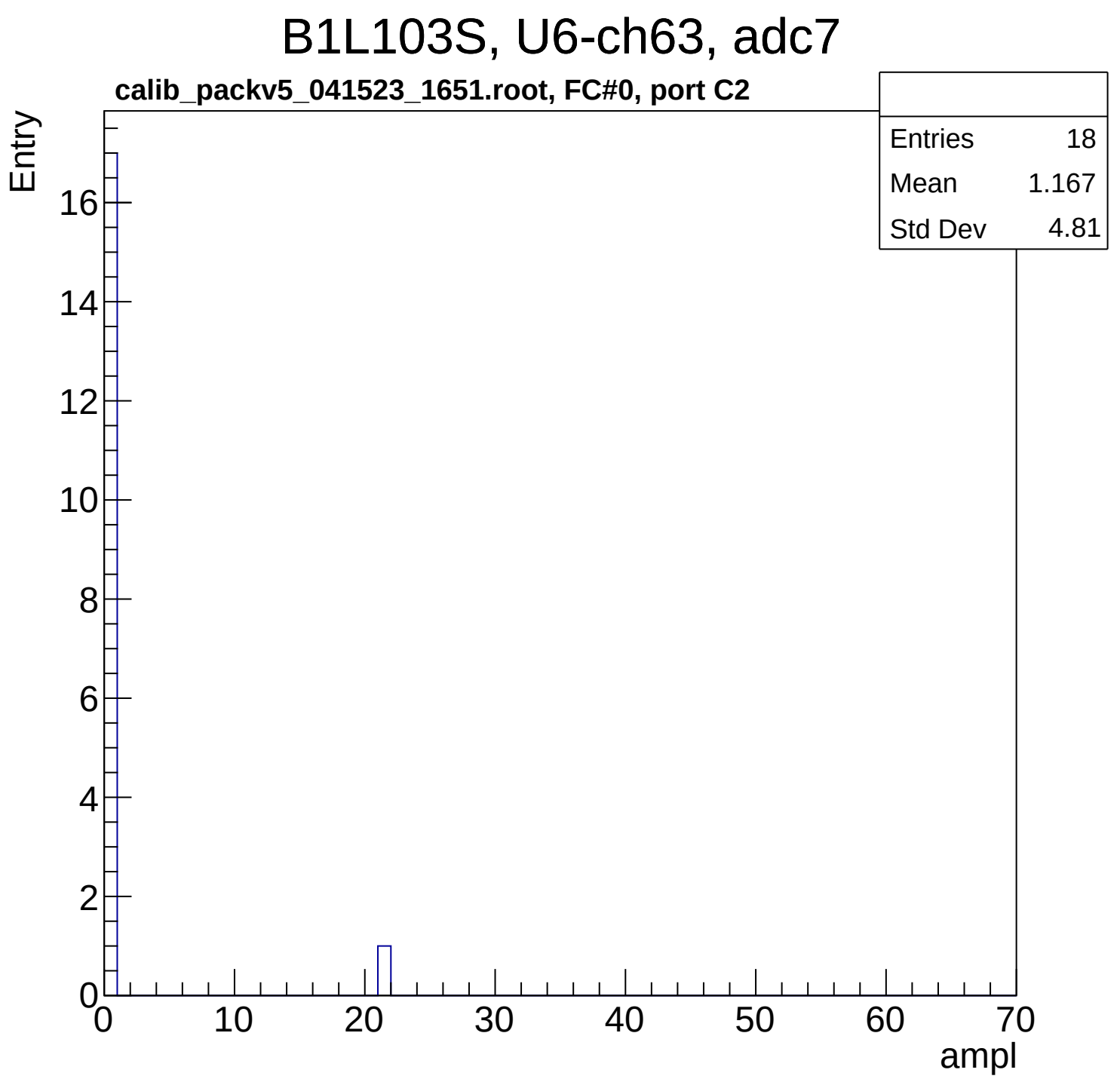
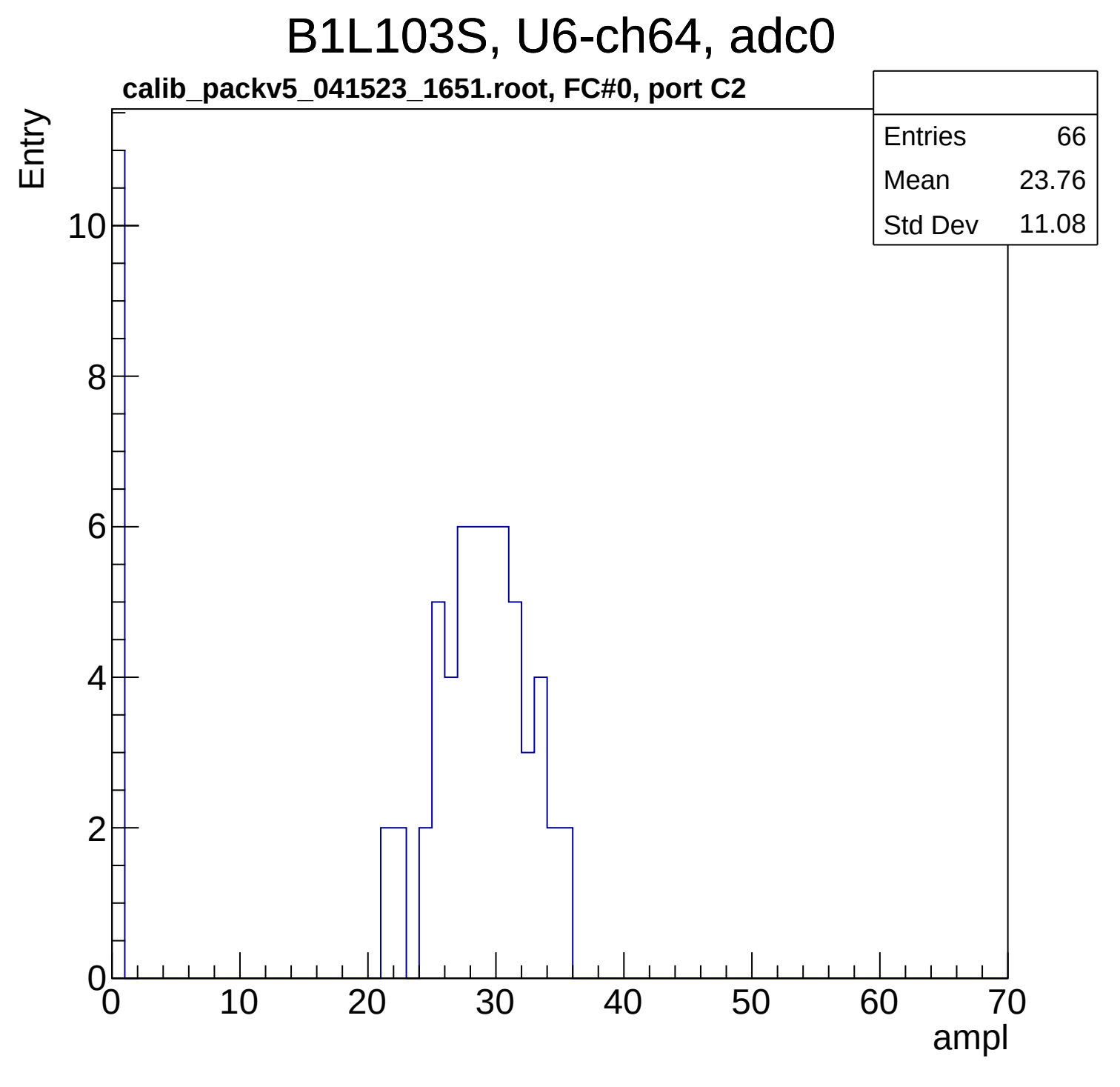
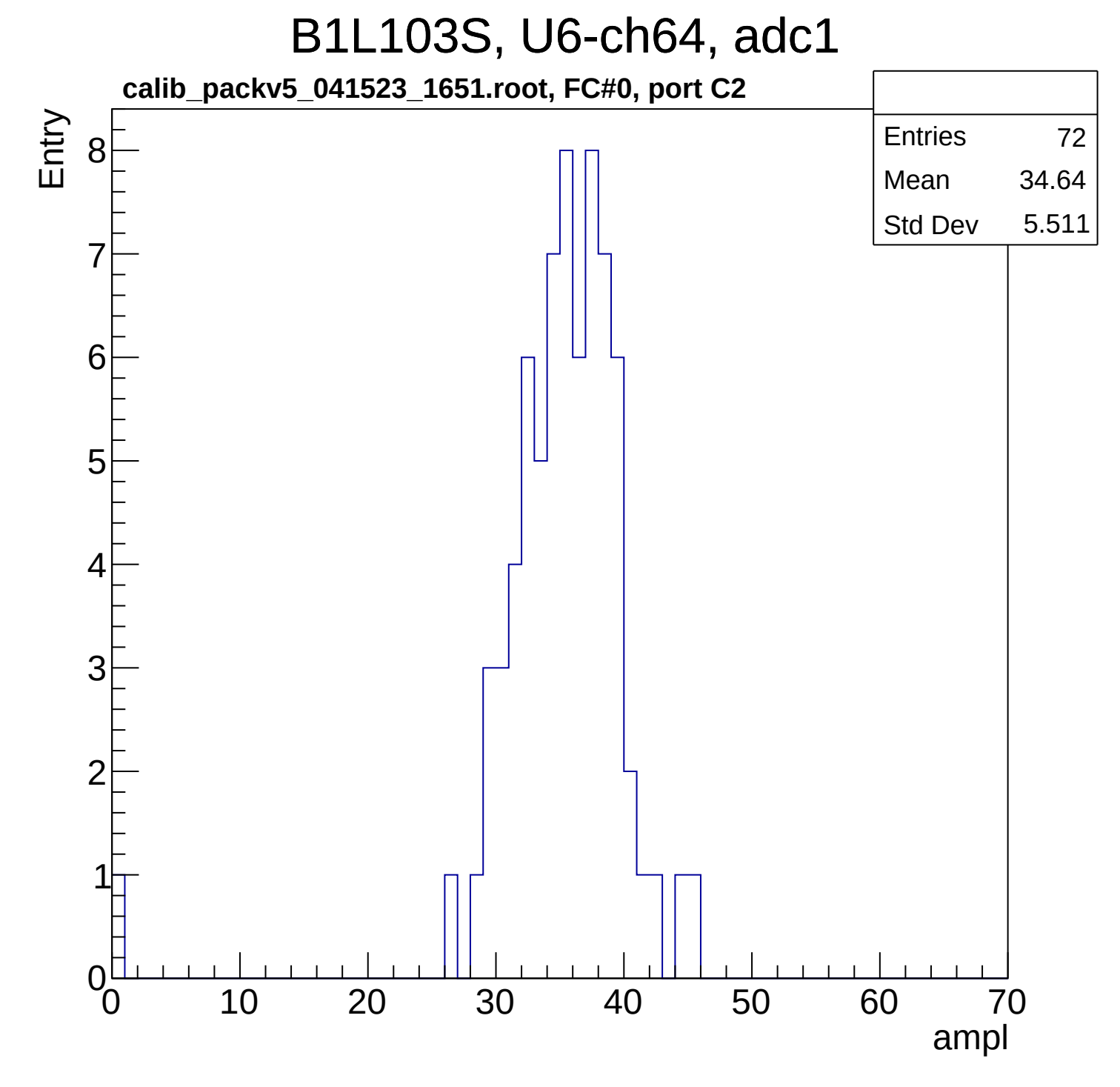
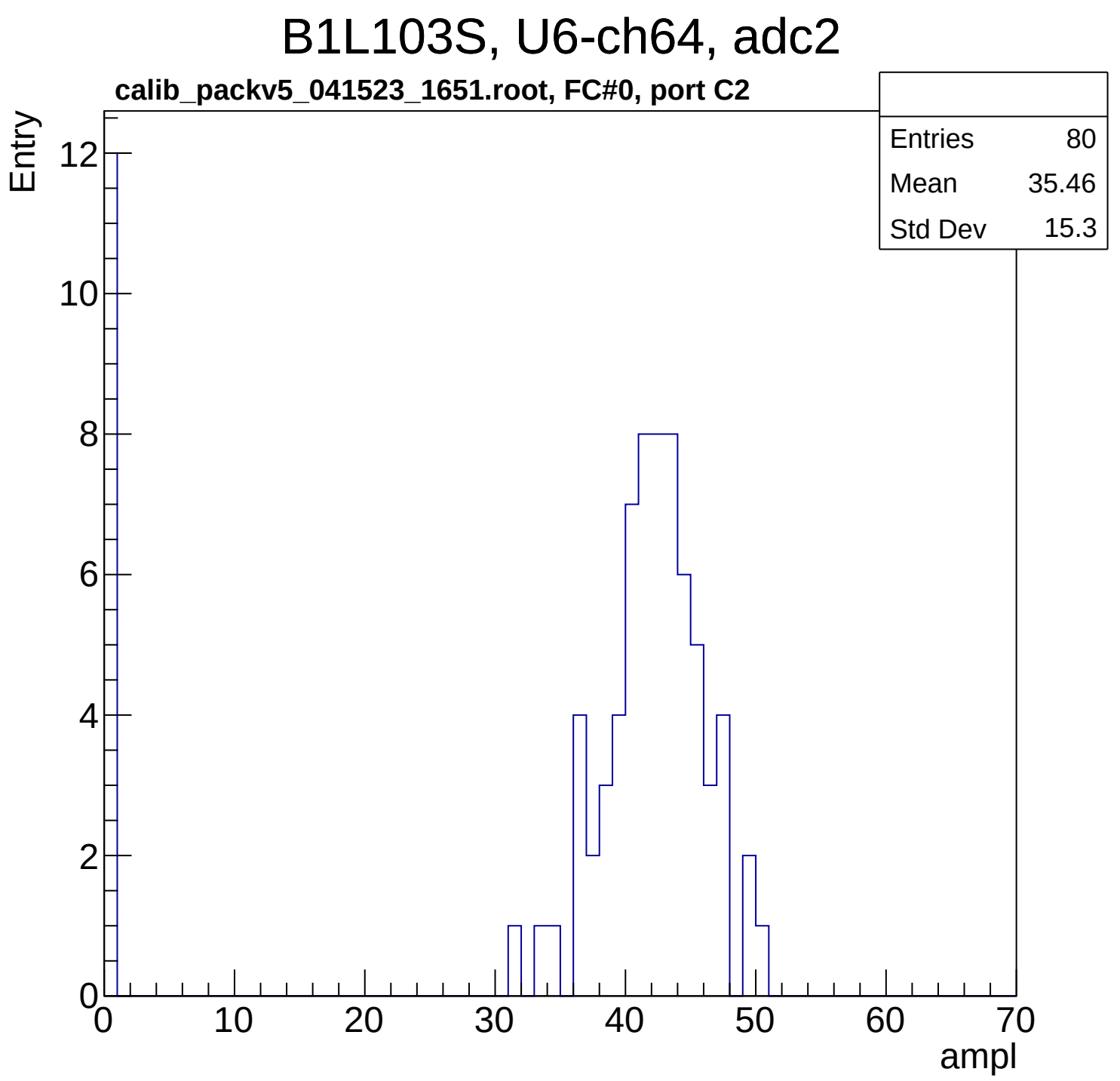
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

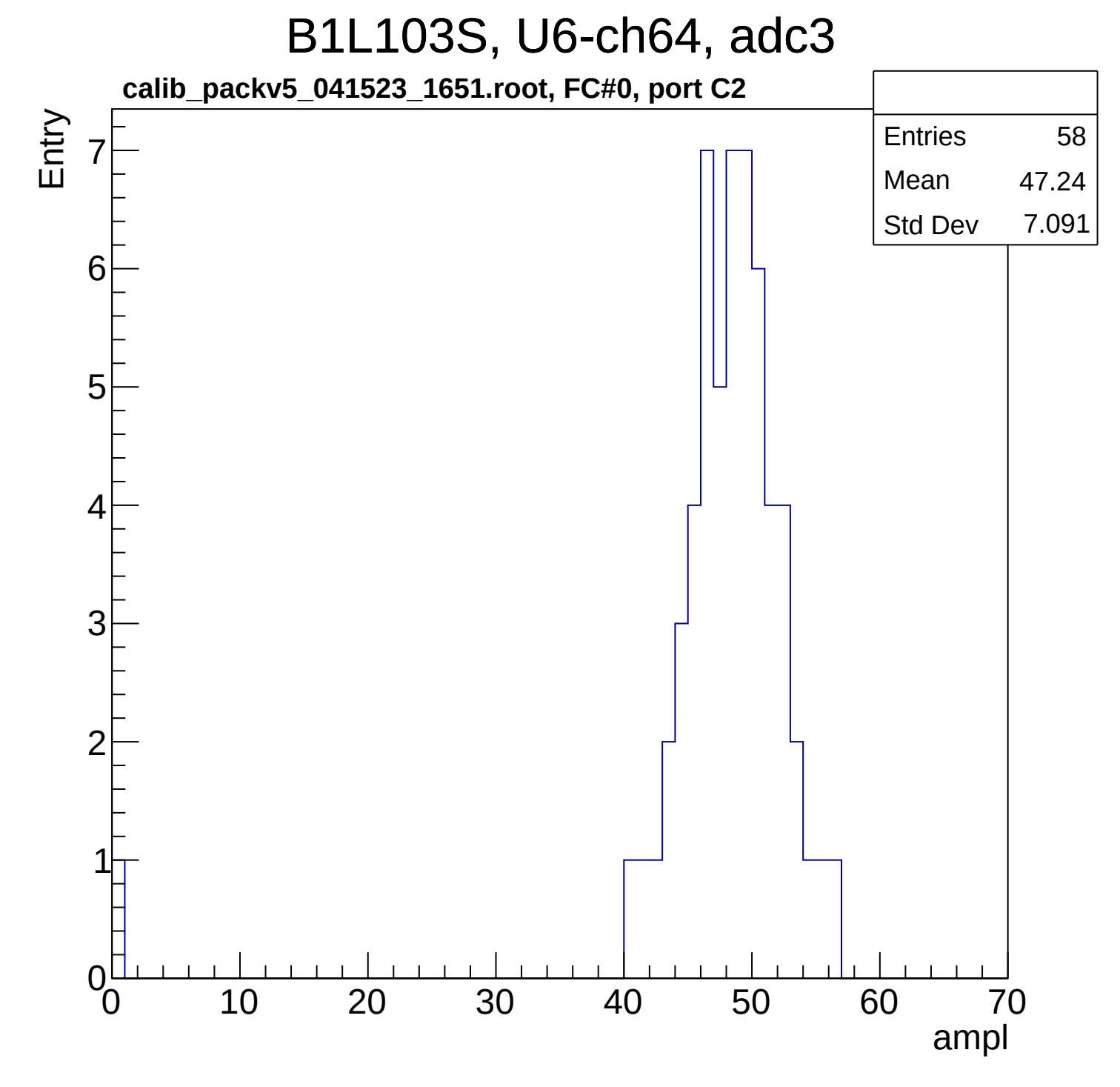

B1L103S, U6-ch63, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 61.5
Std Dev 1.384
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

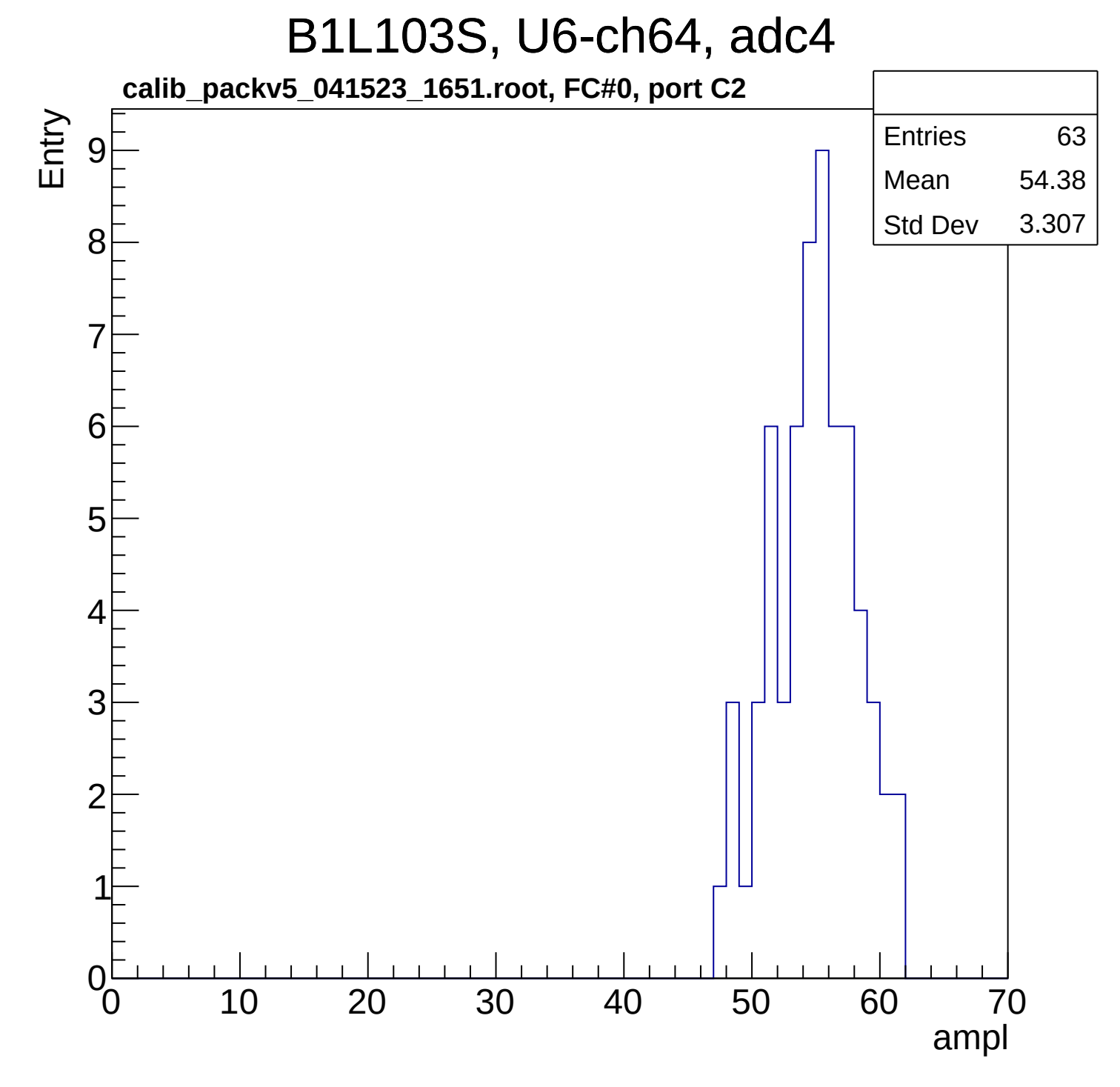

B1L103S, U6-ch63, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.167
Std Dev 4.81
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch64, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 23.76
Std Dev 11.08
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch64, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 34.64
Std Dev 5.511
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch64, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 35.46
Std Dev 15.3
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch64, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 47.24
Std Dev 7.091
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U6-ch64, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 54.38
Std Dev 3.307
Entry
ampl
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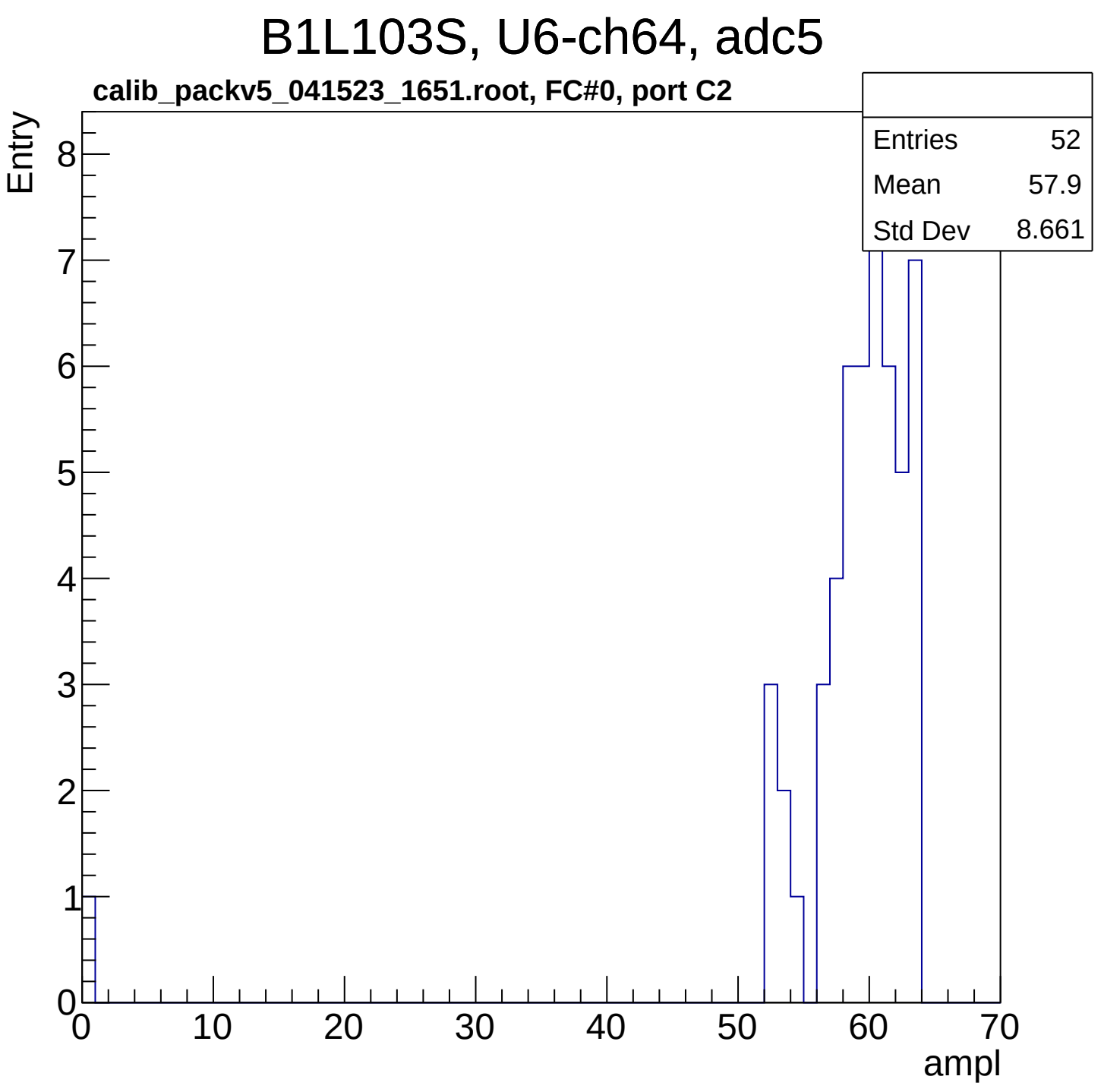
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch64, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 57.9
Std Dev 8.661
Entry
ampl
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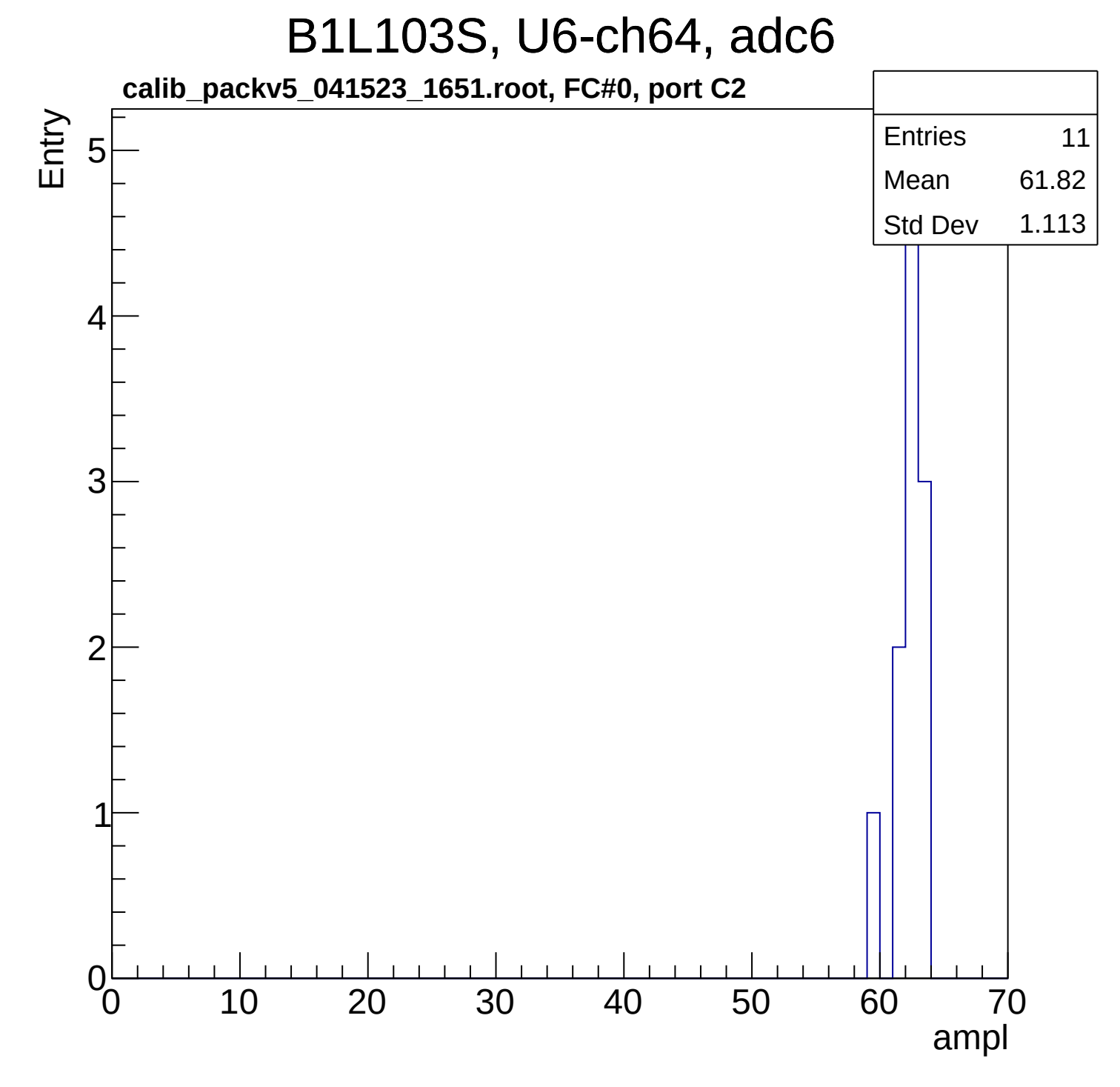
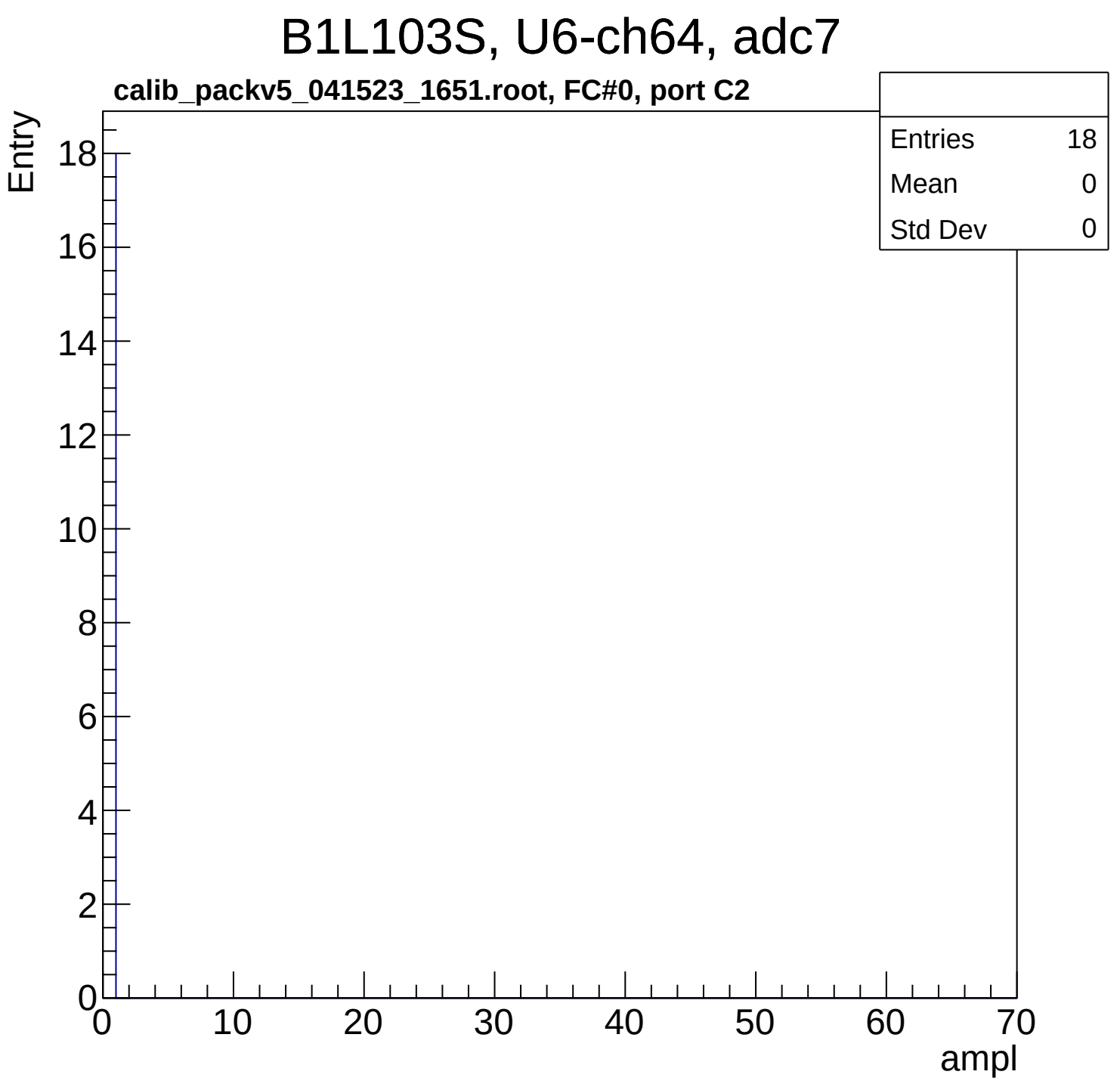
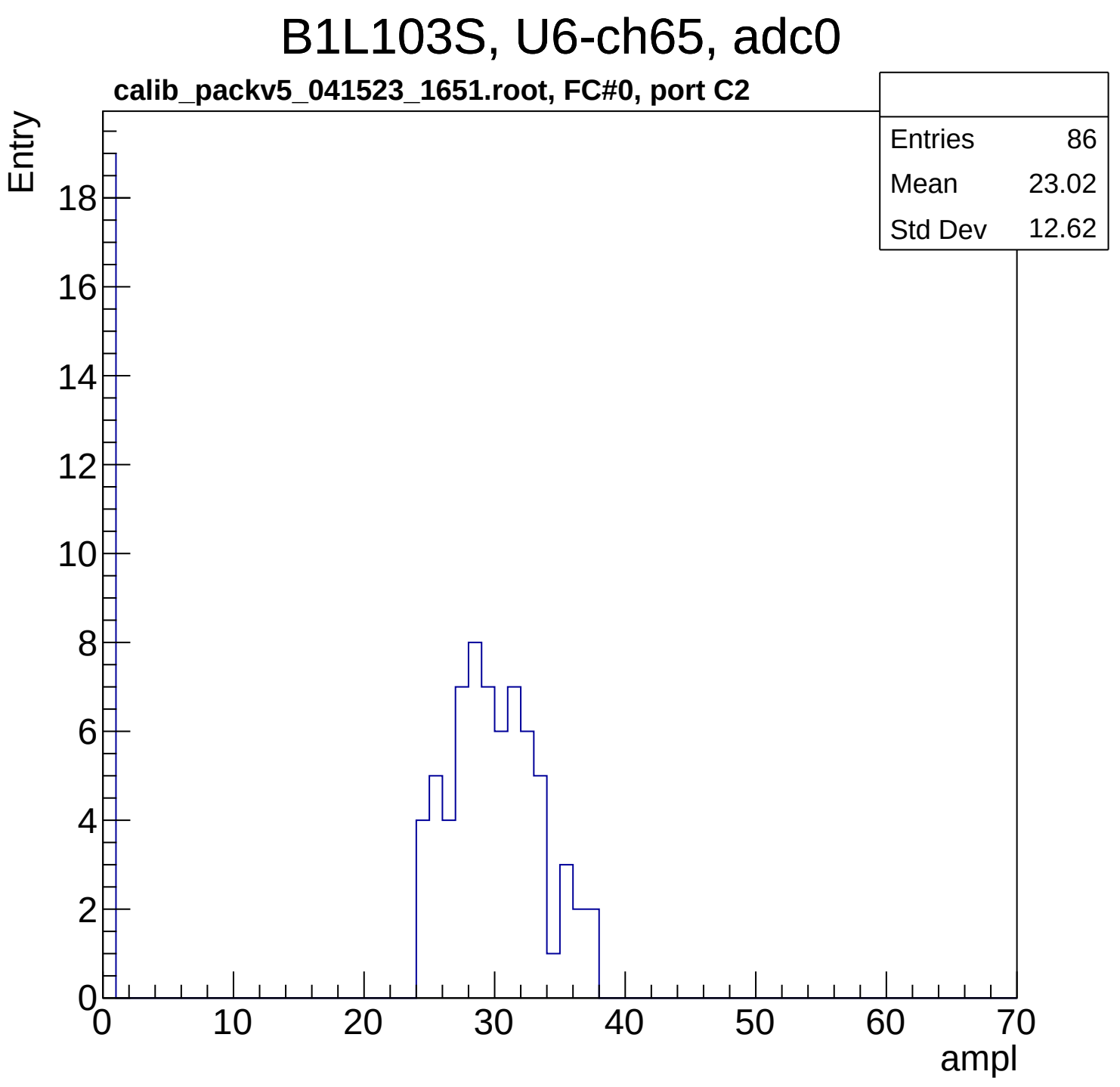
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch64, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 61.82
Std Dev 1.113
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U6-ch64, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch65, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 23.02
Std Dev 12.62
Entry
0
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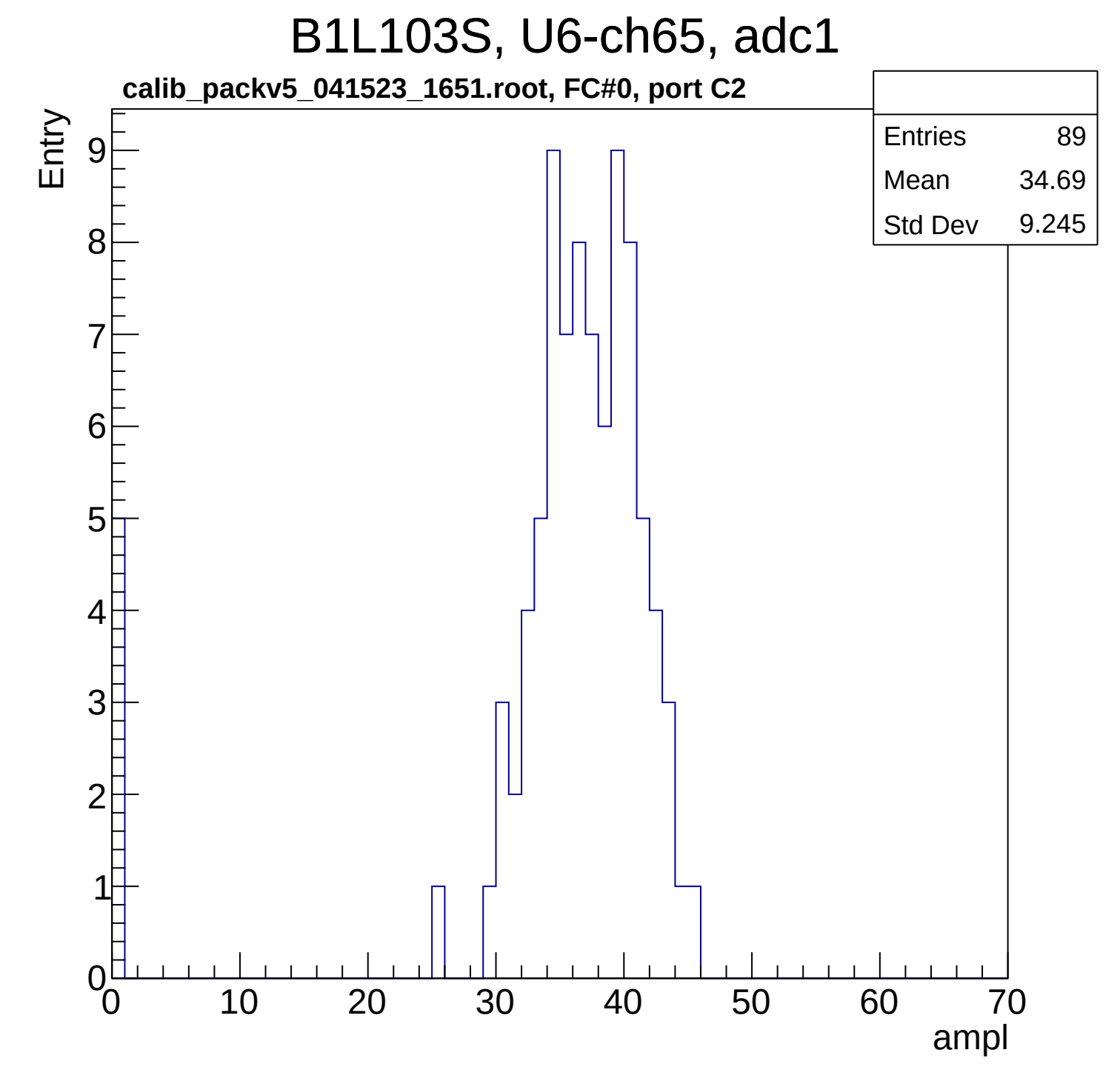
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch65, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 34.69
Std Dev 9.245
Entry
ampl
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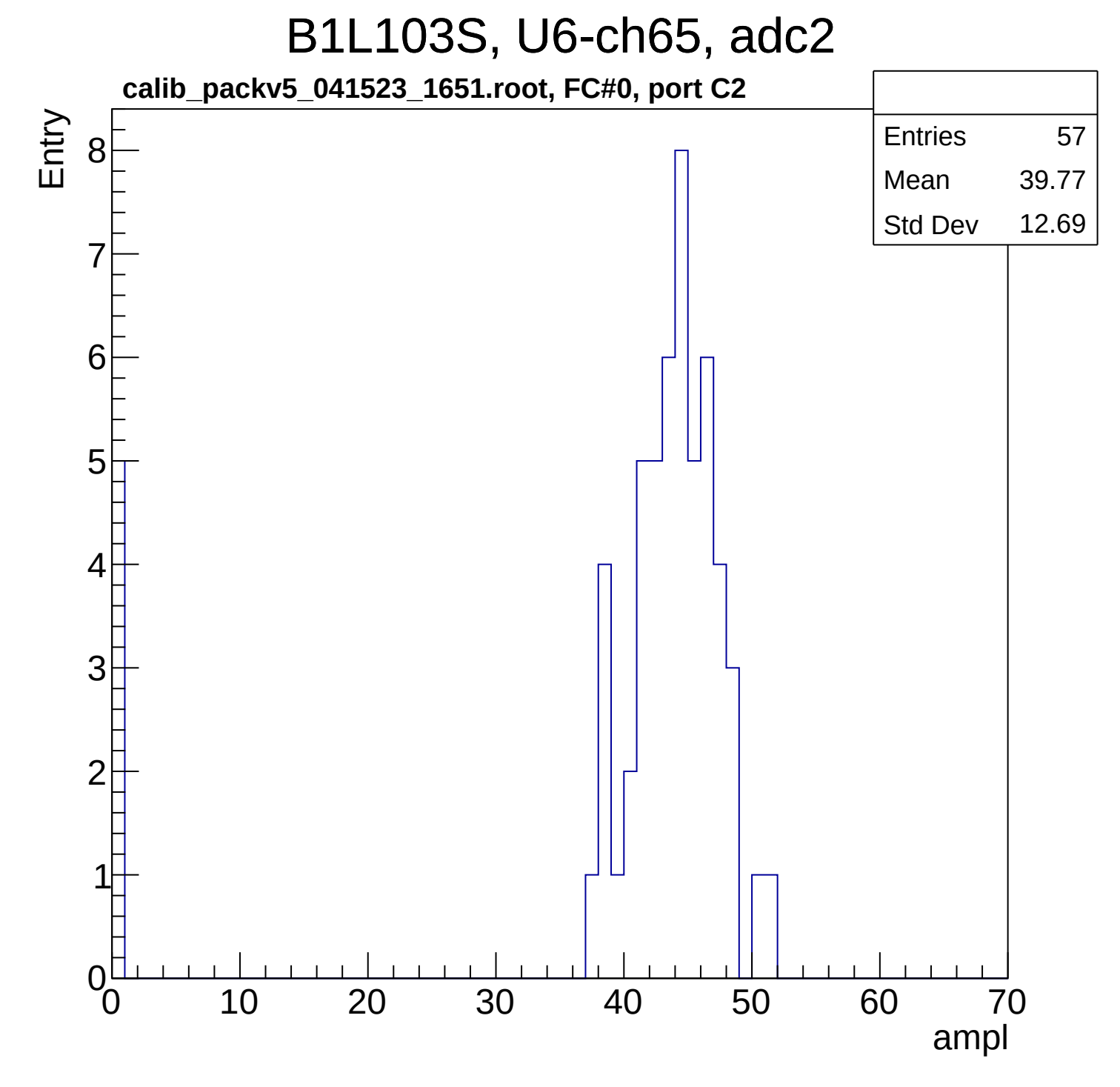
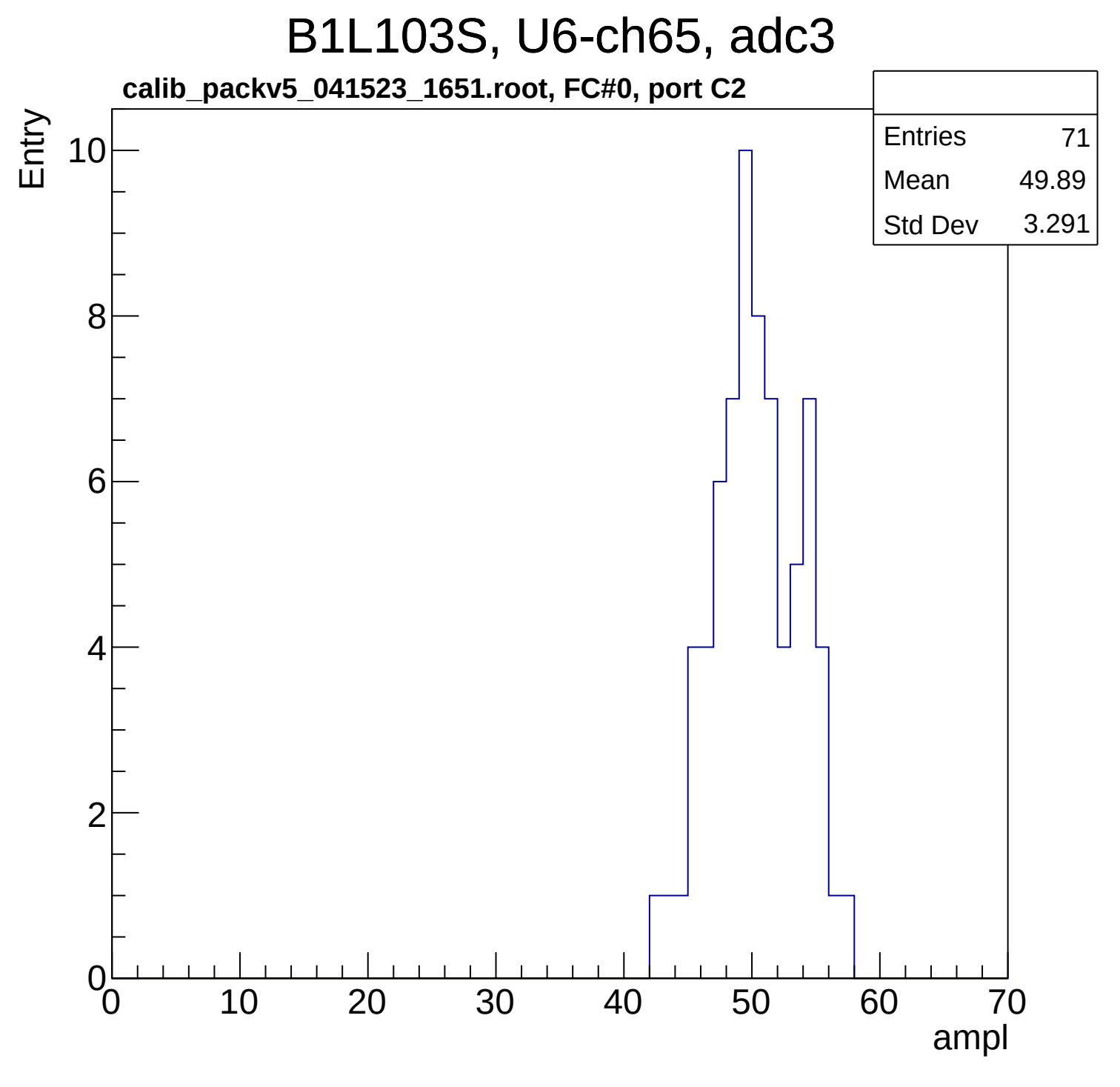
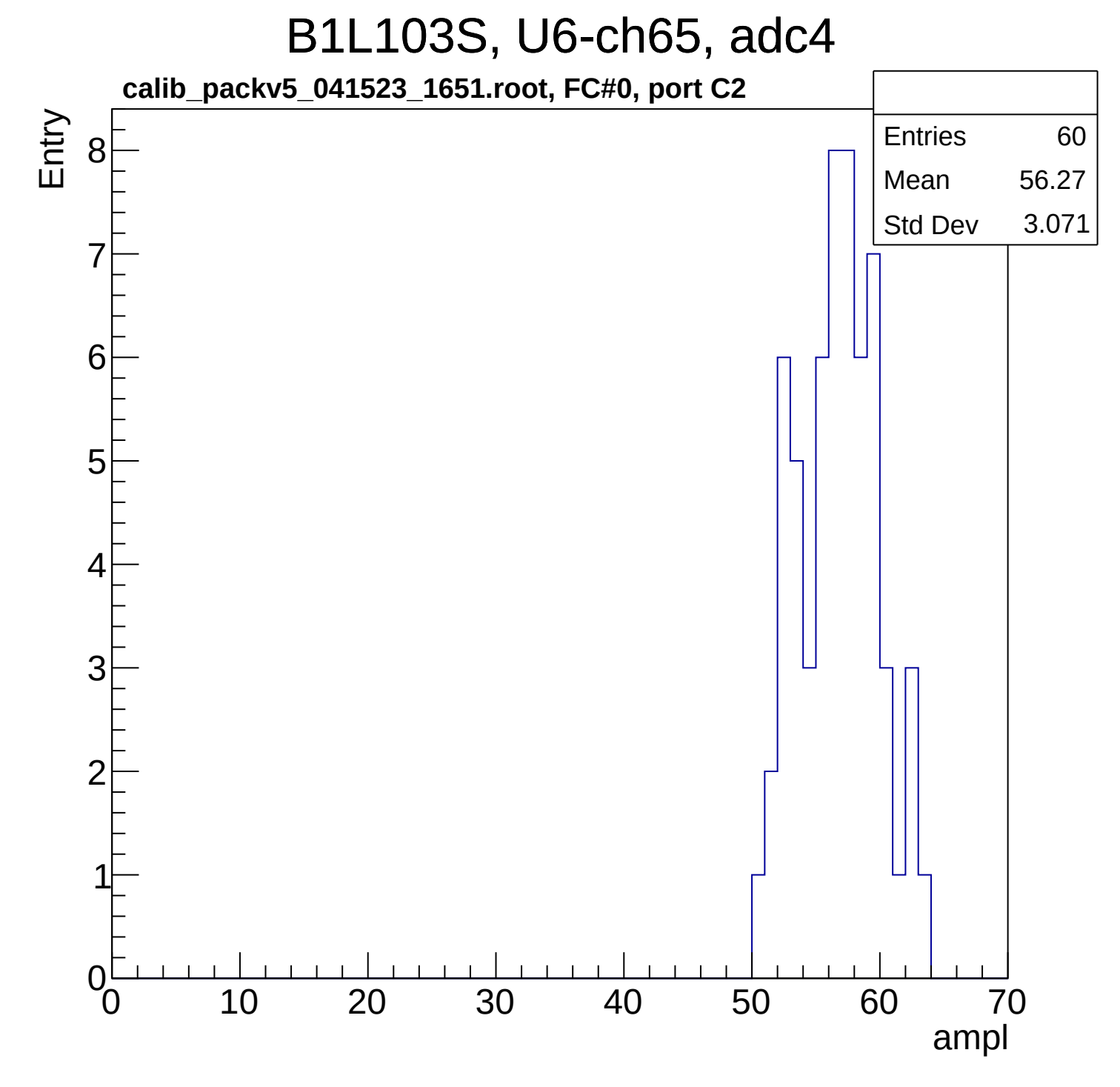
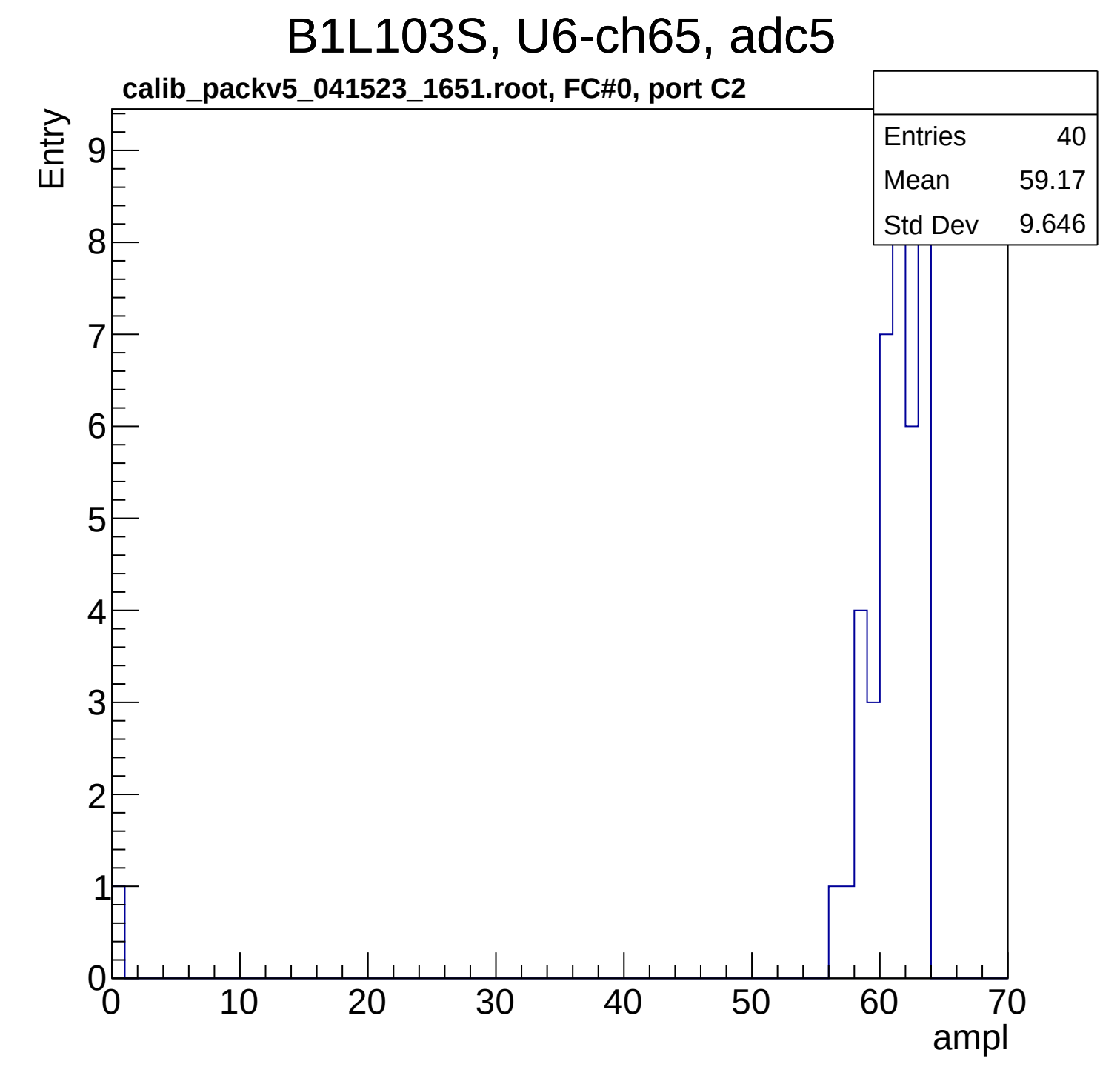
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch65, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 39.77
Std Dev 12.69
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch65, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 49.89
Std Dev 3.291
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U6-ch65, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 56.27
Std Dev 3.071
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch65, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 59.17
Std Dev 9.646
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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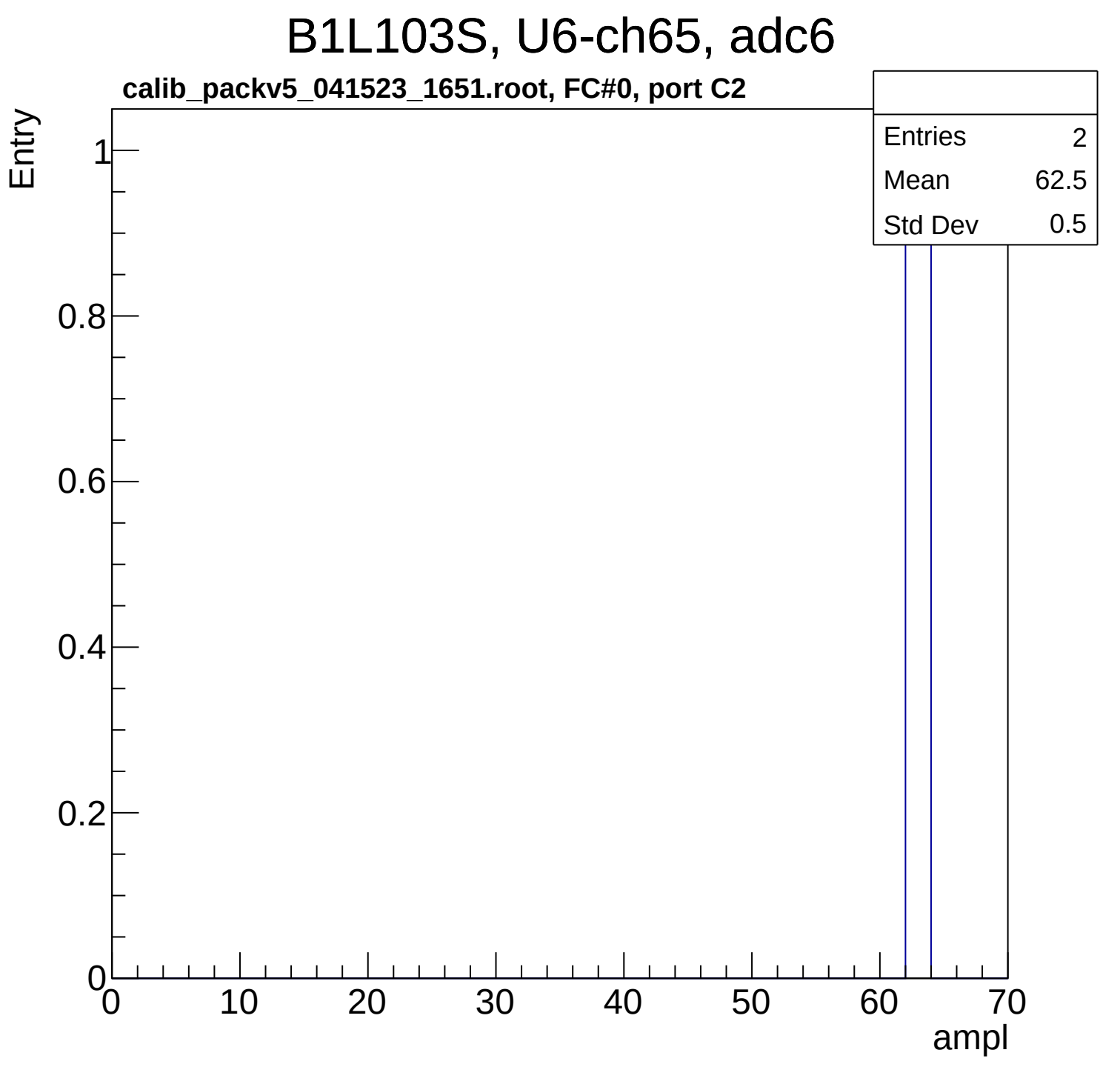
B1L103S, U6-ch65, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
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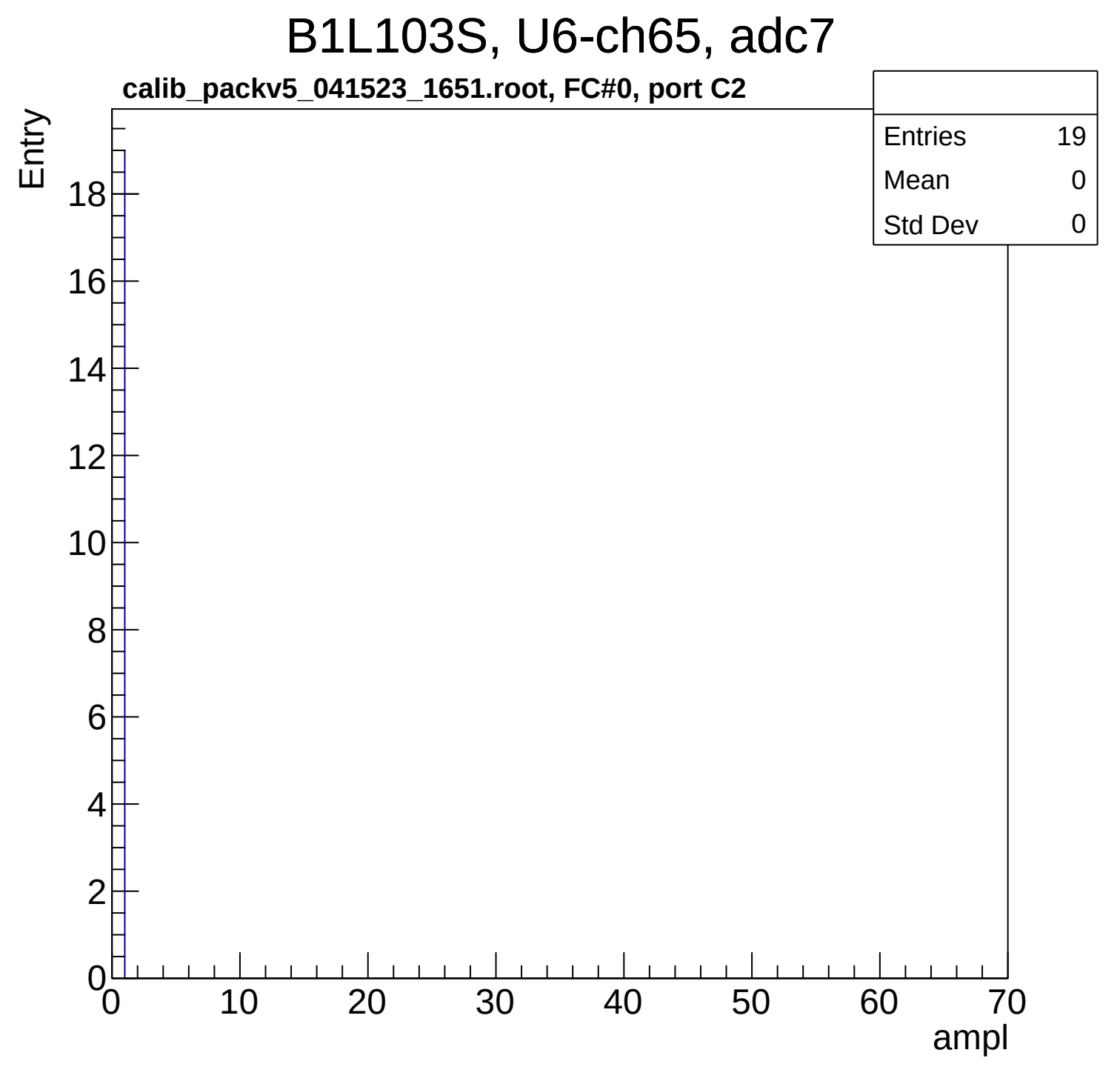
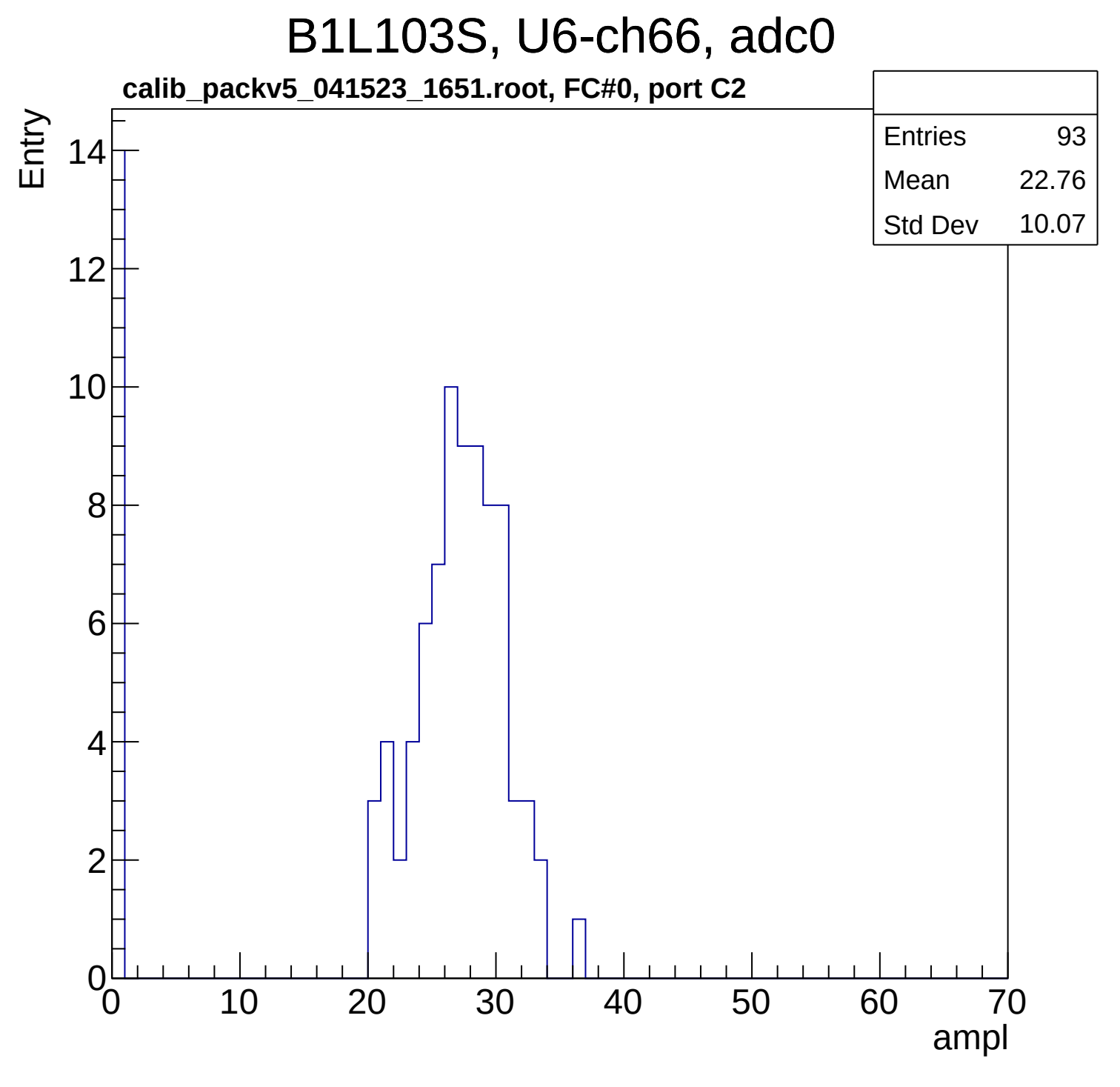
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch65, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch66, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 22.76
Std Dev 10.07
Entry
ampl
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2
4
6
8
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0
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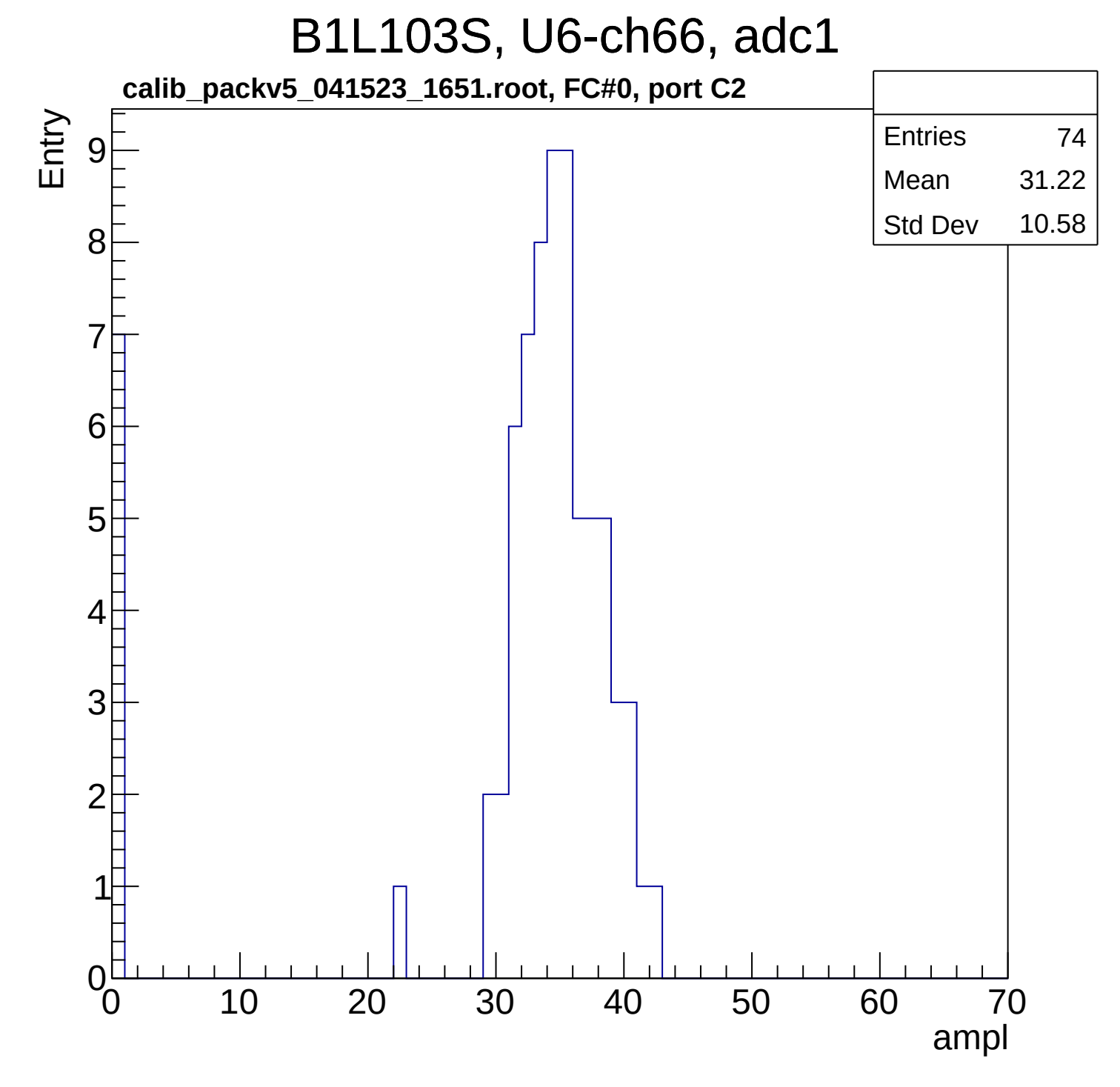
B1L103S, U6-ch66, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 31.22
Std Dev 10.58
Entry
ampl
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4
5
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7
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0
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60
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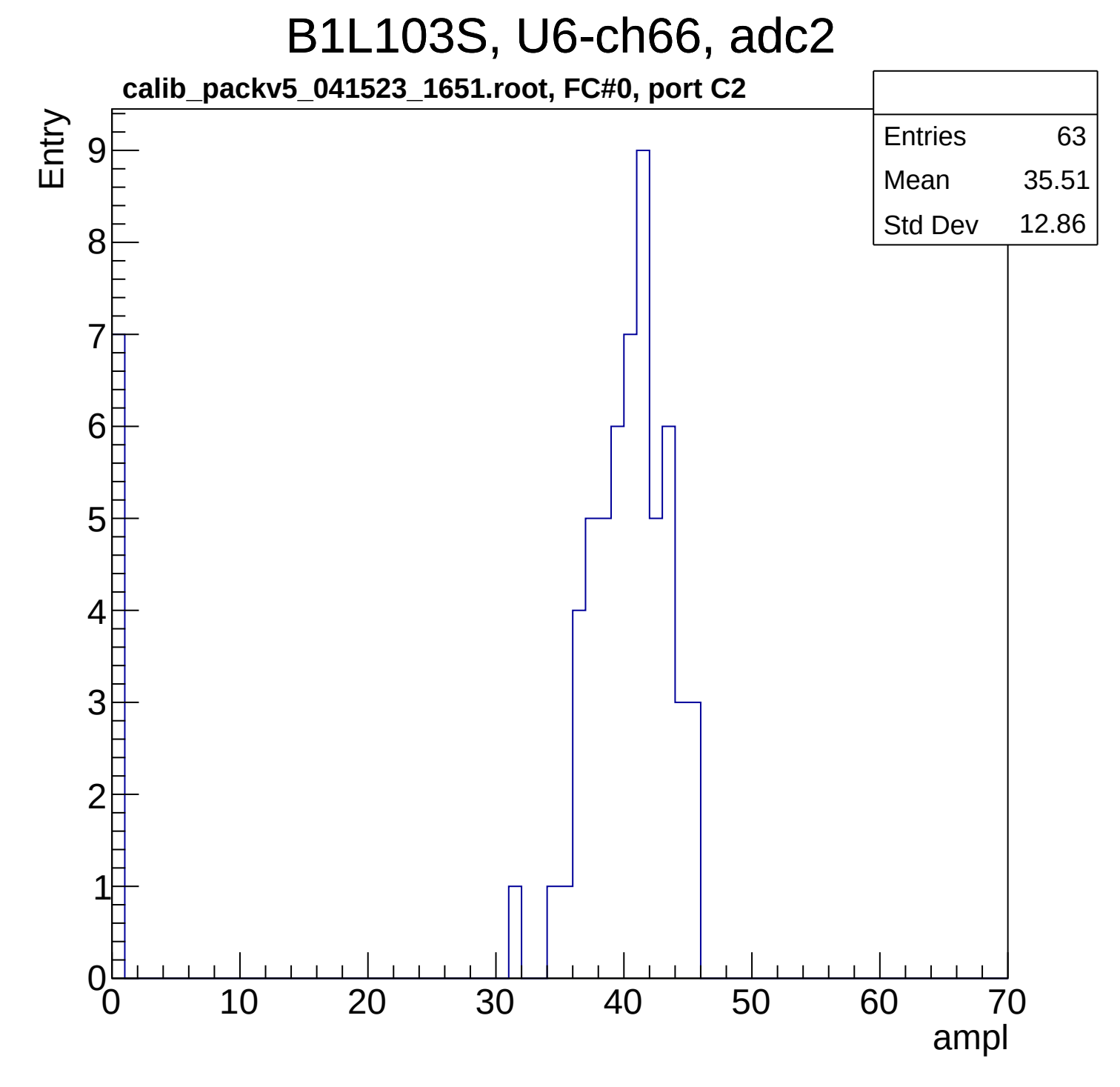
B1L103S, U6-ch66, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 35.51
Std Dev 12.86
Entry
ampl
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3
4
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6
7
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0
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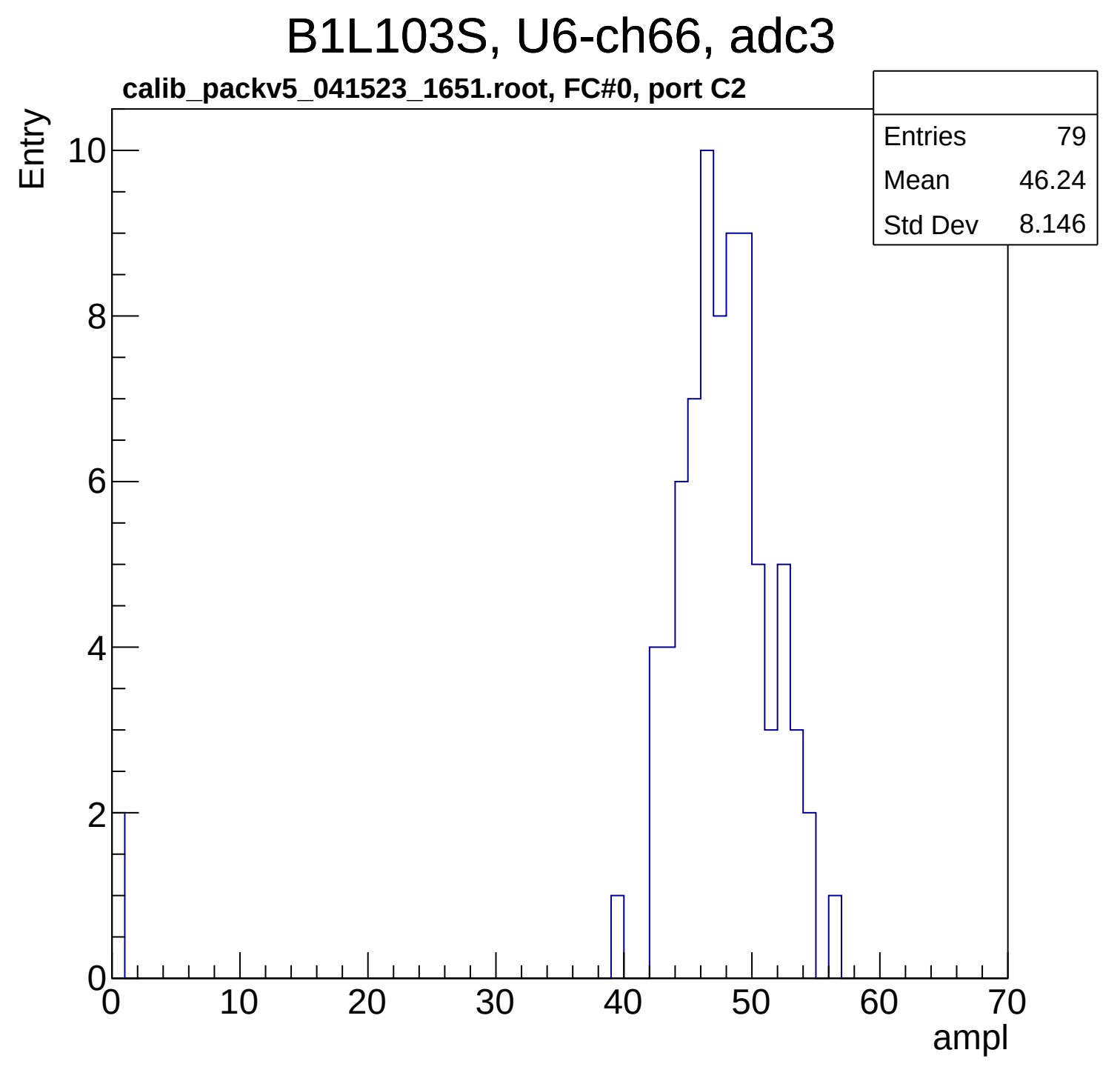
B1L103S, U6-ch66, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 46.24
Std Dev 8.146
Entry
ampl
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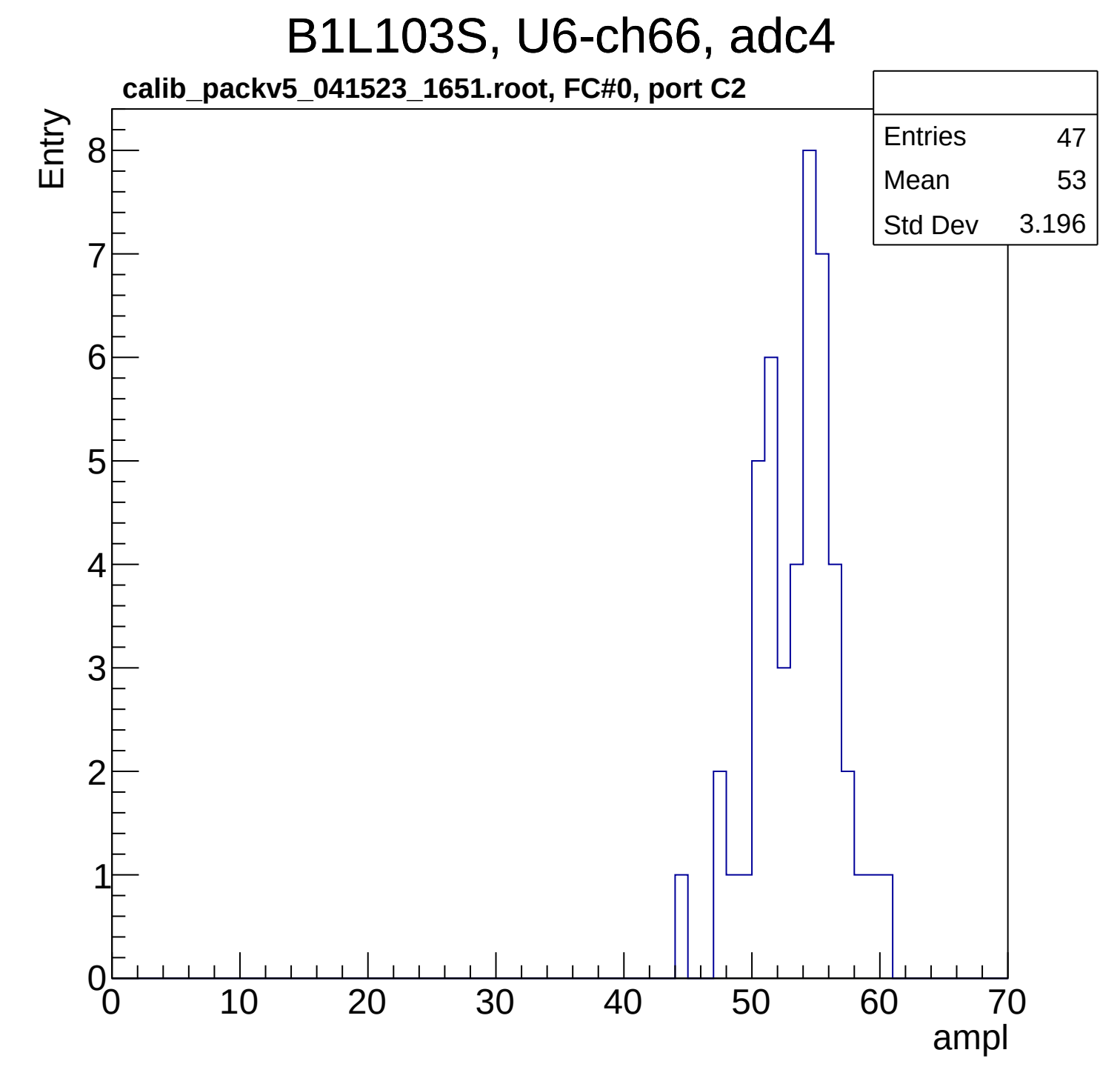
B1L103S, U6-ch66, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 53
Std Dev 3.196
Entry
ampl
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2
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4
5
6
7
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0
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40
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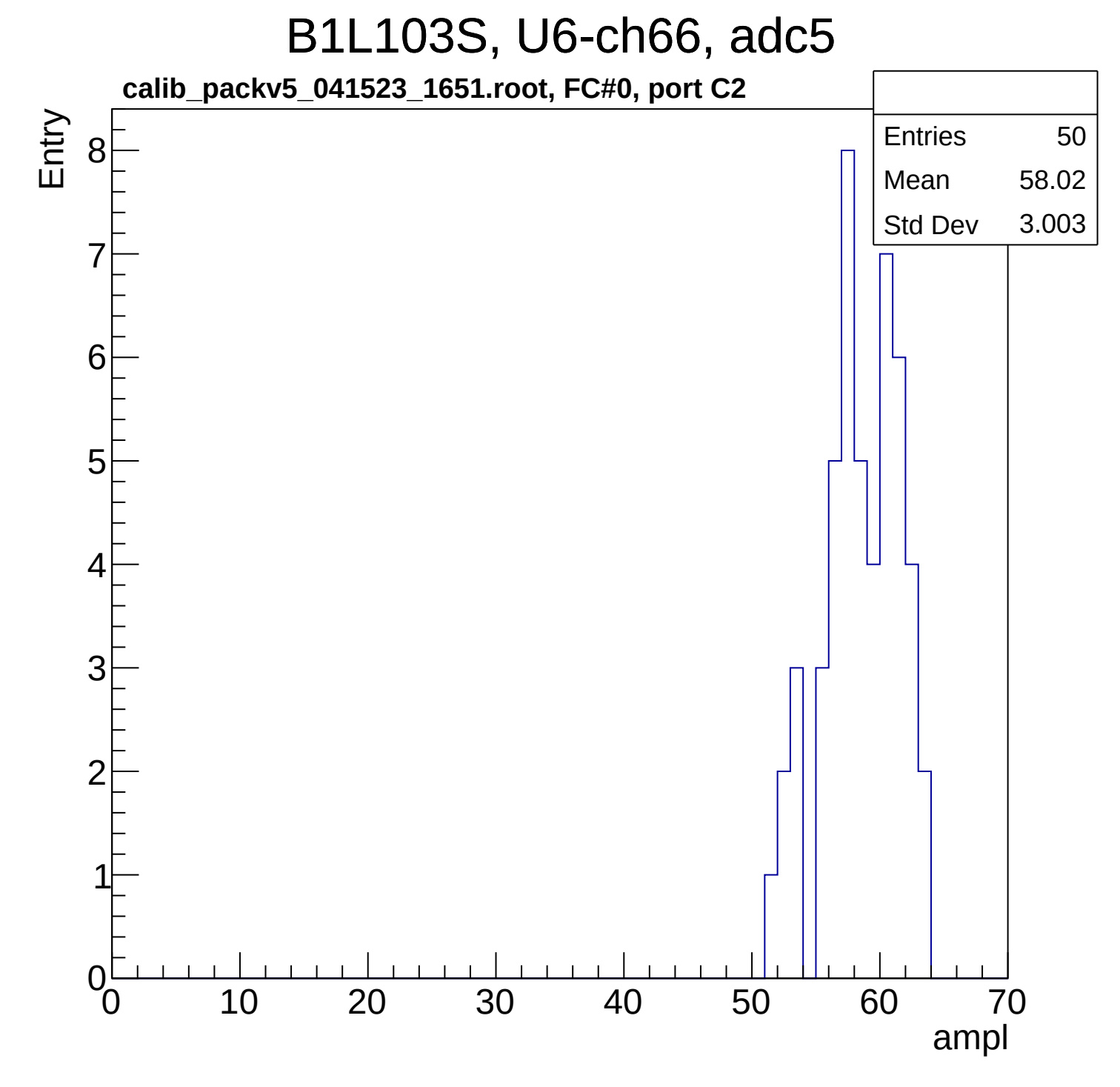
B1L103S, U6-ch66, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 58.02
Std Dev 3.003
Entry
ampl
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3
4
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0
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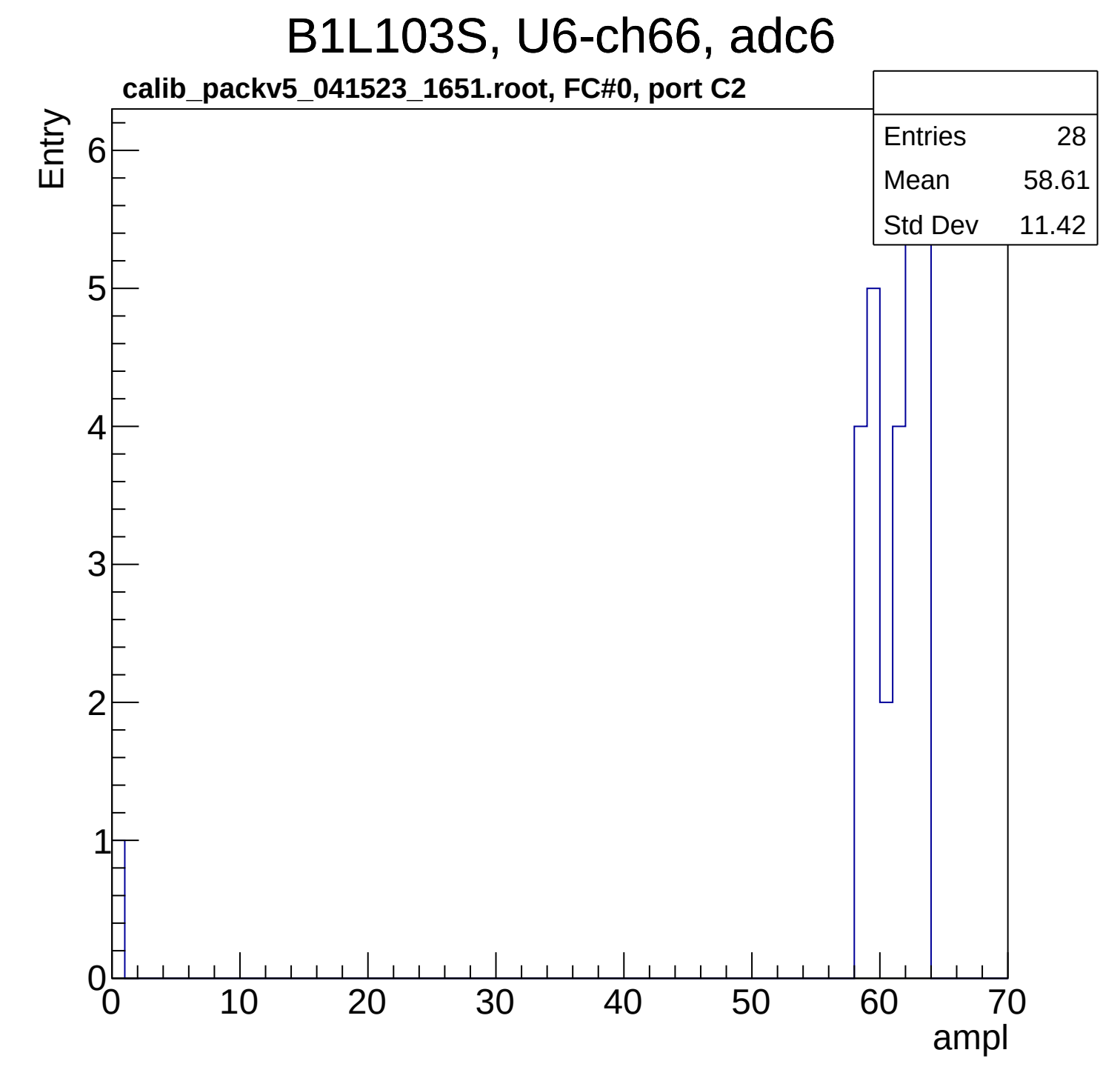
B1L103S, U6-ch66, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 58.61
Std Dev 11.42
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
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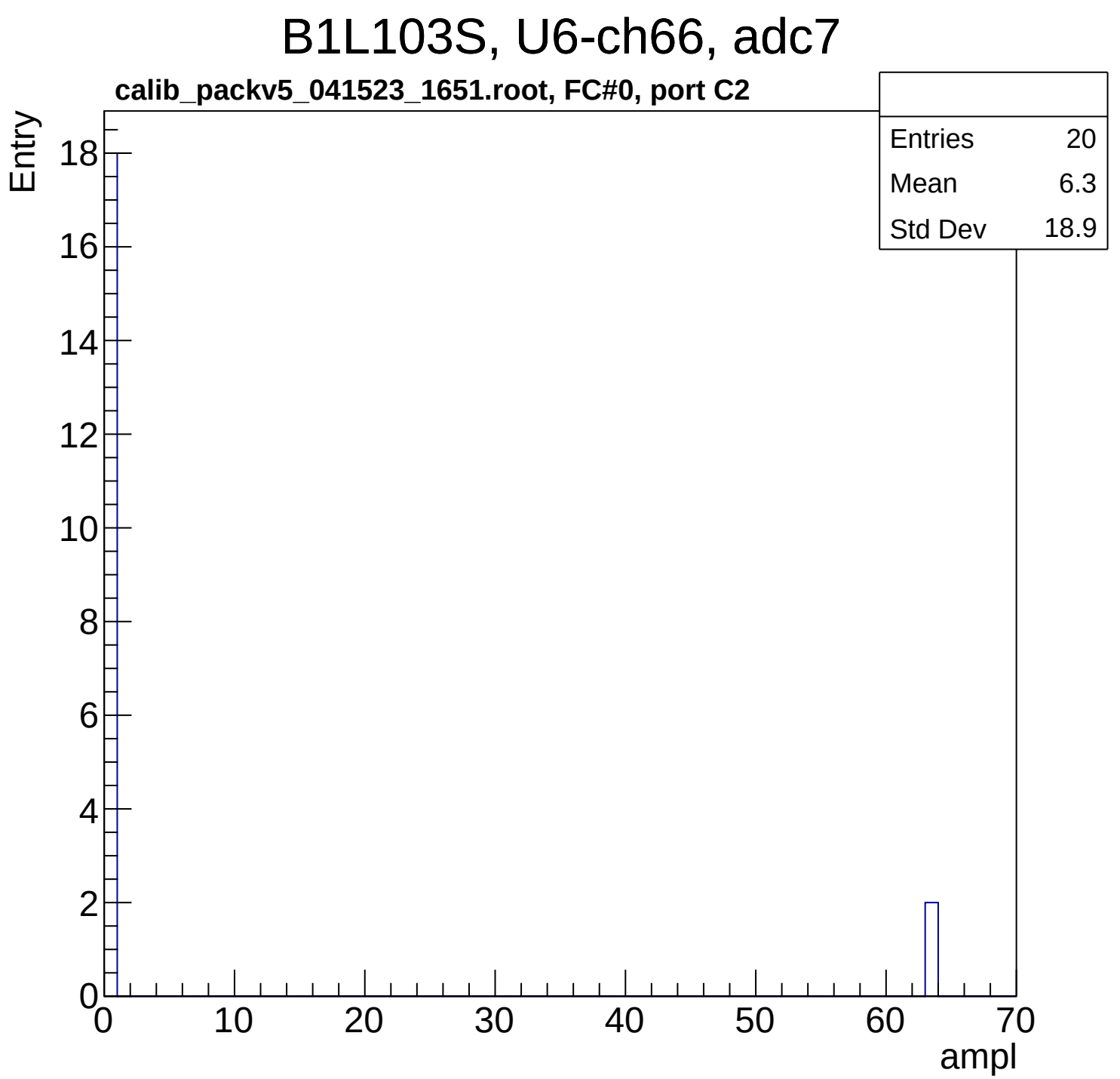
B1L103S, U6-ch66, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 6.3
Std Dev 18.9
Entry
0
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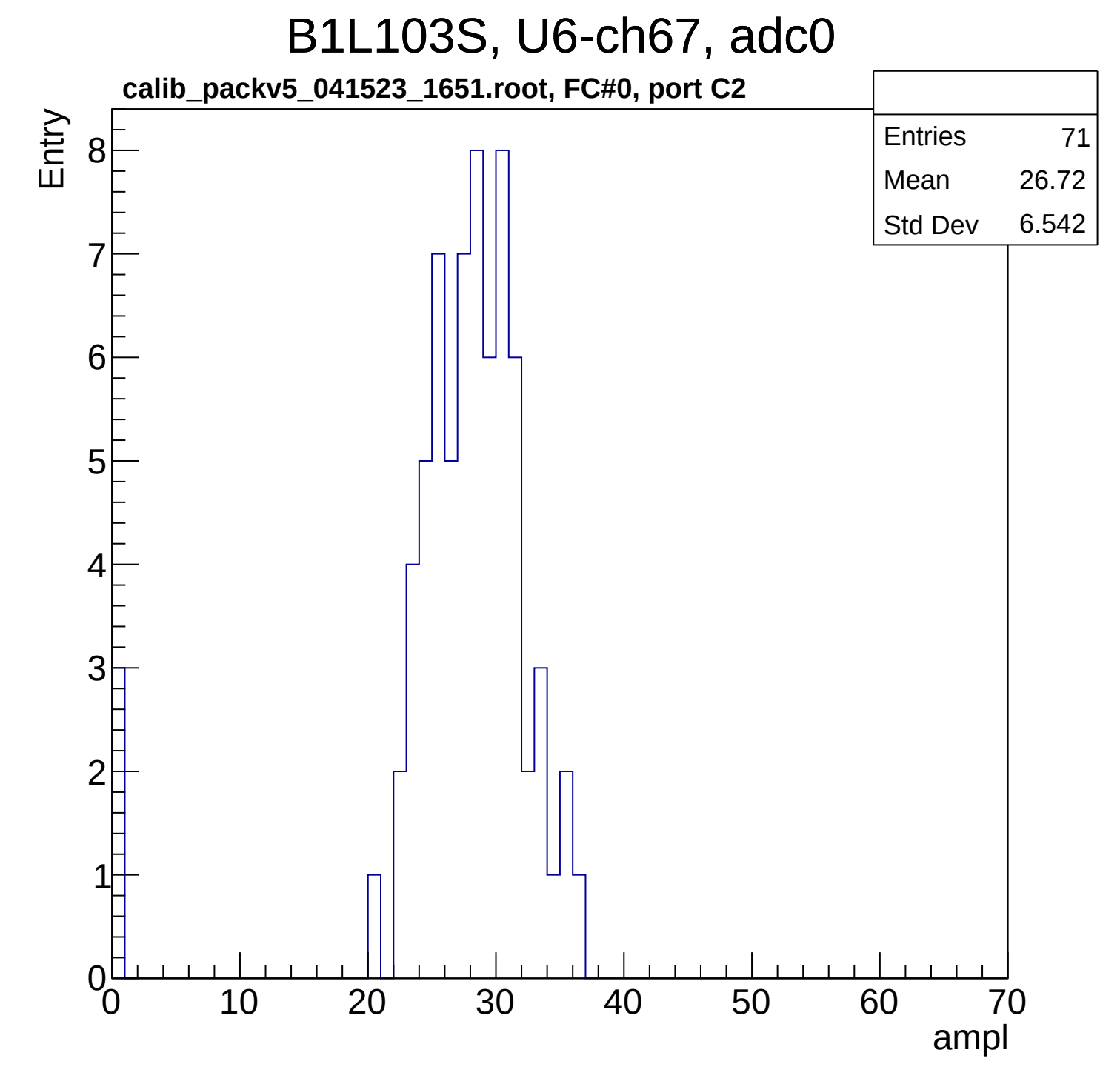
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch67, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 26.72
Std Dev 6.542
Entry
ampl
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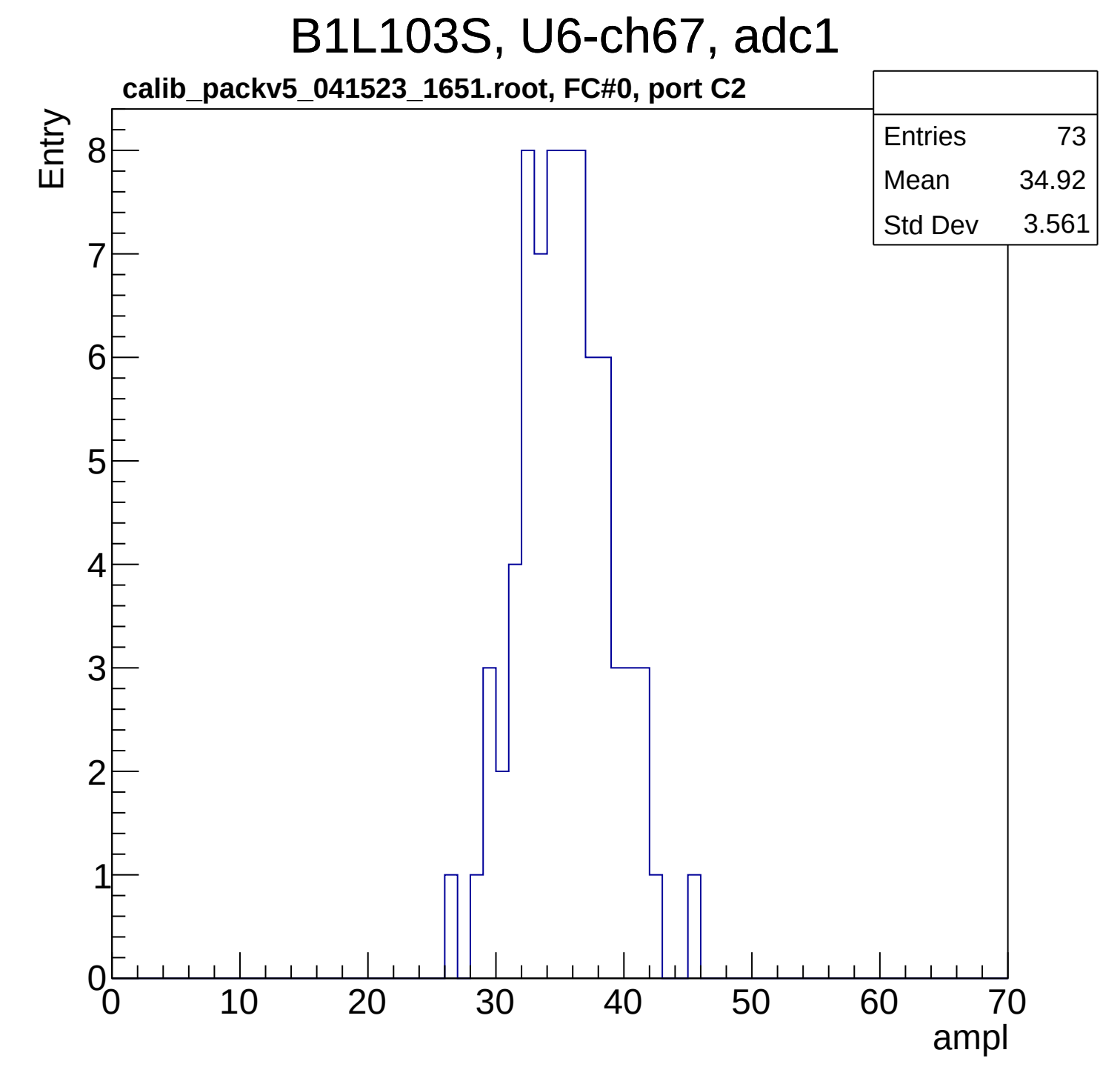
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch67, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 34.92
Std Dev 3.561
Entry
ampl
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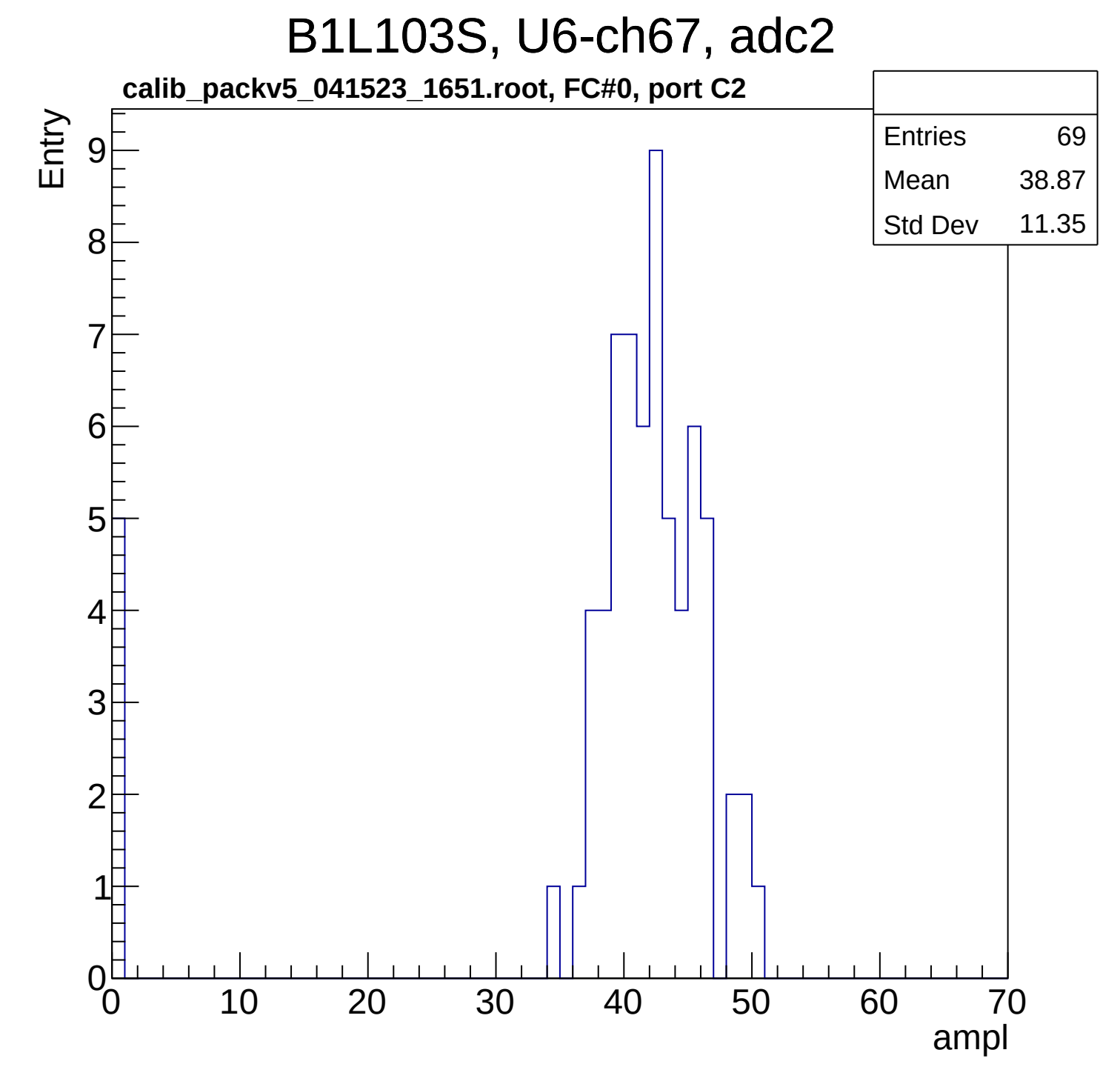
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch67, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 38.87
Std Dev 11.35
Entry
ampl
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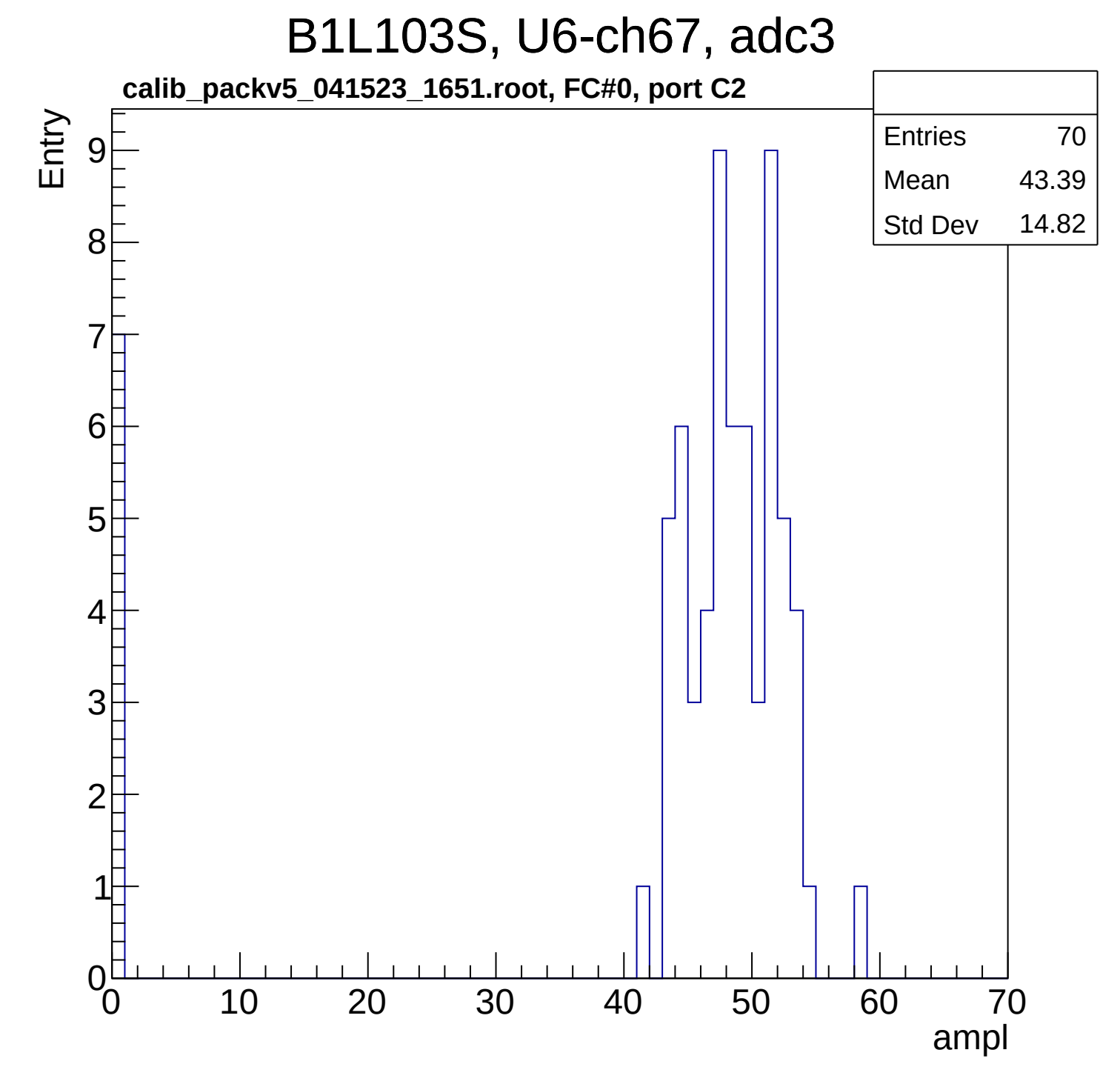
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch67, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 43.39
Std Dev 14.82
Entry
ampl
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2
3
4
5
6
7
8
9
0
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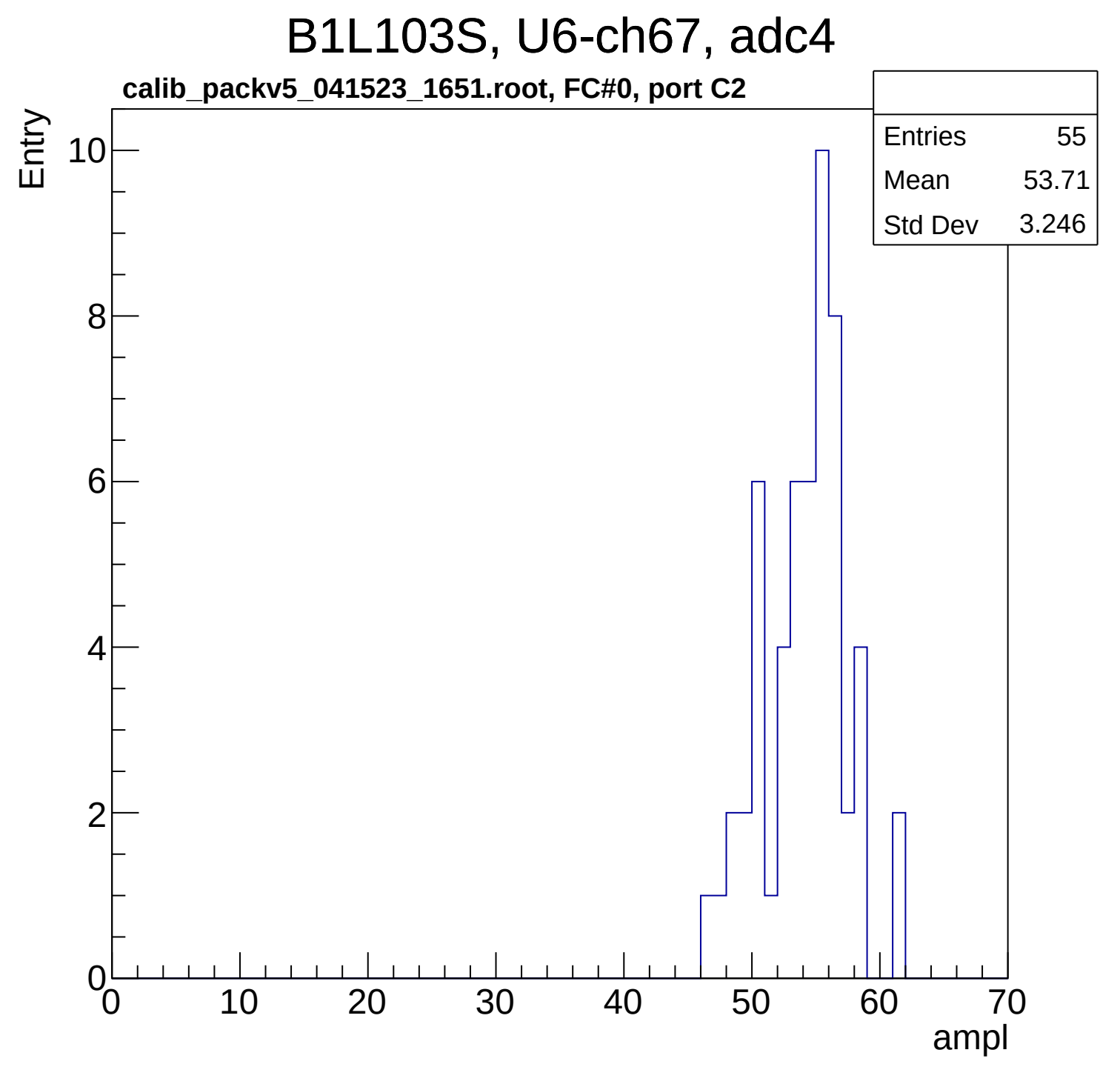
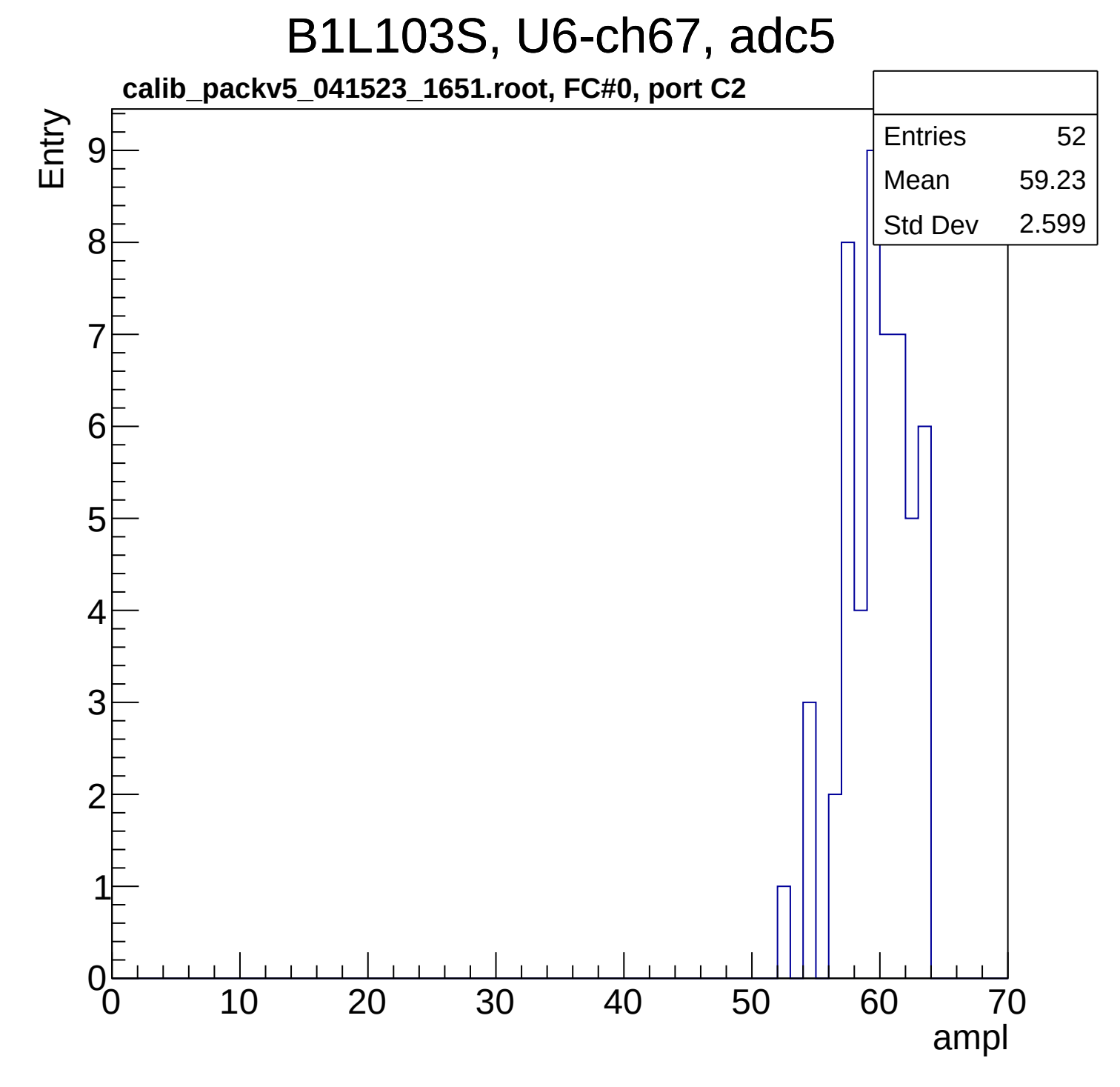
20
30
40
50
60
70


B1L103S, U6-ch67, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 53.71
Std Dev 3.246
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U6-ch67, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 59.23
Std Dev 2.599
Entry
ampl
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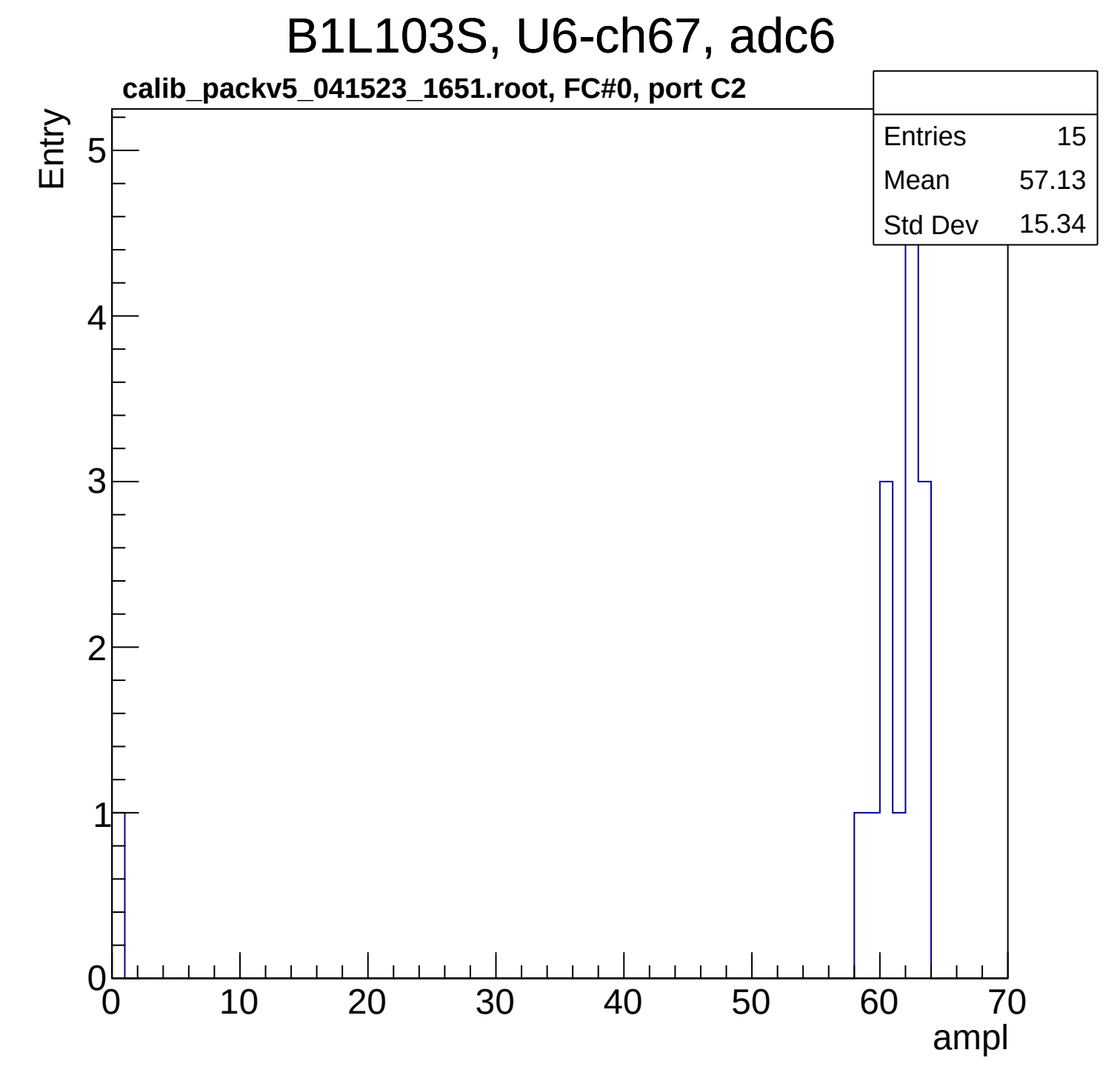
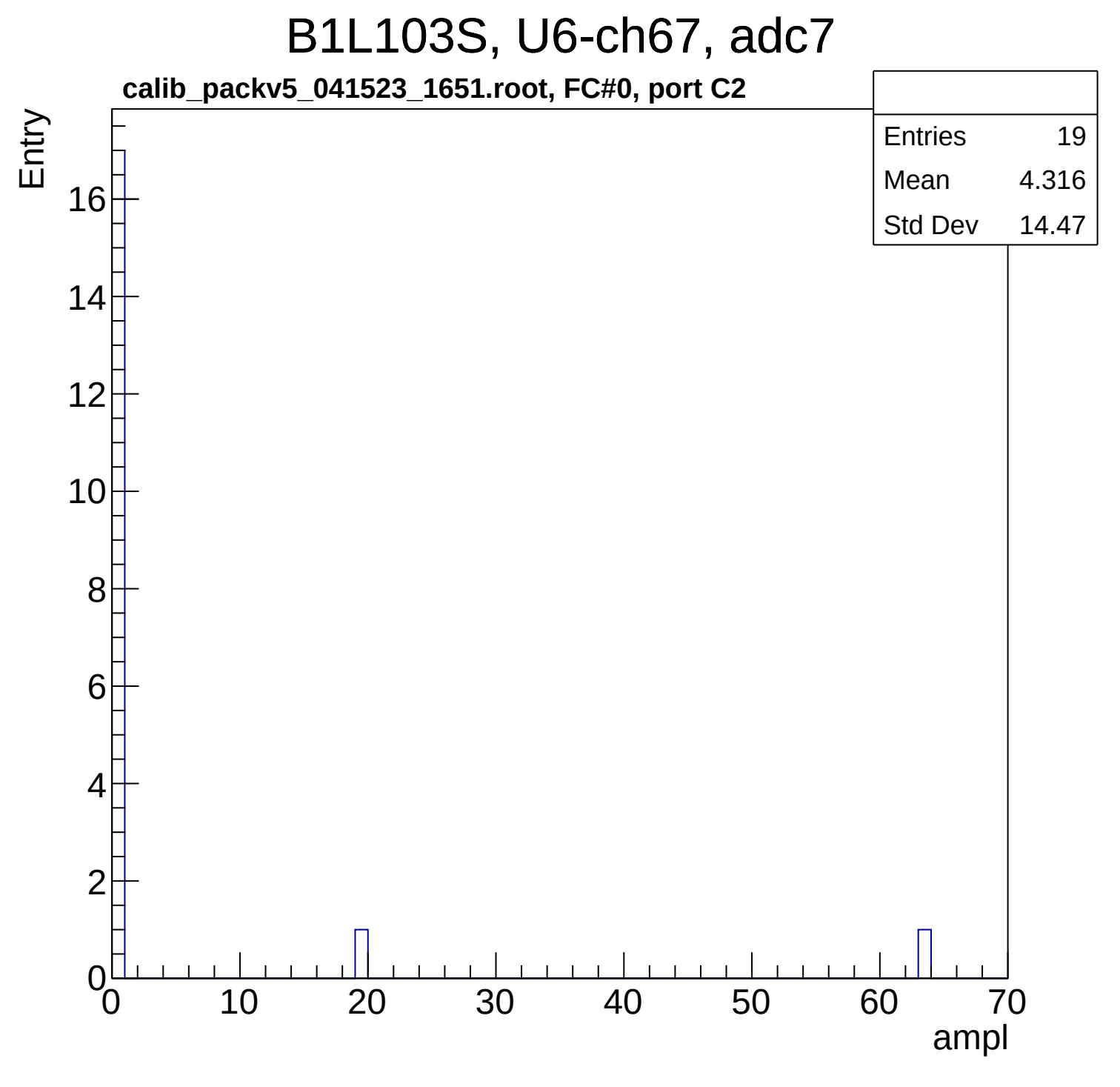
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch67, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 57.13
Std Dev 15.34
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch67, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 4.316
Std Dev 14.47
Entry
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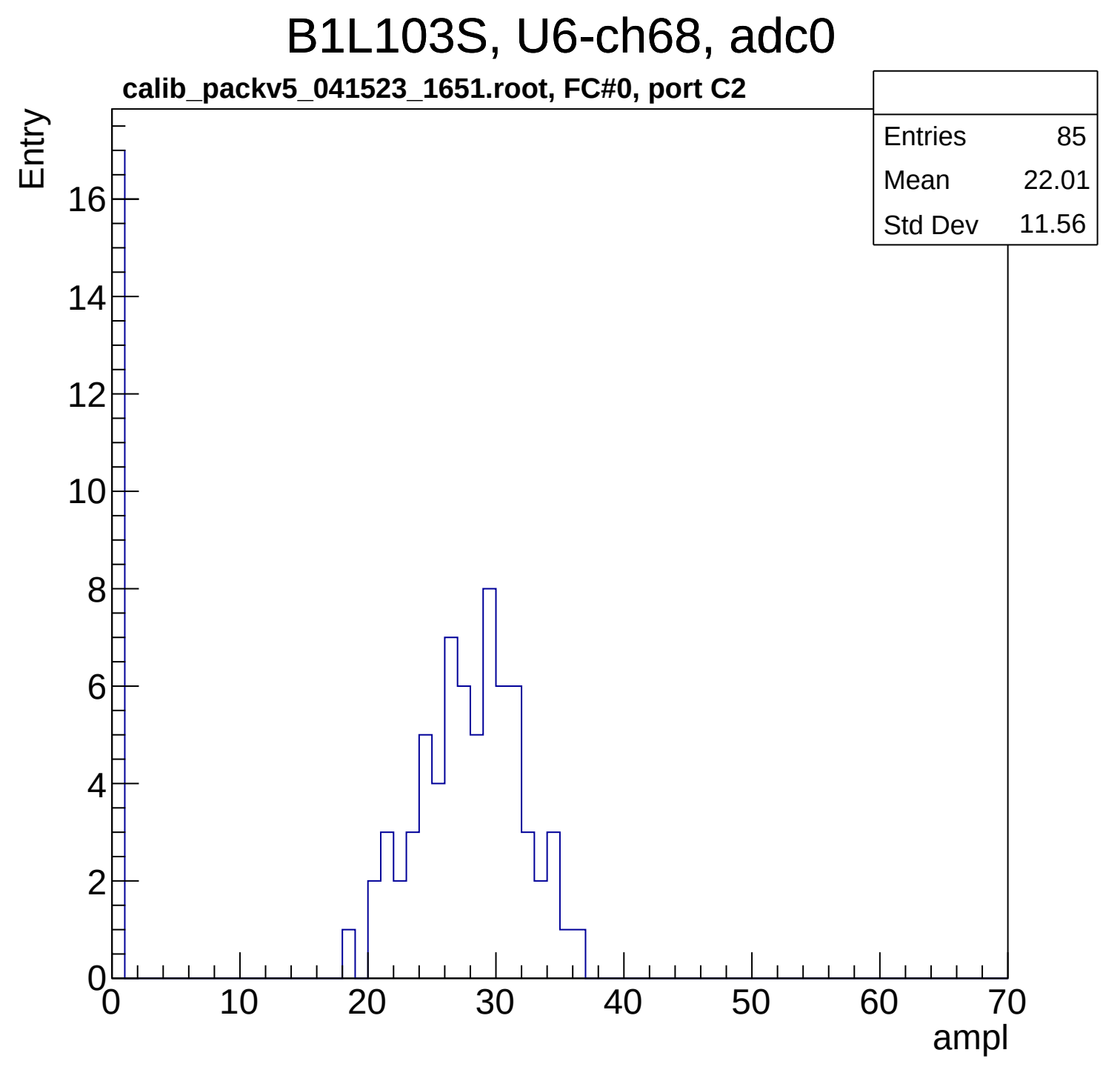
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch68, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 22.01
Std Dev 11.56
Entry
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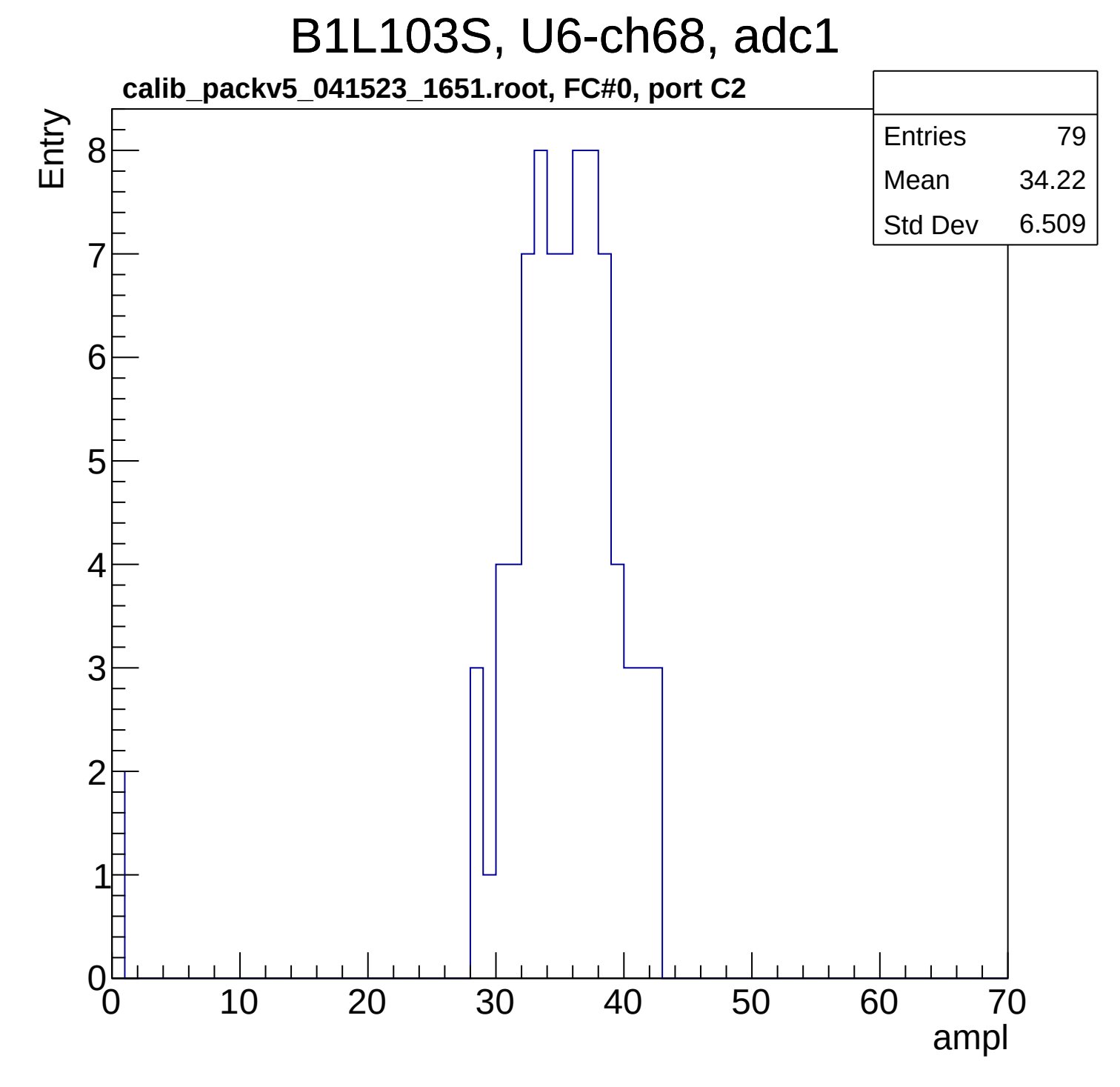
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch68, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 34.22
Std Dev 6.509
Entry
ampl
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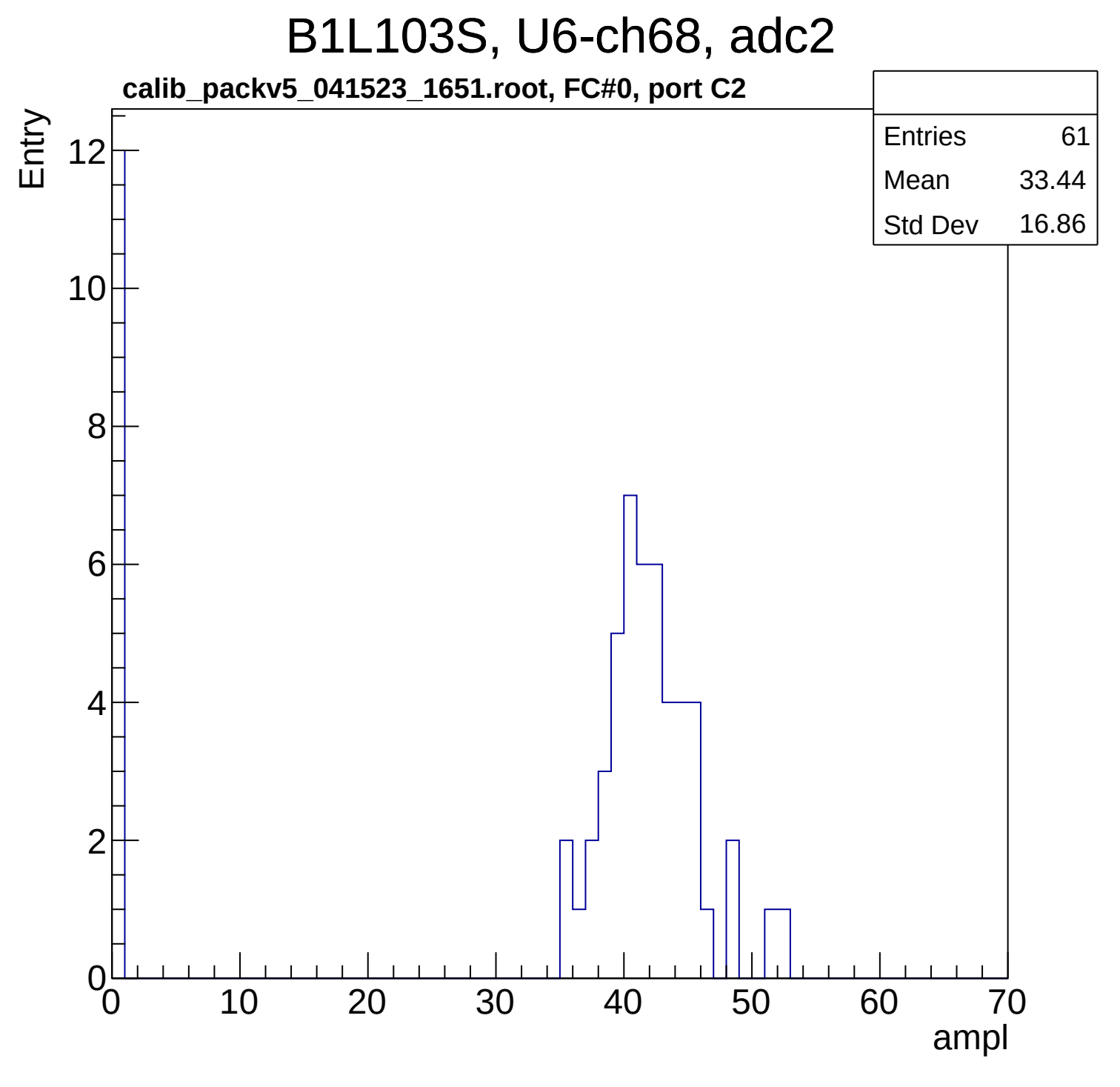
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch68, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 33.44
Std Dev 16.86
Entry
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2
4
6
8
10
12
0
10
20
30
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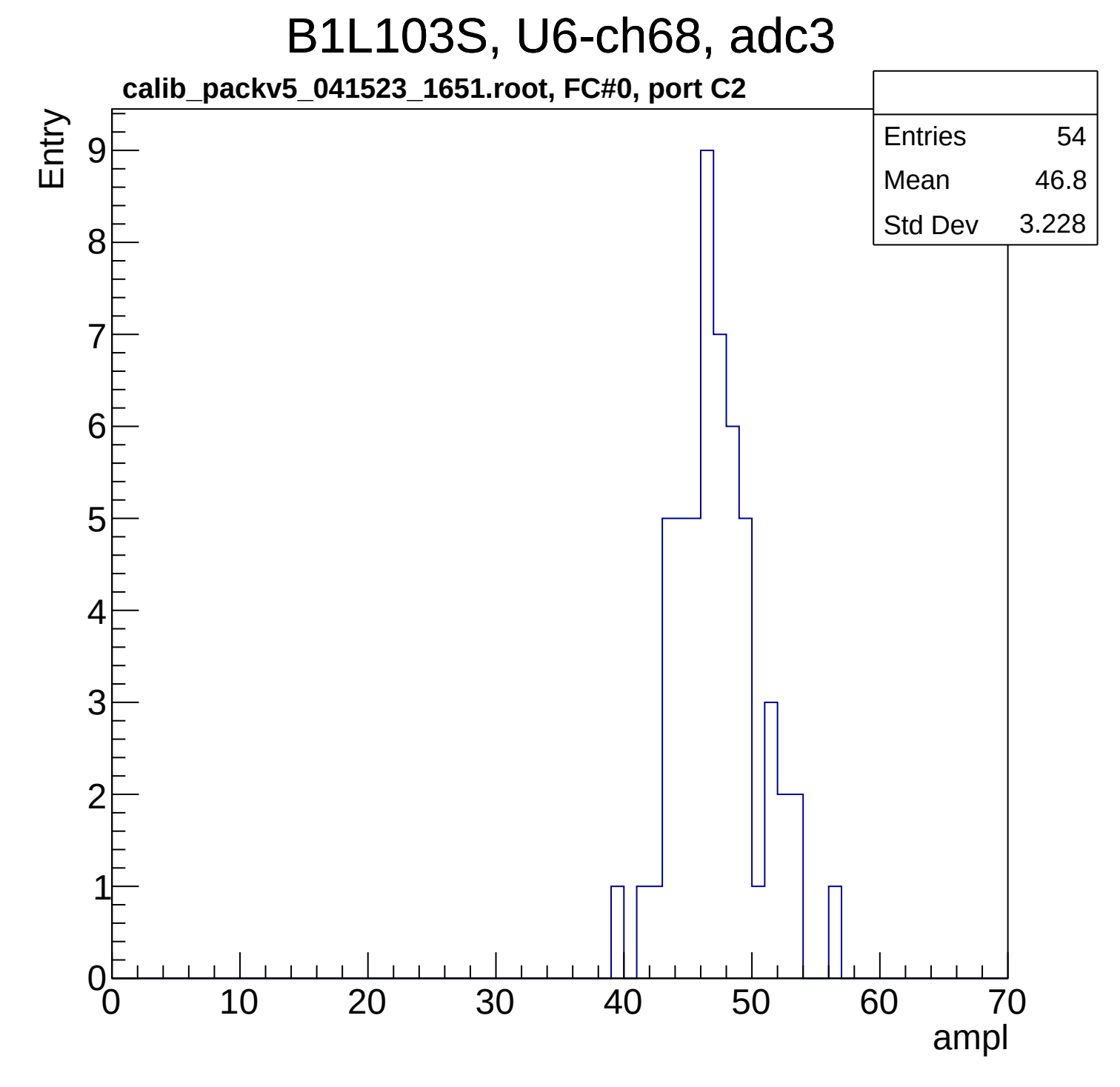
50
60
70
ampl


B1L103S, U6-ch68, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 46.8
Std Dev 3.228
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
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60
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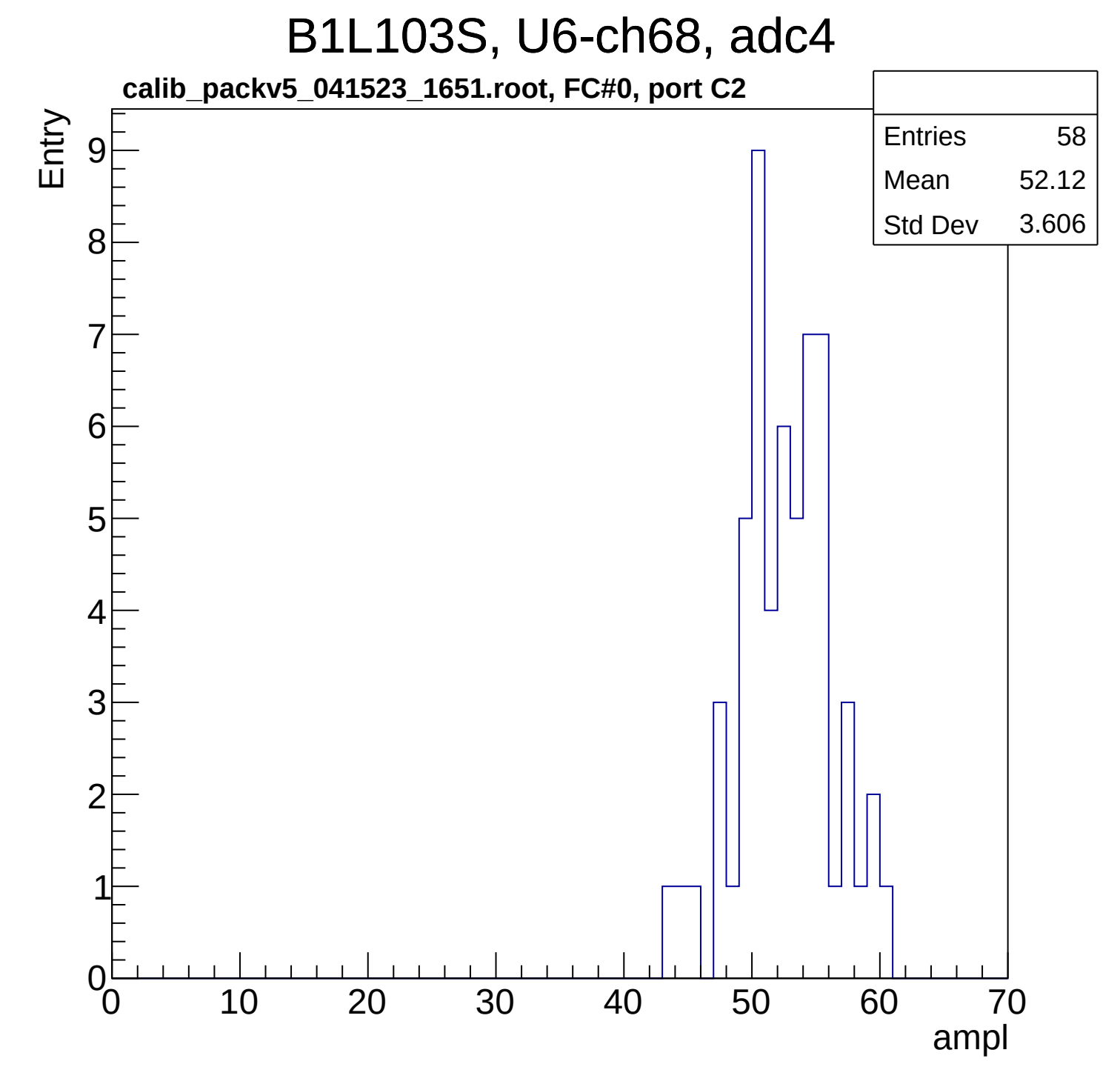
B1L103S, U6-ch68, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 52.12
Std Dev 3.606
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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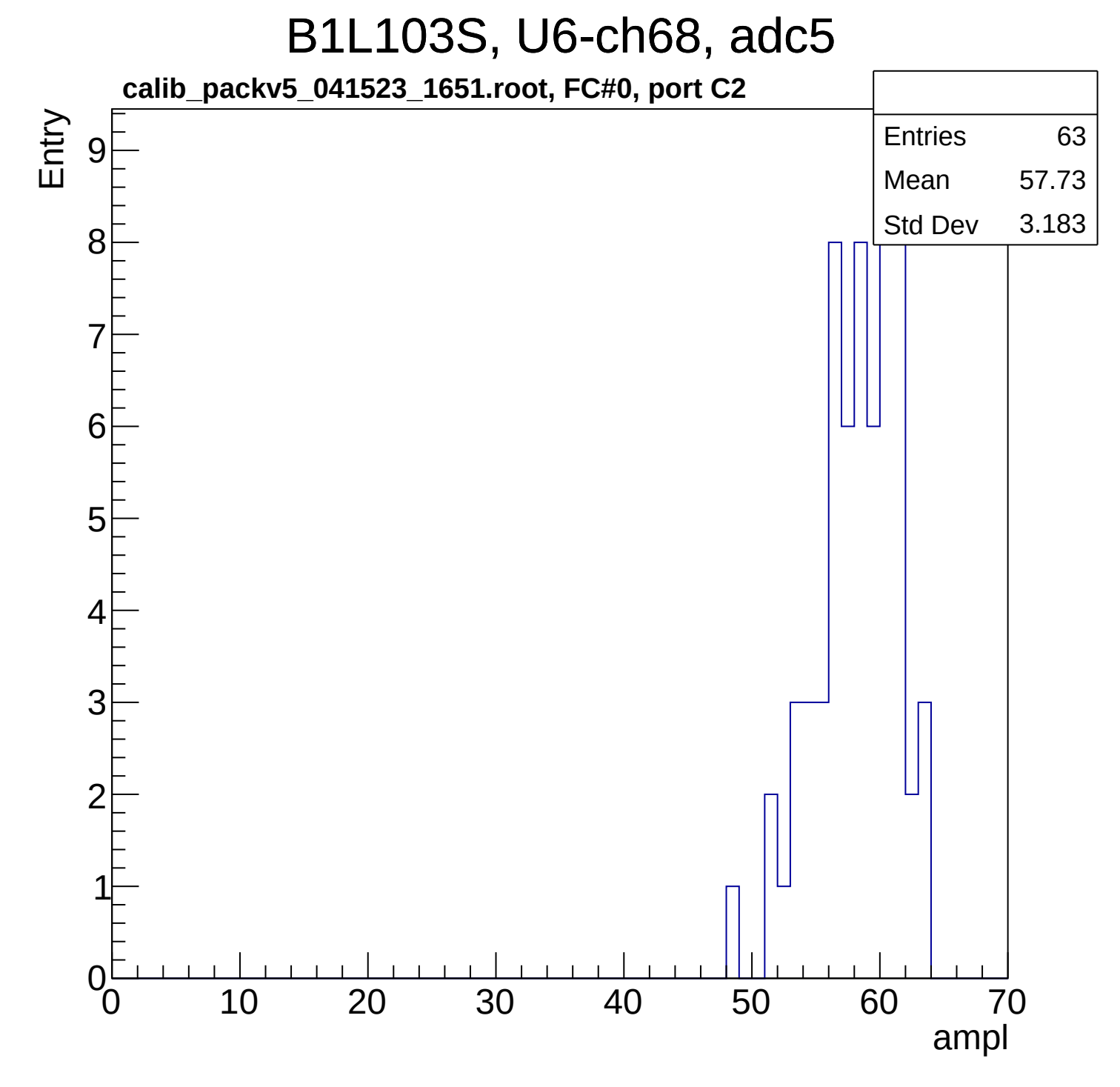
B1L103S, U6-ch68, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 57.73
Std Dev 3.183
Entry
ampl
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2
3
4
5
6
7
8
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0
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40
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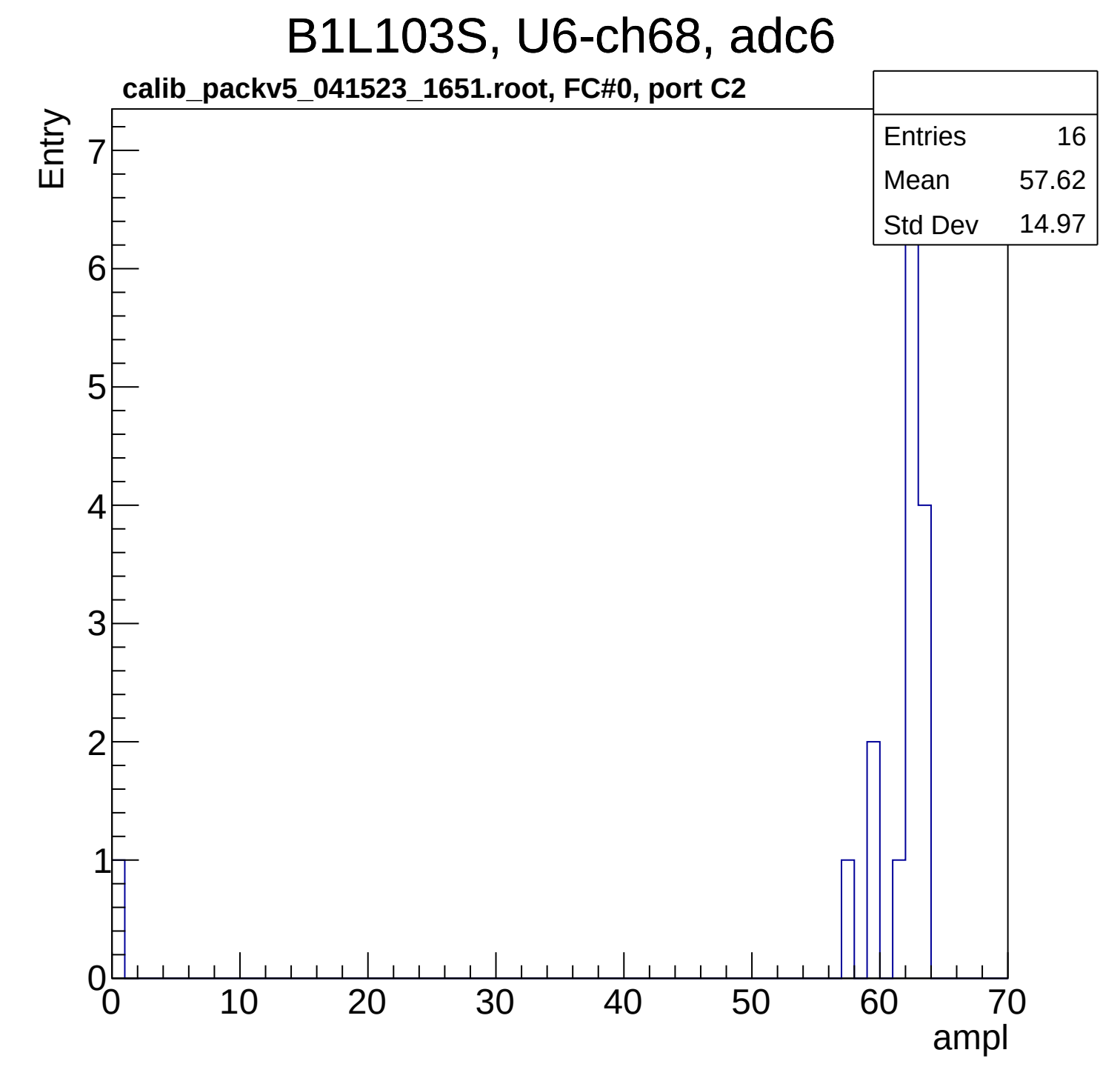
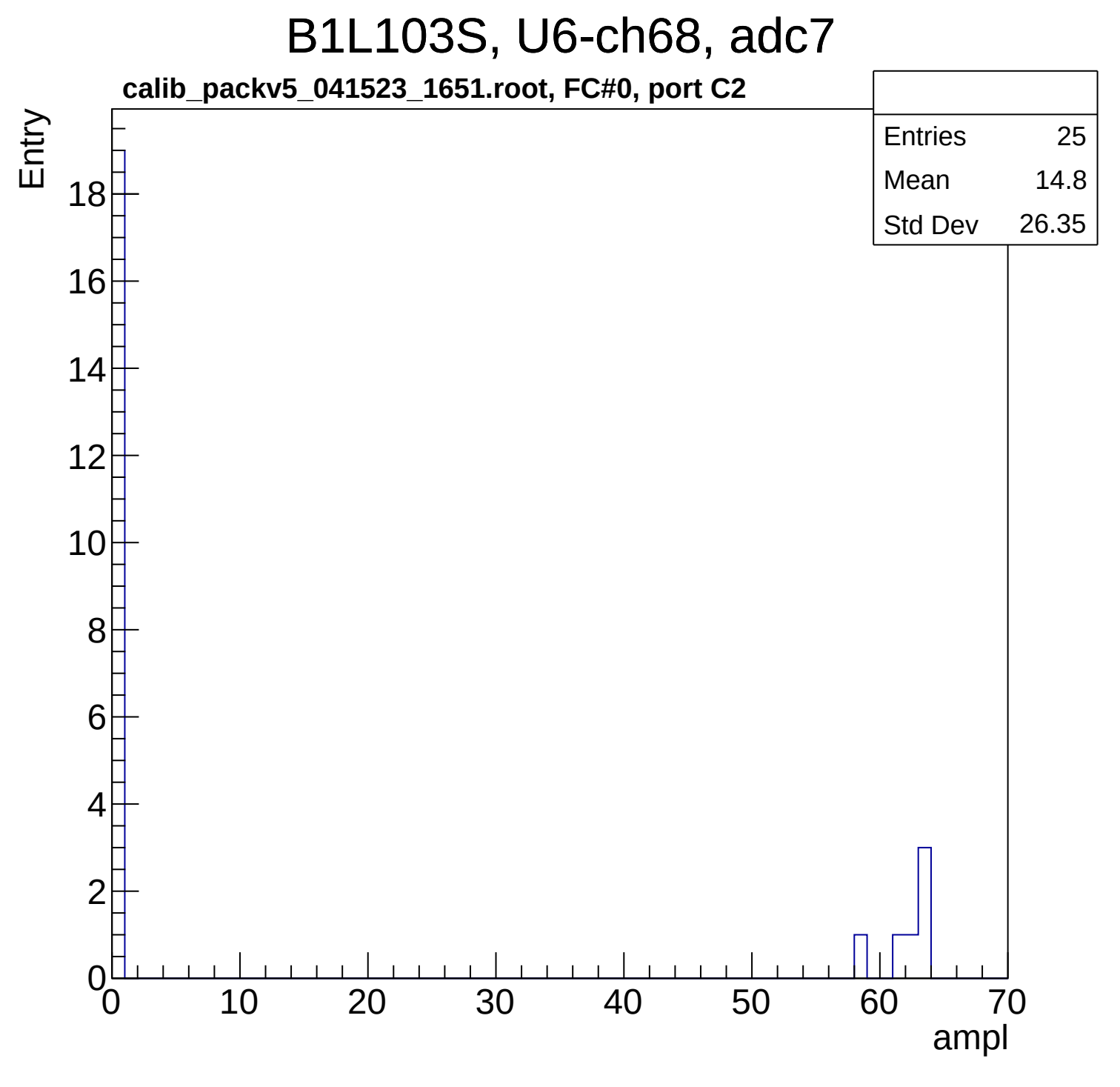
60
70


B1L103S, U6-ch68, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 57.62
Std Dev 14.97
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U6-ch68, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 14.8
Std Dev 26.35
Entry
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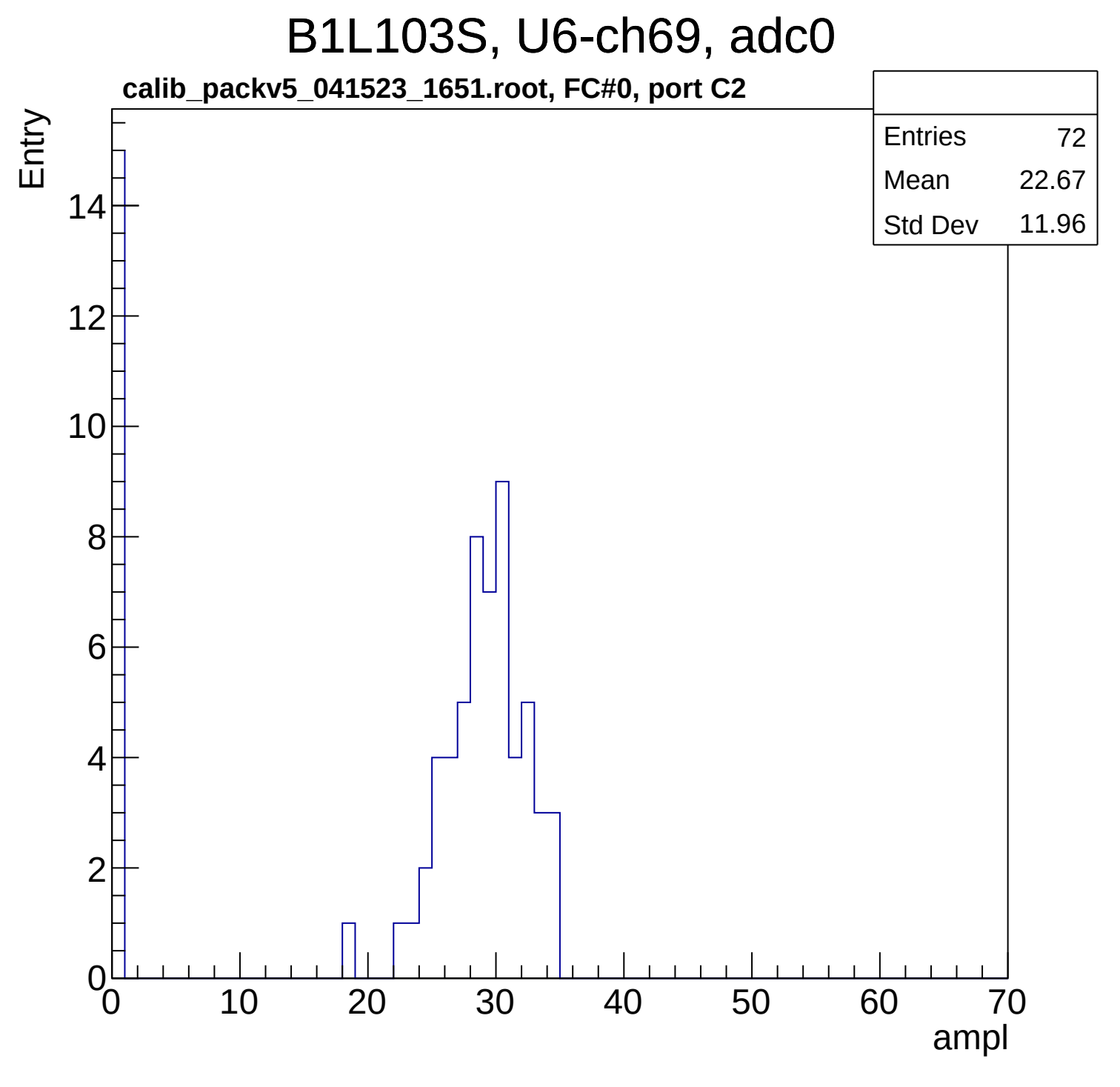
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch69, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 22.67
Std Dev 11.96
Entry
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2
4
6
8
10
12
14
0
10
20
30
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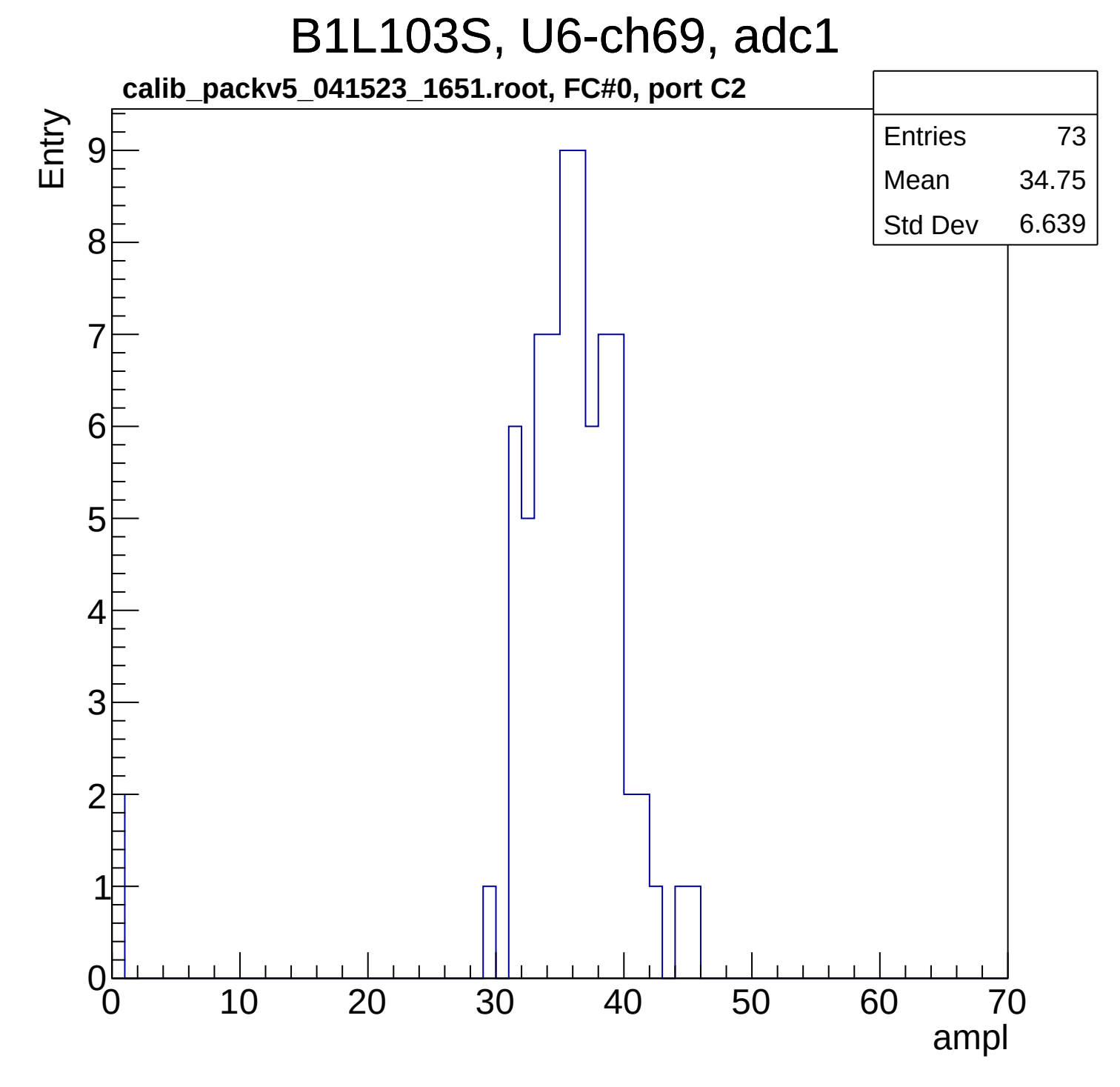
50
60
70
ampl


B1L103S, U6-ch69, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 34.75
Std Dev 6.639
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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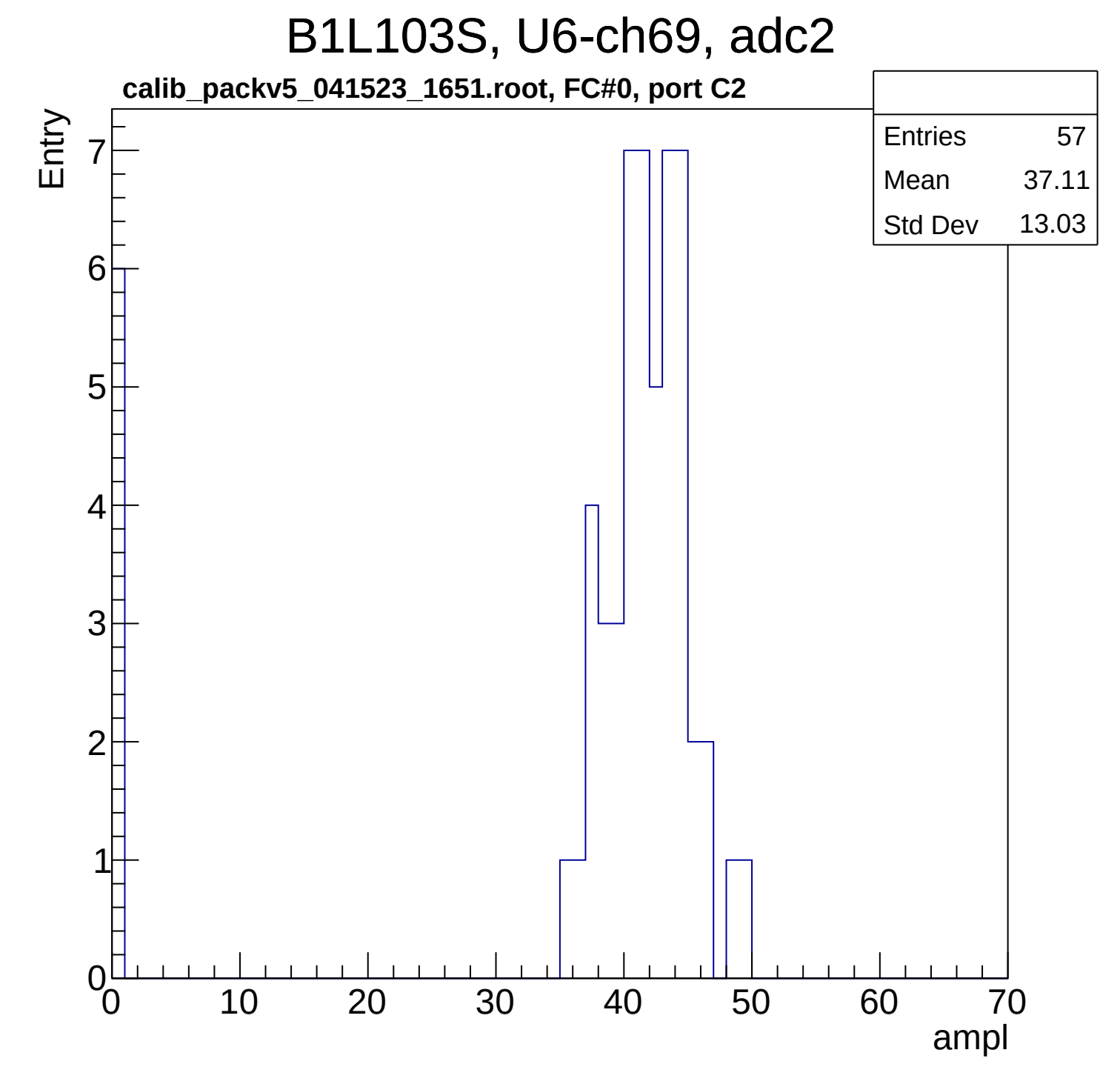
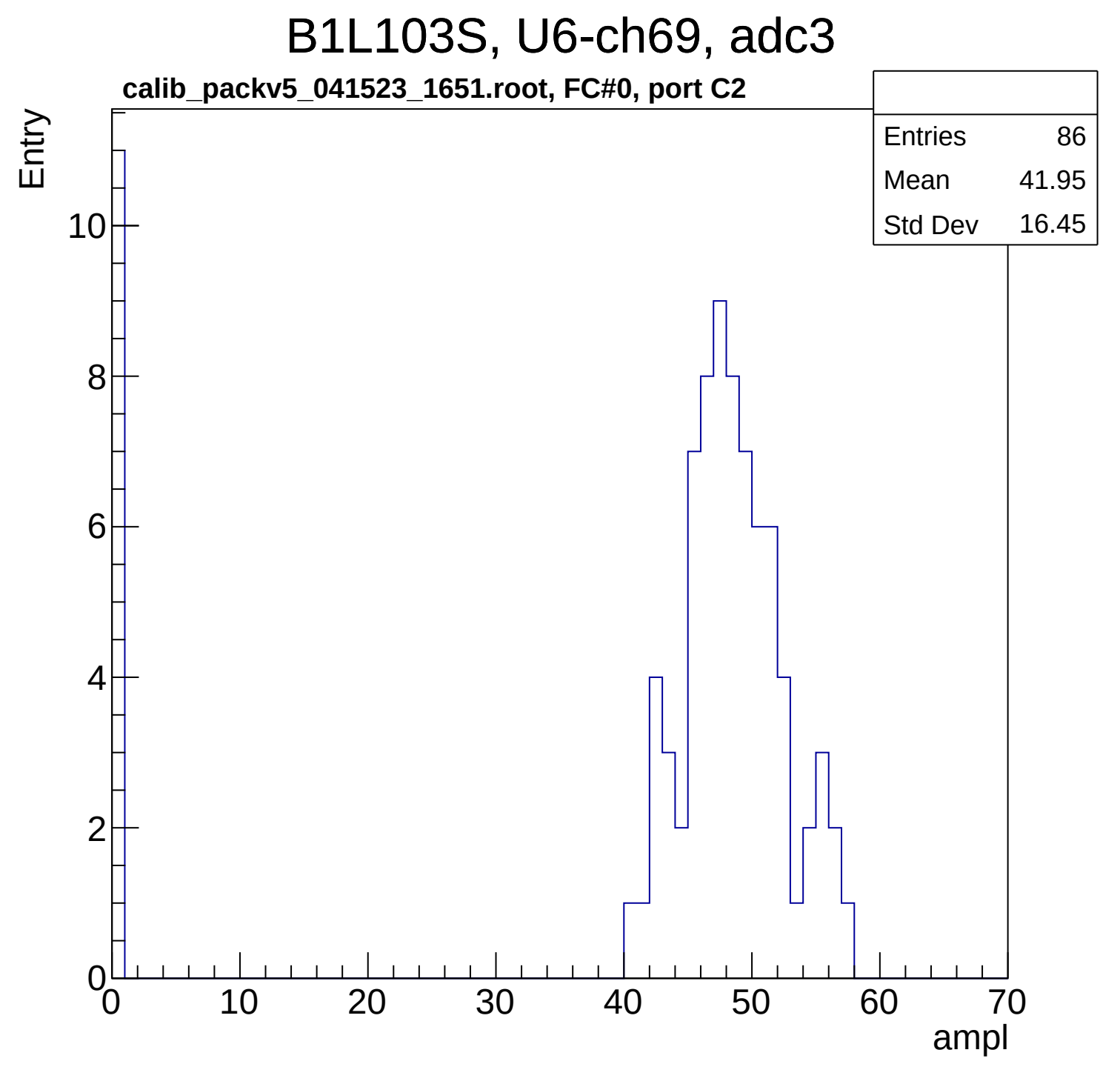
40
50
60
70


B1L103S, U6-ch69, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 37.11
Std Dev 13.03
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U6-ch69, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 41.95
Std Dev 16.45
Entry
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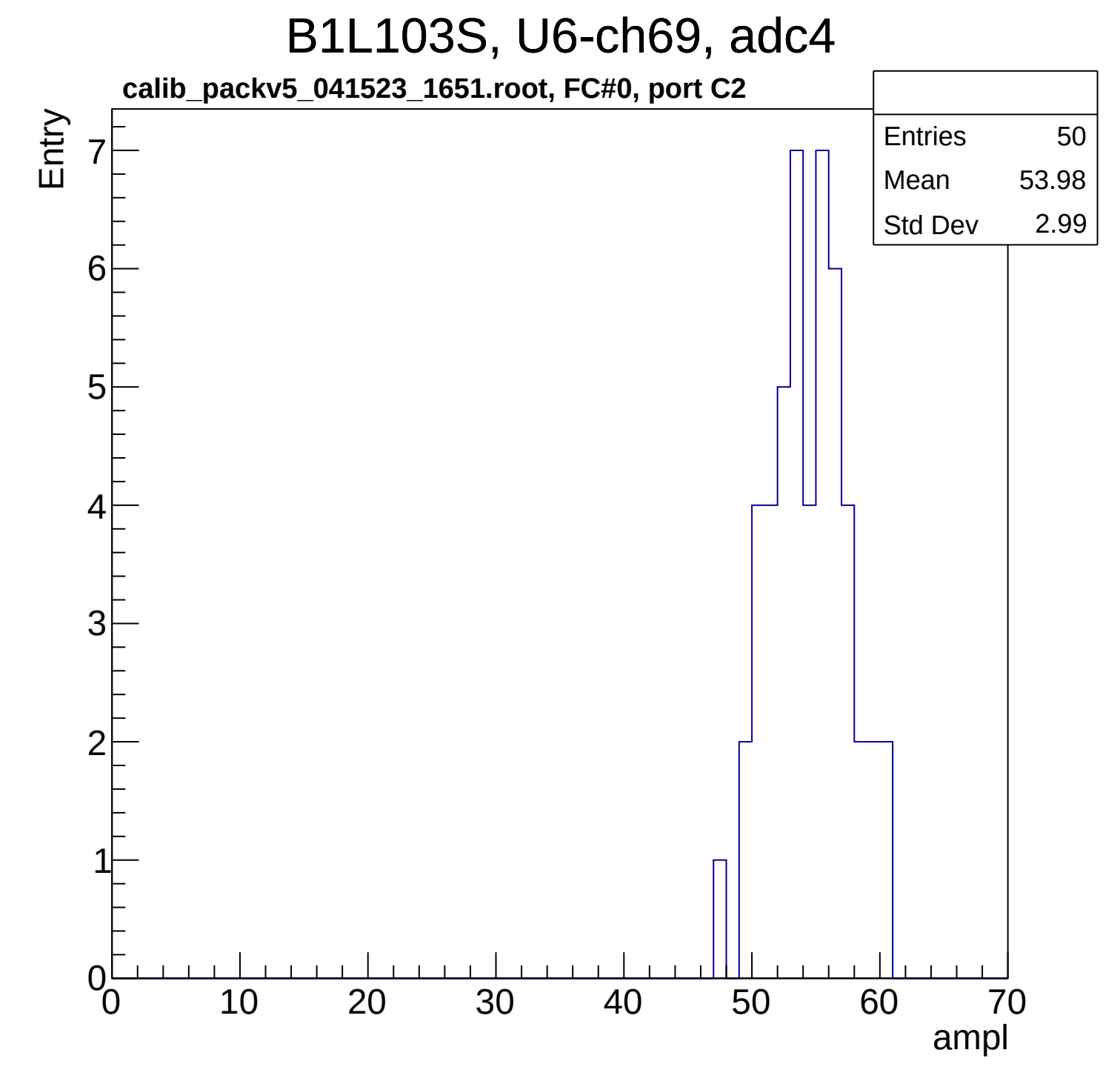
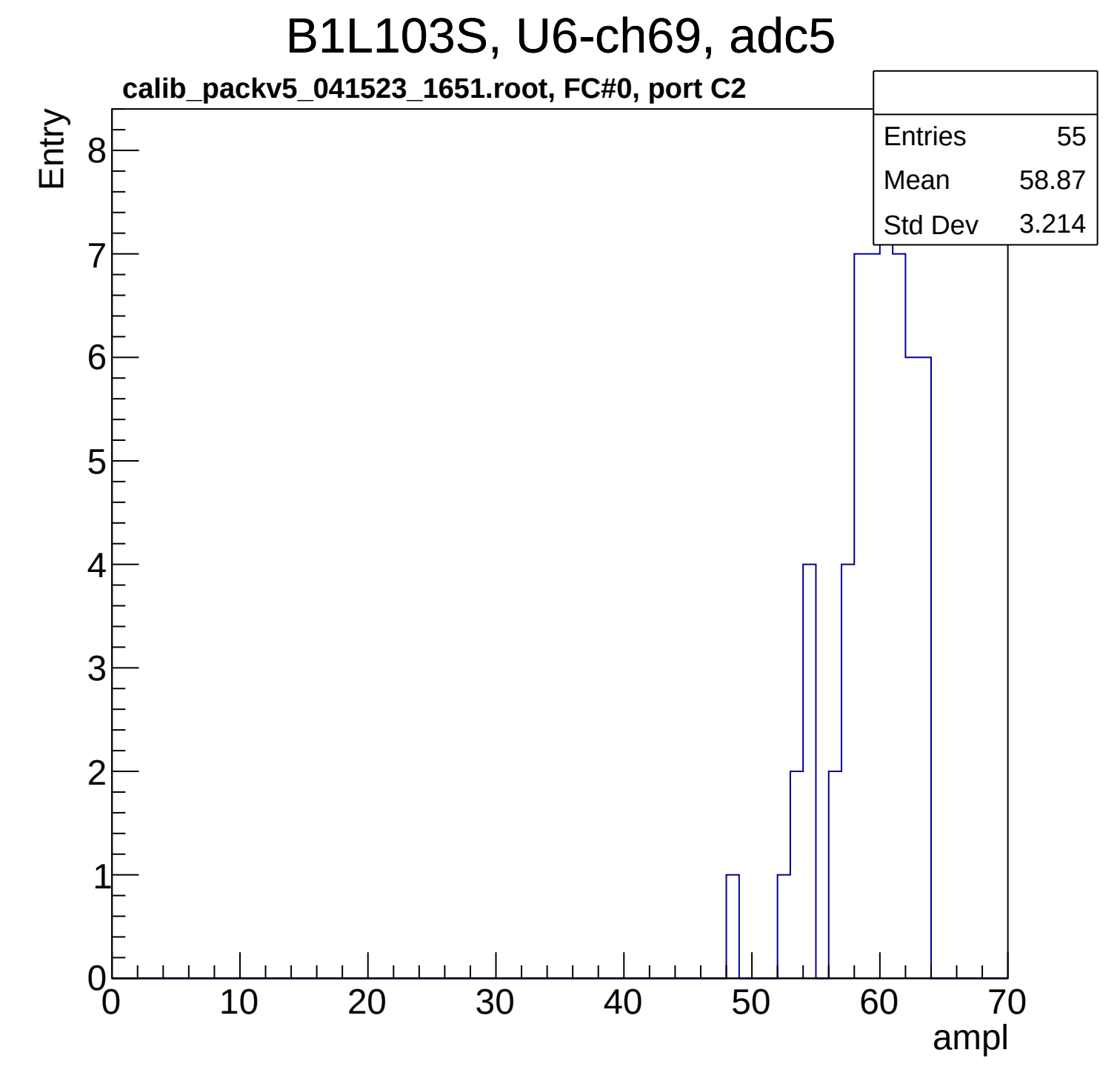
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch69, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 53.98
Std Dev 2.99
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U6-ch69, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 58.87
Std Dev 3.214
Entry
ampl
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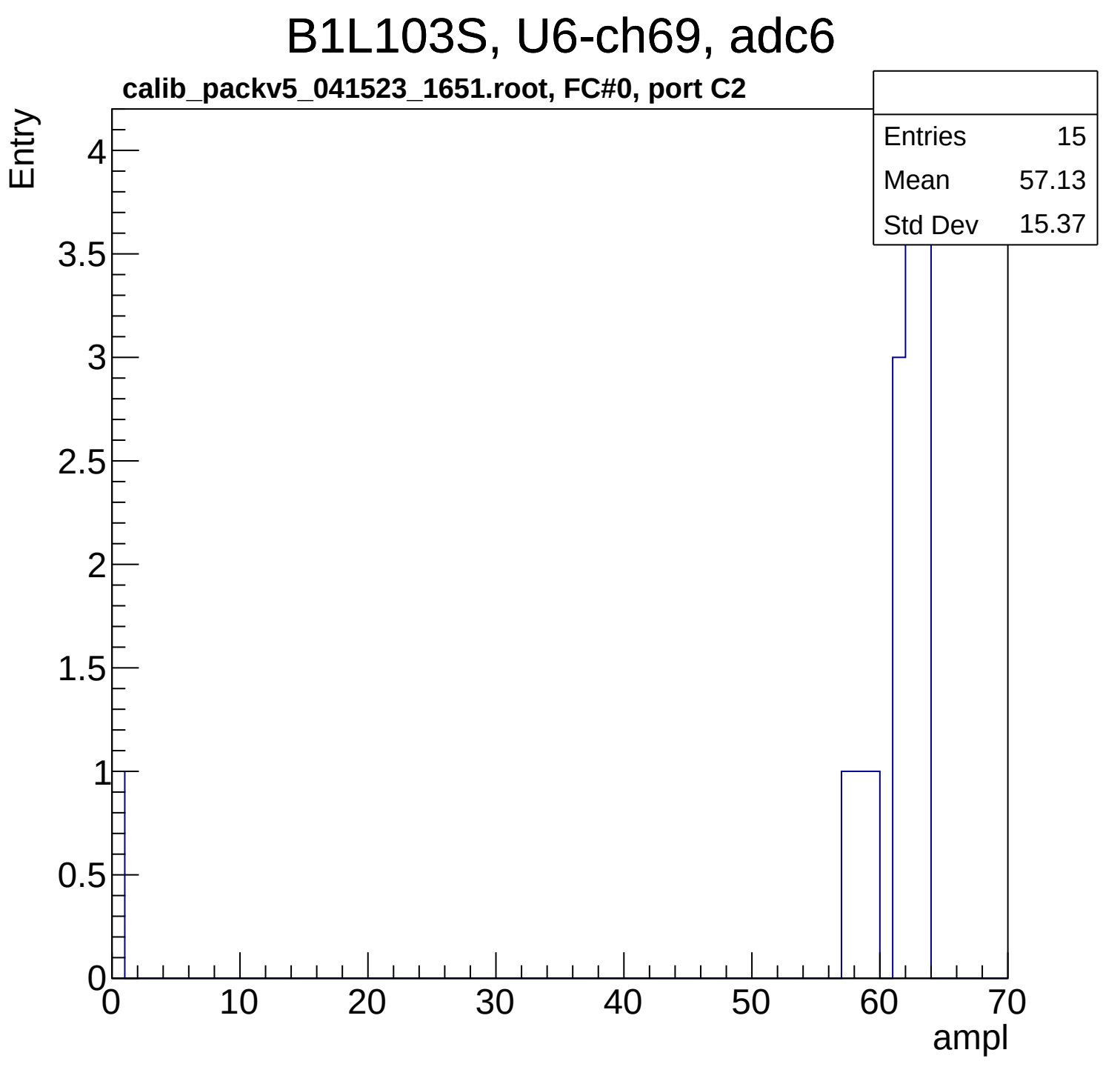
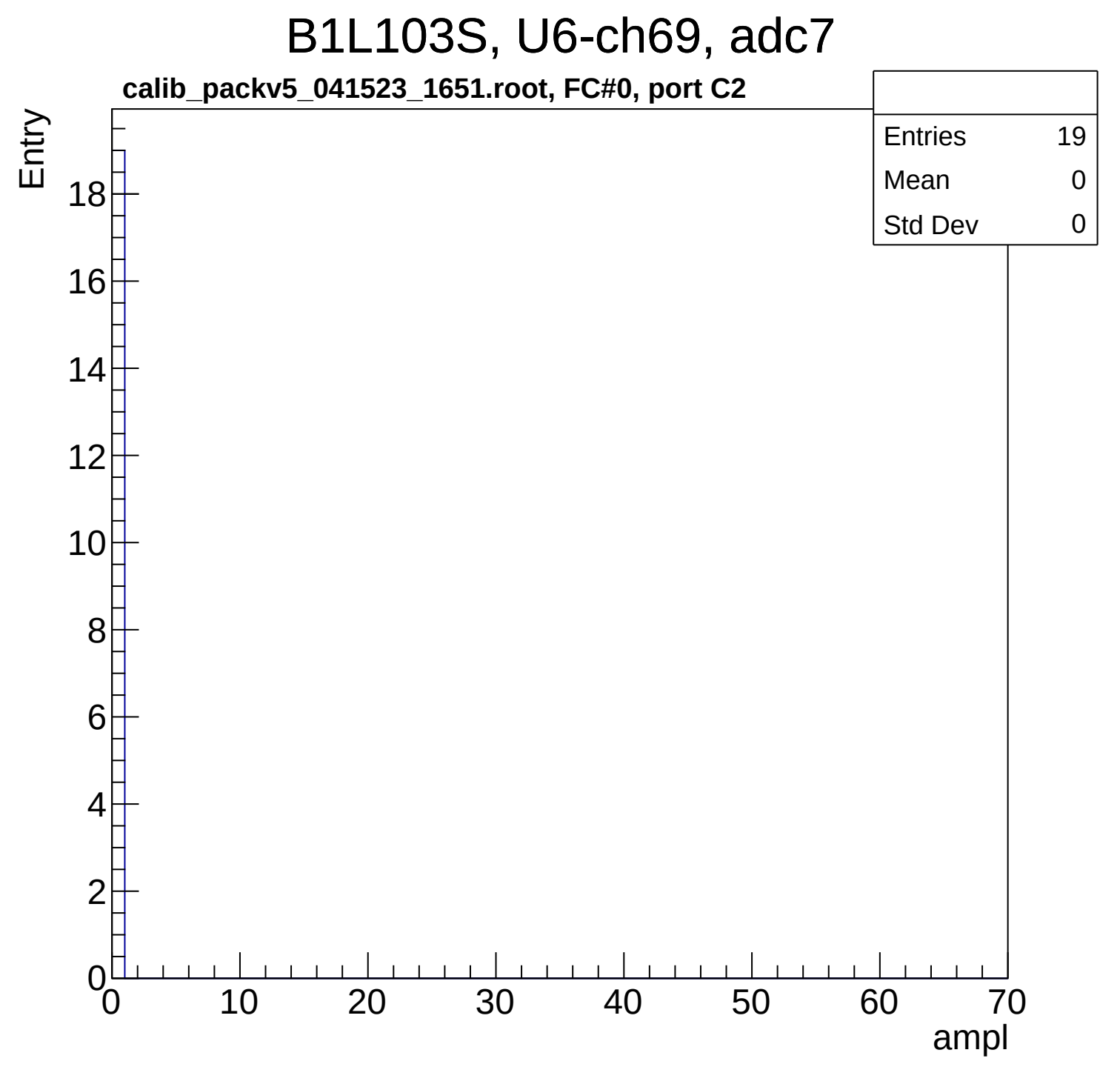
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch69, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 57.13
Std Dev 15.37
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U6-ch69, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
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6
8
10
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14
16
18
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10
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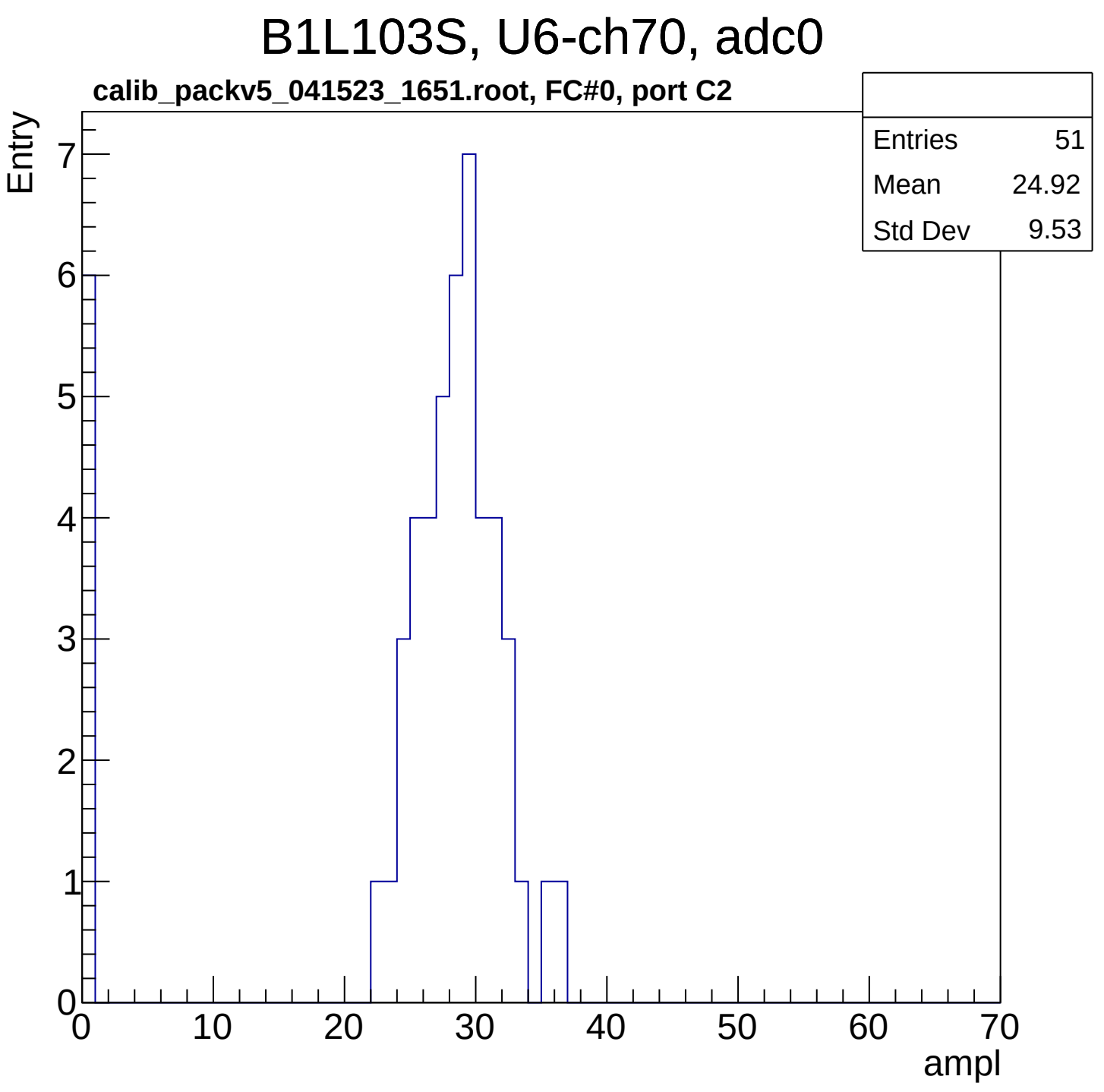
70
ampl


B1L103S, U6-ch70, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 24.92
Std Dev 9.53
Entry
0
1
2
3
4
5
6
7
0
10
20
30
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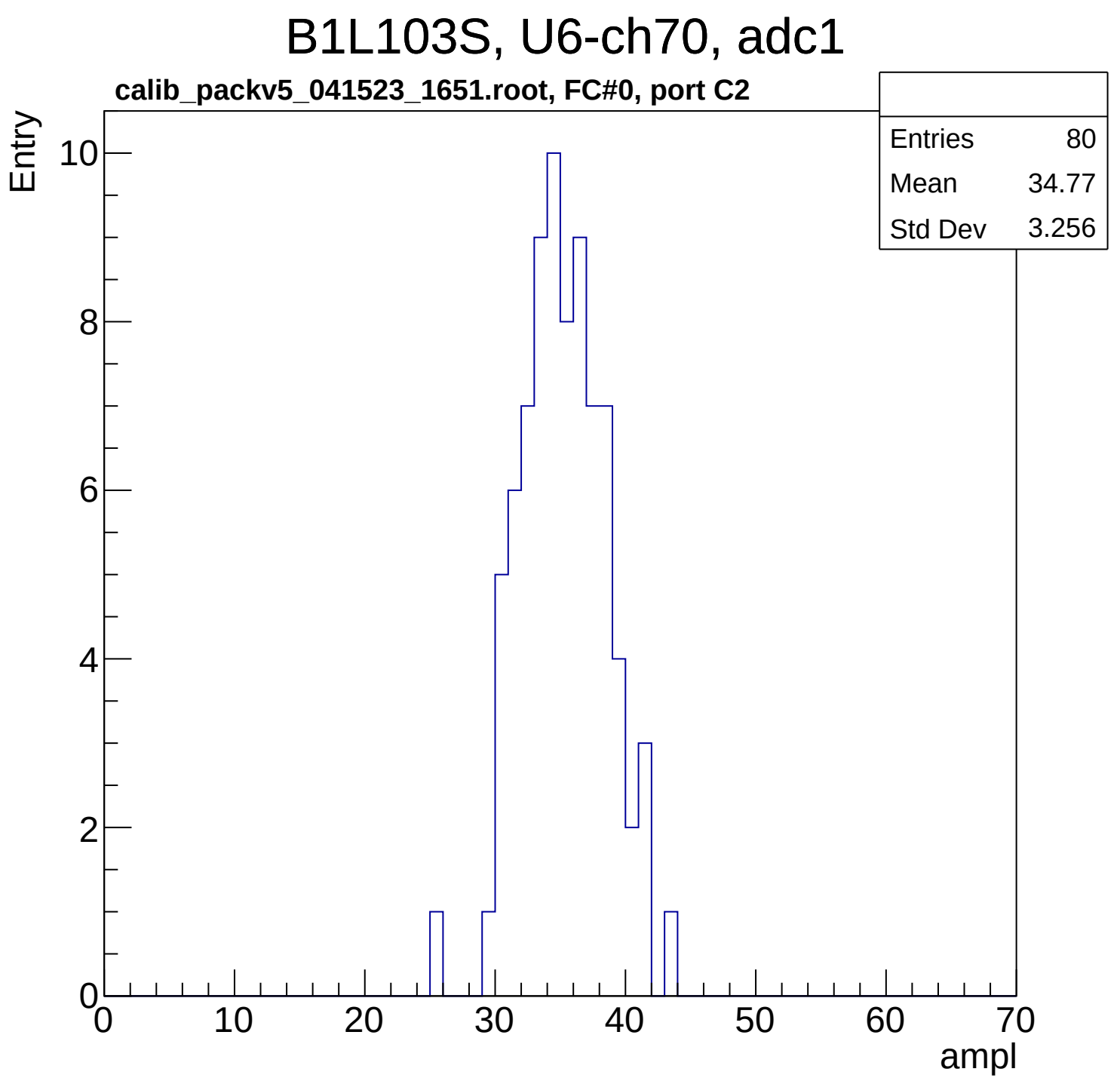
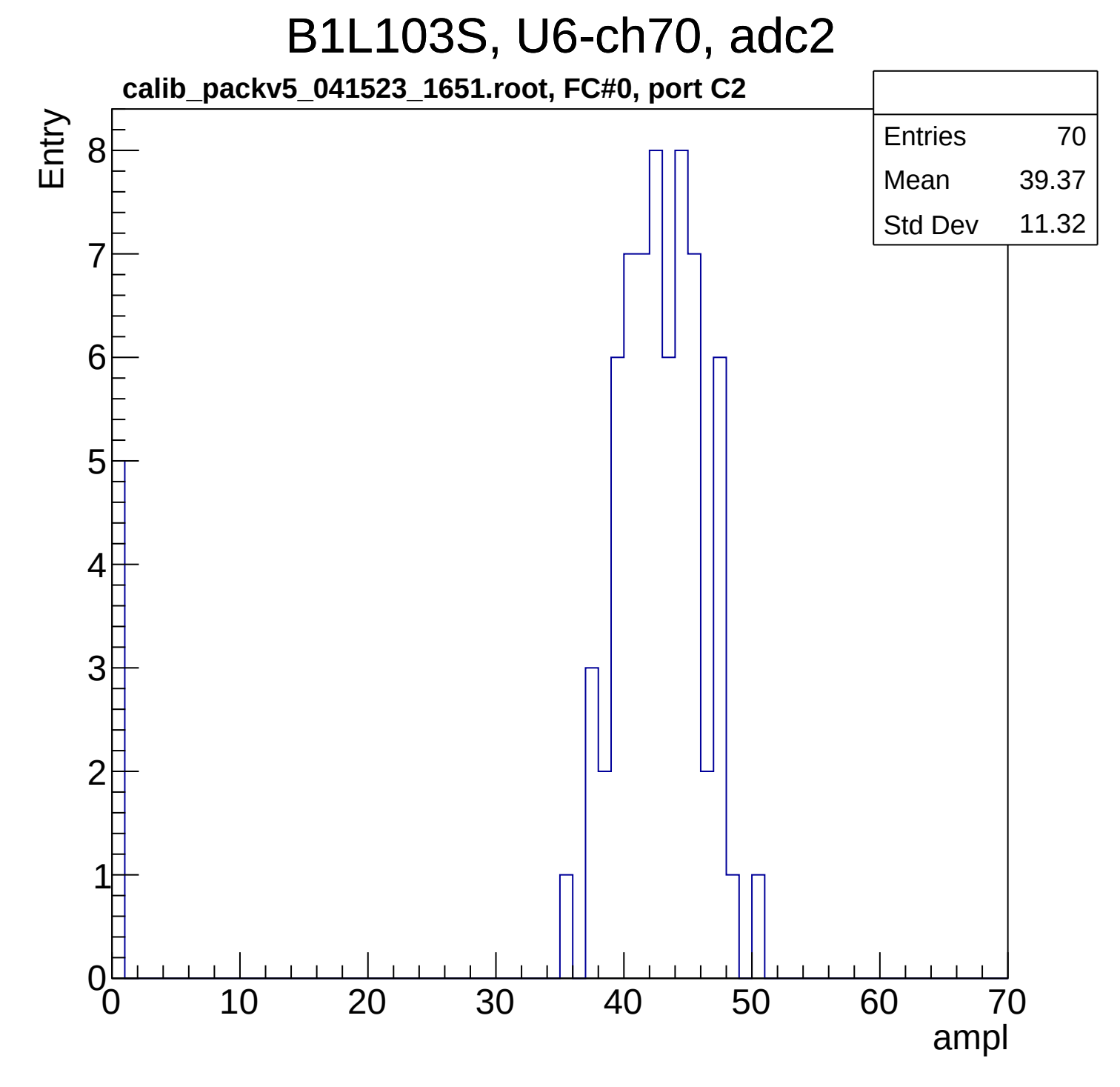
50
60
70
ampl


B1L103S, U6-ch70, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 34.77
Std Dev 3.256
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch70, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 39.37
Std Dev 11.32
Entry
ampl
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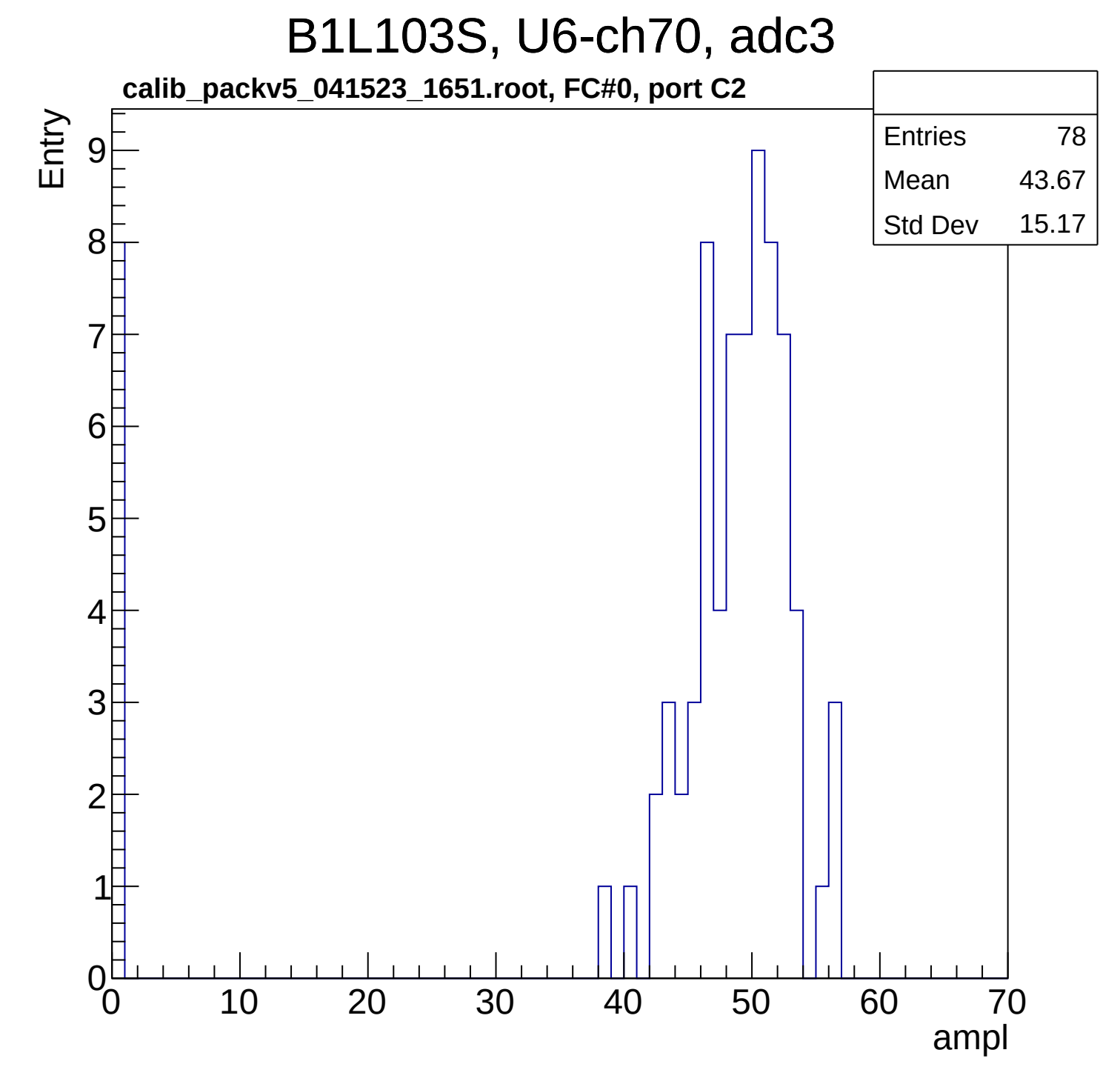
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch70, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 43.67
Std Dev 15.17
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
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60
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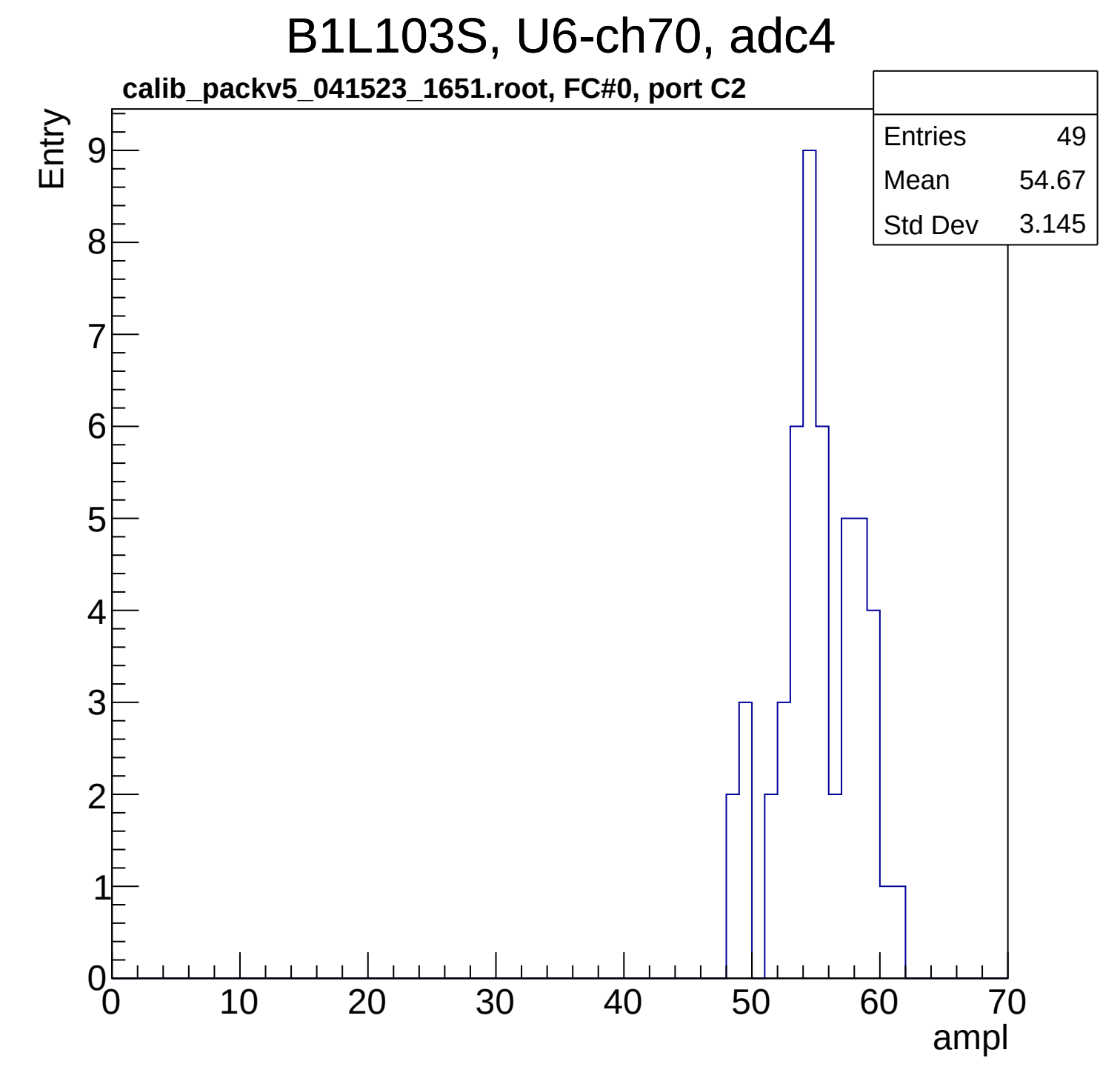
B1L103S, U6-ch70, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 54.67
Std Dev 3.145
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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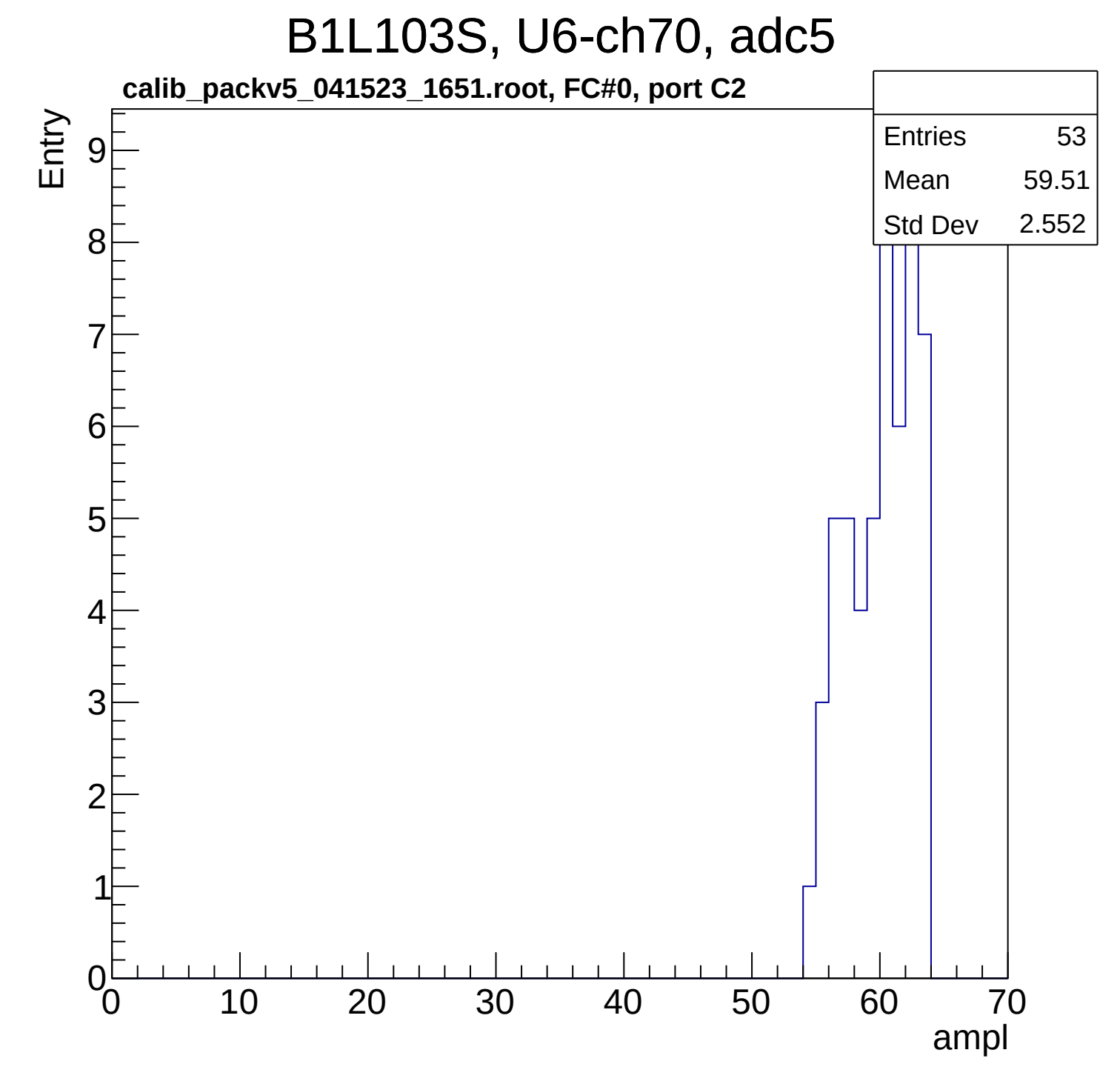
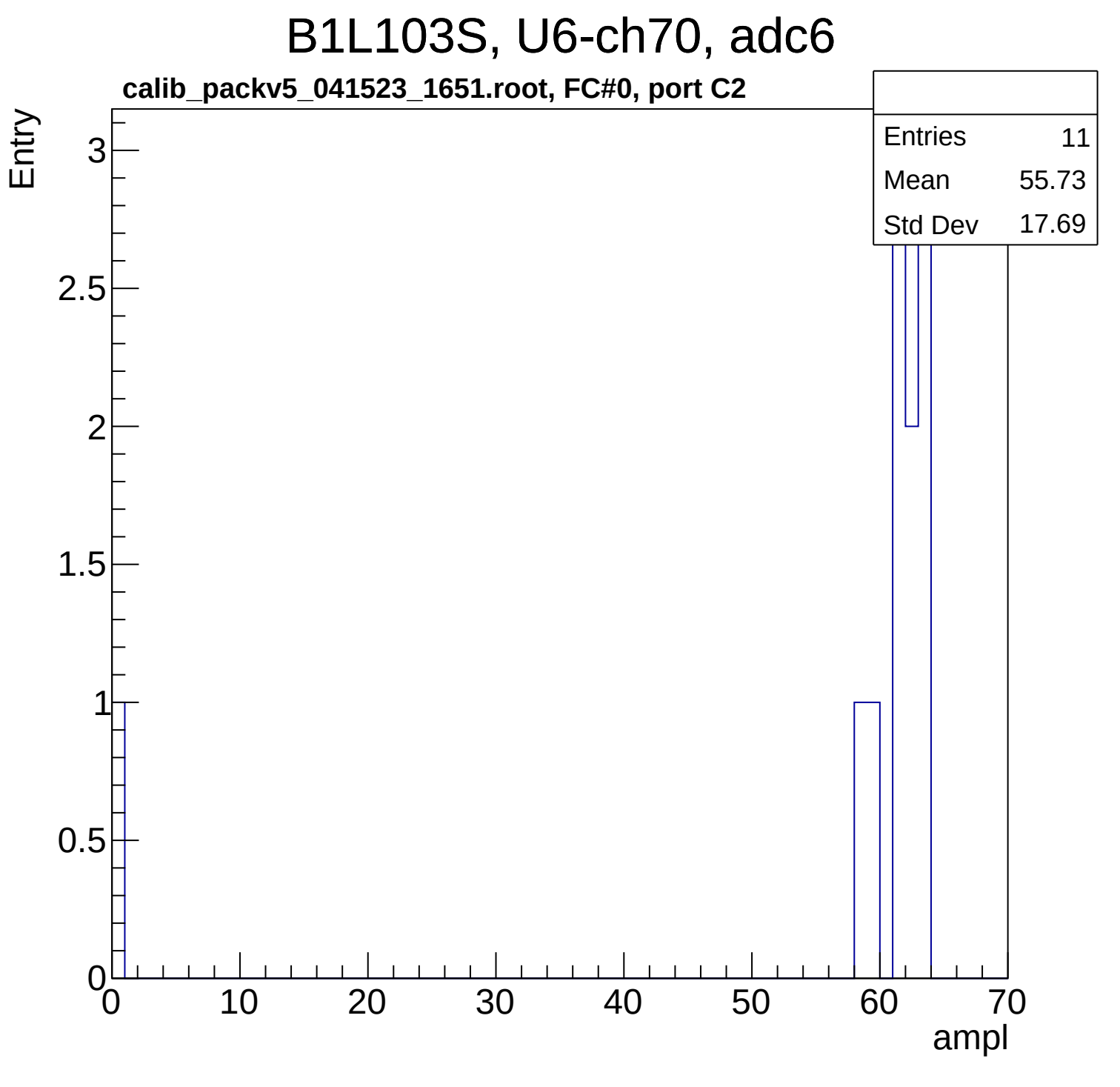
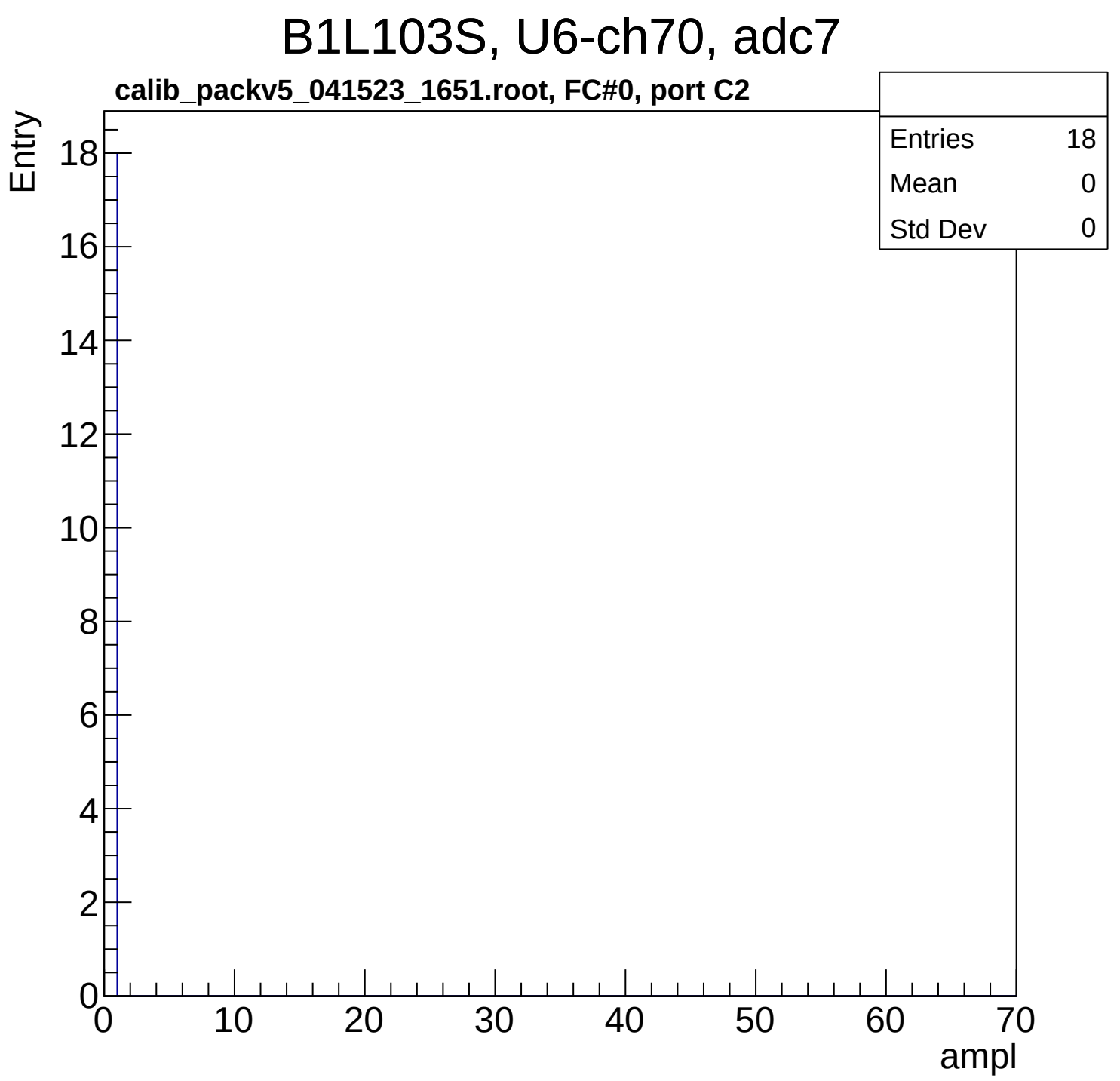
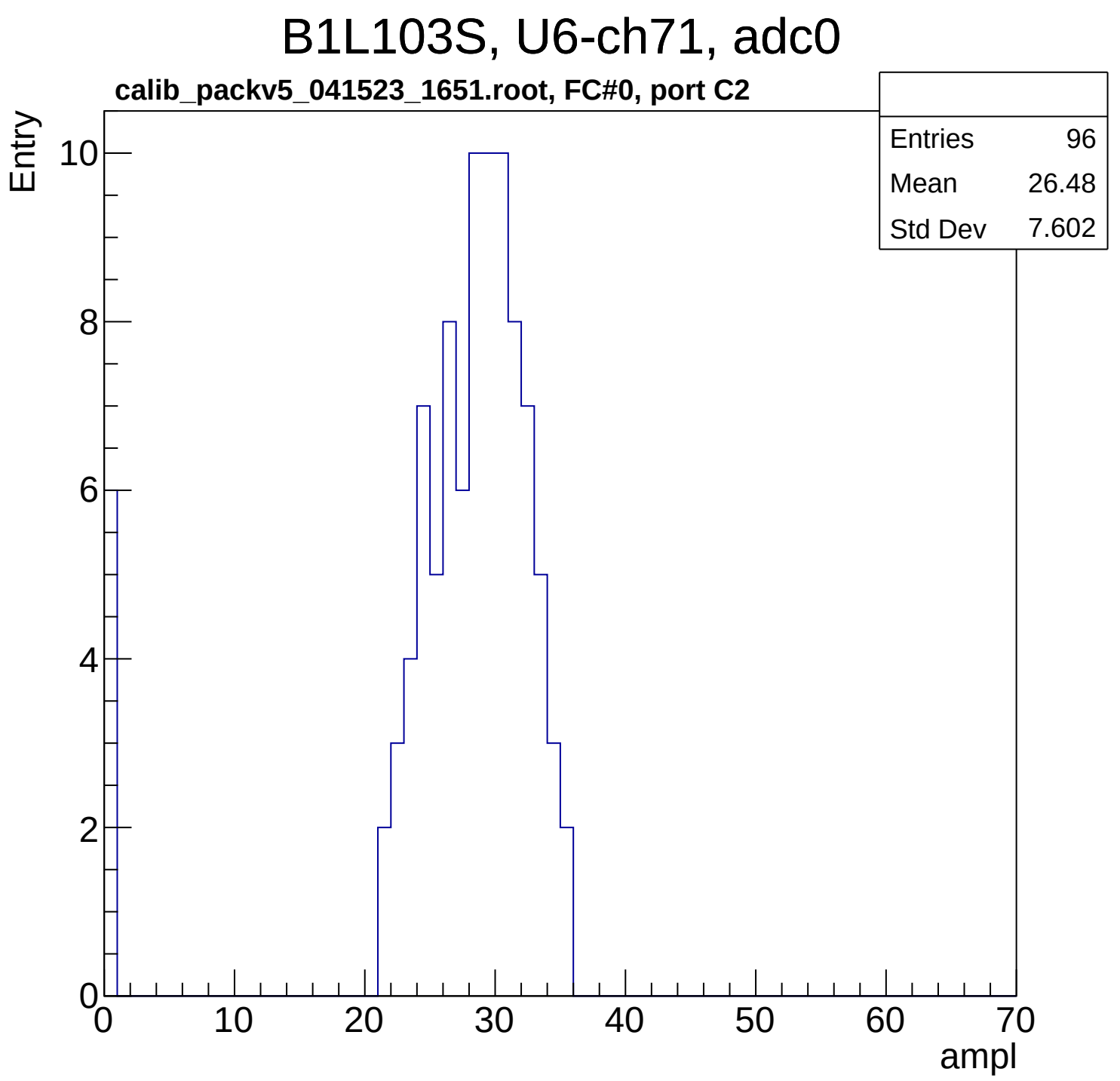
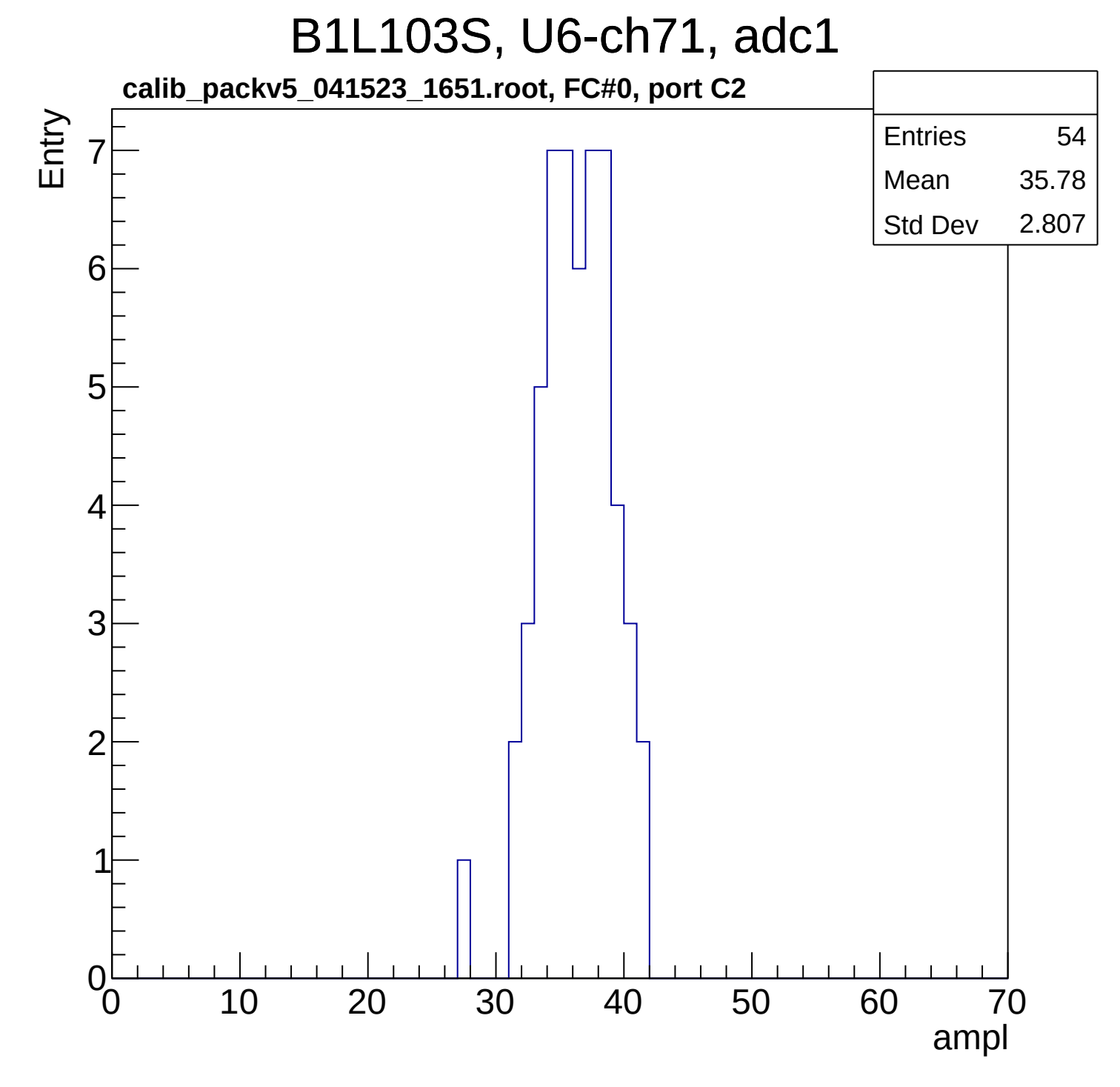
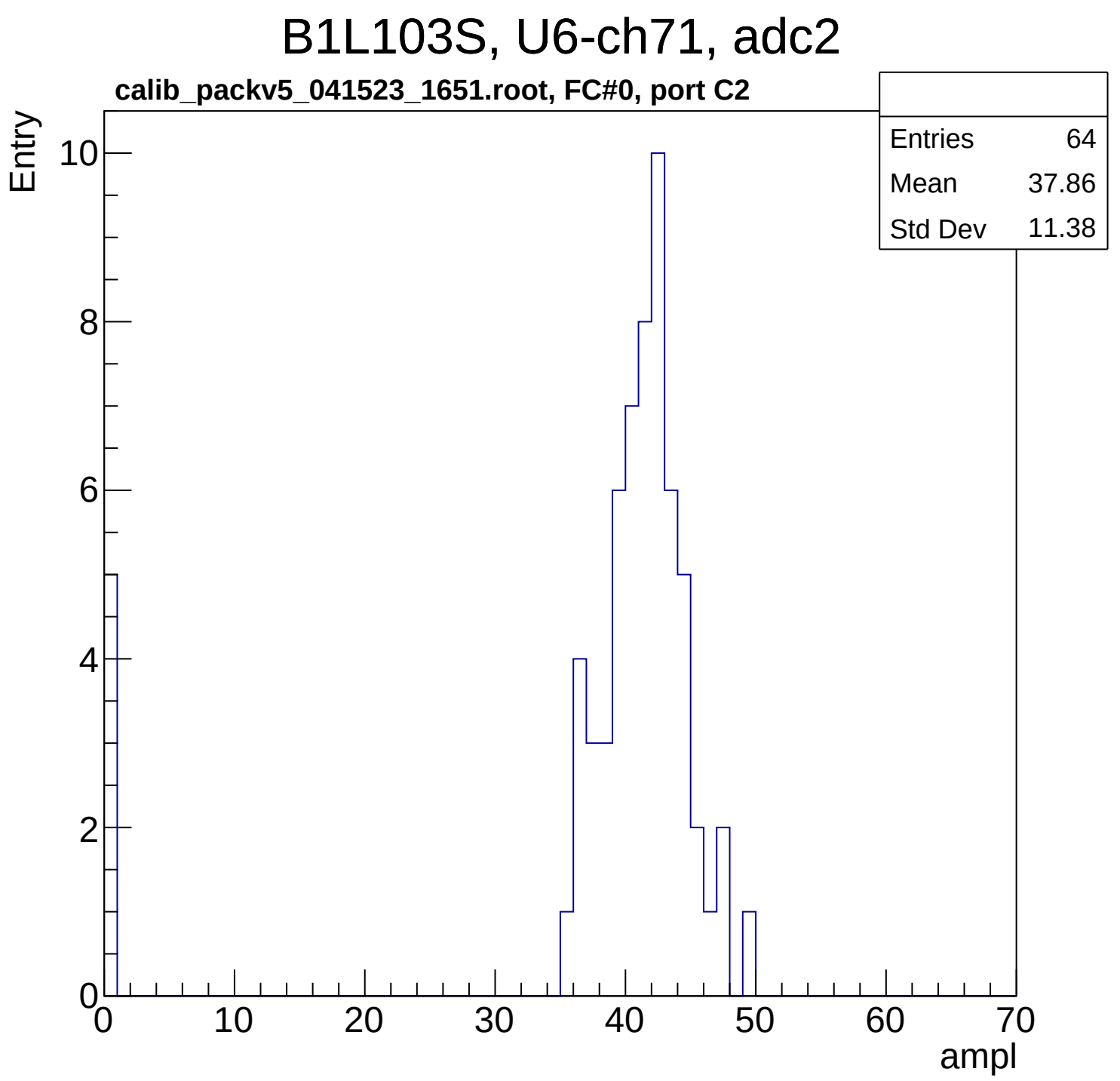

B1L103S, U6-ch70, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 59.51
Std Dev 2.552
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

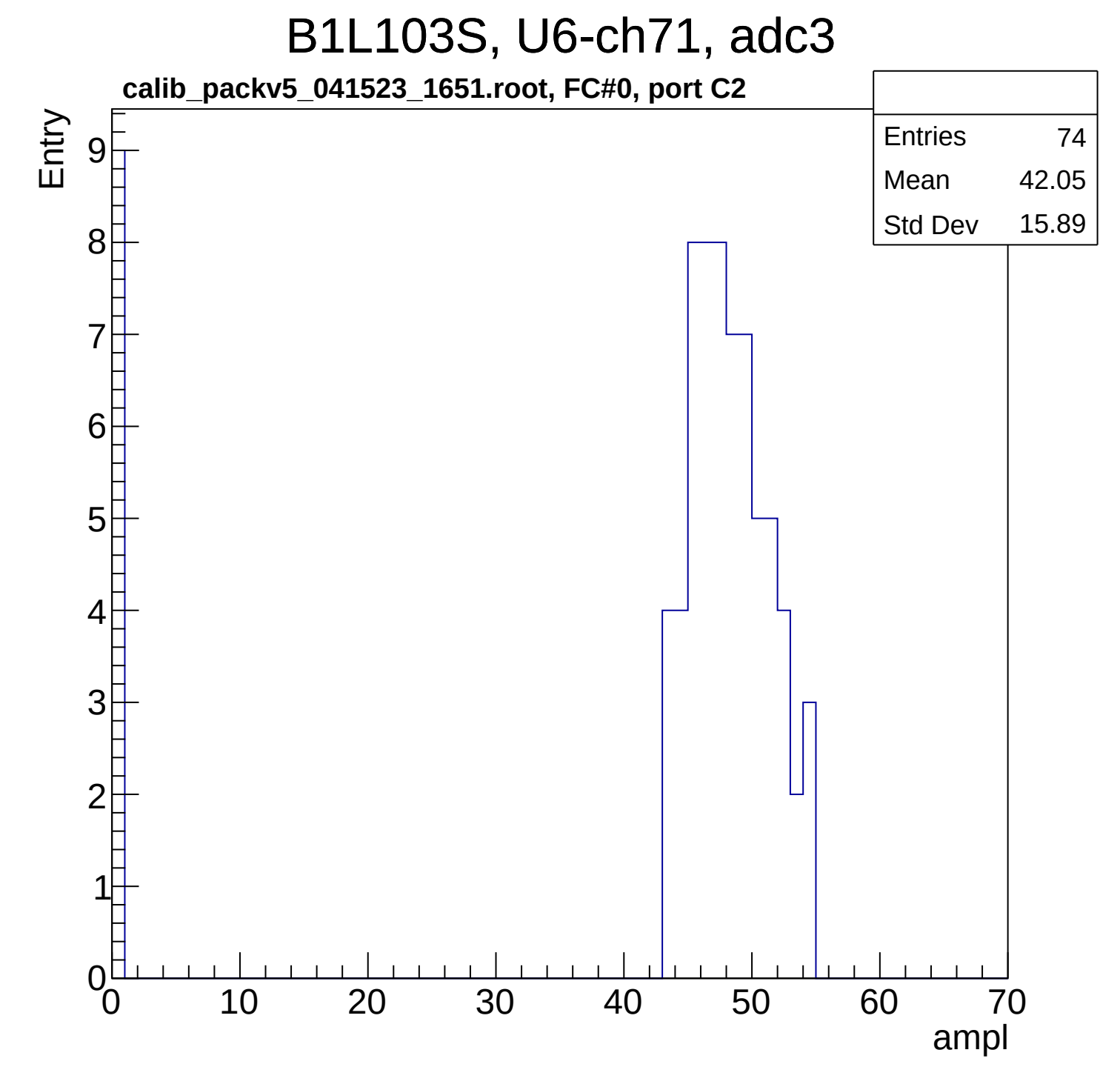

B1L103S, U6-ch70, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 55.73
Std Dev 17.69
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

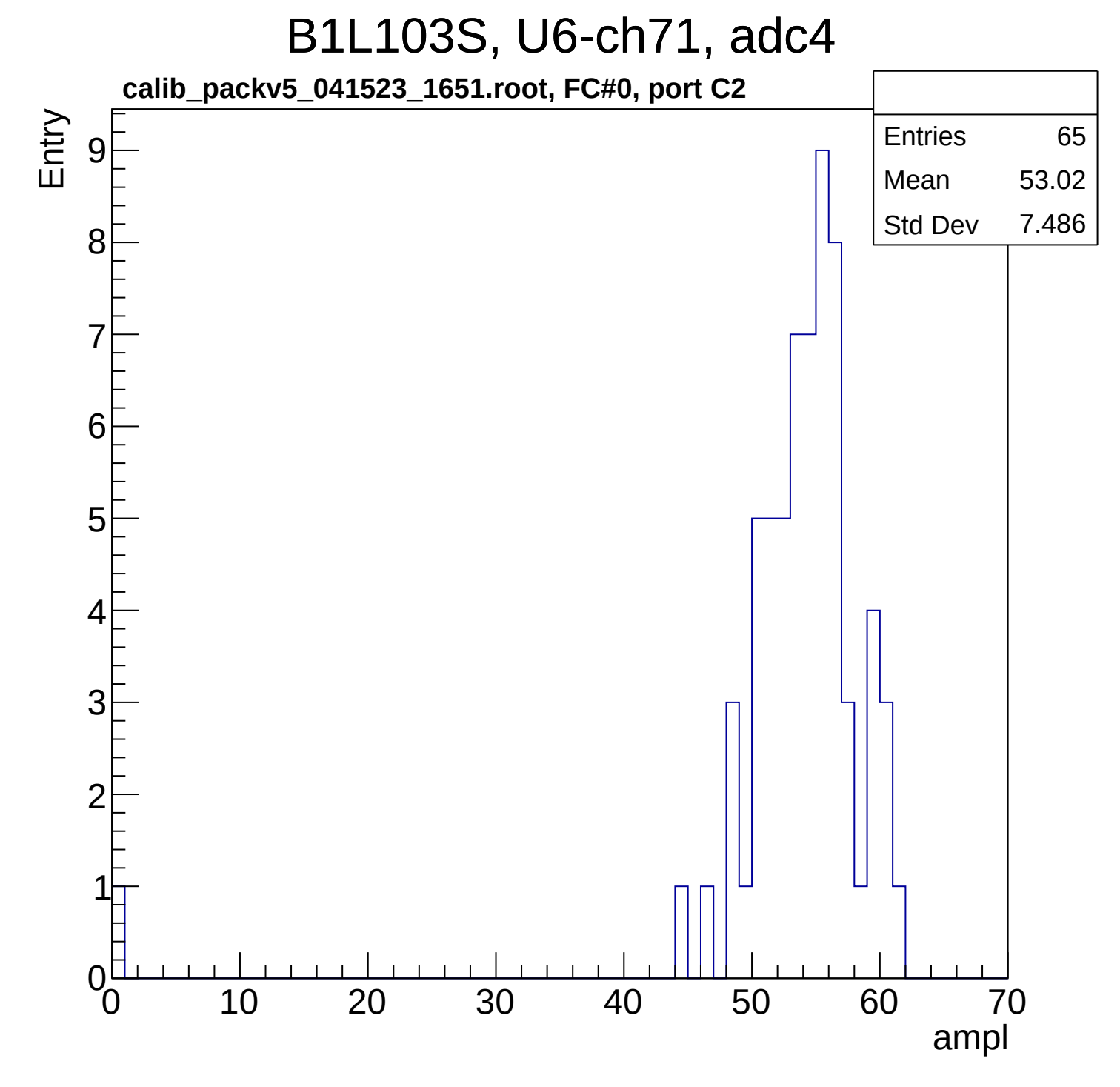

B1L103S, U6-ch70, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

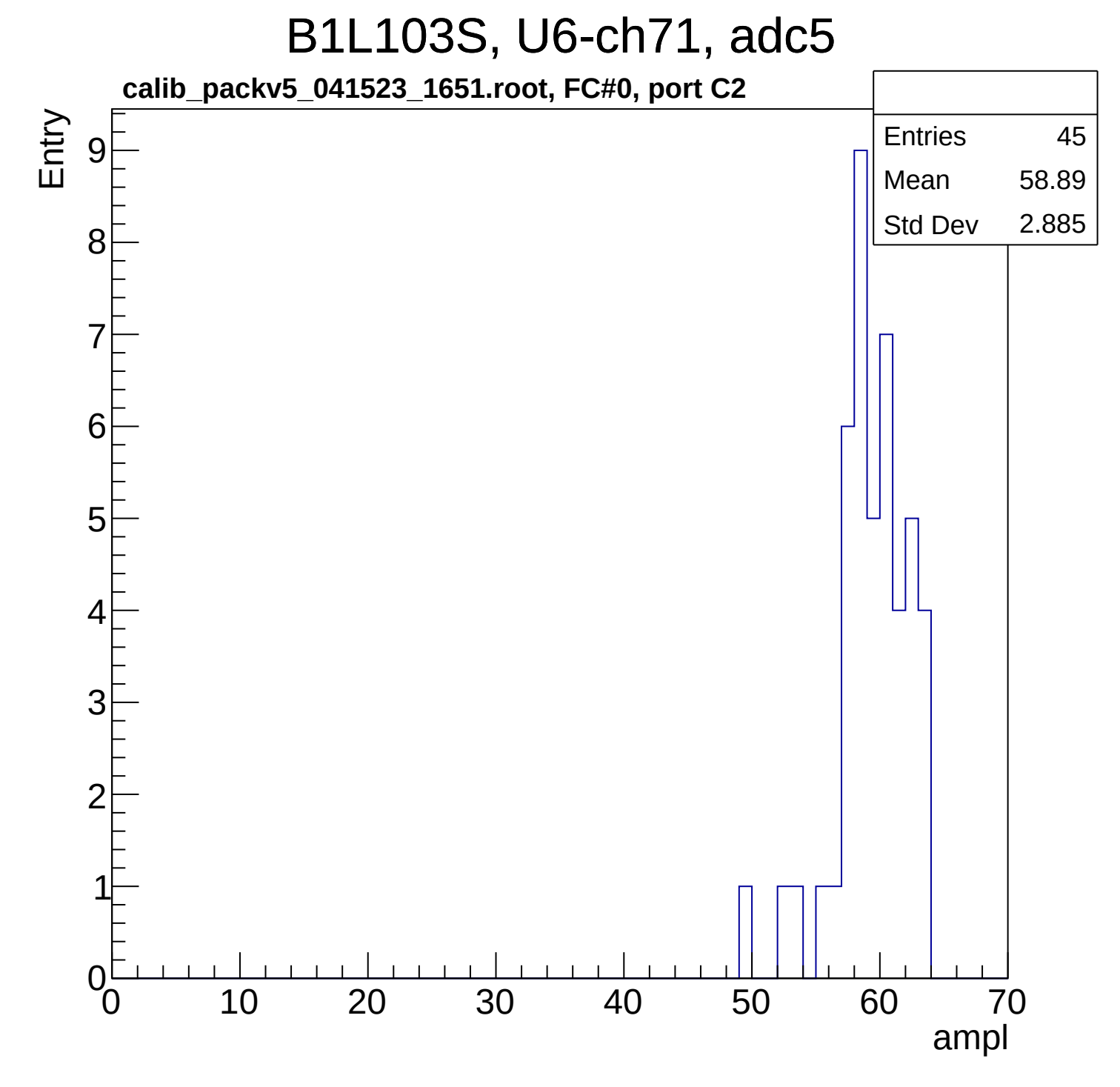

B1L103S, U6-ch71, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 96
Mean 26.48
Std Dev 7.602
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U6-ch71, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 35.78
Std Dev 2.807
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U6-ch71, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 37.86
Std Dev 11.38
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch71, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 42.05
Std Dev 15.89
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch71, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 53.02
Std Dev 7.486
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch71, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 58.89
Std Dev 2.885
Entry
ampl
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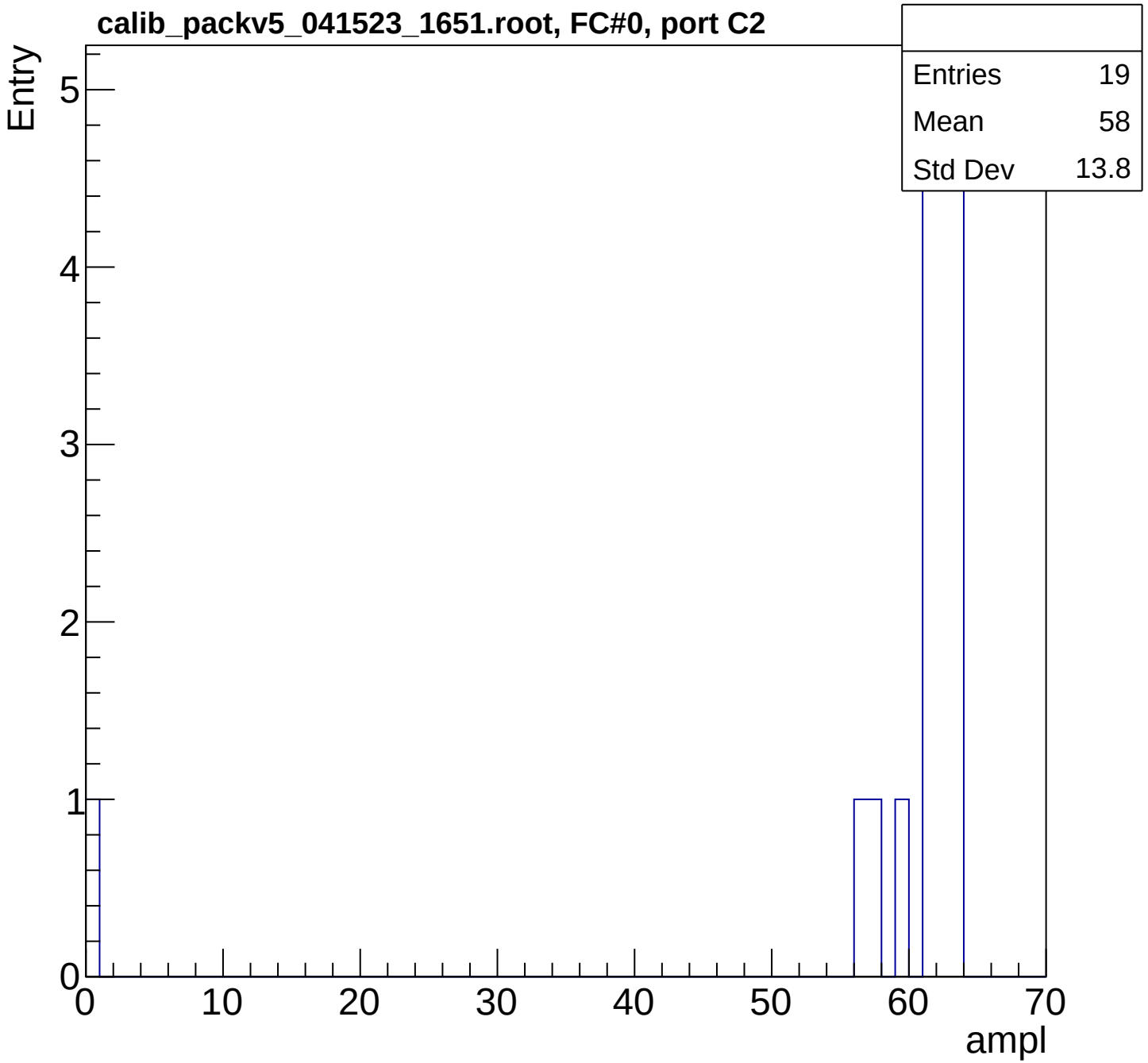
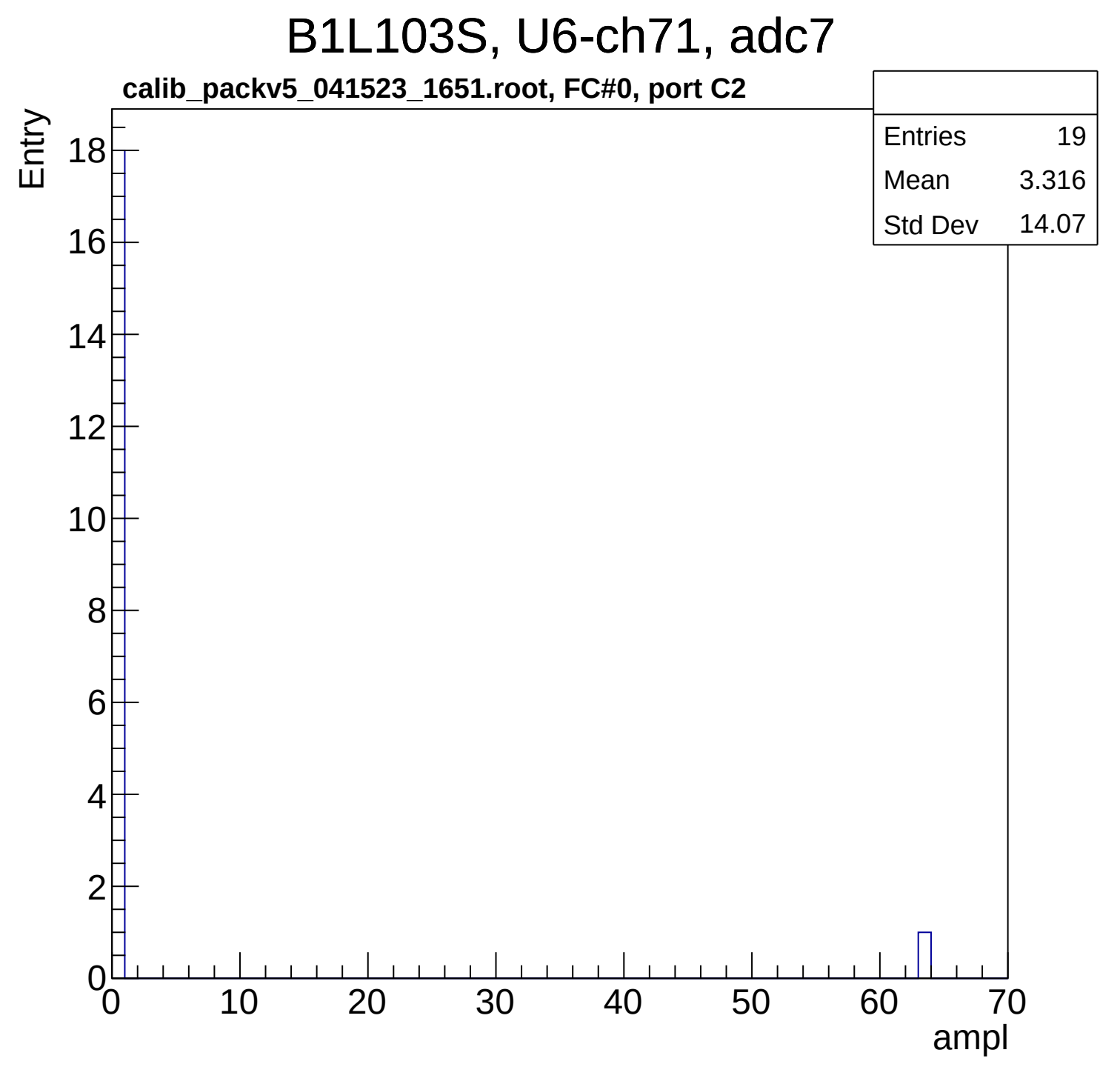
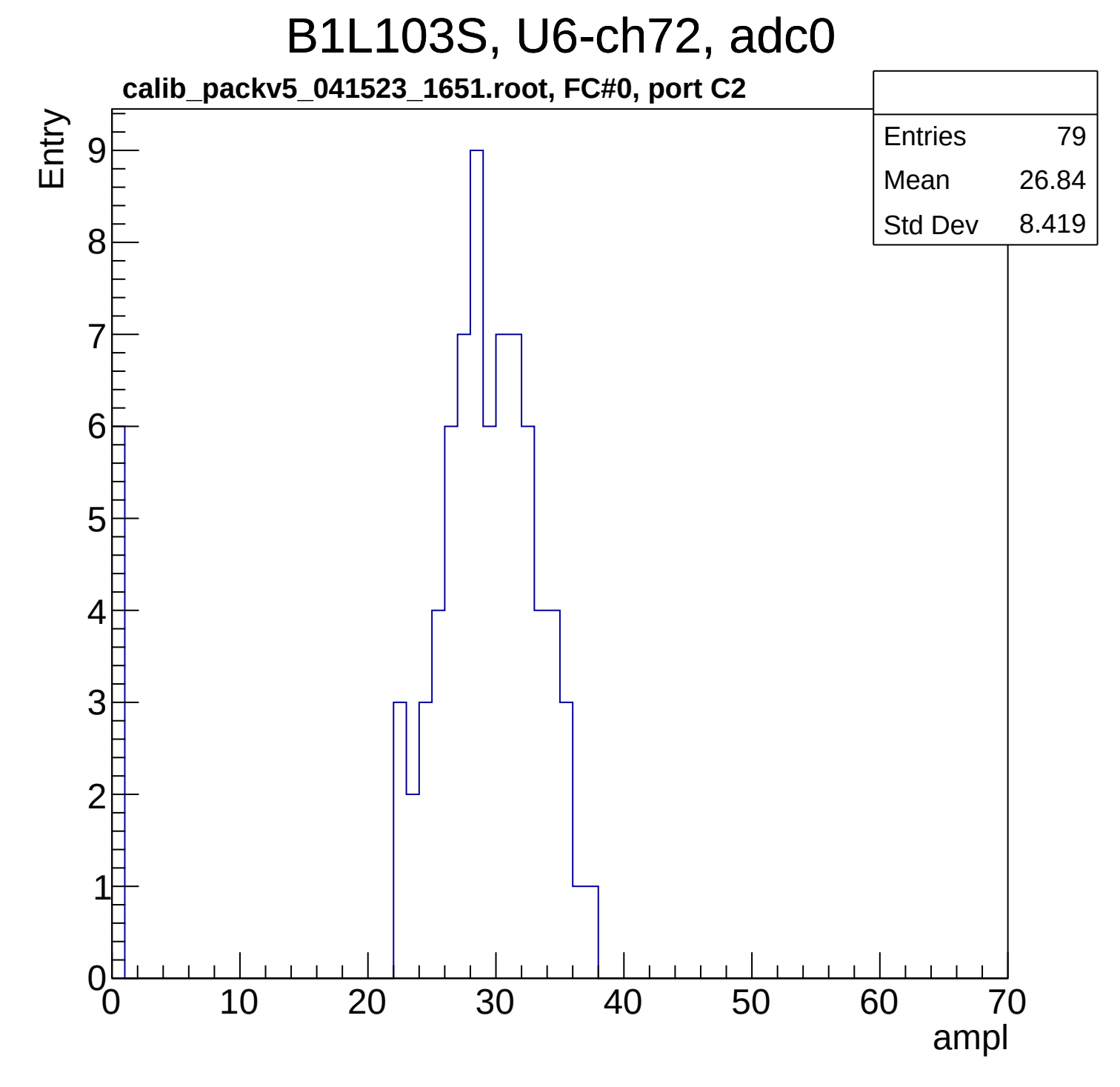
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch71, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 58
Std Dev 13.8
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch71, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.316
Std Dev 14.07
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch72, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 26.84
Std Dev 8.419
Entry
ampl
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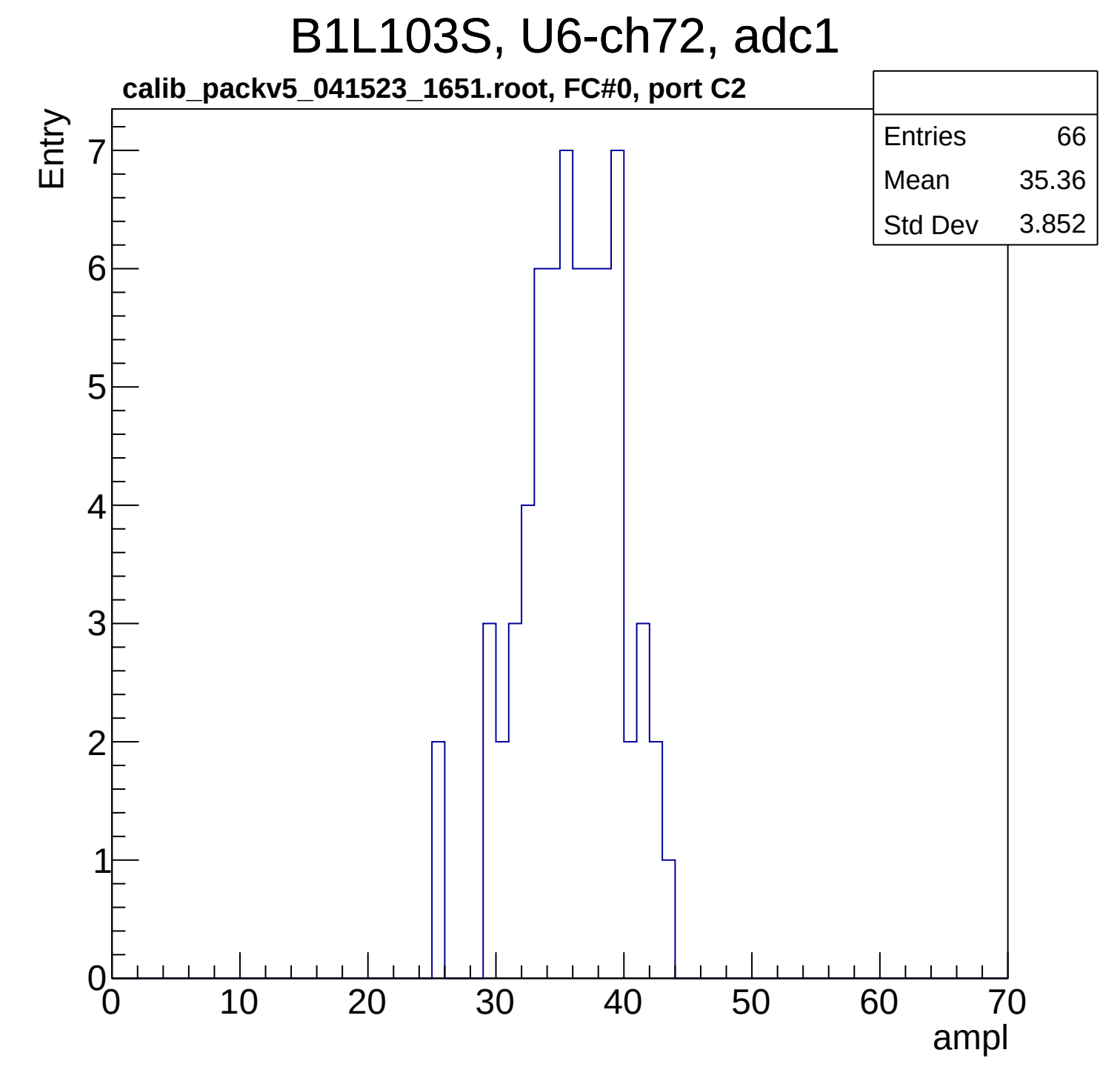
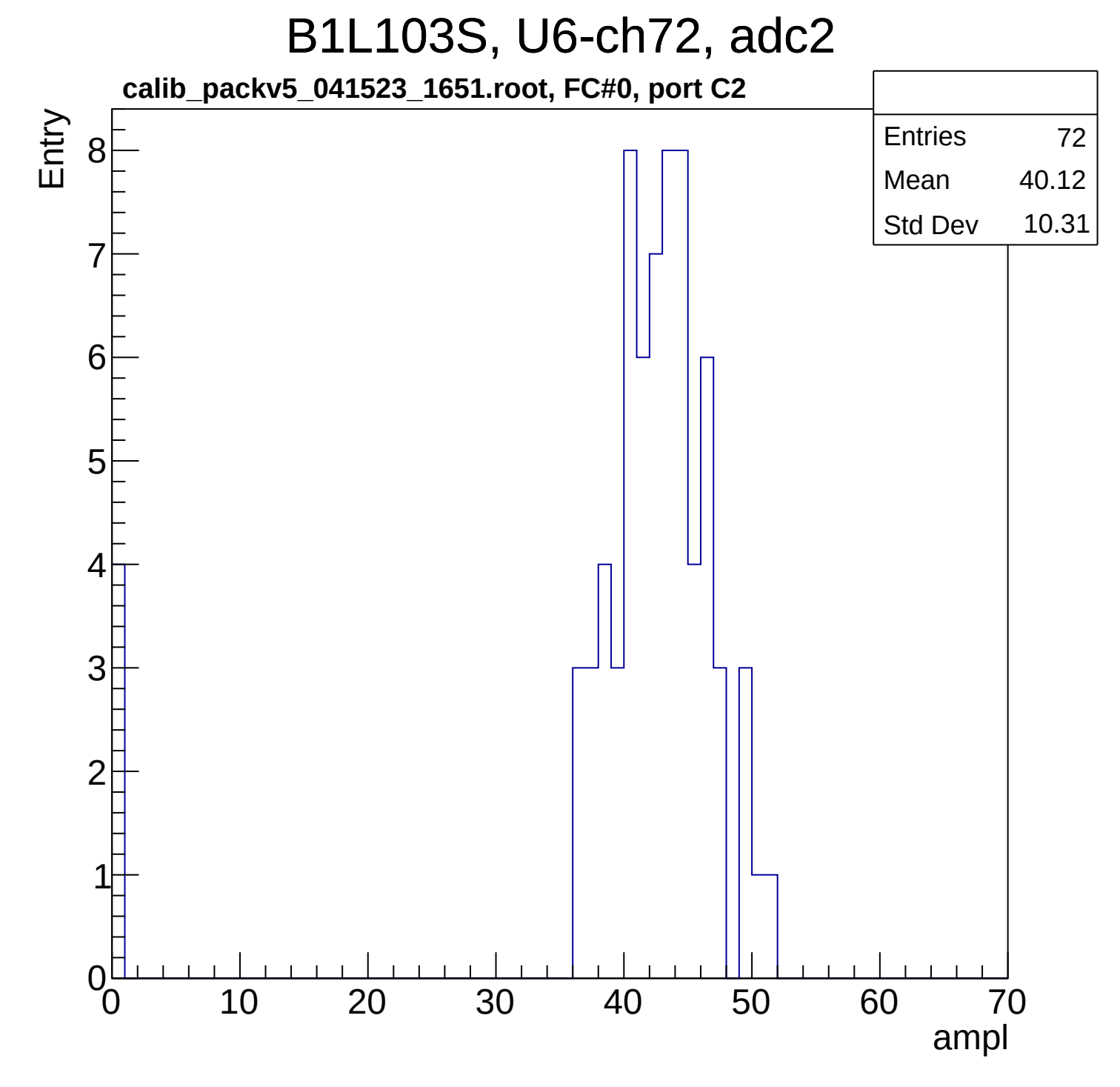
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch72, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 35.36
Std Dev 3.852
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U6-ch72, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 40.12
Std Dev 10.31
Entry
ampl
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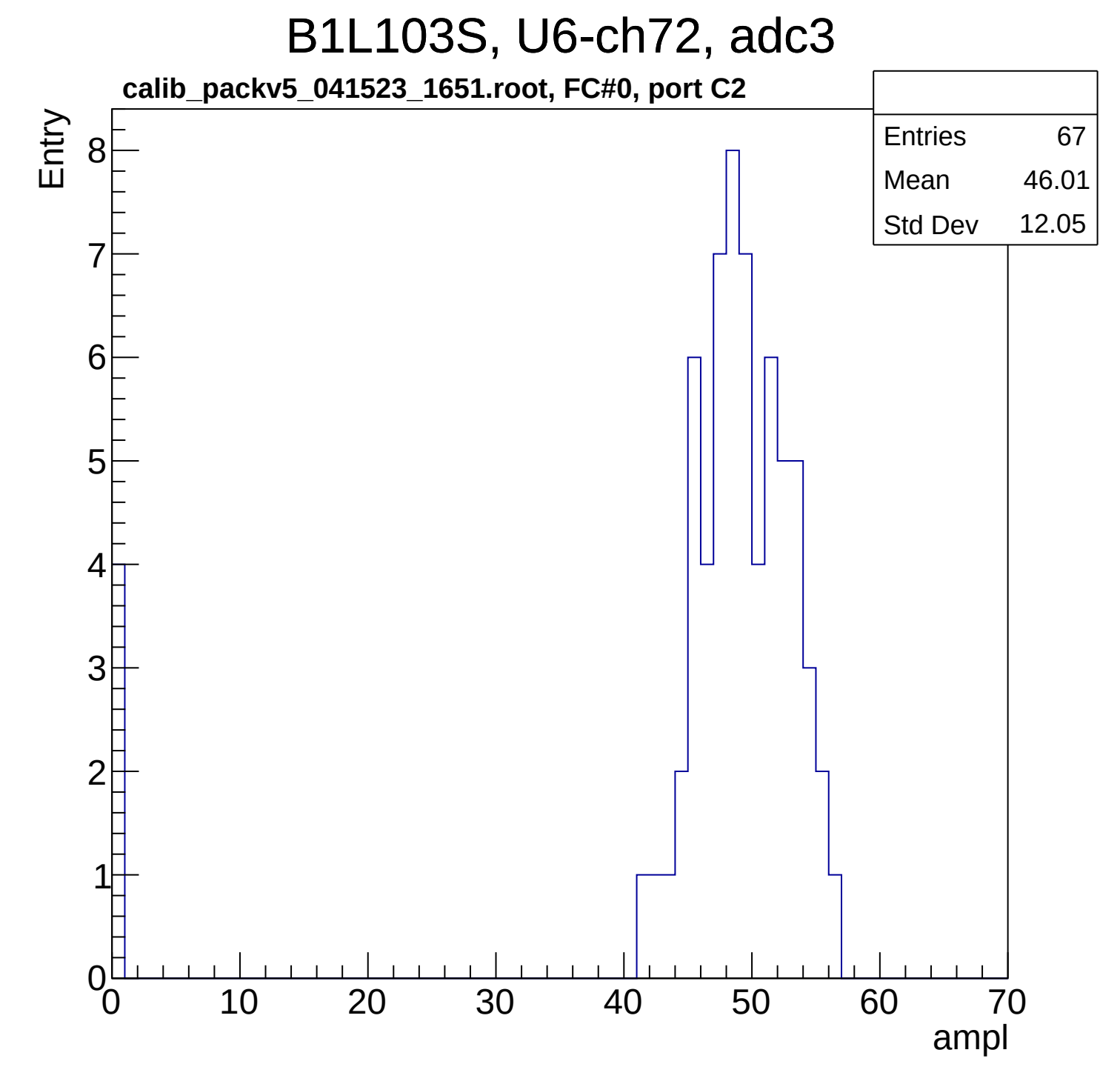
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch72, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 46.01
Std Dev 12.05
Entry
ampl
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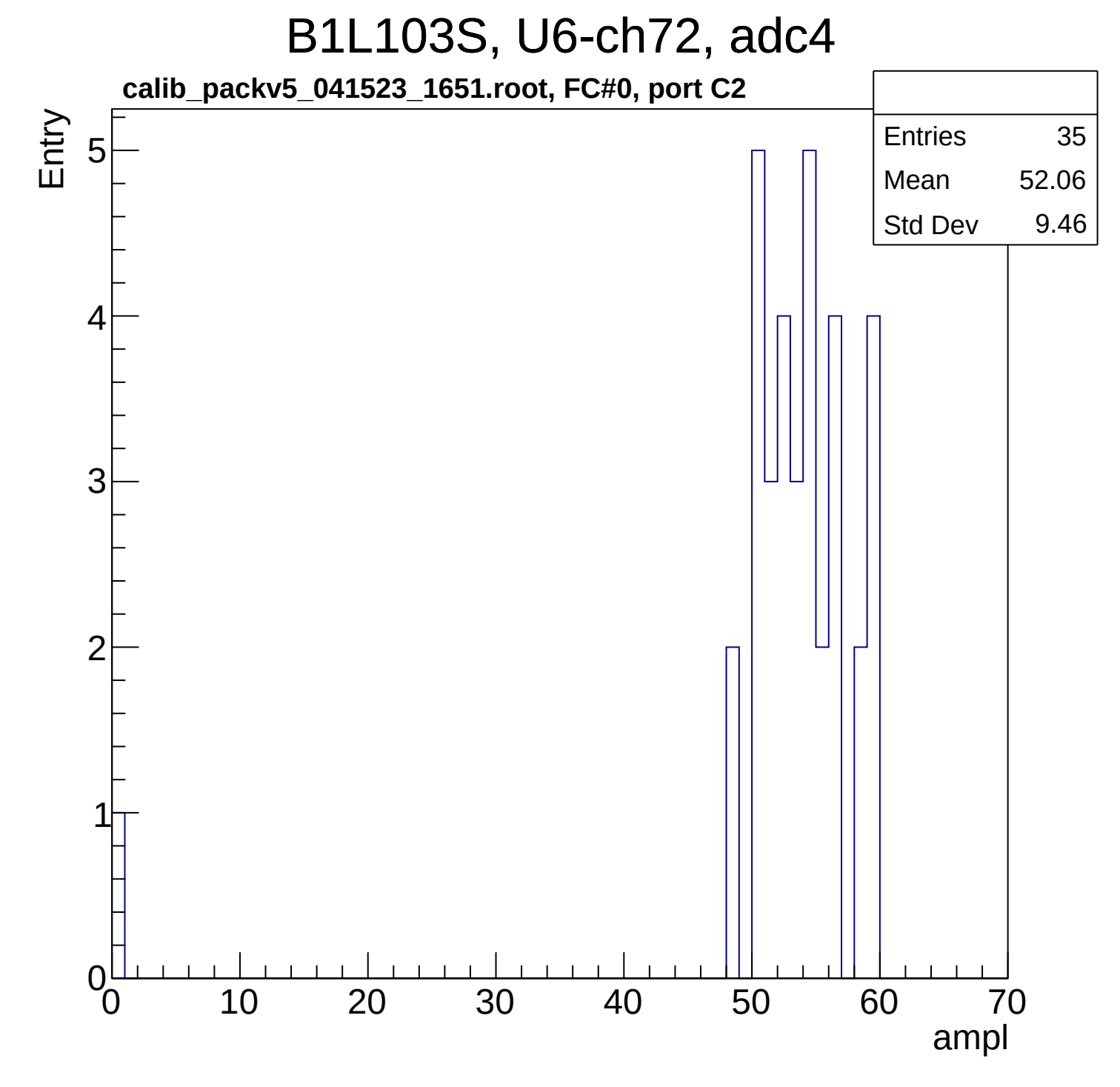
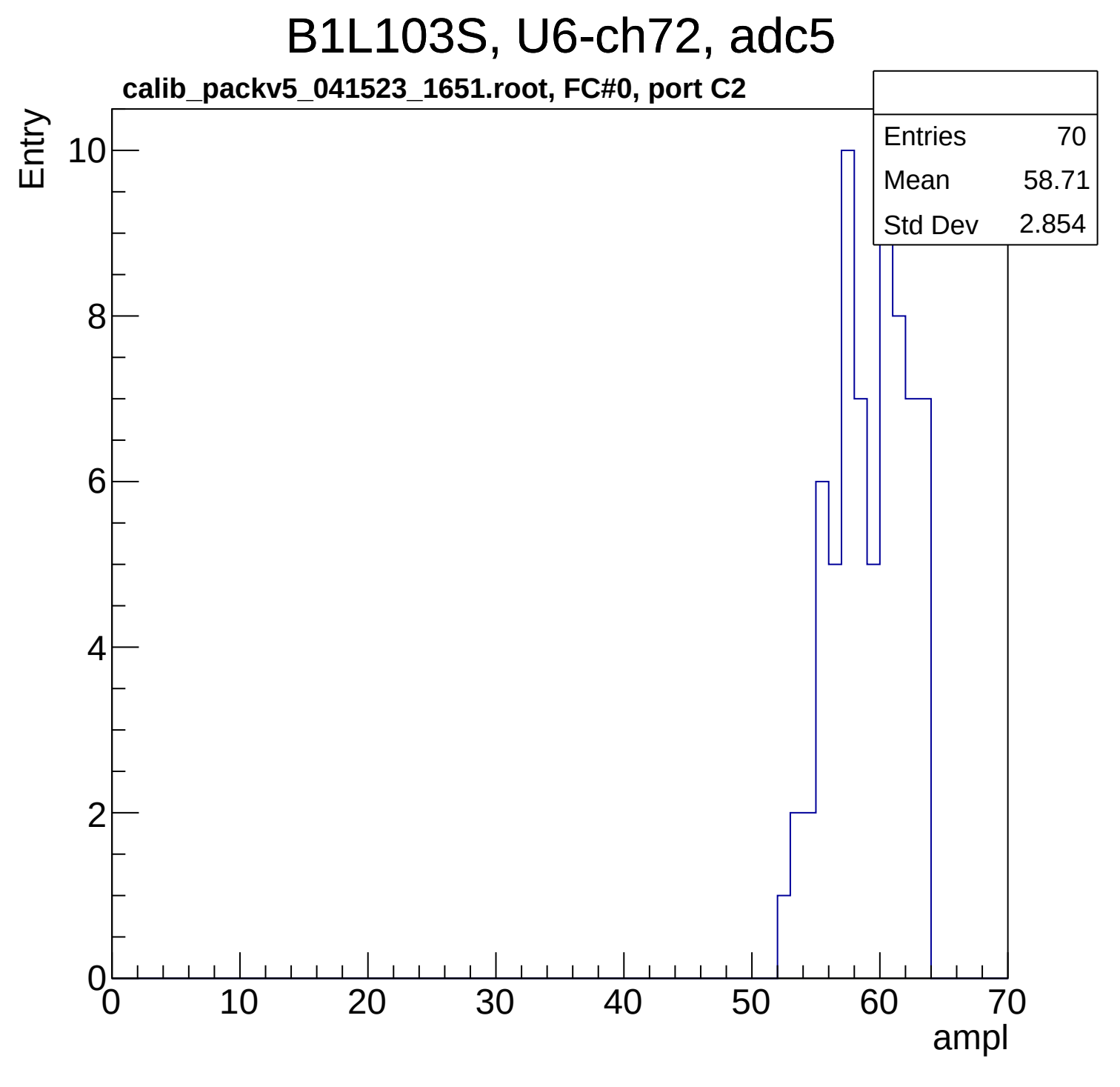
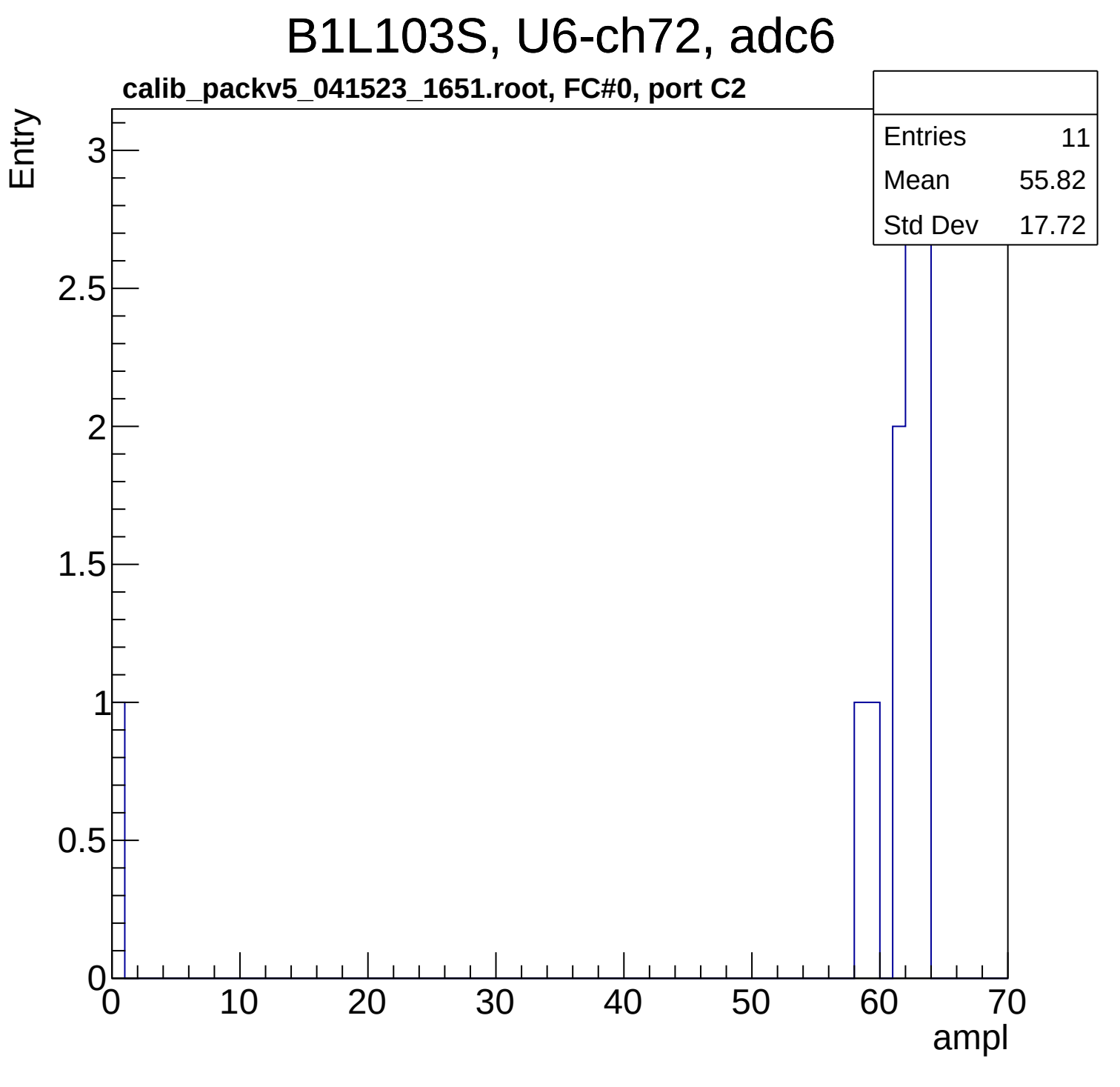
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch72, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 52.06
Std Dev 9.46
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U6-ch72, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 58.71
Std Dev 2.854
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U6-ch72, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 55.82
Std Dev 17.72
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
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40
50
60
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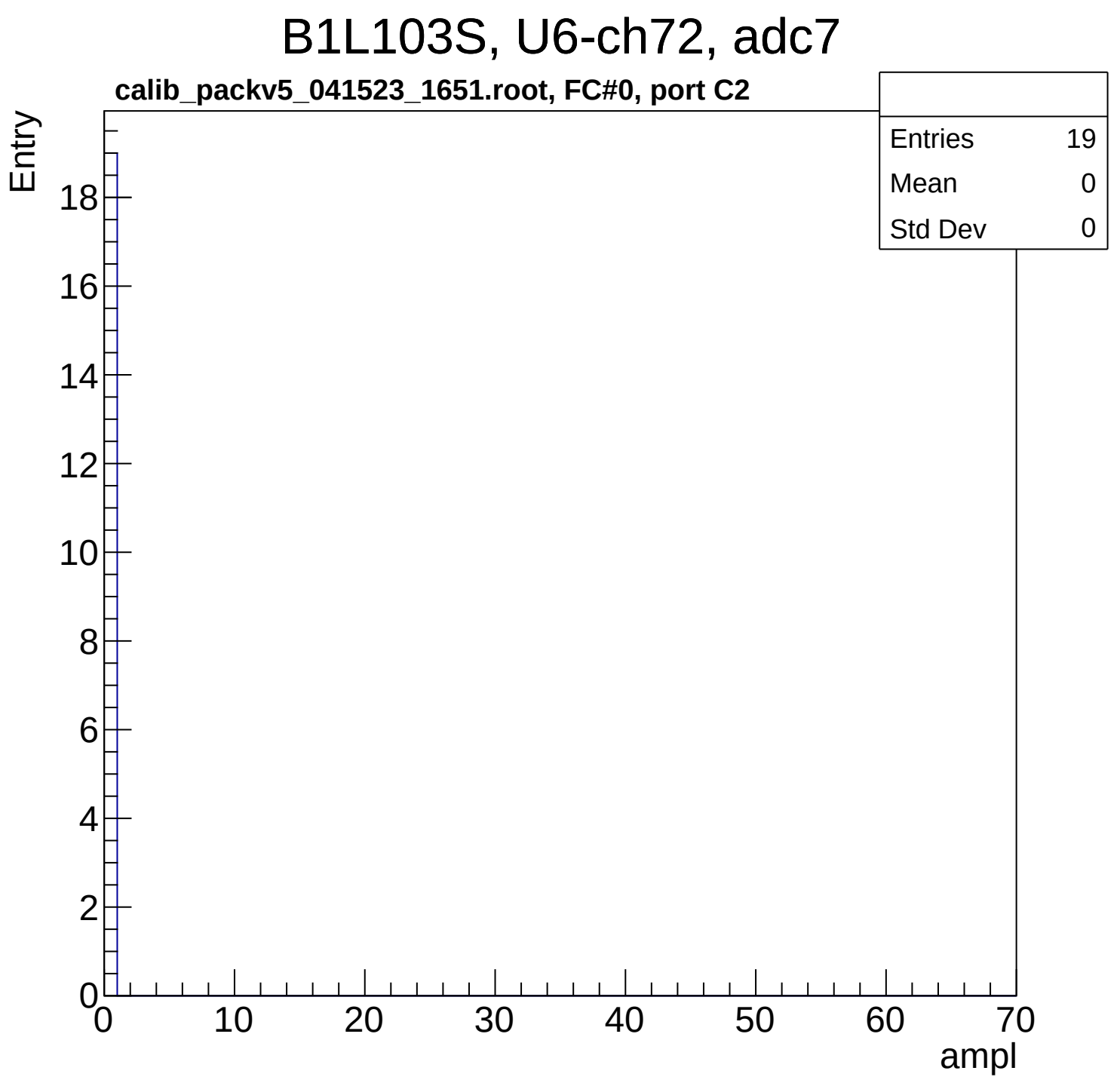
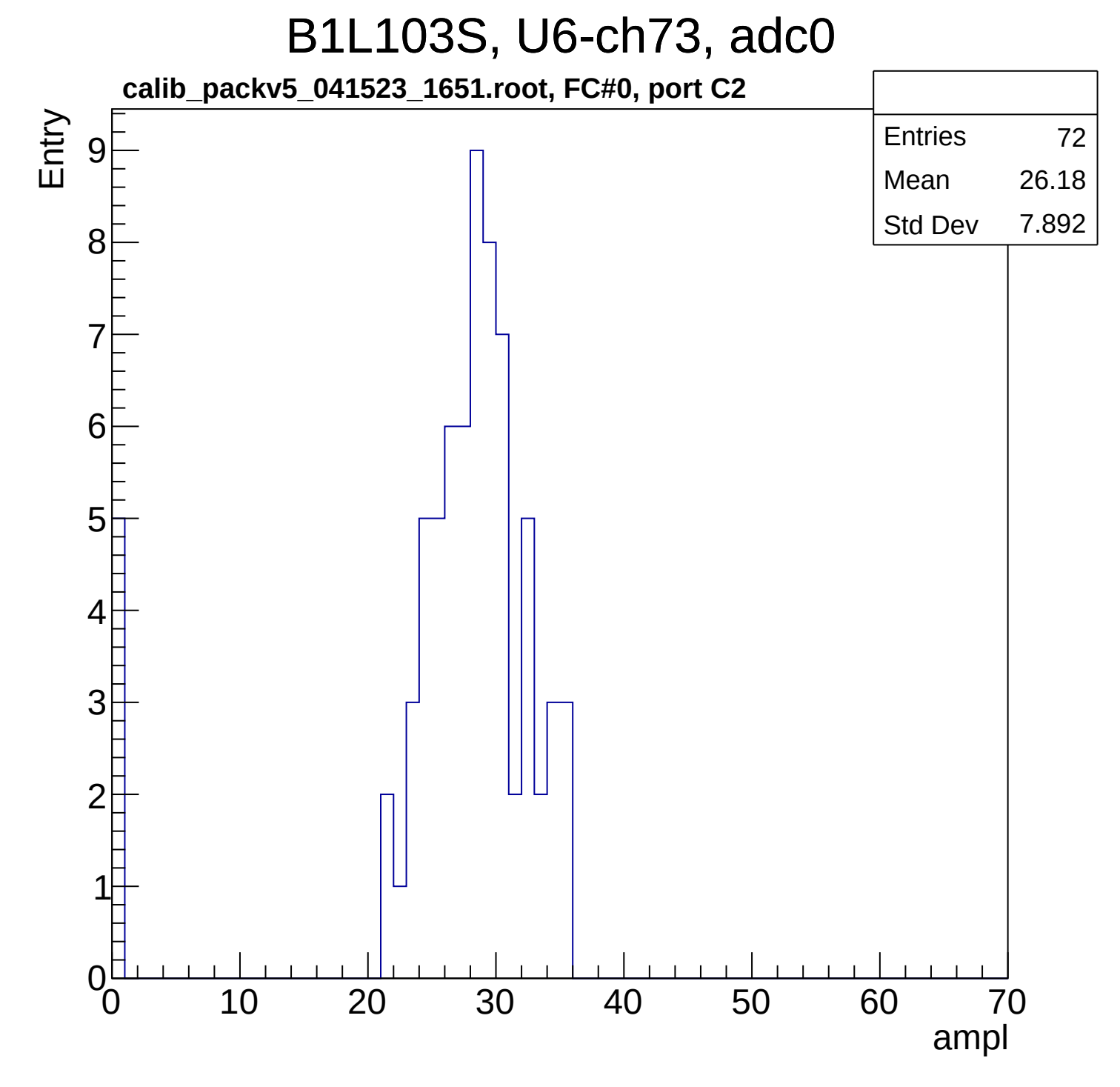

B1L103S, U6-ch72, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch73, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 26.18
Std Dev 7.892
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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40
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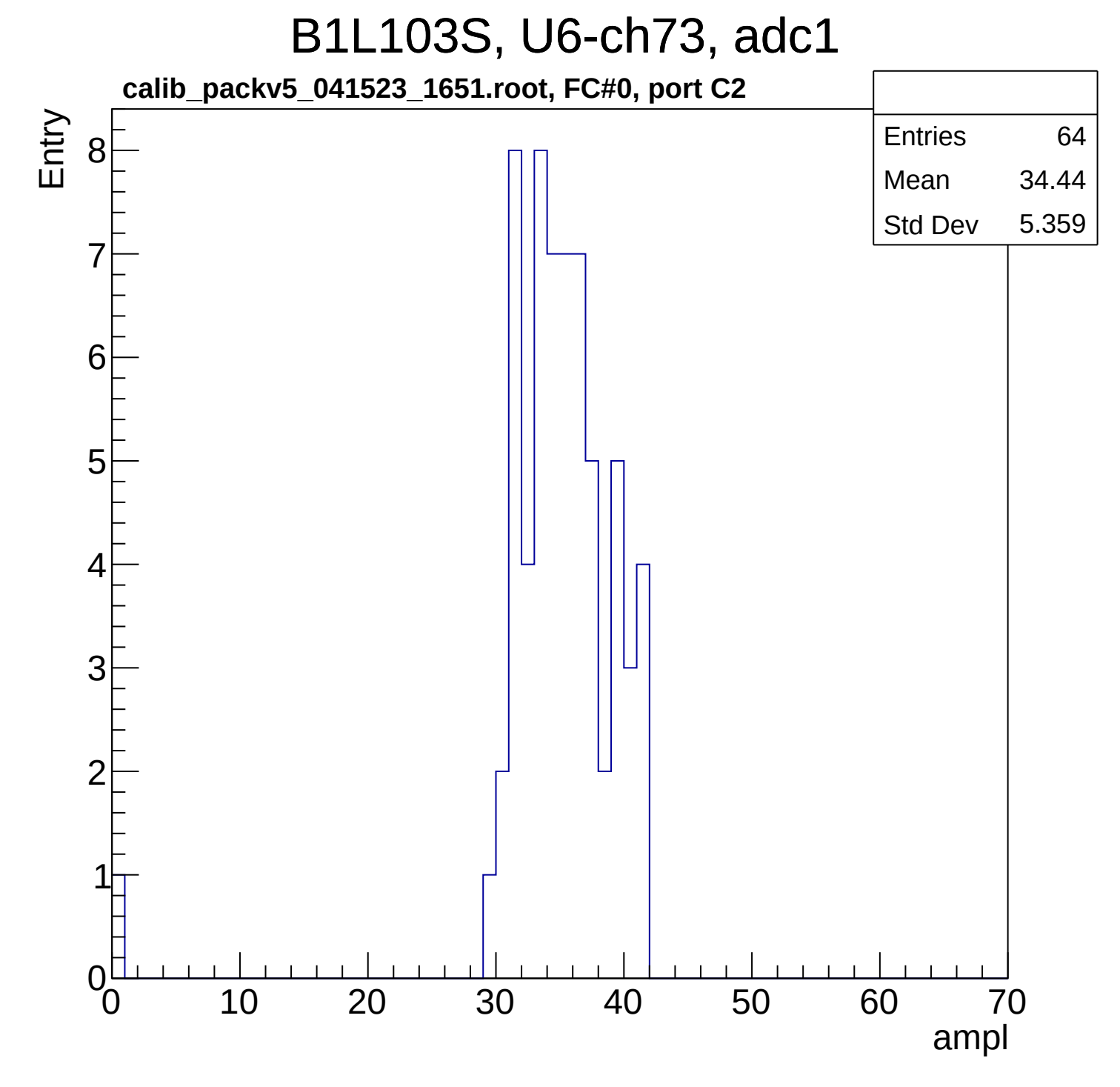
60
70


B1L103S, U6-ch73, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 34.44
Std Dev 5.359
Entry
ampl
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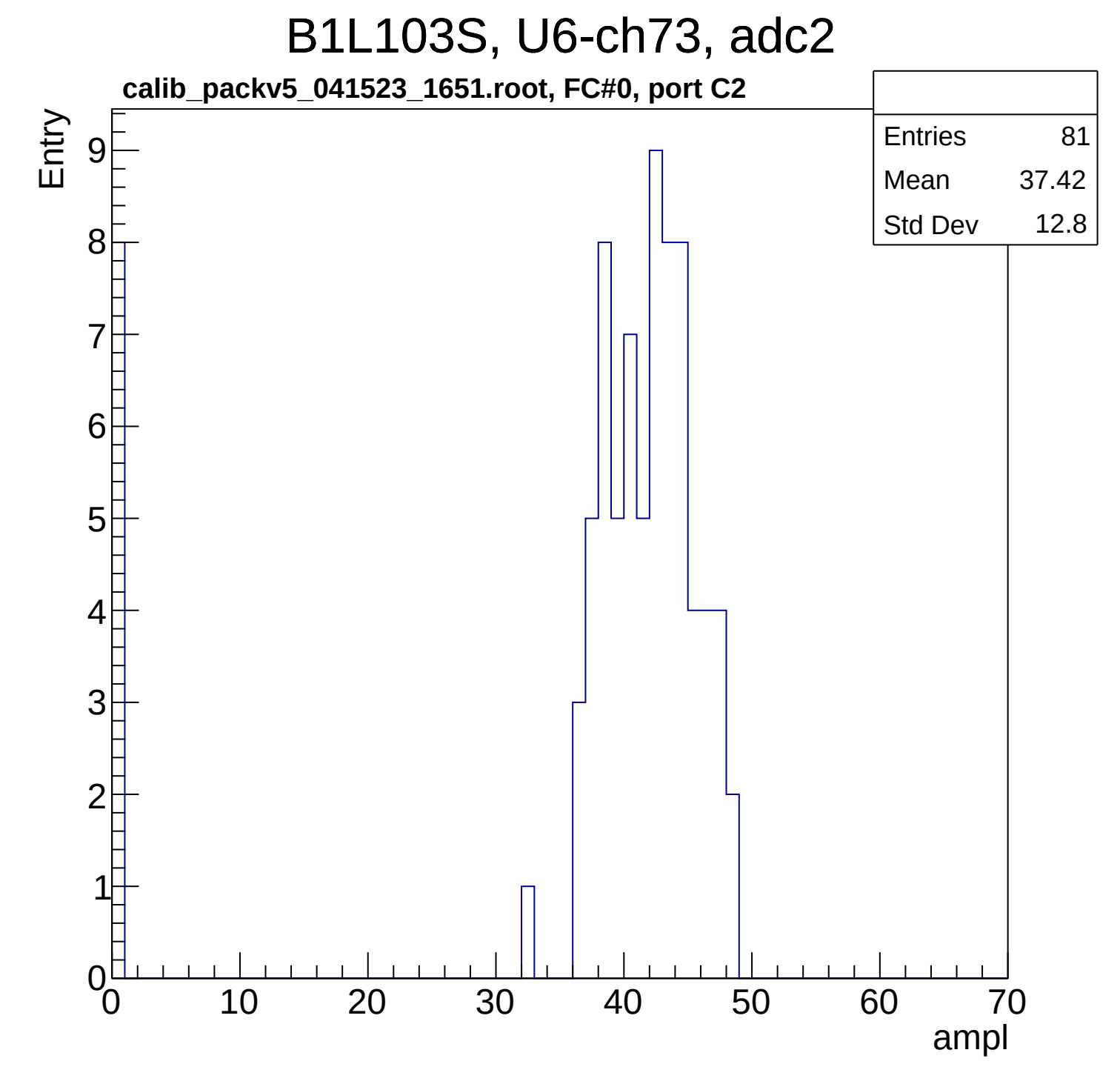
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch73, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 37.42
Std Dev 12.8
Entry
ampl
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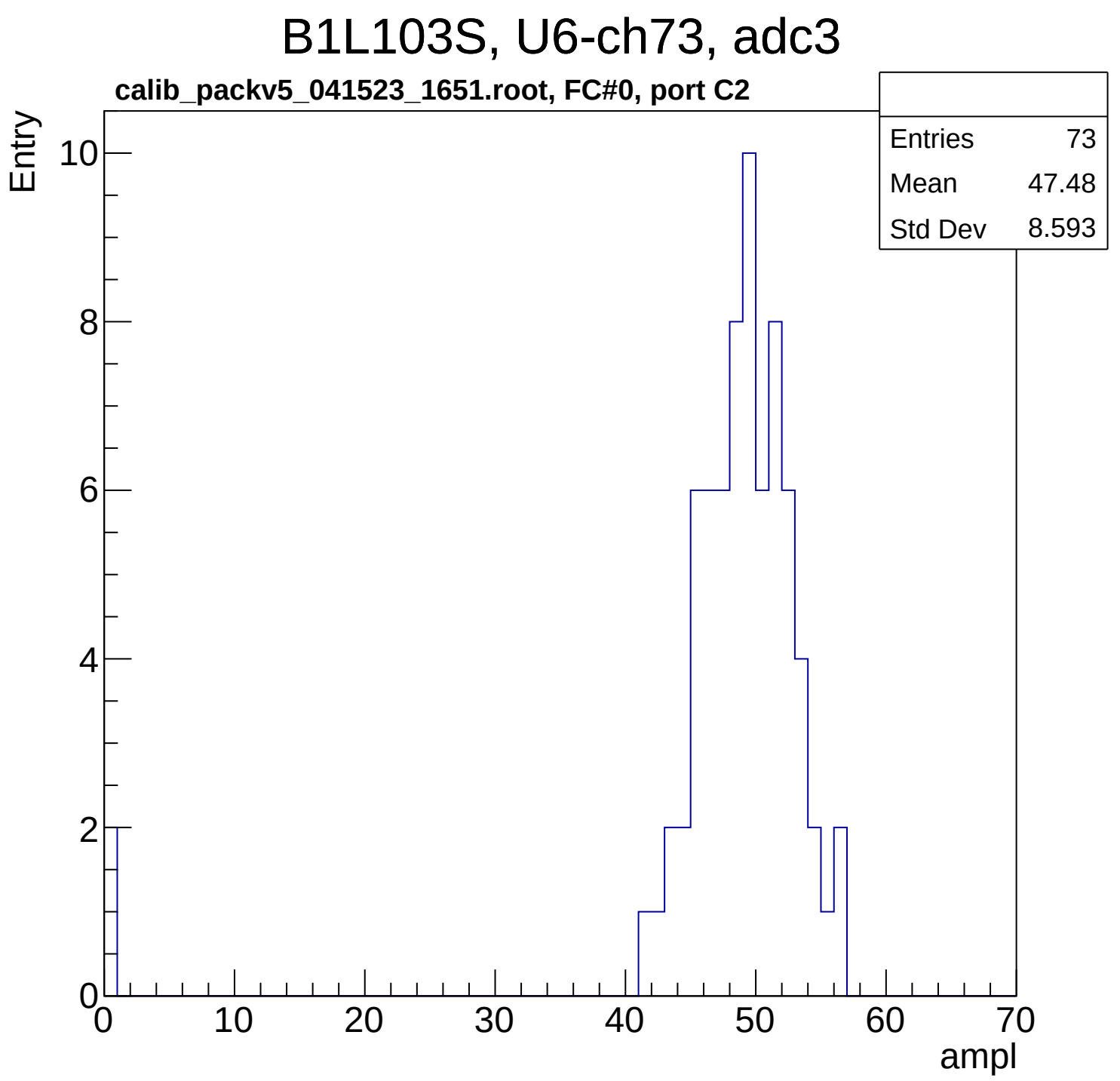
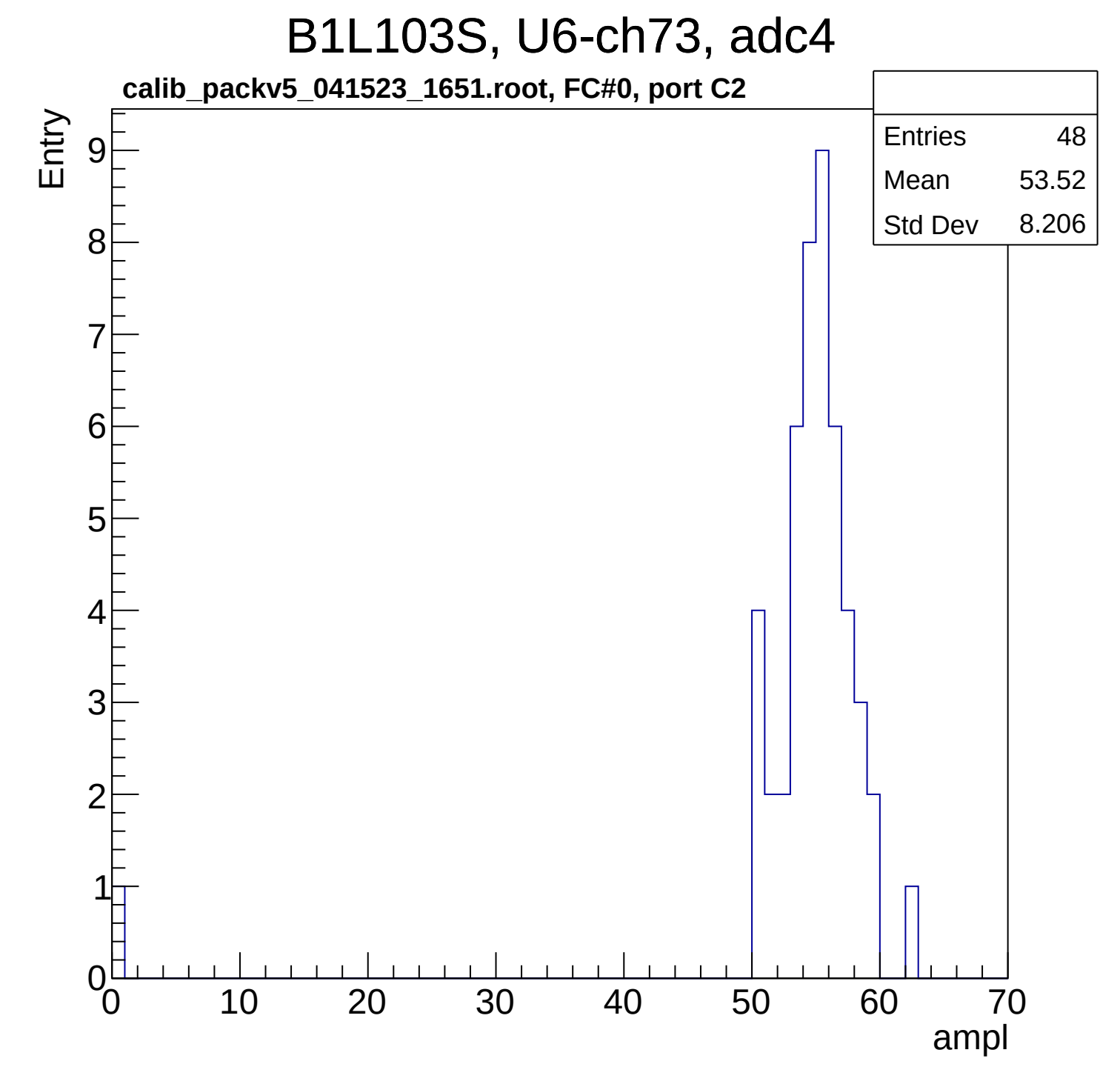
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch73, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 47.48
Std Dev 8.593
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch73, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 53.52
Std Dev 8.206
Entry
ampl
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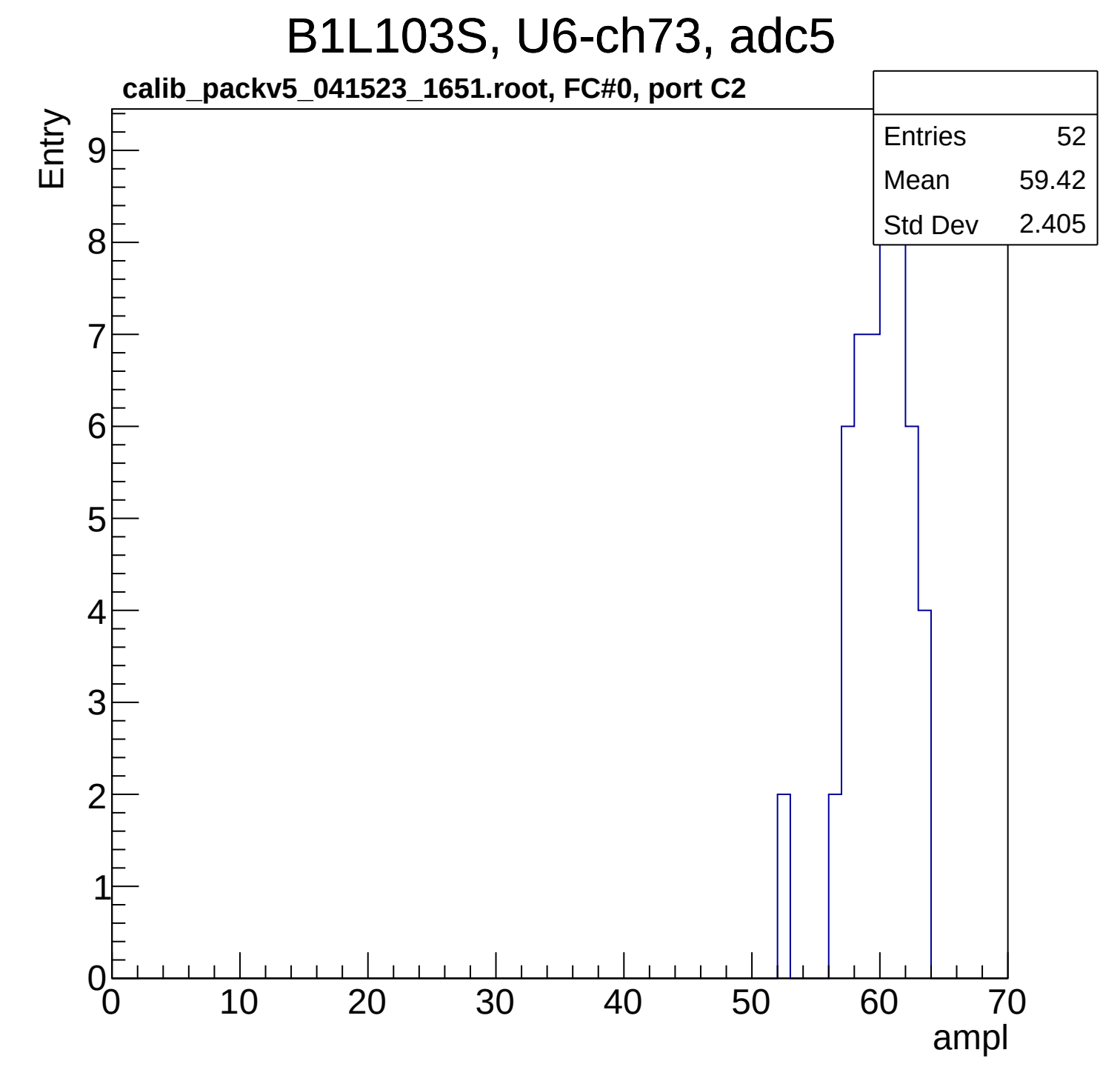
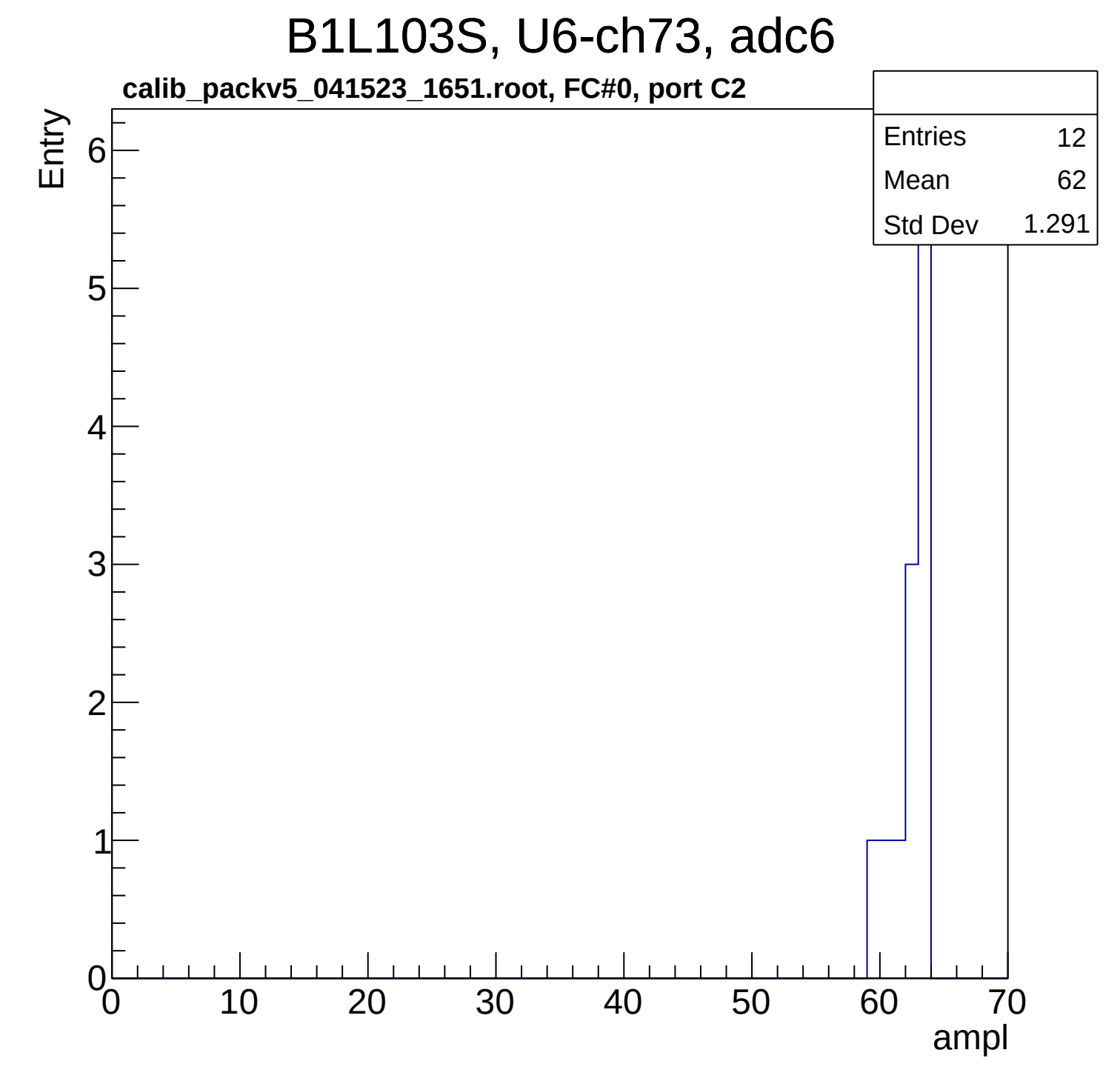
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch73, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 59.42
Std Dev 2.405
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch73, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 62
Std Dev 1.291
Entry
0
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2
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4
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6
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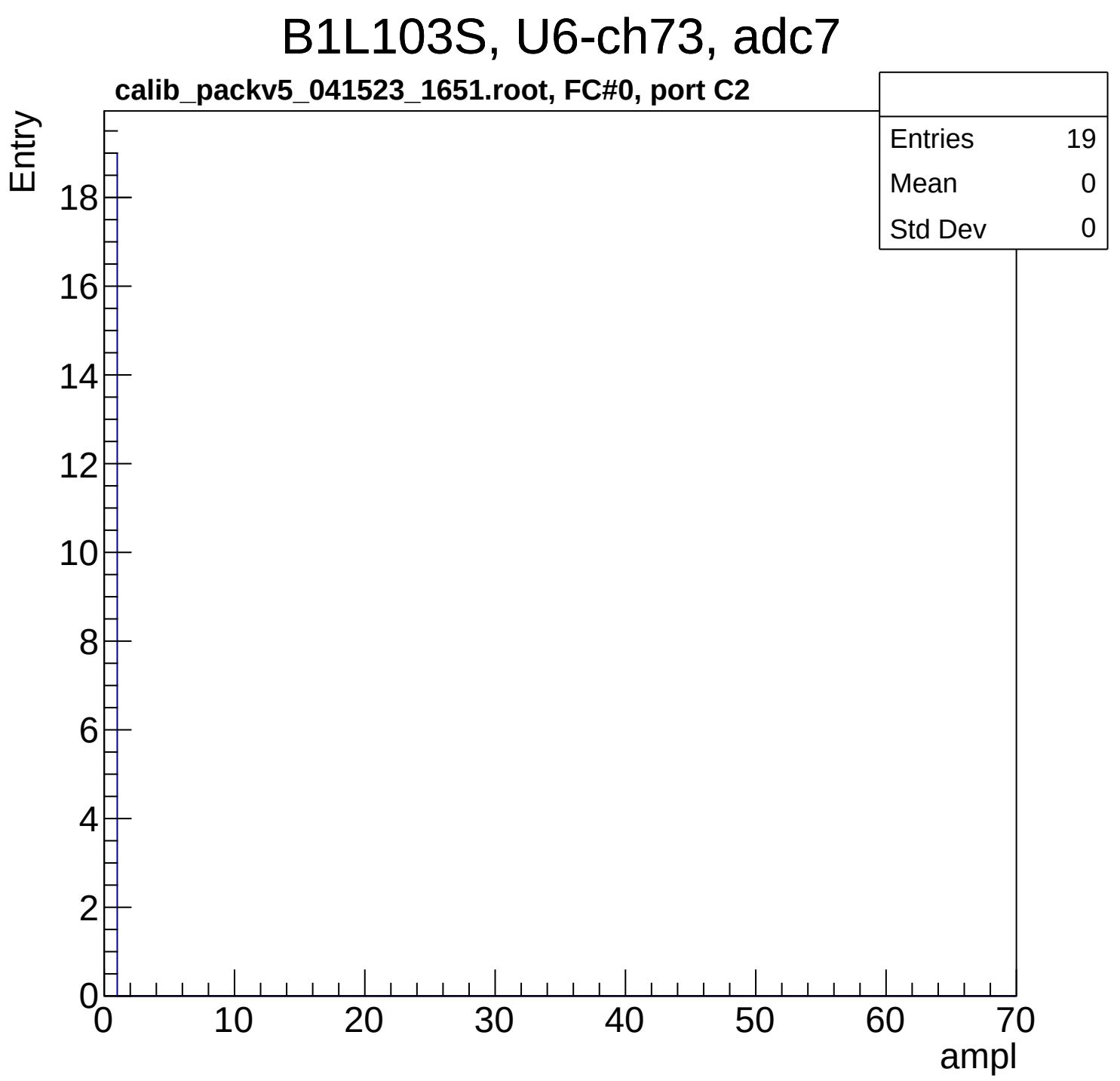
ampl


B1L103S, U6-ch73, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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2
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6
8
10
12
14
16
18
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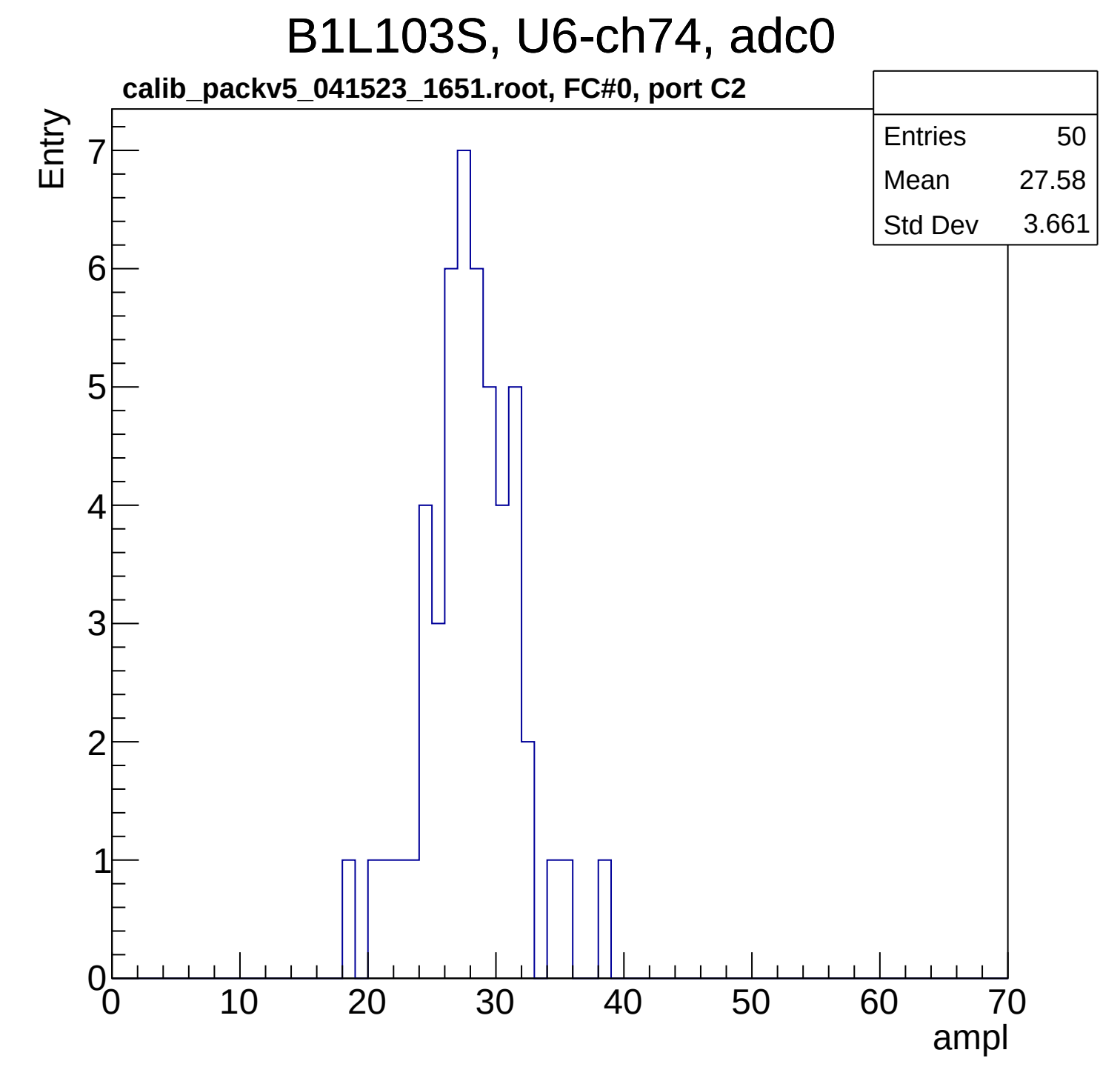
50
60
70
ampl


B1L103S, U6-ch74, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 27.58
Std Dev 3.661
Entry
ampl
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2
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4
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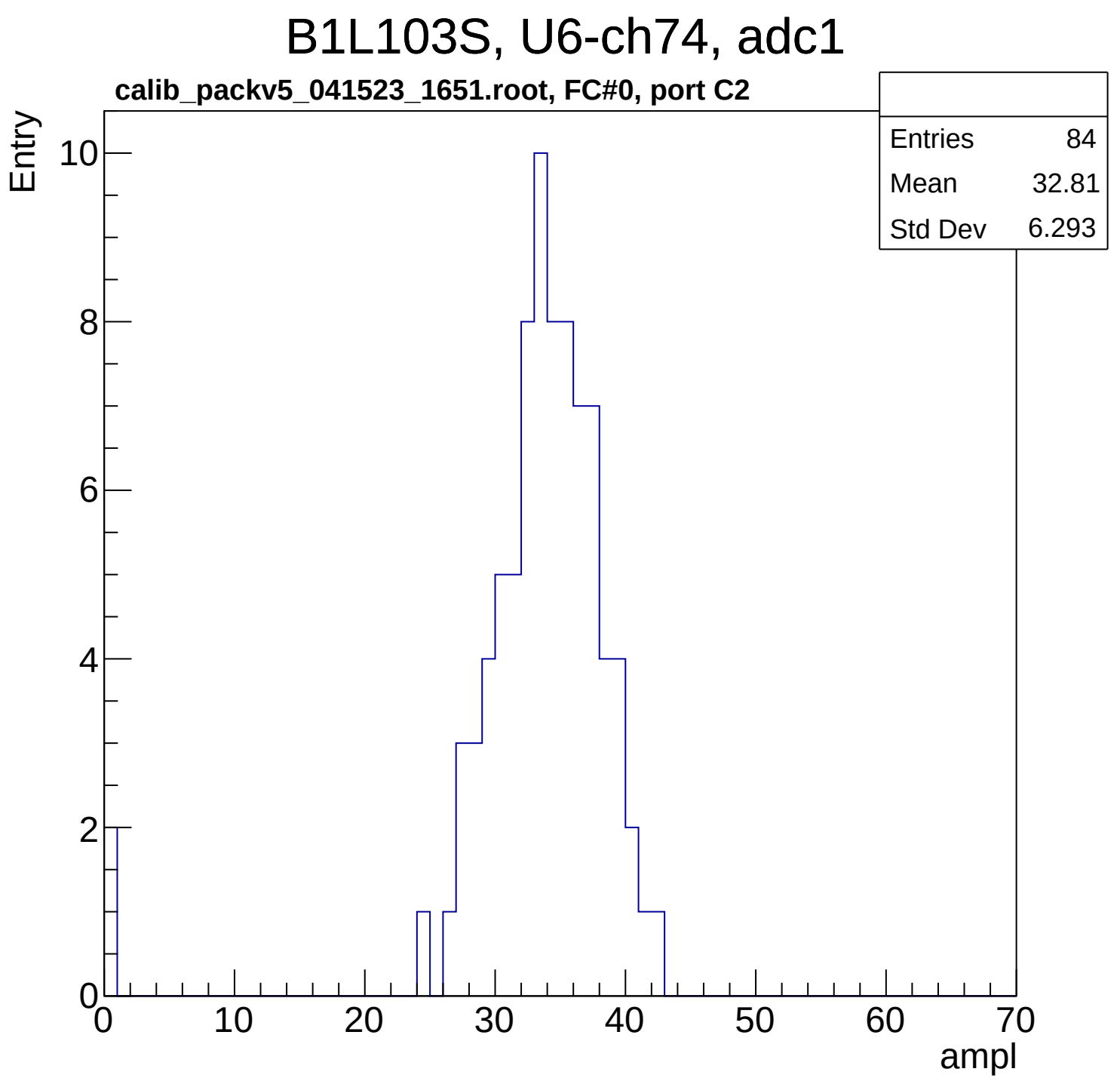
B1L103S, U6-ch74, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 32.81
Std Dev 6.293
Entry
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10
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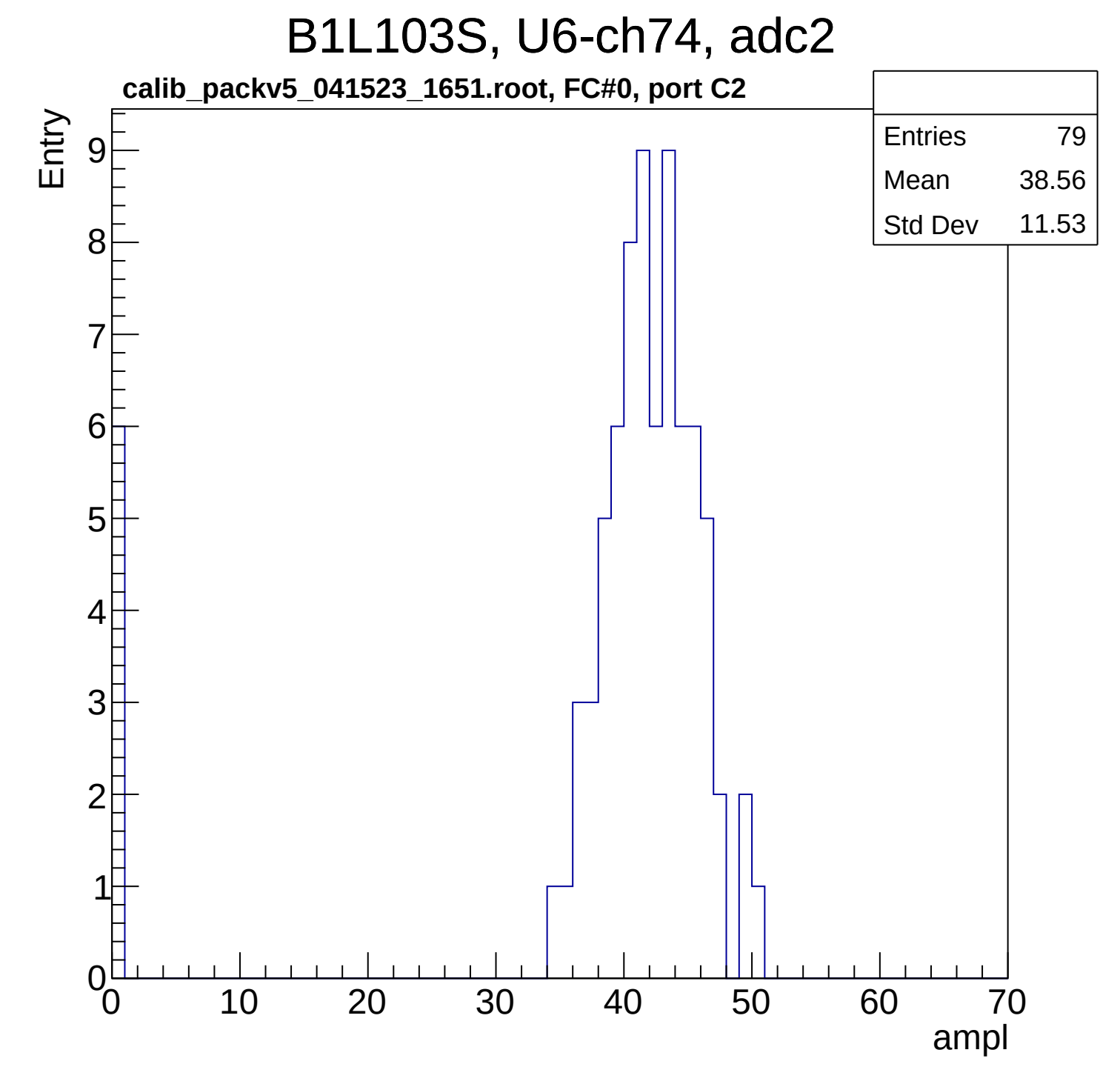
ampl


B1L103S, U6-ch74, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 38.56
Std Dev 11.53
Entry
ampl
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2
3
4
5
6
7
8
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0
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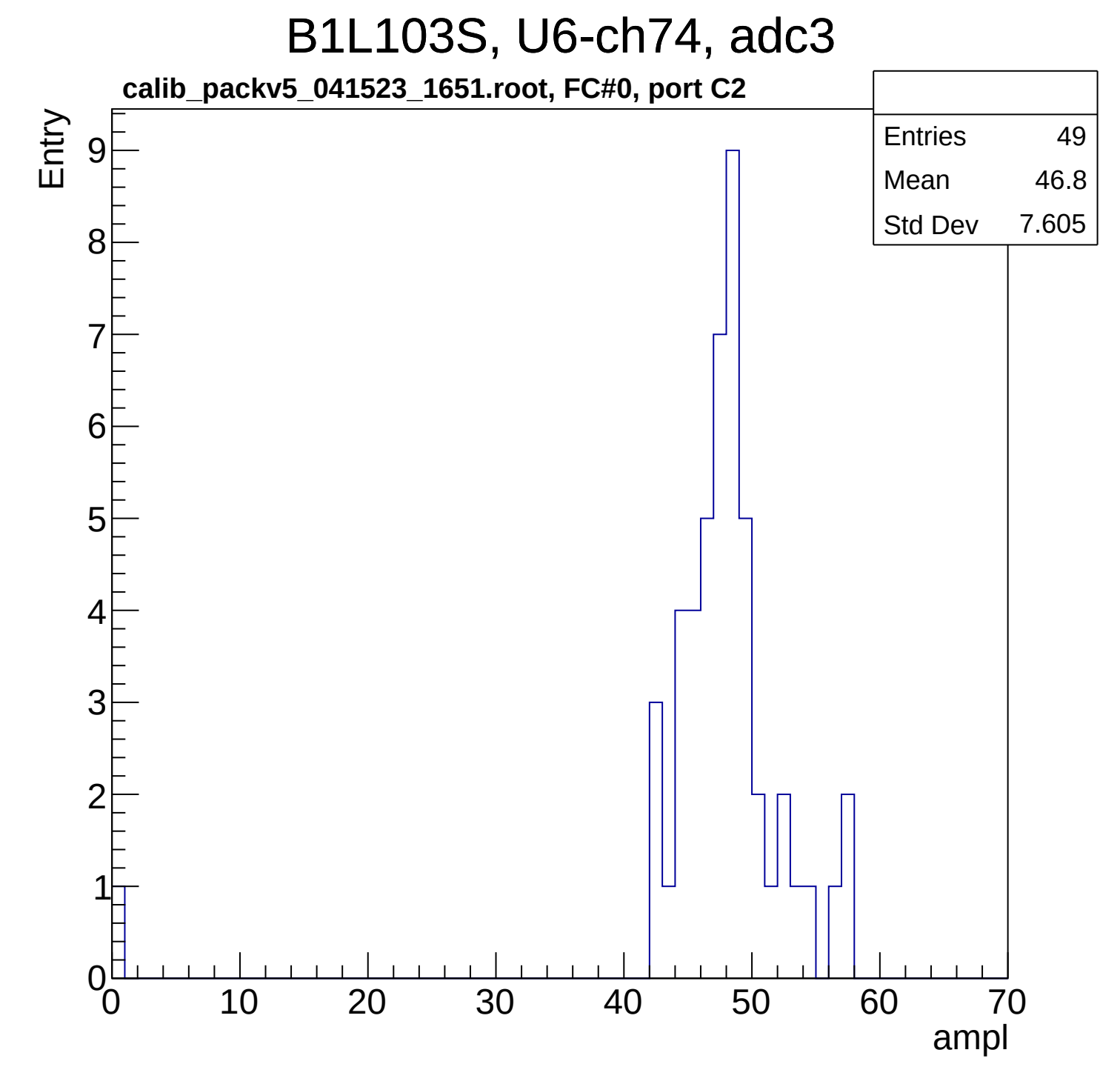
B1L103S, U6-ch74, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 46.8
Std Dev 7.605
Entry
ampl
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2
3
4
5
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7
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0
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40
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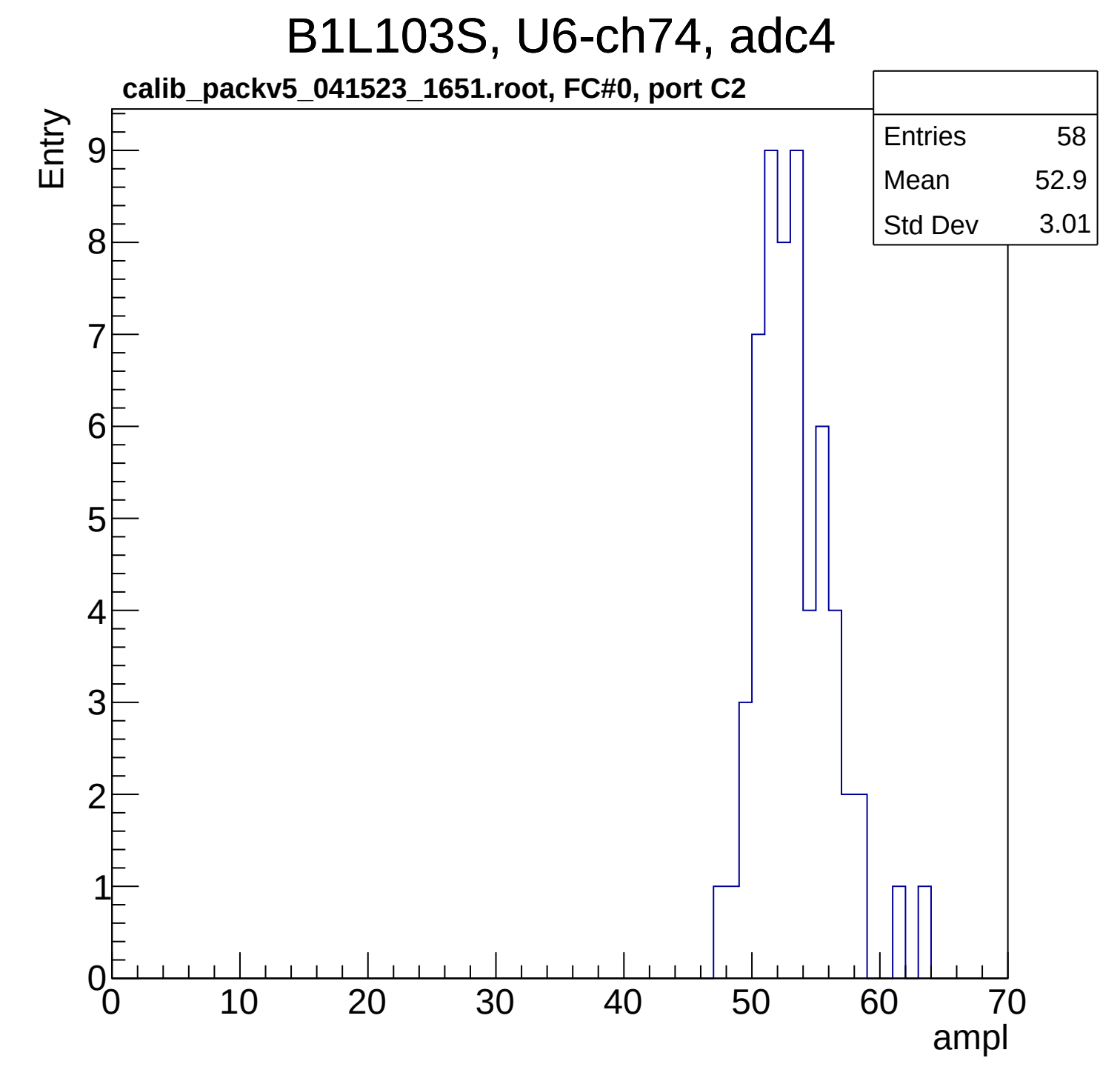
B1L103S, U6-ch74, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 52.9
Std Dev 3.01
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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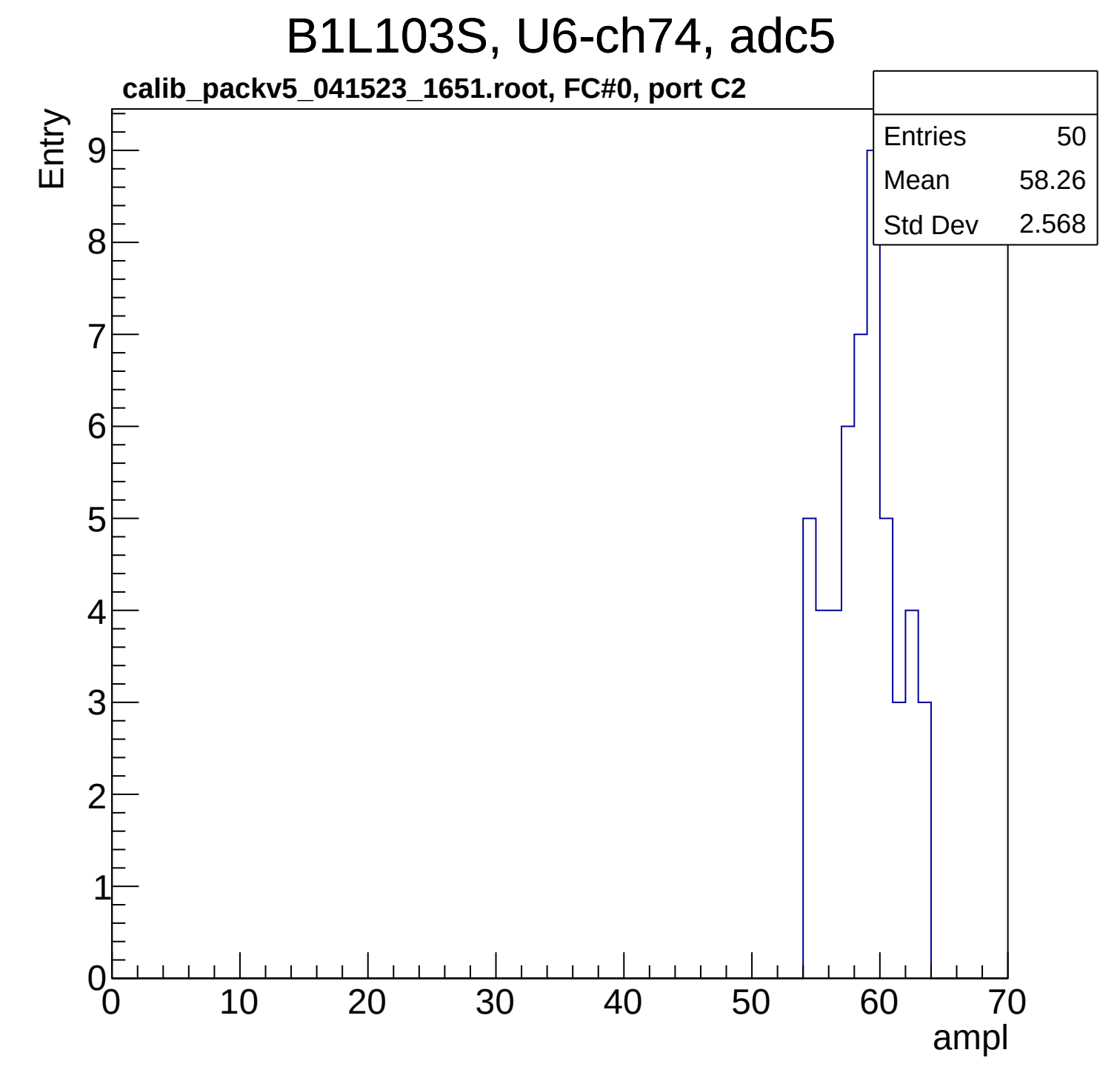
B1L103S, U6-ch74, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 58.26
Std Dev 2.568
Entry
ampl
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3
4
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7
8
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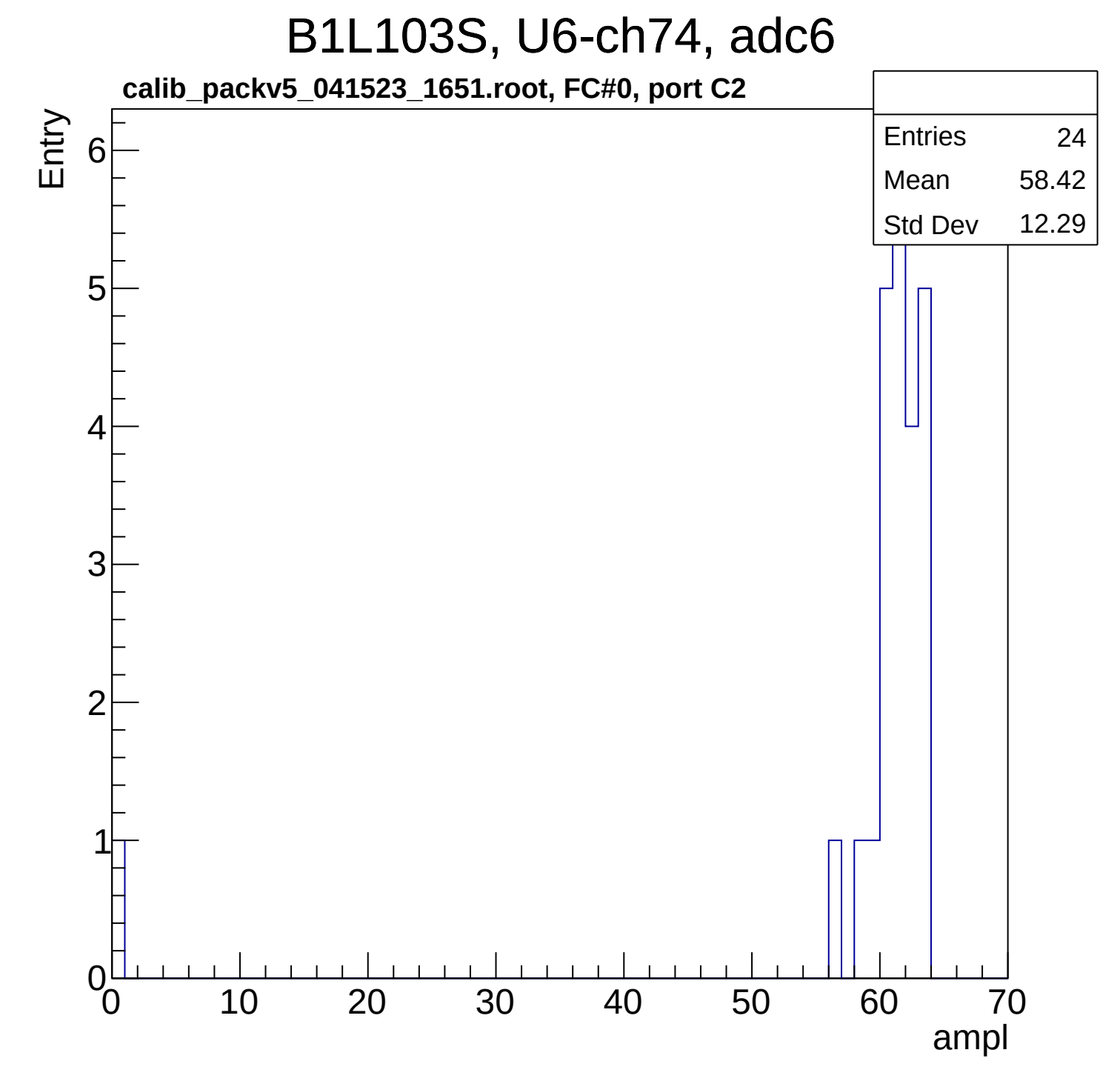
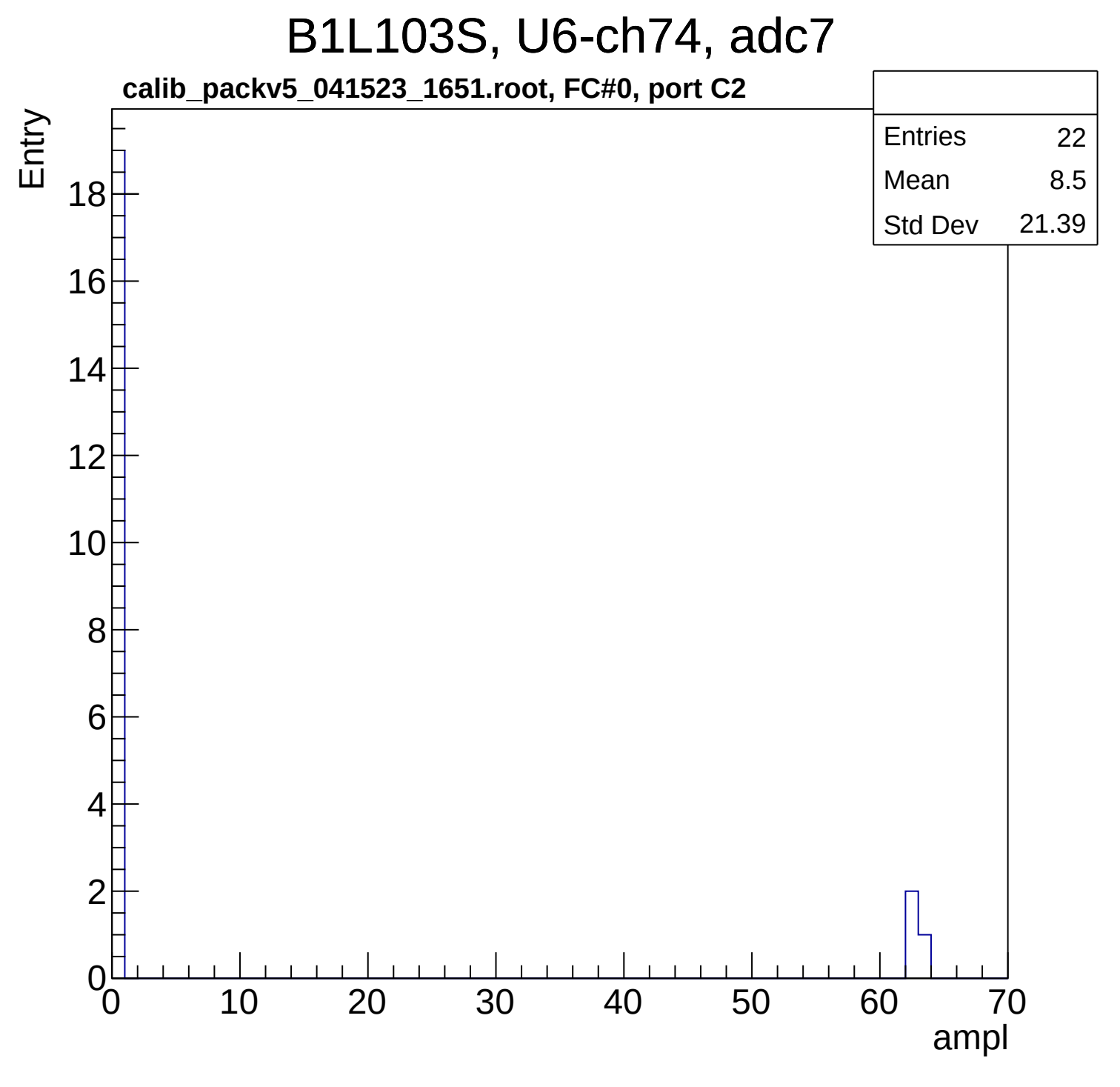
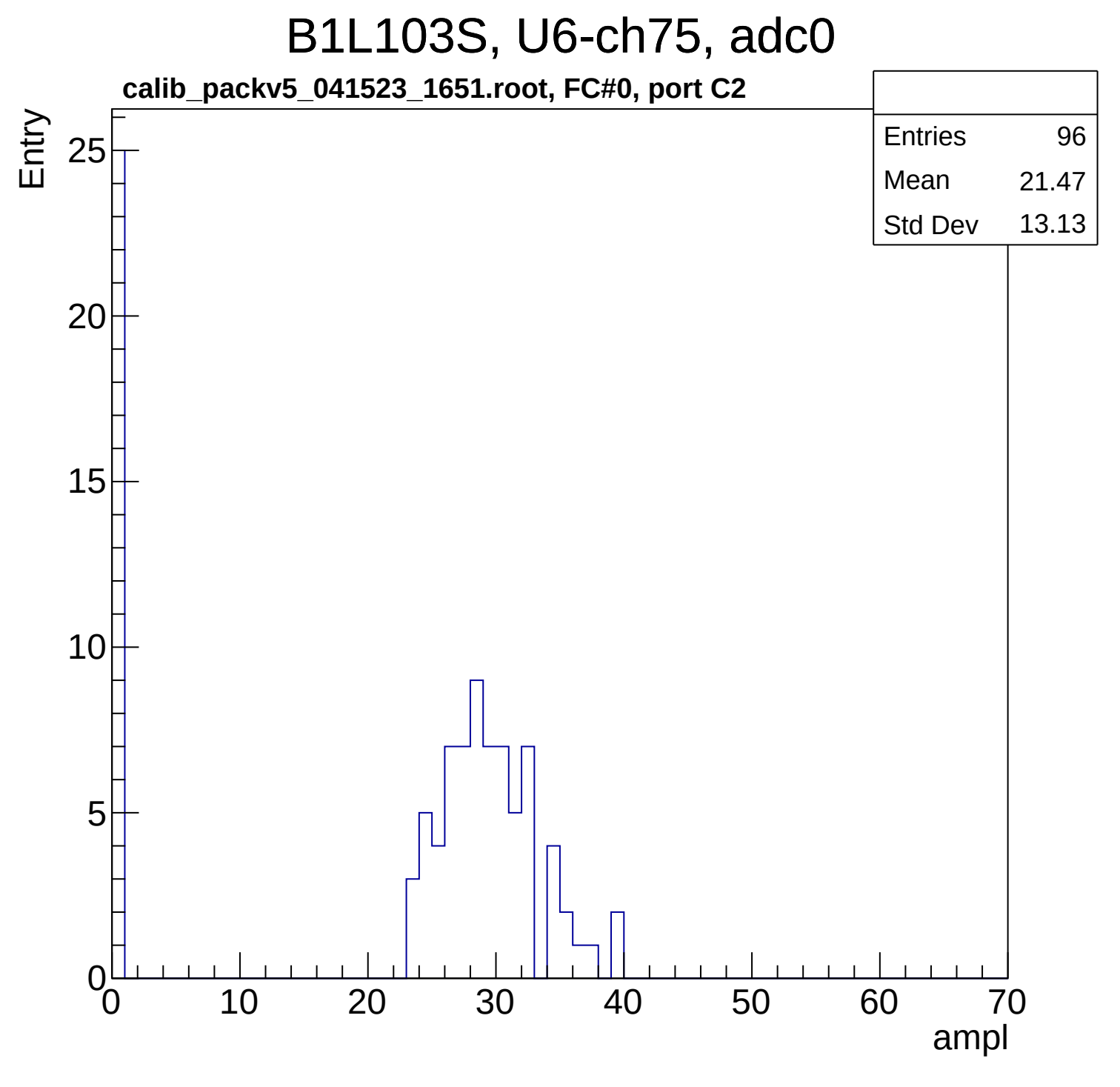
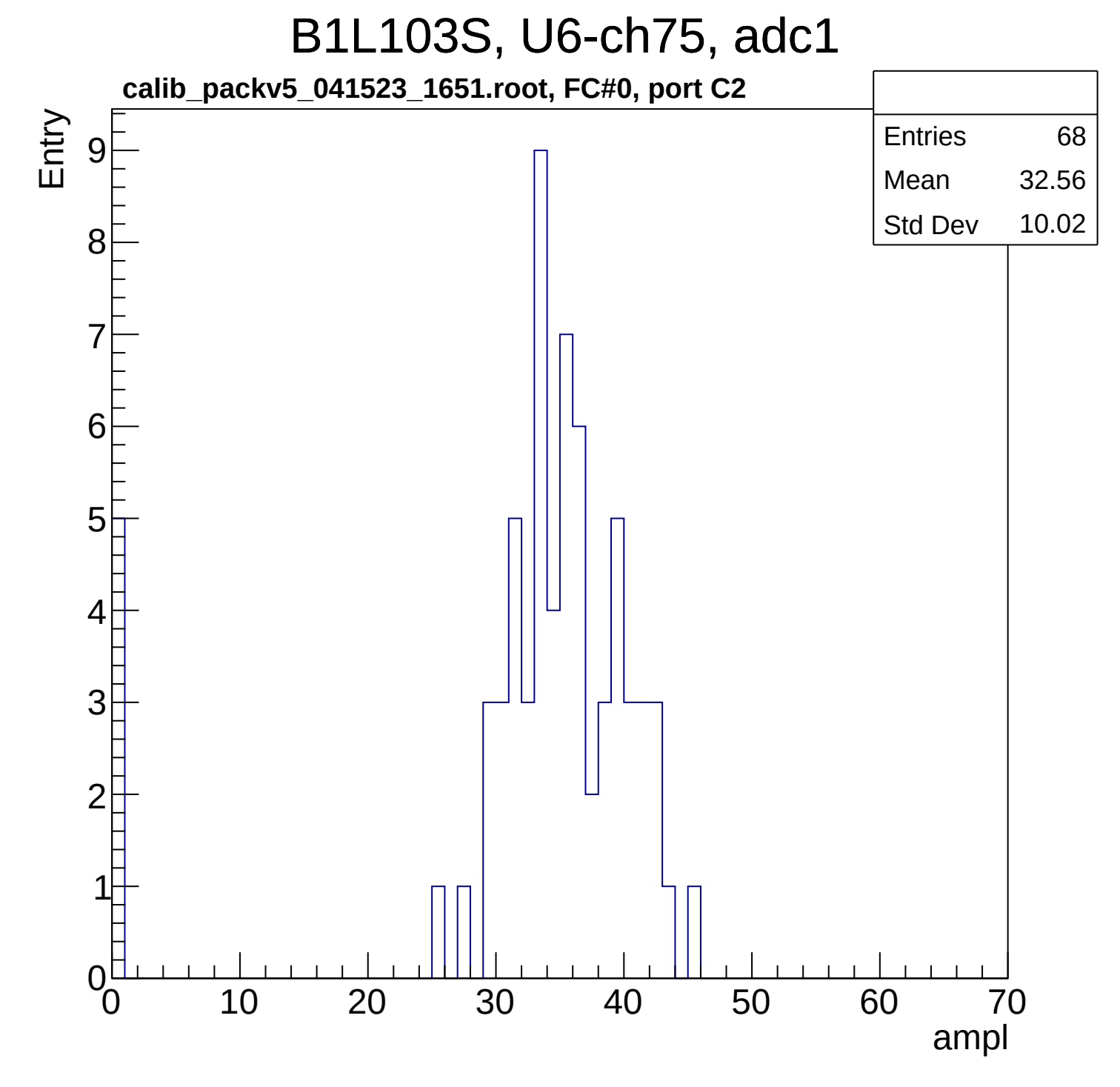

B1L103S, U6-ch74, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 58.42
Std Dev 12.29
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch74, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.5
Std Dev 21.39
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch75, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 96
Mean 21.47
Std Dev 13.13
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch75, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 32.56
Std Dev 10.02
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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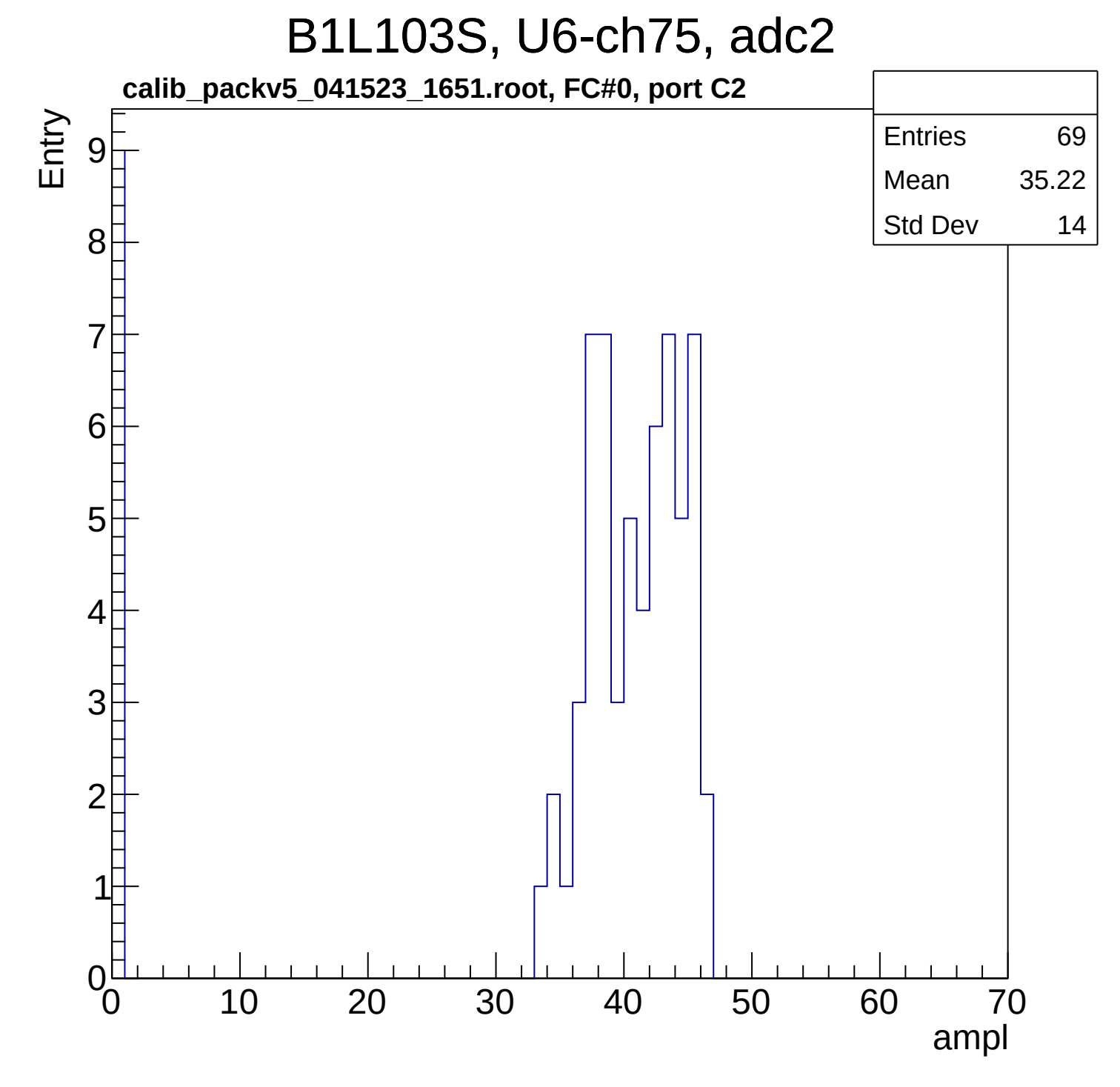
B1L103S, U6-ch75, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 35.22
Std Dev 14
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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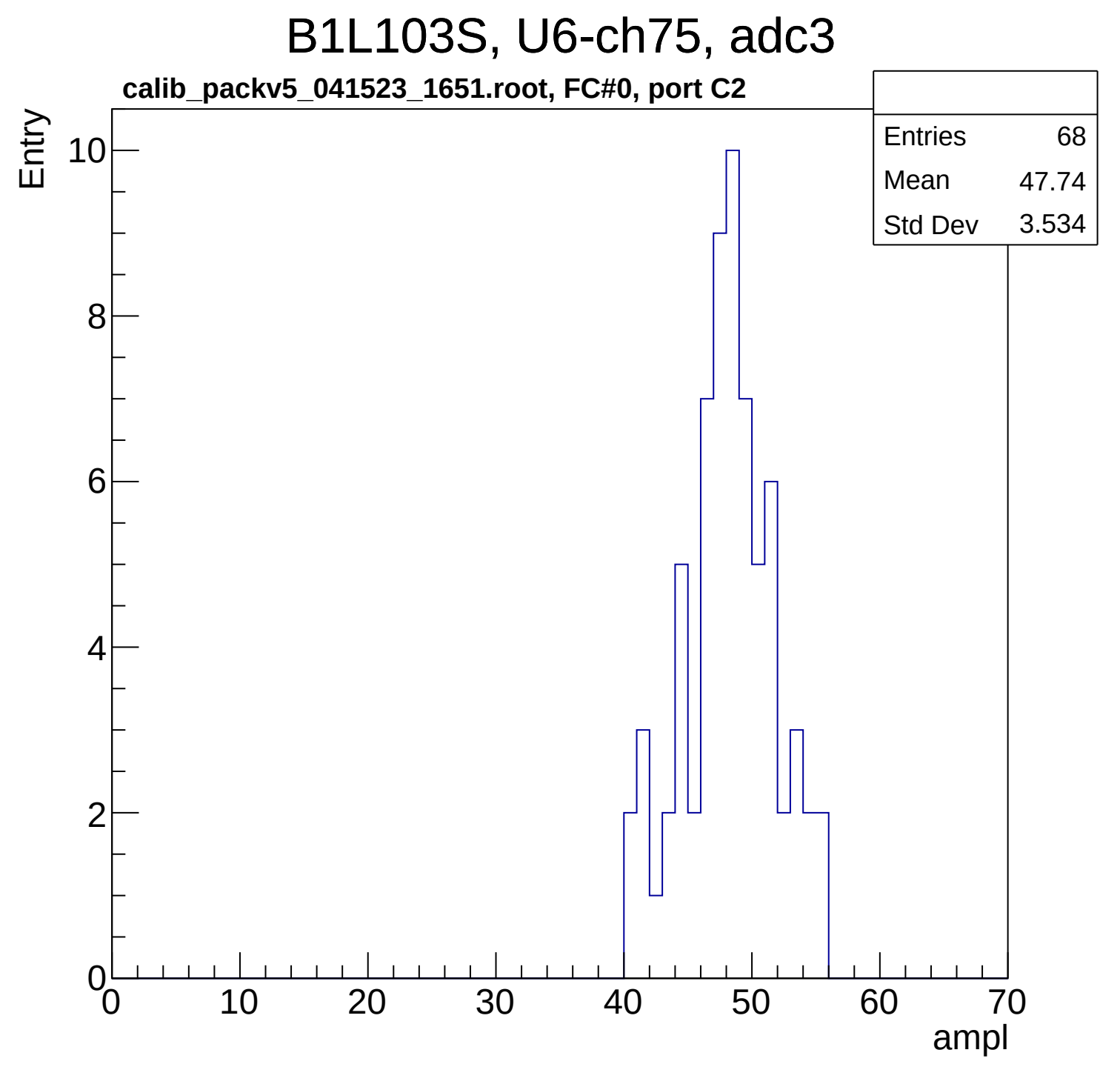
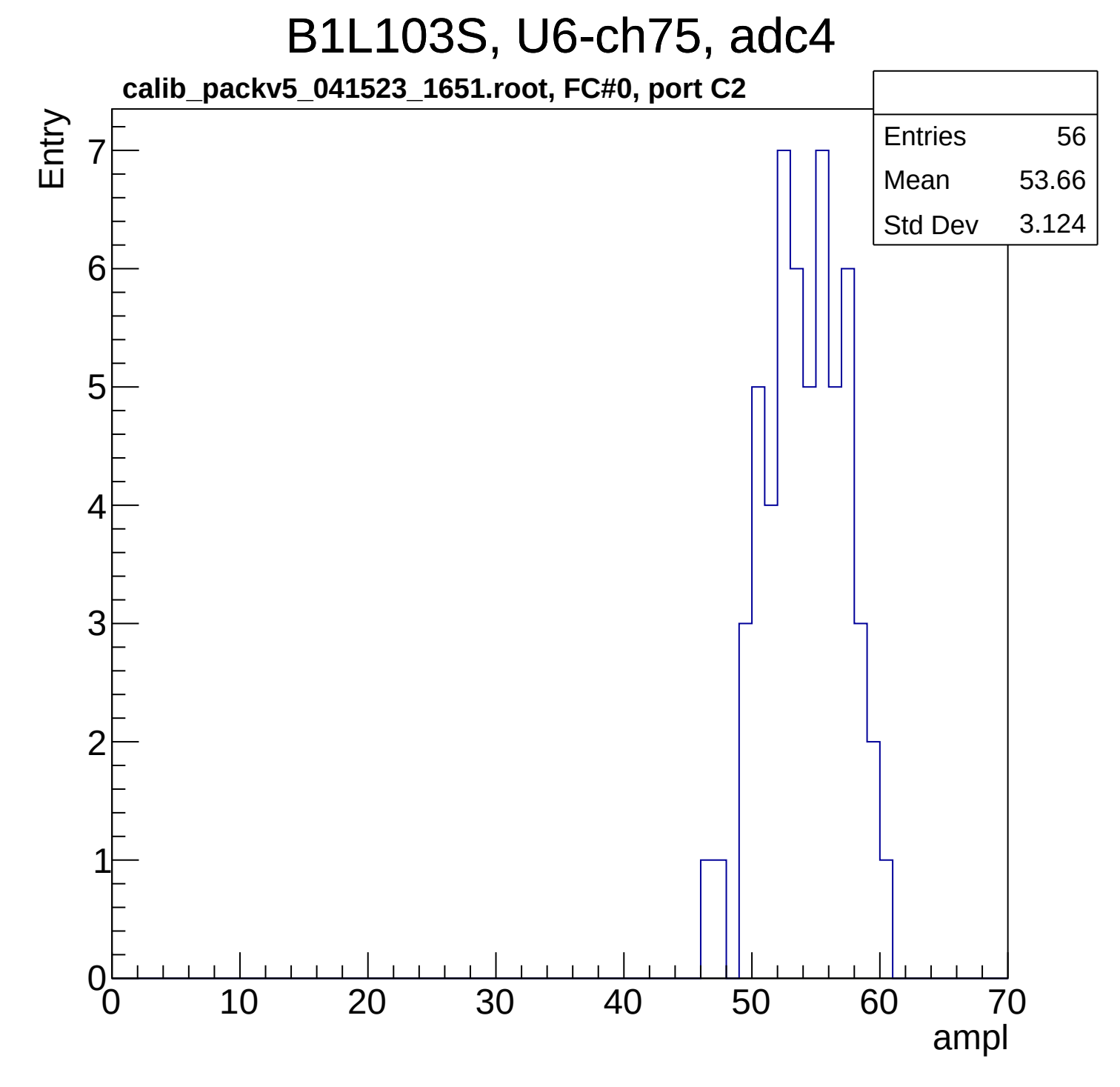
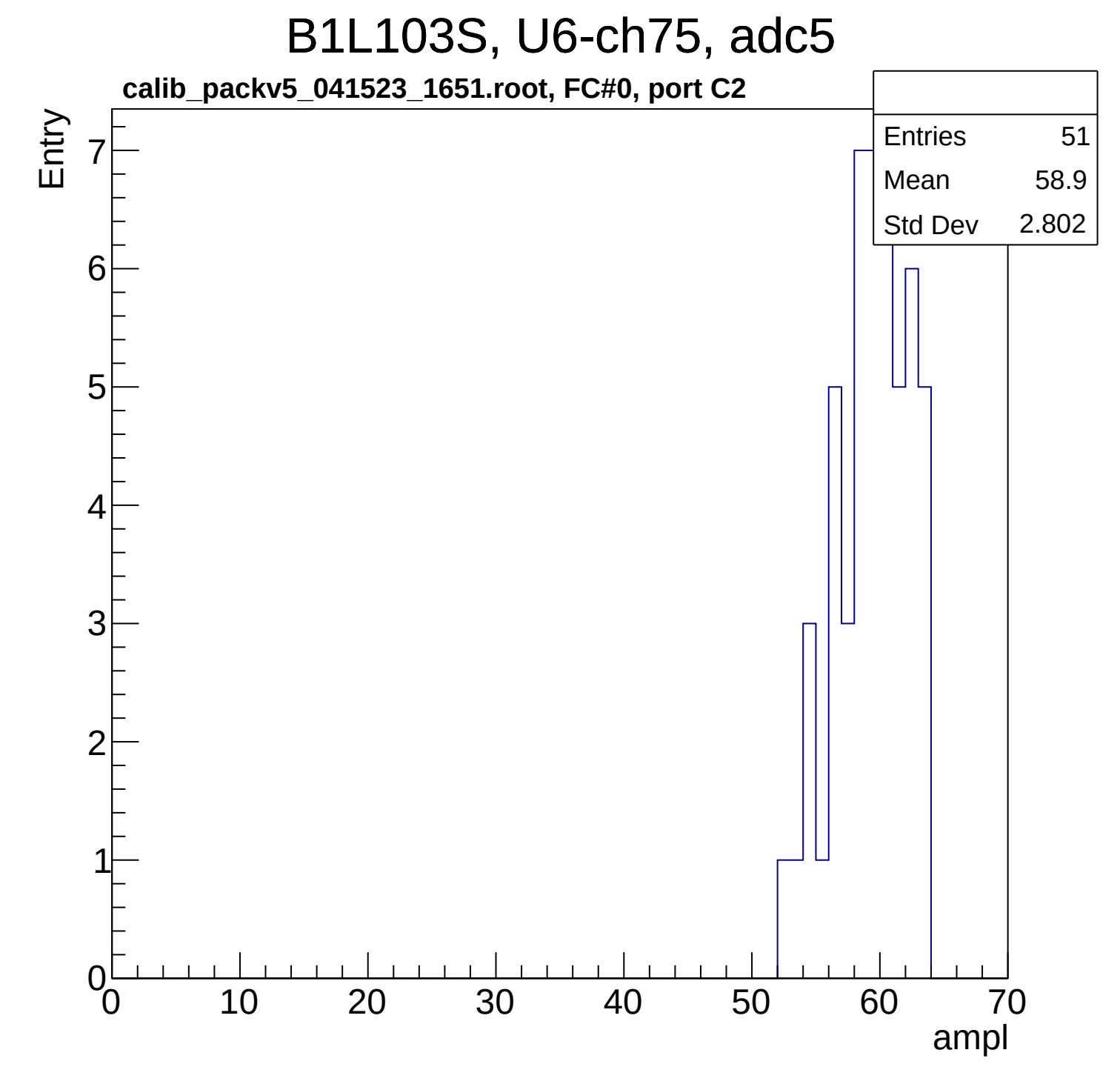

B1L103S, U6-ch75, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 47.74
Std Dev 3.534
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U6-ch75, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 53.66
Std Dev 3.124
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U6-ch75, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 58.9
Std Dev 2.802
Entry
ampl
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2
3
4
5
6
7
0
10
20
30
40
50
60
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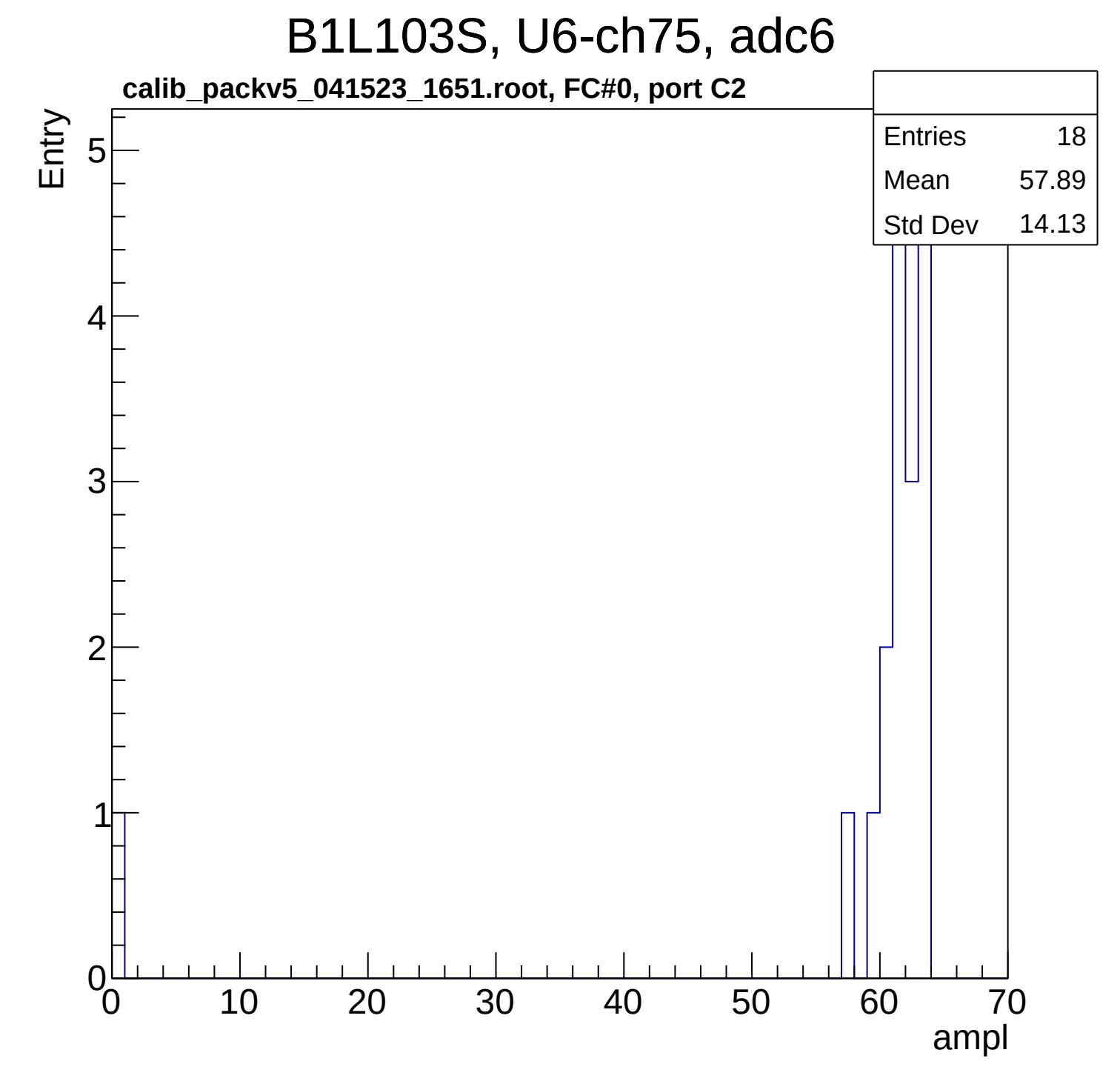
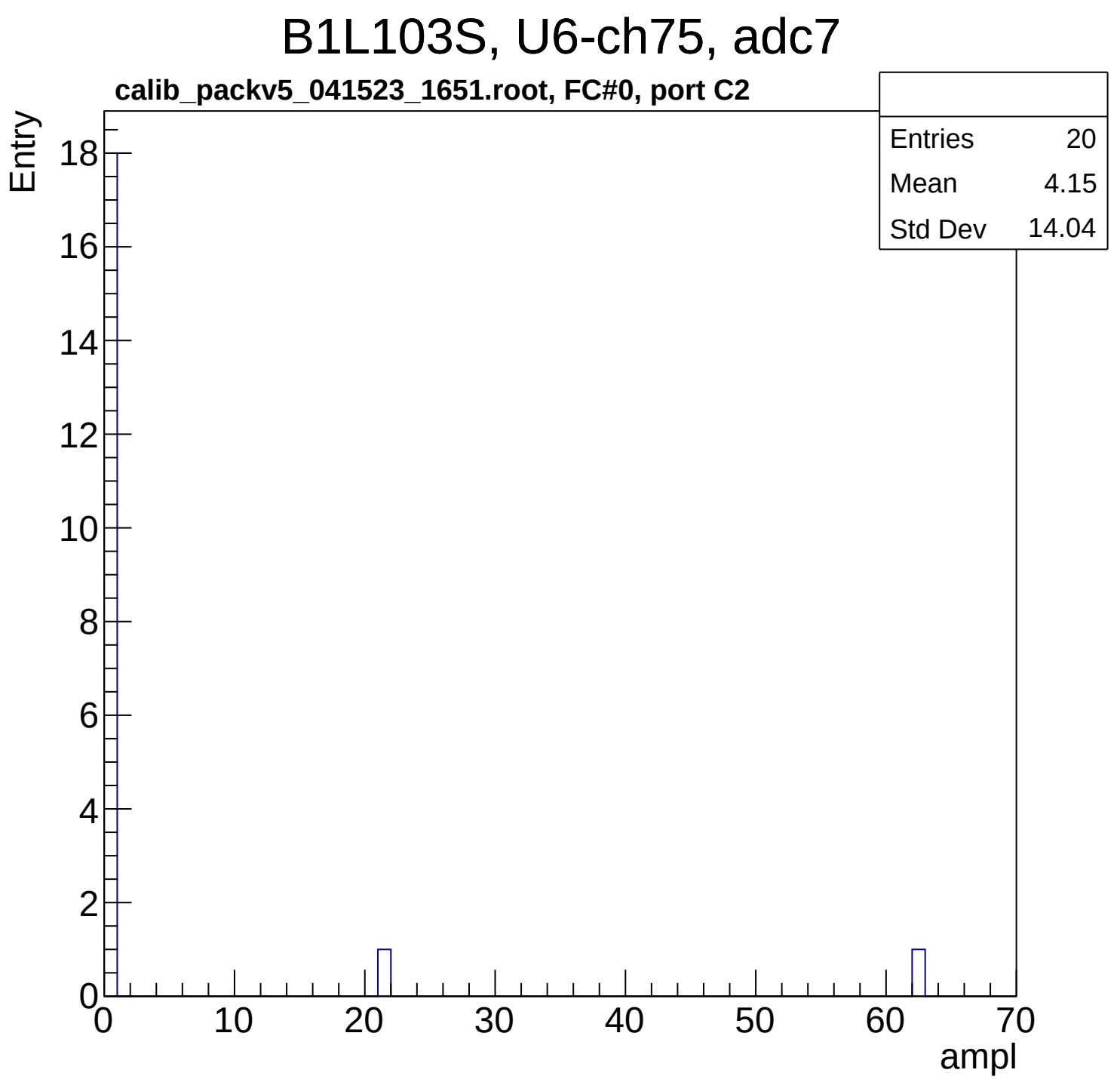

B1L103S, U6-ch75, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 57.89
Std Dev 14.13
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch75, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4.15
Std Dev 14.04
Entry
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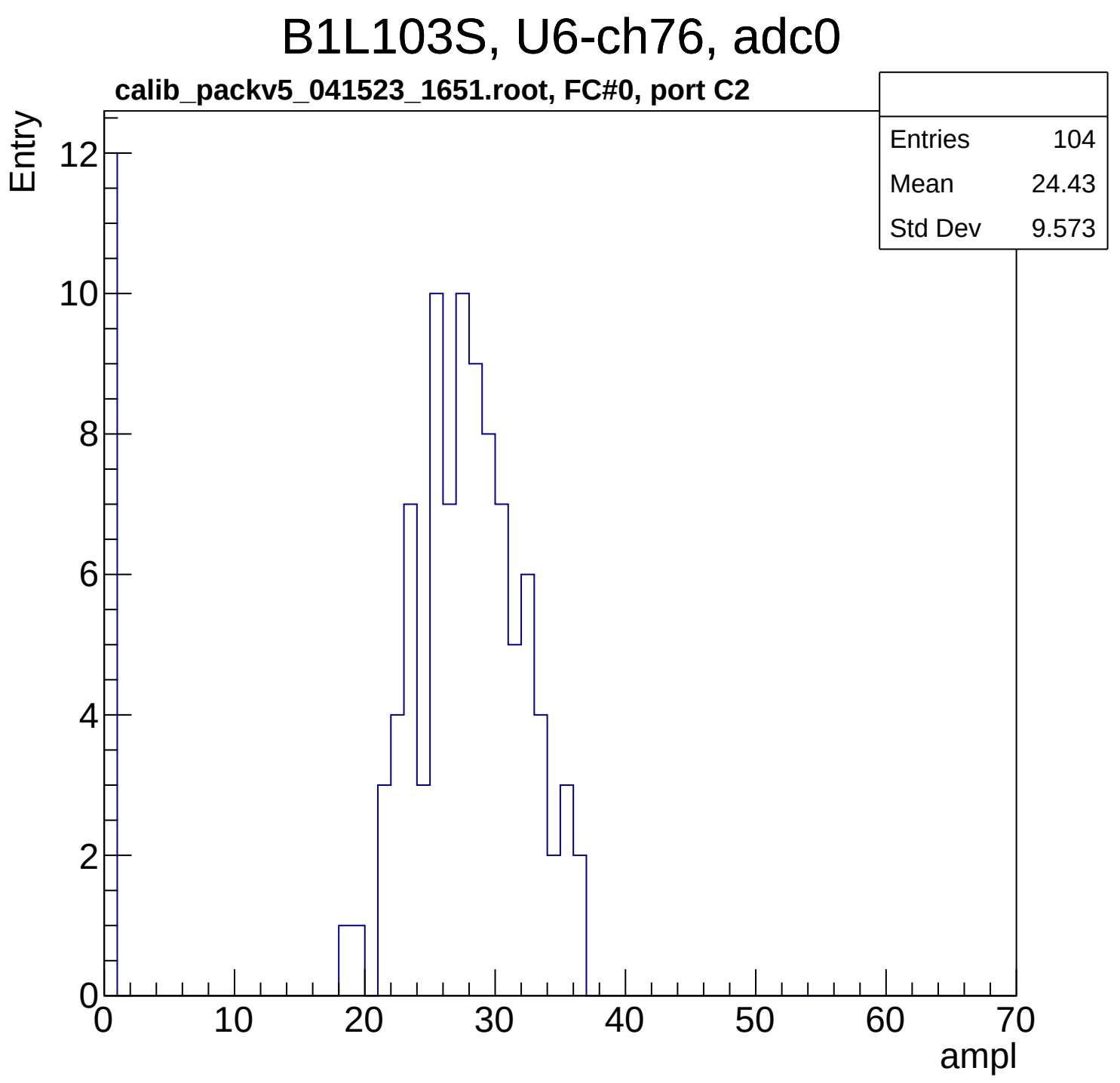
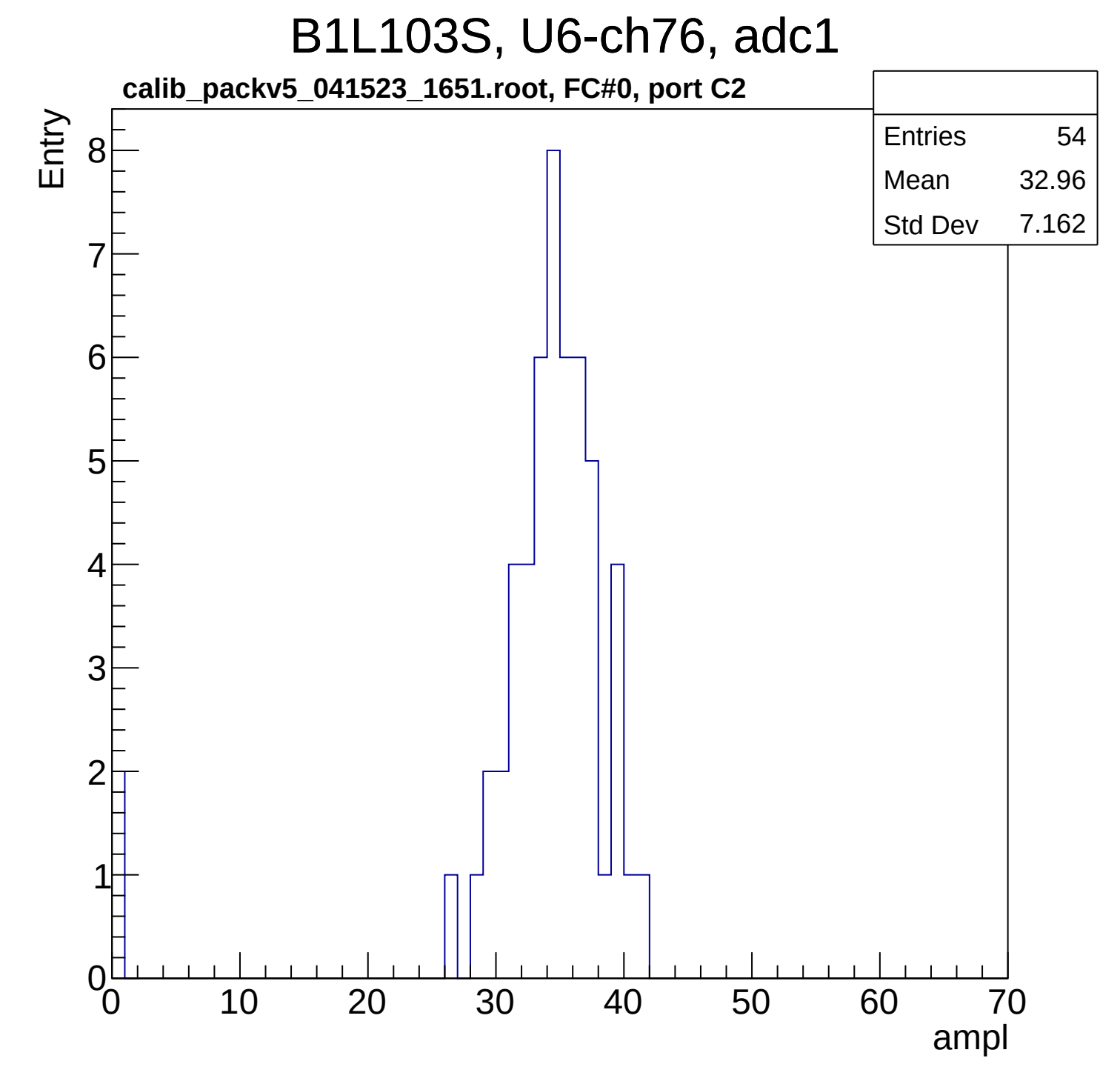
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch76, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 104
Mean 24.43
Std Dev 9.573
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch76, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 32.96
Std Dev 7.162
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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60
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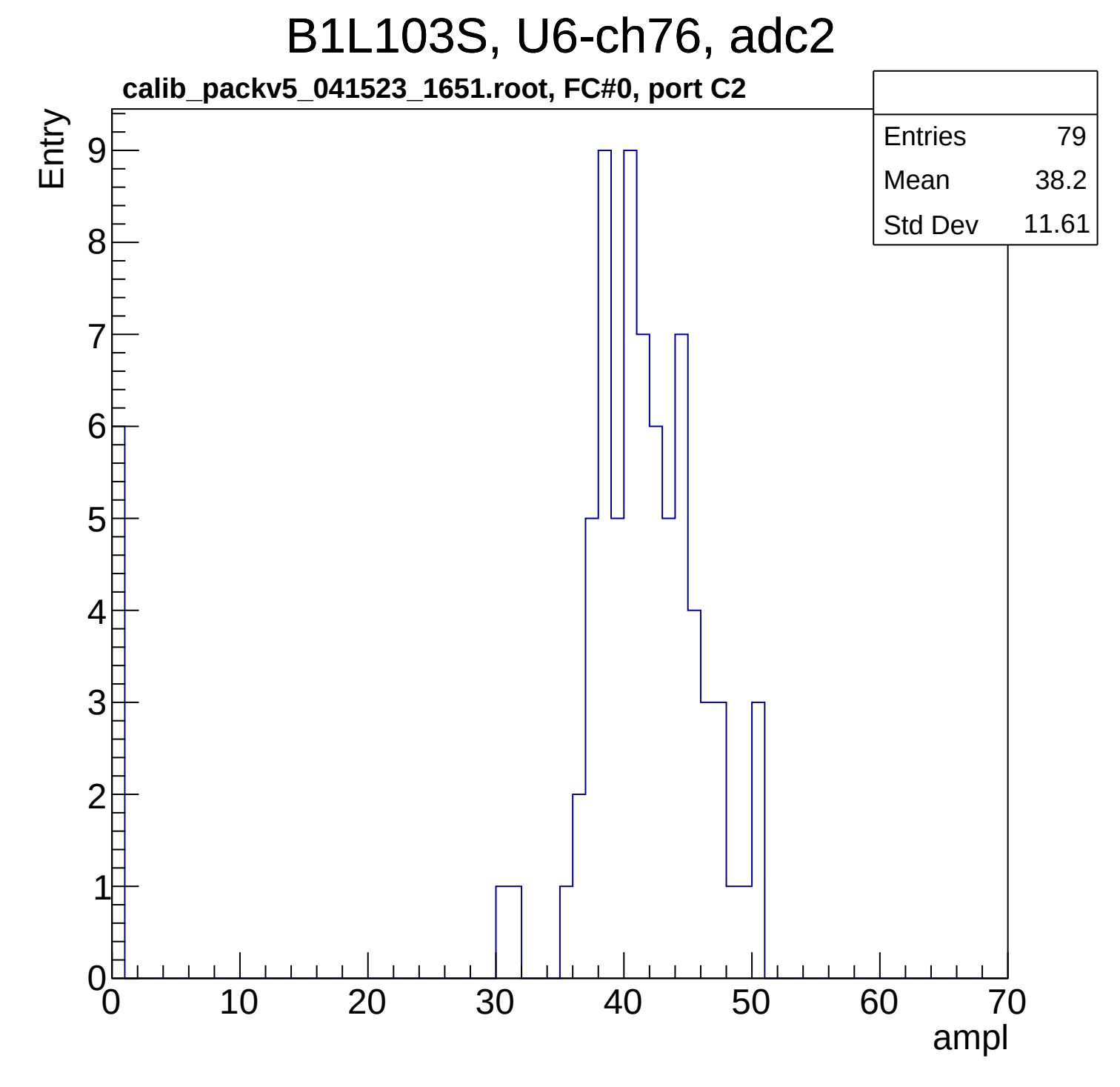
B1L103S, U6-ch76, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 38.2
Std Dev 11.61
Entry
ampl
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2
3
4
5
6
7
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0
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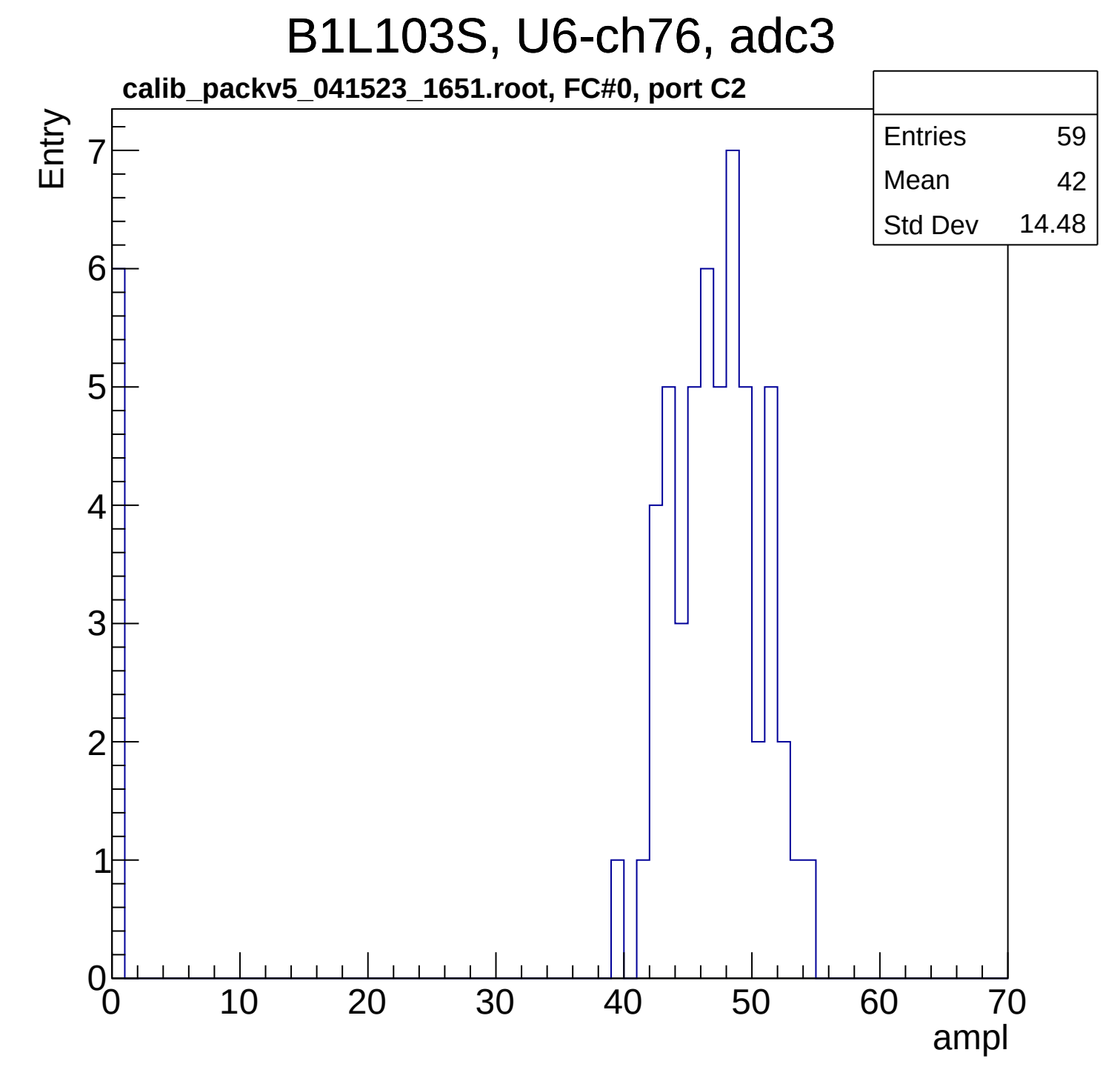
B1L103S, U6-ch76, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 42
Std Dev 14.48
Entry
ampl
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1
2
3
4
5
6
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0
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40
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60
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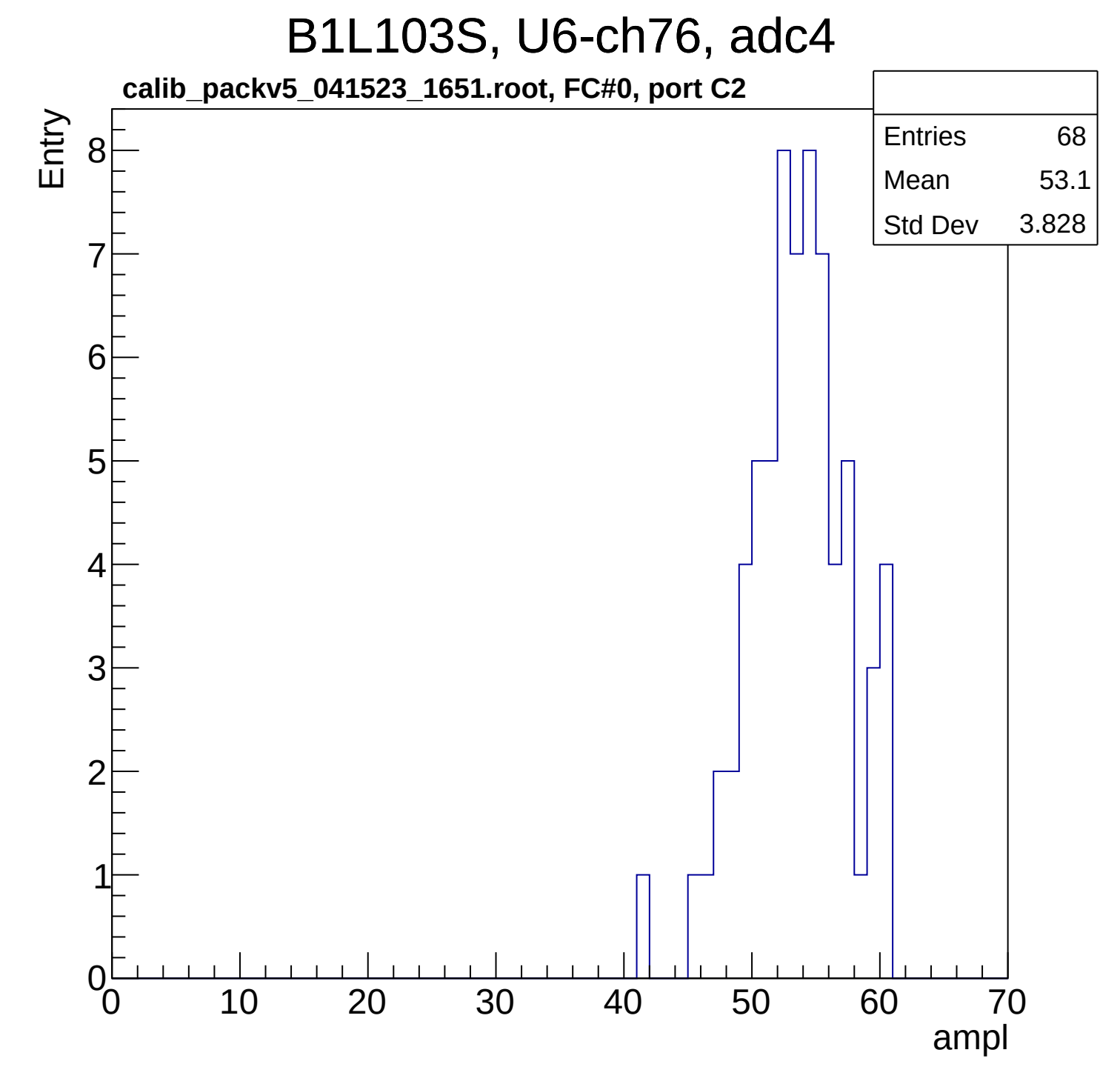
B1L103S, U6-ch76, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 53.1
Std Dev 3.828
Entry
ampl
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1
2
3
4
5
6
7
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0
10
20
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40
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60
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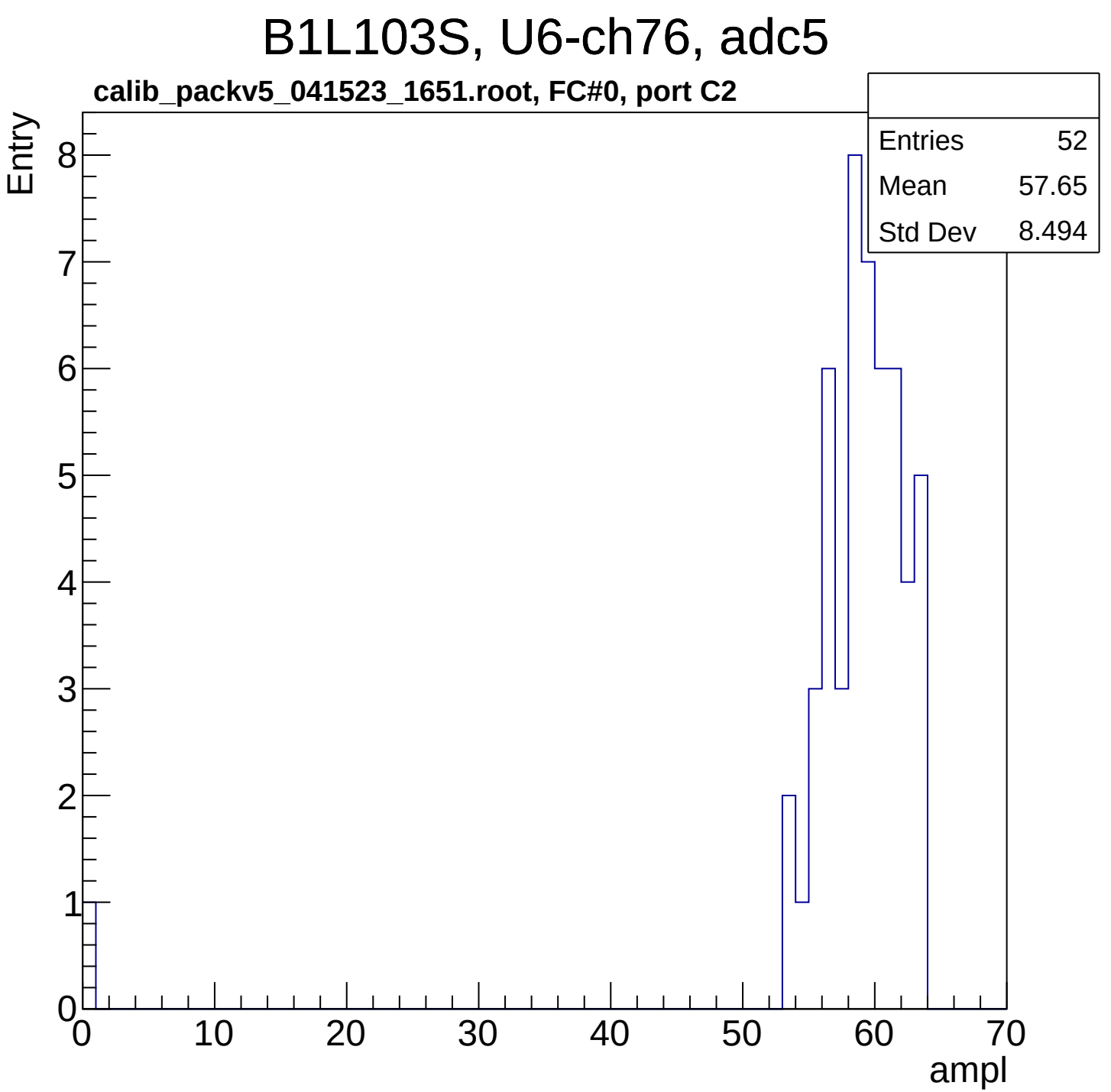
B1L103S, U6-ch76, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 57.65
Std Dev 8.494
Entry
ampl
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2
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4
5
6
7
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0
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60
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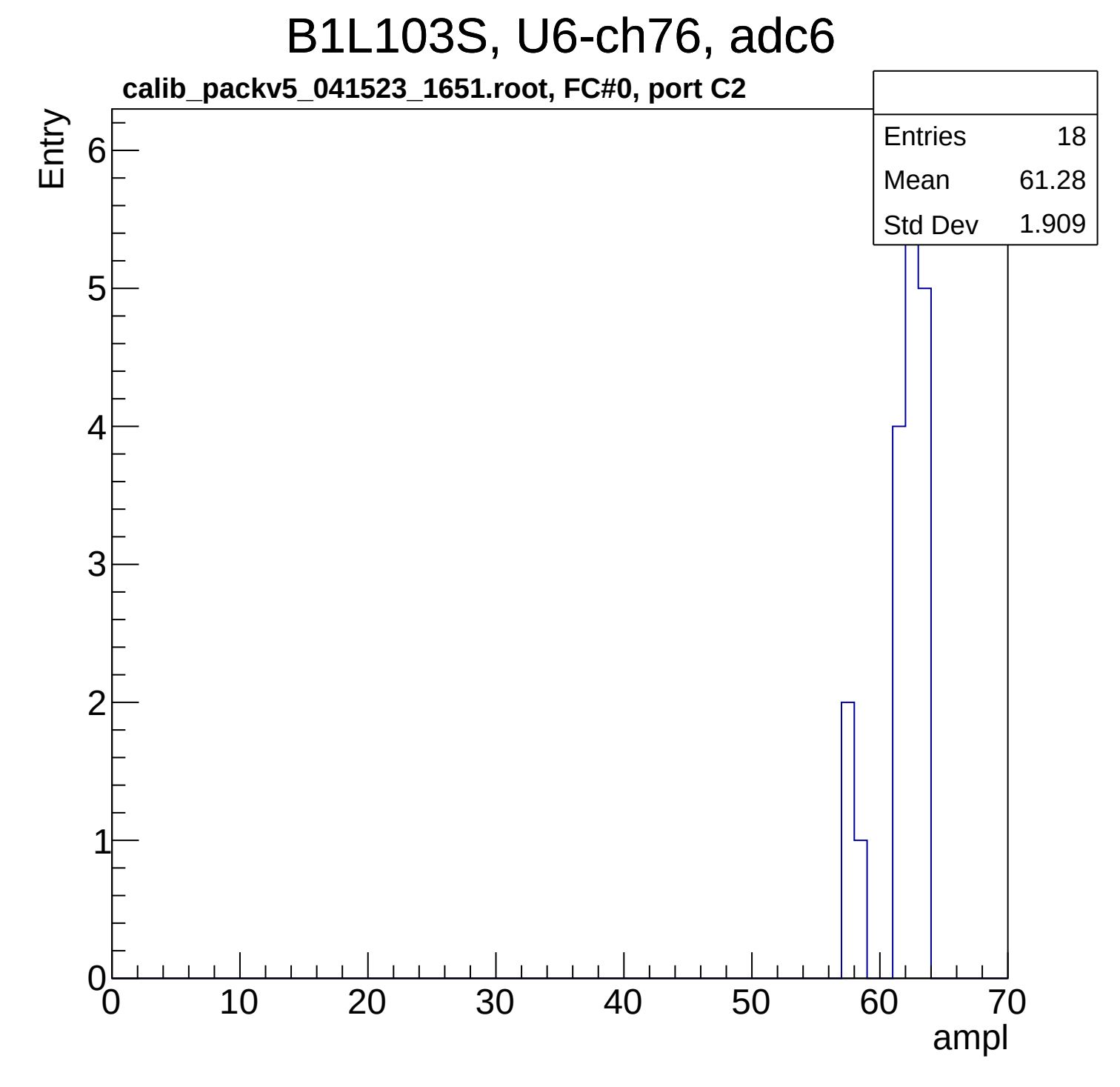
B1L103S, U6-ch76, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 61.28
Std Dev 1.909
Entry
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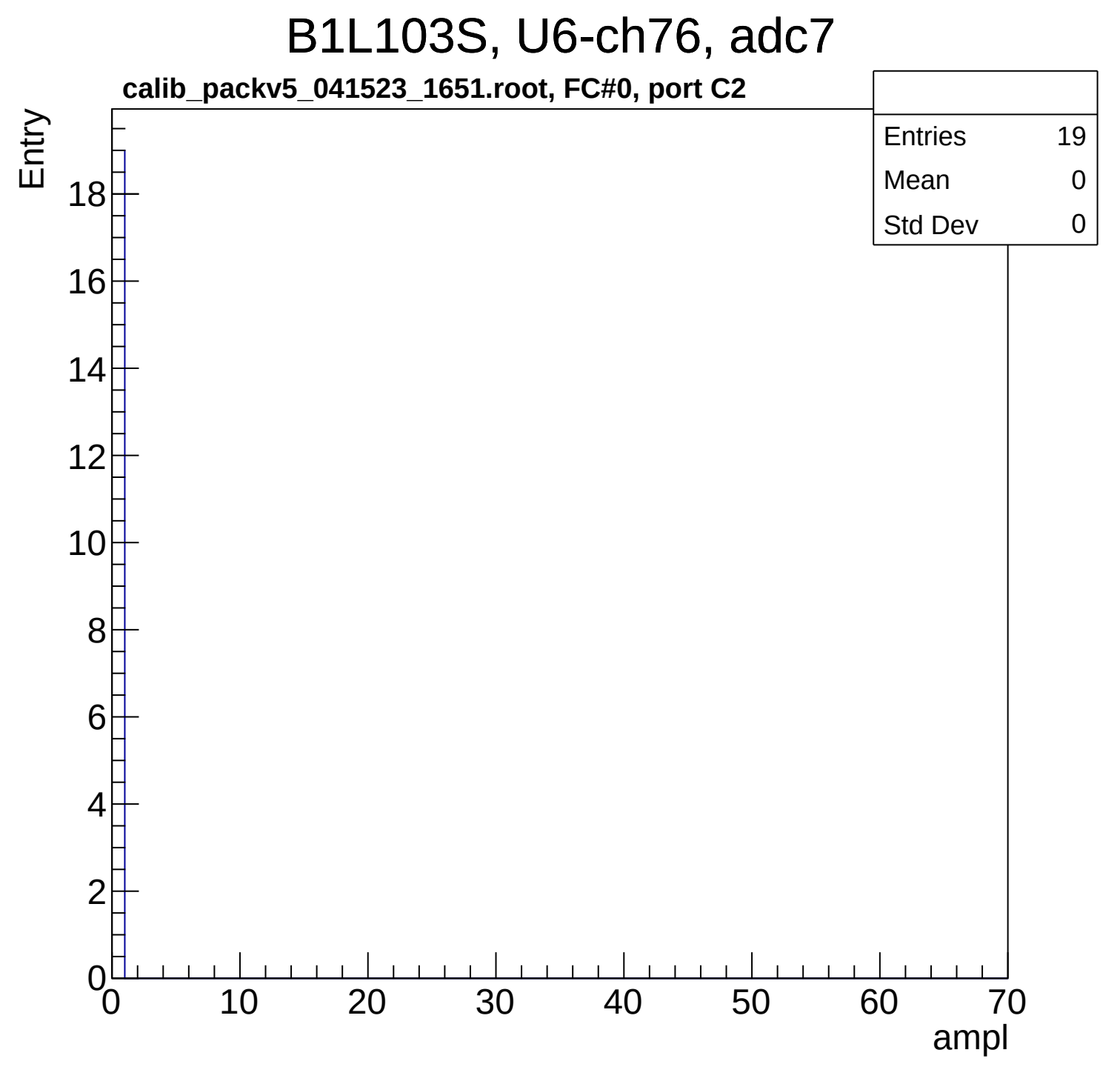
70
ampl


B1L103S, U6-ch76, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
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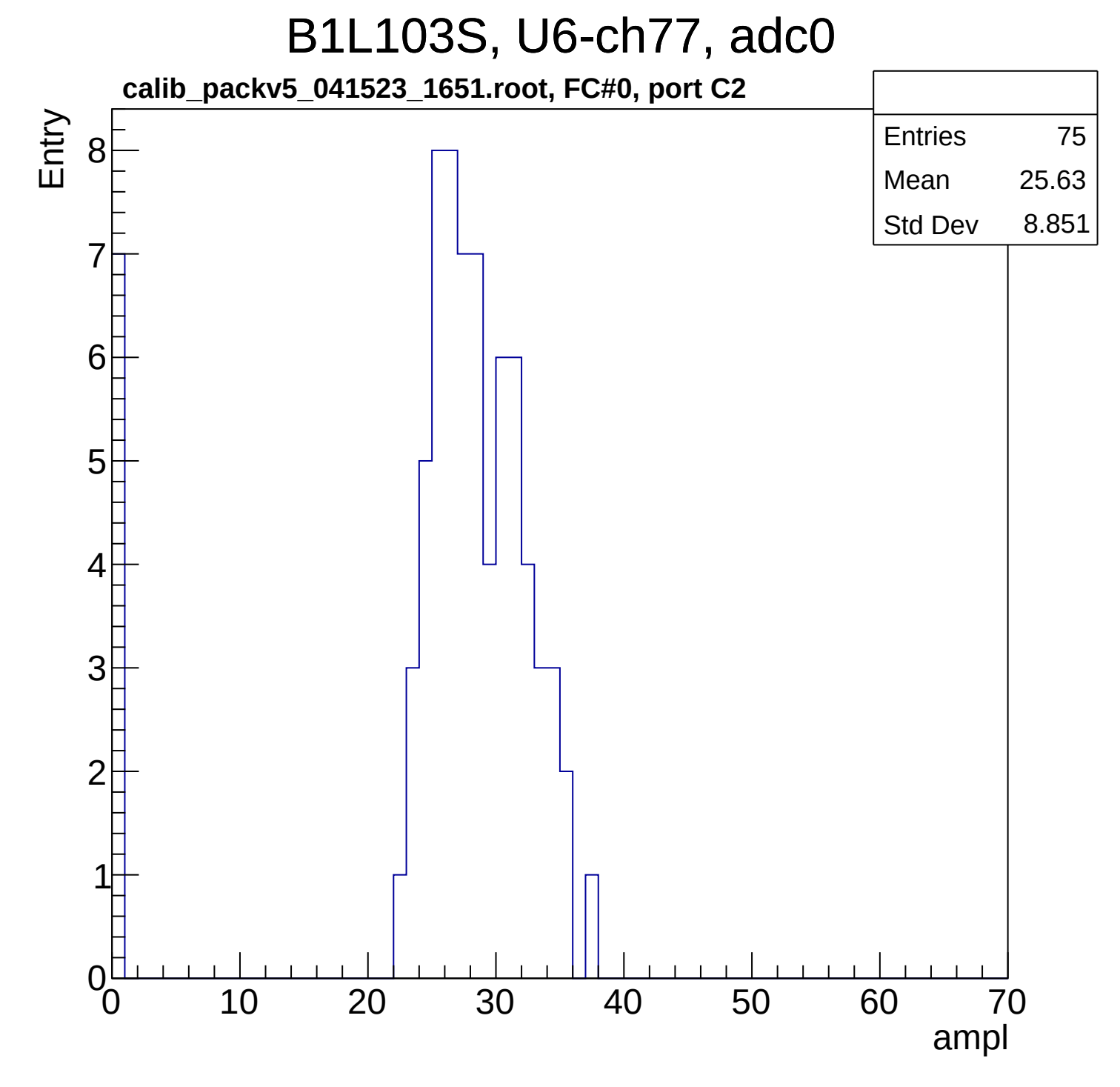
50
60
70
ampl


B1L103S, U6-ch77, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 25.63
Std Dev 8.851
Entry
ampl
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2
3
4
5
6
7
8
0
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60
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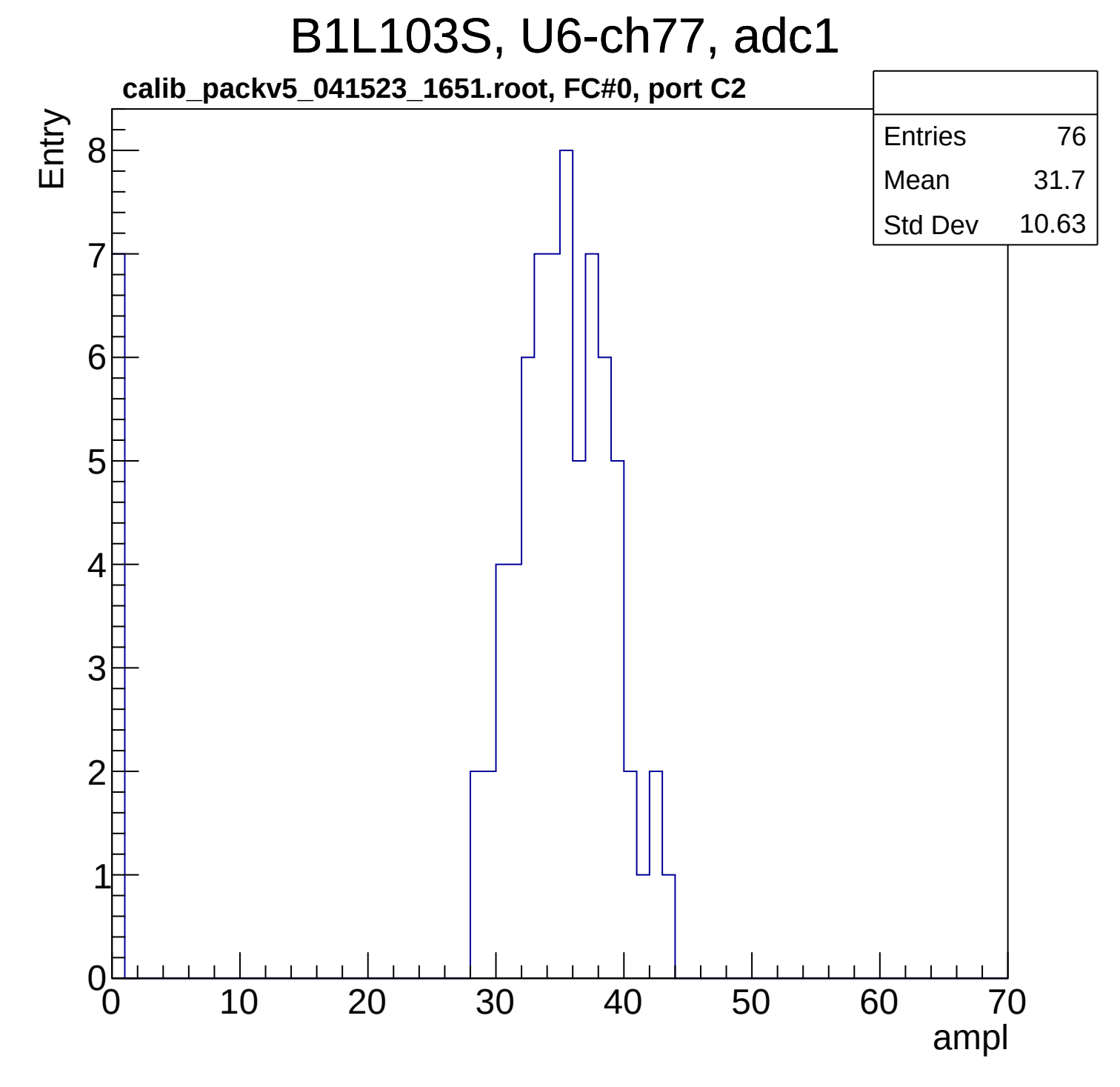
B1L103S, U6-ch77, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 31.7
Std Dev 10.63
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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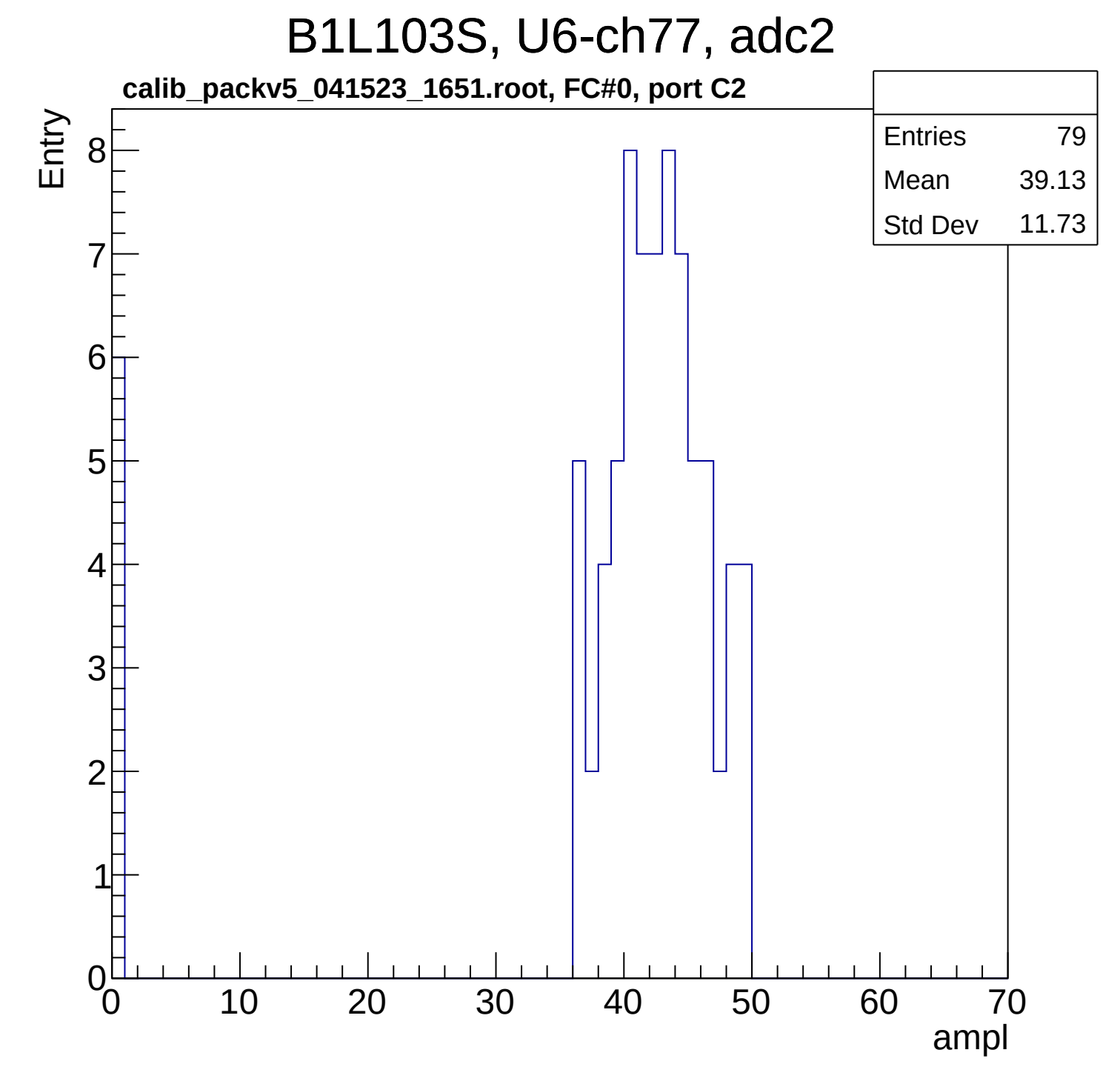
60
70


B1L103S, U6-ch77, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 39.13
Std Dev 11.73
Entry
ampl
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2
3
4
5
6
7
8
0
10
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60
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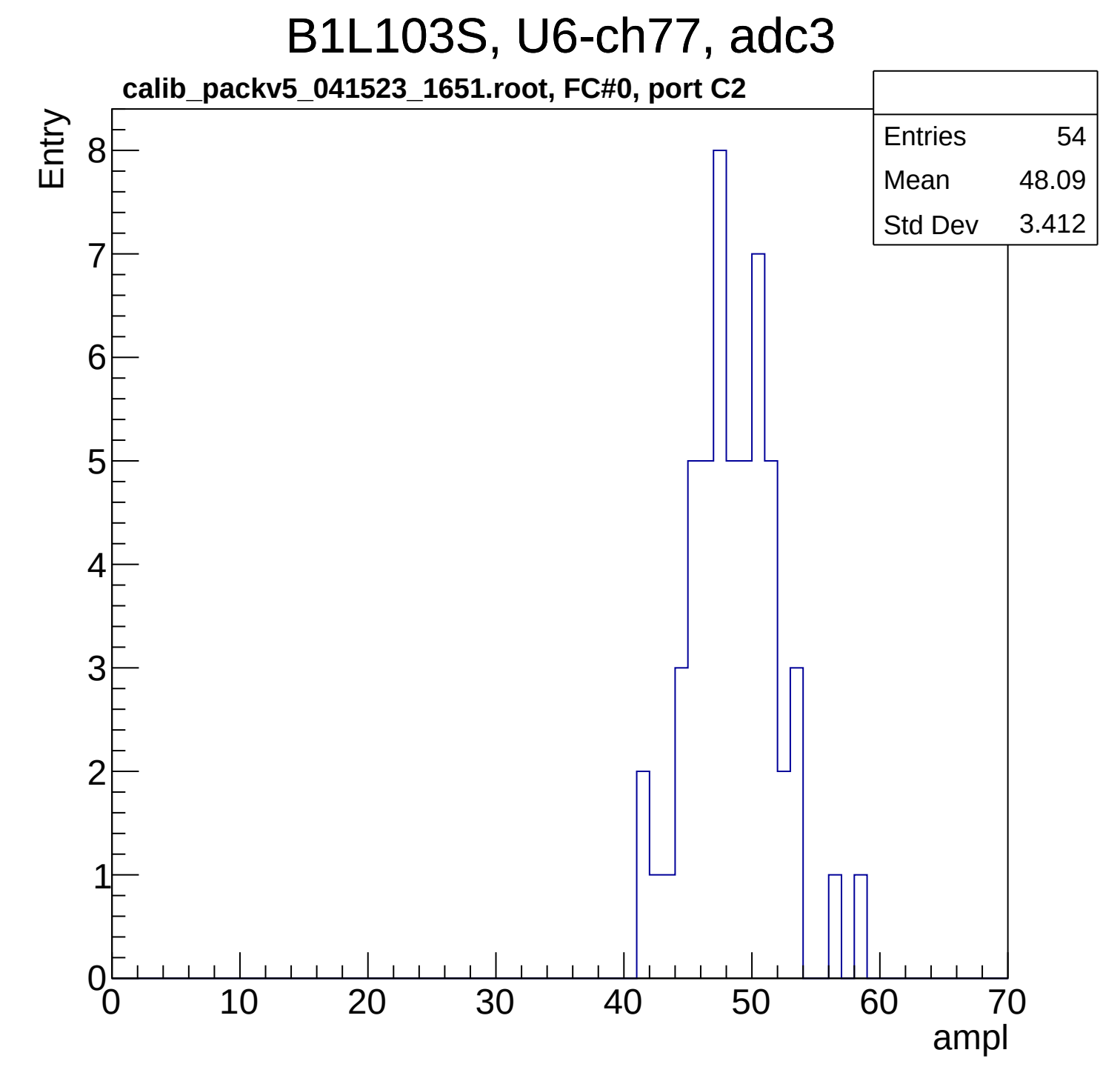
B1L103S, U6-ch77, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 48.09
Std Dev 3.412
Entry
ampl
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2
3
4
5
6
7
8
0
10
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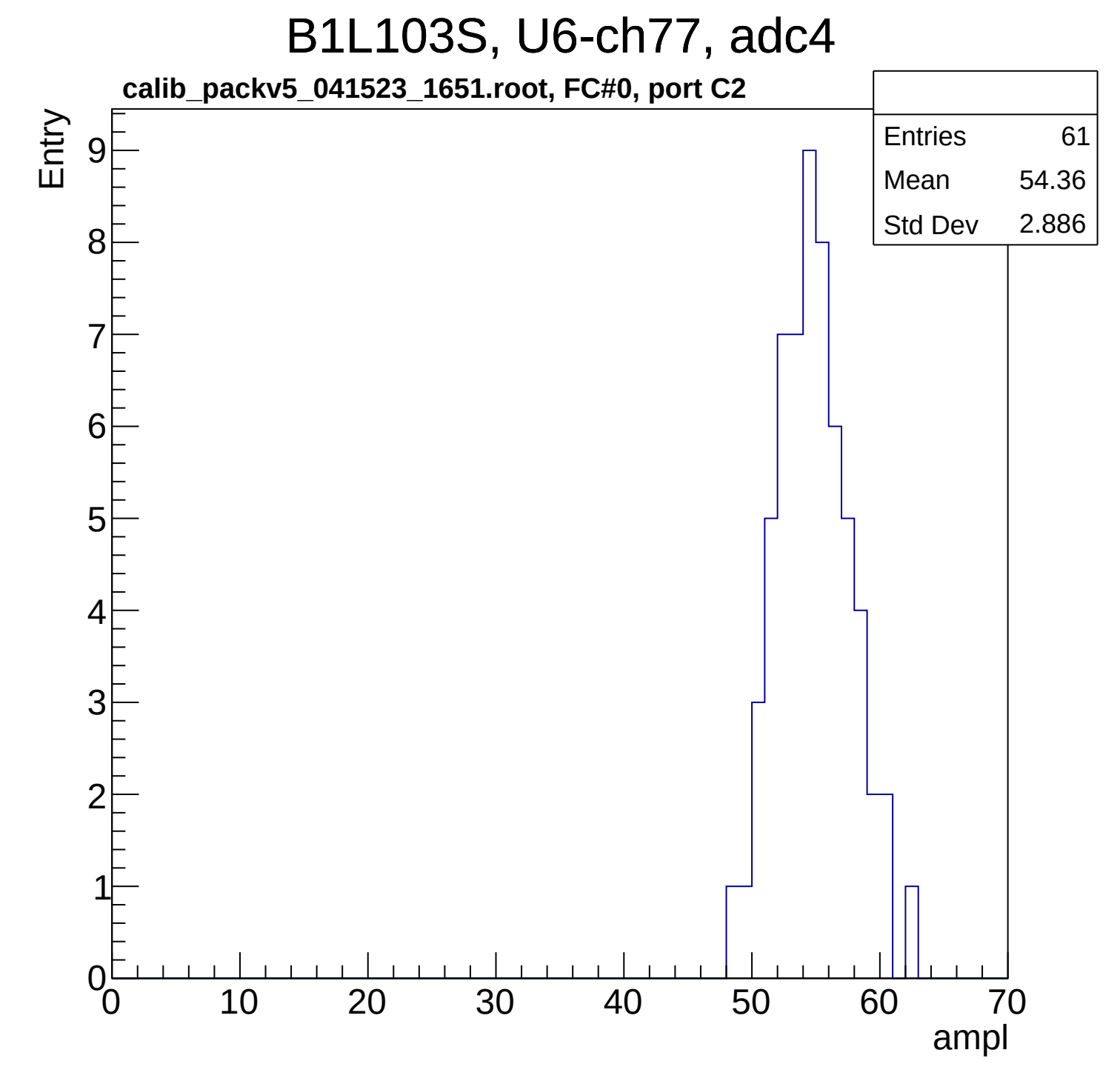
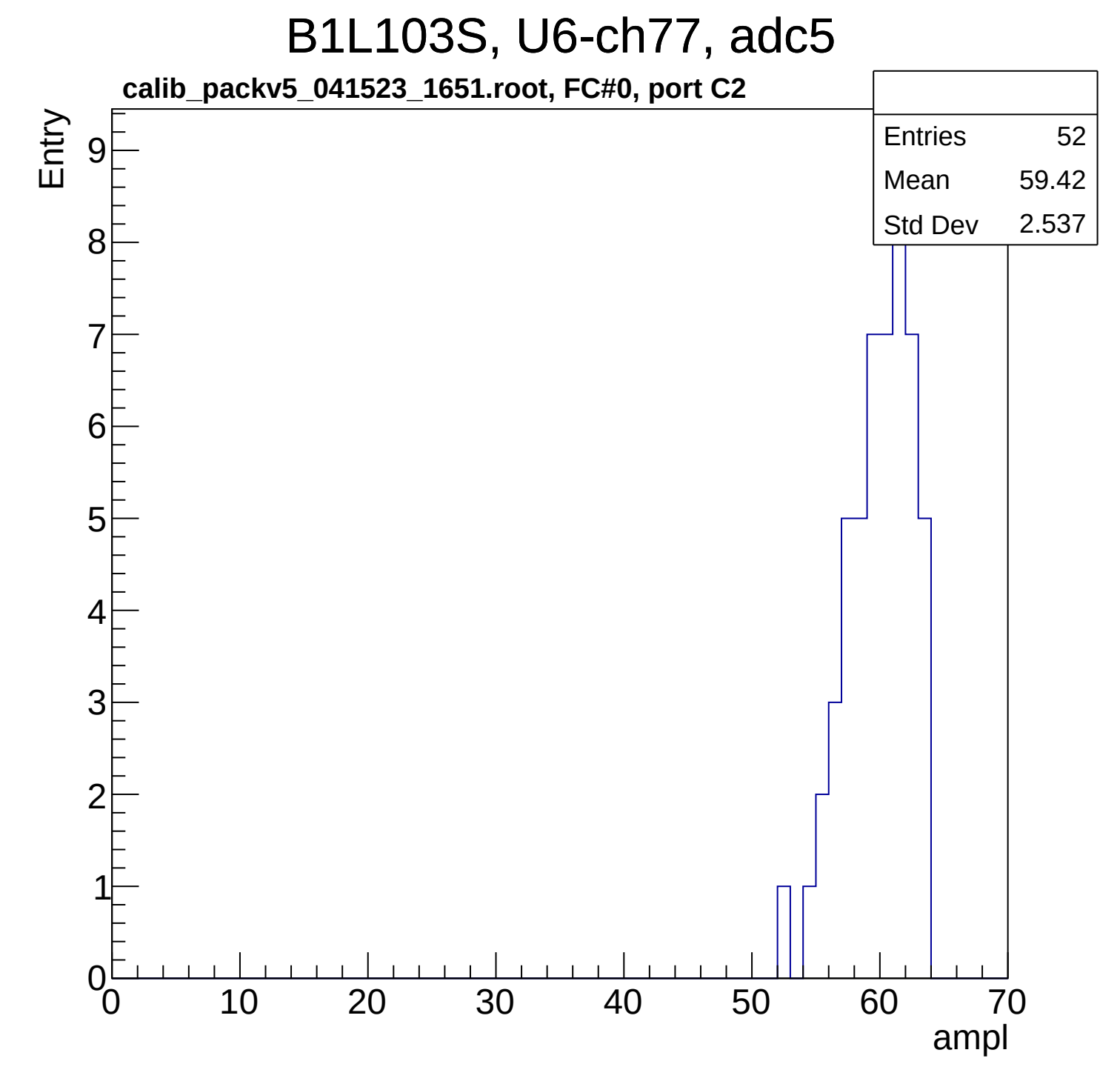
60
70


B1L103S, U6-ch77, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 54.36
Std Dev 2.886
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch77, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 59.42
Std Dev 2.537
Entry
ampl
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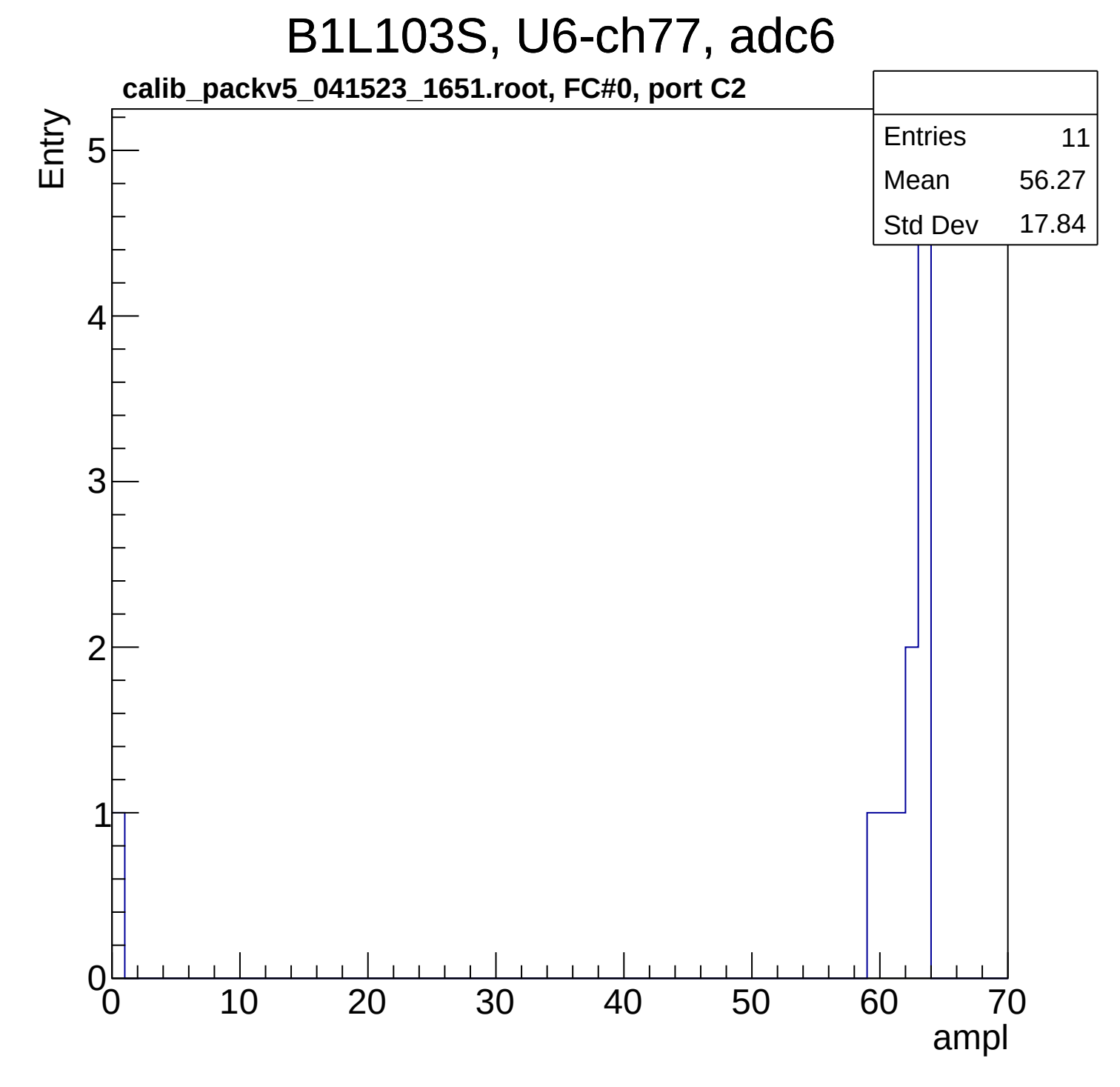
B1L103S, U6-ch77, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 56.27
Std Dev 17.84
Entry
0
1
2
3
4
5
0
10
20
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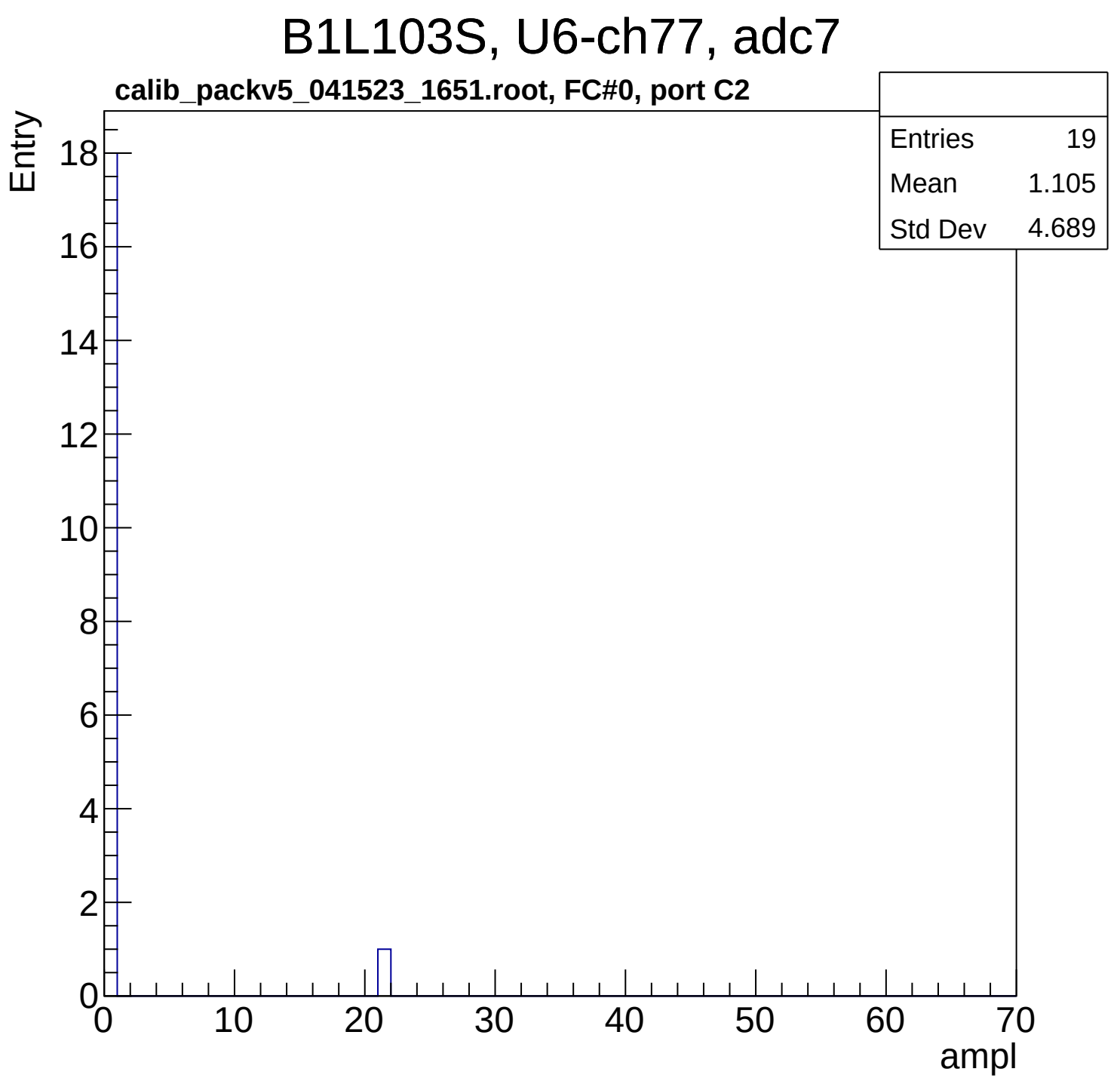
50
60
70
ampl


B1L103S, U6-ch77, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.105
Std Dev 4.689
Entry
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8
10
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14
16
18
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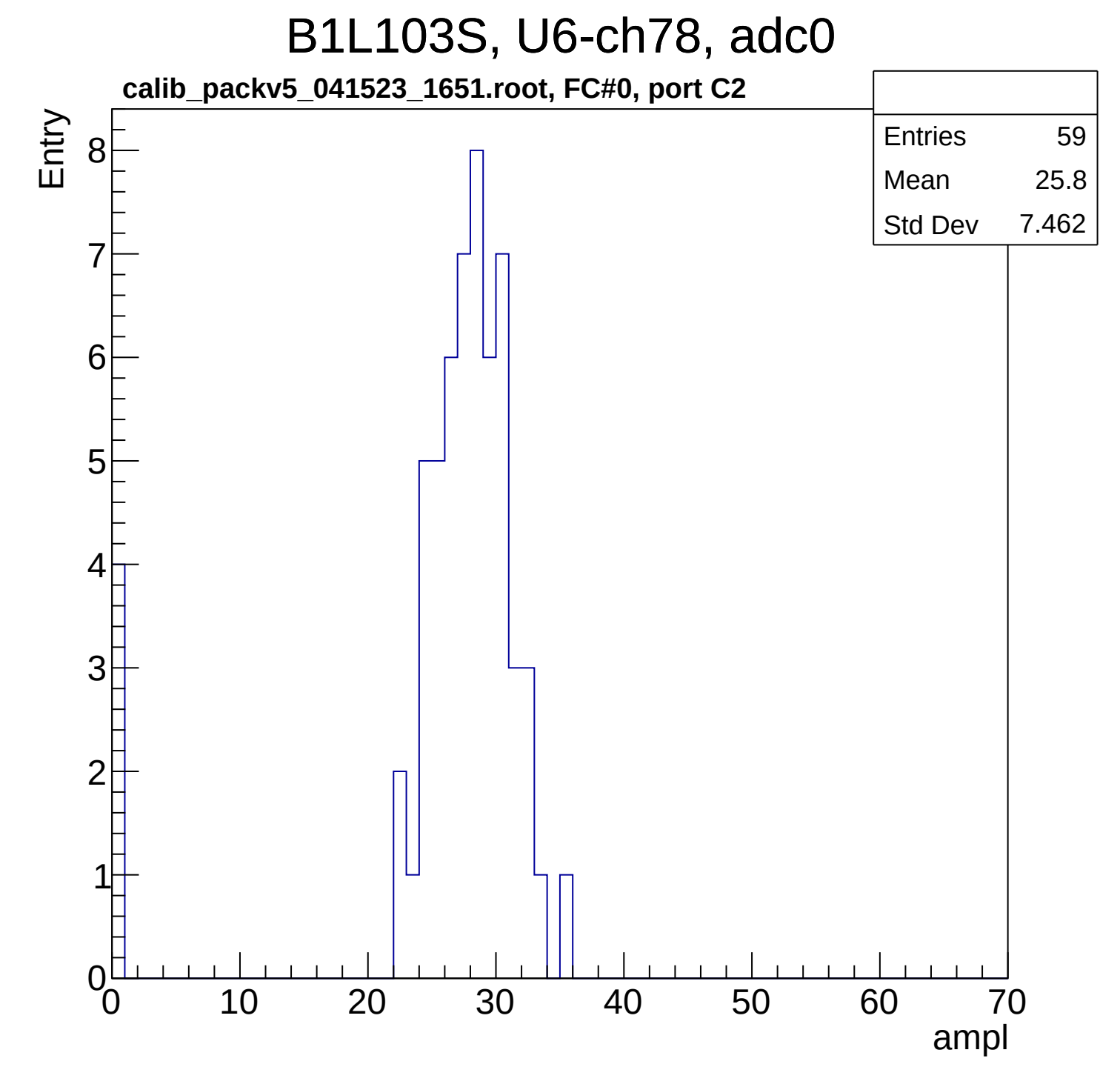
ampl


B1L103S, U6-ch78, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 25.8
Std Dev 7.462
Entry
ampl
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2
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4
5
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0
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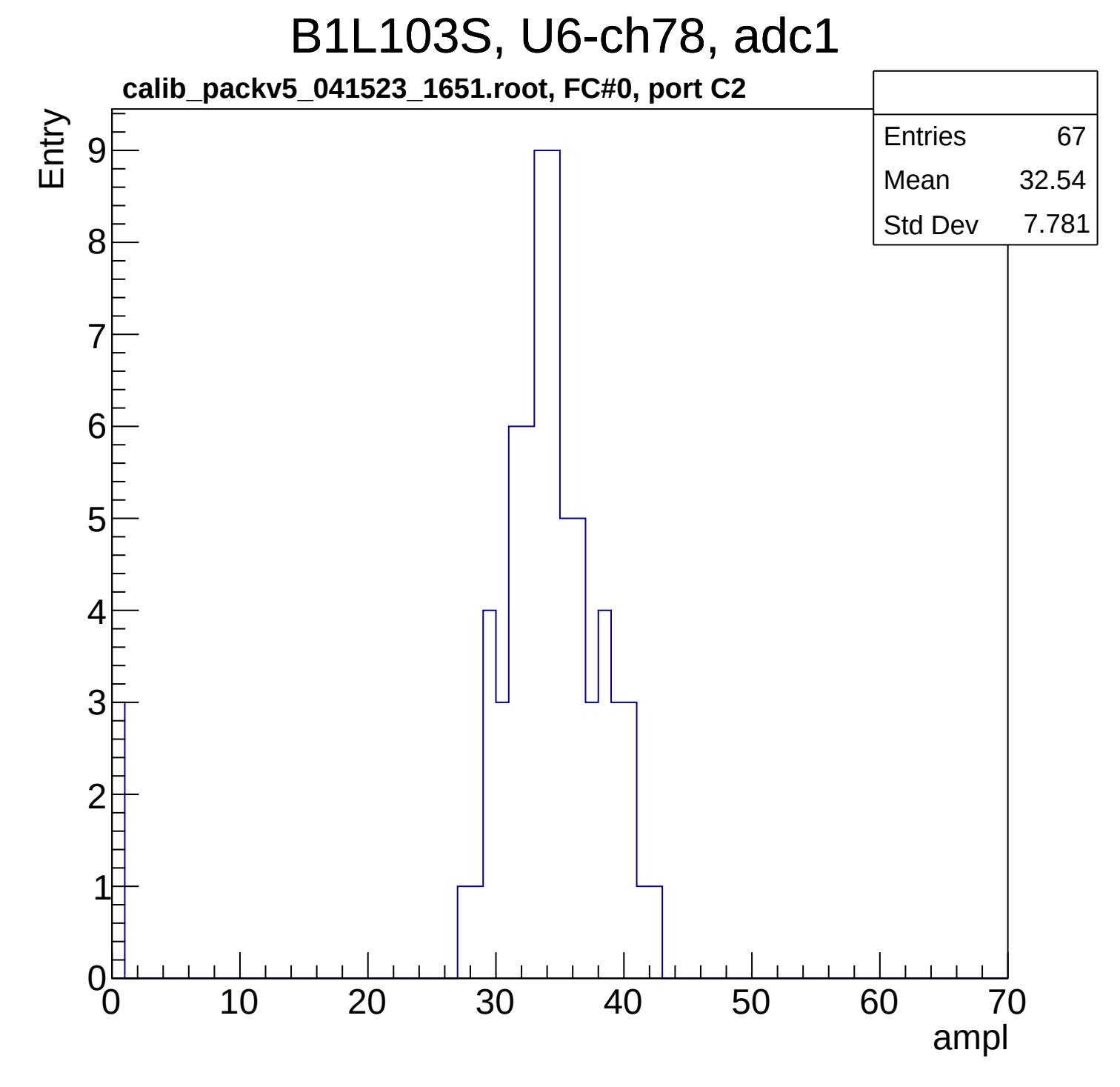
B1L103S, U6-ch78, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 32.54
Std Dev 7.781
Entry
ampl
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4
5
6
7
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0
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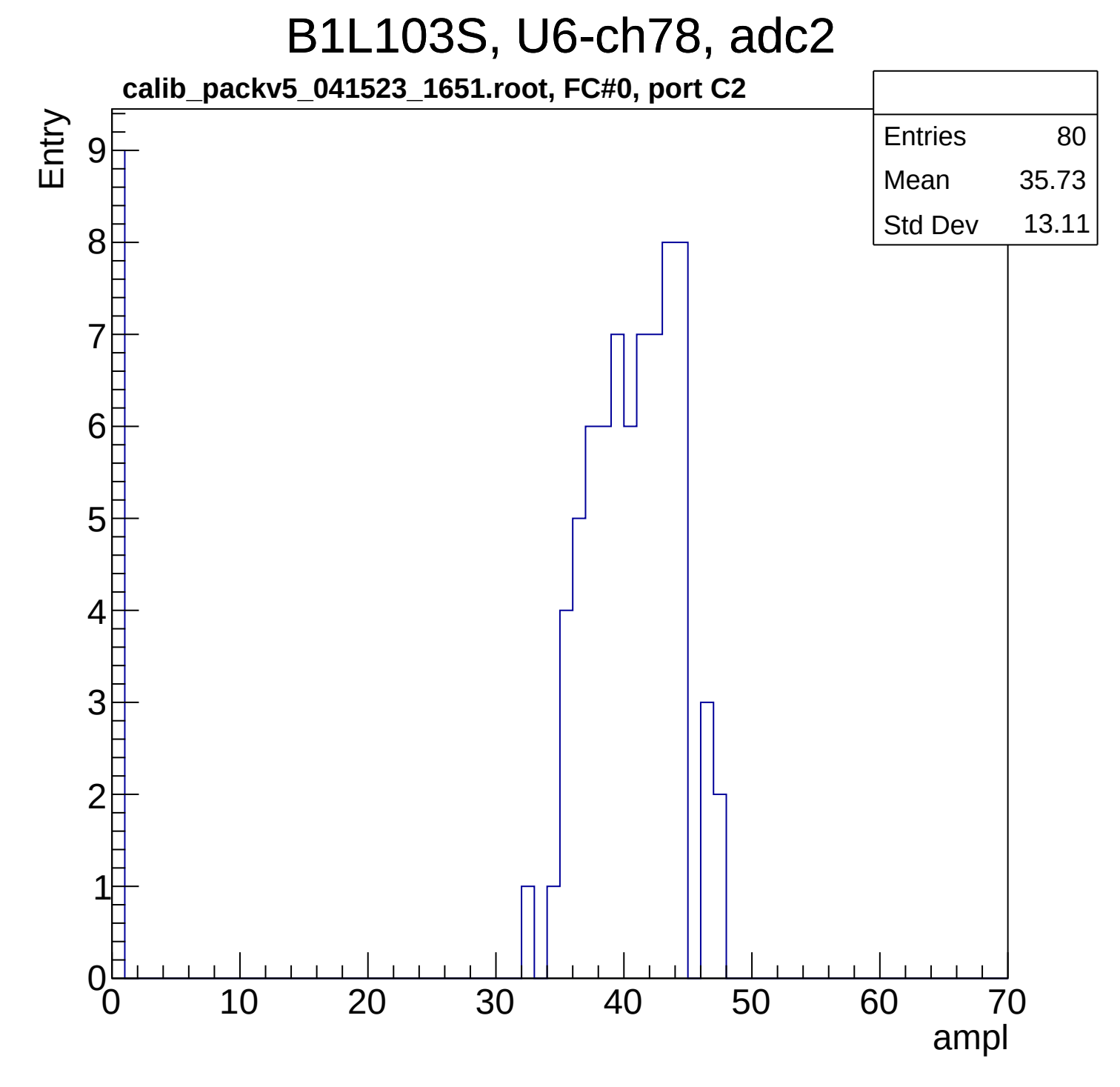
B1L103S, U6-ch78, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 35.73
Std Dev 13.11
Entry
ampl
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6
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0
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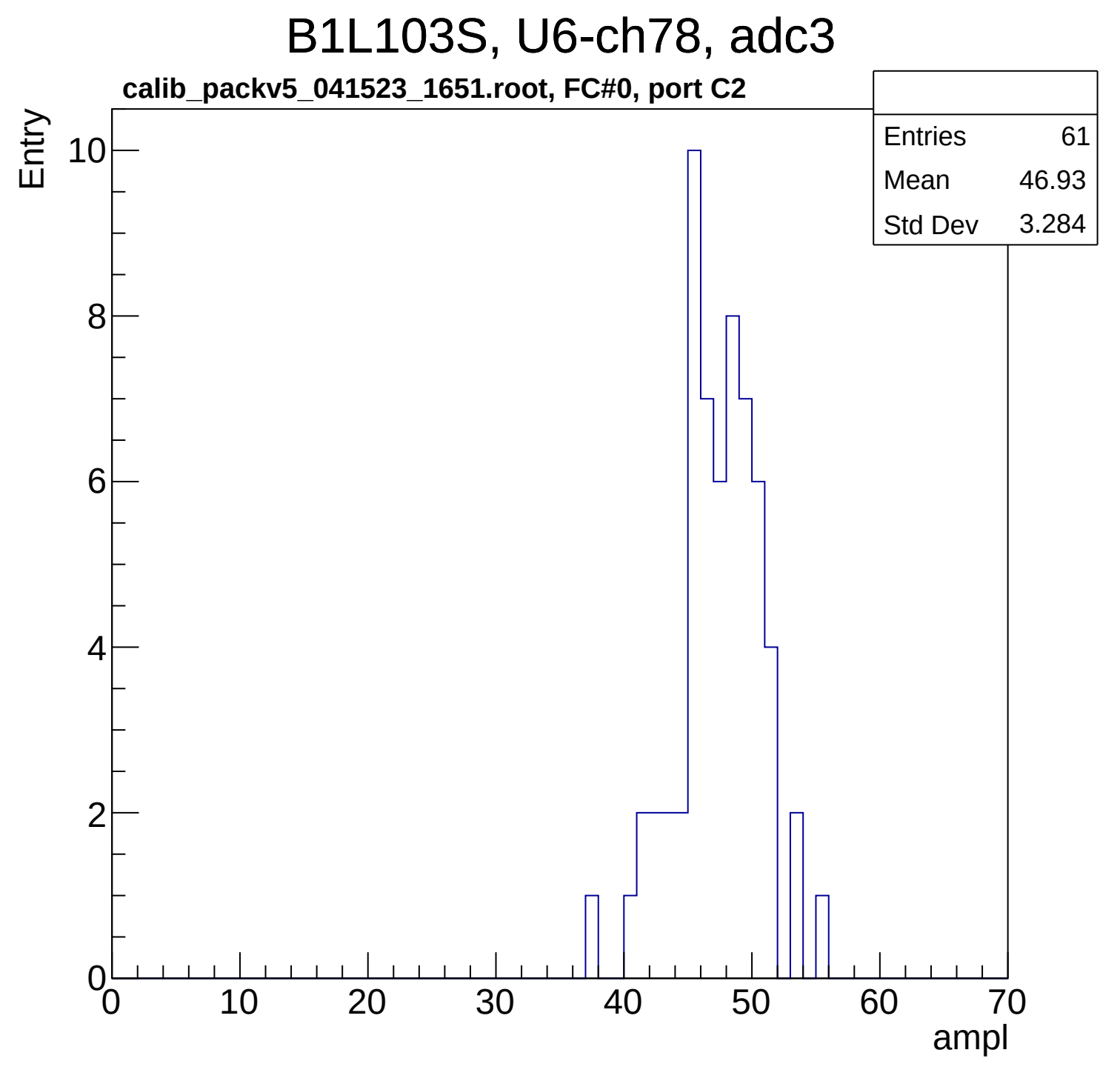
B1L103S, U6-ch78, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 46.93
Std Dev 3.284
Entry
ampl
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4
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0
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40
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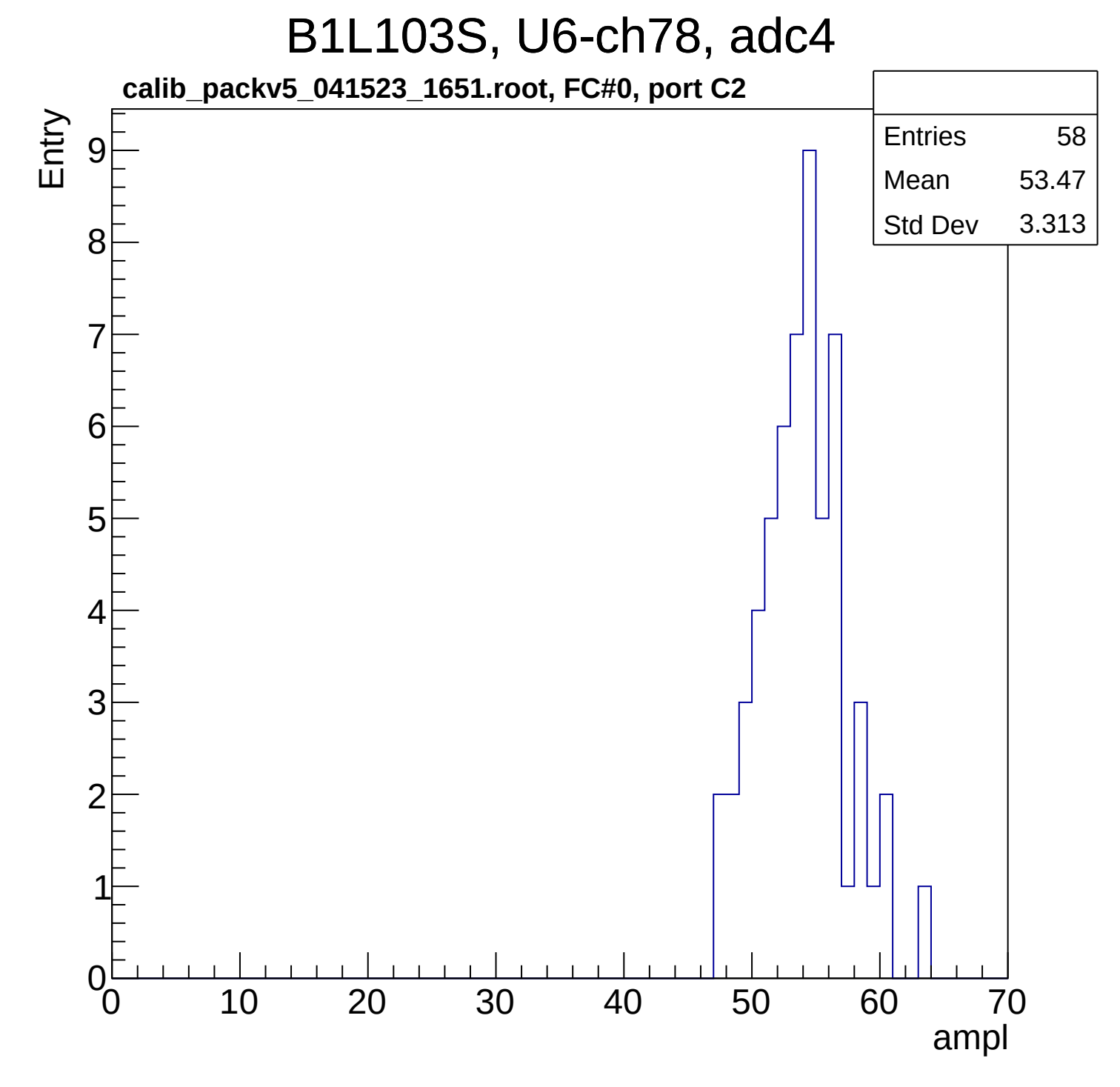
B1L103S, U6-ch78, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 53.47
Std Dev 3.313
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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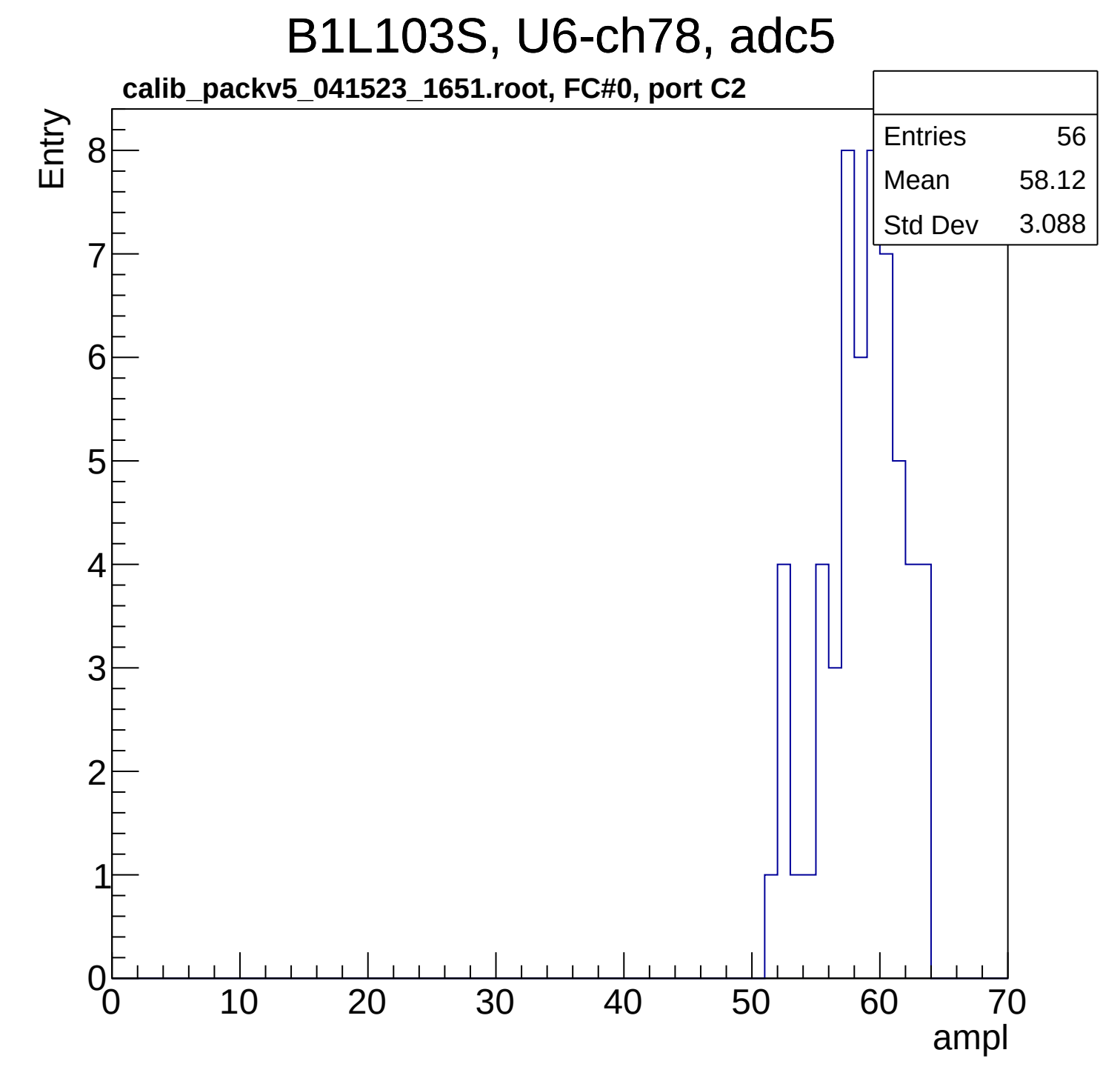
B1L103S, U6-ch78, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 58.12
Std Dev 3.088
Entry
ampl
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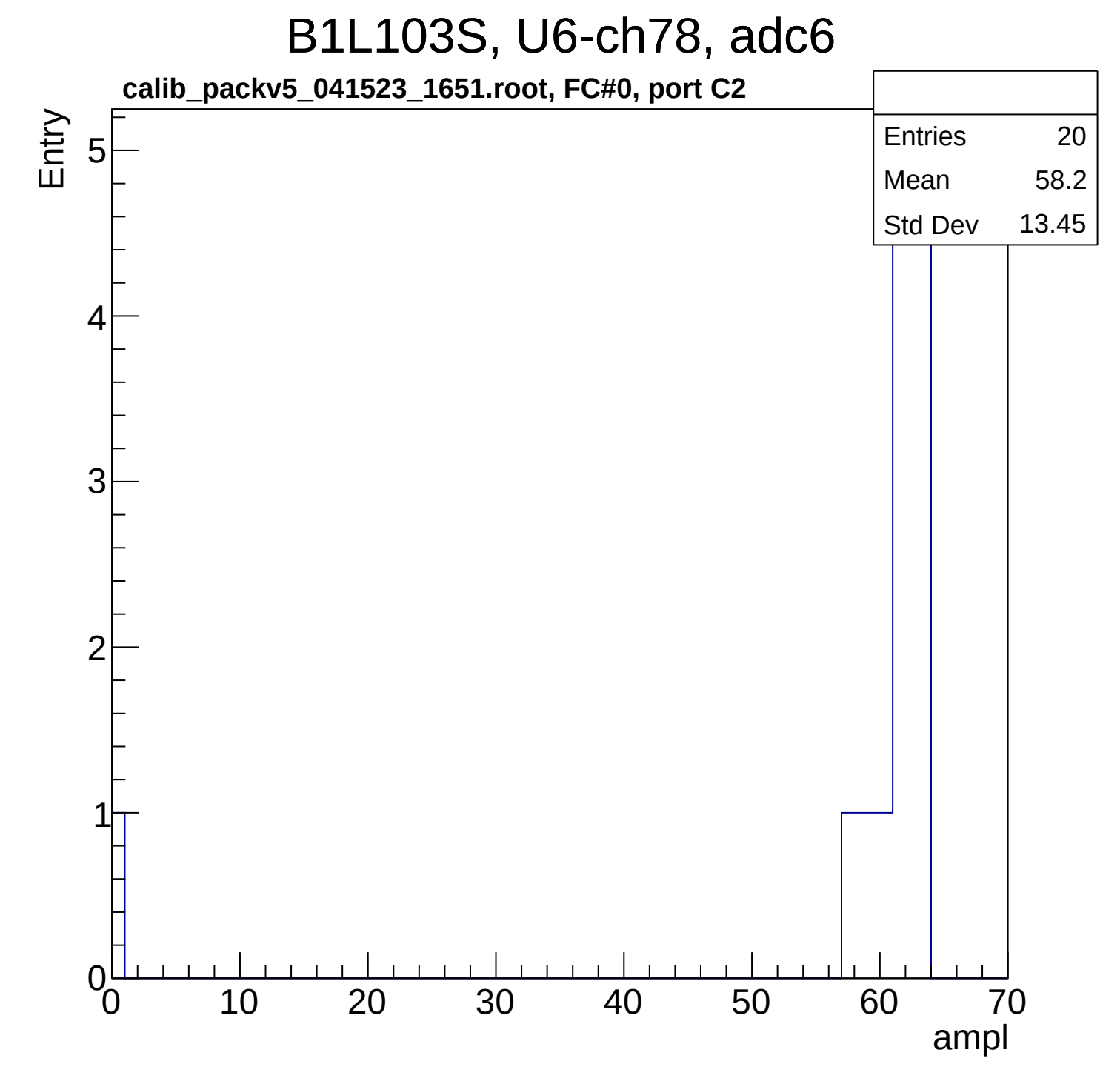
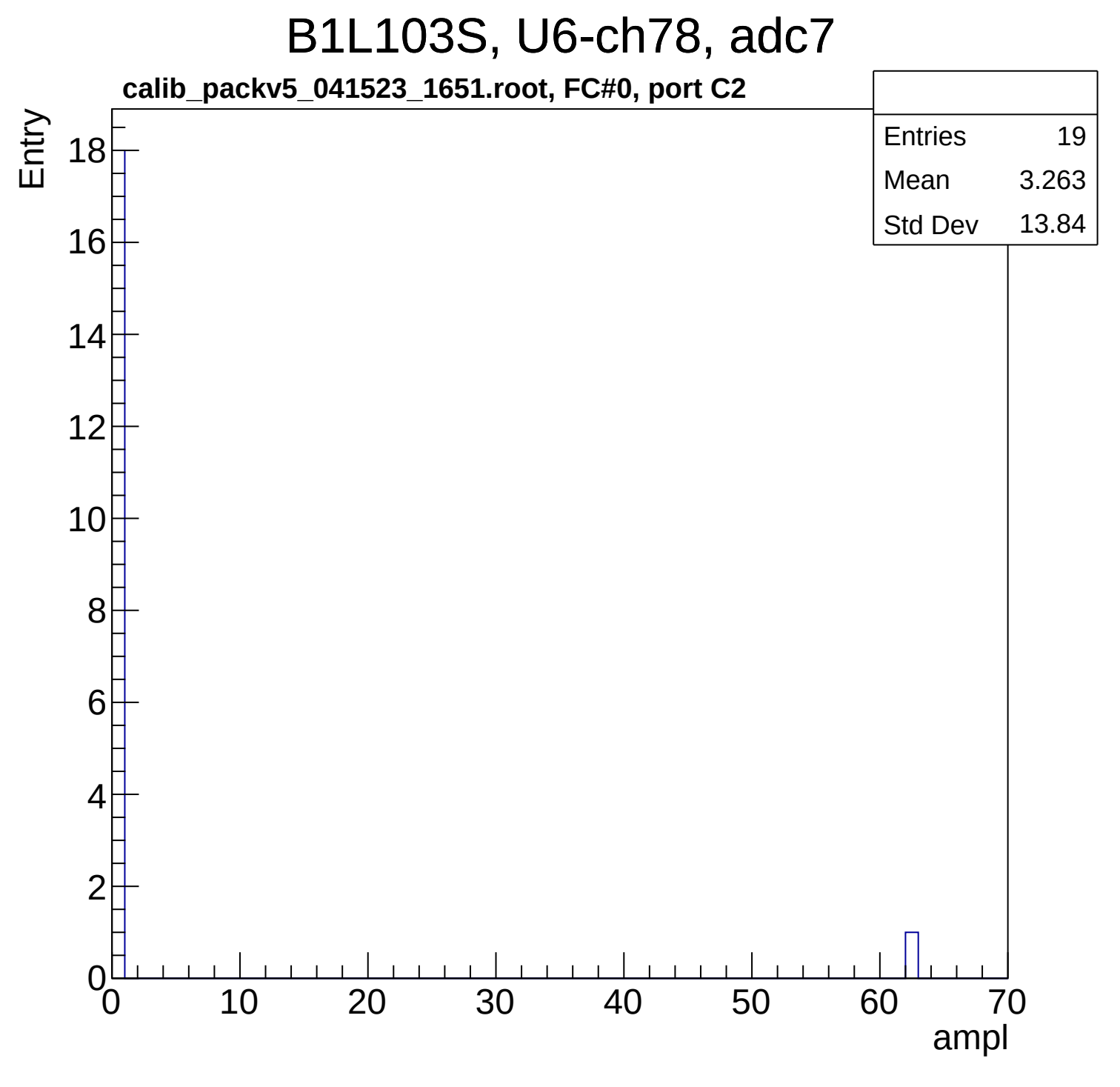
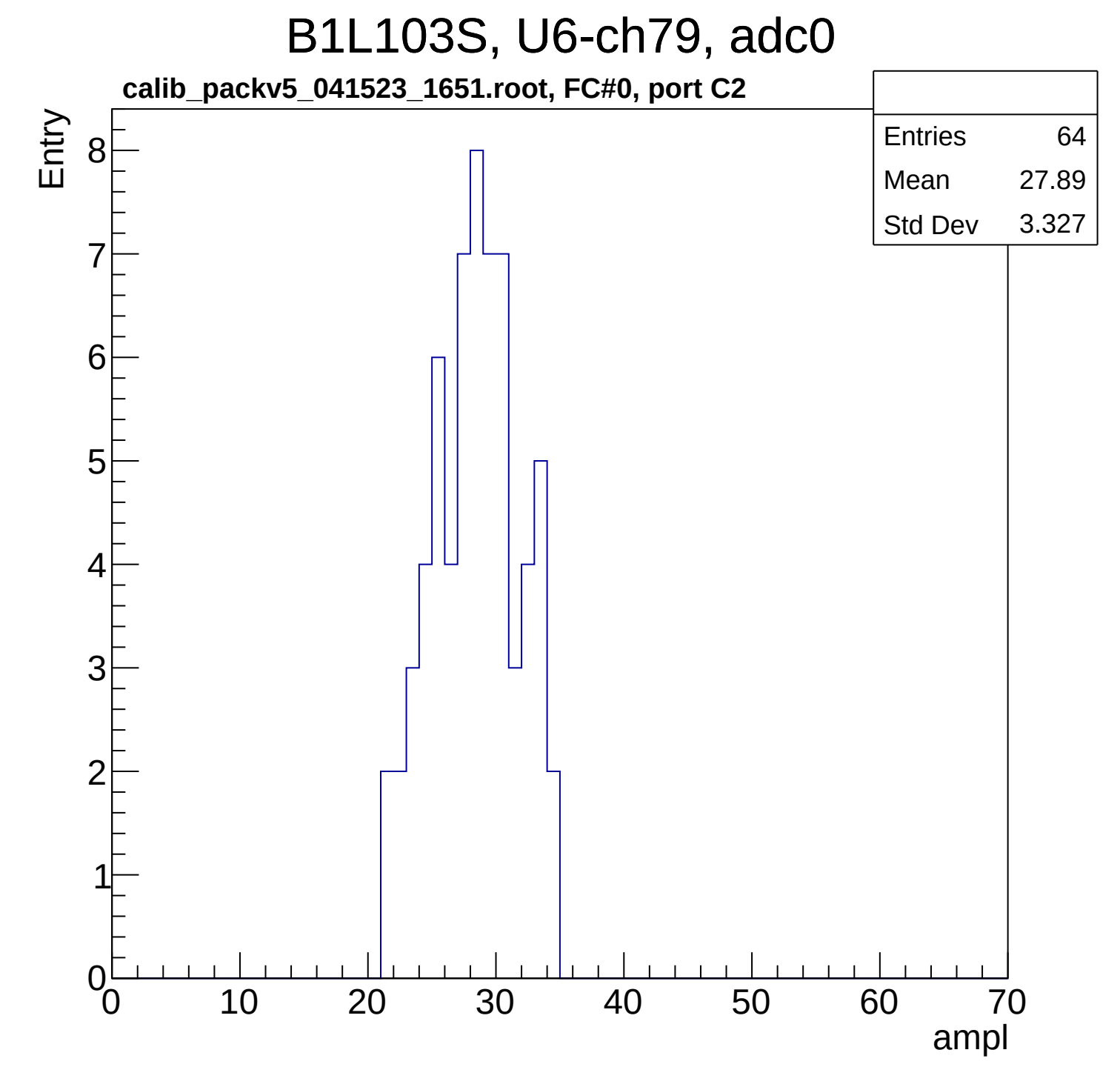
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch78, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 58.2
Std Dev 13.45
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch78, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.263
Std Dev 13.84
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch79, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 27.89
Std Dev 3.327
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
50
60
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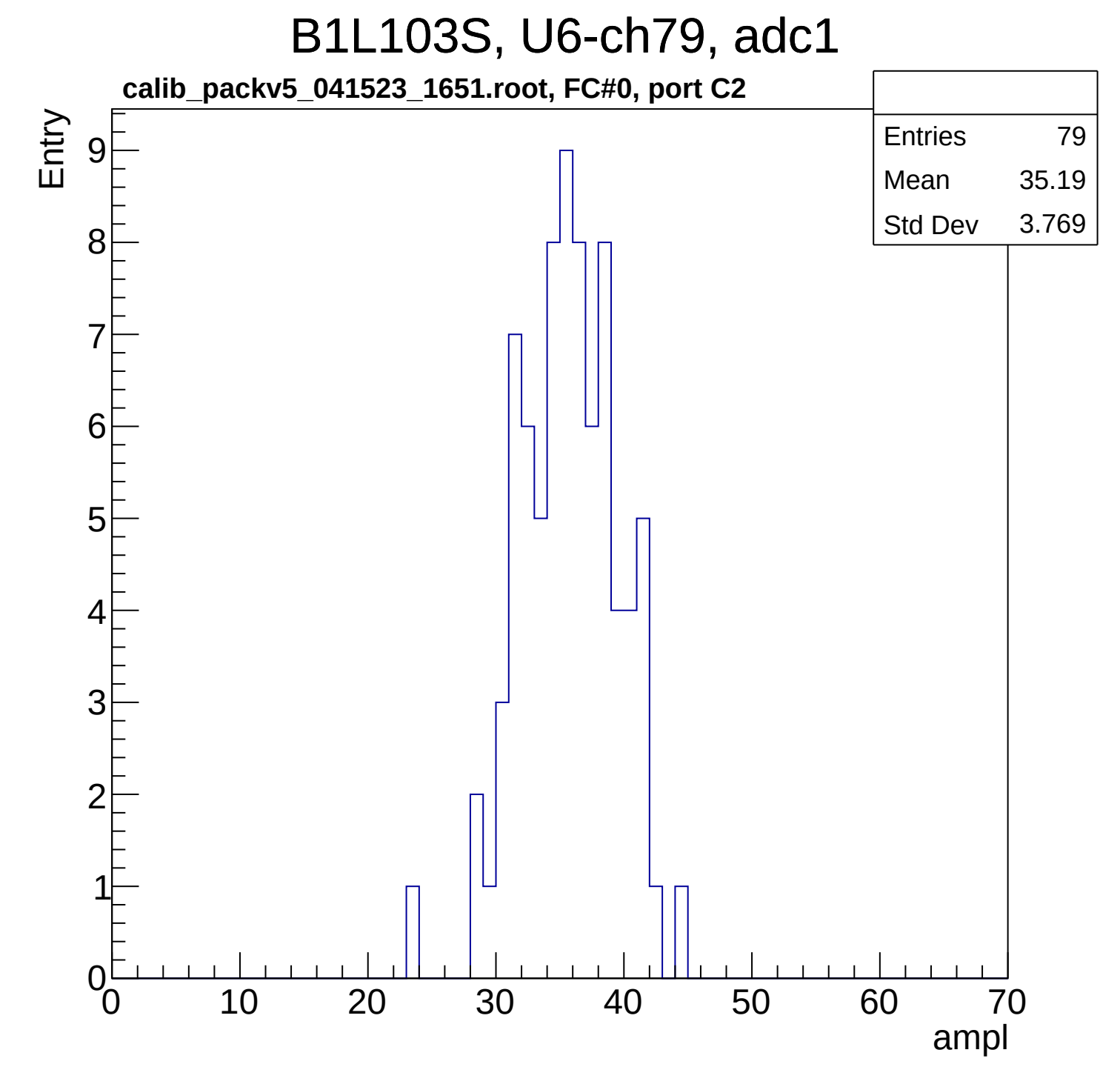
B1L103S, U6-ch79, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 35.19
Std Dev 3.769
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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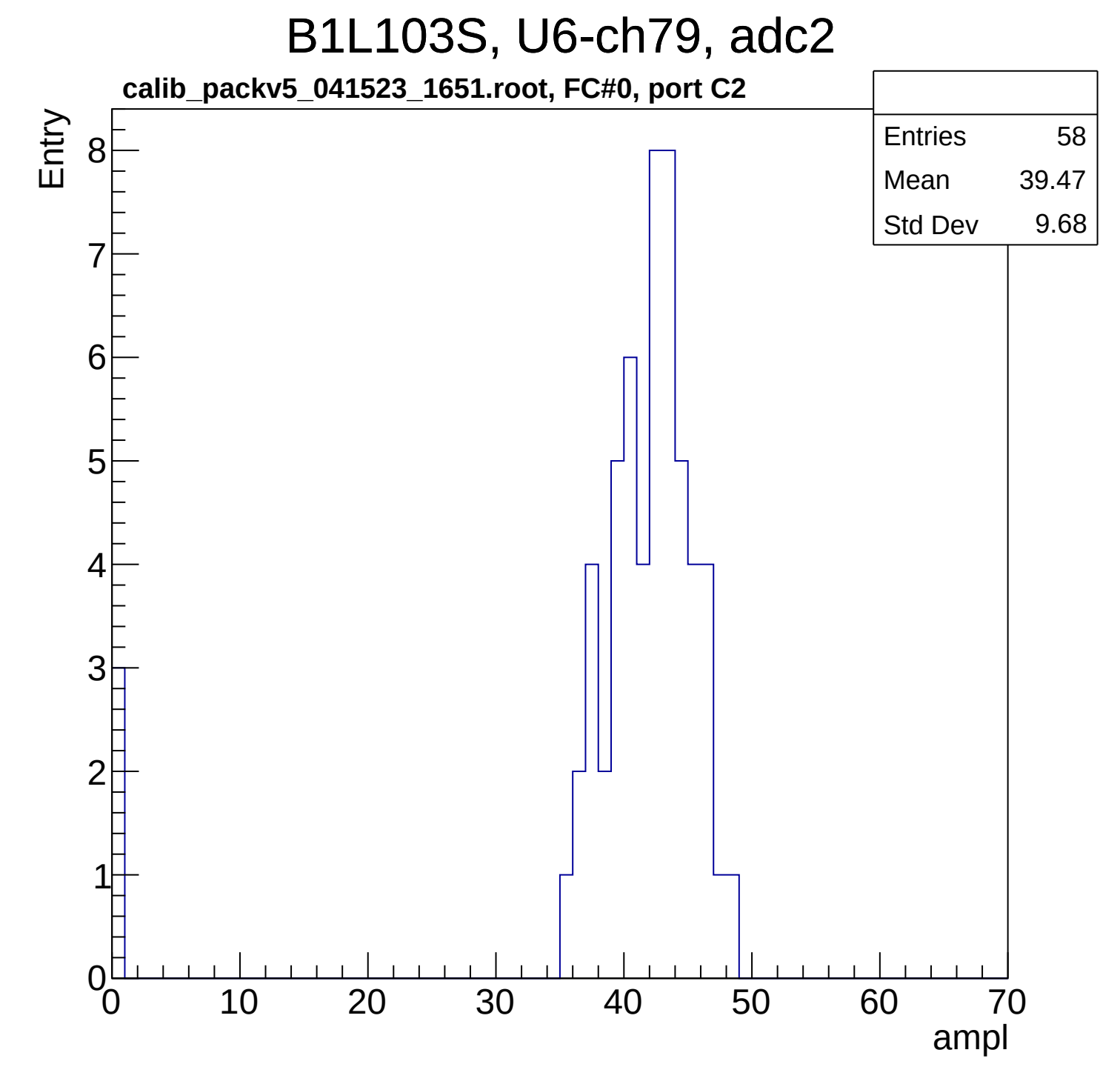
B1L103S, U6-ch79, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 39.47
Std Dev 9.68
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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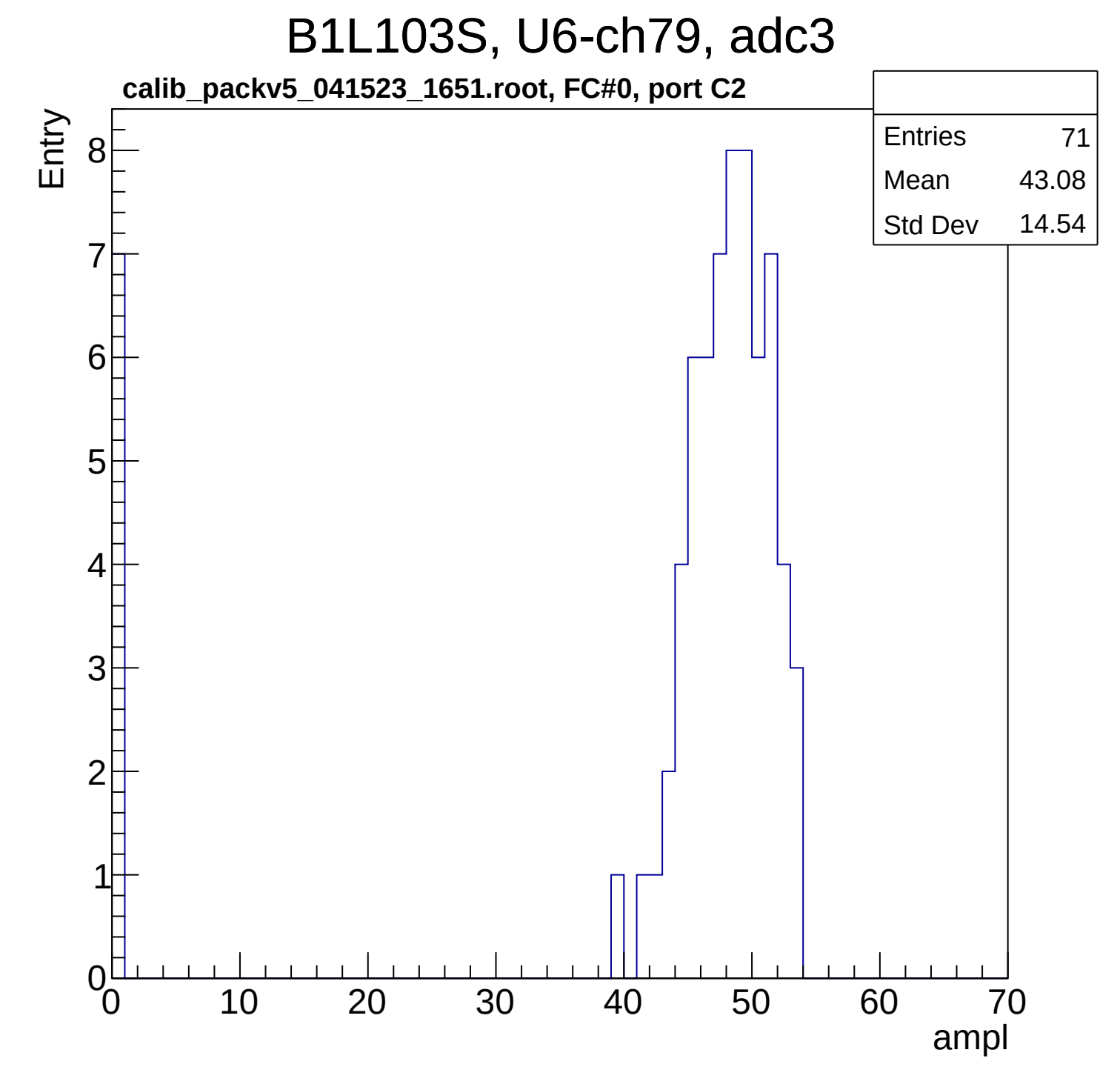
B1L103S, U6-ch79, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 43.08
Std Dev 14.54
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
50
60
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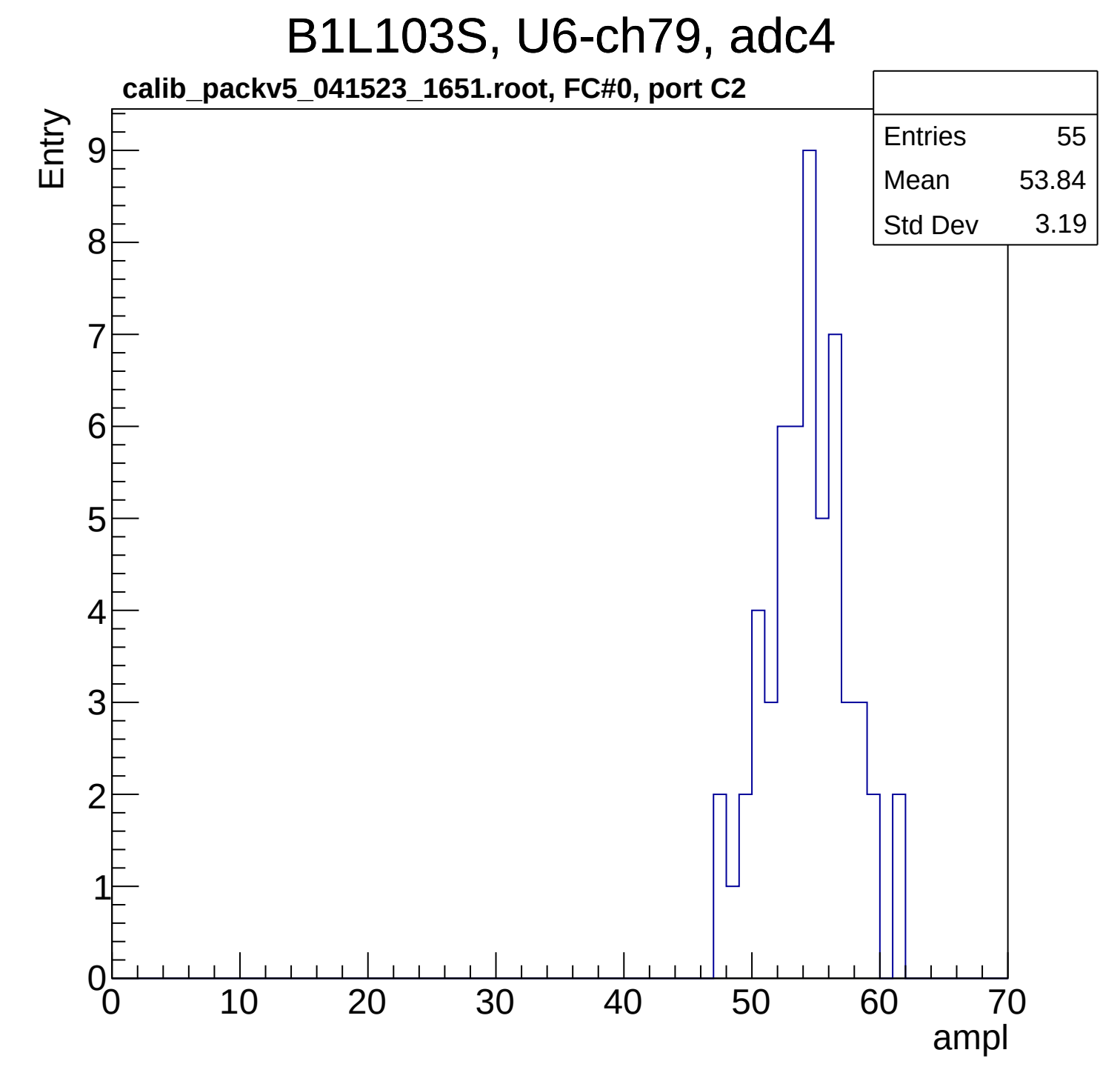
B1L103S, U6-ch79, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 53.84
Std Dev 3.19
Entry
ampl
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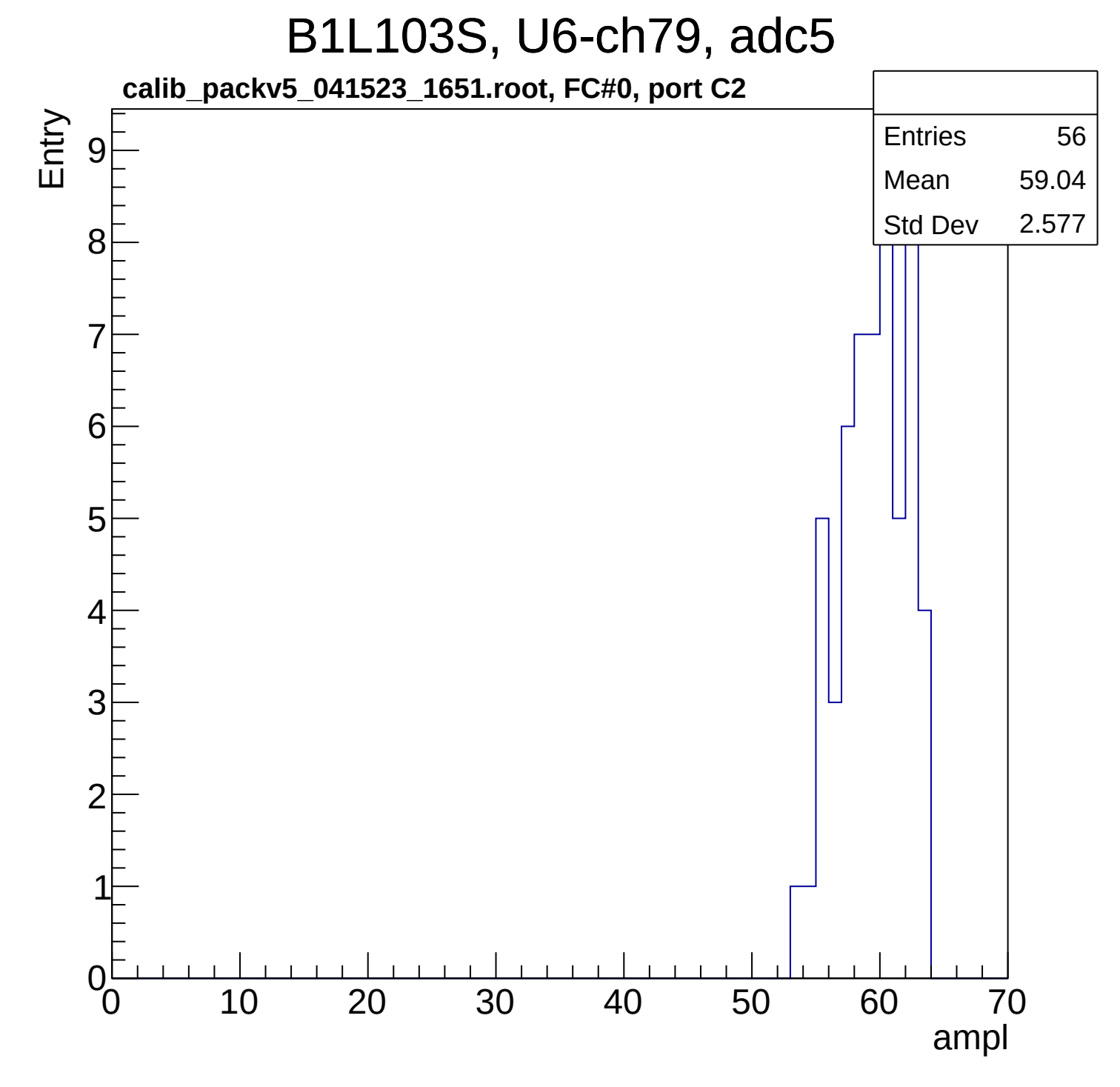
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch79, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 59.04
Std Dev 2.577
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
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60
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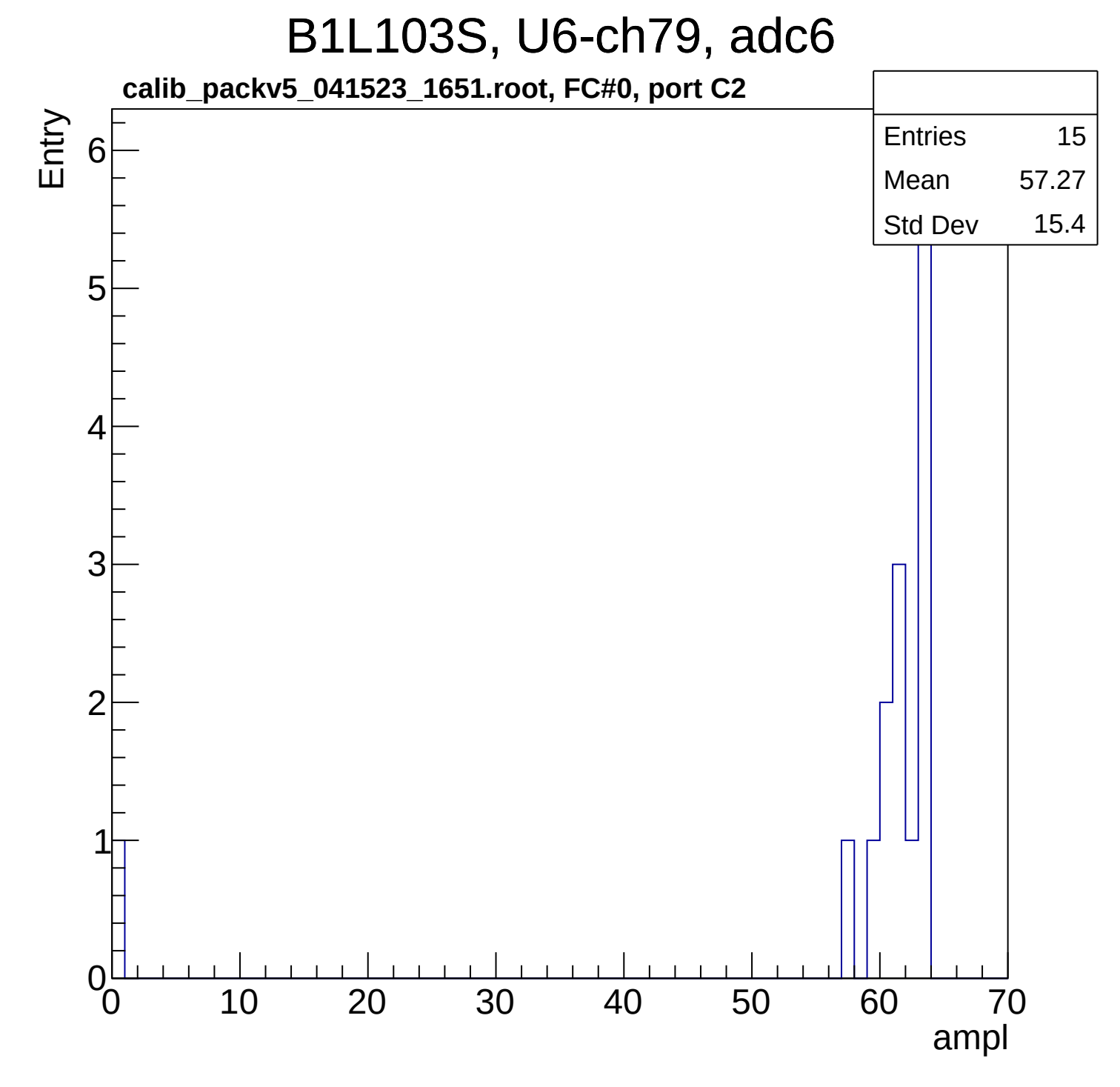
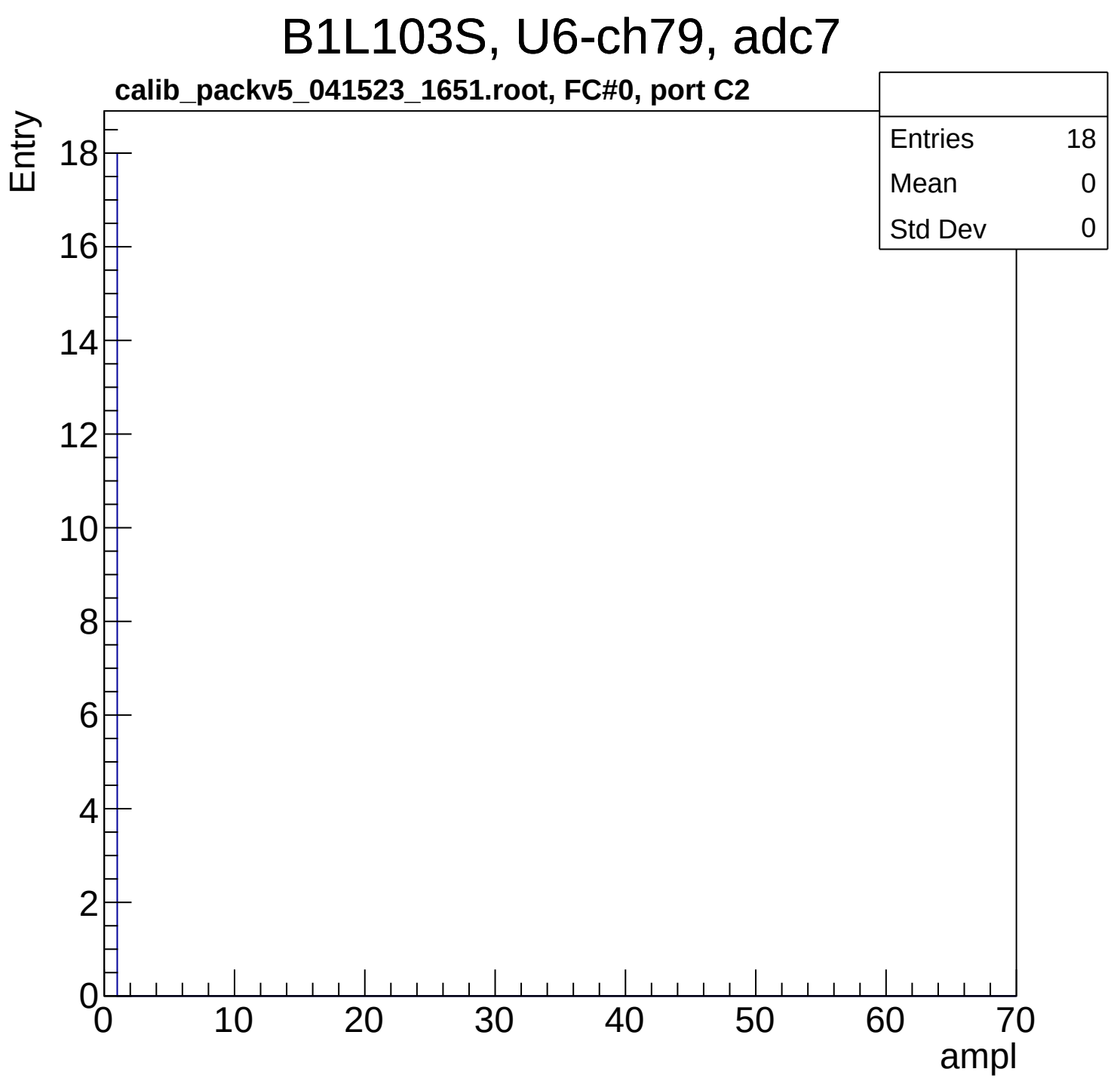

B1L103S, U6-ch79, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 57.27
Std Dev 15.4
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch79, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
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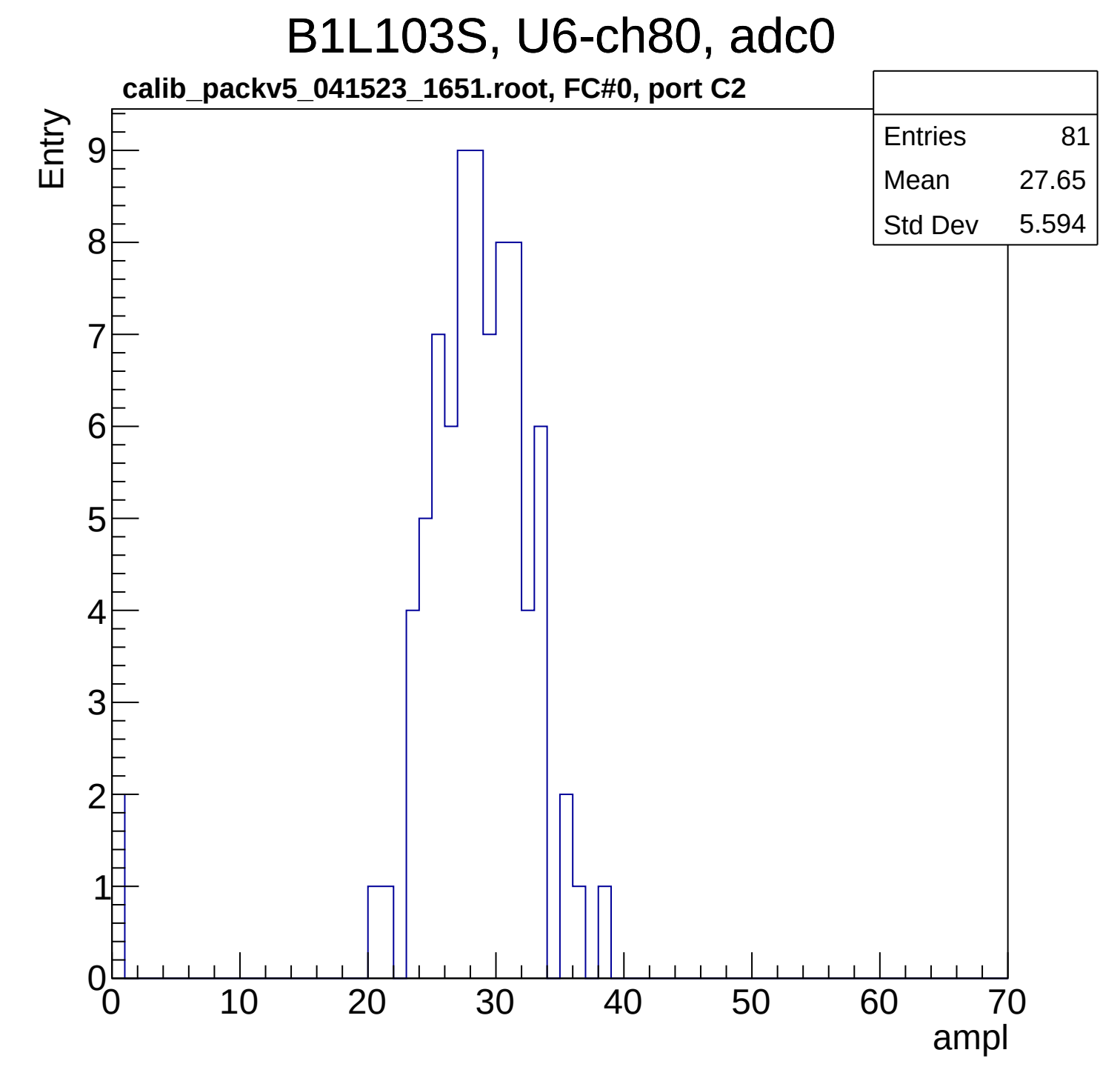
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch80, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 27.65
Std Dev 5.594
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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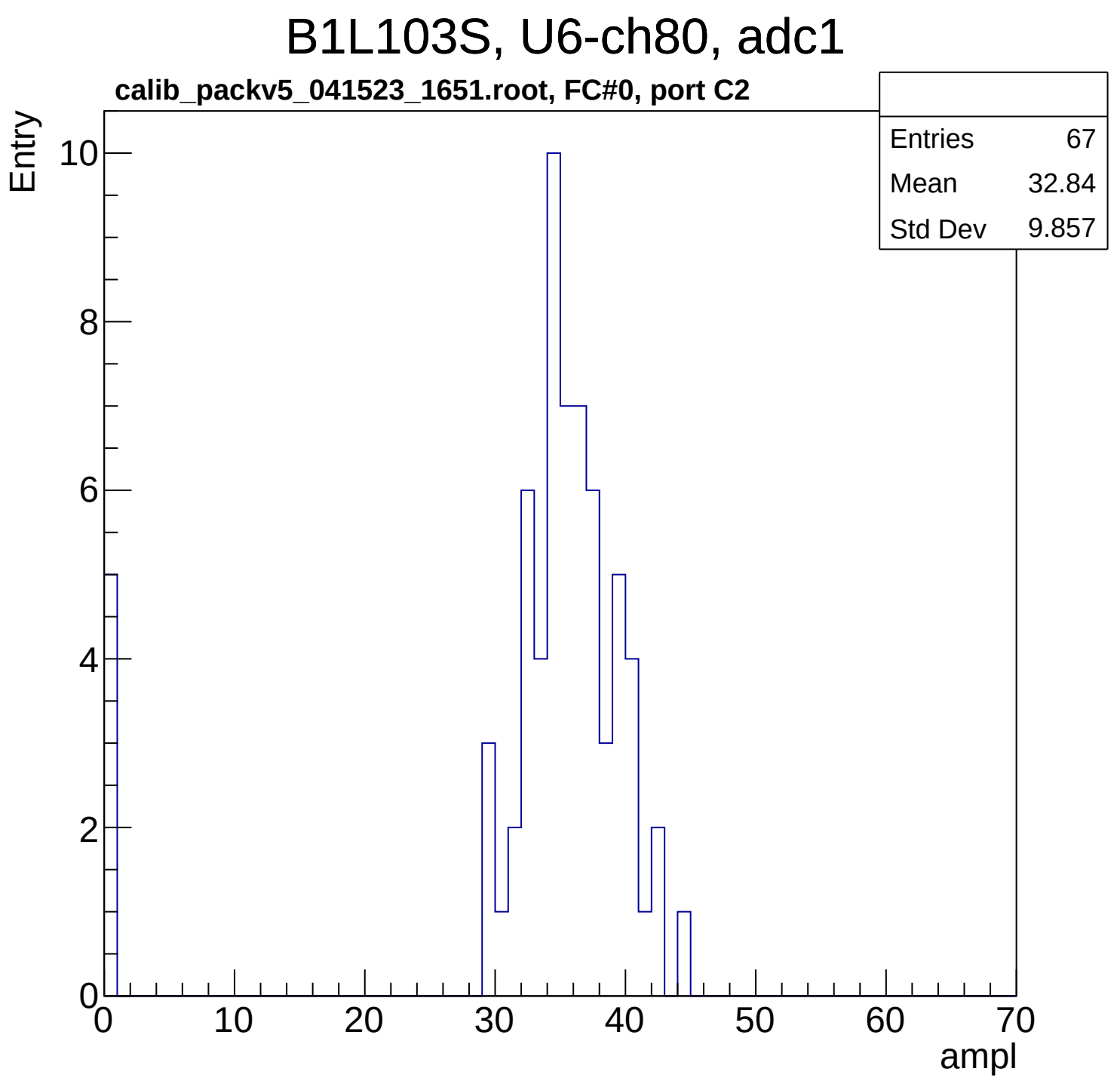
40
50
60
70


B1L103S, U6-ch80, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 32.84
Std Dev 9.857
Entry
ampl
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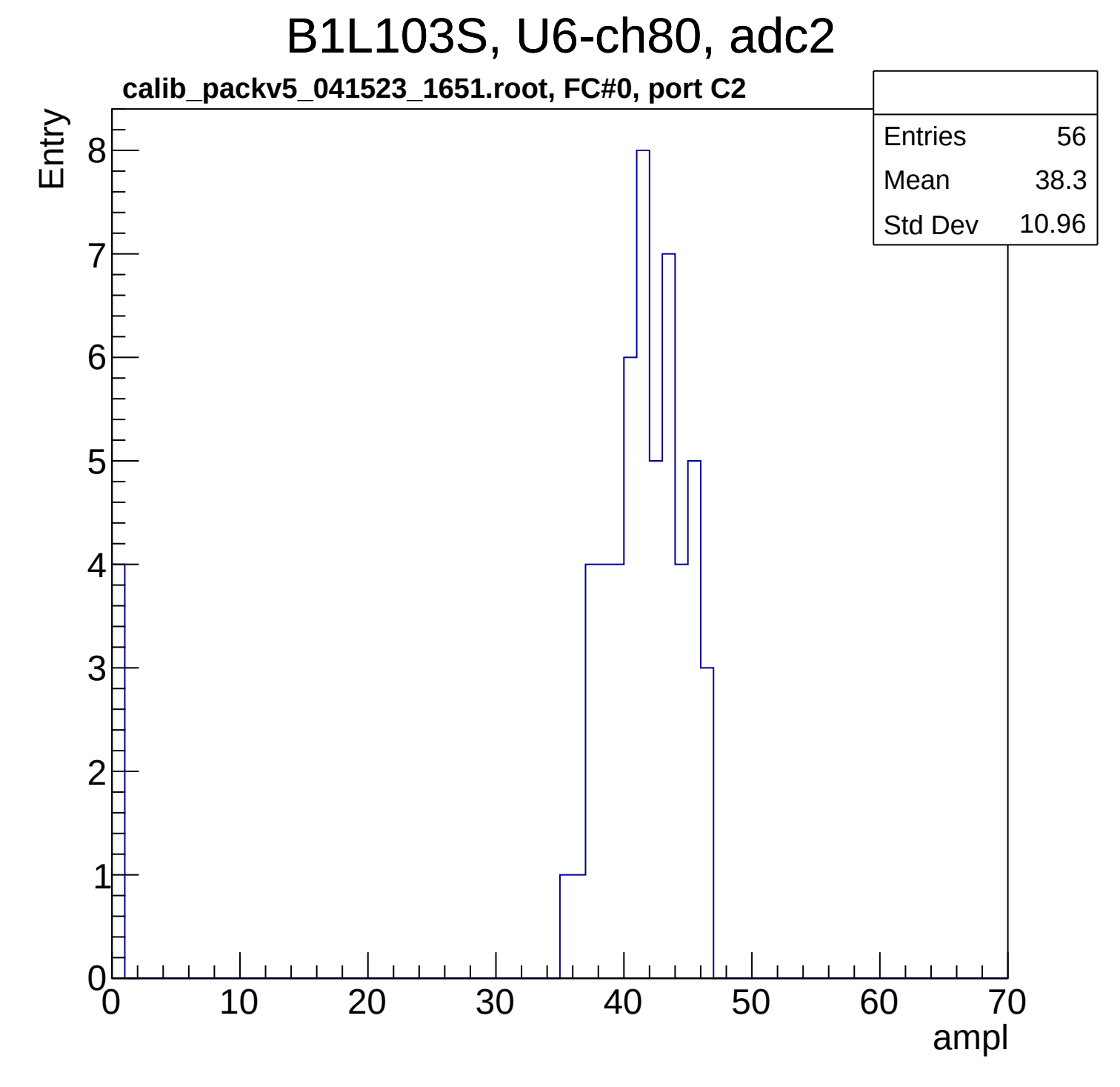
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U6-ch80, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 38.3
Std Dev 10.96
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
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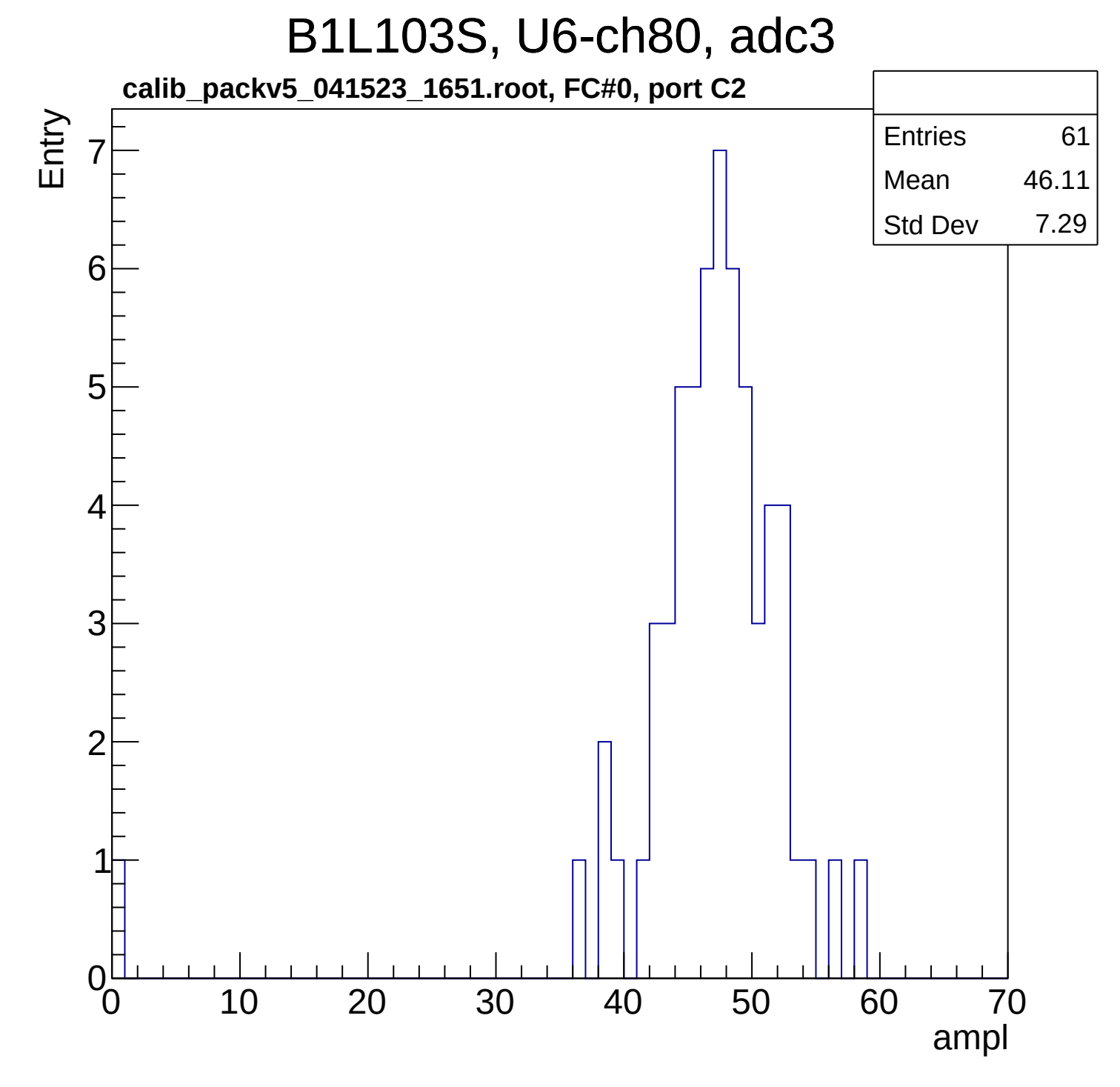
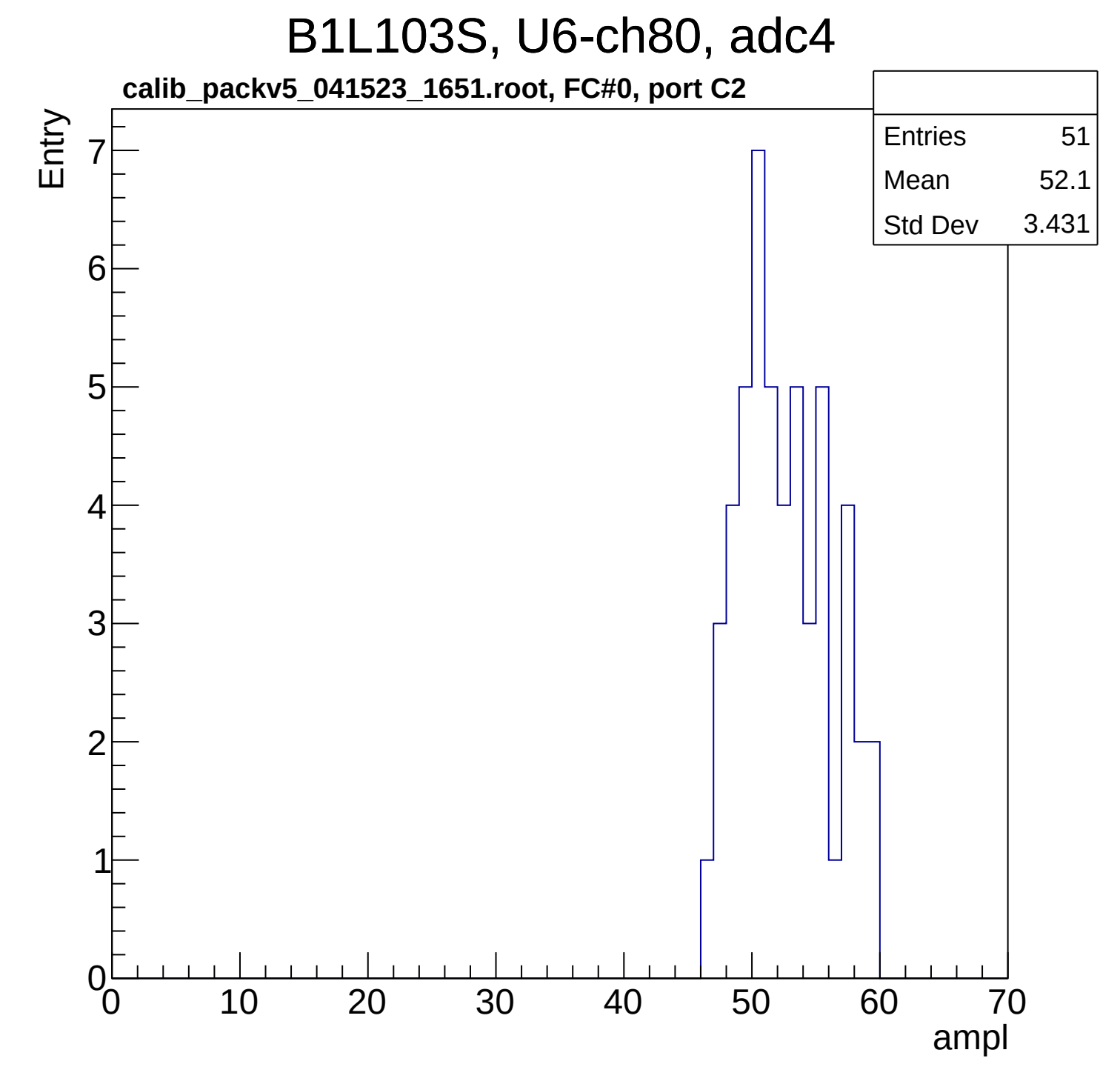
60
70


B1L103S, U6-ch80, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 46.11
Std Dev 7.29
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U6-ch80, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 52.1
Std Dev 3.431
Entry
ampl
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3
4
5
6
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0
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60
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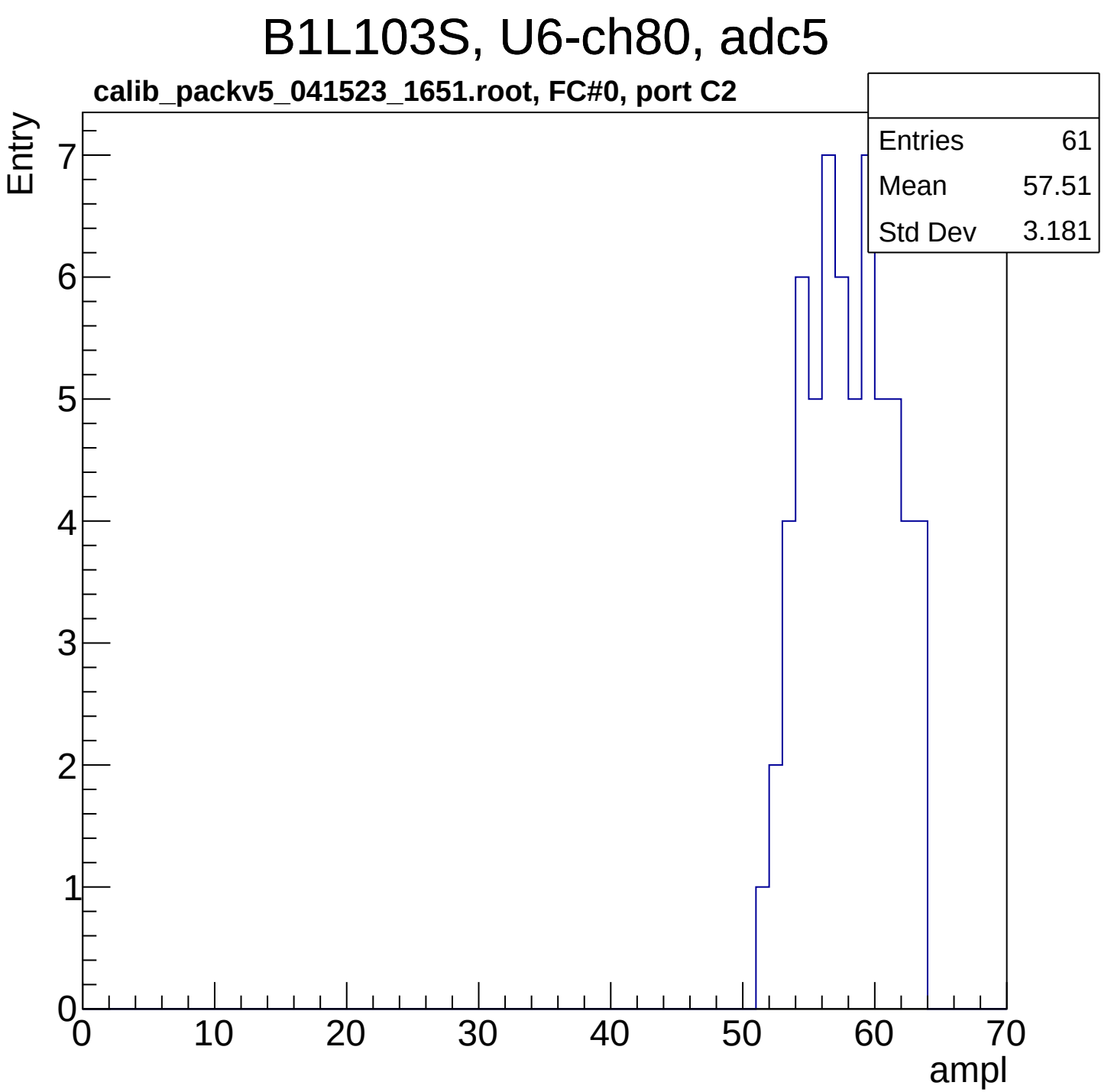
B1L103S, U6-ch80, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 57.51
Std Dev 3.181
Entry
ampl
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4
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0
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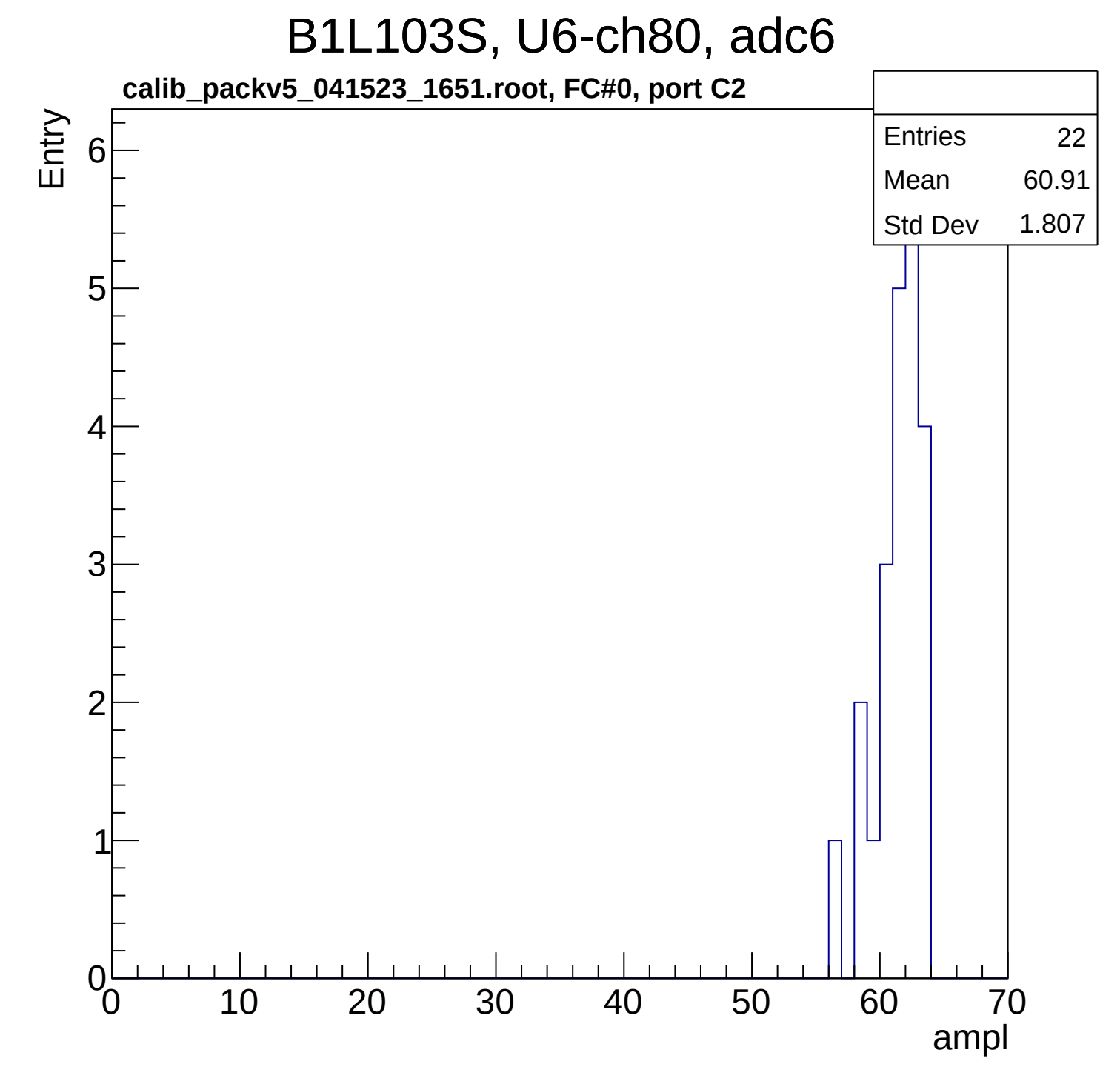
B1L103S, U6-ch80, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 60.91
Std Dev 1.807
Entry
ampl
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2
3
4
5
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0
10
20
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40
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60
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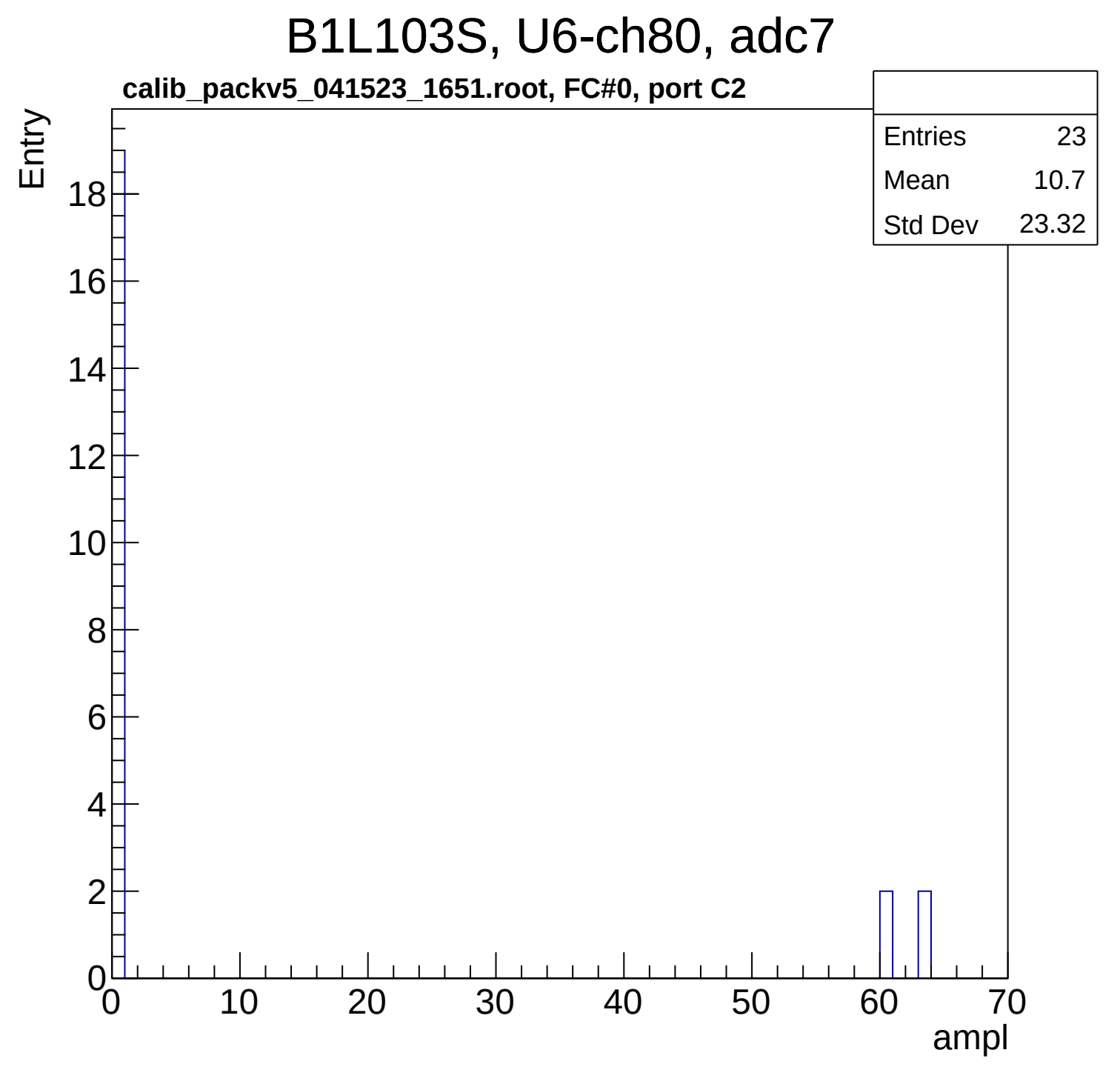
B1L103S, U6-ch80, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 10.7
Std Dev 23.32
Entry
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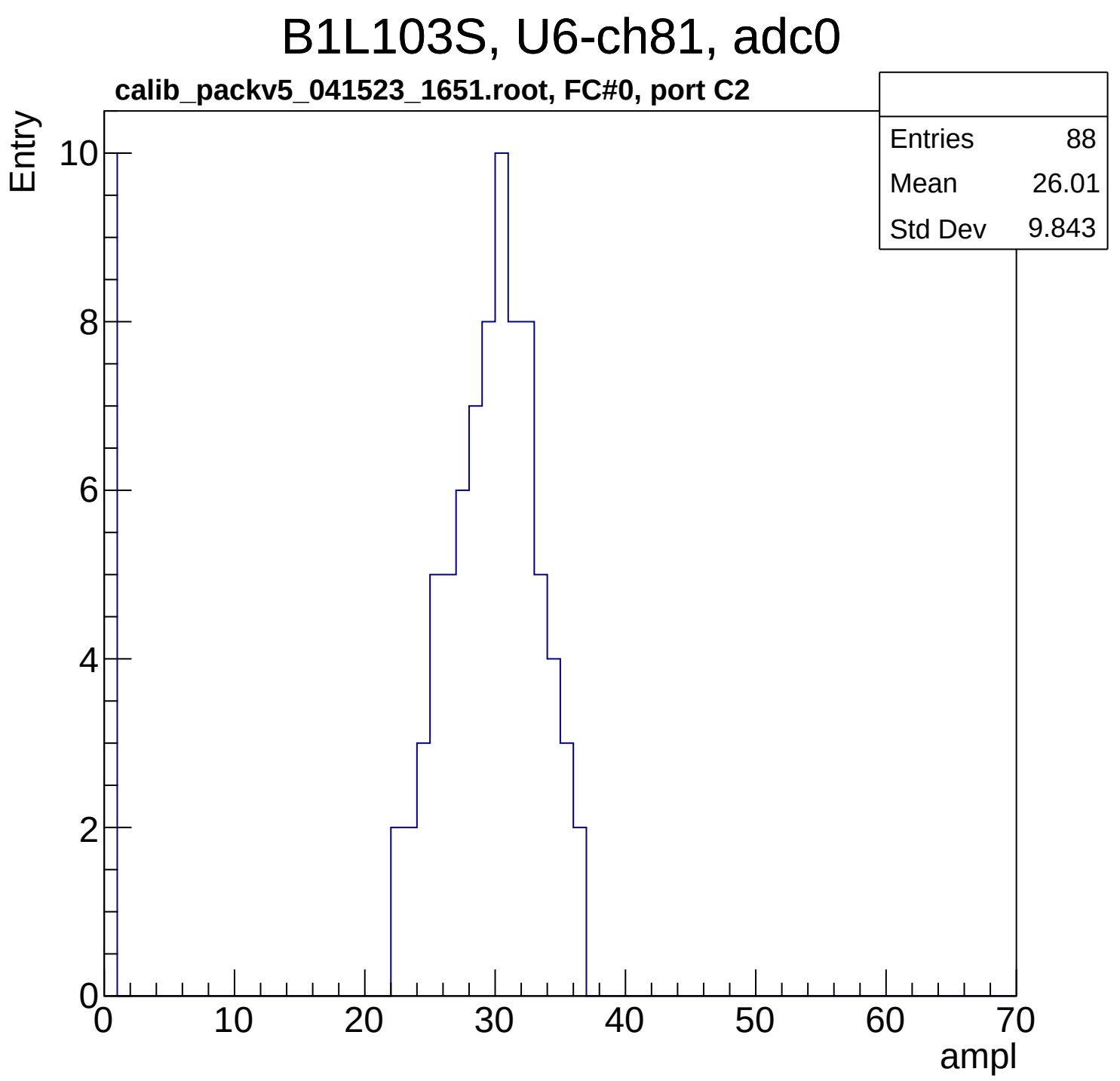
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch81, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 26.01
Std Dev 9.843
Entry
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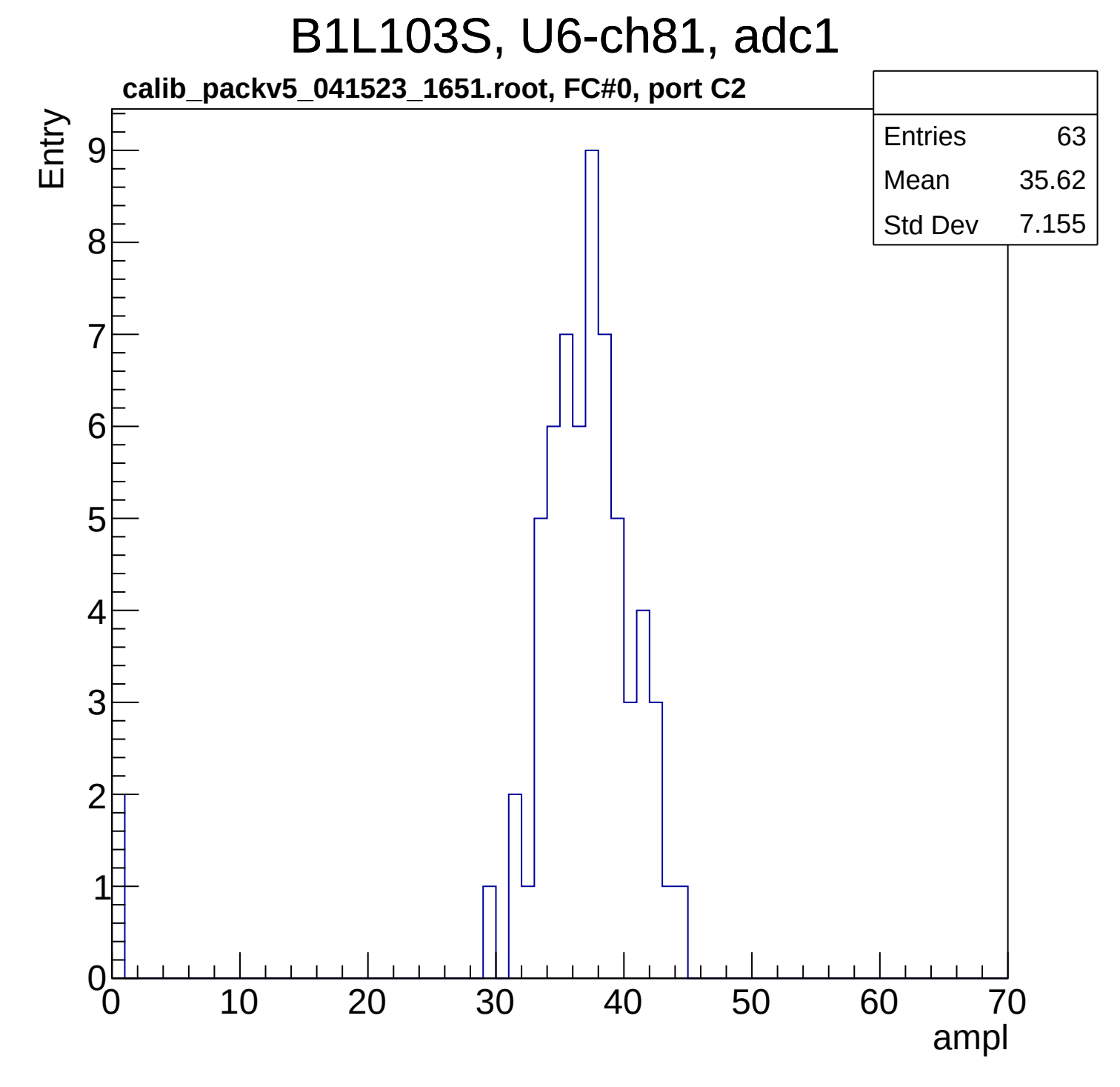
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch81, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 35.62
Std Dev 7.155
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
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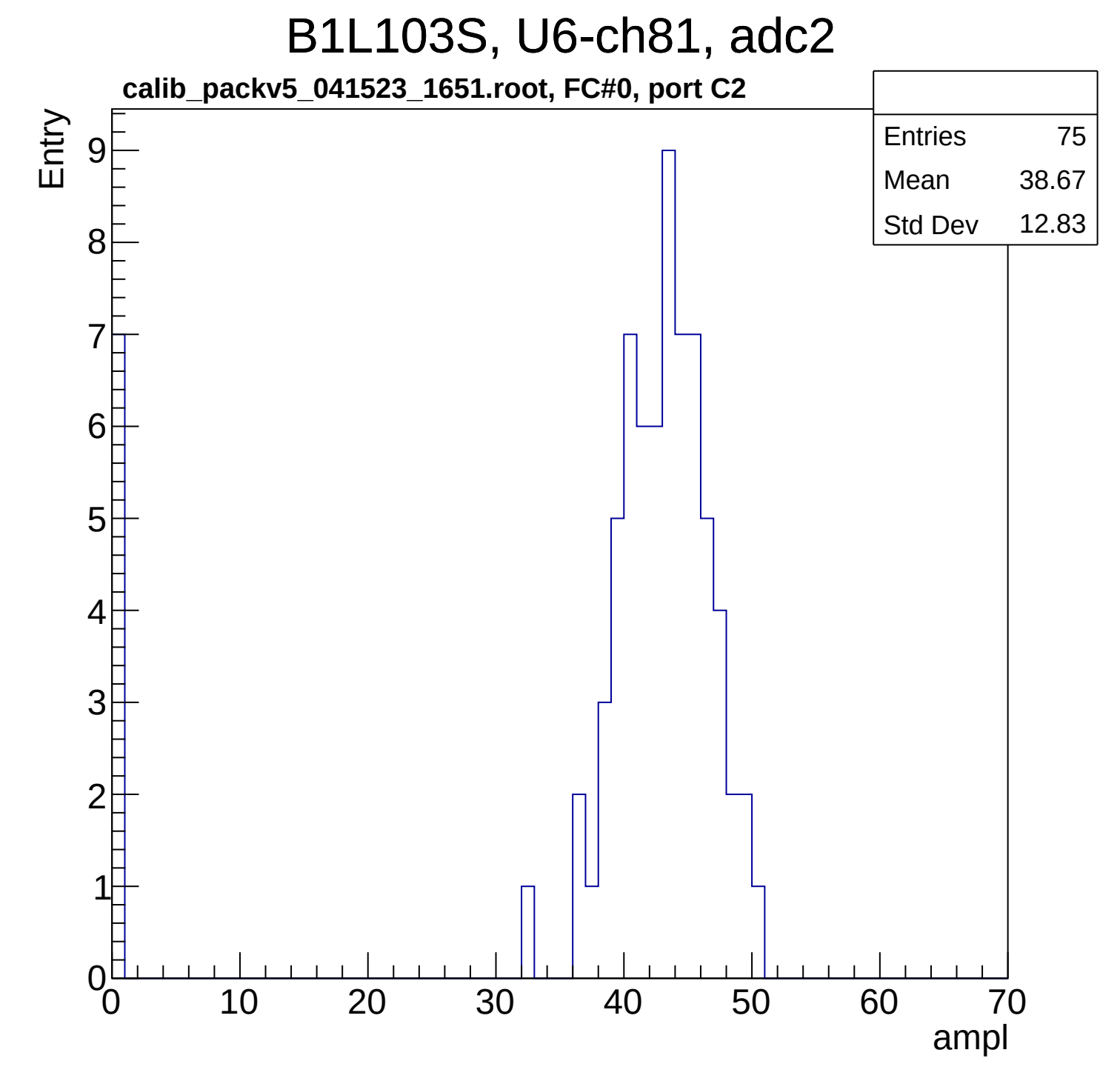
B1L103S, U6-ch81, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 38.67
Std Dev 12.83
Entry
ampl
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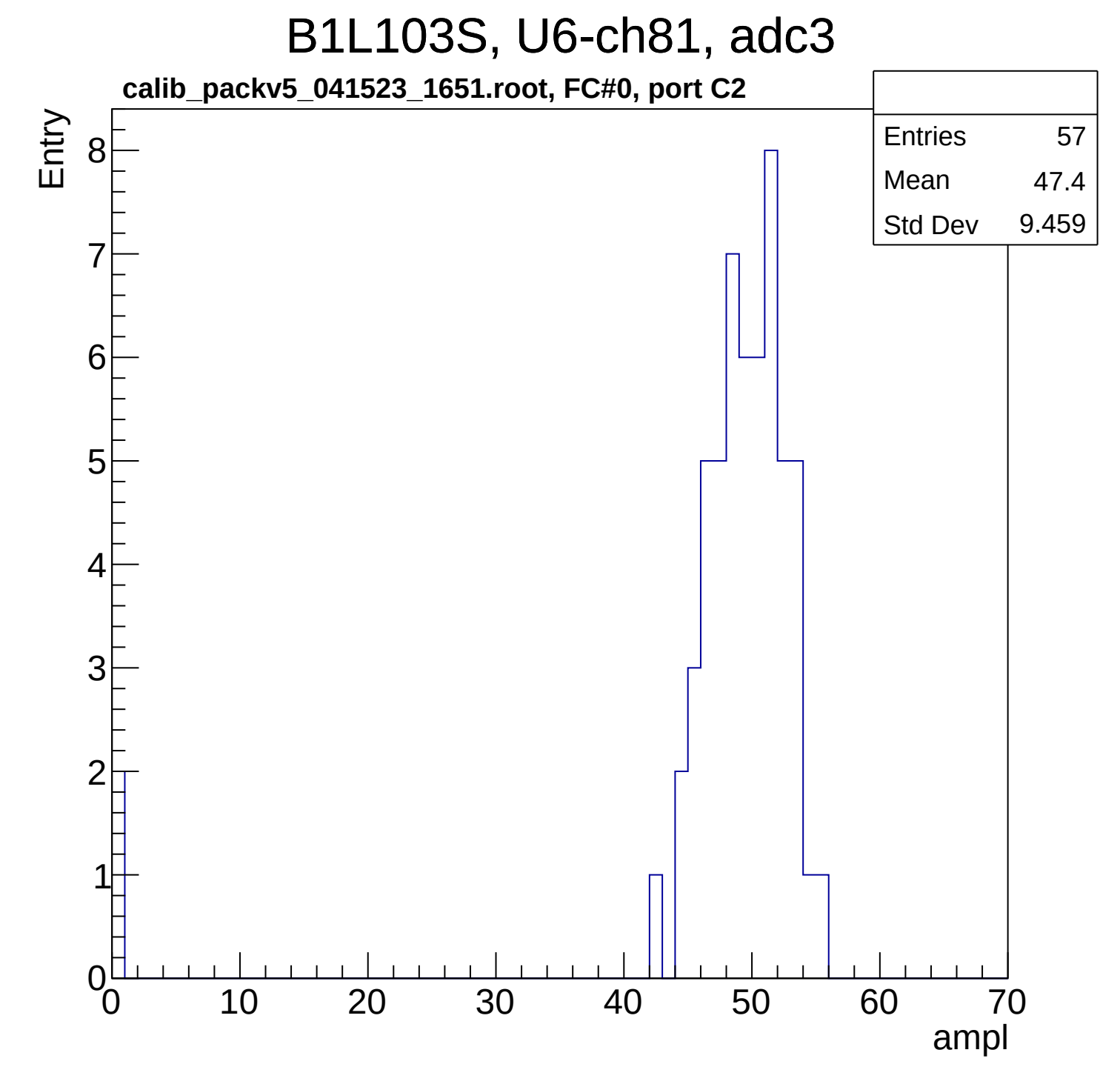
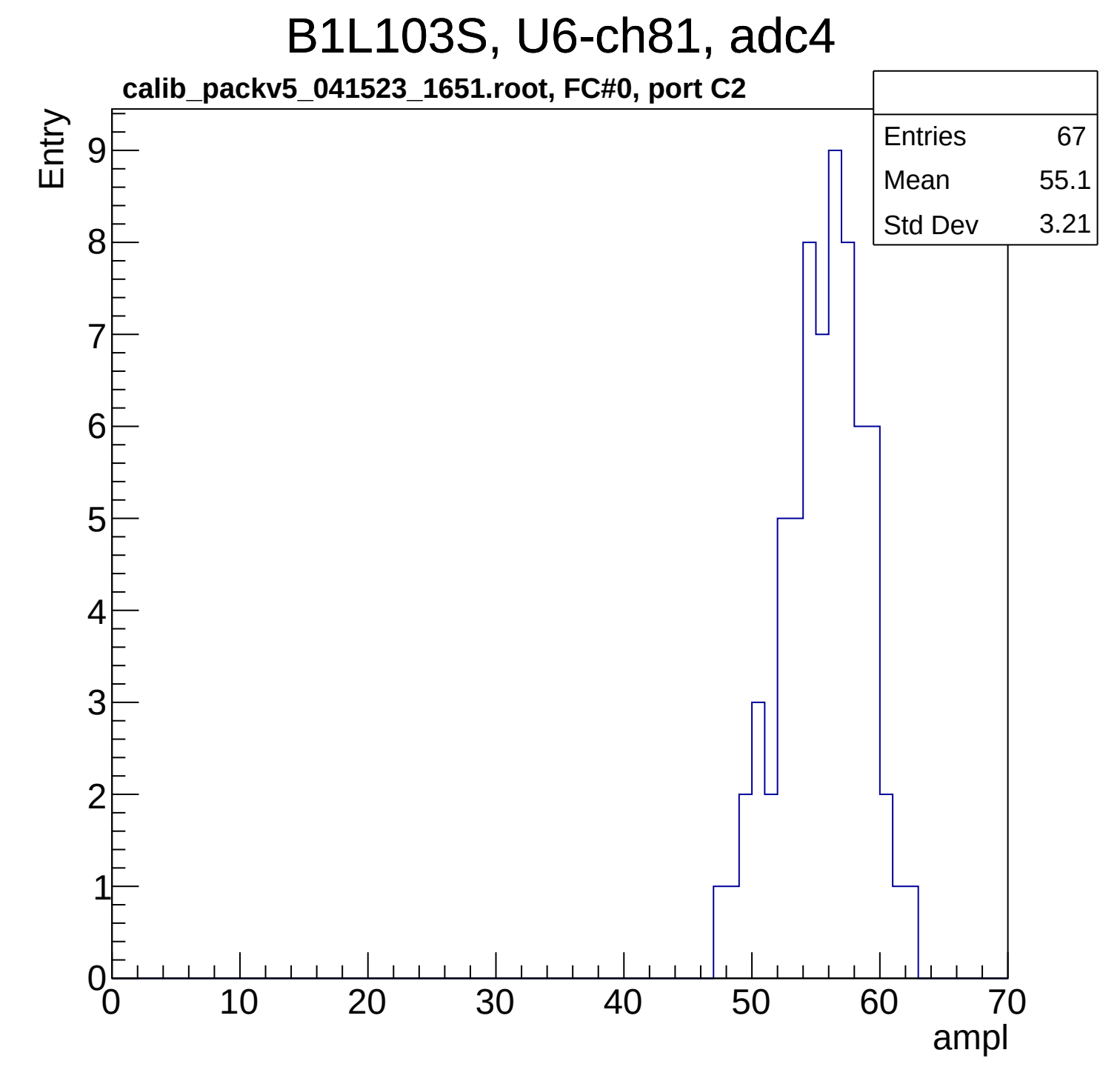
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch81, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 47.4
Std Dev 9.459
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch81, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 55.1
Std Dev 3.21
Entry
ampl
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2
3
4
5
6
7
8
9
0
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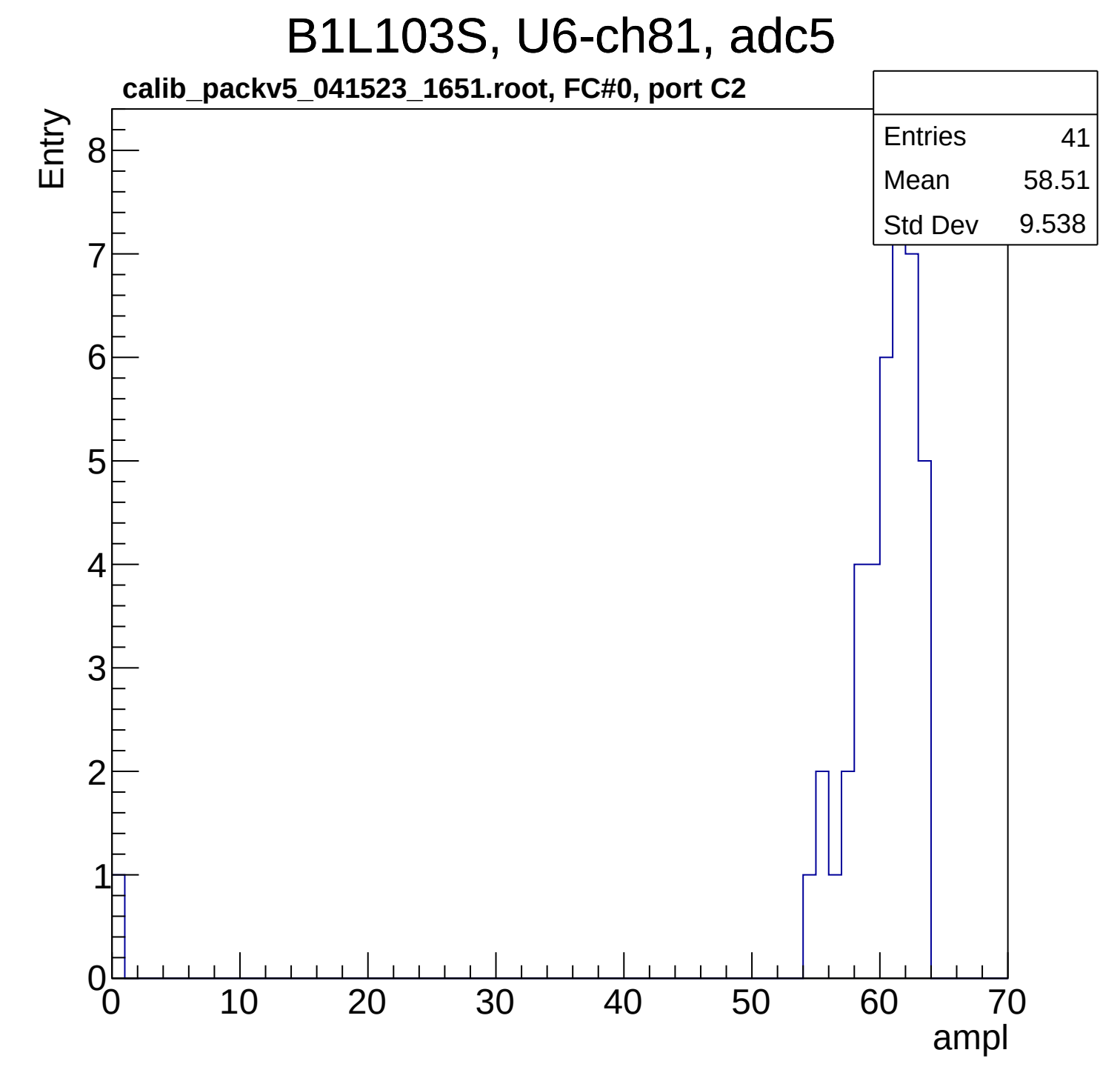
B1L103S, U6-ch81, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 58.51
Std Dev 9.538
Entry
ampl
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0
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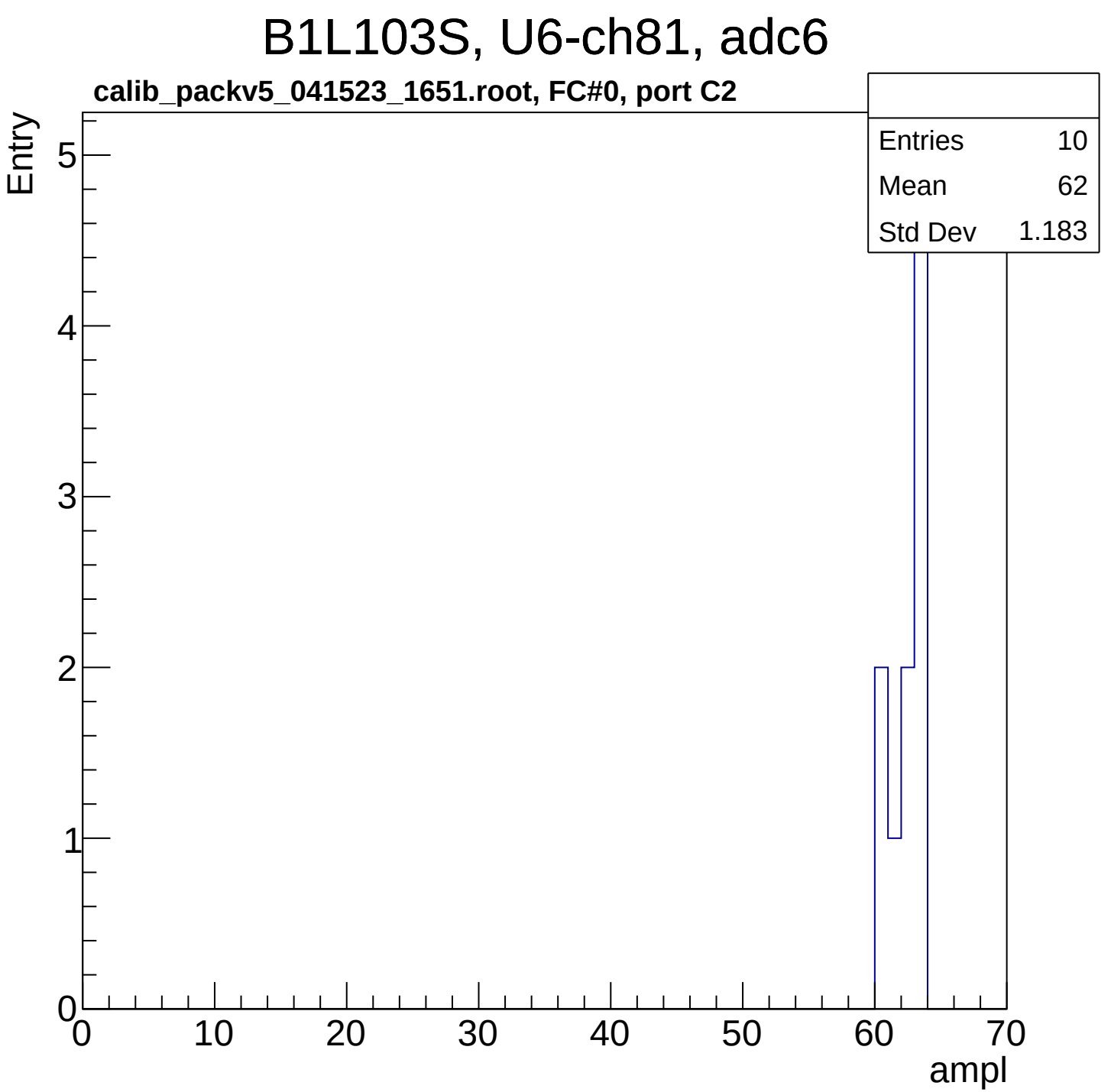
B1L103S, U6-ch81, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 62
Std Dev 1.183
Entry
0
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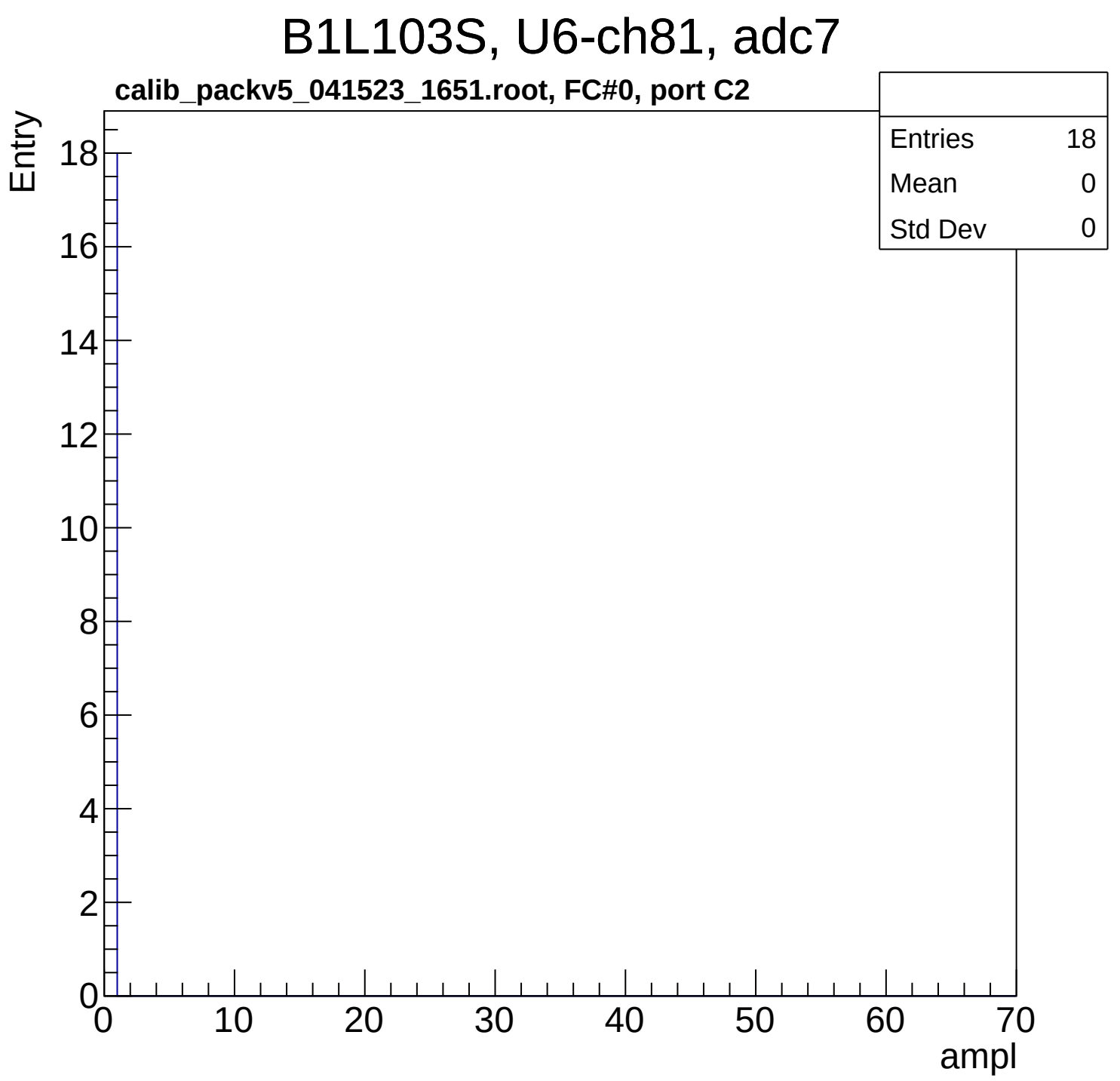
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch81, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
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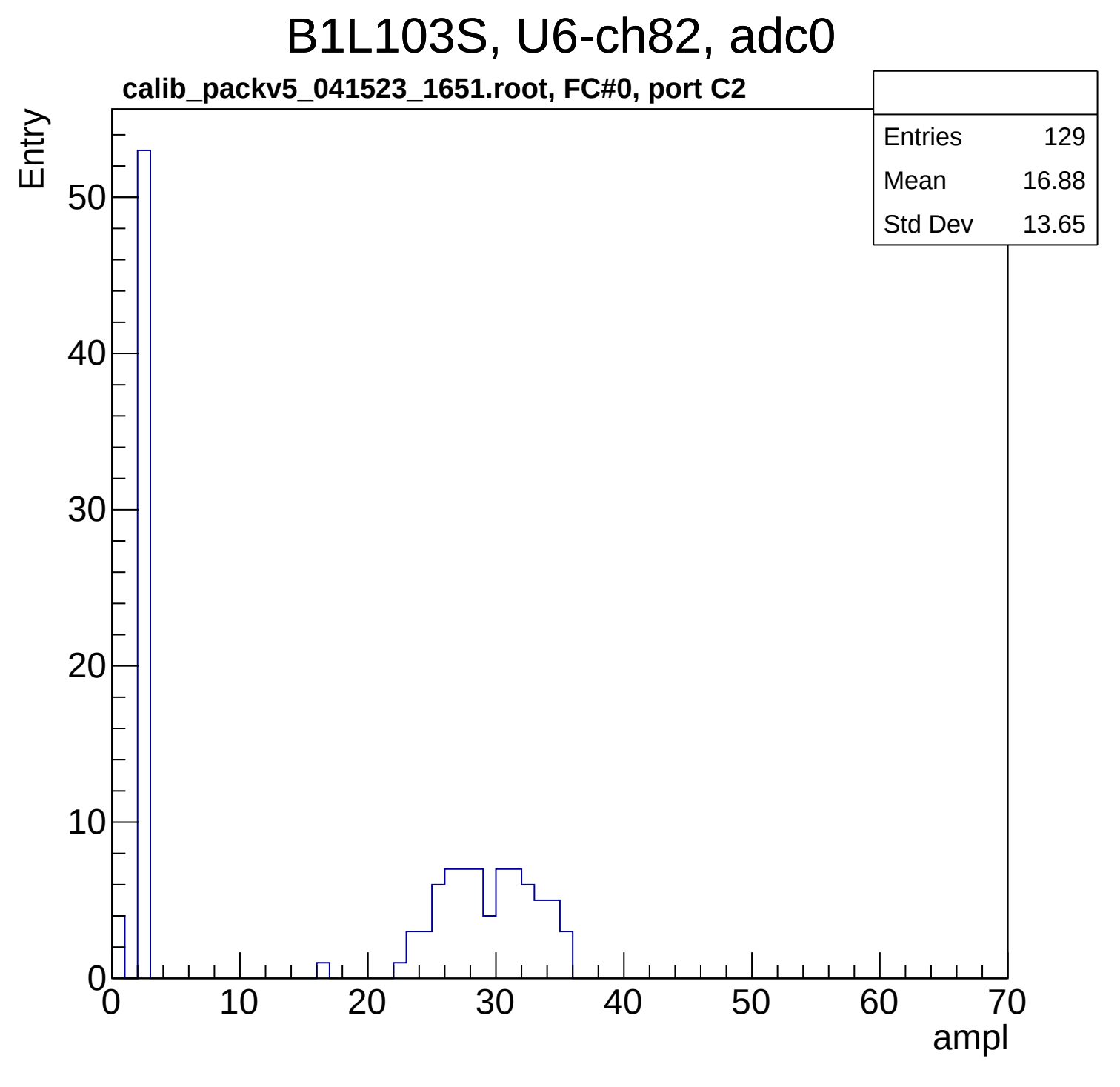
50
60
70
ampl


B1L103S, U6-ch82, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 129
Mean 16.88
Std Dev 13.65
Entry
0
10
20
30
40
50
0
10
20
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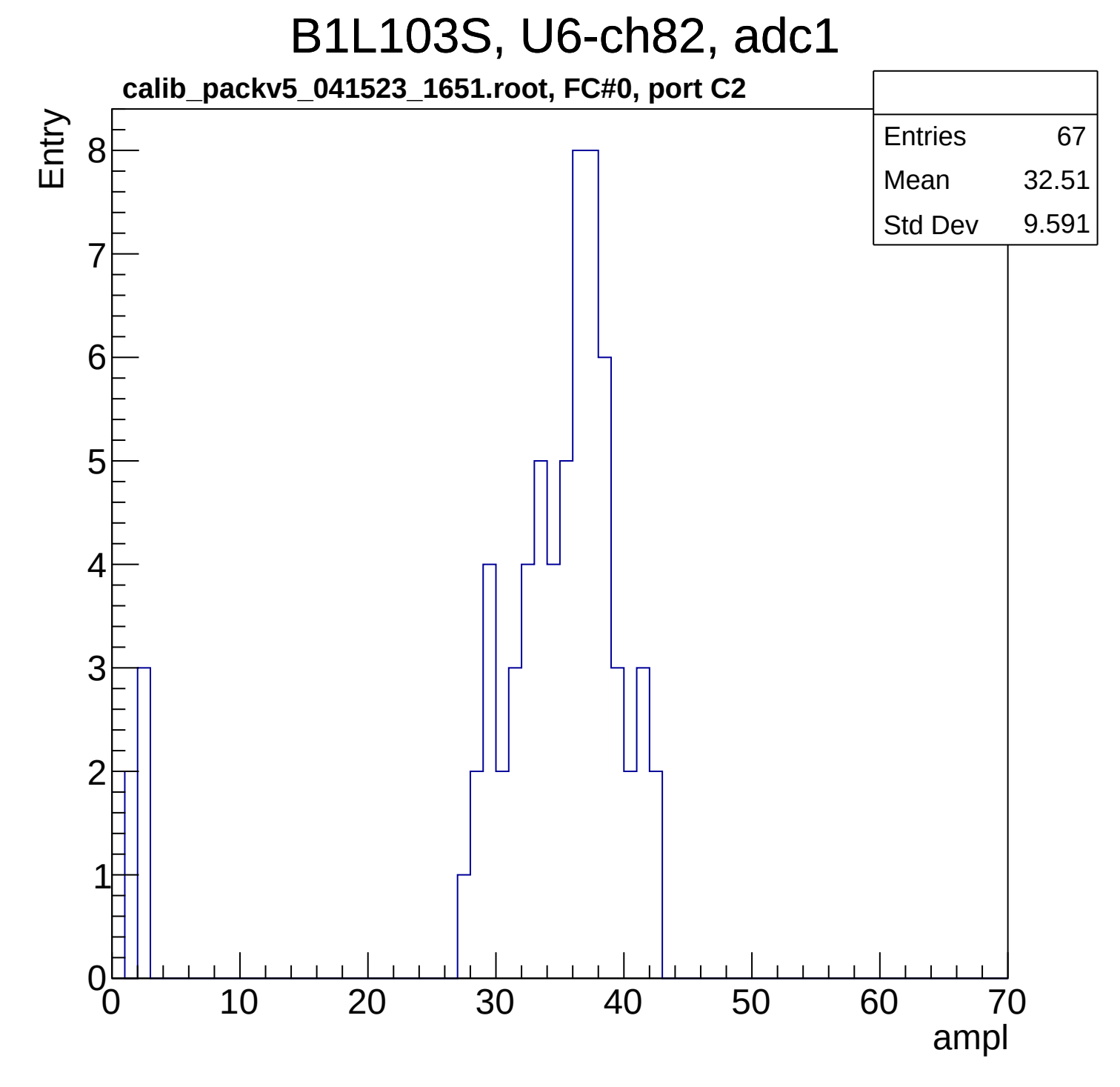
40
50
60
70
ampl


B1L103S, U6-ch82, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 32.51
Std Dev 9.591
Entry
ampl
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2
3
4
5
6
7
8
0
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40
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60
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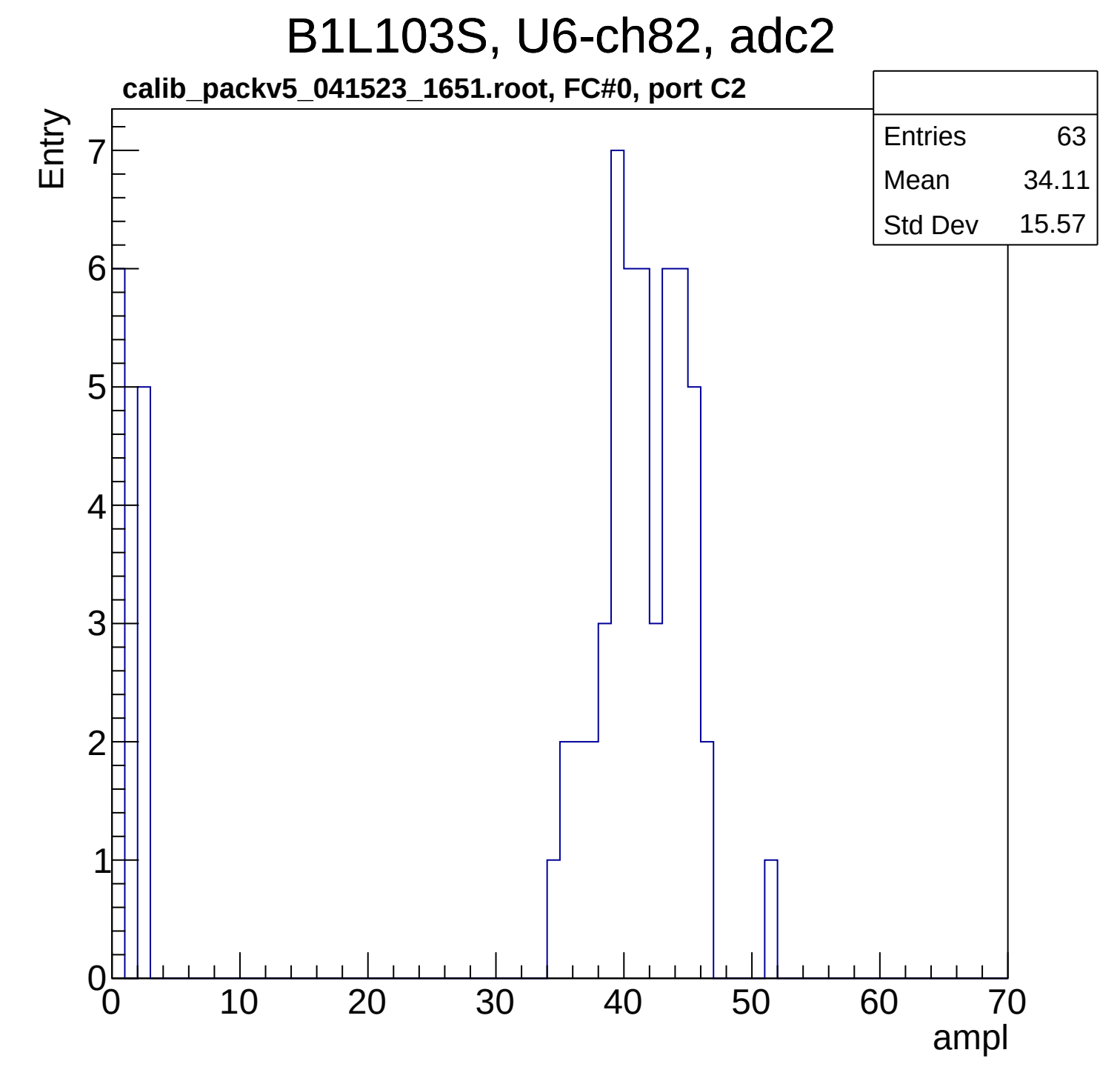
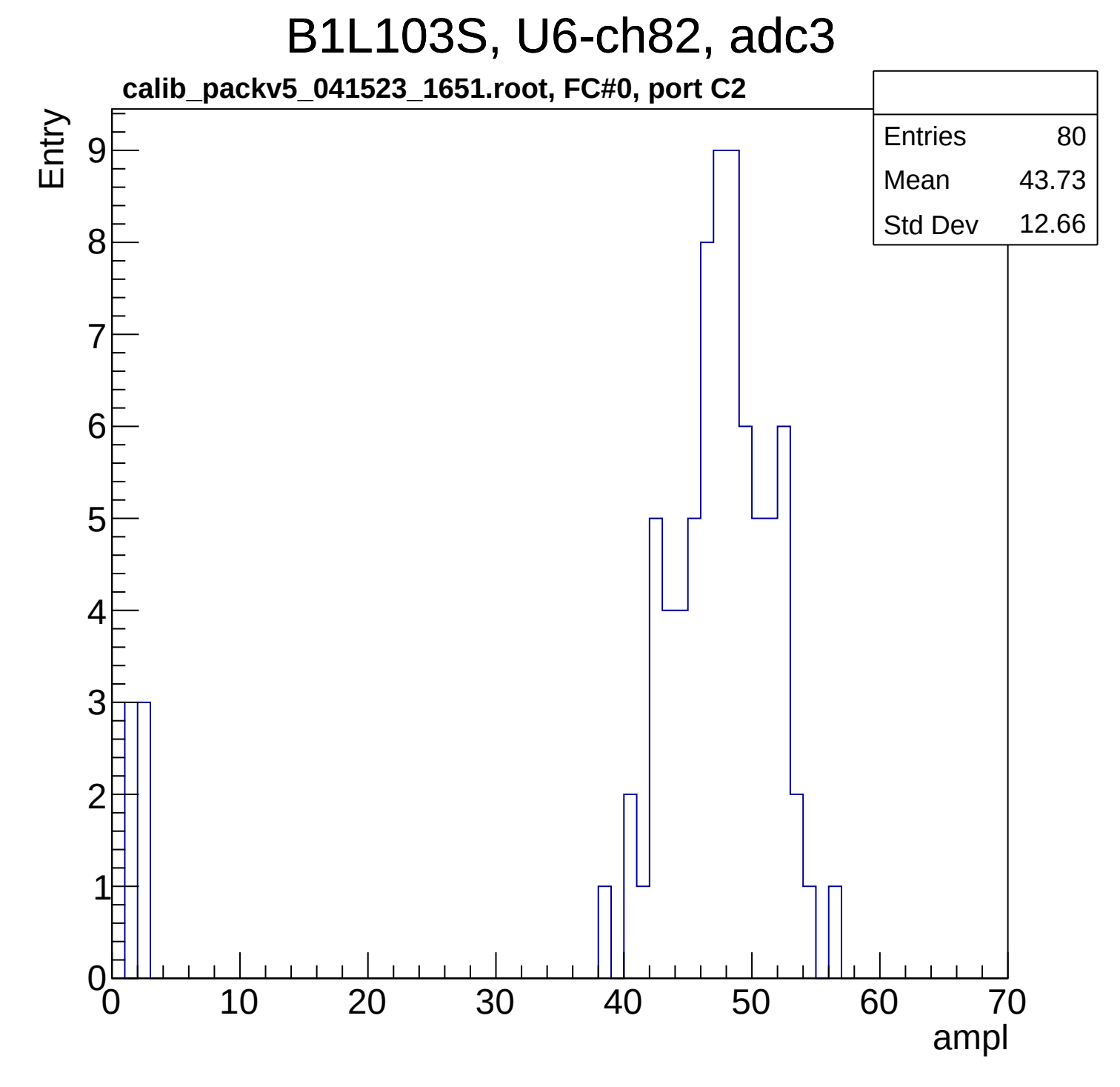
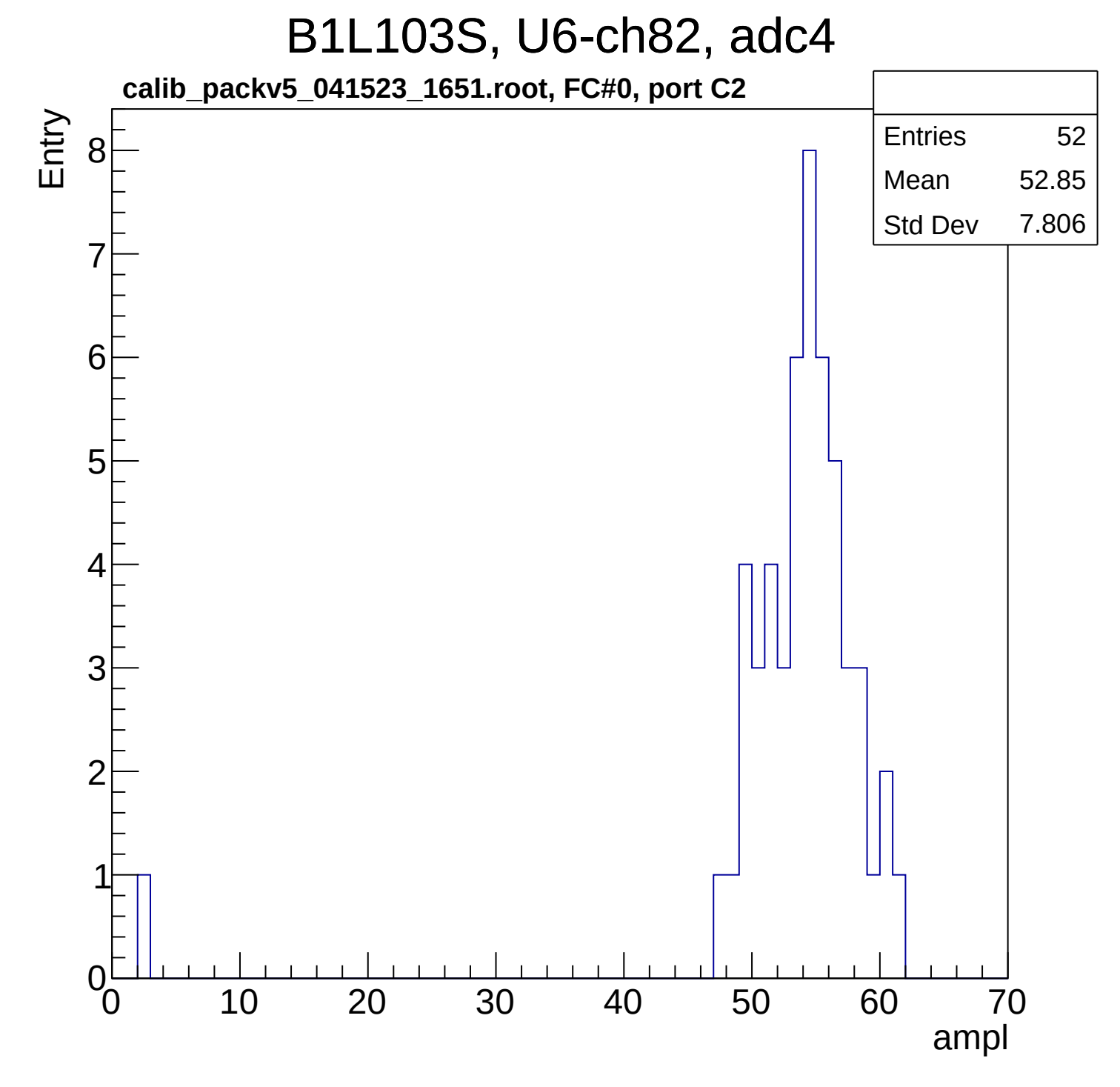
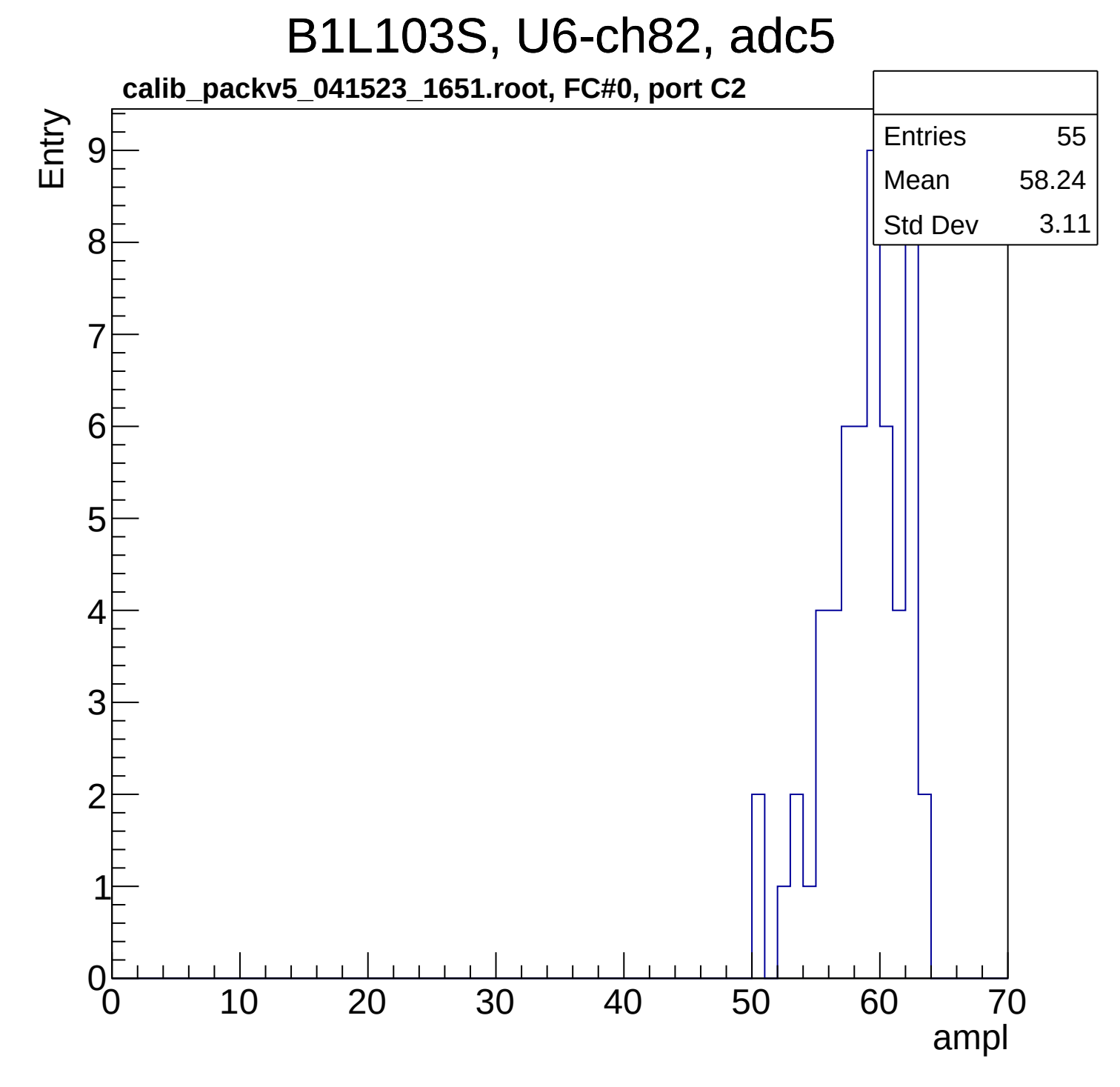
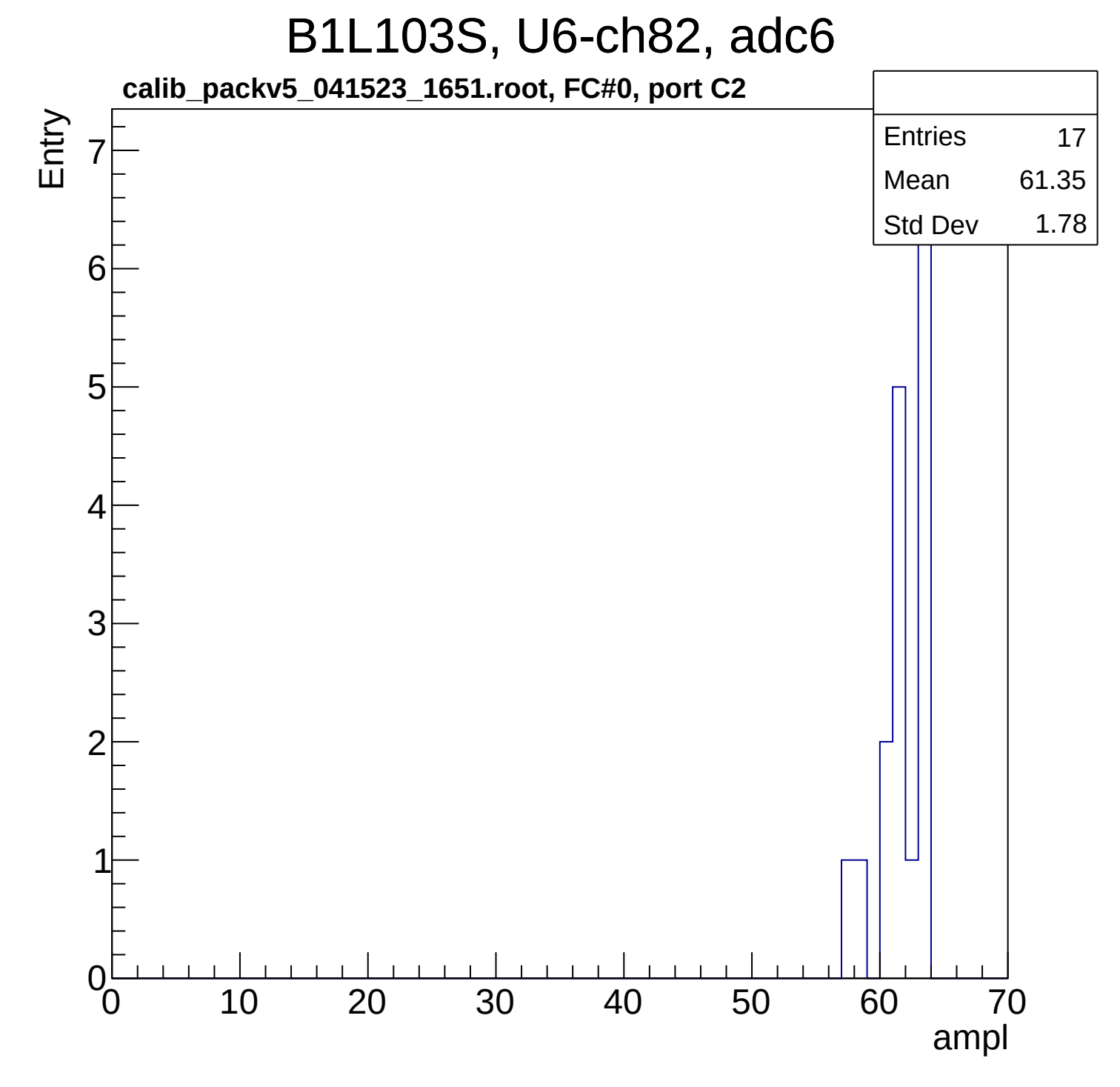
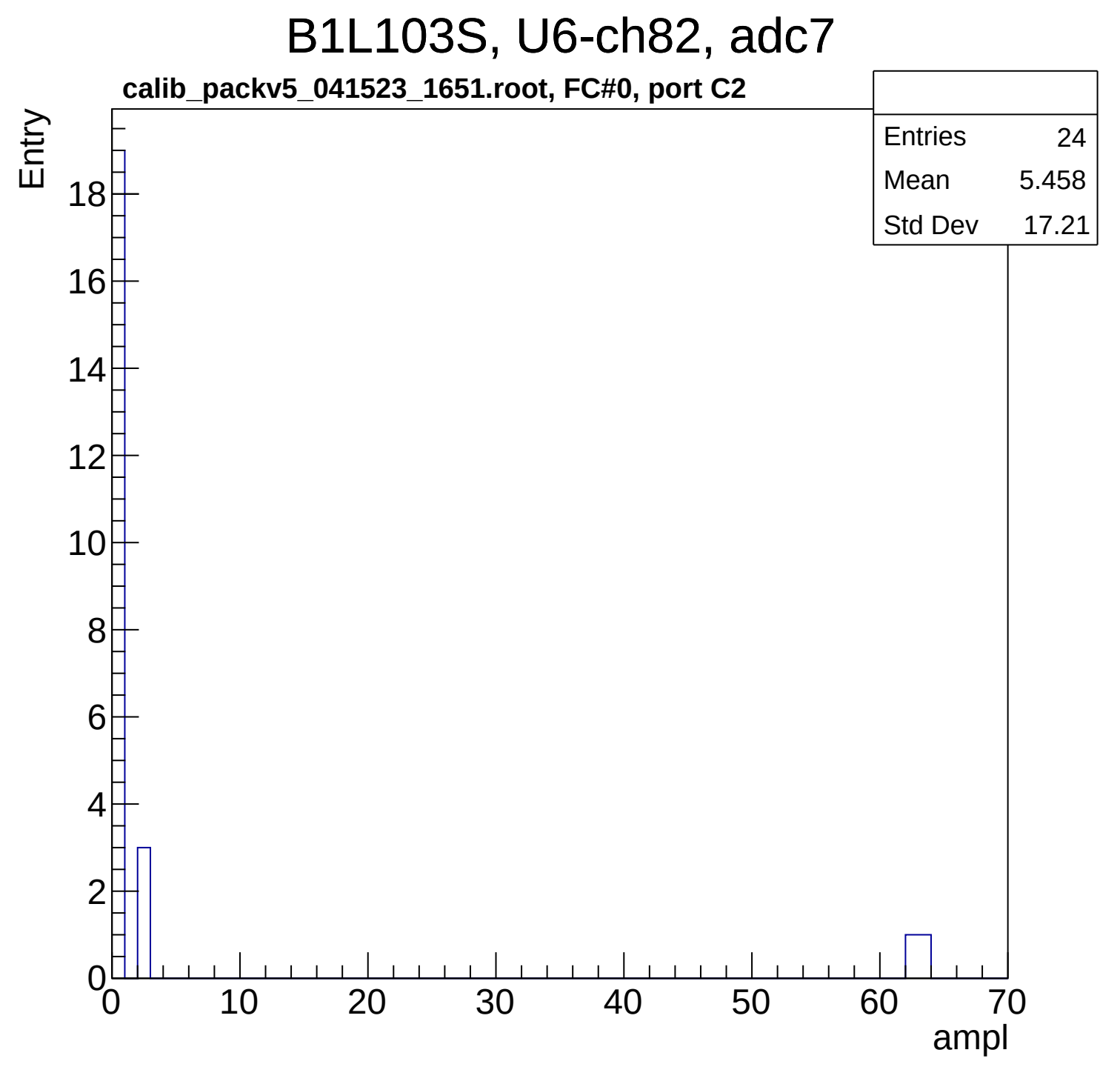

B1L103S, U6-ch82, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 34.11
Std Dev 15.57
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U6-ch82, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 43.73
Std Dev 12.66
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch82, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 52.85
Std Dev 7.806
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch82, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 58.24
Std Dev 3.11
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch82, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 61.35
Std Dev 1.78
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U6-ch82, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 5.458
Std Dev 17.21
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
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40
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60
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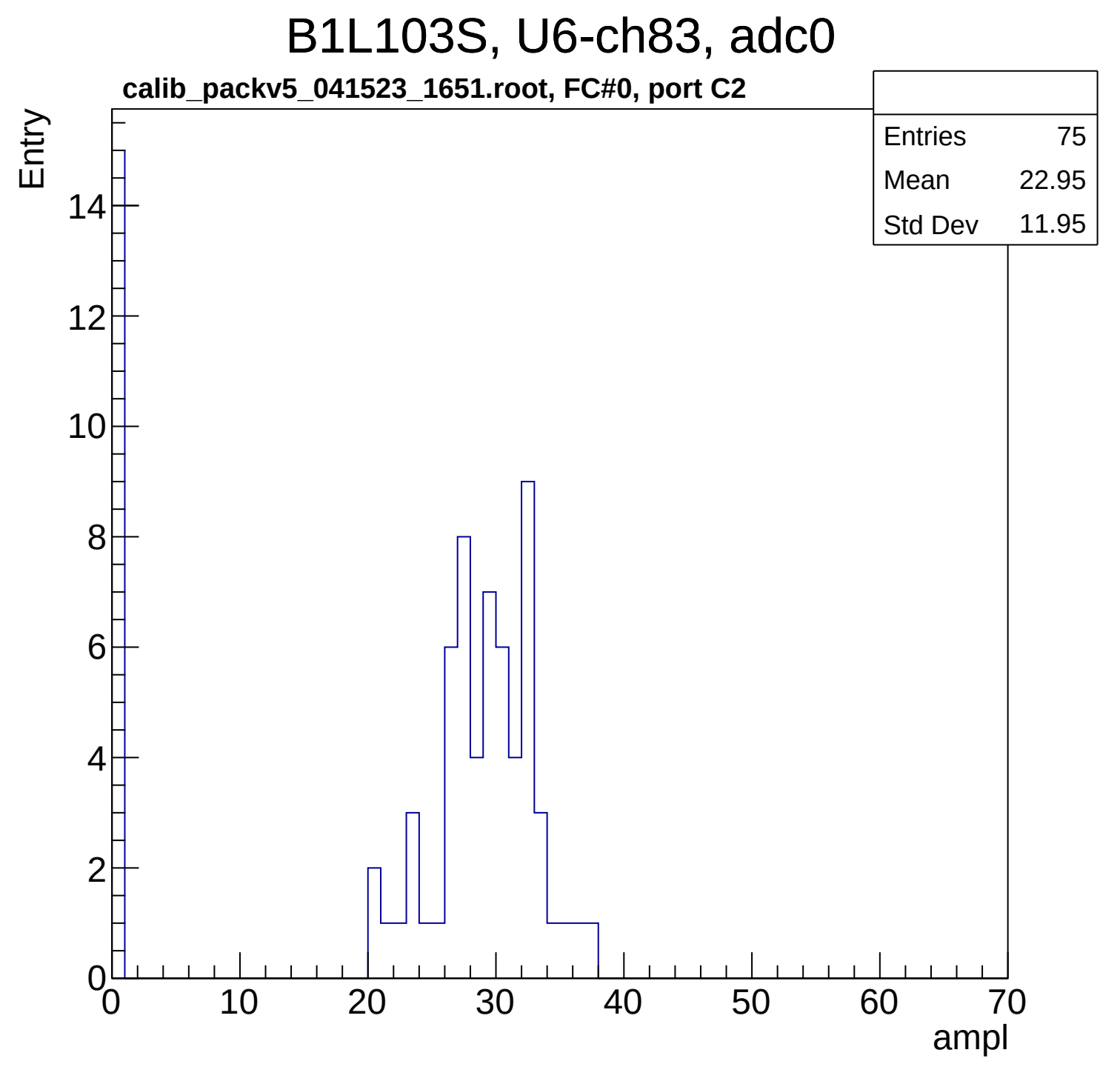
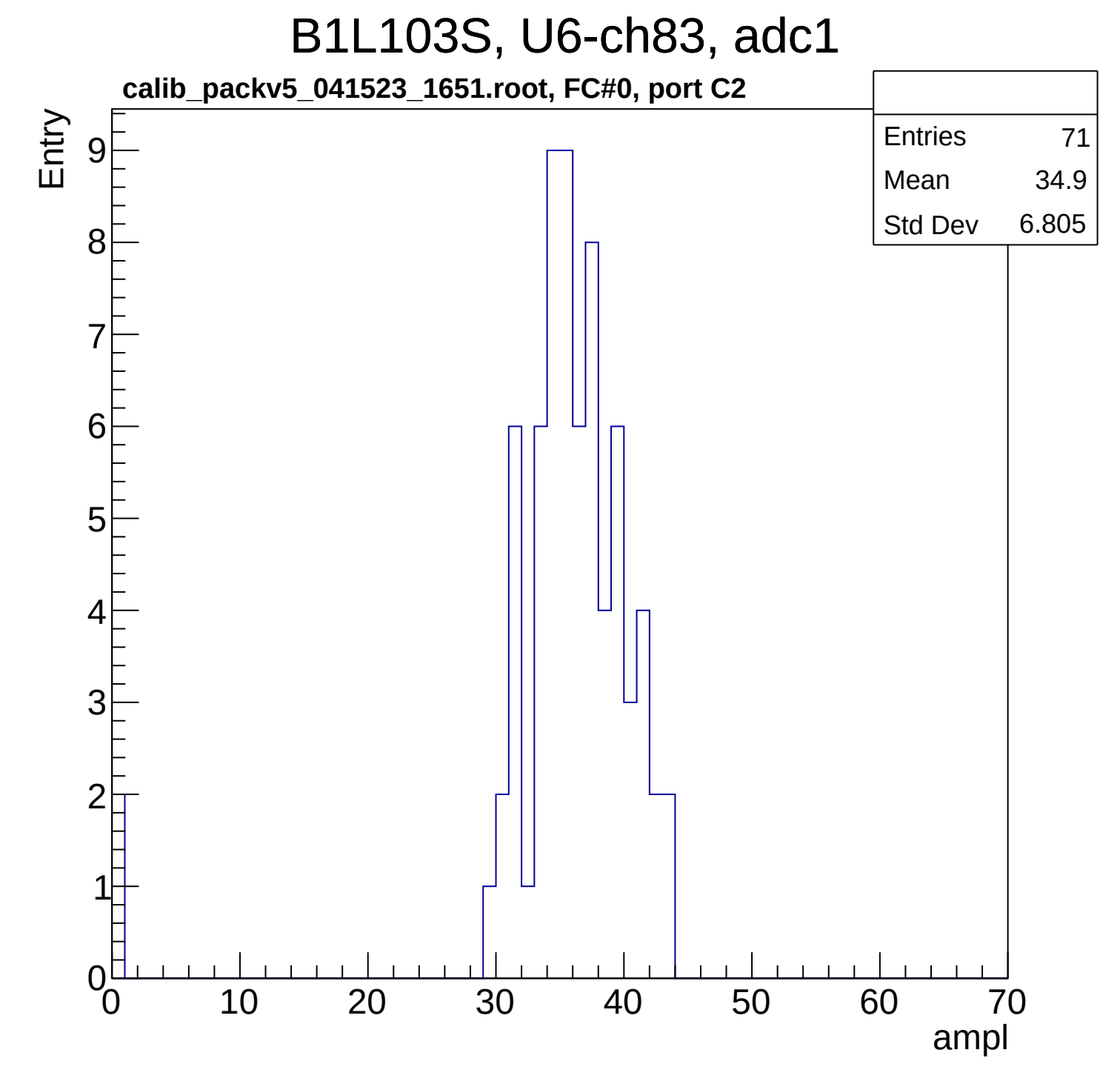

B1L103S, U6-ch83, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 22.95
Std Dev 11.95
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch83, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 34.9
Std Dev 6.805
Entry
ampl
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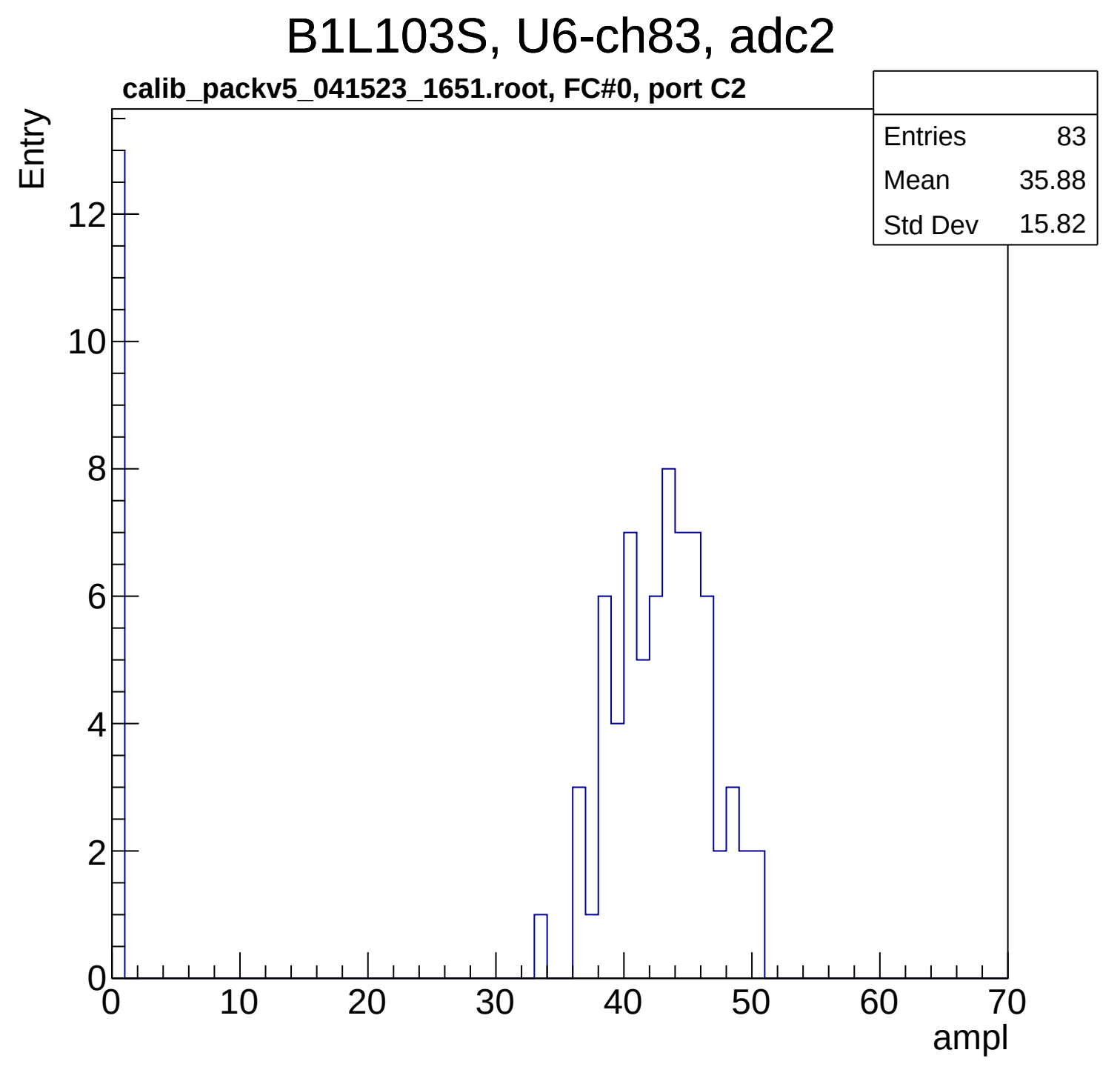
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch83, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 35.88
Std Dev 15.82
Entry
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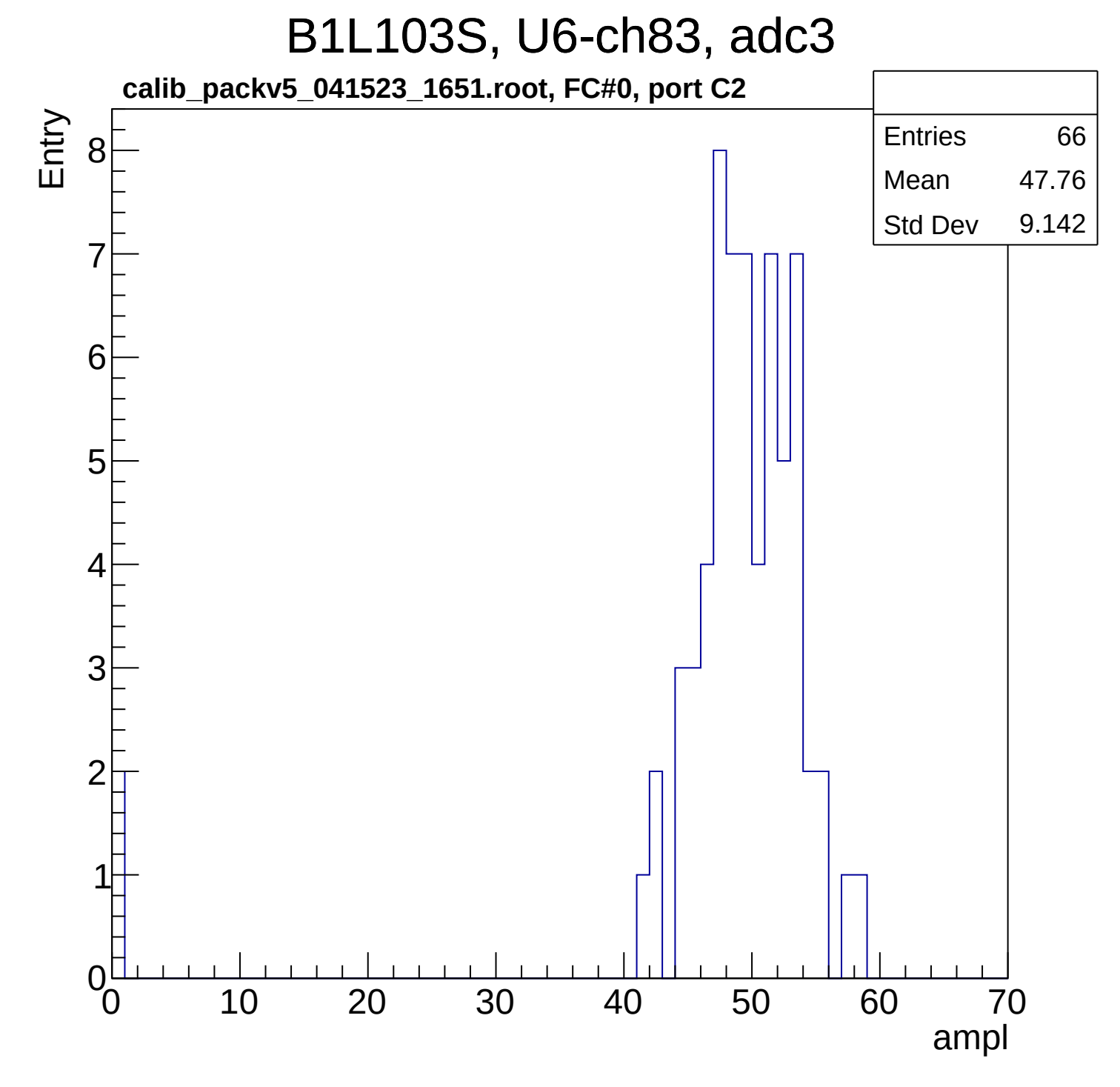
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch83, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 47.76
Std Dev 9.142
Entry
ampl
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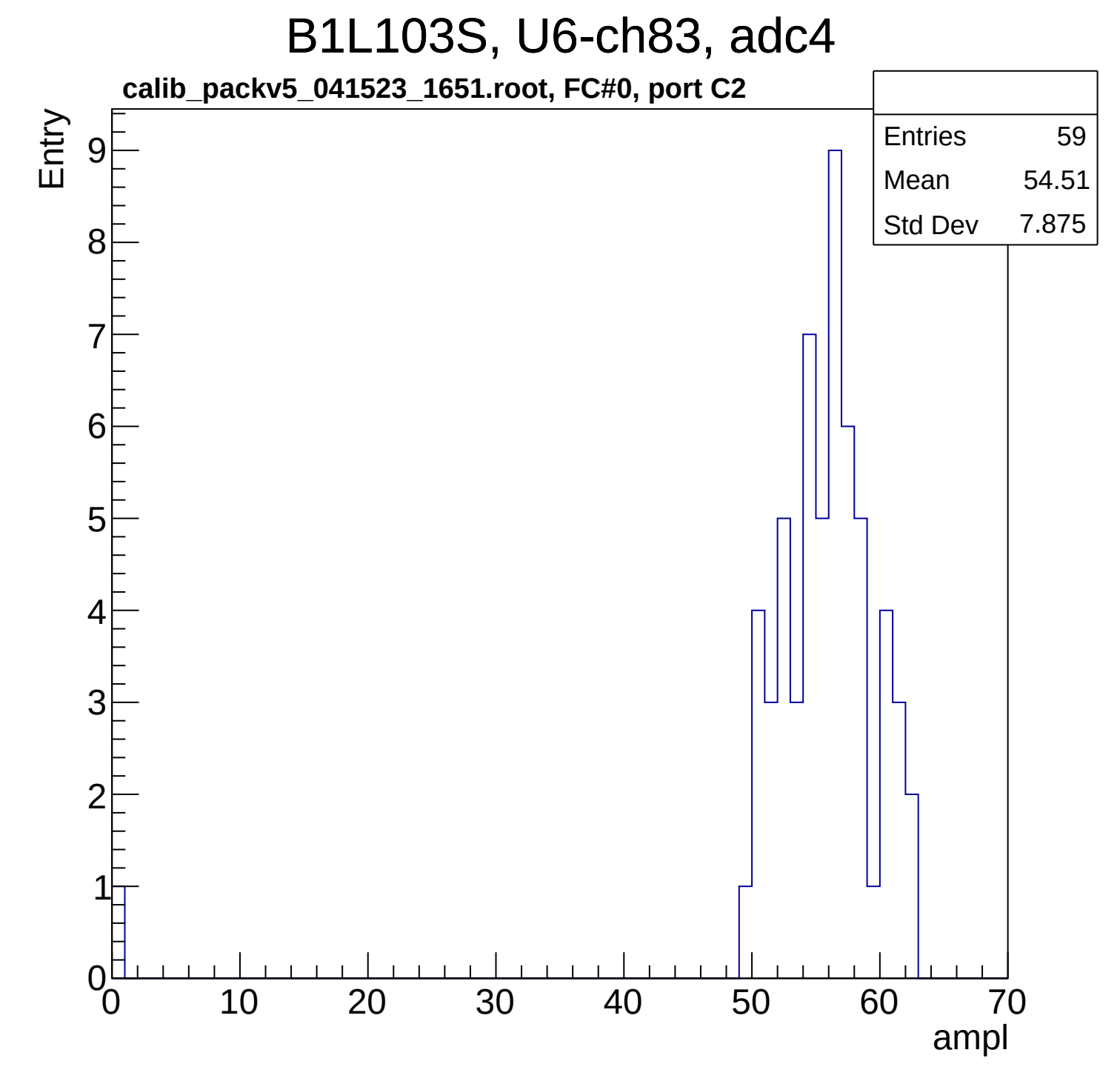
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch83, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 54.51
Std Dev 7.875
Entry
ampl
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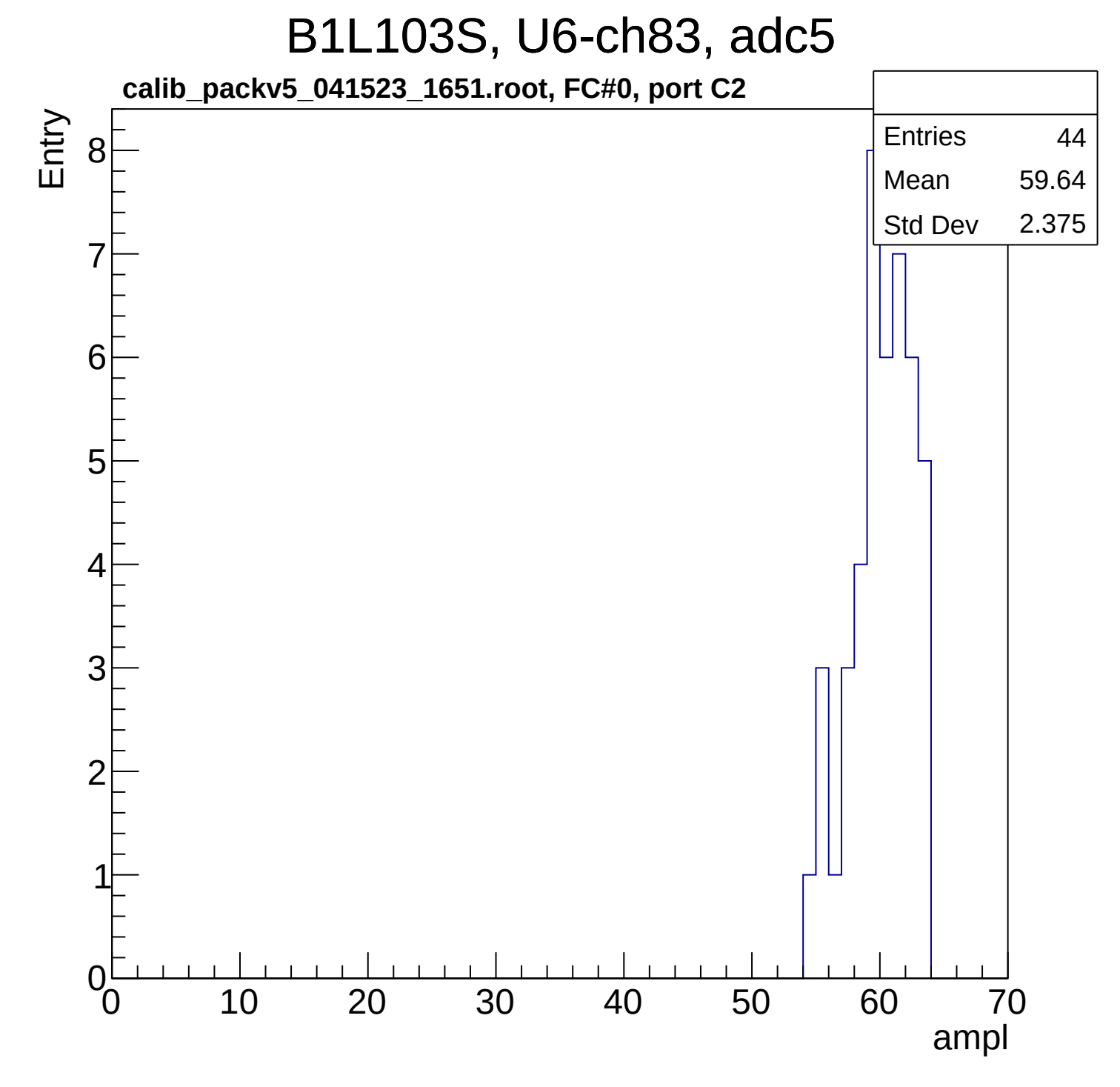
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch83, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 59.64
Std Dev 2.375
Entry
ampl
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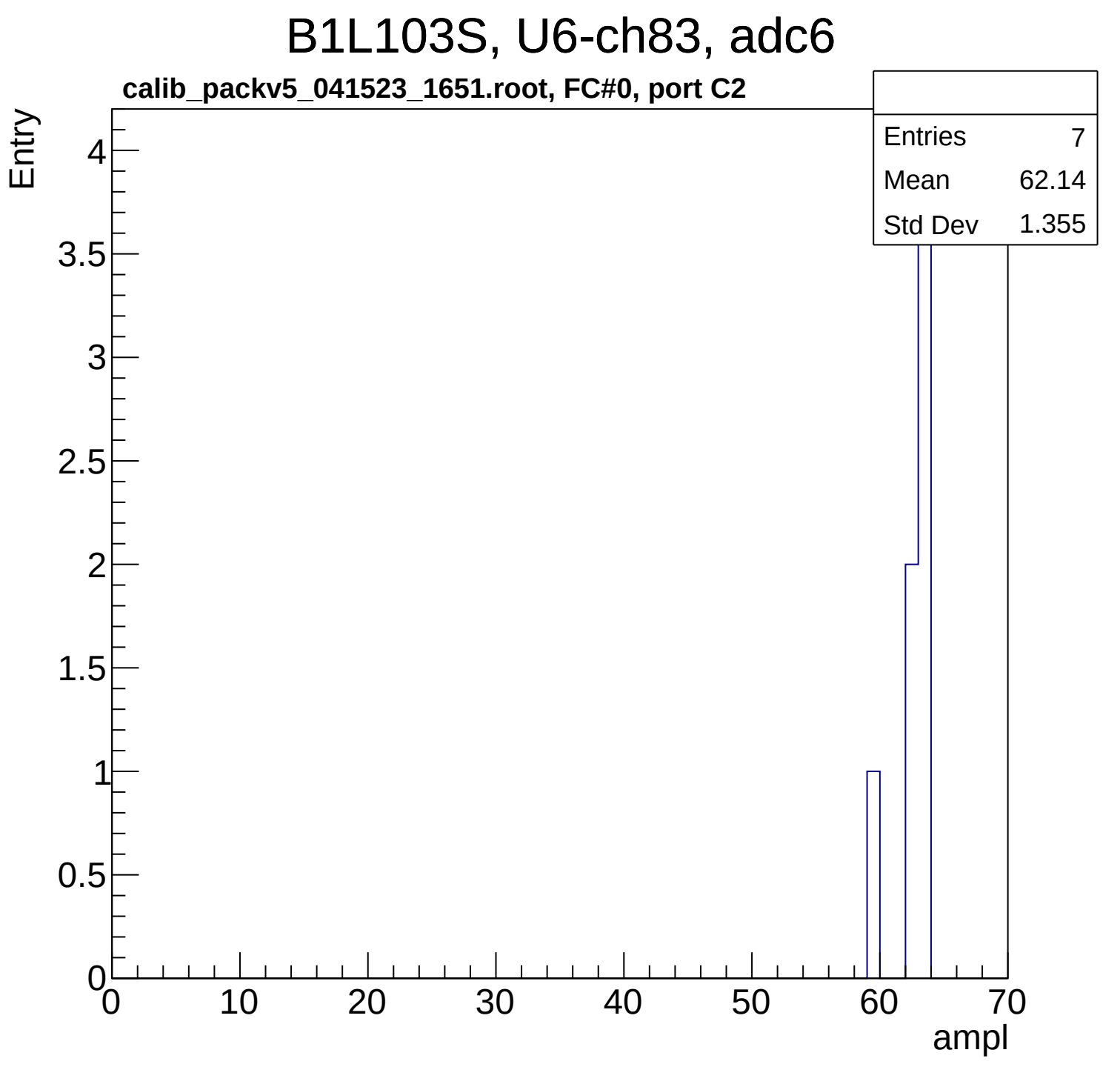
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch83, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 62.14
Std Dev 1.355
Entry
ampl
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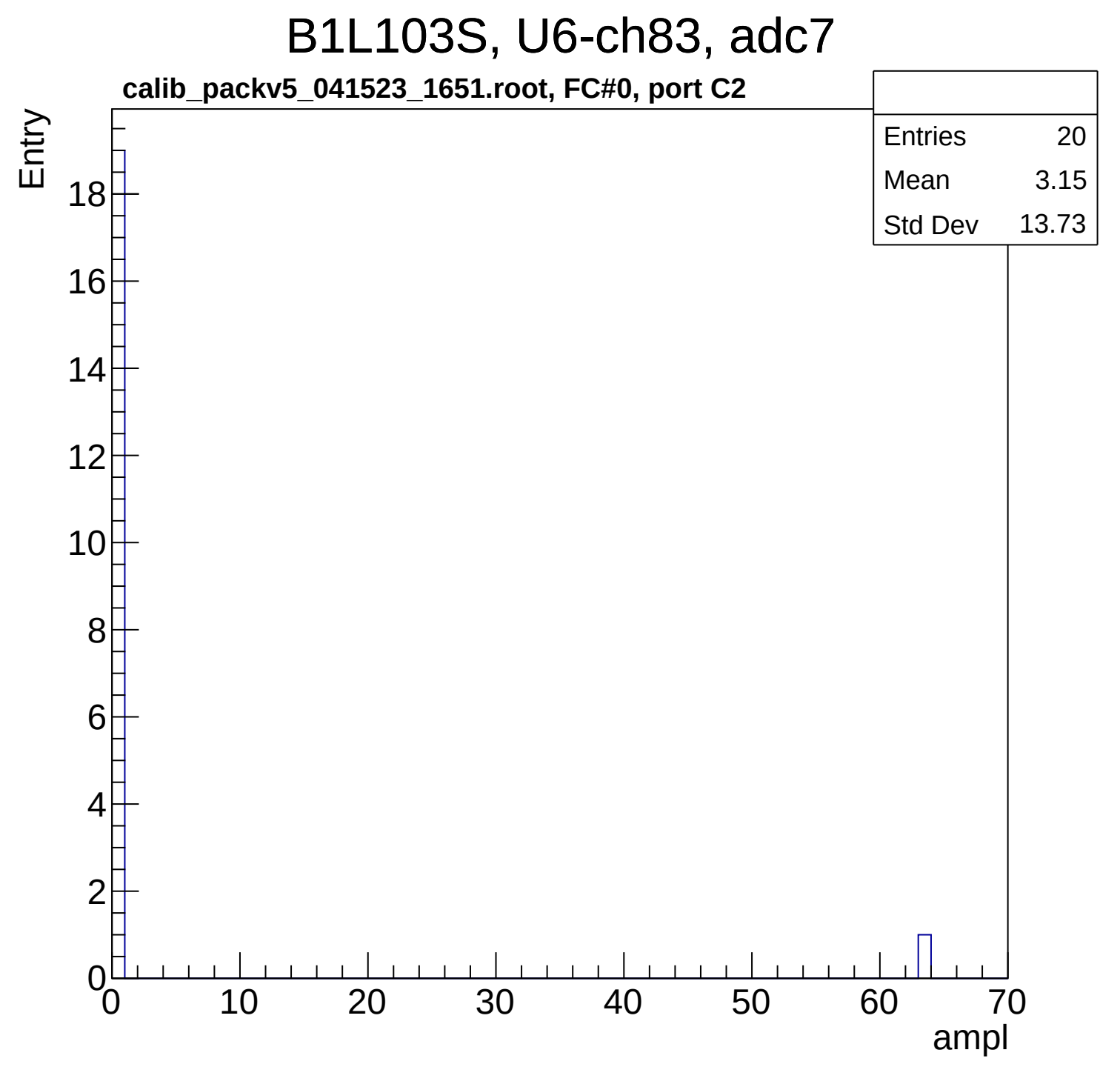
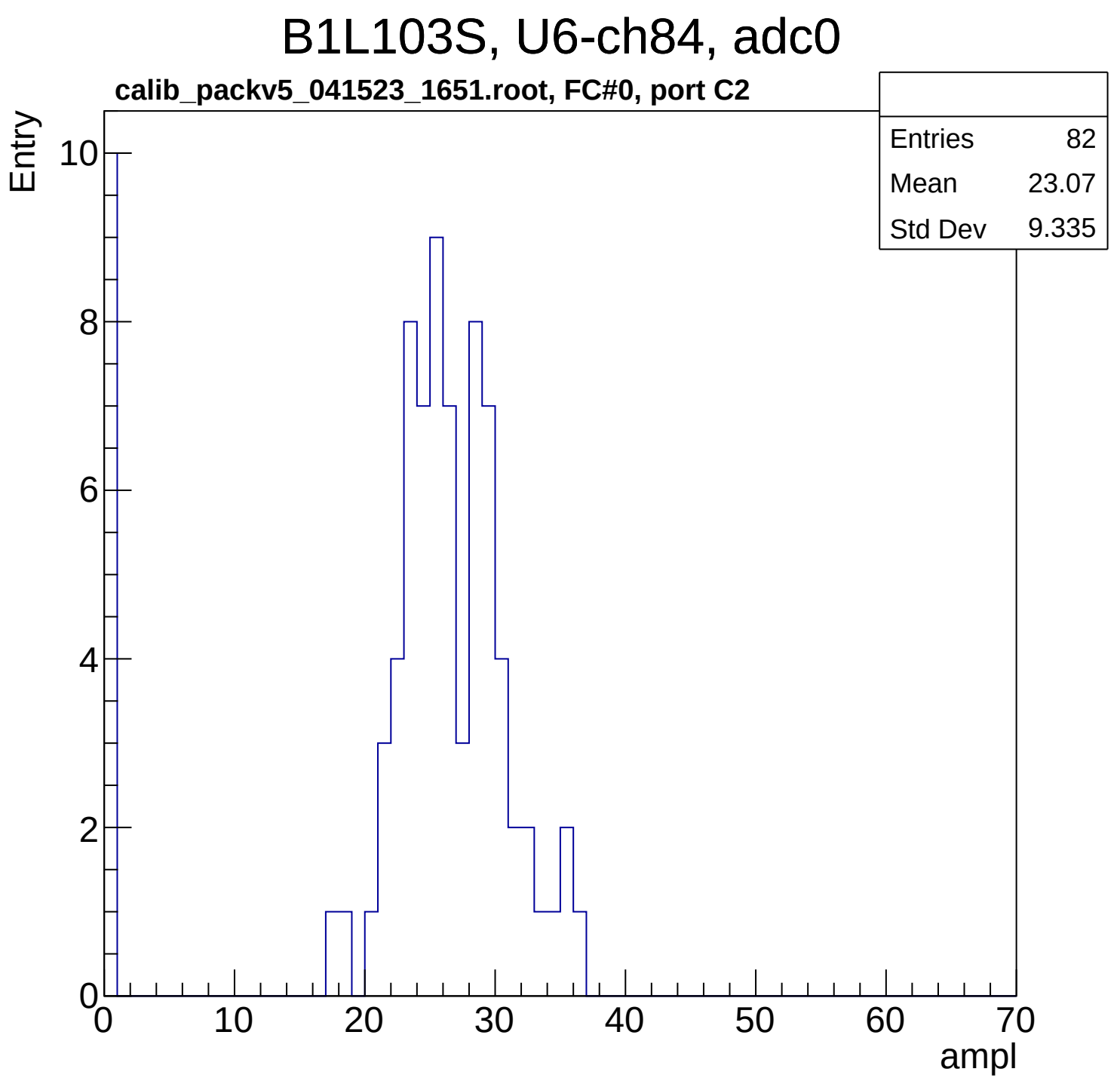
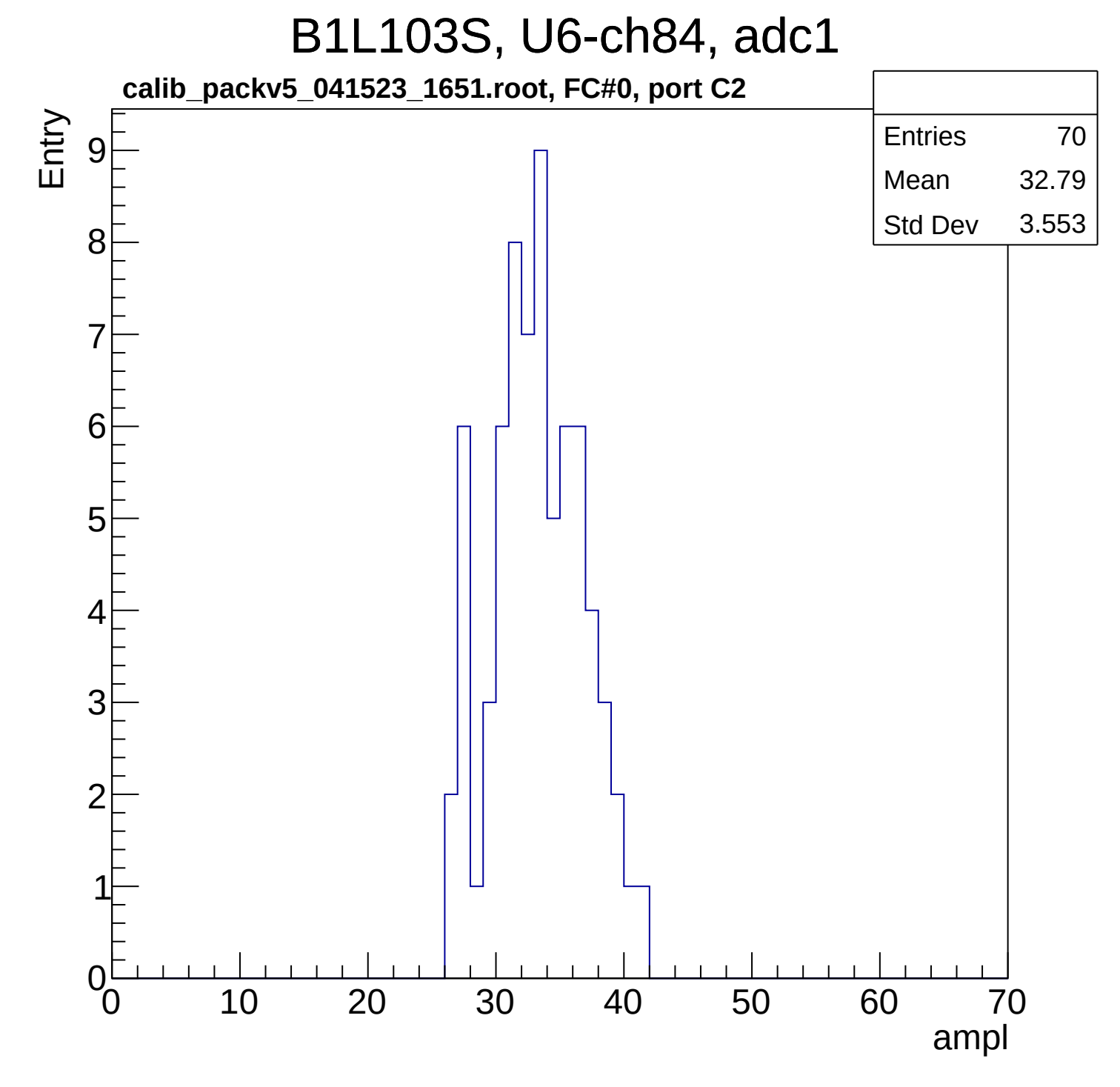
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U6-ch83, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch84, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 23.07
Std Dev 9.335
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U6-ch84, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 32.79
Std Dev 3.553
Entry
ampl
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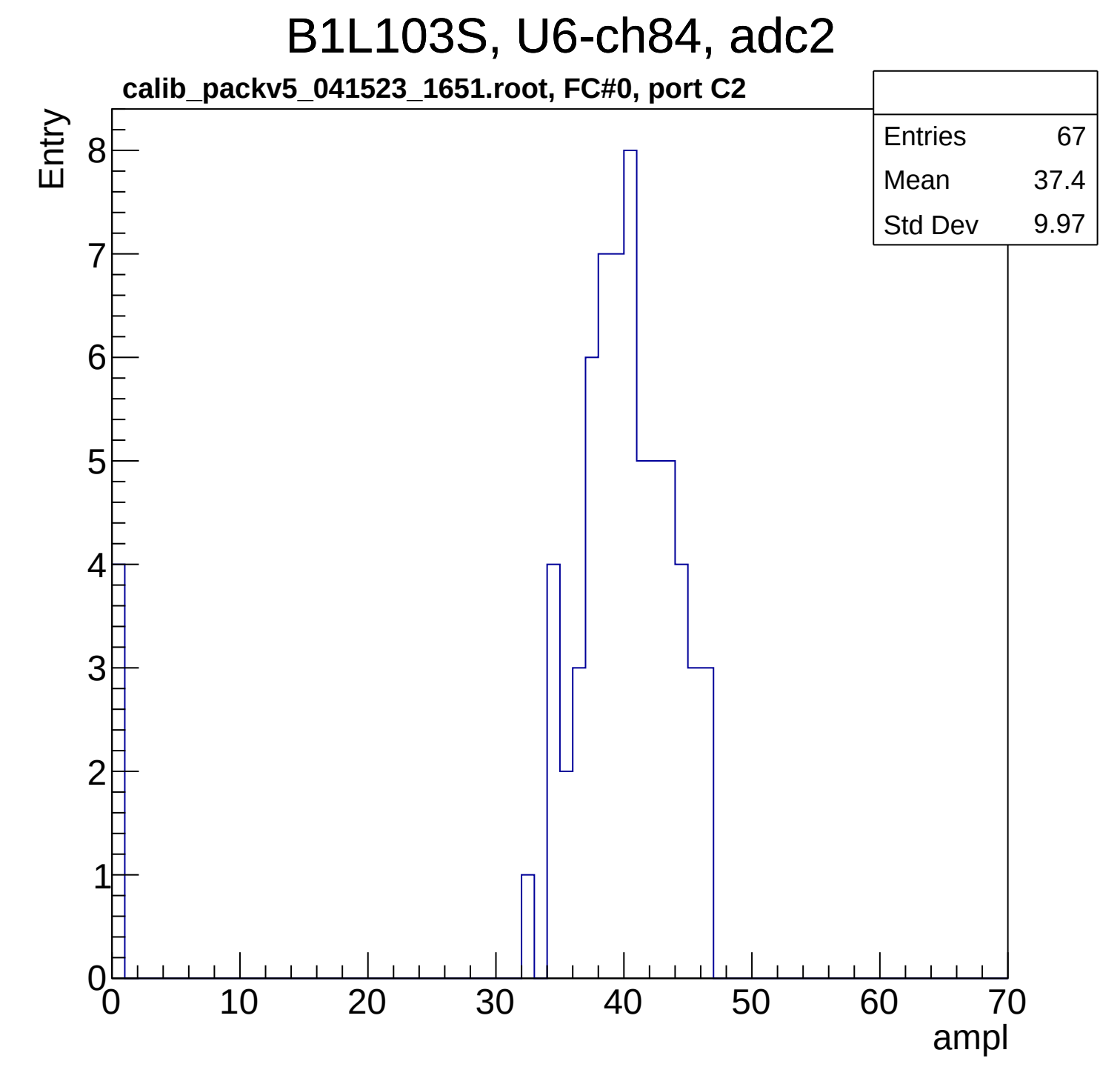
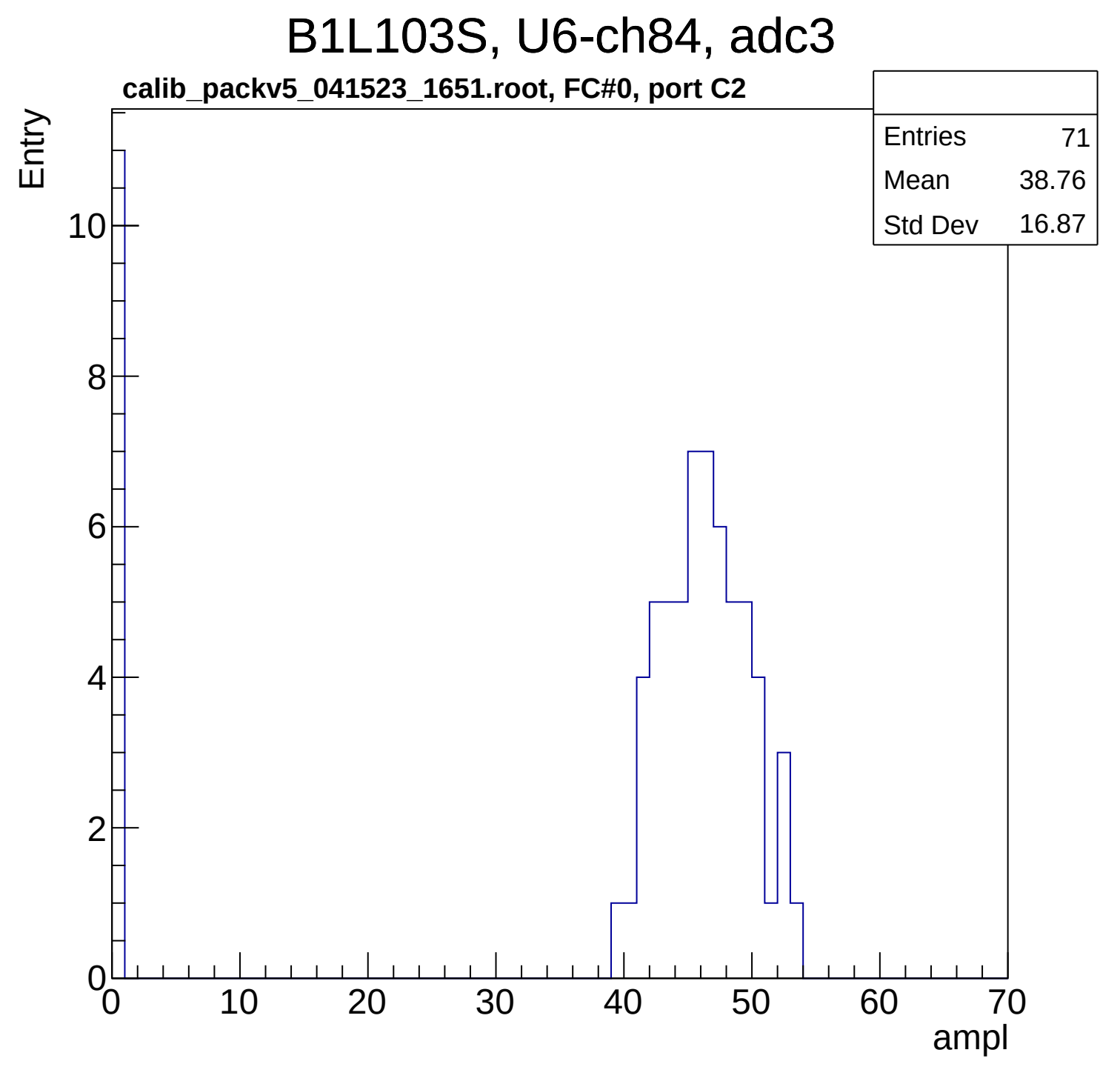
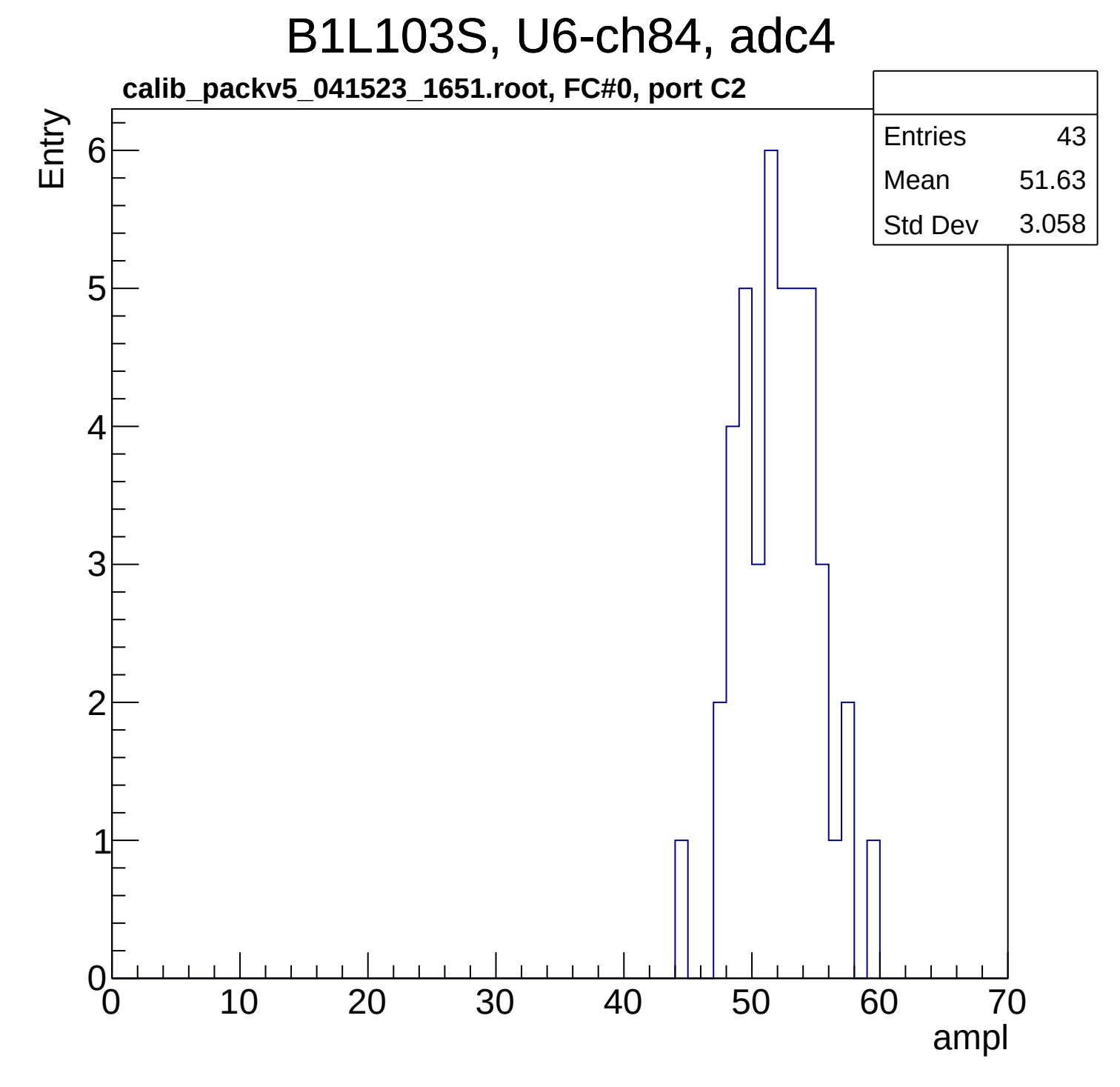
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch84, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 37.4
Std Dev 9.97
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch84, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 38.76
Std Dev 16.87
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch84, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 51.63
Std Dev 3.058
Entry
ampl
0
1
2
3
4
5
6
0
10
20
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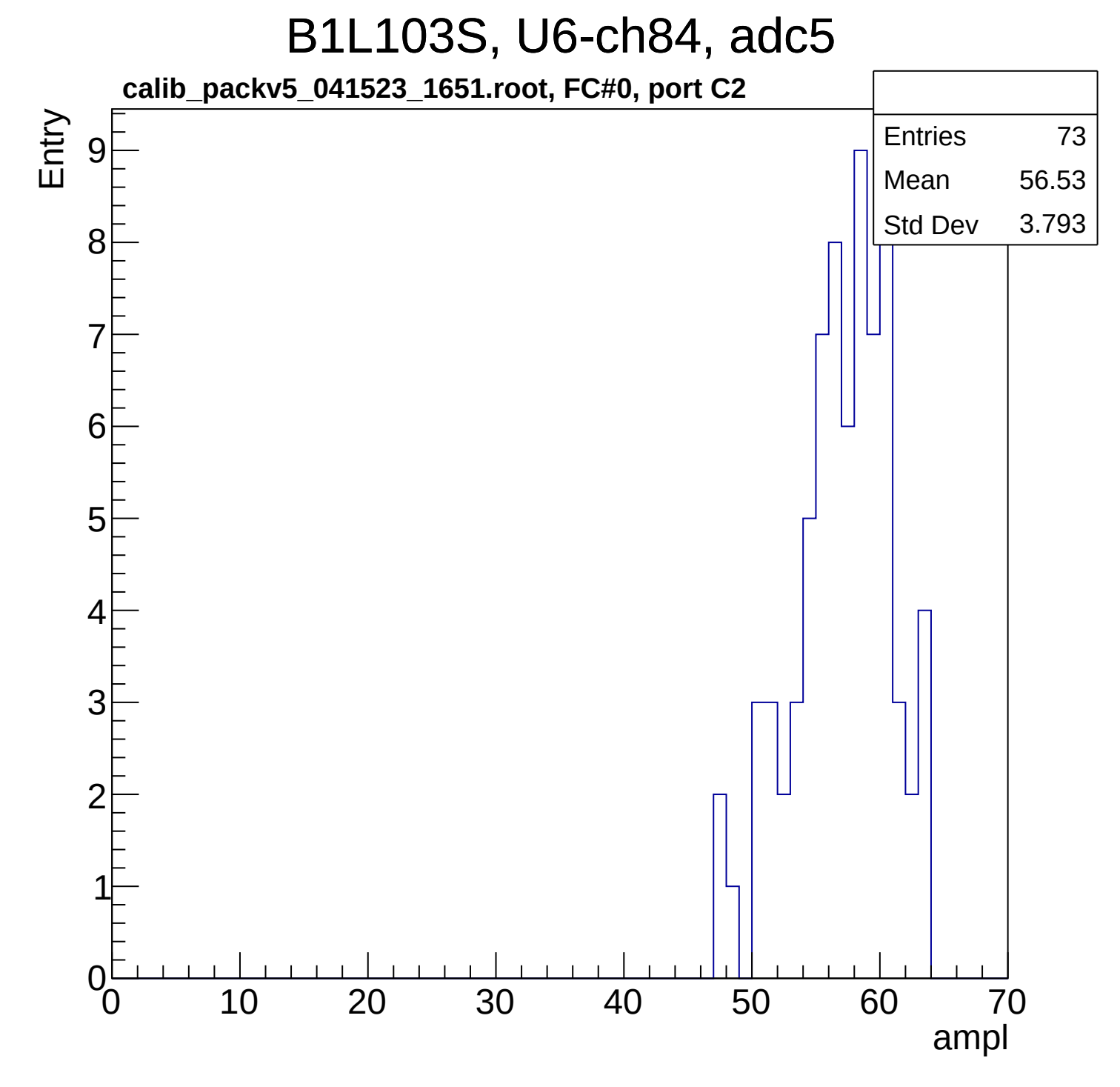
40
50
60
70


B1L103S, U6-ch84, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 56.53
Std Dev 3.793
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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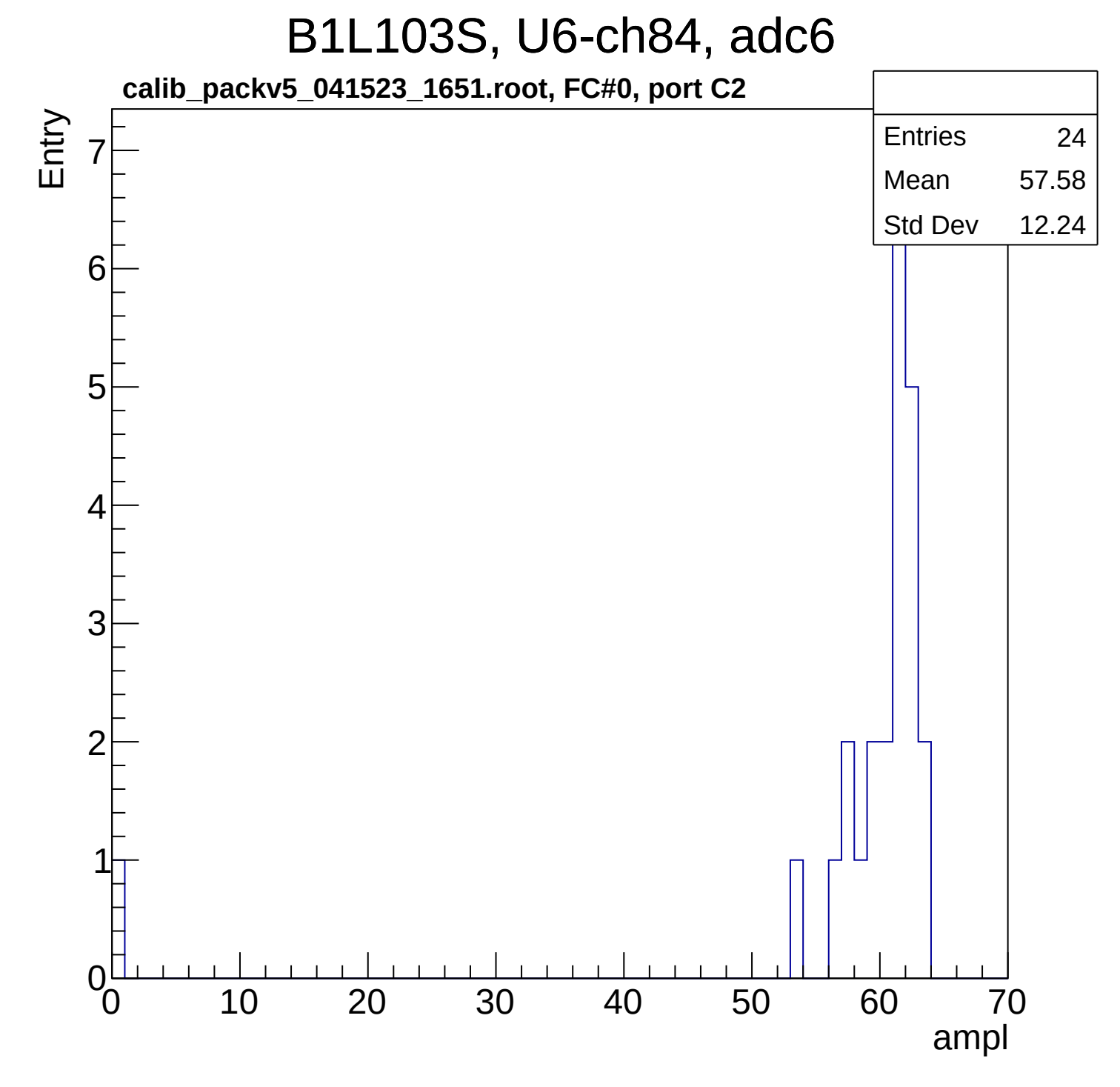
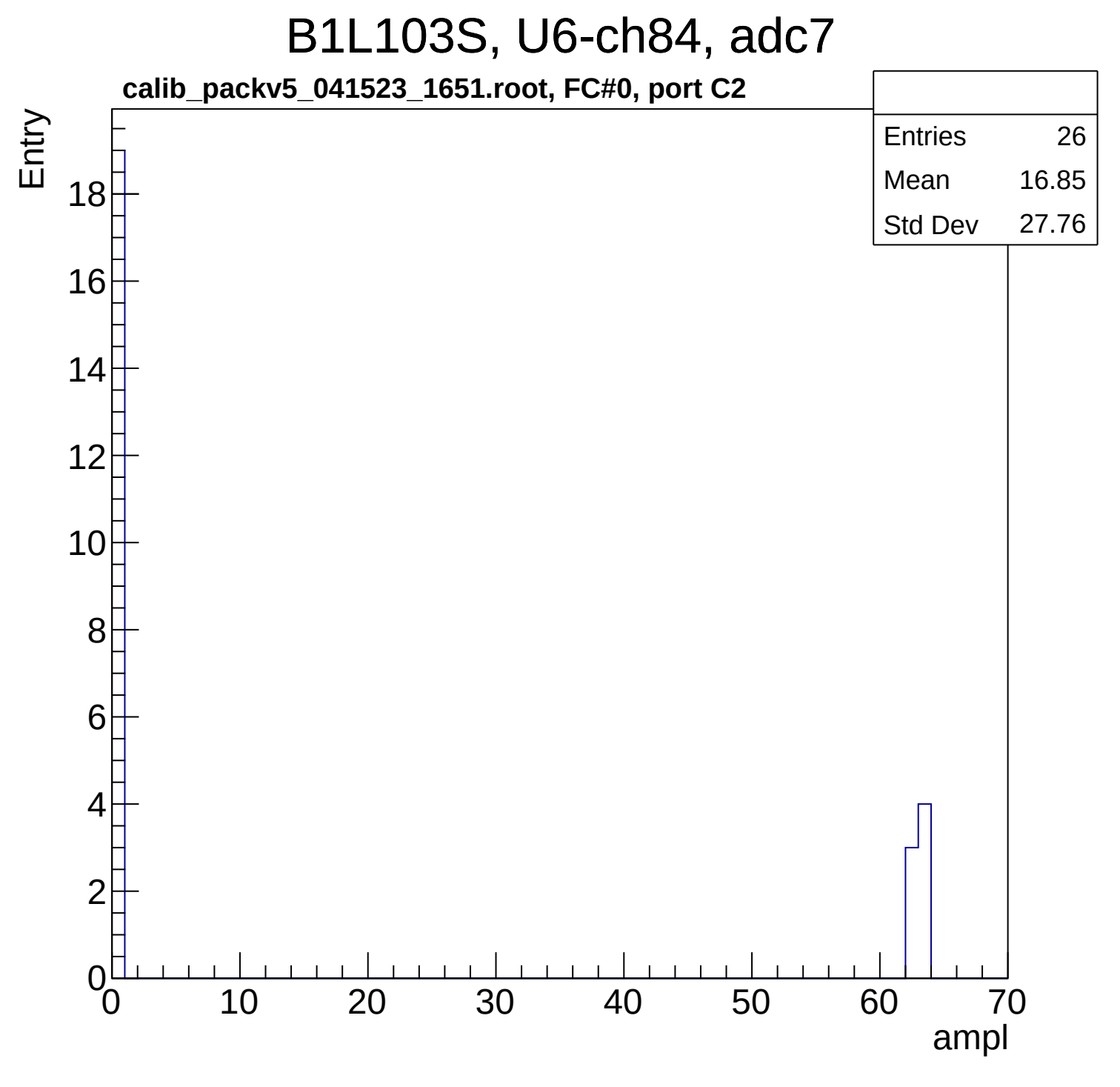
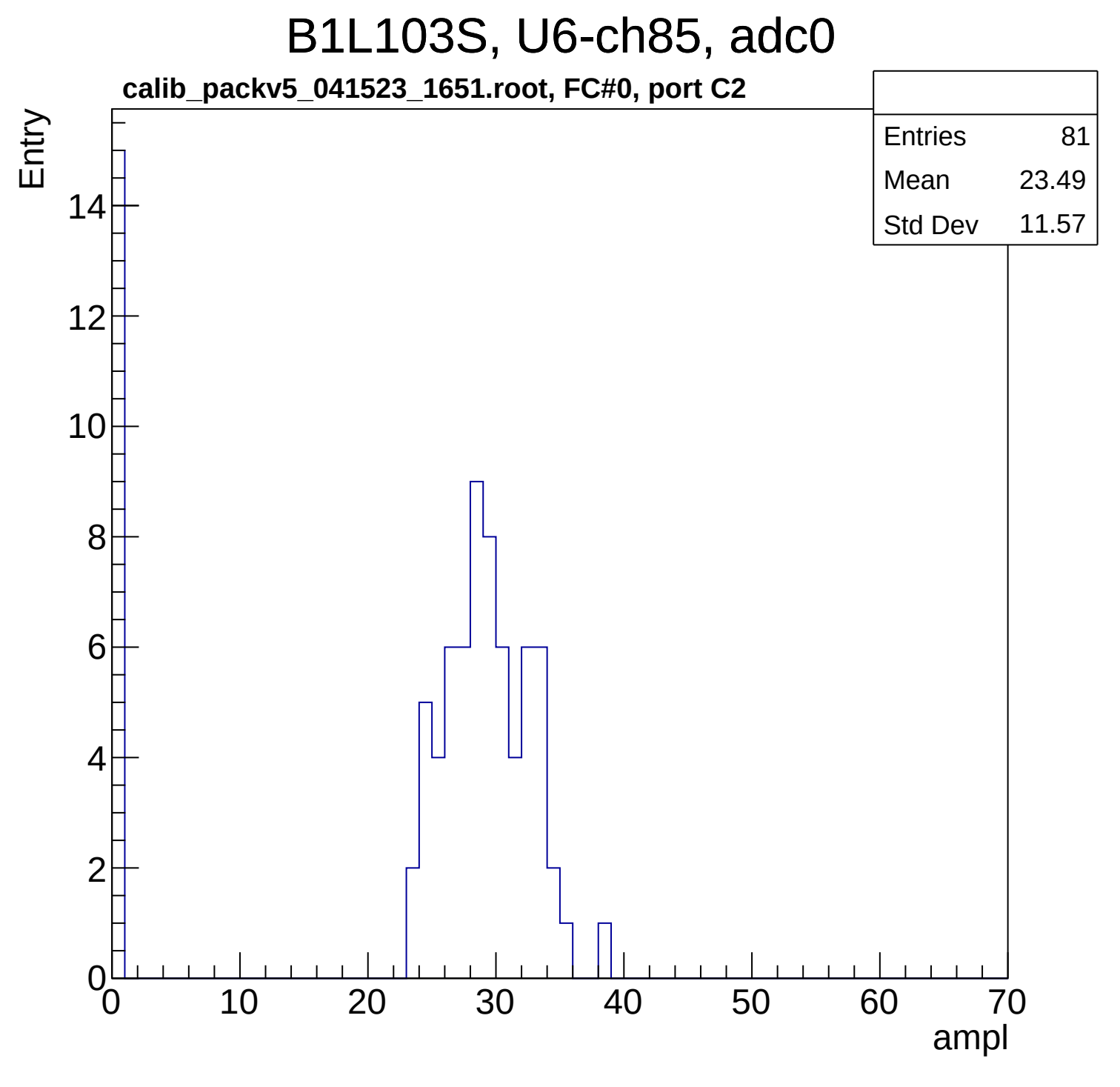
60
70


B1L103S, U6-ch84, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 57.58
Std Dev 12.24
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U6-ch84, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 16.85
Std Dev 27.76
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch85, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 23.49
Std Dev 11.57
Entry
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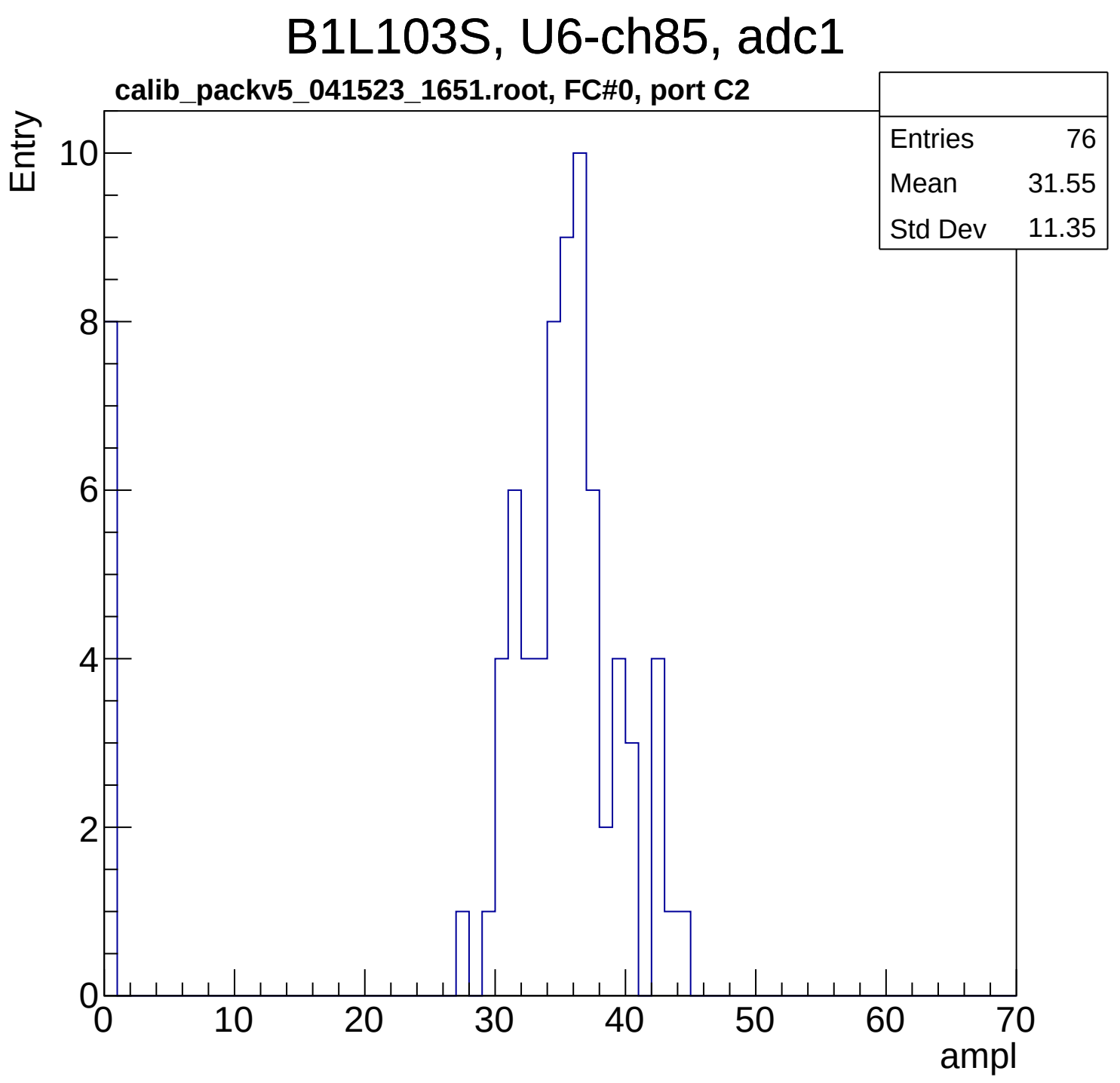
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch85, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 31.55
Std Dev 11.35
Entry
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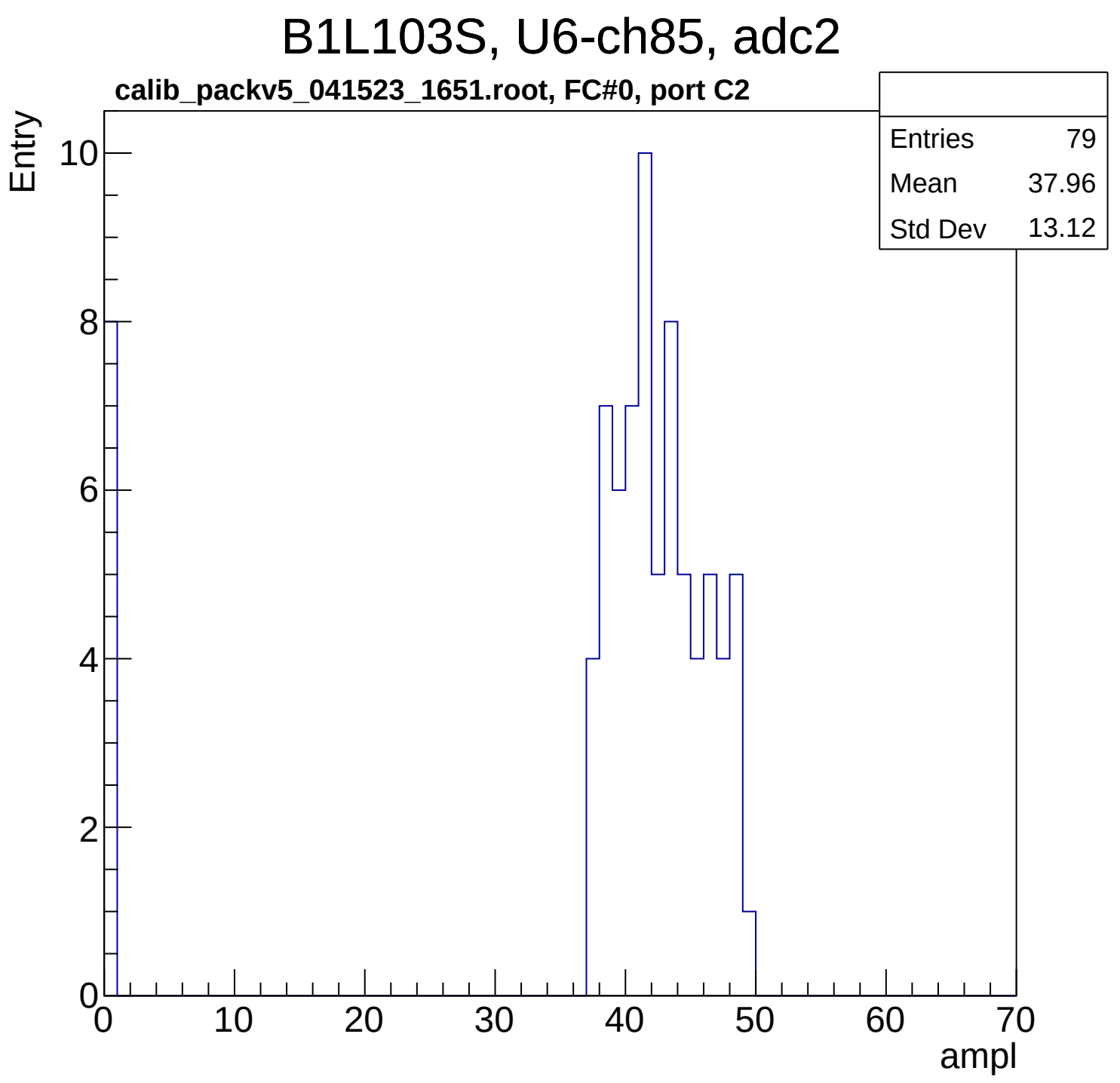
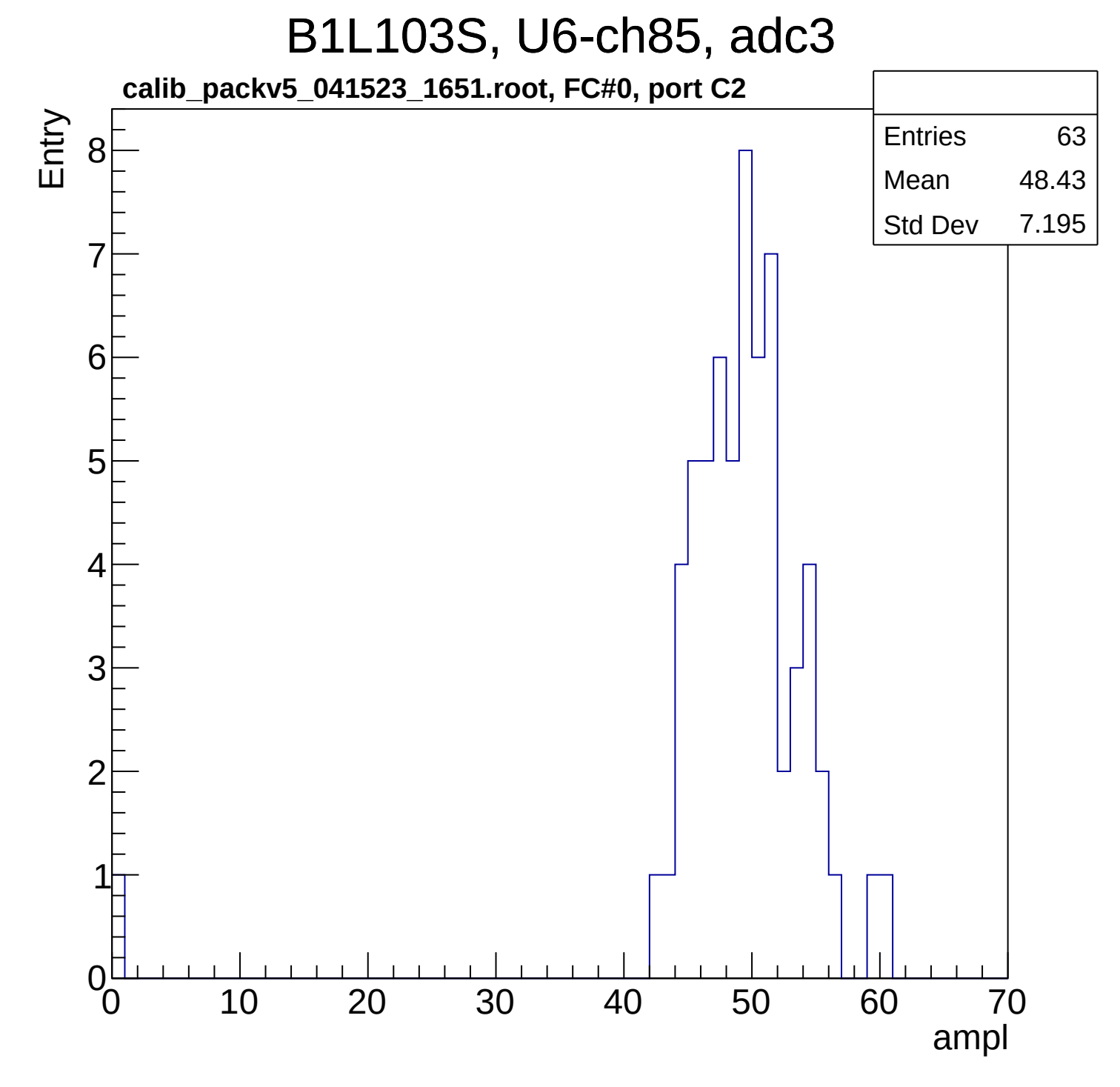
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch85, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 37.96
Std Dev 13.12
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch85, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 48.43
Std Dev 7.195
Entry
ampl
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1
2
3
4
5
6
7
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0
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40
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60
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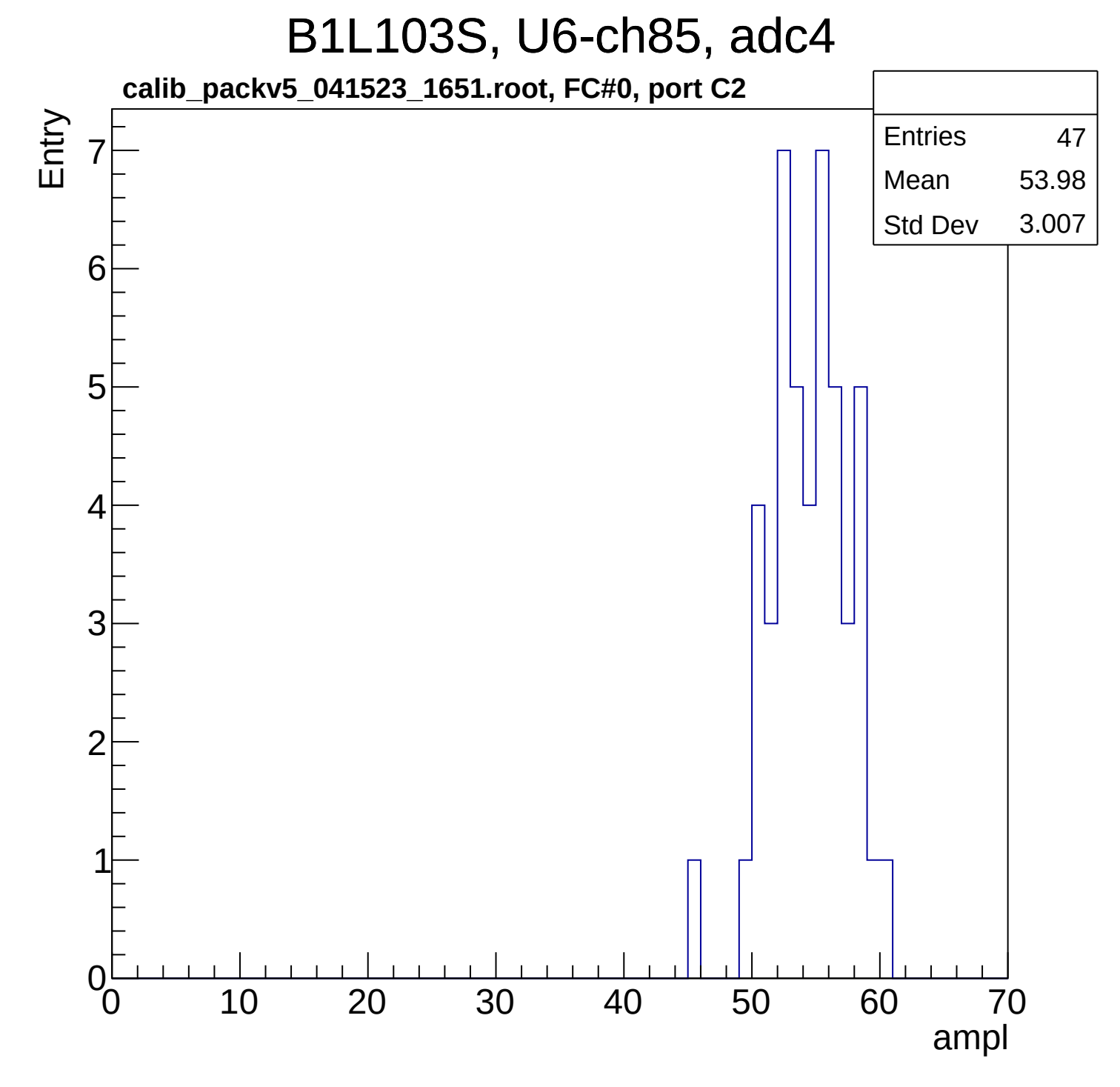
B1L103S, U6-ch85, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 53.98
Std Dev 3.007
Entry
ampl
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4
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6
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20
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40
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60
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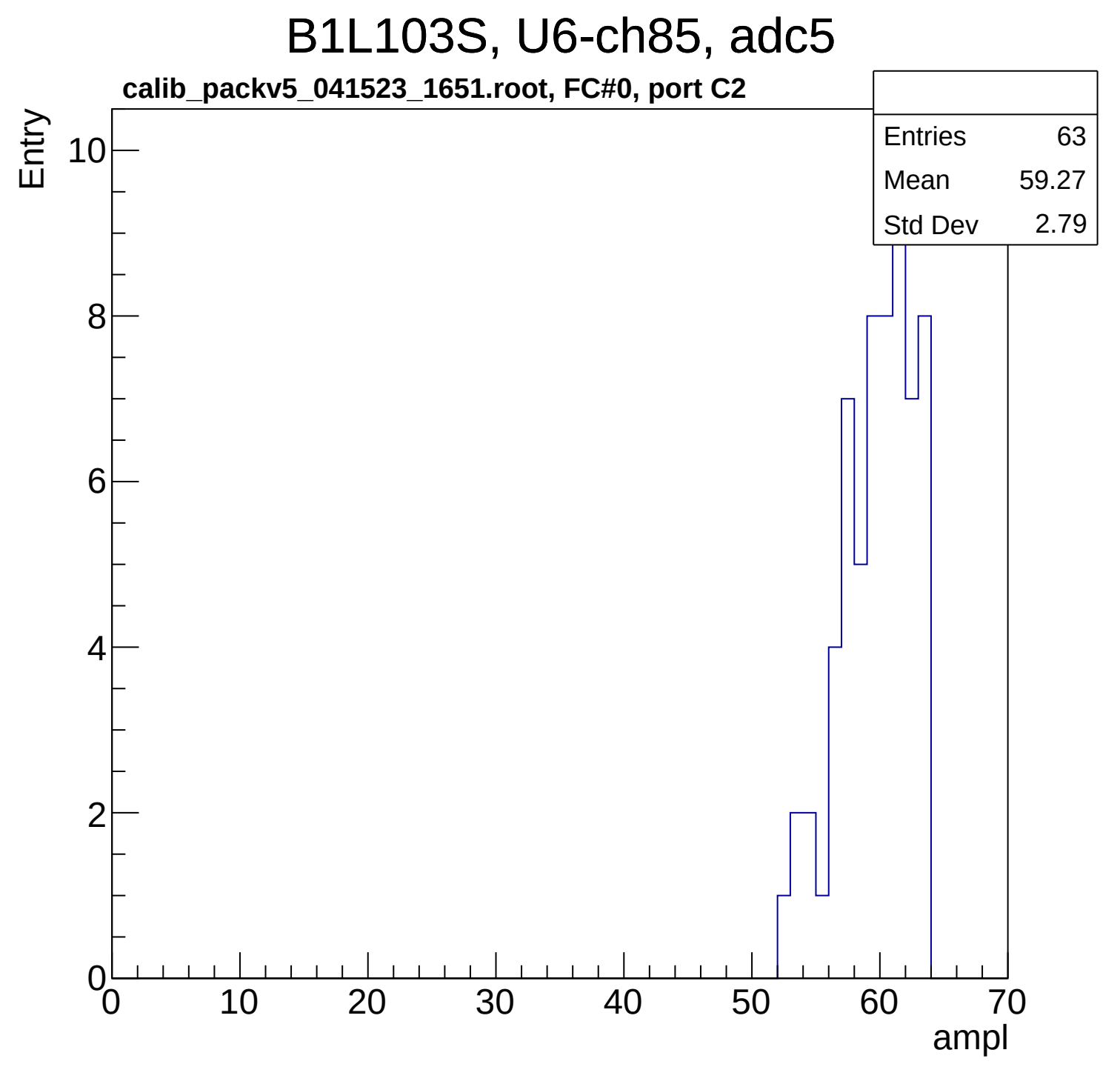
B1L103S, U6-ch85, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 59.27
Std Dev 2.79
Entry
ampl
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8
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0
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40
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60
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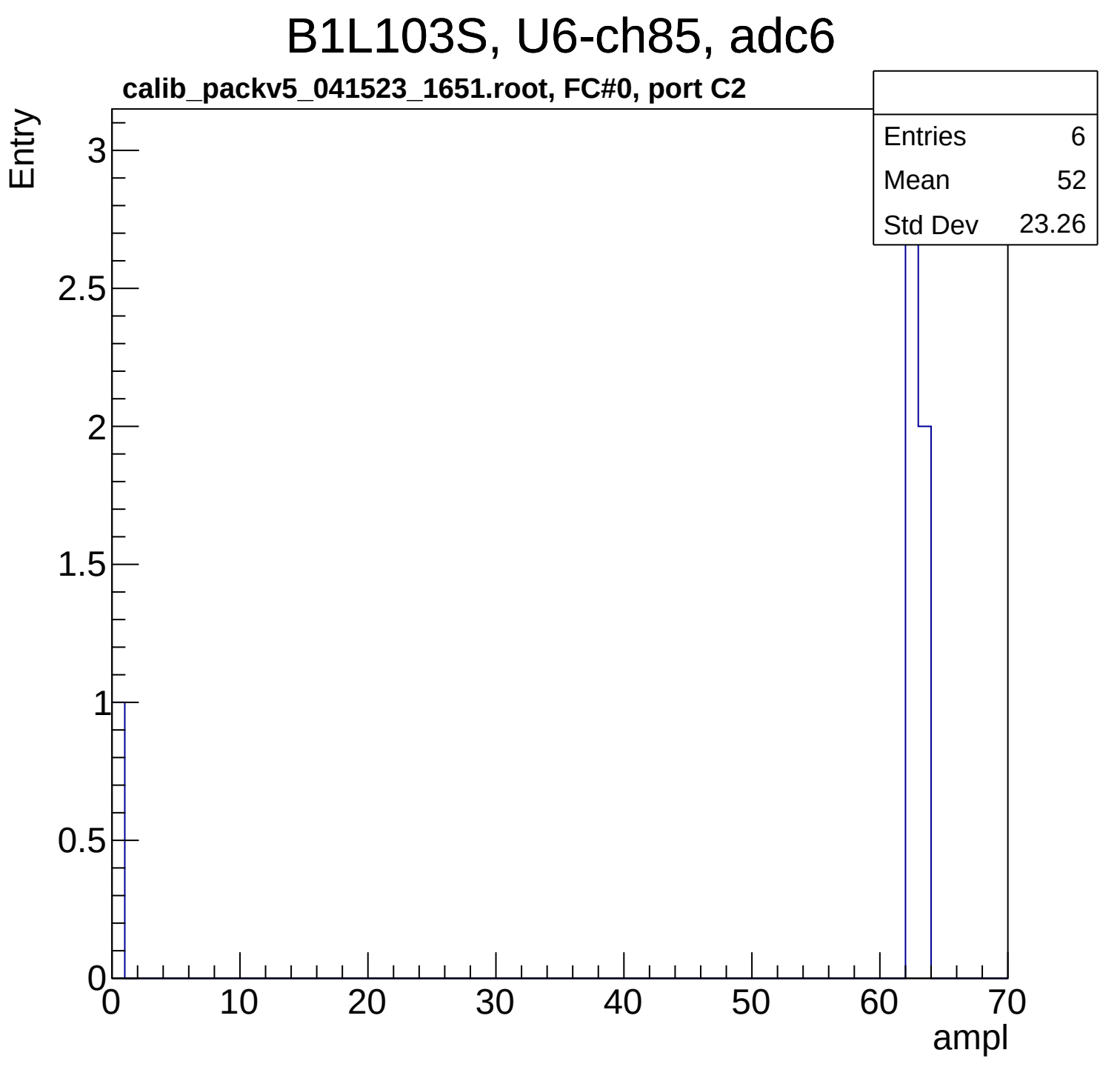
B1L103S, U6-ch85, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 52
Std Dev 23.26
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
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40
50
60
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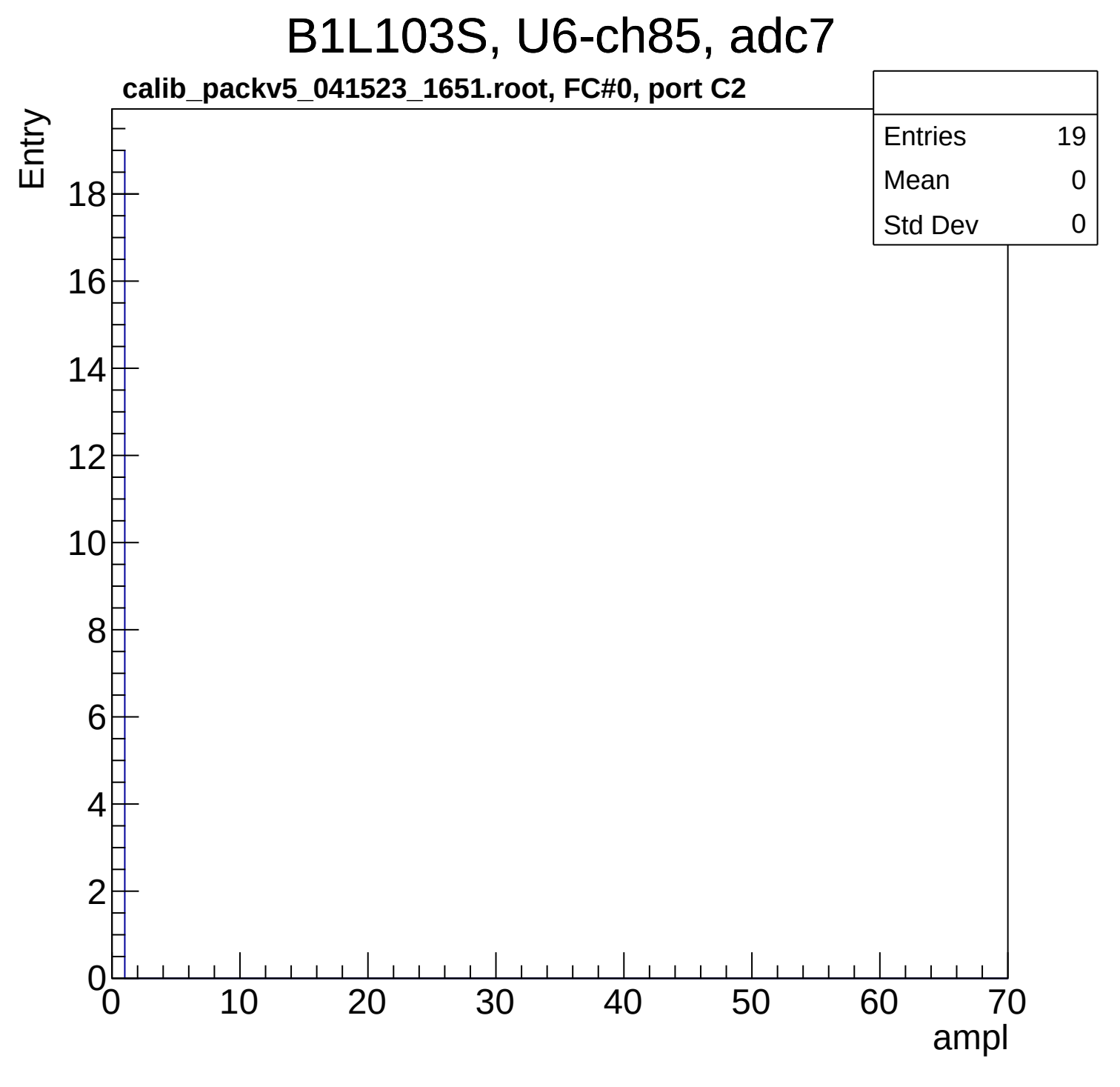
B1L103S, U6-ch85, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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6
8
10
12
14
16
18
0
10
20
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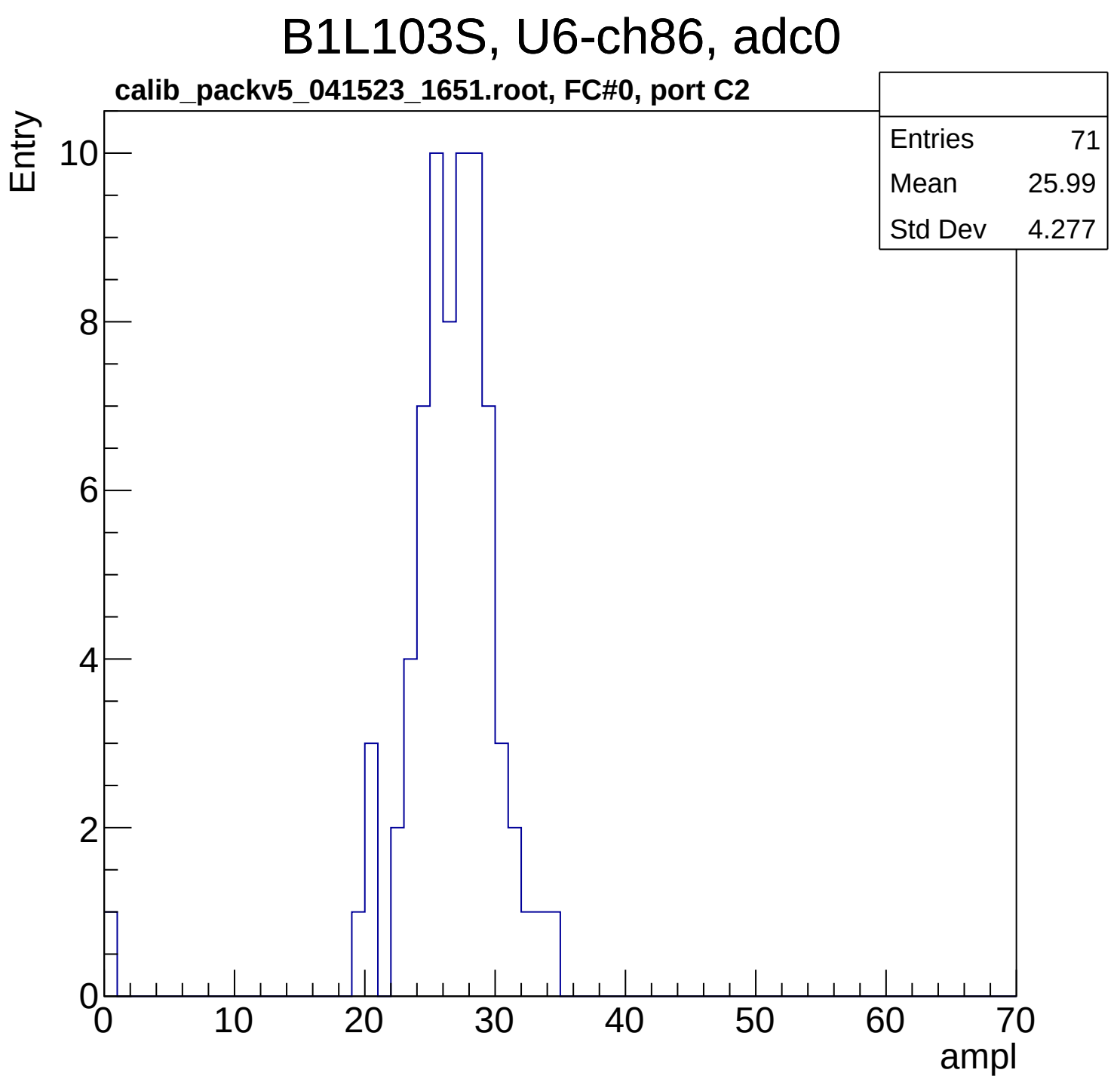
50
60
70
ampl


B1L103S, U6-ch86, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 25.99
Std Dev 4.277
Entry
ampl
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2
4
6
8
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0
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20
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40
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60
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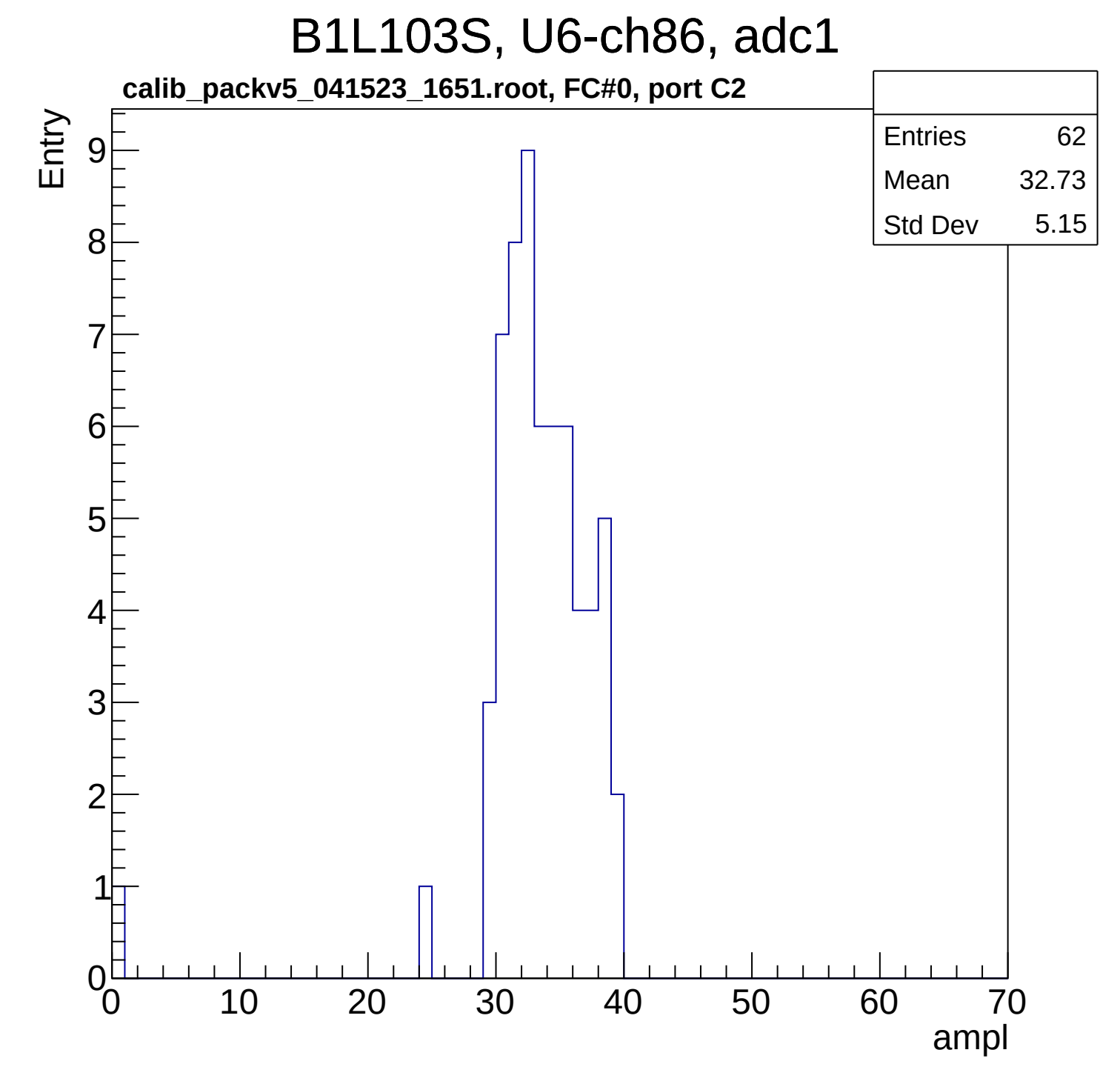
B1L103S, U6-ch86, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 32.73
Std Dev 5.15
Entry
ampl
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3
4
5
6
7
8
9
0
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40
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60
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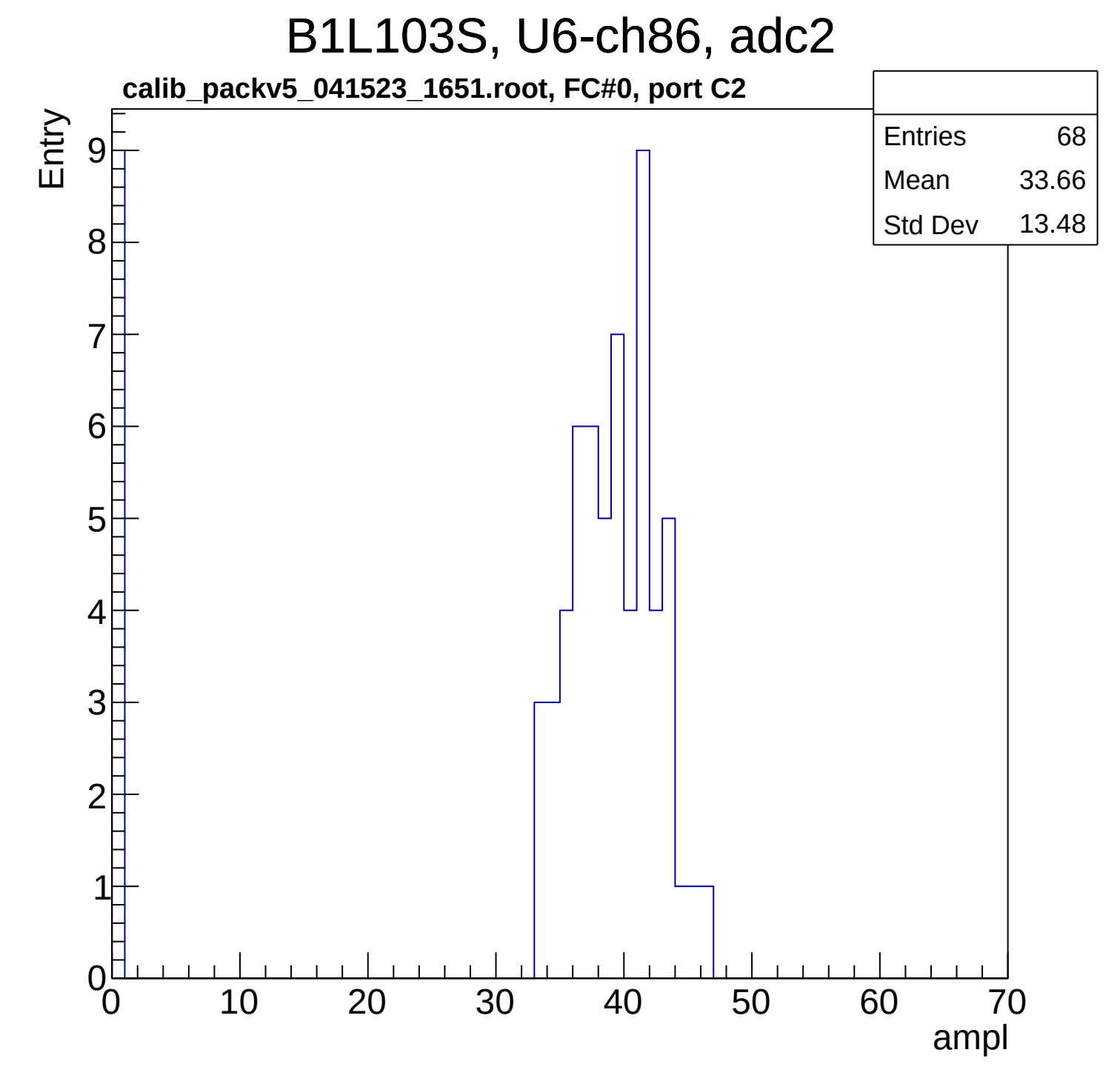
B1L103S, U6-ch86, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 33.66
Std Dev 13.48
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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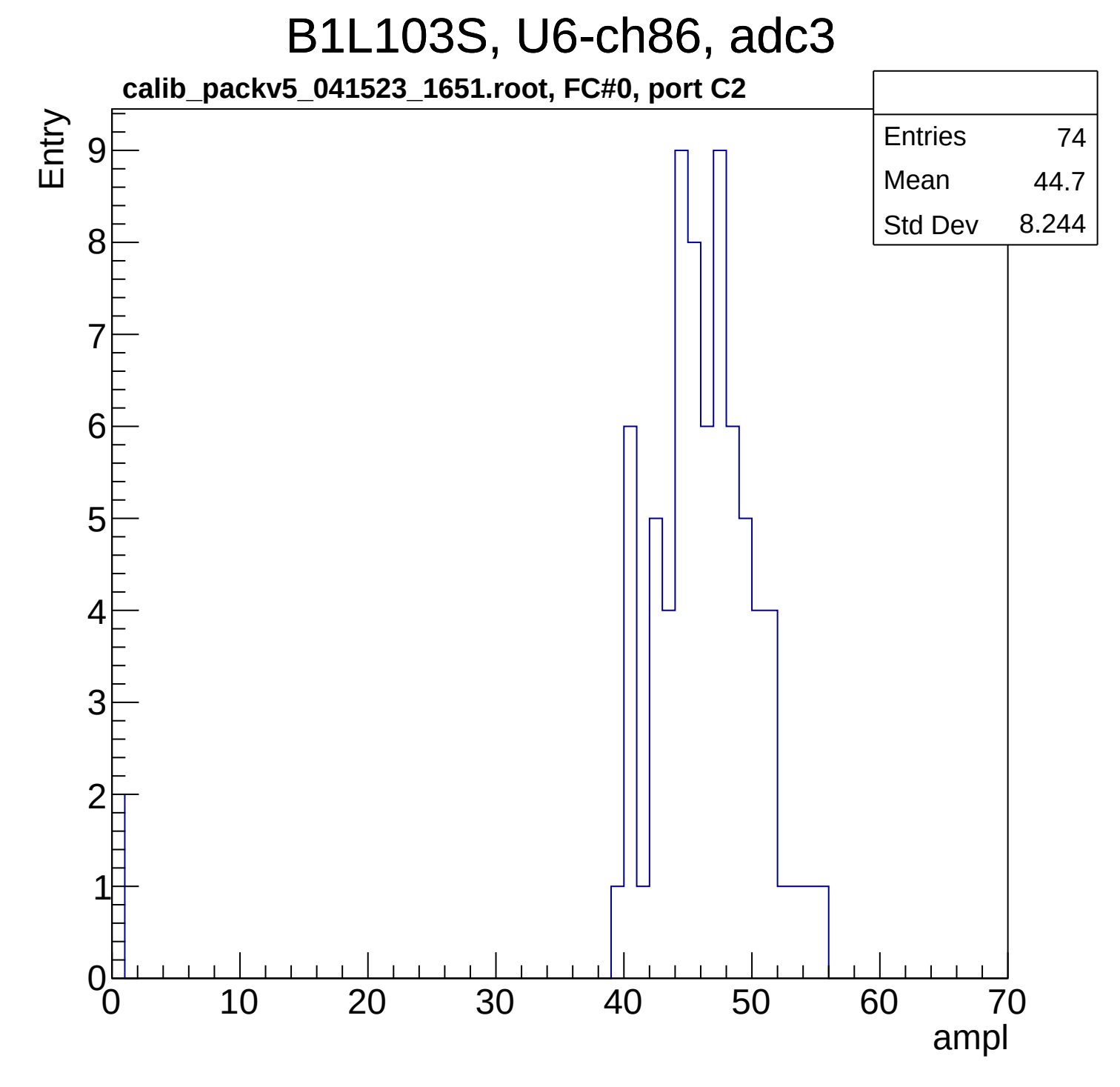
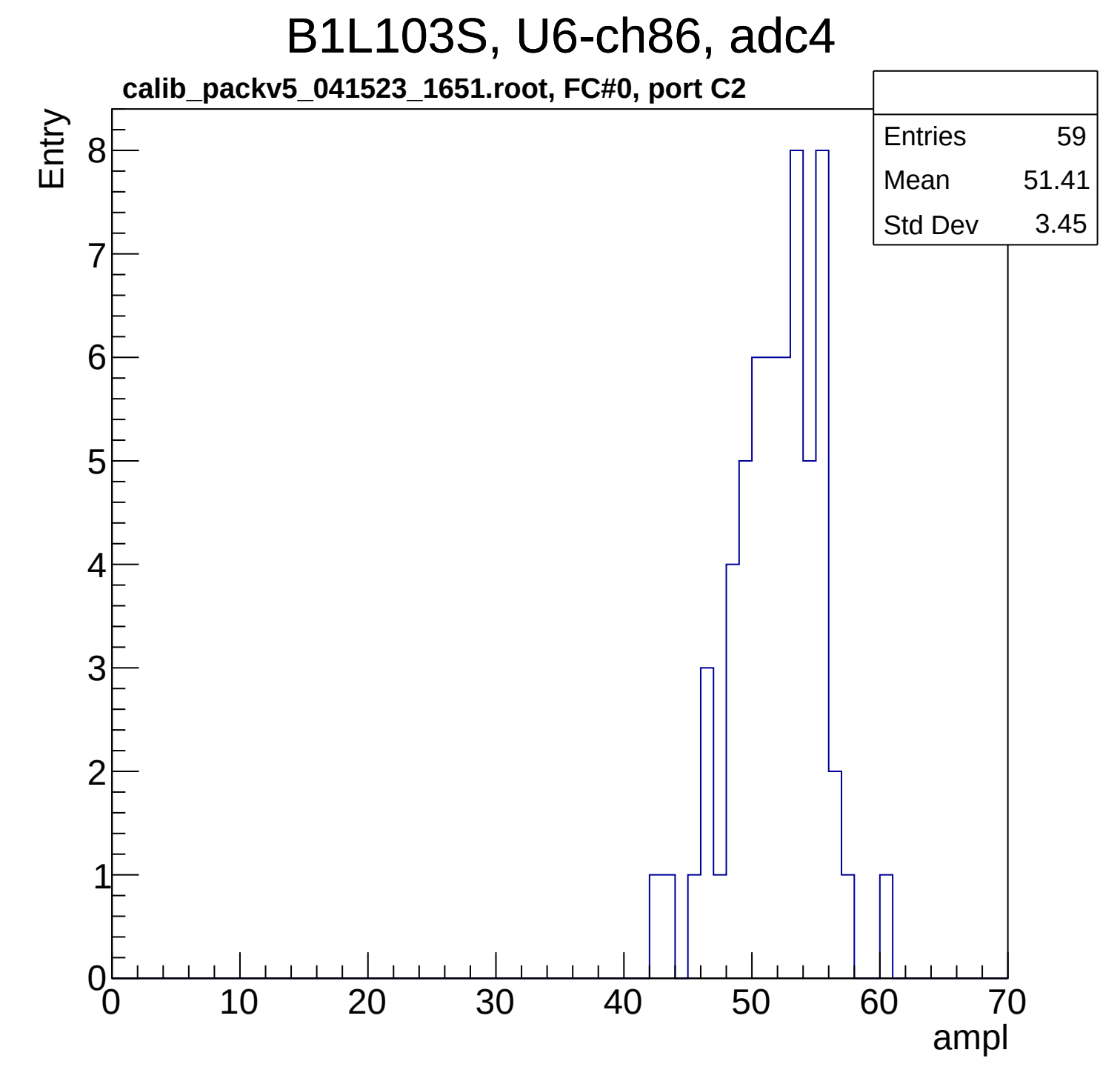
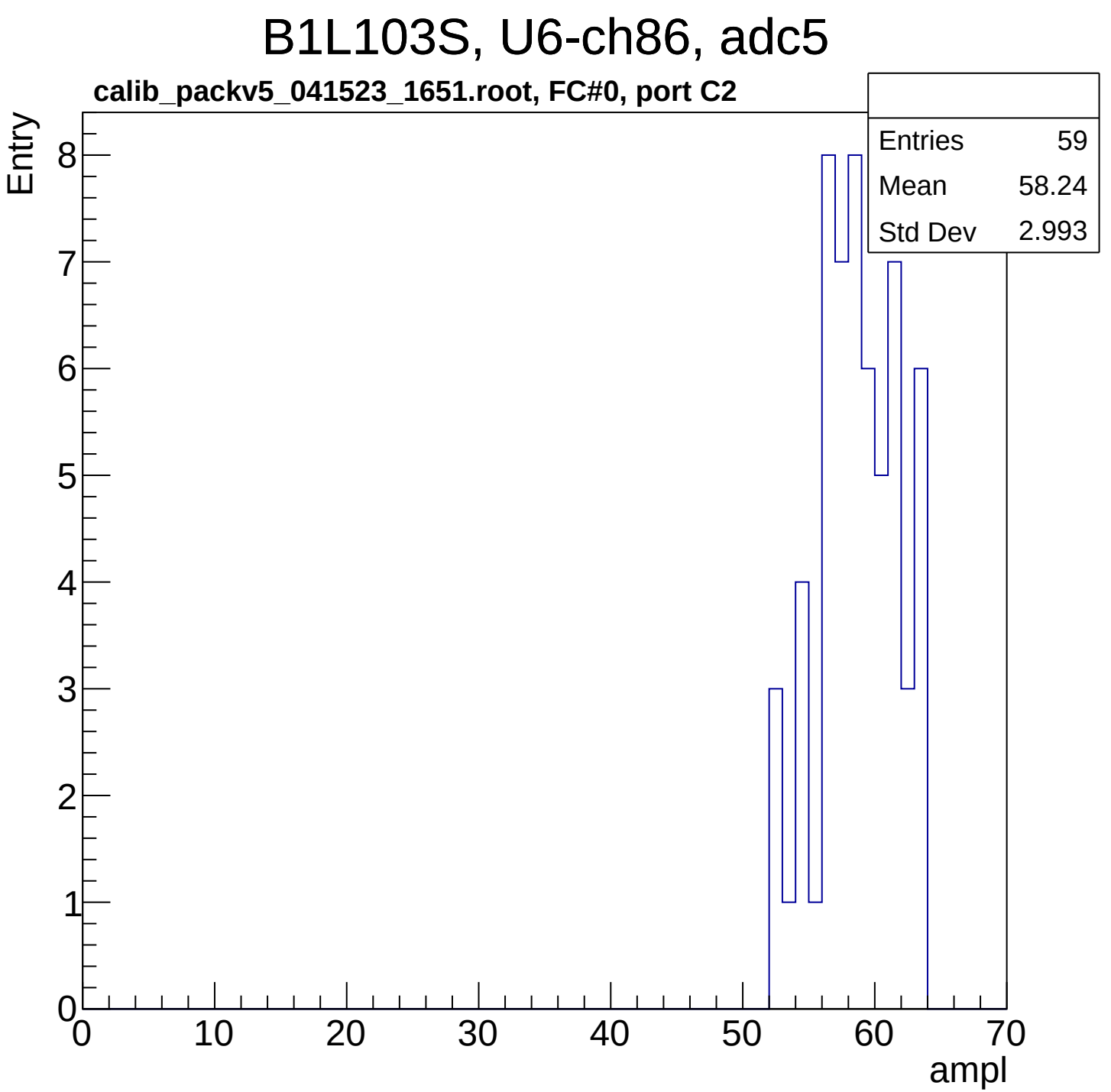

B1L103S, U6-ch86, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 44.7
Std Dev 8.244
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch86, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 51.41
Std Dev 3.45
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch86, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 58.24
Std Dev 2.993
Entry
ampl
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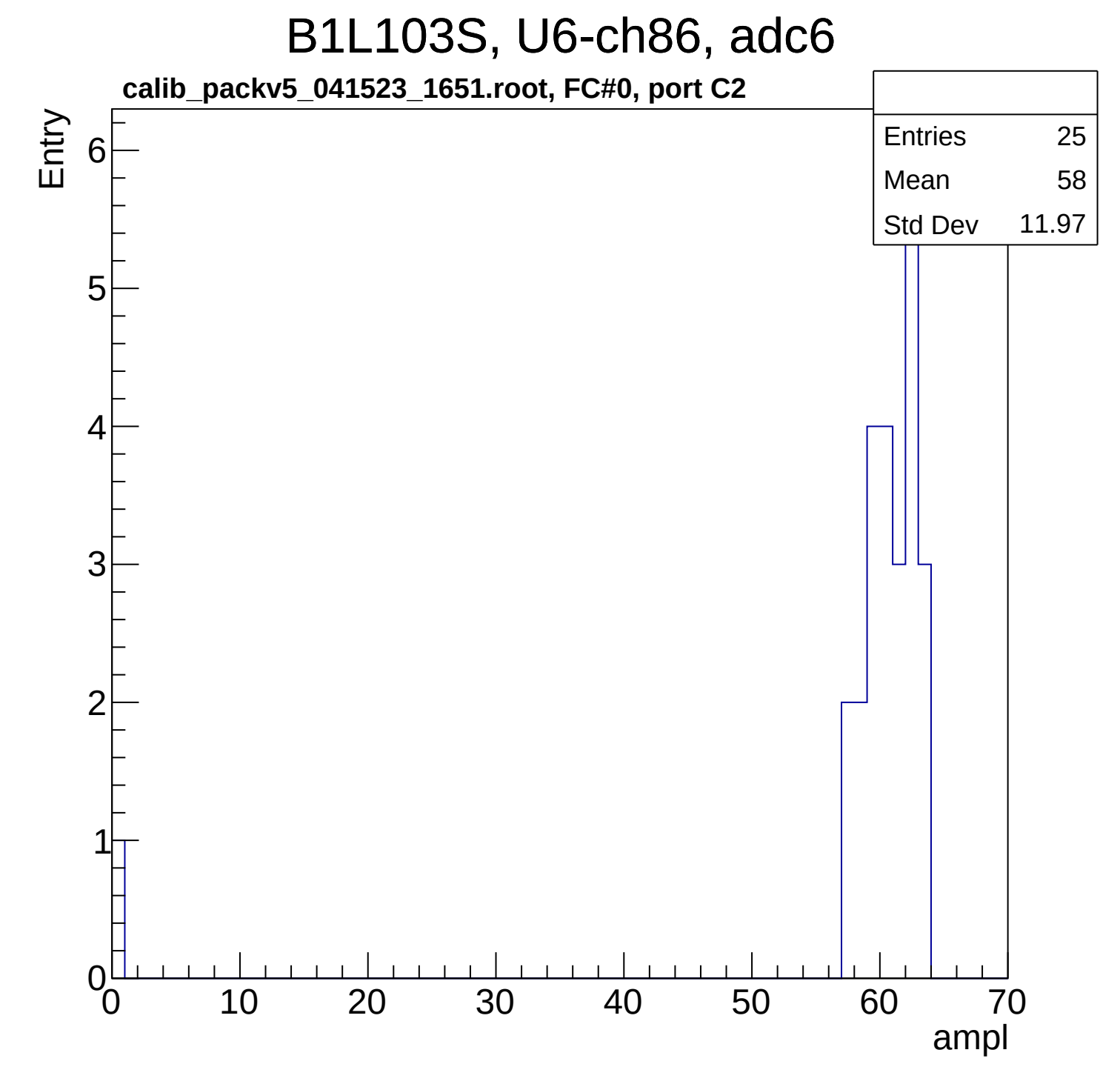
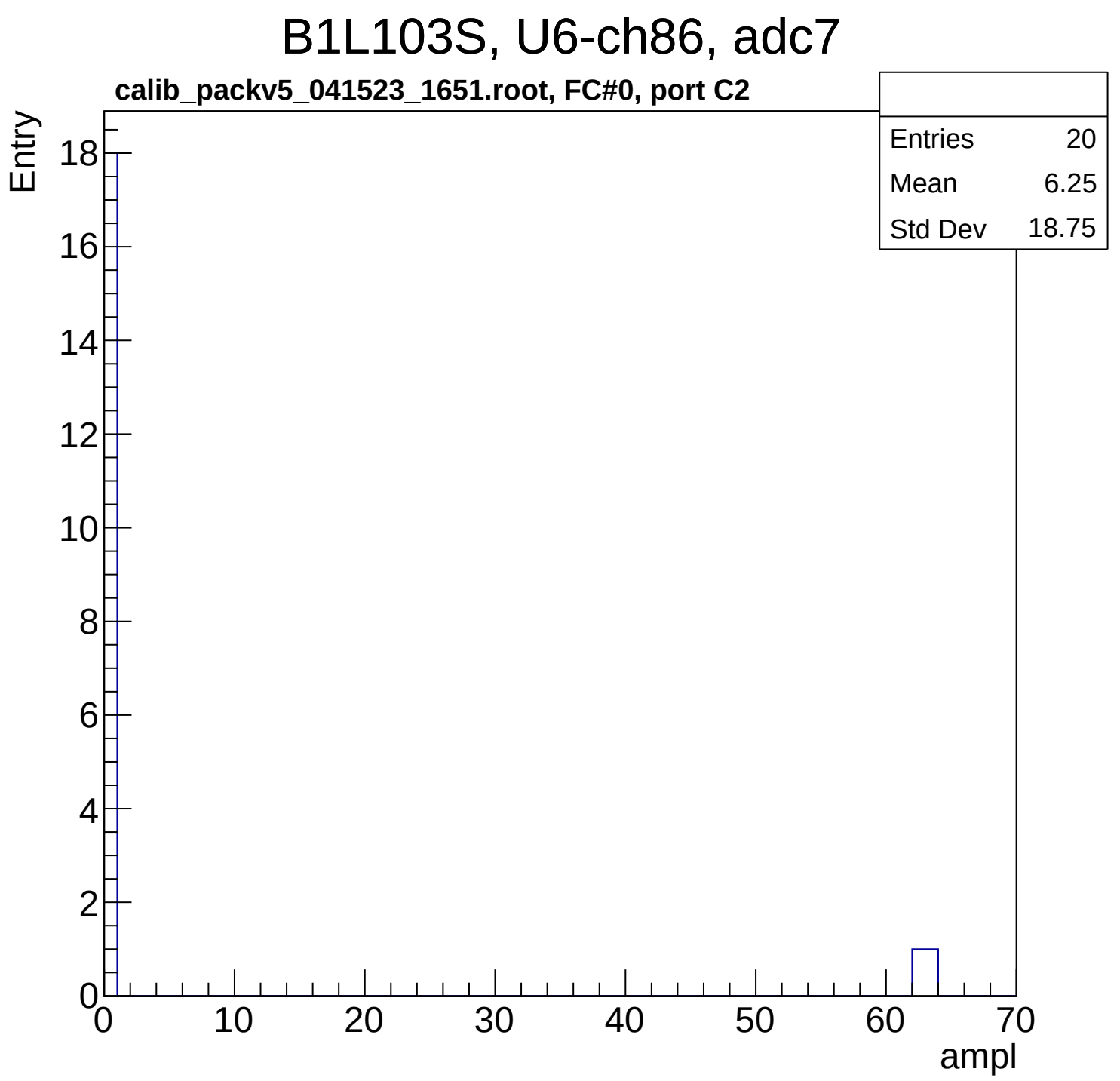
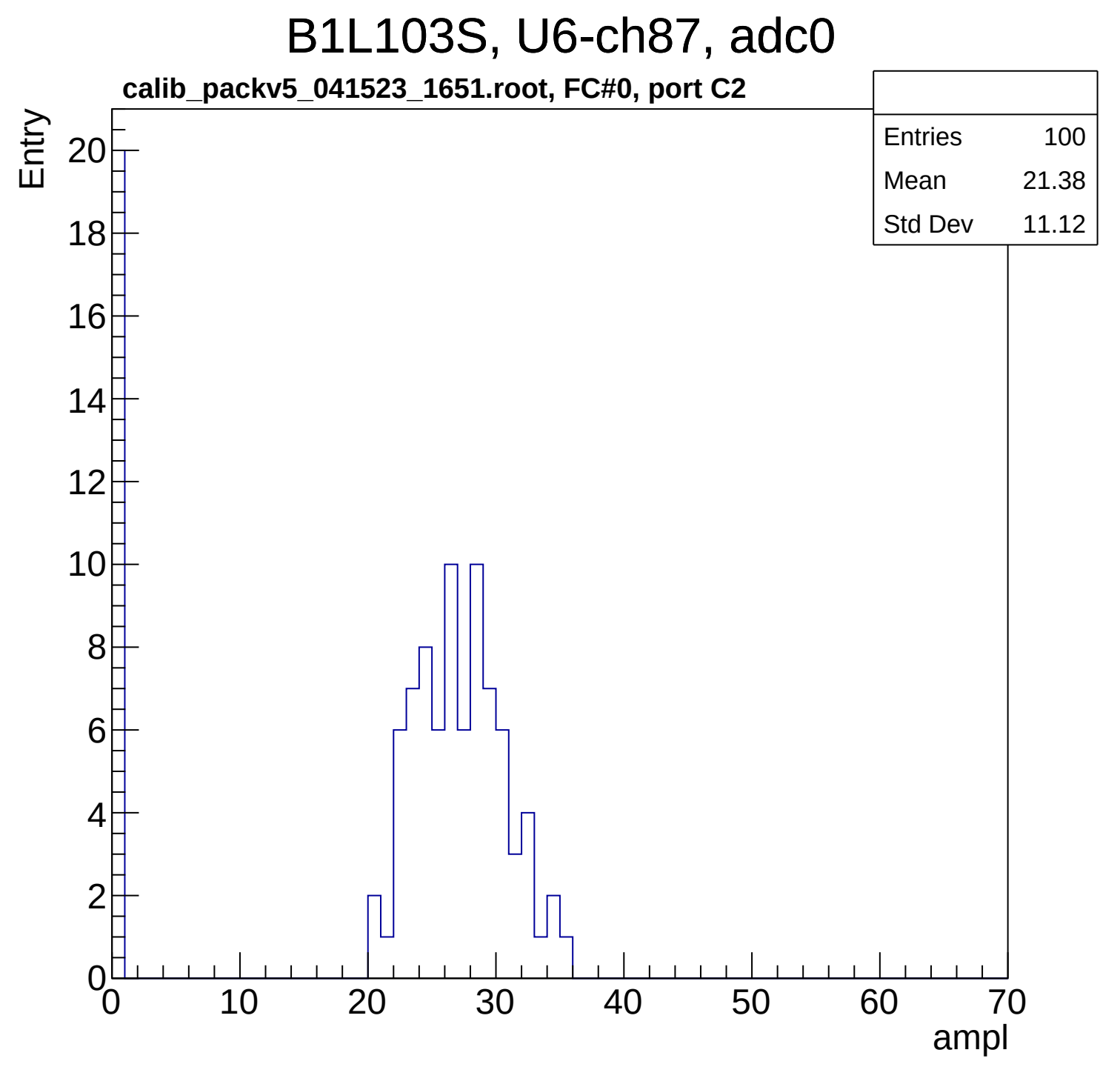
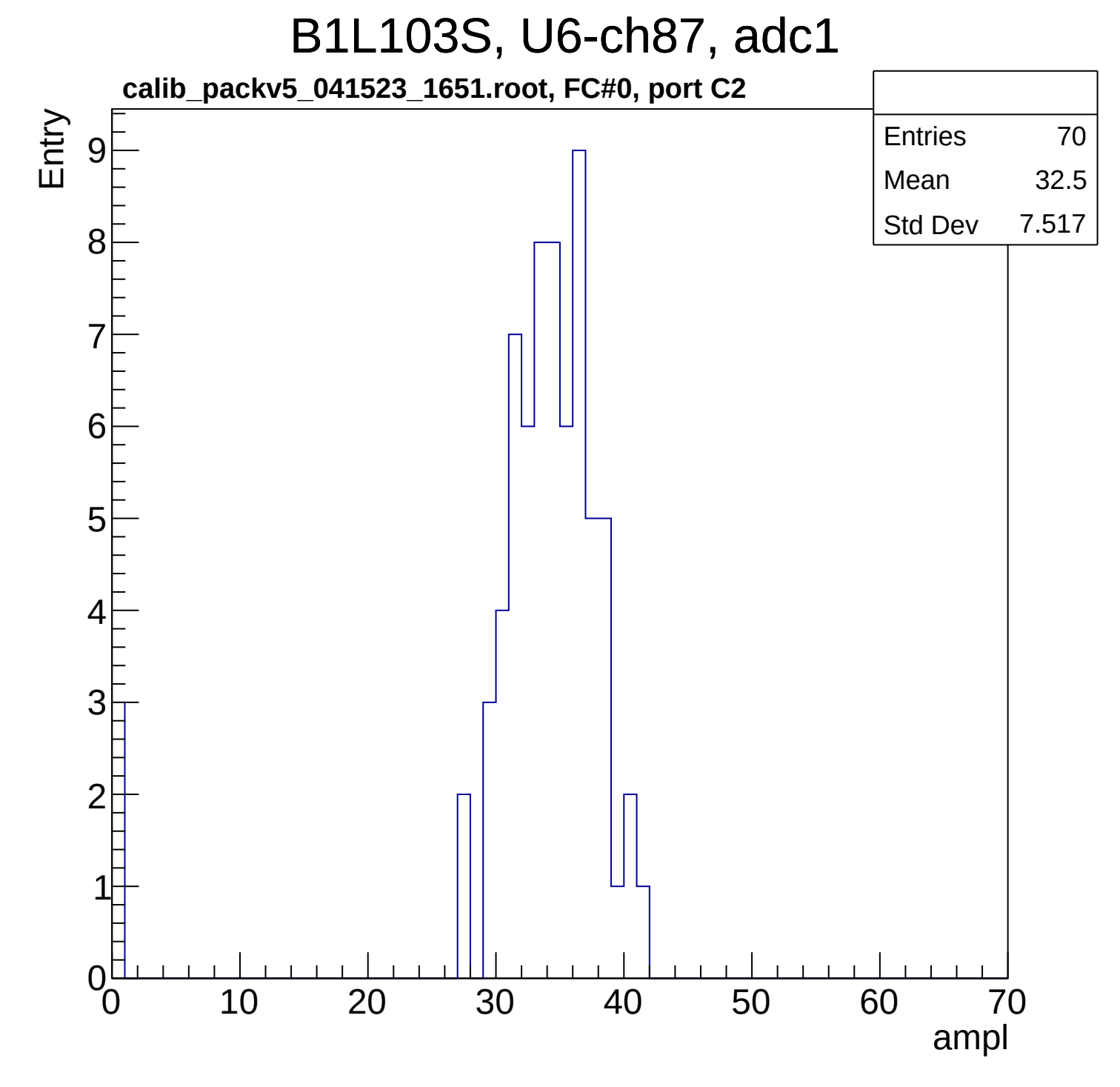
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch86, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 58
Std Dev 11.97
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch86, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 6.25
Std Dev 18.75
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch87, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 100
Mean 21.38
Std Dev 11.12
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70


B1L103S, U6-ch87, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 32.5
Std Dev 7.517
Entry
ampl
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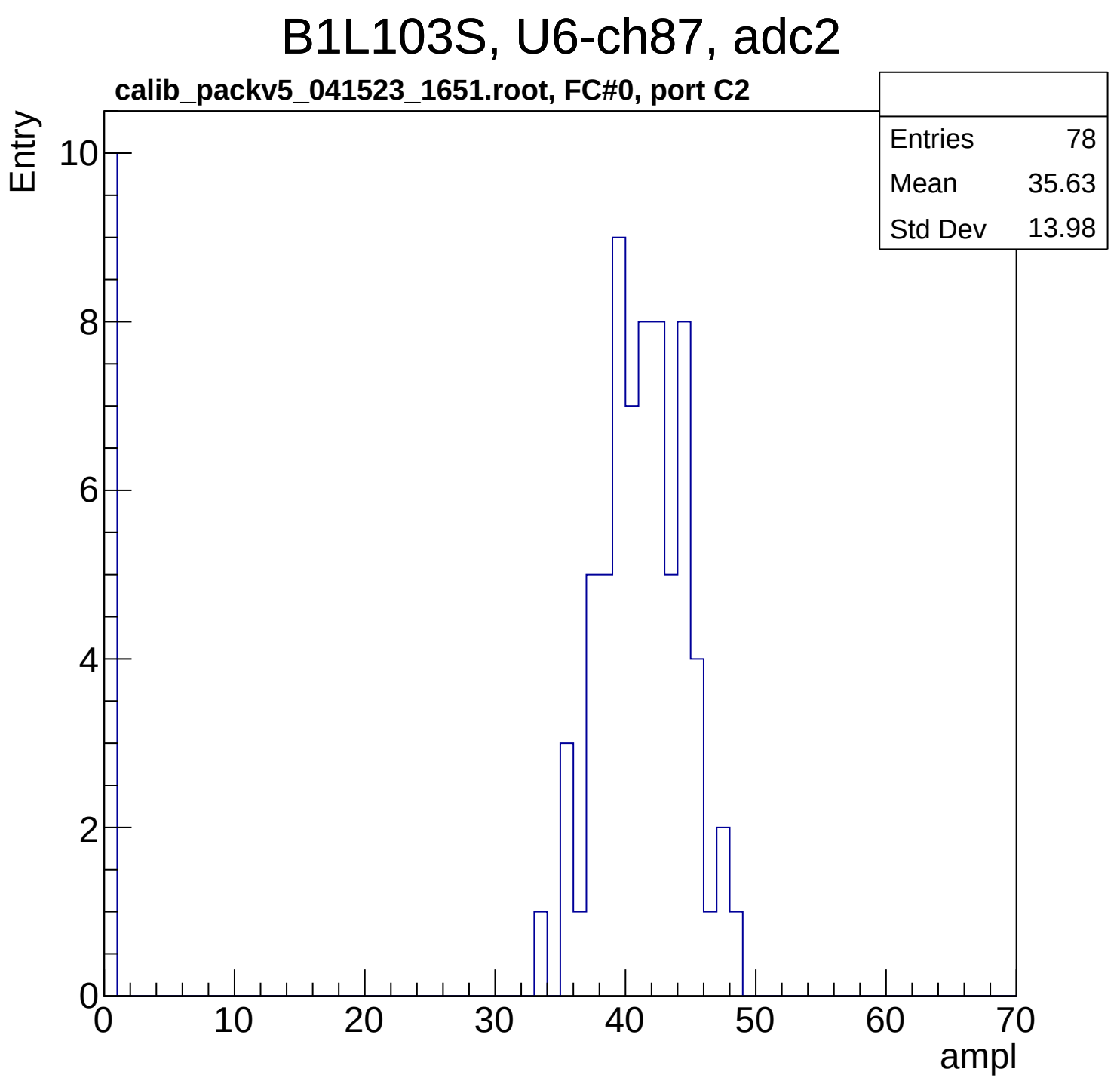
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch87, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 35.63
Std Dev 13.98
Entry
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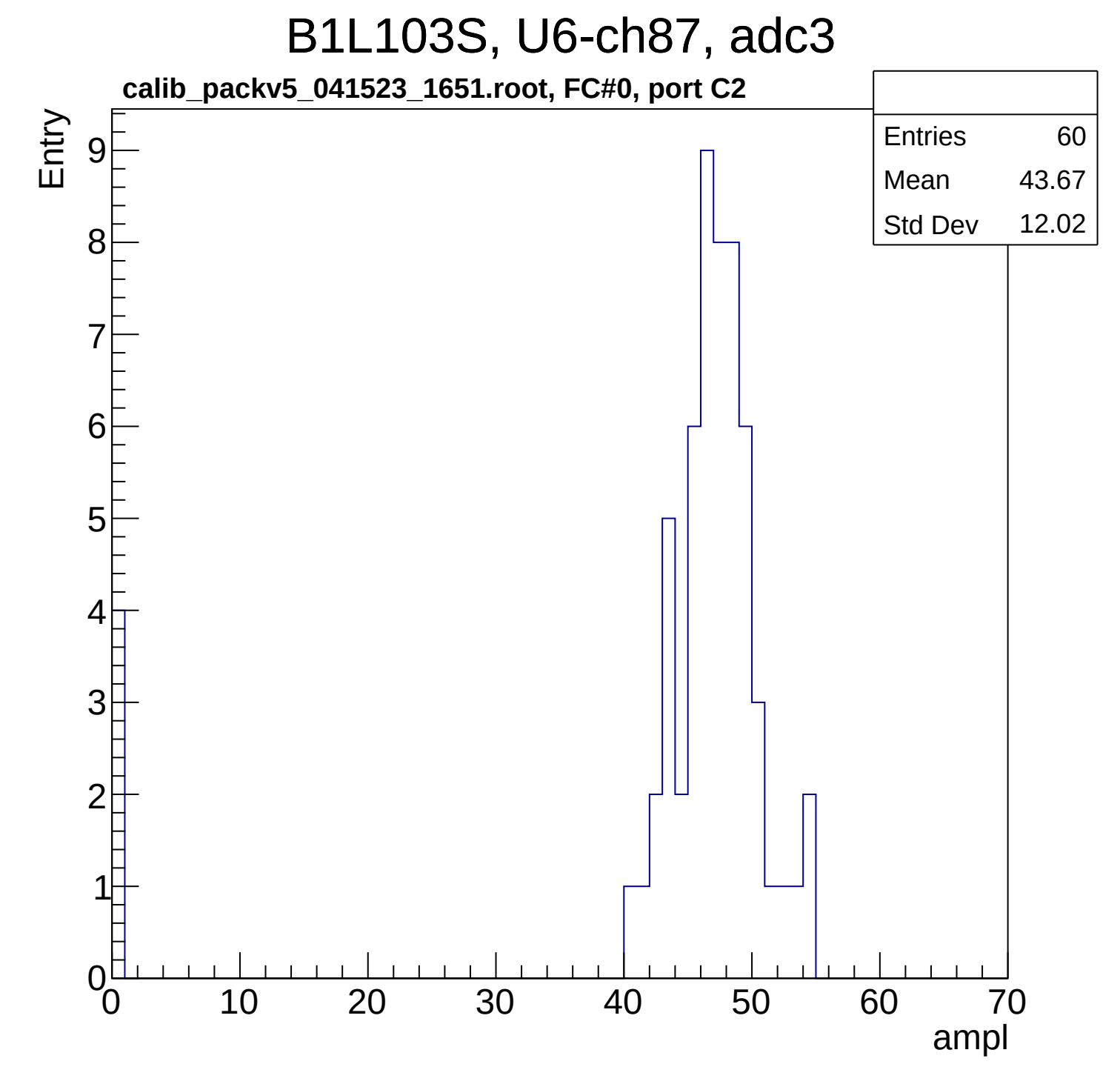
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch87, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 43.67
Std Dev 12.02
Entry
ampl
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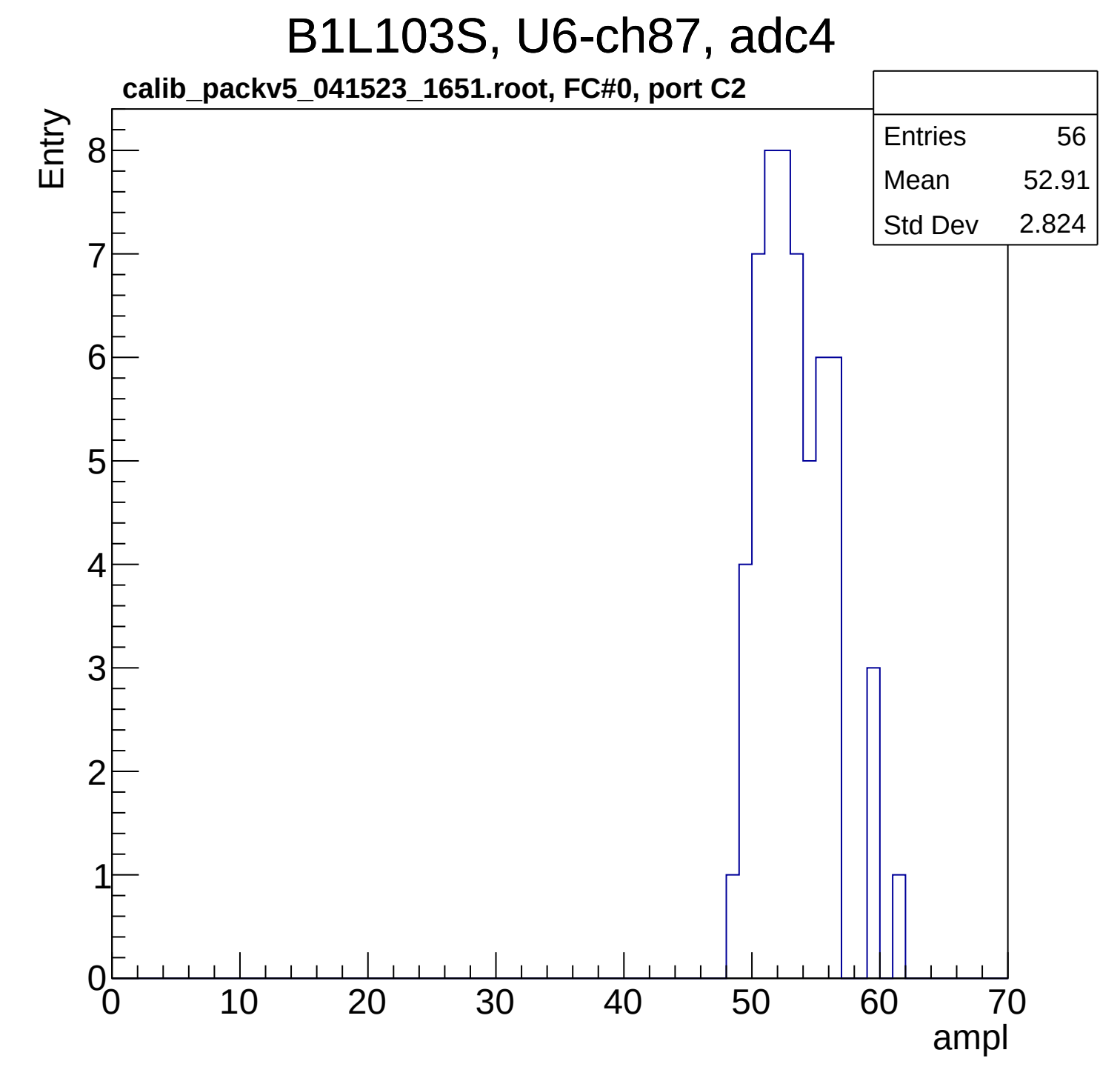
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch87, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 52.91
Std Dev 2.824
Entry
ampl
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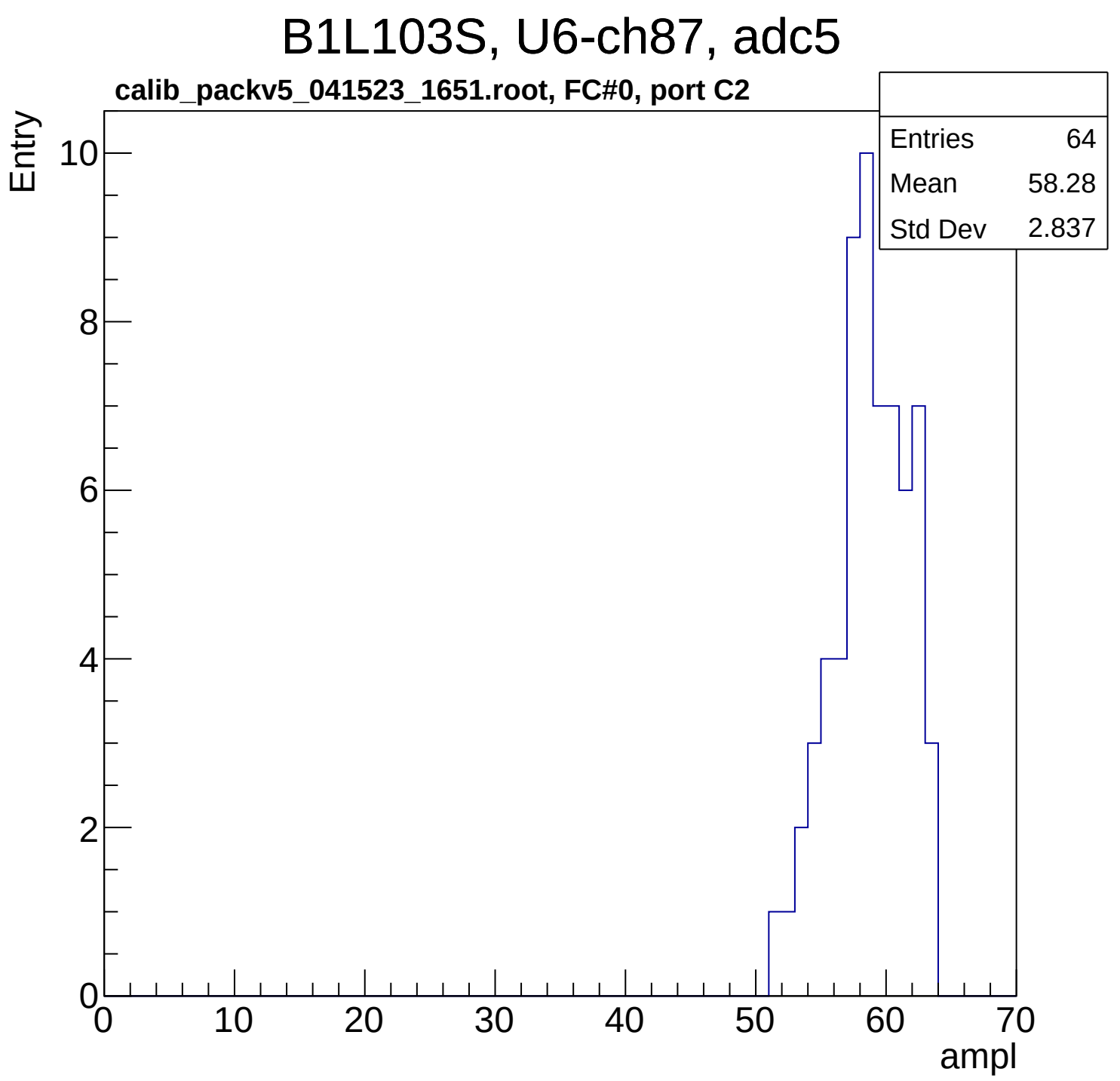
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch87, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 58.28
Std Dev 2.837
Entry
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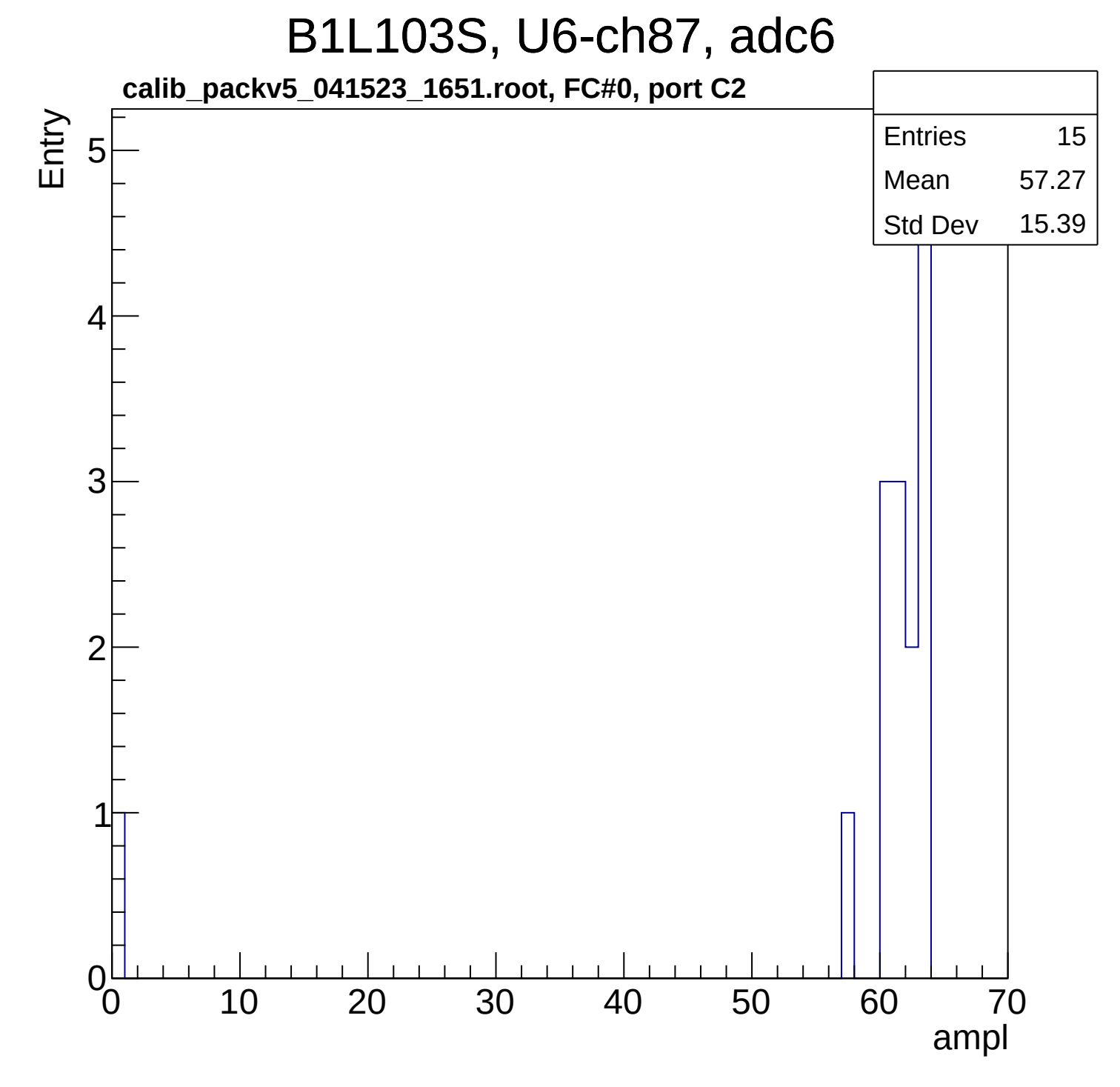
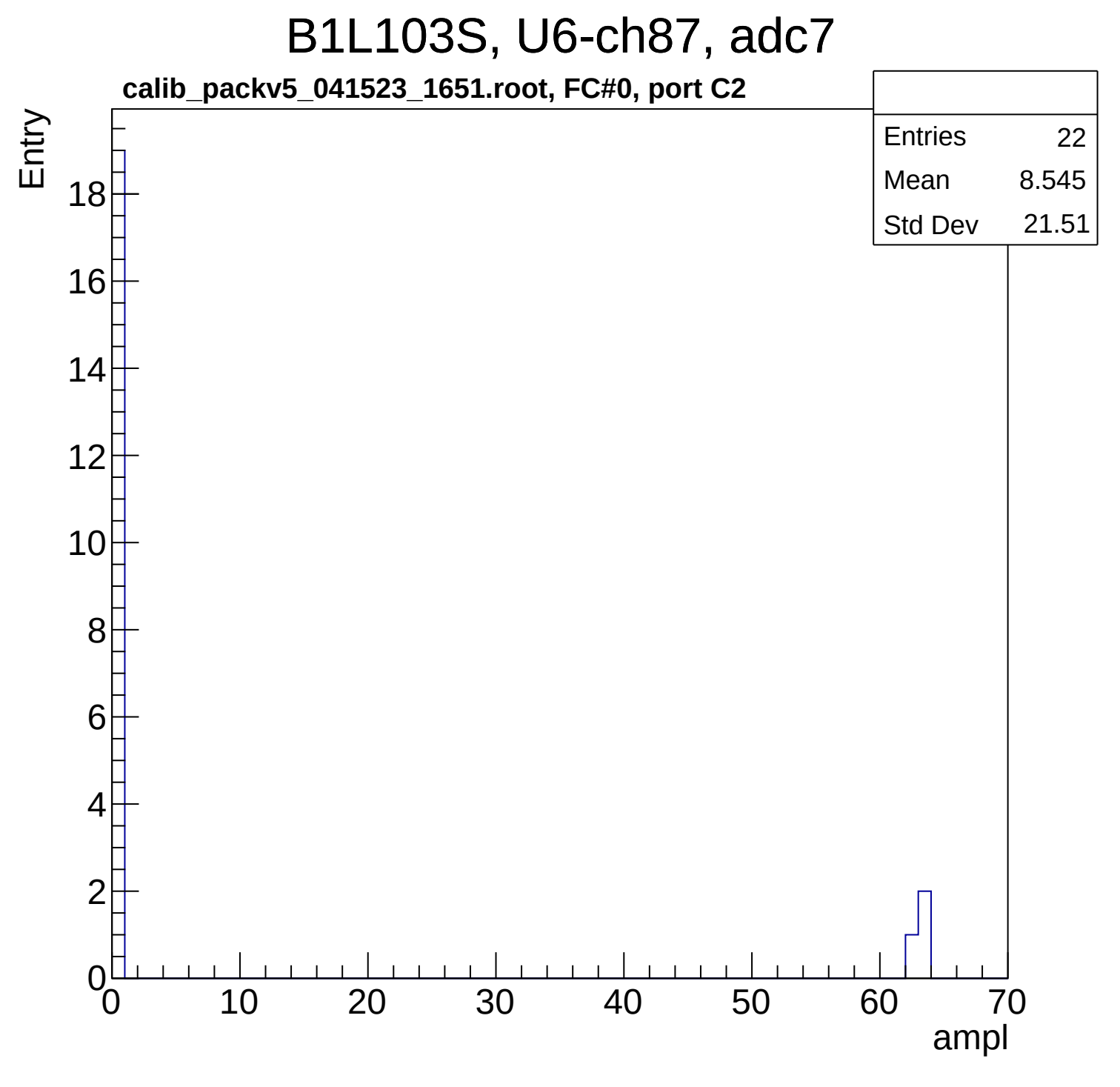
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch87, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 57.27
Std Dev 15.39
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch87, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.545
Std Dev 21.51
Entry
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6
8
10
12
14
16
18
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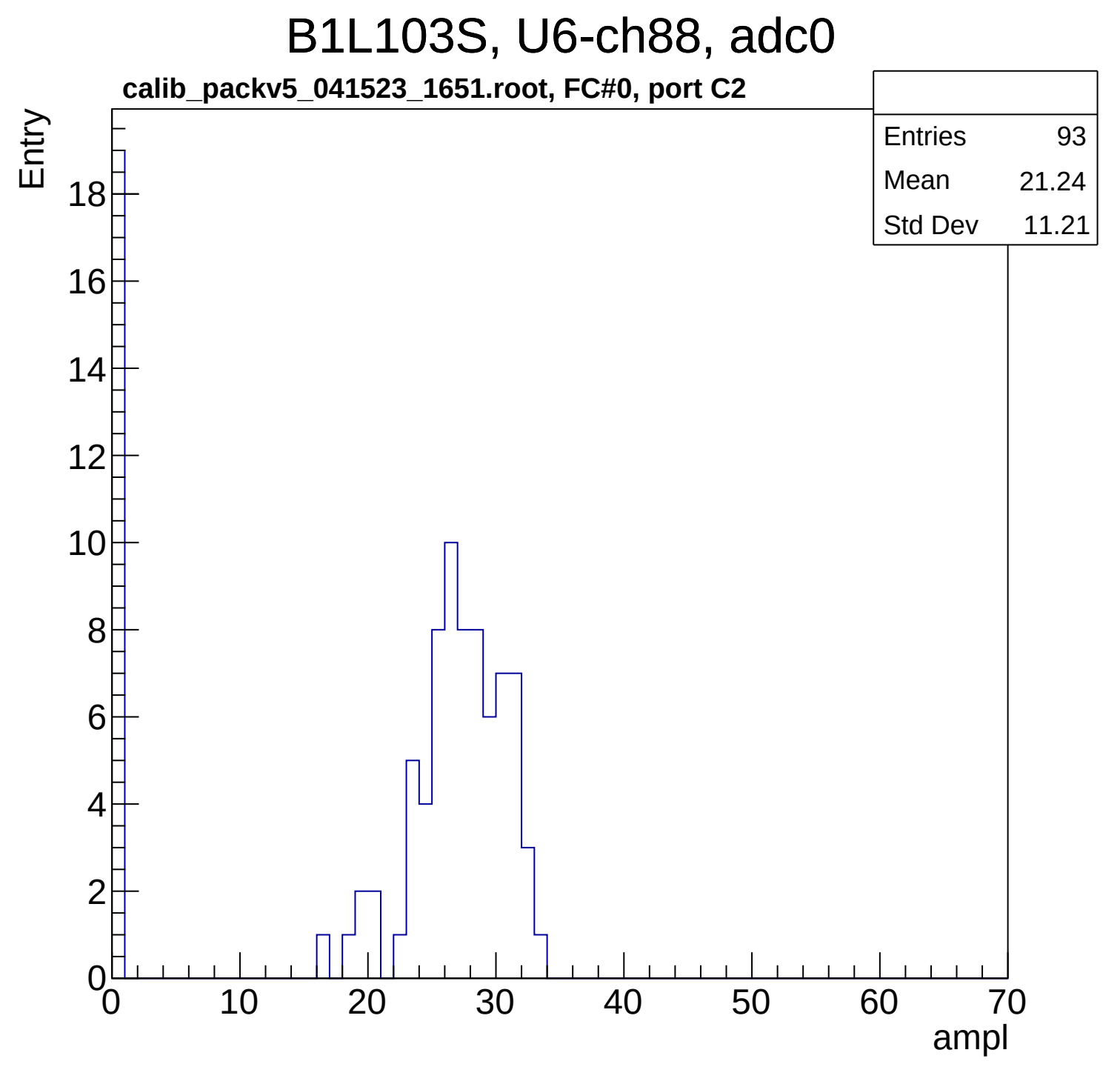
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch88, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 21.24
Std Dev 11.21
Entry
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6
8
10
12
14
16
18
0
10
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30
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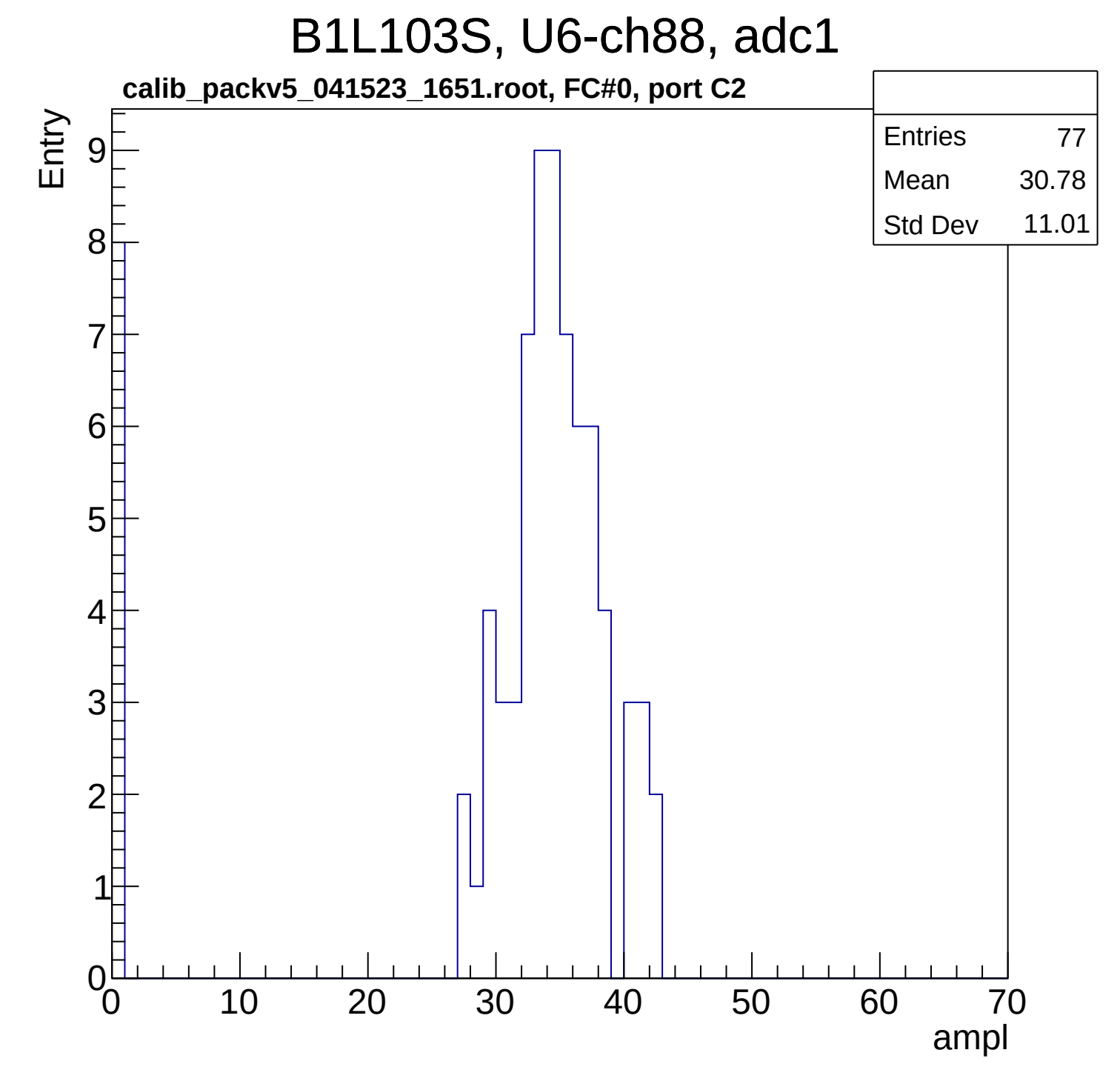
50
60
70
ampl


B1L103S, U6-ch88, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 30.78
Std Dev 11.01
Entry
ampl
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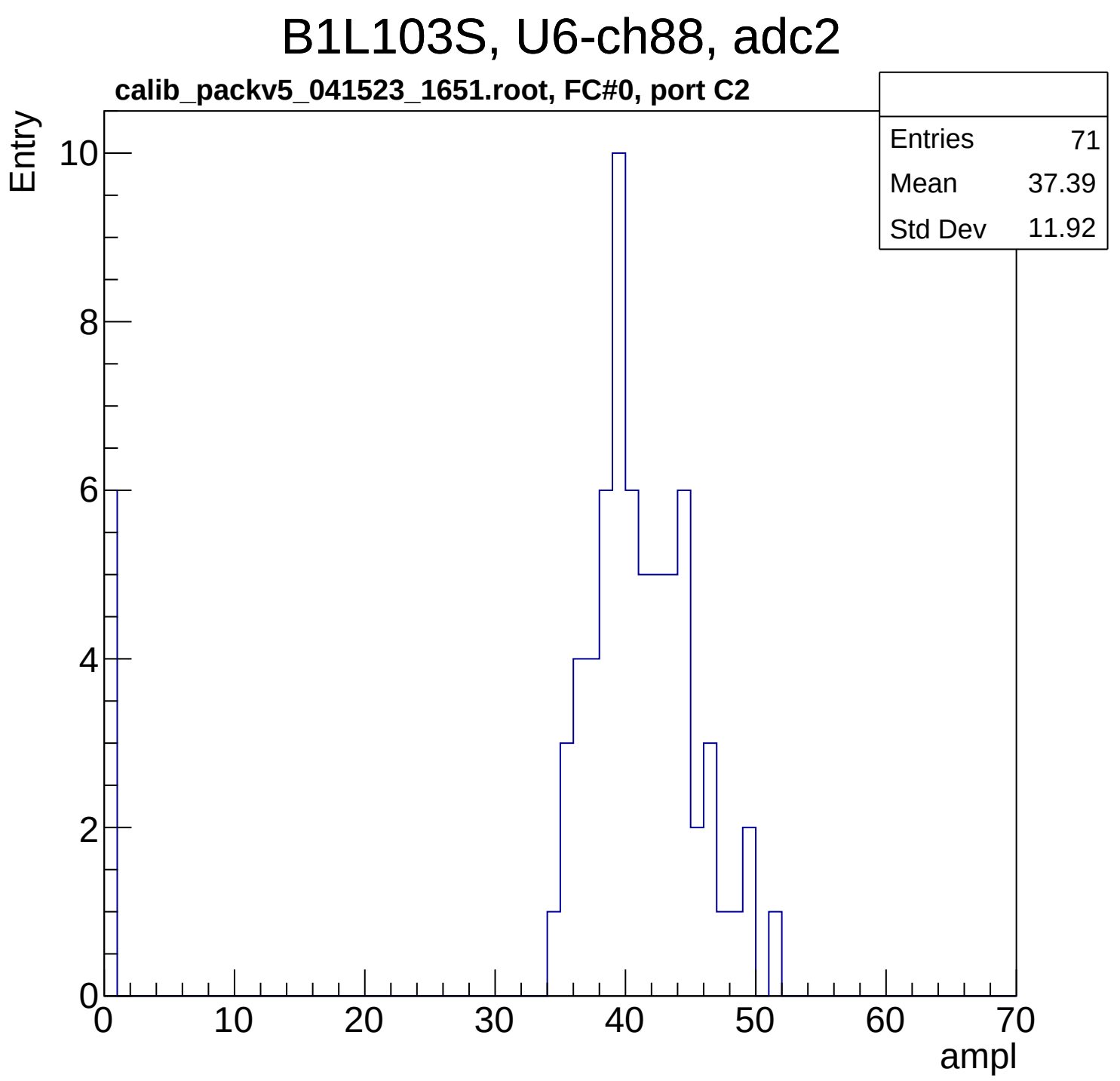
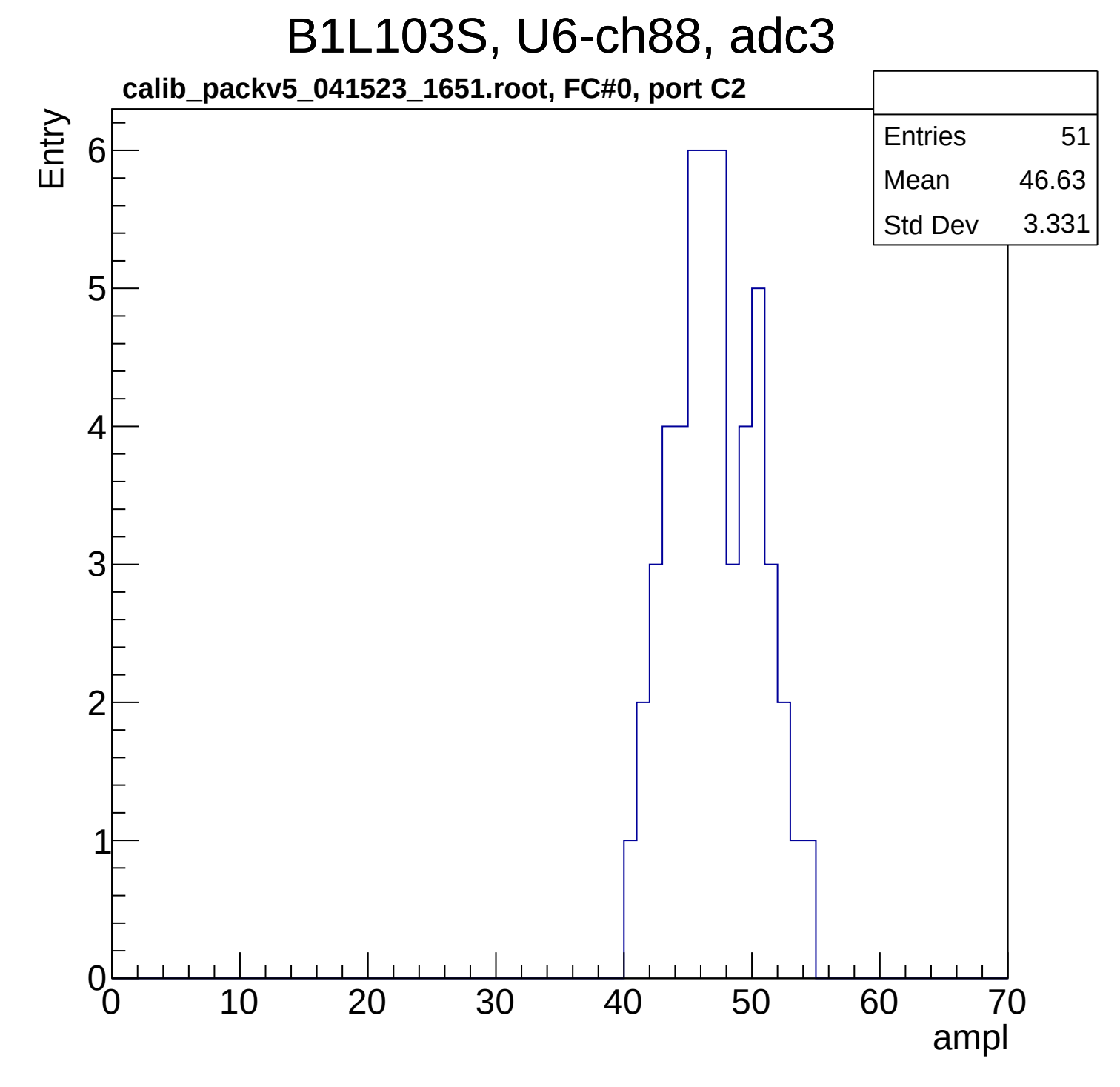
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch88, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 37.39
Std Dev 11.92
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch88, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 46.63
Std Dev 3.331
Entry
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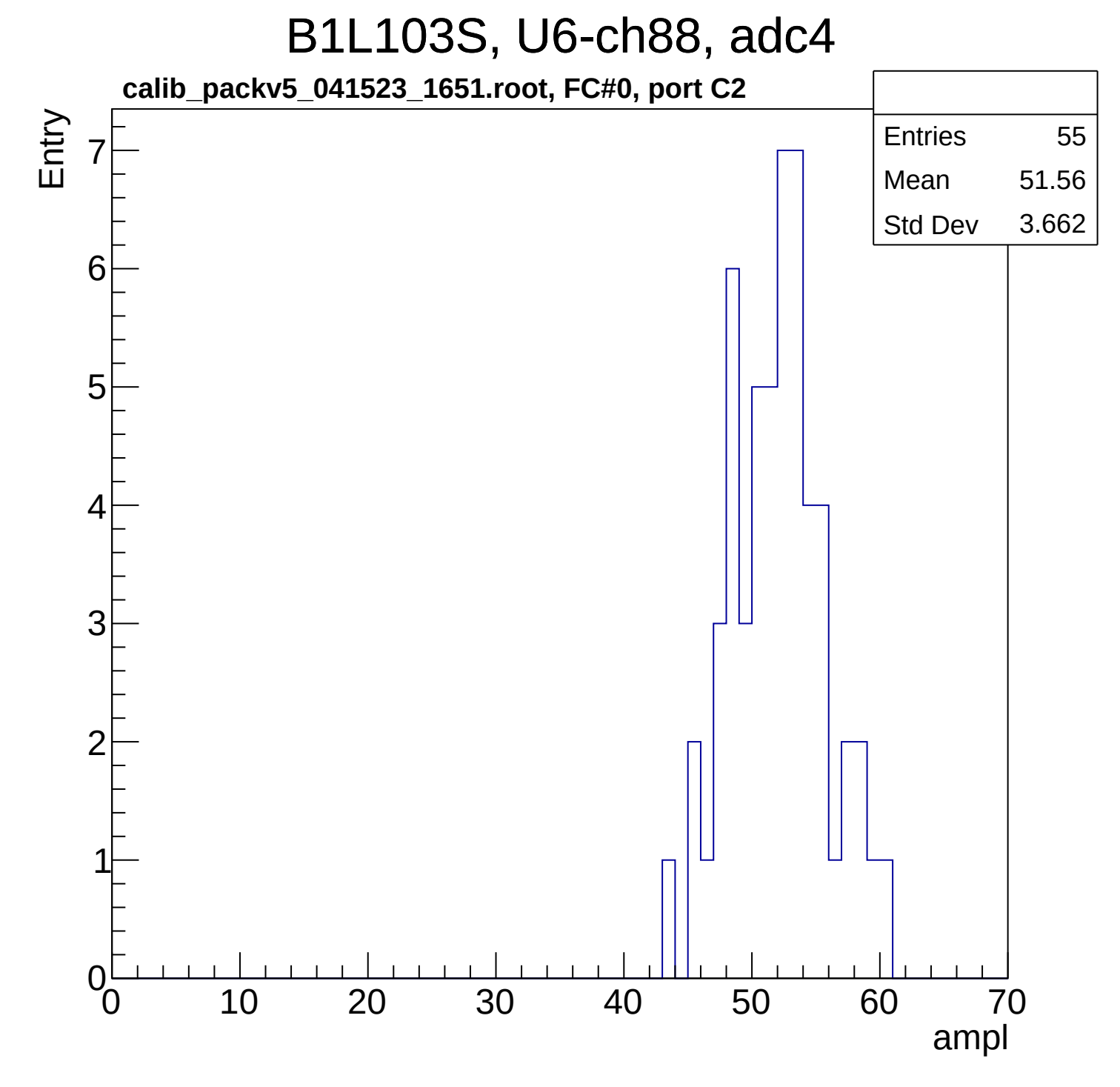
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch88, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 51.56
Std Dev 3.662
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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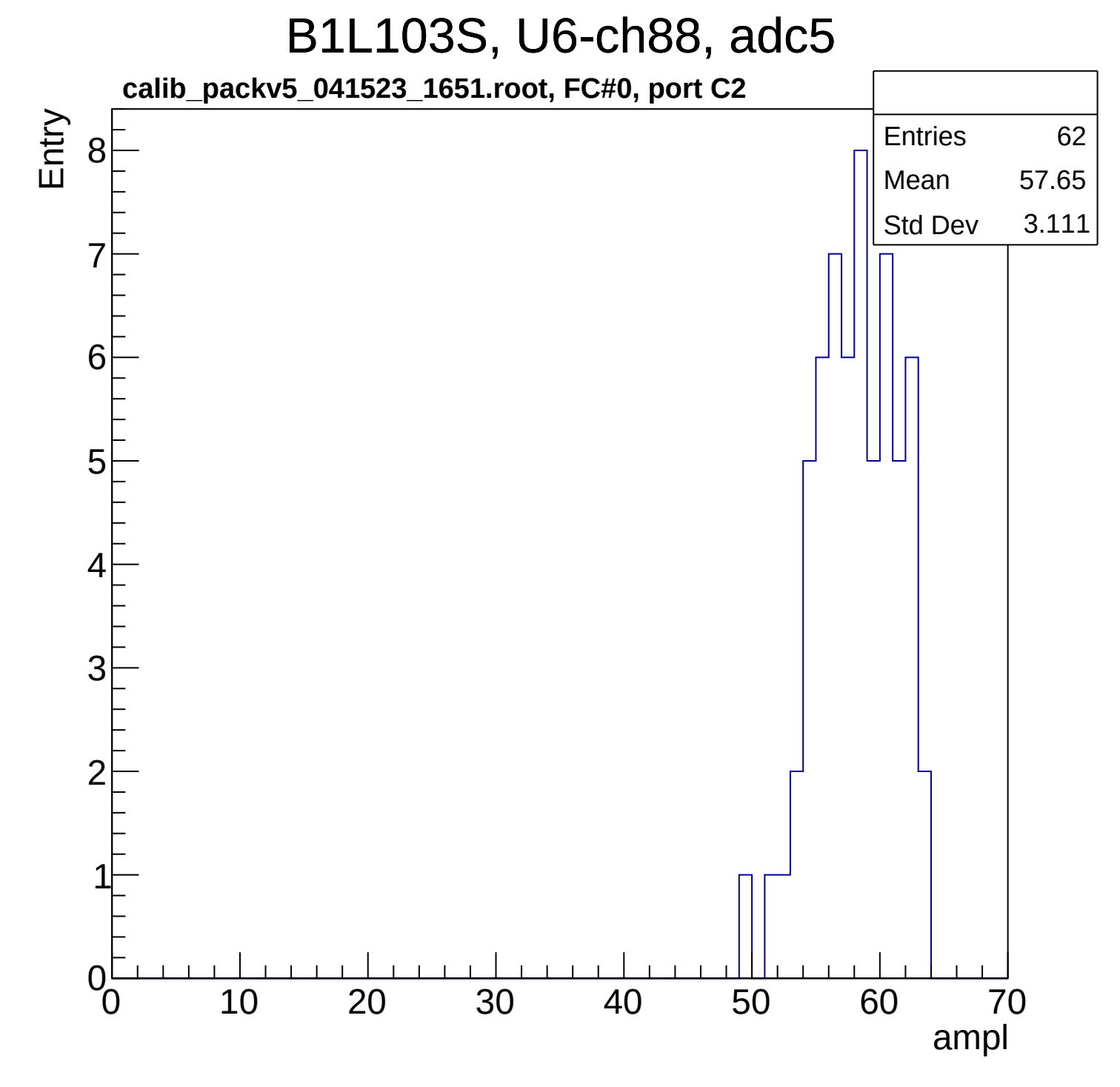
B1L103S, U6-ch88, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 57.65
Std Dev 3.111
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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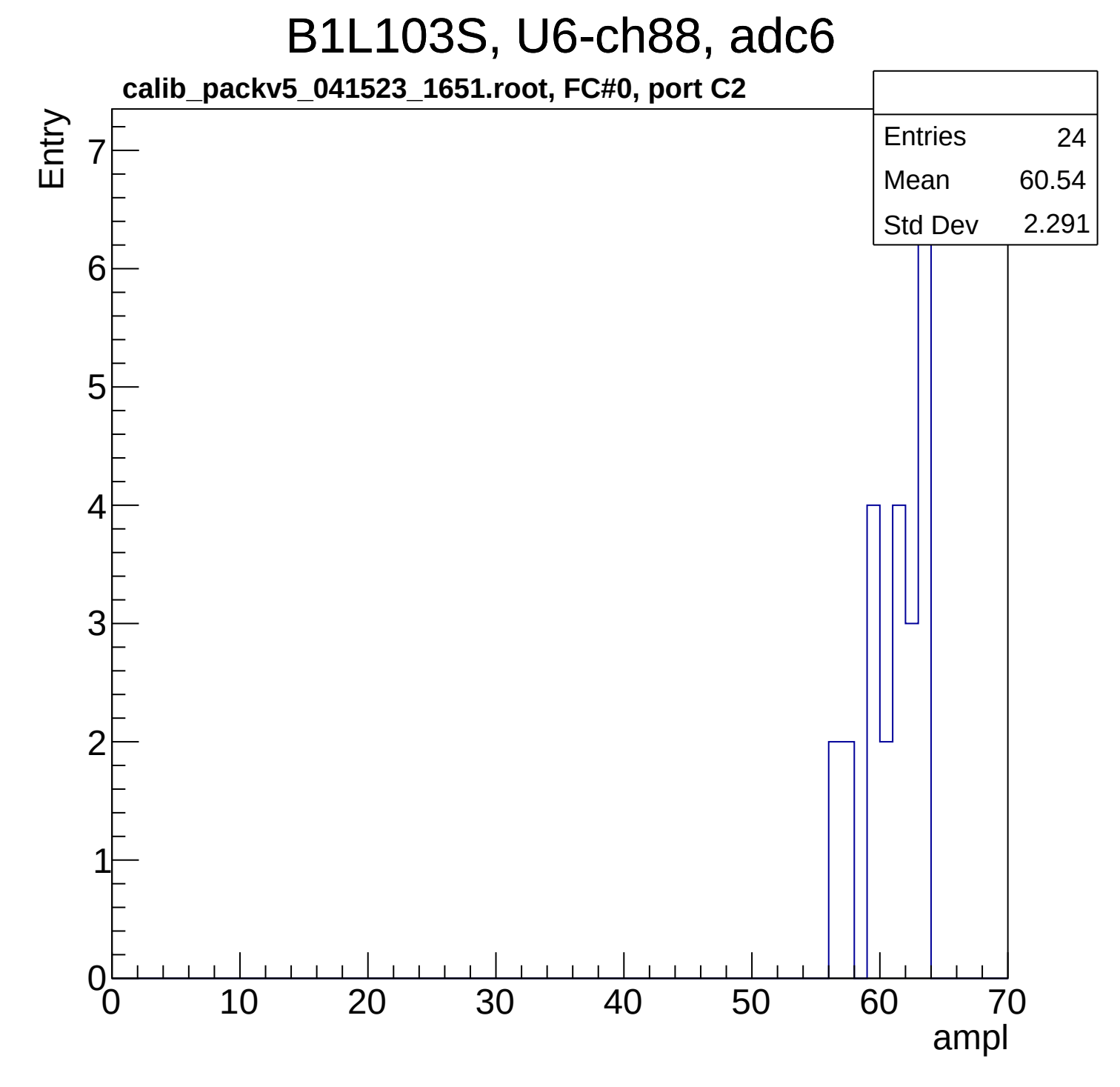
40
50
60
70


B1L103S, U6-ch88, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 60.54
Std Dev 2.291
Entry
ampl
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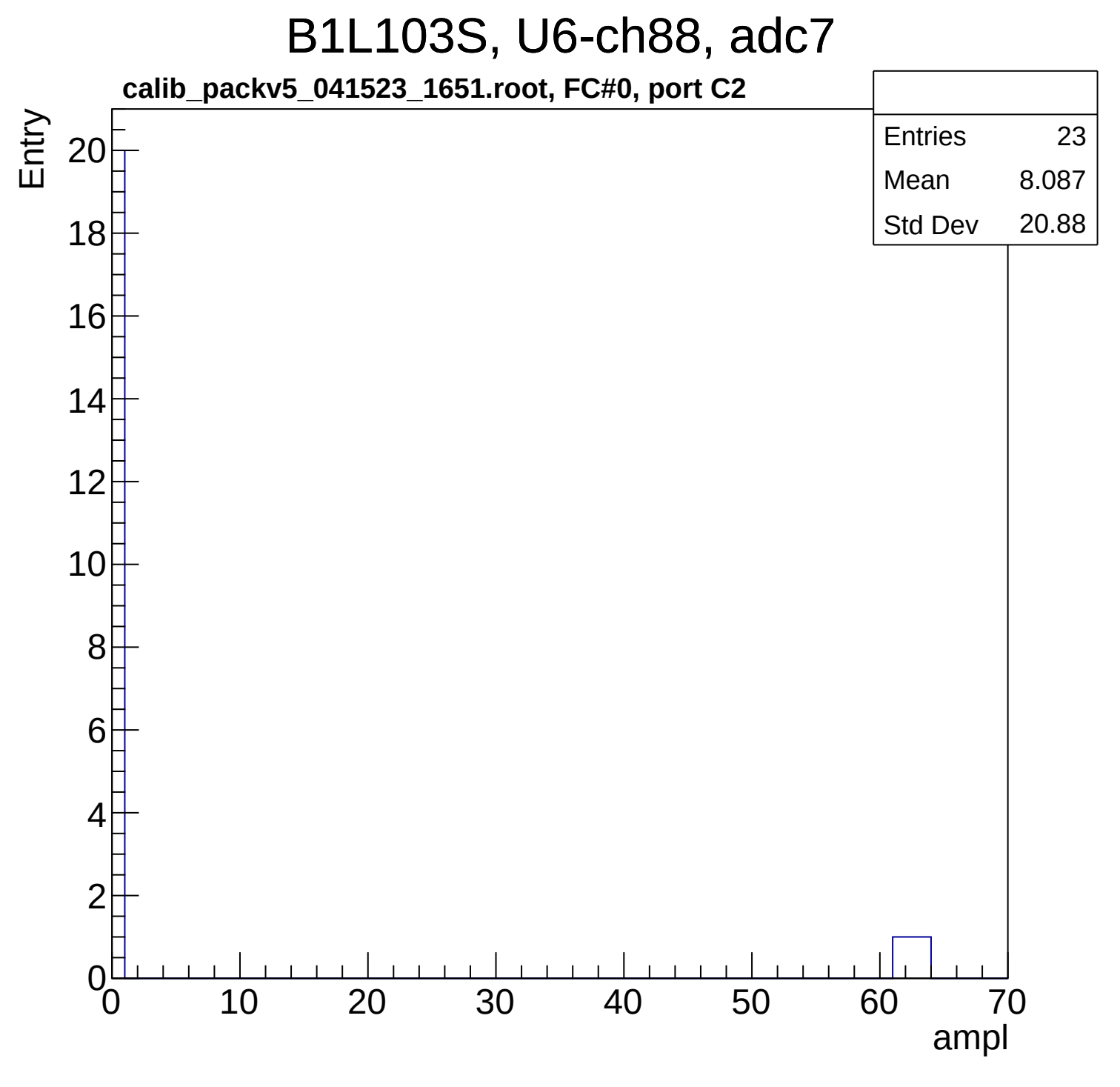
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U6-ch88, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 8.087
Std Dev 20.88
Entry
0
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8
10
12
14
16
18
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10
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30
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50
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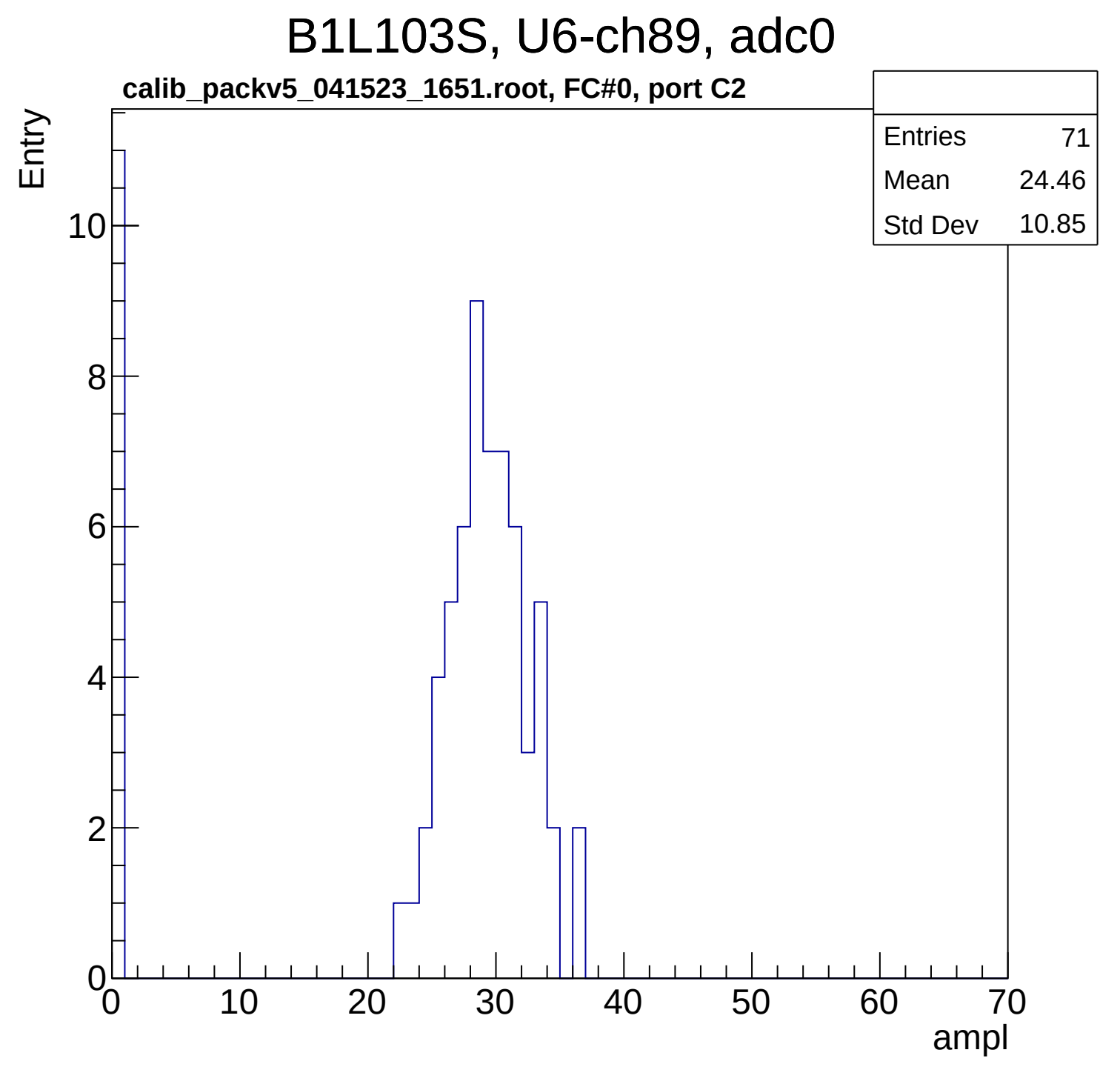
70
ampl


B1L103S, U6-ch89, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 24.46
Std Dev 10.85
Entry
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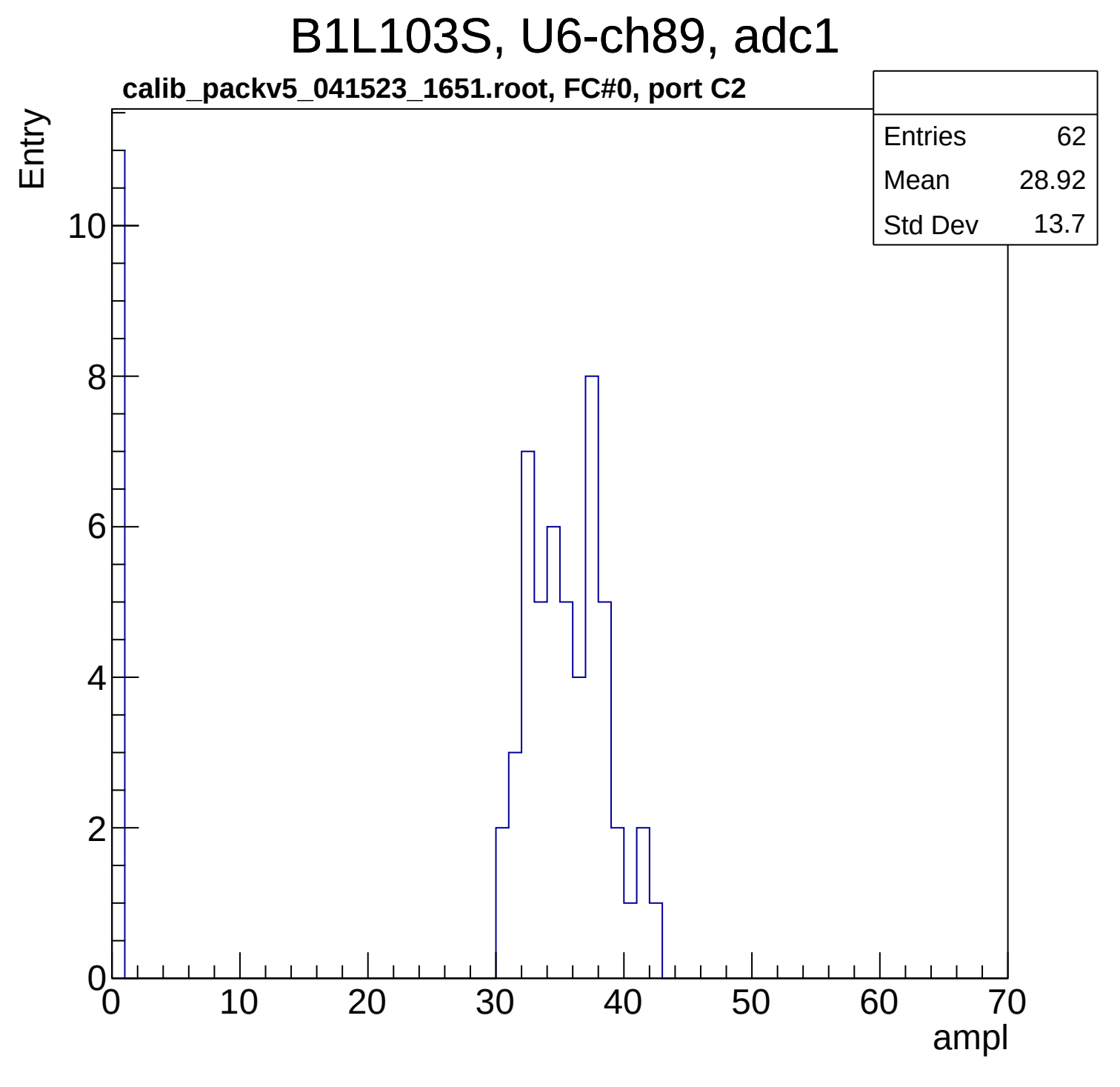
70
ampl


B1L103S, U6-ch89, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 28.92
Std Dev 13.7
Entry
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10
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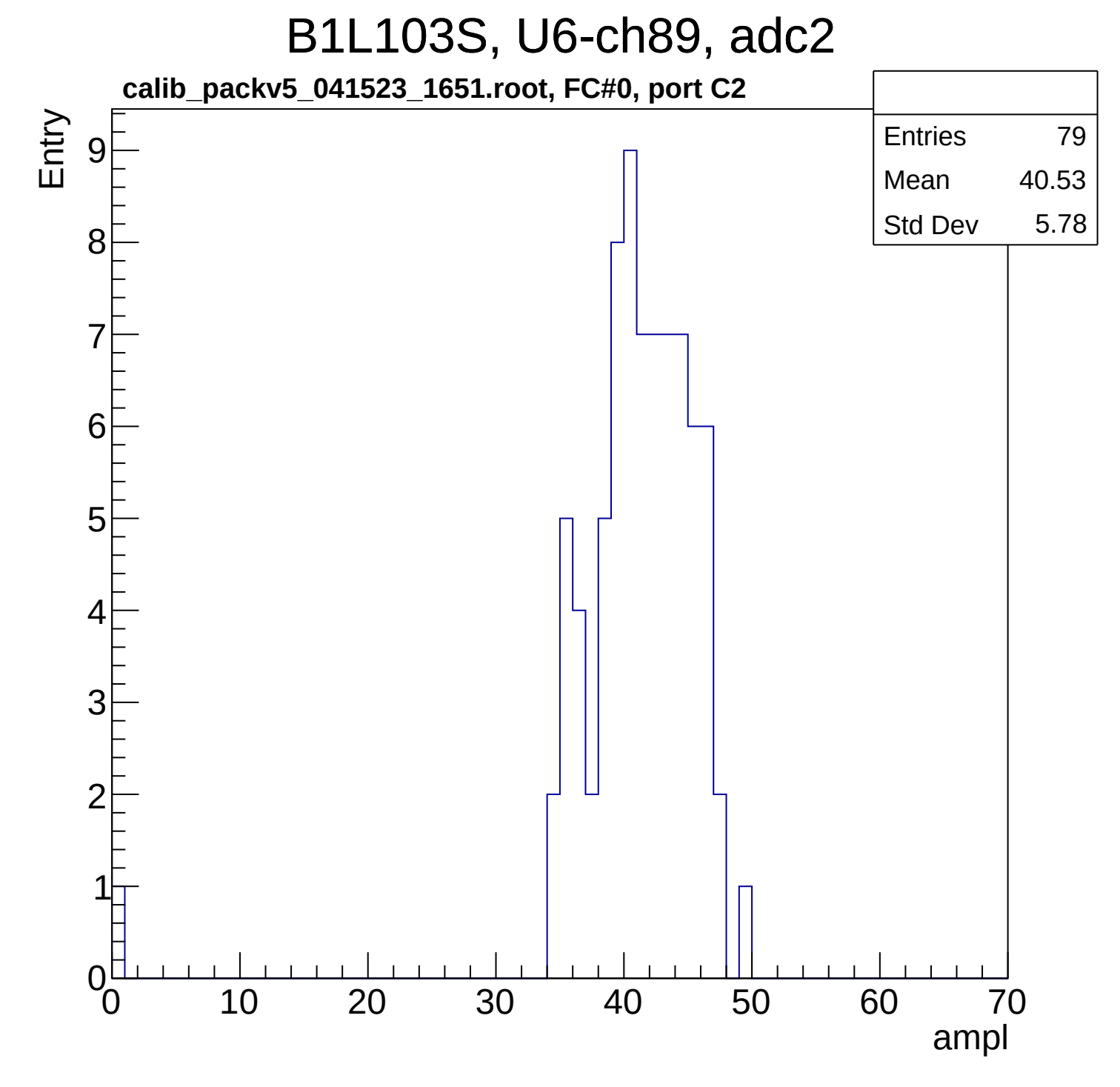
20
30
40
50
60
70
ampl


B1L103S, U6-ch89, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 40.53
Std Dev 5.78
Entry
ampl
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2
3
4
5
6
7
8
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0
10
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40
50
60
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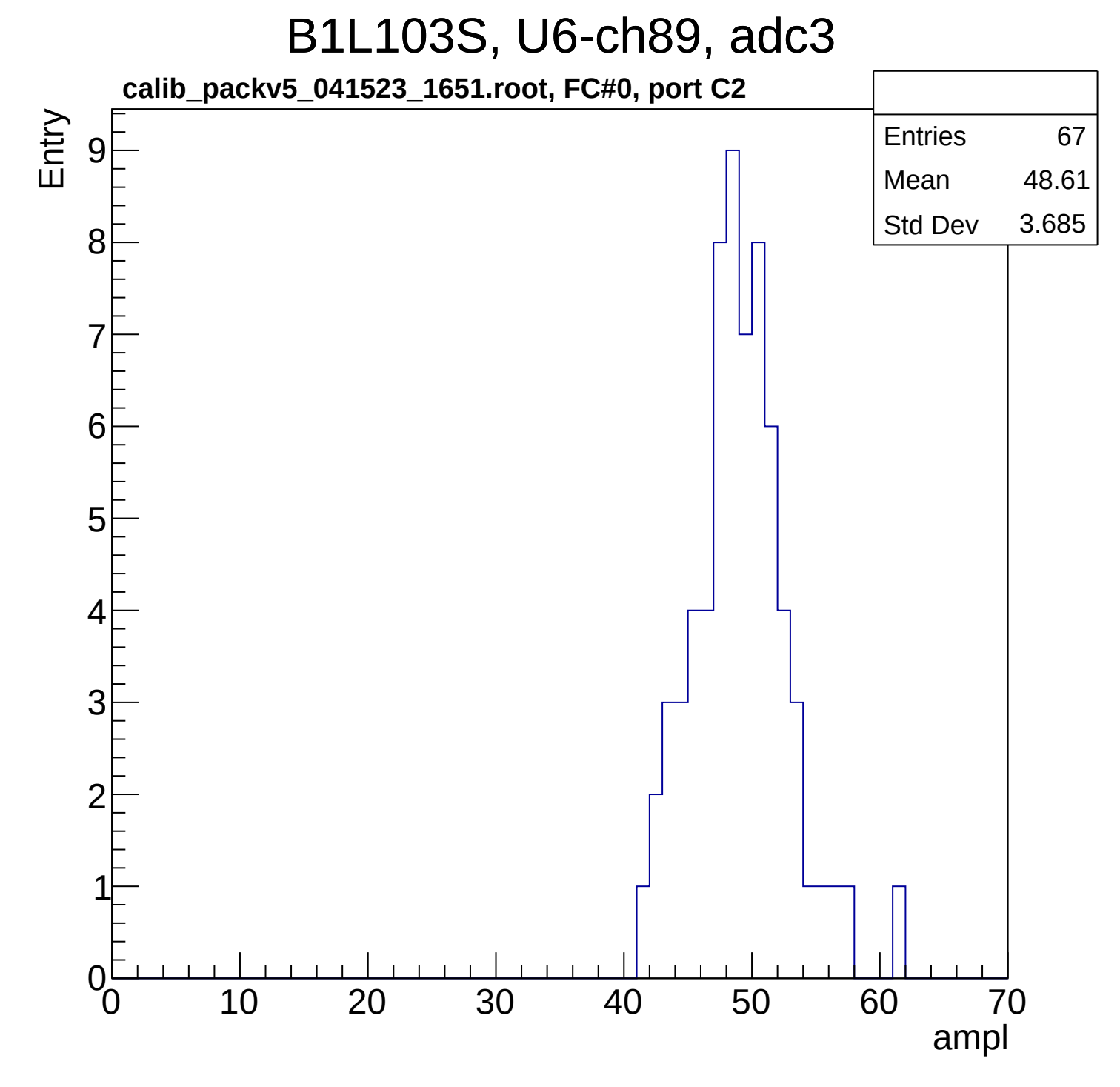
B1L103S, U6-ch89, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 48.61
Std Dev 3.685
Entry
ampl
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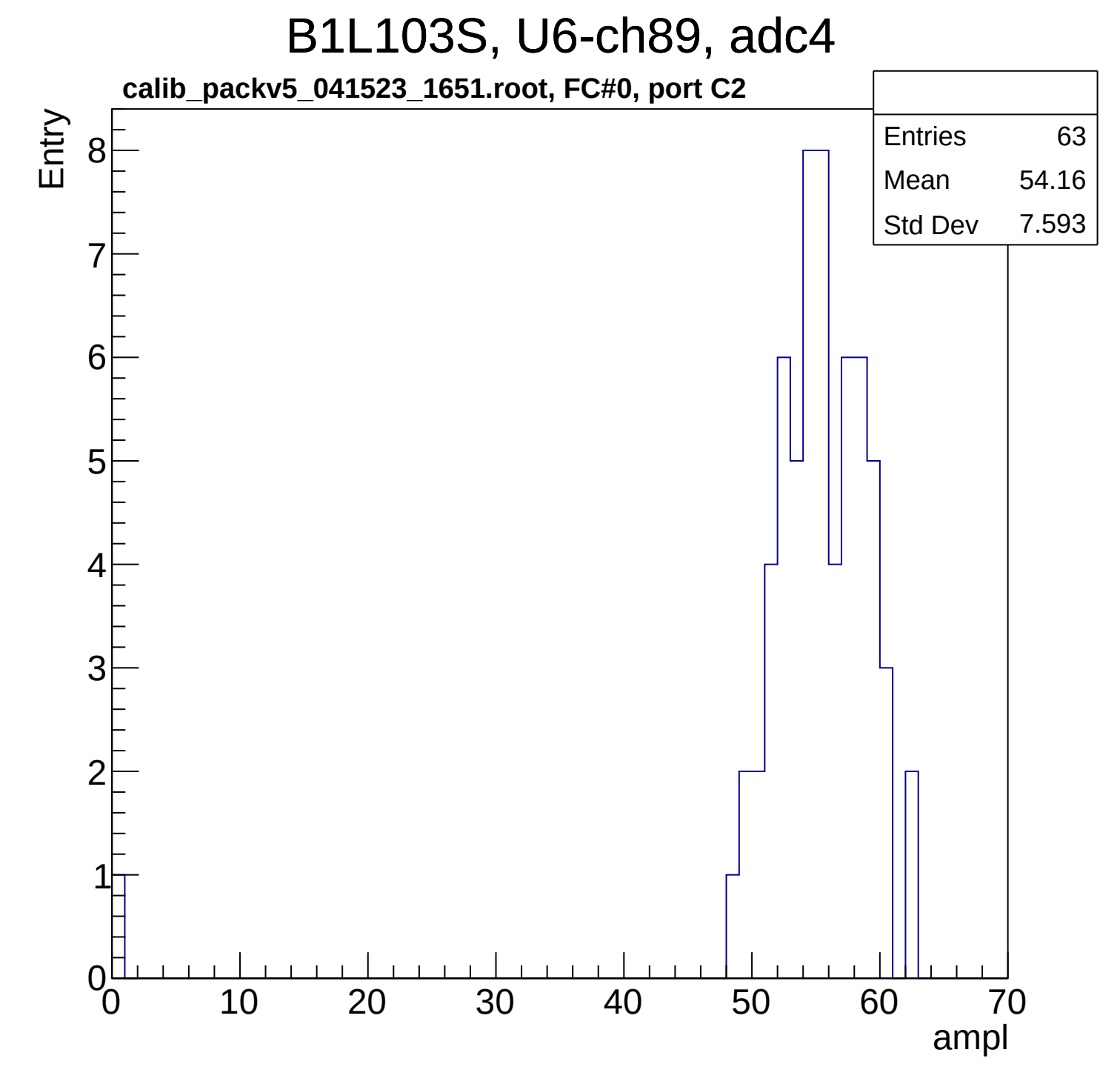
B1L103S, U6-ch89, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 54.16
Std Dev 7.593
Entry
ampl
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0
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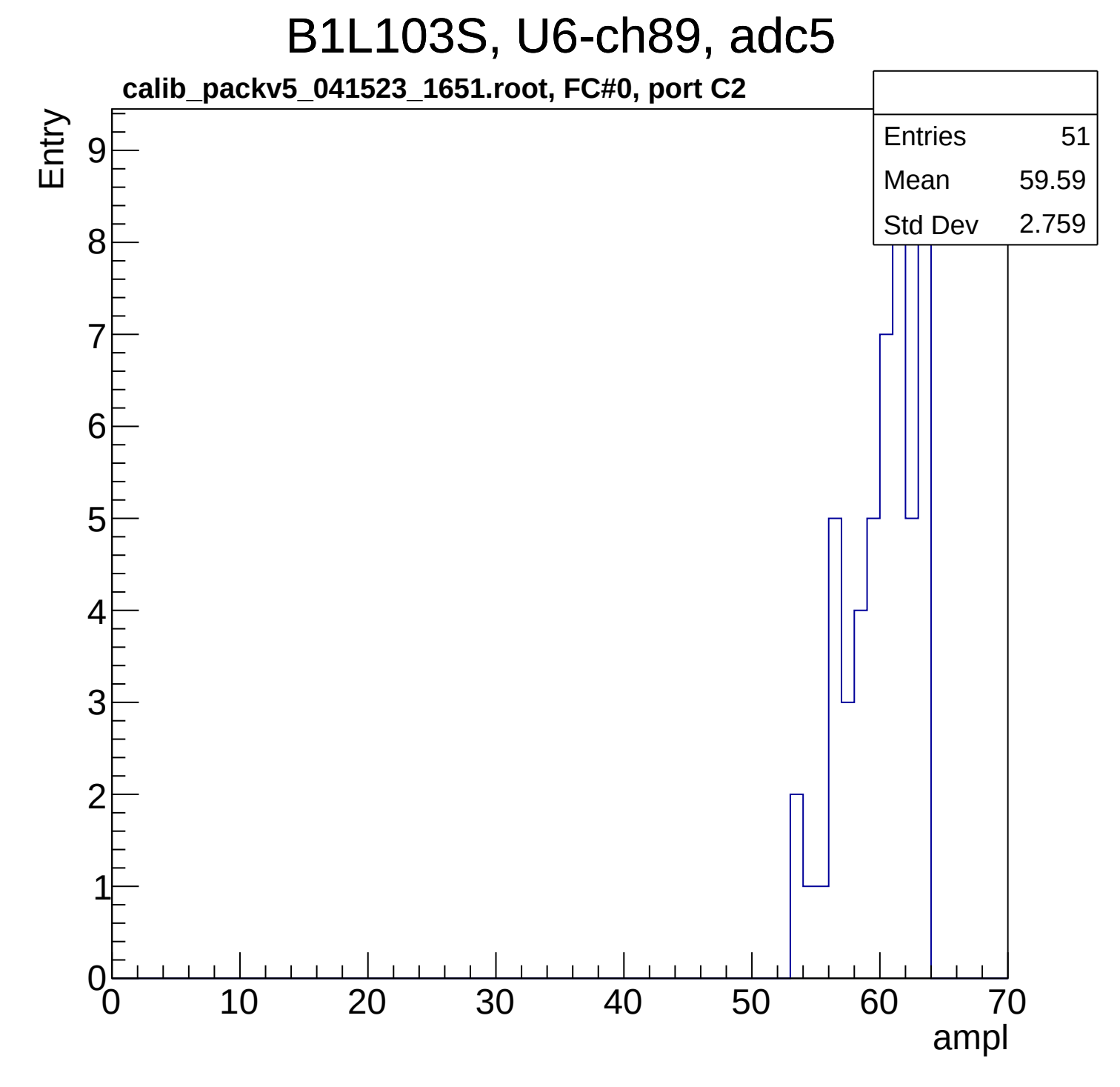
B1L103S, U6-ch89, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 59.59
Std Dev 2.759
Entry
ampl
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2
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4
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6
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0
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60
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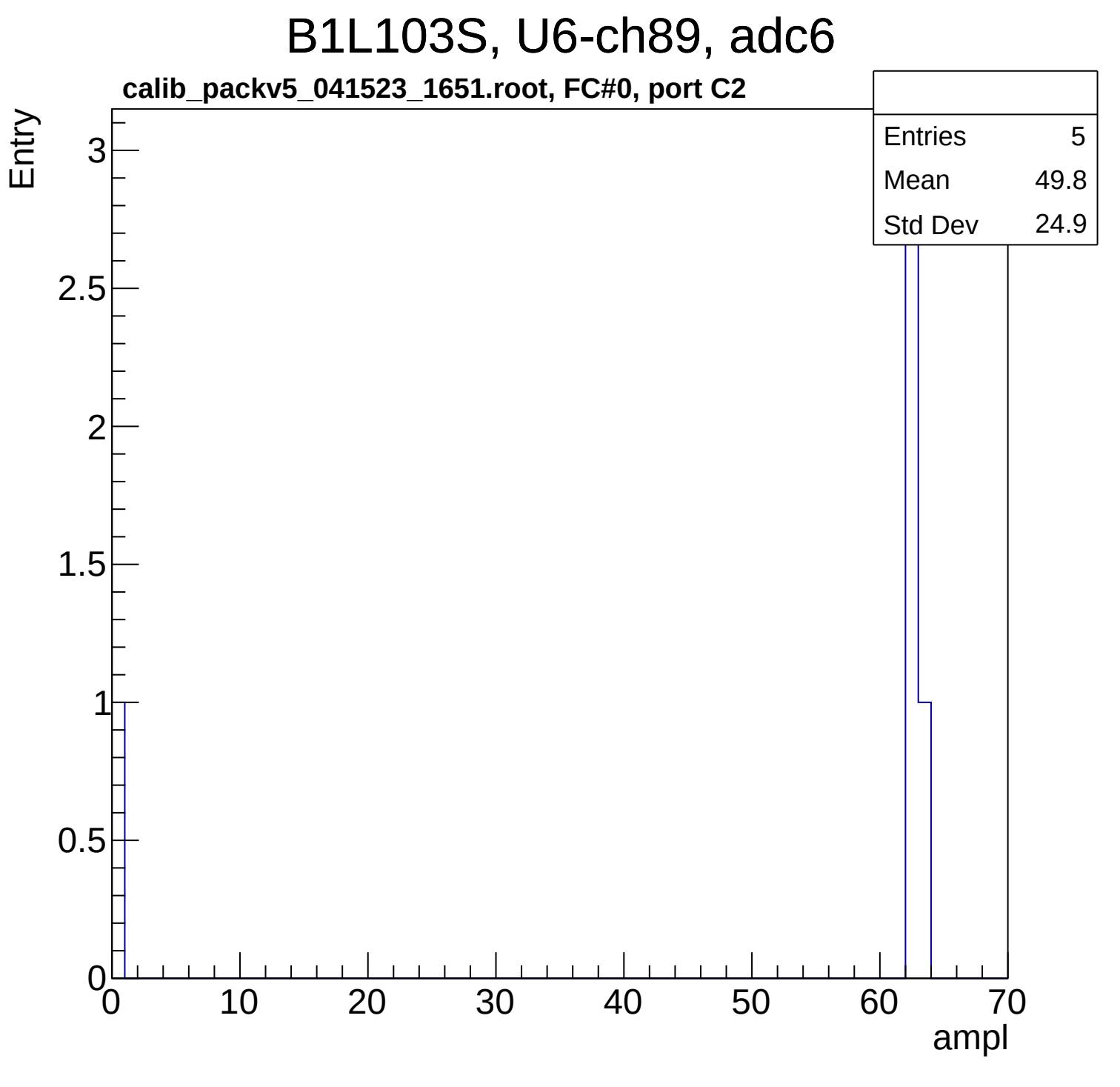
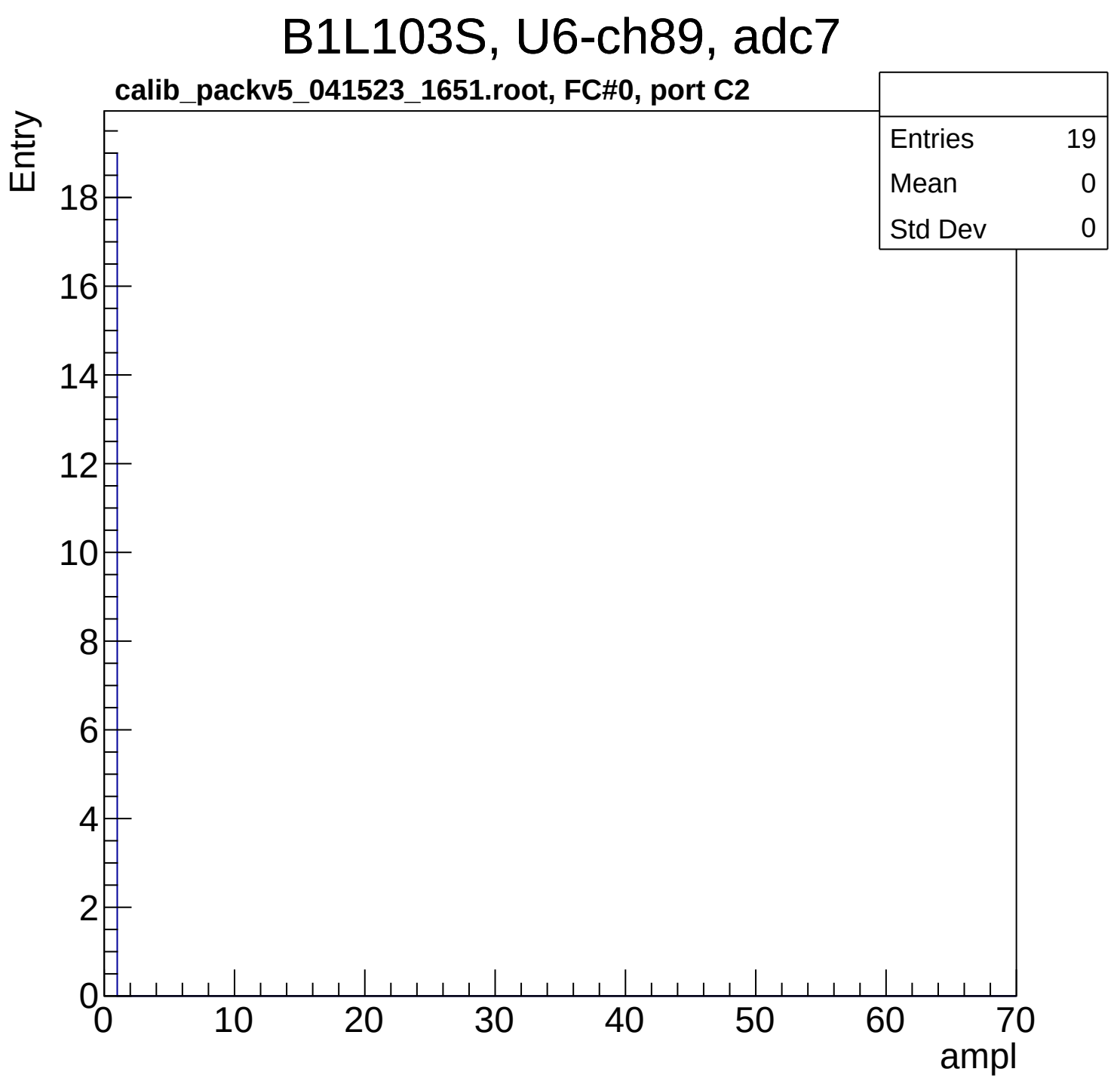
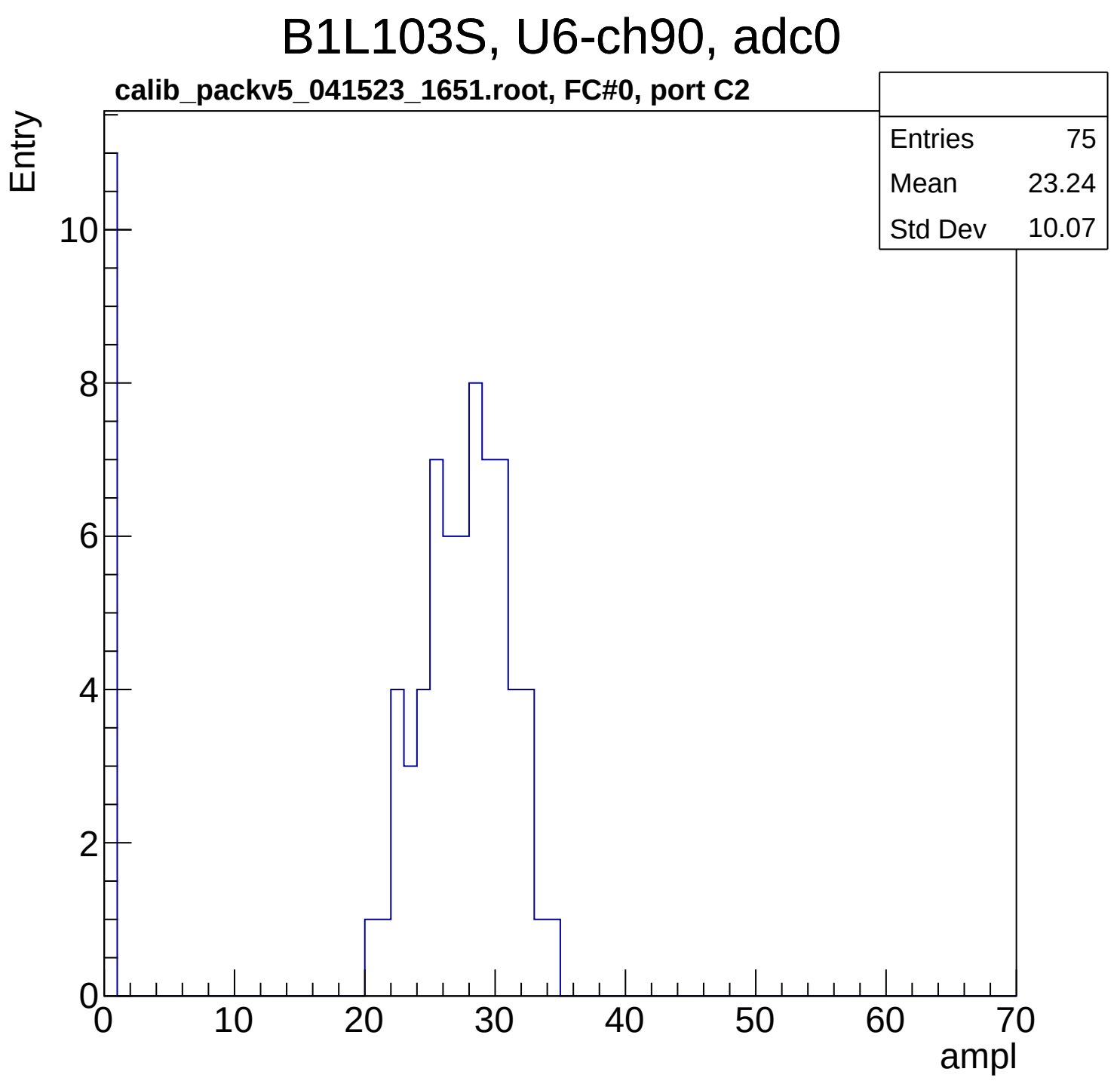
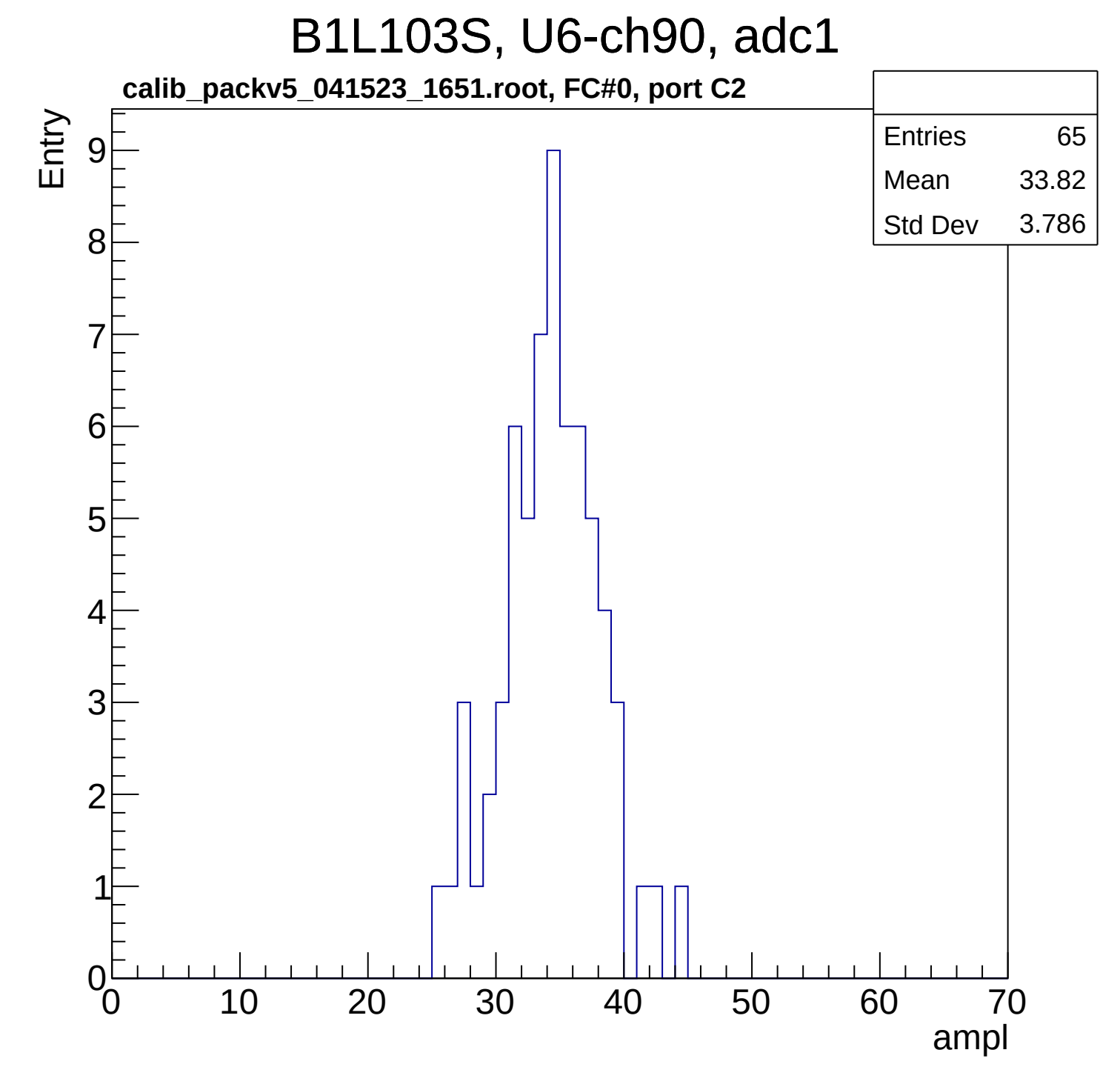

B1L103S, U6-ch89, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 49.8
Std Dev 24.9
Entry
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch89, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch90, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 23.24
Std Dev 10.07
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch90, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 33.82
Std Dev 3.786
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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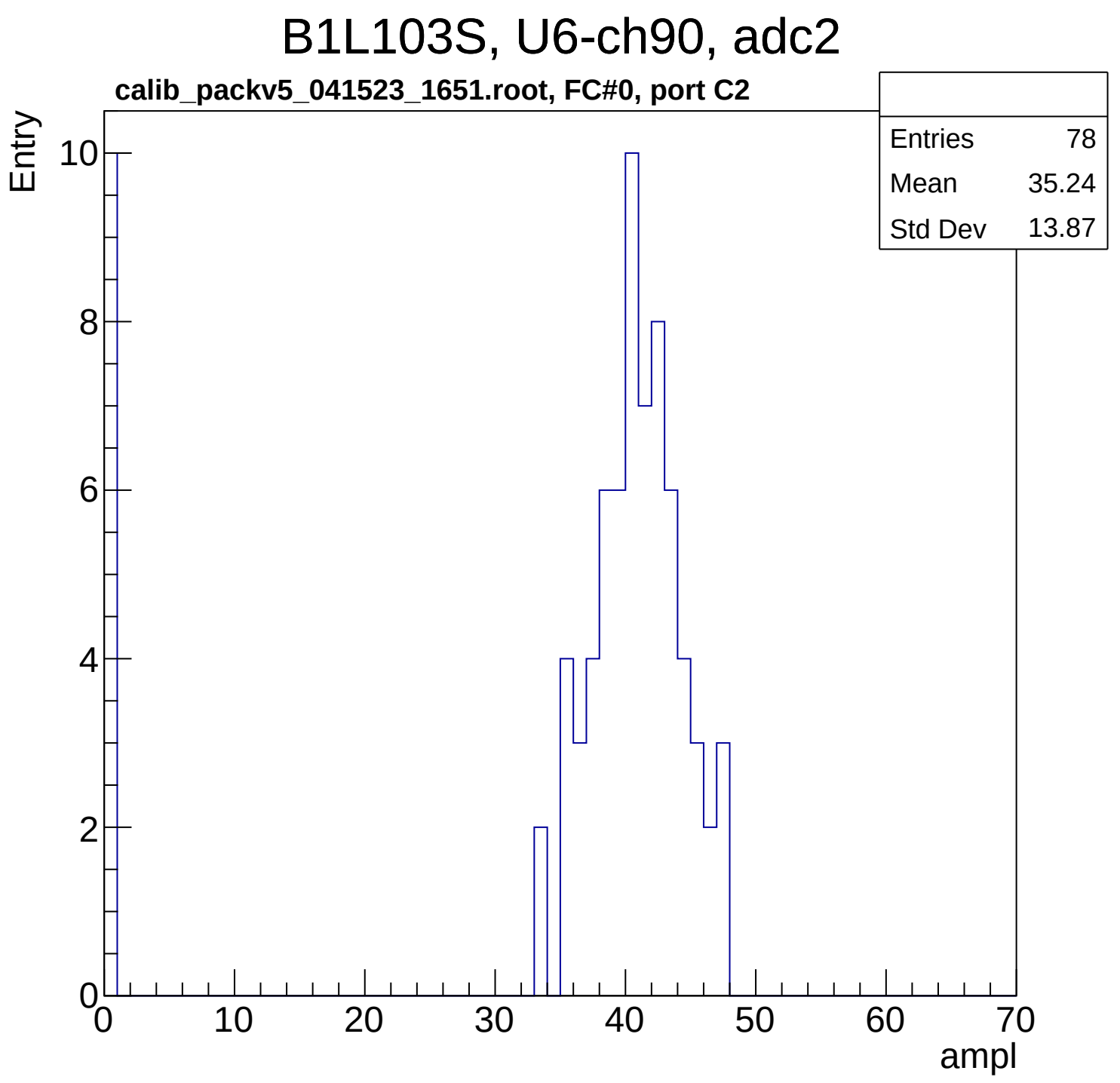
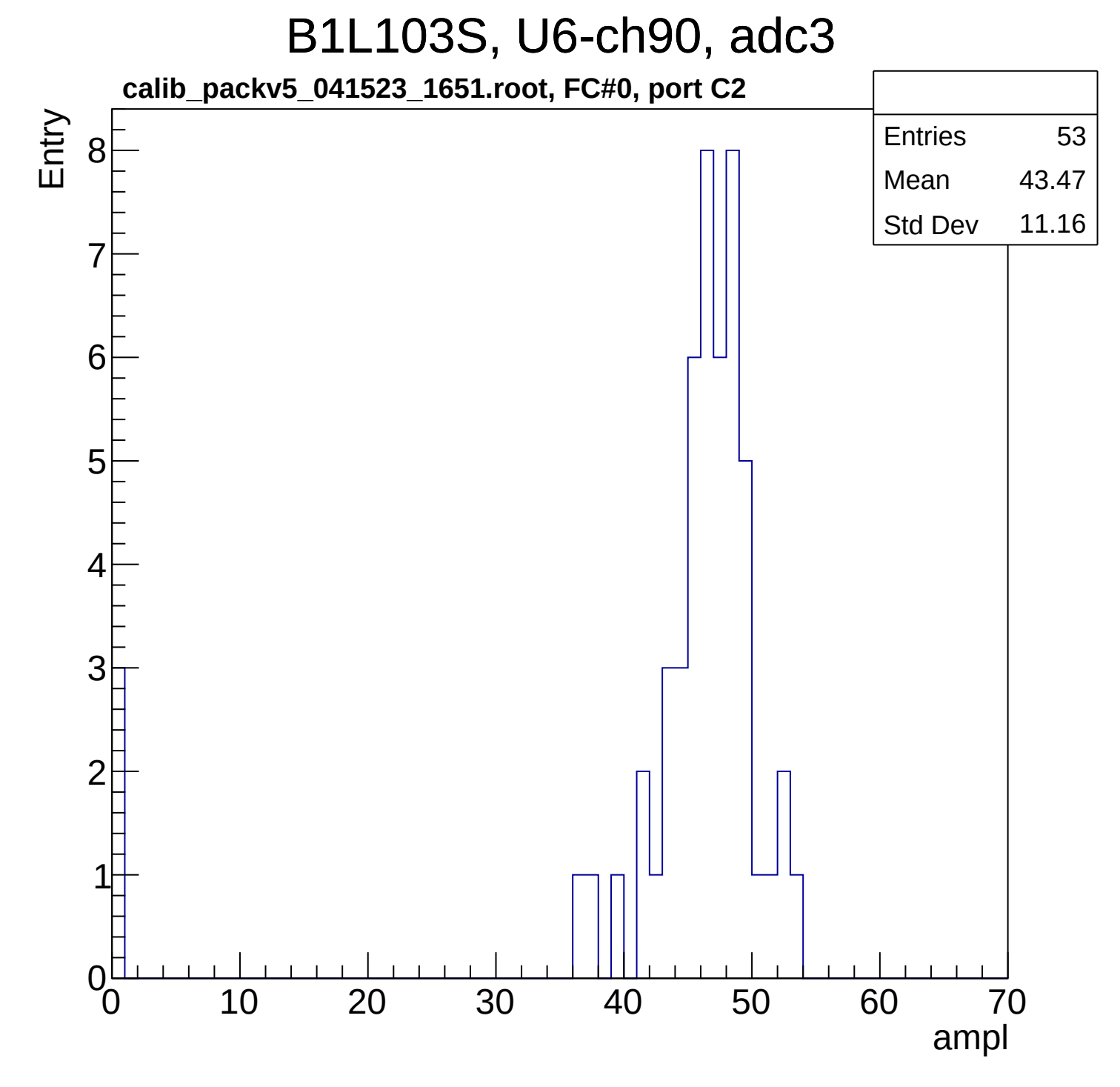
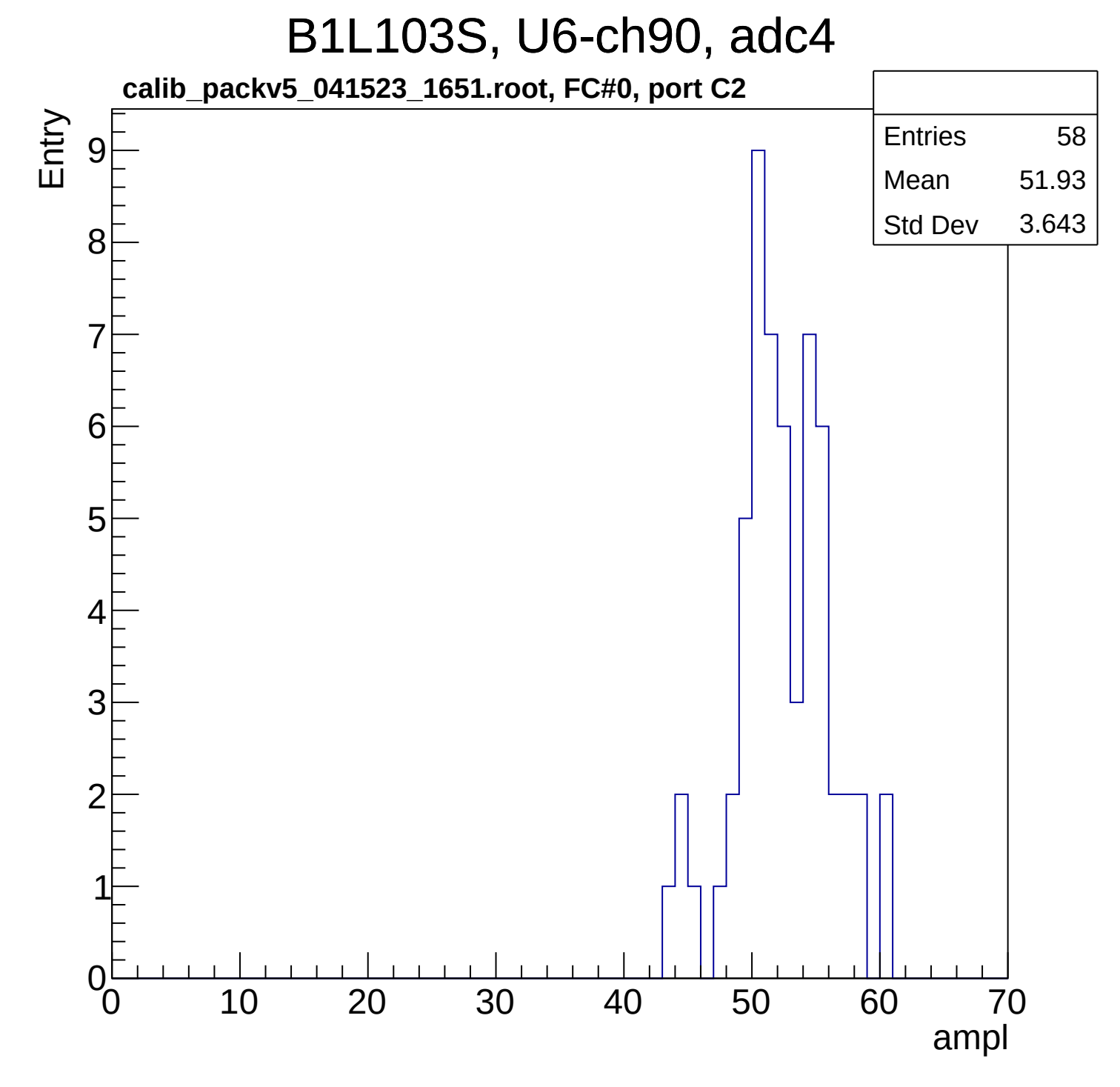
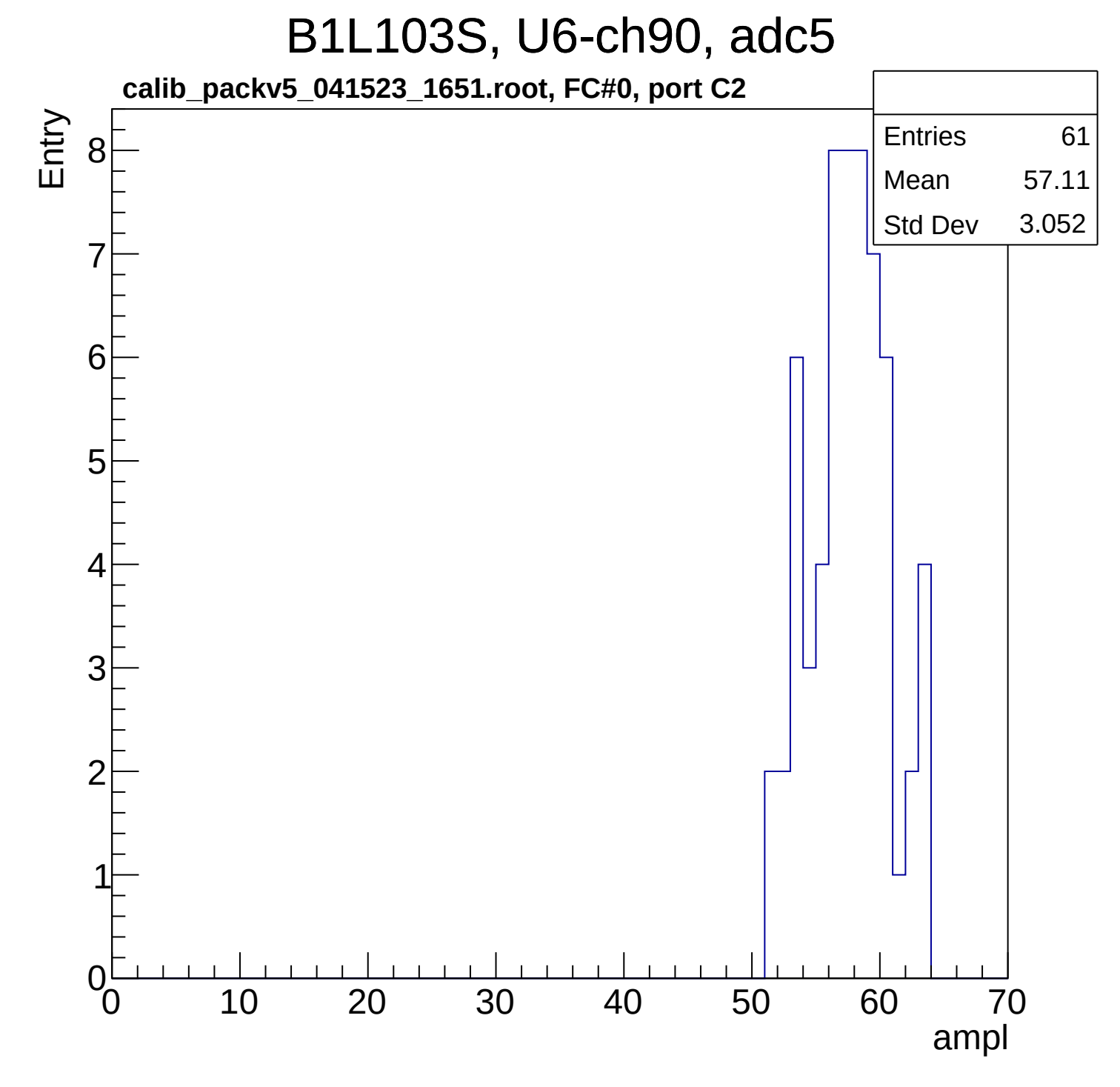
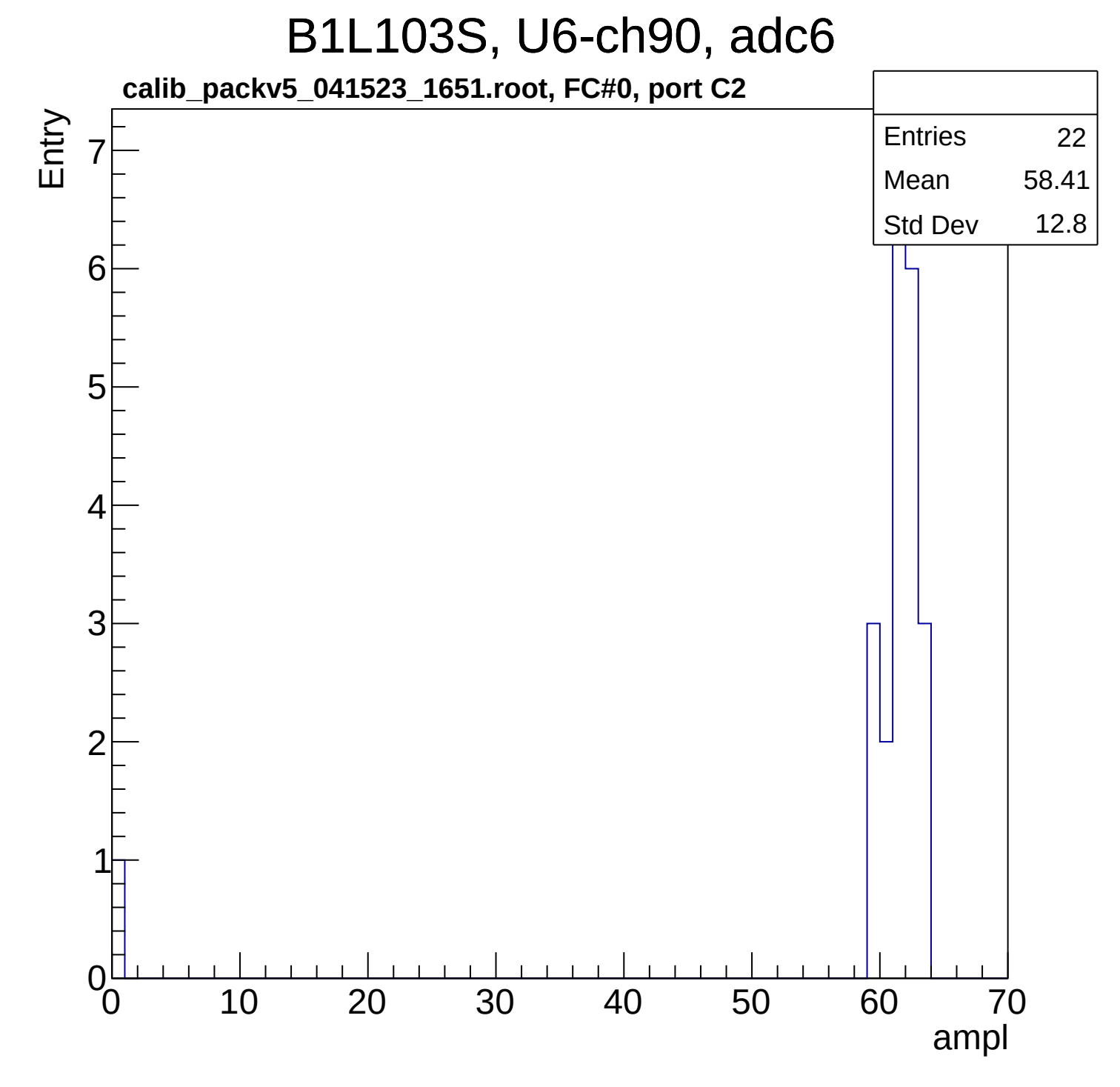
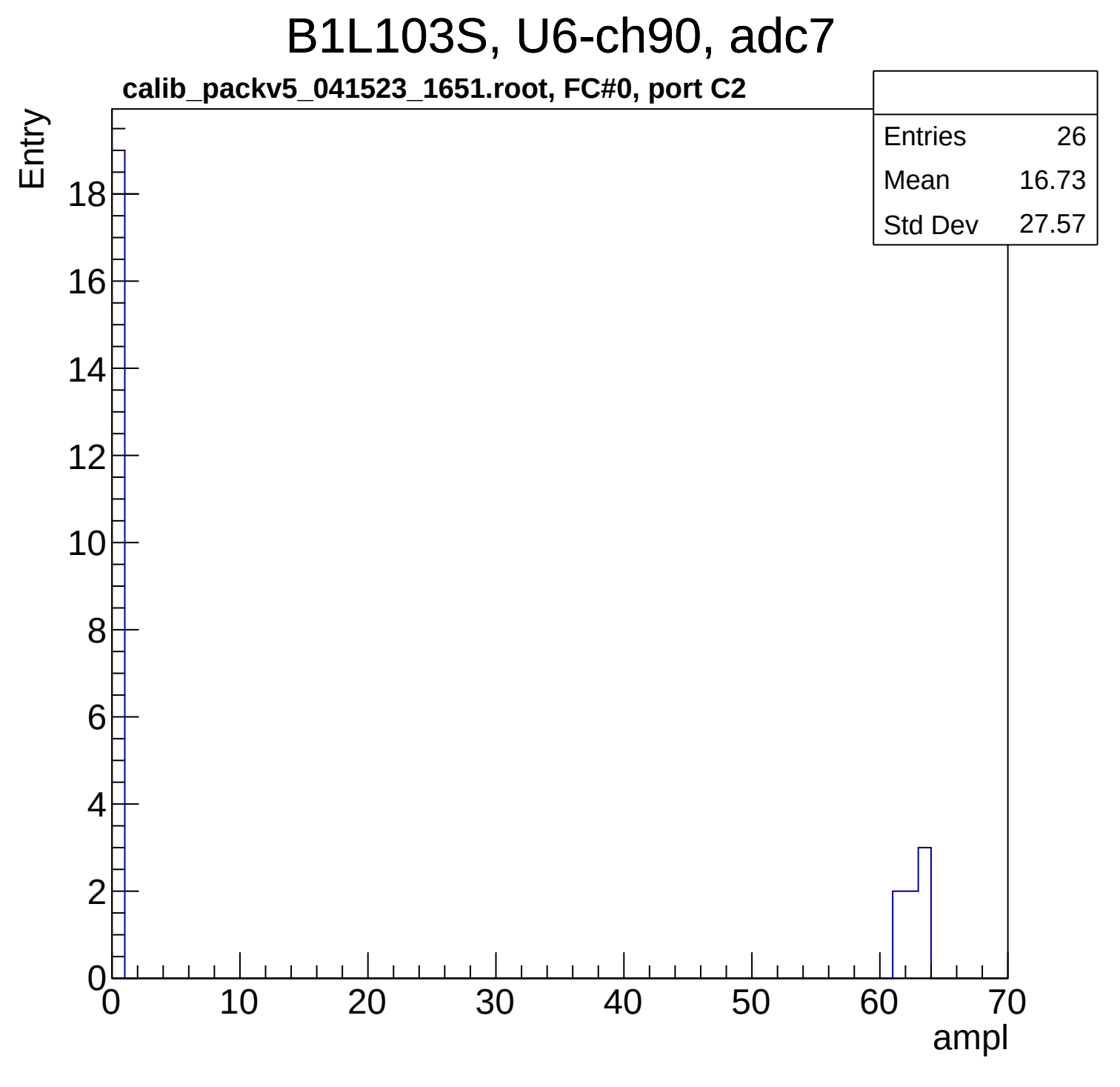

B1L103S, U6-ch90, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 35.24
Std Dev 13.87
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

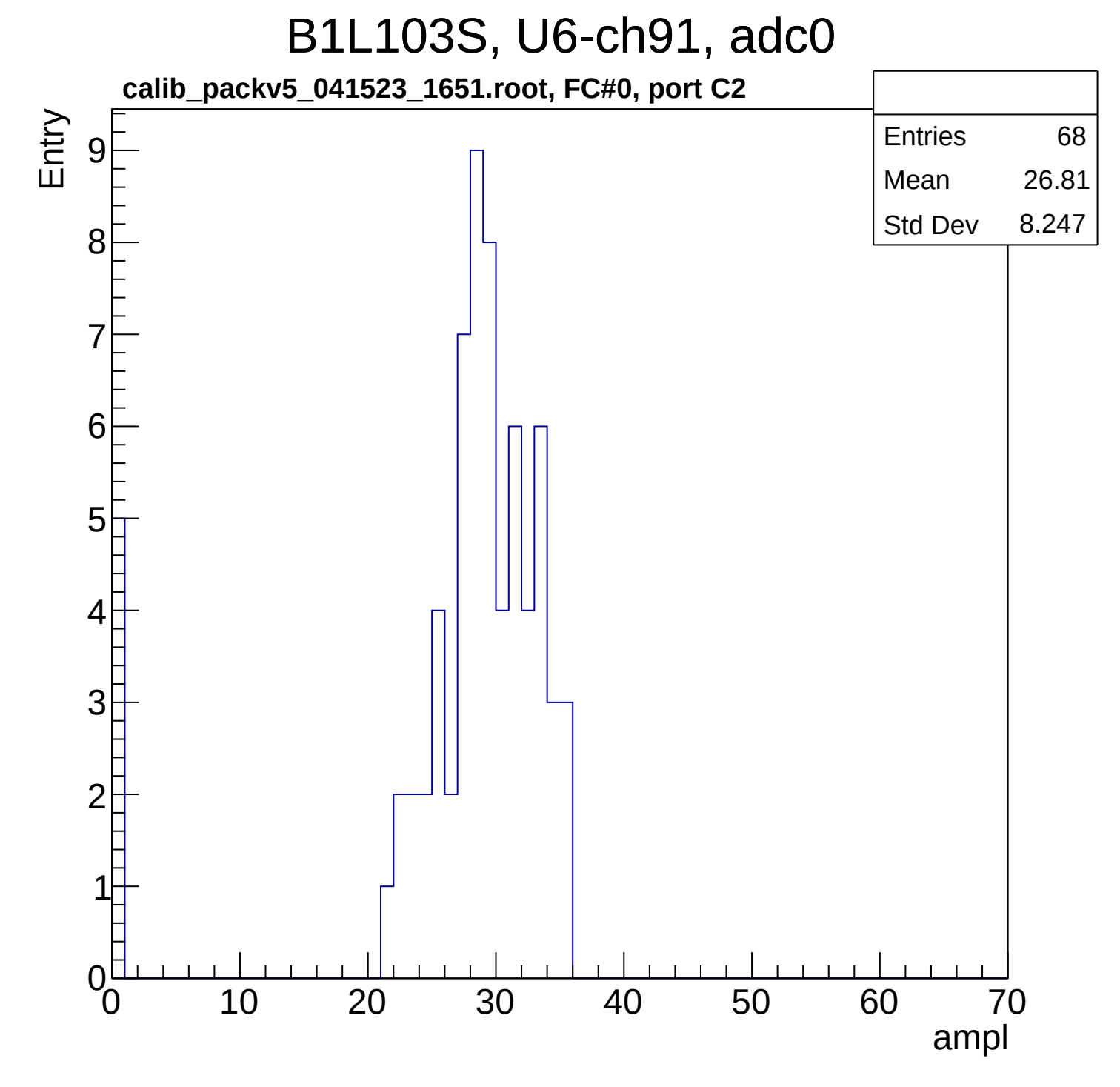

B1L103S, U6-ch90, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 43.47
Std Dev 11.16
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

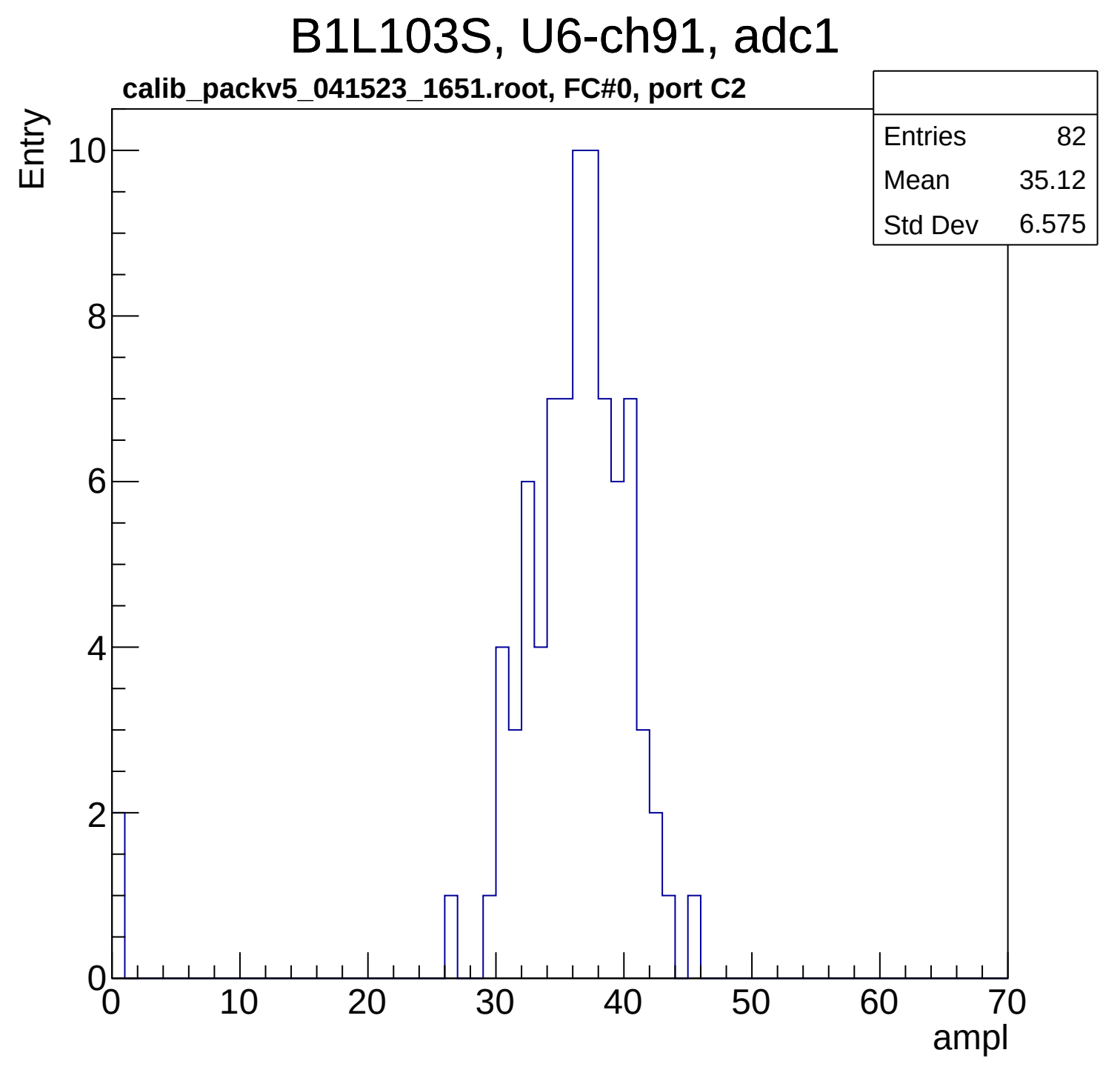

B1L103S, U6-ch90, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 51.93
Std Dev 3.643
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

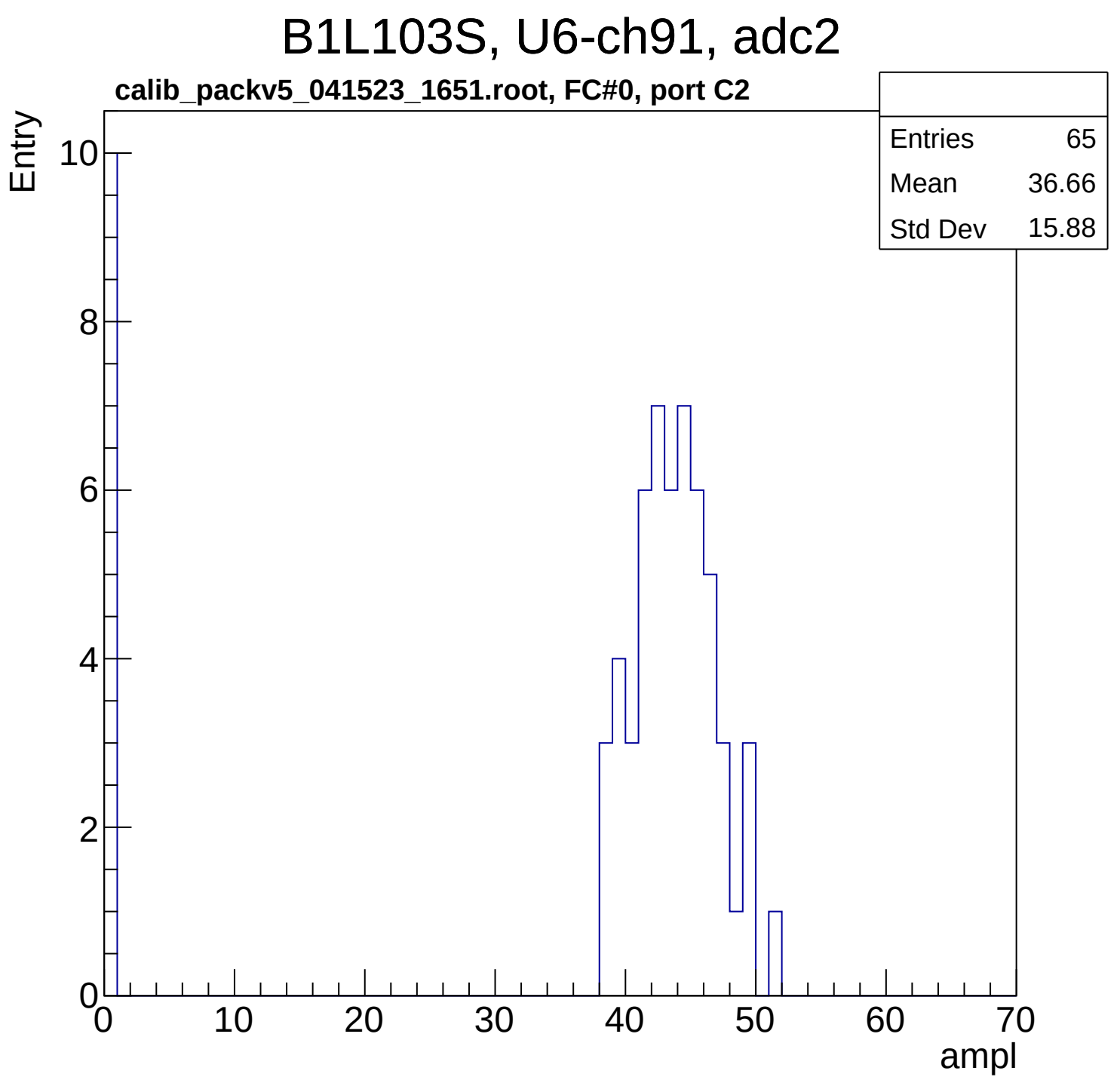

B1L103S, U6-ch90, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 57.11
Std Dev 3.052
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

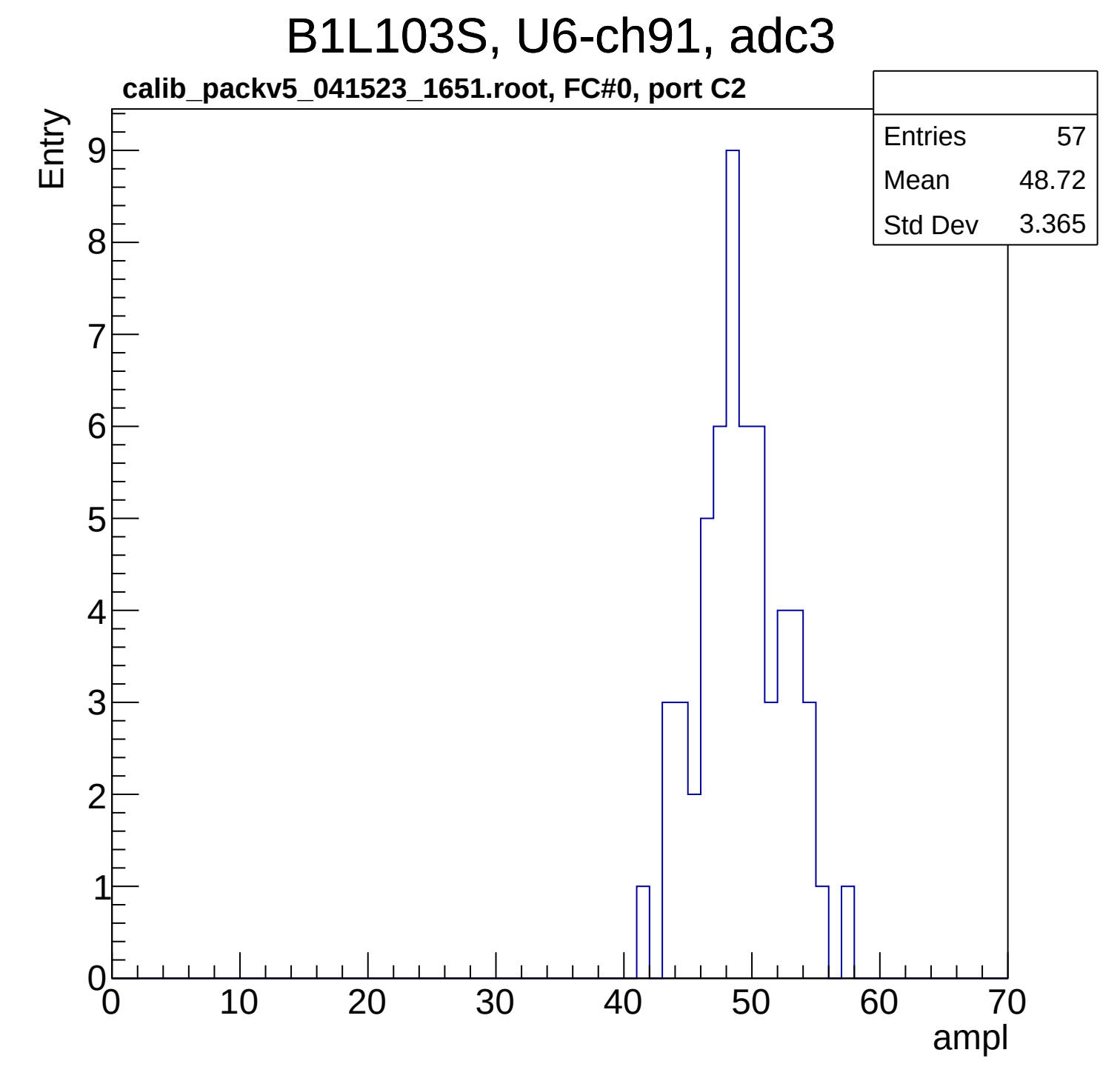

B1L103S, U6-ch90, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 58.41
Std Dev 12.8
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U6-ch90, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 16.73
Std Dev 27.57
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch91, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 26.81
Std Dev 8.247
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch91, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 35.12
Std Dev 6.575
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U6-ch91, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 36.66
Std Dev 15.88
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch91, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 48.72
Std Dev 3.365
Entry
ampl
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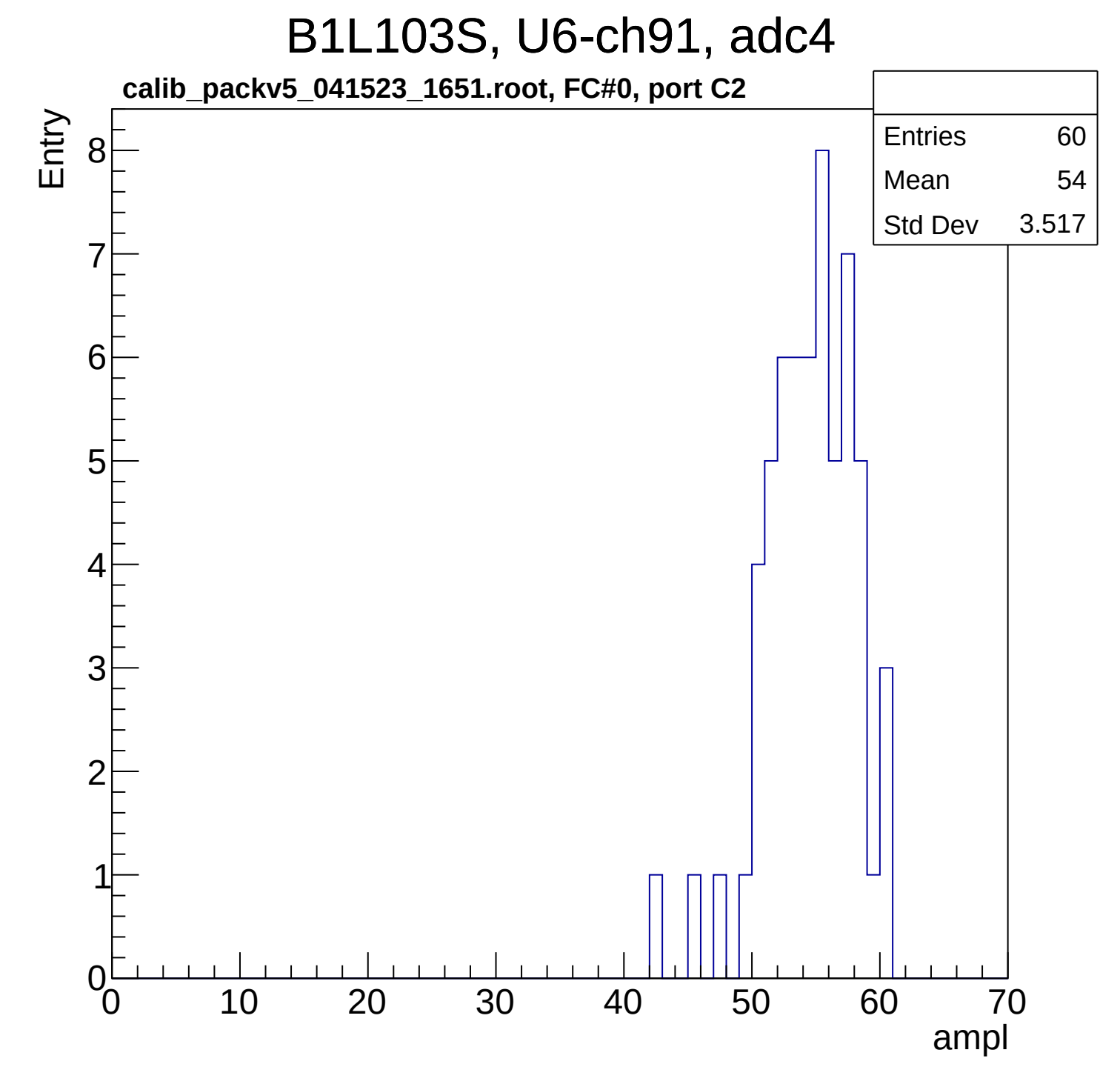
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch91, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 54
Std Dev 3.517
Entry
ampl
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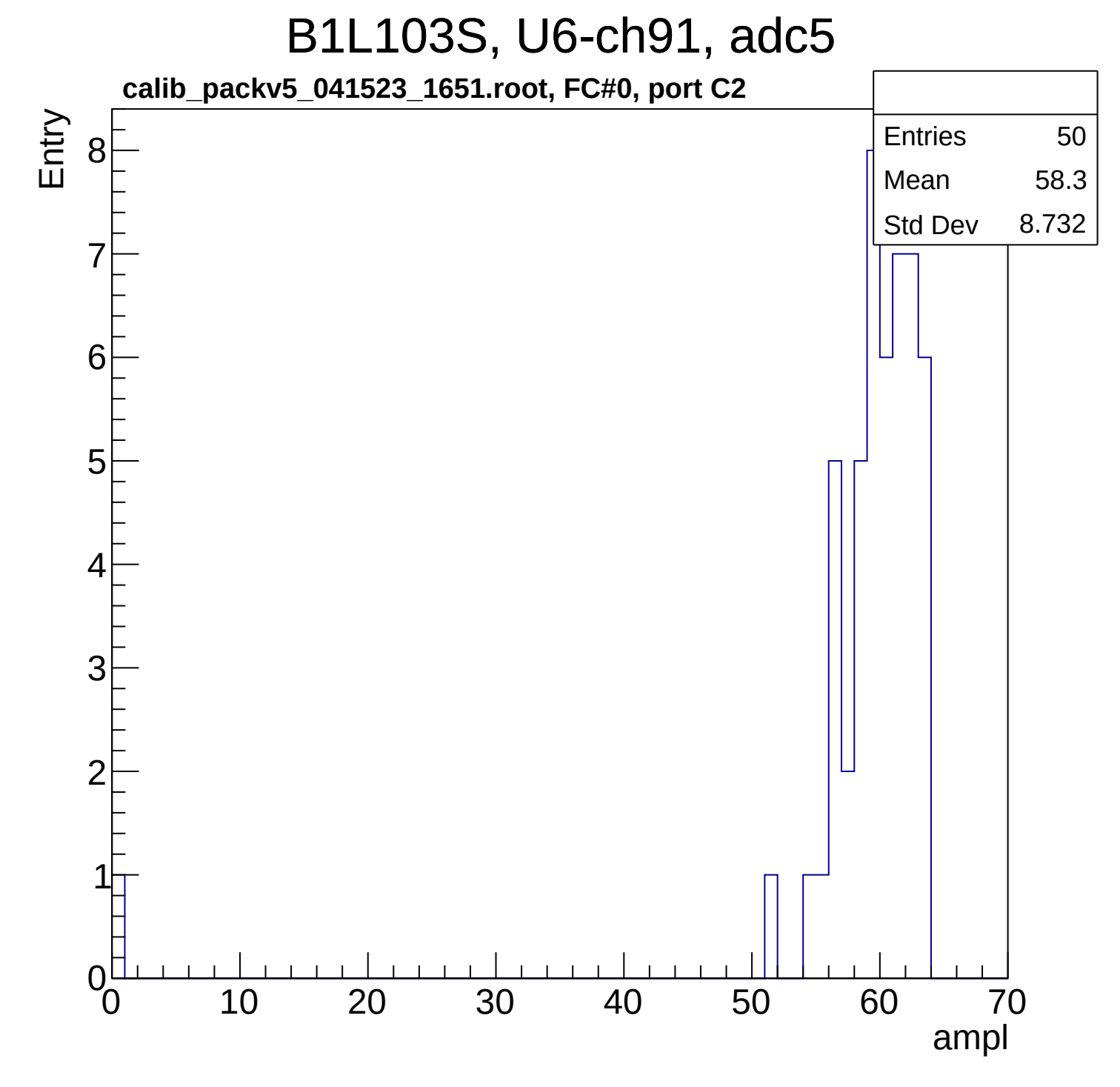
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch91, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 58.3
Std Dev 8.732
Entry
ampl
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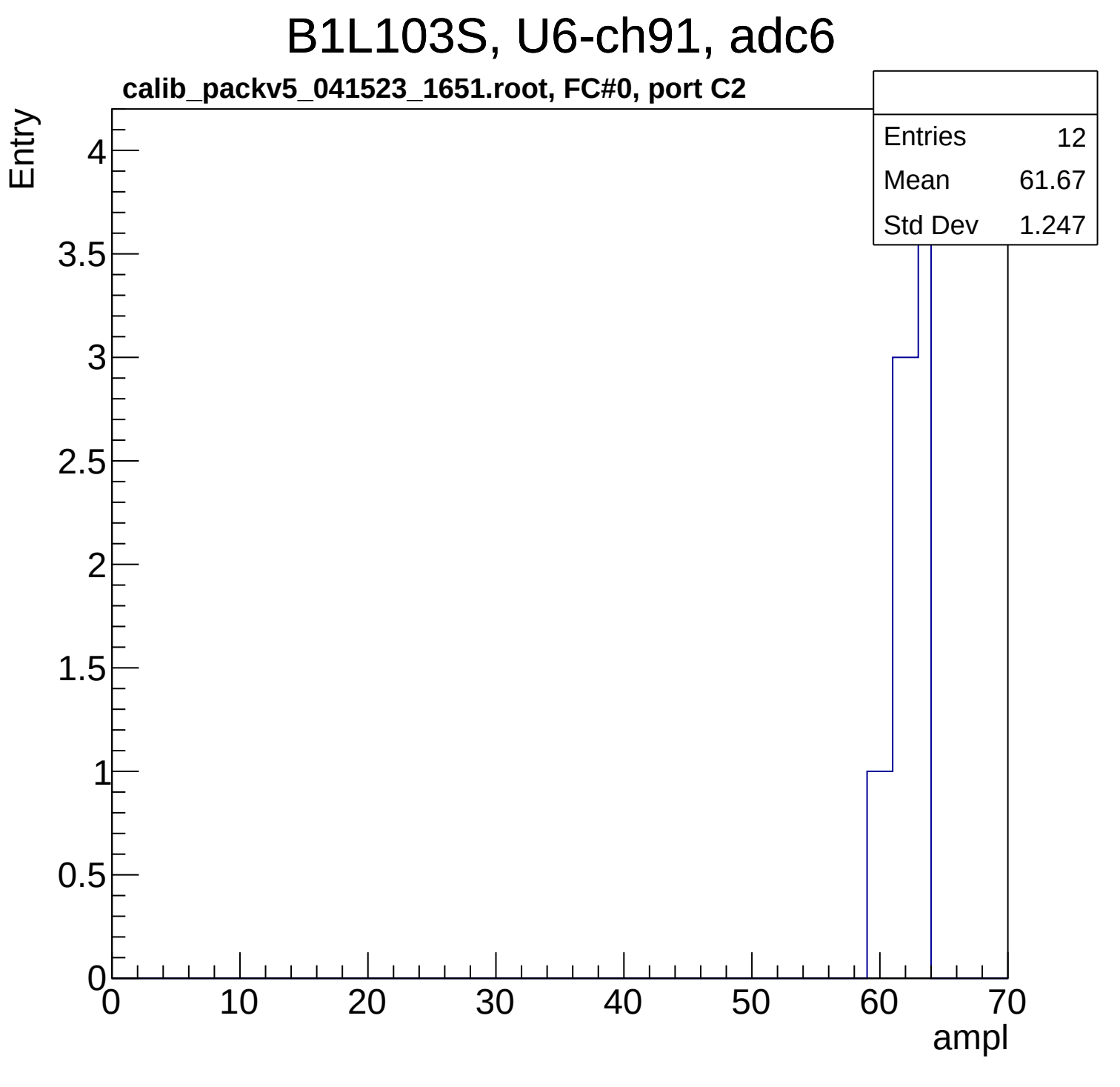
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch91, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.67
Std Dev 1.247
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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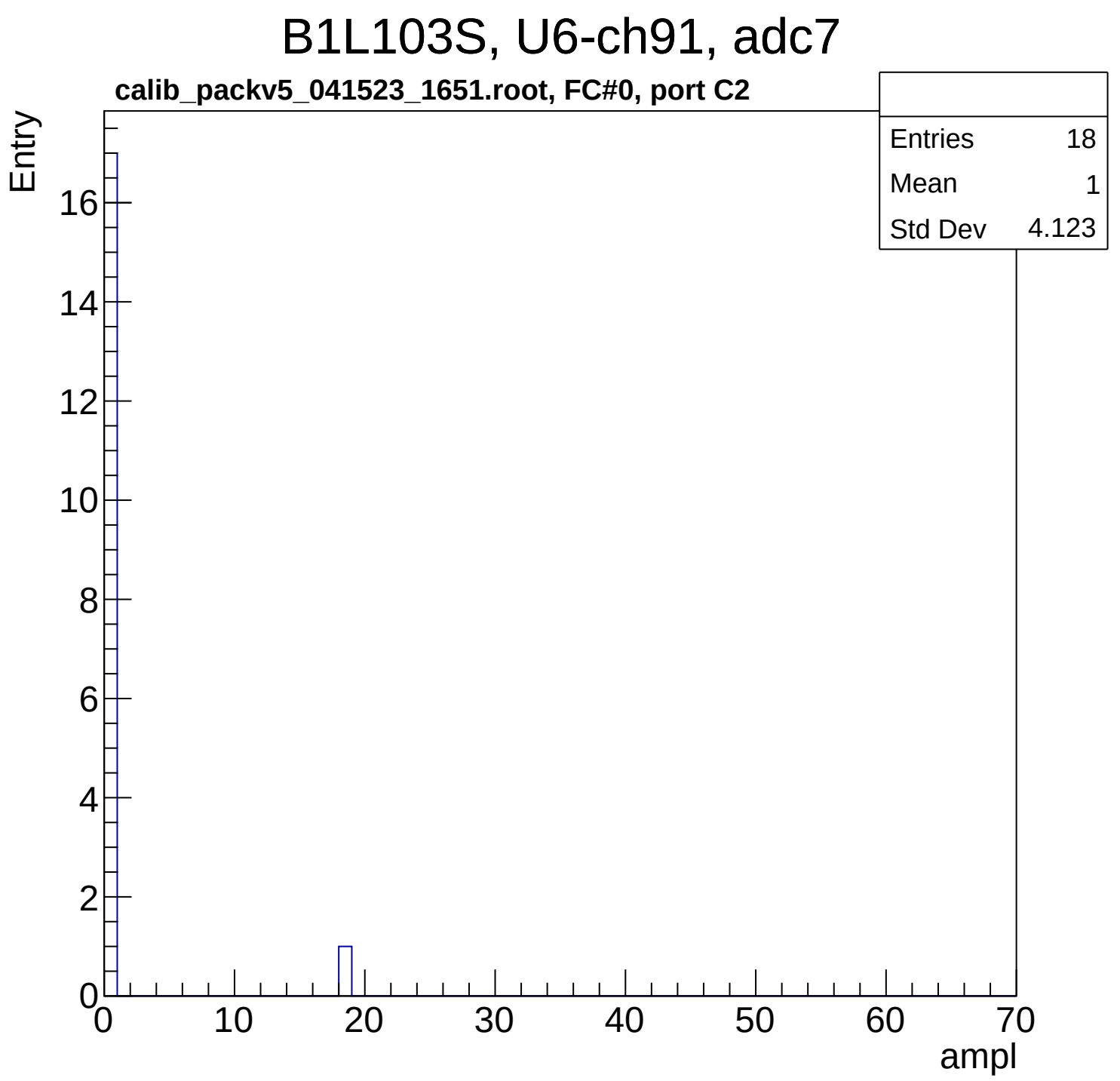
40
50
60
70


B1L103S, U6-ch91, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1
Std Dev 4.123
Entry
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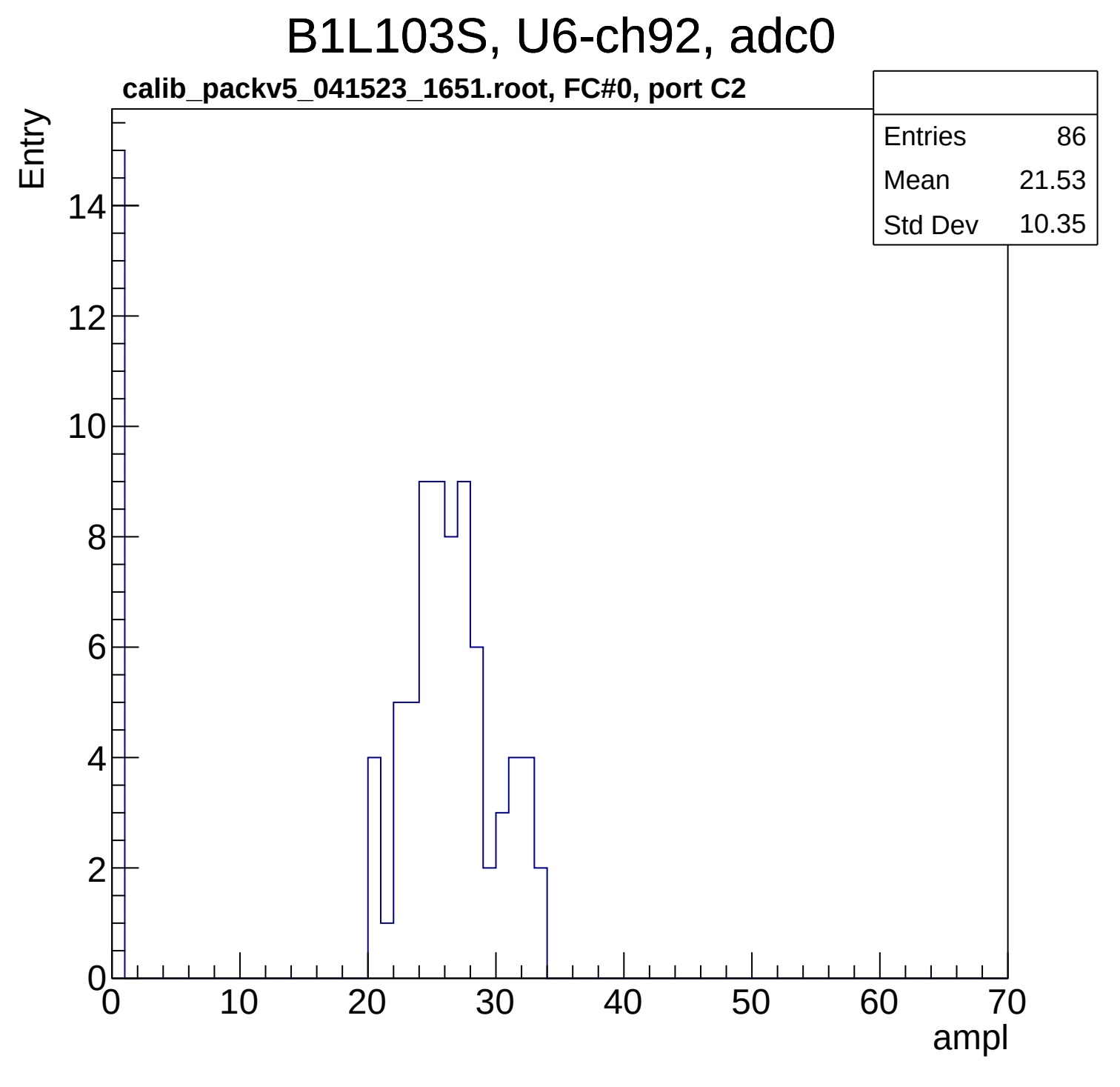
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch92, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 21.53
Std Dev 10.35
Entry
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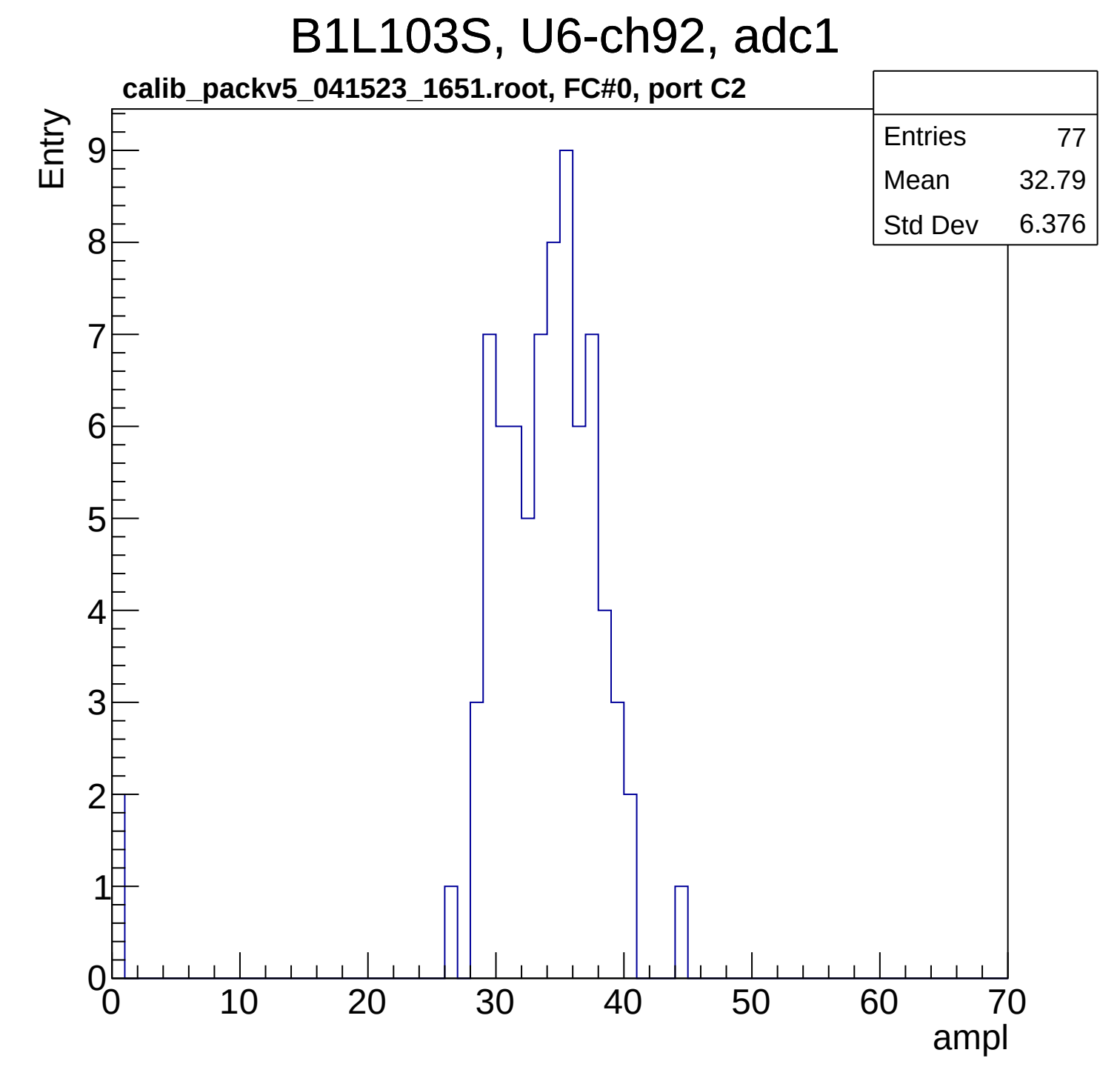
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch92, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 32.79
Std Dev 6.376
Entry
ampl
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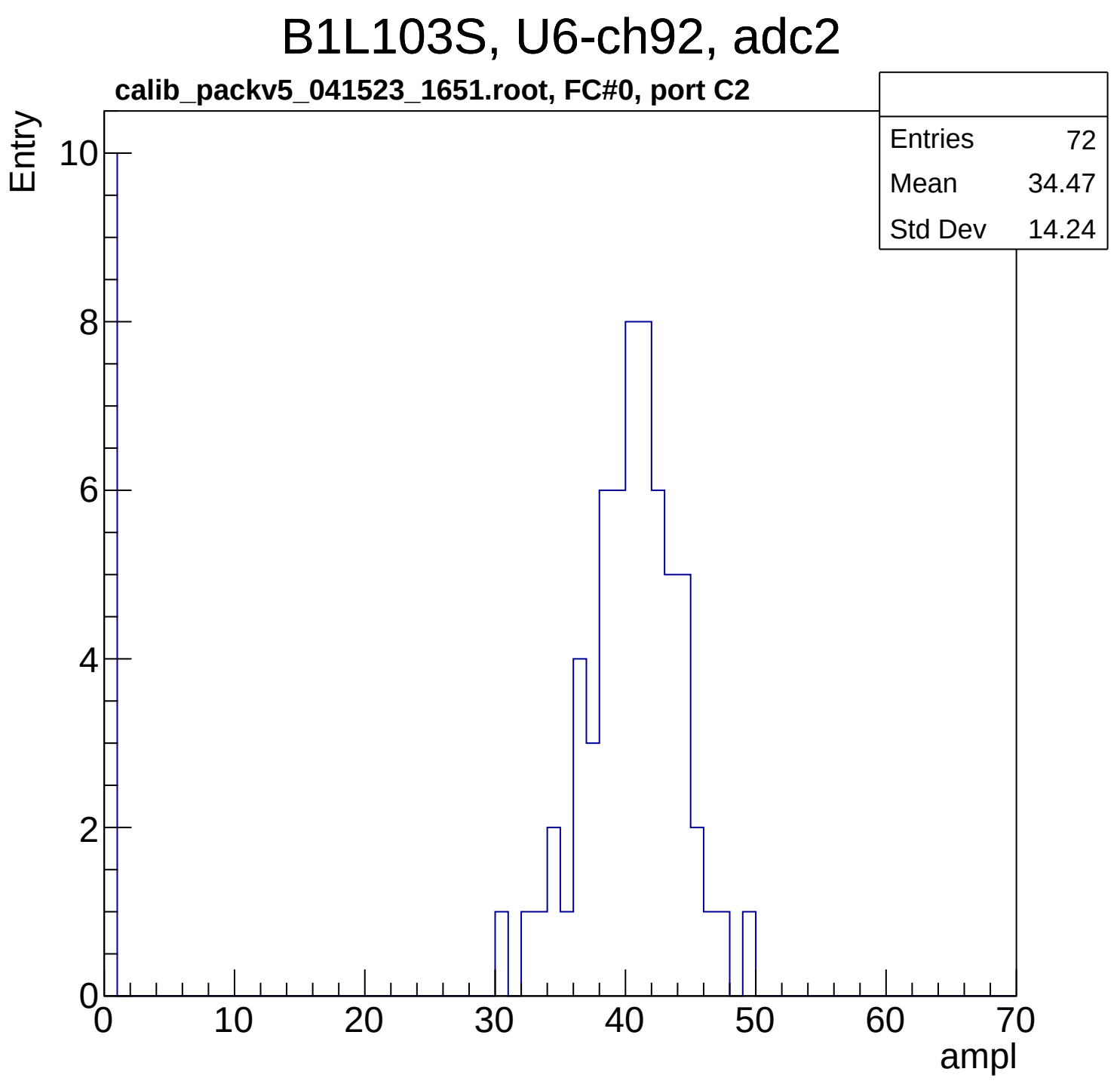
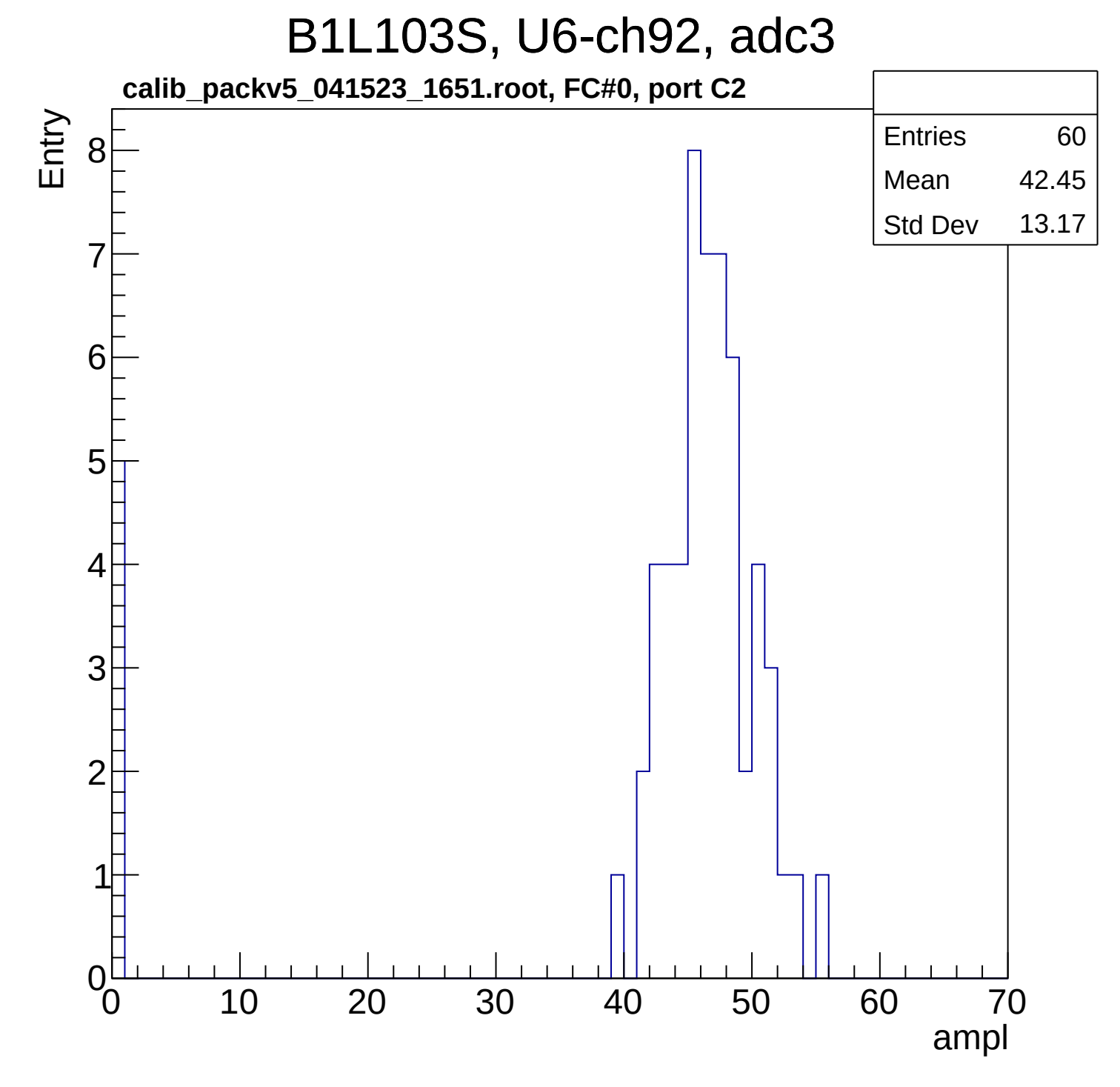
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch92, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 34.47
Std Dev 14.24
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch92, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 42.45
Std Dev 13.17
Entry
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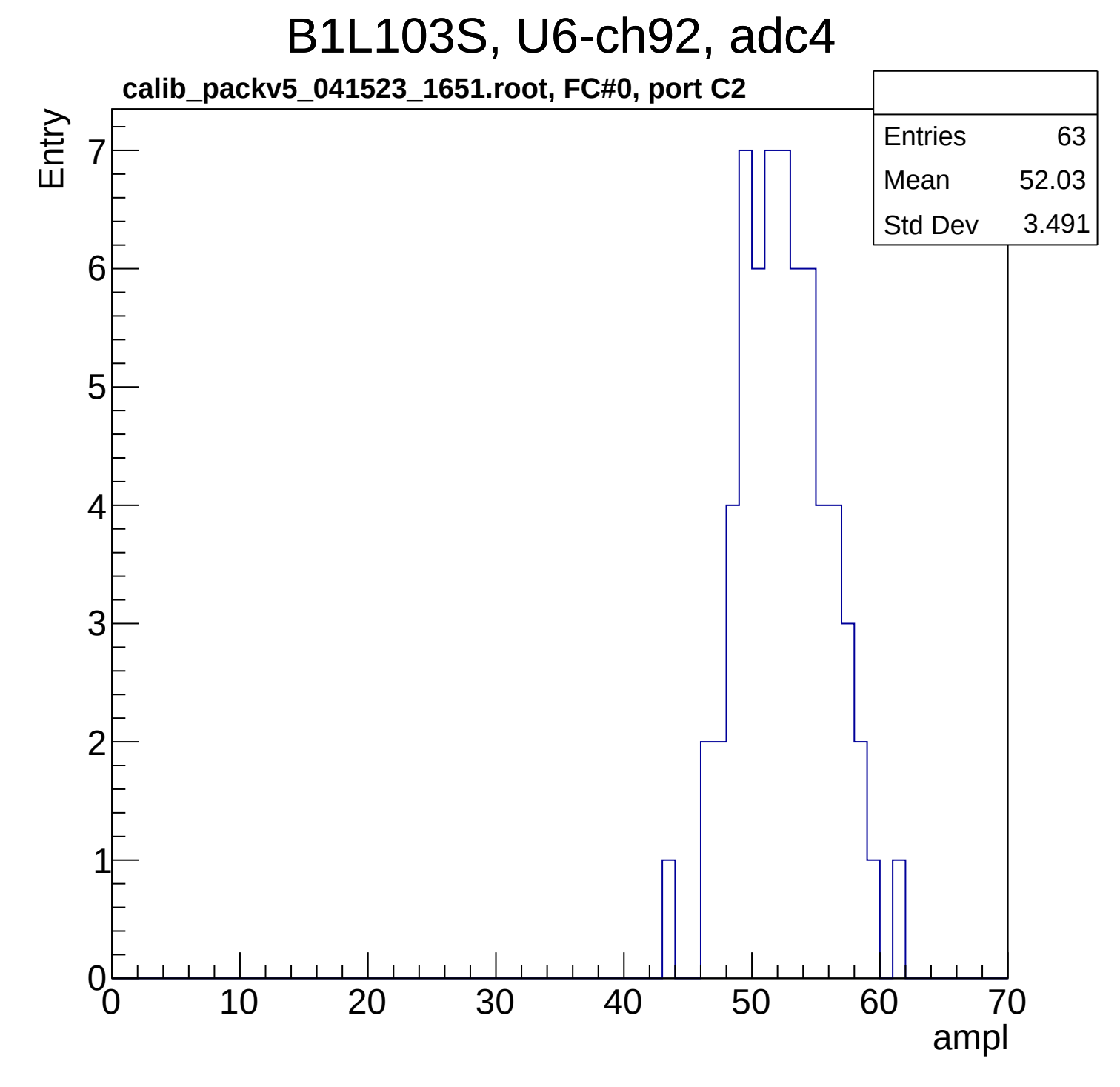
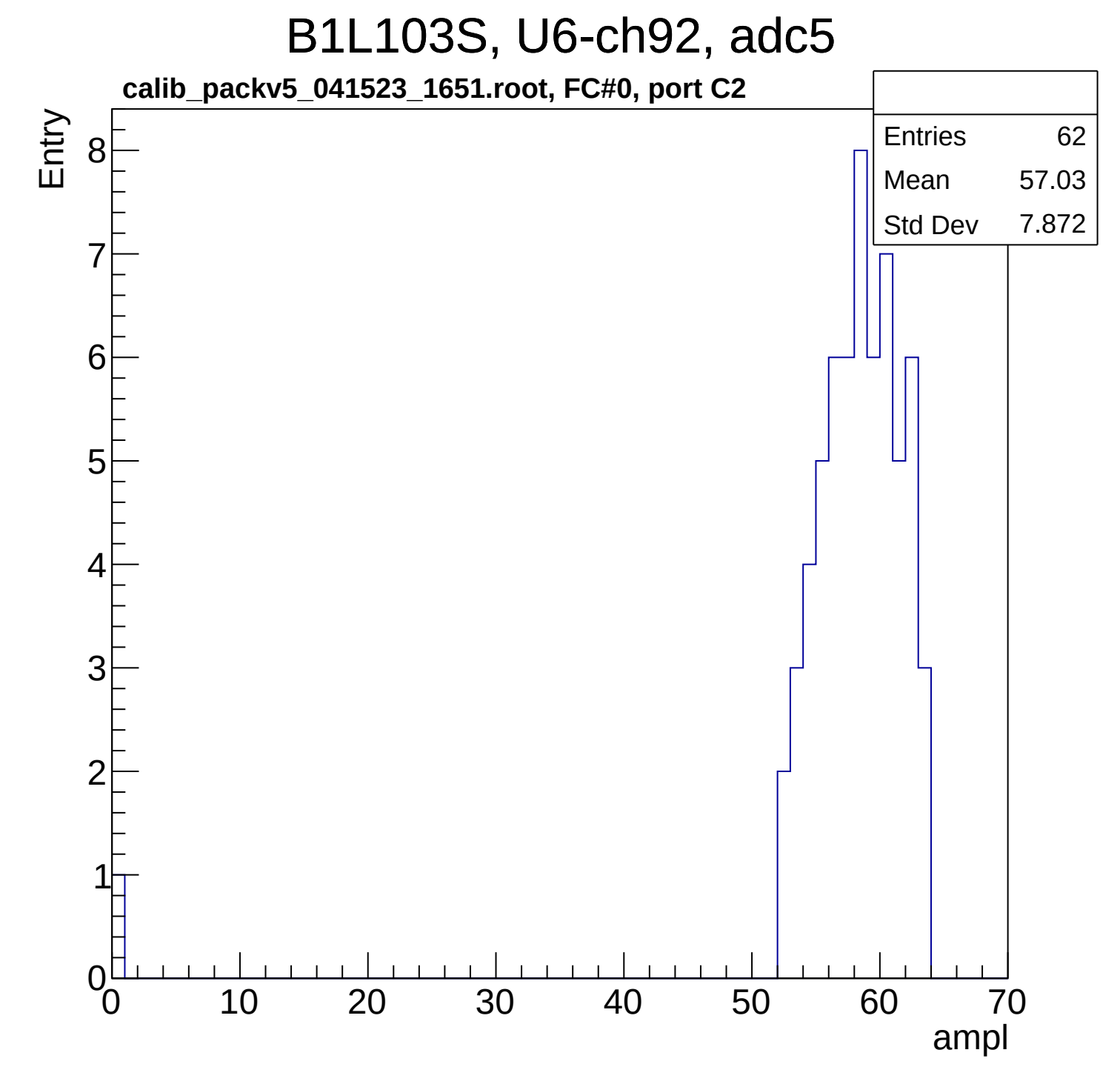
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch92, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 52.03
Std Dev 3.491
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U6-ch92, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 57.03
Std Dev 7.872
Entry
ampl
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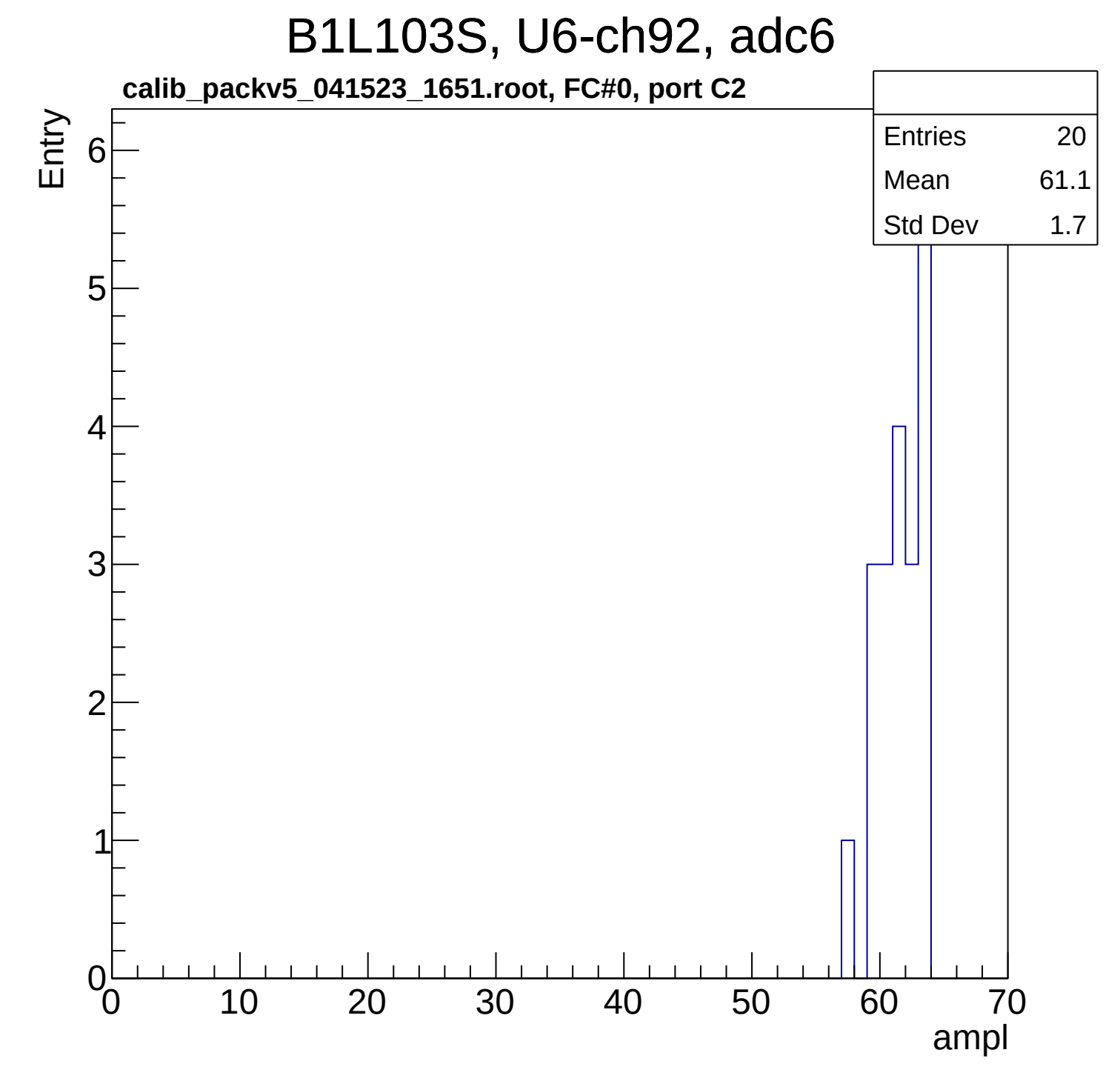
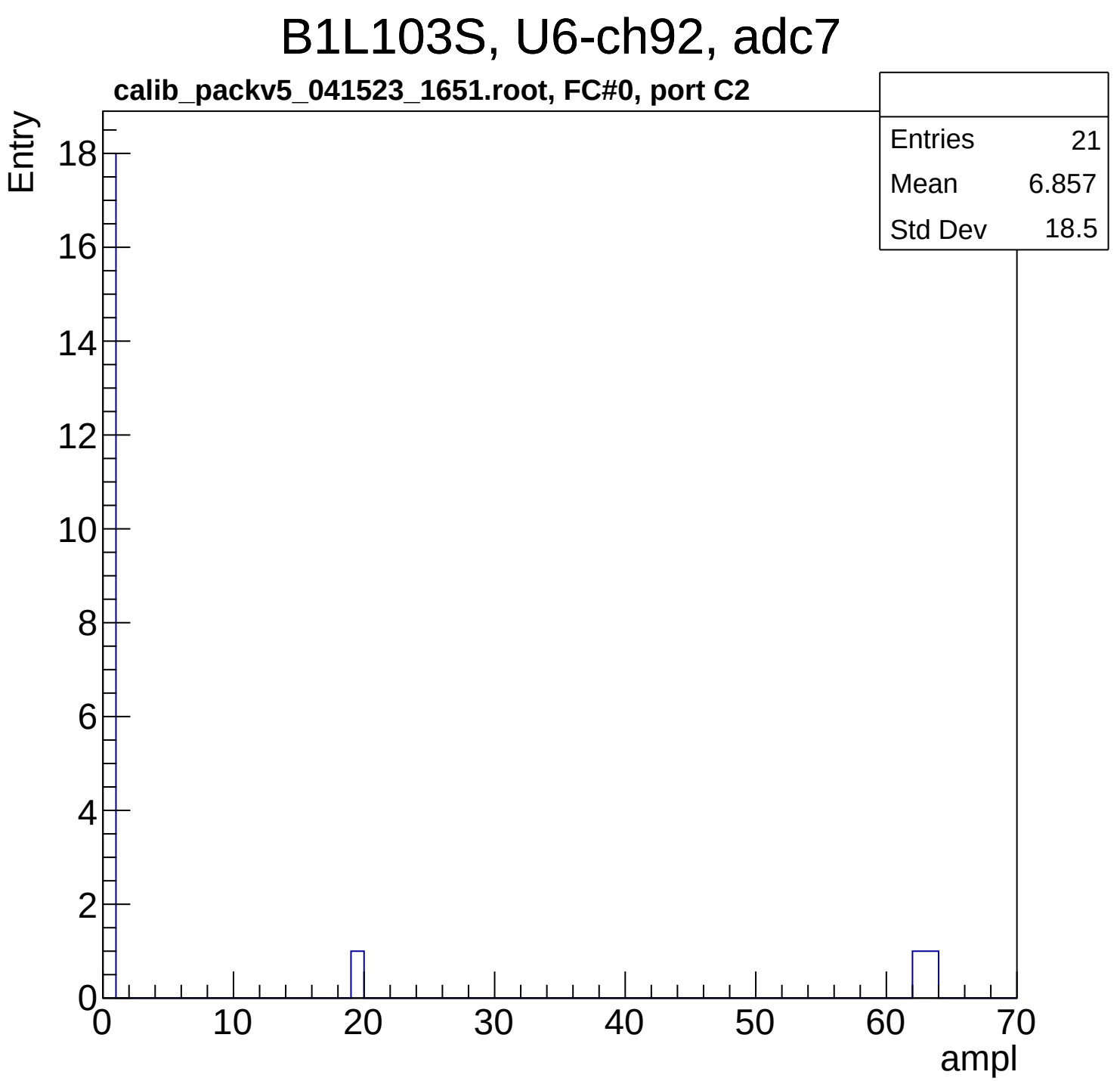
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch92, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 61.1
Std Dev 1.7
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U6-ch92, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 6.857
Std Dev 18.5
Entry
0
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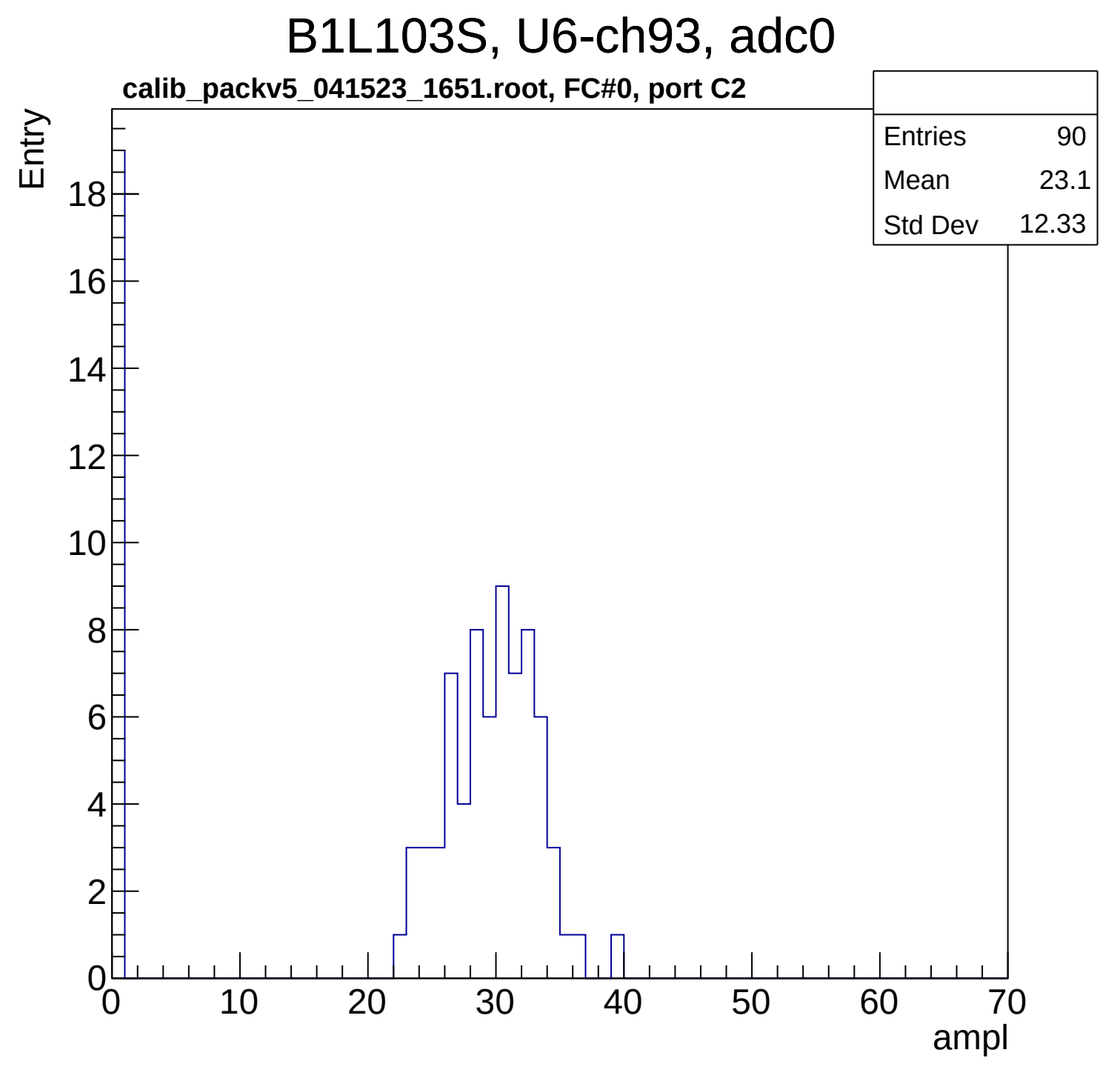
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch93, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 23.1
Std Dev 12.33
Entry
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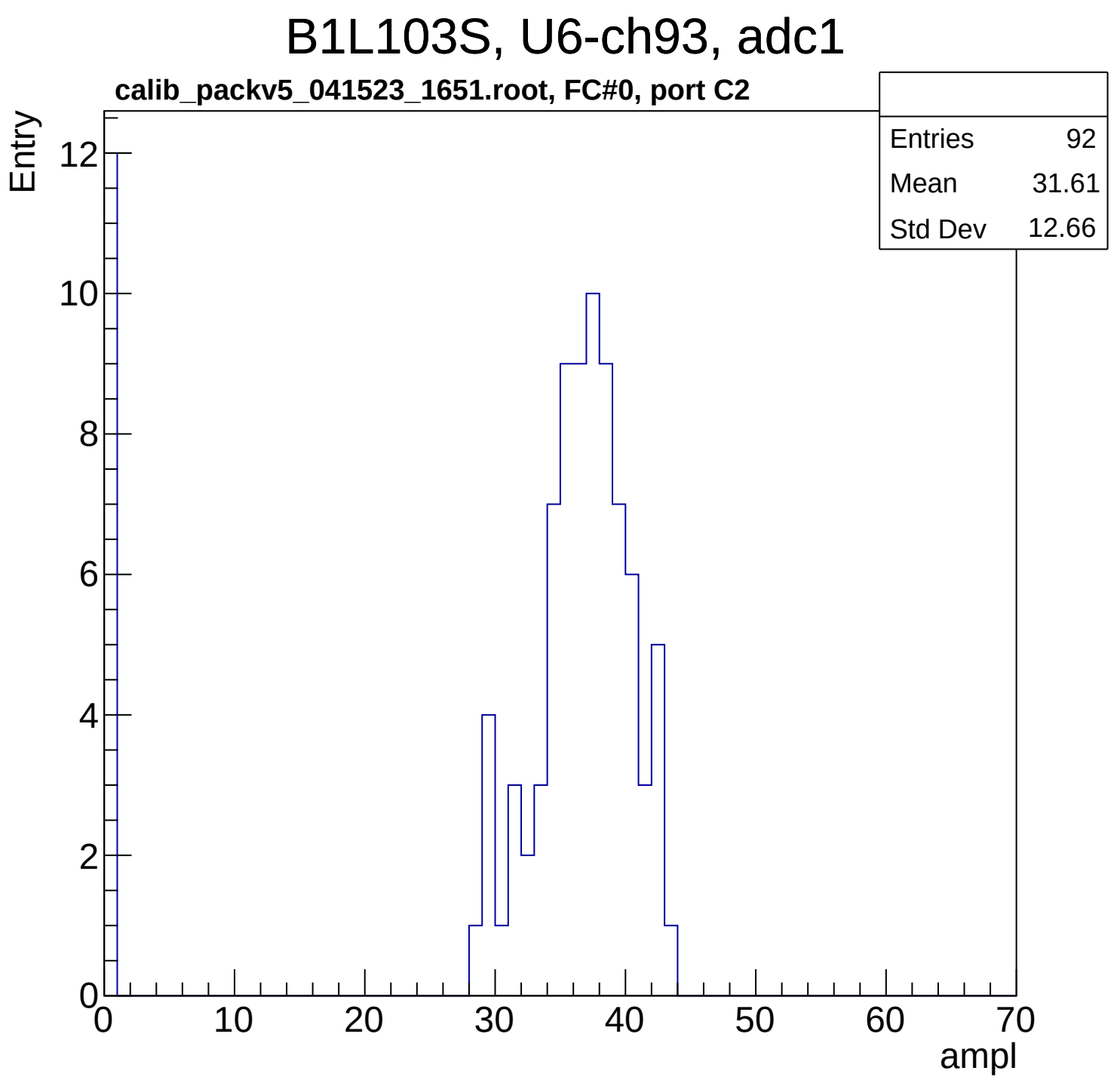
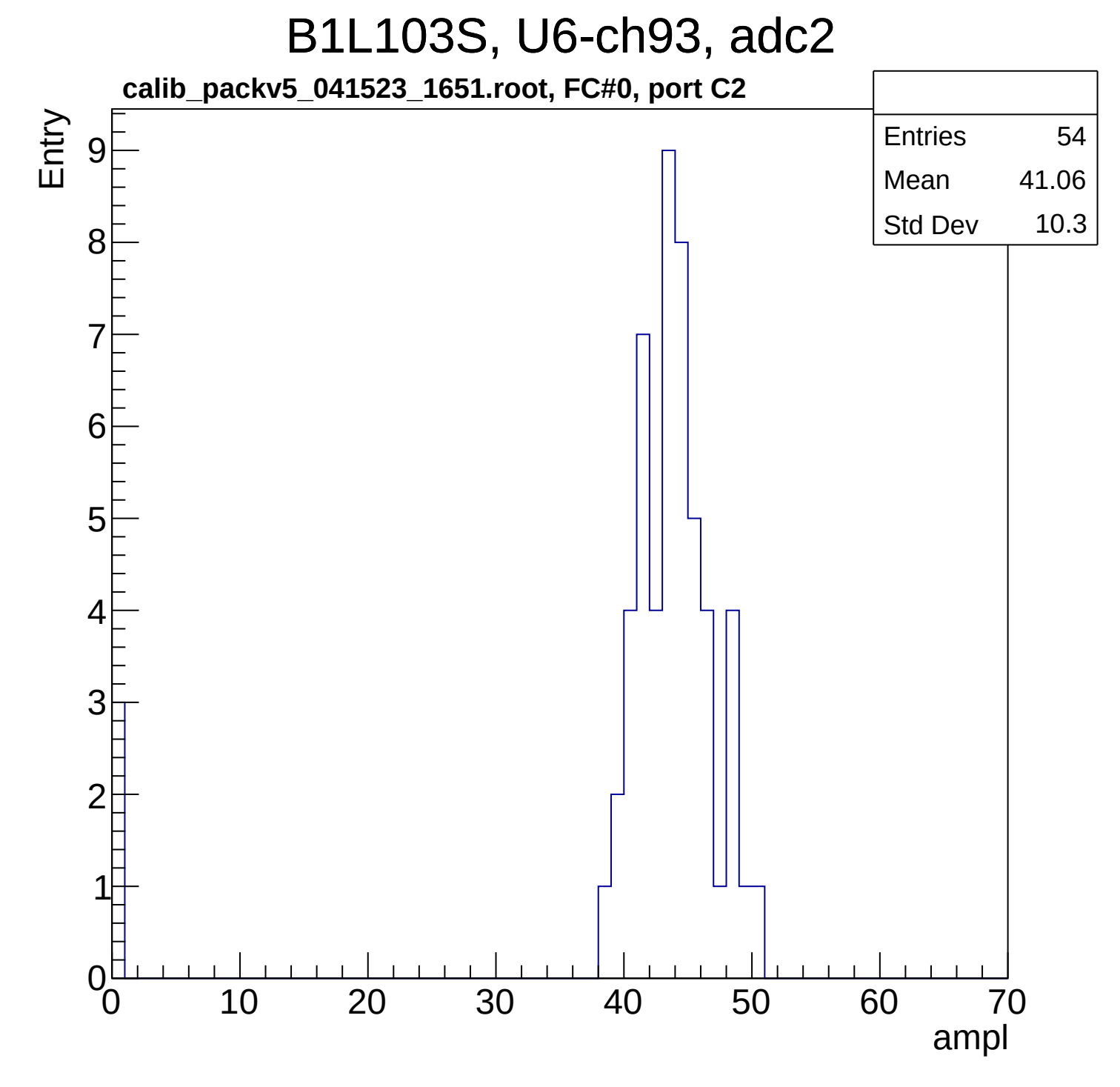
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch93, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 31.61
Std Dev 12.66
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch93, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 41.06
Std Dev 10.3
Entry
ampl
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3
4
5
6
7
8
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0
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60
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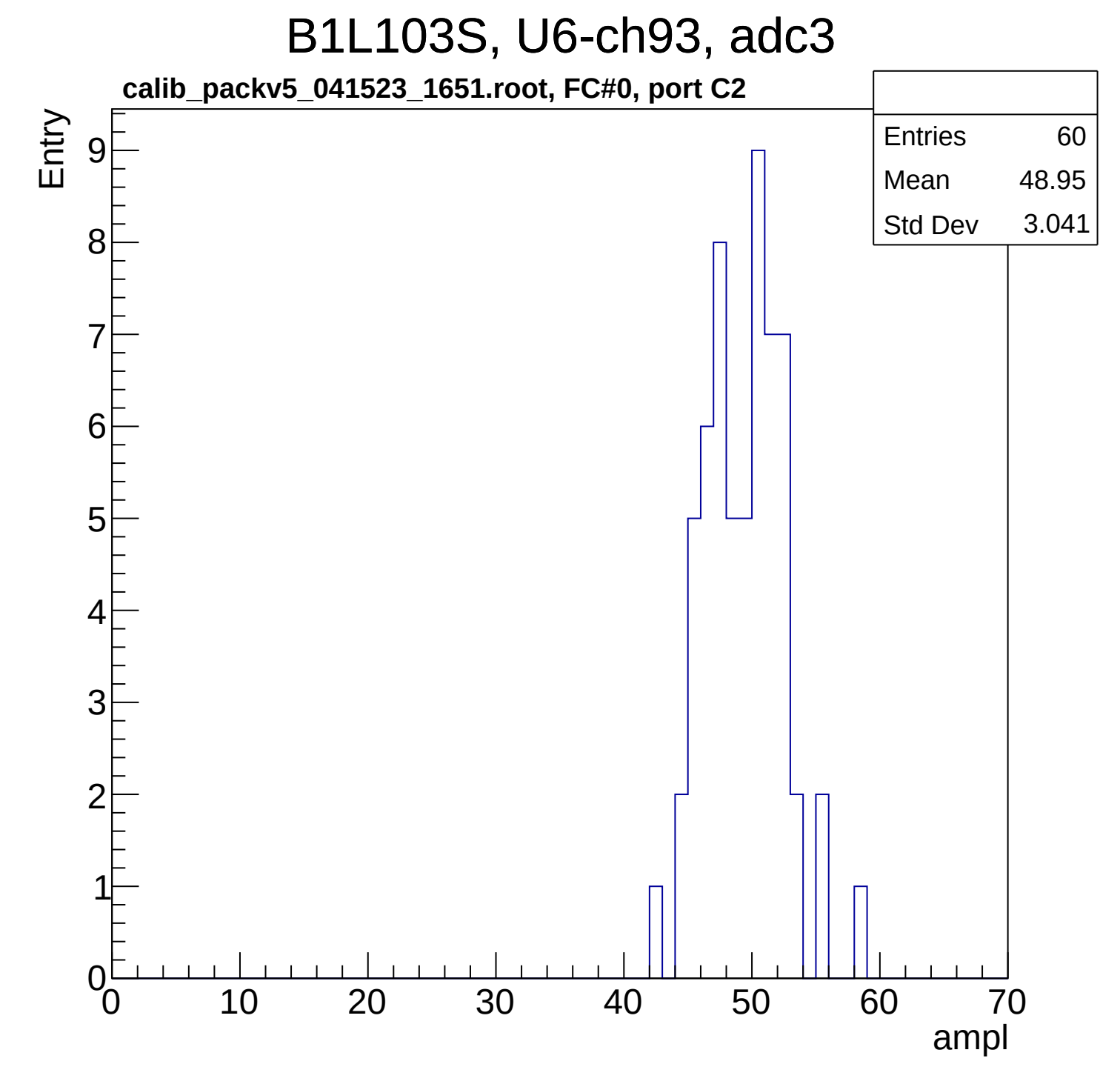
B1L103S, U6-ch93, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 48.95
Std Dev 3.041
Entry
ampl
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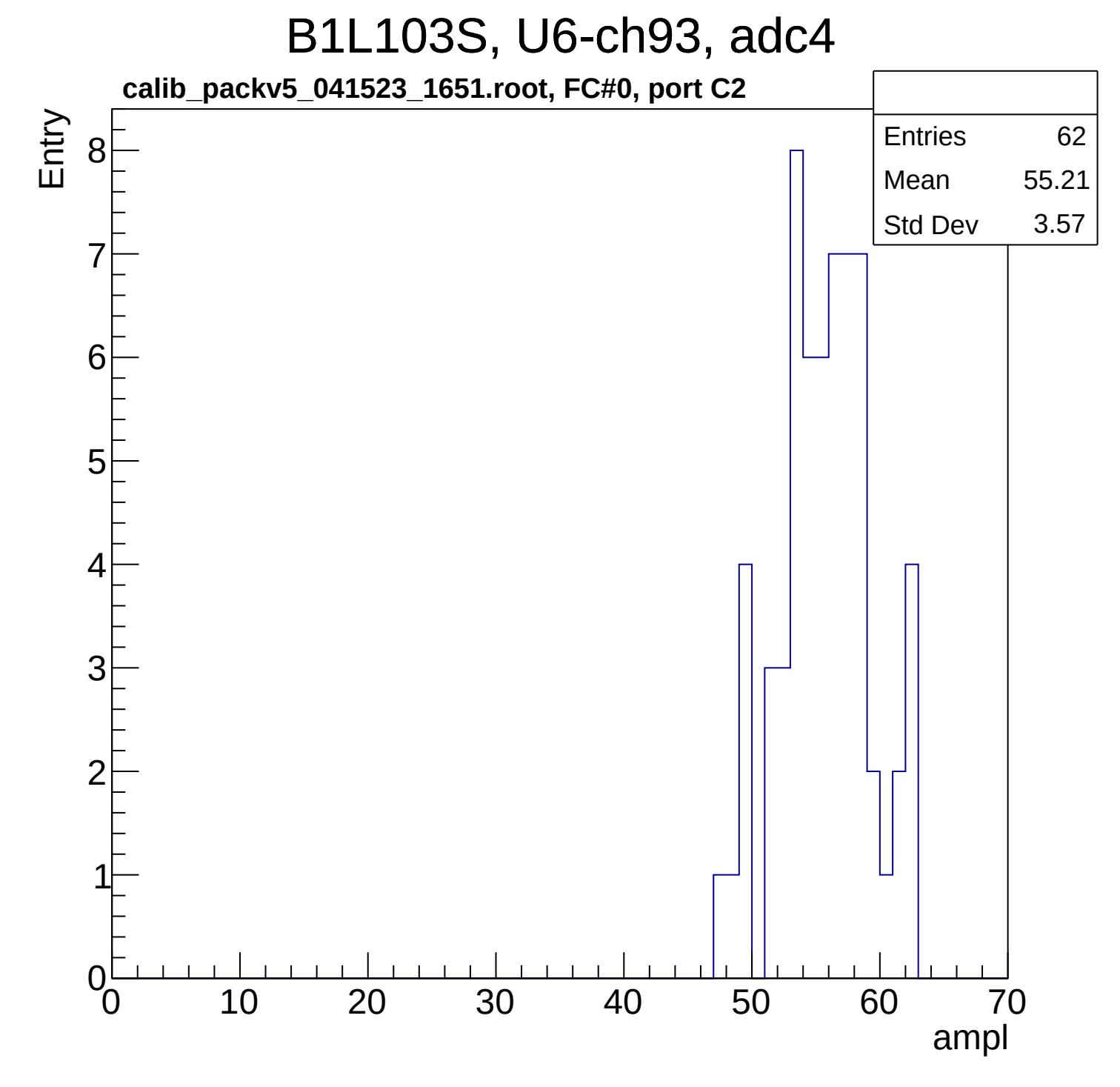
B1L103S, U6-ch93, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 55.21
Std Dev 3.57
Entry
ampl
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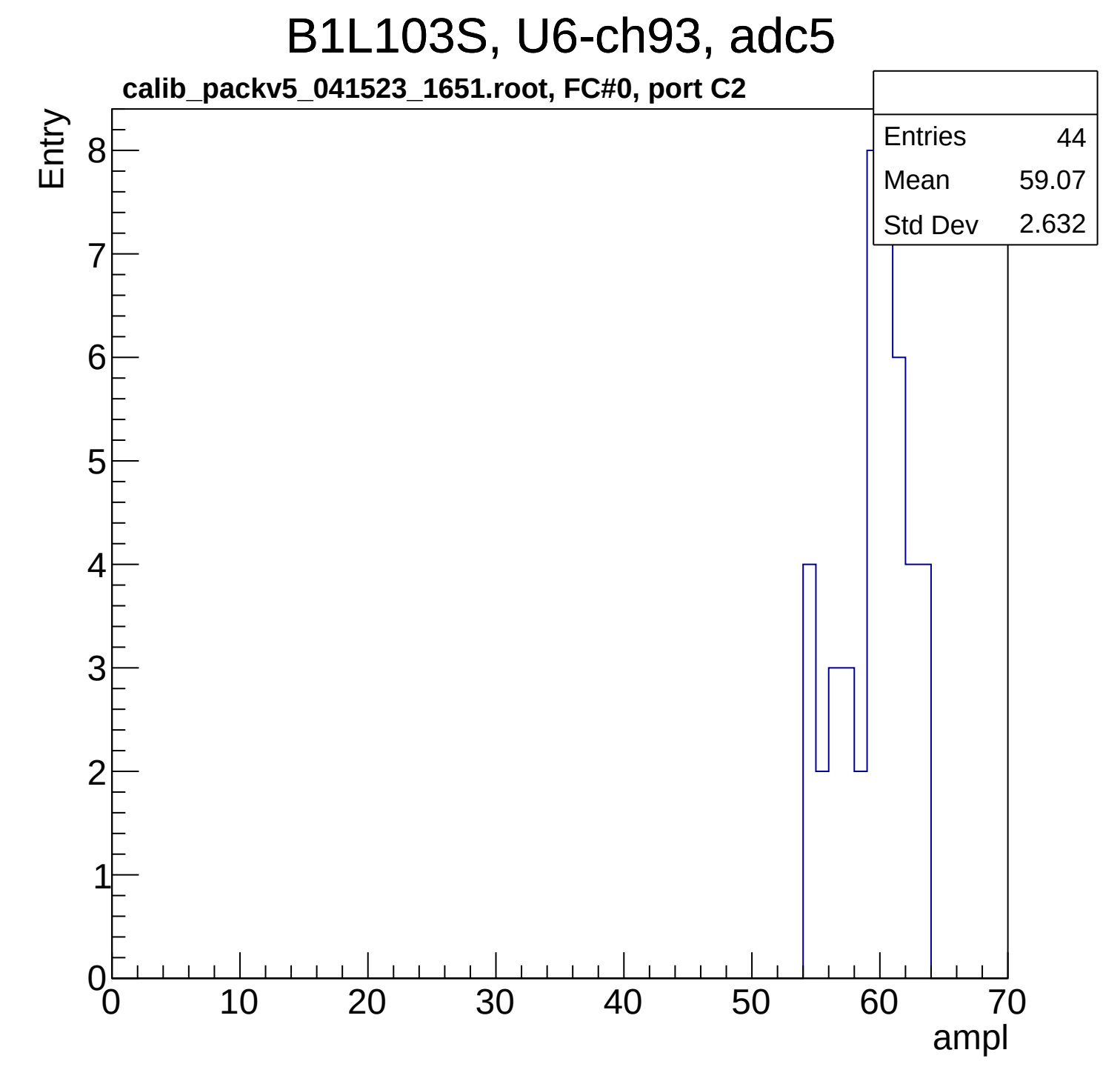
B1L103S, U6-ch93, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 59.07
Std Dev 2.632
Entry
ampl
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2
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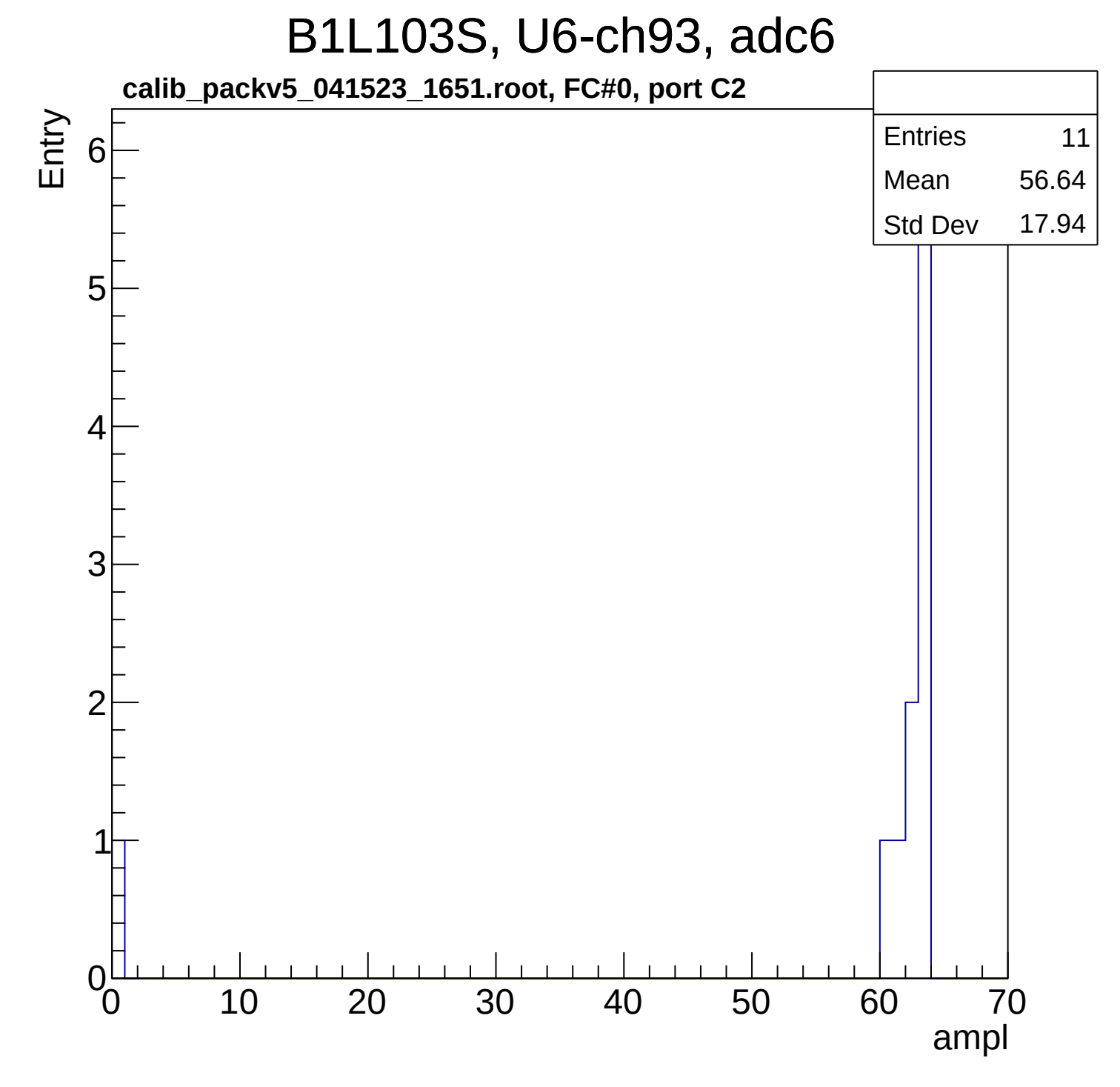
B1L103S, U6-ch93, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 56.64
Std Dev 17.94
Entry
0
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2
3
4
5
6
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10
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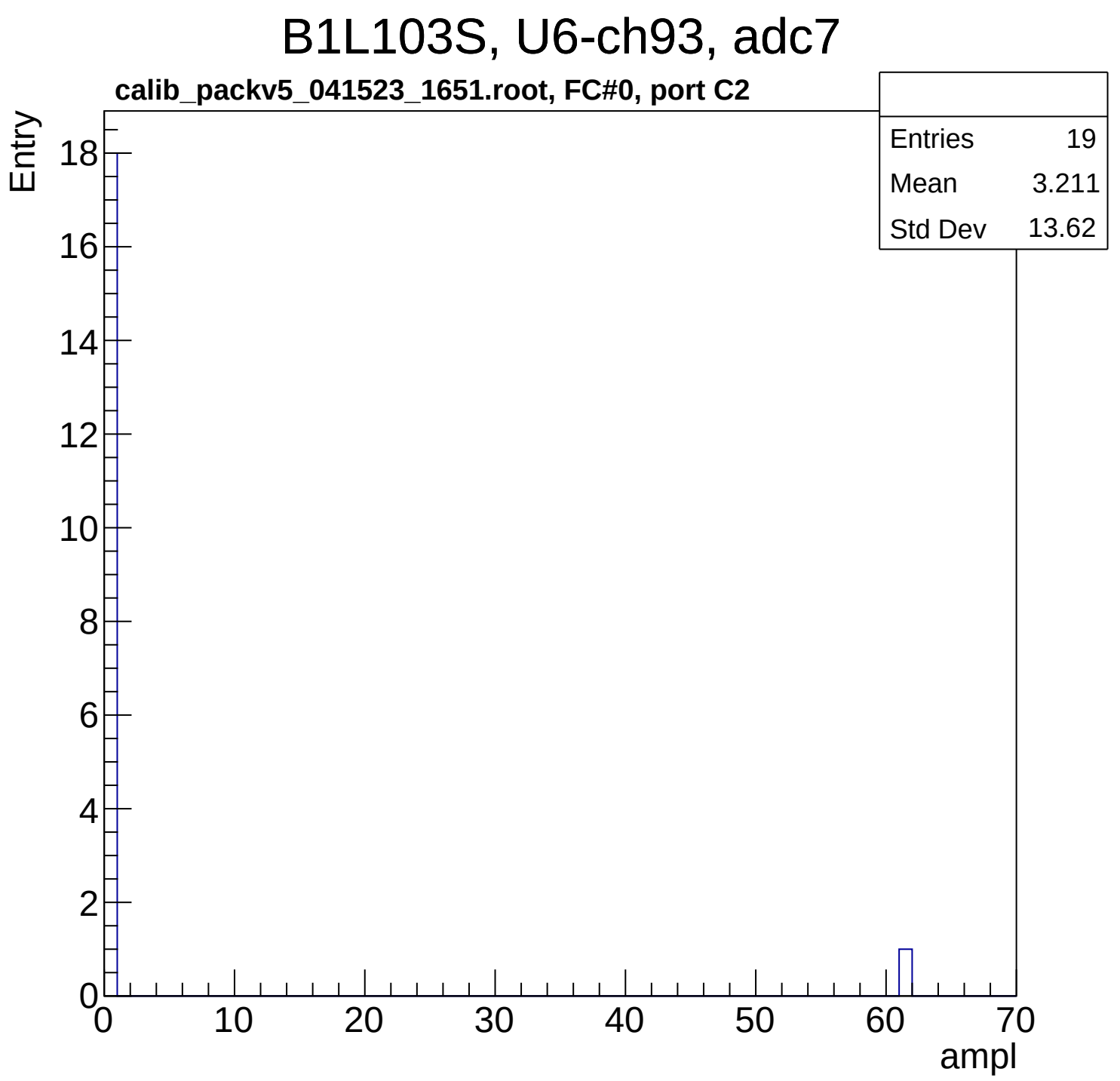
40
50
60
70
ampl


B1L103S, U6-ch93, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.211
Std Dev 13.62
Entry
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6
8
10
12
14
16
18
0
10
20
30
40
50
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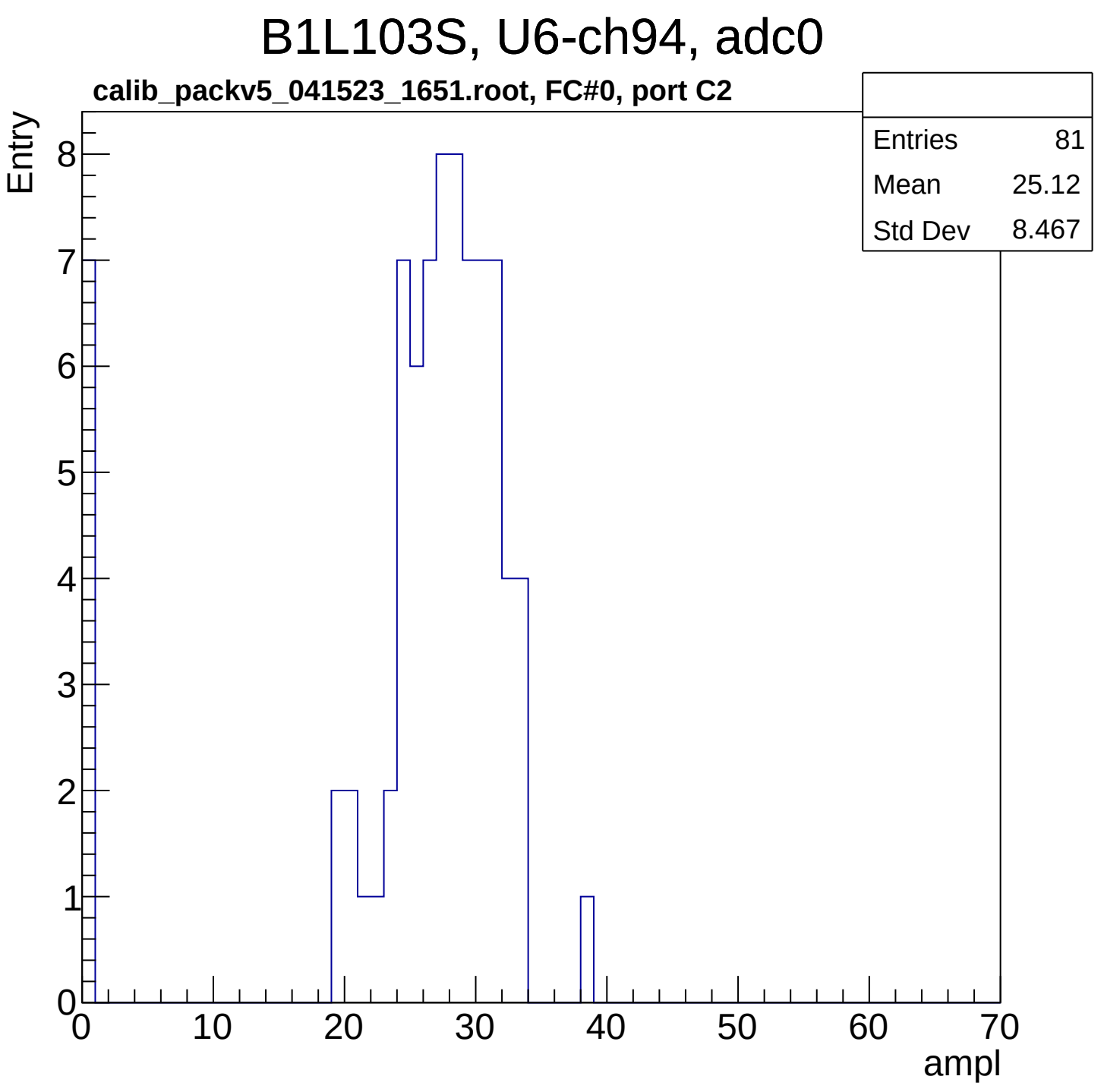
70
ampl


B1L103S, U6-ch94, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 25.12
Std Dev 8.467
Entry
ampl
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1
2
3
4
5
6
7
8
0
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40
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60
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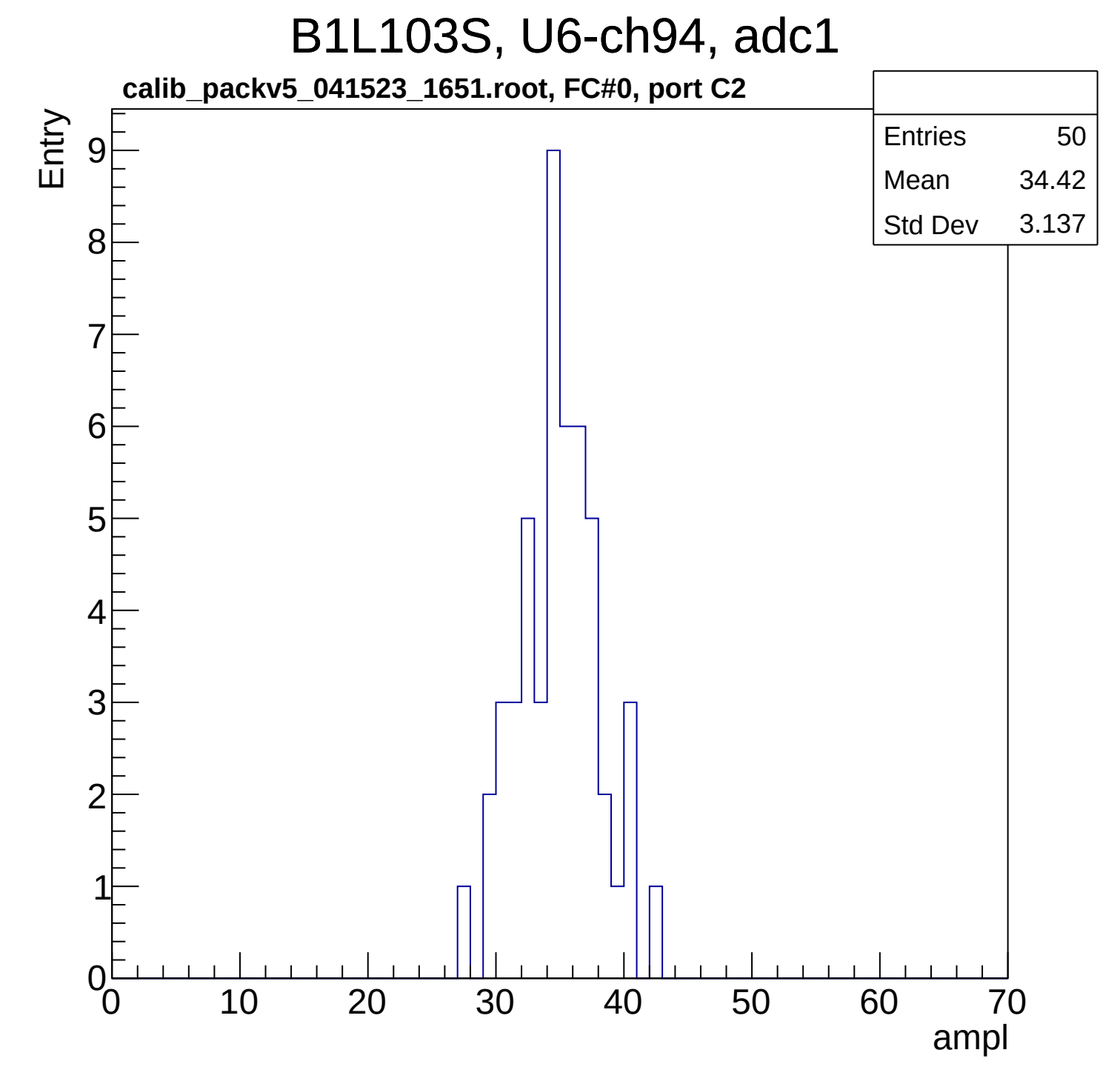
B1L103S, U6-ch94, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 34.42
Std Dev 3.137
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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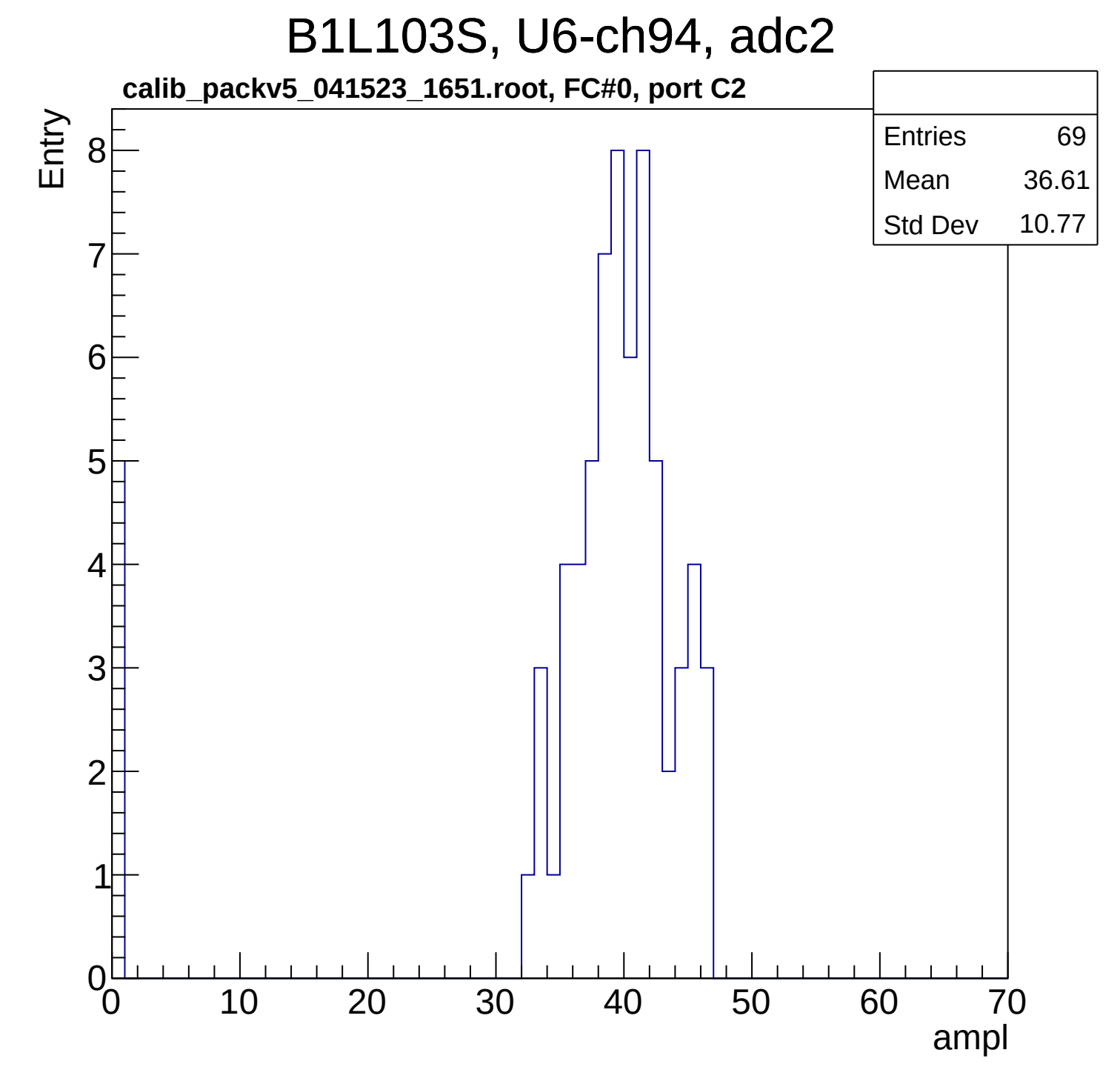
B1L103S, U6-ch94, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 36.61
Std Dev 10.77
Entry
ampl
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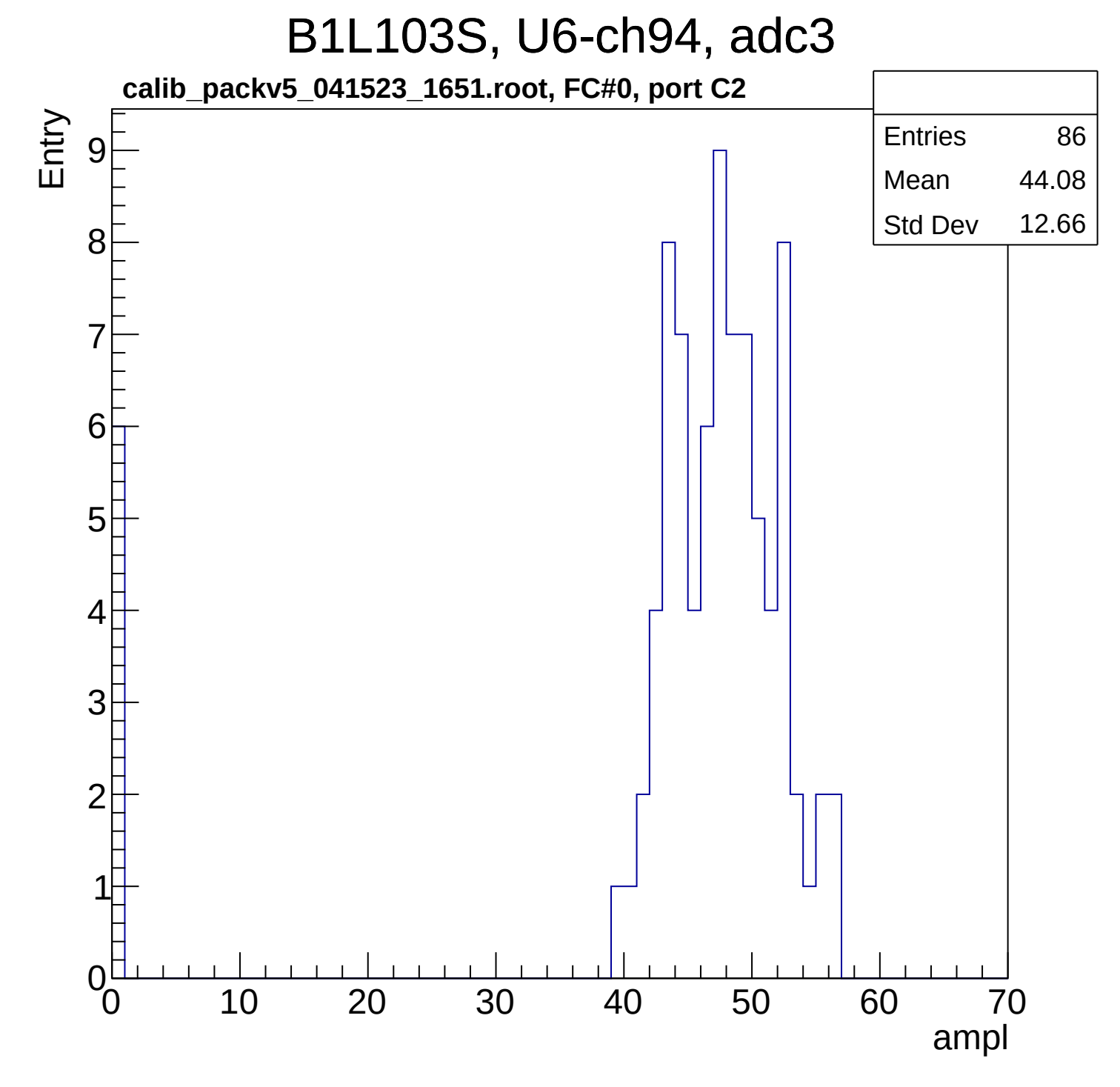
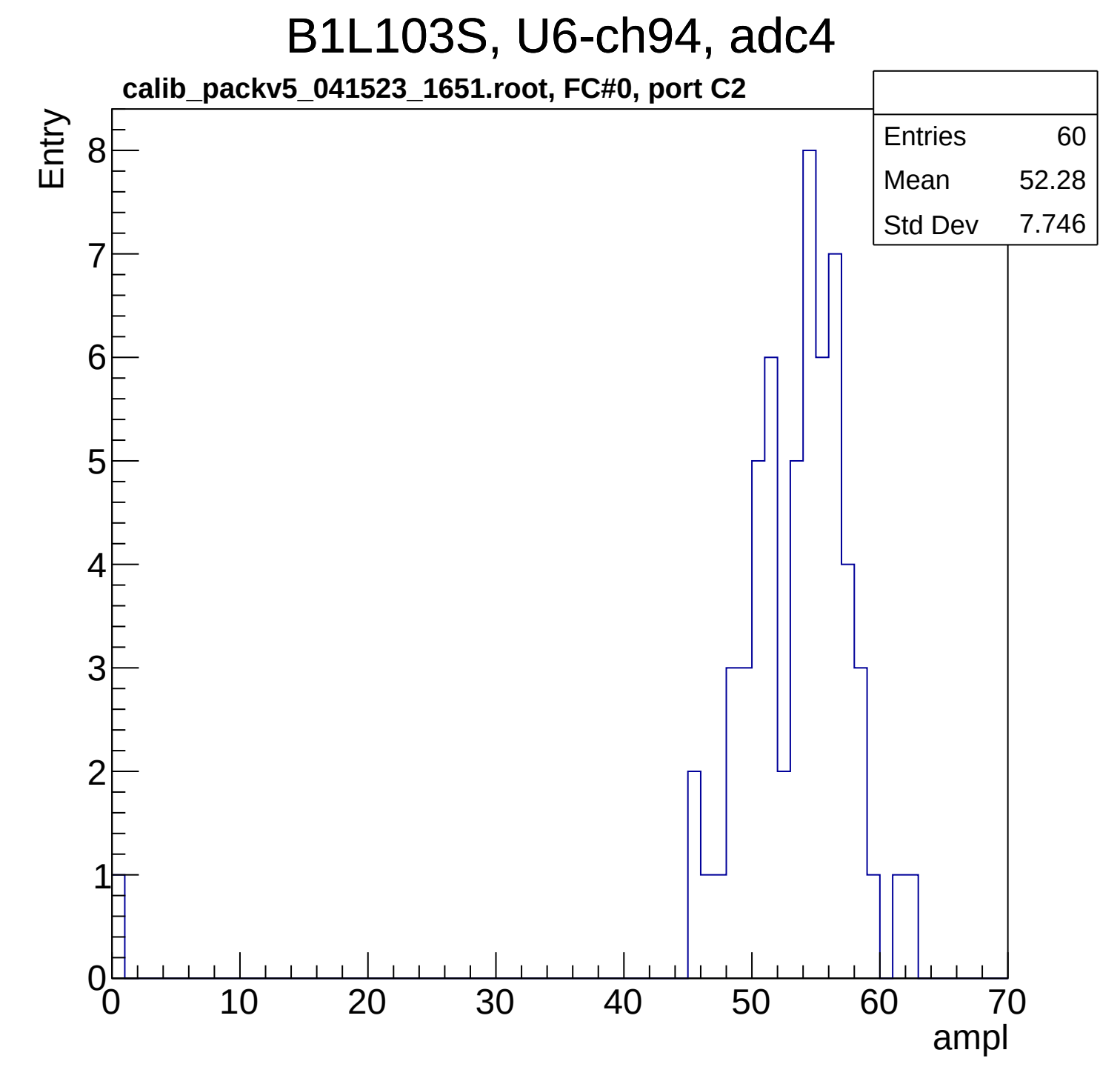
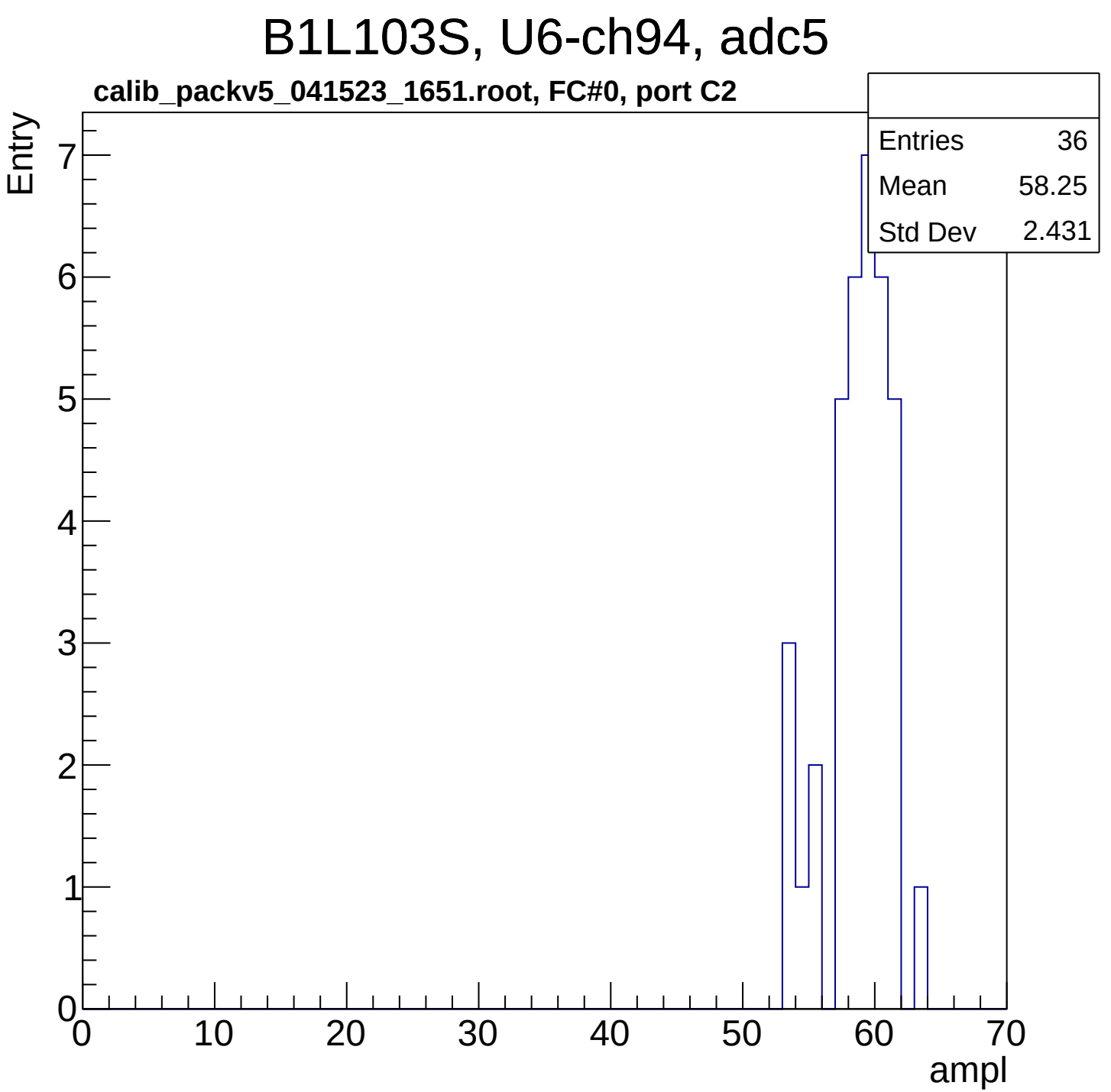
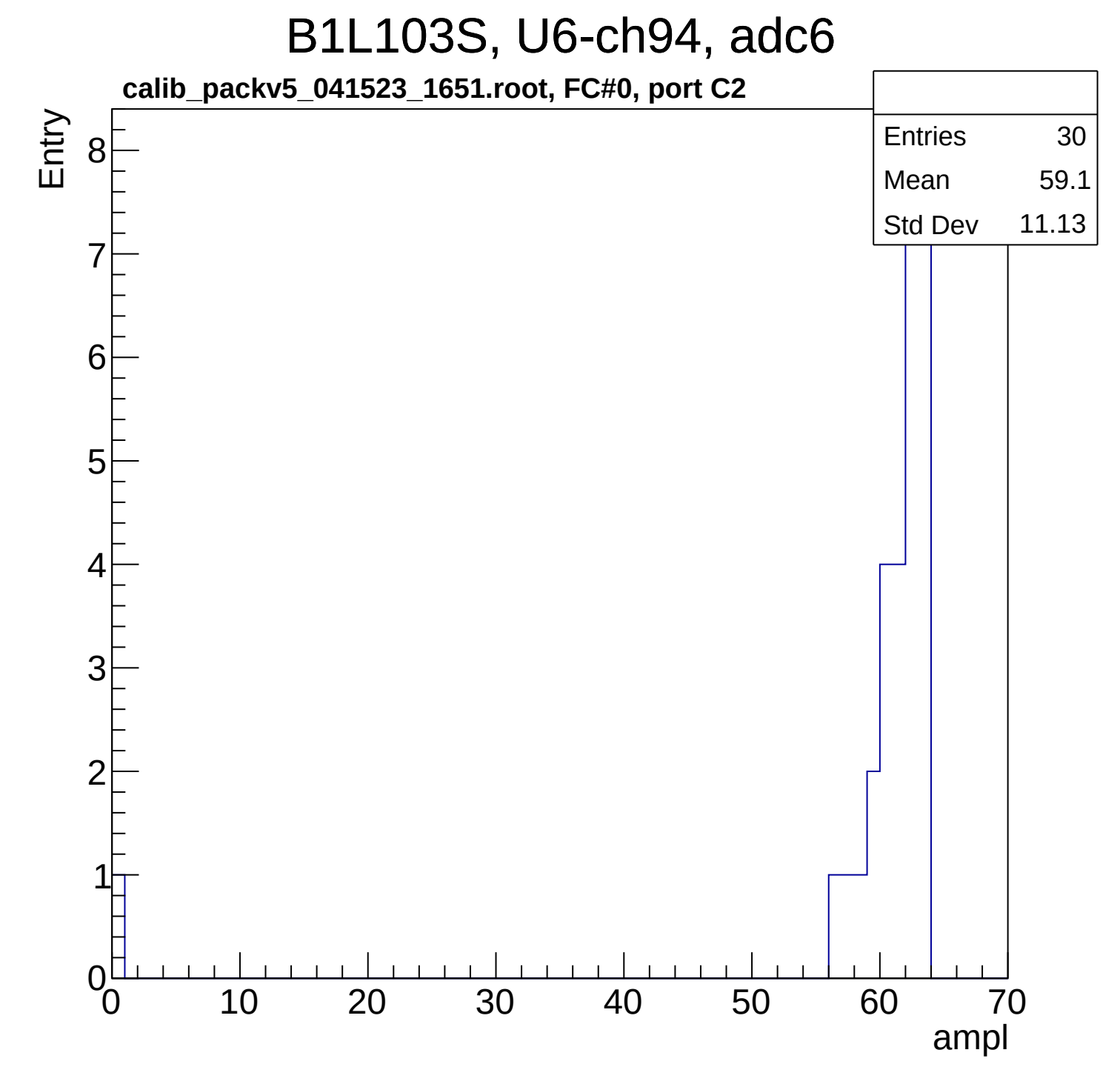
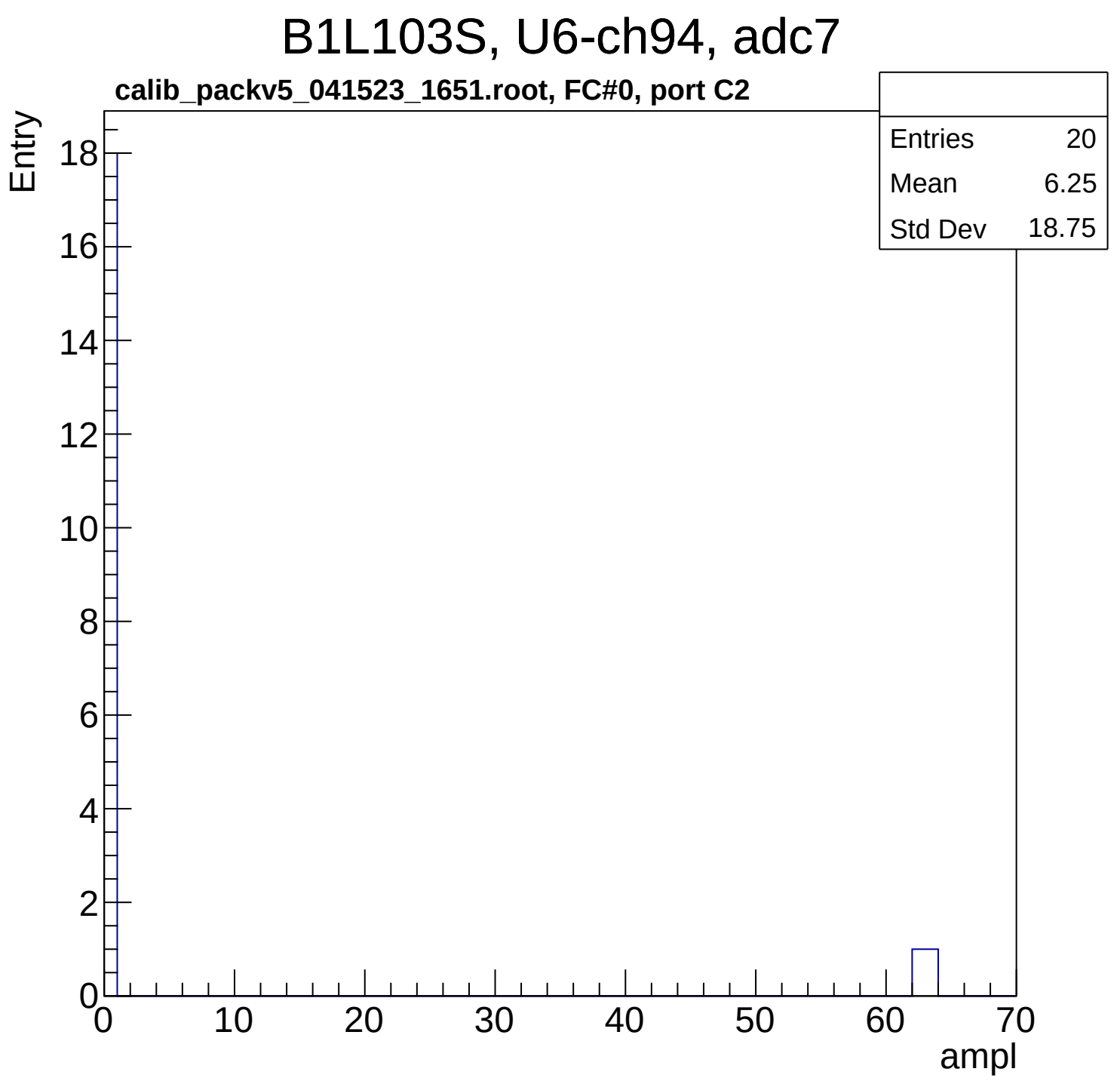
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

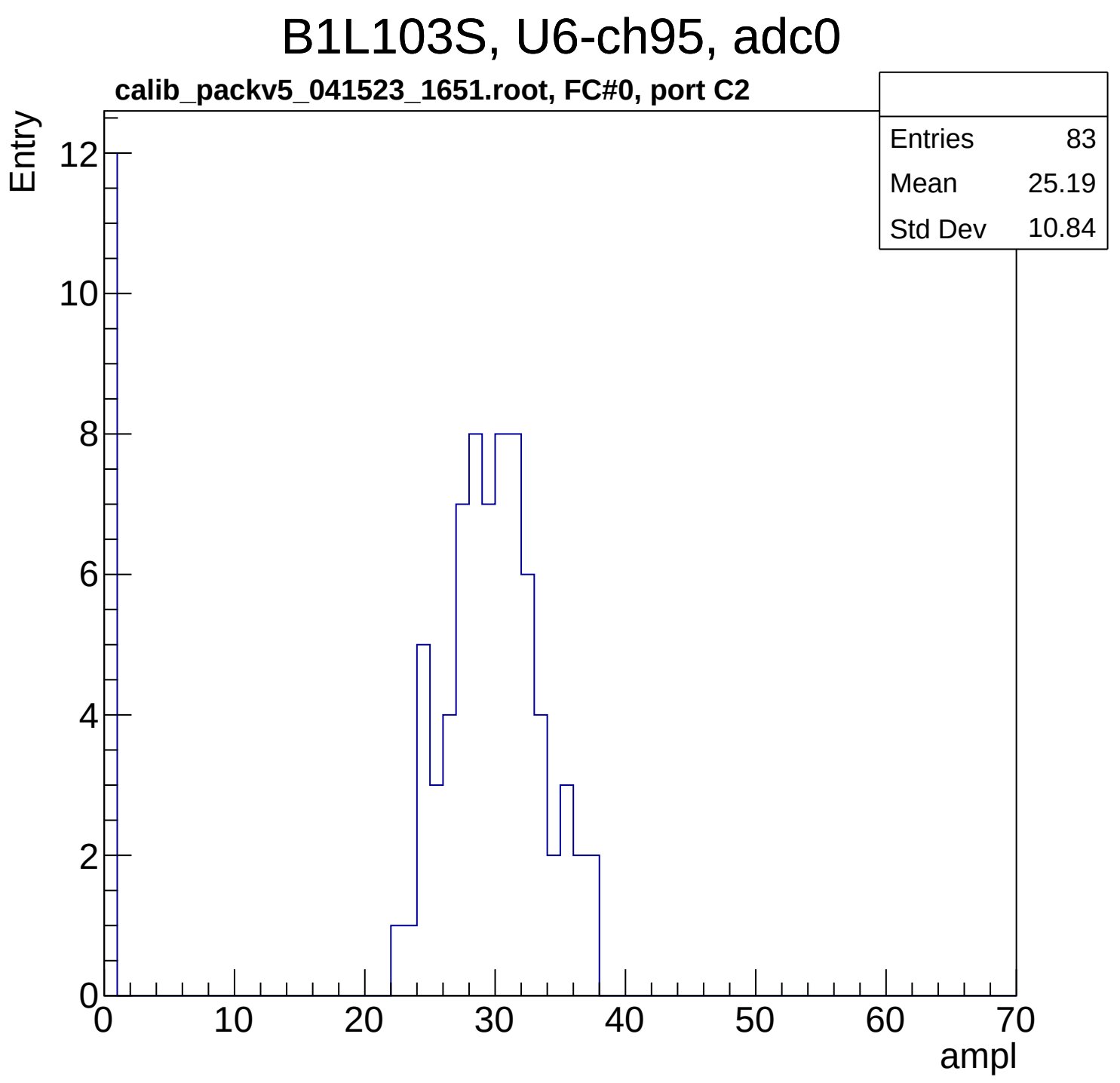

B1L103S, U6-ch94, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 44.08
Std Dev 12.66
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

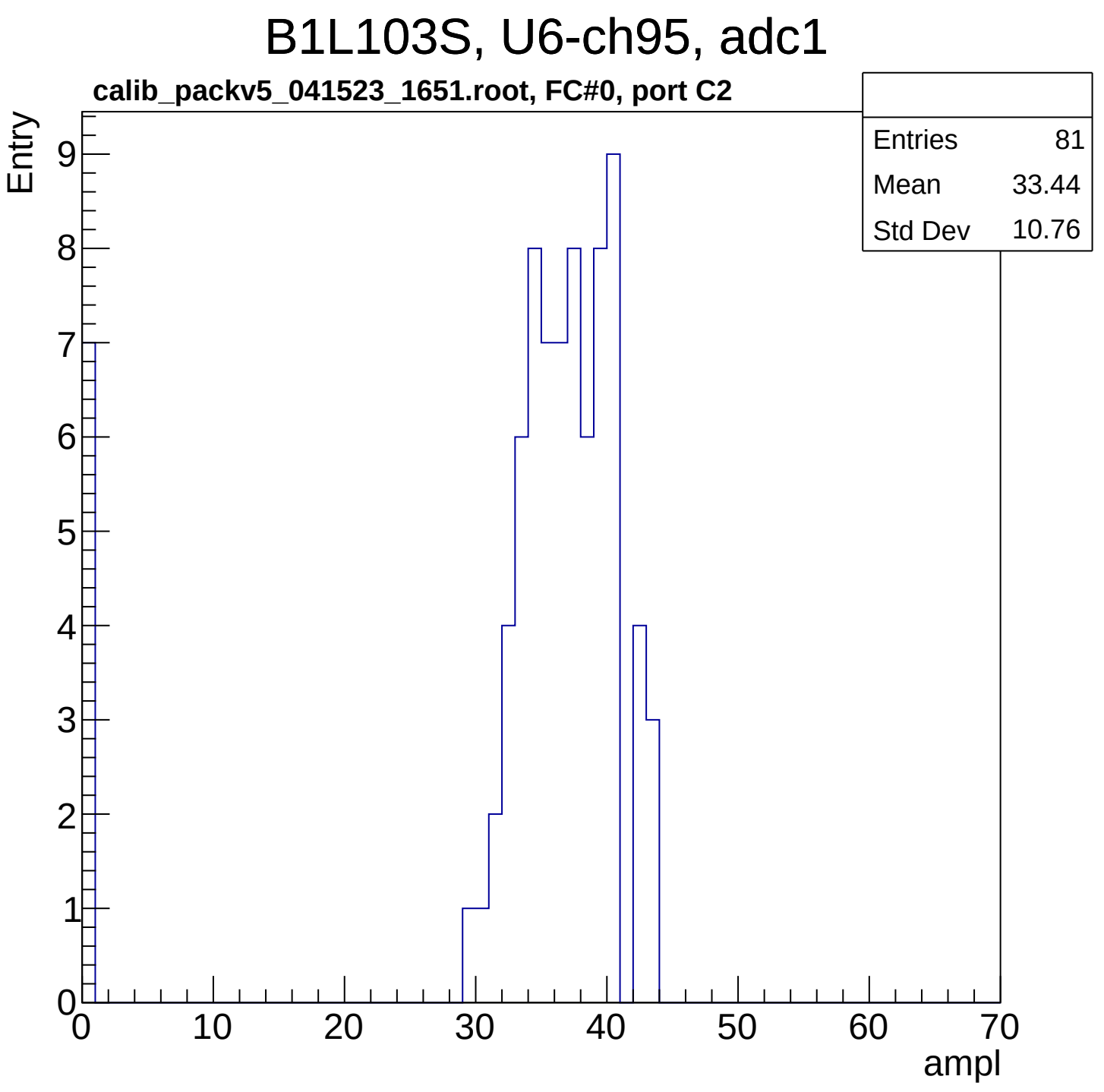

B1L103S, U6-ch94, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 52.28
Std Dev 7.746
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch94, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 58.25
Std Dev 2.431
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U6-ch94, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 59.1
Std Dev 11.13
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch94, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 6.25
Std Dev 18.75
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch95, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 25.19
Std Dev 10.84
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch95, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 33.44
Std Dev 10.76
Entry
ampl
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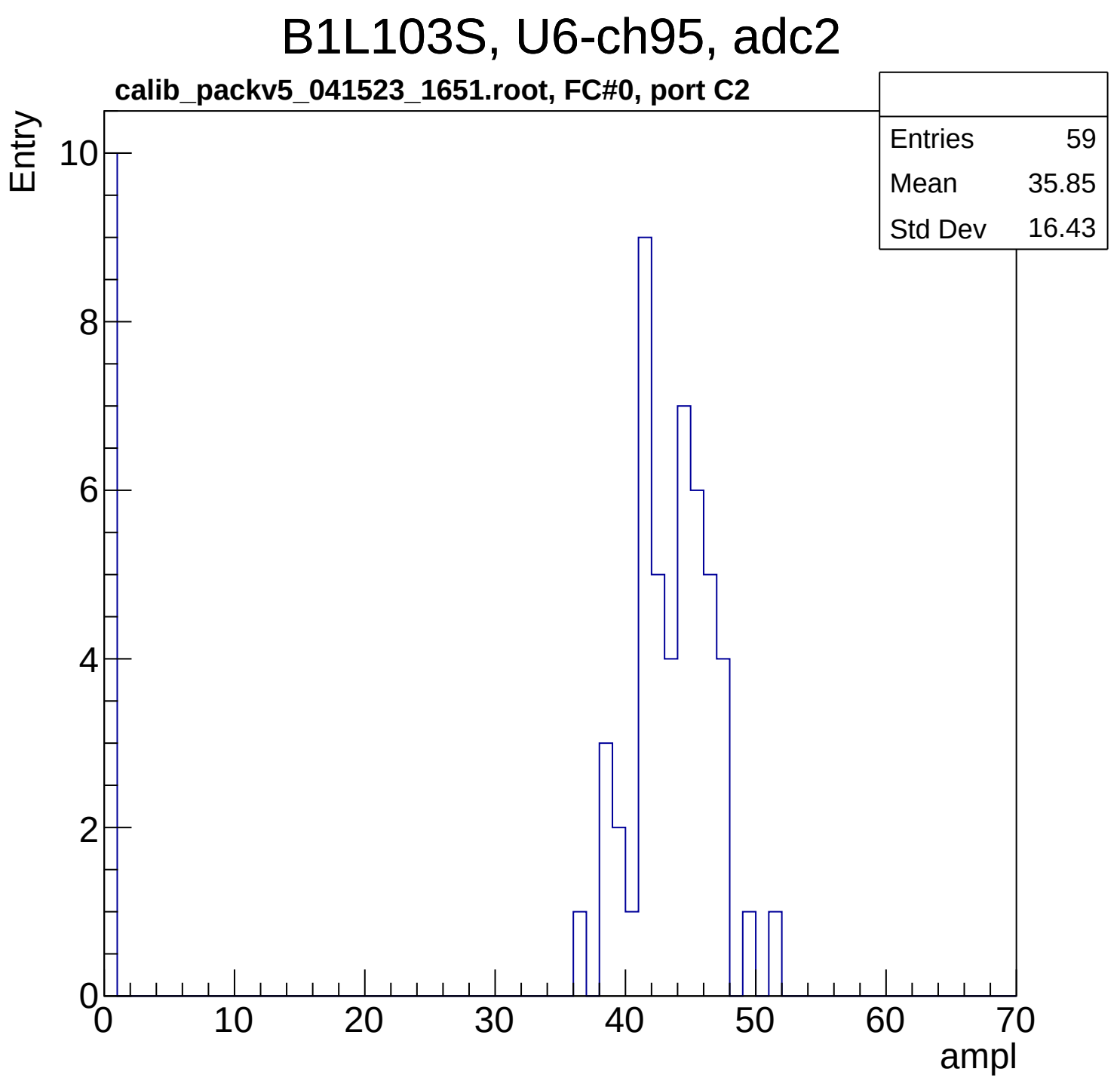
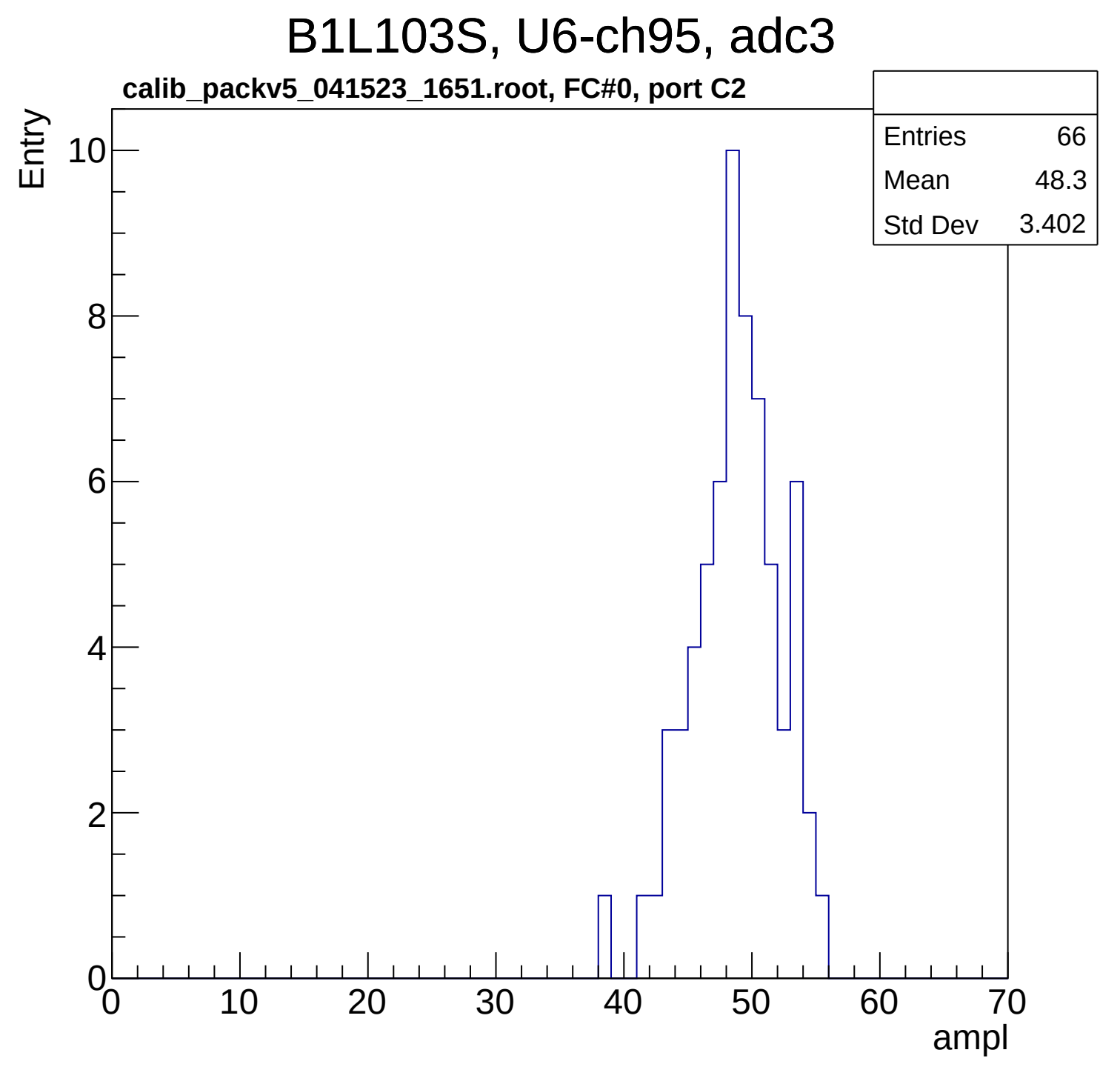
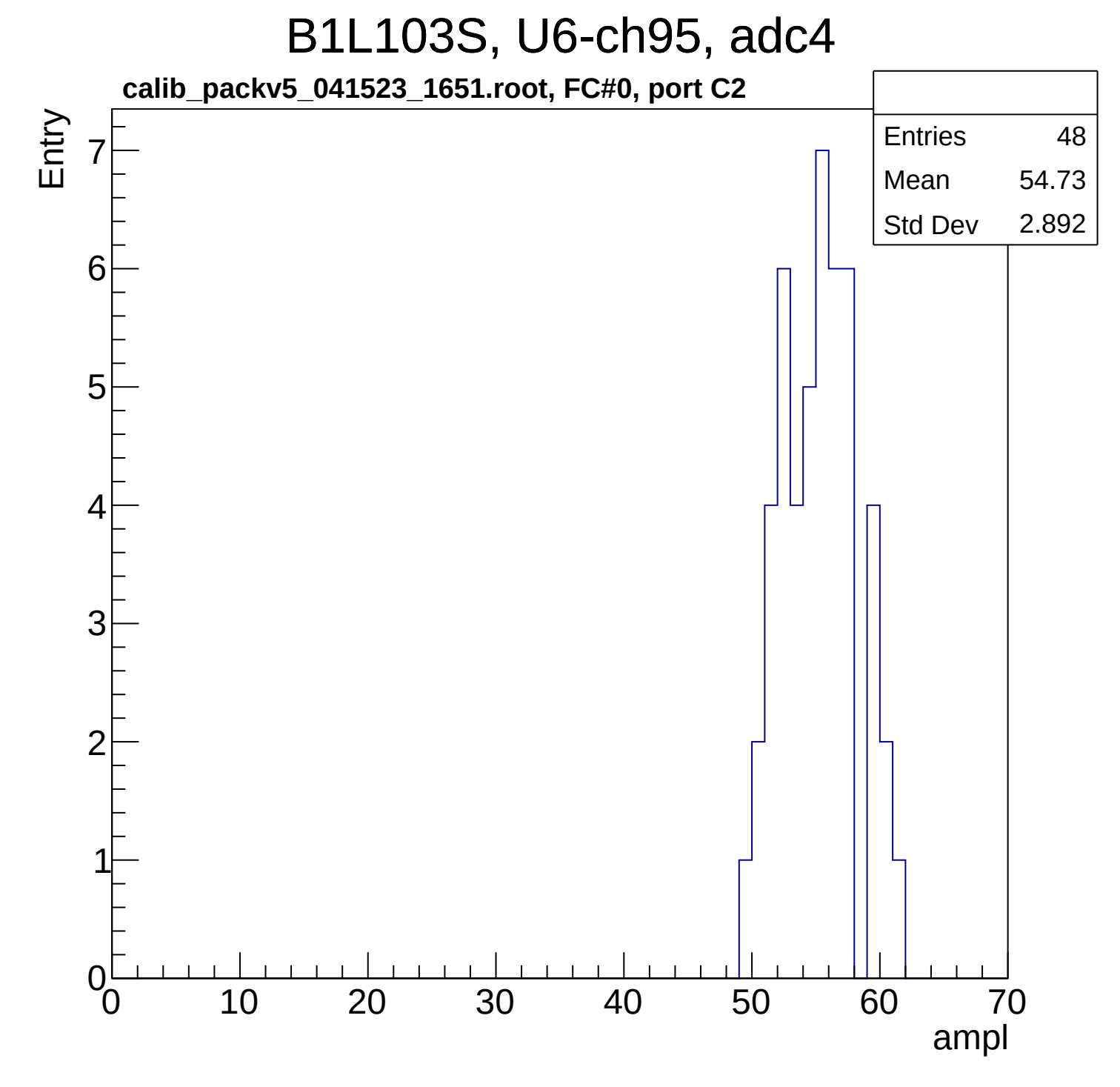
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch95, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 35.85
Std Dev 16.43
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U6-ch95, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 48.3
Std Dev 3.402
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U6-ch95, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 54.73
Std Dev 2.892
Entry
ampl
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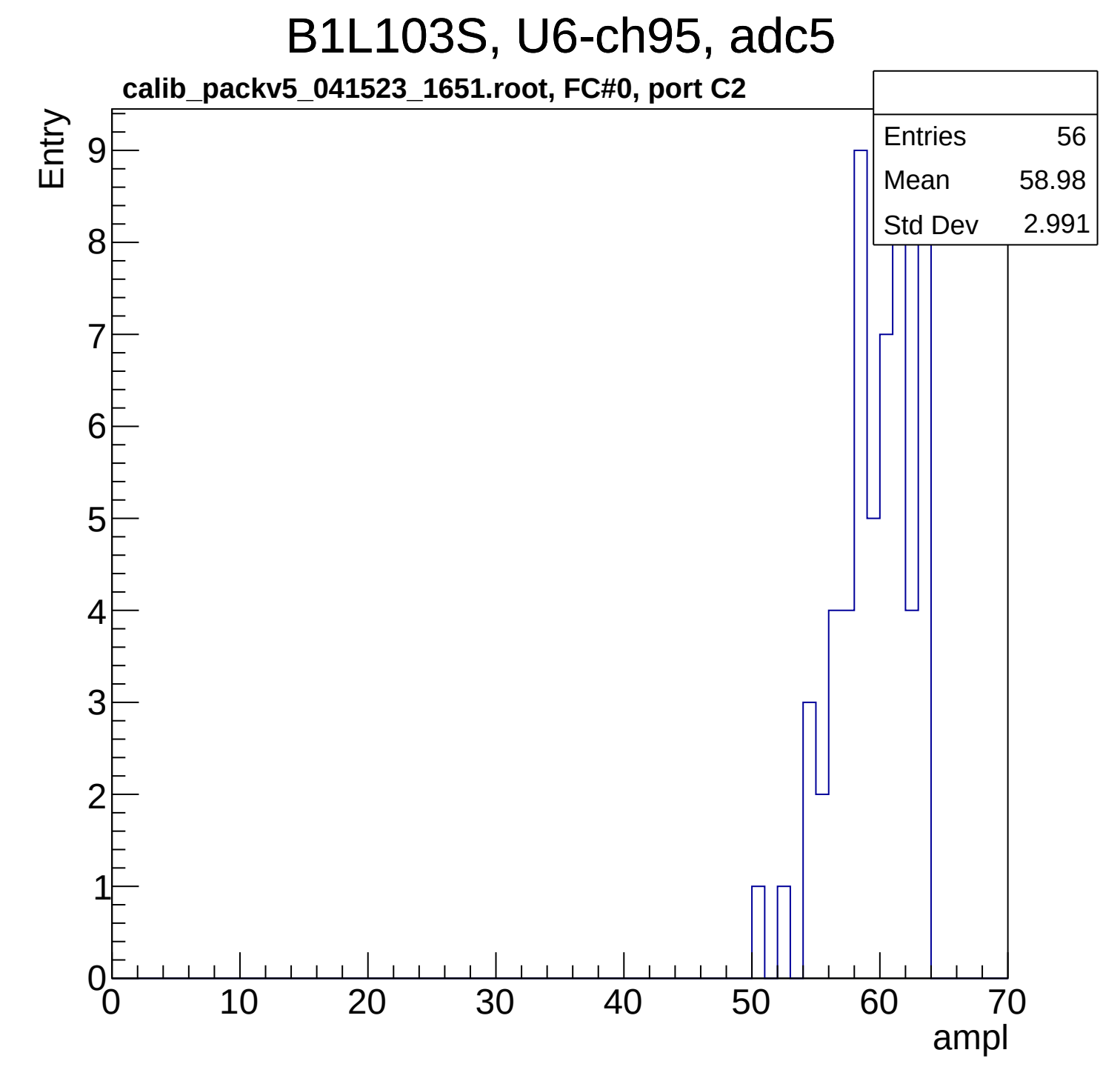
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U6-ch95, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 58.98
Std Dev 2.991
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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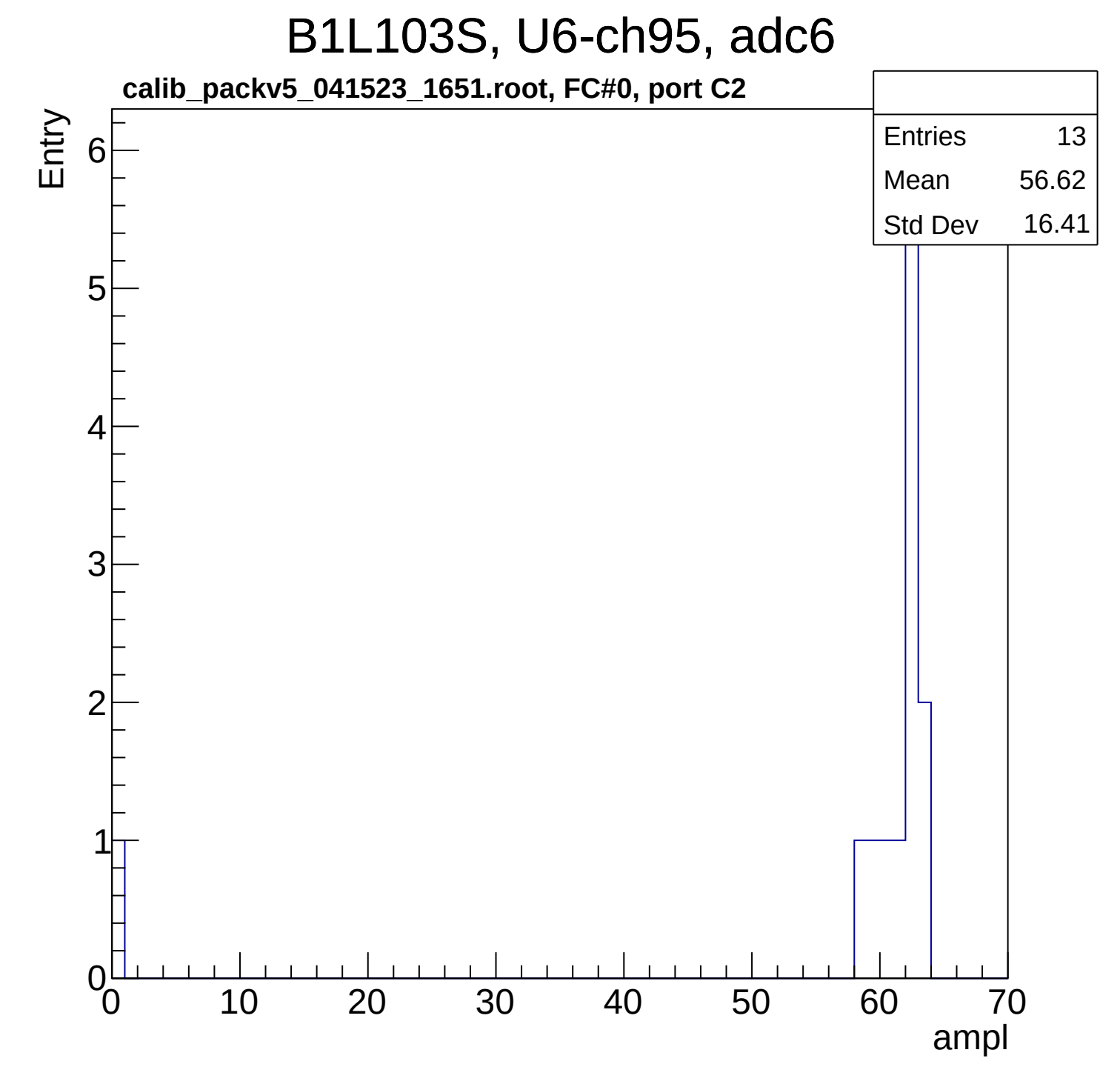
B1L103S, U6-ch95, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 56.62
Std Dev 16.41
Entry
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2
3
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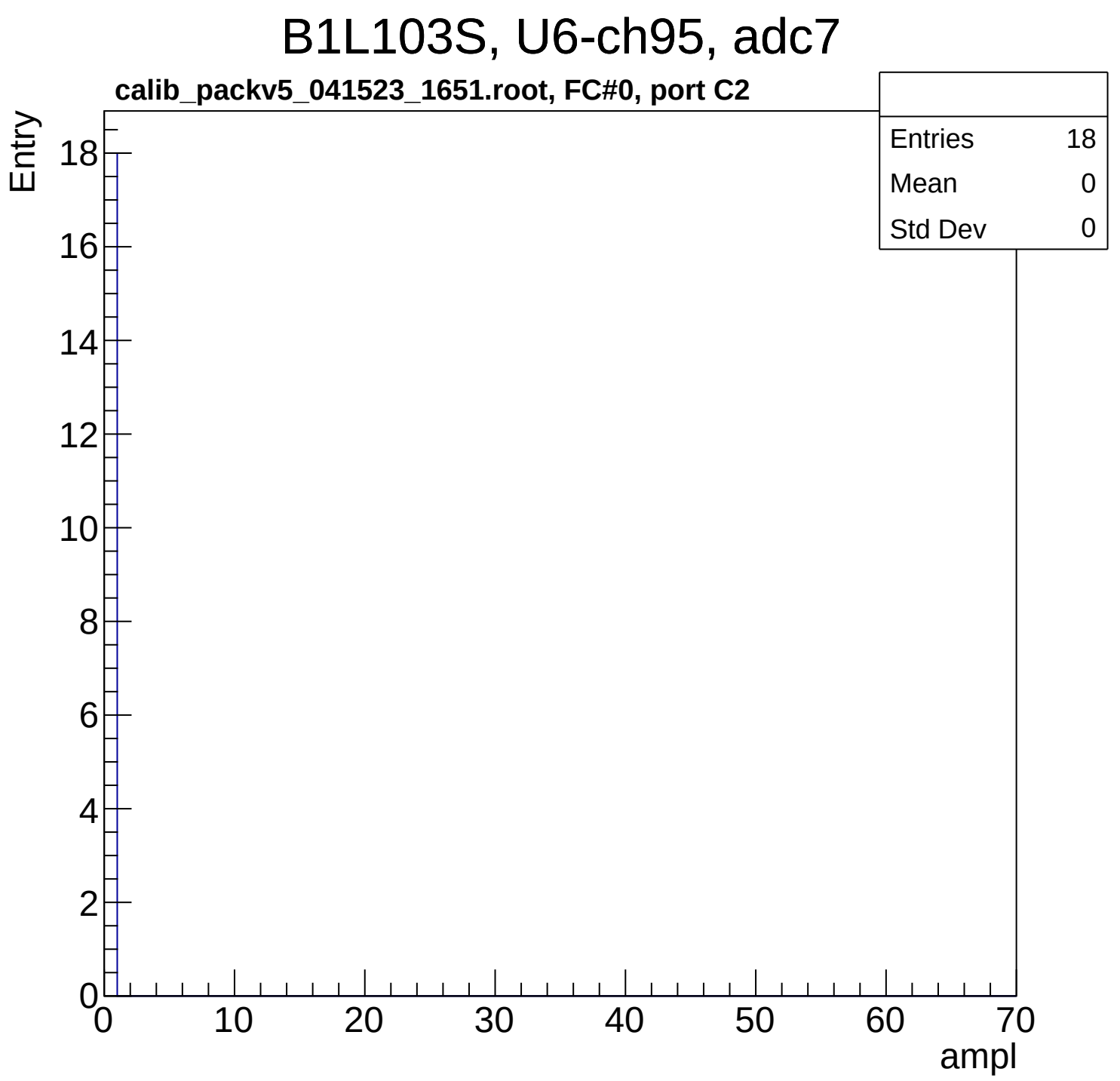
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch95, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
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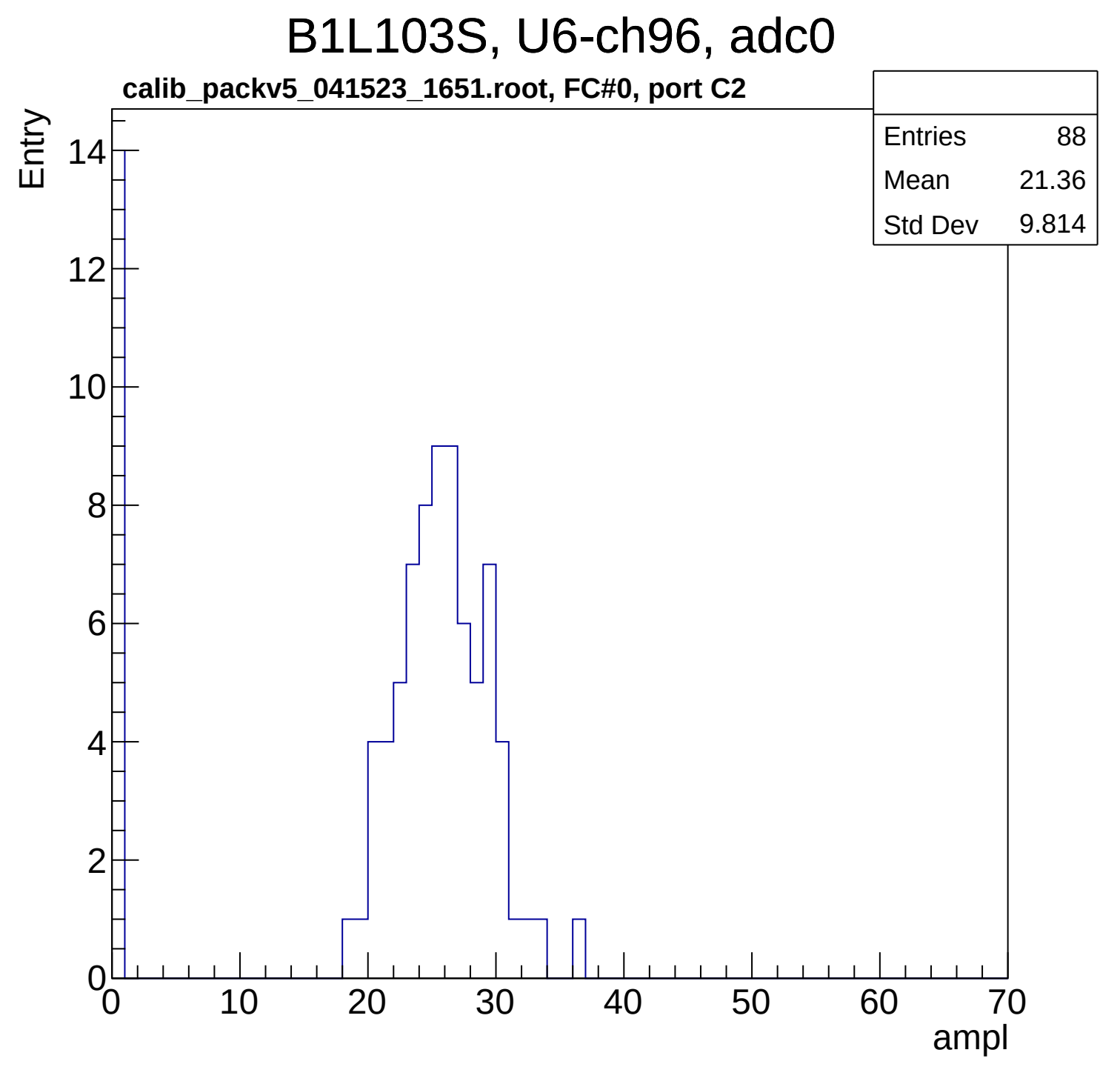
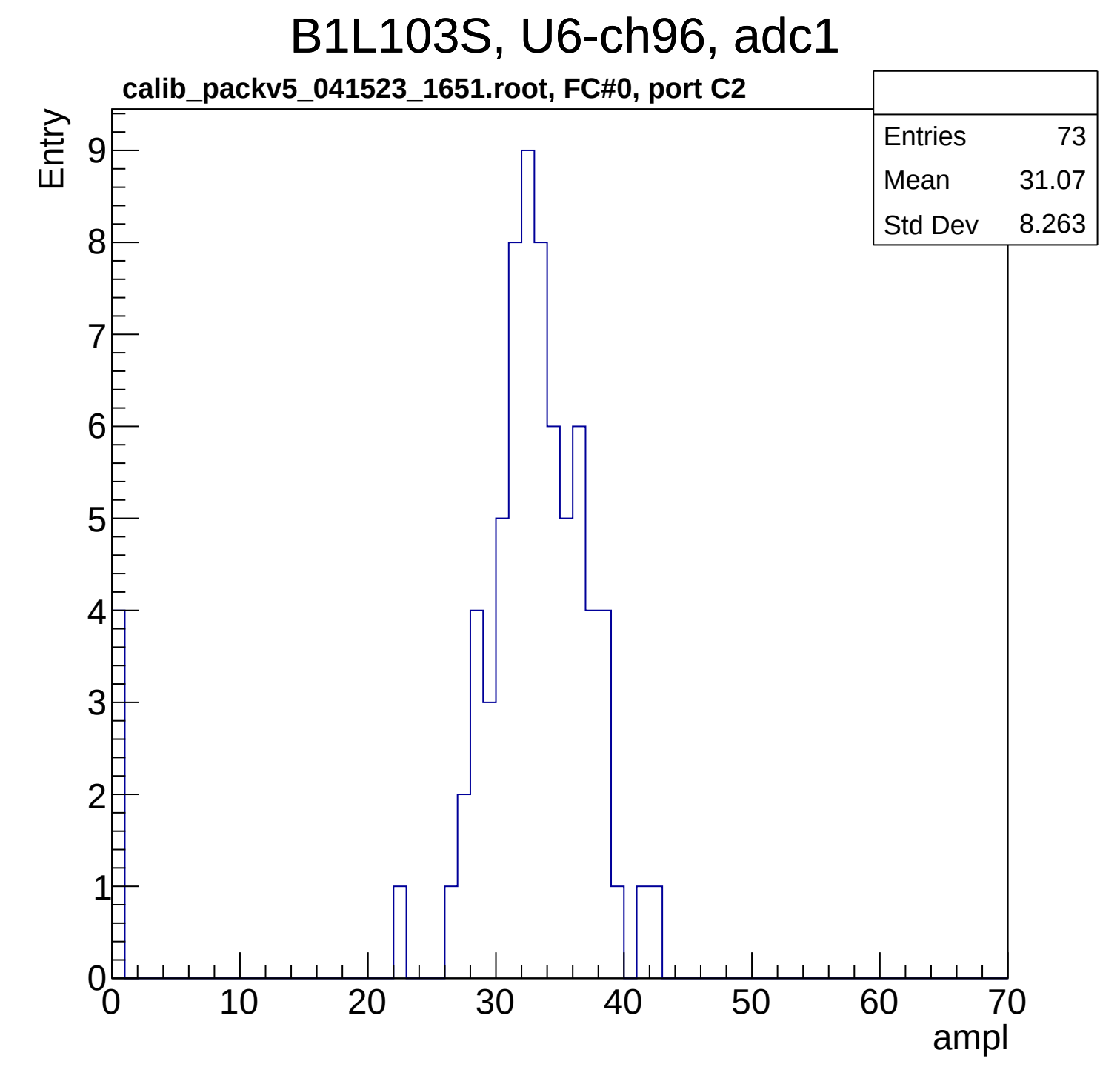
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch96, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 21.36
Std Dev 9.814
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U6-ch96, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 31.07
Std Dev 8.263
Entry
ampl
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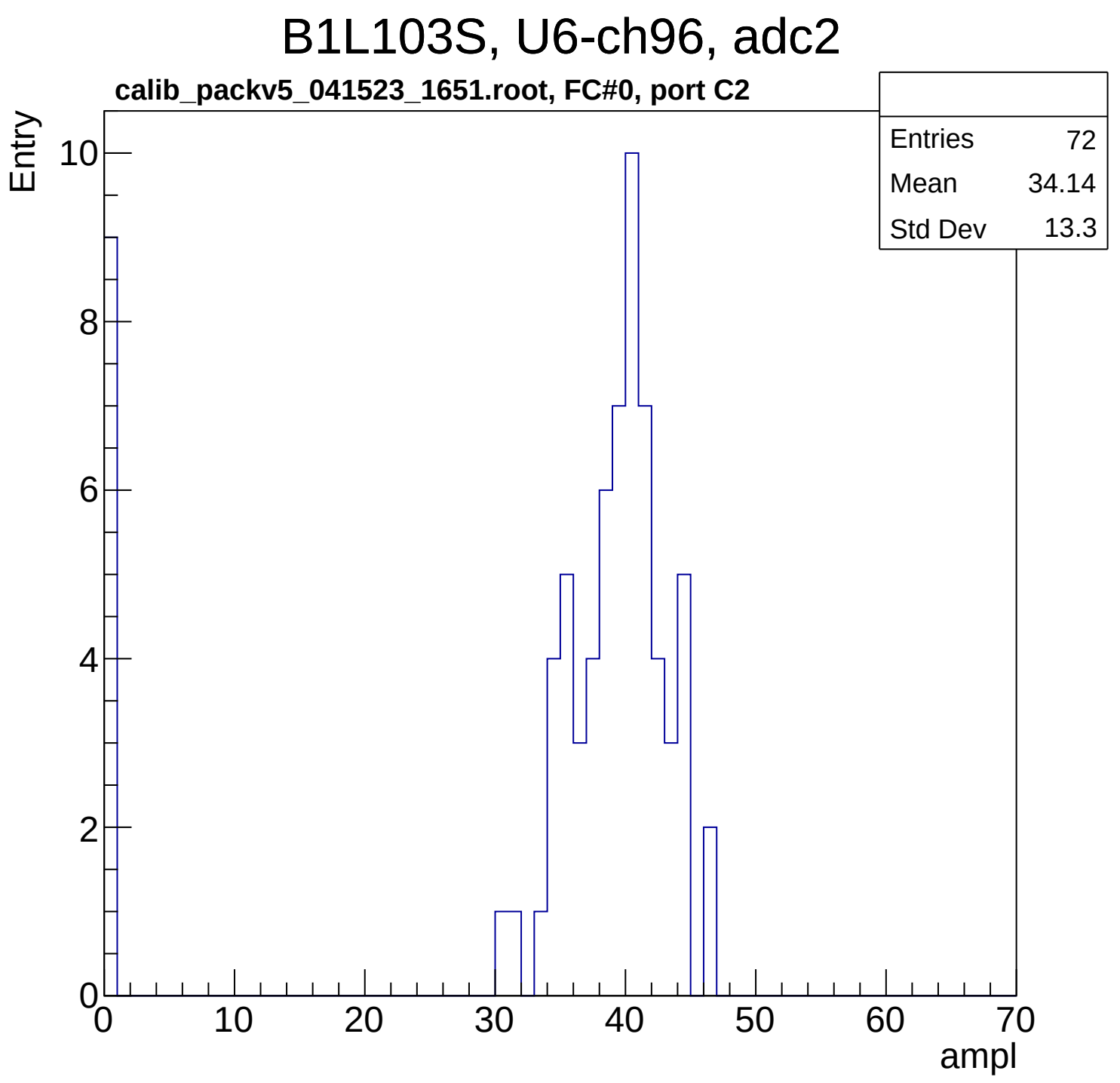
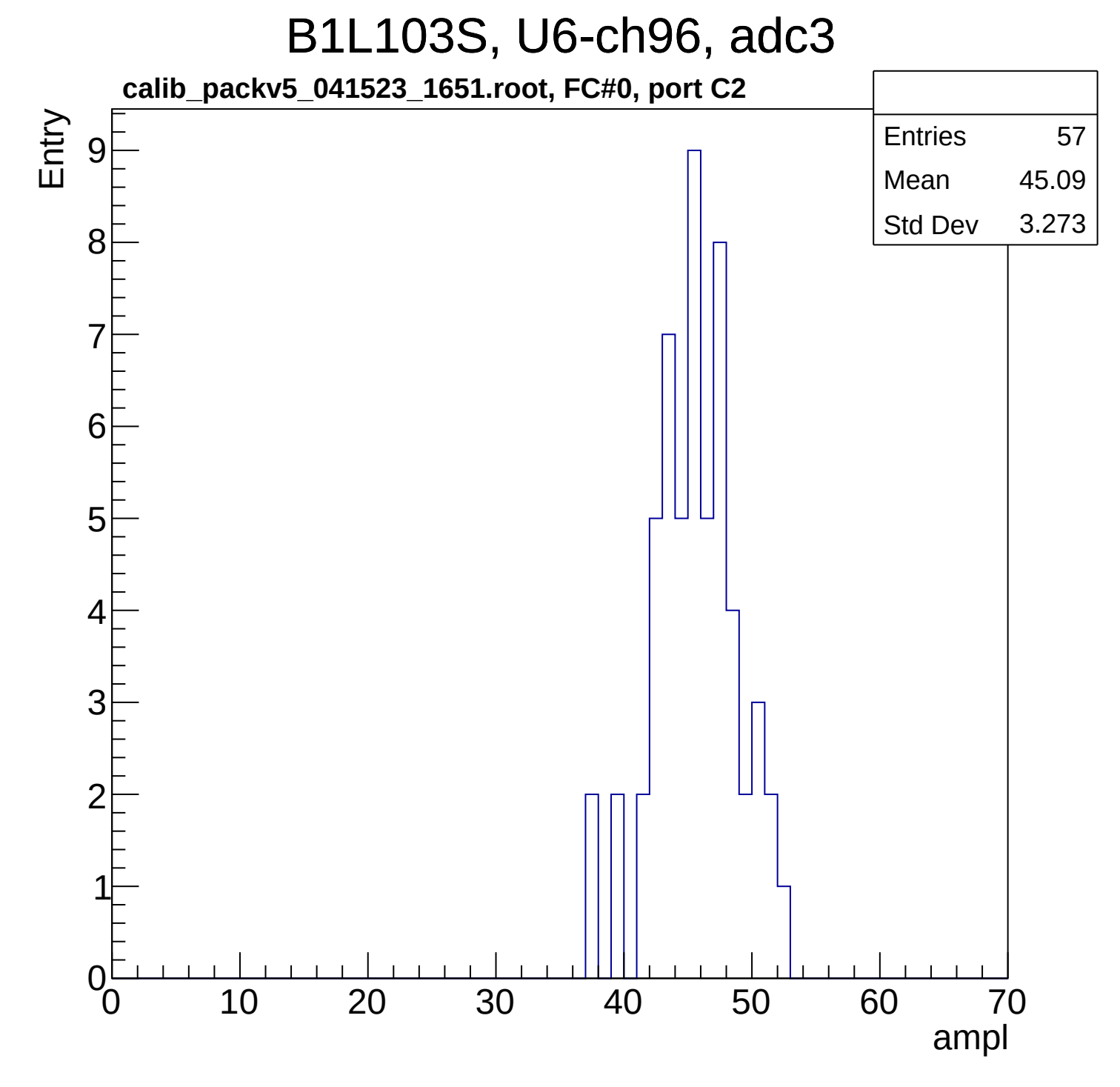
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch96, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 34.14
Std Dev 13.3
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch96, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 45.09
Std Dev 3.273
Entry
ampl
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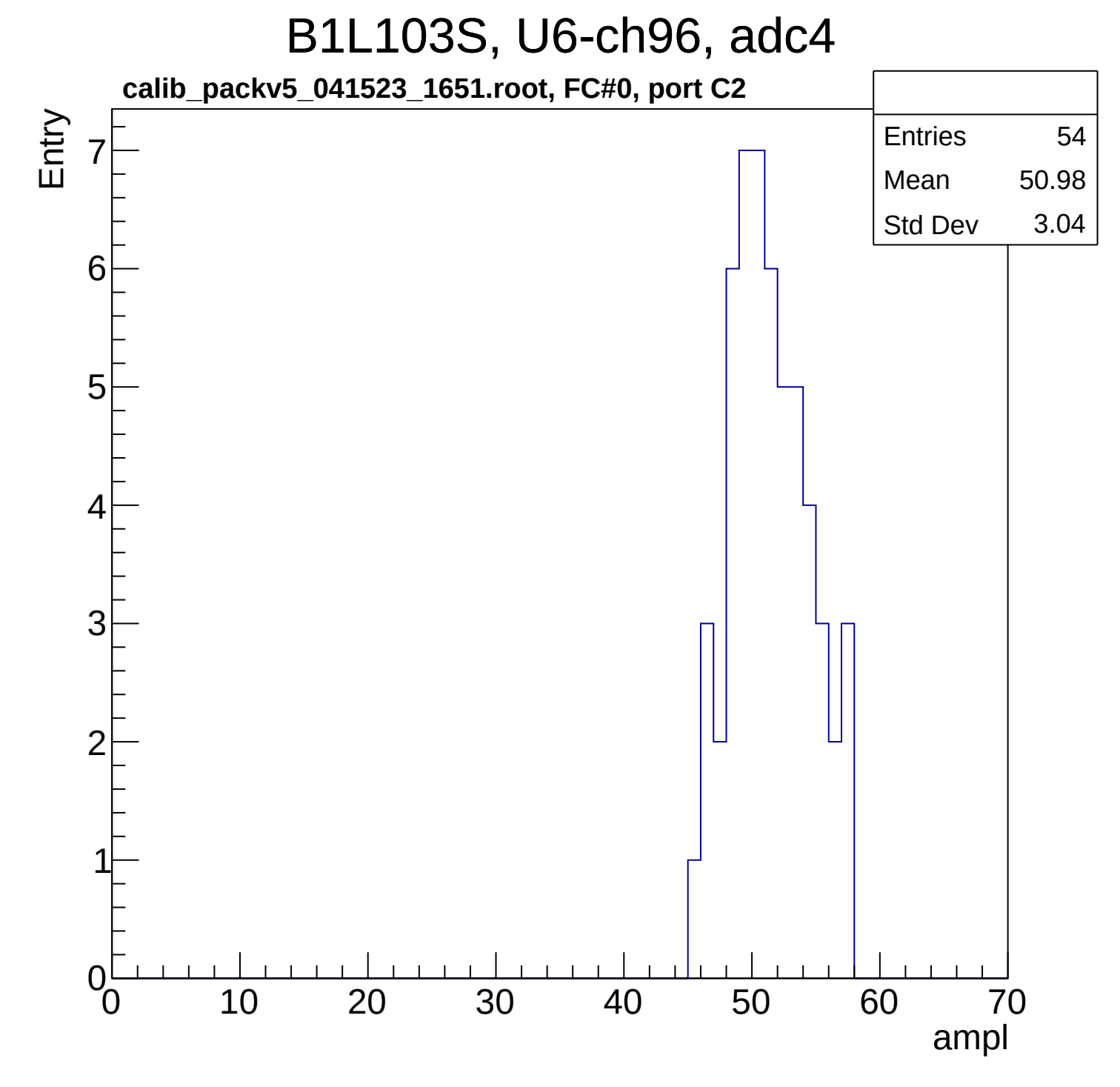
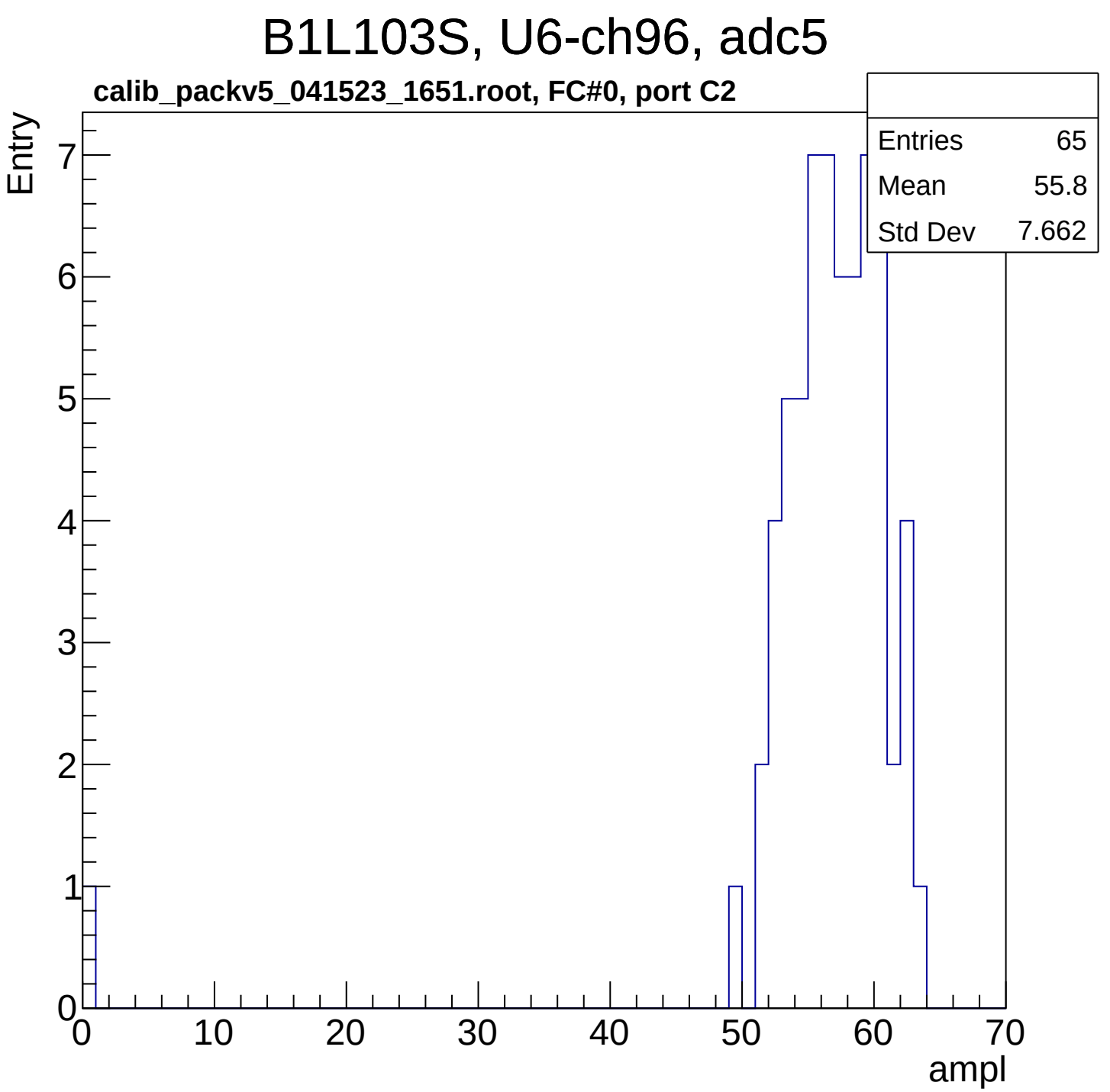
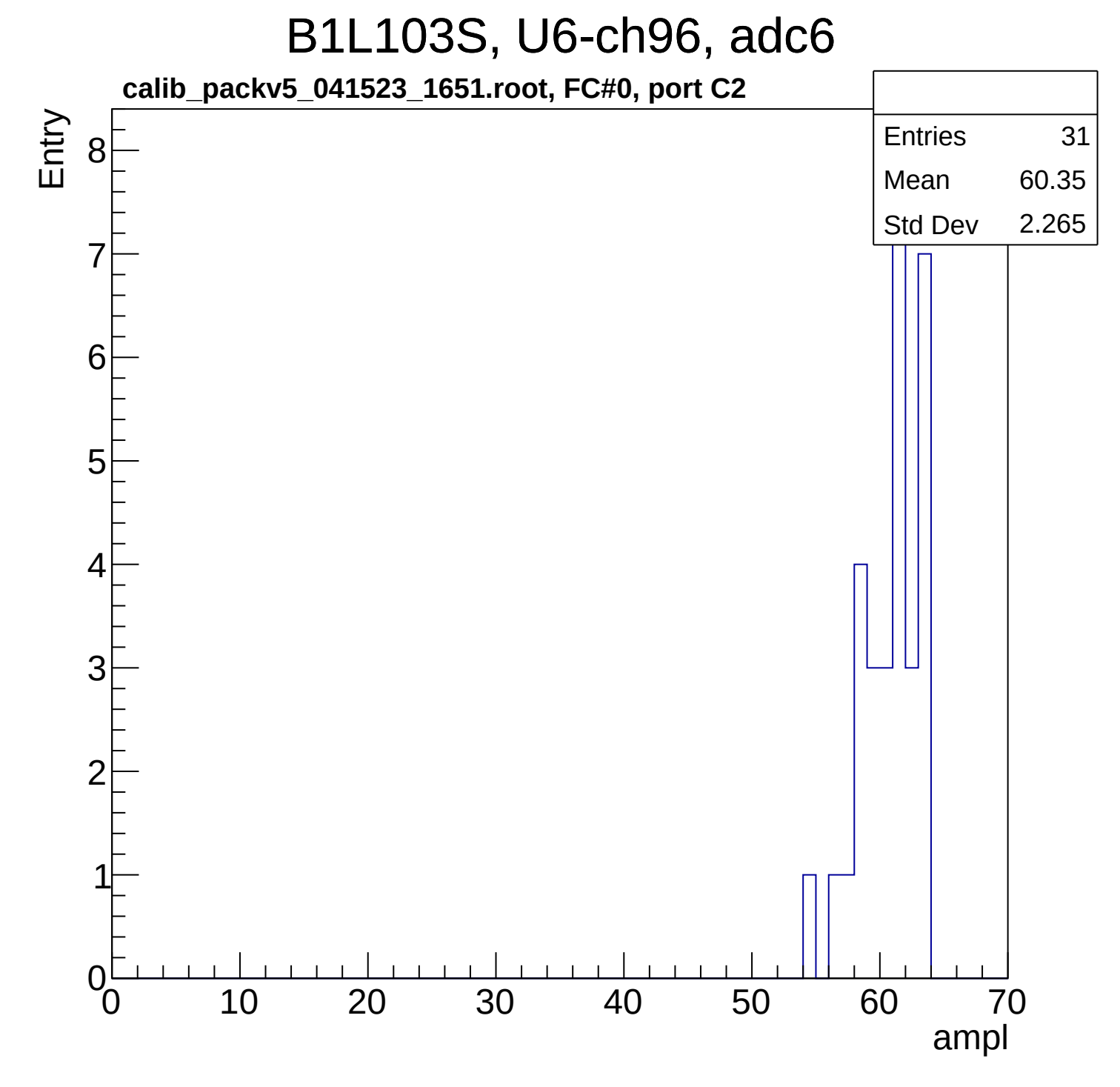
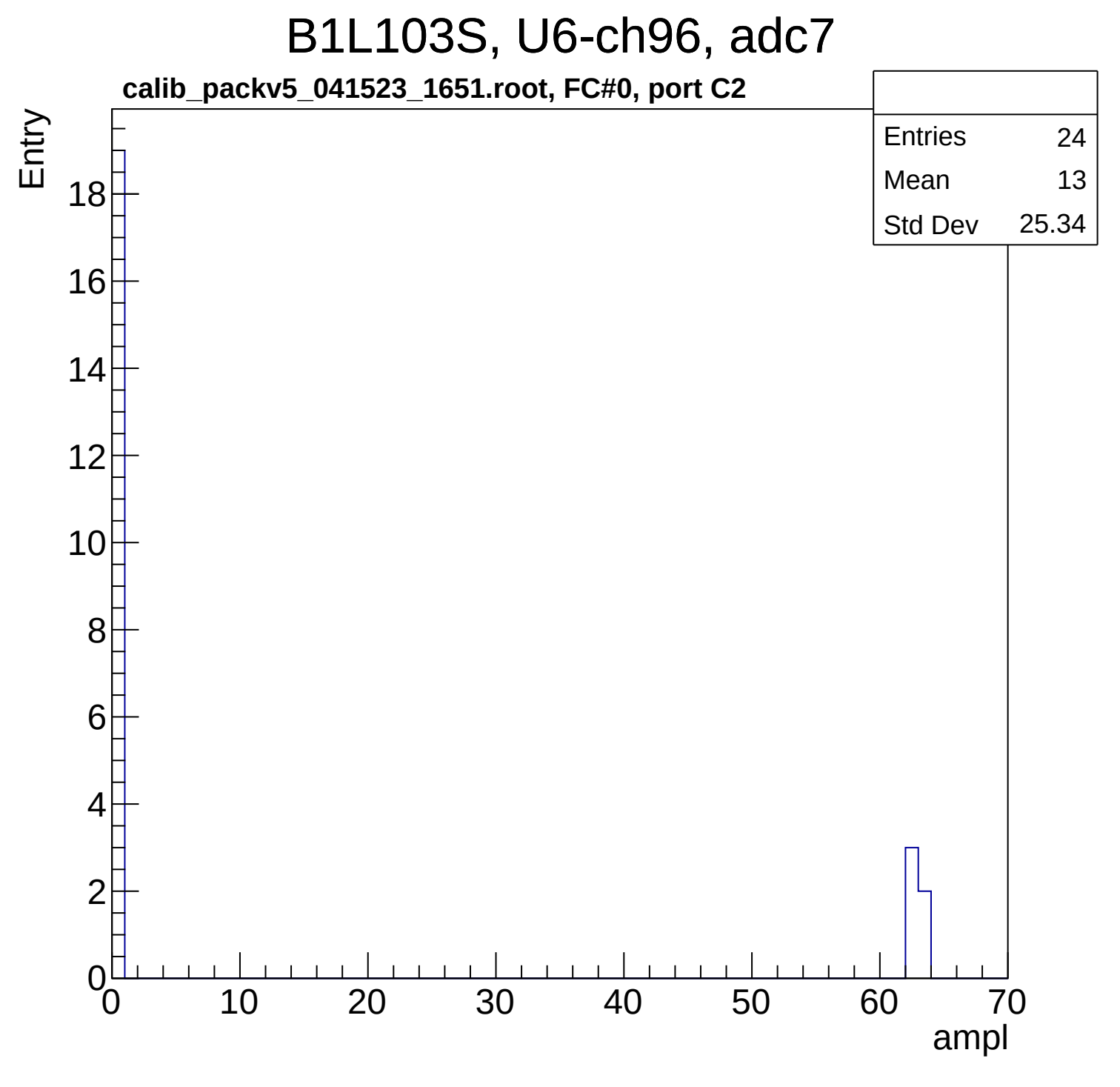
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch96, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 50.98
Std Dev 3.04
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U6-ch96, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 55.8
Std Dev 7.662
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U6-ch96, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 60.35
Std Dev 2.265
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch96, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 13
Std Dev 25.34
Entry
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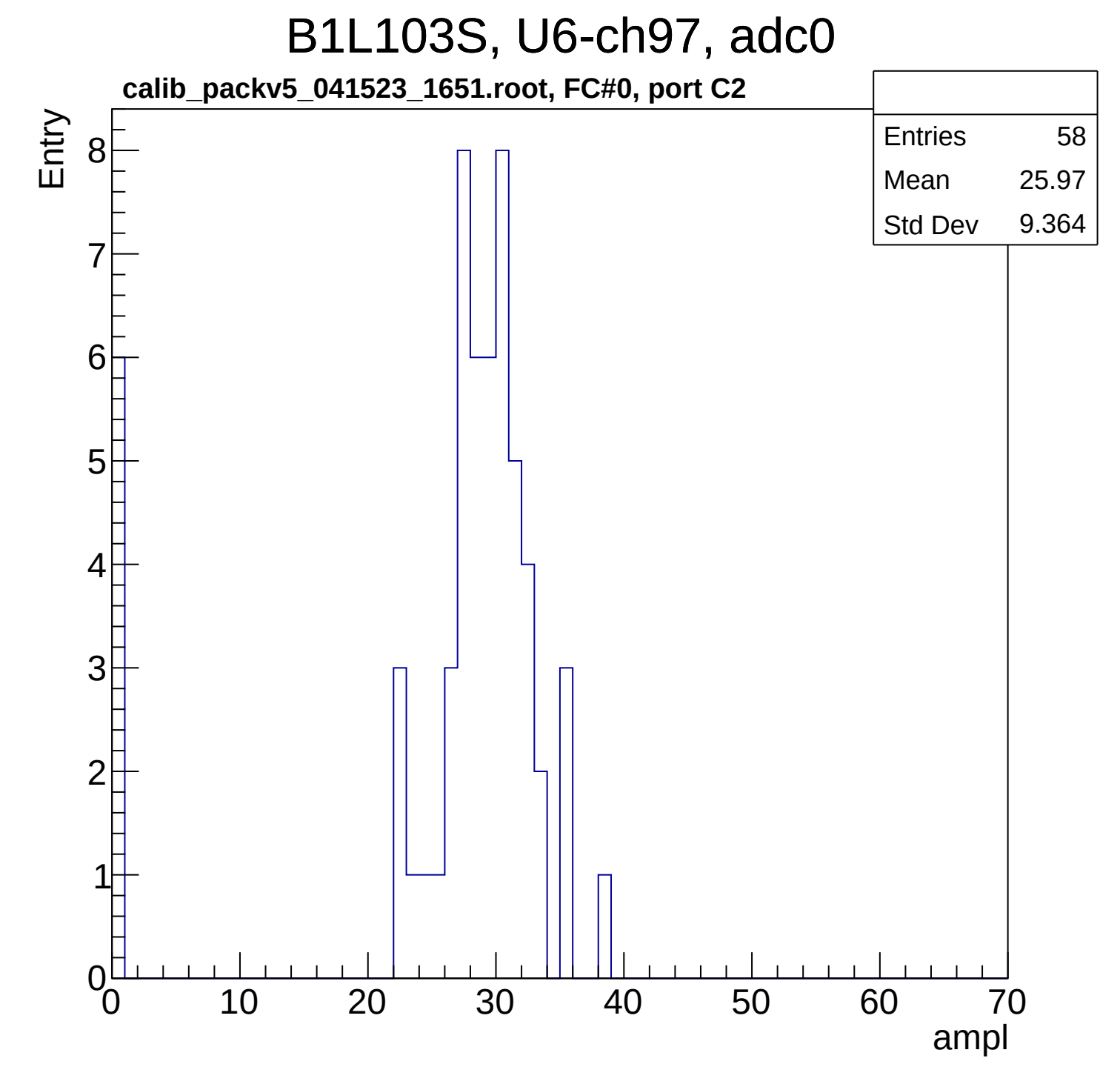
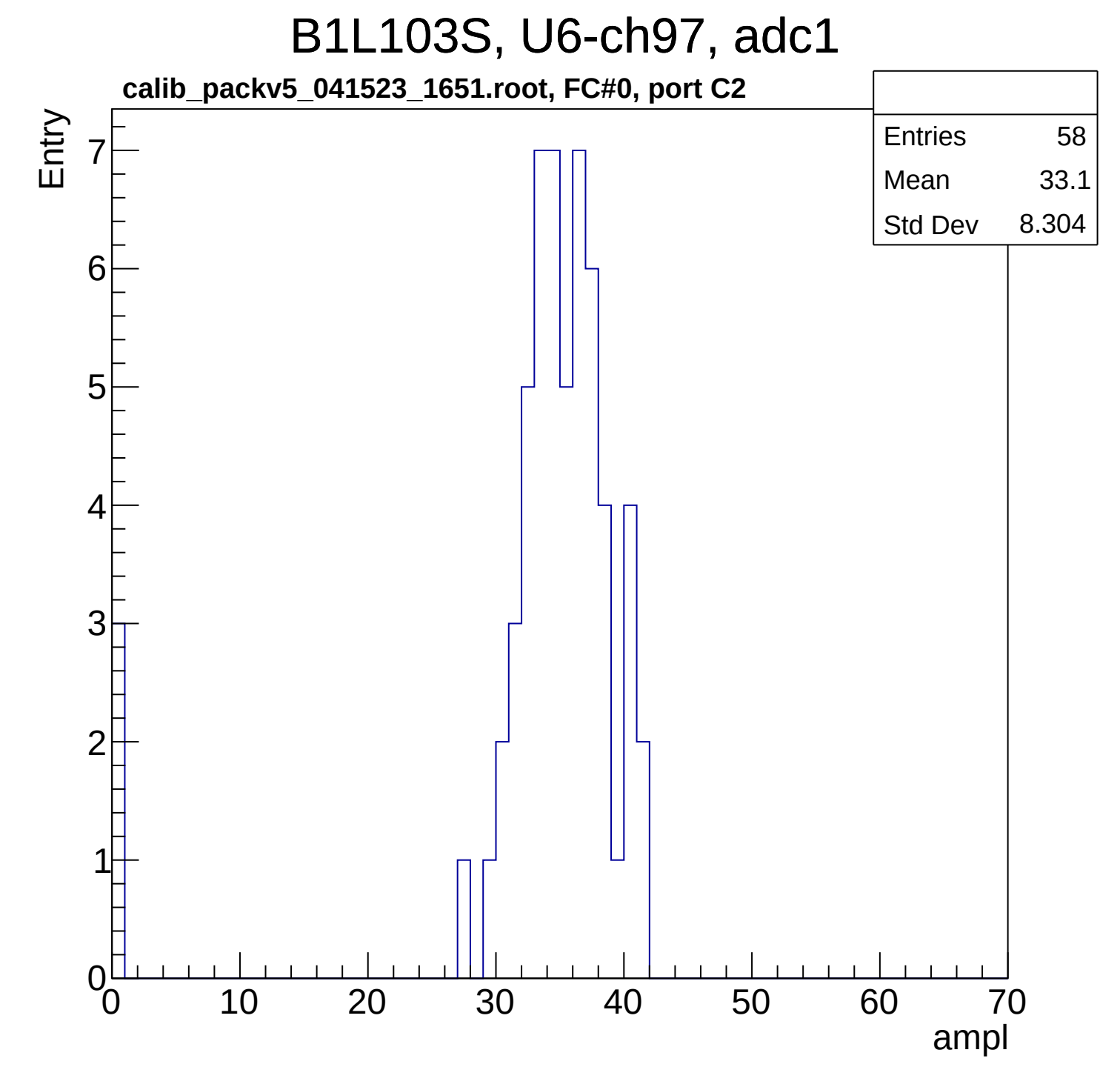
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch97, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 25.97
Std Dev 9.364
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch97, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 33.1
Std Dev 8.304
Entry
ampl
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2
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4
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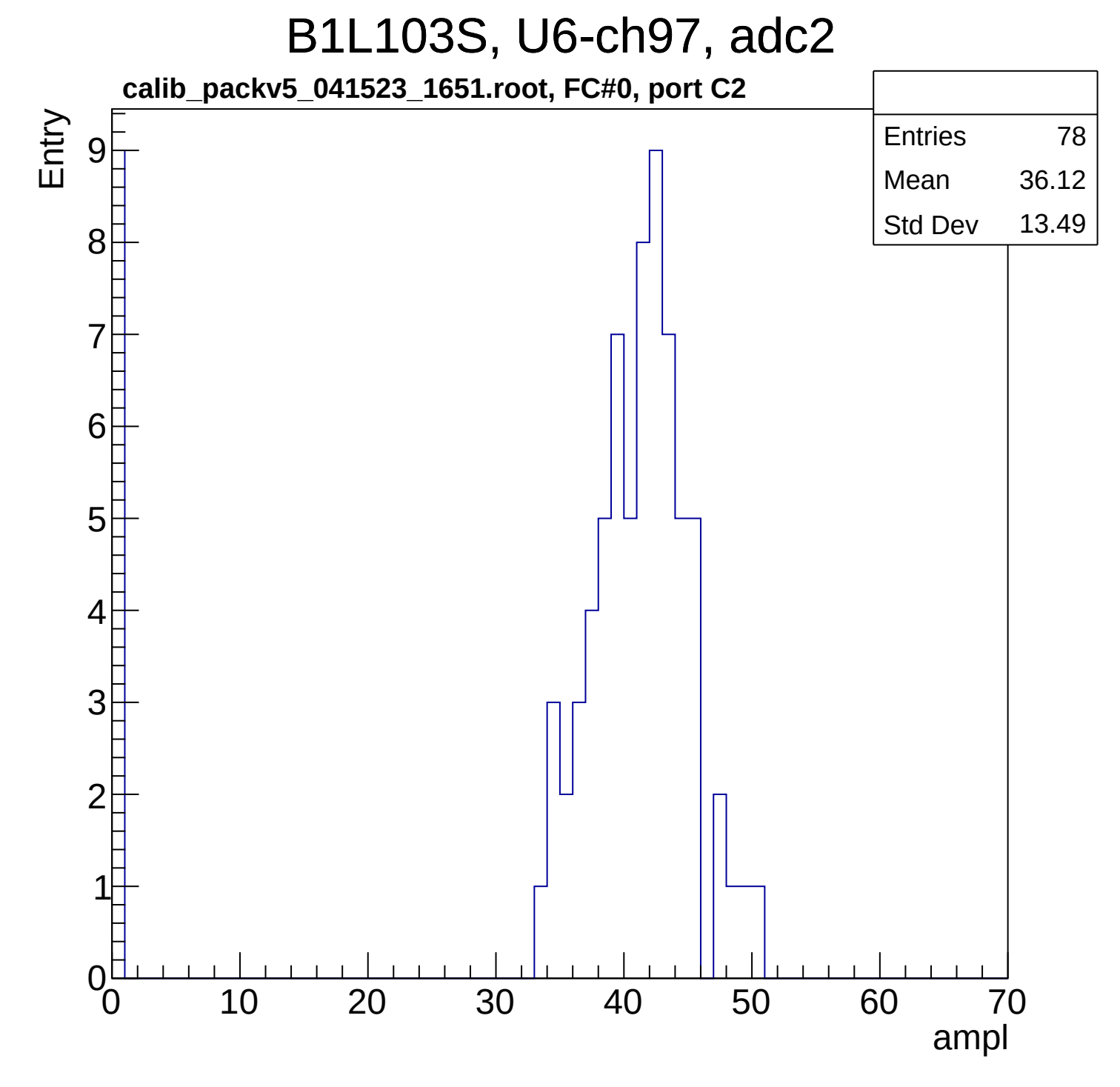
B1L103S, U6-ch97, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 36.12
Std Dev 13.49
Entry
ampl
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5
6
7
8
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0
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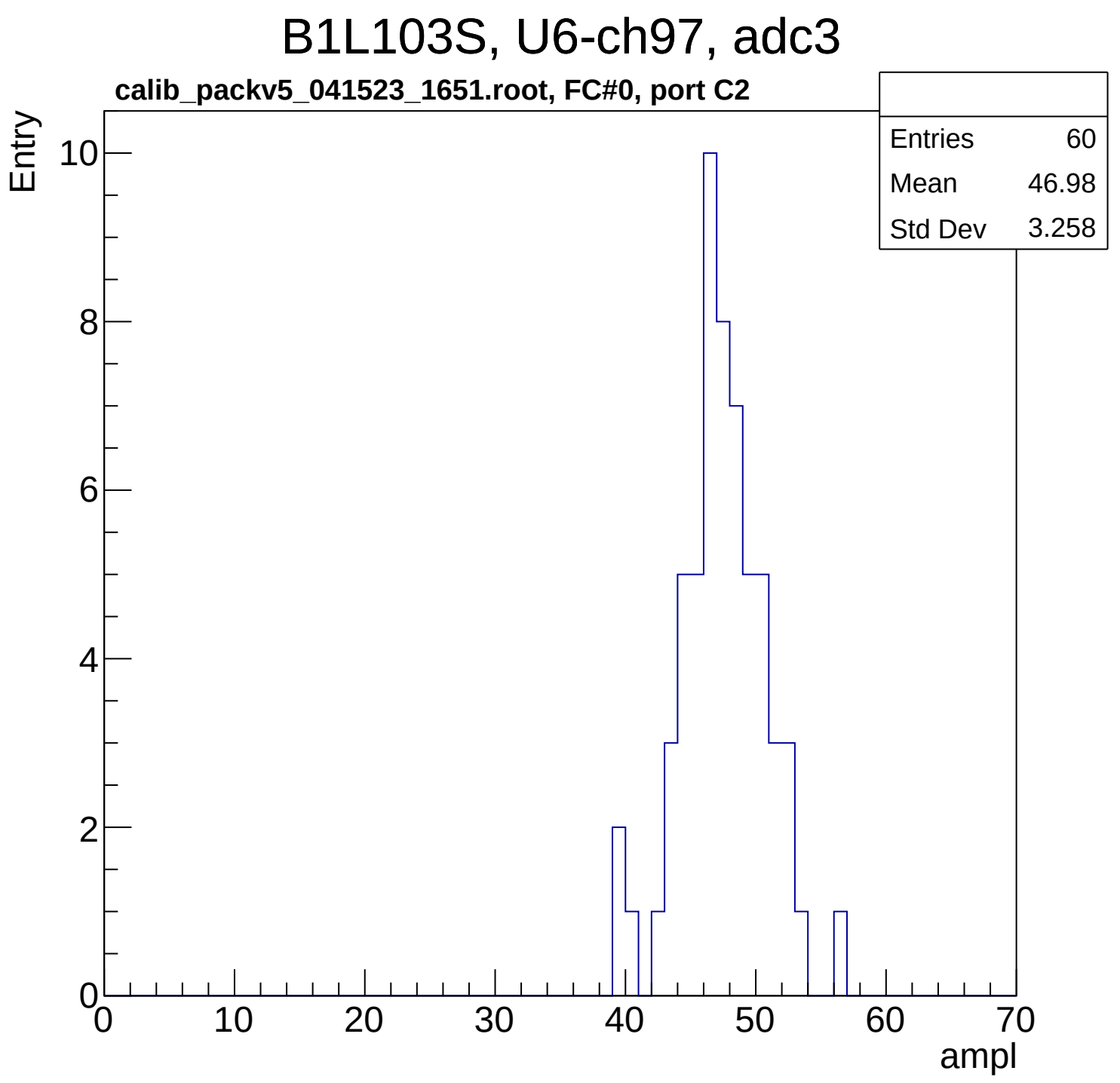
B1L103S, U6-ch97, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 46.98
Std Dev 3.258
Entry
ampl
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4
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0
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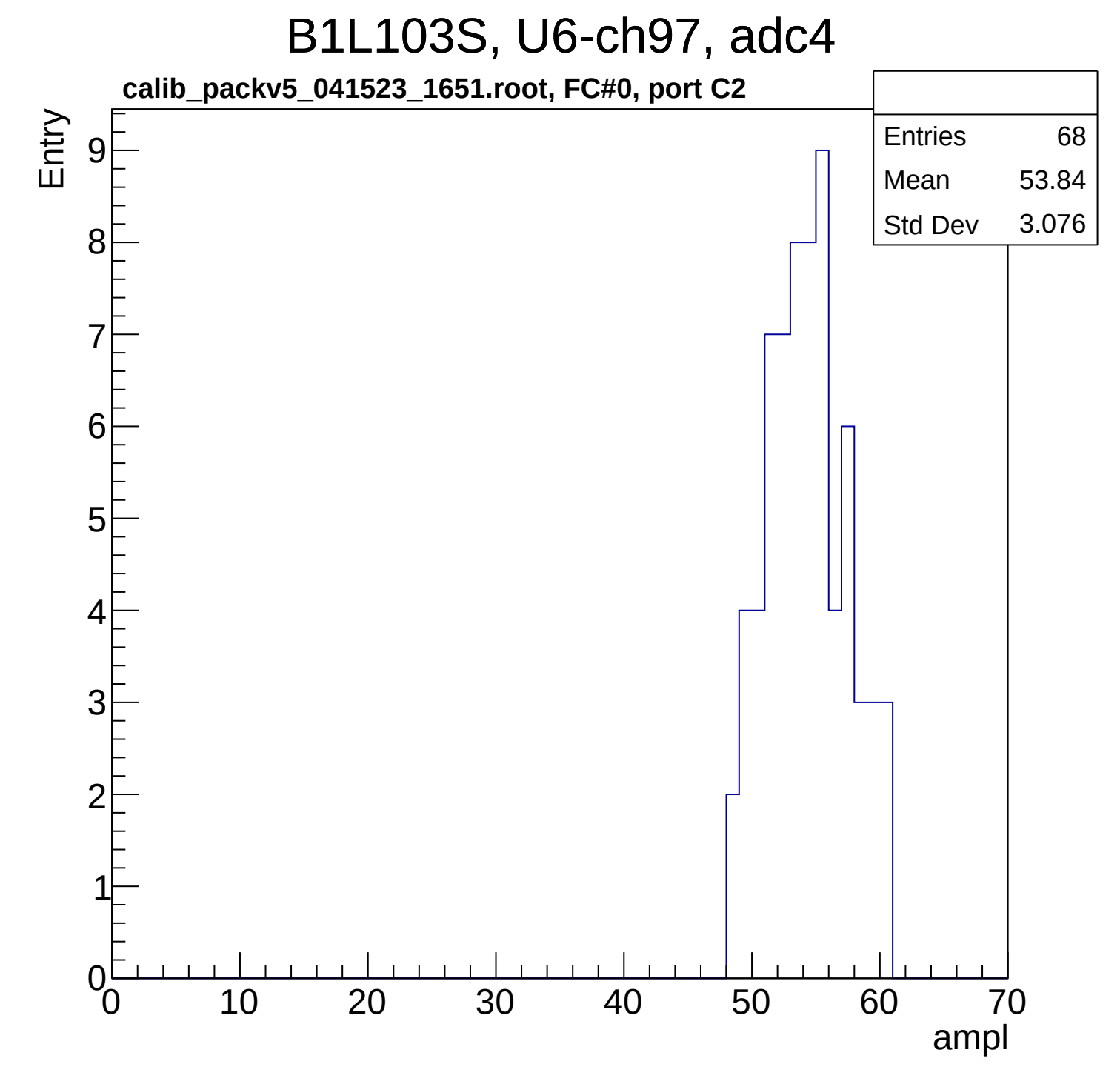
B1L103S, U6-ch97, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 53.84
Std Dev 3.076
Entry
ampl
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6
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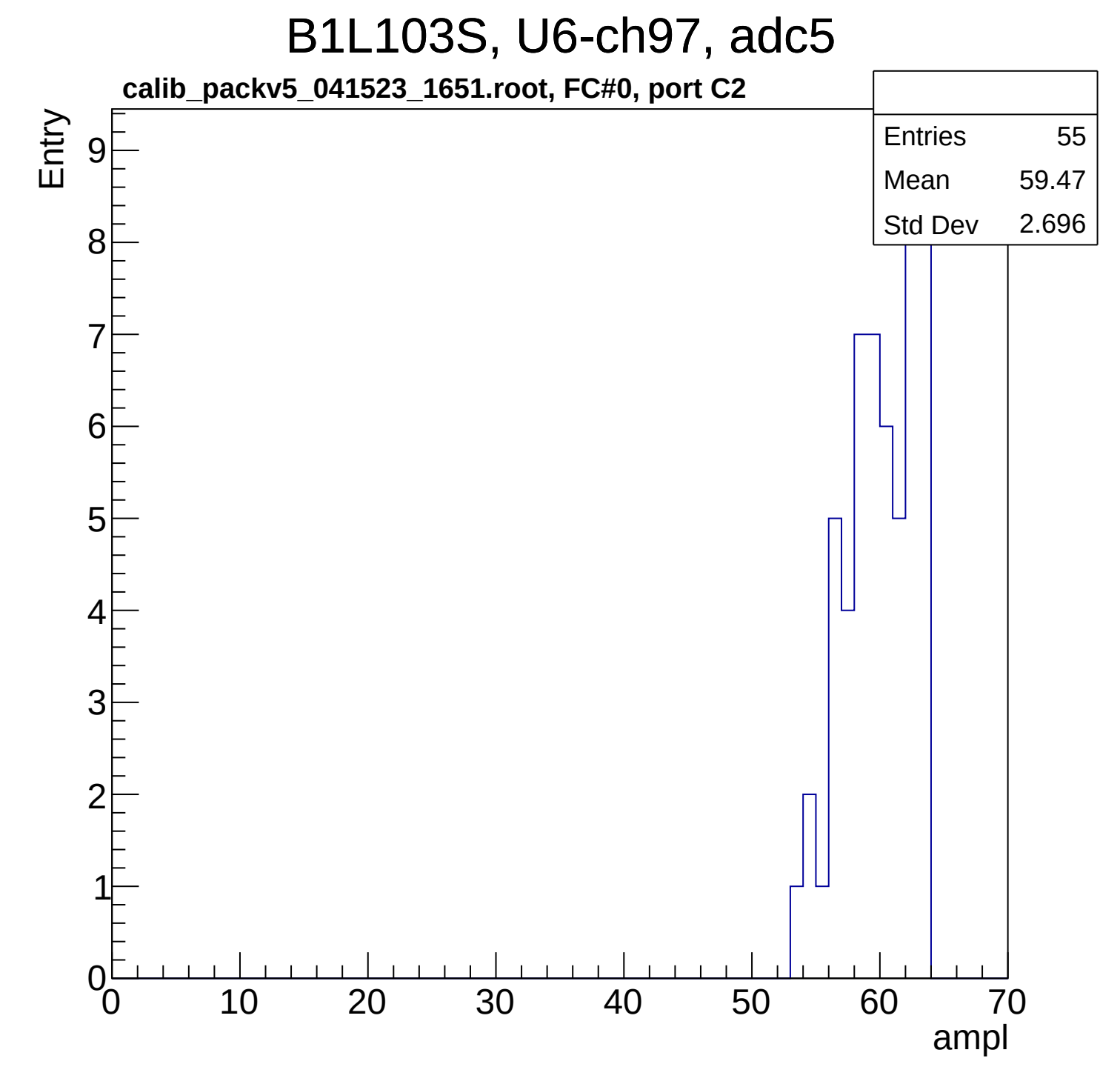
B1L103S, U6-ch97, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 59.47
Std Dev 2.696
Entry
ampl
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4
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8
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0
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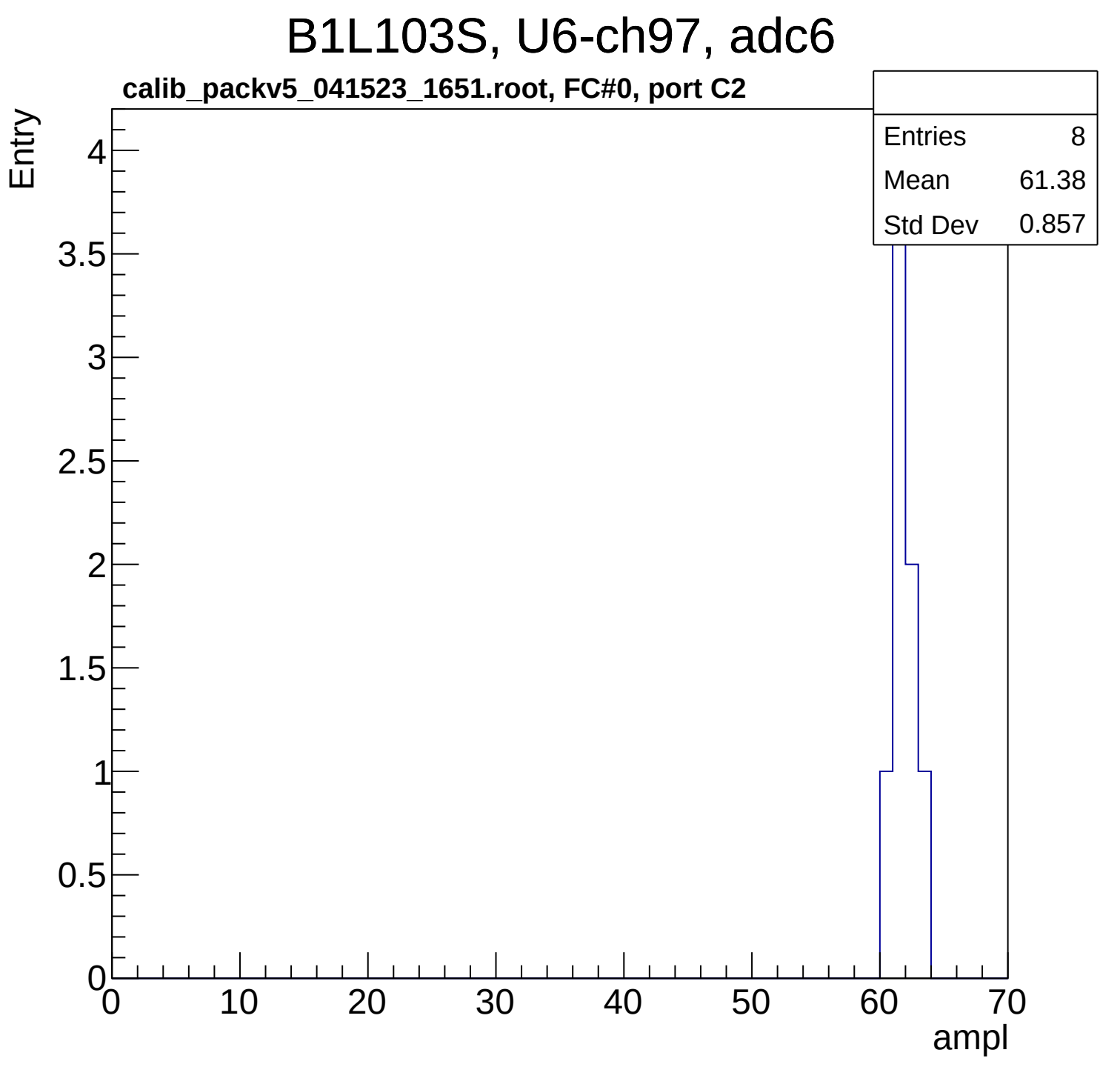
B1L103S, U6-ch97, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 61.38
Std Dev 0.857
Entry
ampl
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1.5
2
2.5
3
3.5
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0
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40
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60
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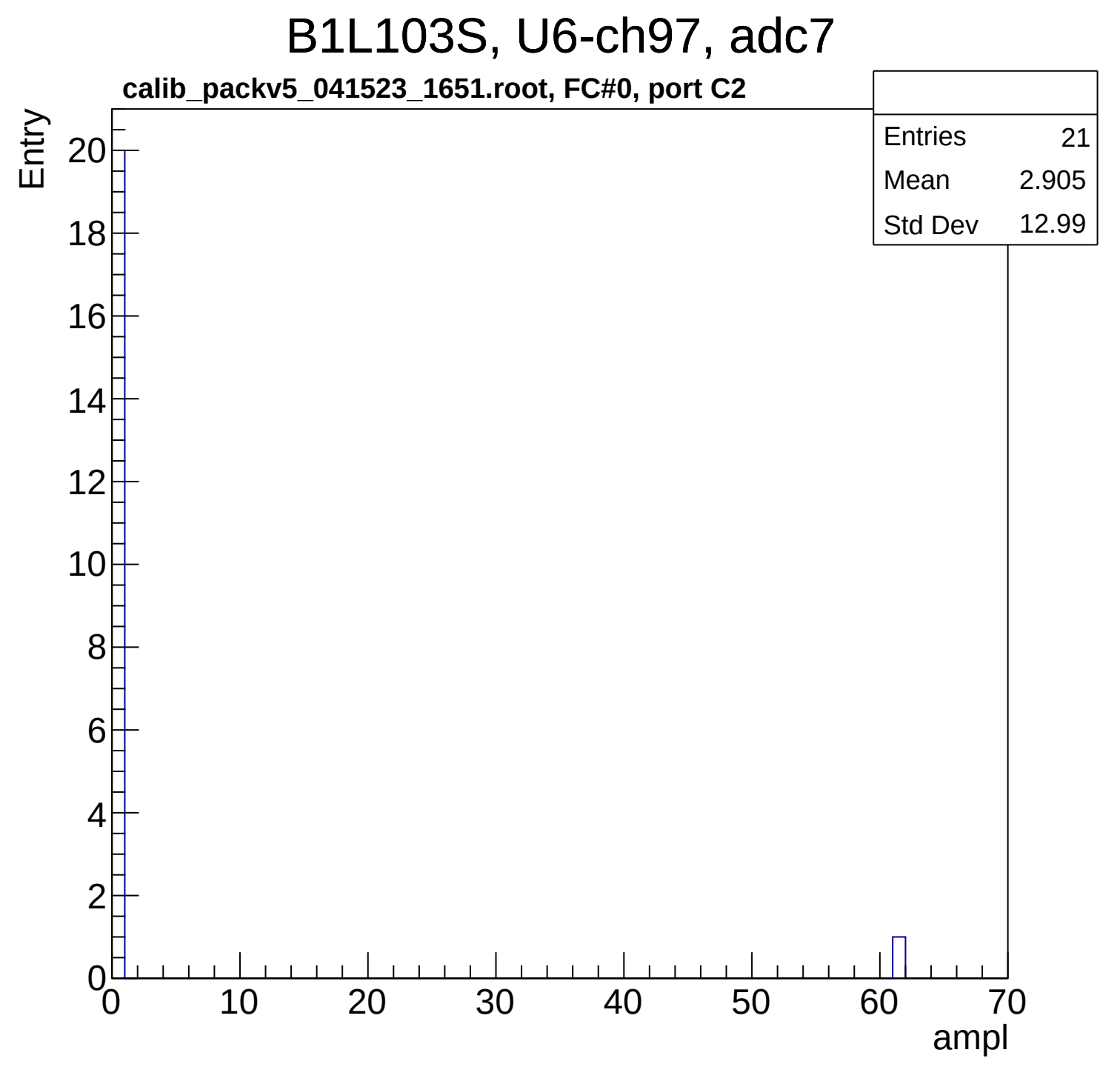
B1L103S, U6-ch97, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 2.905
Std Dev 12.99
Entry
0
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8
10
12
14
16
18
20
0
10
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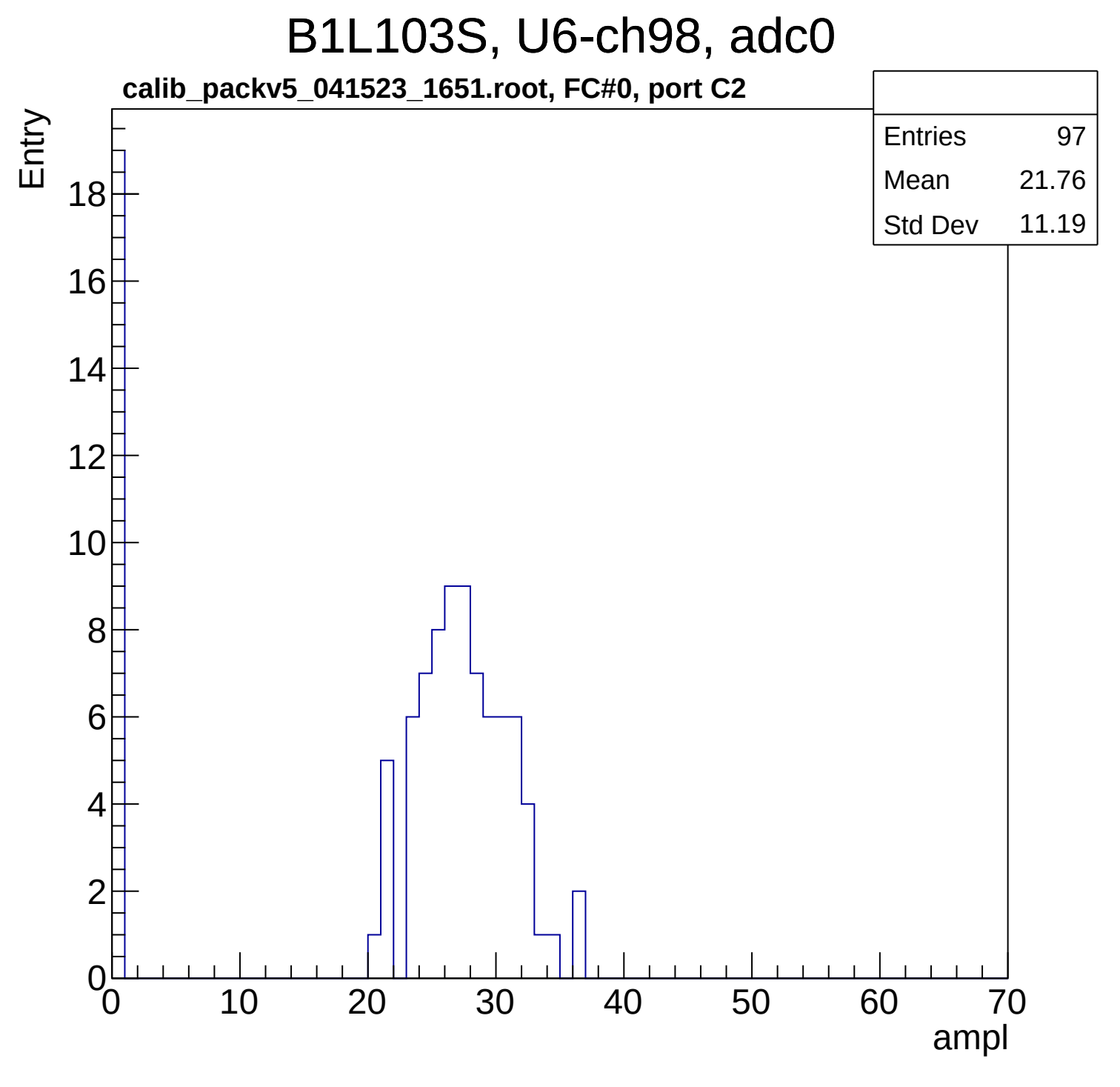
30
40
50
60
70
ampl


B1L103S, U6-ch98, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 21.76
Std Dev 11.19
Entry
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6
8
10
12
14
16
18
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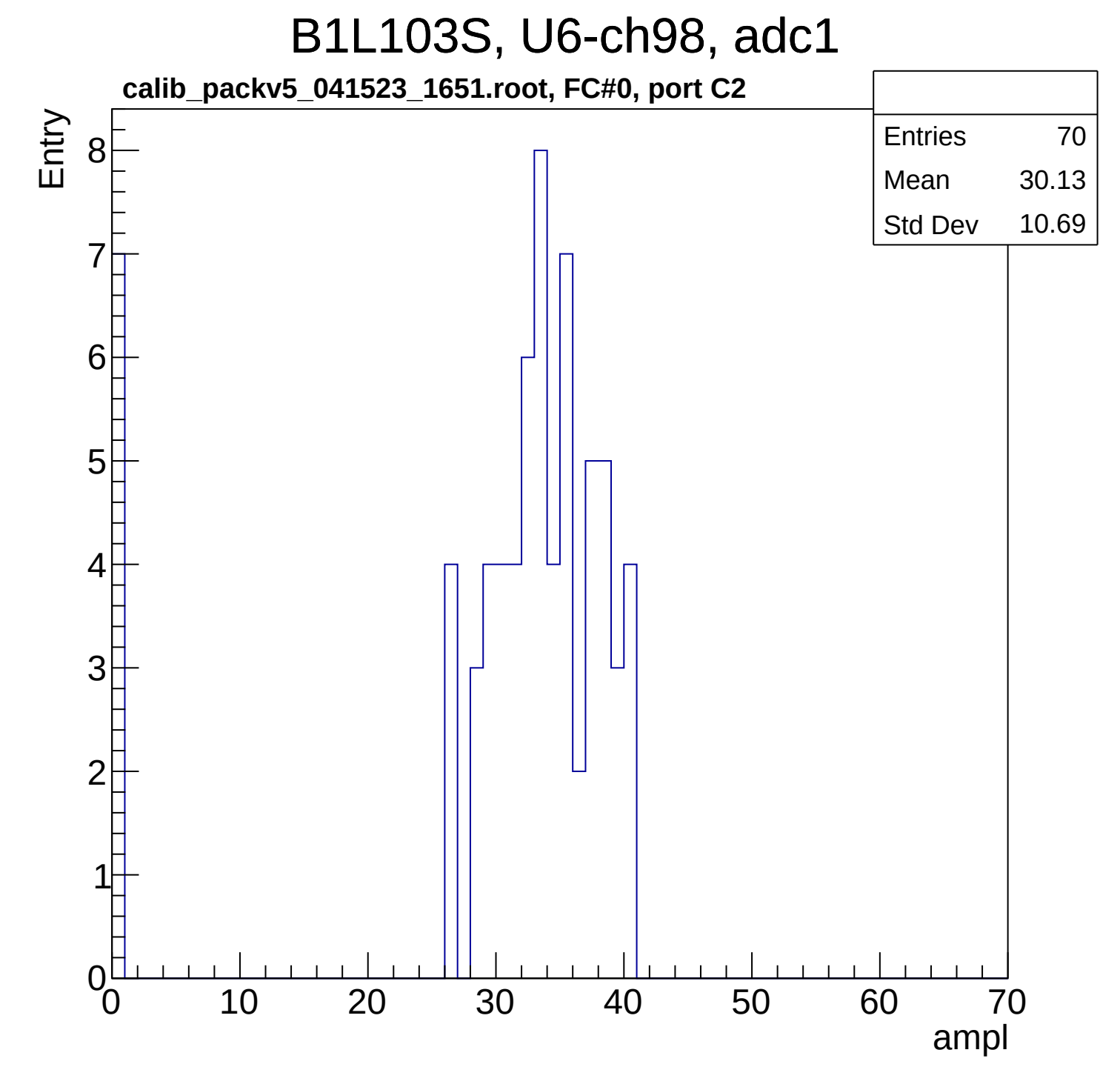
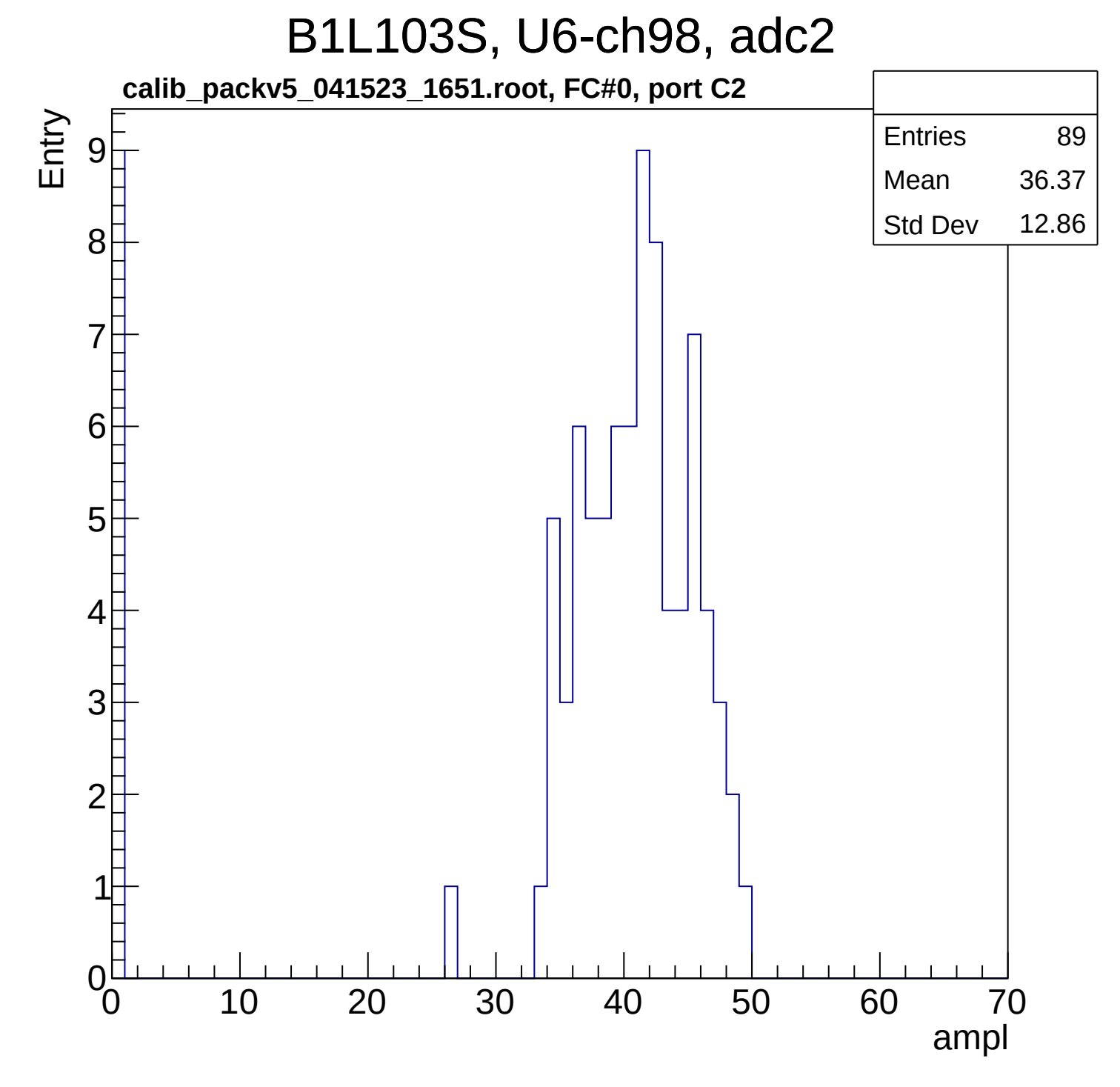
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch98, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 30.13
Std Dev 10.69
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch98, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 36.37
Std Dev 12.86
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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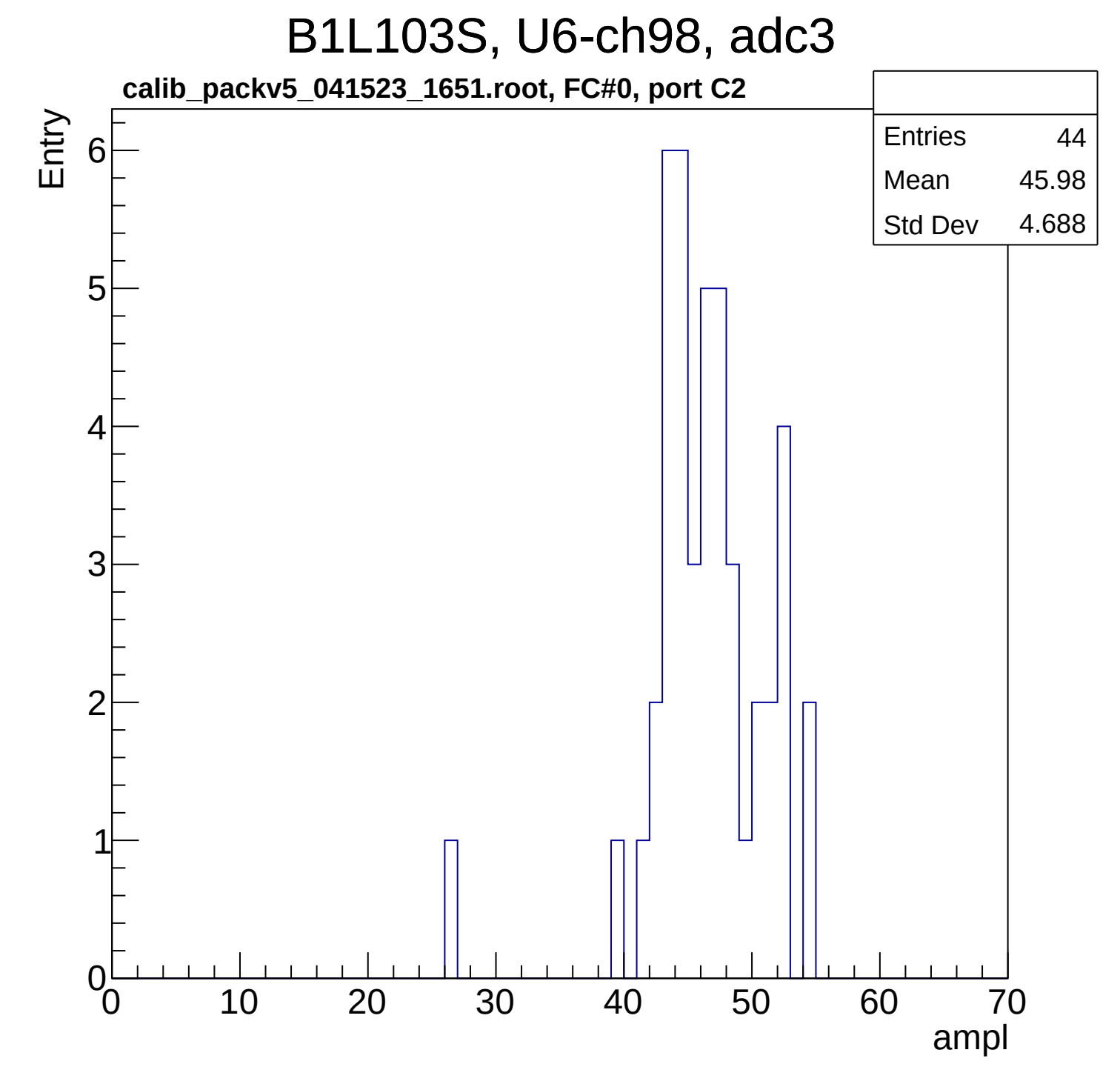
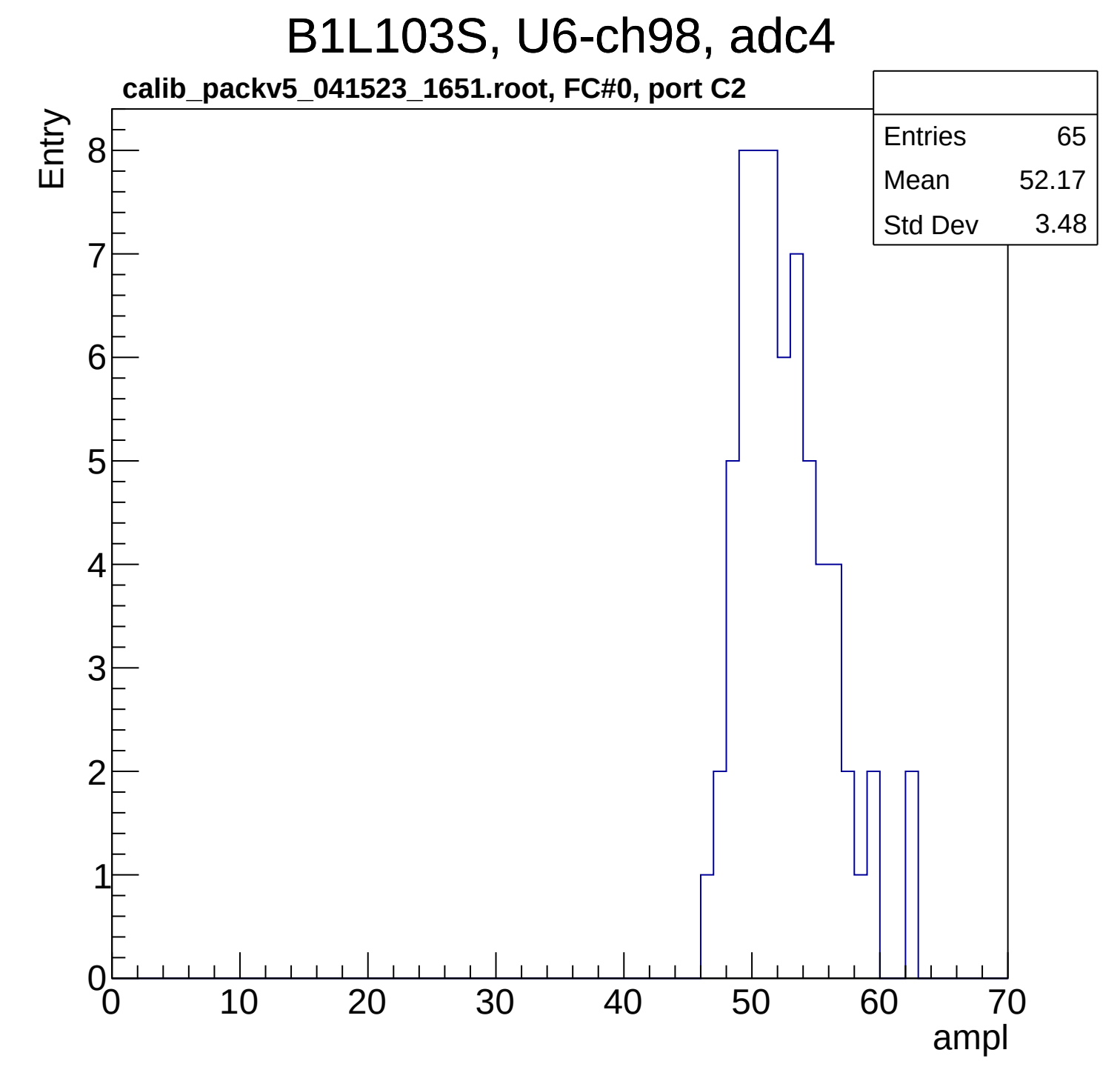

B1L103S, U6-ch98, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 45.98
Std Dev 4.688
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U6-ch98, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 52.17
Std Dev 3.48
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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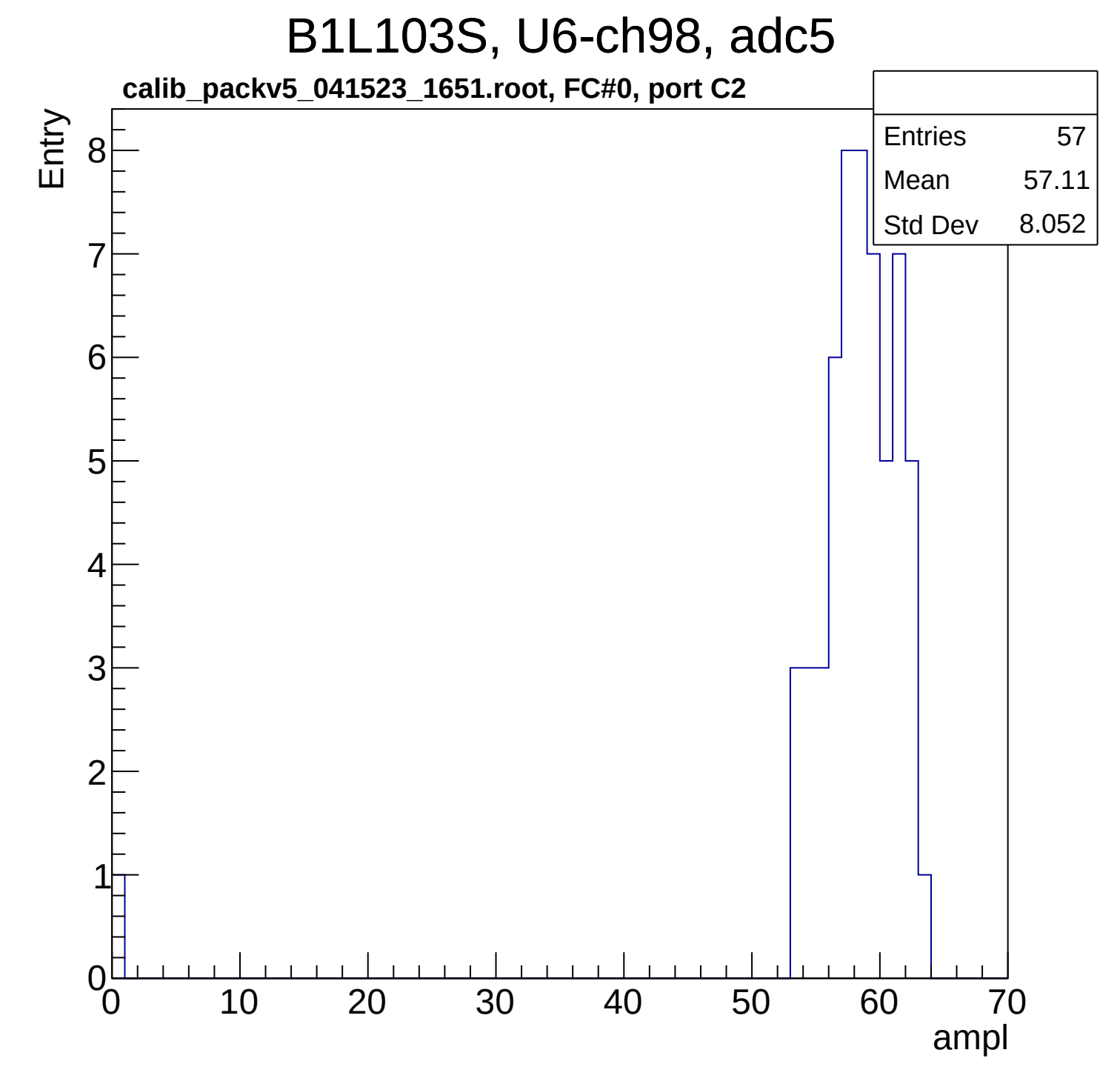
B1L103S, U6-ch98, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 57.11
Std Dev 8.052
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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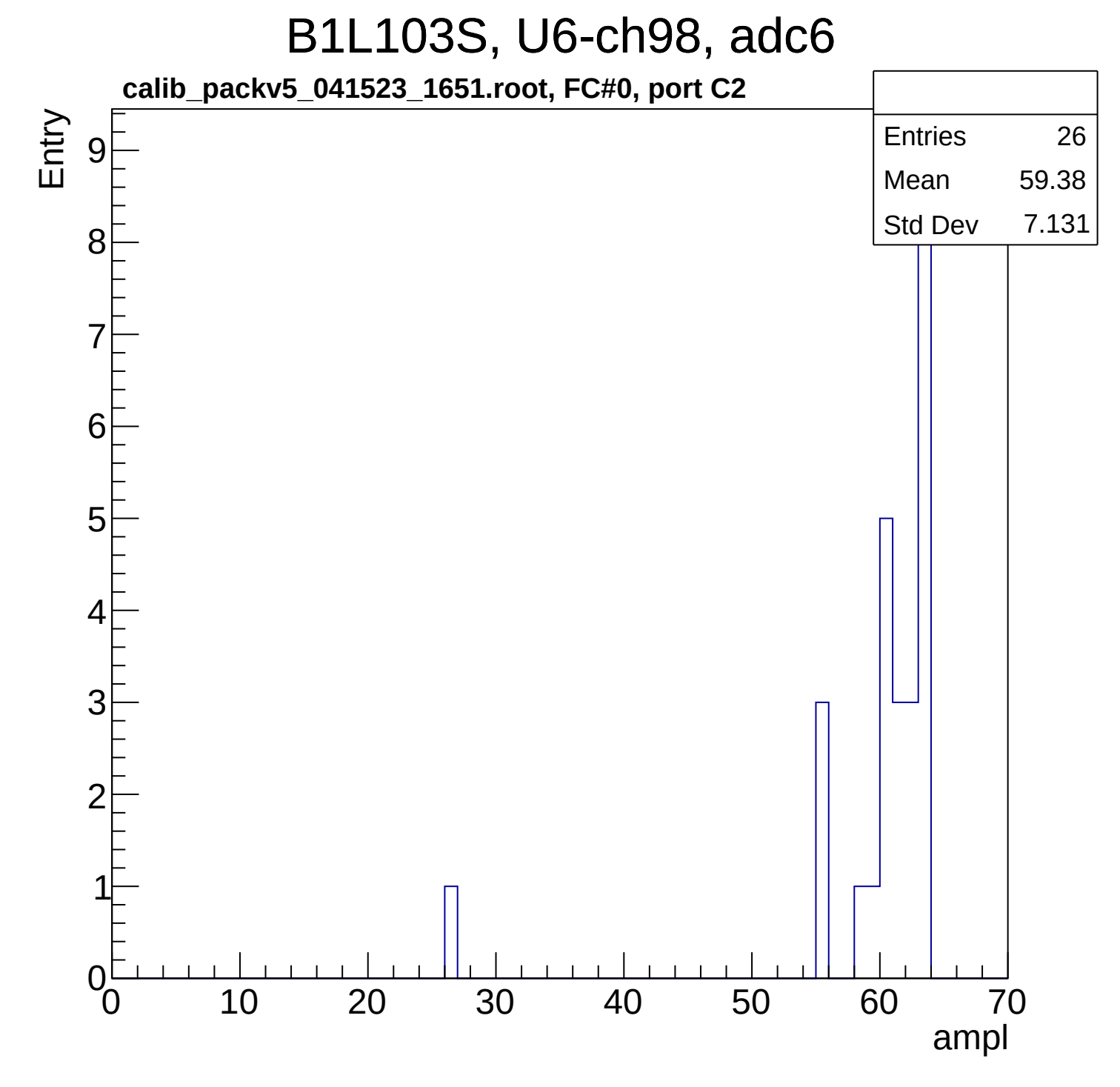
40
50
60
70


B1L103S, U6-ch98, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 59.38
Std Dev 7.131
Entry
ampl
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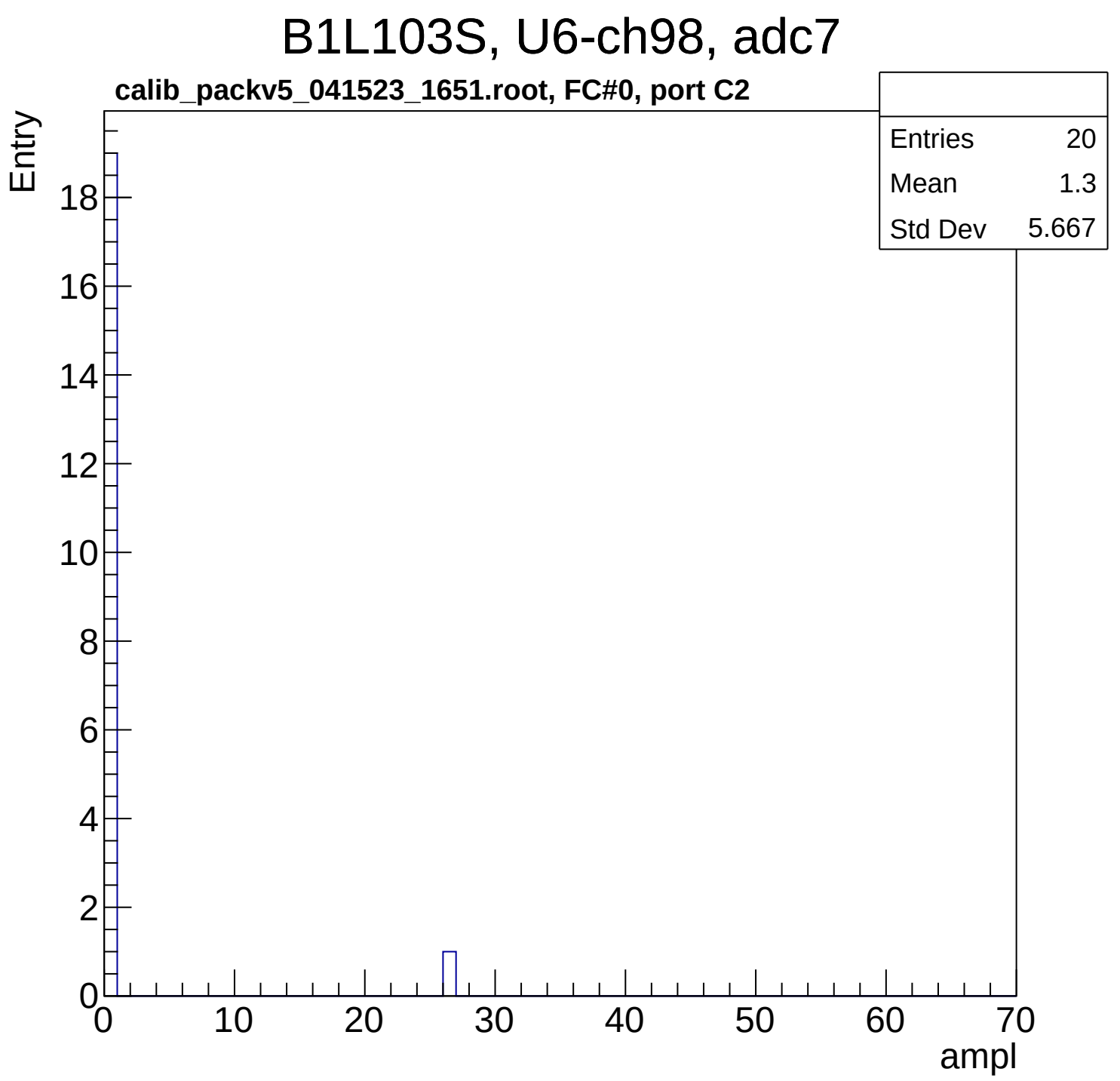
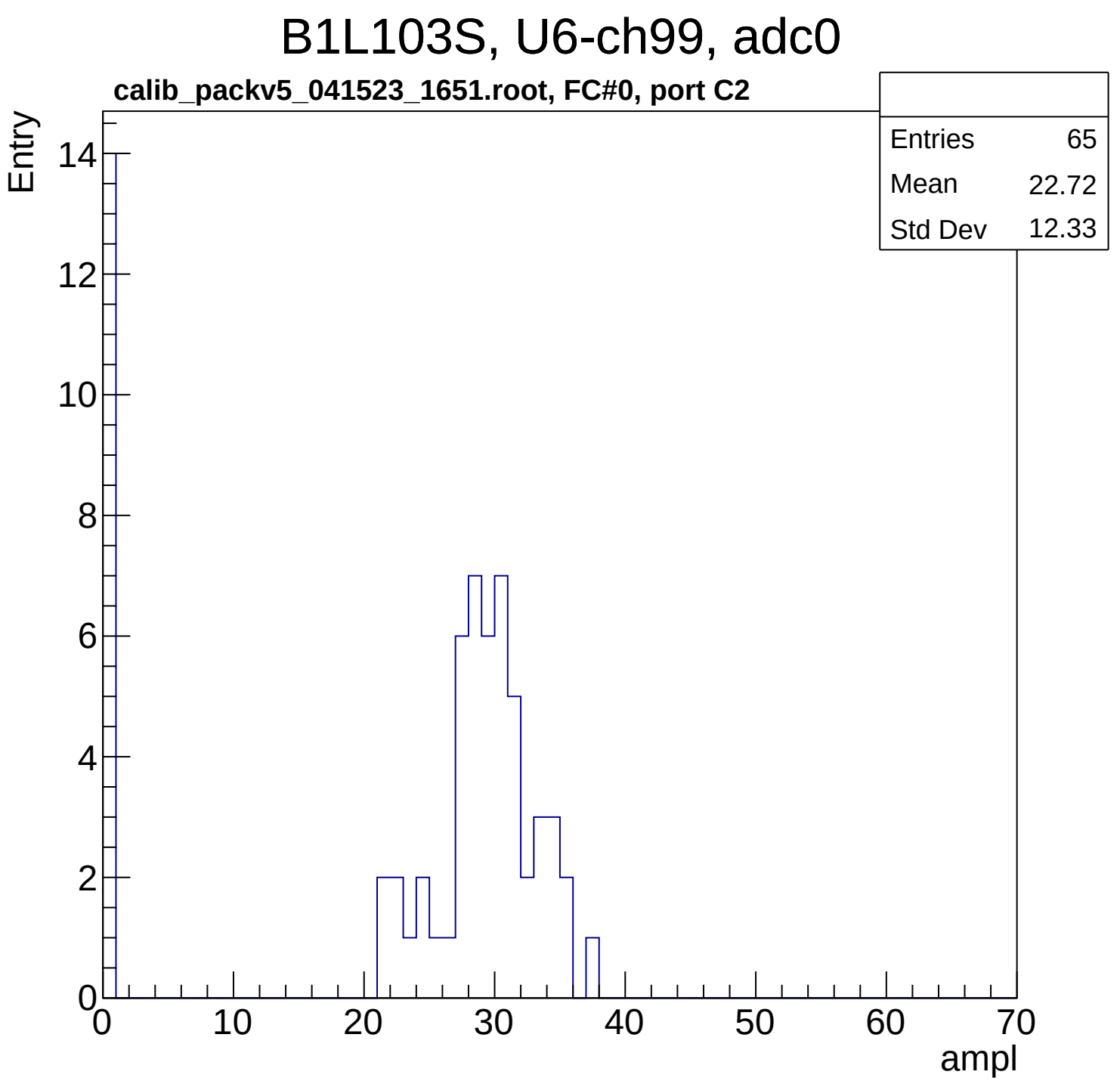
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch98, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 1.3
Std Dev 5.667
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch99, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 22.72
Std Dev 12.33
Entry
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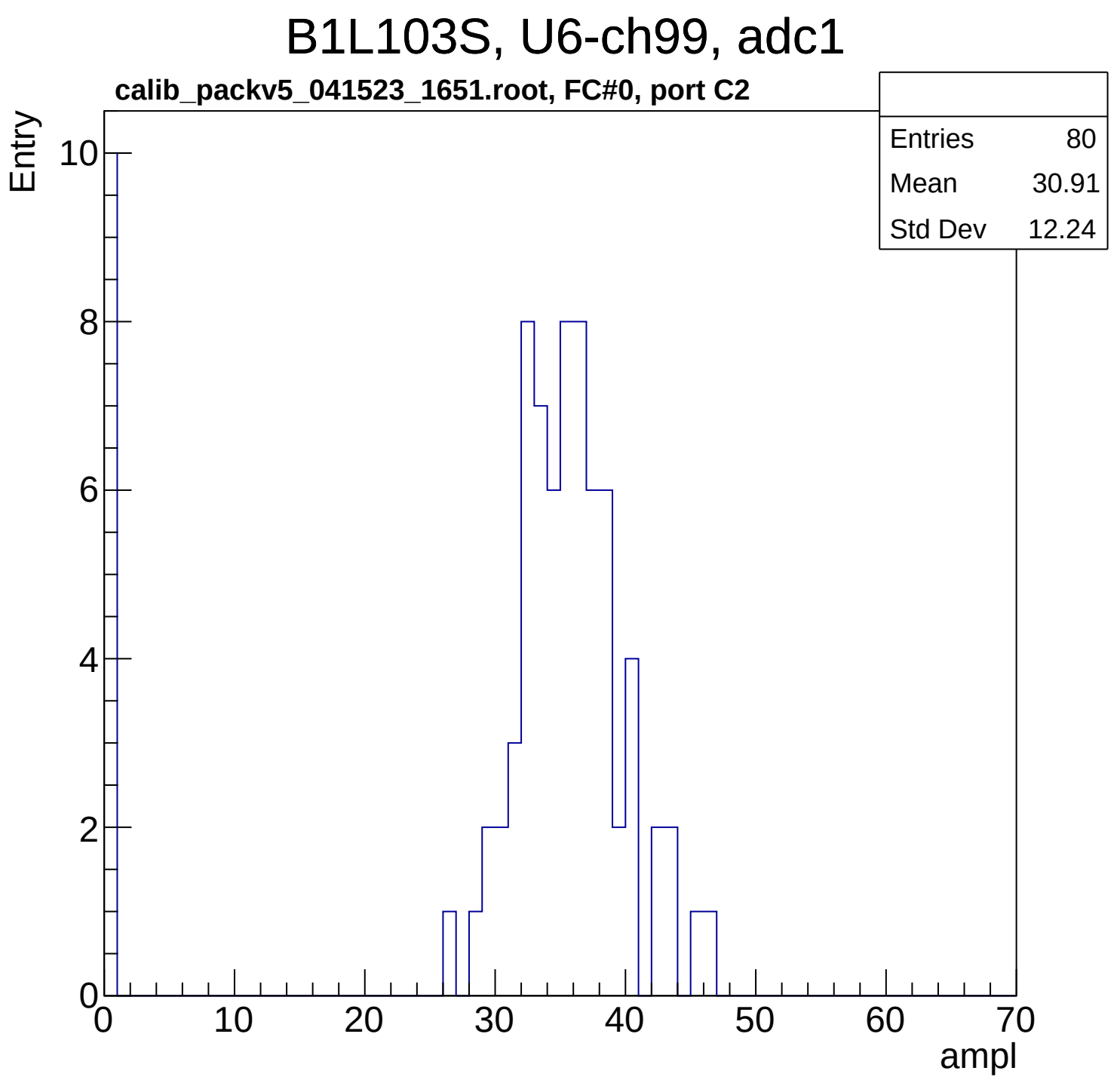
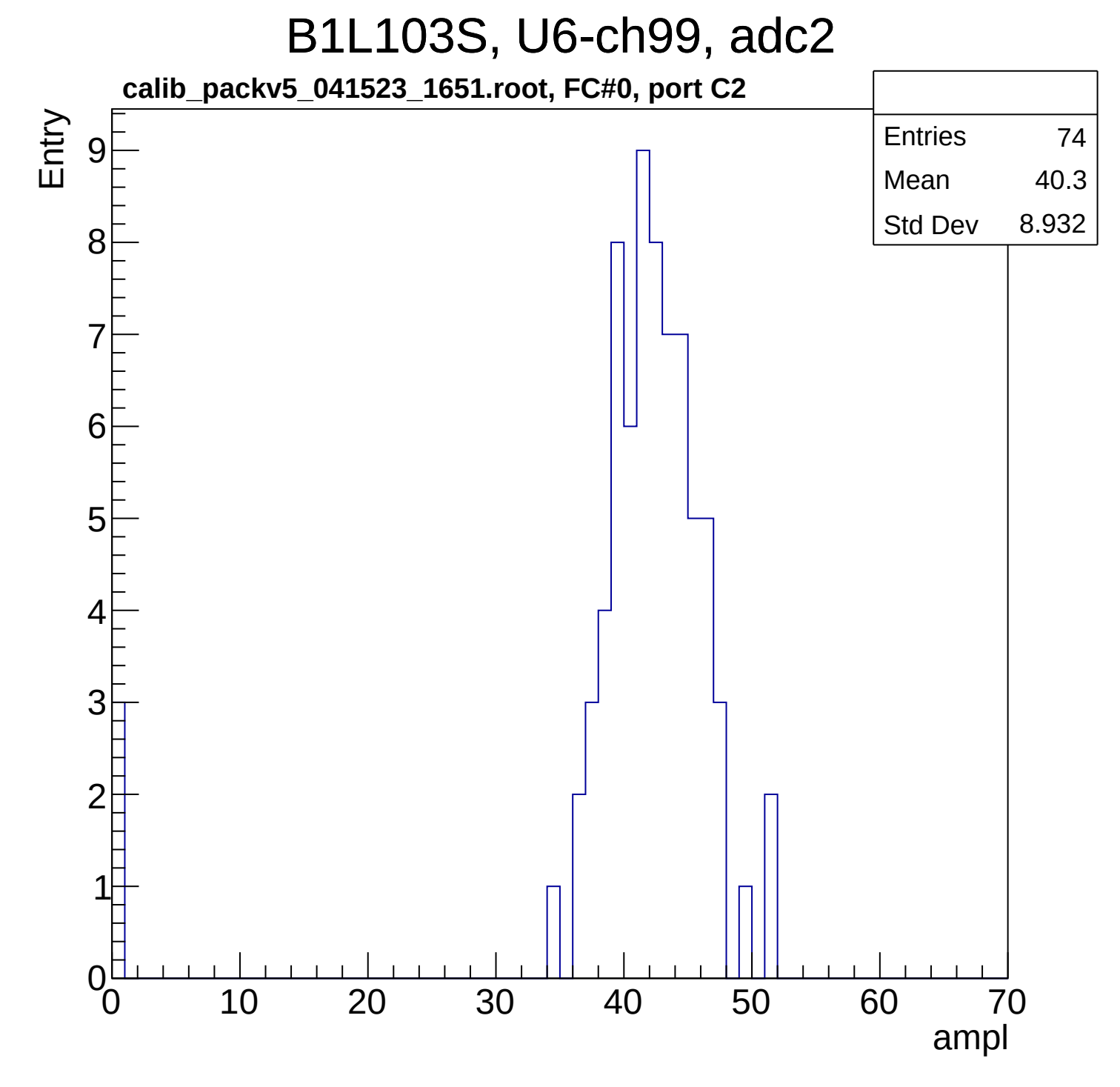
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch99, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 30.91
Std Dev 12.24
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch99, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 40.3
Std Dev 8.932
Entry
ampl
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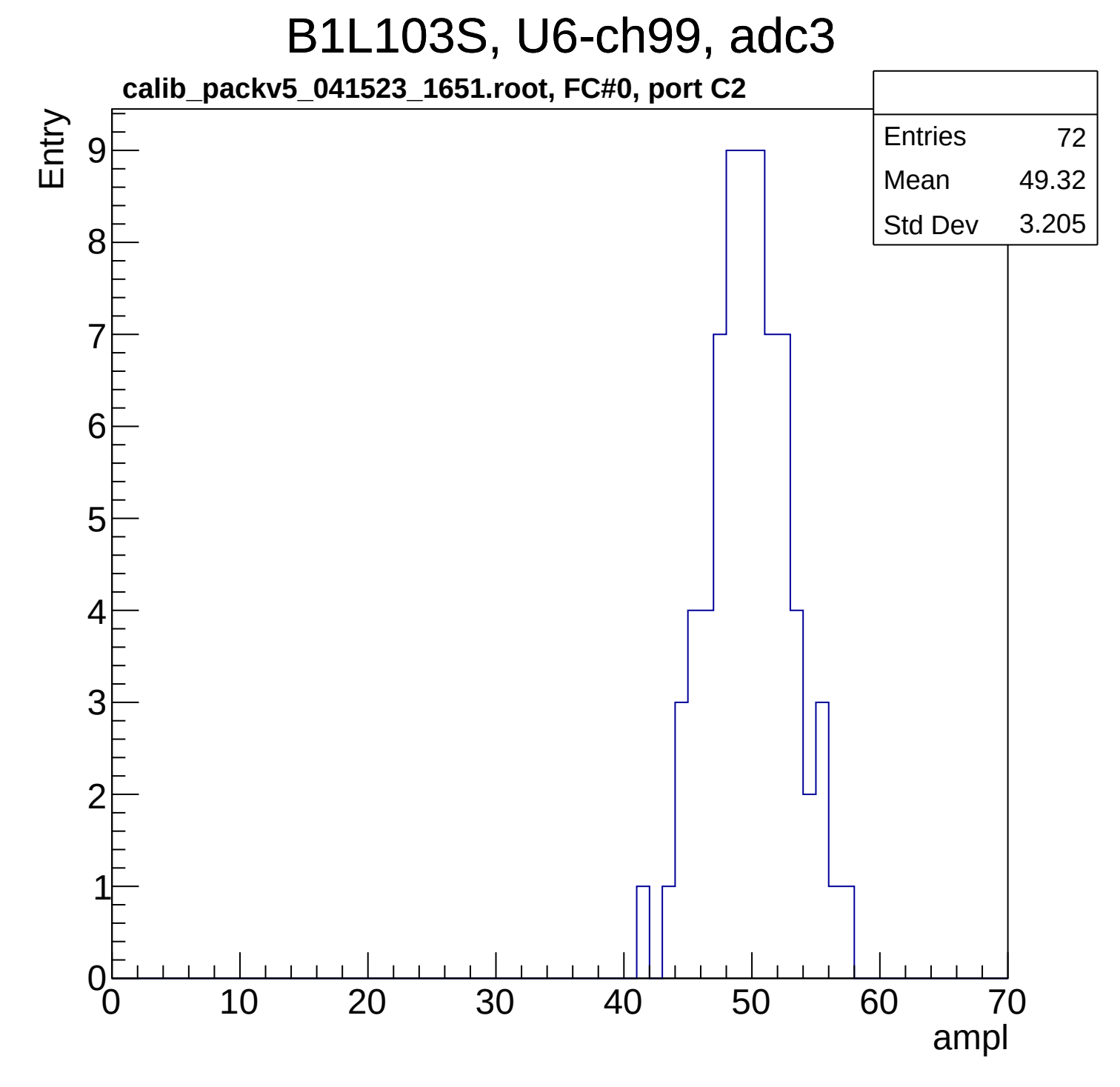
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch99, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 49.32
Std Dev 3.205
Entry
ampl
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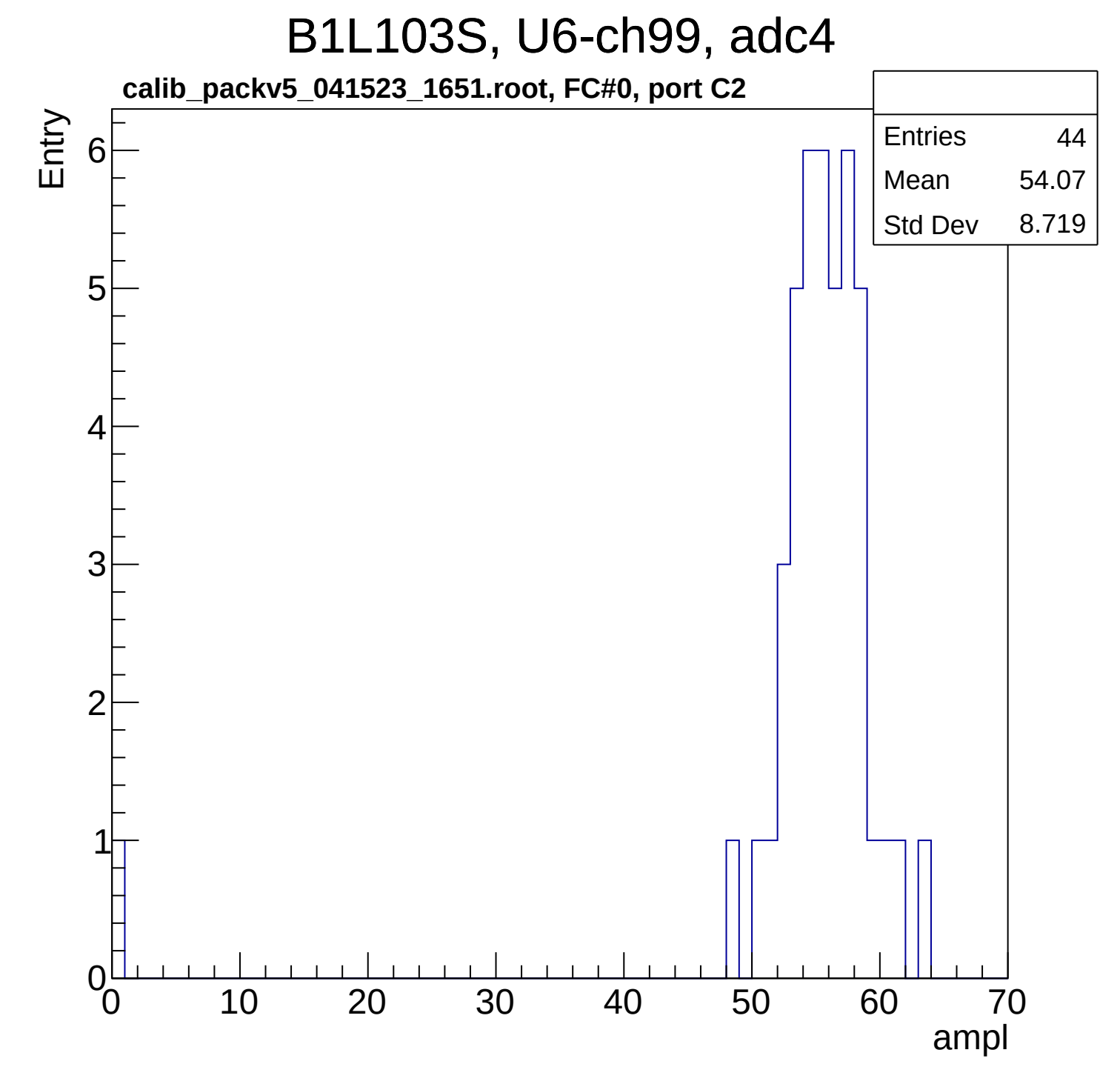
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch99, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 54.07
Std Dev 8.719
Entry
0
1
2
3
4
5
6
0
10
20
30
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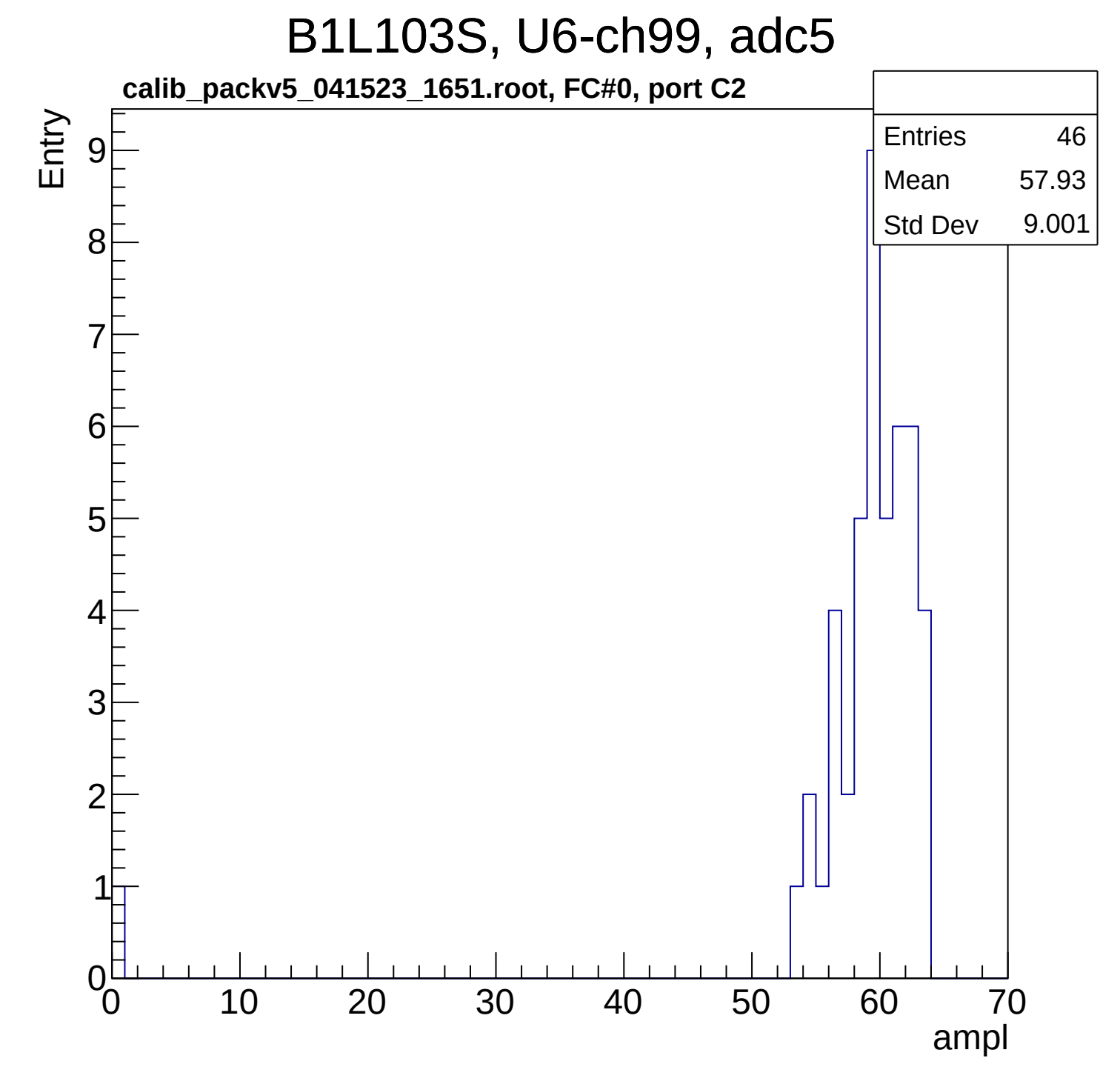
50
60
70
ampl


B1L103S, U6-ch99, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 57.93
Std Dev 9.001
Entry
ampl
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3
4
5
6
7
8
9
0
10
20
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40
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60
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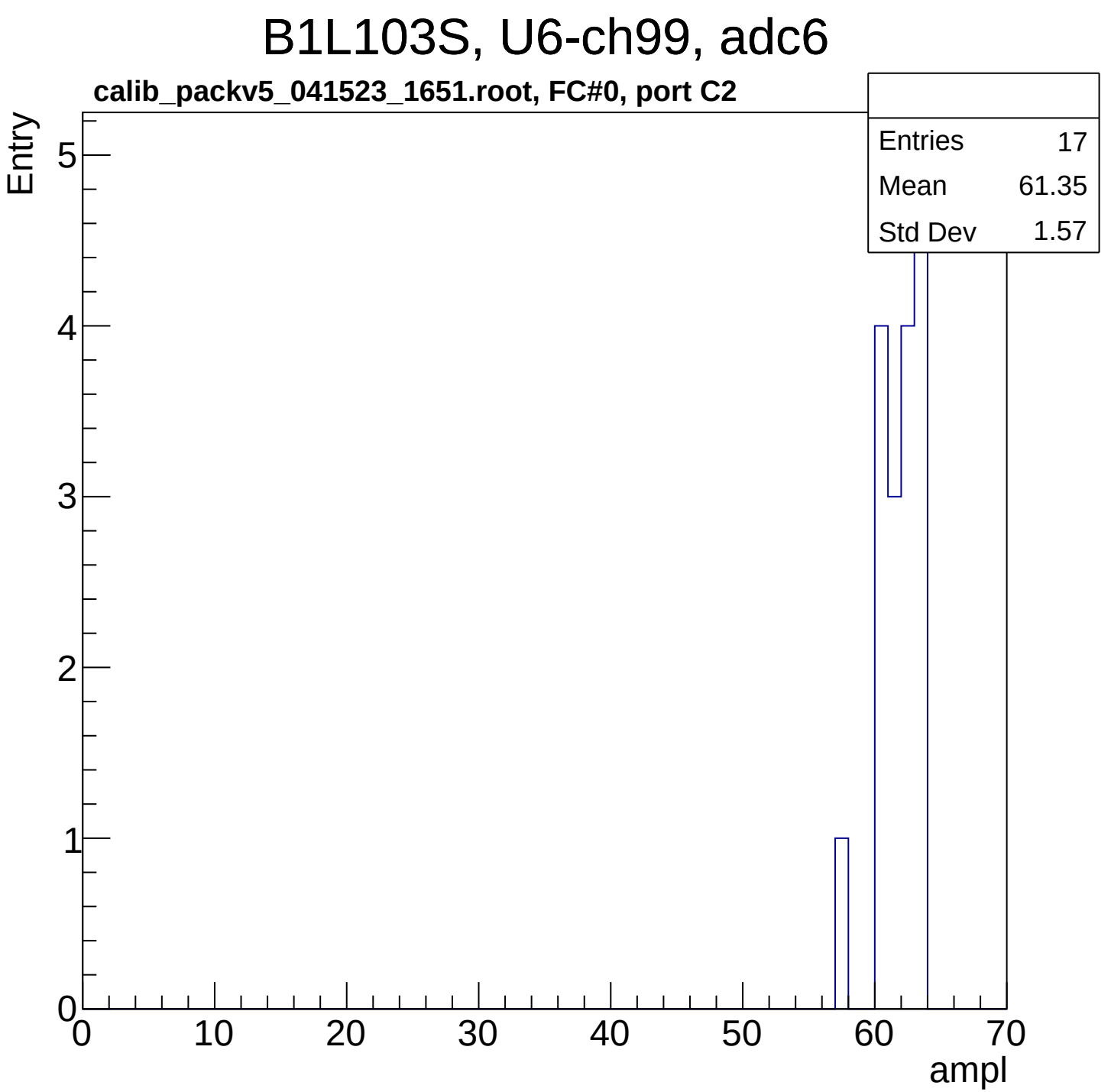
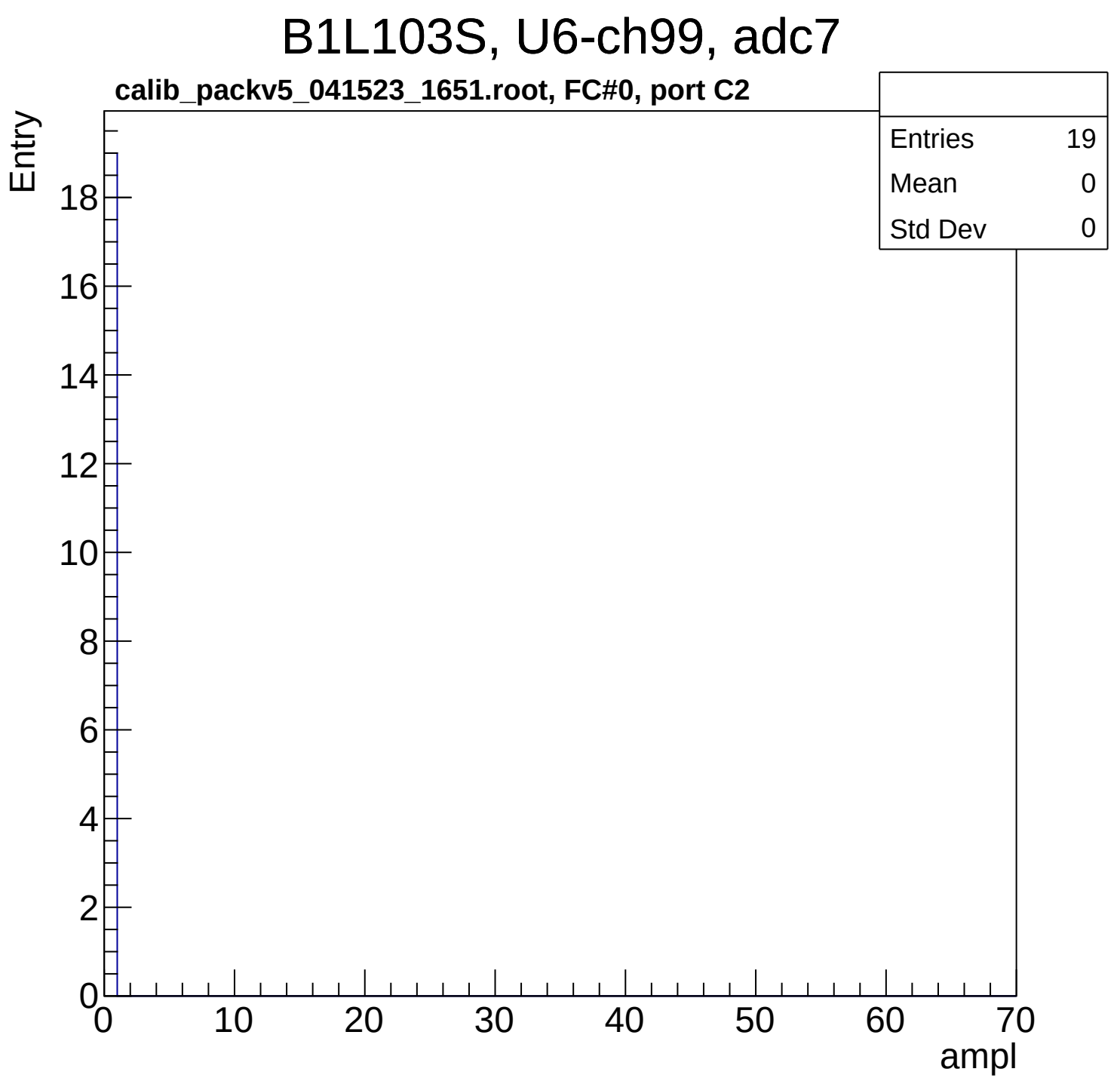

B1L103S, U6-ch99, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 61.35
Std Dev 1.57
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch99, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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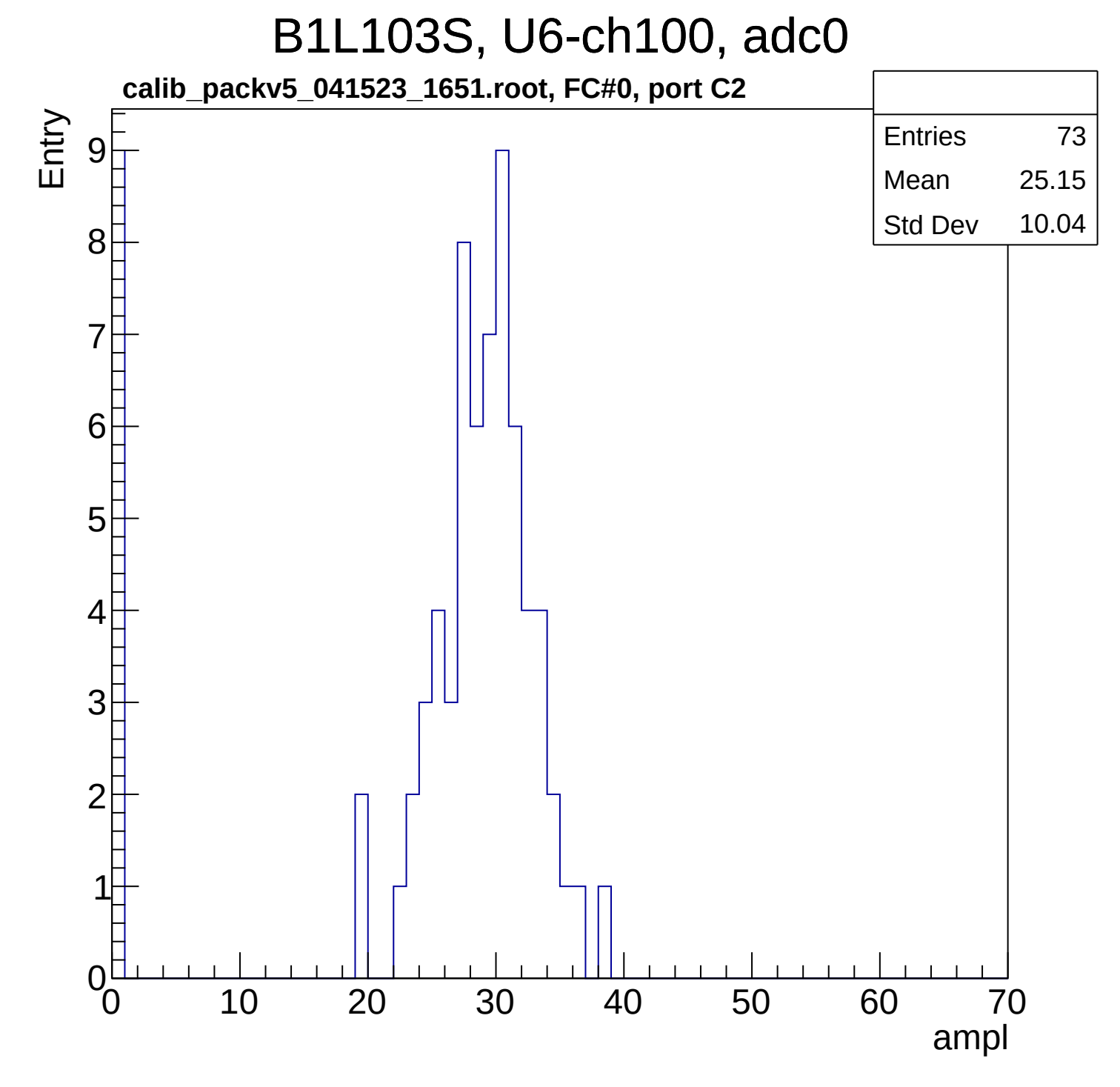
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch100, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 25.15
Std Dev 10.04
Entry
ampl
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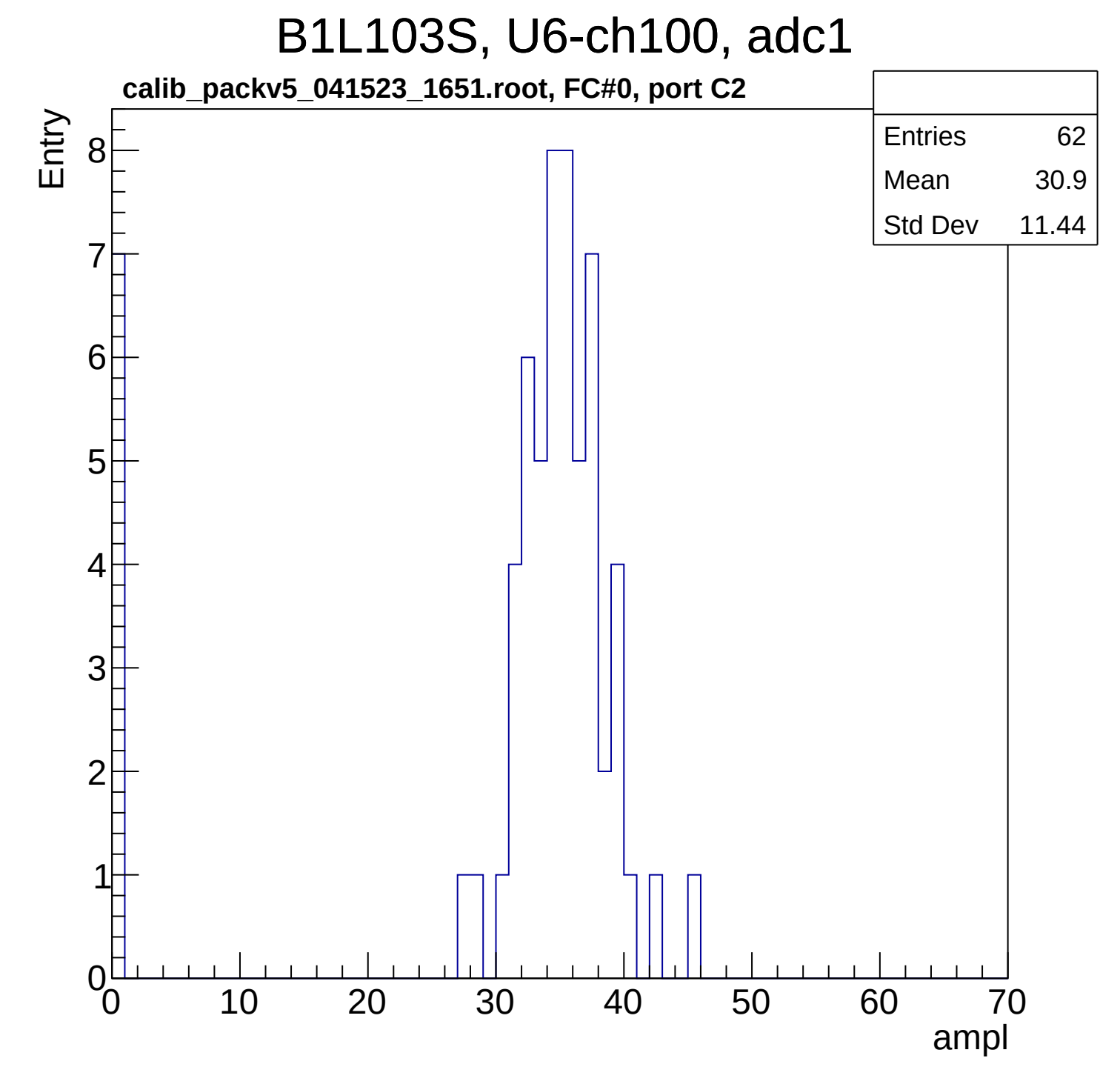
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch100, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 30.9
Std Dev 11.44
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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60
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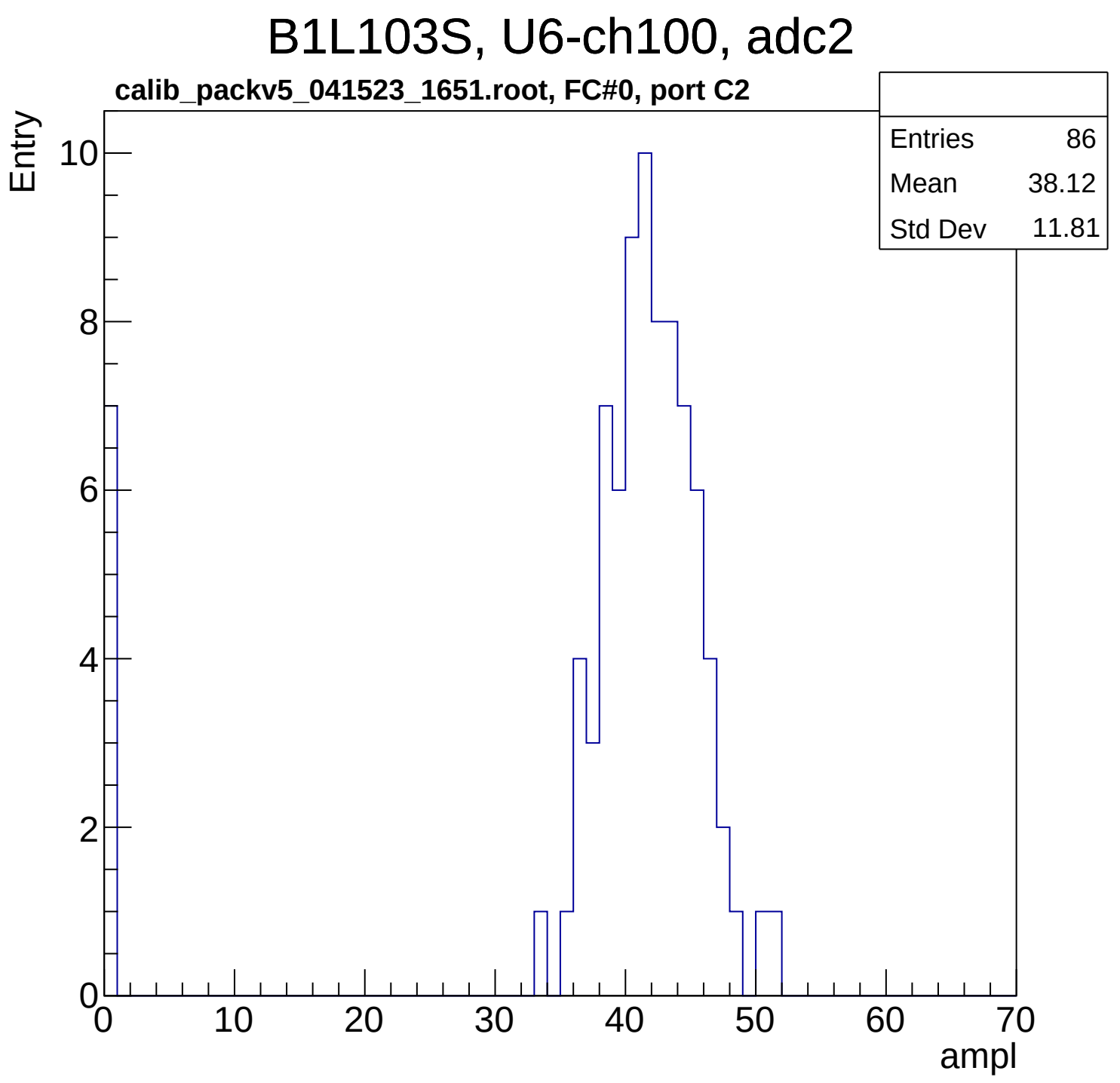
B1L103S, U6-ch100, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 38.12
Std Dev 11.81
Entry
ampl
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4
6
8
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0
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60
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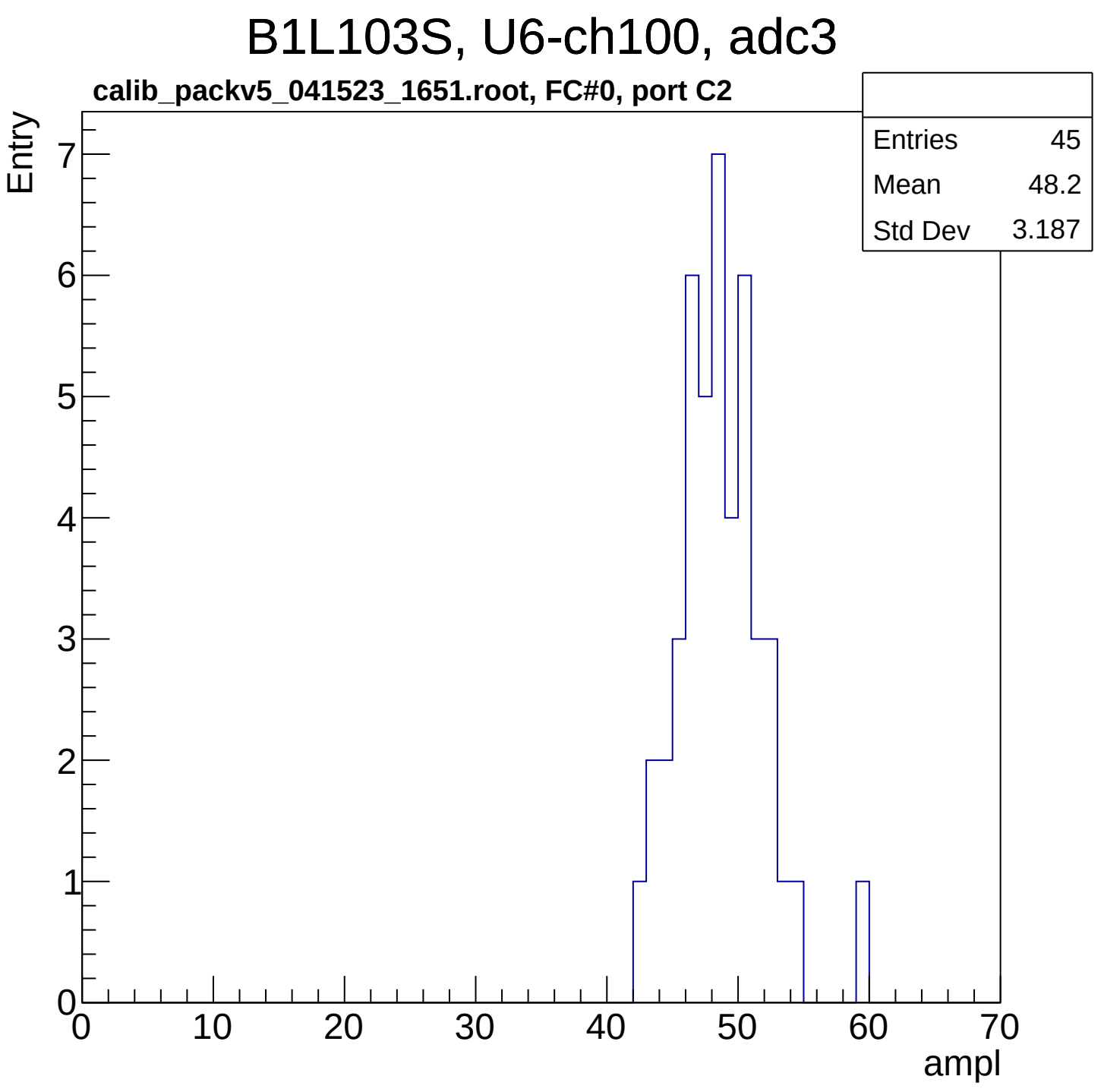
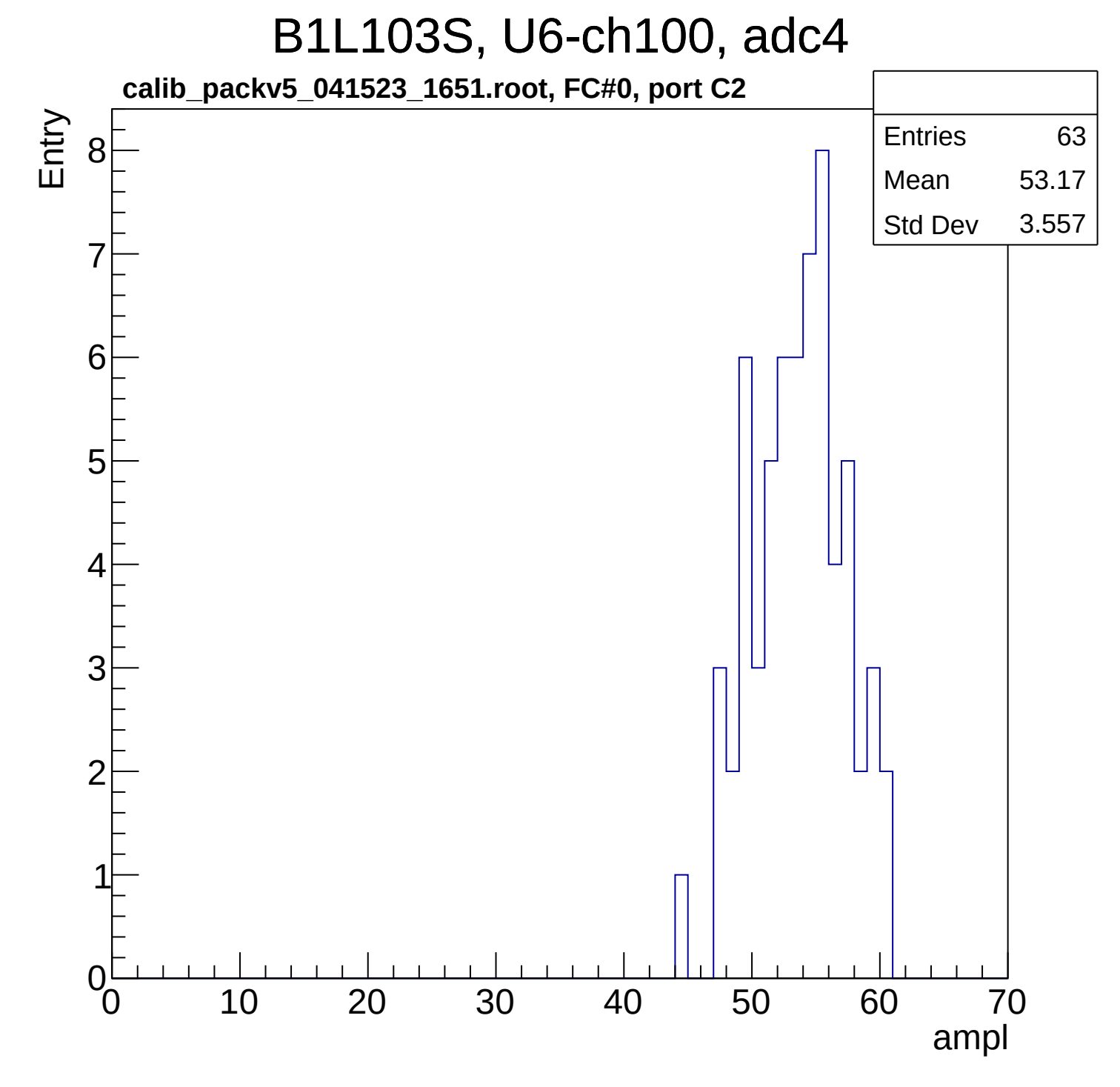

B1L103S, U6-ch100, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 48.2
Std Dev 3.187
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U6-ch100, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 53.17
Std Dev 3.557
Entry
ampl
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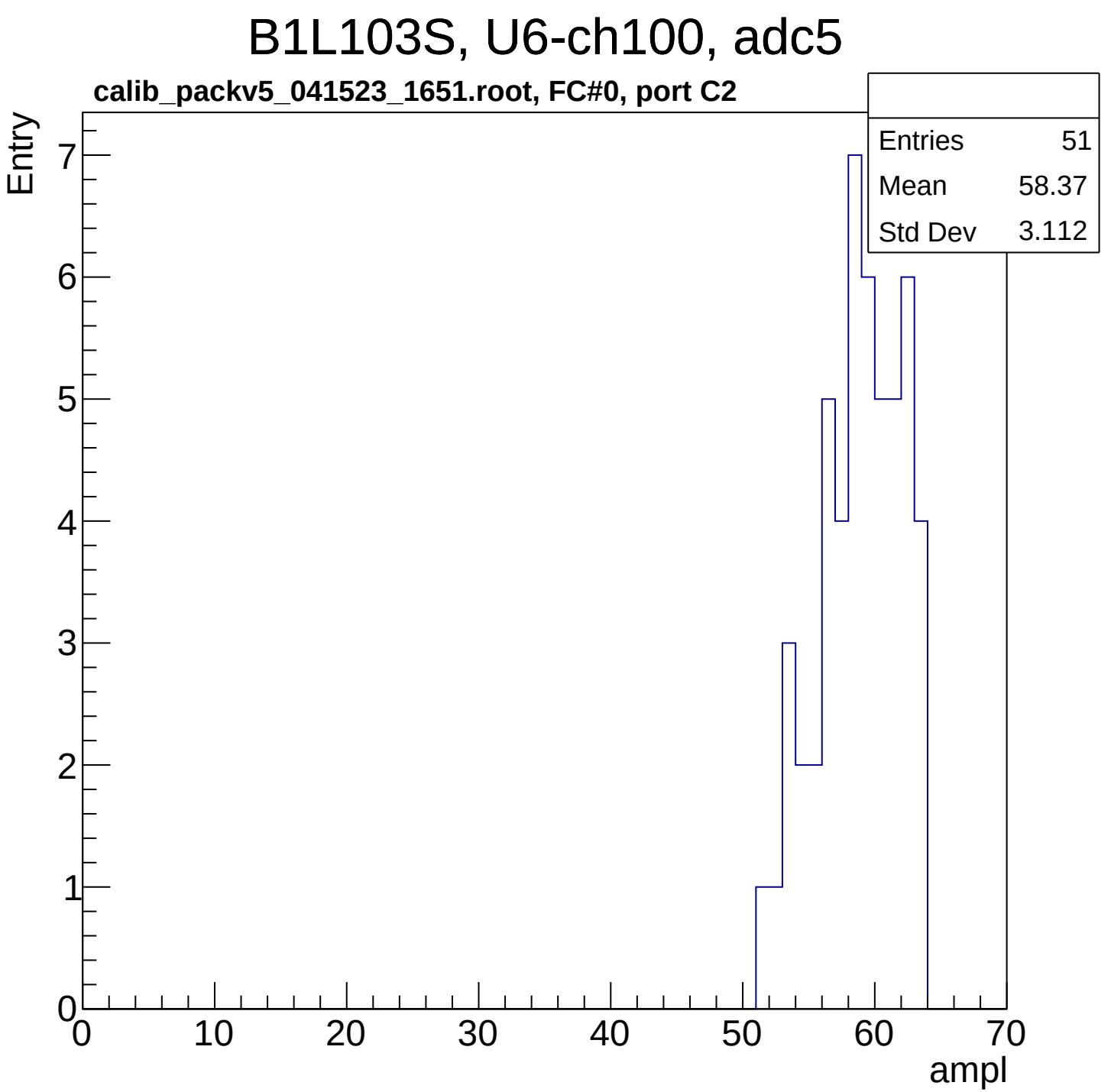
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch100, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 58.37
Std Dev 3.112
Entry
ampl
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1
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3
4
5
6
7
0
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50
60
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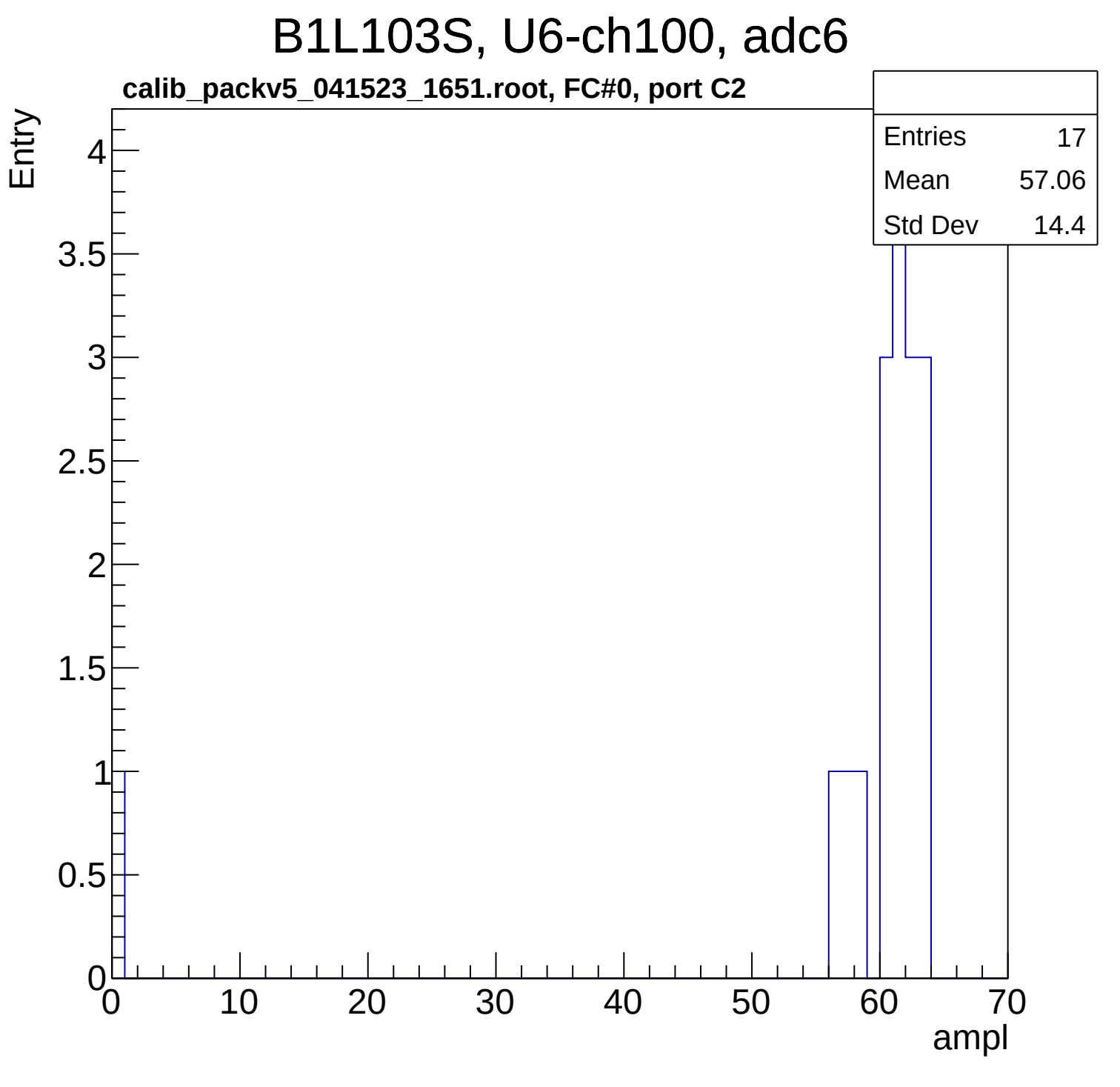
B1L103S, U6-ch100, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 57.06
Std Dev 14.4
Entry
ampl
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0.5
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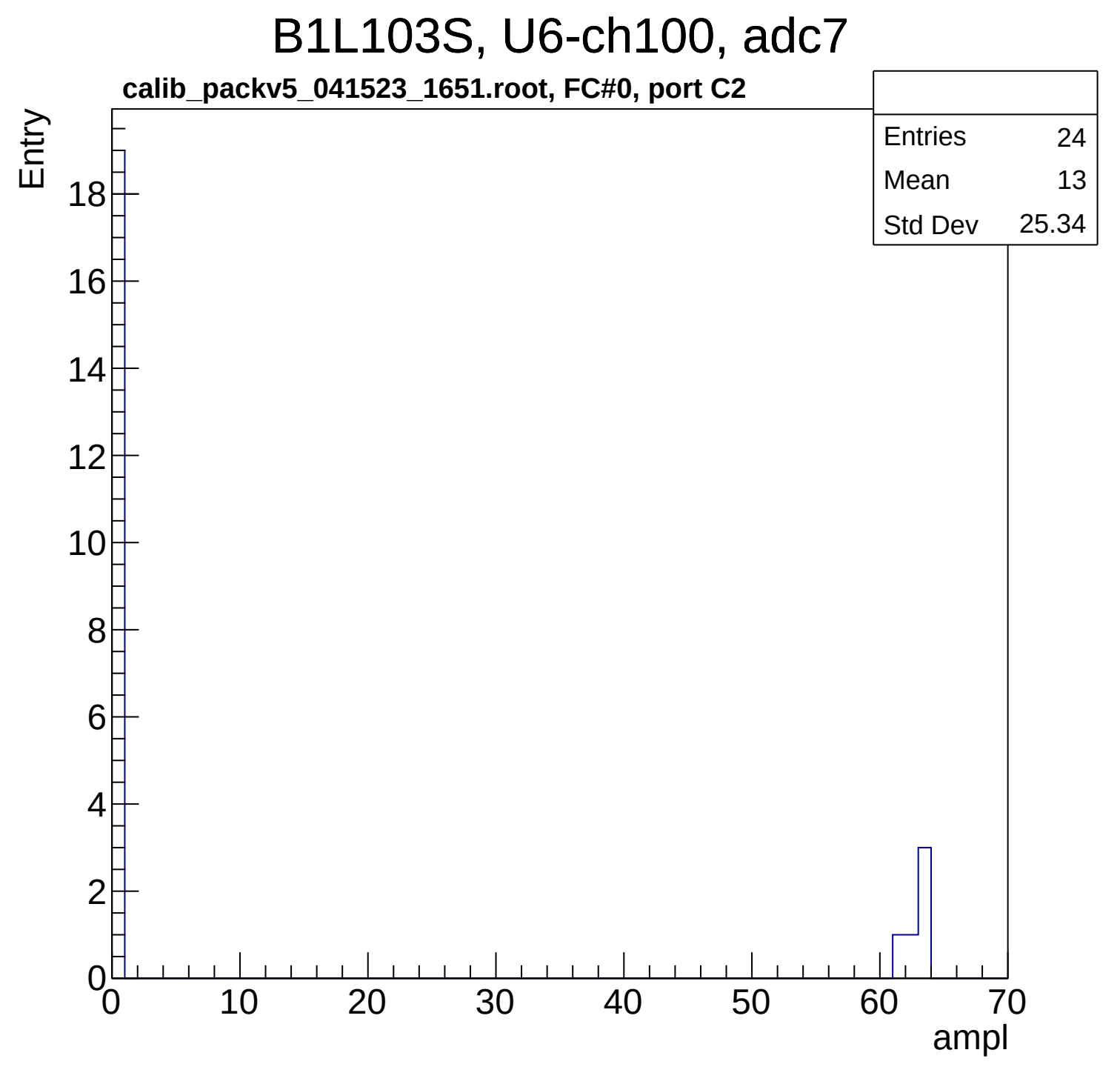
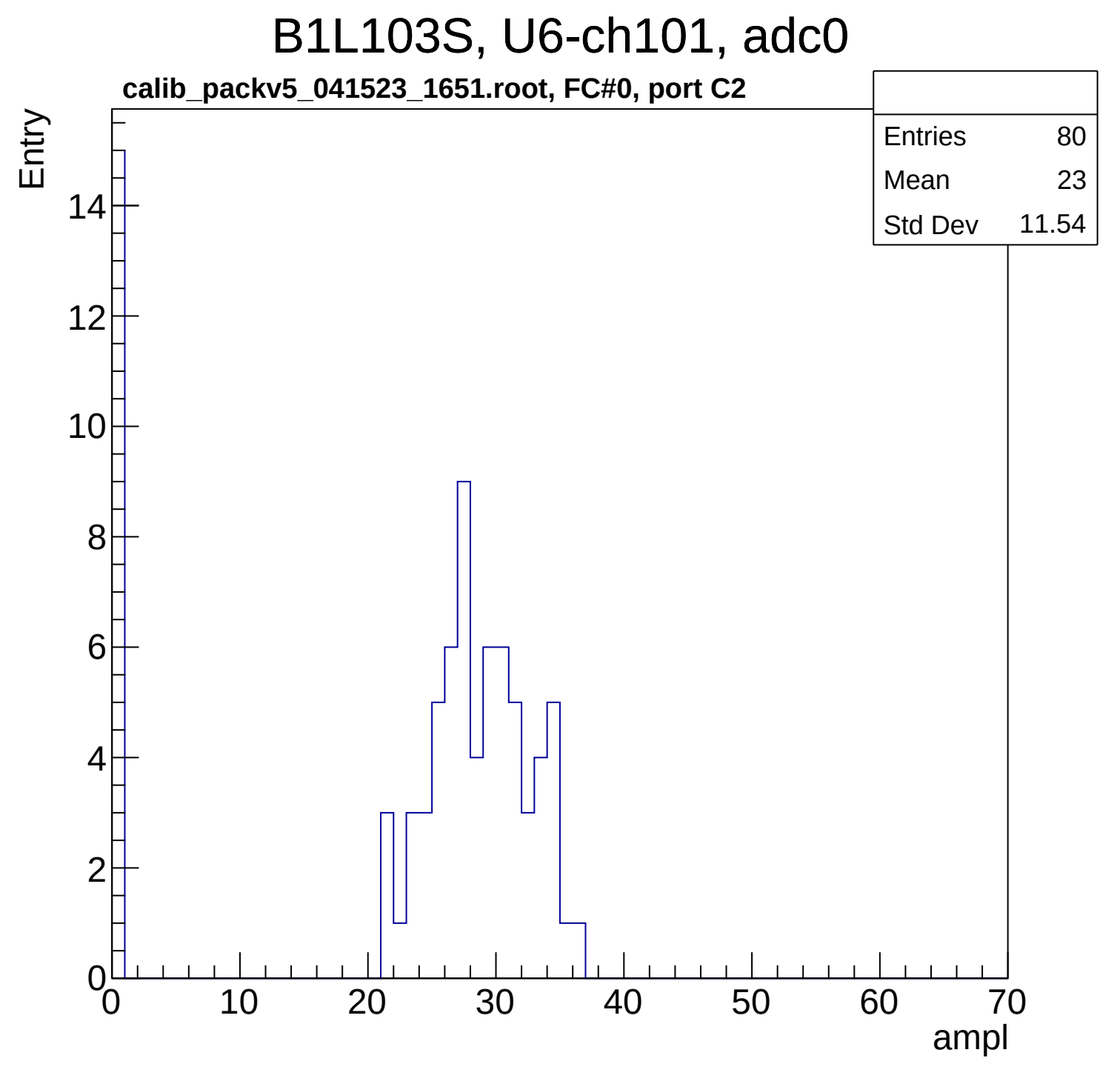
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U6-ch100, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 13
Std Dev 25.34
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch101, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 23
Std Dev 11.54
Entry
0
2
4
6
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10
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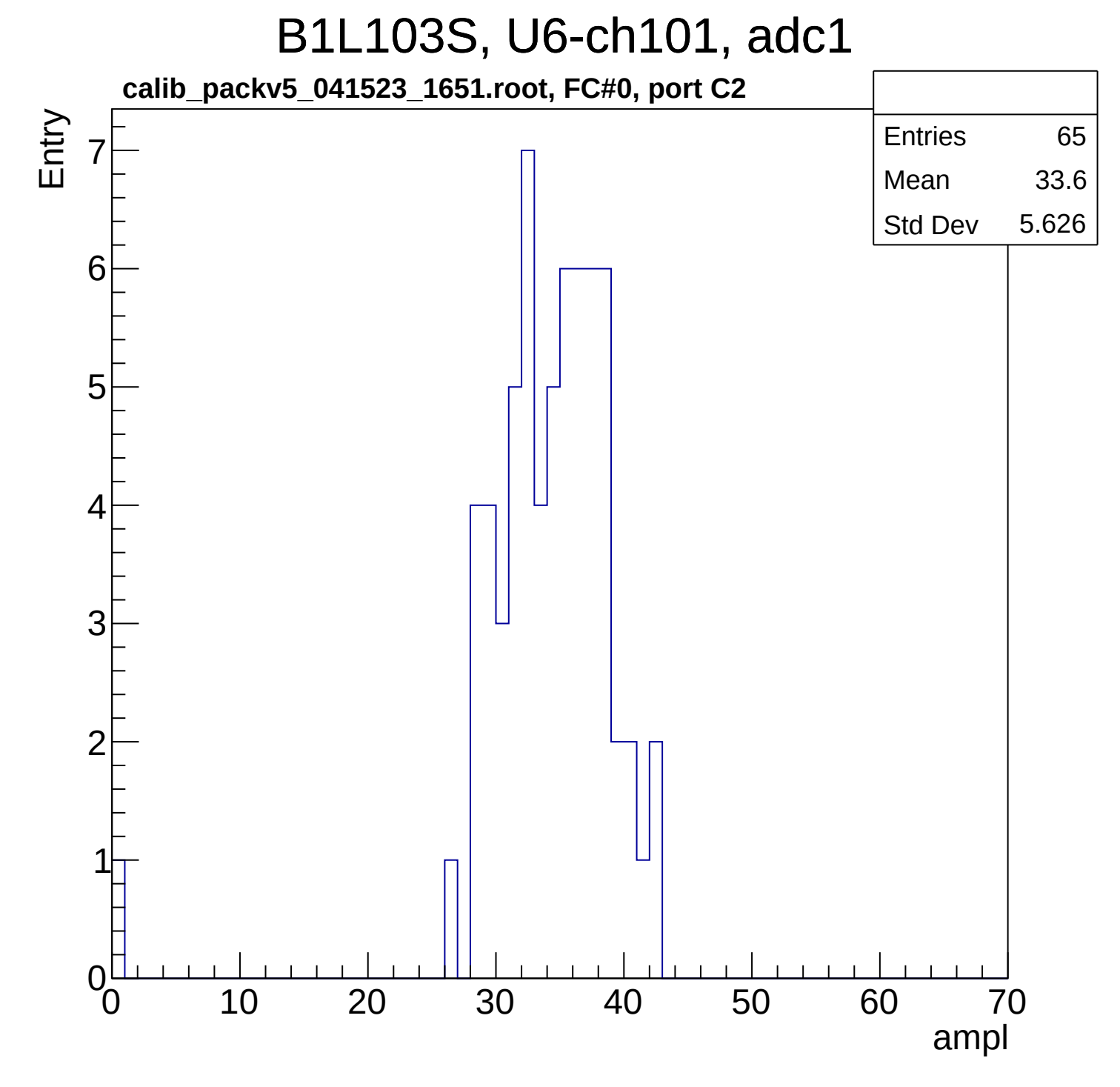
ampl


B1L103S, U6-ch101, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 33.6
Std Dev 5.626
Entry
ampl
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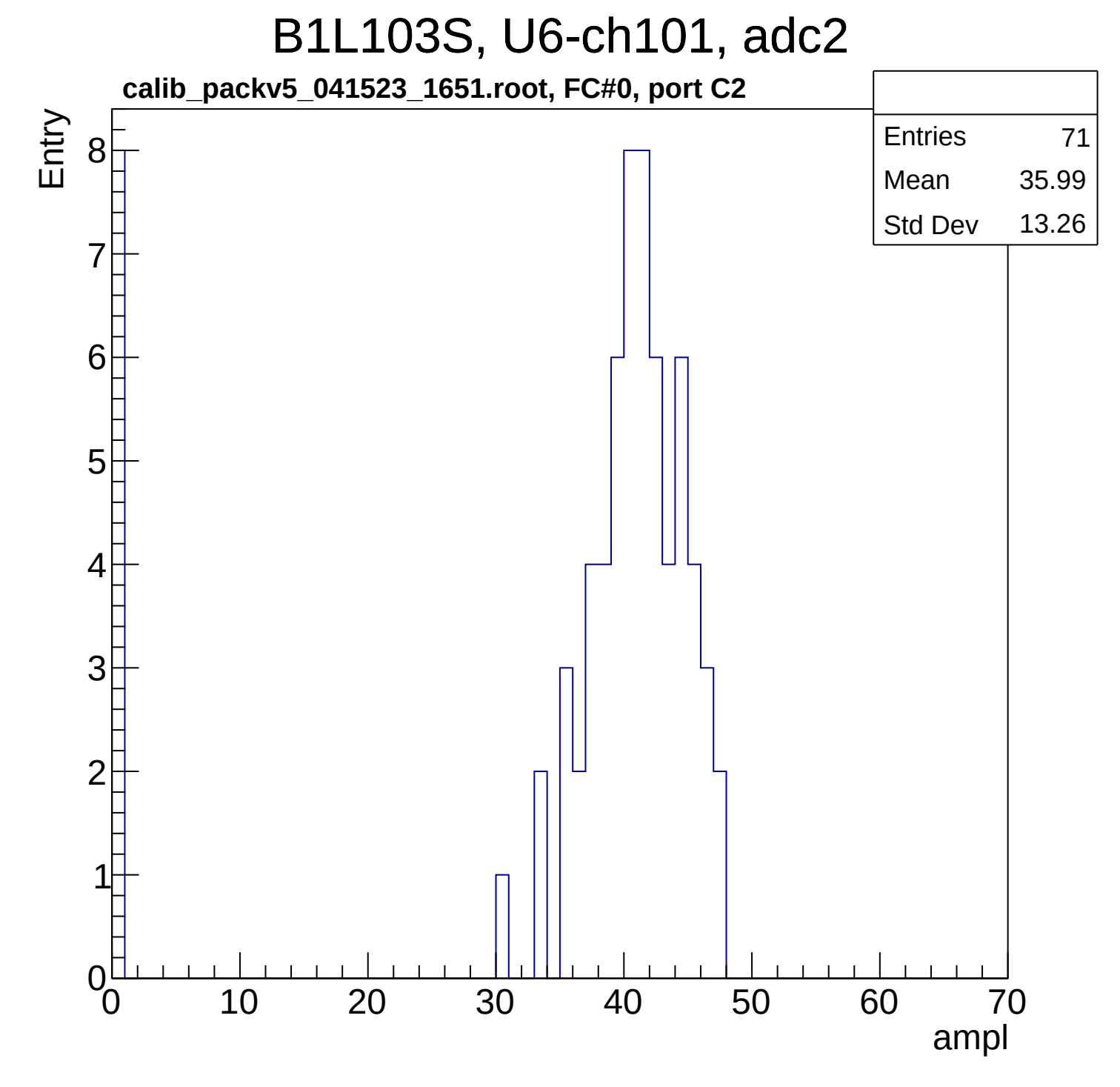
B1L103S, U6-ch101, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 35.99
Std Dev 13.26
Entry
ampl
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0
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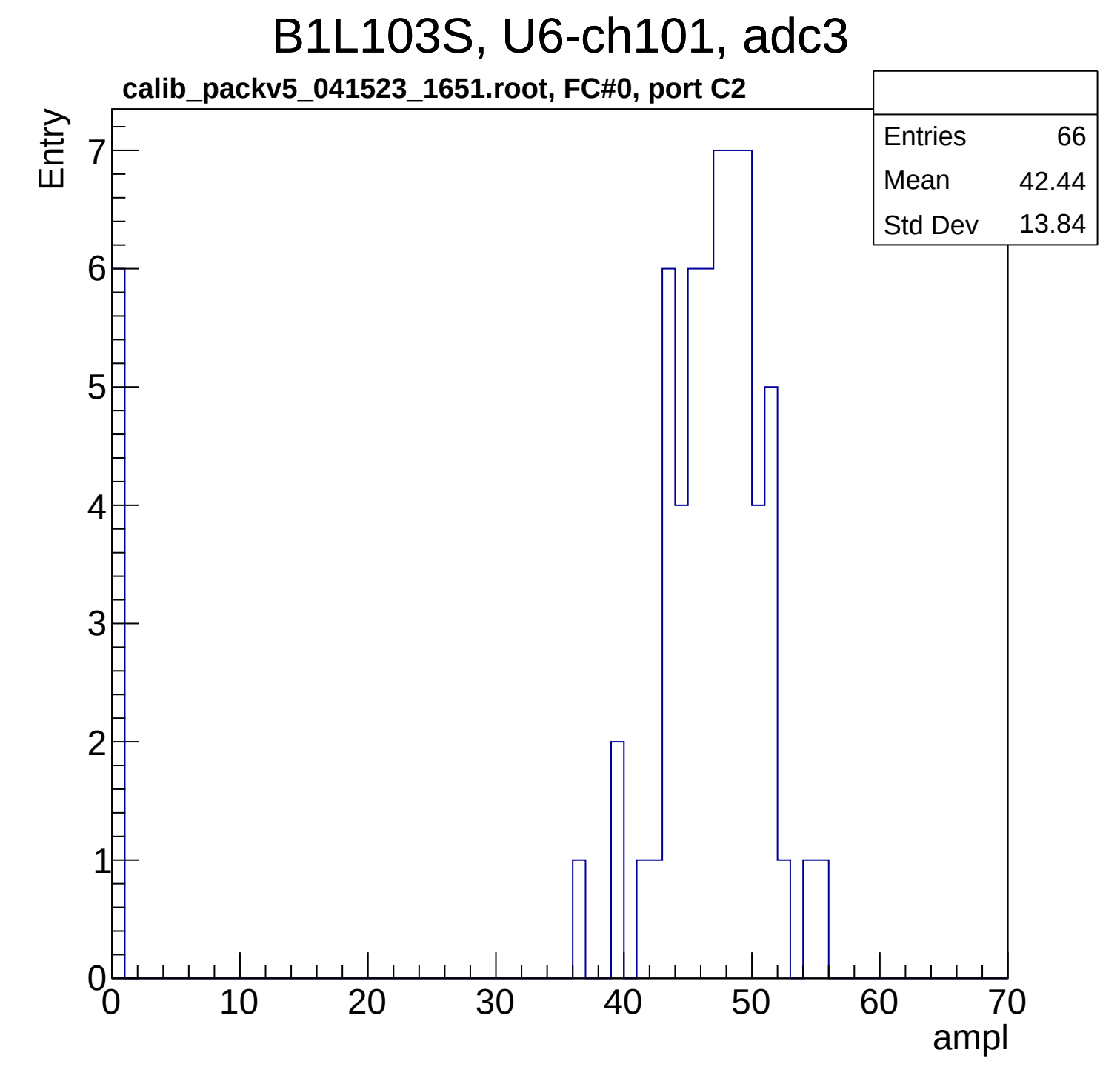
B1L103S, U6-ch101, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 42.44
Std Dev 13.84
Entry
ampl
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1
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4
5
6
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0
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40
50
60
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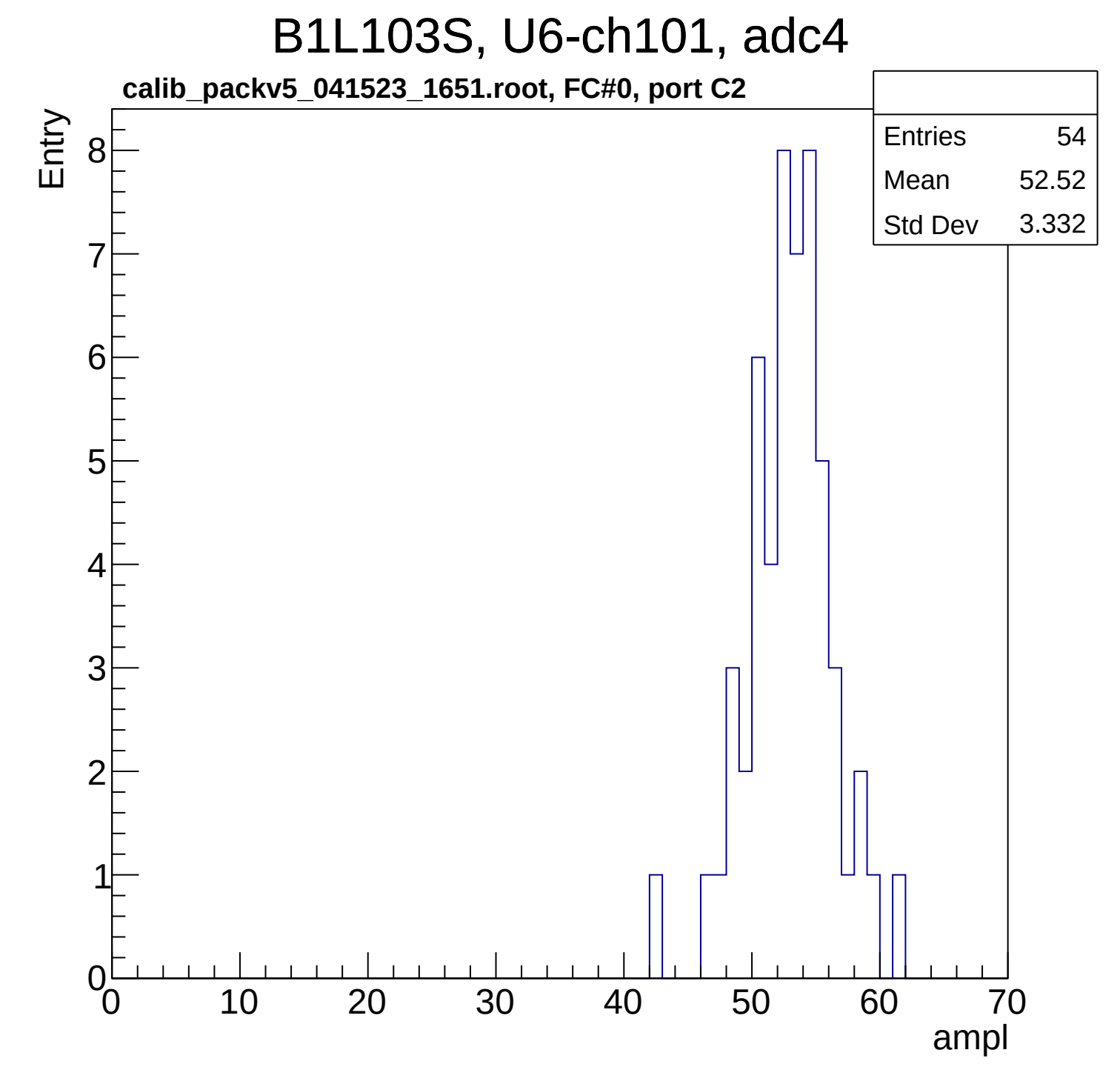
B1L103S, U6-ch101, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 52.52
Std Dev 3.332
Entry
ampl
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5
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0
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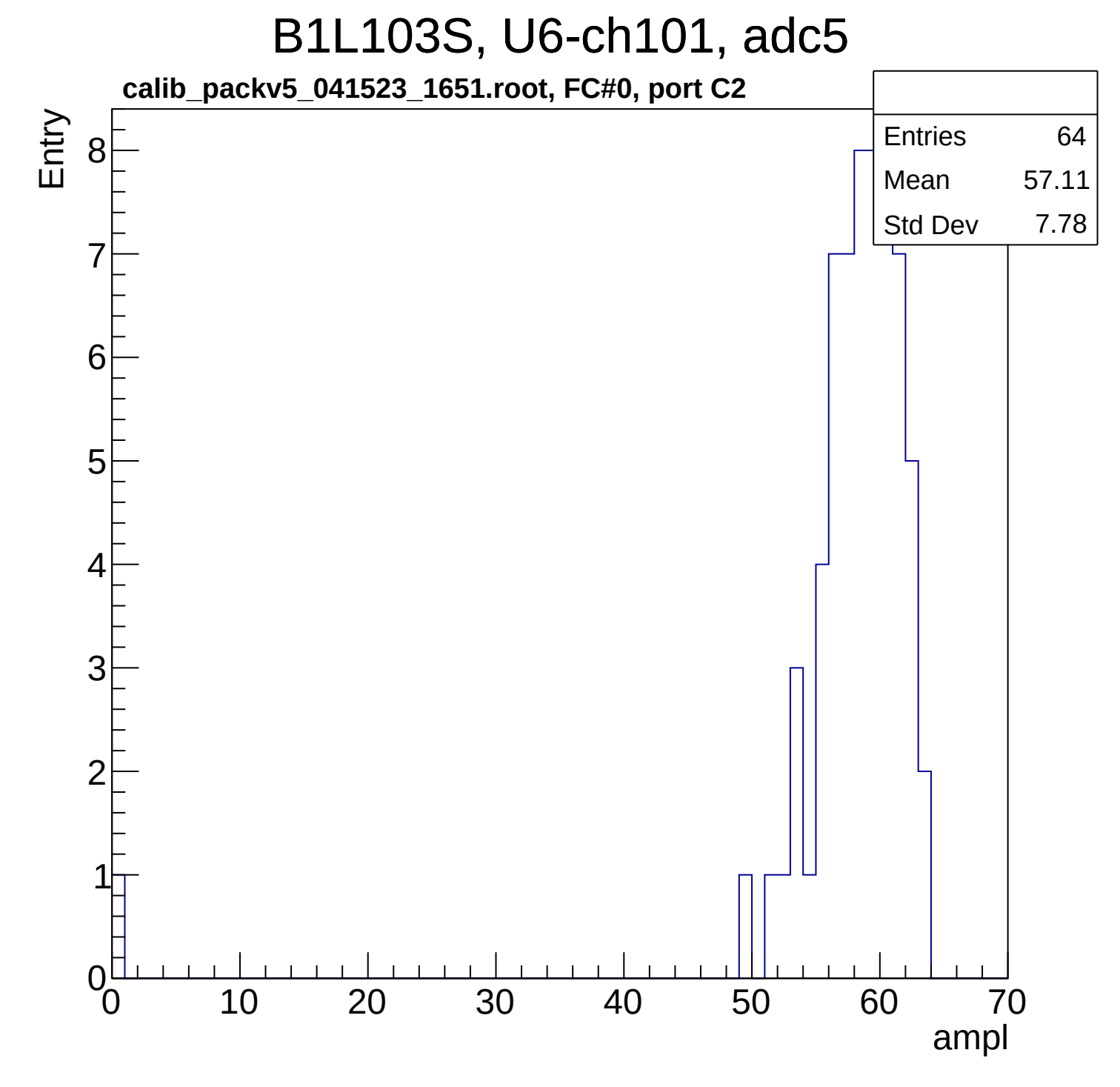
B1L103S, U6-ch101, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 57.11
Std Dev 7.78
Entry
ampl
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7
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0
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40
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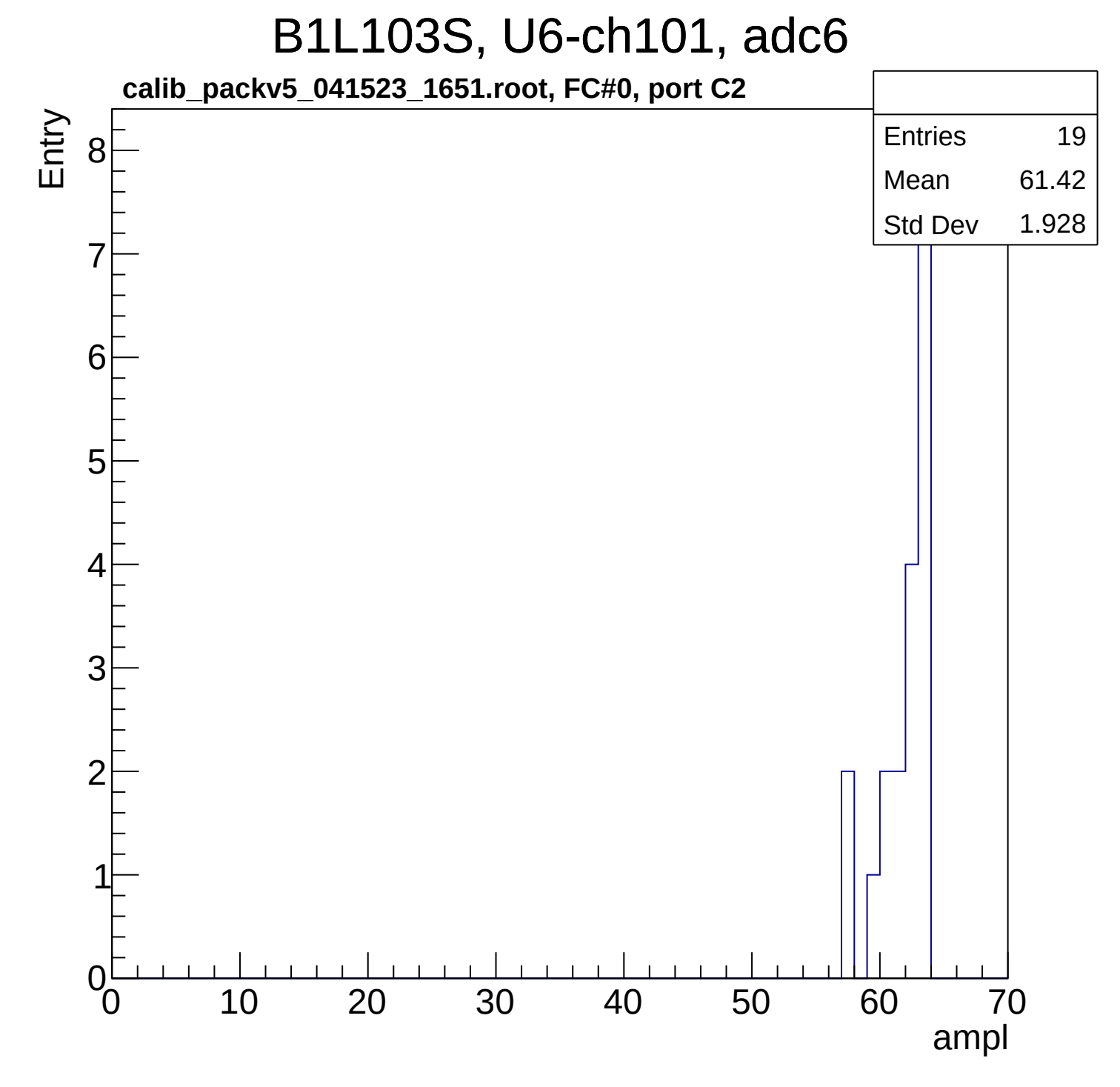
B1L103S, U6-ch101, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 61.42
Std Dev 1.928
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
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60
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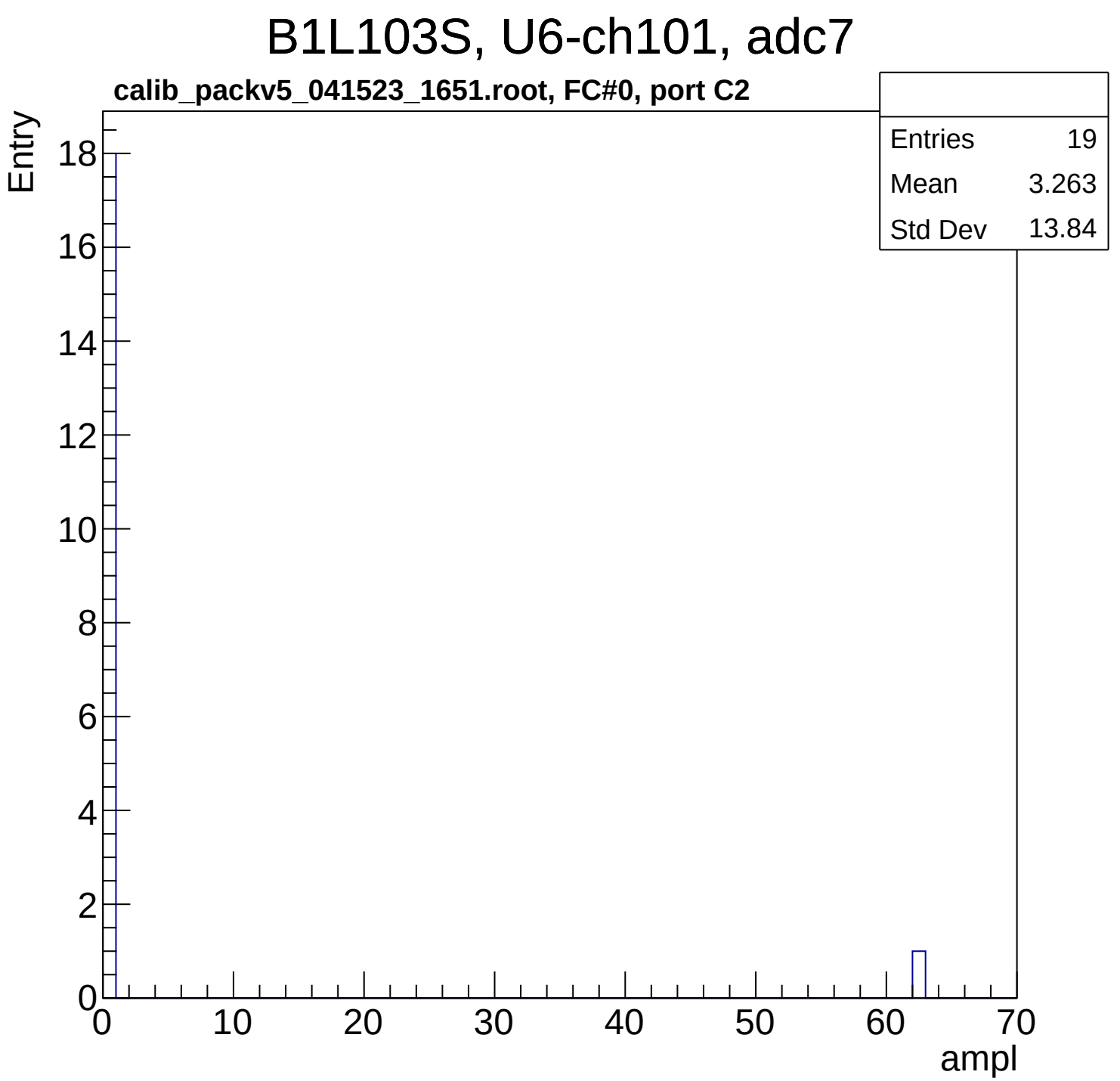
B1L103S, U6-ch101, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.263
Std Dev 13.84
Entry
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6
8
10
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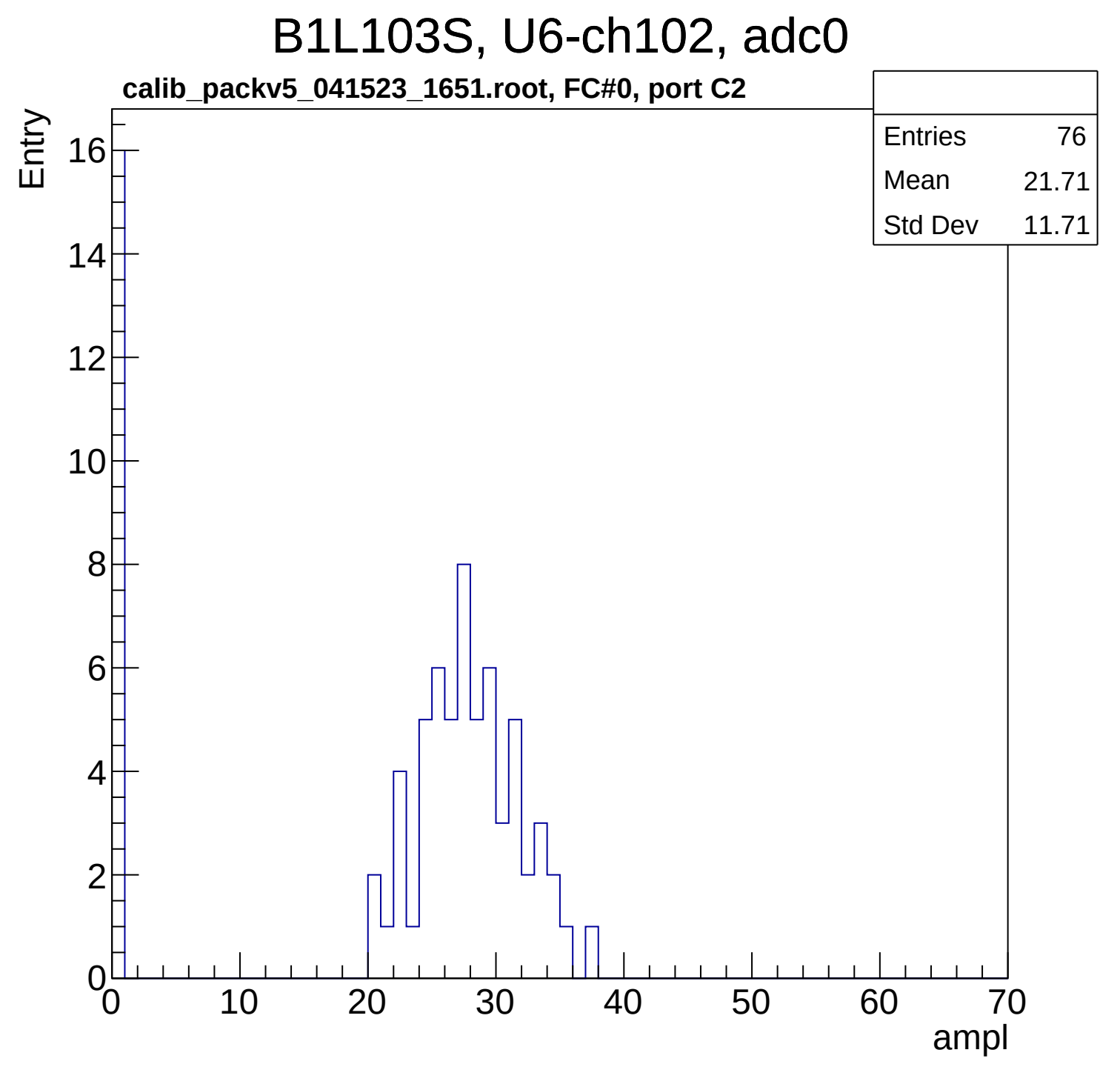
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch102, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 21.71
Std Dev 11.71
Entry
ampl
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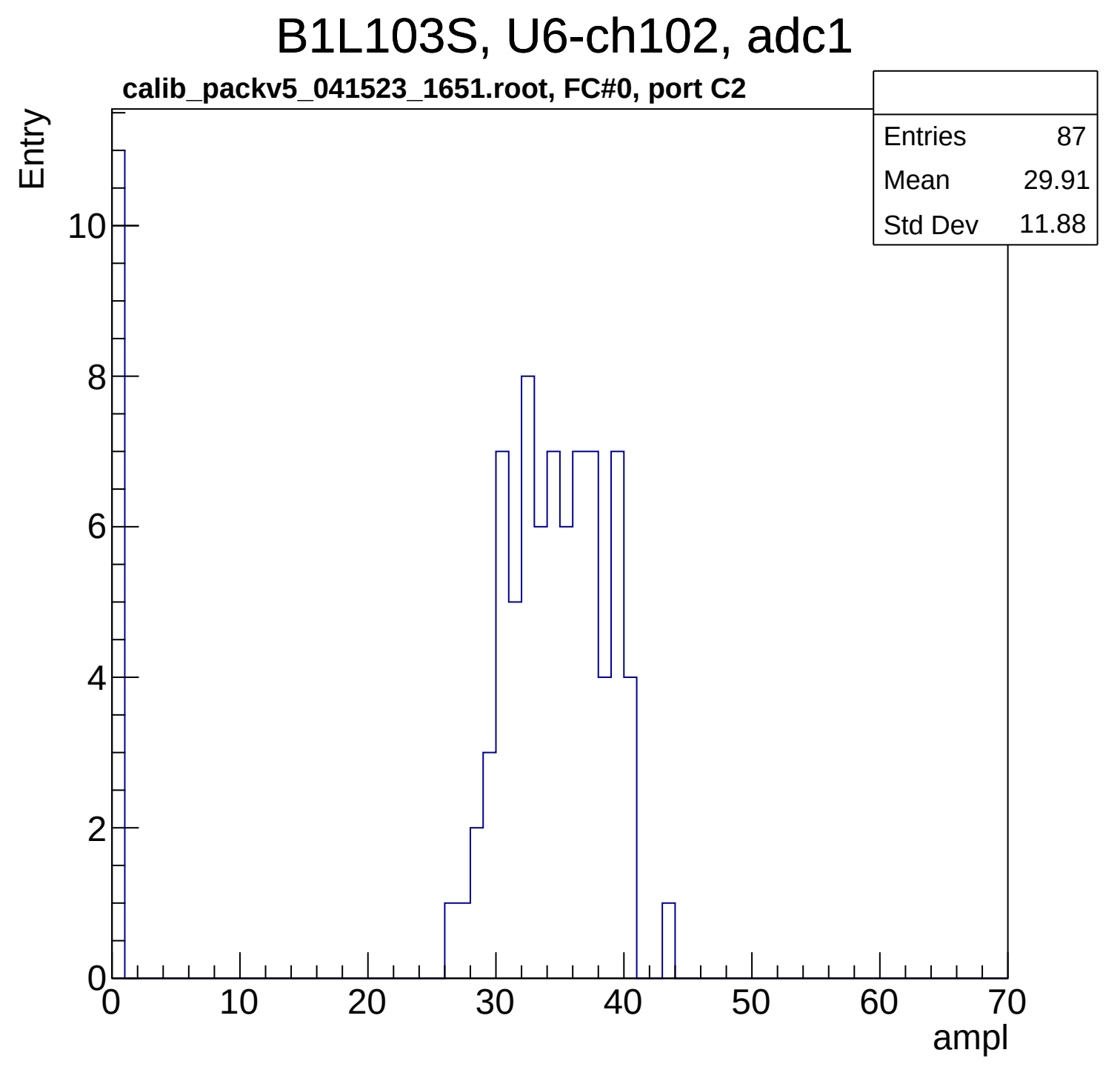
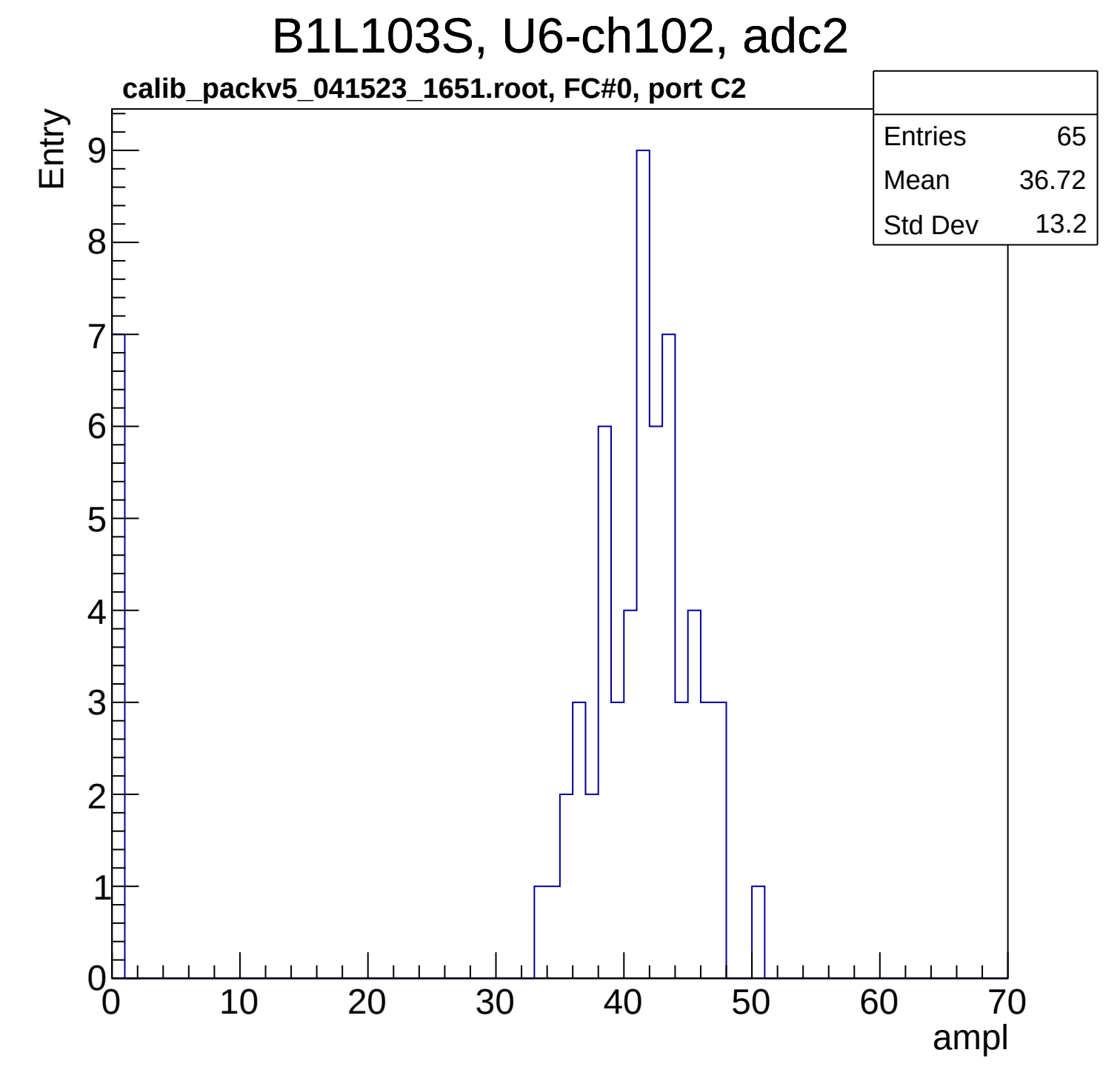
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L103S, U6-ch102, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 29.91
Std Dev 11.88
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch102, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 36.72
Std Dev 13.2
Entry
ampl
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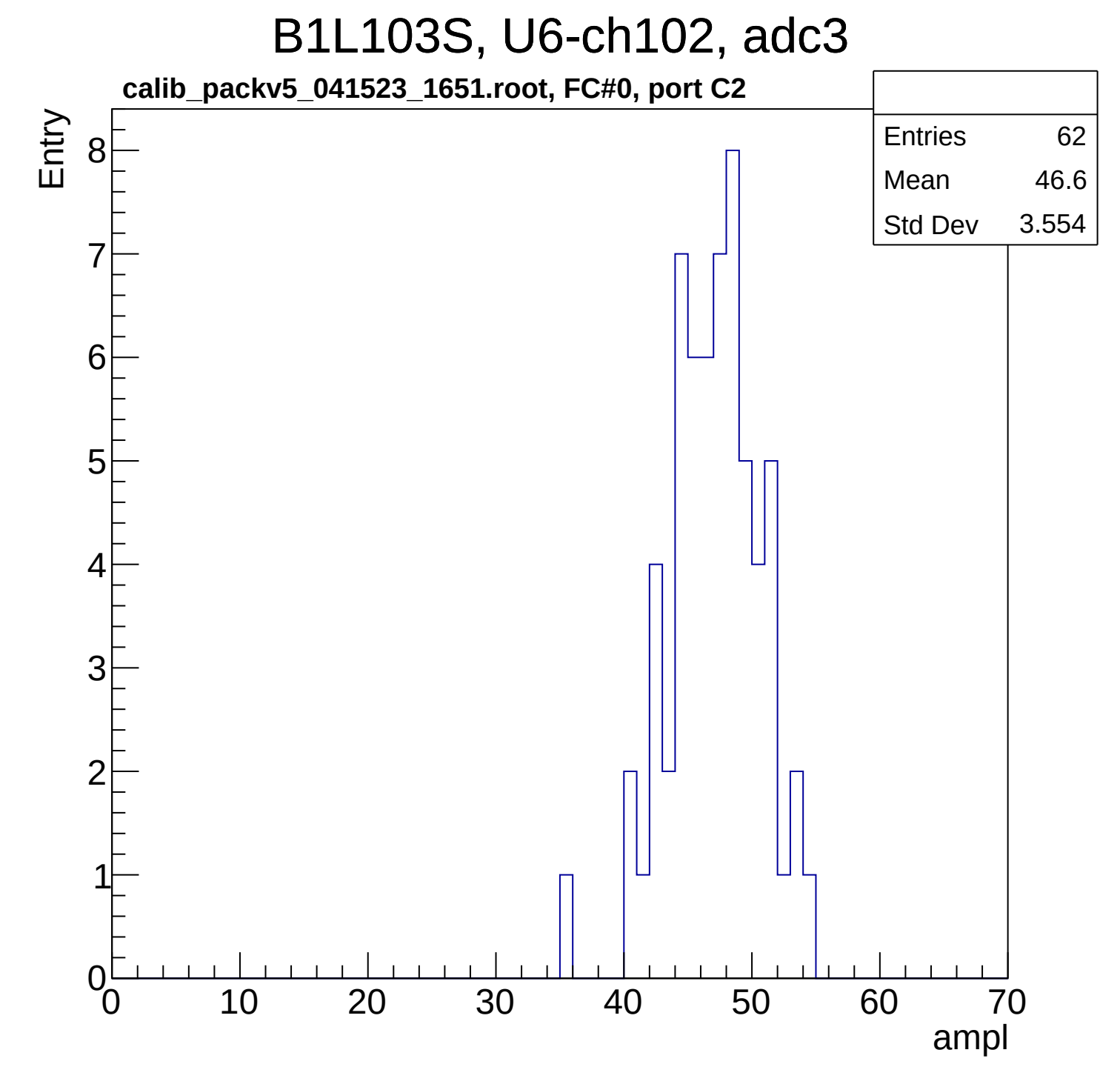
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch102, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 46.6
Std Dev 3.554
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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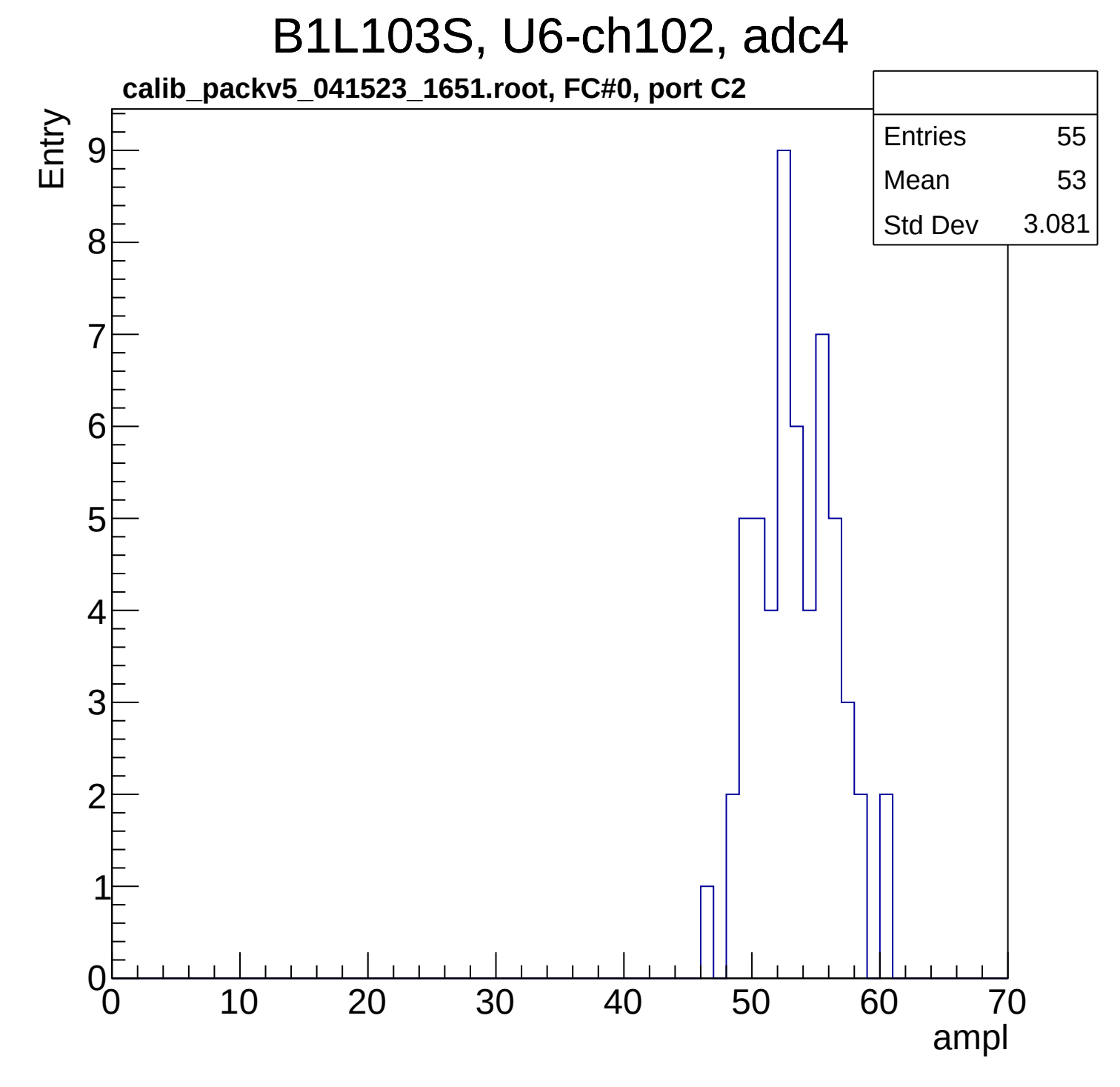
B1L103S, U6-ch102, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 53
Std Dev 3.081
Entry
ampl
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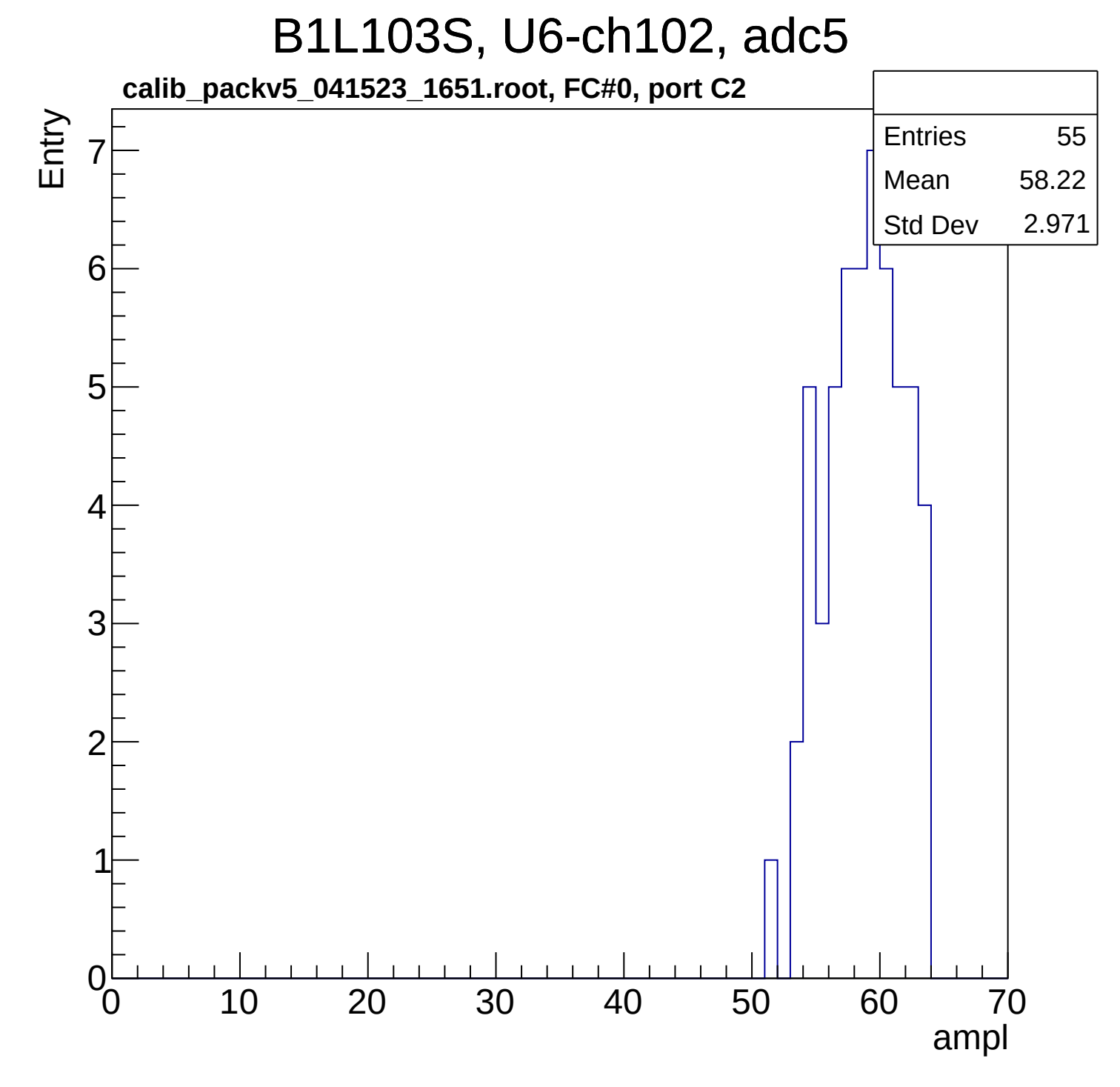
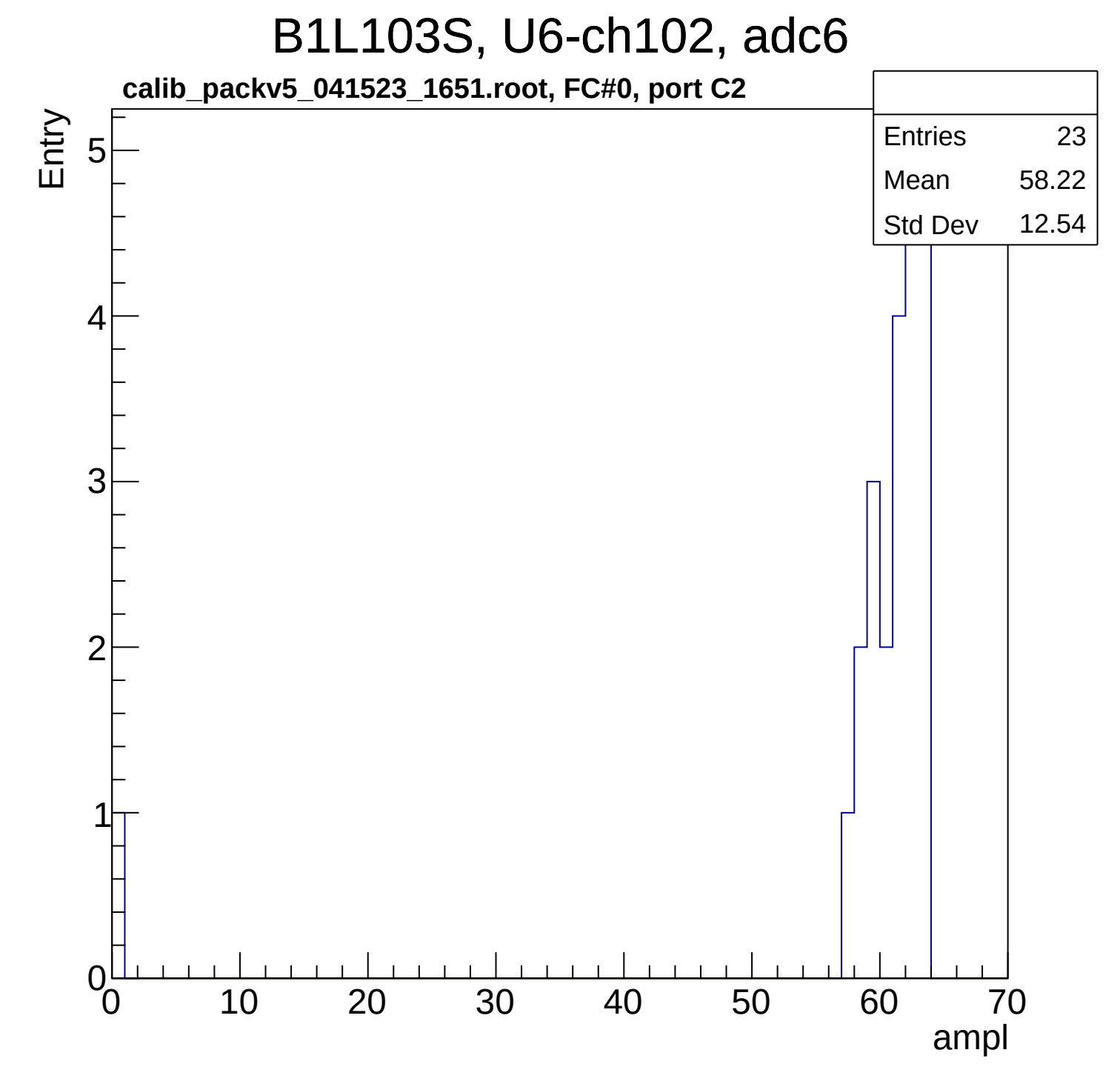
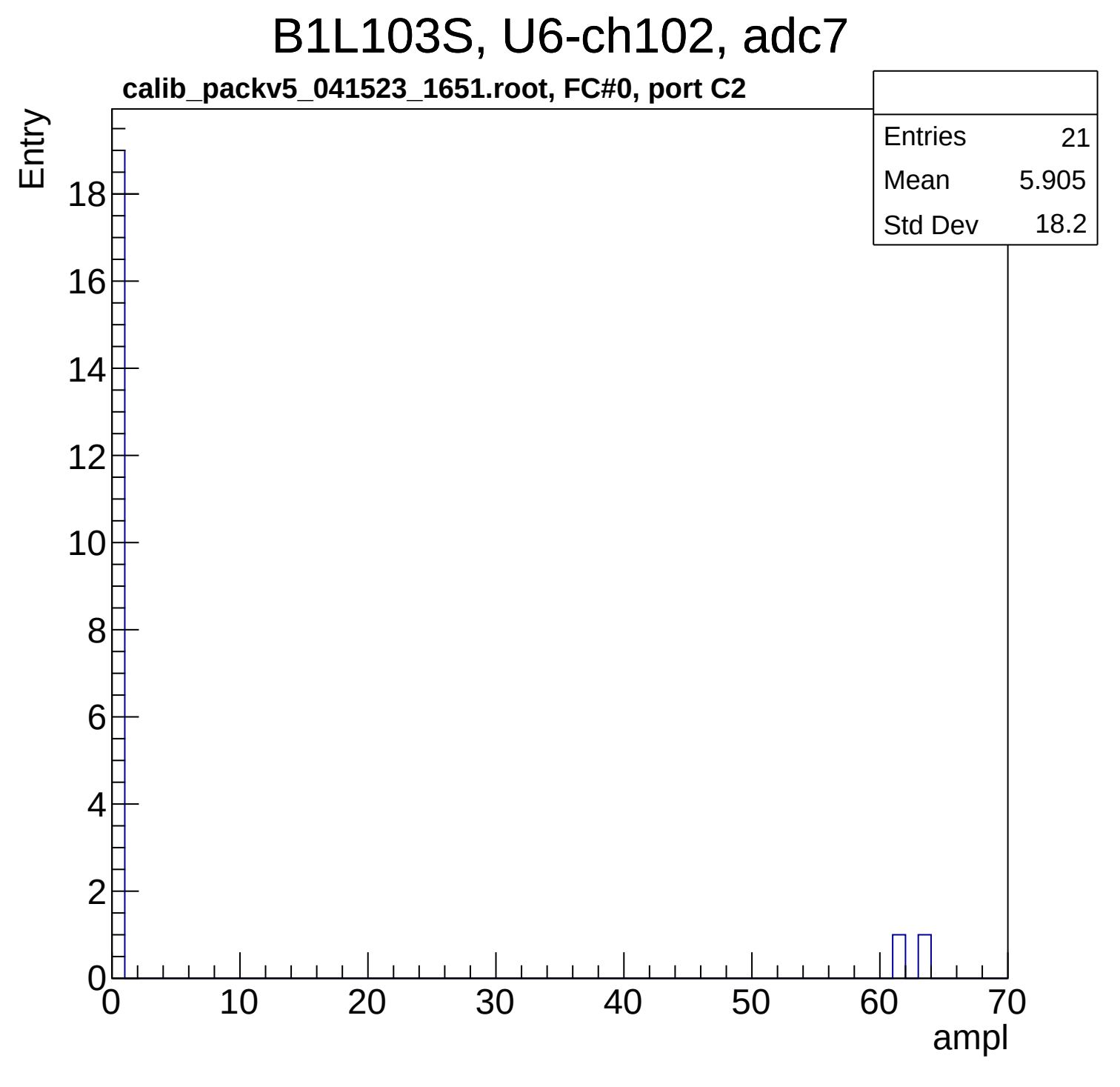
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch102, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 58.22
Std Dev 2.971
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U6-ch102, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 58.22
Std Dev 12.54
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch102, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.905
Std Dev 18.2
Entry
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6
8
10
12
14
16
18
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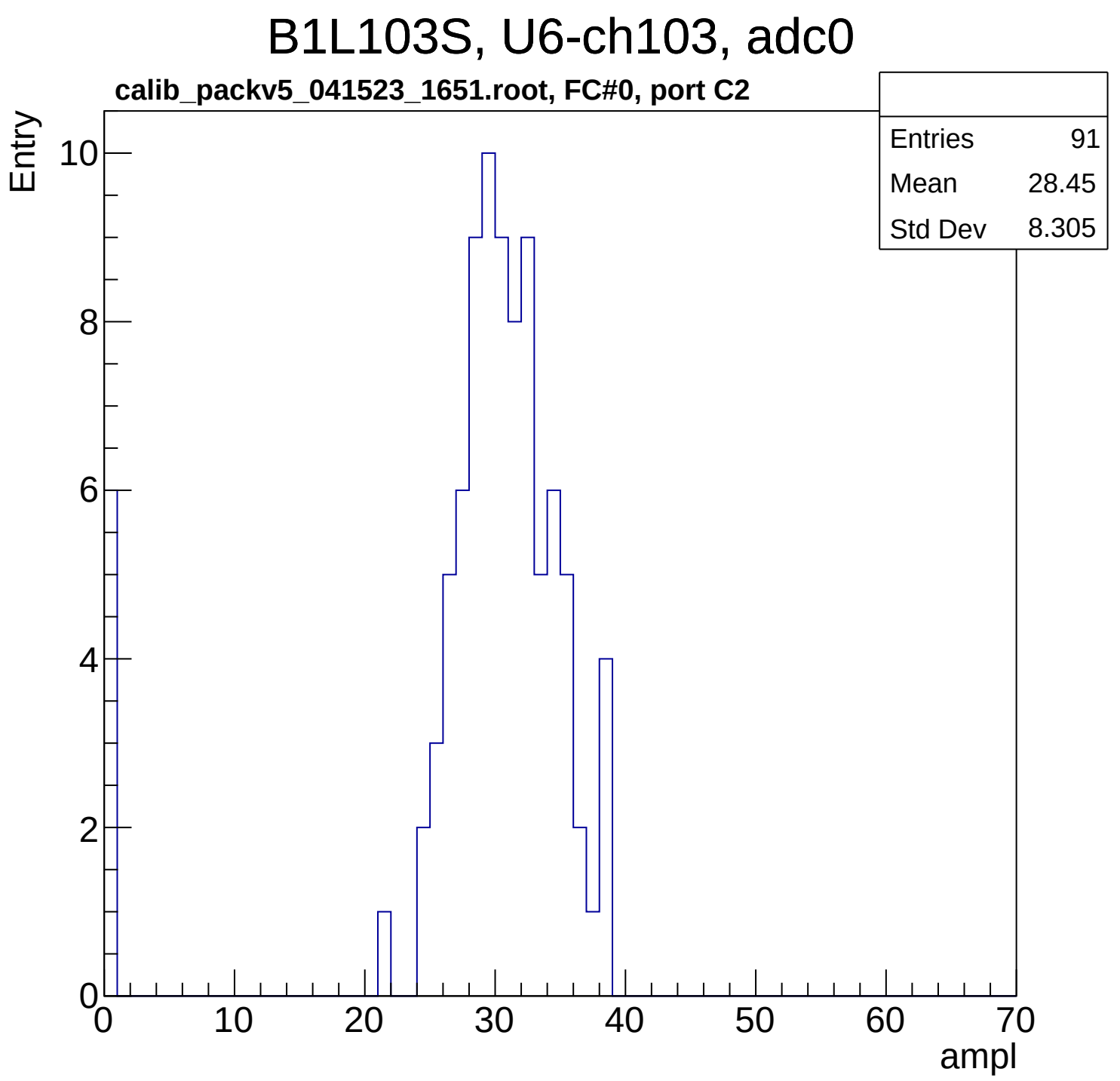
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch103, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 28.45
Std Dev 8.305
Entry
ampl
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2
4
6
8
10
0
10
20
30
40
50
60
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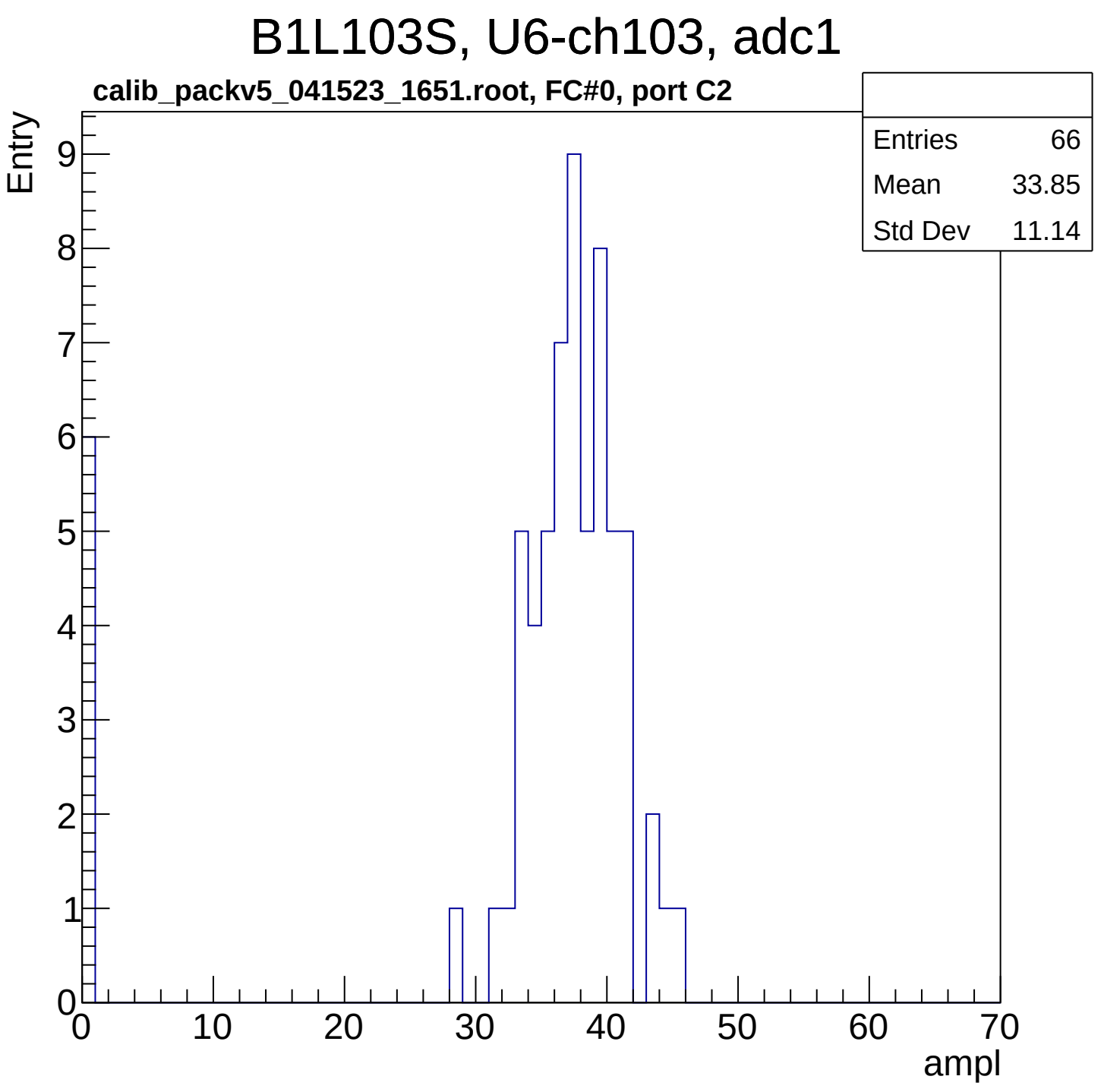
B1L103S, U6-ch103, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 33.85
Std Dev 11.14
Entry
ampl
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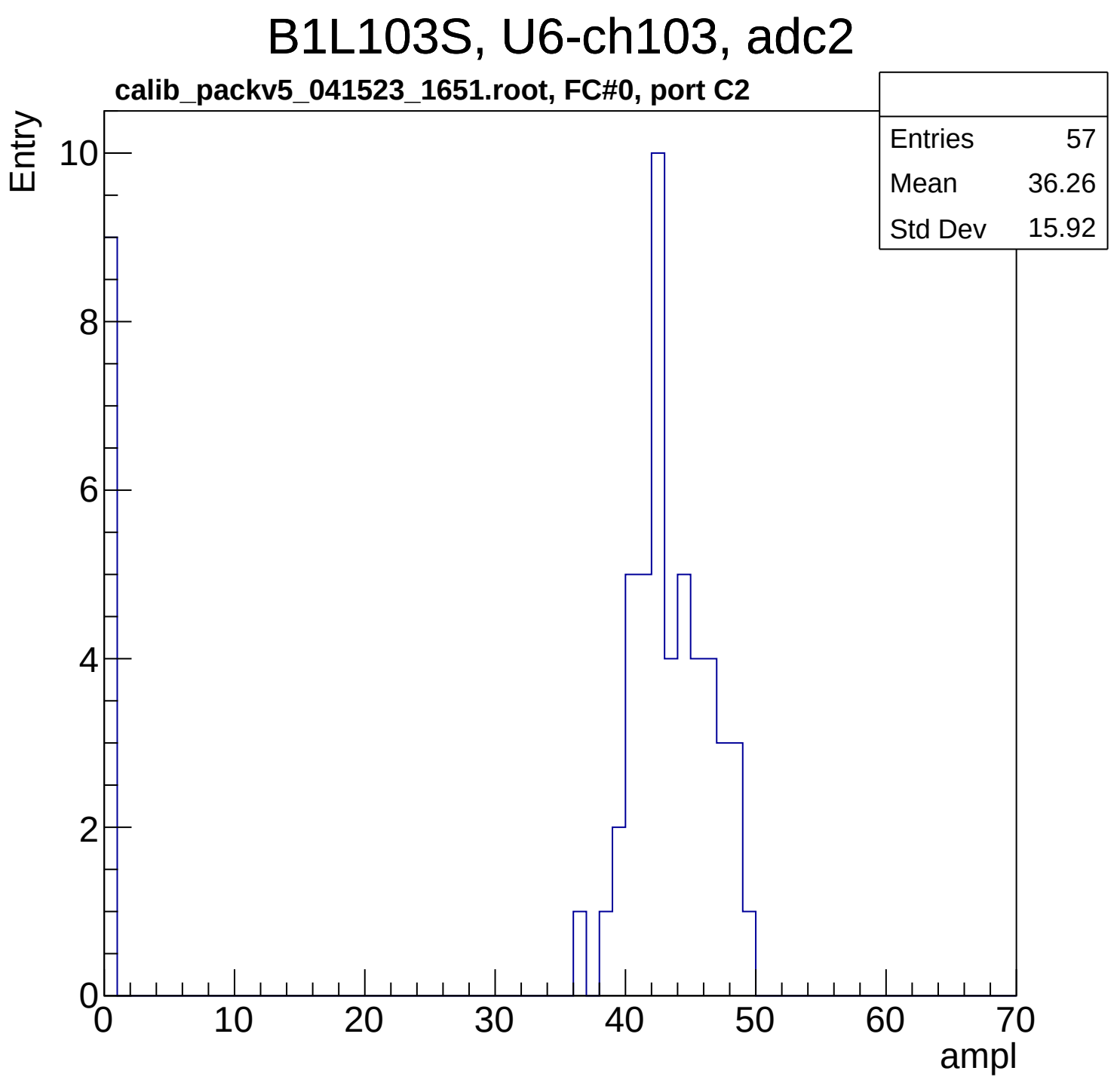
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch103, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 36.26
Std Dev 15.92
Entry
ampl
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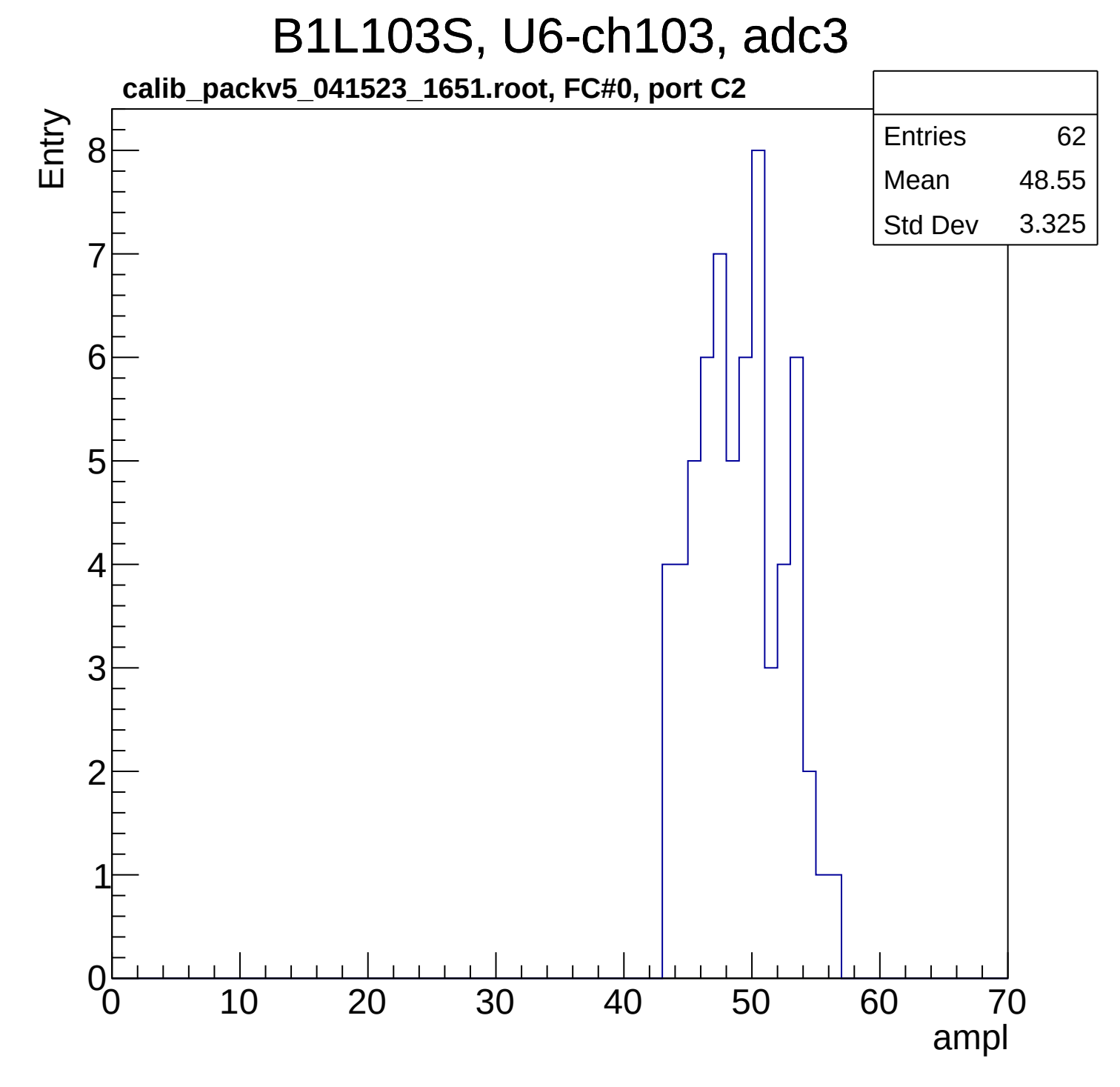
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U6-ch103, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 48.55
Std Dev 3.325
Entry
ampl
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2
3
4
5
6
7
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0
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40
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60
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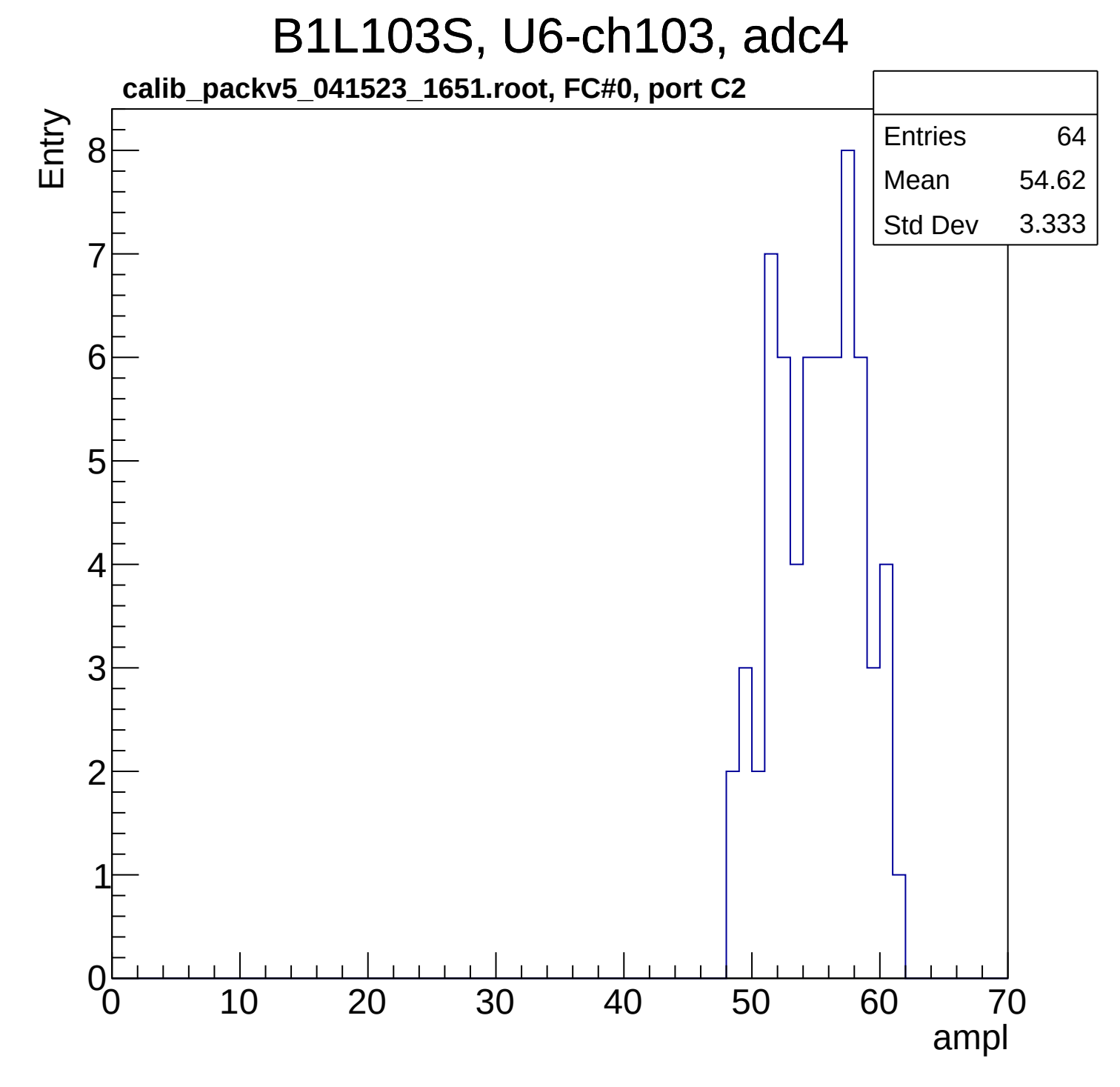
B1L103S, U6-ch103, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 54.62
Std Dev 3.333
Entry
ampl
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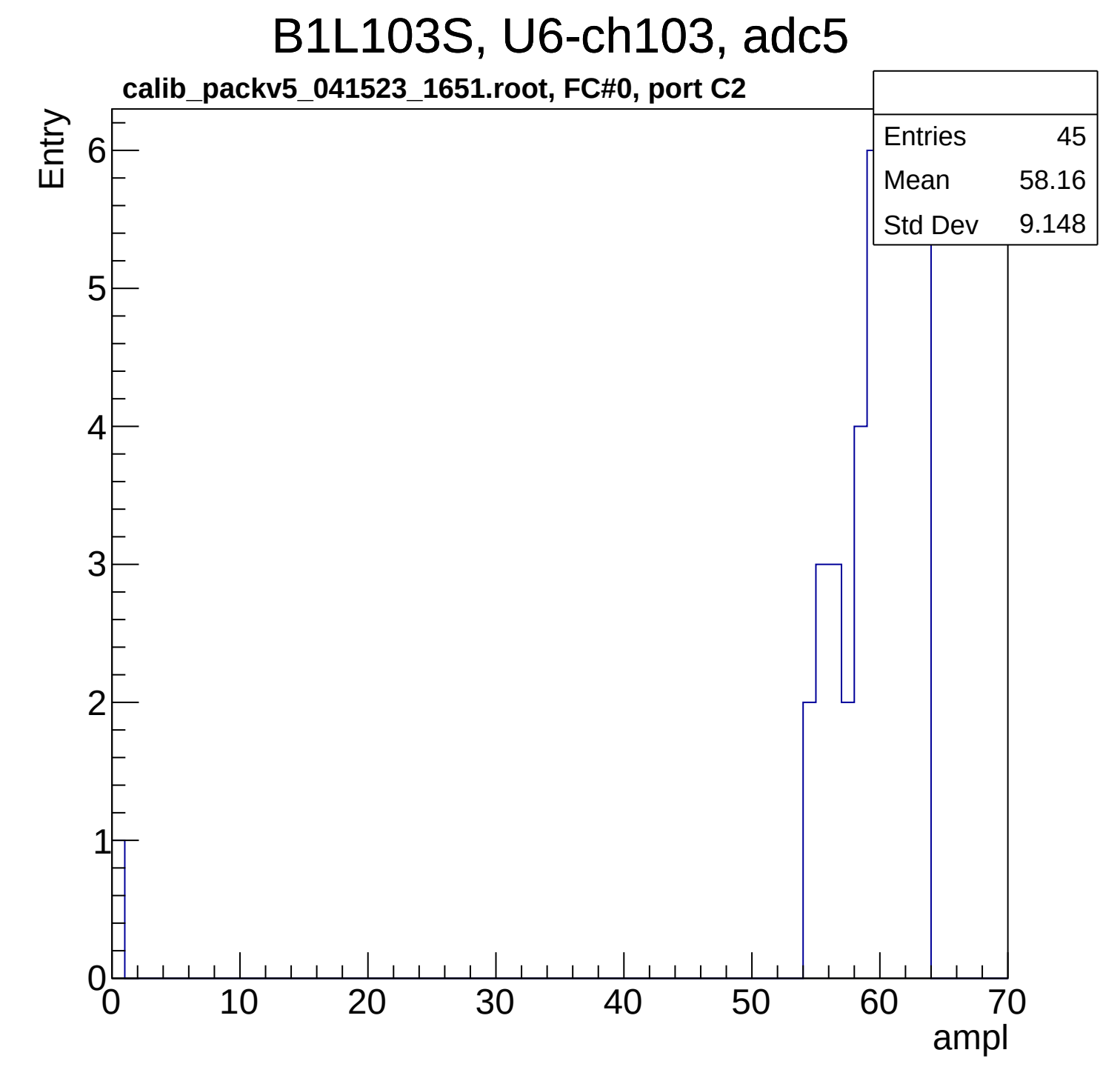
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch103, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 58.16
Std Dev 9.148
Entry
ampl
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3
4
5
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60
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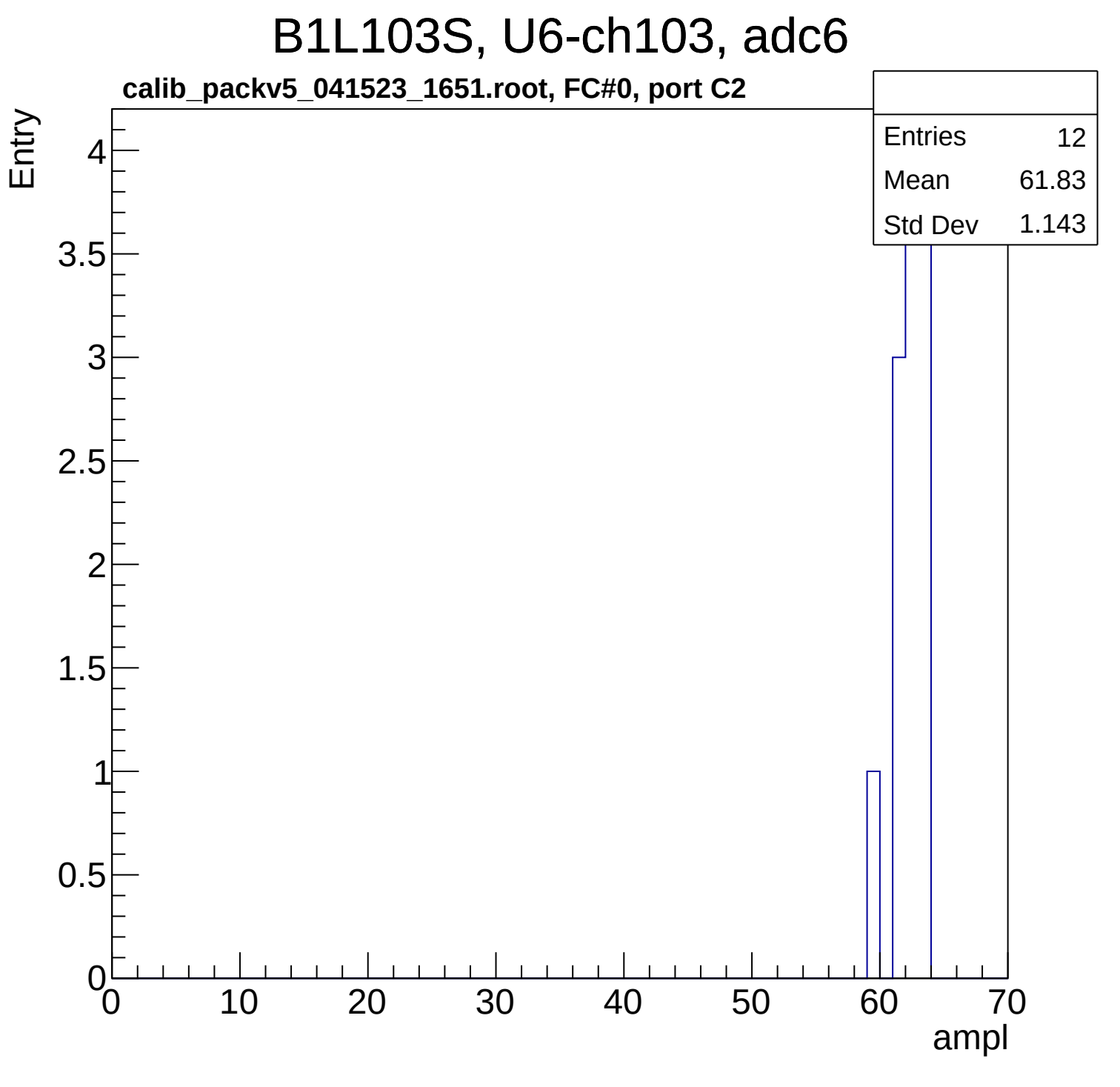
B1L103S, U6-ch103, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.83
Std Dev 1.143
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
10
20
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40
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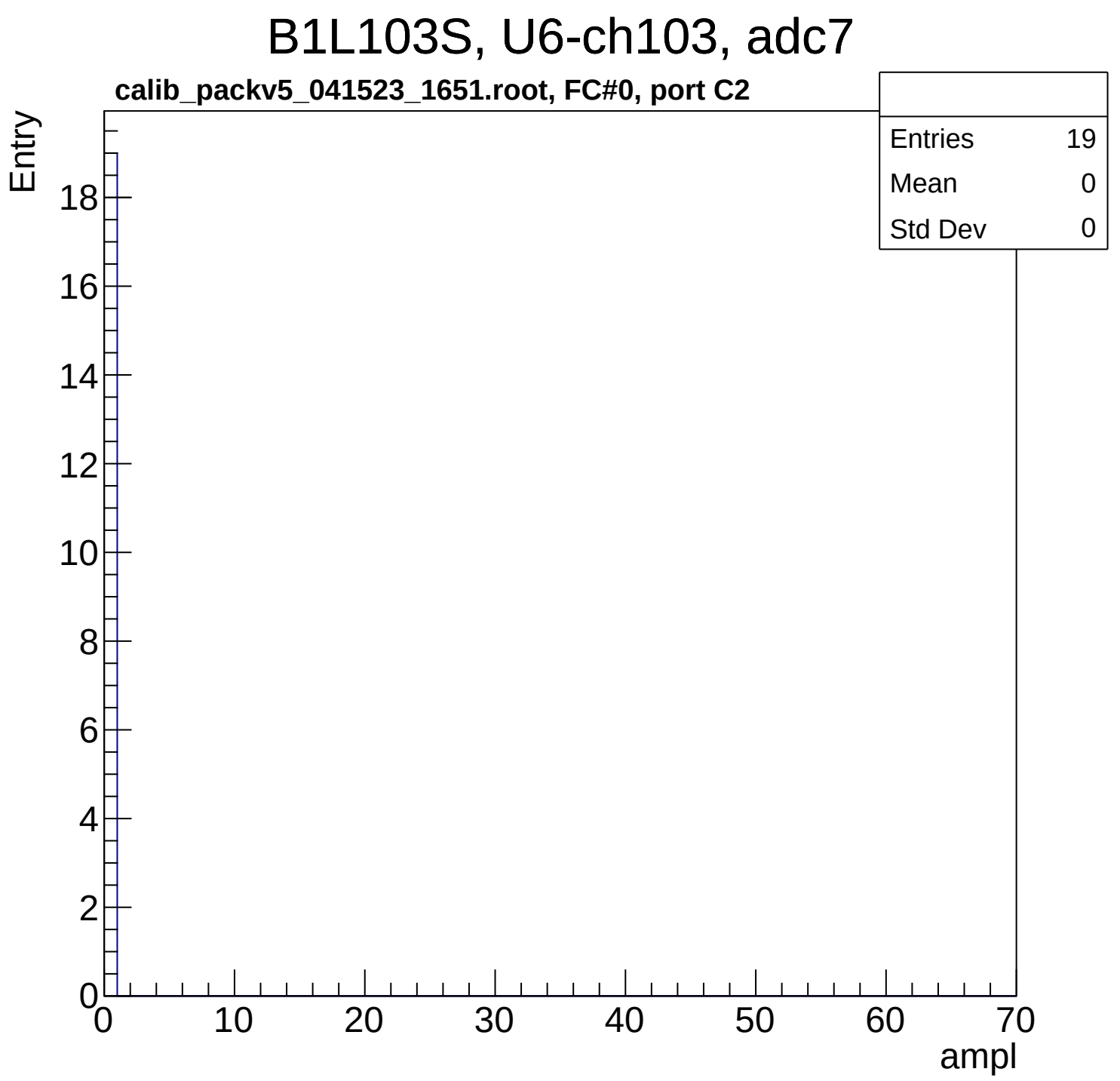
60
70


B1L103S, U6-ch103, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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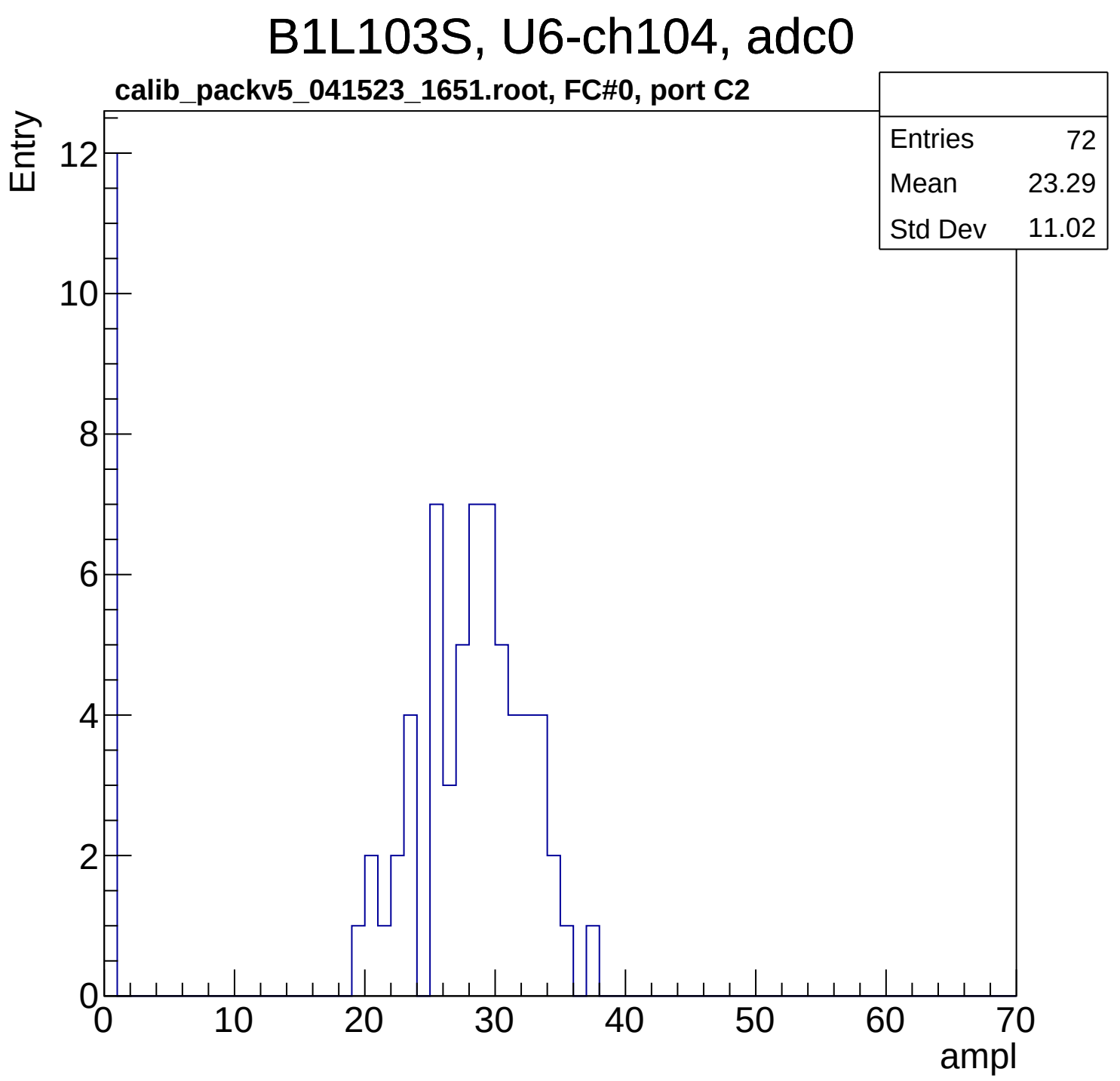
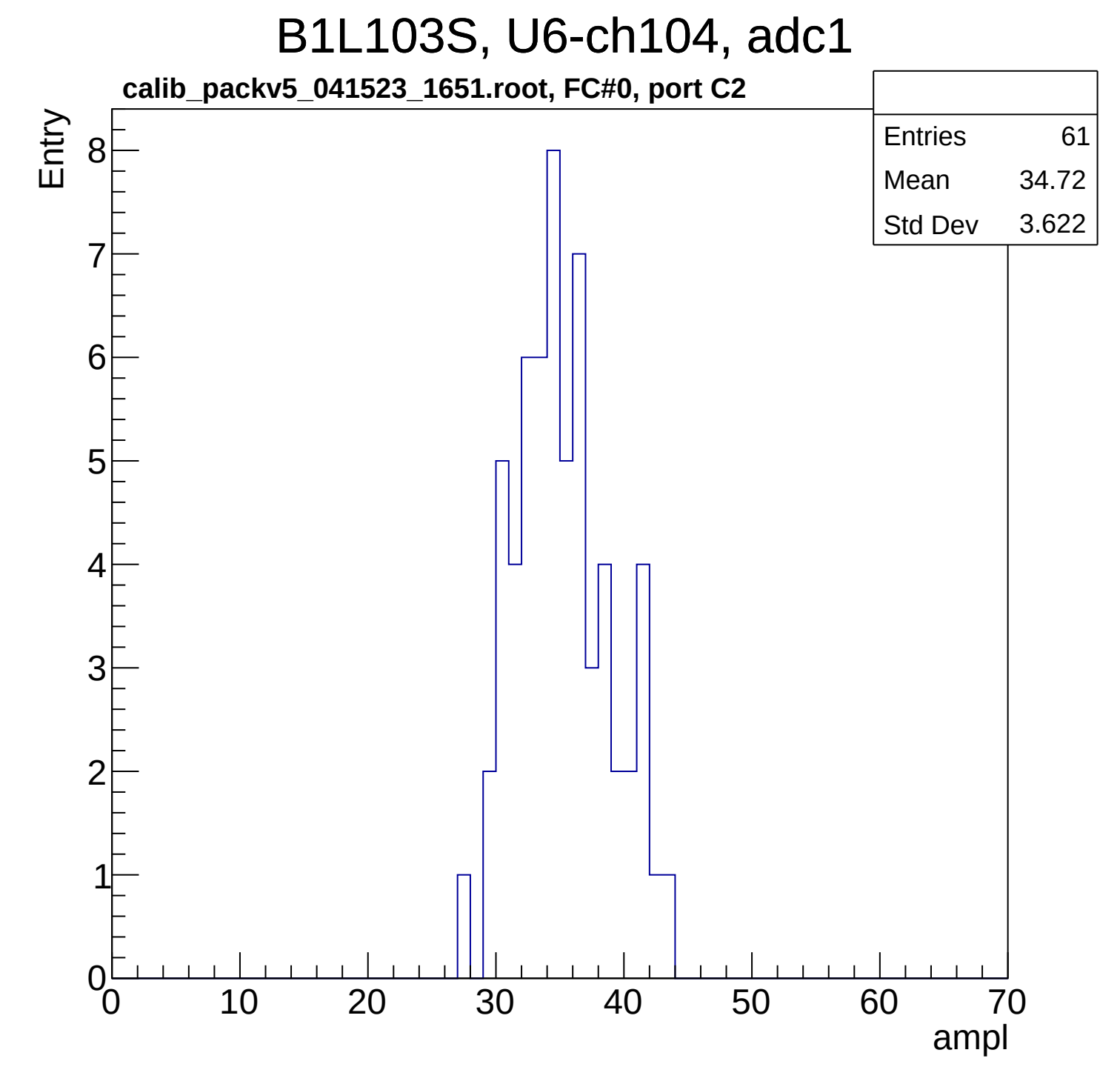
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch104, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 23.29
Std Dev 11.02
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch104, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 34.72
Std Dev 3.622
Entry
ampl
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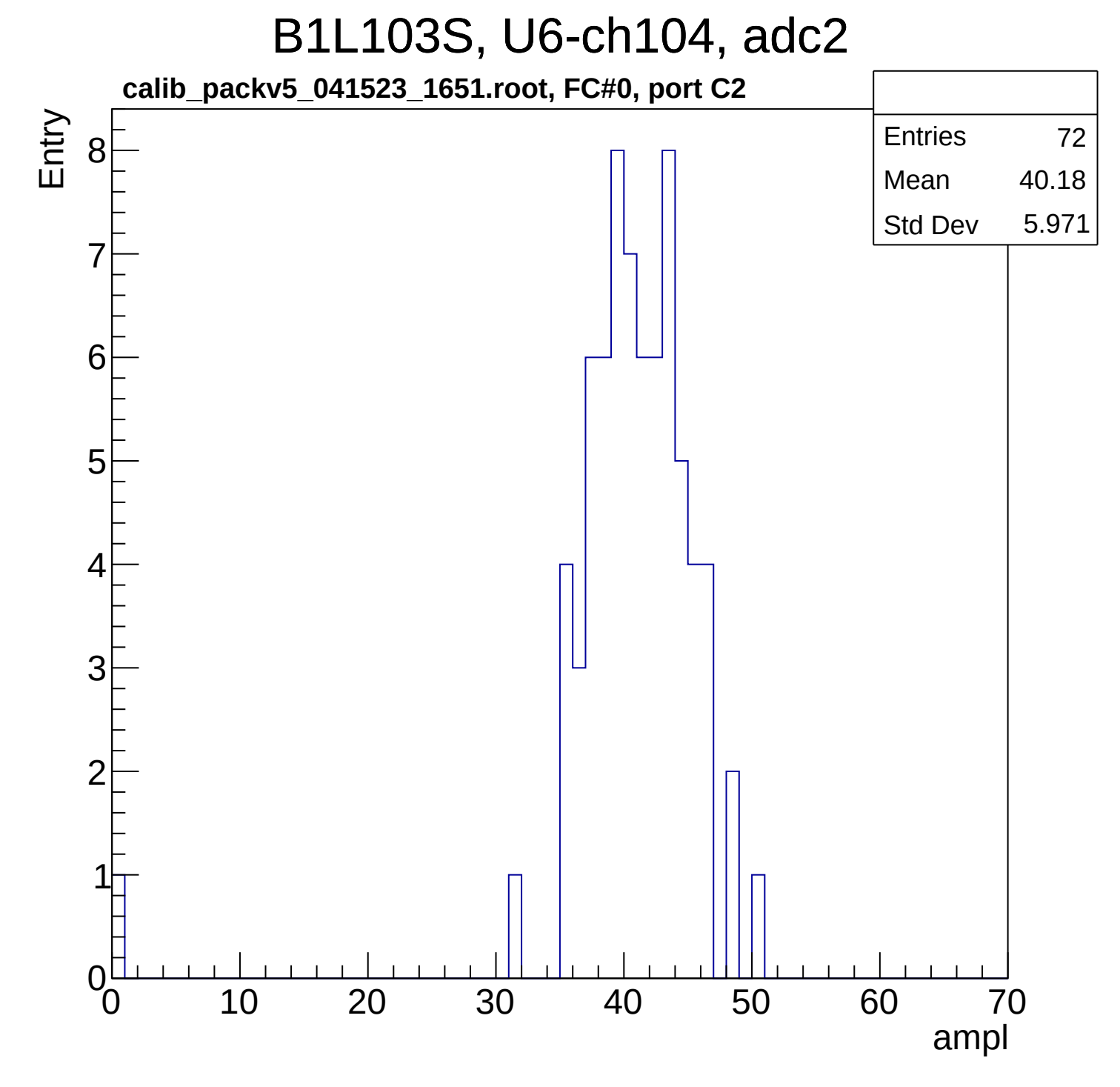
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch104, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 40.18
Std Dev 5.971
Entry
ampl
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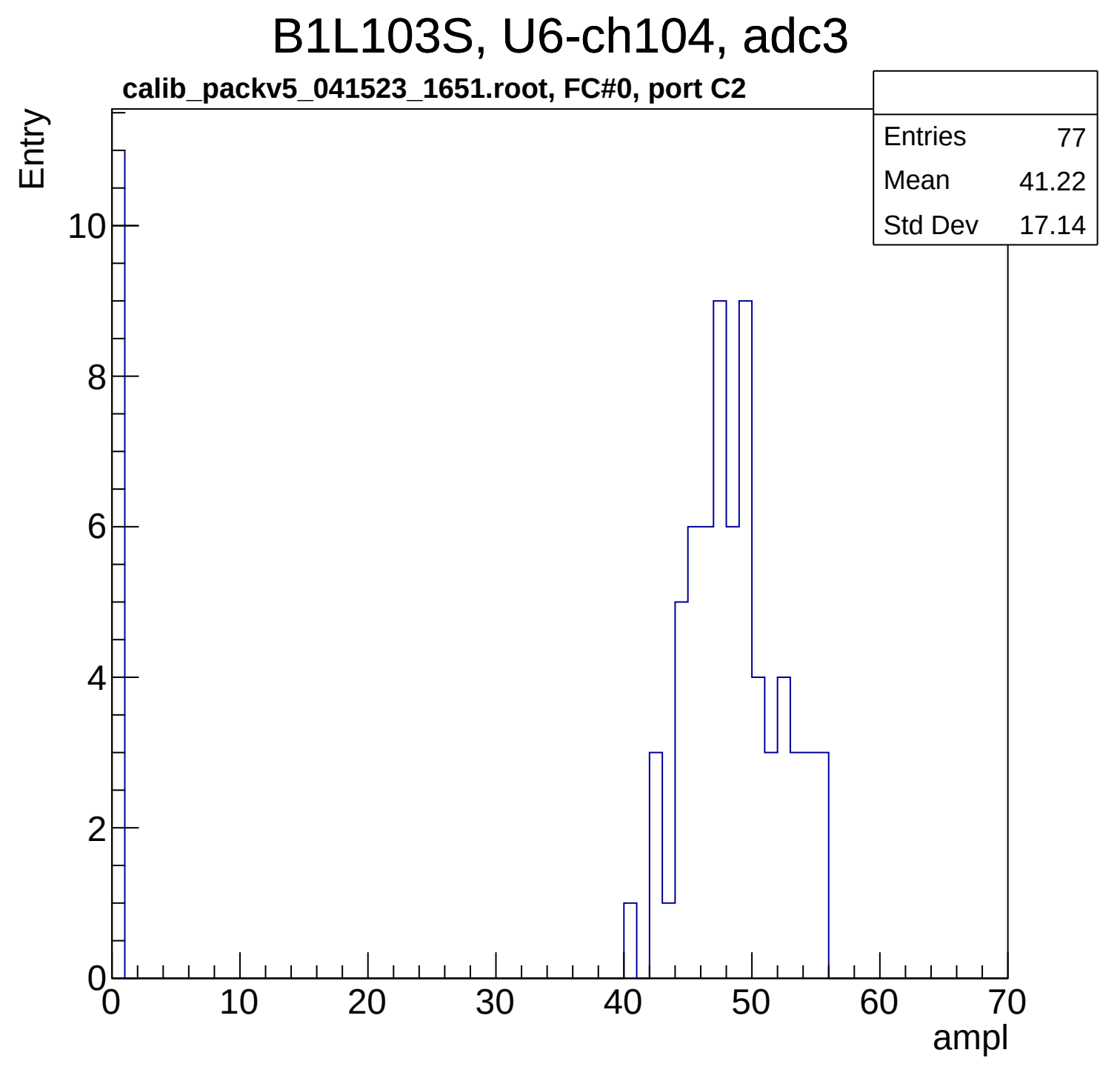
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch104, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 41.22
Std Dev 17.14
Entry
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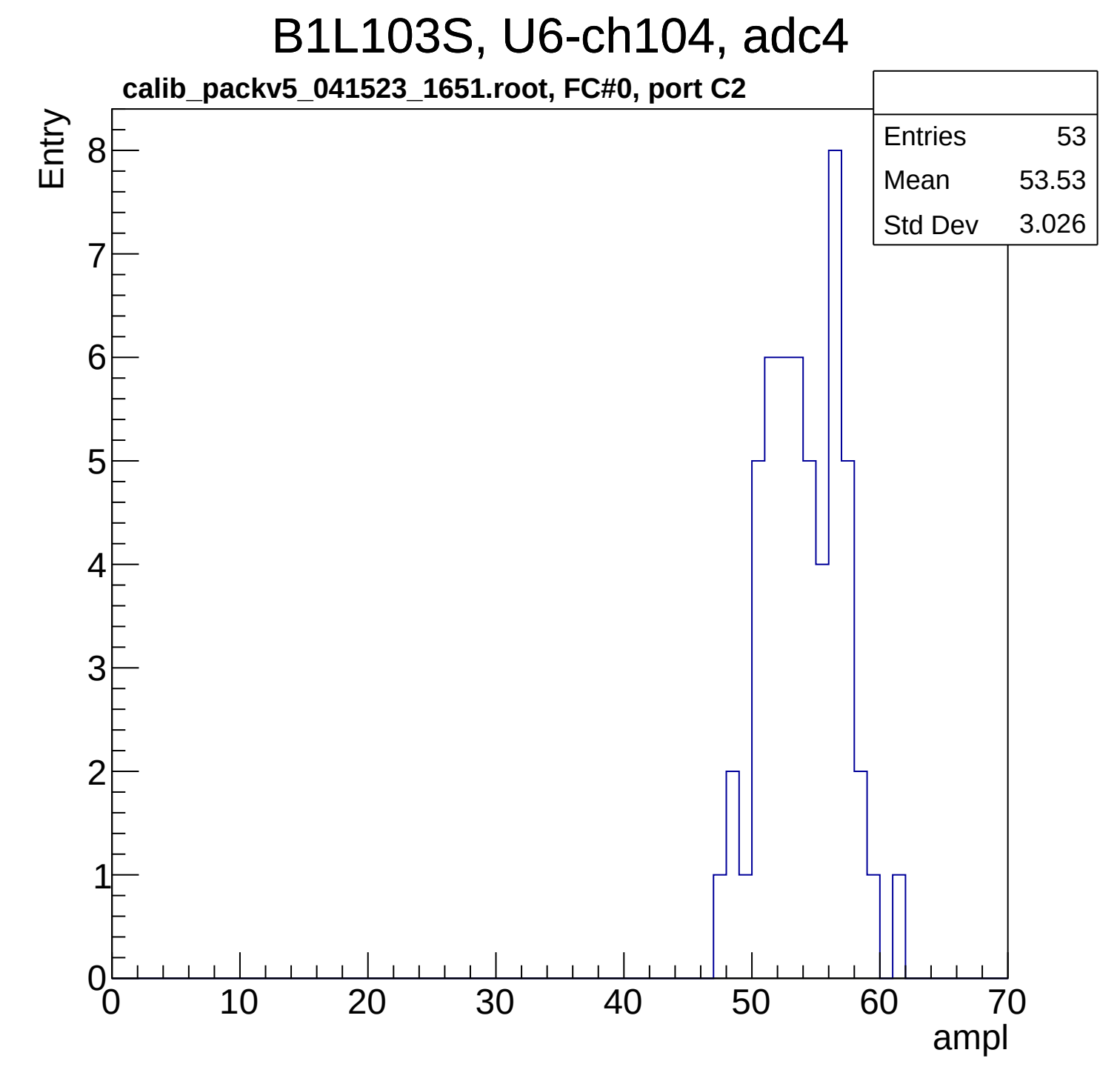
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch104, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 53.53
Std Dev 3.026
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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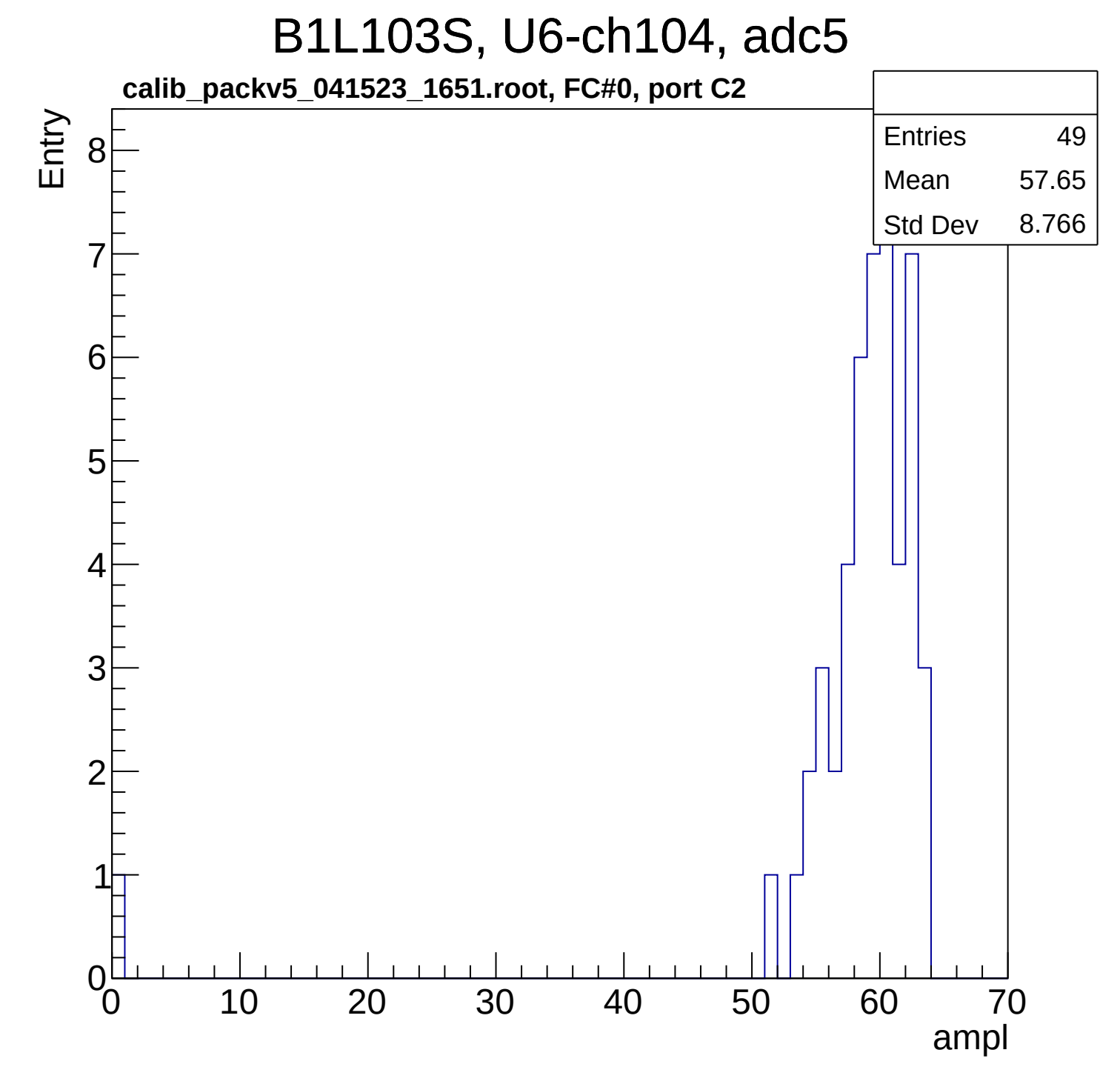
B1L103S, U6-ch104, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 57.65
Std Dev 8.766
Entry
ampl
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1
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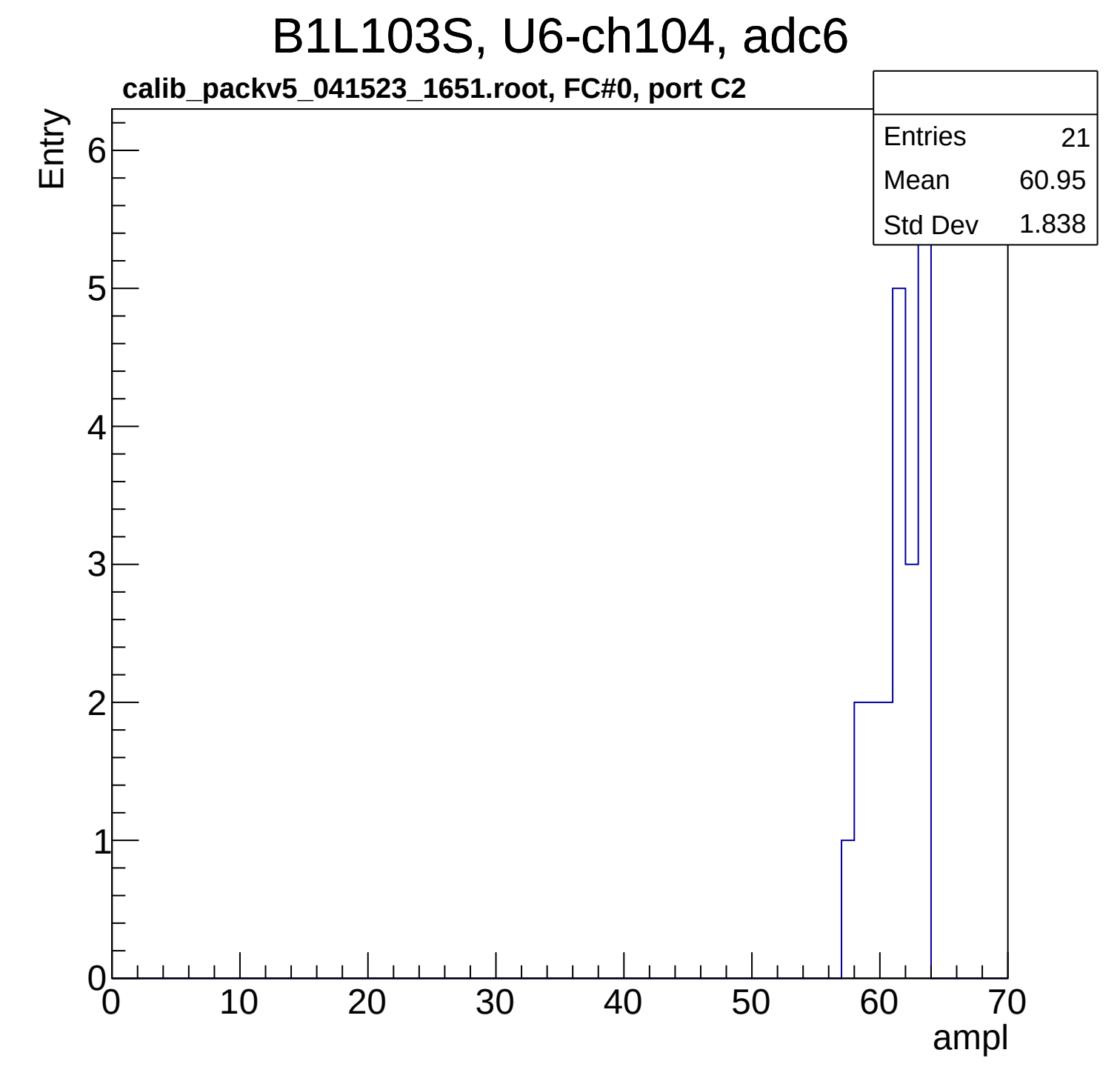
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch104, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 60.95
Std Dev 1.838
Entry
ampl
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2
3
4
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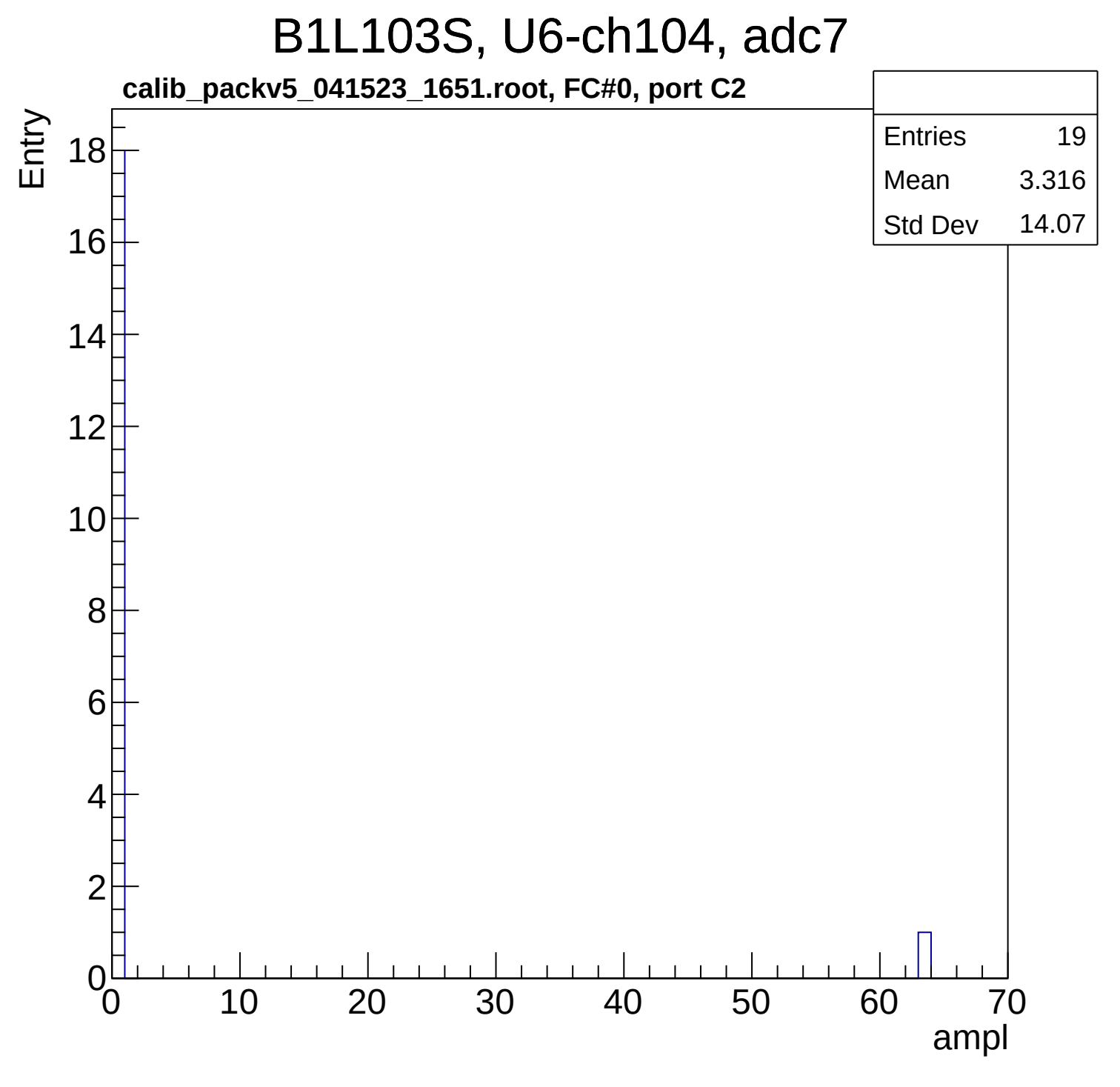
0
10
20
30
40
50
60
70


B1L103S, U6-ch104, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.316
Std Dev 14.07
Entry
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6
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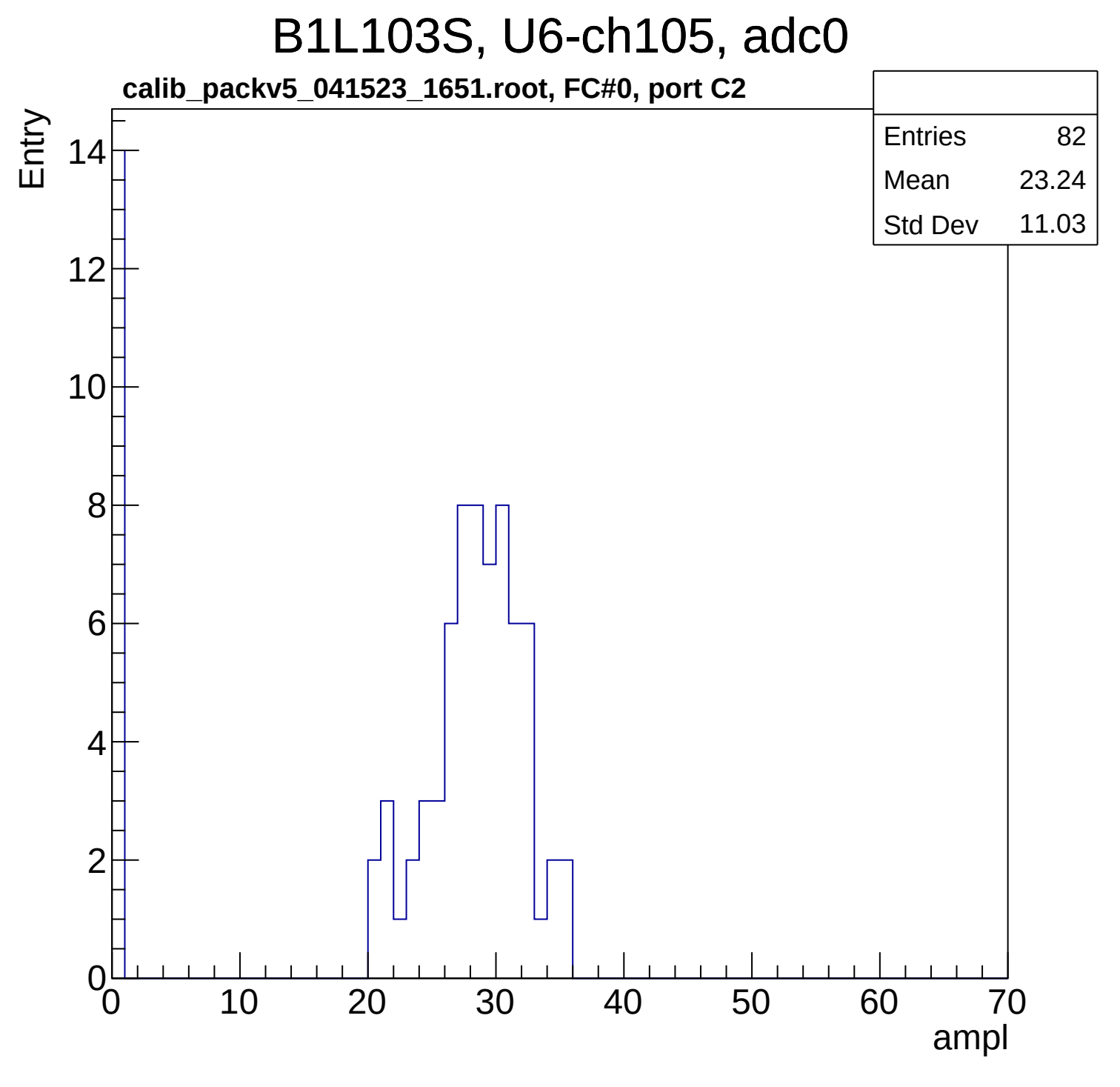
ampl


B1L103S, U6-ch105, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 23.24
Std Dev 11.03
Entry
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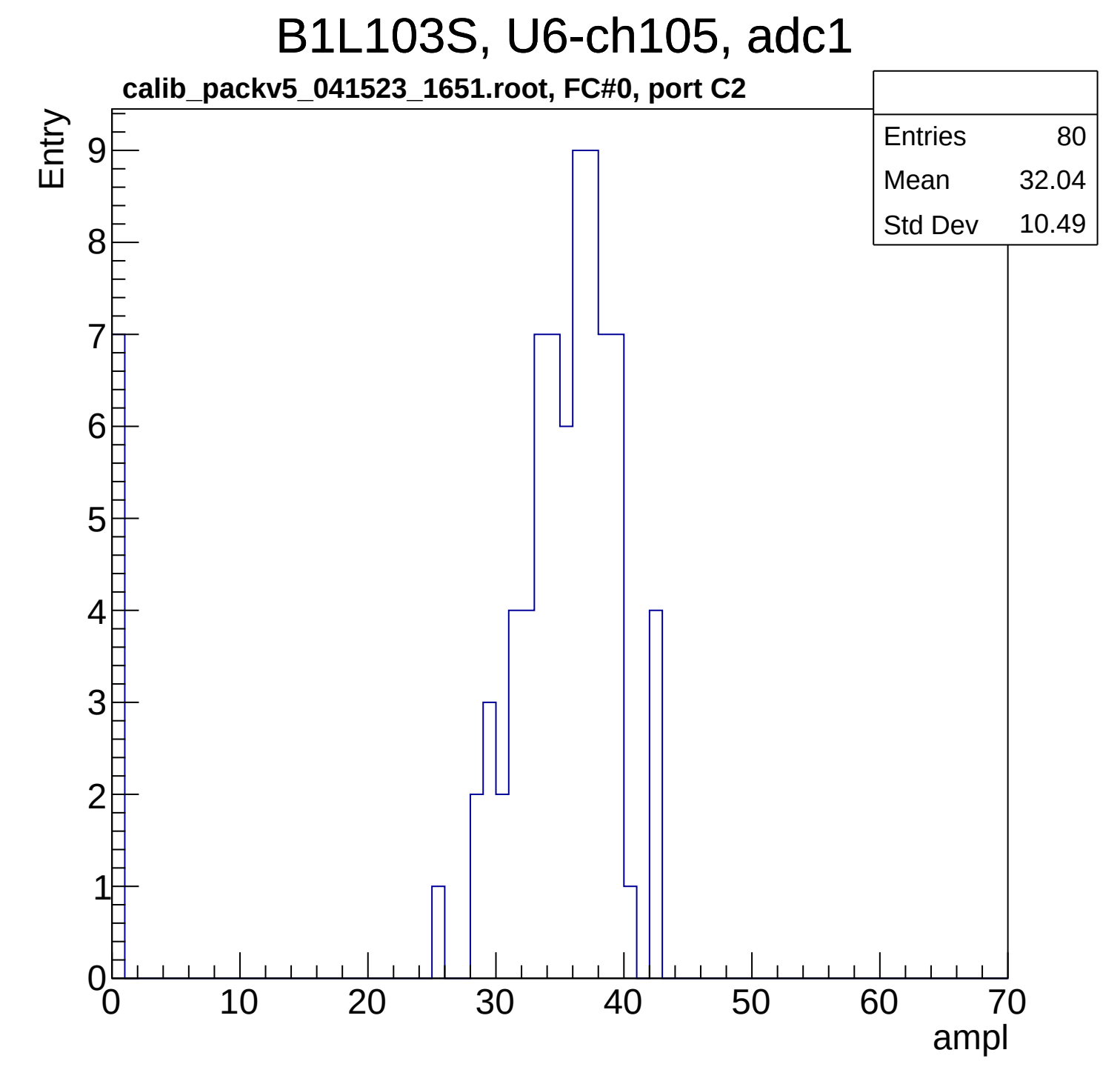
ampl


B1L103S, U6-ch105, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 32.04
Std Dev 10.49
Entry
ampl
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4
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6
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8
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0
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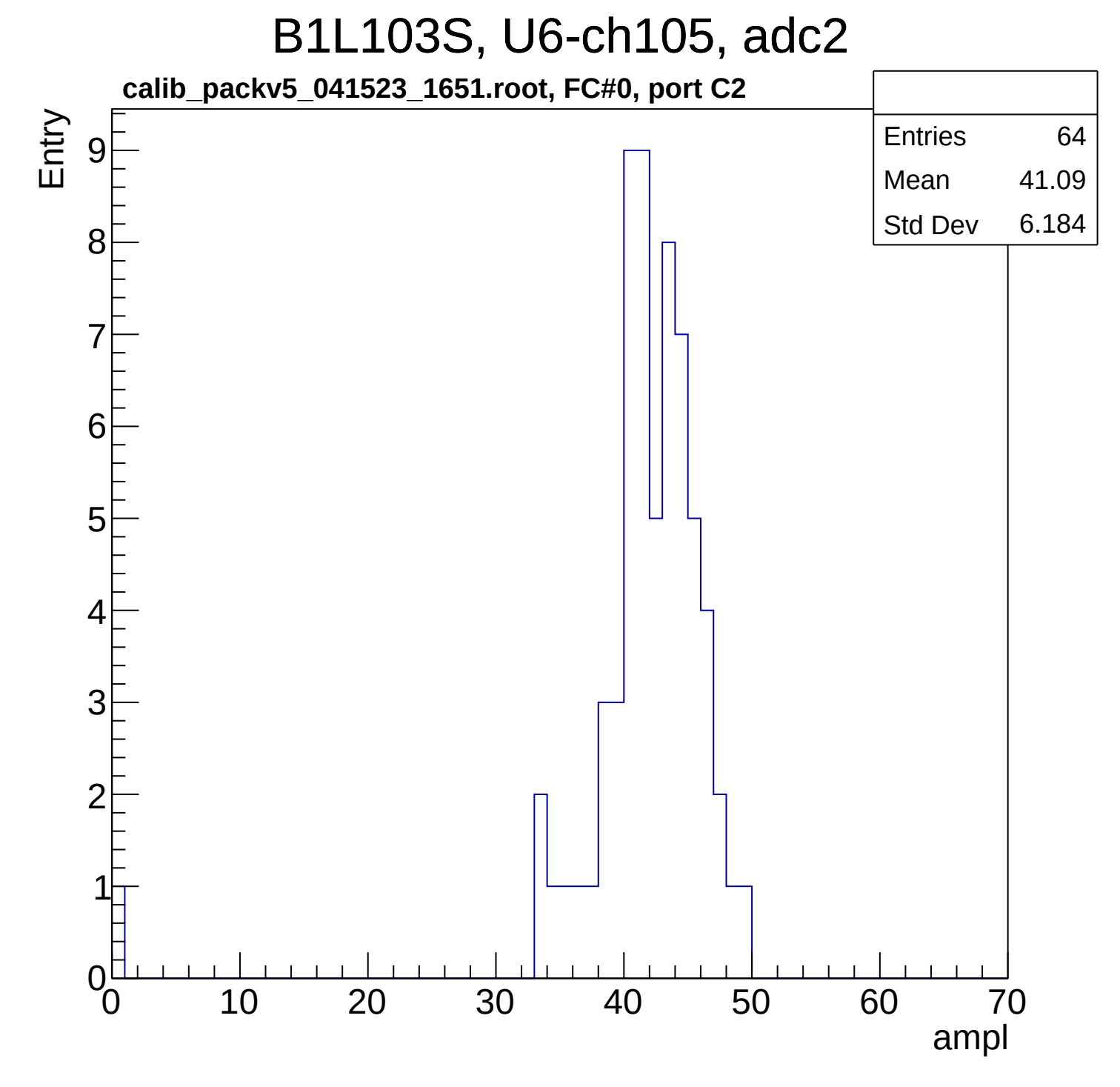
B1L103S, U6-ch105, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 41.09
Std Dev 6.184
Entry
ampl
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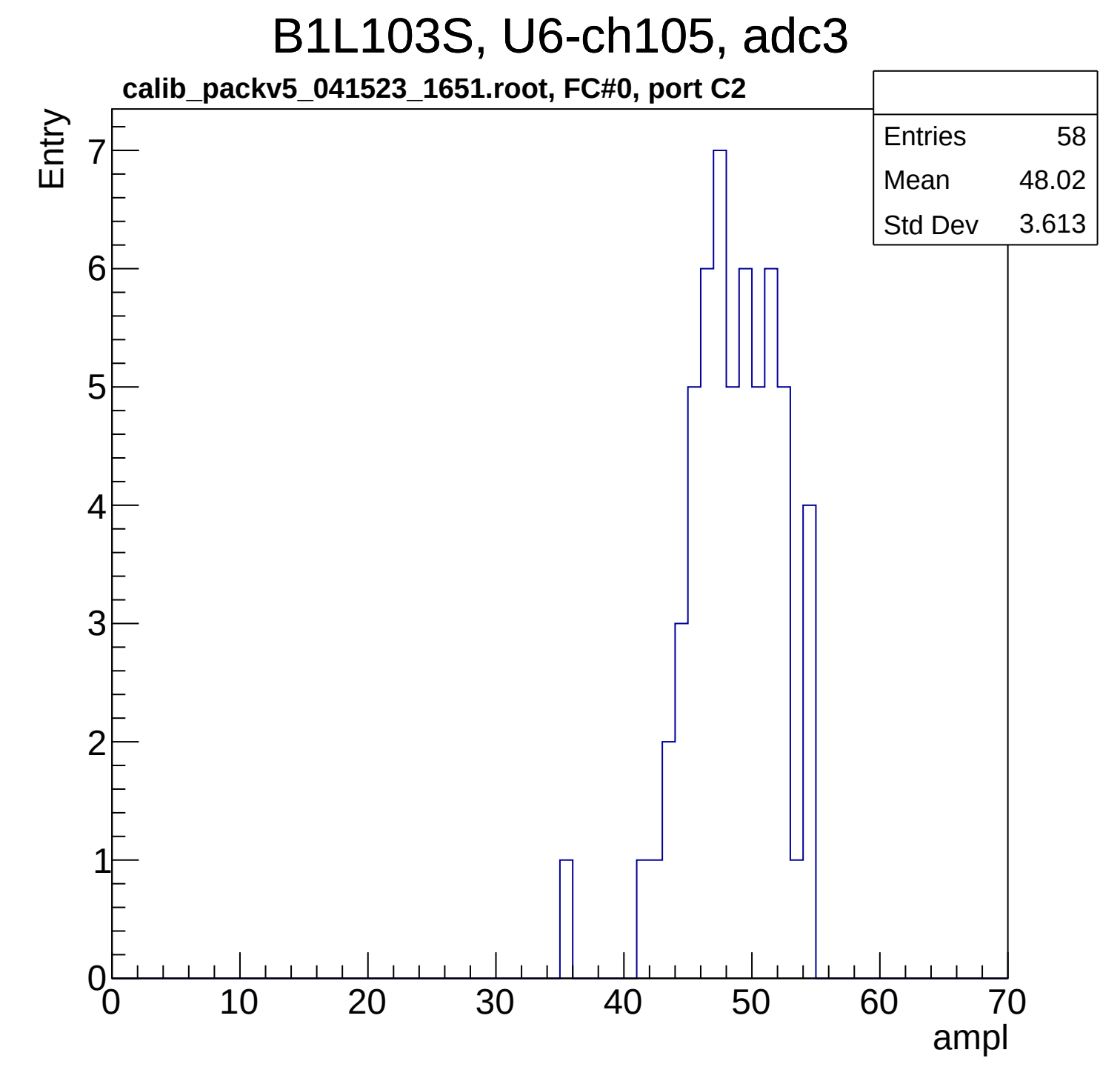
B1L103S, U6-ch105, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 48.02
Std Dev 3.613
Entry
ampl
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0
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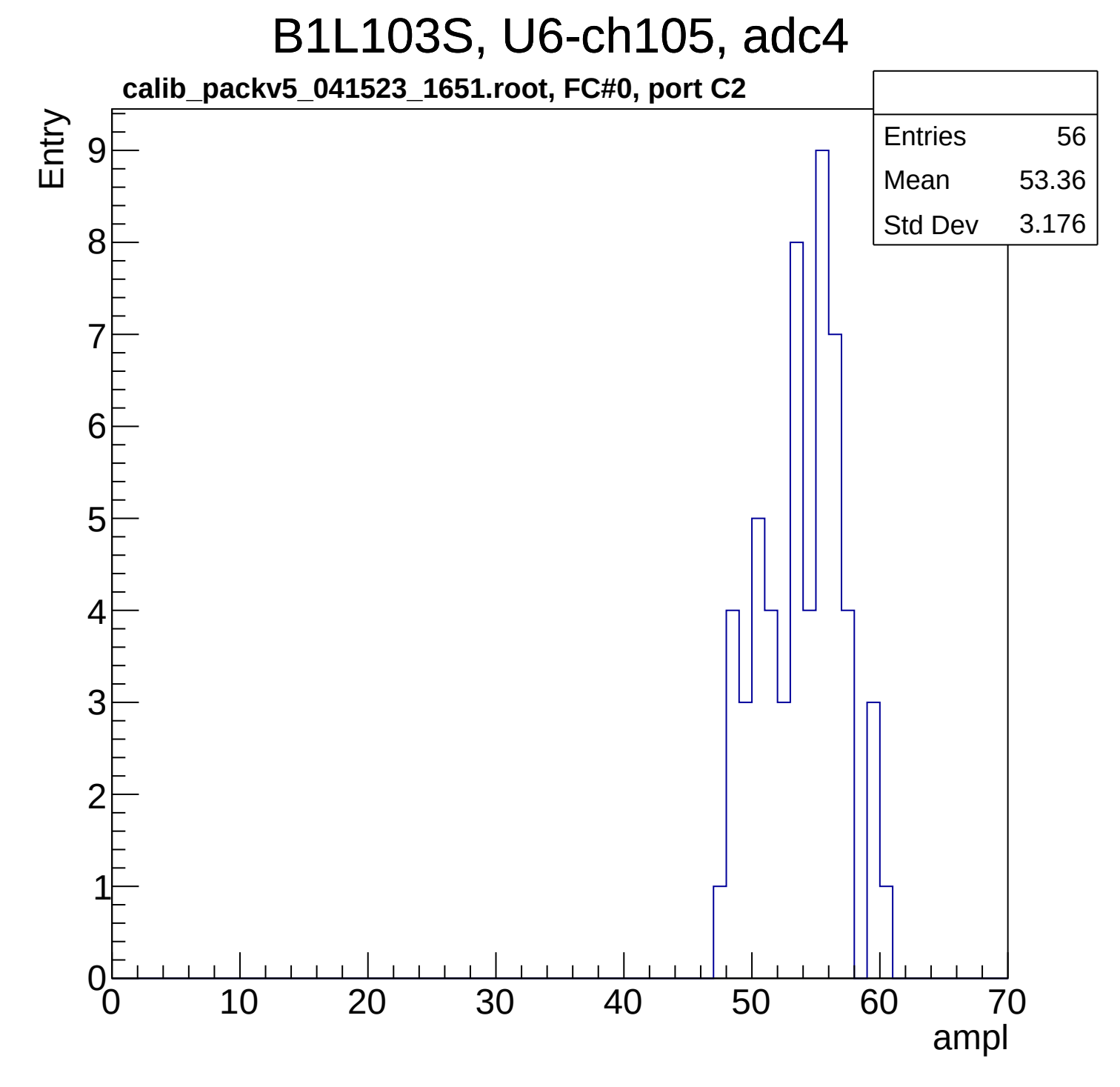
B1L103S, U6-ch105, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 53.36
Std Dev 3.176
Entry
ampl
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7
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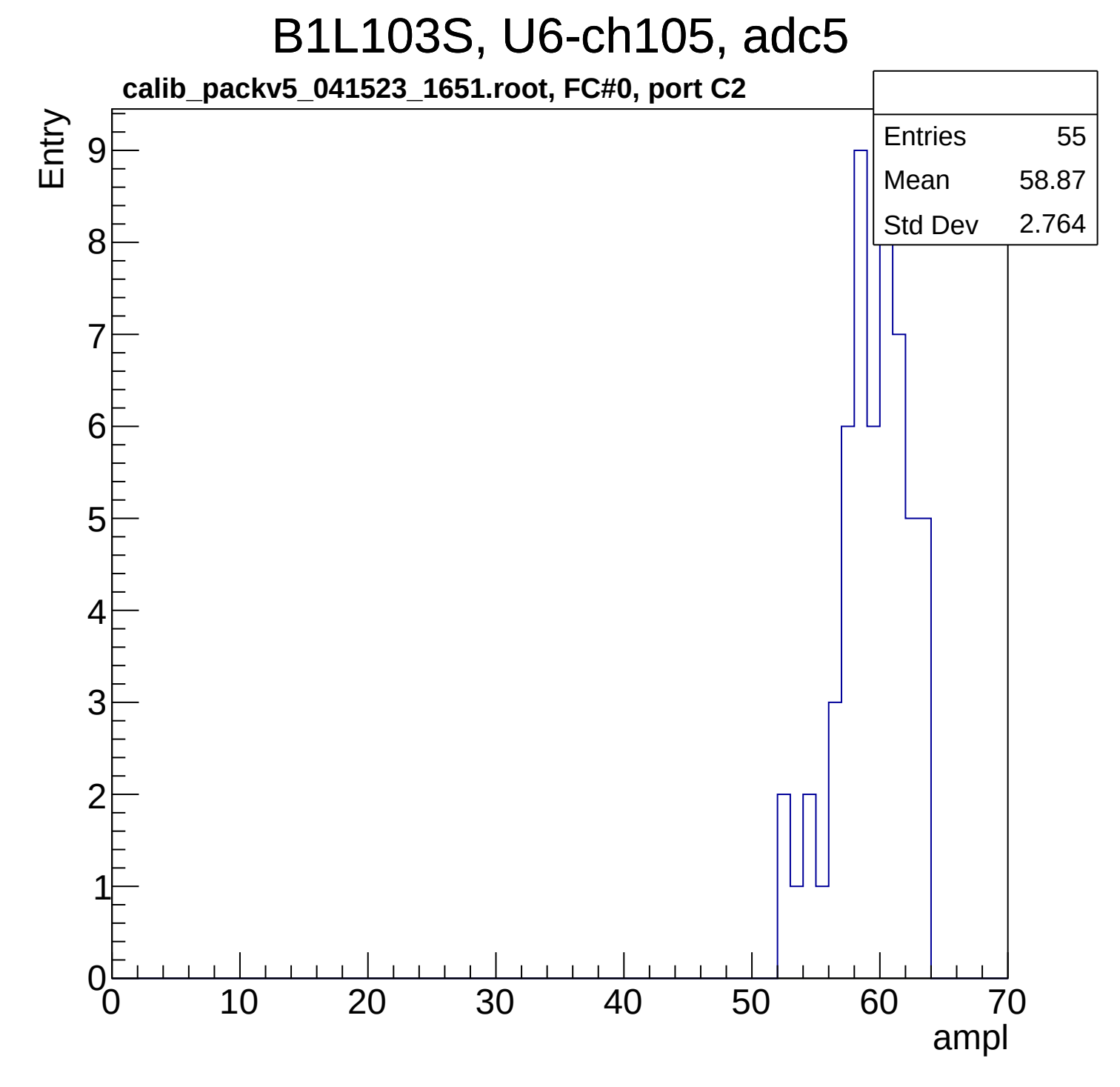
B1L103S, U6-ch105, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 58.87
Std Dev 2.764
Entry
ampl
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7
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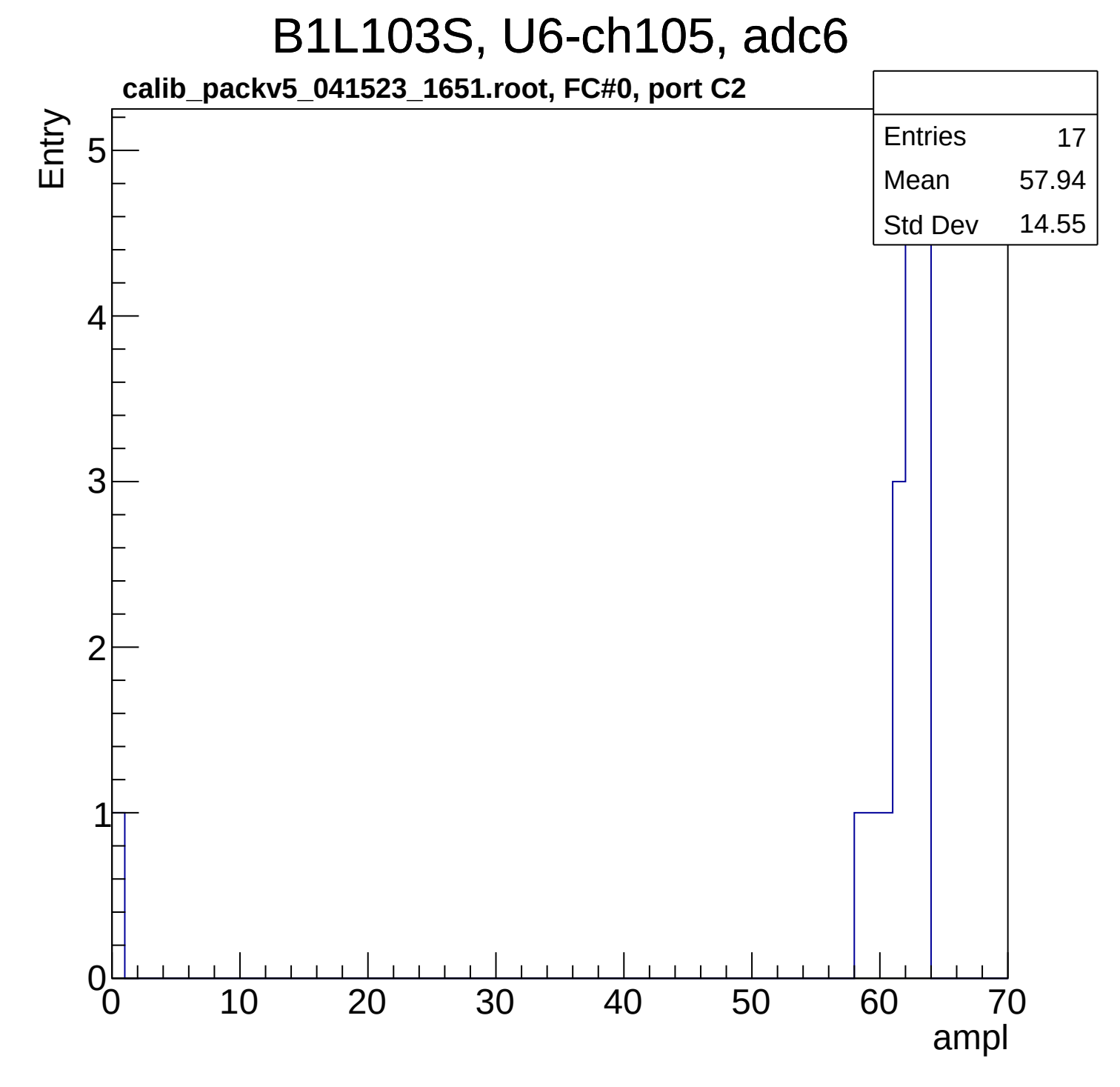
B1L103S, U6-ch105, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 57.94
Std Dev 14.55
Entry
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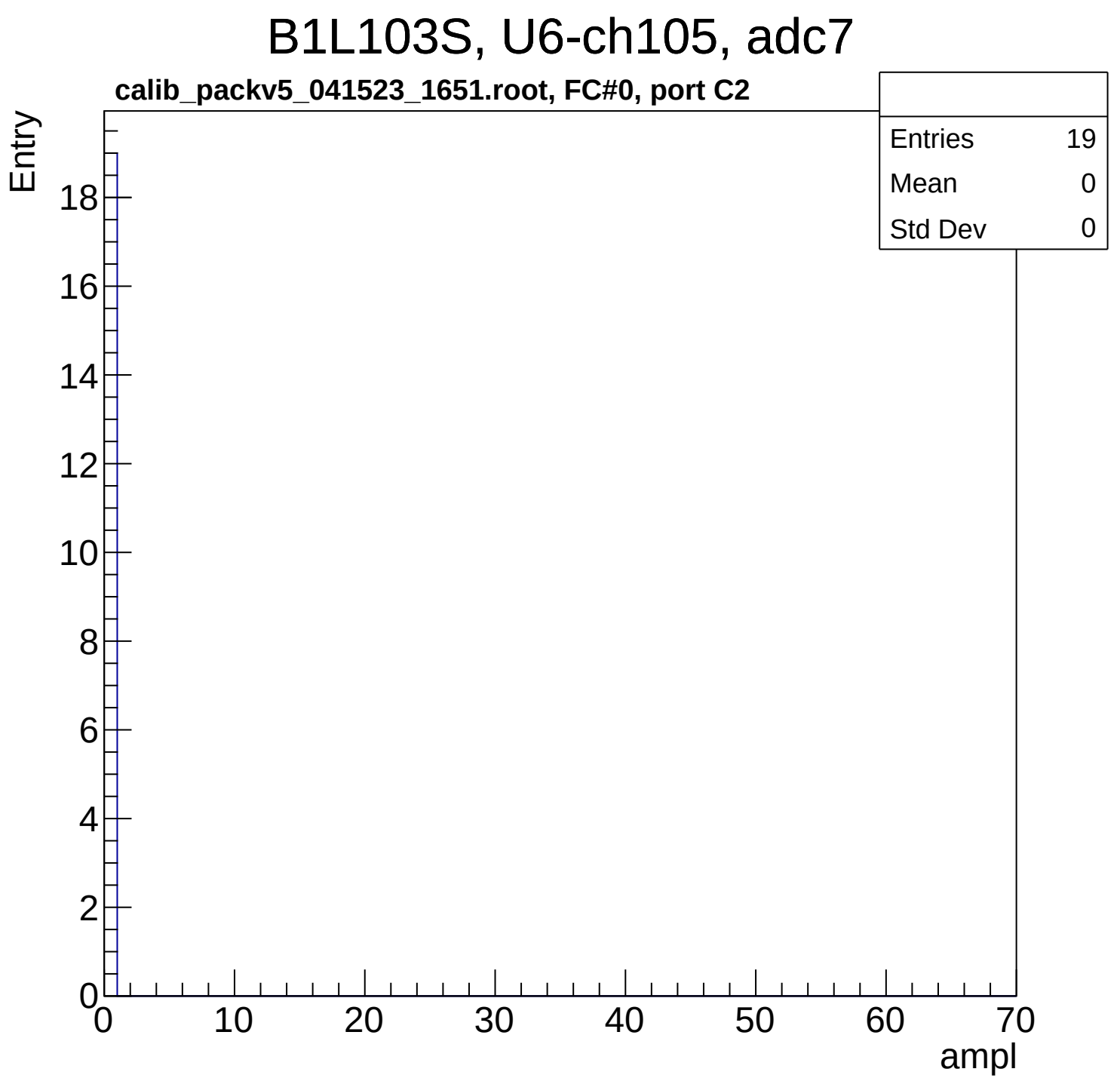
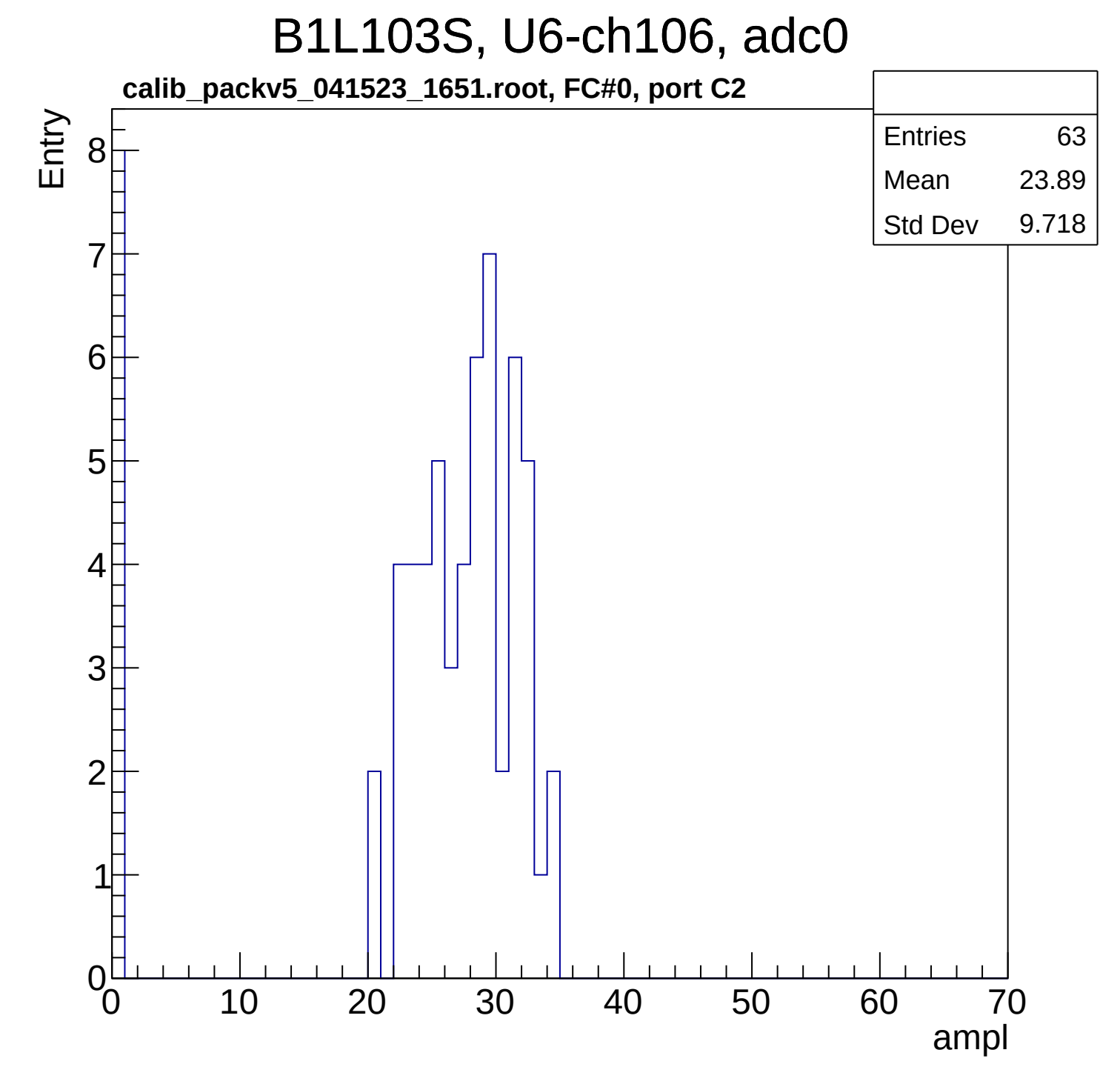
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch105, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch106, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 23.89
Std Dev 9.718
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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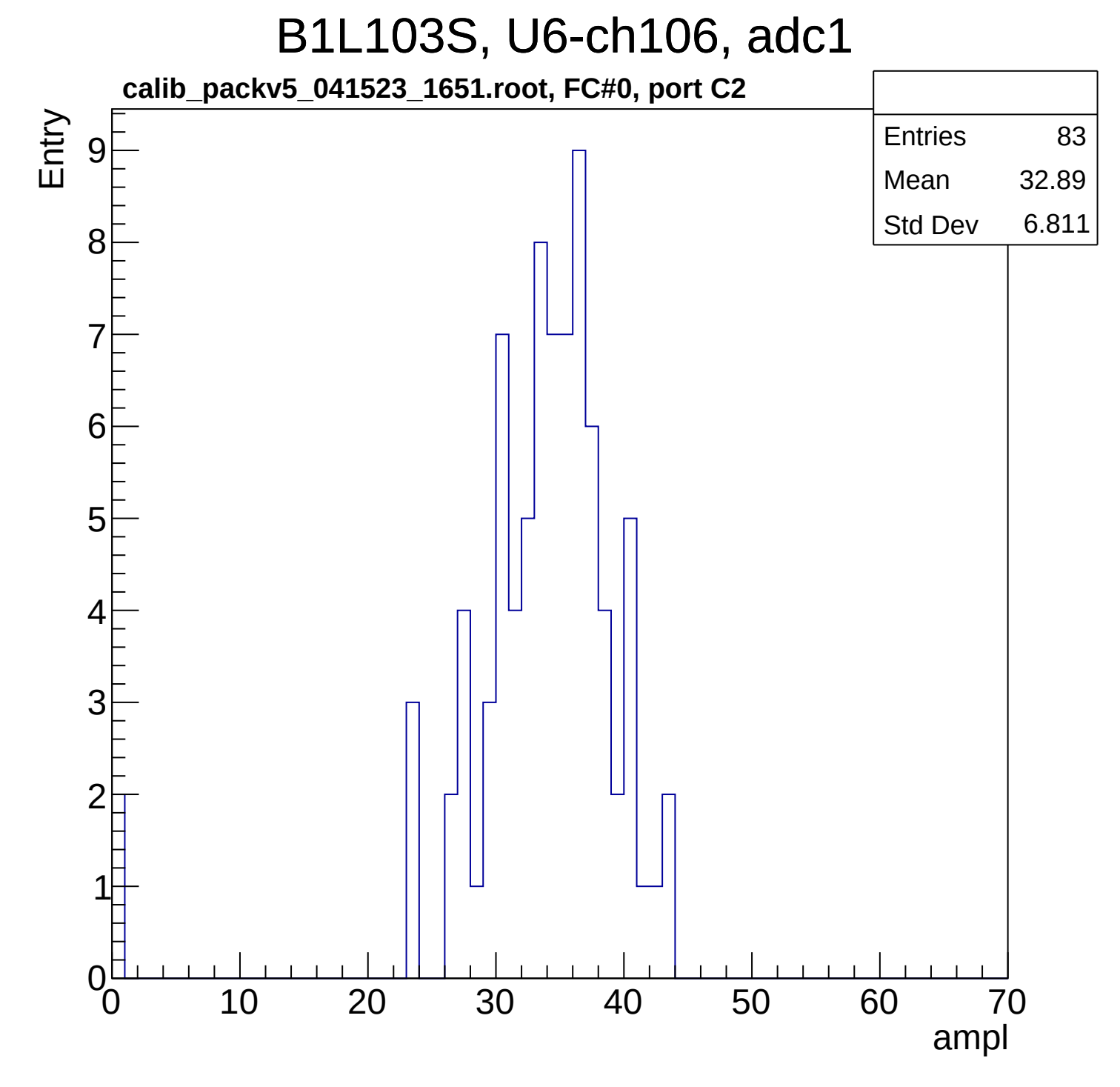
B1L103S, U6-ch106, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 32.89
Std Dev 6.811
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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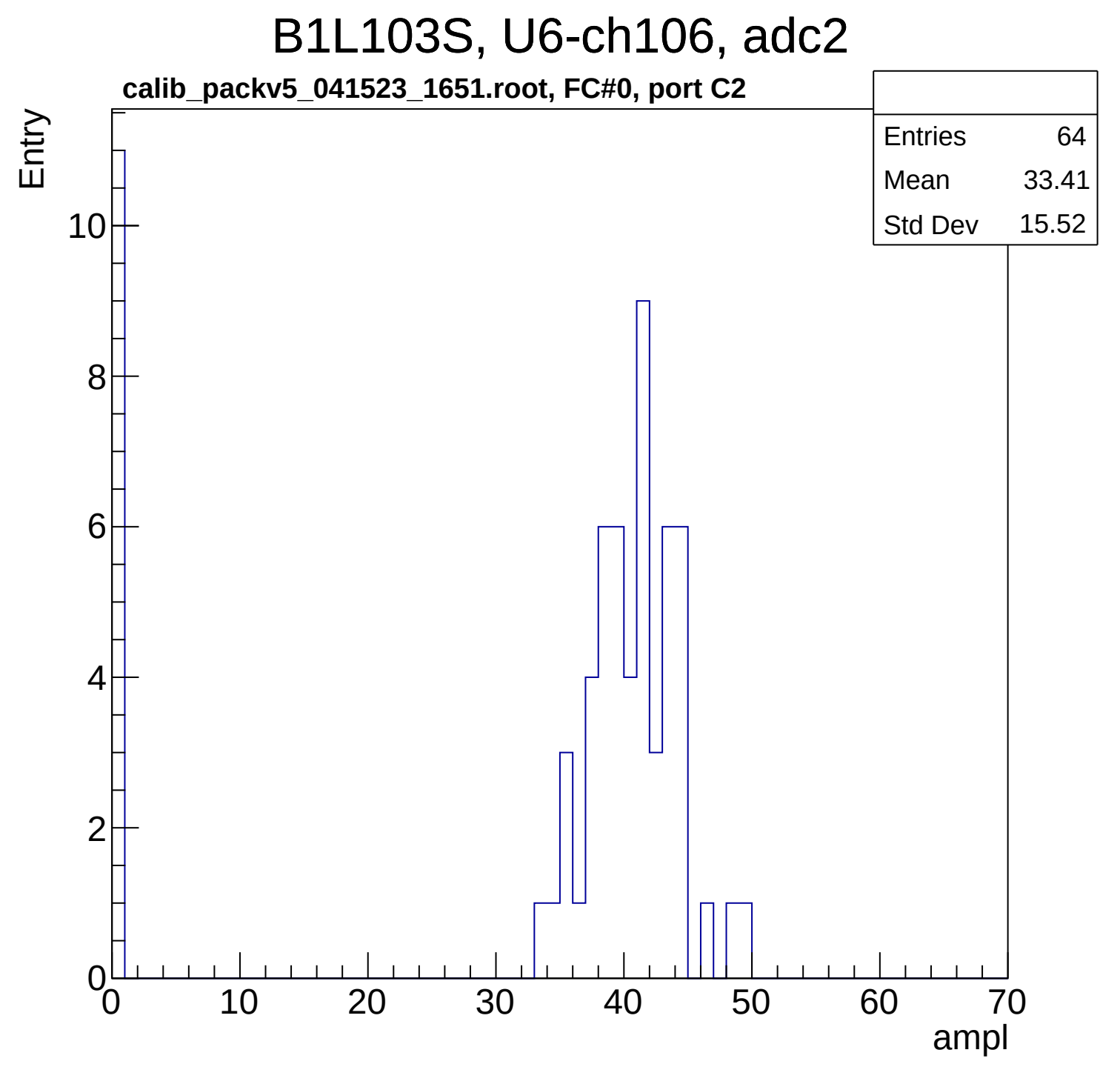
B1L103S, U6-ch106, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 33.41
Std Dev 15.52
Entry
ampl
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4
6
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0
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20
30
40
50
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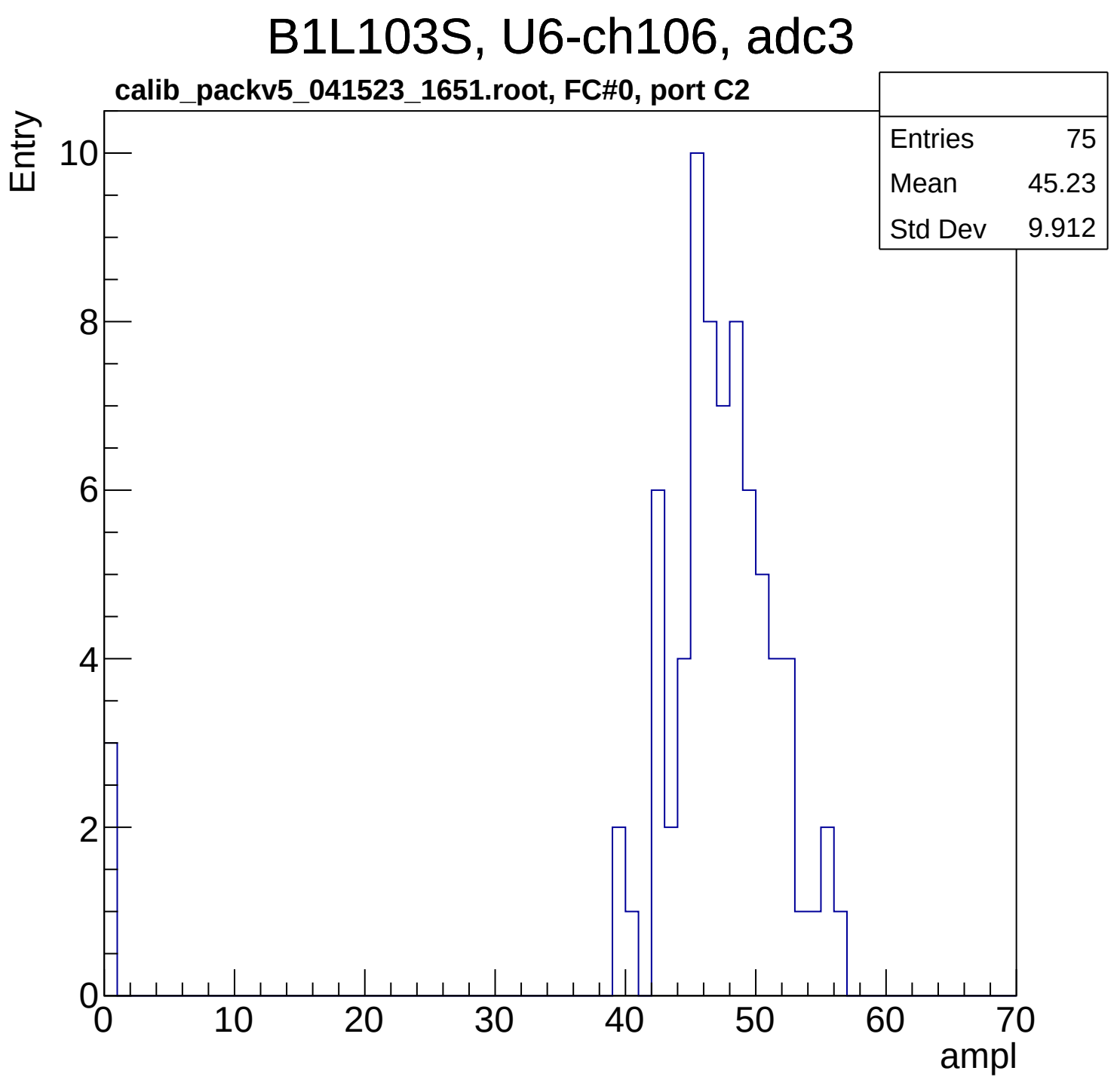
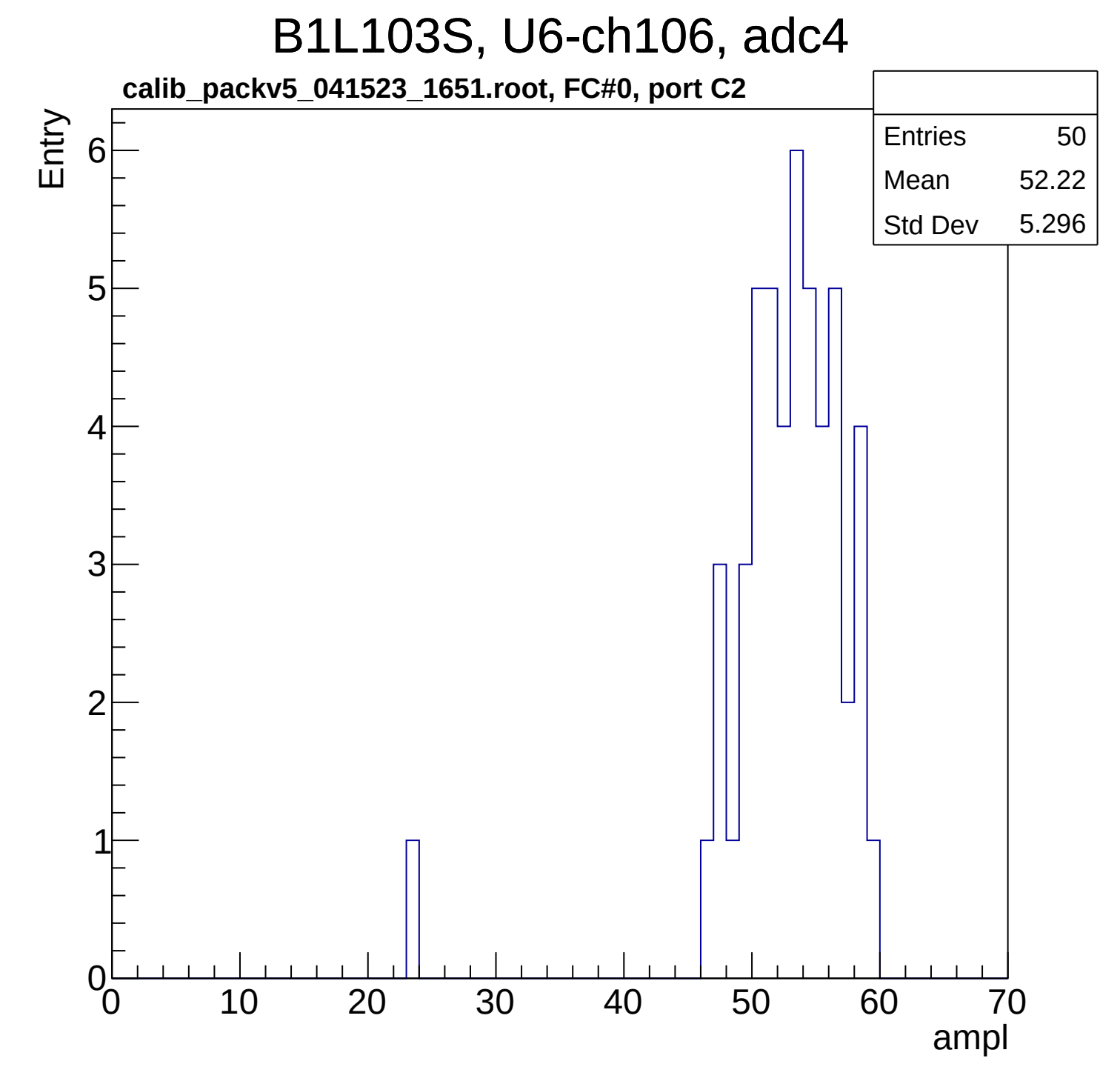

B1L103S, U6-ch106, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 45.23
Std Dev 9.912
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U6-ch106, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 52.22
Std Dev 5.296
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
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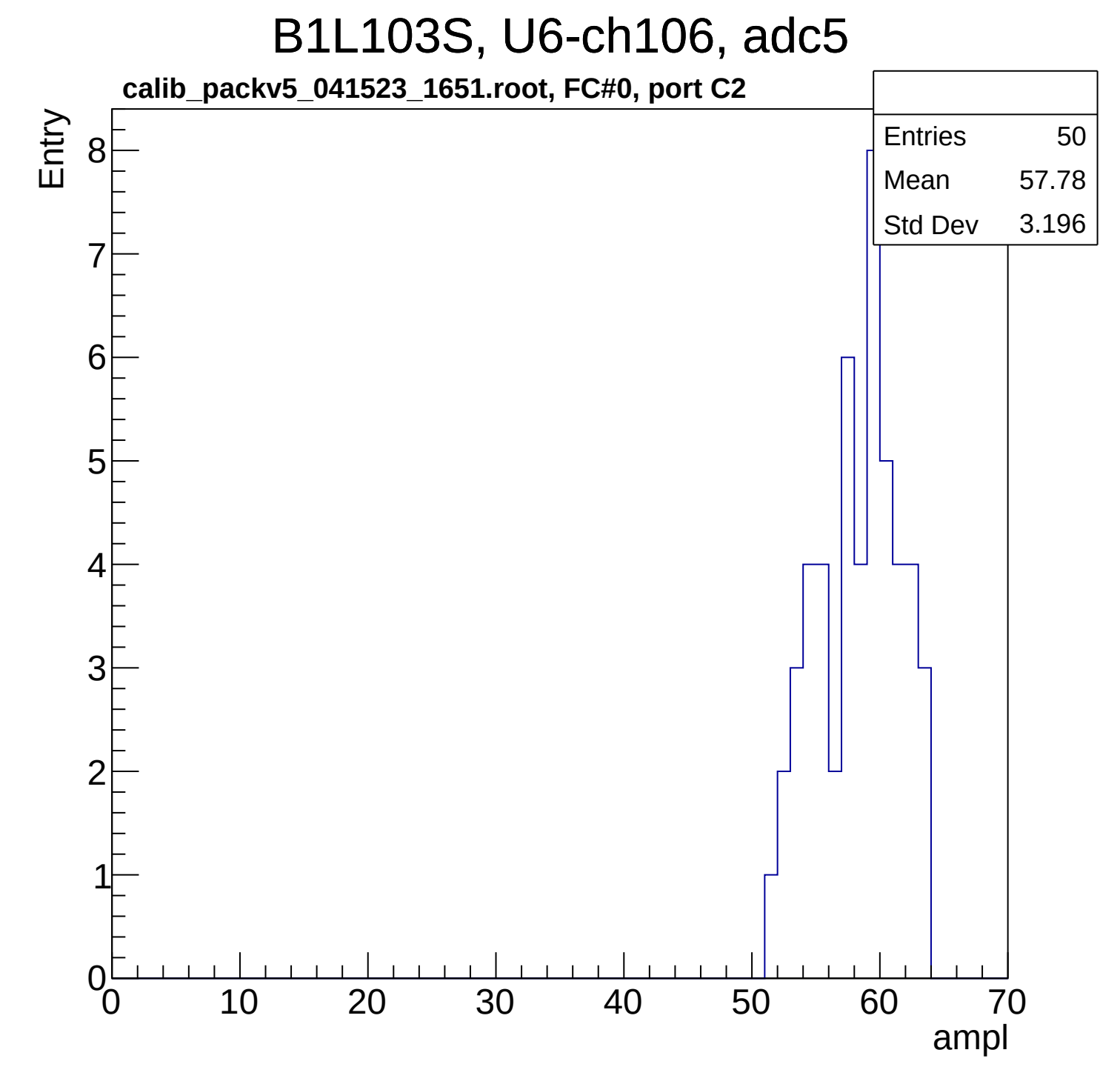
B1L103S, U6-ch106, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 57.78
Std Dev 3.196
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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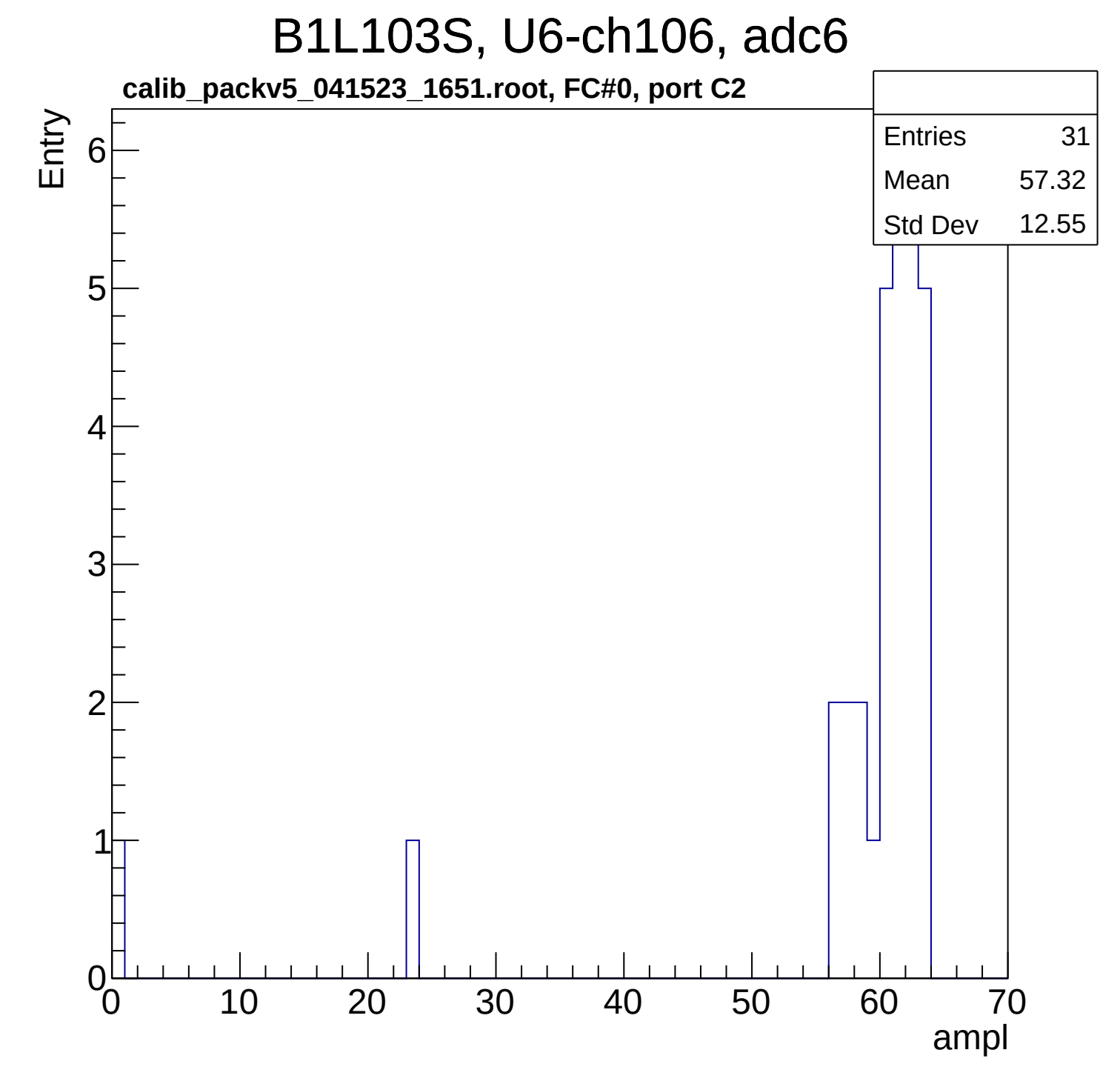
B1L103S, U6-ch106, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 57.32
Std Dev 12.55
Entry
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2
3
4
5
6
0
10
20
30
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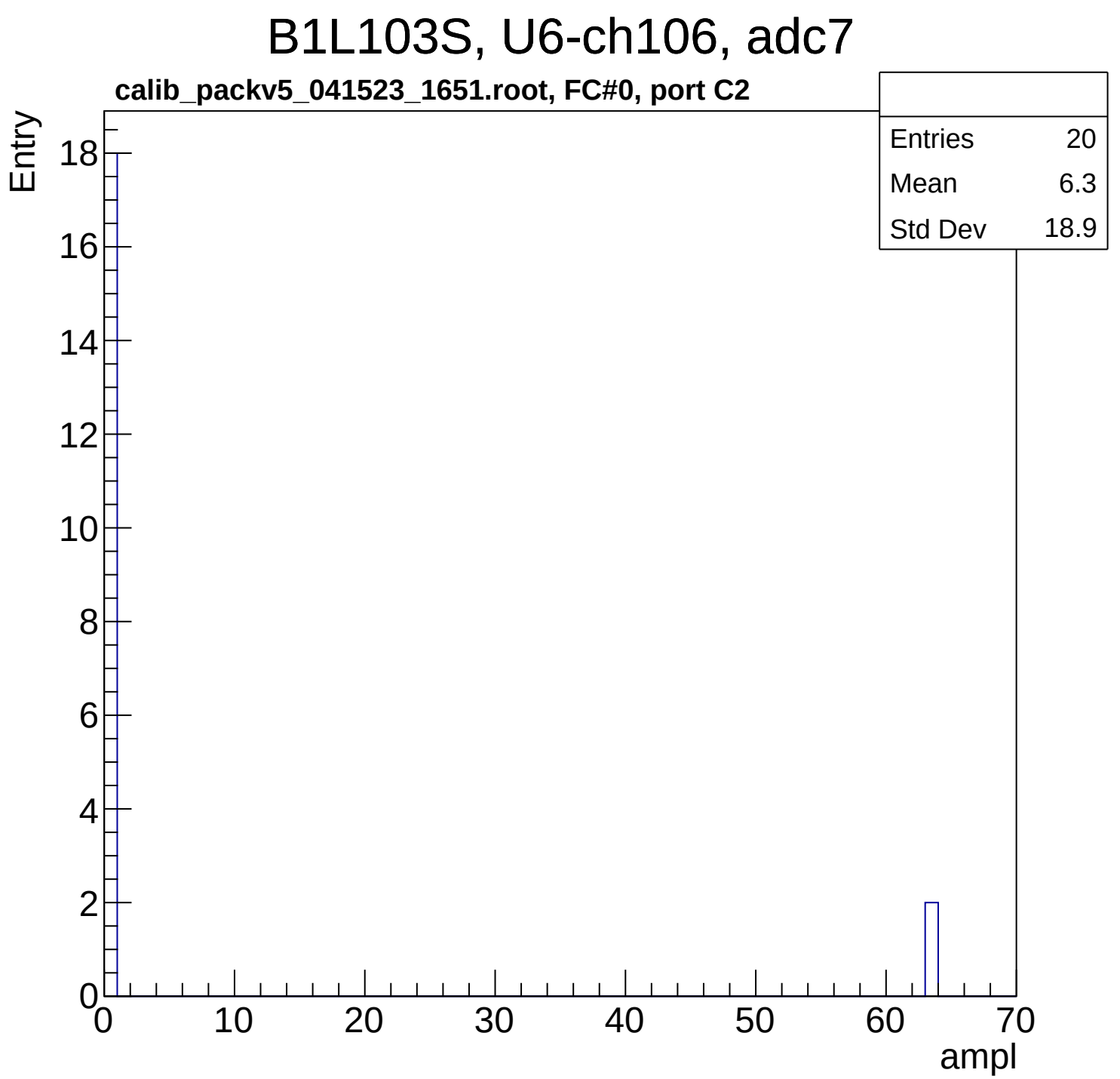
50
60
70
ampl


B1L103S, U6-ch106, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 6.3
Std Dev 18.9
Entry
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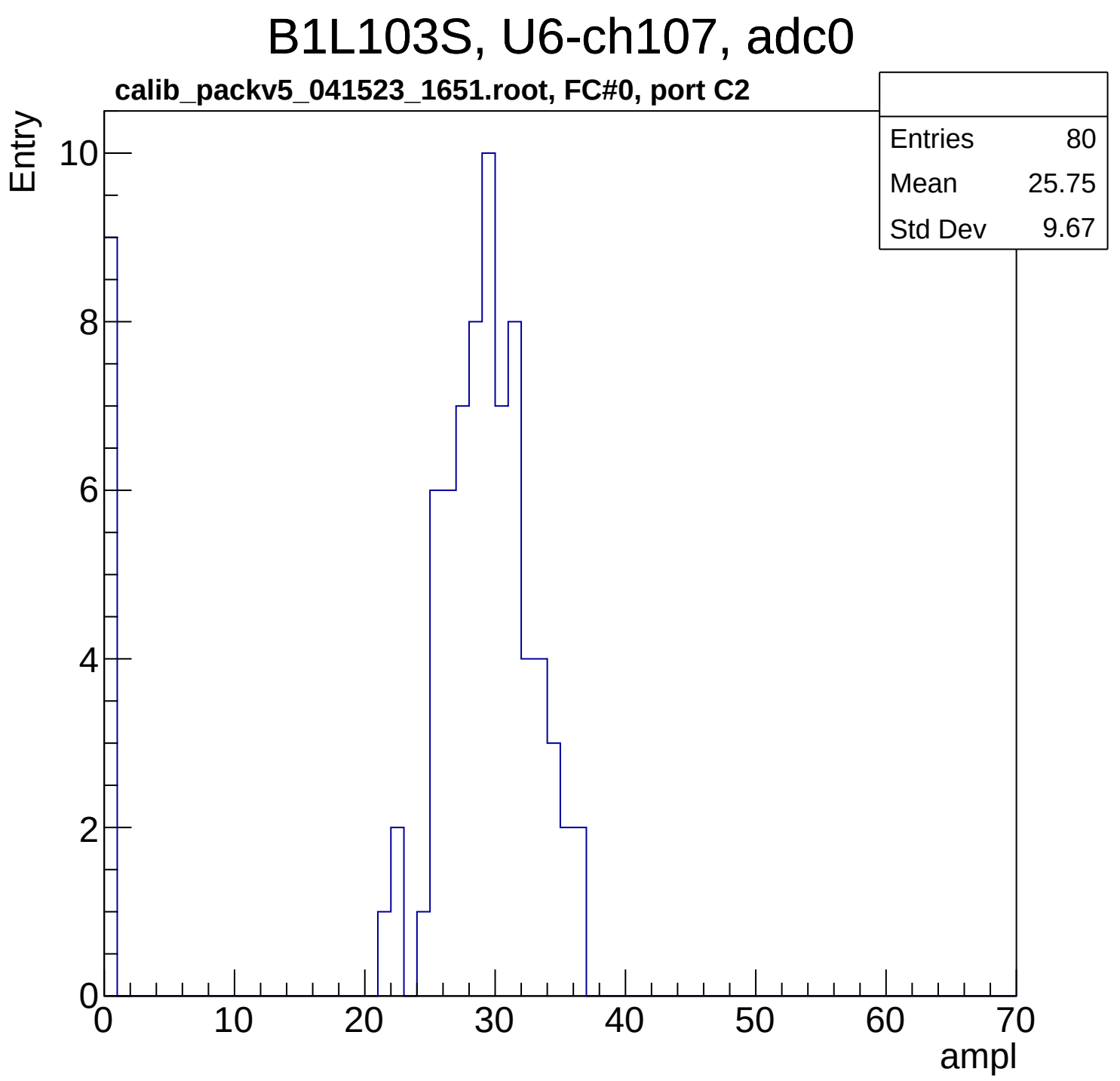
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch107, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 25.75
Std Dev 9.67
Entry
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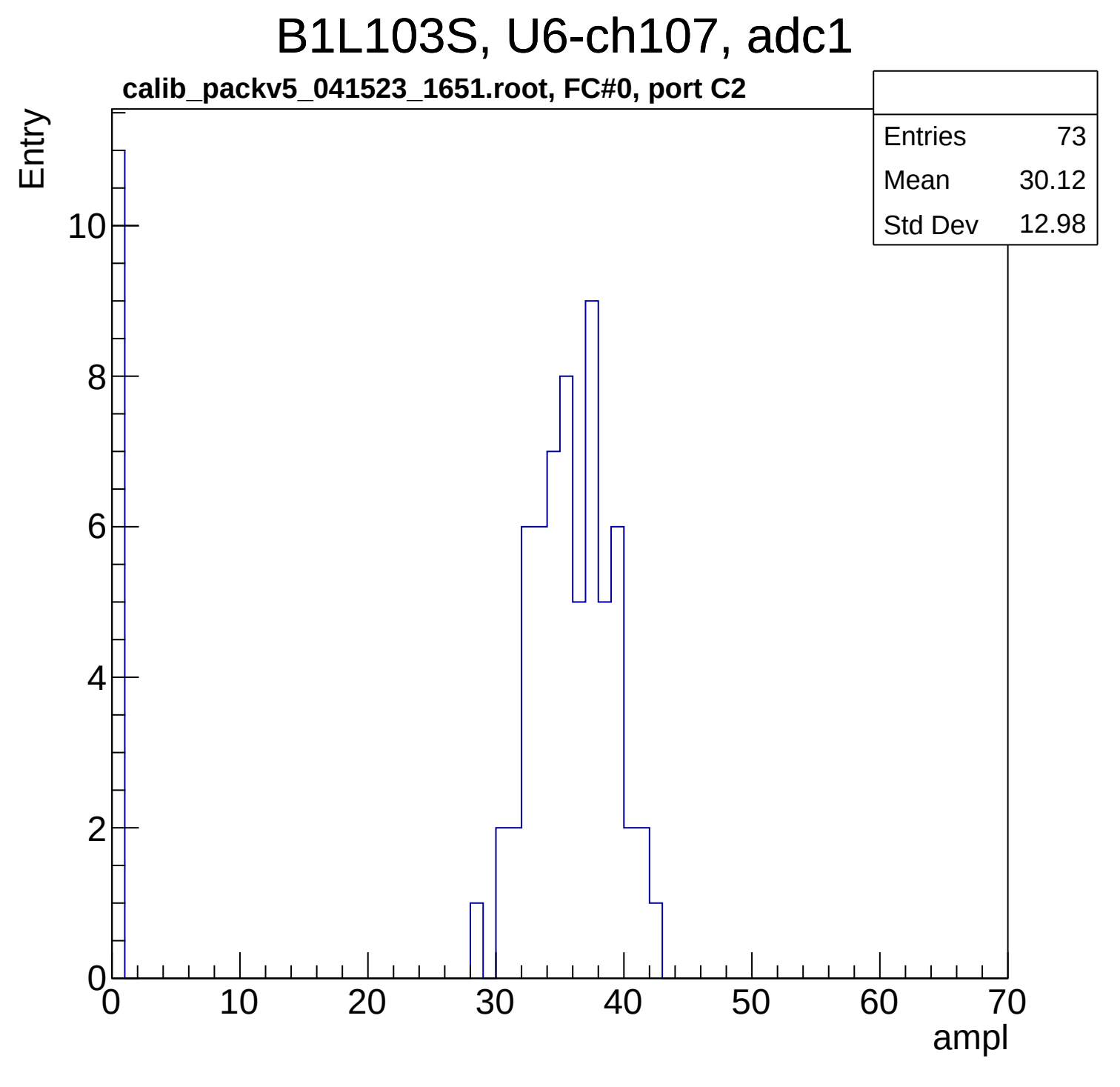
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch107, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 30.12
Std Dev 12.98
Entry
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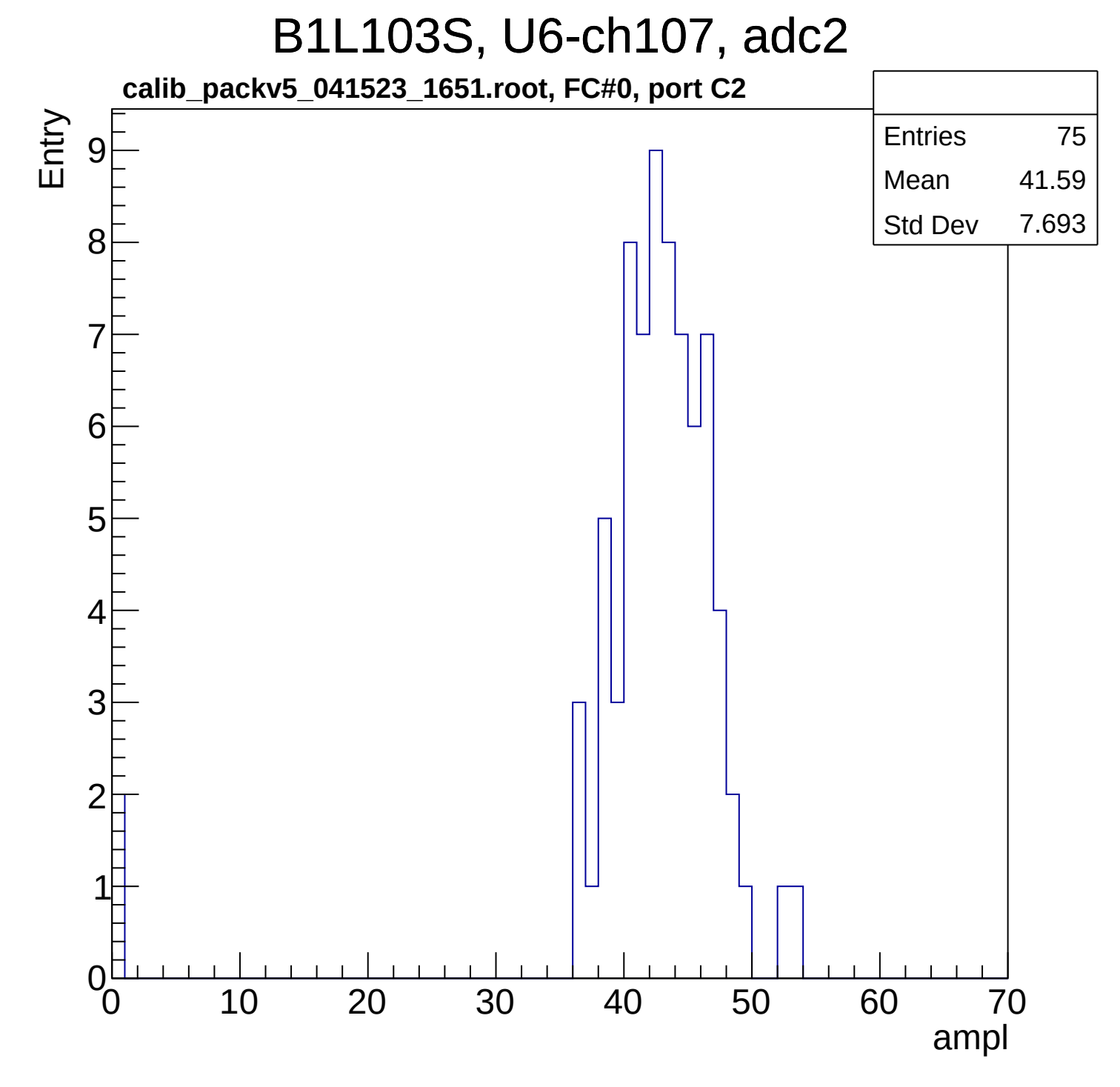
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch107, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 41.59
Std Dev 7.693
Entry
ampl
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3
4
5
6
7
8
9
0
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60
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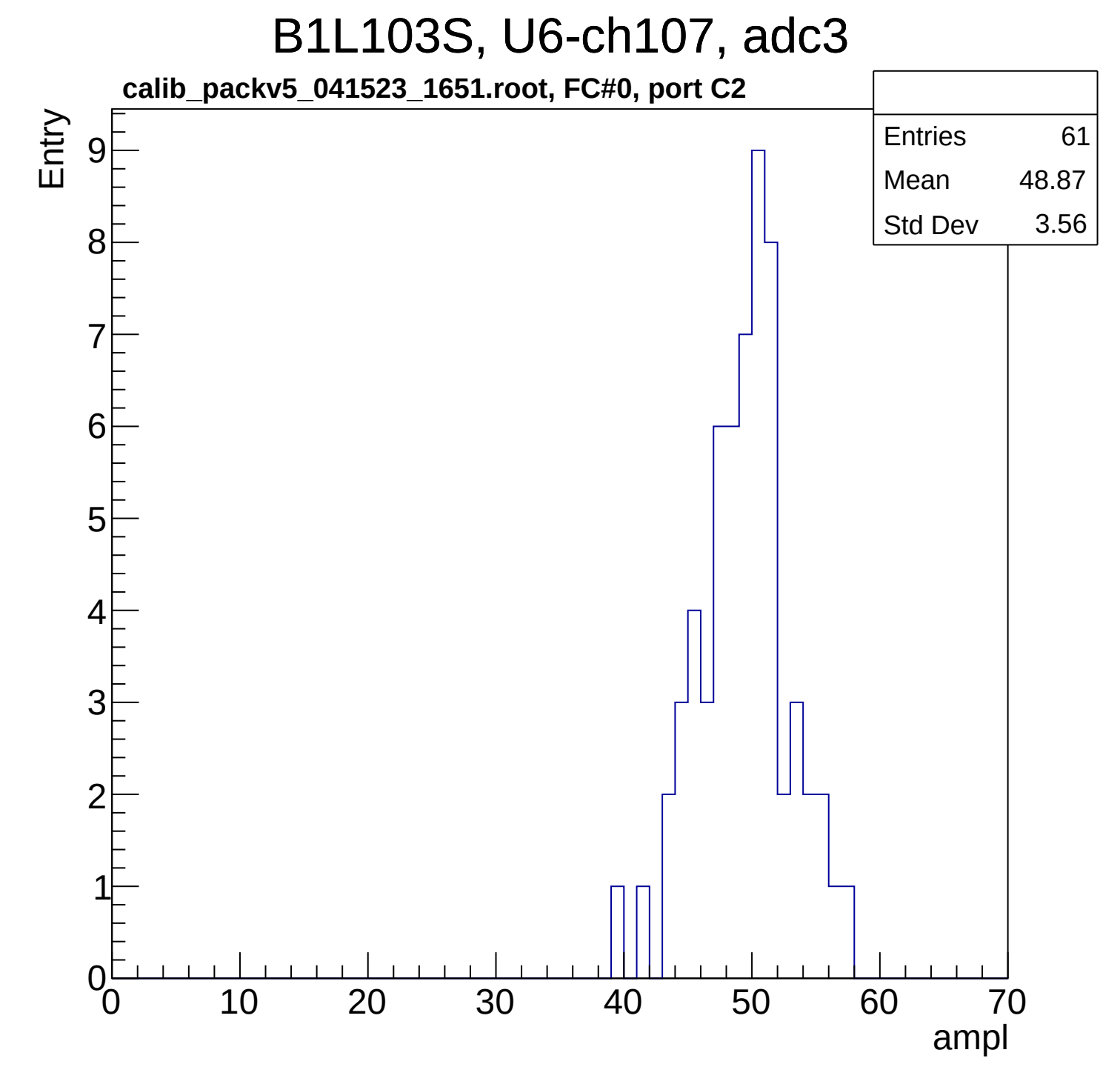
B1L103S, U6-ch107, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 48.87
Std Dev 3.56
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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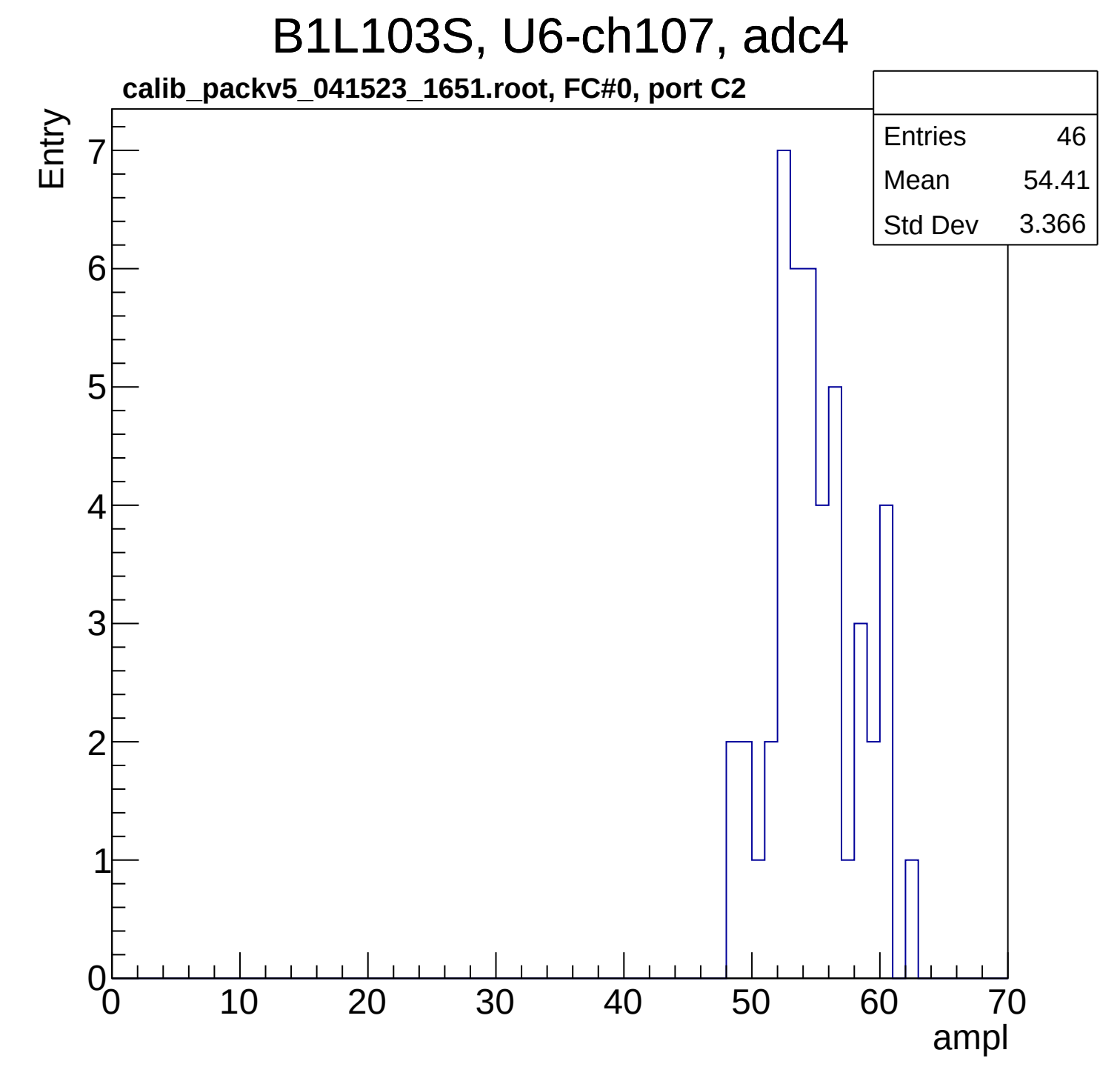
B1L103S, U6-ch107, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 54.41
Std Dev 3.366
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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40
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60
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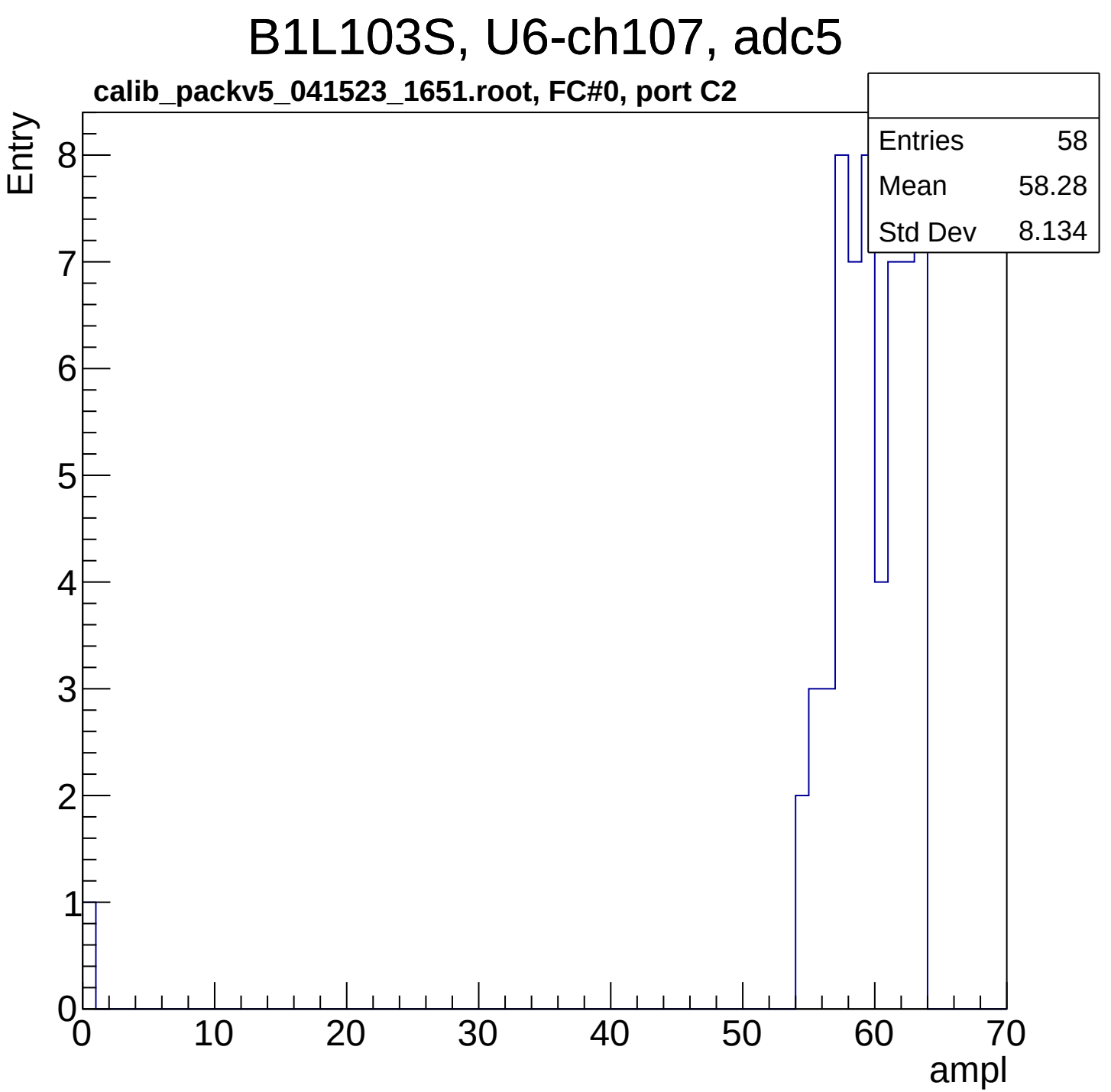
B1L103S, U6-ch107, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 58.28
Std Dev 8.134
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
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60
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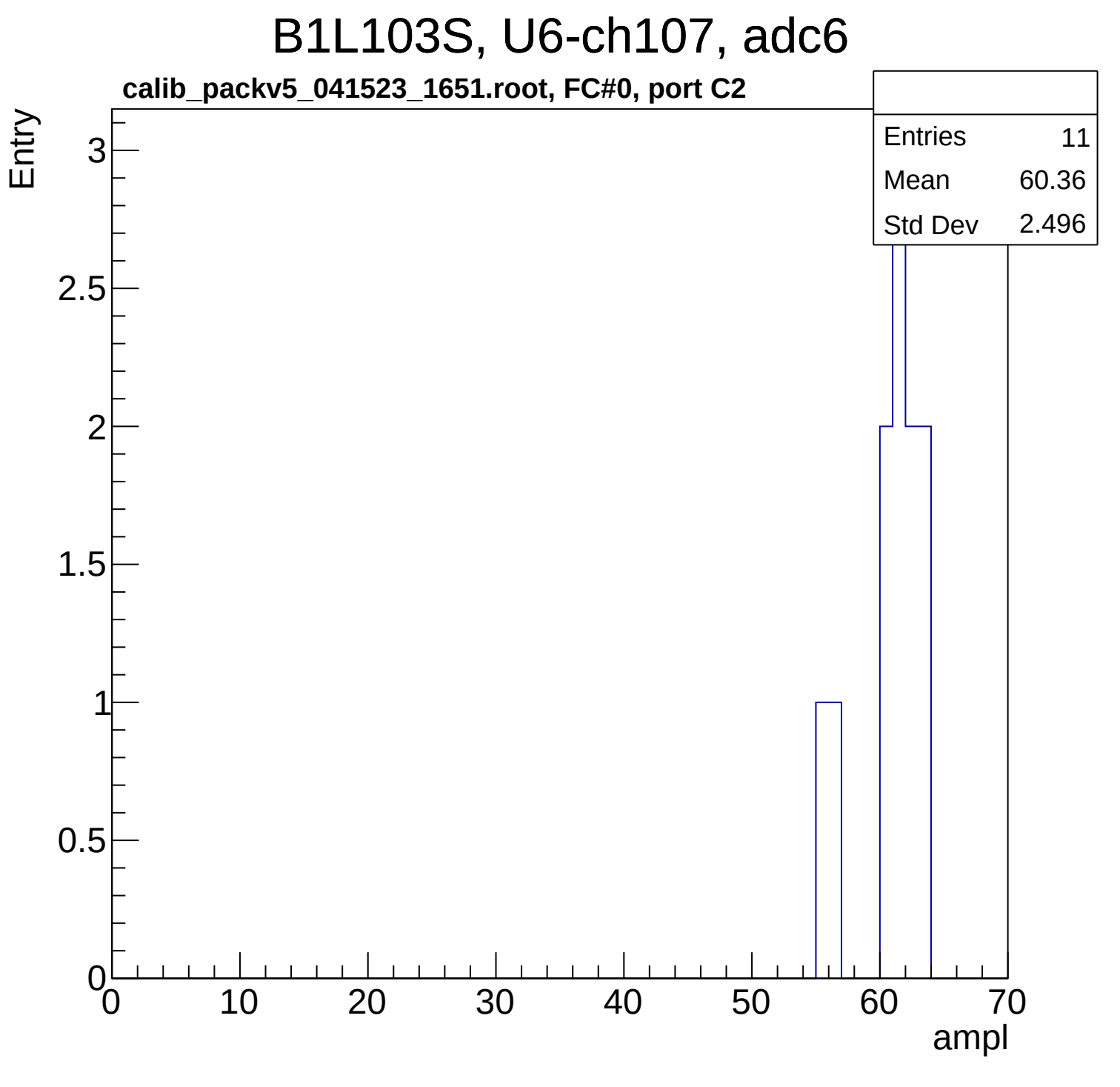
B1L103S, U6-ch107, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 60.36
Std Dev 2.496
Entry
ampl
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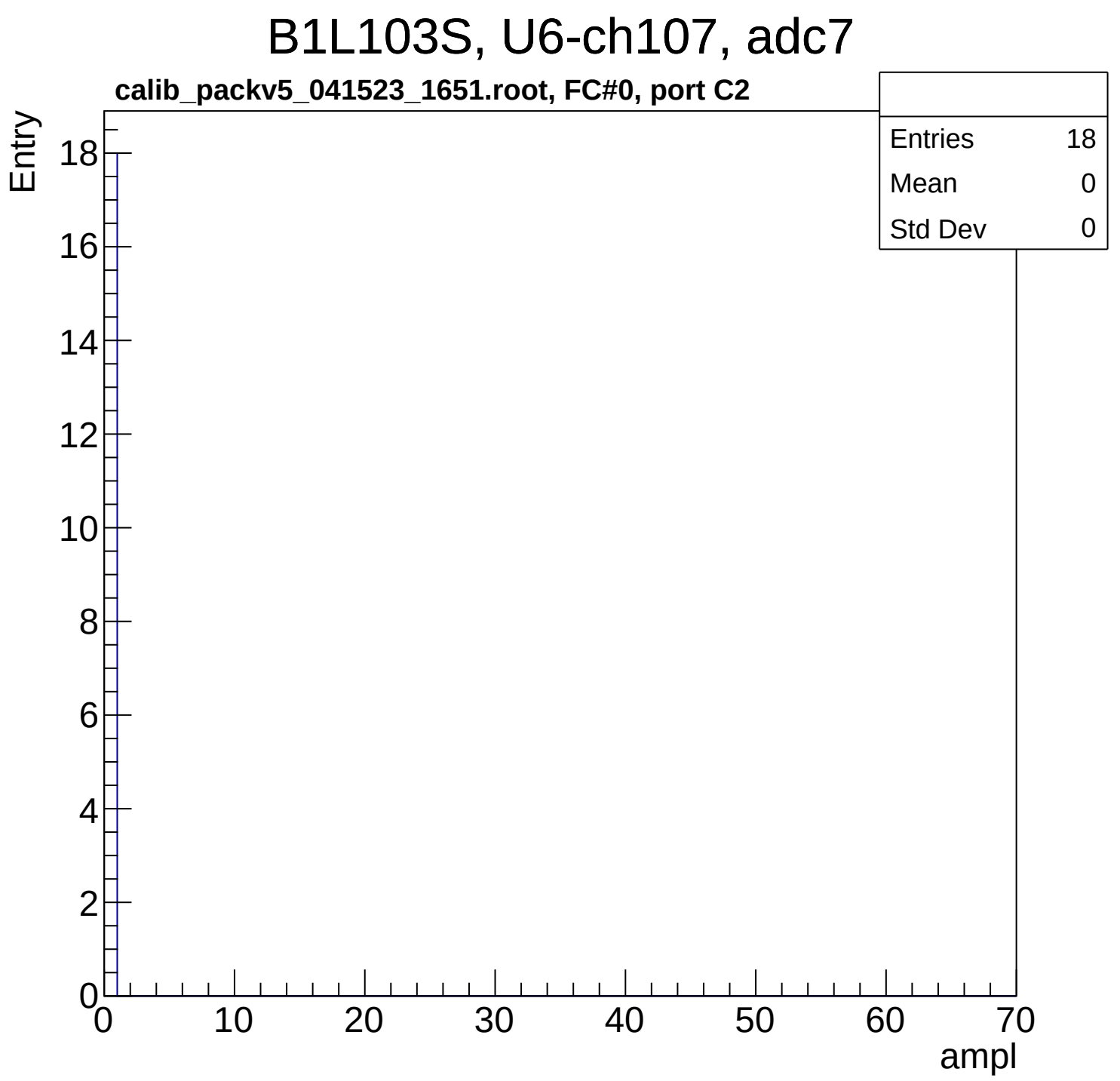
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U6-ch107, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
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8
10
12
14
16
18
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10
20
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50
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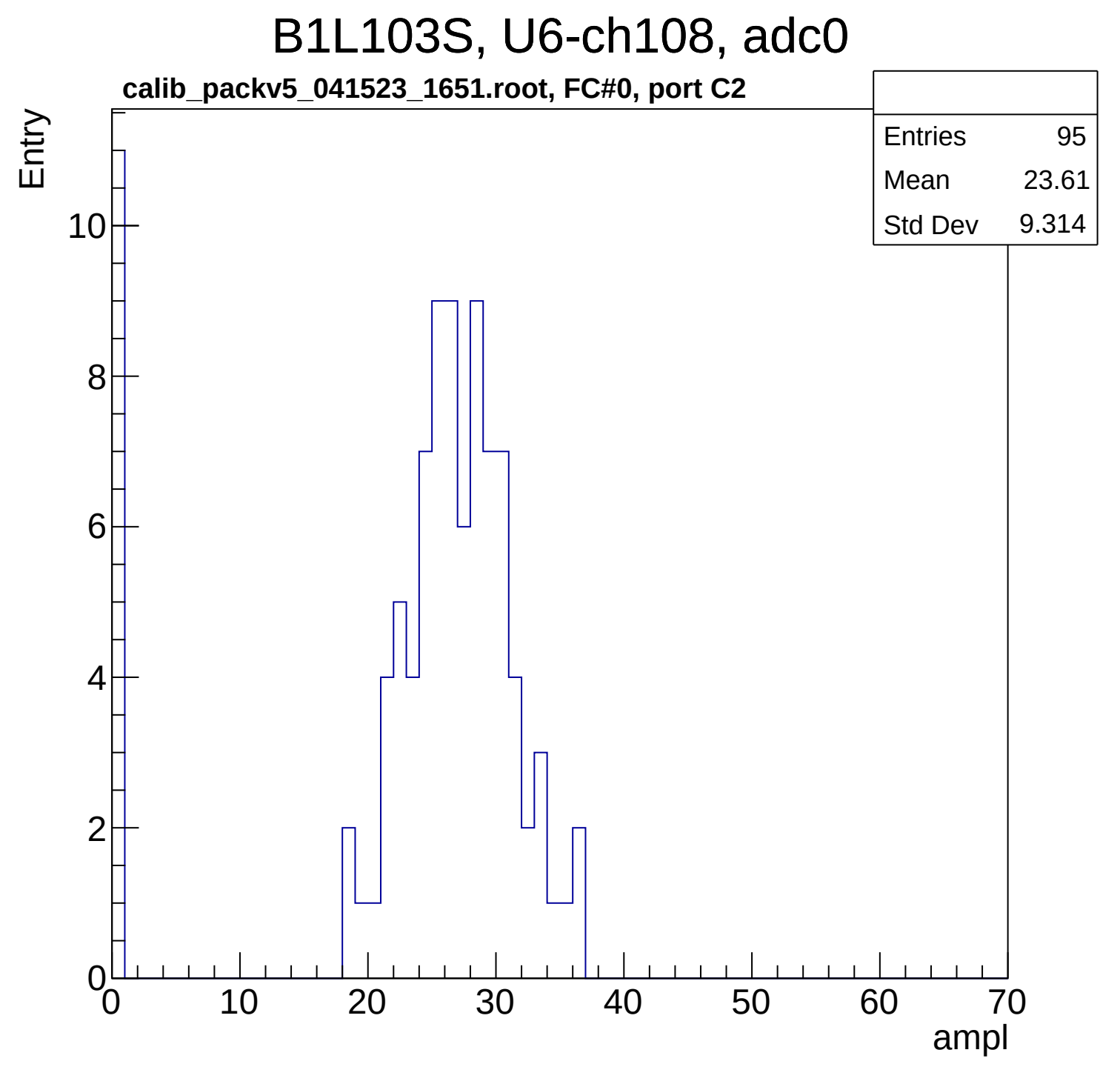
70
ampl


B1L103S, U6-ch108, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 23.61
Std Dev 9.314
Entry
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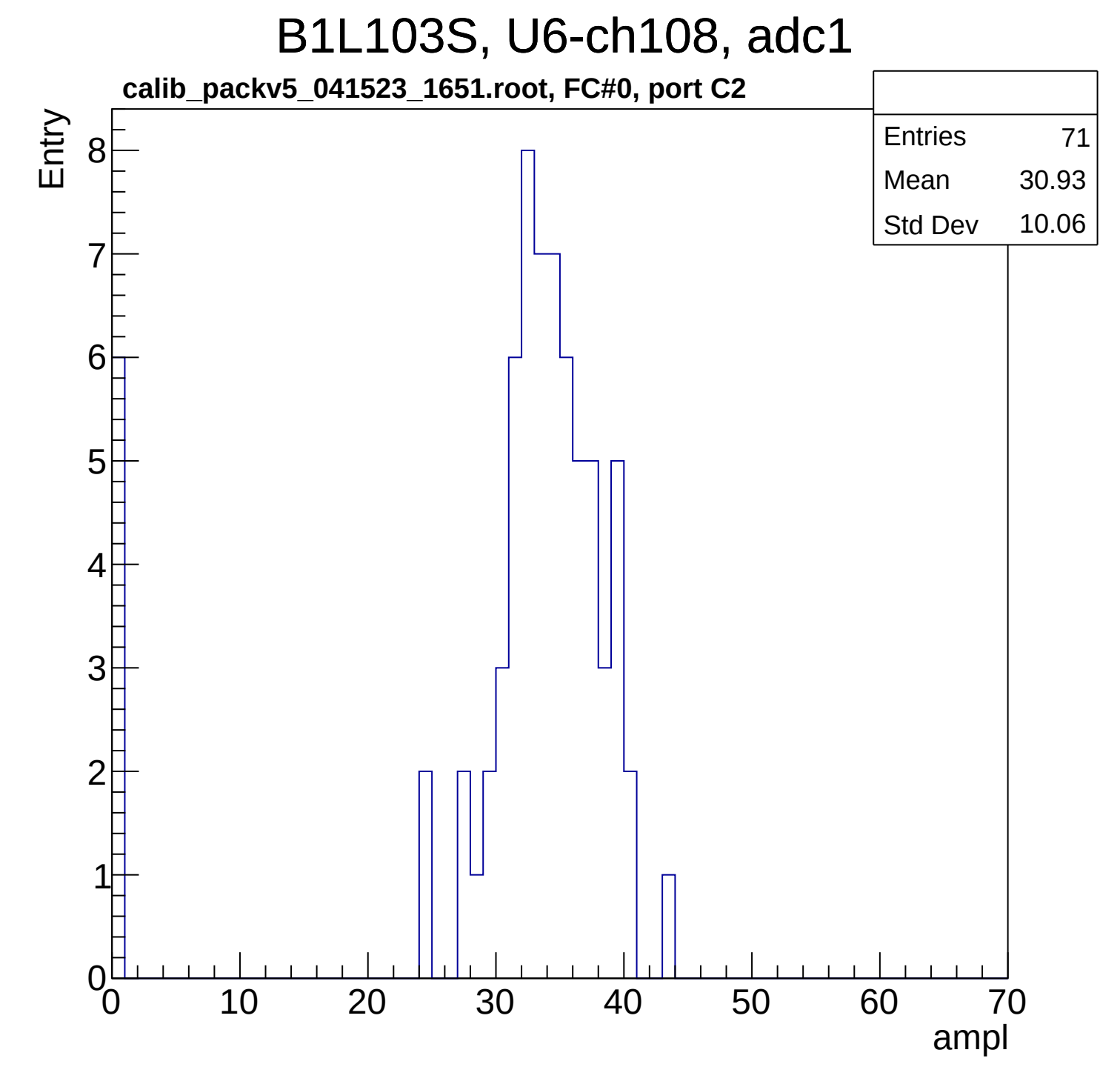
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch108, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 30.93
Std Dev 10.06
Entry
ampl
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1
2
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4
5
6
7
8
0
10
20
30
40
50
60
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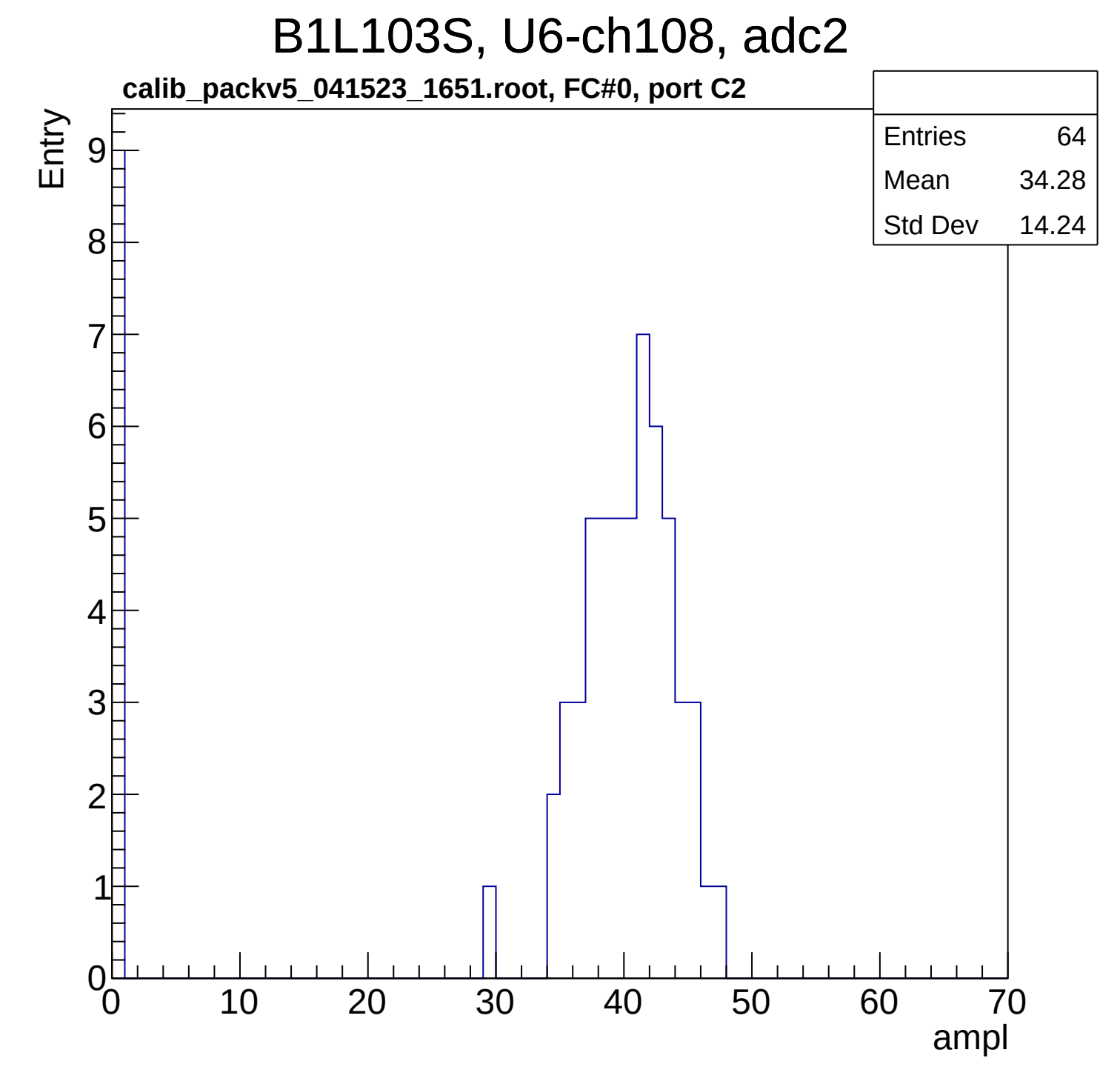
B1L103S, U6-ch108, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 34.28
Std Dev 14.24
Entry
ampl
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3
4
5
6
7
8
9
0
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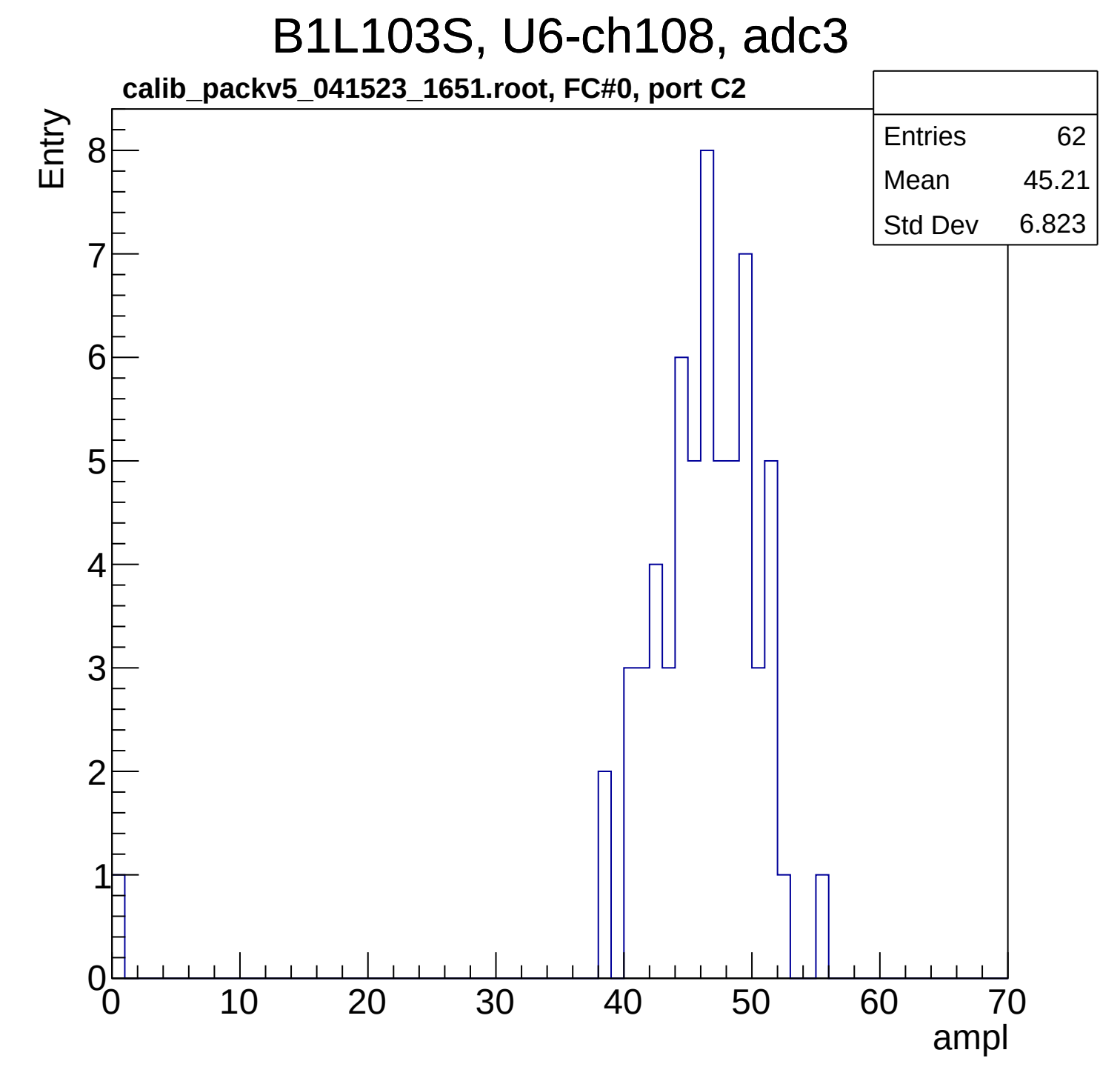
B1L103S, U6-ch108, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 45.21
Std Dev 6.823
Entry
ampl
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2
3
4
5
6
7
8
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10
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40
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60
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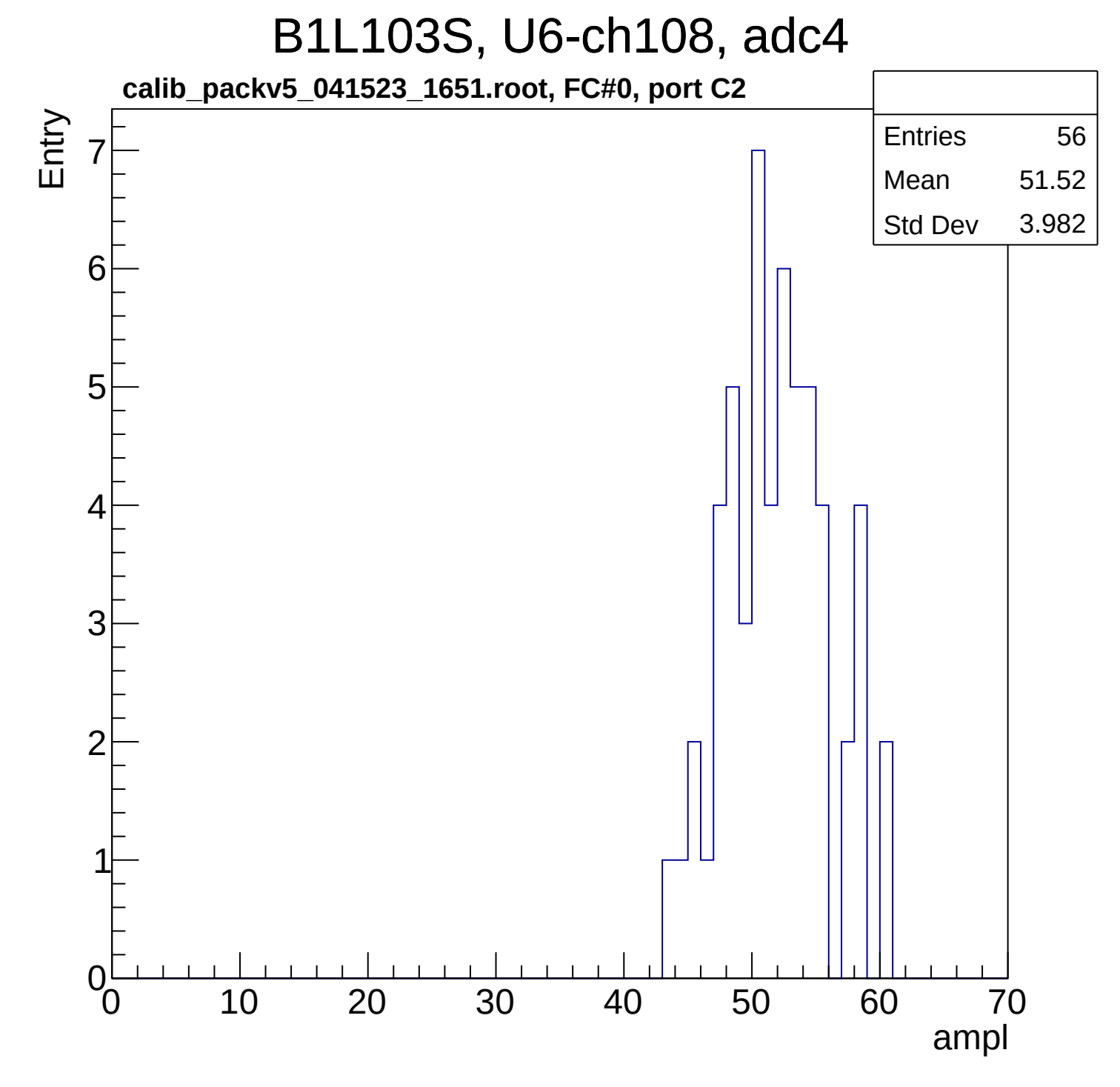
B1L103S, U6-ch108, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 51.52
Std Dev 3.982
Entry
ampl
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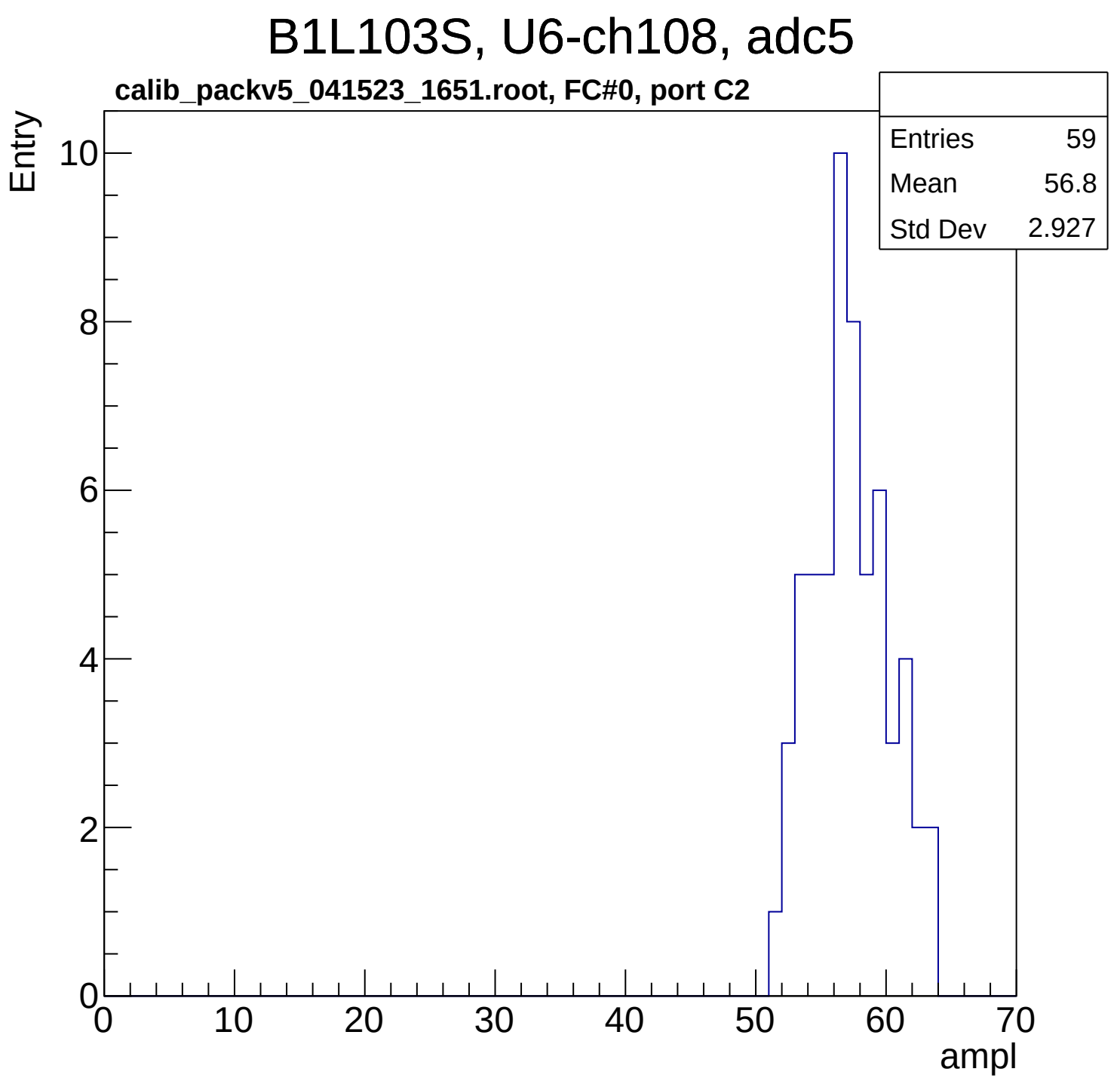
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U6-ch108, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 56.8
Std Dev 2.927
Entry
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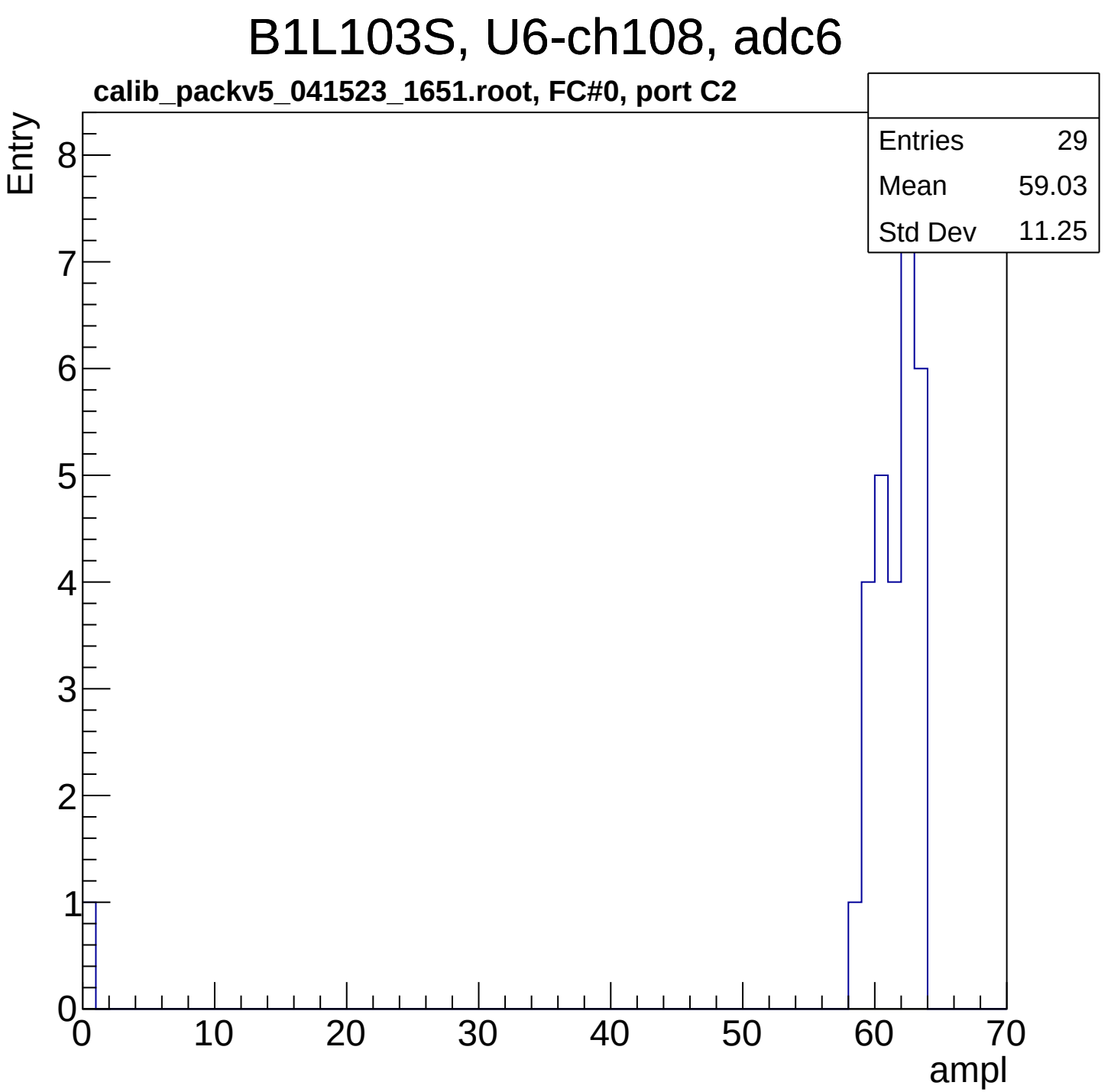
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch108, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 59.03
Std Dev 11.25
Entry
0
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2
3
4
5
6
7
8
0
10
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50
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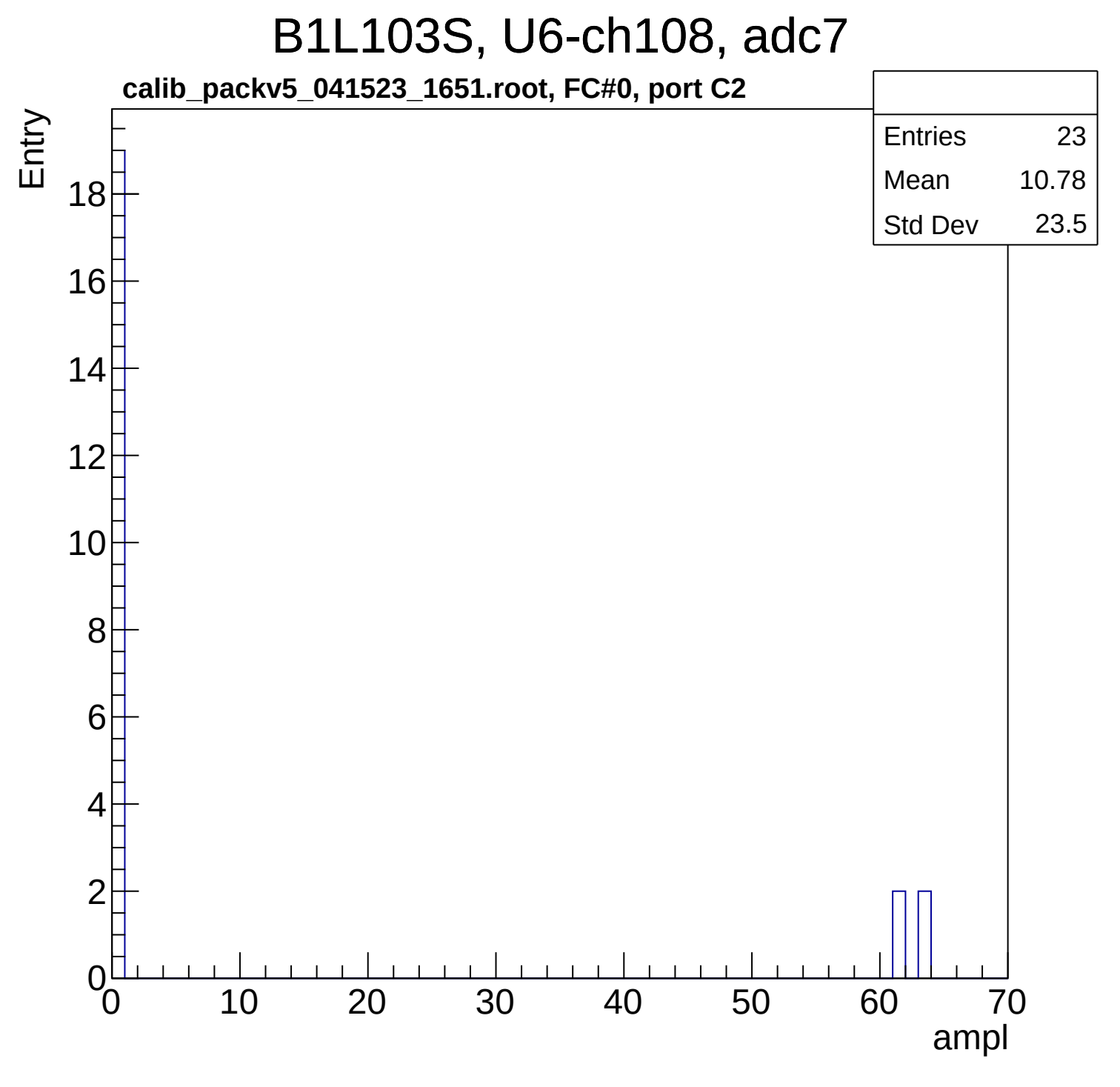
ampl


B1L103S, U6-ch108, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 10.78
Std Dev 23.5
Entry
0
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6
8
10
12
14
16
18
0
10
20
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50
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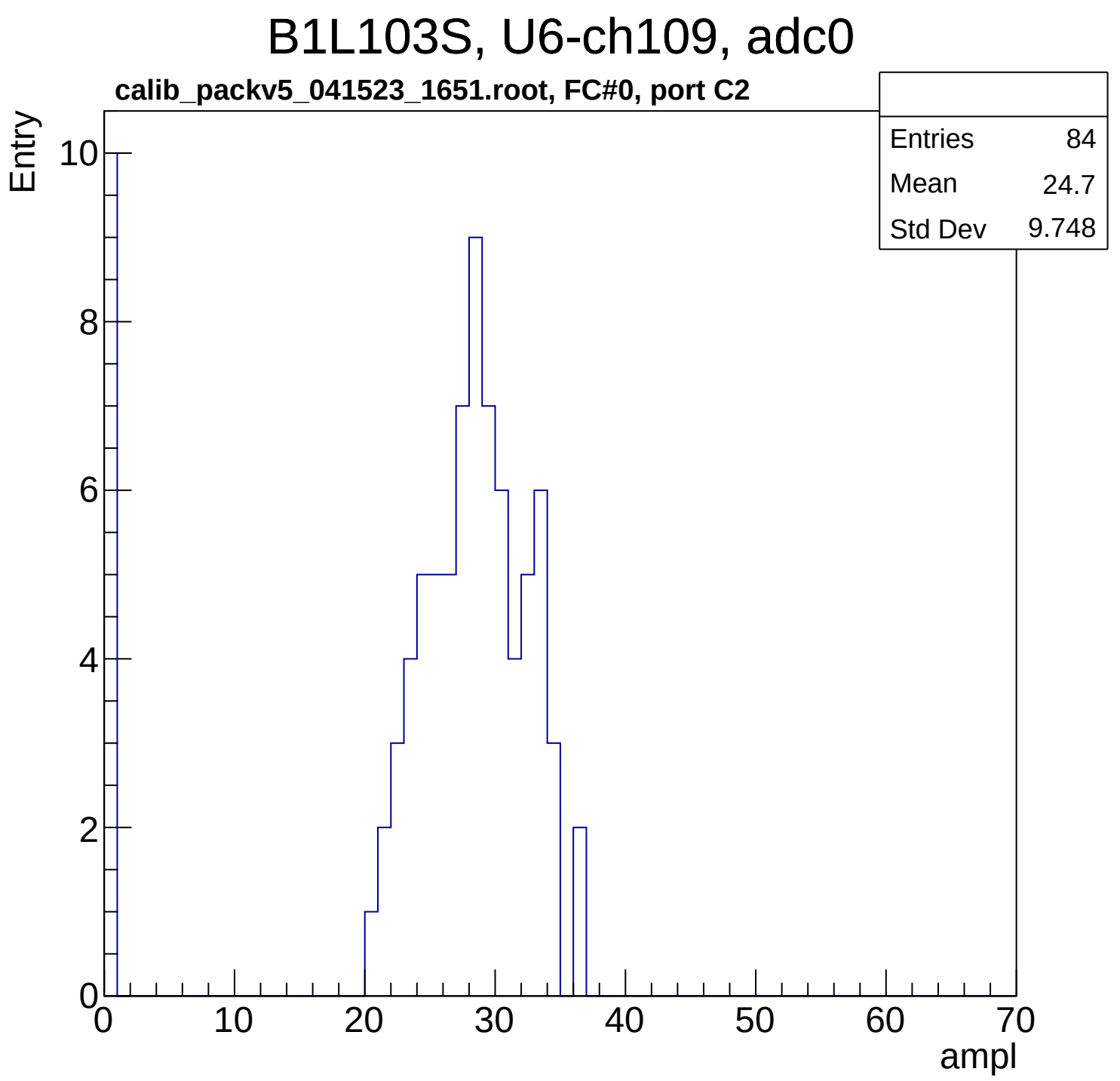
70
ampl


B1L103S, U6-ch109, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 24.7
Std Dev 9.748
Entry
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6
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10
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10
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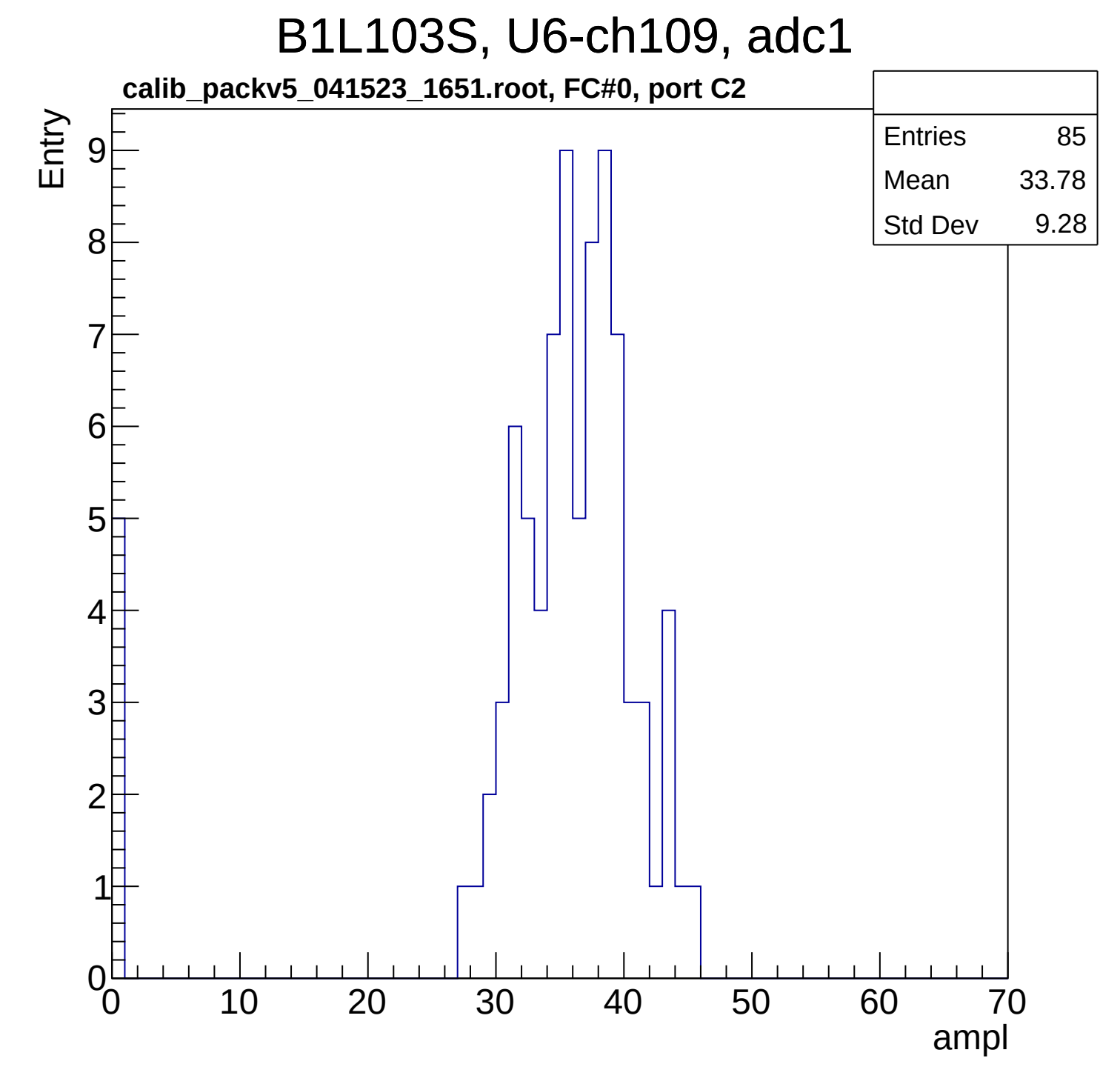
ampl


B1L103S, U6-ch109, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 33.78
Std Dev 9.28
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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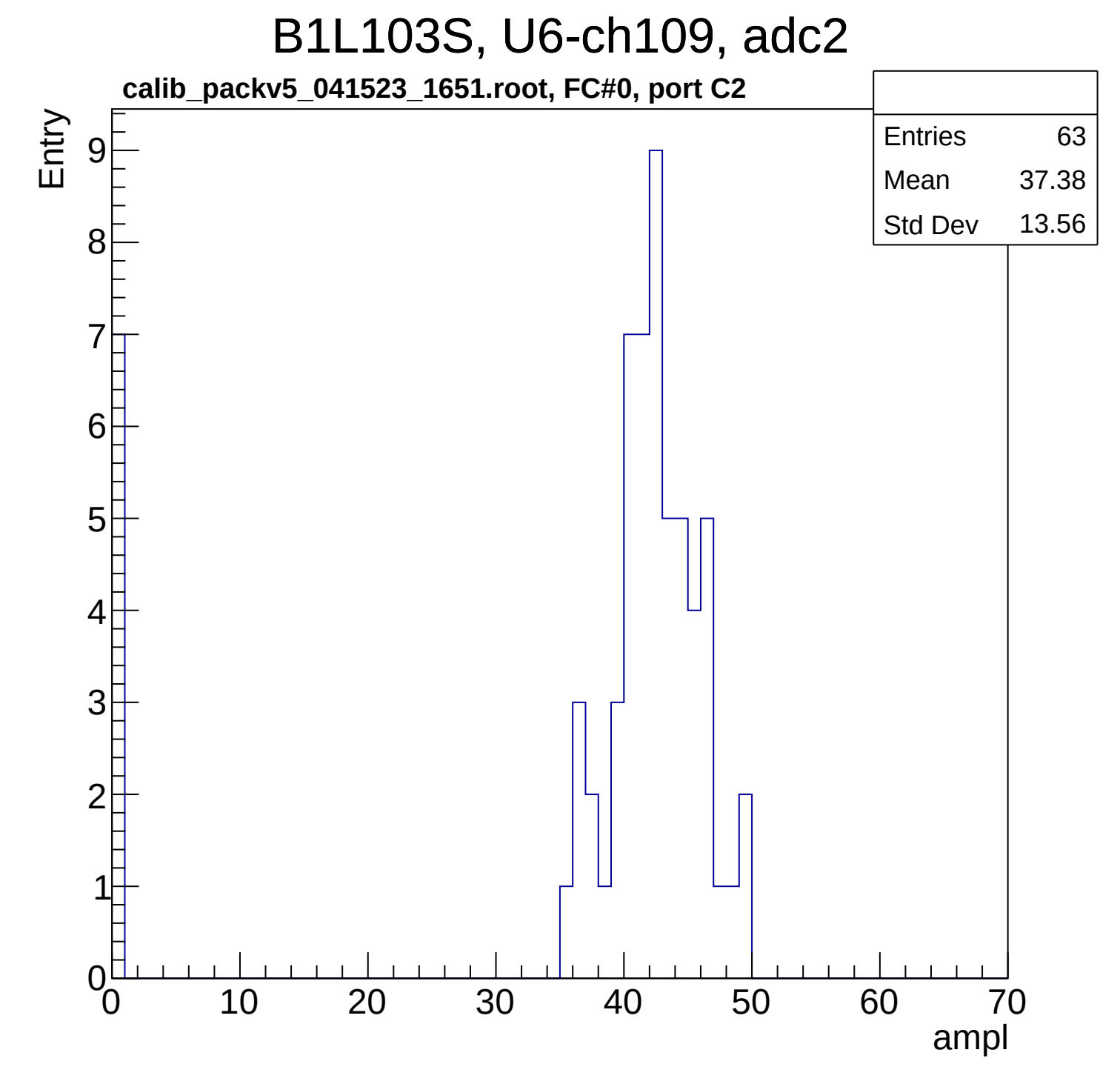
B1L103S, U6-ch109, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 37.38
Std Dev 13.56
Entry
ampl
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2
3
4
5
6
7
8
9
0
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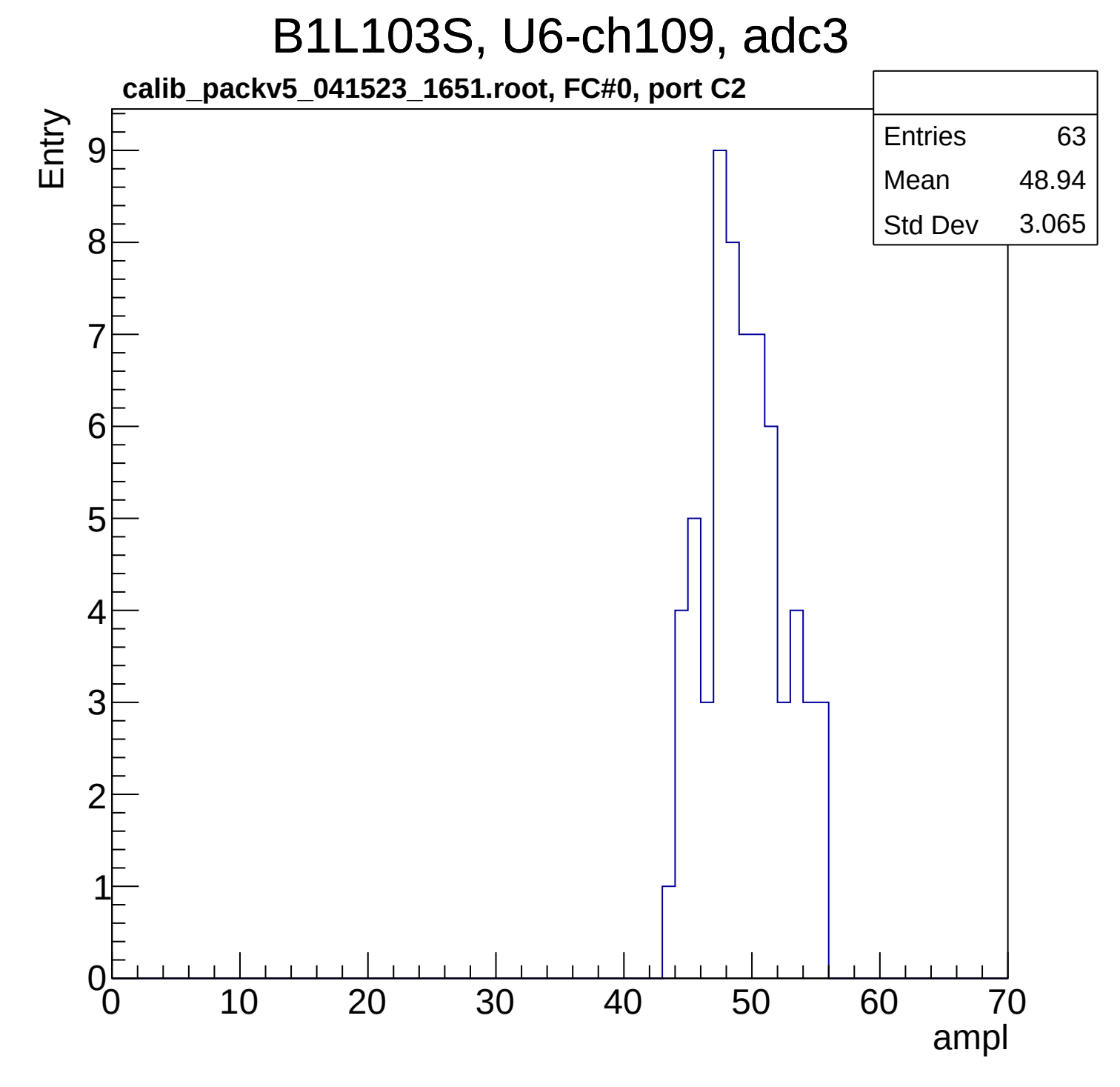
B1L103S, U6-ch109, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 48.94
Std Dev 3.065
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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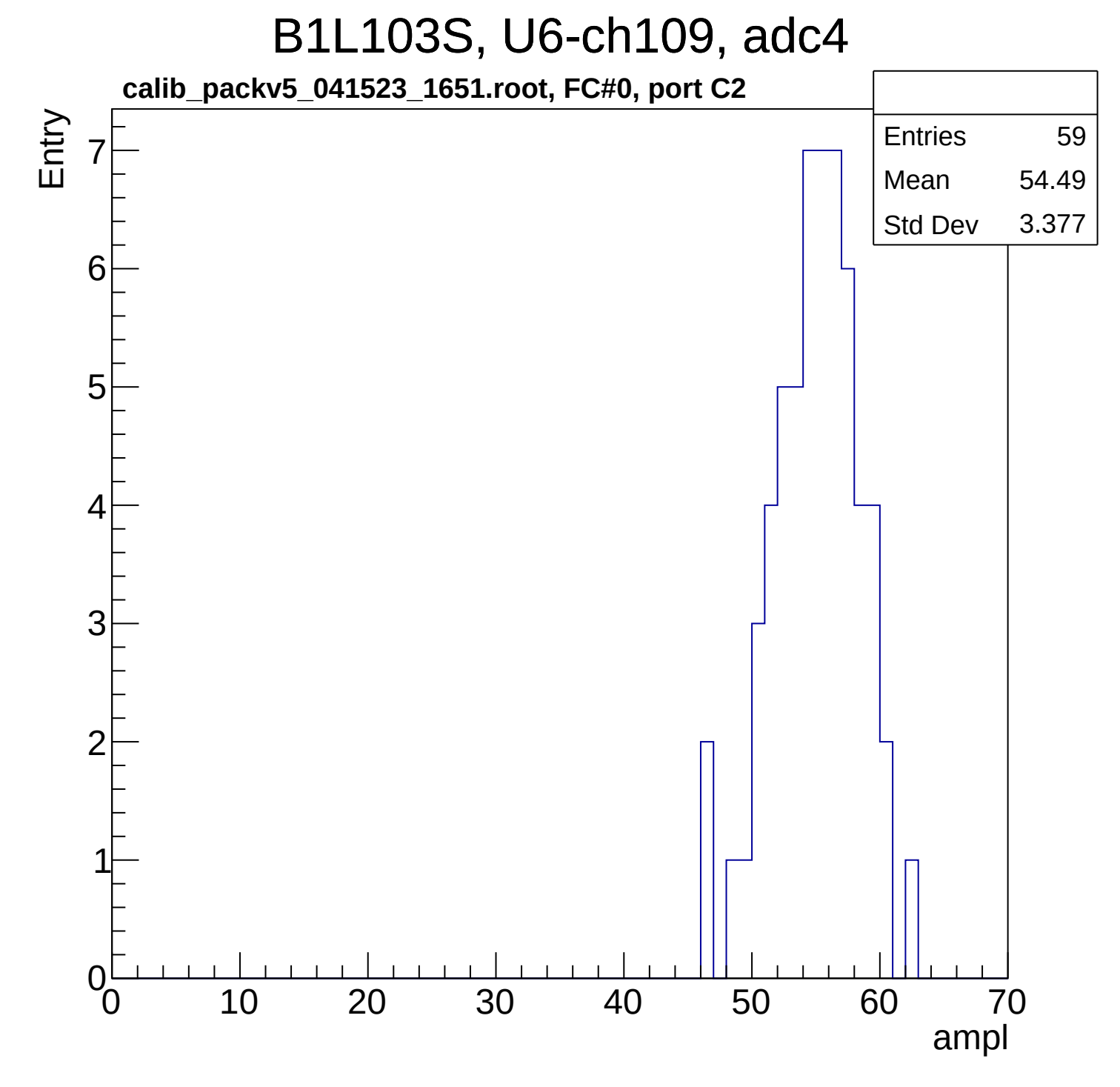
B1L103S, U6-ch109, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 54.49
Std Dev 3.377
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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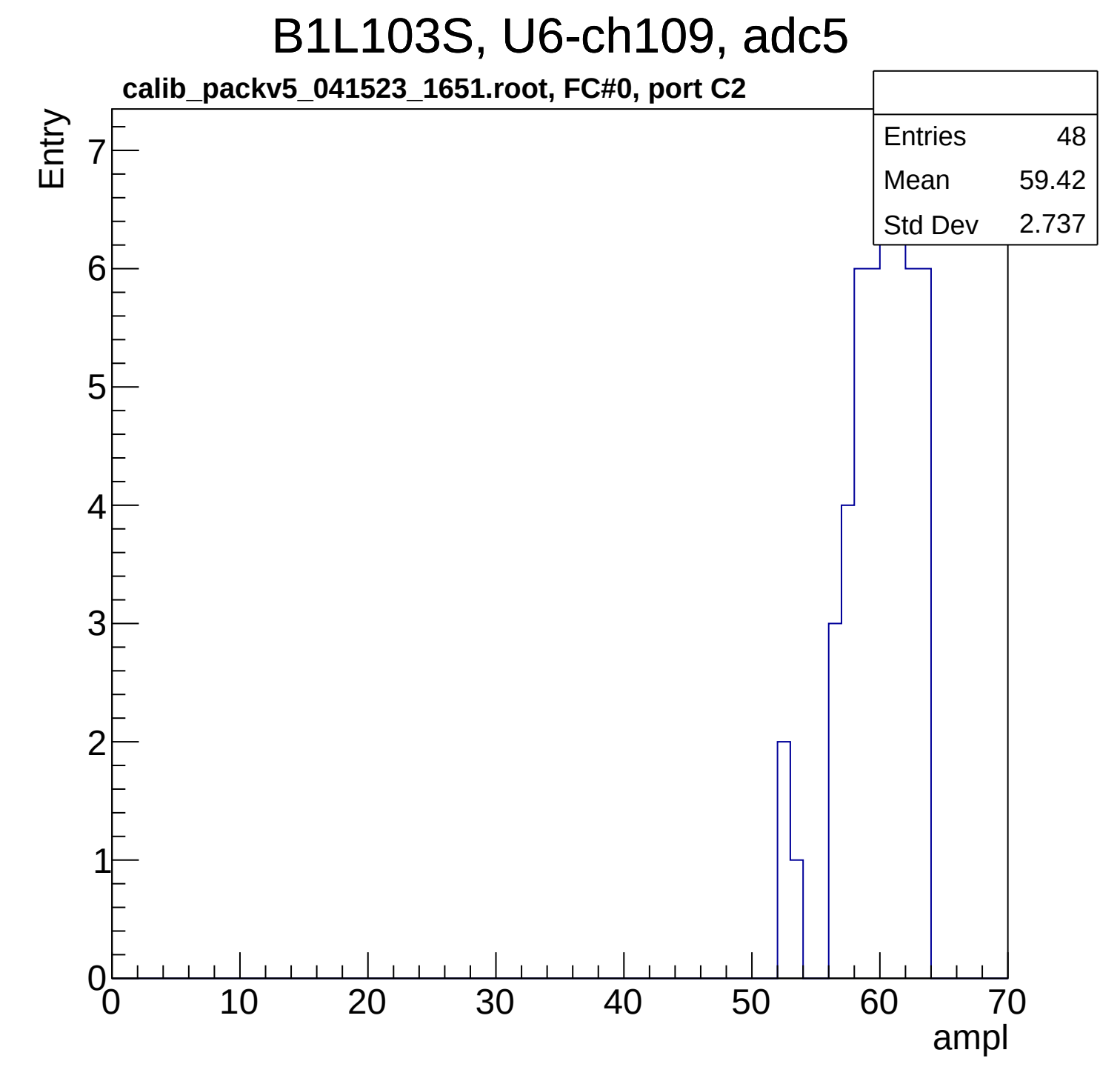
B1L103S, U6-ch109, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 59.42
Std Dev 2.737
Entry
ampl
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1
2
3
4
5
6
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0
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40
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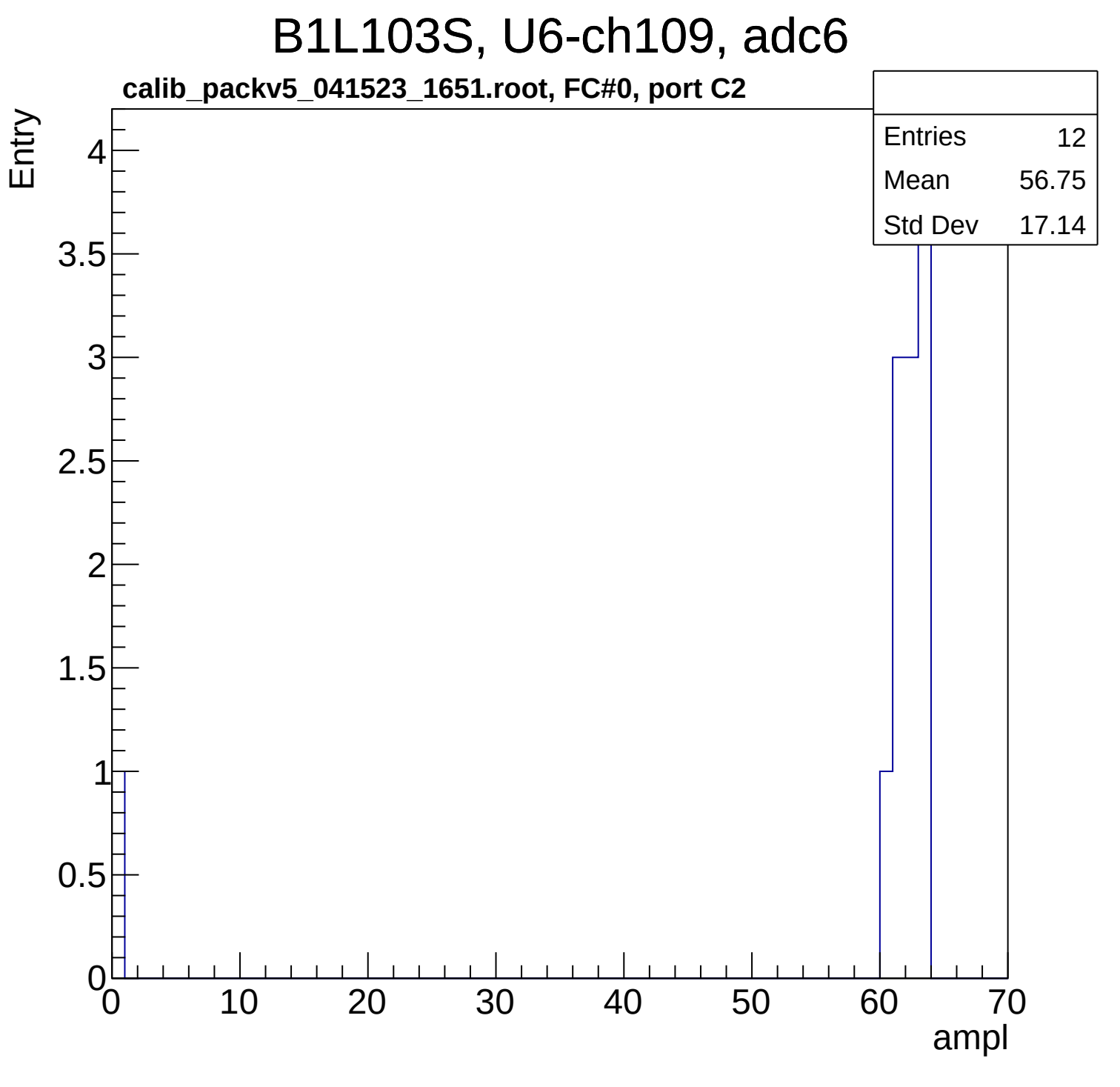
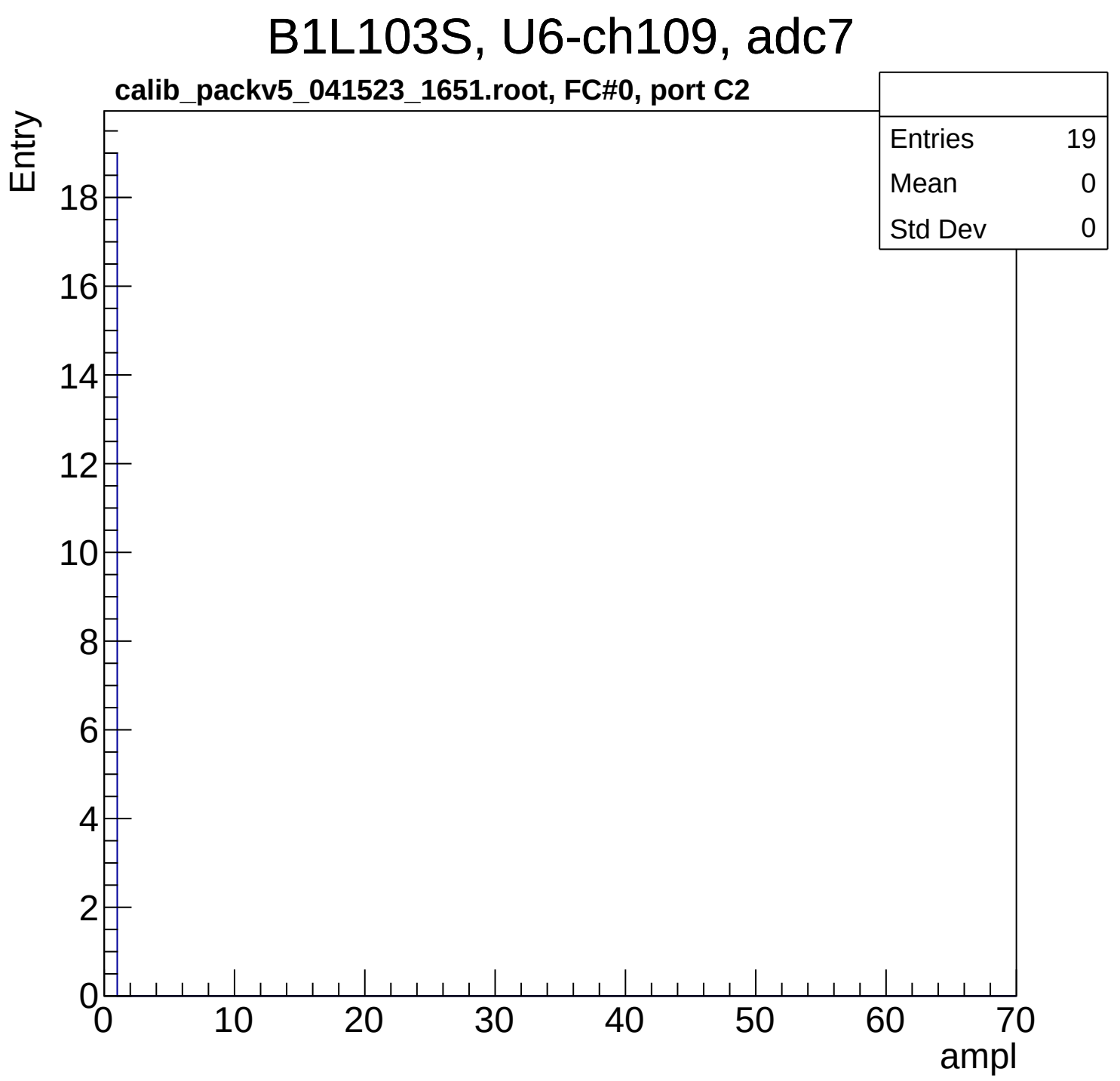
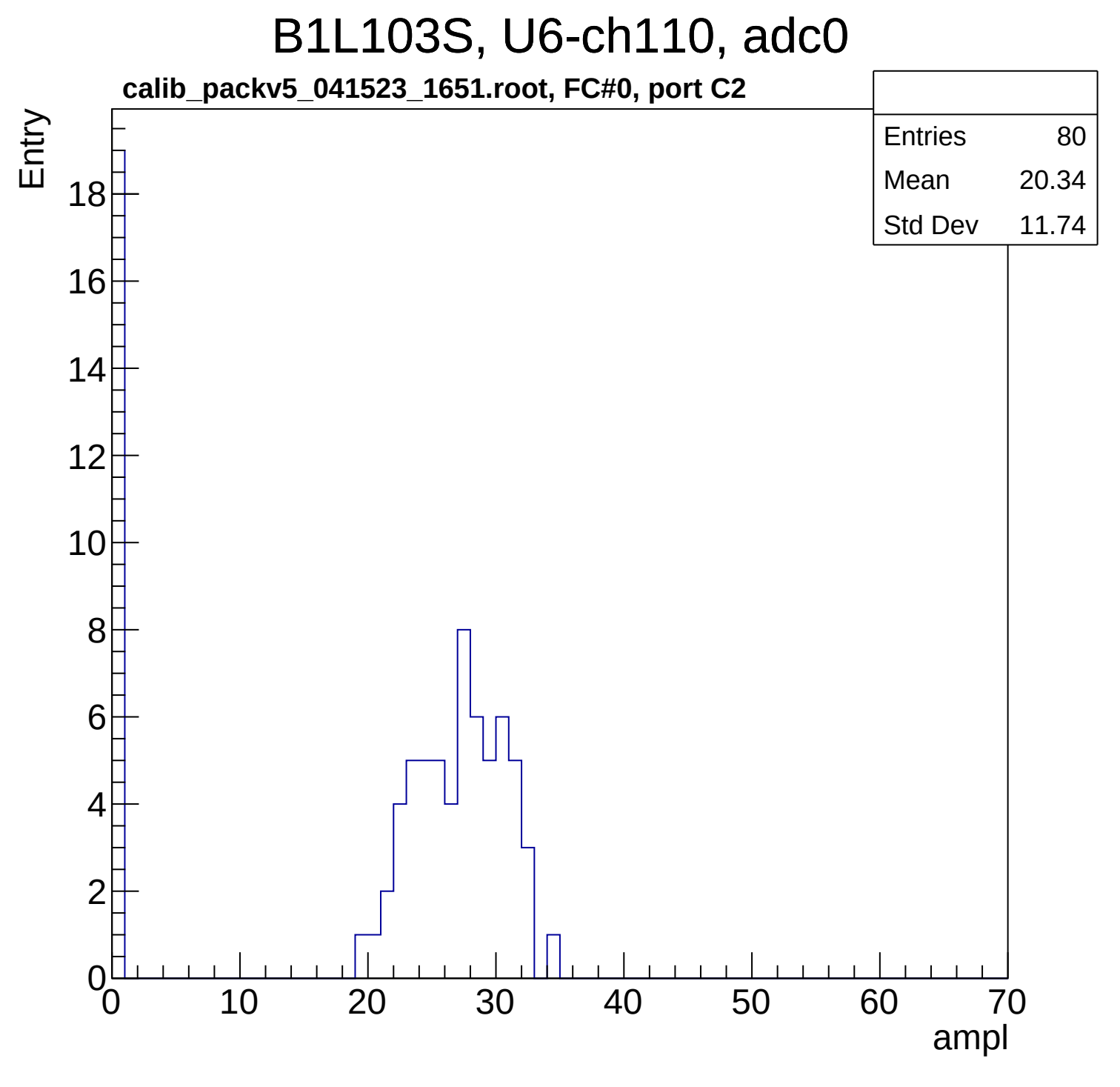
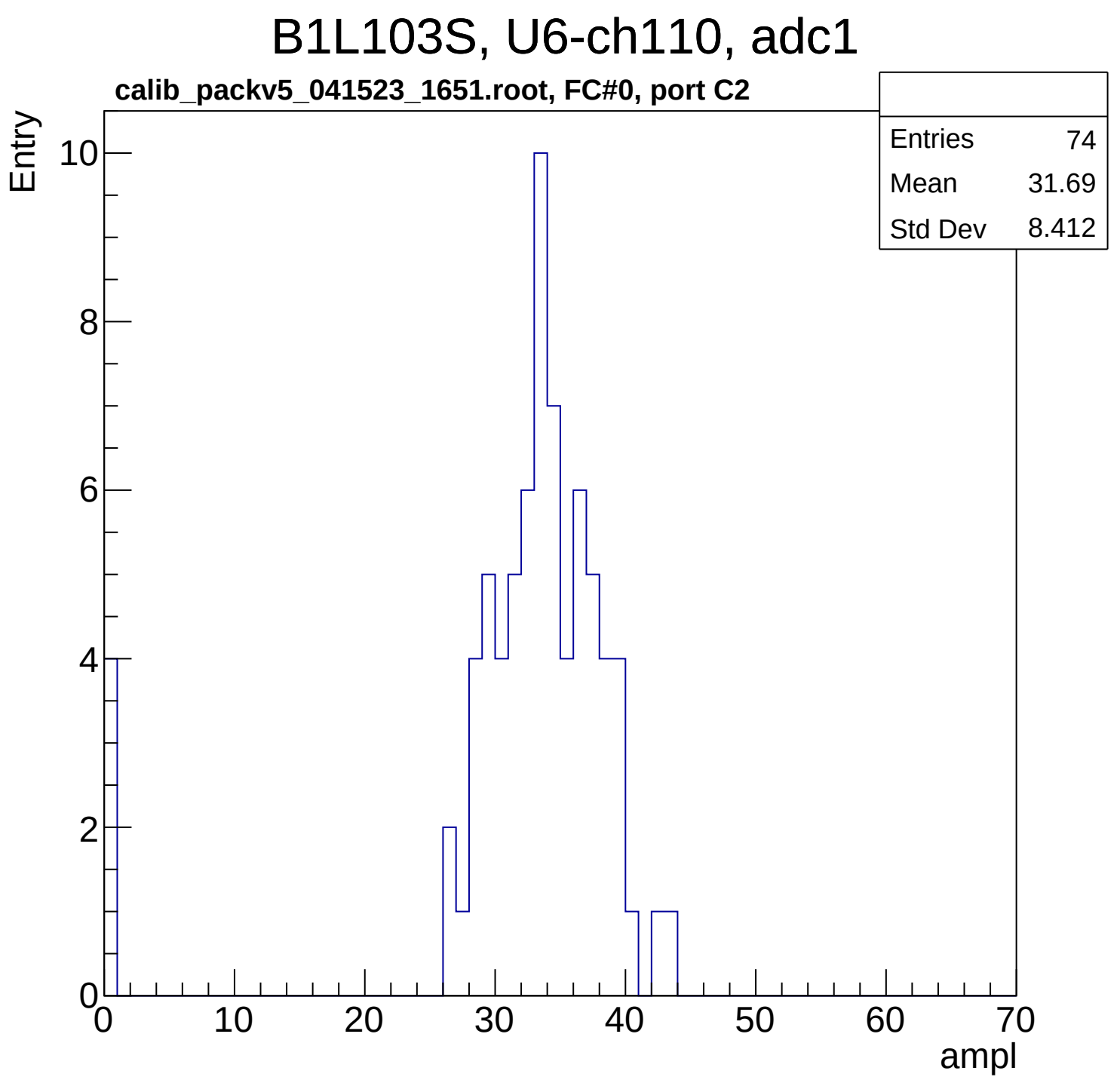
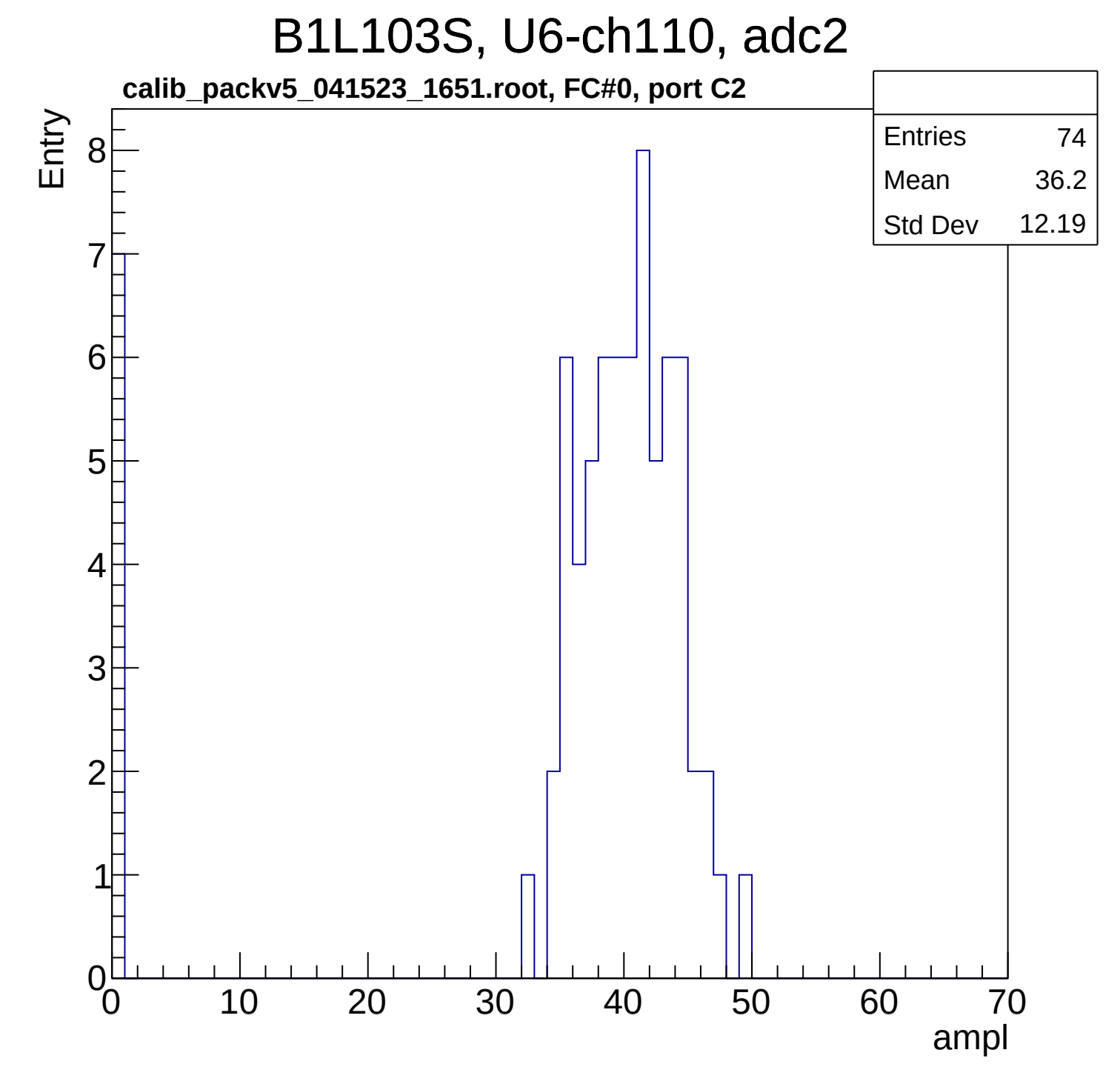

B1L103S, U6-ch109, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 56.75
Std Dev 17.14
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U6-ch109, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch110, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 20.34
Std Dev 11.74
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch110, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 31.69
Std Dev 8.412
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U6-ch110, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 36.2
Std Dev 12.19
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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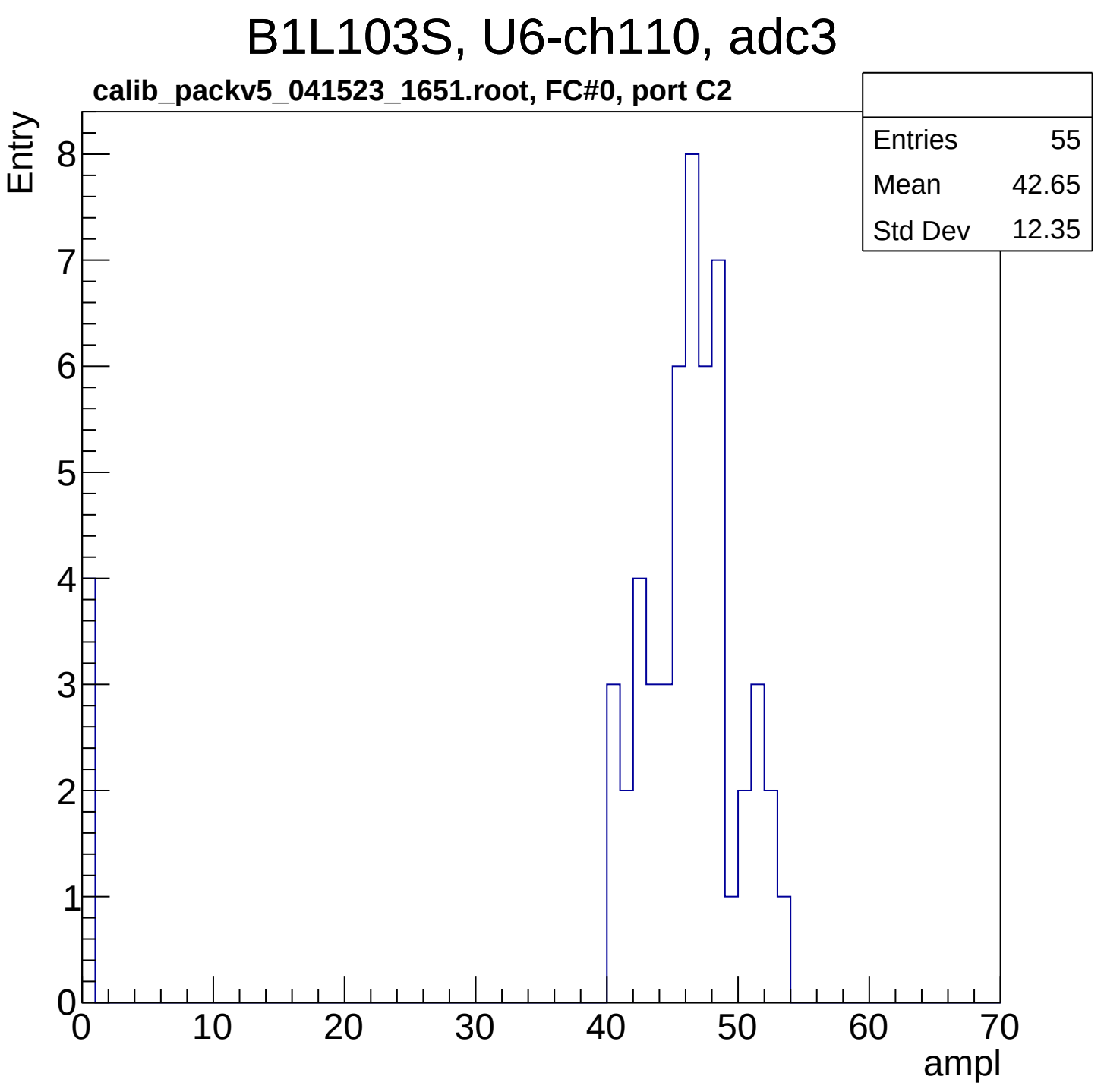
B1L103S, U6-ch110, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 42.65
Std Dev 12.35
Entry
ampl
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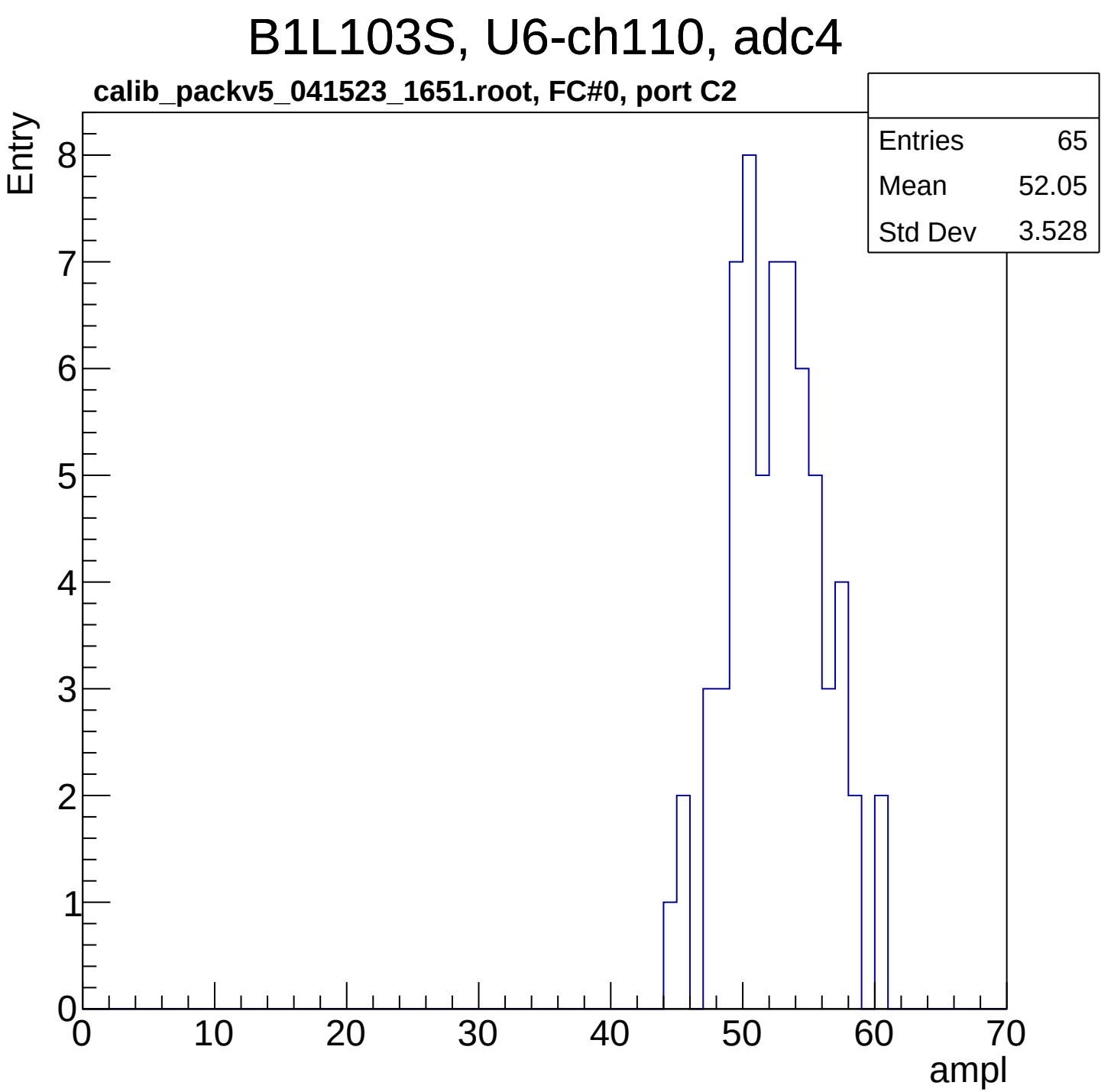
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch110, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 52.05
Std Dev 3.528
Entry
ampl
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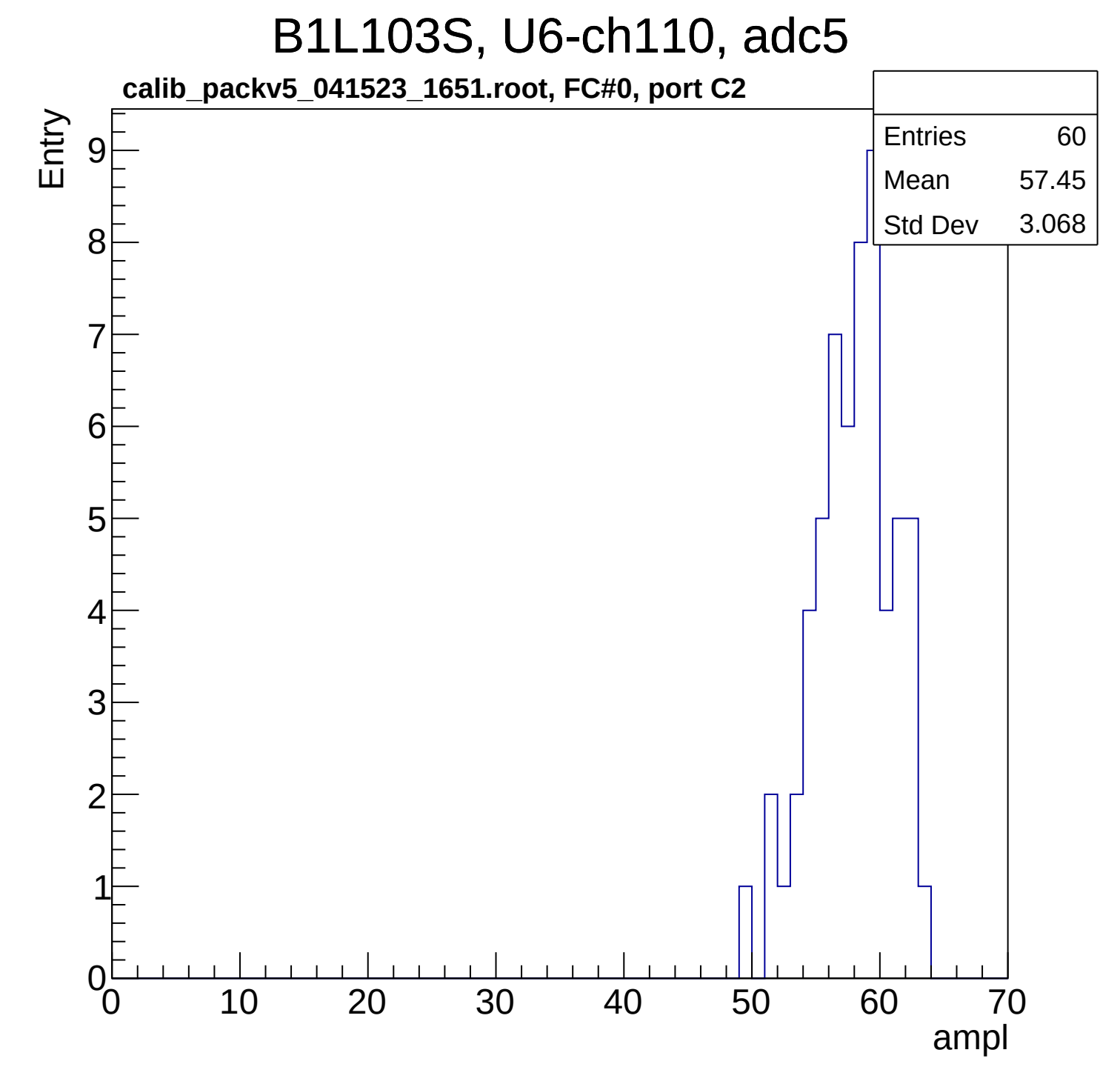
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch110, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 57.45
Std Dev 3.068
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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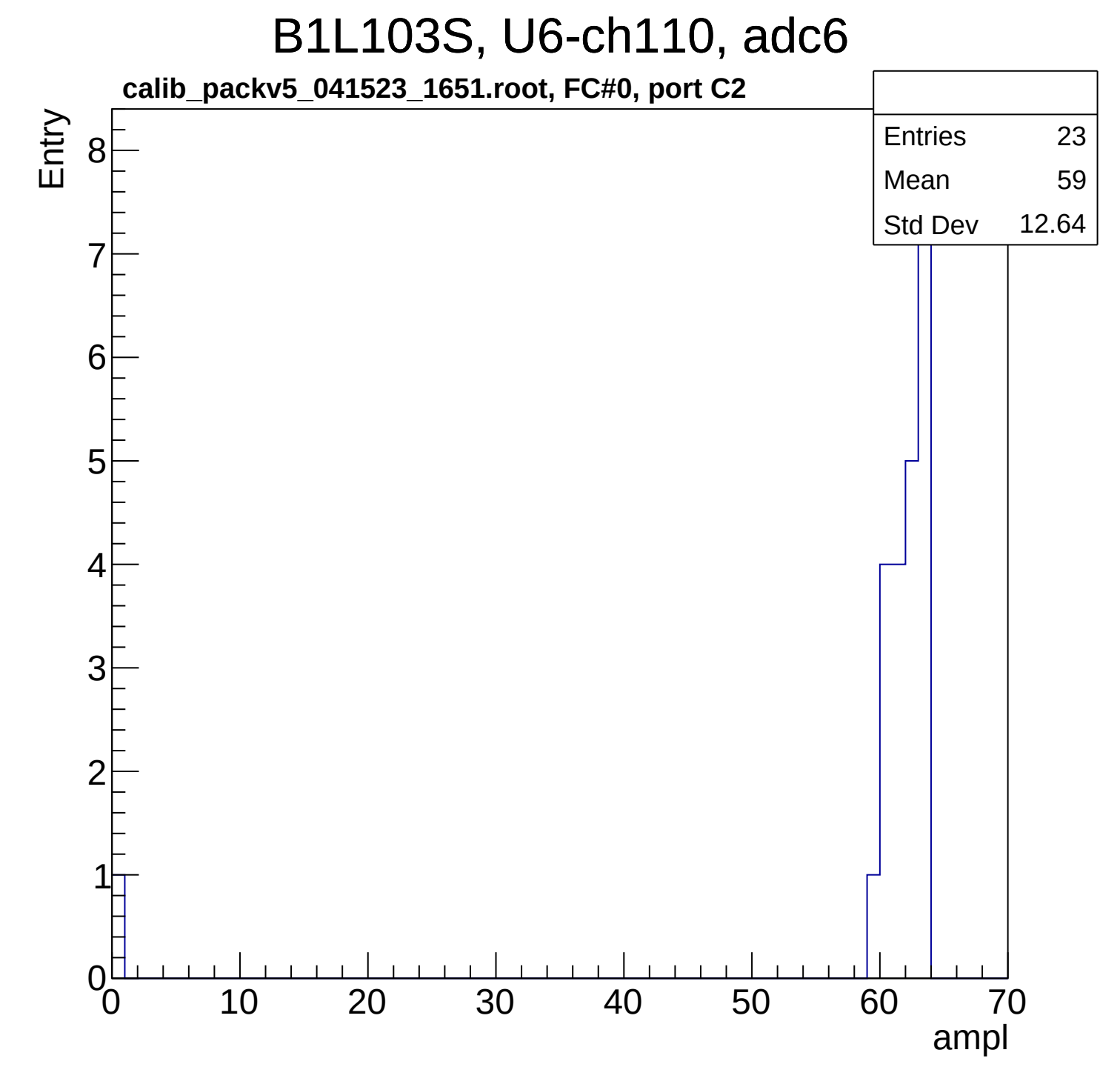
B1L103S, U6-ch110, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 59
Std Dev 12.64
Entry
ampl
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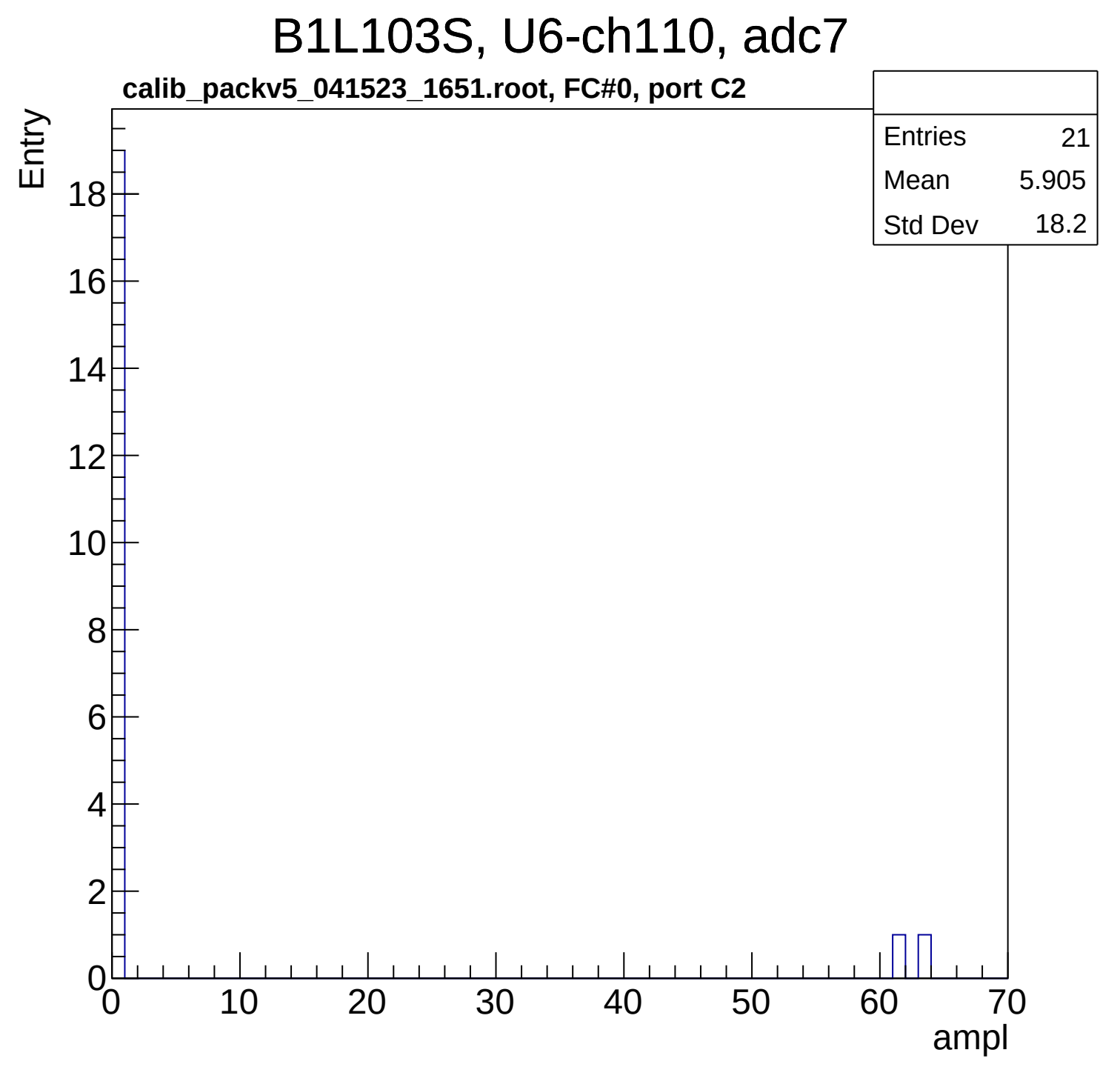
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch110, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.905
Std Dev 18.2
Entry
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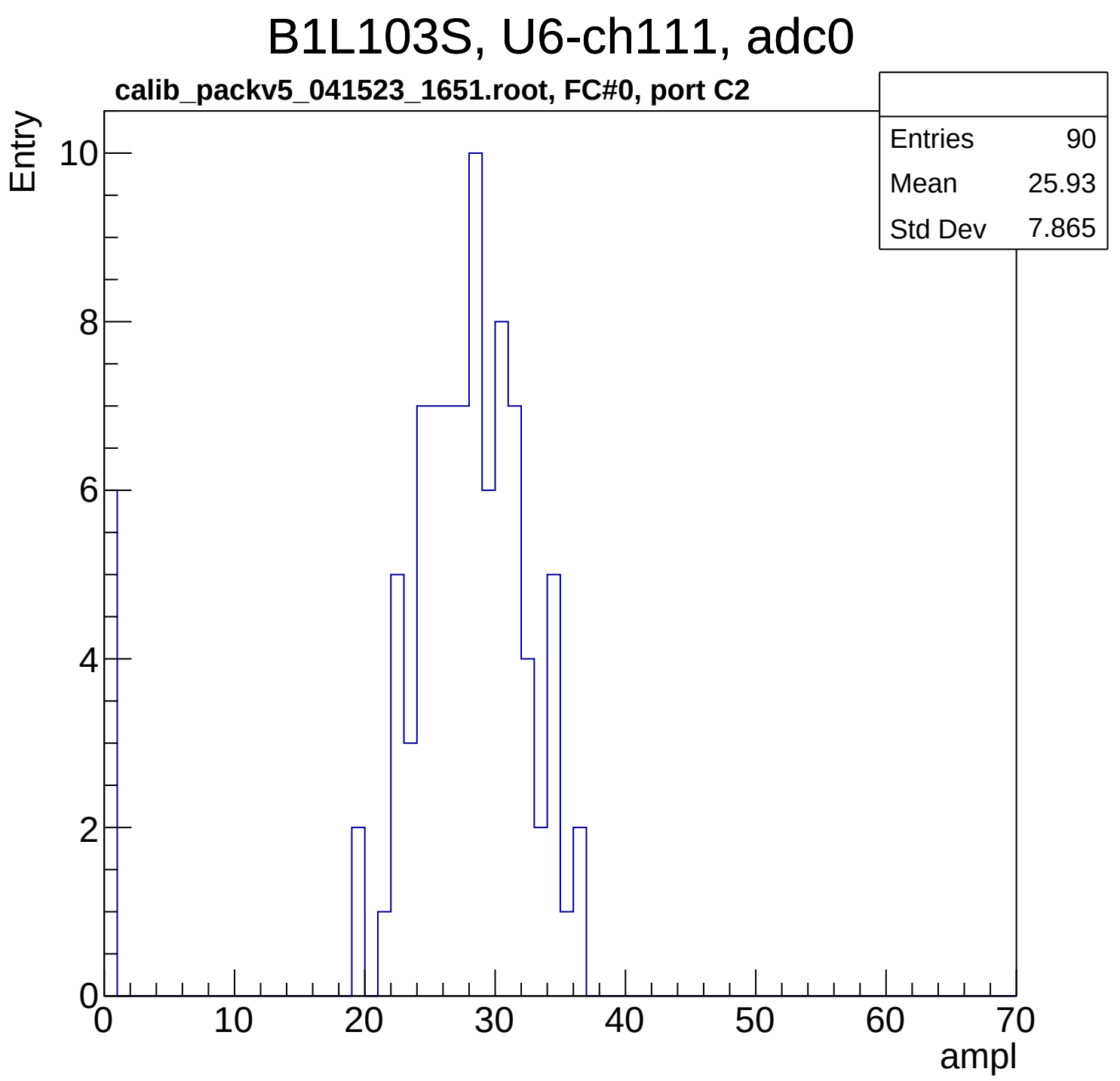
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch111, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 25.93
Std Dev 7.865
Entry
ampl
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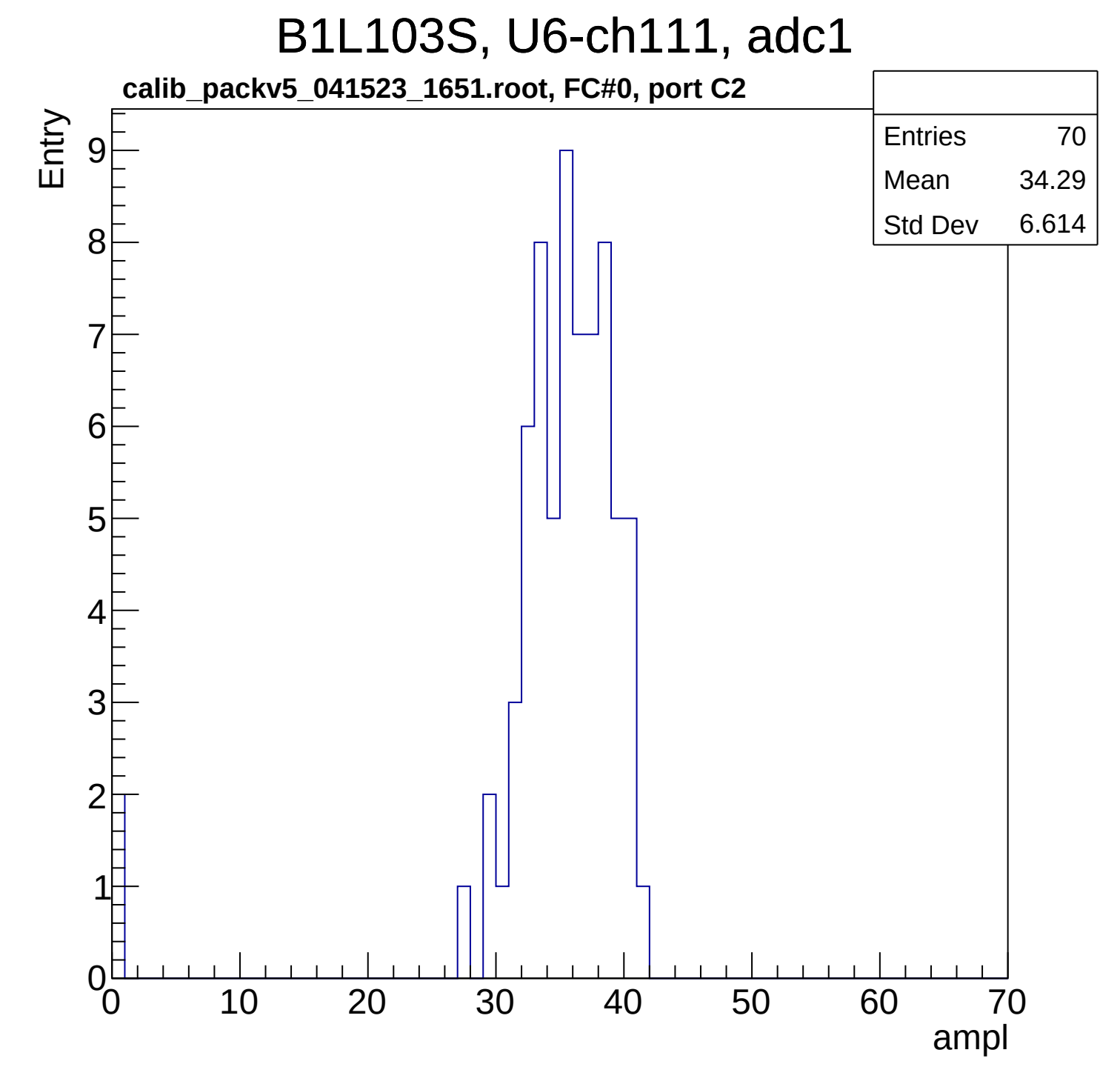
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U6-ch111, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 34.29
Std Dev 6.614
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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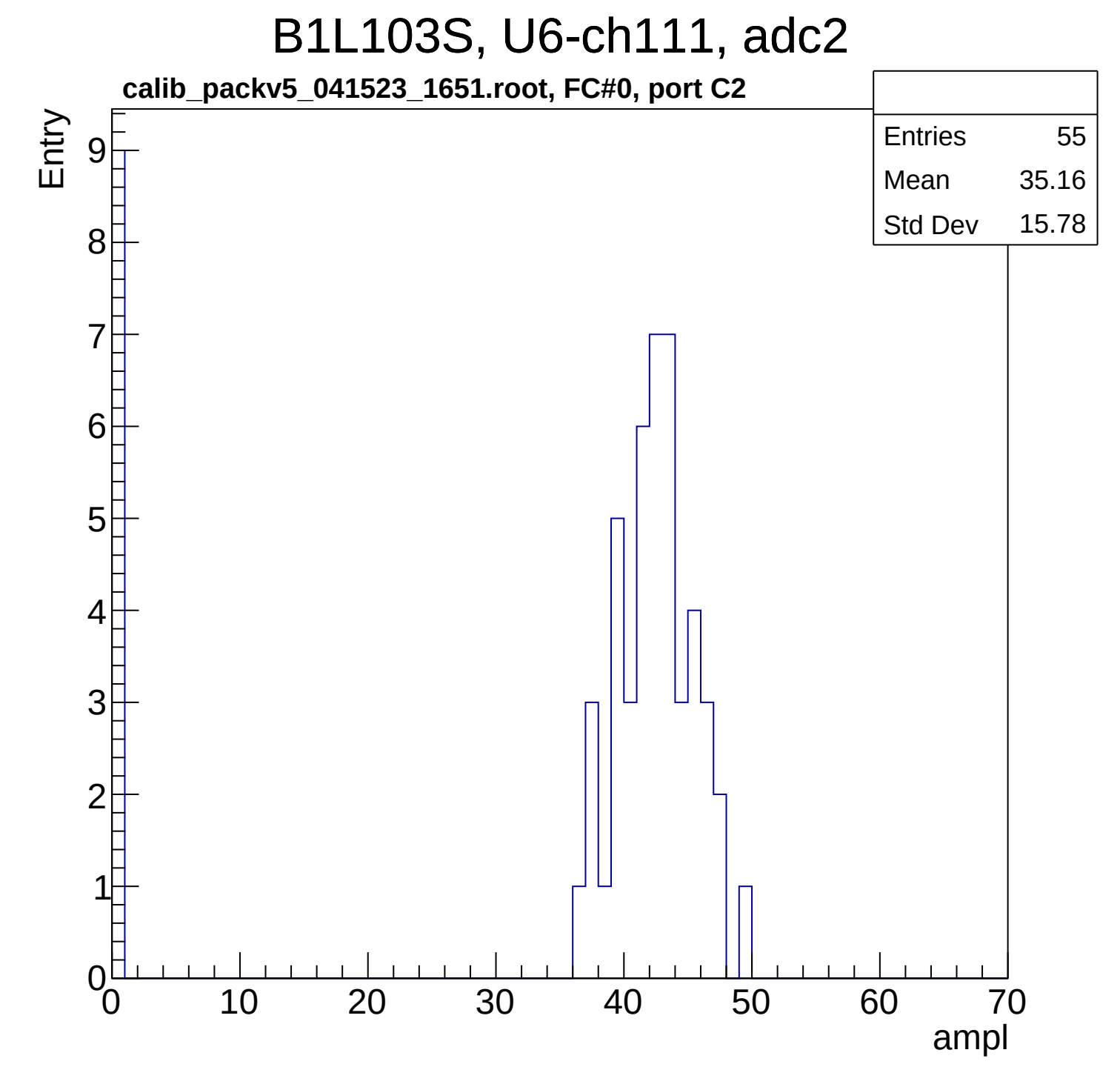
B1L103S, U6-ch111, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 35.16
Std Dev 15.78
Entry
ampl
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2
3
4
5
6
7
8
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0
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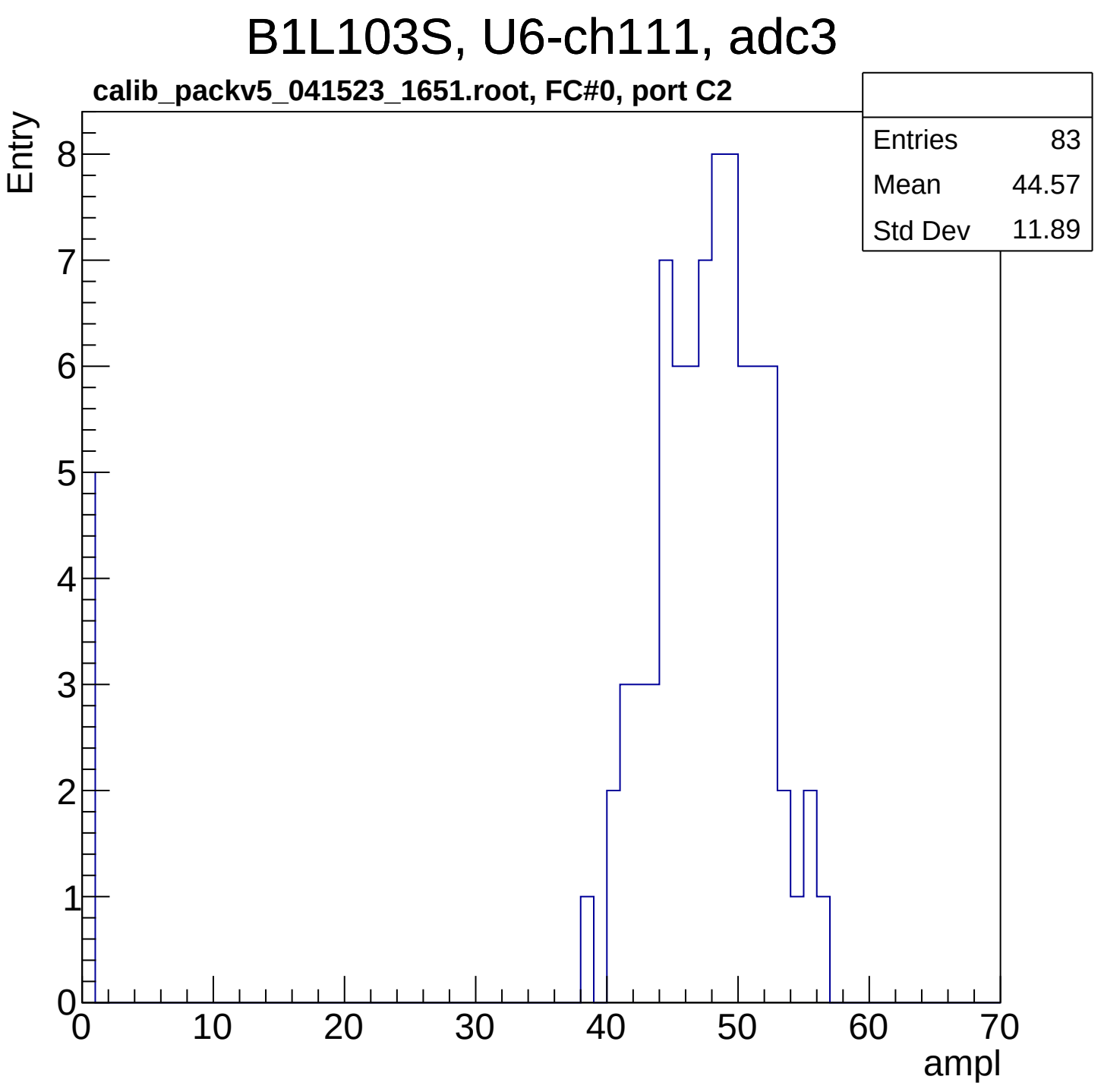
B1L103S, U6-ch111, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 44.57
Std Dev 11.89
Entry
ampl
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2
3
4
5
6
7
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0
10
20
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40
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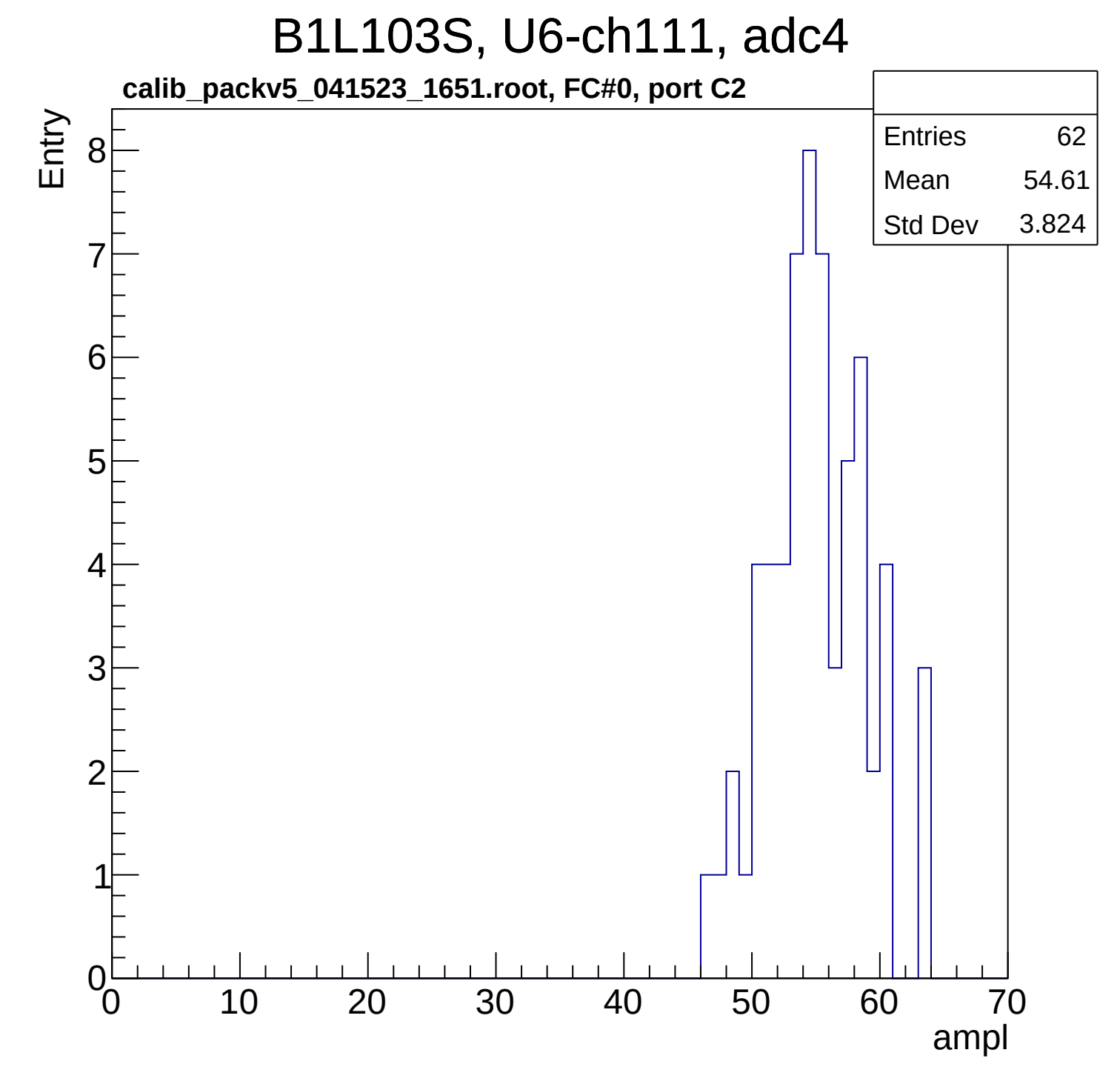
60
70


B1L103S, U6-ch111, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 54.61
Std Dev 3.824
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
50
60
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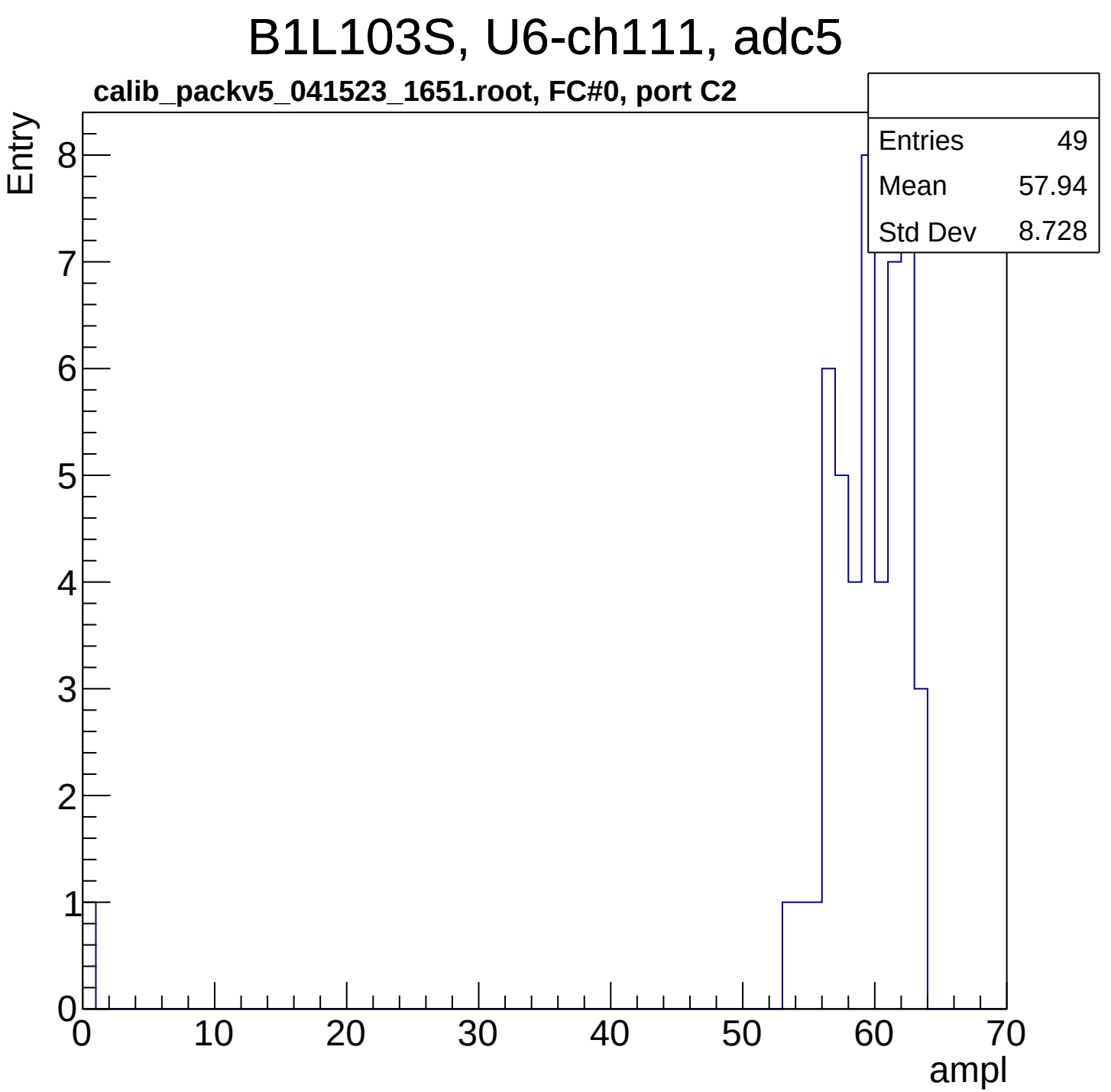
B1L103S, U6-ch111, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 57.94
Std Dev 8.728
Entry
ampl
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2
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4
5
6
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0
10
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40
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60
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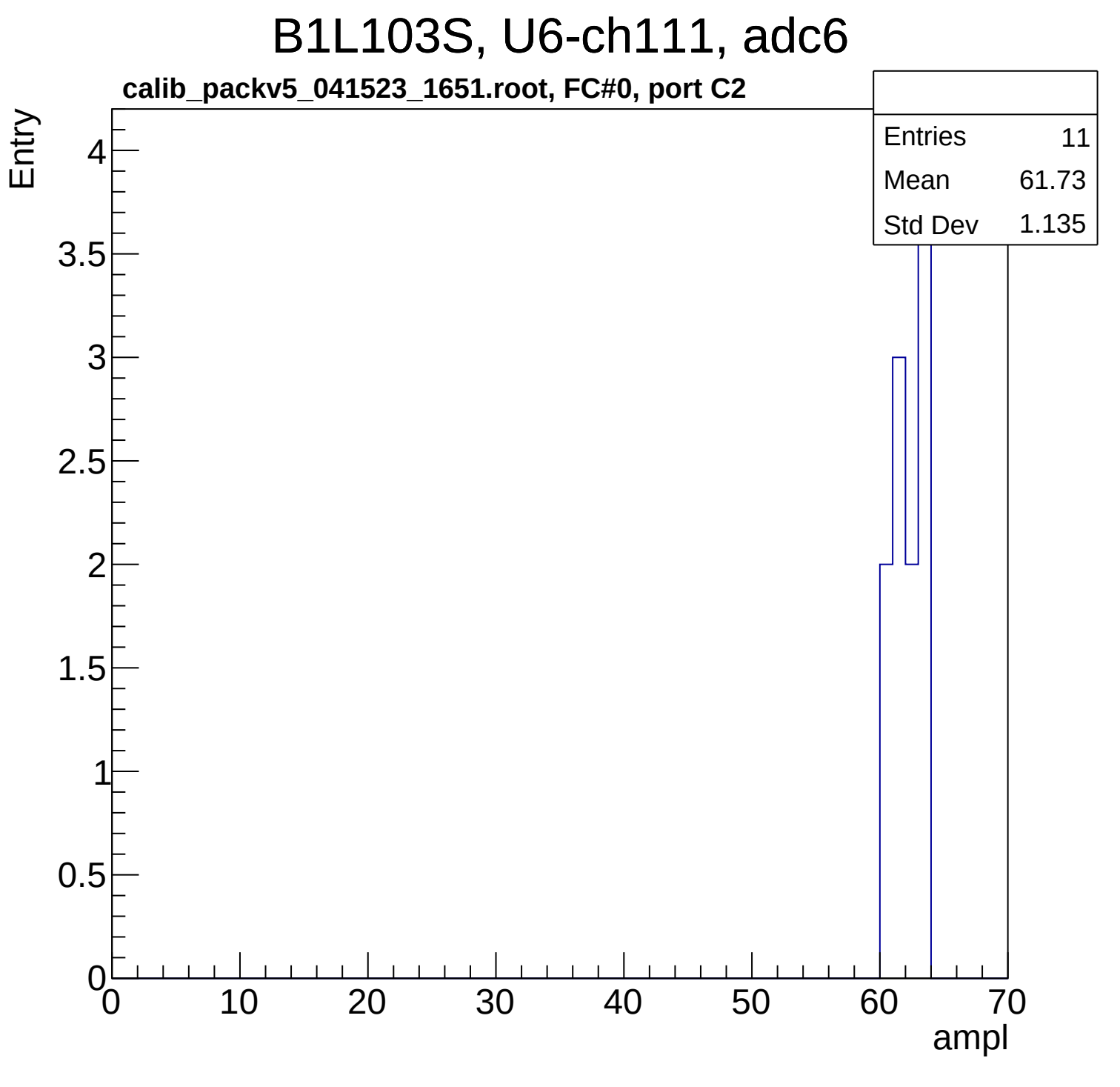
B1L103S, U6-ch111, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 61.73
Std Dev 1.135
Entry
ampl
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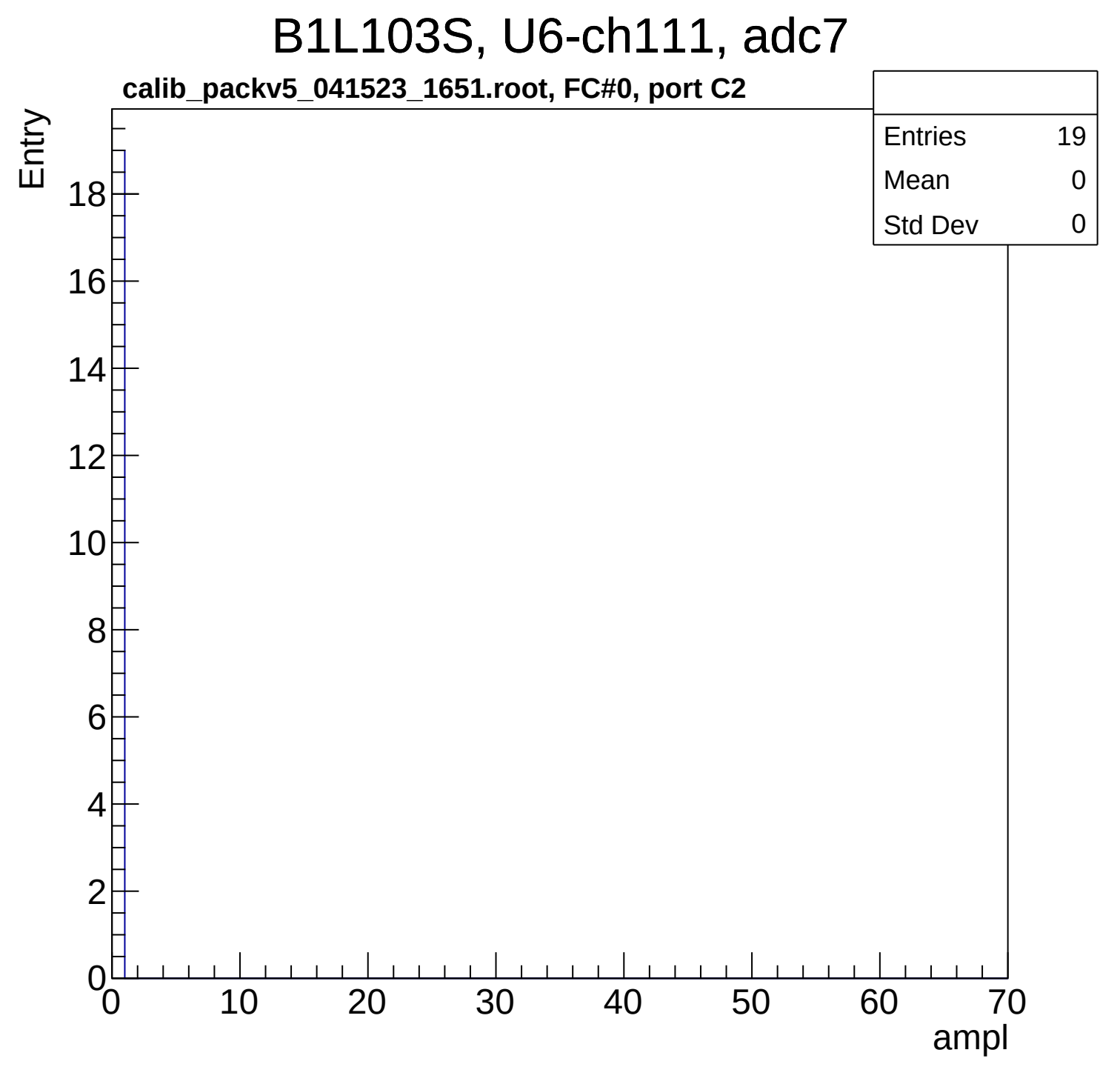
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U6-ch111, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
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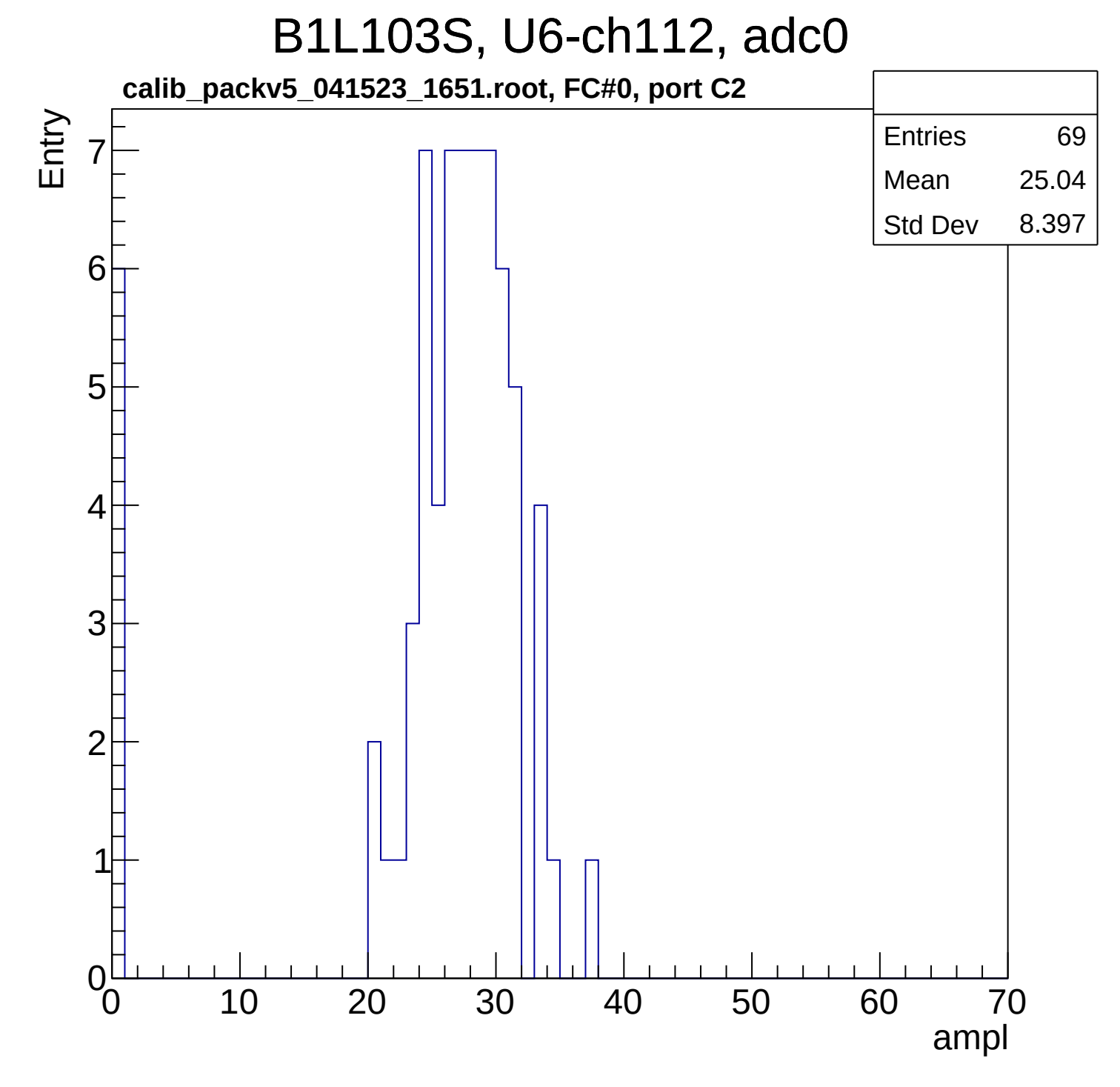
50
60
70
ampl


B1L103S, U6-ch112, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 25.04
Std Dev 8.397
Entry
ampl
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2
3
4
5
6
7
0
10
20
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40
50
60
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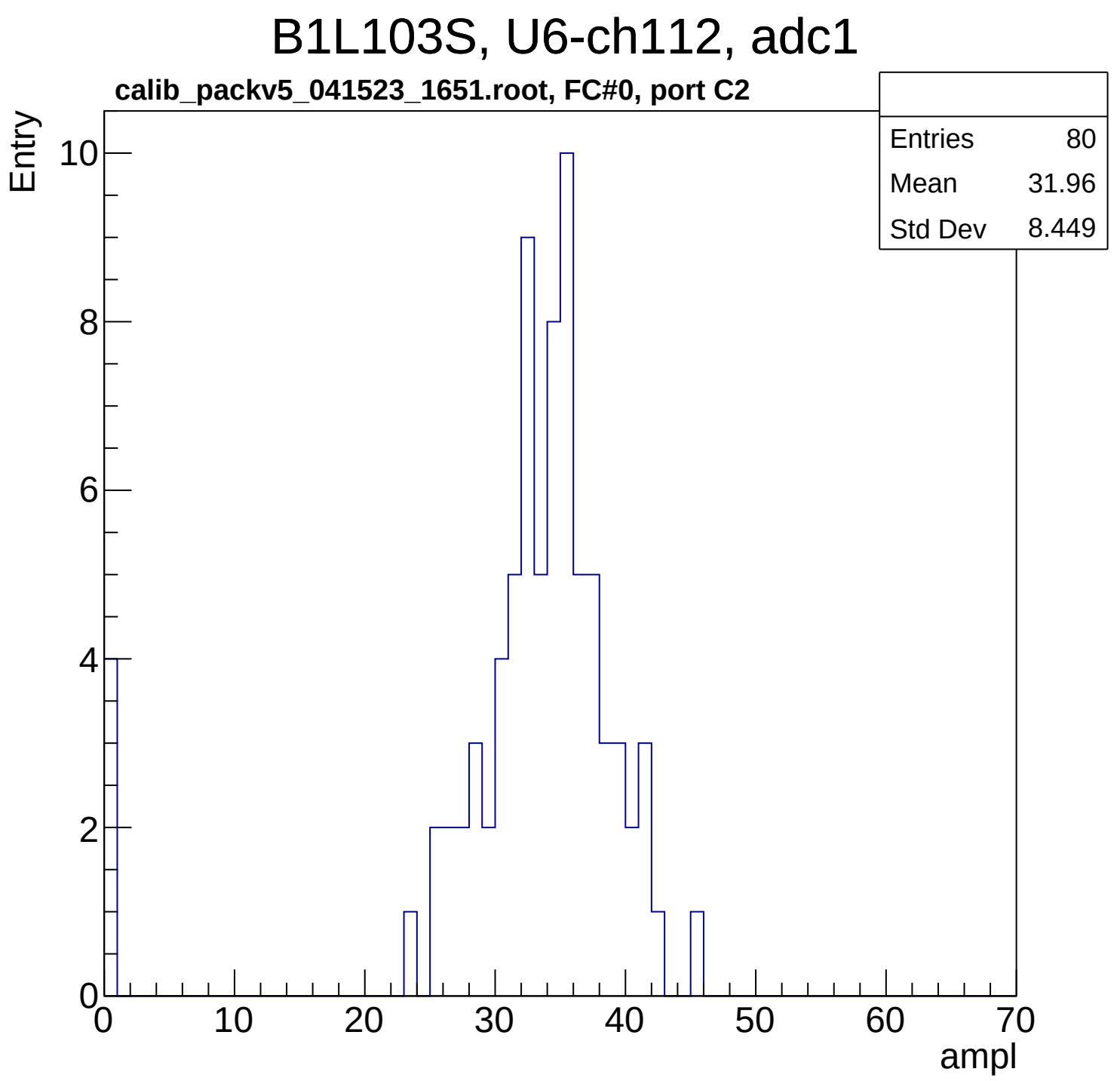
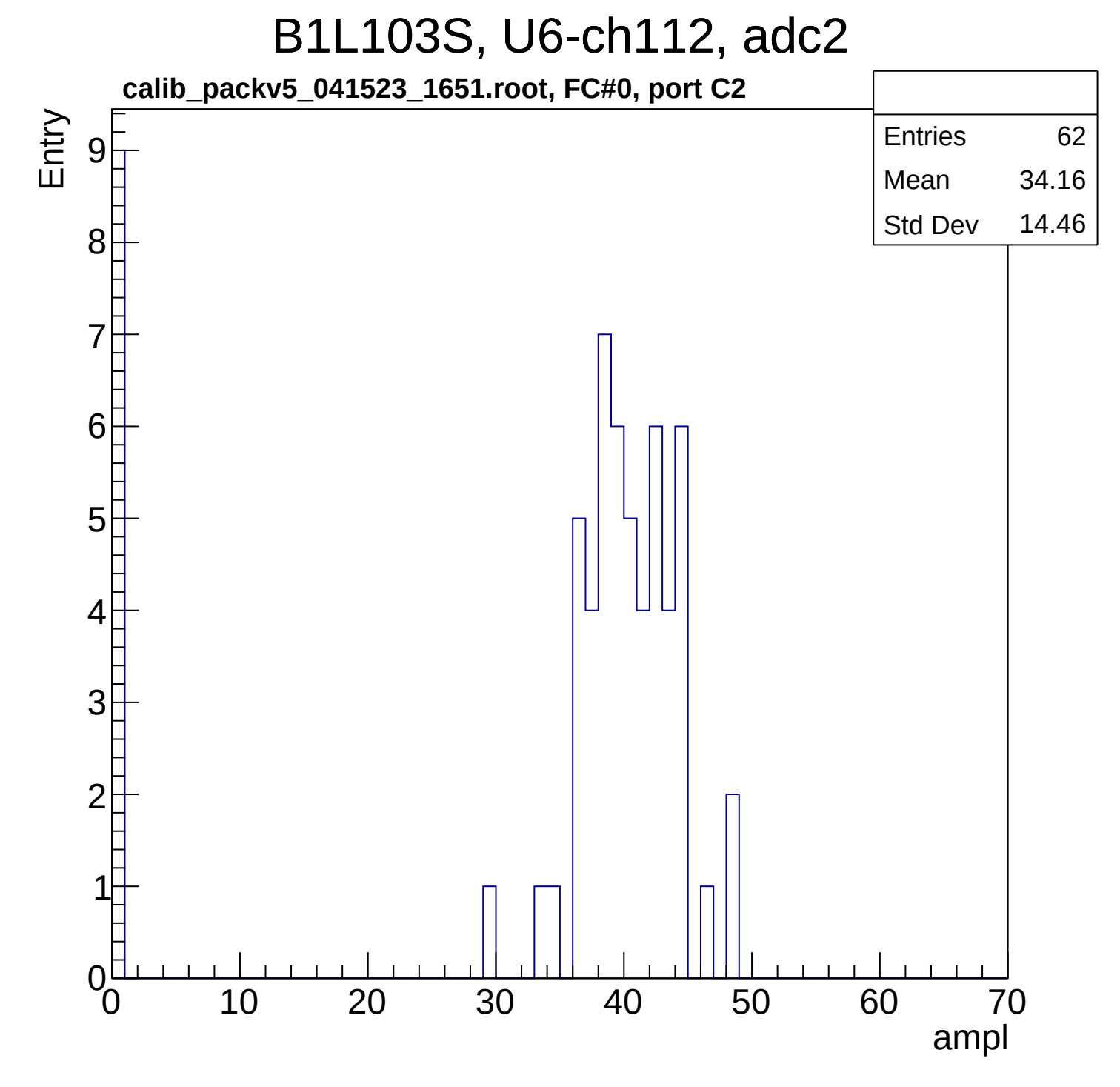

B1L103S, U6-ch112, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 31.96
Std Dev 8.449
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U6-ch112, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 34.16
Std Dev 14.46
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
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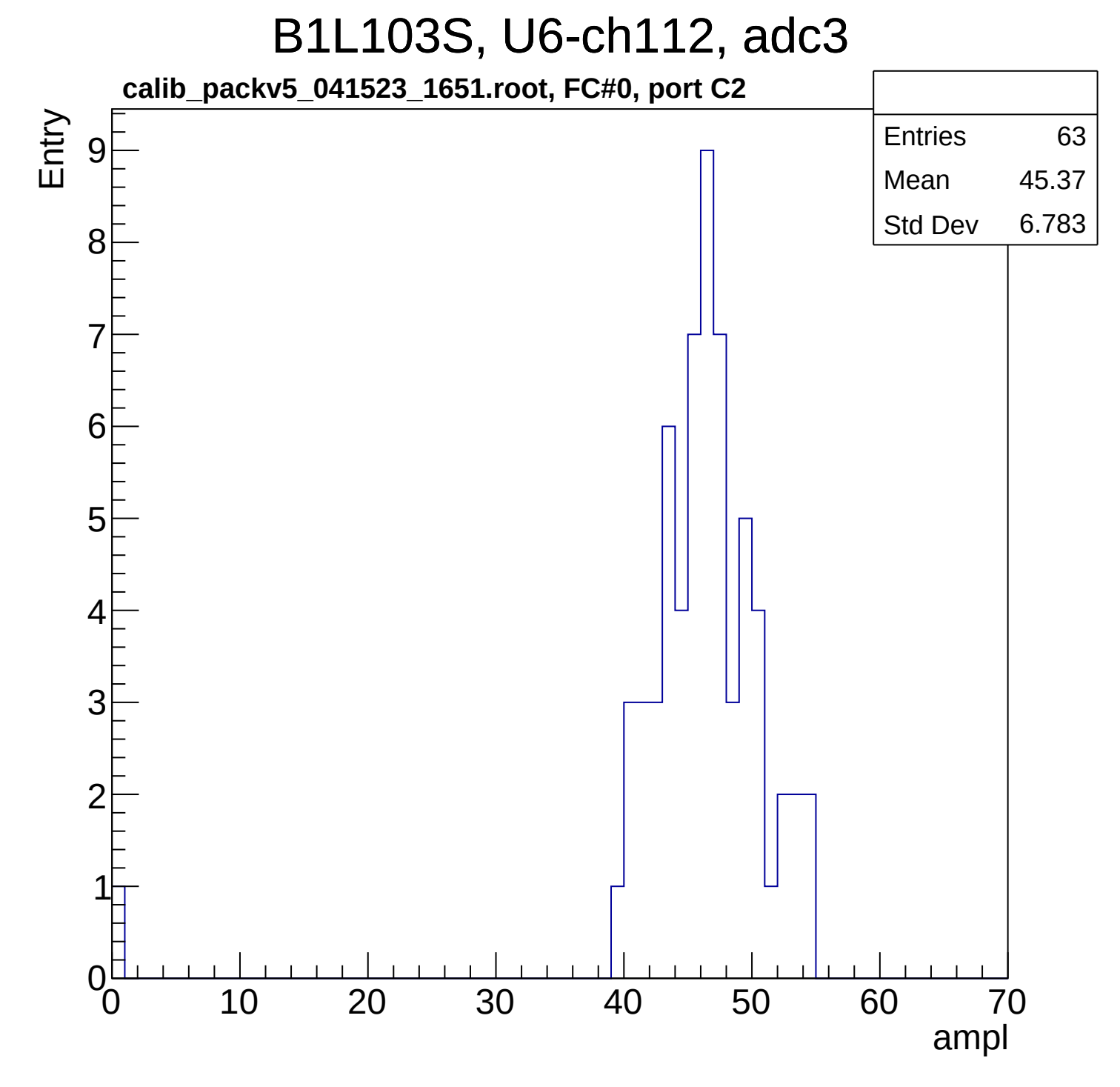
B1L103S, U6-ch112, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 45.37
Std Dev 6.783
Entry
ampl
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2
3
4
5
6
7
8
9
0
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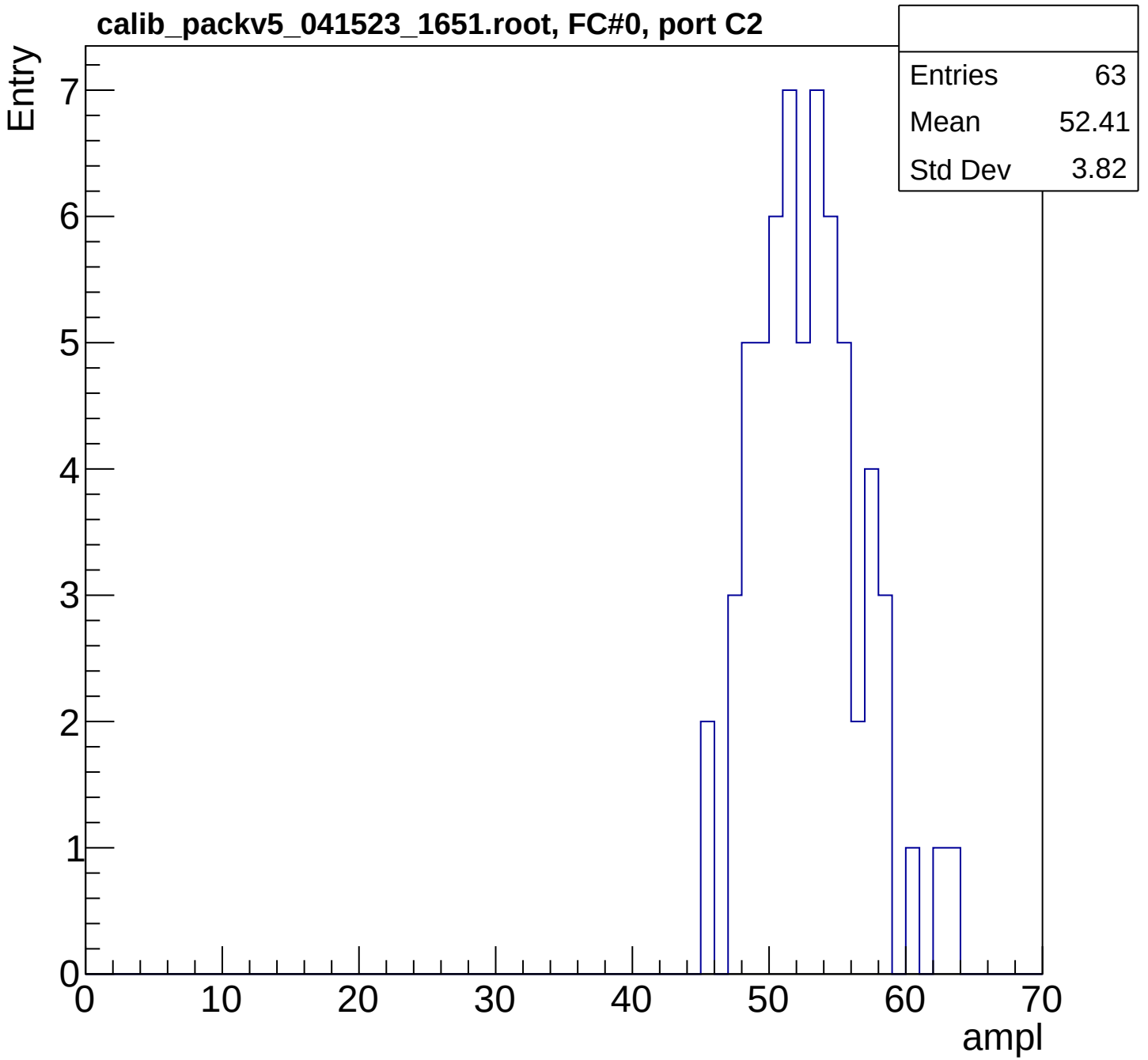
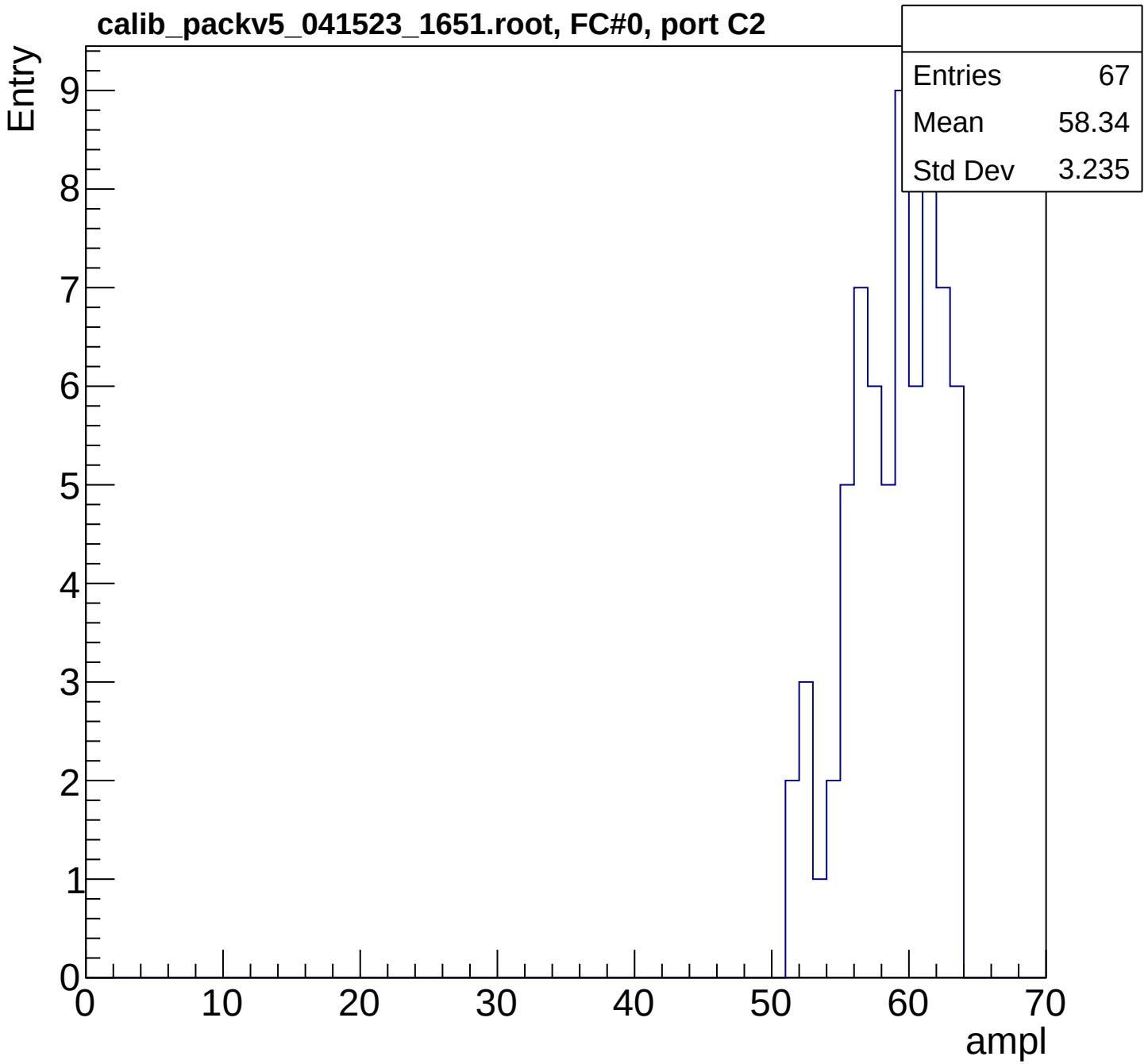
20
30
40
50
60
70


B1L103S, U6-ch112, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 52.41
Std Dev 3.82
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U6-ch112, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 58.34
Std Dev 3.235
Entry
ampl
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2
3
4
5
6
7
8
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0
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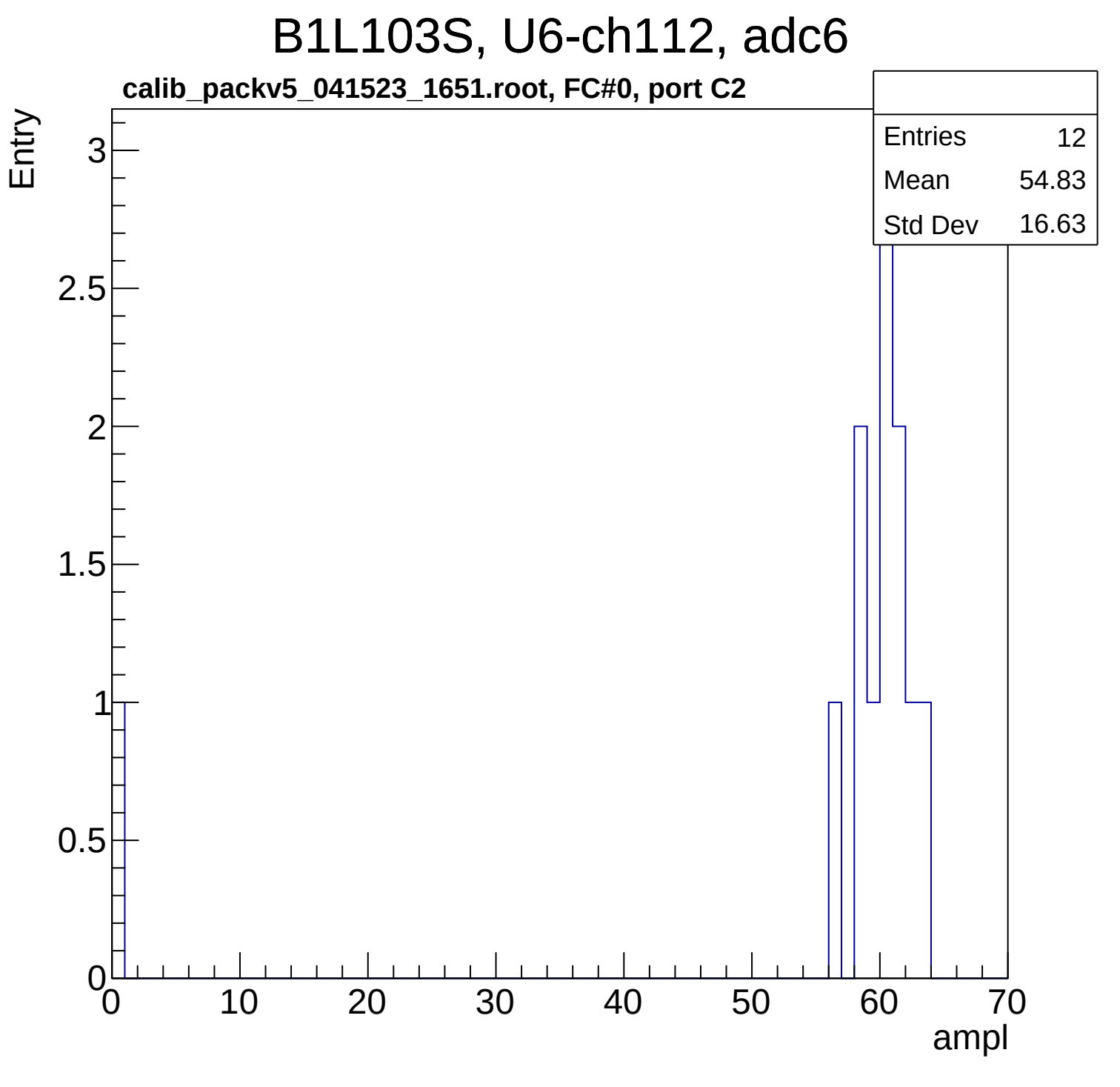
B1L103S, U6-ch112, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 54.83
Std Dev 16.63
Entry
ampl
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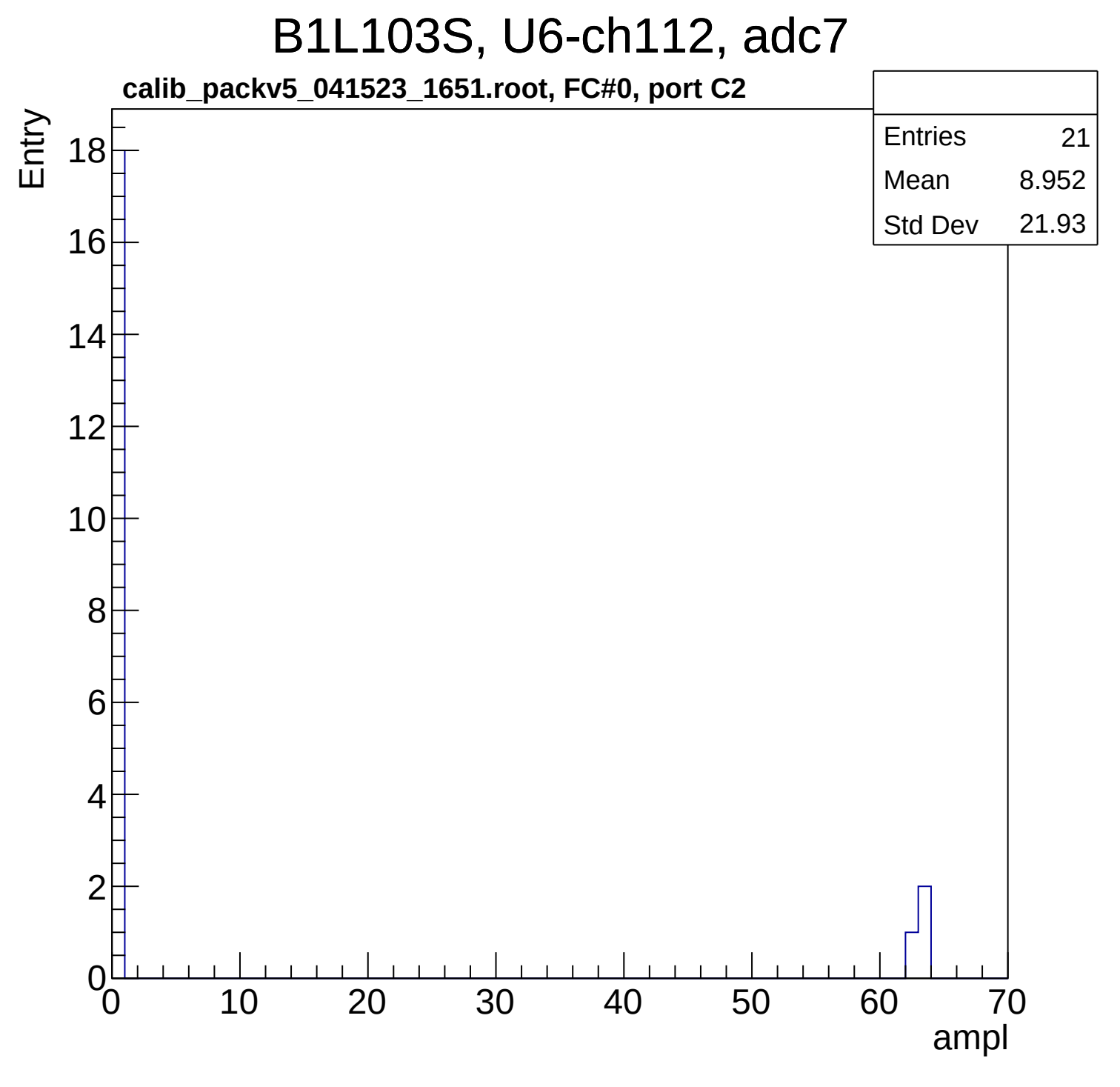
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U6-ch112, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 8.952
Std Dev 21.93
Entry
0
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6
8
10
12
14
16
18
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10
20
30
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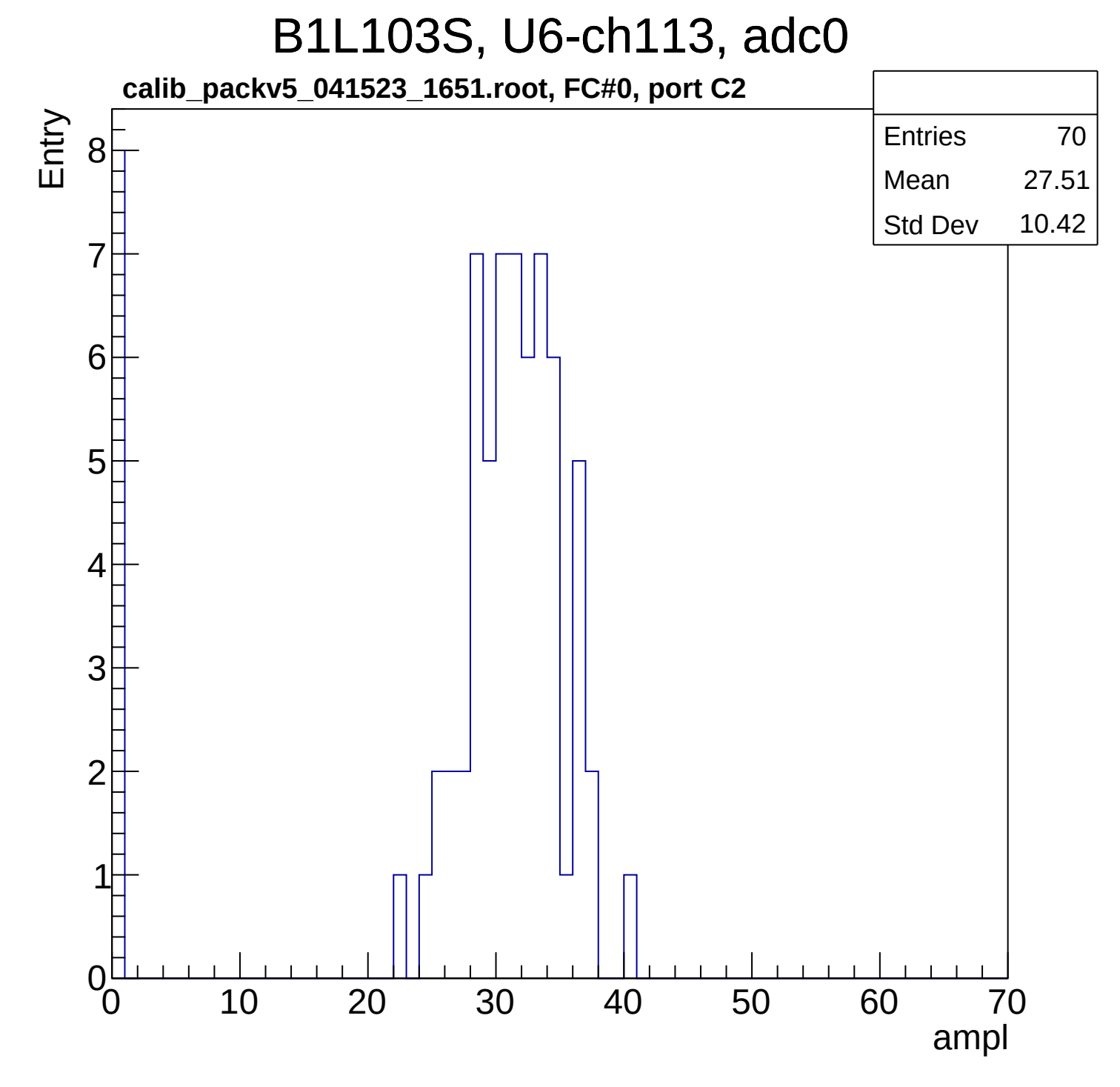
50
60
70
ampl


B1L103S, U6-ch113, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 27.51
Std Dev 10.42
Entry
ampl
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2
3
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7
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0
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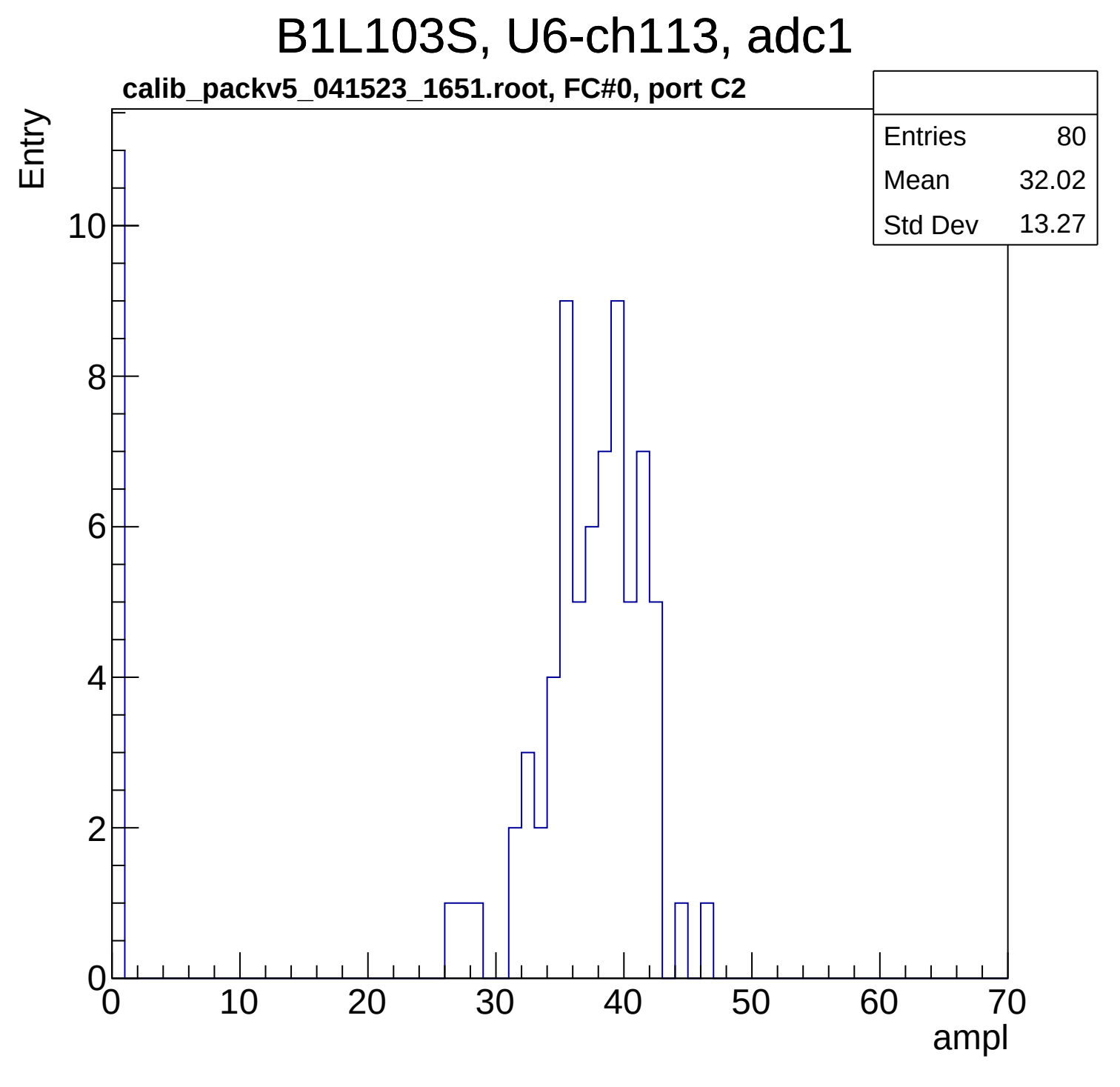
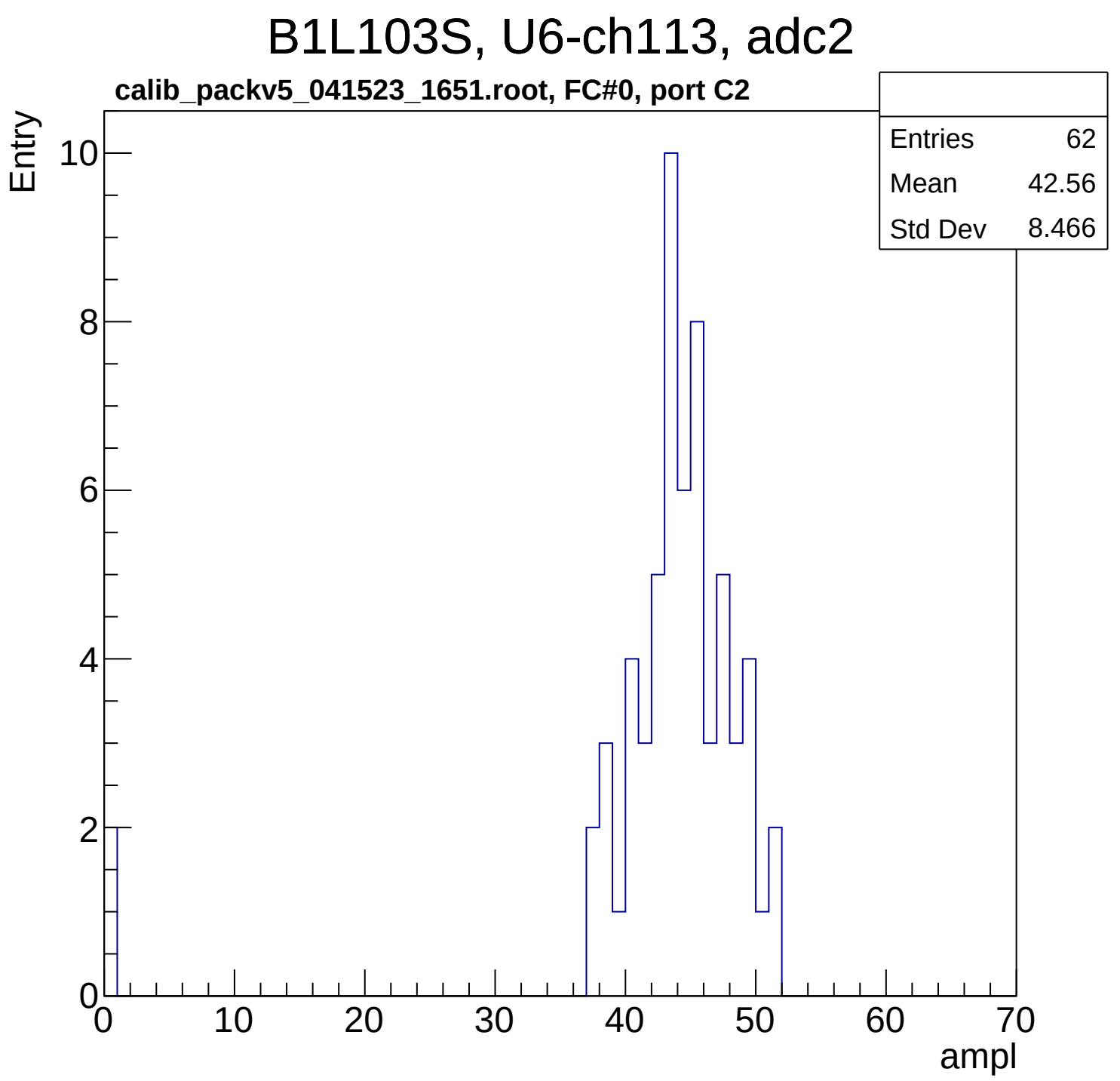

B1L103S, U6-ch113, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 32.02
Std Dev 13.27
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch113, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 42.56
Std Dev 8.466
Entry
ampl
0
2
4
6
8
10
0
10
20
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40
50
60
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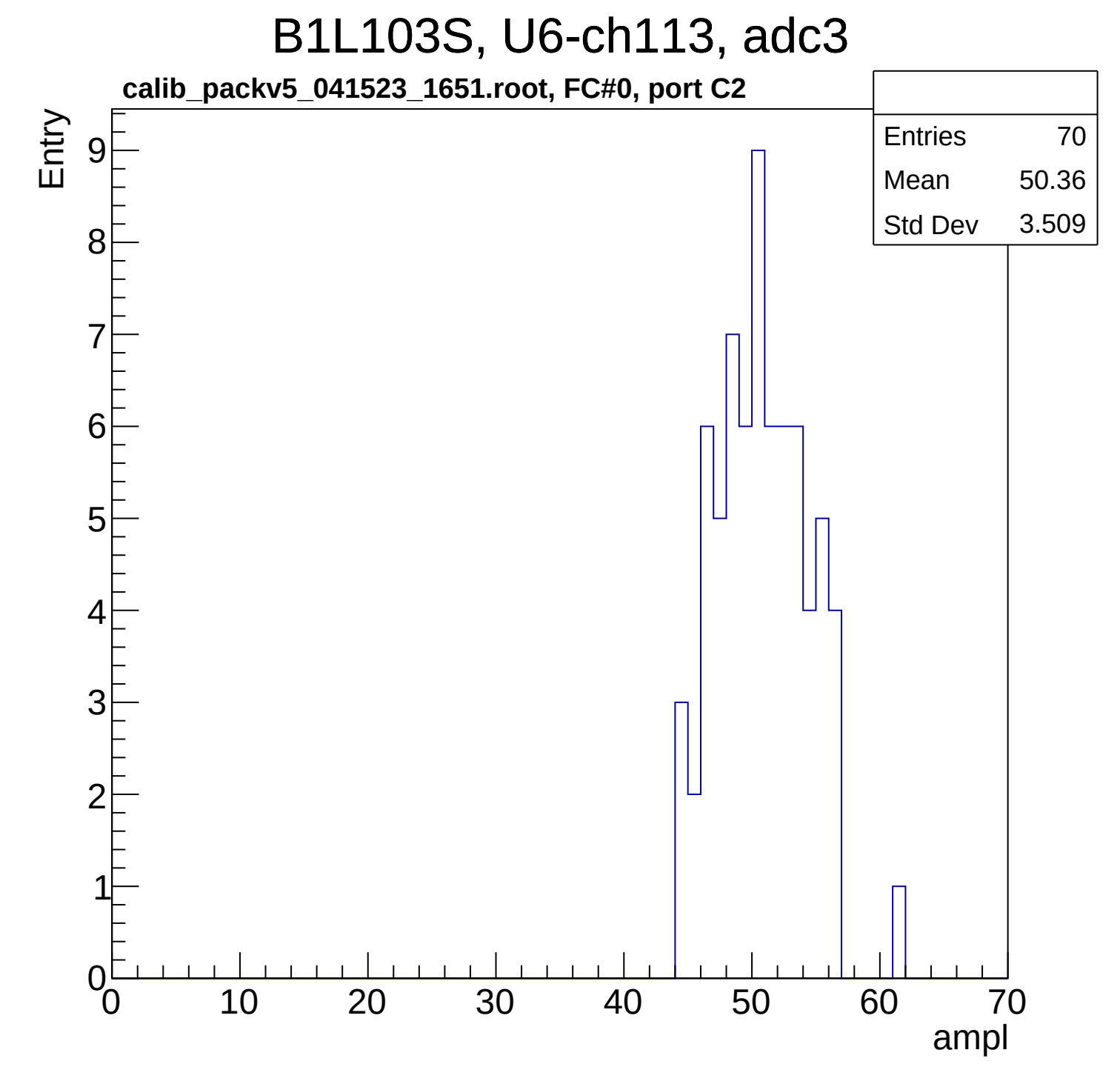
B1L103S, U6-ch113, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 50.36
Std Dev 3.509
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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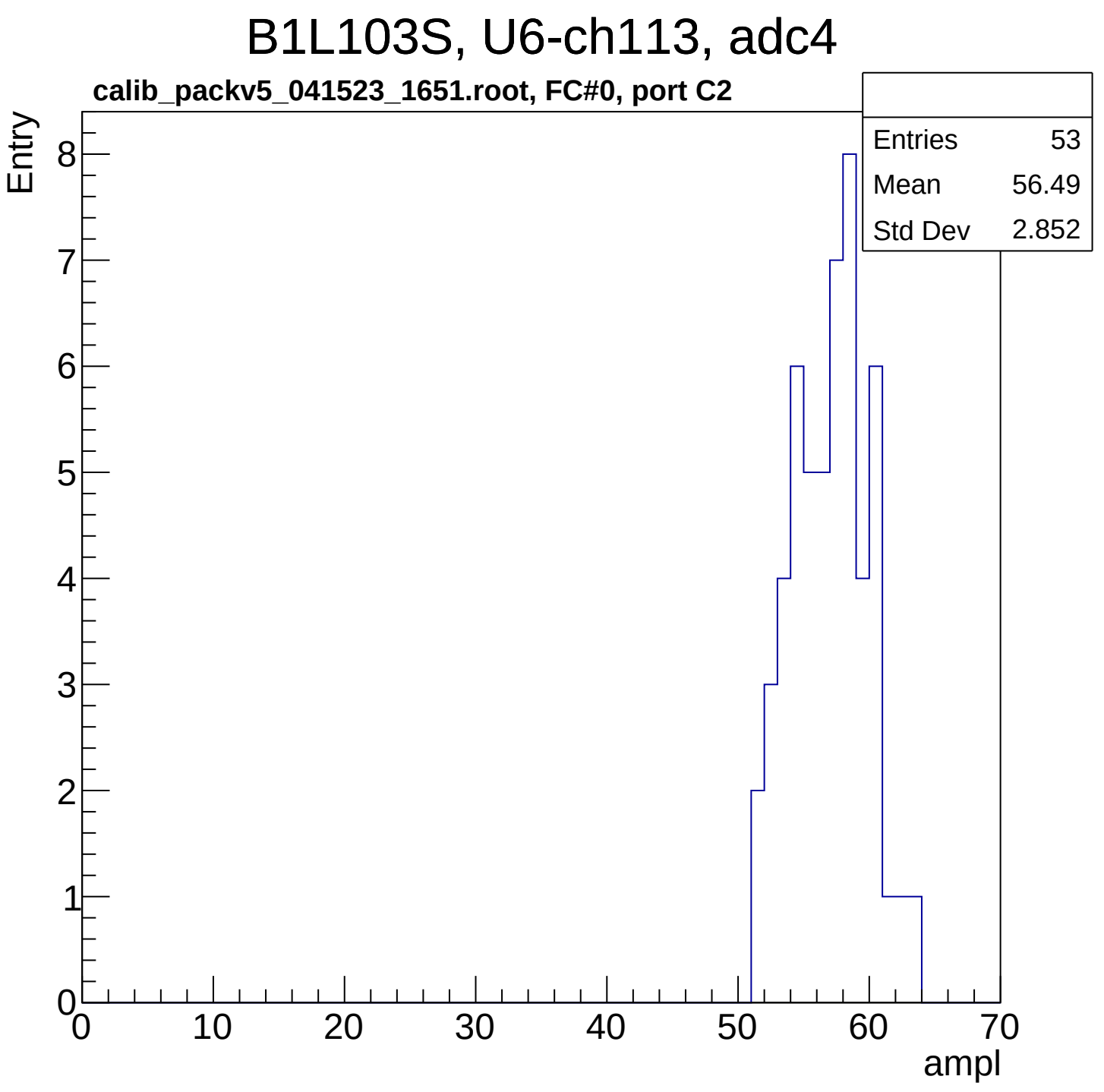
B1L103S, U6-ch113, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 56.49
Std Dev 2.852
Entry
ampl
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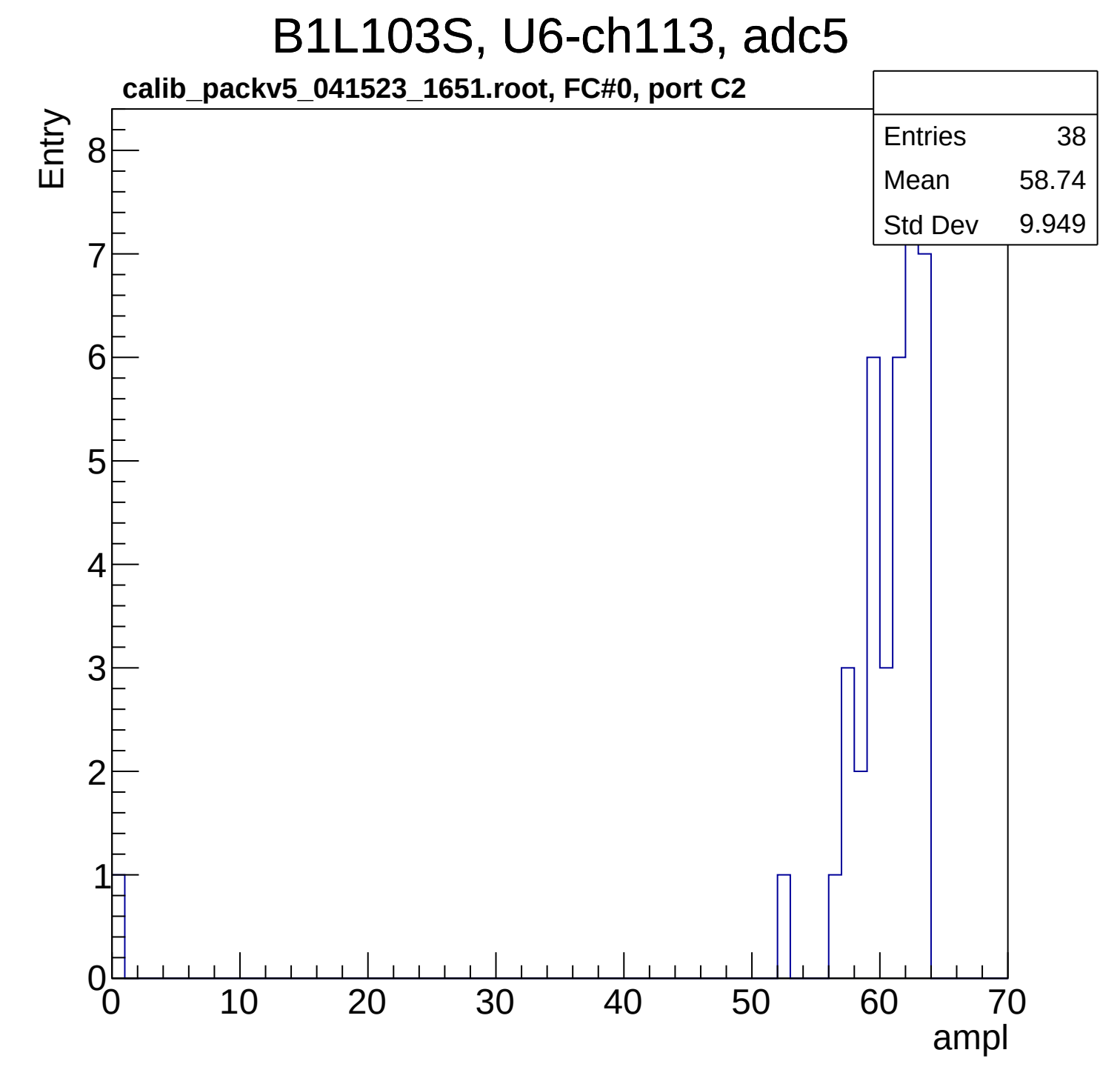
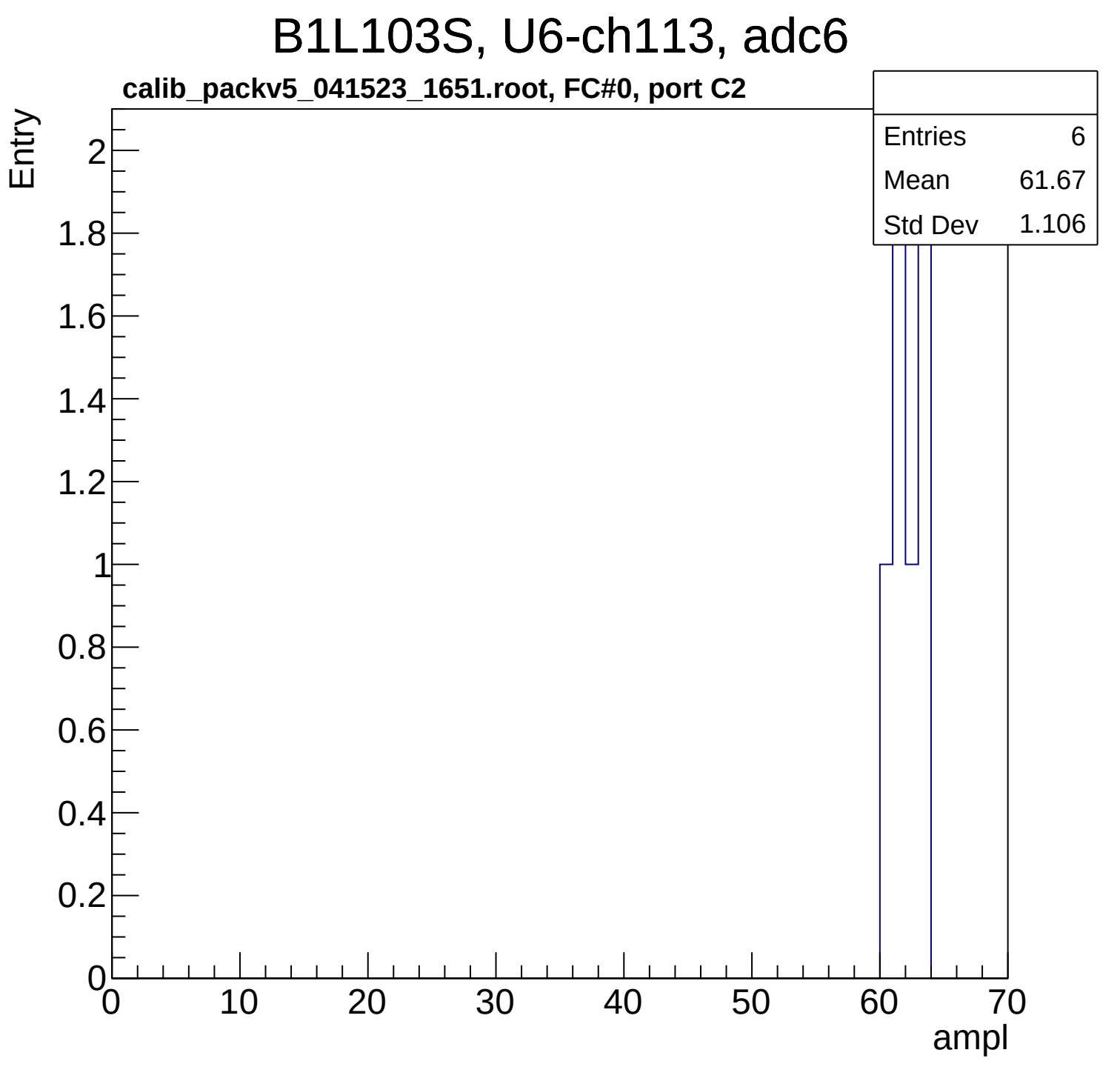
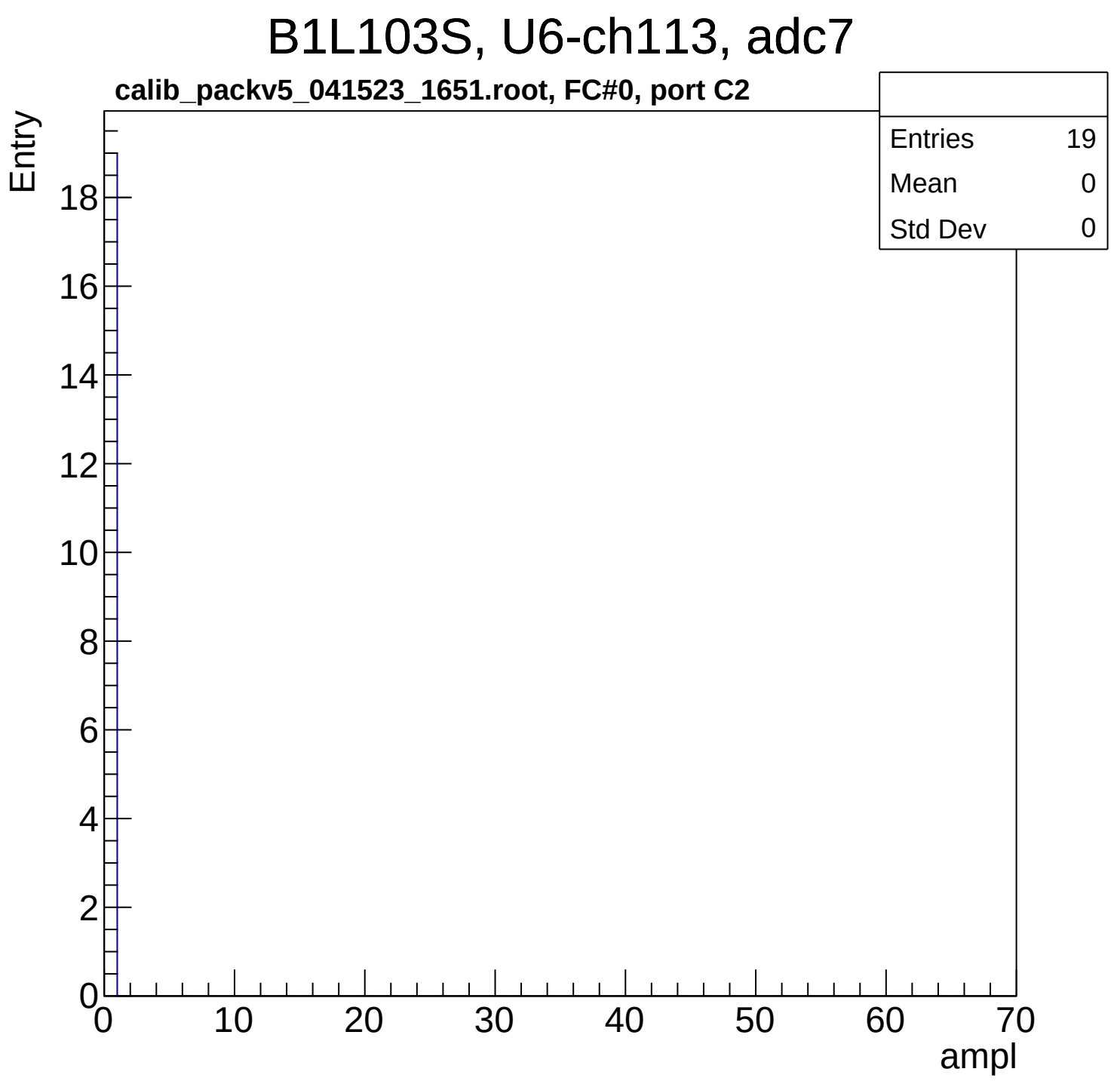
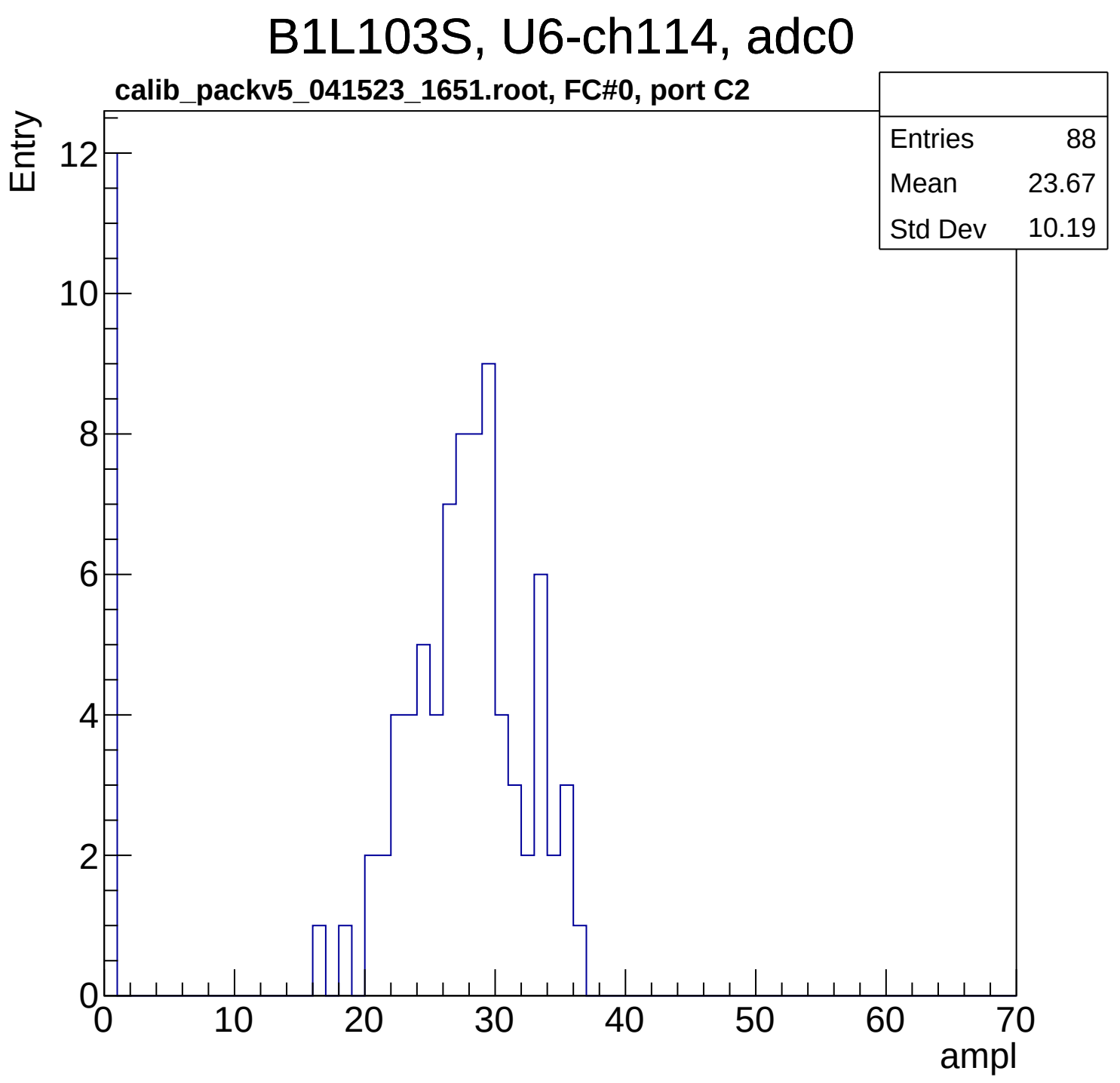
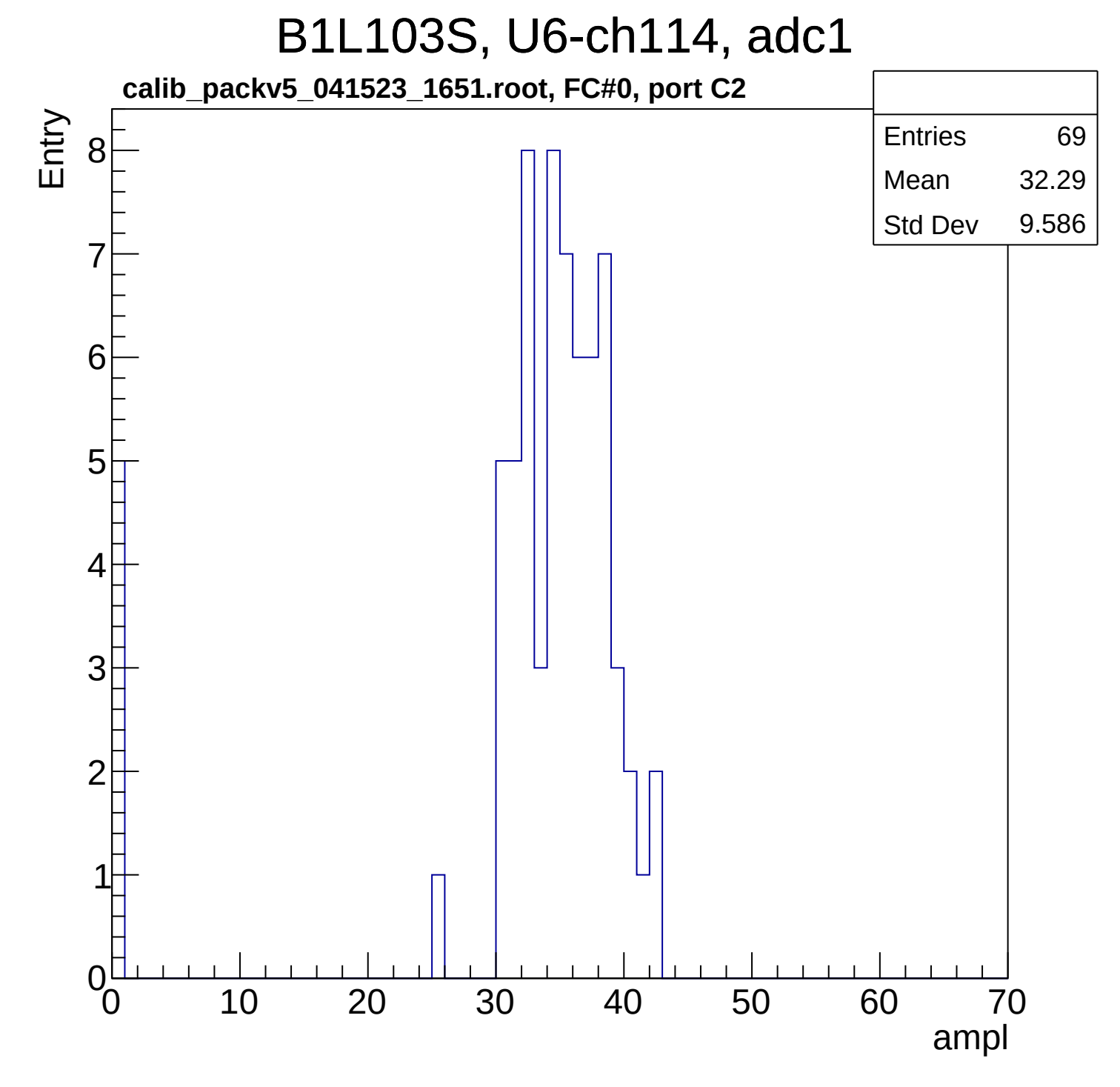
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

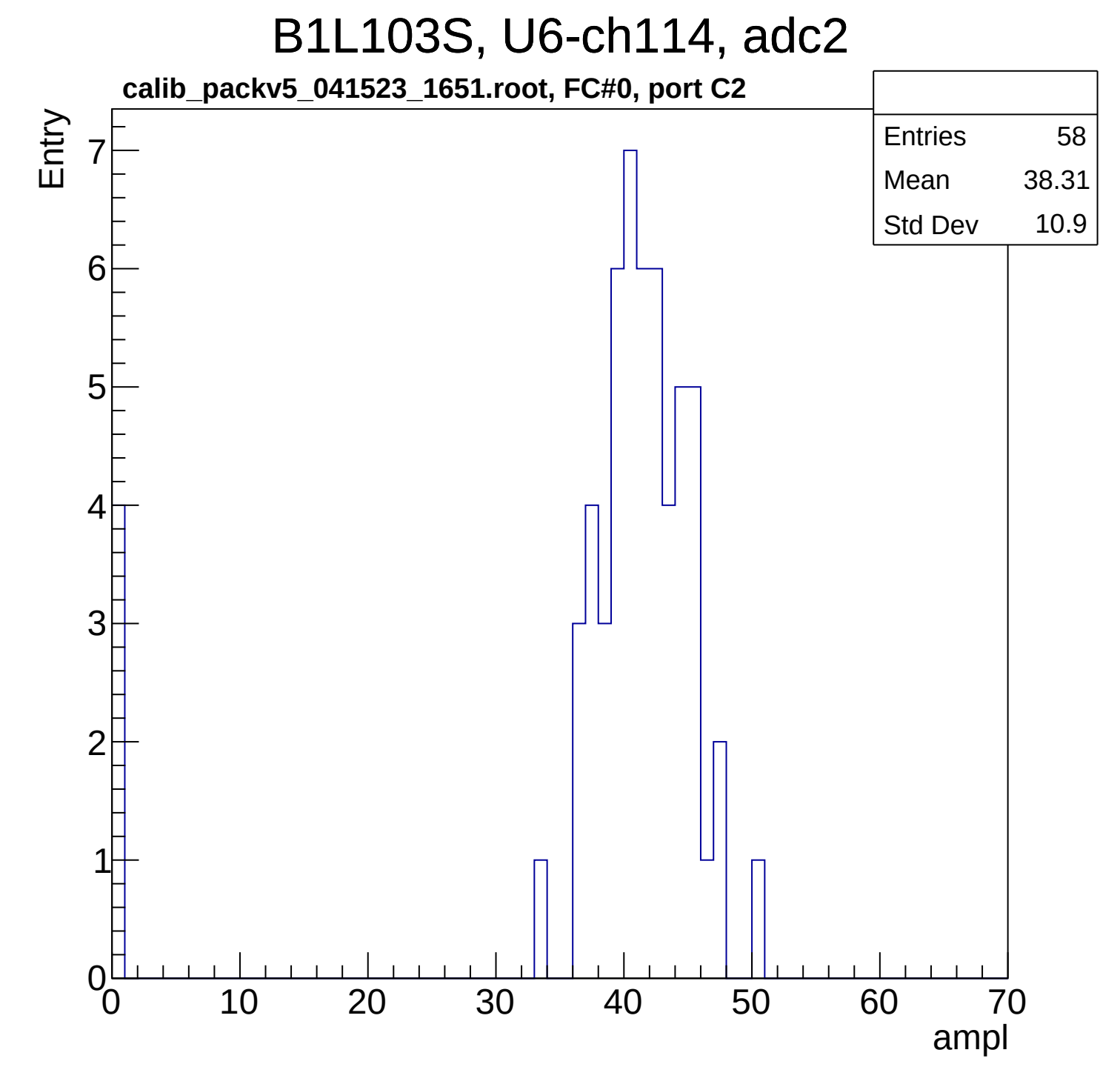

B1L103S, U6-ch113, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 58.74
Std Dev 9.949
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

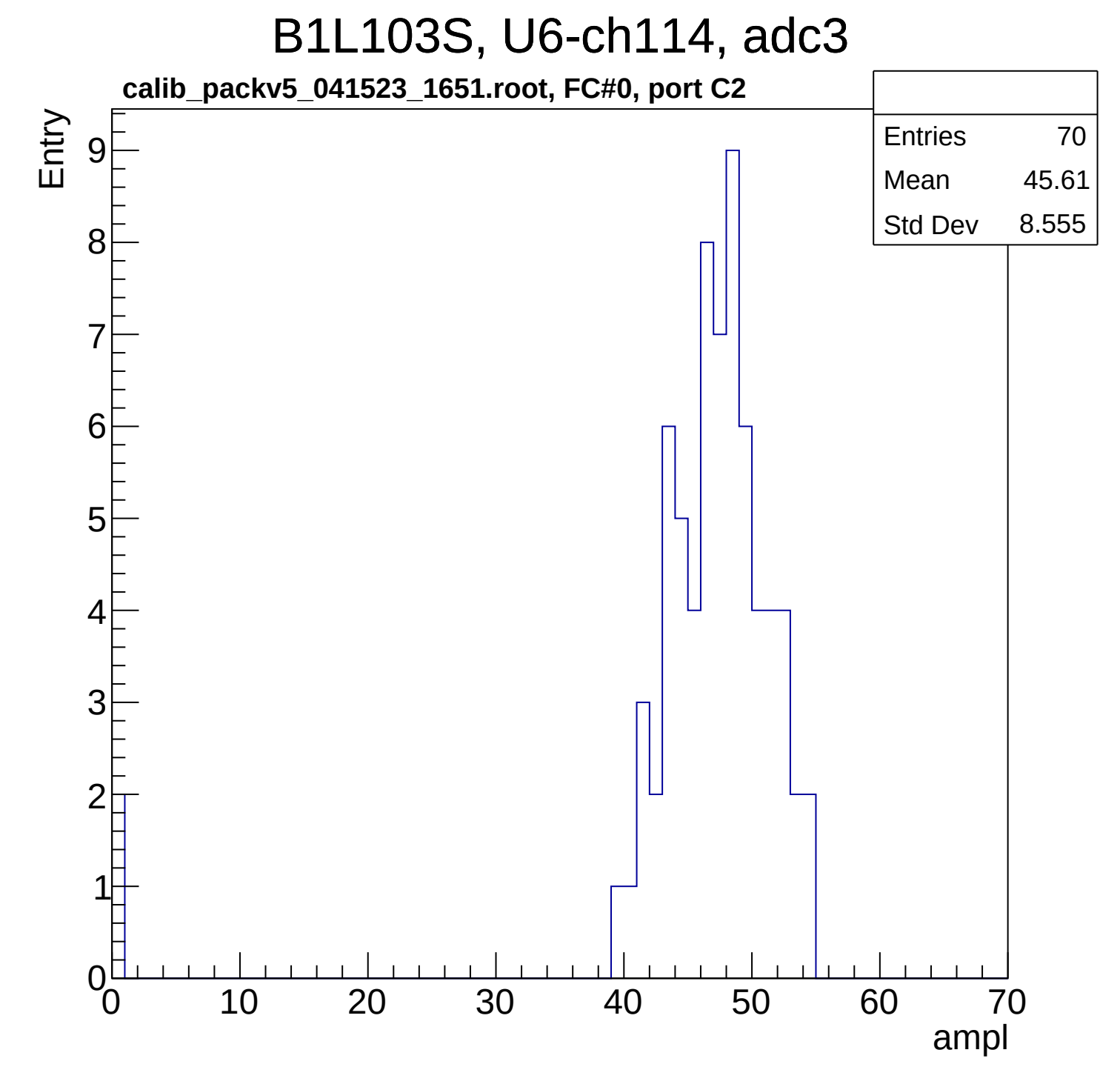

B1L103S, U6-ch113, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 61.67
Std Dev 1.106
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

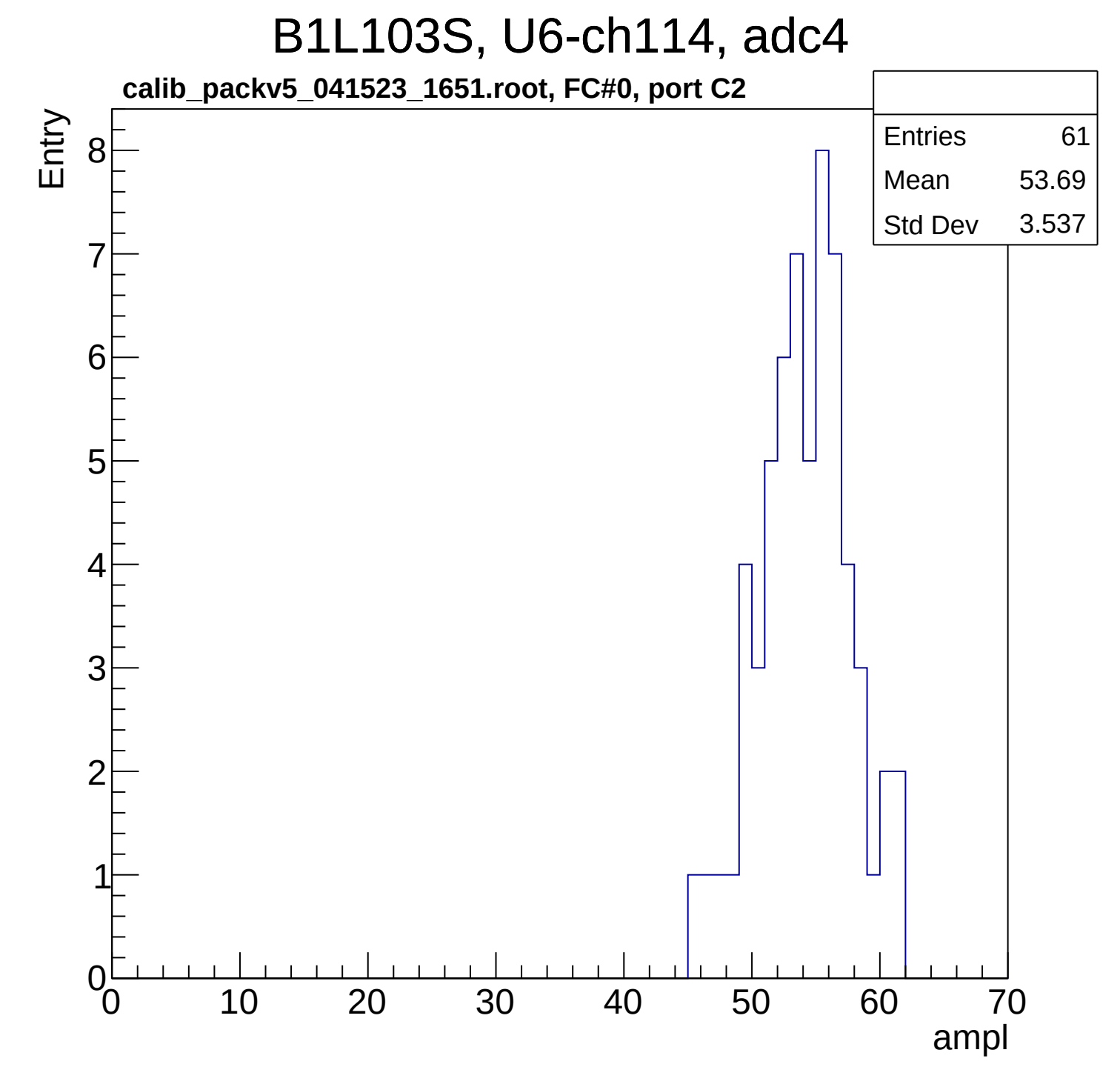

B1L103S, U6-ch113, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

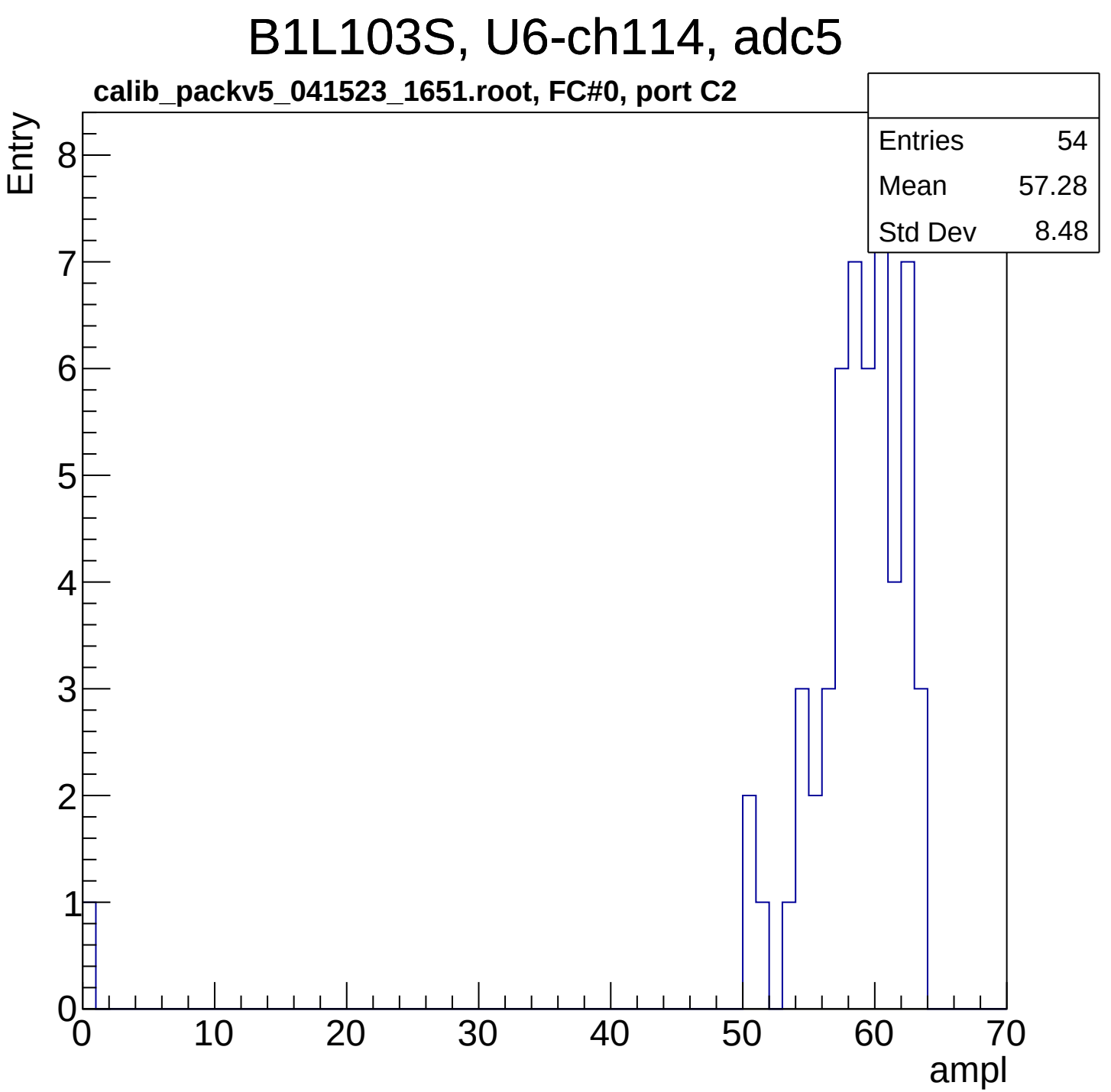

B1L103S, U6-ch114, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 23.67
Std Dev 10.19
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch114, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 32.29
Std Dev 9.586
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch114, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 38.31
Std Dev 10.9
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch114, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 45.61
Std Dev 8.555
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch114, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 53.69
Std Dev 3.537
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch114, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 57.28
Std Dev 8.48
Entry
ampl
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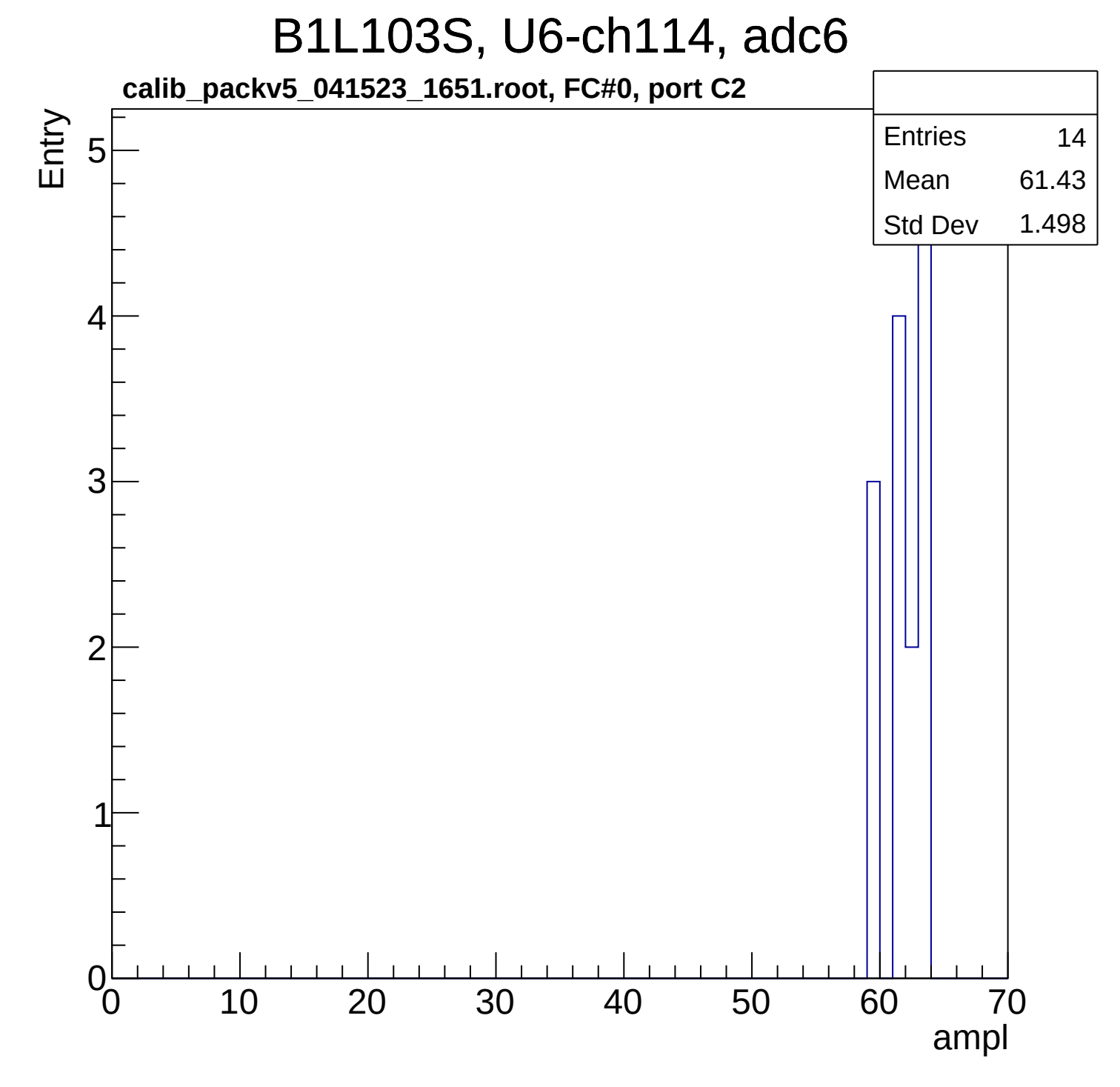
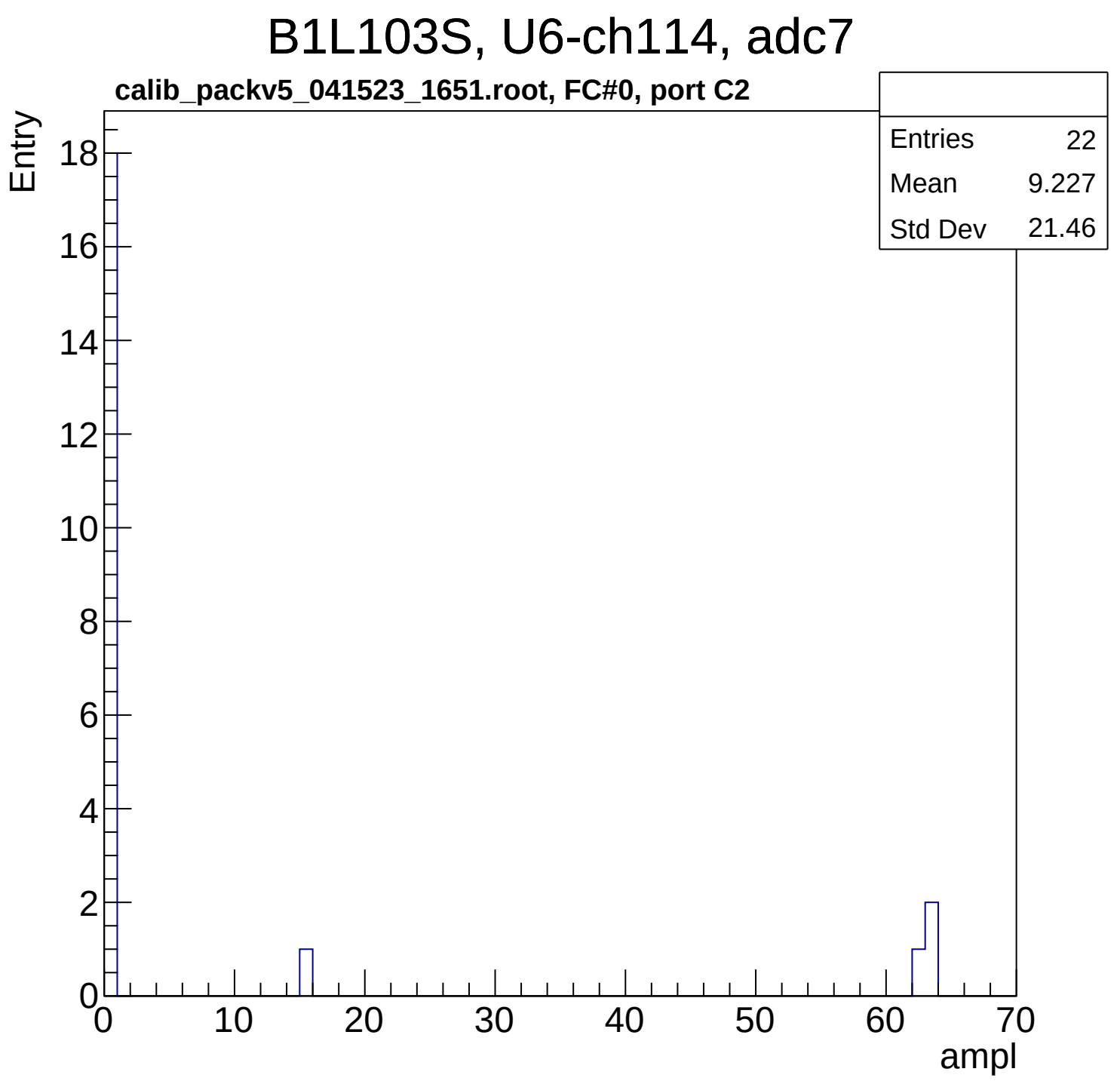
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch114, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 61.43
Std Dev 1.498
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U6-ch114, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 9.227
Std Dev 21.46
Entry
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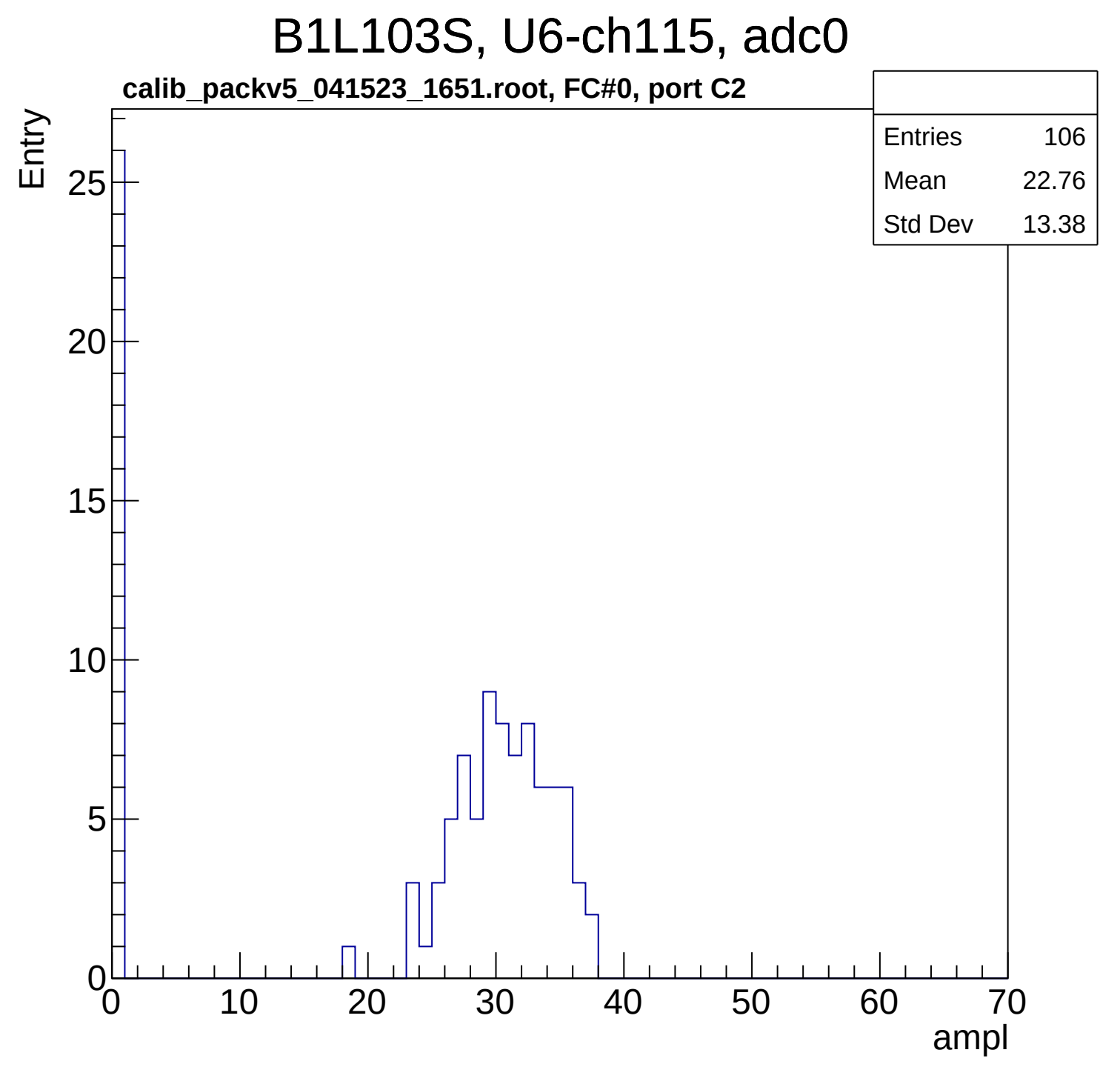
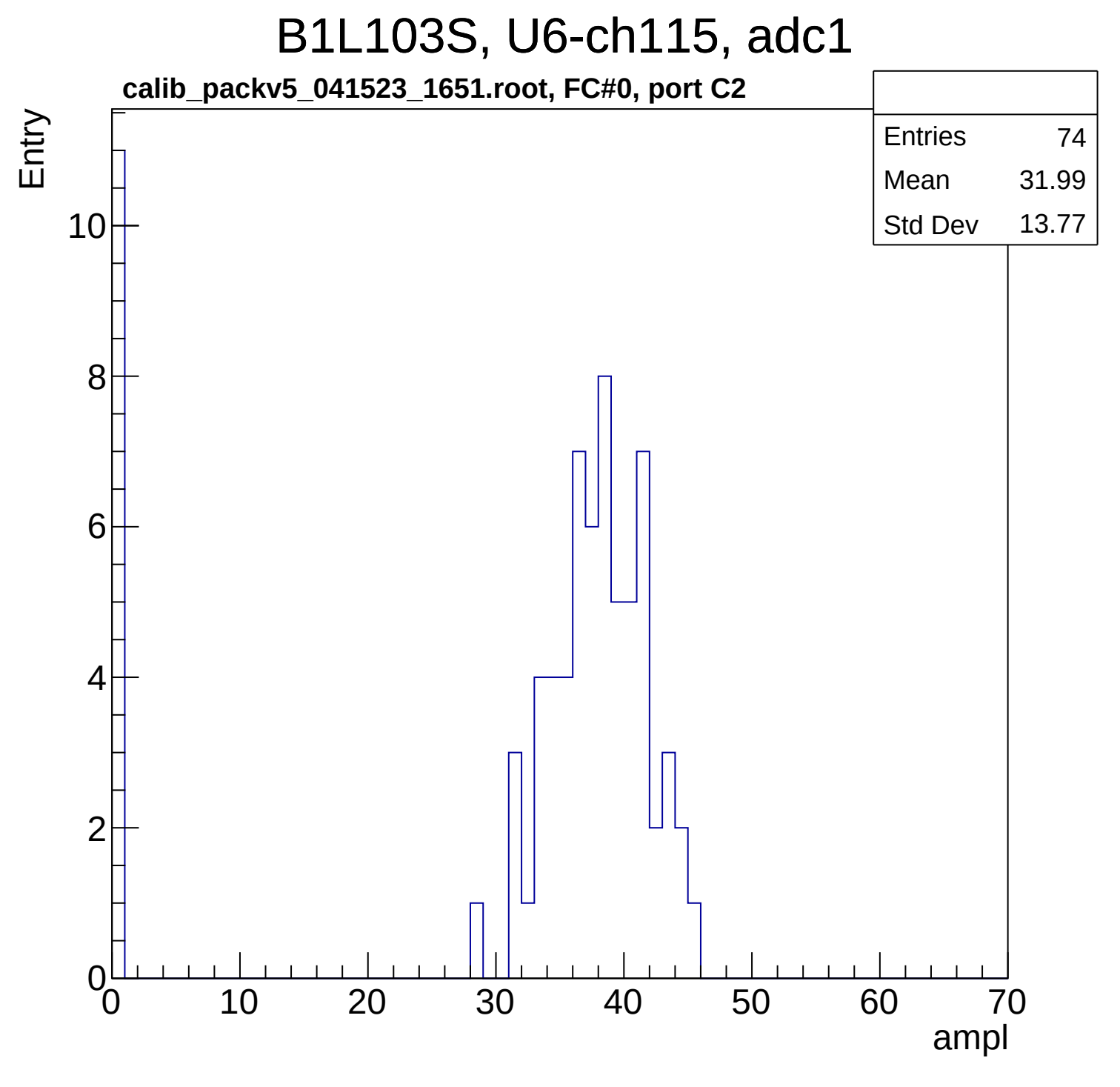
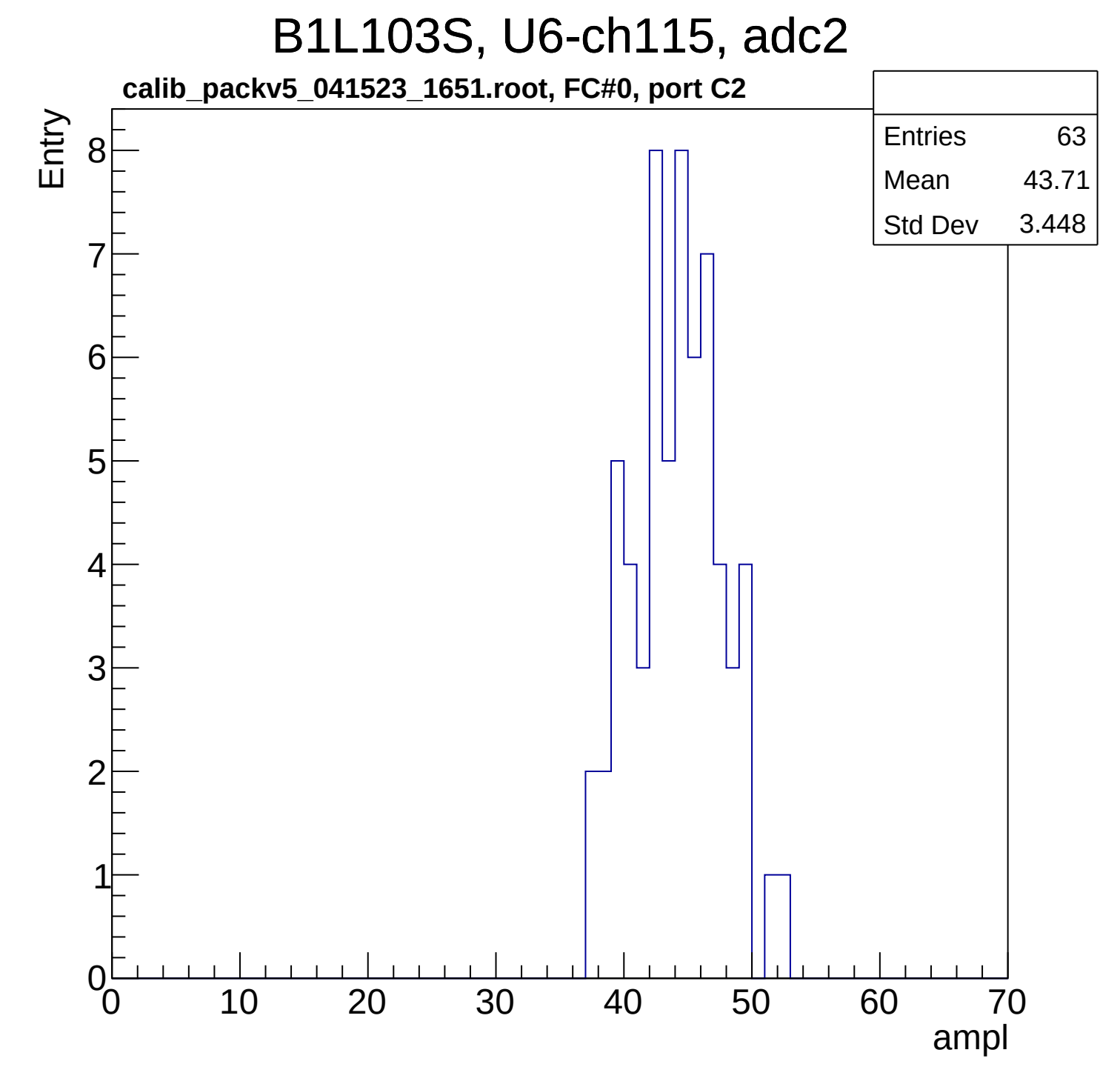
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch115, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 106
Mean 22.76
Std Dev 13.38
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch115, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 31.99
Std Dev 13.77
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch115, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 43.71
Std Dev 3.448
Entry
ampl
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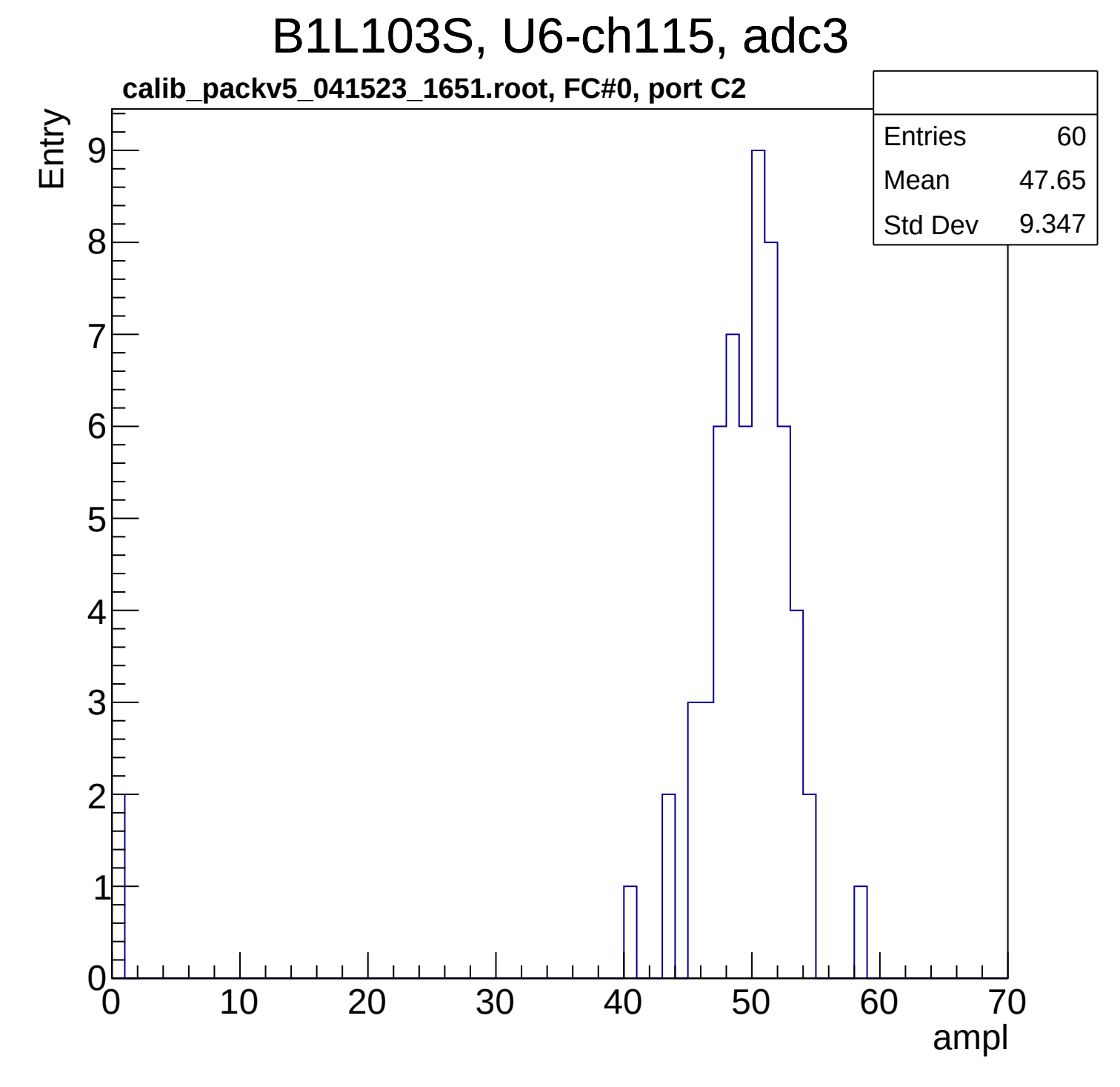
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch115, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 47.65
Std Dev 9.347
Entry
ampl
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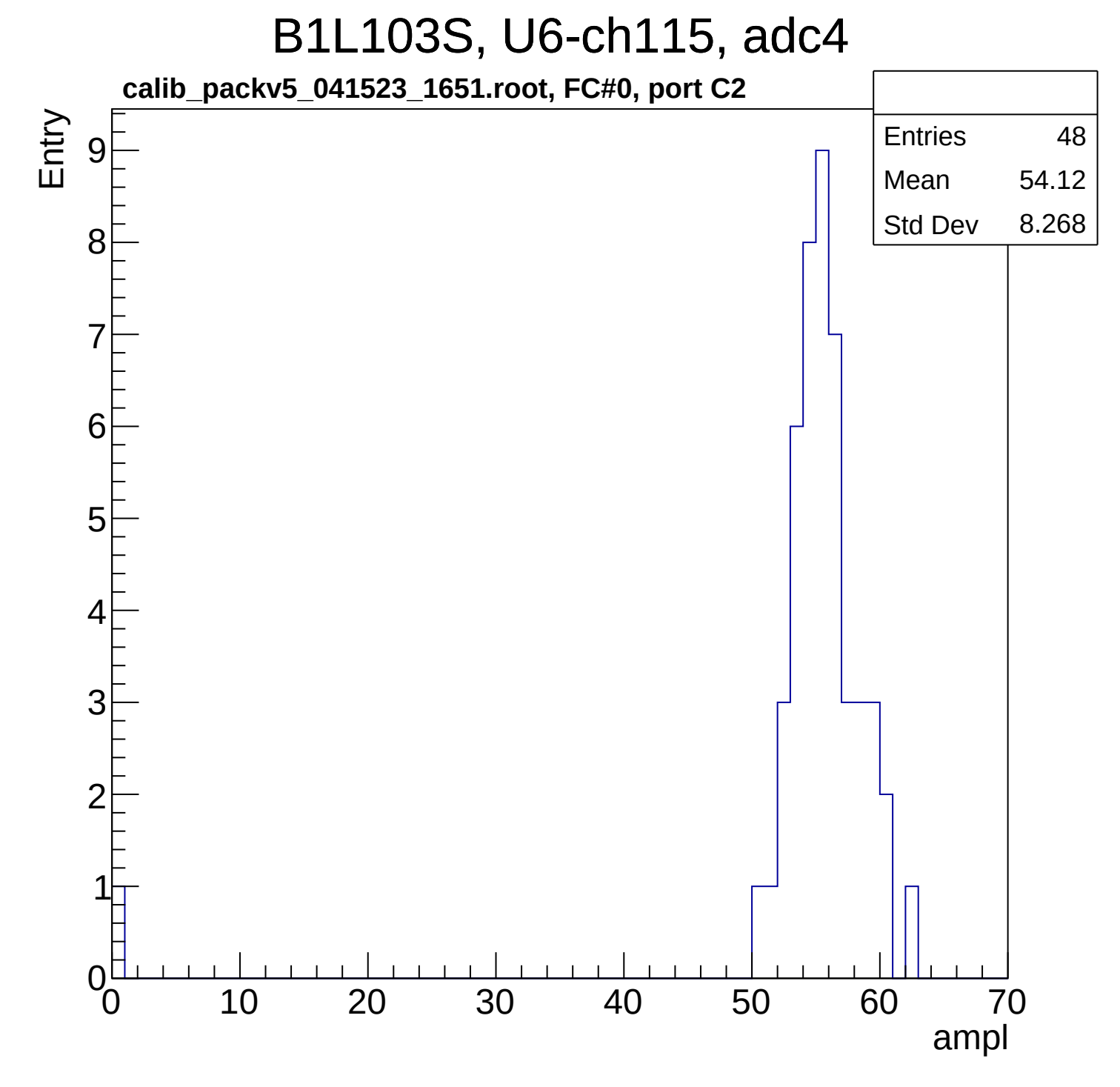
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch115, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 54.12
Std Dev 8.268
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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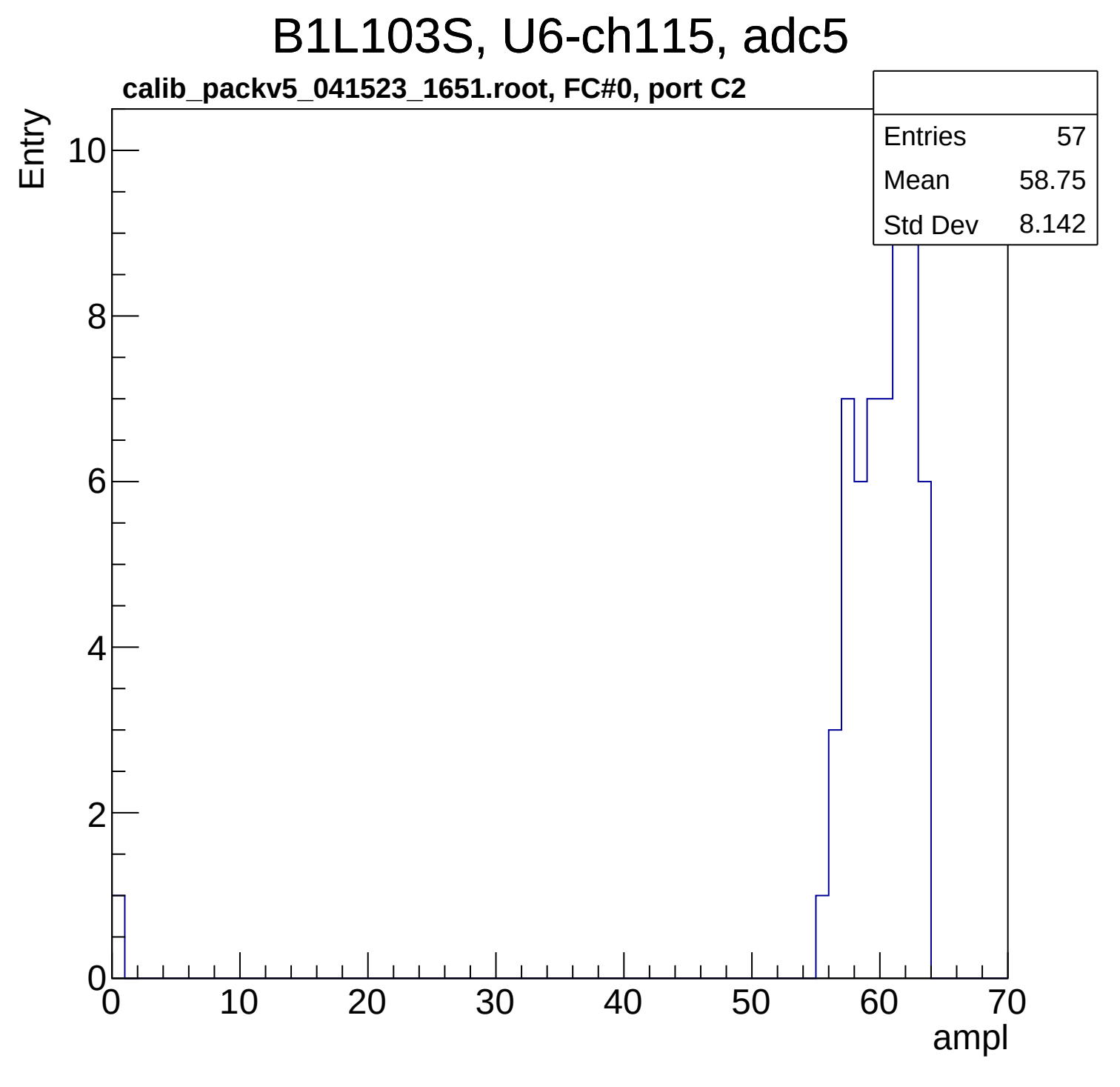
B1L103S, U6-ch115, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 58.75
Std Dev 8.142
Entry
ampl
0
2
4
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8
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0
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40
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60
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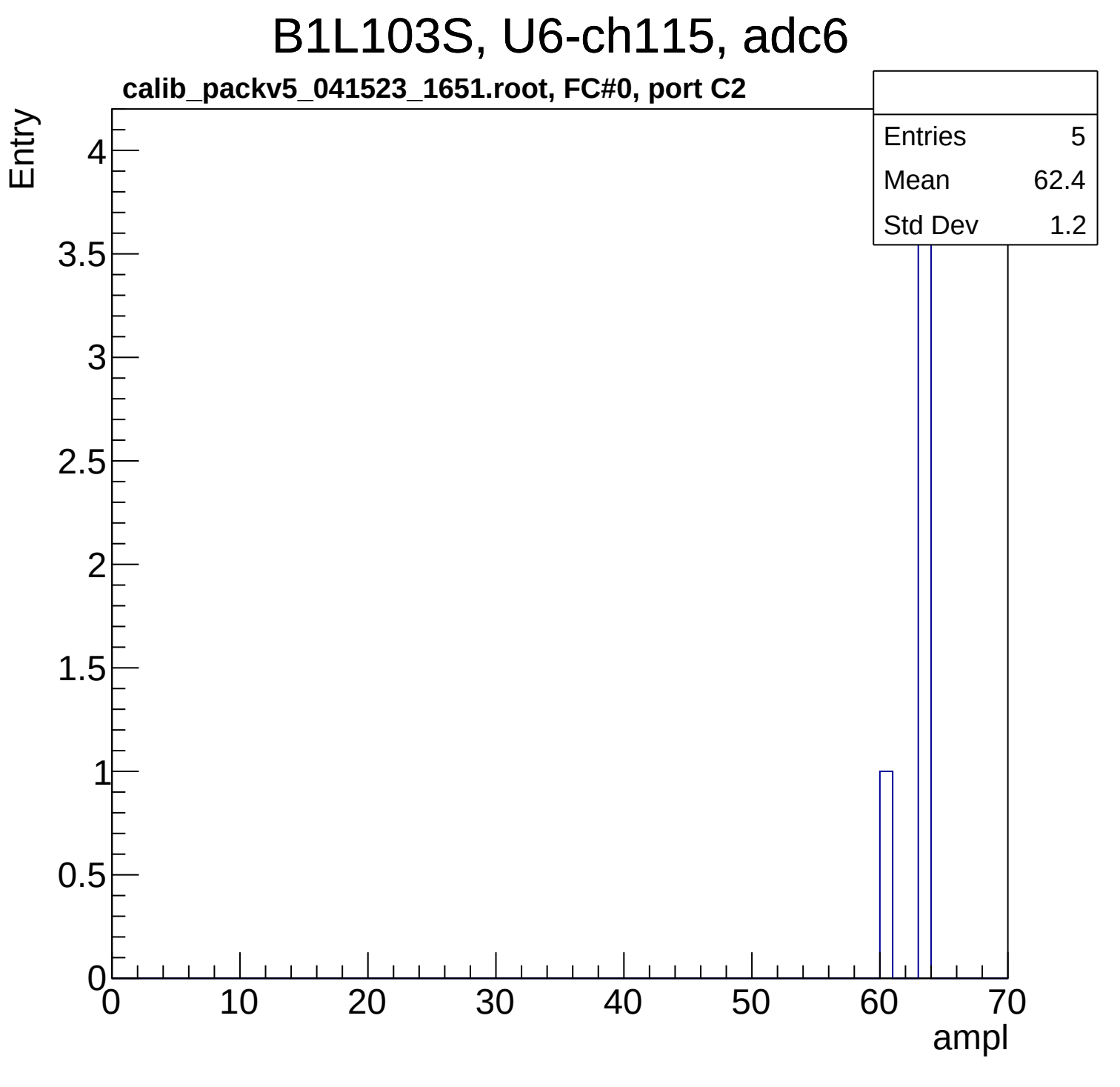
B1L103S, U6-ch115, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 62.4
Std Dev 1.2
Entry
ampl
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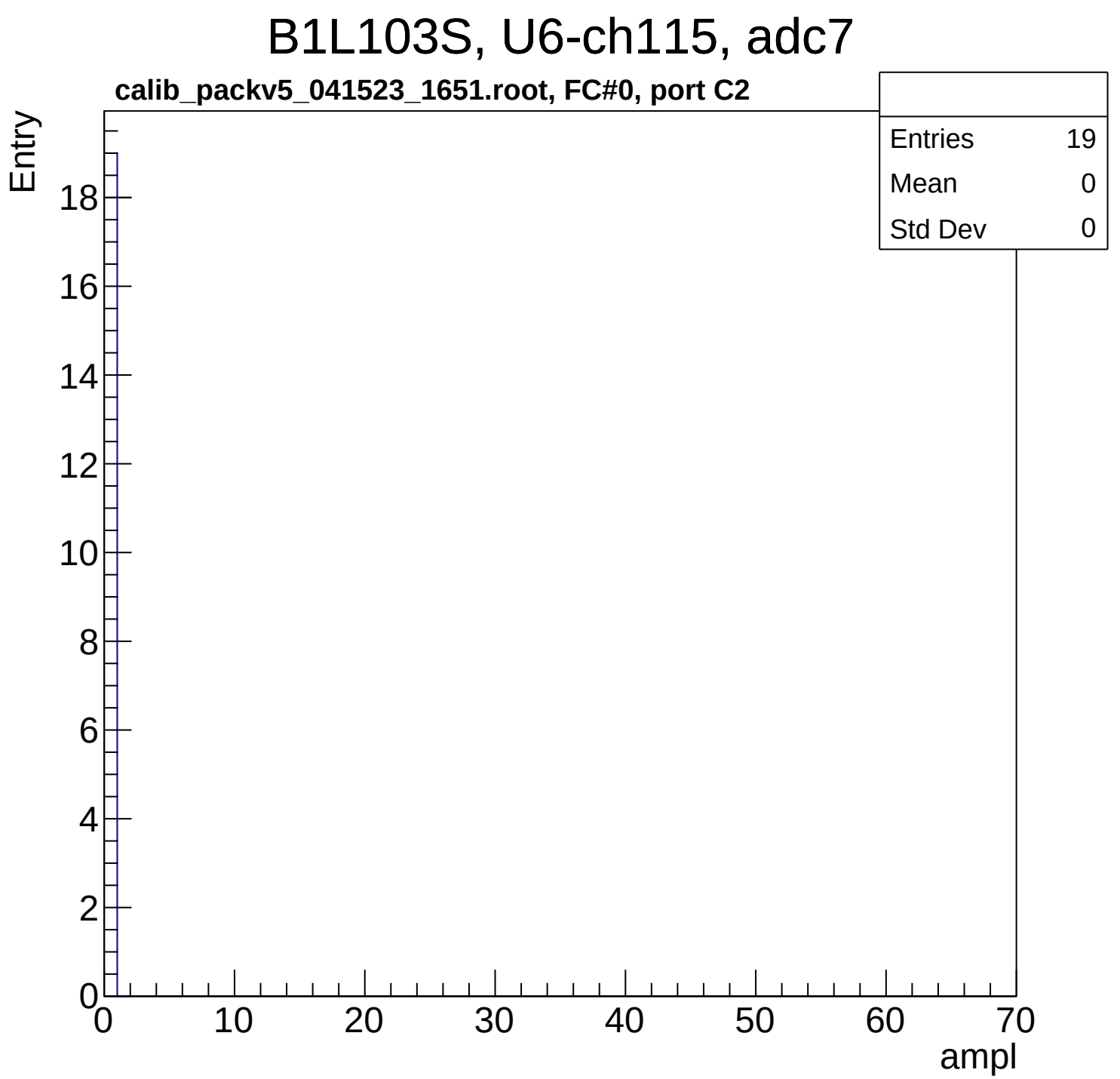
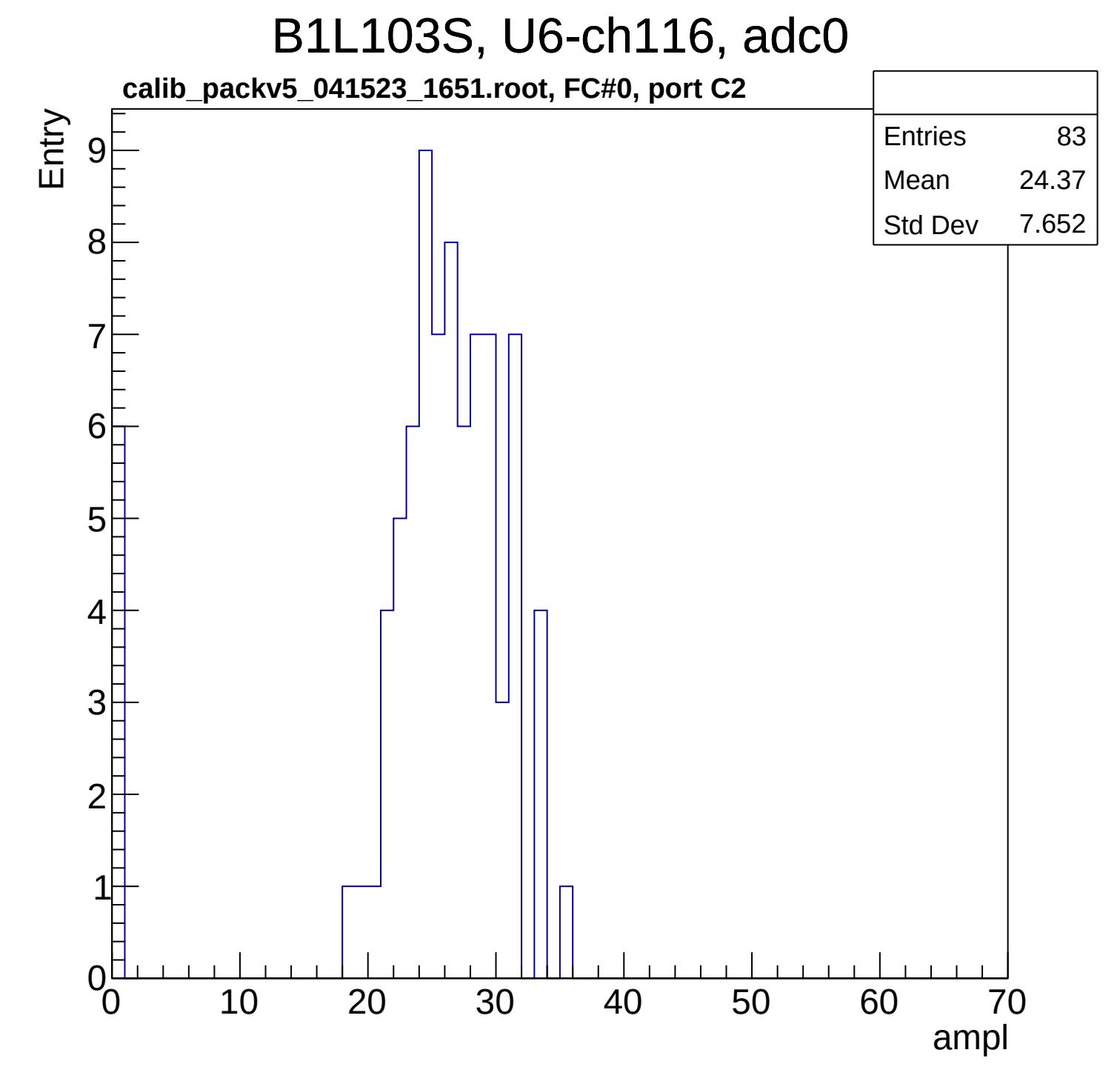
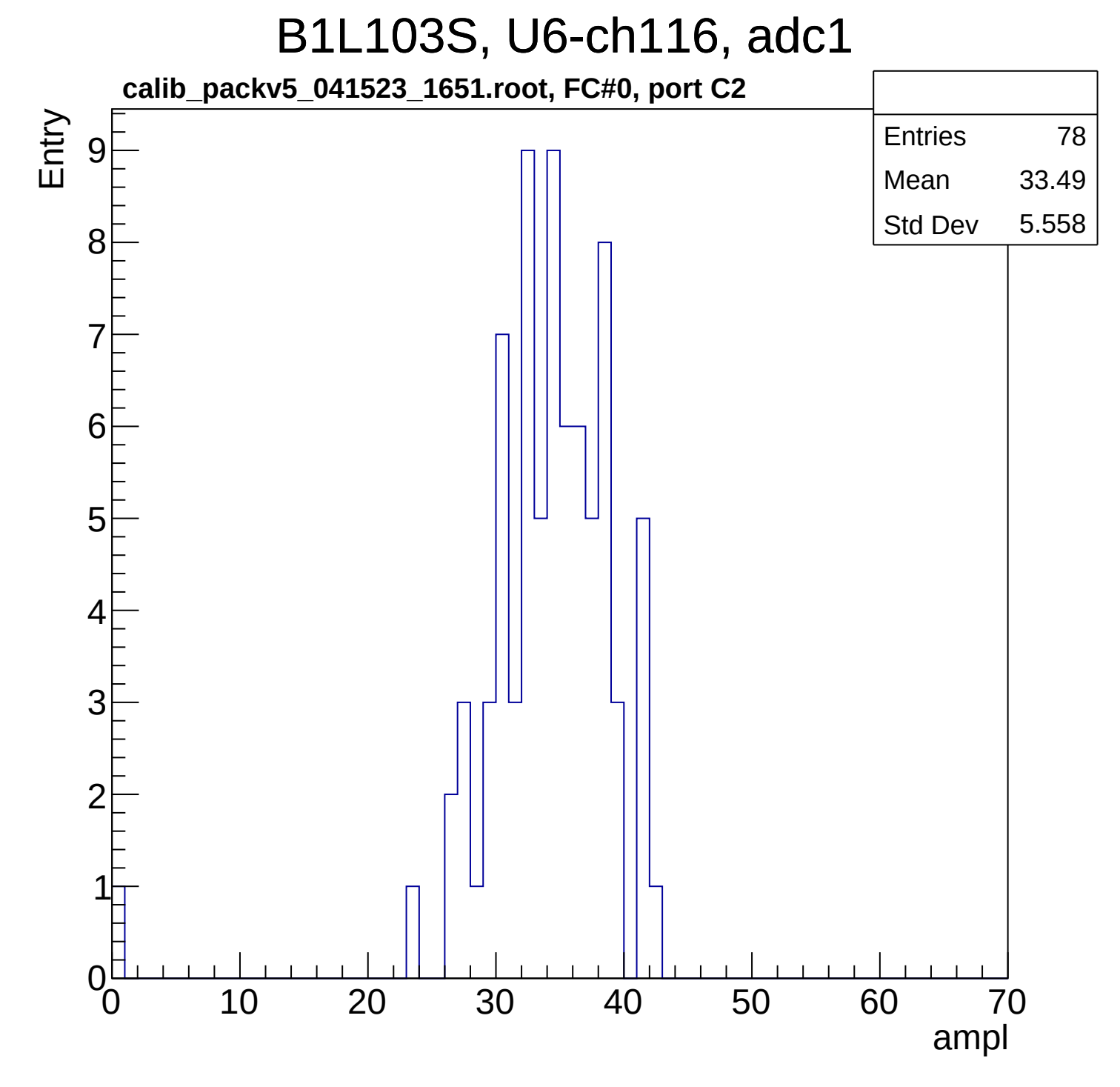
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U6-ch115, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch116, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 24.37
Std Dev 7.652
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch116, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 33.49
Std Dev 5.558
Entry
ampl
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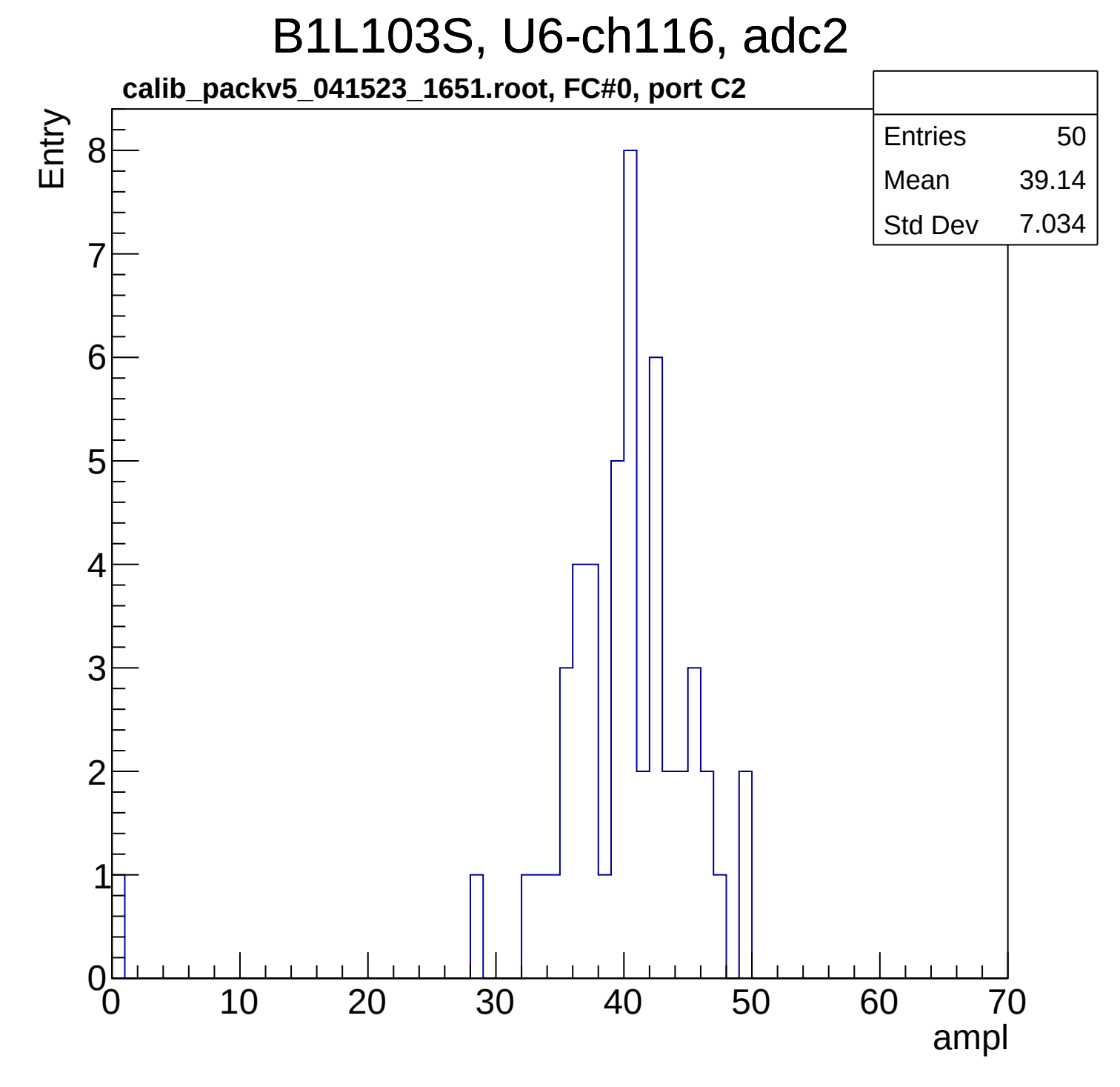
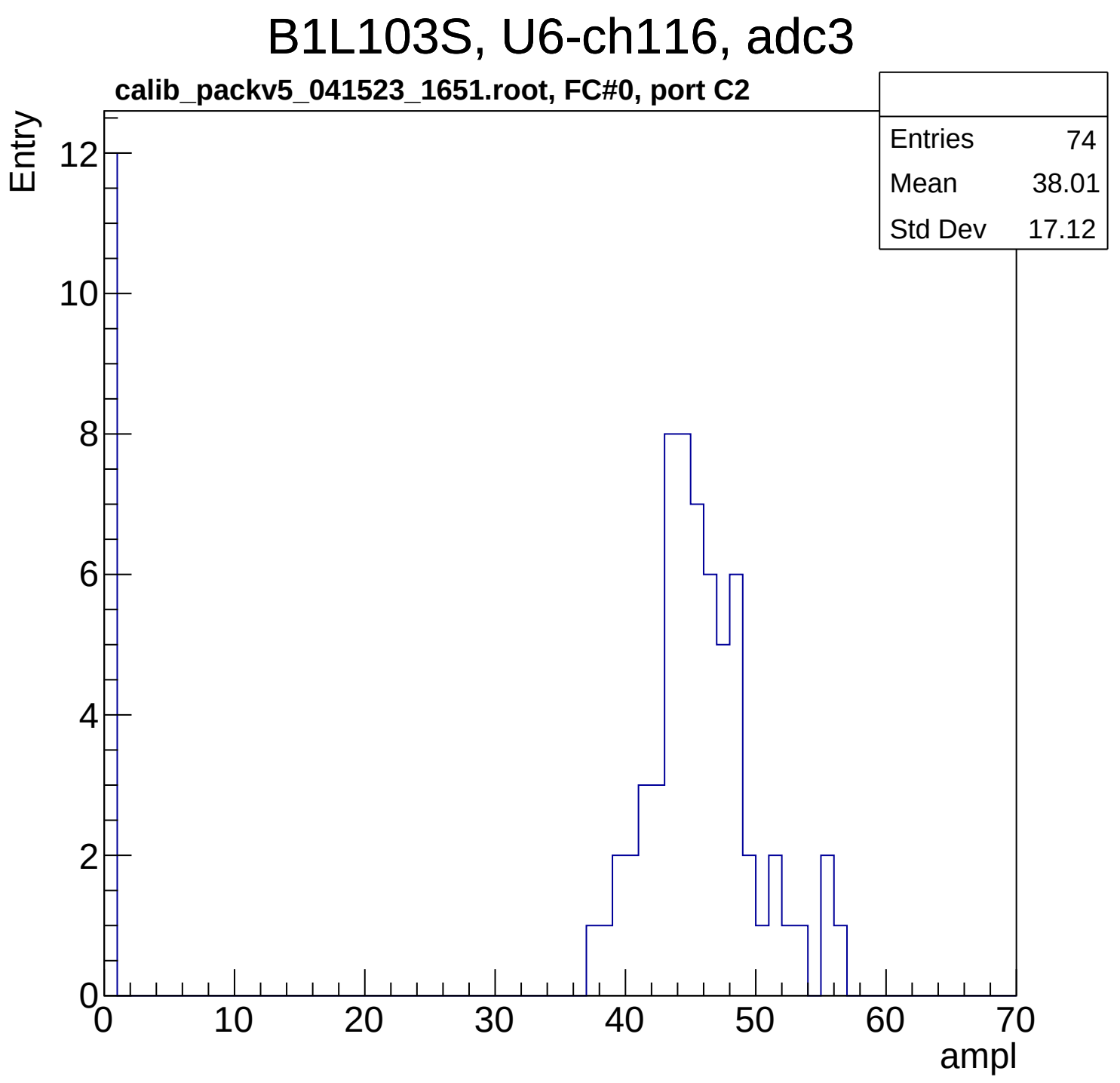
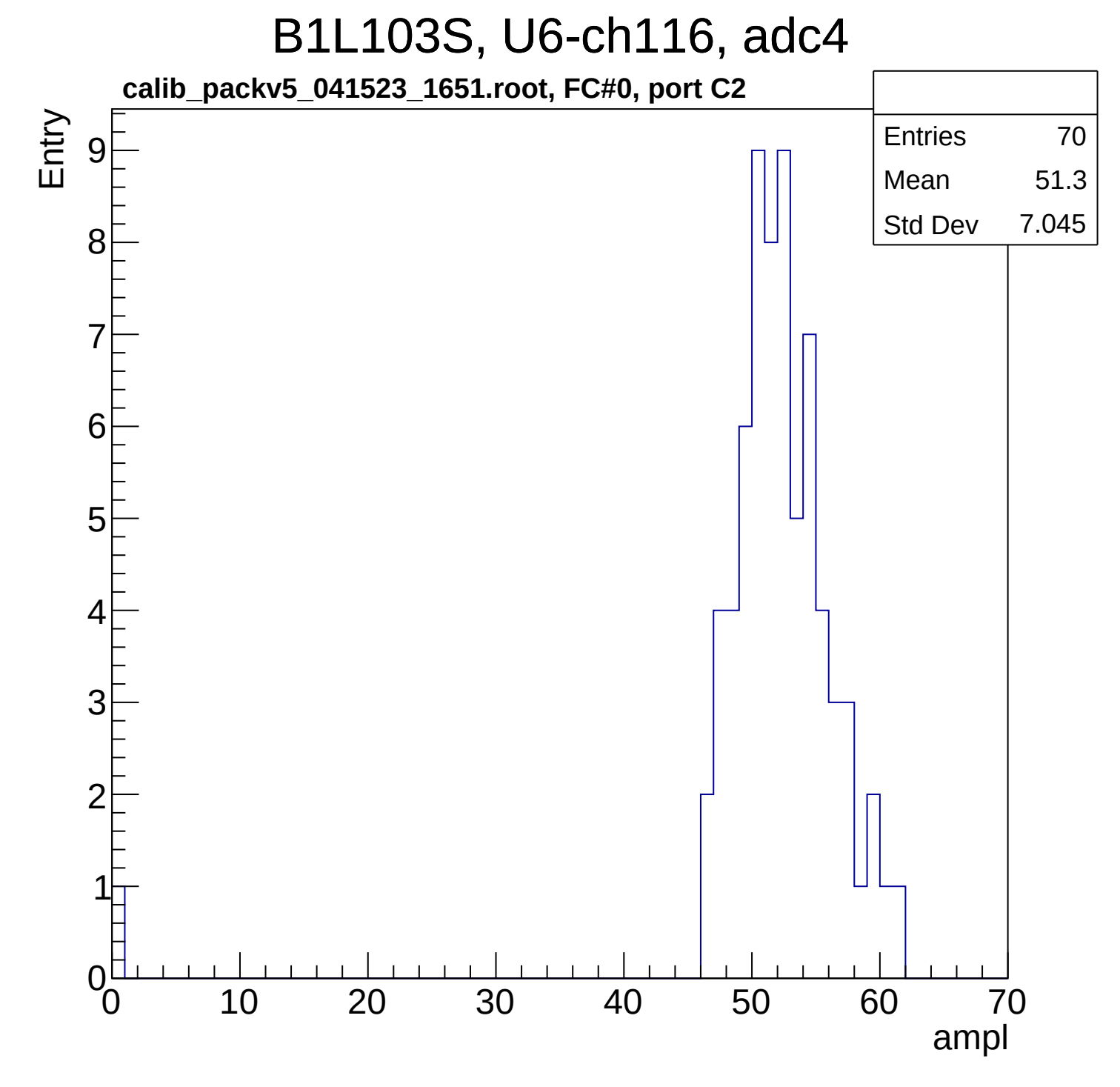
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch116, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 39.14
Std Dev 7.034
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch116, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 38.01
Std Dev 17.12
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch116, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 51.3
Std Dev 7.045
Entry
ampl
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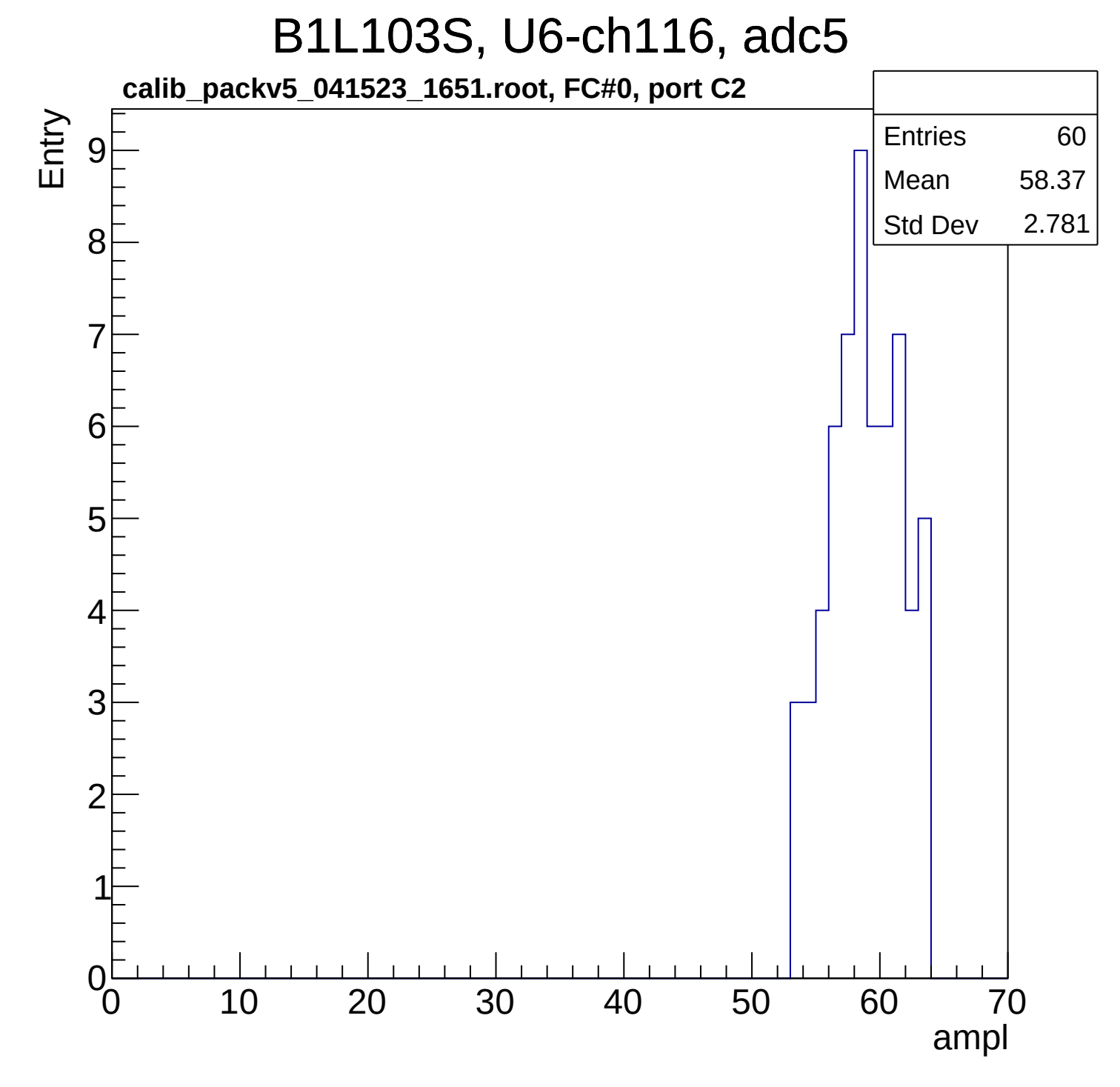
B1L103S, U6-ch116, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 58.37
Std Dev 2.781
Entry
ampl
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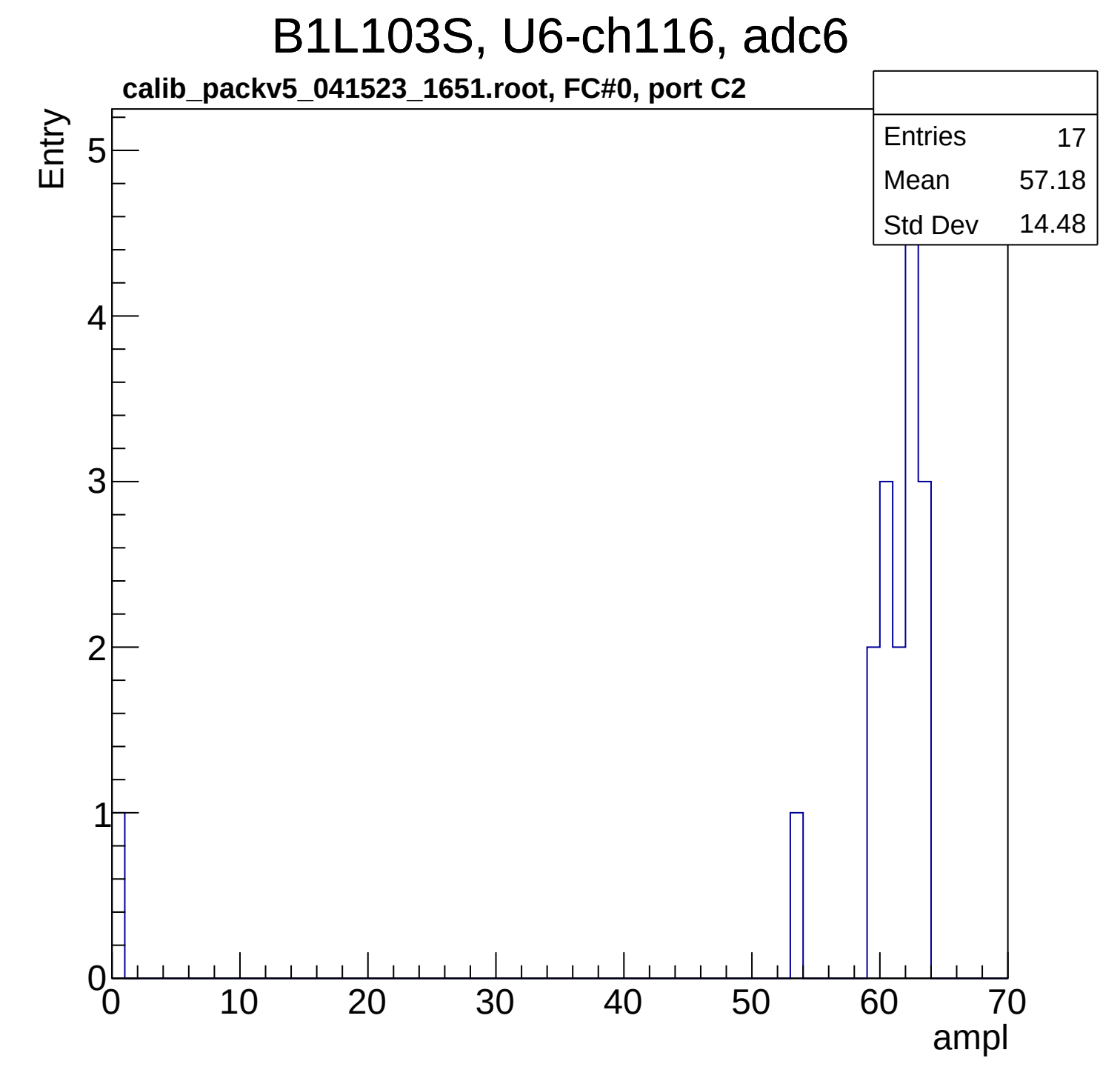
B1L103S, U6-ch116, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 57.18
Std Dev 14.48
Entry
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3
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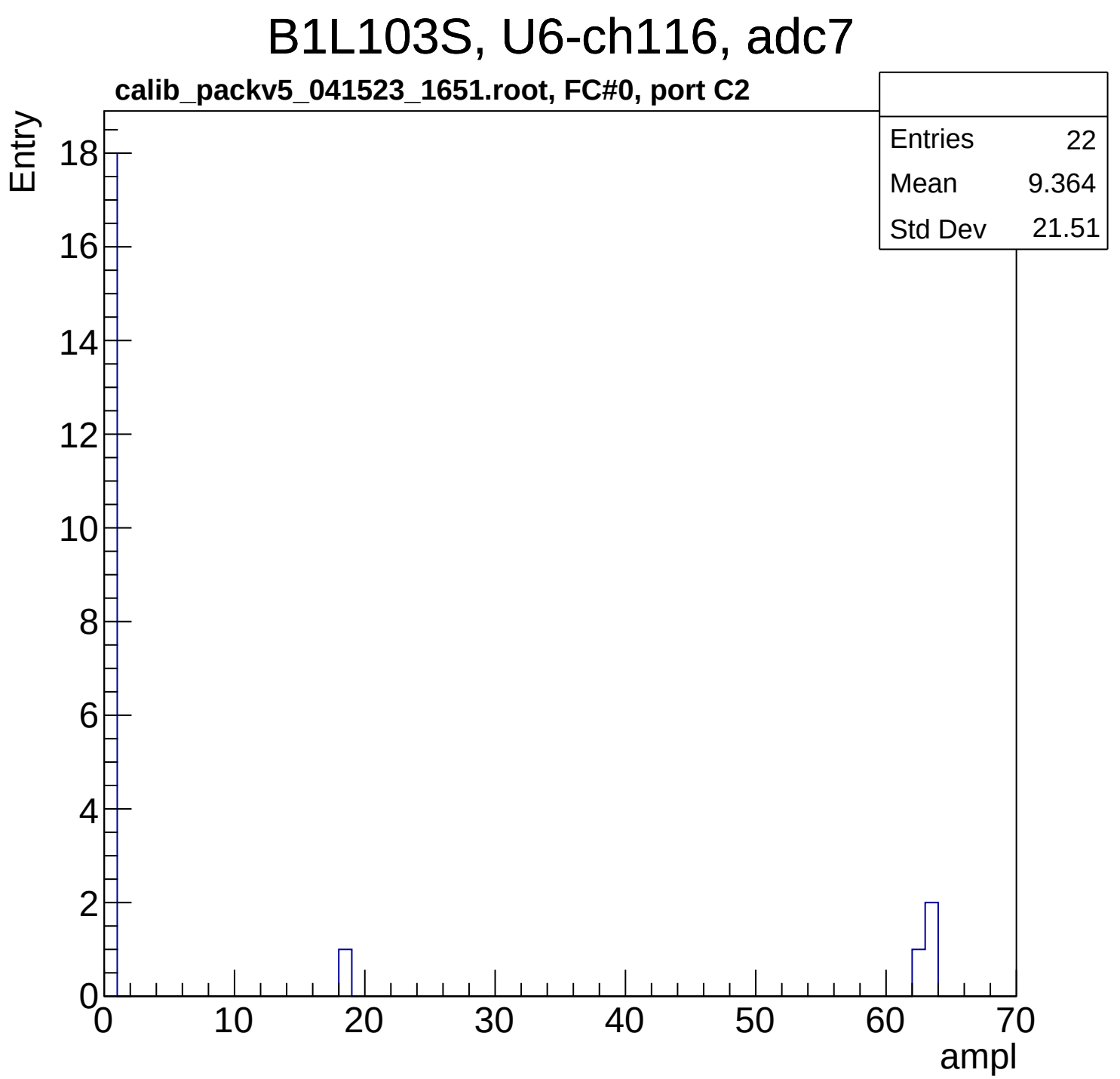
70
ampl


B1L103S, U6-ch116, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 9.364
Std Dev 21.51
Entry
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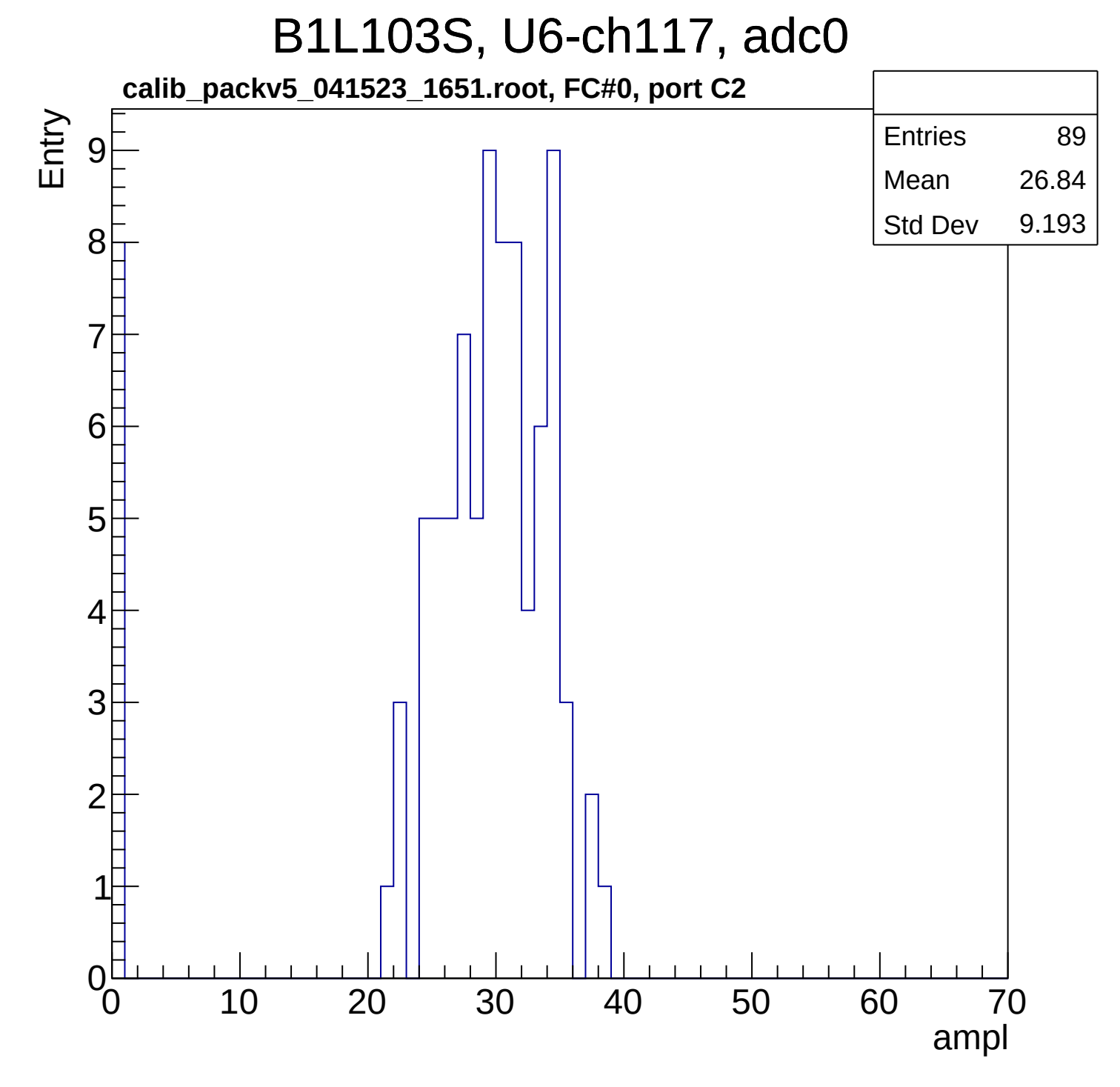
ampl


B1L103S, U6-ch117, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 26.84
Std Dev 9.193
Entry
ampl
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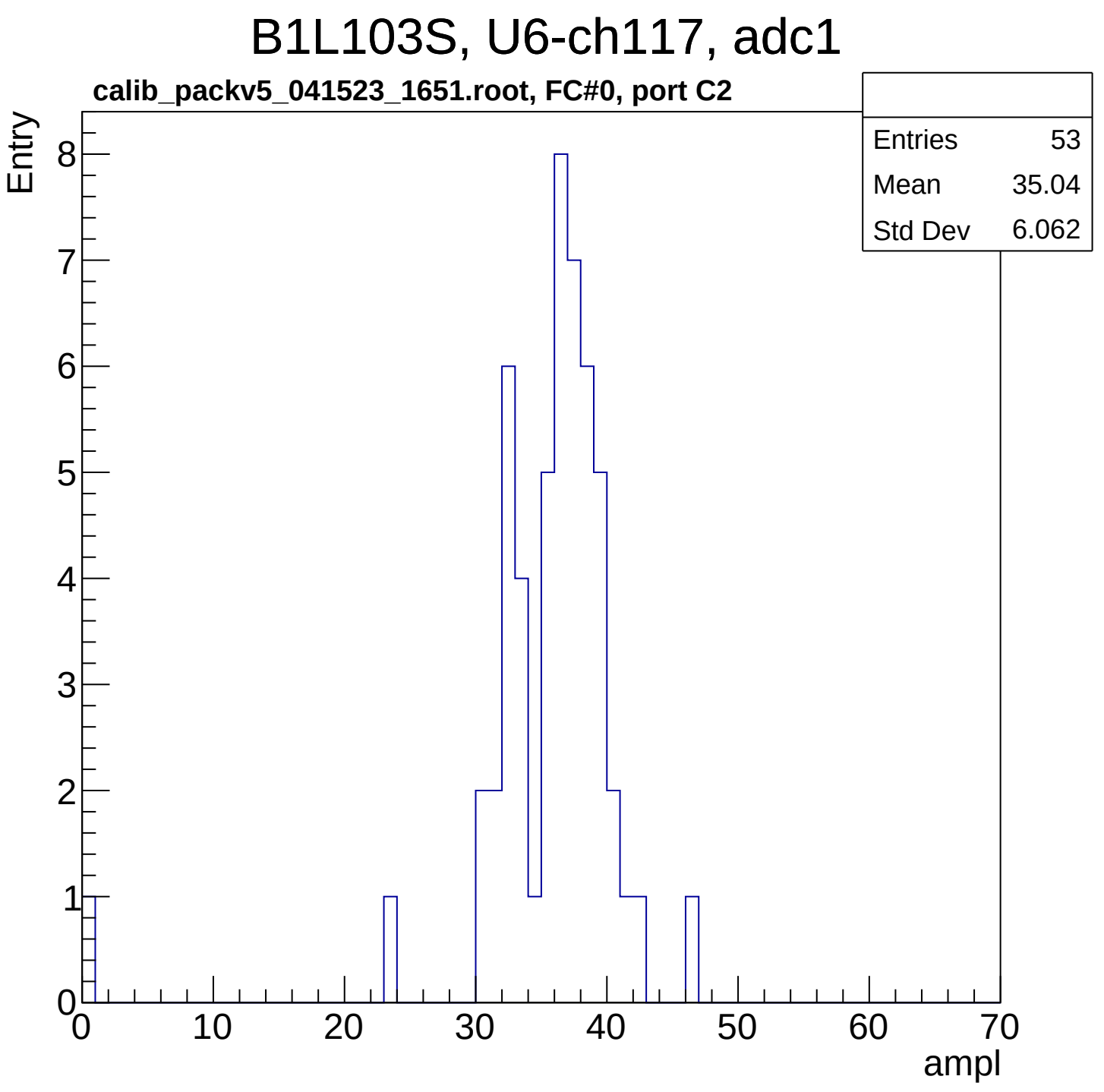
B1L103S, U6-ch117, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 35.04
Std Dev 6.062
Entry
ampl
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0
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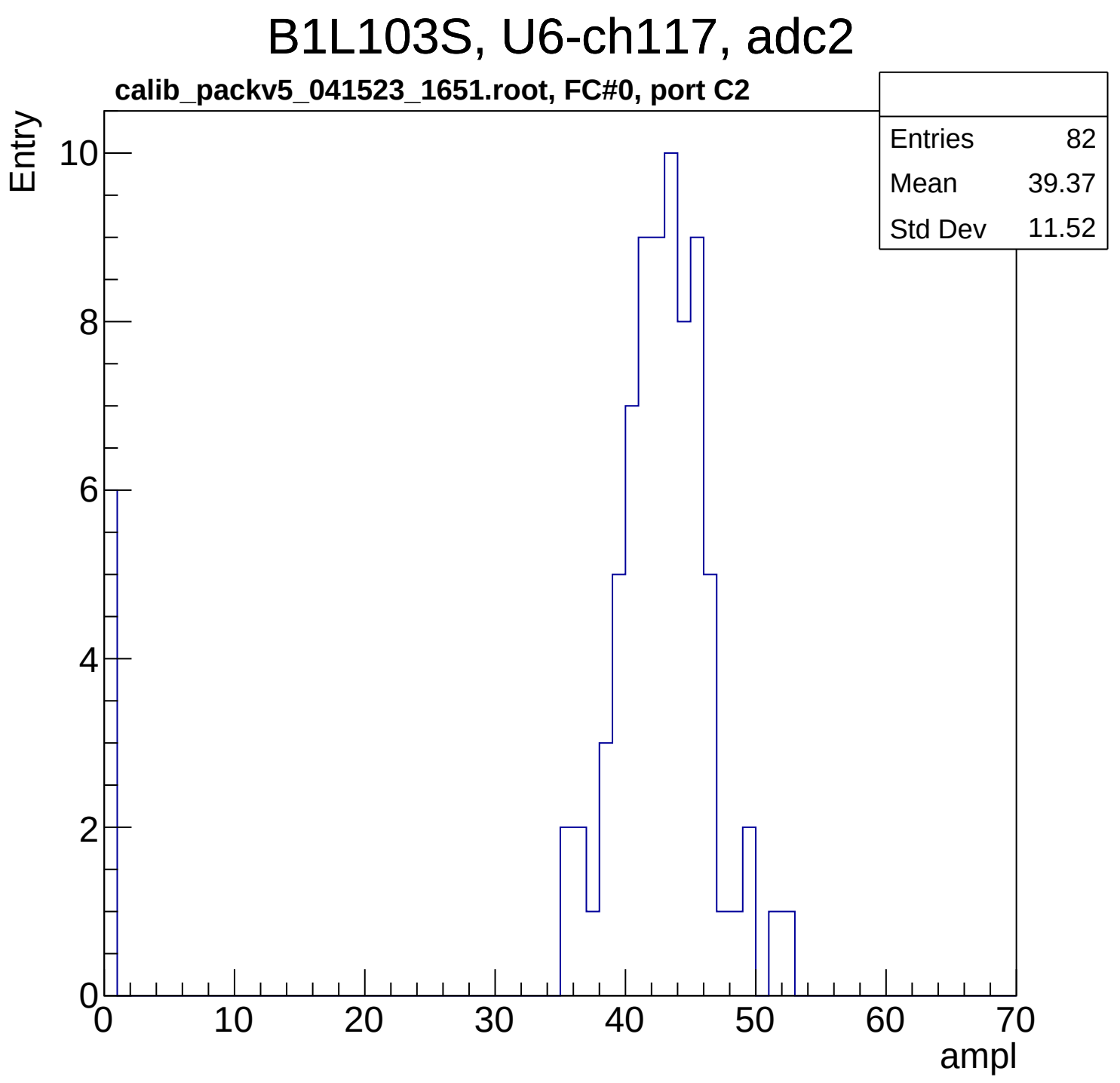
B1L103S, U6-ch117, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 39.37
Std Dev 11.52
Entry
0
2
4
6
8
10
0
10
20
30
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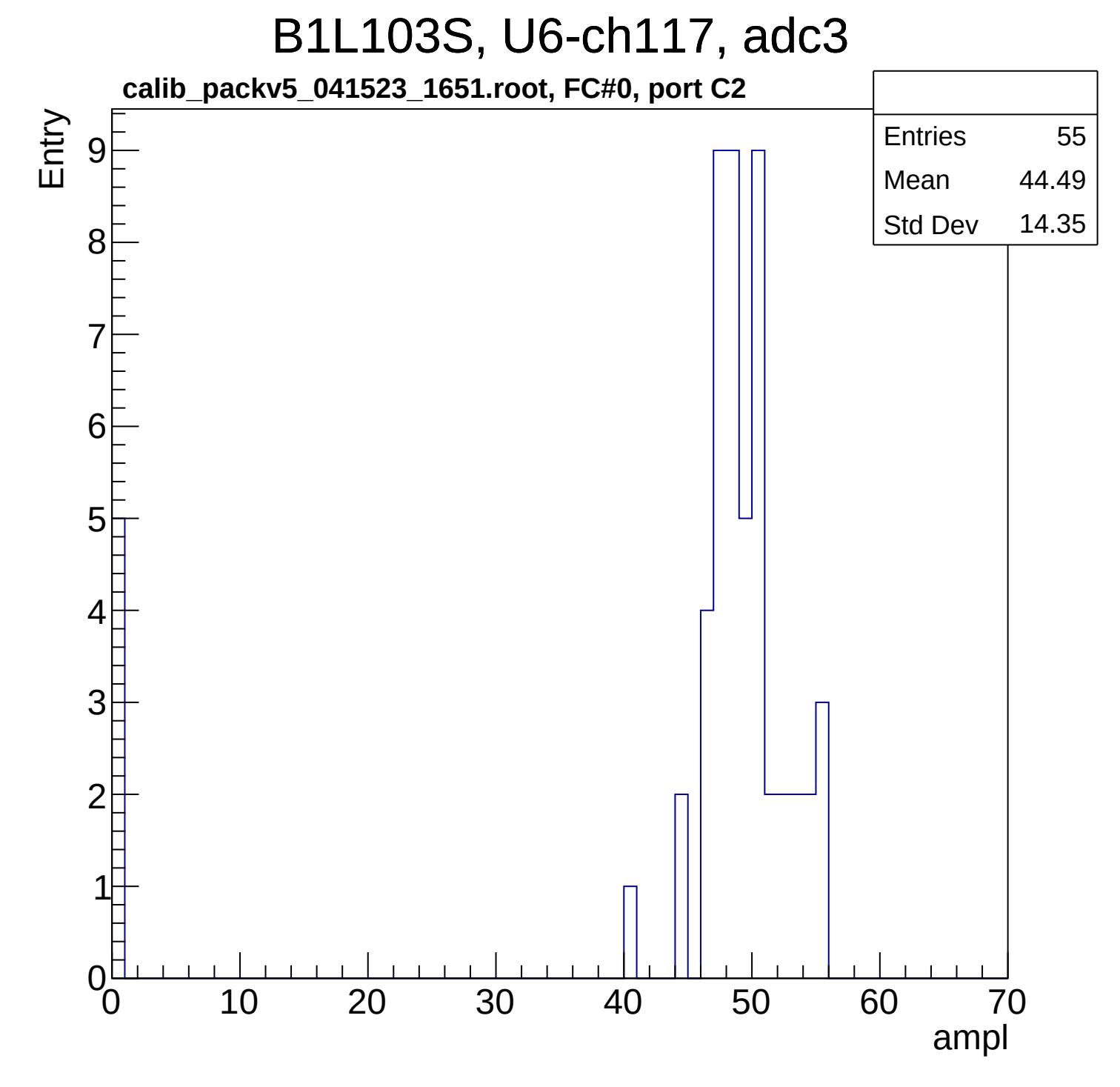
50
60
70
ampl


B1L103S, U6-ch117, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 44.49
Std Dev 14.35
Entry
ampl
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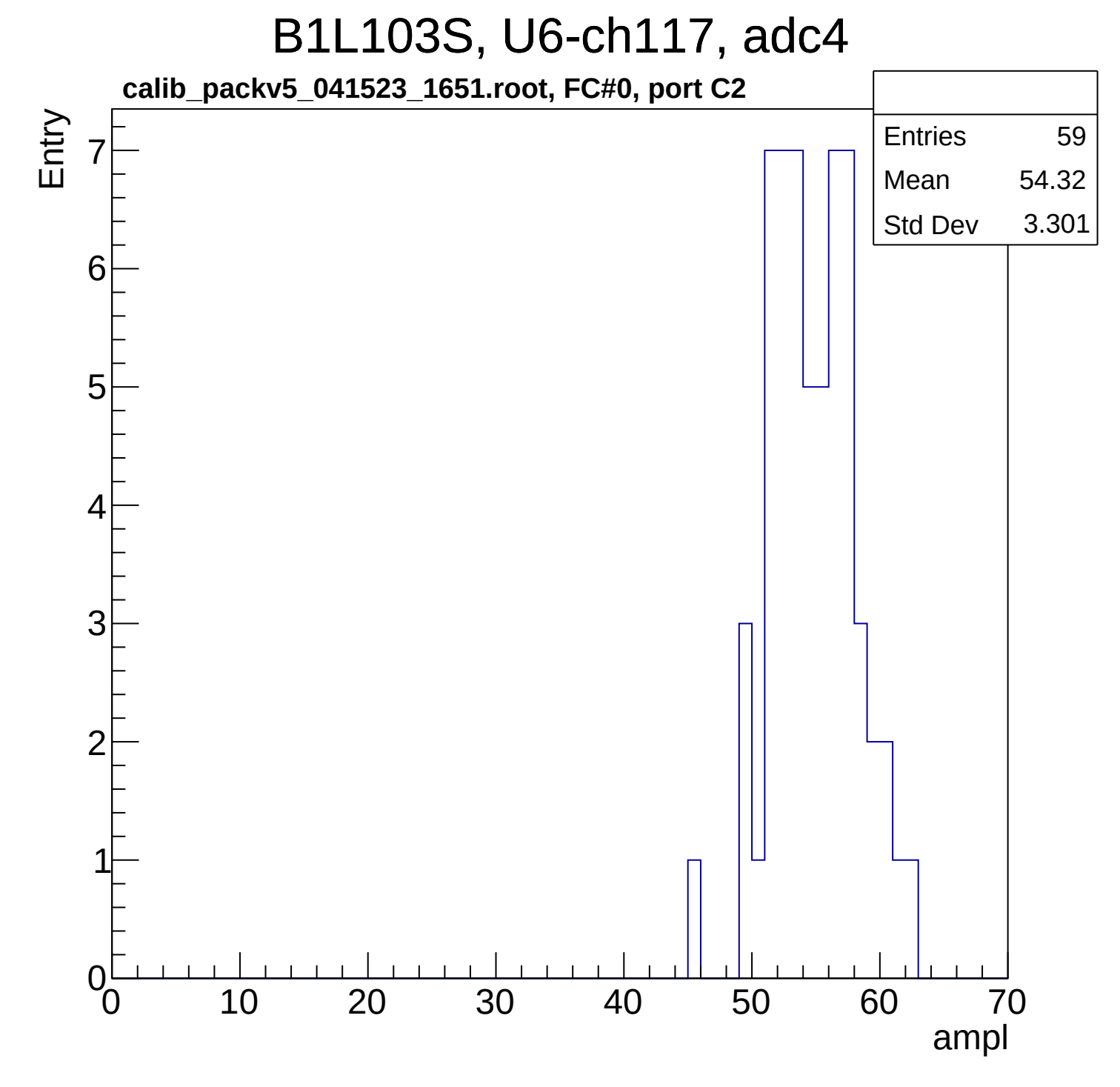
B1L103S, U6-ch117, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 54.32
Std Dev 3.301
Entry
ampl
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2
3
4
5
6
7
0
10
20
30
40
50
60
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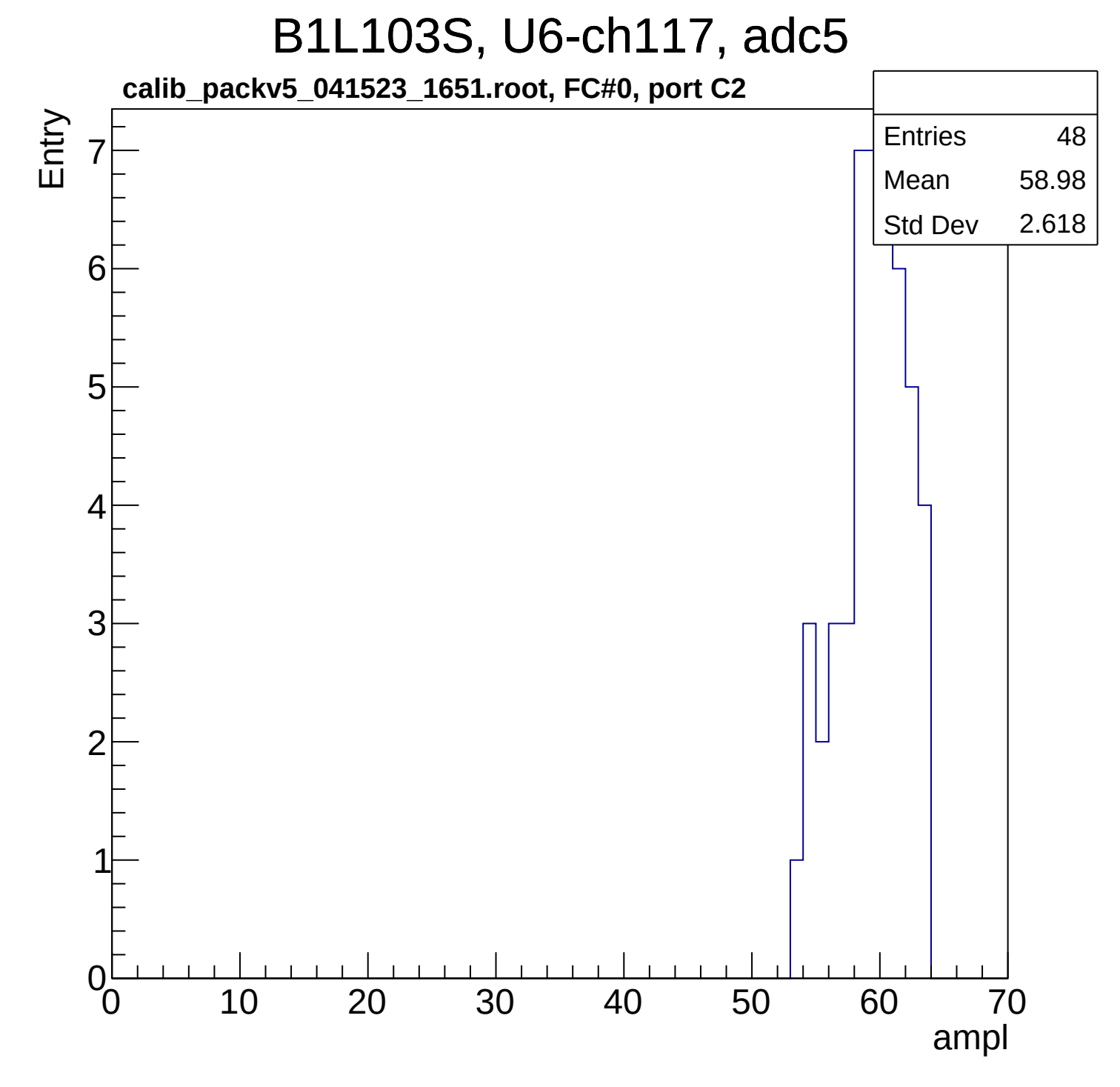
B1L103S, U6-ch117, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 58.98
Std Dev 2.618
Entry
ampl
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2
3
4
5
6
7
0
10
20
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40
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60
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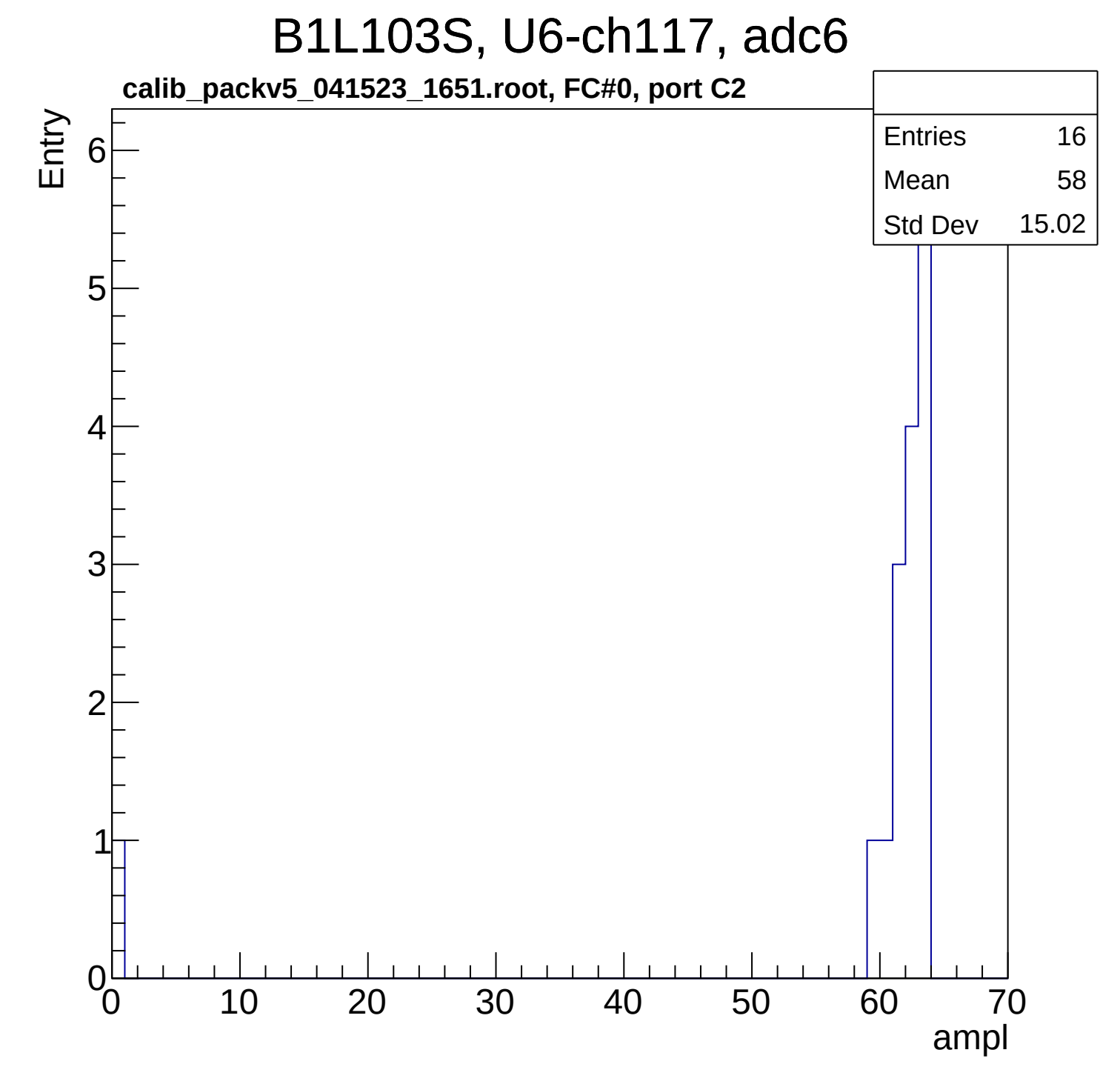
B1L103S, U6-ch117, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 58
Std Dev 15.02
Entry
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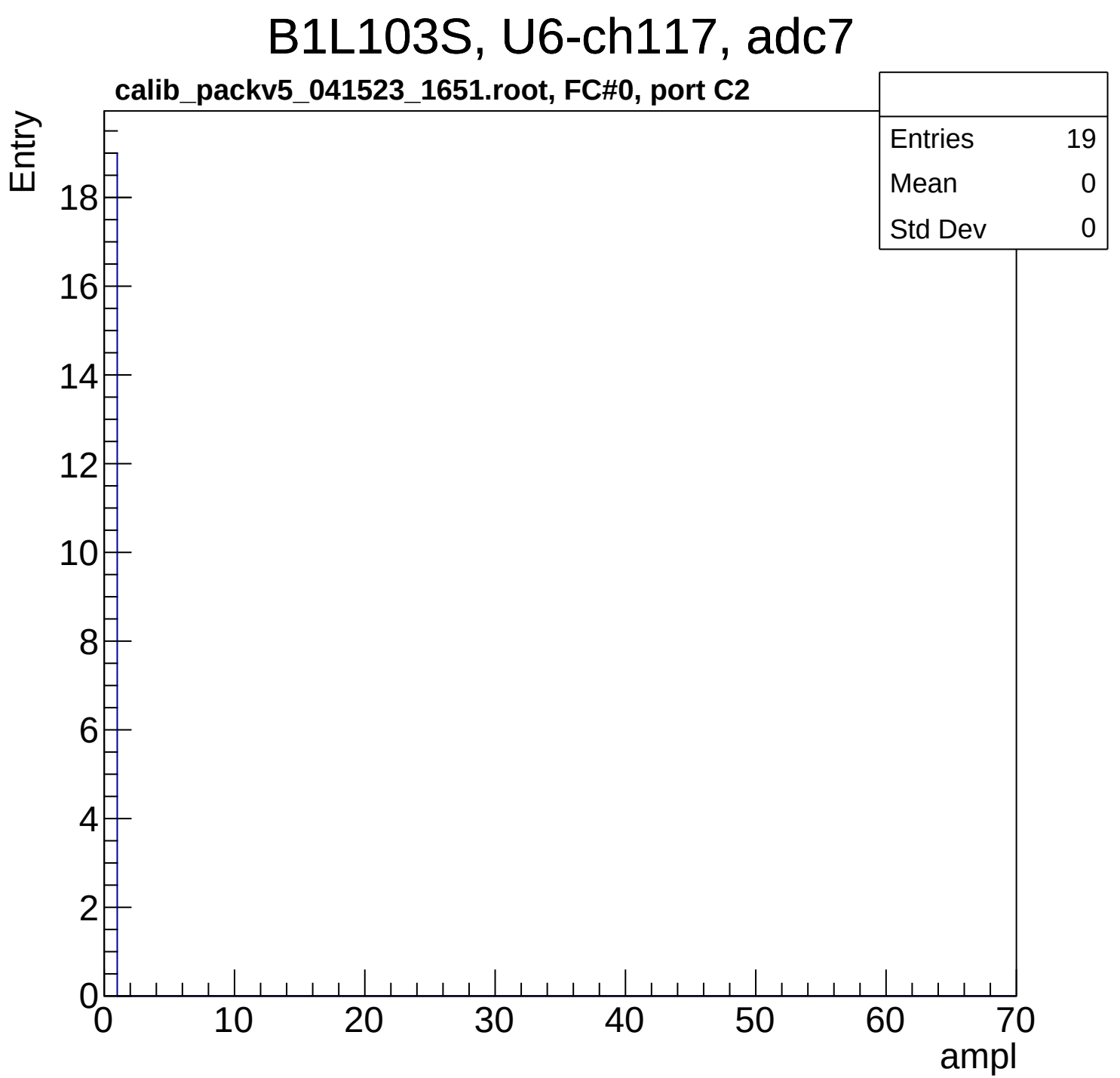
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch117, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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6
8
10
12
14
16
18
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10
20
30
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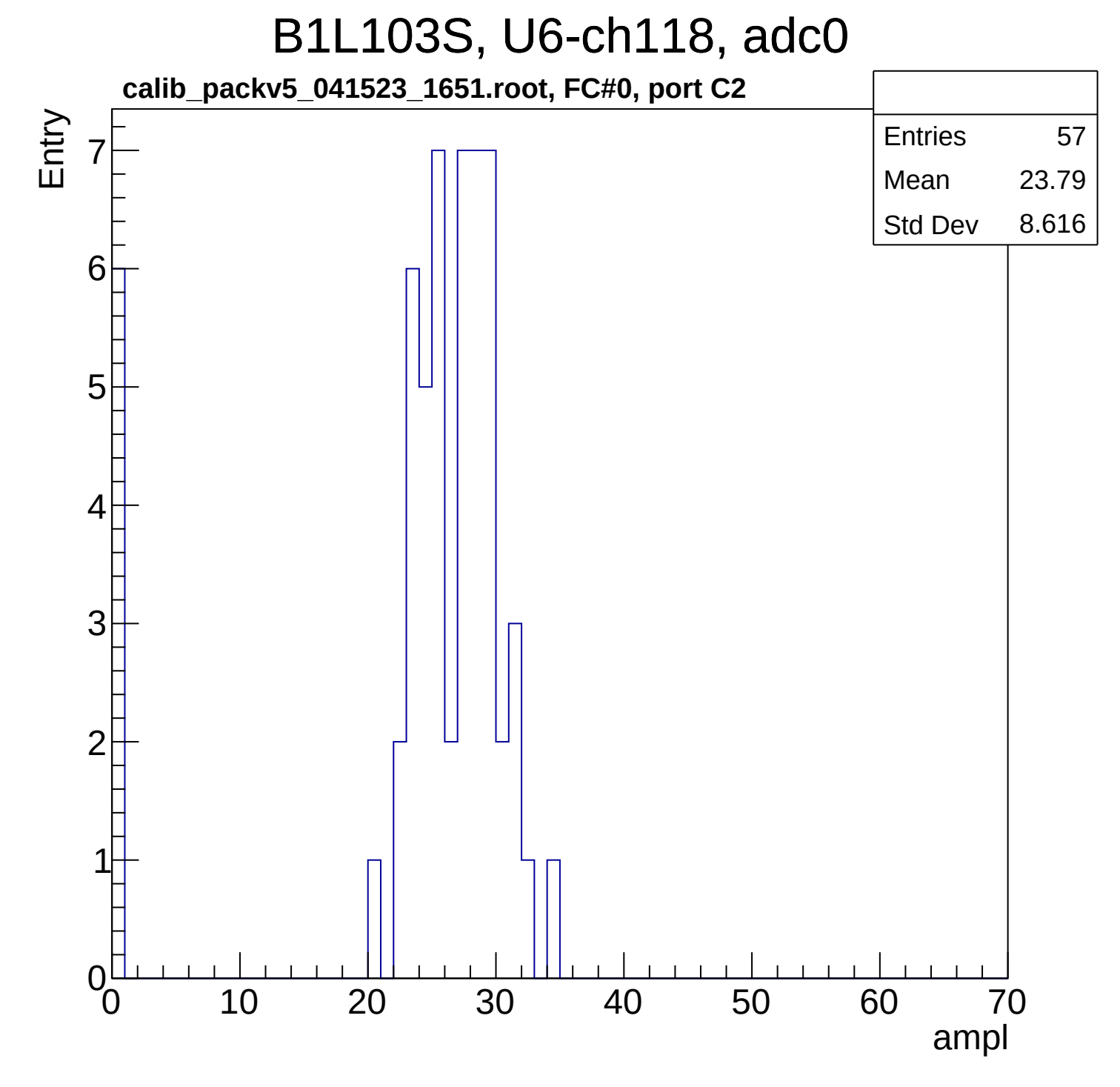
50
60
70
ampl


B1L103S, U6-ch118, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 23.79
Std Dev 8.616
Entry
ampl
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2
3
4
5
6
7
0
10
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40
50
60
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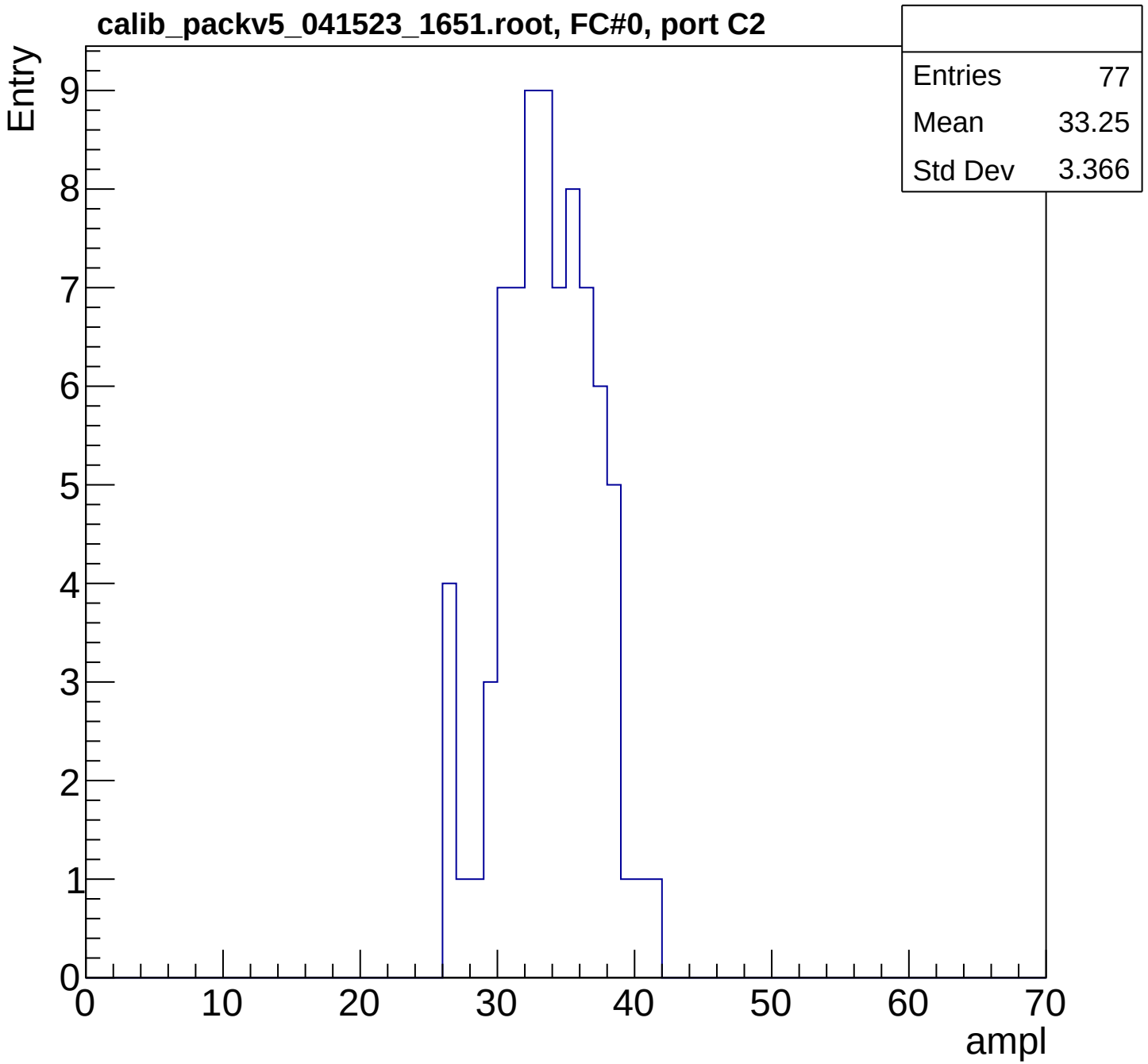
B1L103S, U6-ch118, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 33.25
Std Dev 3.366
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
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60
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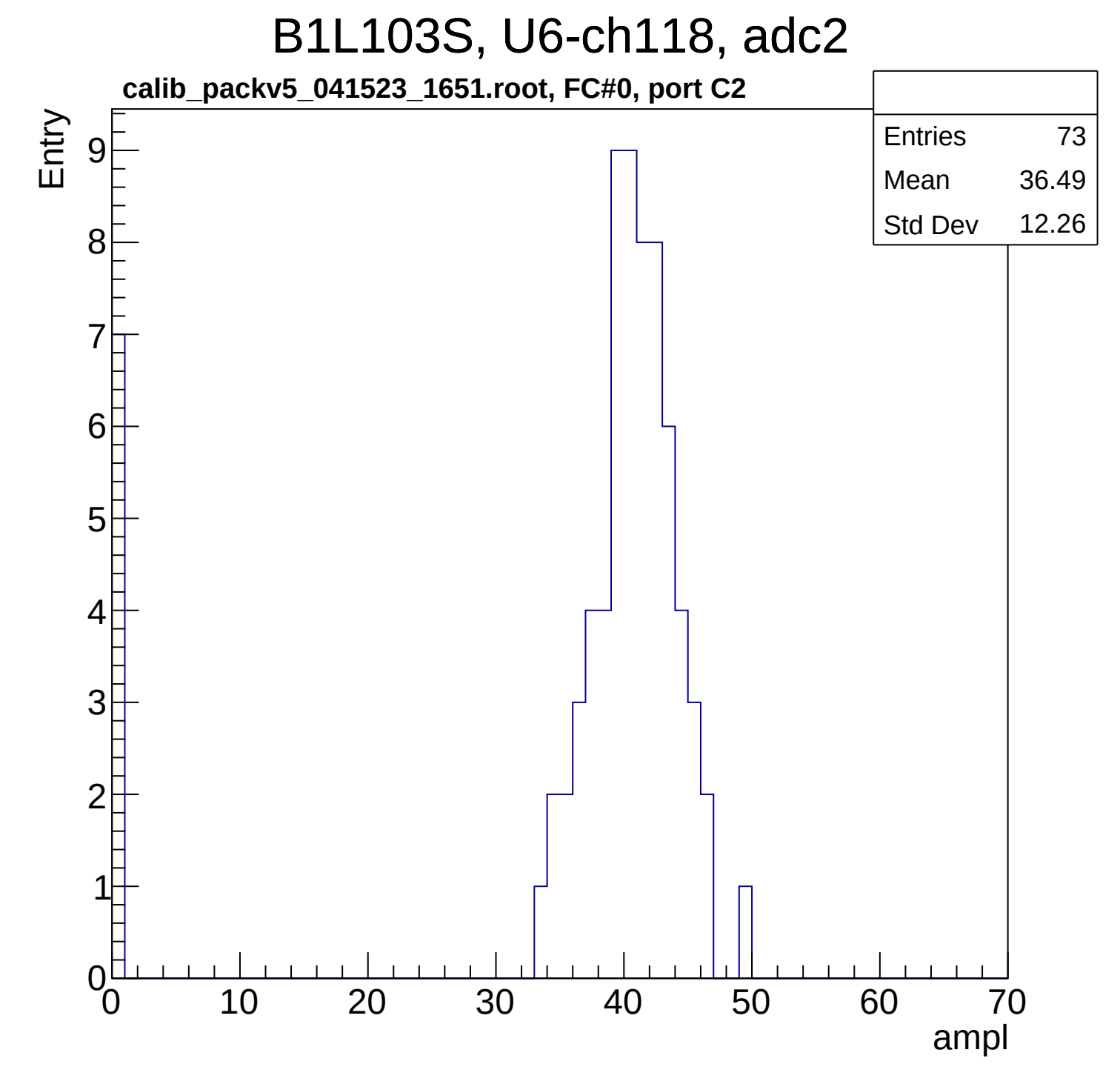
B1L103S, U6-ch118, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 36.49
Std Dev 12.26
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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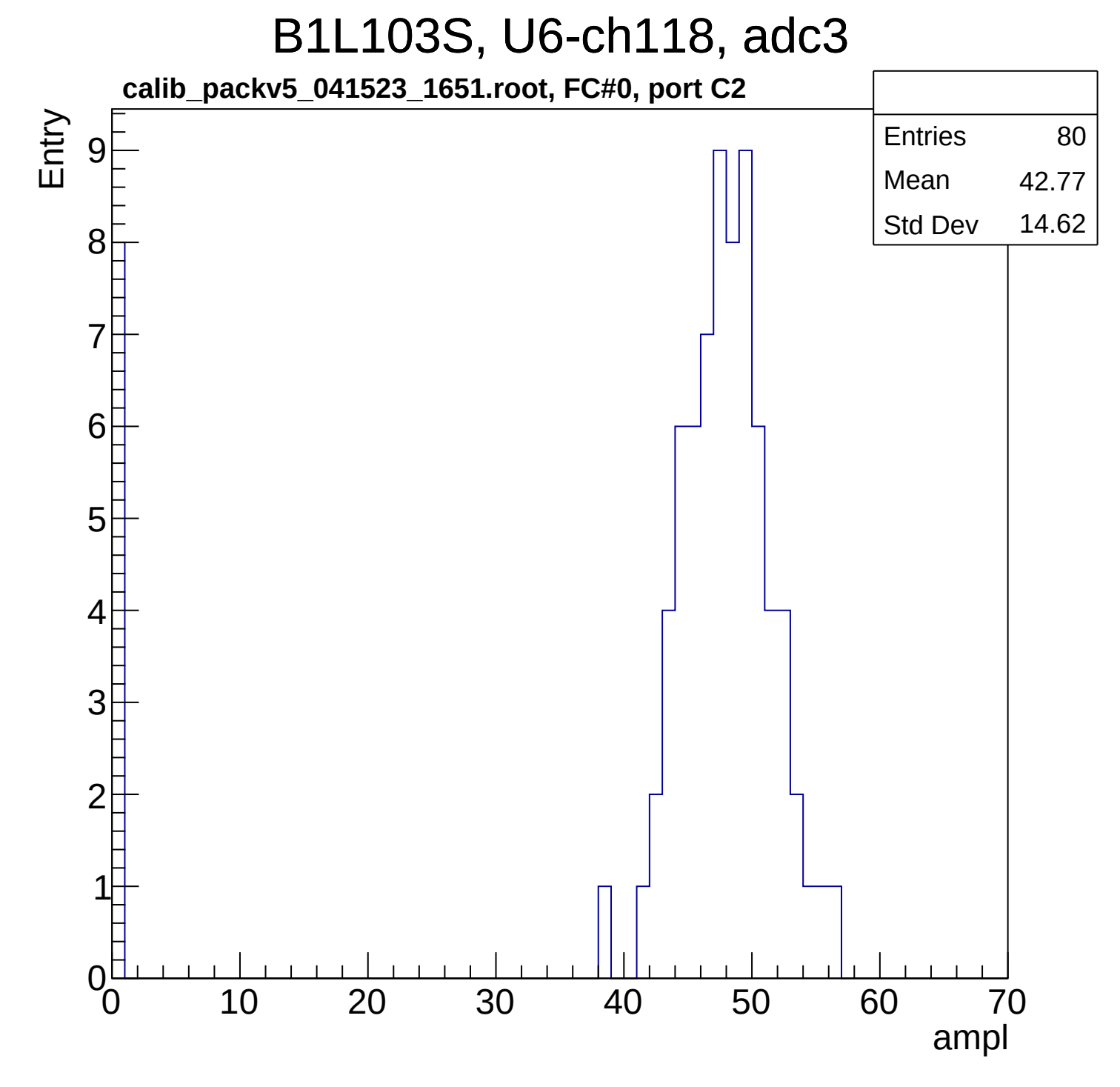
B1L103S, U6-ch118, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 42.77
Std Dev 14.62
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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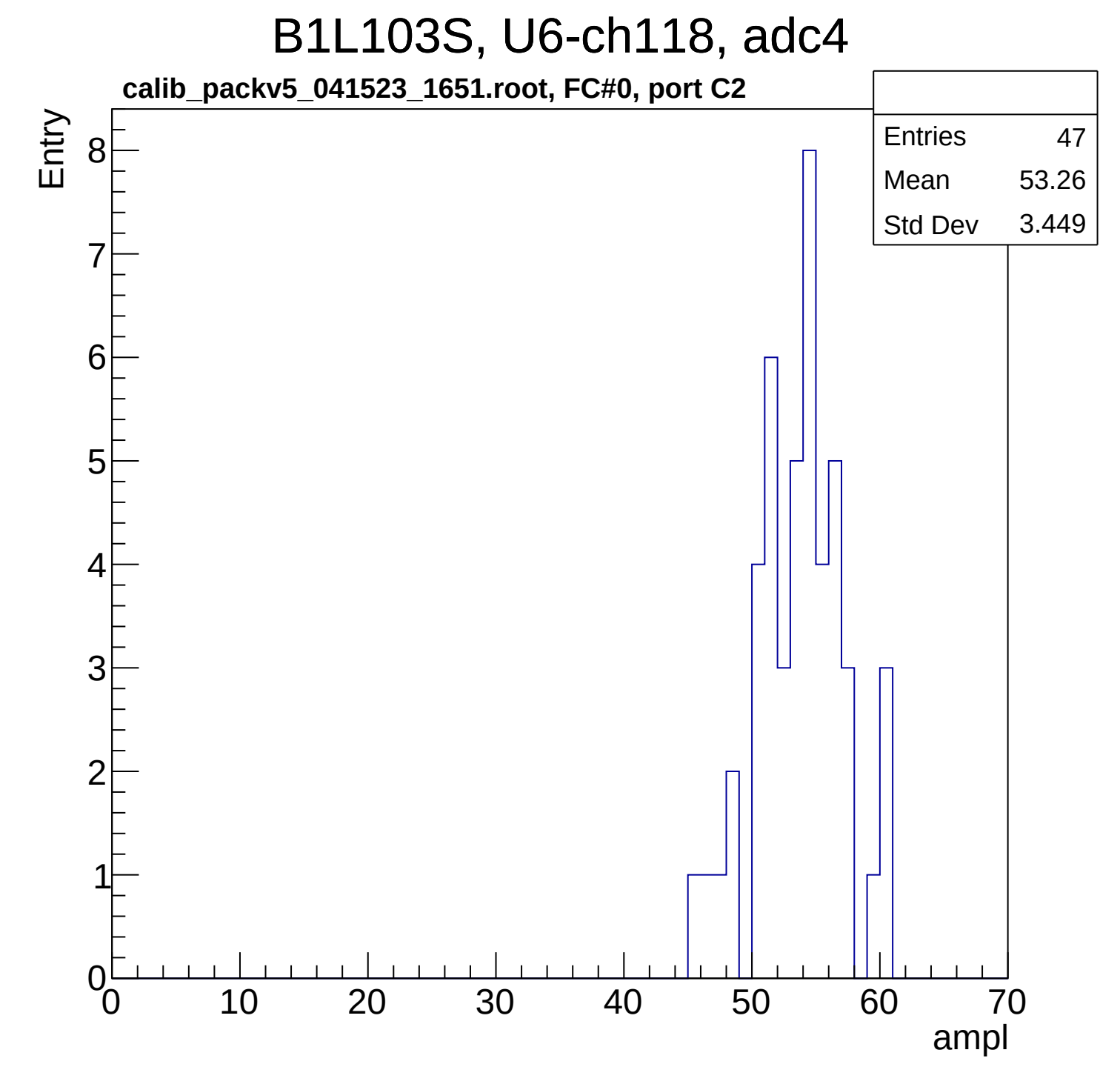
B1L103S, U6-ch118, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 53.26
Std Dev 3.449
Entry
ampl
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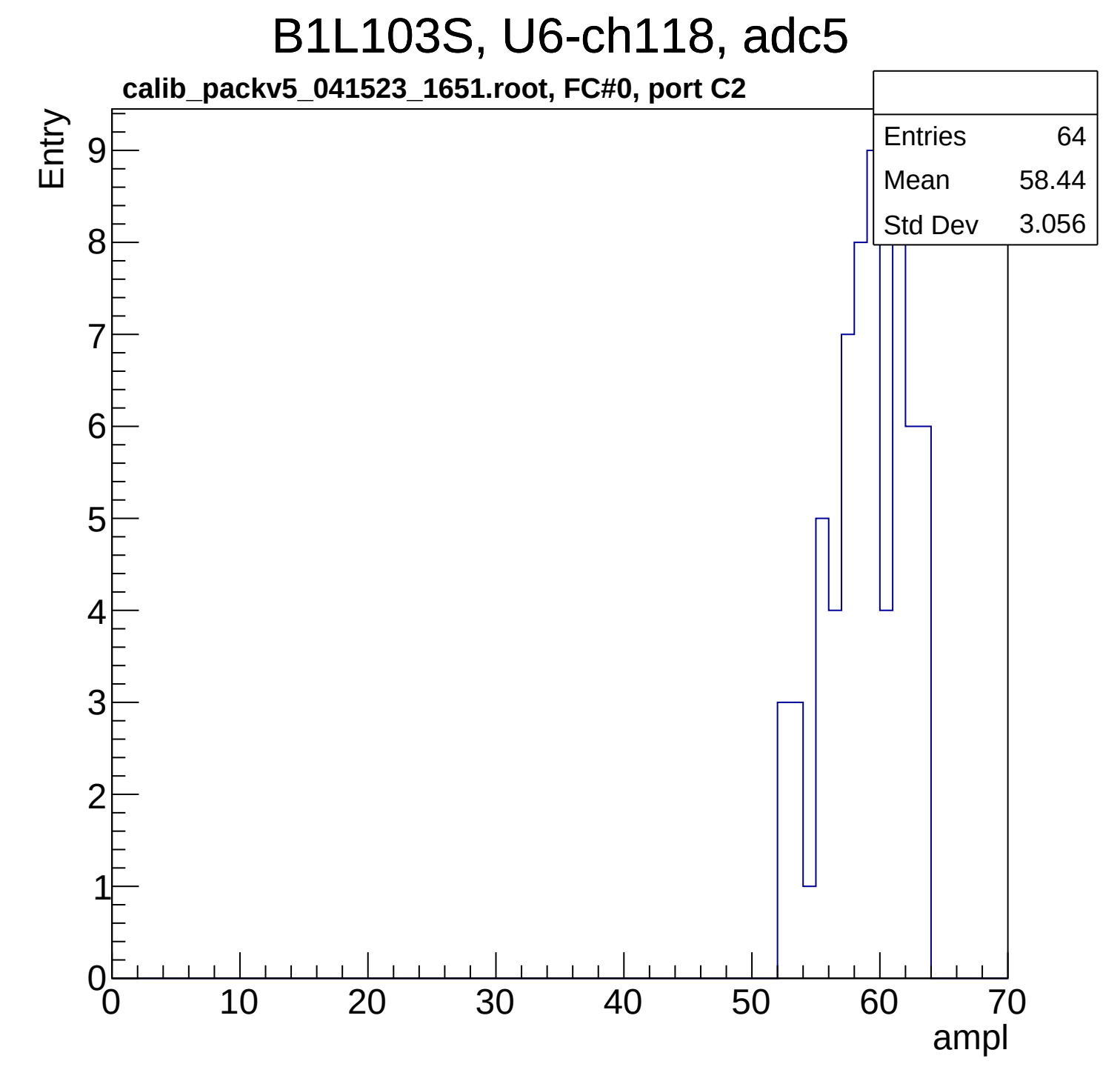
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch118, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 58.44
Std Dev 3.056
Entry
ampl
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4
5
6
7
8
9
0
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60
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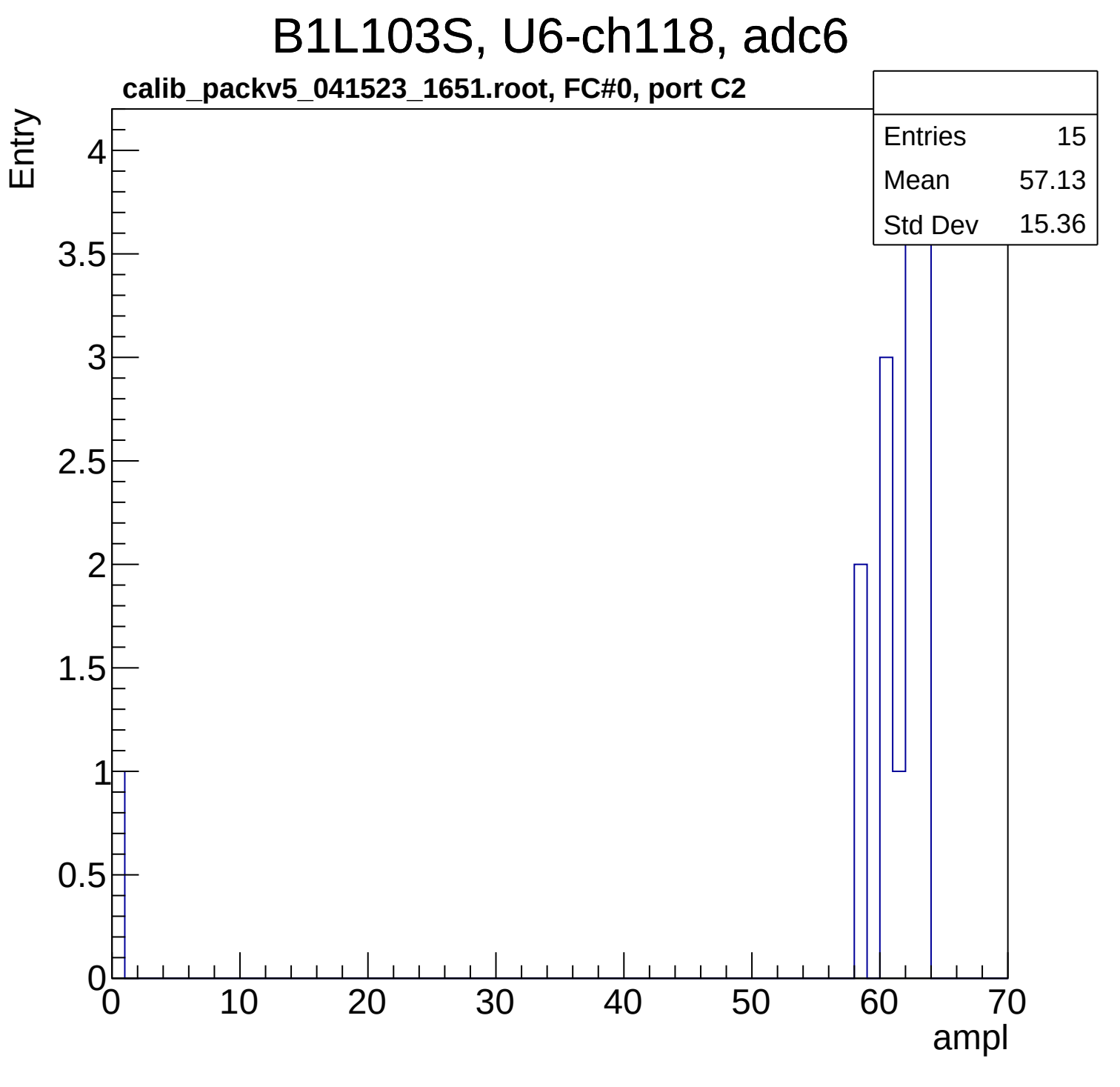
B1L103S, U6-ch118, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 57.13
Std Dev 15.36
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
10
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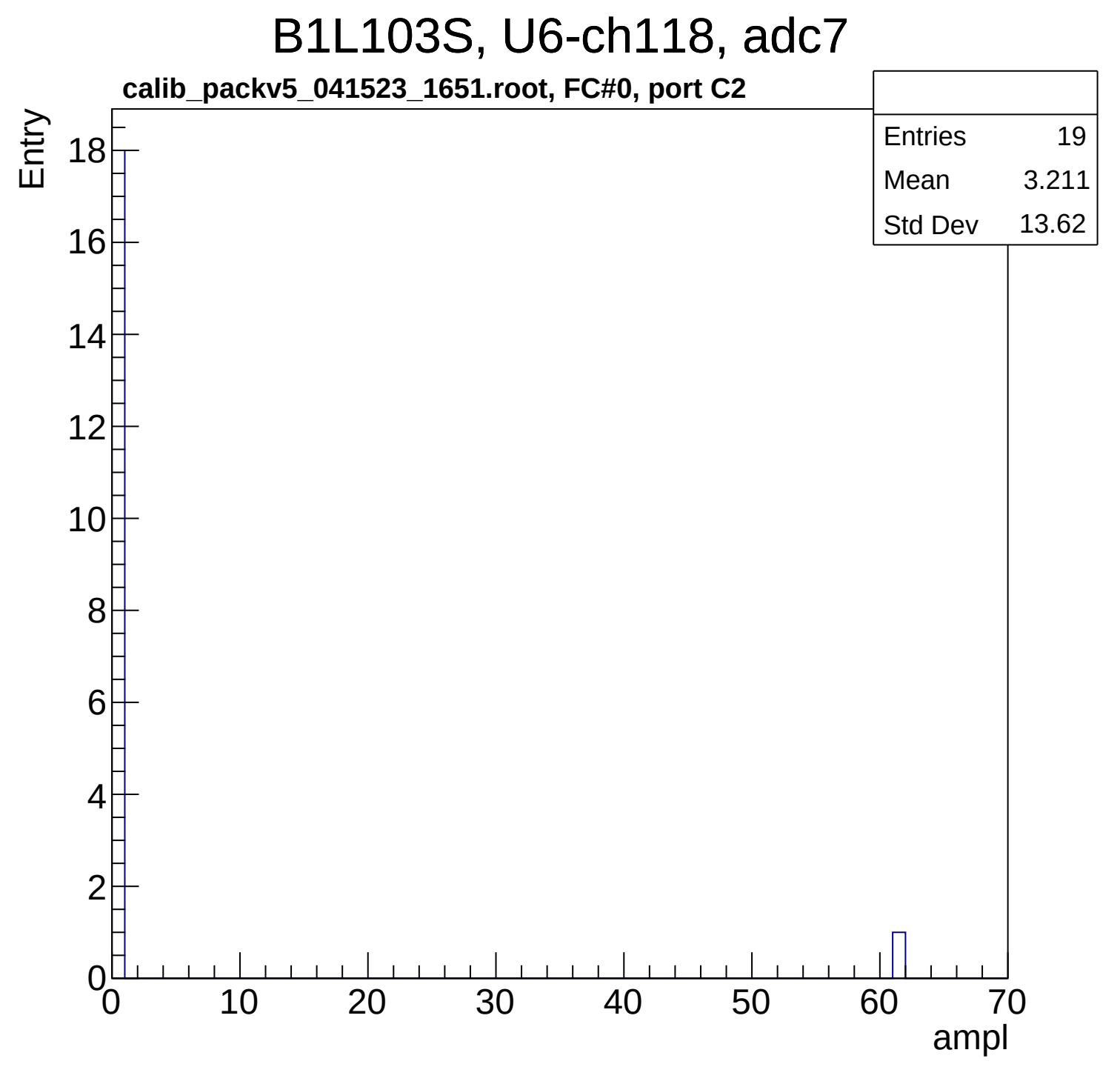
40
50
60
70


B1L103S, U6-ch118, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.211
Std Dev 13.62
Entry
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6
8
10
12
14
16
18
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10
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30
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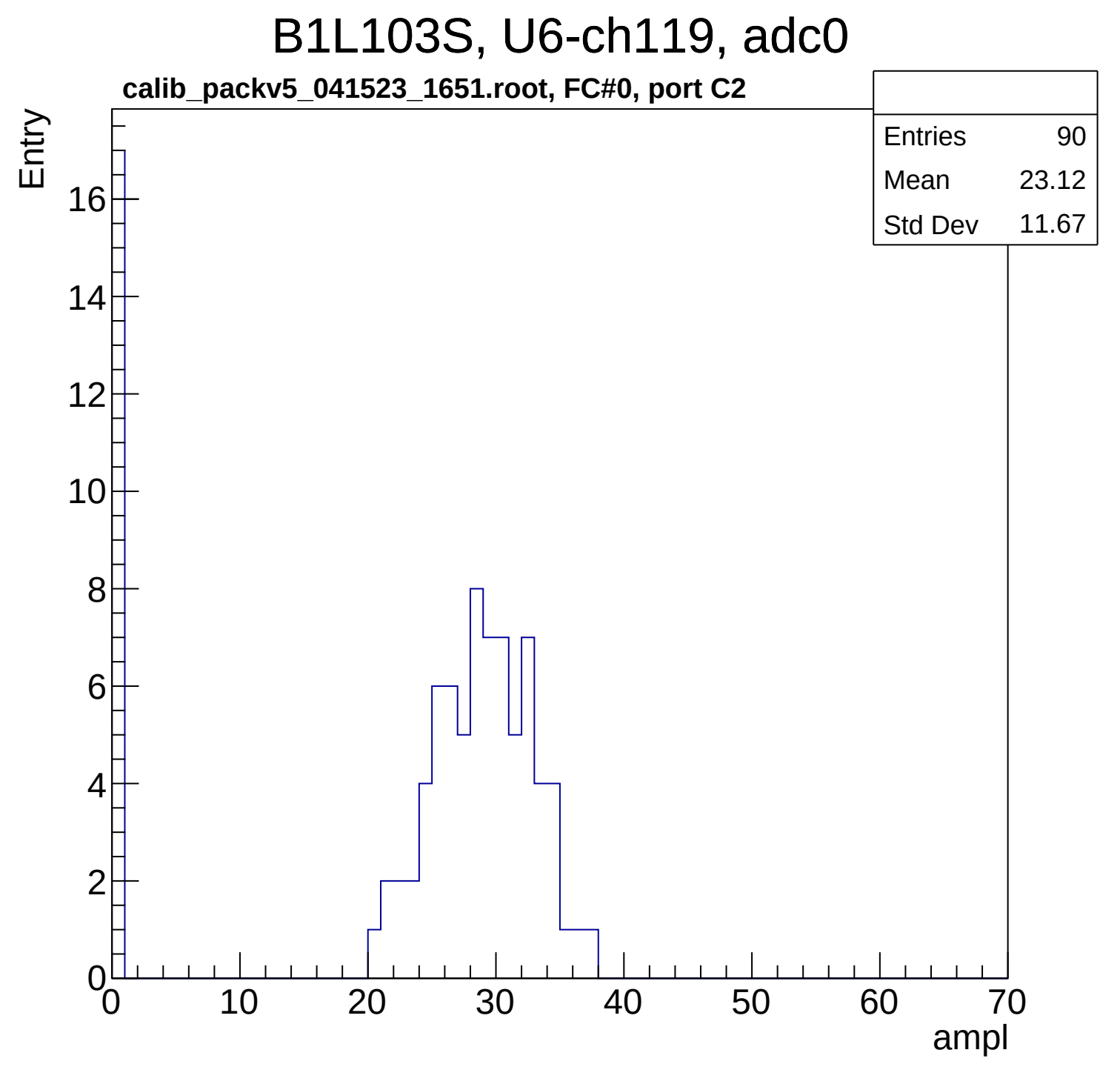
60
70
ampl


B1L103S, U6-ch119, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 23.12
Std Dev 11.67
Entry
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4
6
8
10
12
14
16
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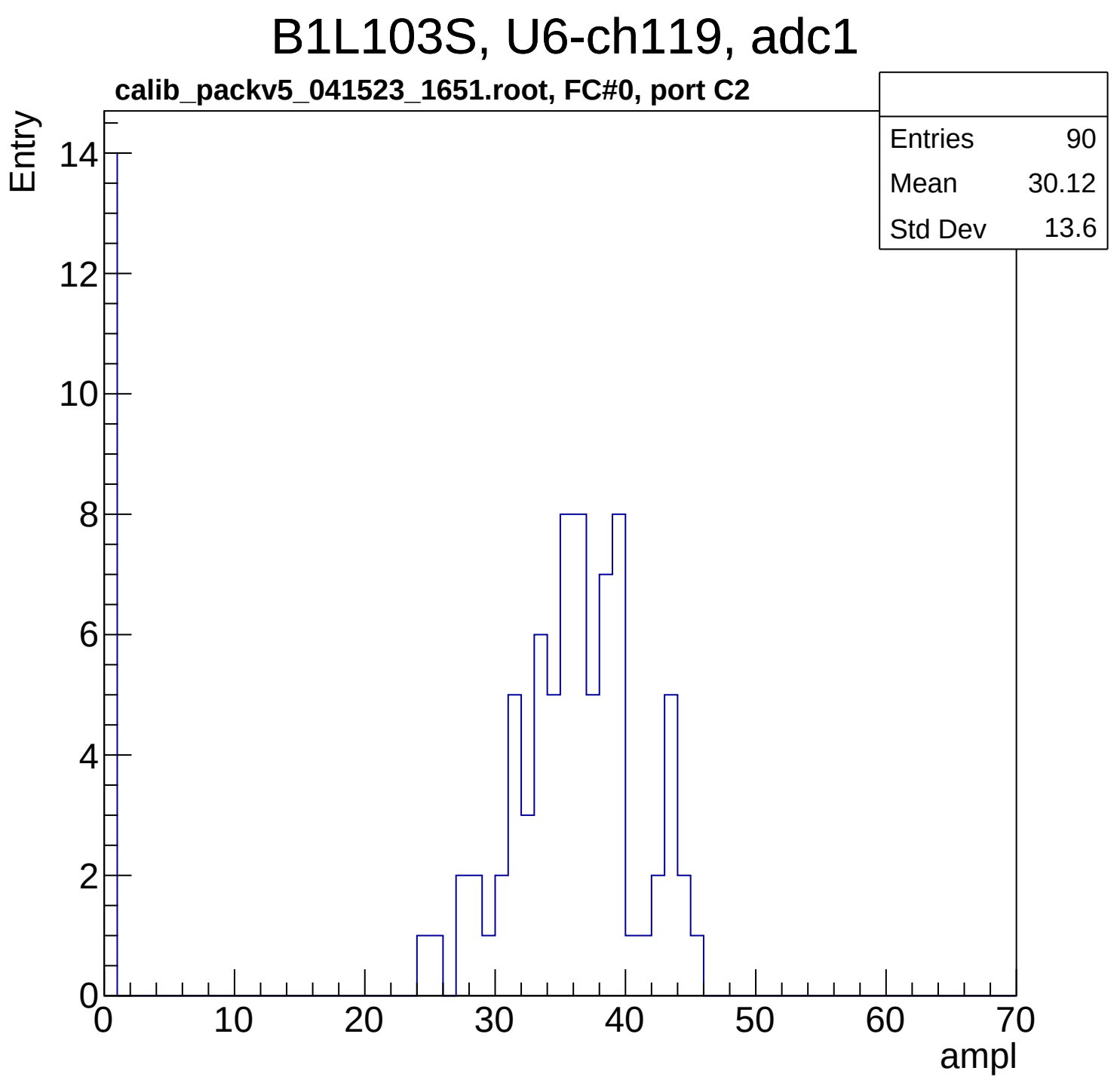
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch119, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 30.12
Std Dev 13.6
Entry
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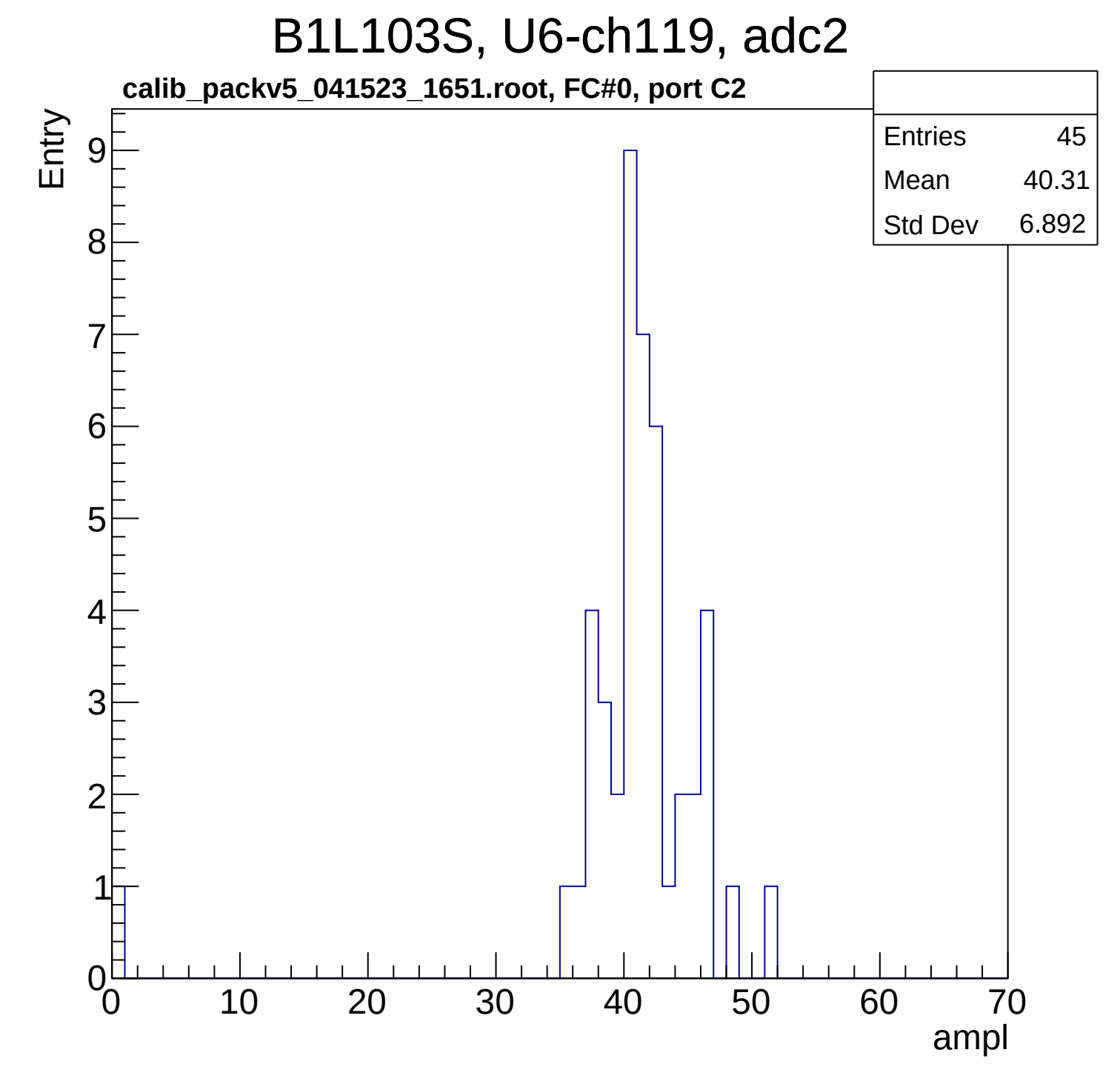
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch119, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 40.31
Std Dev 6.892
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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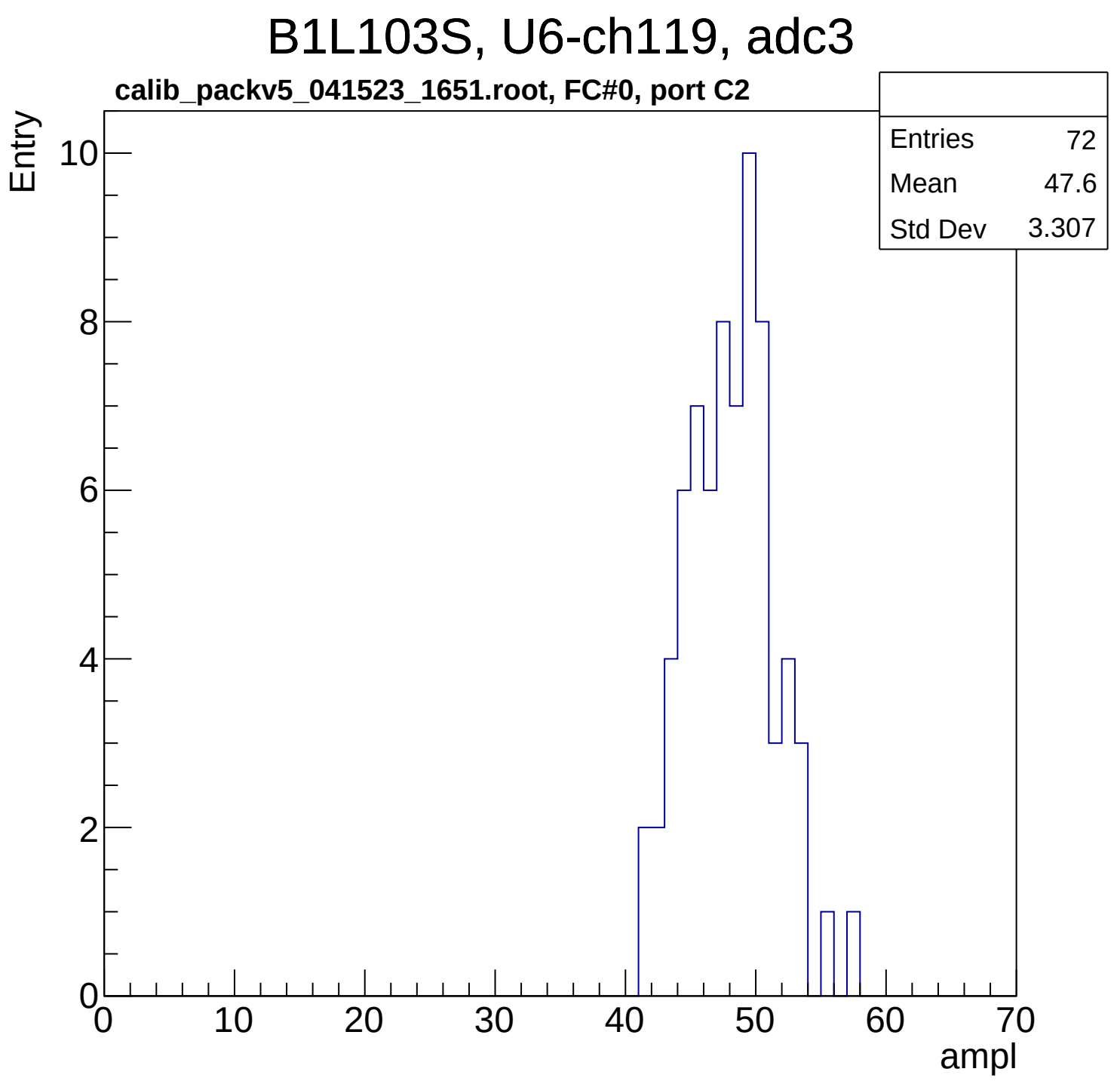
40
50
60
70


B1L103S, U6-ch119, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 47.6
Std Dev 3.307
Entry
ampl
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6
8
10
0
10
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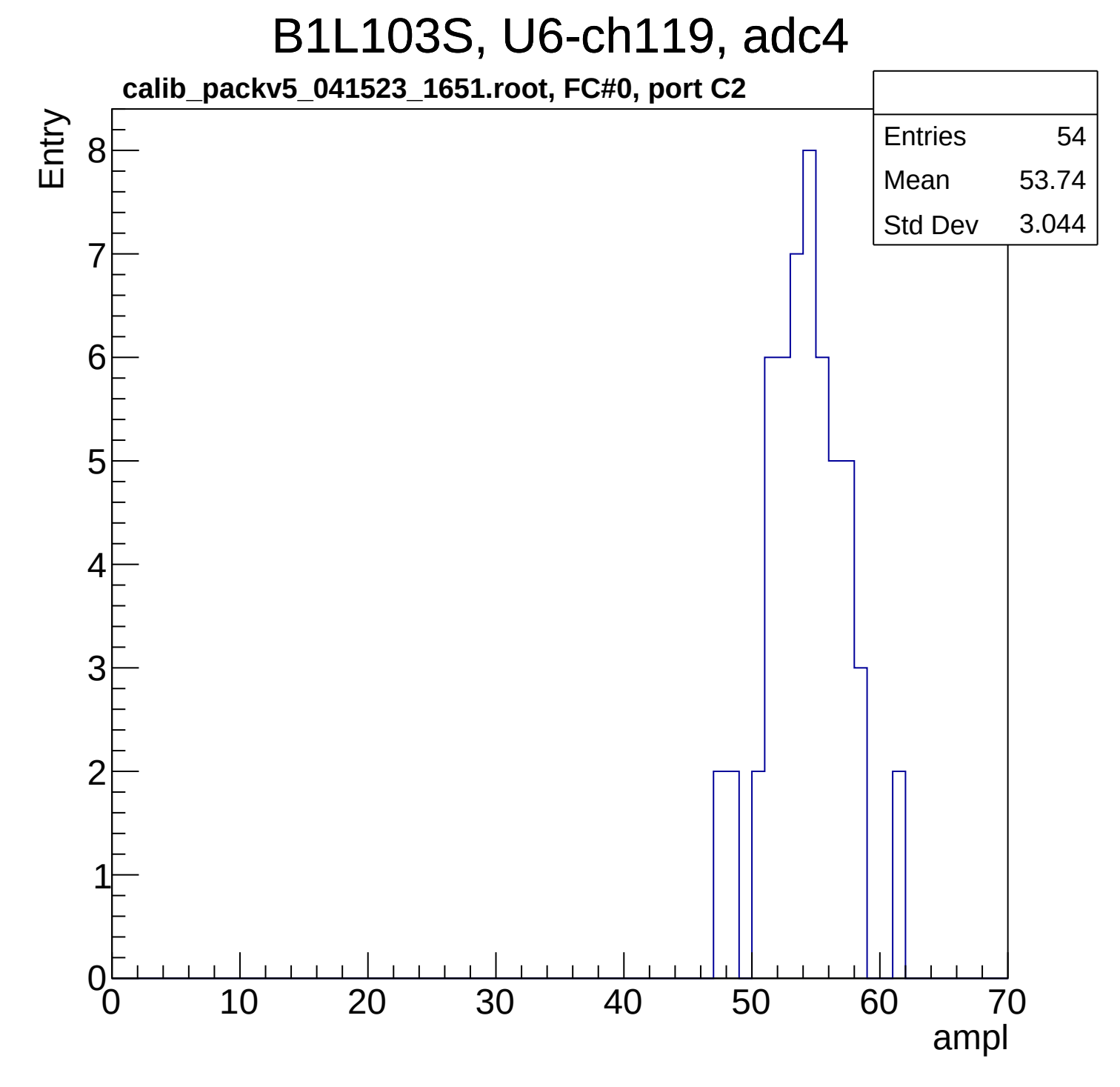
50
60
70


B1L103S, U6-ch119, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 53.74
Std Dev 3.044
Entry
ampl
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2
3
4
5
6
7
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0
10
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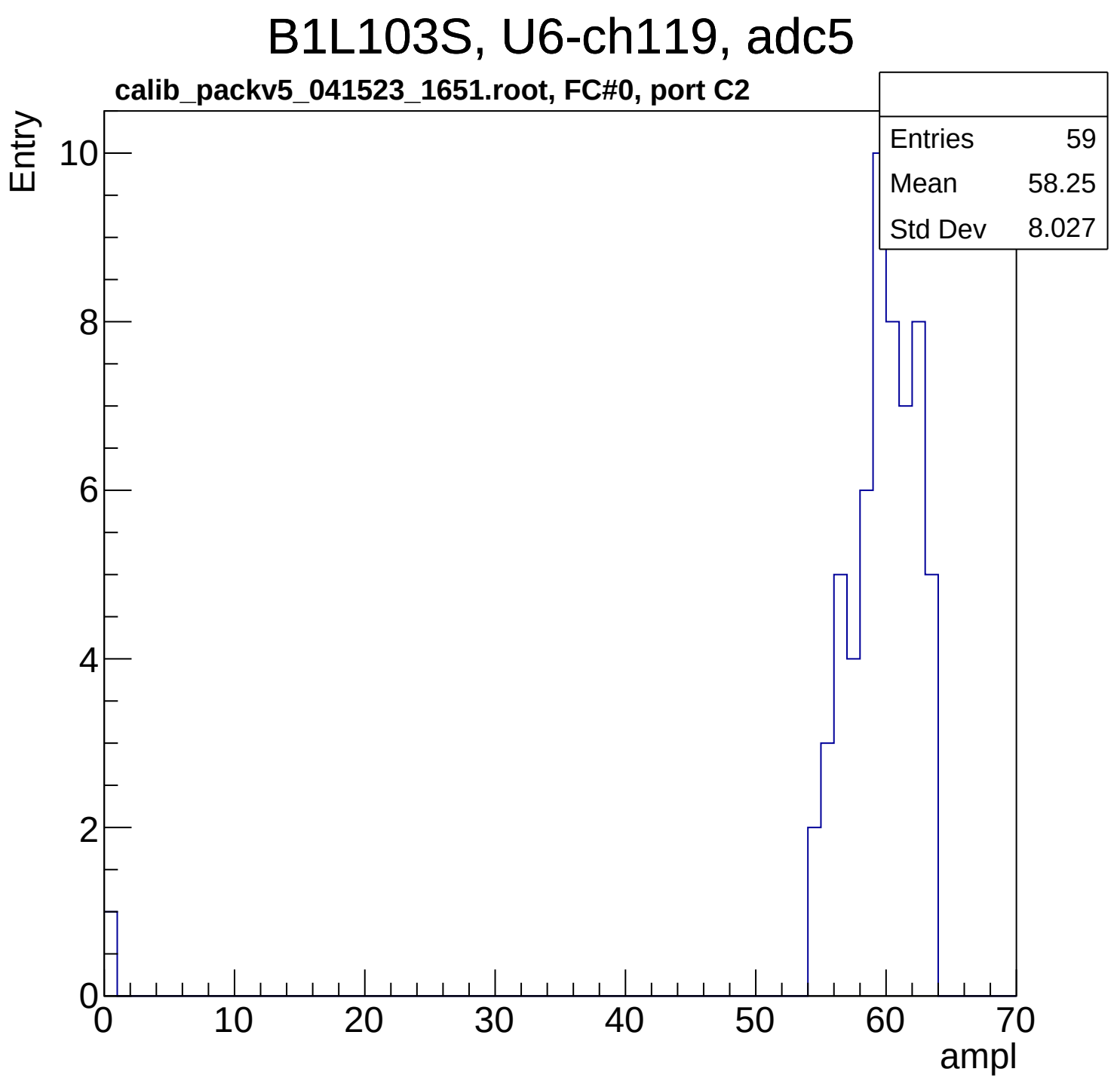
60
70


B1L103S, U6-ch119, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 58.25
Std Dev 8.027
Entry
ampl
0
2
4
6
8
10
0
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20
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60
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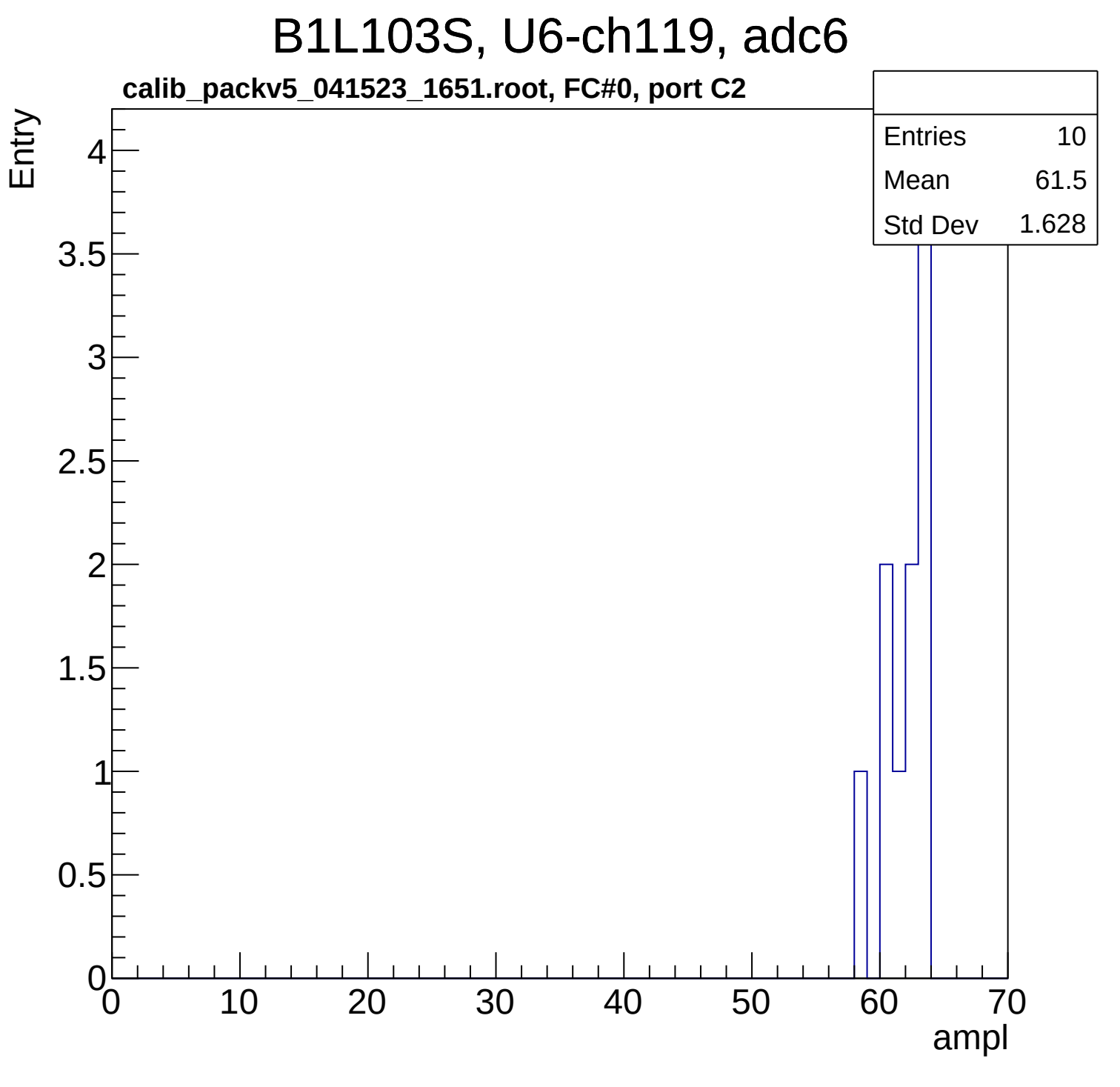
B1L103S, U6-ch119, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61.5
Std Dev 1.628
Entry
ampl
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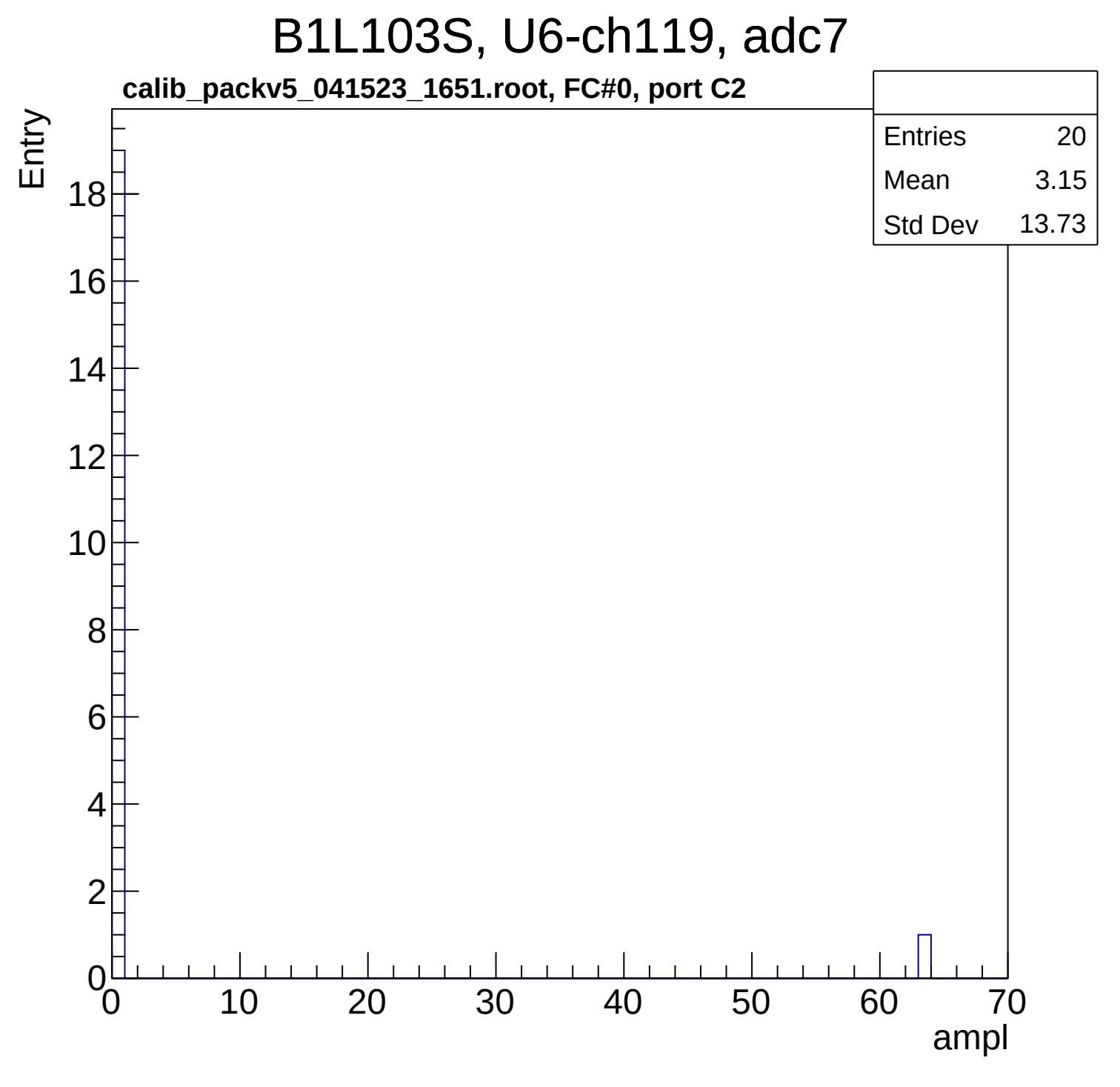
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U6-ch119, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
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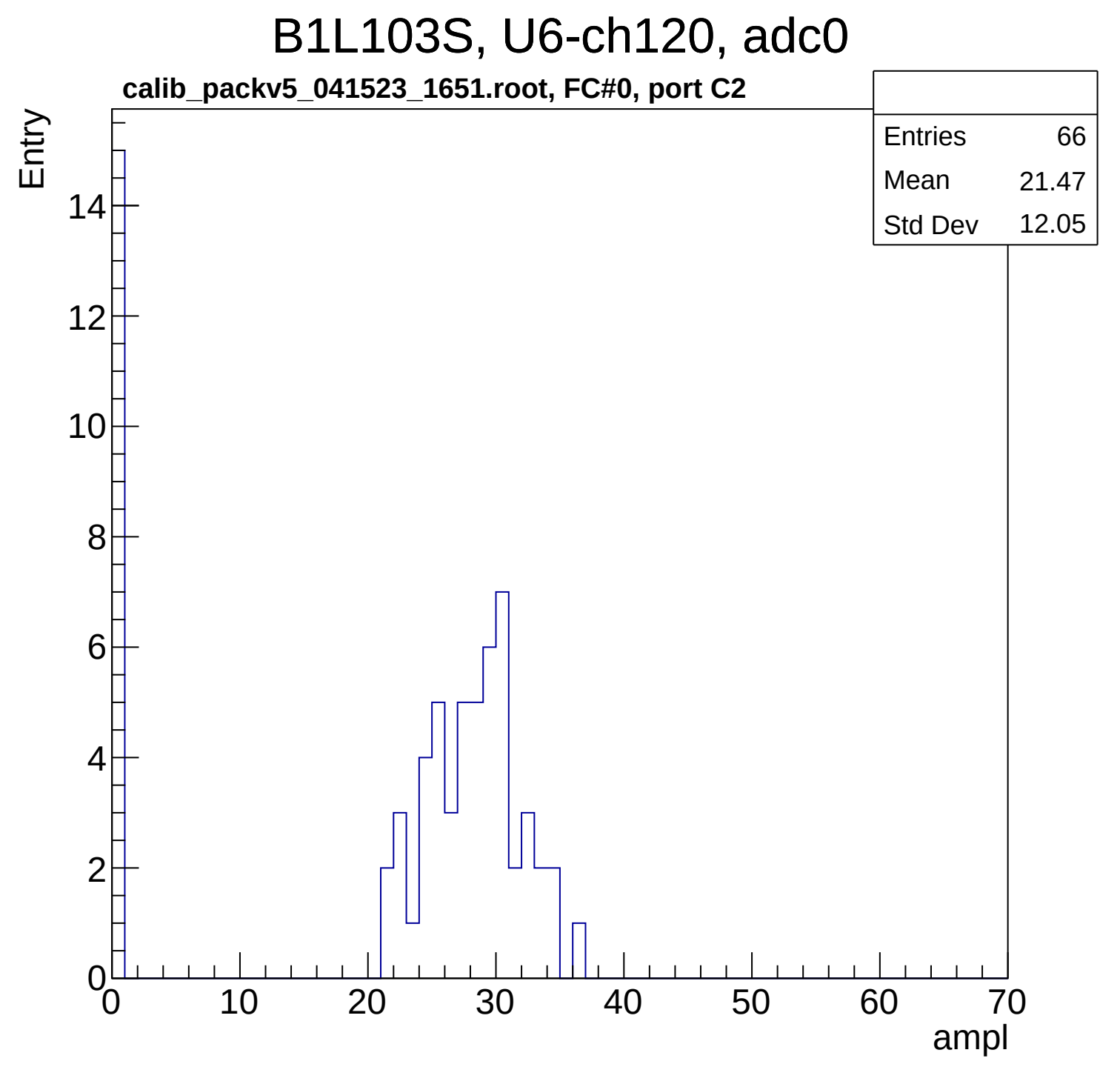
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch120, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 21.47
Std Dev 12.05
Entry
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2
4
6
8
10
12
14
0
10
20
30
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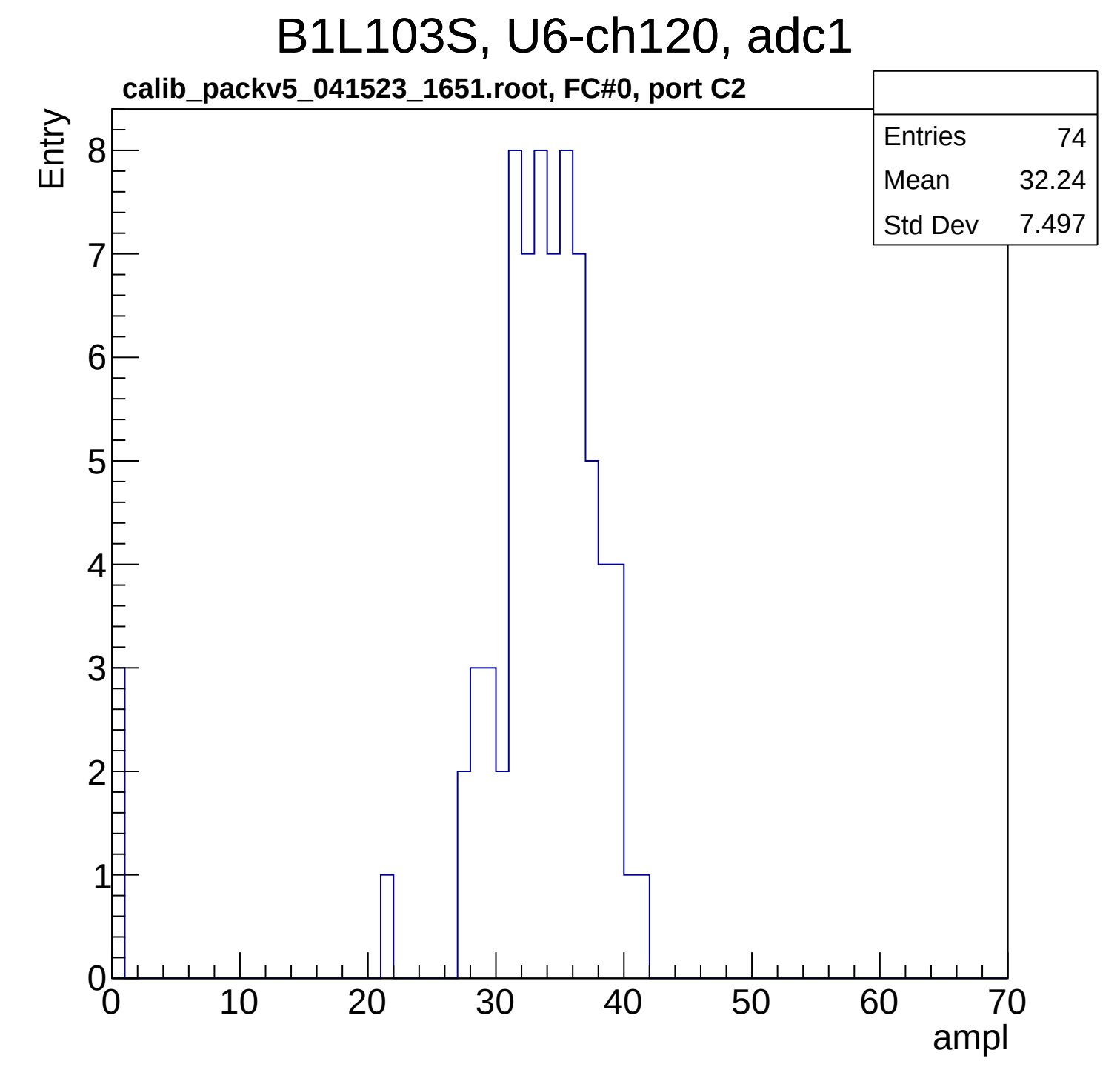
50
60
70
ampl


B1L103S, U6-ch120, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 32.24
Std Dev 7.497
Entry
ampl
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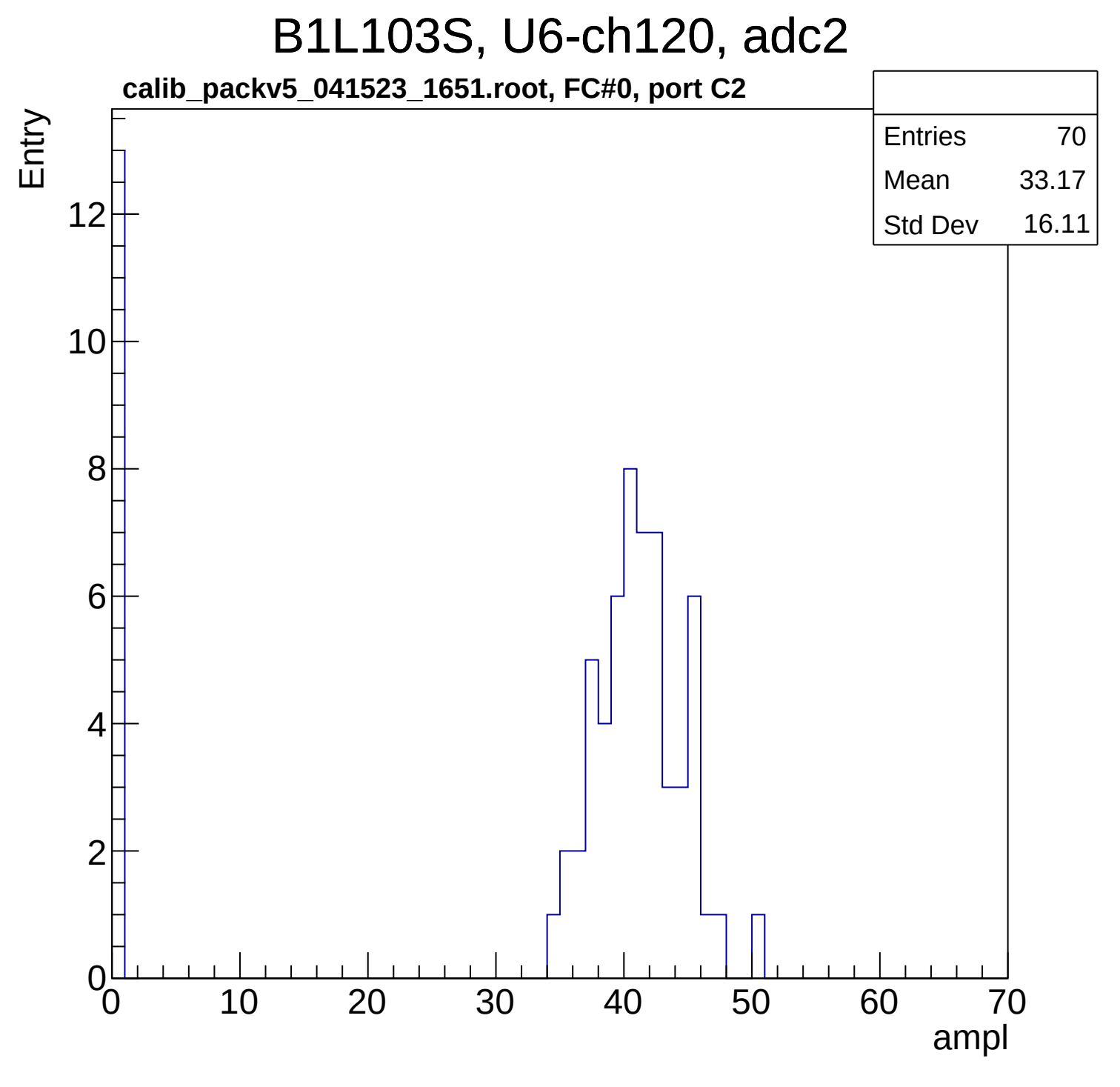
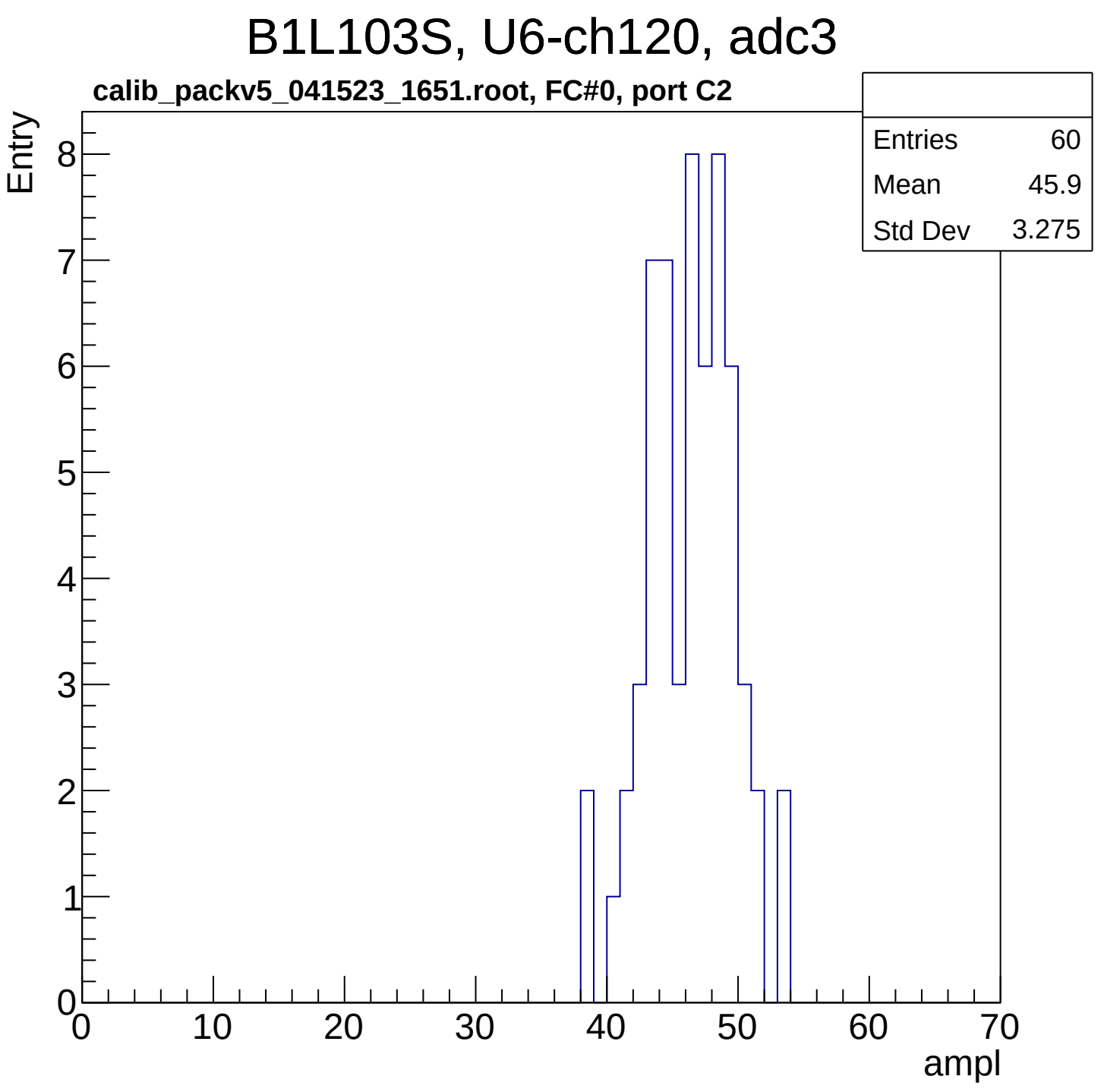
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch120, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 33.17
Std Dev 16.11
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch120, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 45.9
Std Dev 3.275
Entry
ampl
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2
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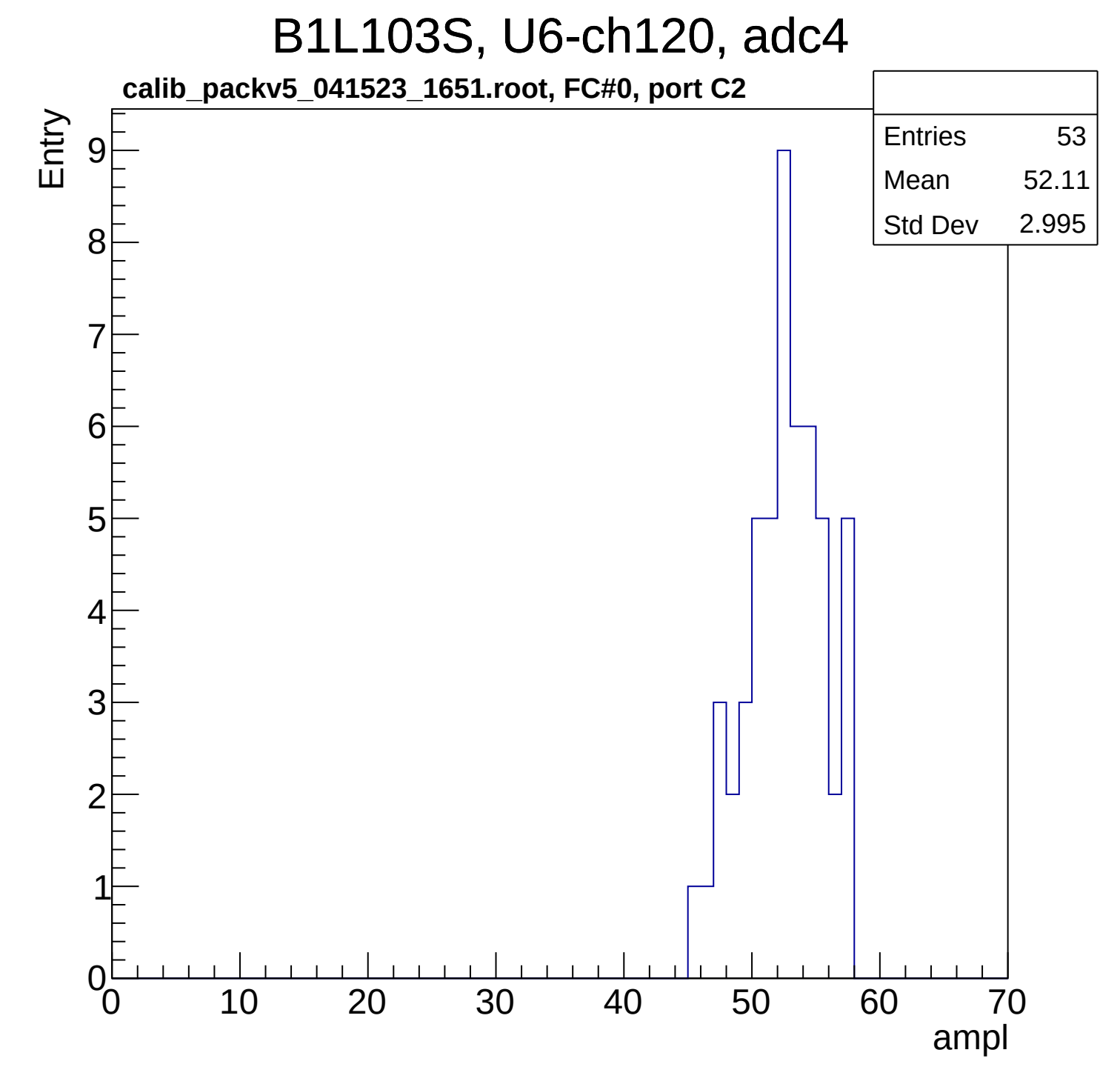
B1L103S, U6-ch120, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 52.11
Std Dev 2.995
Entry
ampl
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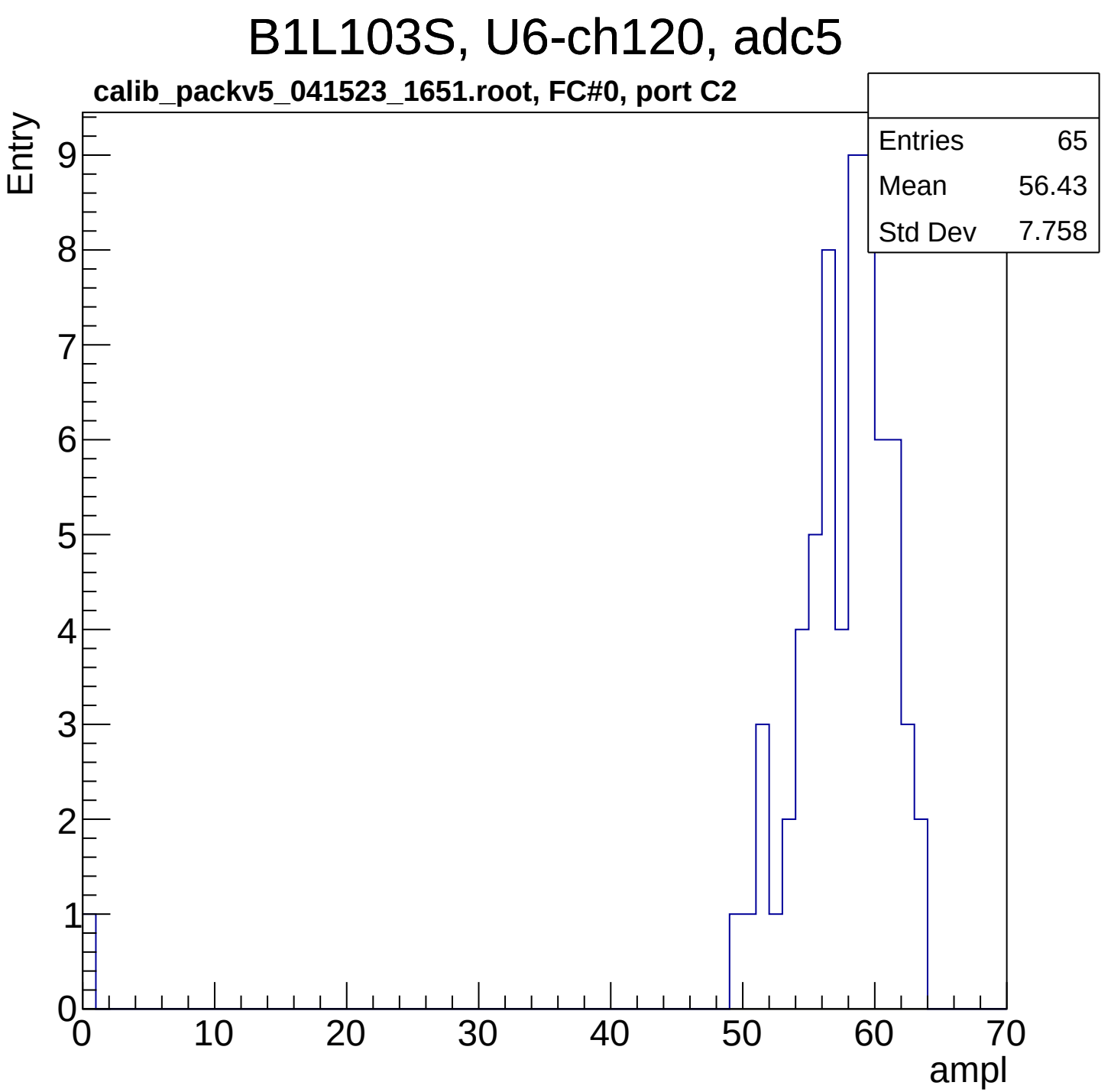
B1L103S, U6-ch120, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 56.43
Std Dev 7.758
Entry
ampl
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4
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6
7
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0
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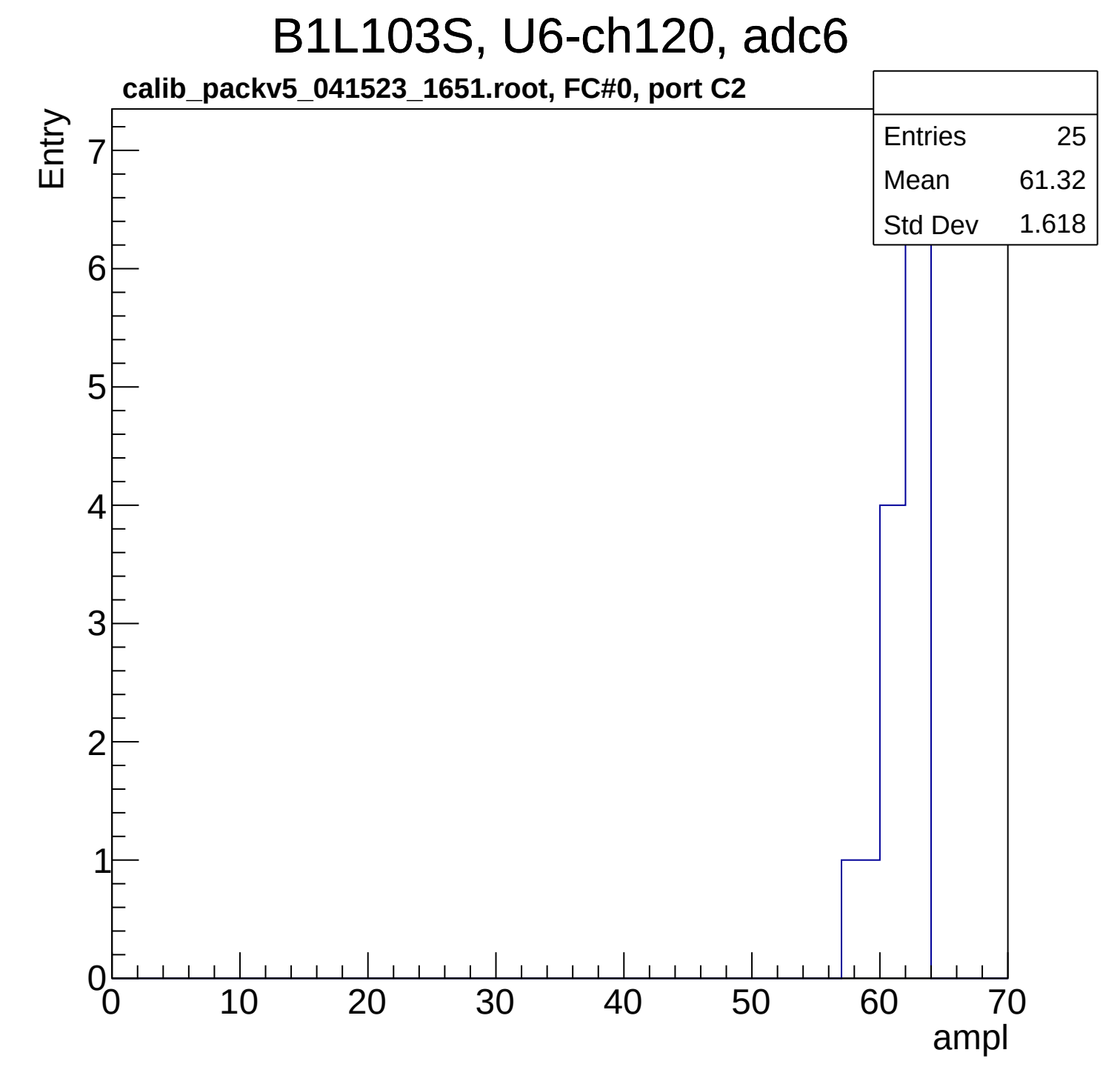
B1L103S, U6-ch120, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 61.32
Std Dev 1.618
Entry
ampl
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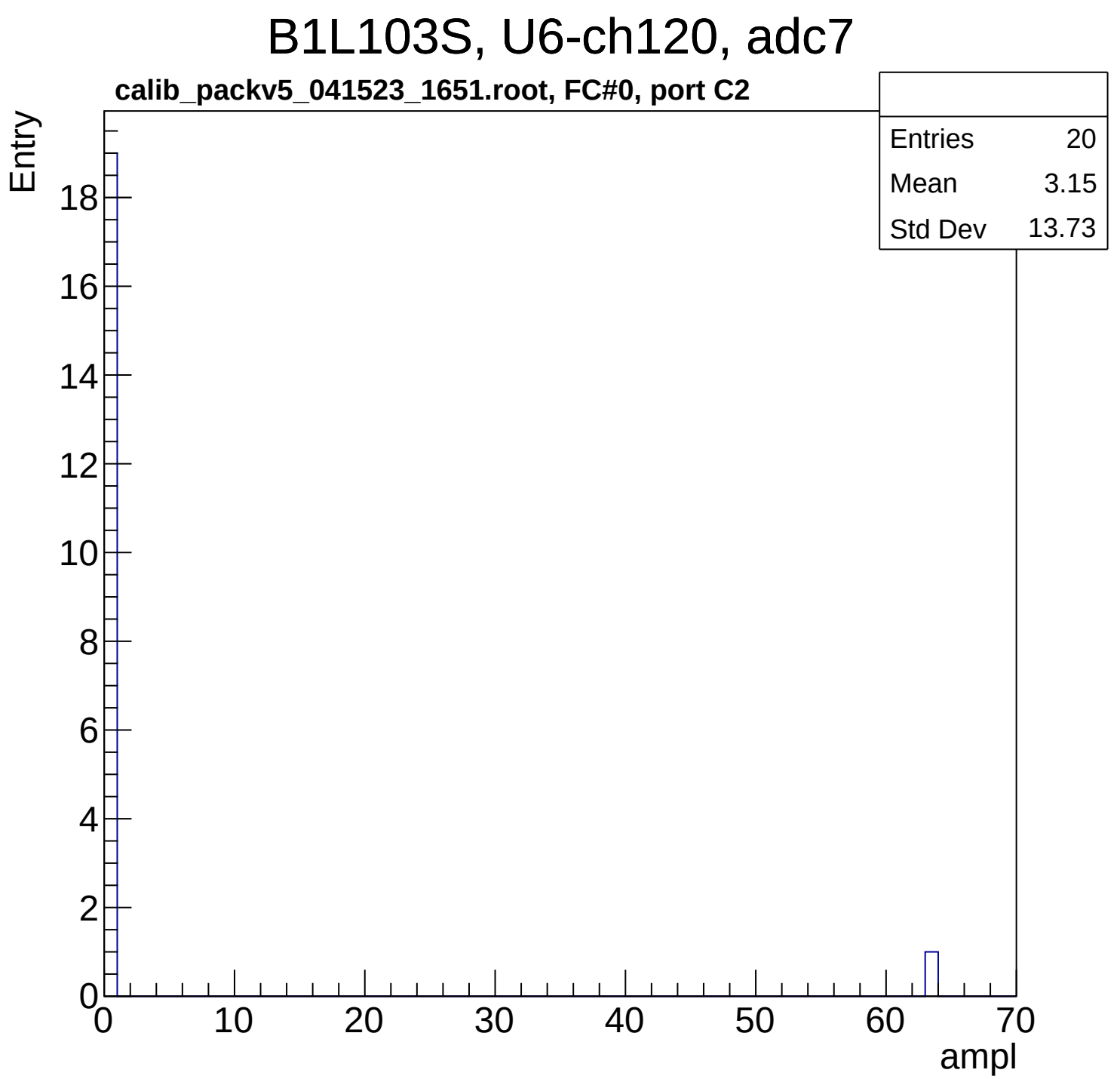
B1L103S, U6-ch120, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
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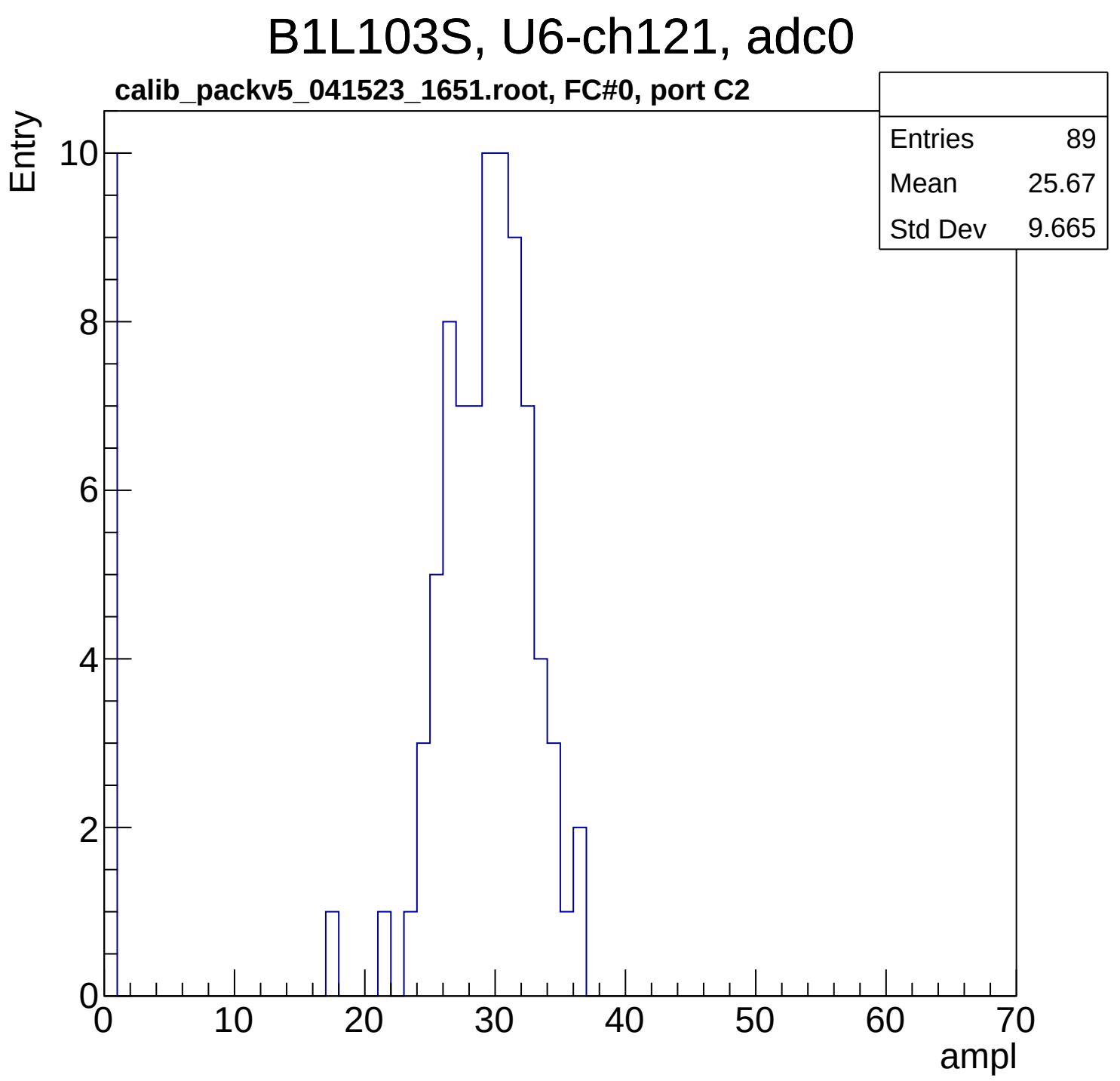
60
70
ampl


B1L103S, U6-ch121, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 25.67
Std Dev 9.665
Entry
ampl
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4
6
8
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0
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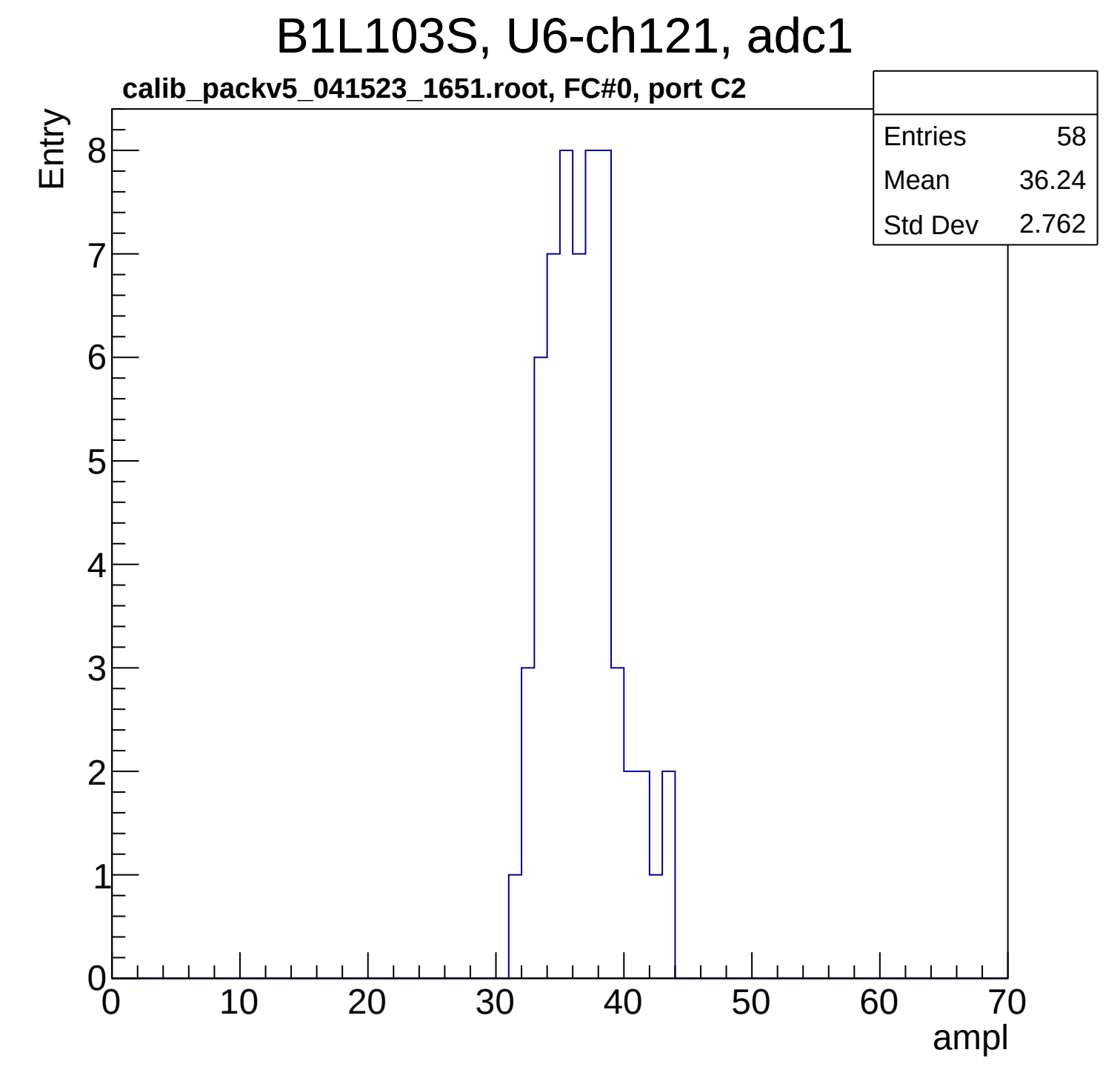
B1L103S, U6-ch121, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 36.24
Std Dev 2.762
Entry
ampl
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2
3
4
5
6
7
8
0
10
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40
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60
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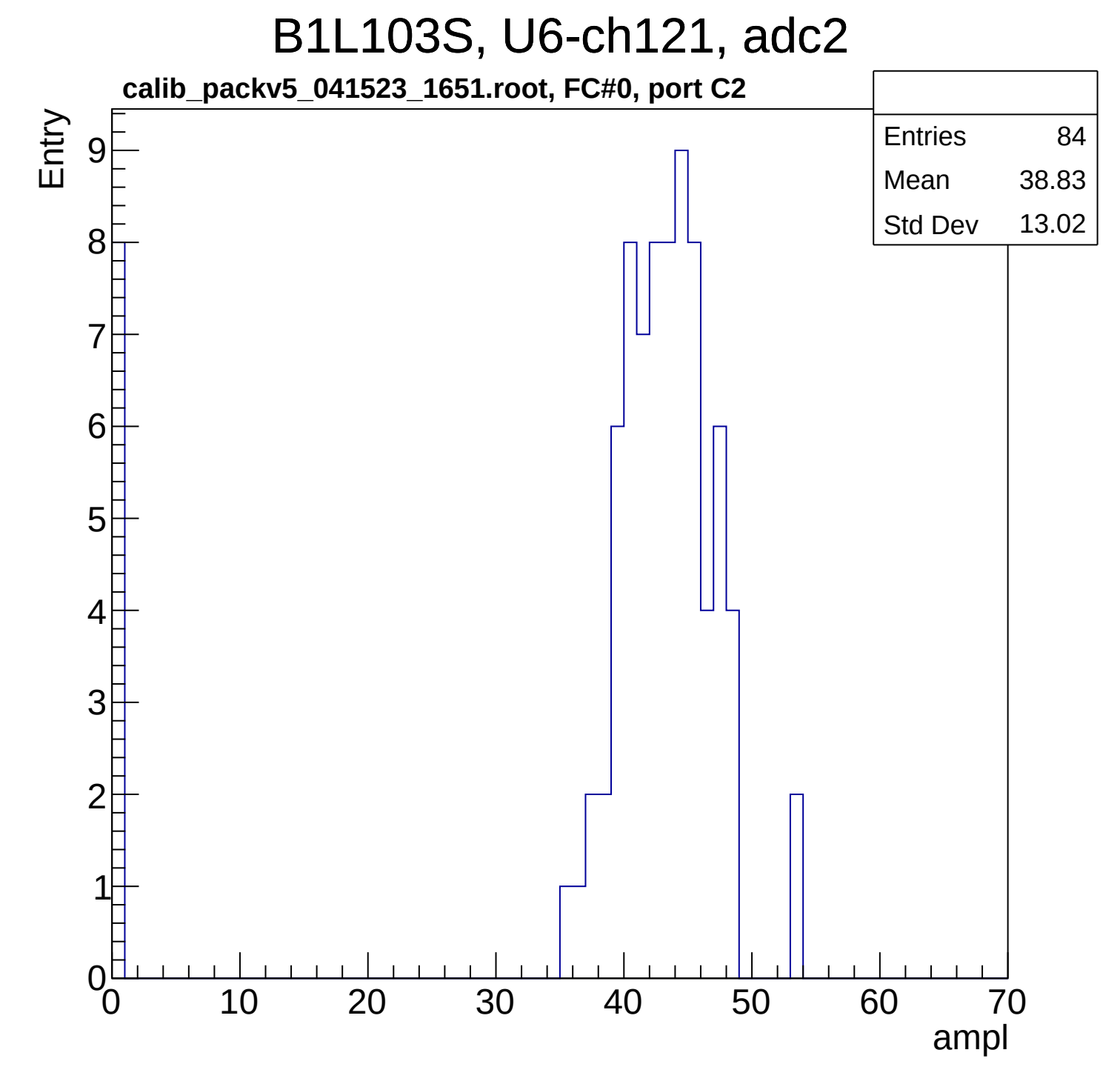
B1L103S, U6-ch121, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 38.83
Std Dev 13.02
Entry
ampl
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3
4
5
6
7
8
9
0
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60
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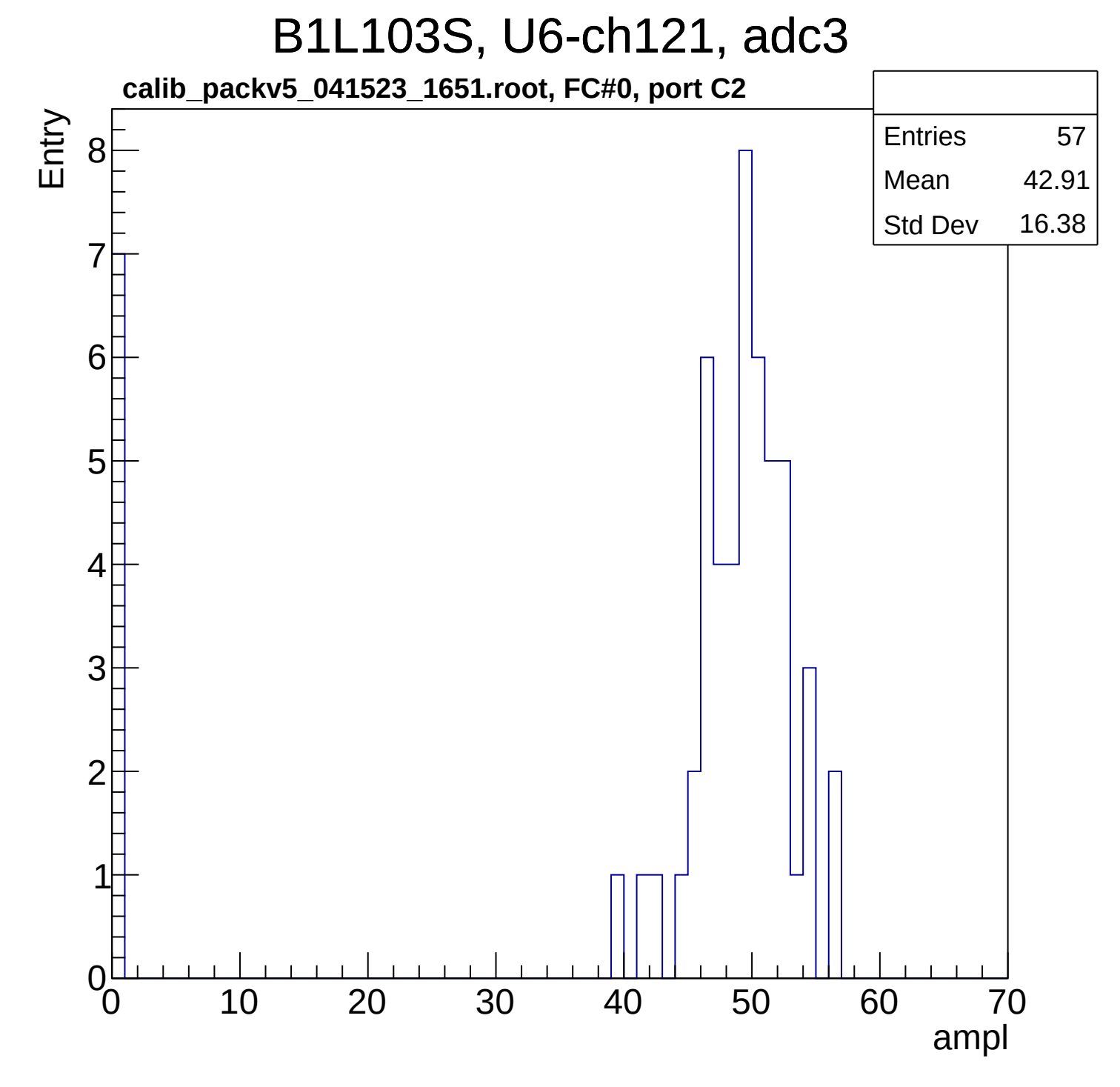
B1L103S, U6-ch121, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 42.91
Std Dev 16.38
Entry
ampl
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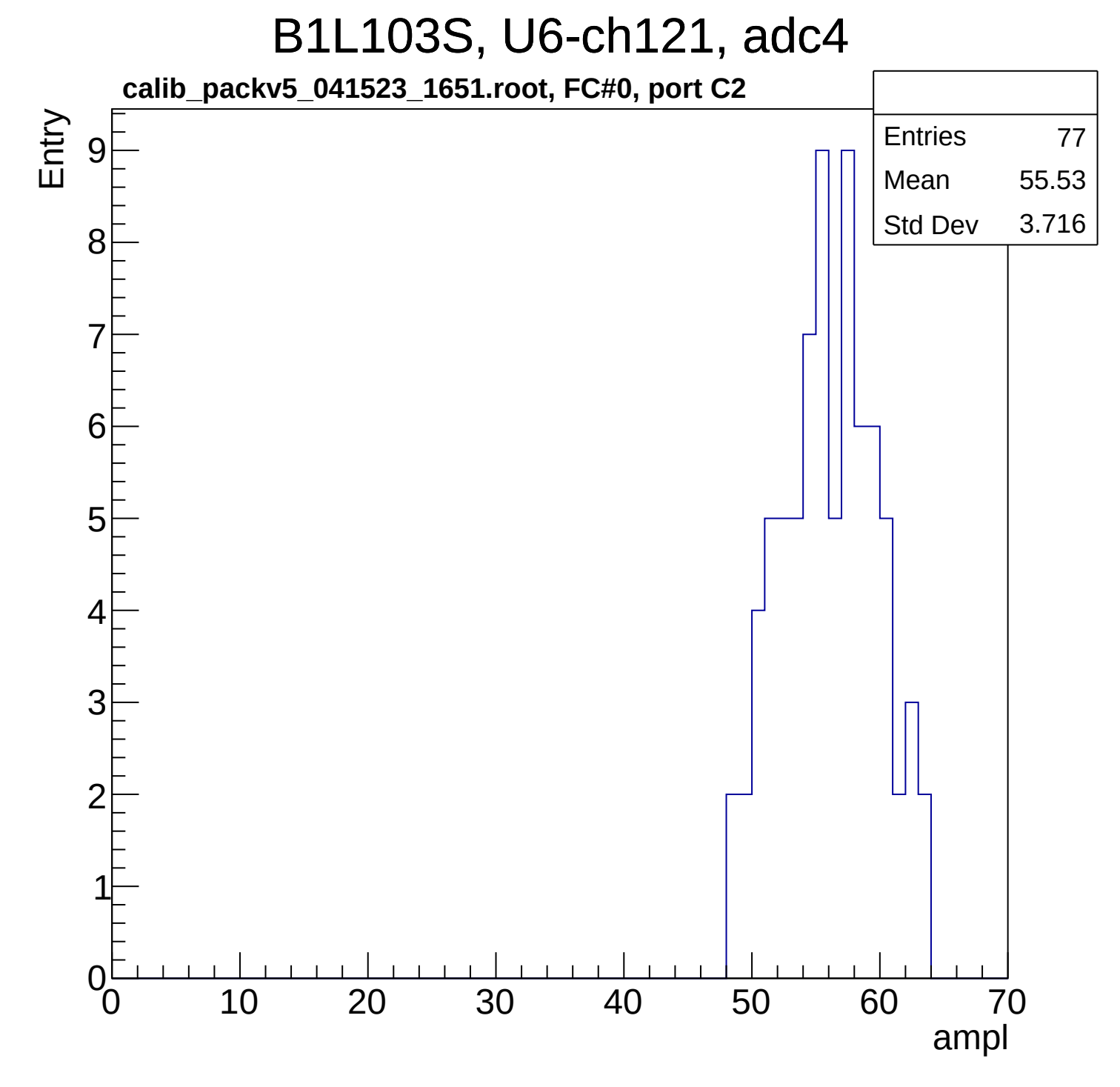
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch121, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 55.53
Std Dev 3.716
Entry
ampl
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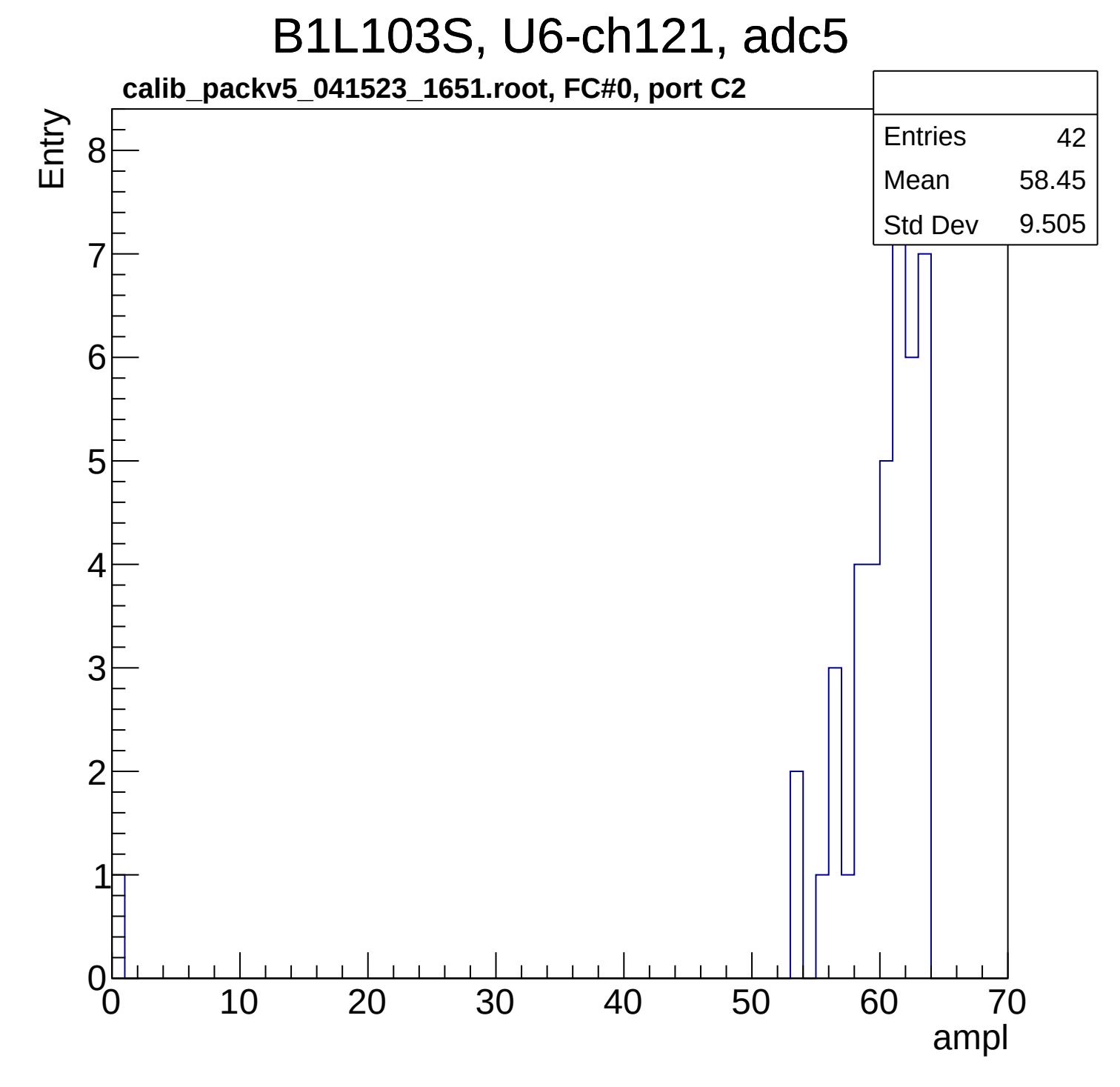
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch121, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 58.45
Std Dev 9.505
Entry
ampl
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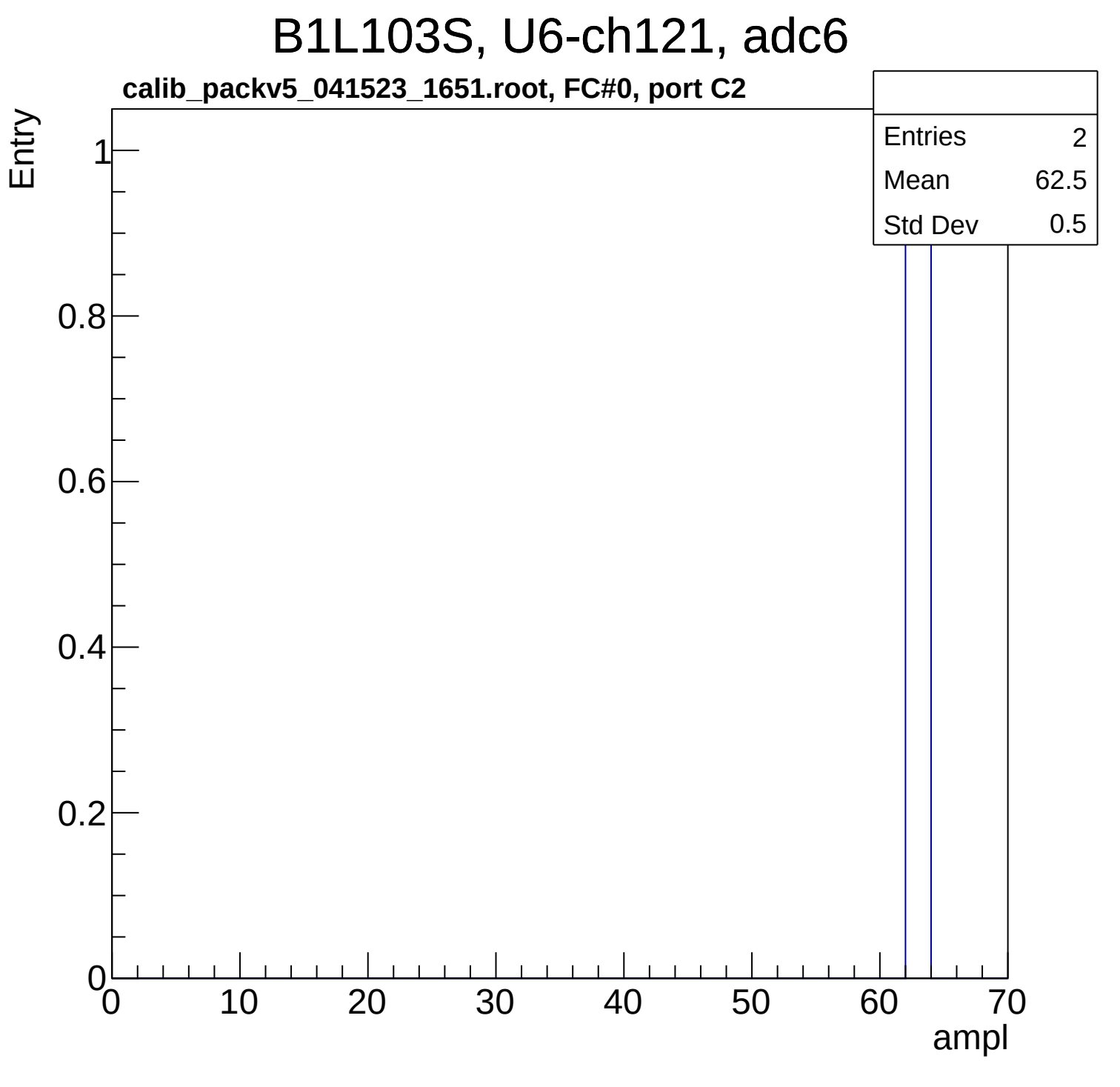
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch121, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
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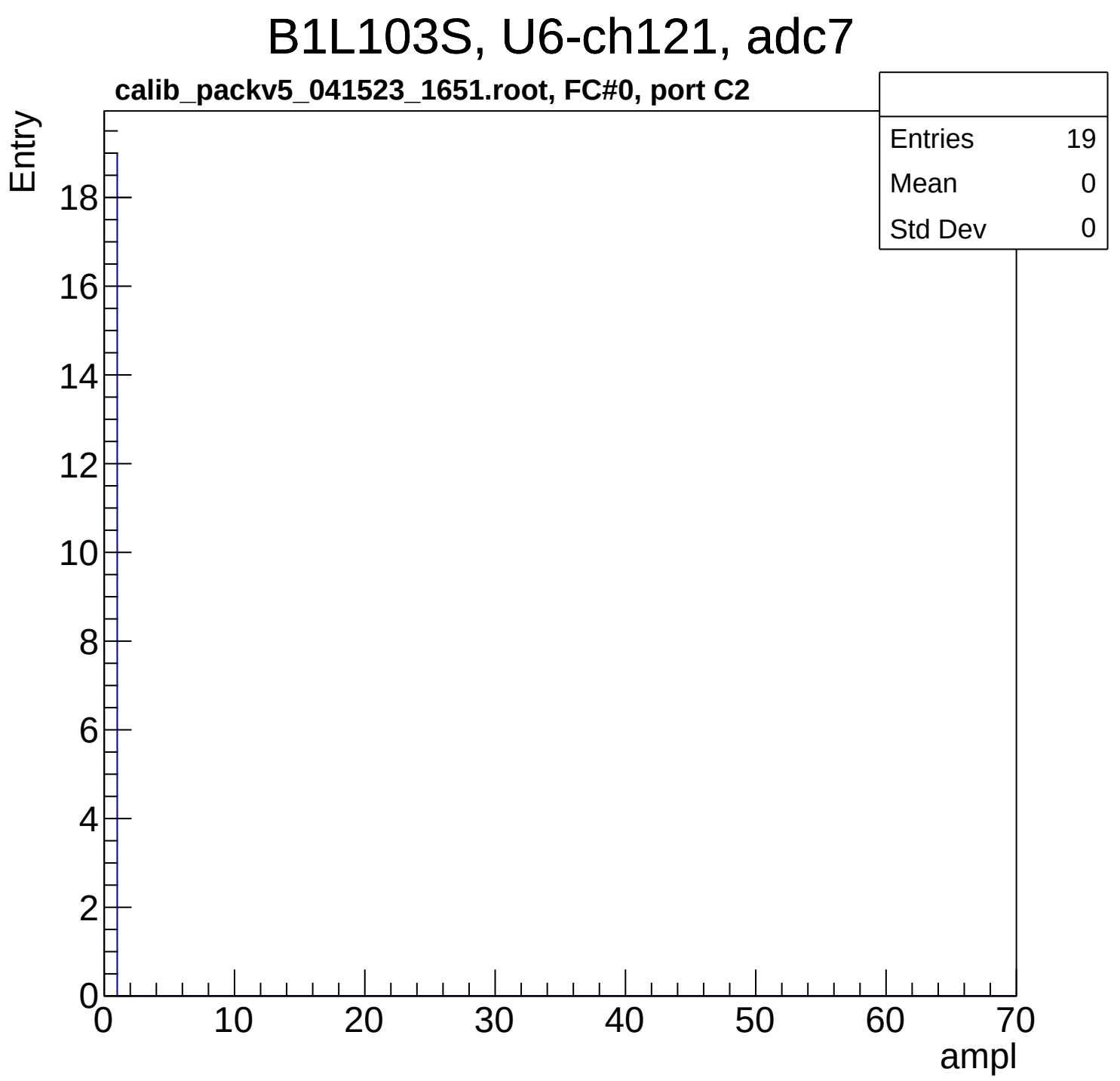
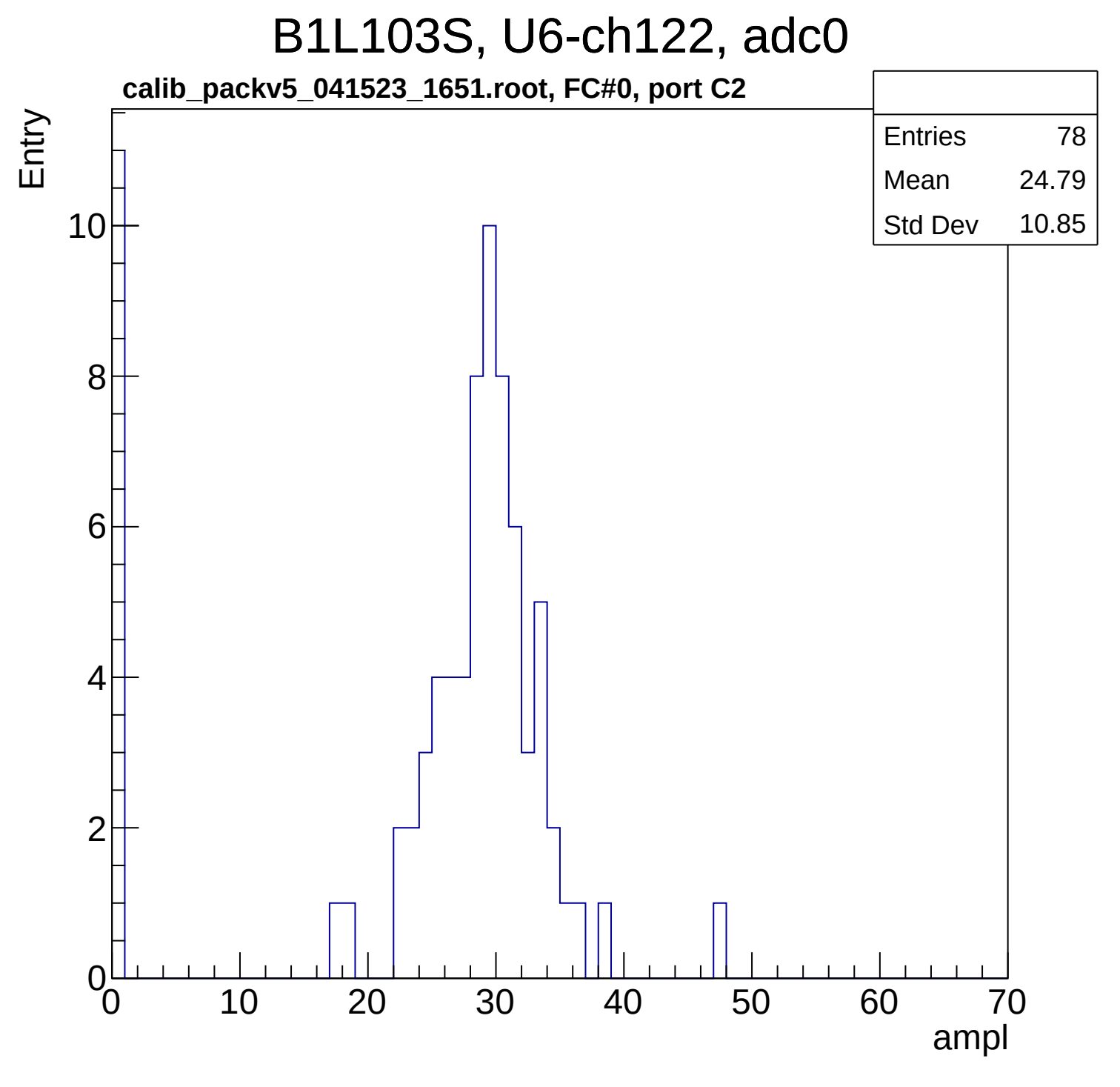
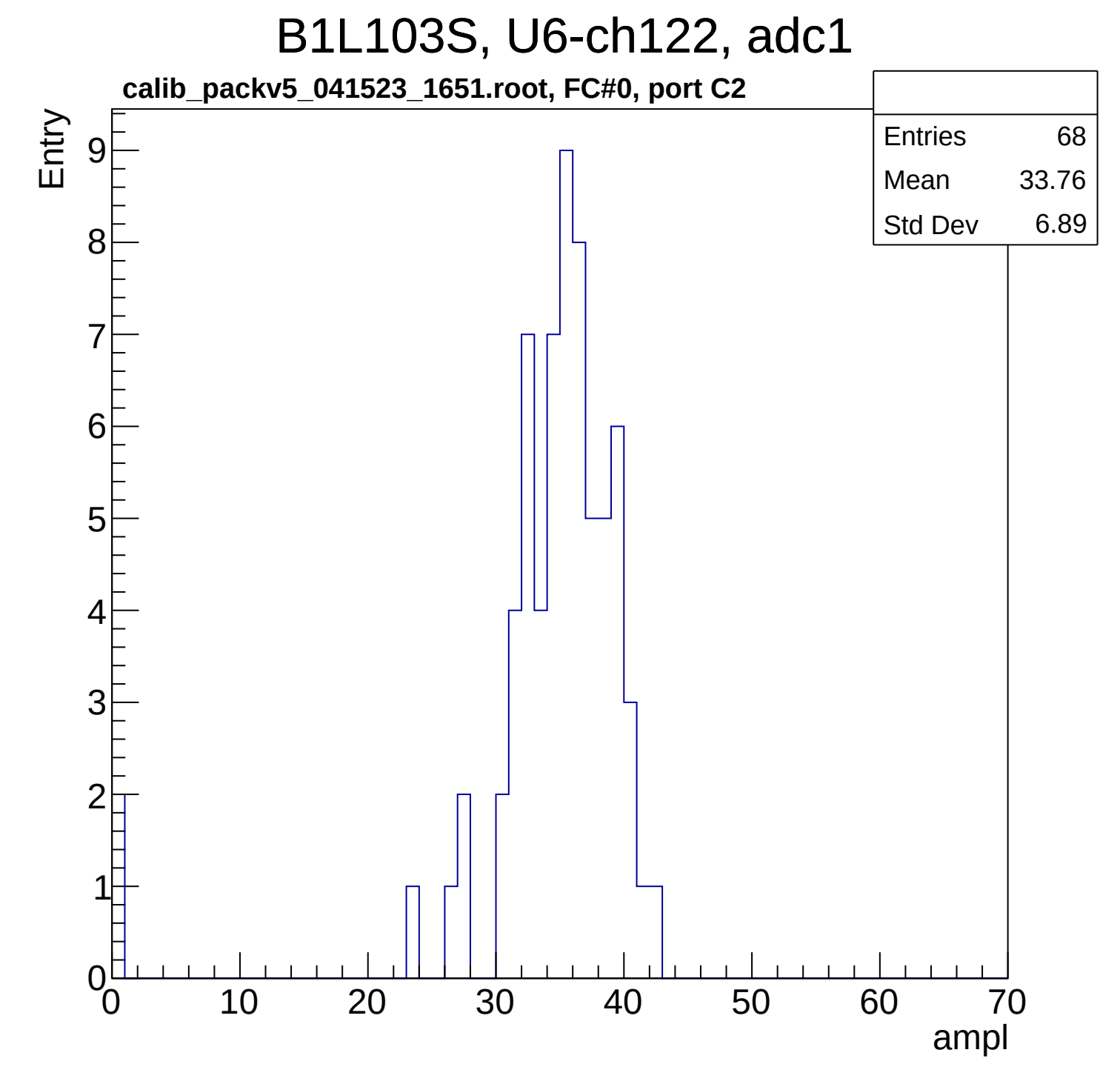
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch121, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch122, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 24.79
Std Dev 10.85
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch122, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 33.76
Std Dev 6.89
Entry
ampl
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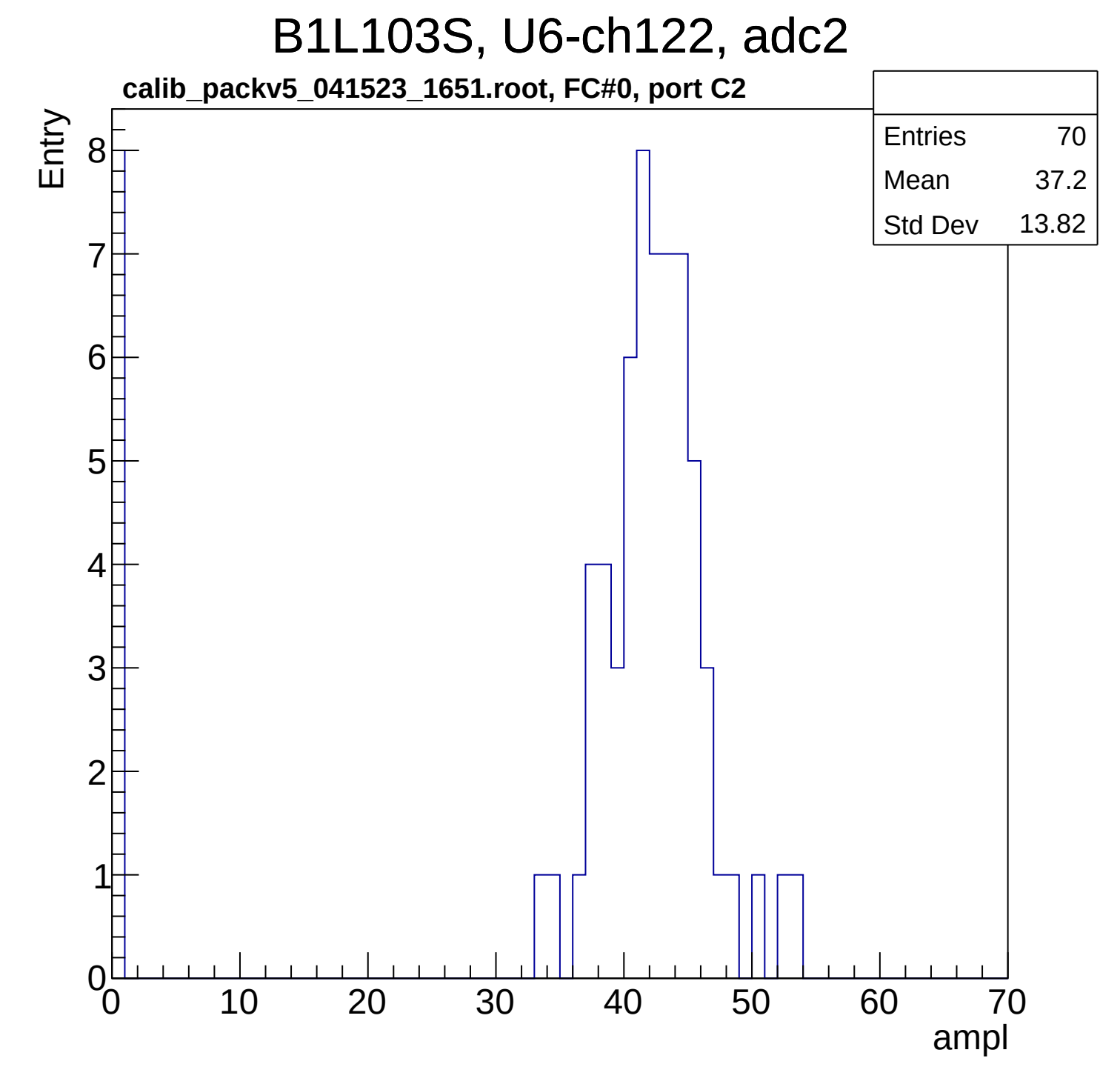
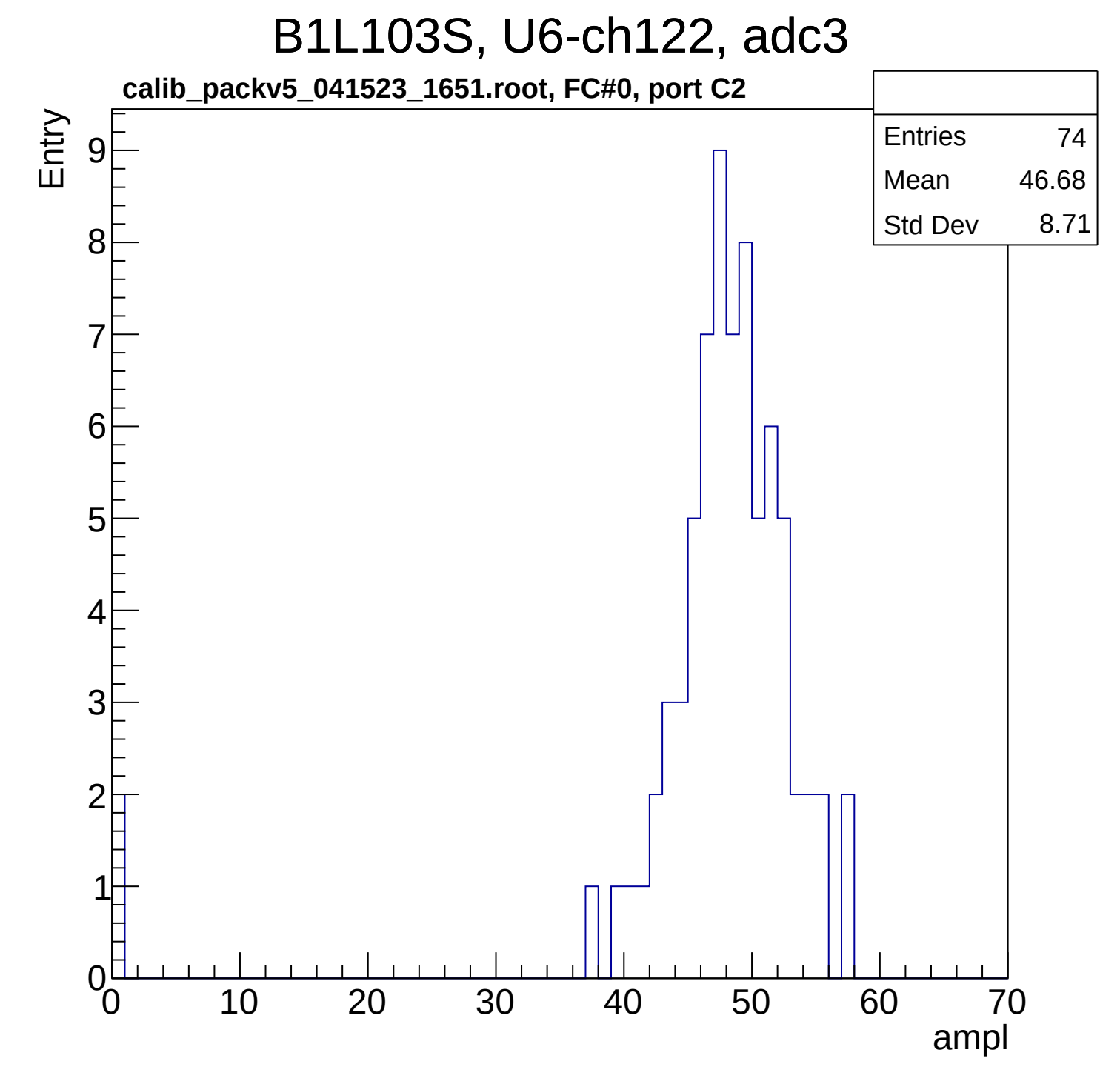
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch122, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 37.2
Std Dev 13.82
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch122, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 46.68
Std Dev 8.71
Entry
ampl
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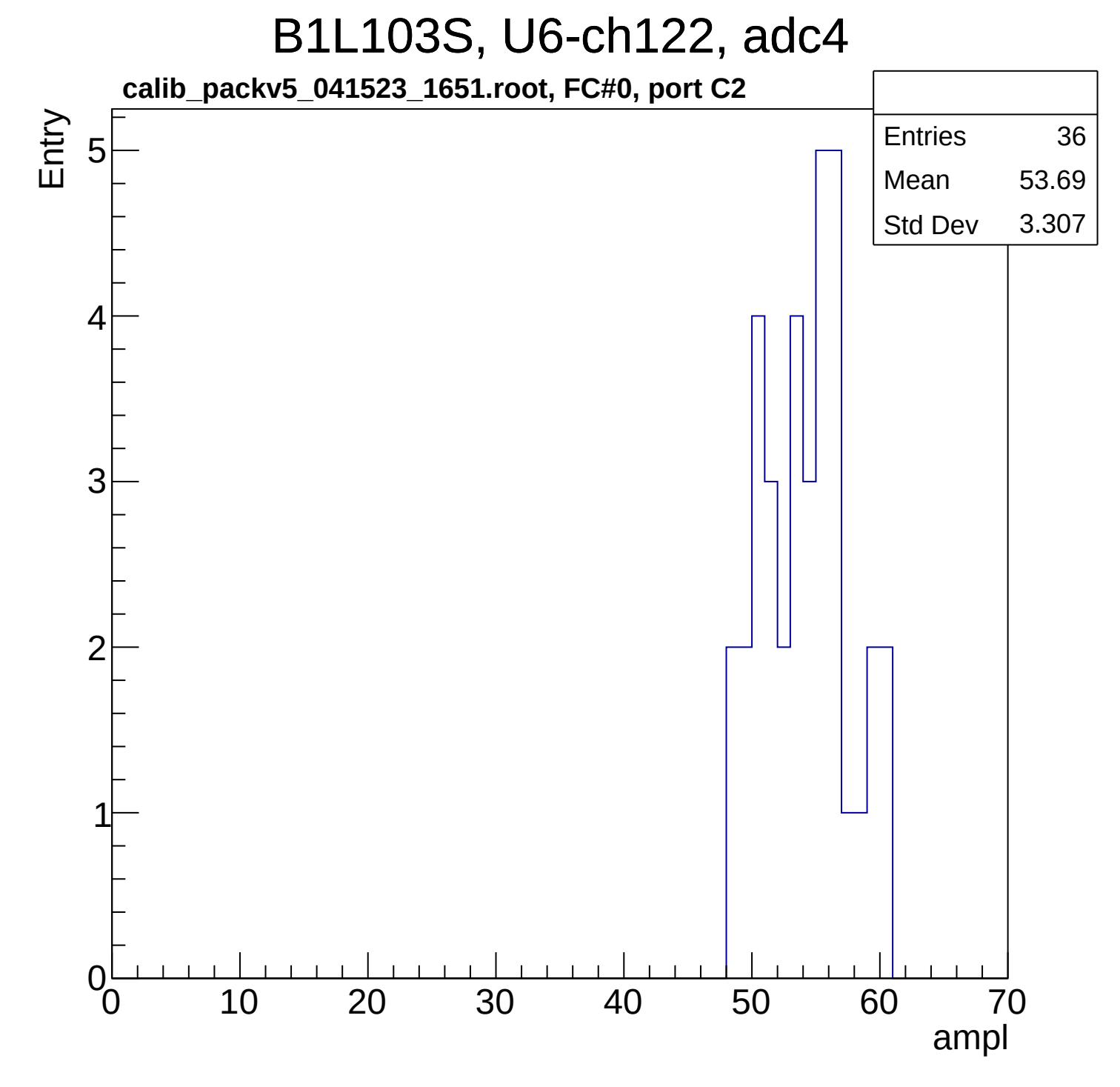
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch122, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 53.69
Std Dev 3.307
Entry
ampl
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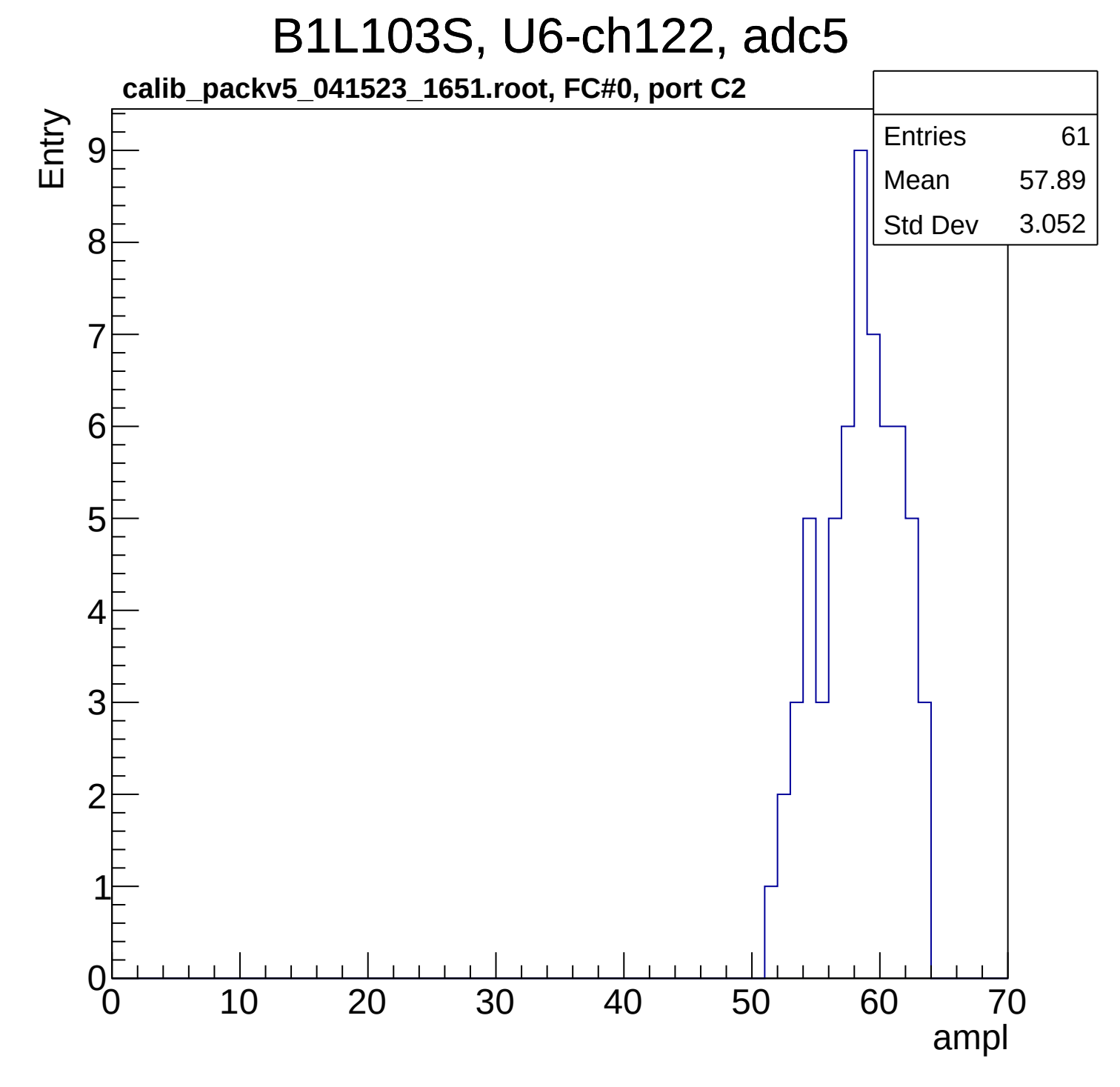
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U6-ch122, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 57.89
Std Dev 3.052
Entry
ampl
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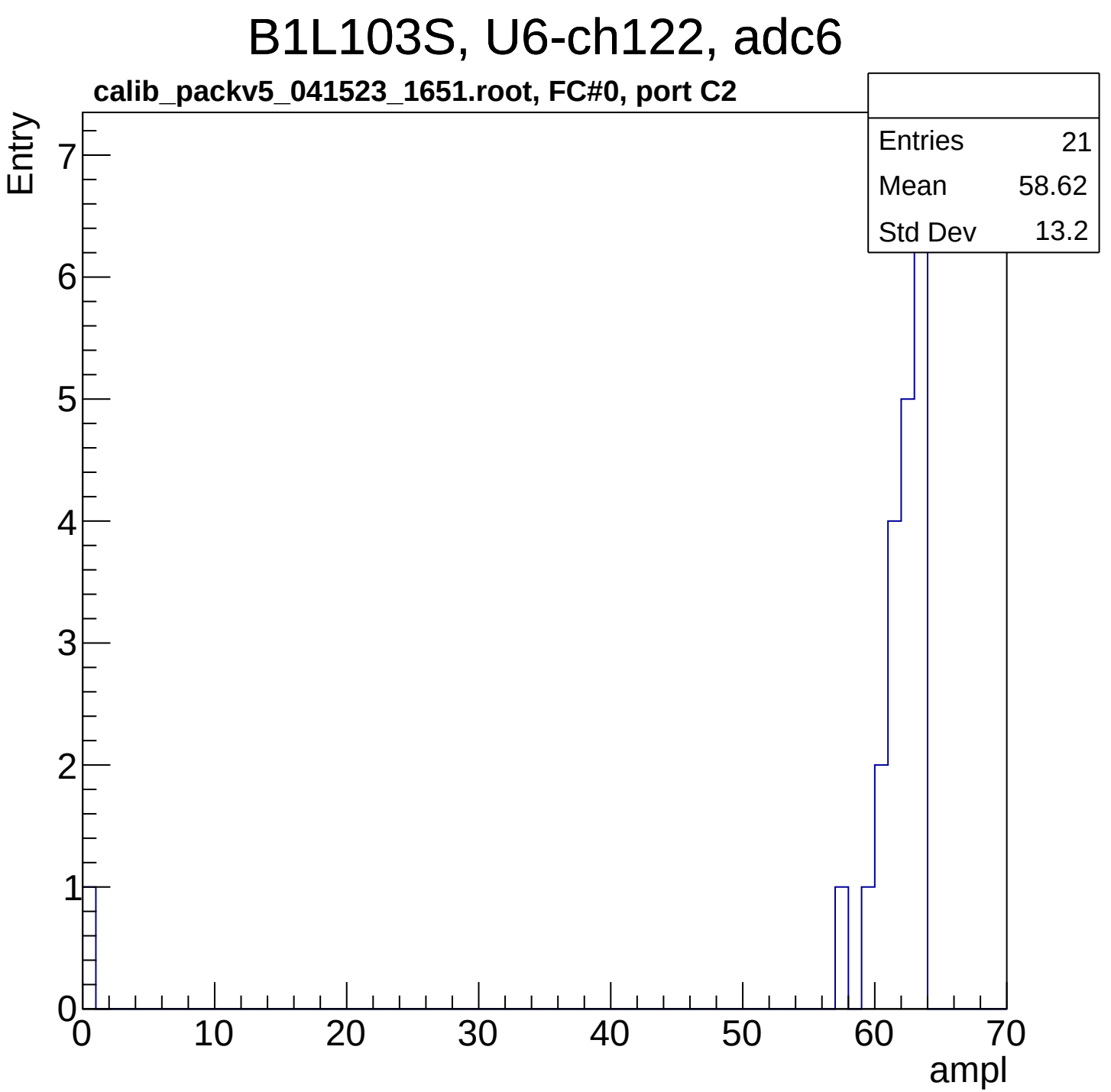
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch122, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 58.62
Std Dev 13.2
Entry
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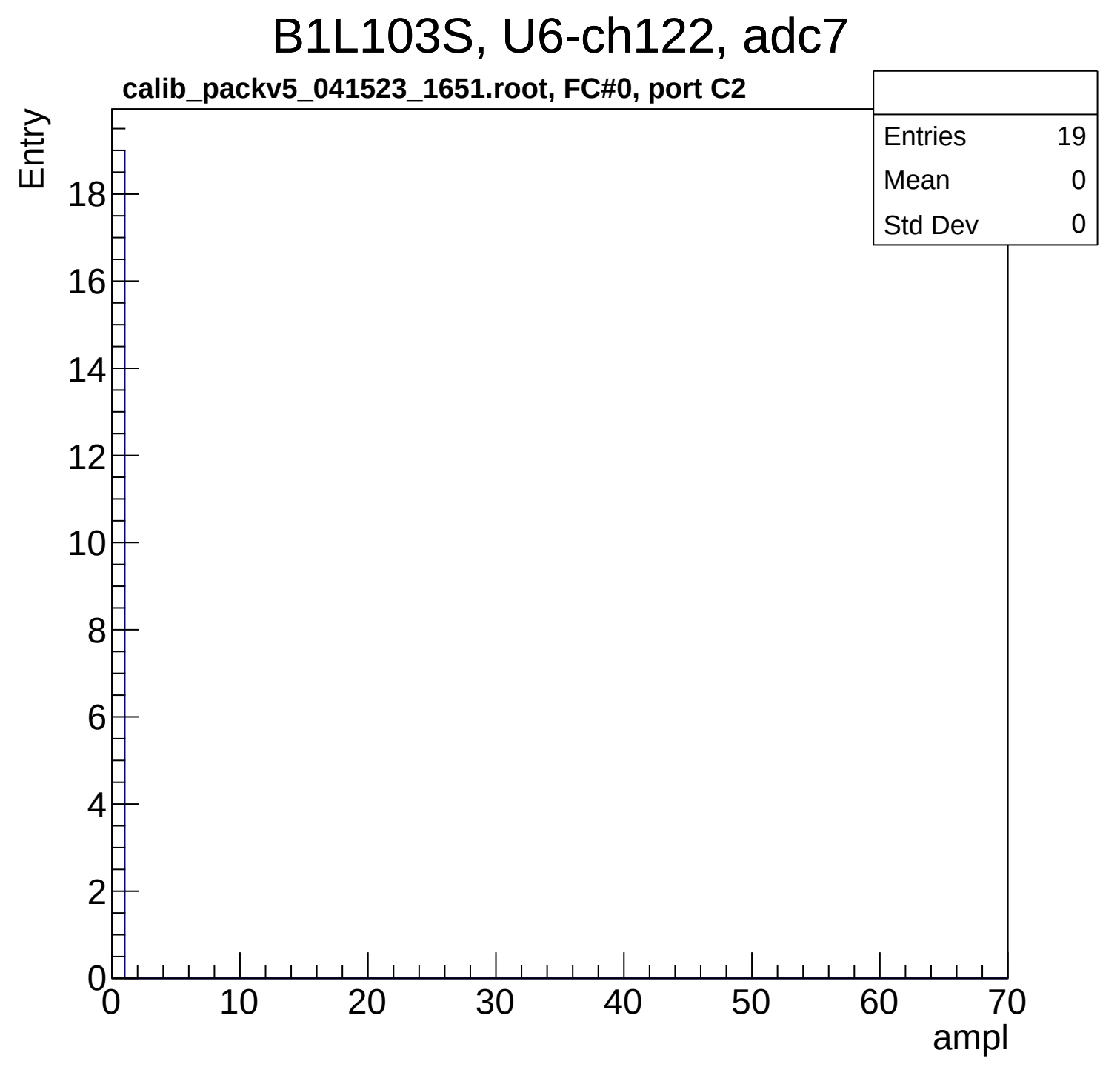
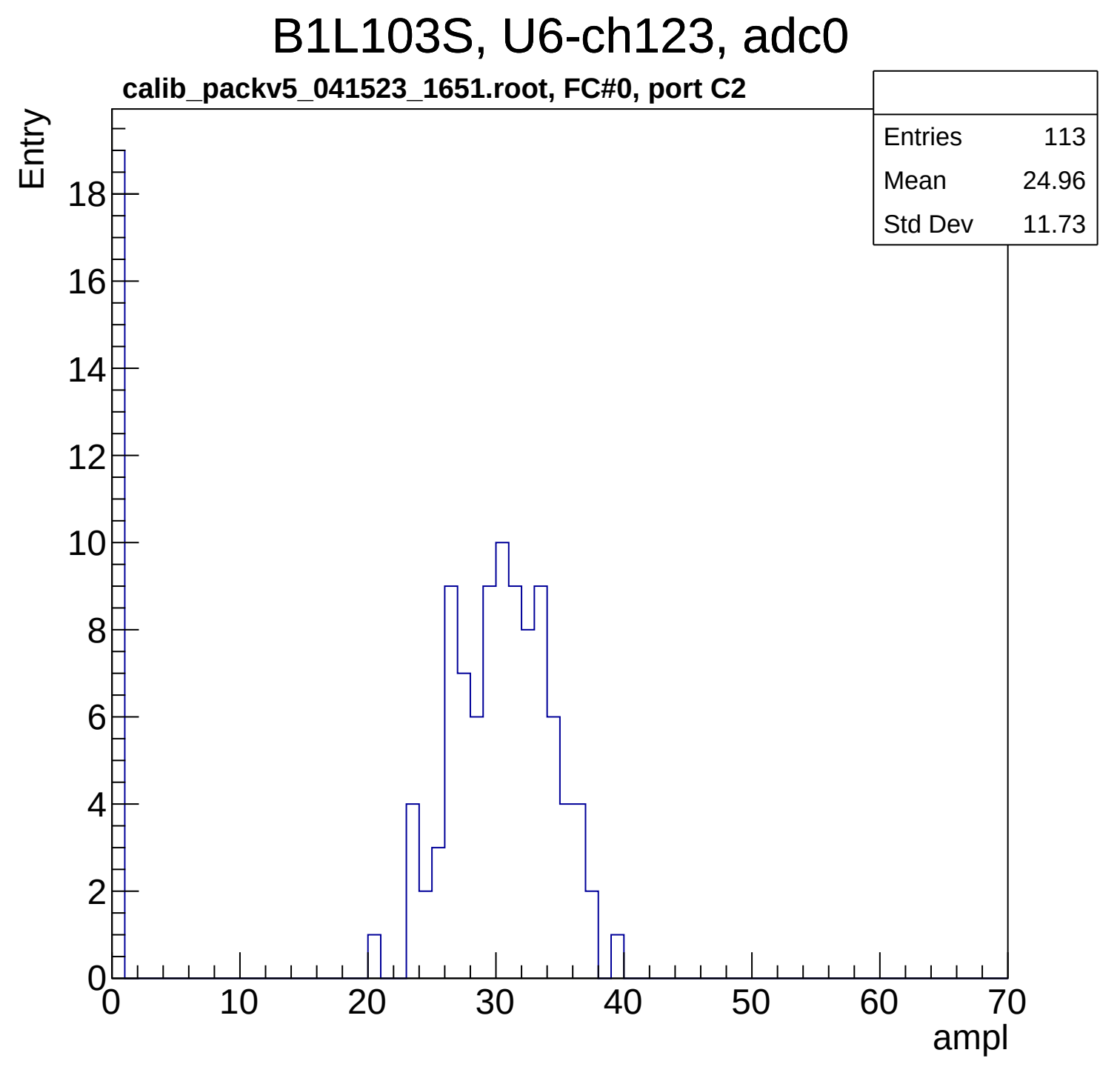
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch122, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch123, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 113
Mean 24.96
Std Dev 11.73
Entry
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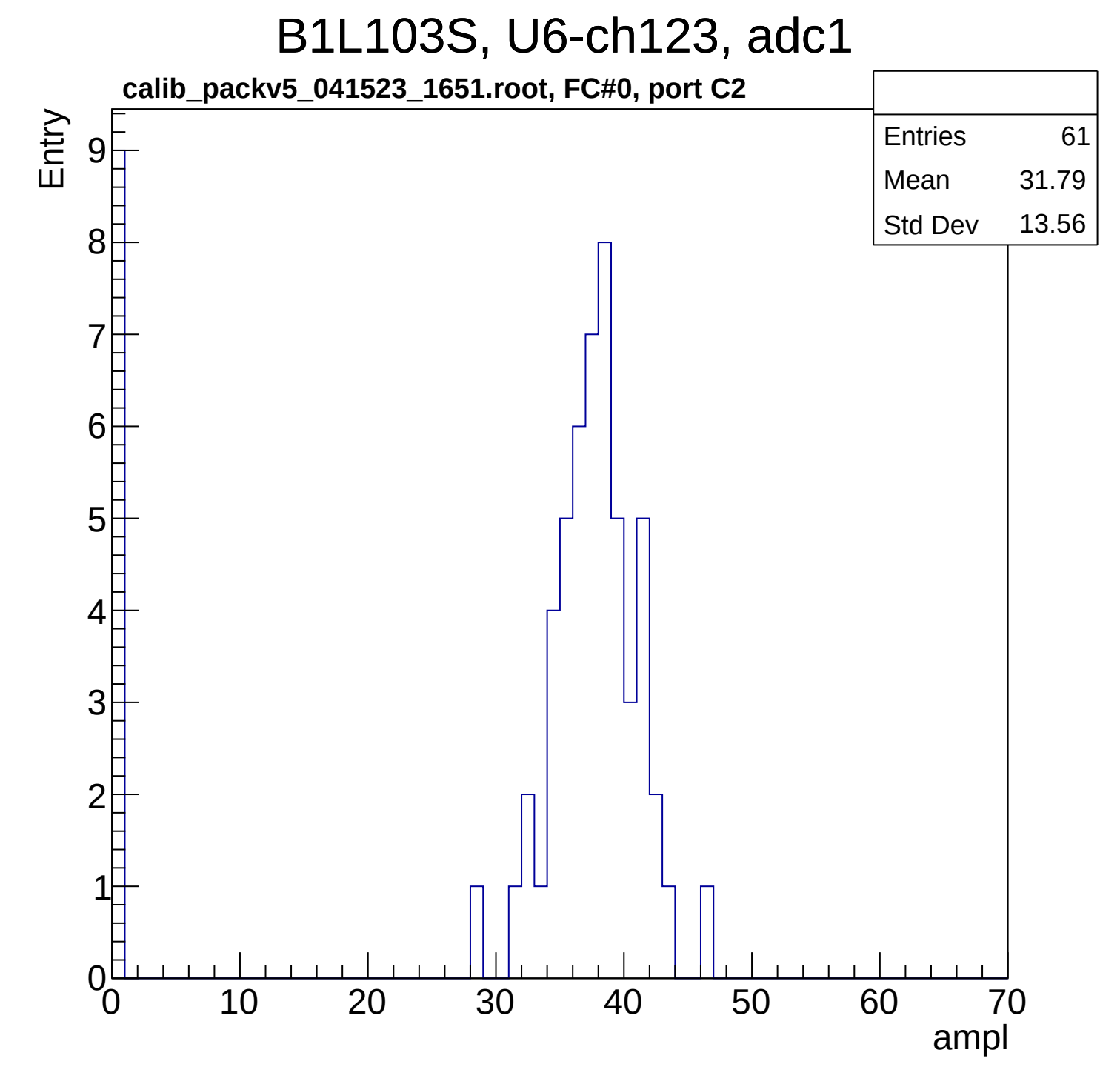
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch123, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 31.79
Std Dev 13.56
Entry
ampl
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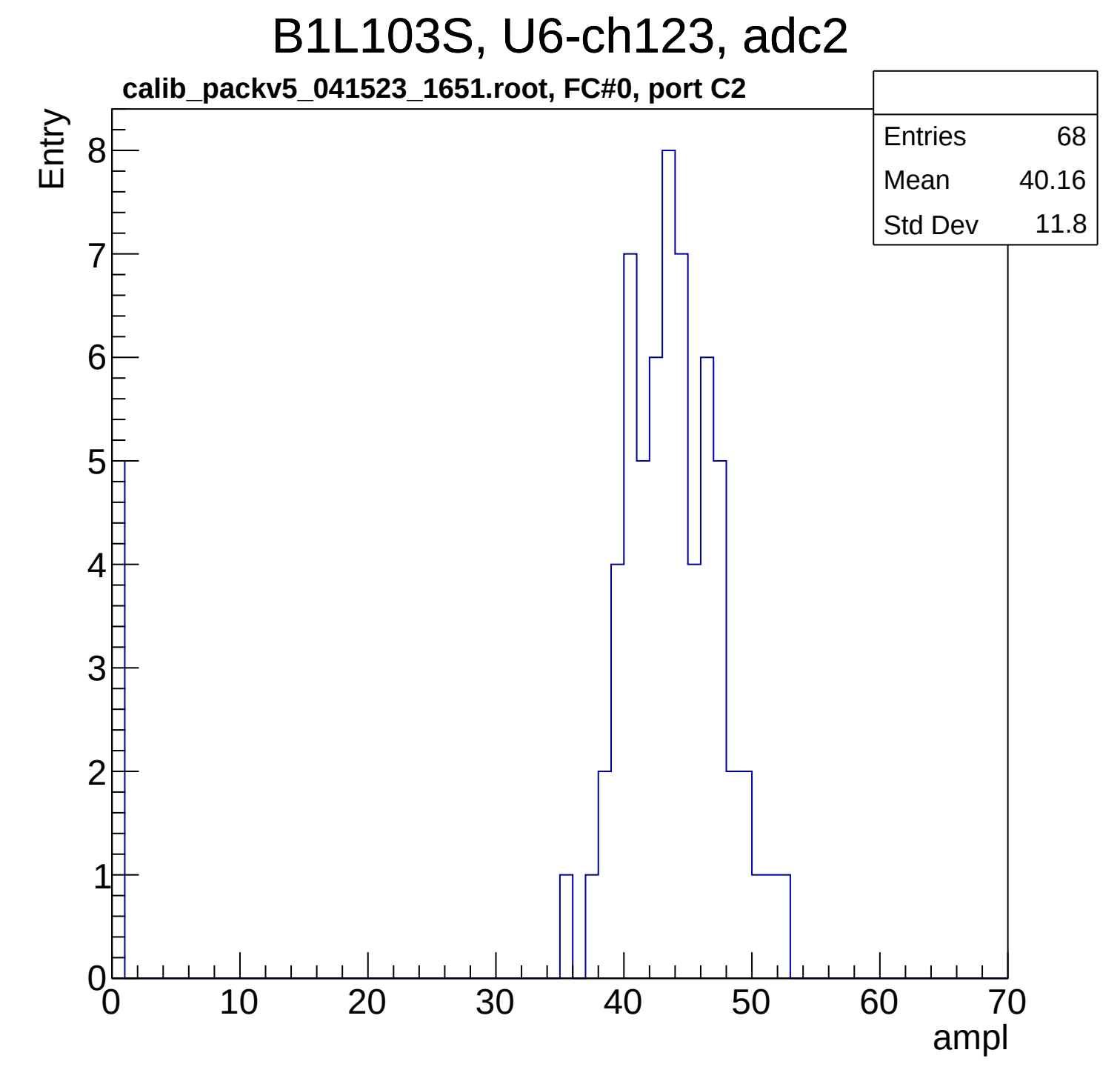
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch123, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 40.16
Std Dev 11.8
Entry
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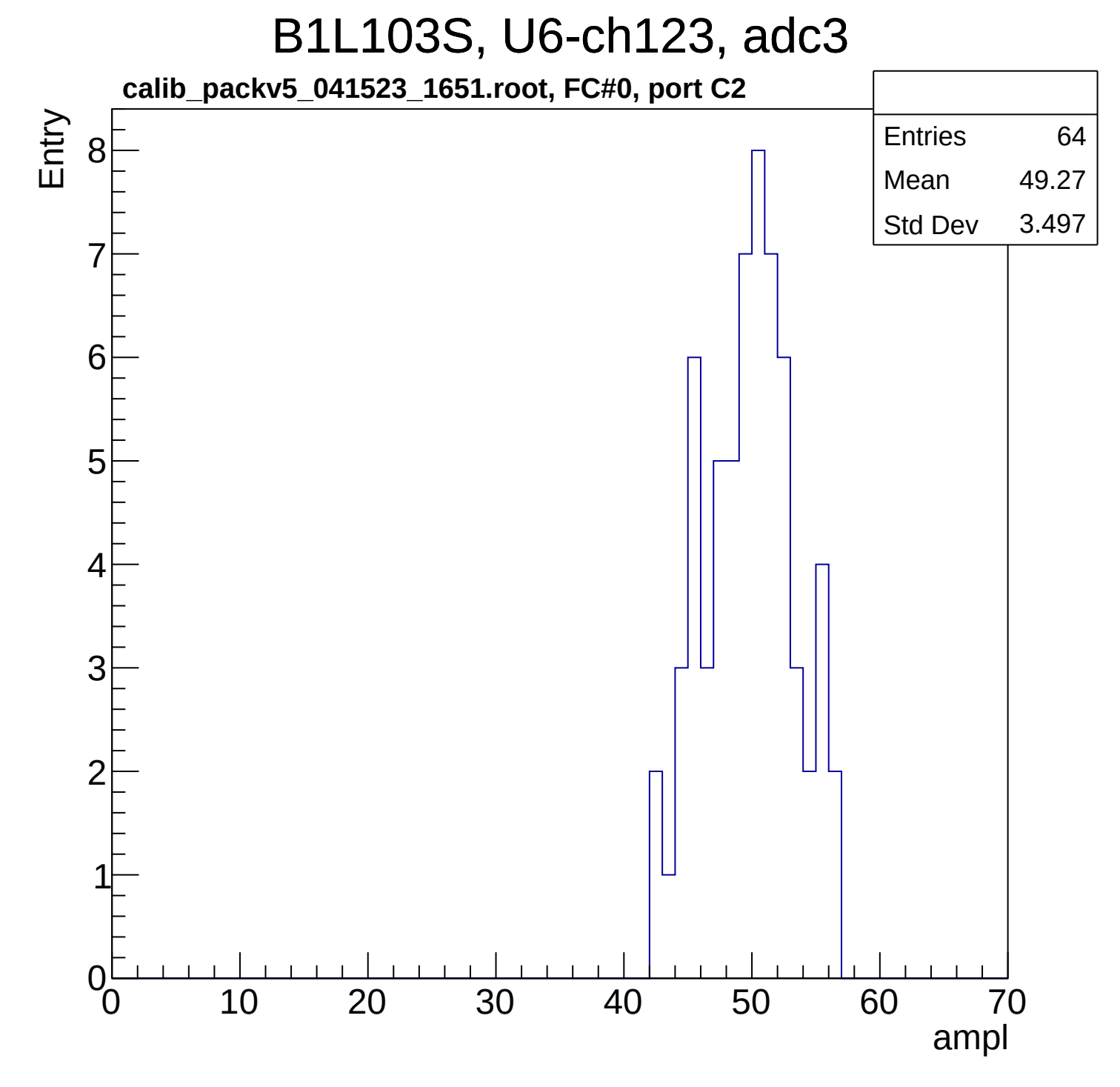
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch123, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 49.27
Std Dev 3.497
Entry
ampl
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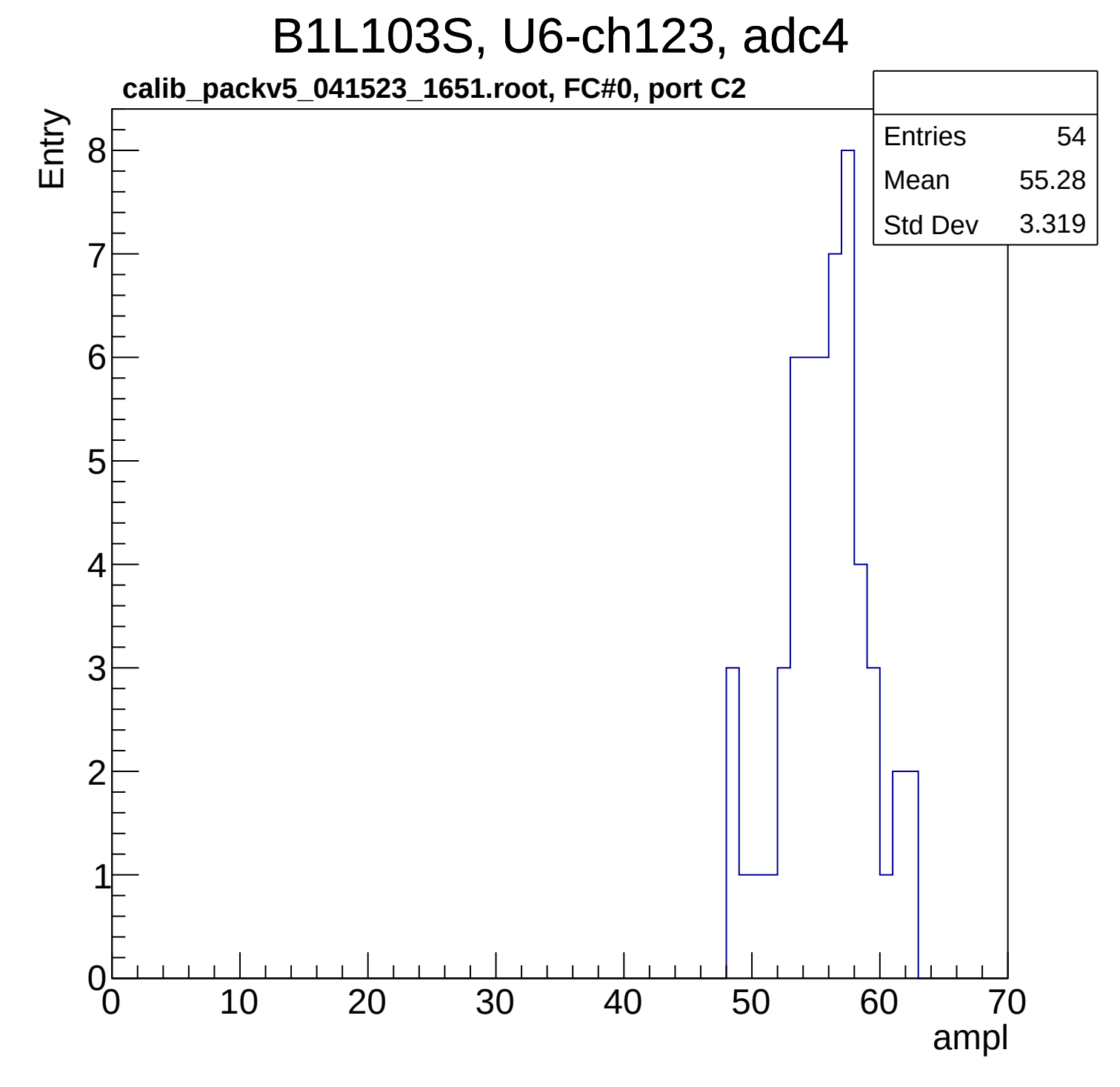
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch123, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 55.28
Std Dev 3.319
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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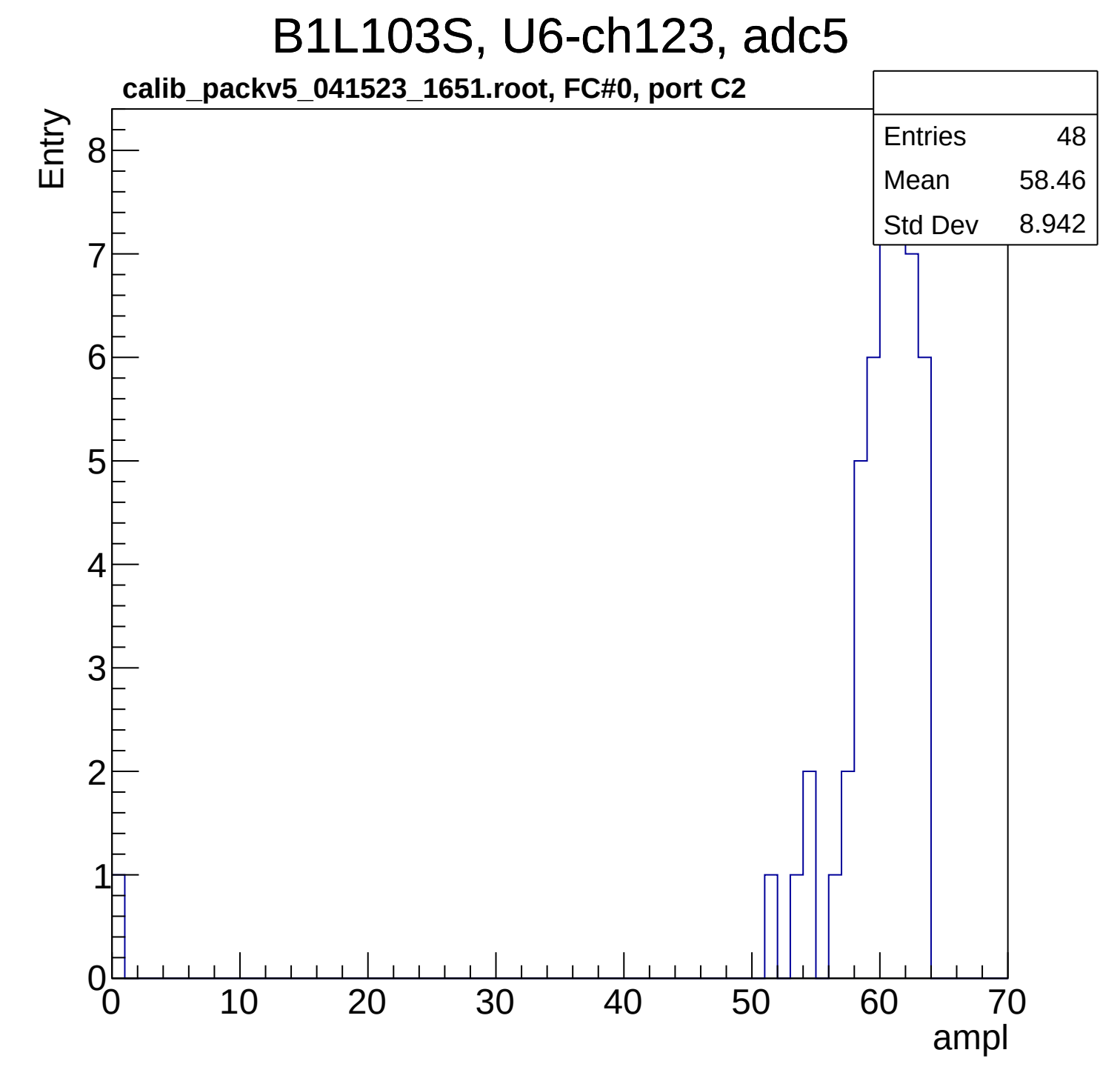
B1L103S, U6-ch123, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 58.46
Std Dev 8.942
Entry
ampl
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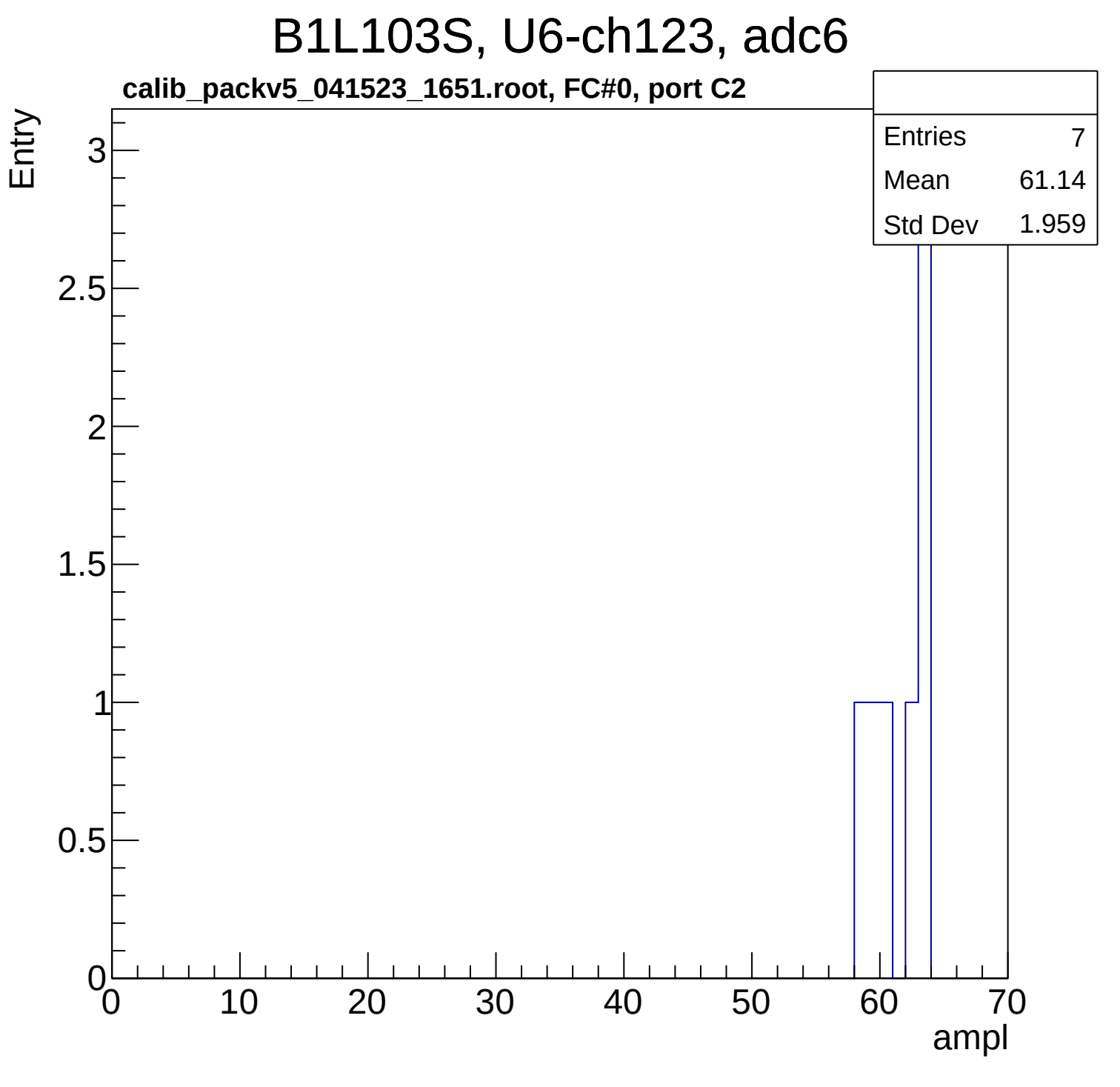
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch123, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 61.14
Std Dev 1.959
Entry
ampl
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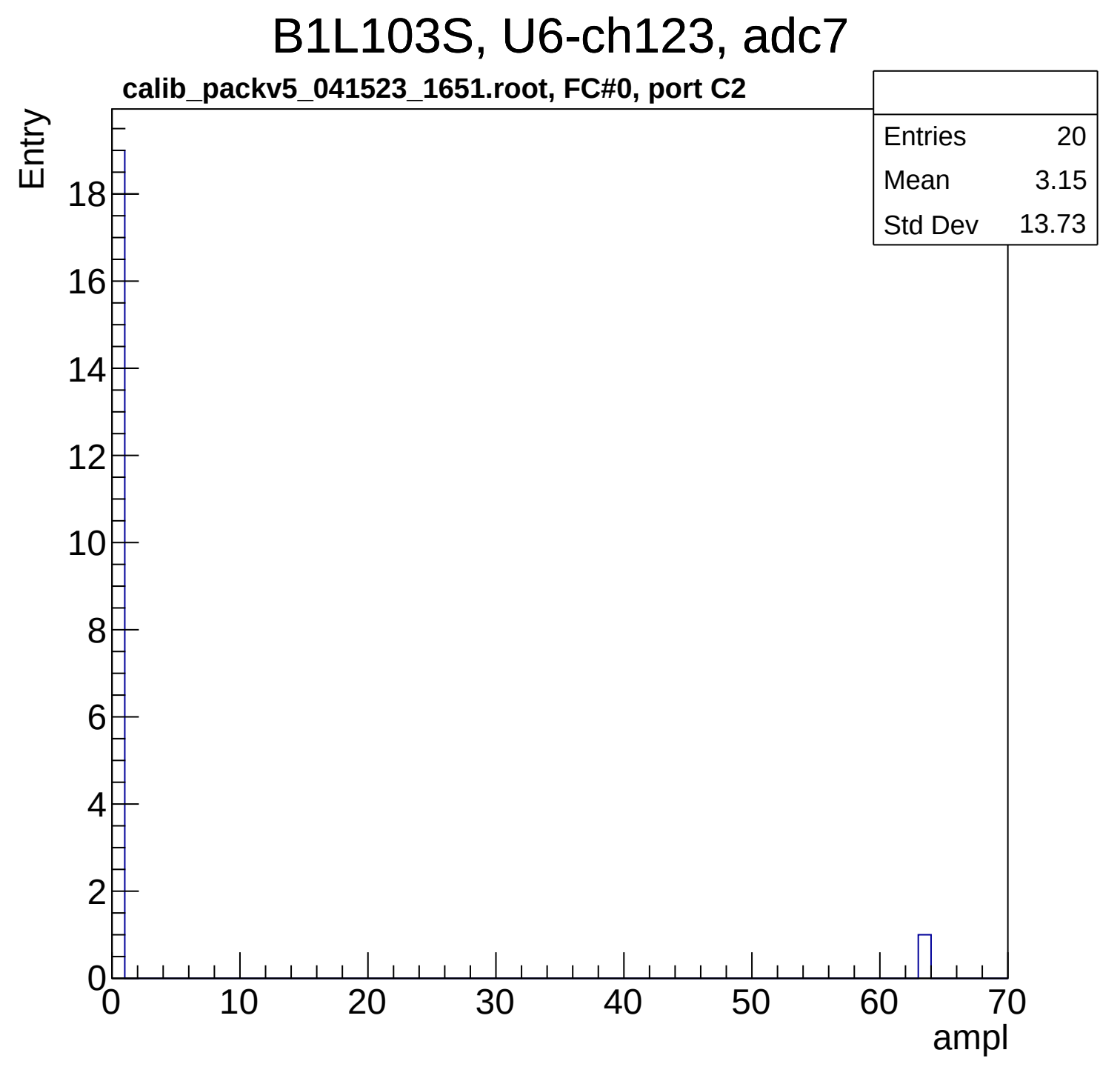
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U6-ch123, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
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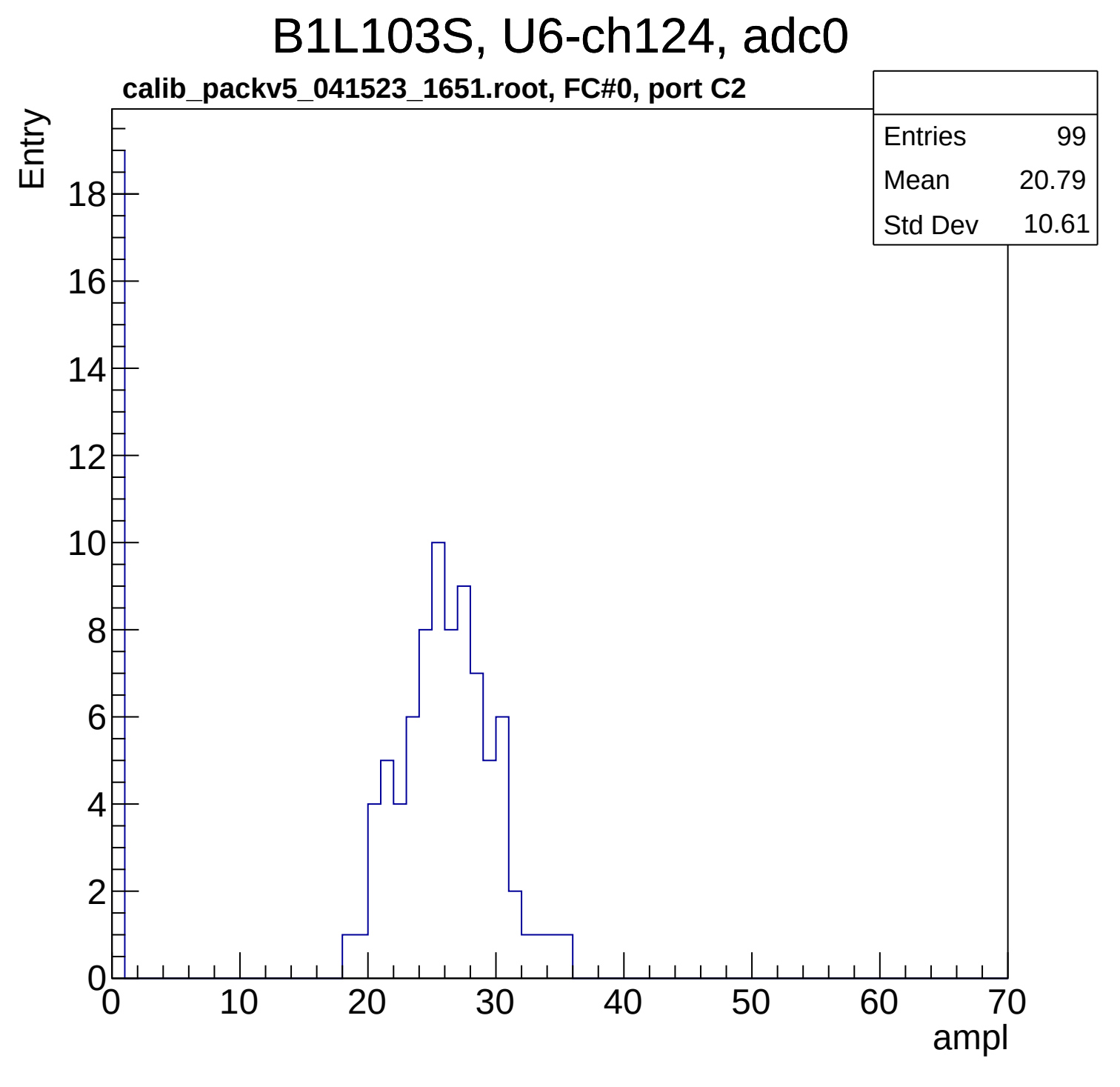
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch124, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 20.79
Std Dev 10.61
Entry
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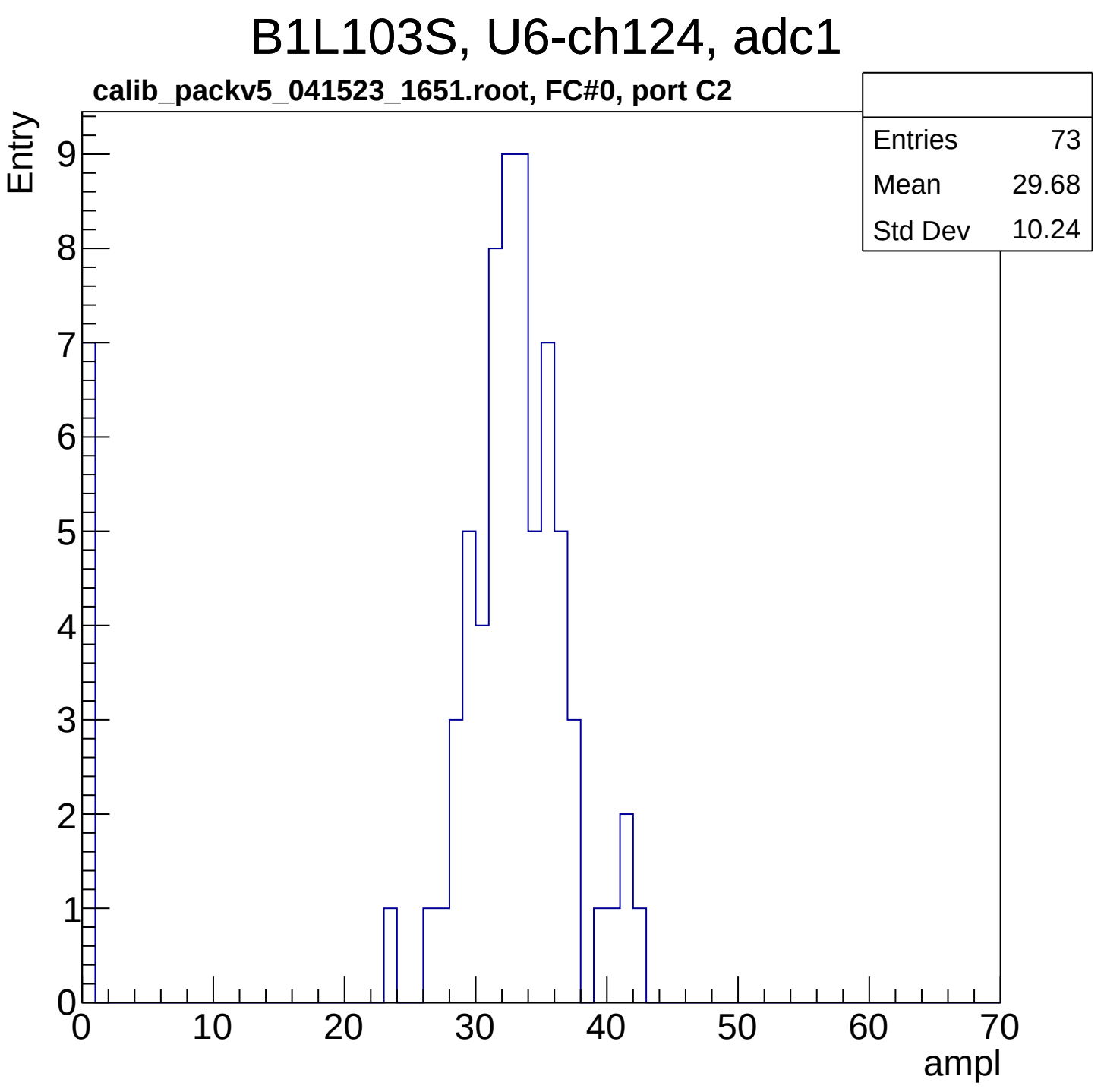
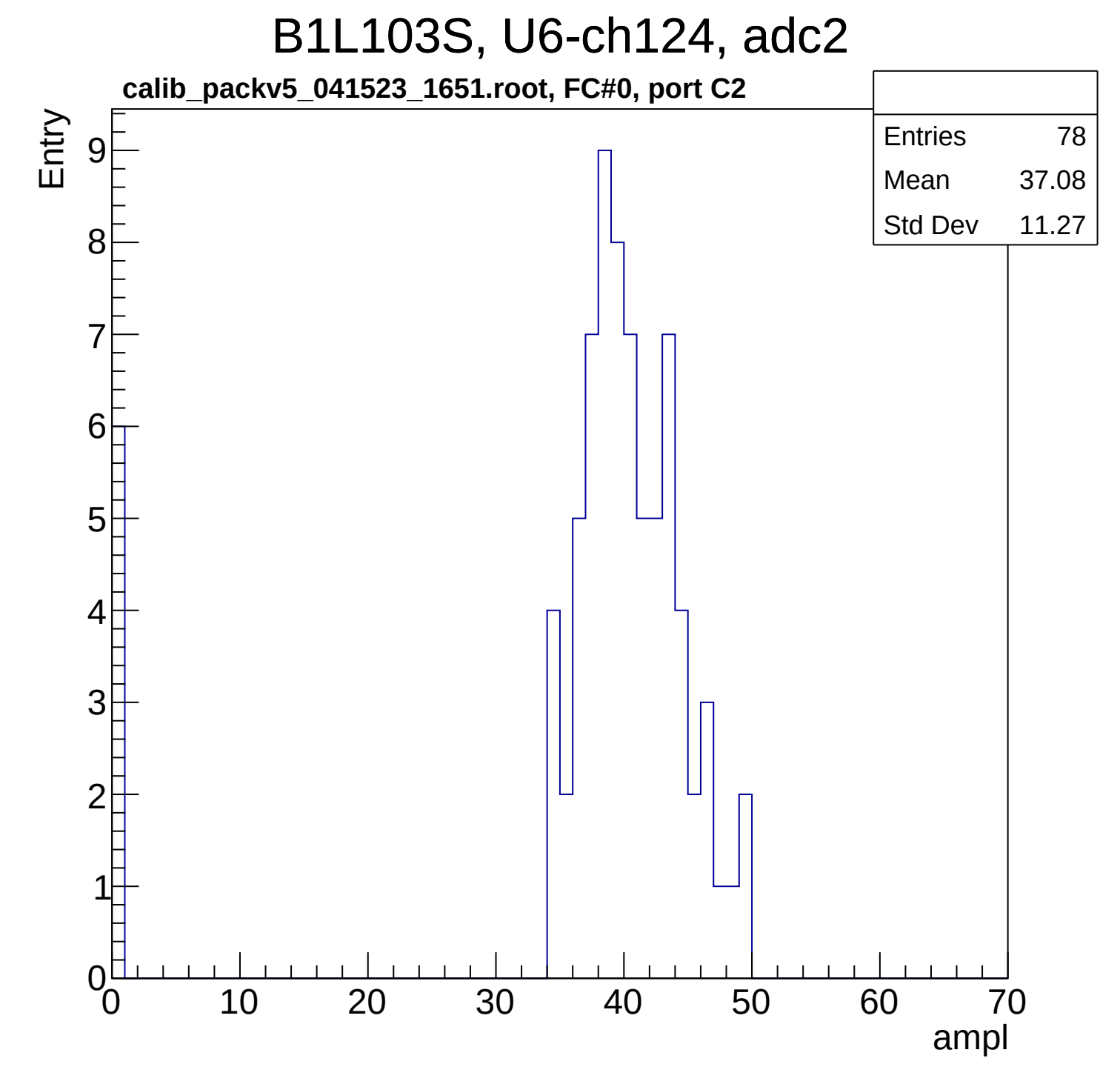
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch124, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 29.68
Std Dev 10.24
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch124, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 37.08
Std Dev 11.27
Entry
ampl
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3
4
5
6
7
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0
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60
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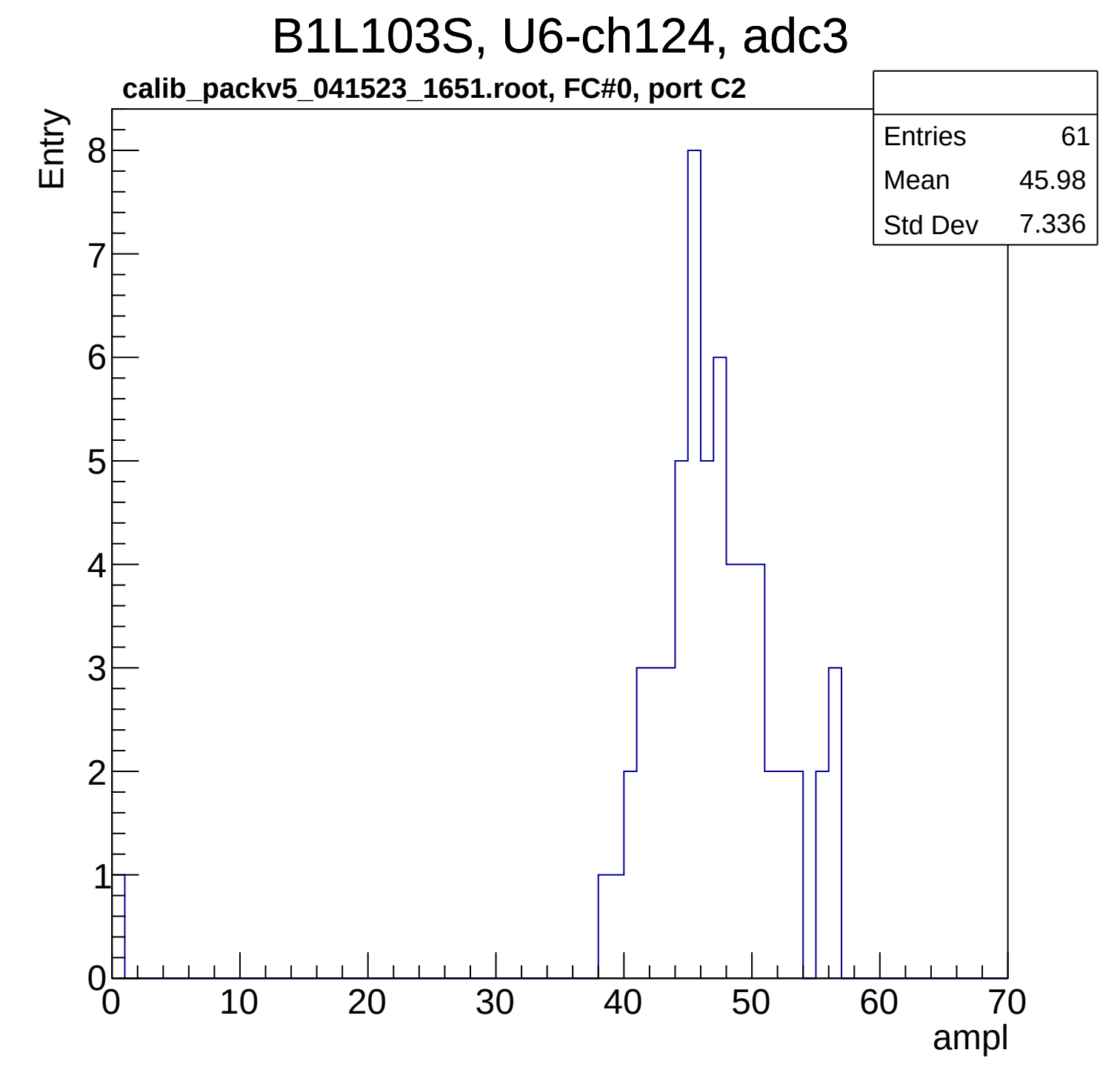
B1L103S, U6-ch124, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 45.98
Std Dev 7.336
Entry
ampl
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2
3
4
5
6
7
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0
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40
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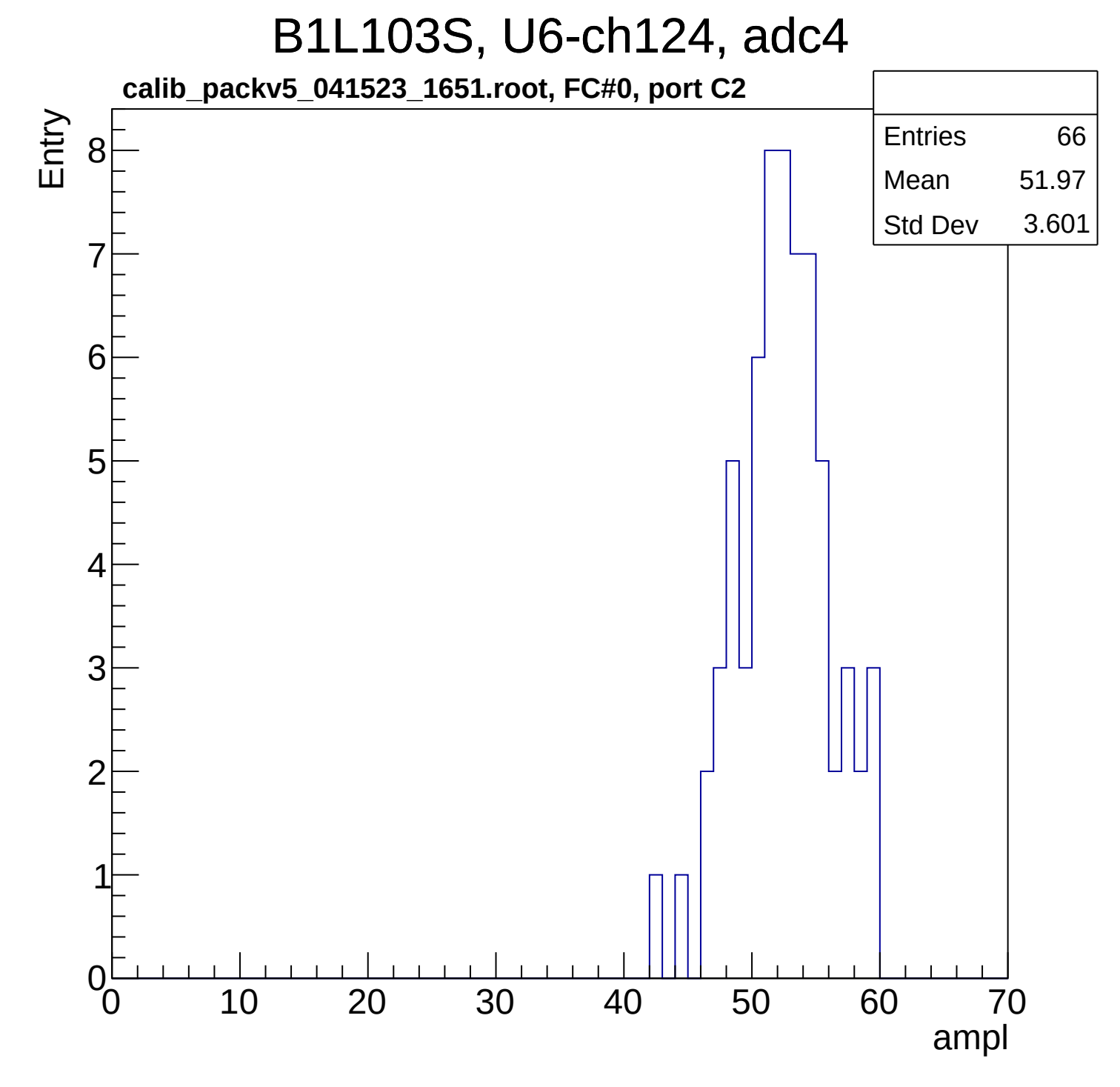
B1L103S, U6-ch124, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 51.97
Std Dev 3.601
Entry
ampl
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2
3
4
5
6
7
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0
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40
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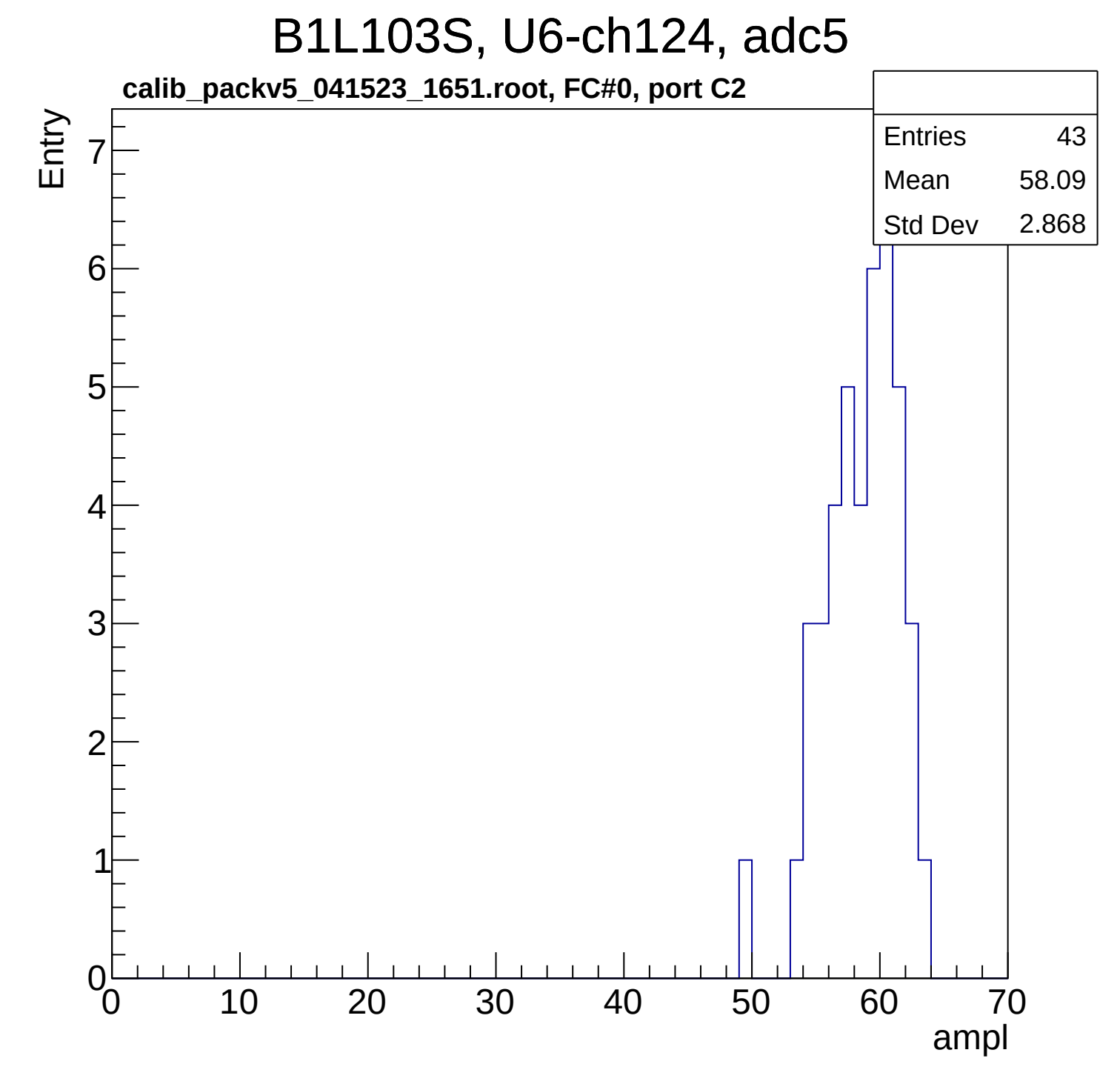
B1L103S, U6-ch124, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 58.09
Std Dev 2.868
Entry
ampl
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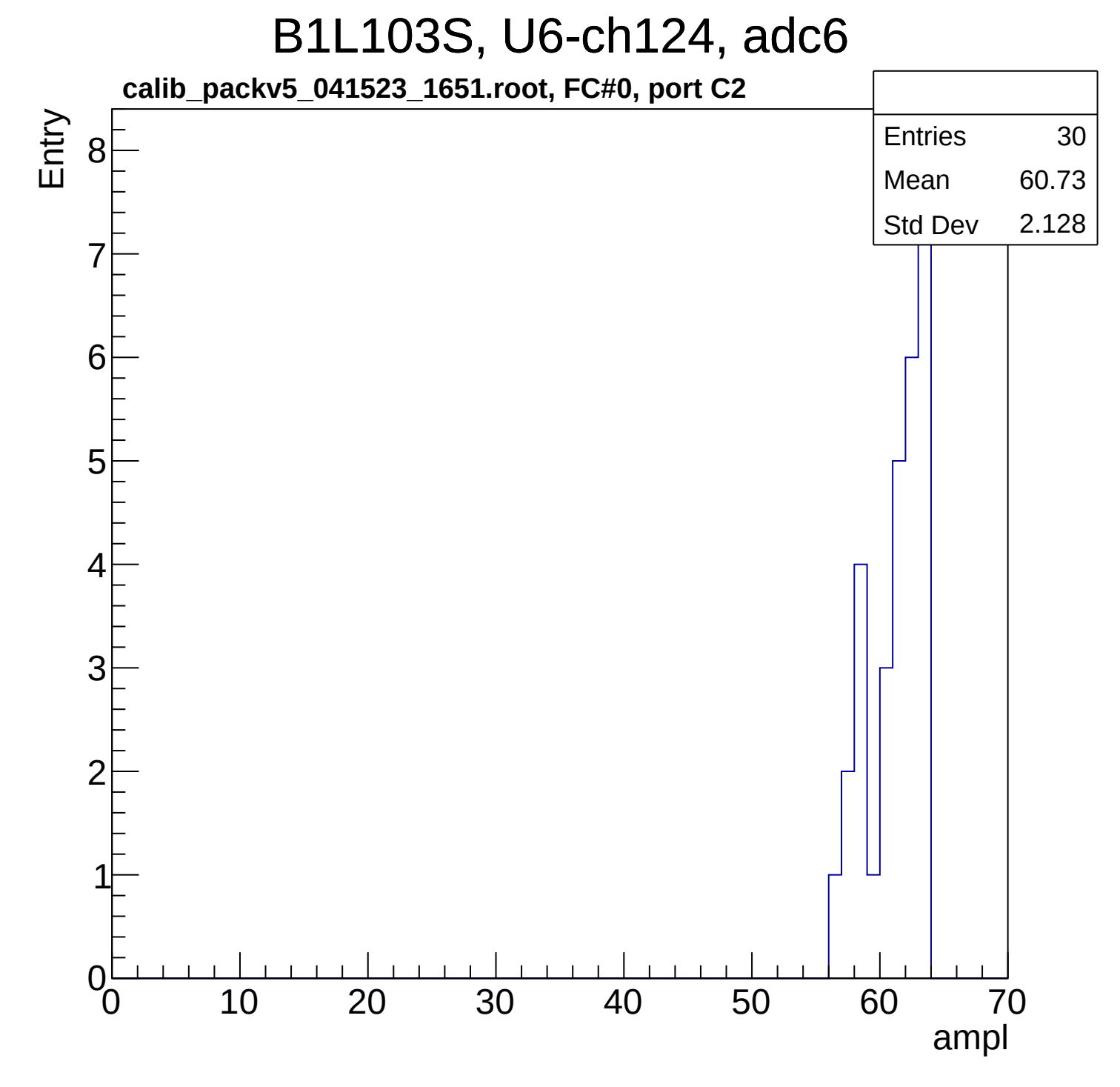
B1L103S, U6-ch124, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 60.73
Std Dev 2.128
Entry
ampl
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1
2
3
4
5
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7
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0
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40
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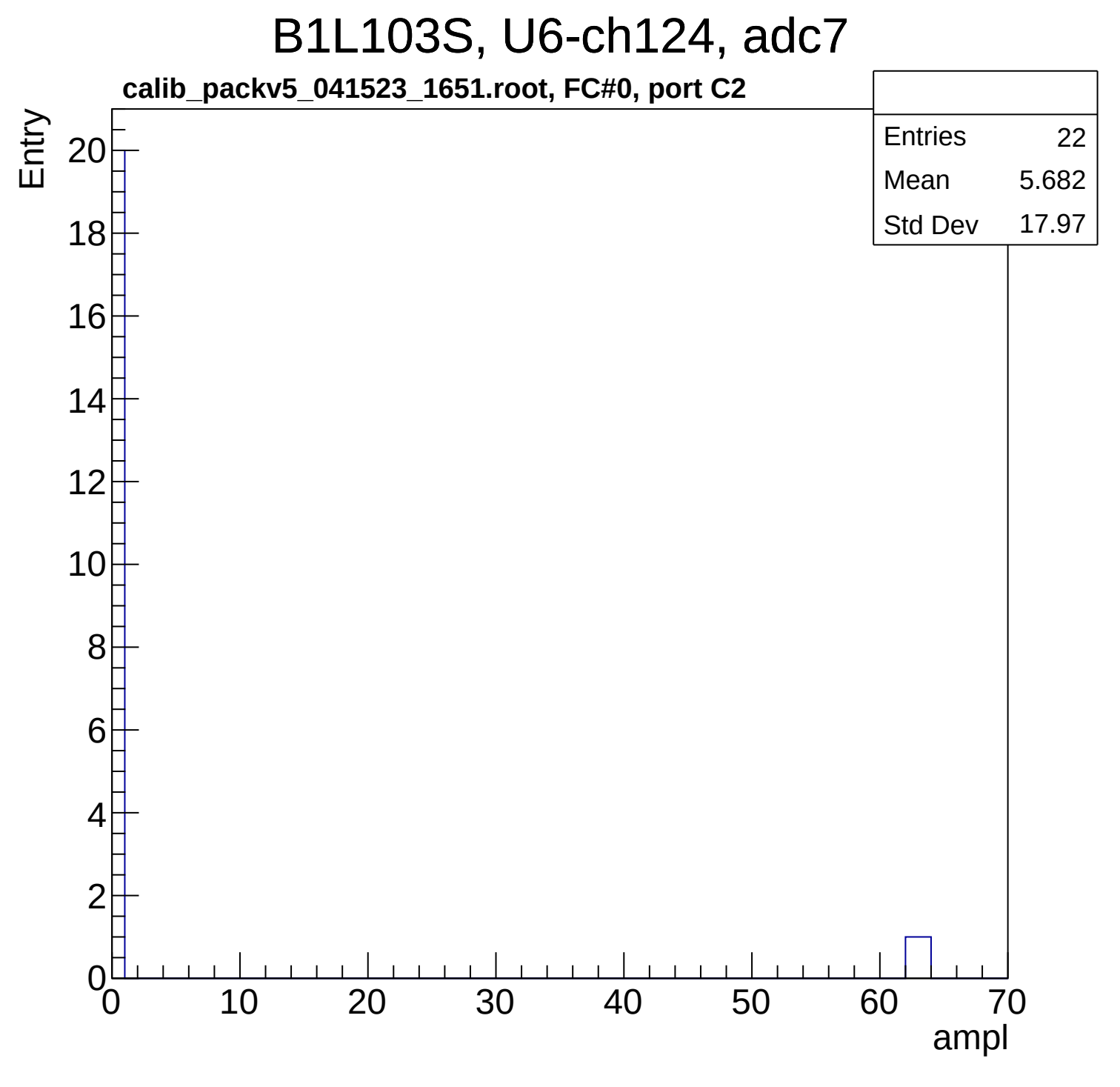
B1L103S, U6-ch124, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 5.682
Std Dev 17.97
Entry
0
2
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8
10
12
14
16
18
20
0
10
20
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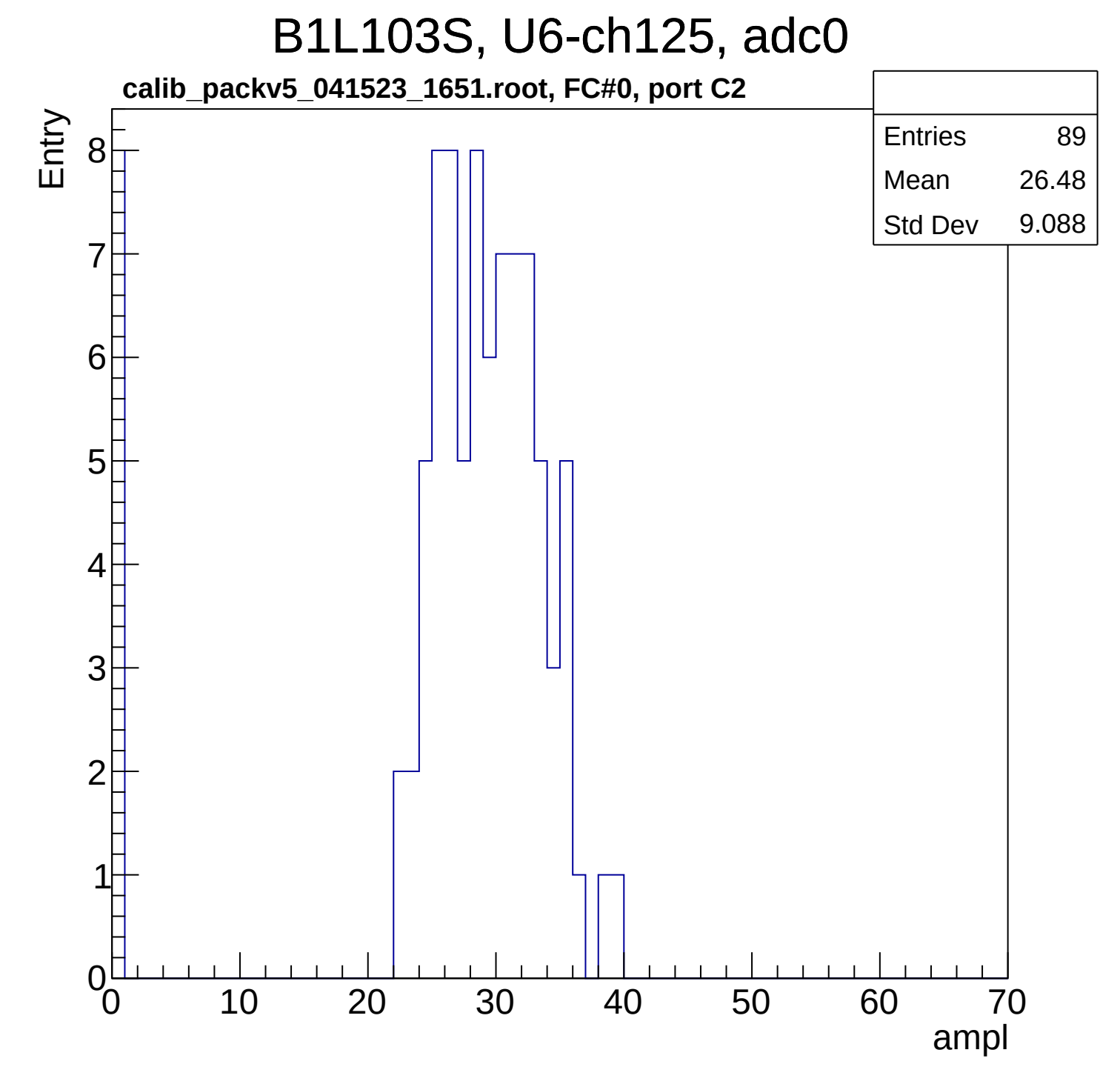
40
50
60
70
ampl


B1L103S, U6-ch125, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 26.48
Std Dev 9.088
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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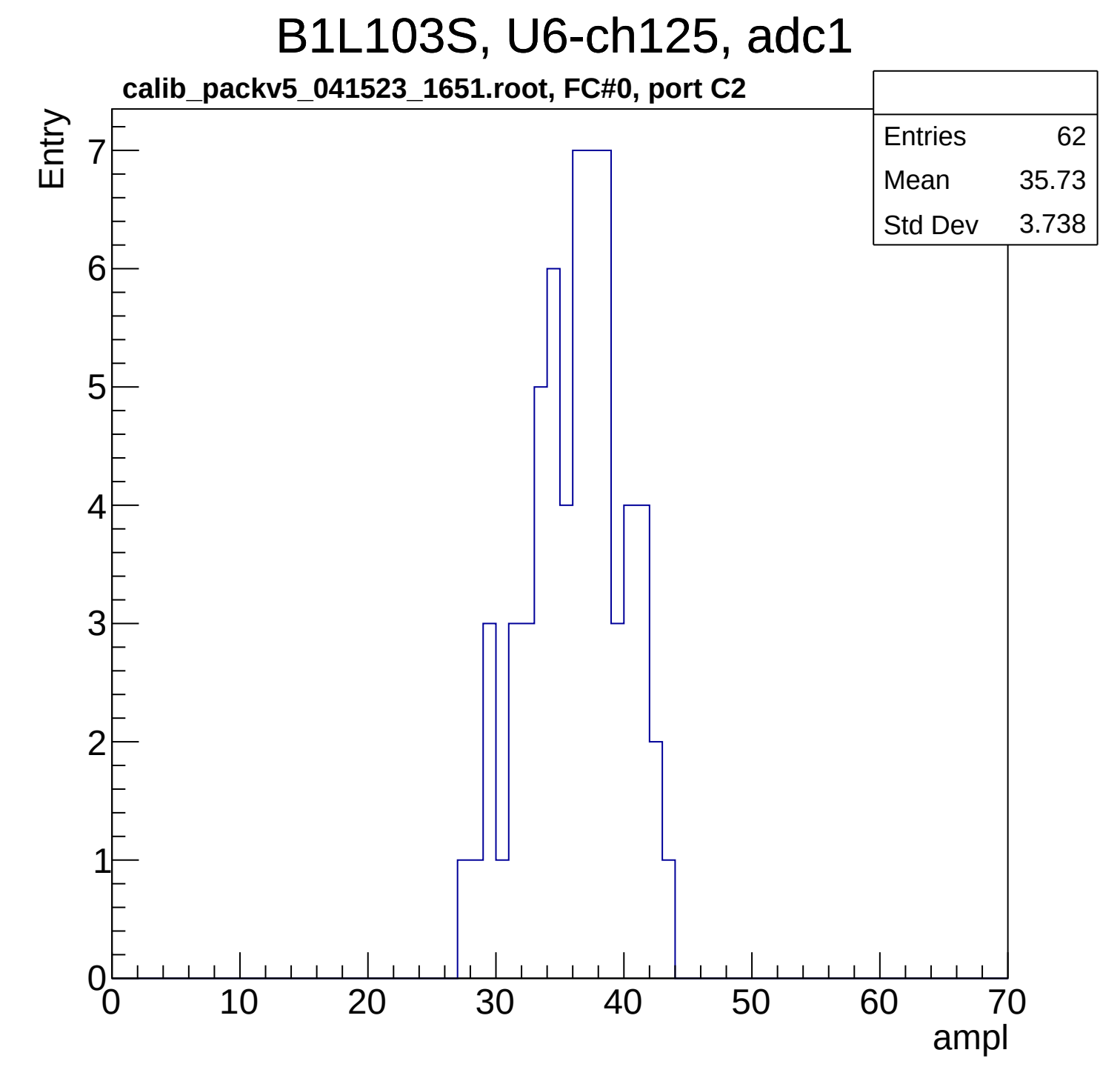
B1L103S, U6-ch125, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 35.73
Std Dev 3.738
Entry
ampl
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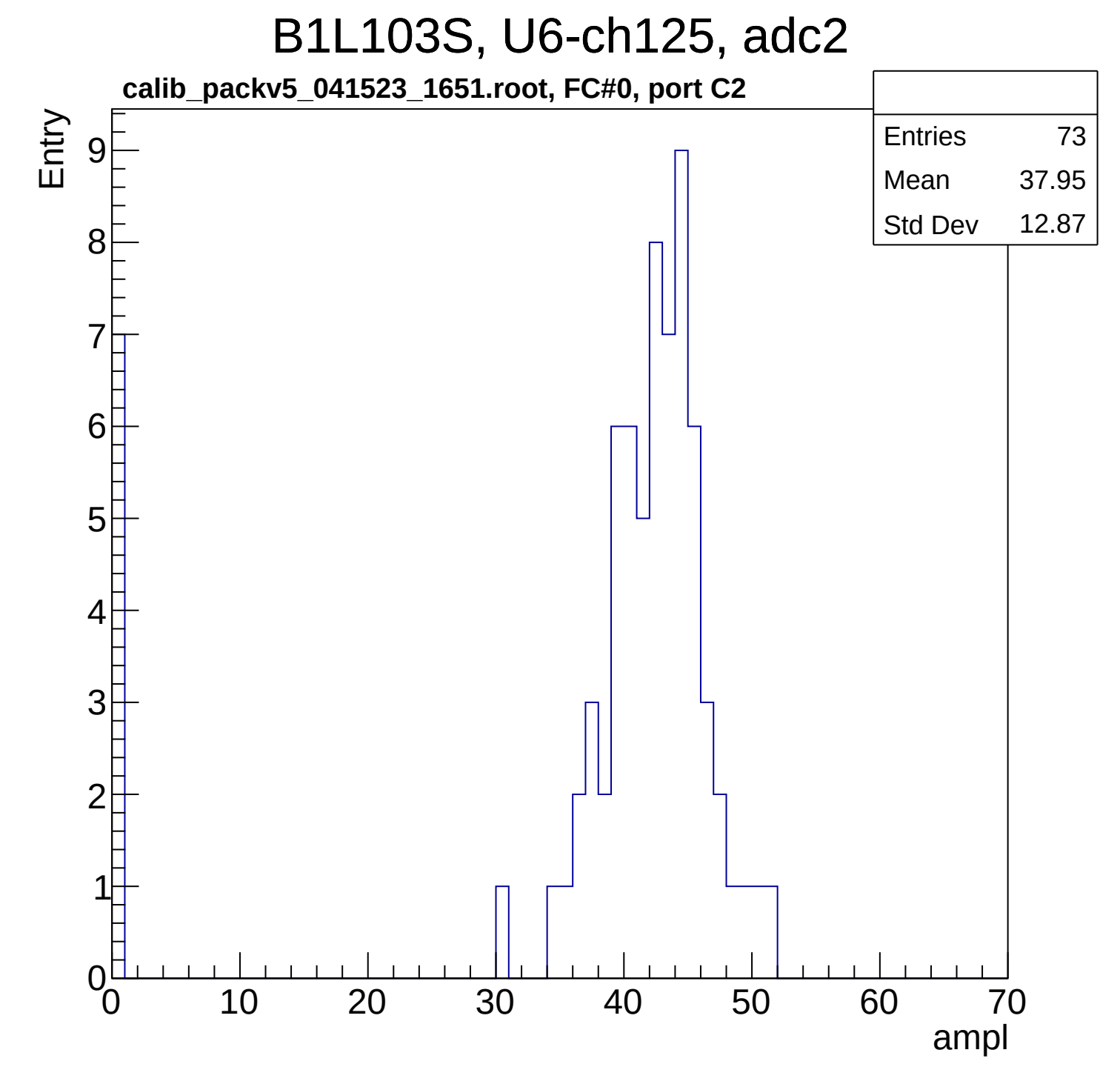
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U6-ch125, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 37.95
Std Dev 12.87
Entry
ampl
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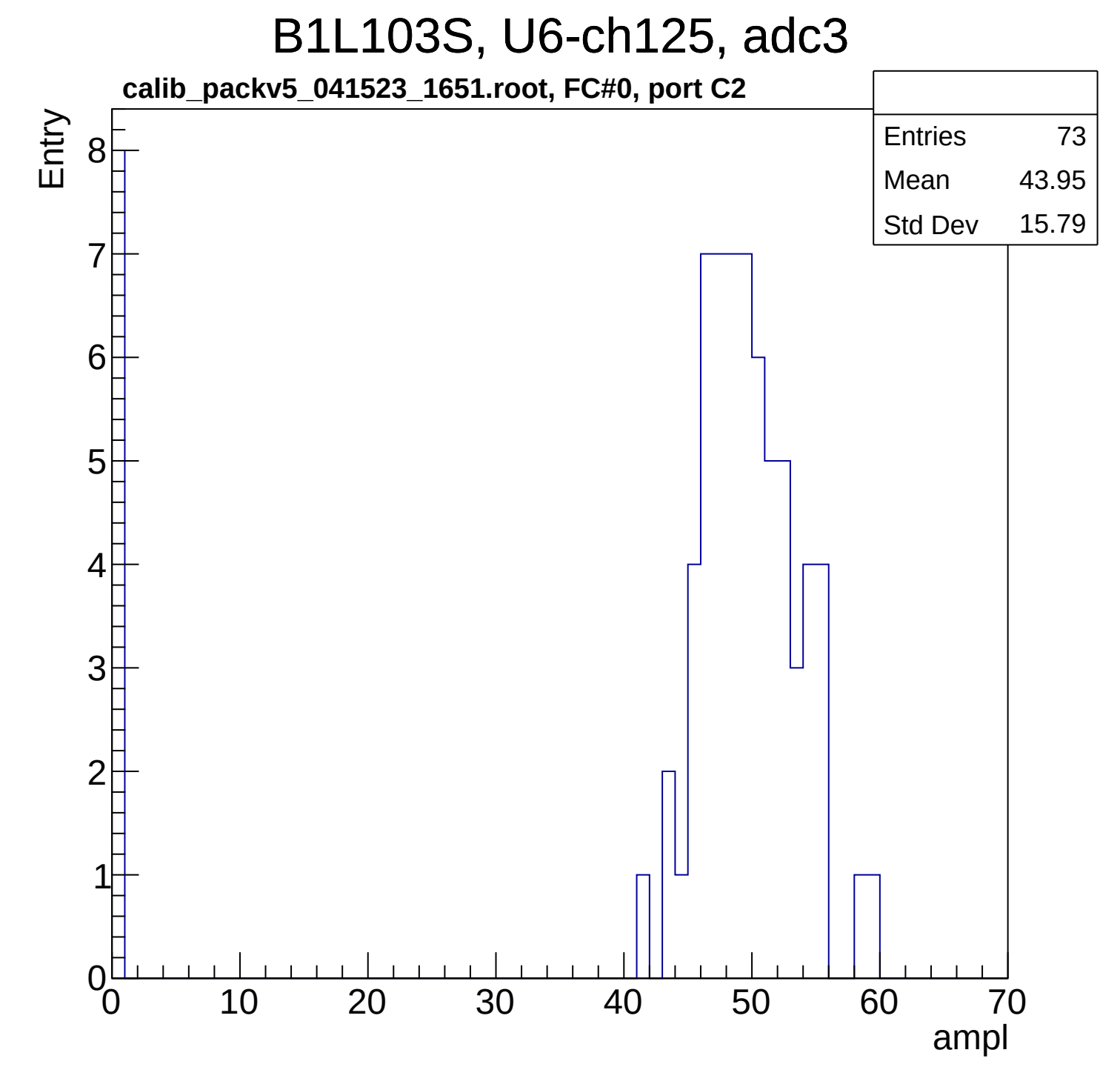
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch125, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 43.95
Std Dev 15.79
Entry
ampl
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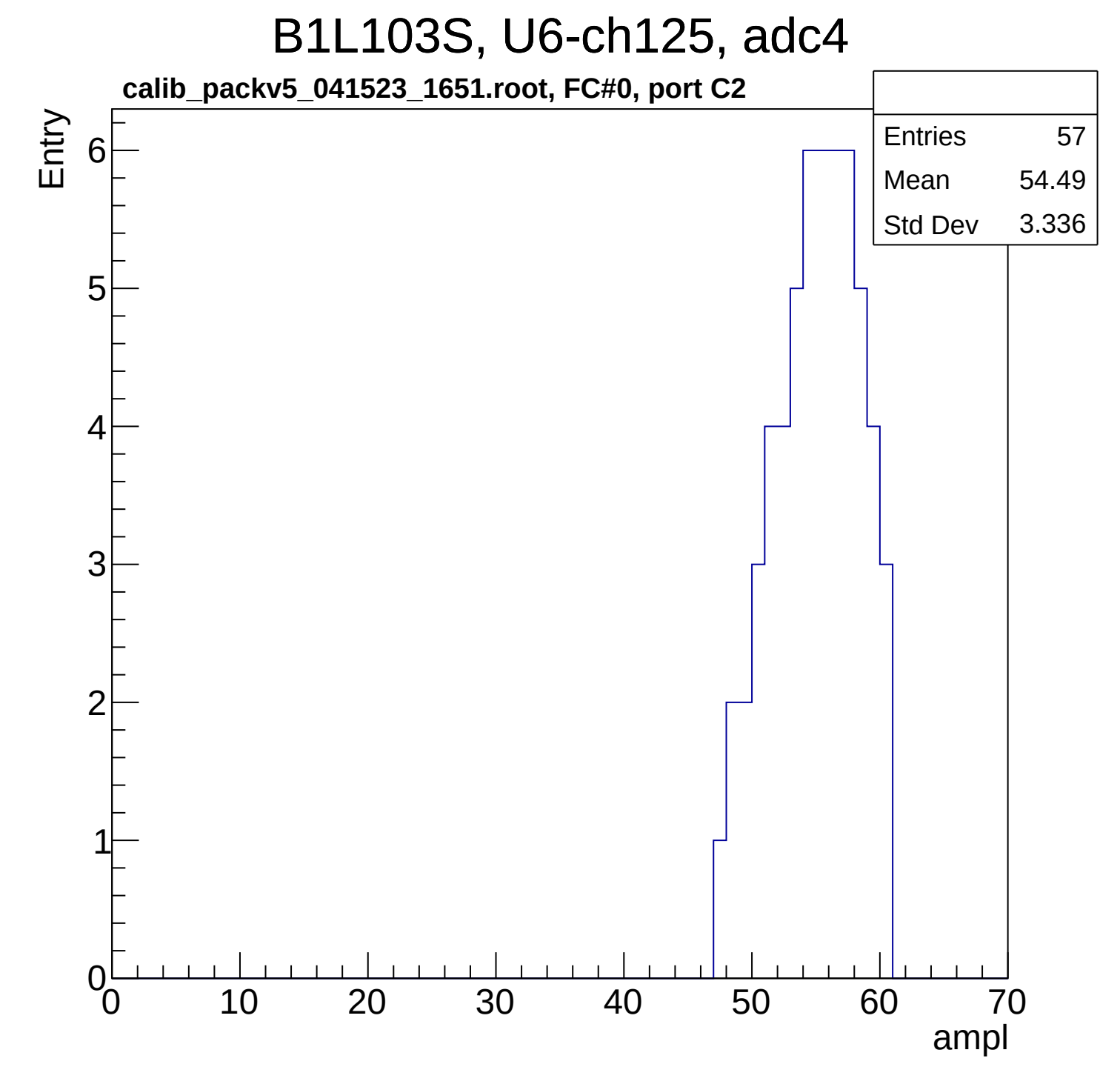
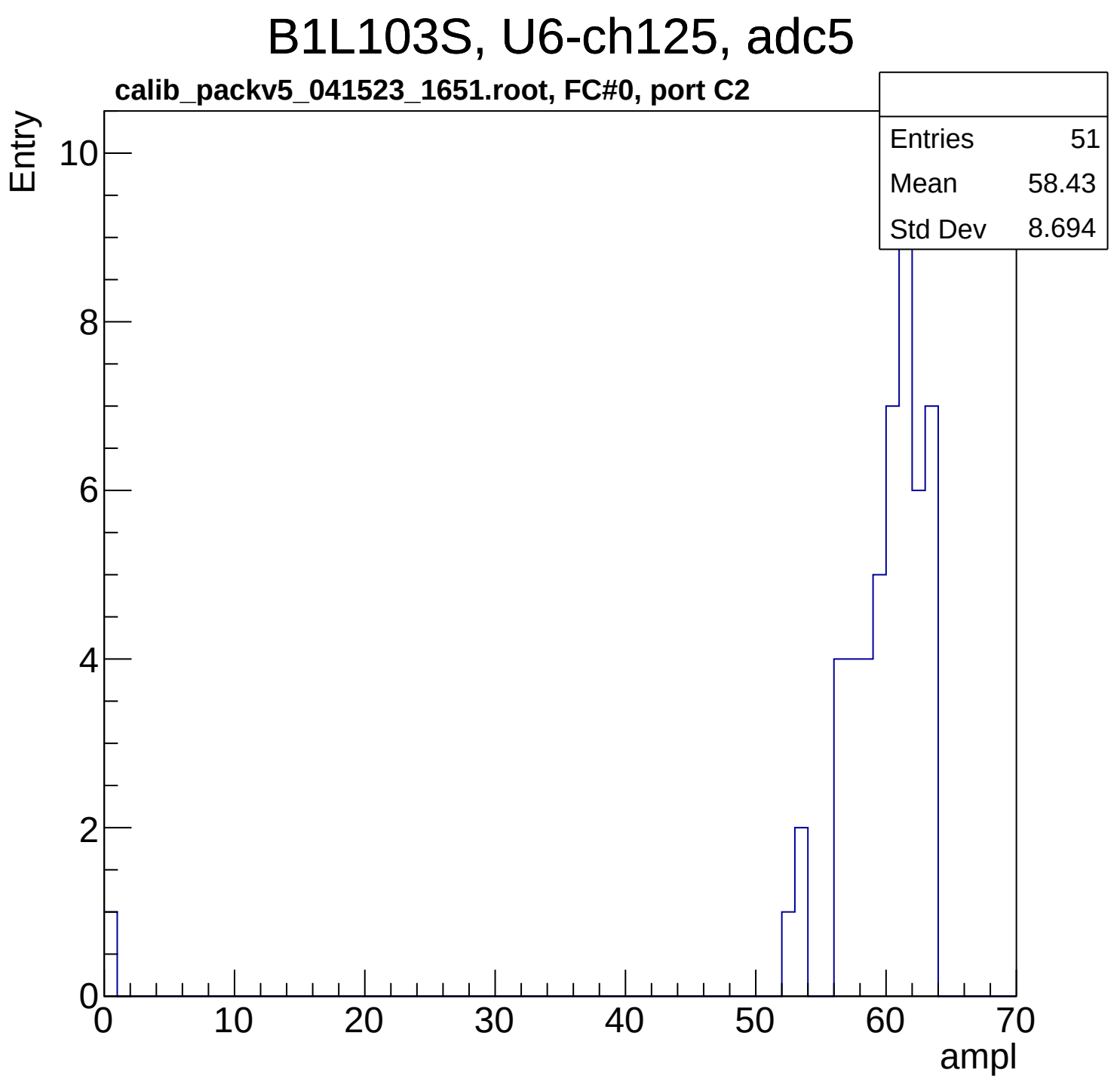
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch125, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 54.49
Std Dev 3.336
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U6-ch125, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 58.43
Std Dev 8.694
Entry
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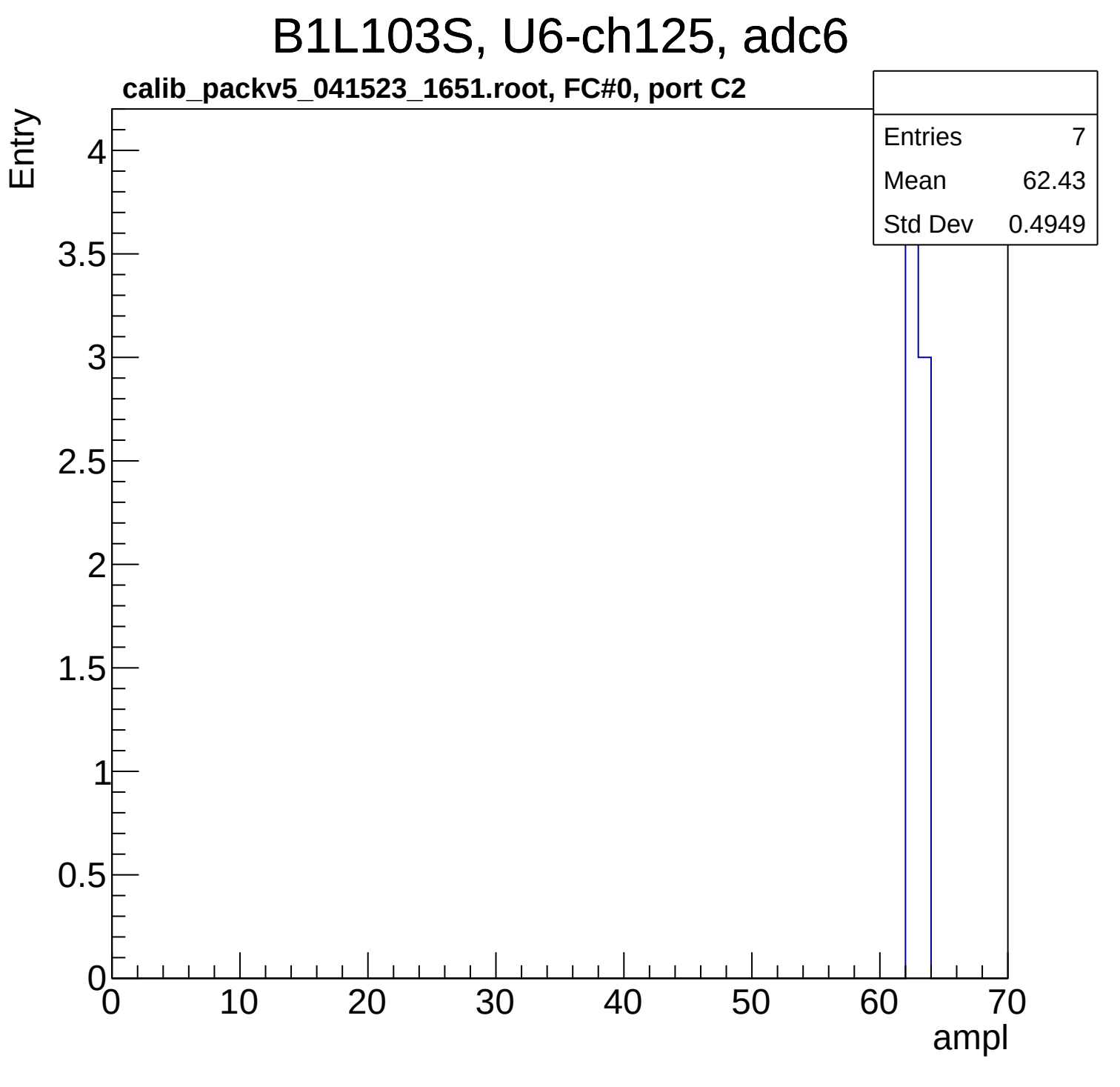
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch125, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 62.43
Std Dev 0.4949
Entry
ampl
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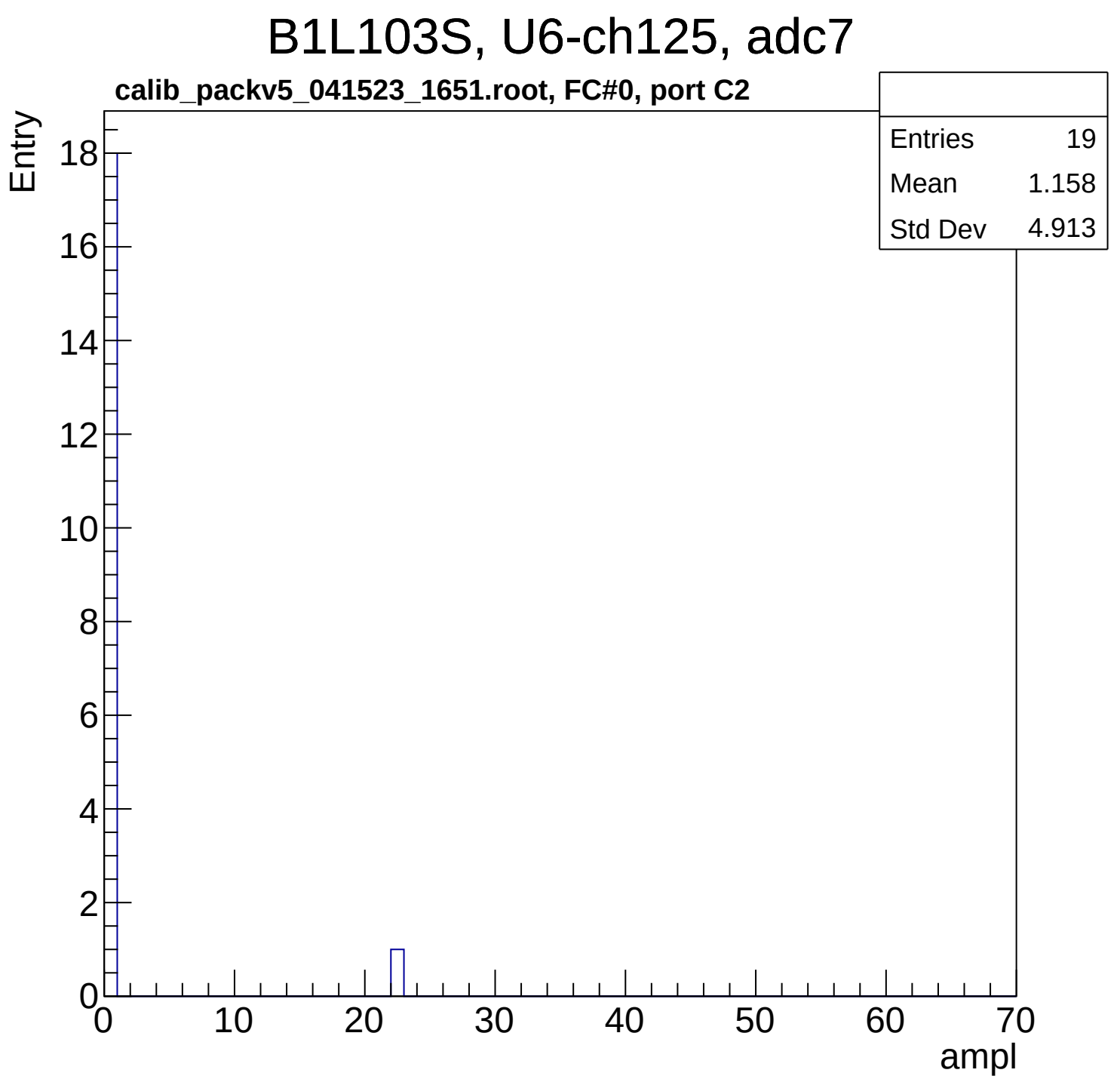
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U6-ch125, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.158
Std Dev 4.913
Entry
0
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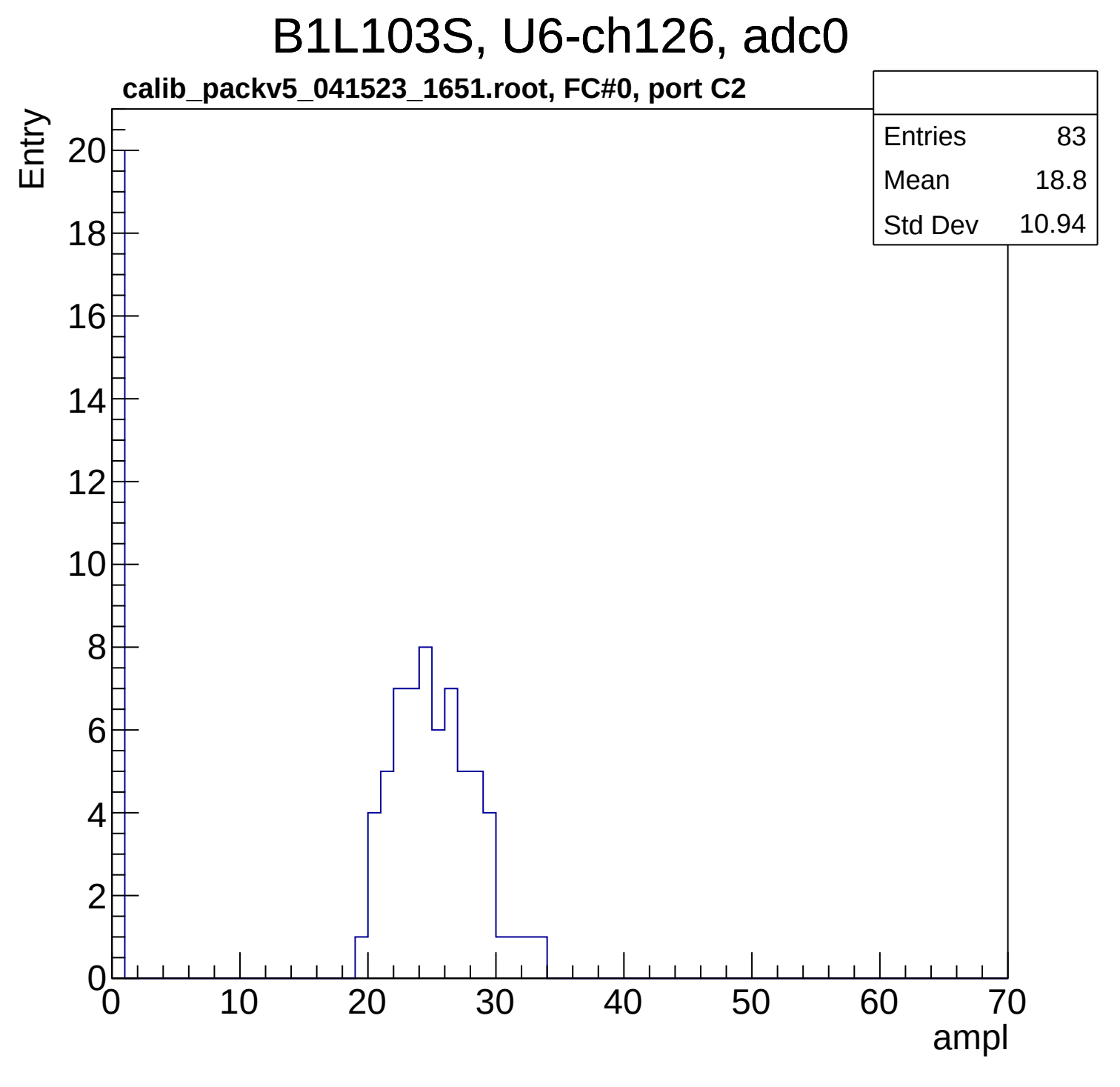
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch126, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 18.8
Std Dev 10.94
Entry
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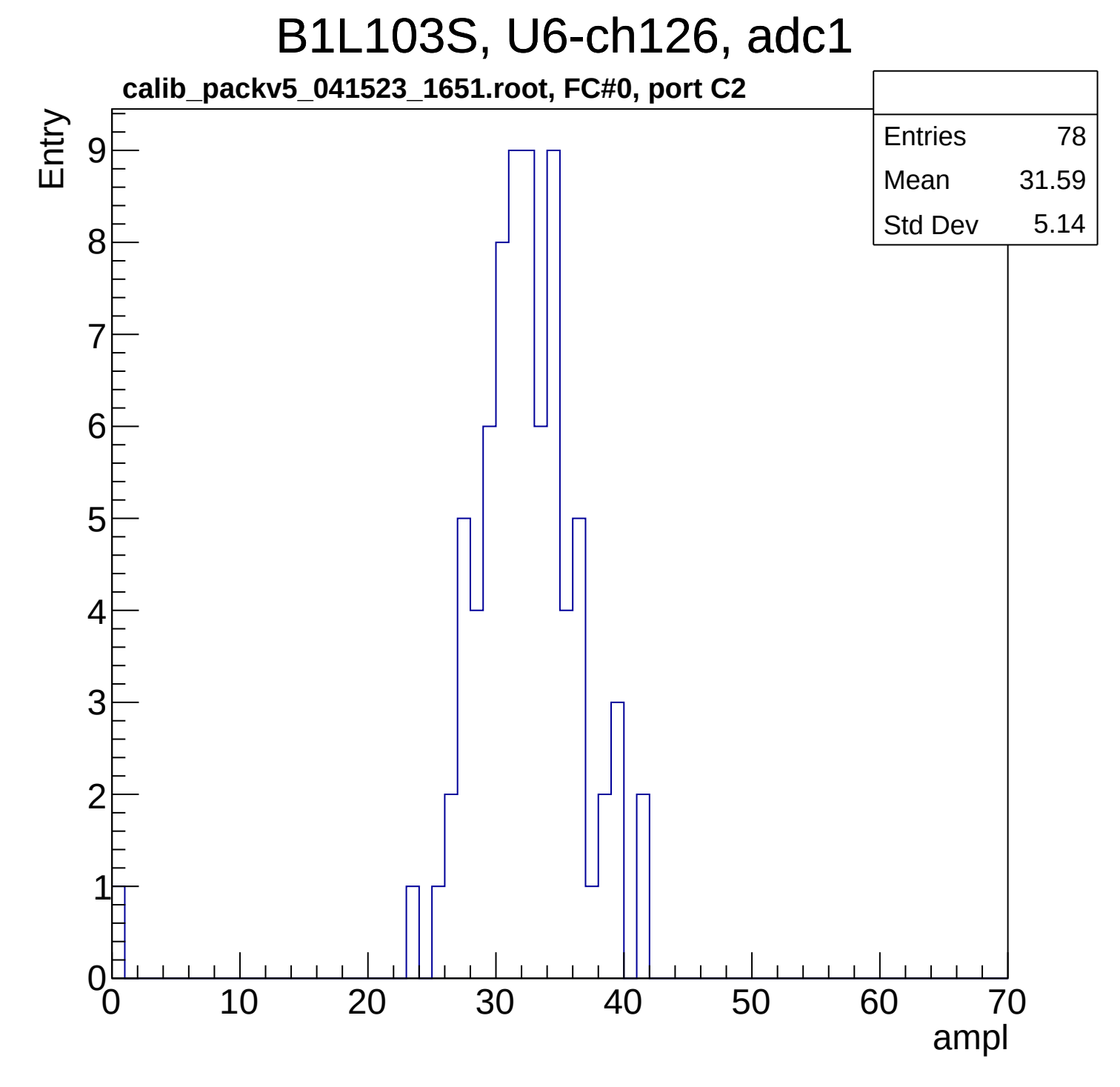
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch126, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 31.59
Std Dev 5.14
Entry
ampl
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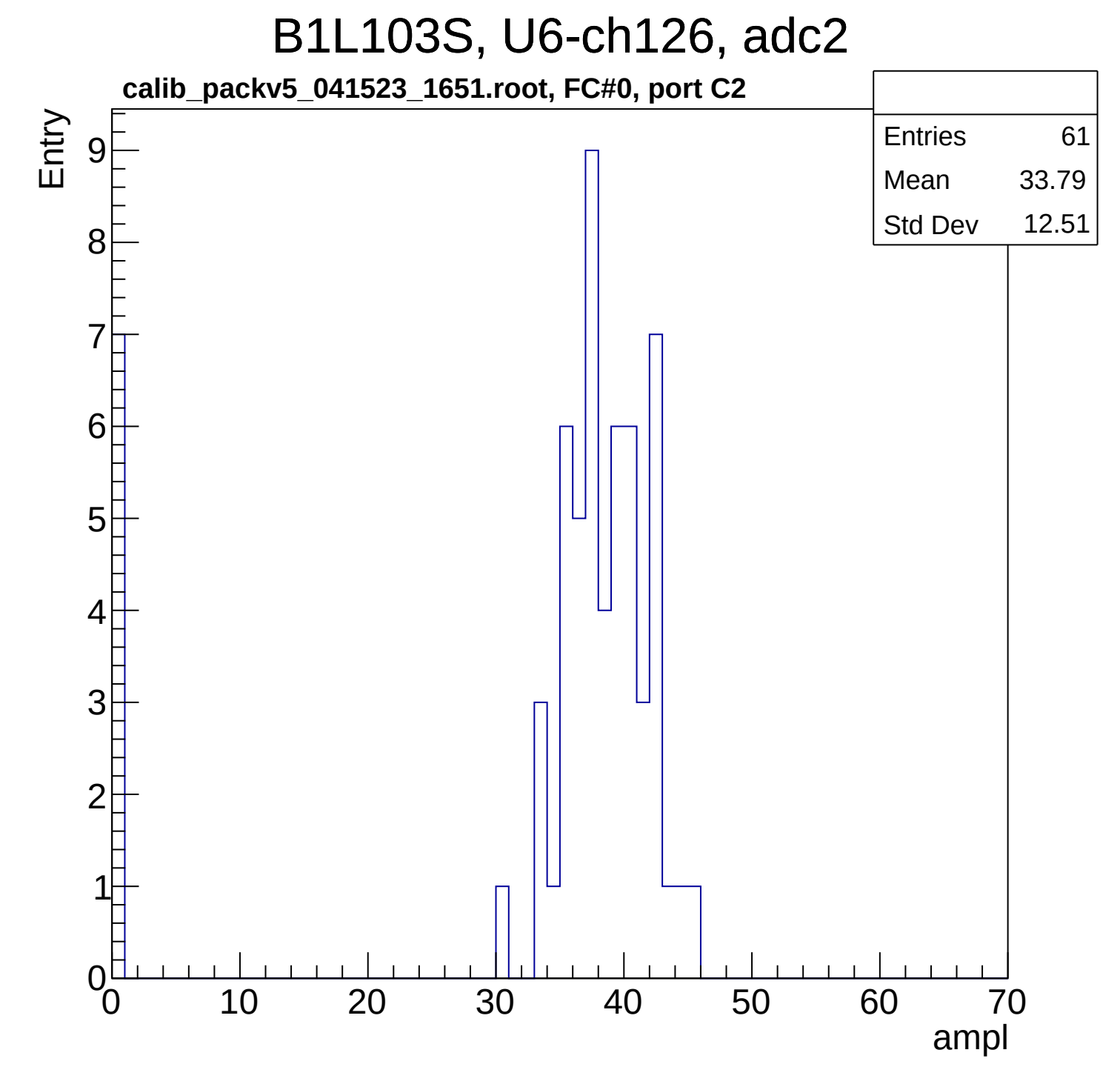
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch126, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 33.79
Std Dev 12.51
Entry
ampl
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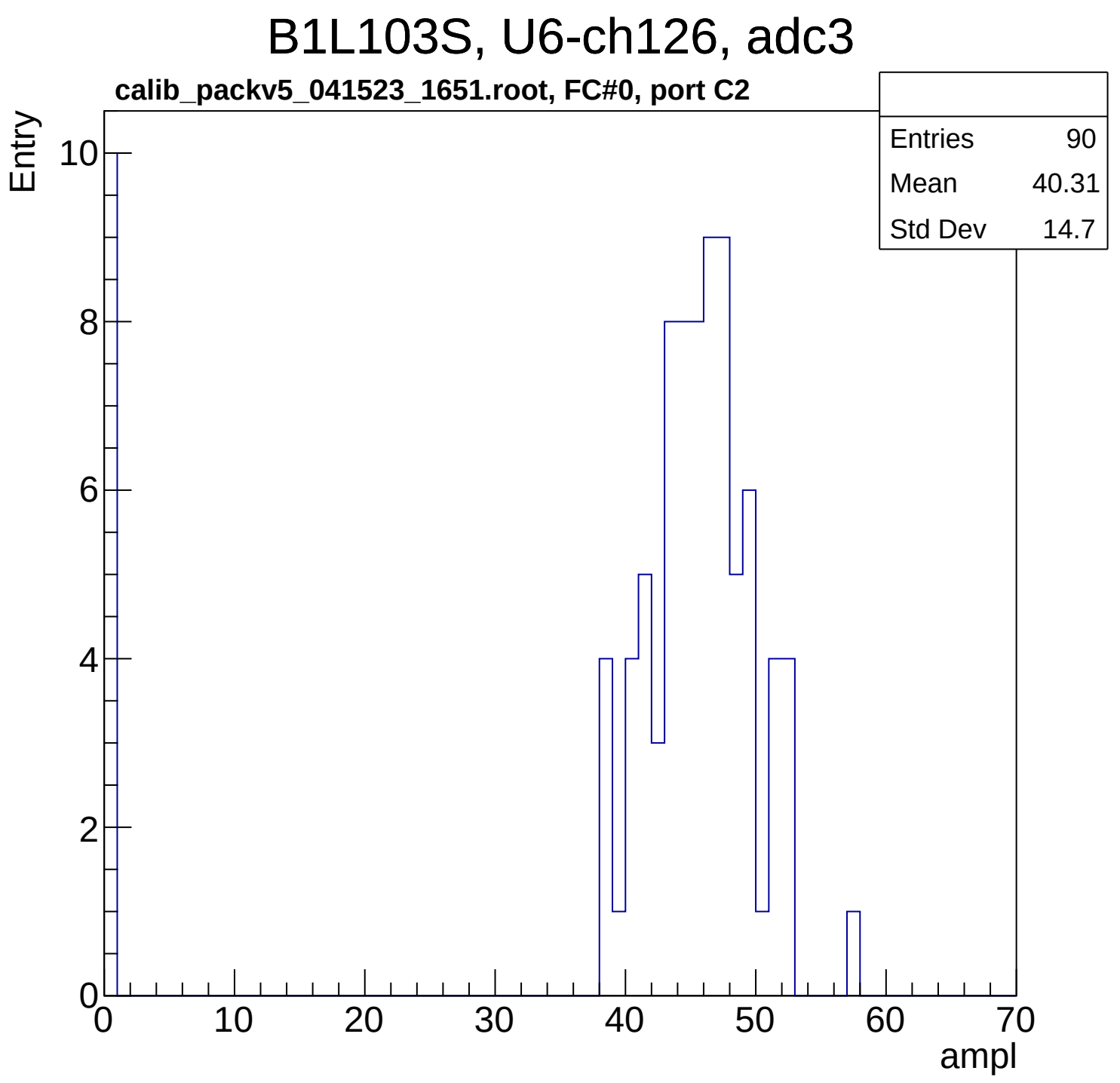
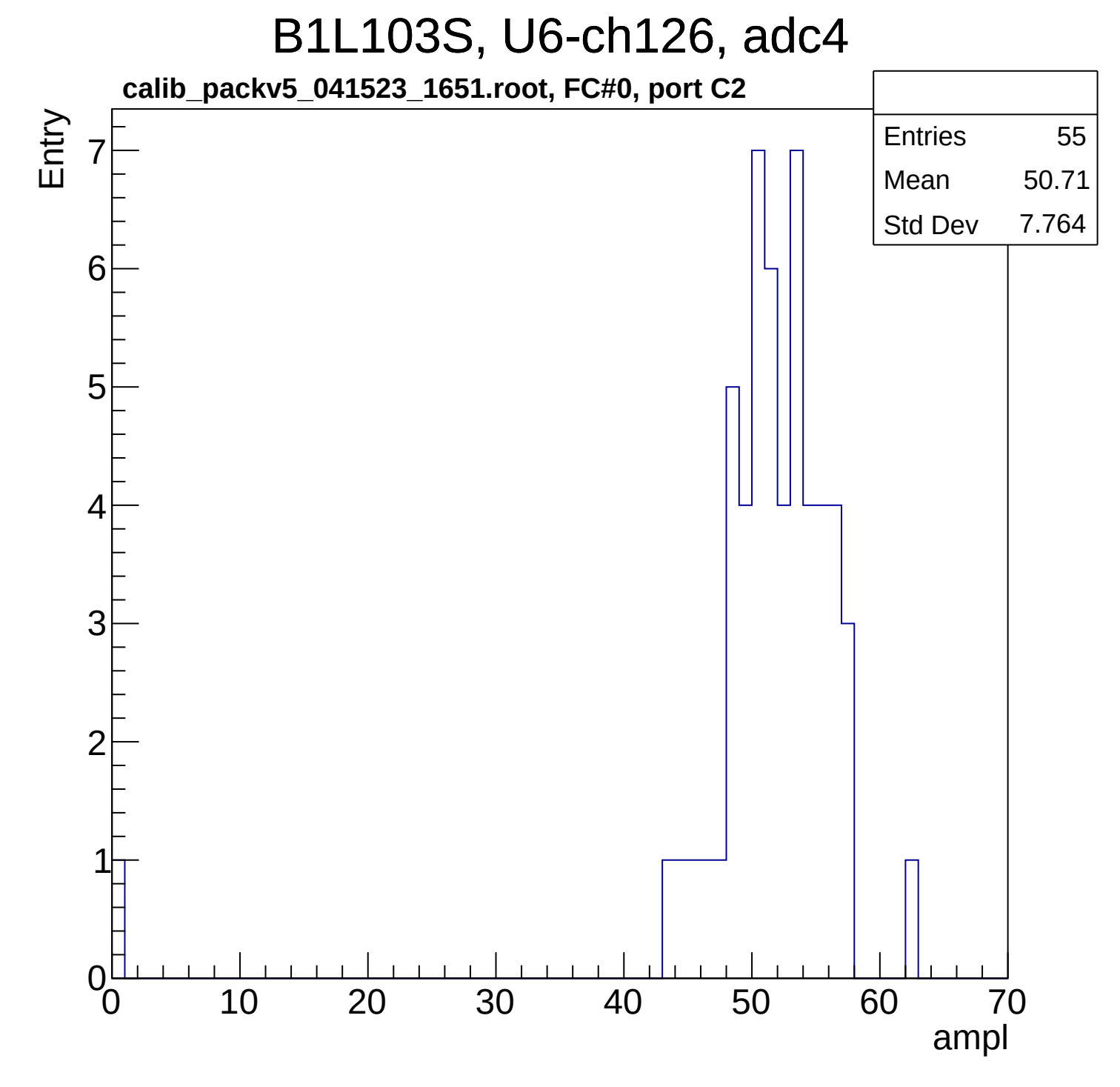
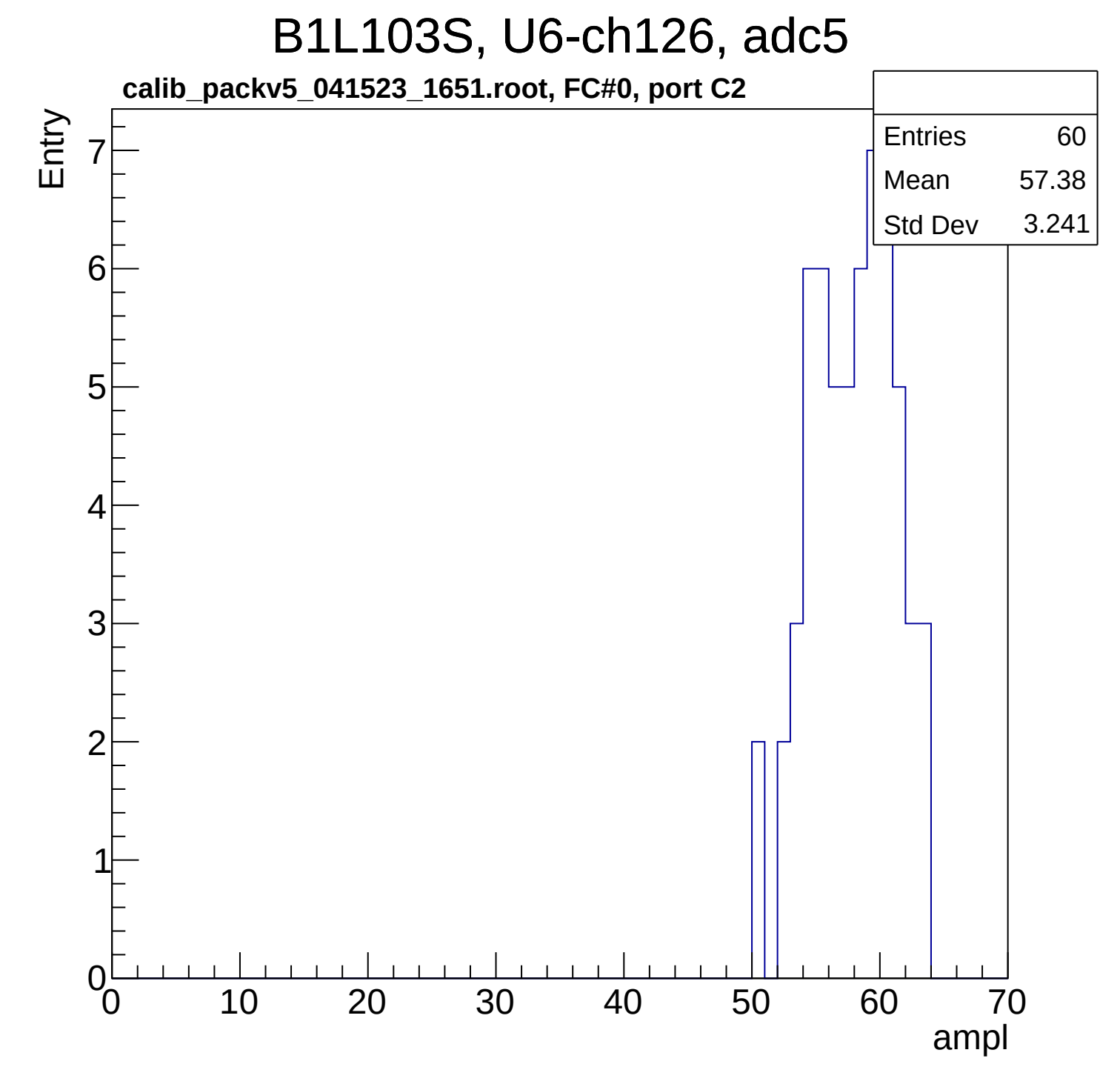
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U6-ch126, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 40.31
Std Dev 14.7
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch126, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 50.71
Std Dev 7.764
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U6-ch126, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 57.38
Std Dev 3.241
Entry
ampl
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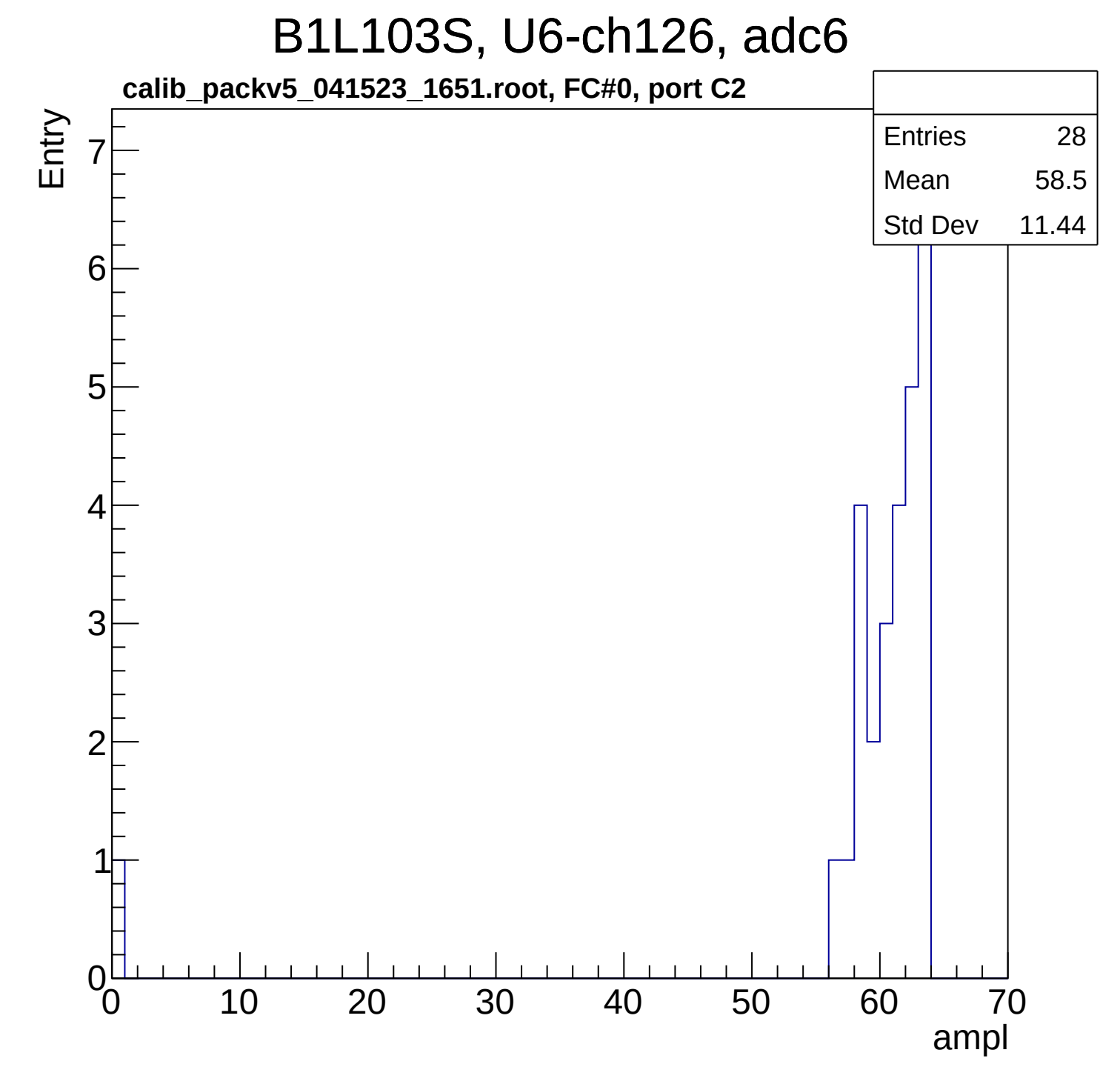
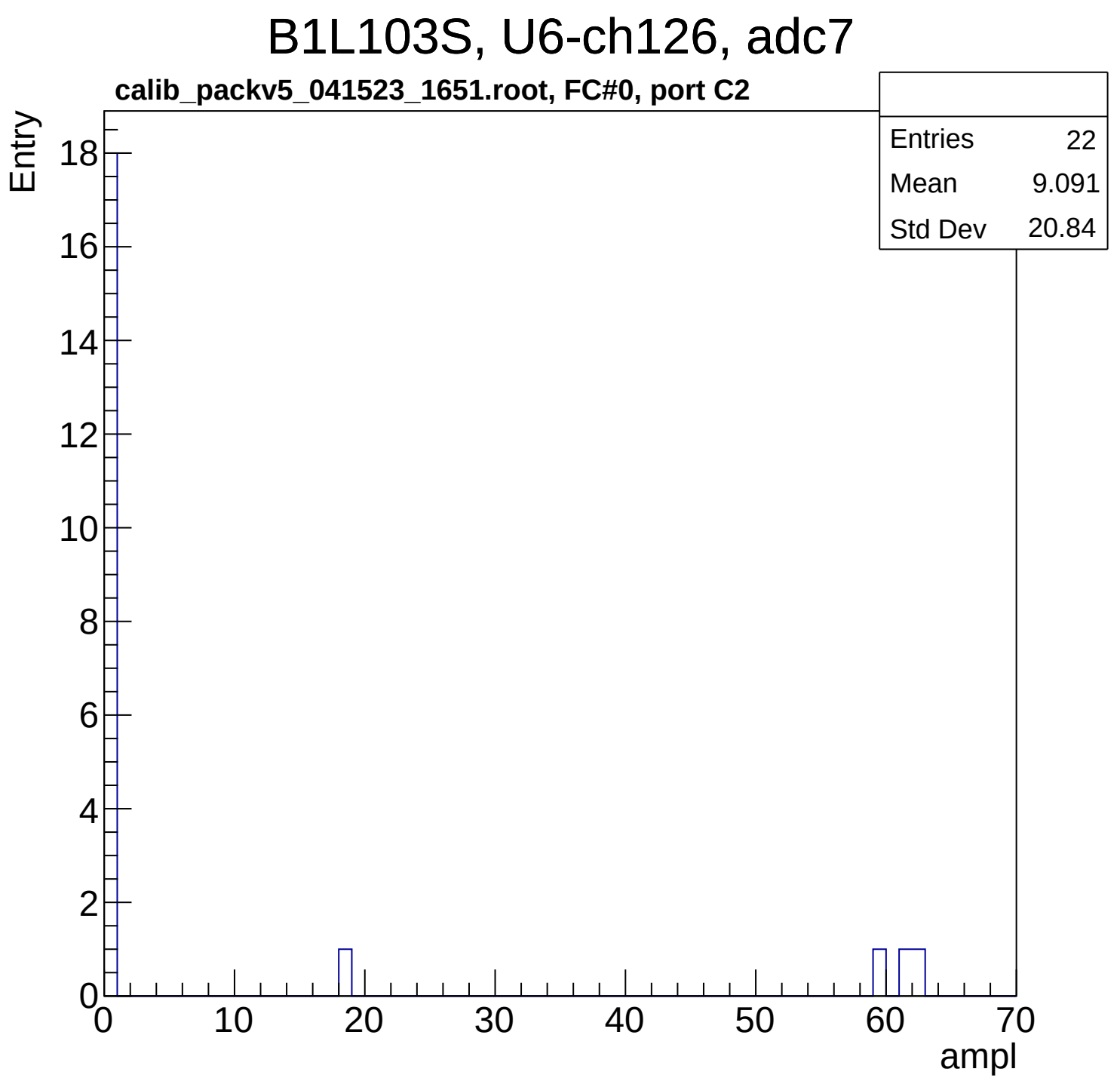
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U6-ch126, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 58.5
Std Dev 11.44
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U6-ch126, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 9.091
Std Dev 20.84
Entry
0
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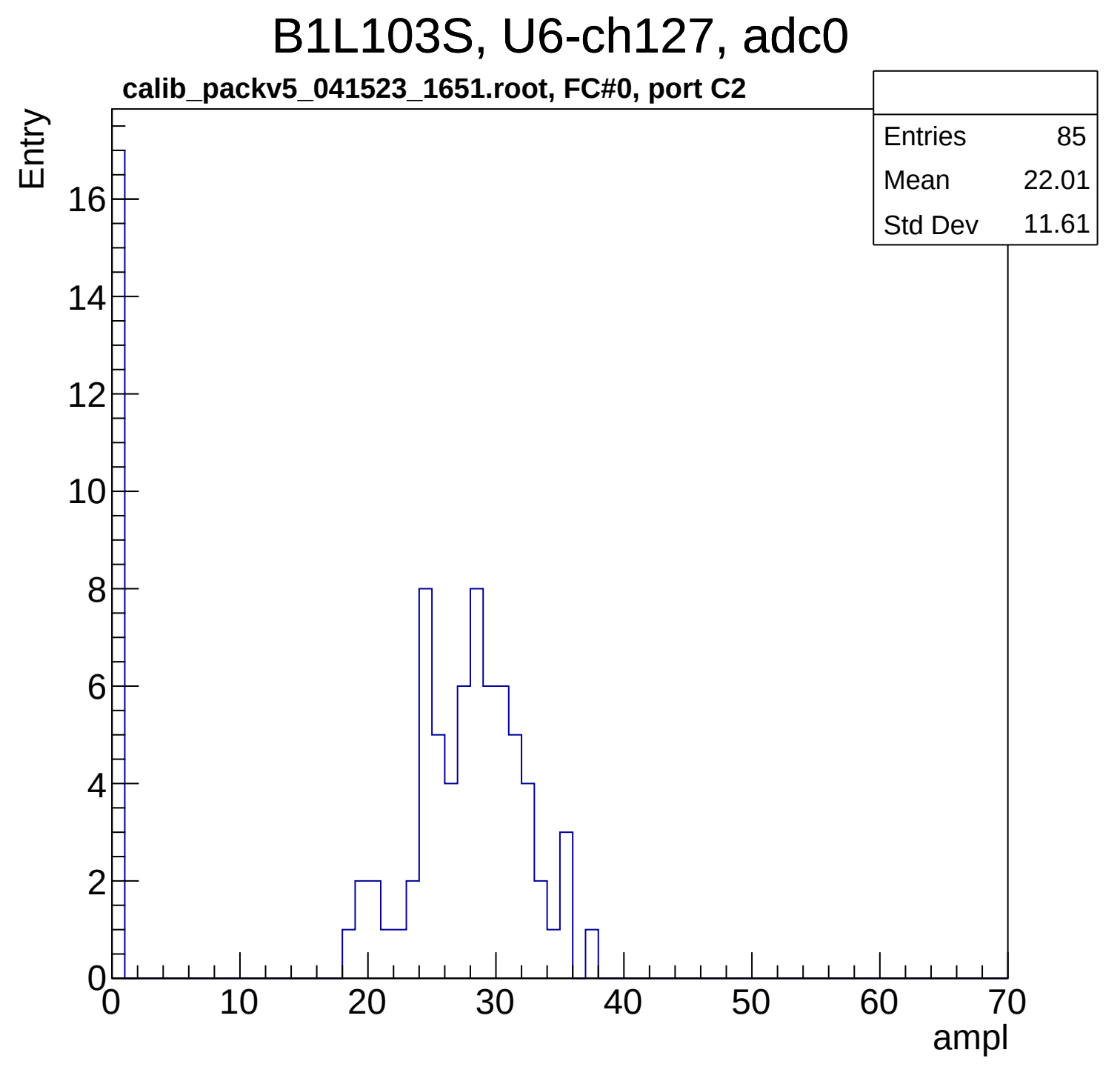
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch127, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 22.01
Std Dev 11.61
Entry
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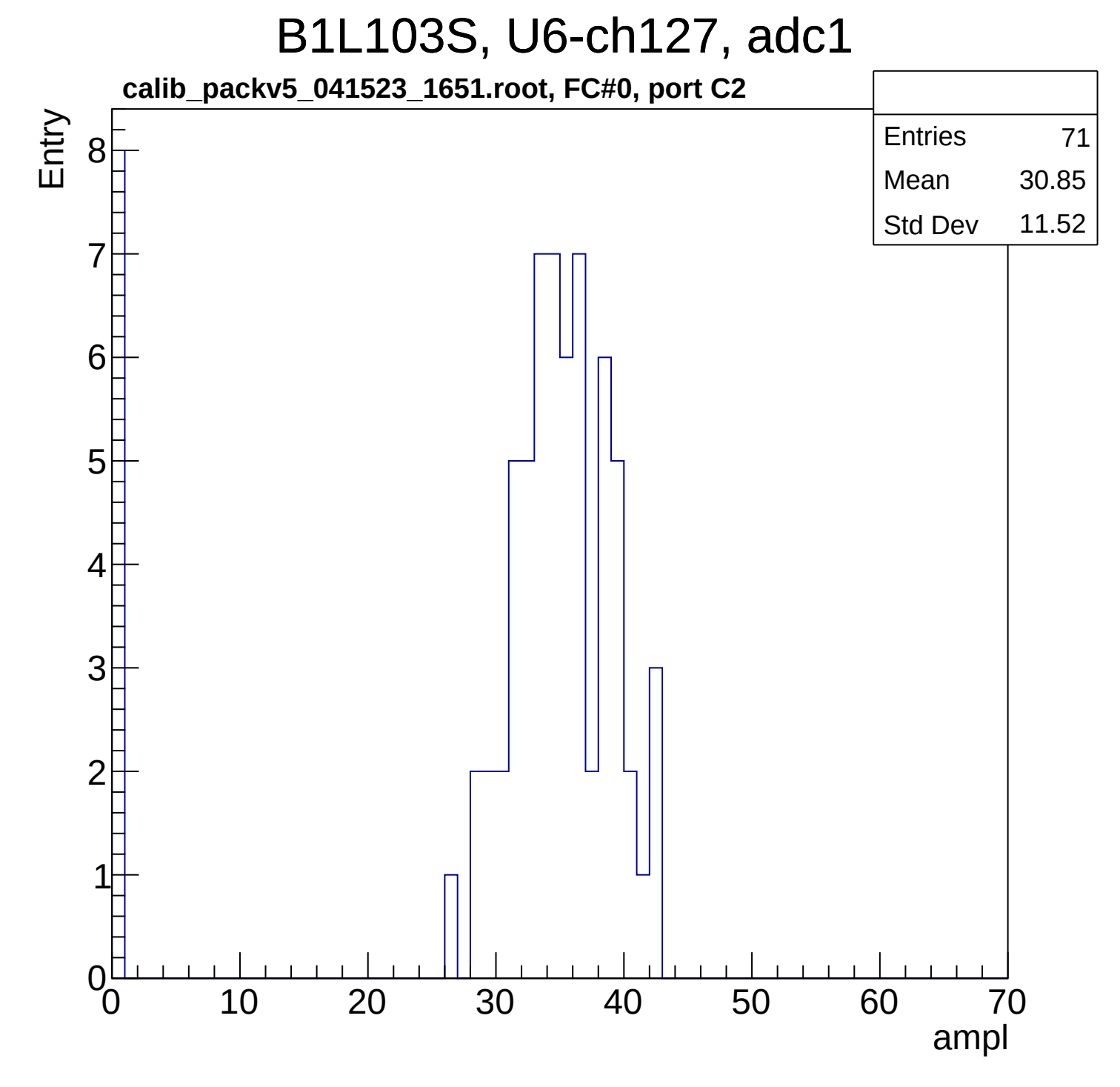
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch127, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 30.85
Std Dev 11.52
Entry
ampl
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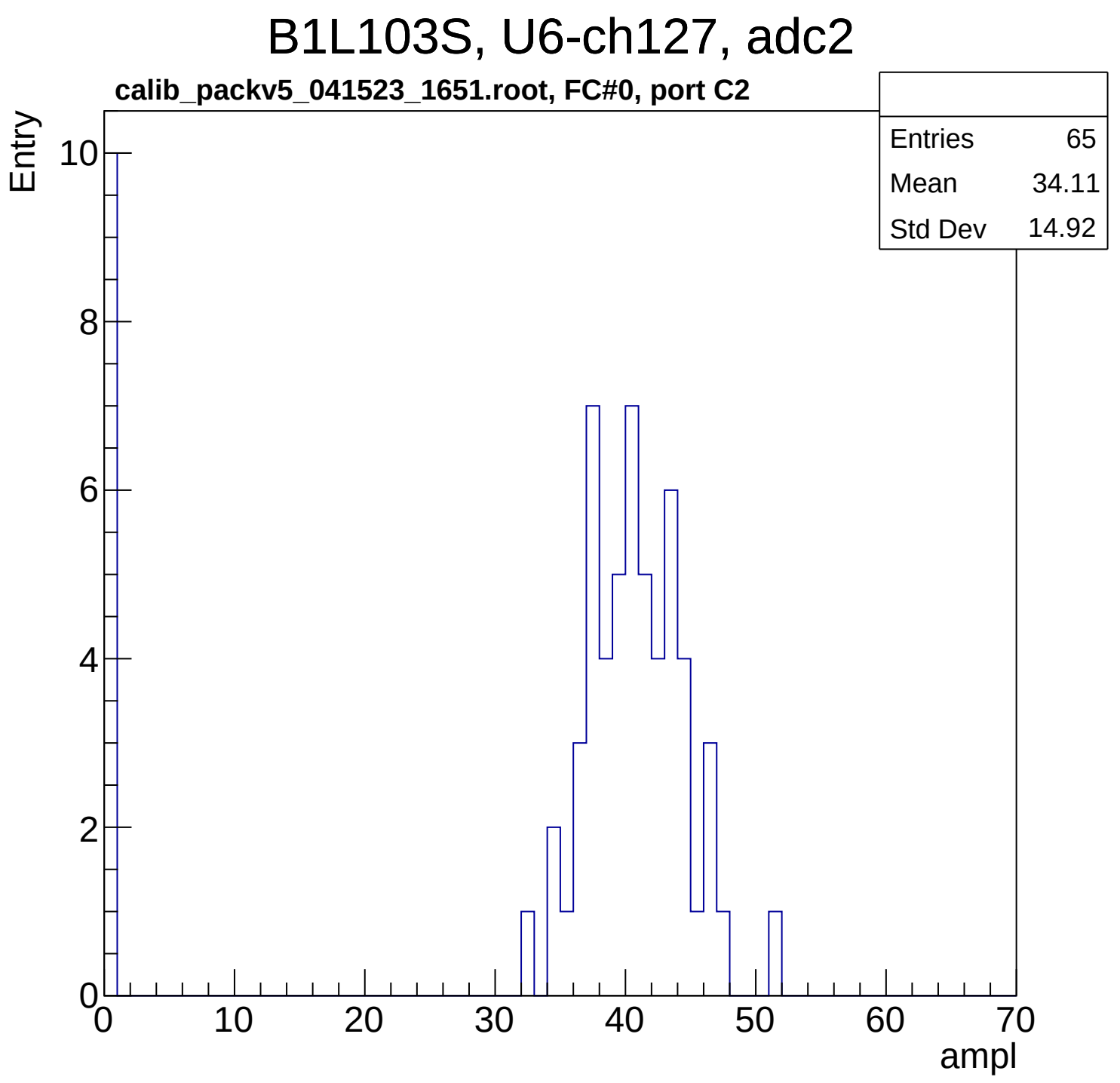
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U6-ch127, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 34.11
Std Dev 14.92
Entry
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4
6
8
10
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10
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50
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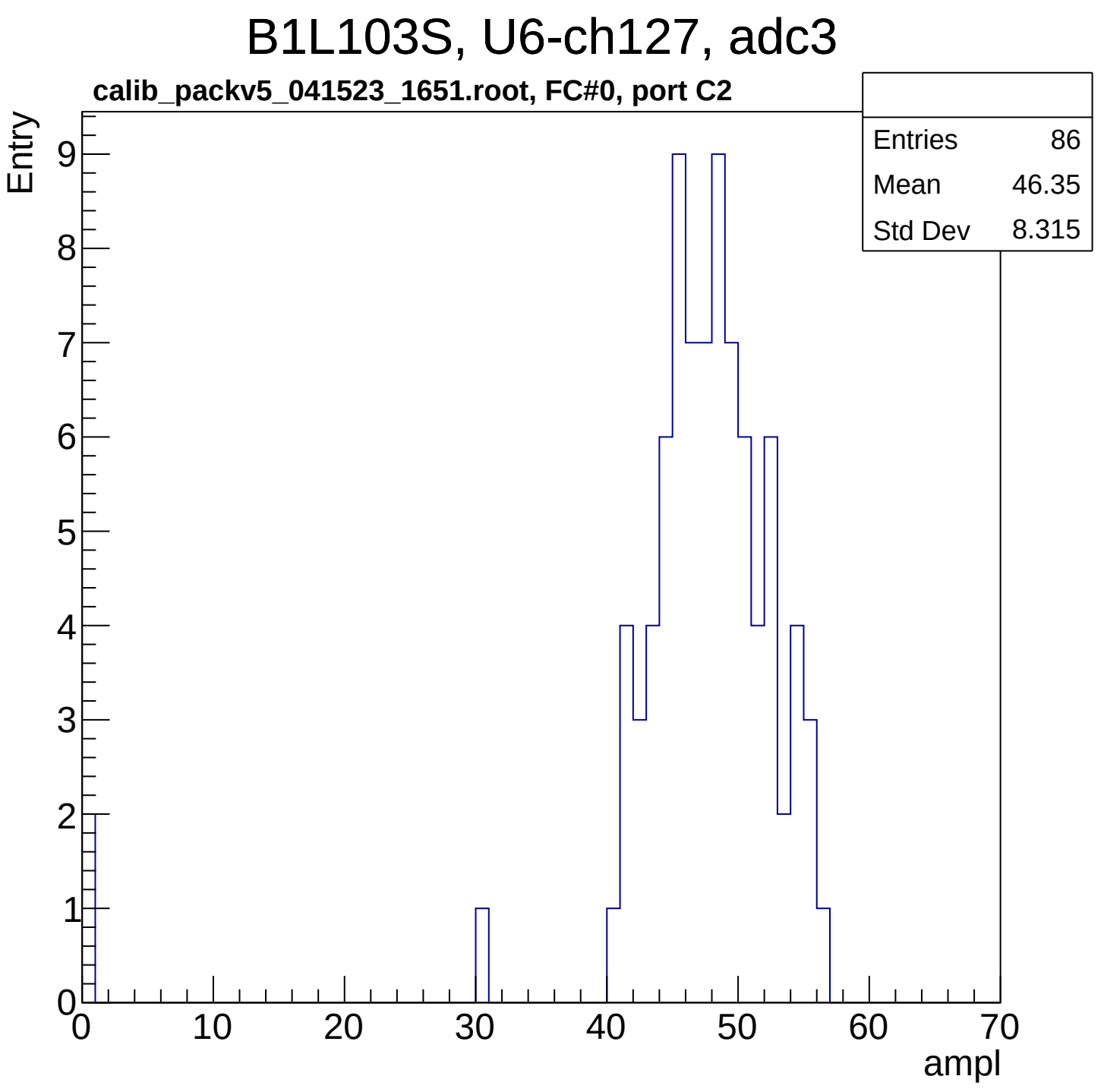
70
ampl


B1L103S, U6-ch127, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 46.35
Std Dev 8.315
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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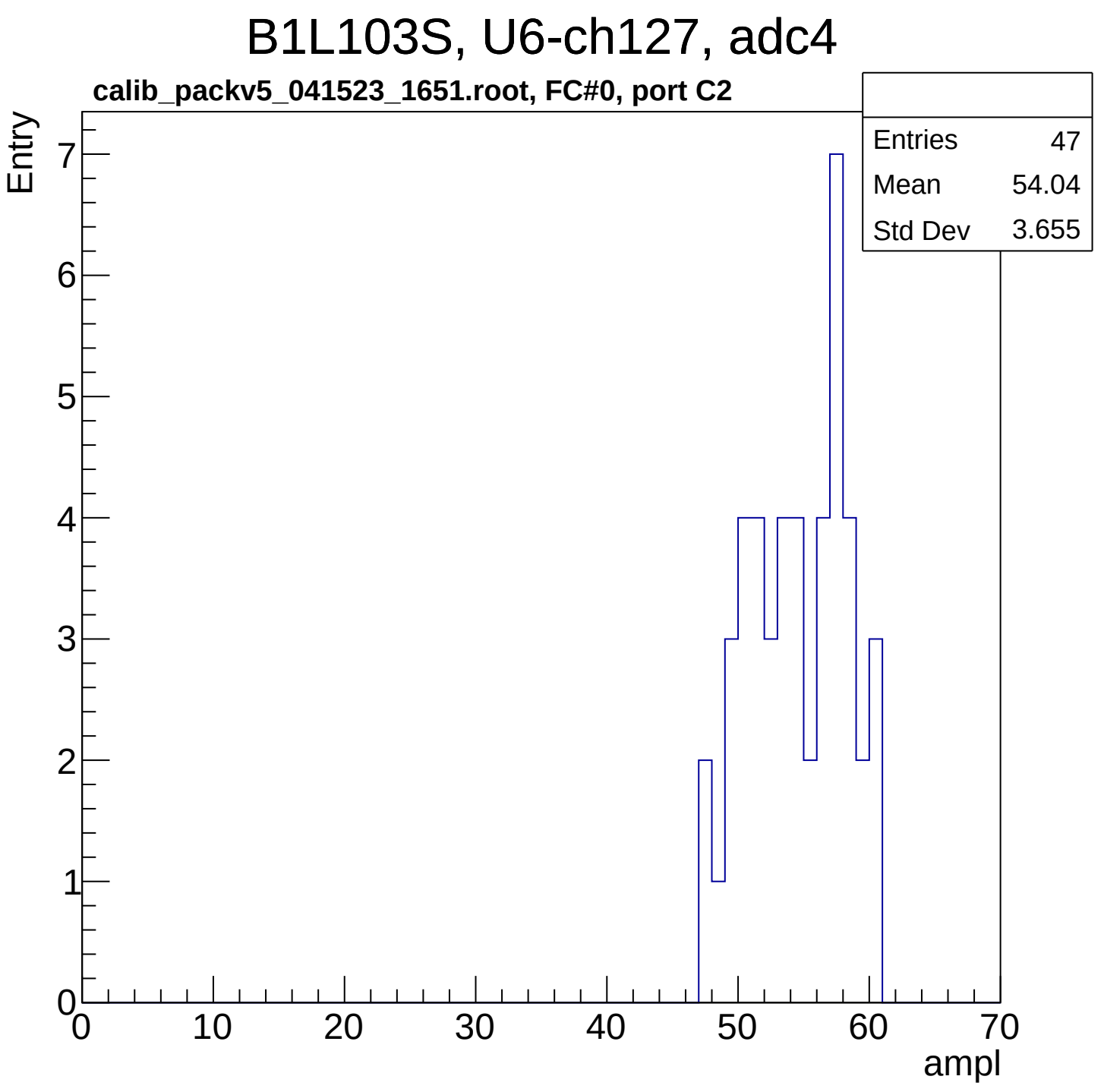
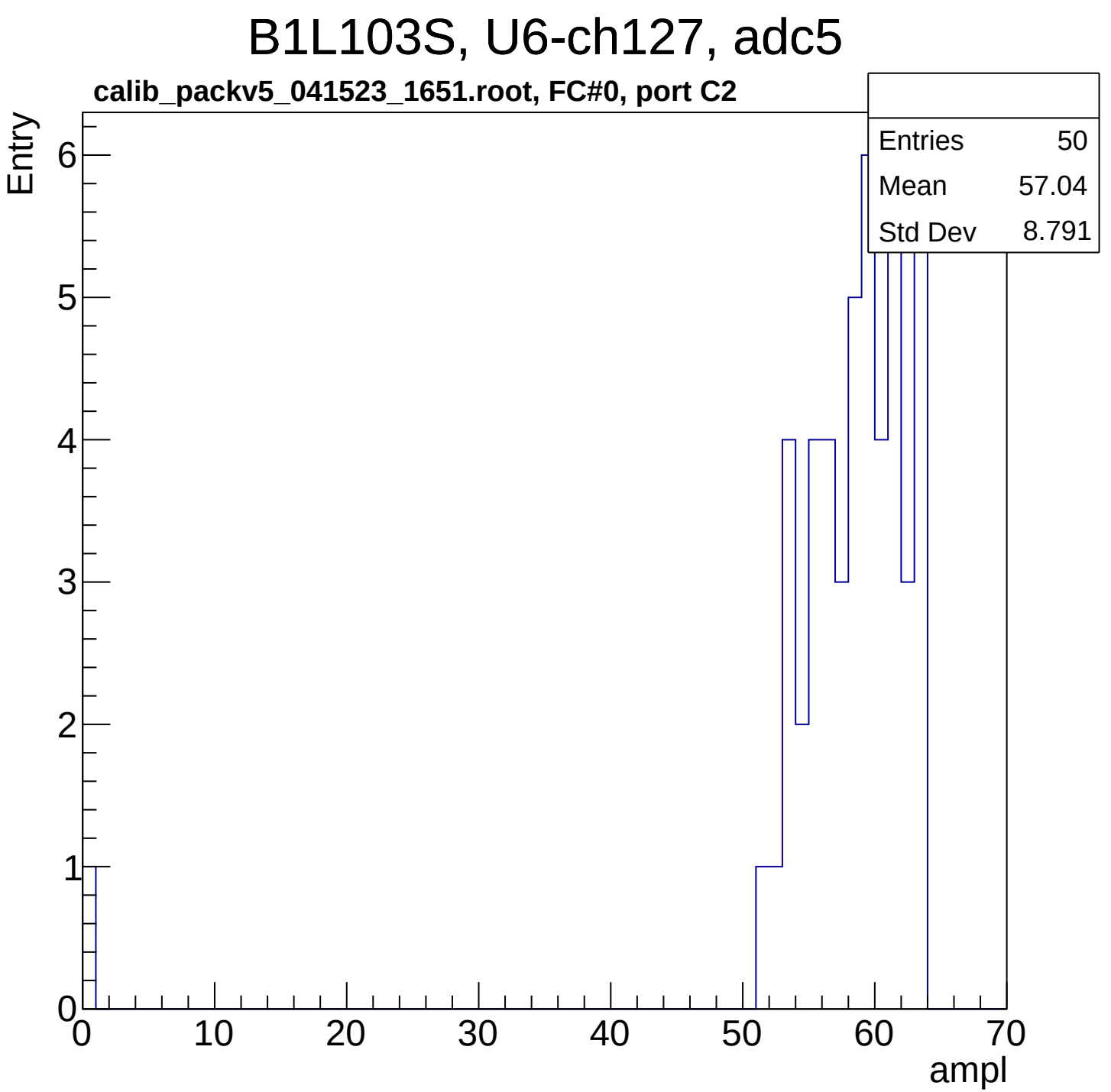
40
50
60
70


B1L103S, U6-ch127, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 54.04
Std Dev 3.655
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U6-ch127, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 57.04
Std Dev 8.791
Entry
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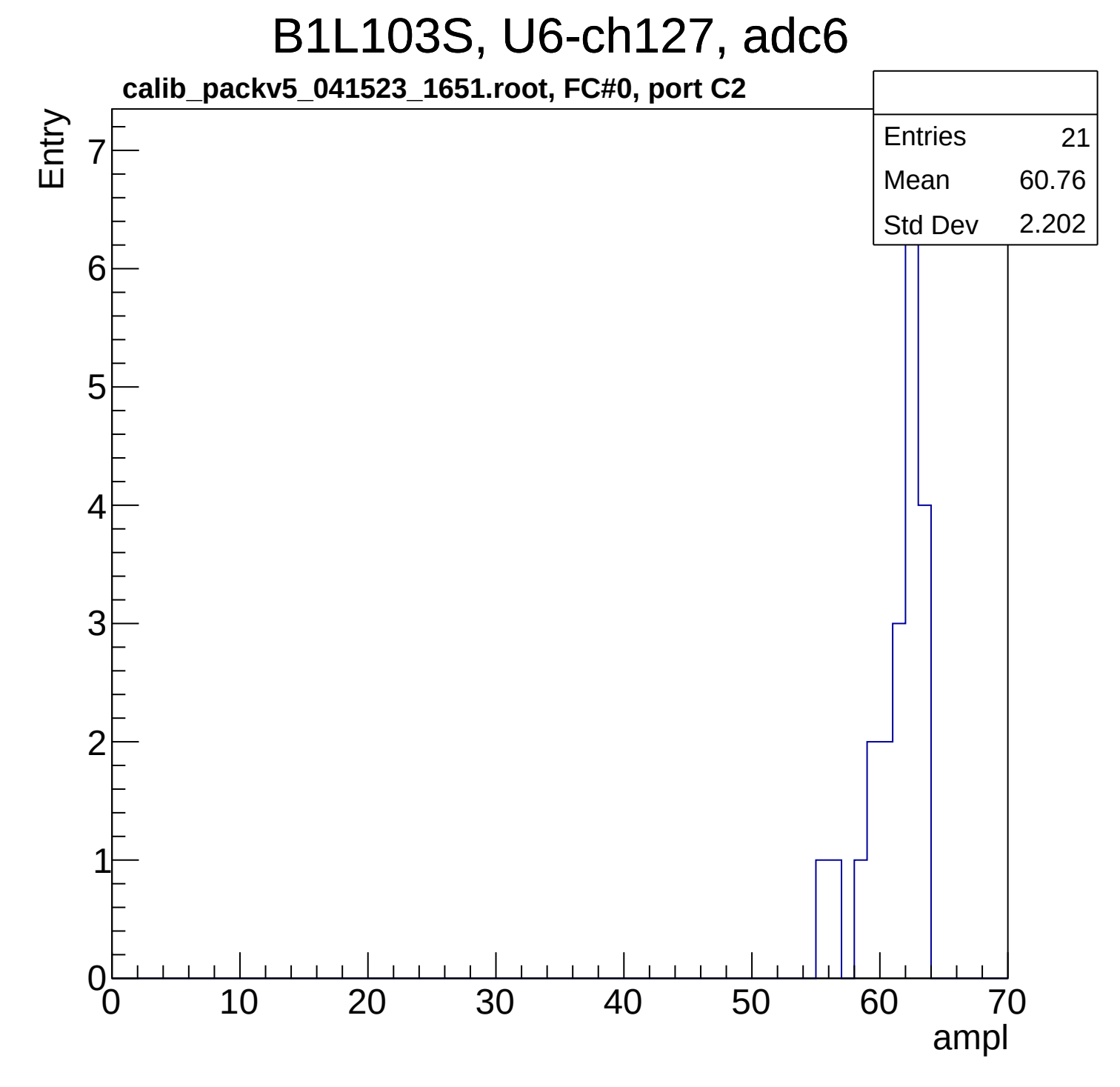
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U6-ch127, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 60.76
Std Dev 2.202
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
50
60
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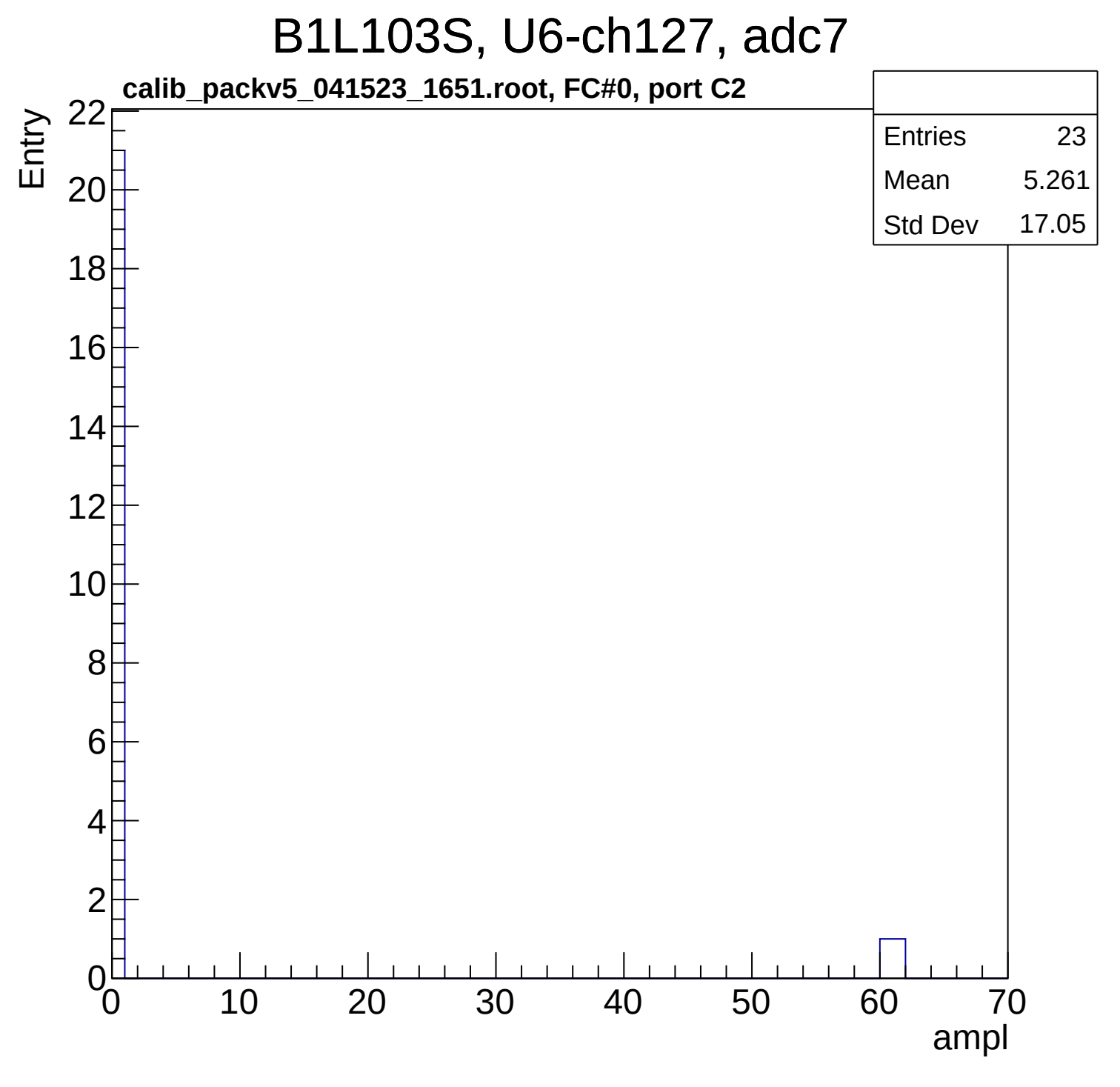
B1L103S, U6-ch127, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 5.261
Std Dev 17.05
Entry
ampl
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8
10
12
14
16
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20
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0
10
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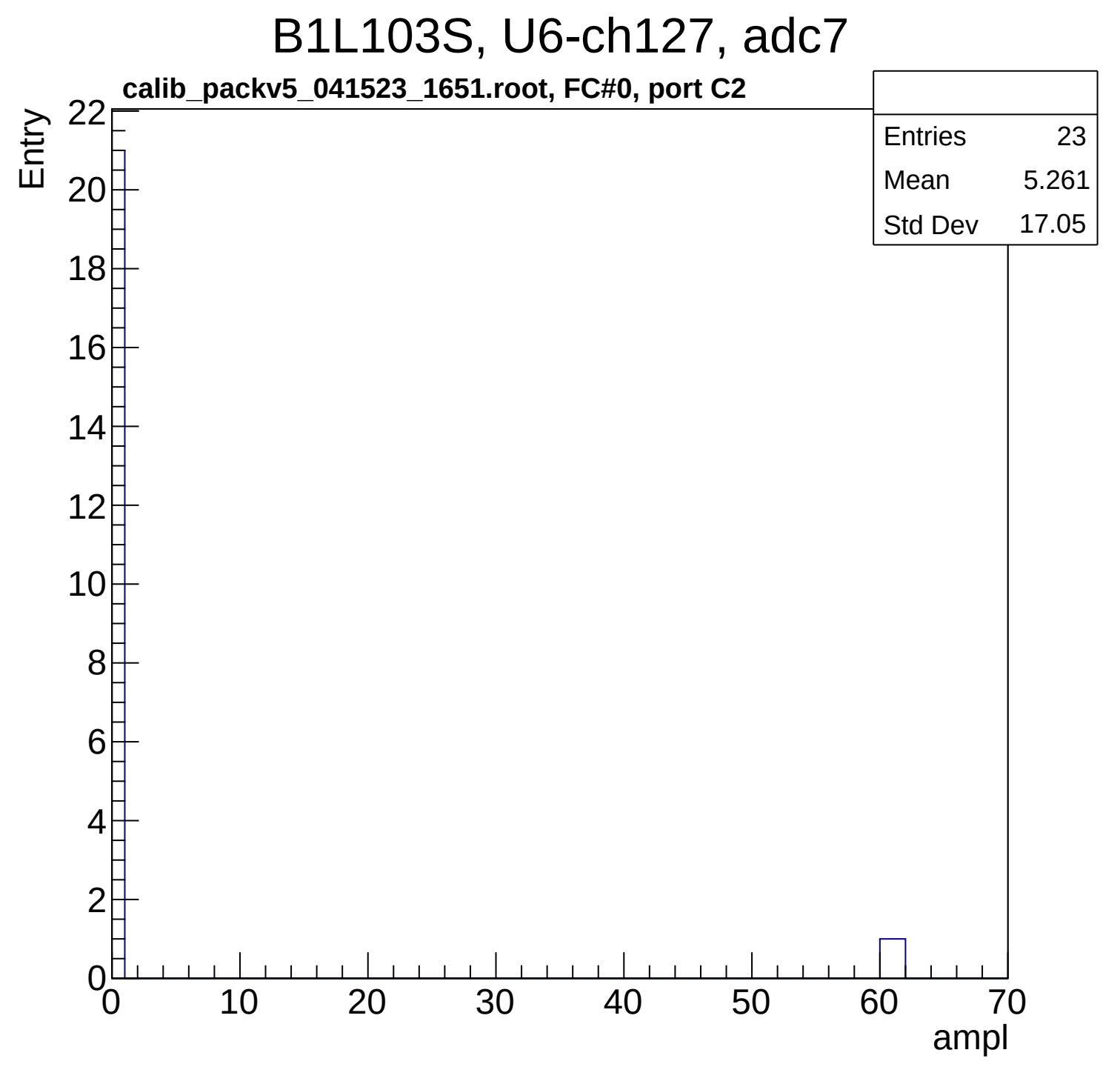
50
60
70


B1L103S, U6-ch127, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 5.261
Std Dev 17.05
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
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0
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60
70