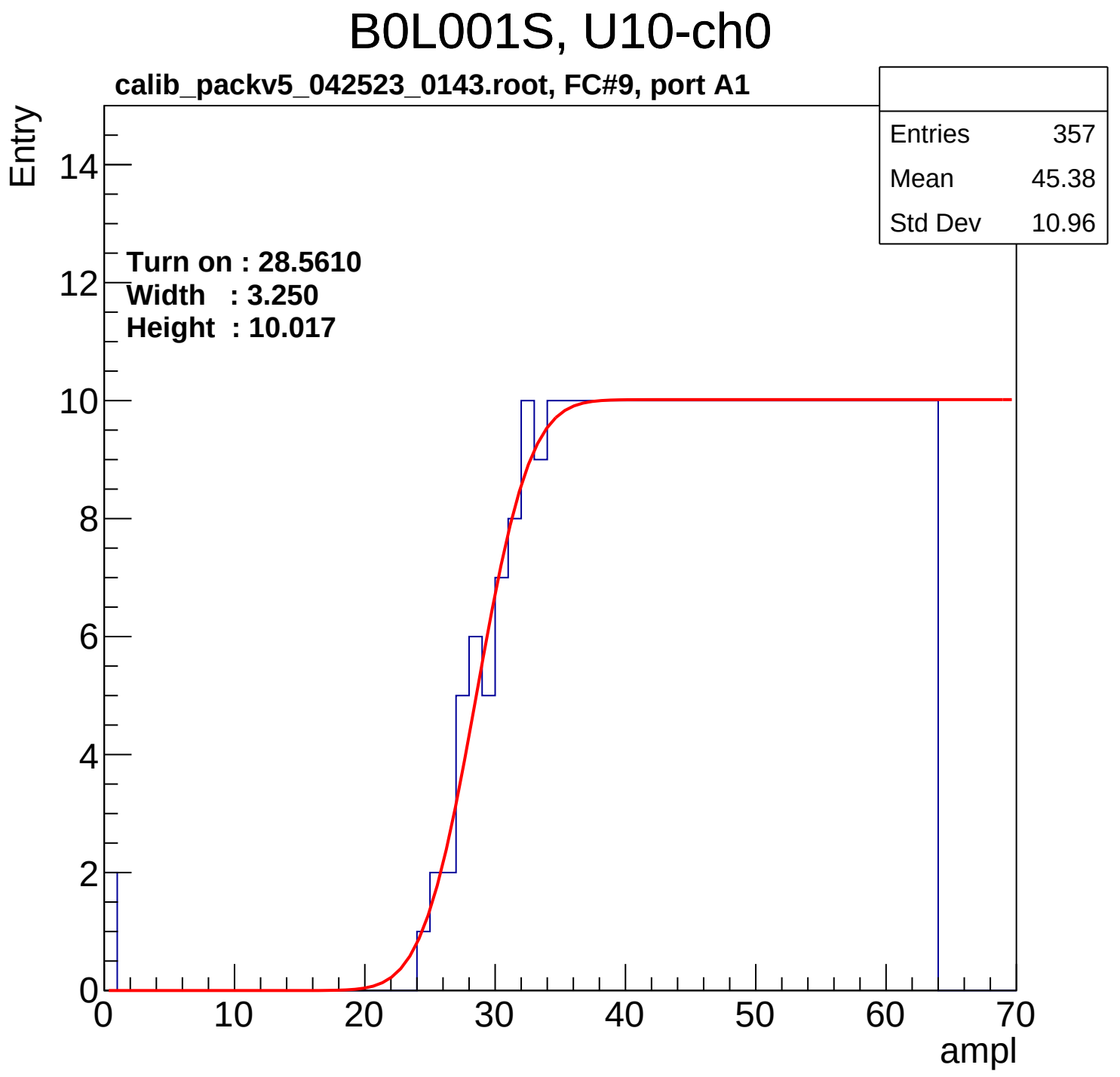
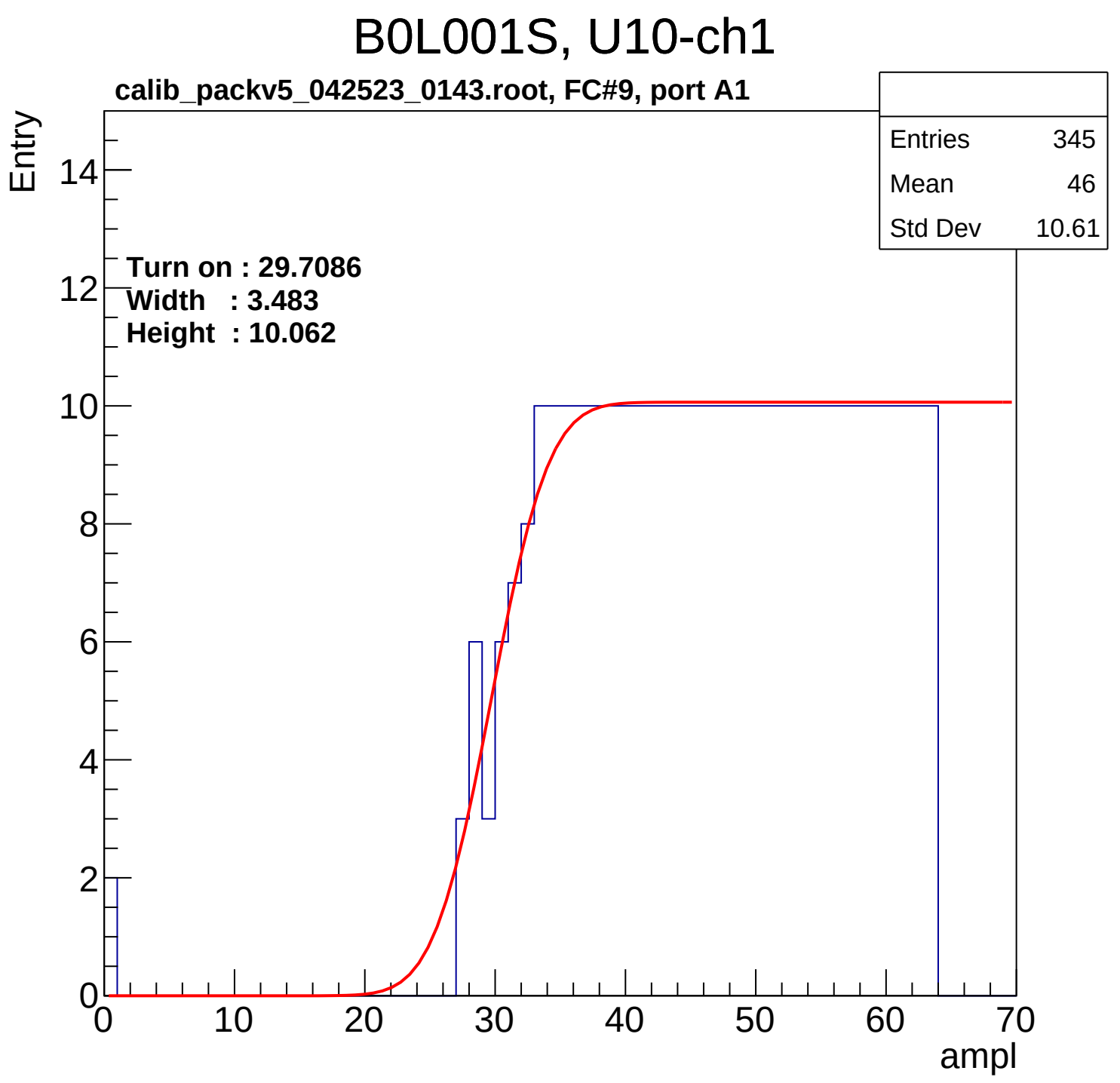
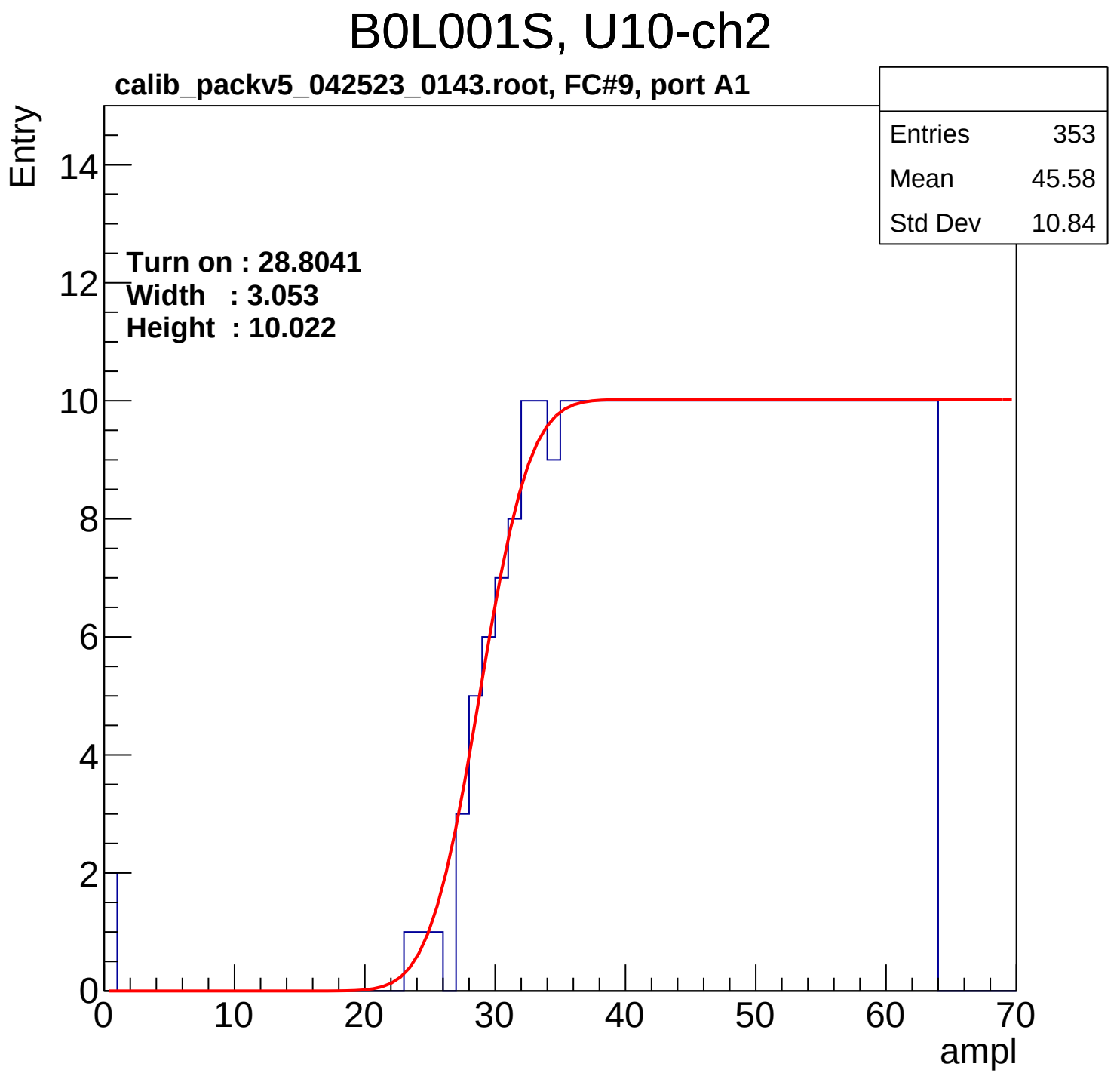
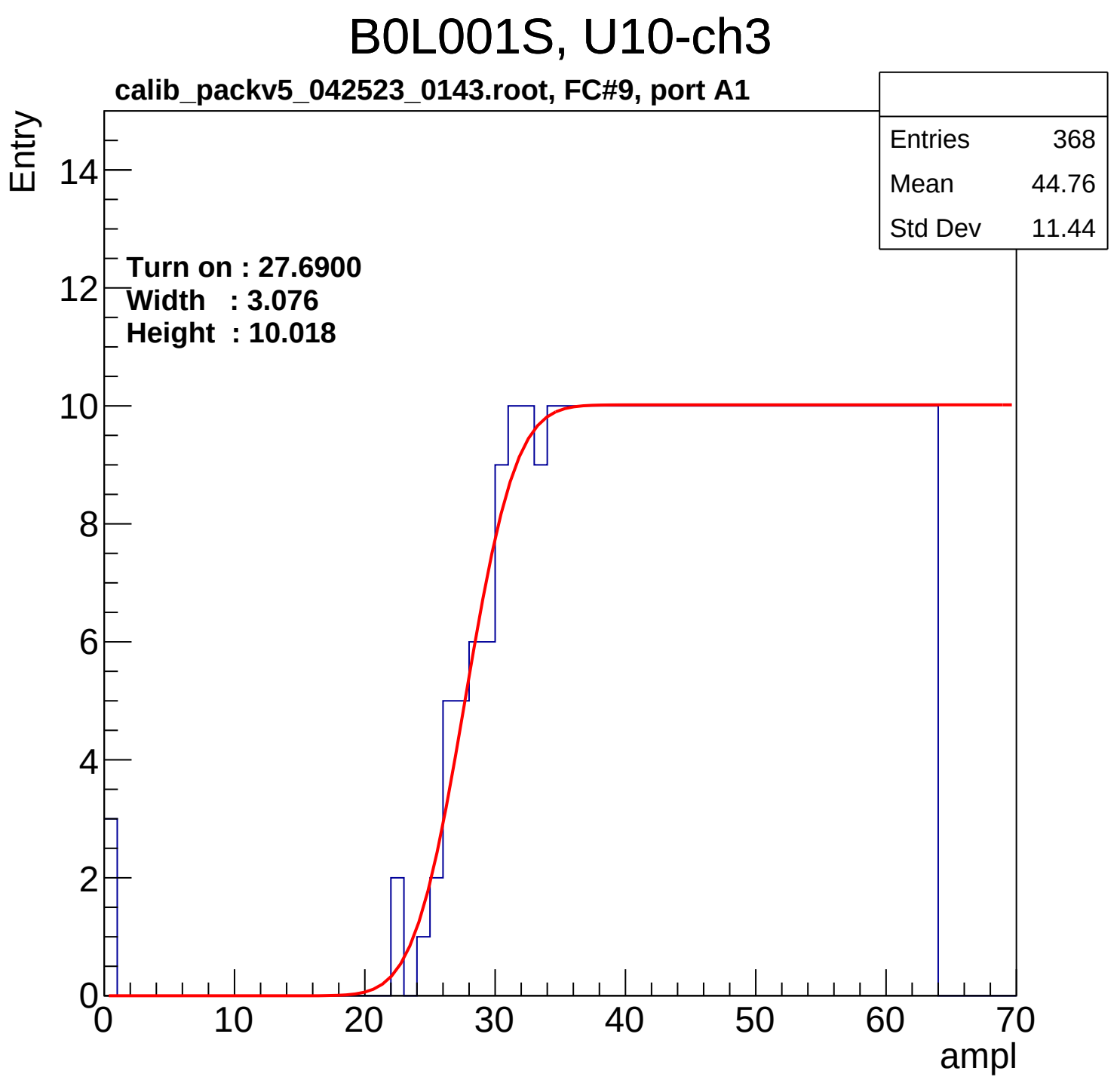
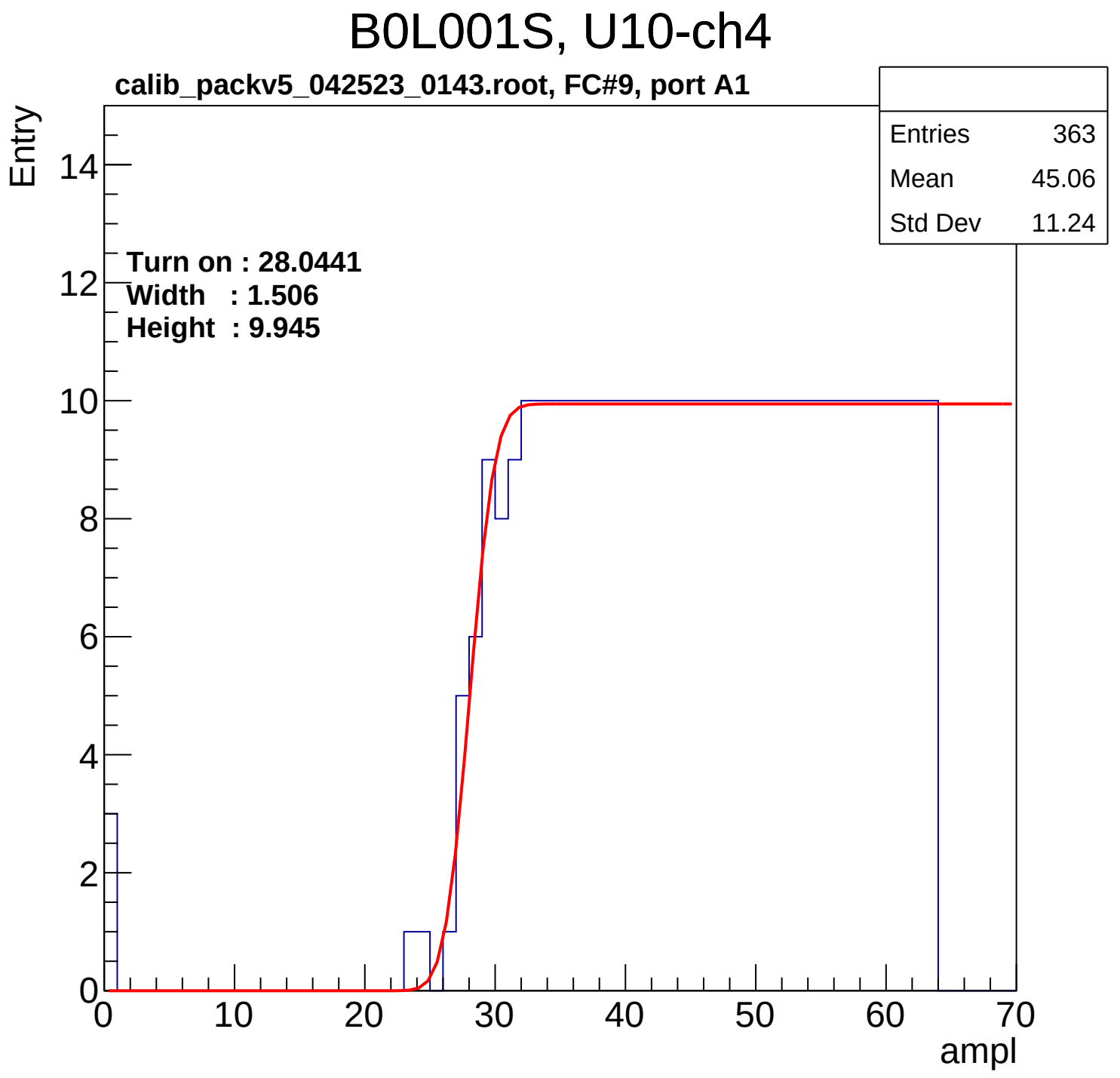
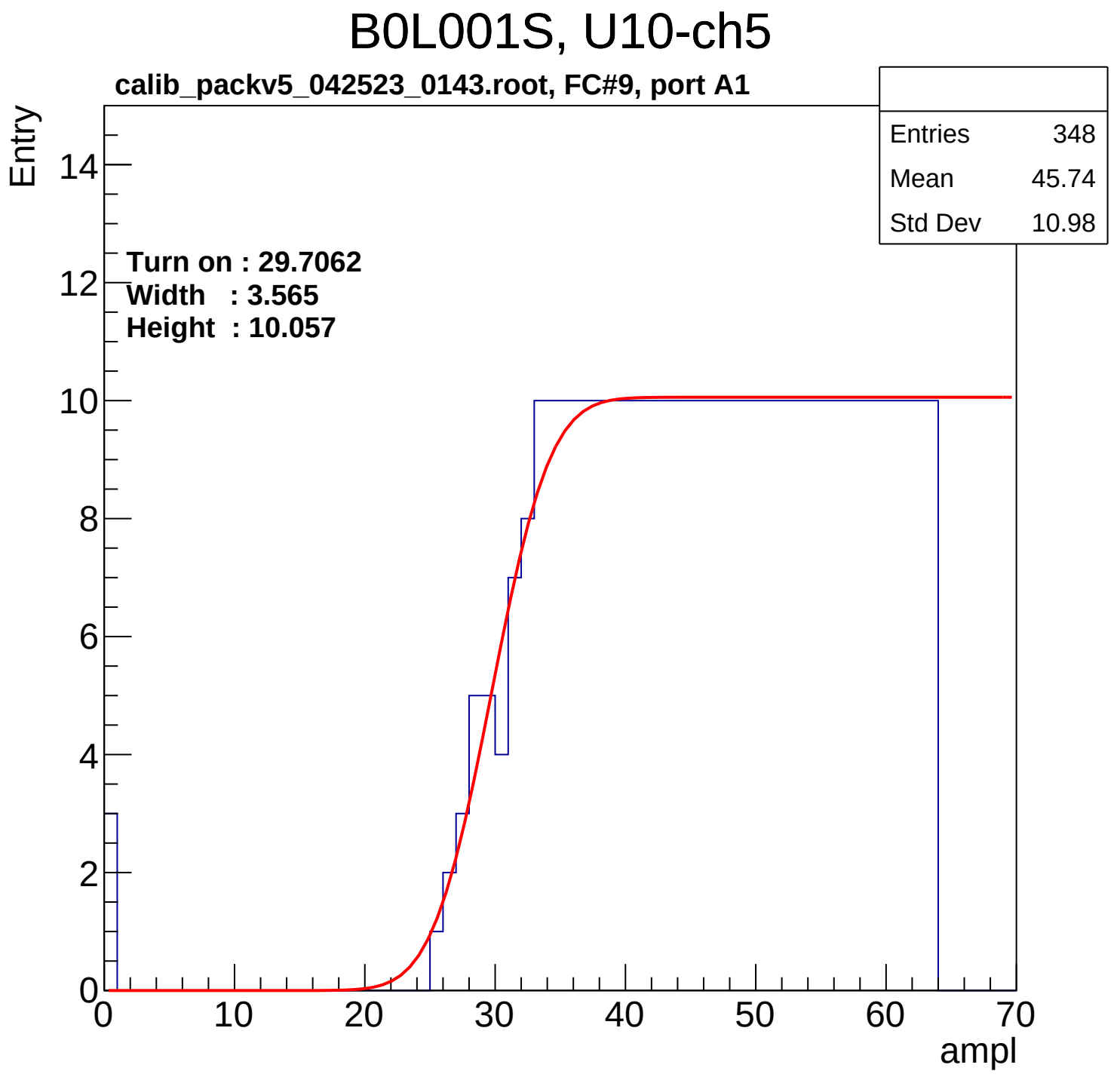

B0L001S, U10-ch0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 357
Mean 45.38
Std Dev 10.96
Turn on : 28.5610
Width : 3.250
Height : 10.017
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

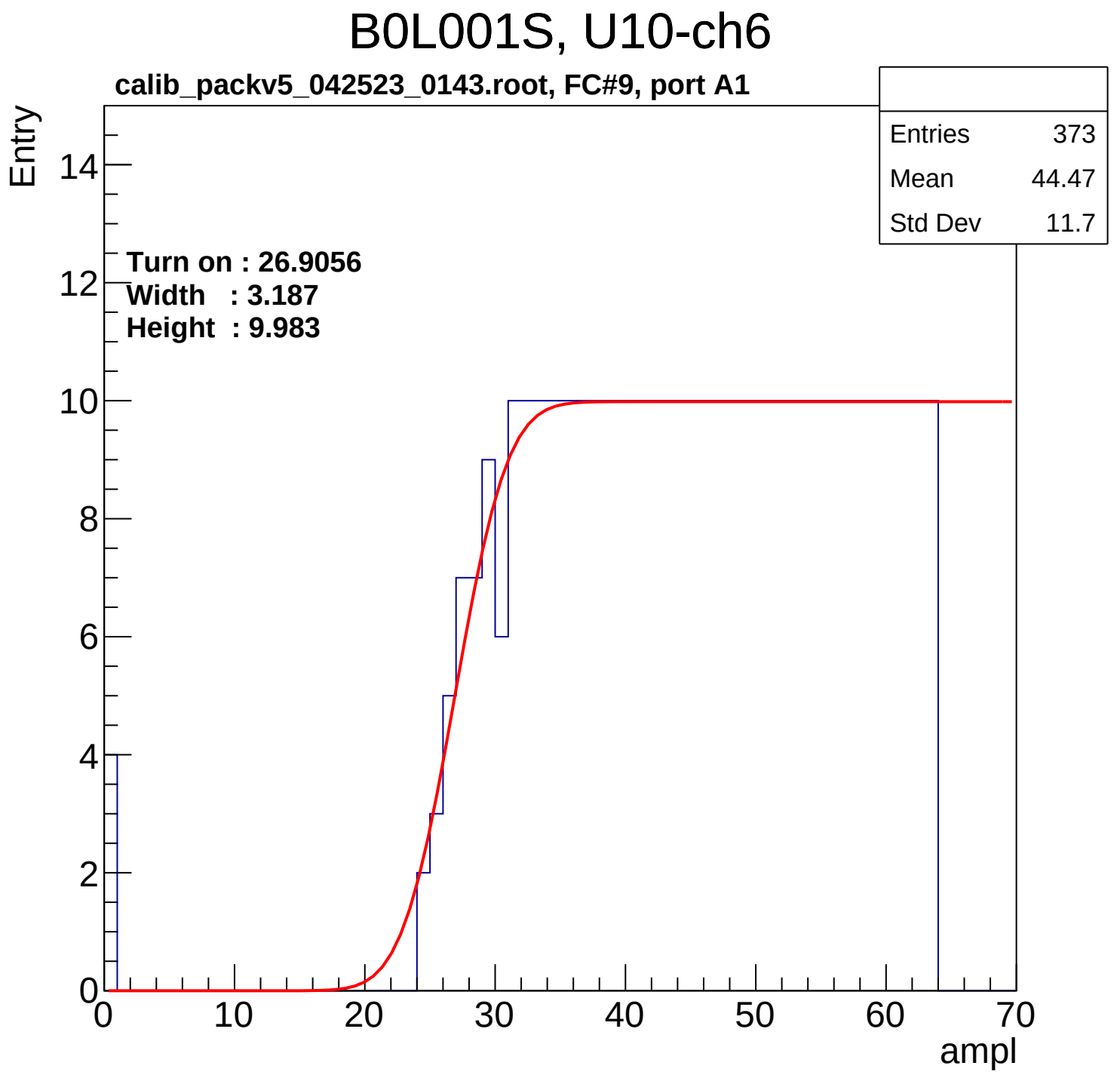

B0L001S, U10-ch1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 345
Mean 46
Std Dev 10.61
Turn on : 29.7086
Width : 3.483
Height : 10.062
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

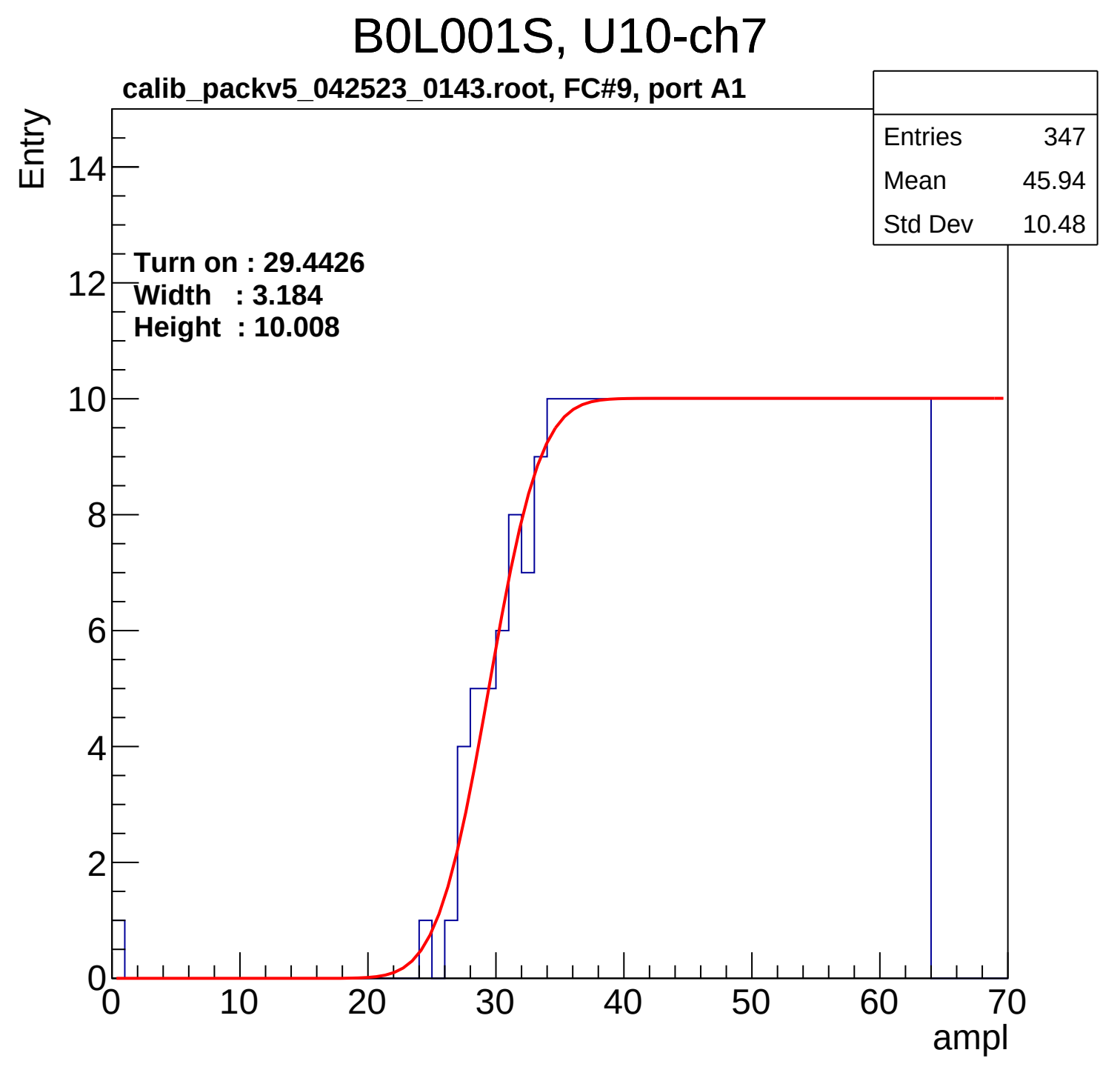

B0L001S, U10-ch2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 353
Mean 45.58
Std Dev 10.84
Turn on : 28.8041
Width : 3.053
Height : 10.022
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

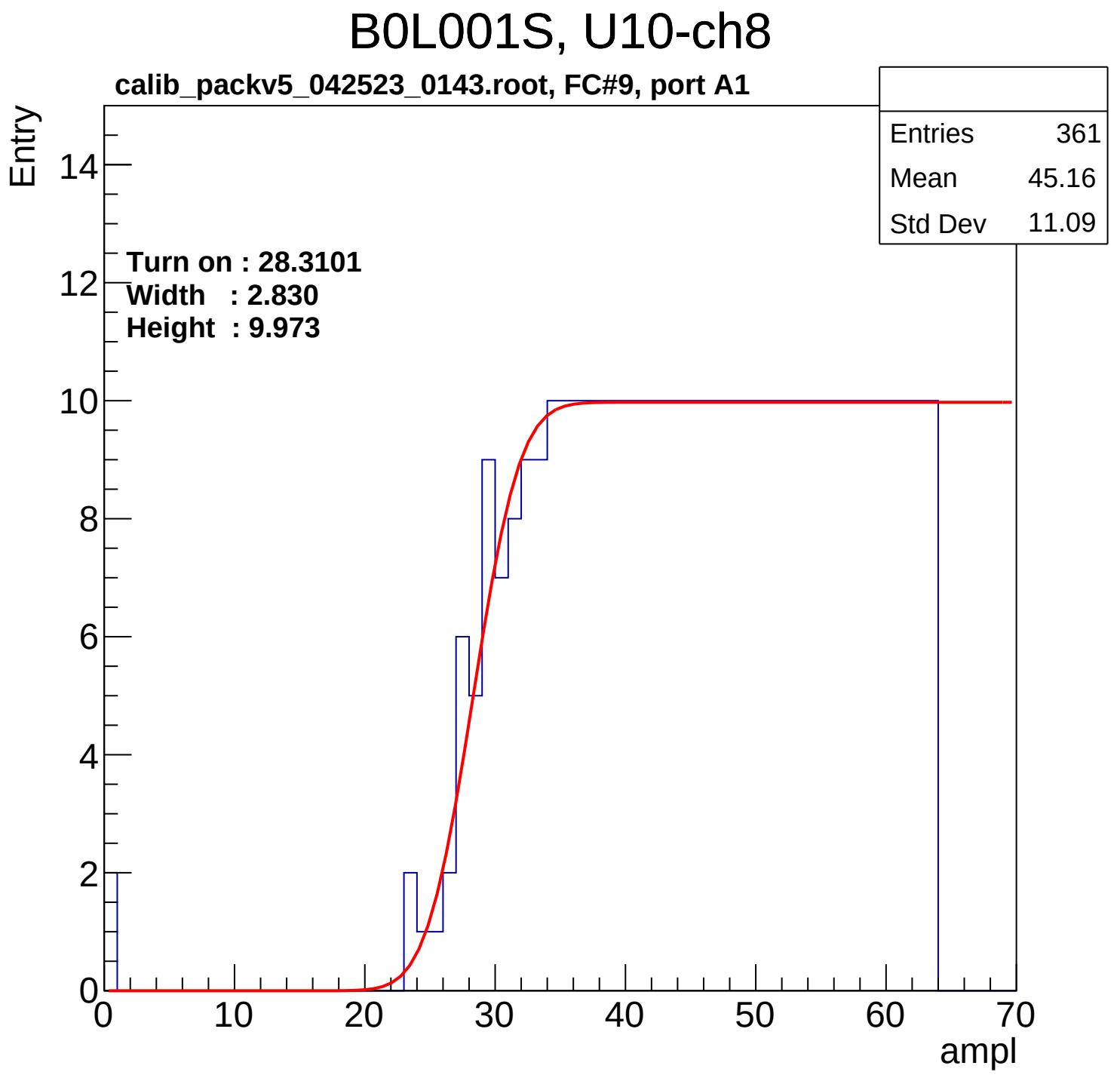

B0L001S, U10-ch3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.76
Std Dev 11.44
Turn on : 27.6900
Width : 3.076
Height : 10.018
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

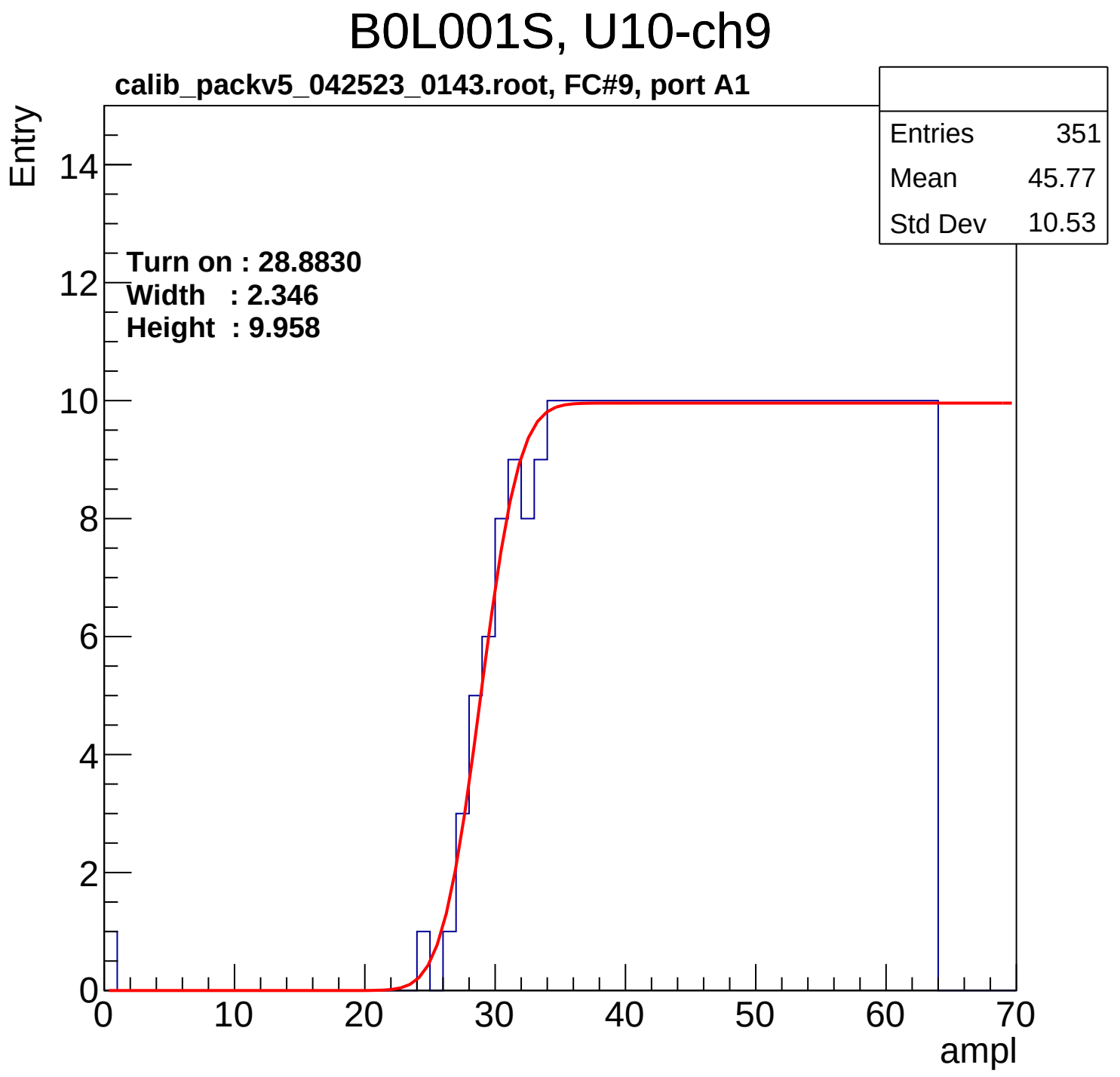

B0L001S, U10-ch4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 45.06
Std Dev 11.24
Turn on : 28.0441
Width : 1.506
Height : 9.945
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

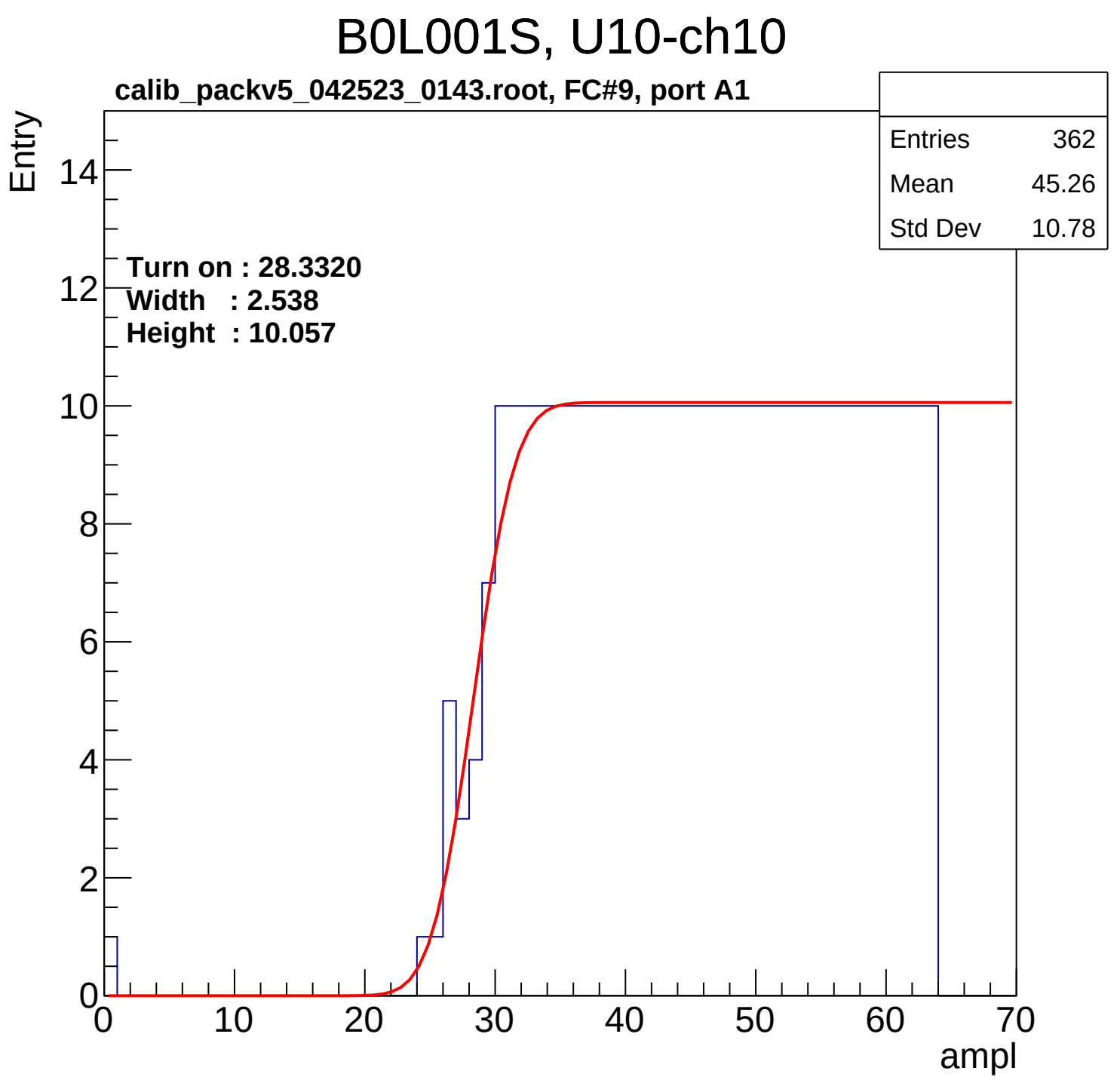

B0L001S, U10-ch5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 348
Mean 45.74
Std Dev 10.98
Turn on : 29.7062
Width : 3.565
Height : 10.057
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

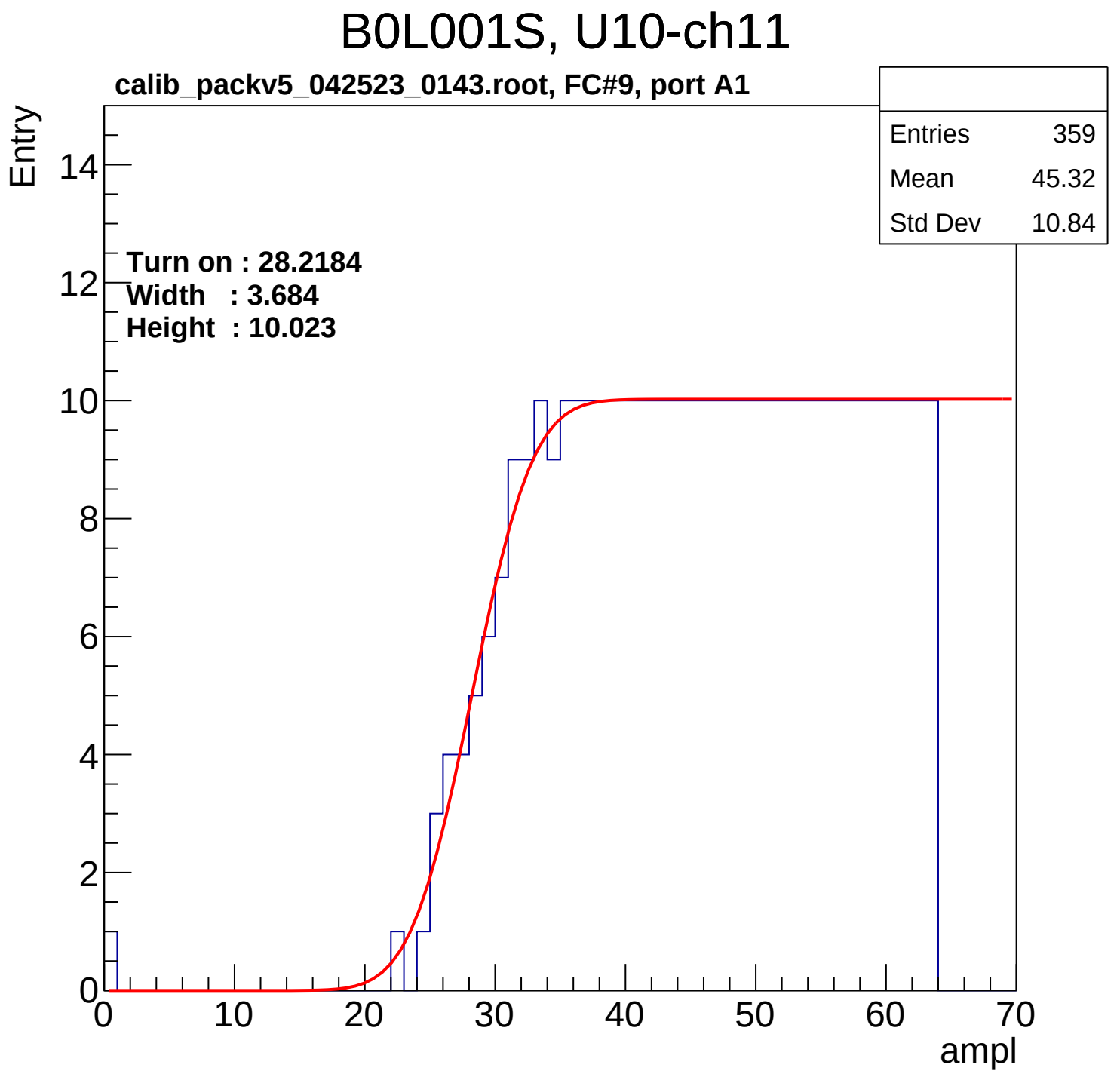

B0L001S, U10-ch6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 373
Mean 44.47
Std Dev 11.7
Turn on : 26.9056
Width : 3.187
Height : 9.983
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

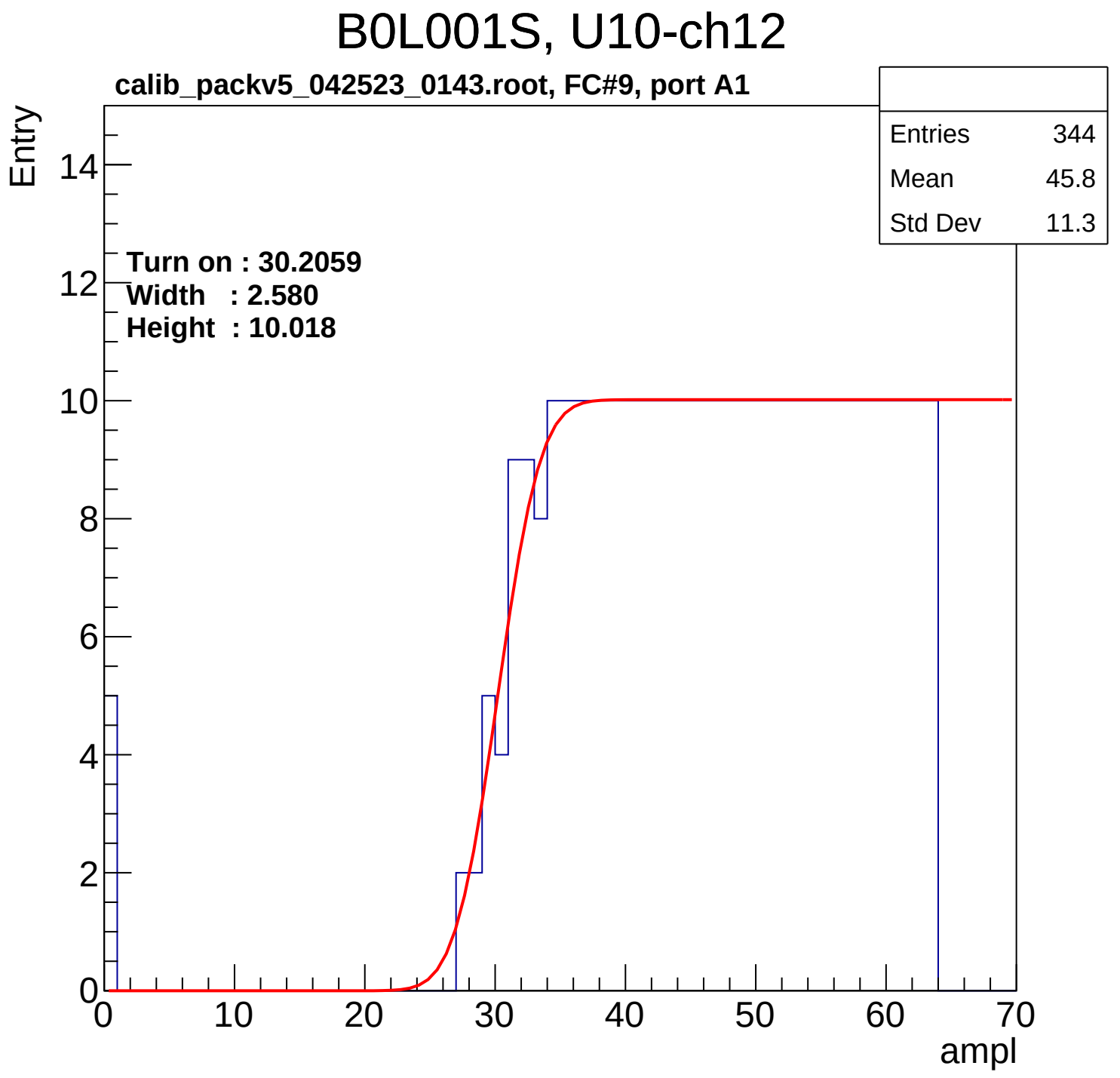

B0L001S, U10-ch7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 347
Mean 45.94
Std Dev 10.48
Turn on : 29.4426
Width : 3.184
Height : 10.008
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

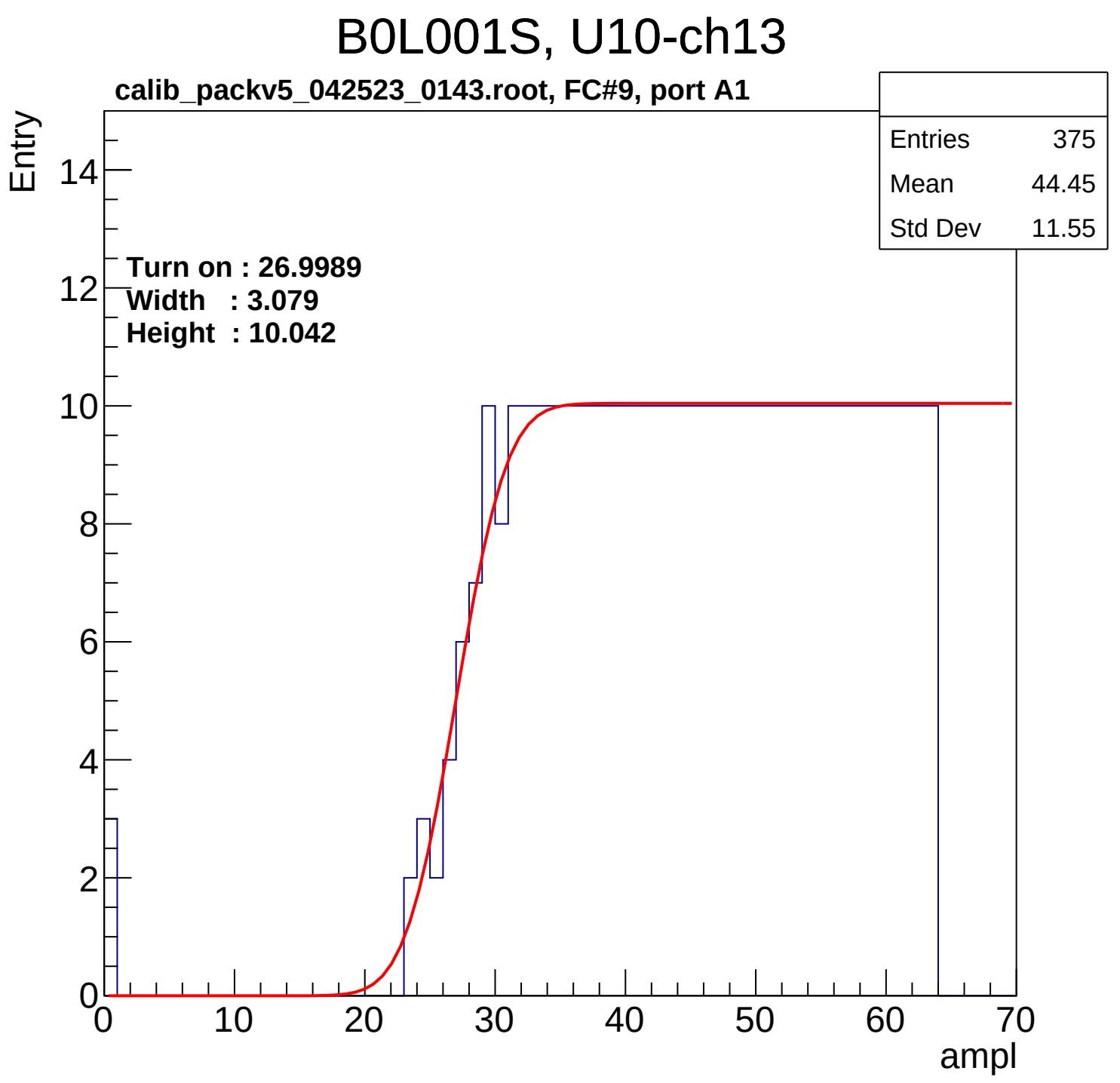

B0L001S, U10-ch8
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 45.16
Std Dev 11.09
Turn on : 28.3101
Width : 2.830
Height : 9.973
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

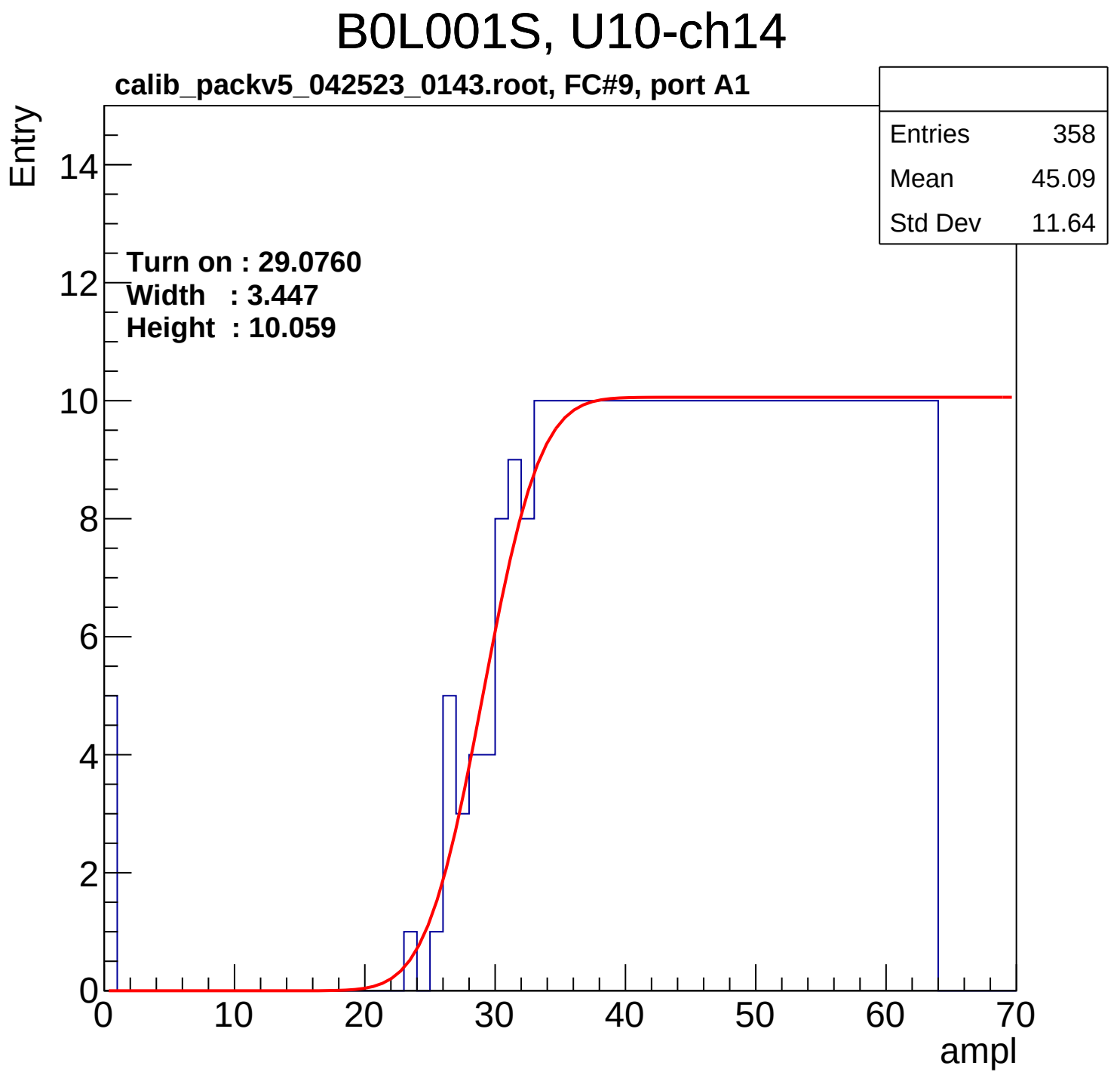

B0L001S, U10-ch9
calib_packv5_042523_0143.root, FC#9, port A1
Entries 351
Mean 45.77
Std Dev 10.53
Turn on : 28.8830
Width : 2.346
Height : 9.958
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

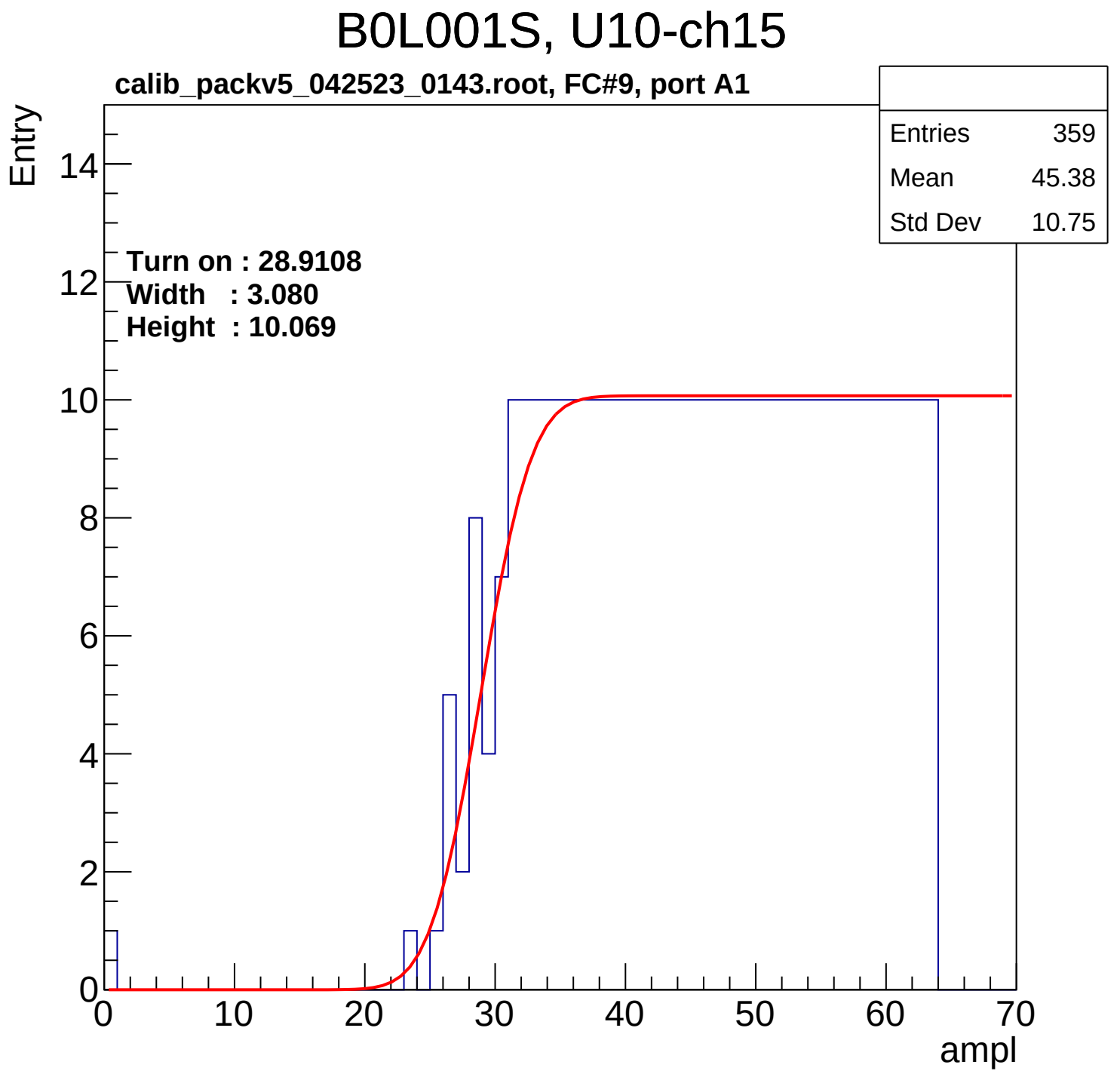

B0L001S, U10-ch10
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 45.26
Std Dev 10.78
Turn on : 28.3320
Width : 2.538
Height : 10.057
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

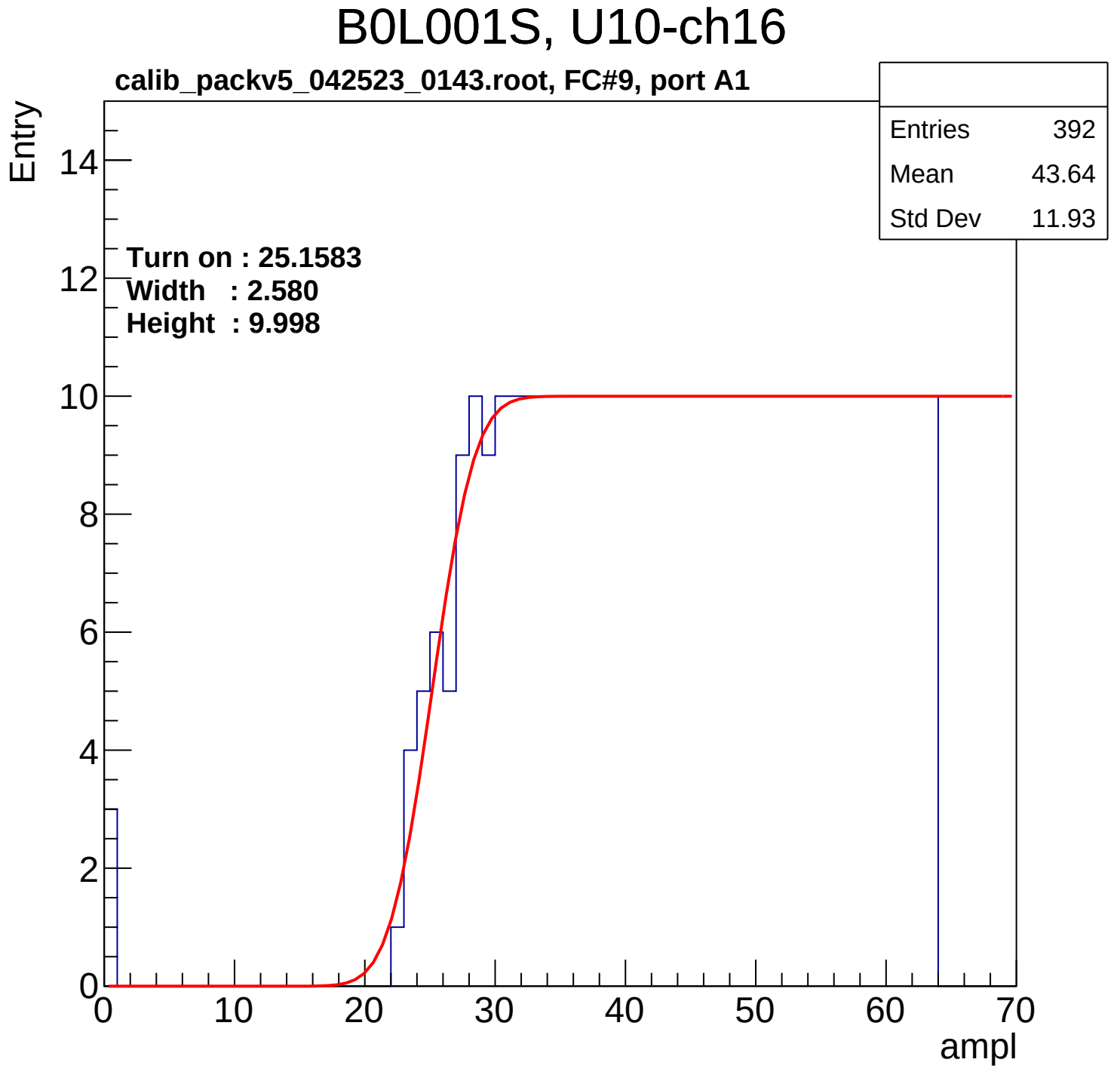

B0L001S, U10-ch11
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 45.32
Std Dev 10.84
Turn on : 28.2184
Width : 3.684
Height : 10.023
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

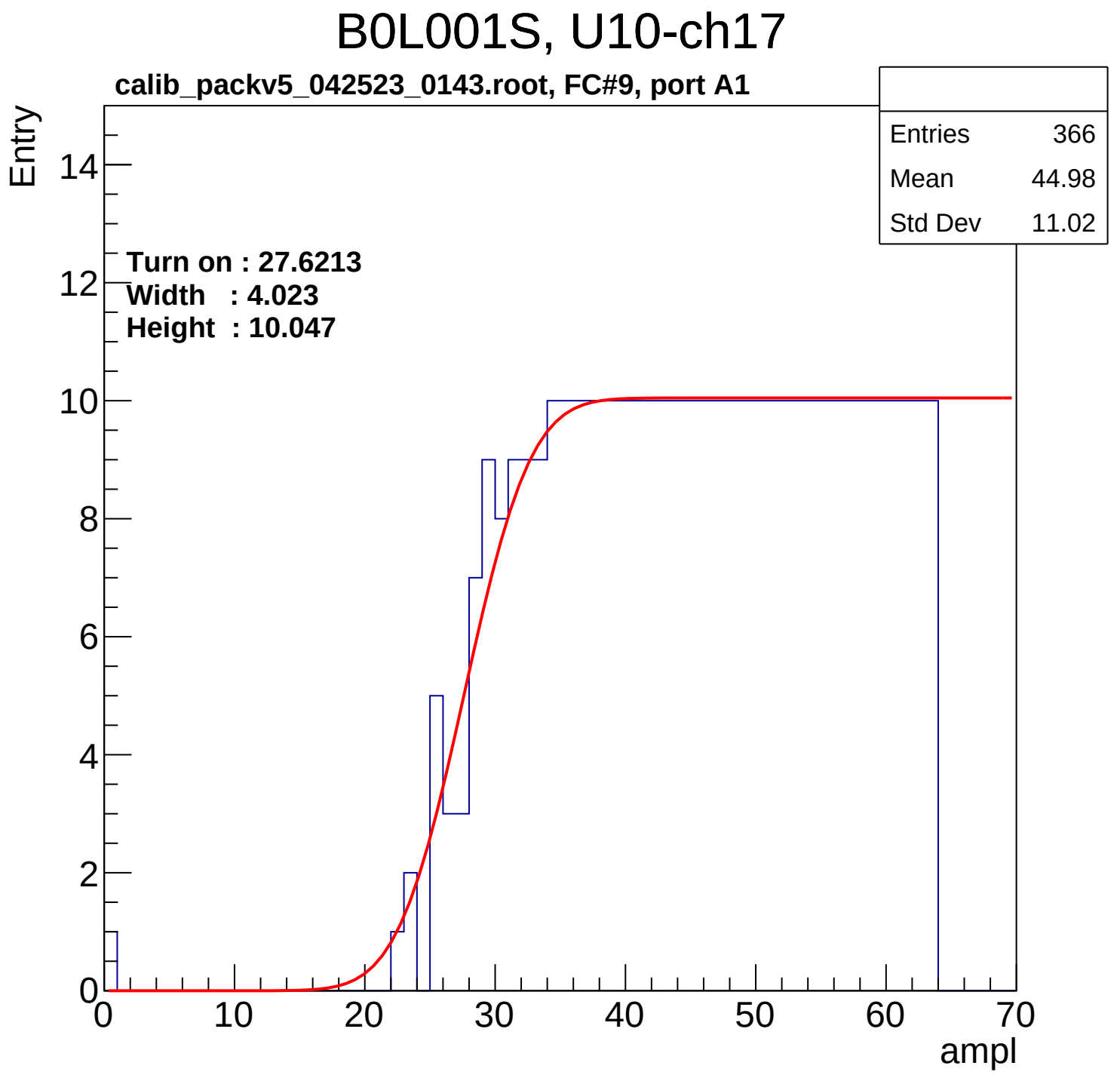

B0L001S, U10-ch12
calib_packv5_042523_0143.root, FC#9, port A1
Entries 344
Mean 45.8
Std Dev 11.3
Turn on : 30.2059
Width : 2.580
Height : 10.018
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

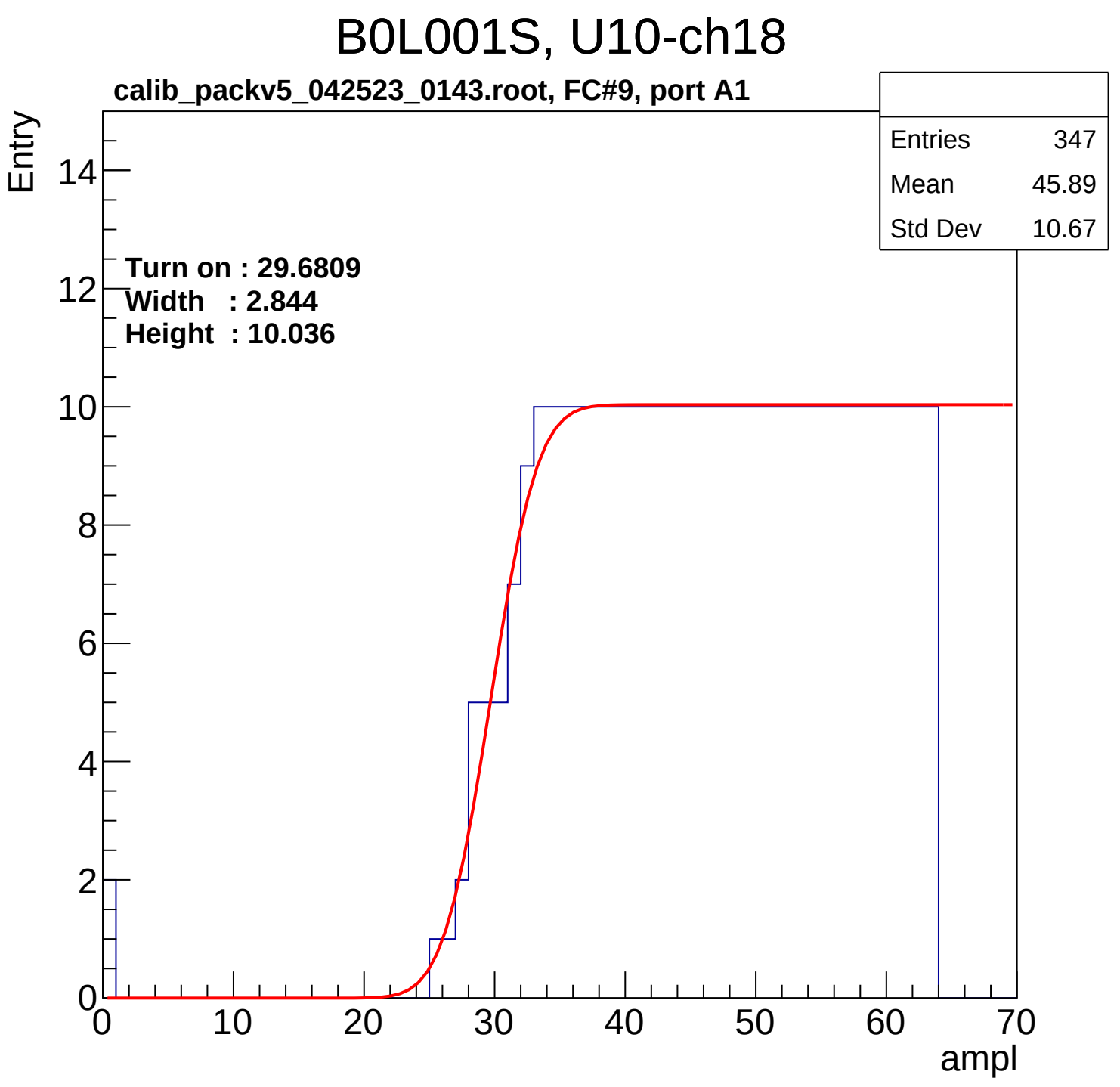

B0L001S, U10-ch13
calib_packv5_042523_0143.root, FC#9, port A1
Entries 375
Mean 44.45
Std Dev 11.55
Turn on : 26.9989
Width : 3.079
Height : 10.042
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

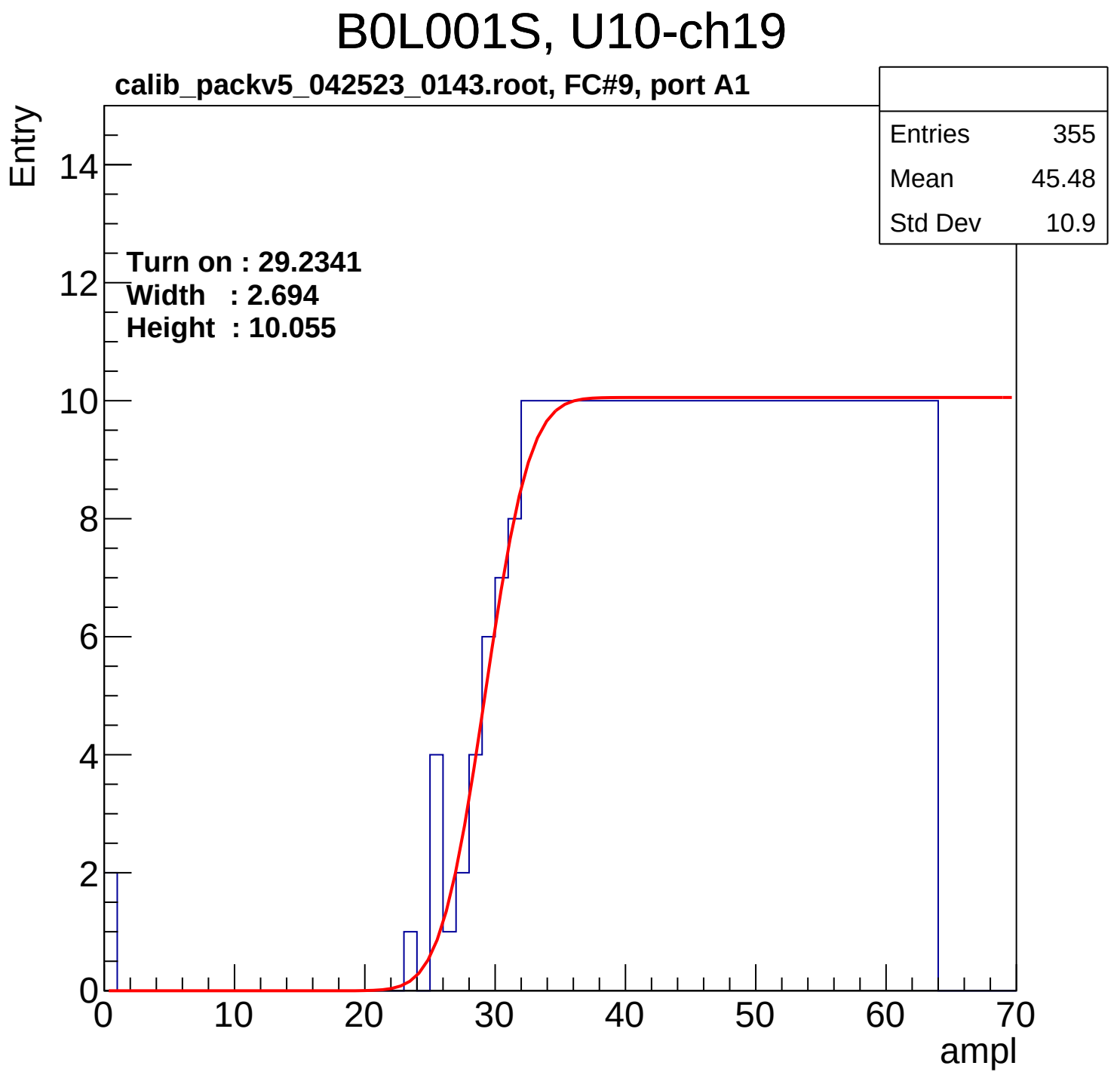

B0L001S, U10-ch14
calib_packv5_042523_0143.root, FC#9, port A1
Entries 358
Mean 45.09
Std Dev 11.64
Turn on : 29.0760
Width : 3.447
Height : 10.059
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

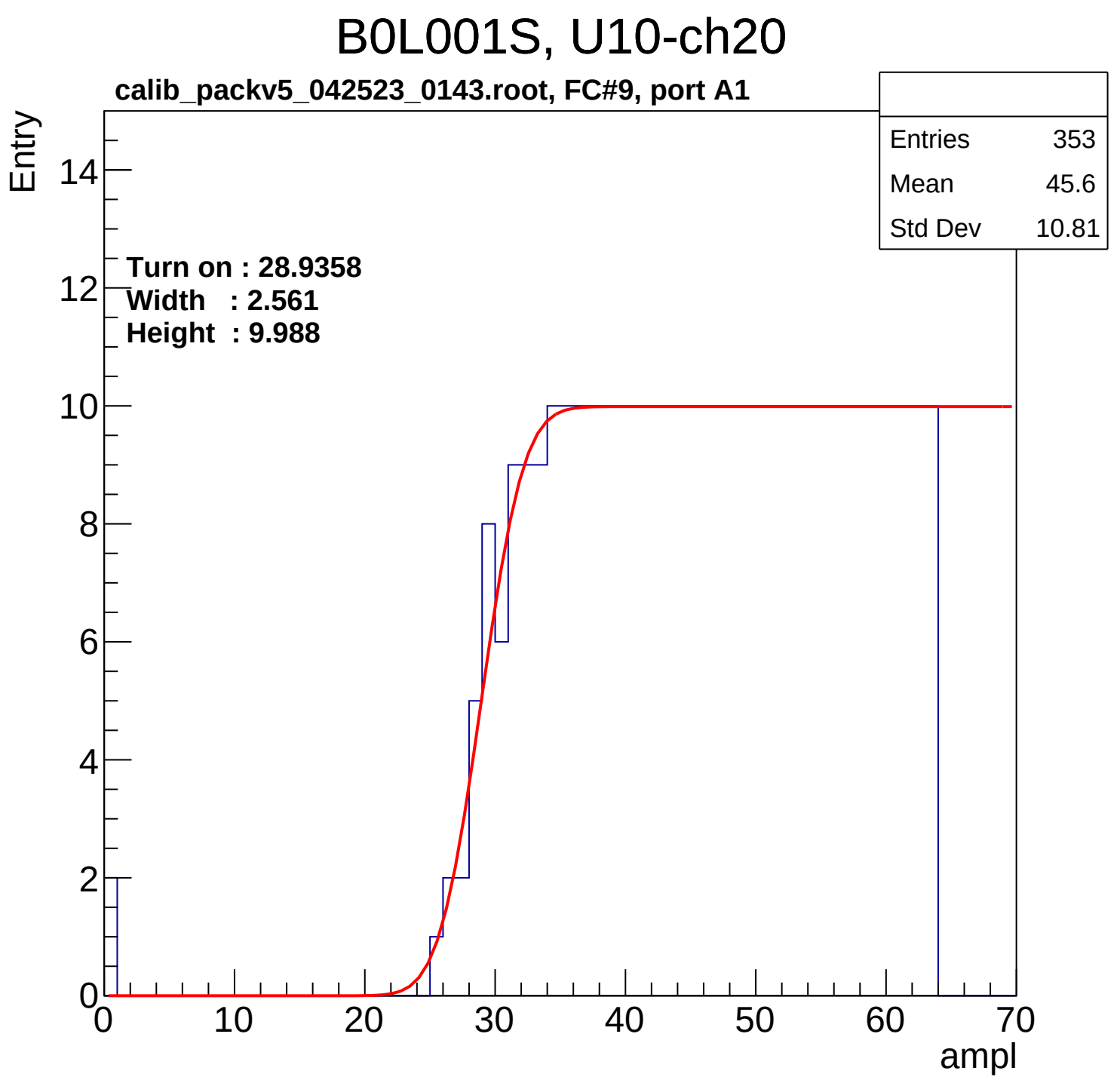

B0L001S, U10-ch15
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 45.38
Std Dev 10.75
Turn on : 28.9108
Width : 3.080
Height : 10.069
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

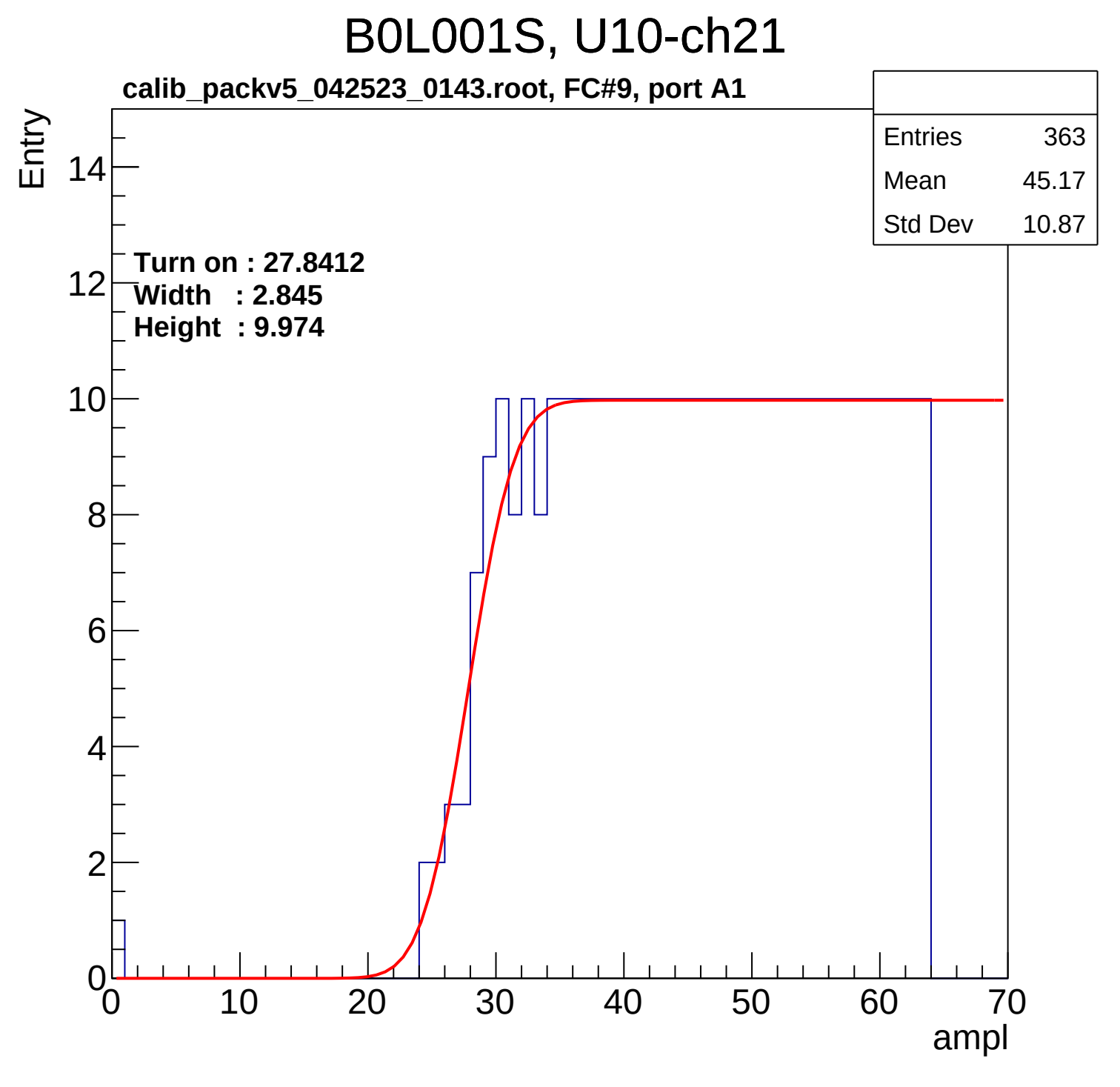

B0L001S, U10-ch16
calib_packv5_042523_0143.root, FC#9, port A1
Entries 392
Mean 43.64
Std Dev 11.93
Turn on : 25.1583
Width : 2.580
Height : 9.998
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

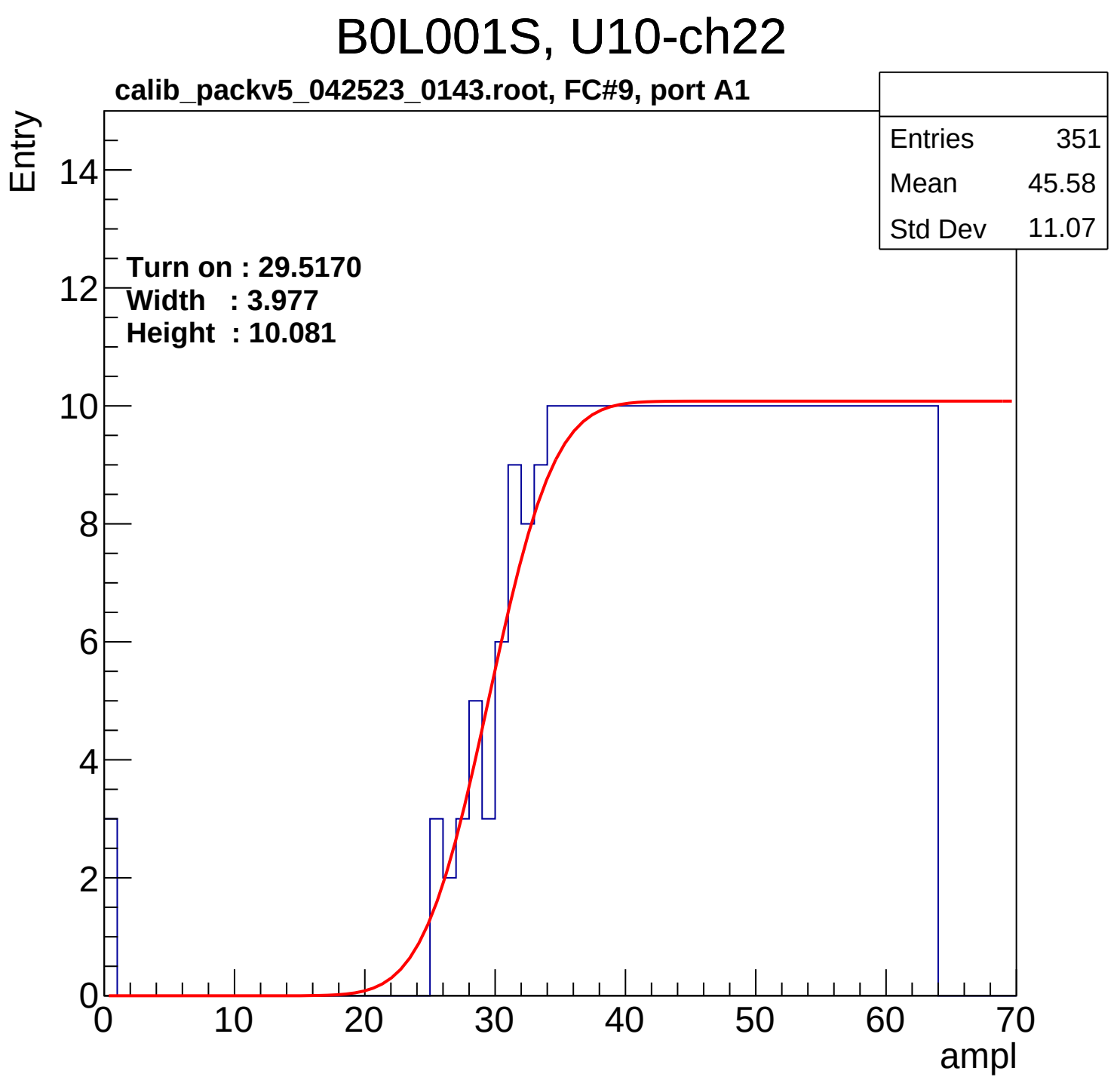

B0L001S, U10-ch17
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.98
Std Dev 11.02
Turn on : 27.6213
Width : 4.023
Height : 10.047
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

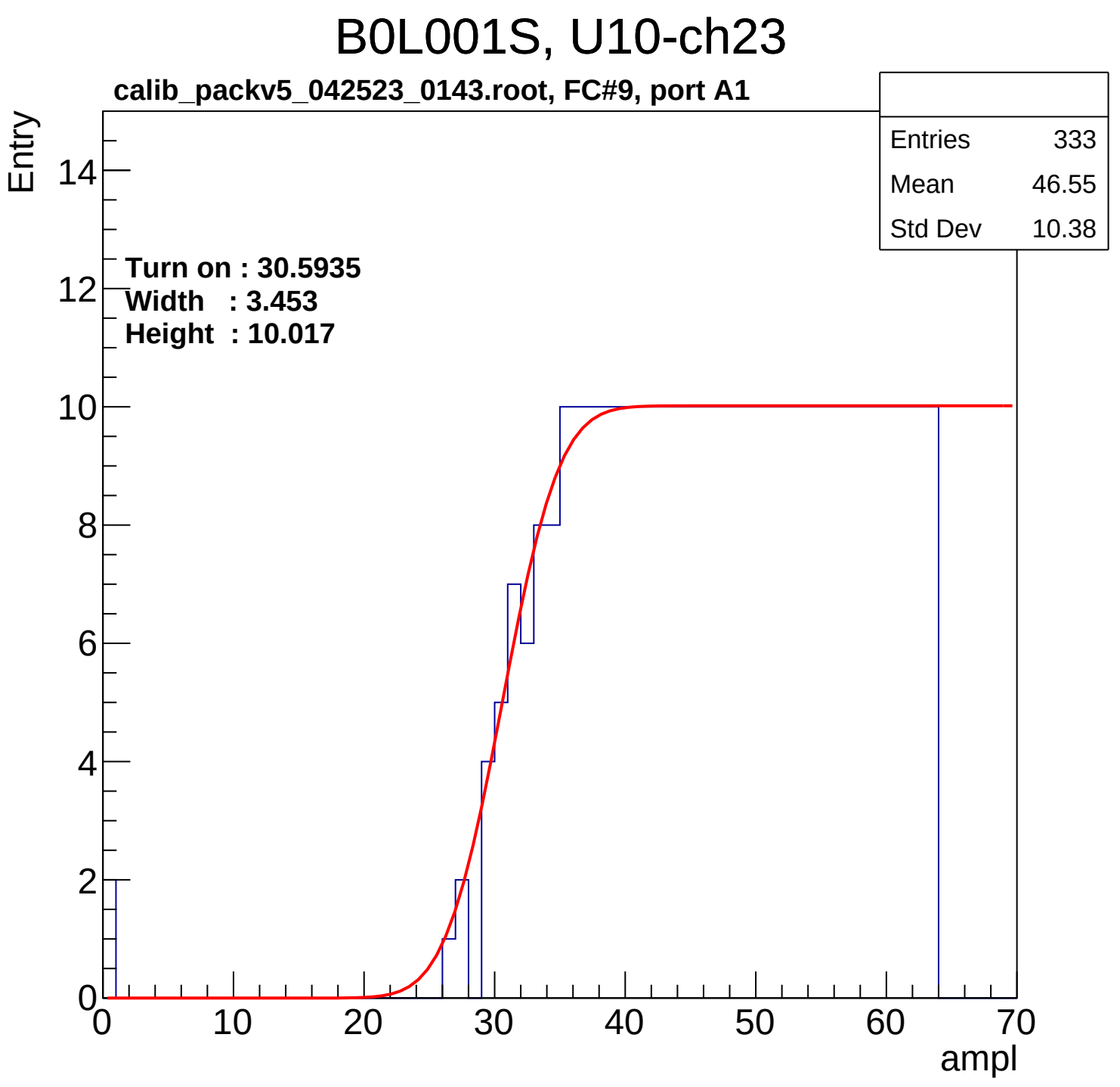

B0L001S, U10-ch18
calib_packv5_042523_0143.root, FC#9, port A1
Entries 347
Mean 45.89
Std Dev 10.67
Turn on : 29.6809
Width : 2.844
Height : 10.036
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

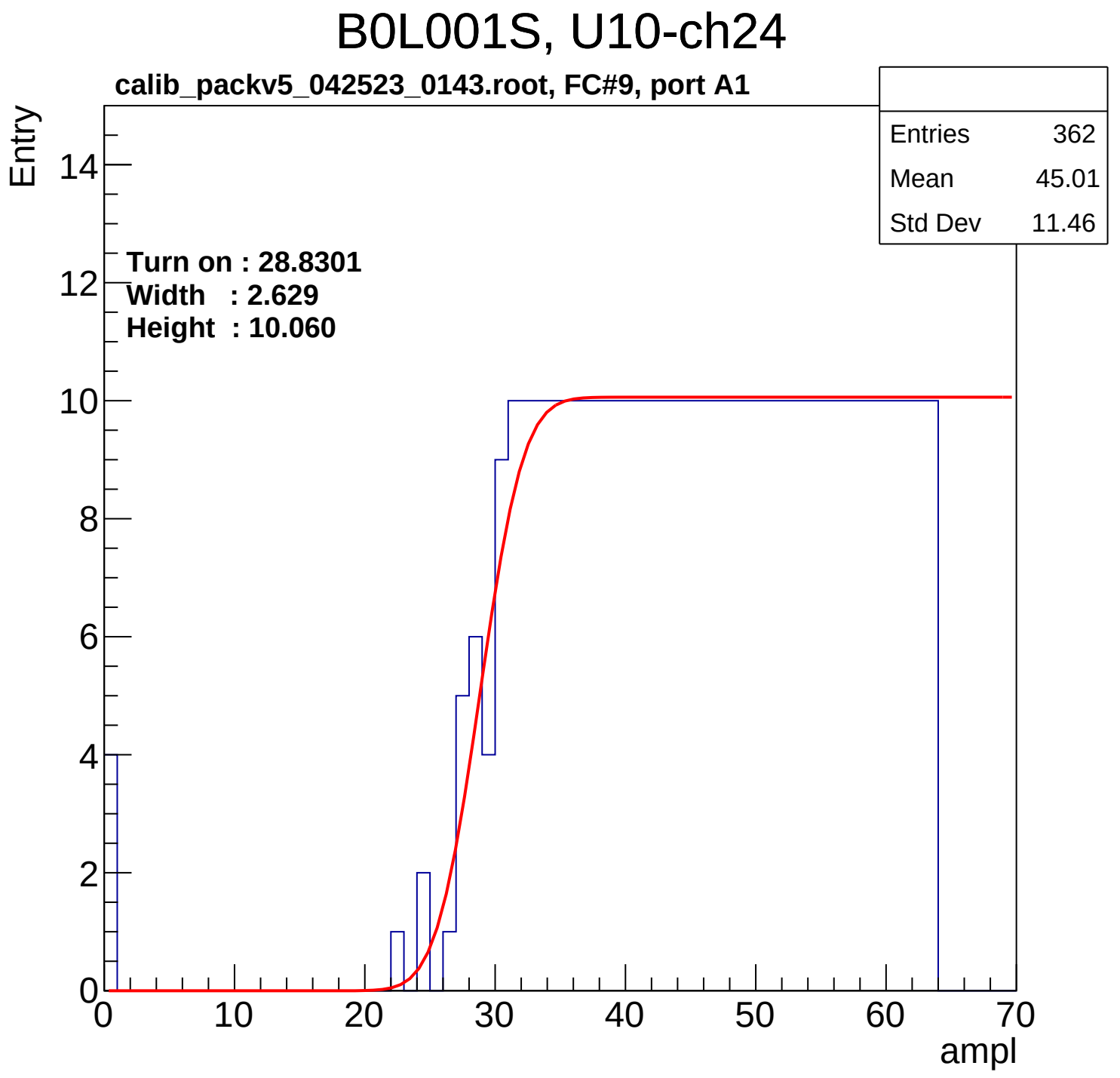

B0L001S, U10-ch19
calib_packv5_042523_0143.root, FC#9, port A1
Entries 355
Mean 45.48
Std Dev 10.9
Turn on : 29.2341
Width : 2.694
Height : 10.055
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

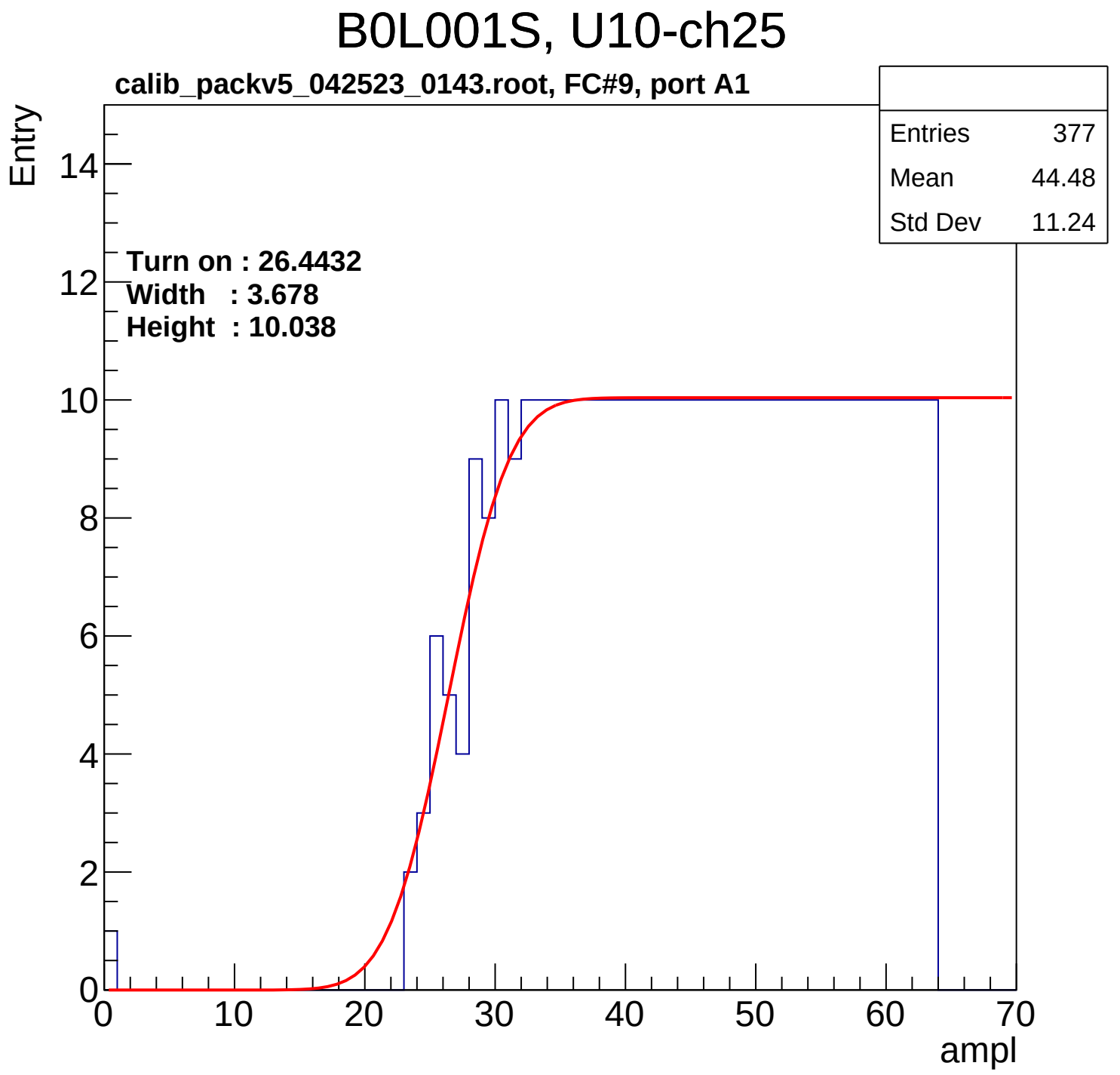

B0L001S, U10-ch20
calib_packv5_042523_0143.root, FC#9, port A1
Entries 353
Mean 45.6
Std Dev 10.81
Turn on : 28.9358
Width : 2.561
Height : 9.988
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

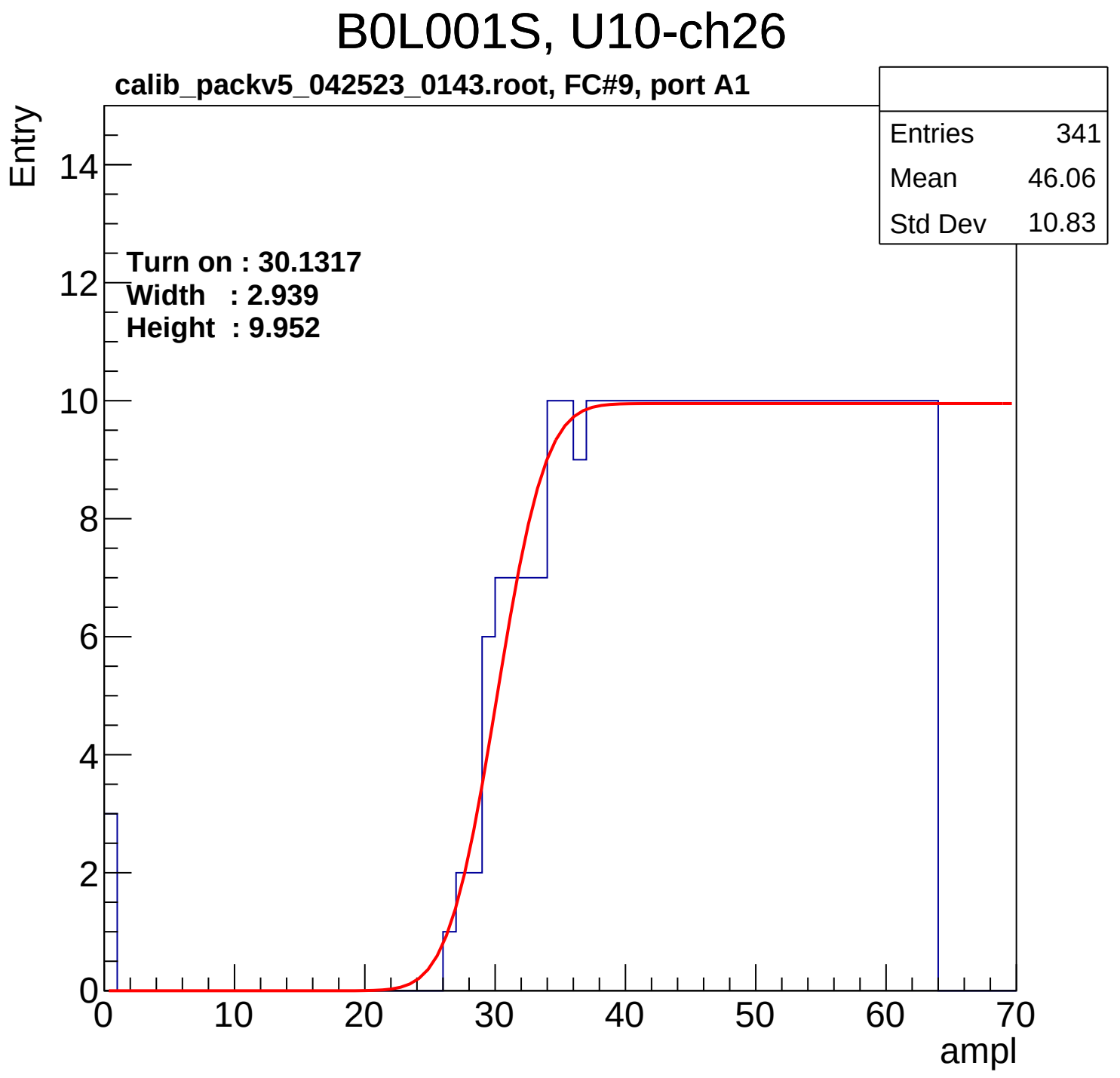

B0L001S, U10-ch21
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 45.17
Std Dev 10.87
Turn on : 27.8412
Width : 2.845
Height : 9.974
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

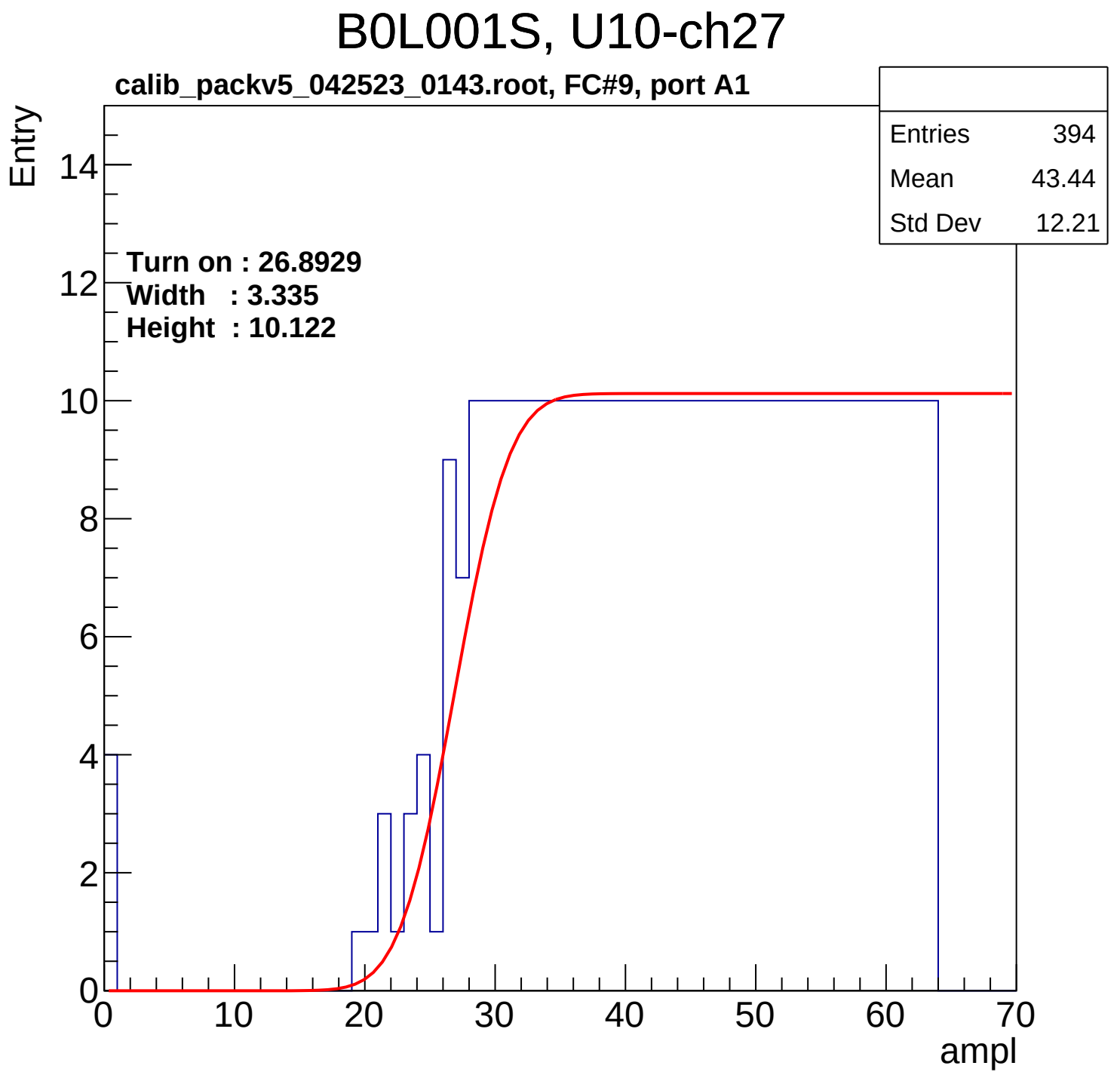

B0L001S, U10-ch22
calib_packv5_042523_0143.root, FC#9, port A1
Entries 351
Mean 45.58
Std Dev 11.07
Turn on : 29.5170
Width : 3.977
Height : 10.081
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

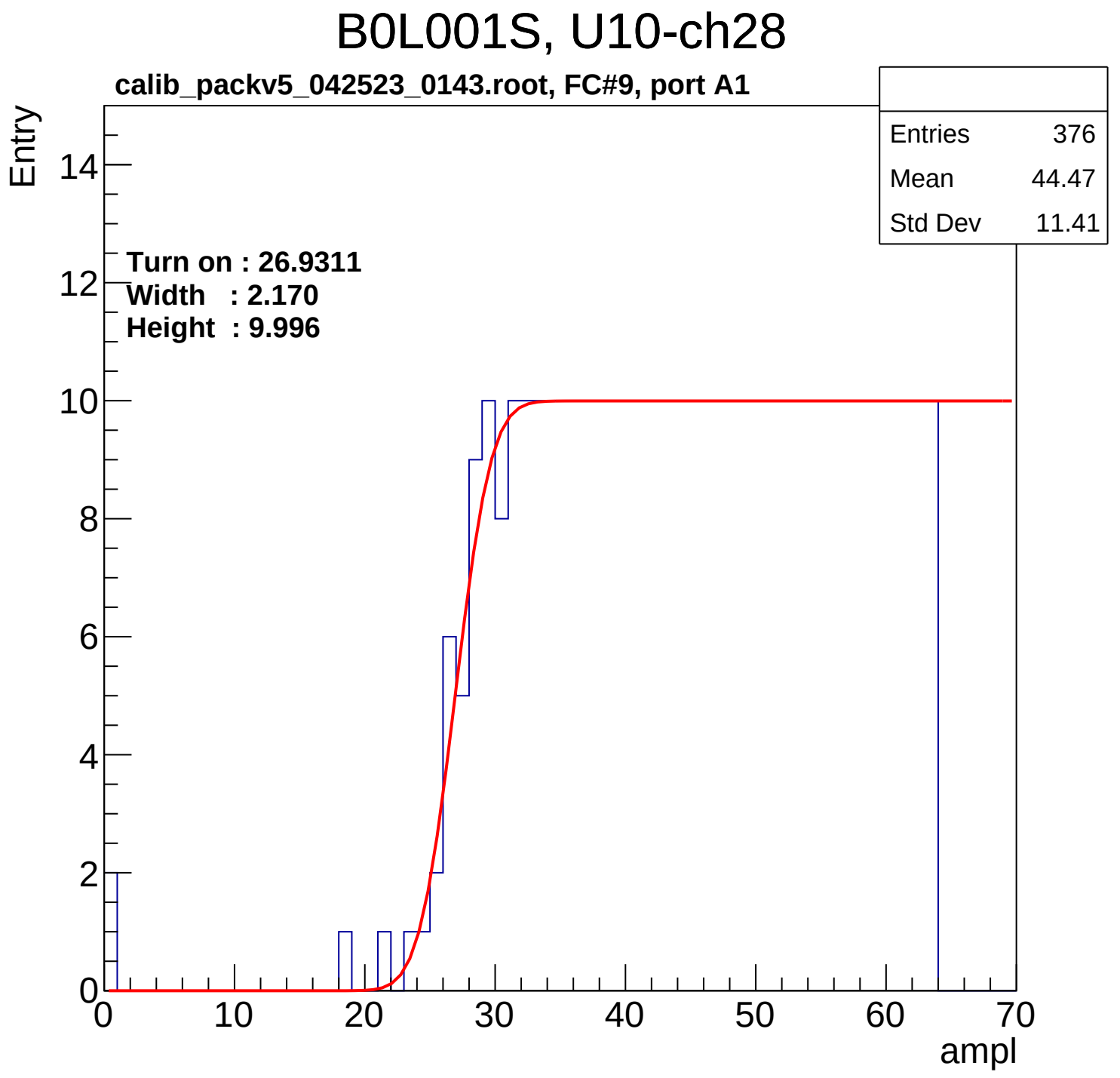

B0L001S, U10-ch23
calib_packv5_042523_0143.root, FC#9, port A1
Entries 333
Mean 46.55
Std Dev 10.38
Turn on : 30.5935
Width : 3.453
Height : 10.017
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

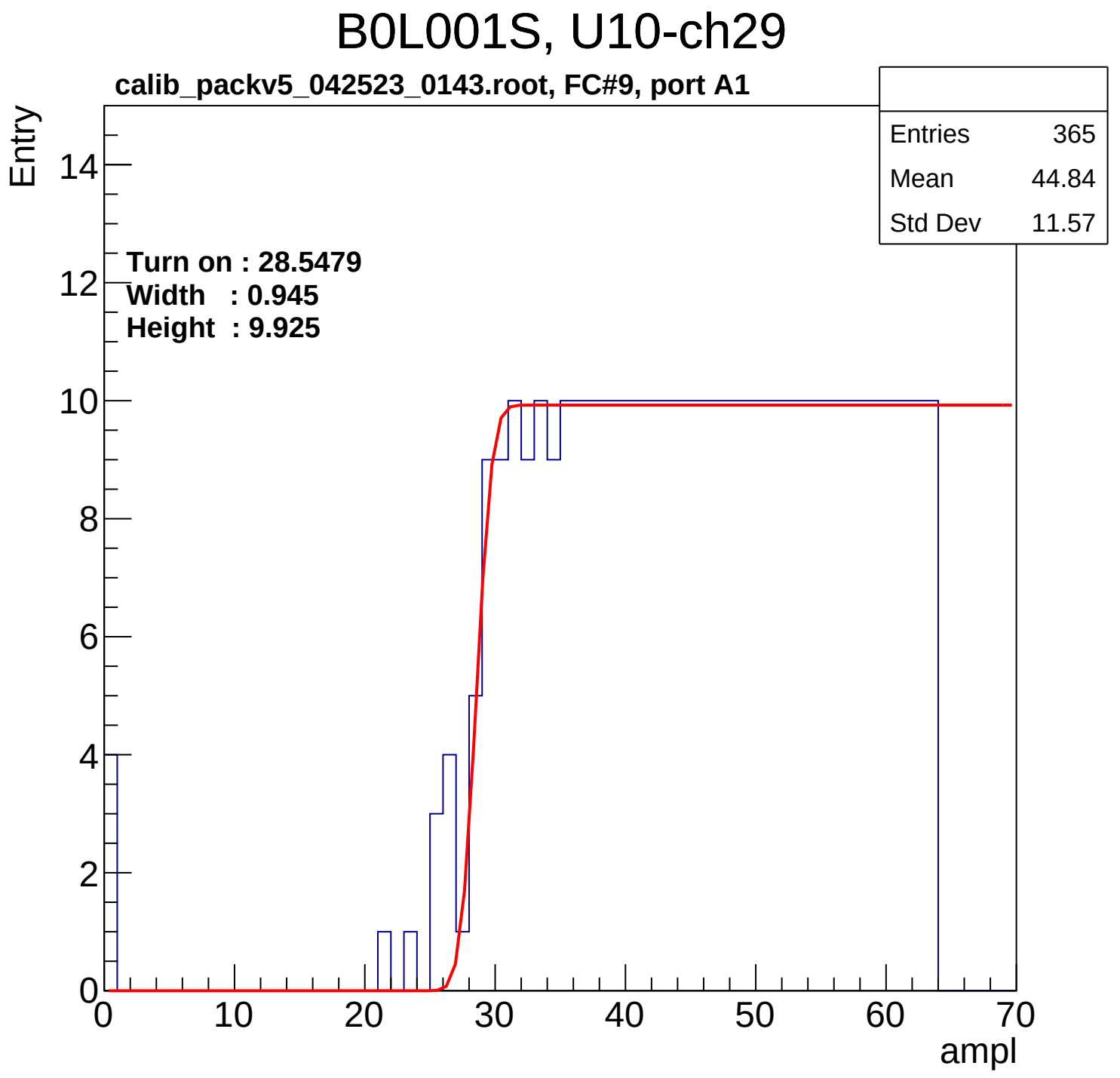

B0L001S, U10-ch24
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 45.01
Std Dev 11.46
Turn on : 28.8301
Width : 2.629
Height : 10.060
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

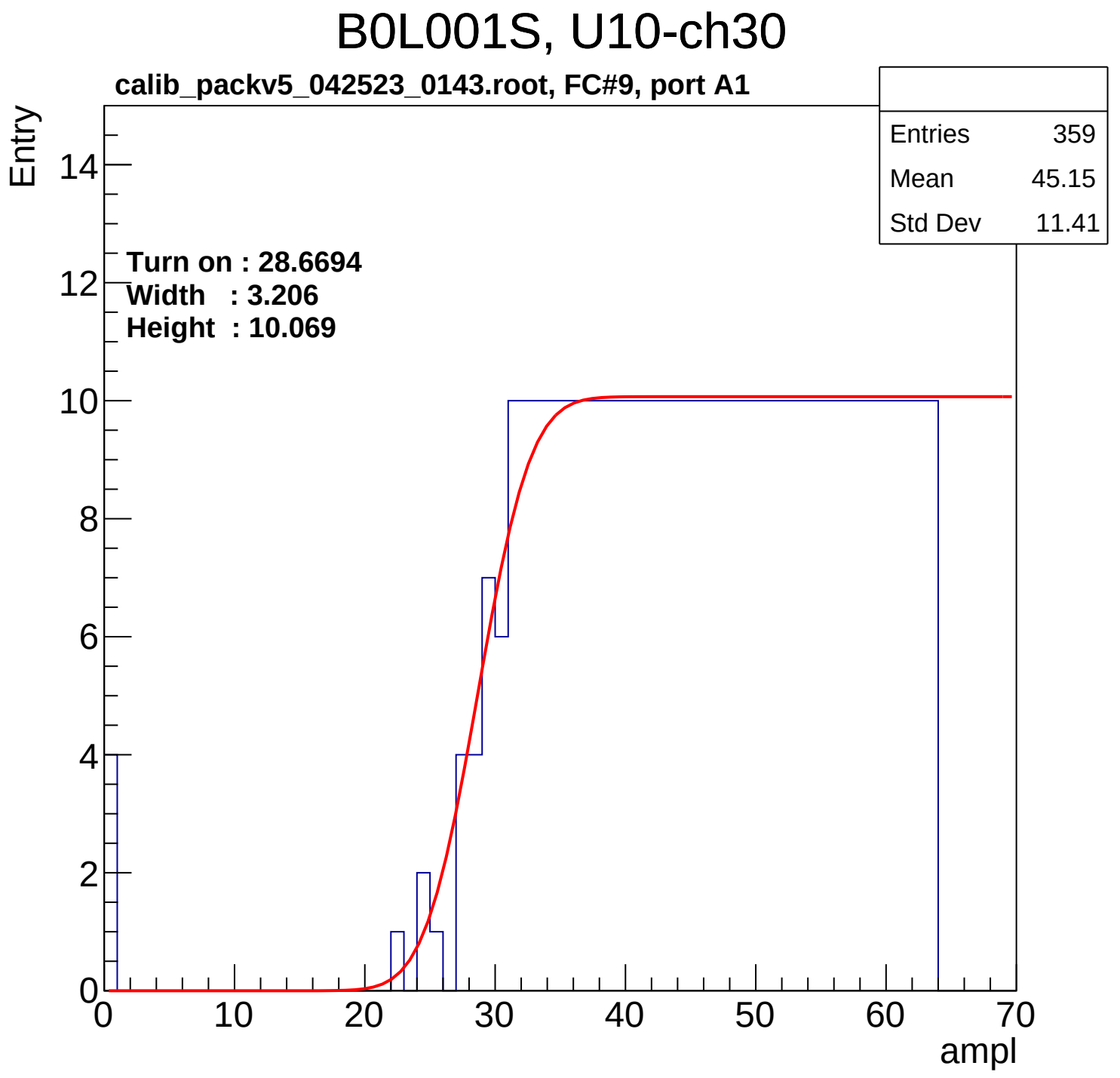

B0L001S, U10-ch25
calib_packv5_042523_0143.root, FC#9, port A1
Entries 377
Mean 44.48
Std Dev 11.24
Turn on : 26.4432
Width : 3.678
Height : 10.038
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

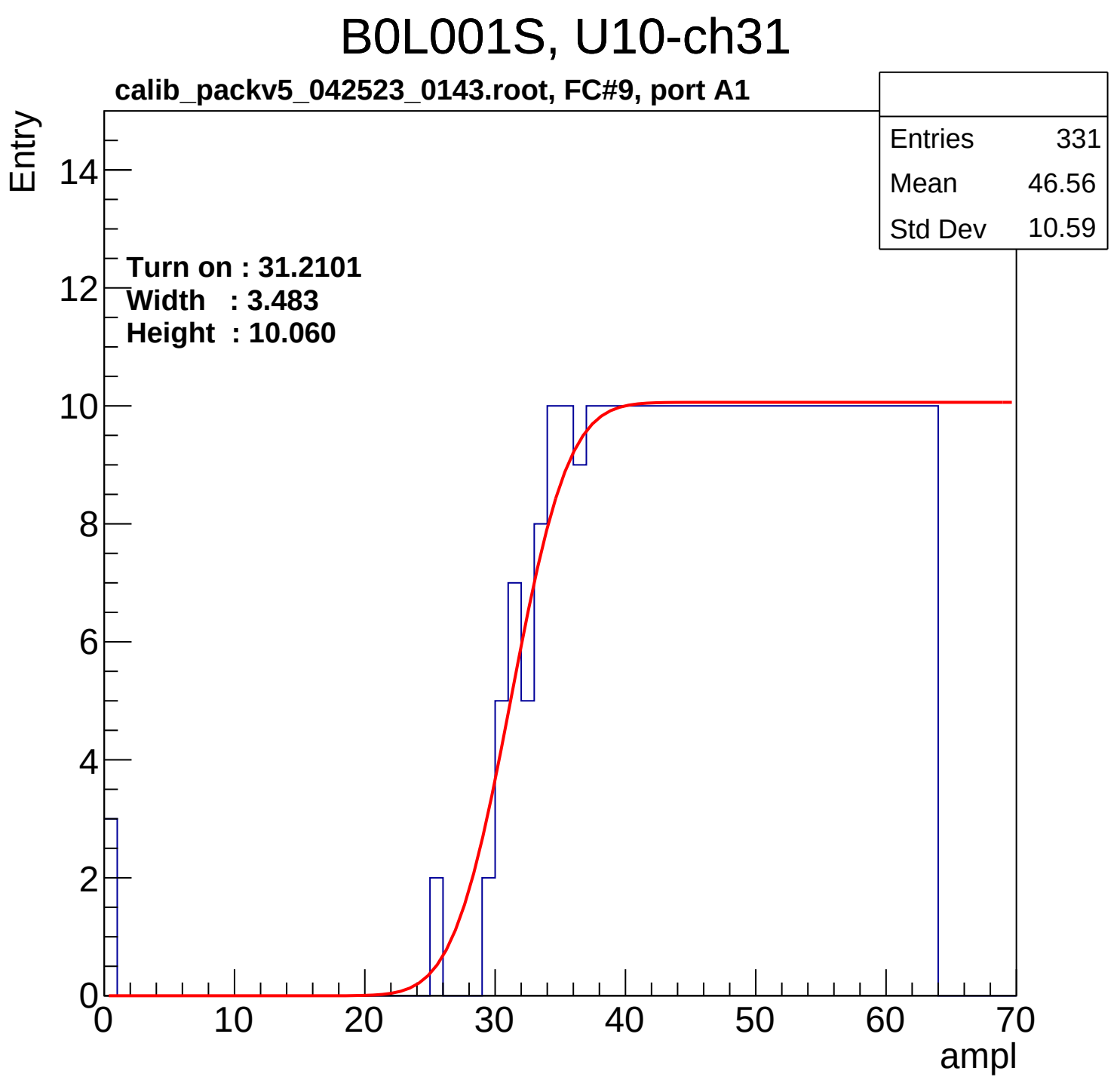

B0L001S, U10-ch26
calib_packv5_042523_0143.root, FC#9, port A1
Entries 341
Mean 46.06
Std Dev 10.83
Turn on : 30.1317
Width : 2.939
Height : 9.952
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

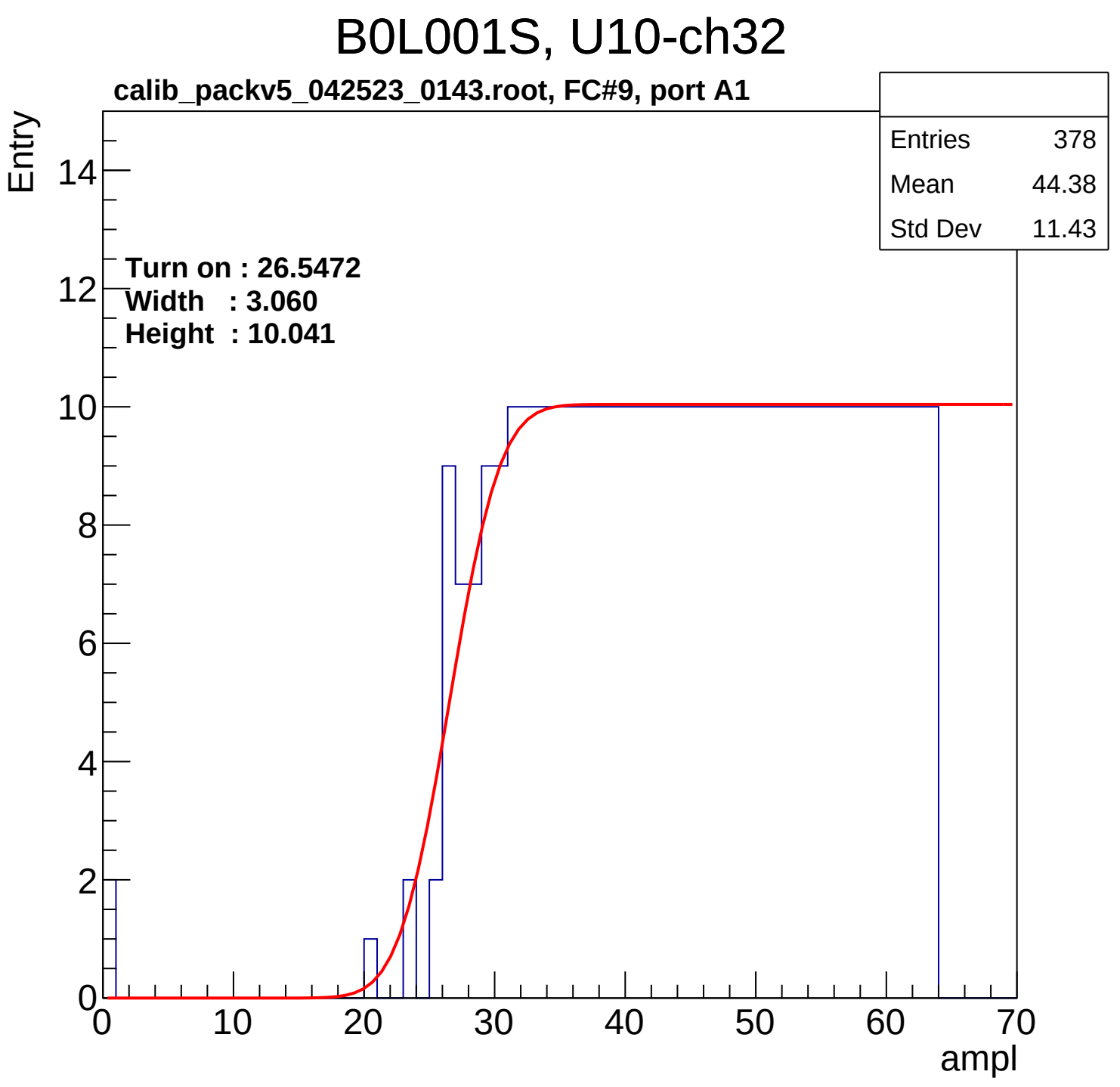

B0L001S, U10-ch27
calib_packv5_042523_0143.root, FC#9, port A1
Entries 394
Mean 43.44
Std Dev 12.21
Turn on : 26.8929
Width : 3.335
Height : 10.122
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

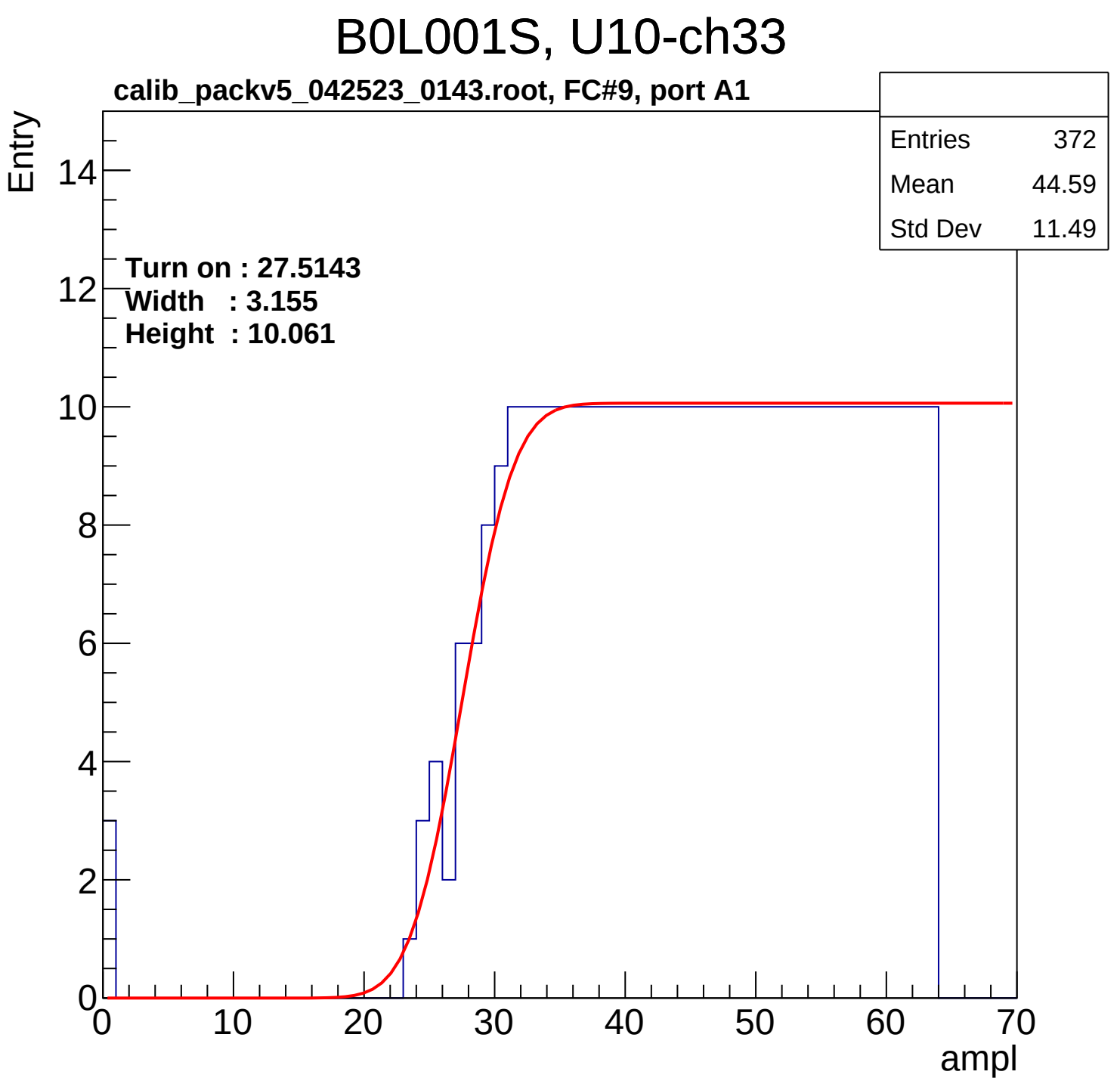

B0L001S, U10-ch28
calib_packv5_042523_0143.root, FC#9, port A1
Entries 376
Mean 44.47
Std Dev 11.41
Turn on : 26.9311
Width : 2.170
Height : 9.996
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

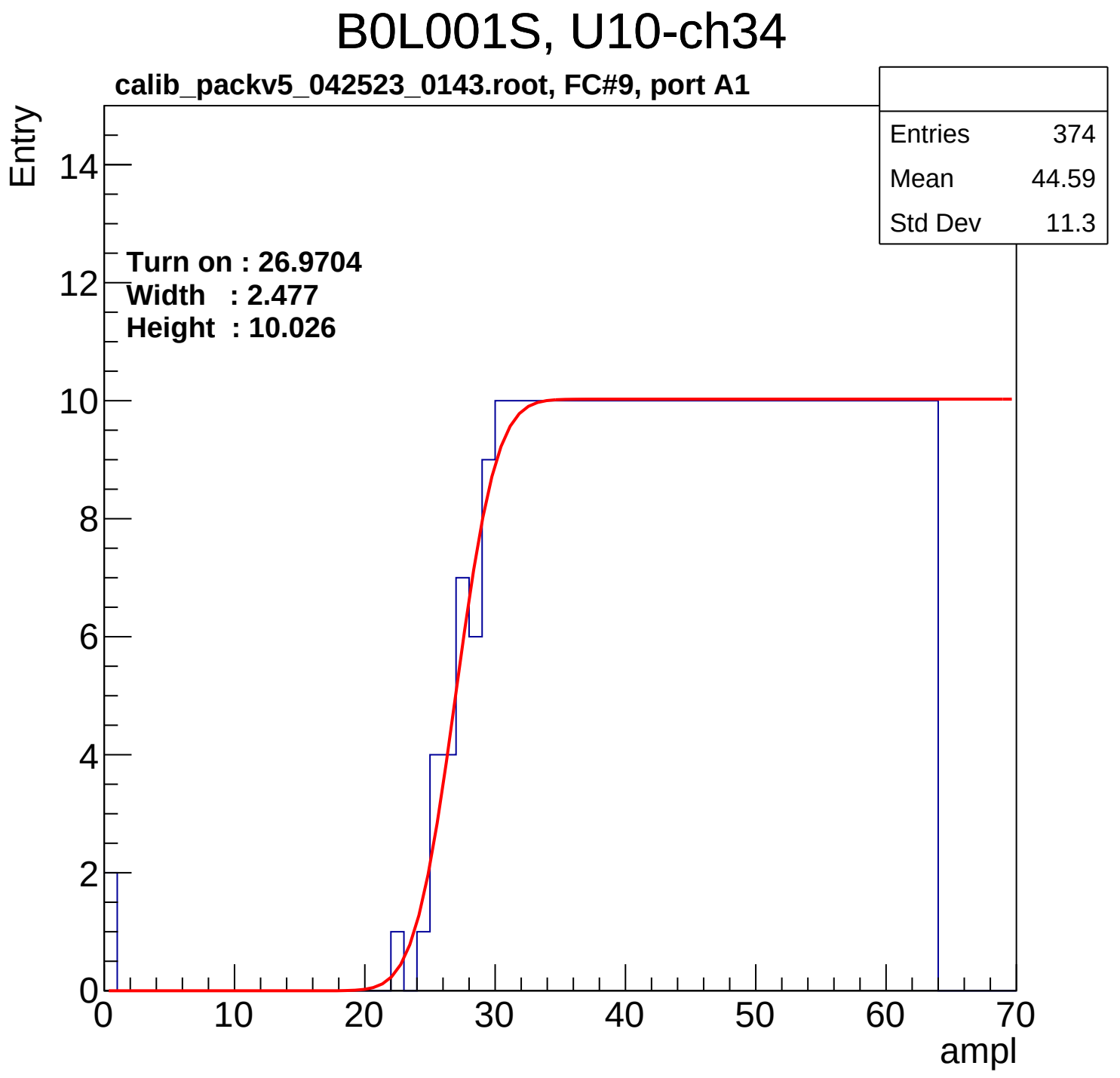

B0L001S, U10-ch29
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 44.84
Std Dev 11.57
Turn on : 28.5479
Width : 0.945
Height : 9.925
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

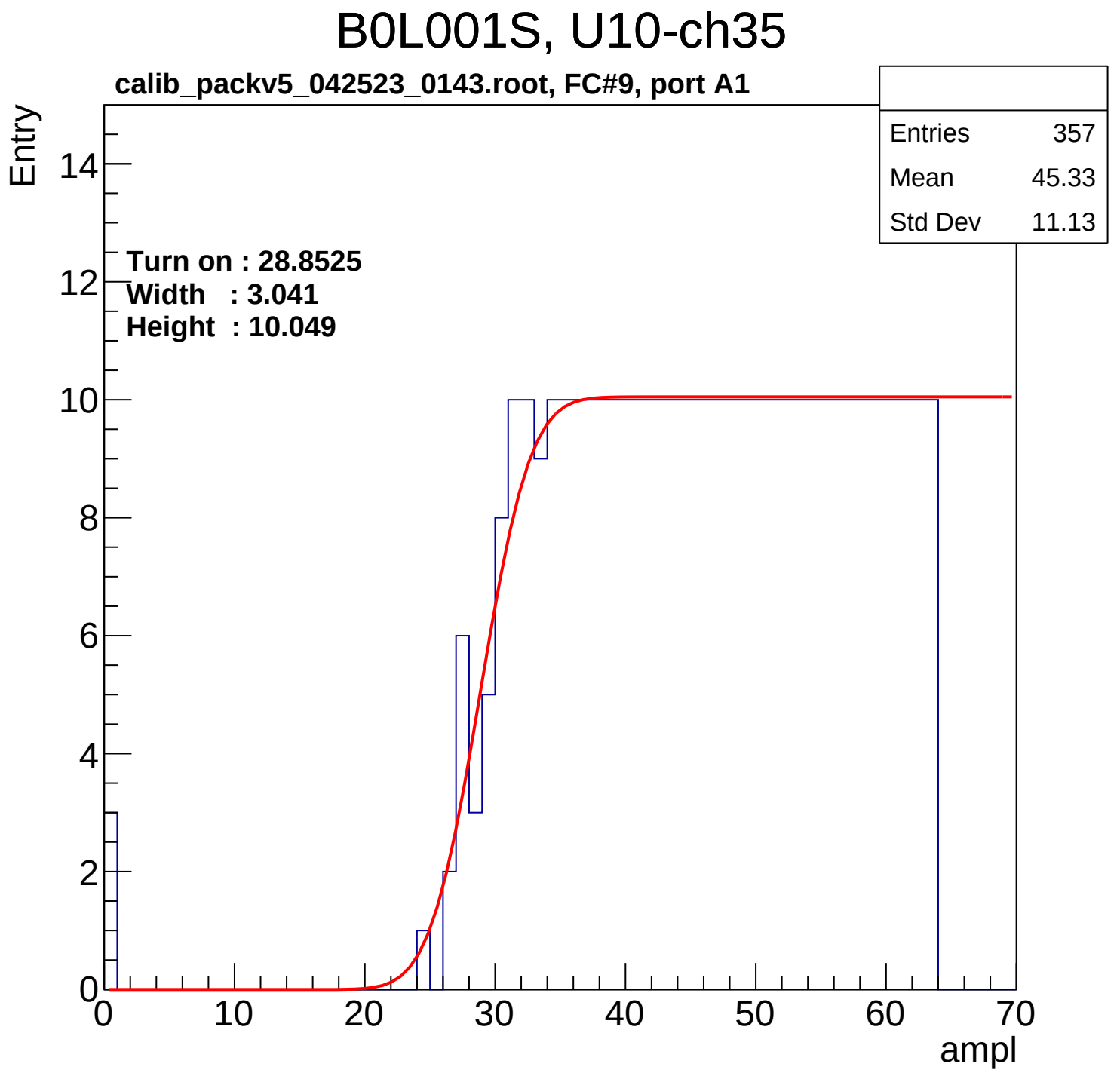

B0L001S, U10-ch30
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 45.15
Std Dev 11.41
Turn on : 28.6694
Width : 3.206
Height : 10.069
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

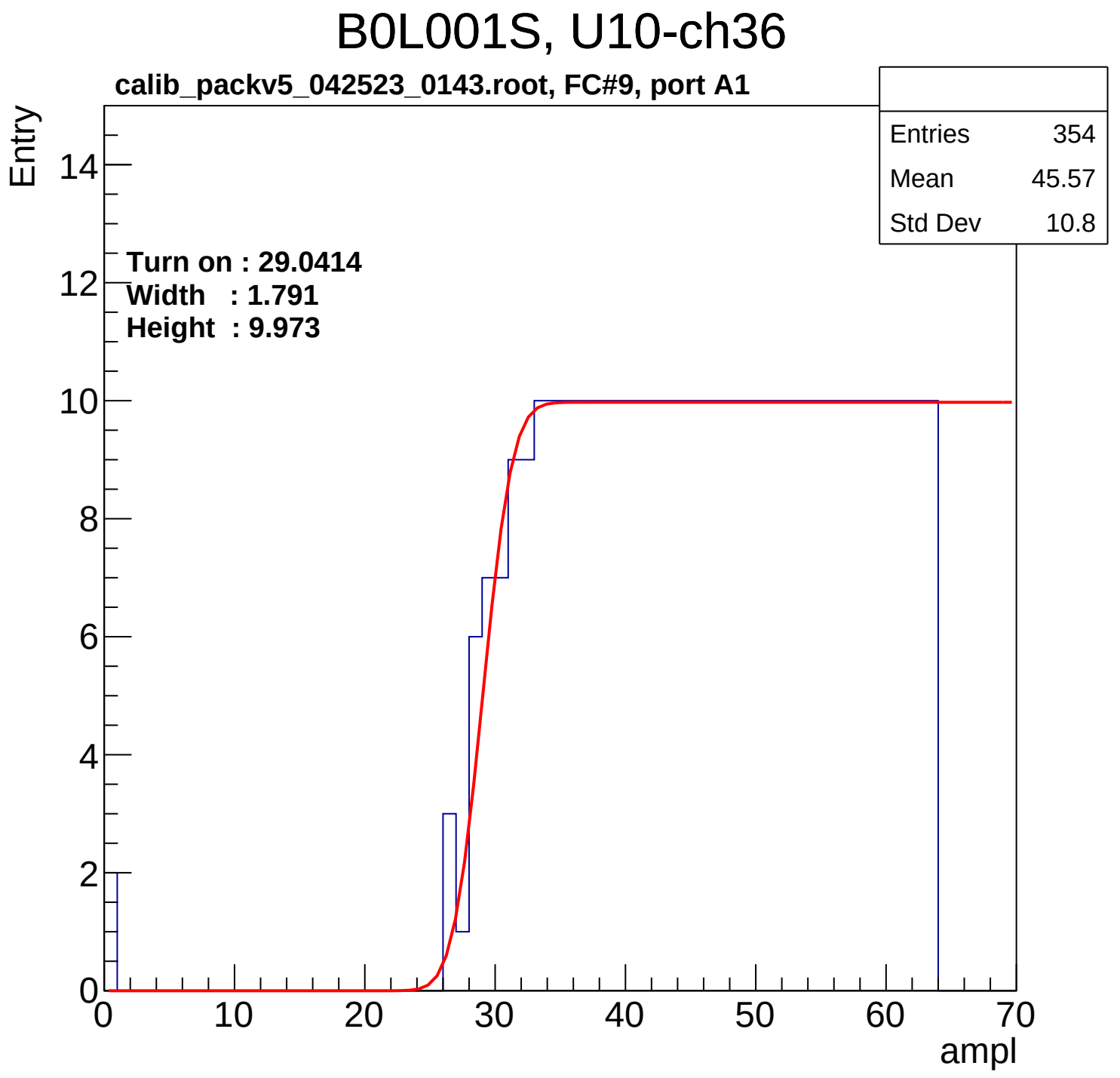

B0L001S, U10-ch31
calib_packv5_042523_0143.root, FC#9, port A1
Entries 331
Mean 46.56
Std Dev 10.59
Turn on : 31.2101
Width : 3.483
Height : 10.060
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

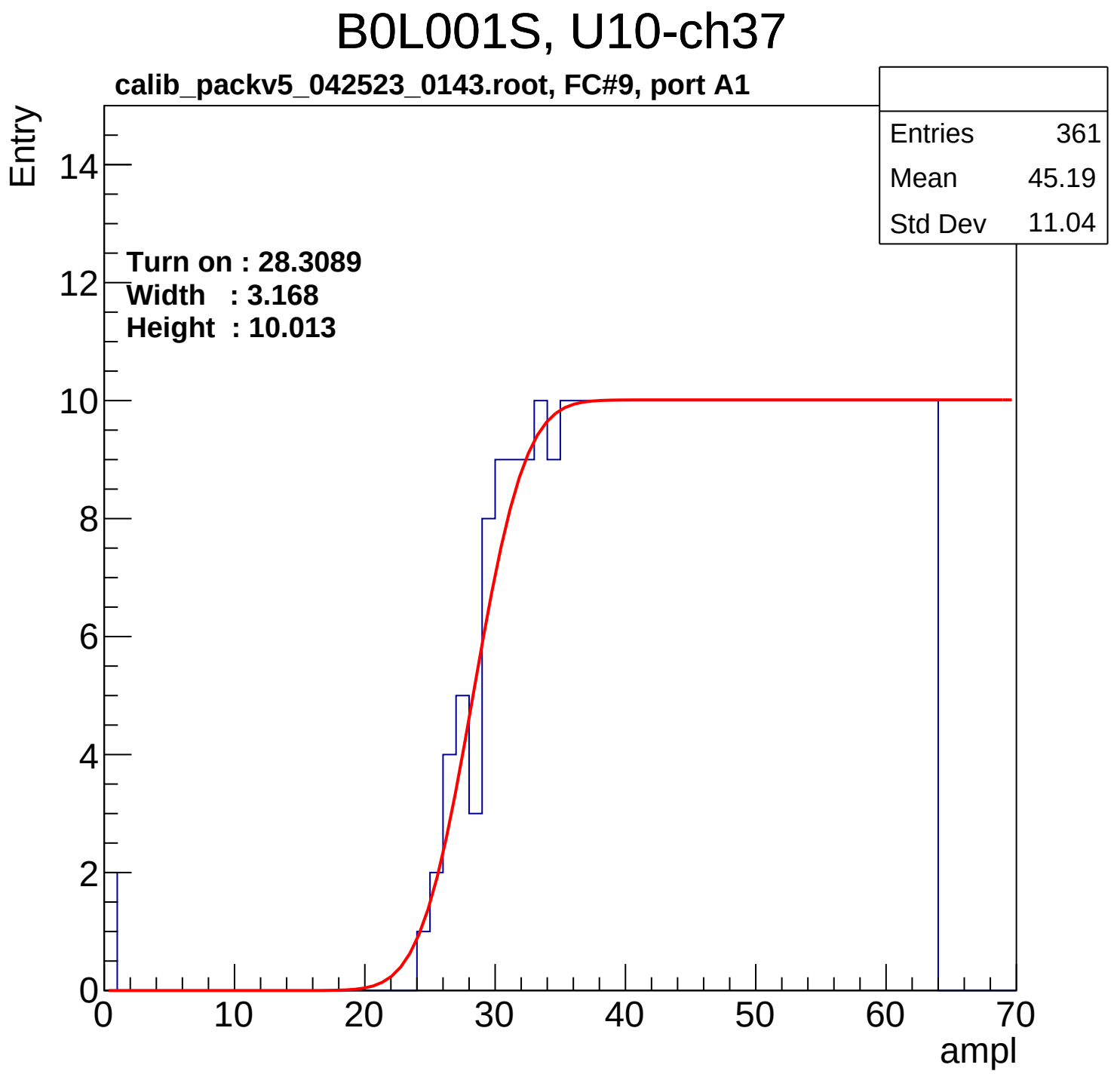

B0L001S, U10-ch32
calib_packv5_042523_0143.root, FC#9, port A1
Entries 378
Mean 44.38
Std Dev 11.43
Turn on : 26.5472
Width : 3.060
Height : 10.041
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

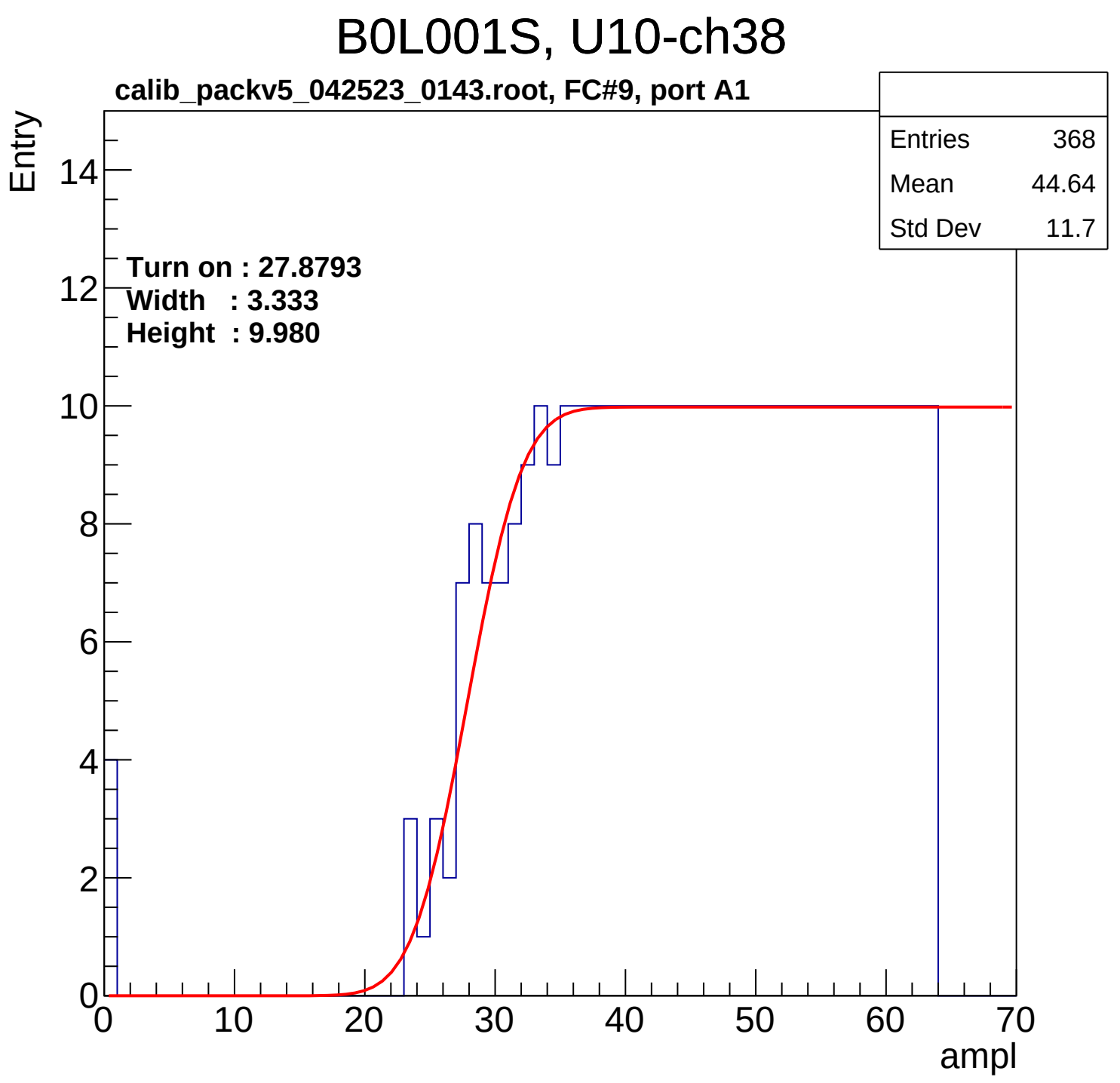

B0L001S, U10-ch33
calib_packv5_042523_0143.root, FC#9, port A1
Entries 372
Mean 44.59
Std Dev 11.49
Turn on : 27.5143
Width : 3.155
Height : 10.061
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

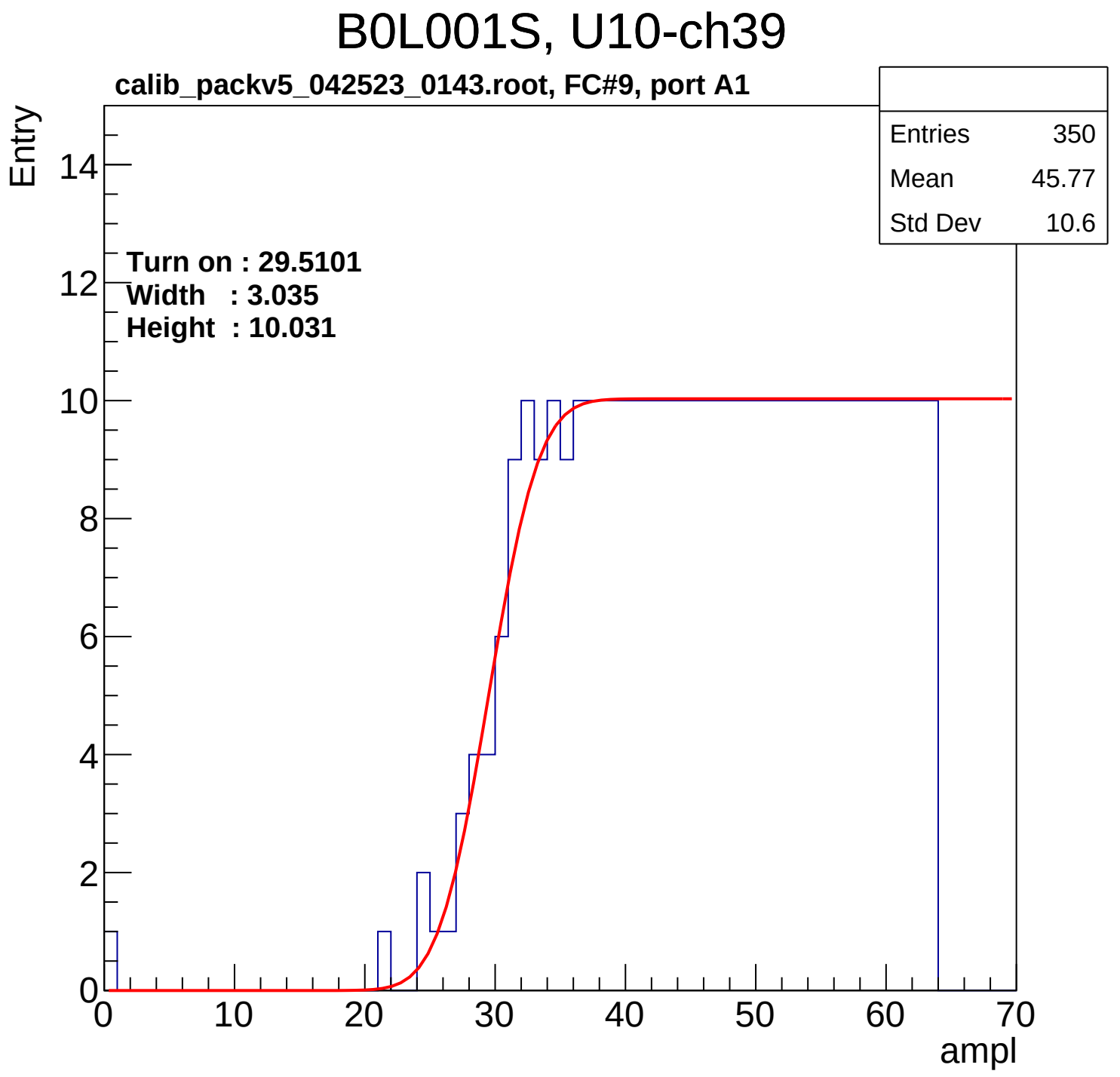

B0L001S, U10-ch34
calib_packv5_042523_0143.root, FC#9, port A1
Entries 374
Mean 44.59
Std Dev 11.3
Turn on : 26.9704
Width : 2.477
Height : 10.026
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

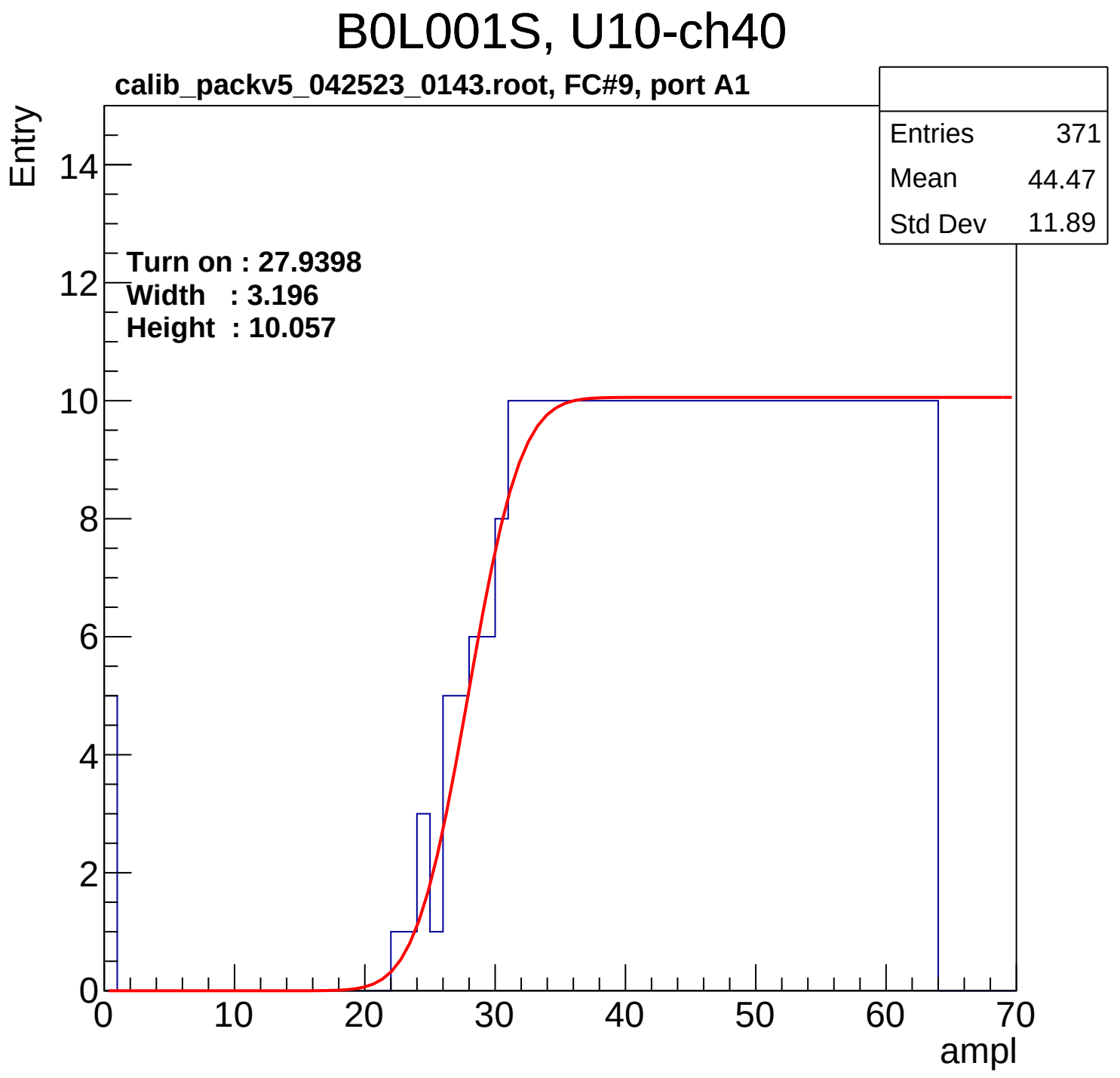

B0L001S, U10-ch35
calib_packv5_042523_0143.root, FC#9, port A1
Entries 357
Mean 45.33
Std Dev 11.13
Turn on : 28.8525
Width : 3.041
Height : 10.049
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

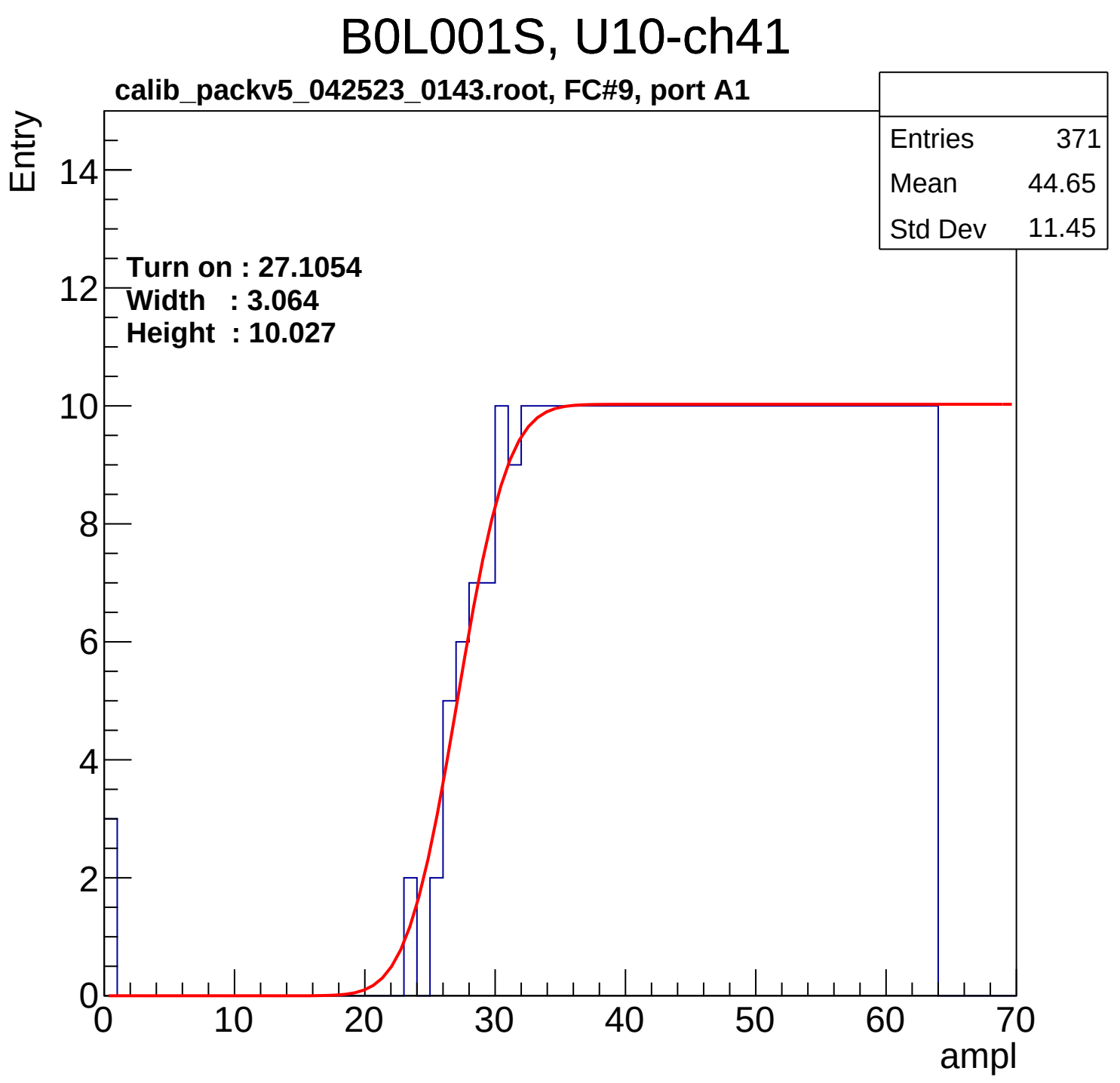

B0L001S, U10-ch36
calib_packv5_042523_0143.root, FC#9, port A1
Entries 354
Mean 45.57
Std Dev 10.8
Turn on : 29.0414
Width : 1.791
Height : 9.973
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

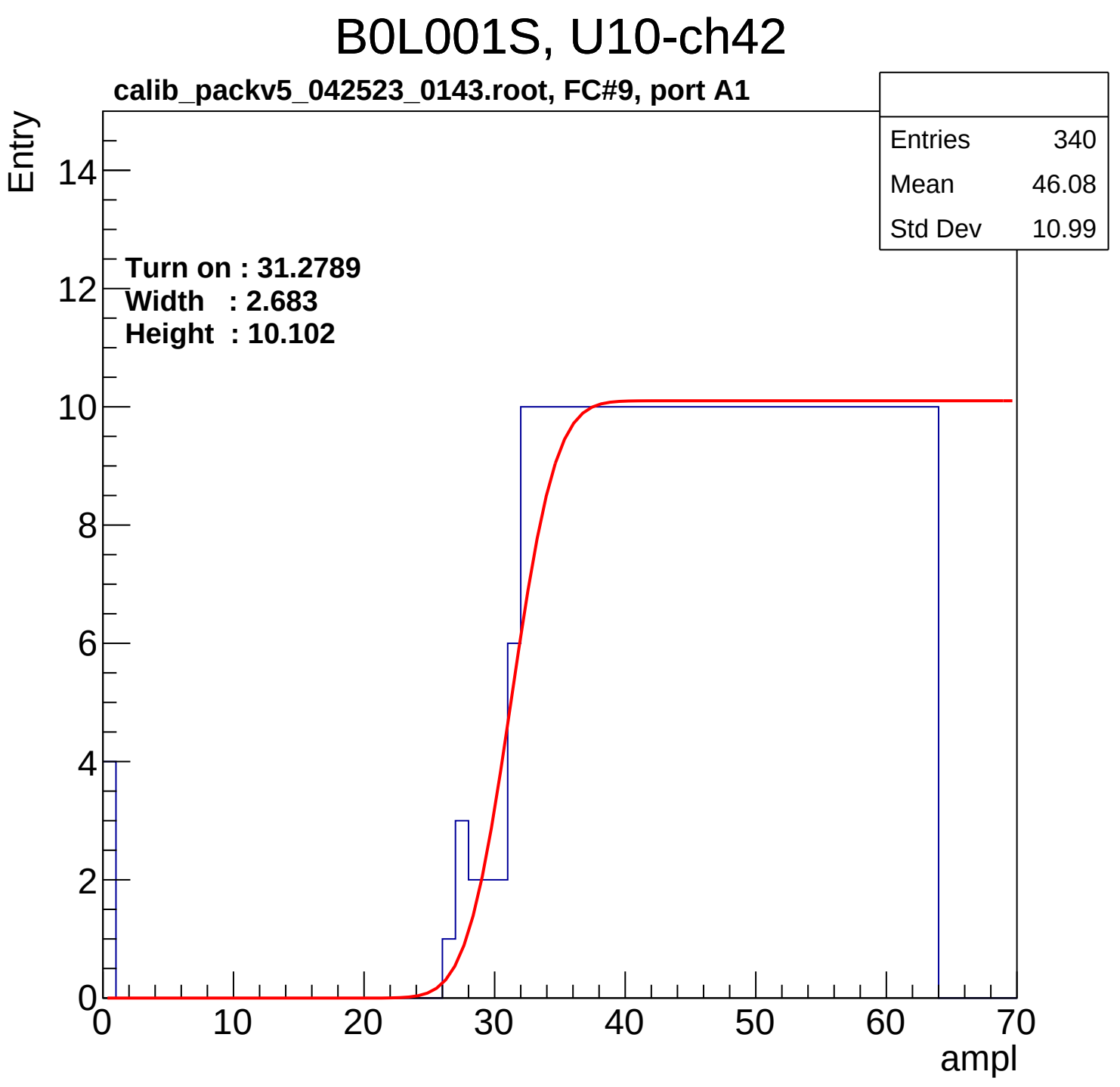

B0L001S, U10-ch37
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 45.19
Std Dev 11.04
Turn on : 28.3089
Width : 3.168
Height : 10.013
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

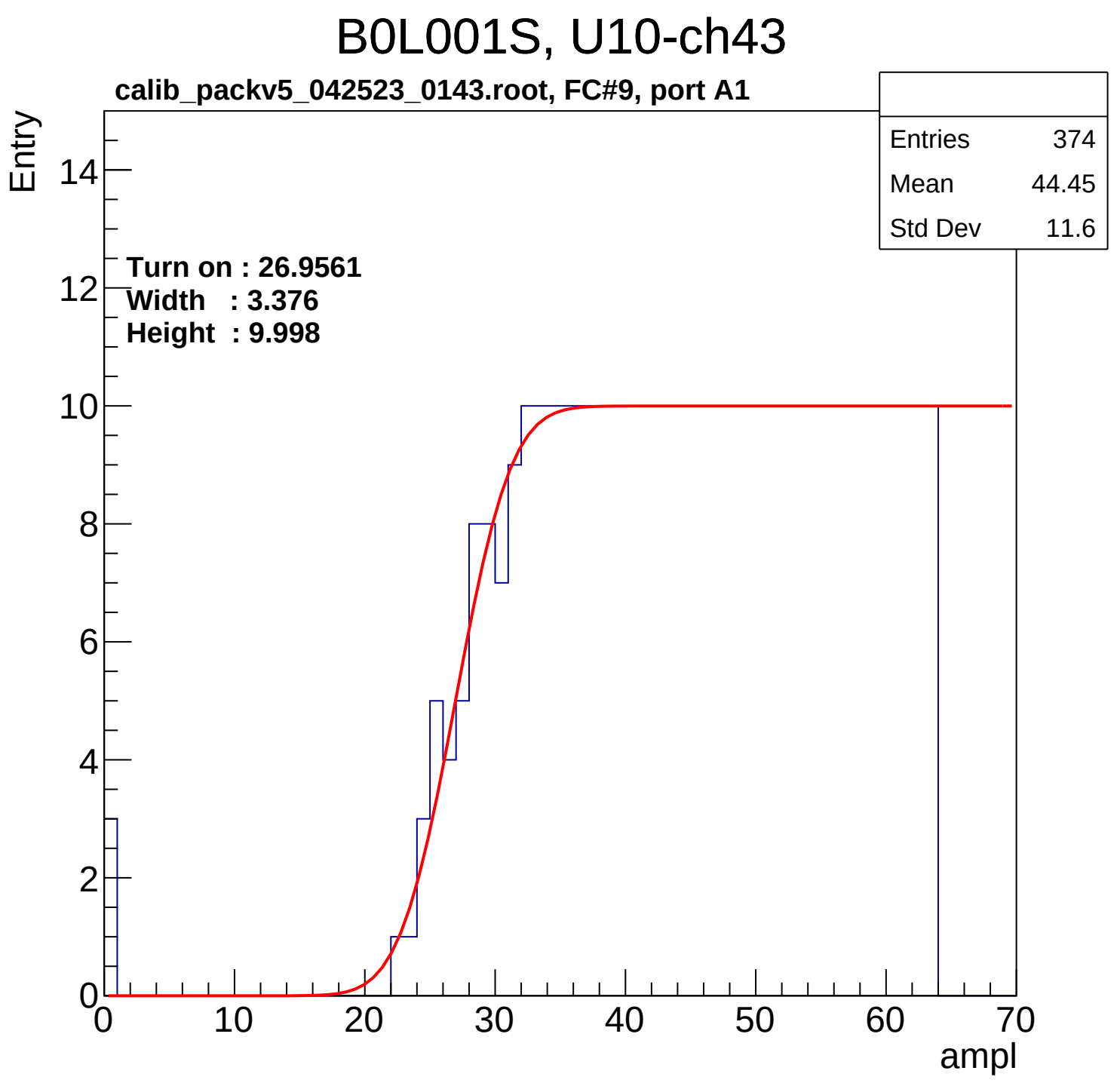

B0L001S, U10-ch38
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.64
Std Dev 11.7
Turn on : 27.8793
Width : 3.333
Height : 9.980
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

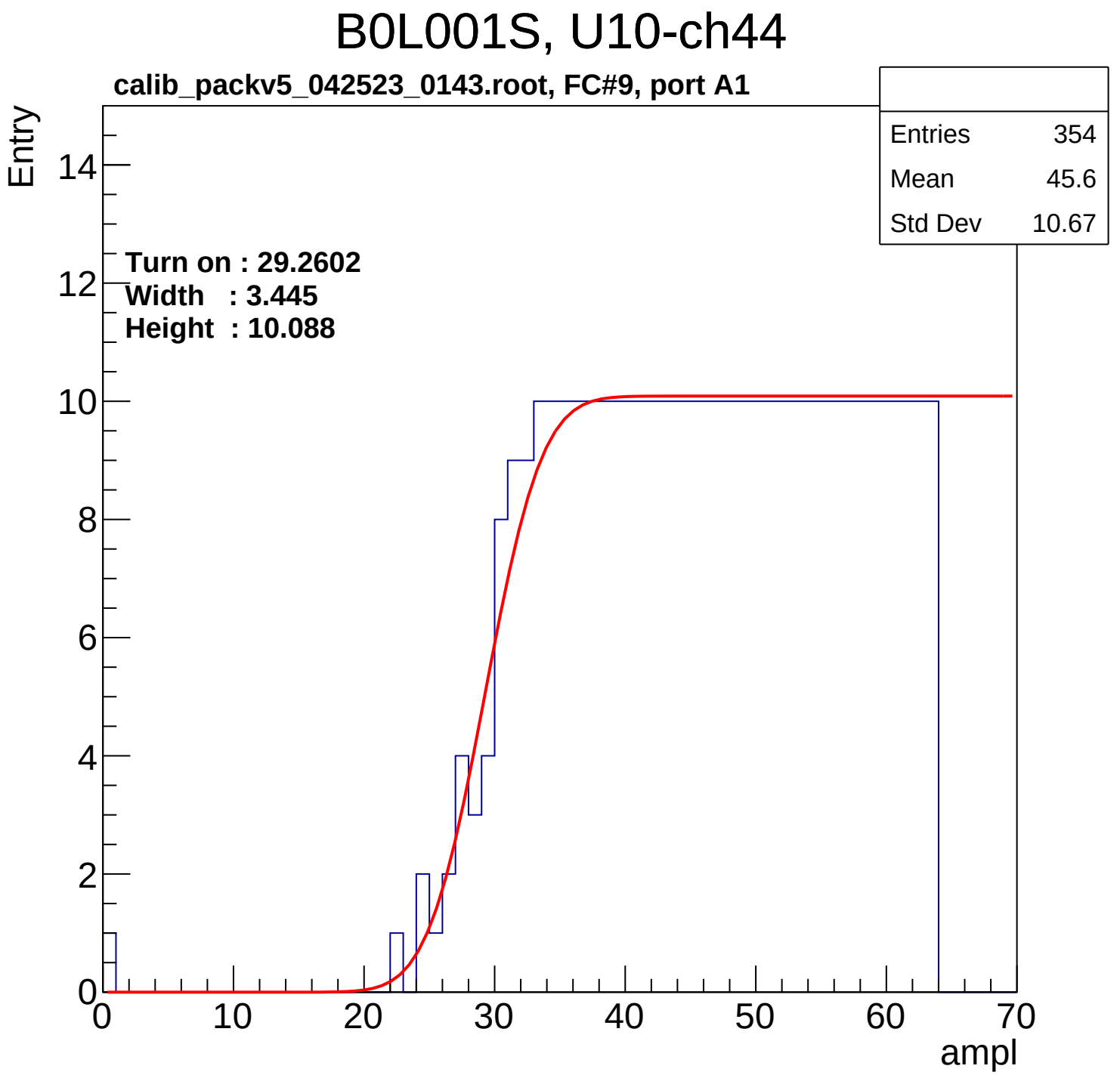

B0L001S, U10-ch39
calib_packv5_042523_0143.root, FC#9, port A1
Entries 350
Mean 45.77
Std Dev 10.6
Turn on : 29.5101
Width : 3.035
Height : 10.031
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

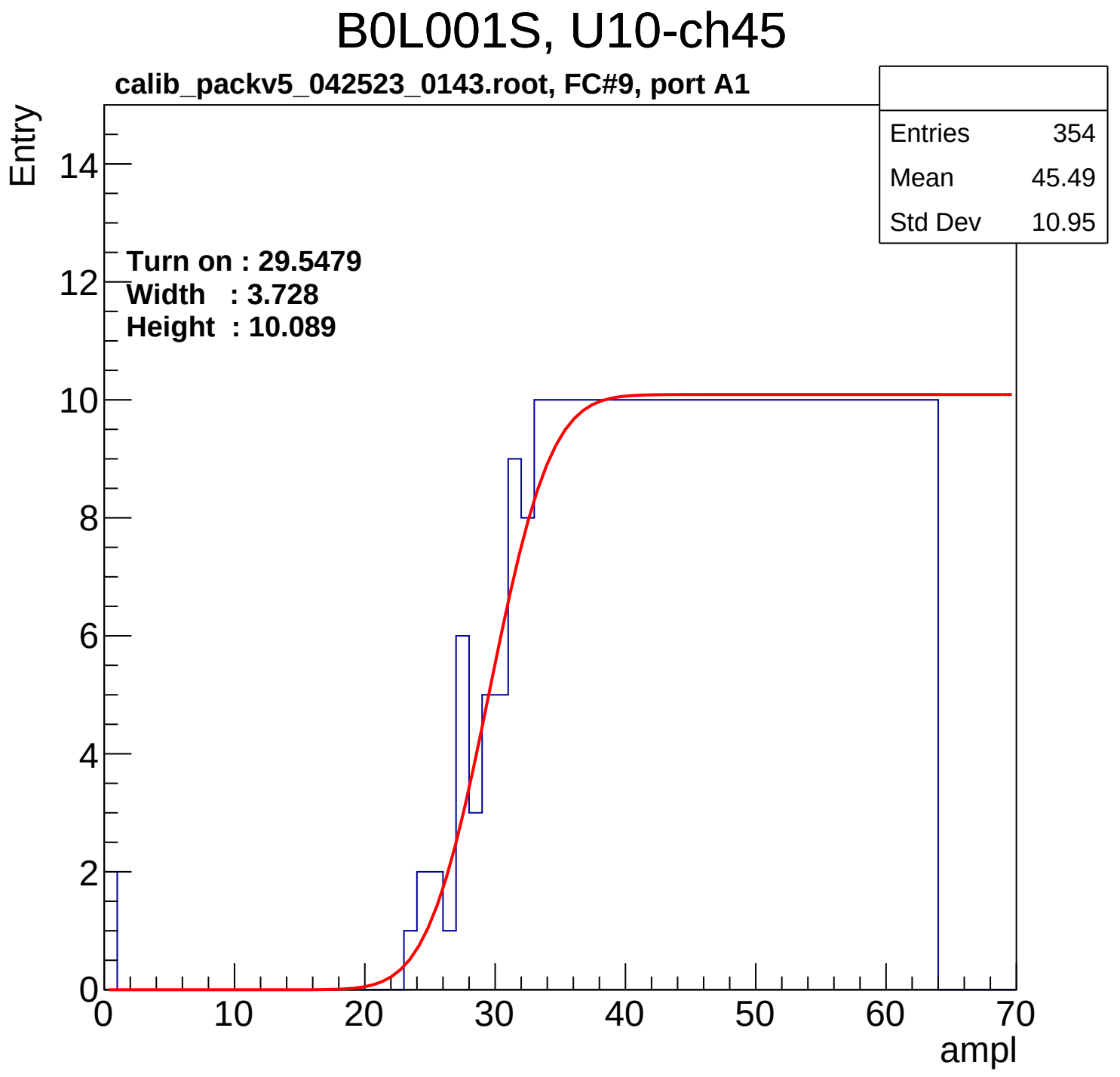

B0L001S, U10-ch40
calib_packv5_042523_0143.root, FC#9, port A1
Entries 371
Mean 44.47
Std Dev 11.89
Turn on : 27.9398
Width : 3.196
Height : 10.057
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

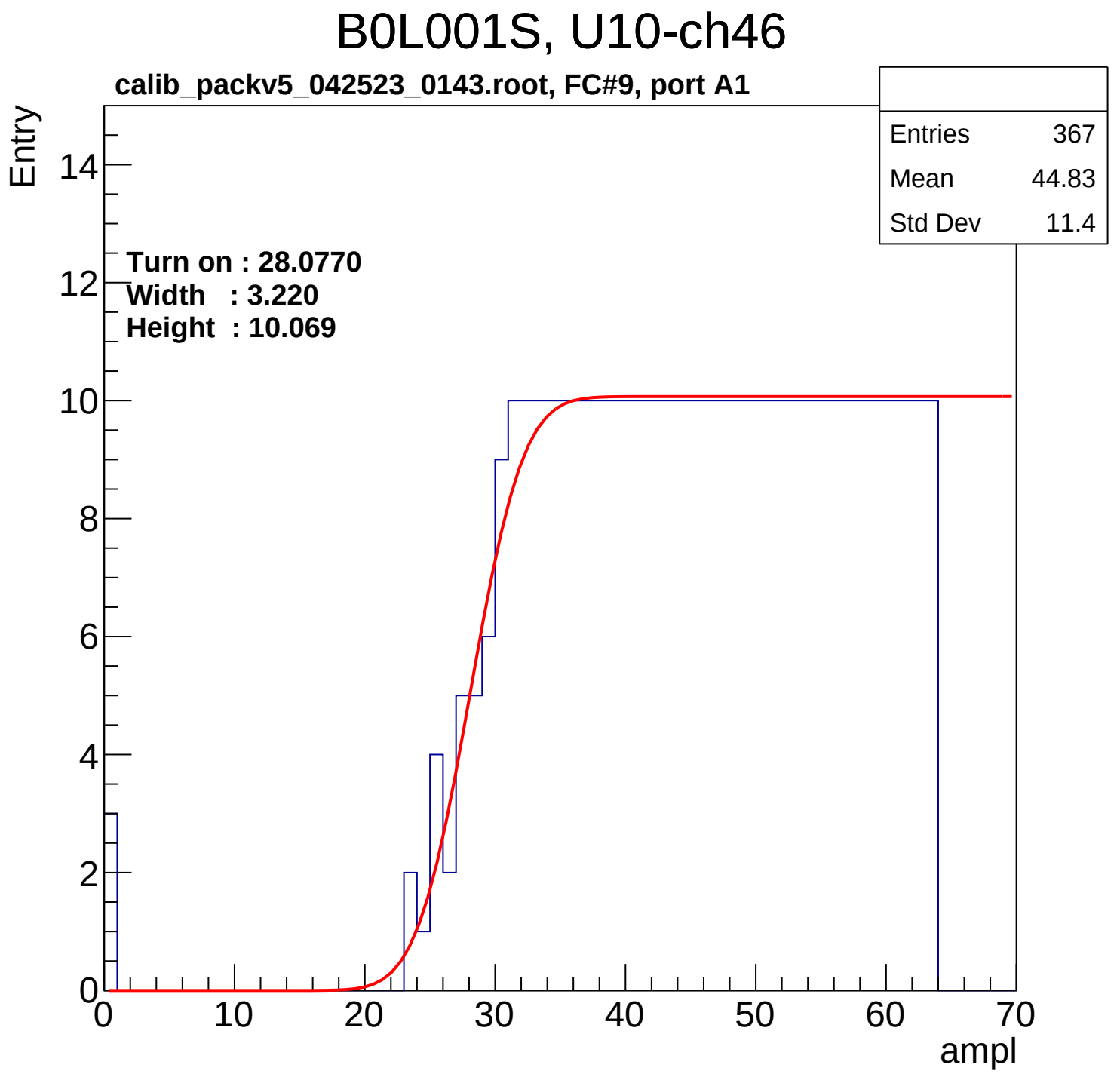

B0L001S, U10-ch41
calib_packv5_042523_0143.root, FC#9, port A1
Entries 371
Mean 44.65
Std Dev 11.45
Turn on : 27.1054
Width : 3.064
Height : 10.027
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

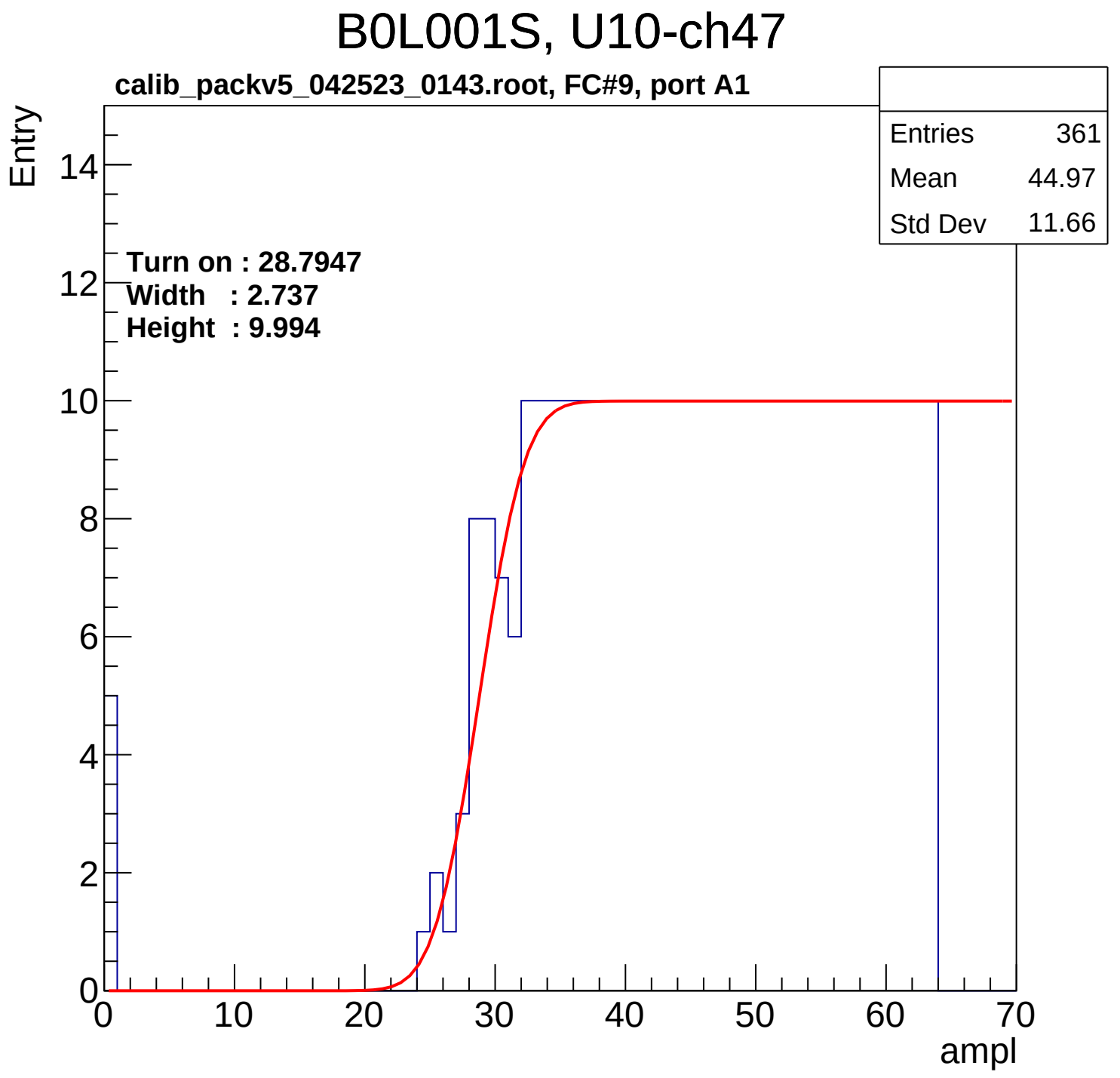

B0L001S, U10-ch42
calib_packv5_042523_0143.root, FC#9, port A1
Entries 340
Mean 46.08
Std Dev 10.99
Turn on : 31.2789
Width : 2.683
Height : 10.102
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

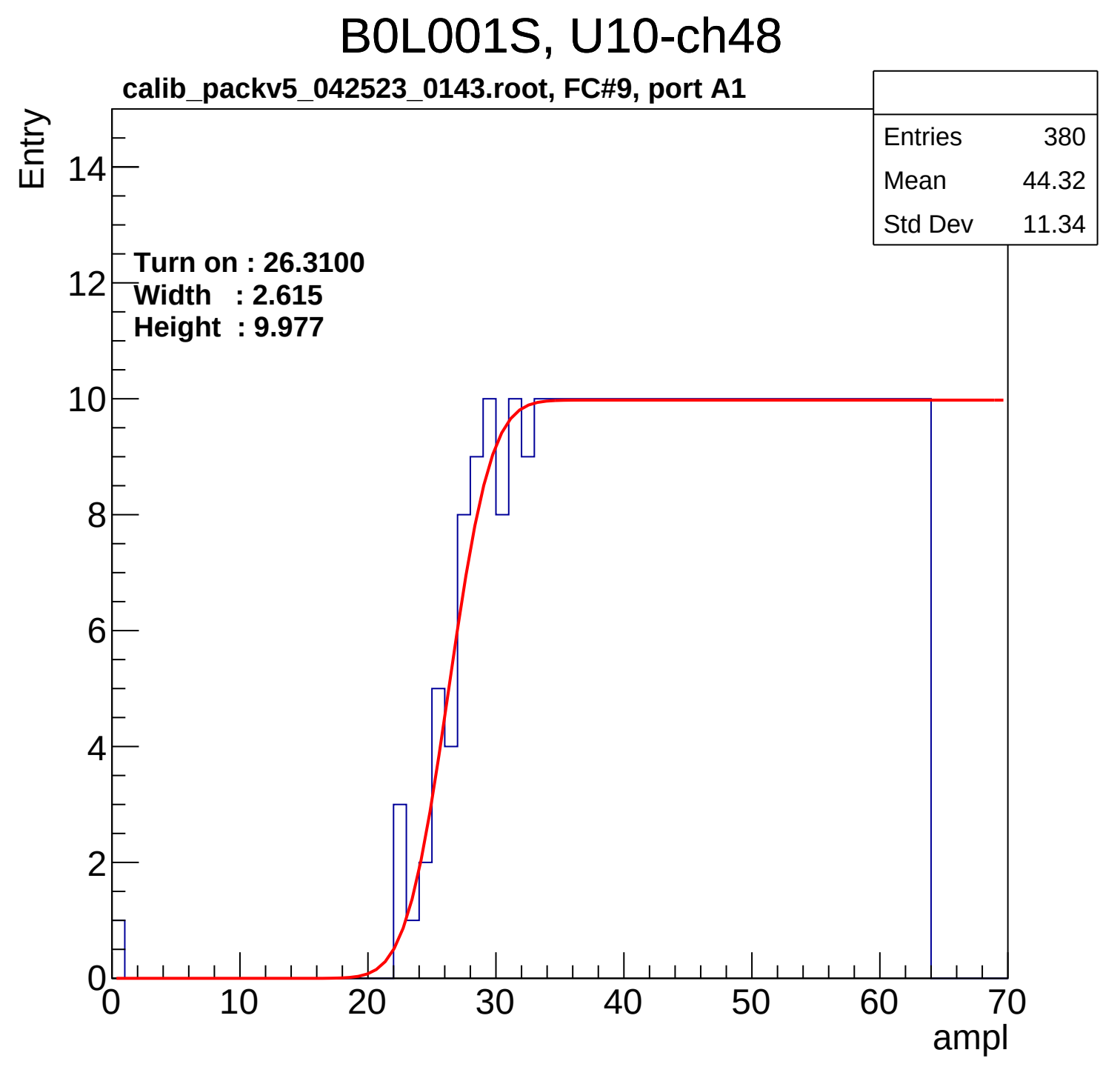

B0L001S, U10-ch43
calib_packv5_042523_0143.root, FC#9, port A1
Entries 374
Mean 44.45
Std Dev 11.6
Turn on : 26.9561
Width : 3.376
Height : 9.998
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

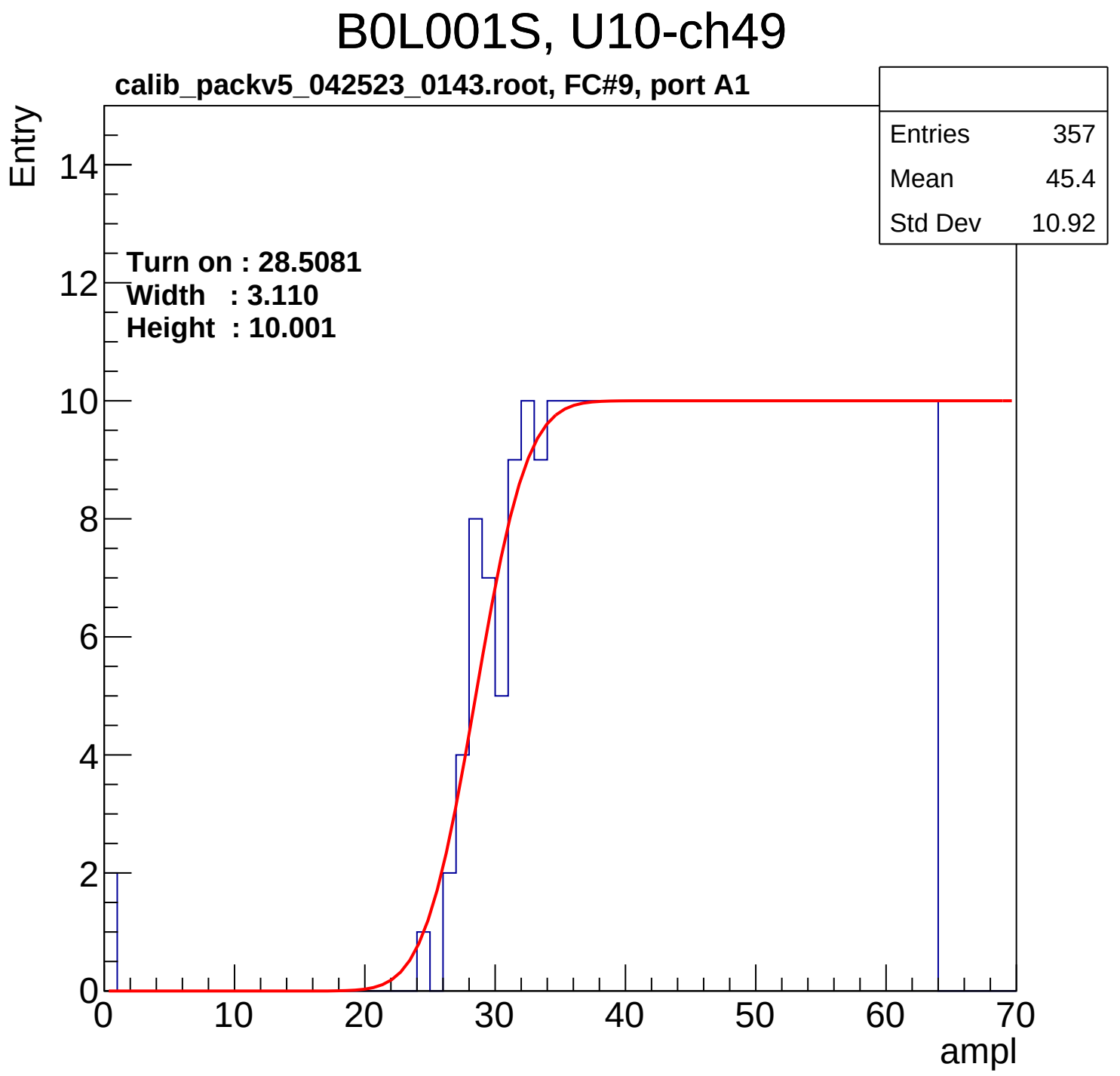

B0L001S, U10-ch44
calib_packv5_042523_0143.root, FC#9, port A1
Entries 354
Mean 45.6
Std Dev 10.67
Turn on : 29.2602
Width : 3.445
Height : 10.088
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

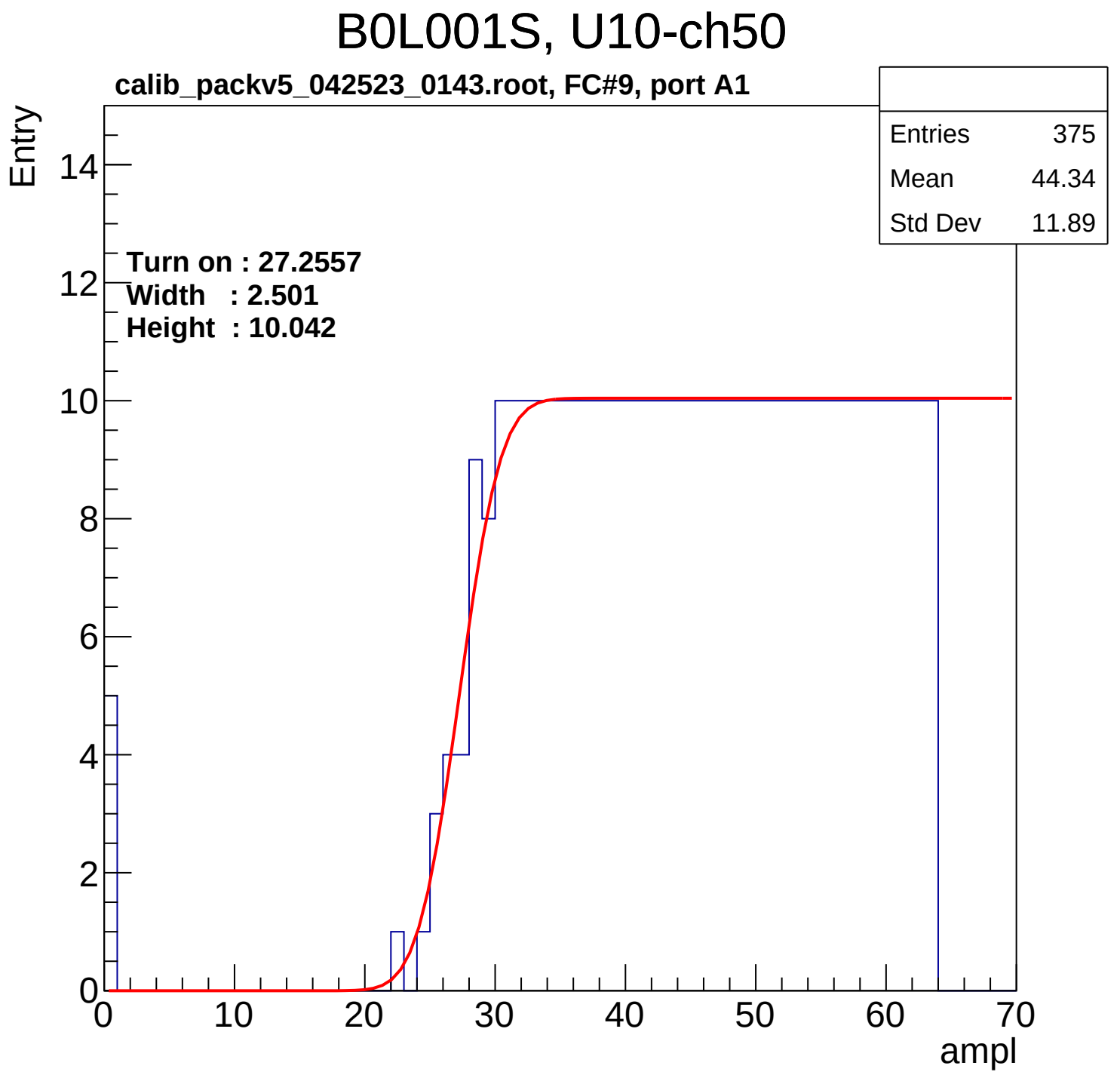

B0L001S, U10-ch45
calib_packv5_042523_0143.root, FC#9, port A1
Entries 354
Mean 45.49
Std Dev 10.95
Turn on : 29.5479
Width : 3.728
Height : 10.089
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

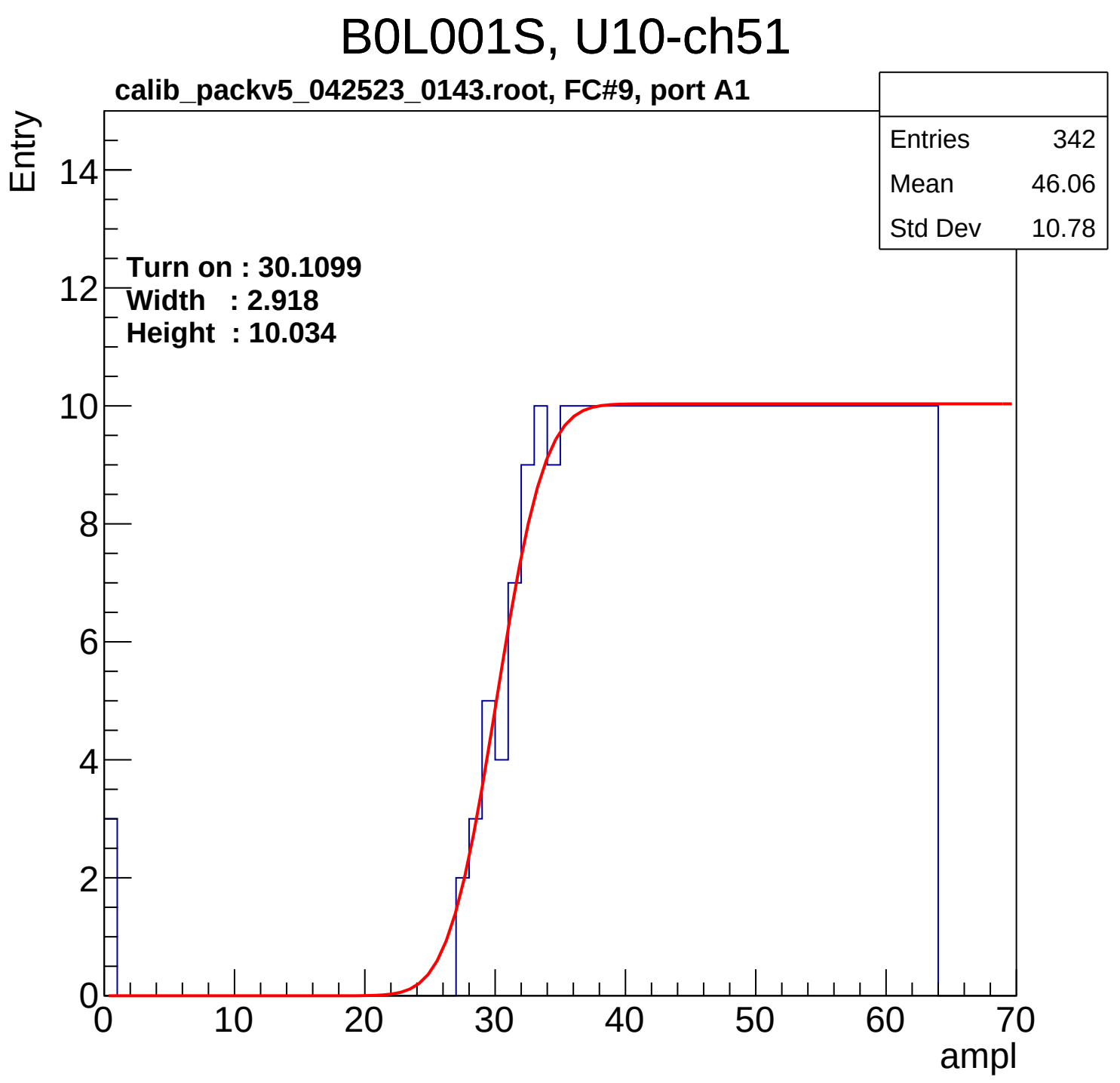

B0L001S, U10-ch46
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.83
Std Dev 11.4
Turn on : 28.0770
Width : 3.220
Height : 10.069
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

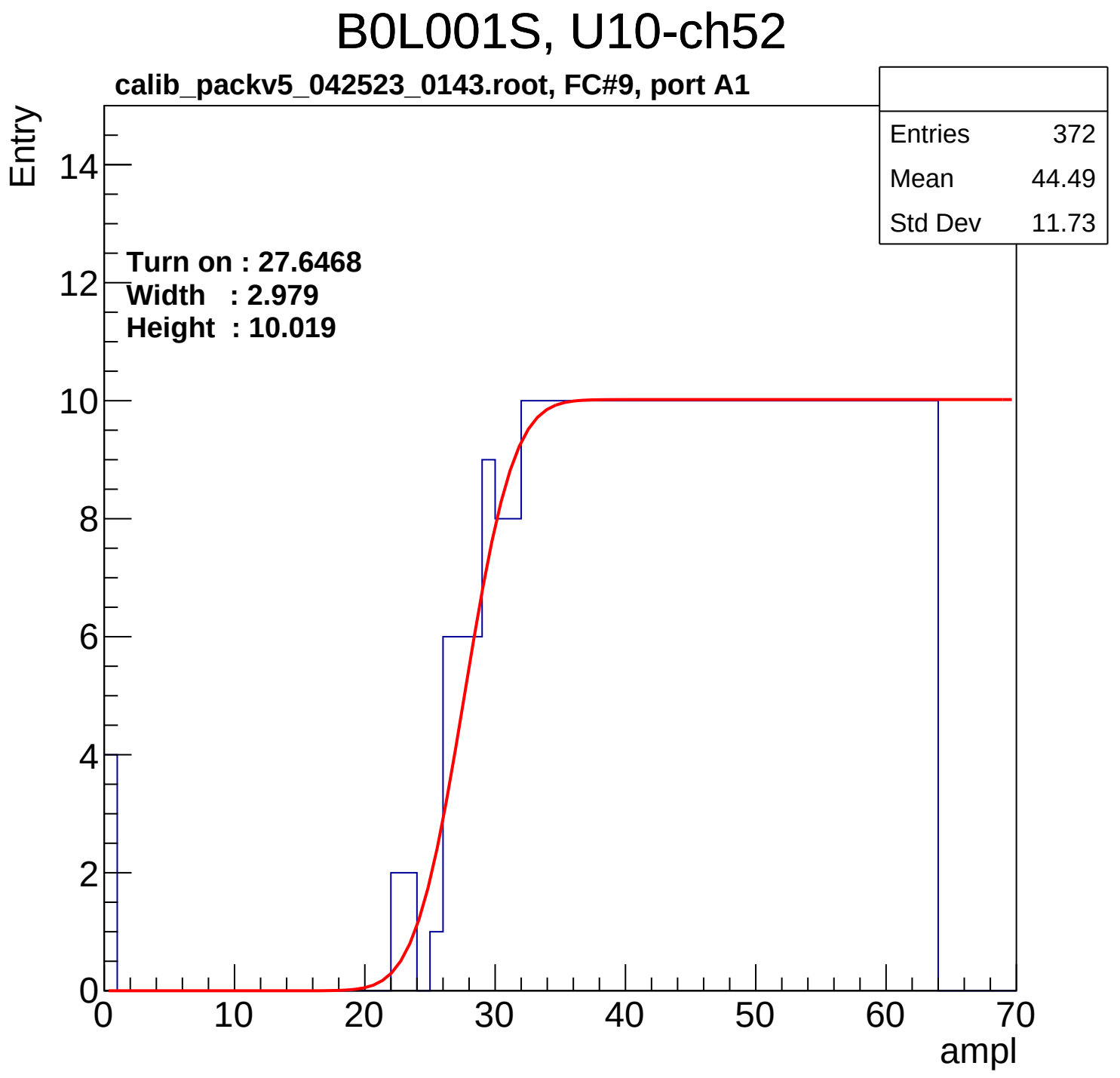

B0L001S, U10-ch47
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 44.97
Std Dev 11.66
Turn on : 28.7947
Width : 2.737
Height : 9.994
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

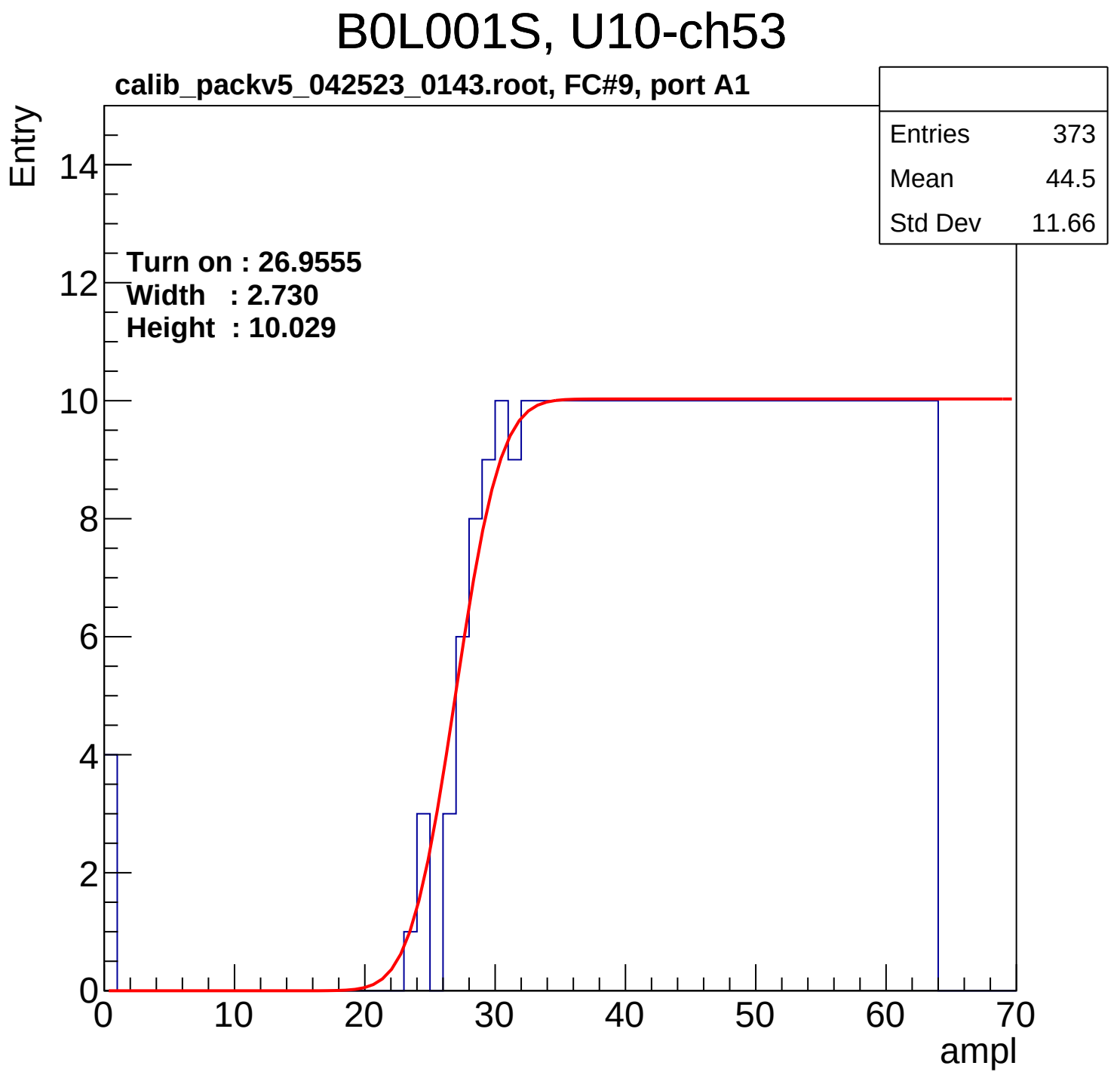

B0L001S, U10-ch48
calib_packv5_042523_0143.root, FC#9, port A1
Entries 380
Mean 44.32
Std Dev 11.34
Turn on : 26.3100
Width : 2.615
Height : 9.977
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

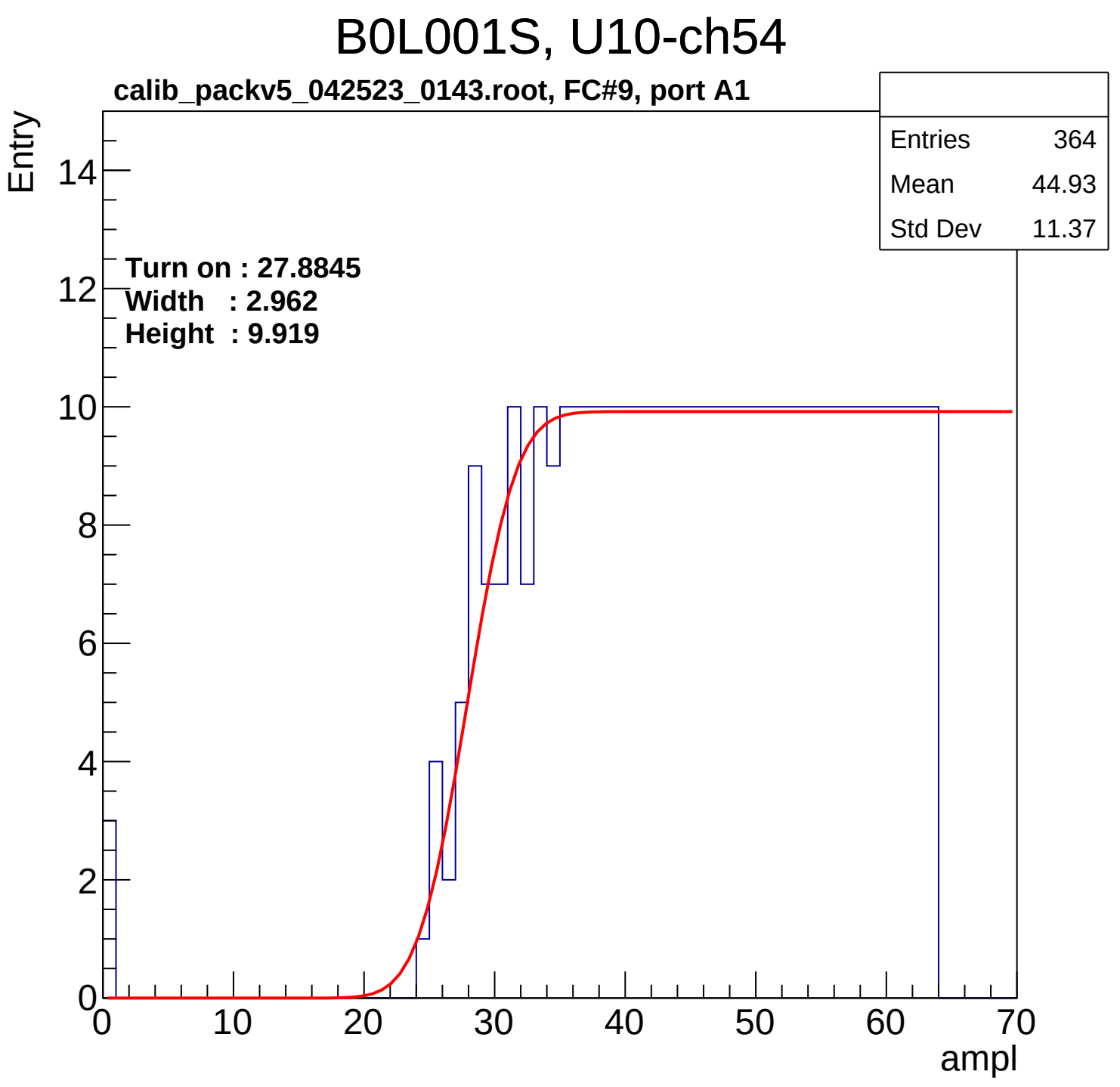

B0L001S, U10-ch49
calib_packv5_042523_0143.root, FC#9, port A1
Entries 357
Mean 45.4
Std Dev 10.92
Turn on : 28.5081
Width : 3.110
Height : 10.001
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

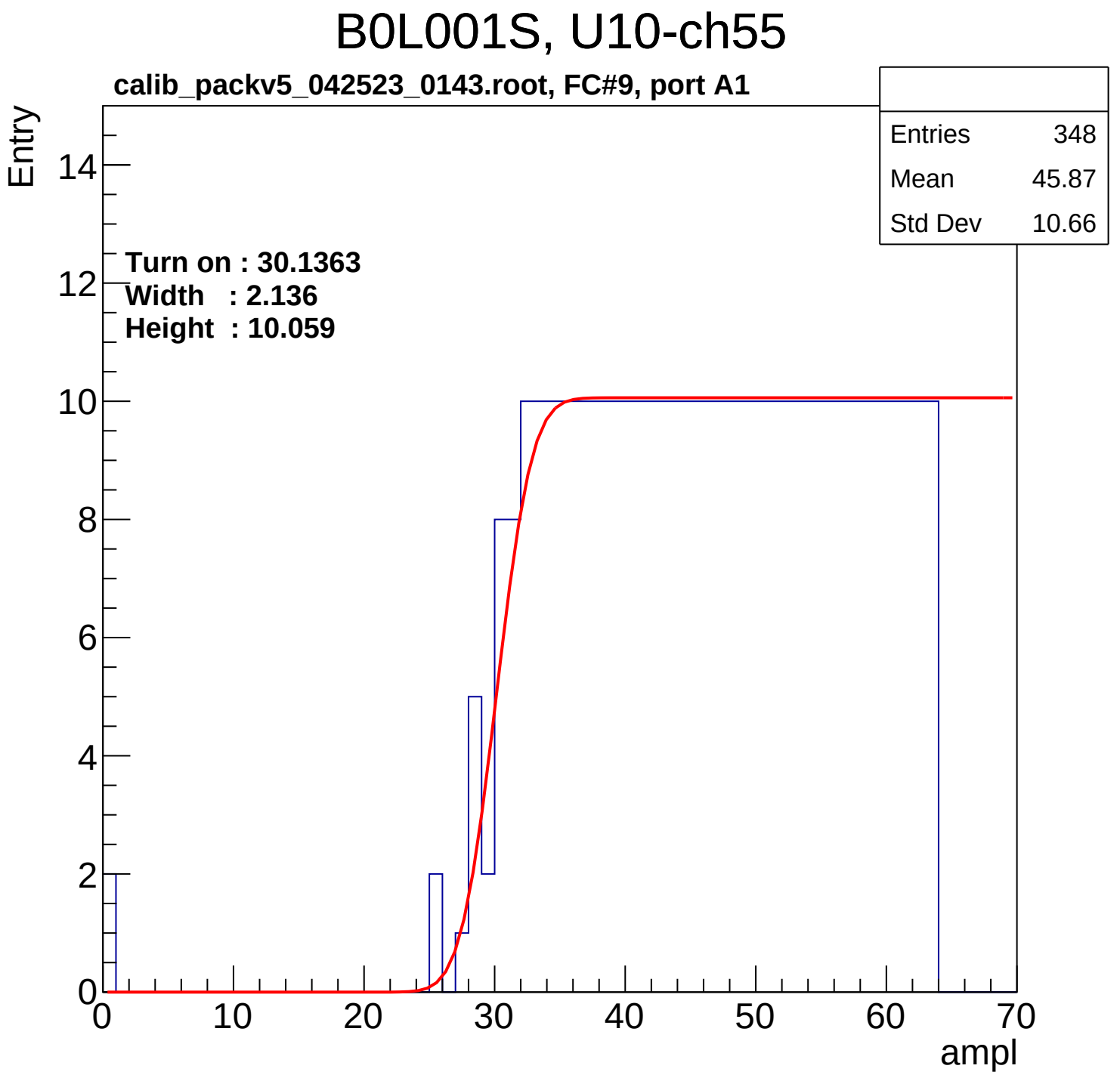

B0L001S, U10-ch50
calib_packv5_042523_0143.root, FC#9, port A1
Entries 375
Mean 44.34
Std Dev 11.89
Turn on : 27.2557
Width : 2.501
Height : 10.042
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

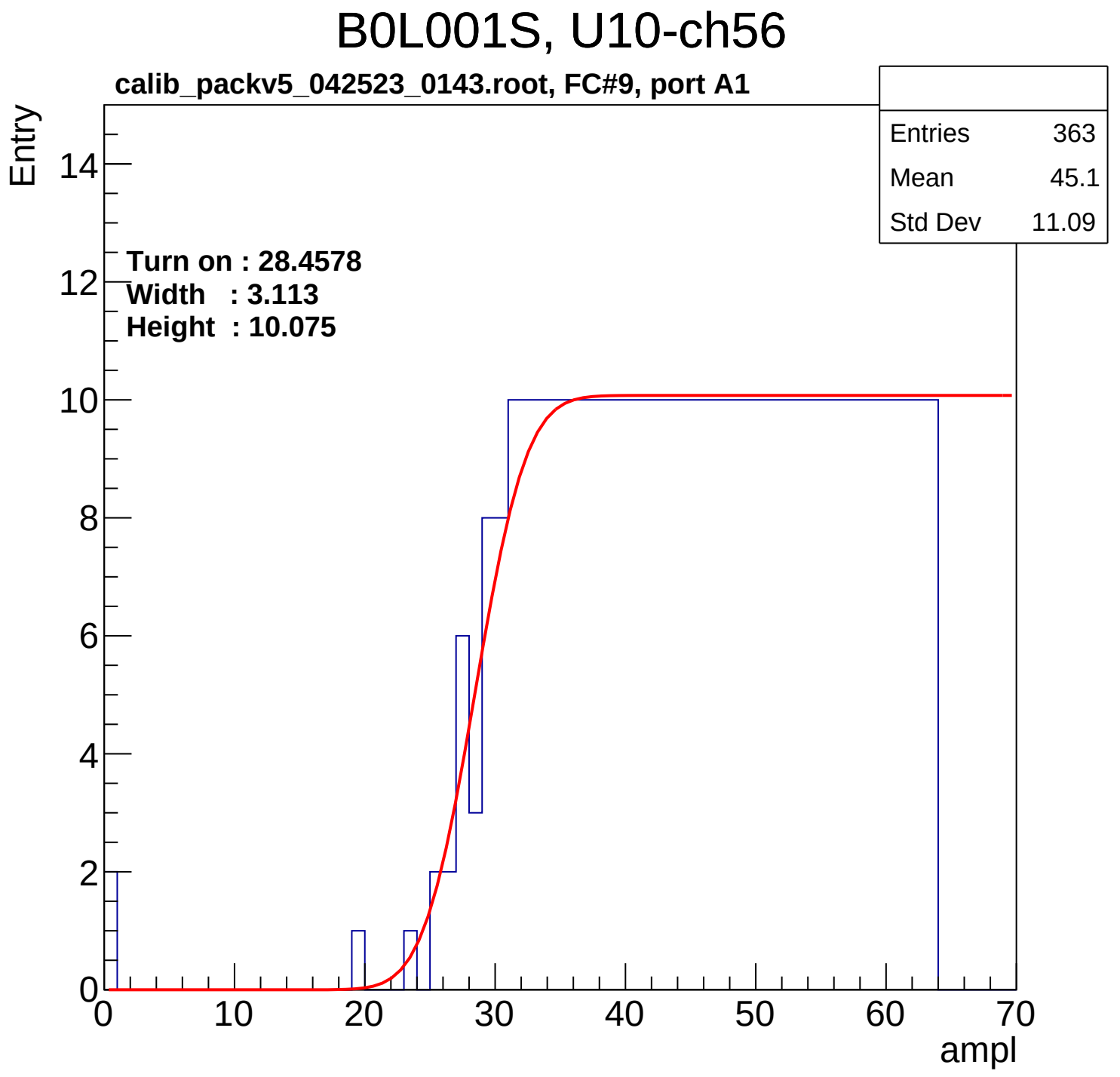

B0L001S, U10-ch51
calib_packv5_042523_0143.root, FC#9, port A1
Entries 342
Mean 46.06
Std Dev 10.78
Turn on : 30.1099
Width : 2.918
Height : 10.034
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

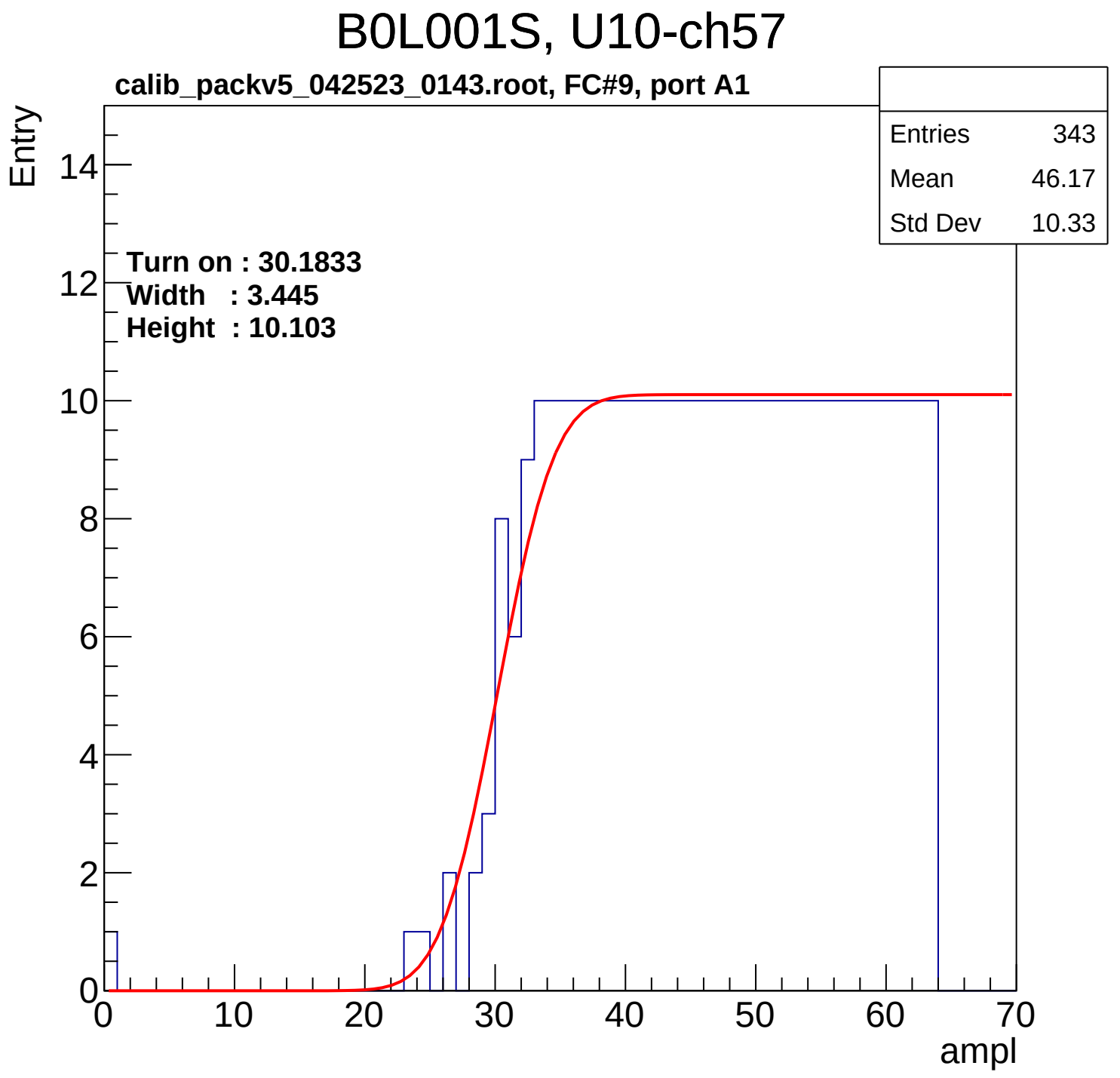

B0L001S, U10-ch52
calib_packv5_042523_0143.root, FC#9, port A1
Entries 372
Mean 44.49
Std Dev 11.73
Turn on : 27.6468
Width : 2.979
Height : 10.019
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

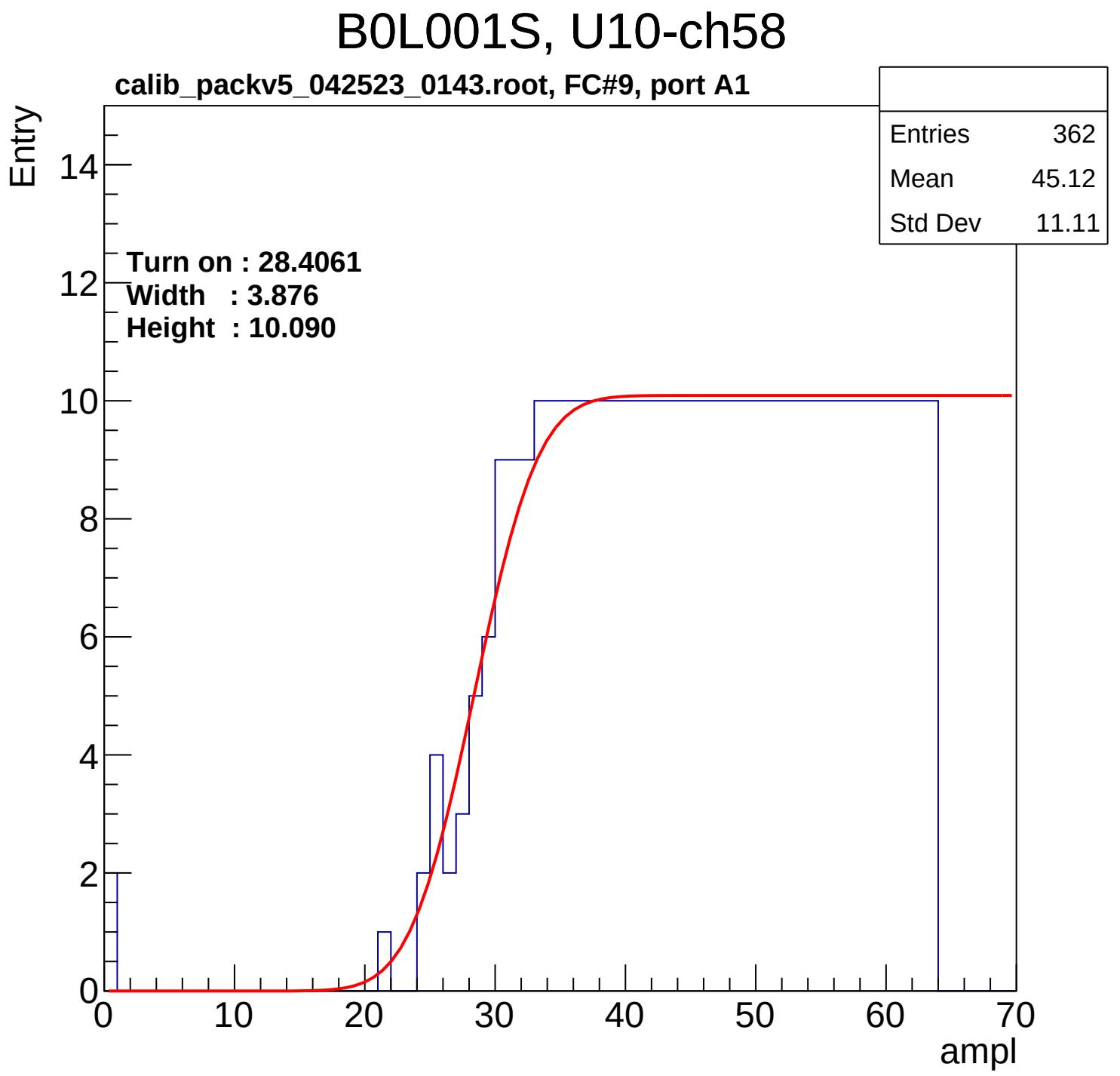

B0L001S, U10-ch53
calib_packv5_042523_0143.root, FC#9, port A1
Entries 373
Mean 44.5
Std Dev 11.66
Turn on : 26.9555
Width : 2.730
Height : 10.029
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

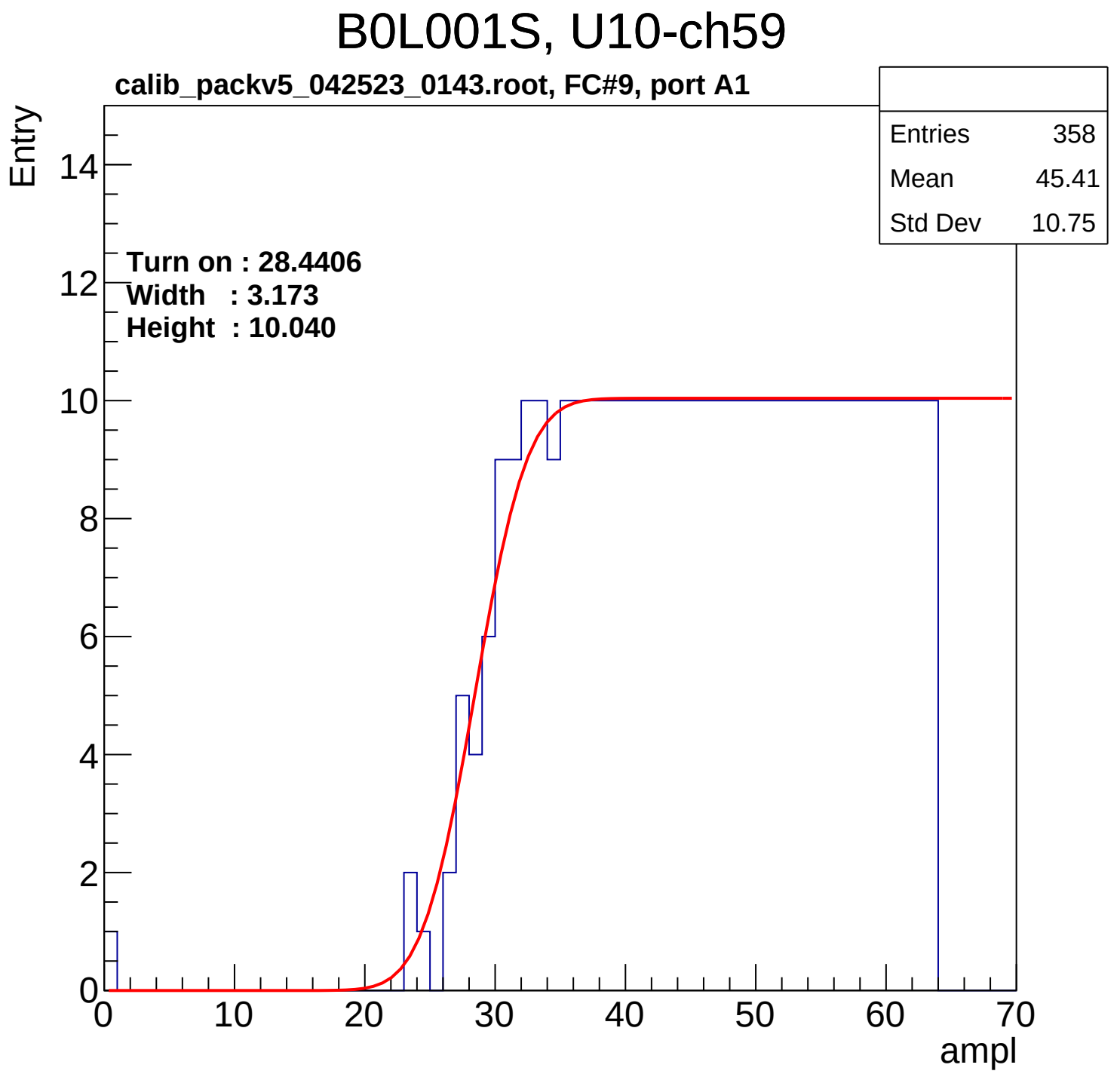

B0L001S, U10-ch54
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 44.93
Std Dev 11.37
Turn on : 27.8845
Width : 2.962
Height : 9.919
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

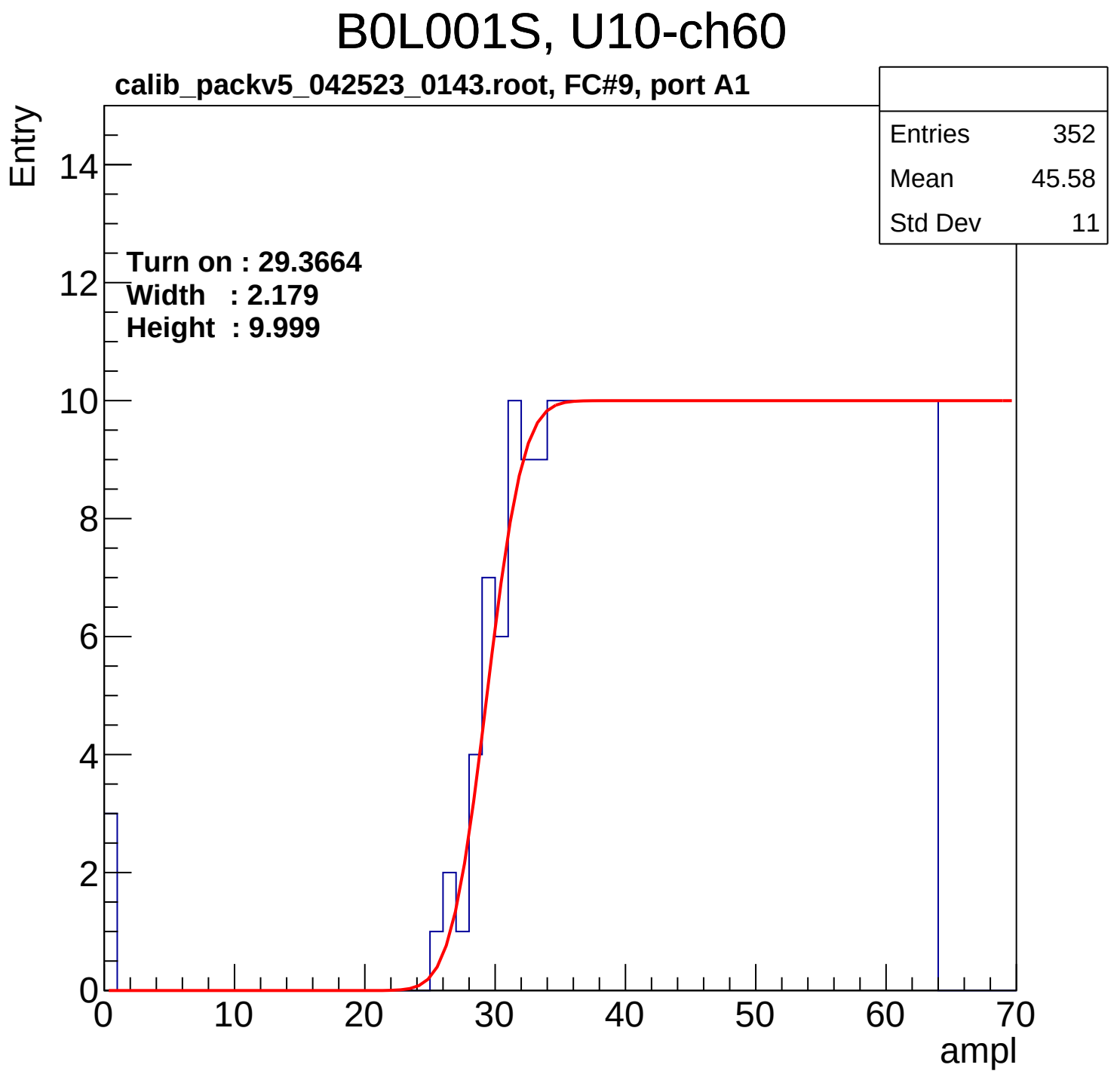

B0L001S, U10-ch55
calib_packv5_042523_0143.root, FC#9, port A1
Entries 348
Mean 45.87
Std Dev 10.66
Turn on : 30.1363
Width : 2.136
Height : 10.059
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

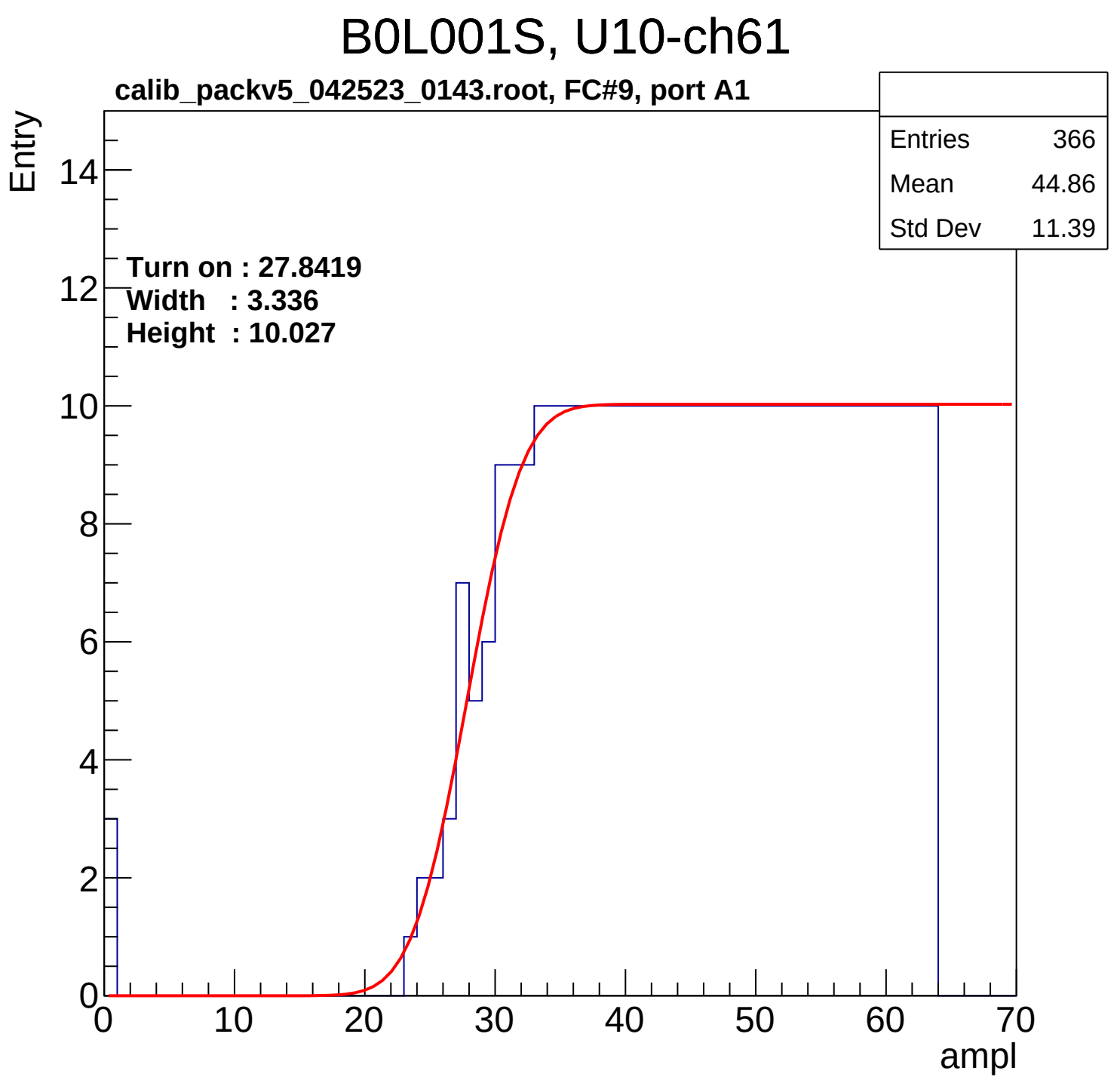

B0L001S, U10-ch56
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 45.1
Std Dev 11.09
Turn on : 28.4578
Width : 3.113
Height : 10.075
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

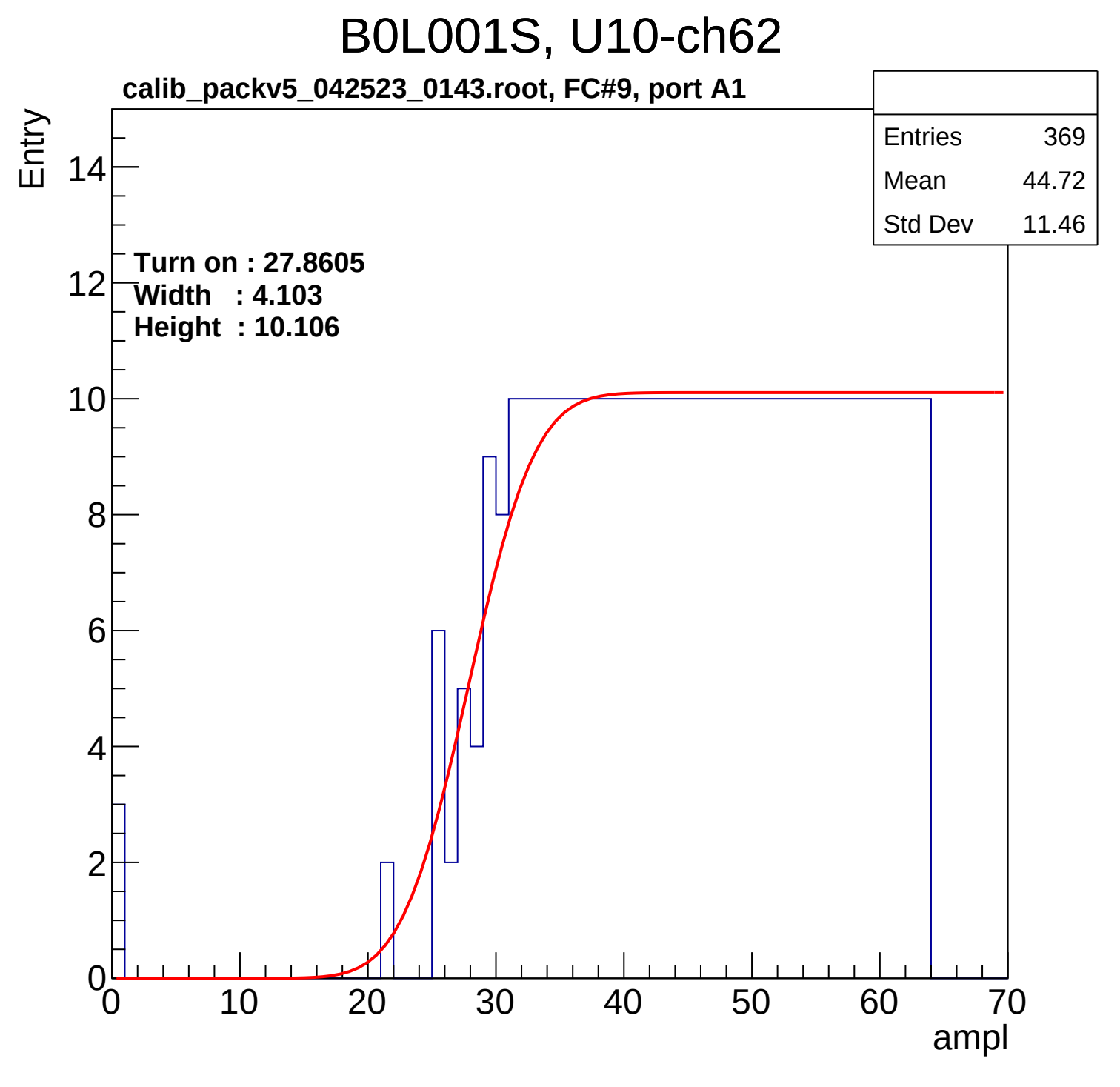

B0L001S, U10-ch57
calib_packv5_042523_0143.root, FC#9, port A1
Entries 343
Mean 46.17
Std Dev 10.33
Turn on : 30.1833
Width : 3.445
Height : 10.103
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

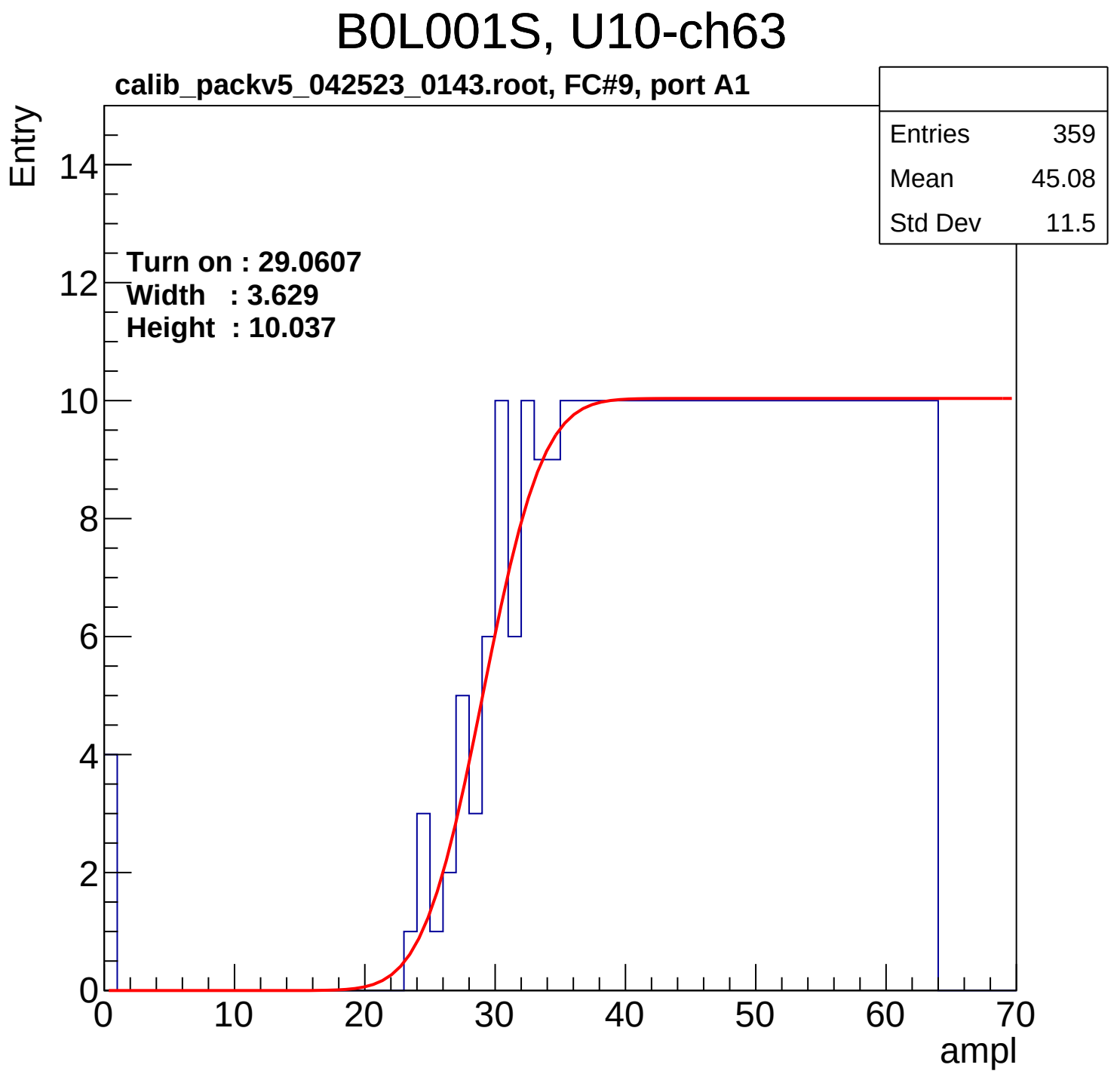

B0L001S, U10-ch58
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 45.12
Std Dev 11.11
Turn on : 28.4061
Width : 3.876
Height : 10.090
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

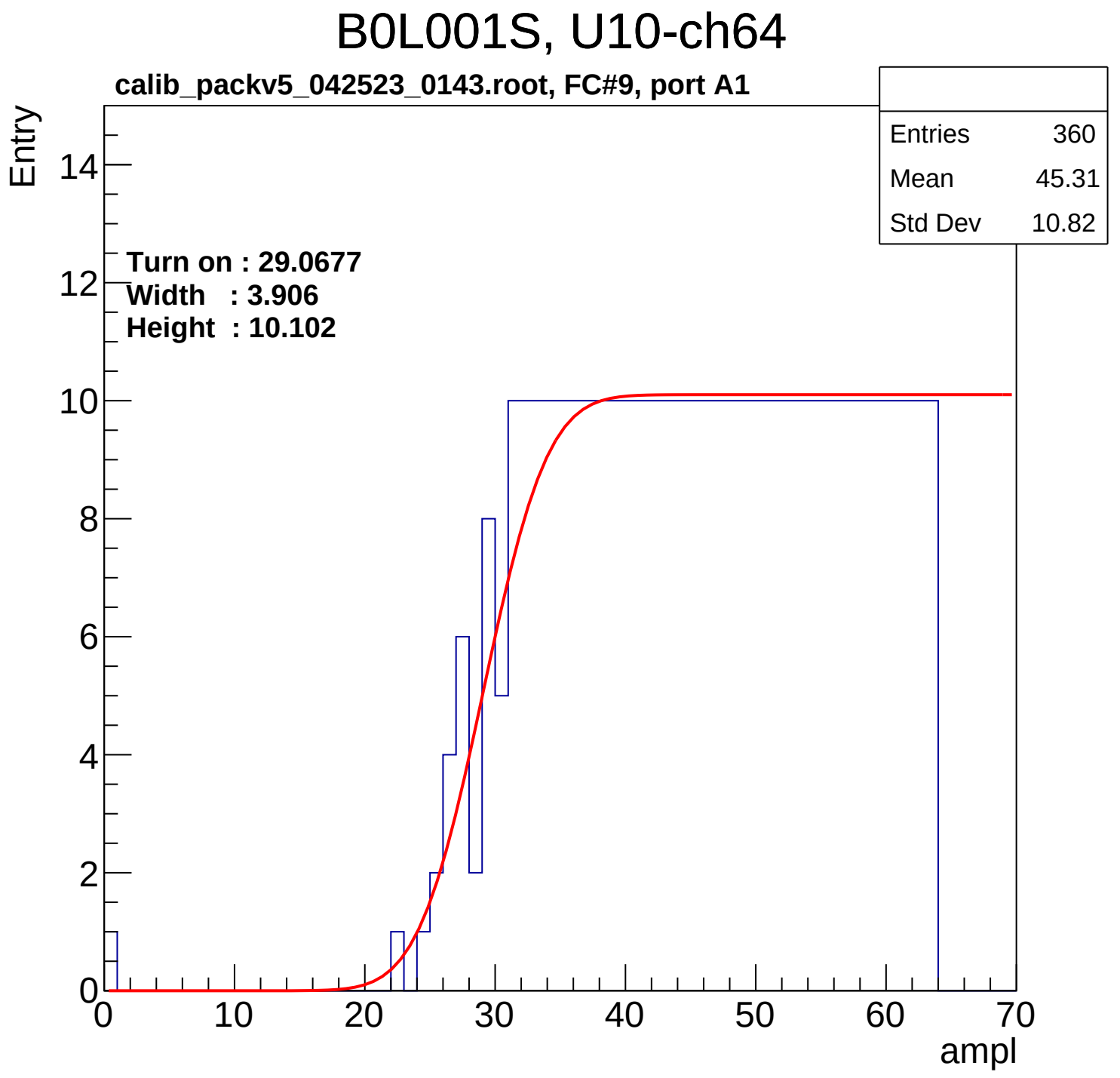

B0L001S, U10-ch59
calib_packv5_042523_0143.root, FC#9, port A1
Entries 358
Mean 45.41
Std Dev 10.75
Turn on : 28.4406
Width : 3.173
Height : 10.040
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

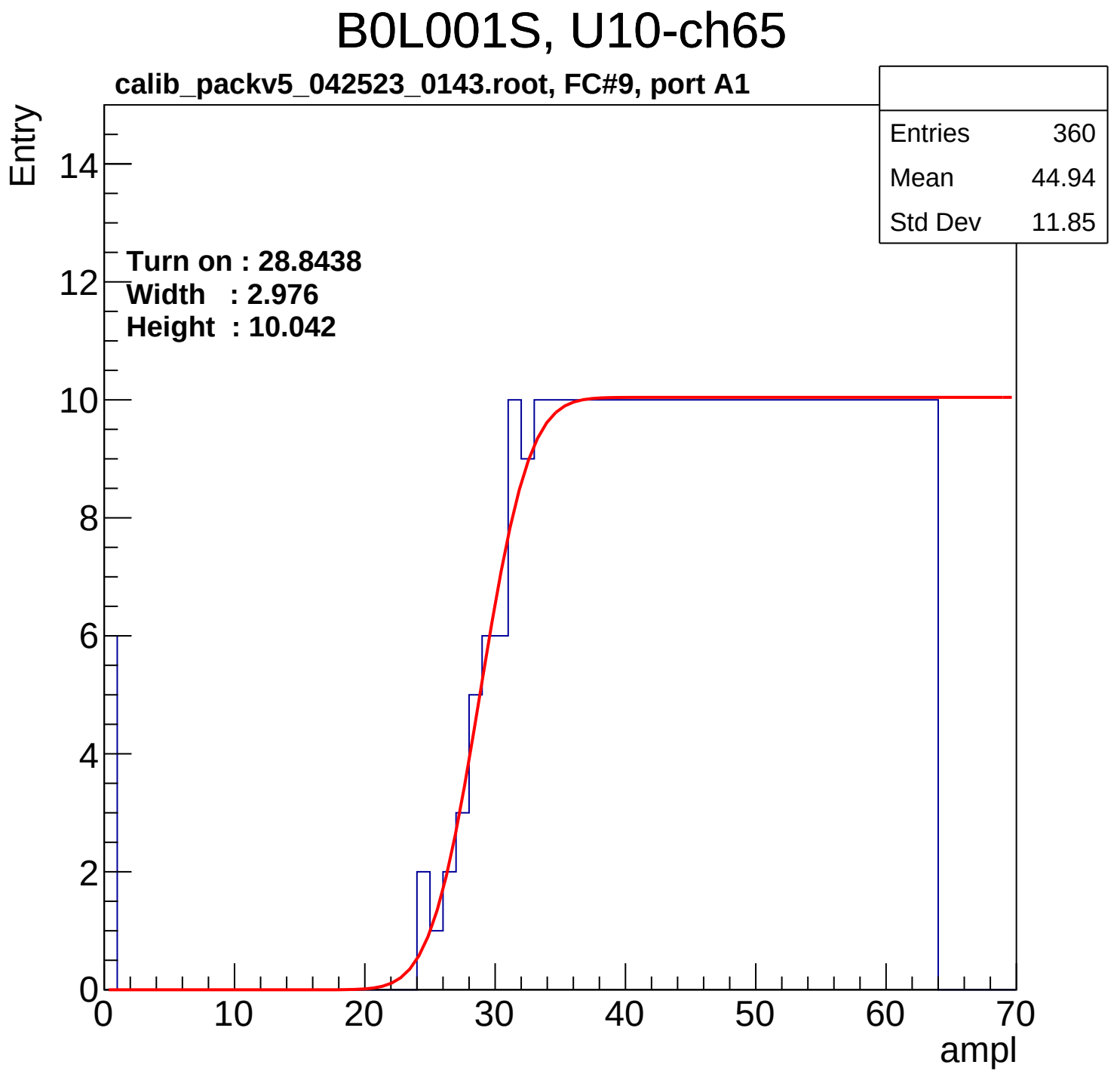

B0L001S, U10-ch60
calib_packv5_042523_0143.root, FC#9, port A1
Entries 352
Mean 45.58
Std Dev 11
Turn on : 29.3664
Width : 2.179
Height : 9.999
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

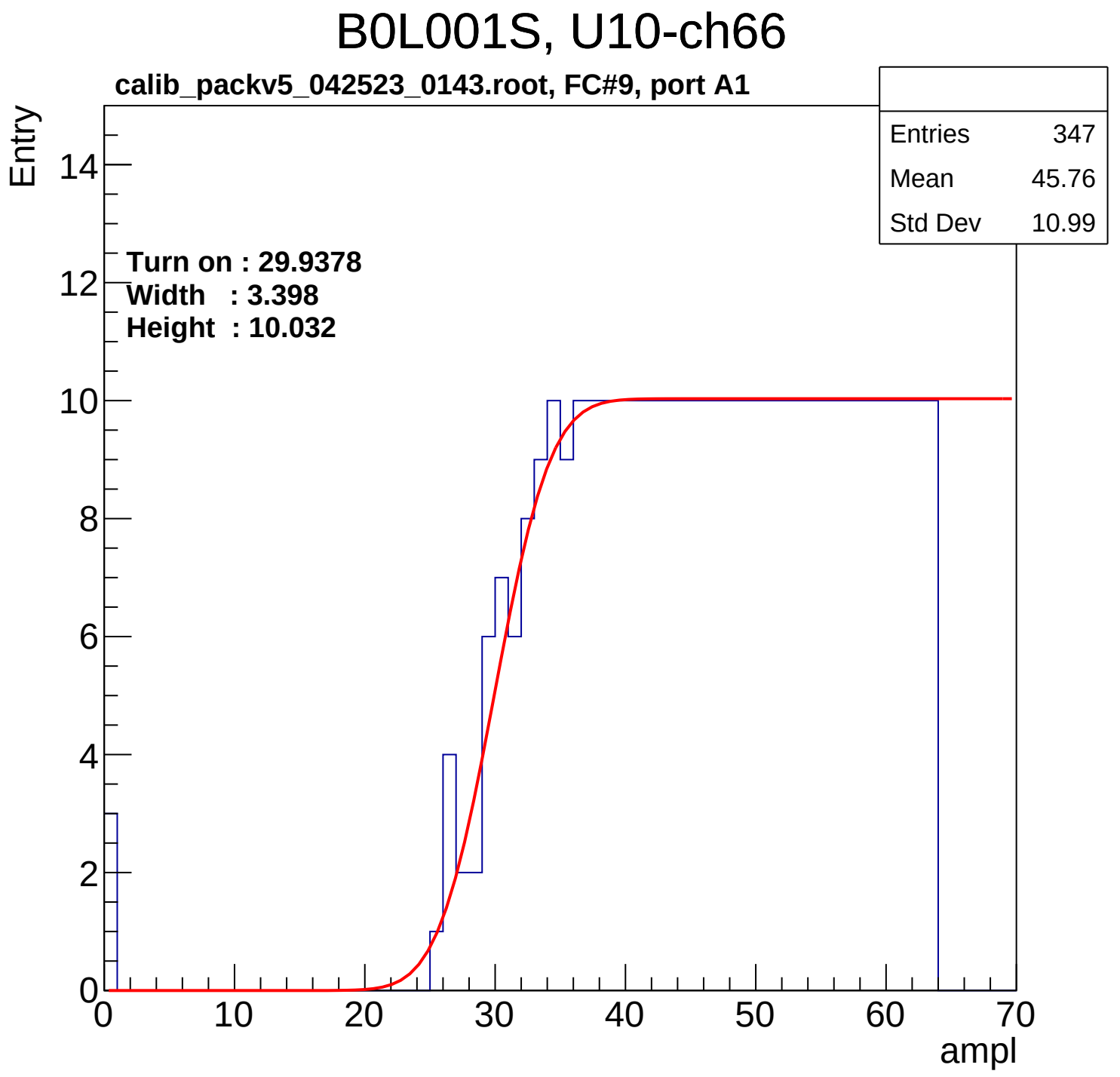

B0L001S, U10-ch61
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.86
Std Dev 11.39
Turn on : 27.8419
Width : 3.336
Height : 10.027
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

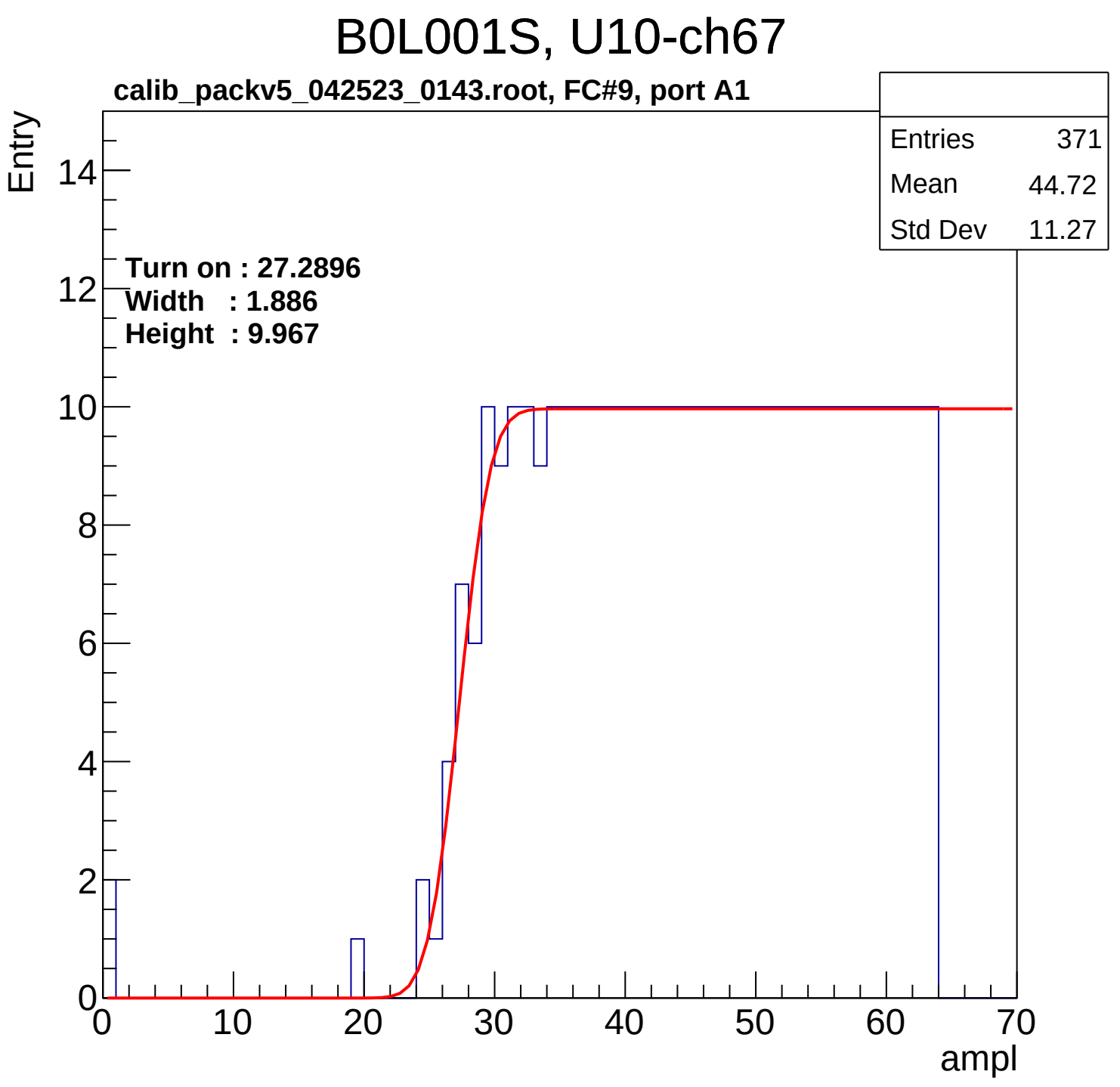

B0L001S, U10-ch62
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.72
Std Dev 11.46
Turn on : 27.8605
Width : 4.103
Height : 10.106
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

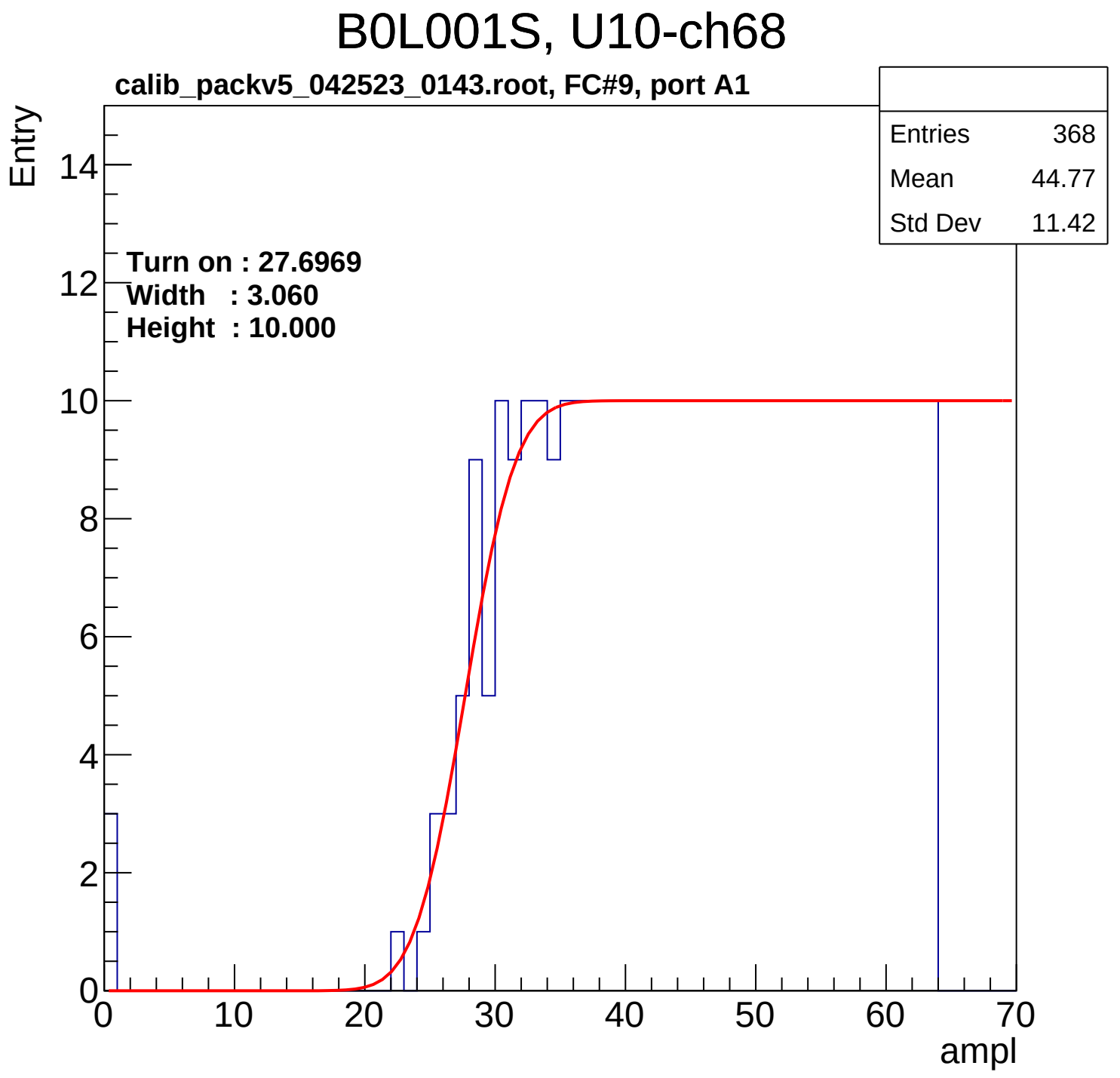

B0L001S, U10-ch63
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 45.08
Std Dev 11.5
Turn on : 29.0607
Width : 3.629
Height : 10.037
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

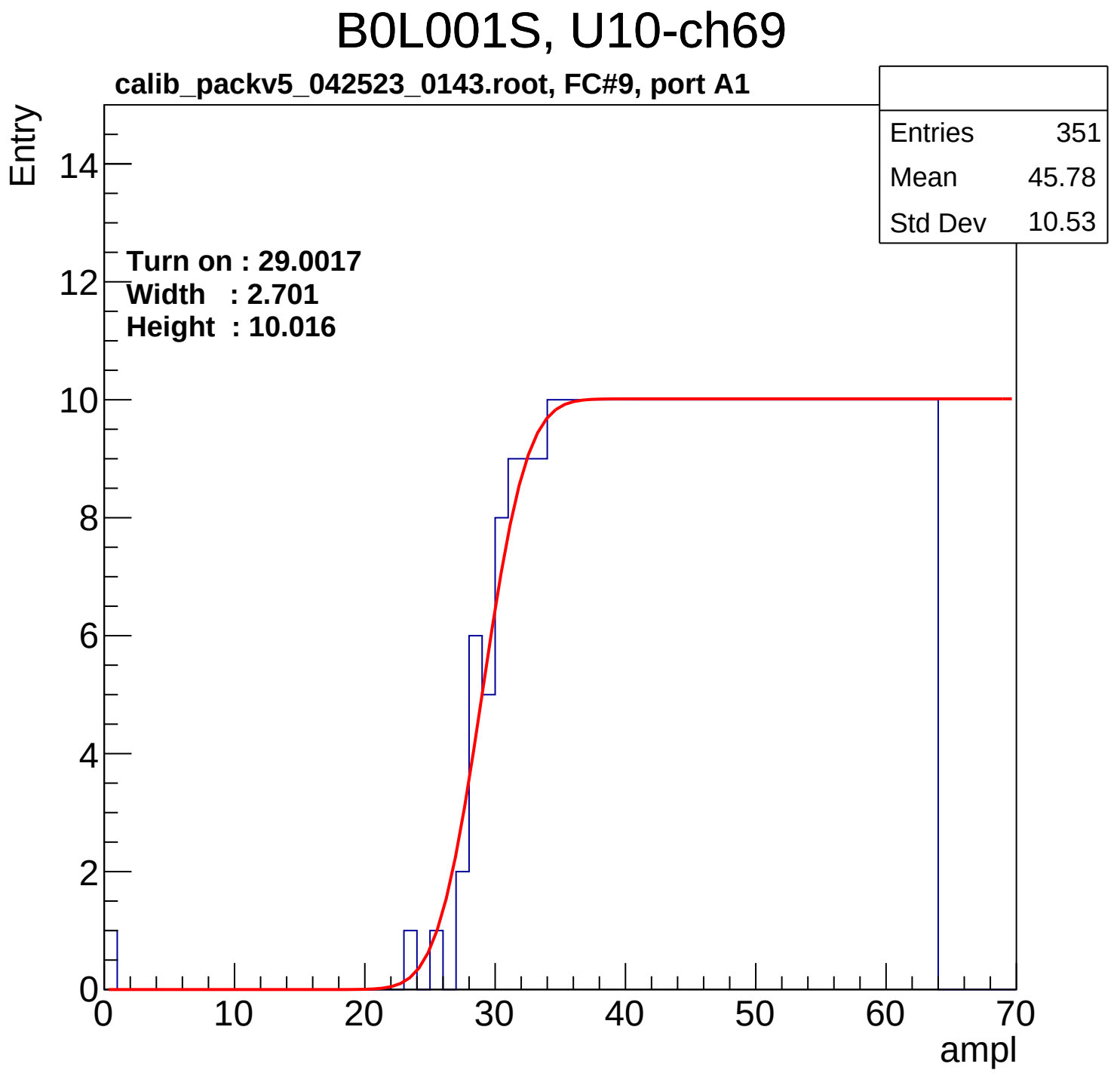

B0L001S, U10-ch64
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 45.31
Std Dev 10.82
Turn on : 29.0677
Width : 3.906
Height : 10.102
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

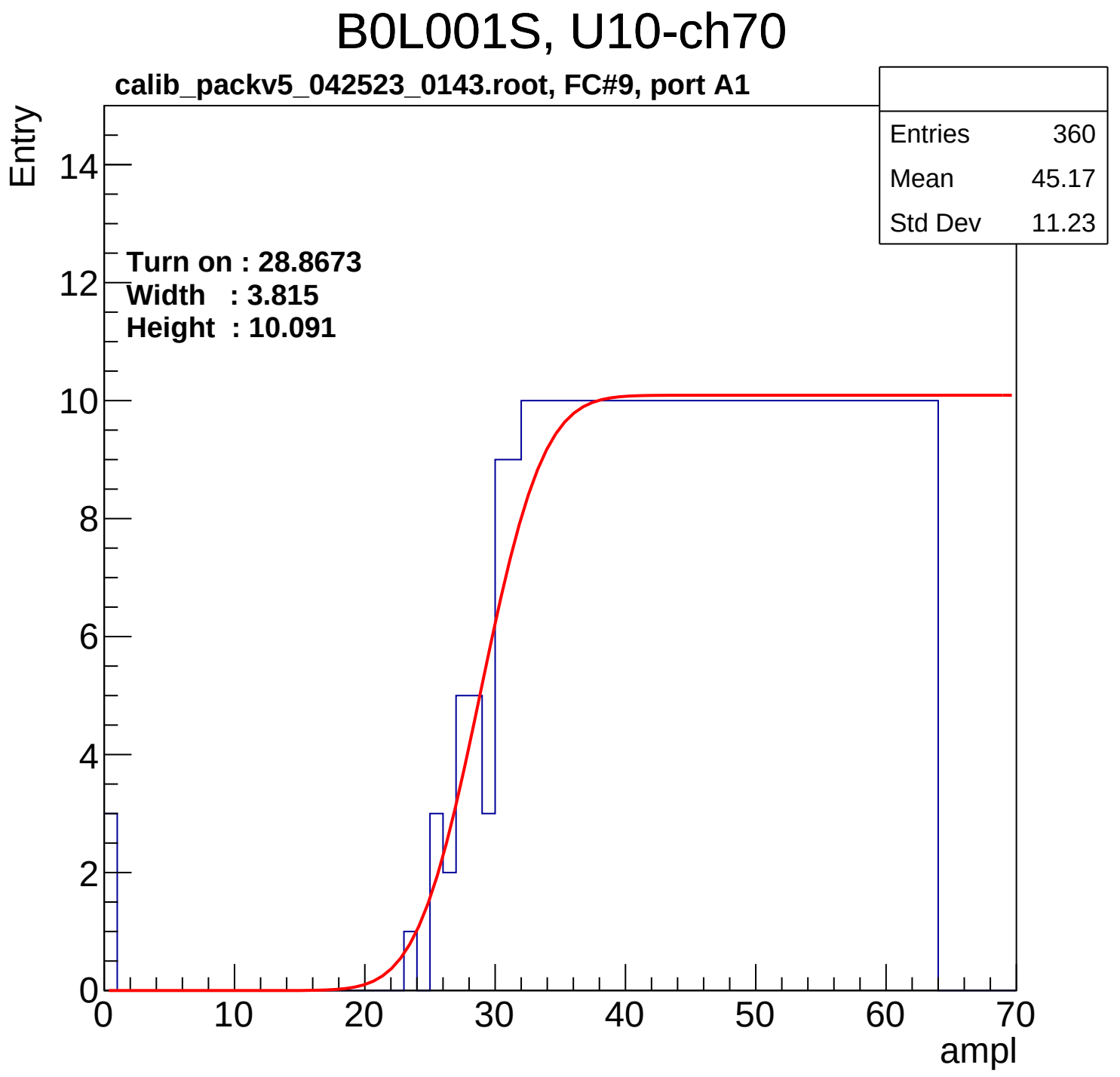

B0L001S, U10-ch65
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 44.94
Std Dev 11.85
Turn on : 28.8438
Width : 2.976
Height : 10.042
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

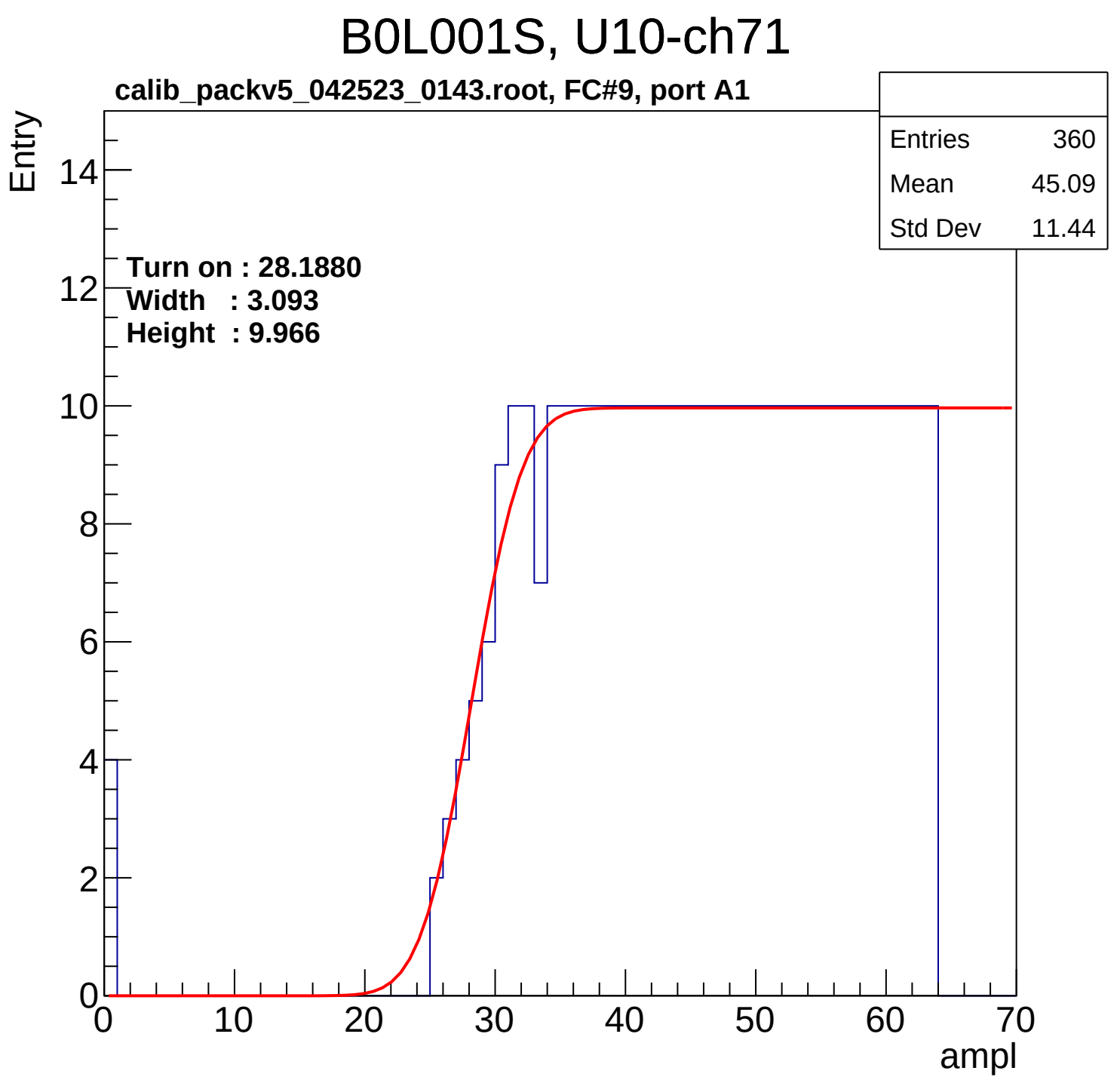

B0L001S, U10-ch66
calib_packv5_042523_0143.root, FC#9, port A1
Entries 347
Mean 45.76
Std Dev 10.99
Turn on : 29.9378
Width : 3.398
Height : 10.032
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

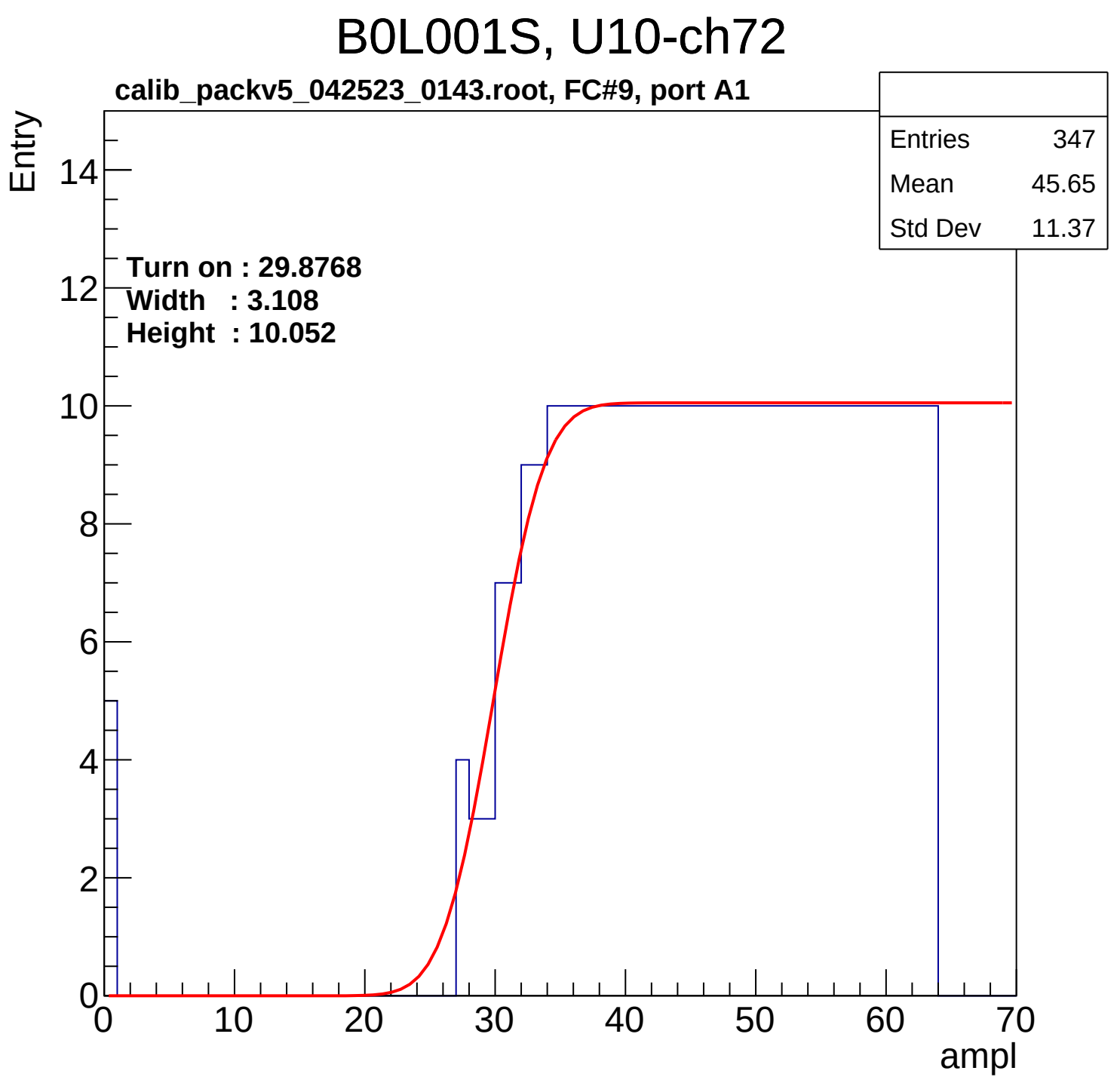

B0L001S, U10-ch67
calib_packv5_042523_0143.root, FC#9, port A1
Entries 371
Mean 44.72
Std Dev 11.27
Turn on : 27.2896
Width : 1.886
Height : 9.967
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

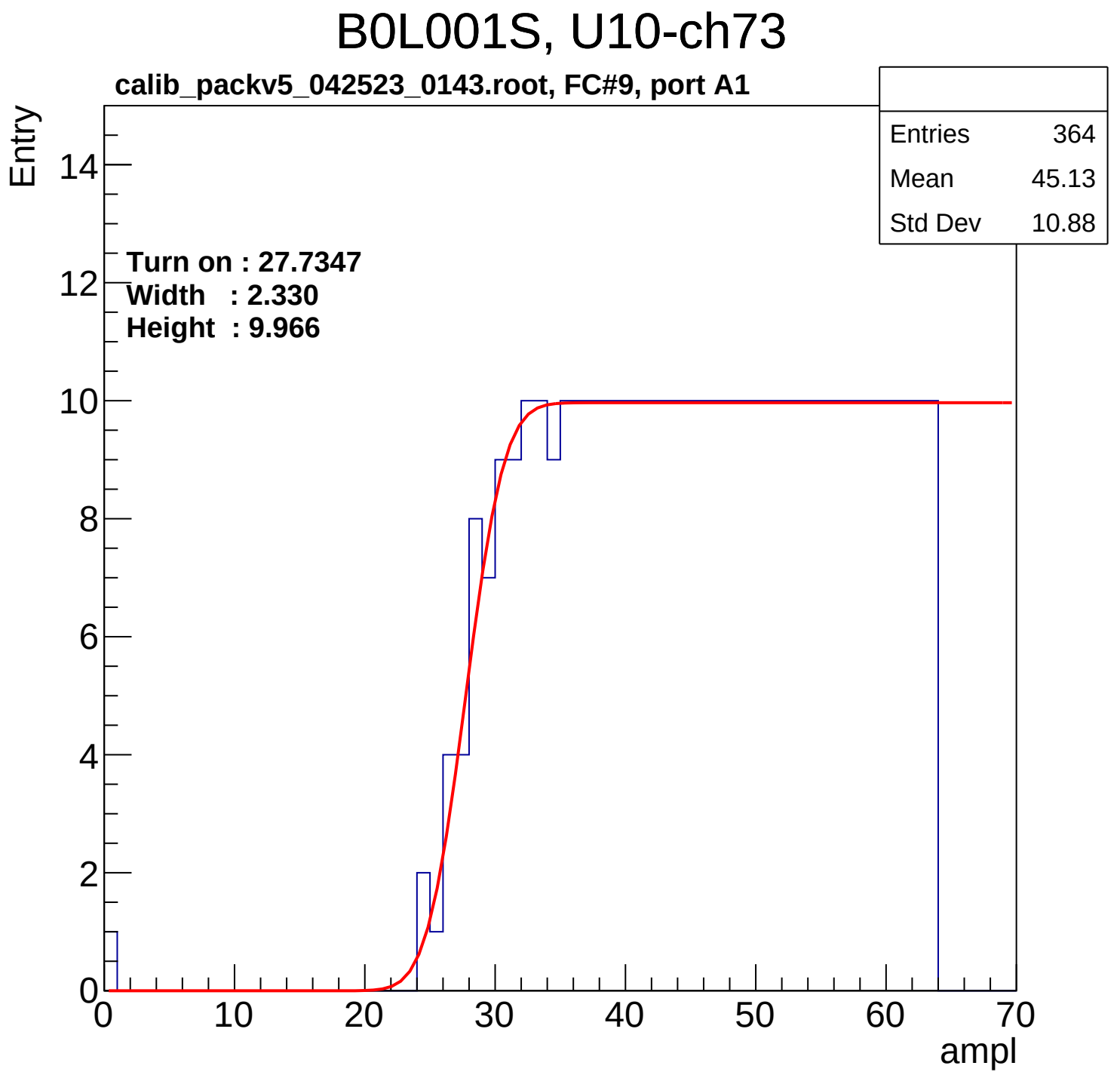

B0L001S, U10-ch68
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.77
Std Dev 11.42
Turn on : 27.6969
Width : 3.060
Height : 10.000
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

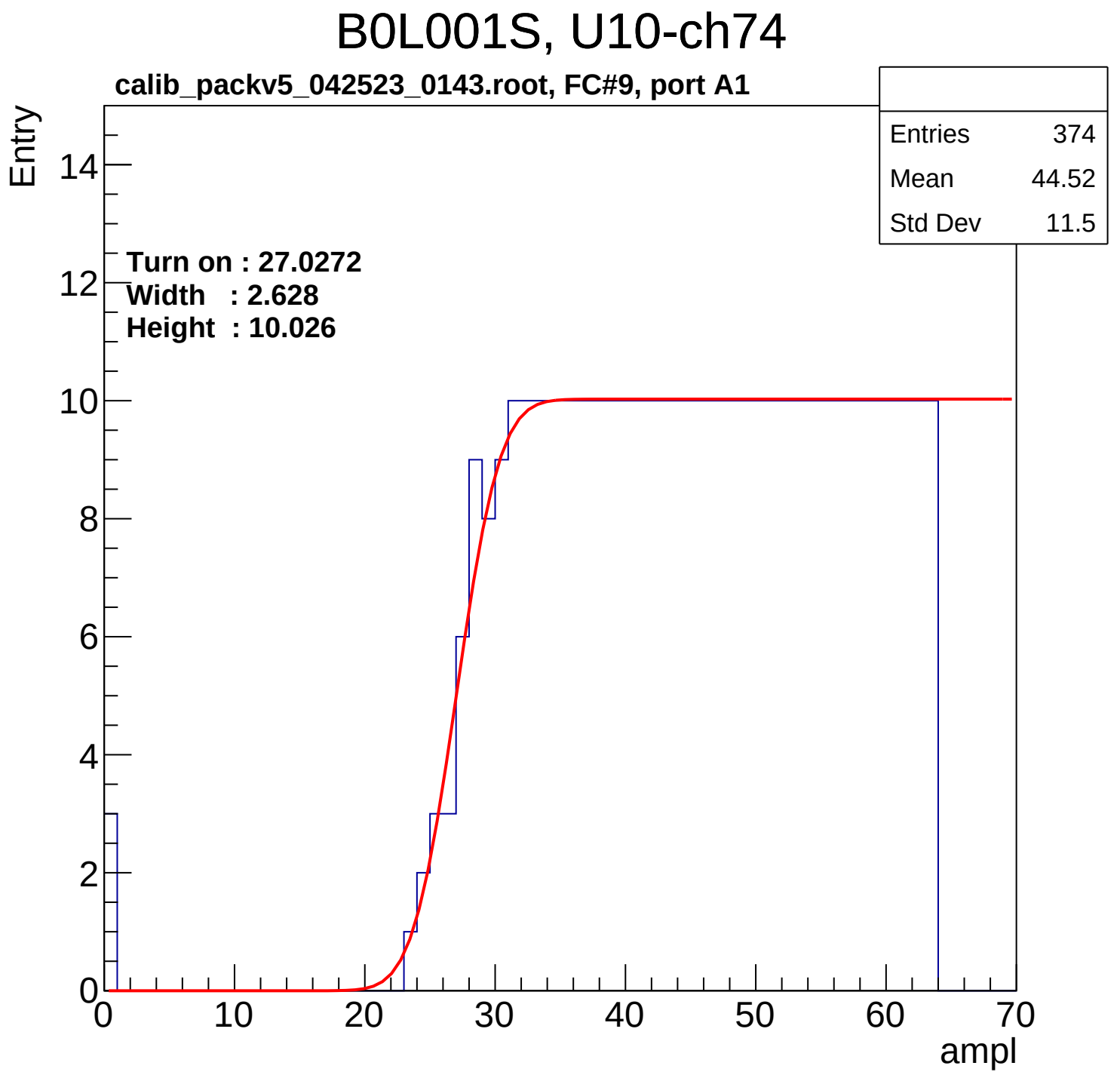

B0L001S, U10-ch69
calib_packv5_042523_0143.root, FC#9, port A1
Entries 351
Mean 45.78
Std Dev 10.53
Turn on : 29.0017
Width : 2.701
Height : 10.016
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

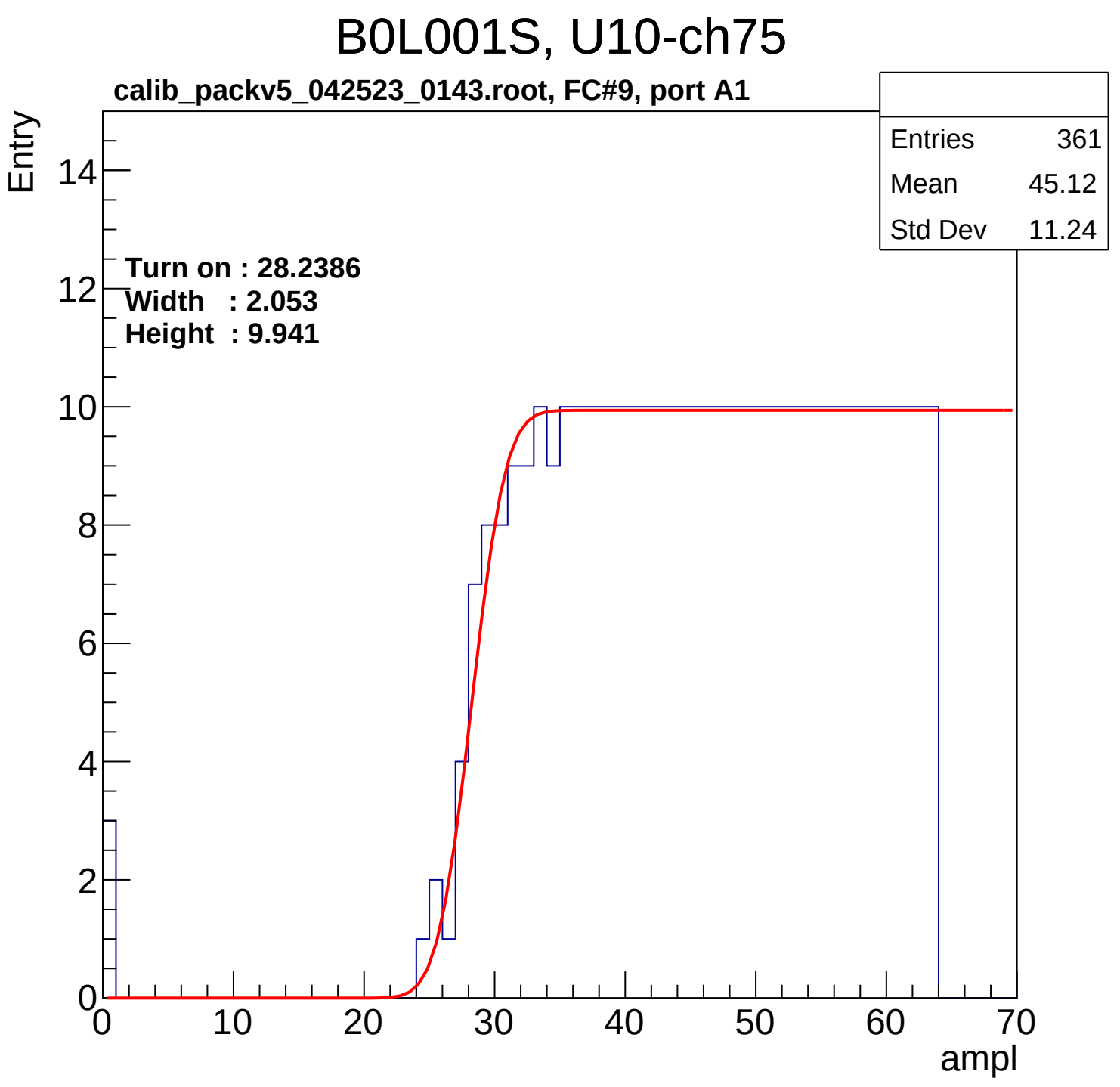

B0L001S, U10-ch70
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 45.17
Std Dev 11.23
Turn on : 28.8673
Width : 3.815
Height : 10.091
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

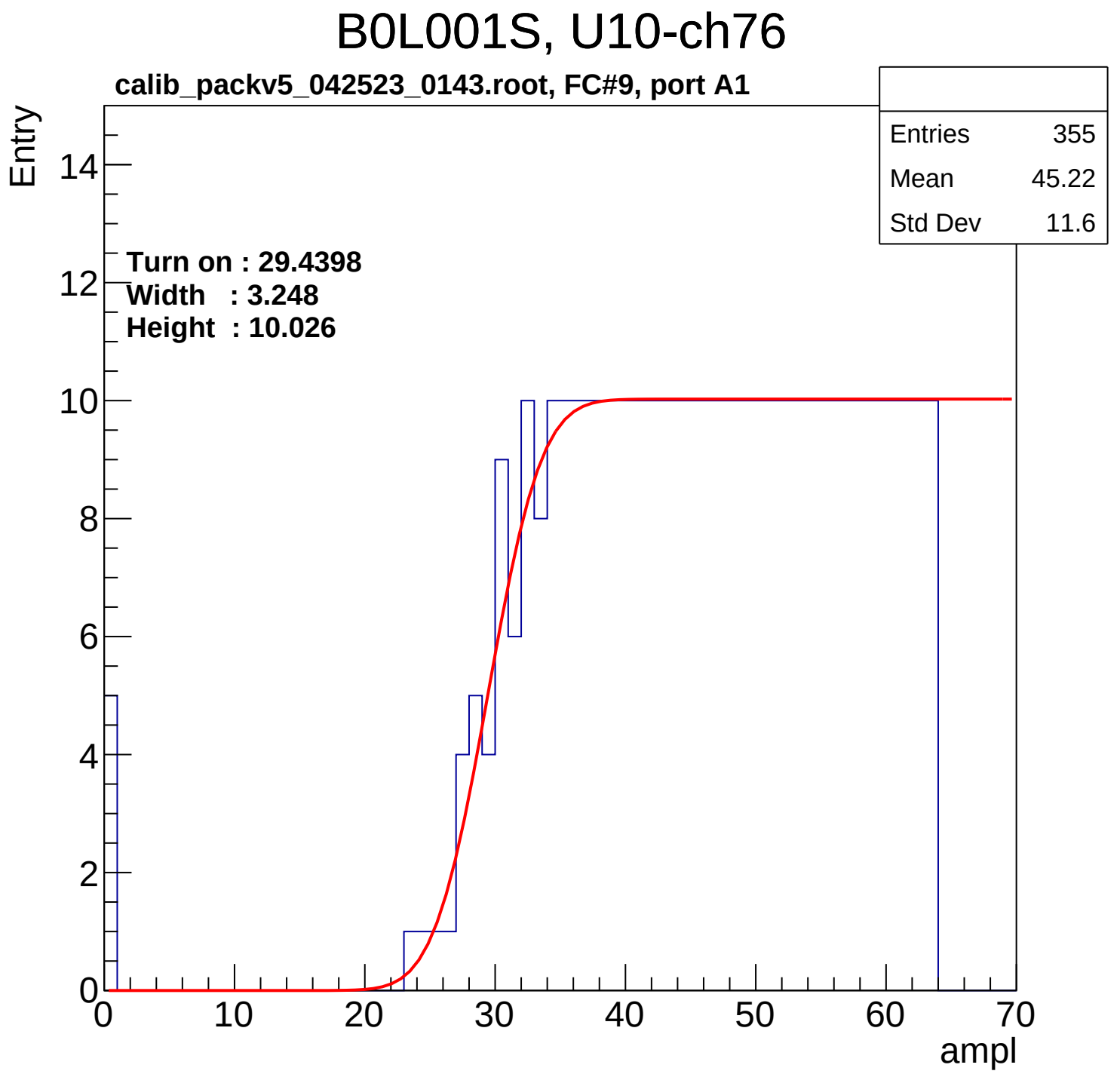

B0L001S, U10-ch71
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 45.09
Std Dev 11.44
Turn on : 28.1880
Width : 3.093
Height : 9.966
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

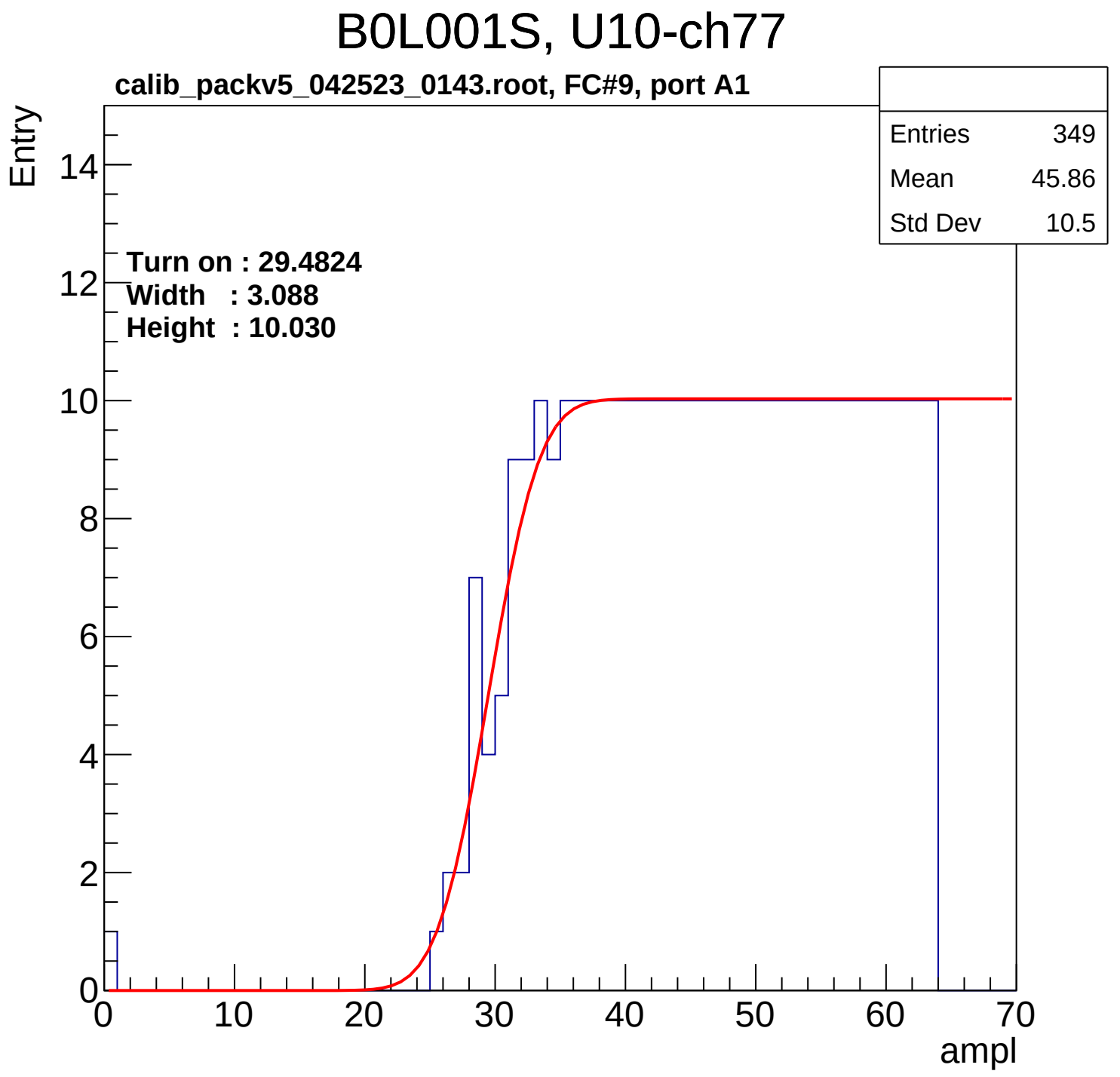

B0L001S, U10-ch72
calib_packv5_042523_0143.root, FC#9, port A1
Entries 347
Mean 45.65
Std Dev 11.37
Turn on : 29.8768
Width : 3.108
Height : 10.052
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

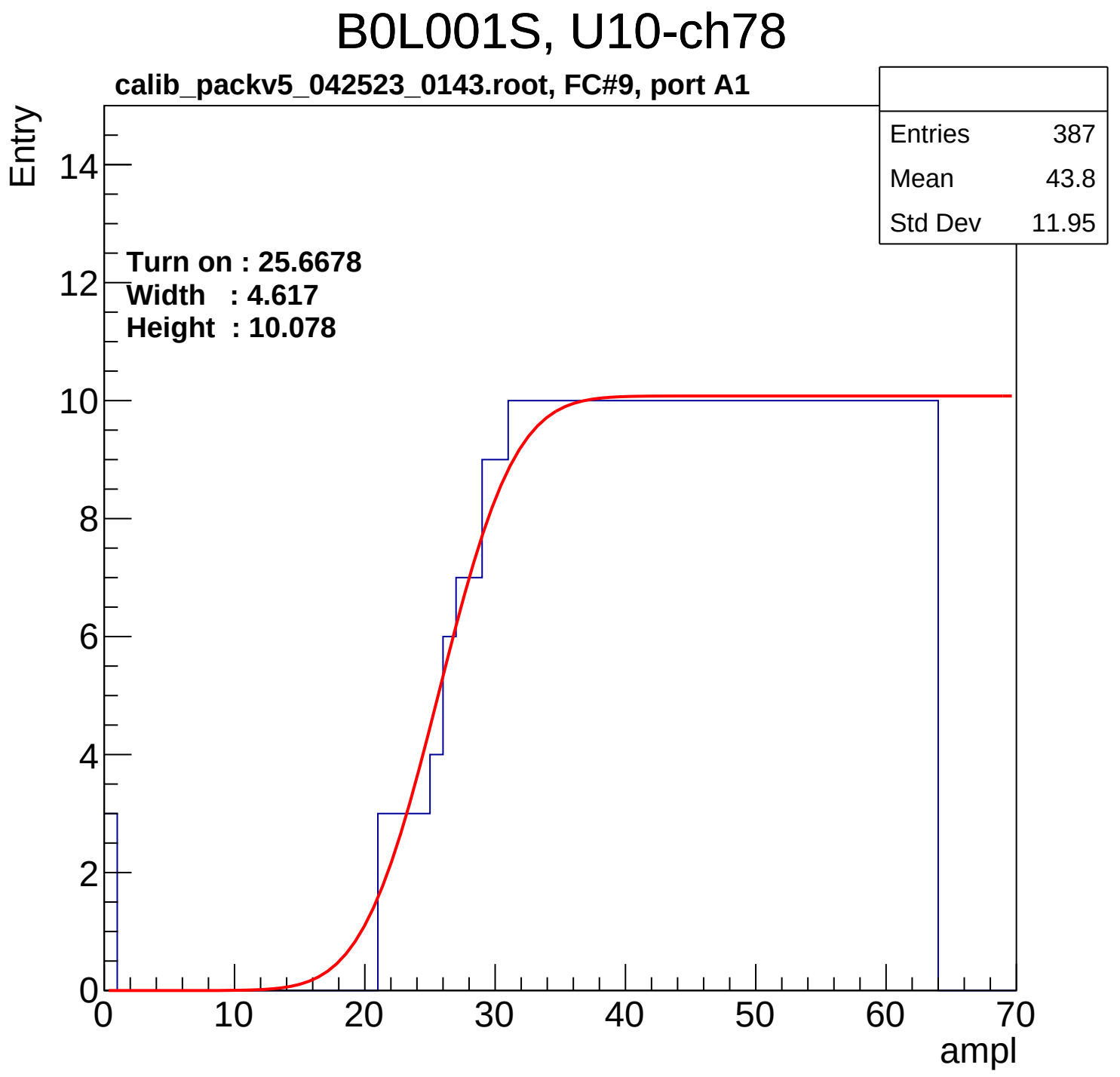

B0L001S, U10-ch73
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 45.13
Std Dev 10.88
Turn on : 27.7347
Width : 2.330
Height : 9.966
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

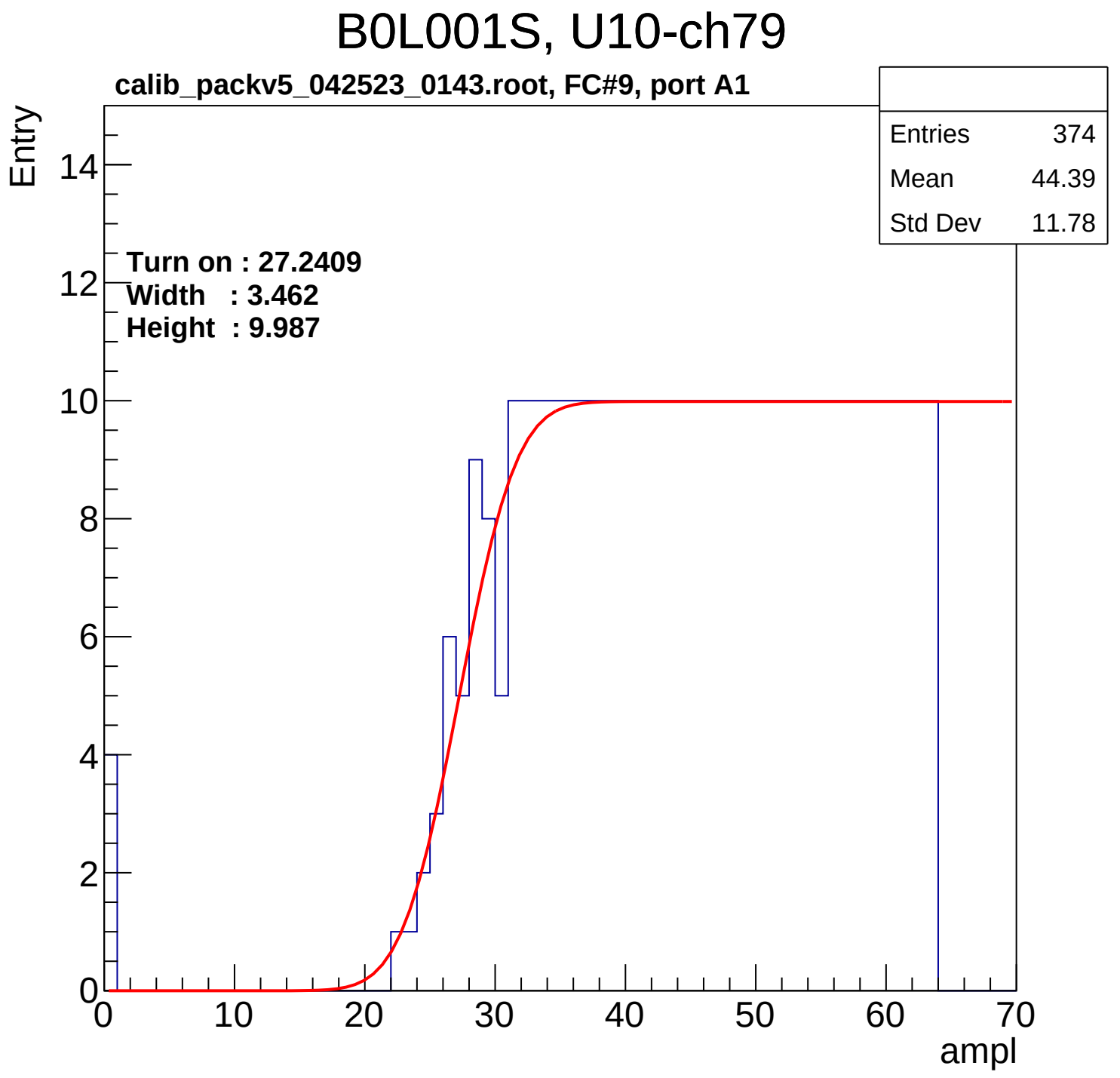

B0L001S, U10-ch74
calib_packv5_042523_0143.root, FC#9, port A1
Entries 374
Mean 44.52
Std Dev 11.5
Turn on : 27.0272
Width : 2.628
Height : 10.026
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

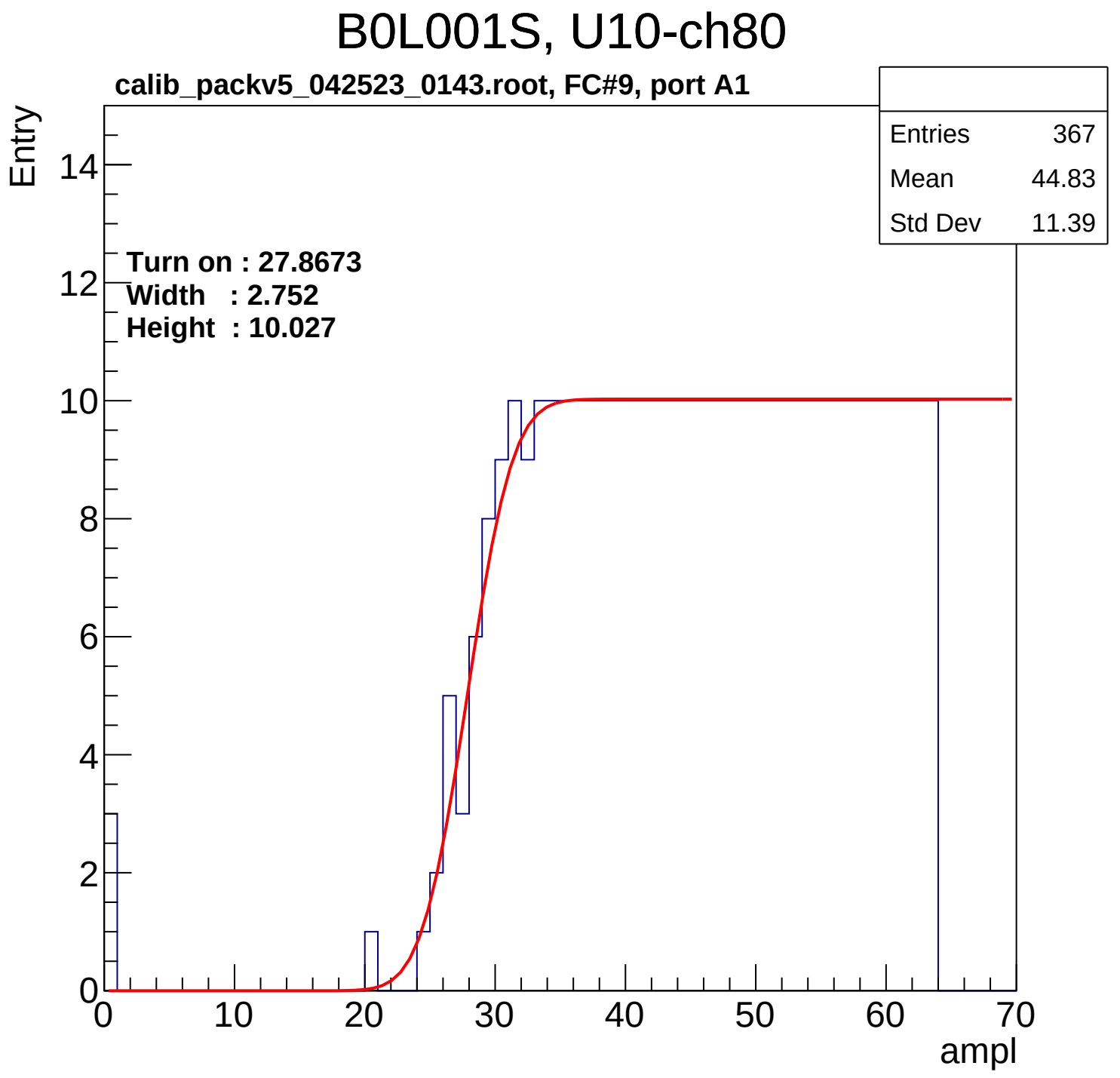

B0L001S, U10-ch75
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 45.12
Std Dev 11.24
Turn on : 28.2386
Width : 2.053
Height : 9.941
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

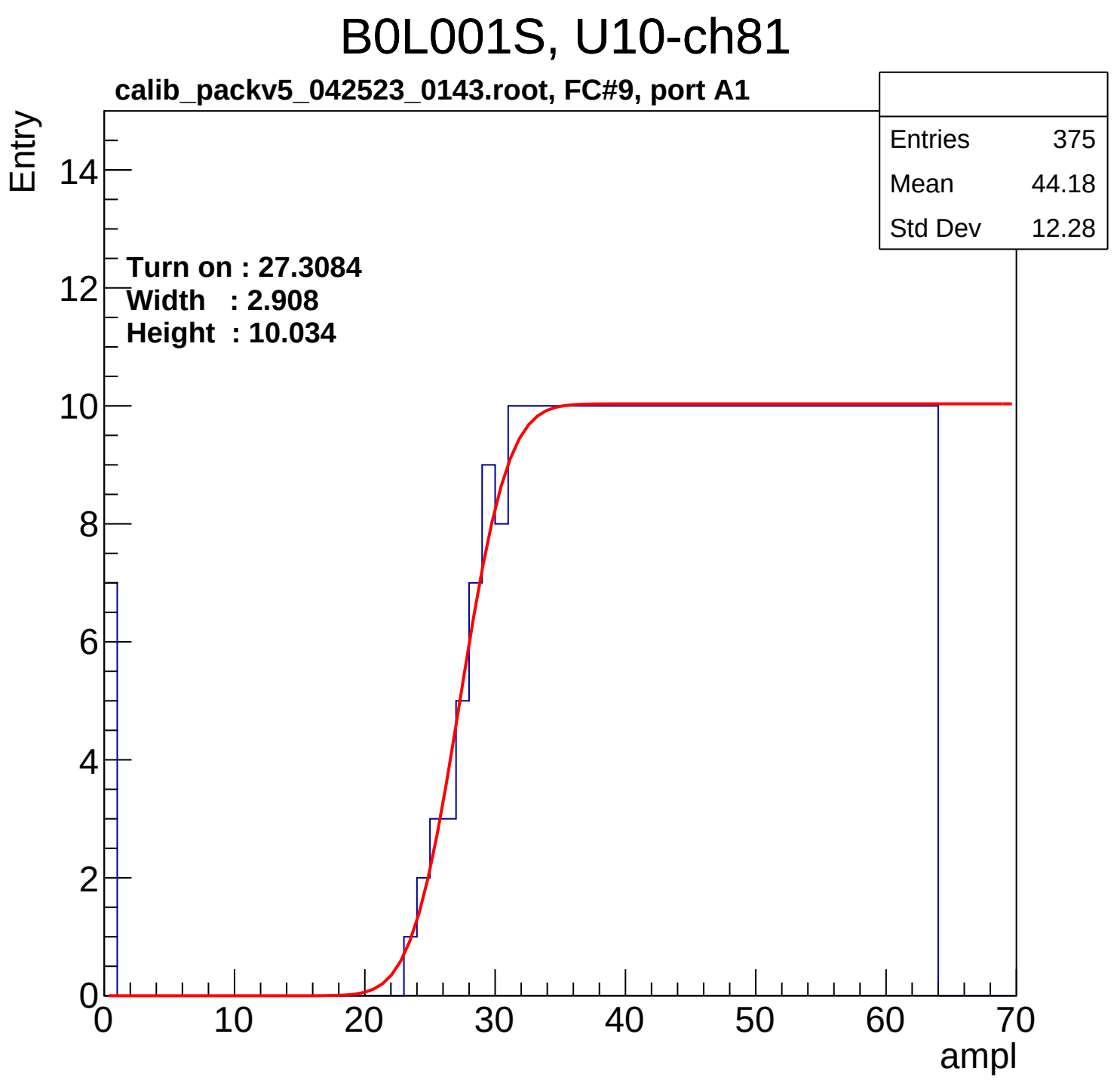

B0L001S, U10-ch76
calib_packv5_042523_0143.root, FC#9, port A1
Entries 355
Mean 45.22
Std Dev 11.6
Turn on : 29.4398
Width : 3.248
Height : 10.026
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

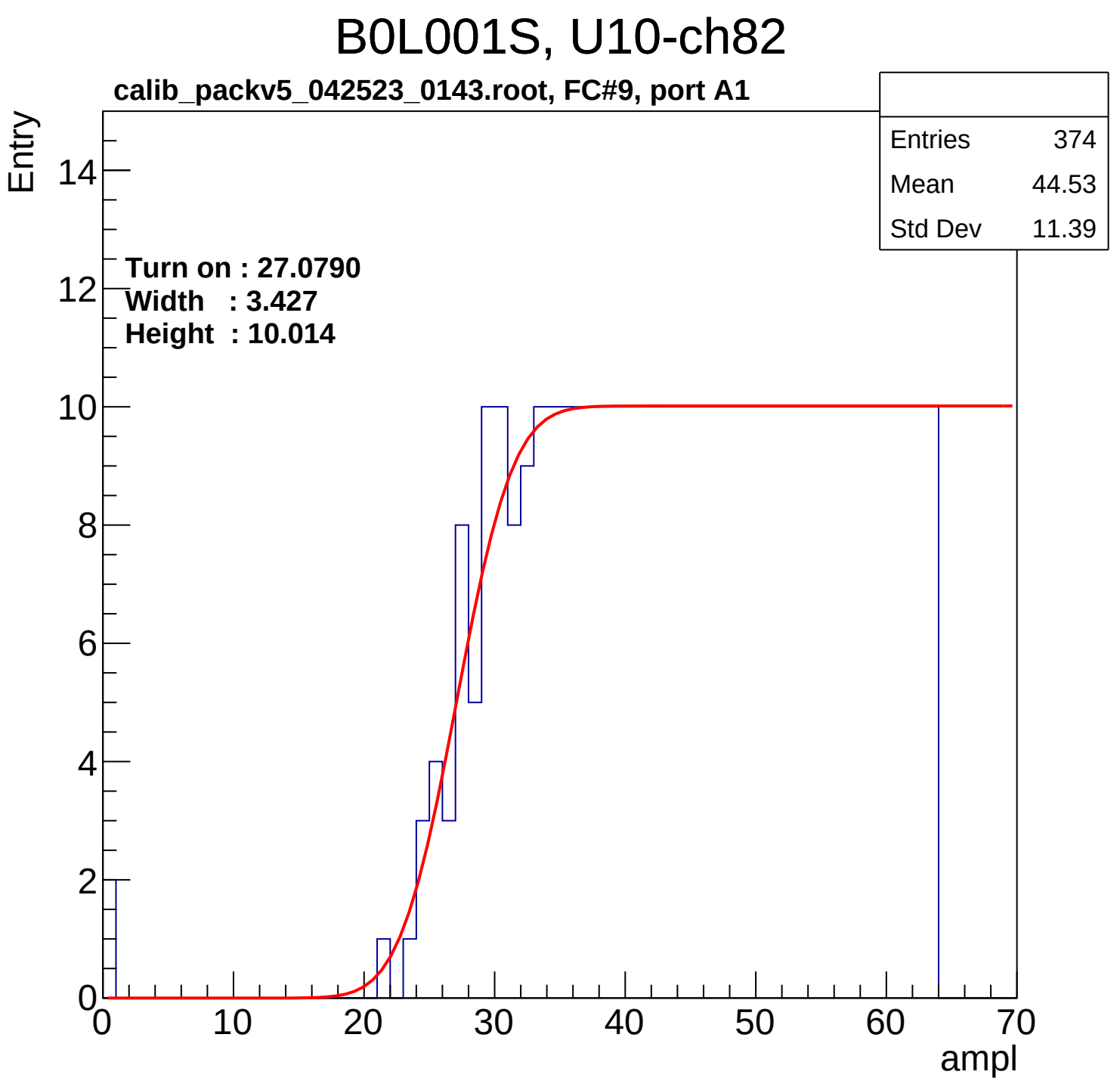

B0L001S, U10-ch77
calib_packv5_042523_0143.root, FC#9, port A1
Entries 349
Mean 45.86
Std Dev 10.5
Turn on : 29.4824
Width : 3.088
Height : 10.030
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

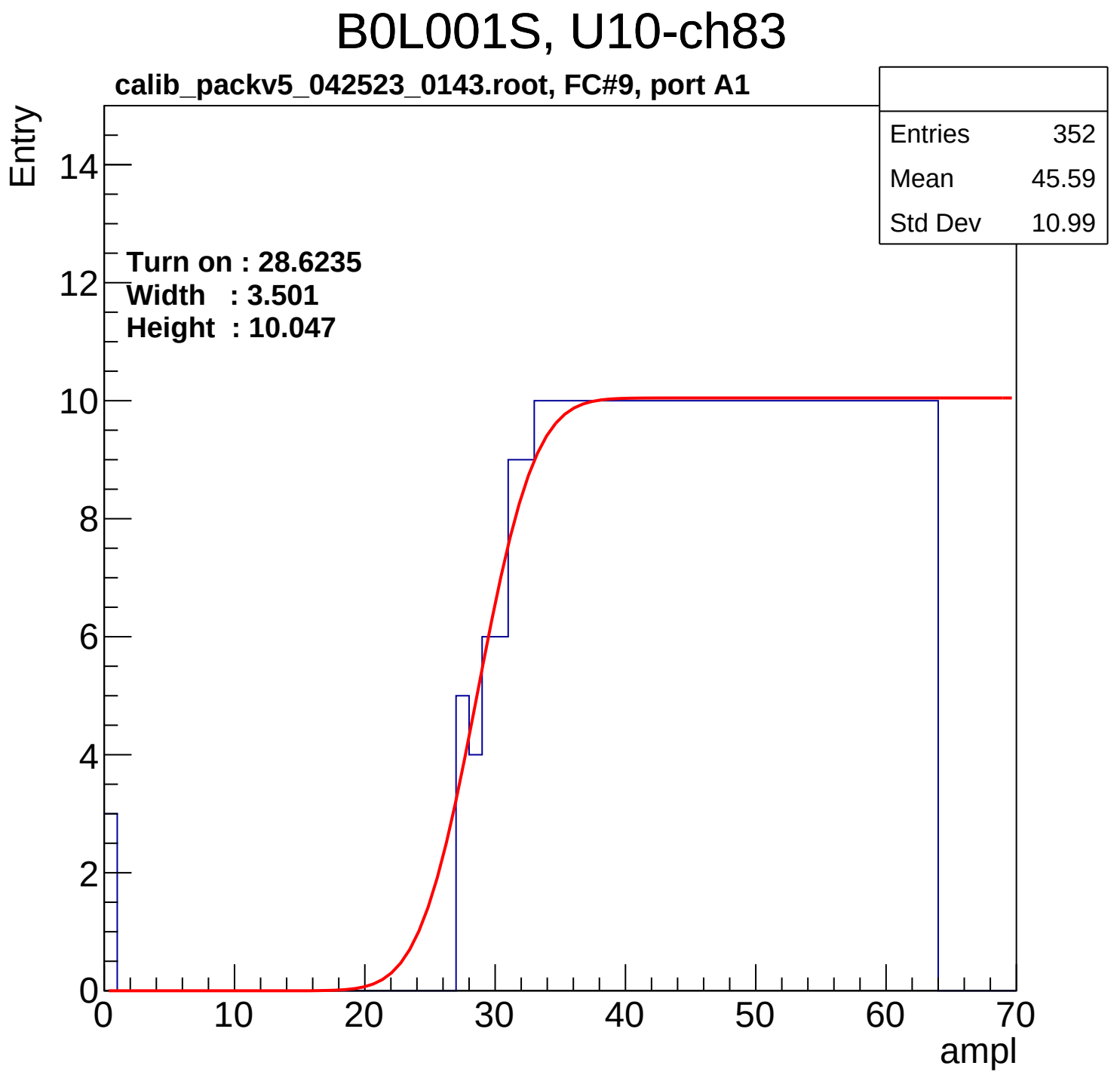

B0L001S, U10-ch78
calib_packv5_042523_0143.root, FC#9, port A1
Entries 387
Mean 43.8
Std Dev 11.95
Turn on : 25.6678
Width : 4.617
Height : 10.078
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

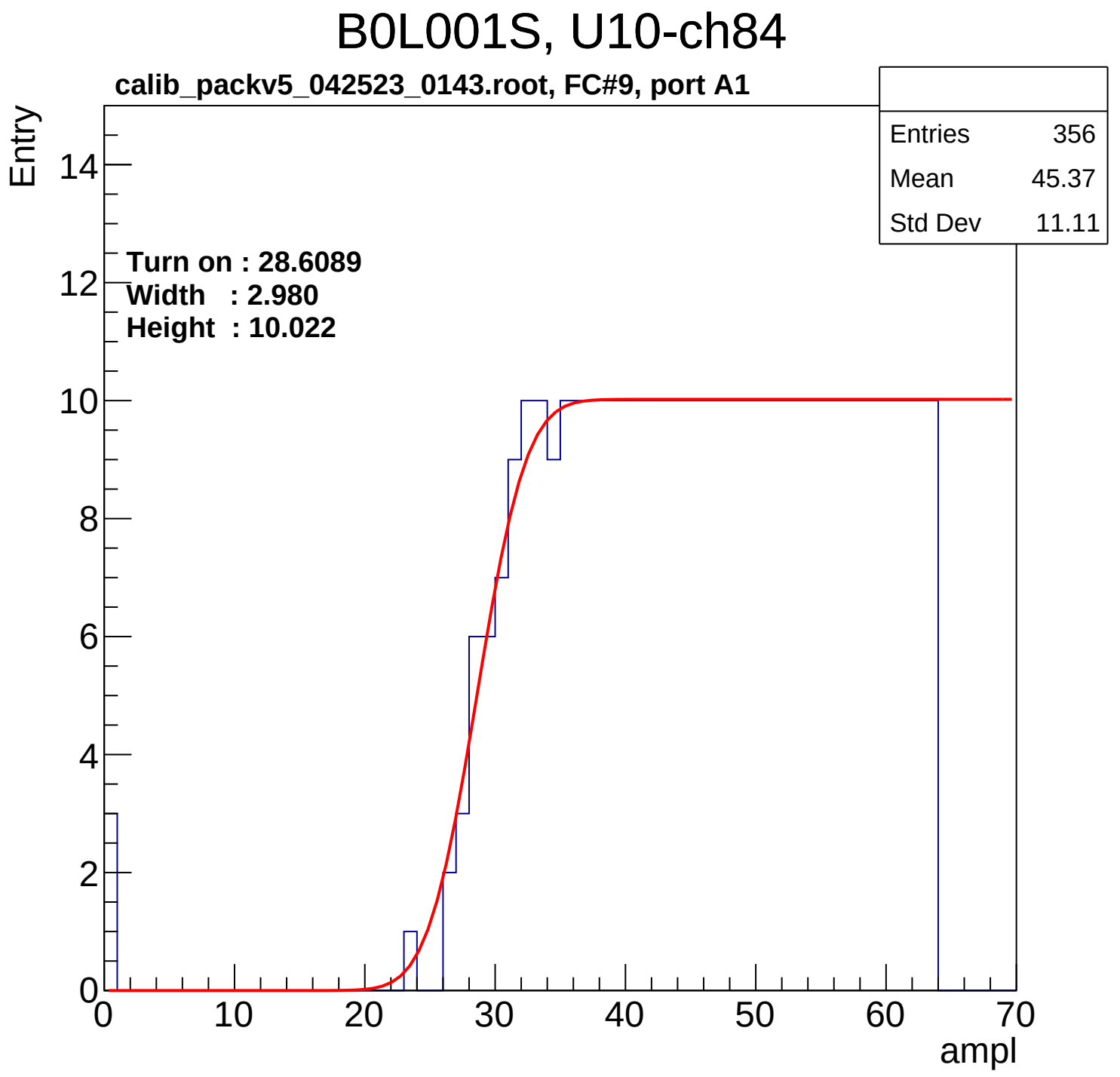

B0L001S, U10-ch79
calib_packv5_042523_0143.root, FC#9, port A1
Entries 374
Mean 44.39
Std Dev 11.78
Turn on : 27.2409
Width : 3.462
Height : 9.987
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

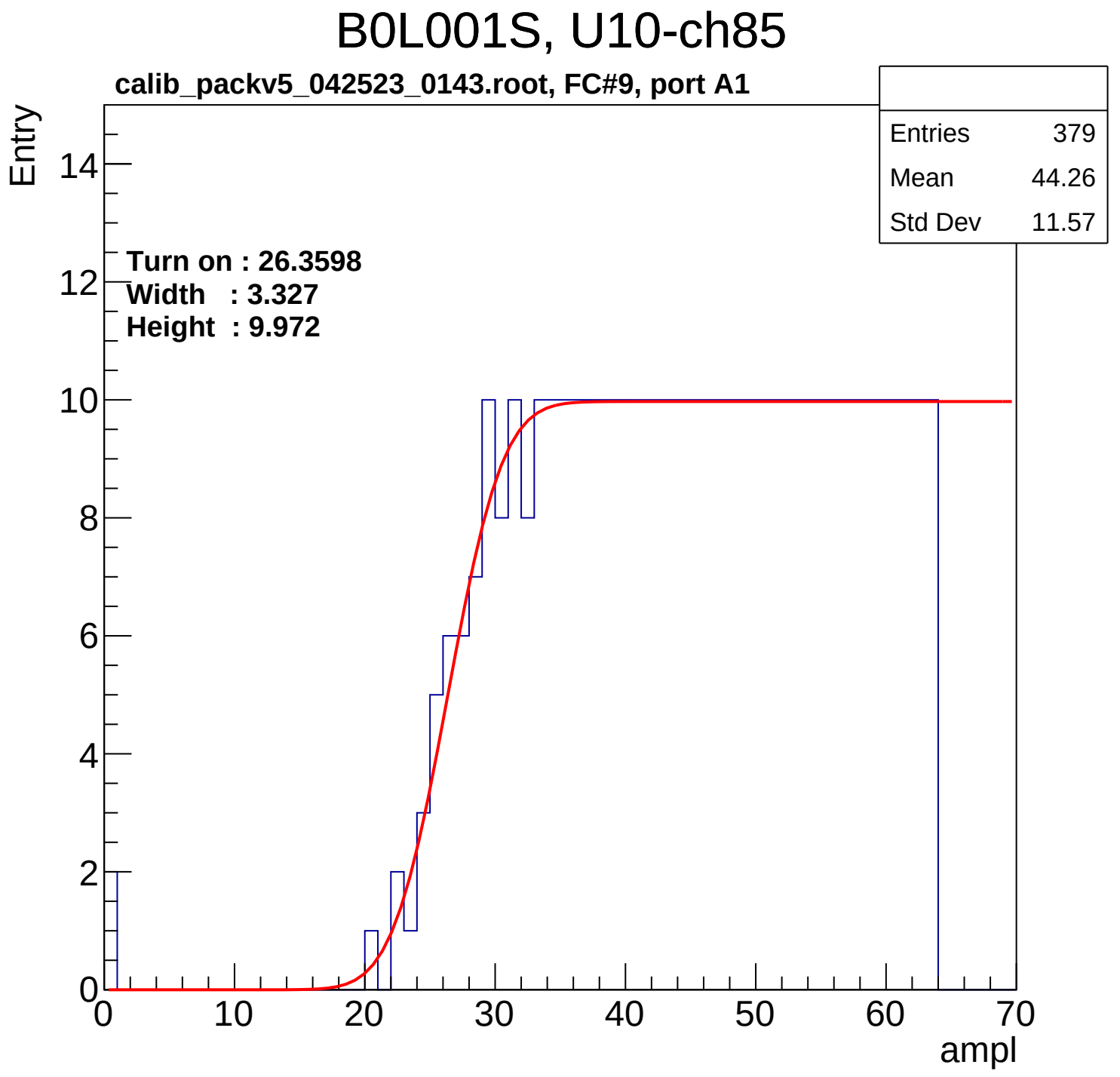

B0L001S, U10-ch80
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.83
Std Dev 11.39
Turn on : 27.8673
Width : 2.752
Height : 10.027
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

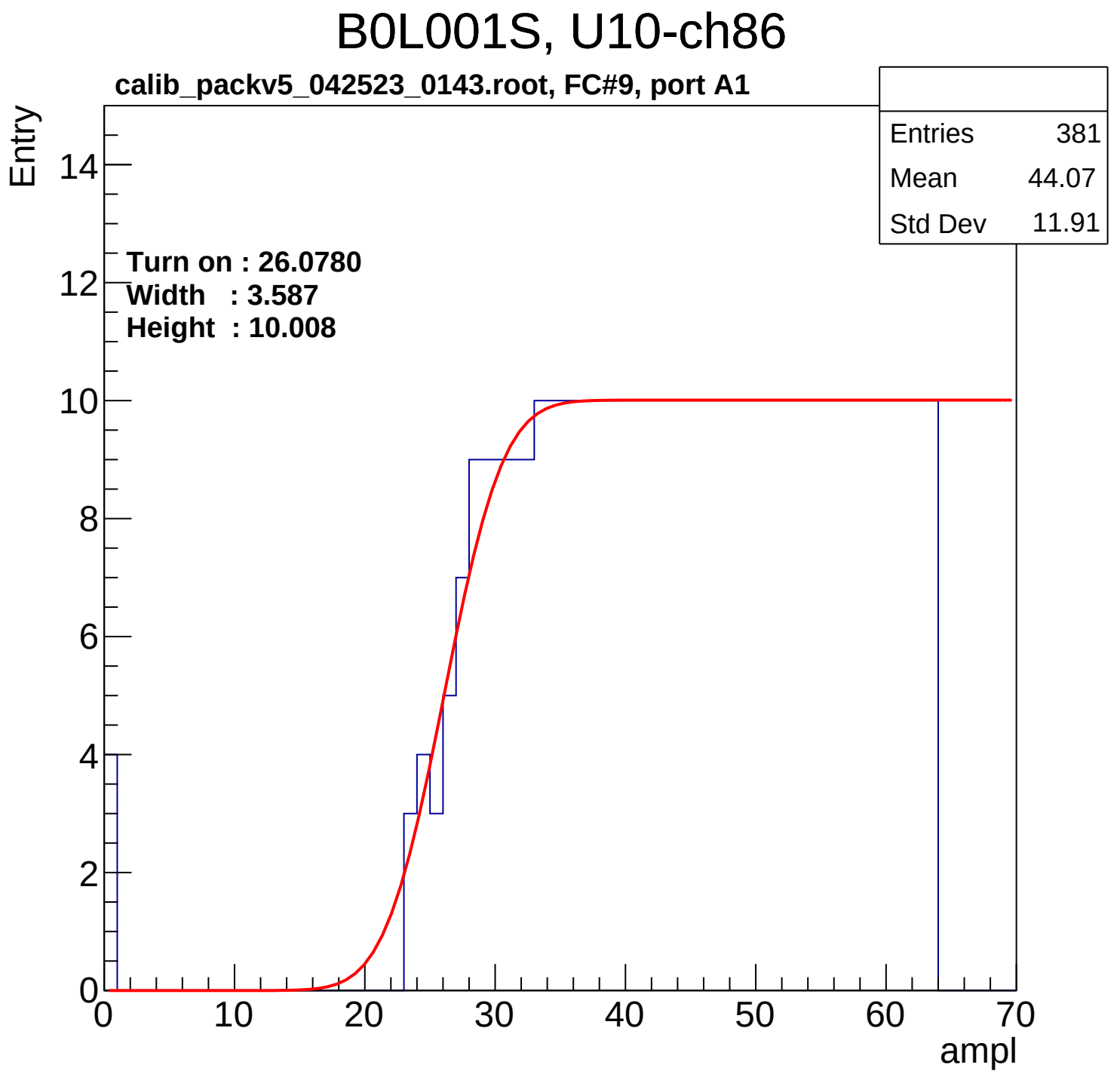

B0L001S, U10-ch81
calib_packv5_042523_0143.root, FC#9, port A1
Entries 375
Mean 44.18
Std Dev 12.28
Turn on : 27.3084
Width : 2.908
Height : 10.034
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

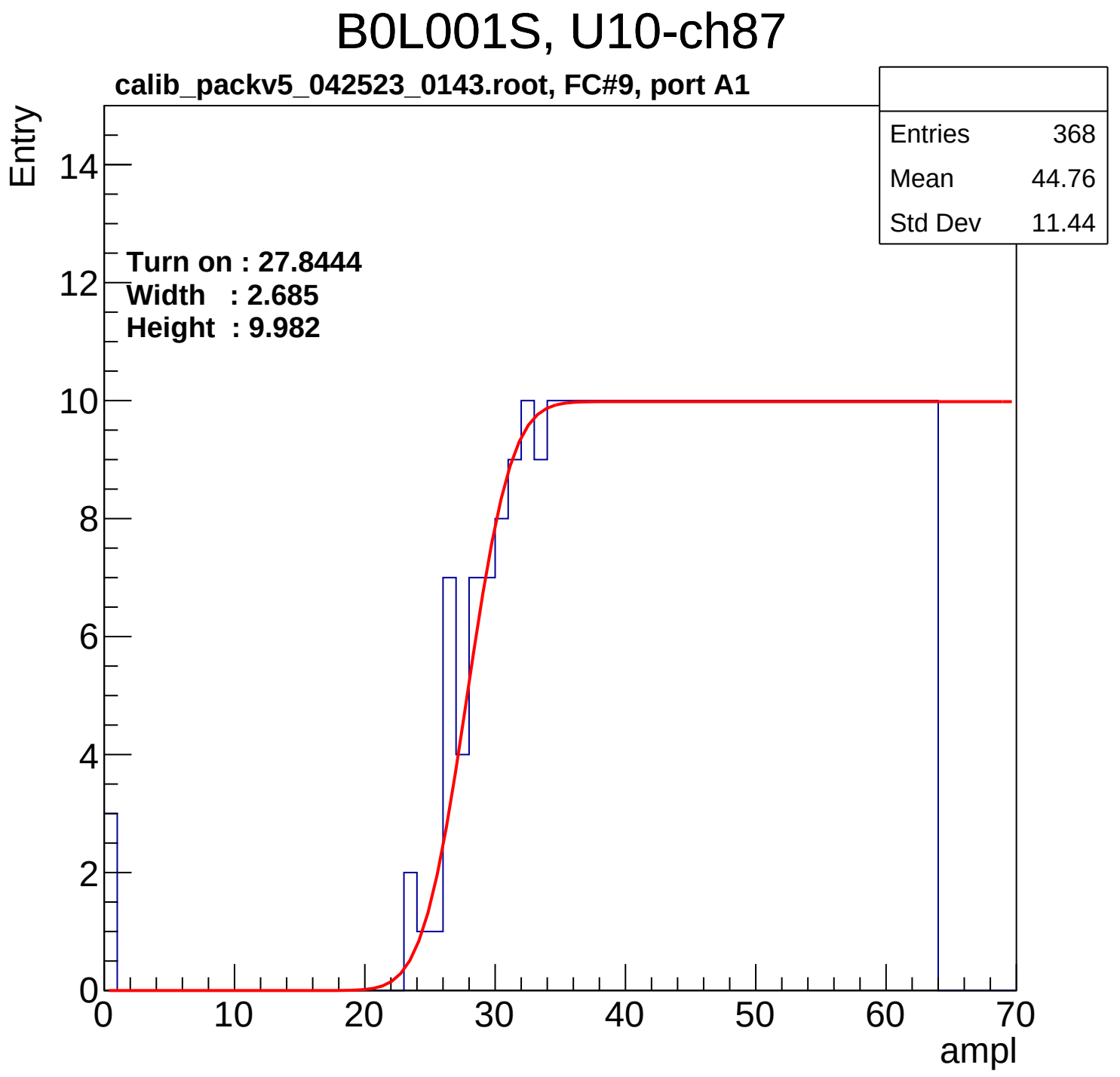

B0L001S, U10-ch82
calib_packv5_042523_0143.root, FC#9, port A1
Entries 374
Mean 44.53
Std Dev 11.39
Turn on : 27.0790
Width : 3.427
Height : 10.014
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

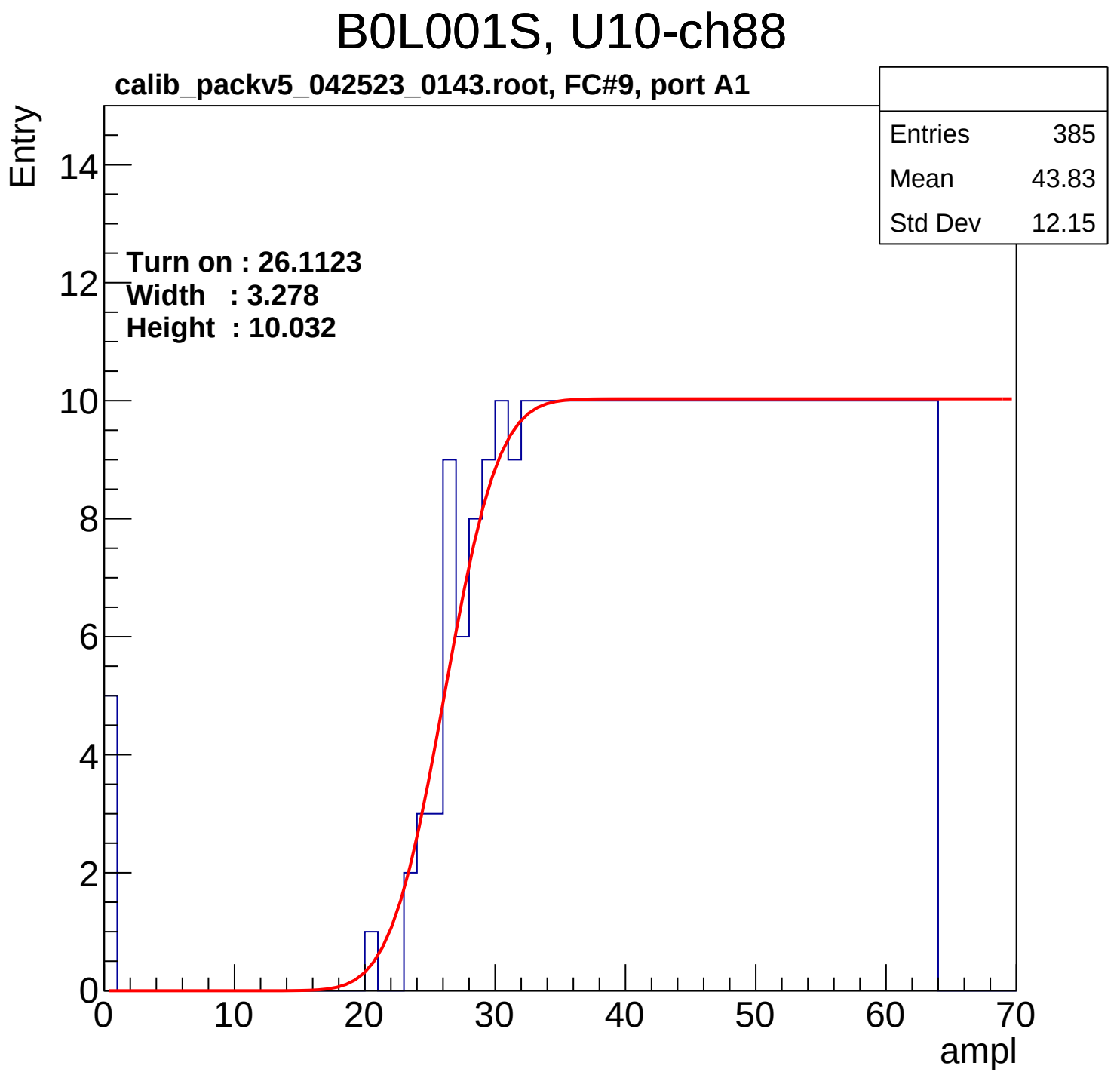

B0L001S, U10-ch83
calib_packv5_042523_0143.root, FC#9, port A1
Entries 352
Mean 45.59
Std Dev 10.99
Turn on : 28.6235
Width : 3.501
Height : 10.047
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

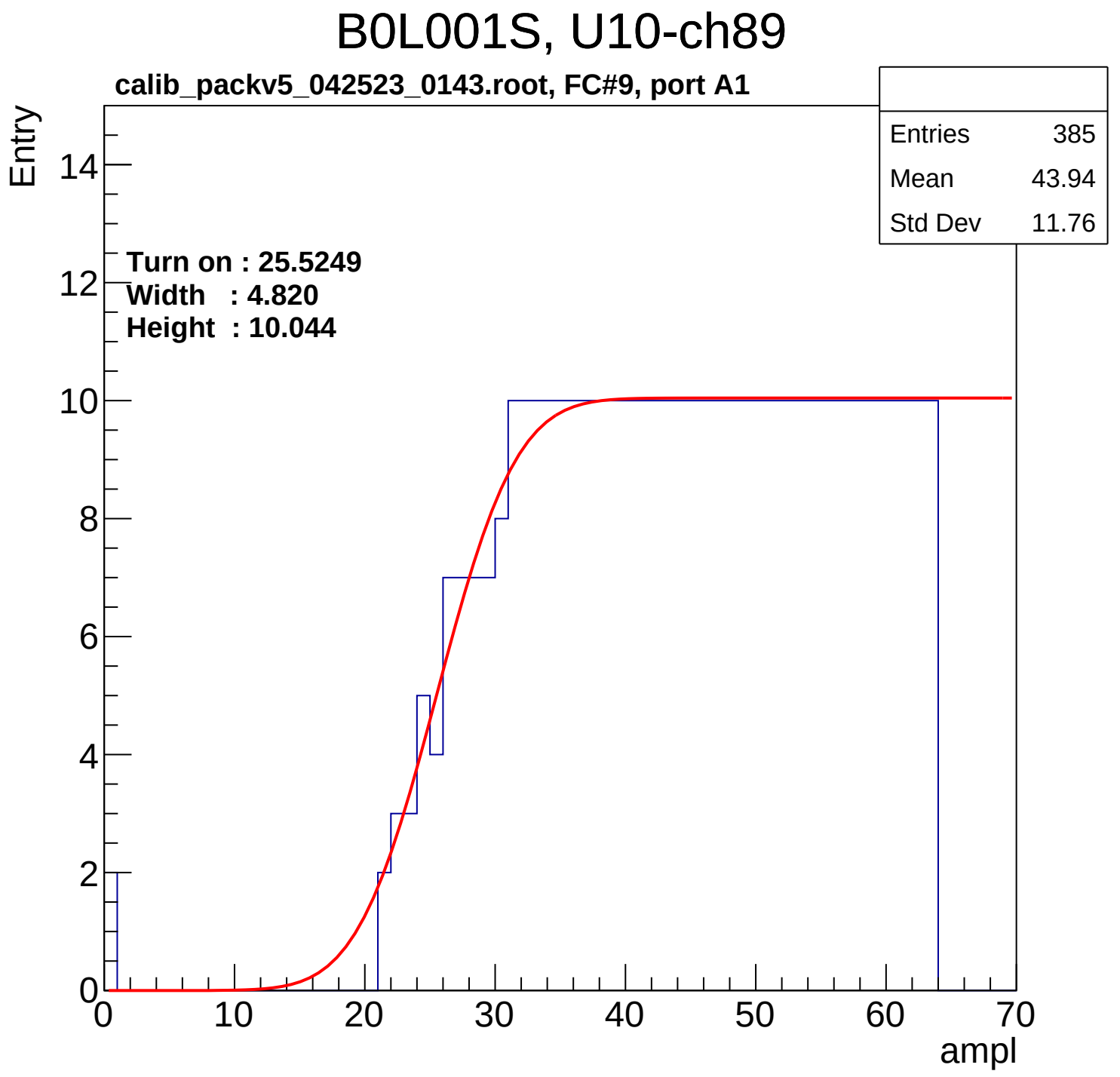

B0L001S, U10-ch84
calib_packv5_042523_0143.root, FC#9, port A1
Entries 356
Mean 45.37
Std Dev 11.11
Turn on : 28.6089
Width : 2.980
Height : 10.022
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

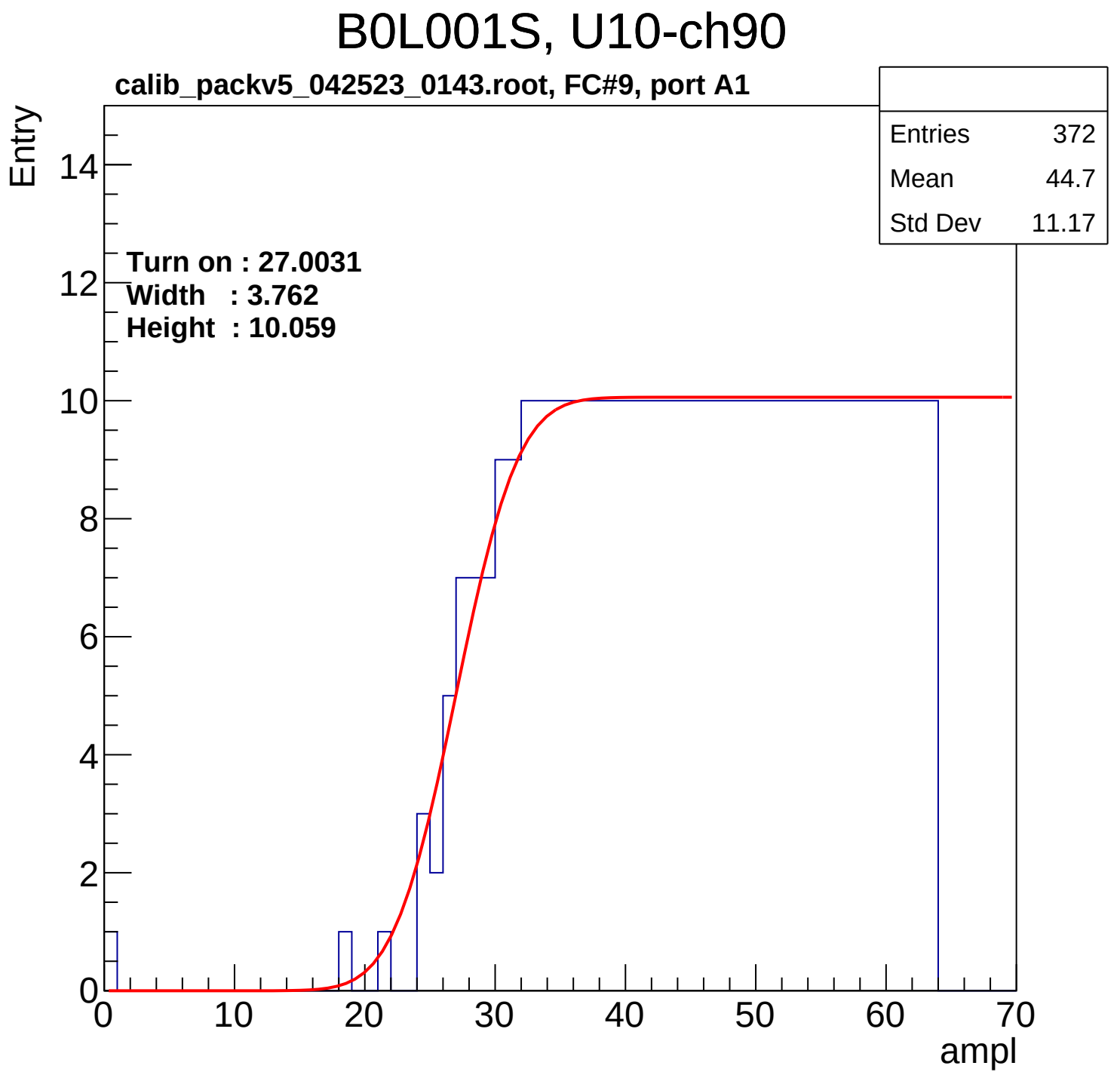

B0L001S, U10-ch85
calib_packv5_042523_0143.root, FC#9, port A1
Entries 379
Mean 44.26
Std Dev 11.57
Turn on : 26.3598
Width : 3.327
Height : 9.972
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

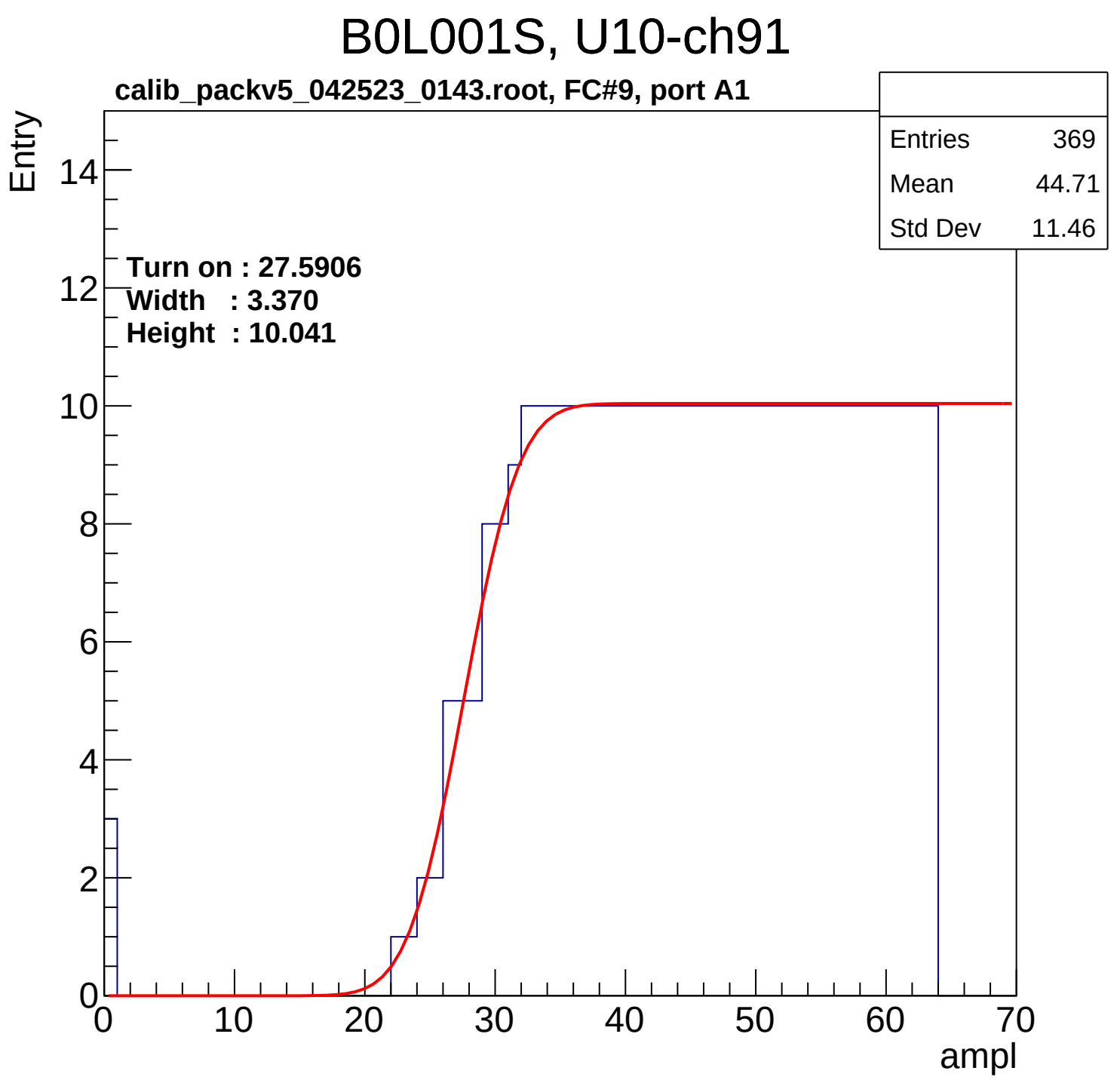

B0L001S, U10-ch86
calib_packv5_042523_0143.root, FC#9, port A1
Entries 381
Mean 44.07
Std Dev 11.91
Turn on : 26.0780
Width : 3.587
Height : 10.008
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

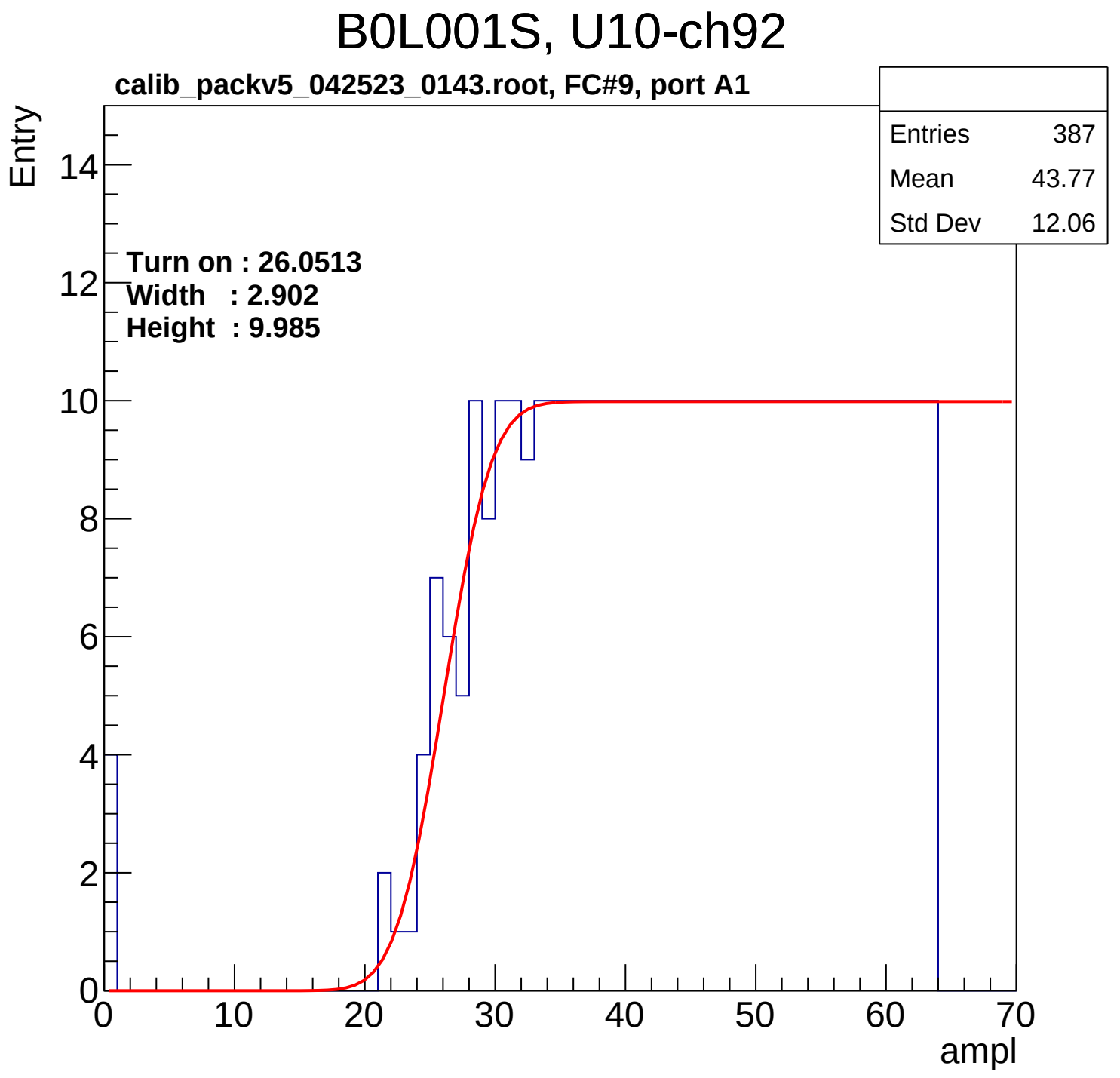

B0L001S, U10-ch87
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.76
Std Dev 11.44
Turn on : 27.8444
Width : 2.685
Height : 9.982
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

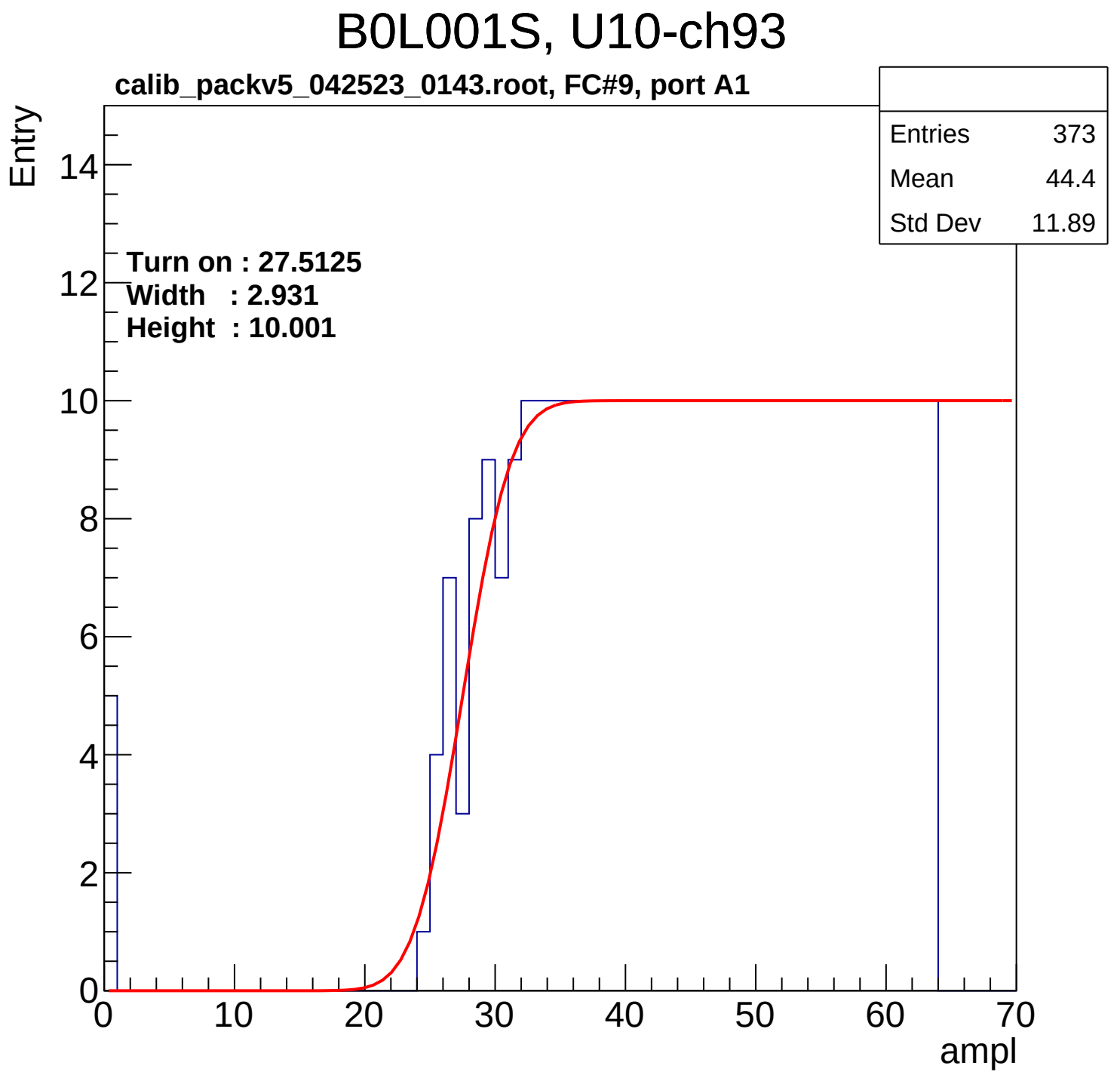

B0L001S, U10-ch88
calib_packv5_042523_0143.root, FC#9, port A1
Entries 385
Mean 43.83
Std Dev 12.15
Turn on : 26.1123
Width : 3.278
Height : 10.032
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

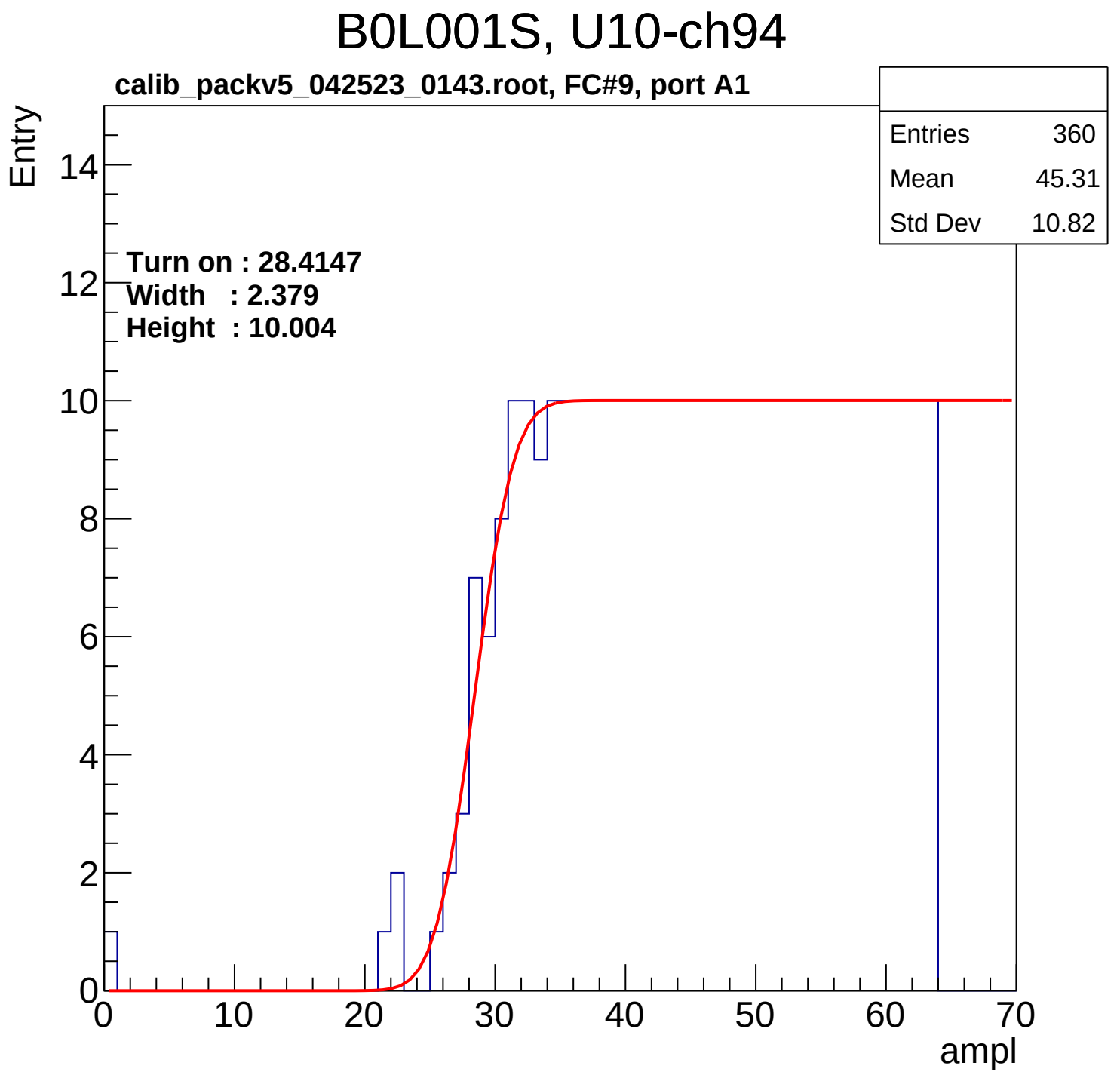

B0L001S, U10-ch89
calib_packv5_042523_0143.root, FC#9, port A1
Entries 385
Mean 43.94
Std Dev 11.76
Turn on : 25.5249
Width : 4.820
Height : 10.044
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

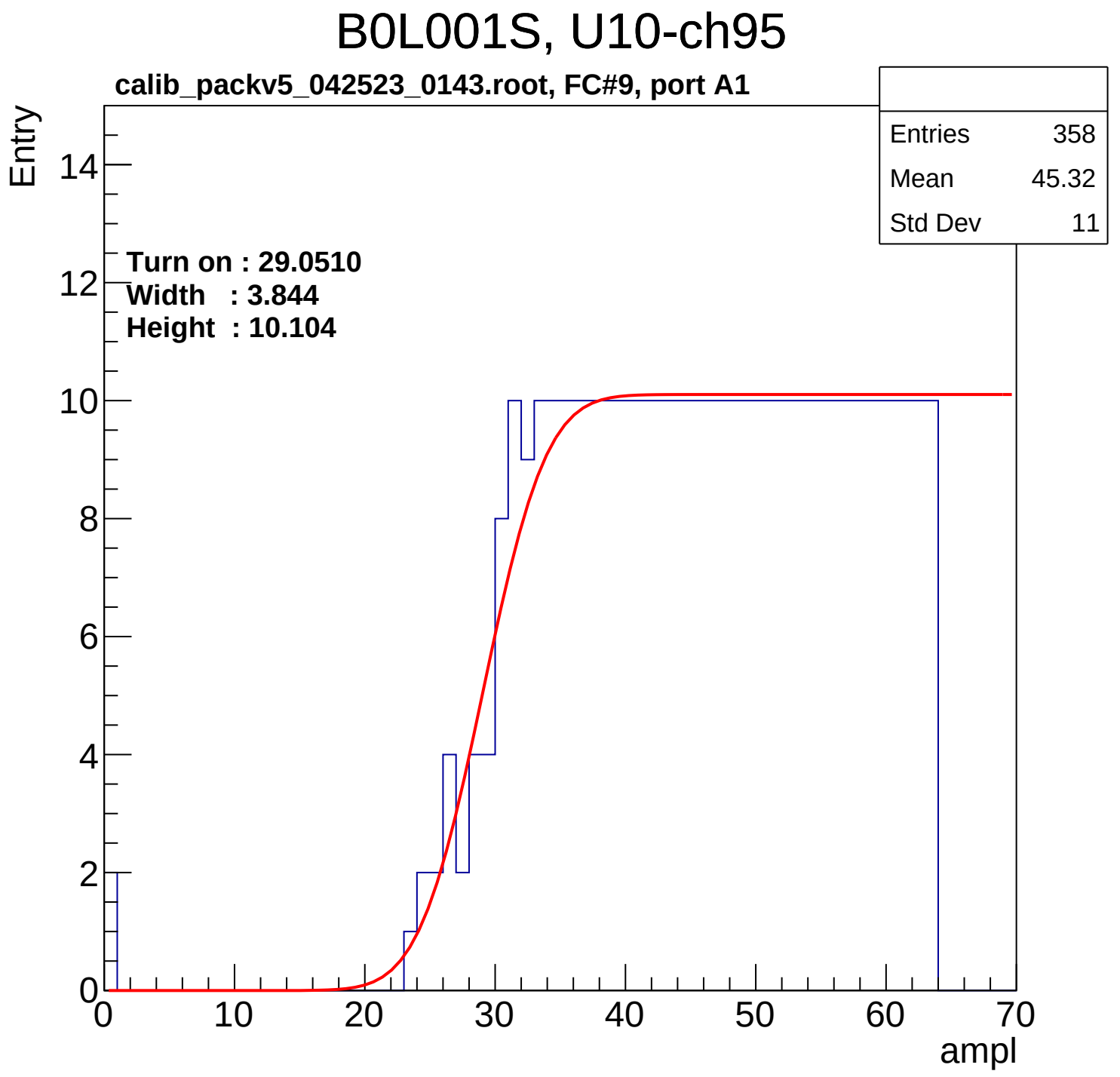

B0L001S, U10-ch90
calib_packv5_042523_0143.root, FC#9, port A1
Entries 372
Mean 44.7
Std Dev 11.17
Turn on : 27.0031
Width : 3.762
Height : 10.059
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

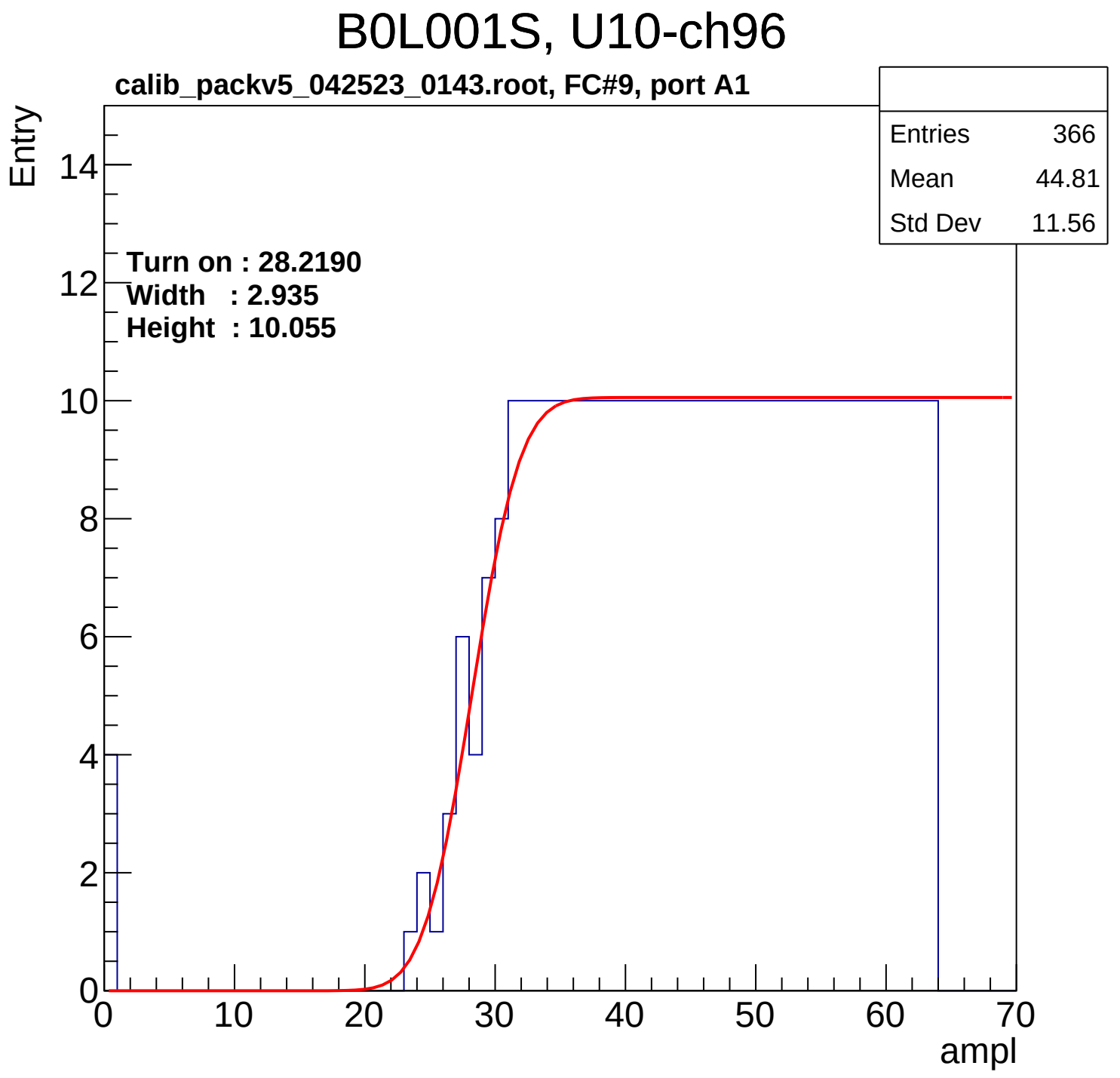

B0L001S, U10-ch91
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.71
Std Dev 11.46
Turn on : 27.5906
Width : 3.370
Height : 10.041
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

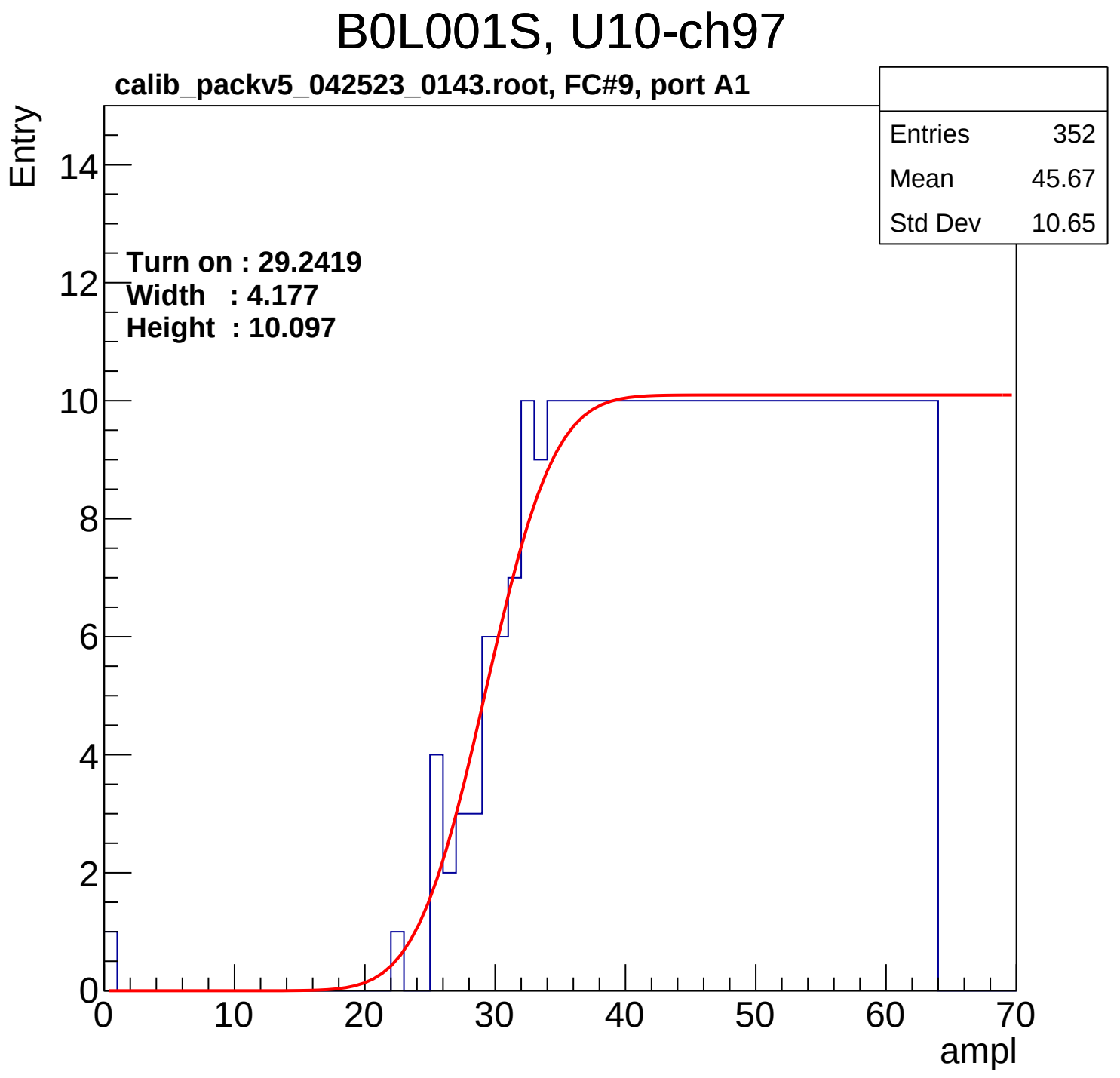

B0L001S, U10-ch92
calib_packv5_042523_0143.root, FC#9, port A1
Entries 387
Mean 43.77
Std Dev 12.06
Turn on : 26.0513
Width : 2.902
Height : 9.985
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

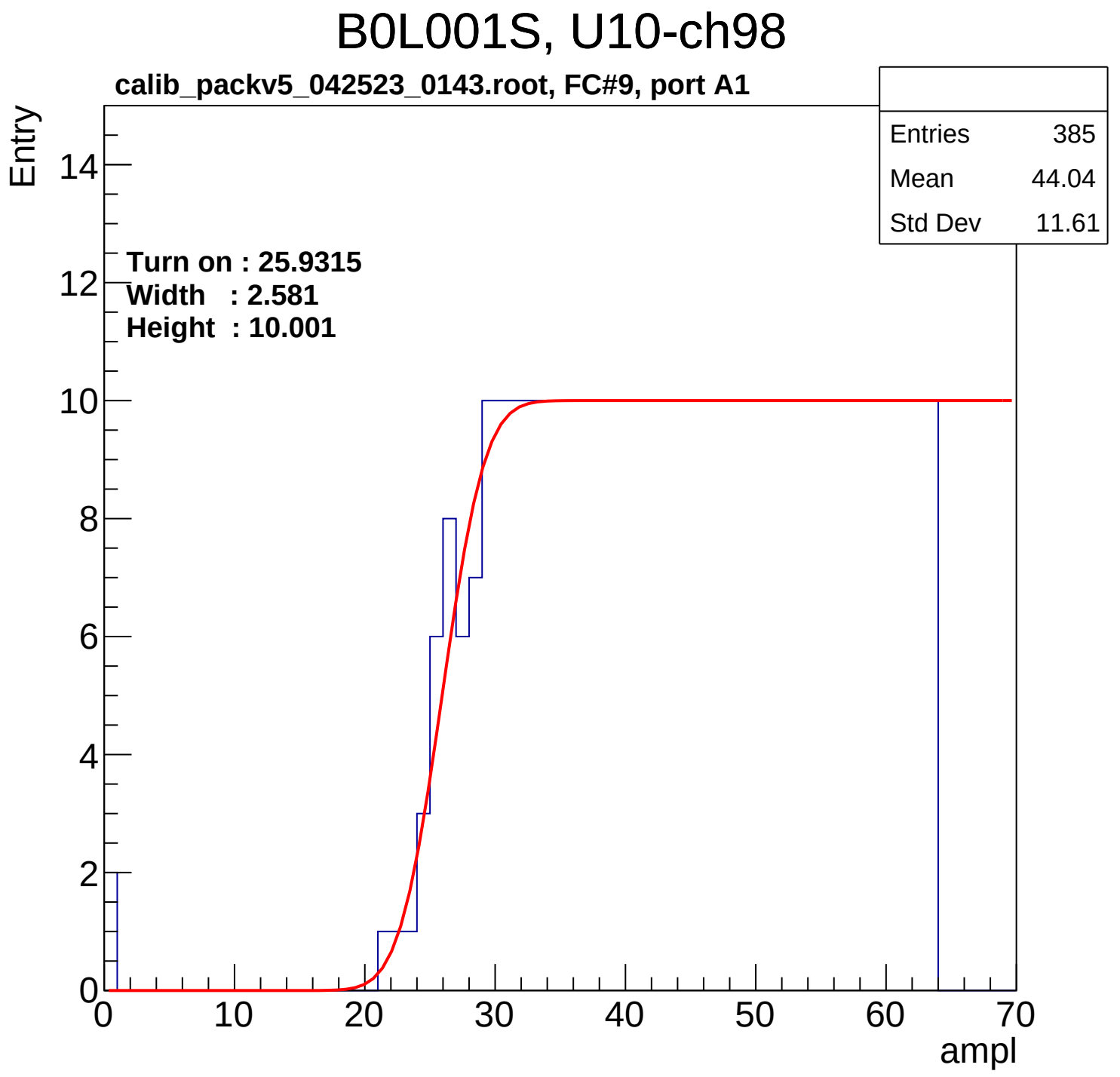

B0L001S, U10-ch93
calib_packv5_042523_0143.root, FC#9, port A1
Entries 373
Mean 44.4
Std Dev 11.89
Turn on : 27.5125
Width : 2.931
Height : 10.001
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

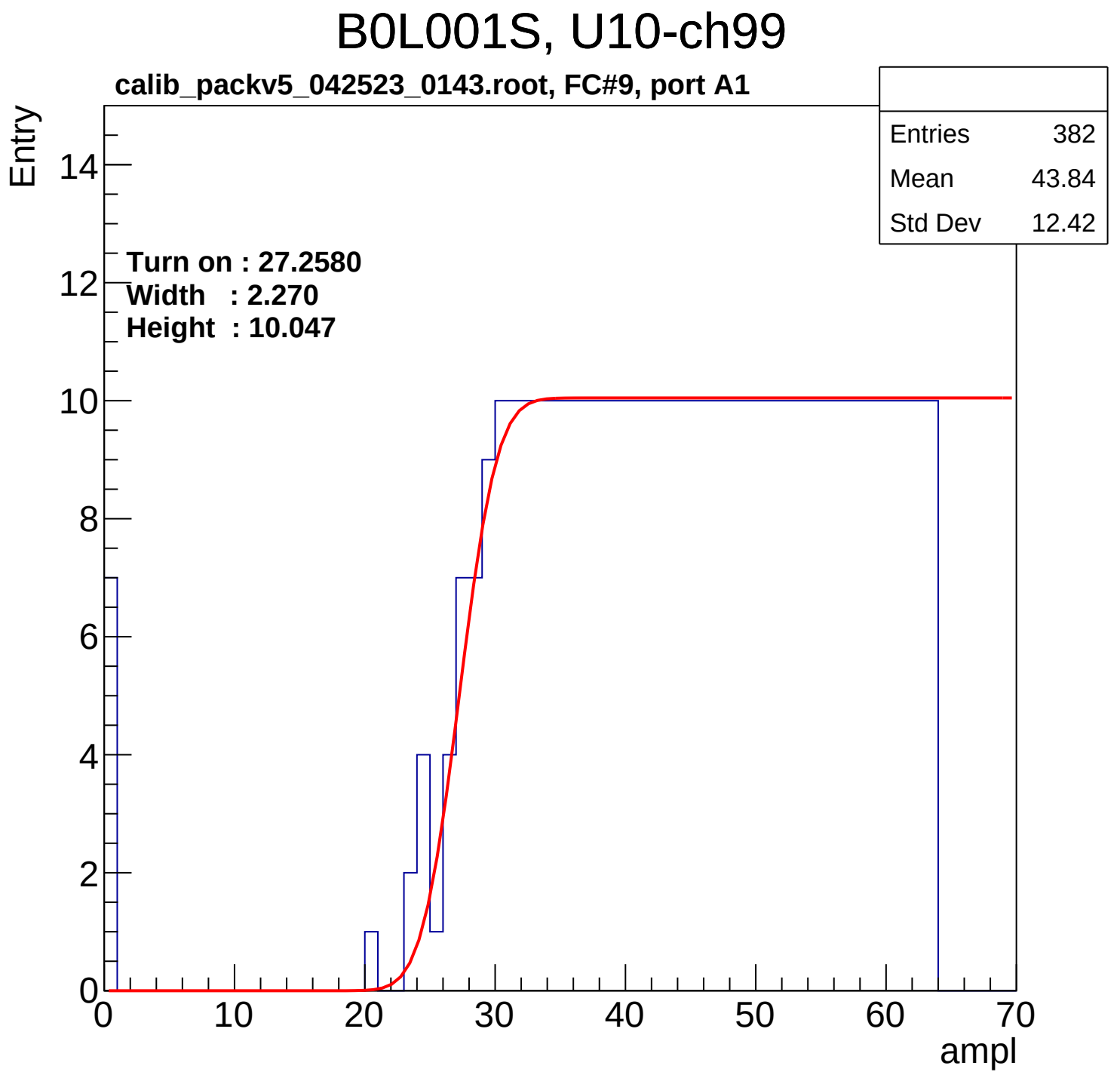

B0L001S, U10-ch94
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 45.31
Std Dev 10.82
Turn on : 28.4147
Width : 2.379
Height : 10.004
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

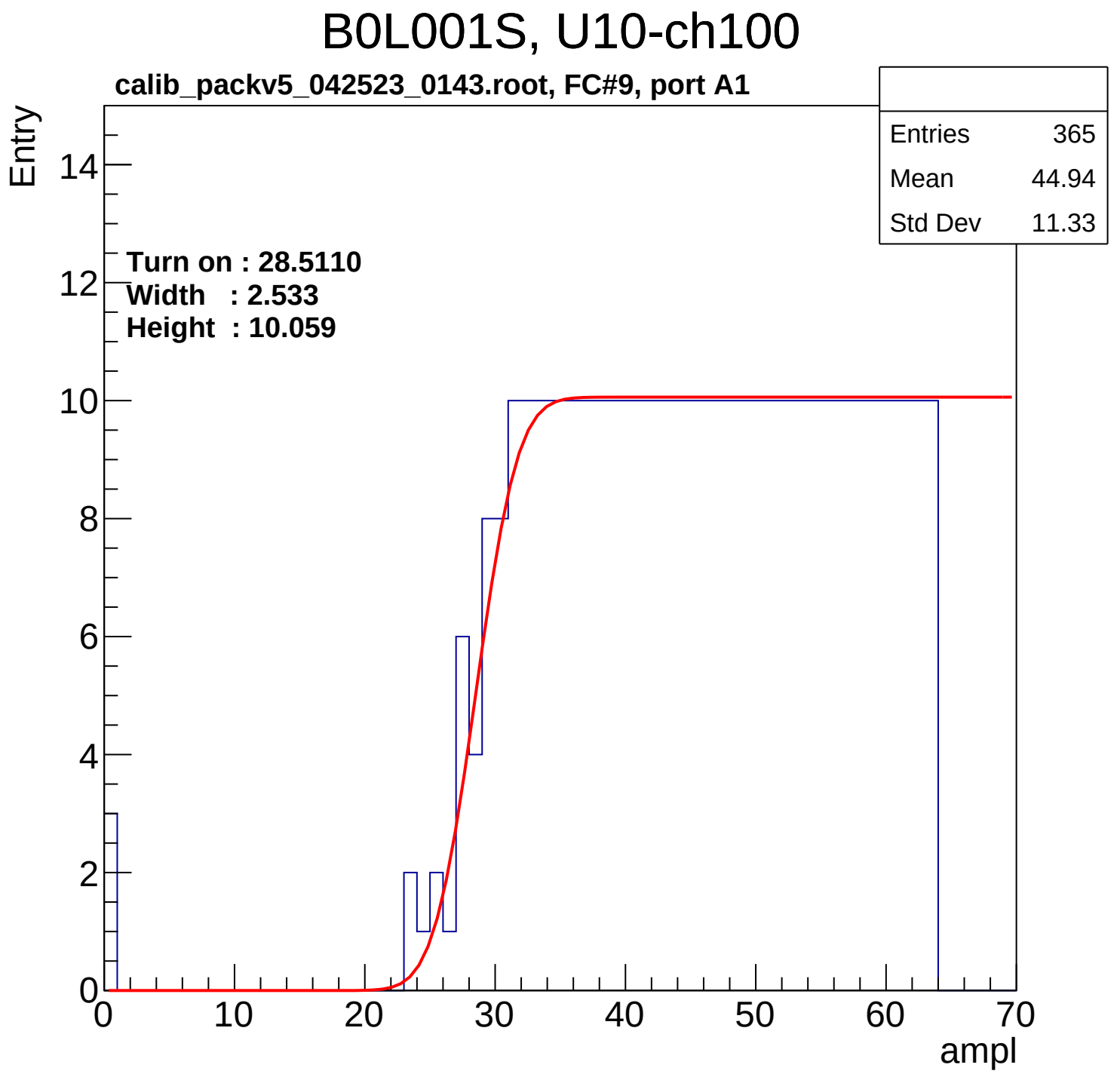

B0L001S, U10-ch95
calib_packv5_042523_0143.root, FC#9, port A1
Entries 358
Mean 45.32
Std Dev 11
Turn on : 29.0510
Width : 3.844
Height : 10.104
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

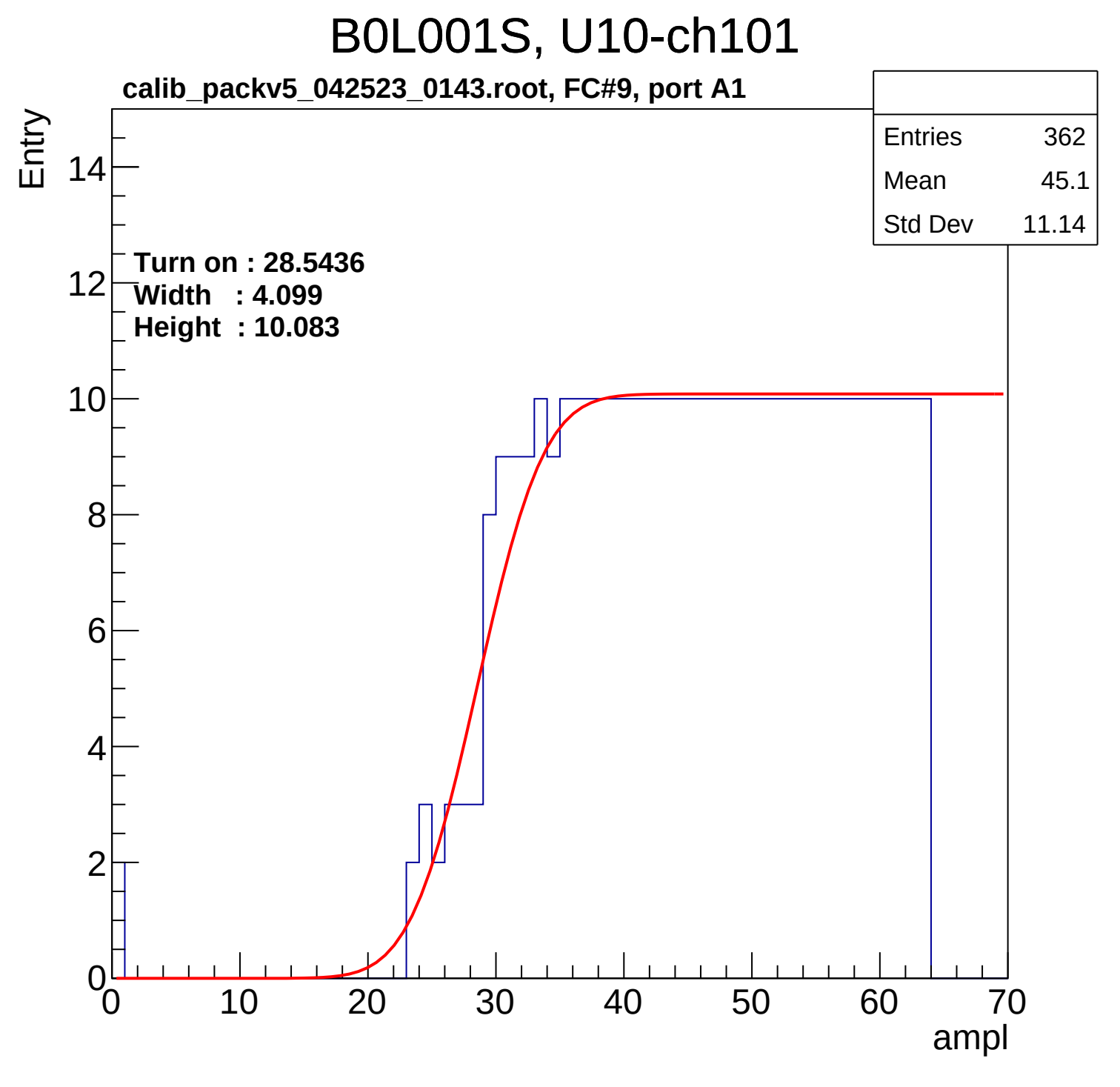

B0L001S, U10-ch96
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.81
Std Dev 11.56
Turn on : 28.2190
Width : 2.935
Height : 10.055
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

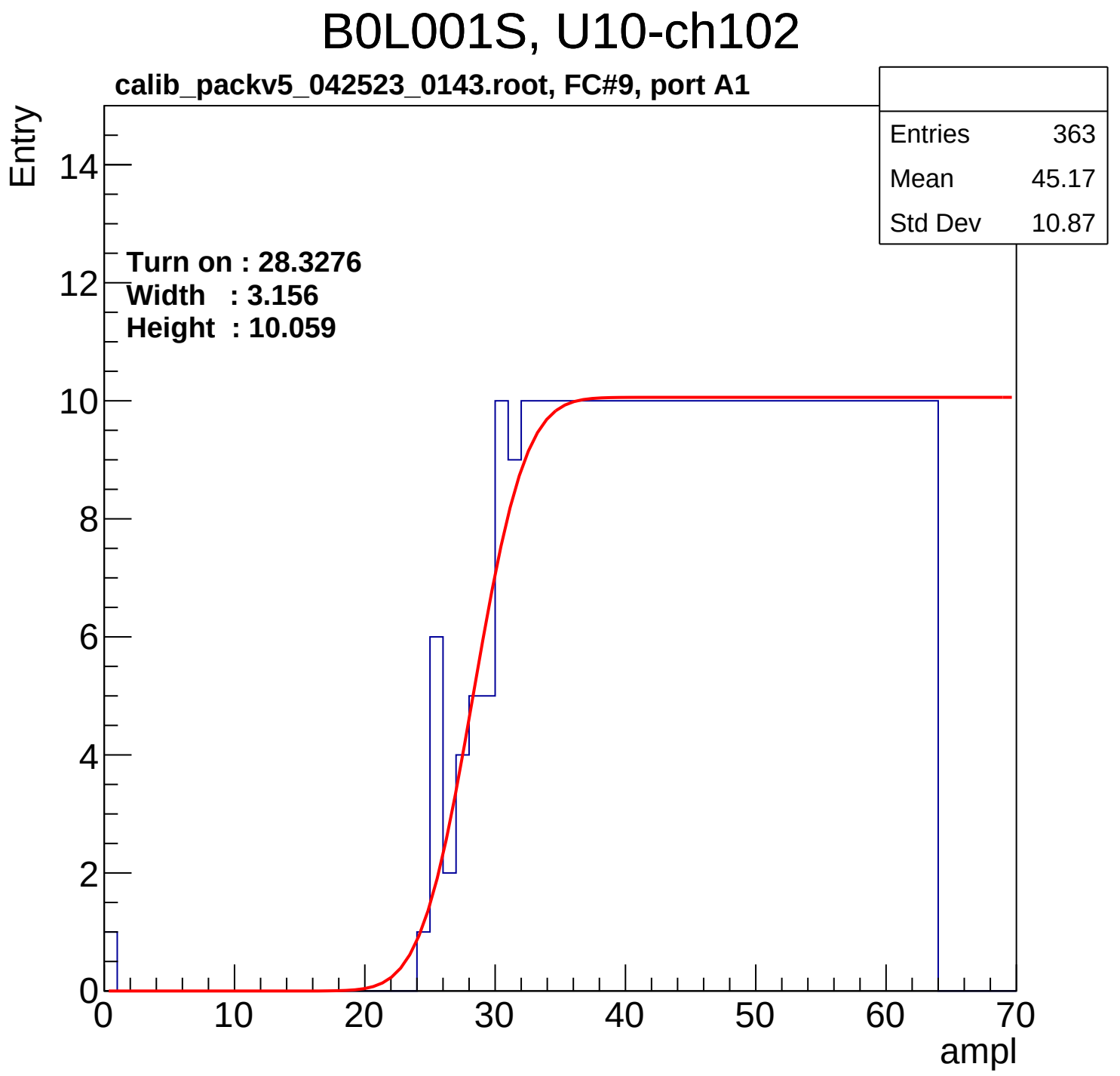

B0L001S, U10-ch97
calib_packv5_042523_0143.root, FC#9, port A1
Entries 352
Mean 45.67
Std Dev 10.65
Turn on : 29.2419
Width : 4.177
Height : 10.097
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

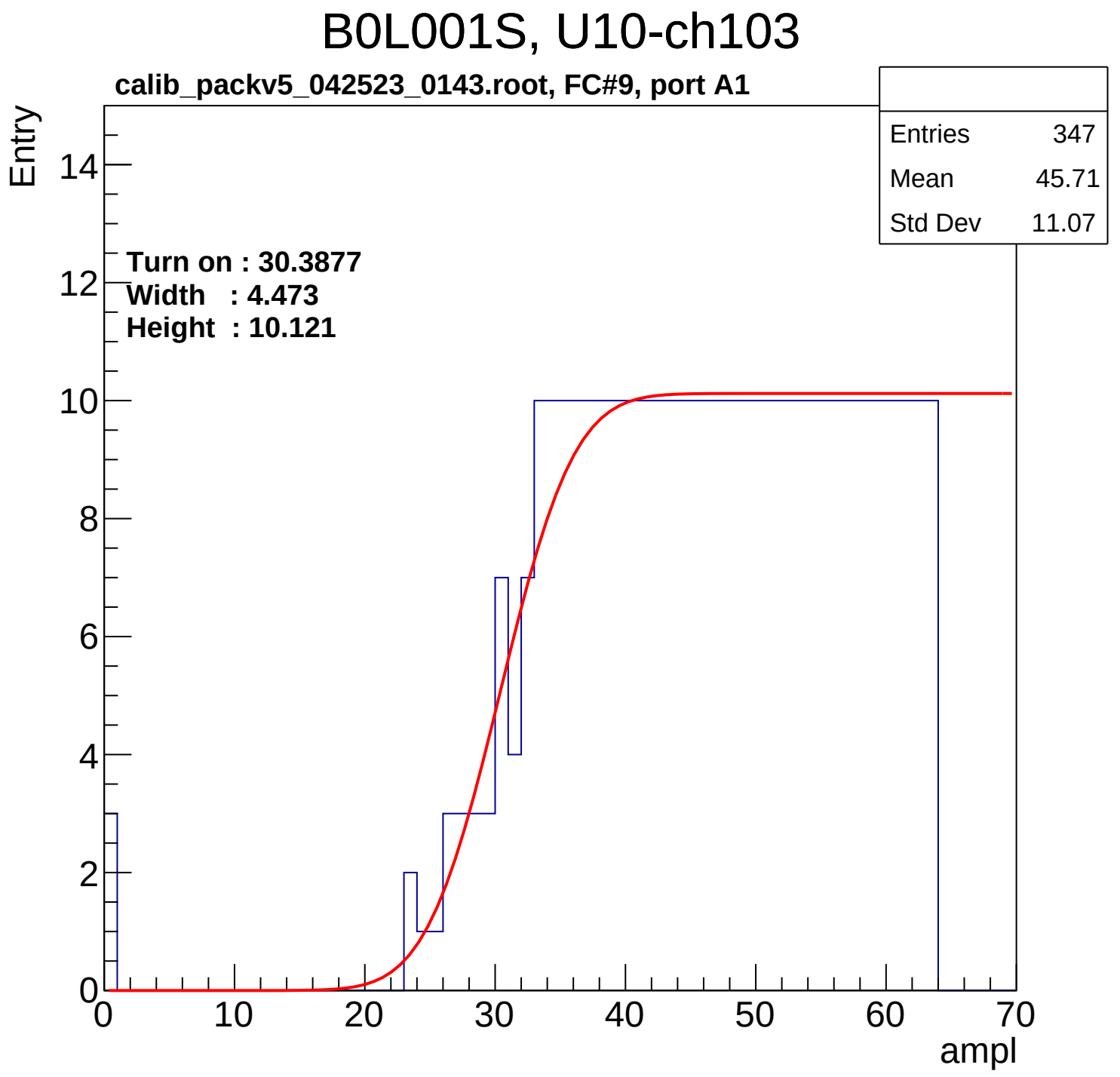

B0L001S, U10-ch98
calib_packv5_042523_0143.root, FC#9, port A1
Entries 385
Mean 44.04
Std Dev 11.61
Turn on : 25.9315
Width : 2.581
Height : 10.001
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

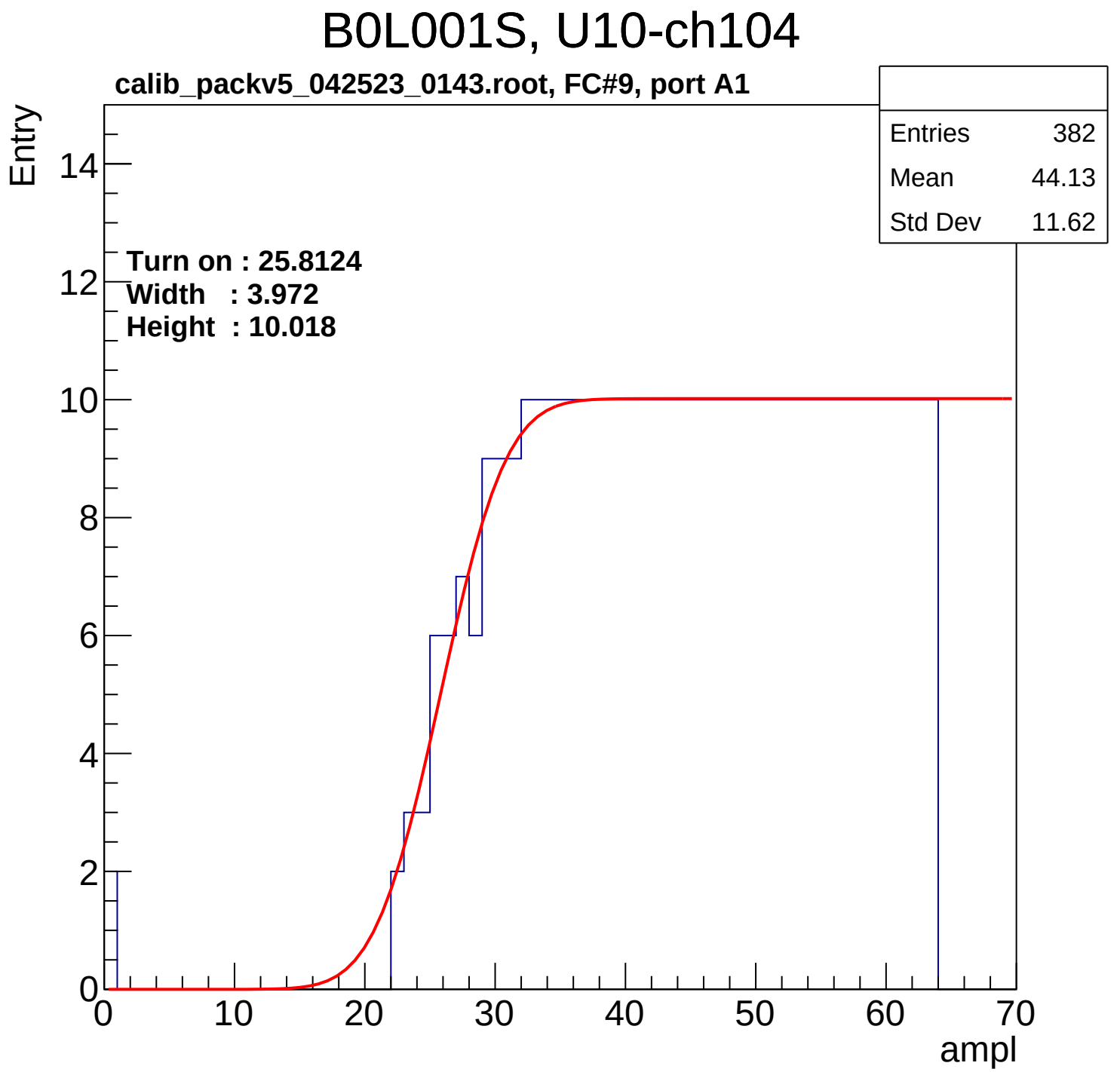

B0L001S, U10-ch99
calib_packv5_042523_0143.root, FC#9, port A1
Entries 382
Mean 43.84
Std Dev 12.42
Turn on : 27.2580
Width : 2.270
Height : 10.047
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

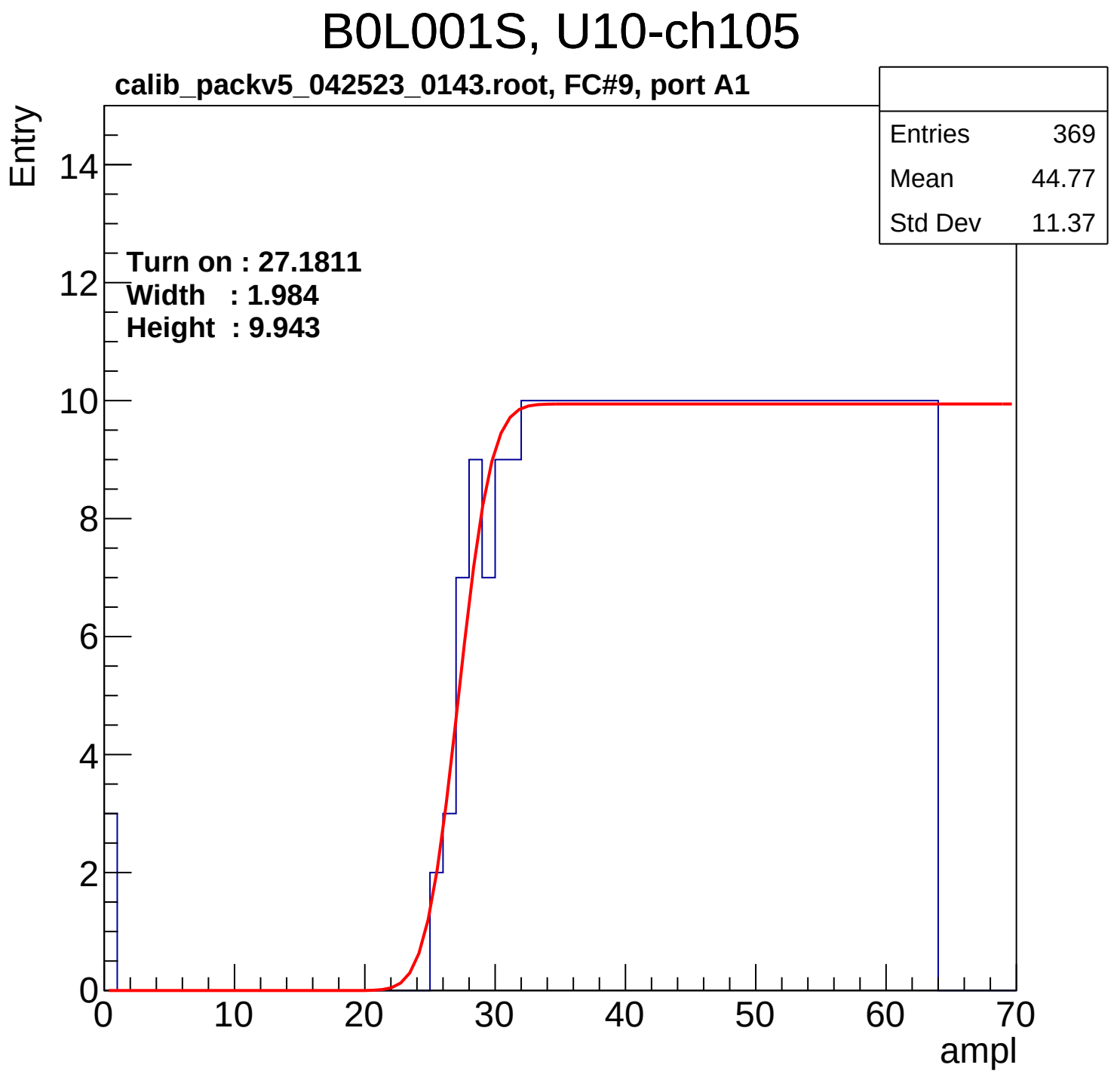

B0L001S, U10-ch100
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 44.94
Std Dev 11.33
Turn on : 28.5110
Width : 2.533
Height : 10.059
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

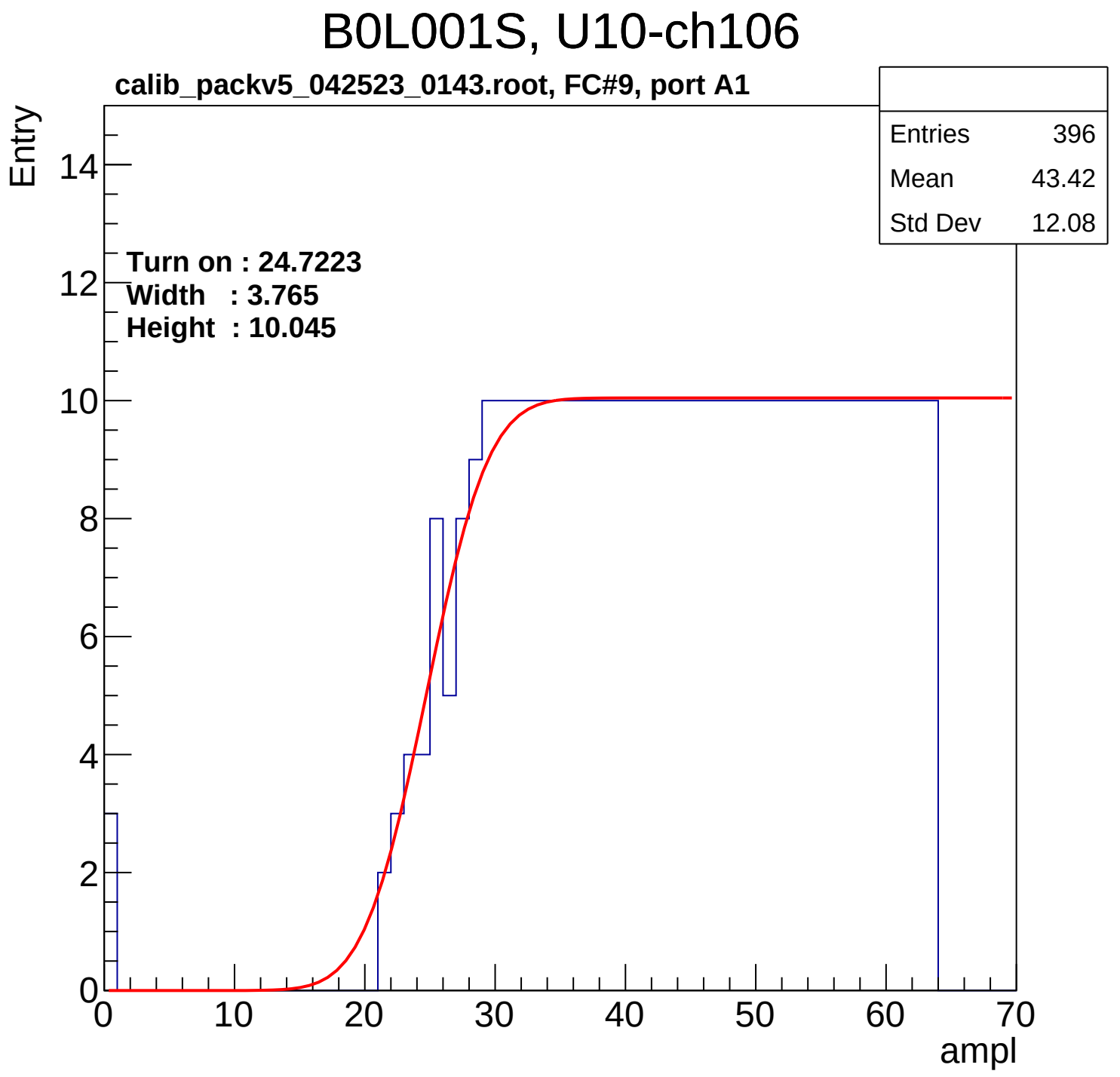

B0L001S, U10-ch101
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 45.1
Std Dev 11.14
Turn on : 28.5436
Width : 4.099
Height : 10.083
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

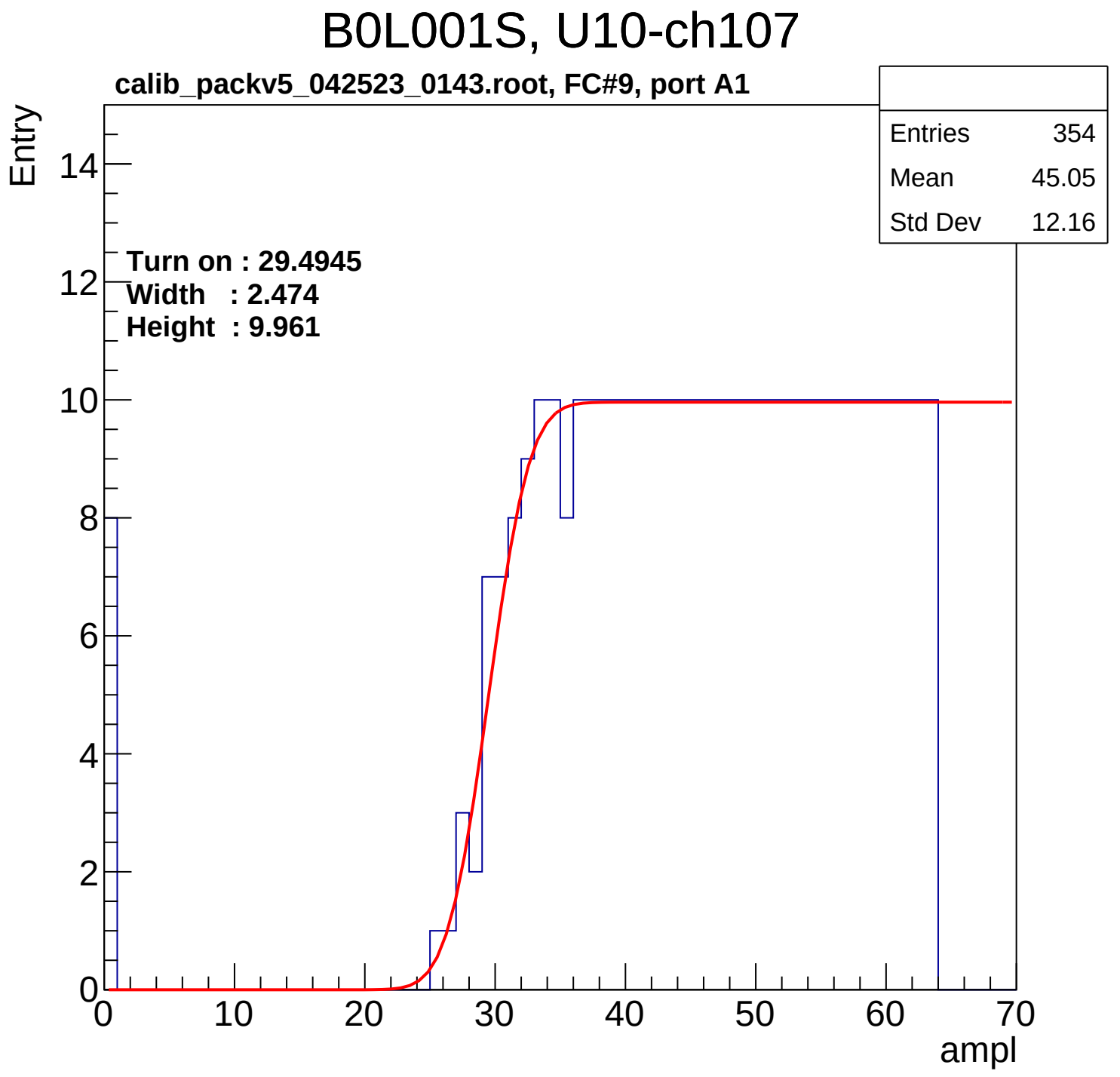

B0L001S, U10-ch102
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 45.17
Std Dev 10.87
Turn on : 28.3276
Width : 3.156
Height : 10.059
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

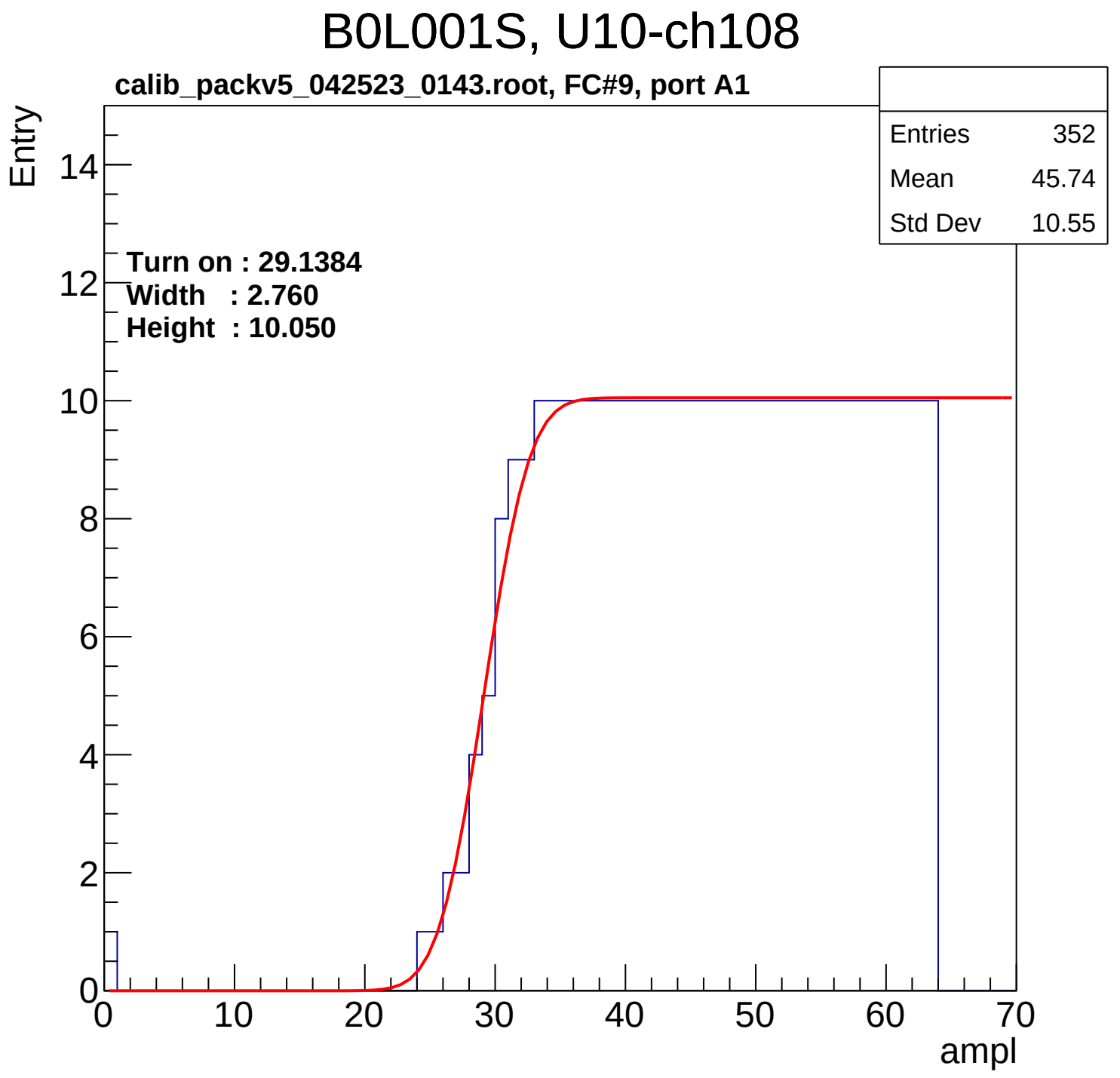

B0L001S, U10-ch103
calib_packv5_042523_0143.root, FC#9, port A1
Entries 347
Mean 45.71
Std Dev 11.07
Turn on : 30.3877
Width : 4.473
Height : 10.121
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

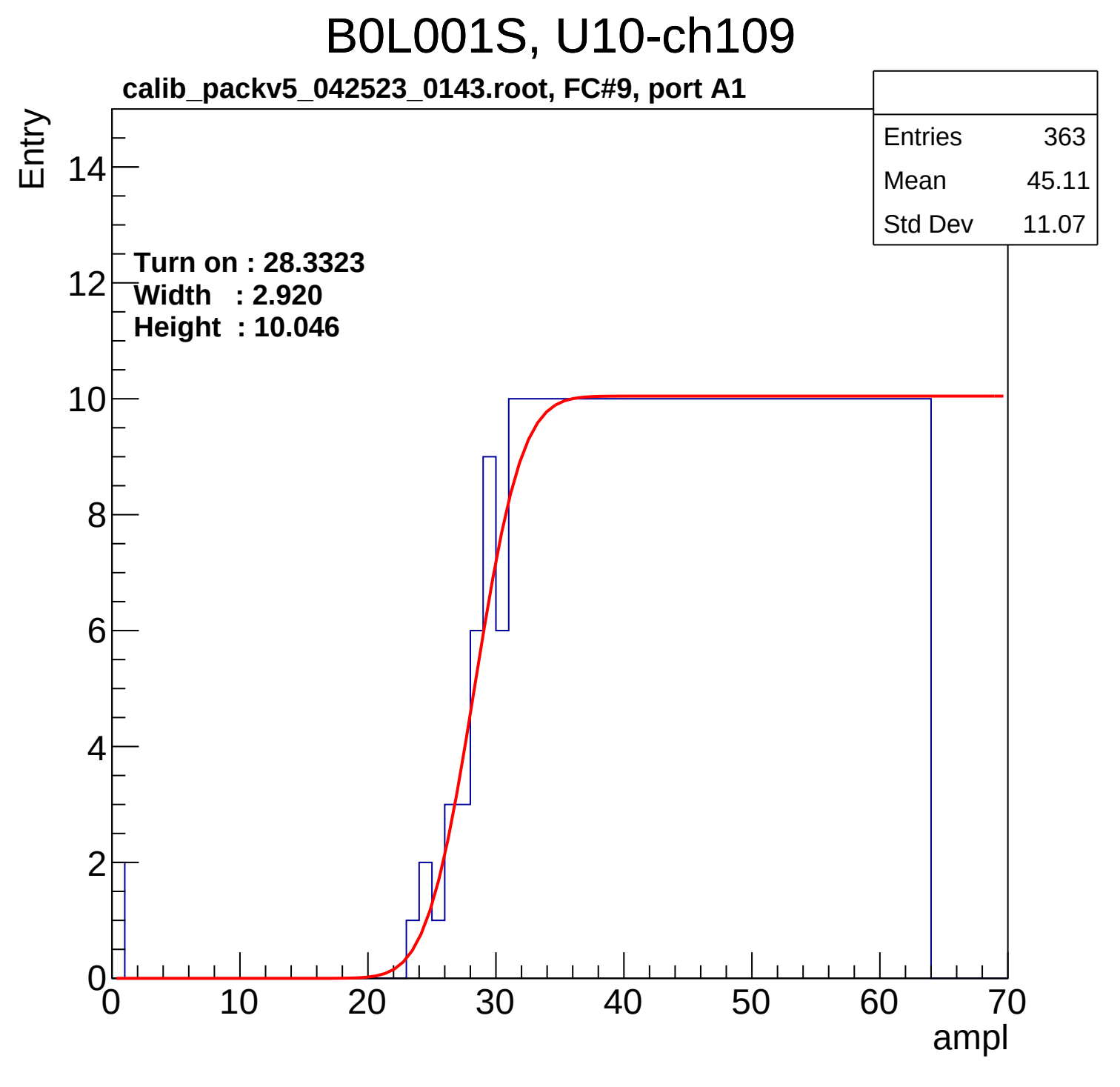

B0L001S, U10-ch104
calib_packv5_042523_0143.root, FC#9, port A1
Entries 382
Mean 44.13
Std Dev 11.62
Turn on : 25.8124
Width : 3.972
Height : 10.018
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

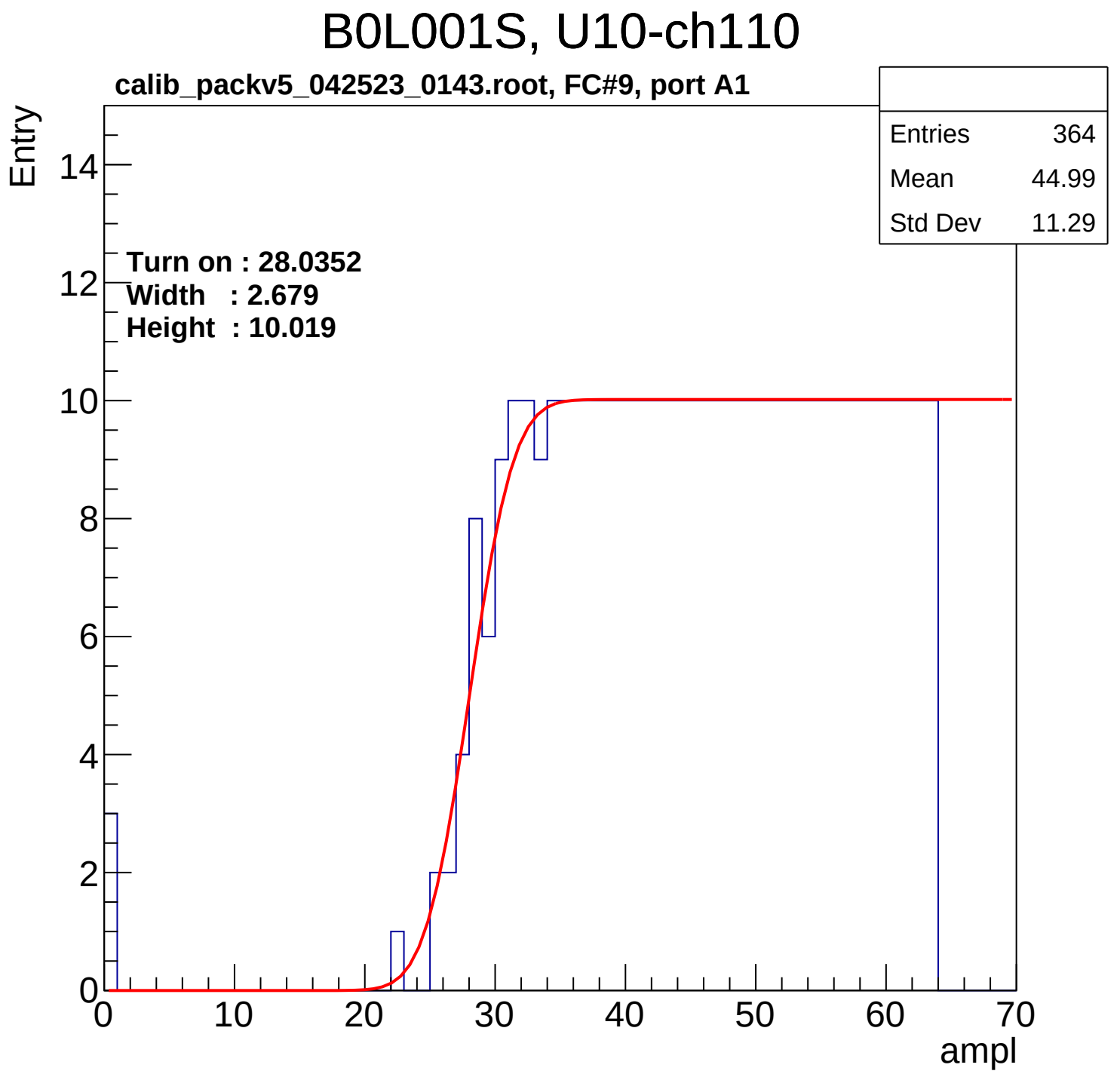

B0L001S, U10-ch105
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.77
Std Dev 11.37
Turn on : 27.1811
Width : 1.984
Height : 9.943
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

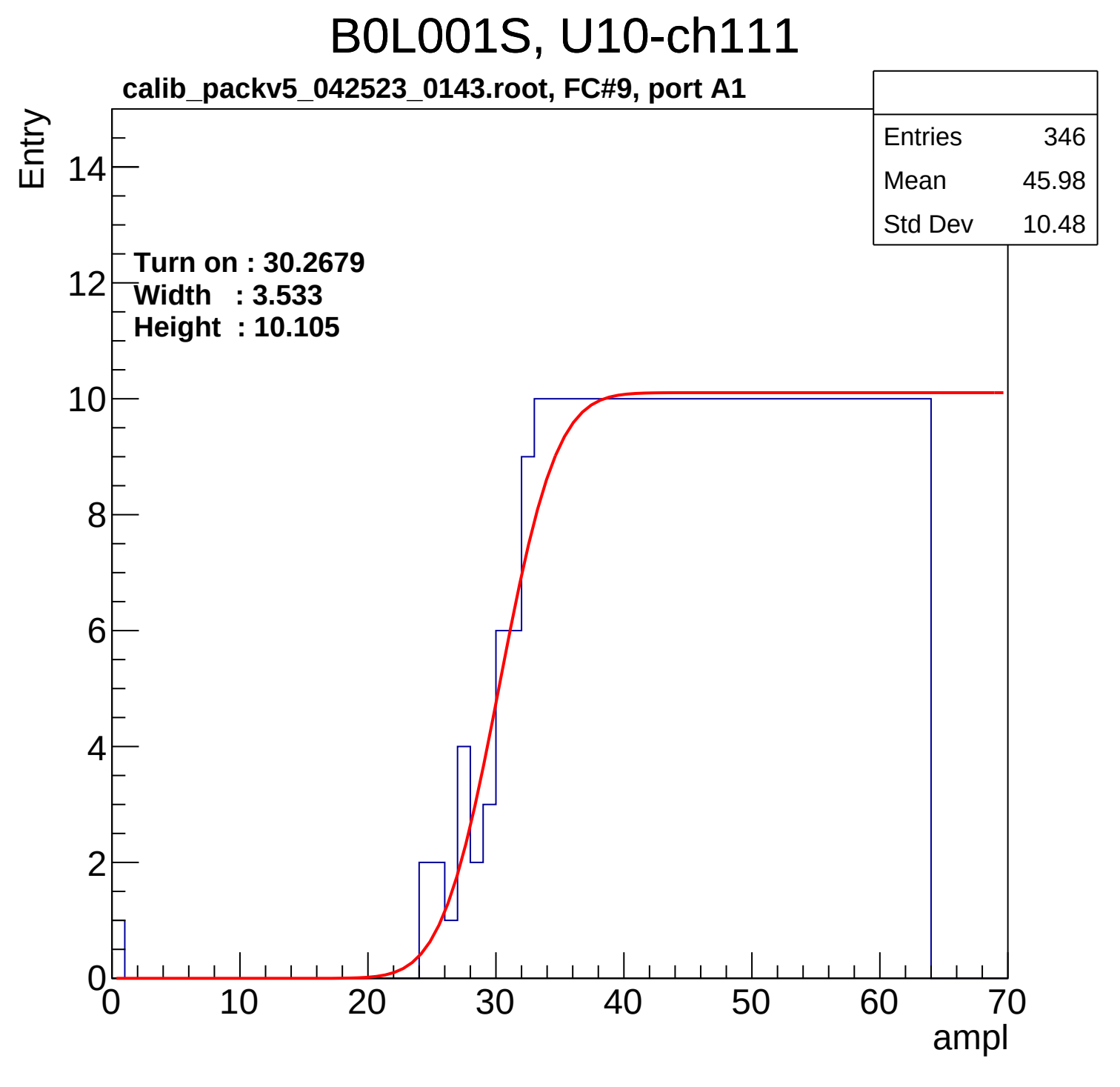

B0L001S, U10-ch106
calib_packv5_042523_0143.root, FC#9, port A1
Entries 396
Mean 43.42
Std Dev 12.08
Turn on : 24.7223
Width : 3.765
Height : 10.045
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

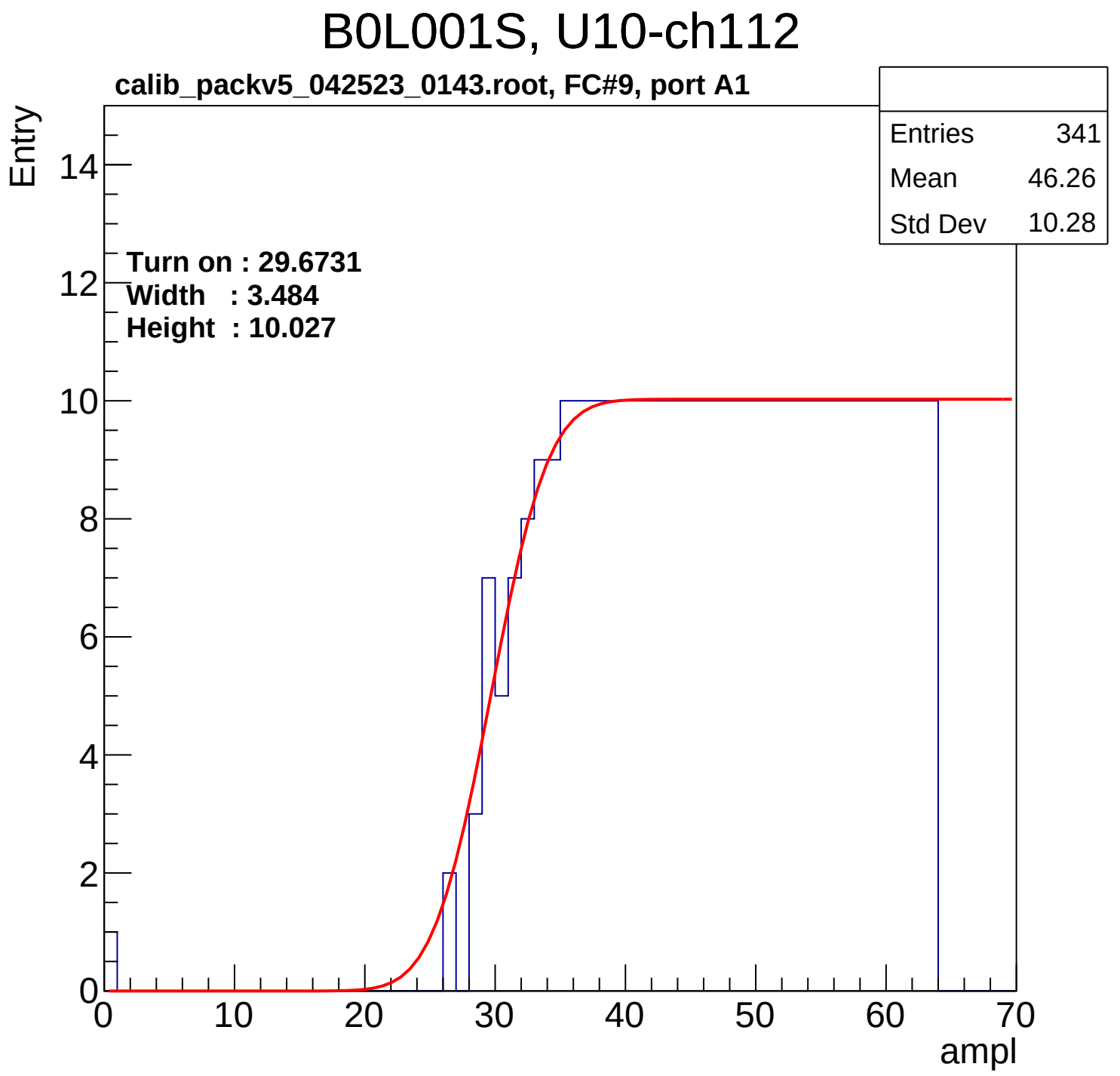

B0L001S, U10-ch107
calib_packv5_042523_0143.root, FC#9, port A1
Entries 354
Mean 45.05
Std Dev 12.16
Turn on : 29.4945
Width : 2.474
Height : 9.961
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

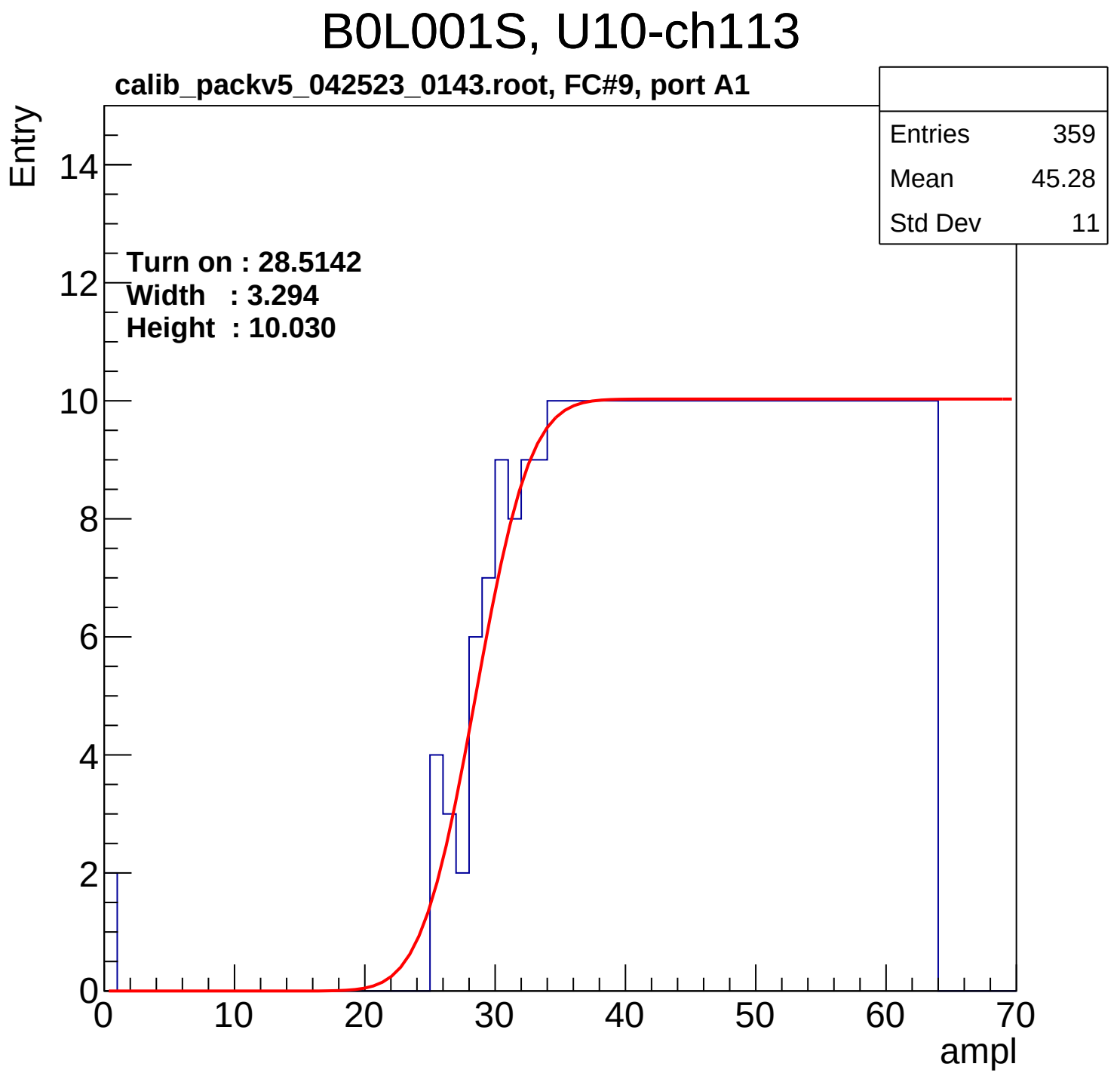

B0L001S, U10-ch108
calib_packv5_042523_0143.root, FC#9, port A1
Entries 352
Mean 45.74
Std Dev 10.55
Turn on : 29.1384
Width : 2.760
Height : 10.050
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

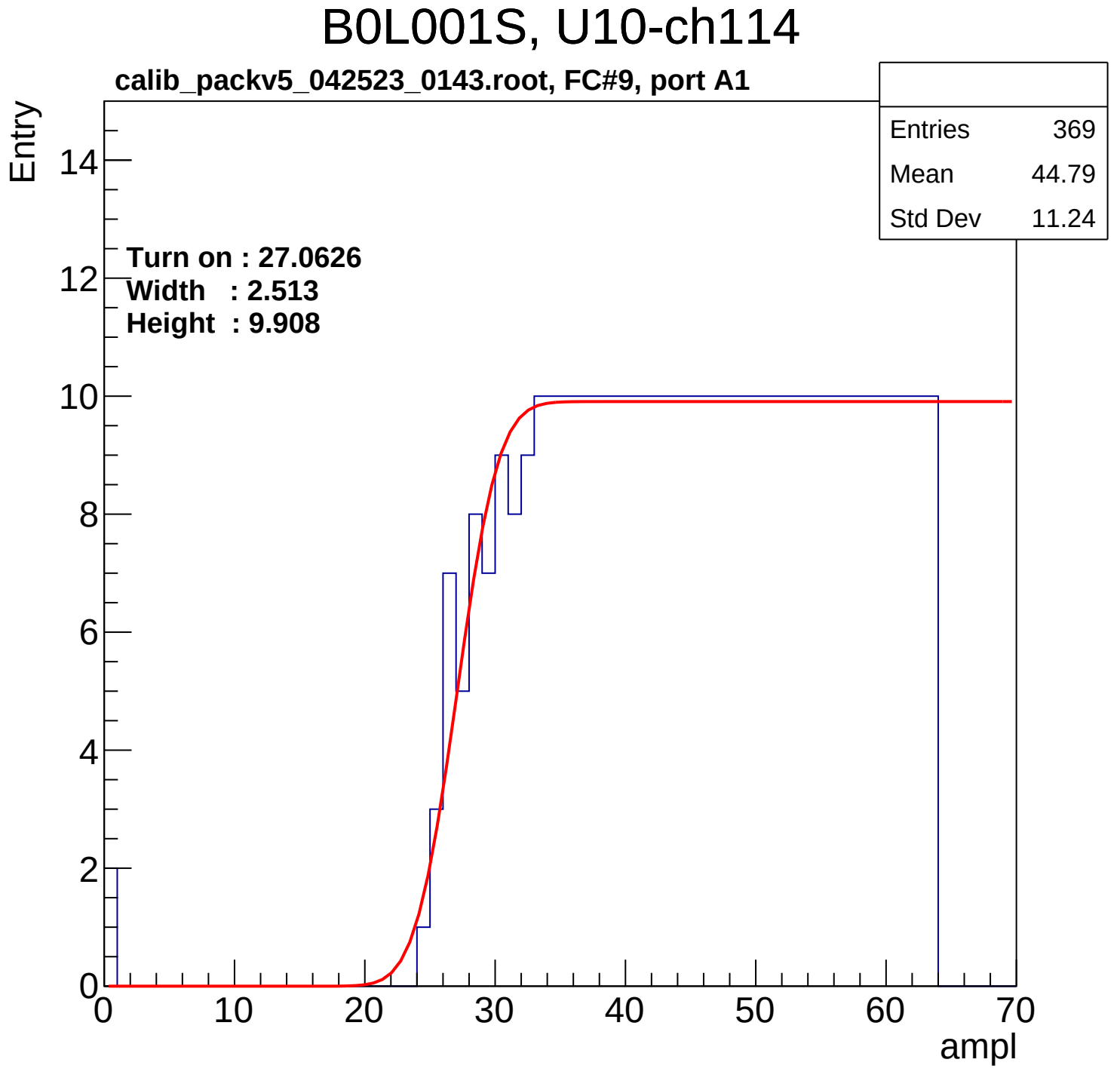

B0L001S, U10-ch109
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 45.11
Std Dev 11.07
Turn on : 28.3323
Width : 2.920
Height : 10.046
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

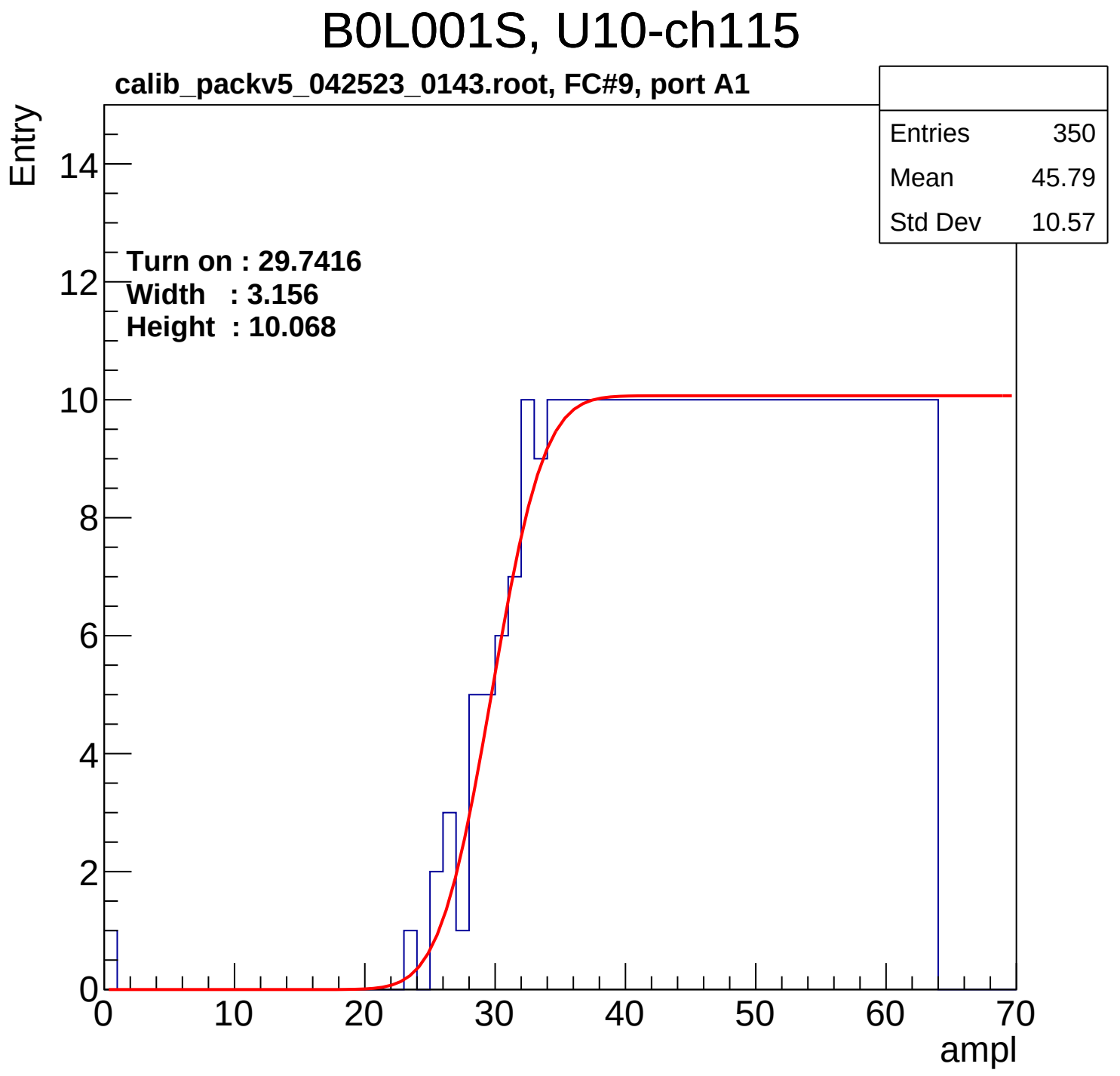

B0L001S, U10-ch110
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 44.99
Std Dev 11.29
Turn on : 28.0352
Width : 2.679
Height : 10.019
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

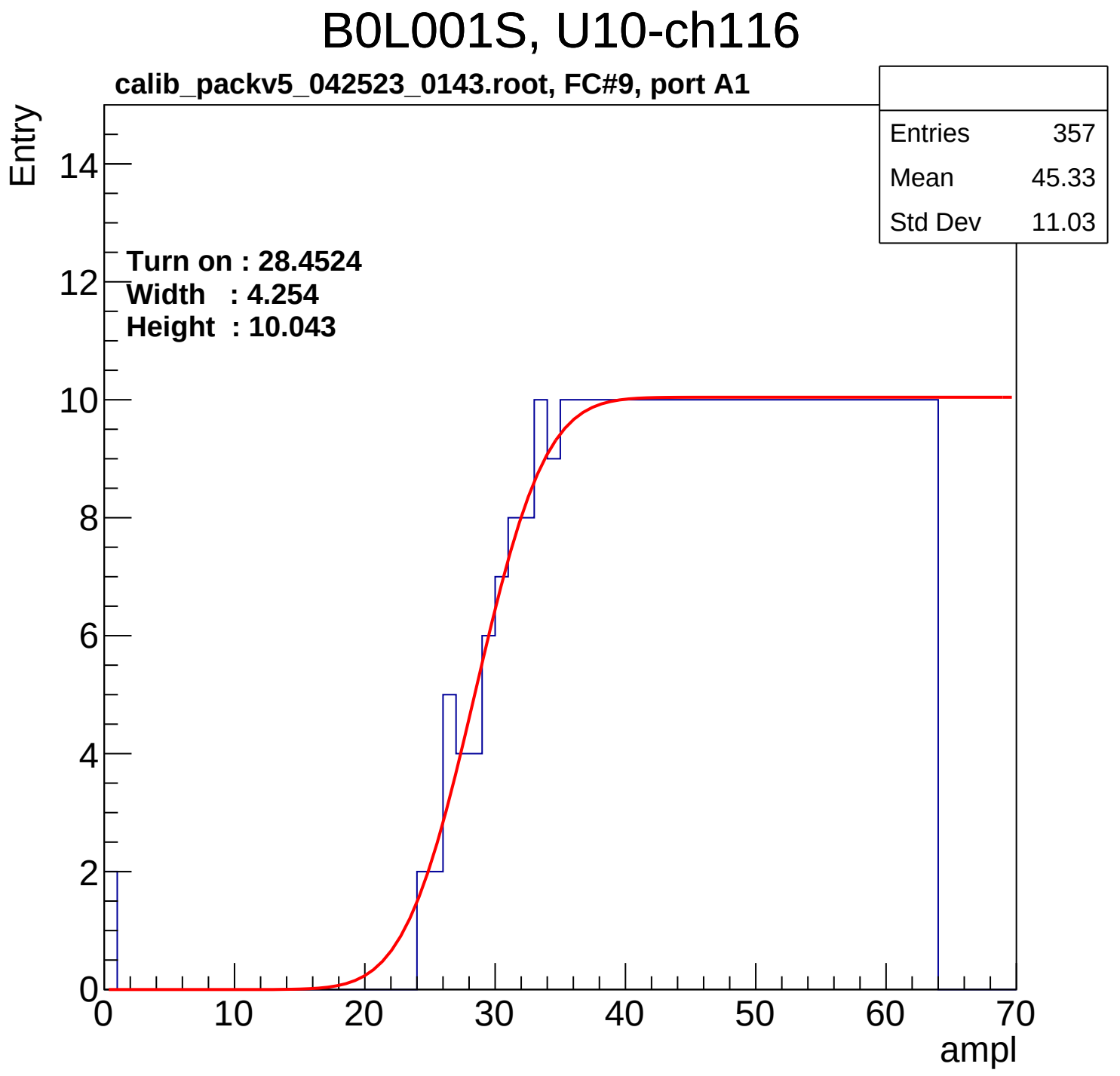

B0L001S, U10-ch111
calib_packv5_042523_0143.root, FC#9, port A1
Entries 346
Mean 45.98
Std Dev 10.48
Turn on : 30.2679
Width : 3.533
Height : 10.105
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

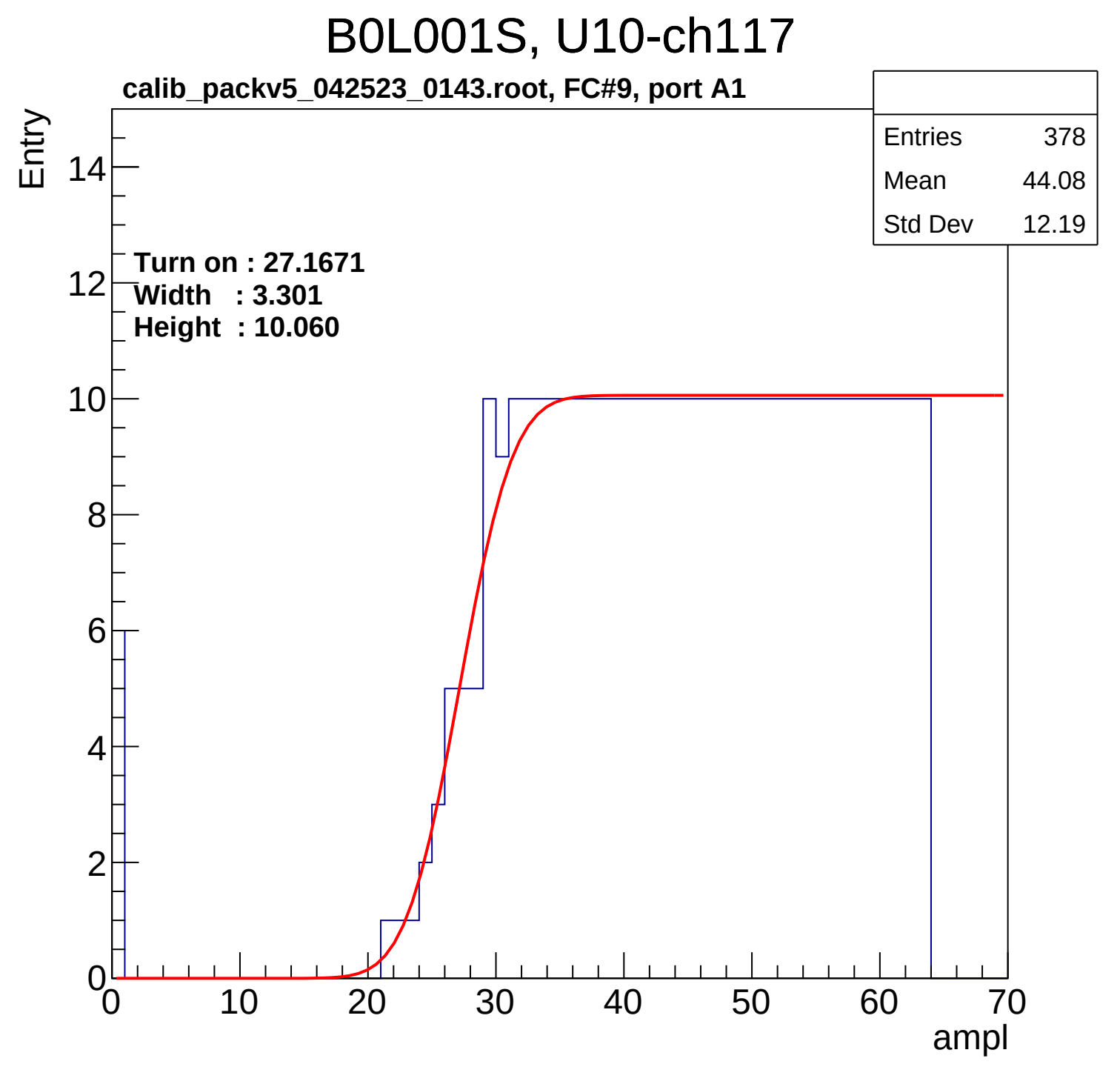

B0L001S, U10-ch112
calib_packv5_042523_0143.root, FC#9, port A1
Entries 341
Mean 46.26
Std Dev 10.28
Turn on : 29.6731
Width : 3.484
Height : 10.027
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

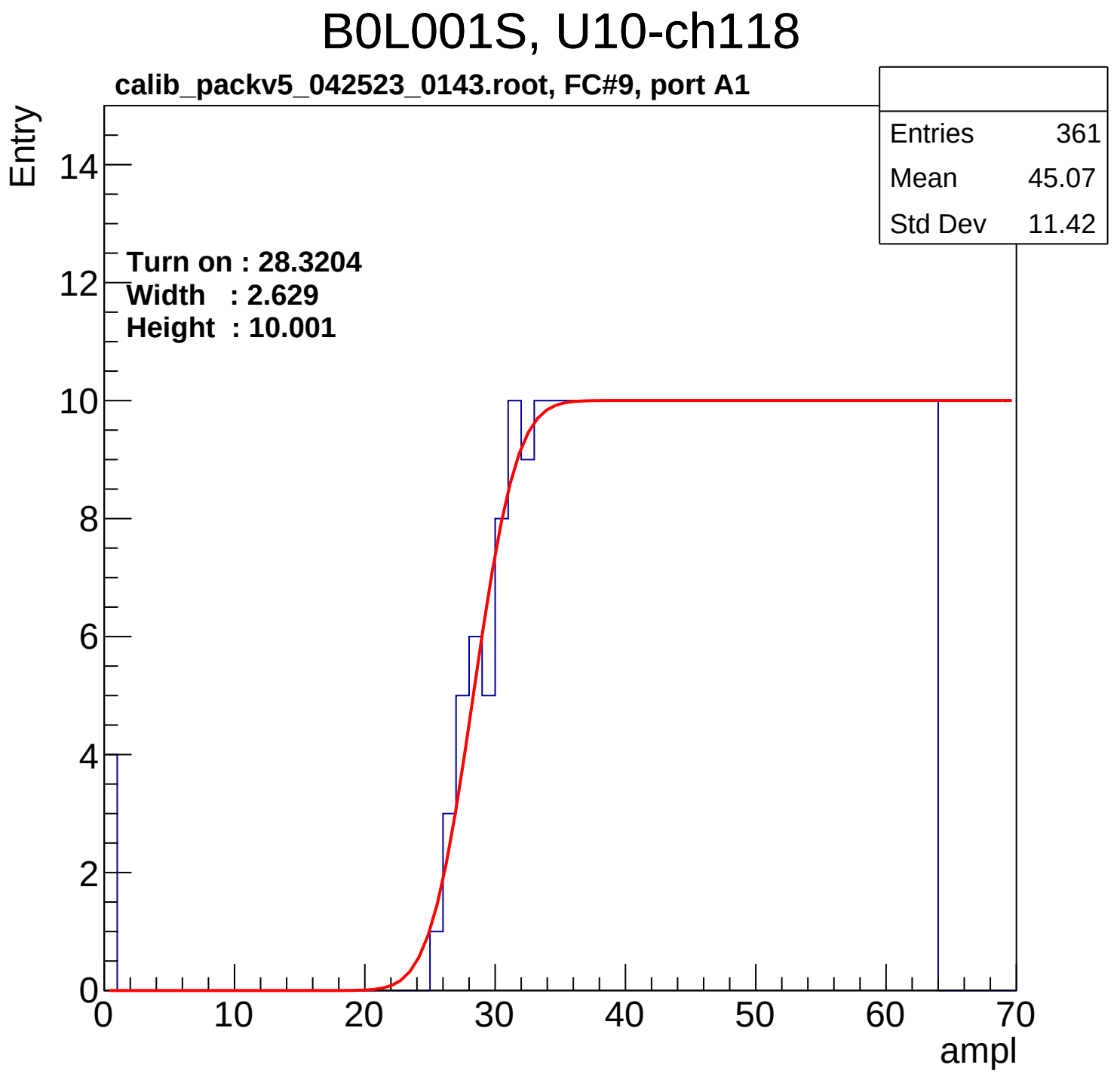

B0L001S, U10-ch113
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 45.28
Std Dev 11
Turn on : 28.5142
Width : 3.294
Height : 10.030
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

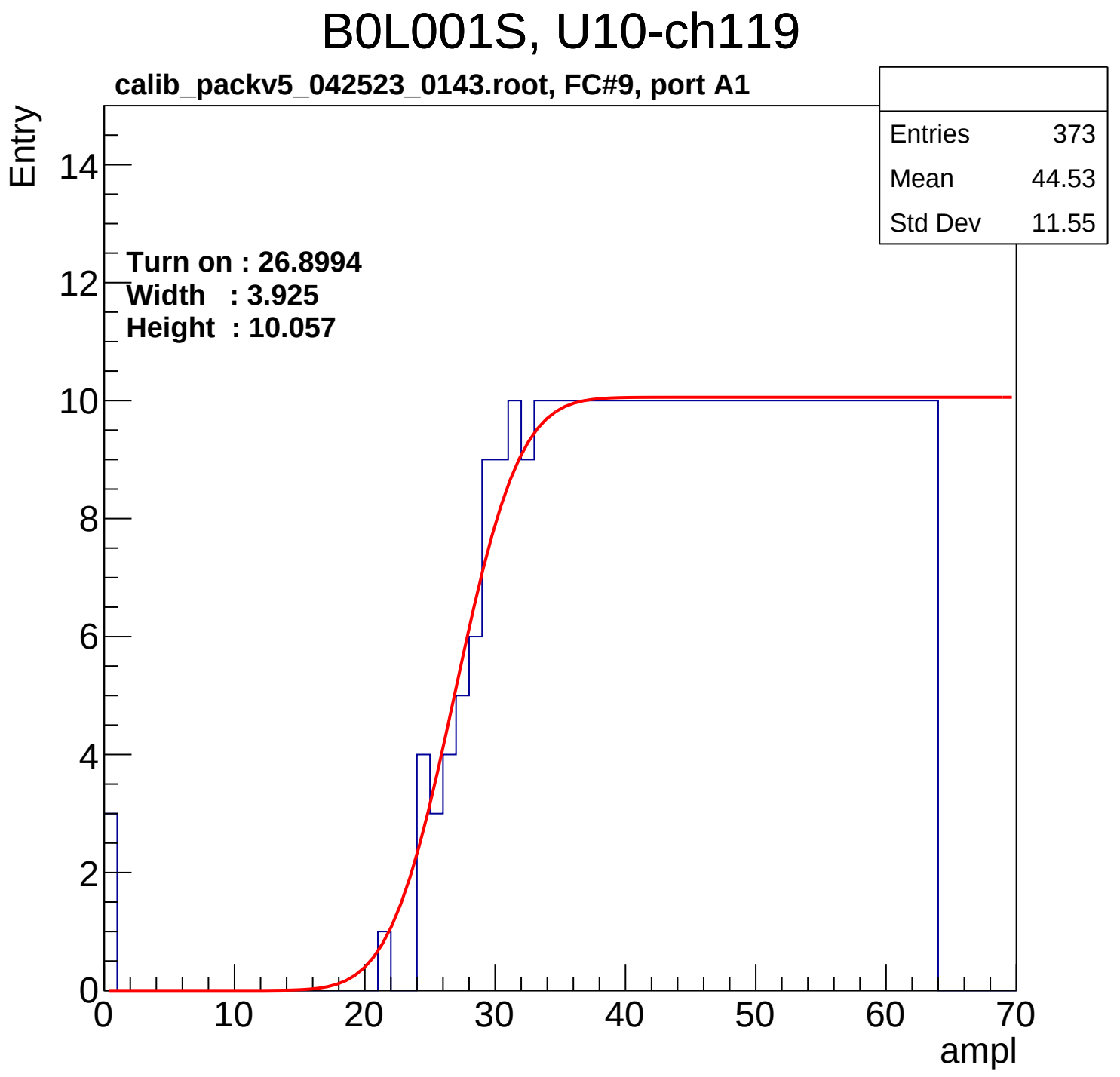

B0L001S, U10-ch114
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.79
Std Dev 11.24
Turn on : 27.0626
Width : 2.513
Height : 9.908
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

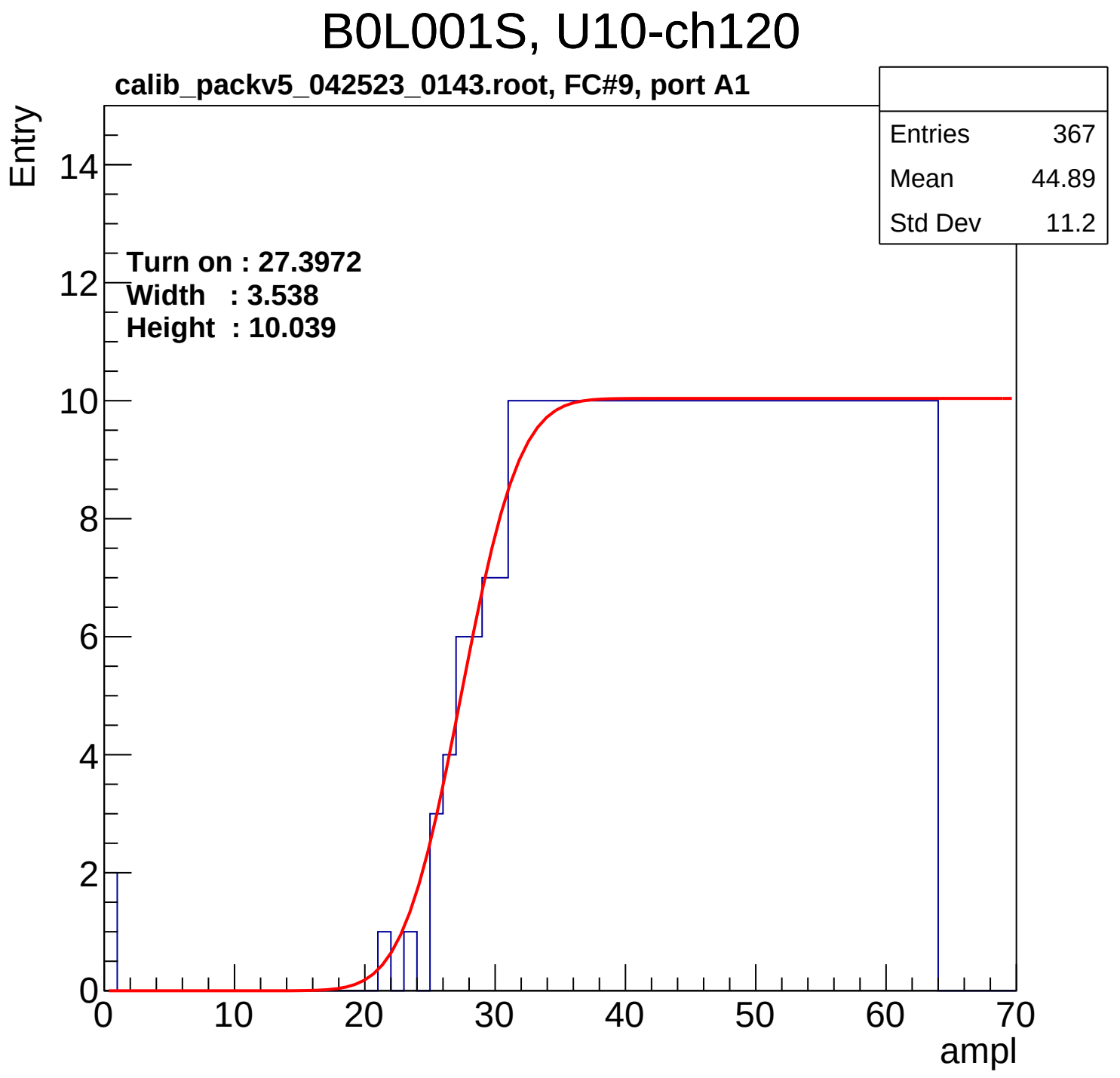

B0L001S, U10-ch115
calib_packv5_042523_0143.root, FC#9, port A1
Entries 350
Mean 45.79
Std Dev 10.57
Turn on : 29.7416
Width : 3.156
Height : 10.068
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

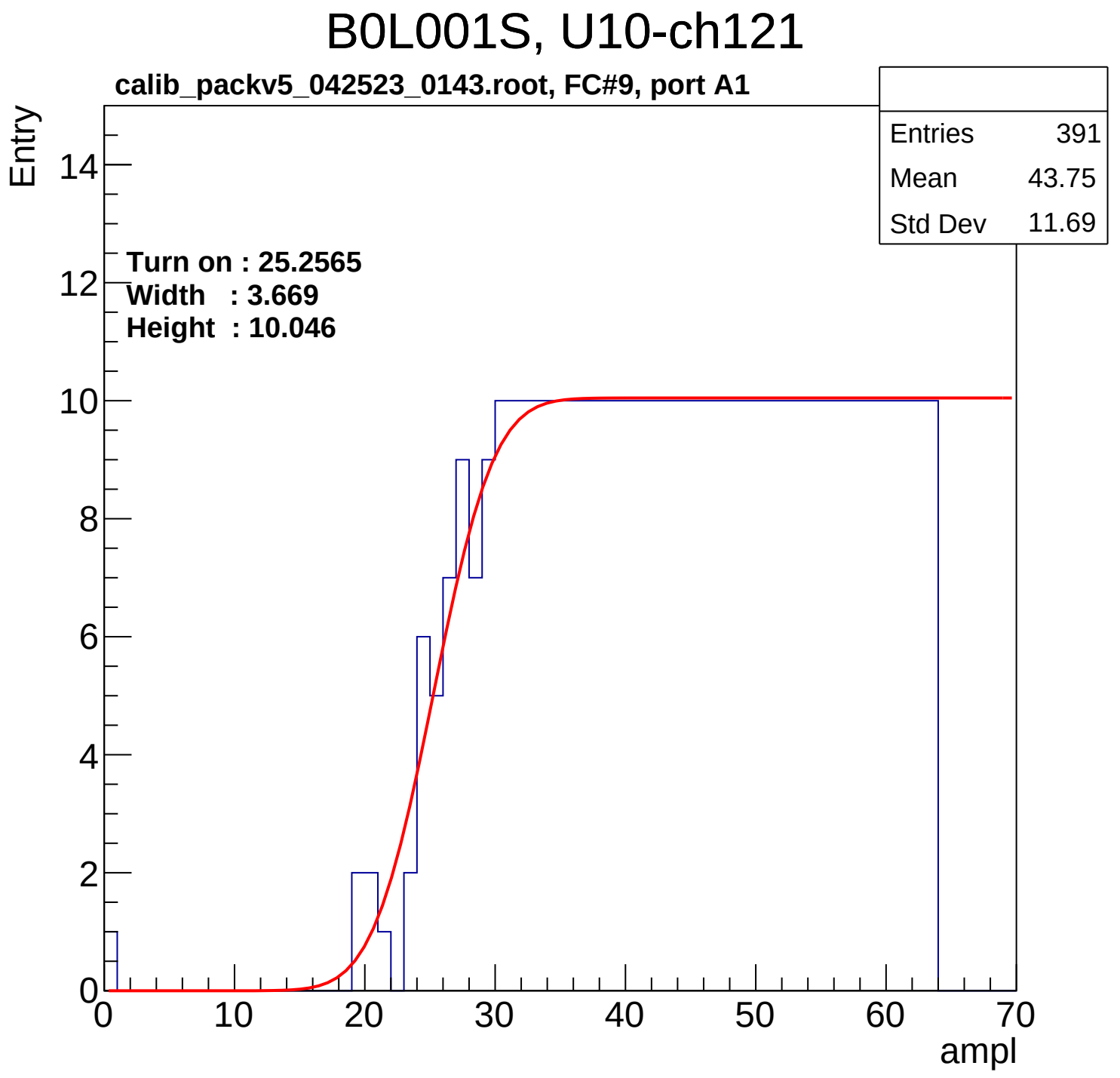

B0L001S, U10-ch116
calib_packv5_042523_0143.root, FC#9, port A1
Entries 357
Mean 45.33
Std Dev 11.03
Turn on : 28.4524
Width : 4.254
Height : 10.043
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

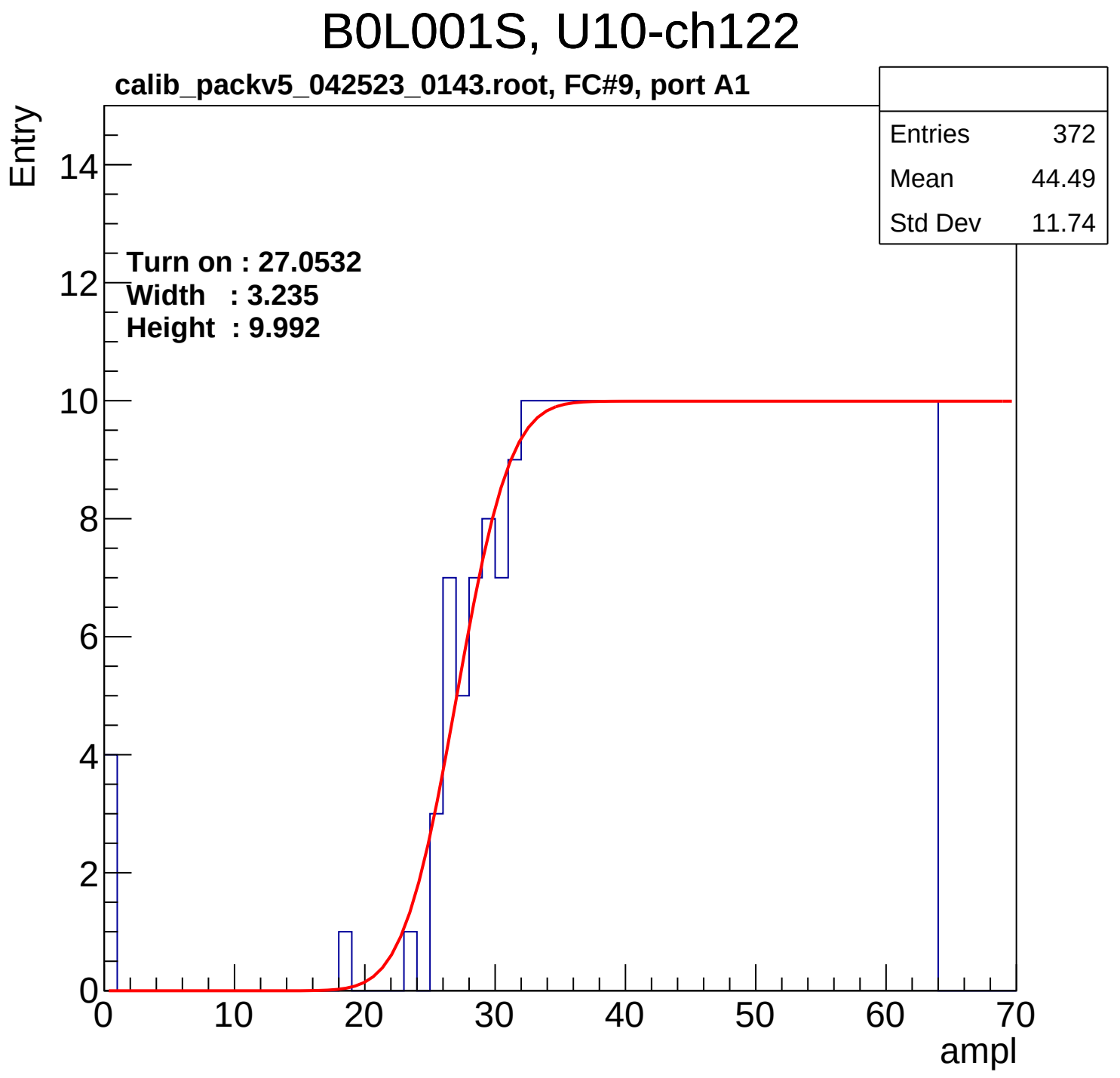

B0L001S, U10-ch117
calib_packv5_042523_0143.root, FC#9, port A1
Entries 378
Mean 44.08
Std Dev 12.19
Turn on : 27.1671
Width : 3.301
Height : 10.060
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

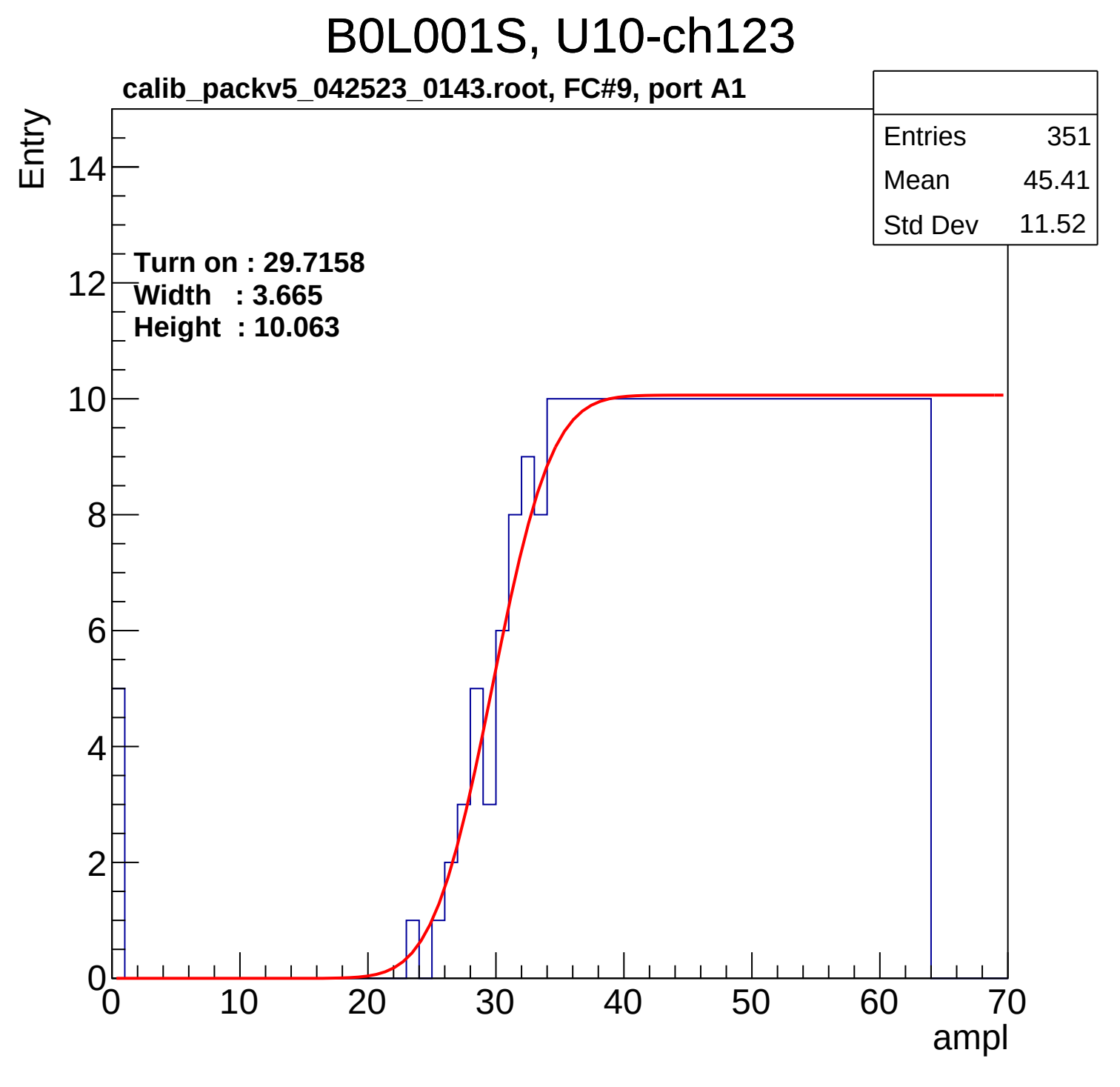

B0L001S, U10-ch118
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 45.07
Std Dev 11.42
Turn on : 28.3204
Width : 2.629
Height : 10.001
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

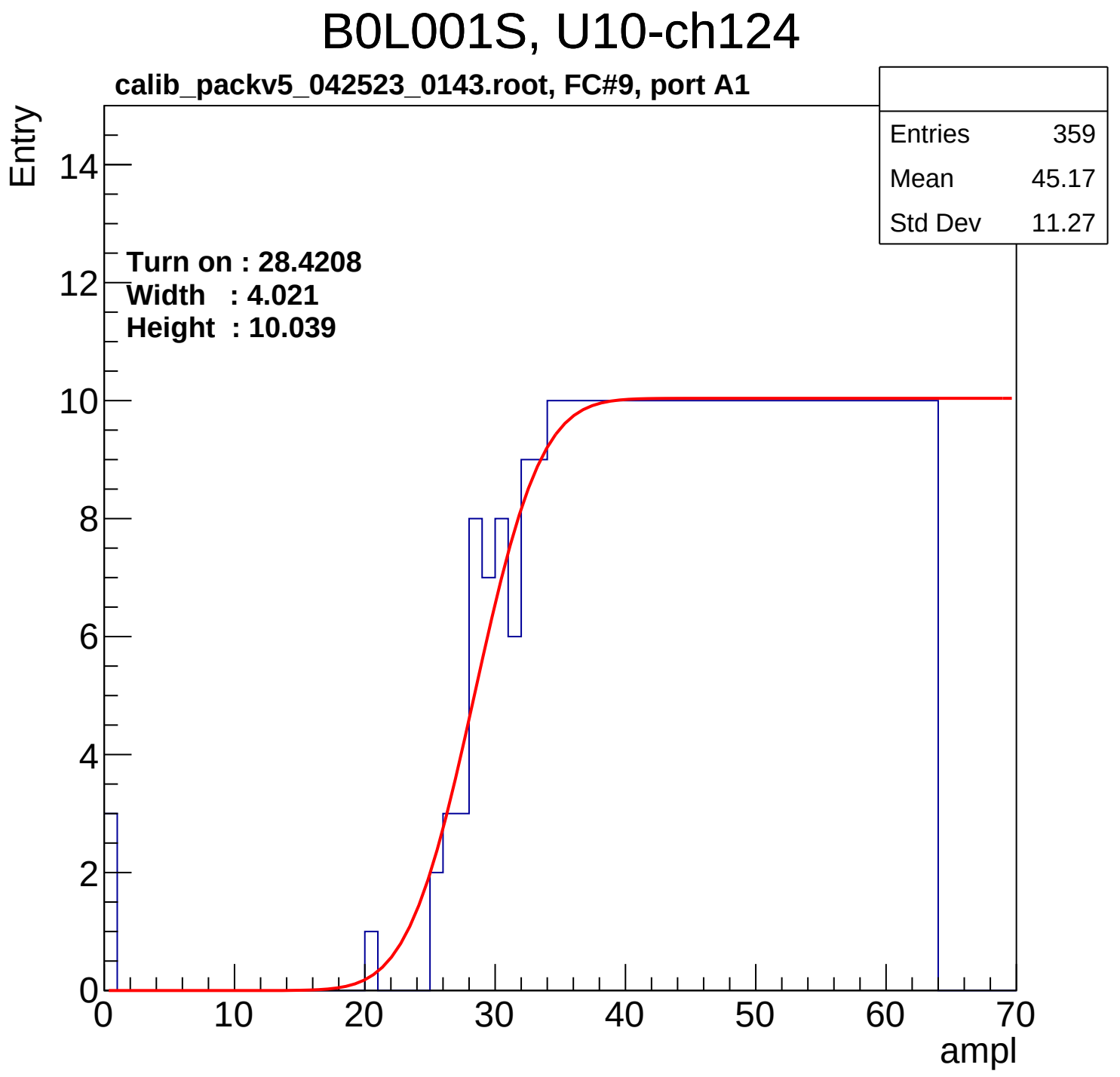

B0L001S, U10-ch119
calib_packv5_042523_0143.root, FC#9, port A1
Entries 373
Mean 44.53
Std Dev 11.55
Turn on : 26.8994
Width : 3.925
Height : 10.057
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

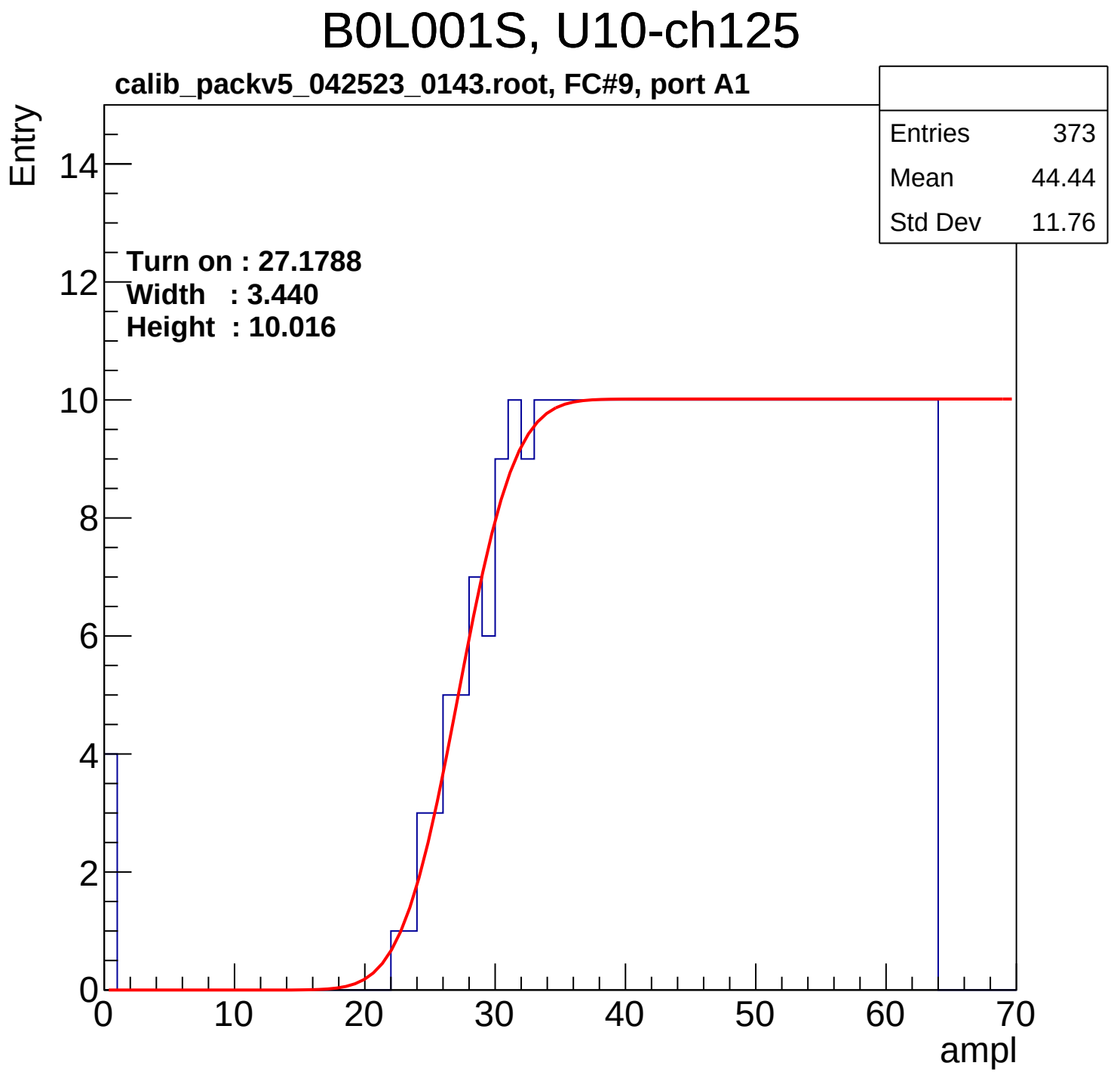

B0L001S, U10-ch120
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.89
Std Dev 11.2
Turn on : 27.3972
Width : 3.538
Height : 10.039
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

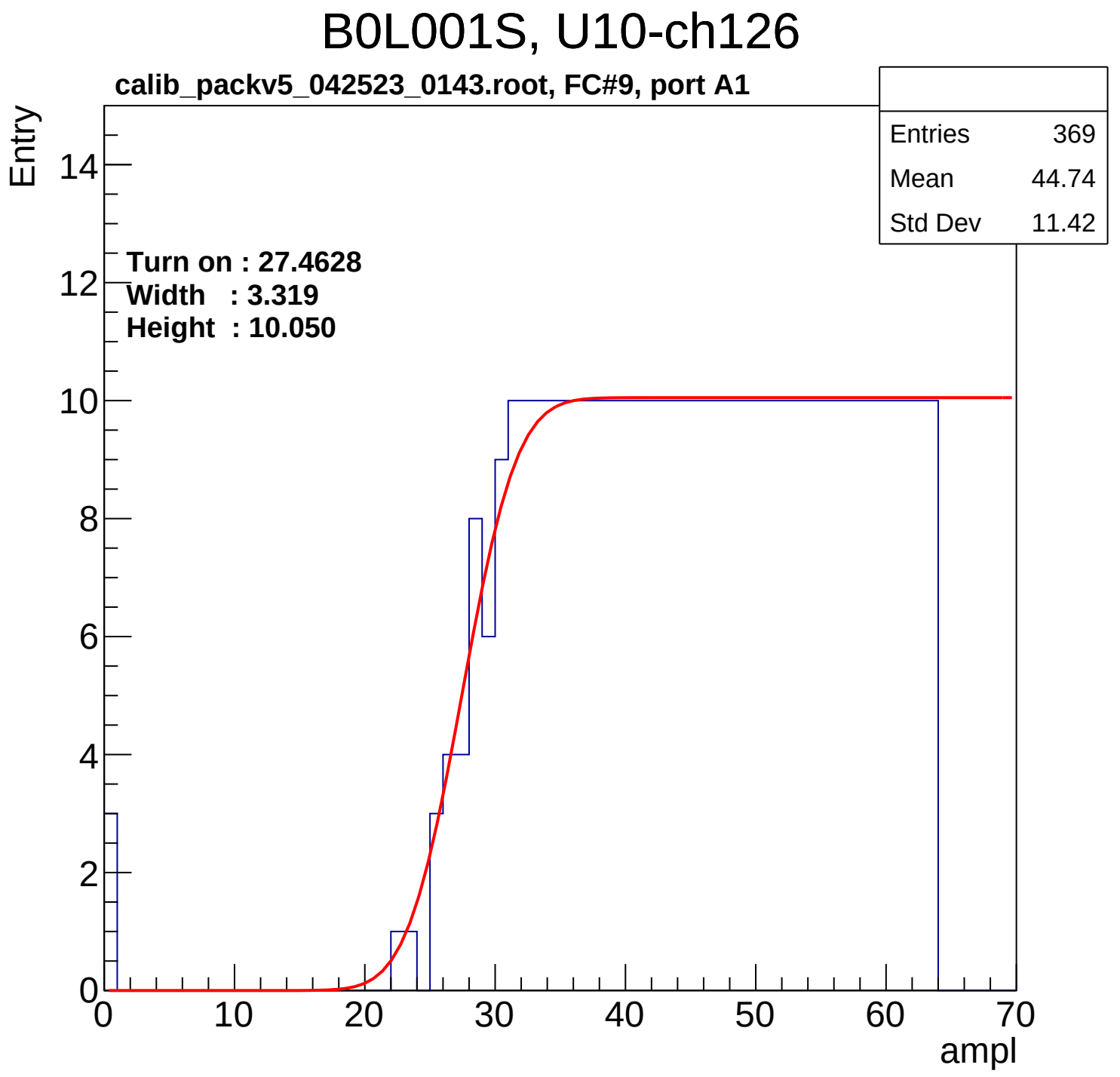

B0L001S, U10-ch121
calib_packv5_042523_0143.root, FC#9, port A1
Entries 391
Mean 43.75
Std Dev 11.69
Turn on : 25.2565
Width : 3.669
Height : 10.046
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

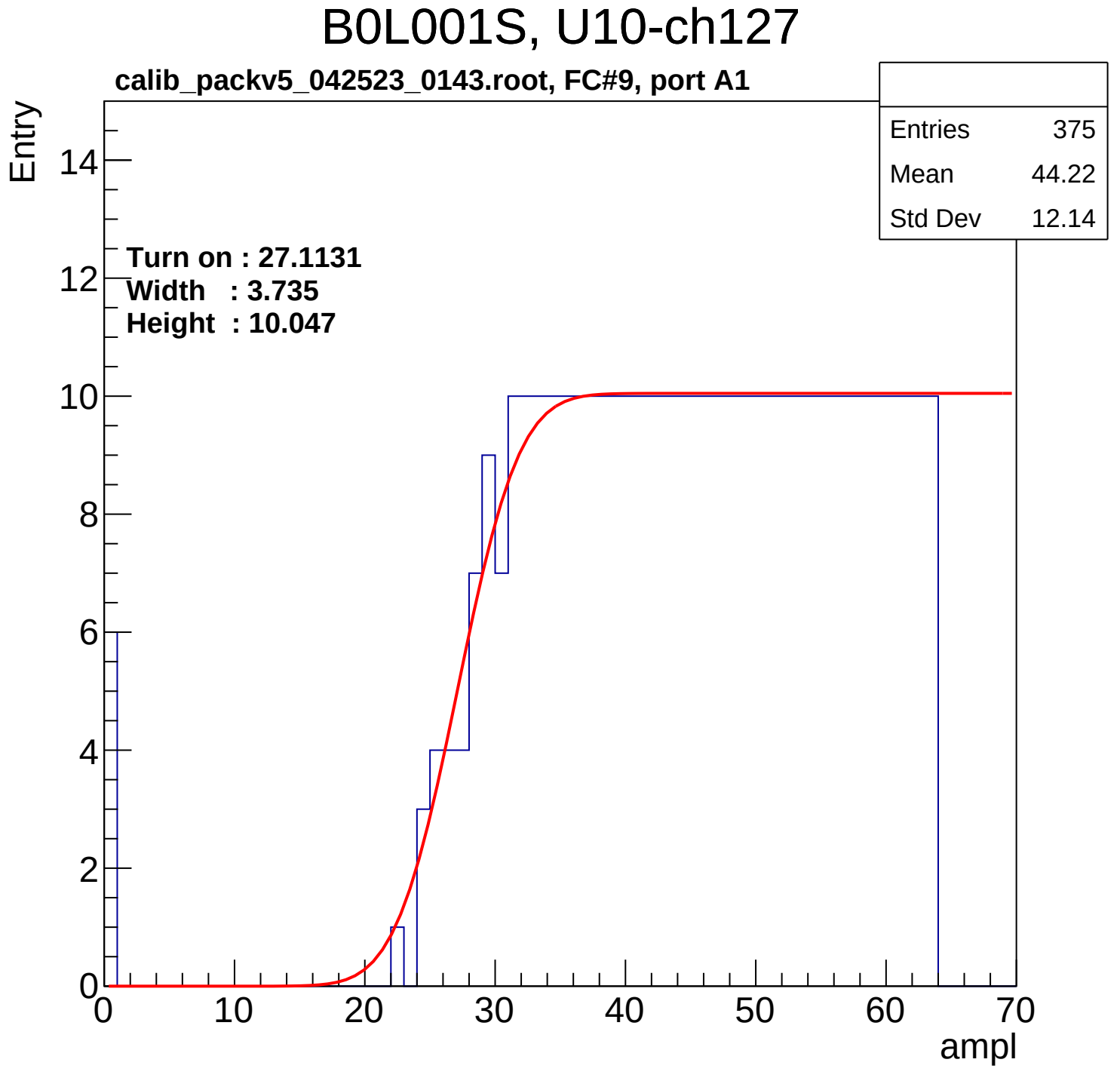

B0L001S, U10-ch122
calib_packv5_042523_0143.root, FC#9, port A1
Entries 372
Mean 44.49
Std Dev 11.74
Turn on : 27.0532
Width : 3.235
Height : 9.992
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

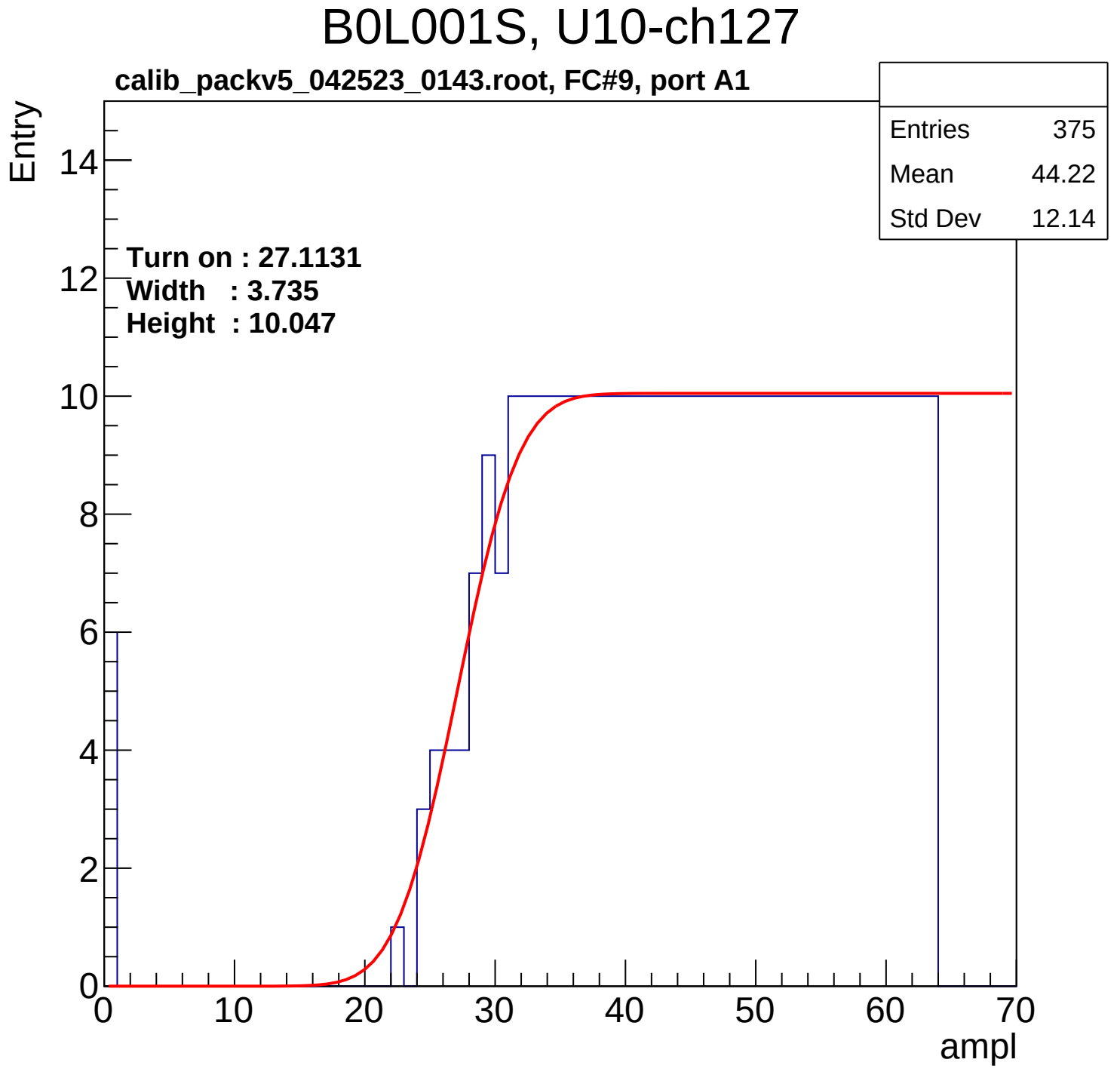

B0L001S, U10-ch123
calib_packv5_042523_0143.root, FC#9, port A1
Entries 351
Mean 45.41
Std Dev 11.52
Turn on : 29.7158
Width : 3.665
Height : 10.063
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U10-ch124
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 45.17
Std Dev 11.27
Turn on : 28.4208
Width : 4.021
Height : 10.039
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U10-ch125
calib_packv5_042523_0143.root, FC#9, port A1
Entries 373
Mean 44.44
Std Dev 11.76
Turn on : 27.1788
Width : 3.440
Height : 10.016
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U10-ch126
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.74
Std Dev 11.42
Turn on : 27.4628
Width : 3.319
Height : 10.050
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U10-ch127
calib_packv5_042523_0143.root, FC#9, port A1
Entries 375
Mean 44.22
Std Dev 12.14
Turn on : 27.1131
Width : 3.735
Height : 10.047
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U10-ch127
calib_packv5_042523_0143.root, FC#9, port A1
Entries 375
Mean 44.22
Std Dev 12.14
Turn on : 27.1131
Width : 3.735
Height : 10.047
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70