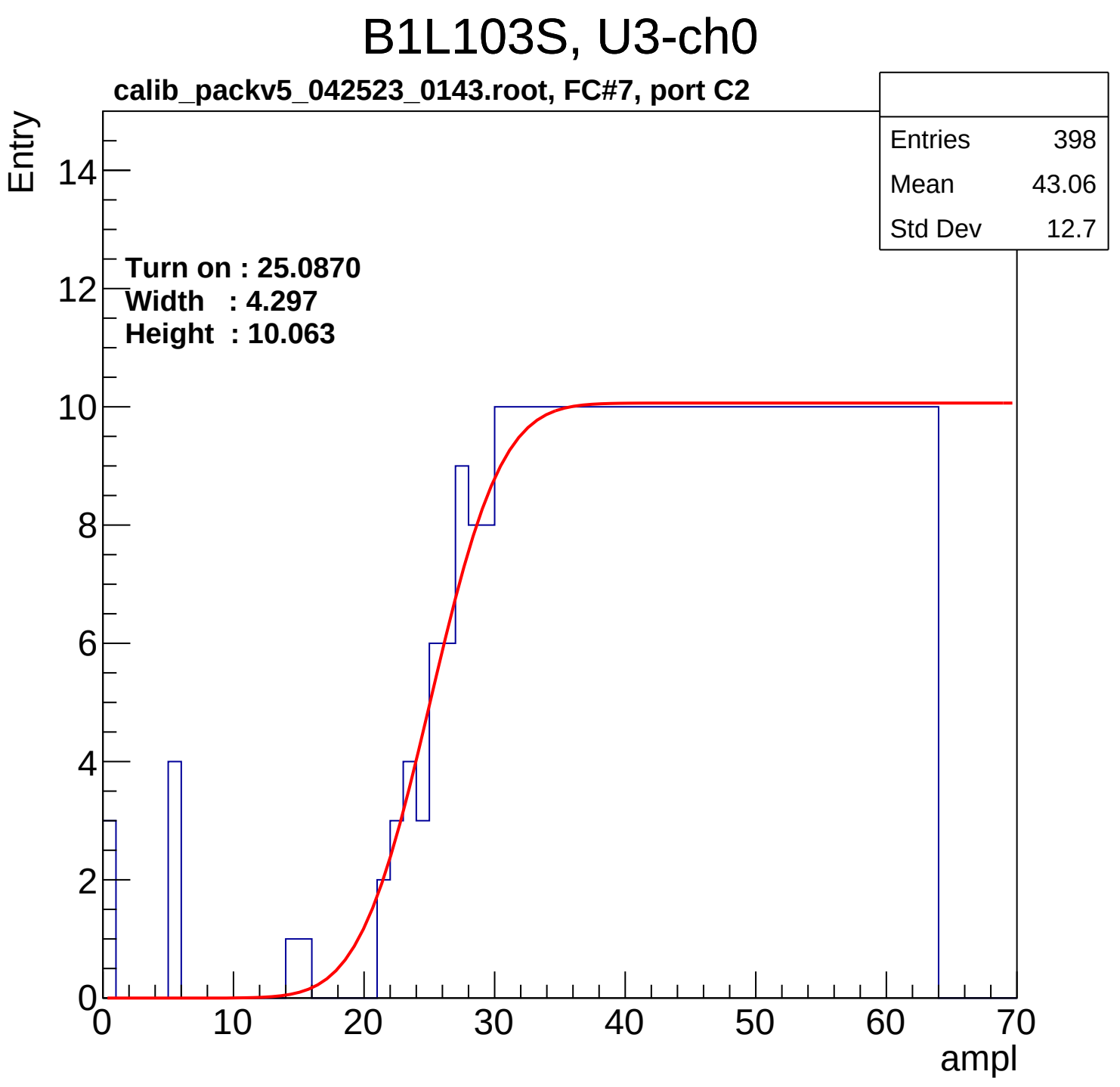
B1L103S, U3-ch0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 398
Mean 43.06
Std Dev 12.7
Turn on : 25.0870
Width : 4.297
Height : 10.063
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ampl
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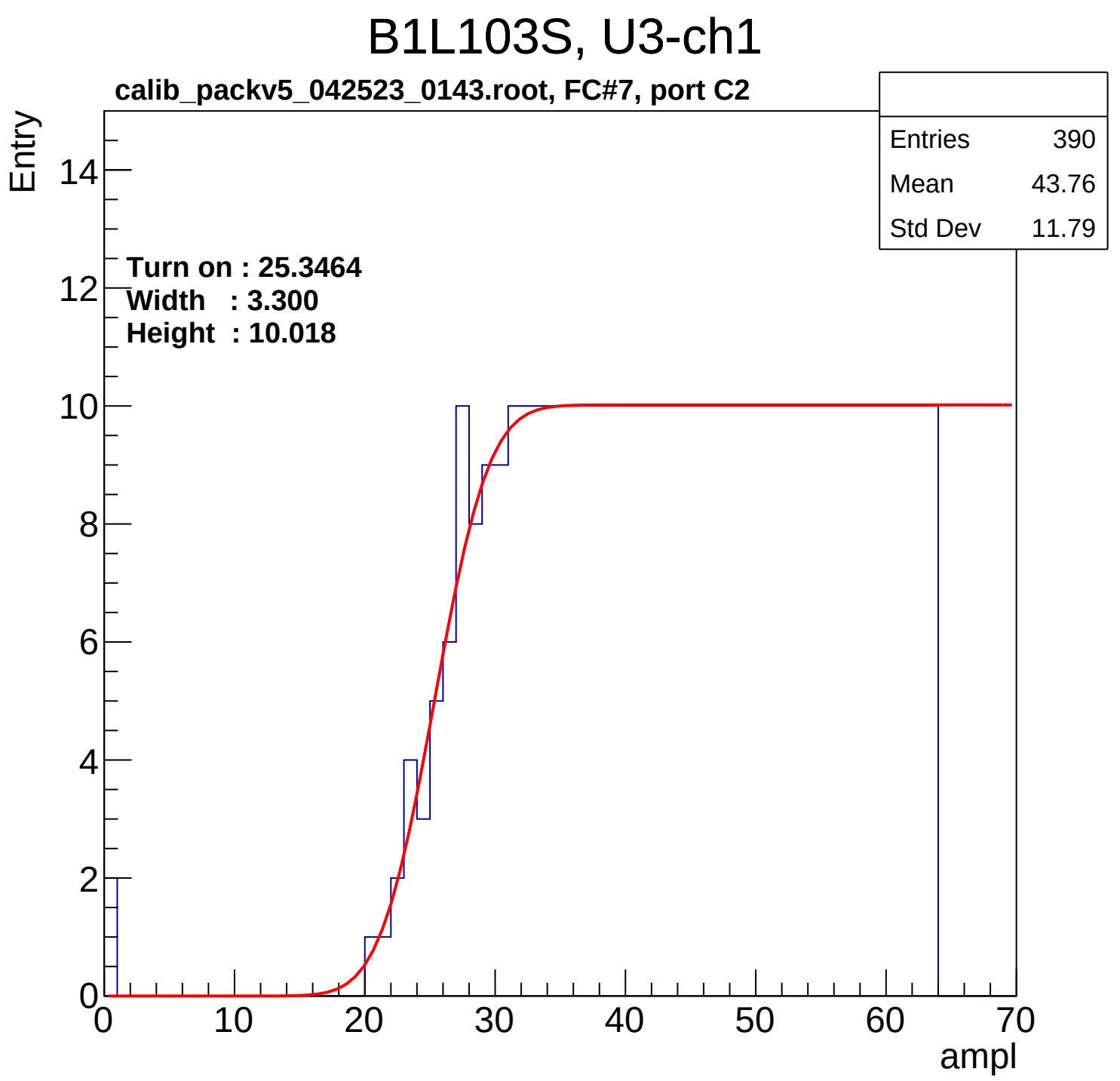
B1L103S, U3-ch1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 390
Mean 43.76
Std Dev 11.79
Turn on : 25.3464
Width : 3.300
Height : 10.018
Entry
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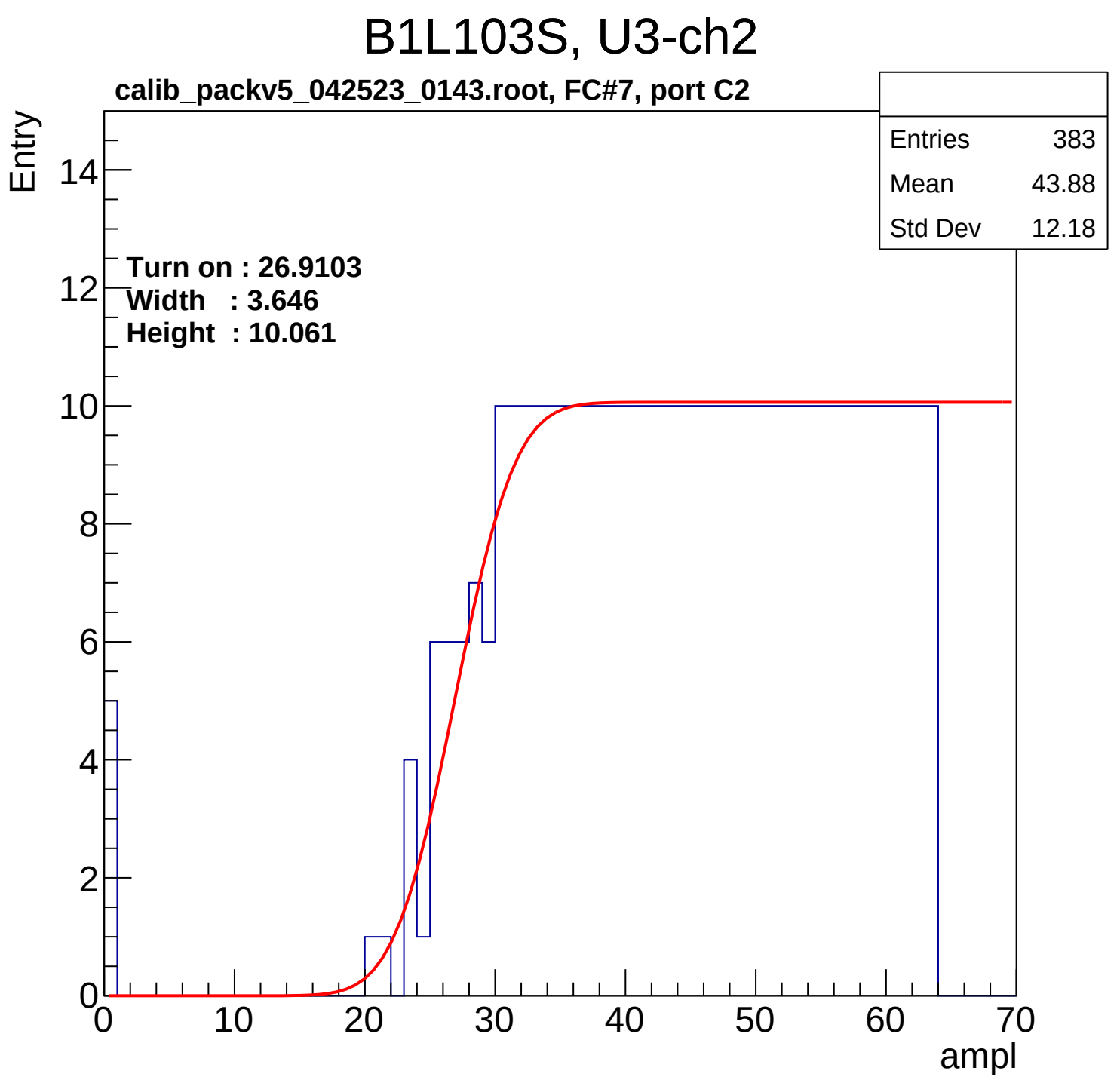
B1L103S, U3-ch2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 383
Mean 43.88
Std Dev 12.18
Turn on : 26.9103
Width : 3.646
Height : 10.061
Entry
ampl
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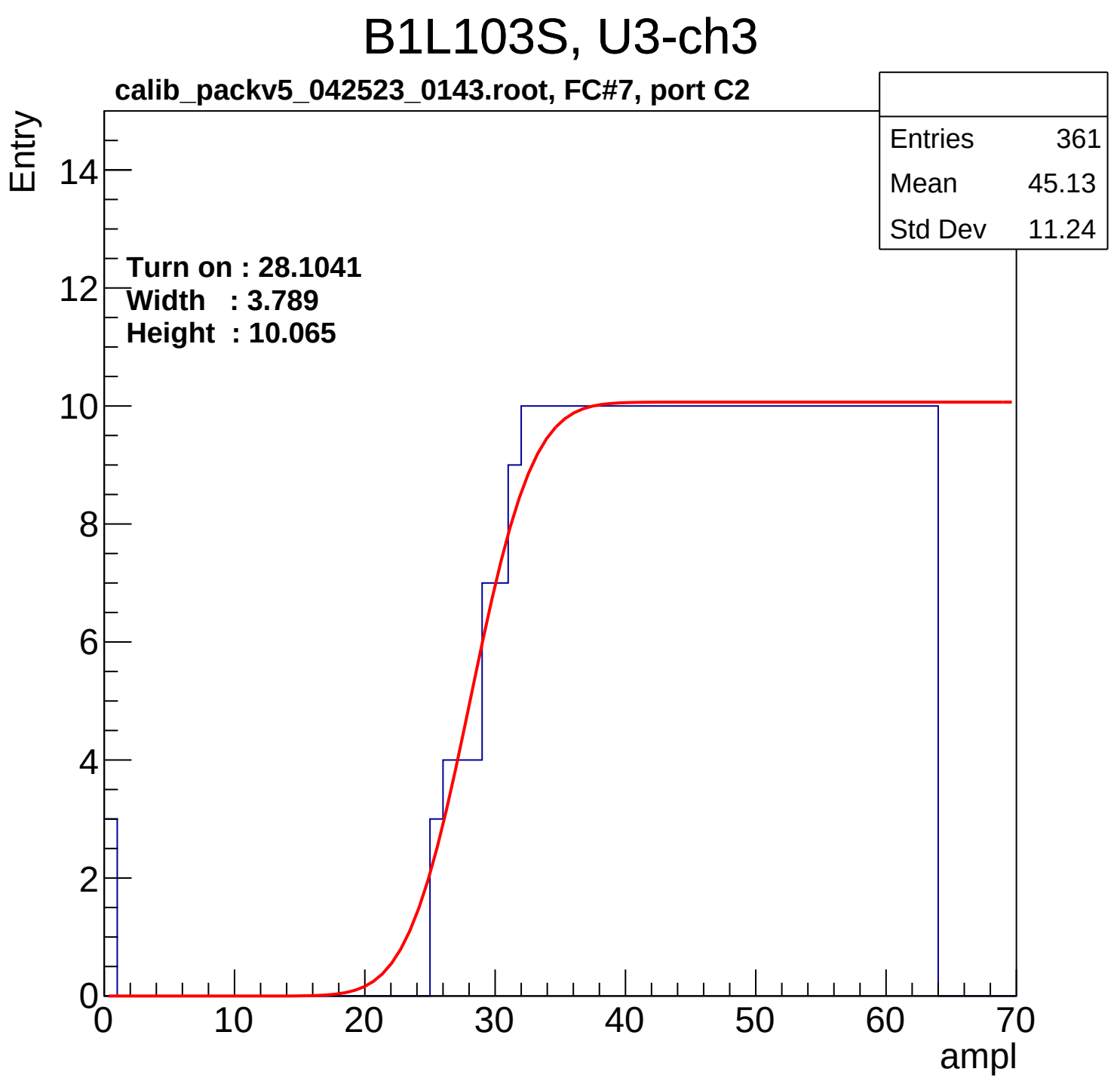
B1L103S, U3-ch3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 361
Mean 45.13
Std Dev 11.24
Turn on : 28.1041
Width : 3.789
Height : 10.065
Entry
ampl
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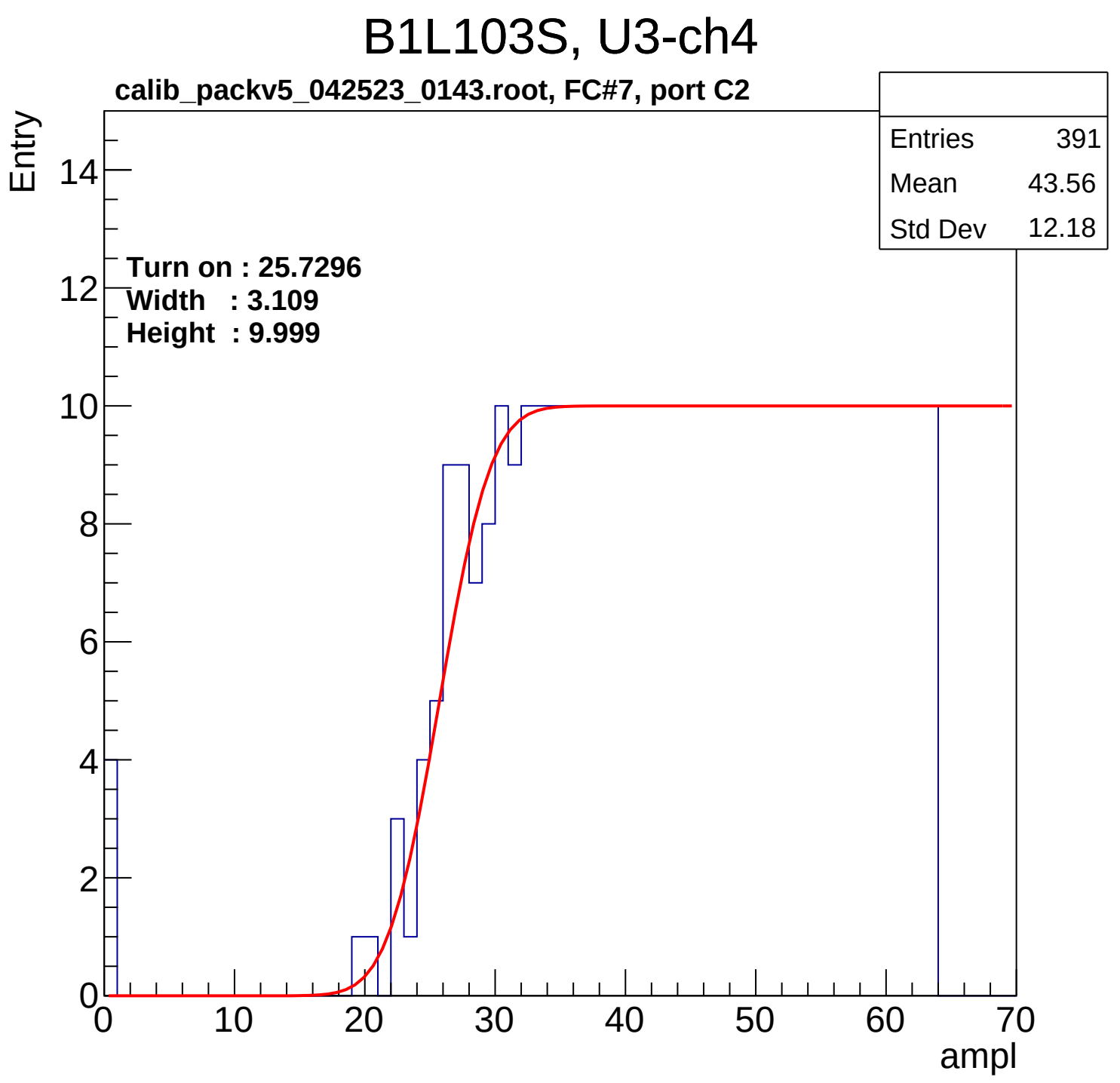
B1L103S, U3-ch4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 391
Mean 43.56
Std Dev 12.18
Turn on : 25.7296
Width : 3.109
Height : 9.999
Entry
ampl
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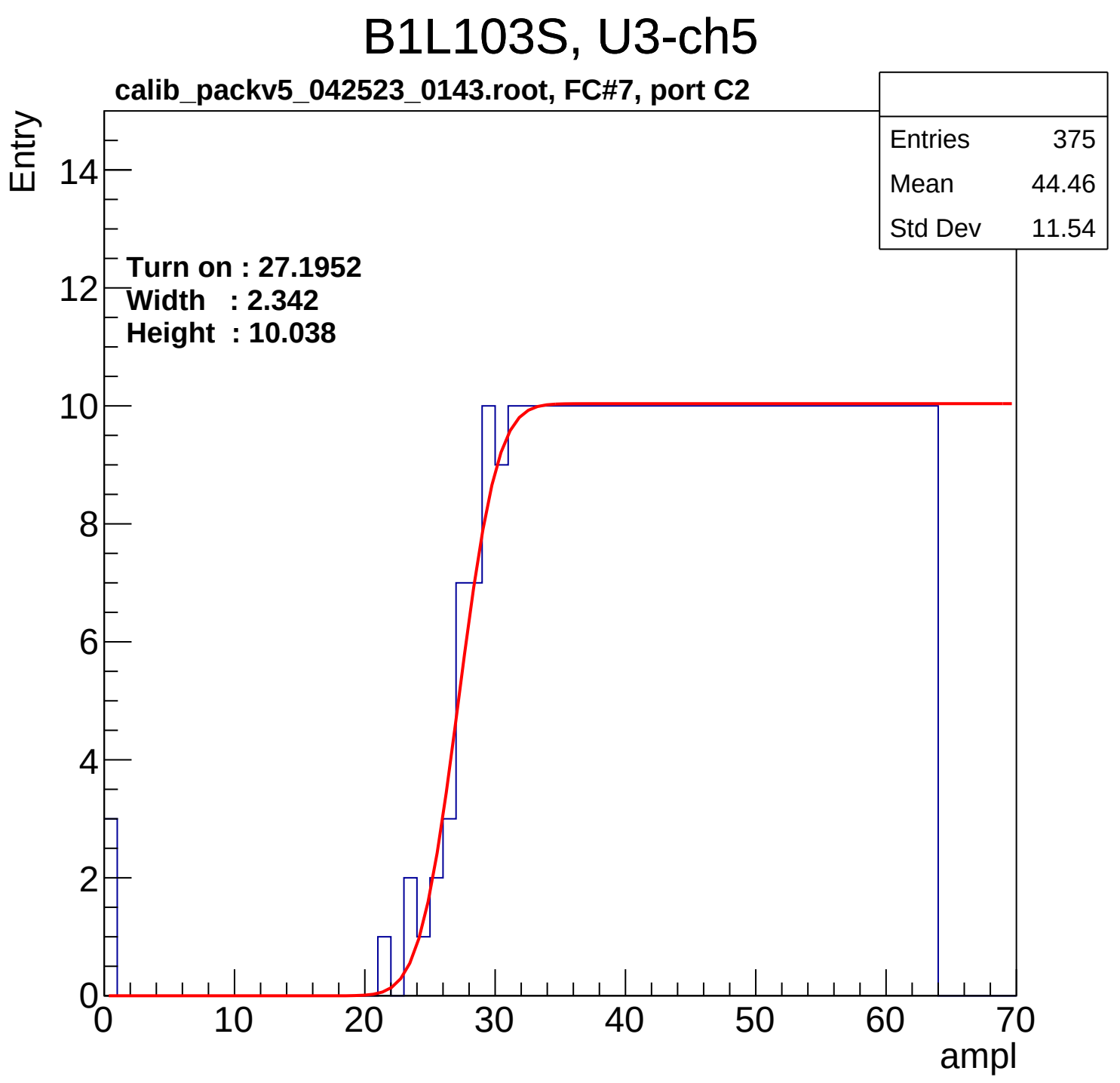
B1L103S, U3-ch5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 375
Mean 44.46
Std Dev 11.54
Turn on : 27.1952
Width : 2.342
Height : 10.038
Entry
ampl
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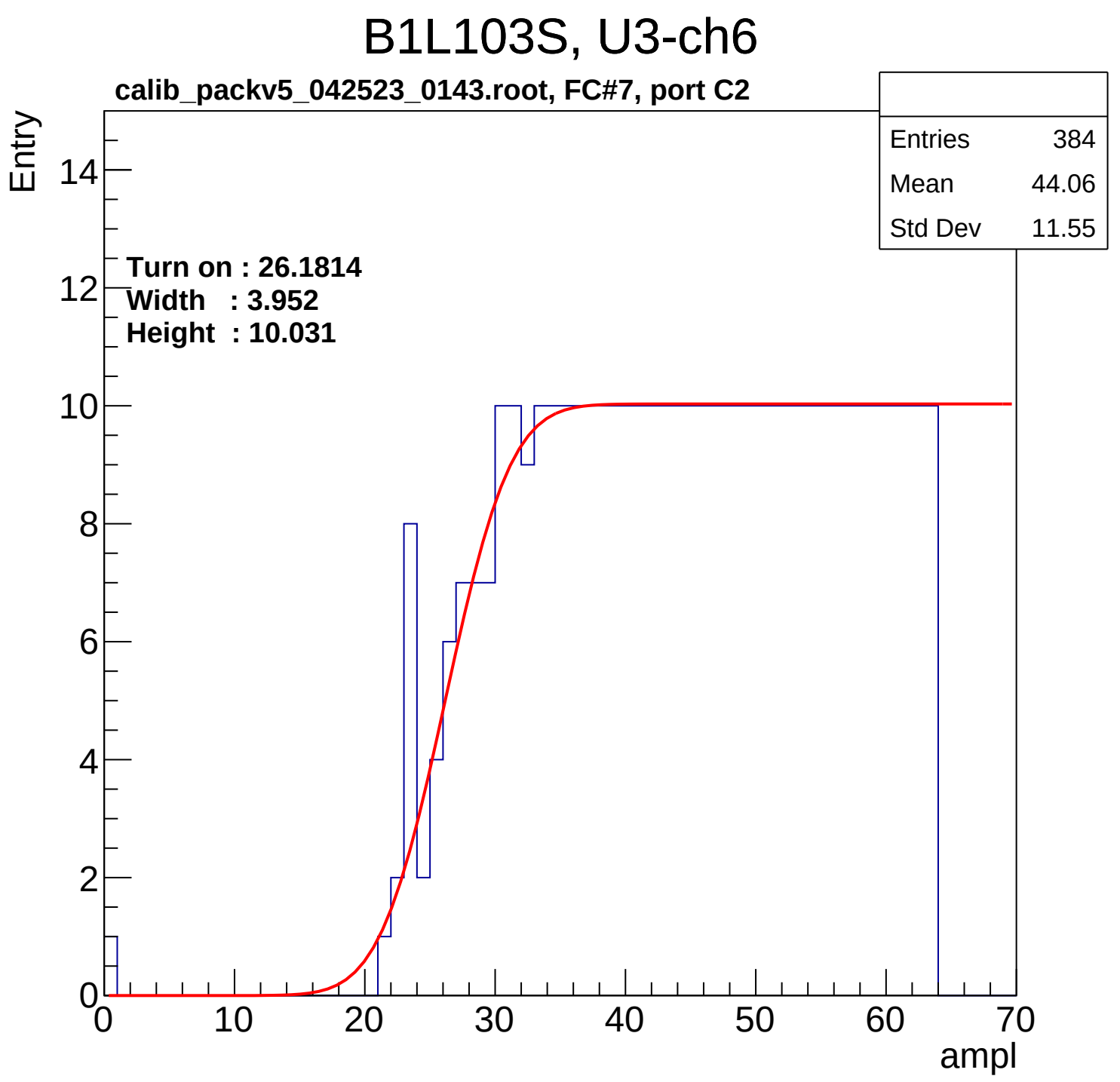
B1L103S, U3-ch6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 384
Mean 44.06
Std Dev 11.55
Turn on : 26.1814
Width : 3.952
Height : 10.031
Entry
ampl
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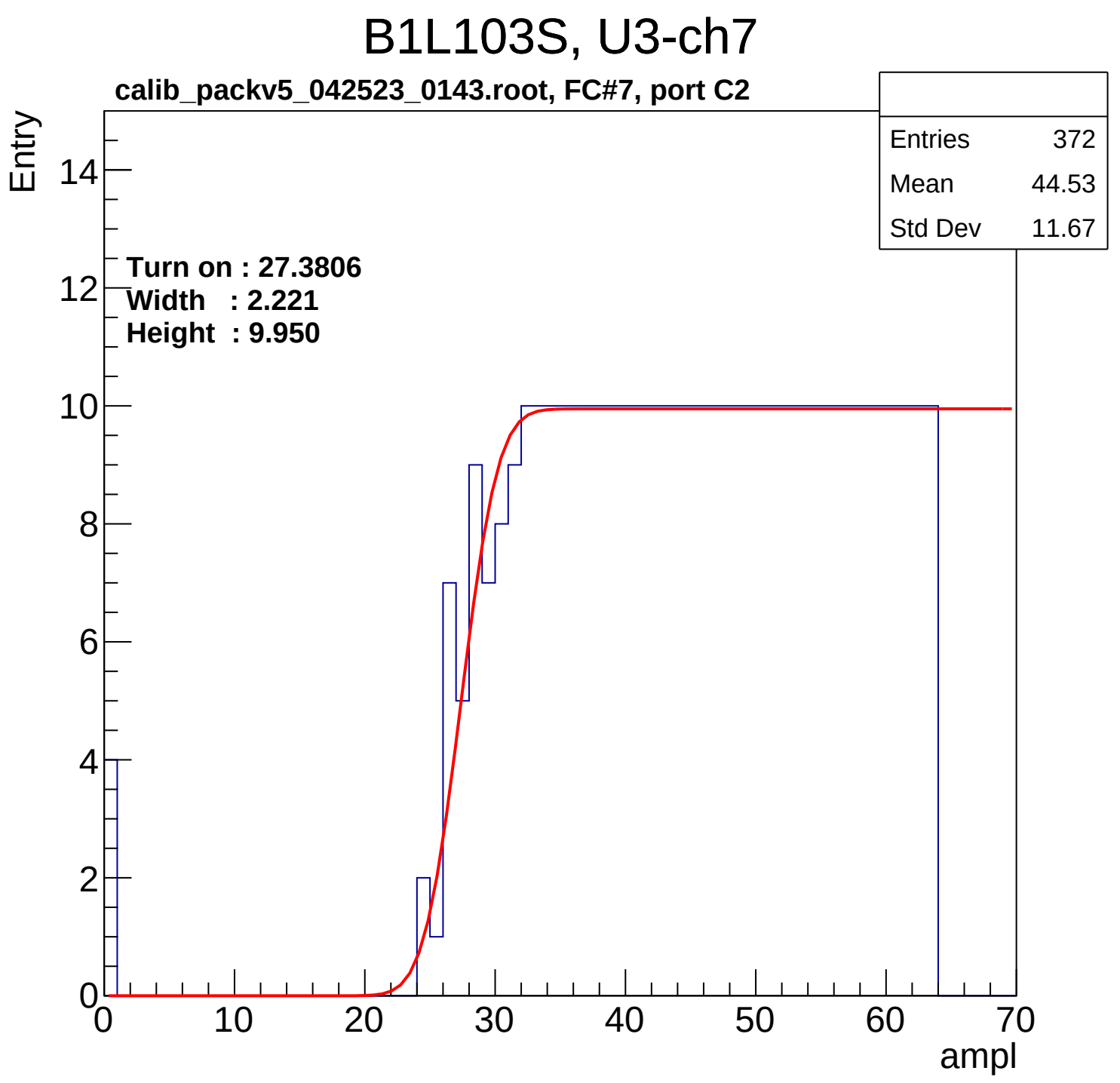
B1L103S, U3-ch7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 372
Mean 44.53
Std Dev 11.67
Turn on : 27.3806
Width : 2.221
Height : 9.950
Entry
ampl
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6
8
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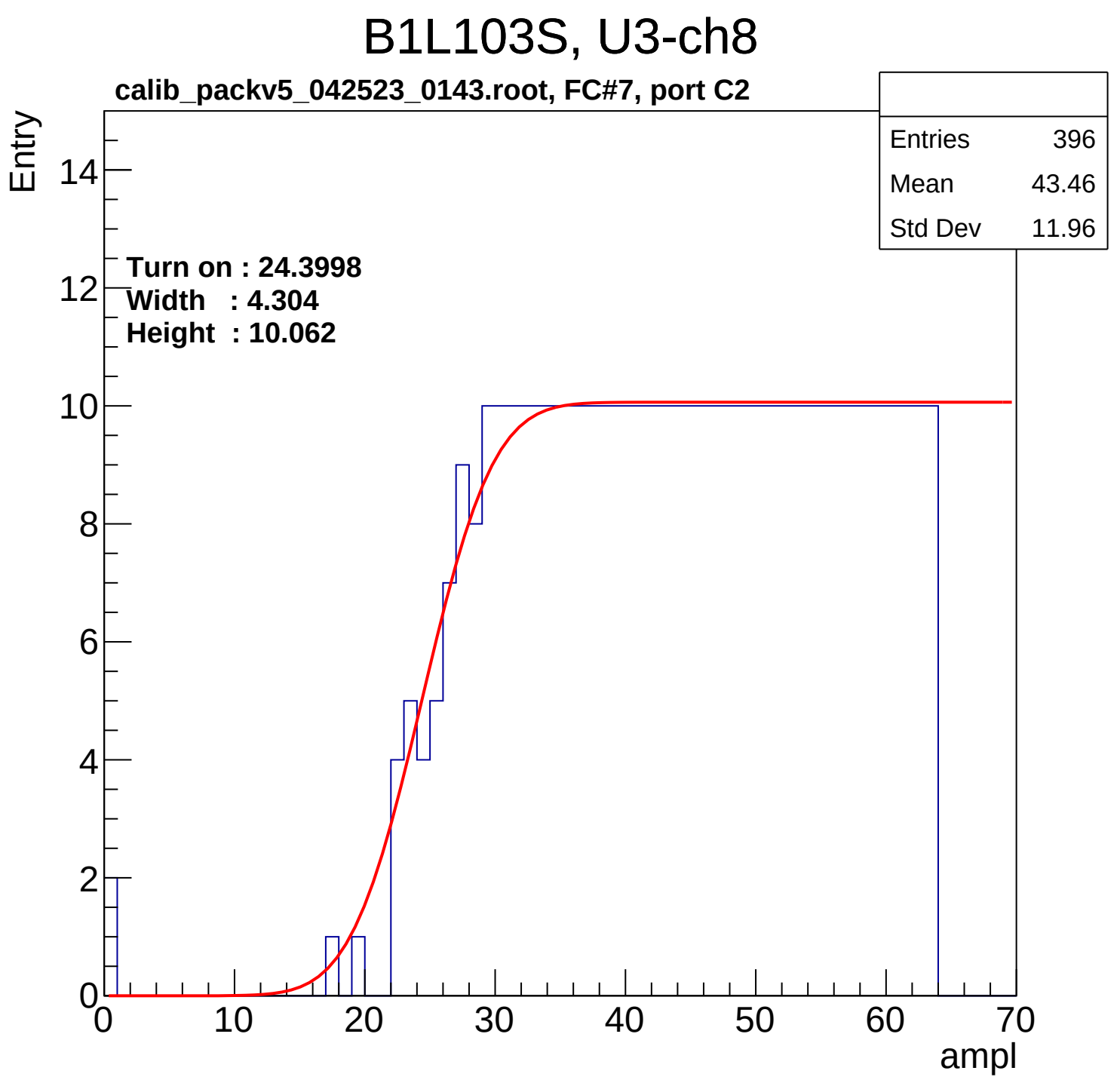
B1L103S, U3-ch8
calib_packv5_042523_0143.root, FC#7, port C2
Entries 396
Mean 43.46
Std Dev 11.96
Turn on : 24.3998
Width : 4.304
Height : 10.062
Entry
ampl
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6
8
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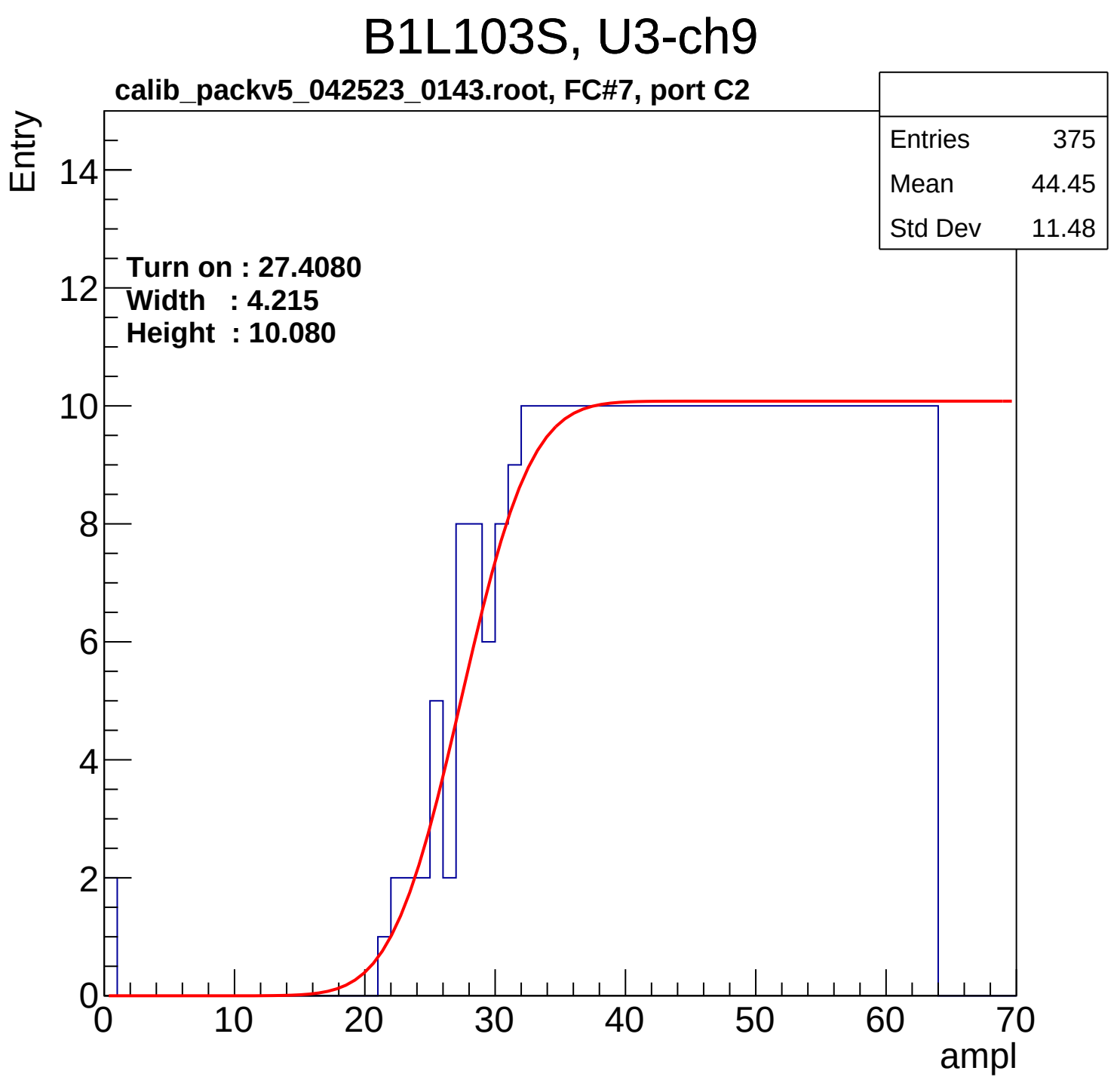
B1L103S, U3-ch9
calib_packv5_042523_0143.root, FC#7, port C2
Entries 375
Mean 44.45
Std Dev 11.48
Turn on : 27.4080
Width : 4.215
Height : 10.080
Entry
ampl
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6
8
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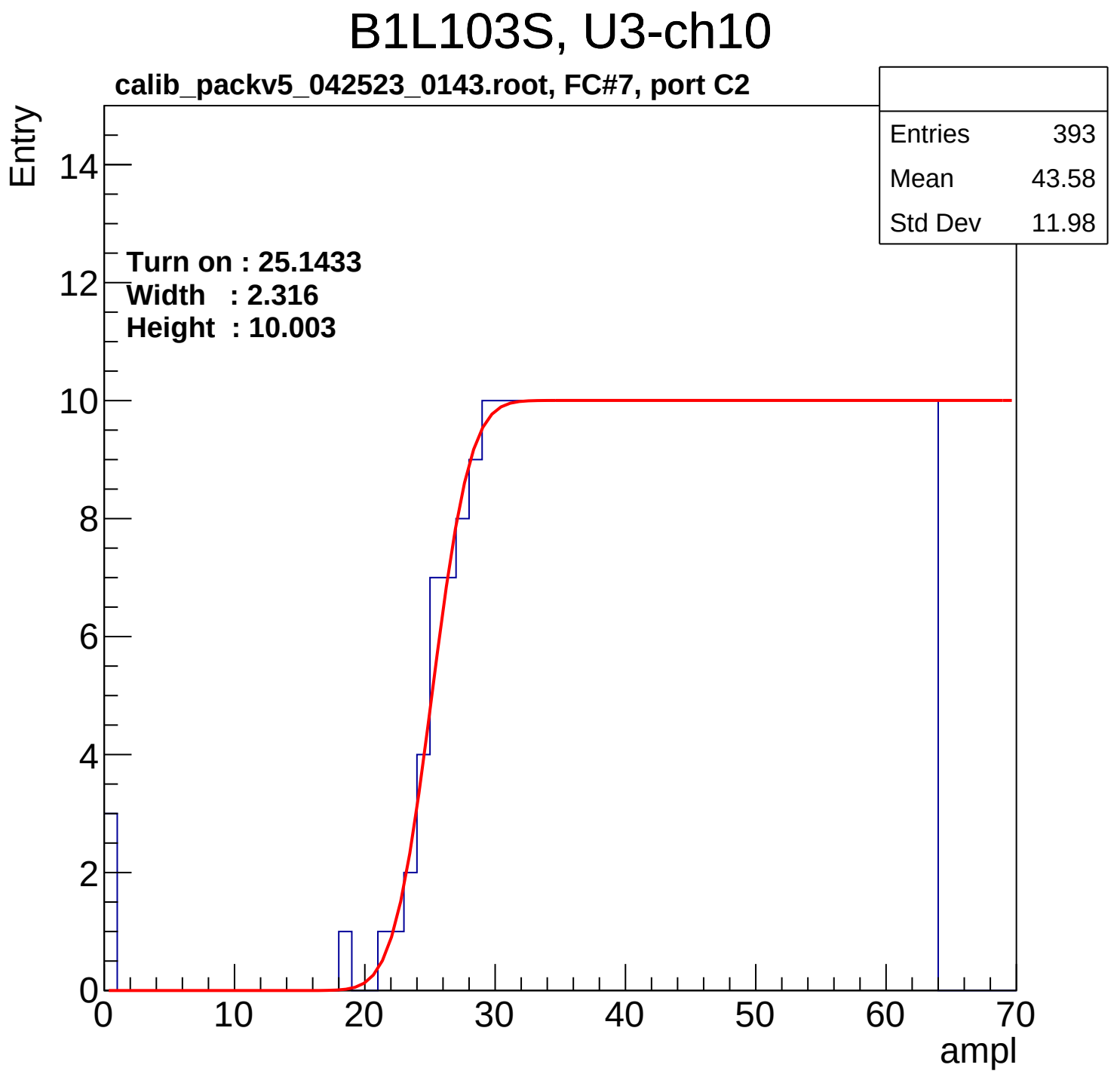
B1L103S, U3-ch10
calib_packv5_042523_0143.root, FC#7, port C2
Entries 393
Mean 43.58
Std Dev 11.98
Turn on : 25.1433
Width : 2.316
Height : 10.003
Entry
ampl
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6
8
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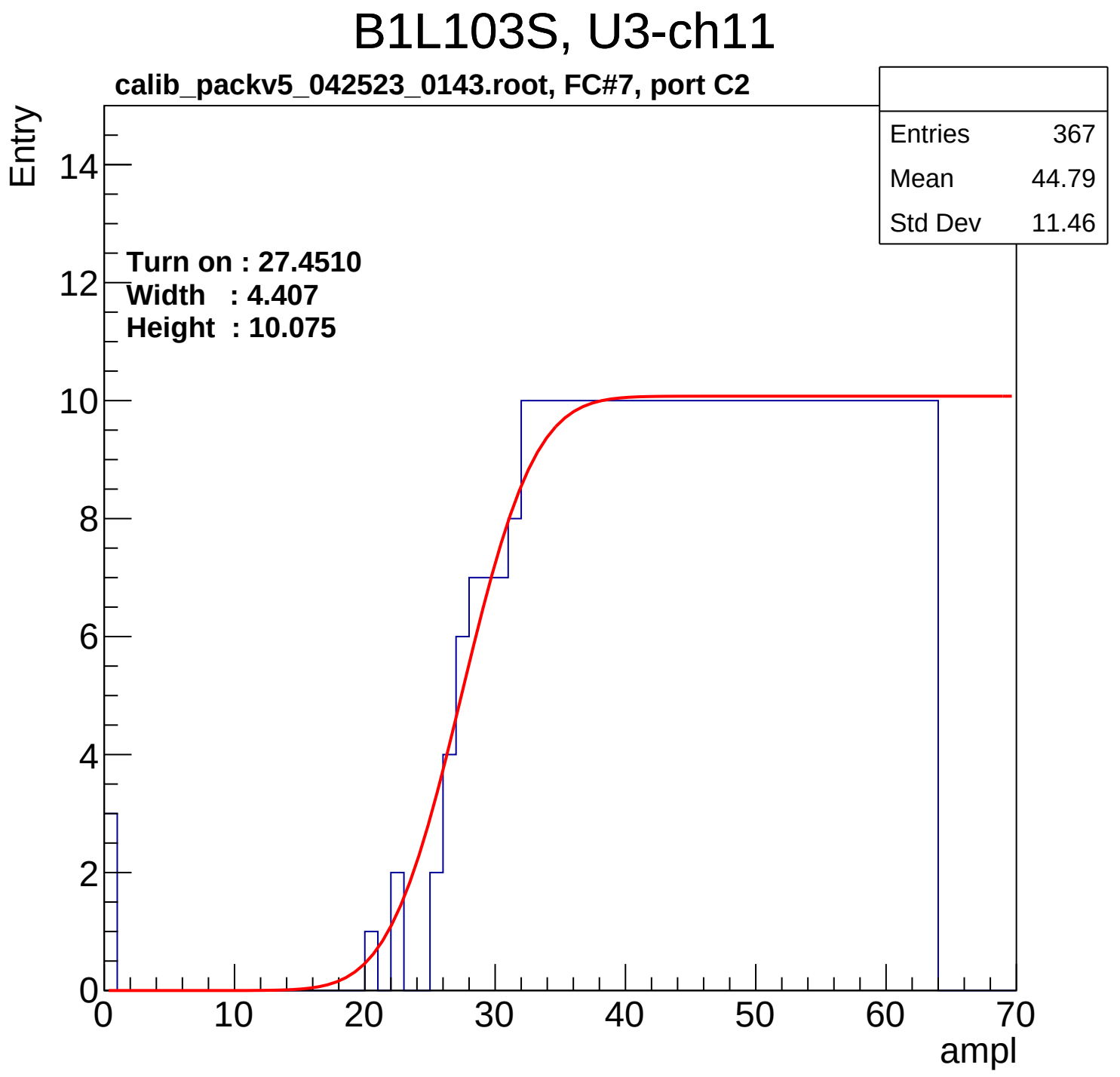
B1L103S, U3-ch11
calib_packv5_042523_0143.root, FC#7, port C2
Entries 367
Mean 44.79
Std Dev 11.46
Turn on : 27.4510
Width : 4.407
Height : 10.075
Entry
ampl
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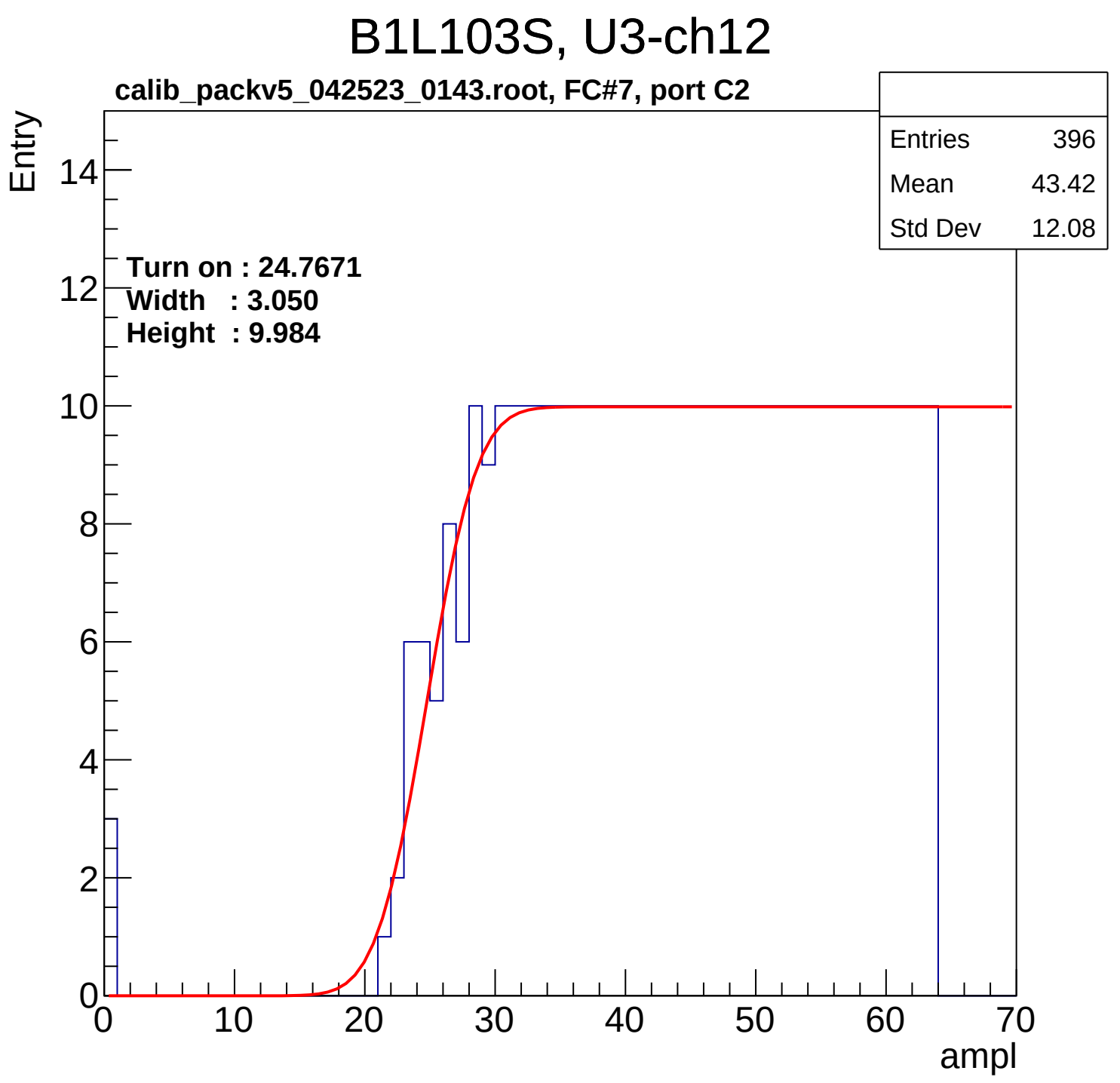
B1L103S, U3-ch12
calib_packv5_042523_0143.root, FC#7, port C2
Entries 396
Mean 43.42
Std Dev 12.08
Turn on : 24.7671
Width : 3.050
Height : 9.984
Entry
ampl
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6
8
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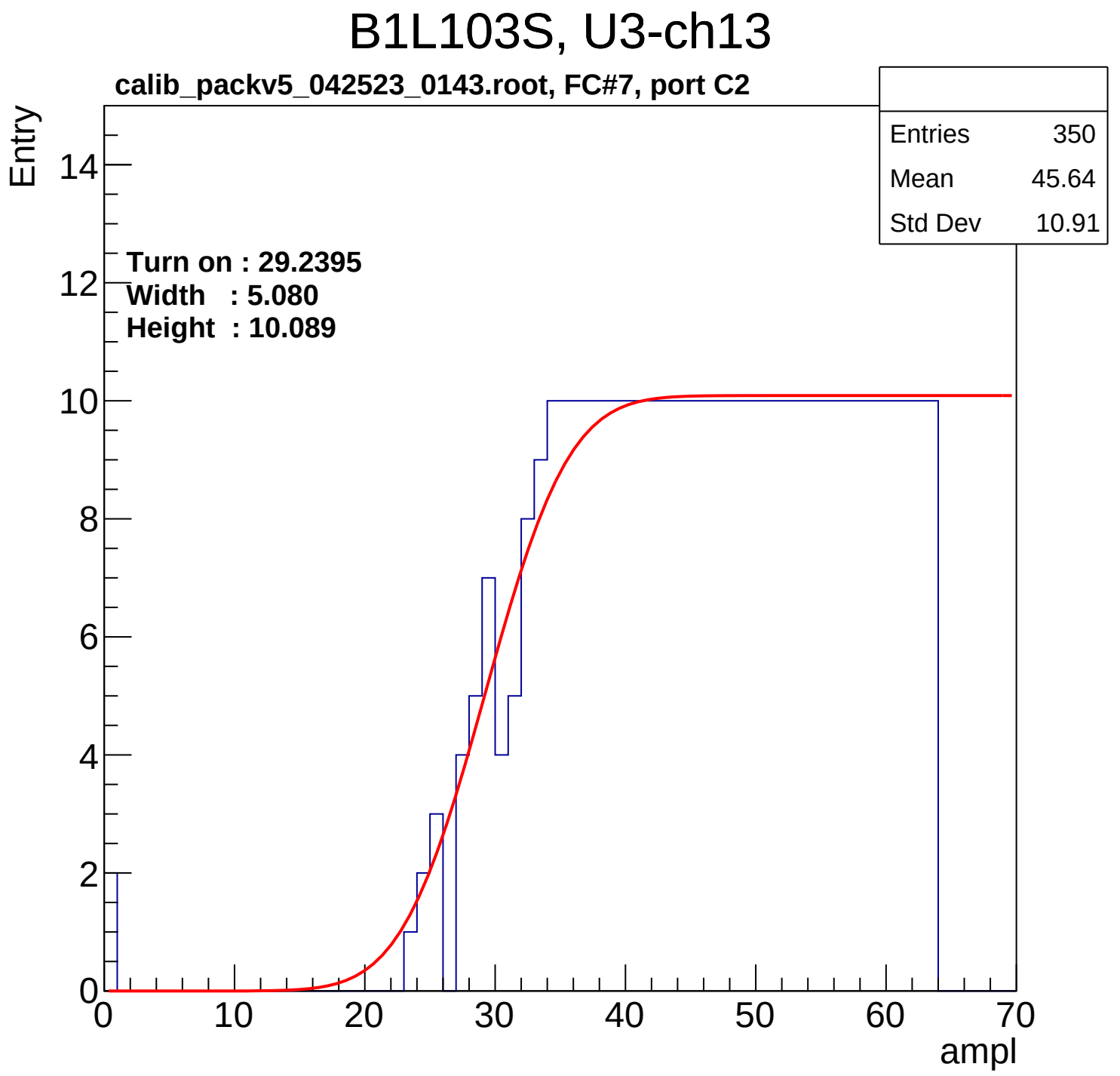
B1L103S, U3-ch13
calib_packv5_042523_0143.root, FC#7, port C2
Entries 350
Mean 45.64
Std Dev 10.91
Turn on : 29.2395
Width : 5.080
Height : 10.089
Entry
ampl
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4
6
8
10
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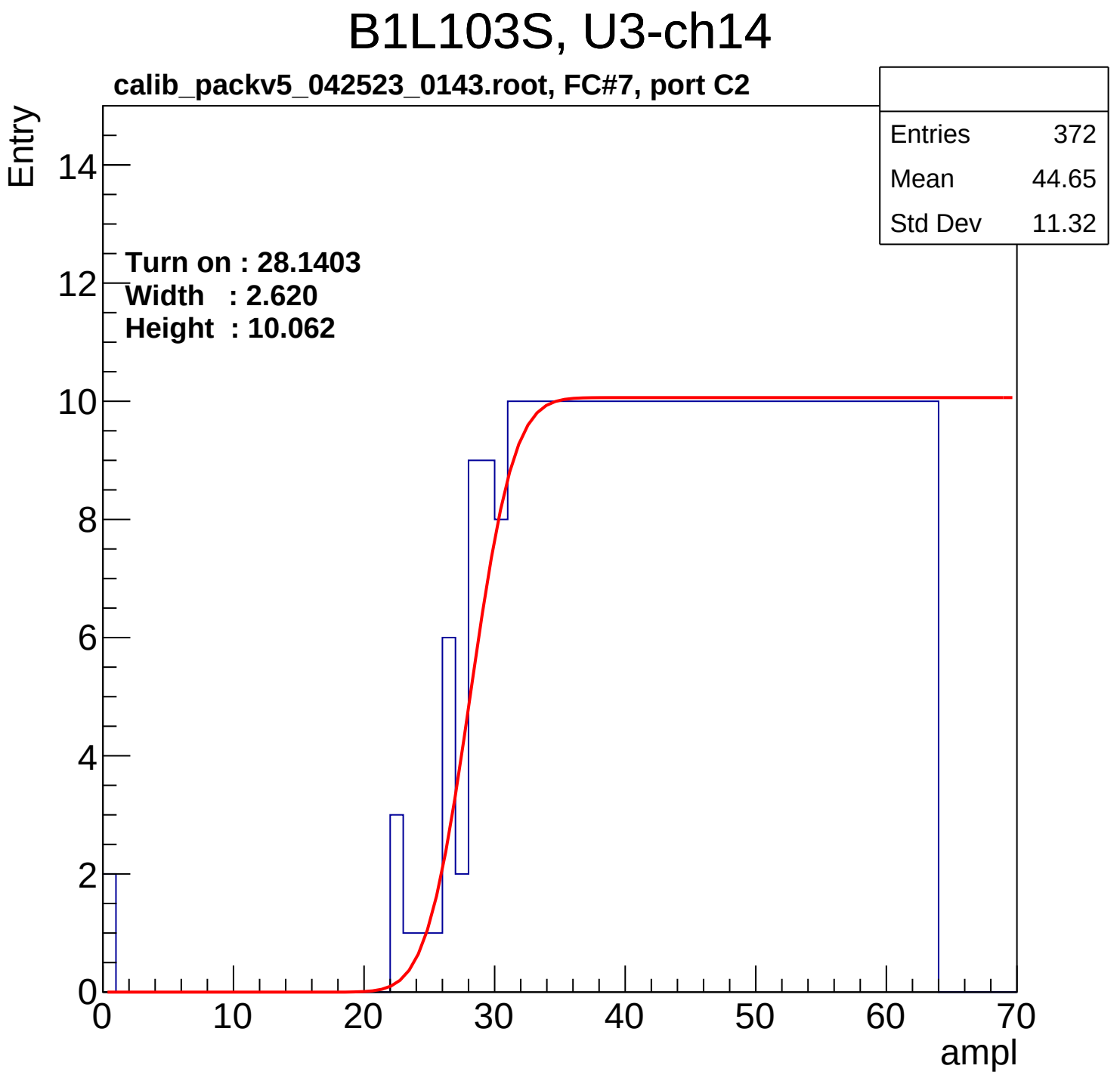
B1L103S, U3-ch14
calib_packv5_042523_0143.root, FC#7, port C2
Entries 372
Mean 44.65
Std Dev 11.32
Turn on : 28.1403
Width : 2.620
Height : 10.062
Entry
ampl
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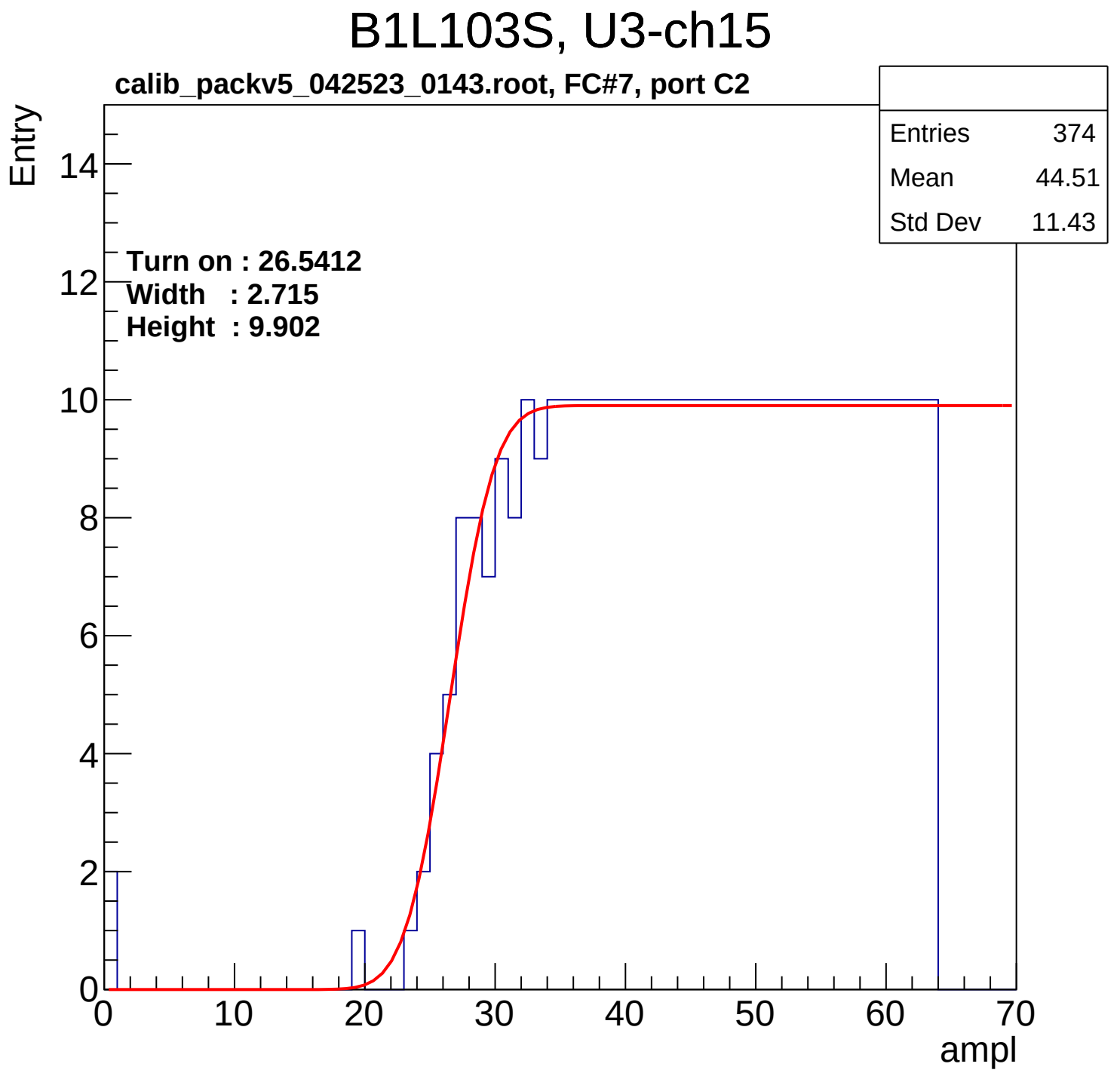
B1L103S, U3-ch15
calib_packv5_042523_0143.root, FC#7, port C2
Entries 374
Mean 44.51
Std Dev 11.43
Turn on : 26.5412
Width : 2.715
Height : 9.902
Entry
ampl
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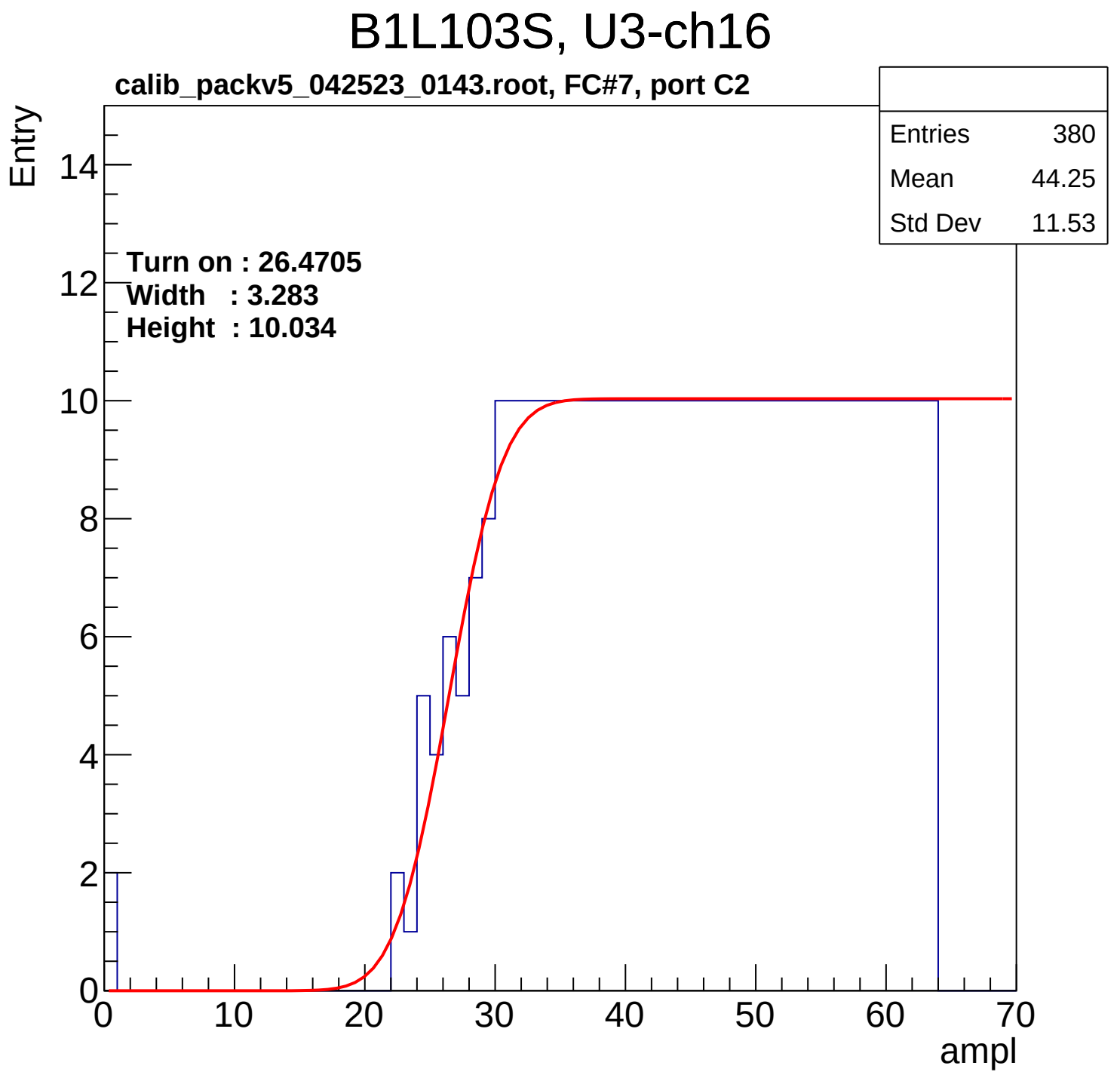
B1L103S, U3-ch16
calib_packv5_042523_0143.root, FC#7, port C2
Entries 380
Mean 44.25
Std Dev 11.53
Turn on : 26.4705
Width : 3.283
Height : 10.034
Entry
ampl
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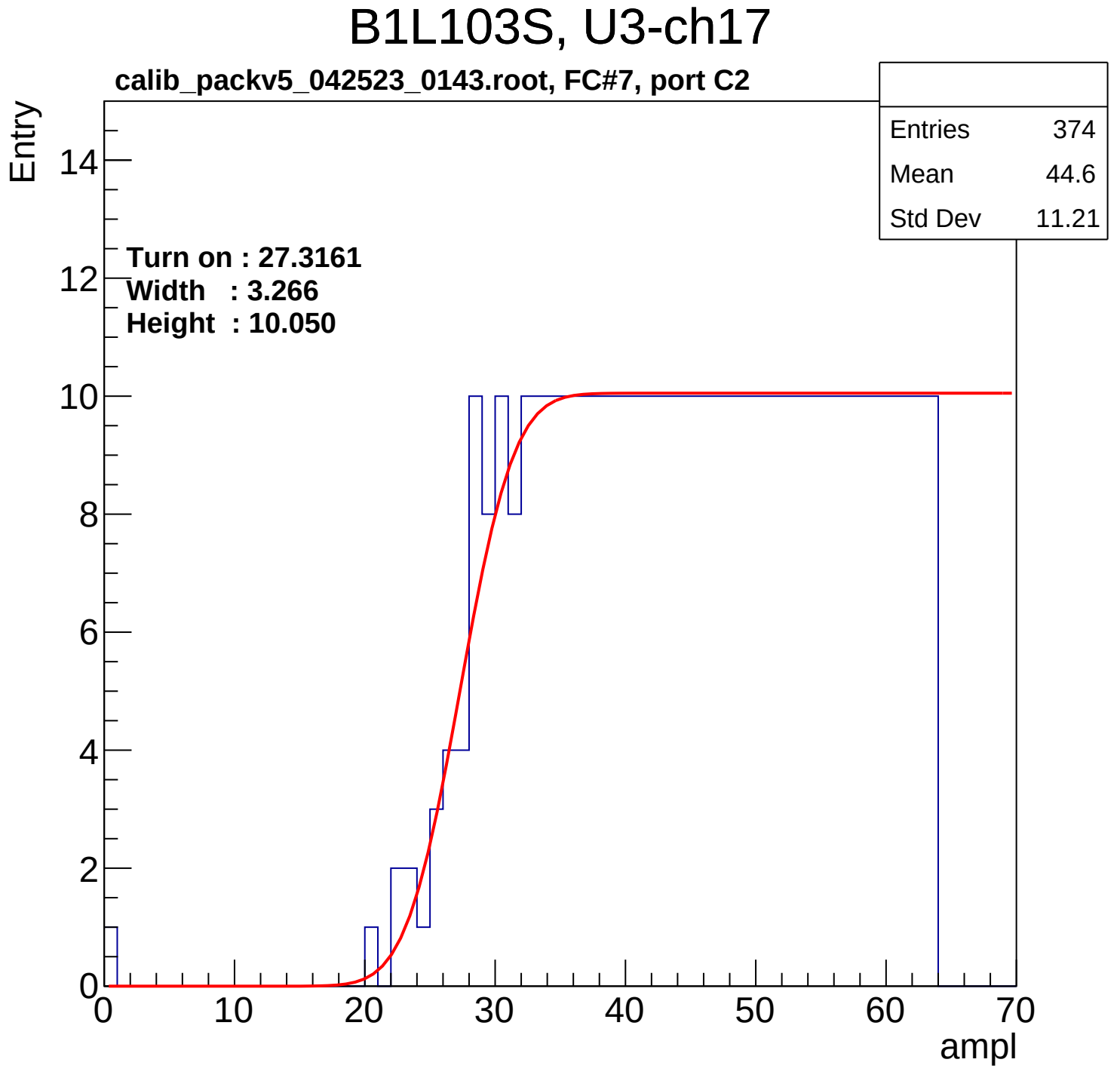
B1L103S, U3-ch17
calib_packv5_042523_0143.root, FC#7, port C2
Entries 374
Mean 44.6
Std Dev 11.21
Turn on : 27.3161
Width : 3.266
Height : 10.050
Entry
ampl
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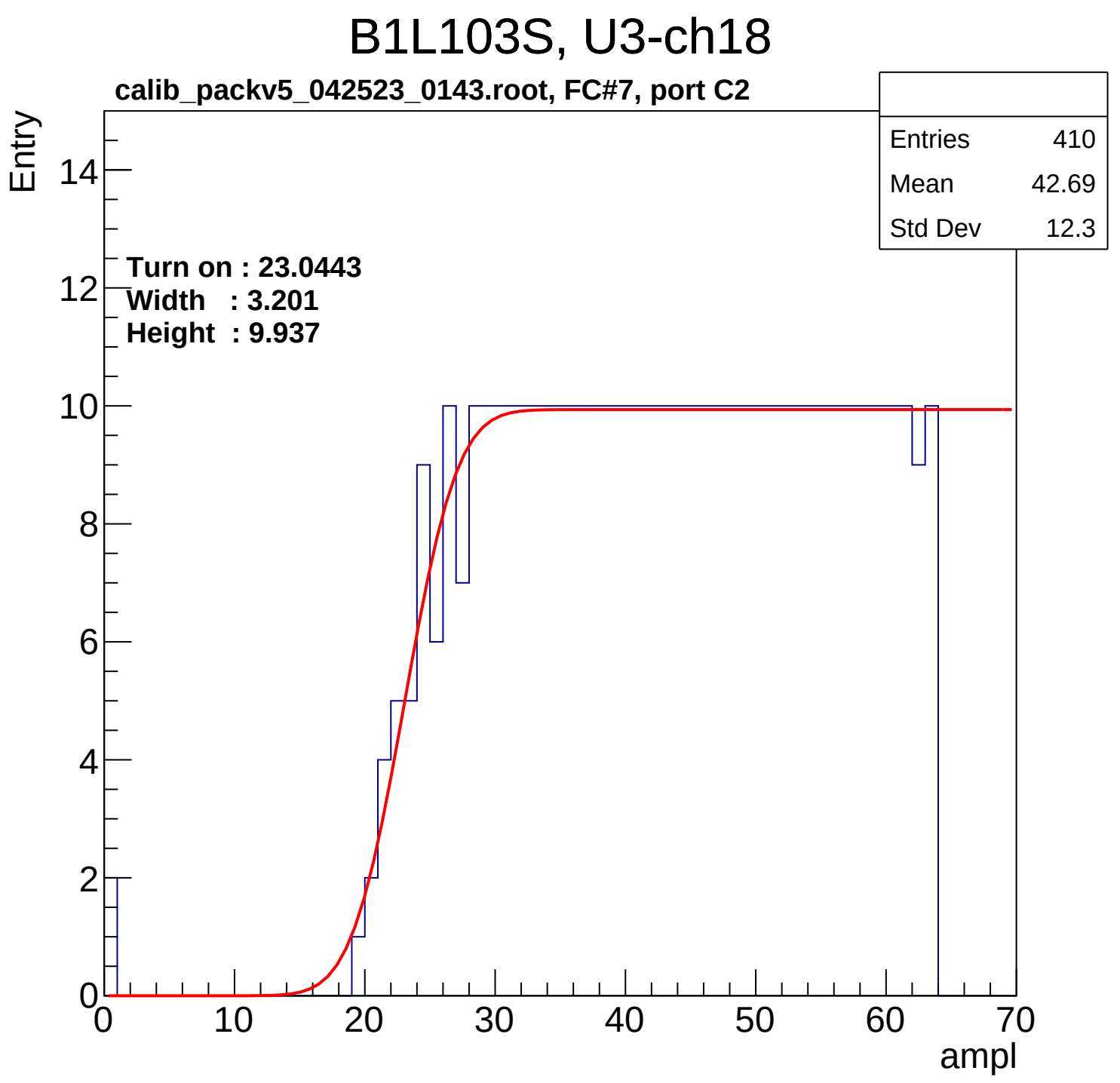
B1L103S, U3-ch18
calib_packv5_042523_0143.root, FC#7, port C2
Entries 410
Mean 42.69
Std Dev 12.3
Turn on : 23.0443
Width : 3.201
Height : 9.937
Entry
ampl
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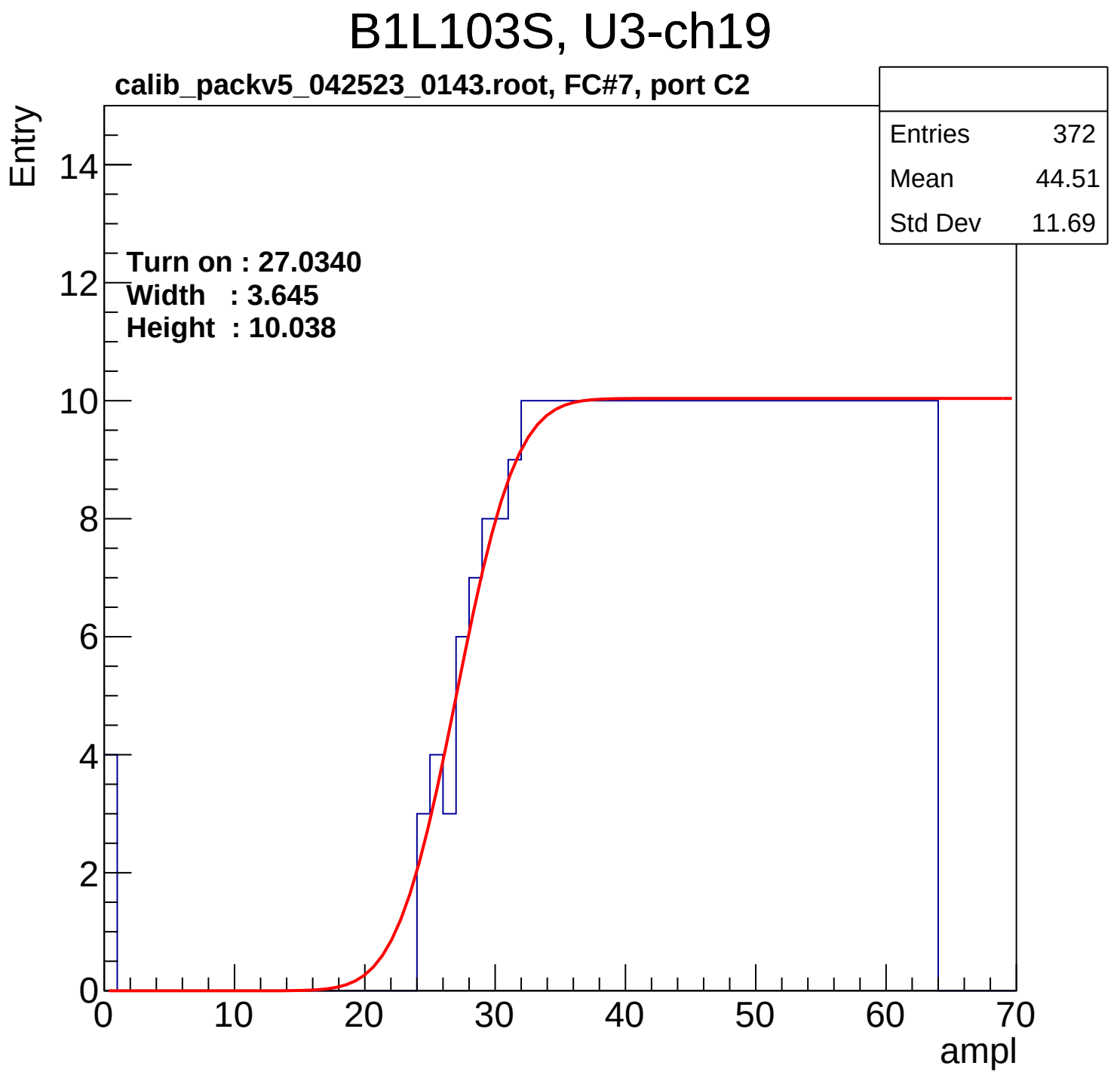
B1L103S, U3-ch19
calib_packv5_042523_0143.root, FC#7, port C2
Entries 372
Mean 44.51
Std Dev 11.69
Turn on : 27.0340
Width : 3.645
Height : 10.038
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ampl
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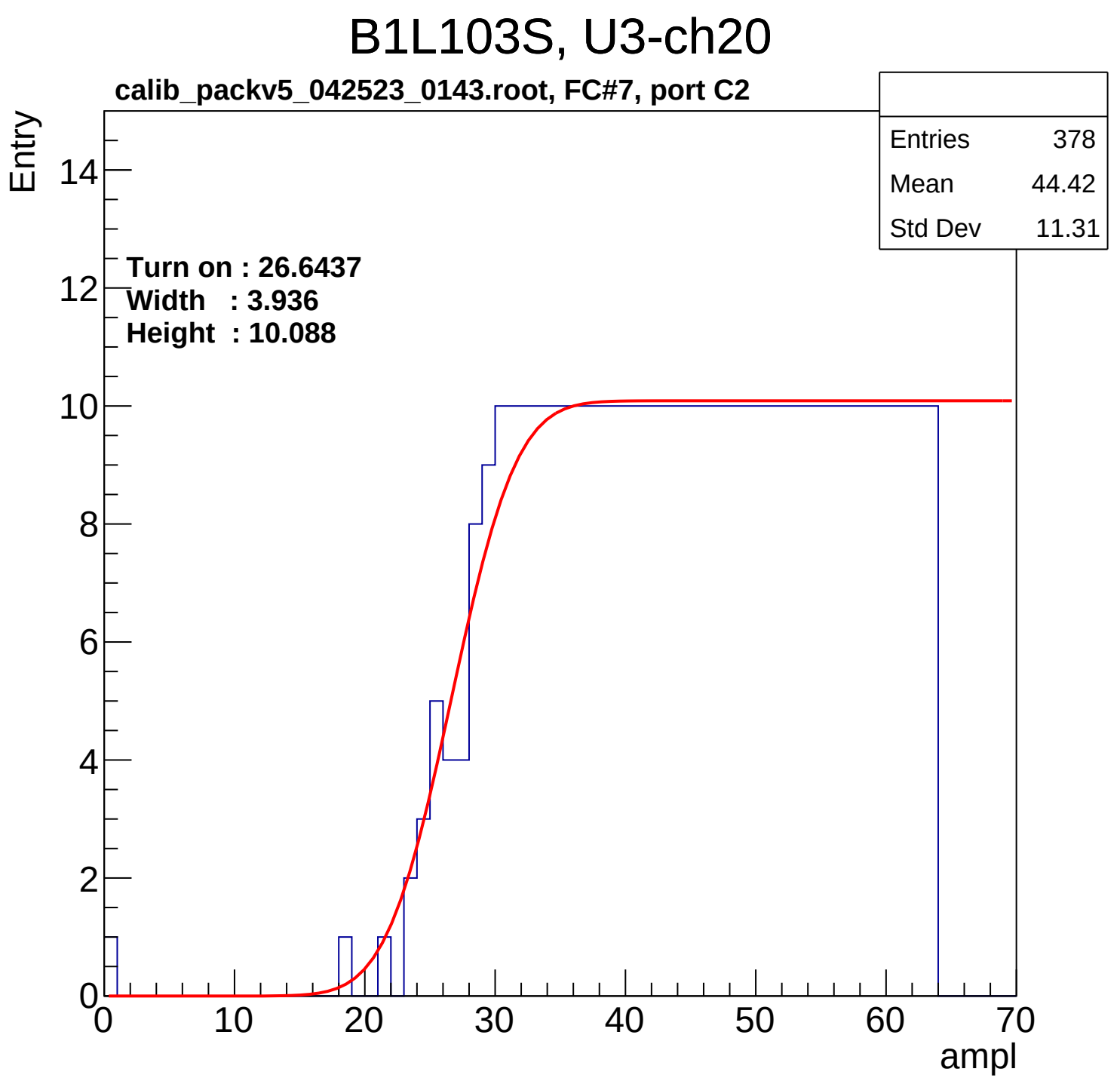
B1L103S, U3-ch20
calib_packv5_042523_0143.root, FC#7, port C2
Entries 378
Mean 44.42
Std Dev 11.31
Turn on : 26.6437
Width : 3.936
Height : 10.088
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ampl
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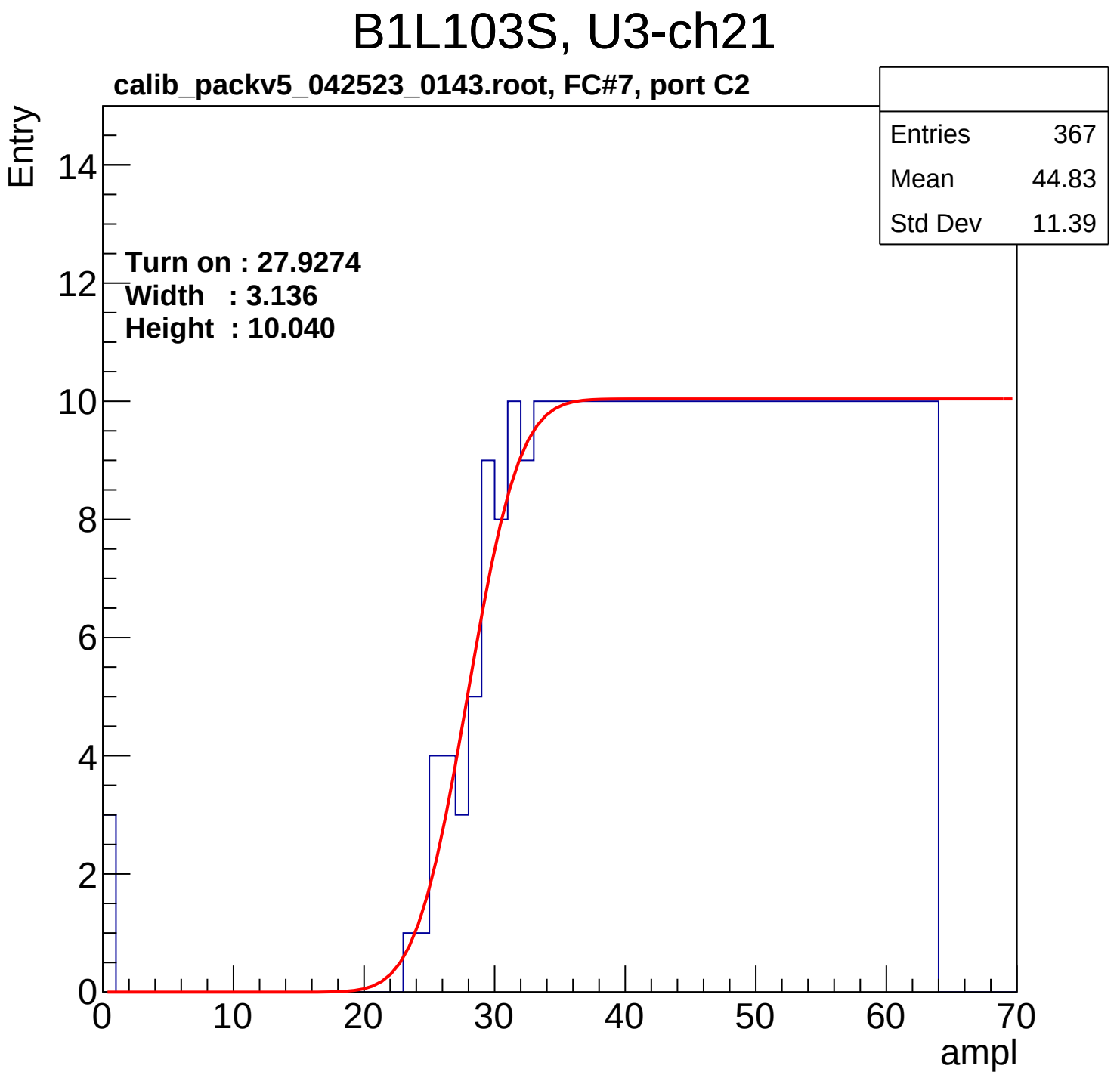
B1L103S, U3-ch21
calib_packv5_042523_0143.root, FC#7, port C2
Entries 367
Mean 44.83
Std Dev 11.39
Turn on : 27.9274
Width : 3.136
Height : 10.040
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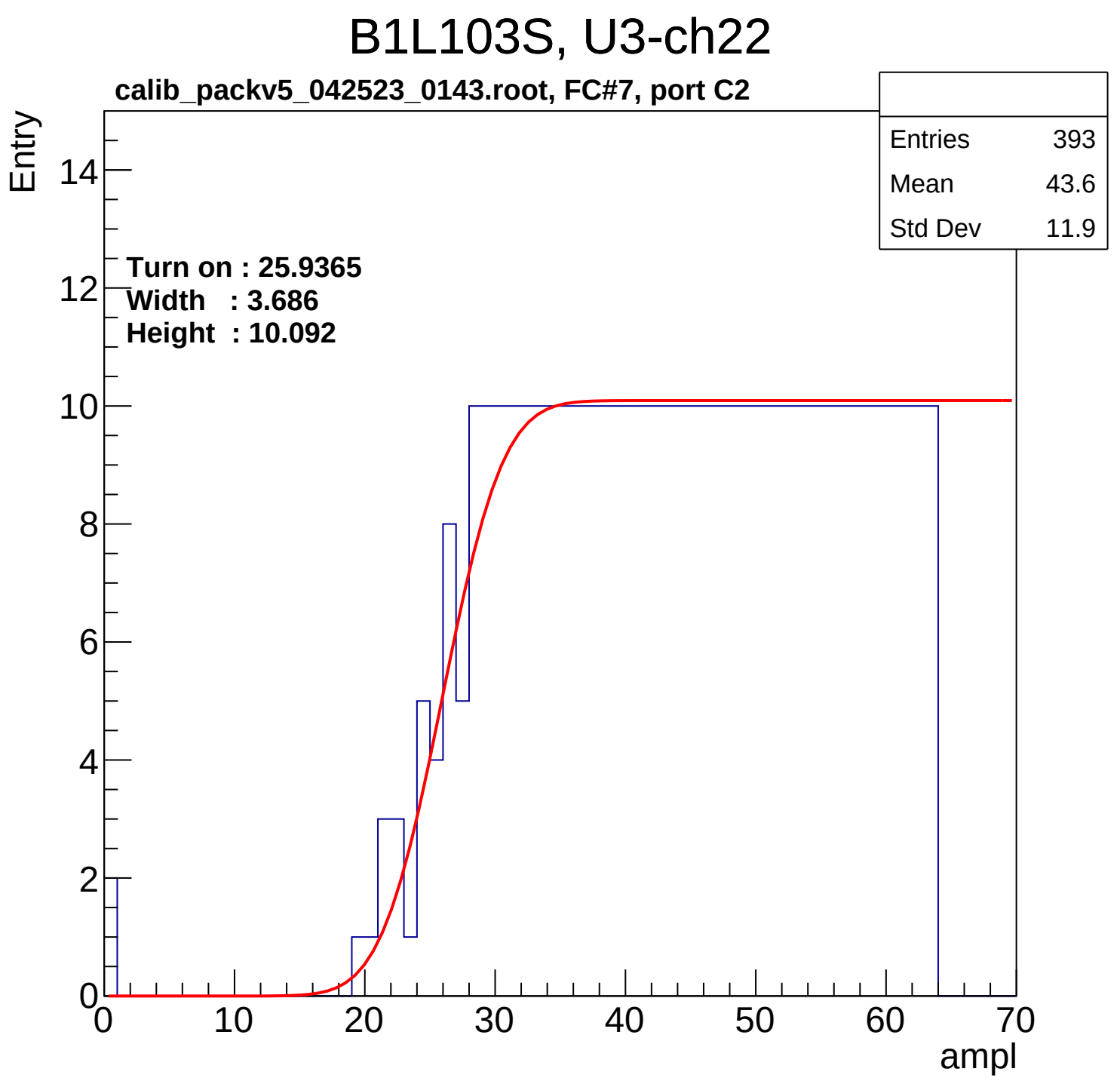
B1L103S, U3-ch22
calib_packv5_042523_0143.root, FC#7, port C2
Entries 393
Mean 43.6
Std Dev 11.9
Turn on : 25.9365
Width : 3.686
Height : 10.092
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ampl
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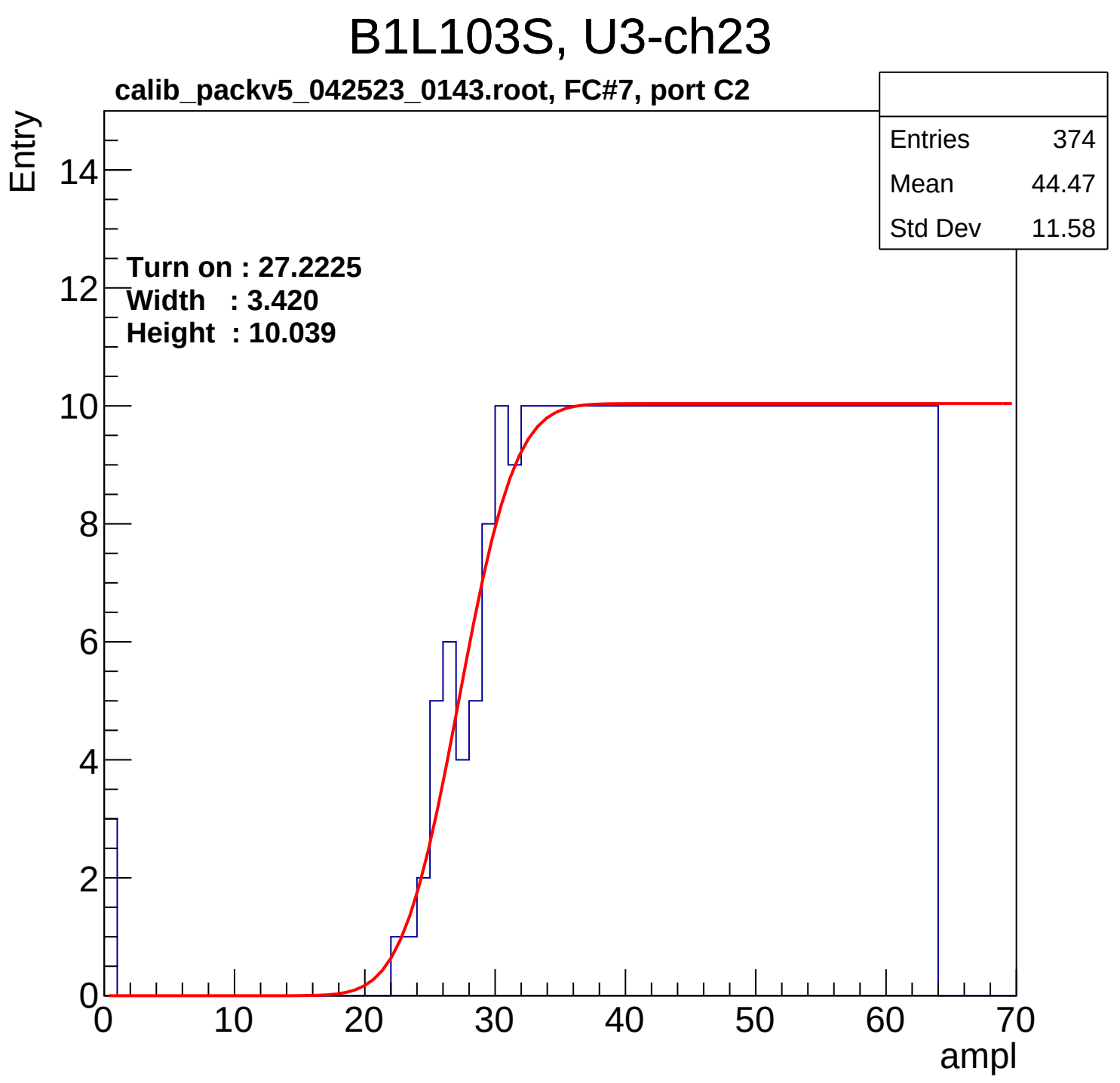
B1L103S, U3-ch23
calib_packv5_042523_0143.root, FC#7, port C2
Entries 374
Mean 44.47
Std Dev 11.58
Turn on : 27.2225
Width : 3.420
Height : 10.039
Entry
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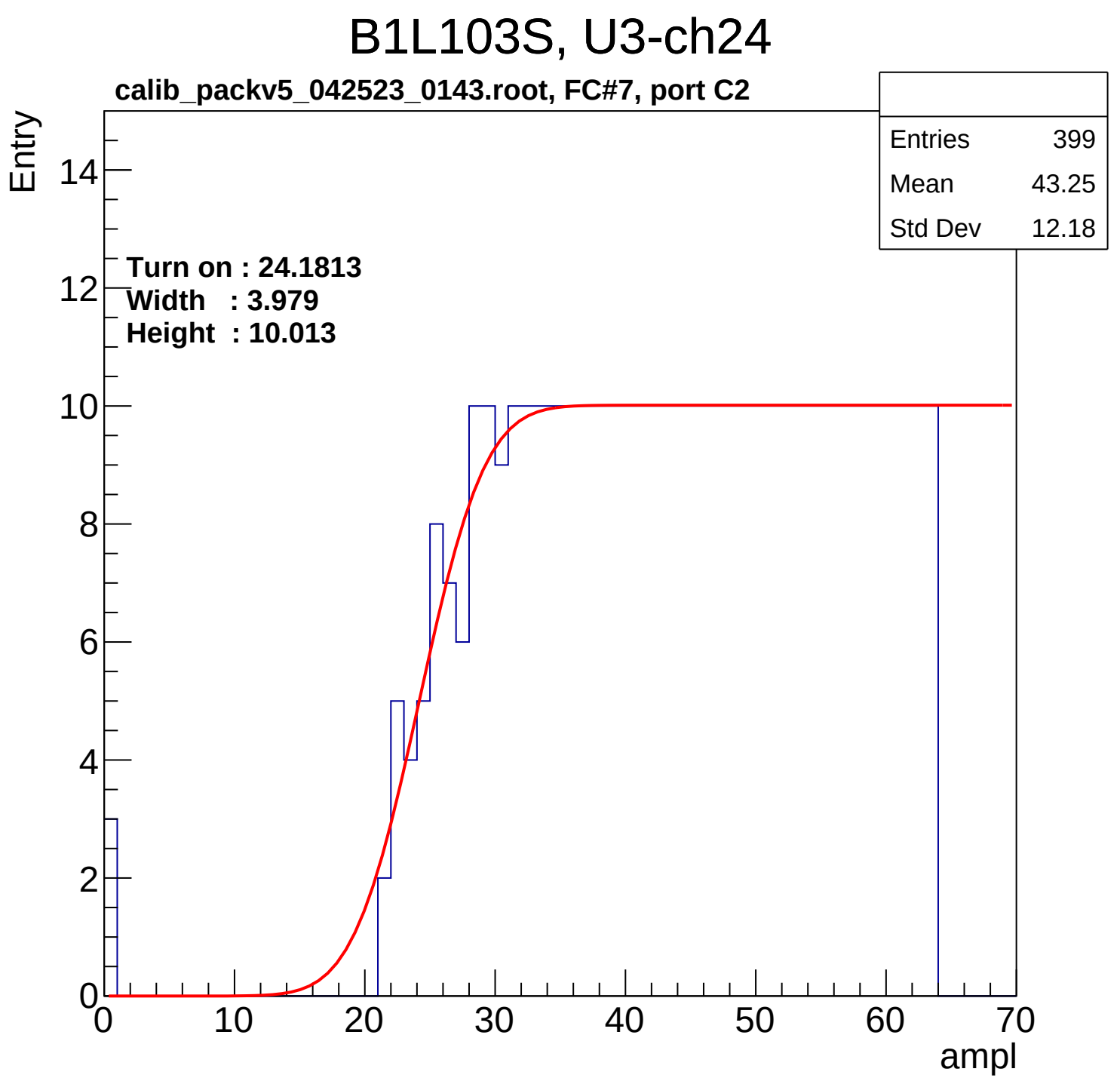
B1L103S, U3-ch24
calib_packv5_042523_0143.root, FC#7, port C2
Entries 399
Mean 43.25
Std Dev 12.18
Turn on : 24.1813
Width : 3.979
Height : 10.013
Entry
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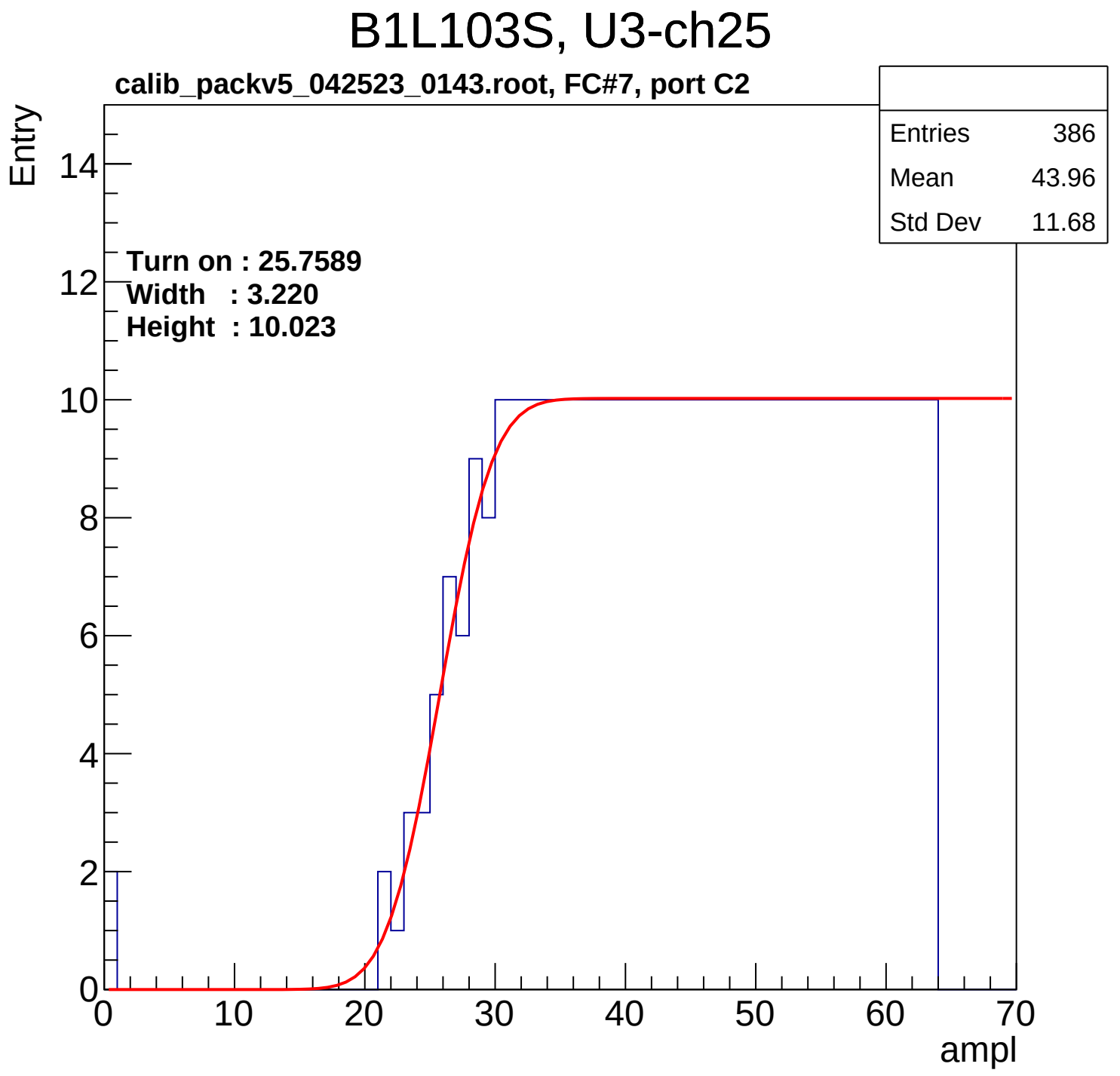
B1L103S, U3-ch25
calib_packv5_042523_0143.root, FC#7, port C2
Entries 386
Mean 43.96
Std Dev 11.68
Turn on : 25.7589
Width : 3.220
Height : 10.023
Entry
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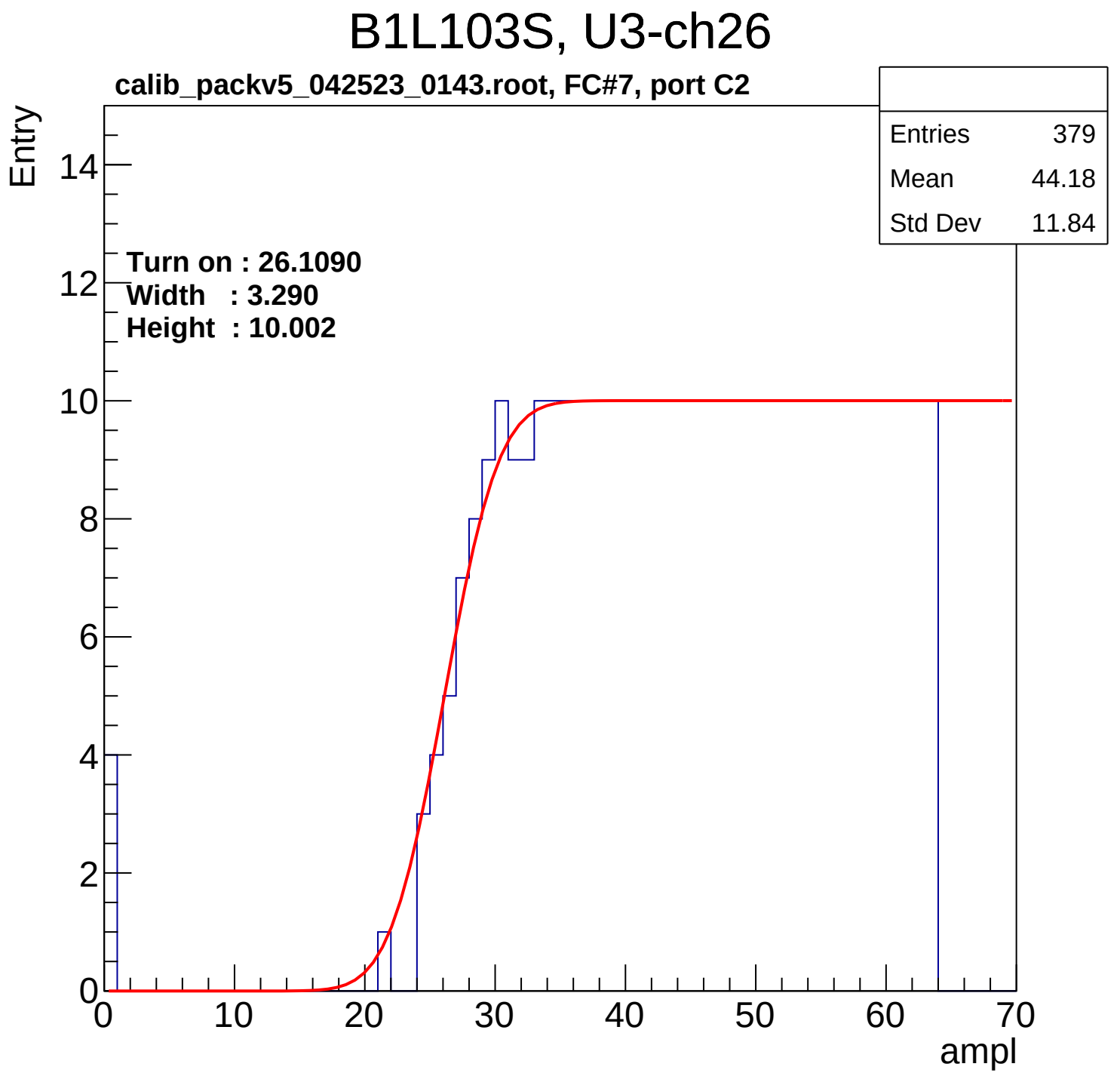
B1L103S, U3-ch26
calib_packv5_042523_0143.root, FC#7, port C2
Entries 379
Mean 44.18
Std Dev 11.84
Turn on : 26.1090
Width : 3.290
Height : 10.002
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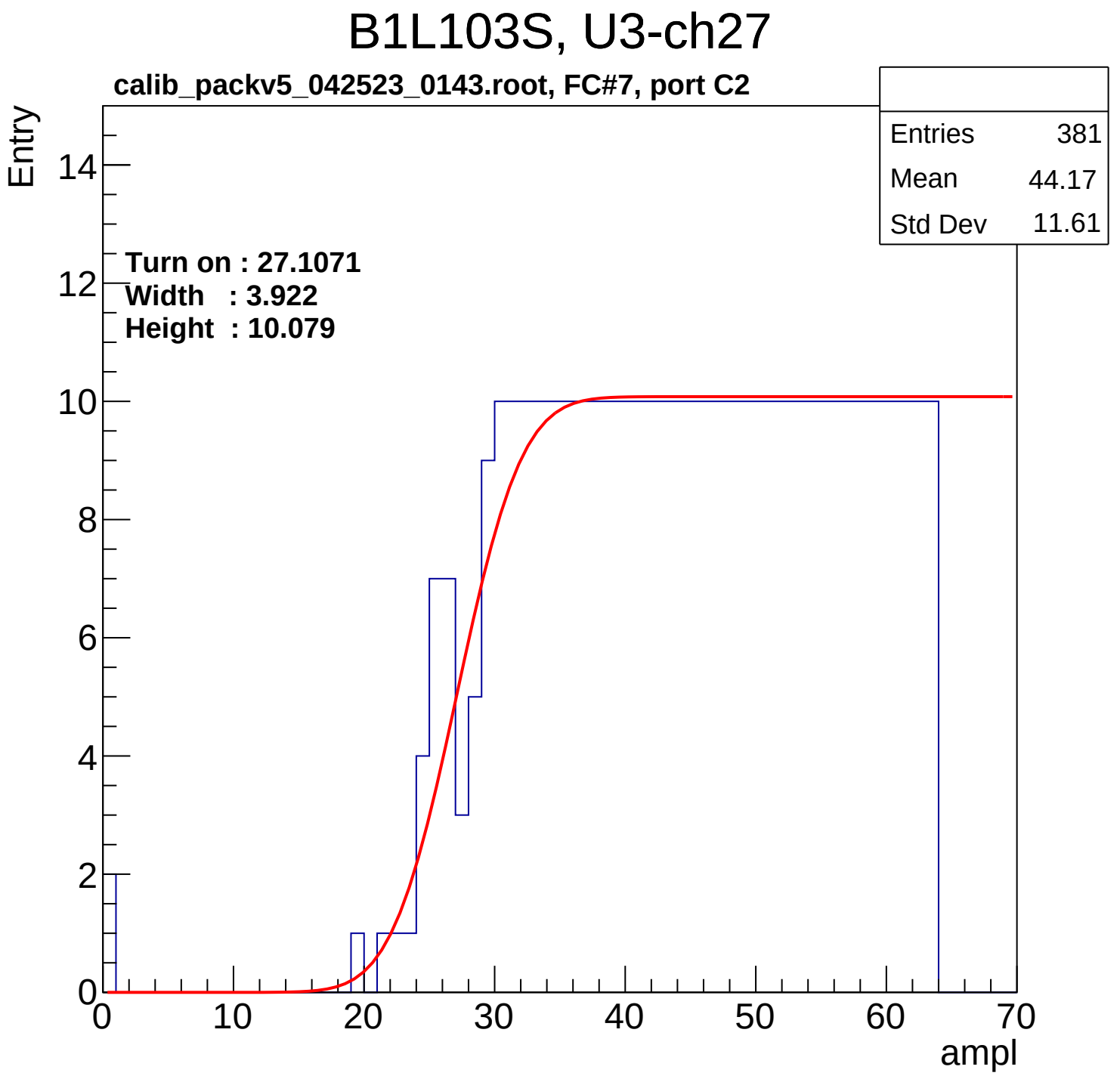
B1L103S, U3-ch27
calib_packv5_042523_0143.root, FC#7, port C2
Entries 381
Mean 44.17
Std Dev 11.61
Turn on : 27.1071
Width : 3.922
Height : 10.079
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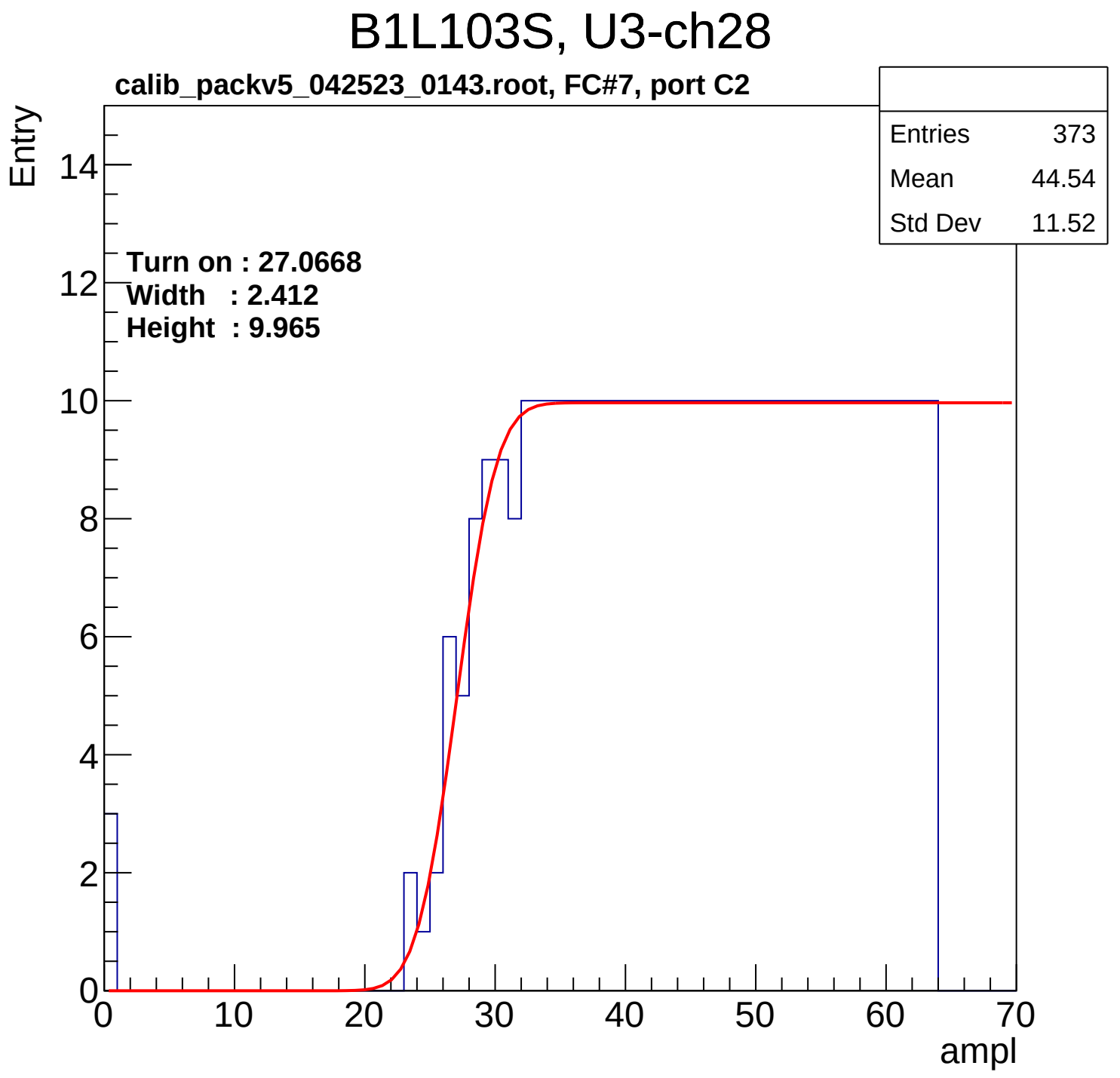
B1L103S, U3-ch28
calib_packv5_042523_0143.root, FC#7, port C2
Entries 373
Mean 44.54
Std Dev 11.52
Turn on : 27.0668
Width : 2.412
Height : 9.965
Entry
ampl
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4
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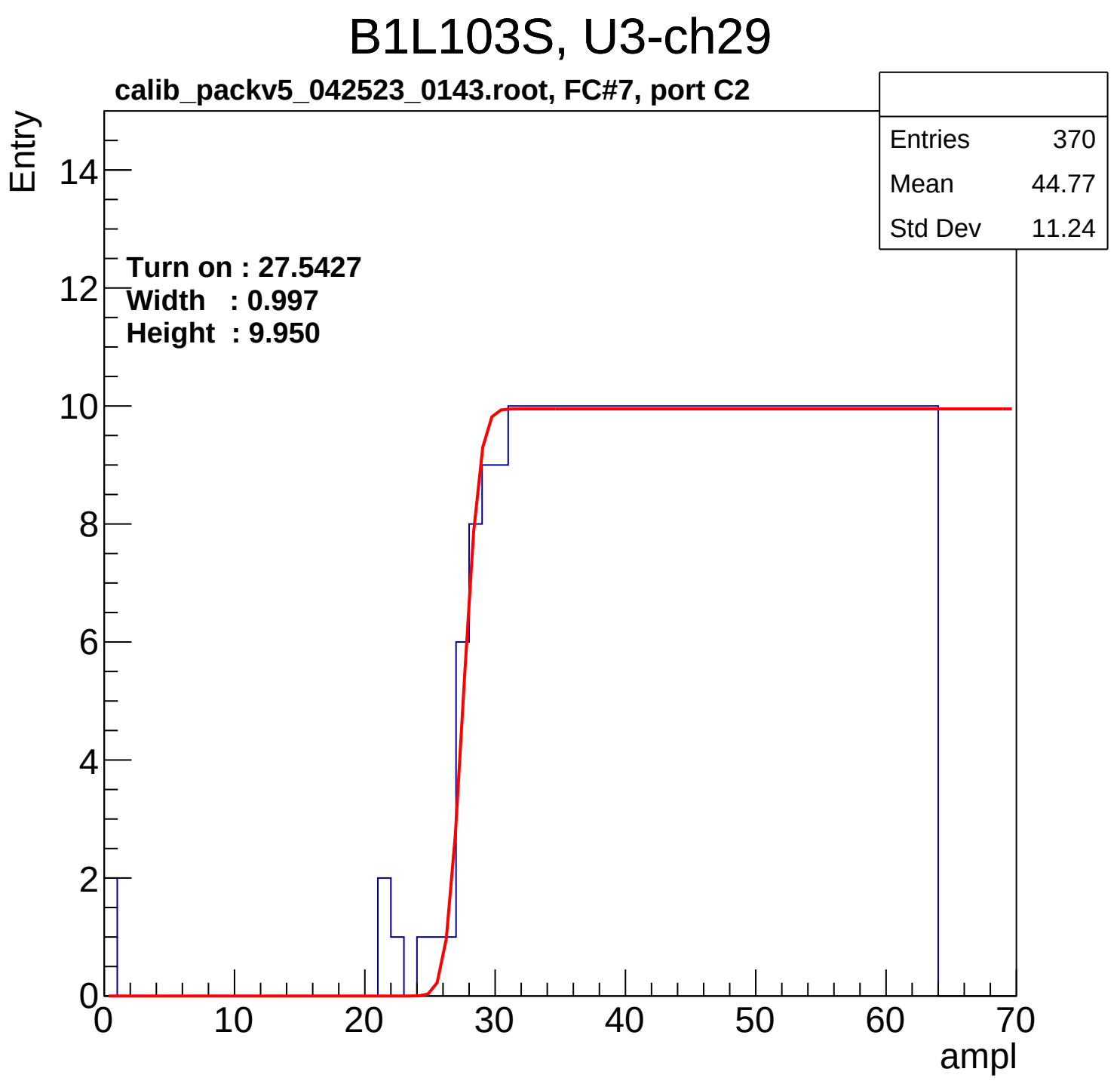
B1L103S, U3-ch29
calib_packv5_042523_0143.root, FC#7, port C2
Entries 370
Mean 44.77
Std Dev 11.24
Turn on : 27.5427
Width : 0.997
Height : 9.950
Entry
ampl
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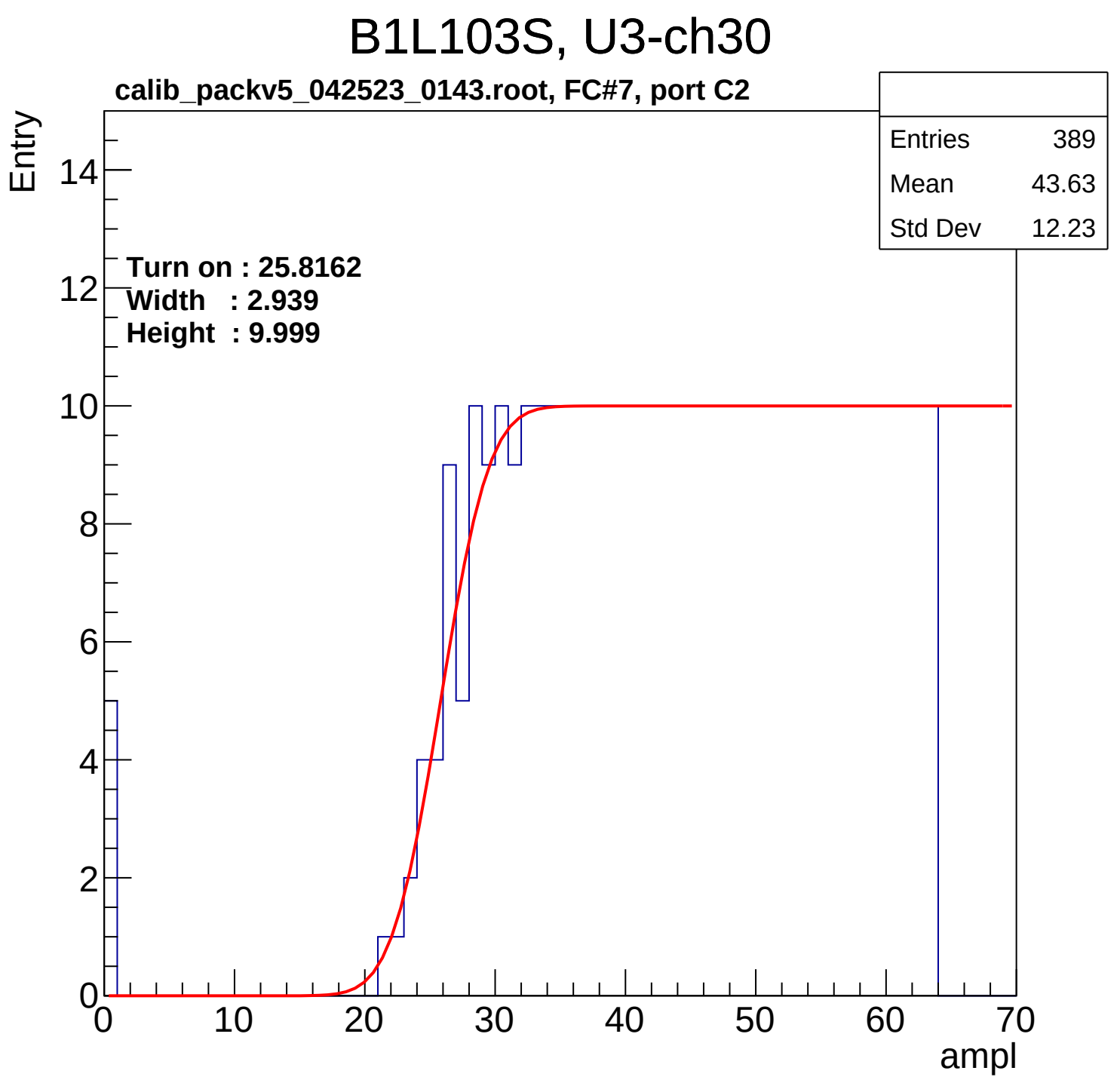
B1L103S, U3-ch30
calib_packv5_042523_0143.root, FC#7, port C2
Entries 389
Mean 43.63
Std Dev 12.23
Turn on : 25.8162
Width : 2.939
Height : 9.999
Entry
ampl
0
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6
8
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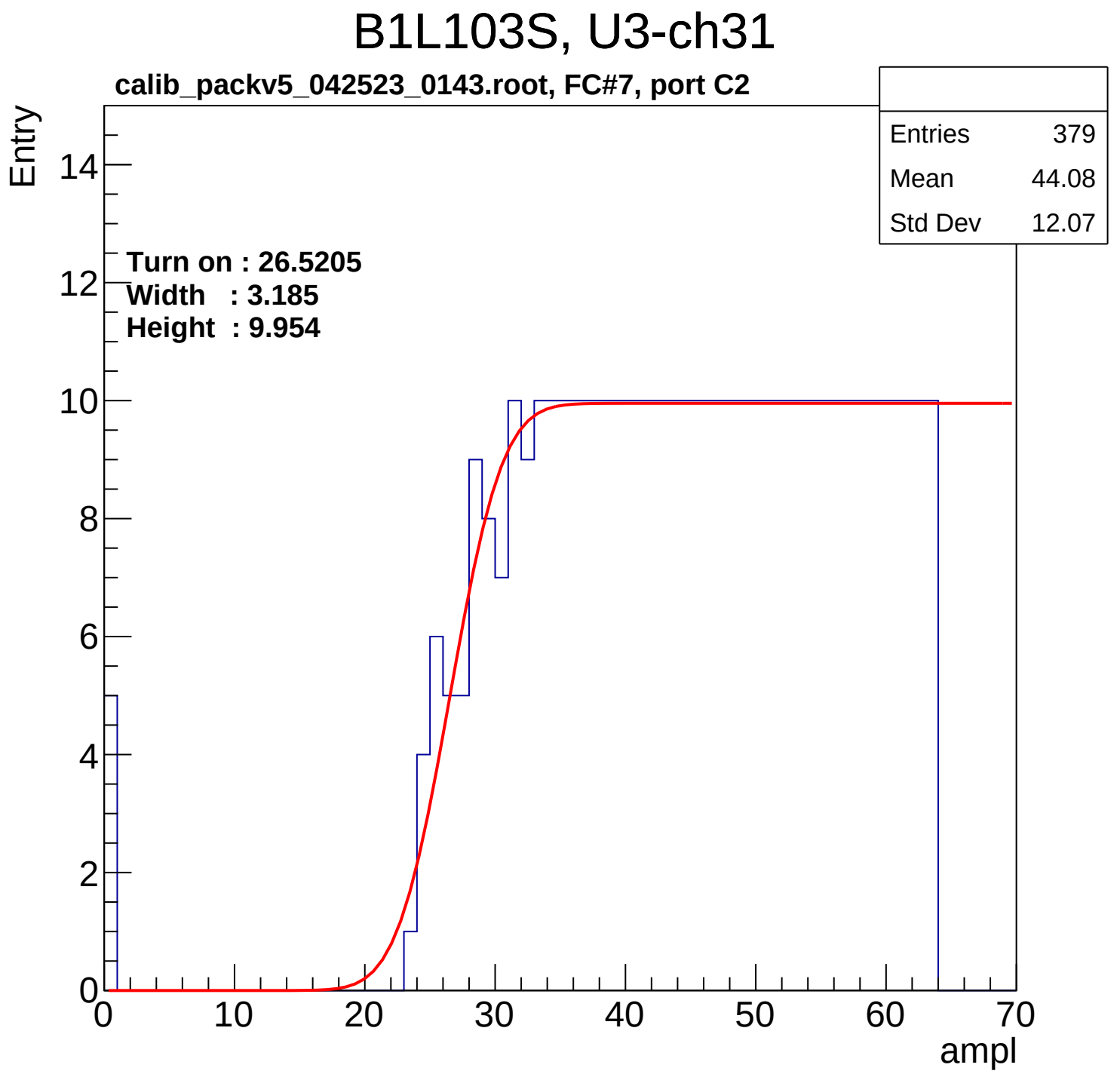
B1L103S, U3-ch31
calib_packv5_042523_0143.root, FC#7, port C2
Entries 379
Mean 44.08
Std Dev 12.07
Turn on : 26.5205
Width : 3.185
Height : 9.954
Entry
ampl
0
2
4
6
8
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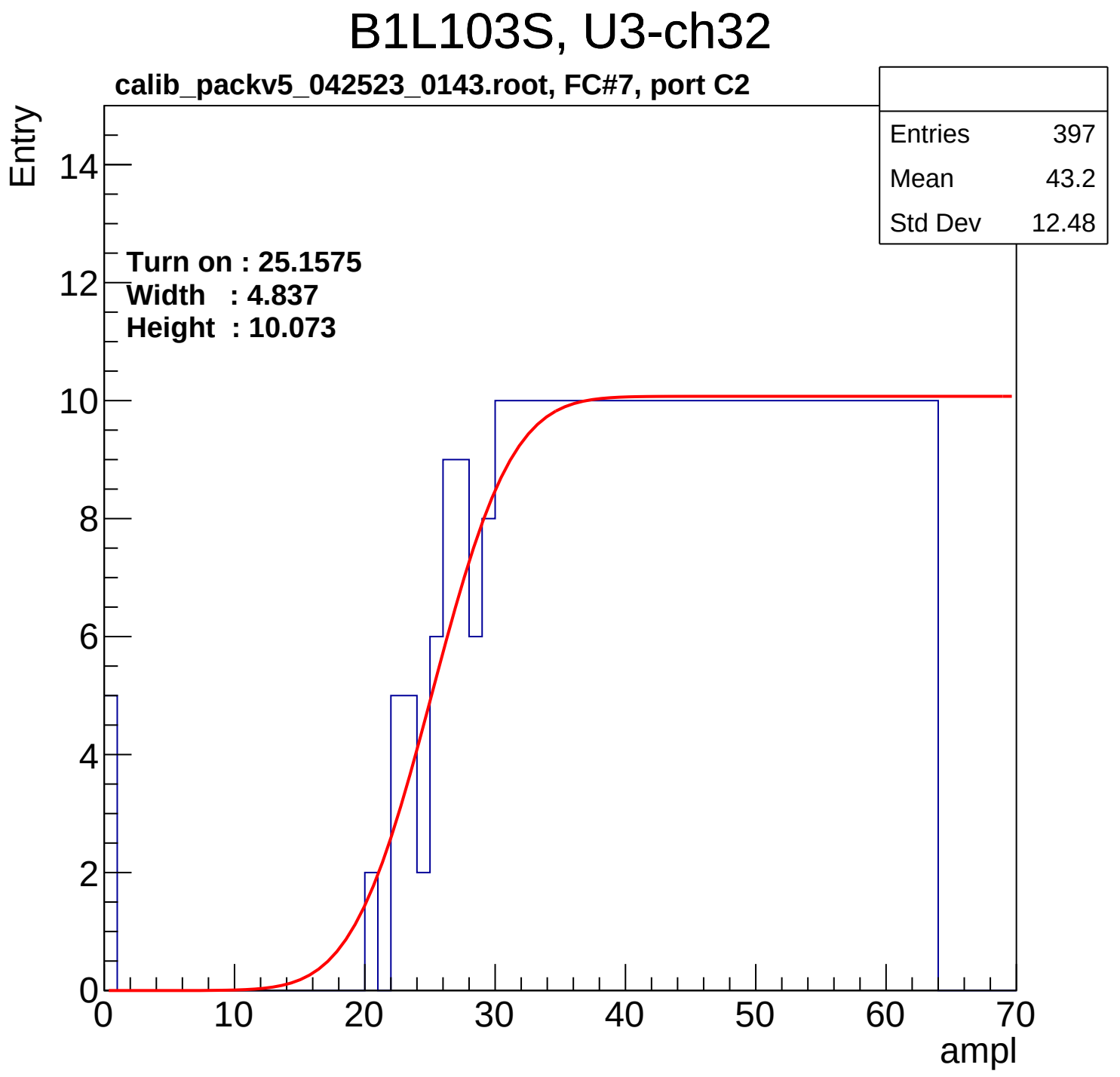
B1L103S, U3-ch32
calib_packv5_042523_0143.root, FC#7, port C2
Entries 397
Mean 43.2
Std Dev 12.48
Turn on : 25.1575
Width : 4.837
Height : 10.073
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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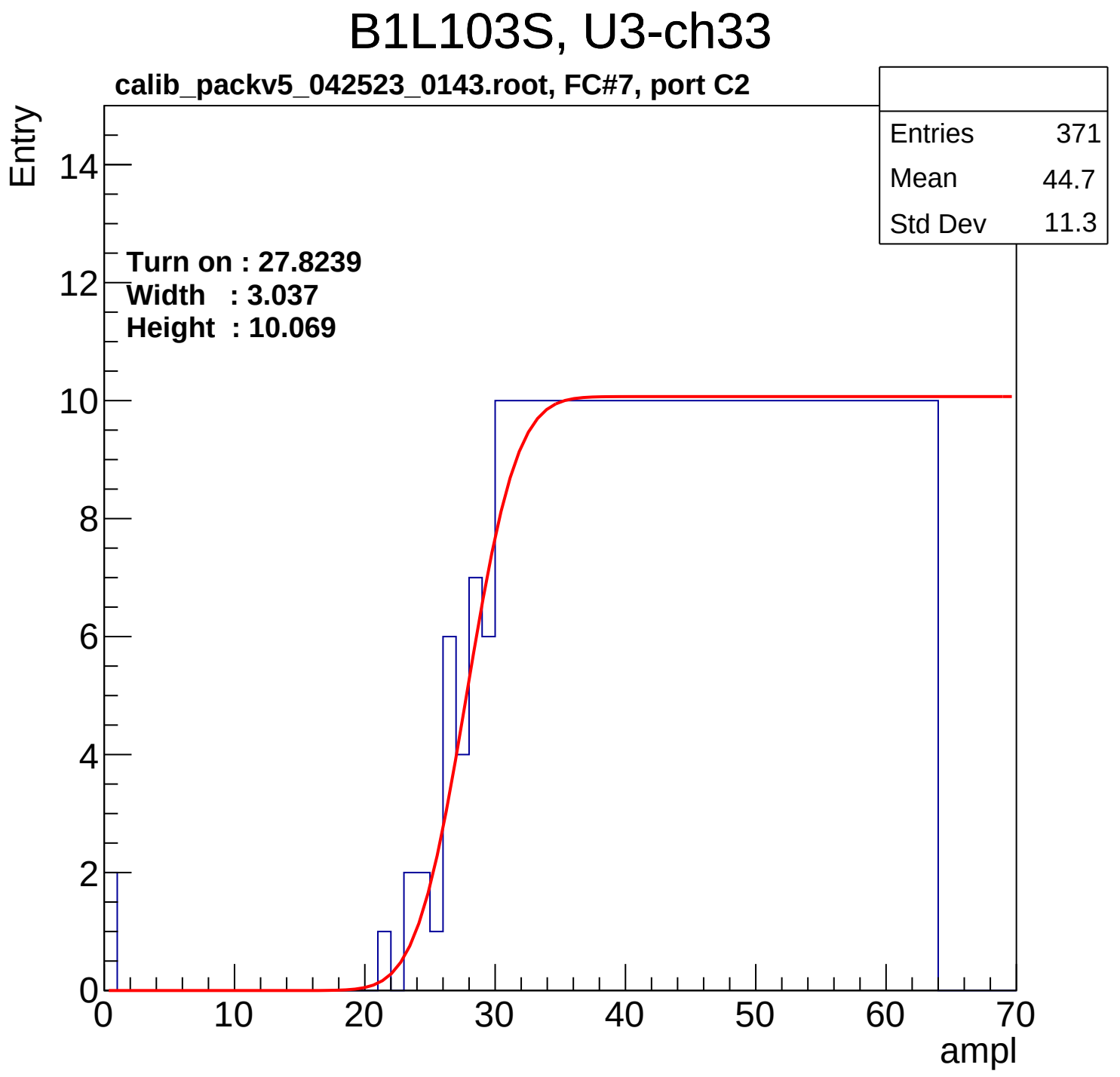
B1L103S, U3-ch33
calib_packv5_042523_0143.root, FC#7, port C2
Entries 371
Mean 44.7
Std Dev 11.3
Turn on : 27.8239
Width : 3.037
Height : 10.069
Entry
ampl
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6
8
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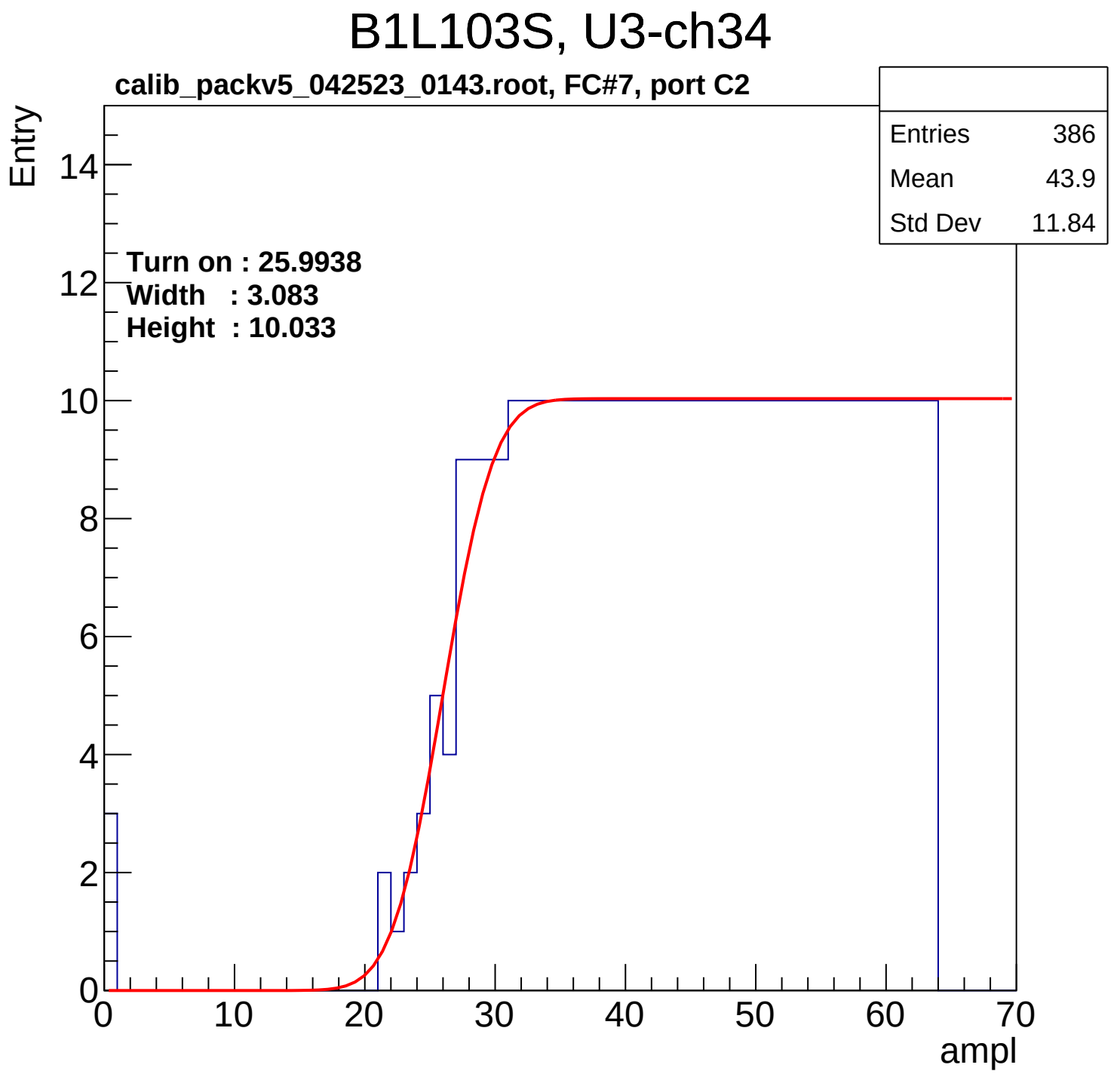
B1L103S, U3-ch34
calib_packv5_042523_0143.root, FC#7, port C2
Entries 386
Mean 43.9
Std Dev 11.84
Turn on : 25.9938
Width : 3.083
Height : 10.033
Entry
ampl
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2
4
6
8
10
12
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0
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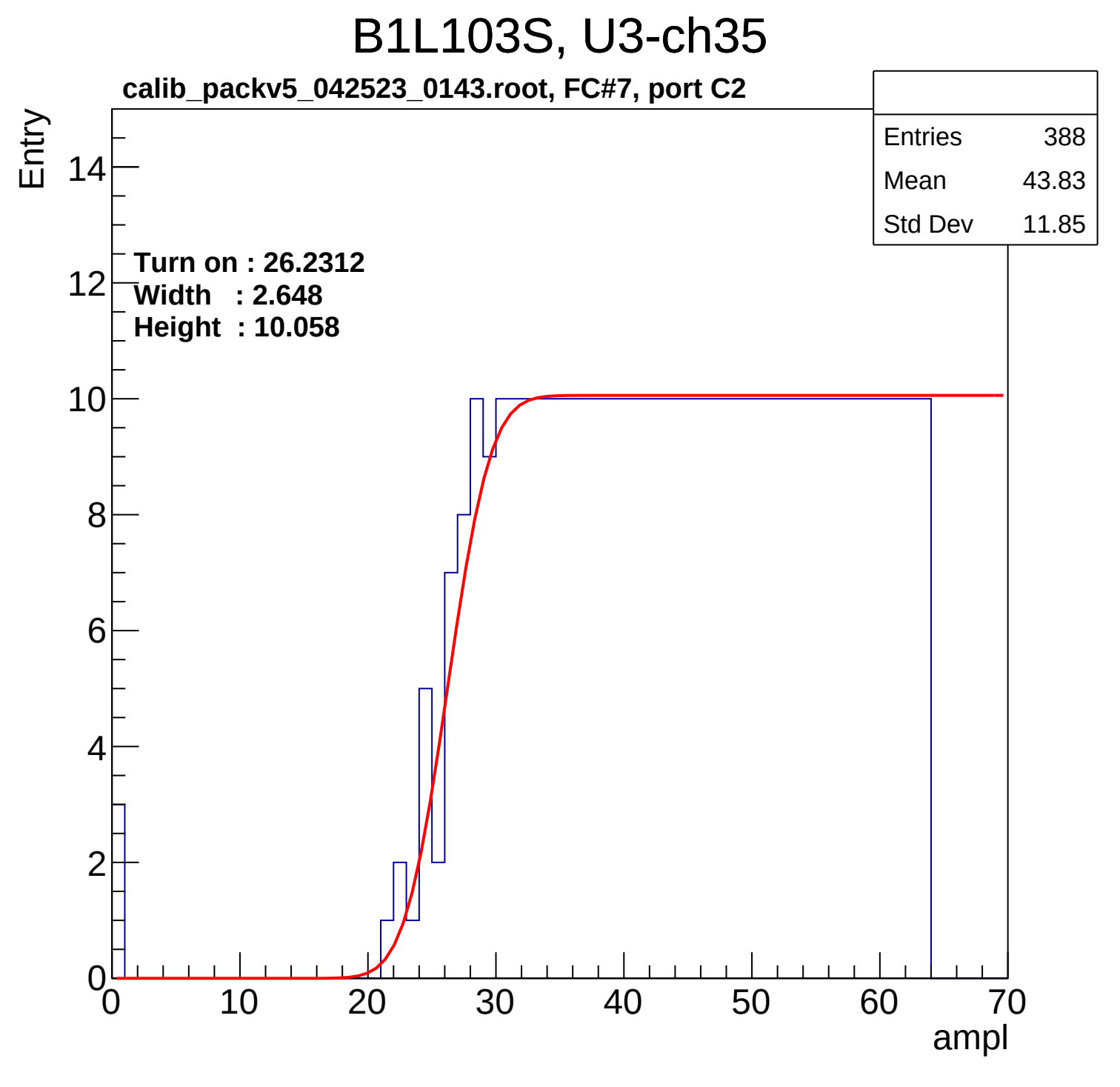
B1L103S, U3-ch35
calib_packv5_042523_0143.root, FC#7, port C2
Entries 388
Mean 43.83
Std Dev 11.85
Turn on : 26.2312
Width : 2.648
Height : 10.058
Entry
ampl
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2
4
6
8
10
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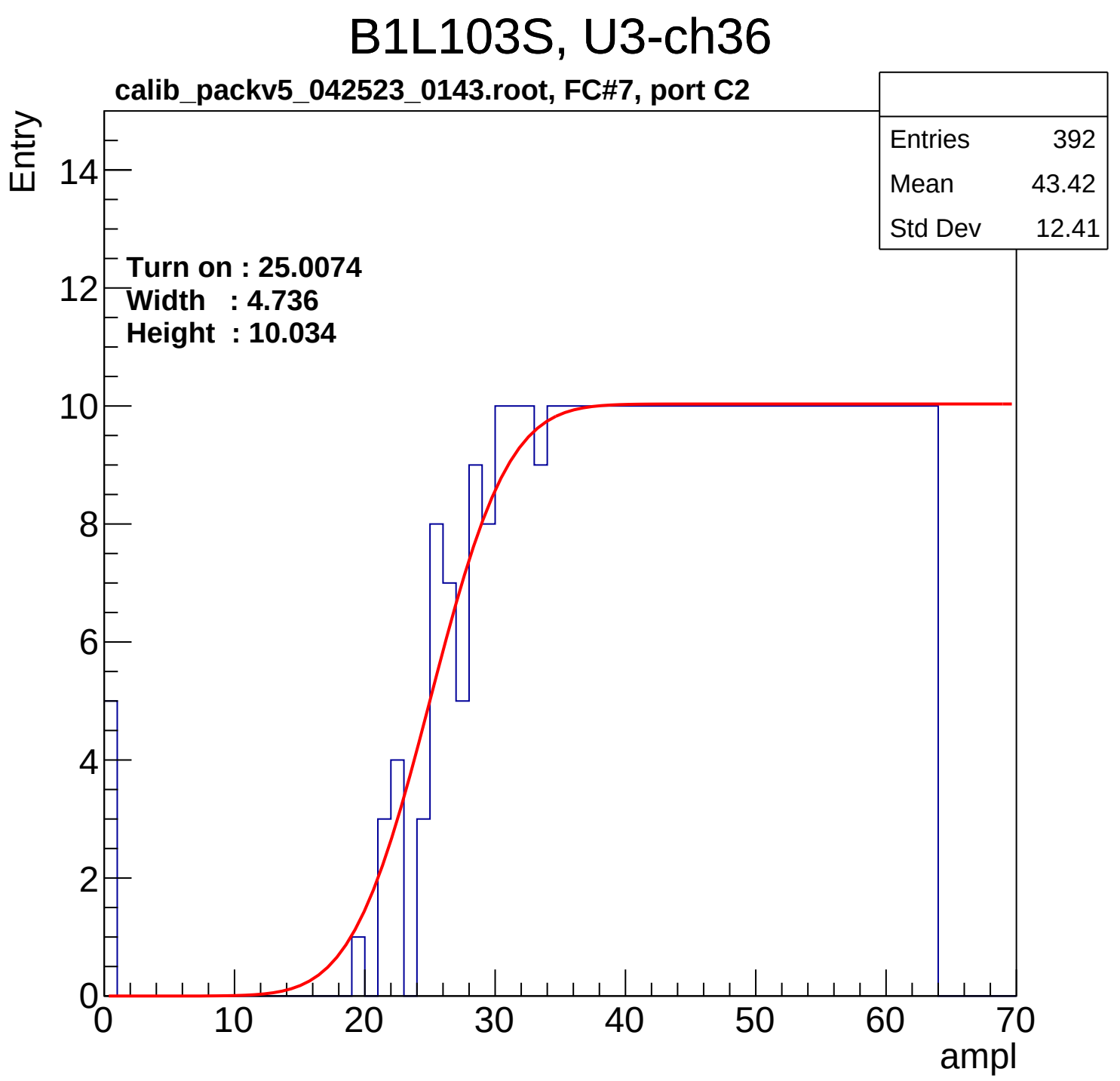
B1L103S, U3-ch36
calib_packv5_042523_0143.root, FC#7, port C2
Entries 392
Mean 43.42
Std Dev 12.41
Turn on : 25.0074
Width : 4.736
Height : 10.034
Entry
ampl
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2
4
6
8
10
12
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0
10
20
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40
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60
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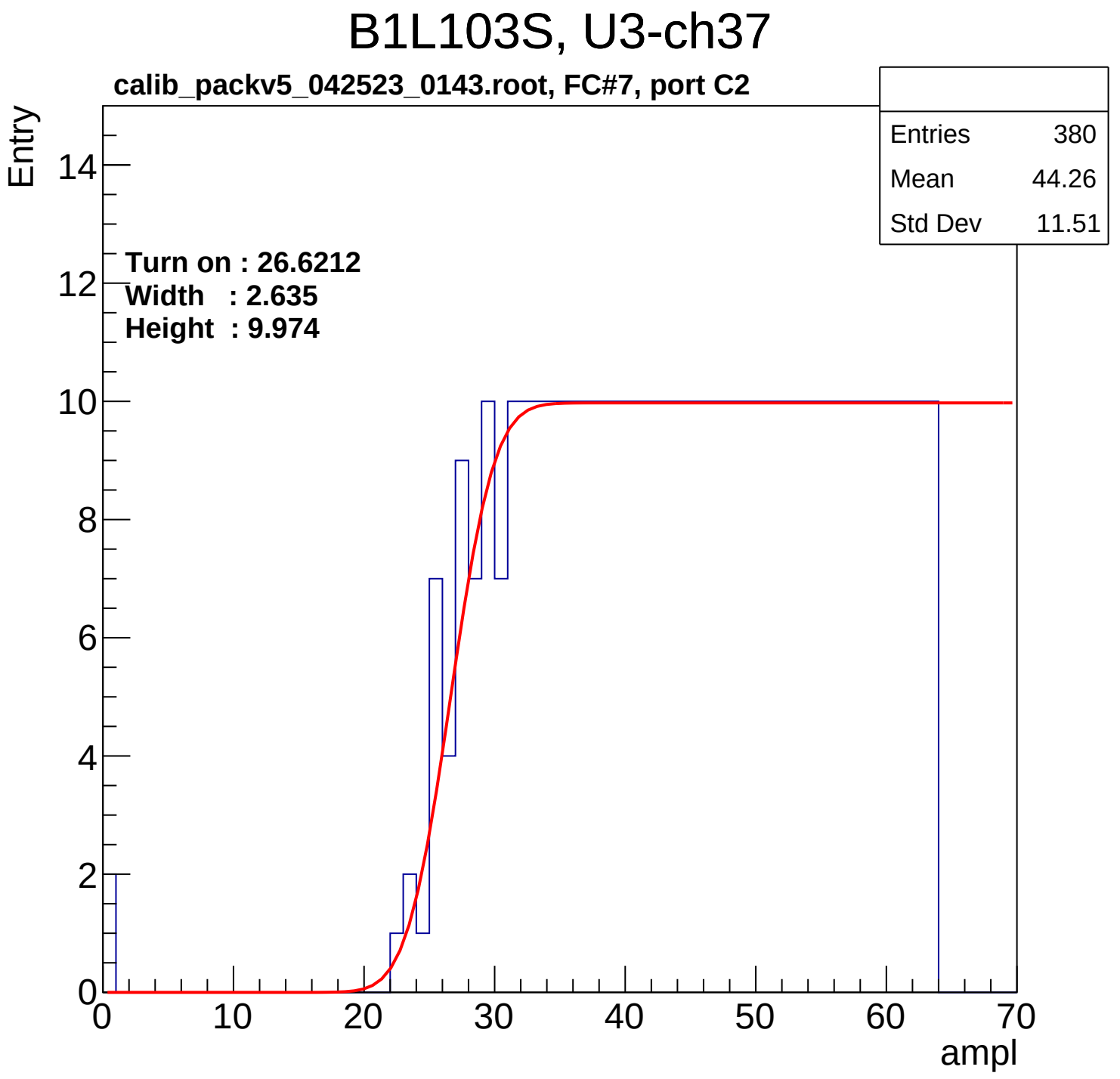
B1L103S, U3-ch37
calib_packv5_042523_0143.root, FC#7, port C2
Entries 380
Mean 44.26
Std Dev 11.51
Turn on : 26.6212
Width : 2.635
Height : 9.974
Entry
ampl
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2
4
6
8
10
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0
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20
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60
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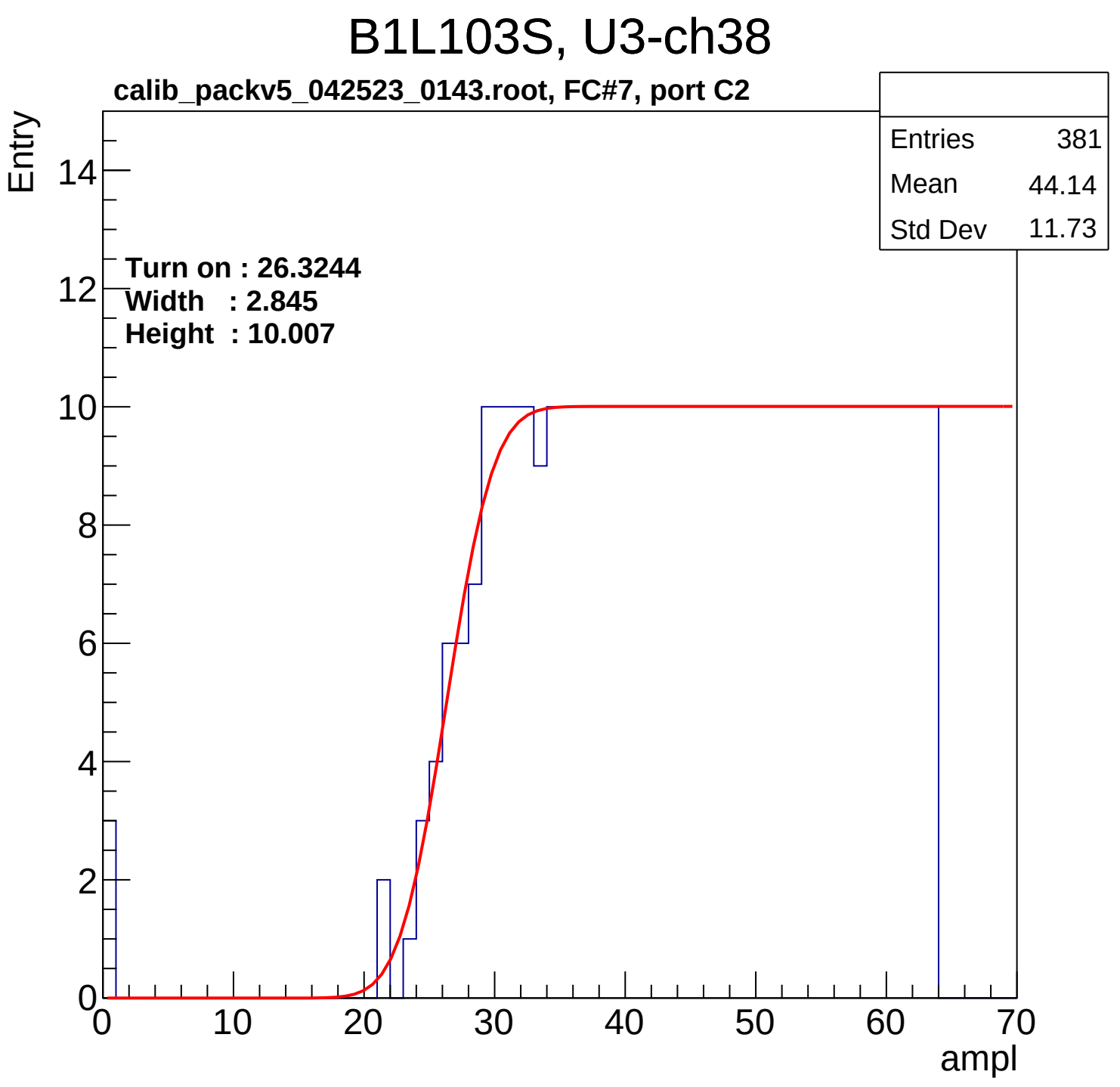
B1L103S, U3-ch38
calib_packv5_042523_0143.root, FC#7, port C2
Entries 381
Mean 44.14
Std Dev 11.73
Turn on : 26.3244
Width : 2.845
Height : 10.007
Entry
ampl
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2
4
6
8
10
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0
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60
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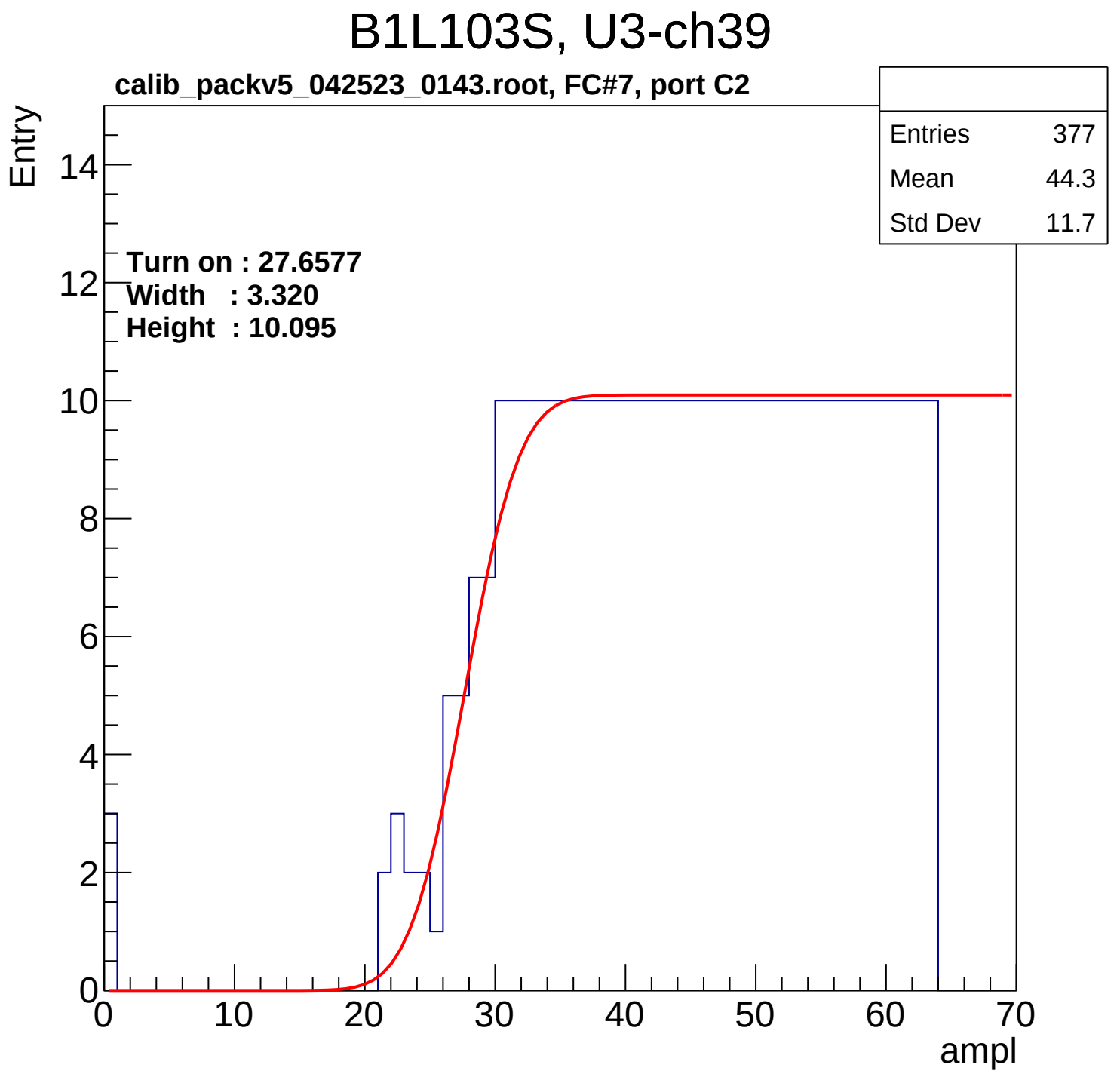
B1L103S, U3-ch39
calib_packv5_042523_0143.root, FC#7, port C2
Entries 377
Mean 44.3
Std Dev 11.7
Turn on : 27.6577
Width : 3.320
Height : 10.095
Entry
ampl
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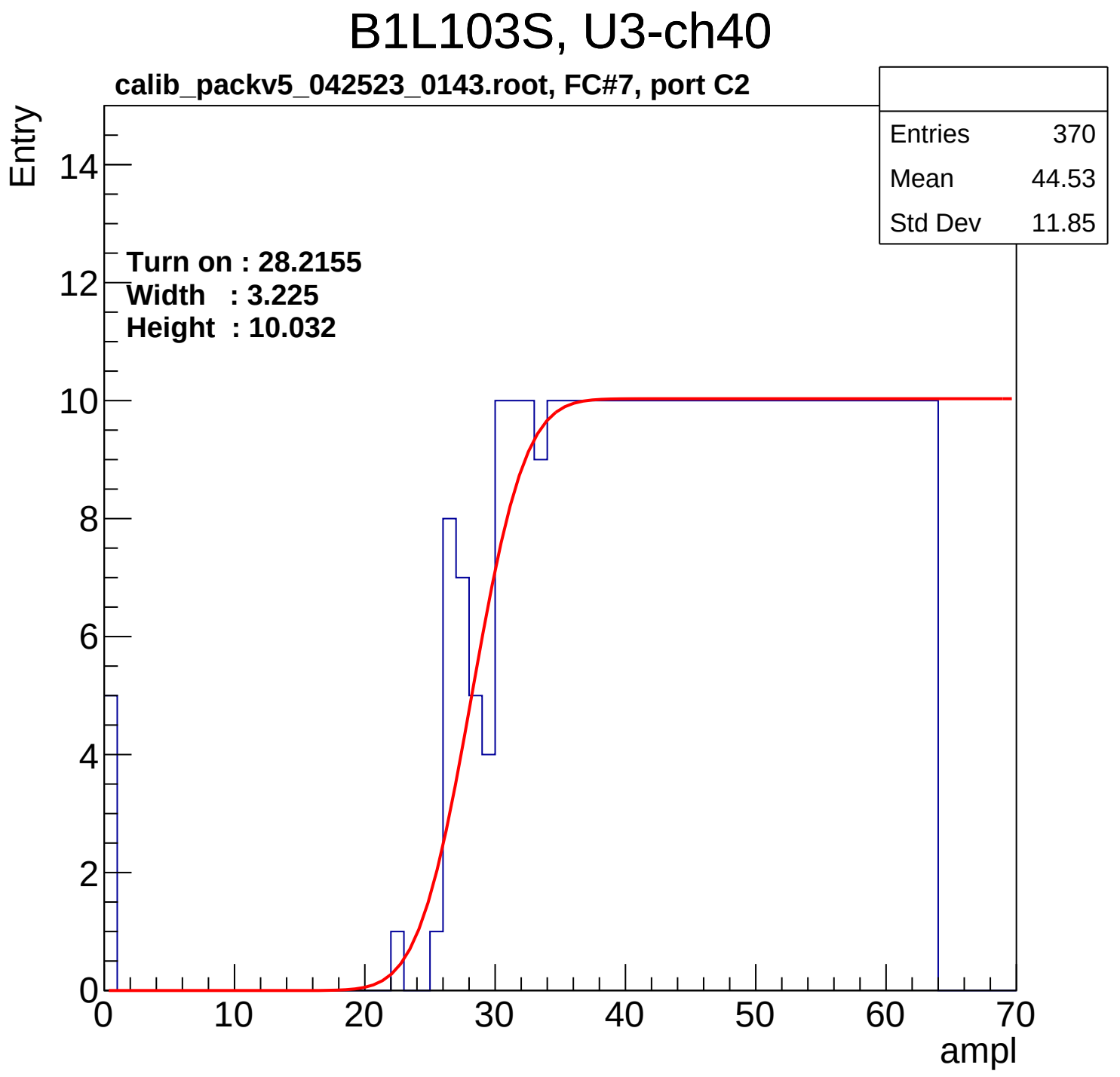
B1L103S, U3-ch40
calib_packv5_042523_0143.root, FC#7, port C2
Entries 370
Mean 44.53
Std Dev 11.85
Turn on : 28.2155
Width : 3.225
Height : 10.032
Entry
ampl
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2
4
6
8
10
12
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0
10
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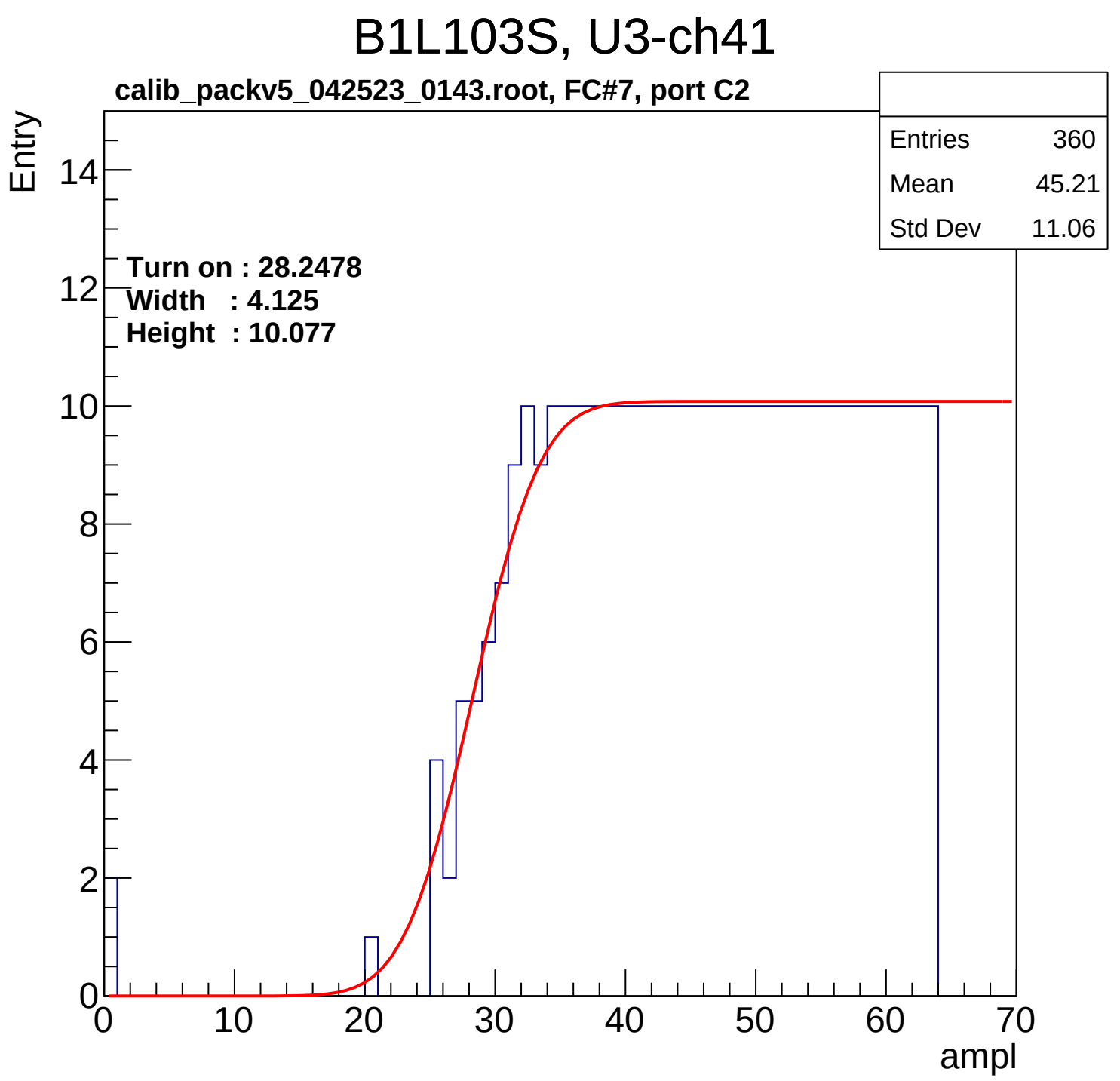
B1L103S, U3-ch41
calib_packv5_042523_0143.root, FC#7, port C2
Entries 360
Mean 45.21
Std Dev 11.06
Turn on : 28.2478
Width : 4.125
Height : 10.077
Entry
ampl
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2
4
6
8
10
12
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0
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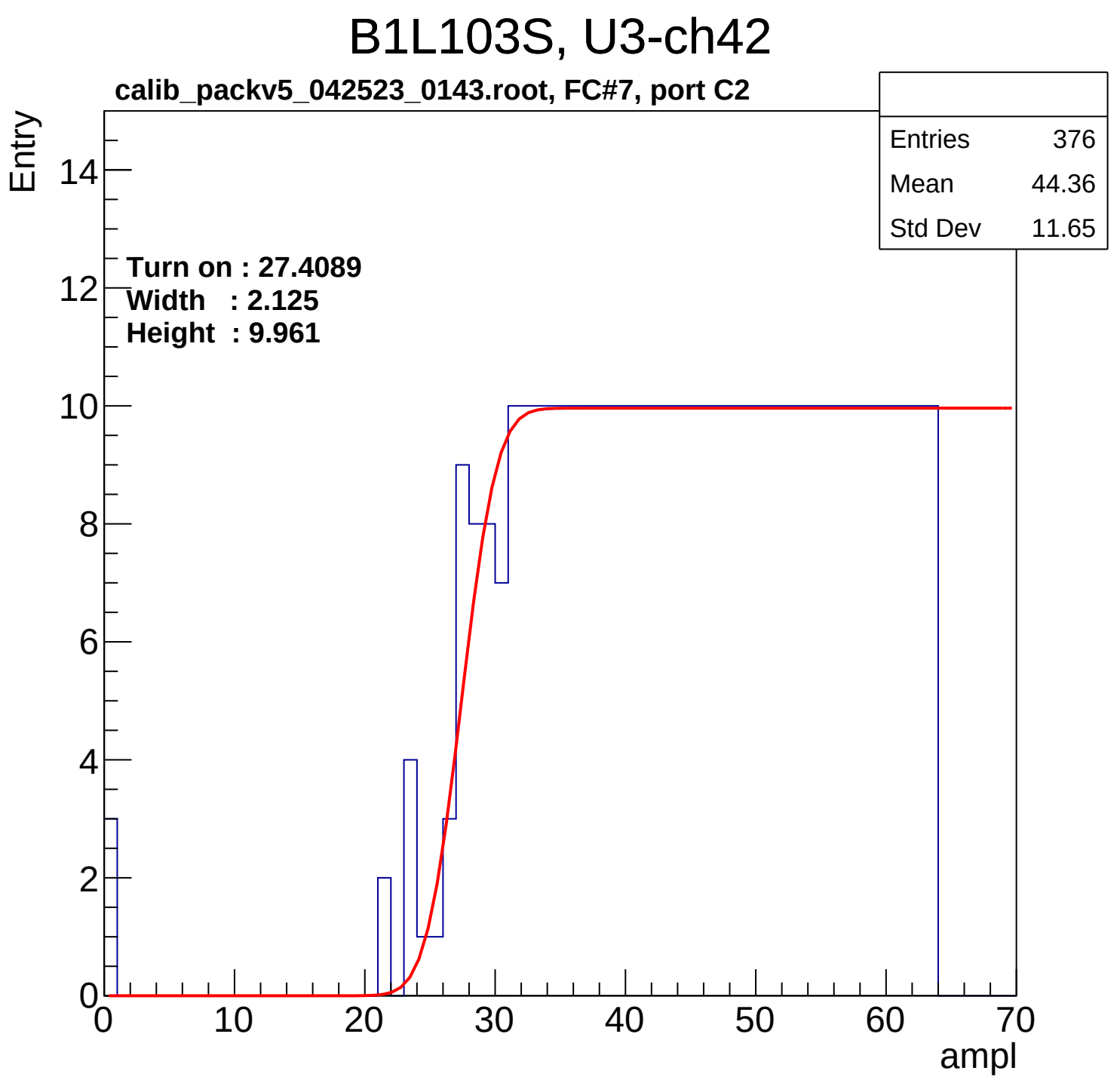
B1L103S, U3-ch42
calib_packv5_042523_0143.root, FC#7, port C2
Entries 376
Mean 44.36
Std Dev 11.65
Turn on : 27.4089
Width : 2.125
Height : 9.961
Entry
ampl
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2
4
6
8
10
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0
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20
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60
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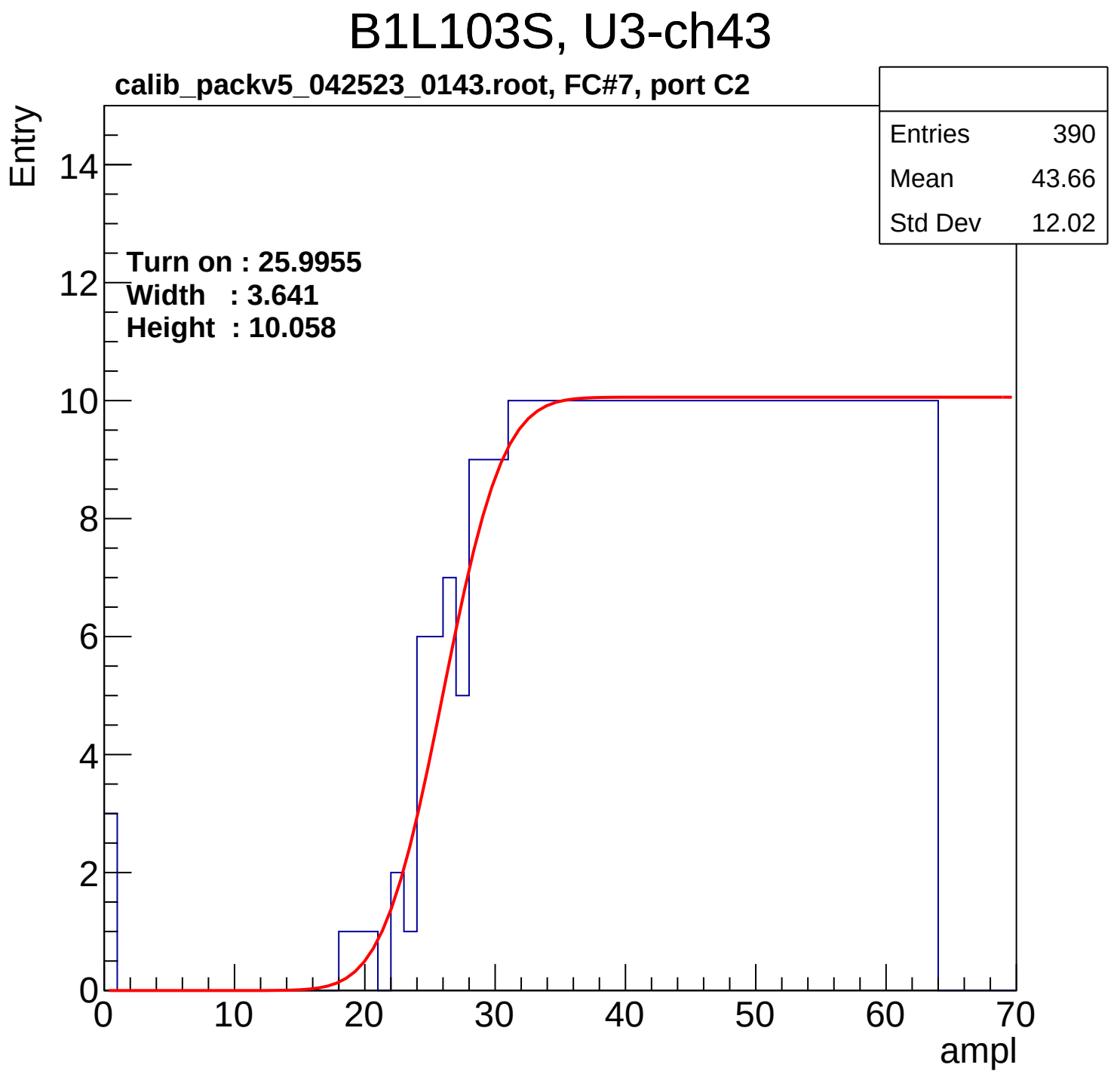
B1L103S, U3-ch43
calib_packv5_042523_0143.root, FC#7, port C2
Entries 390
Mean 43.66
Std Dev 12.02
Turn on : 25.9955
Width : 3.641
Height : 10.058
Entry
ampl
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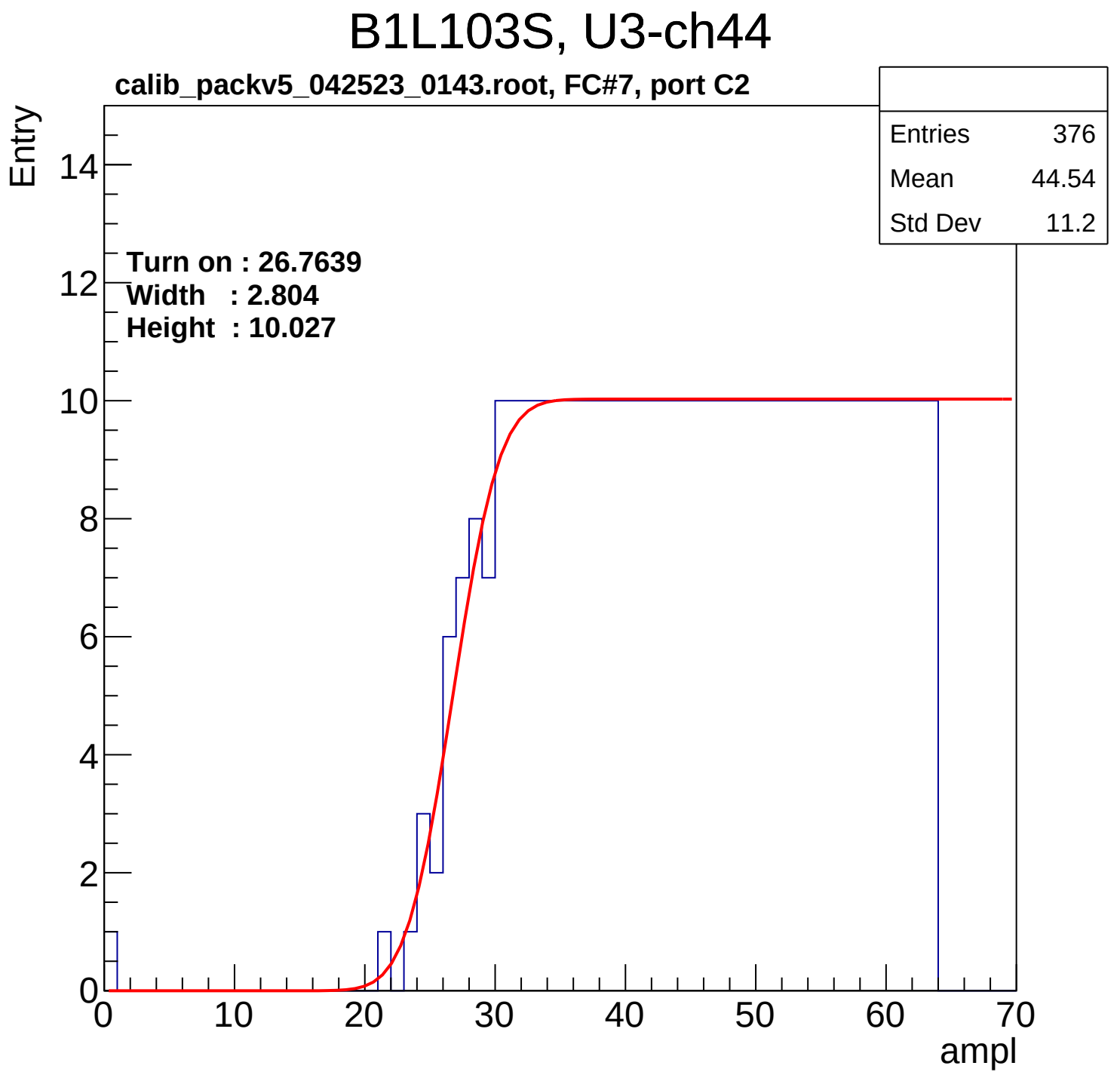
B1L103S, U3-ch44
calib_packv5_042523_0143.root, FC#7, port C2
Entries 376
Mean 44.54
Std Dev 11.2
Turn on : 26.7639
Width : 2.804
Height : 10.027
Entry
ampl
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6
8
10
12
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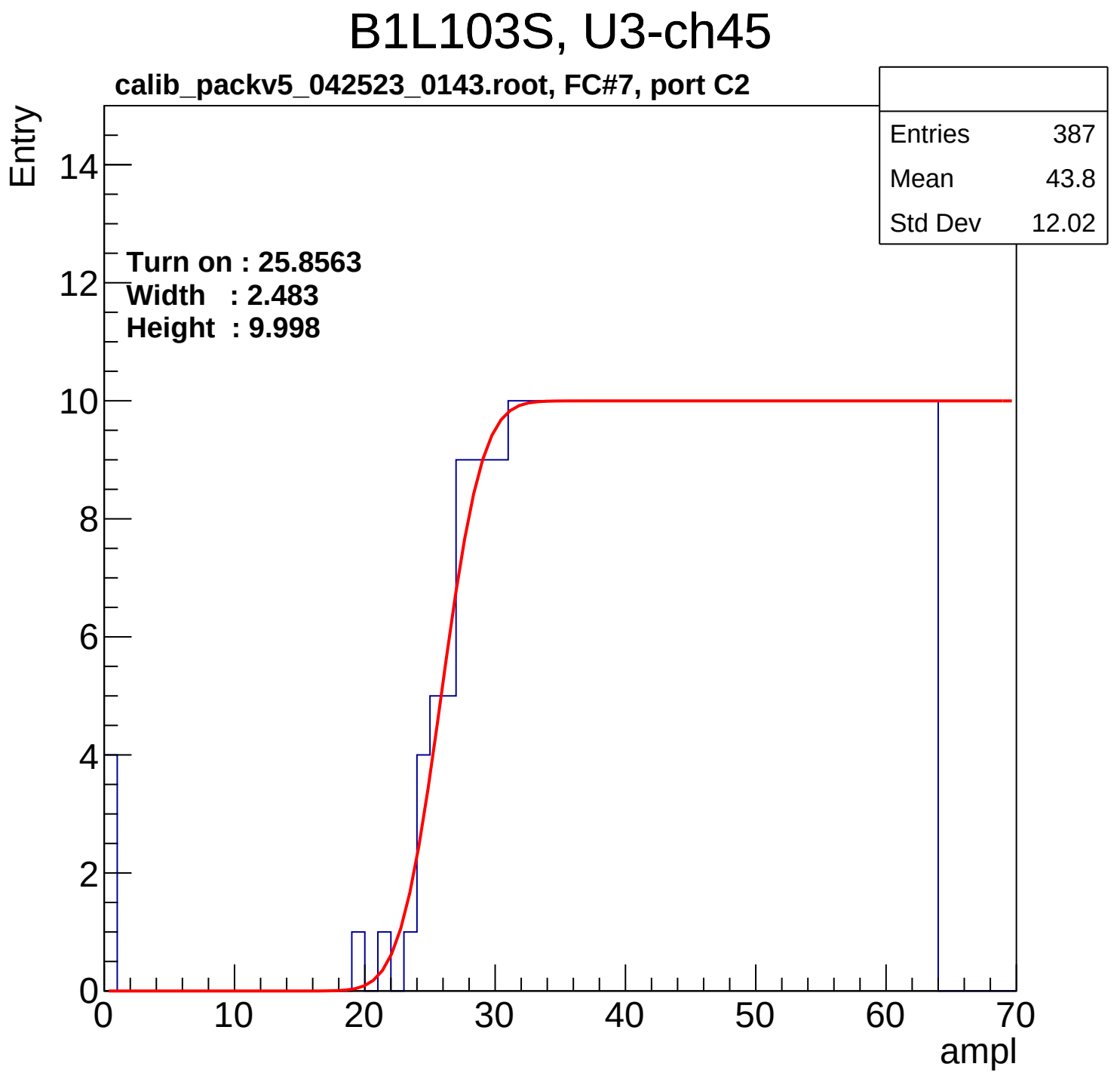
B1L103S, U3-ch45
calib_packv5_042523_0143.root, FC#7, port C2
Entries 387
Mean 43.8
Std Dev 12.02
Turn on : 25.8563
Width : 2.483
Height : 9.998
Entry
ampl
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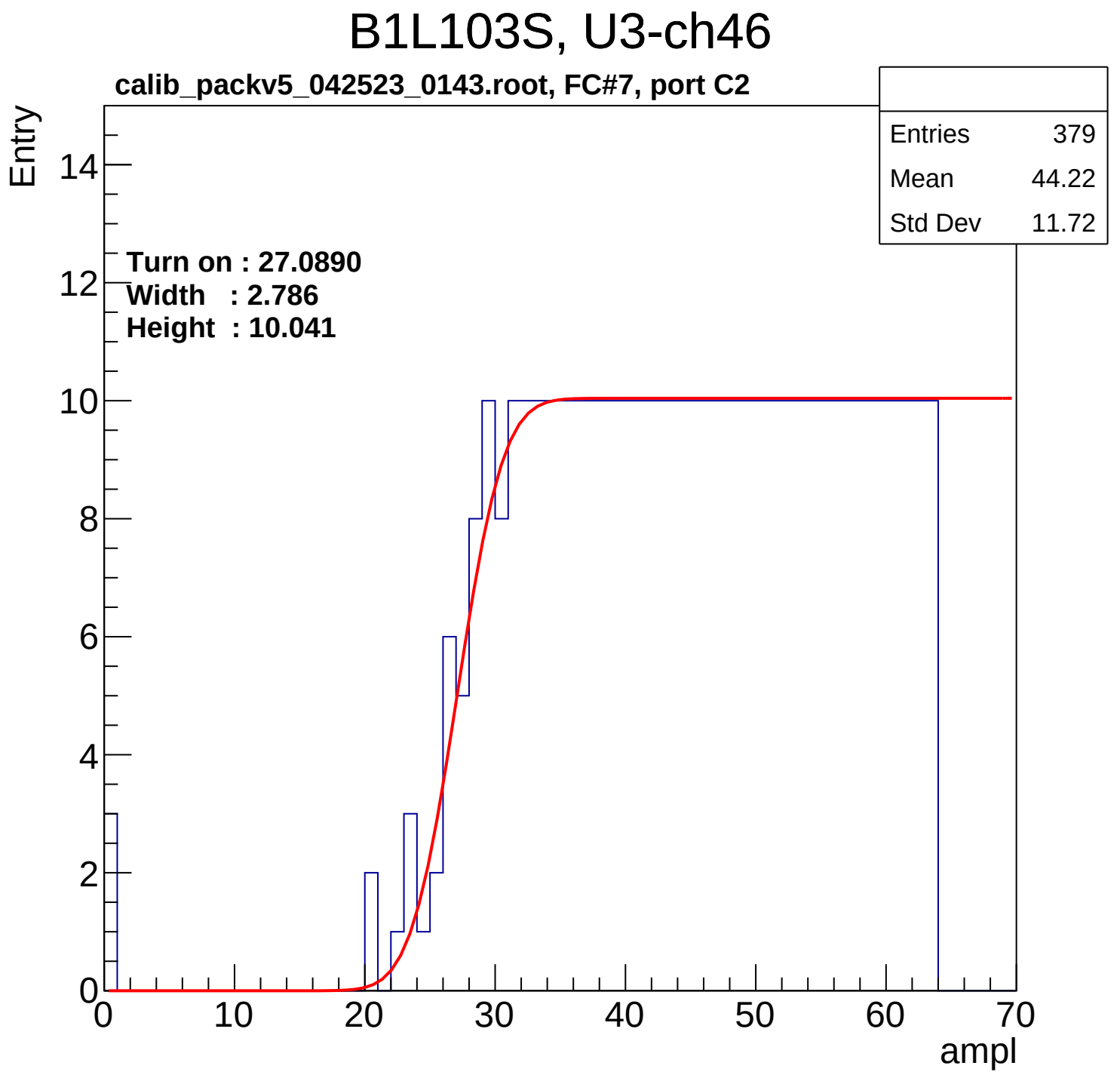
B1L103S, U3-ch46
calib_packv5_042523_0143.root, FC#7, port C2
Entries 379
Mean 44.22
Std Dev 11.72
Turn on : 27.0890
Width : 2.786
Height : 10.041
Entry
ampl
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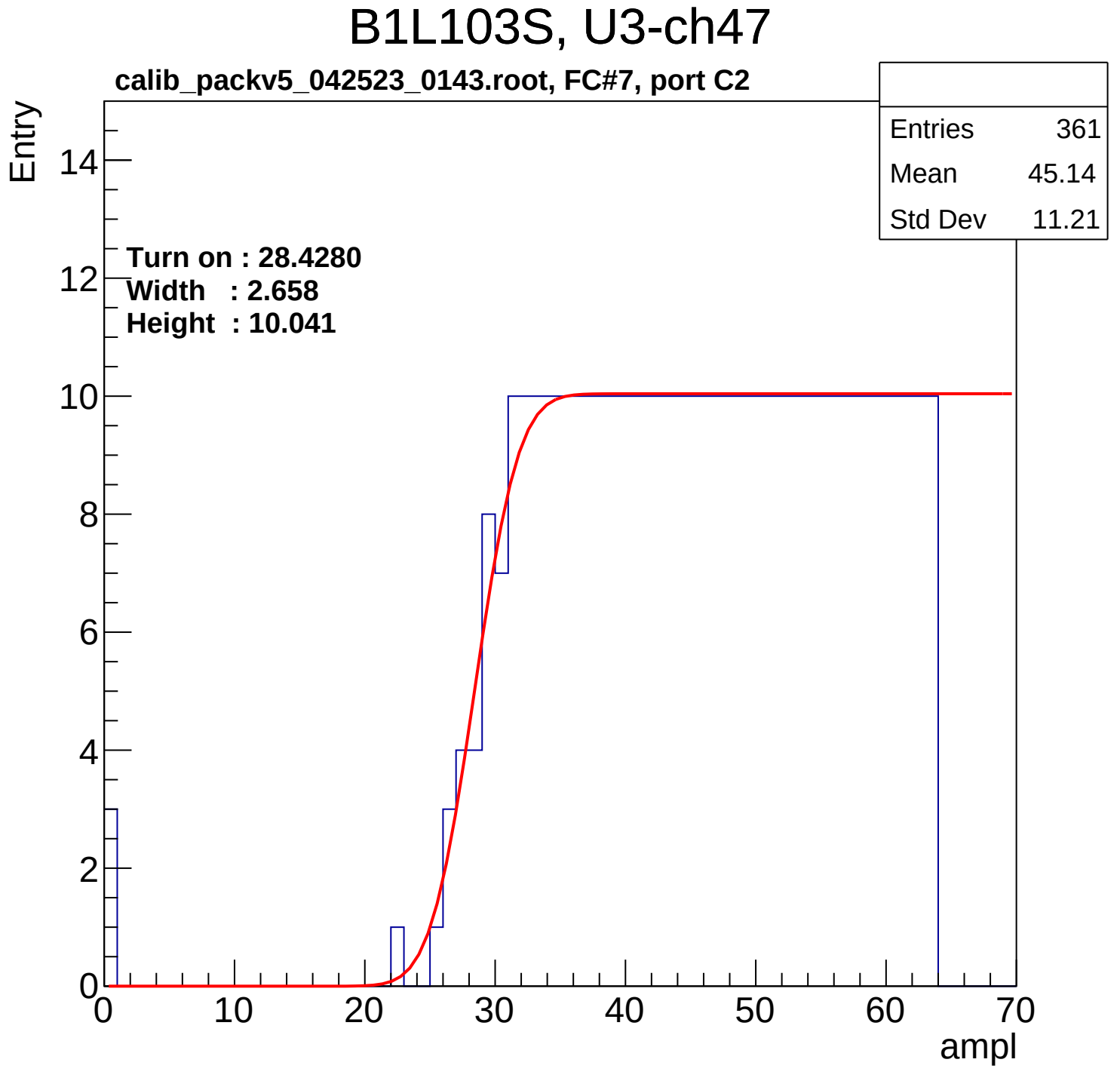
B1L103S, U3-ch47
calib_packv5_042523_0143.root, FC#7, port C2
Entries 361
Mean 45.14
Std Dev 11.21
Turn on : 28.4280
Width : 2.658
Height : 10.041
Entry
ampl
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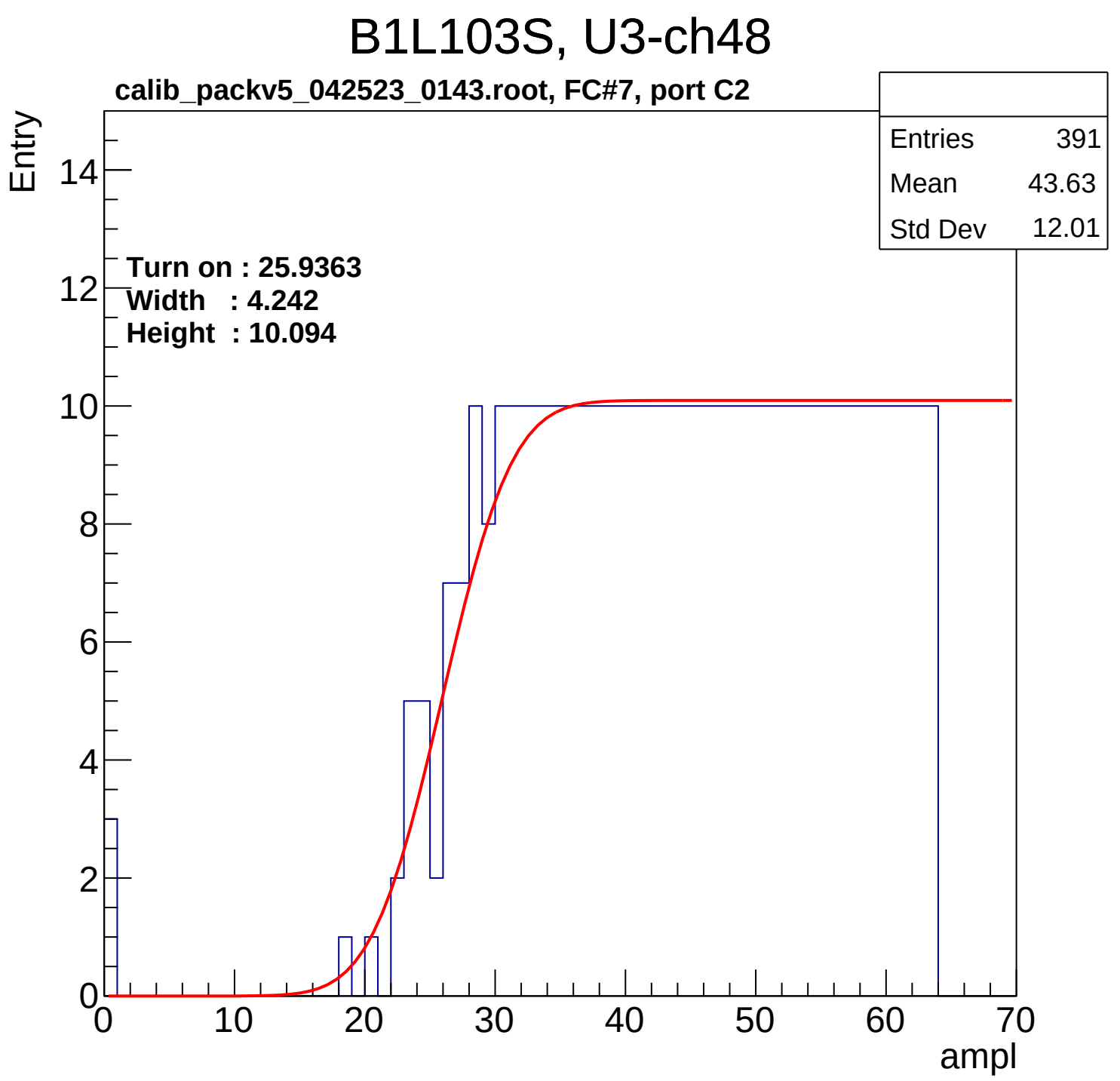
B1L103S, U3-ch48
calib_packv5_042523_0143.root, FC#7, port C2
Entries 391
Mean 43.63
Std Dev 12.01
Turn on : 25.9363
Width : 4.242
Height : 10.094
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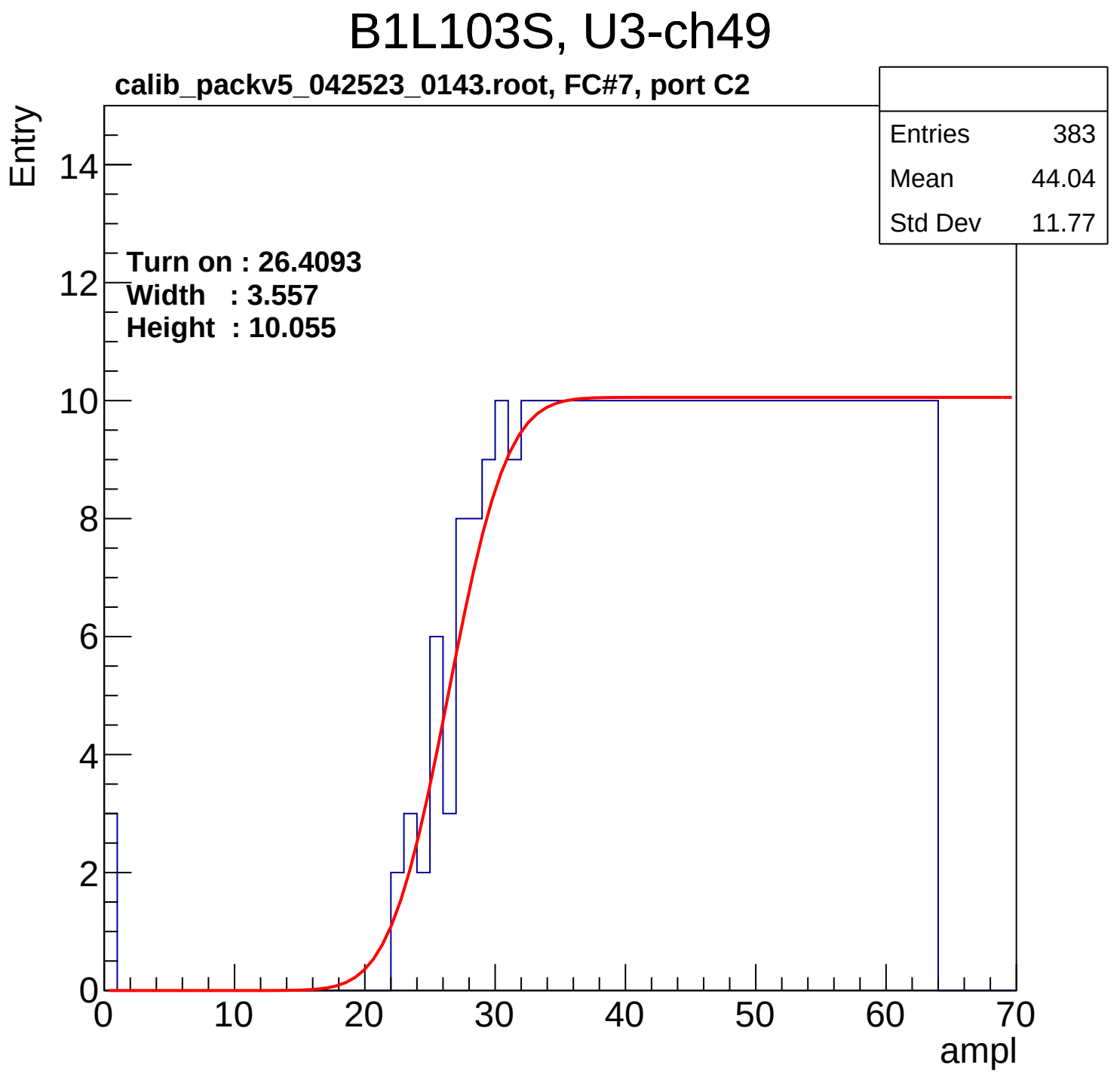
B1L103S, U3-ch49
calib_packv5_042523_0143.root, FC#7, port C2
Entries 383
Mean 44.04
Std Dev 11.77
Turn on : 26.4093
Width : 3.557
Height : 10.055
Entry
ampl
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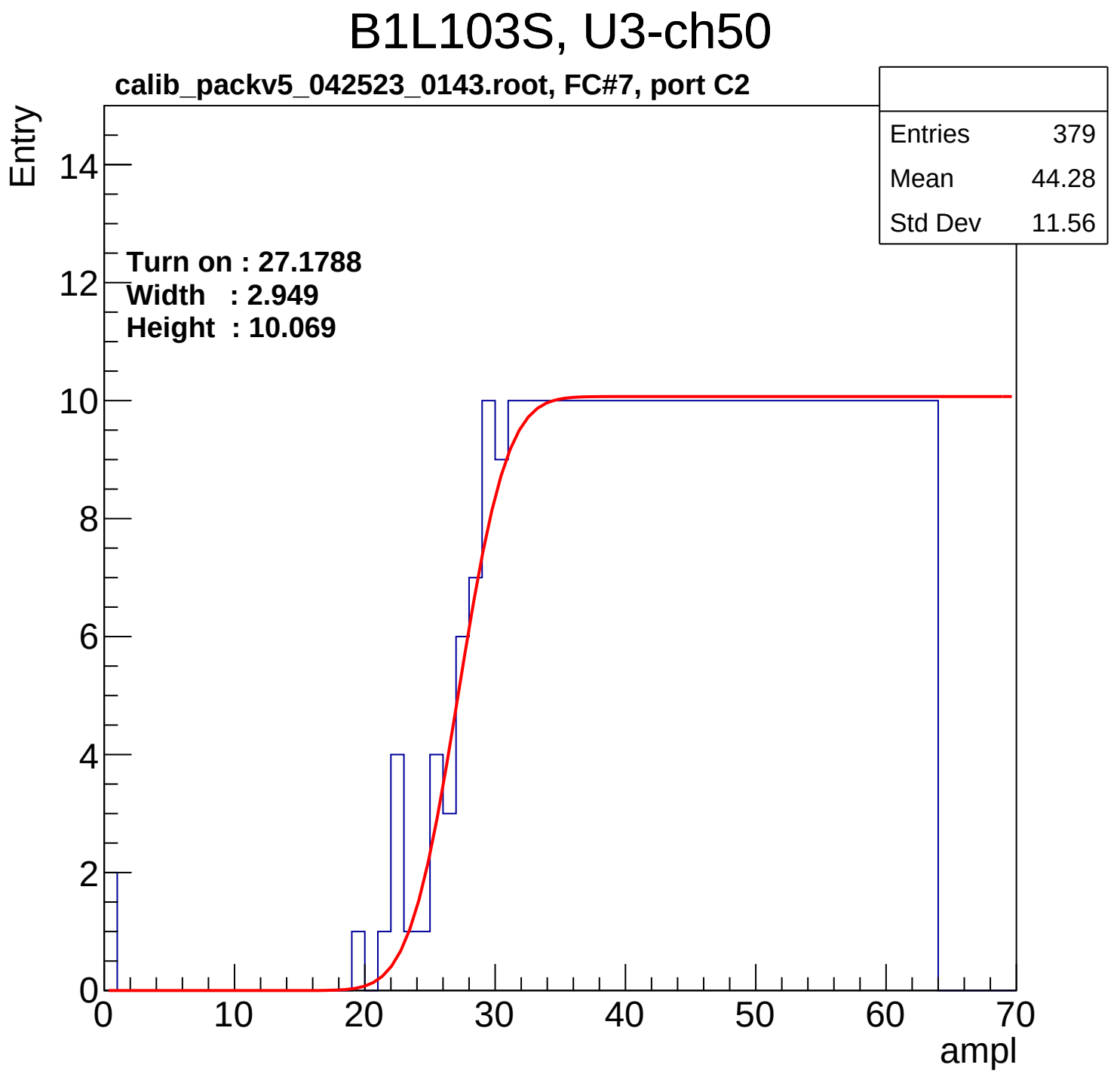
B1L103S, U3-ch50
calib_packv5_042523_0143.root, FC#7, port C2
Entries 379
Mean 44.28
Std Dev 11.56
Turn on : 27.1788
Width : 2.949
Height : 10.069
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ampl
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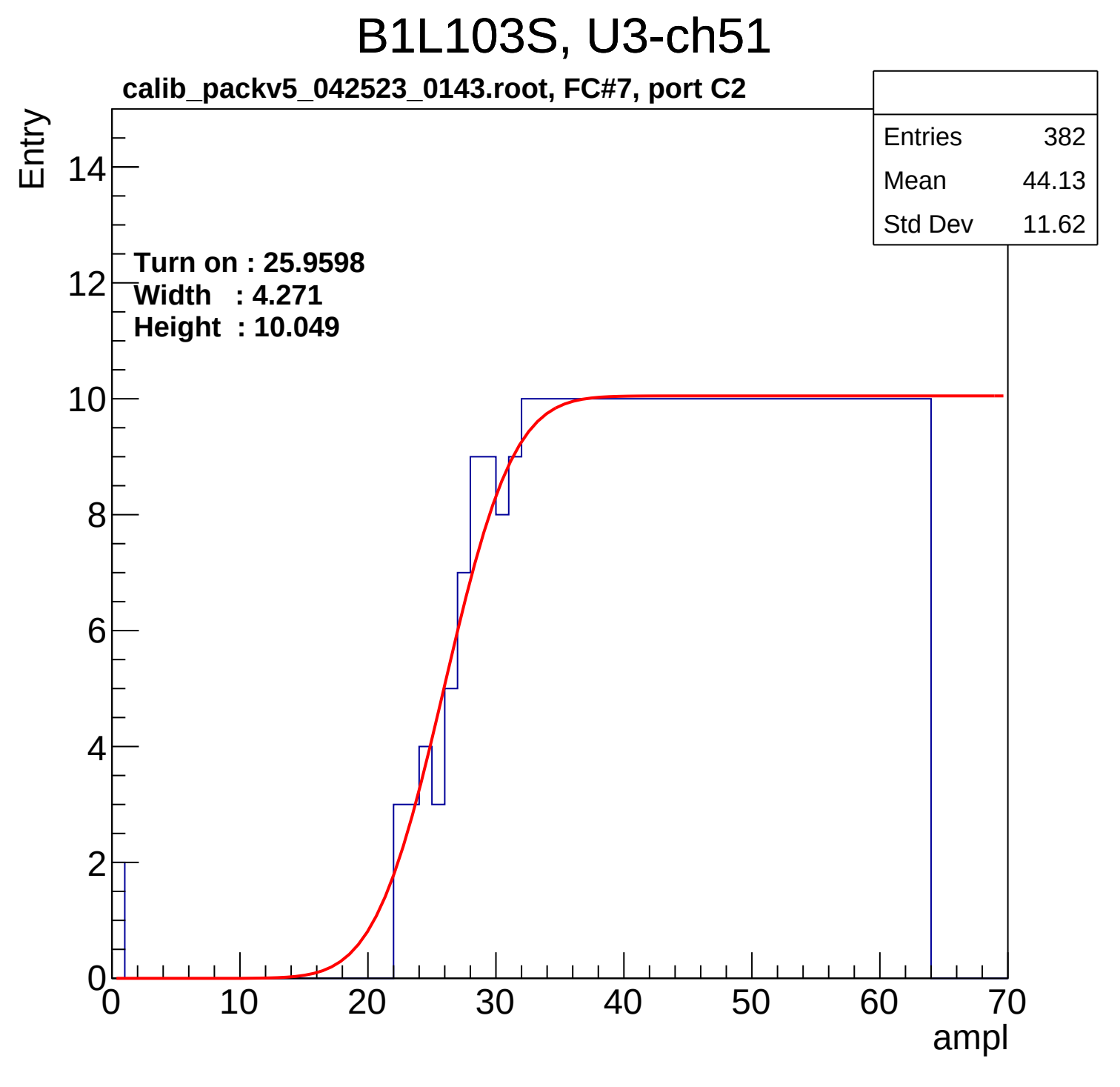
B1L103S, U3-ch51
calib_packv5_042523_0143.root, FC#7, port C2
Entries 382
Mean 44.13
Std Dev 11.62
Turn on : 25.9598
Width : 4.271
Height : 10.049
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ampl
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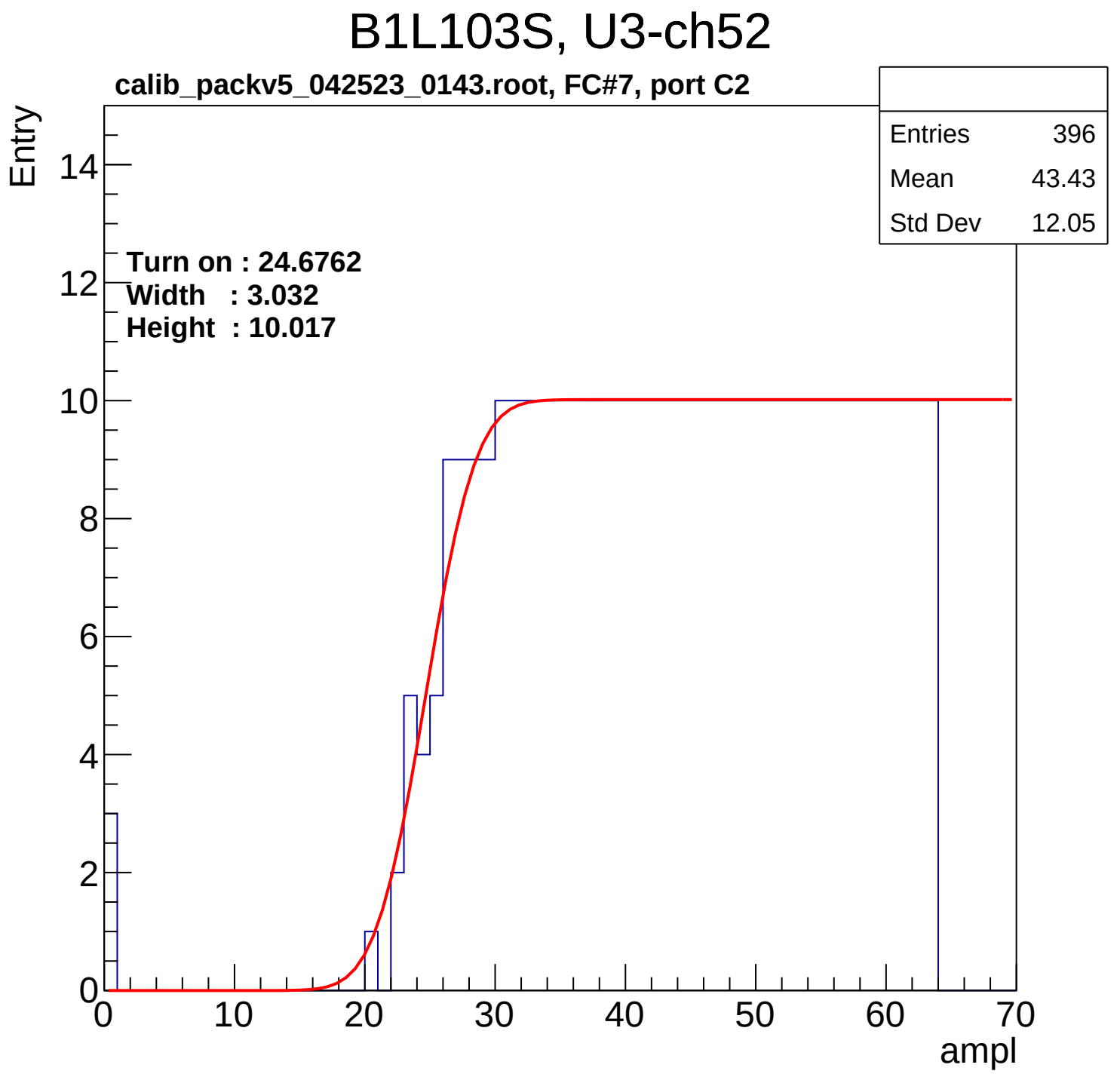
B1L103S, U3-ch52
calib_packv5_042523_0143.root, FC#7, port C2
Entries 396
Mean 43.43
Std Dev 12.05
Turn on : 24.6762
Width : 3.032
Height : 10.017
Entry
ampl
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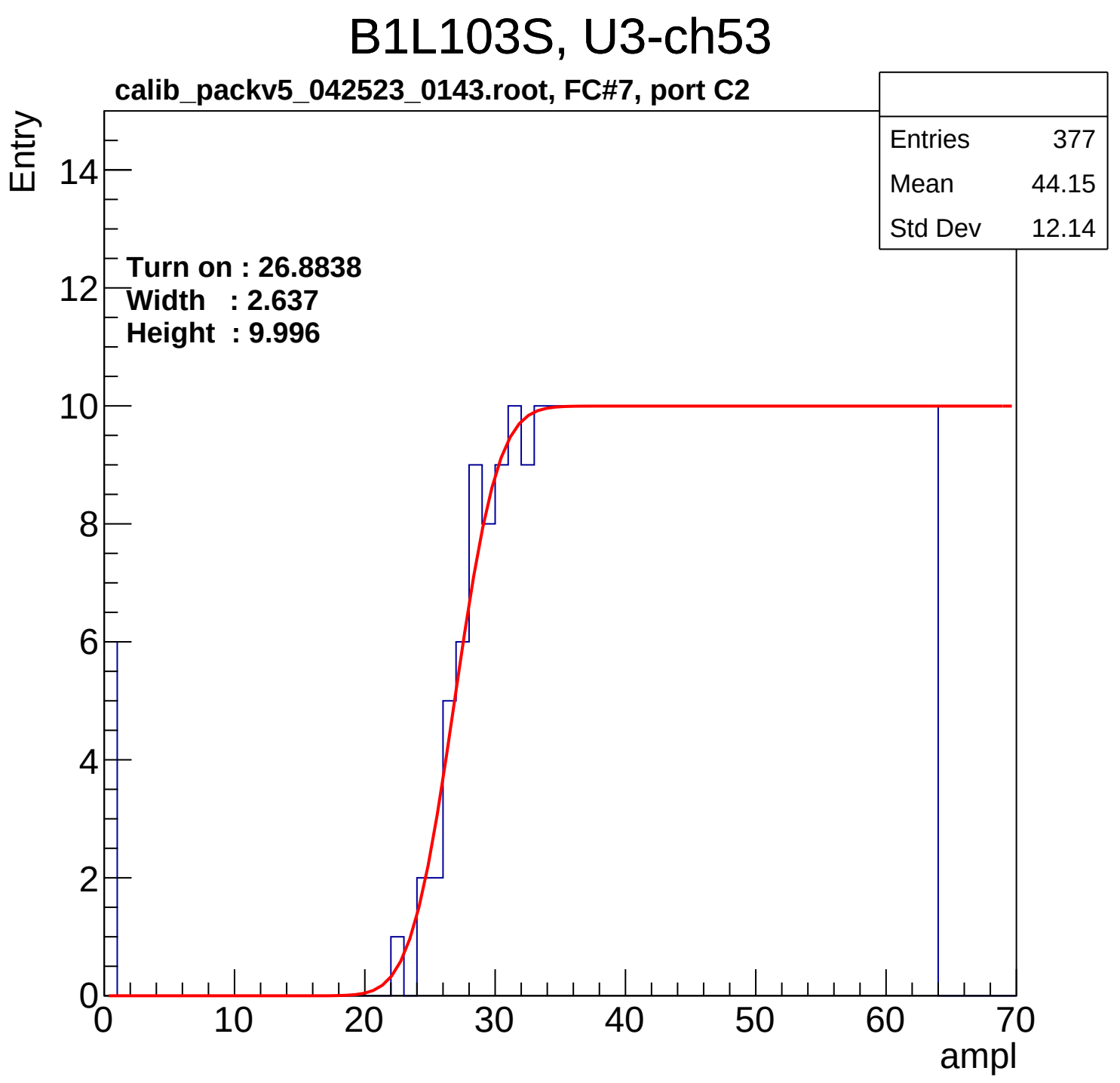
B1L103S, U3-ch53
calib_packv5_042523_0143.root, FC#7, port C2
Entries 377
Mean 44.15
Std Dev 12.14
Turn on : 26.8838
Width : 2.637
Height : 9.996
Entry
ampl
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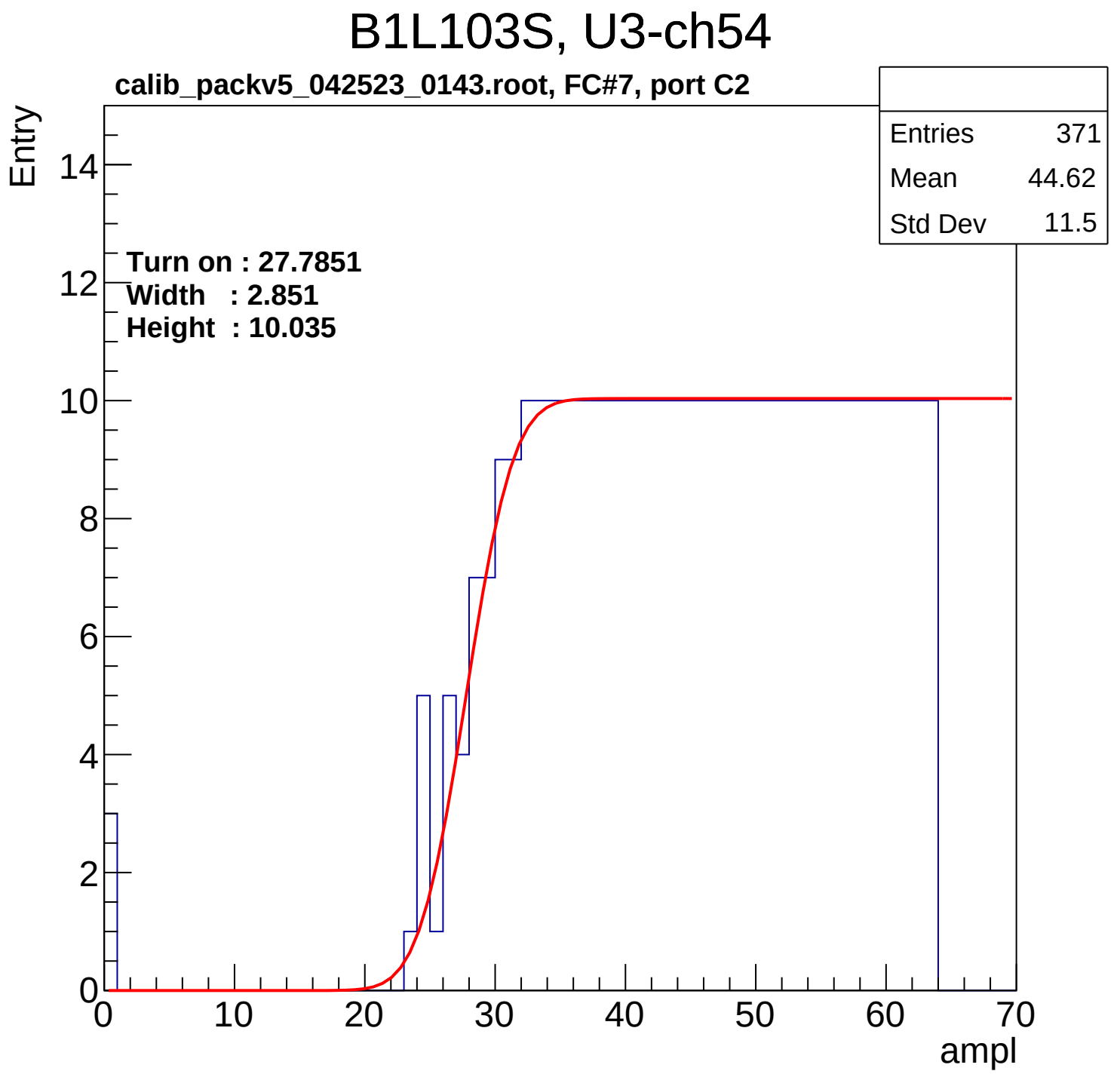
B1L103S, U3-ch54
calib_packv5_042523_0143.root, FC#7, port C2
Entries 371
Mean 44.62
Std Dev 11.5
Turn on : 27.7851
Width : 2.851
Height : 10.035
Entry
ampl
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6
8
10
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60
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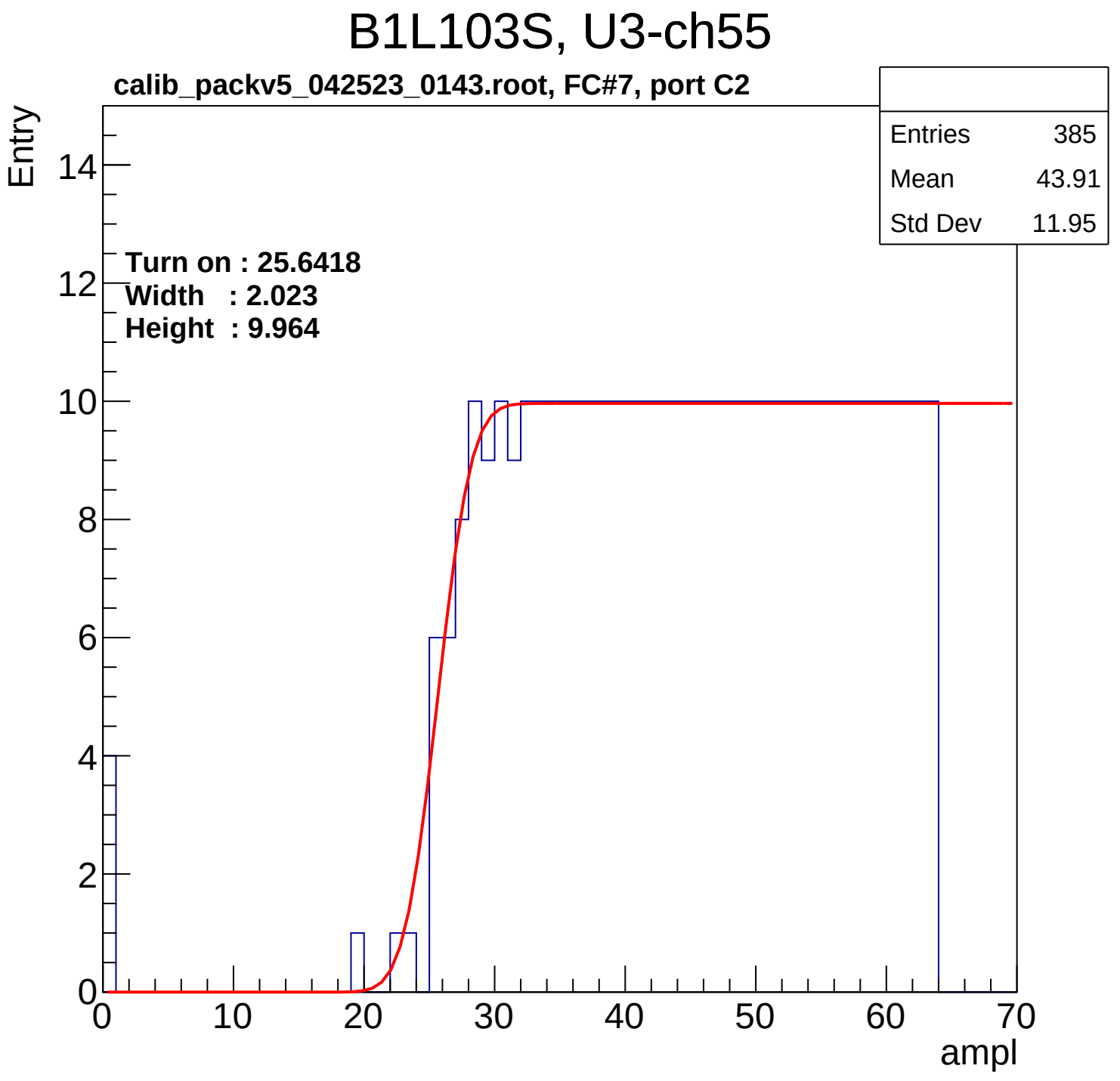
B1L103S, U3-ch55
calib_packv5_042523_0143.root, FC#7, port C2
Entries 385
Mean 43.91
Std Dev 11.95
Turn on : 25.6418
Width : 2.023
Height : 9.964
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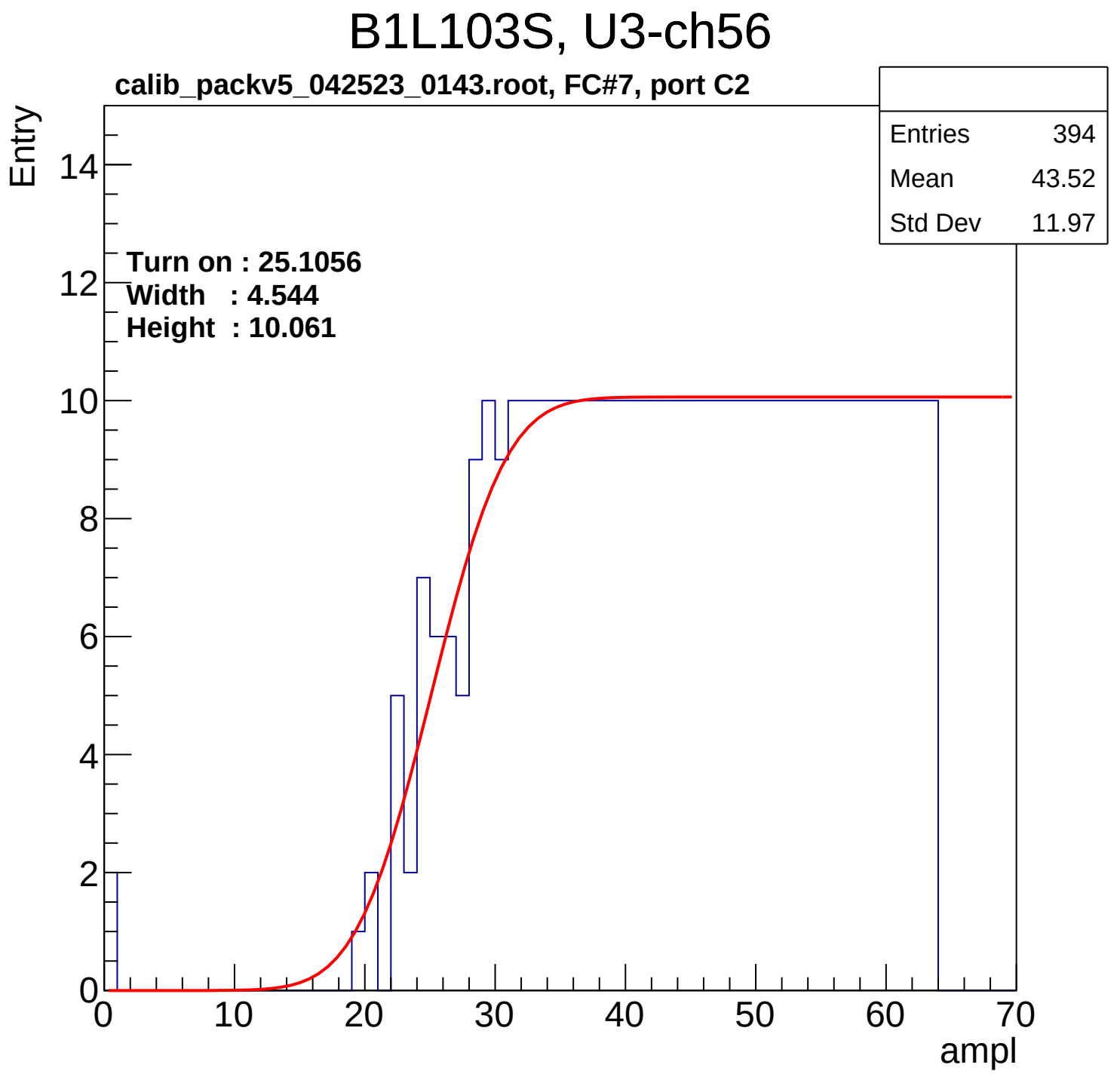
B1L103S, U3-ch56
calib_packv5_042523_0143.root, FC#7, port C2
Entries 394
Mean 43.52
Std Dev 11.97
Turn on : 25.1056
Width : 4.544
Height : 10.061
Entry
ampl
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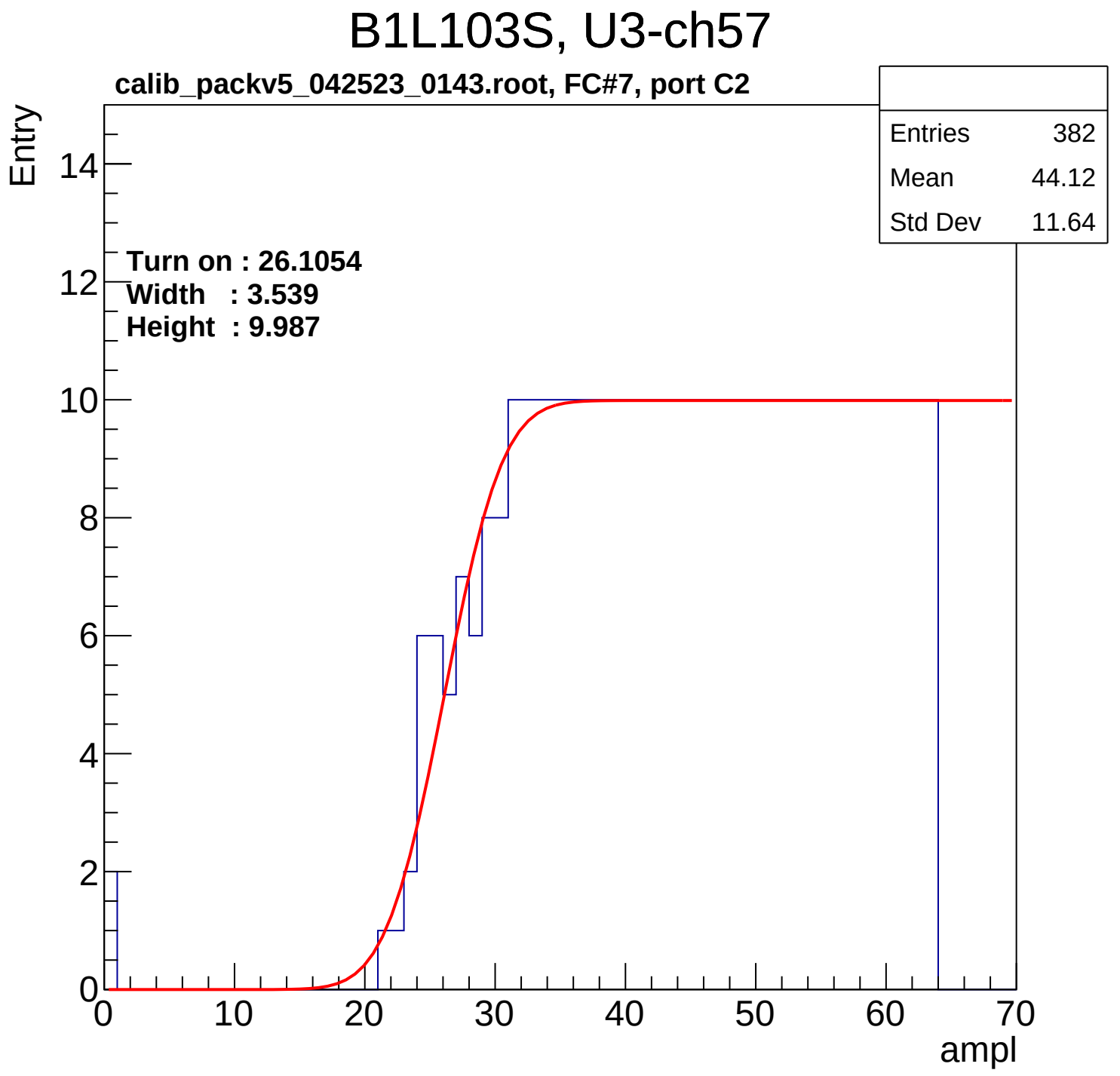
B1L103S, U3-ch57
calib_packv5_042523_0143.root, FC#7, port C2
Entries 382
Mean 44.12
Std Dev 11.64
Turn on : 26.1054
Width : 3.539
Height : 9.987
Entry
ampl
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6
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10
20
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40
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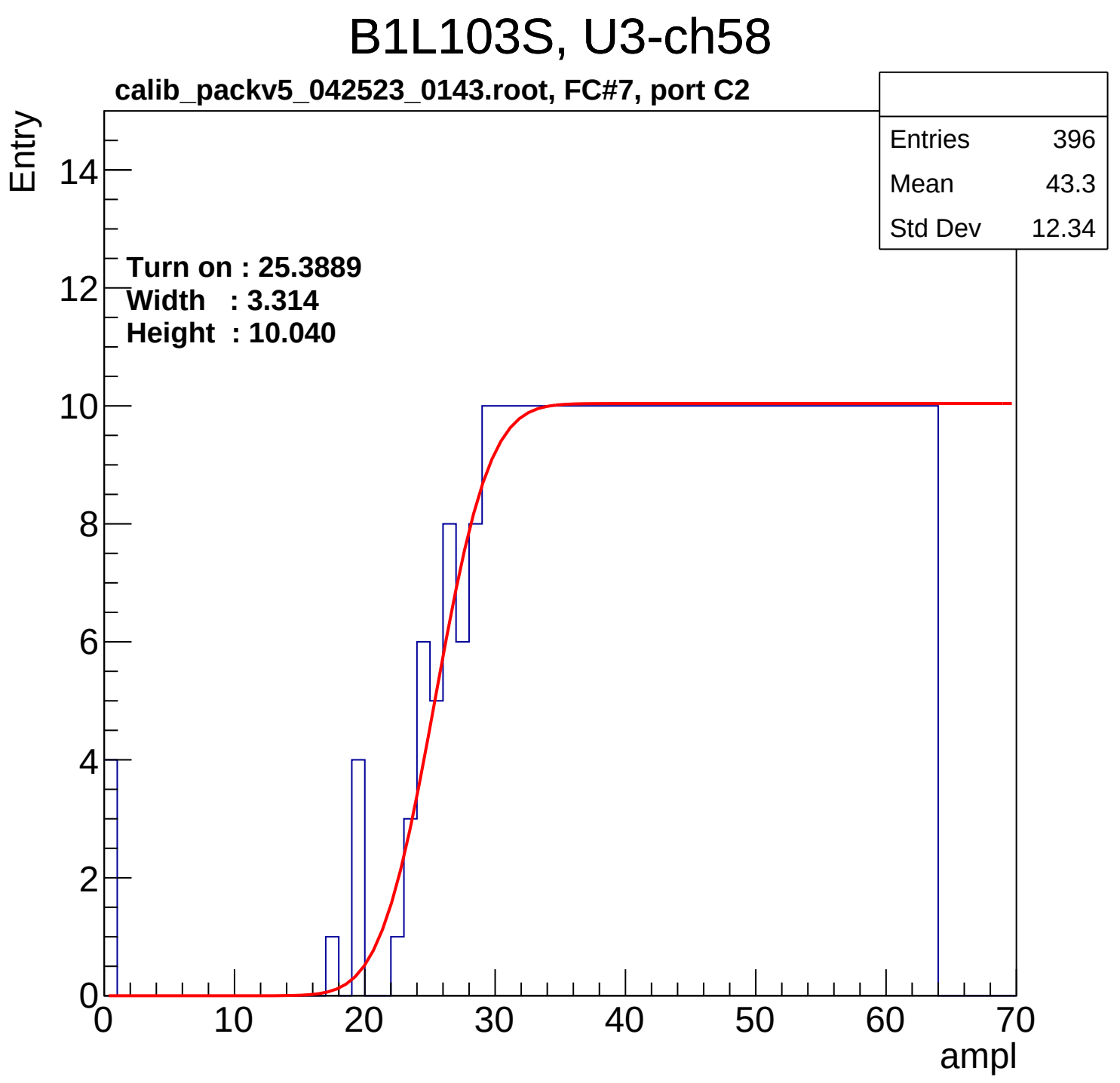
B1L103S, U3-ch58
calib_packv5_042523_0143.root, FC#7, port C2
Entries 396
Mean 43.3
Std Dev 12.34
Turn on : 25.3889
Width : 3.314
Height : 10.040
Entry
ampl
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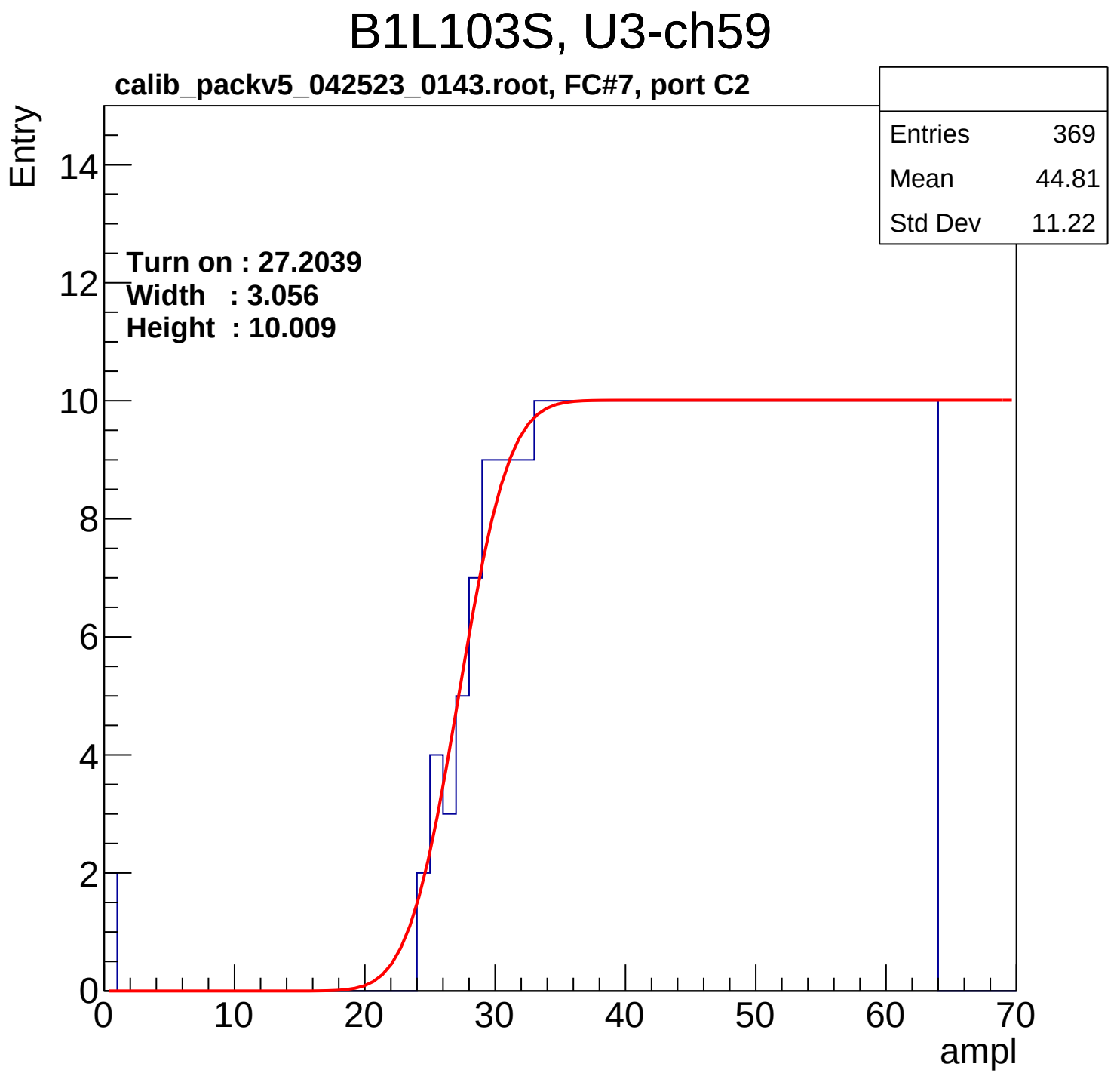
B1L103S, U3-ch59
calib_packv5_042523_0143.root, FC#7, port C2
Entries 369
Mean 44.81
Std Dev 11.22
Turn on : 27.2039
Width : 3.056
Height : 10.009
Entry
ampl
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2
4
6
8
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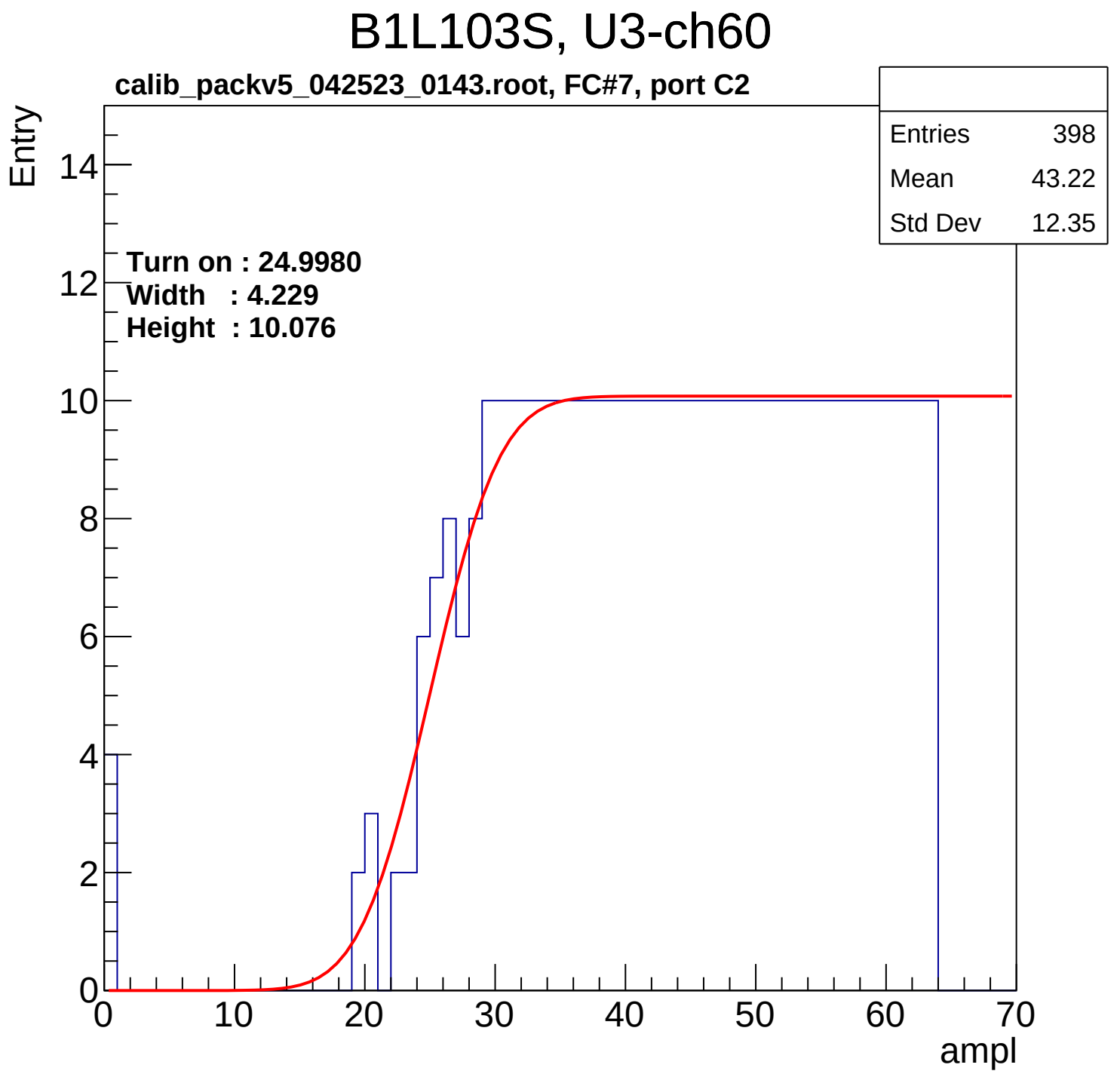
B1L103S, U3-ch60
calib_packv5_042523_0143.root, FC#7, port C2
Entries 398
Mean 43.22
Std Dev 12.35
Turn on : 24.9980
Width : 4.229
Height : 10.076
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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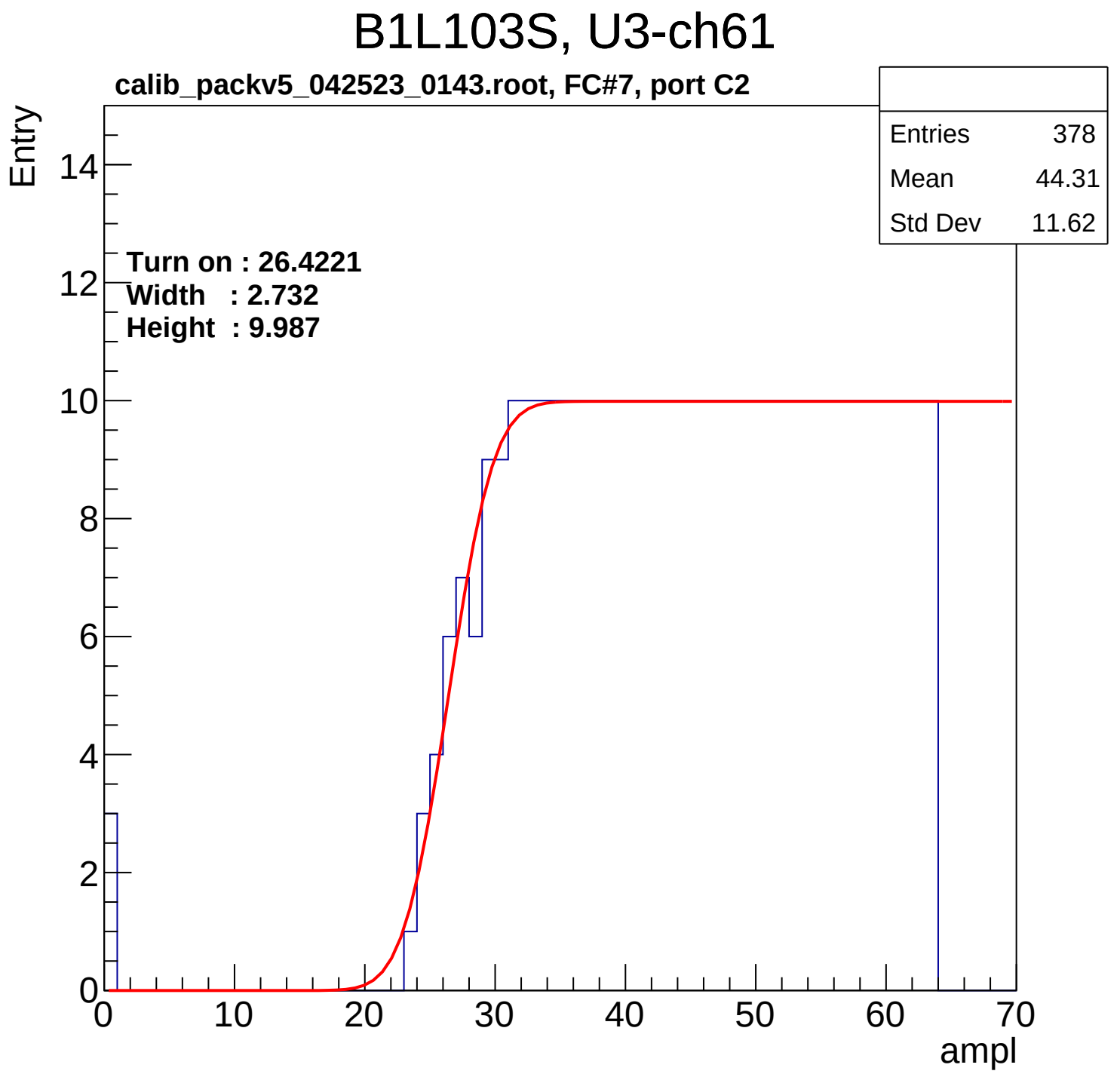
B1L103S, U3-ch61
calib_packv5_042523_0143.root, FC#7, port C2
Entries 378
Mean 44.31
Std Dev 11.62
Turn on : 26.4221
Width : 2.732
Height : 9.987
Entry
ampl
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2
4
6
8
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12
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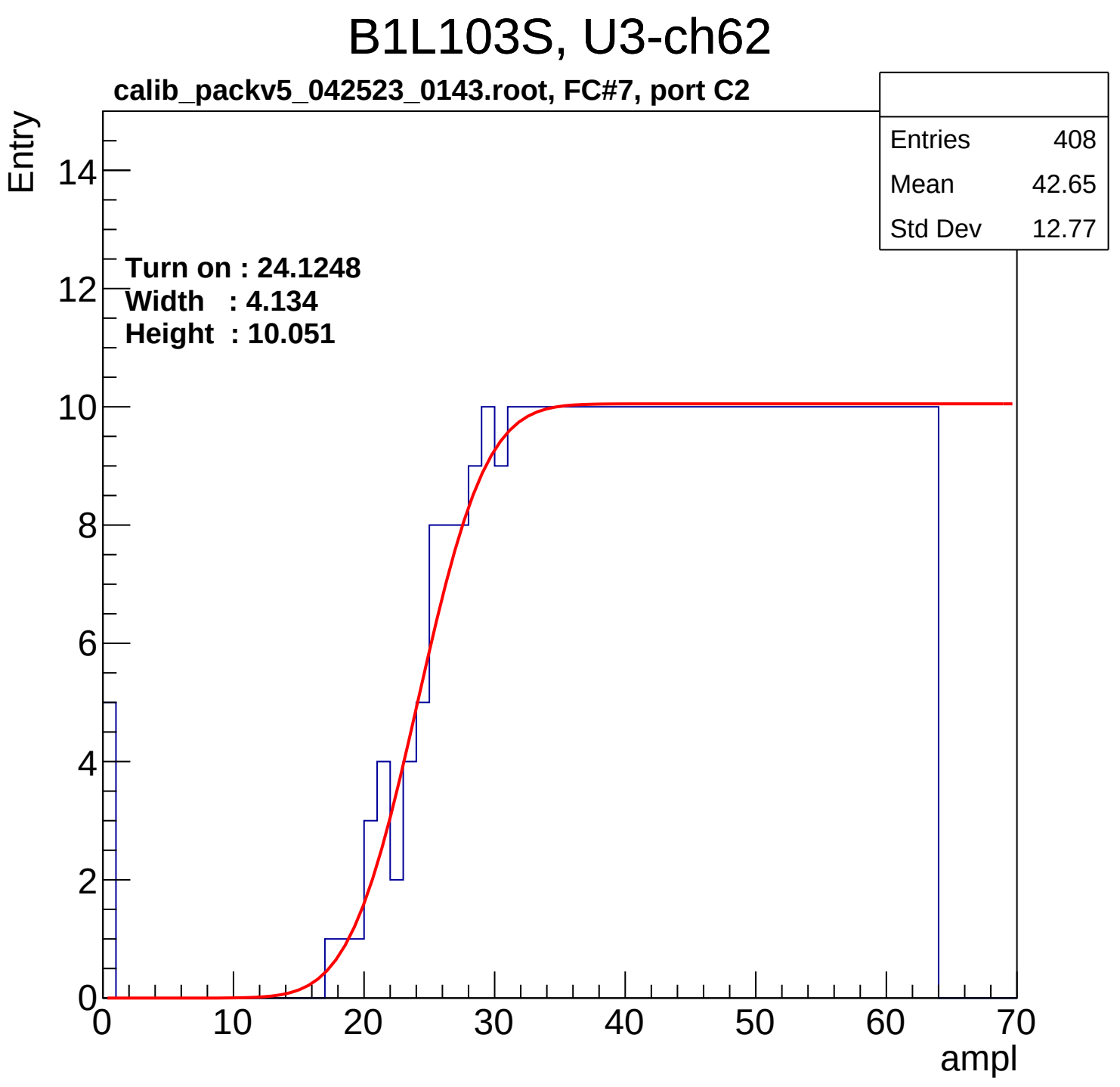
B1L103S, U3-ch62
calib_packv5_042523_0143.root, FC#7, port C2
Entries 408
Mean 42.65
Std Dev 12.77
Turn on : 24.1248
Width : 4.134
Height : 10.051
Entry
ampl
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2
4
6
8
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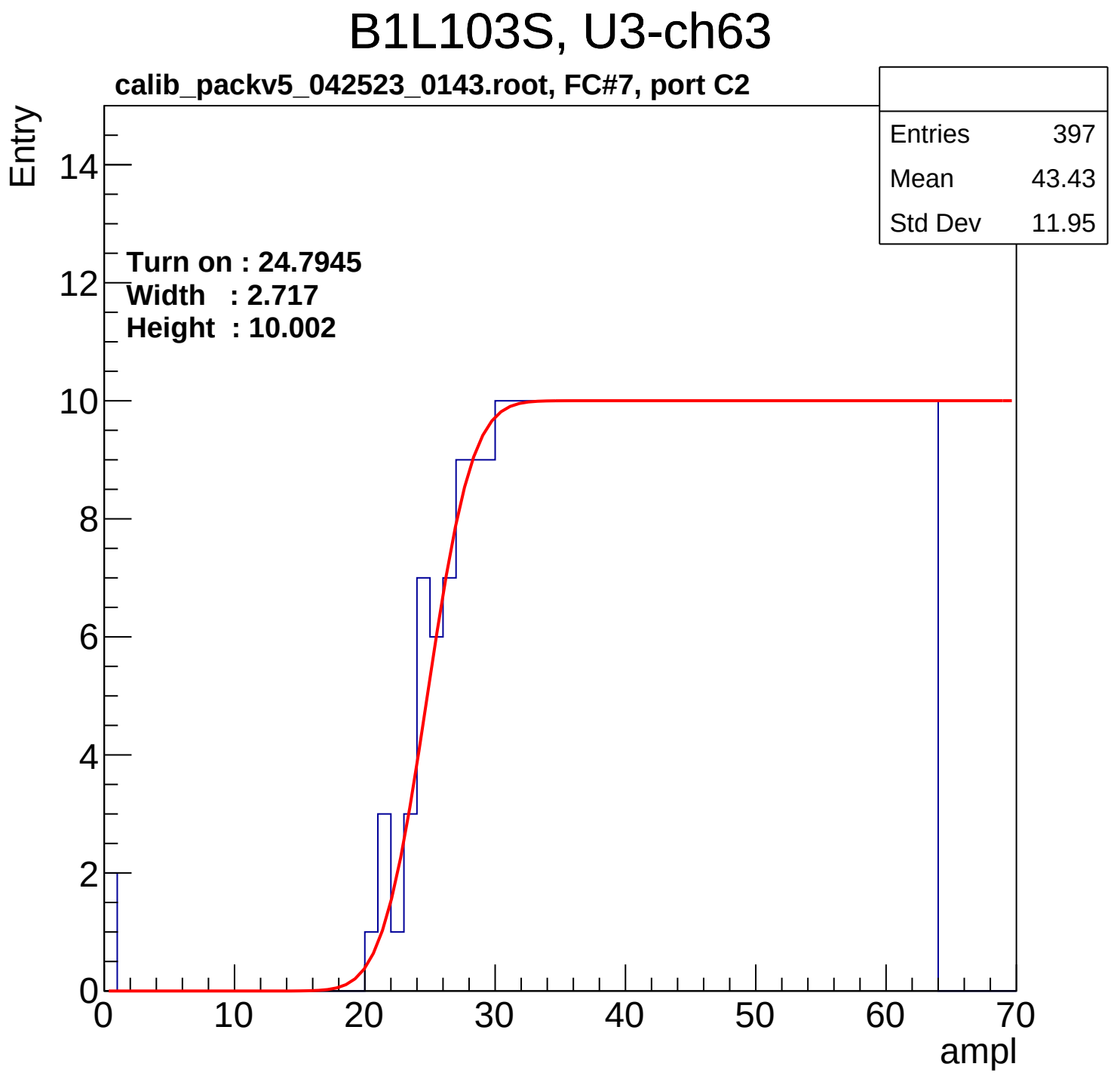
B1L103S, U3-ch63
calib_packv5_042523_0143.root, FC#7, port C2
Entries 397
Mean 43.43
Std Dev 11.95
Turn on : 24.7945
Width : 2.717
Height : 10.002
Entry
ampl
0
2
4
6
8
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12
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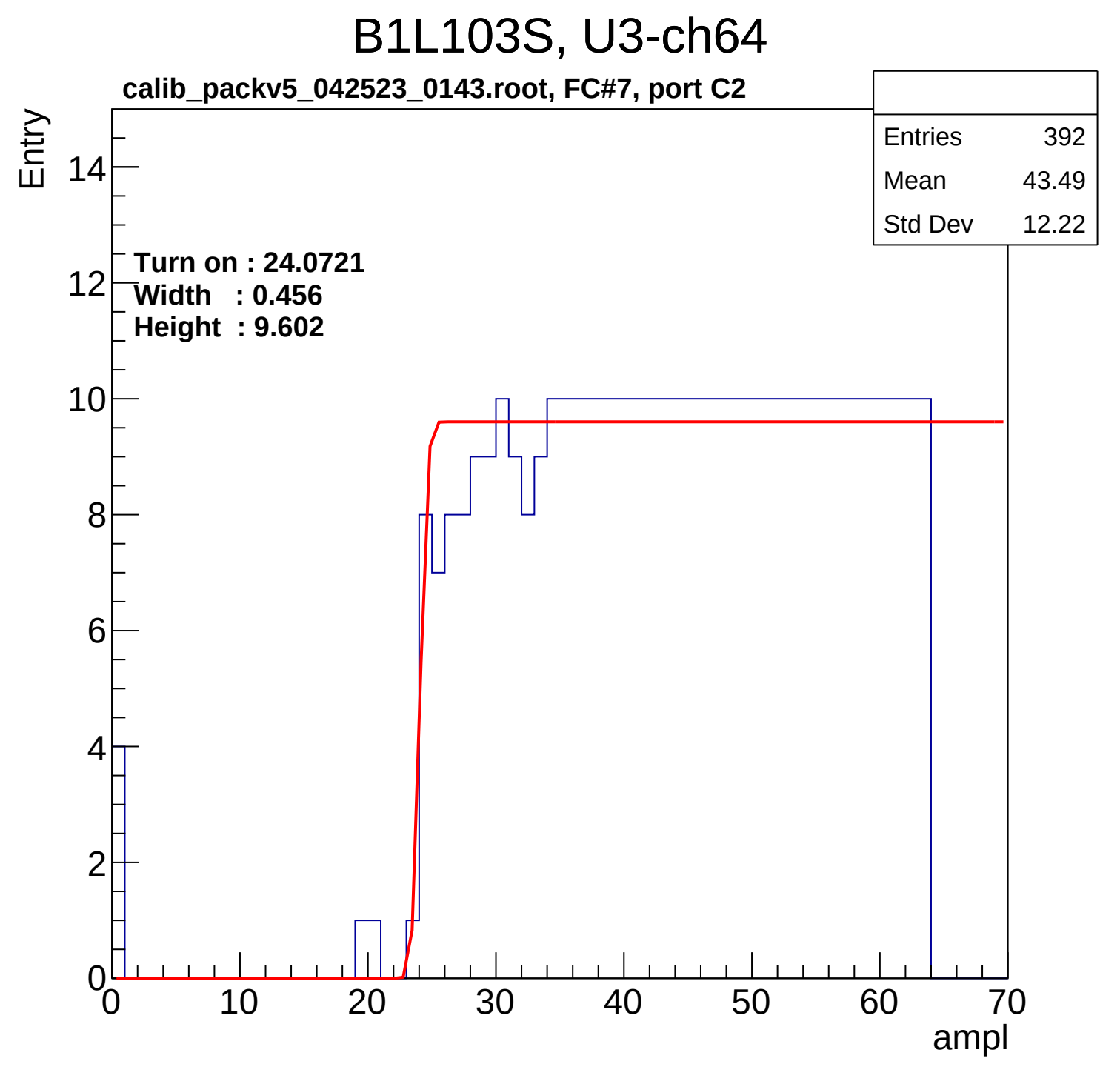
B1L103S, U3-ch64
calib_packv5_042523_0143.root, FC#7, port C2
Entries 392
Mean 43.49
Std Dev 12.22
Turn on : 24.0721
Width : 0.456
Height : 9.602
Entry
ampl
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2
4
6
8
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12
14
0
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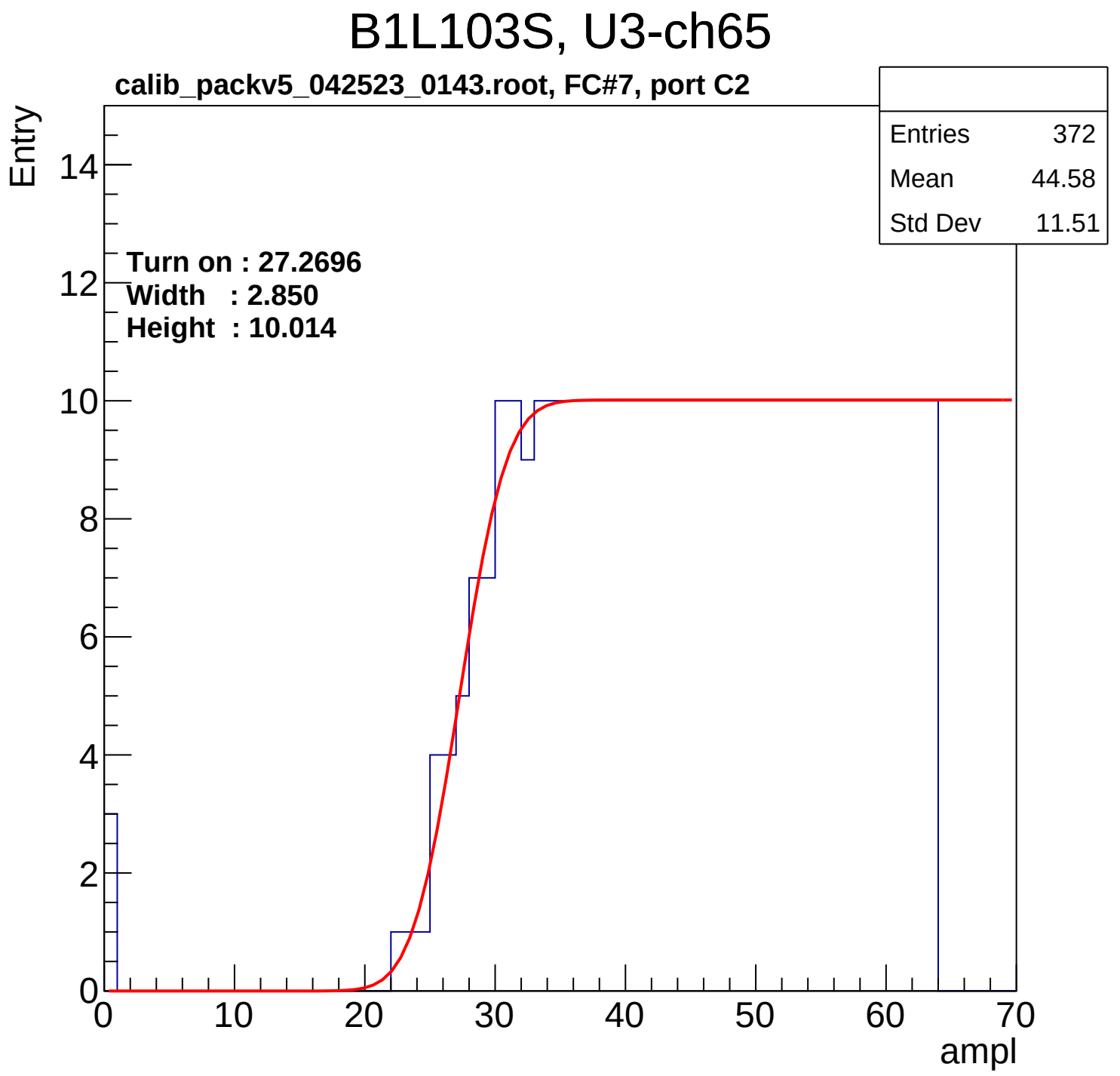
B1L103S, U3-ch65
calib_packv5_042523_0143.root, FC#7, port C2
Entries 372
Mean 44.58
Std Dev 11.51
Turn on : 27.2696
Width : 2.850
Height : 10.014
Entry
ampl
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2
4
6
8
10
12
14
0
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40
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60
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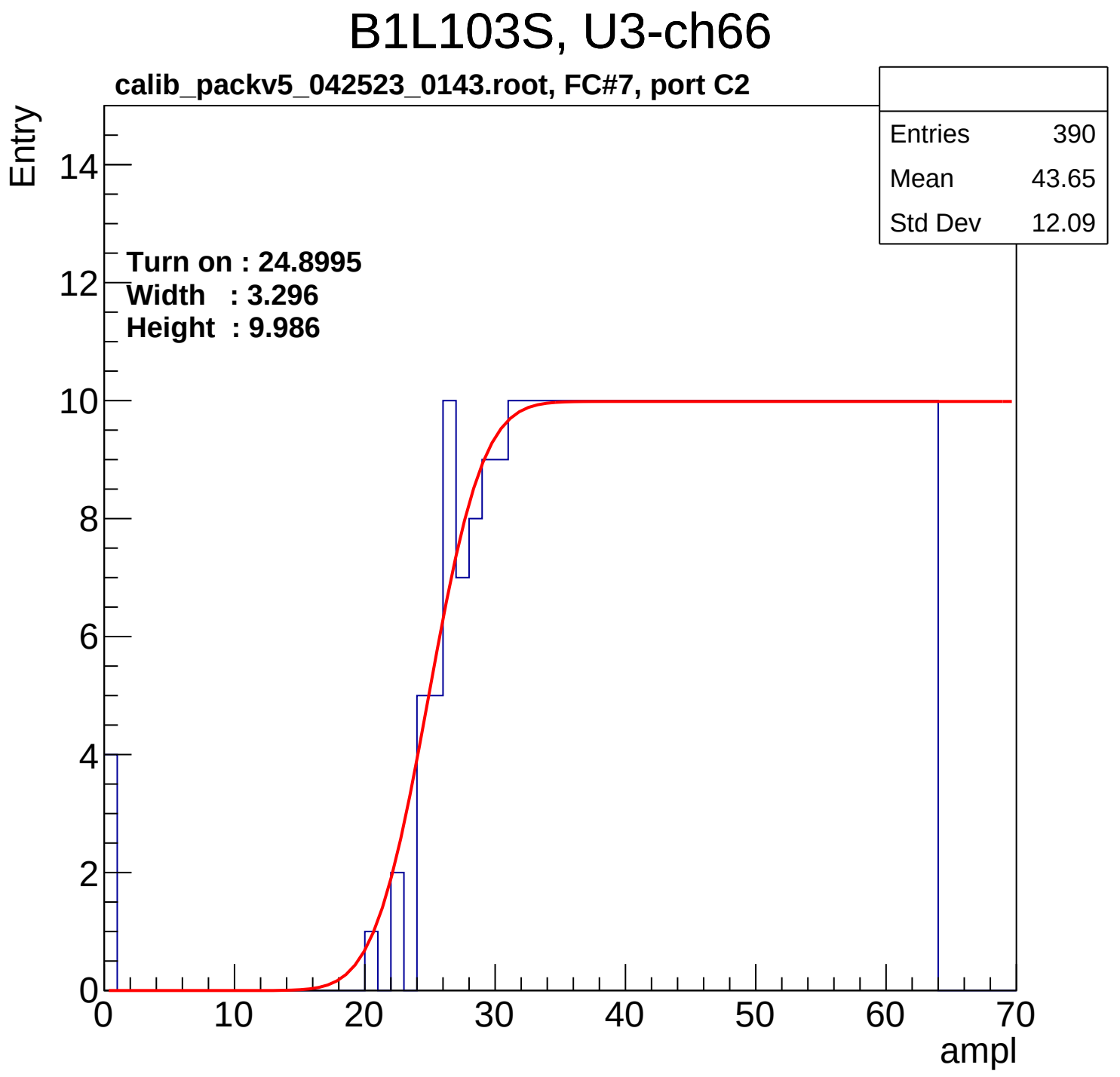
B1L103S, U3-ch66
calib_packv5_042523_0143.root, FC#7, port C2
Entries 390
Mean 43.65
Std Dev 12.09
Turn on : 24.8995
Width : 3.296
Height : 9.986
Entry
ampl
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6
8
10
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0
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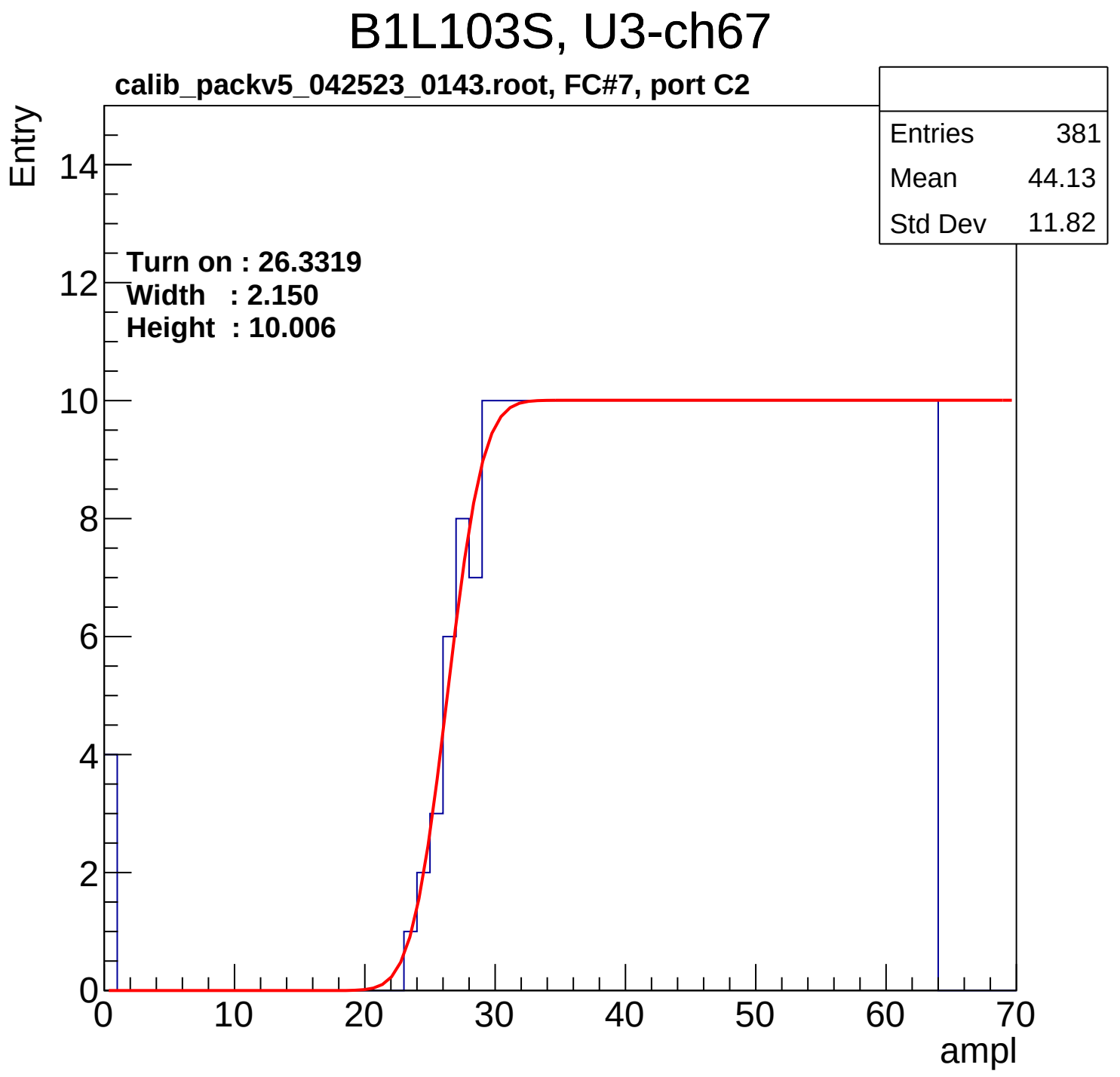
B1L103S, U3-ch67
calib_packv5_042523_0143.root, FC#7, port C2
Entries 381
Mean 44.13
Std Dev 11.82
Turn on : 26.3319
Width : 2.150
Height : 10.006
Entry
ampl
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2
4
6
8
10
12
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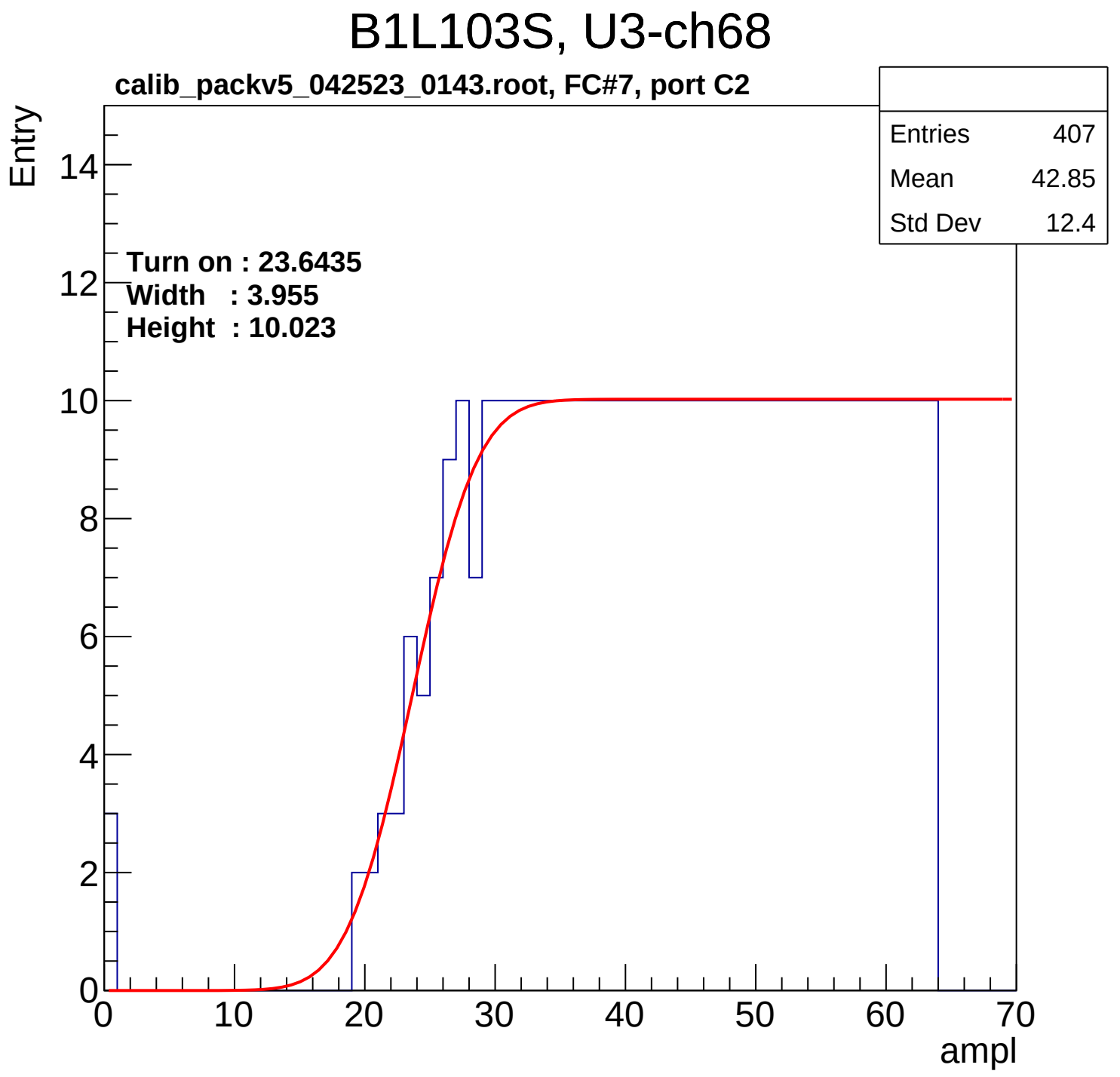
B1L103S, U3-ch68
calib_packv5_042523_0143.root, FC#7, port C2
Entries 407
Mean 42.85
Std Dev 12.4
Turn on : 23.6435
Width : 3.955
Height : 10.023
Entry
ampl
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6
8
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0
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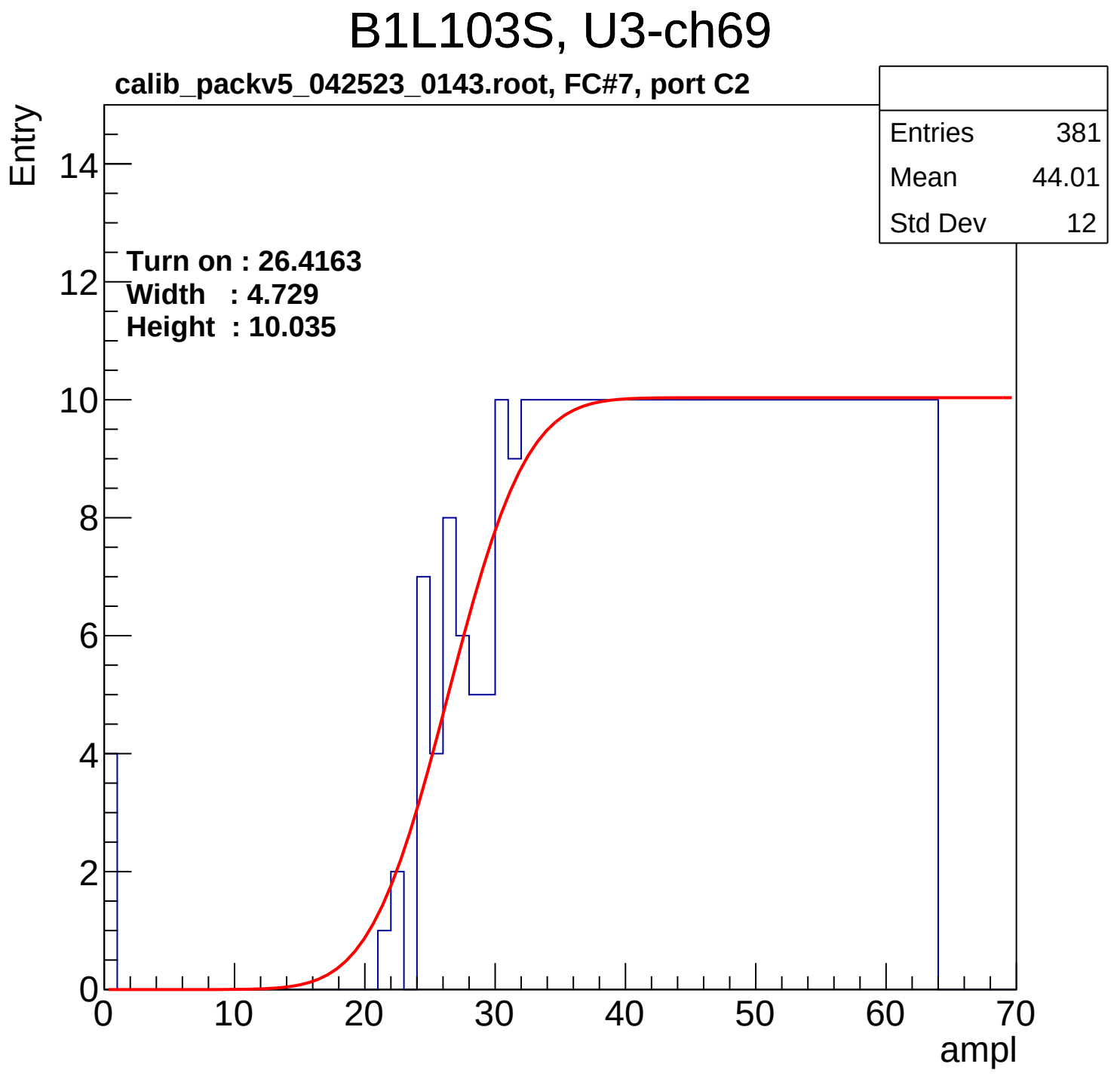
B1L103S, U3-ch69
calib_packv5_042523_0143.root, FC#7, port C2
Entries 381
Mean 44.01
Std Dev 12
Turn on : 26.4163
Width : 4.729
Height : 10.035
Entry
ampl
0
2
4
6
8
10
12
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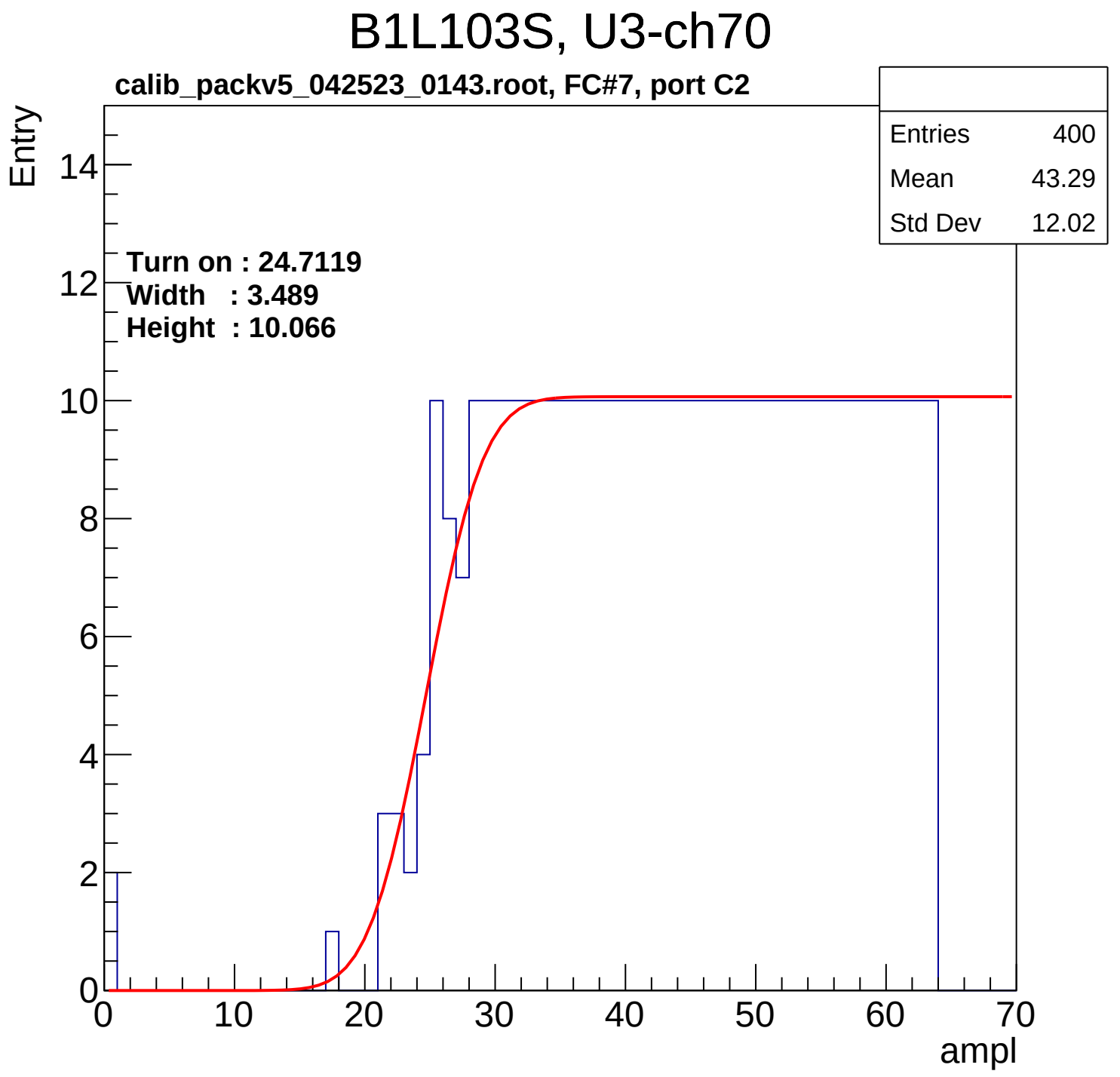
B1L103S, U3-ch70
calib_packv5_042523_0143.root, FC#7, port C2
Entries 400
Mean 43.29
Std Dev 12.02
Turn on : 24.7119
Width : 3.489
Height : 10.066
Entry
ampl
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8
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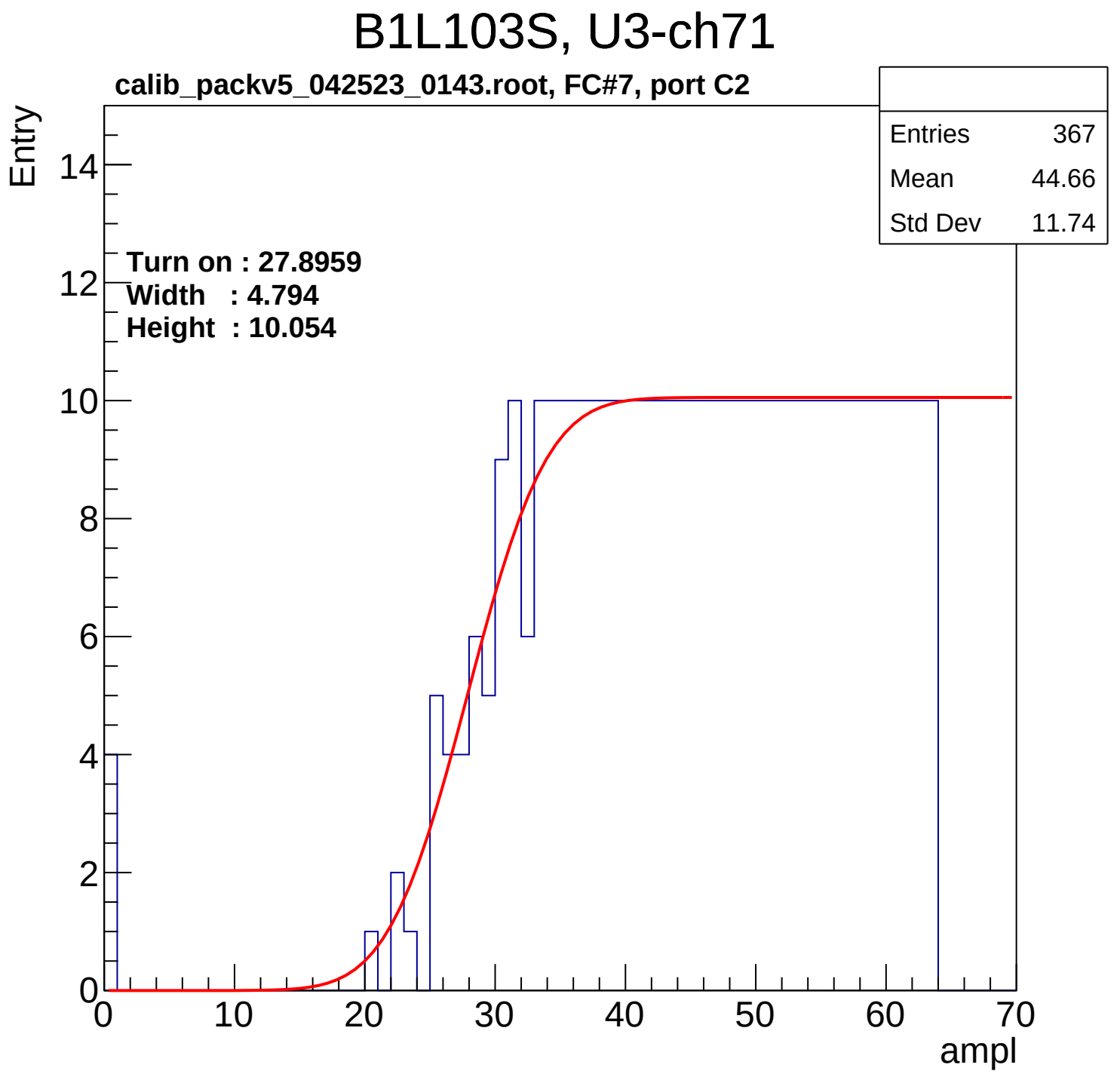
B1L103S, U3-ch71
calib_packv5_042523_0143.root, FC#7, port C2
Entries 367
Mean 44.66
Std Dev 11.74
Turn on : 27.8959
Width : 4.794
Height : 10.054
Entry
ampl
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6
8
10
12
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0
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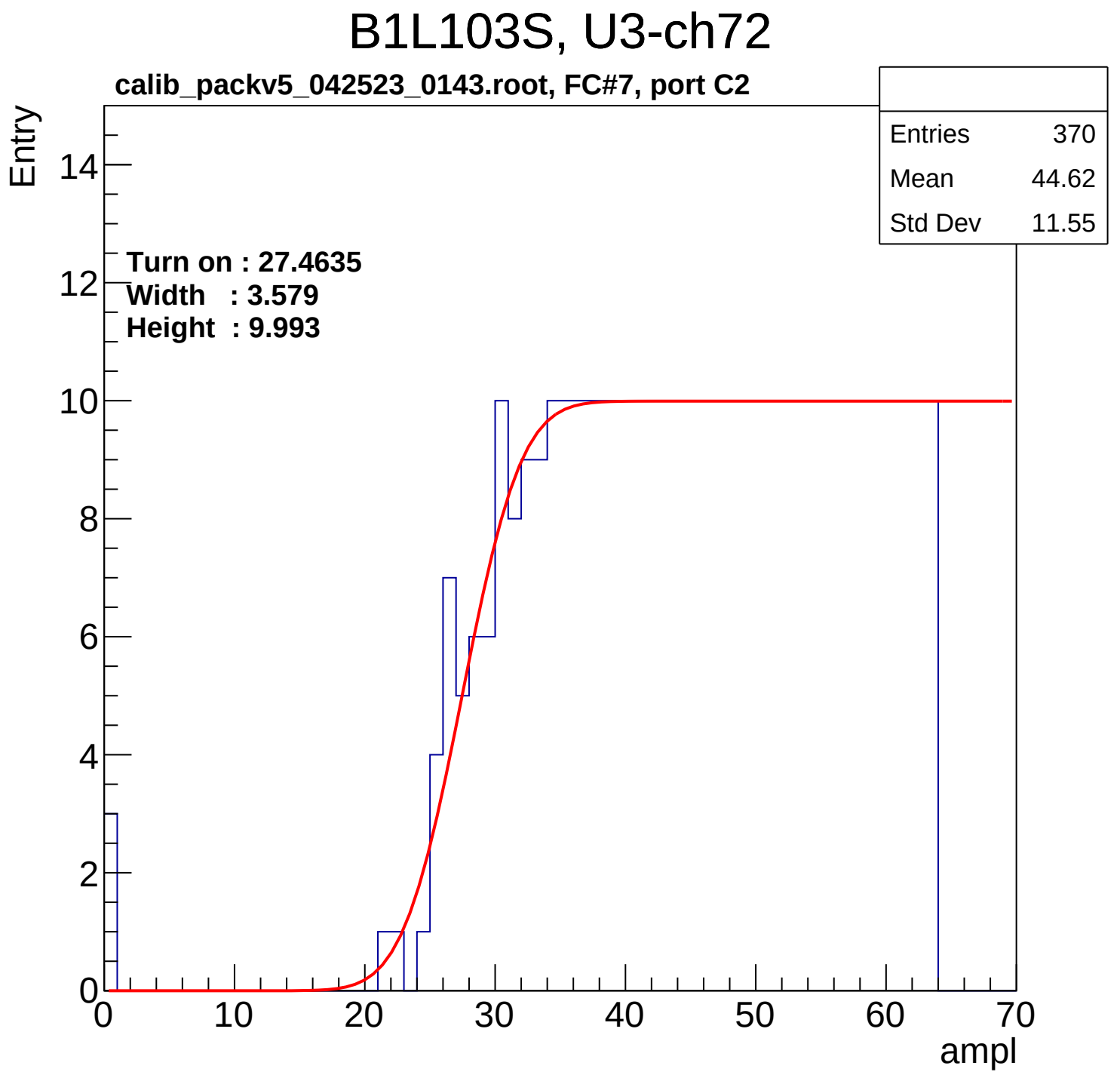
B1L103S, U3-ch72
calib_packv5_042523_0143.root, FC#7, port C2
Entries 370
Mean 44.62
Std Dev 11.55
Turn on : 27.4635
Width : 3.579
Height : 9.993
Entry
ampl
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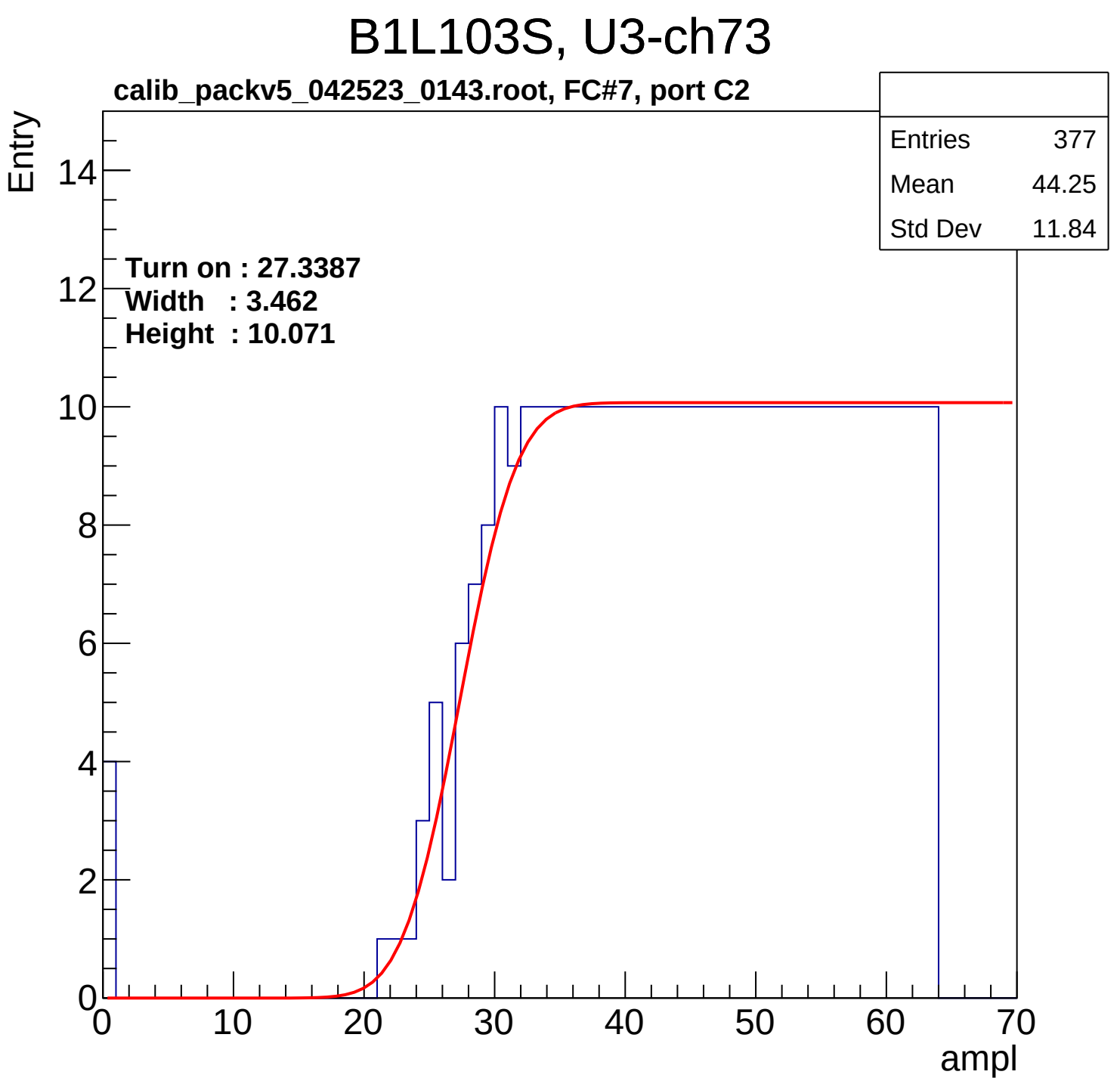
B1L103S, U3-ch73
calib_packv5_042523_0143.root, FC#7, port C2
Entries 377
Mean 44.25
Std Dev 11.84
Turn on : 27.3387
Width : 3.462
Height : 10.071
Entry
ampl
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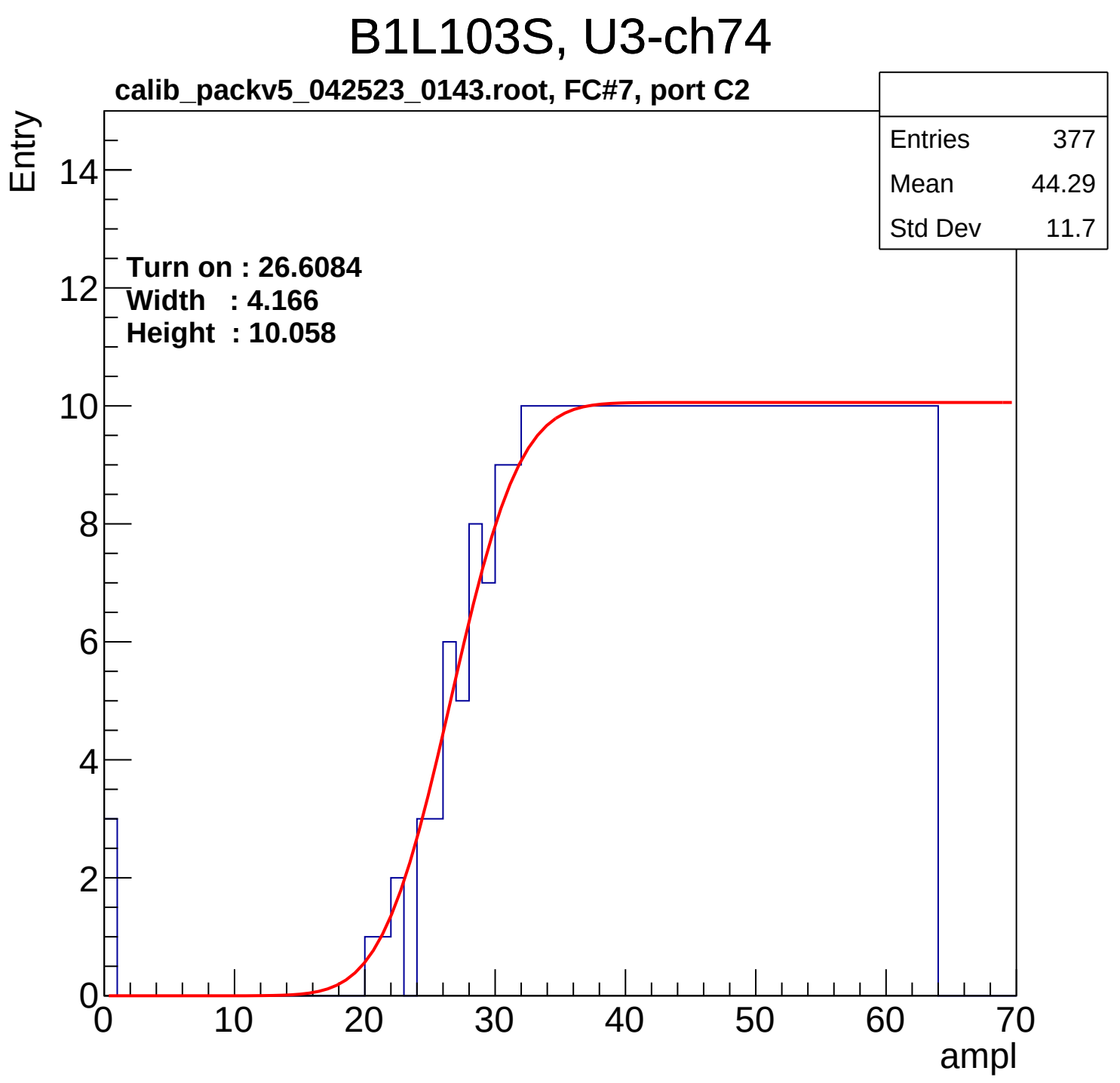
B1L103S, U3-ch74
calib_packv5_042523_0143.root, FC#7, port C2
Entries 377
Mean 44.29
Std Dev 11.7
Turn on : 26.6084
Width : 4.166
Height : 10.058
Entry
ampl
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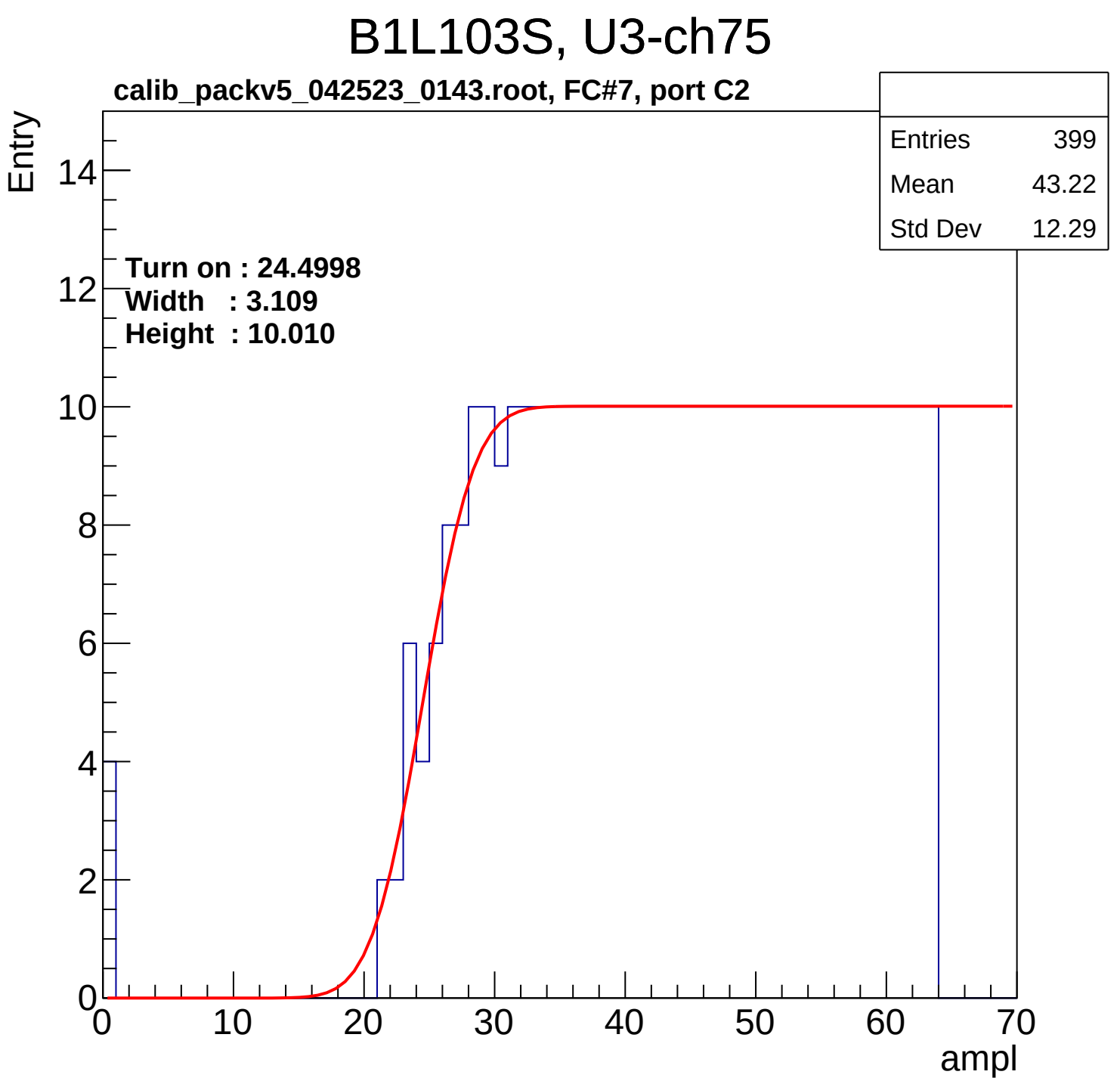
B1L103S, U3-ch75
calib_packv5_042523_0143.root, FC#7, port C2
Entries 399
Mean 43.22
Std Dev 12.29
Turn on : 24.4998
Width : 3.109
Height : 10.010
Entry
ampl
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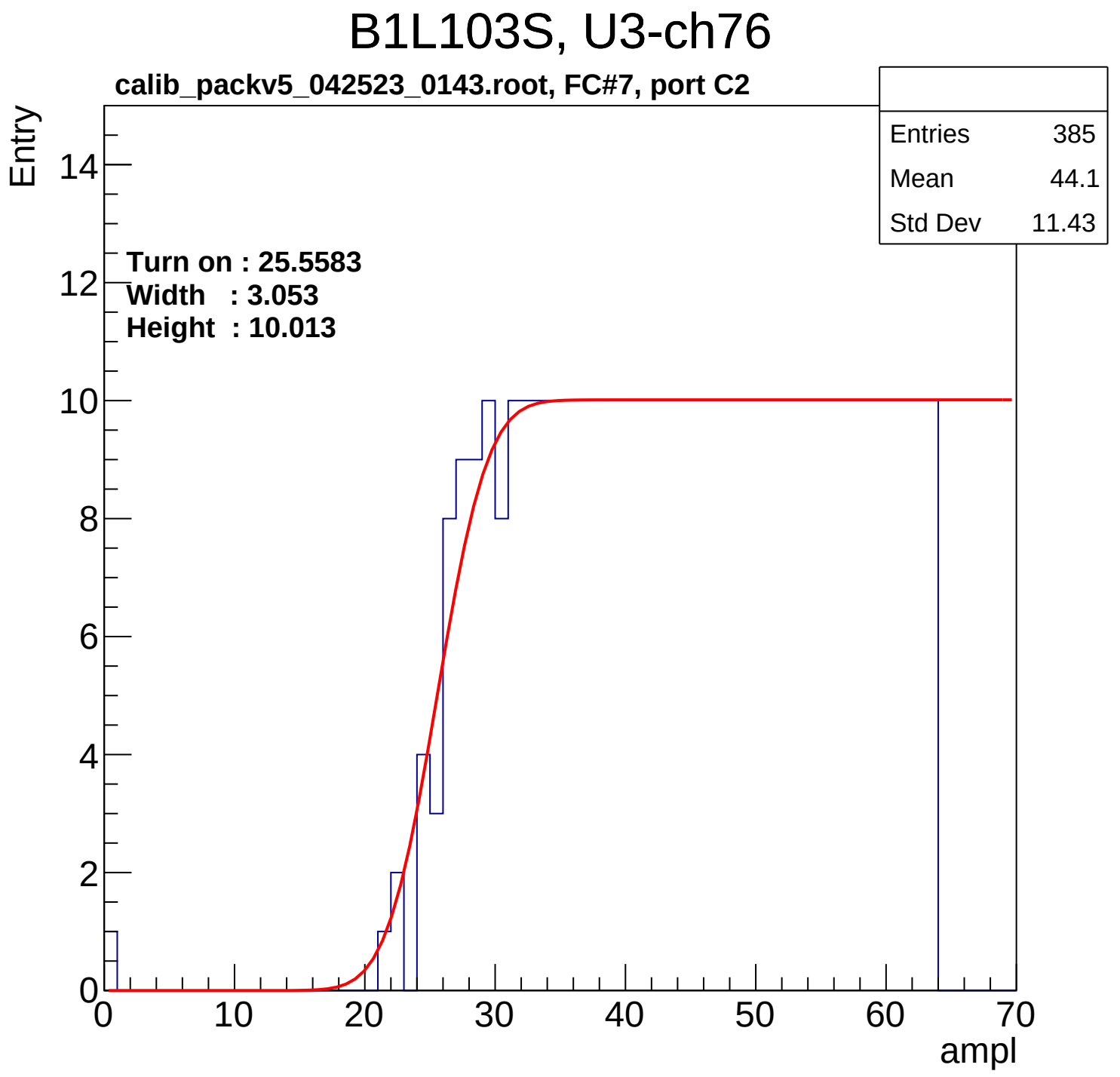
B1L103S, U3-ch76
calib_packv5_042523_0143.root, FC#7, port C2
Entries 385
Mean 44.1
Std Dev 11.43
Turn on : 25.5583
Width : 3.053
Height : 10.013
Entry
ampl
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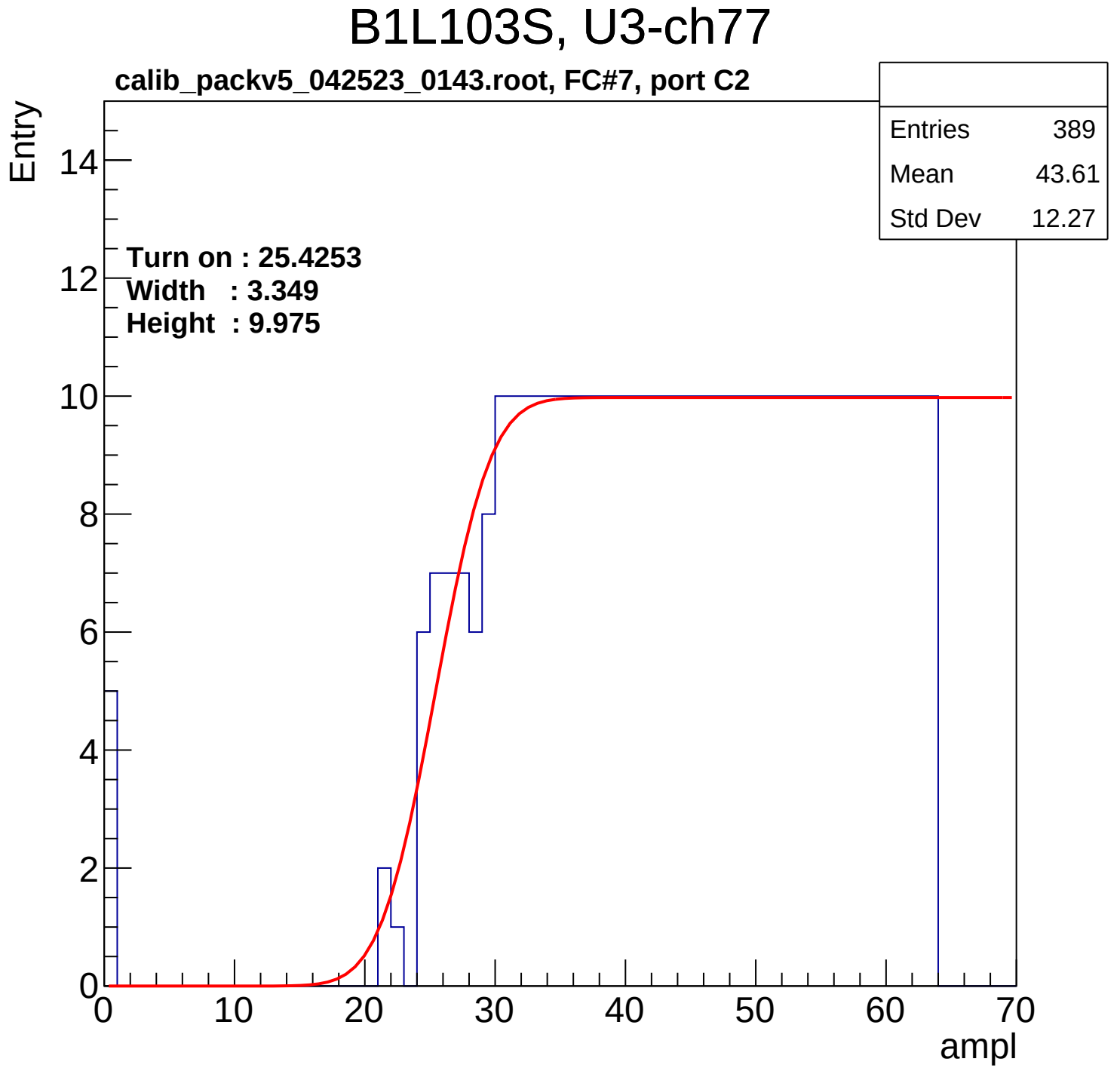
B1L103S, U3-ch77
calib_packv5_042523_0143.root, FC#7, port C2
Entries 389
Mean 43.61
Std Dev 12.27
Turn on : 25.4253
Width : 3.349
Height : 9.975
Entry
ampl
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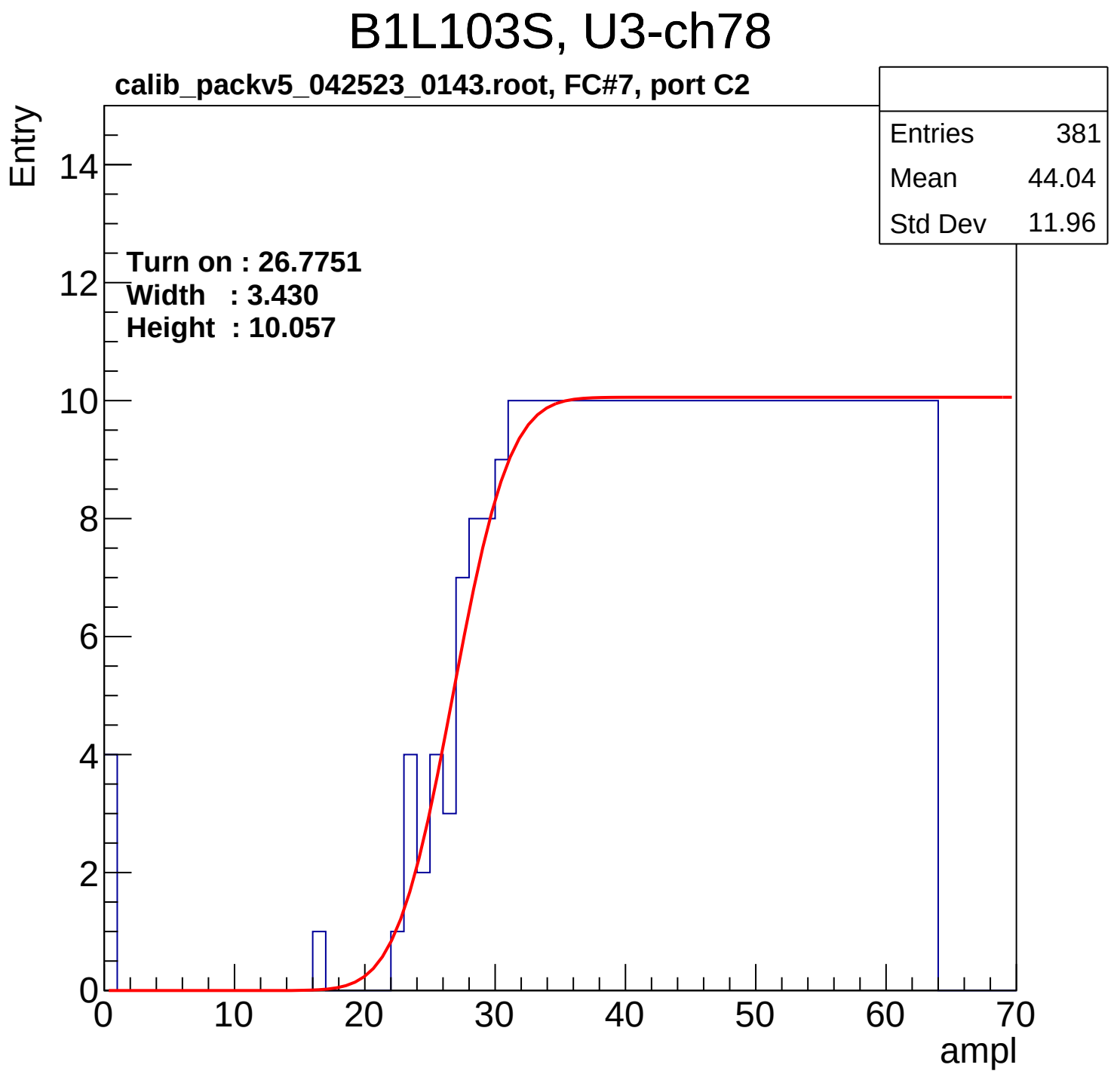
B1L103S, U3-ch78
calib_packv5_042523_0143.root, FC#7, port C2
Entries 381
Mean 44.04
Std Dev 11.96
Turn on : 26.7751
Width : 3.430
Height : 10.057
Entry
ampl
0
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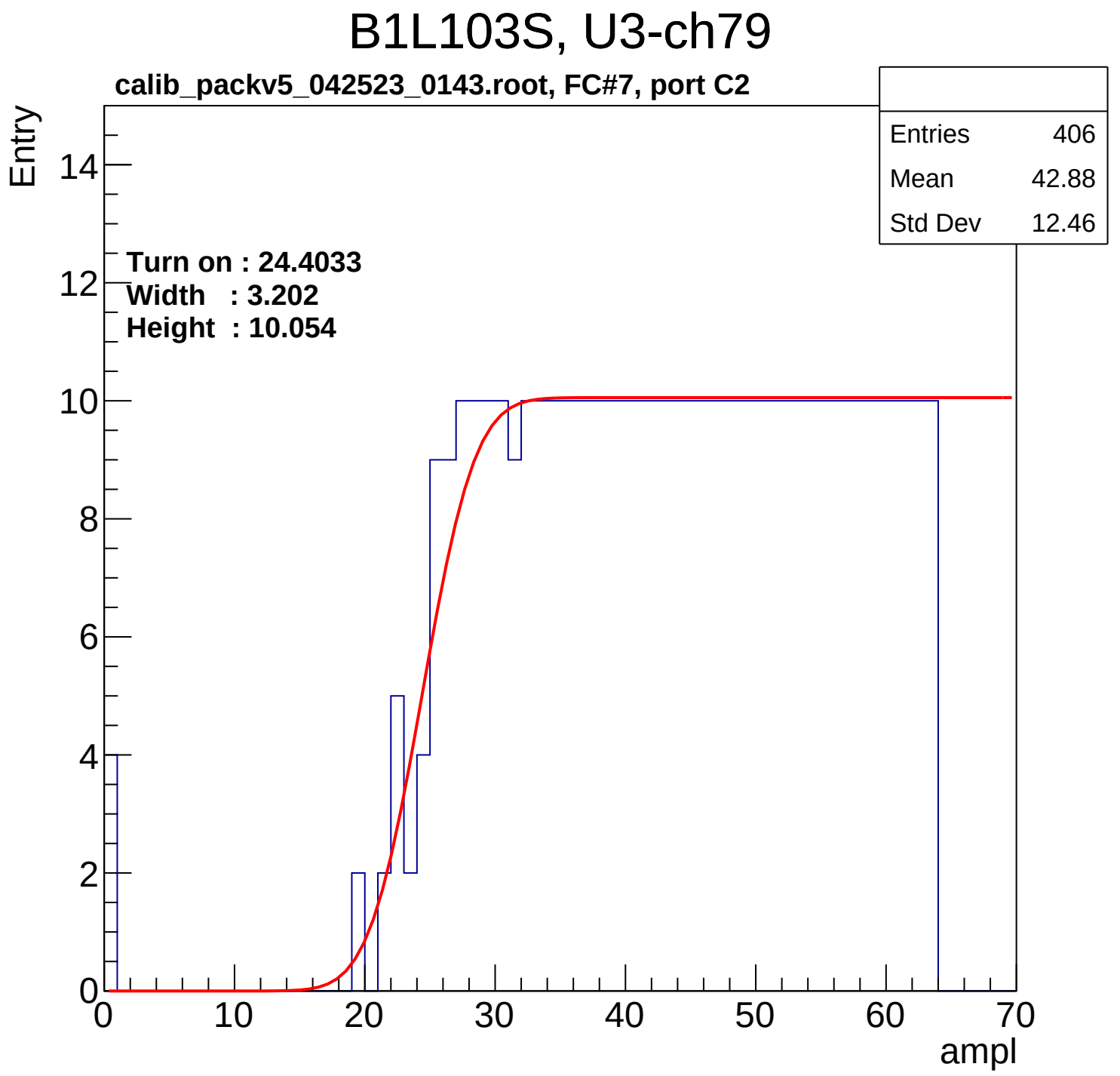
B1L103S, U3-ch79
calib_packv5_042523_0143.root, FC#7, port C2
Entries 406
Mean 42.88
Std Dev 12.46
Turn on : 24.4033
Width : 3.202
Height : 10.054
Entry
ampl
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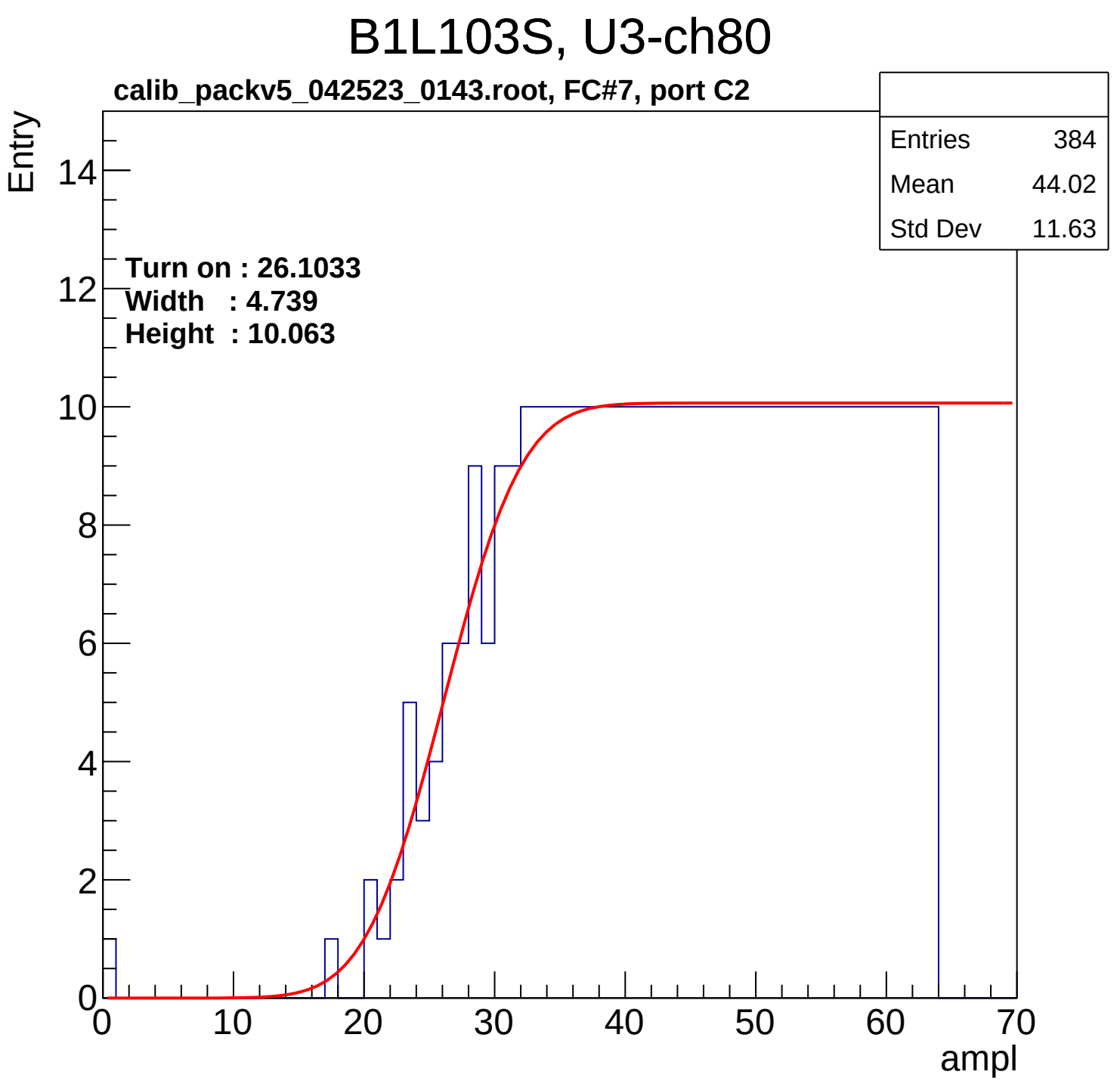
B1L103S, U3-ch80
calib_packv5_042523_0143.root, FC#7, port C2
Entries 384
Mean 44.02
Std Dev 11.63
Turn on : 26.1033
Width : 4.739
Height : 10.063
Entry
ampl
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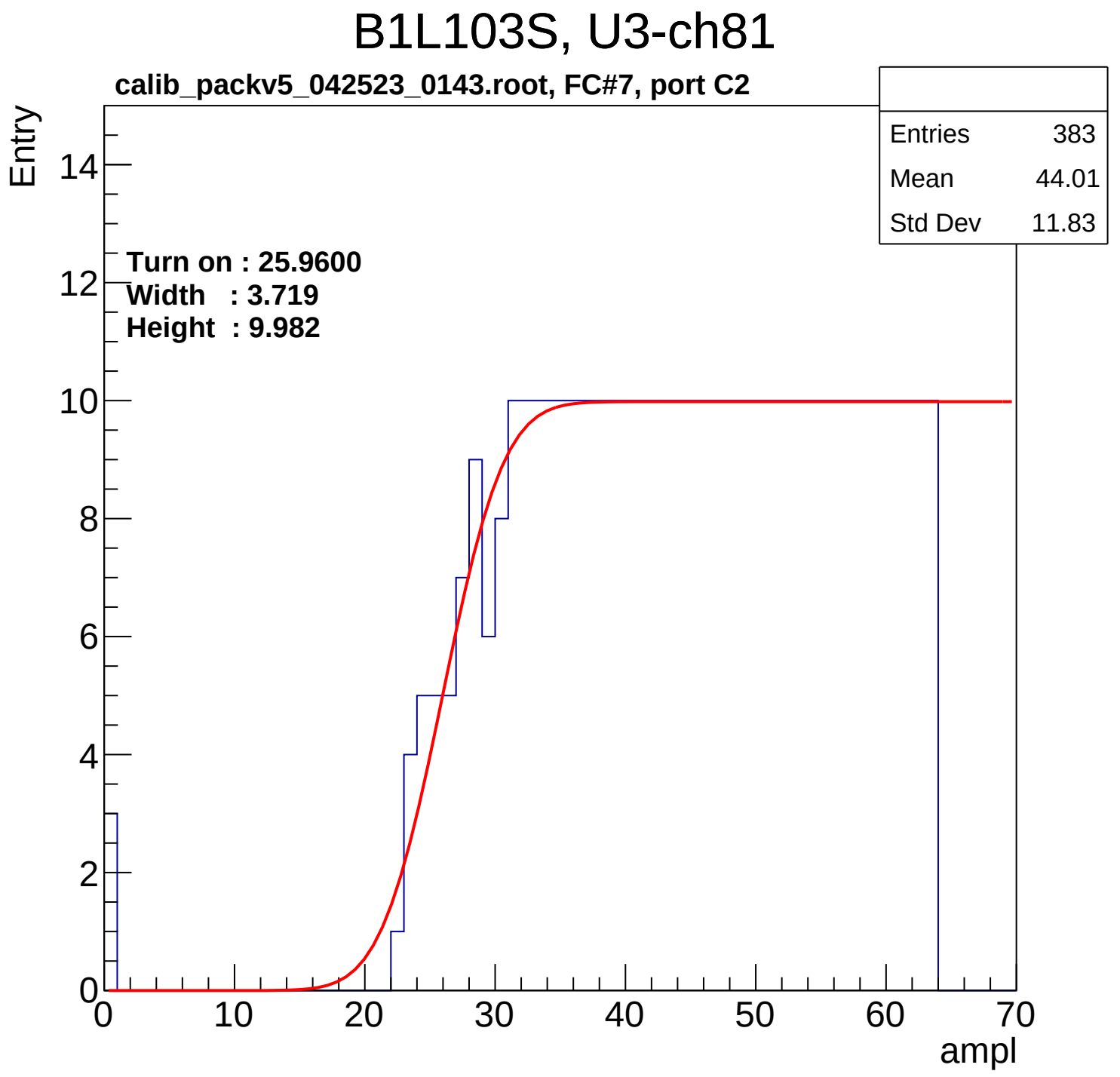
B1L103S, U3-ch81
calib_packv5_042523_0143.root, FC#7, port C2
Entries 383
Mean 44.01
Std Dev 11.83
Turn on : 25.9600
Width : 3.719
Height : 9.982
Entry
ampl
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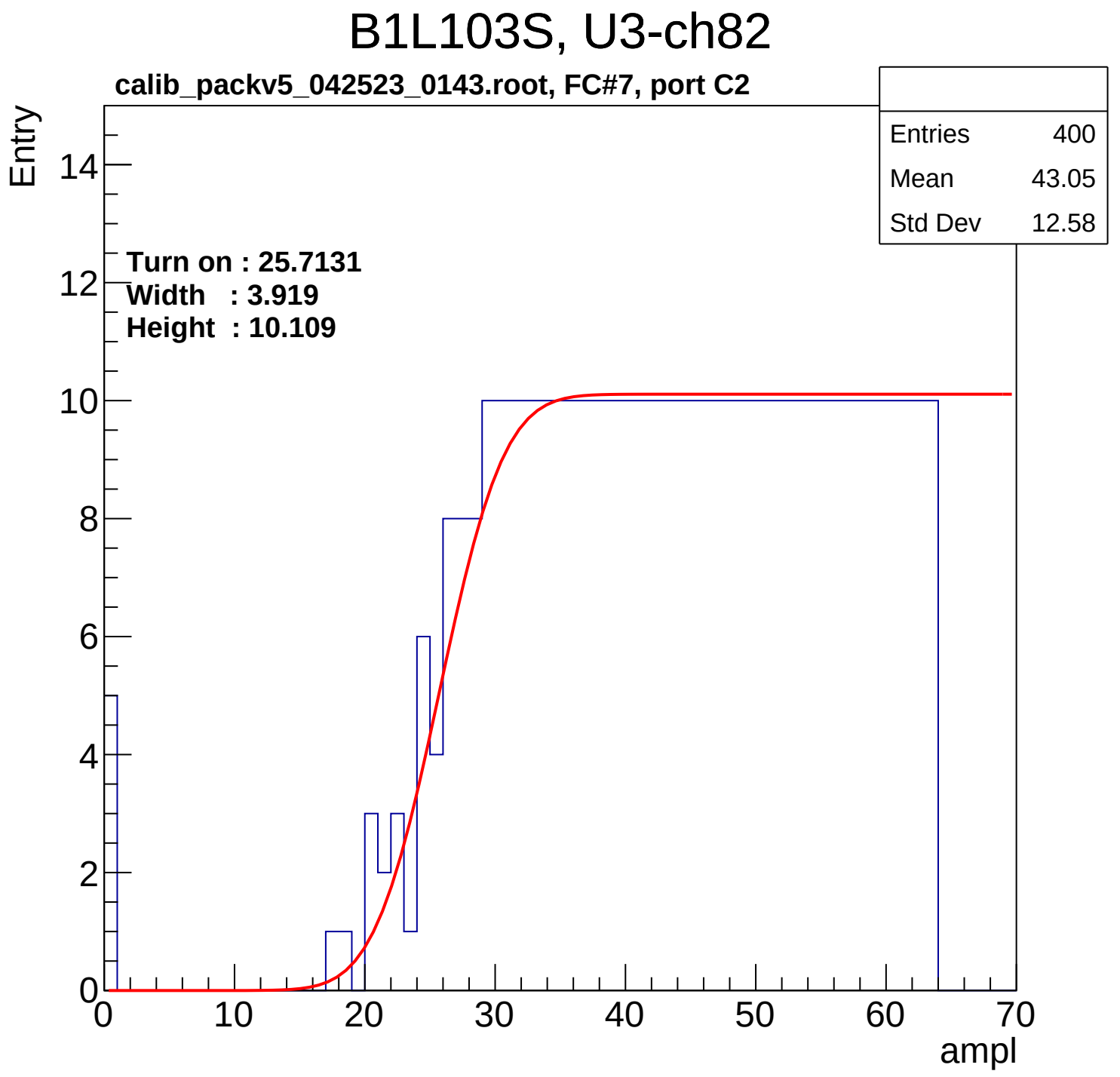
B1L103S, U3-ch82
calib_packv5_042523_0143.root, FC#7, port C2
Entries 400
Mean 43.05
Std Dev 12.58
Turn on : 25.7131
Width : 3.919
Height : 10.109
Entry
ampl
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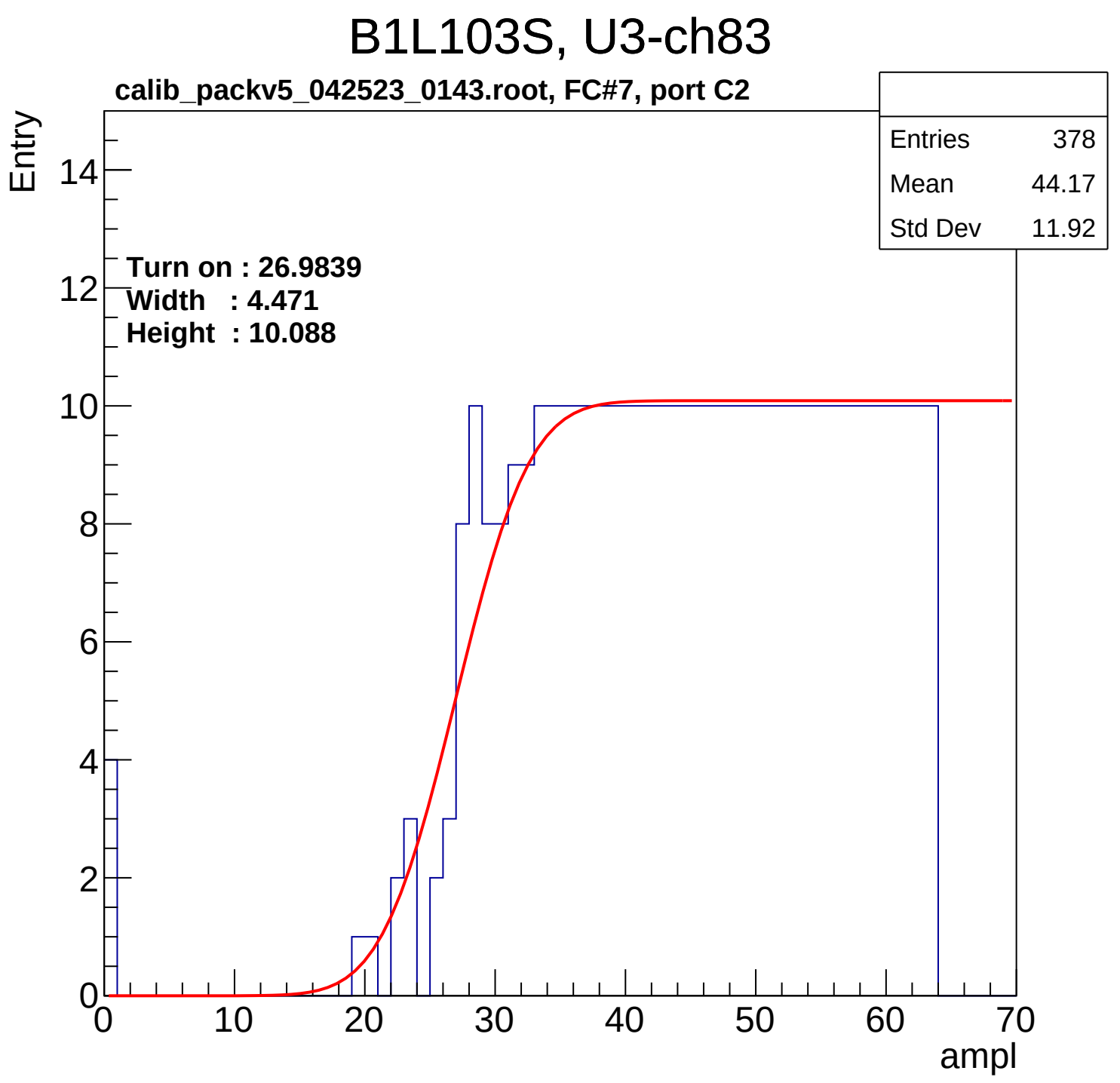
B1L103S, U3-ch83
calib_packv5_042523_0143.root, FC#7, port C2
Entries 378
Mean 44.17
Std Dev 11.92
Turn on : 26.9839
Width : 4.471
Height : 10.088
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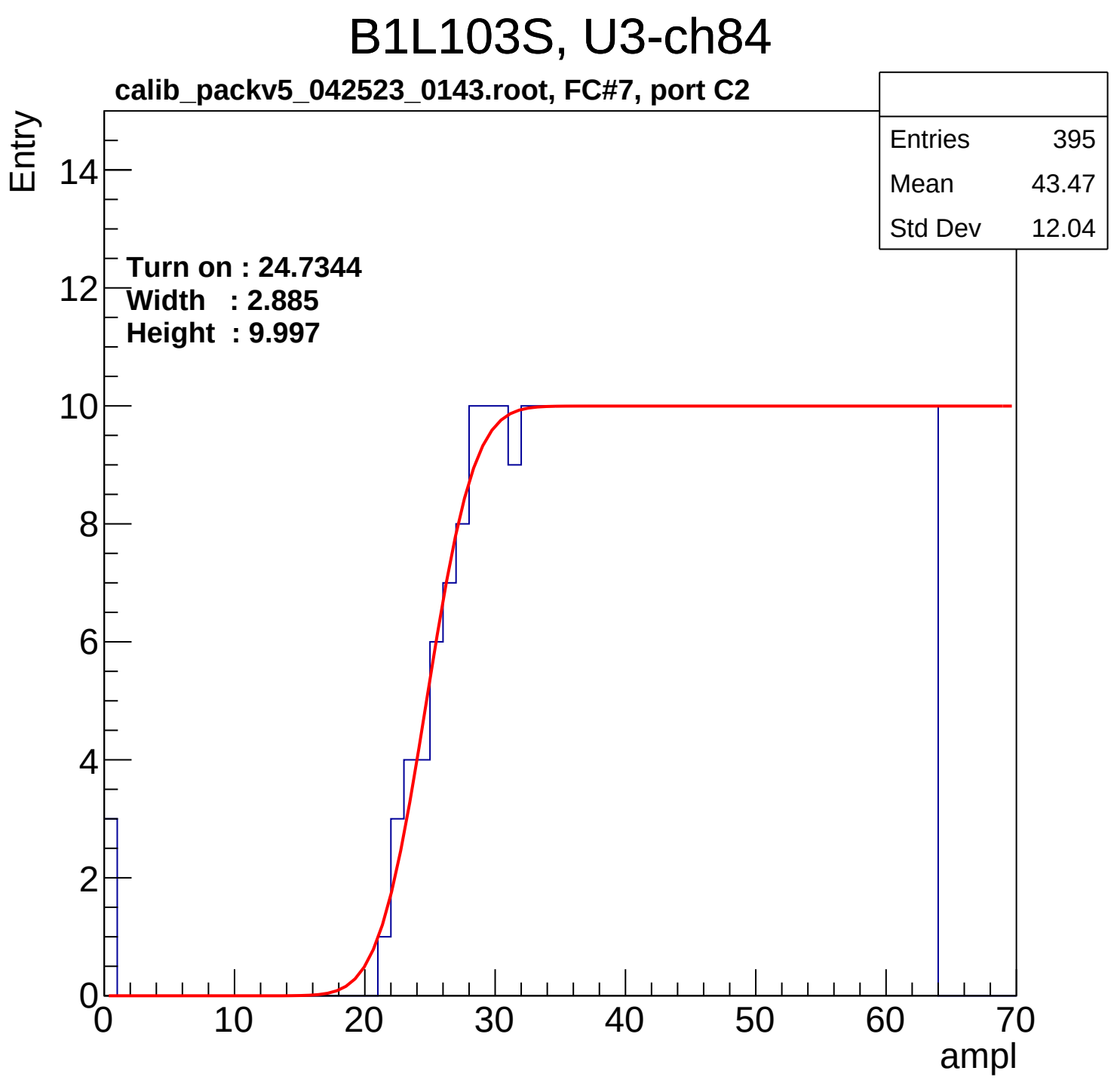
B1L103S, U3-ch84
calib_packv5_042523_0143.root, FC#7, port C2
Entries 395
Mean 43.47
Std Dev 12.04
Turn on : 24.7344
Width : 2.885
Height : 9.997
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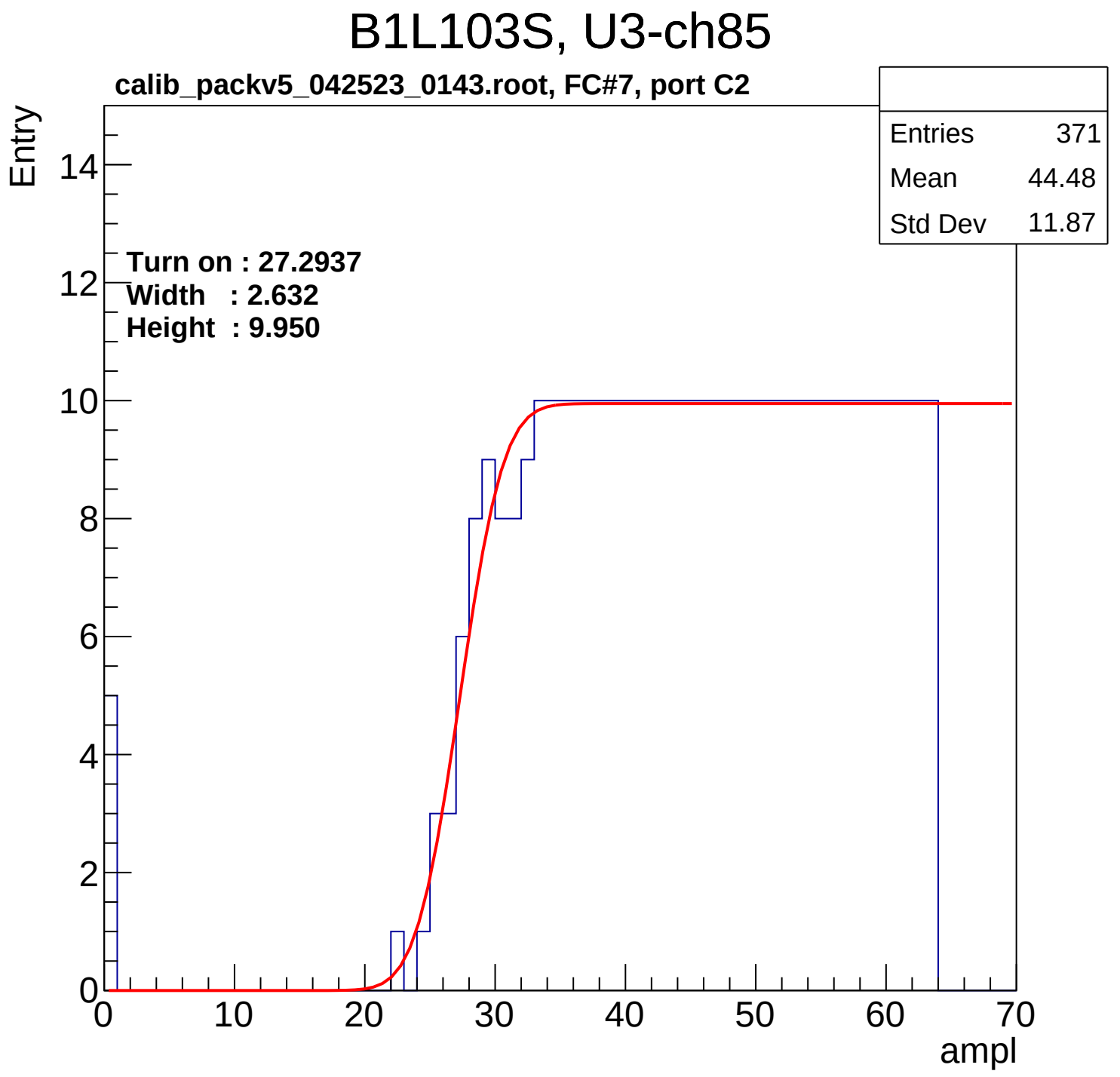
B1L103S, U3-ch85
calib_packv5_042523_0143.root, FC#7, port C2
Entries 371
Mean 44.48
Std Dev 11.87
Turn on : 27.2937
Width : 2.632
Height : 9.950
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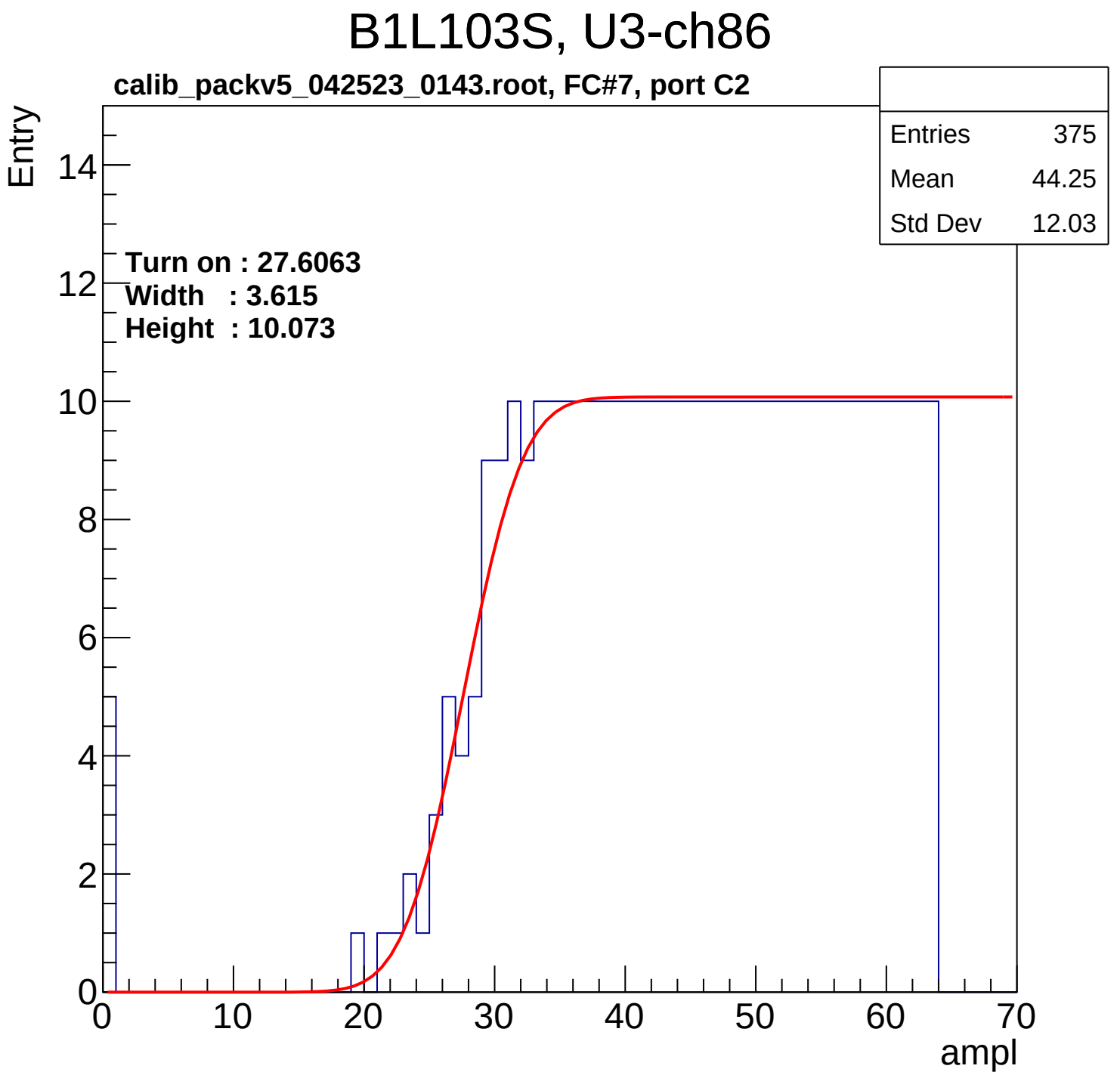
B1L103S, U3-ch86
calib_packv5_042523_0143.root, FC#7, port C2
Entries 375
Mean 44.25
Std Dev 12.03
Turn on : 27.6063
Width : 3.615
Height : 10.073
Entry
ampl
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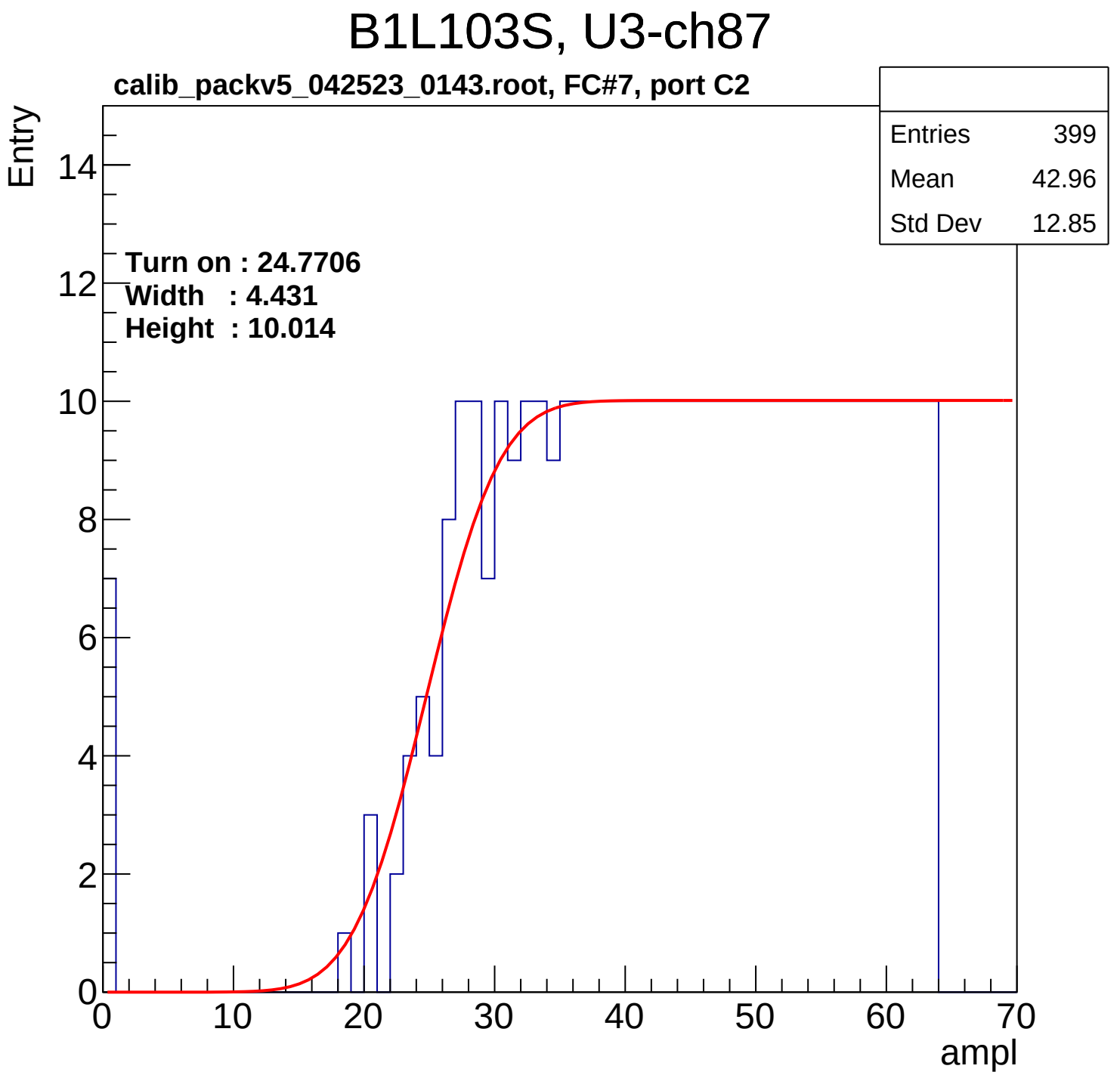
B1L103S, U3-ch87
calib_packv5_042523_0143.root, FC#7, port C2
Entries 399
Mean 42.96
Std Dev 12.85
Turn on : 24.7706
Width : 4.431
Height : 10.014
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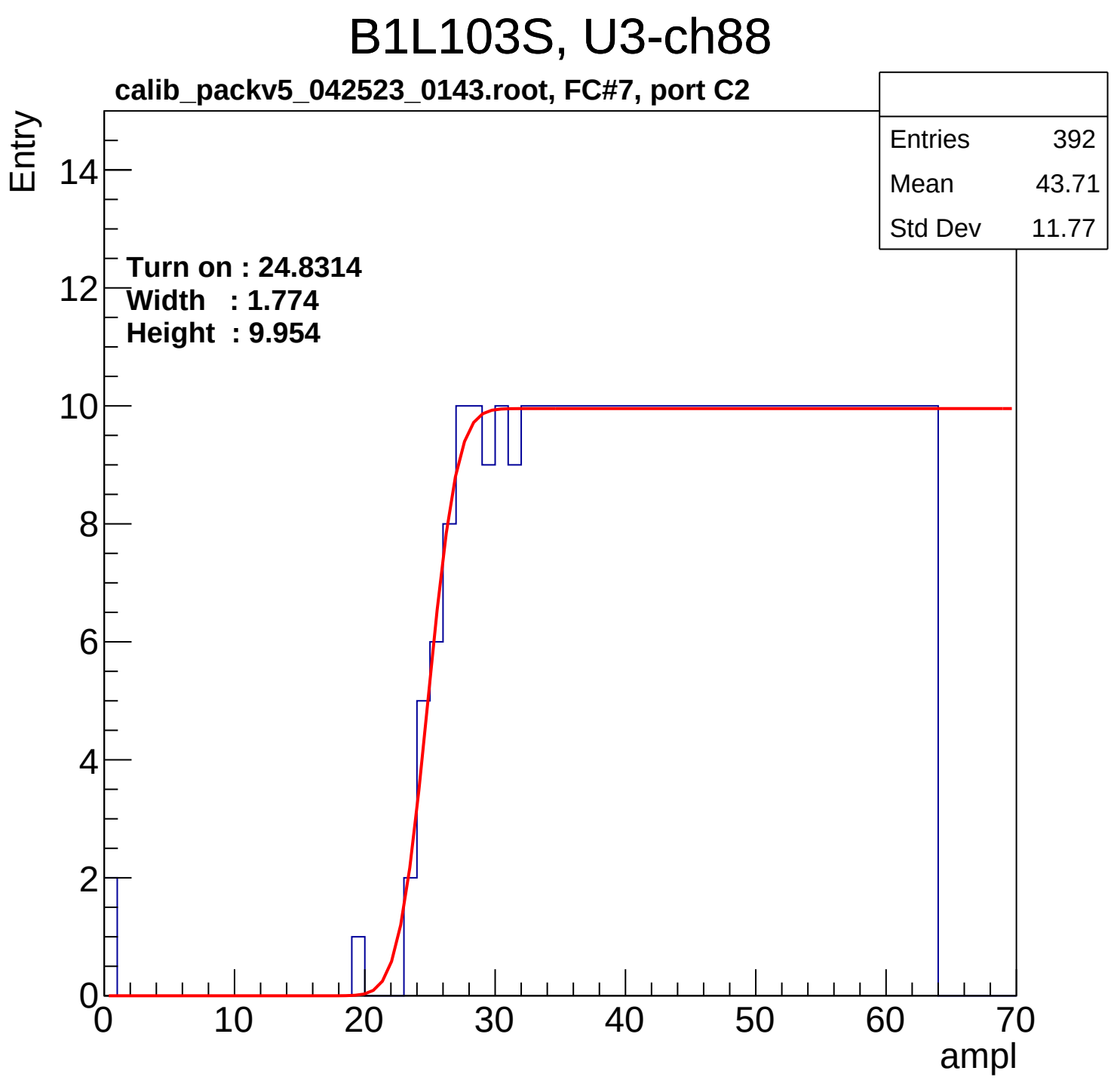
B1L103S, U3-ch88
calib_packv5_042523_0143.root, FC#7, port C2
Entries 392
Mean 43.71
Std Dev 11.77
Turn on : 24.8314
Width : 1.774
Height : 9.954
Entry
ampl
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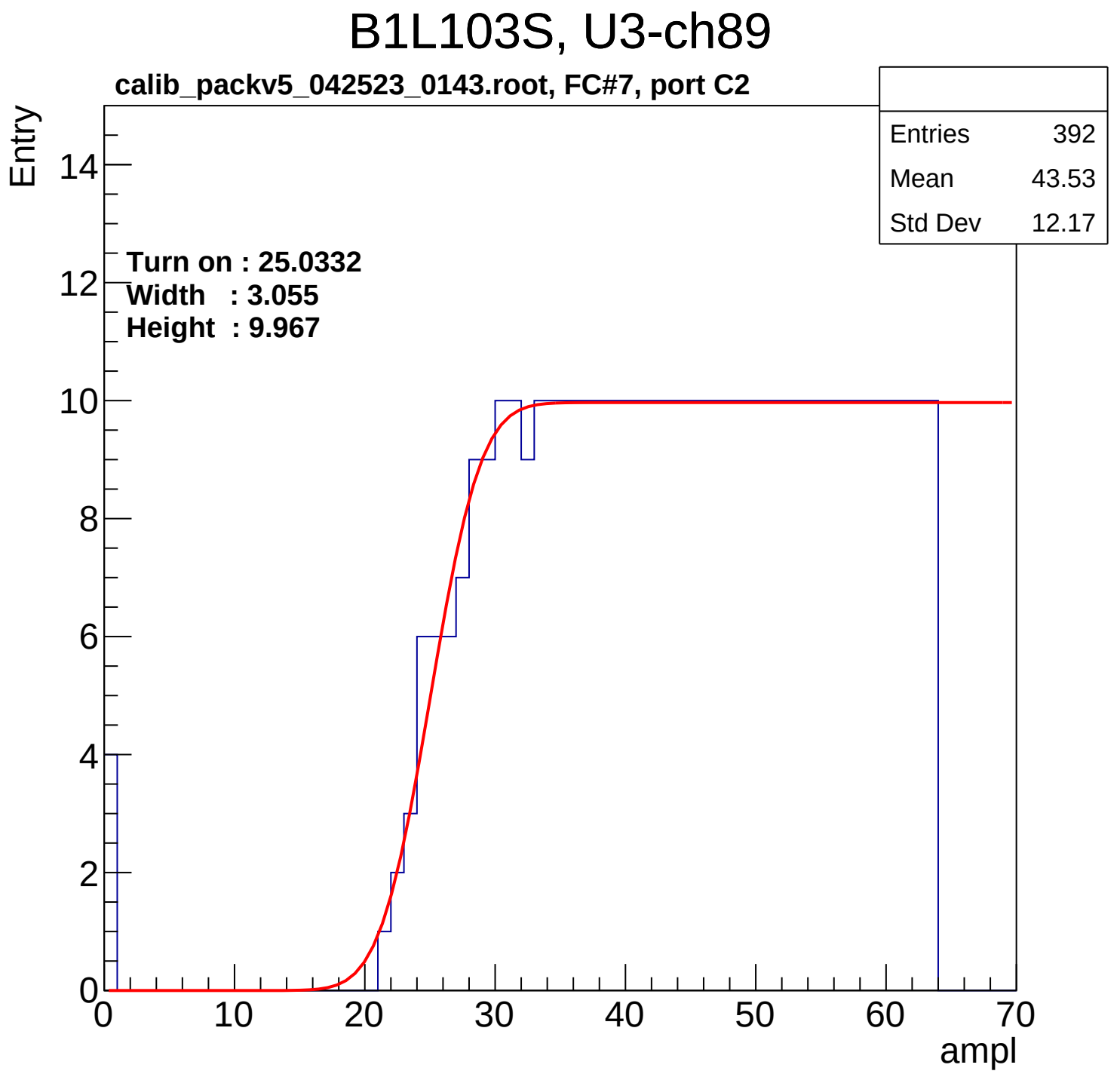
B1L103S, U3-ch89
calib_packv5_042523_0143.root, FC#7, port C2
Entries 392
Mean 43.53
Std Dev 12.17
Turn on : 25.0332
Width : 3.055
Height : 9.967
Entry
ampl
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4
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8
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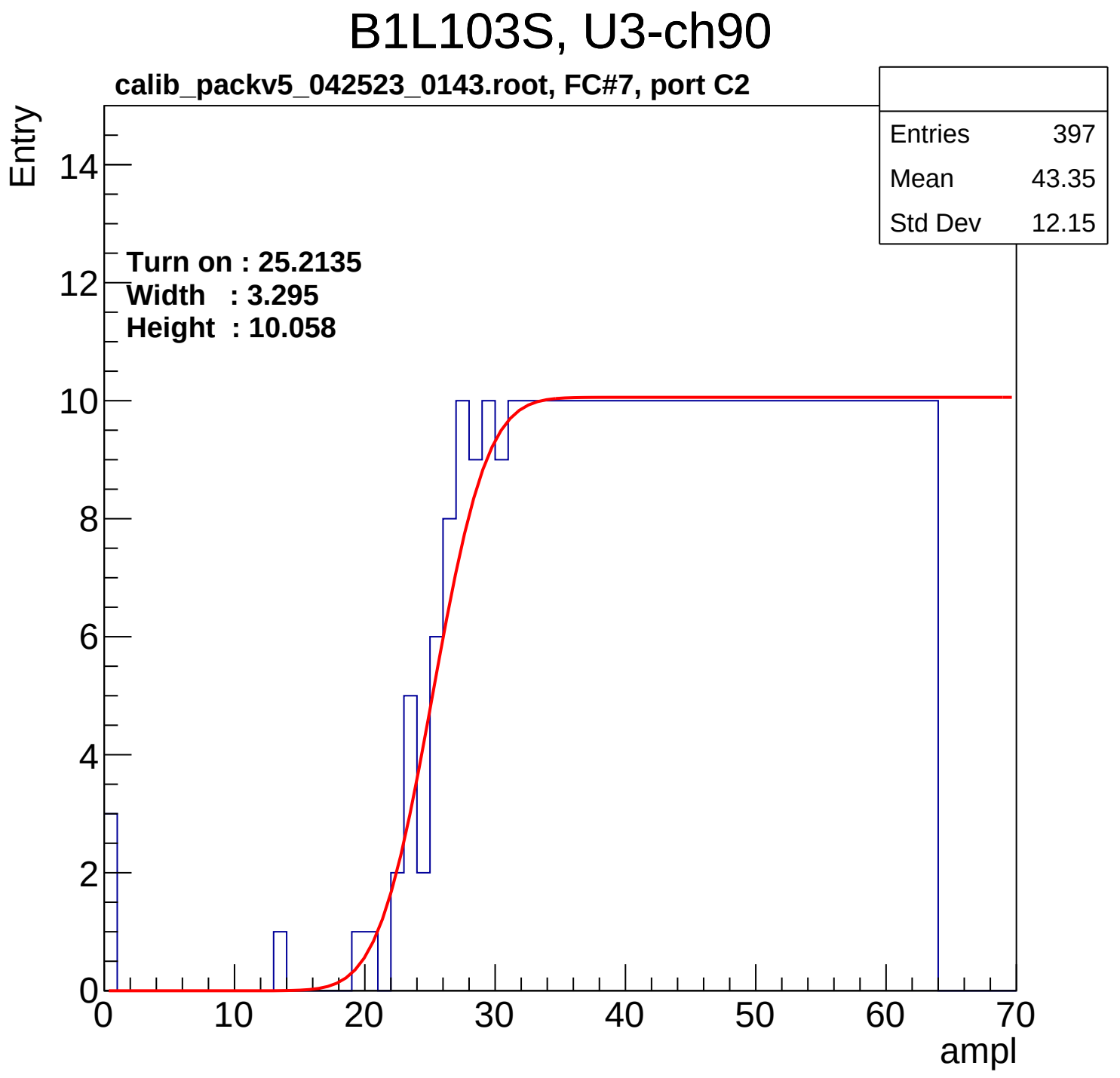
B1L103S, U3-ch90
calib_packv5_042523_0143.root, FC#7, port C2
Entries 397
Mean 43.35
Std Dev 12.15
Turn on : 25.2135
Width : 3.295
Height : 10.058
Entry
ampl
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4
6
8
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12
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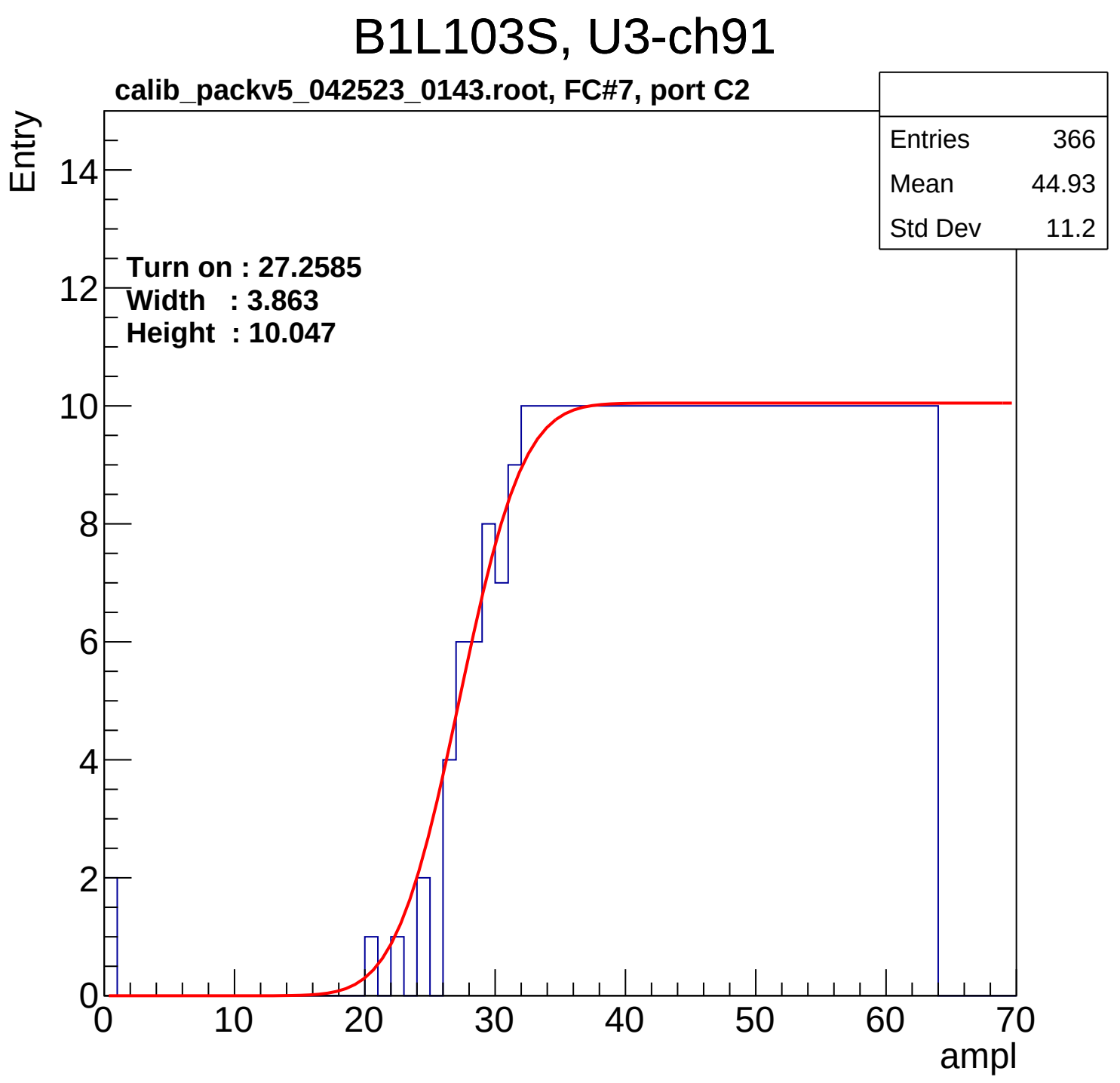
B1L103S, U3-ch91
calib_packv5_042523_0143.root, FC#7, port C2
Entries 366
Mean 44.93
Std Dev 11.2
Turn on : 27.2585
Width : 3.863
Height : 10.047
Entry
ampl
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2
4
6
8
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12
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0
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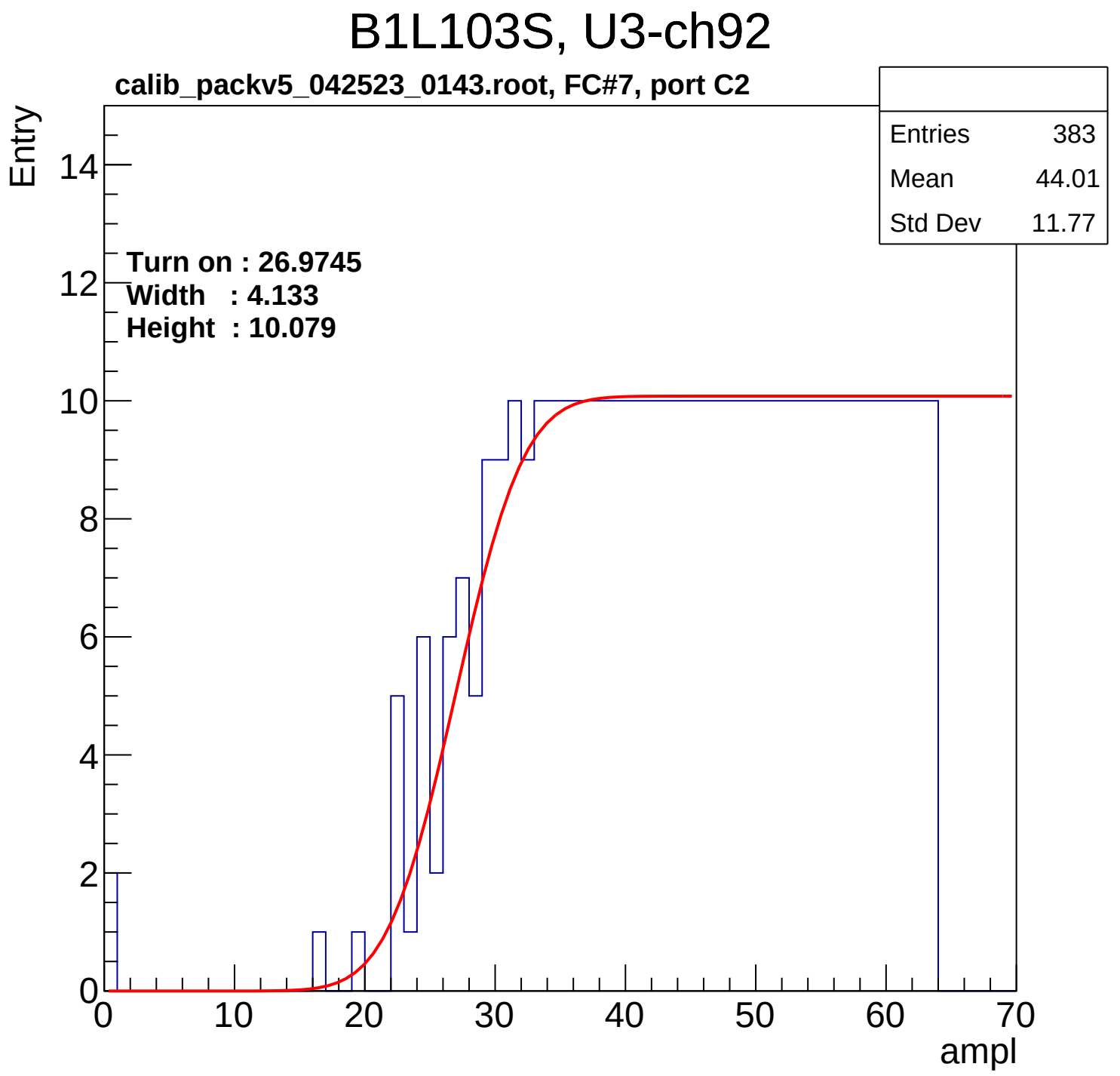
B1L103S, U3-ch92
calib_packv5_042523_0143.root, FC#7, port C2
Entries 383
Mean 44.01
Std Dev 11.77
Turn on : 26.9745
Width : 4.133
Height : 10.079
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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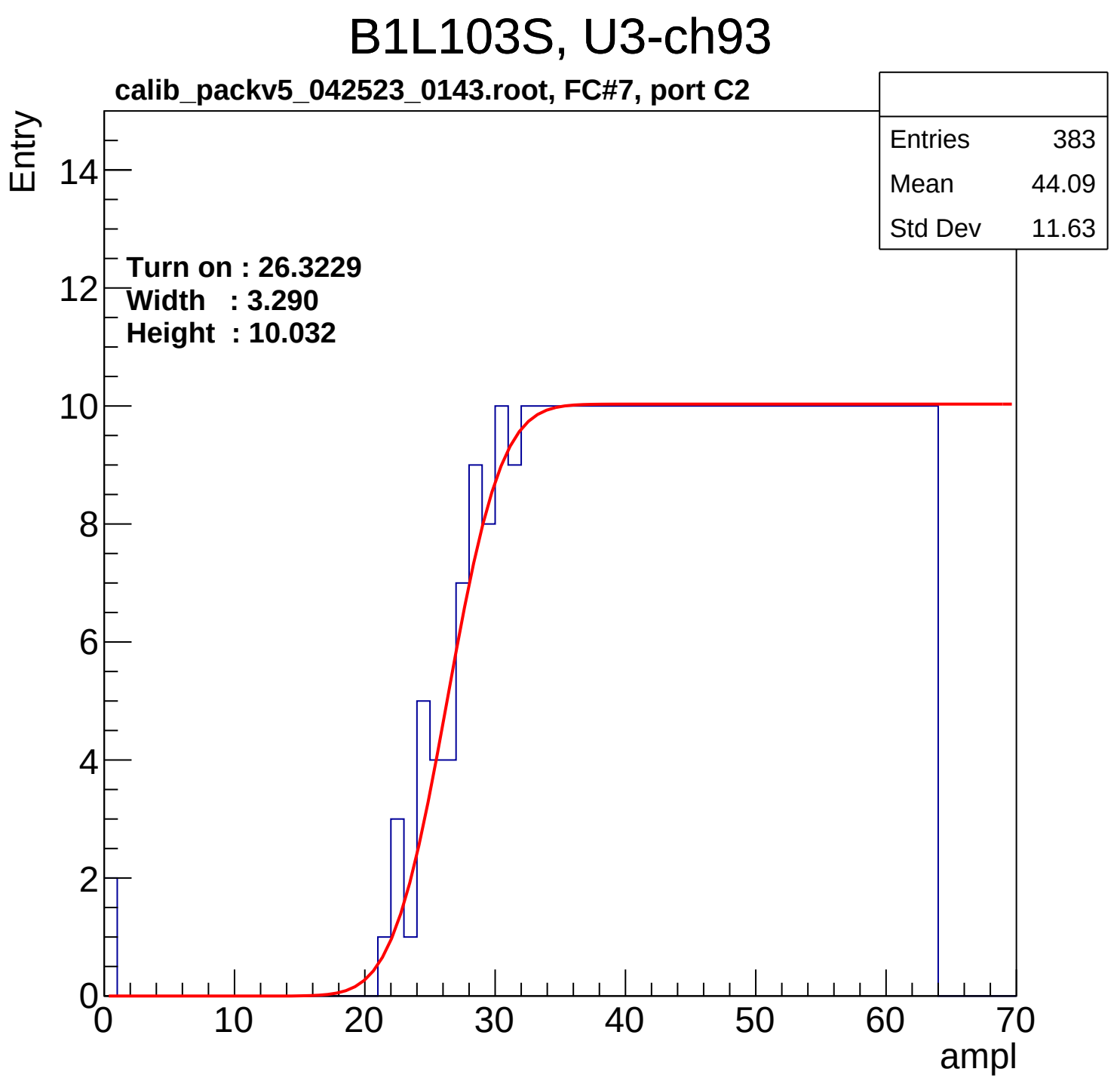
B1L103S, U3-ch93
calib_packv5_042523_0143.root, FC#7, port C2
Entries 383
Mean 44.09
Std Dev 11.63
Turn on : 26.3229
Width : 3.290
Height : 10.032
Entry
ampl
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2
4
6
8
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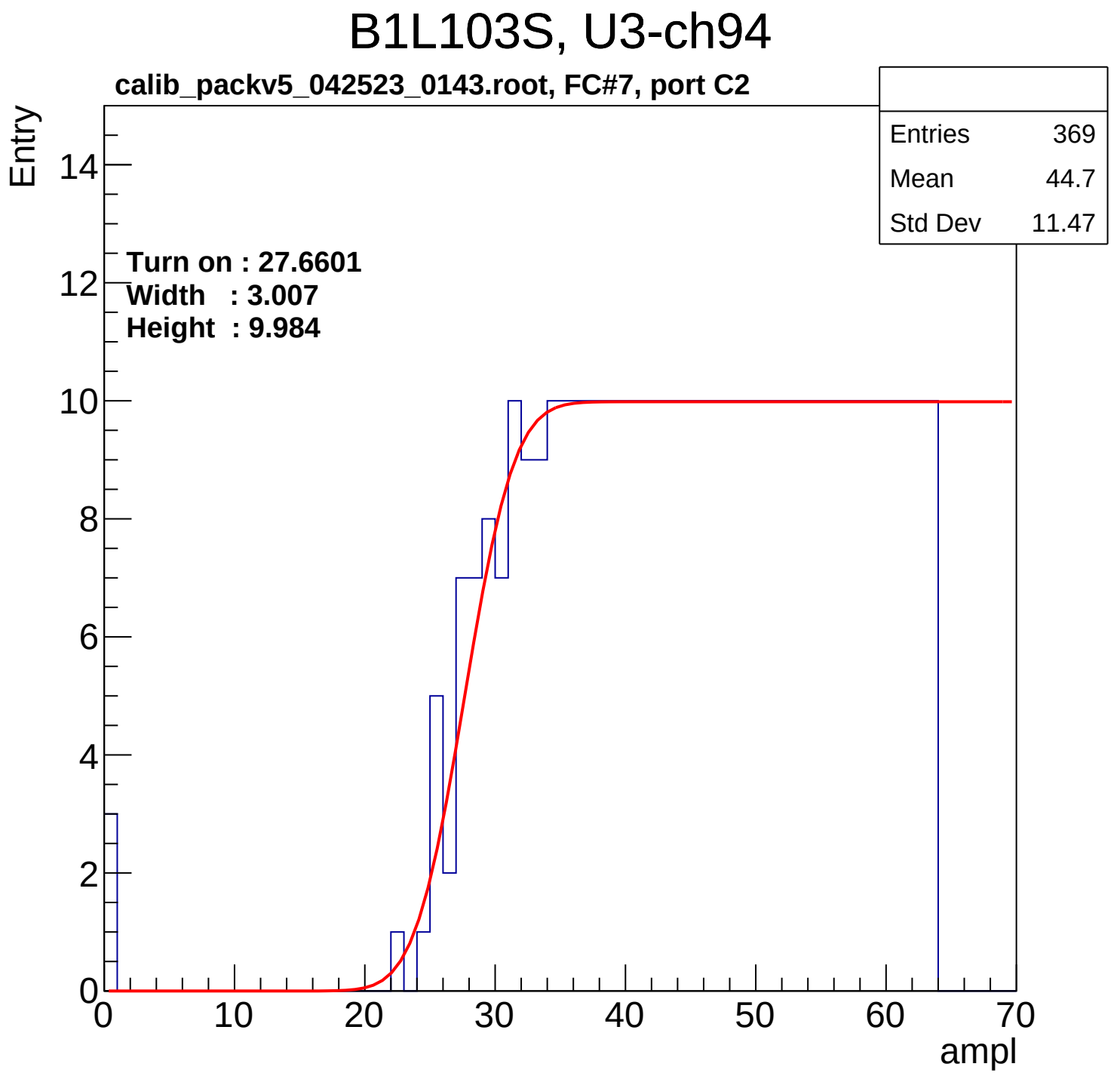
B1L103S, U3-ch94
calib_packv5_042523_0143.root, FC#7, port C2
Entries 369
Mean 44.7
Std Dev 11.47
Turn on : 27.6601
Width : 3.007
Height : 9.984
Entry
ampl
0
2
4
6
8
10
12
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60
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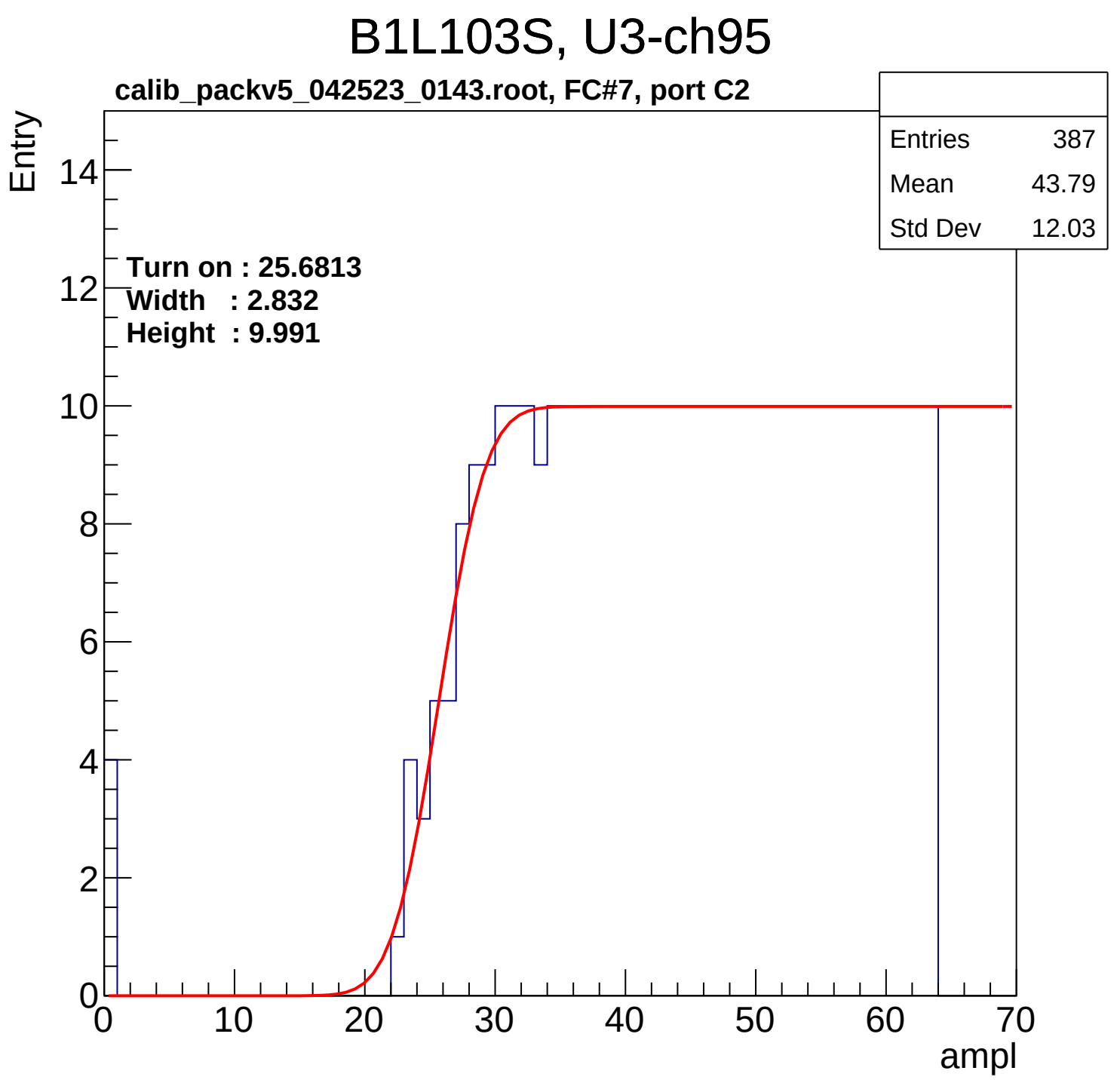
B1L103S, U3-ch95
calib_packv5_042523_0143.root, FC#7, port C2
Entries 387
Mean 43.79
Std Dev 12.03
Turn on : 25.6813
Width : 2.832
Height : 9.991
Entry
ampl
0
2
4
6
8
10
12
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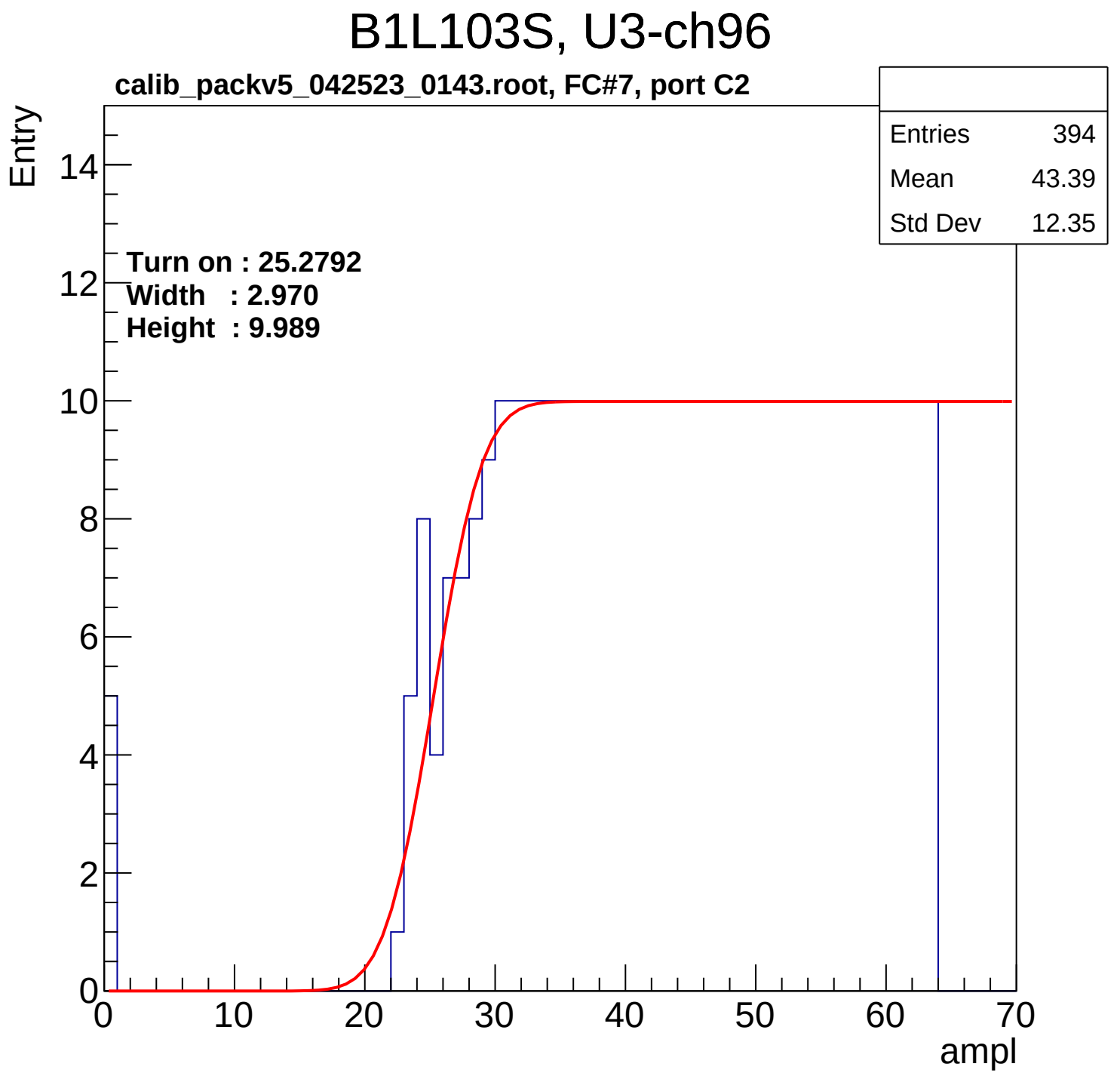
B1L103S, U3-ch96
calib_packv5_042523_0143.root, FC#7, port C2
Entries 394
Mean 43.39
Std Dev 12.35
Turn on : 25.2792
Width : 2.970
Height : 9.989
Entry
ampl
0
2
4
6
8
10
12
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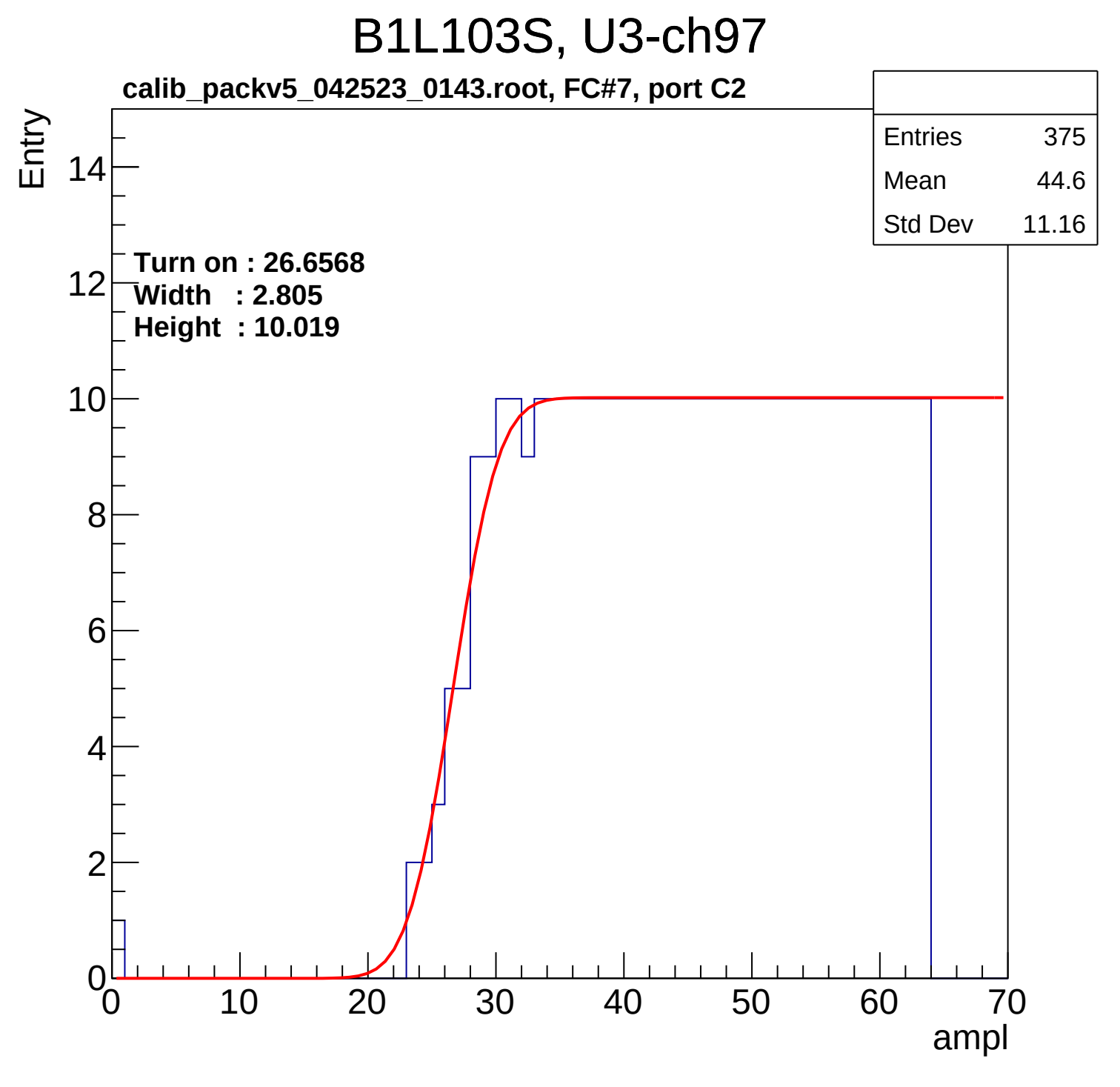
B1L103S, U3-ch97
calib_packv5_042523_0143.root, FC#7, port C2
Entries 375
Mean 44.6
Std Dev 11.16
Turn on : 26.6568
Width : 2.805
Height : 10.019
Entry
ampl
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4
6
8
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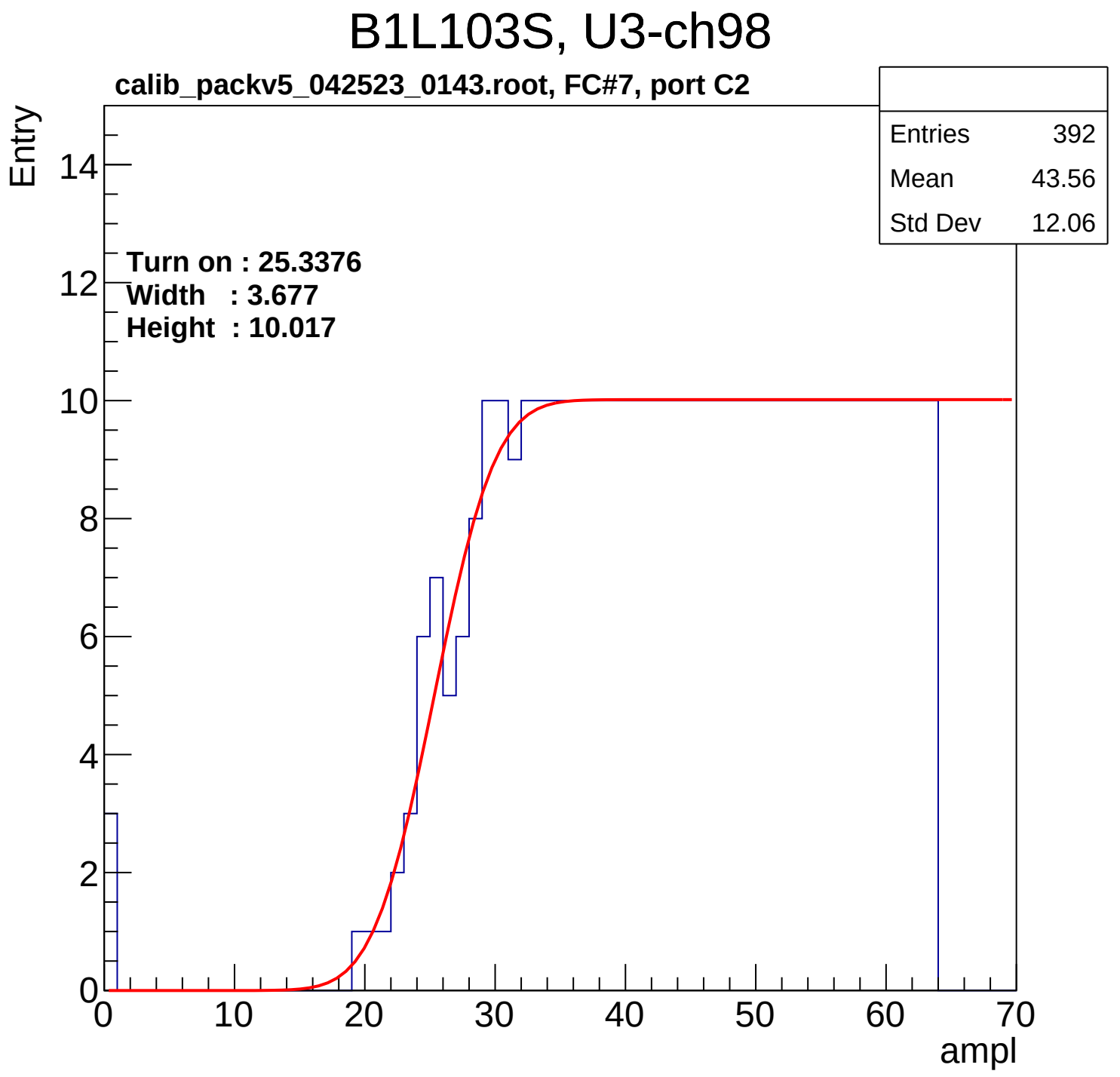
B1L103S, U3-ch98
calib_packv5_042523_0143.root, FC#7, port C2
Entries 392
Mean 43.56
Std Dev 12.06
Turn on : 25.3376
Width : 3.677
Height : 10.017
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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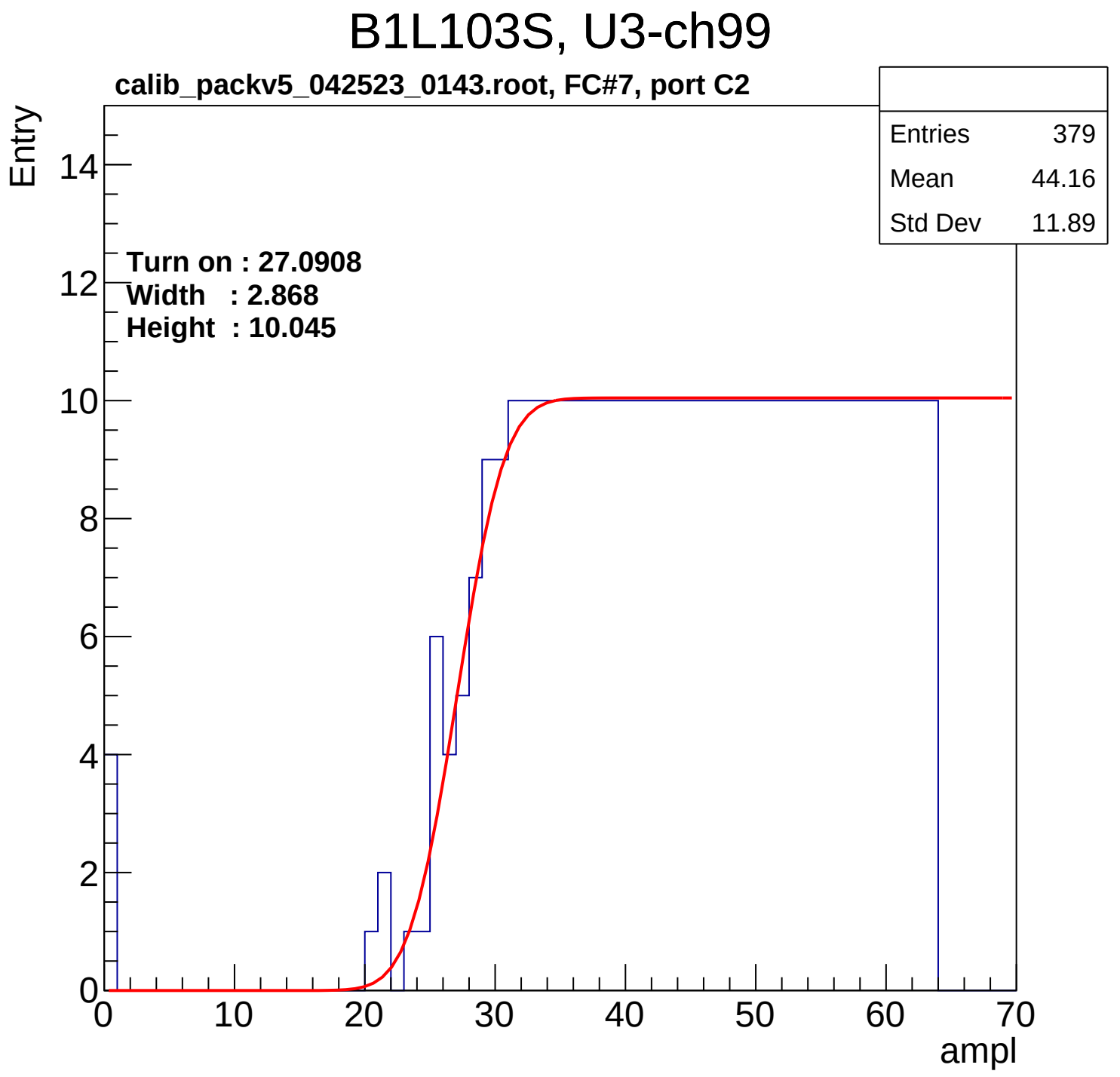
B1L103S, U3-ch99
calib_packv5_042523_0143.root, FC#7, port C2
Entries 379
Mean 44.16
Std Dev 11.89
Turn on : 27.0908
Width : 2.868
Height : 10.045
Entry
ampl
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6
8
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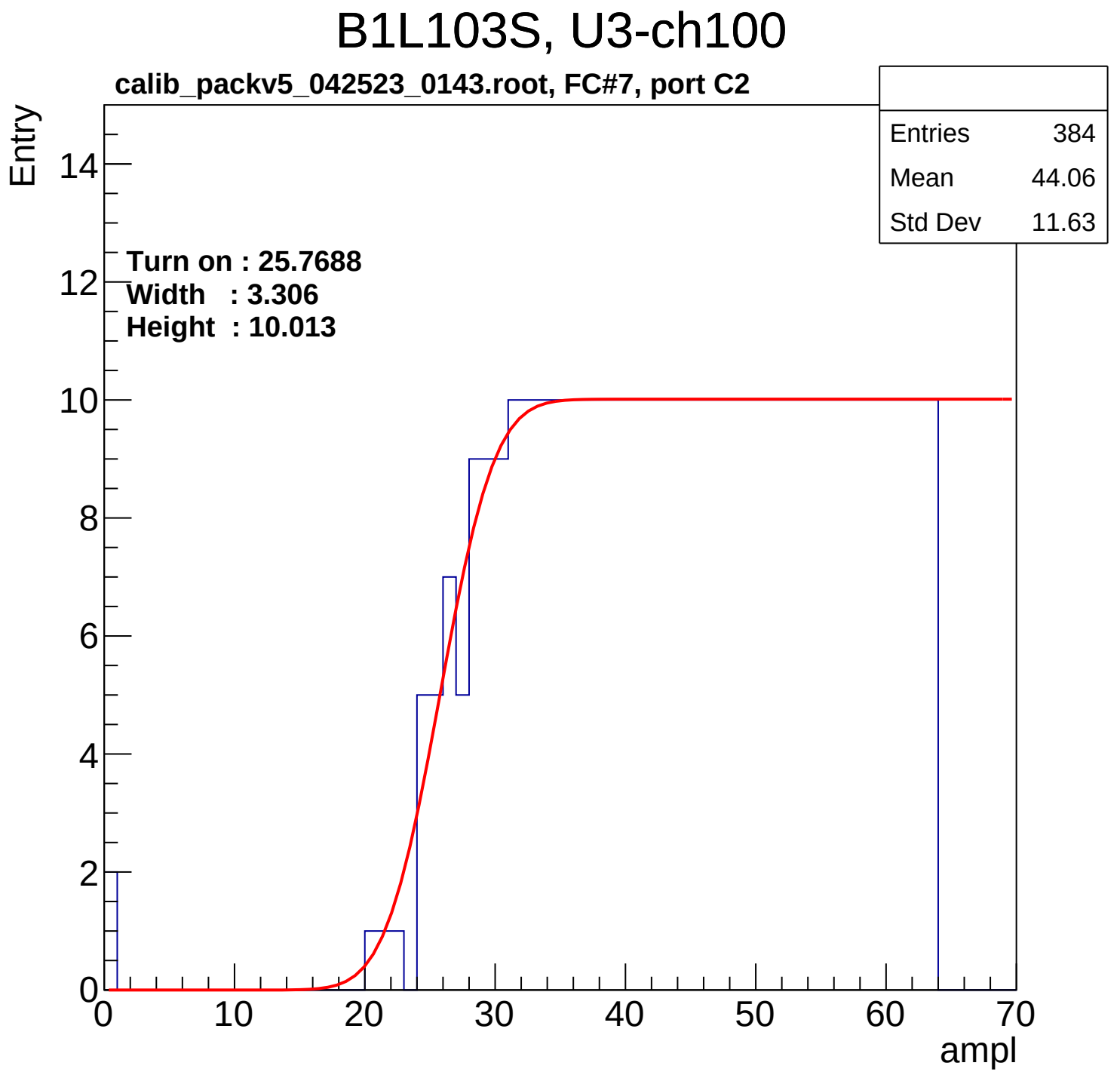
B1L103S, U3-ch100
calib_packv5_042523_0143.root, FC#7, port C2
Entries 384
Mean 44.06
Std Dev 11.63
Turn on : 25.7688
Width : 3.306
Height : 10.013
Entry
ampl
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6
8
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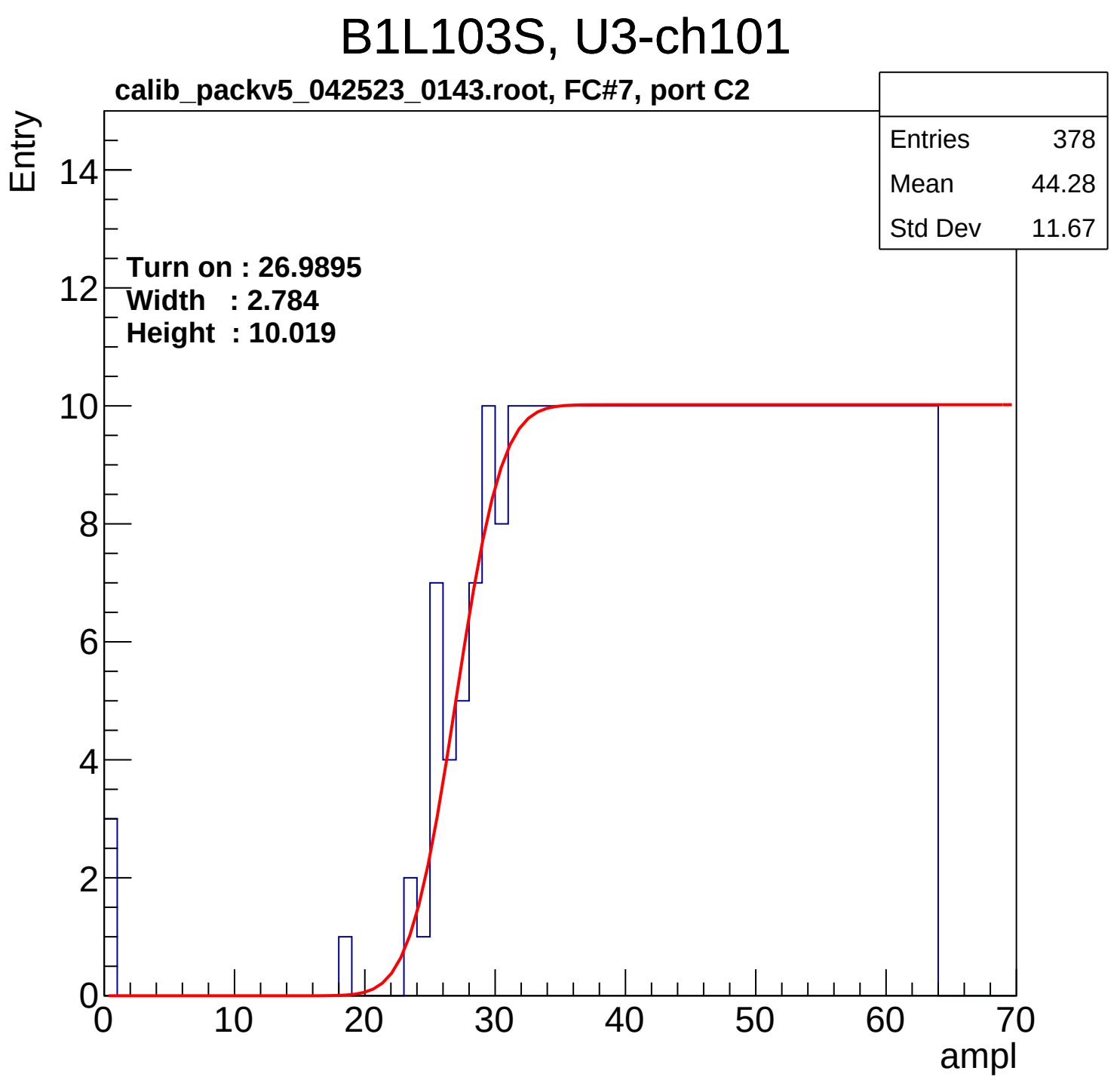
B1L103S, U3-ch101
calib_packv5_042523_0143.root, FC#7, port C2
Entries 378
Mean 44.28
Std Dev 11.67
Turn on : 26.9895
Width : 2.784
Height : 10.019
Entry
ampl
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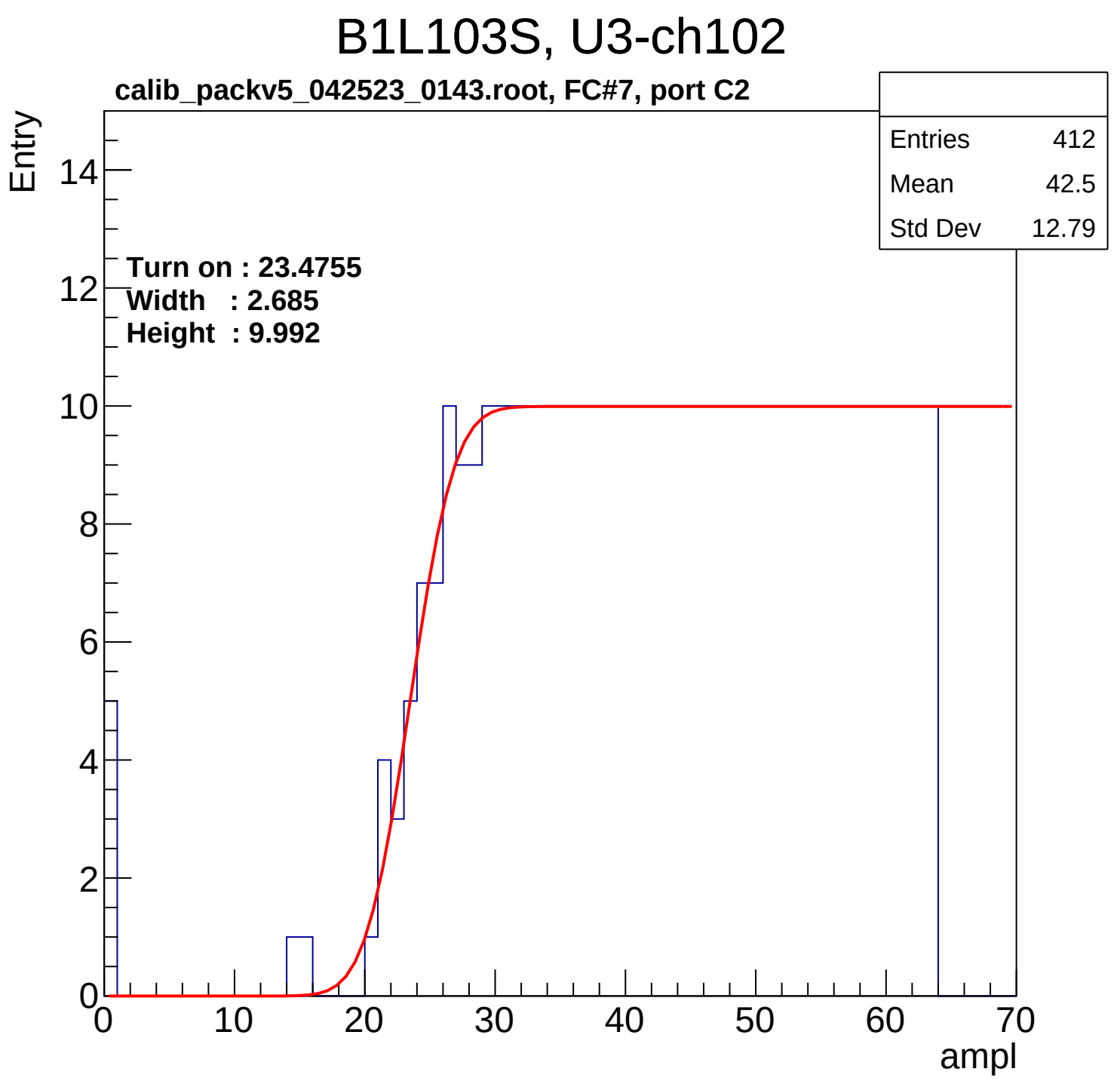
B1L103S, U3-ch102
calib_packv5_042523_0143.root, FC#7, port C2
Entries 412
Mean 42.5
Std Dev 12.79
Turn on : 23.4755
Width : 2.685
Height : 9.992
Entry
ampl
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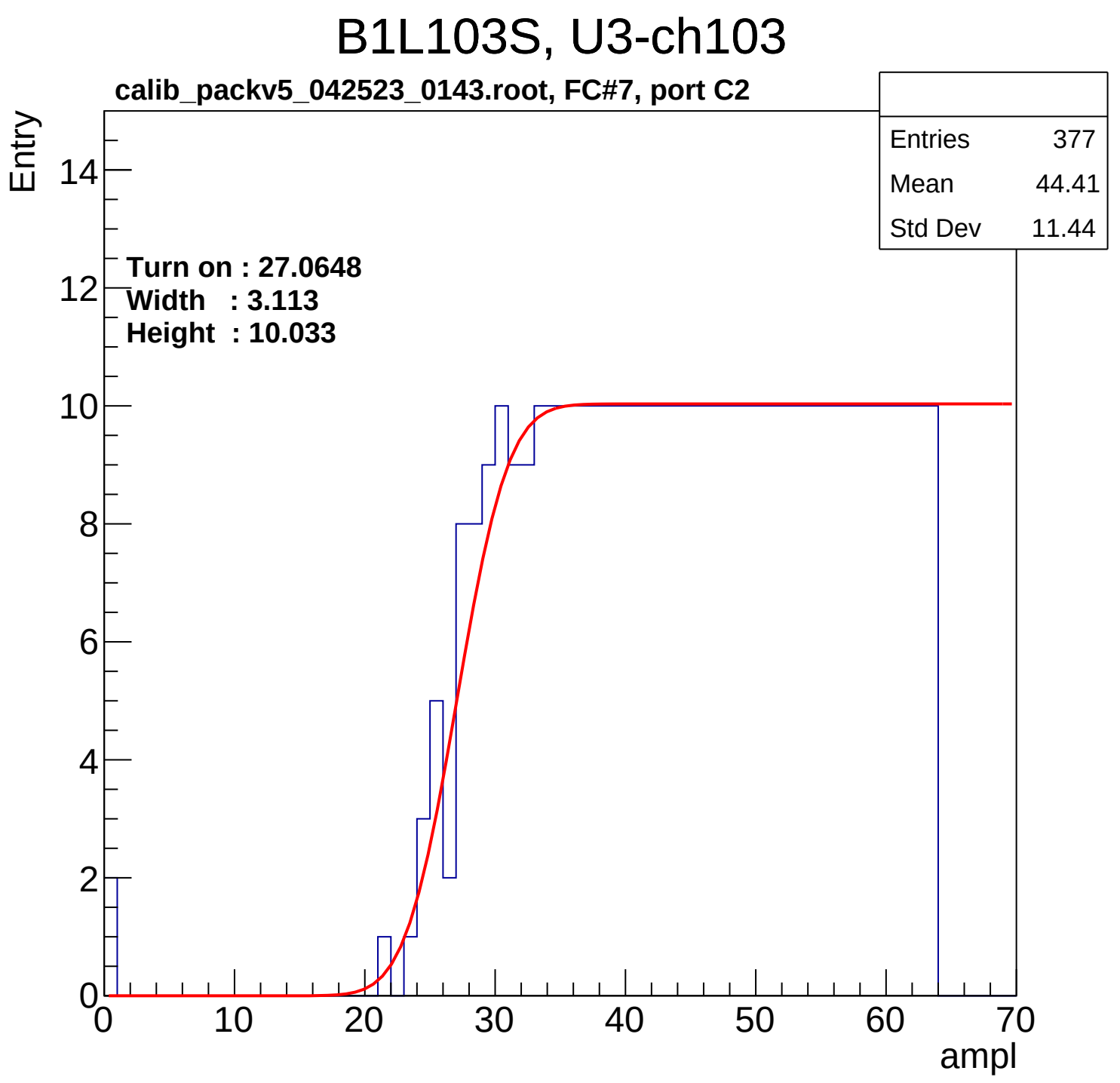
B1L103S, U3-ch103
calib_packv5_042523_0143.root, FC#7, port C2
Entries 377
Mean 44.41
Std Dev 11.44
Turn on : 27.0648
Width : 3.113
Height : 10.033
Entry
ampl
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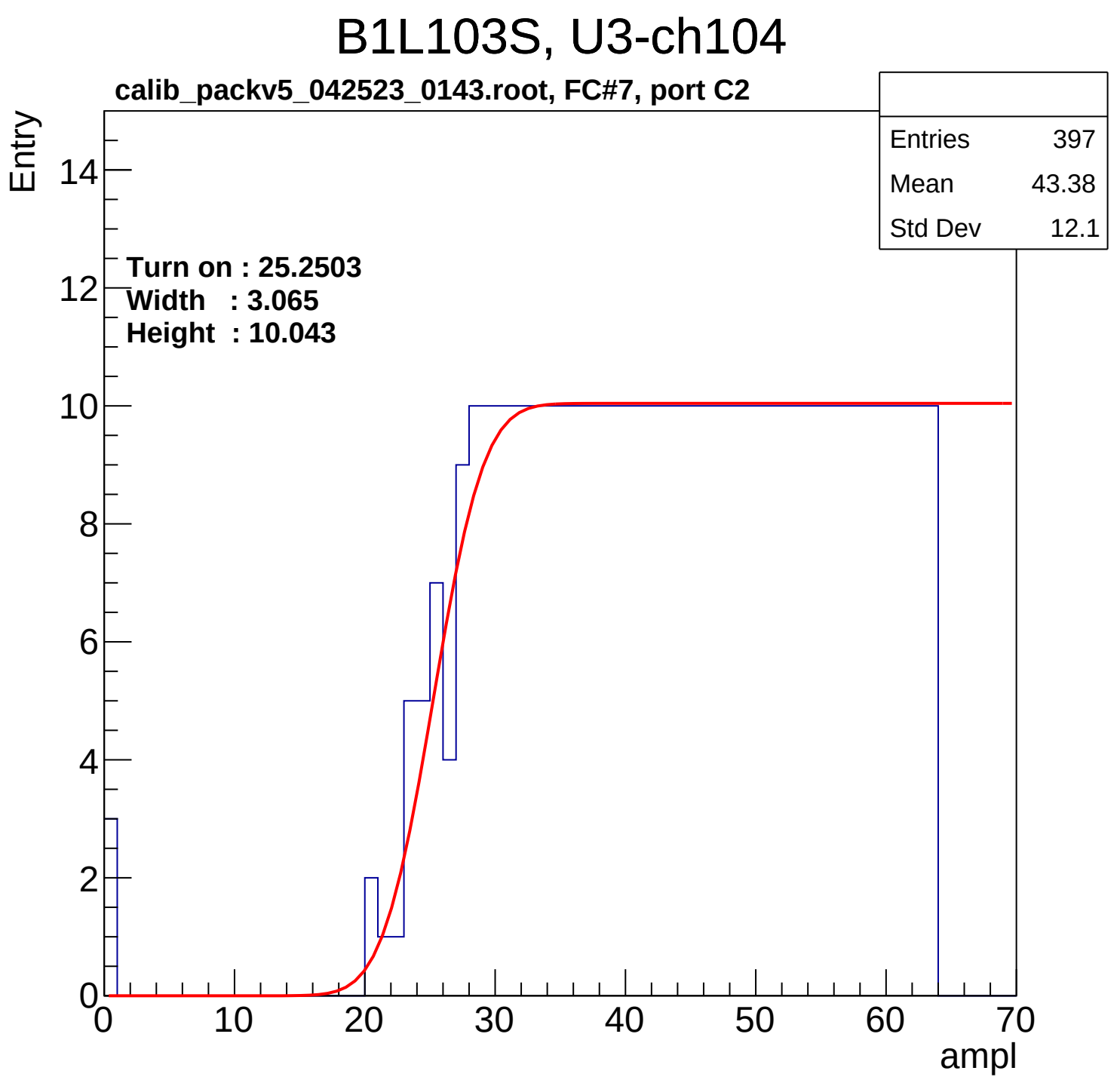
B1L103S, U3-ch104
calib_packv5_042523_0143.root, FC#7, port C2
Entries 397
Mean 43.38
Std Dev 12.1
Turn on : 25.2503
Width : 3.065
Height : 10.043
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ampl
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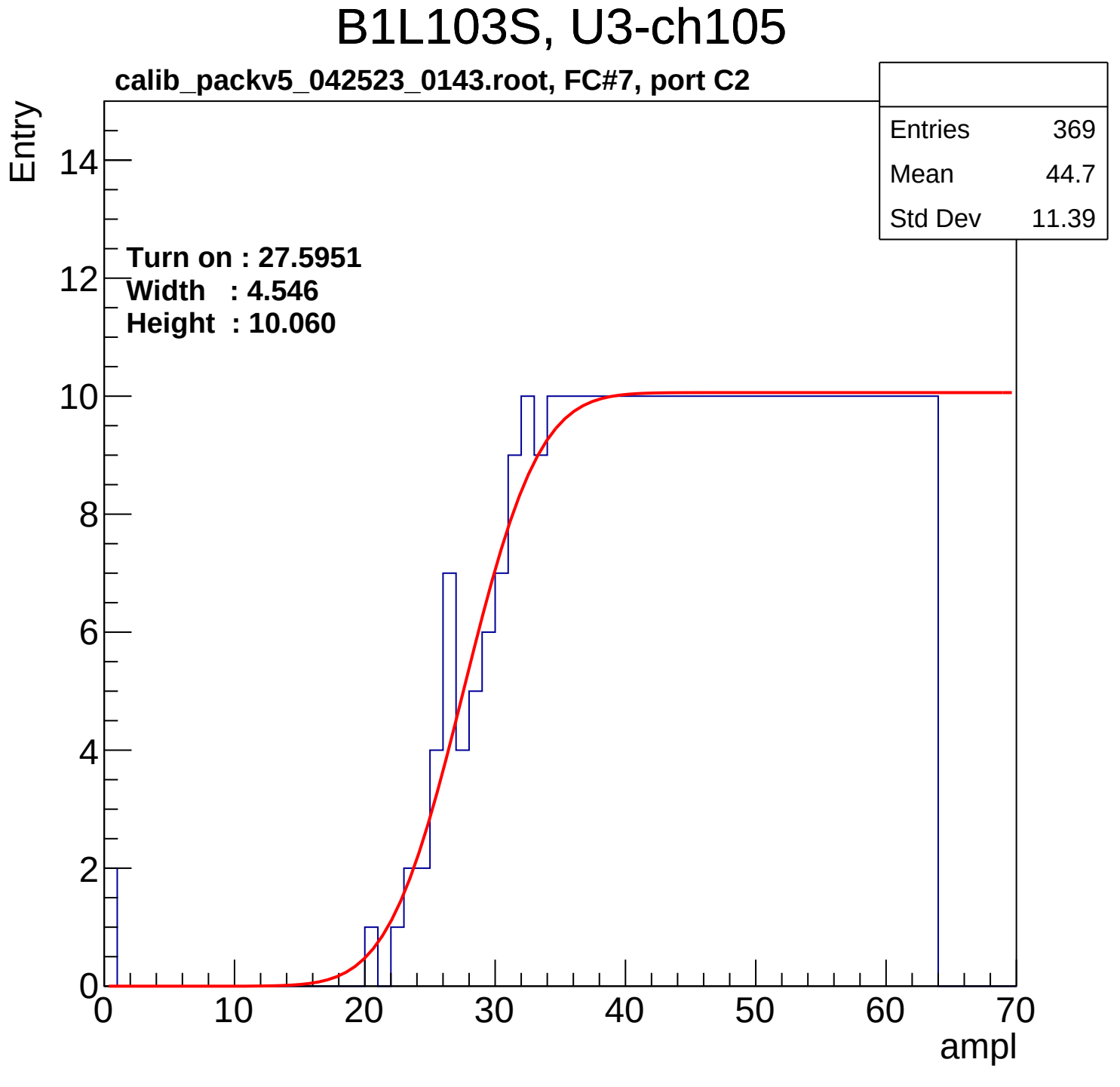
B1L103S, U3-ch105
calib_packv5_042523_0143.root, FC#7, port C2
Entries 369
Mean 44.7
Std Dev 11.39
Turn on : 27.5951
Width : 4.546
Height : 10.060
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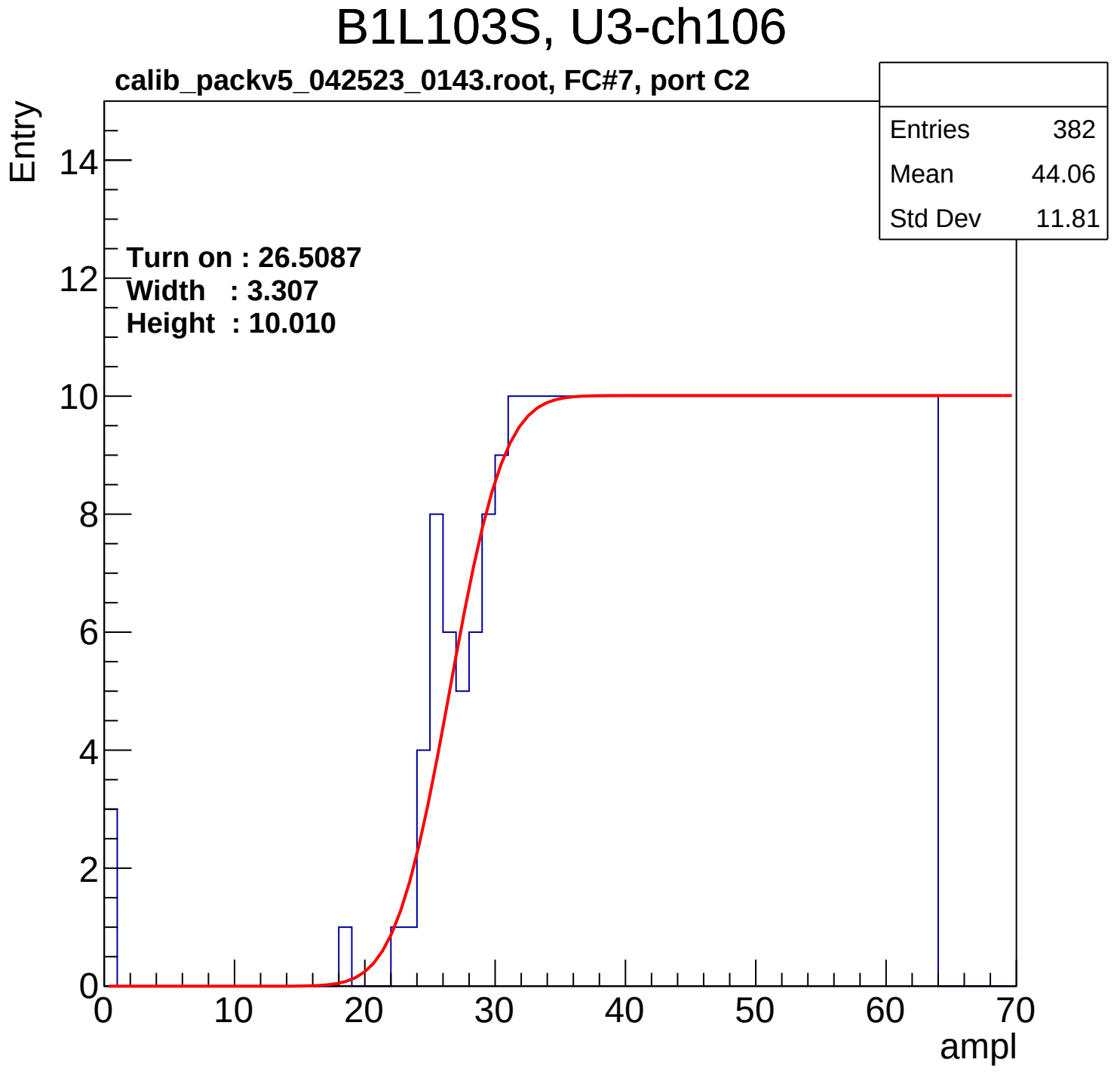
B1L103S, U3-ch106
calib_packv5_042523_0143.root, FC#7, port C2
Entries 382
Mean 44.06
Std Dev 11.81
Turn on : 26.5087
Width : 3.307
Height : 10.010
Entry
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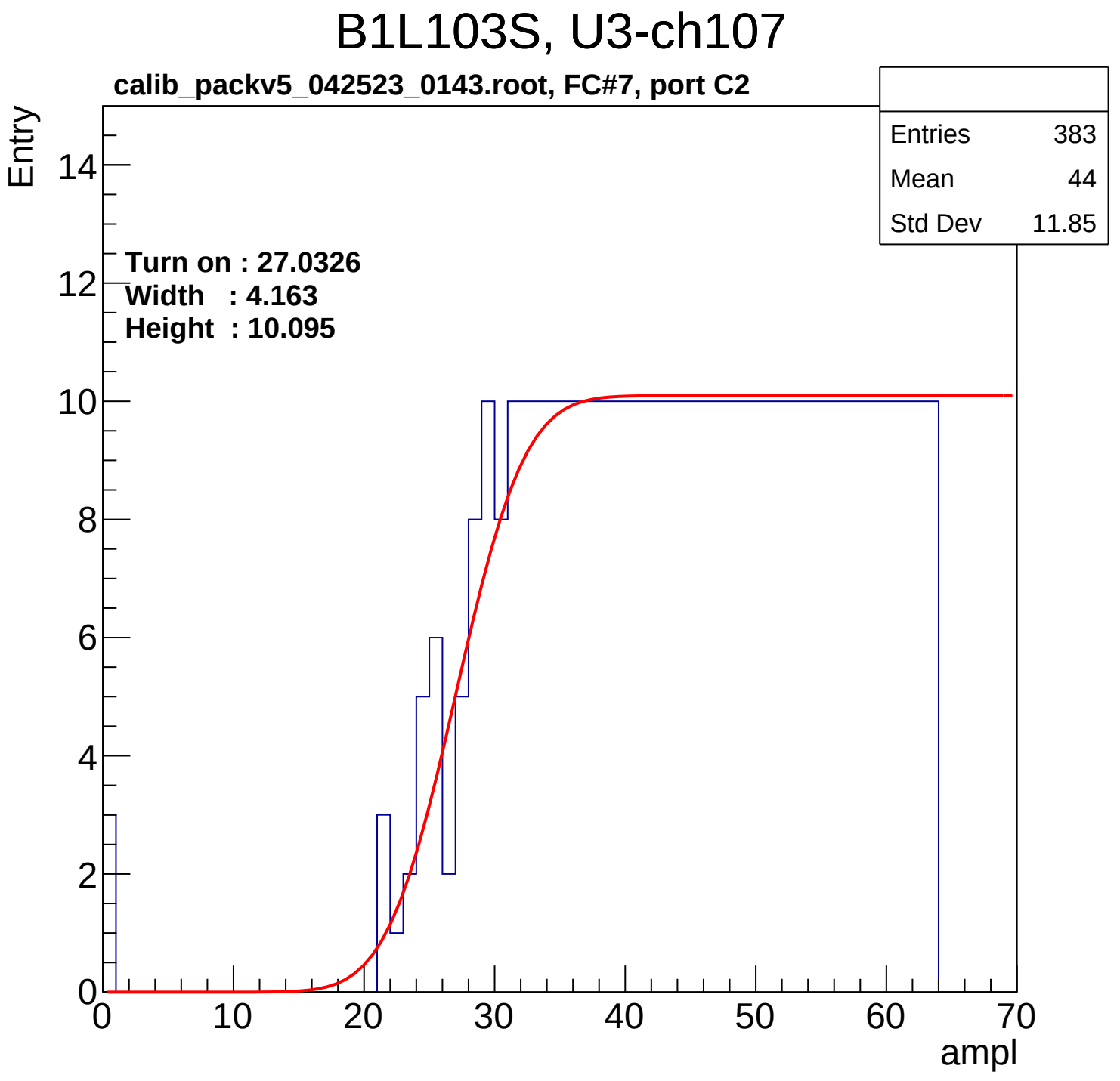
B1L103S, U3-ch107
calib_packv5_042523_0143.root, FC#7, port C2
Entries 383
Mean 44
Std Dev 11.85
Turn on : 27.0326
Width : 4.163
Height : 10.095
Entry
ampl
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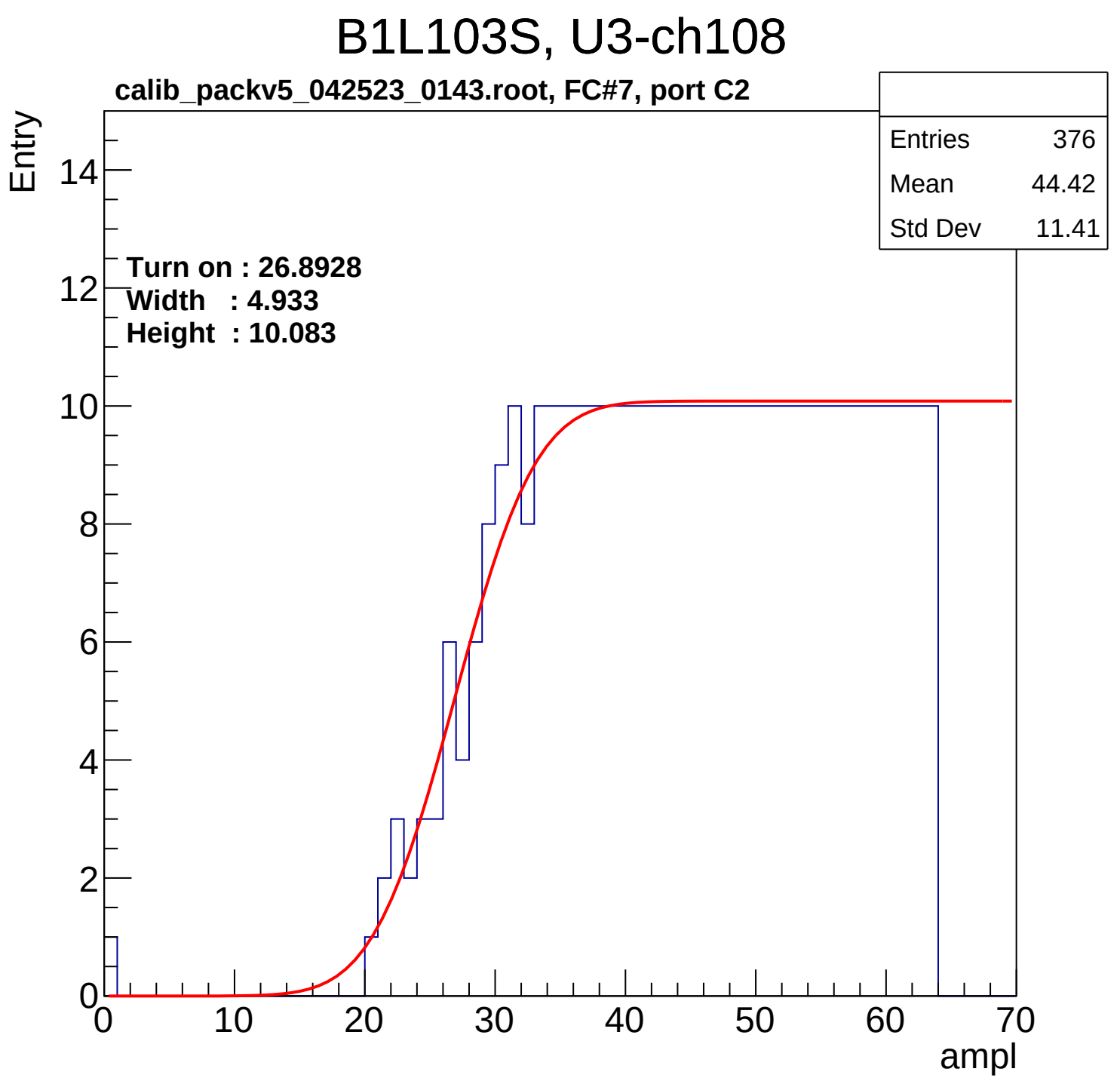
B1L103S, U3-ch108
calib_packv5_042523_0143.root, FC#7, port C2
Entries 376
Mean 44.42
Std Dev 11.41
Turn on : 26.8928
Width : 4.933
Height : 10.083
Entry
ampl
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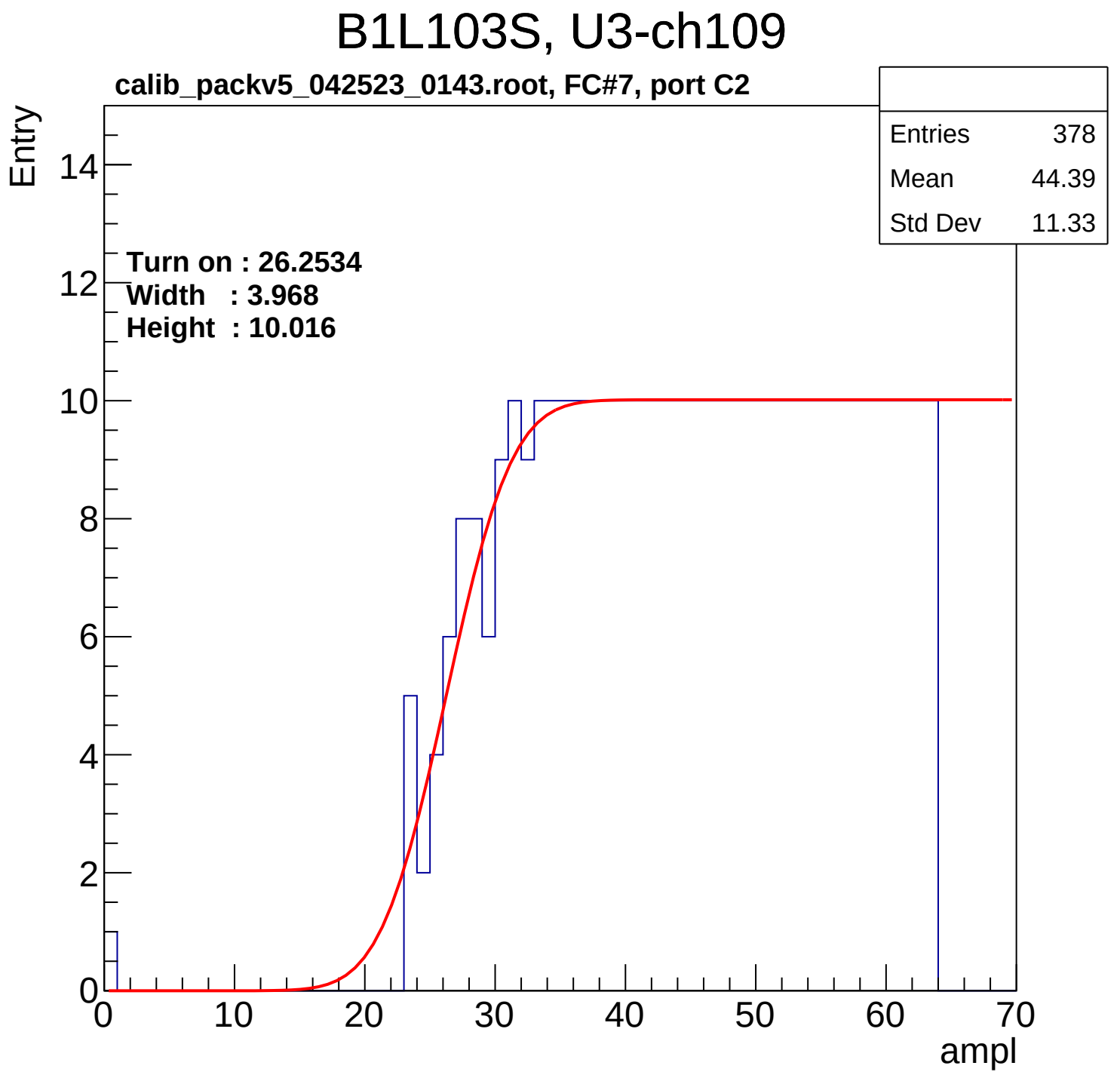
B1L103S, U3-ch109
calib_packv5_042523_0143.root, FC#7, port C2
Entries 378
Mean 44.39
Std Dev 11.33
Turn on : 26.2534
Width : 3.968
Height : 10.016
Entry
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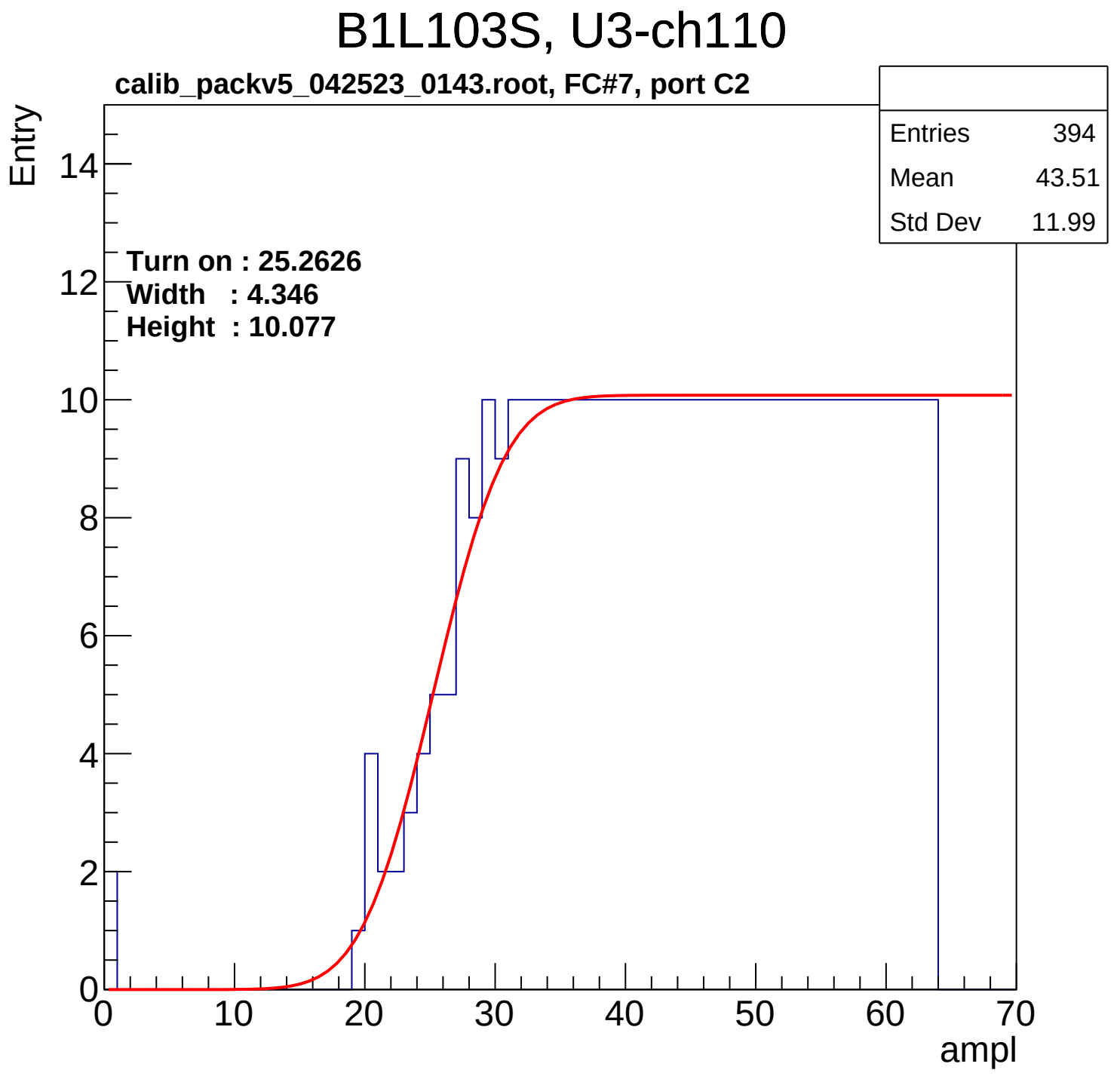
B1L103S, U3-ch110
calib_packv5_042523_0143.root, FC#7, port C2
Entries 394
Mean 43.51
Std Dev 11.99
Turn on : 25.2626
Width : 4.346
Height : 10.077
Entry
ampl
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6
8
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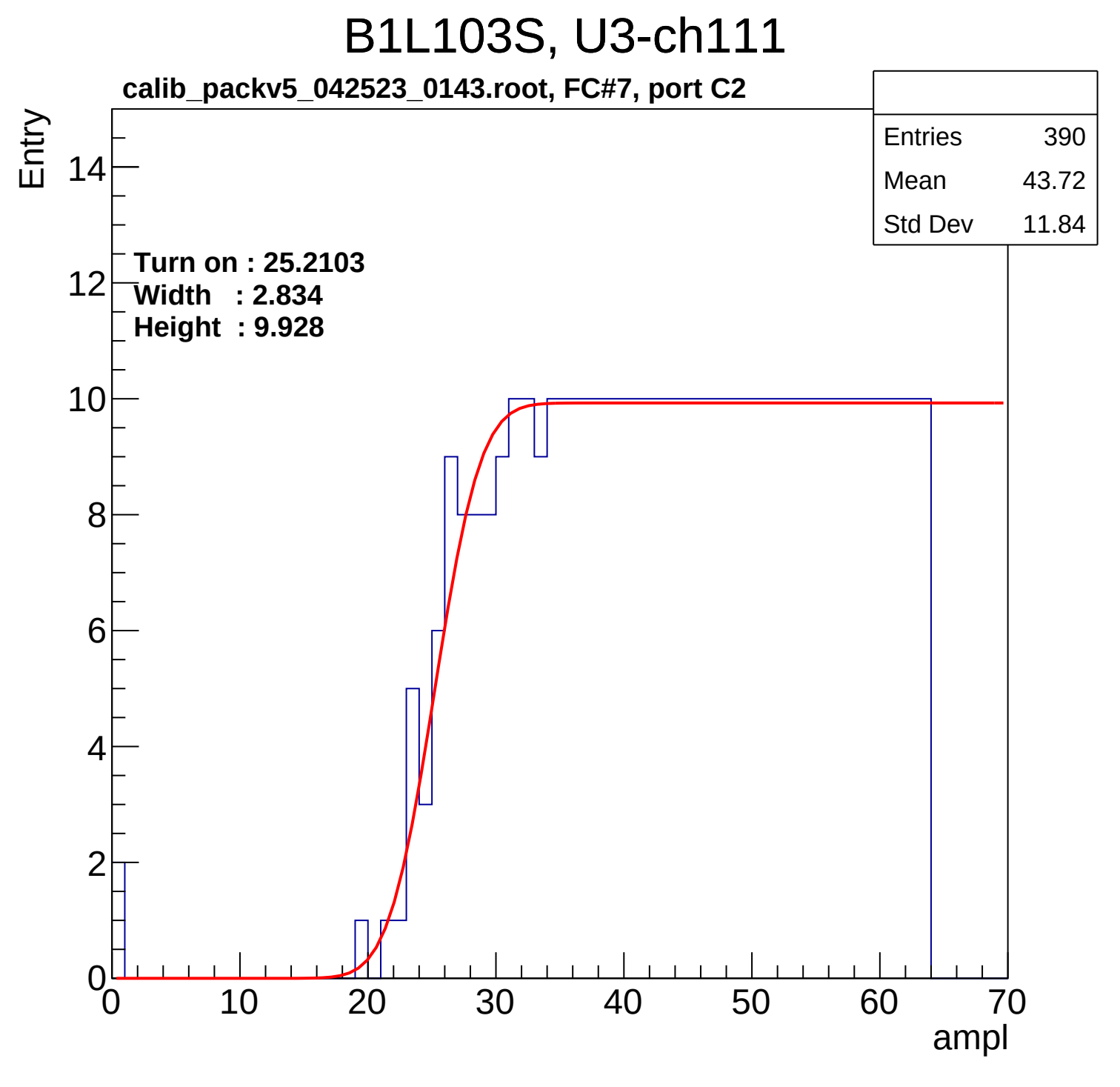
B1L103S, U3-ch111
calib_packv5_042523_0143.root, FC#7, port C2
Entries 390
Mean 43.72
Std Dev 11.84
Turn on : 25.2103
Width : 2.834
Height : 9.928
Entry
ampl
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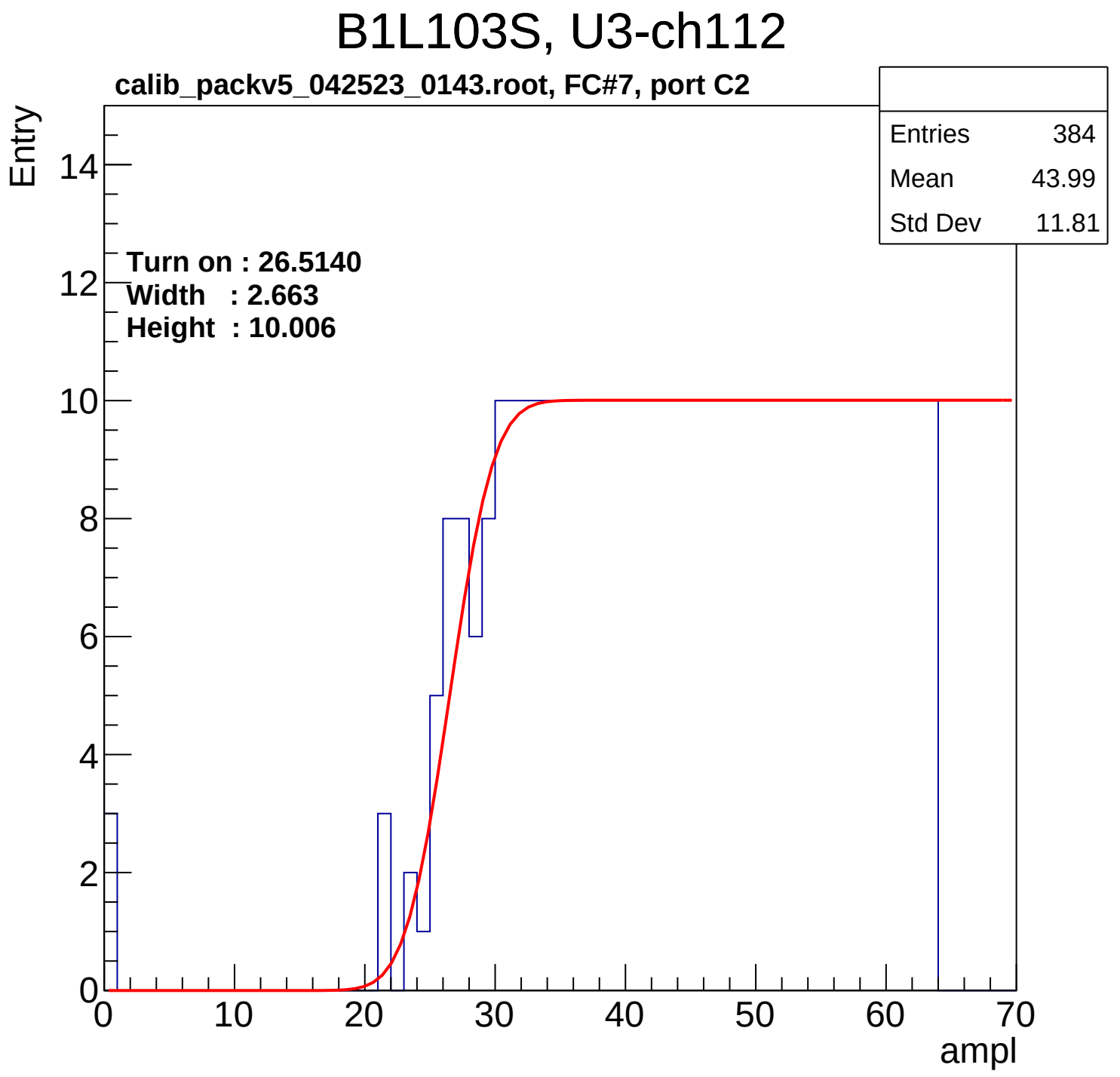
B1L103S, U3-ch112
calib_packv5_042523_0143.root, FC#7, port C2
Entries 384
Mean 43.99
Std Dev 11.81
Turn on : 26.5140
Width : 2.663
Height : 10.006
Entry
ampl
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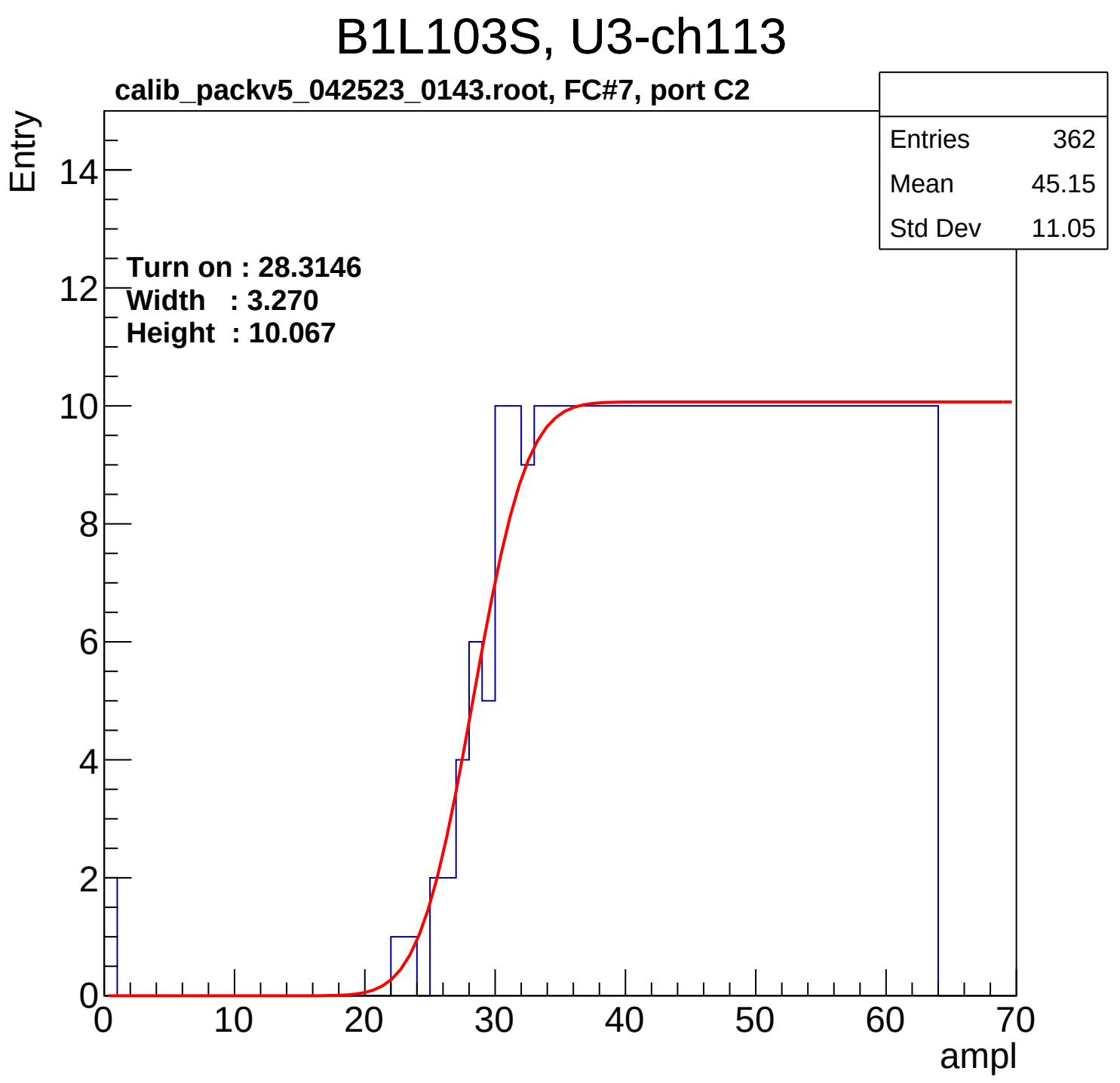
B1L103S, U3-ch113
calib_packv5_042523_0143.root, FC#7, port C2
Entries 362
Mean 45.15
Std Dev 11.05
Turn on : 28.3146
Width : 3.270
Height : 10.067
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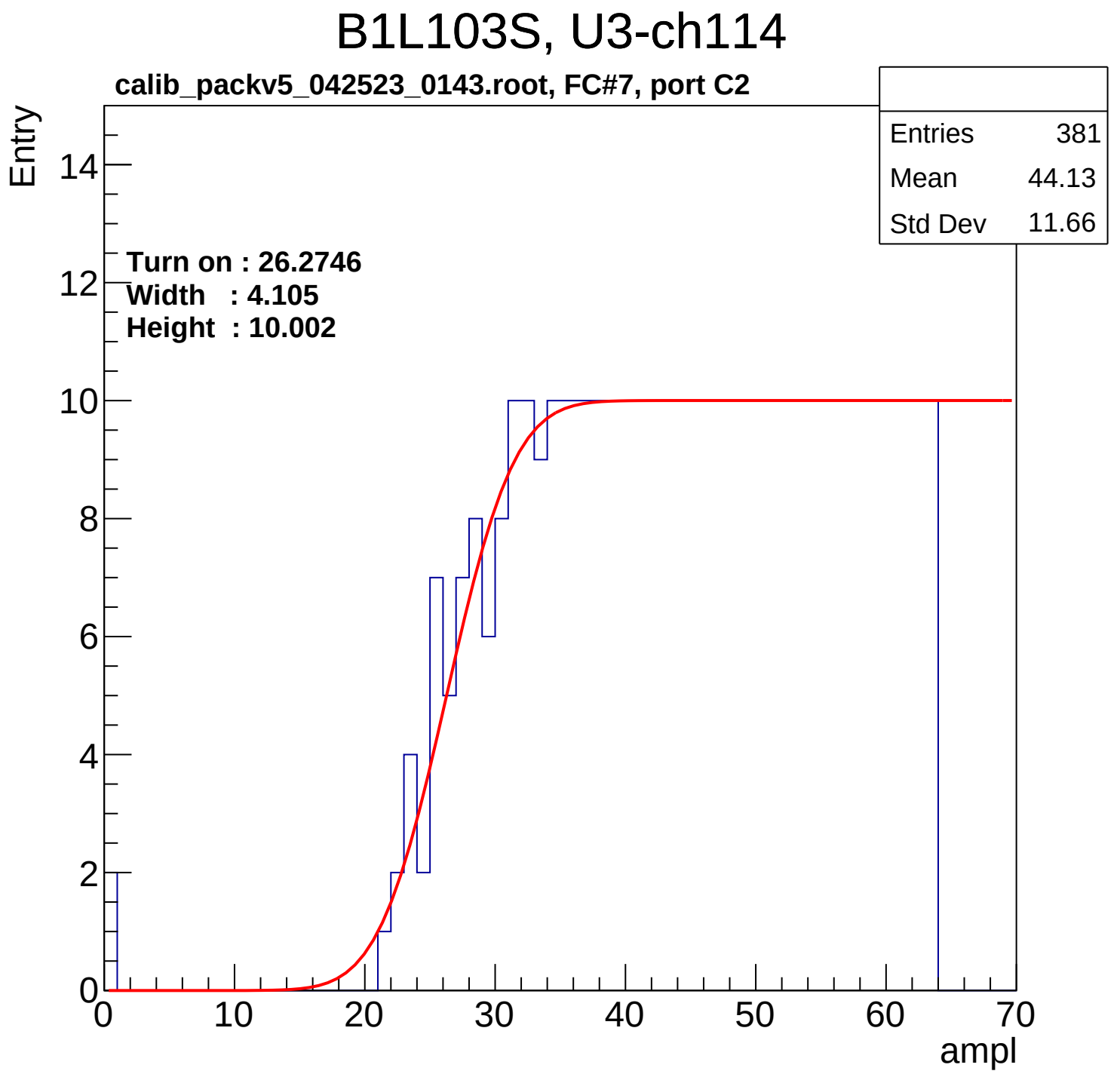
B1L103S, U3-ch114
calib_packv5_042523_0143.root, FC#7, port C2
Entries 381
Mean 44.13
Std Dev 11.66
Turn on : 26.2746
Width : 4.105
Height : 10.002
Entry
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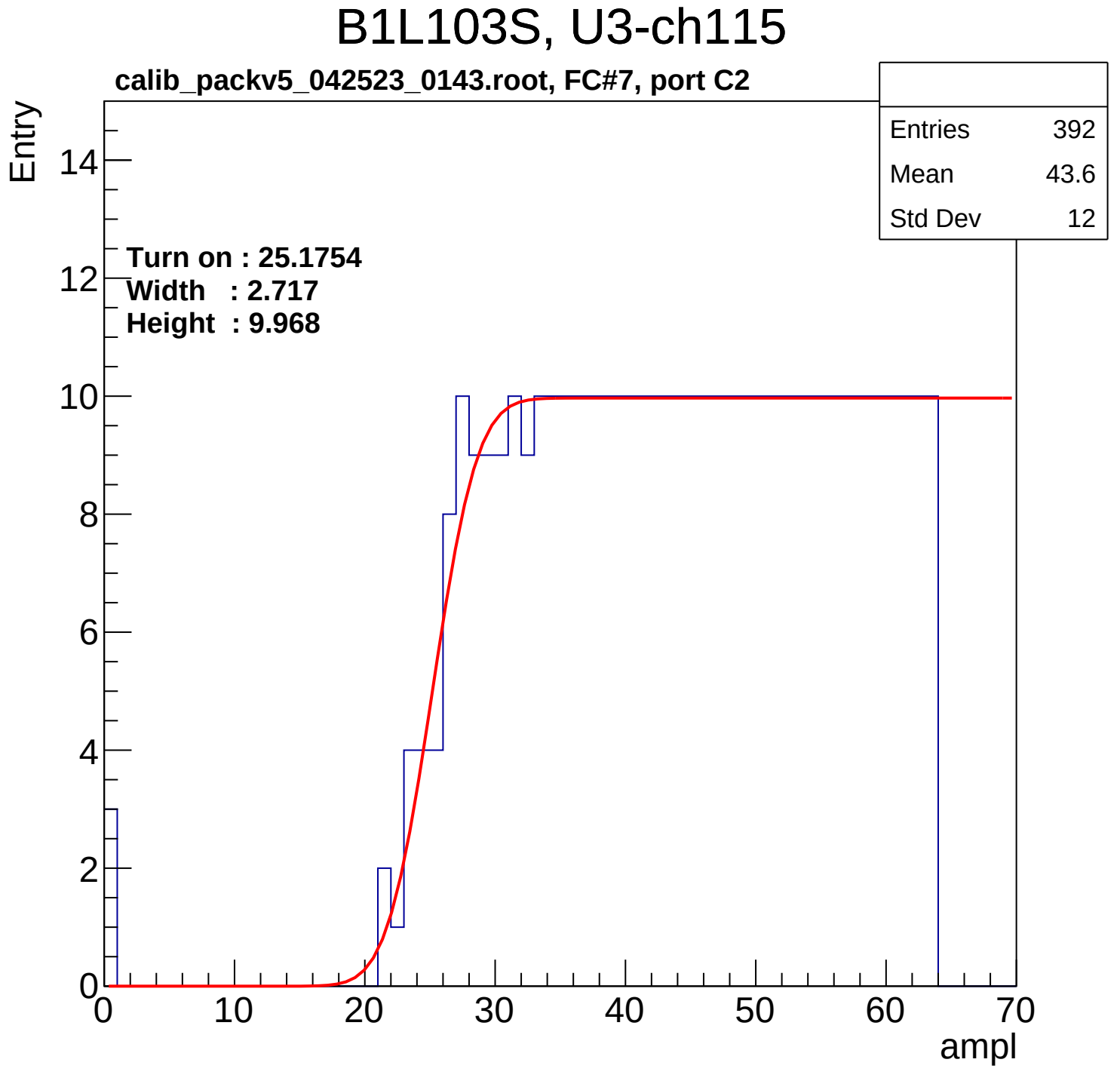
B1L103S, U3-ch115
calib_packv5_042523_0143.root, FC#7, port C2
Entries 392
Mean 43.6
Std Dev 12
Turn on : 25.1754
Width : 2.717
Height : 9.968
Entry
ampl
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2
4
6
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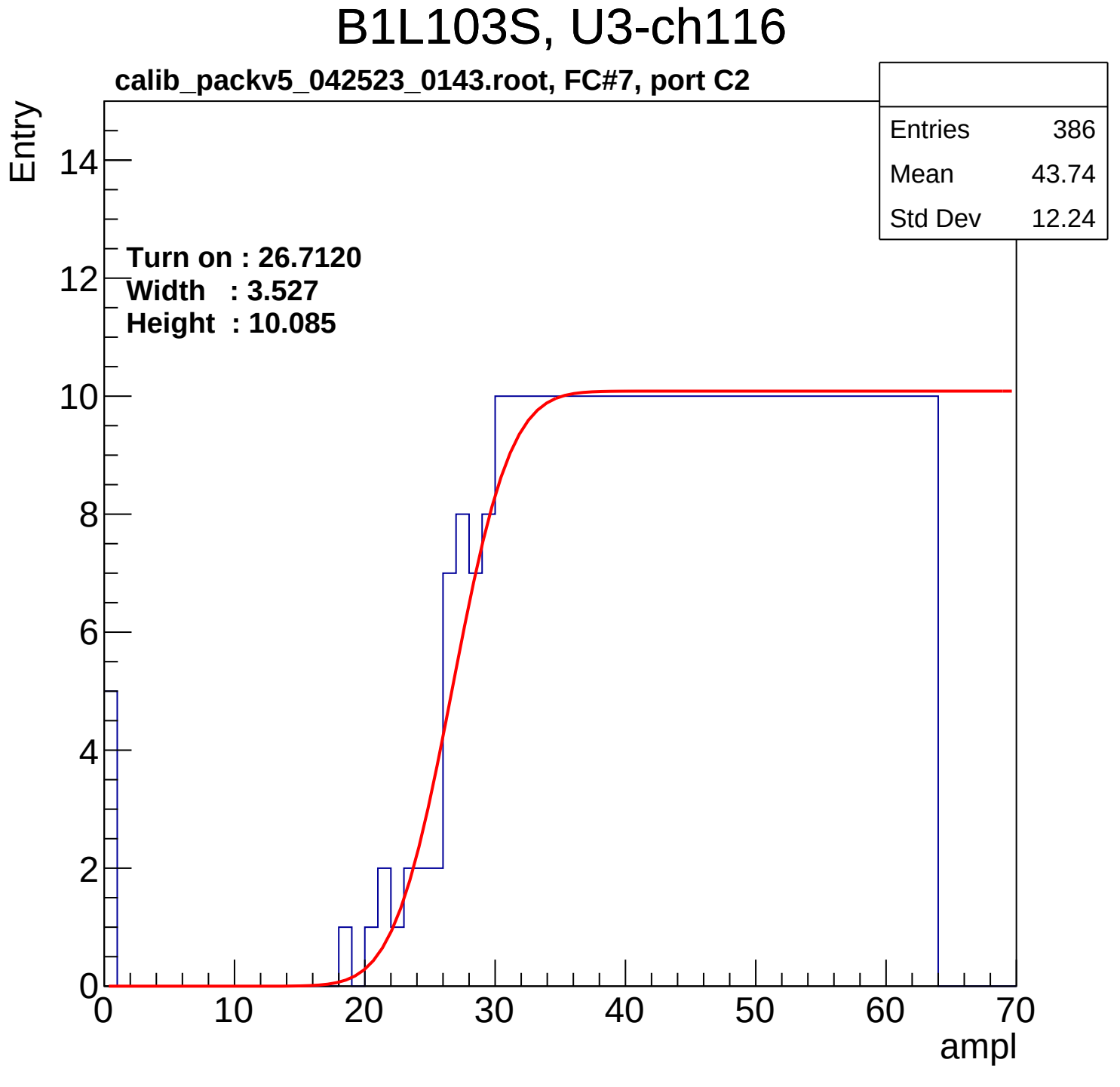
B1L103S, U3-ch116
calib_packv5_042523_0143.root, FC#7, port C2
Entries 386
Mean 43.74
Std Dev 12.24
Turn on : 26.7120
Width : 3.527
Height : 10.085
Entry
ampl
0
2
4
6
8
10
12
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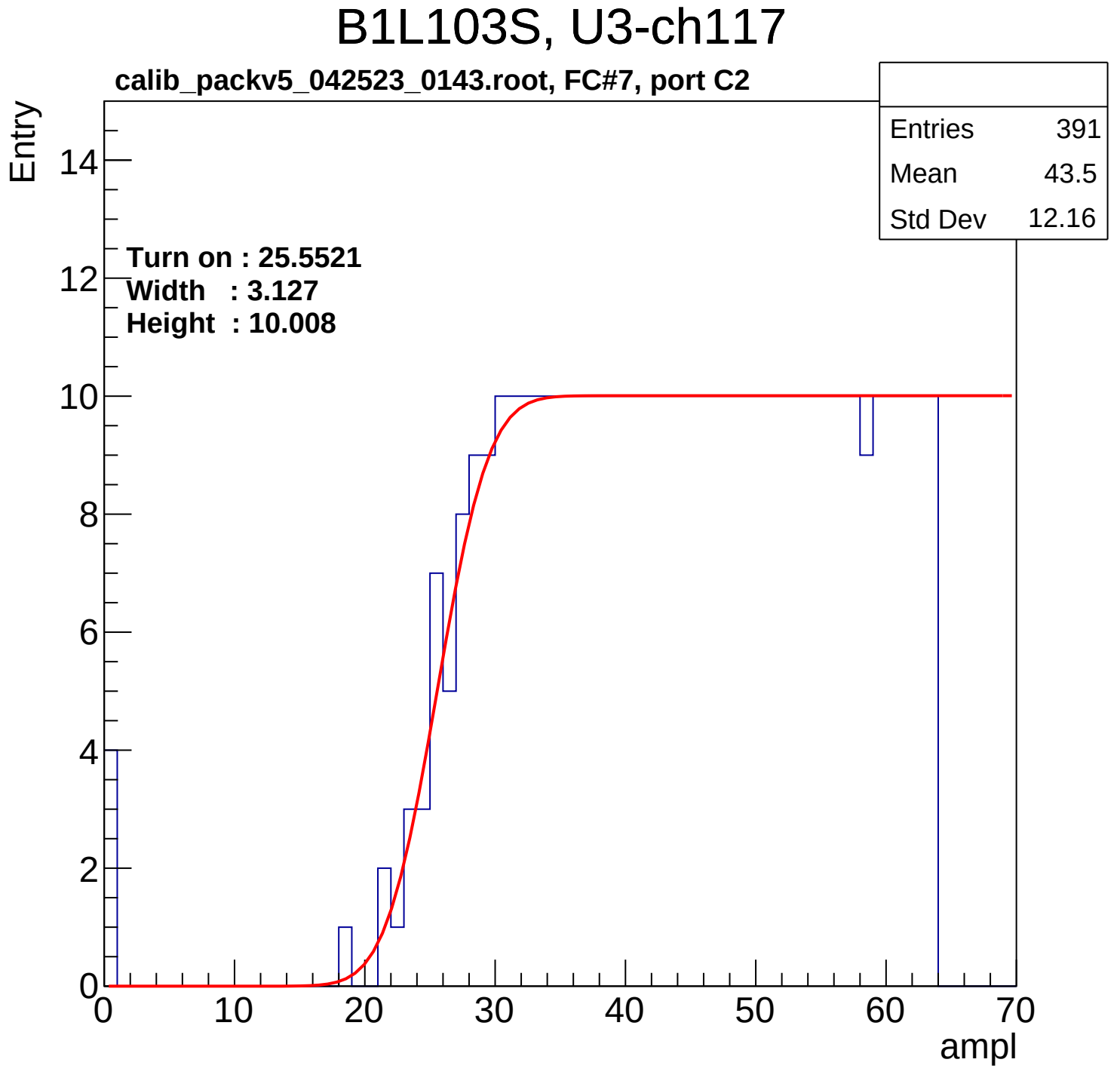
B1L103S, U3-ch117
calib_packv5_042523_0143.root, FC#7, port C2
Entries 391
Mean 43.5
Std Dev 12.16
Turn on : 25.5521
Width : 3.127
Height : 10.008
Entry
ampl
0
2
4
6
8
10
12
14
0
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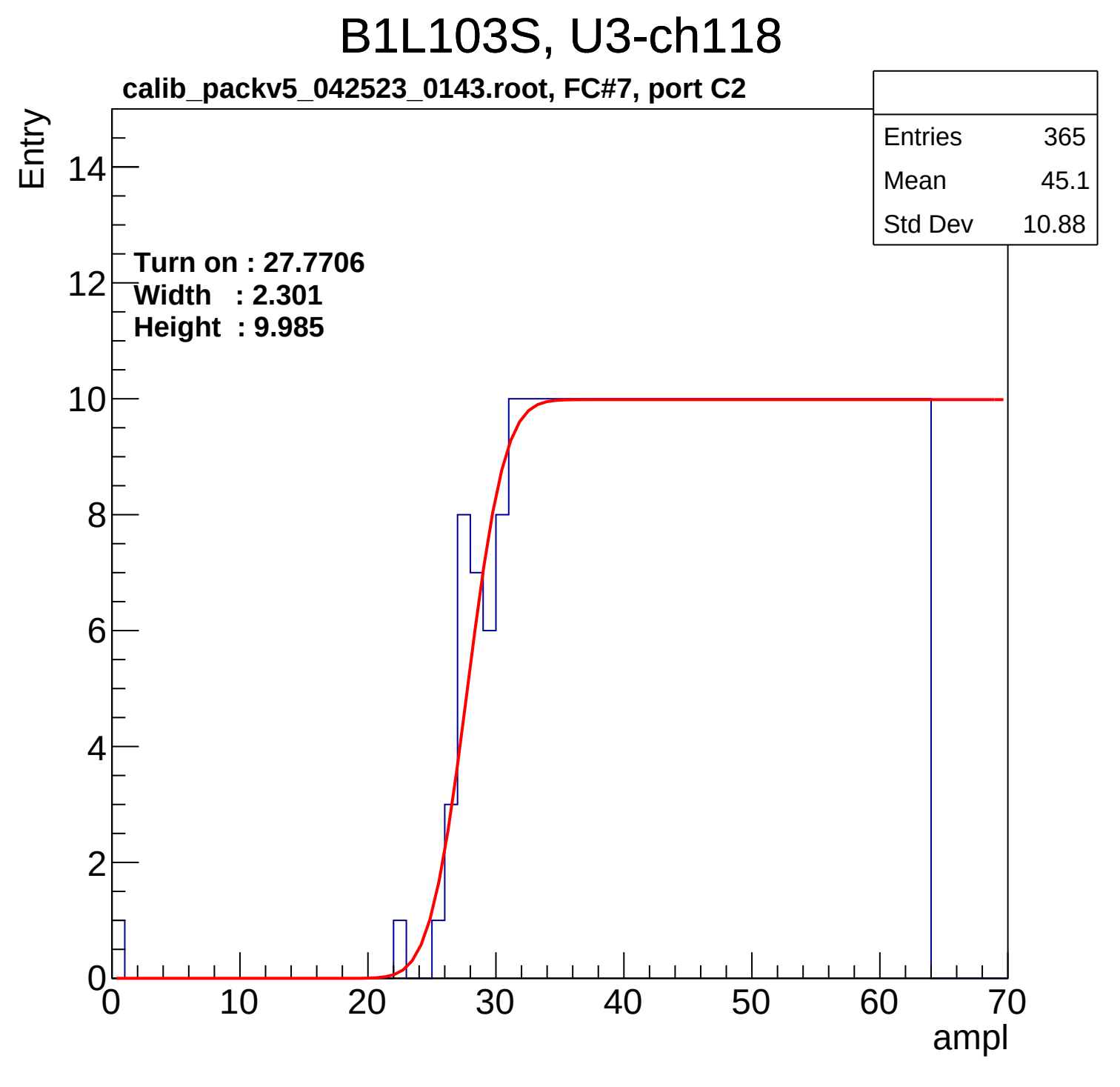
B1L103S, U3-ch118
calib_packv5_042523_0143.root, FC#7, port C2
Entries 365
Mean 45.1
Std Dev 10.88
Turn on : 27.7706
Width : 2.301
Height : 9.985
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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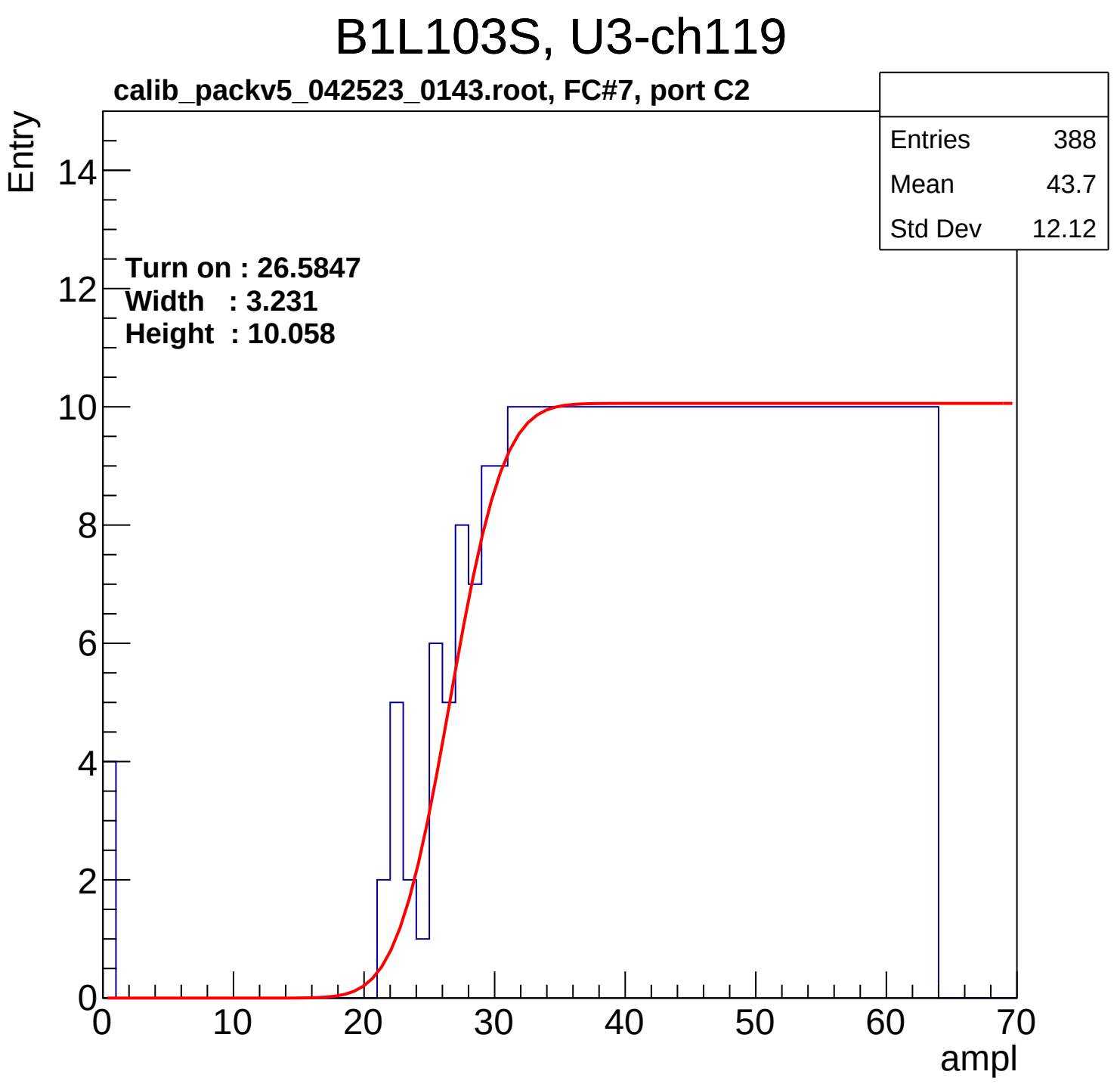
B1L103S, U3-ch119
calib_packv5_042523_0143.root, FC#7, port C2
Entries 388
Mean 43.7
Std Dev 12.12
Turn on : 26.5847
Width : 3.231
Height : 10.058
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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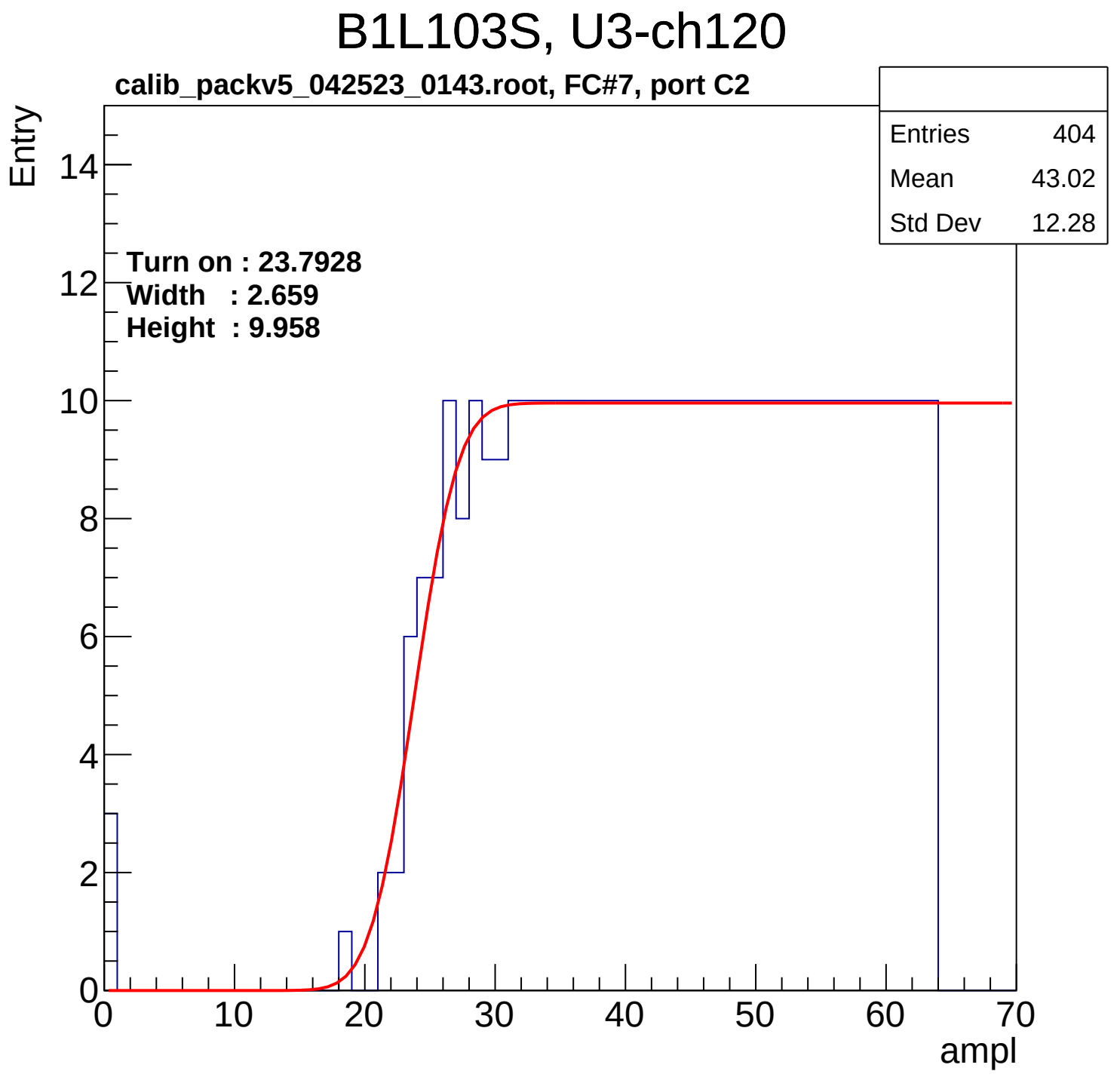
B1L103S, U3-ch120
calib_packv5_042523_0143.root, FC#7, port C2
Entries 404
Mean 43.02
Std Dev 12.28
Turn on : 23.7928
Width : 2.659
Height : 9.958
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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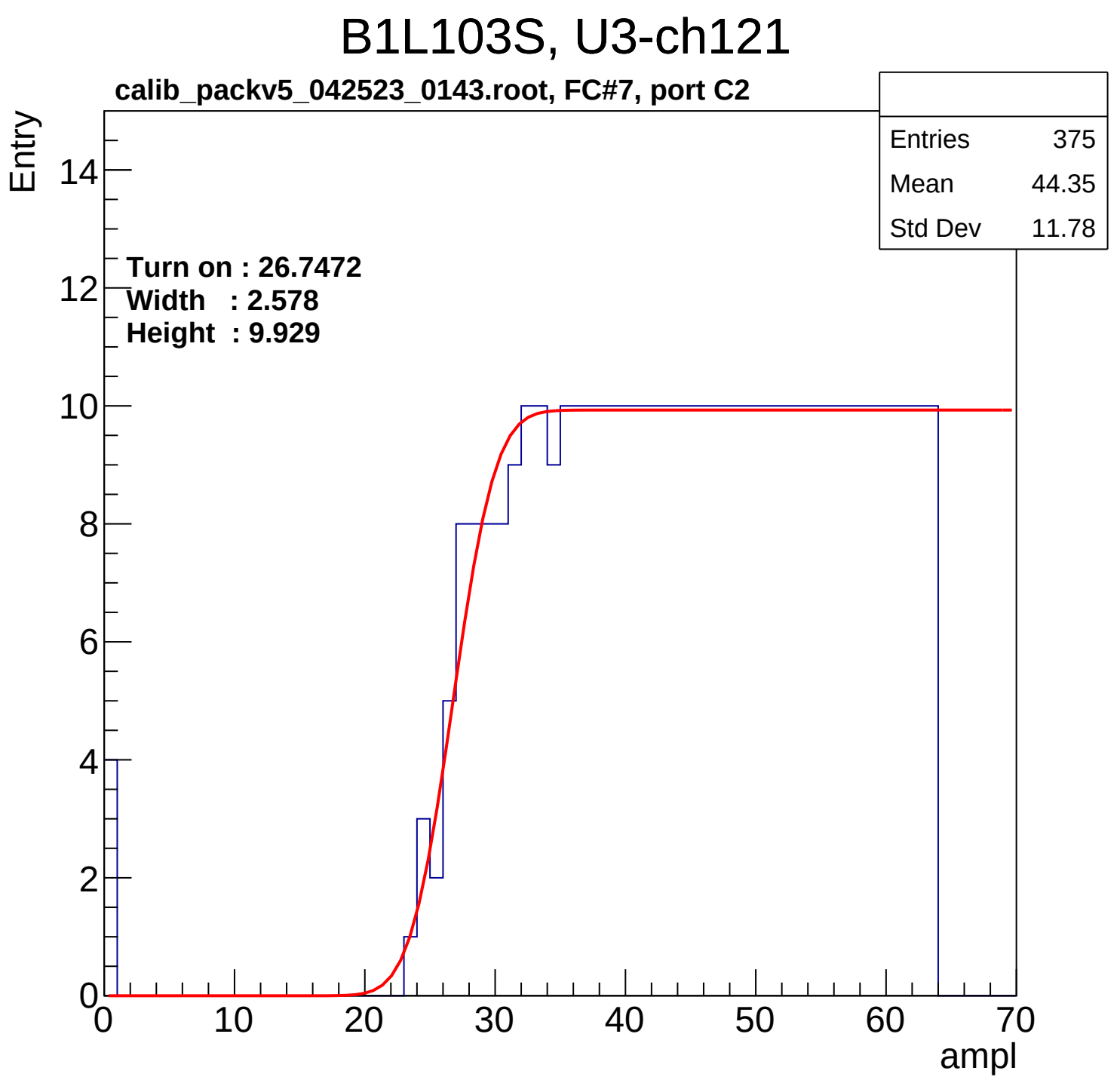
B1L103S, U3-ch121
calib_packv5_042523_0143.root, FC#7, port C2
Entries 375
Mean 44.35
Std Dev 11.78
Turn on : 26.7472
Width : 2.578
Height : 9.929
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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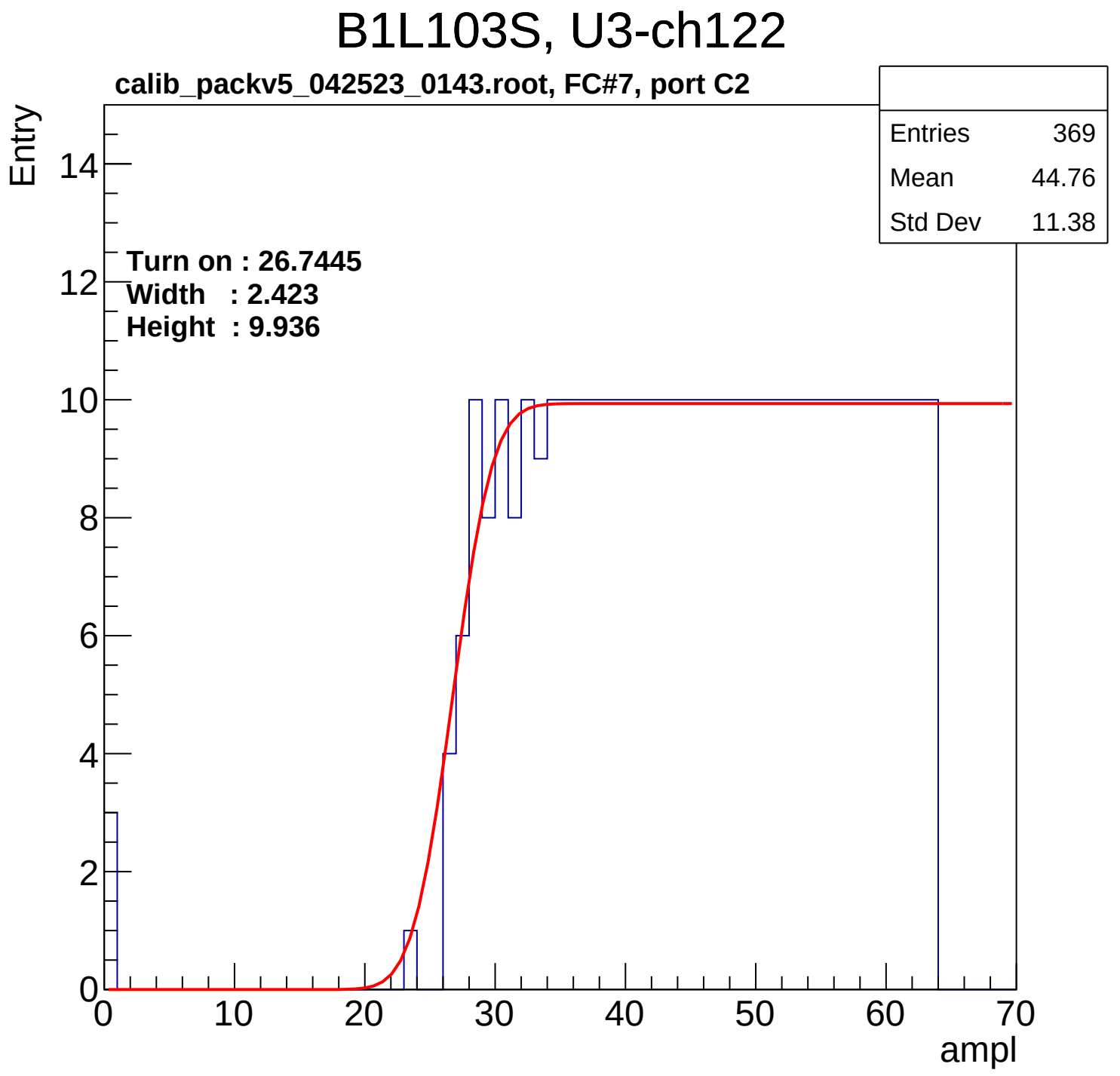
B1L103S, U3-ch122
calib_packv5_042523_0143.root, FC#7, port C2
Entries 369
Mean 44.76
Std Dev 11.38
Turn on : 26.7445
Width : 2.423
Height : 9.936
Entry
ampl
0
2
4
6
8
10
12
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0
10
20
30
40
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60
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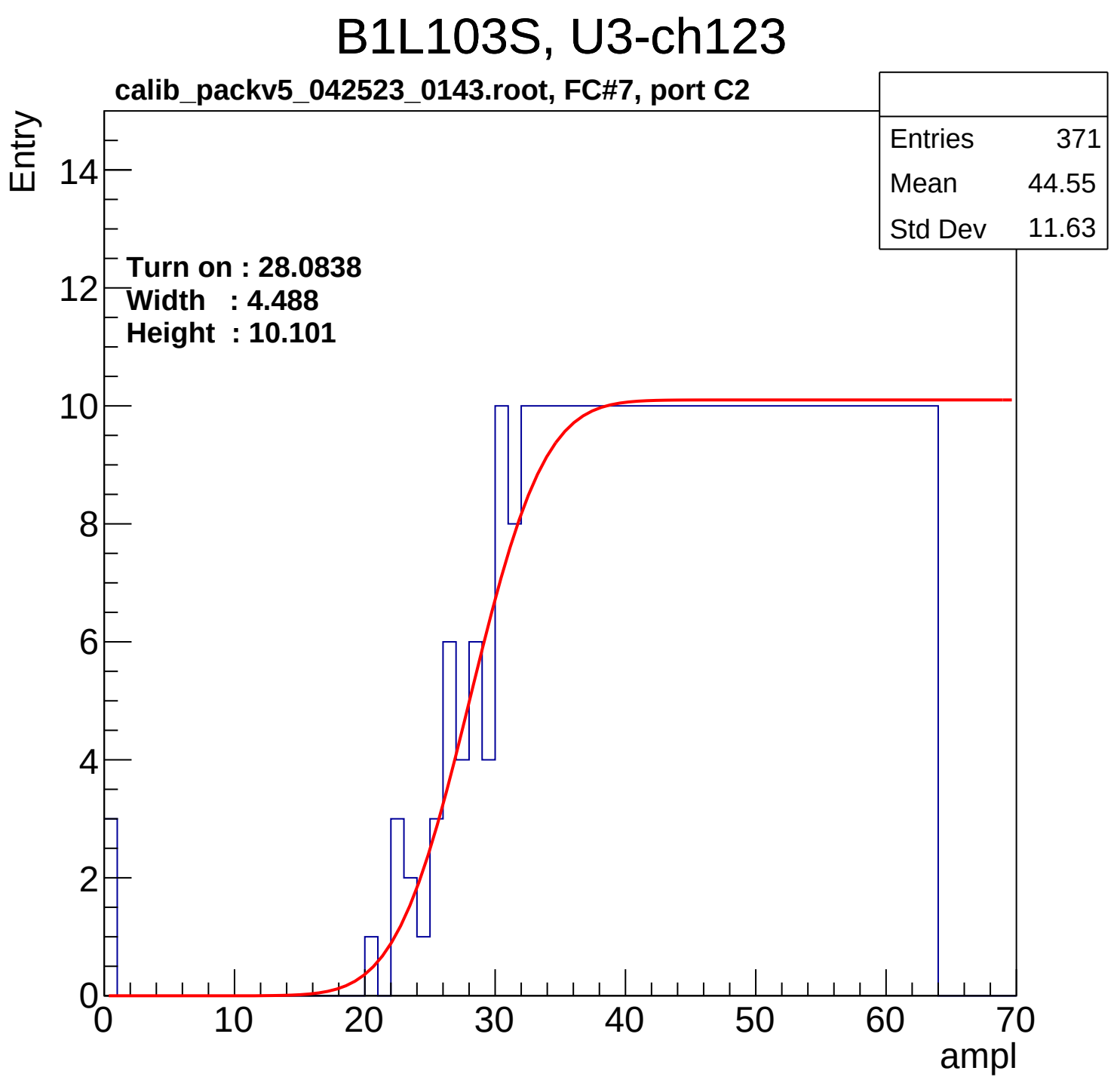
B1L103S, U3-ch123
calib_packv5_042523_0143.root, FC#7, port C2
Entries 371
Mean 44.55
Std Dev 11.63
Turn on : 28.0838
Width : 4.488
Height : 10.101
Entry
ampl
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2
4
6
8
10
12
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0
10
20
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40
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60
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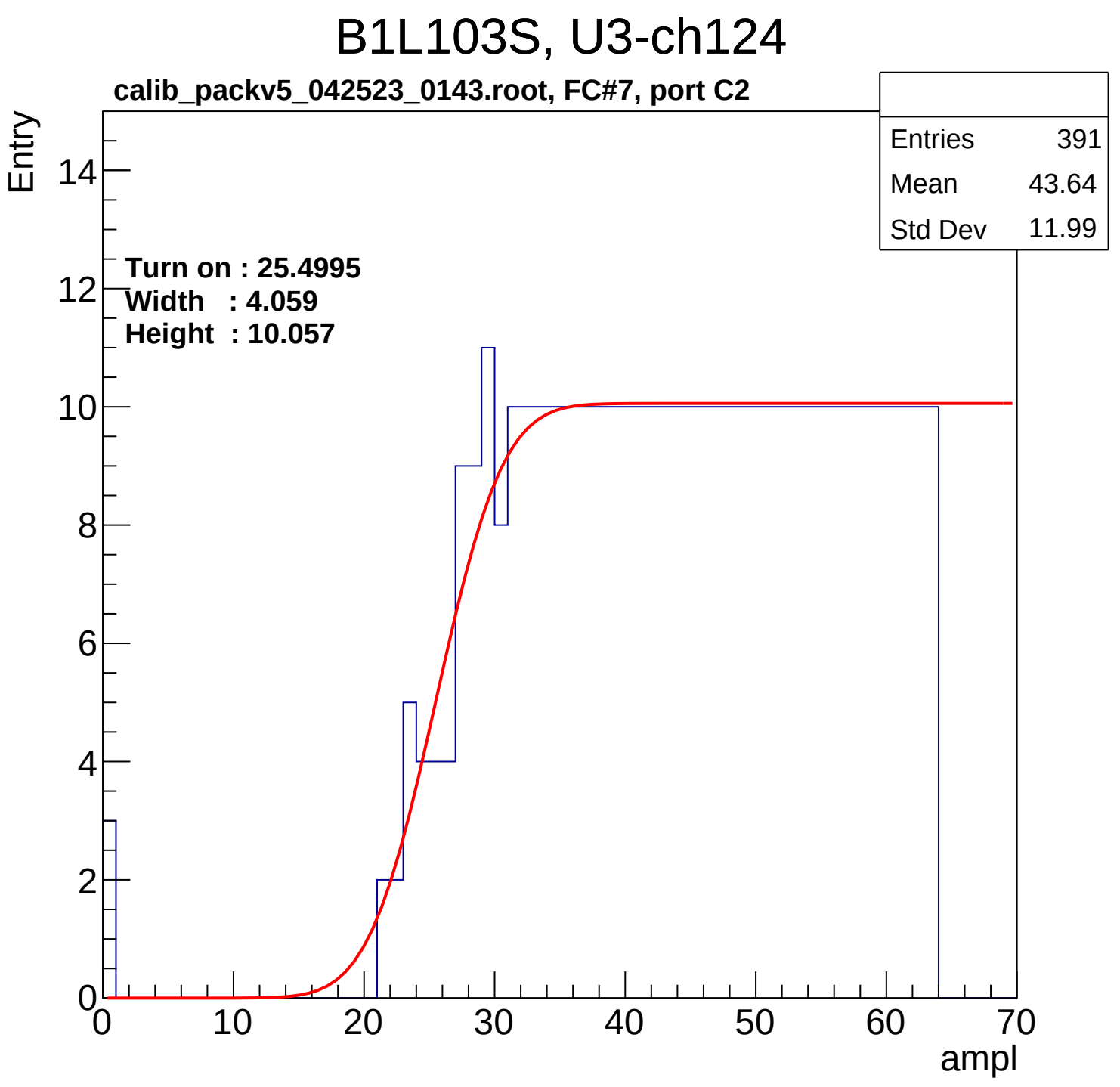
B1L103S, U3-ch124
calib_packv5_042523_0143.root, FC#7, port C2
Entries 391
Mean 43.64
Std Dev 11.99
Turn on : 25.4995
Width : 4.059
Height : 10.057
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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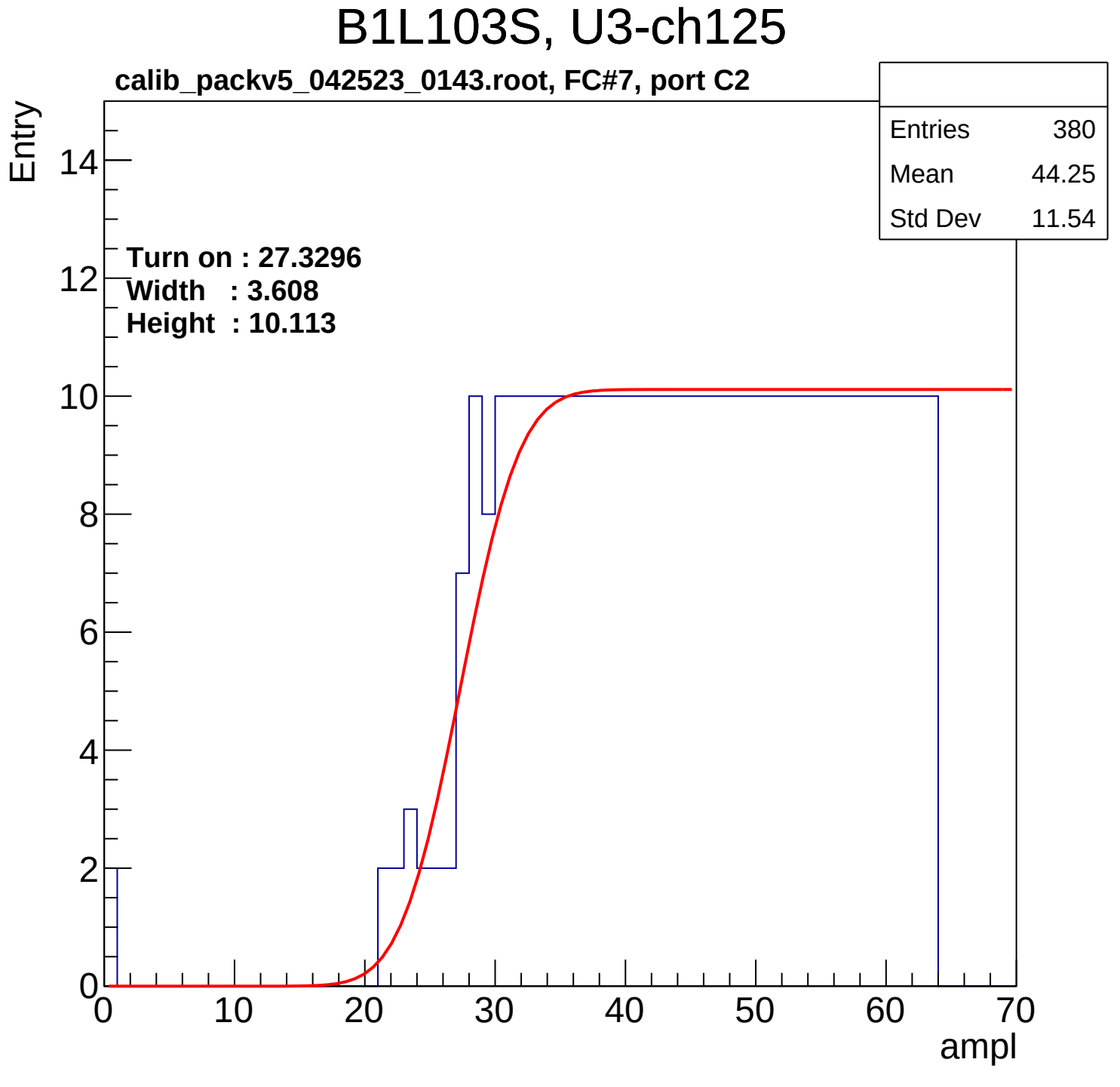
B1L103S, U3-ch125
calib_packv5_042523_0143.root, FC#7, port C2
Entries 380
Mean 44.25
Std Dev 11.54
Turn on : 27.3296
Width : 3.608
Height : 10.113
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
50
60
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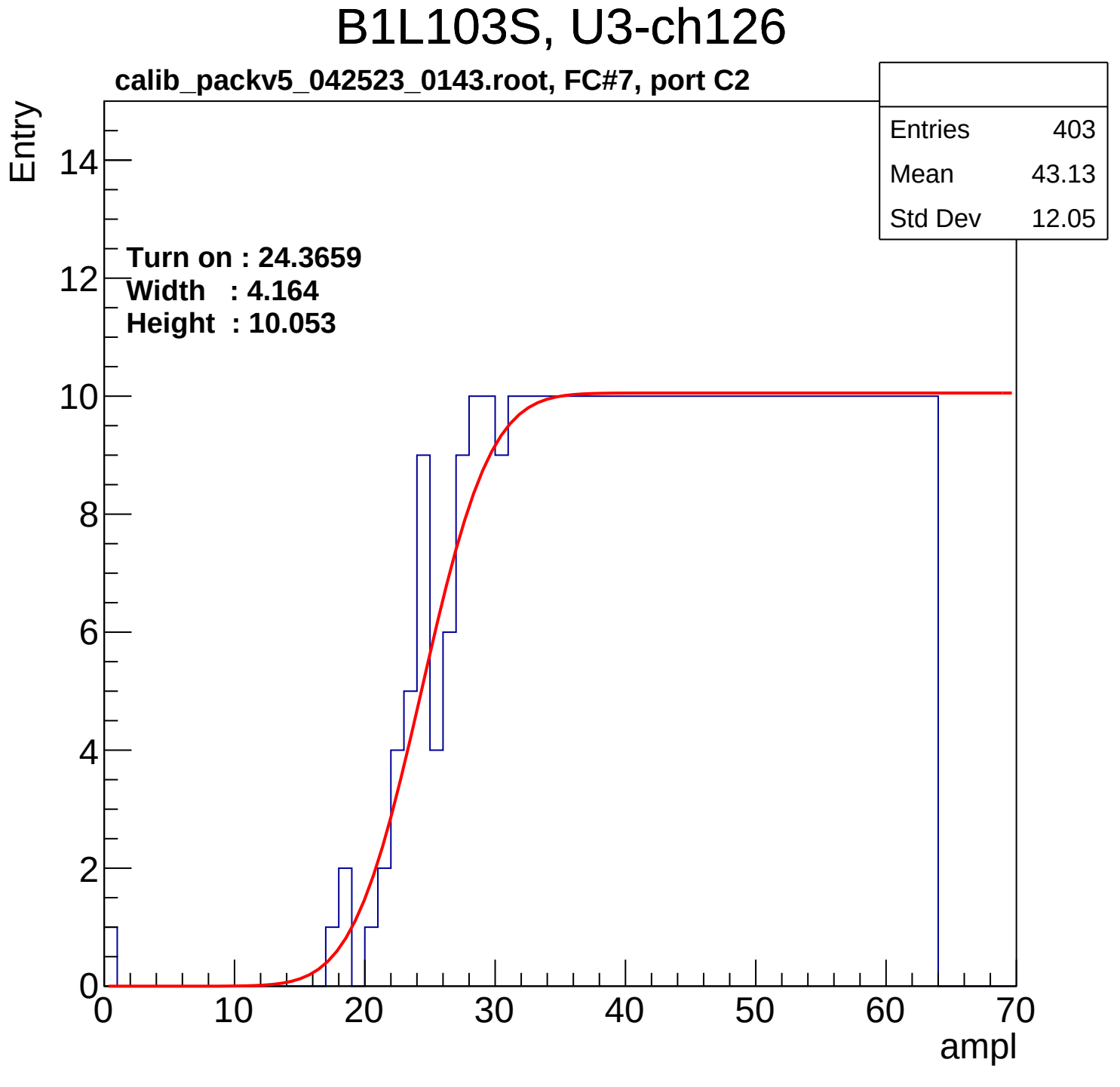
B1L103S, U3-ch126
calib_packv5_042523_0143.root, FC#7, port C2
Entries 403
Mean 43.13
Std Dev 12.05
Turn on : 24.3659
Width : 4.164
Height : 10.053
Entry
ampl
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2
4
6
8
10
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0
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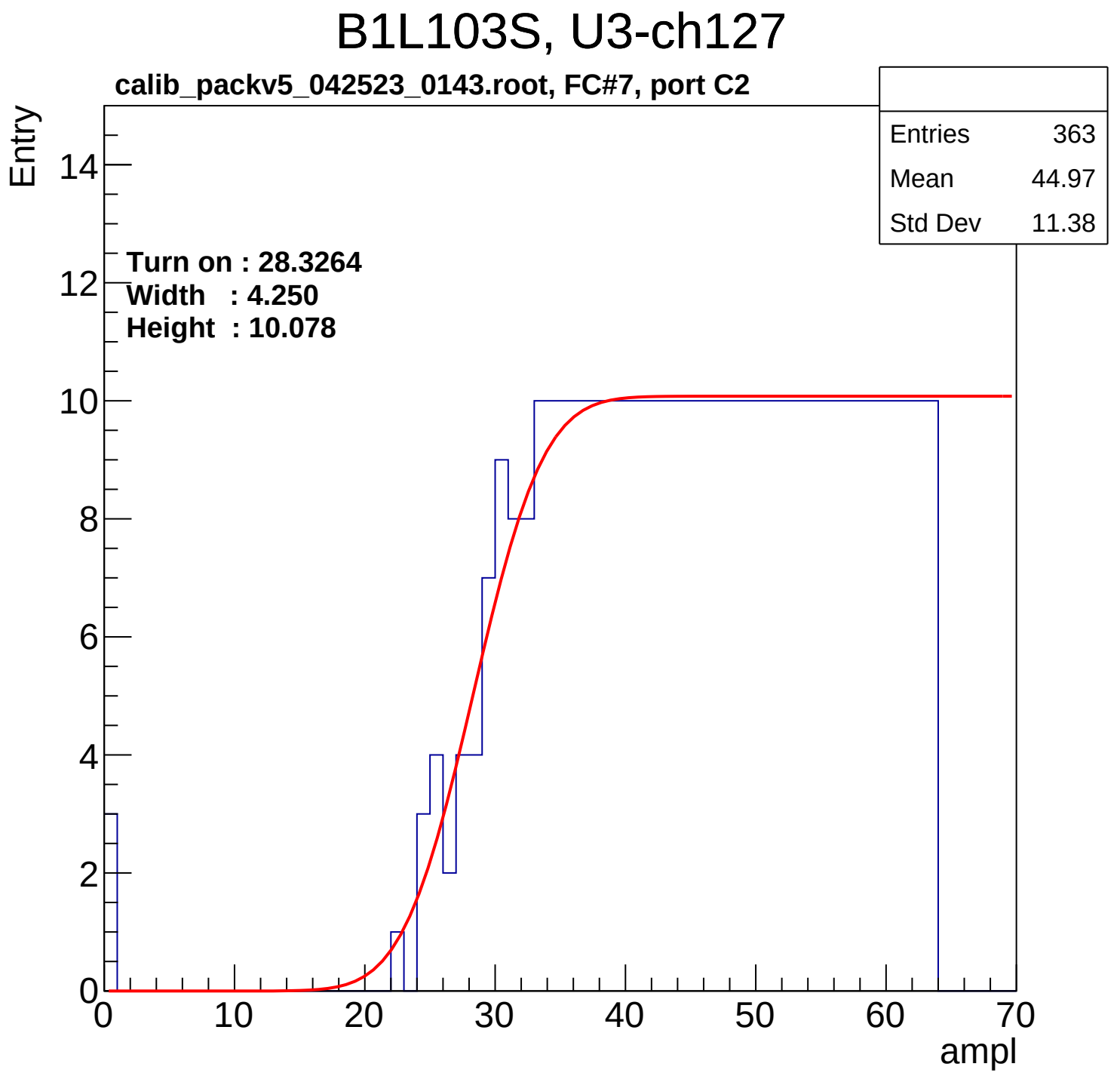
B1L103S, U3-ch127
calib_packv5_042523_0143.root, FC#7, port C2
Entries 363
Mean 44.97
Std Dev 11.38
Turn on : 28.3264
Width : 4.250
Height : 10.078
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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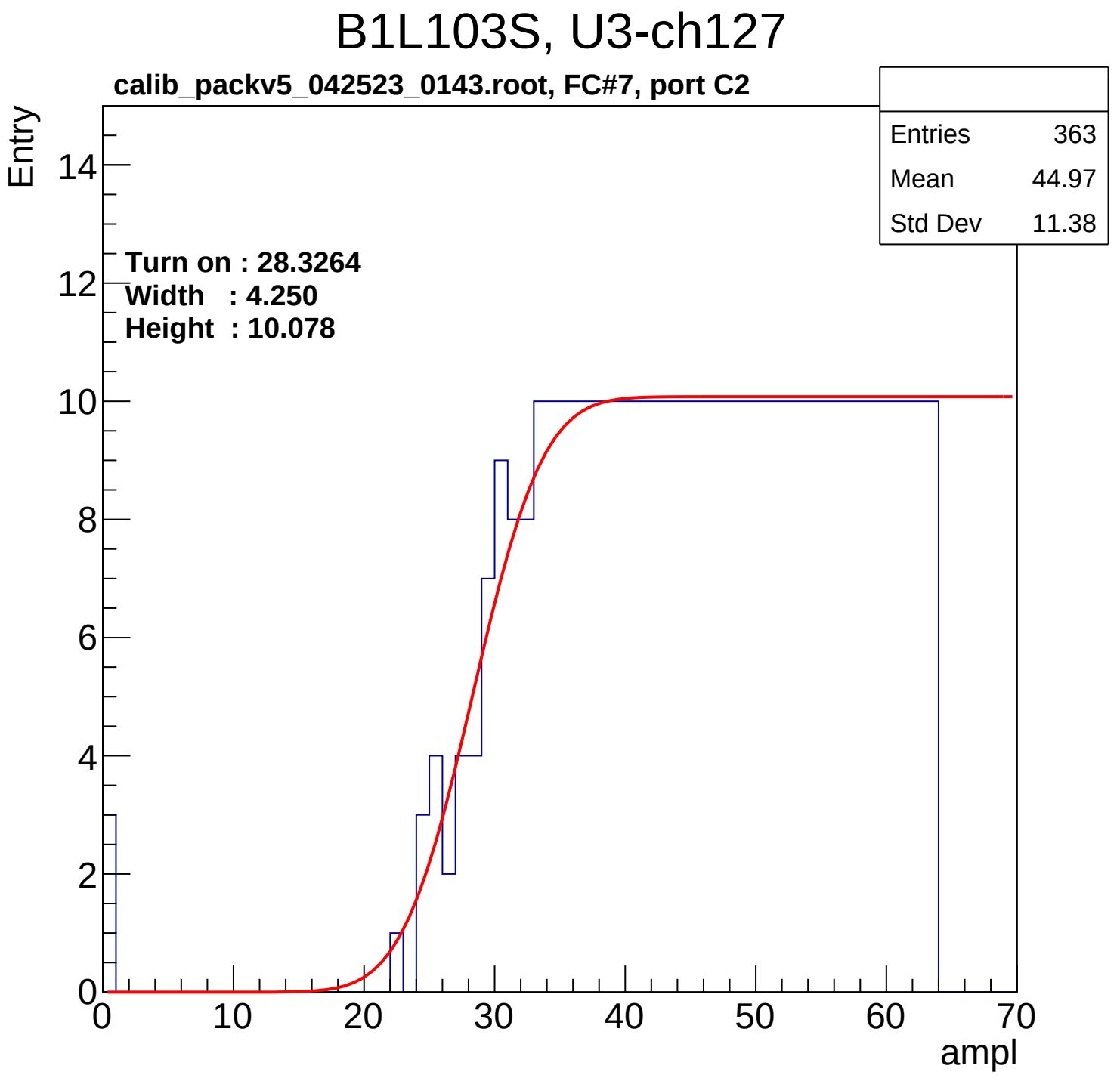
60
70


B1L103S, U3-ch127
calib_packv5_042523_0143.root, FC#7, port C2
Entries 363
Mean 44.97
Std Dev 11.38
Turn on : 28.3264
Width : 4.250
Height : 10.078
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70