

B1L100S, U4-ch0

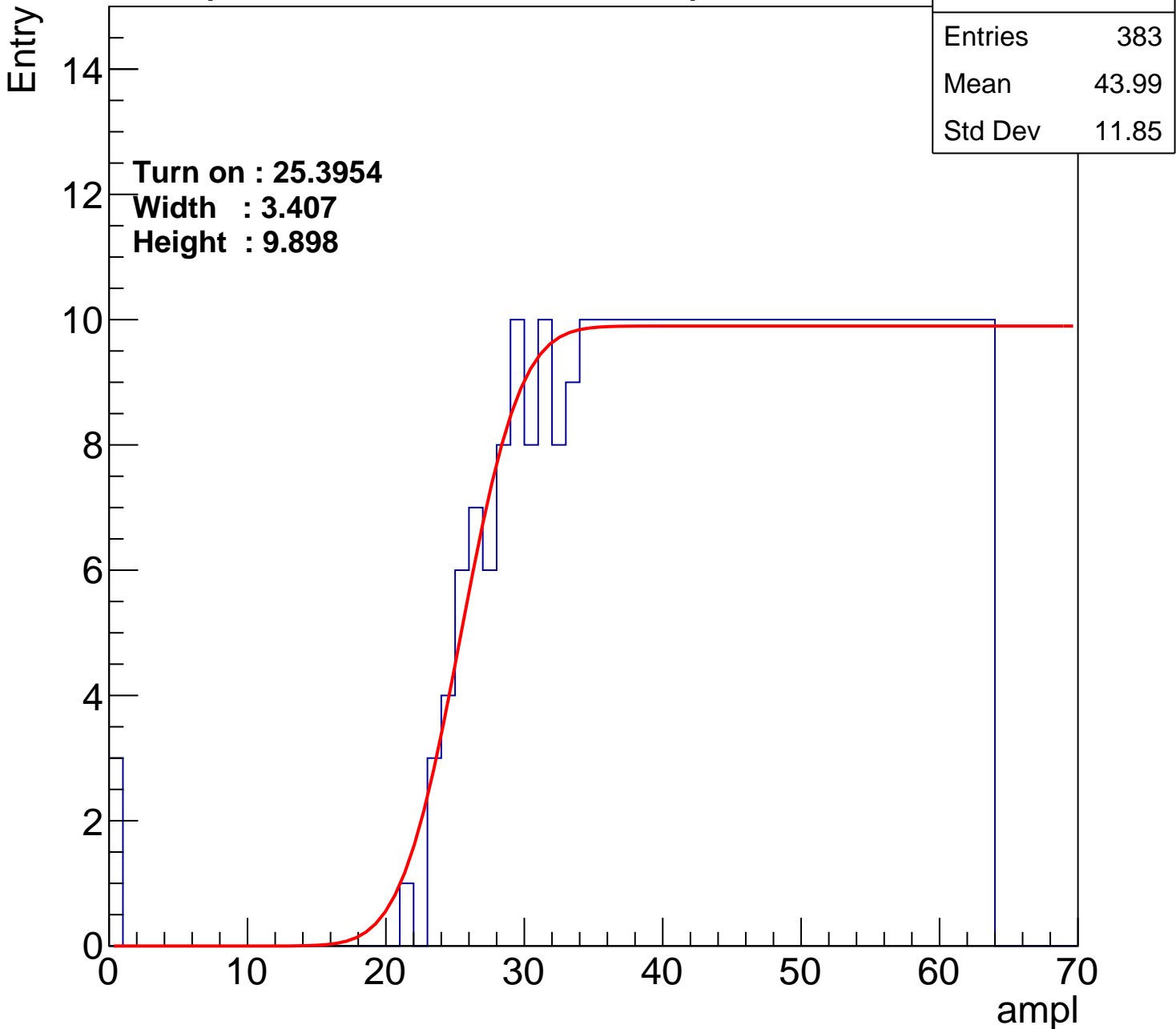
calib_packv5_042523_0143.root, FC#4, port A2

Entries	383
Mean	43.99
Std Dev	11.85

Turn on : 25.3954

Width : 3.407

Height : 9.898



B1L100S, U4-ch1

calib_packv5_042523_0143.root, FC#4, port A2

Entries	367
Mean	44.6
Std Dev	11.99

Turn on : 28.6805

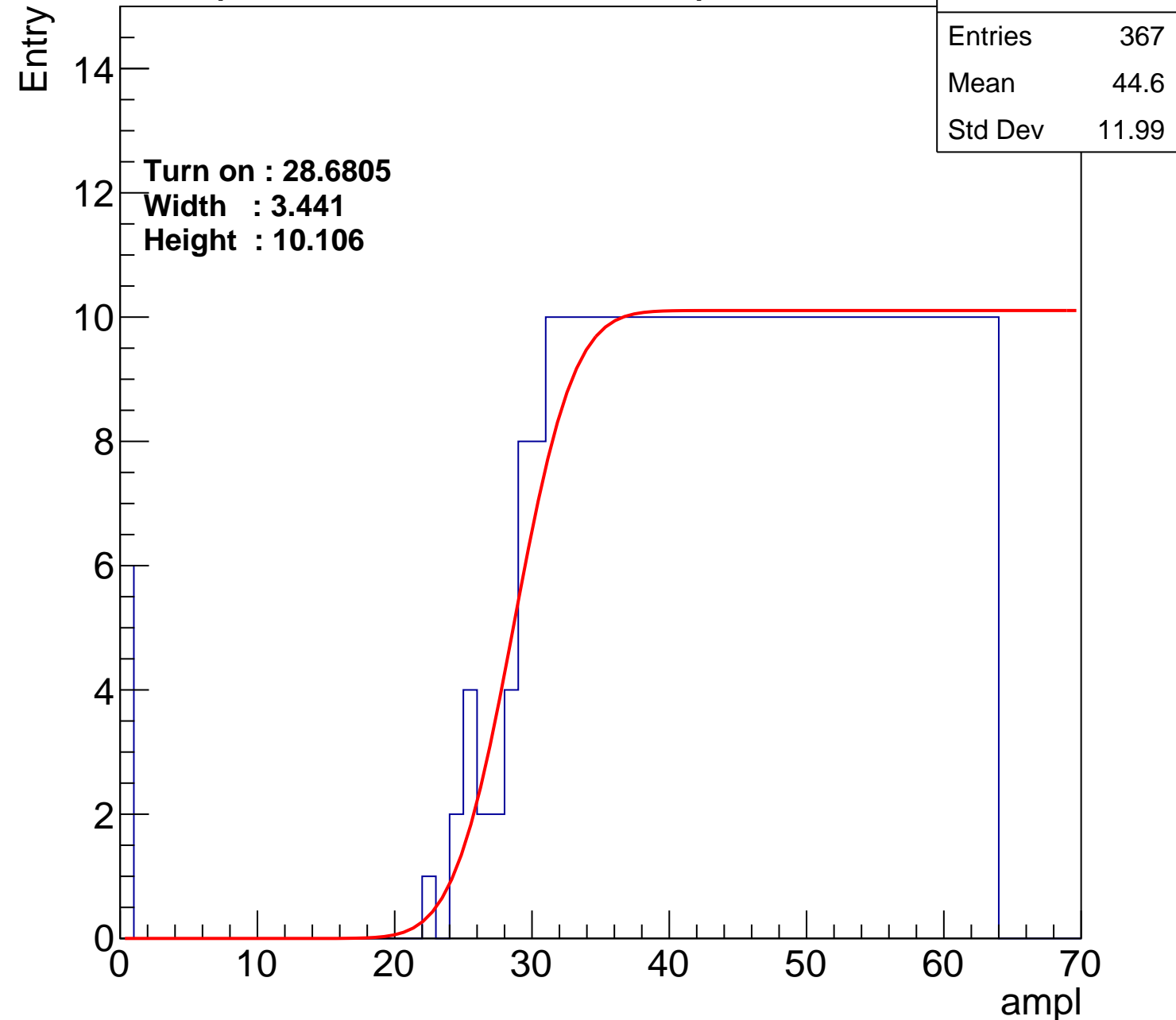
Width : 3.441

Height : 10.106

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch2

calib_packv5_042523_0143.root, FC#4, port A2

Entries	386
Mean	43.83
Std Dev	12.02

Turn on : 26.0145

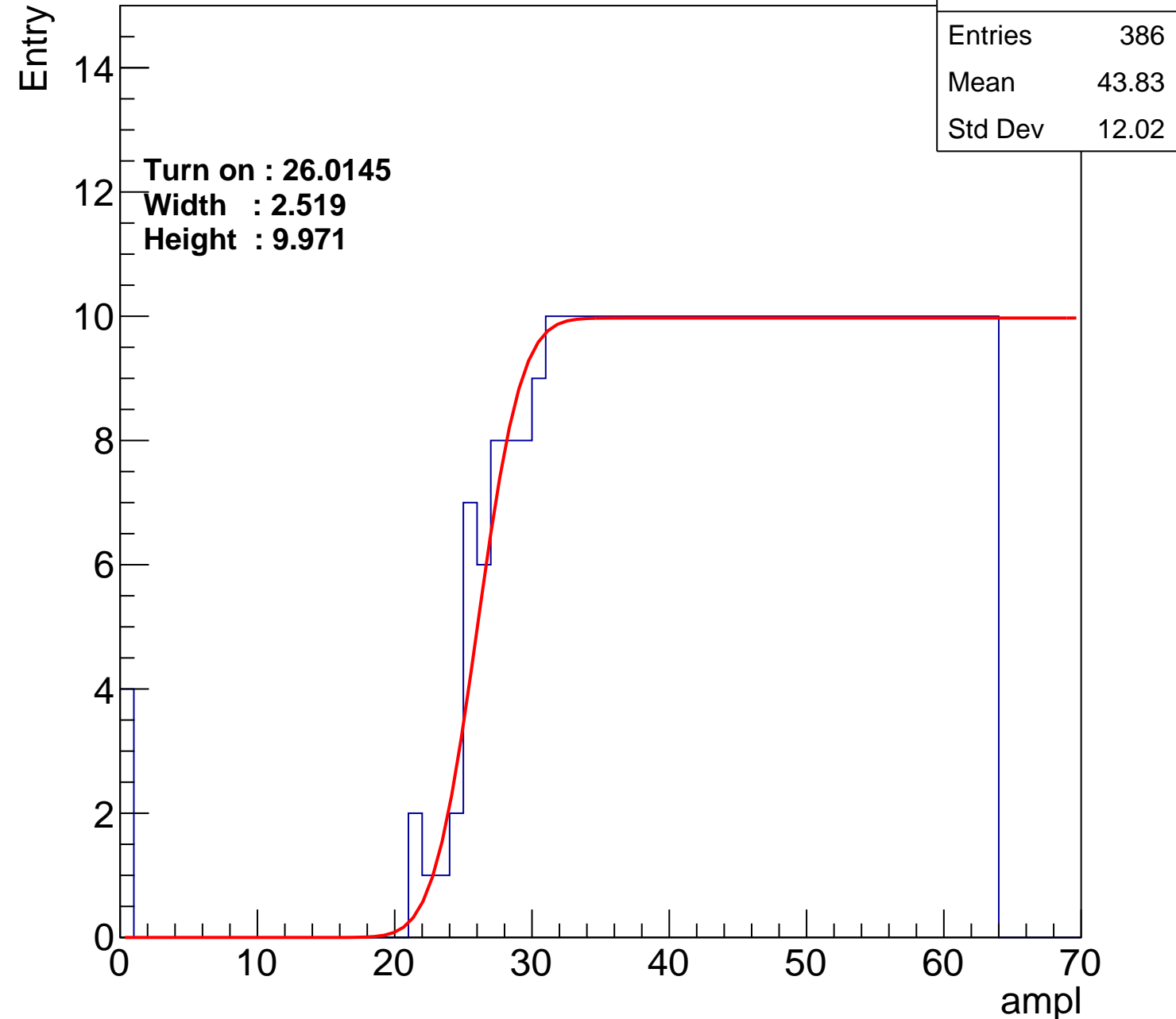
Width : 2.519

Height : 9.971

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch3

calib_packv5_042523_0143.root, FC#4, port A2

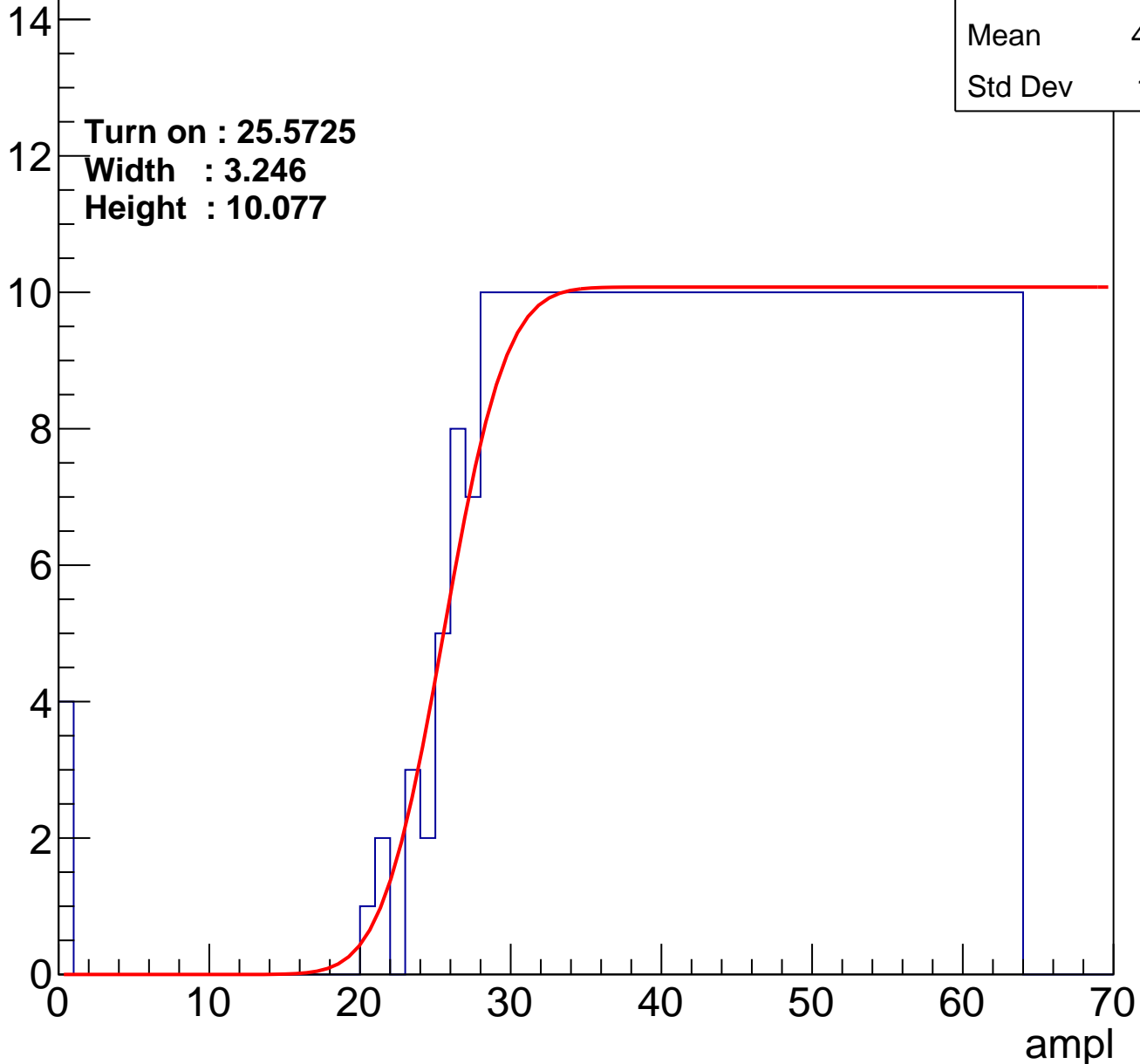
Entries	392
Mean	43.57
Std Dev	12.11

Turn on : 25.5725

Width : 3.246

Height : 10.077

Entry



B1L100S, U4-ch4

calib_packv5_042523_0143.root, FC#4, port A2

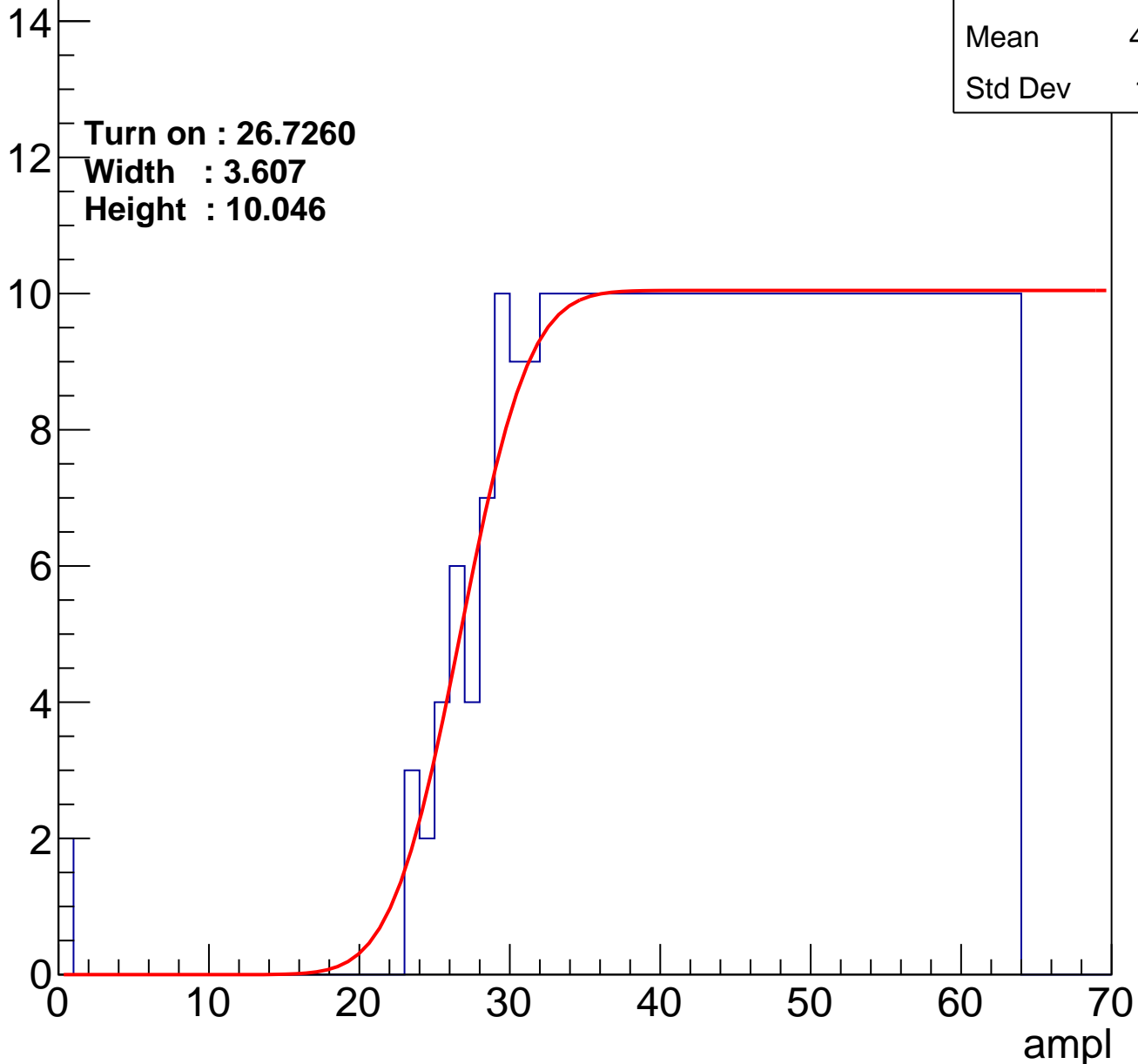
Entries	376
Mean	44.46
Std Dev	11.41

Turn on : 26.7260

Width : 3.607

Height : 10.046

Entry



B1L100S, U4-ch5

calib_packv5_042523_0143.root, FC#4, port A2

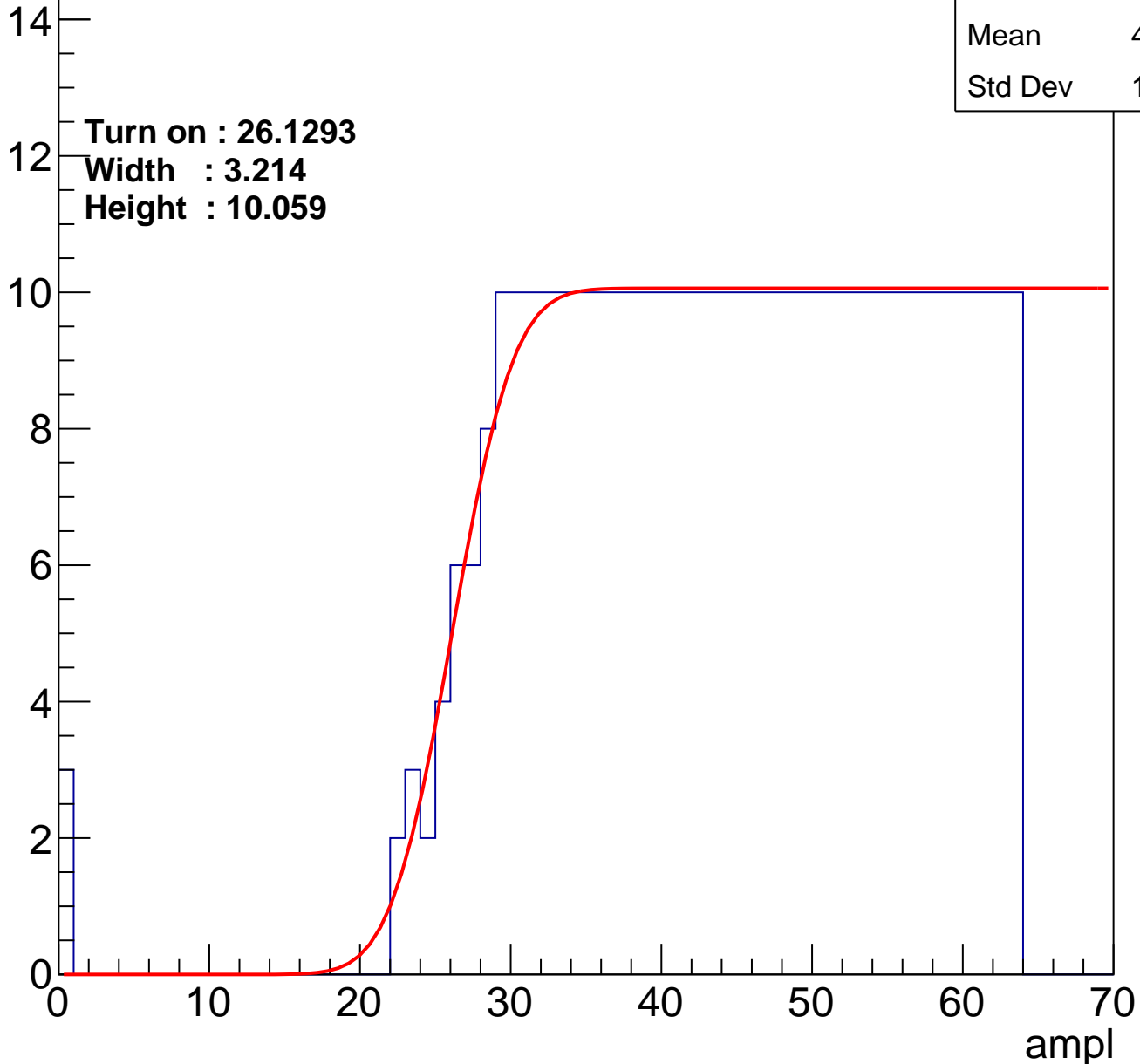
Entries	384
Mean	44.02
Std Dev	11.77

Turn on : 26.1293

Width : 3.214

Height : 10.059

Entry



B1L100S, U4-ch6

calib_packv5_042523_0143.root, FC#4, port A2

Entries	388
Mean	43.96
Std Dev	11.51

Turn on : 25.4158

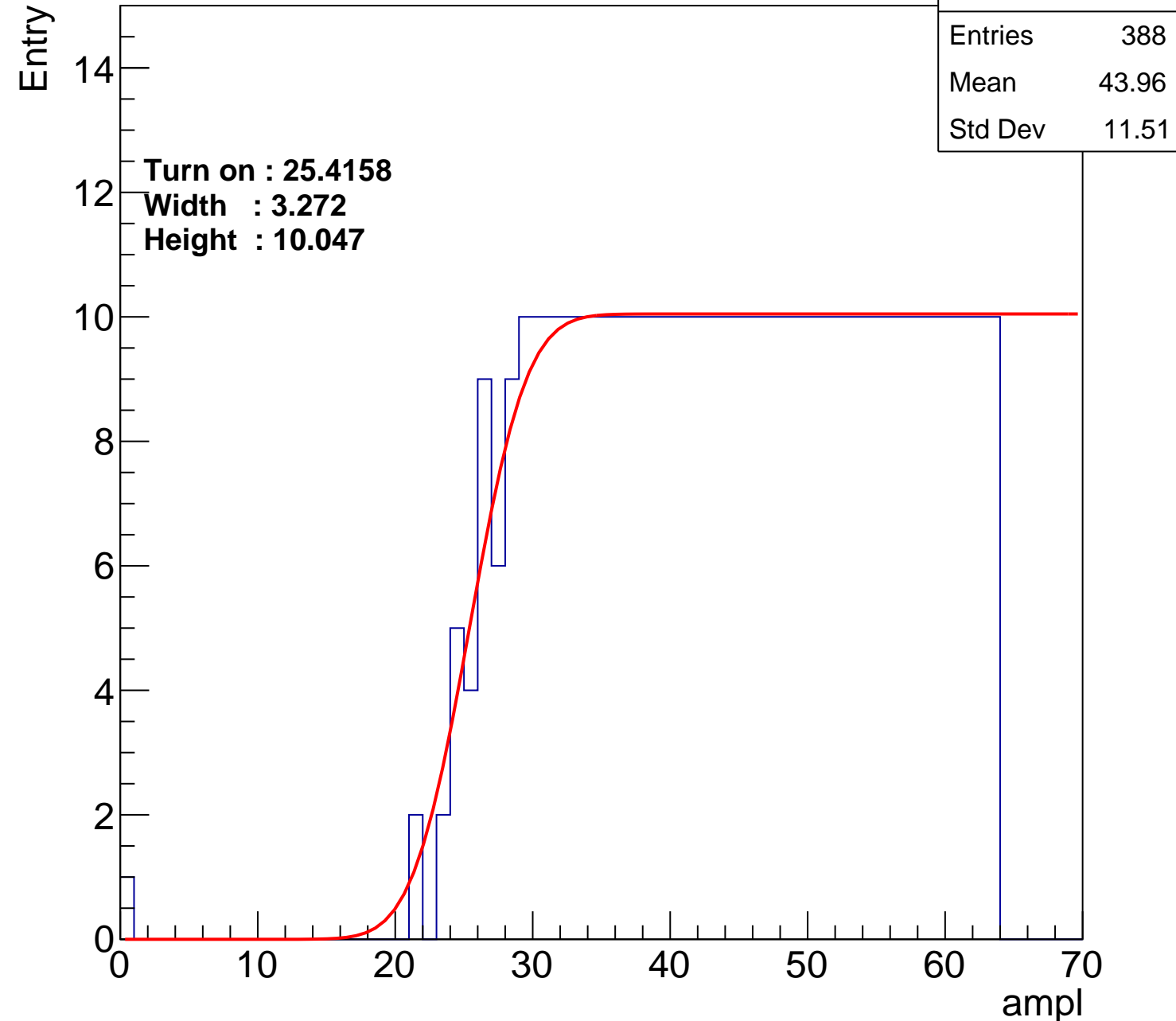
Width : 3.272

Height : 10.047

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch7

calib_packv5_042523_0143.root, FC#4, port A2

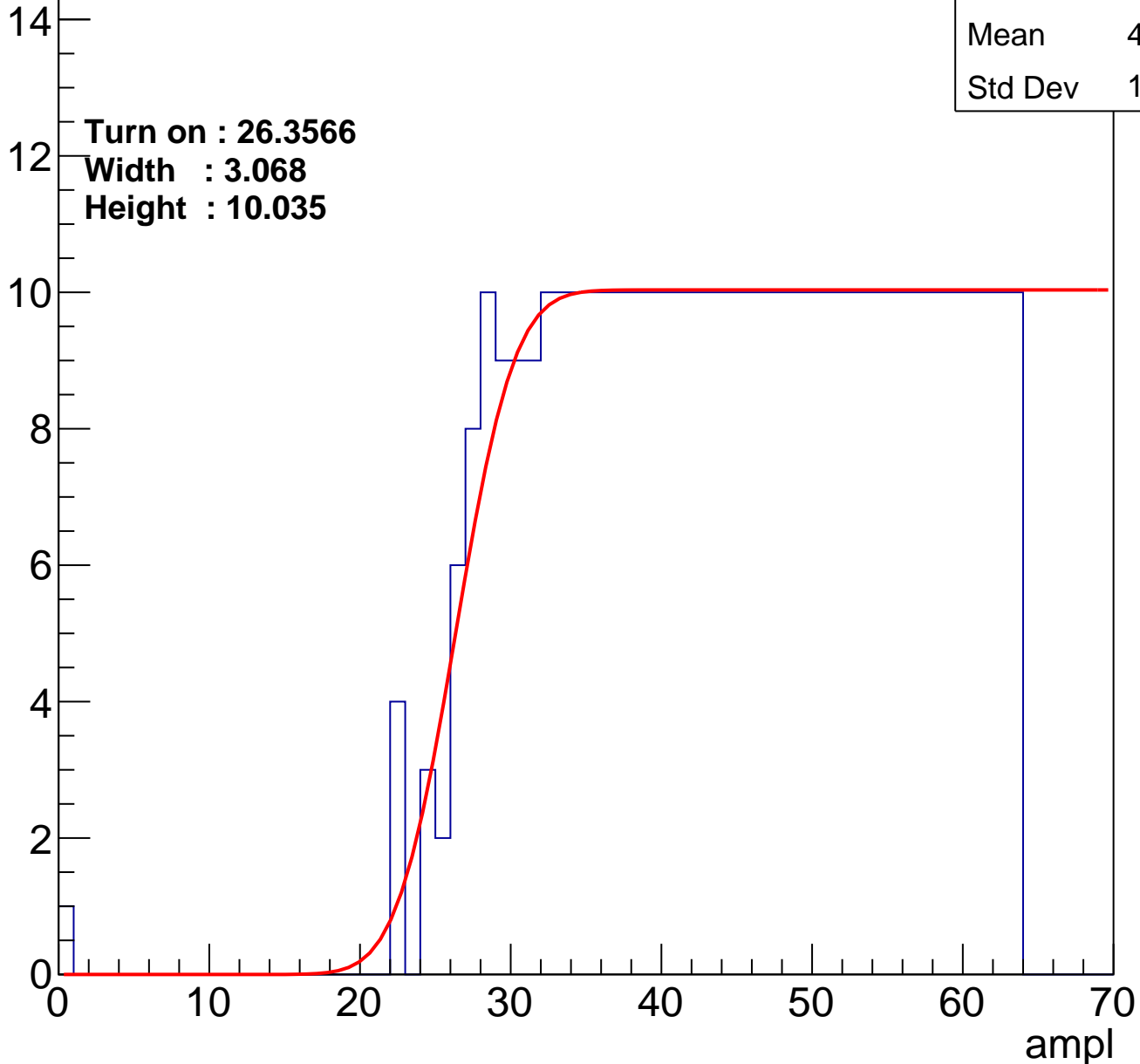
Entries	381
Mean	44.28
Std Dev	11.35

Turn on : 26.3566

Width : 3.068

Height : 10.035

Entry



B1L100S, U4-ch8

calib_packv5_042523_0143.root, FC#4, port A2

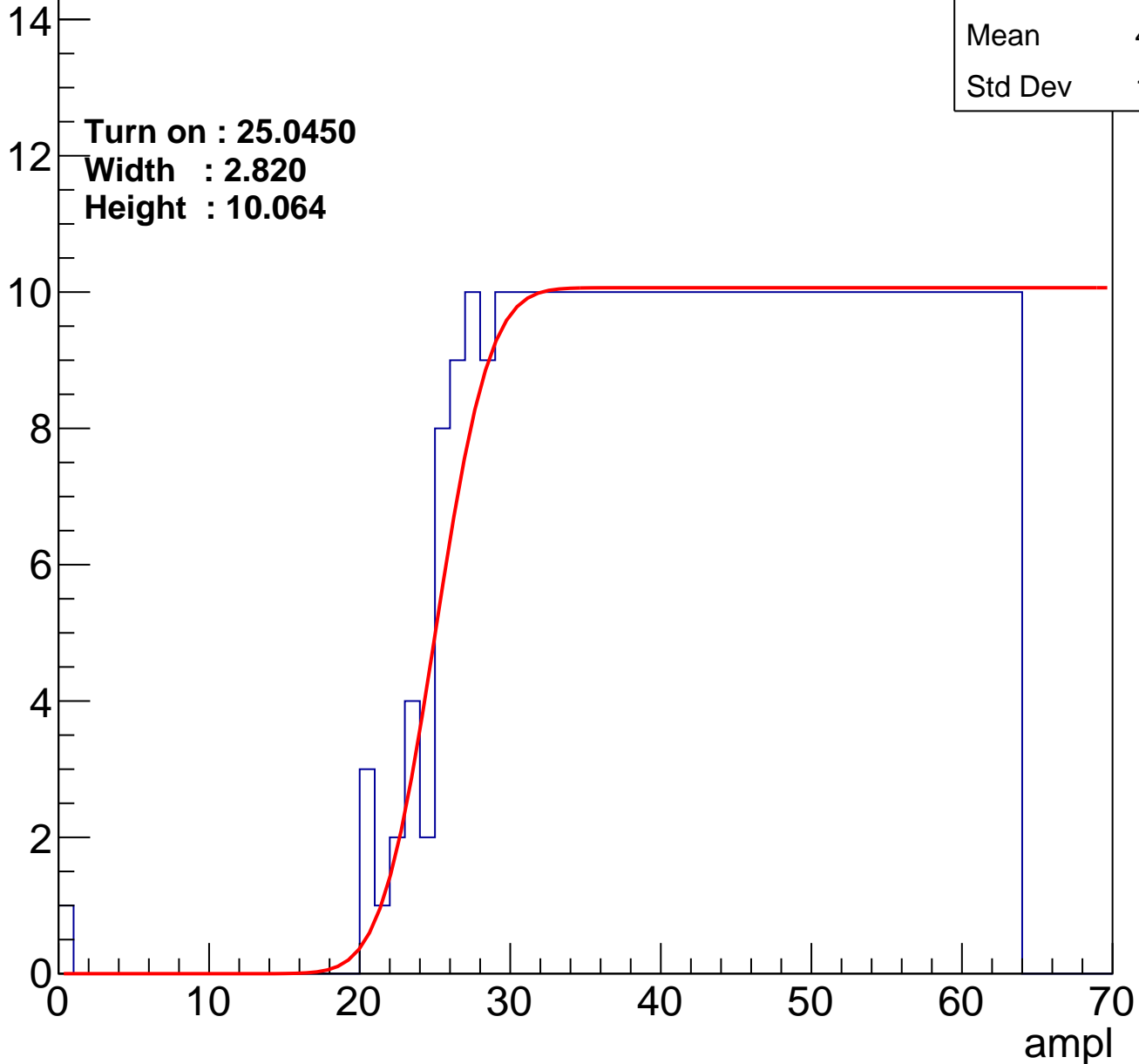
Entries	399
Mean	43.41
Std Dev	11.81

Turn on : 25.0450

Width : 2.820

Height : 10.064

Entry



B1L100S, U4-ch9

calib_packv5_042523_0143.root, FC#4, port A2

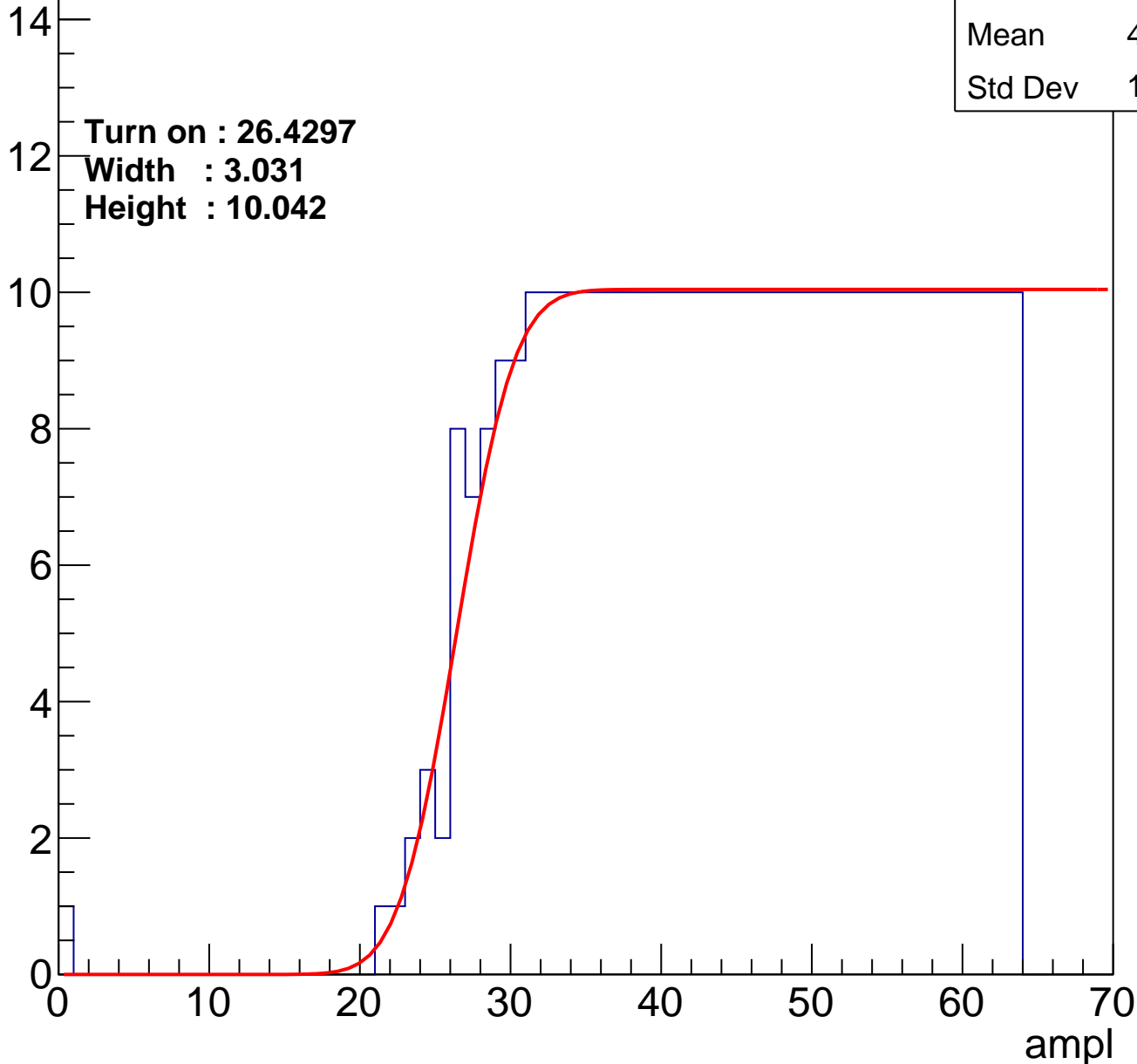
Entries	381
Mean	44.29
Std Dev	11.35

Turn on : 26.4297

Width : 3.031

Height : 10.042

Entry



B1L100S, U4-ch10

calib_packv5_042523_0143.root, FC#4, port A2

Entries	367
Mean	44.94
Std Dev	11.04

Turn on : 27.8324

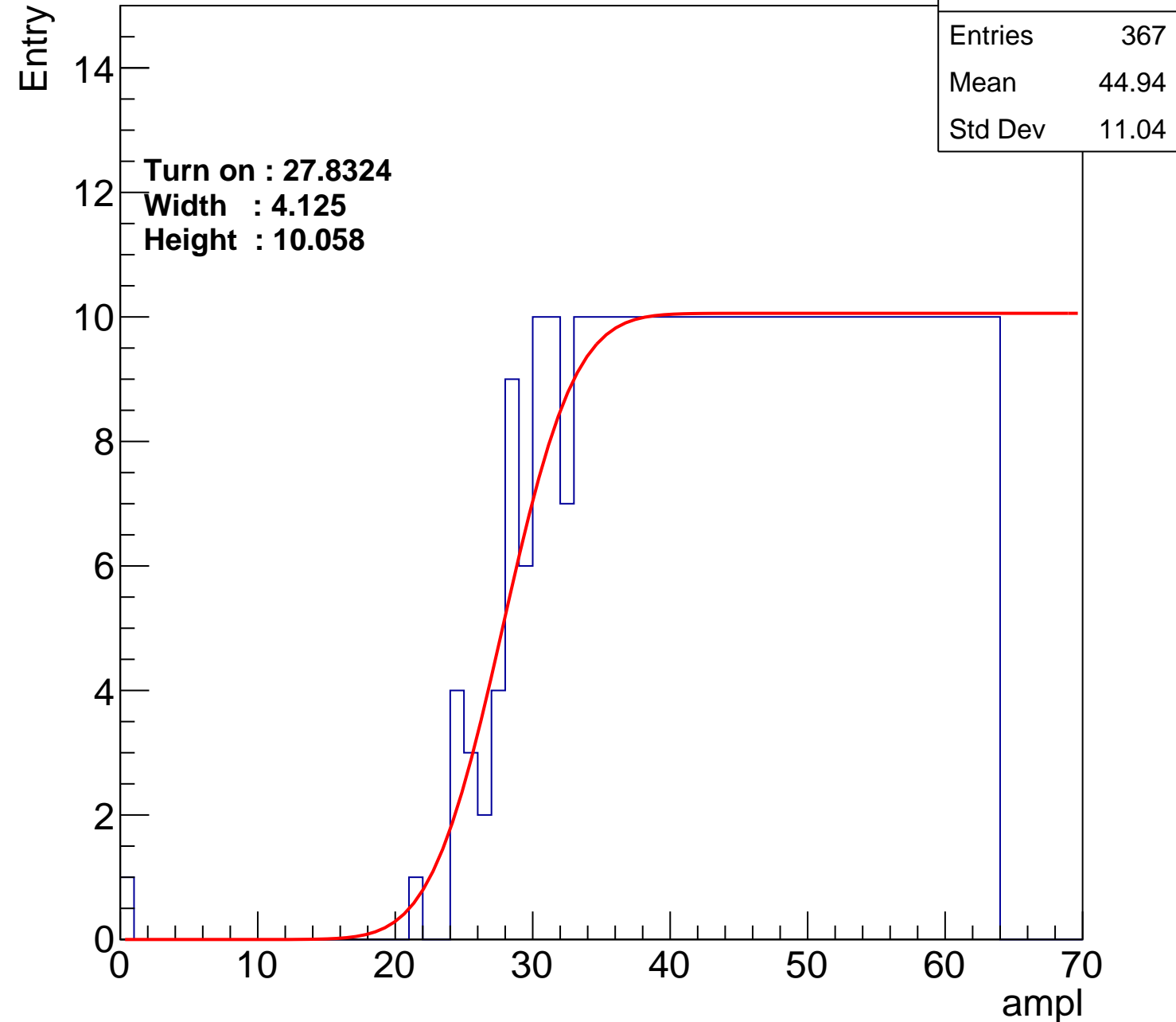
Width : 4.125

Height : 10.058

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch11

calib_packv5_042523_0143.root, FC#4, port A2

Entries	366
Mean	44.92
Std Dev	11.21

Turn on : 27.8291

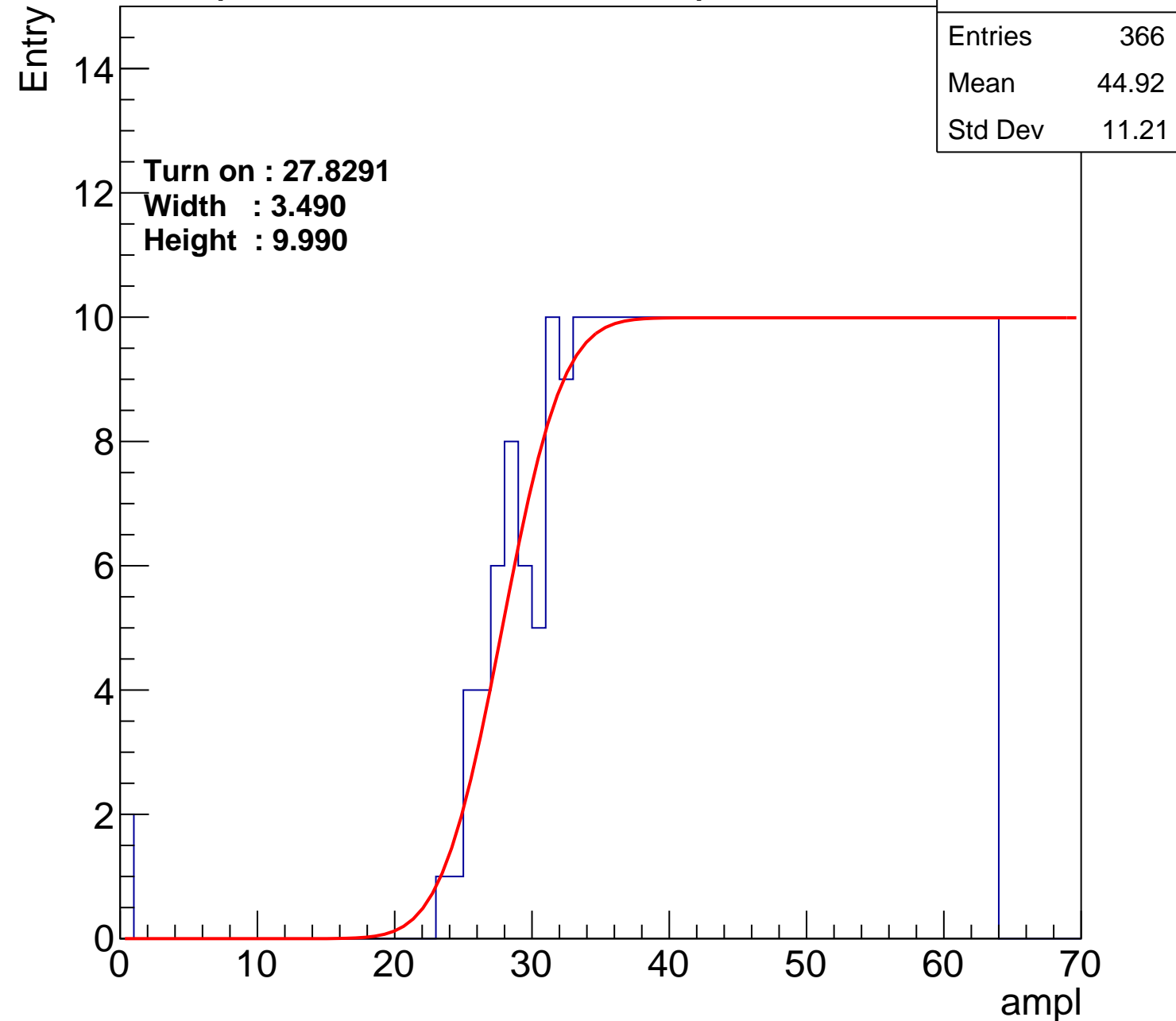
Width : 3.490

Height : 9.990

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch12

calib_packv5_042523_0143.root, FC#4, port A2

Entries	379
Mean	44.27
Std Dev	11.63

Turn on : 26.4845

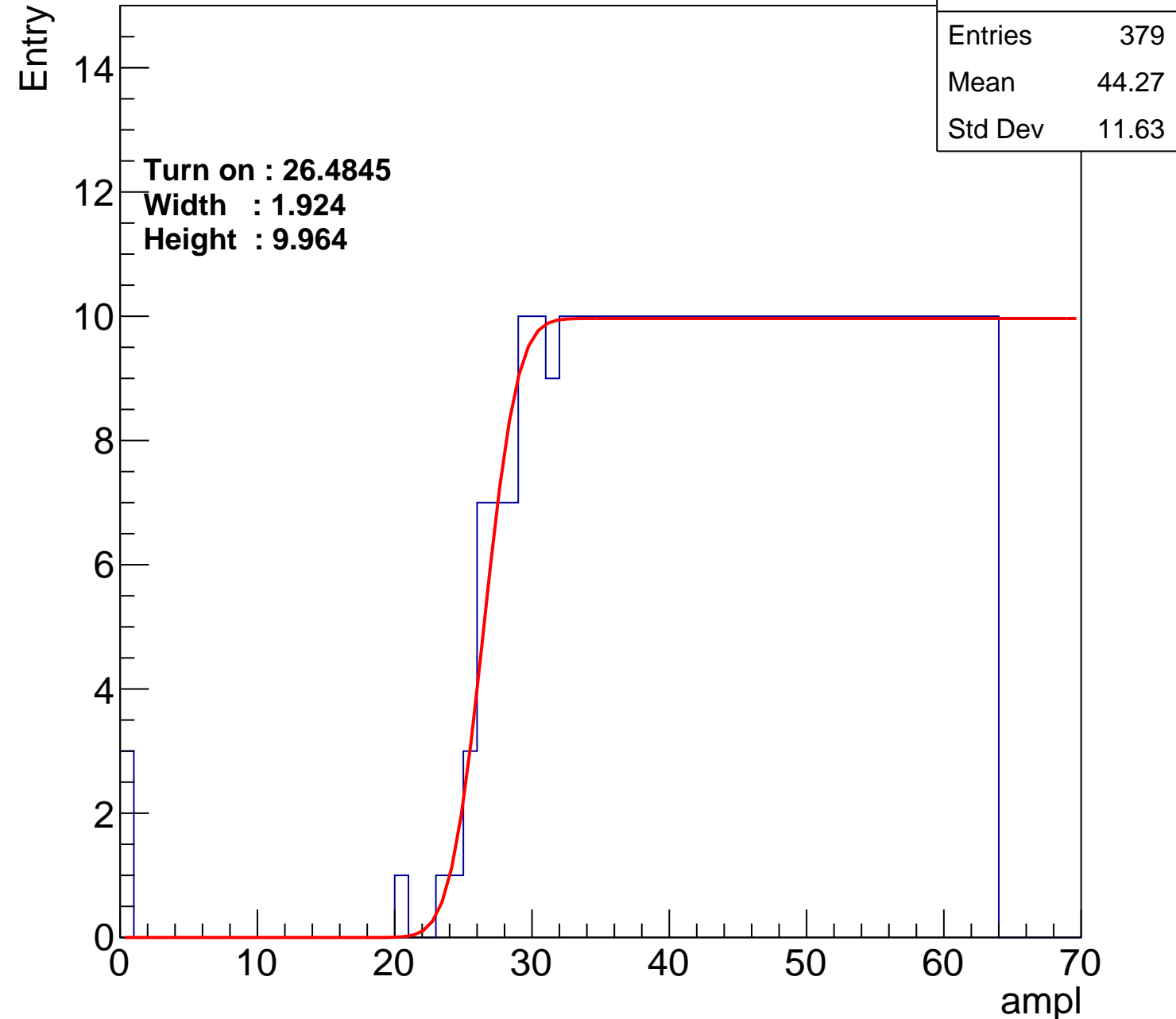
Width : 1.924

Height : 9.964

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch13

calib_packv5_042523_0143.root, FC#4, port A2

Entries	377
Mean	44.25
Std Dev	11.85

Turn on : 26.7192

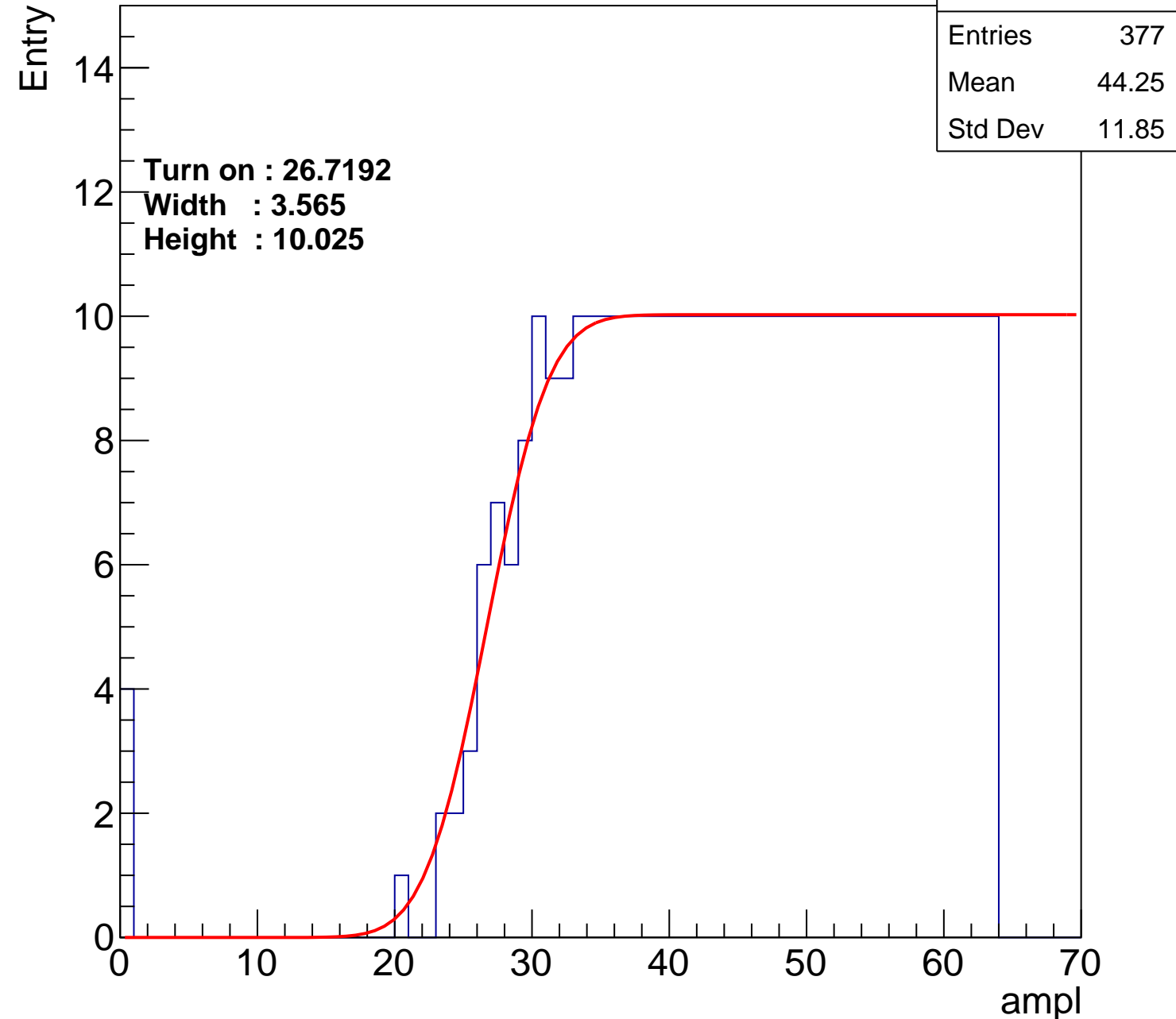
Width : 3.565

Height : 10.025

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch14

calib_packv5_042523_0143.root, FC#4, port A2

Entries	368
Mean	44.8
Std Dev	11.3

Turn on : 27.8916

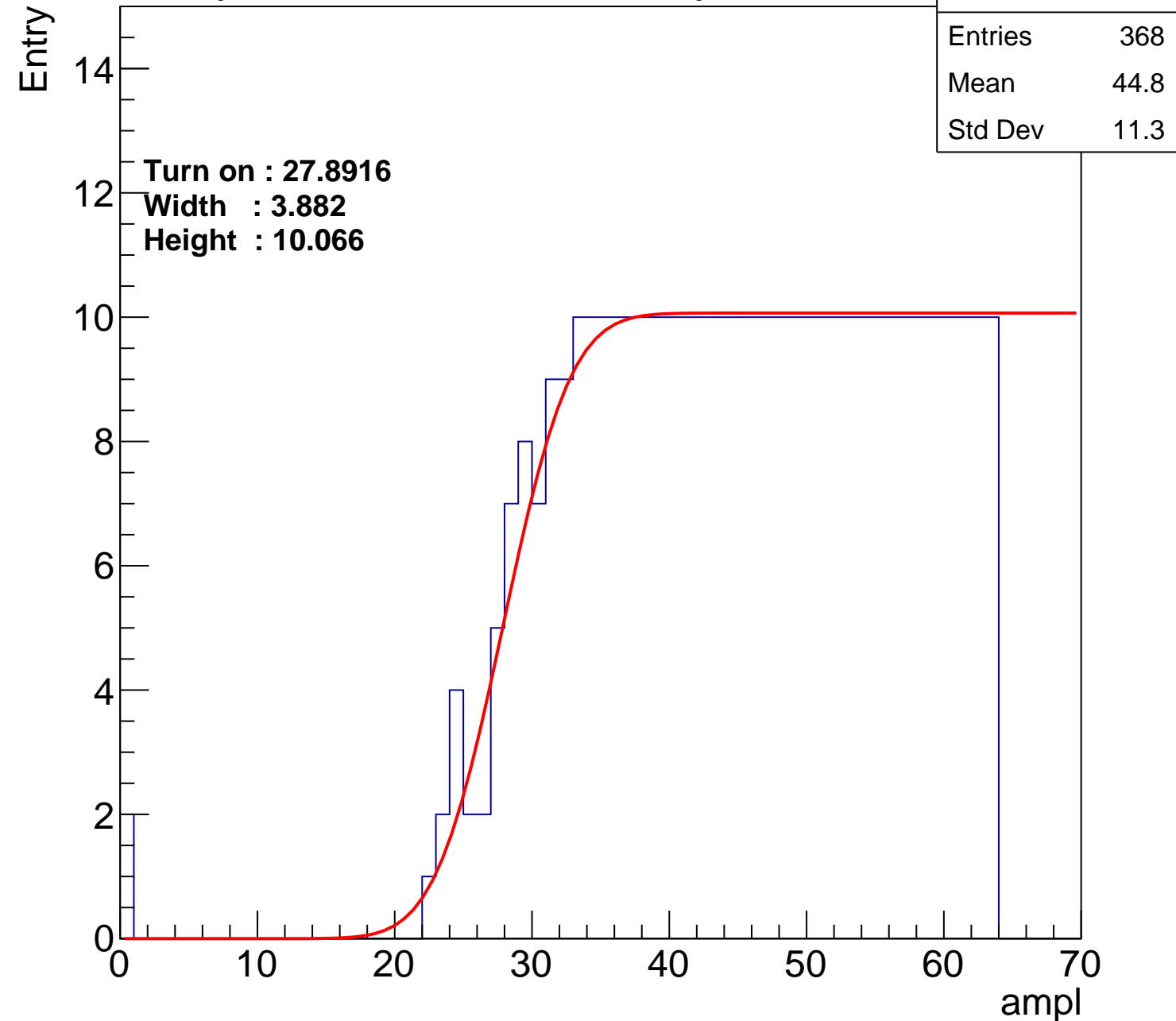
Width : 3.882

Height : 10.066

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch15

calib_packv5_042523_0143.root, FC#4, port A2

Entries	367
Mean	44.88
Std Dev	11.3

Turn on : 27.5789

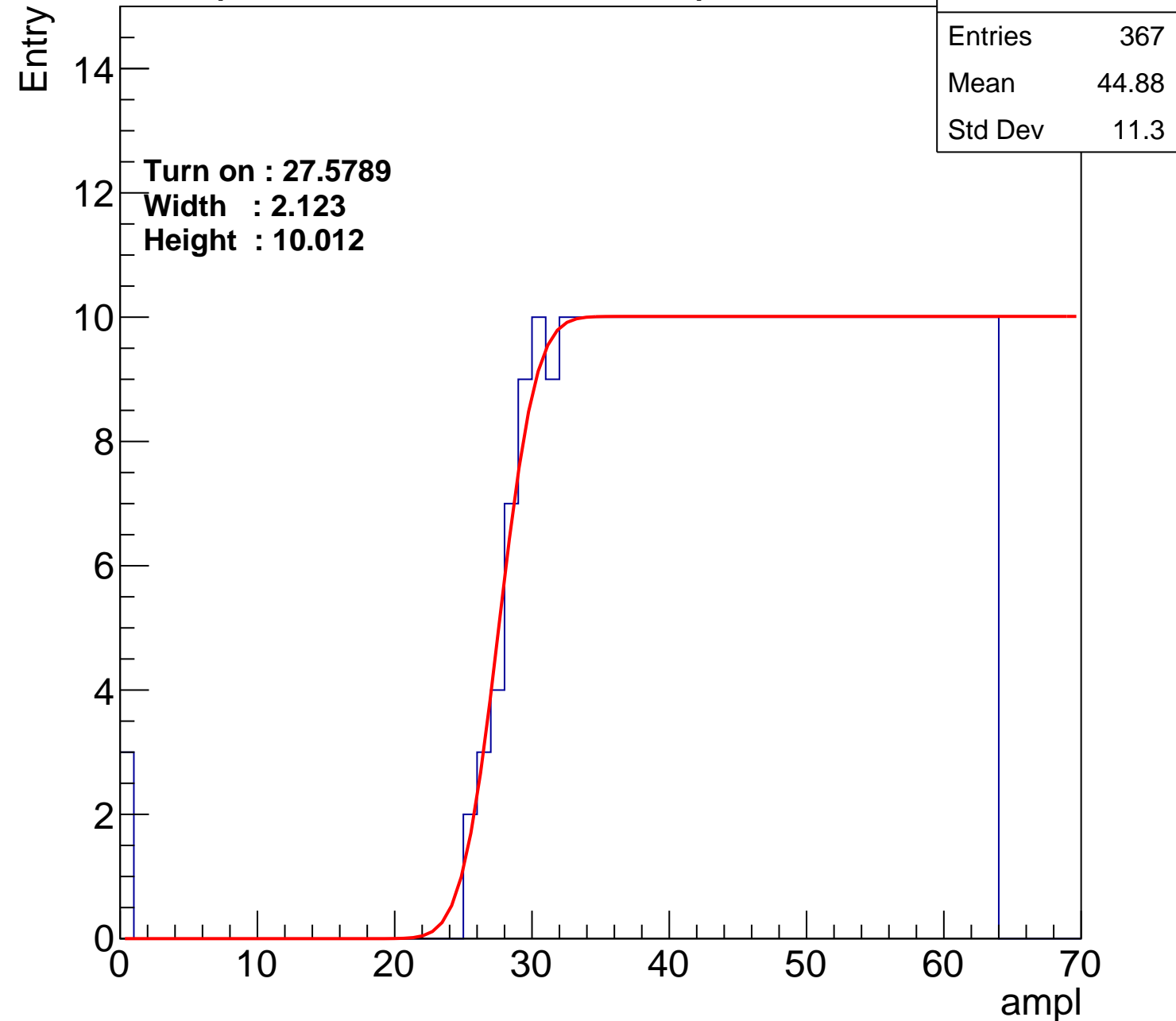
Width : 2.123

Height : 10.012

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch16

calib_packv5_042523_0143.root, FC#4, port A2

Entries	377
Mean	44.5
Std Dev	11.21

Turn on : 26.2497

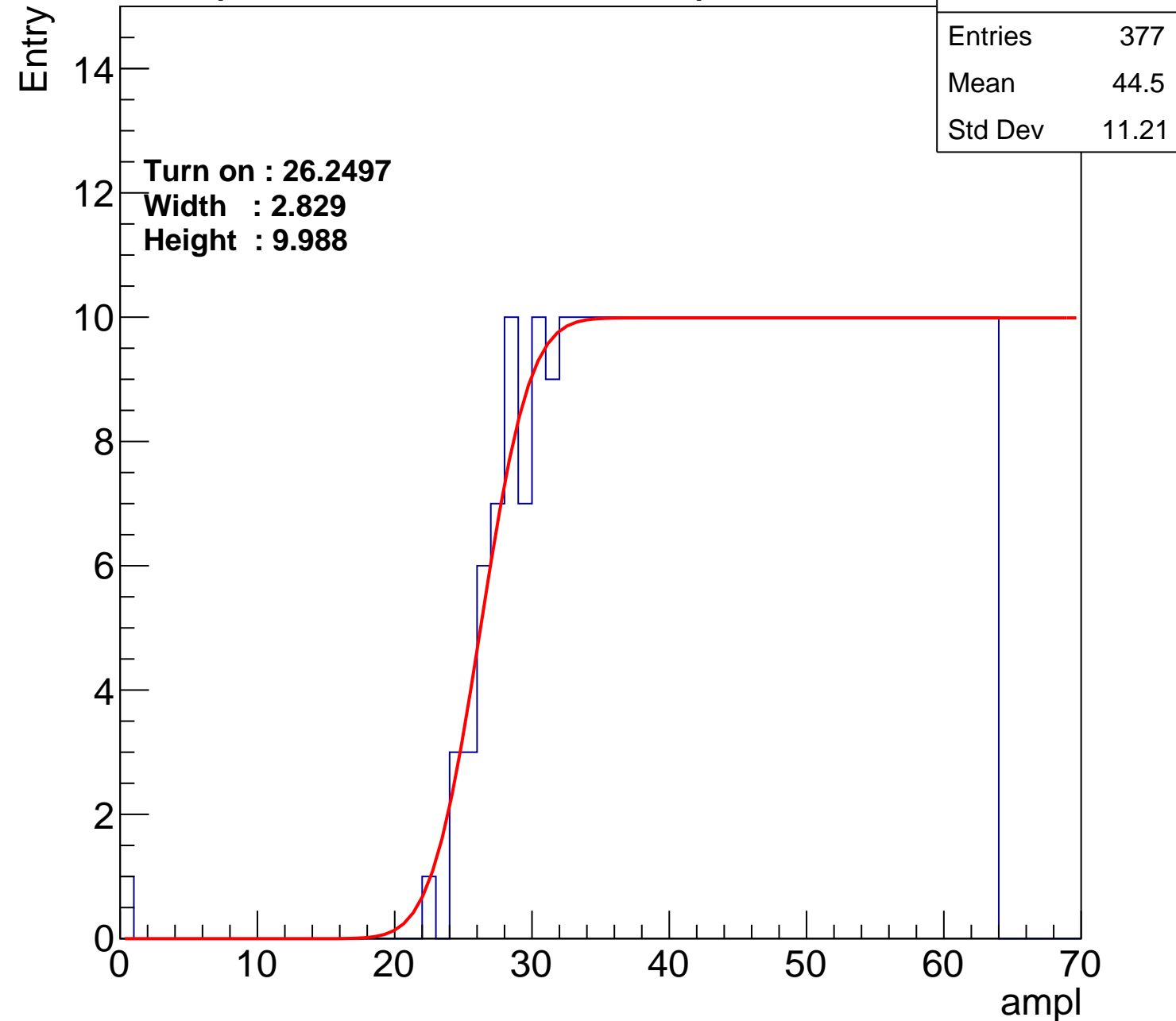
Width : 2.829

Height : 9.988

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch17

calib_packv5_042523_0143.root, FC#4, port A2

Entries	380
Mean	44.23
Std Dev	11.65

Turn on : 26.8789

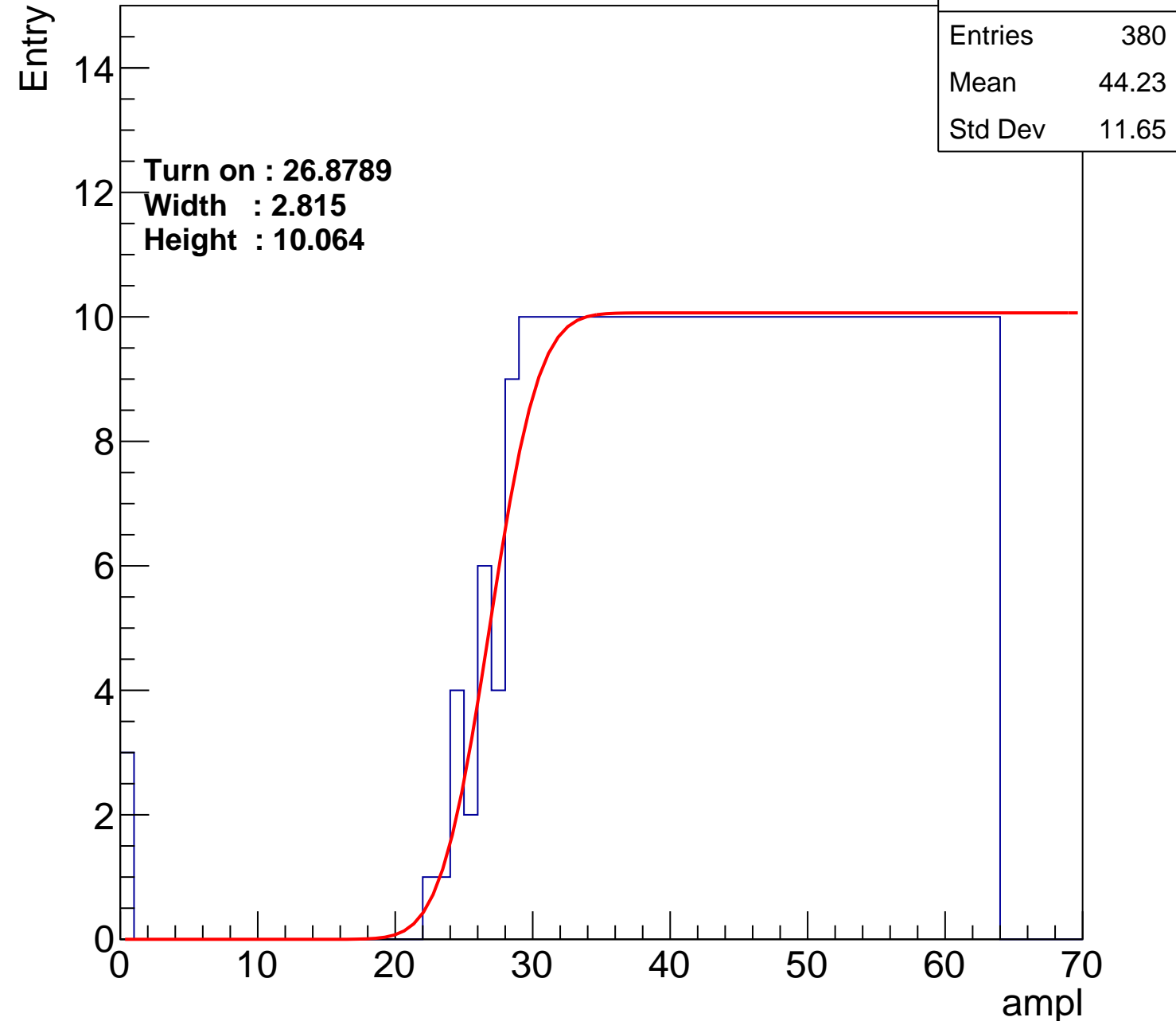
Width : 2.815

Height : 10.064

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch18

calib_packv5_042523_0143.root, FC#4, port A2

Entries	374
Mean	44.63
Std Dev	11.16

Turn on : 26.9182

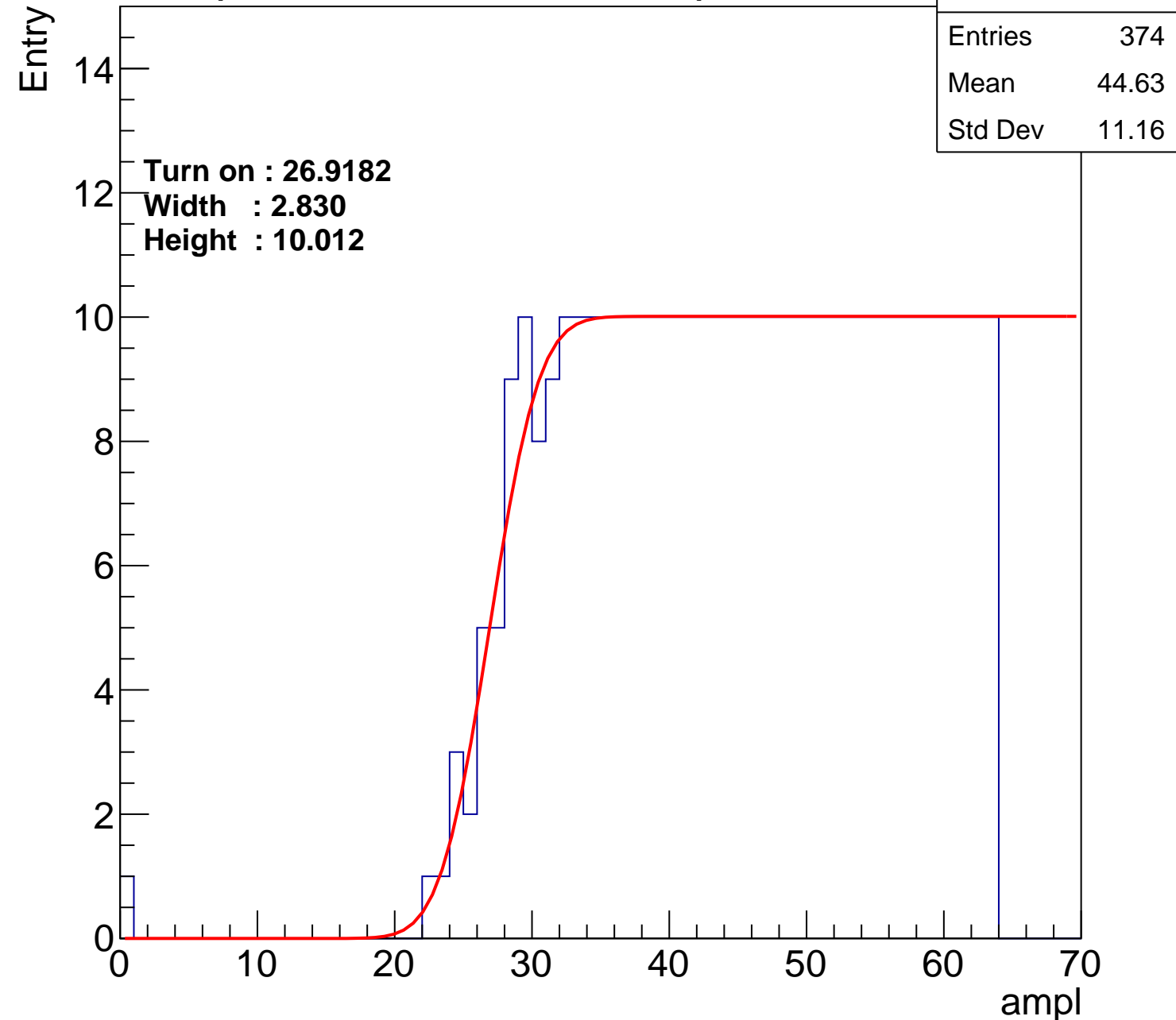
Width : 2.830

Height : 10.012

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch19

calib_packv5_042523_0143.root, FC#4, port A2

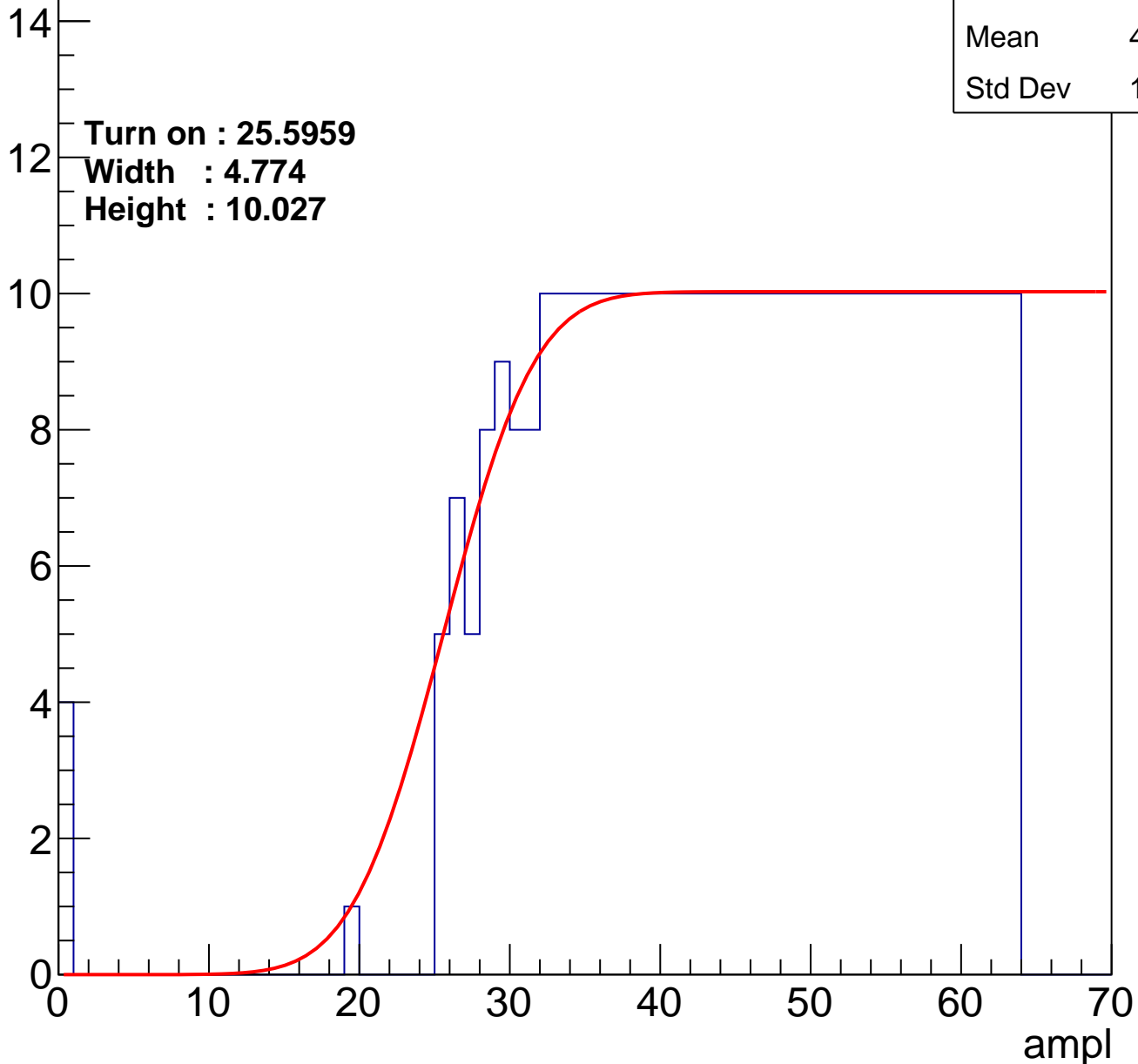
Entries	375
Mean	44.36
Std Dev	11.78

Turn on : 25.5959

Width : 4.774

Height : 10.027

Entry



B1L100S, U4-ch20

calib_packv5_042523_0143.root, FC#4, port A2

Entries	356
Mean	45.4
Std Dev	10.97

Turn on : 29.2207

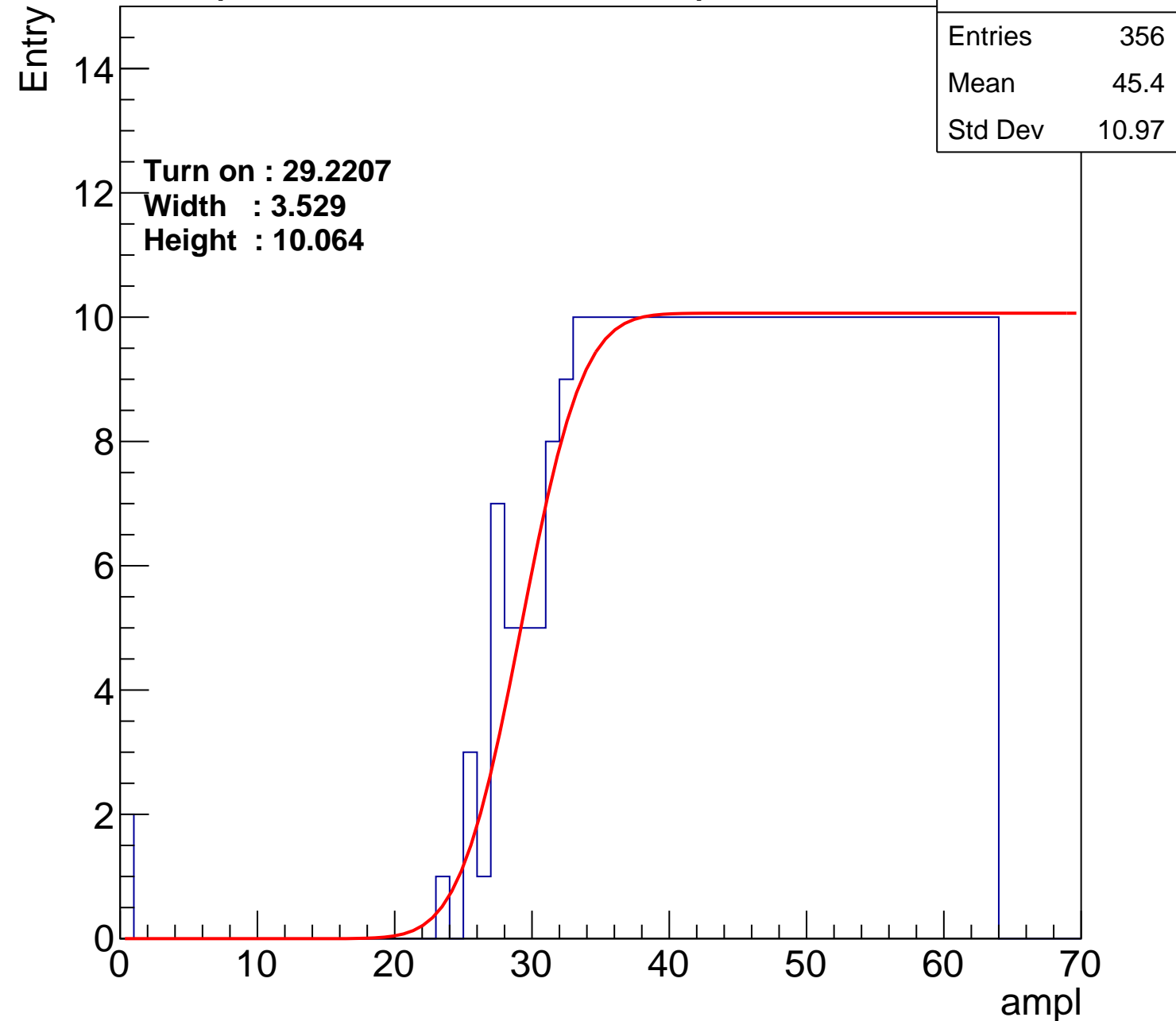
Width : 3.529

Height : 10.064

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch21

calib_packv5_042523_0143.root, FC#4, port A2

Entries	389
Mean	43.53
Std Dev	12.45

Turn on : 26.3182

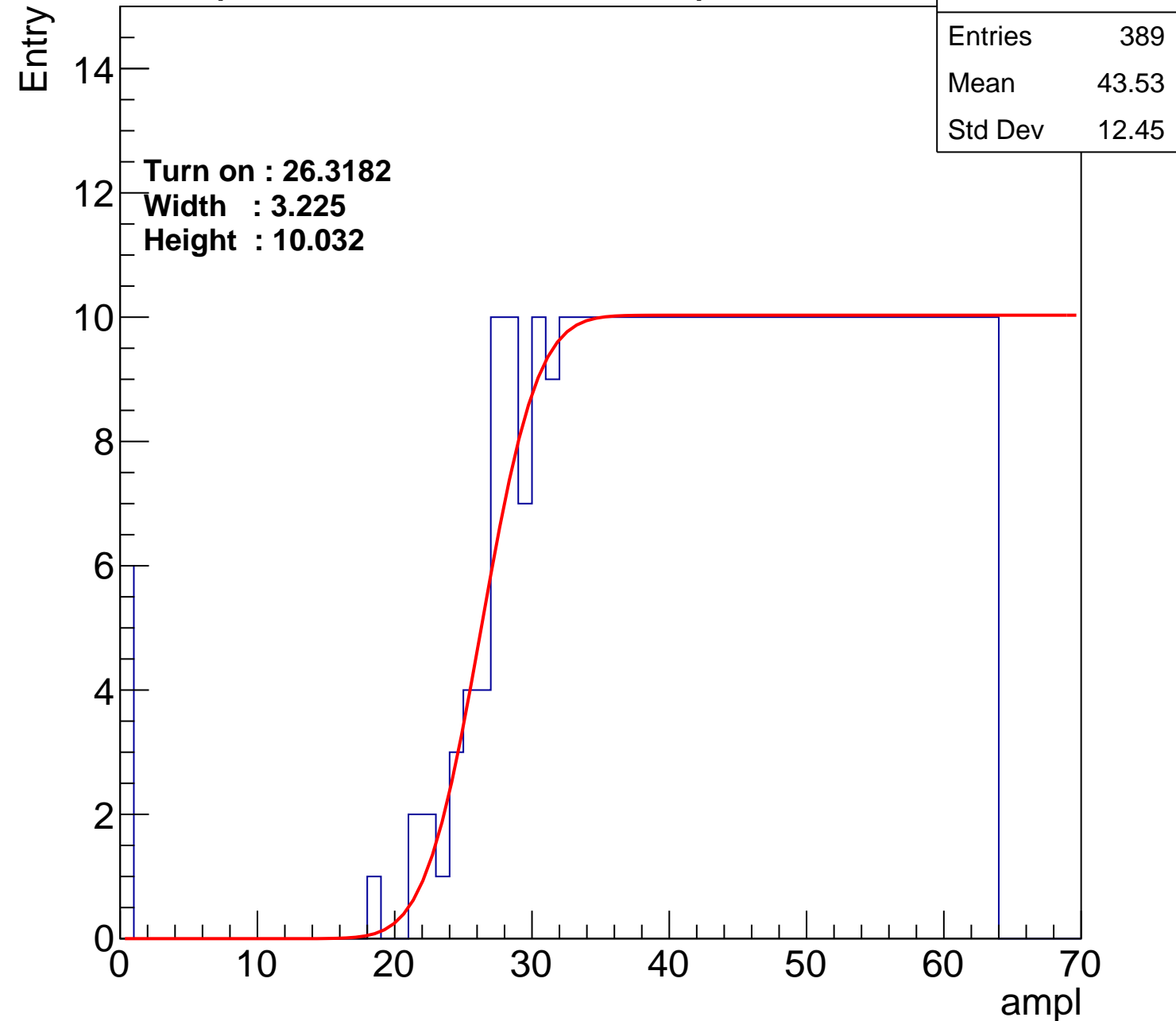
Width : 3.225

Height : 10.032

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch22

calib_packv5_042523_0143.root, FC#4, port A2

Entries	384
Mean	44.13
Std Dev	11.45

Turn on : 26.0445

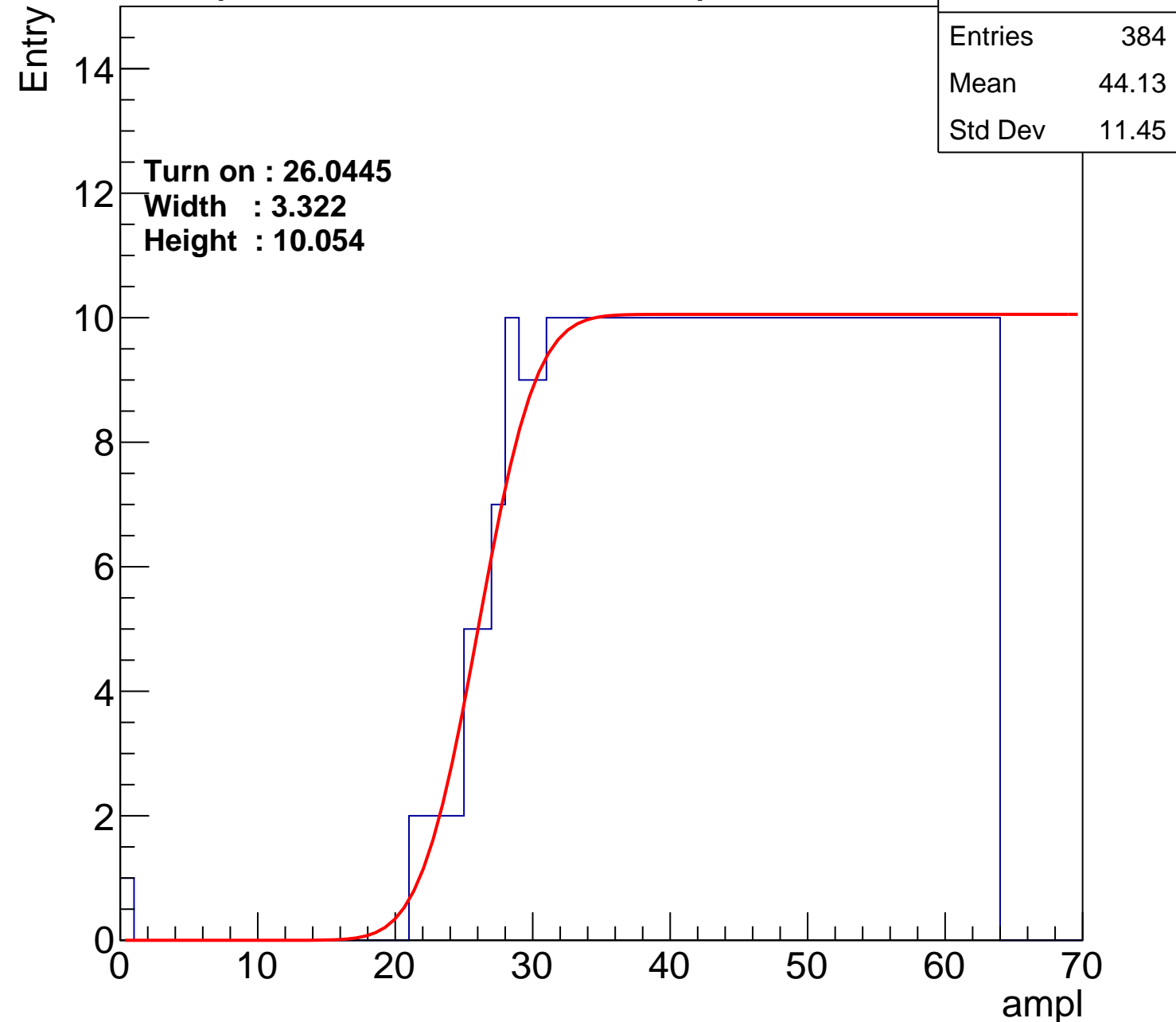
Width : 3.322

Height : 10.054

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch23

calib_packv5_042523_0143.root, FC#4, port A2

Entries	379
Mean	43.97
Std Dev	12.38

Turn on : 26.7959

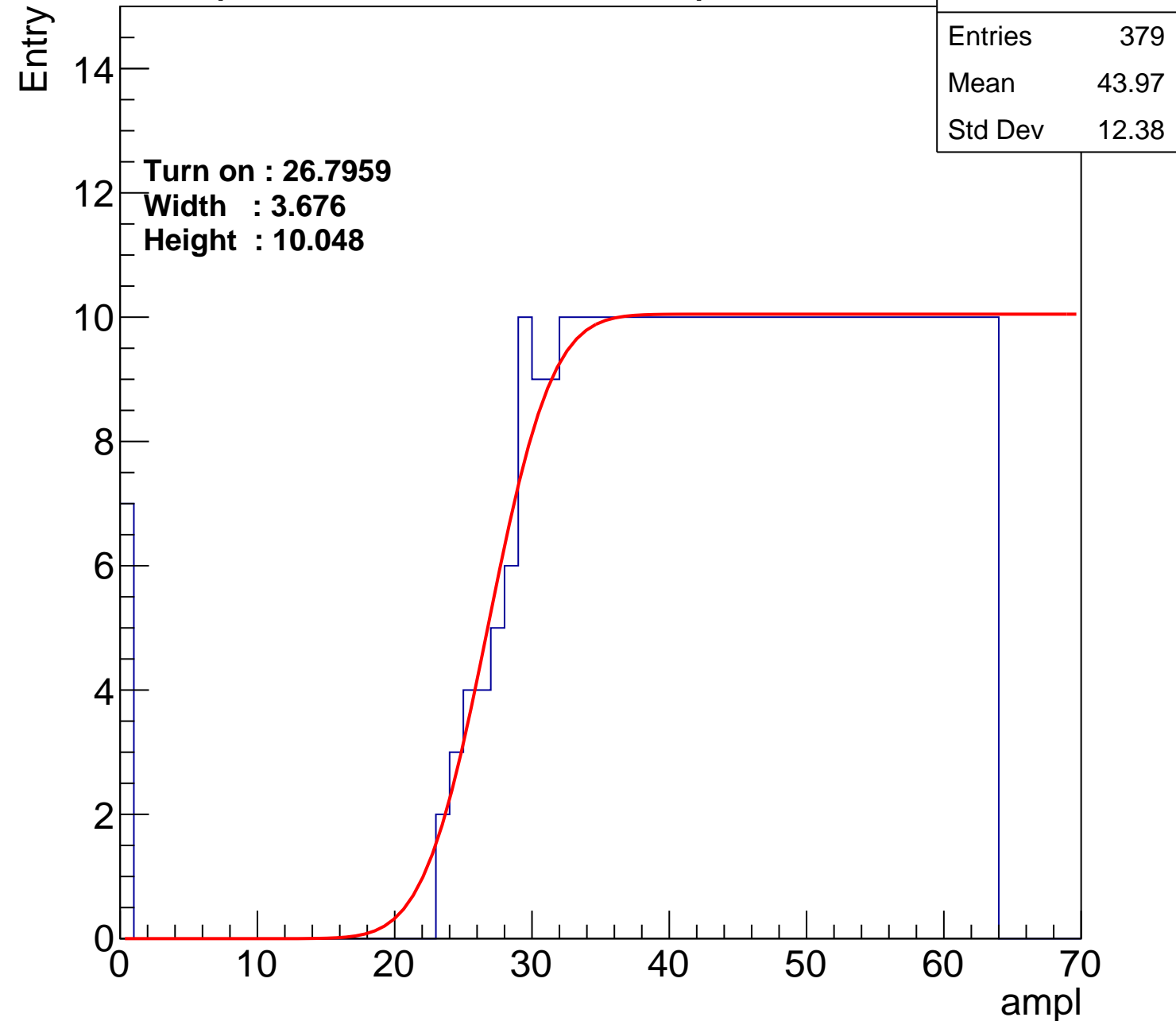
Width : 3.676

Height : 10.048

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch24

calib_packv5_042523_0143.root, FC#4, port A2

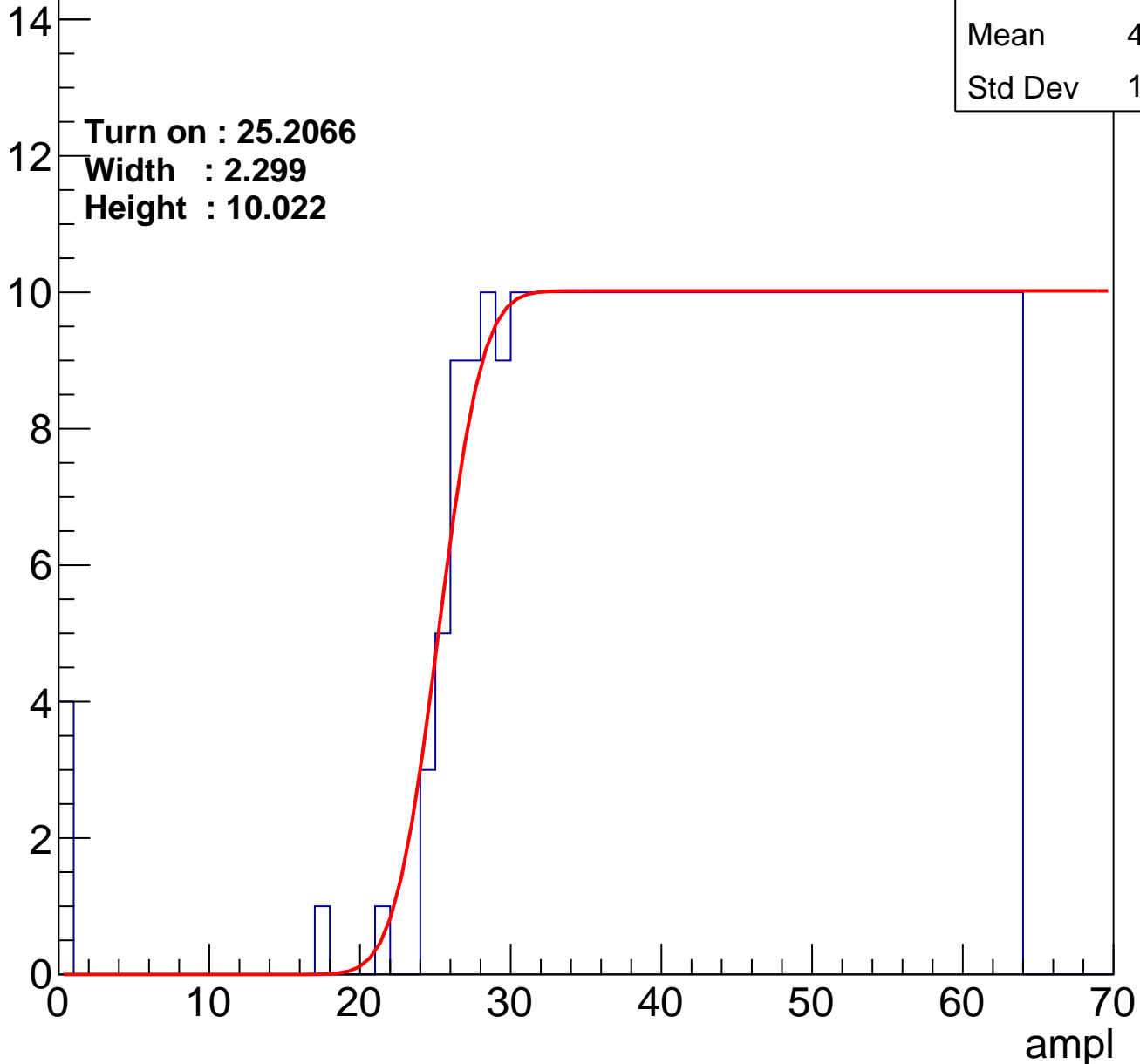
Entries	391
Mean	43.64
Std Dev	12.06

Turn on : 25.2066

Width : 2.299

Height : 10.022

Entry



B1L100S, U4-ch25

calib_packv5_042523_0143.root, FC#4, port A2

Entries	383
Mean	44.06
Std Dev	11.75

Turn on : 26.5788

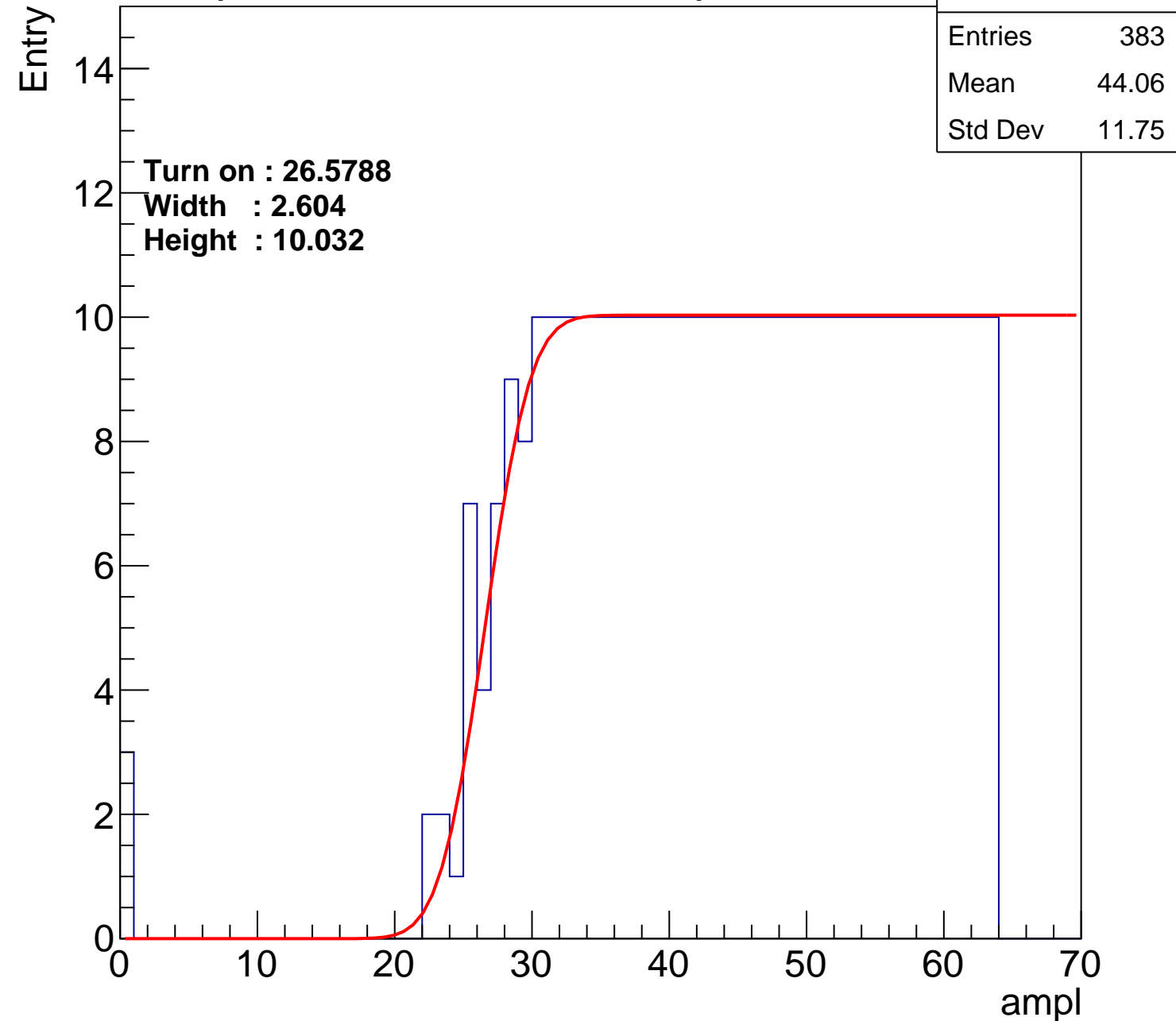
Width : 2.604

Height : 10.032

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch26

calib_packv5_042523_0143.root, FC#4, port A2

Entries	375
Mean	44.37
Std Dev	11.76

Turn on : 26.8138

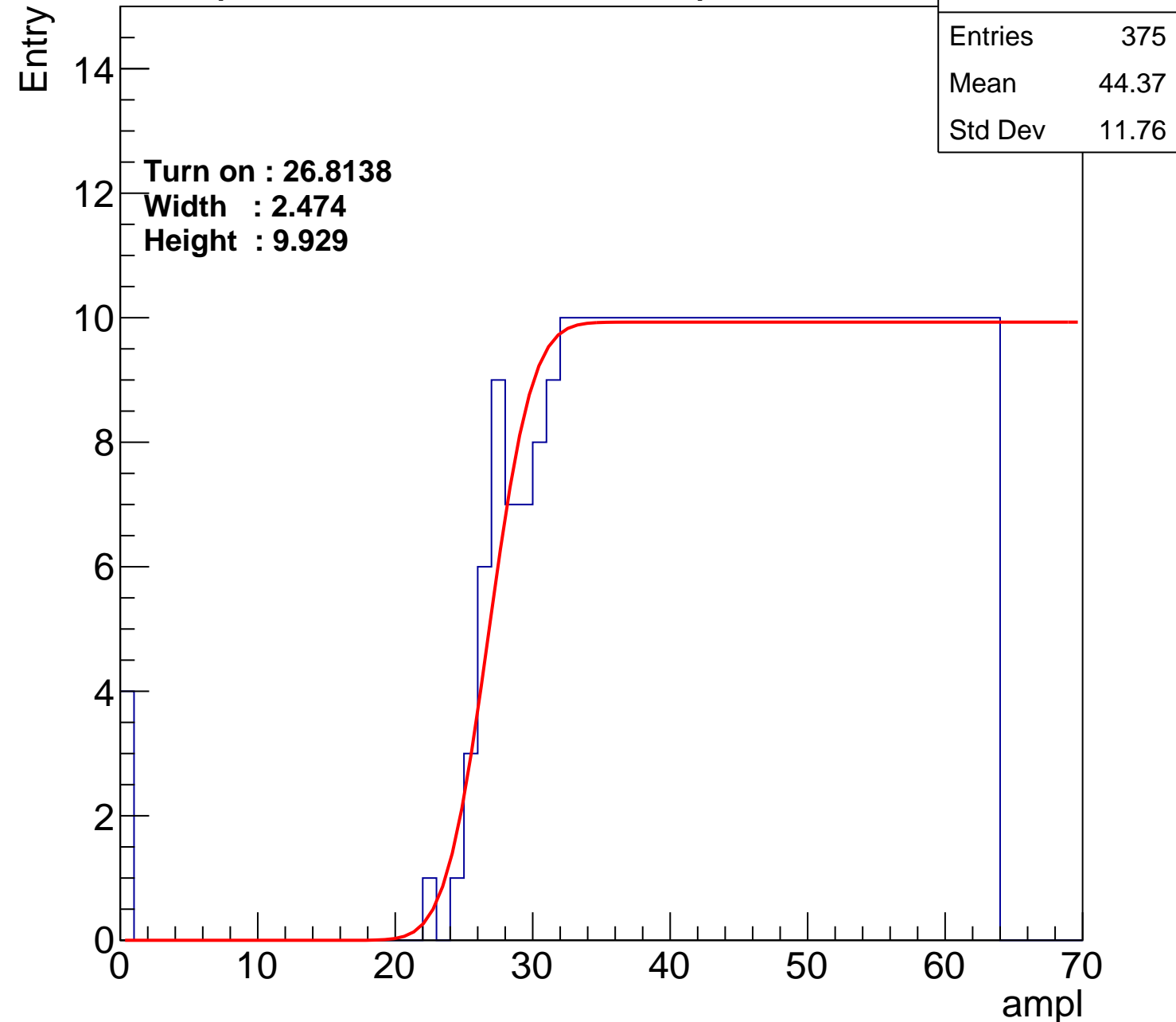
Width : 2.474

Height : 9.929

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch27

calib_packv5_042523_0143.root, FC#4, port A2

Entries	386
Mean	43.87
Std Dev	11.9

Turn on : 25.7875

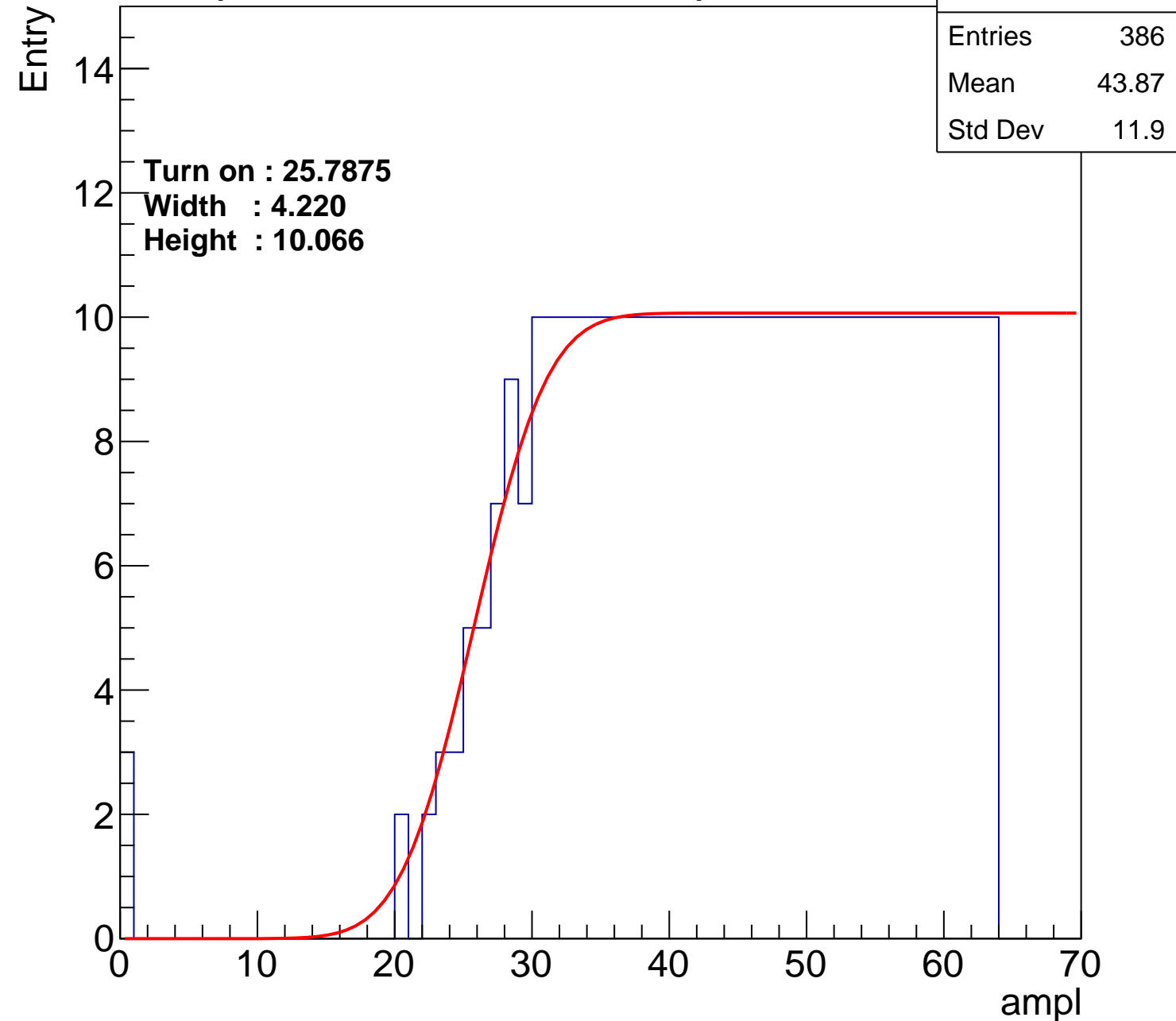
Width : 4.220

Height : 10.066

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch28

calib_packv5_042523_0143.root, FC#4, port A2

Entries	389
Mean	43.61
Std Dev	12.26

Turn on : 25.7445

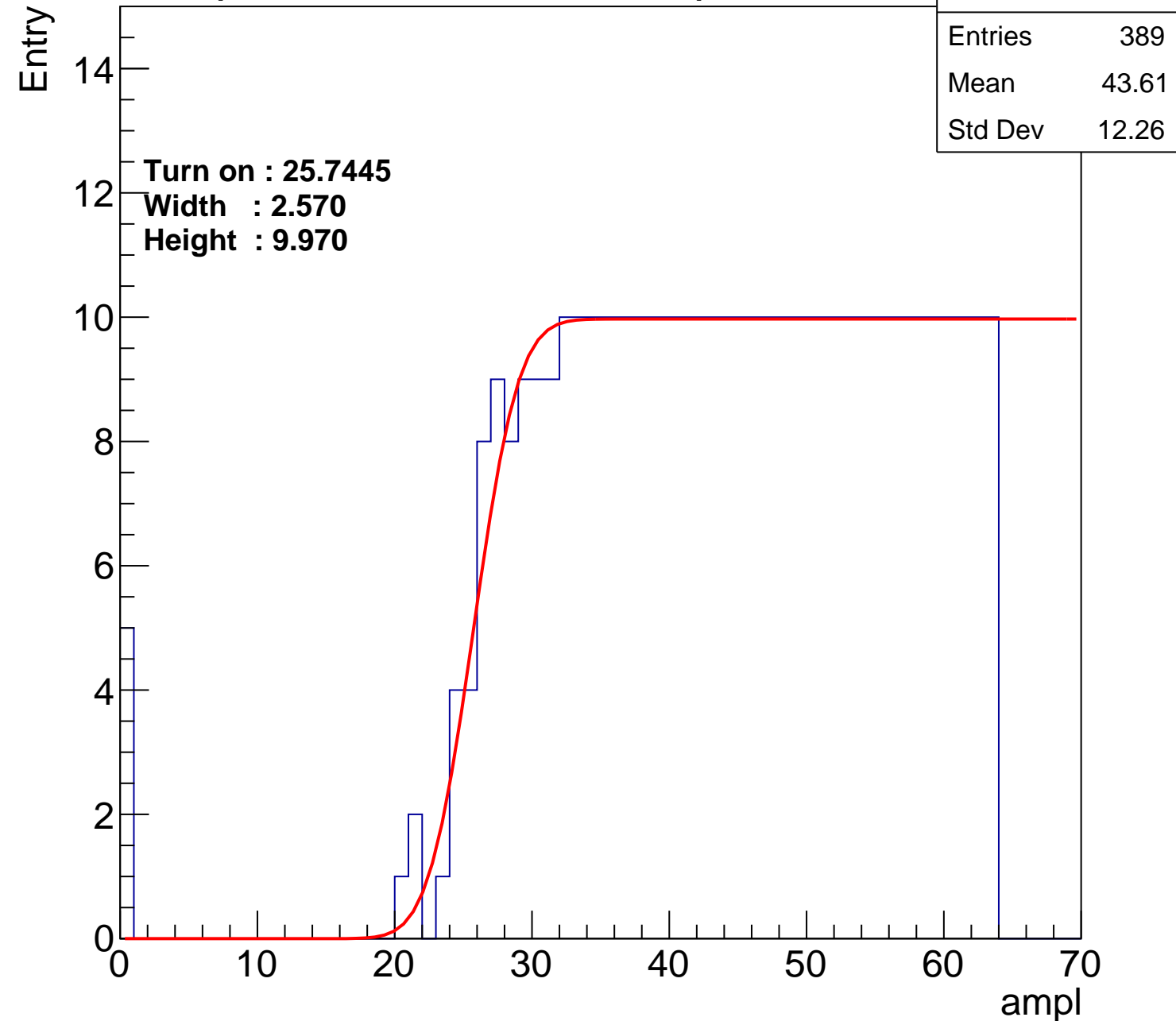
Width : 2.570

Height : 9.970

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch29

calib_packv5_042523_0143.root, FC#4, port A2

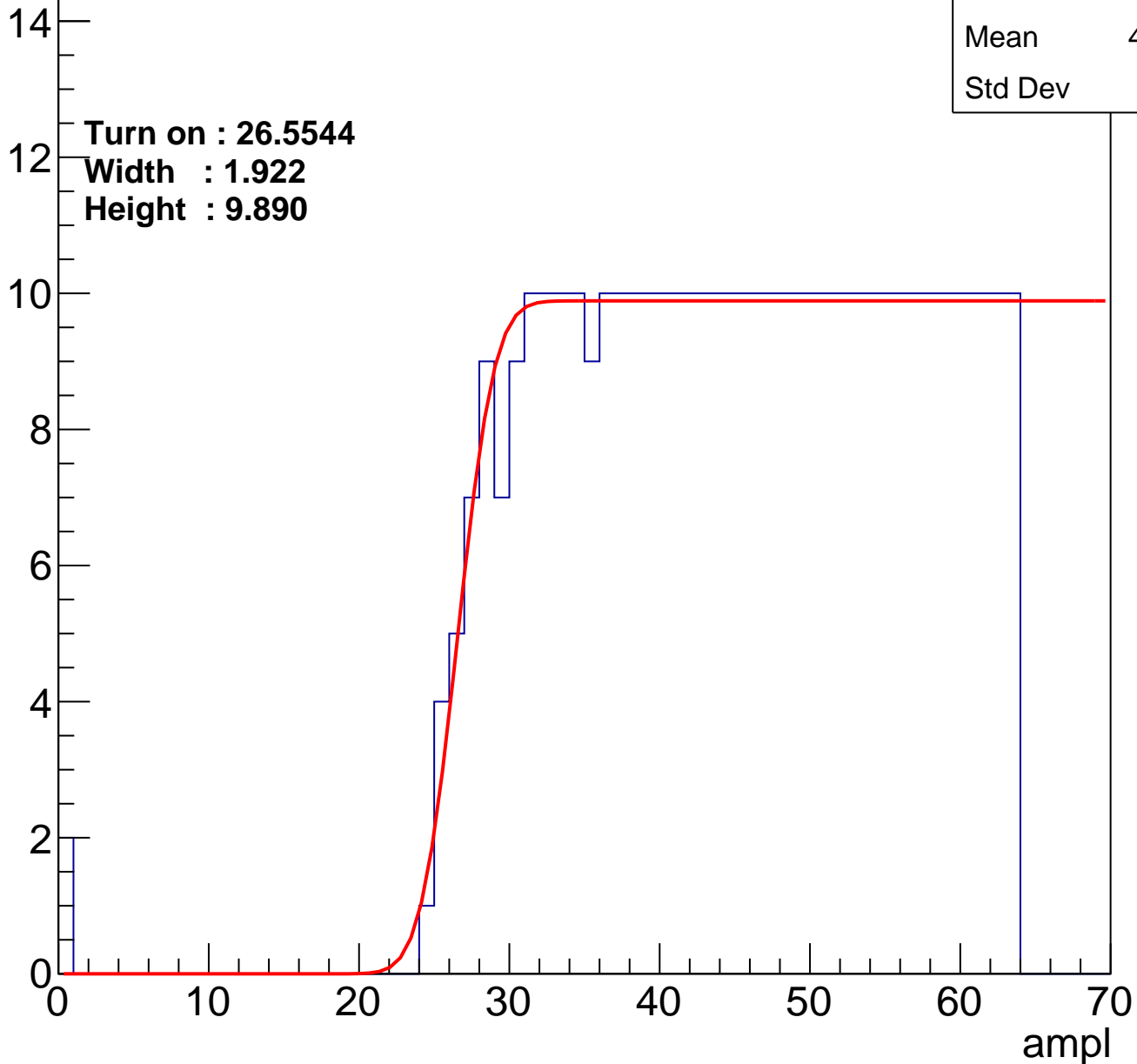
Entries	373
Mean	44.62
Std Dev	11.3

Turn on : 26.5544

Width : 1.922

Height : 9.890

Entry



B1L100S, U4-ch30

calib_packv5_042523_0143.root, FC#4, port A2

Entries	349
Mean	45.8
Std Dev	10.71

Turn on : 29.6216

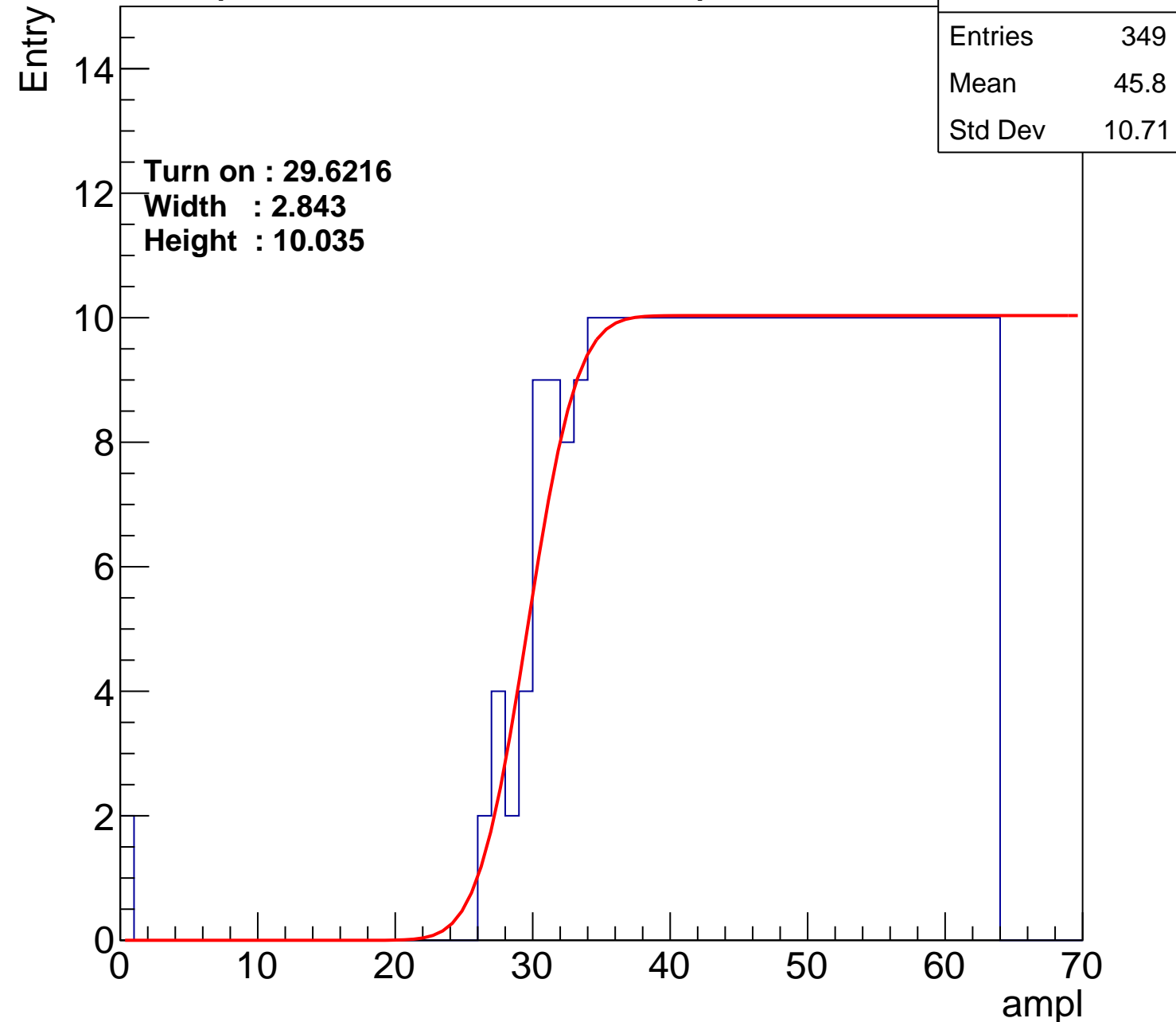
Width : 2.843

Height : 10.035

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch31

calib_packv5_042523_0143.root, FC#4, port A2

Entries	384
Mean	44.16
Std Dev	11.38

Turn on : 25.4133

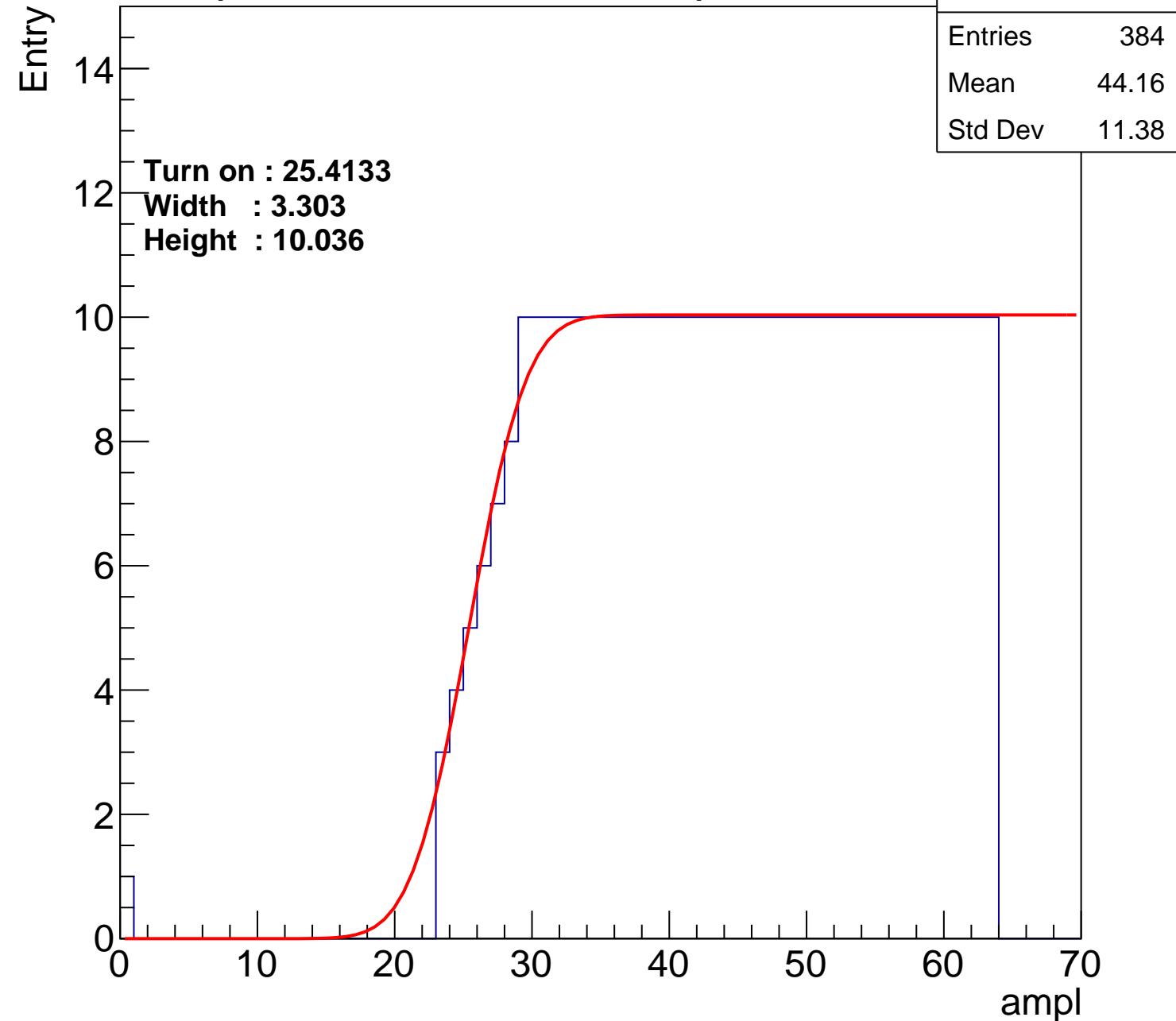
Width : 3.303

Height : 10.036

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch32

calib_packv5_042523_0143.root, FC#4, port A2

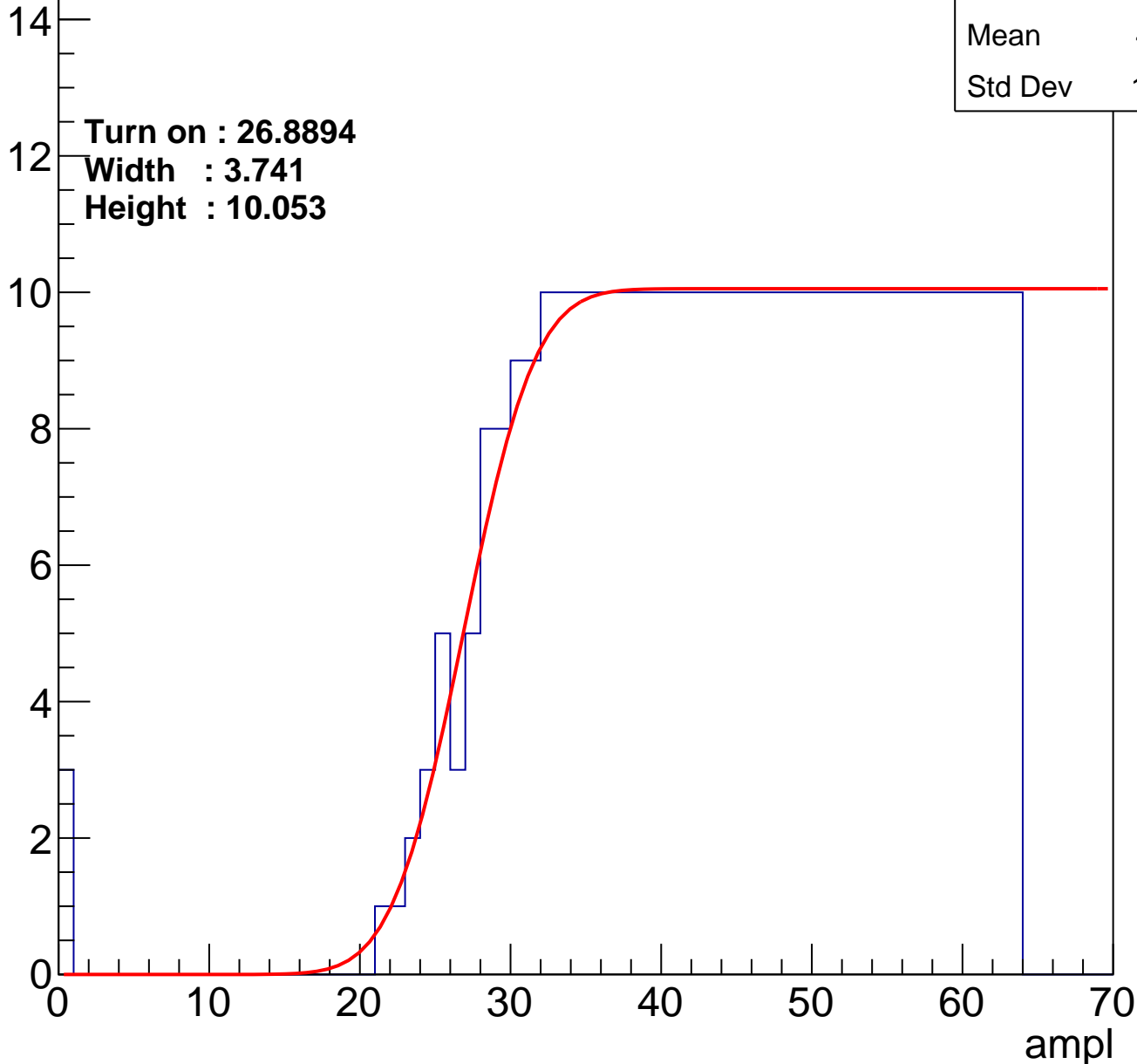
Entries	377
Mean	44.31
Std Dev	11.68

Turn on : 26.8894

Width : 3.741

Height : 10.053

Entry



B1L100S, U4-ch33

calib_packv5_042523_0143.root, FC#4, port A2

Entries	370
Mean	44.71
Std Dev	11.42

Turn on : 28.1137

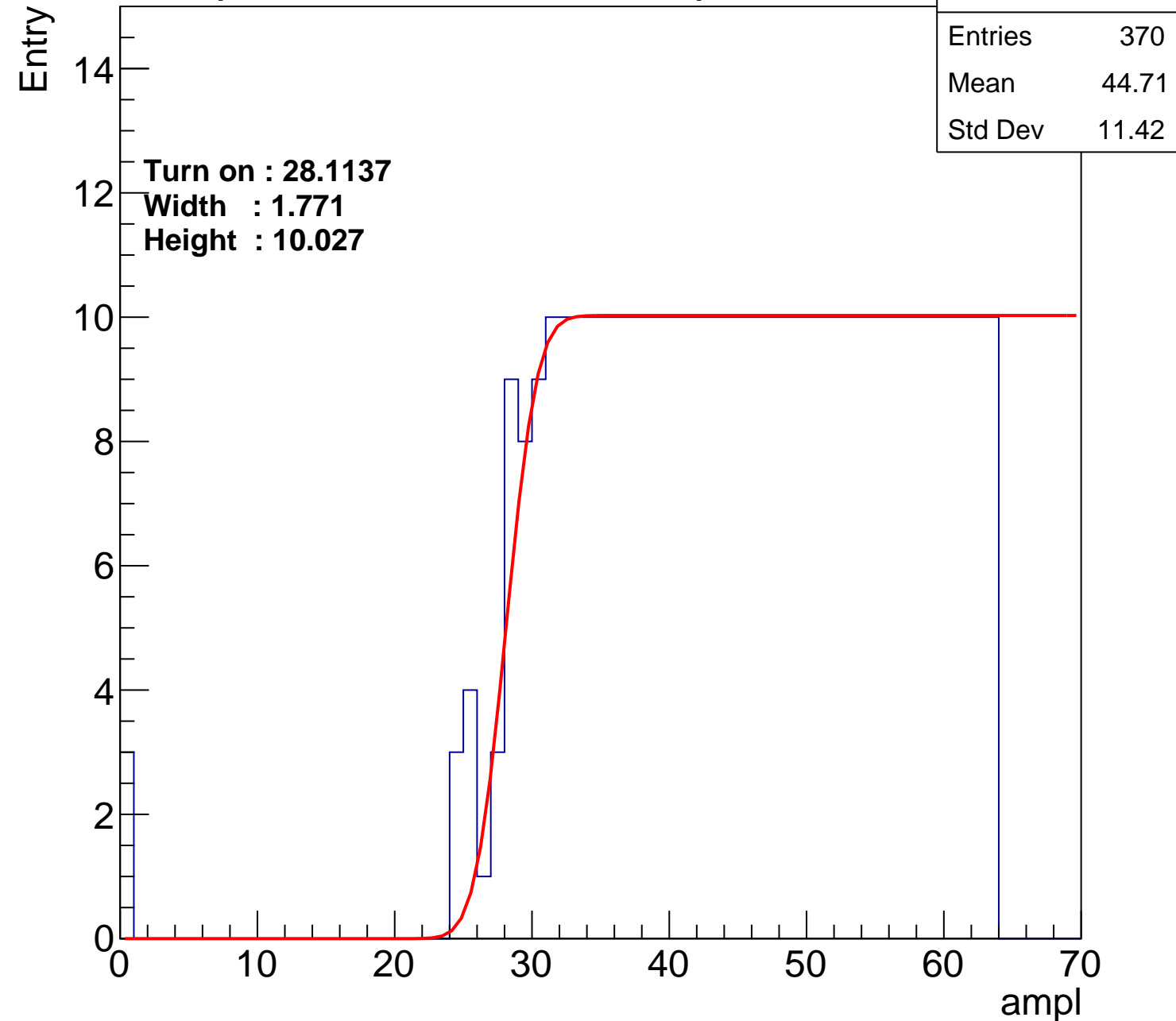
Width : 1.771

Height : 10.027

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch34

calib_packv5_042523_0143.root, FC#4, port A2

Entries	363
Mean	44.92
Std Dev	11.54

Turn on : 28.7173

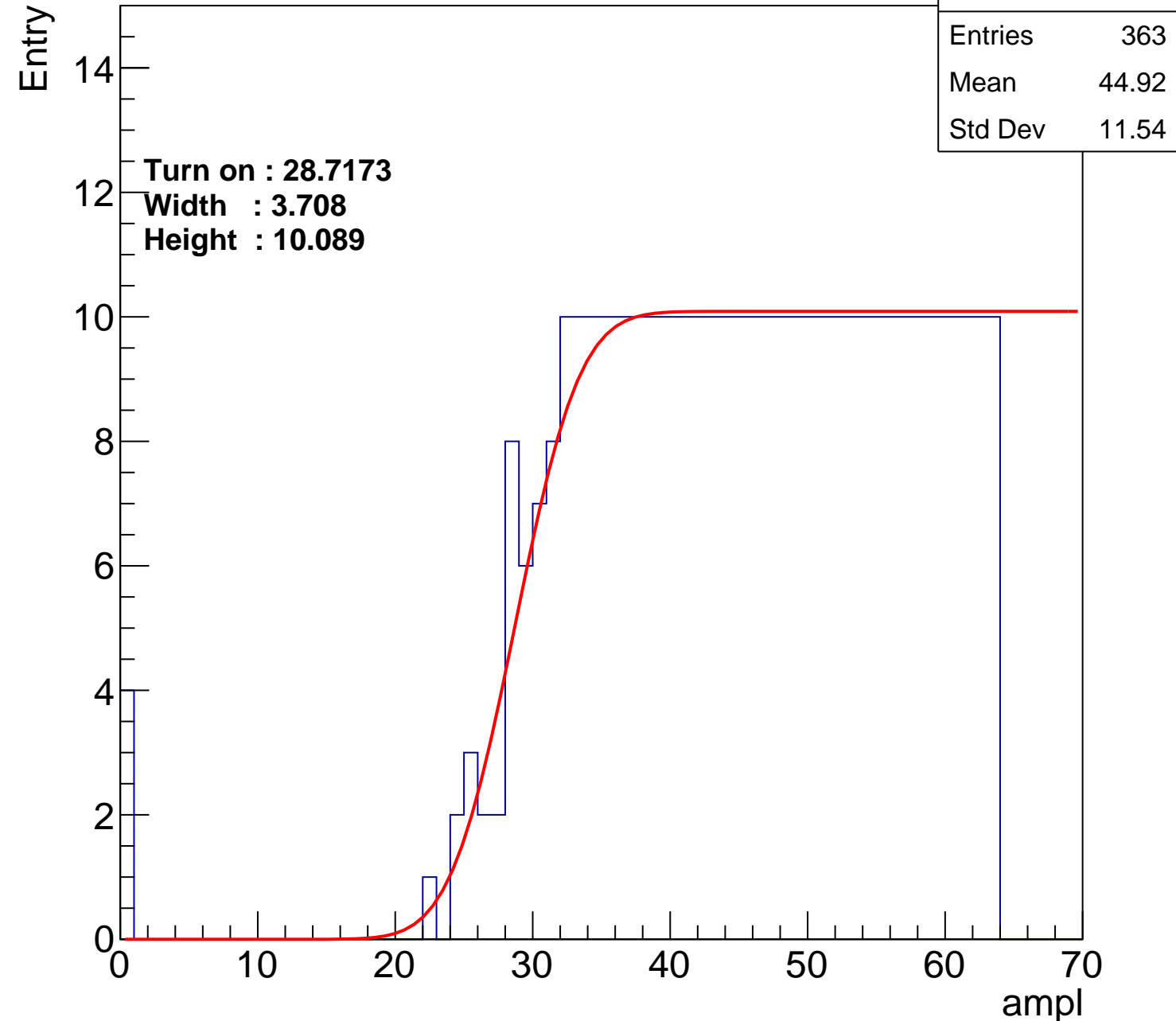
Width : 3.708

Height : 10.089

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch35

calib_packv5_042523_0143.root, FC#4, port A2

Entries	380
Mean	44.15
Std Dev	11.85

Turn on : 26.7041

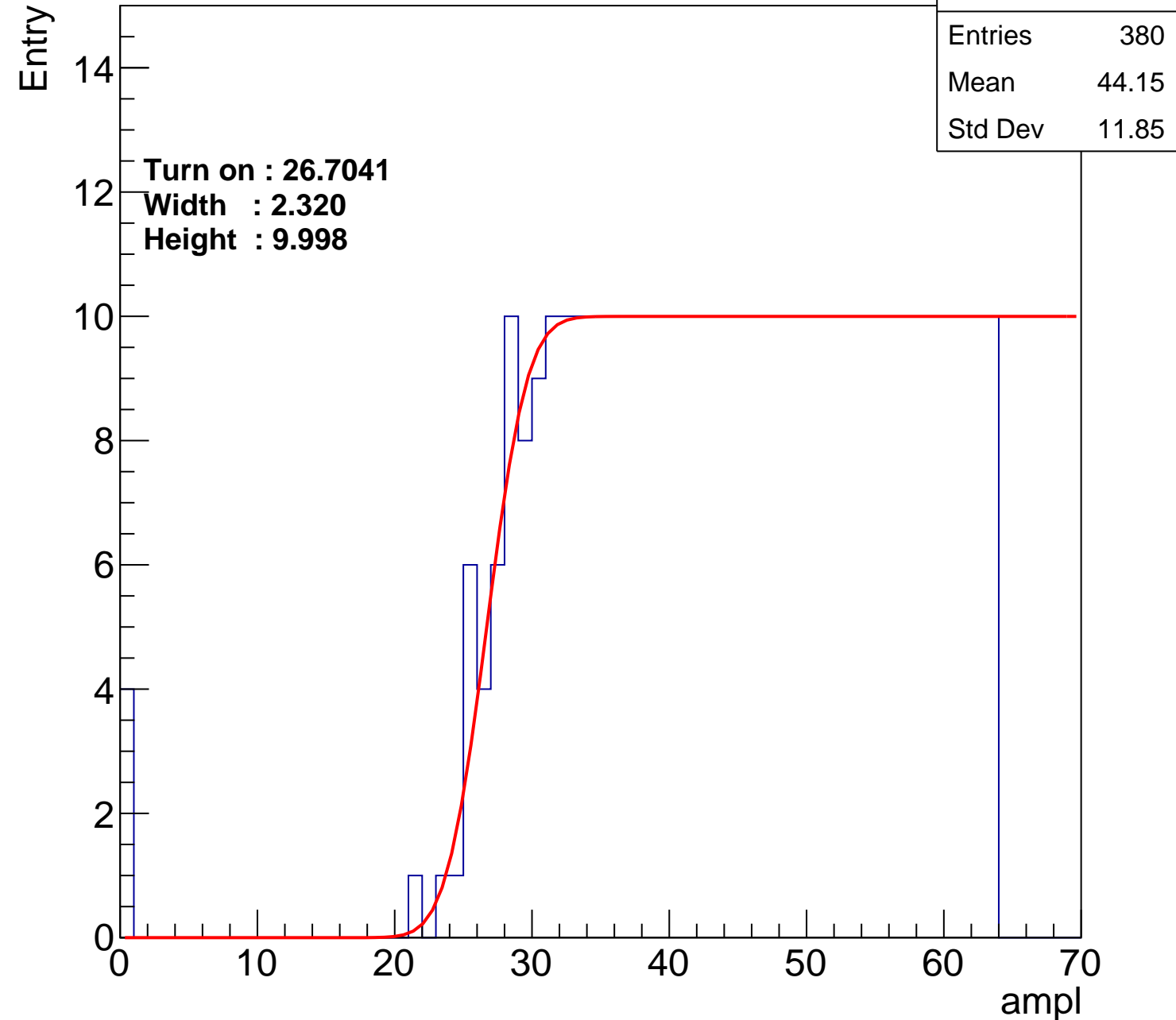
Width : 2.320

Height : 9.998

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch36

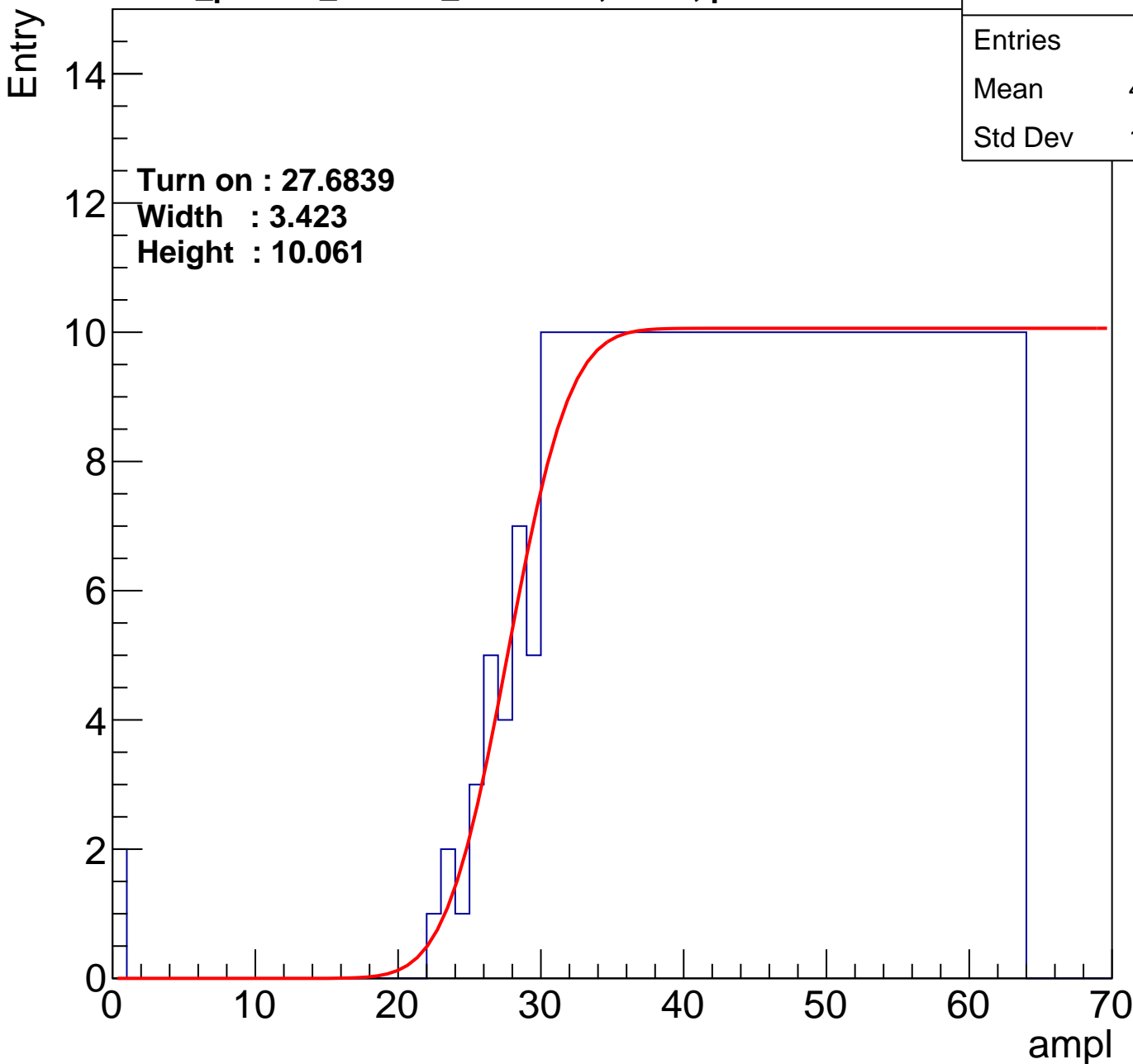
calib_packv5_042523_0143.root, FC#4, port A2

Entries	370
Mean	44.75
Std Dev	11.28

Turn on : 27.6839

Width : 3.423

Height : 10.061



B1L100S, U4-ch37

calib_packv5_042523_0143.root, FC#4, port A2

Entries	401
Mean	43.17
Std Dev	12.22

Turn on : 24.7871

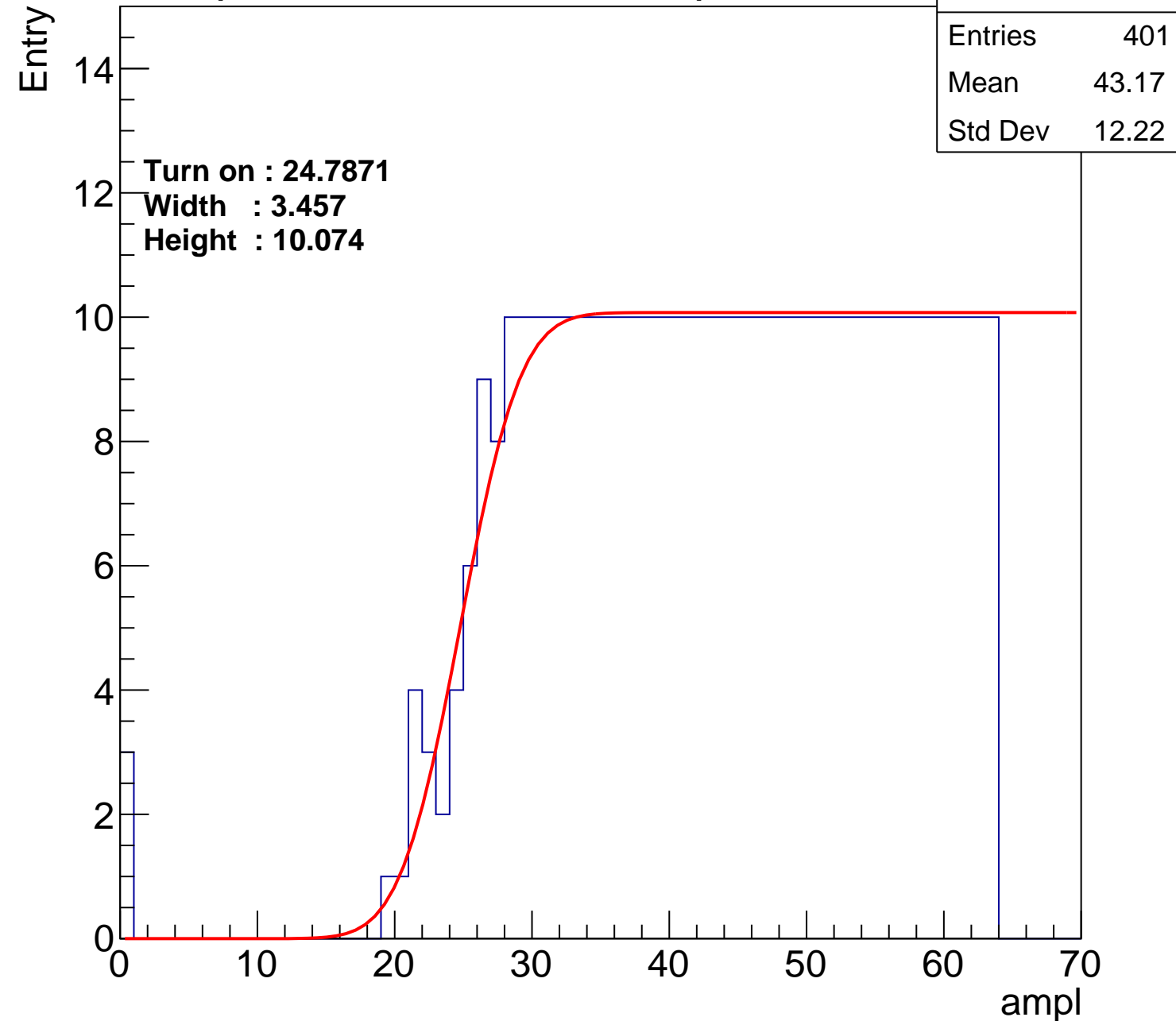
Width : 3.457

Height : 10.074

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch38

calib_packv5_042523_0143.root, FC#4, port A2

Entries	400
Mean	43.23
Std Dev	12.13

Turn on : 24.5665

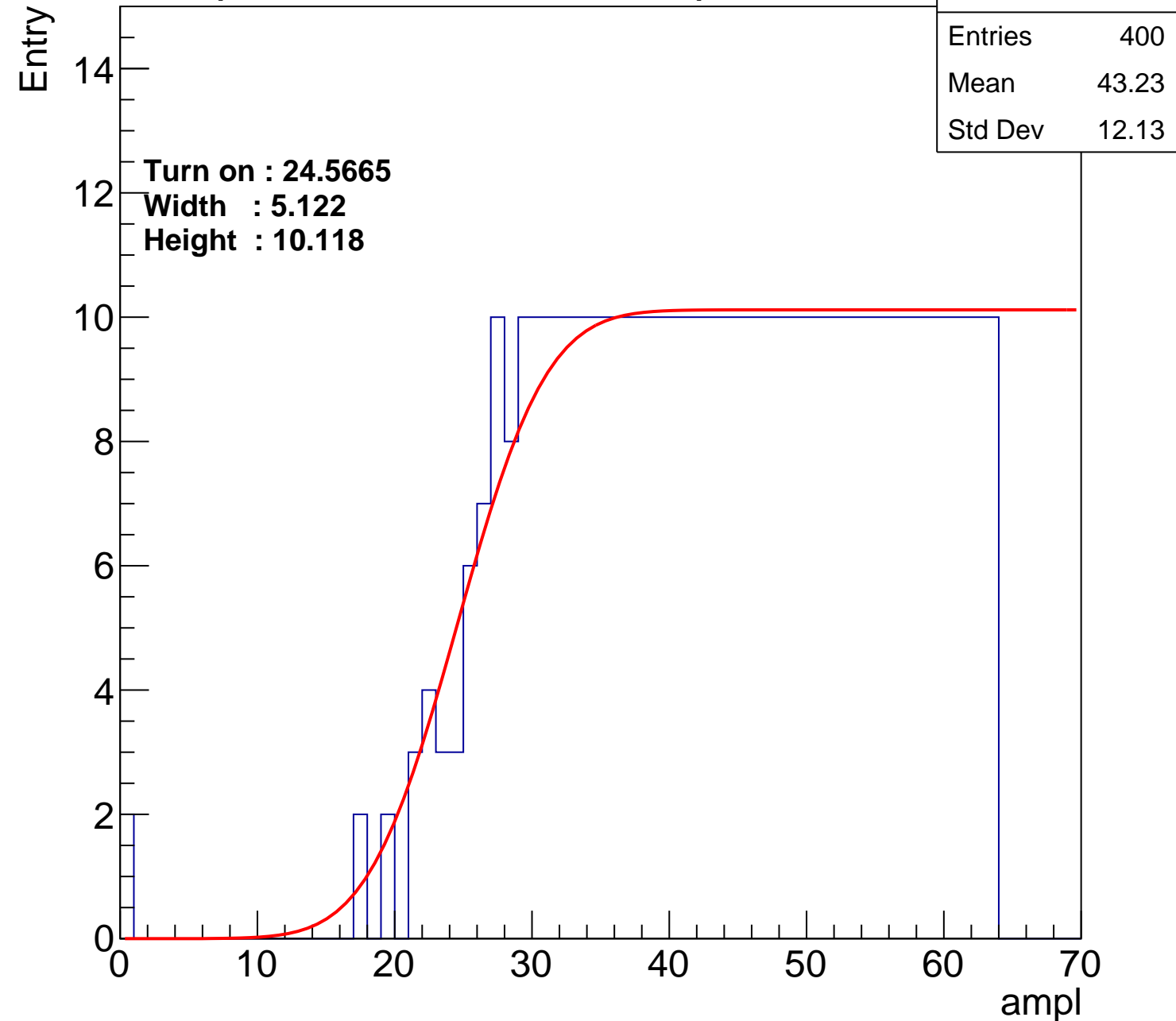
Width : 5.122

Height : 10.118

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch39

calib_packv5_042523_0143.root, FC#4, port A2

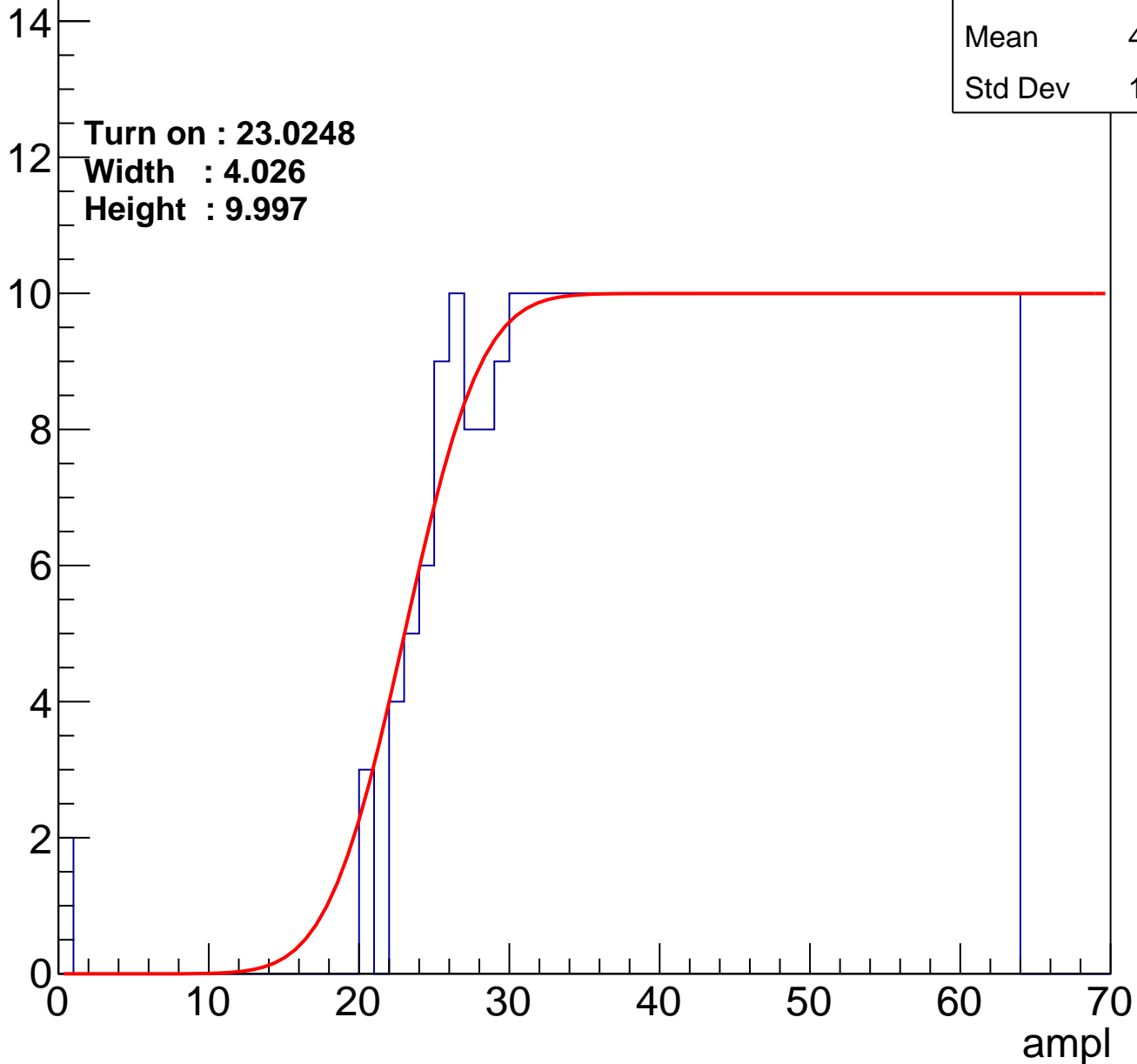
Entries	404
Mean	43.08
Std Dev	12.14

Turn on : 23.0248

Width : 4.026

Height : 9.997

Entry



B1L100S, U4-ch40

calib_packv5_042523_0143.root, FC#4, port A2

Entries	383
Mean	44.08
Std Dev	11.72

Turn on : 26.3075

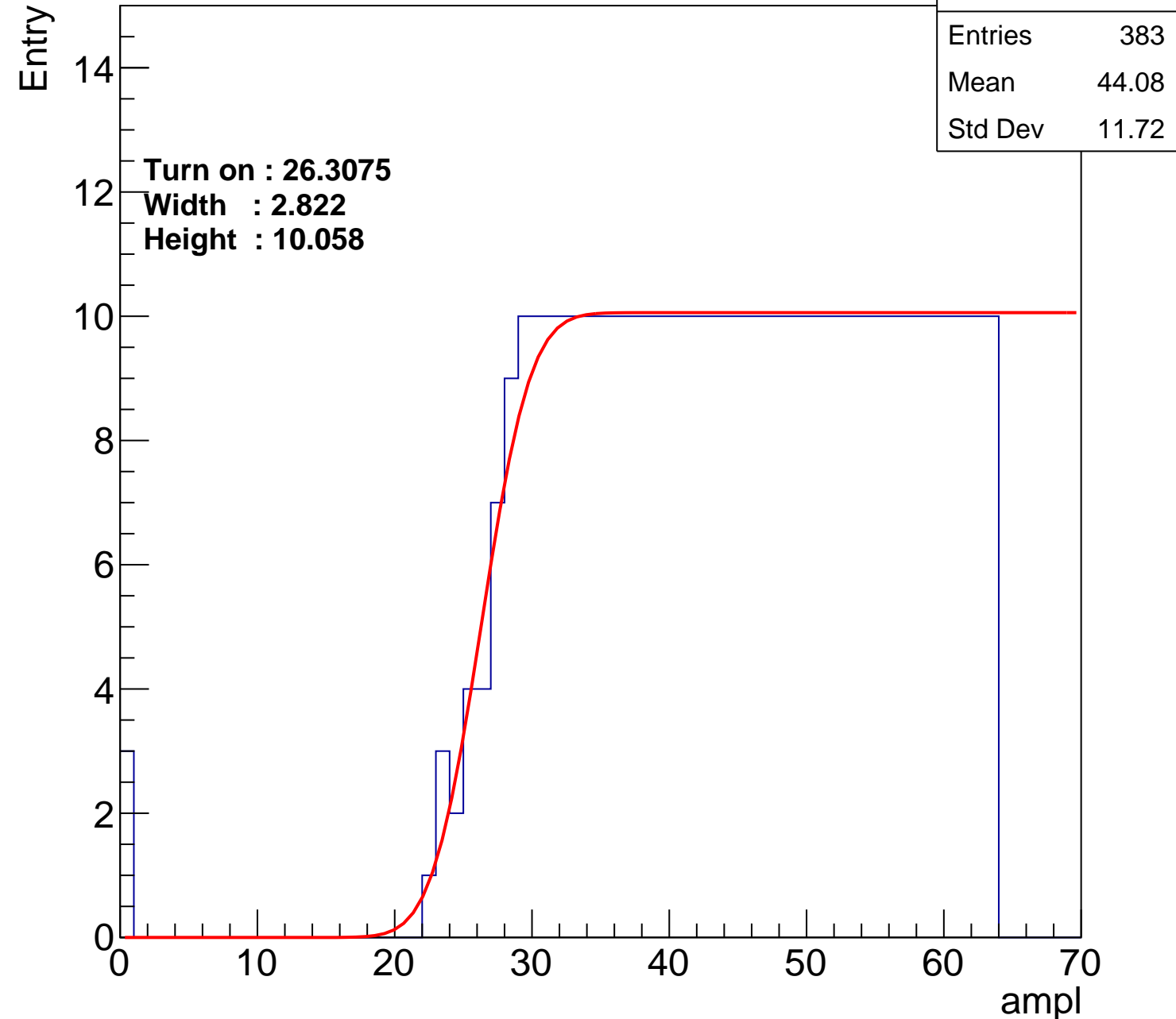
Width : 2.822

Height : 10.058

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch41

calib_packv5_042523_0143.root, FC#4, port A2

Entries	380
Mean	44.29
Std Dev	11.38

Turn on : 25.9353

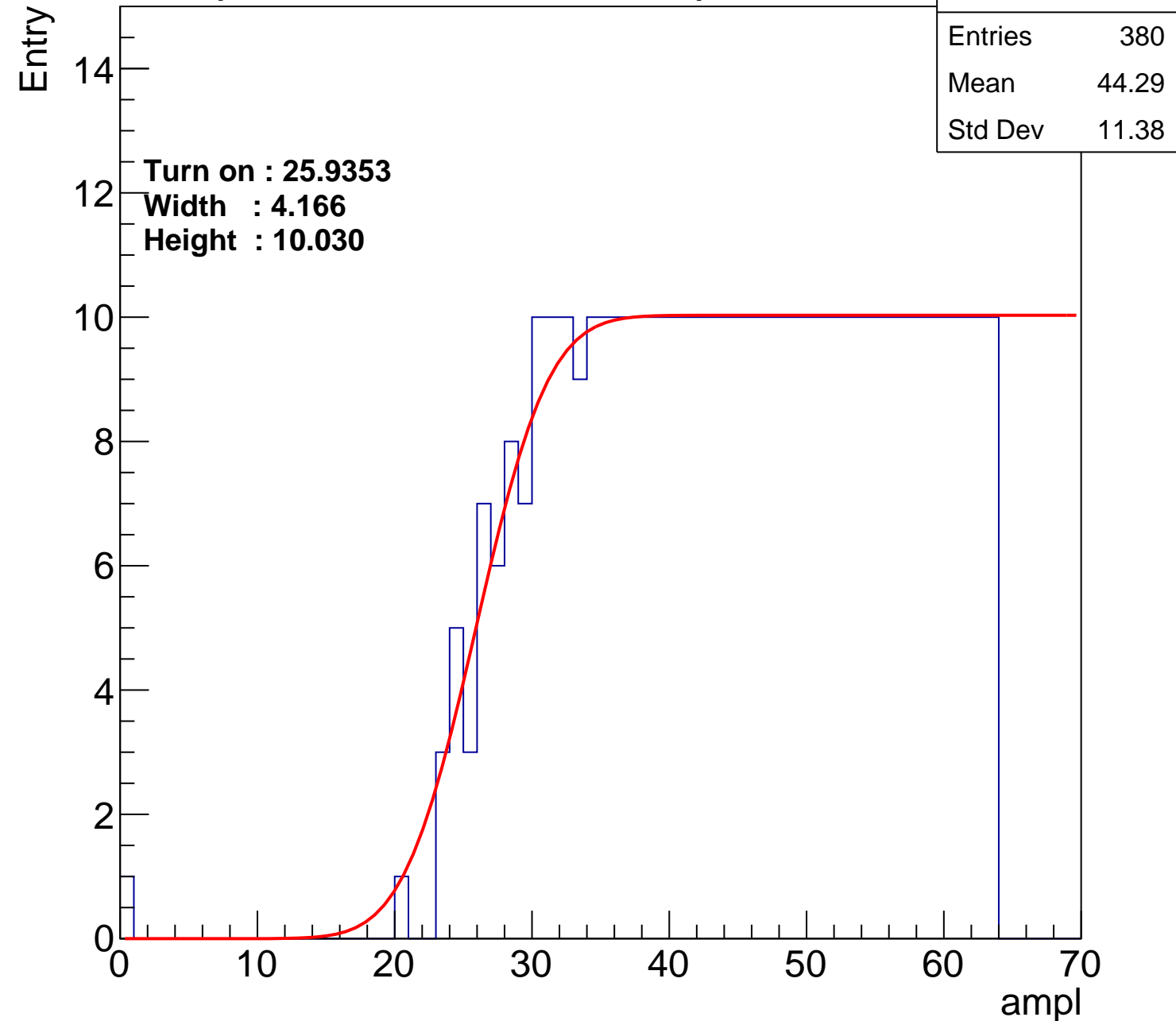
Width : 4.166

Height : 10.030

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch42

calib_packv5_042523_0143.root, FC#4, port A2

Entries	370
Mean	44.76
Std Dev	11.24

Turn on : 27.3432

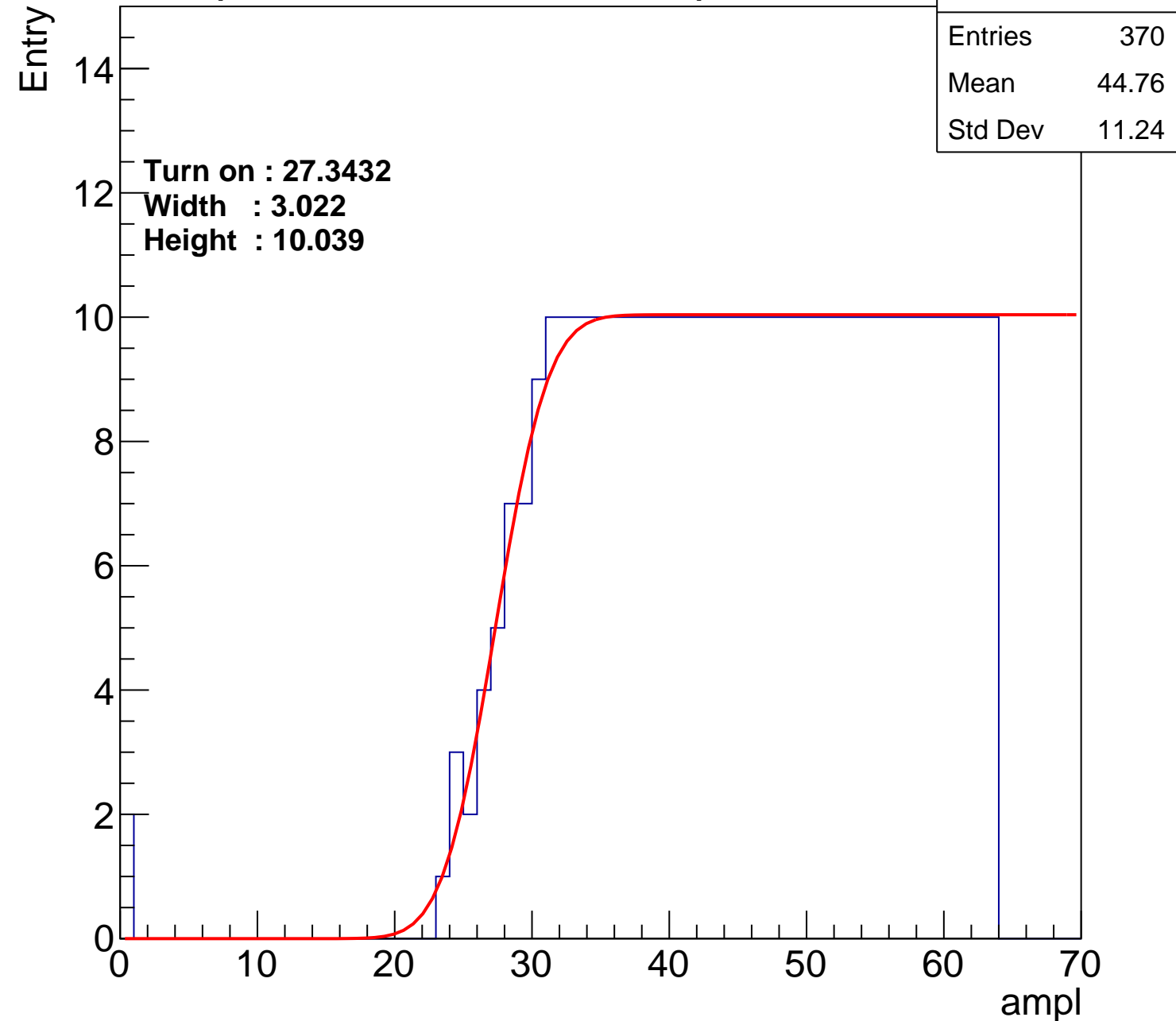
Width : 3.022

Height : 10.039

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch43

calib_packv5_042523_0143.root, FC#4, port A2

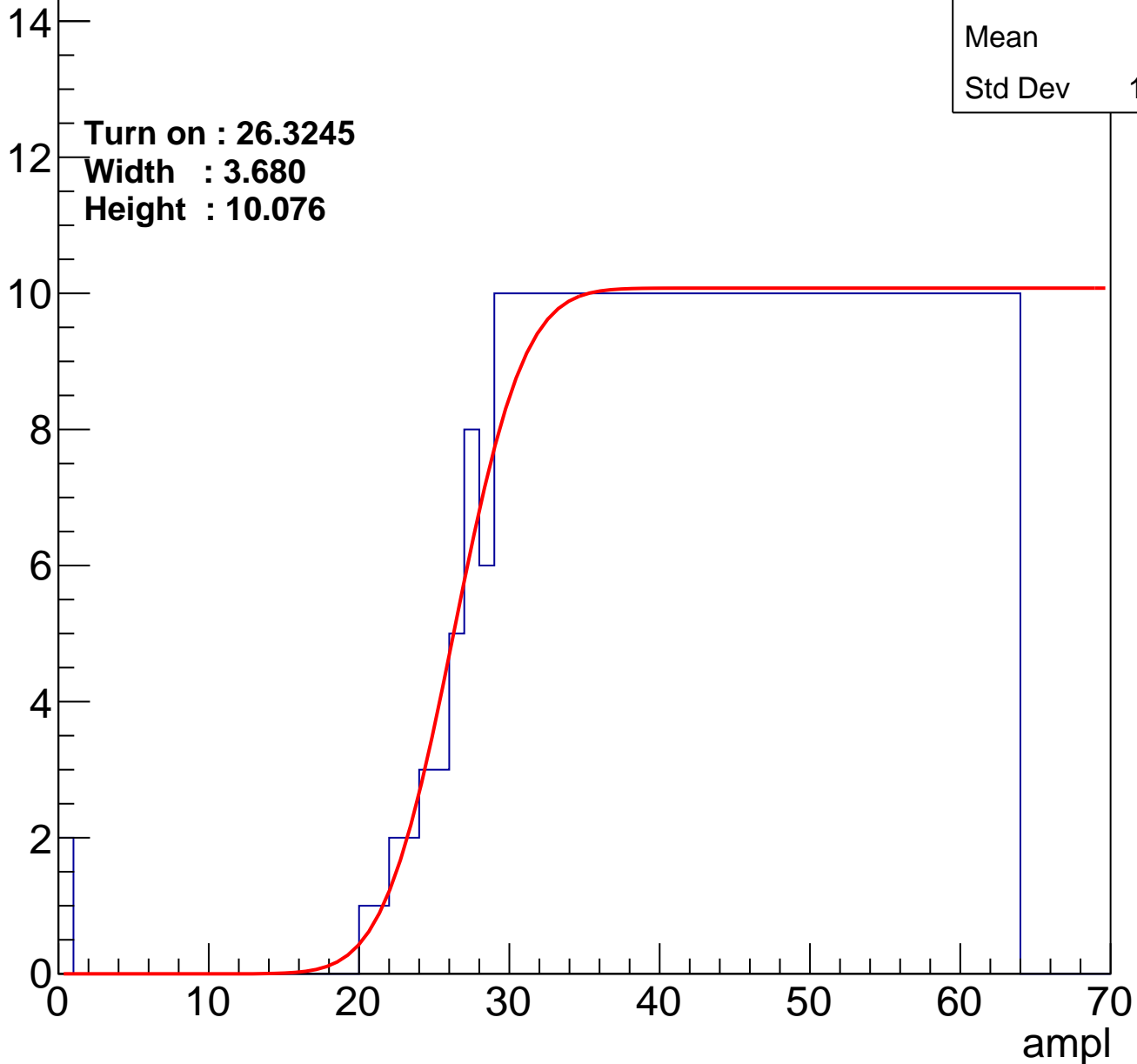
Entries	383
Mean	44.1
Std Dev	11.62

Turn on : 26.3245

Width : 3.680

Height : 10.076

Entry



B1L100S, U4-ch44

calib_packv5_042523_0143.root, FC#4, port A2

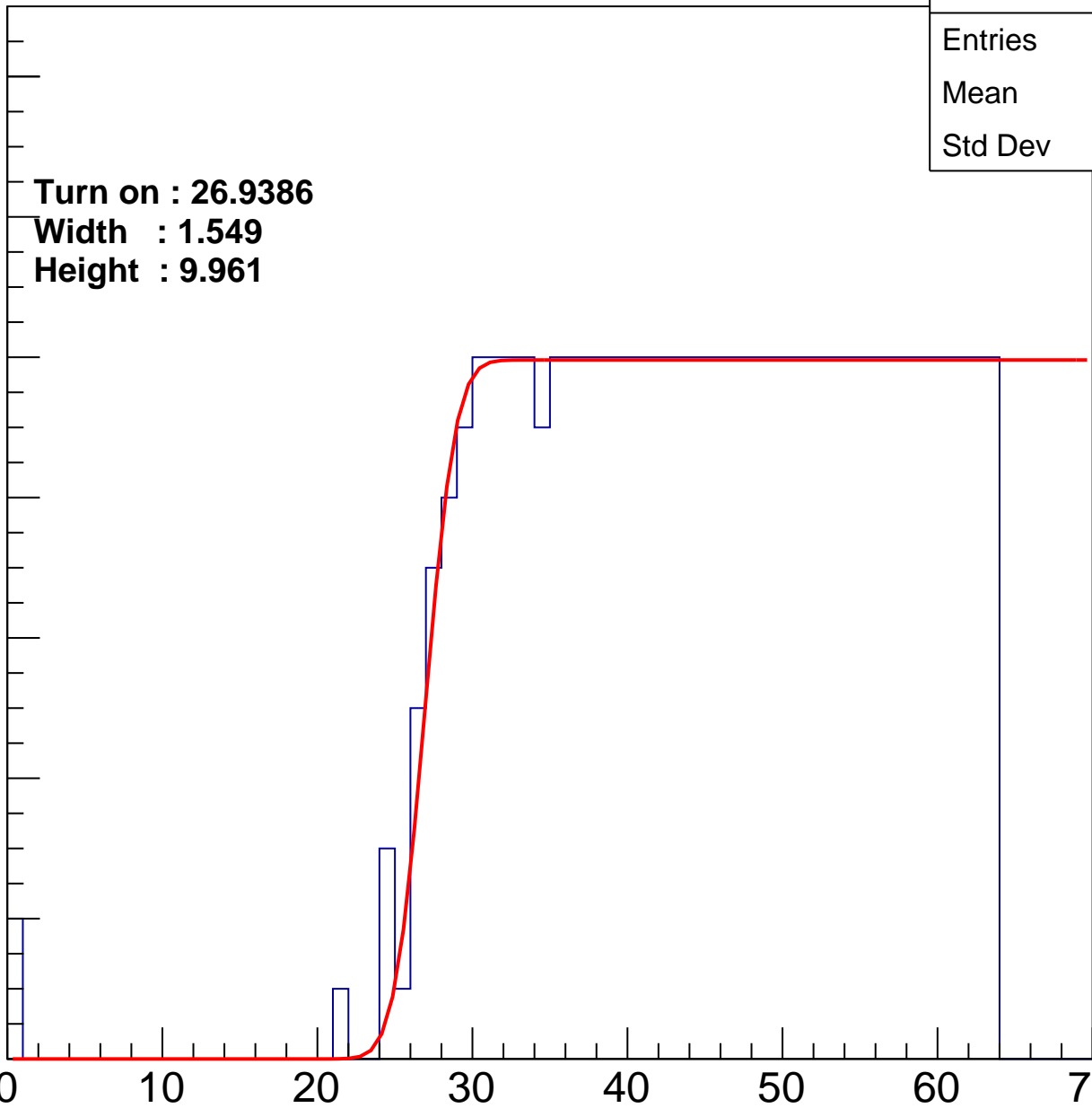
Entry

14
12
10
8
6
4
2
0

Turn on : 26.9386
Width : 1.549
Height : 9.961

Entries	375
Mean	44.53
Std Dev	11.35

ampl



B1L100S, U4-ch45

calib_packv5_042523_0143.root, FC#4, port A2

Entries	363
Mean	45.07
Std Dev	11.12

Turn on : 28.0663

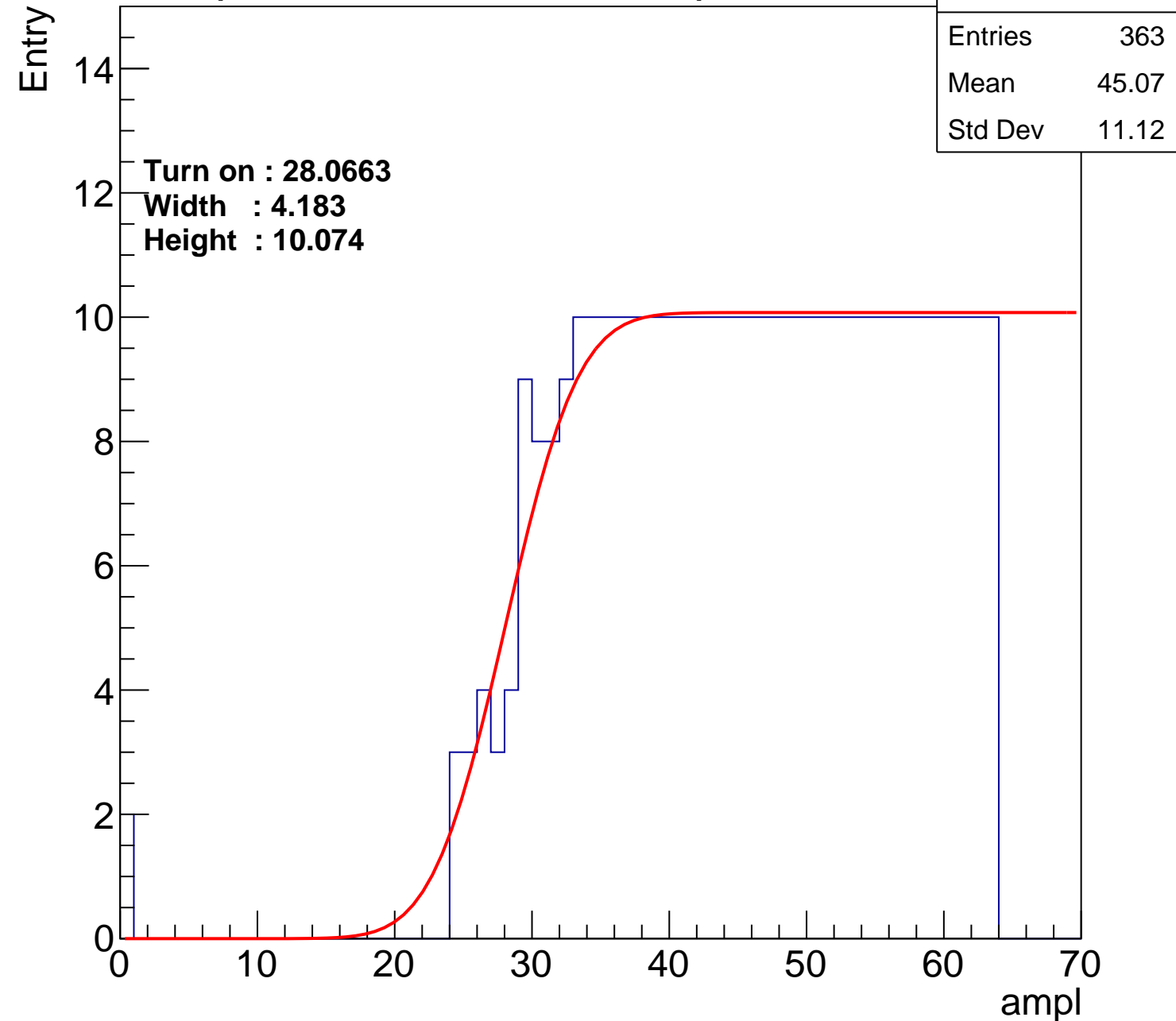
Width : 4.183

Height : 10.074

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch46

calib_packv5_042523_0143.root, FC#4, port A2

Entries	353
Mean	45.53
Std Dev	11.03

Turn on : 29.1267

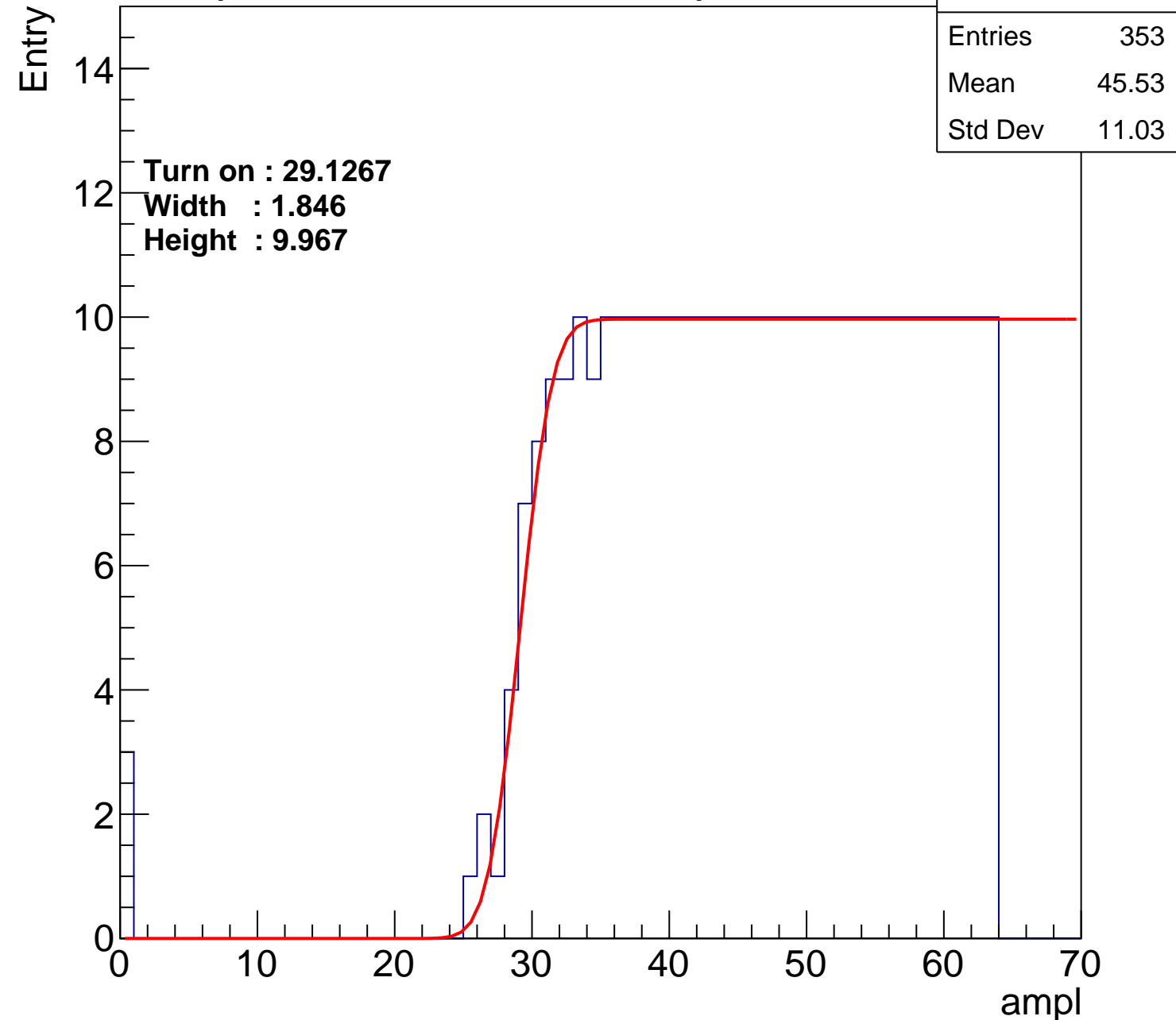
Width : 1.846

Height : 9.967

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch47

calib_packv5_042523_0143.root, FC#4, port A2

Entries	371
Mean	44.57
Std Dev	11.66

Turn on : 27.4241

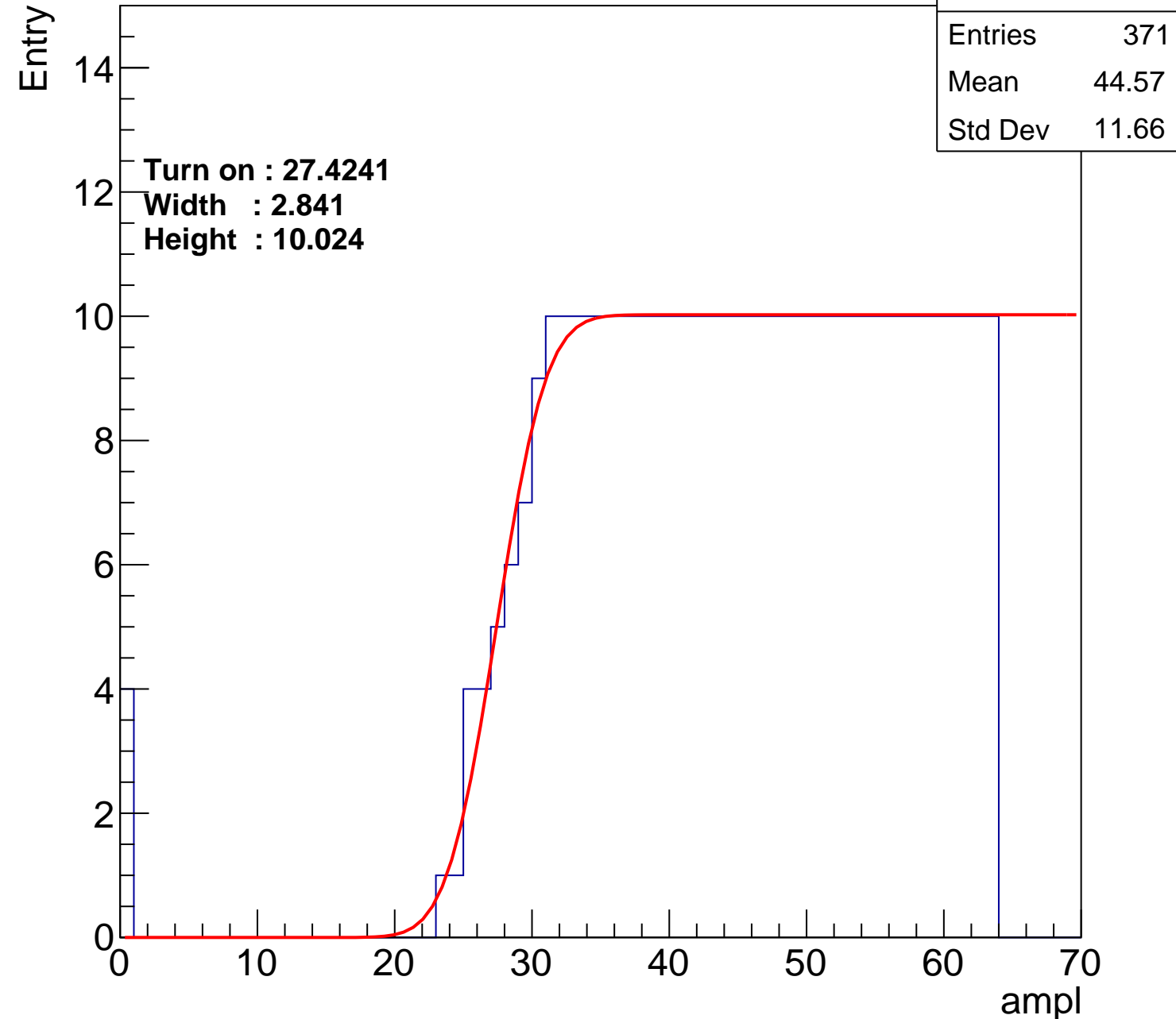
Width : 2.841

Height : 10.024

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch48

calib_packv5_042523_0143.root, FC#4, port A2

Entries	375
Mean	44.32
Std Dev	11.92

Turn on : 27.0065

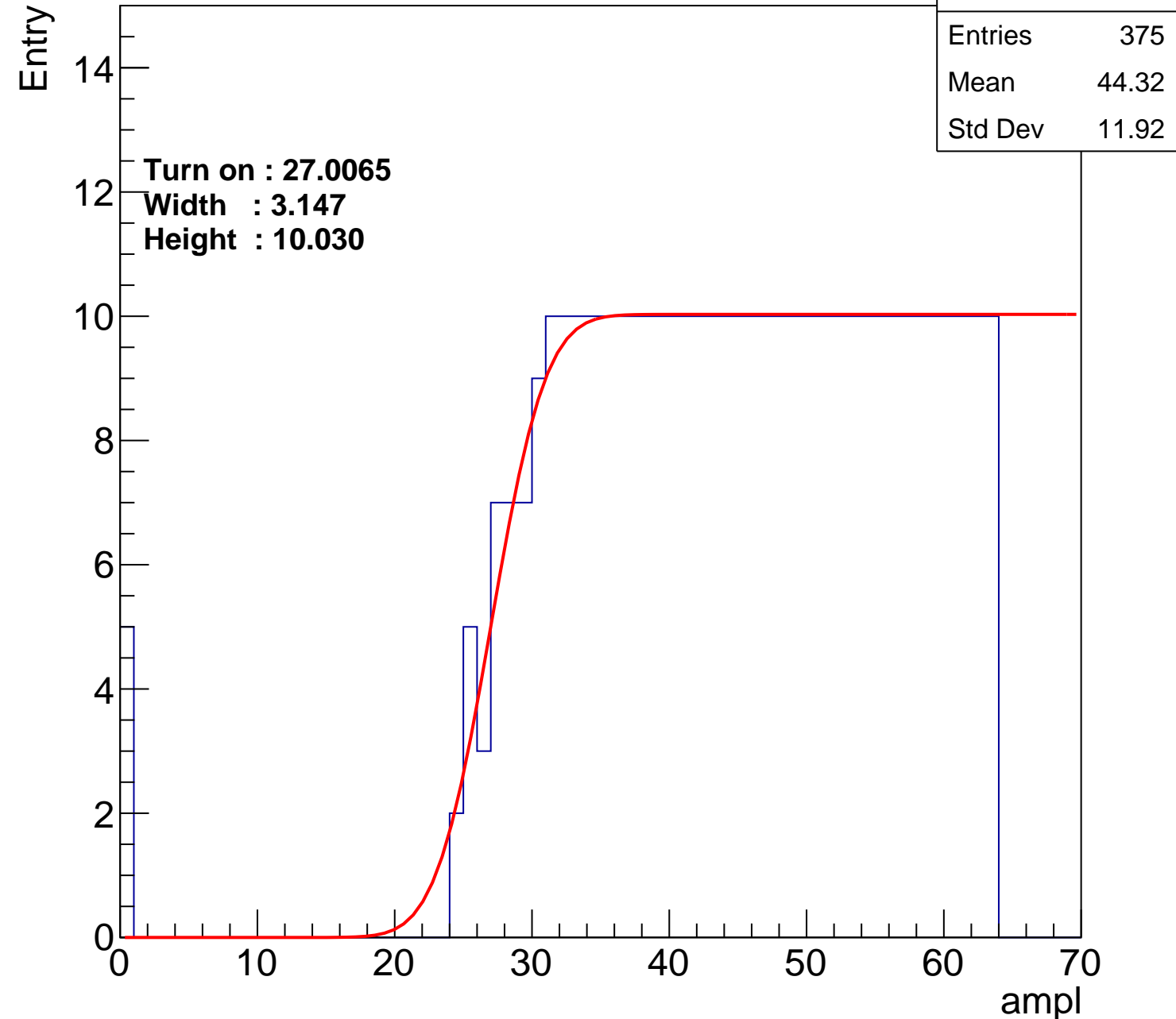
Width : 3.147

Height : 10.030

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch49

calib_packv5_042523_0143.root, FC#4, port A2

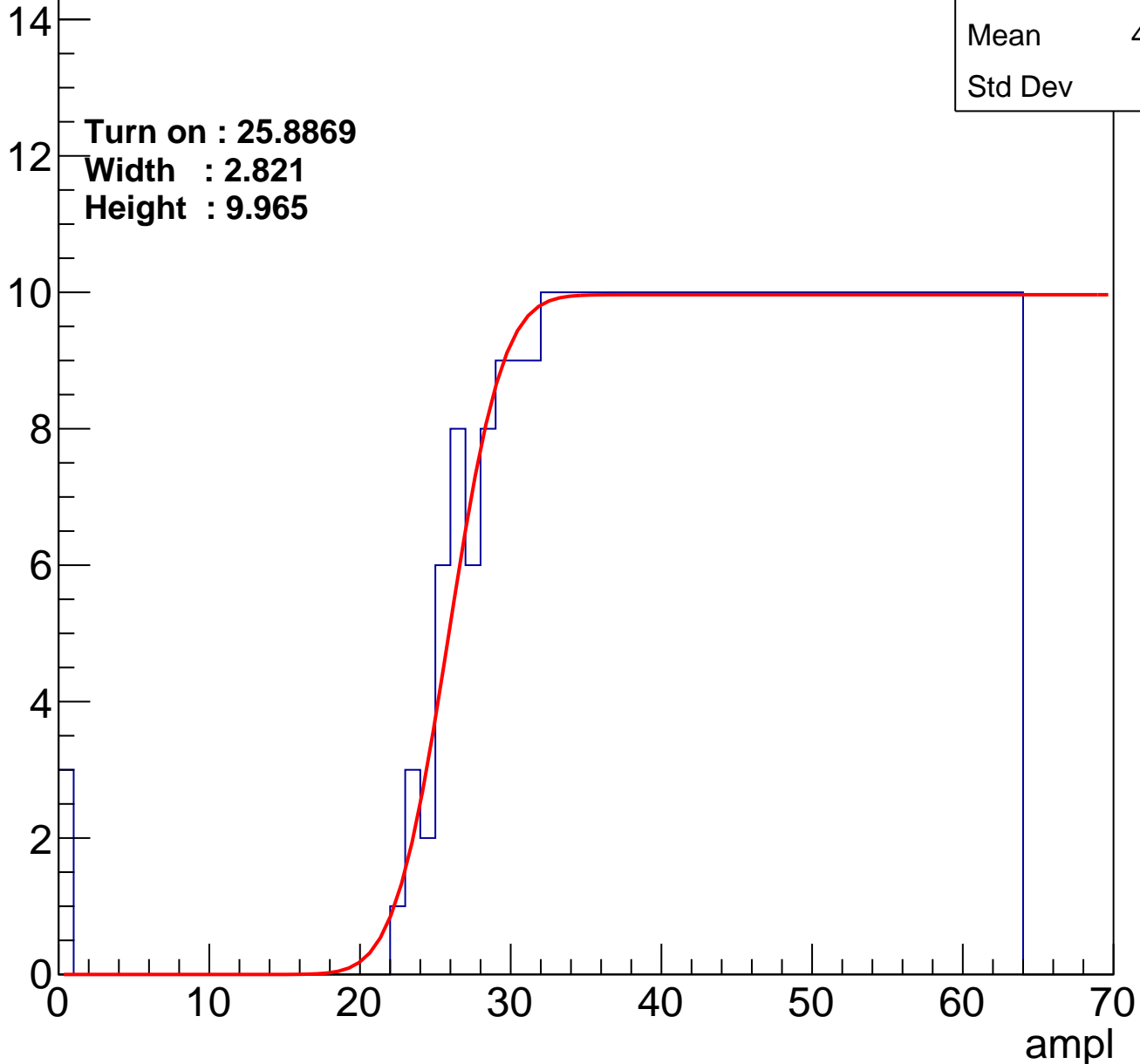
Entries	384
Mean	43.99
Std Dev	11.8

Turn on : 25.8869

Width : 2.821

Height : 9.965

Entry



B1L100S, U4-ch50

calib_packv5_042523_0143.root, FC#4, port A2

Entries	404
Mean	42.89
Std Dev	12.6

Turn on : 23.9664

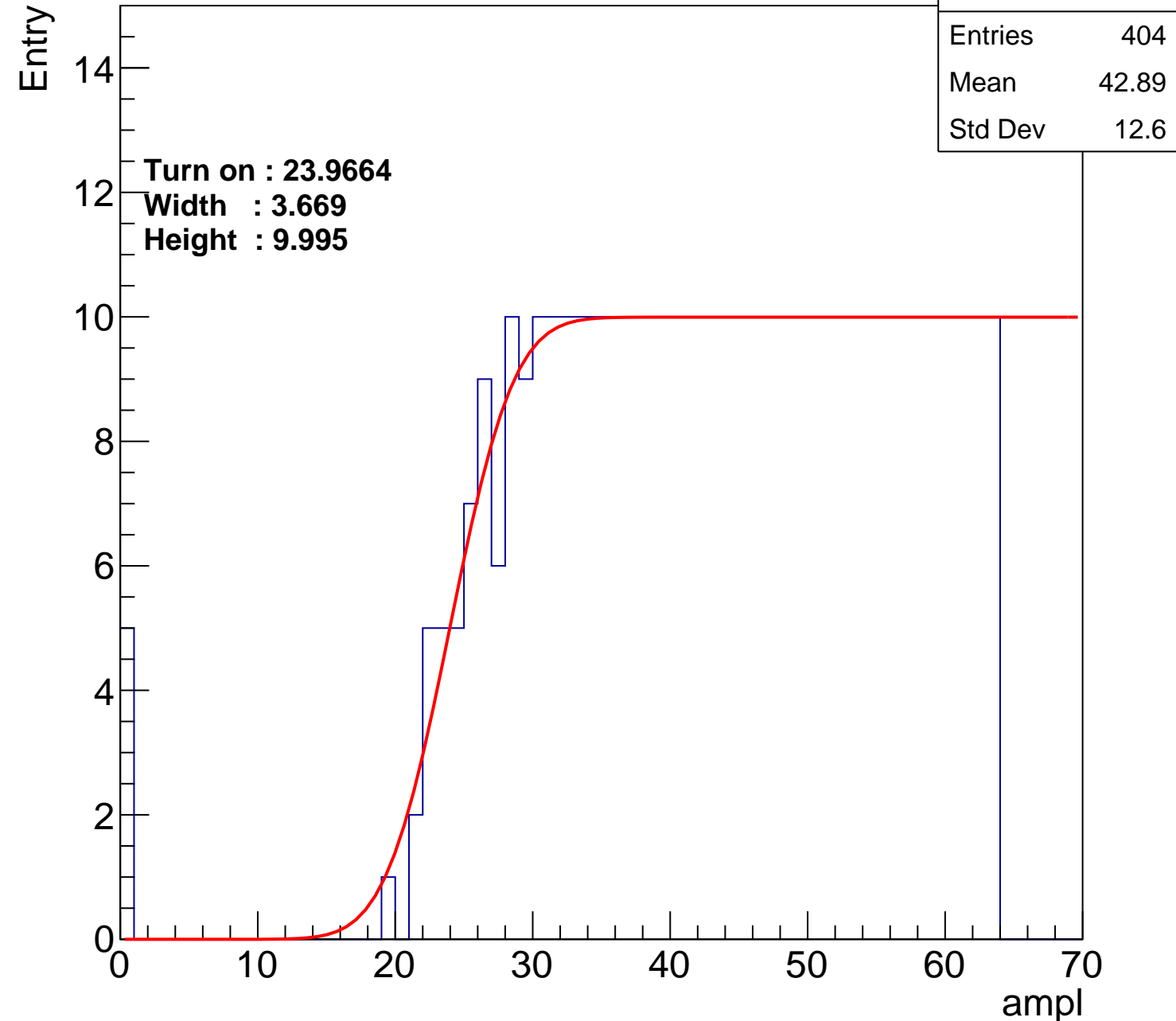
Width : 3.669

Height : 9.995

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch51

calib_packv5_042523_0143.root, FC#4, port A2

Entries	397
Mean	43.34
Std Dev	12.15

Turn on : 24.4756

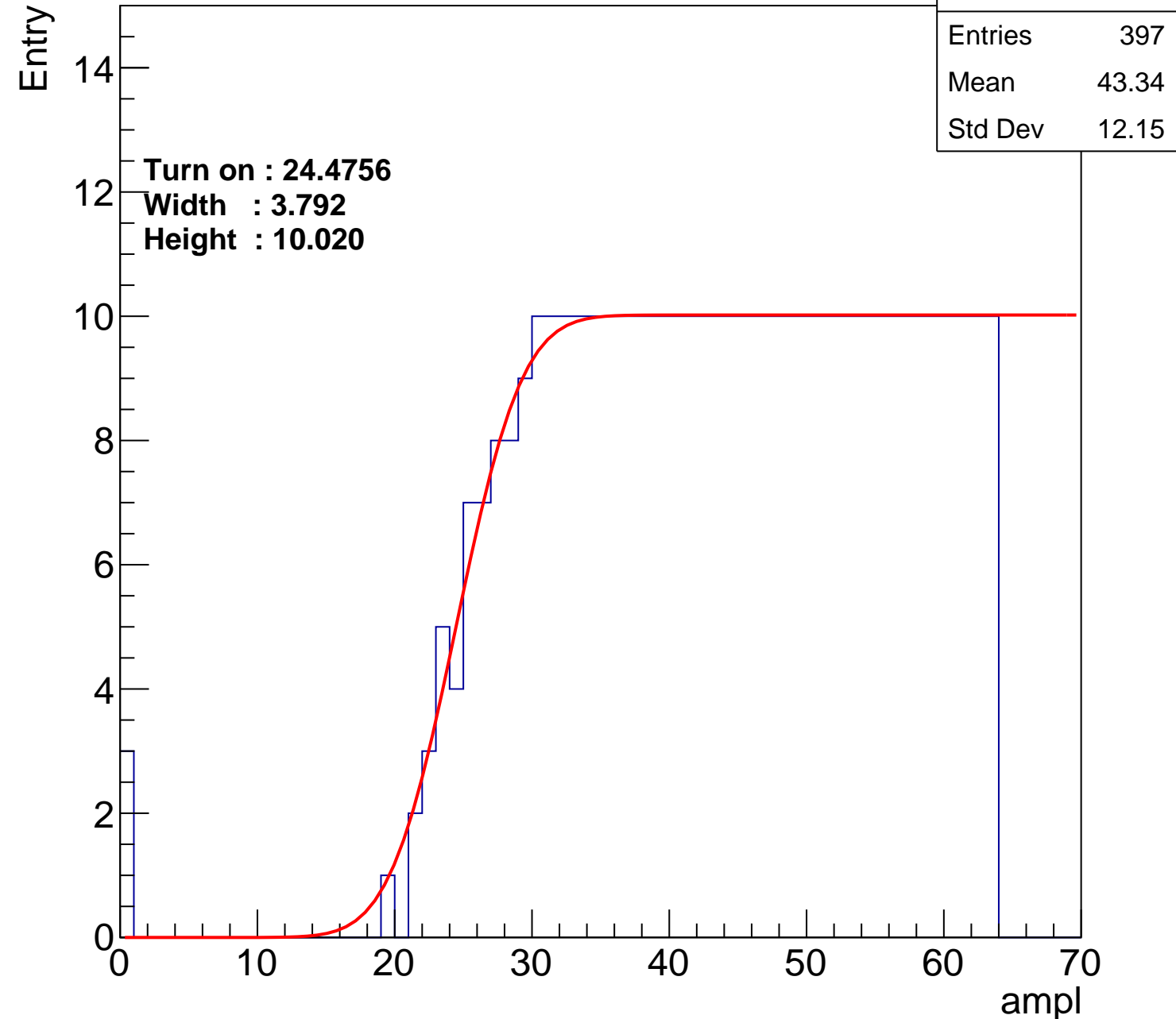
Width : 3.792

Height : 10.020

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch52

calib_packv5_042523_0143.root, FC#4, port A2

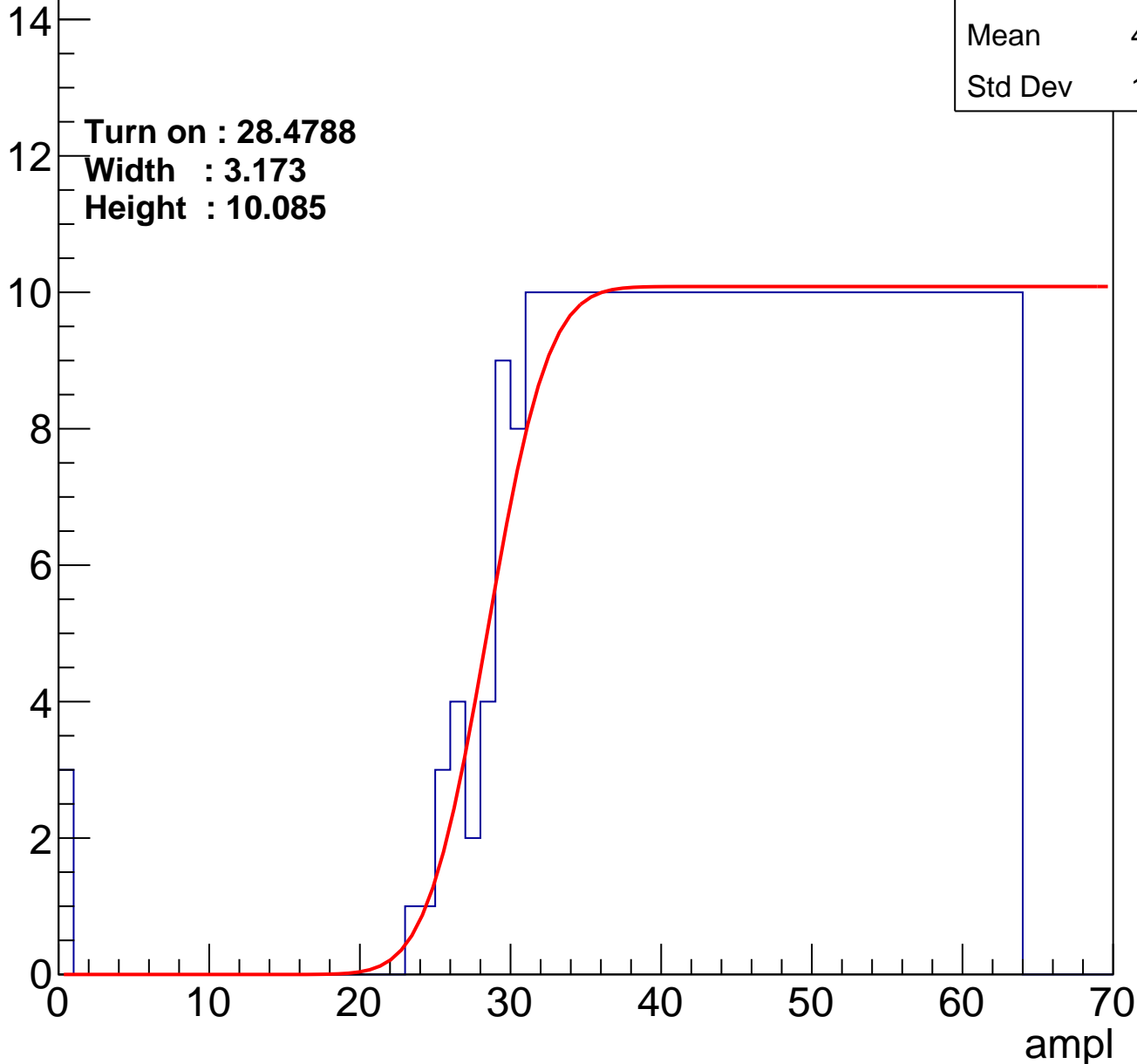
Entries	365
Mean	44.94
Std Dev	11.32

Turn on : 28.4788

Width : 3.173

Height : 10.085

Entry



B1L100S, U4-ch53

calib_packv5_042523_0143.root, FC#4, port A2

Entries	387
Mean	43.93
Std Dev	11.68

Turn on : 26.1581

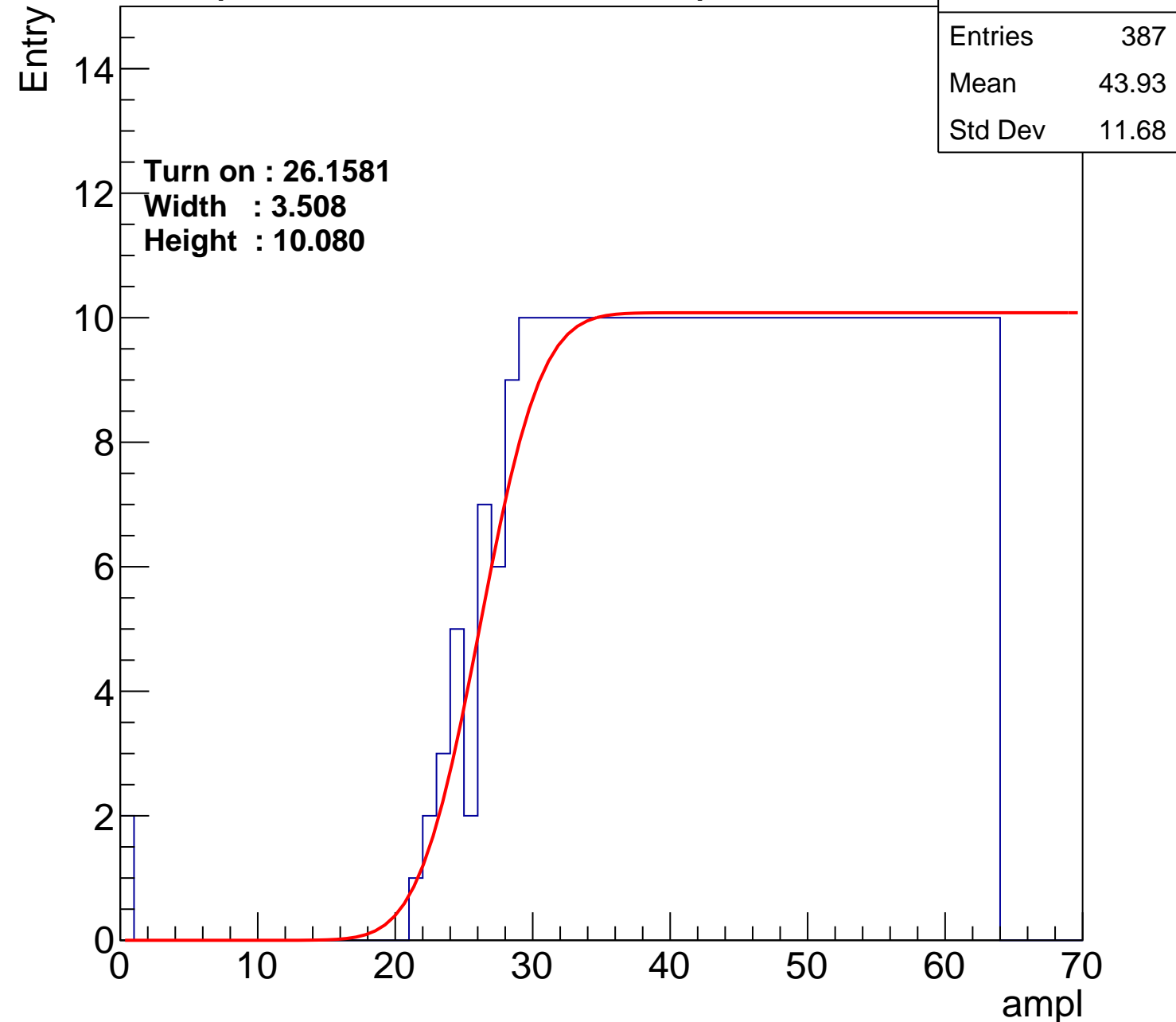
Width : 3.508

Height : 10.080

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch54

calib_packv5_042523_0143.root, FC#4, port A2

Entries	387
Mean	43.94
Std Dev	11.66

Turn on : 25.7016

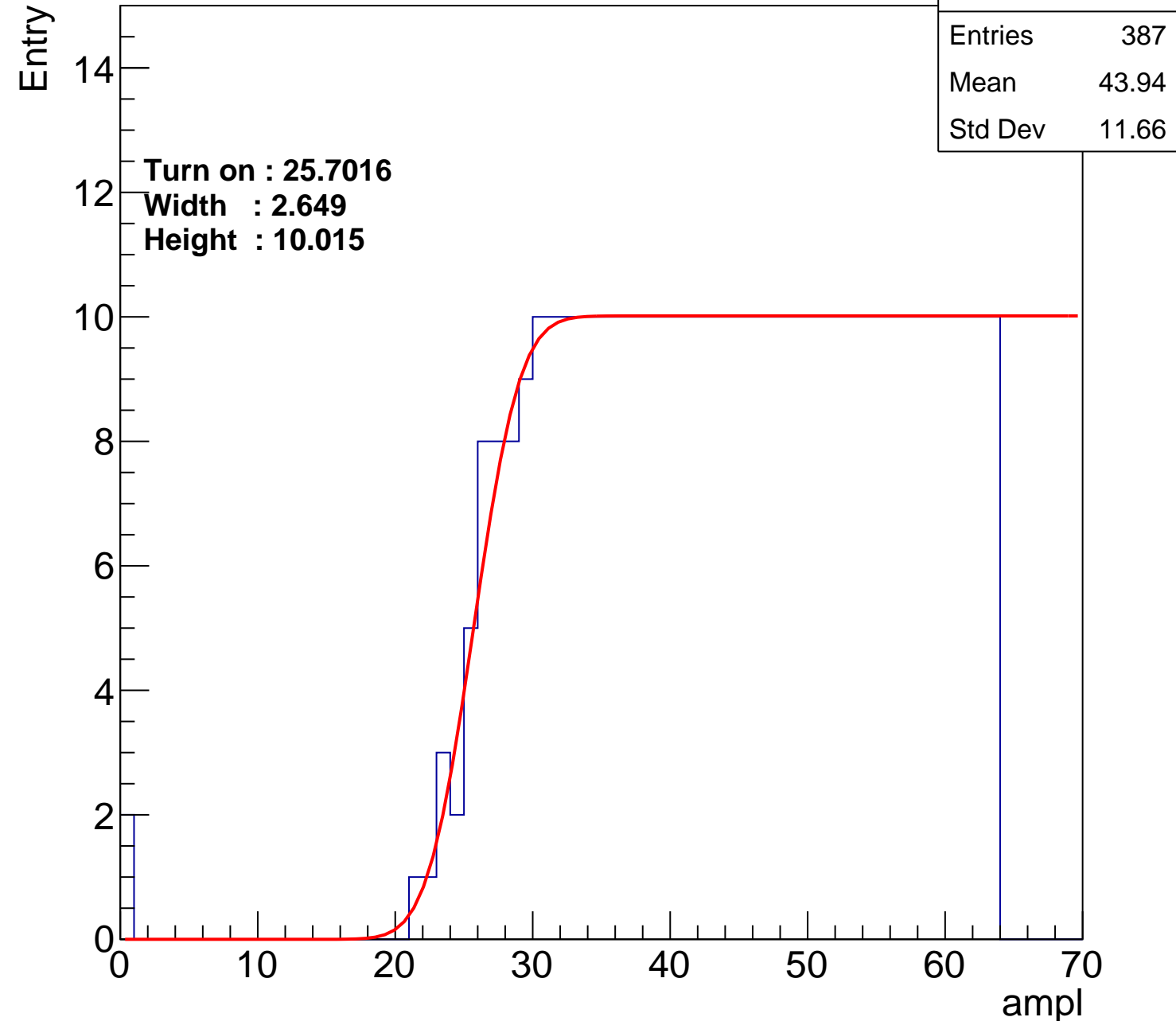
Width : 2.649

Height : 10.015

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch55

calib_packv5_042523_0143.root, FC#4, port A2

Entries	382
Mean	44.14
Std Dev	11.62

Turn on : 26.5914

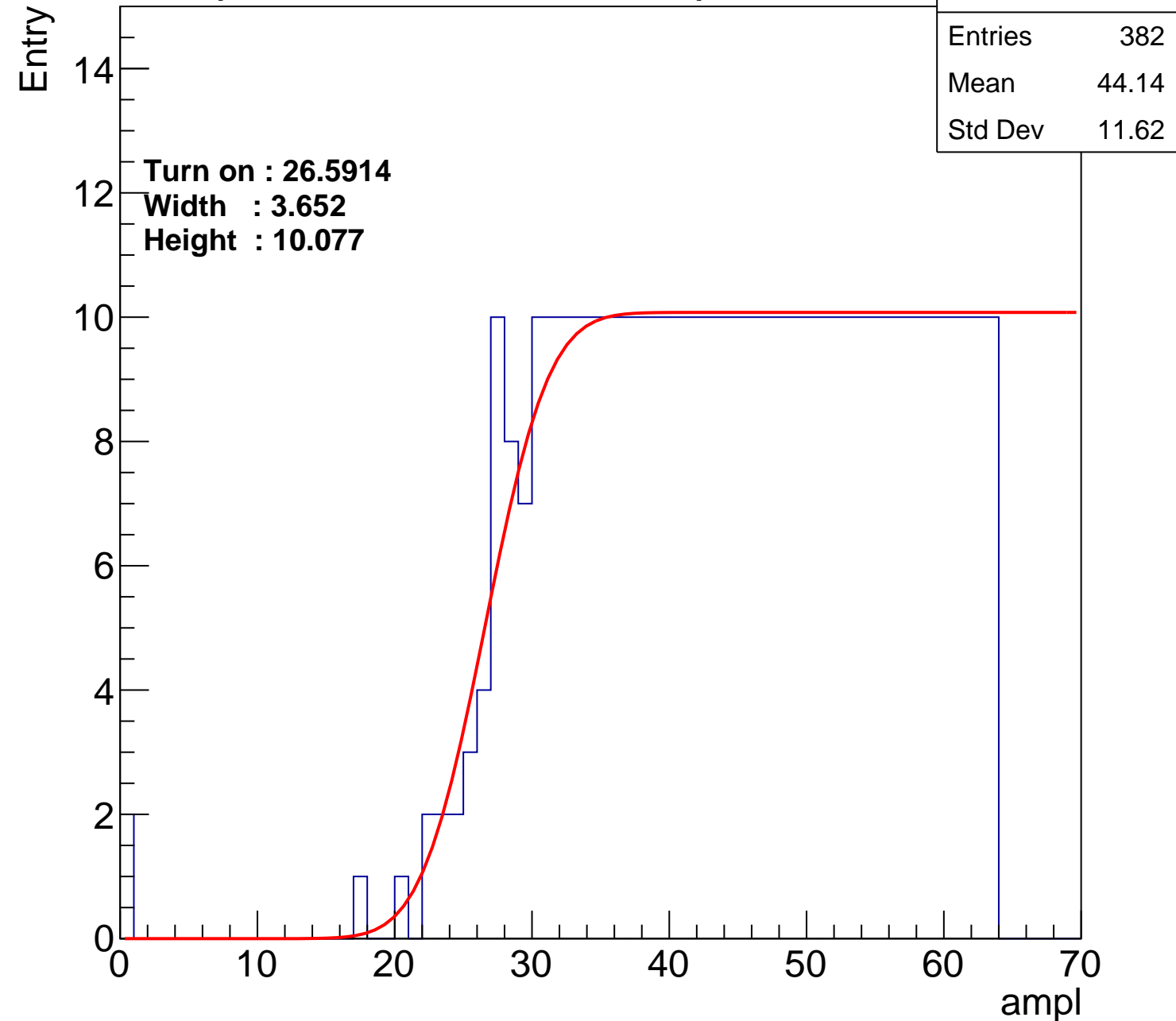
Width : 3.652

Height : 10.077

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch56

calib_packv5_042523_0143.root, FC#4, port A2

Entries	387
Mean	43.95
Std Dev	11.65

Turn on : 26.1999

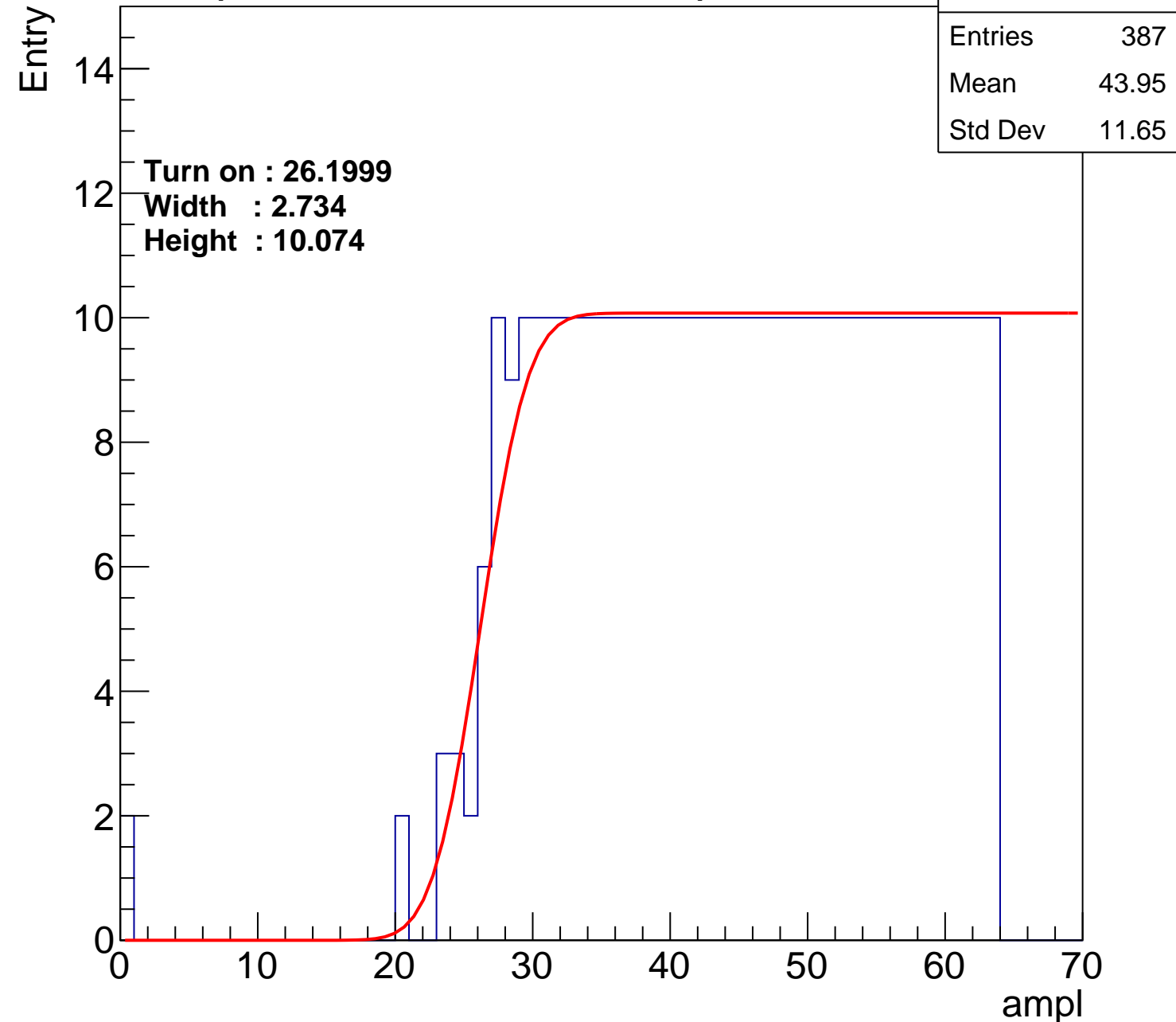
Width : 2.734

Height : 10.074

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch57

calib_packv5_042523_0143.root, FC#4, port A2

Entries	377
Mean	44.37
Std Dev	11.57

Turn on : 26.8290

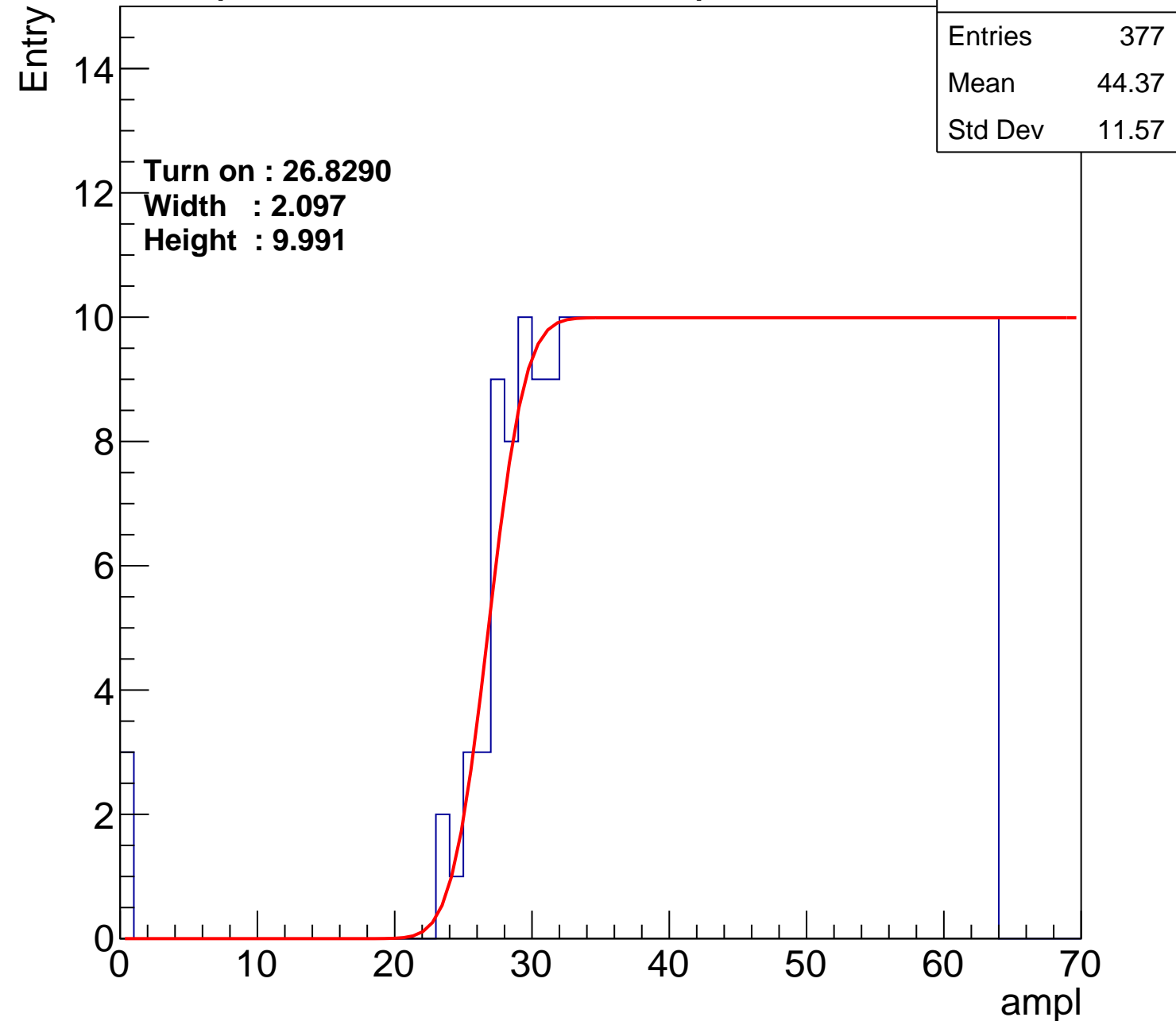
Width : 2.097

Height : 9.991

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch58

calib_packv5_042523_0143.root, FC#4, port A2

Entries	395
Mean	43.44
Std Dev	12.04

Turn on : 24.6268

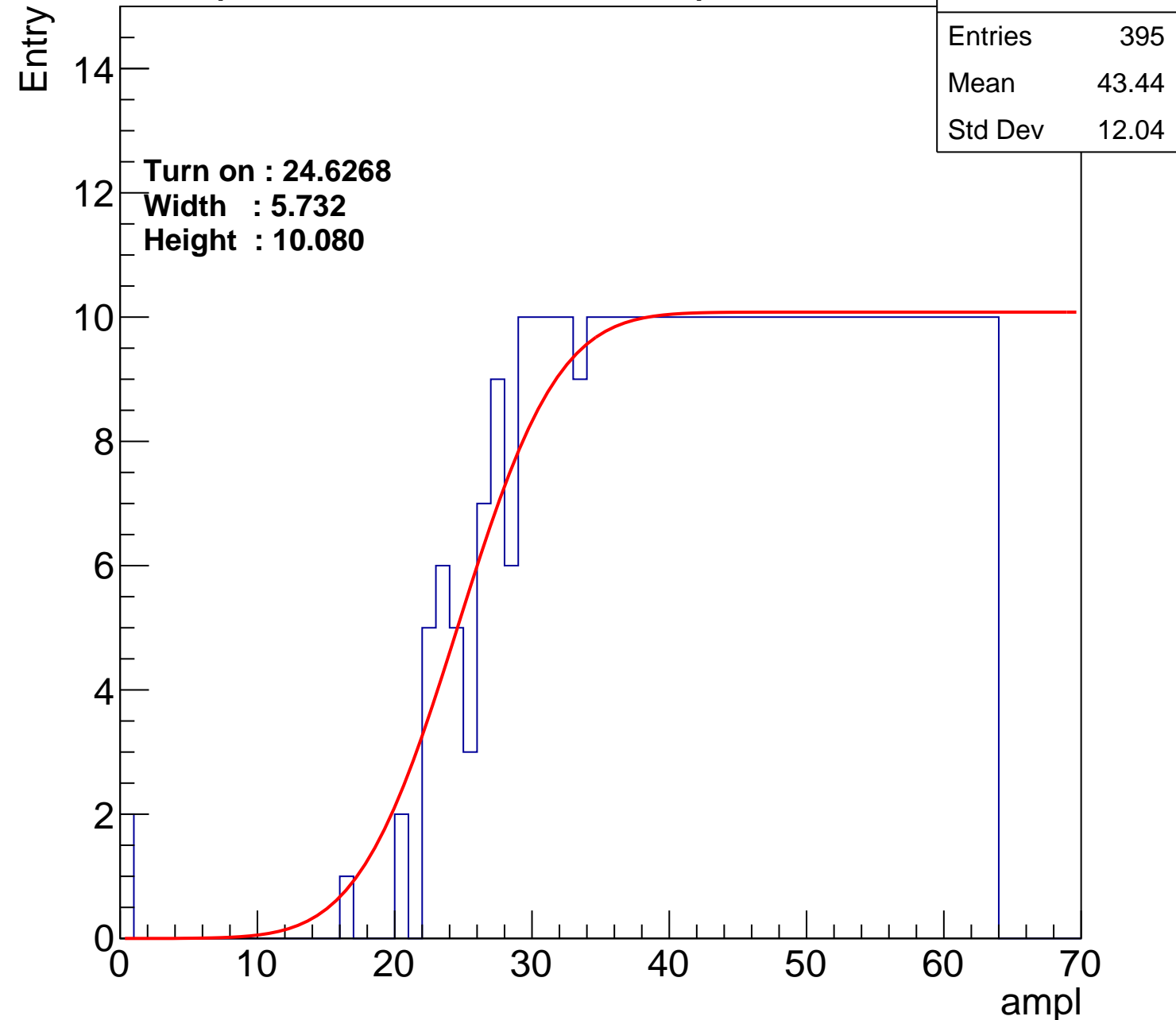
Width : 5.732

Height : 10.080

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch59

calib_packv5_042523_0143.root, FC#4, port A2

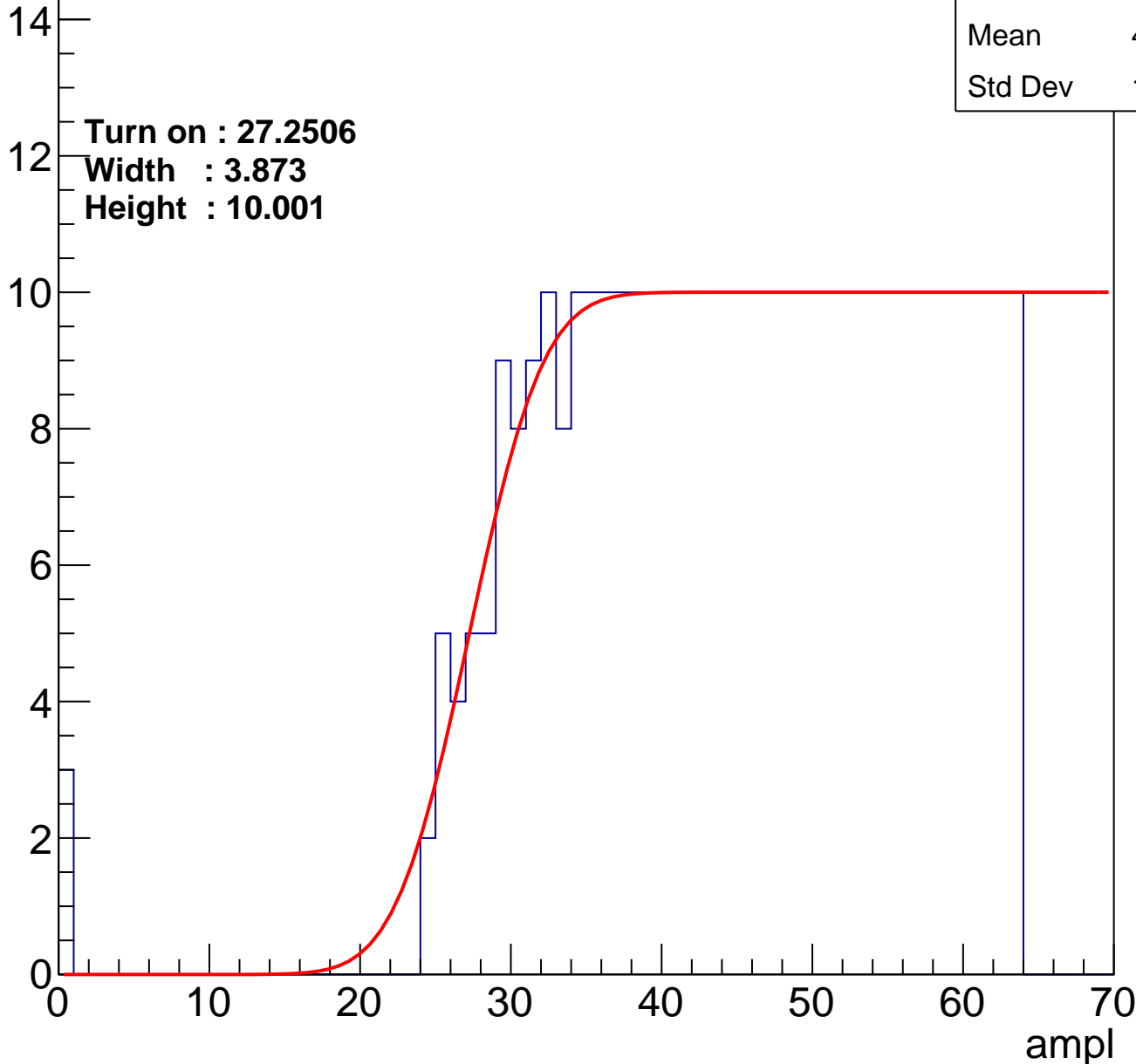
Entries	368
Mean	44.74
Std Dev	11.46

Turn on : 27.2506

Width : 3.873

Height : 10.001

Entry



B1L100S, U4-ch60

calib_packv5_042523_0143.root, FC#4, port A2

Entries	400
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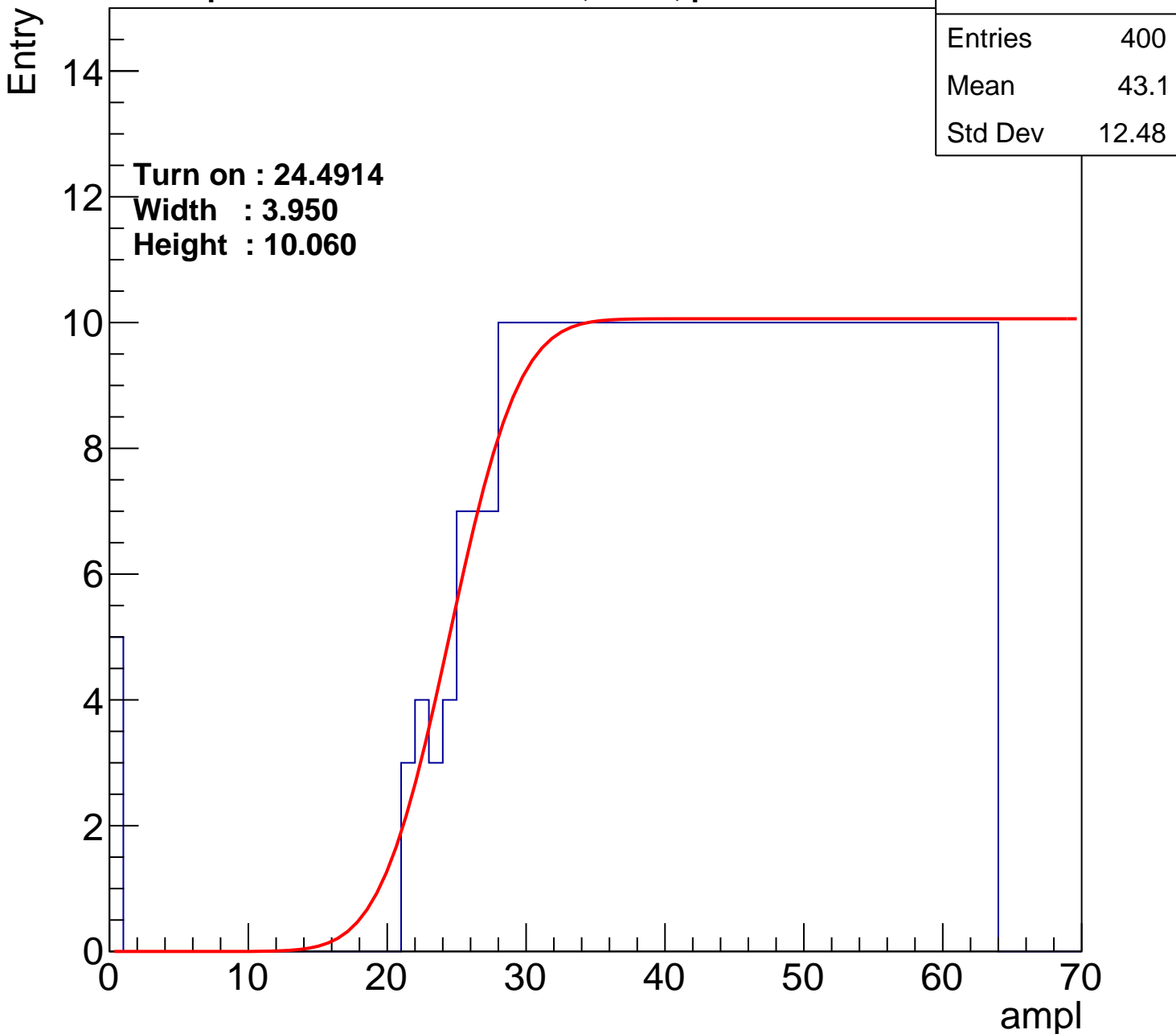
Mean	43.1
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Std Dev	12.48
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Turn on : 24.4914

Width : 3.950

Height : 10.060



B1L100S, U4-ch61

calib_packv5_042523_0143.root, FC#4, port A2

Entries	390
Mean	43.61
Std Dev	12.16

Turn on : 25.4909

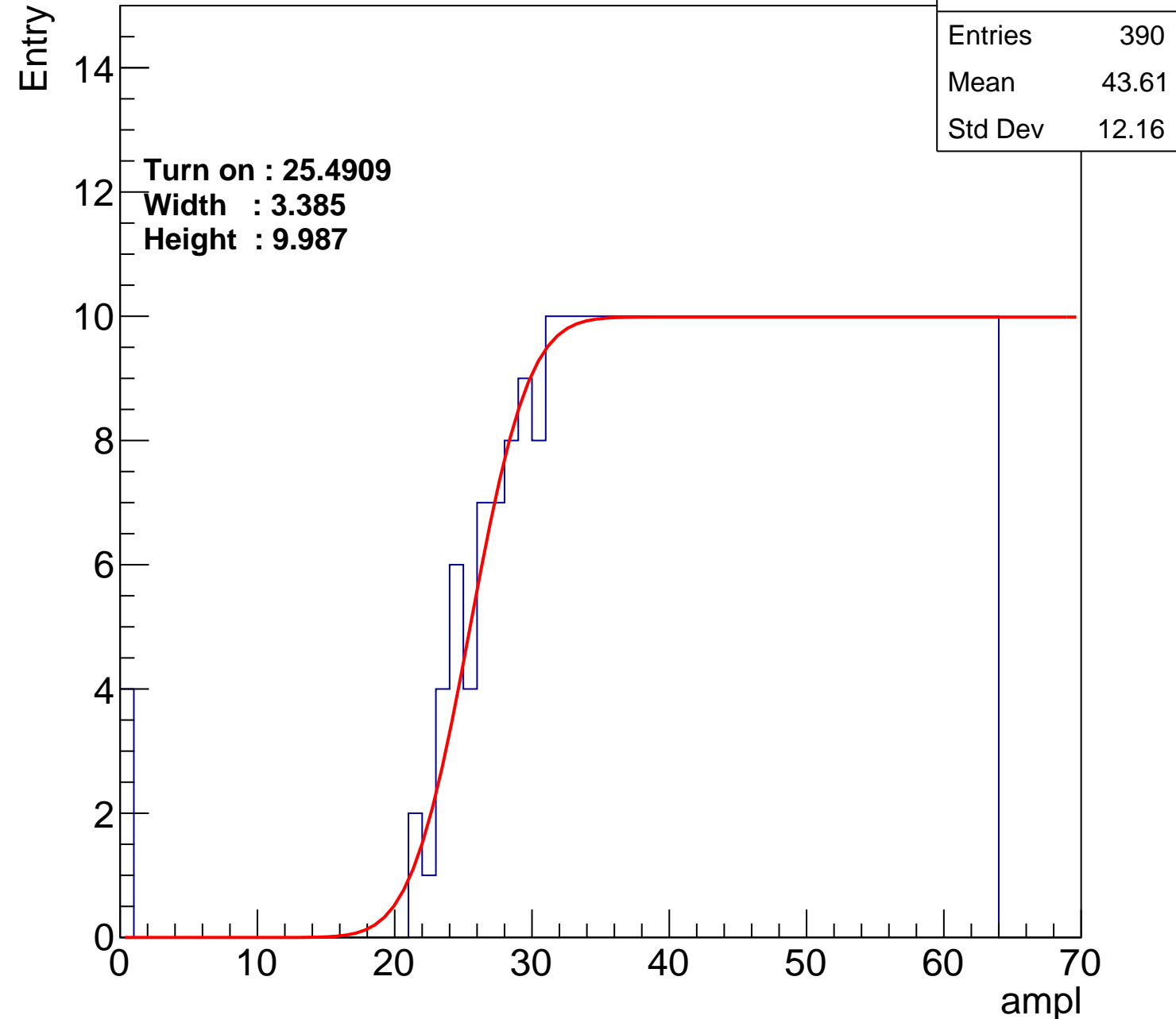
Width : 3.385

Height : 9.987

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch62

calib_packv5_042523_0143.root, FC#4, port A2

Entries	402
Mean	43.22
Std Dev	11.96

Turn on : 24.2391

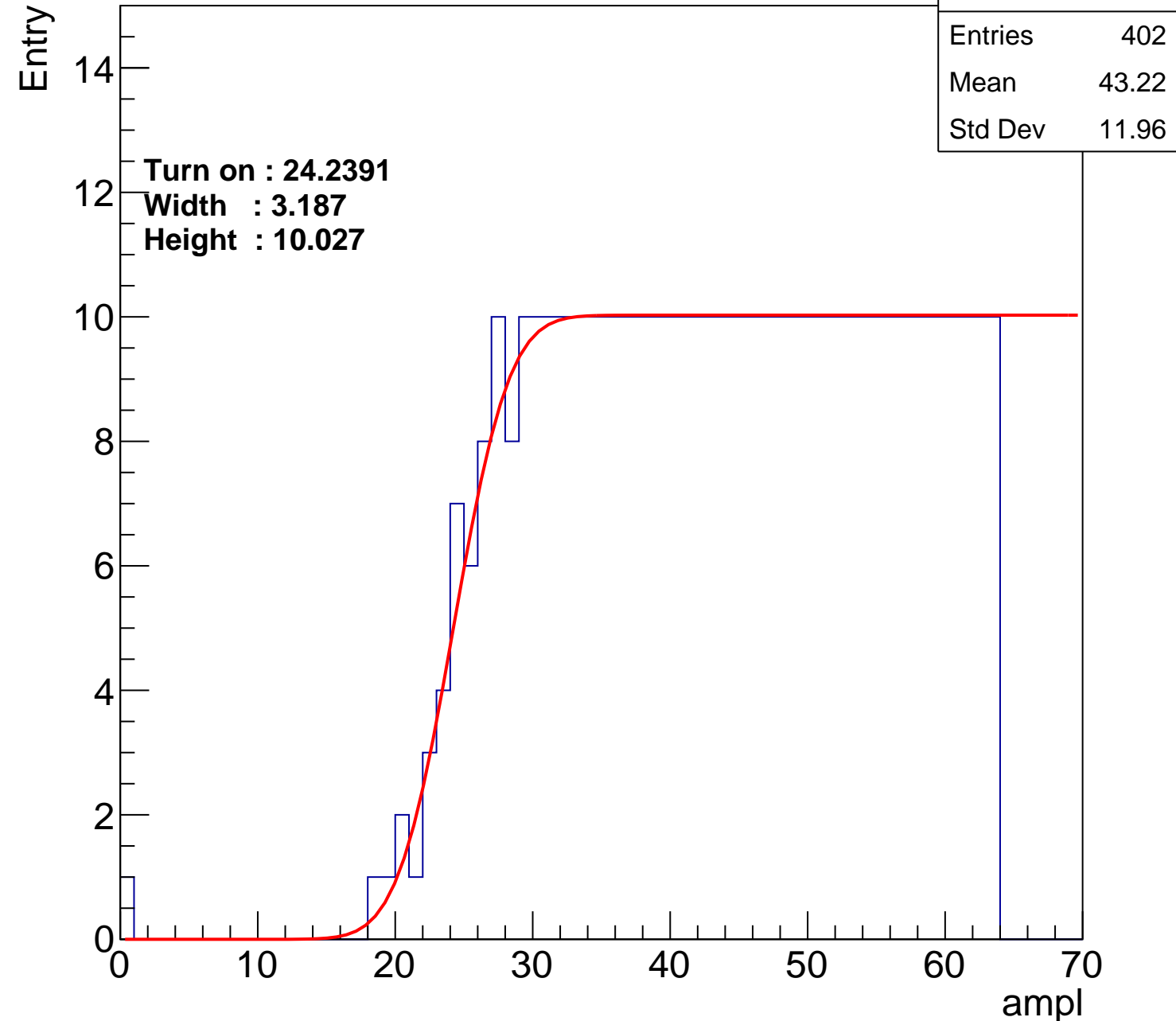
Width : 3.187

Height : 10.027

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch63

calib_packv5_042523_0143.root, FC#4, port A2

Entries	362
Mean	45.01
Std Dev	11.37

Turn on : 28.1850

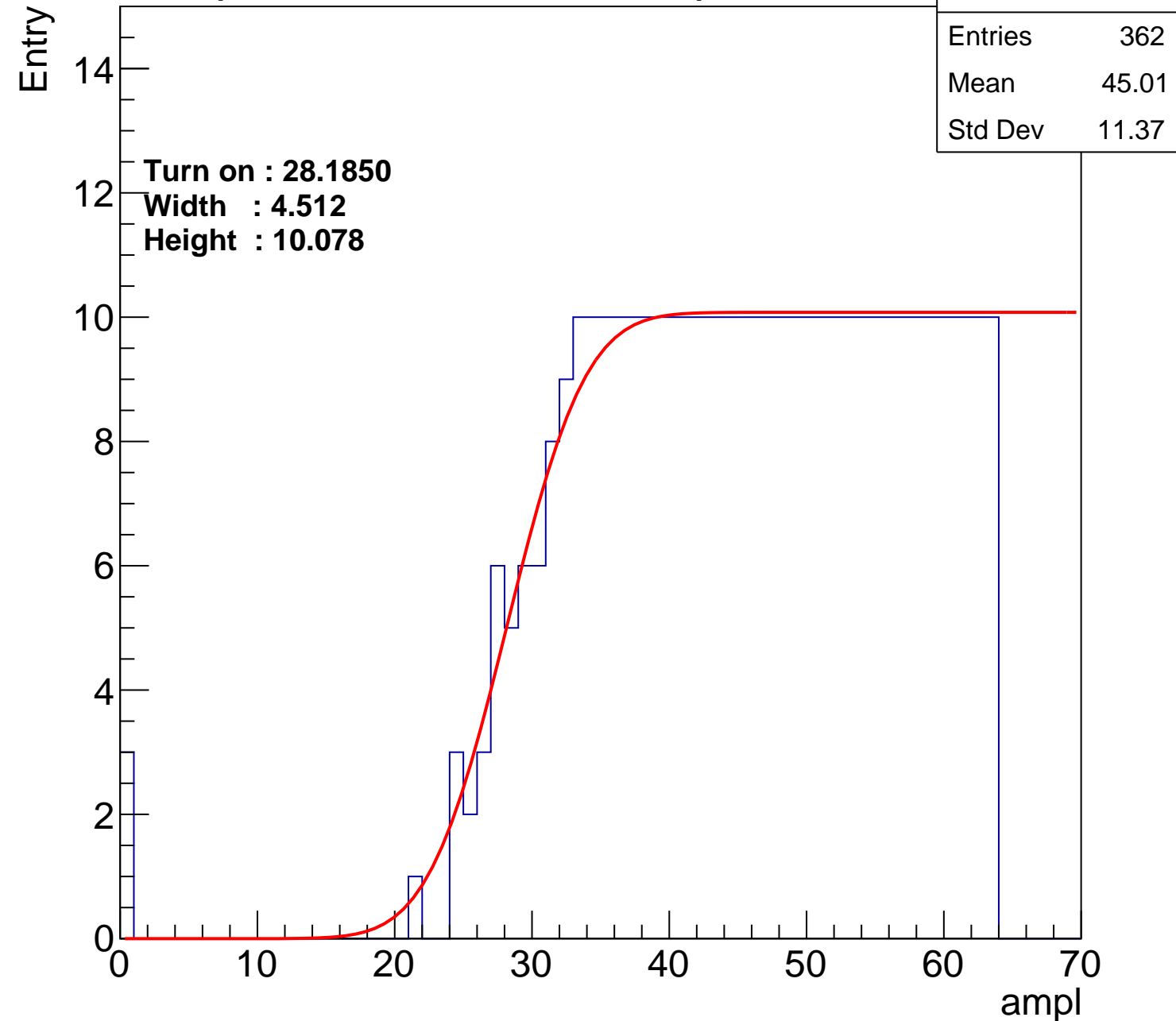
Width : 4.512

Height : 10.078

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch64

calib_packv5_042523_0143.root, FC#4, port A2

Entries	373
Mean	44.64
Std Dev	11.21

Turn on : 27.1015

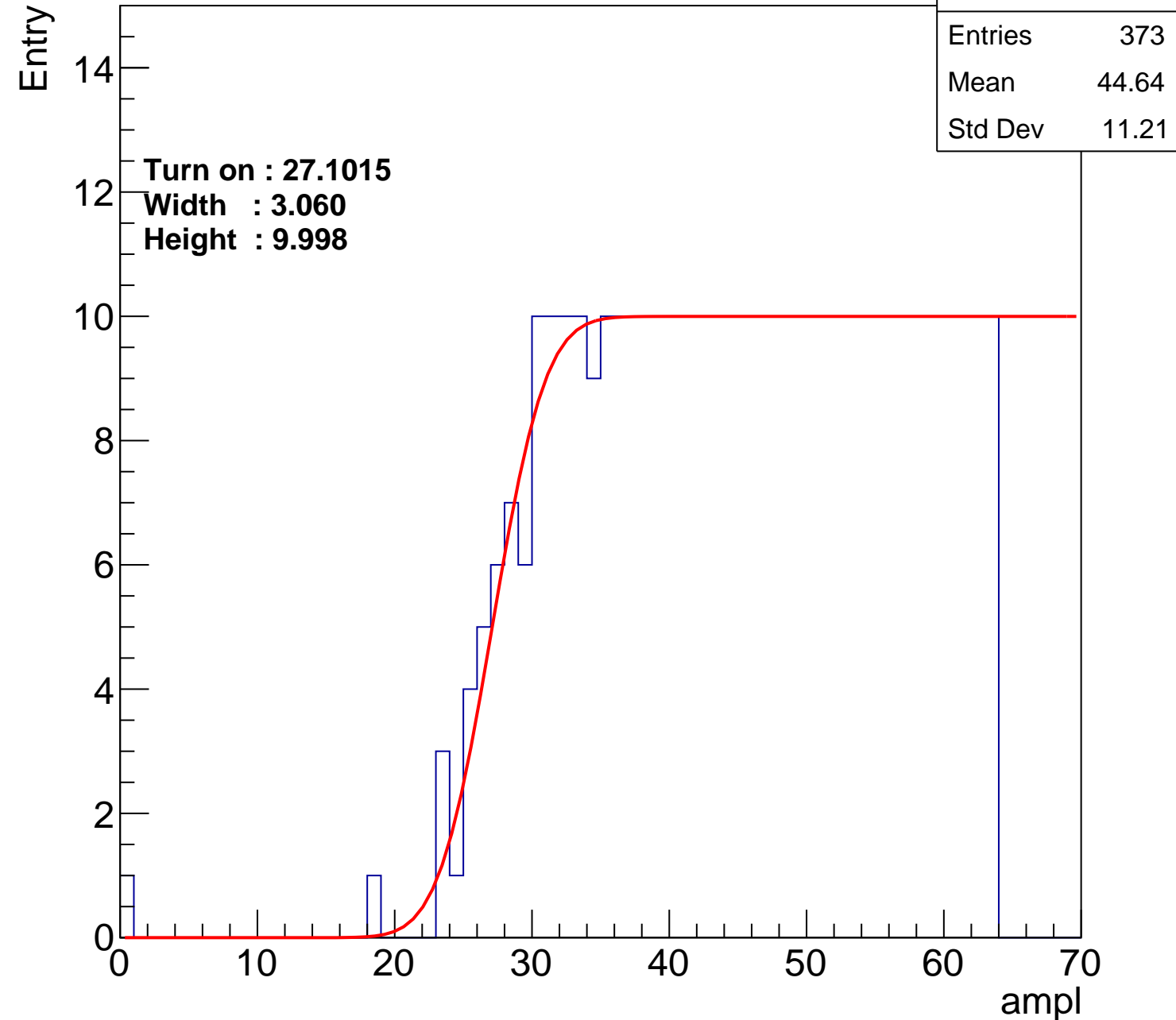
Width : 3.060

Height : 9.998

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch65

calib_packv5_042523_0143.root, FC#4, port A2

Entries	353
Mean	45.48
Std Dev	11.11

Turn on : 29.0852

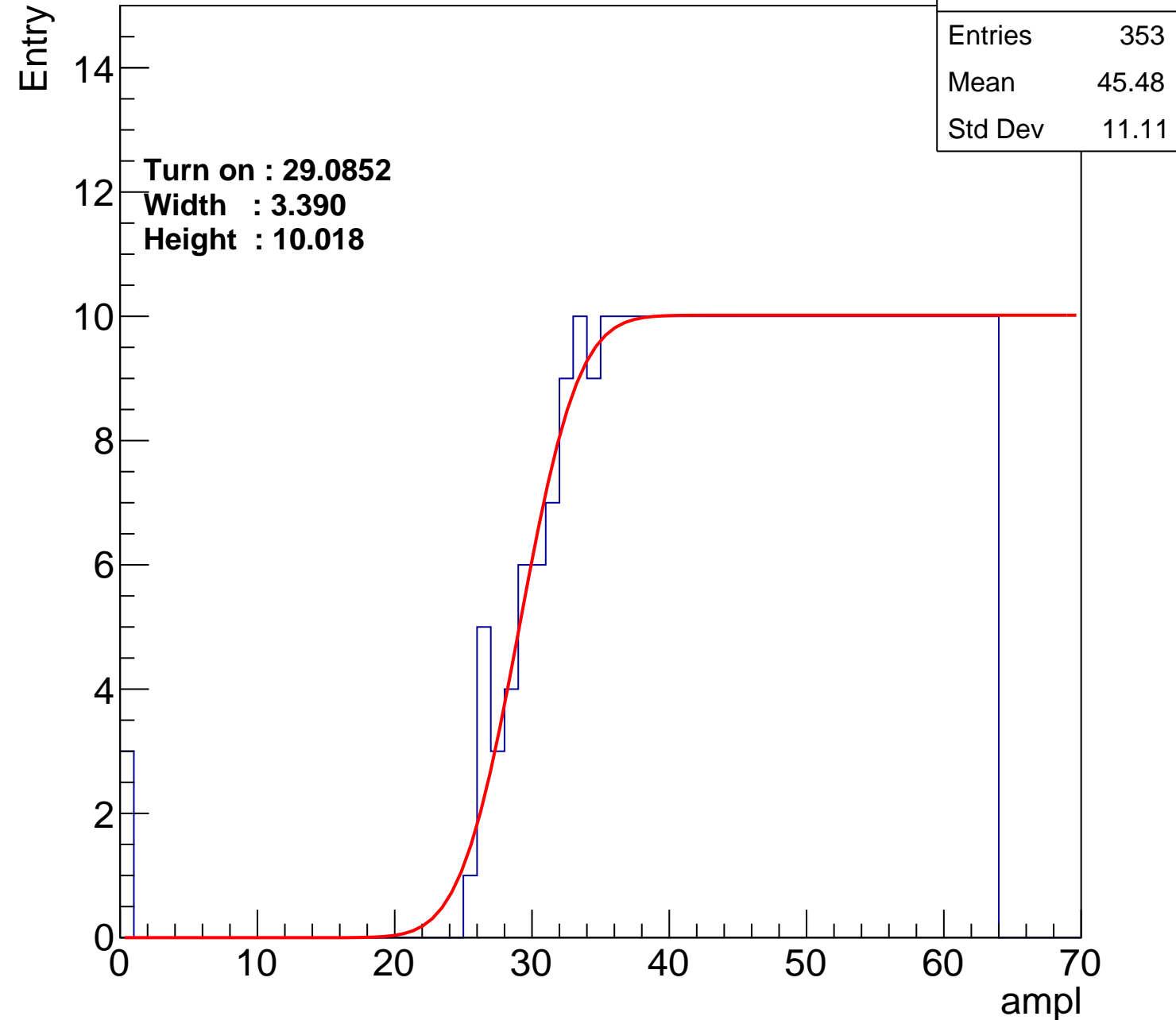
Width : 3.390

Height : 10.018

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch66

calib_packv5_042523_0143.root, FC#4, port A2

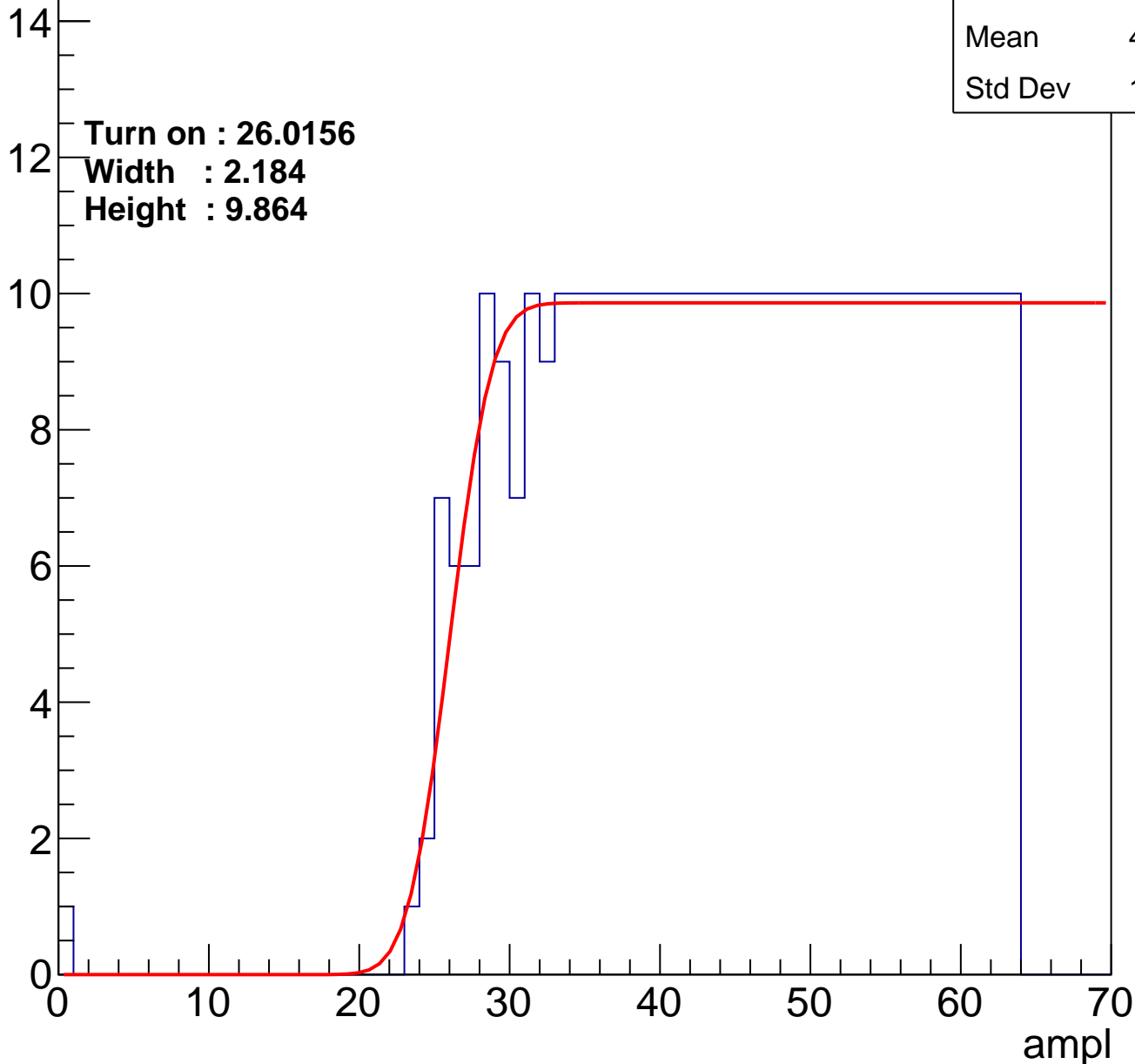
Entry

Entries	378
Mean	44.43
Std Dev	11.27

Turn on : 26.0156

Width : 2.184

Height : 9.864



B1L100S, U4-ch67

calib_packv5_042523_0143.root, FC#4, port A2

Entries	385
Mean	43.94
Std Dev	11.83

Turn on : 25.5749

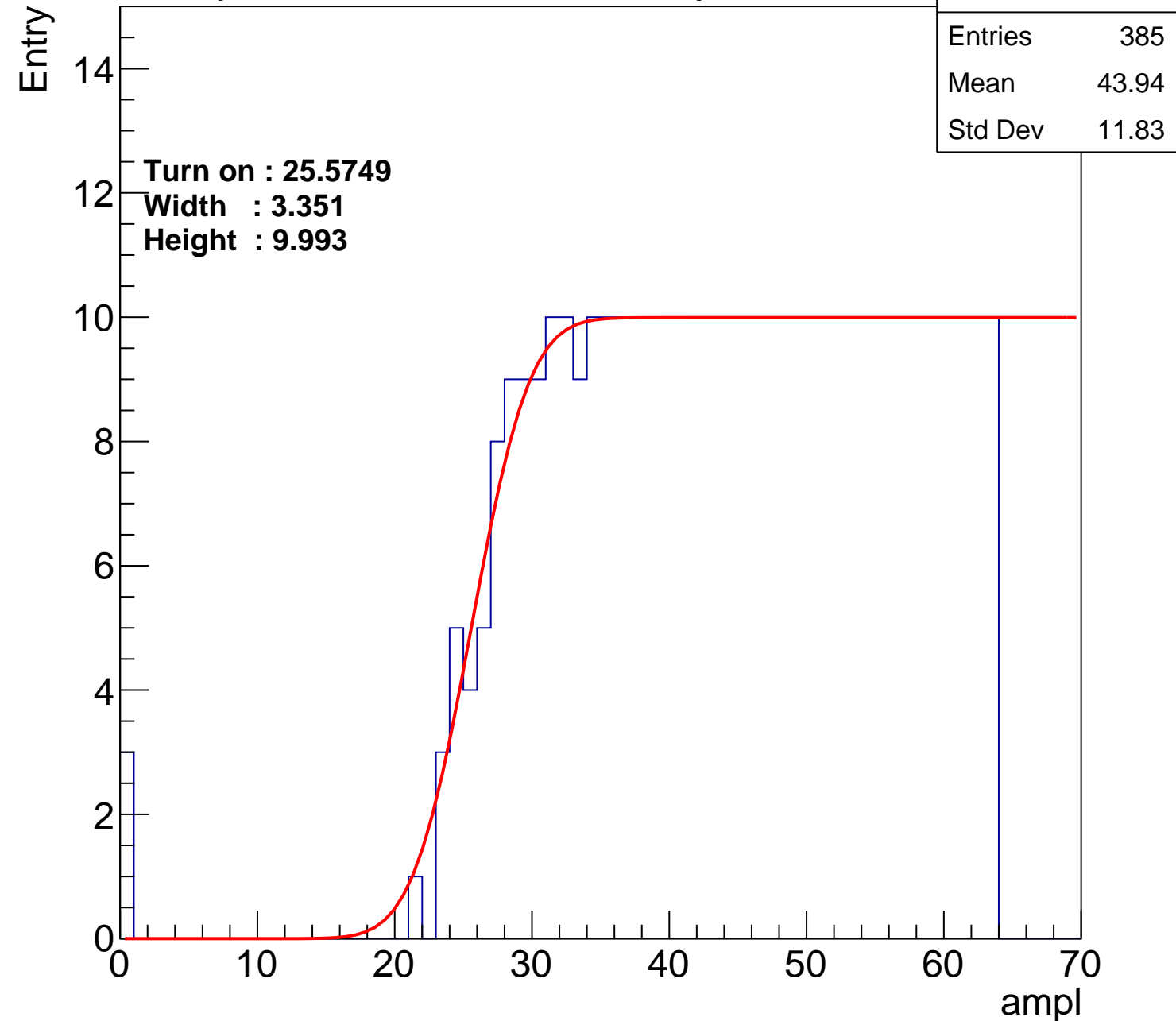
Width : 3.351

Height : 9.993

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch68

calib_packv5_042523_0143.root, FC#4, port A2

Entries	404
Mean	42.75
Std Dev	12.92

Turn on : 25.0562

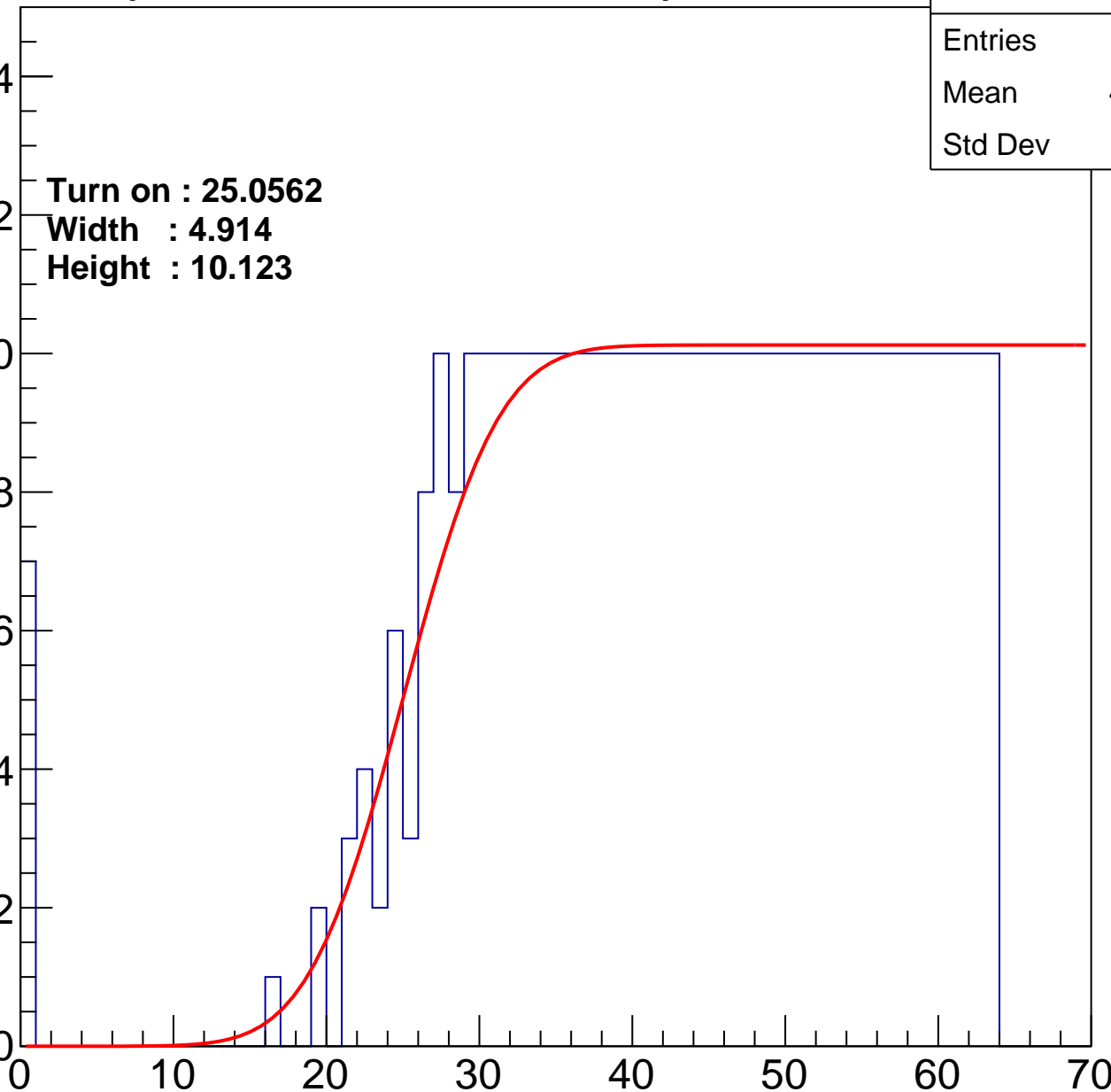
Width : 4.914

Height : 10.123

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch69

calib_packv5_042523_0143.root, FC#4, port A2

Entries	370
Mean	44.79
Std Dev	11.21

Turn on : 27.1541

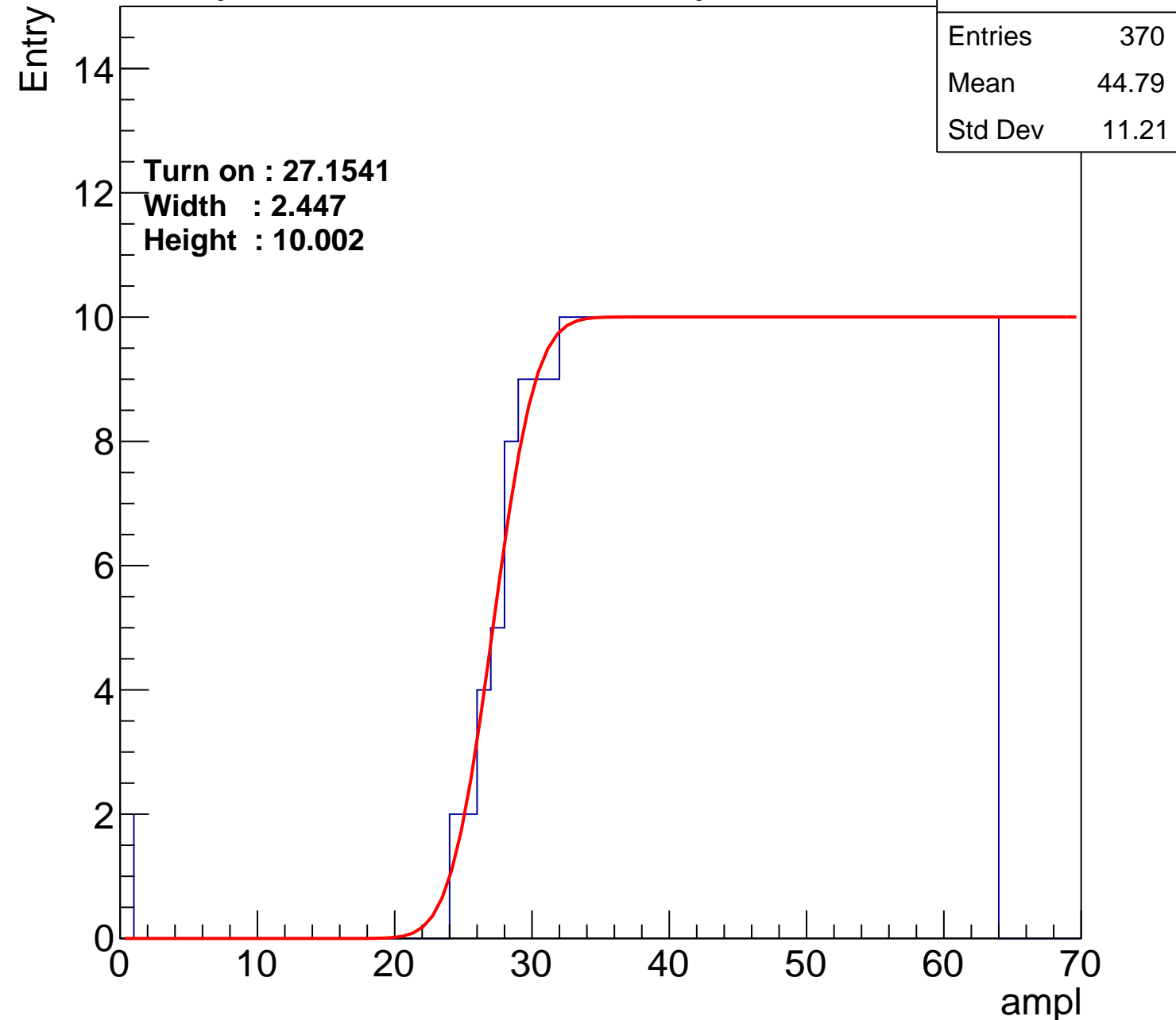
Width : 2.447

Height : 10.002

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch70

calib_packv5_042523_0143.root, FC#4, port A2

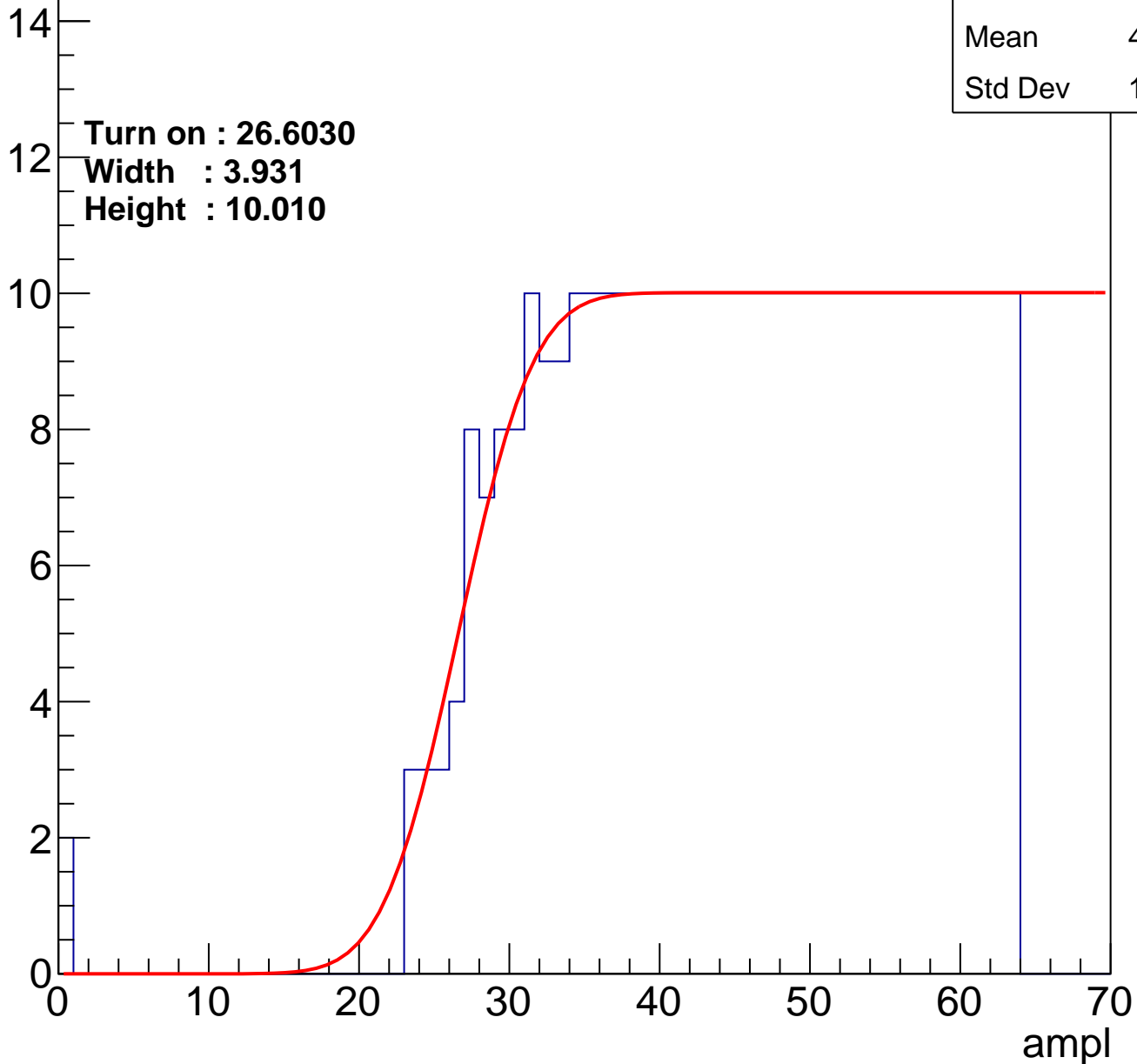
Entries	374
Mean	44.52
Std Dev	11.42

Turn on : 26.6030

Width : 3.931

Height : 10.010

Entry



B1L100S, U4-ch71

calib_packv5_042523_0143.root, FC#4, port A2

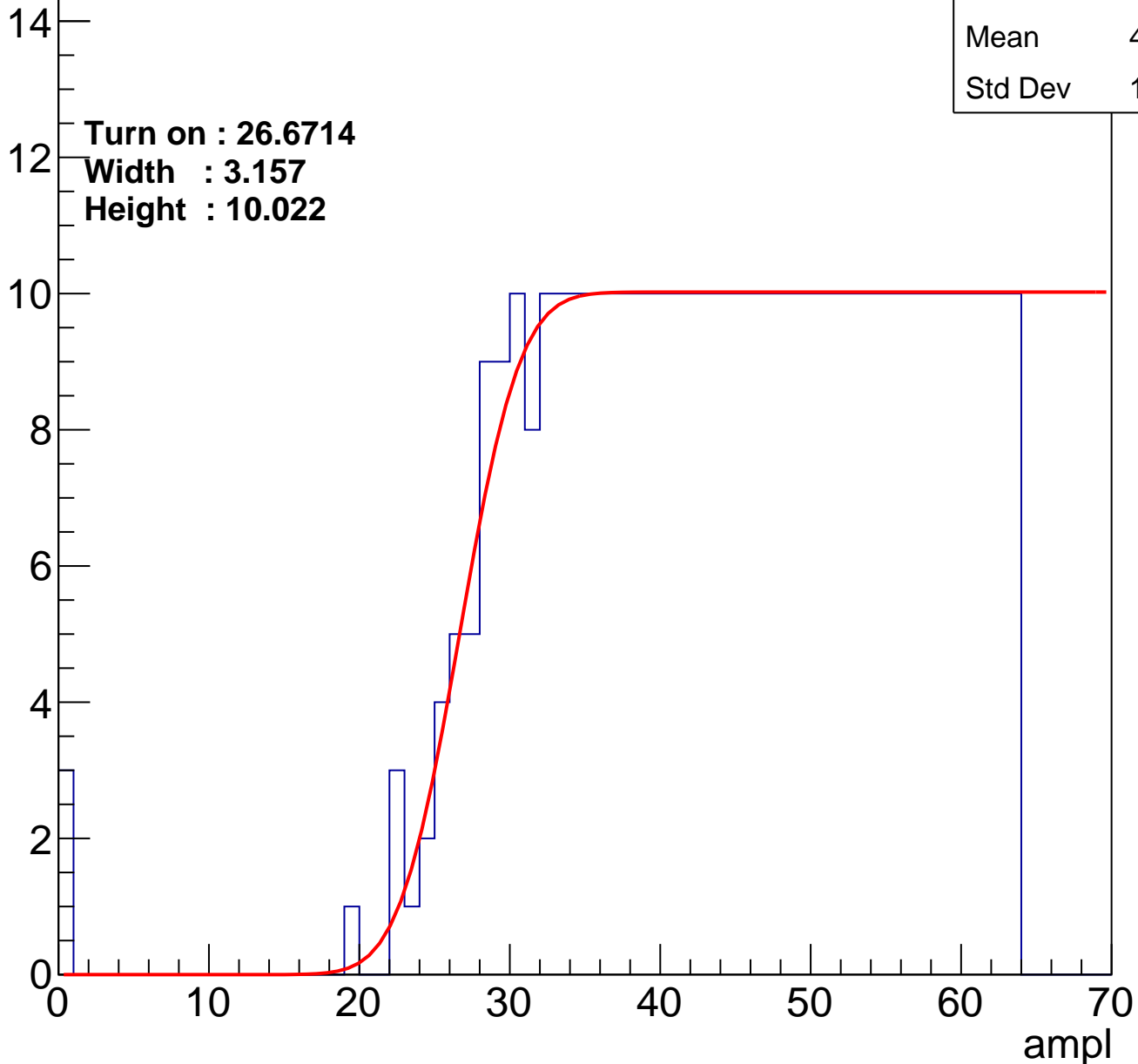
Entries	380
Mean	44.16
Std Dev	11.75

Turn on : 26.6714

Width : 3.157

Height : 10.022

Entry



B1L100S, U4-ch72

calib_packv5_042523_0143.root, FC#4, port A2

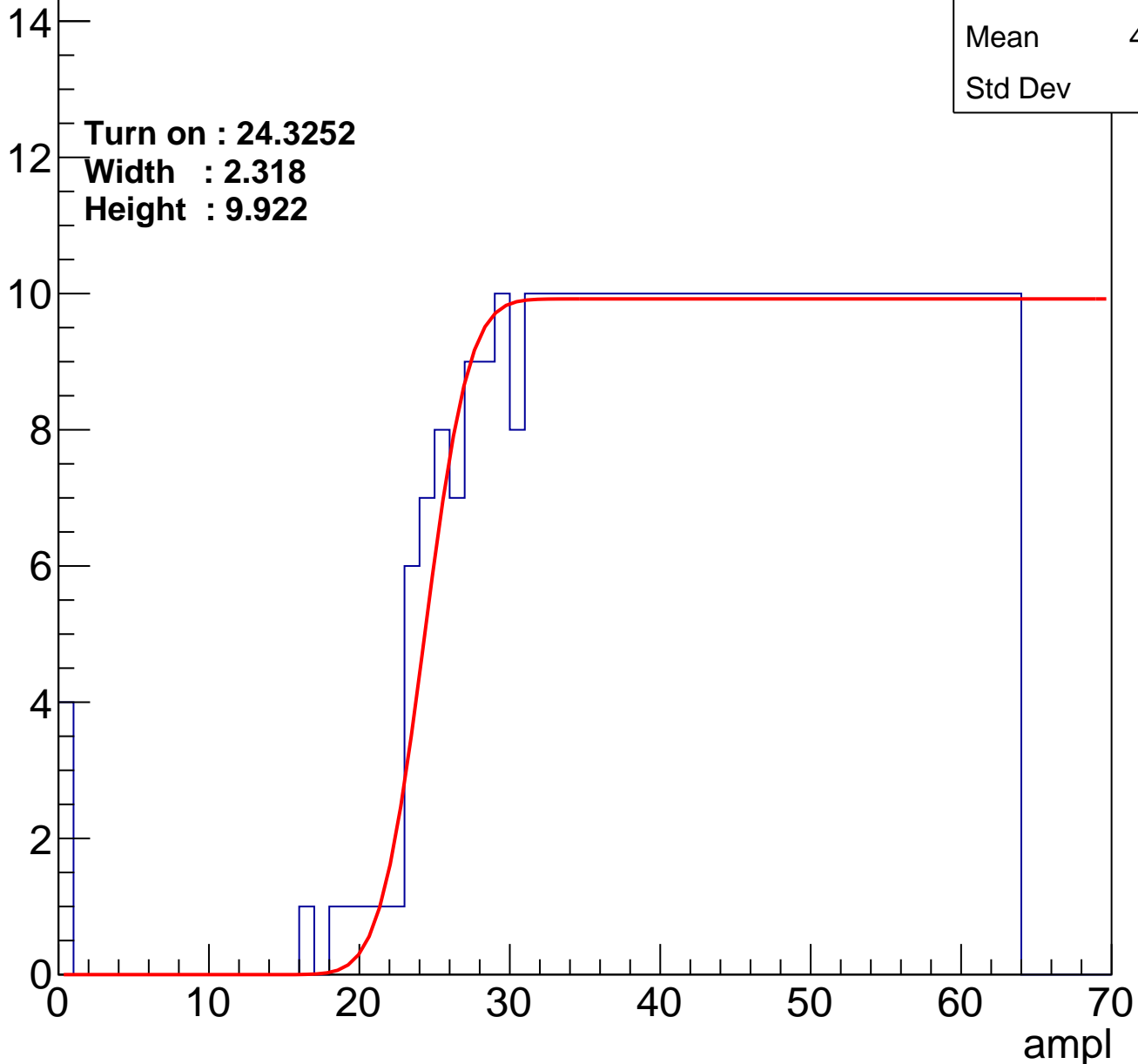
Entries	404
Mean	42.92
Std Dev	12.5

Turn on : 24.3252

Width : 2.318

Height : 9.922

Entry



B1L100S, U4-ch73

calib_packv5_042523_0143.root, FC#4, port A2

Entries	368
Mean	44.74
Std Dev	11.47

Turn on : 27.9803

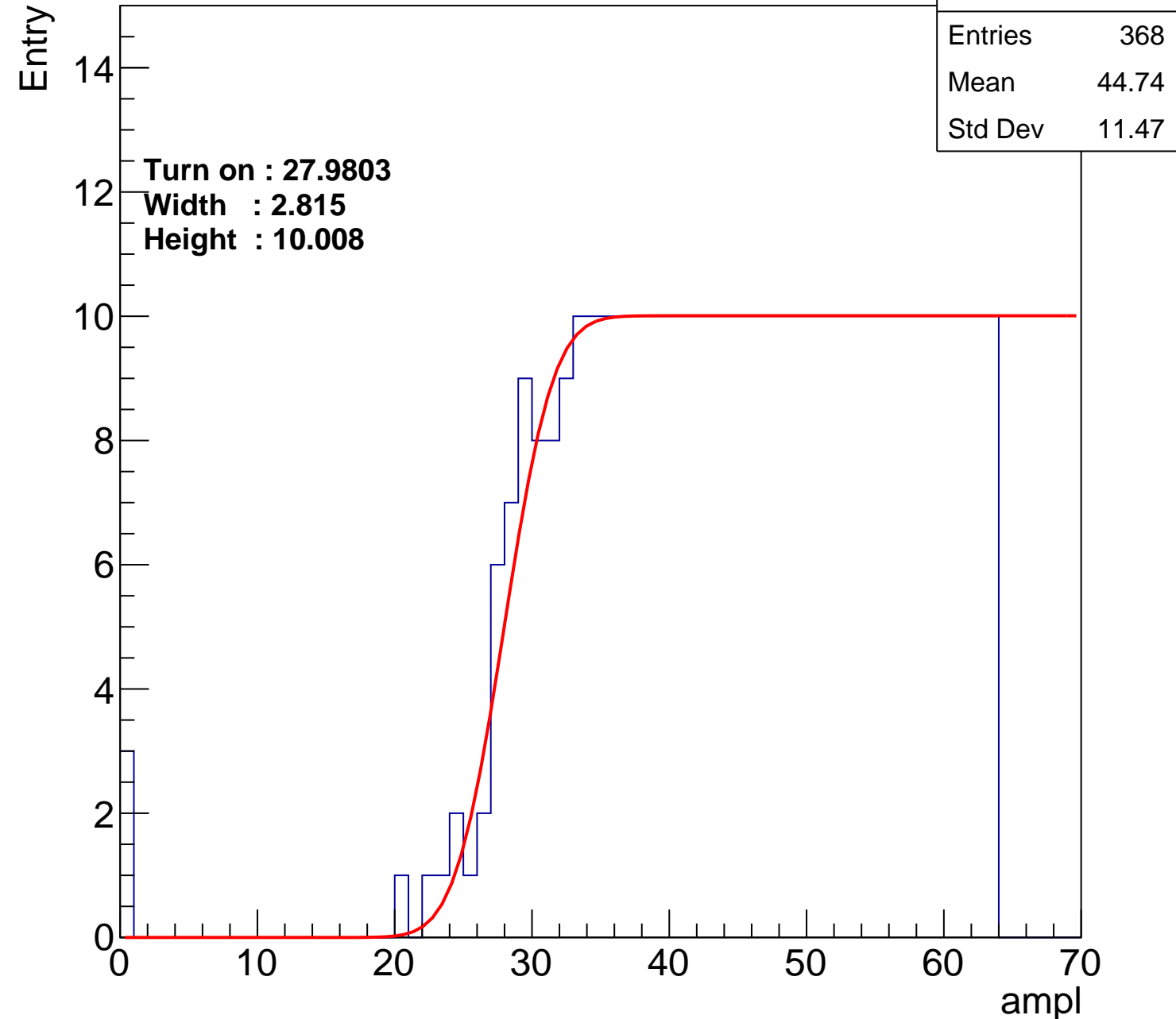
Width : 2.815

Height : 10.008

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch74

calib_packv5_042523_0143.root, FC#4, port A2

Entries	397
Mean	43.24
Std Dev	12.42

Turn on : 24.9119

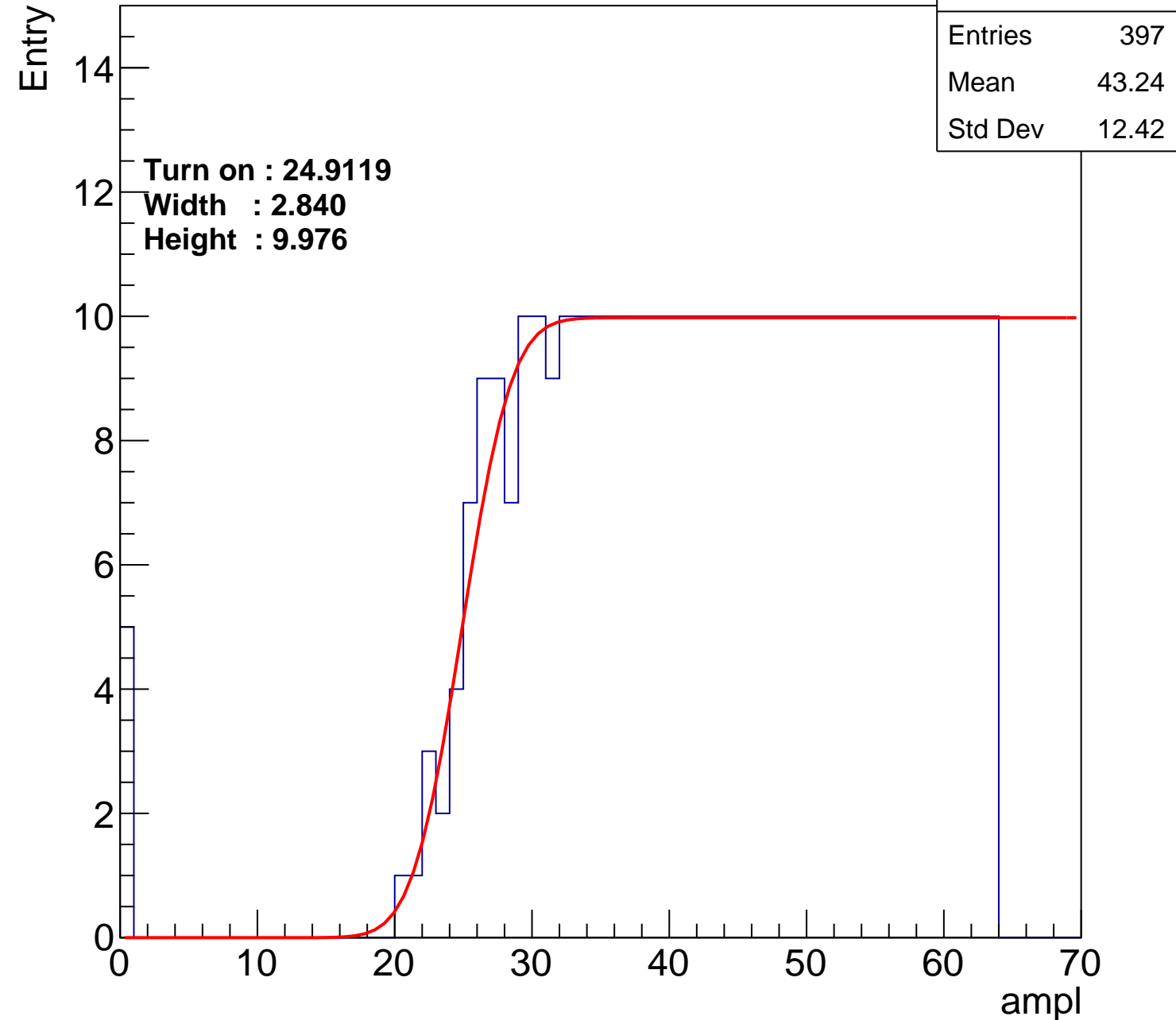
Width : 2.840

Height : 9.976

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch75

calib_packv5_042523_0143.root, FC#4, port A2

Entries	380
Mean	44.14
Std Dev	11.86

Turn on : 26.5911

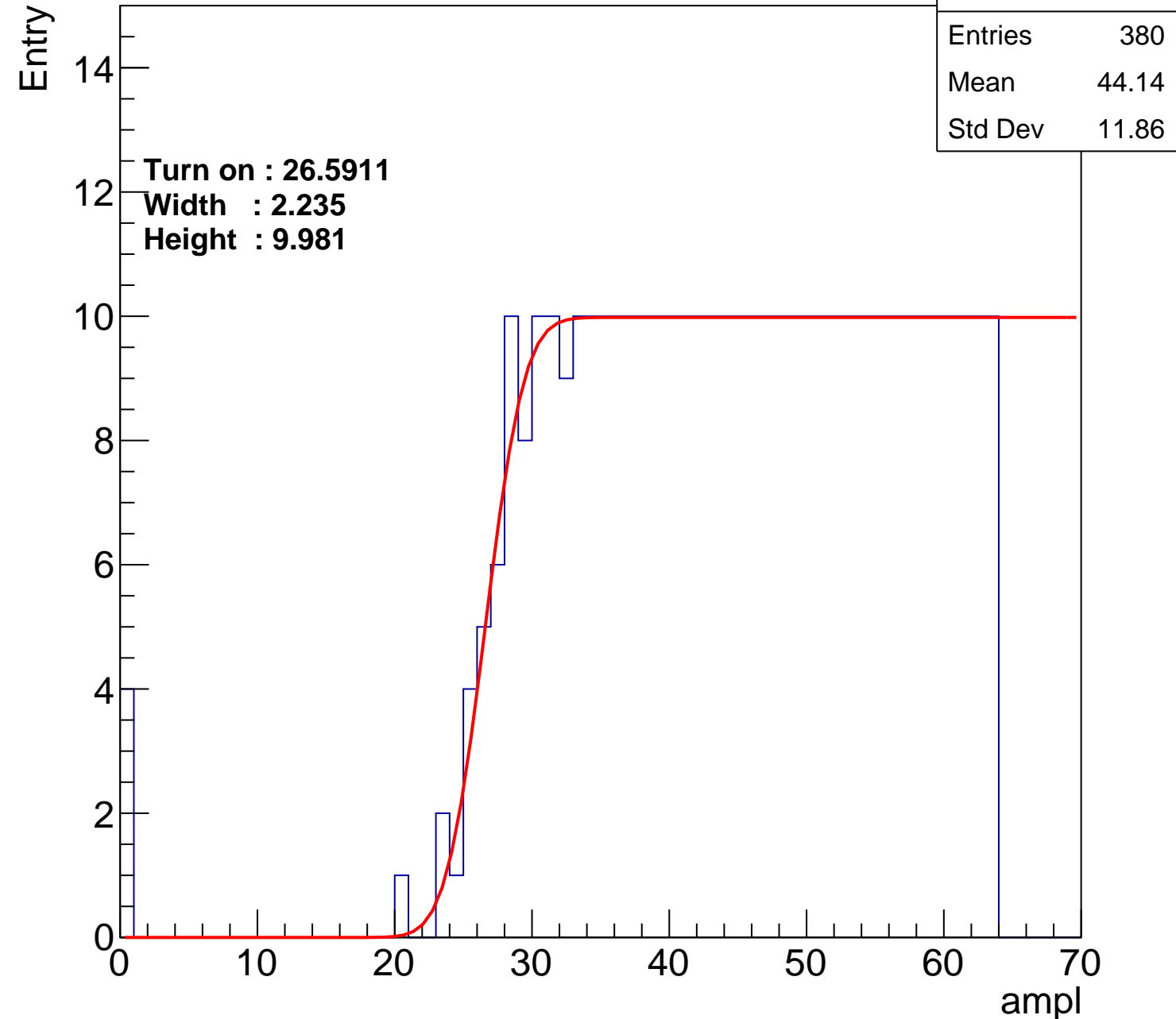
Width : 2.235

Height : 9.981

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch76

calib_packv5_042523_0143.root, FC#4, port A2

Entries	389
Mean	43.75
Std Dev	11.86

Turn on : 25.8277

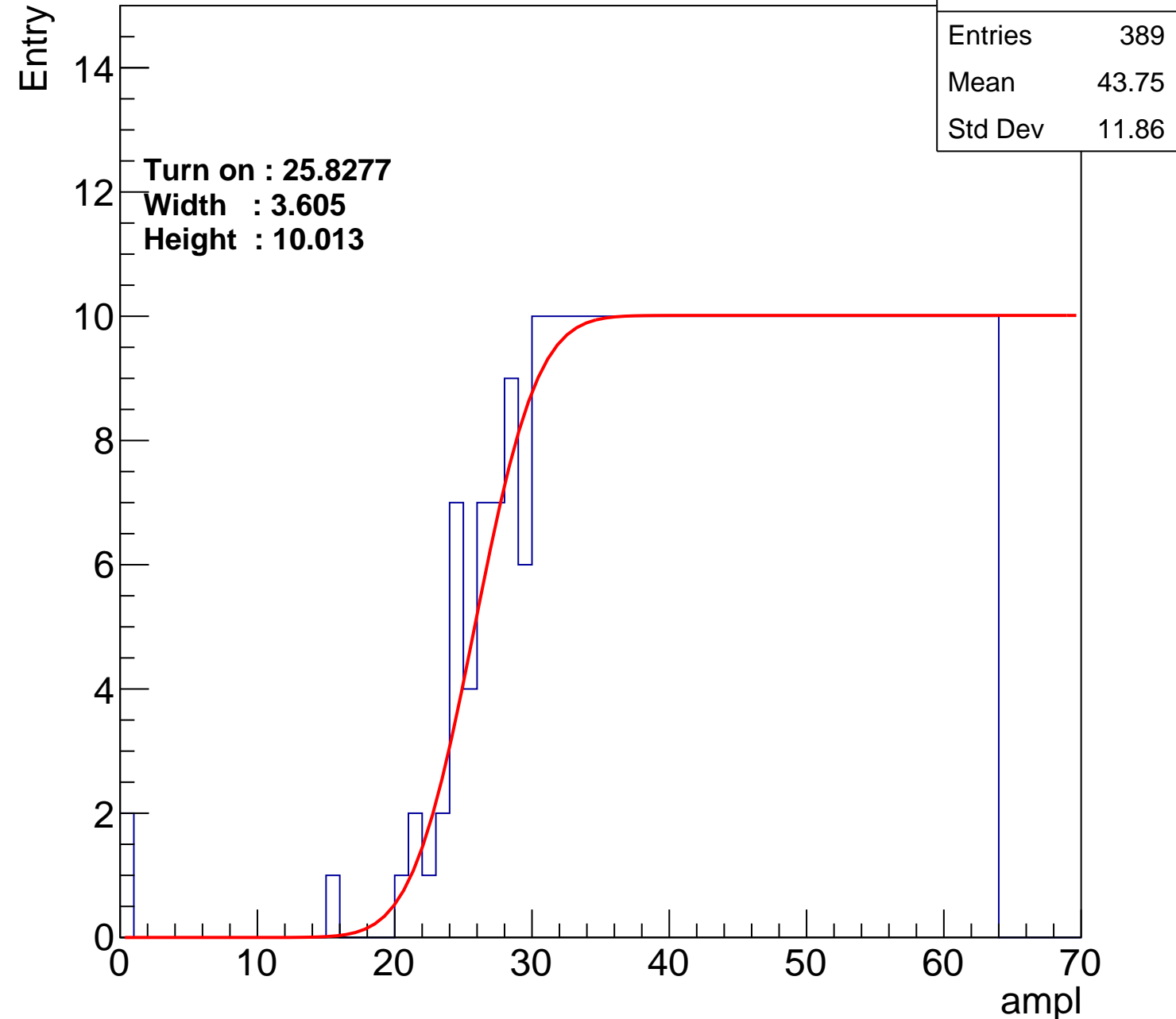
Width : 3.605

Height : 10.013

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch77

calib_packv5_042523_0143.root, FC#4, port A2

Entries	374
Mean	44.48
Std Dev	11.57

Turn on : 27.4822

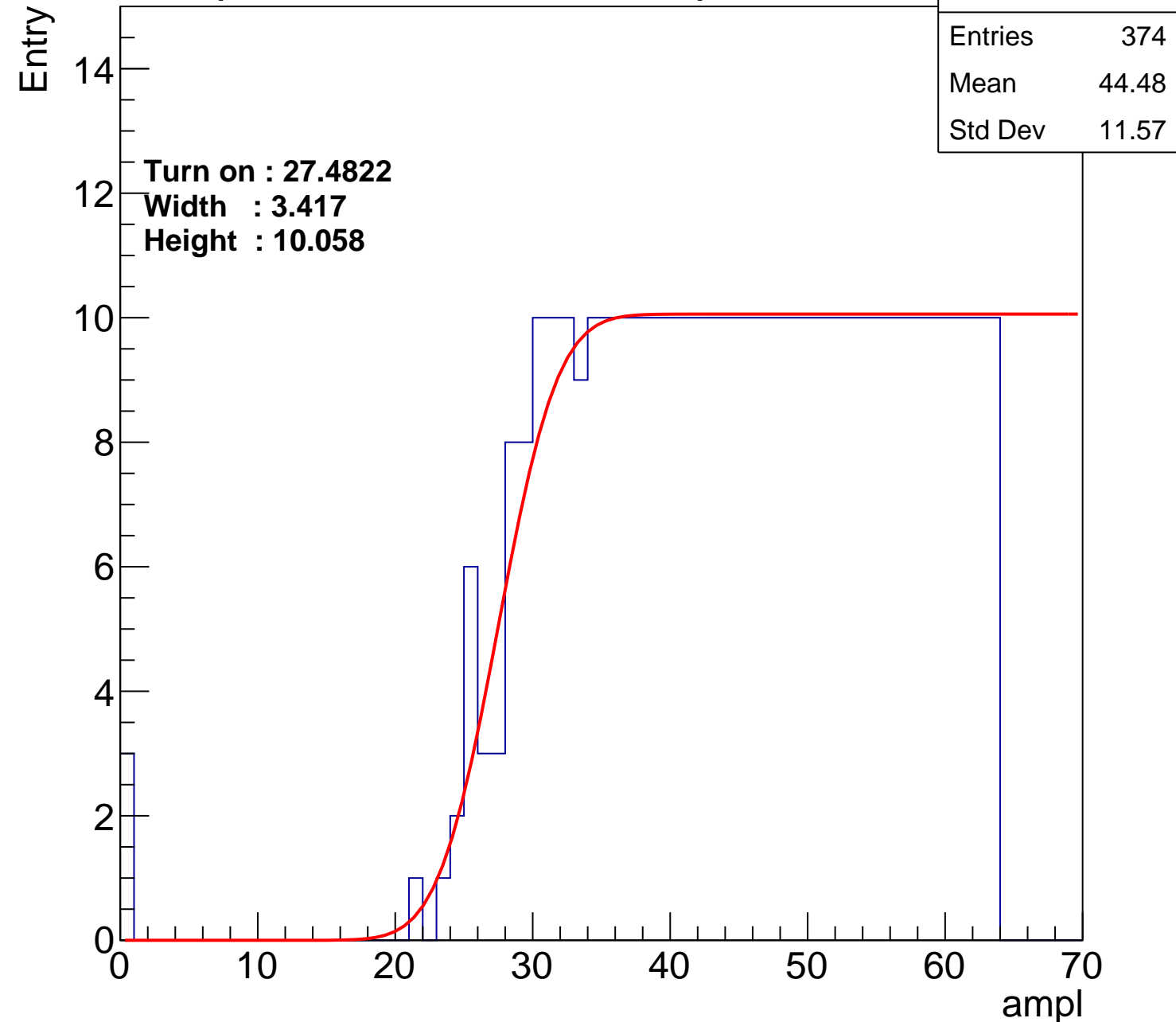
Width : 3.417

Height : 10.058

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch78

calib_packv5_042523_0143.root, FC#4, port A2

Entries	386
Mean	43.82
Std Dev	12.05

Turn on : 26.1847

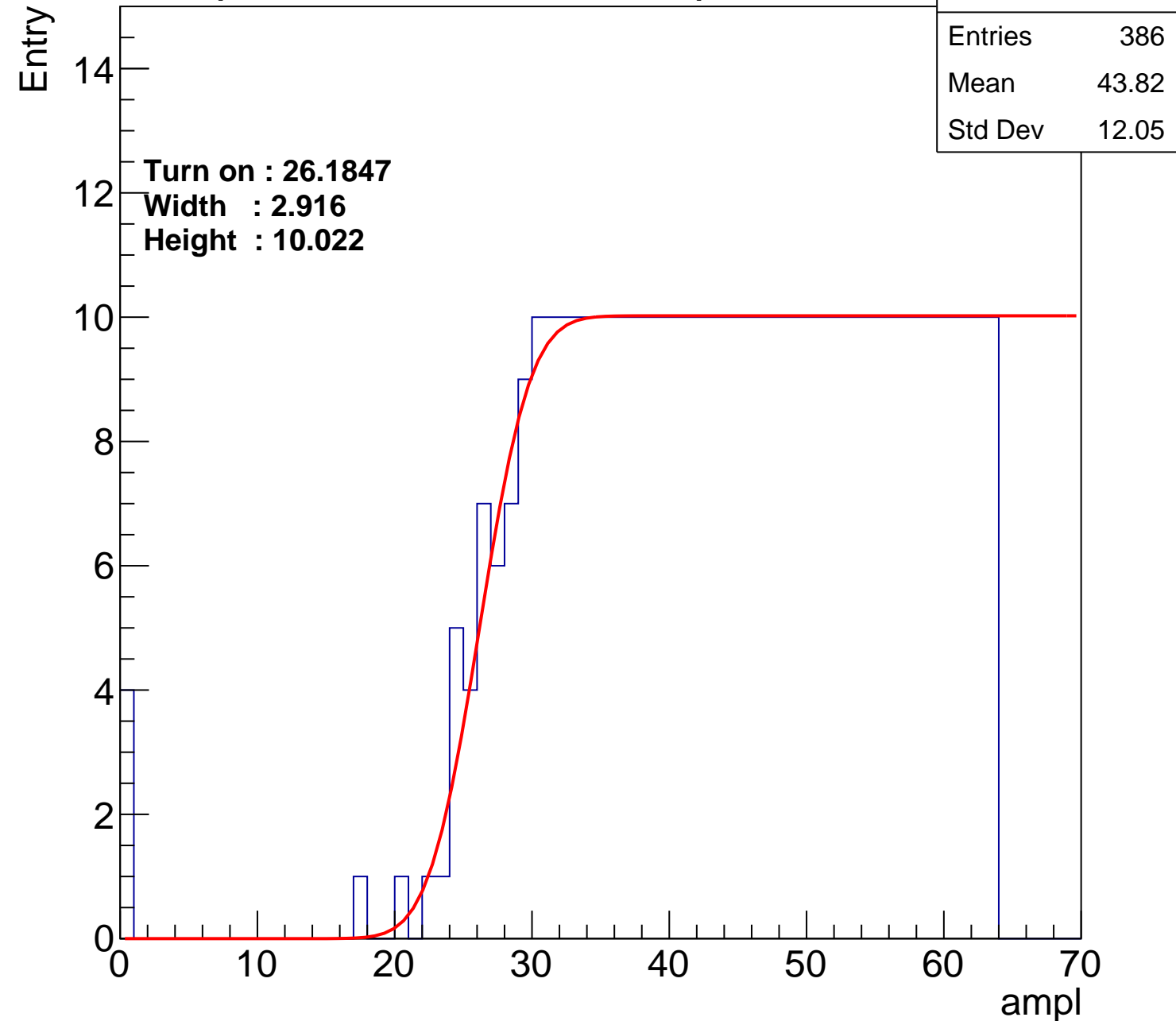
Width : 2.916

Height : 10.022

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch79

calib_packv5_042523_0143.root, FC#4, port A2

Entries	386
Mean	44.03
Std Dev	11.49

Turn on : 25.4502

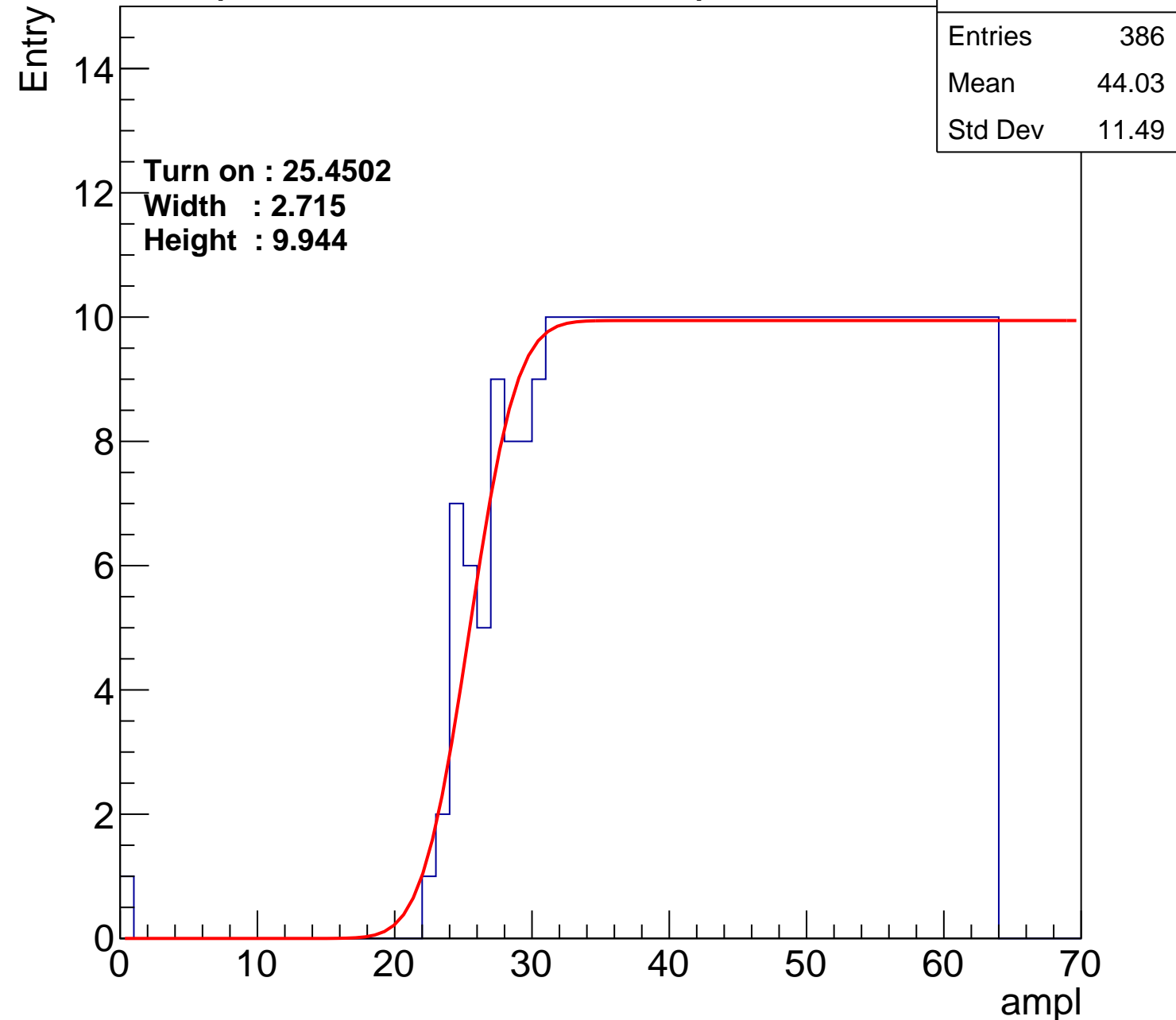
Width : 2.715

Height : 9.944

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch80

calib_packv5_042523_0143.root, FC#4, port A2

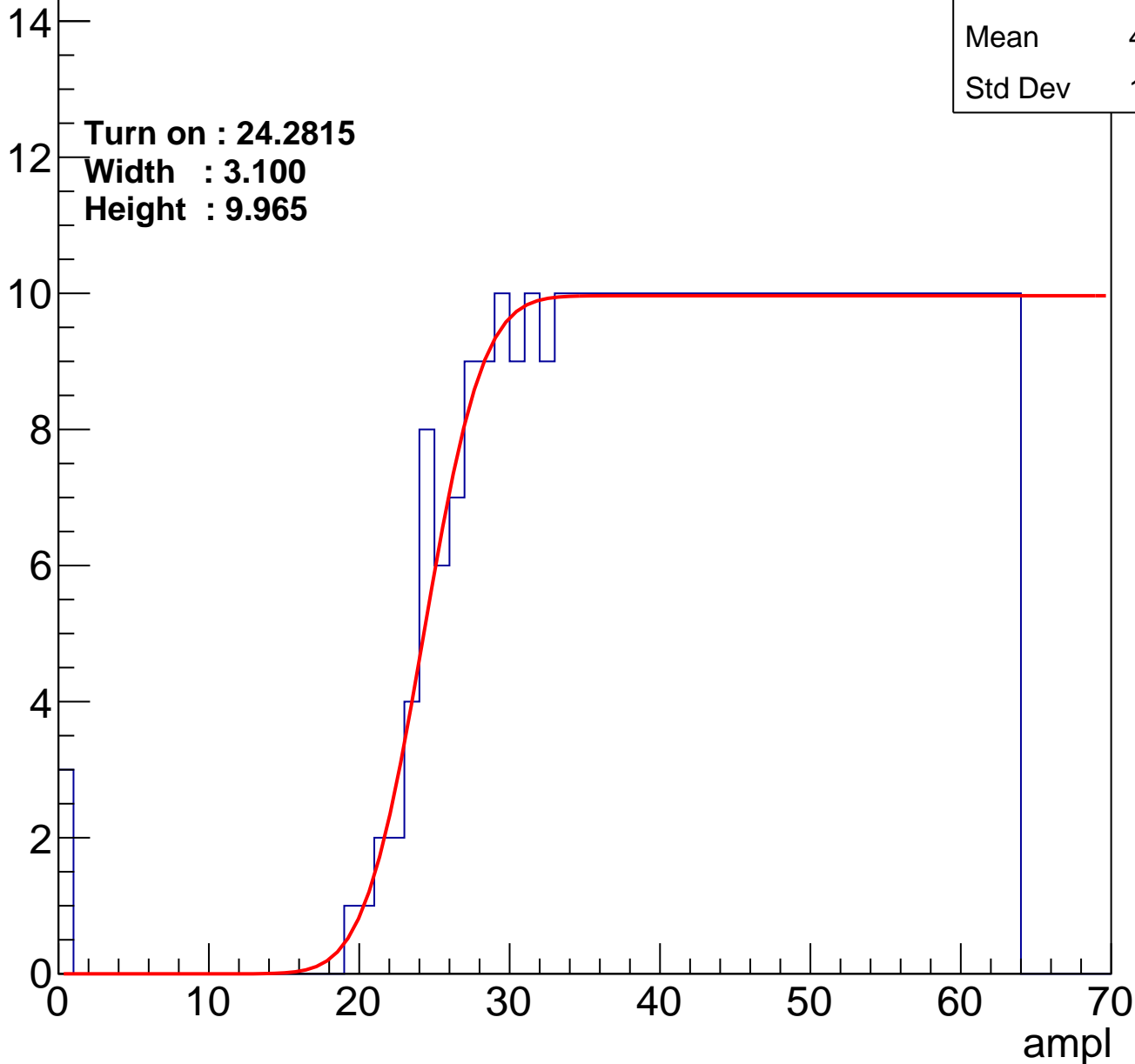
Entry

Entries	400
Mean	43.19
Std Dev	12.23

Turn on : 24.2815

Width : 3.100

Height : 9.965



B1L100S, U4-ch81

calib_packv5_042523_0143.root, FC#4, port A2

Entries	377
Mean	44.43
Std Dev	11.34

Turn on : 26.9550

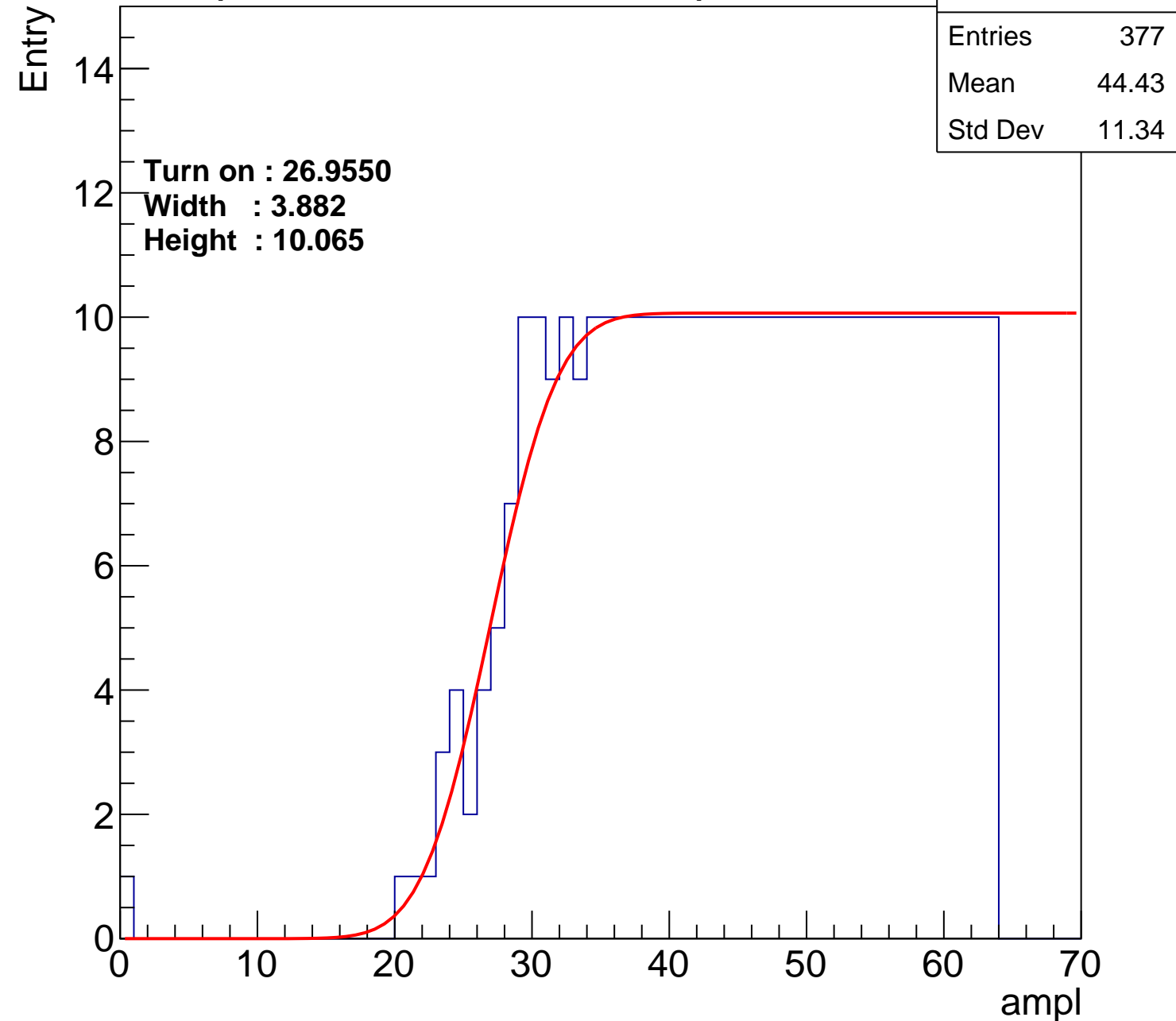
Width : 3.882

Height : 10.065

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch82

calib_packv5_042523_0143.root, FC#4, port A2

Entries	383
Mean	43.9
Std Dev	12.14

Turn on : 26.9350

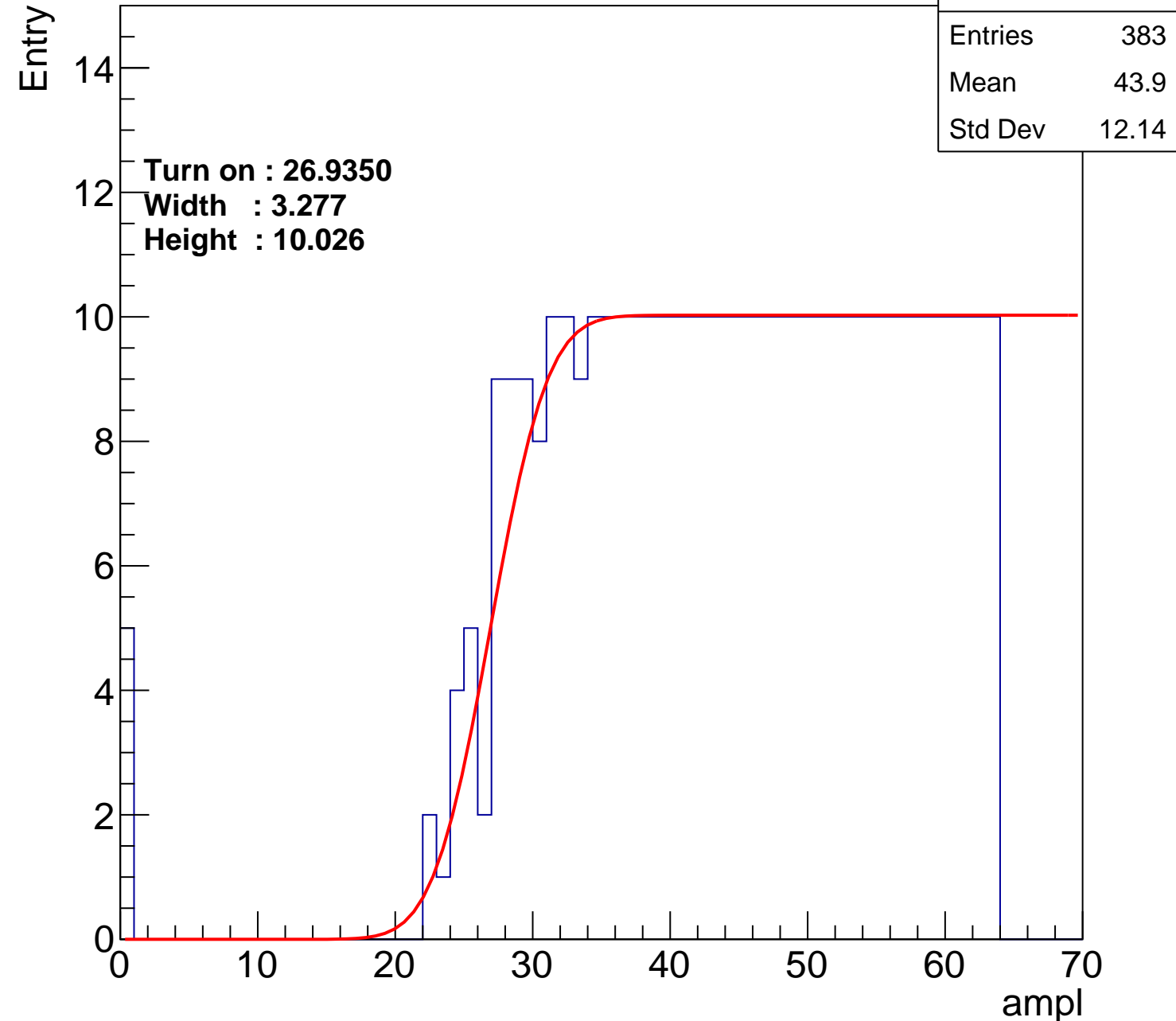
Width : 3.277

Height : 10.026

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch83

calib_packv5_042523_0143.root, FC#4, port A2

Entries	387
Mean	43.77
Std Dev	12.14

Turn on : 26.4099

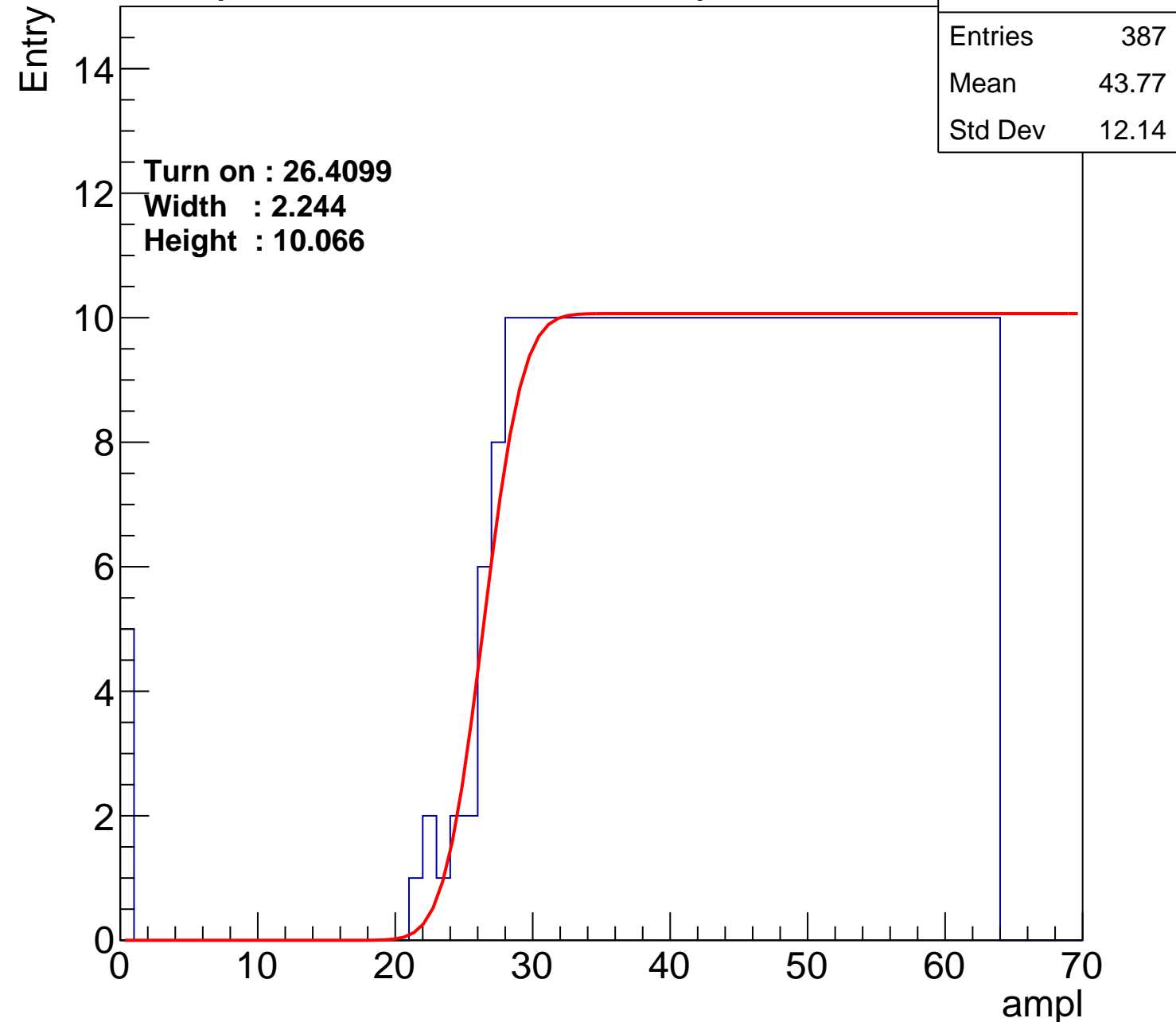
Width : 2.244

Height : 10.066

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch84

calib_packv5_042523_0143.root, FC#4, port A2

Entries	368
Mean	44.86
Std Dev	11.21

Turn on : 27.7197

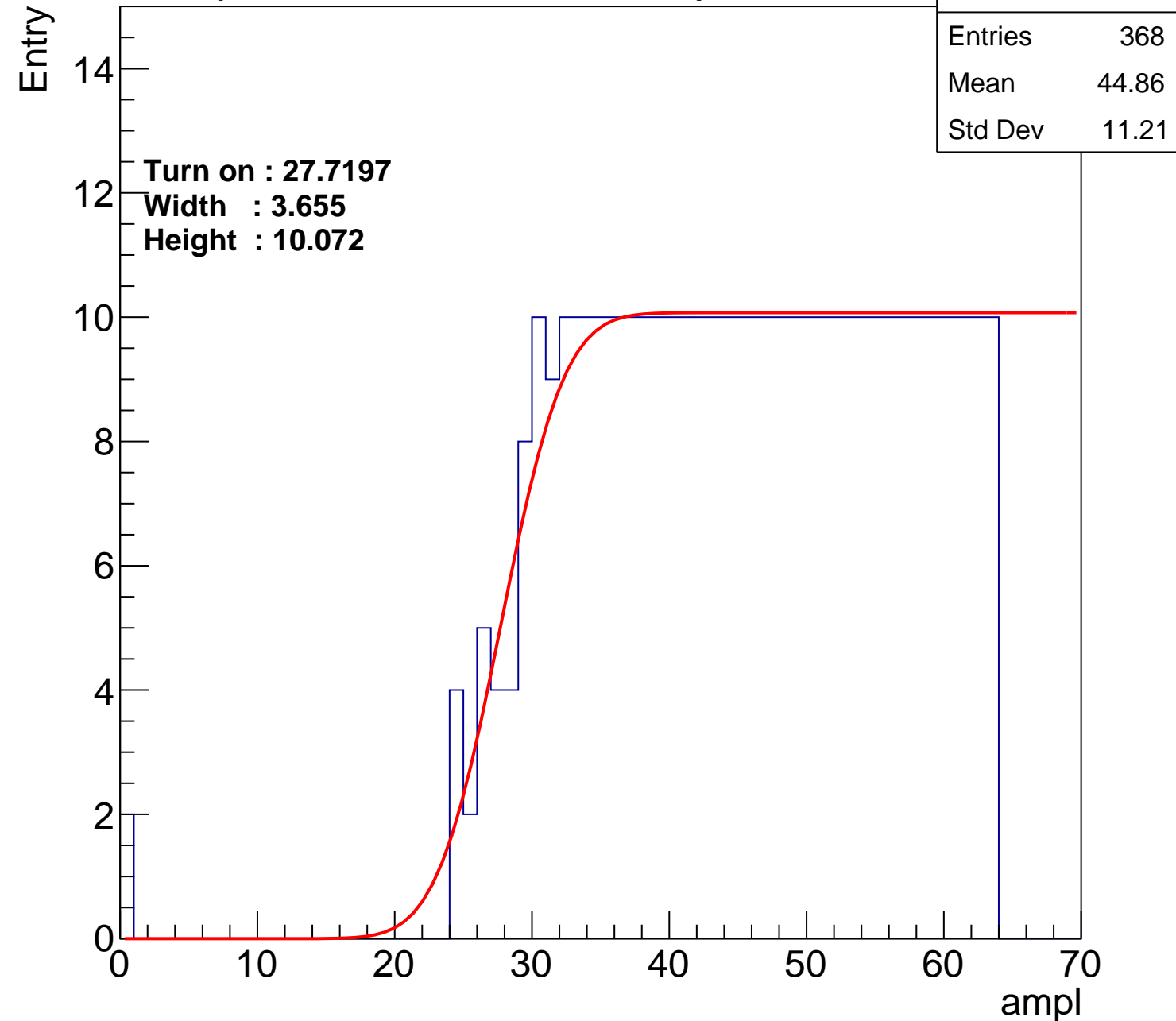
Width : 3.655

Height : 10.072

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch85

calib_packv5_042523_0143.root, FC#4, port A2

Entries	366
Mean	45.01
Std Dev	10.98

Turn on : 28.3819

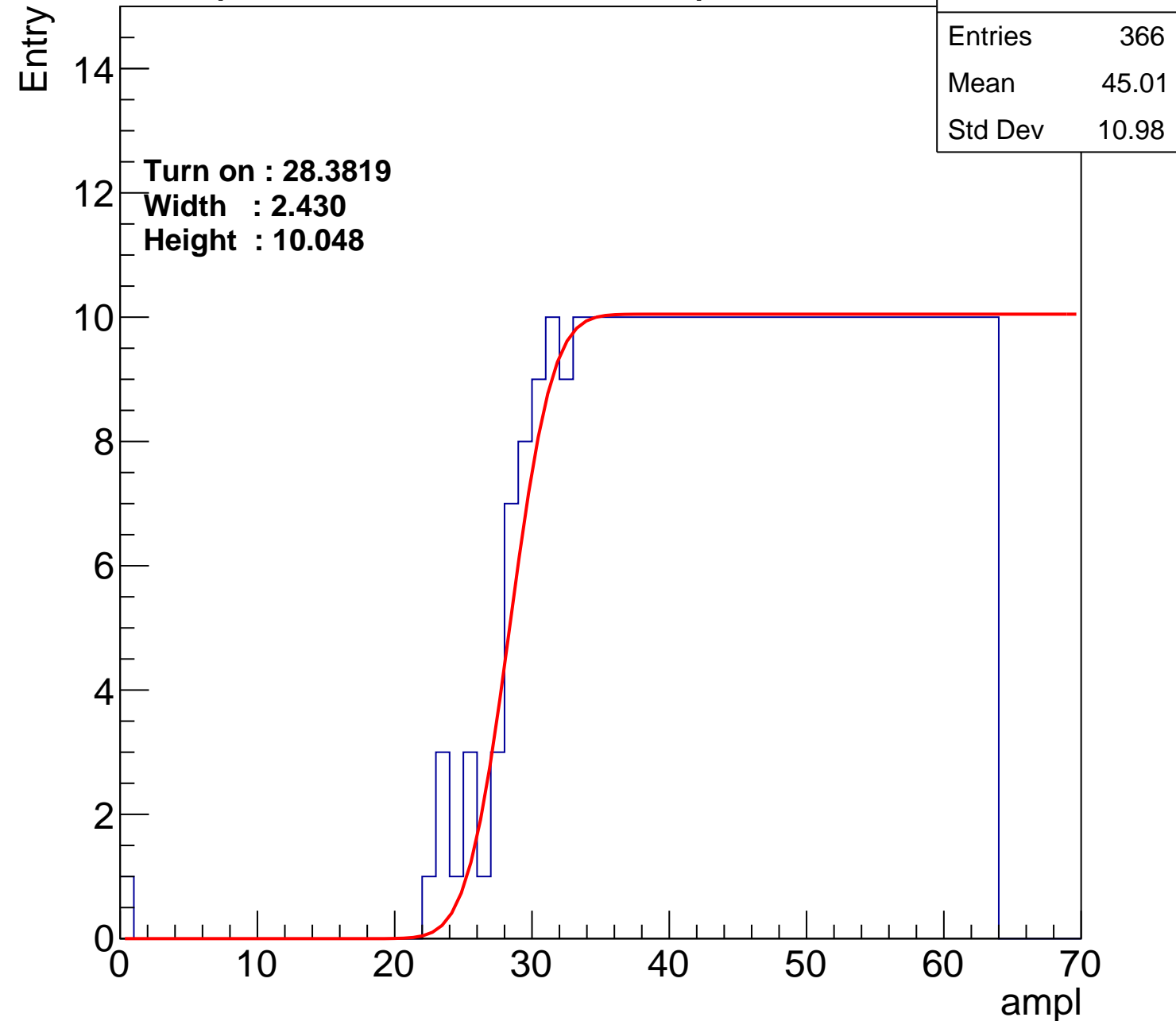
Width : 2.430

Height : 10.048

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch86

calib_packv5_042523_0143.root, FC#4, port A2

Entries	369
Mean	44.81
Std Dev	11.22

Turn on : 27.4128

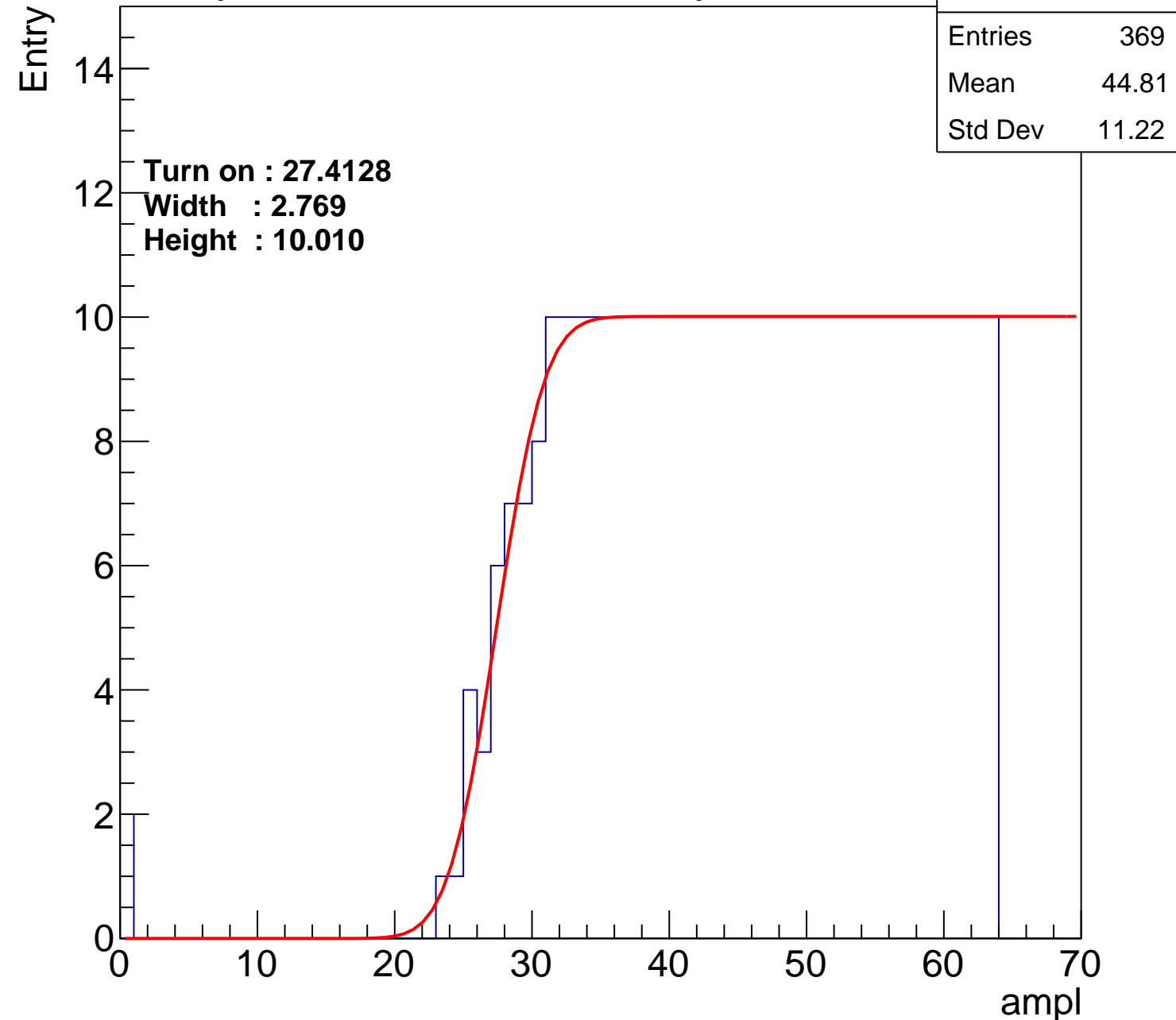
Width : 2.769

Height : 10.010

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch87

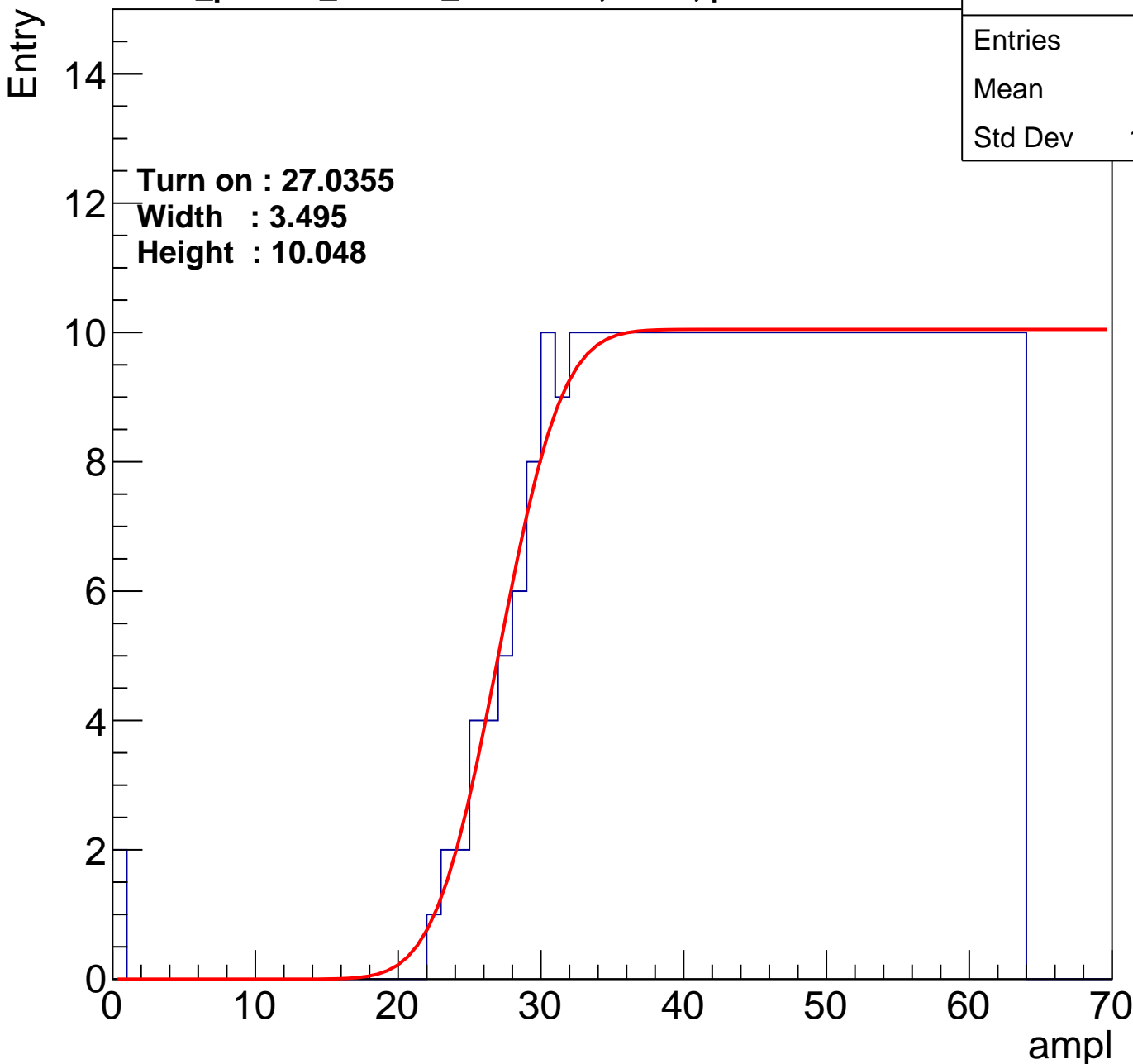
calib_packv5_042523_0143.root, FC#4, port A2

Entries	373
Mean	44.6
Std Dev	11.36

Turn on : 27.0355

Width : 3.495

Height : 10.048



B1L100S, U4-ch88

calib_packv5_042523_0143.root, FC#4, port A2

Entries	384
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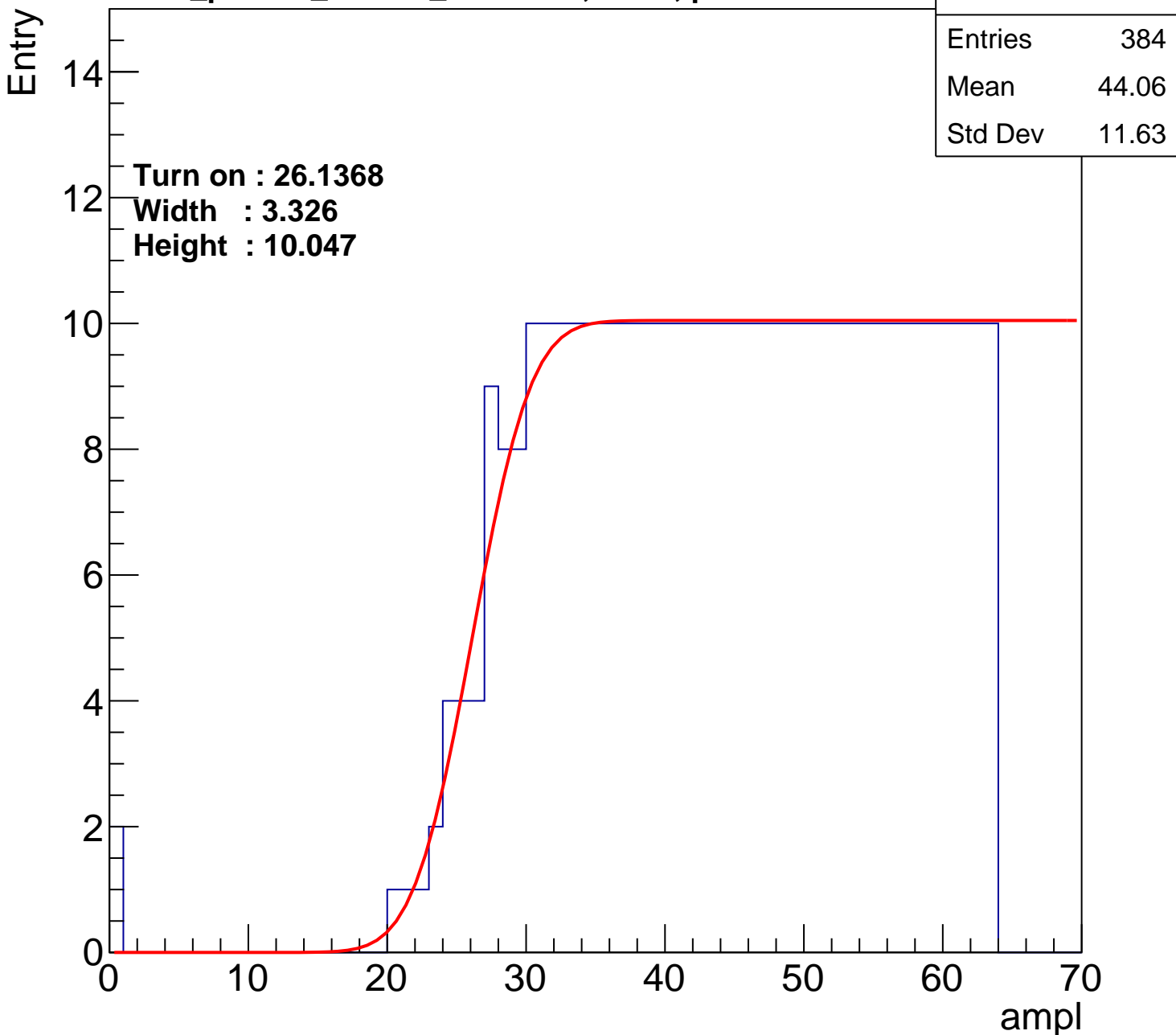
Mean	44.06
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Std Dev	11.63
---------	-------

Turn on : 26.1368

Width : 3.326

Height : 10.047



B1L100S, U4-ch89

calib_packv5_042523_0143.root, FC#4, port A2

Entries	374
Mean	44.59
Std Dev	11.3

Turn on : 27.0699

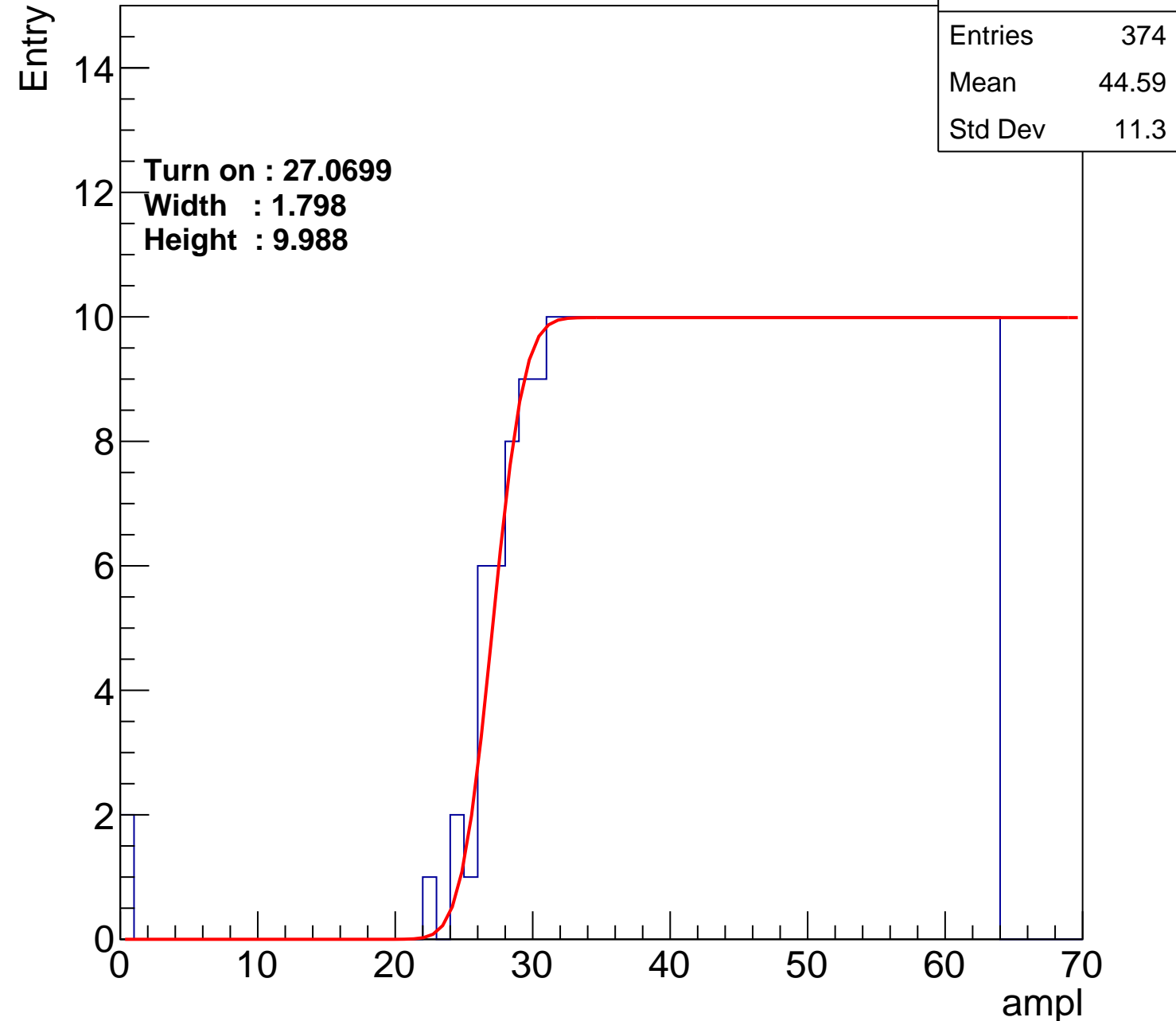
Width : 1.798

Height : 9.988

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch90

calib_packv5_042523_0143.root, FC#4, port A2

Entries	371
Mean	44.65
Std Dev	11.38

Turn on : 27.6018

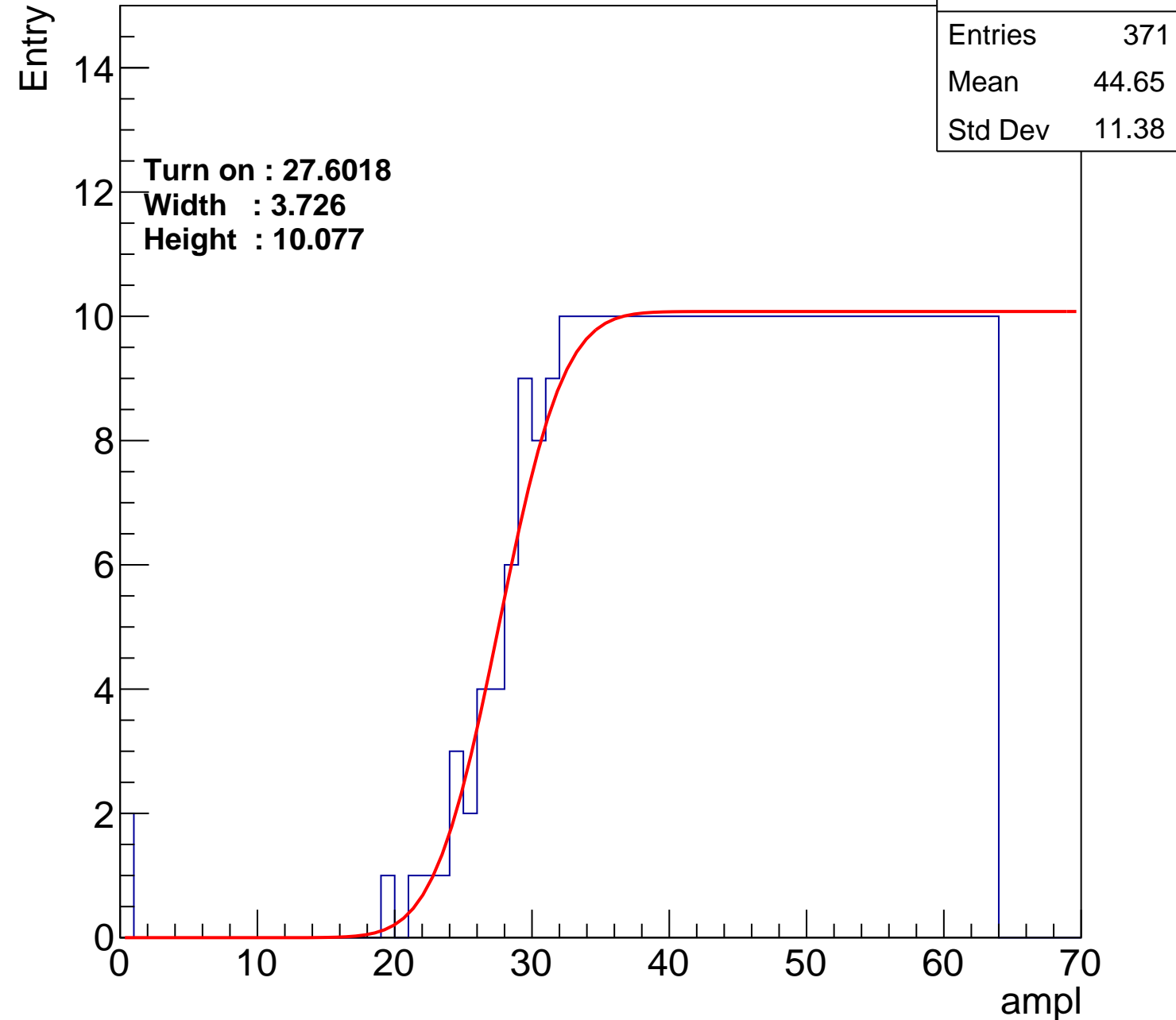
Width : 3.726

Height : 10.077

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch91

calib_packv5_042523_0143.root, FC#4, port A2

Entries	378
Mean	44.22
Std Dev	11.83

Turn on : 26.7500

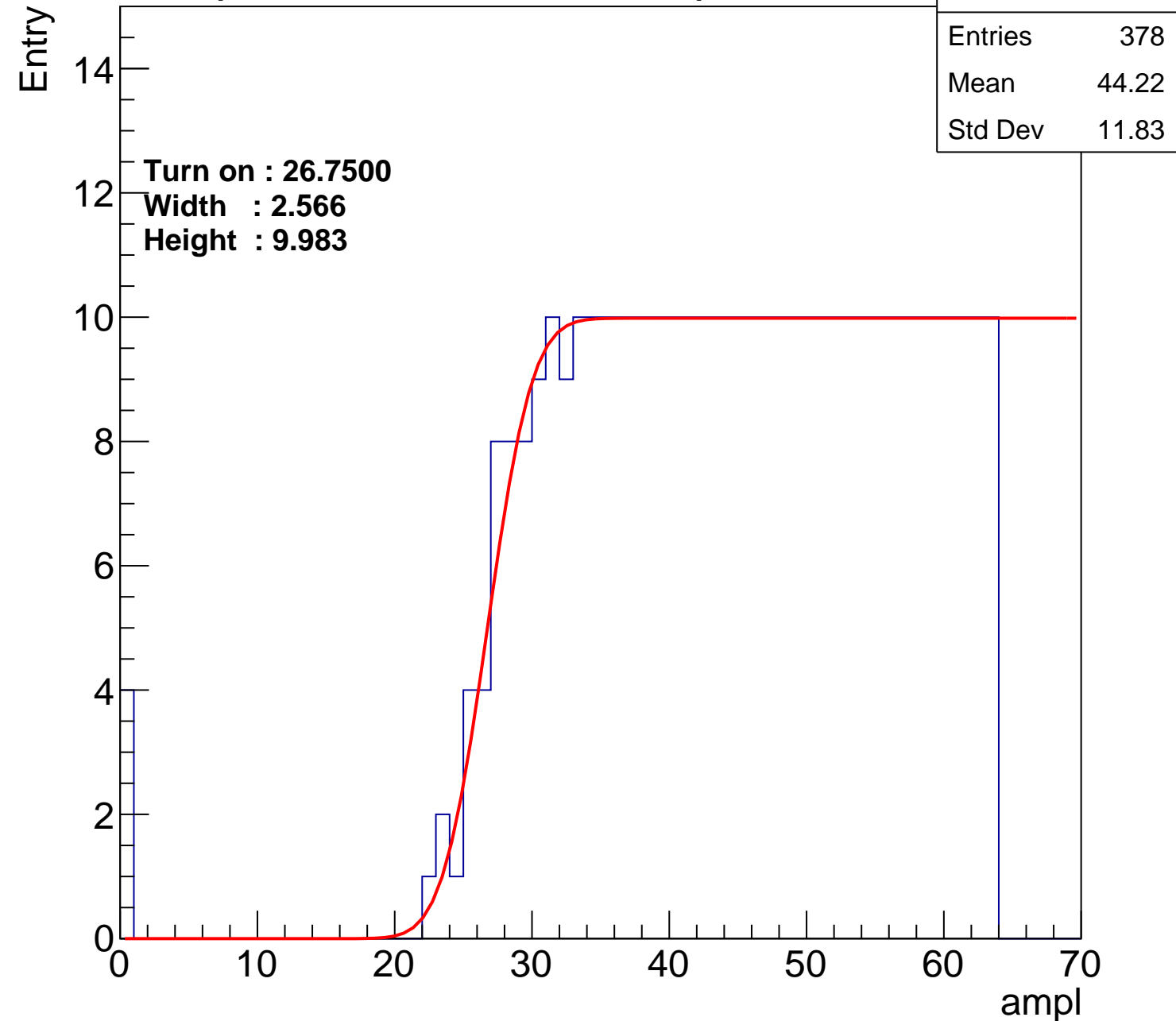
Width : 2.566

Height : 9.983

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch92

calib_packv5_042523_0143.root, FC#4, port A2

Entries	374
Mean	44.4
Std Dev	11.76

Turn on : 27.1587

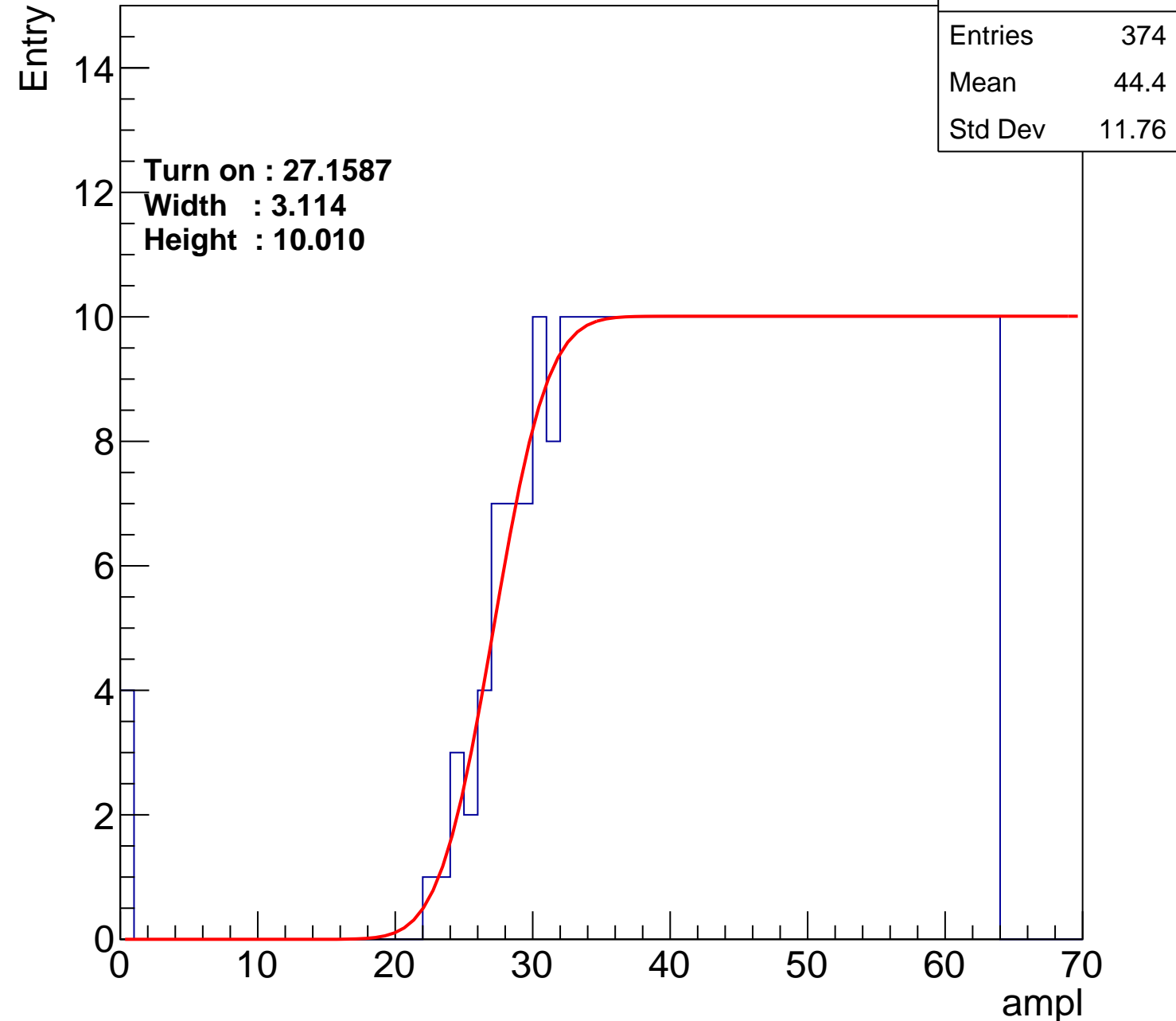
Width : 3.114

Height : 10.010

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch93

calib_packv5_042523_0143.root, FC#4, port A2

Entries	407
Mean	42.95
Std Dev	12.19

Turn on : 23.7618

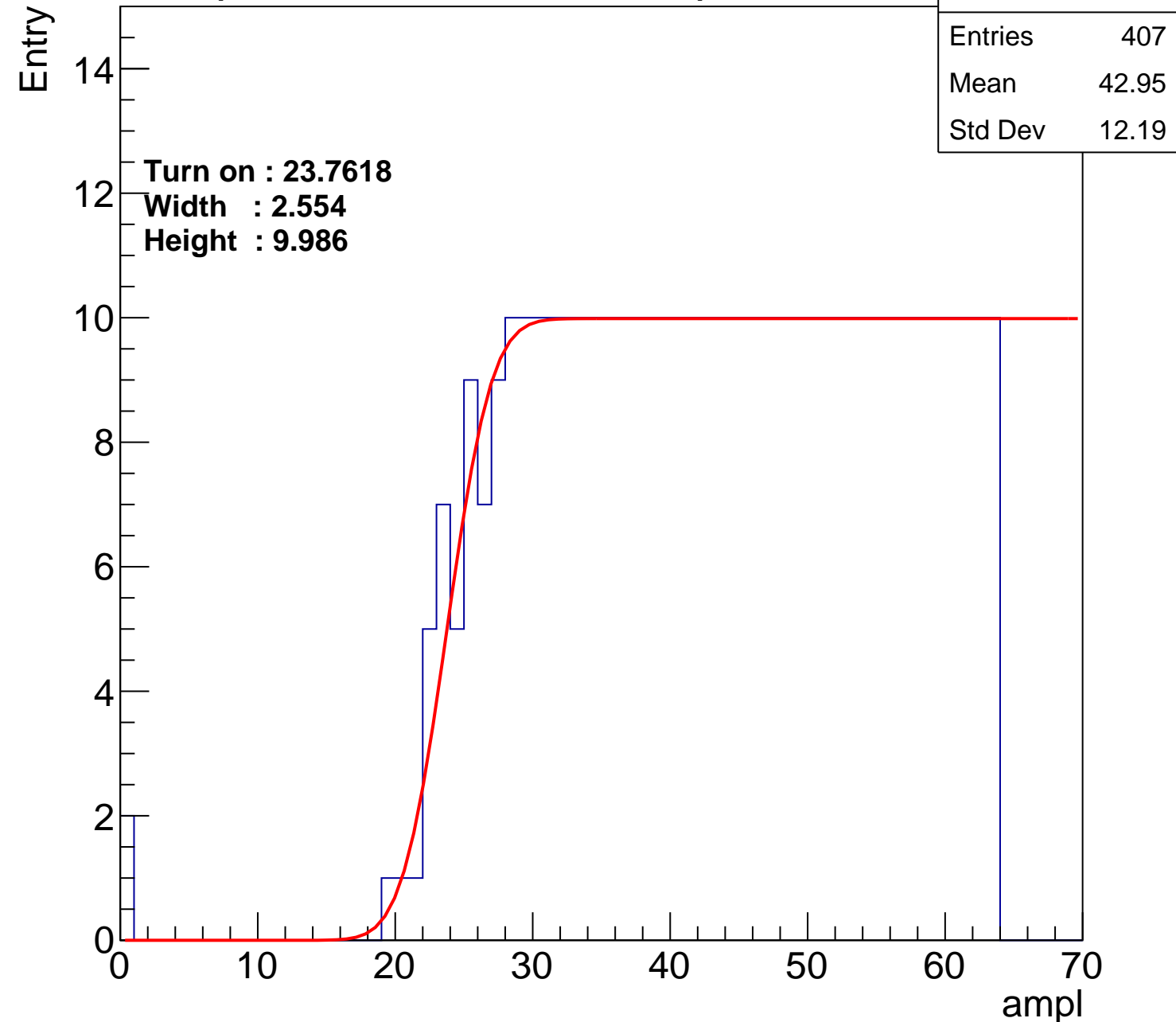
Width : 2.554

Height : 9.986

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch94

calib_packv5_042523_0143.root, FC#4, port A2

Entries	363
Mean	45.08
Std Dev	11.11

Turn on : 27.9852

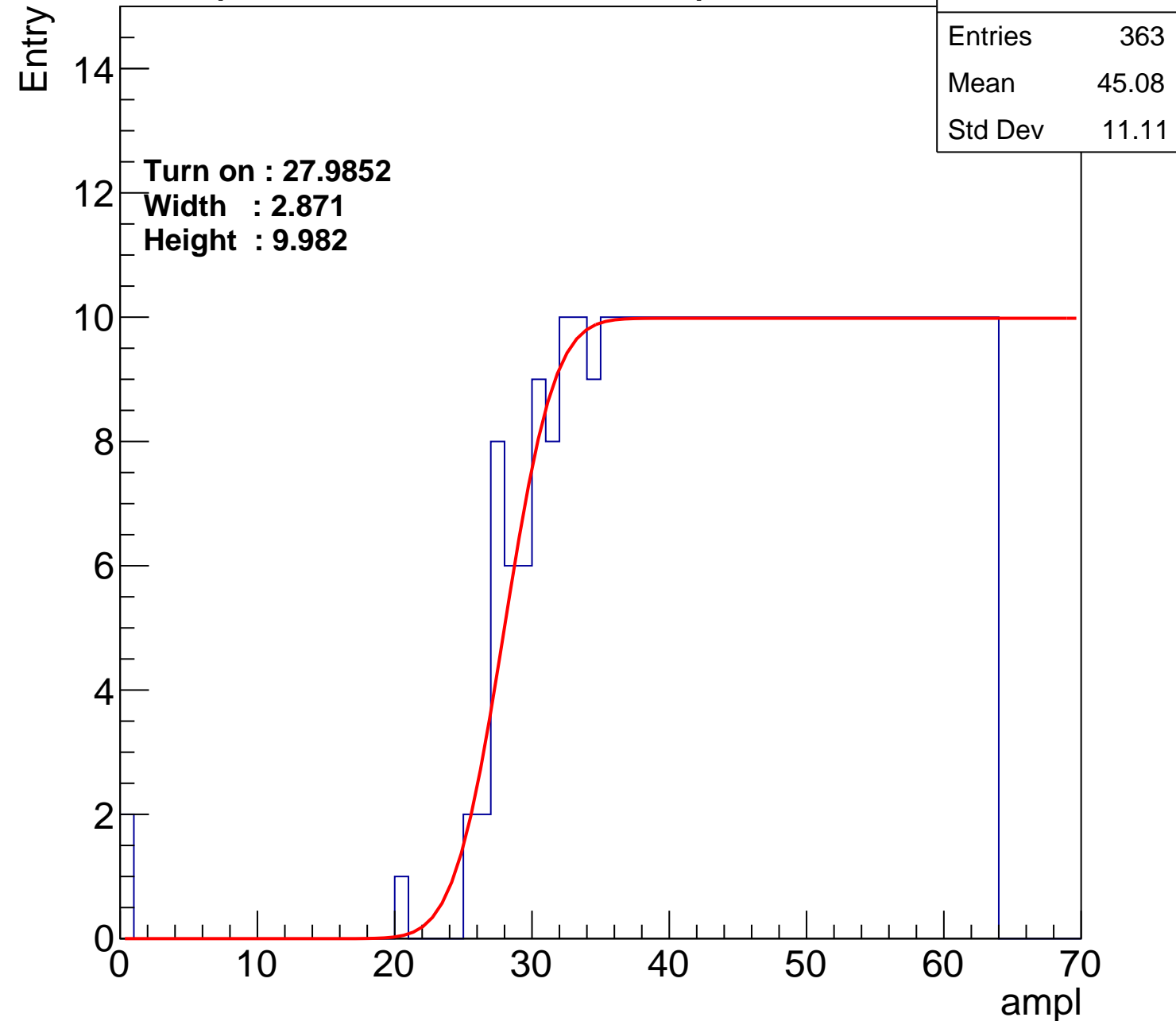
Width : 2.871

Height : 9.982

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch95

calib_packv5_042523_0143.root, FC#4, port A2

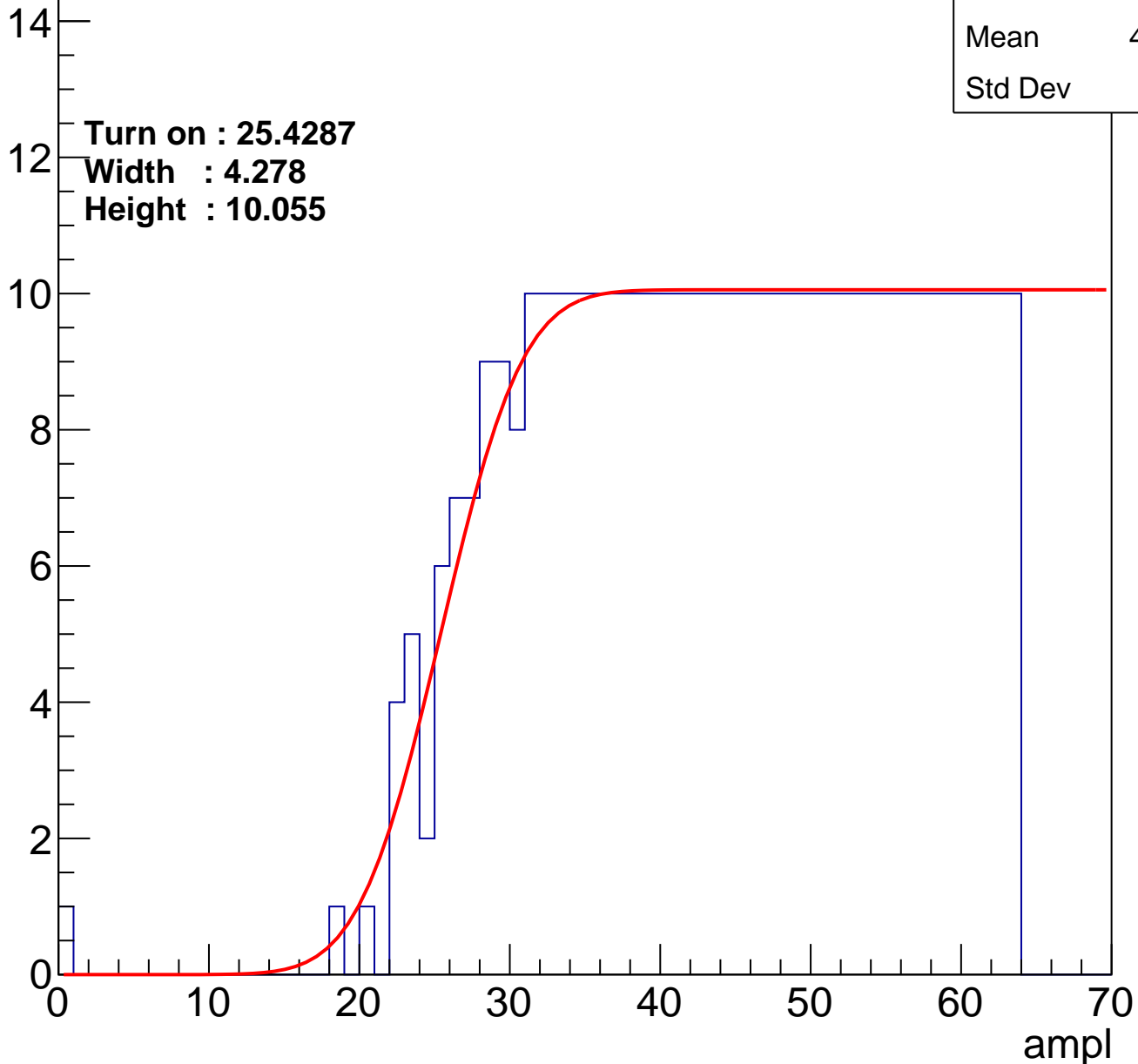
Entries	390
Mean	43.78
Std Dev	11.7

Turn on : 25.4287

Width : 4.278

Height : 10.055

Entry



B1L100S, U4-ch96

calib_packv5_042523_0143.root, FC#4, port A2

Entries	378
Mean	44.43
Std Dev	11.28

Turn on : 27.0113

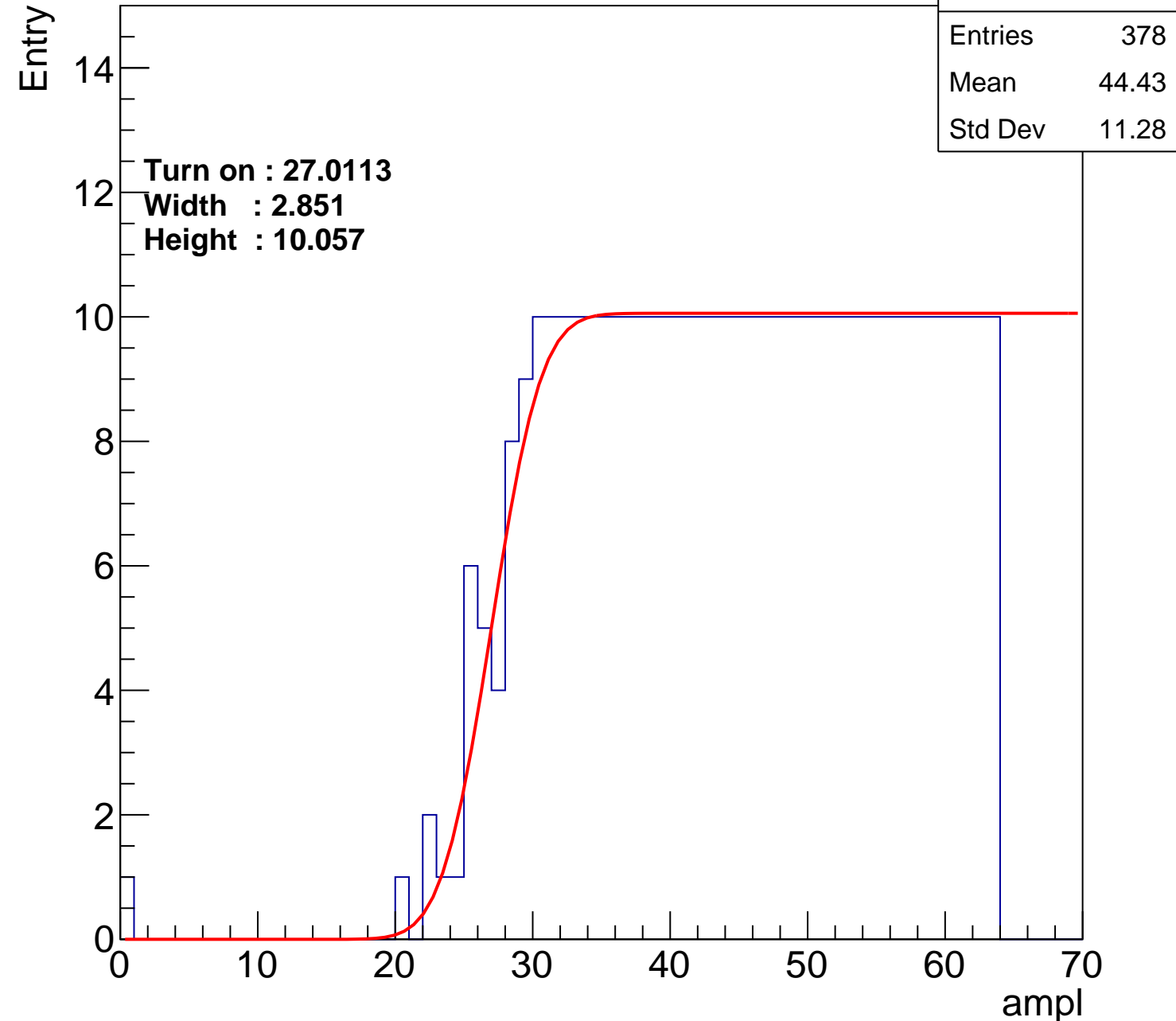
Width : 2.851

Height : 10.057

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch97

calib_packv5_042523_0143.root, FC#4, port A2

Entries	369
Mean	44.84
Std Dev	11.18

Turn on : 27.5464

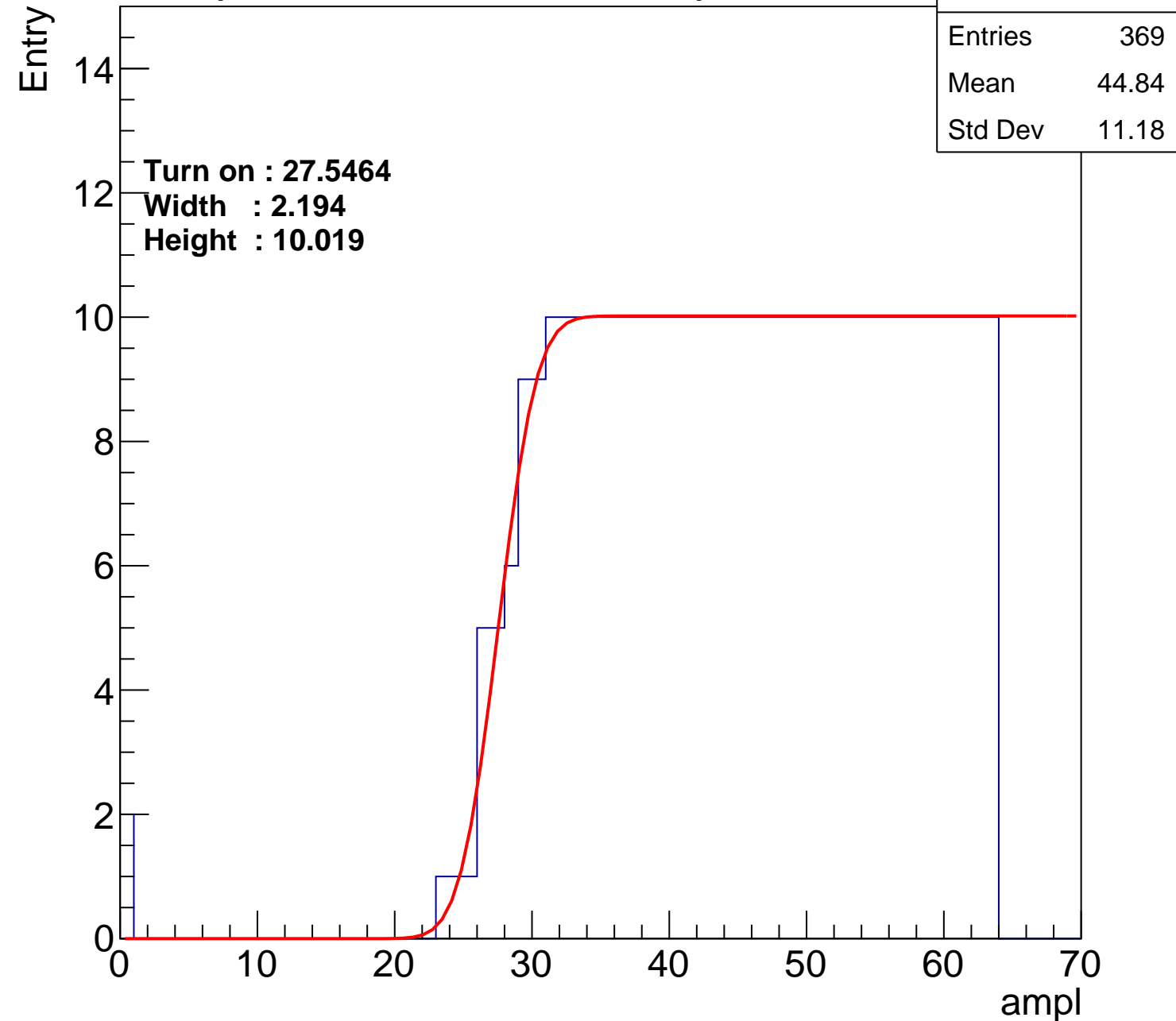
Width : 2.194

Height : 10.019

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch98

calib_packv5_042523_0143.root, FC#4, port A2

Entries	387
Mean	43.83
Std Dev	11.9

Turn on : 25.8855

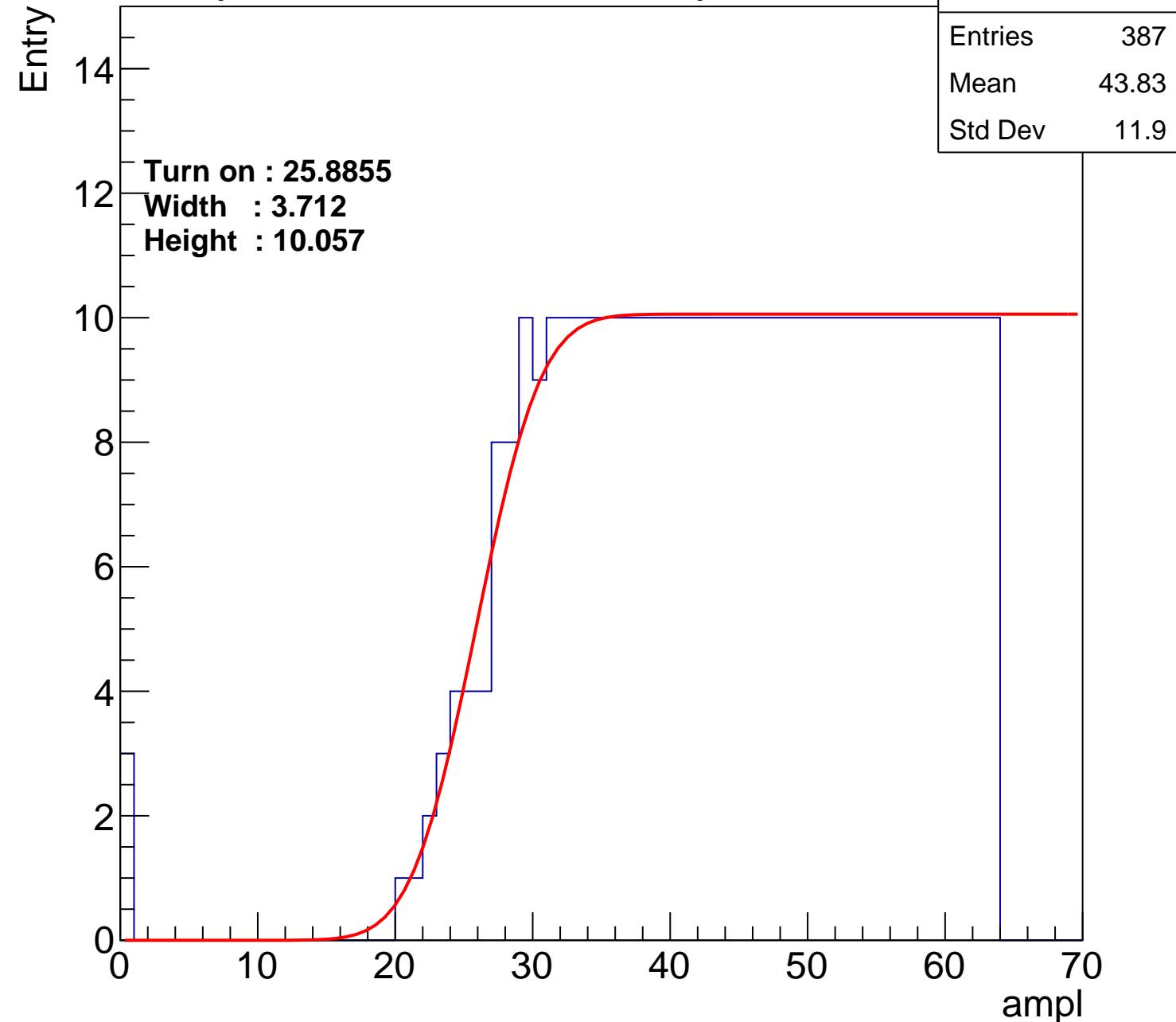
Width : 3.712

Height : 10.057

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch99

calib_packv5_042523_0143.root, FC#4, port A2

Entries	380
Mean	44.25
Std Dev	11.53

Turn on : 26.7678

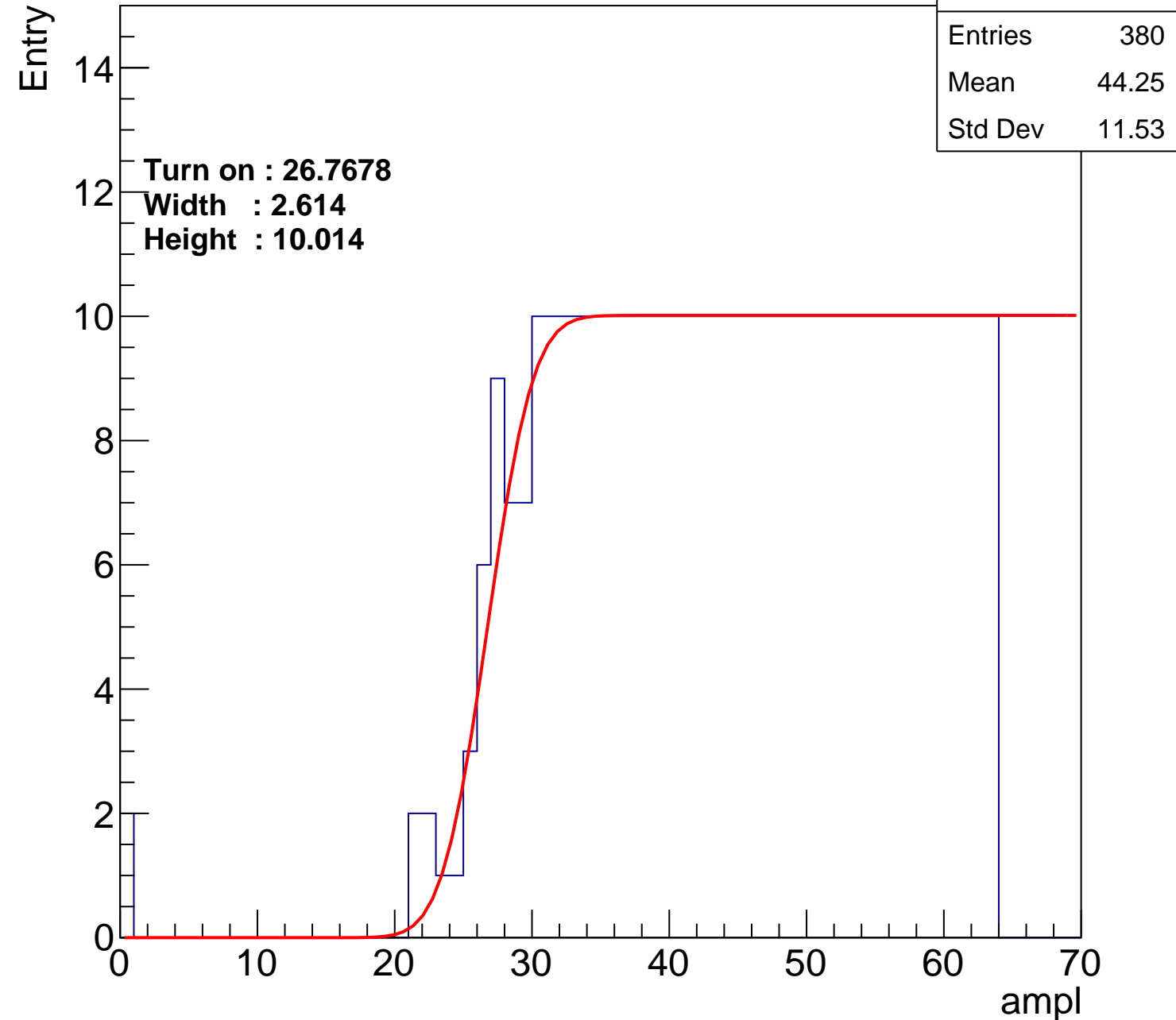
Width : 2.614

Height : 10.014

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch100

calib_packv5_042523_0143.root, FC#4, port A2

Entries	369
Mean	44.85
Std Dev	11.08

Turn on : 27.6310

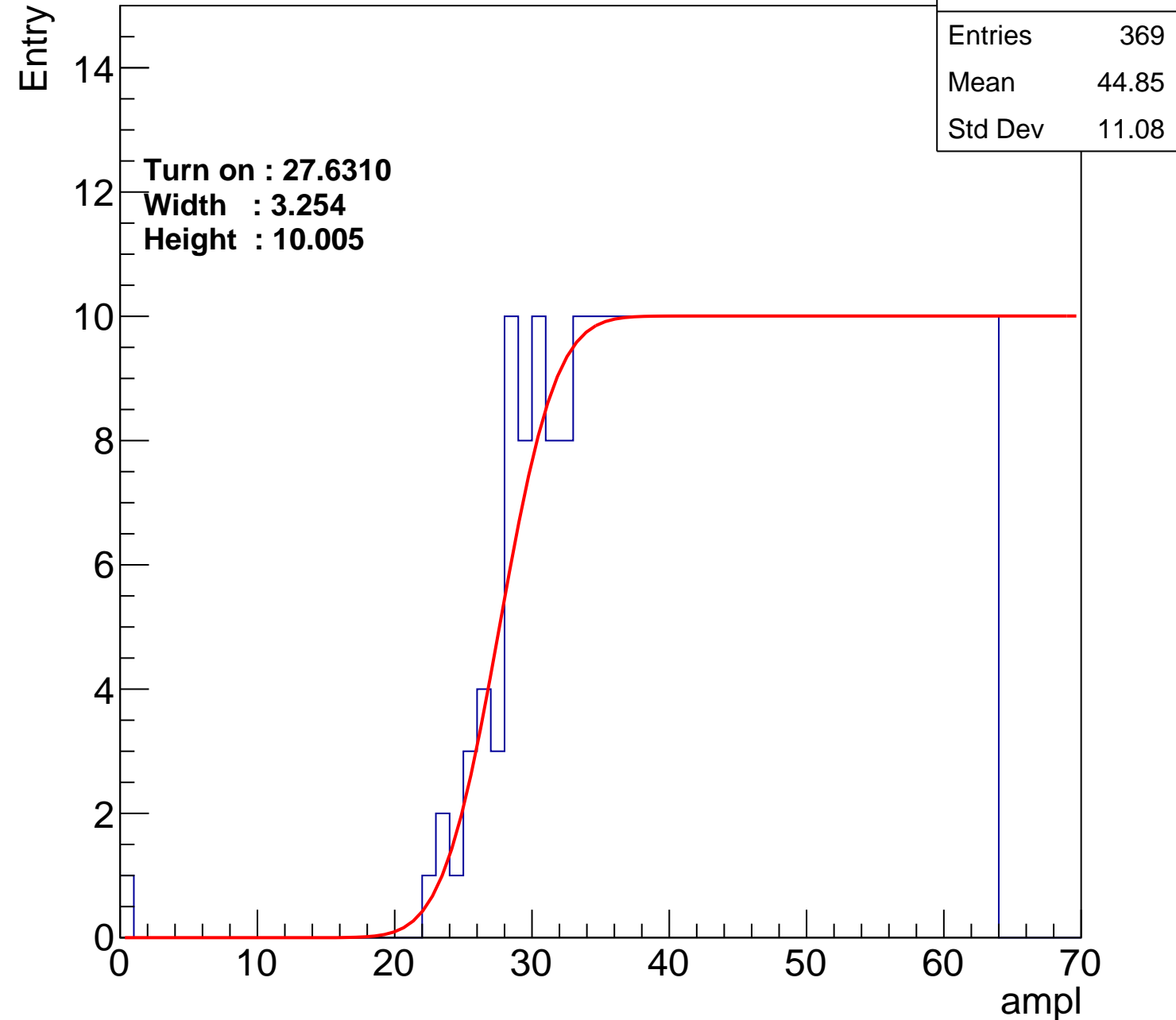
Width : 3.254

Height : 10.005

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch101

calib_packv5_042523_0143.root, FC#4, port A2

Entries	372
Mean	44.64
Std Dev	11.33

Turn on : 27.3235

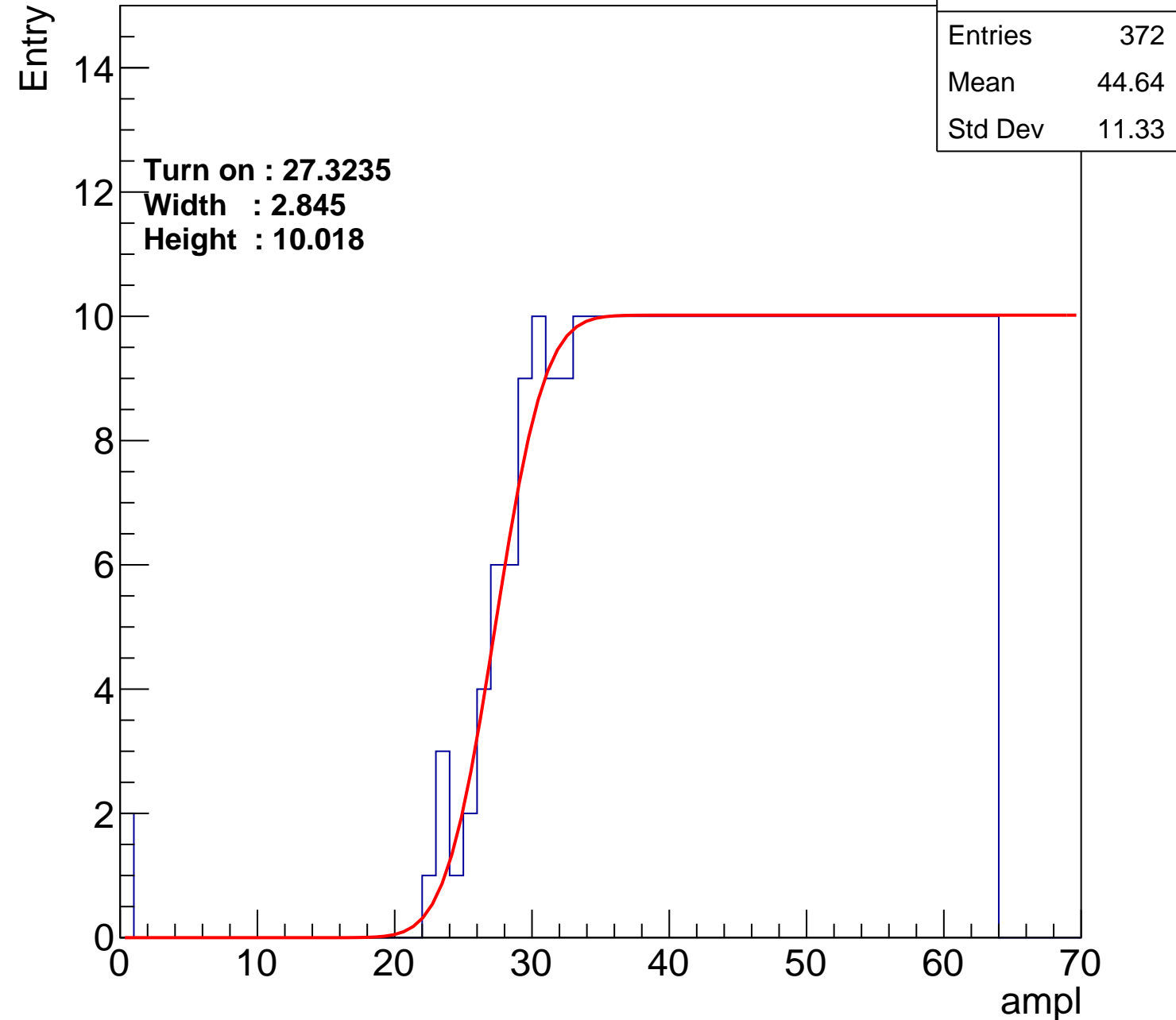
Width : 2.845

Height : 10.018

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch102

calib_packv5_042523_0143.root, FC#4, port A2

Entries	383
Mean	43.99
Std Dev	11.86

Turn on : 26.2276

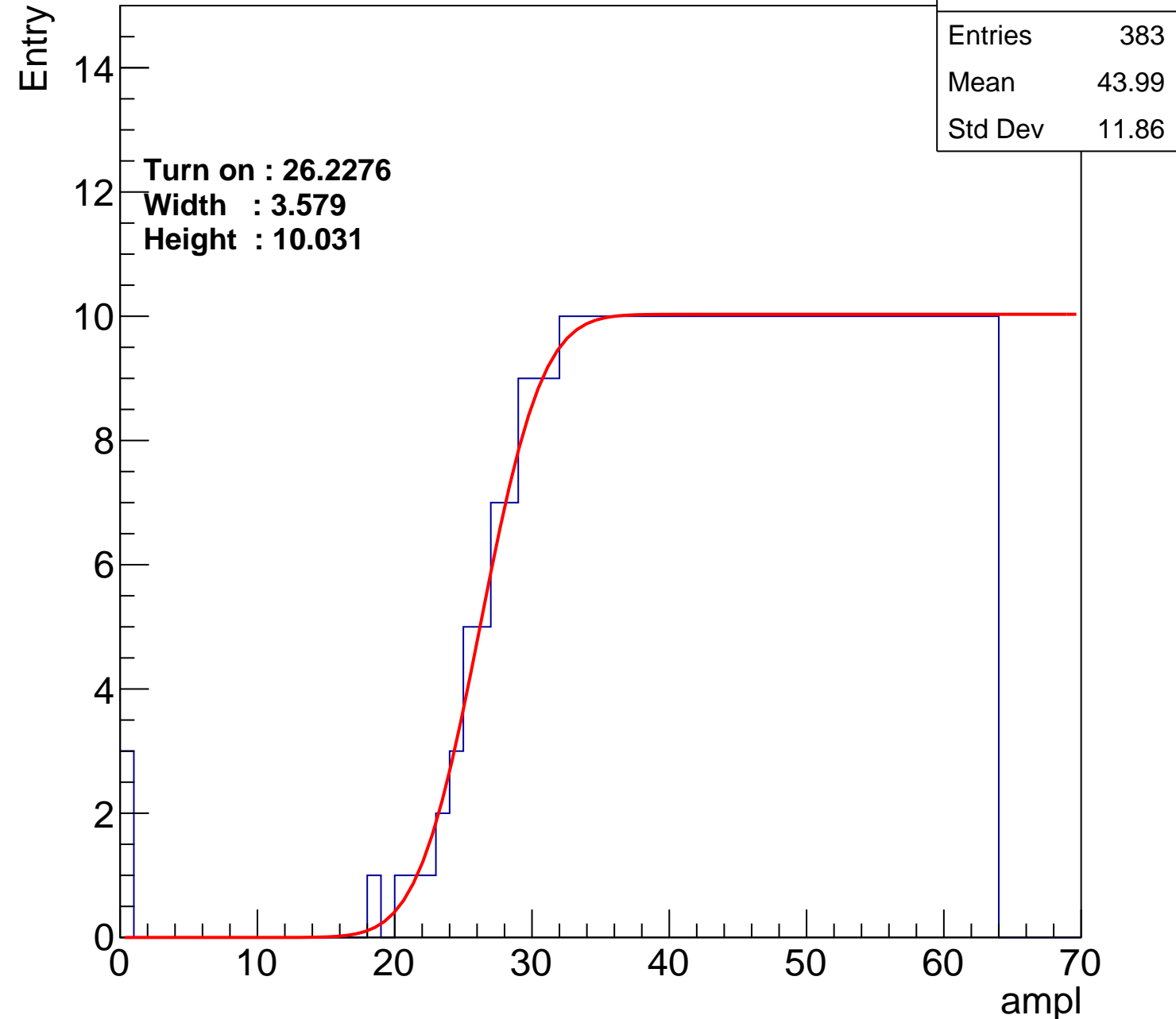
Width : 3.579

Height : 10.031

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch103

calib_packv5_042523_0143.root, FC#4, port A2

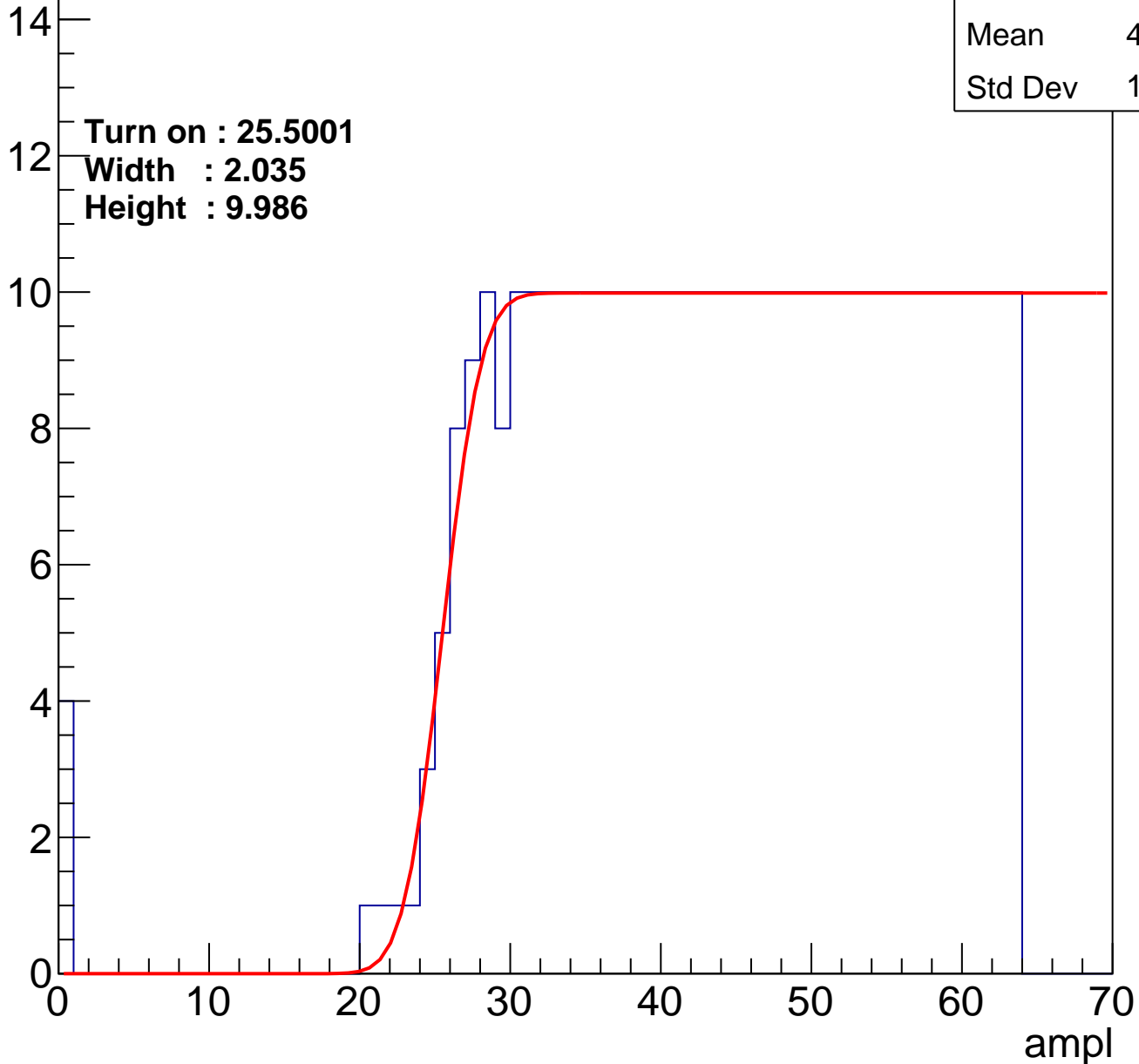
Entries	391
Mean	43.62
Std Dev	12.09

Turn on : 25.5001

Width : 2.035

Height : 9.986

Entry



B1L100S, U4-ch104

calib_packv5_042523_0143.root, FC#4, port A2

Entries	390
Mean	43.51
Std Dev	12.37

Turn on : 25.9890

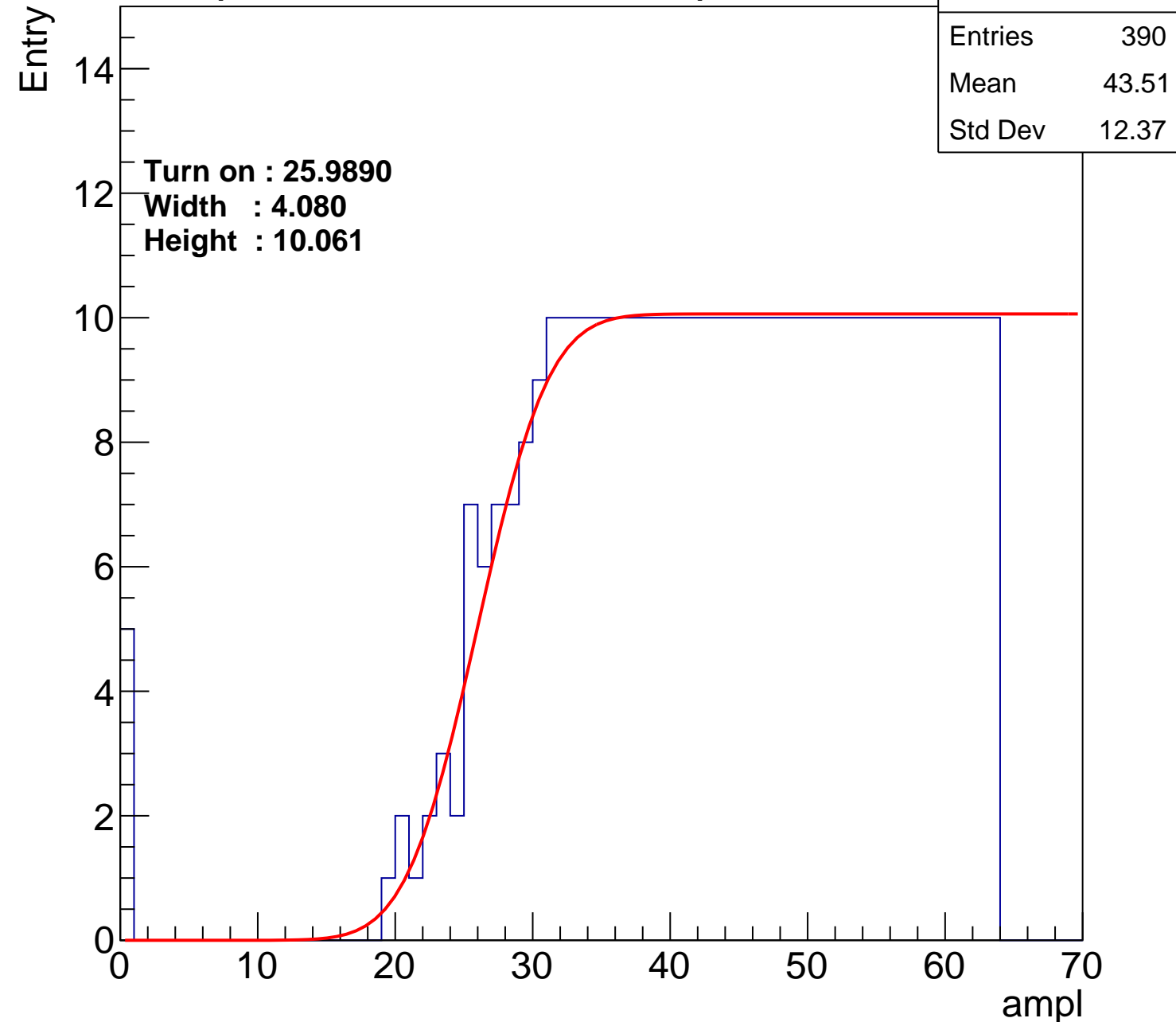
Width : 4.080

Height : 10.061

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch105

calib_packv5_042523_0143.root, FC#4, port A2

Entries	380
Mean	44.11
Std Dev	11.91

Turn on : 26.6696

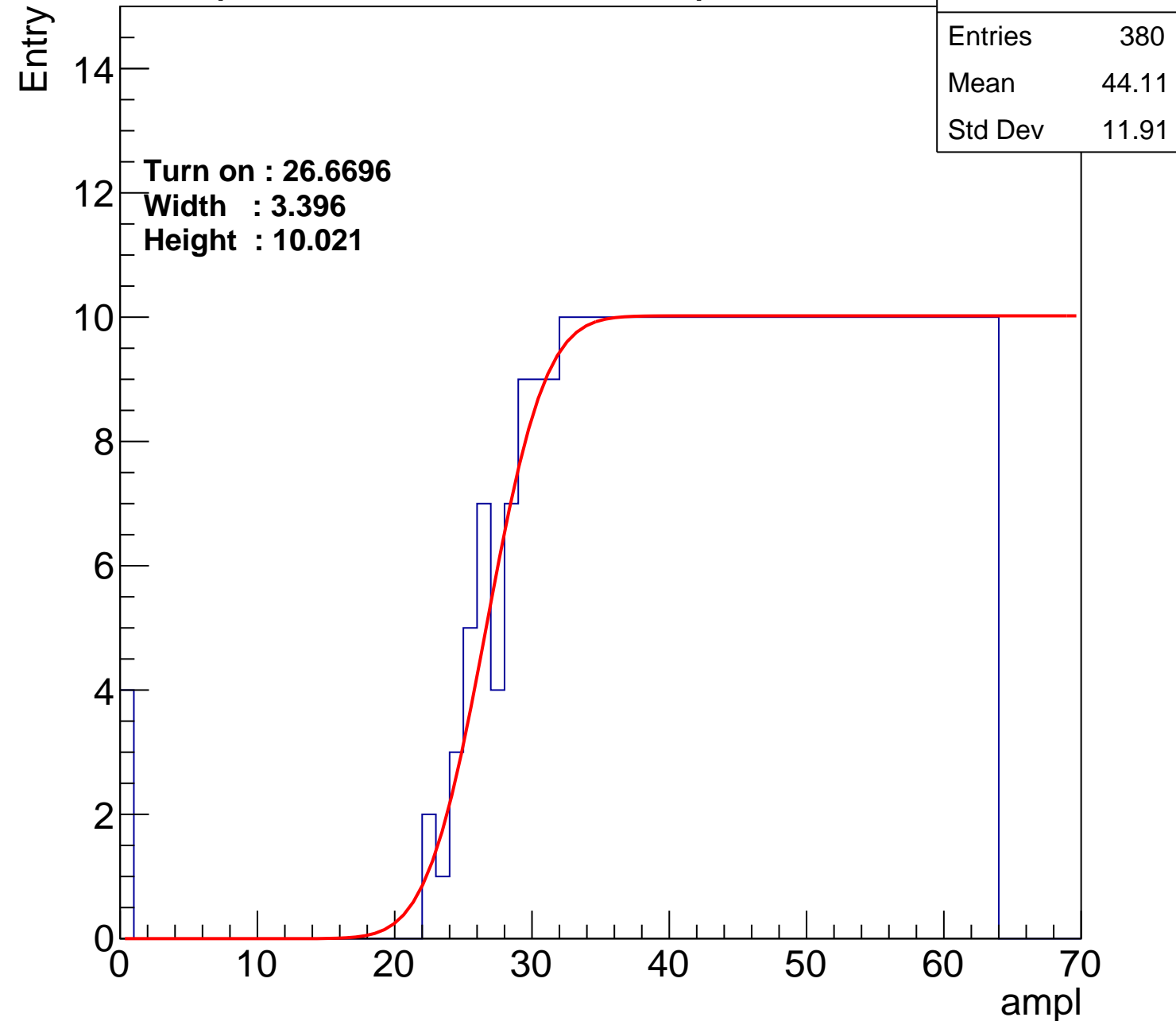
Width : 3.396

Height : 10.021

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch106

calib_packv5_042523_0143.root, FC#4, port A2

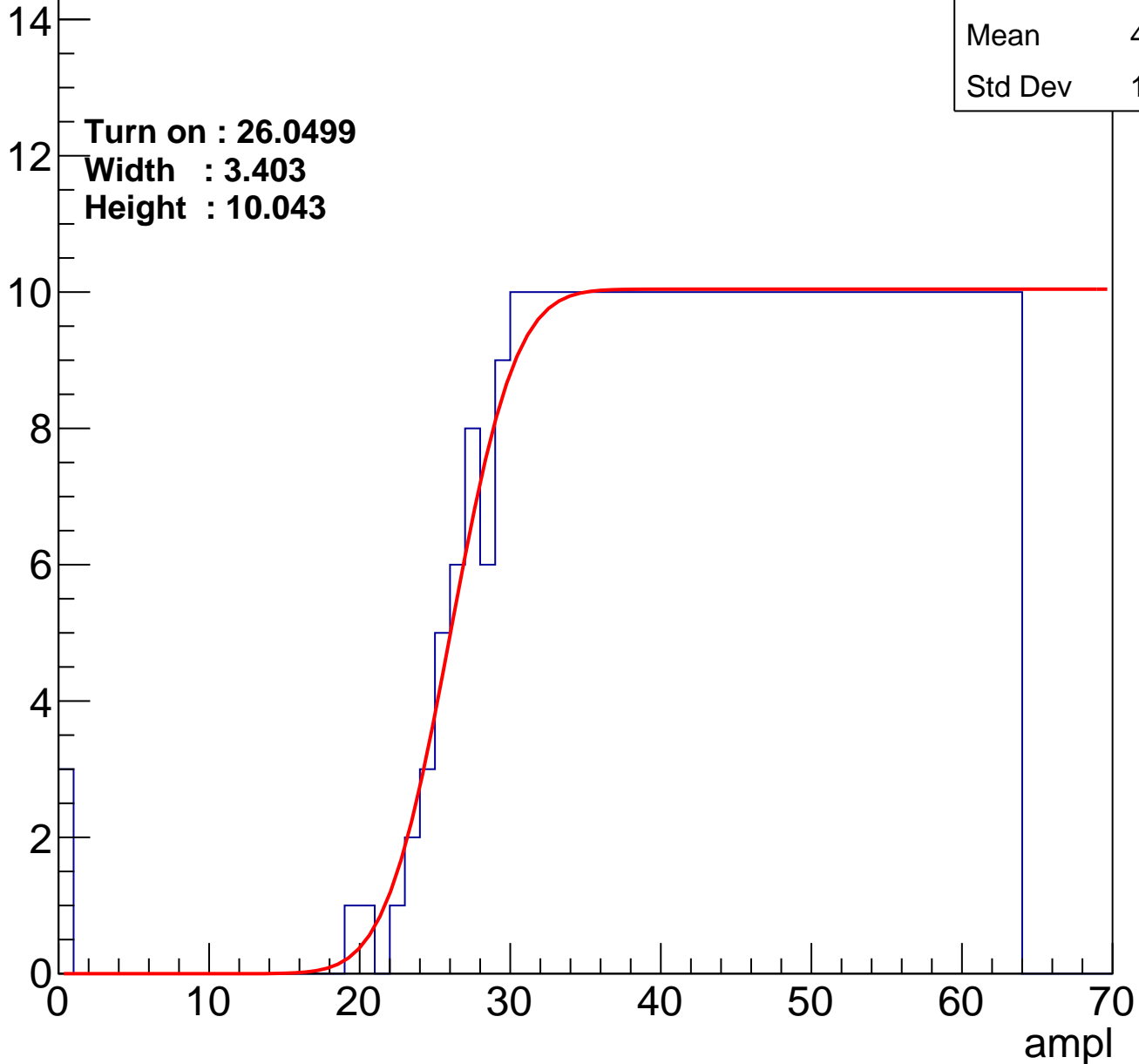
Entries	385
Mean	43.94
Std Dev	11.85

Turn on : 26.0499

Width : 3.403

Height : 10.043

Entry



B1L100S, U4-ch107

calib_packv5_042523_0143.root, FC#4, port A2

Entries	375
Mean	44.37
Std Dev	11.68

Turn on : 27.2432

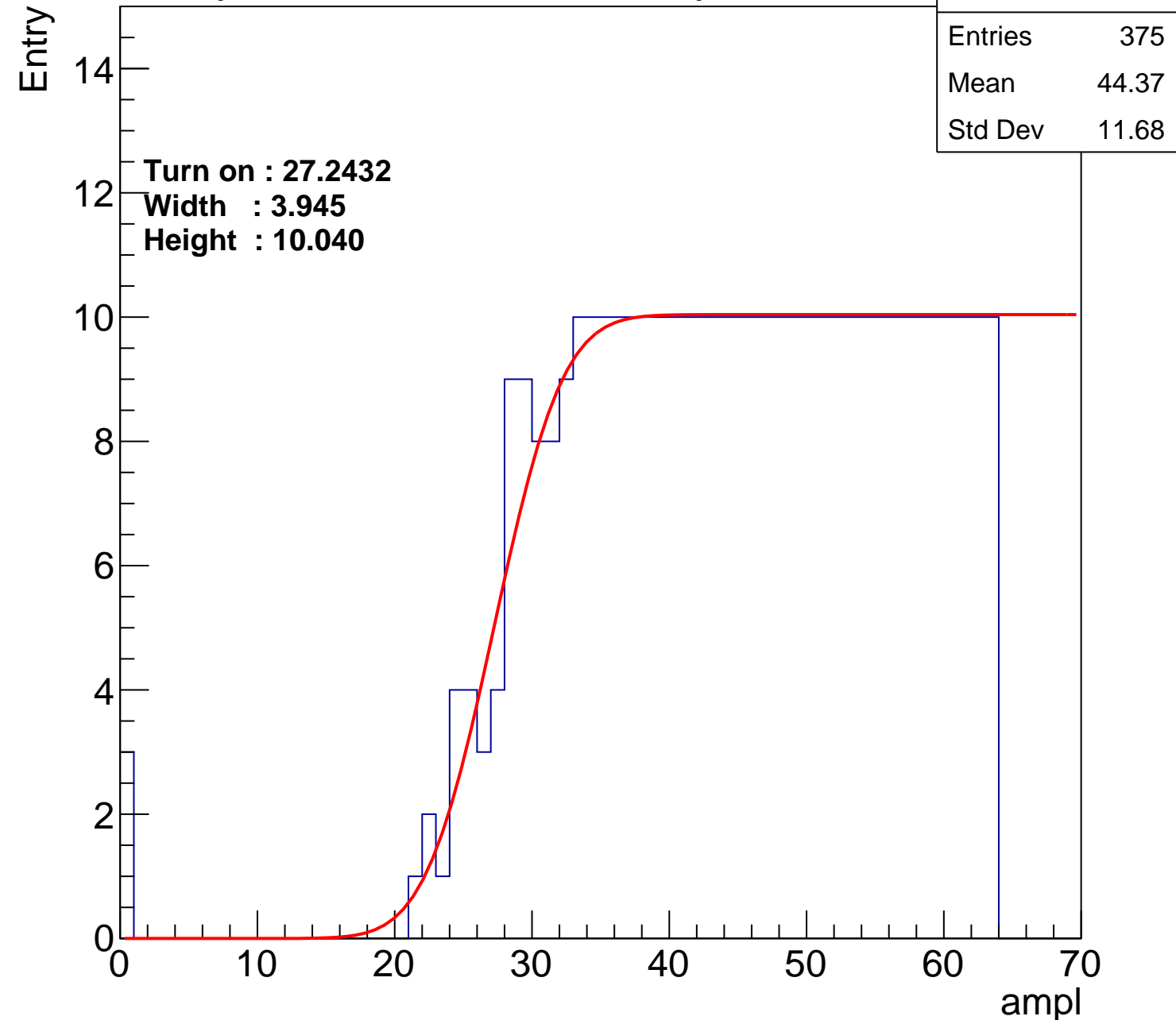
Width : 3.945

Height : 10.040

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch108

calib_packv5_042523_0143.root, FC#4, port A2

Entries	385
Mean	43.94
Std Dev	11.77

Turn on : 26.5620

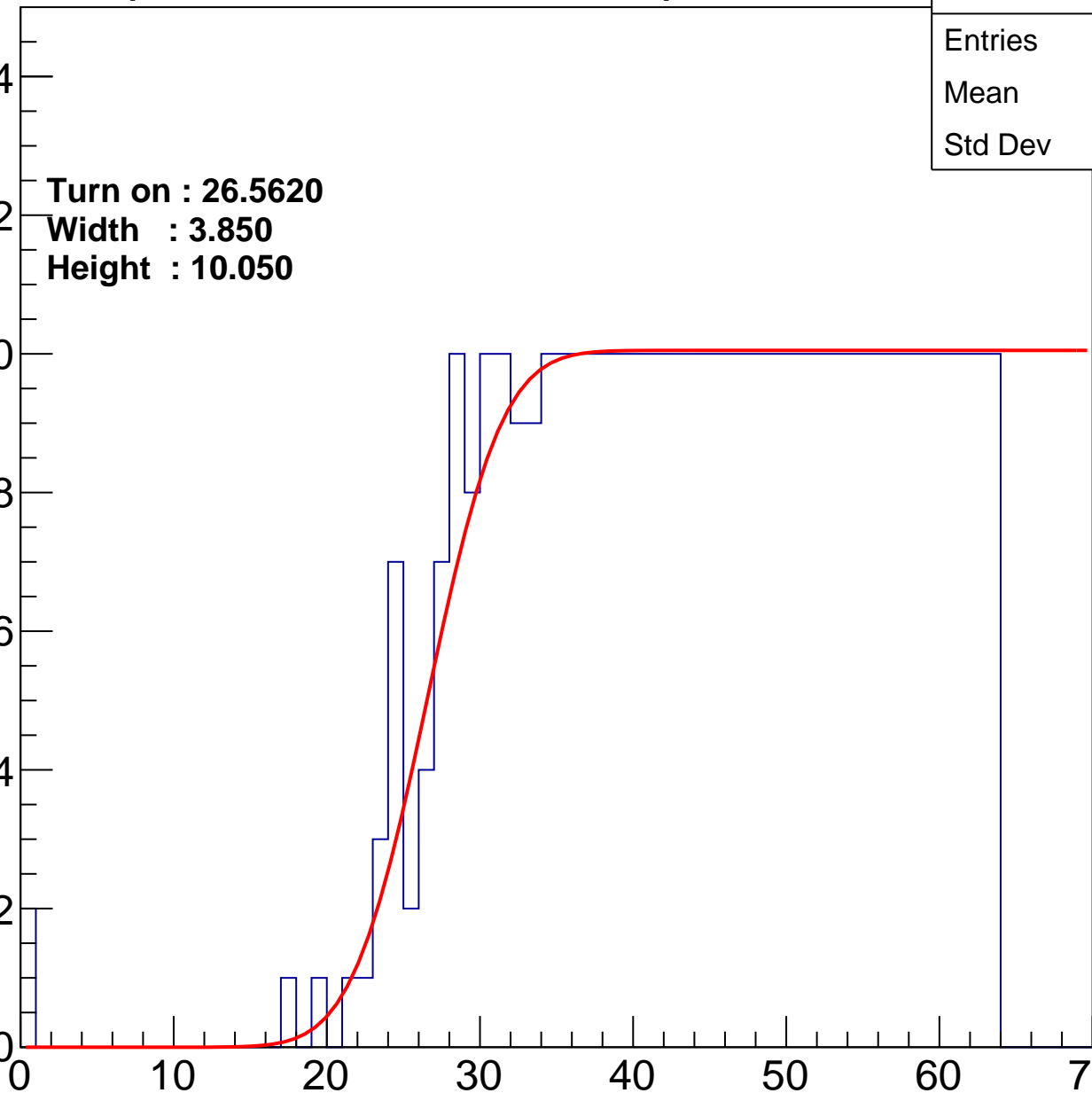
Width : 3.850

Height : 10.050

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch109

calib_packv5_042523_0143.root, FC#4, port A2

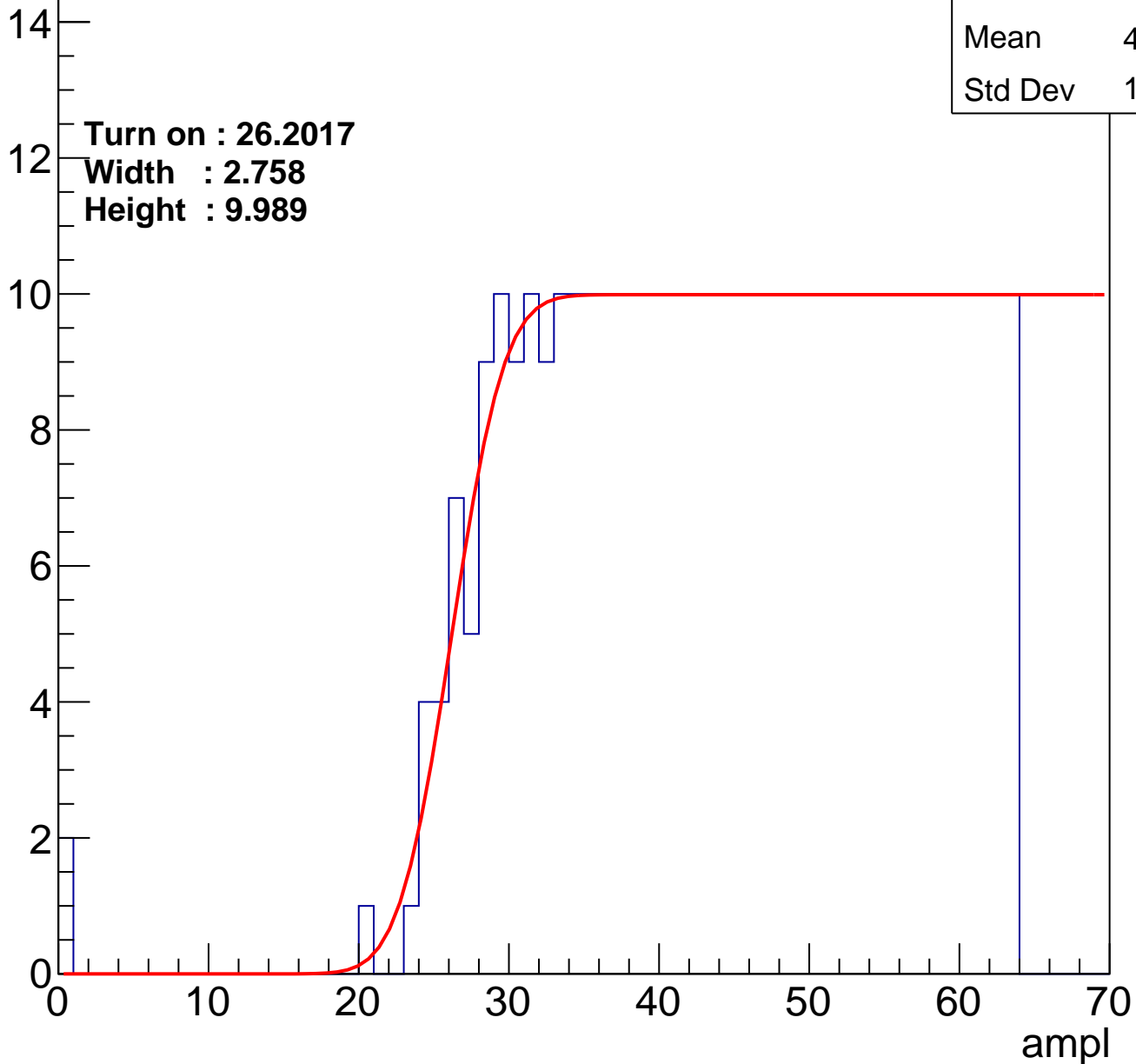
Entries	381
Mean	44.22
Std Dev	11.53

Turn on : 26.2017

Width : 2.758

Height : 9.989

Entry



B1L100S, U4-ch110

calib_packv5_042523_0143.root, FC#4, port A2

Entries	385
Mean	43.99
Std Dev	11.68

Turn on : 25.5500

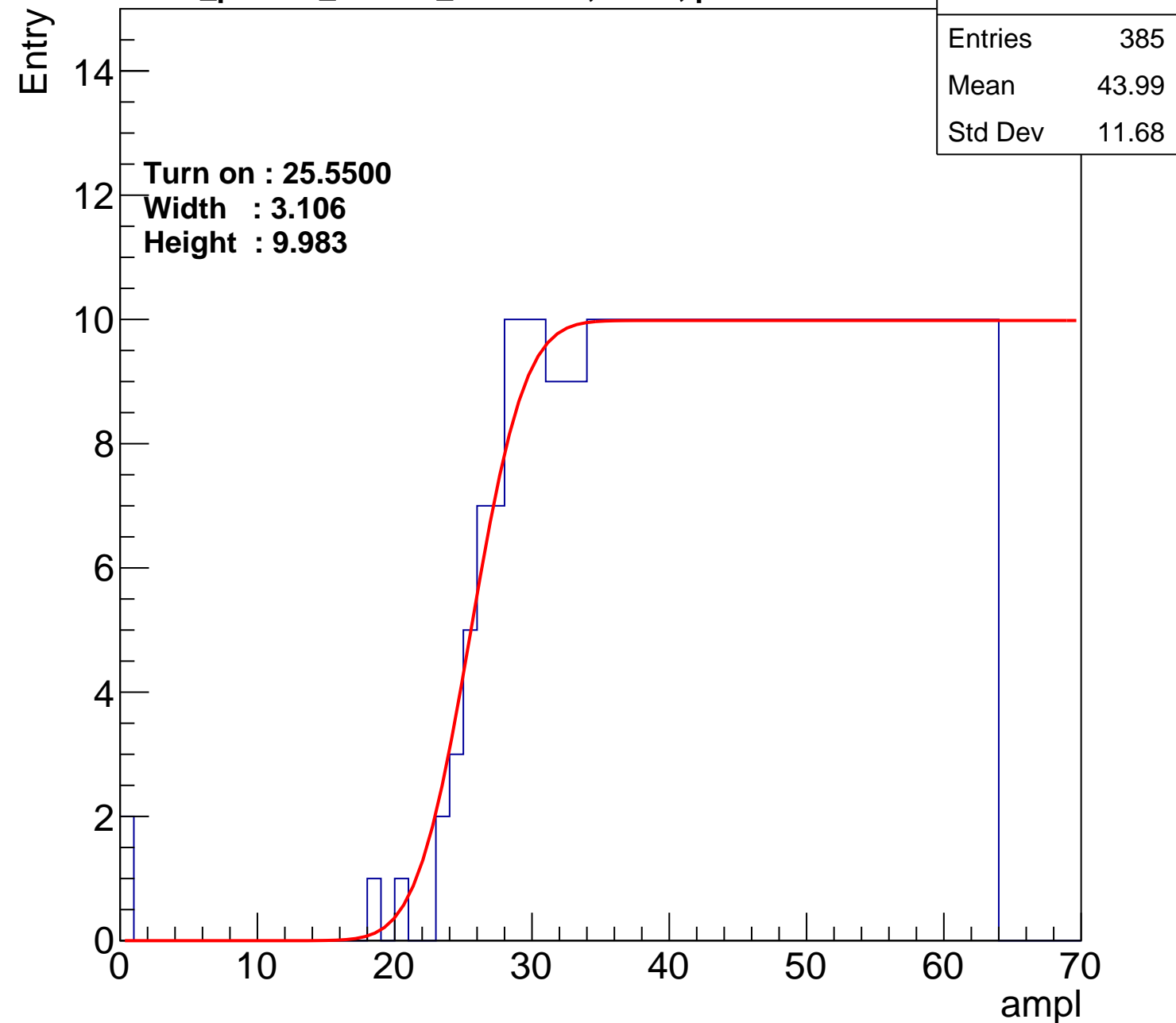
Width : 3.106

Height : 9.983

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch111

calib_packv5_042523_0143.root, FC#4, port A2

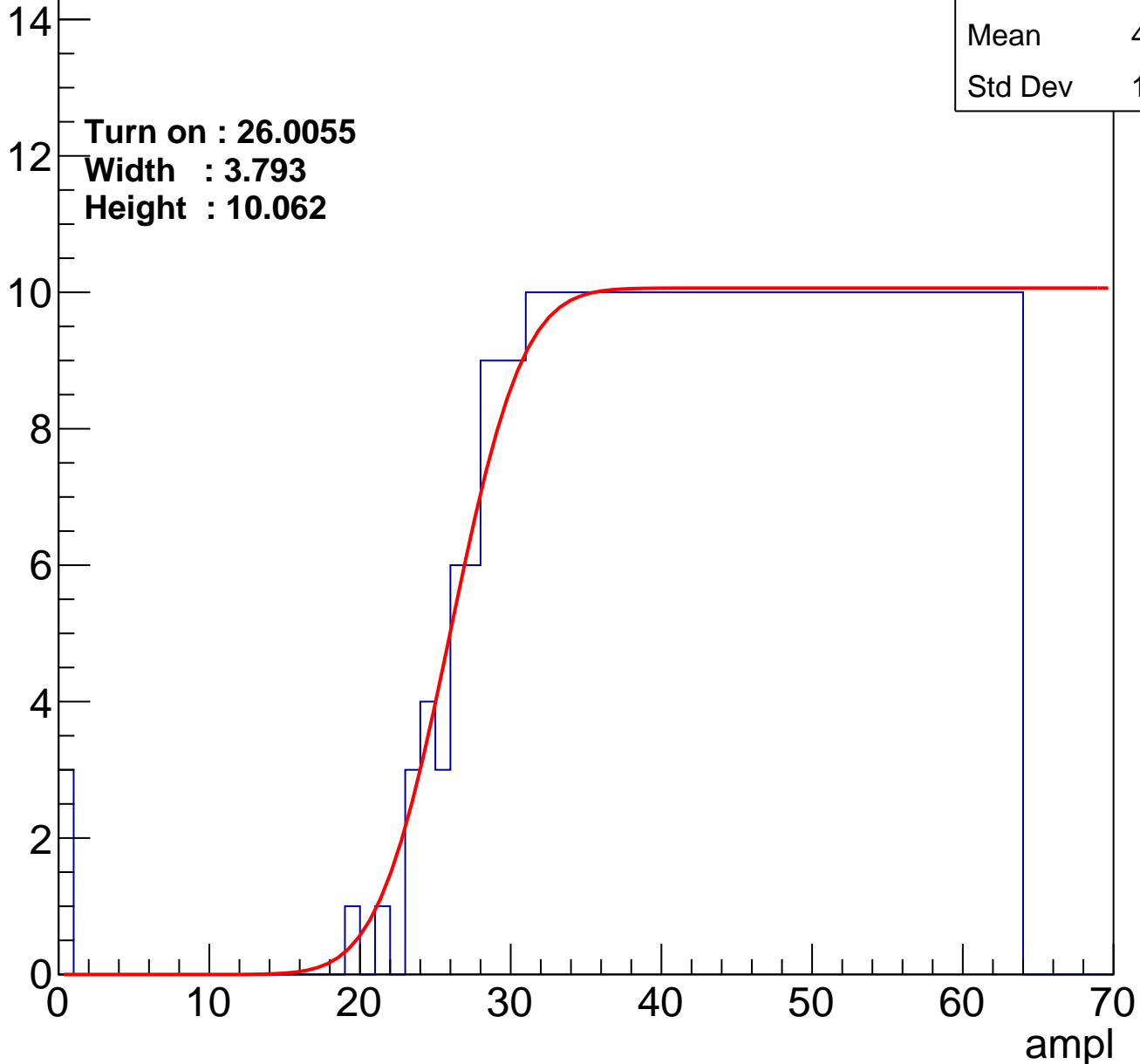
Entries	384
Mean	43.99
Std Dev	11.82

Turn on : 26.0055

Width : 3.793

Height : 10.062

Entry



B1L100S, U4-ch112

calib_packv5_042523_0143.root, FC#4, port A2

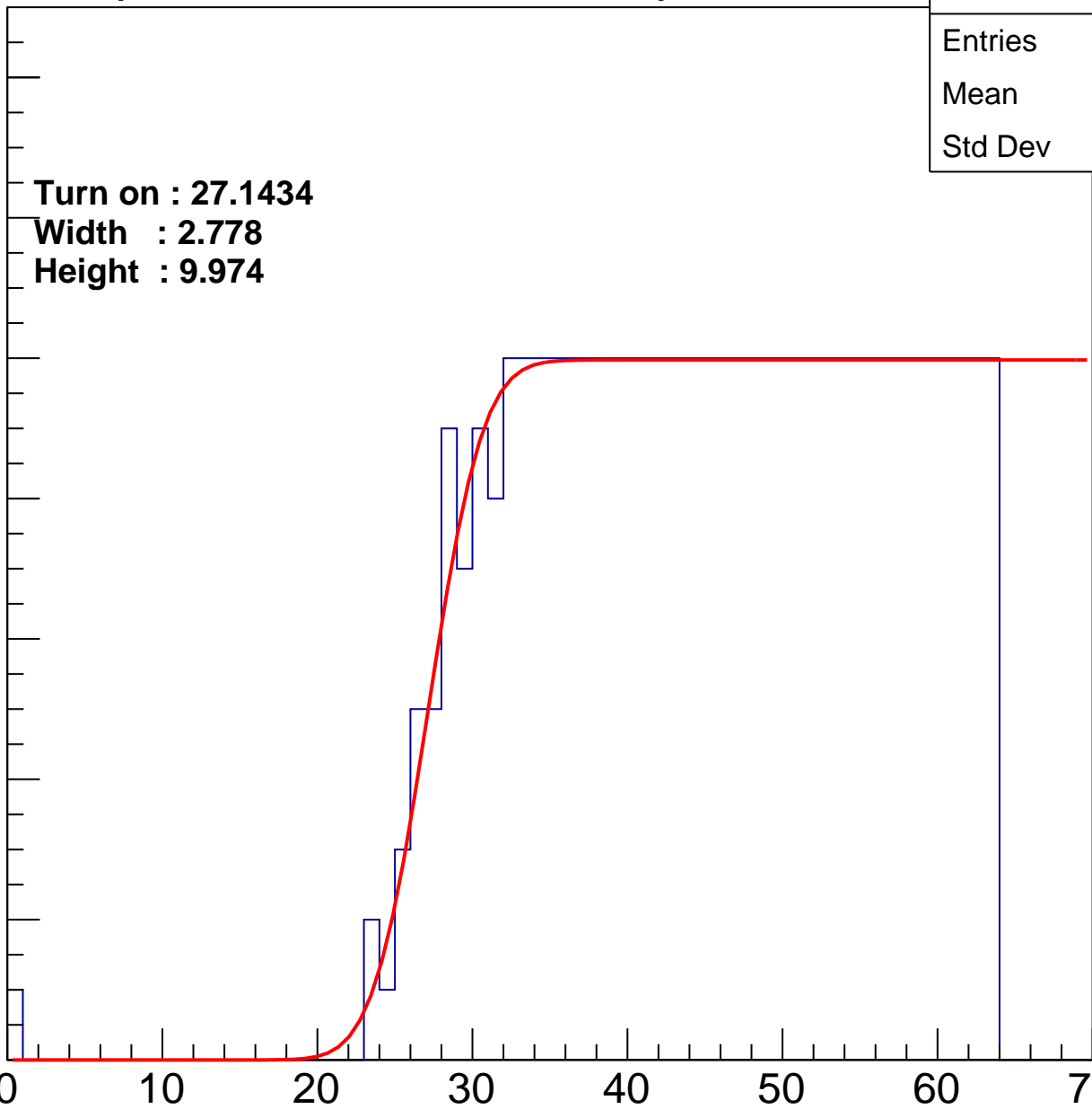
Entry

14
12
10
8
6
4
2
0

Turn on : 27.1434
Width : 2.778
Height : 9.974

Entries	370
Mean	44.82
Std Dev	11.07

ampl



B1L100S, U4-ch113

calib_packv5_042523_0143.root, FC#4, port A2

Entries	377
Mean	44.37
Std Dev	11.5

Turn on : 26.7552

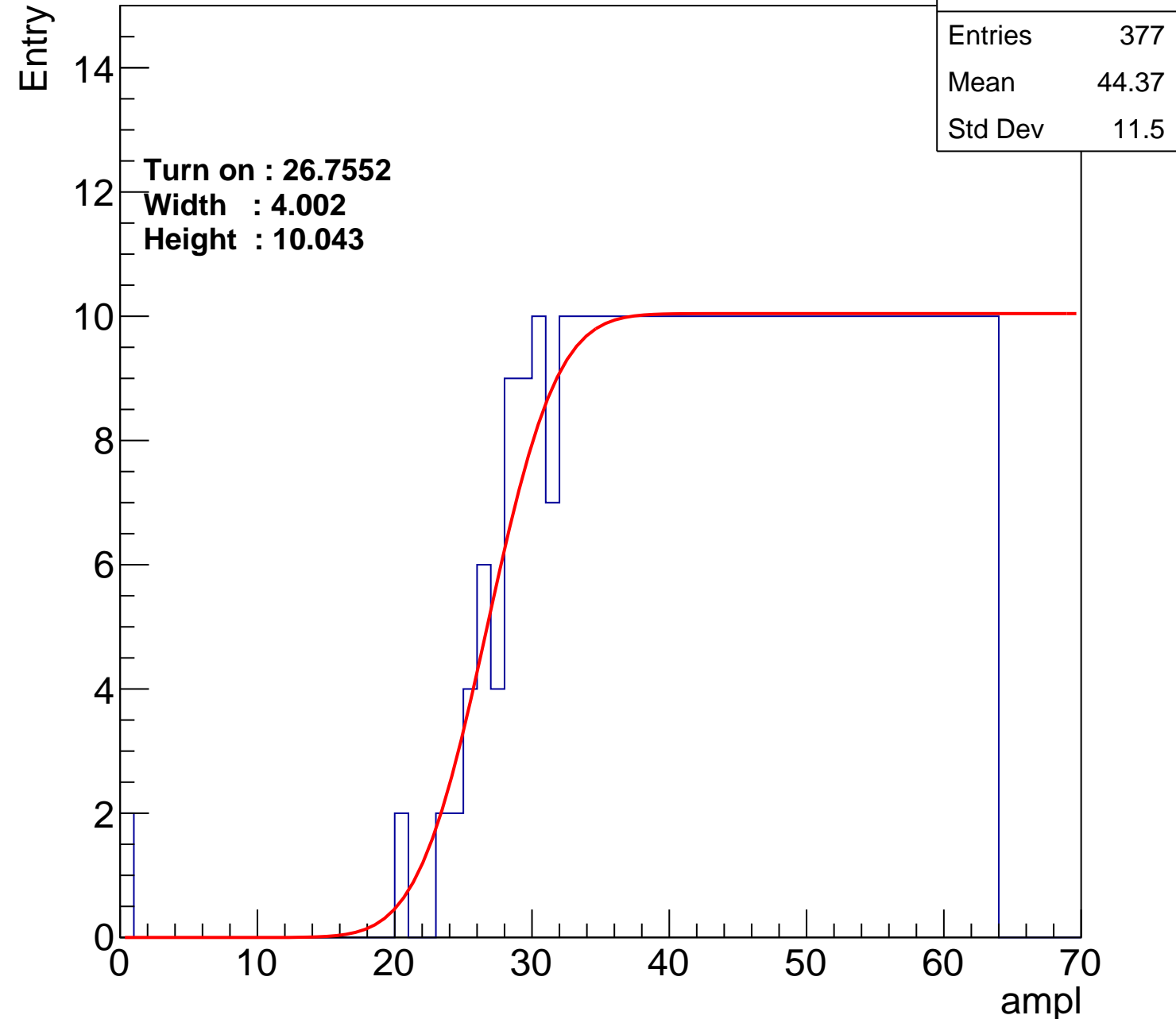
Width : 4.002

Height : 10.043

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch114

calib_packv5_042523_0143.root, FC#4, port A2

Entries	374
Mean	44.45
Std Dev	11.61

Turn on : 27.3656

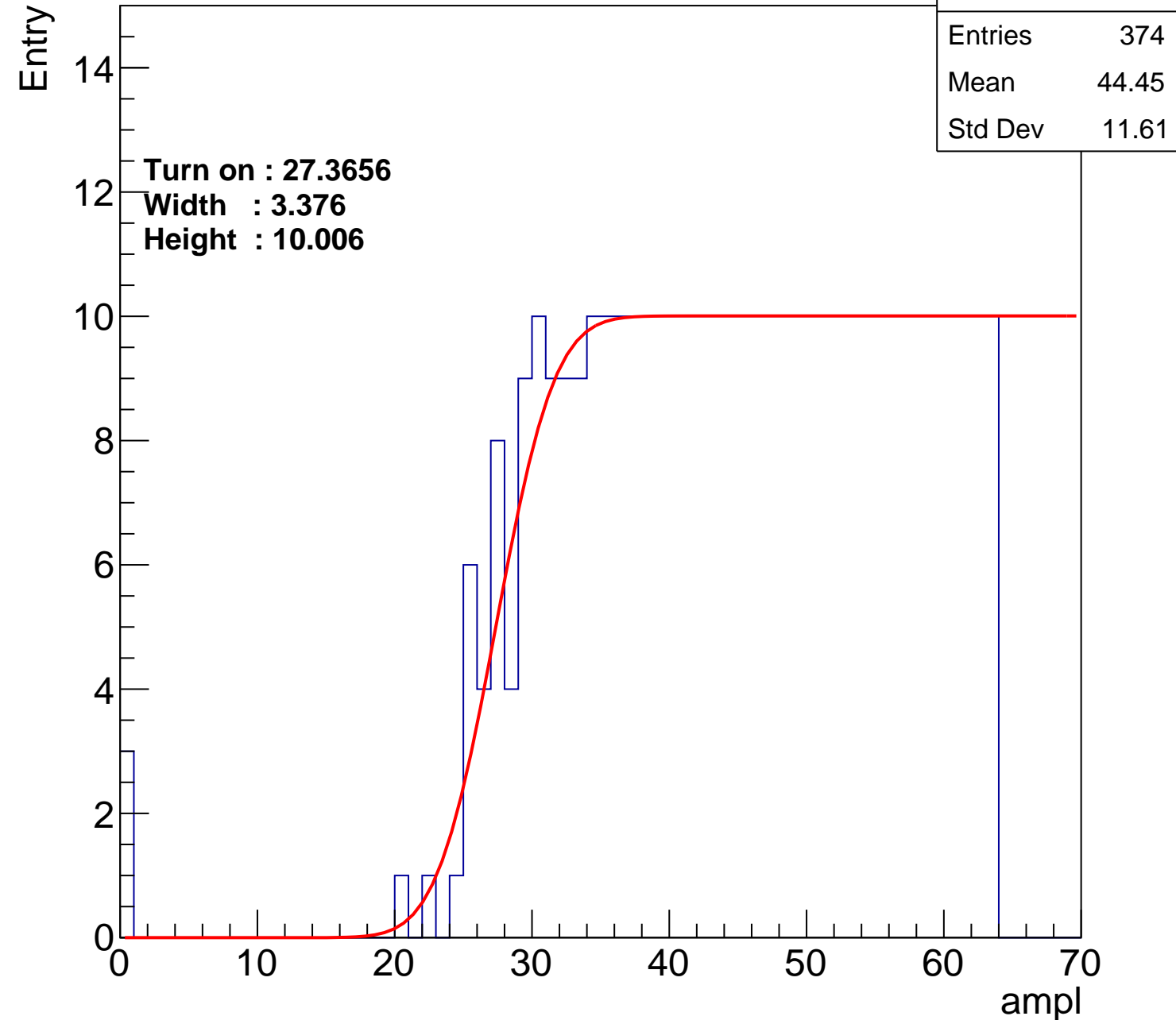
Width : 3.376

Height : 10.006

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch115

calib_packv5_042523_0143.root, FC#4, port A2

Entries	379
Mean	44.28
Std Dev	11.54

Turn on : 26.0799

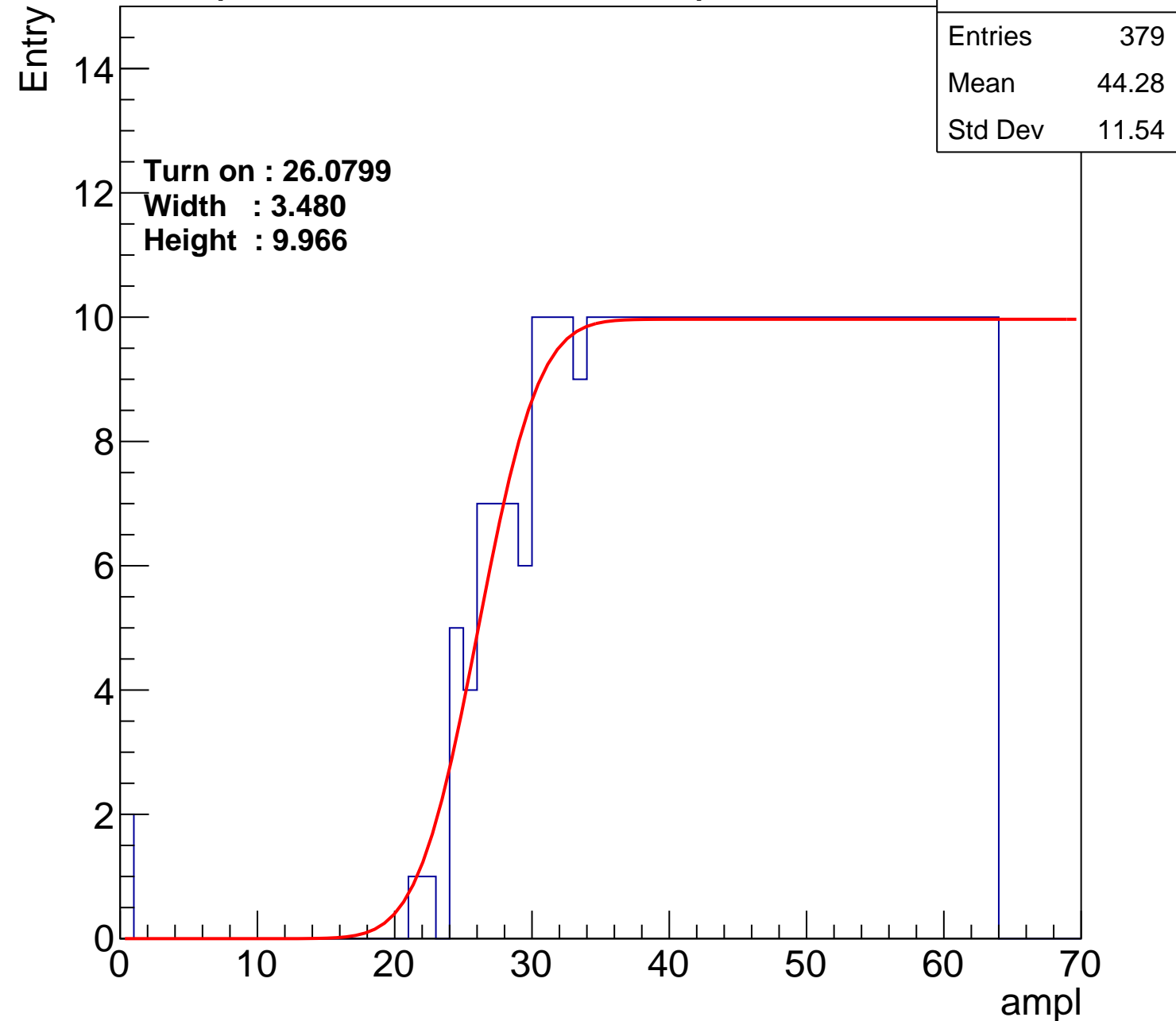
Width : 3.480

Height : 9.966

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch116

calib_packv5_042523_0143.root, FC#4, port A2

Entries	360
Mean	45.08
Std Dev	11.45

Turn on : 28.2233

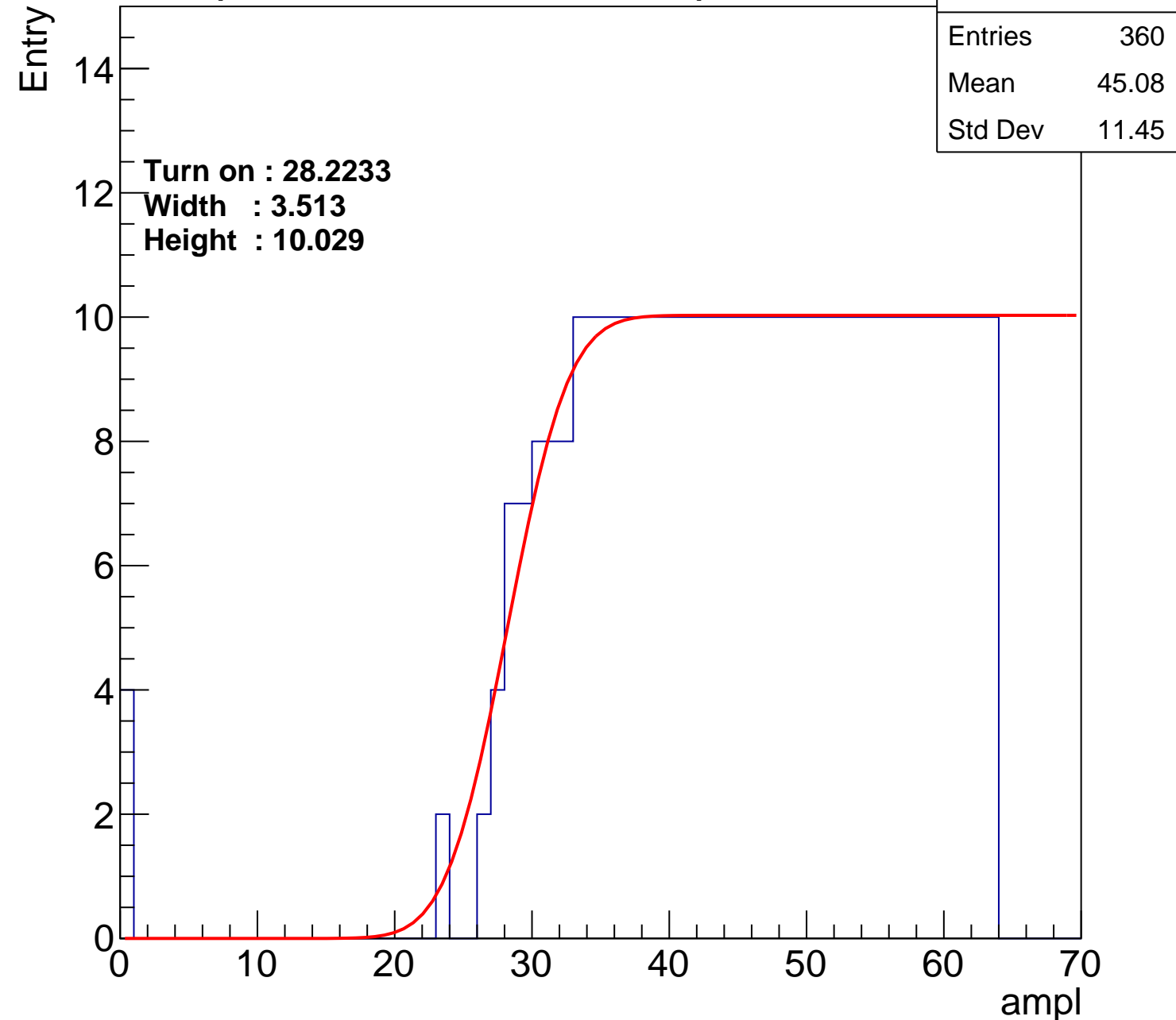
Width : 3.513

Height : 10.029

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch117

calib_packv5_042523_0143.root, FC#4, port A2

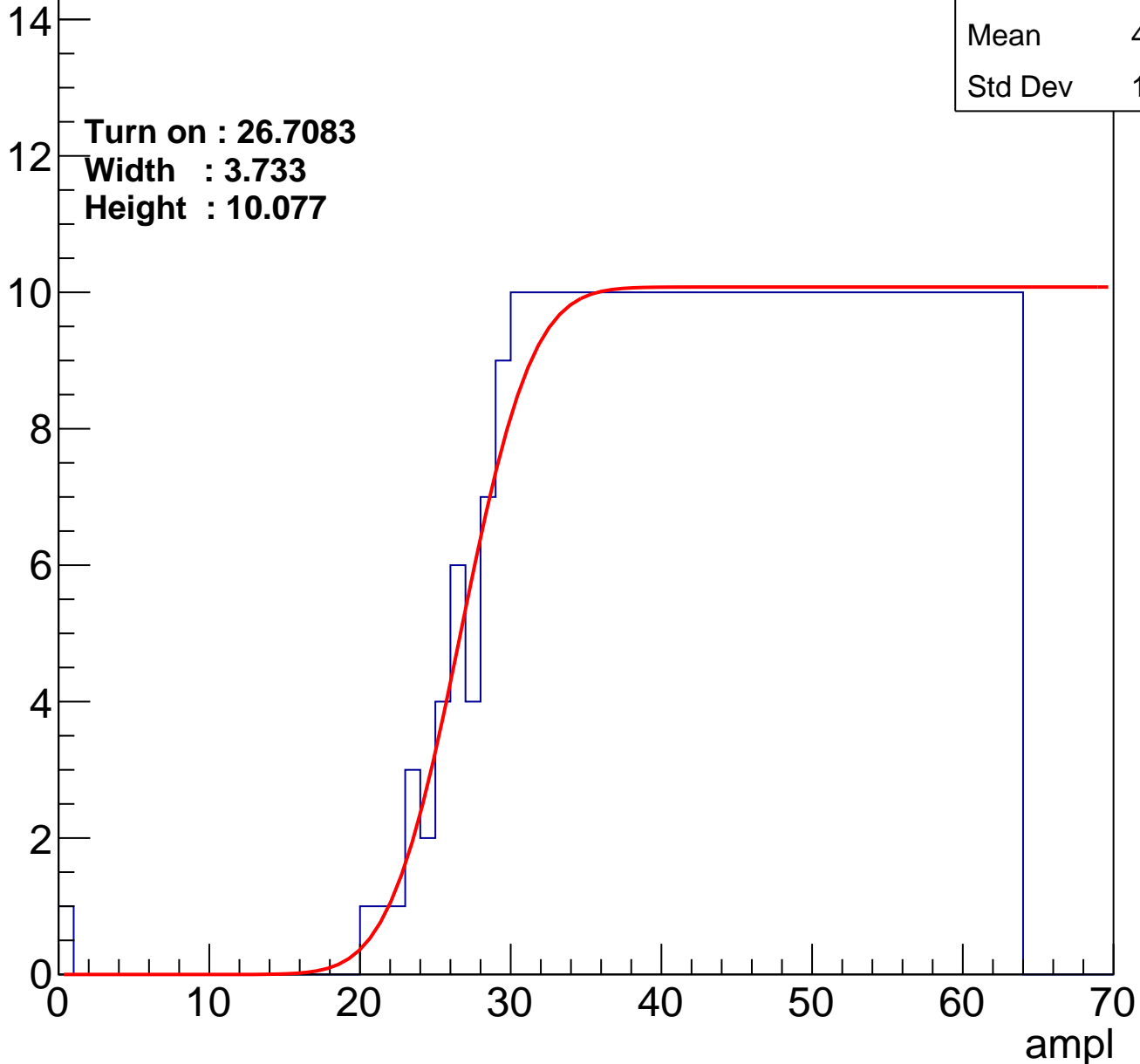
Entries	379
Mean	44.36
Std Dev	11.35

Turn on : 26.7083

Width : 3.733

Height : 10.077

Entry



B1L100S, U4-ch118

calib_packv5_042523_0143.root, FC#4, port A2

Entries	406
Mean	43.04
Std Dev	12.05

Turn on : 24.1198

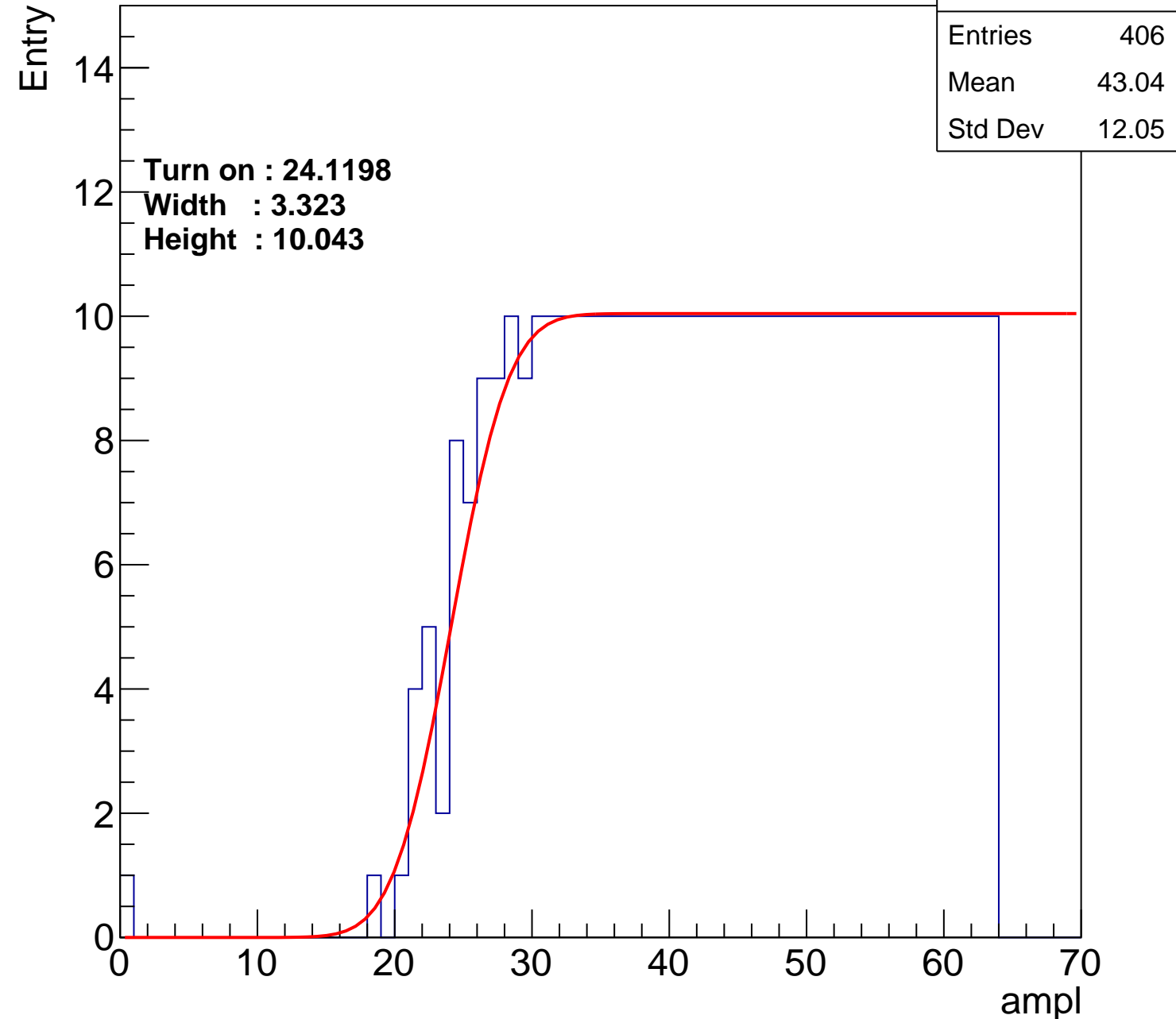
Width : 3.323

Height : 10.043

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch119

calib_packv5_042523_0143.root, FC#4, port A2

Entries	391
Mean	43.78
Std Dev	11.64

Turn on : 25.3051

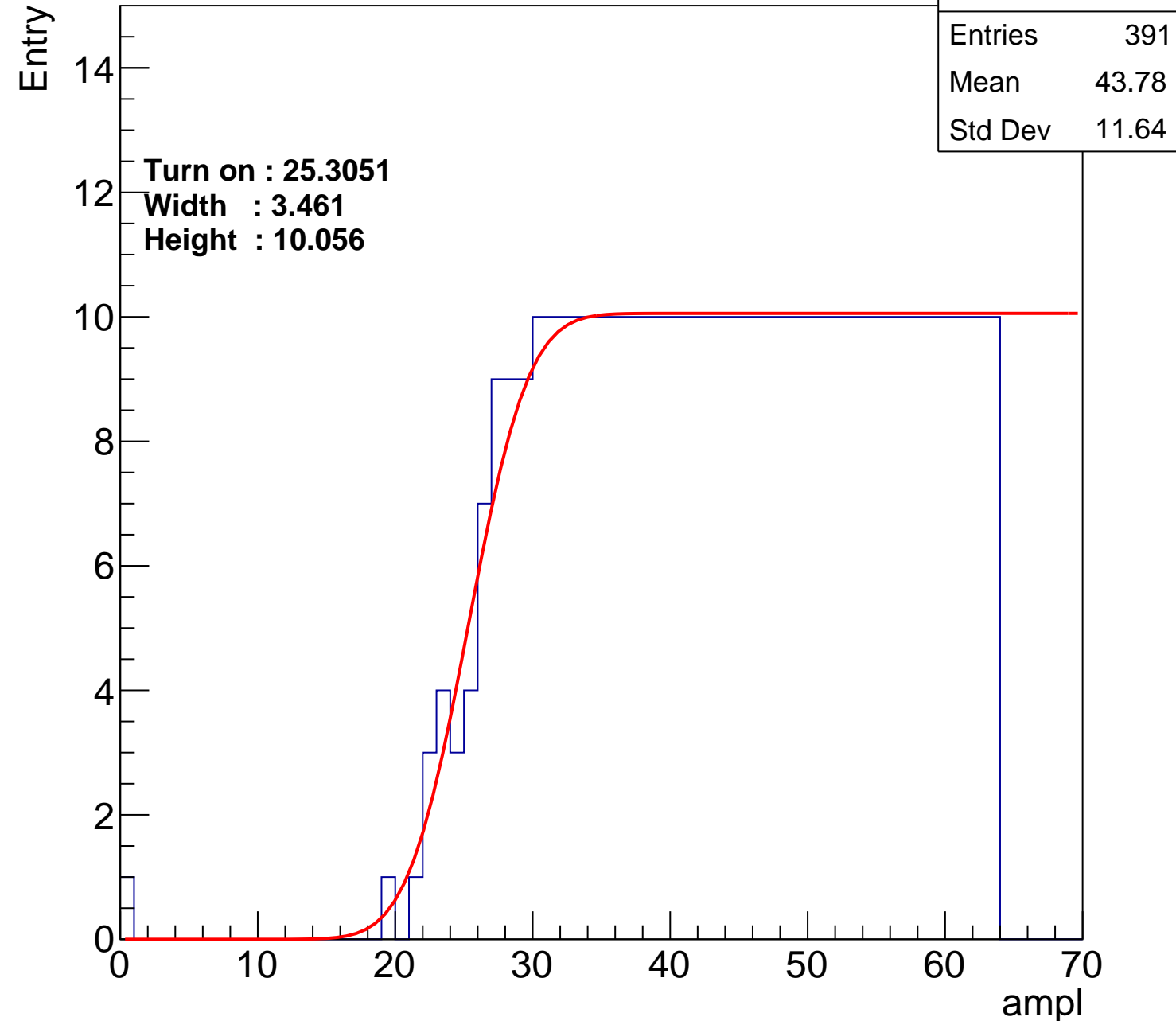
Width : 3.461

Height : 10.056

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch120

calib_packv5_042523_0143.root, FC#4, port A2

Entries	370
Mean	44.66
Std Dev	11.49

Turn on : 27.3097

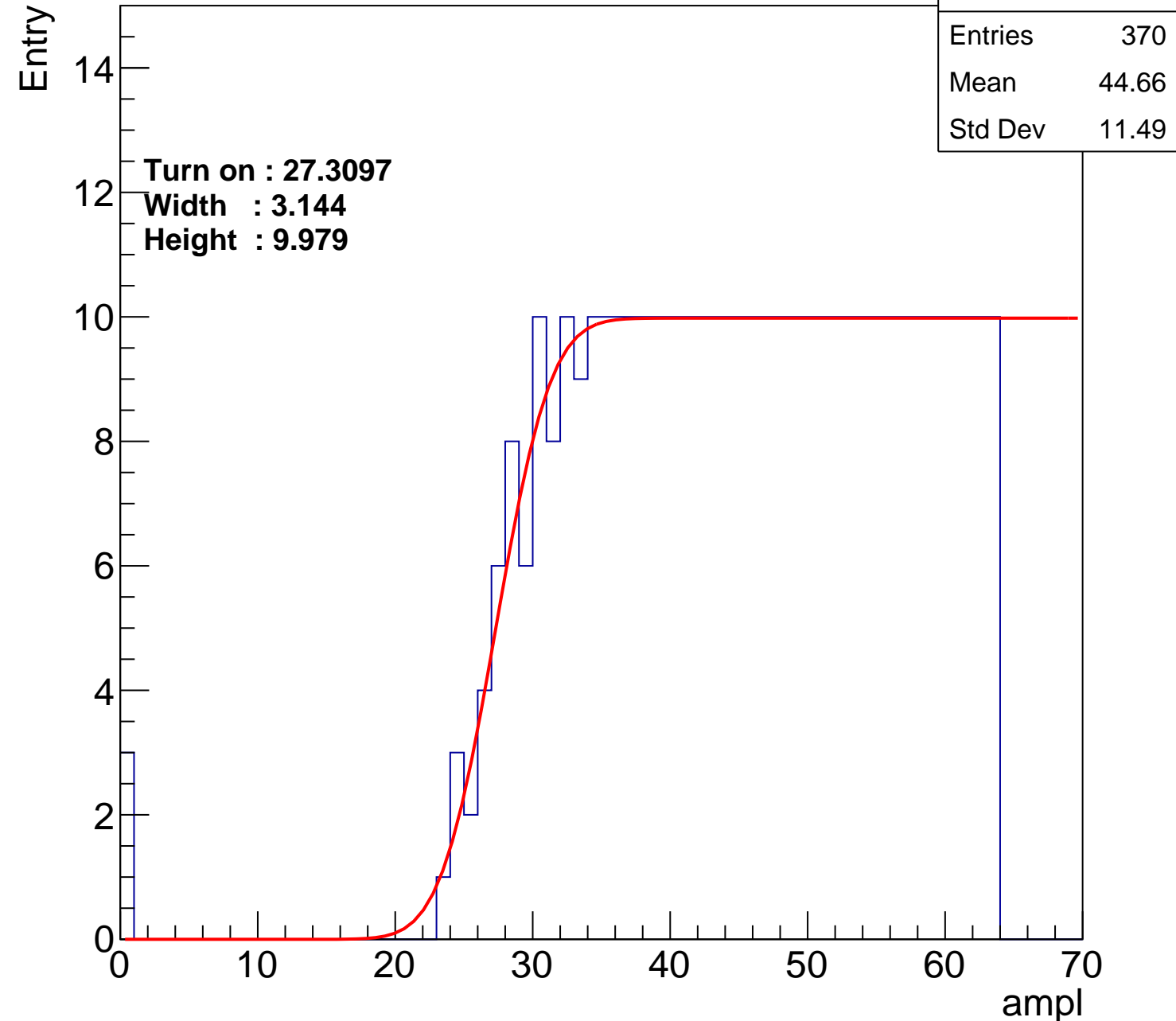
Width : 3.144

Height : 9.979

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch121

calib_packv5_042523_0143.root, FC#4, port A2

Entries	376
Mean	44.28
Std Dev	11.83

Turn on : 26.8112

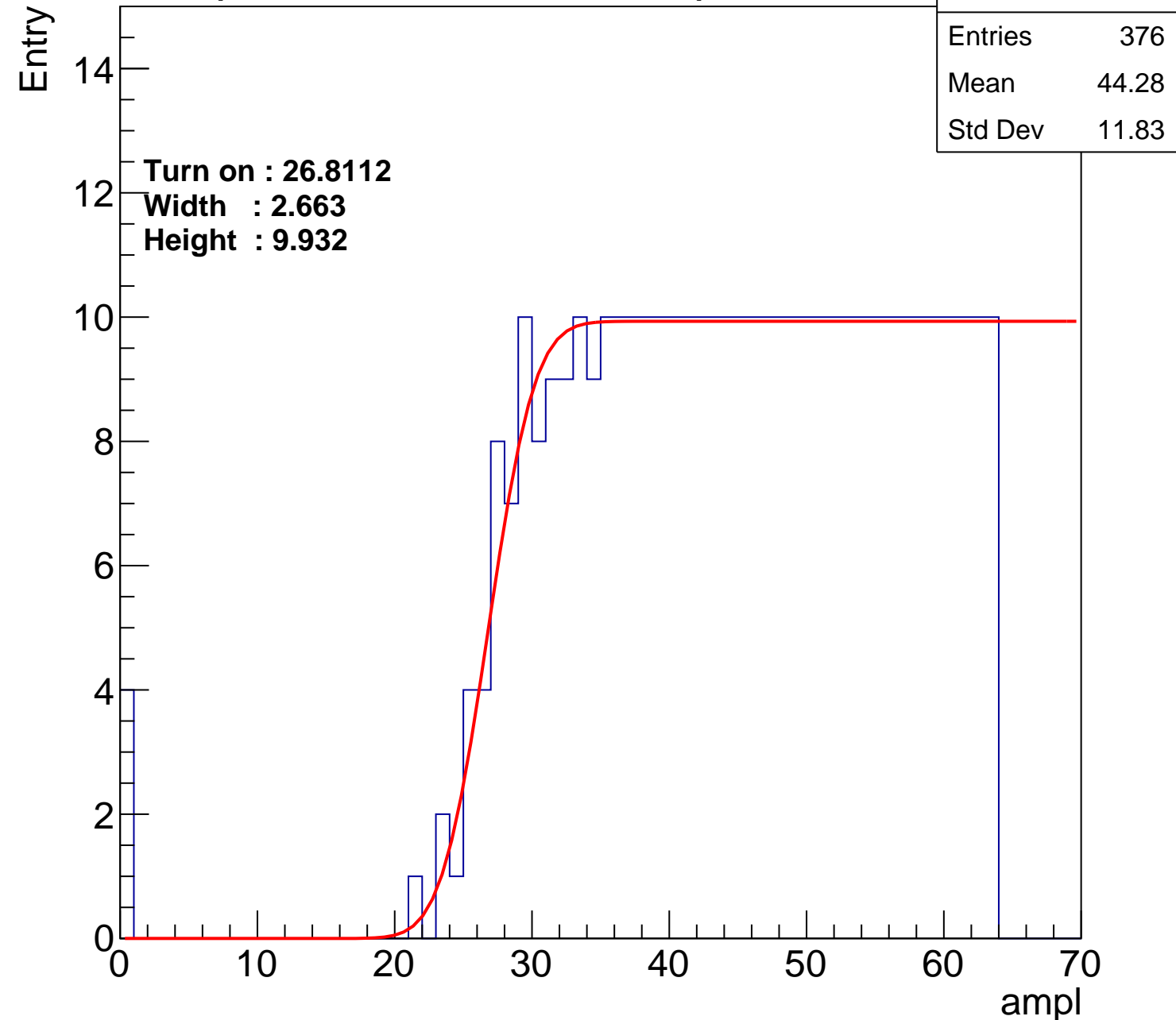
Width : 2.663

Height : 9.932

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch122

calib_packv5_042523_0143.root, FC#4, port A2

Entries	374
Mean	44.61
Std Dev	11.19

Turn on : 26.4533

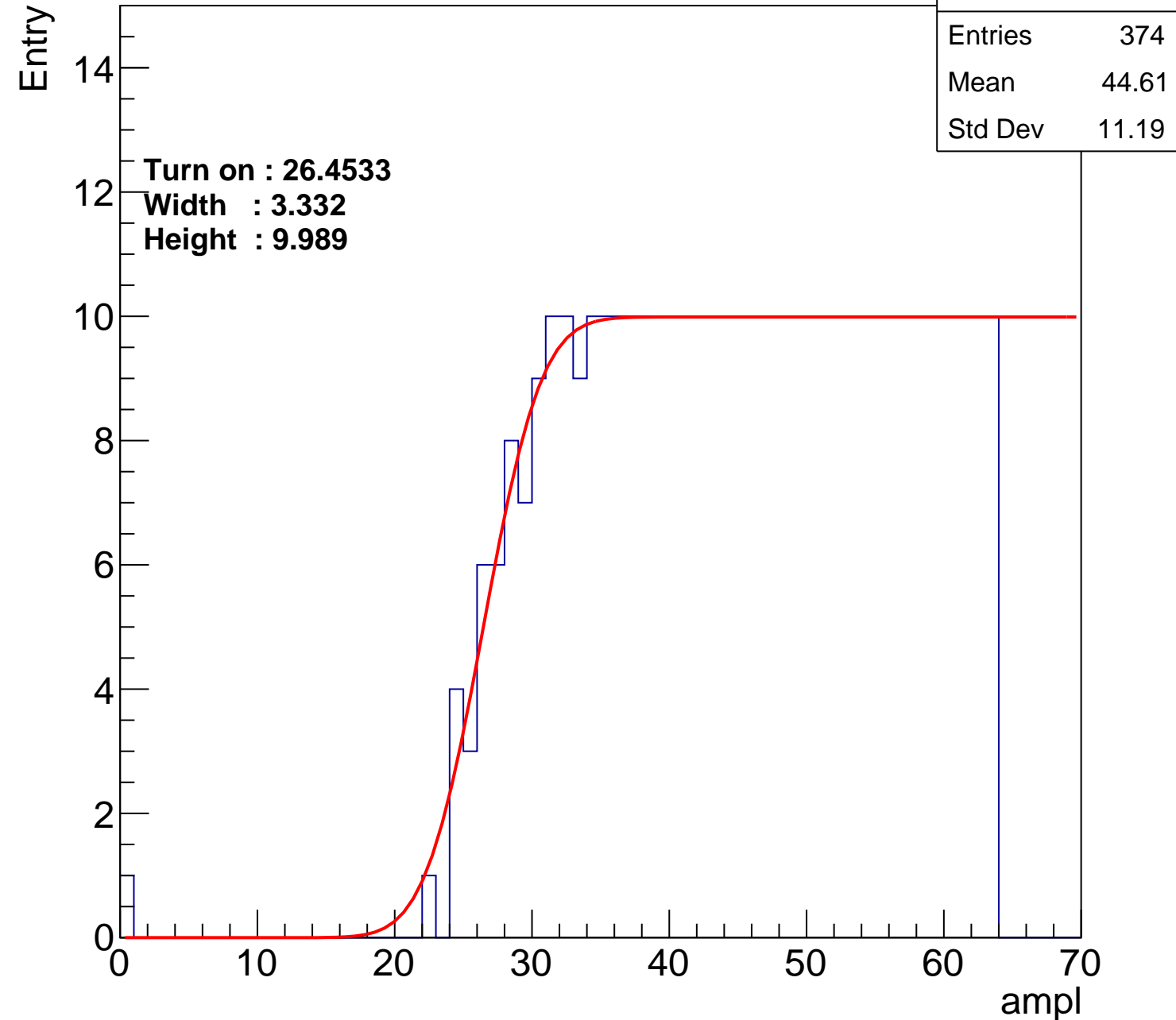
Width : 3.332

Height : 9.989

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch123

calib_packv5_042523_0143.root, FC#4, port A2

Entries	365
Mean	44.93
Std Dev	11.34

Turn on : 28.1261

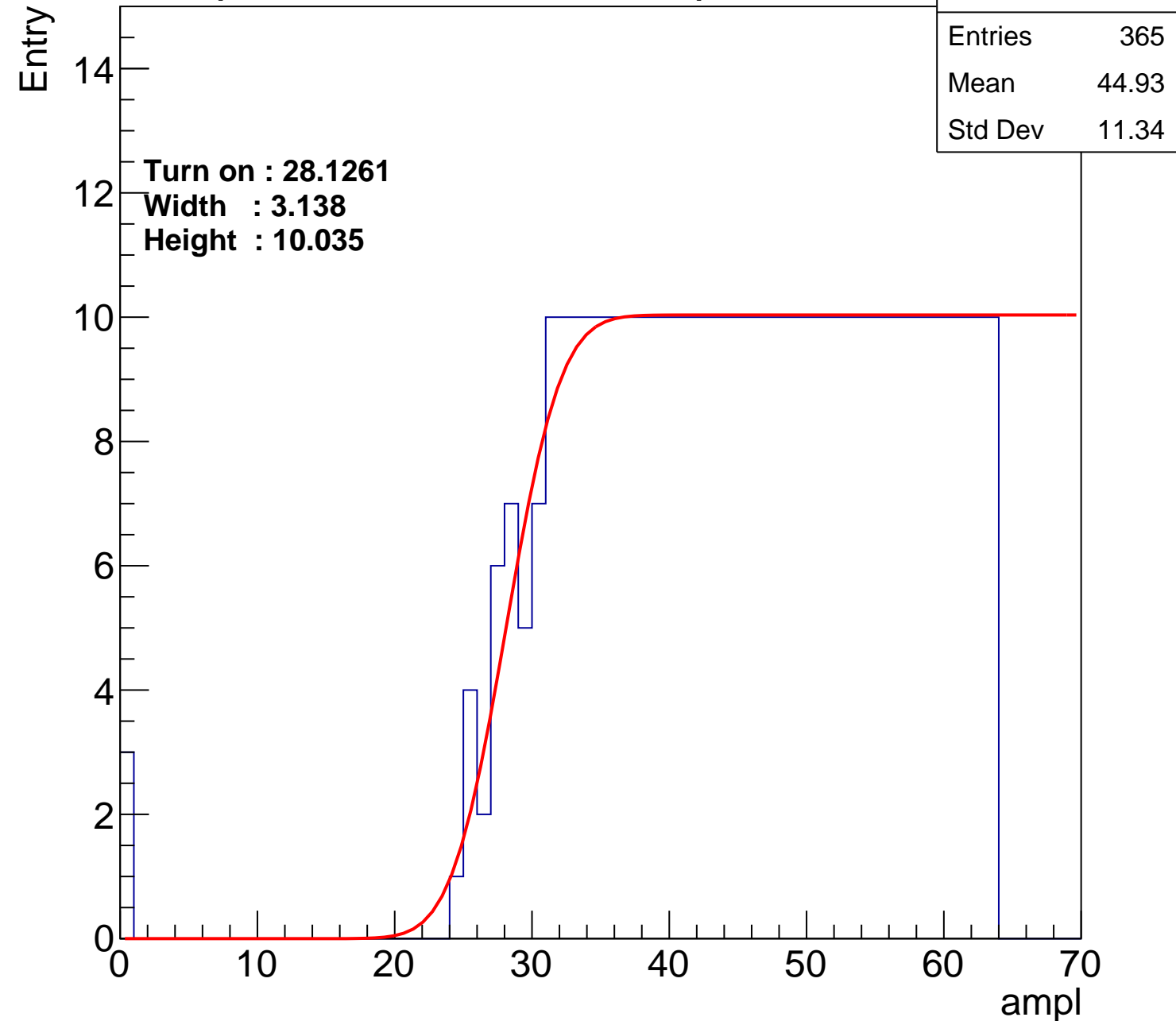
Width : 3.138

Height : 10.035

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch124

calib_packv5_042523_0143.root, FC#4, port A2

Entries	367
Mean	44.84
Std Dev	11.3

Turn on : 28.3832

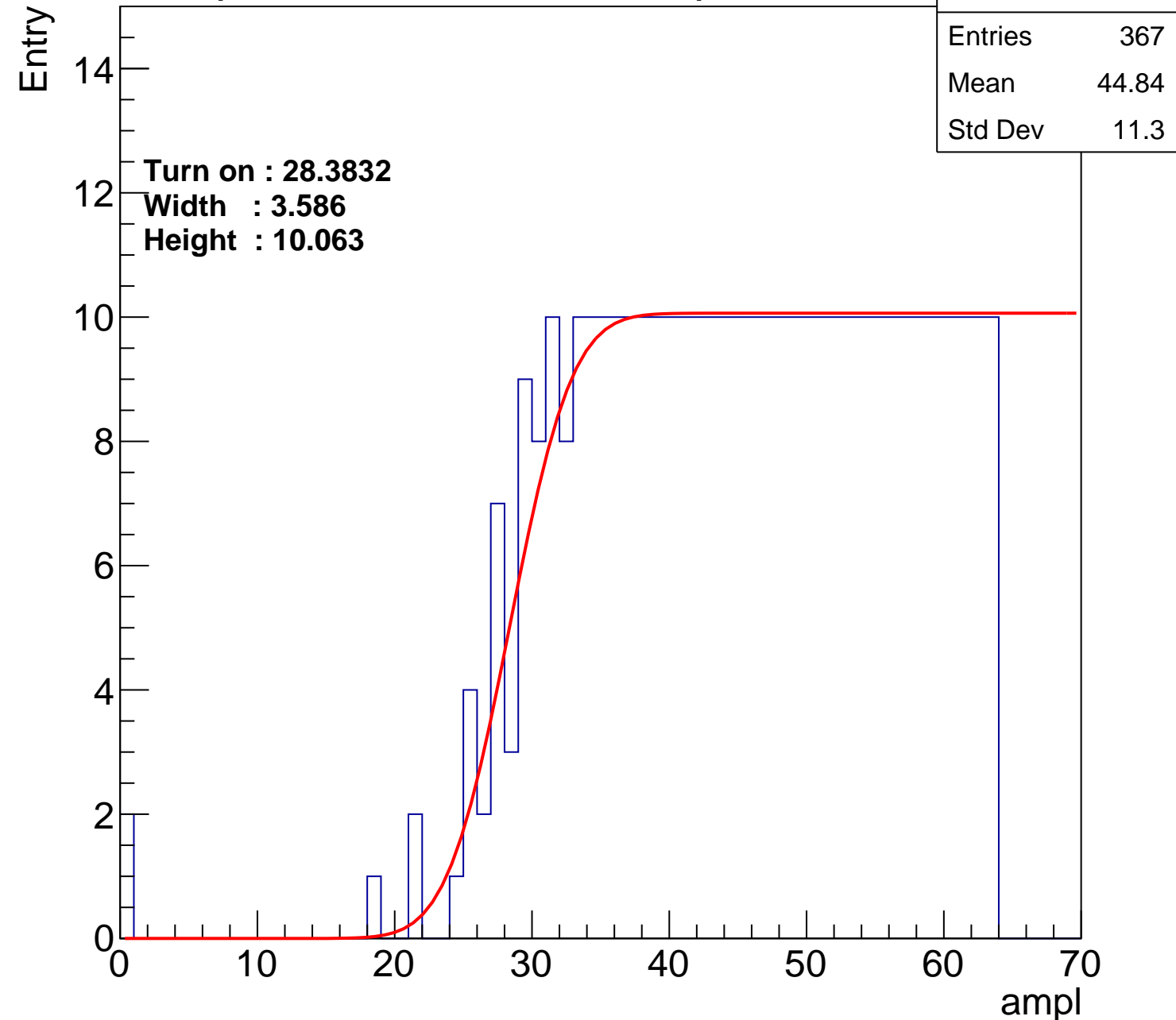
Width : 3.586

Height : 10.063

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch125

calib_packv5_042523_0143.root, FC#4, port A2

Entries	369
Mean	44.86
Std Dev	11.05

Turn on : 27.1842

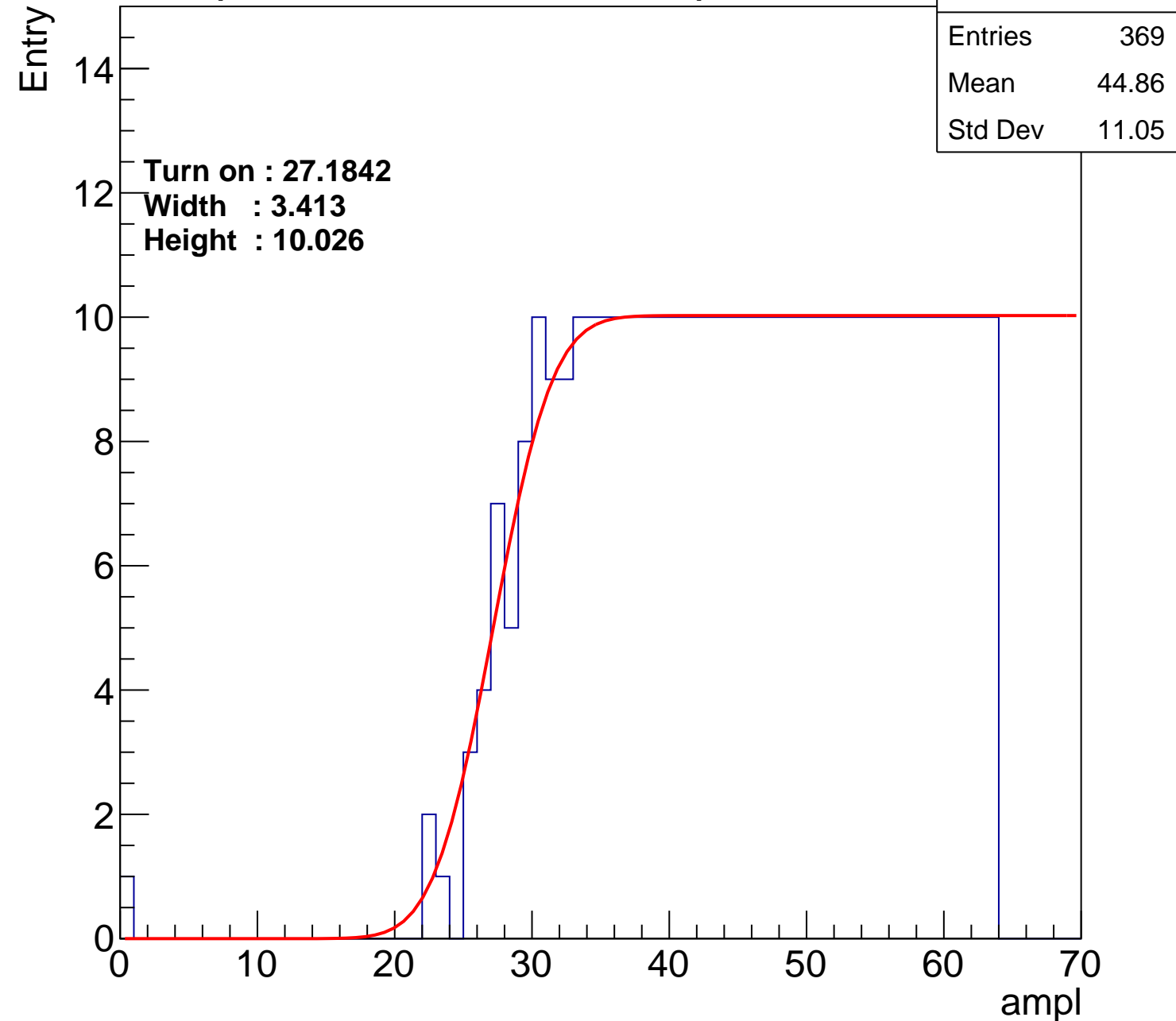
Width : 3.413

Height : 10.026

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U4-ch126

calib_packv5_042523_0143.root, FC#4, port A2

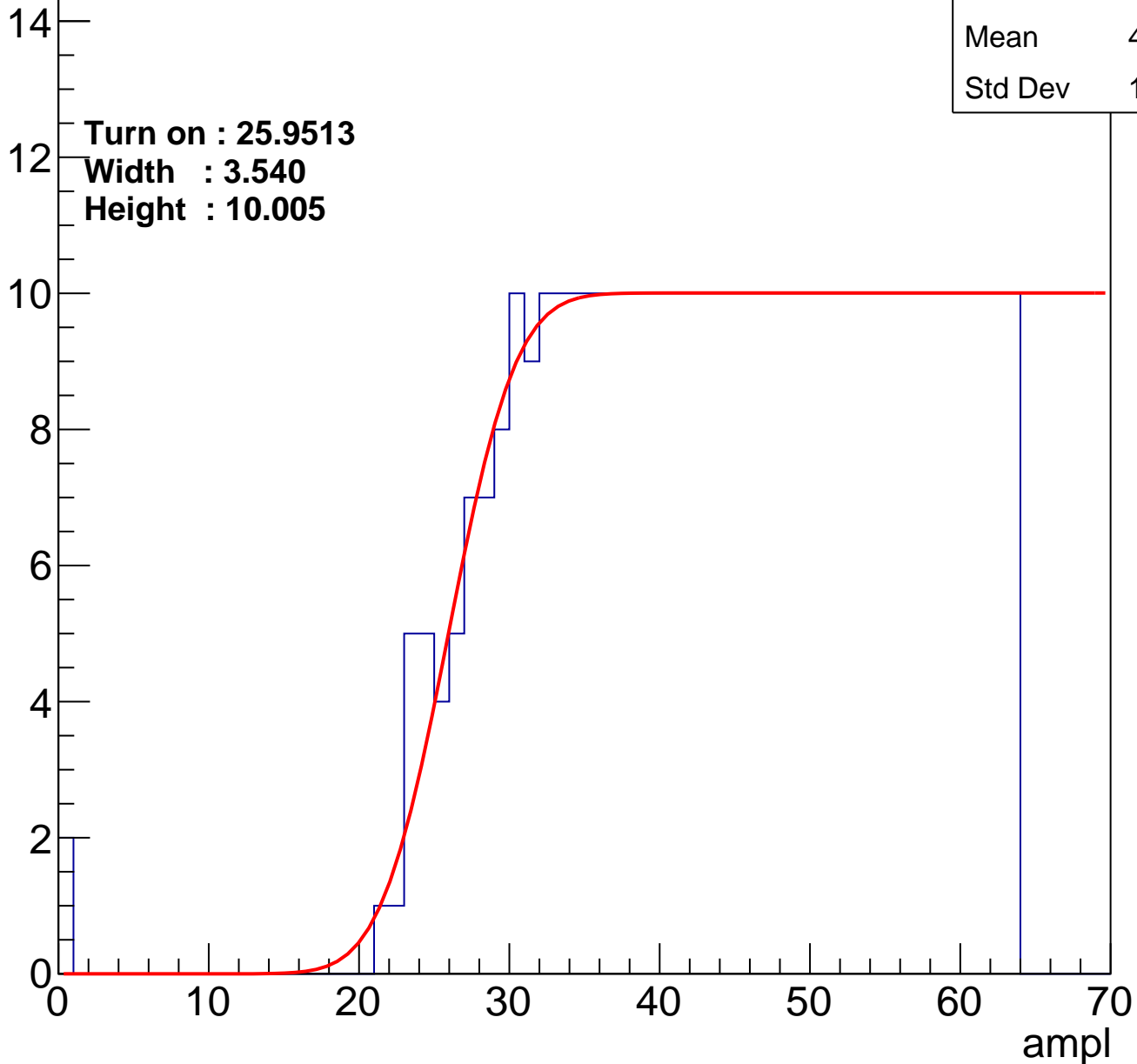
Entries	384
Mean	44.02
Std Dev	11.69

Turn on : 25.9513

Width : 3.540

Height : 10.005

Entry



B1L100S, U4-ch127

calib_packv5_042523_0143.root, FC#4, port A2

Entries	362
Mean	45.15
Std Dev	10.95

Turn on : 28.2021

Width : 2.993

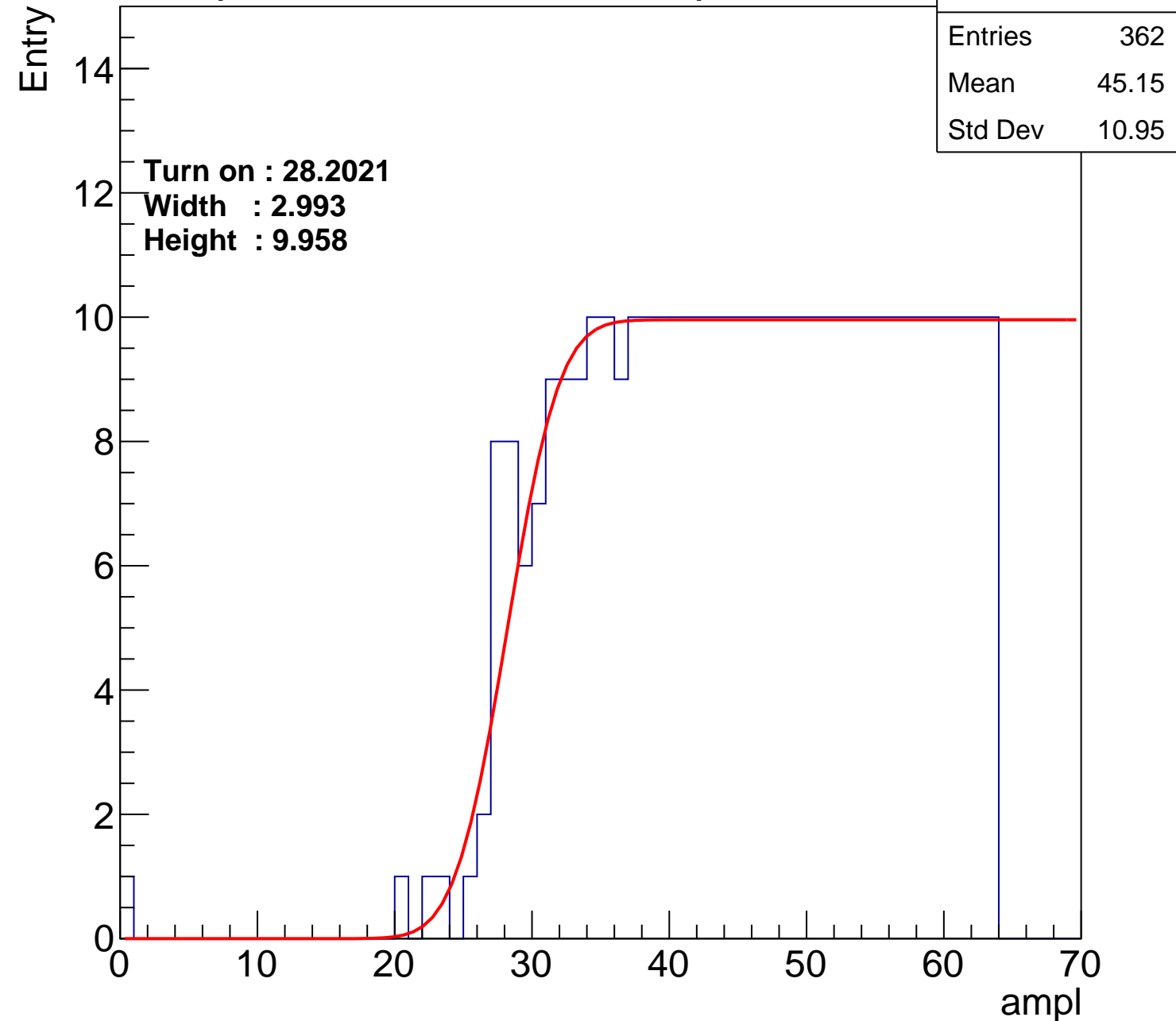
Height : 9.958

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L100S, U4-ch127

calib_packv5_042523_0143.root, FC#4, port A2

Entries	362
Mean	45.15
Std Dev	10.95

Turn on : 28.2021

Width : 2.993

Height : 9.958

Entry

14
12
10
8
6
4
2
0

ampl

