



# B1L101S, U9-ch0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	396
Mean	43.29
Std Dev	12.4

Turn on : 24.9634

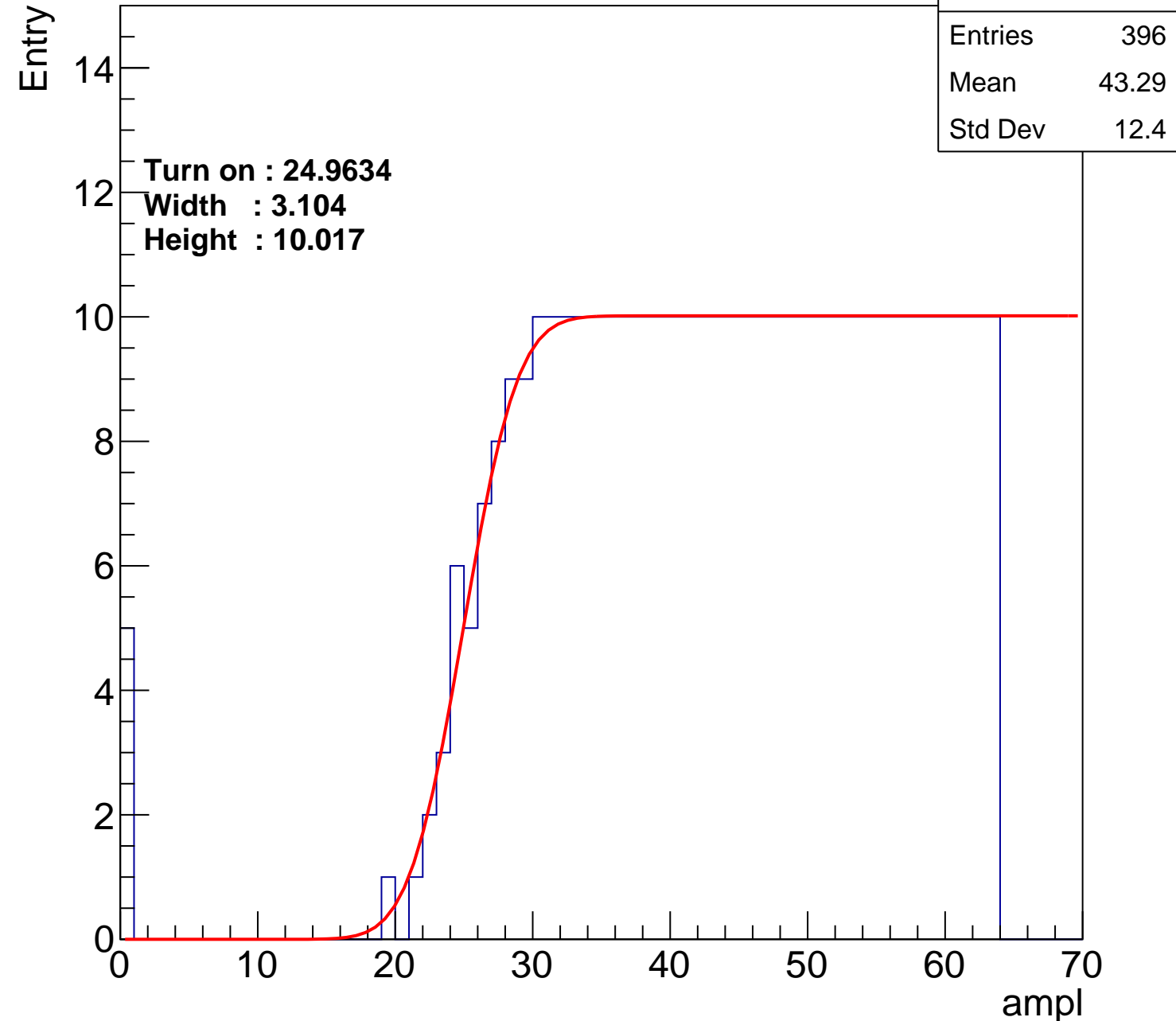
Width : 3.104

Height : 10.017

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch1

calib\_packv5\_042523\_0143.root, FC#0, port D2

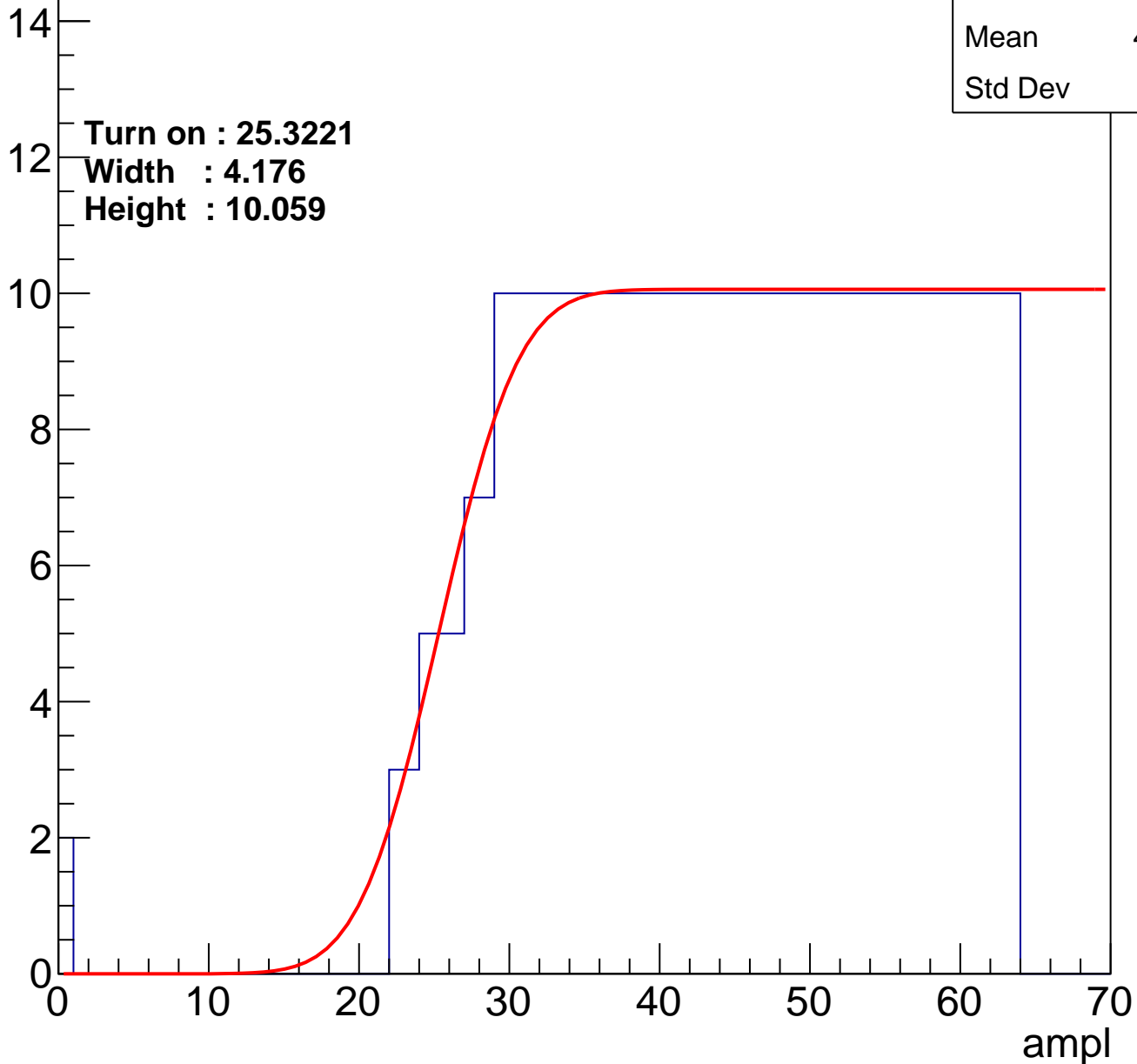
Entries	387
Mean	43.91
Std Dev	11.7

Turn on : 25.3221

Width : 4.176

Height : 10.059

Entry



# B1L101S, U9-ch2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	398
Mean	43.06
Std Dev	12.77

Turn on : 25.4931

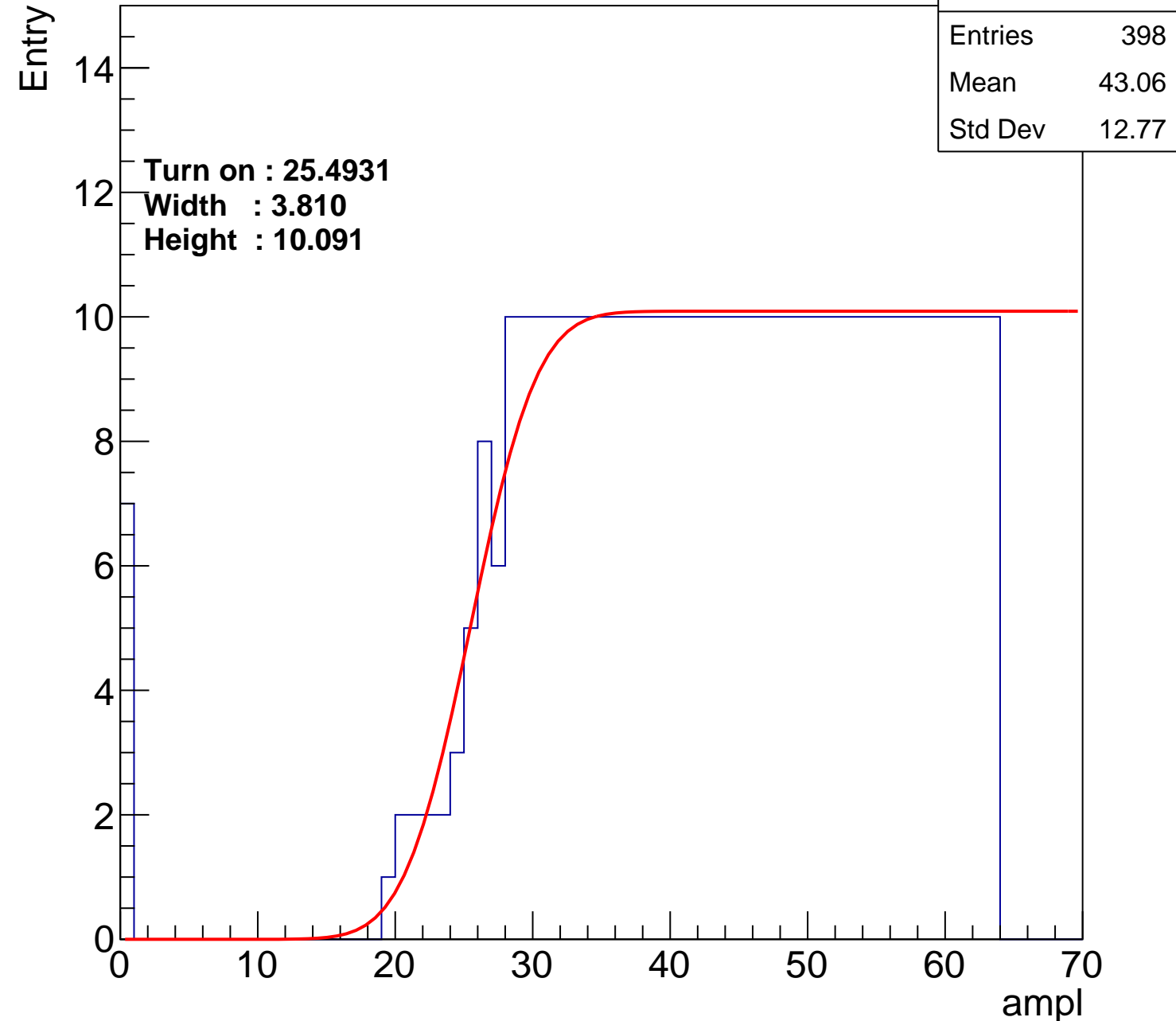
Width : 3.810

Height : 10.091

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	374
Mean	44.53
Std Dev	11.4

Turn on : 26.9384

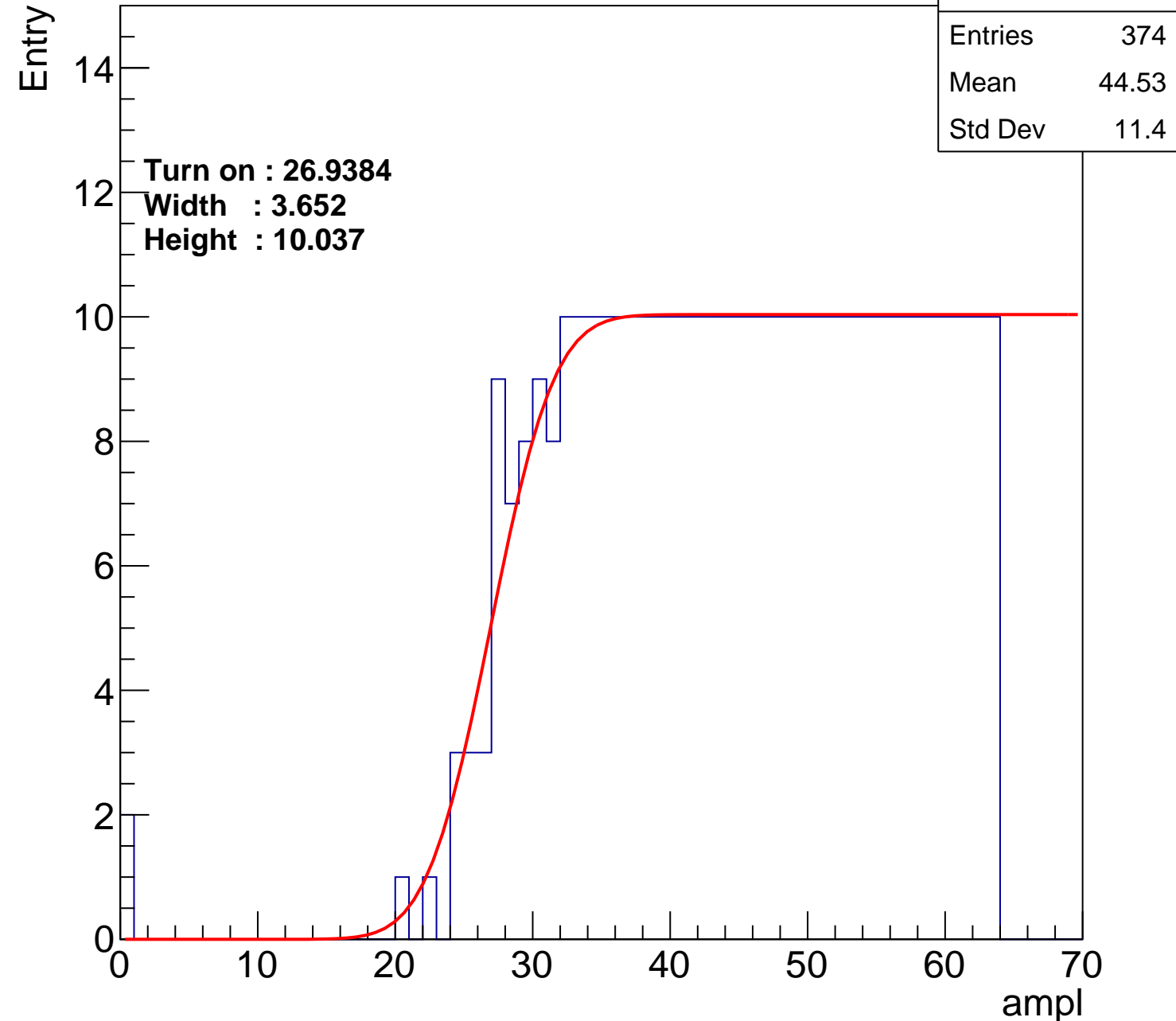
Width : 3.652

Height : 10.037

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	377
Mean	44.42
Std Dev	11.34

Turn on : 26.3241

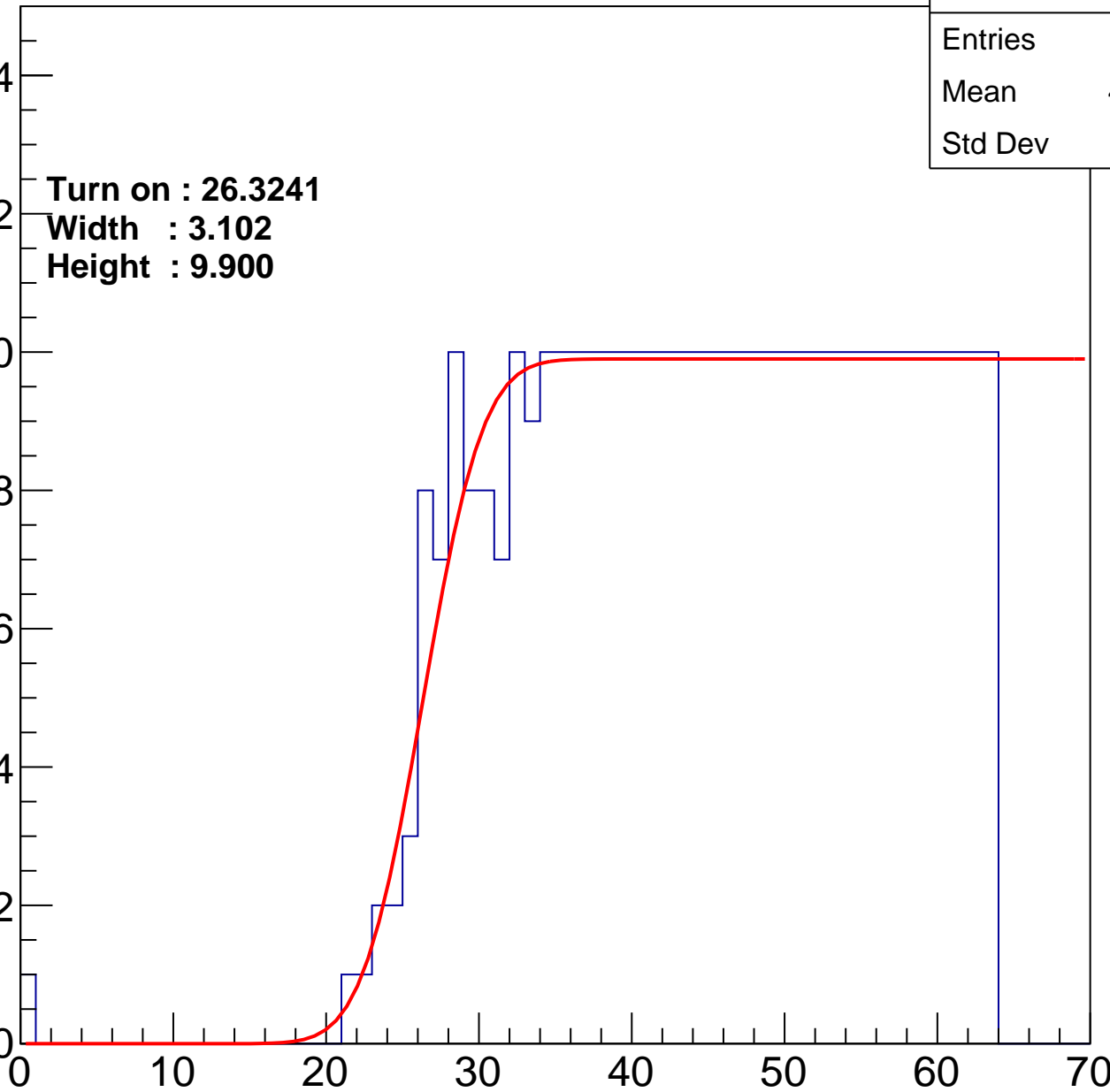
Width : 3.102

Height : 9.900

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	380
Mean	44.23
Std Dev	11.64

Turn on : 26.3218

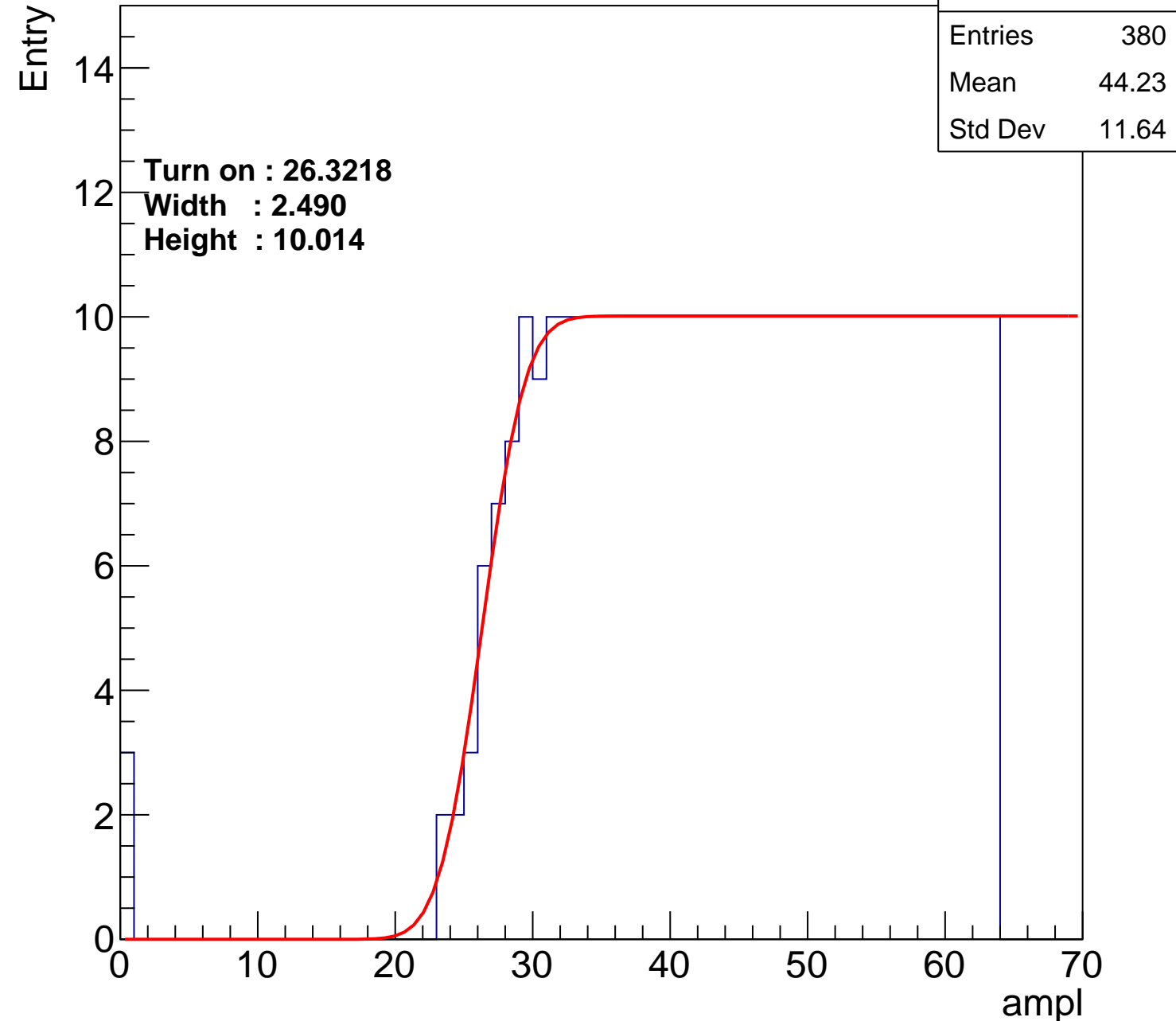
Width : 2.490

Height : 10.014

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch6

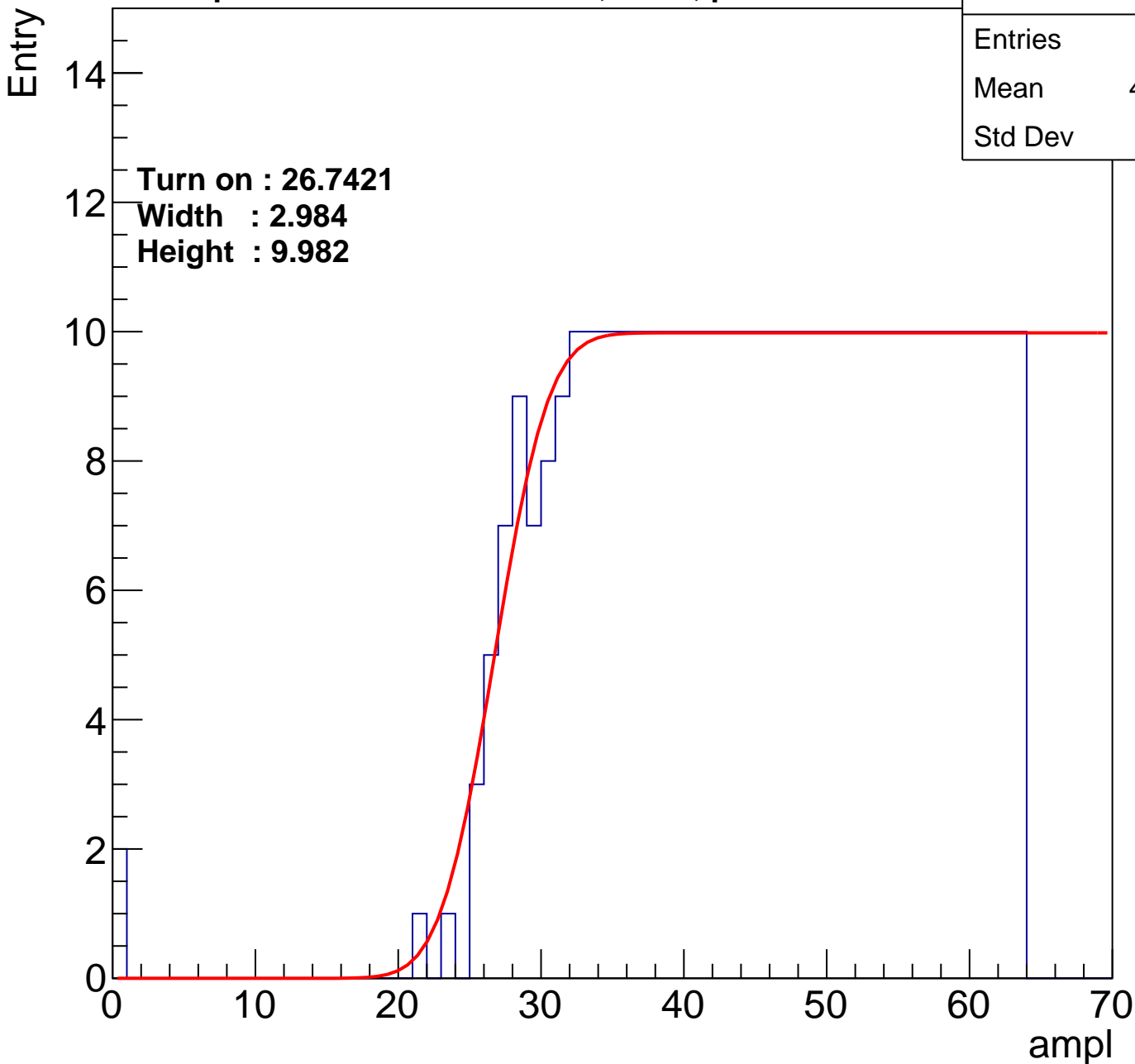
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	372
Mean	44.66
Std Dev	11.31

Turn on : 26.7421

Width : 2.984

Height : 9.982





# B1L101S, U9-ch7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	386
Mean	43.96
Std Dev	11.68

Turn on : 25.8485

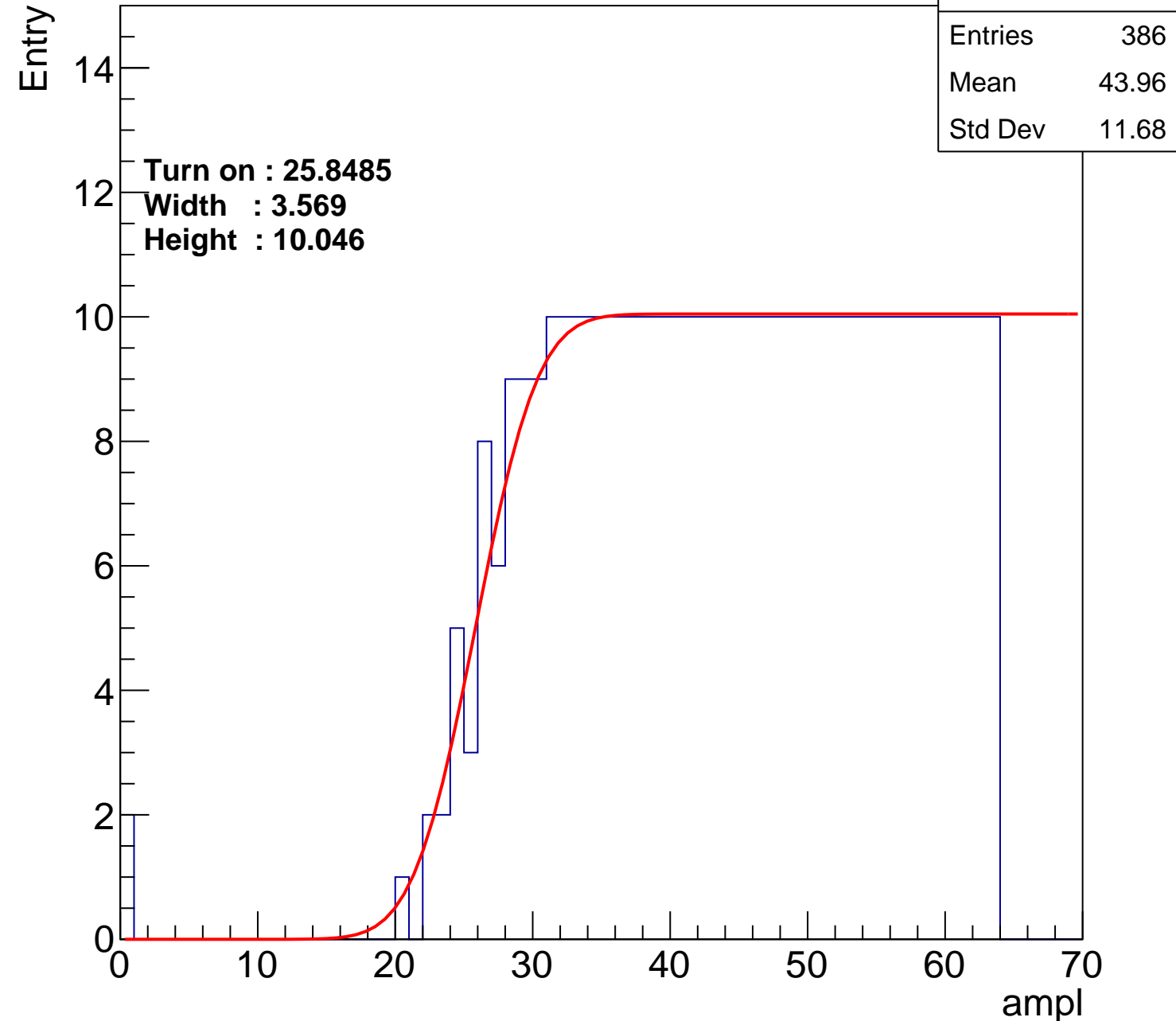
Width : 3.569

Height : 10.046

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch8

calib\_packv5\_042523\_0143.root, FC#0, port D2

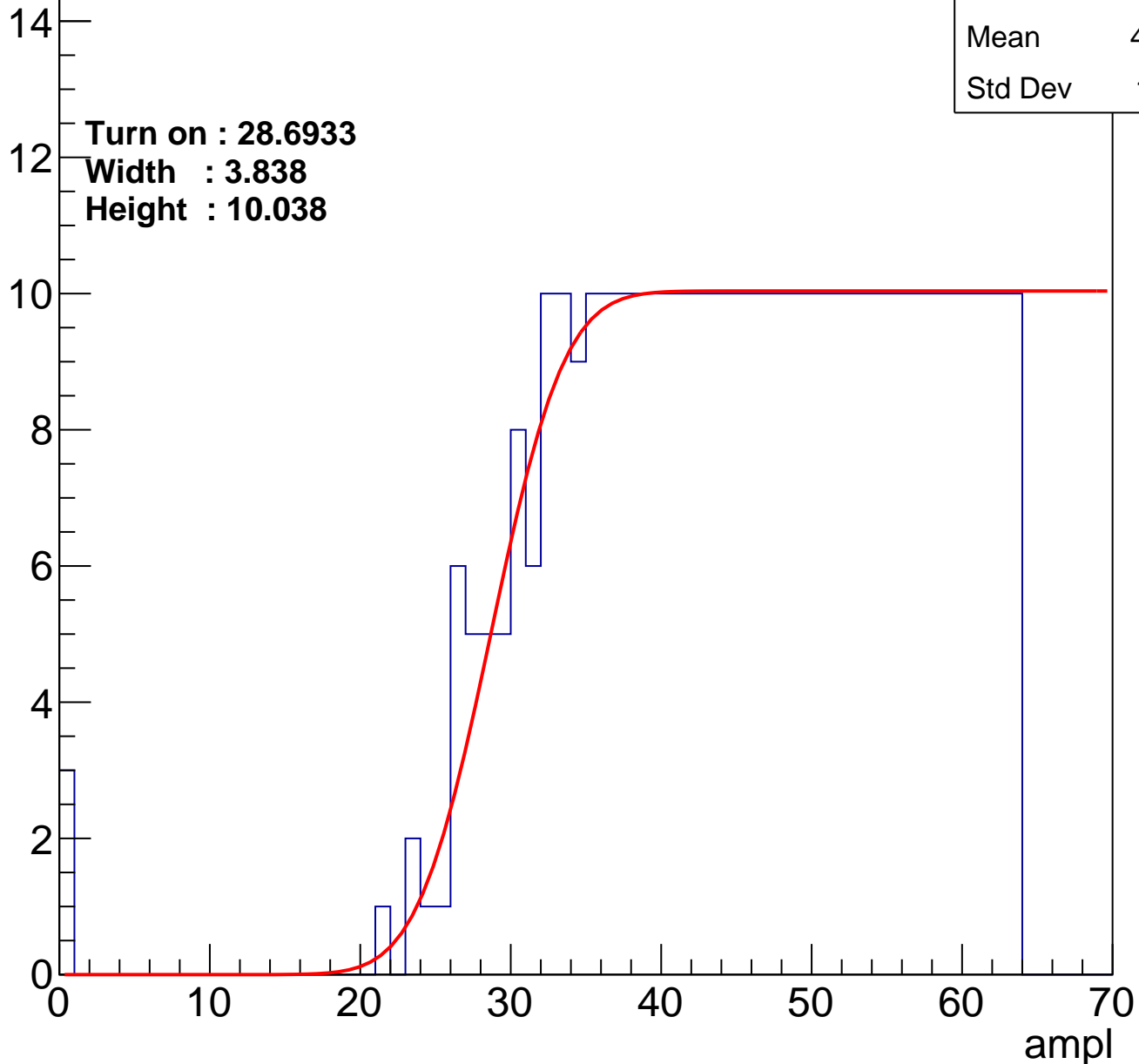
Entries	362
Mean	44.98
Std Dev	11.41

Turn on : 28.6933

Width : 3.838

Height : 10.038

Entry



# B1L101S, U9-ch9

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	379
Mean	44.17
Std Dev	11.87

Turn on : 27.3392

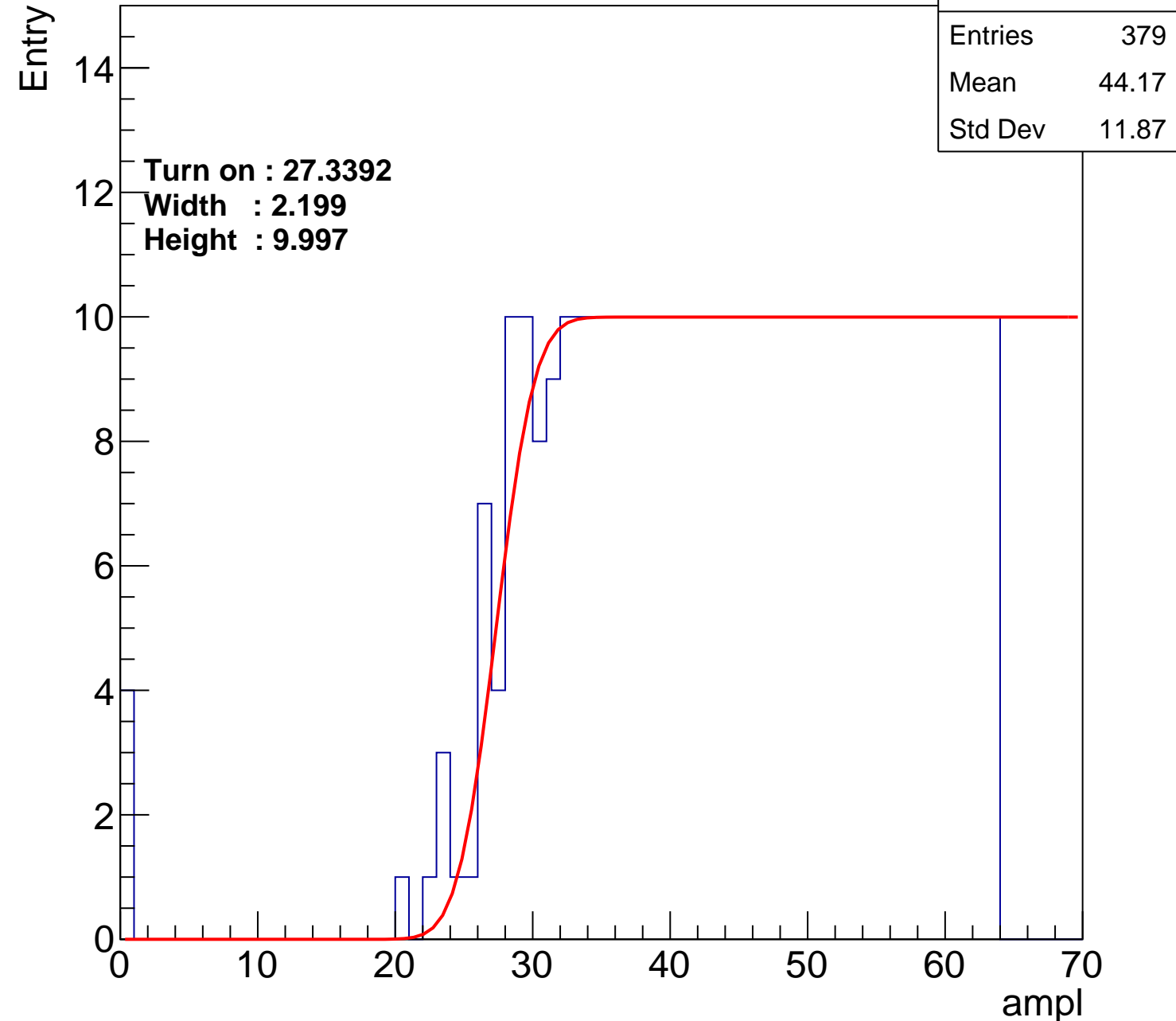
Width : 2.199

Height : 9.997

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch10

calib\_packv5\_042523\_0143.root, FC#0, port D2

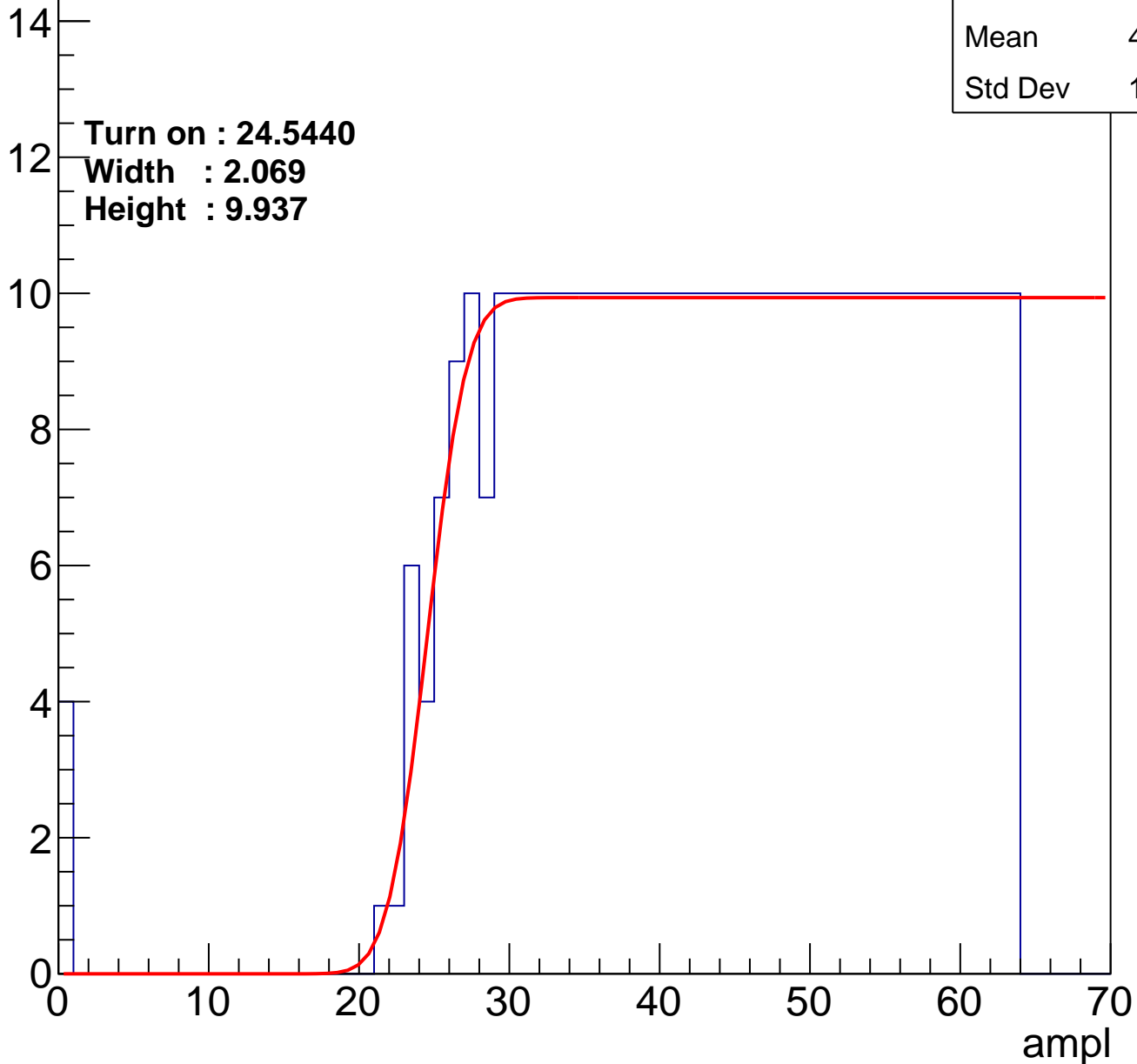
Entries	399
Mean	43.24
Std Dev	12.26

**Turn on : 24.5440**

**Width : 2.069**

**Height : 9.937**

Entry



# B1L101S, U9-ch11

calib\_packv5\_042523\_0143.root, FC#0, port D2

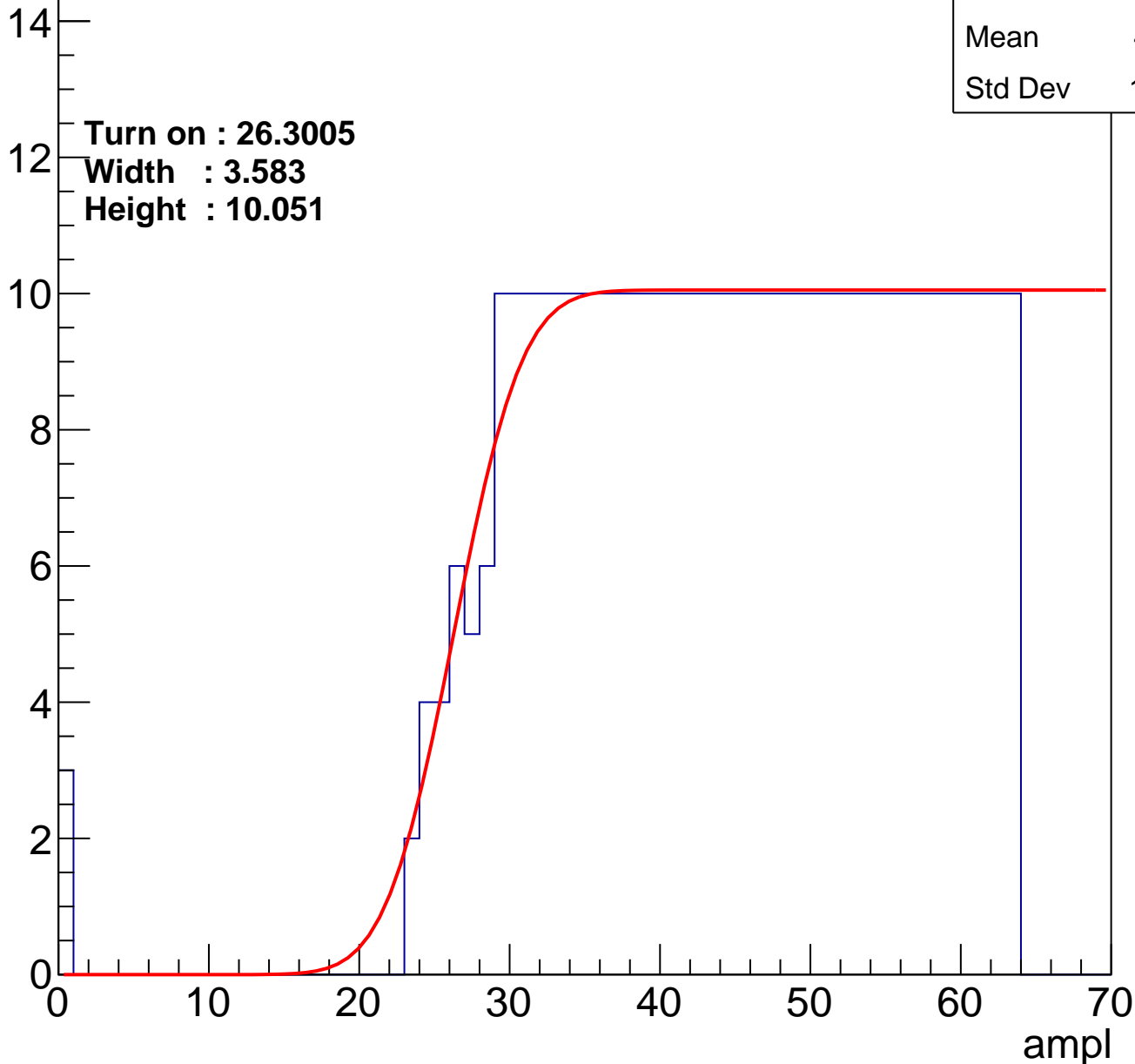
Entries	380
Mean	44.21
Std Dev	11.67

Turn on : 26.3005

Width : 3.583

Height : 10.051

Entry



# B1L101S, U9-ch12

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	383
Mean	44.09
Std Dev	11.71

**Turn on : 26.2960**

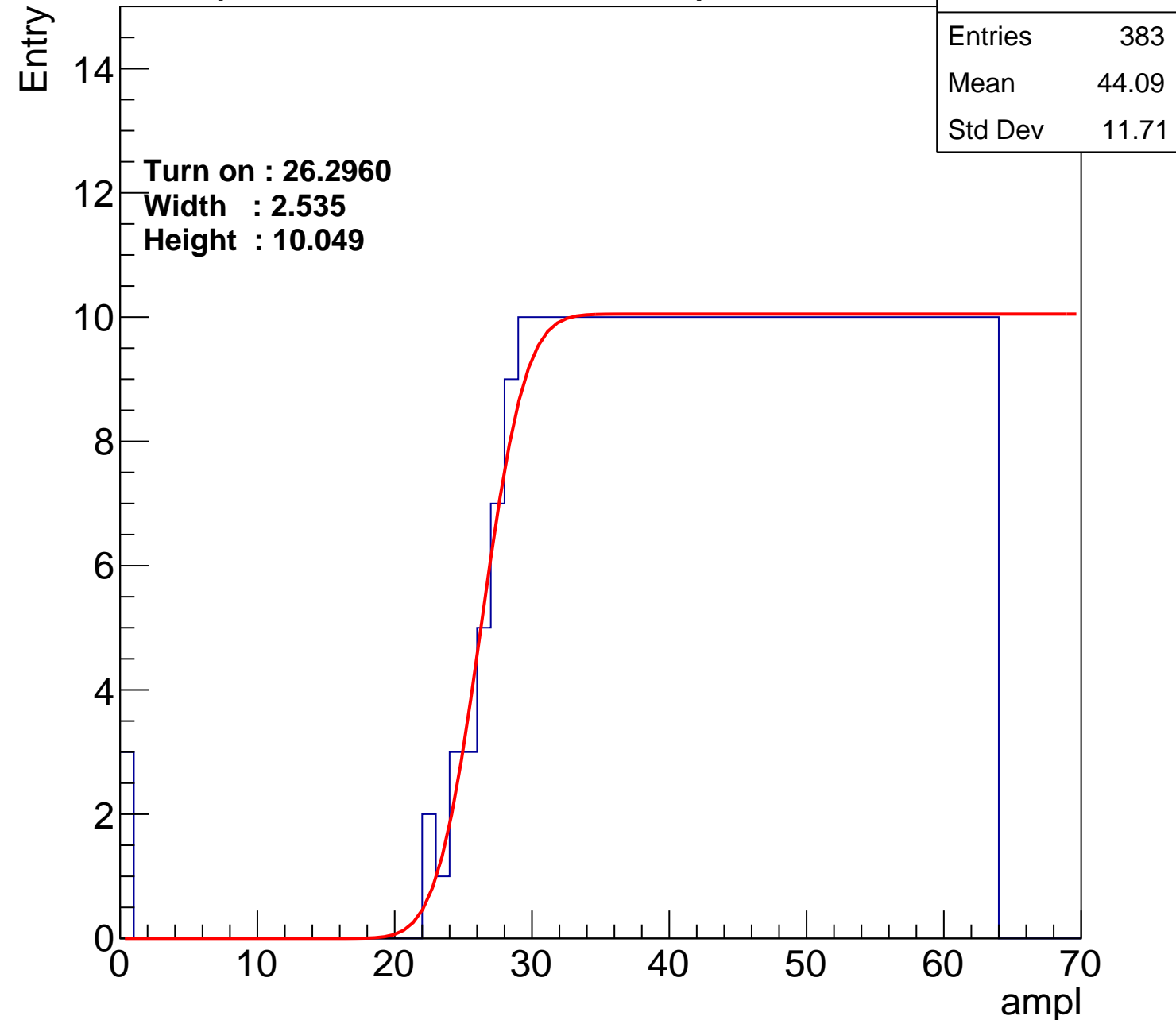
**Width : 2.535**

**Height : 10.049**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch13

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	373
Mean	44.54
Std Dev	11.52

Turn on : 27.0595

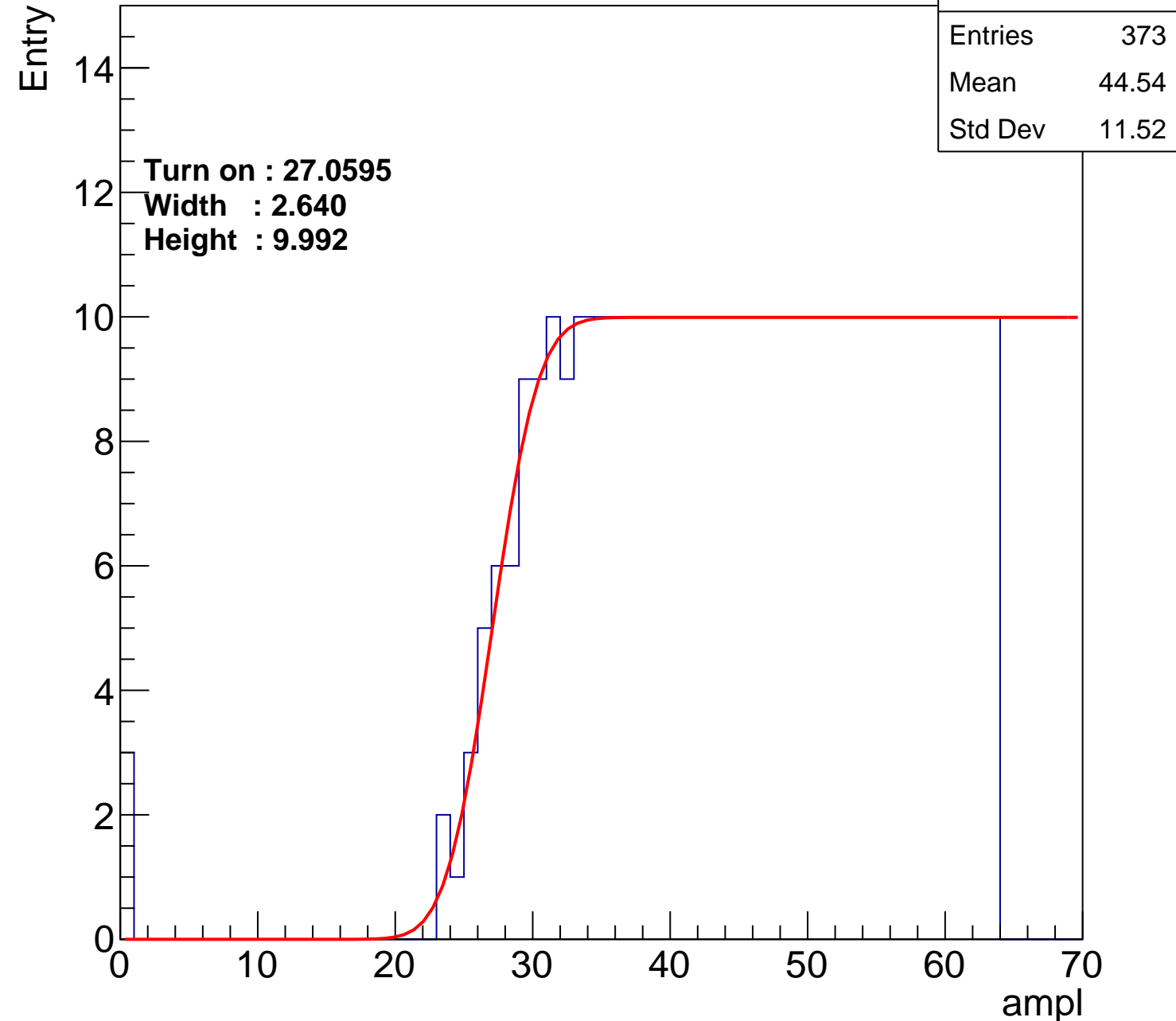
Width : 2.640

Height : 9.992

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch14

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	374
Mean	44.48
Std Dev	11.58

Turn on : 27.2913

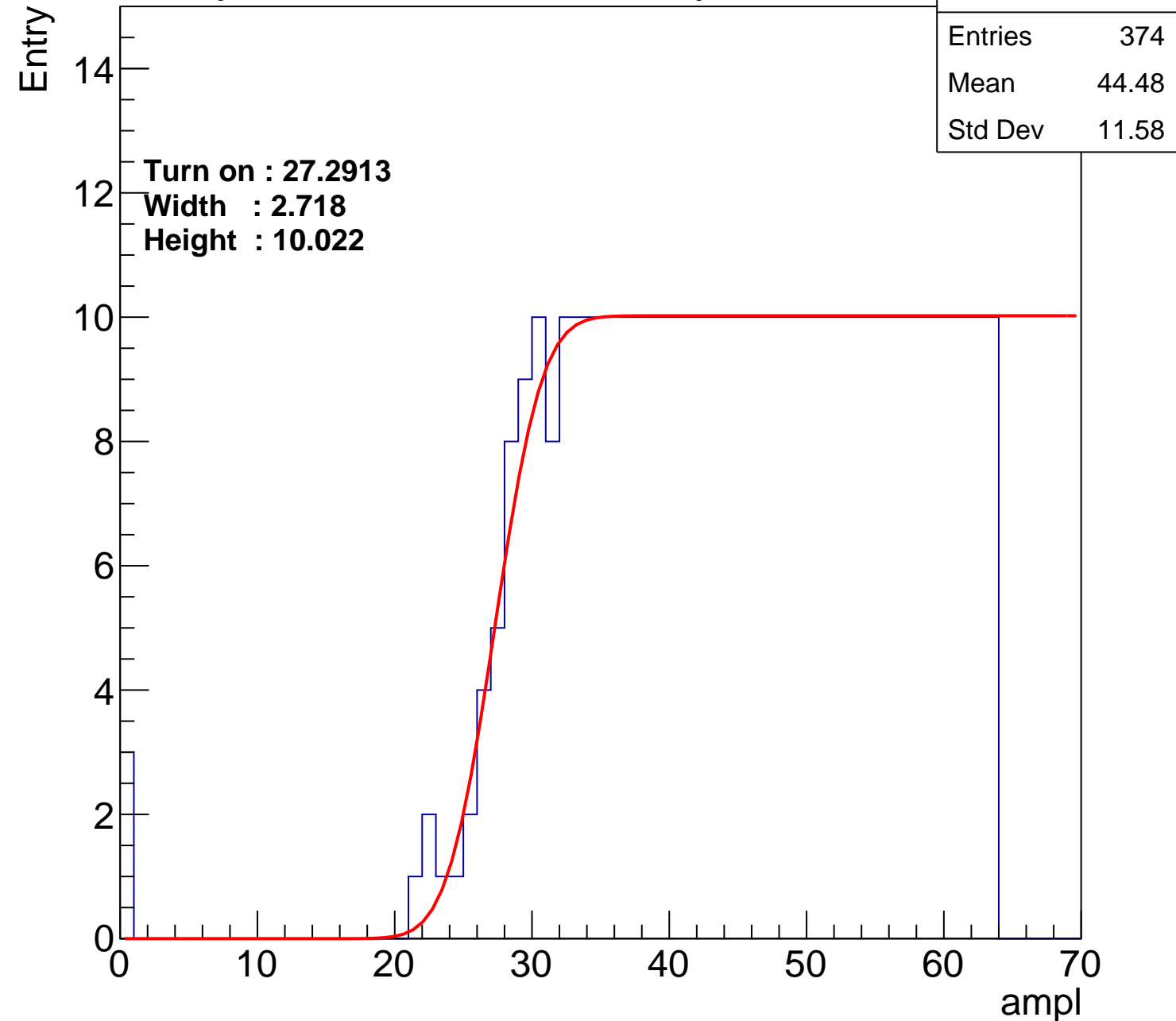
Width : 2.718

Height : 10.022

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L101S, U9-ch15

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	365
Mean	44.82
Std Dev	11.6

**Turn on : 28.2692**

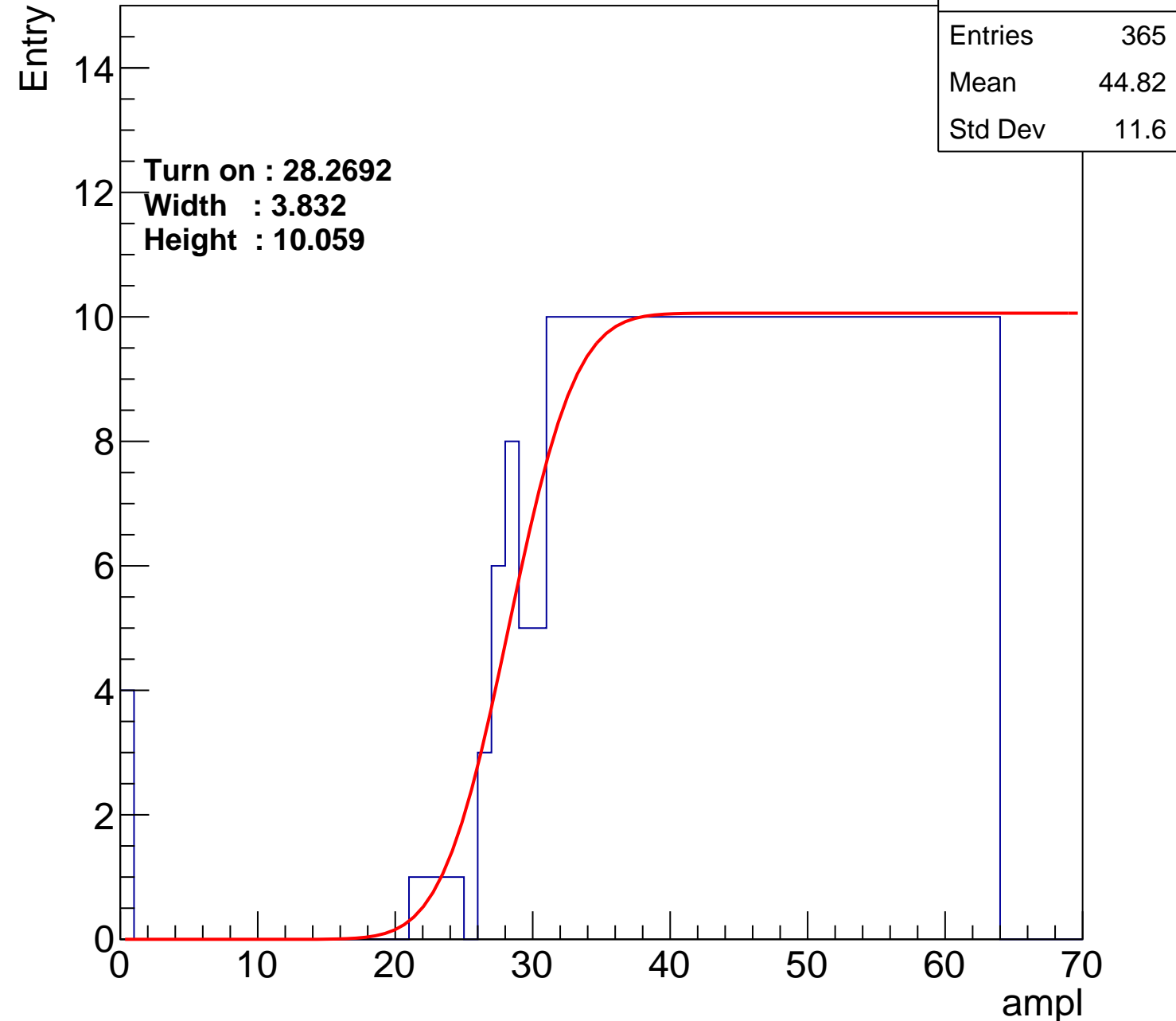
**Width : 3.832**

**Height : 10.059**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch16

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	361
Mean	45.23
Std Dev	10.87

Turn on : 27.9032

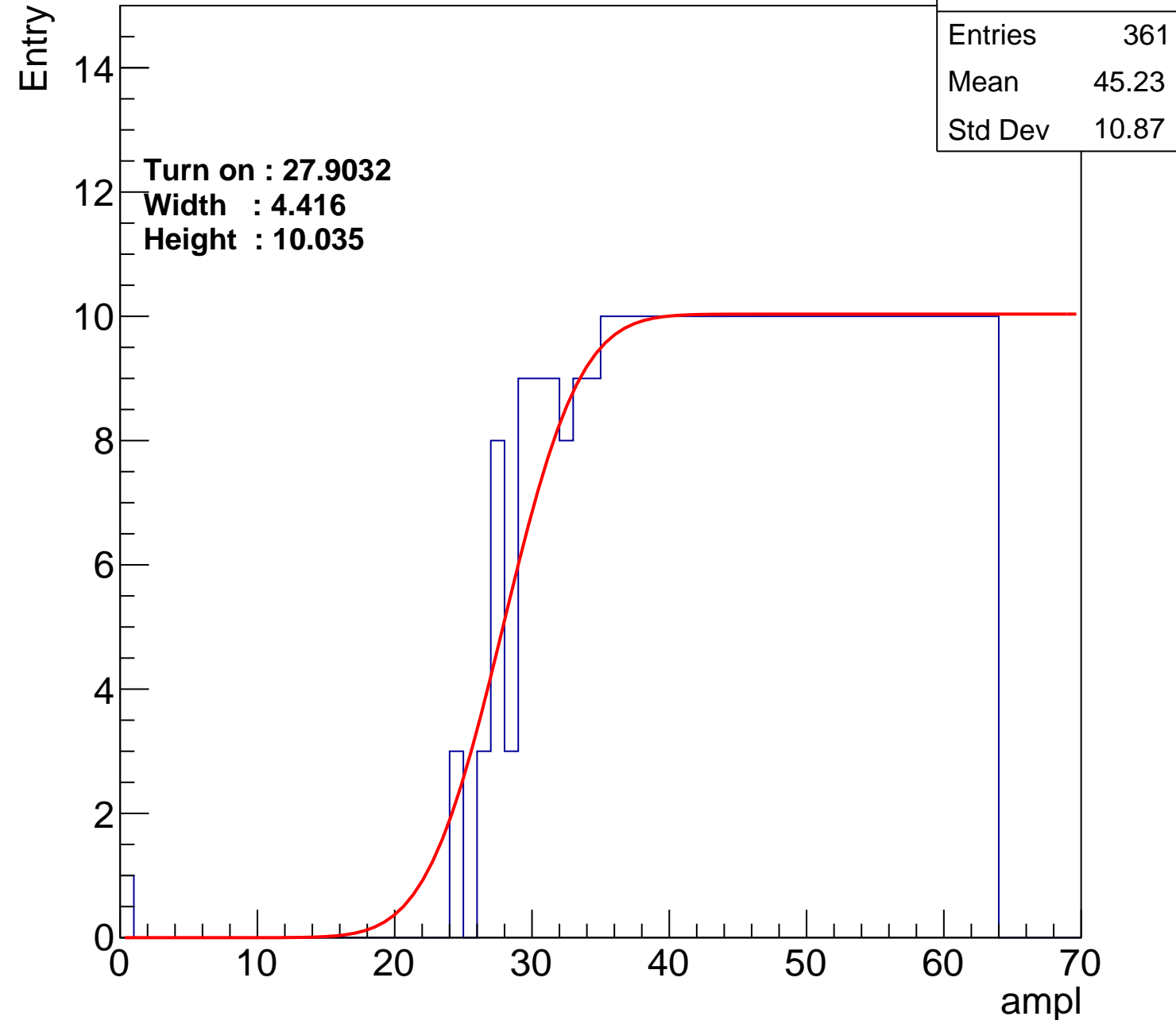
Width : 4.416

Height : 10.035

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch17

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	372
Mean	44.7
Std Dev	11.15

Turn on : 27.2266

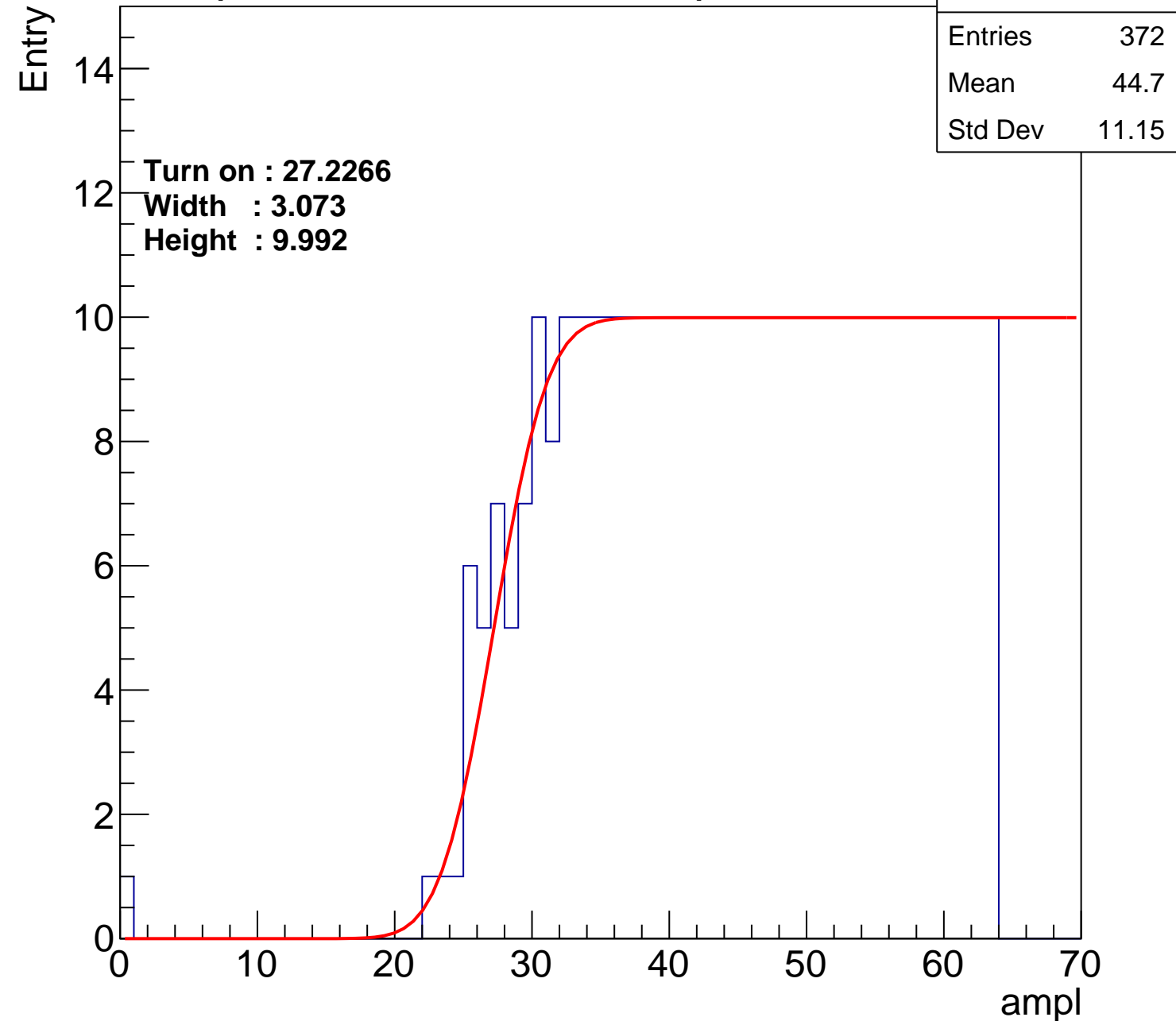
Width : 3.073

Height : 9.992

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch18

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	389
Mean	43.65
Std Dev	12.21

**Turn on : 25.7938**

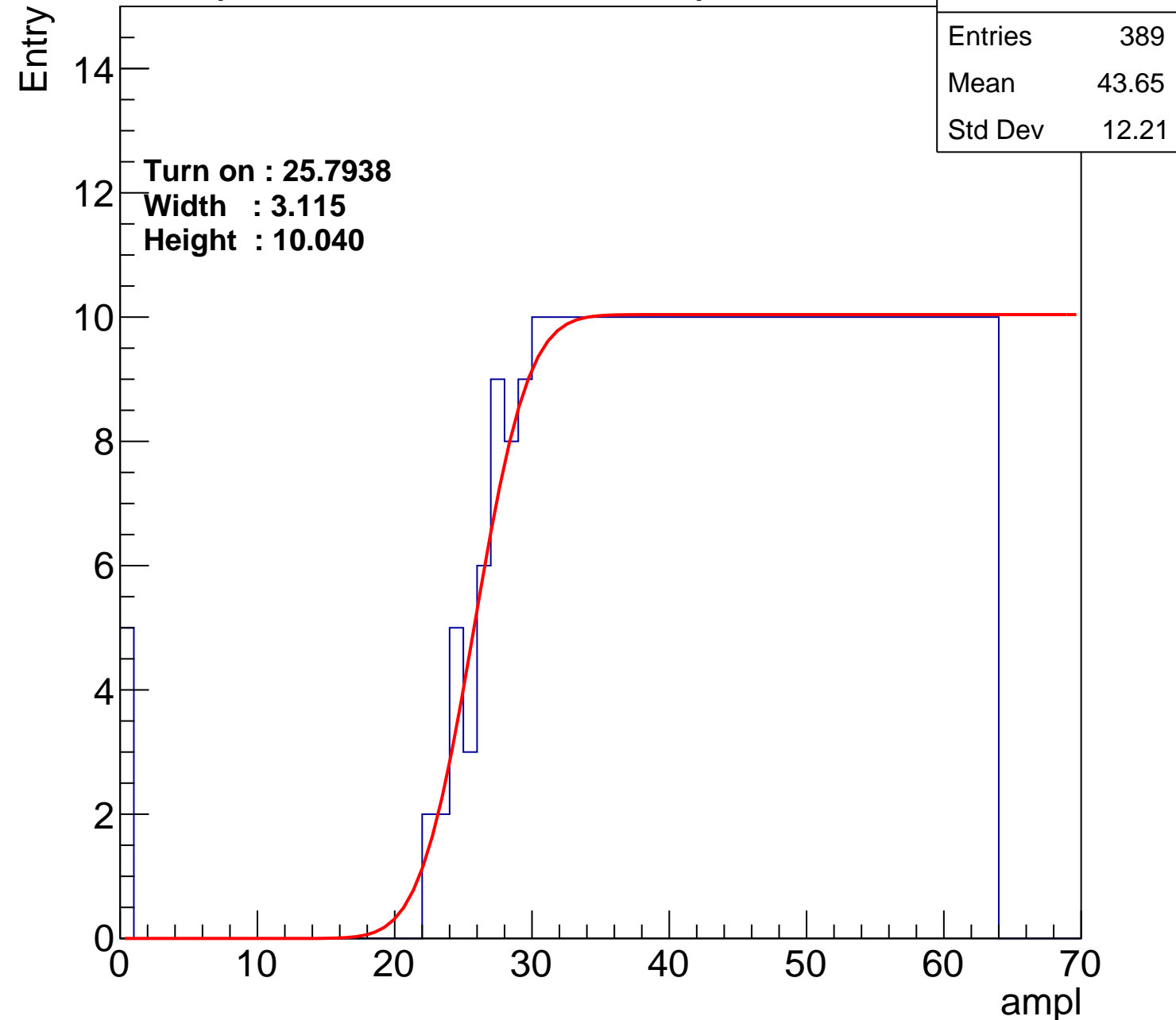
**Width : 3.115**

**Height : 10.040**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch19

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	345
Mean	46.08
Std Dev	10.35

Turn on : 29.4665

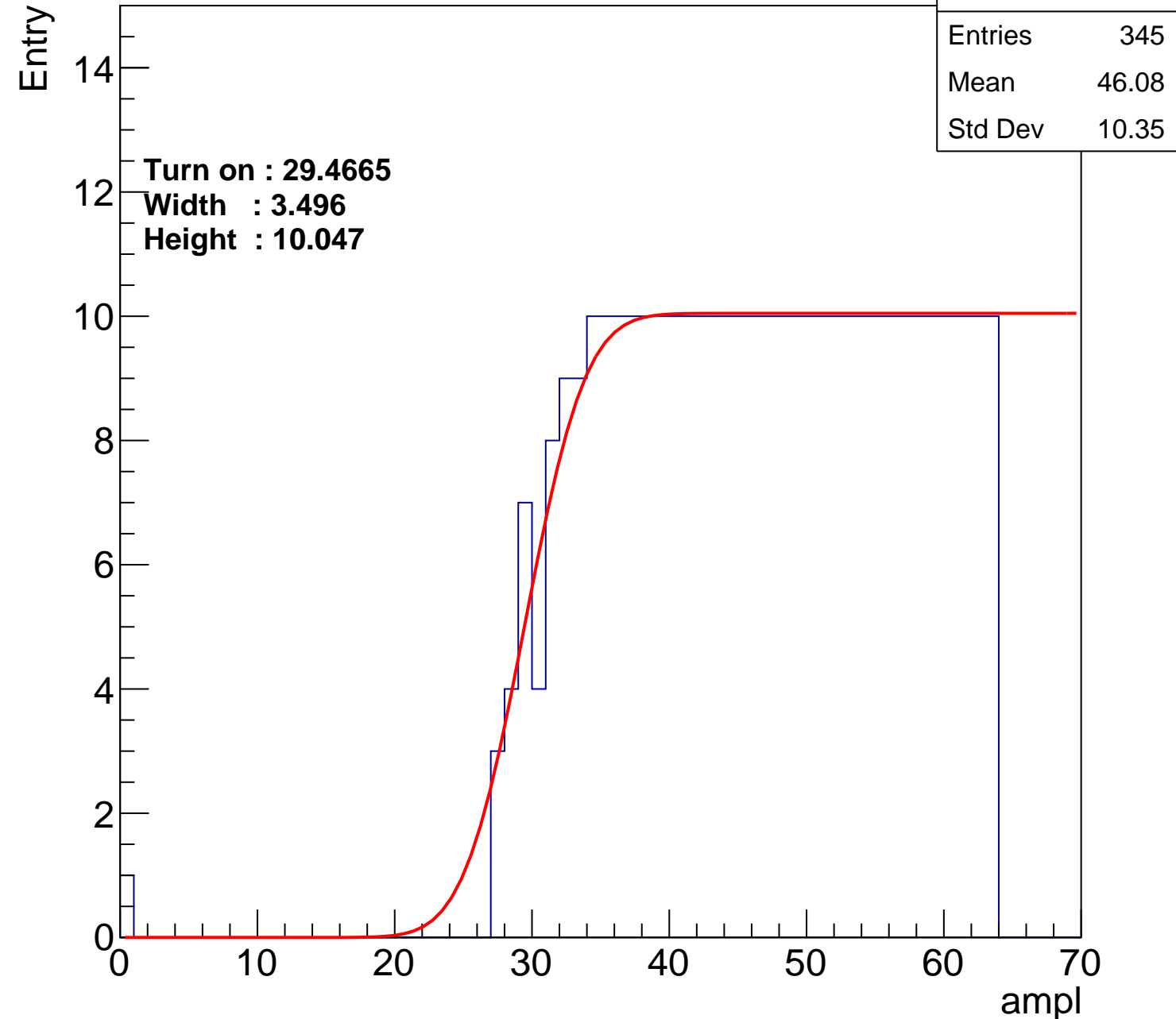
Width : 3.496

Height : 10.047

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch20

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	383
Mean	43.99
Std Dev	11.93

Turn on : 26.4468

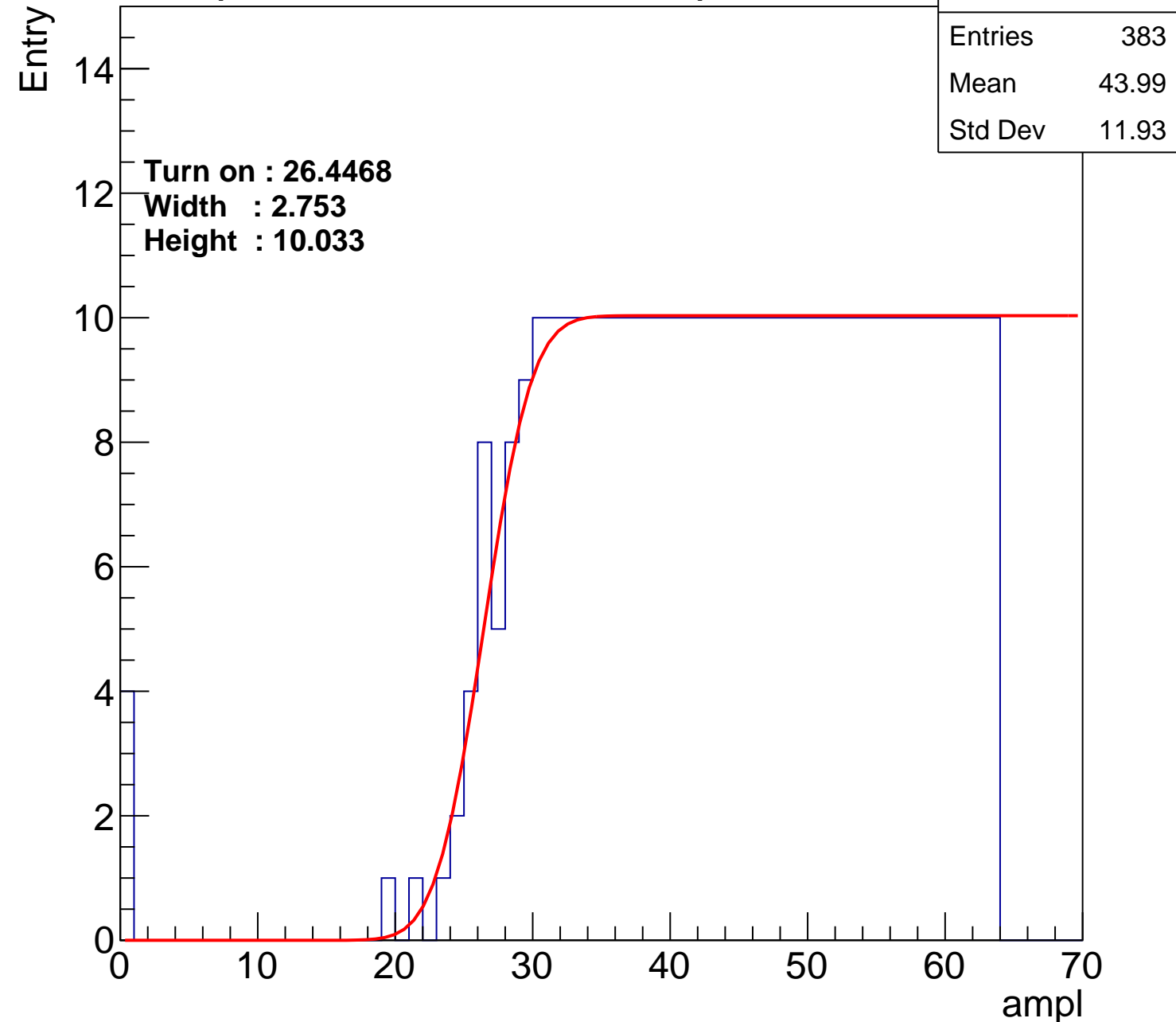
Width : 2.753

Height : 10.033

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch21

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	376
Mean	44.53
Std Dev	11.22

Turn on : 26.7489

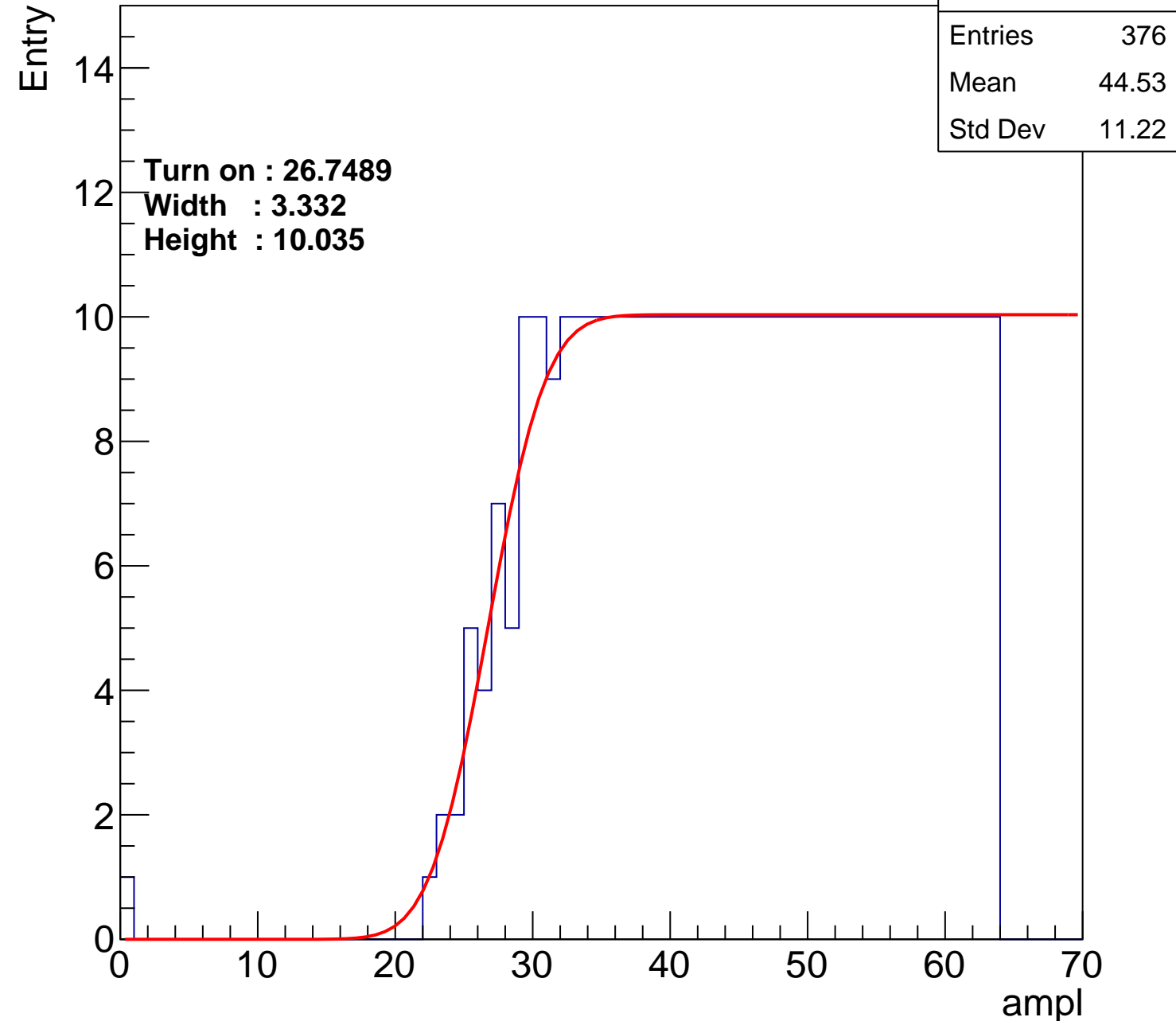
Width : 3.332

Height : 10.035

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch22

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	385
Mean	43.99
Std Dev	11.68

Turn on : 25.4449

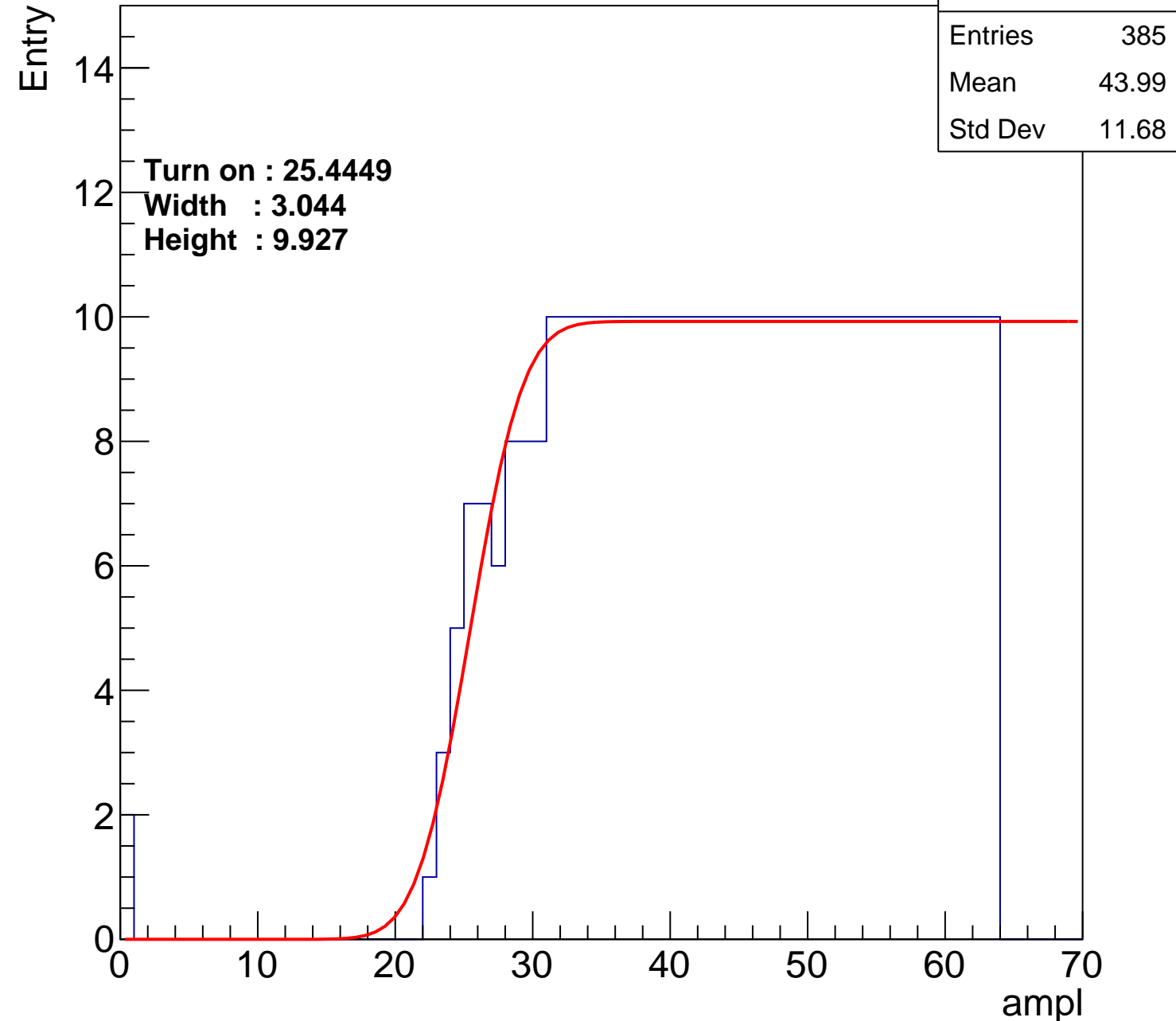
Width : 3.044

Height : 9.927

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L101S, U9-ch23

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	377
Mean	44.31
Std Dev	11.67

Turn on : 26.3146

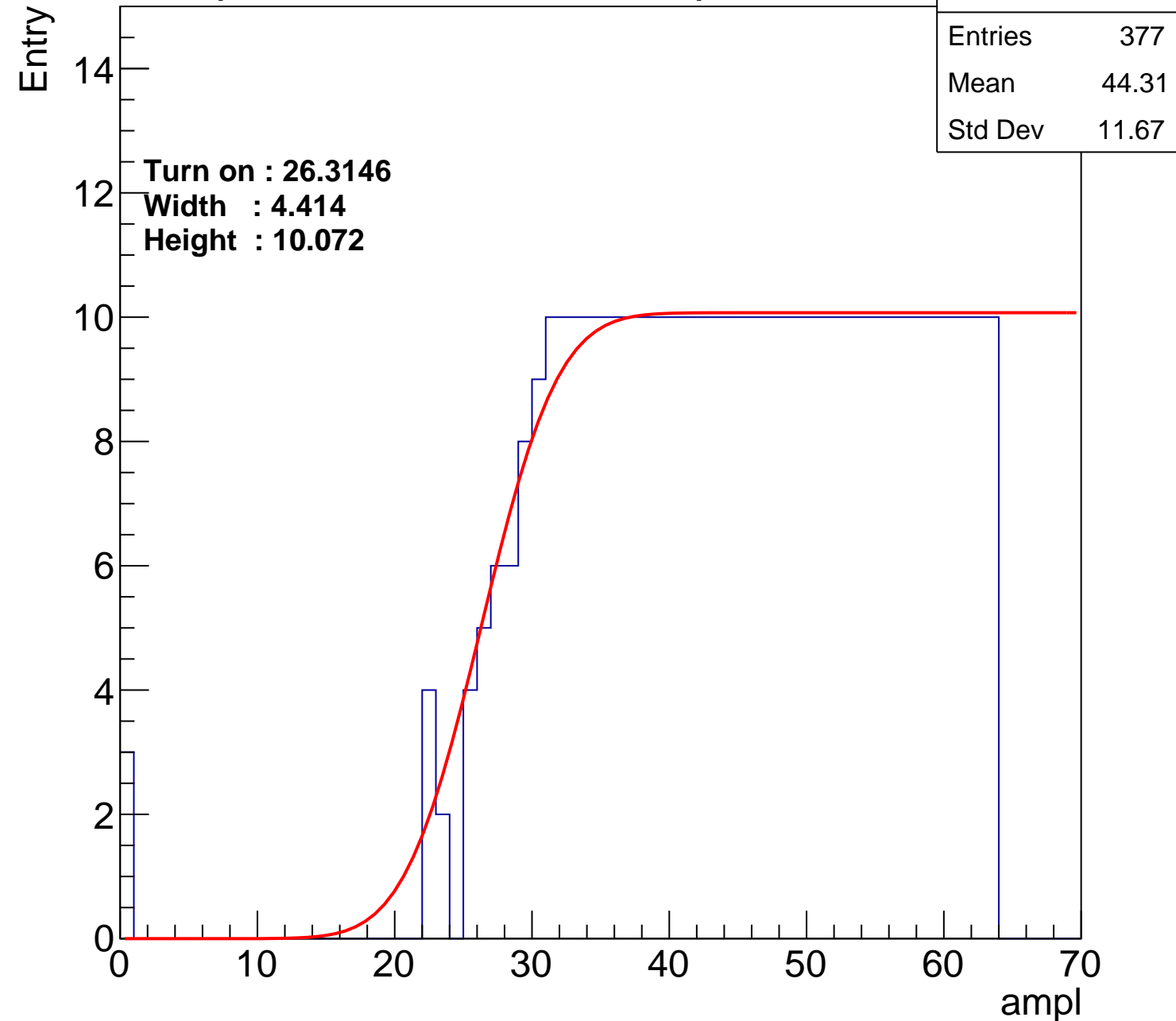
Width : 4.414

Height : 10.072

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch24

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	384
Mean	44.02
Std Dev	11.77

Turn on : 26.2842

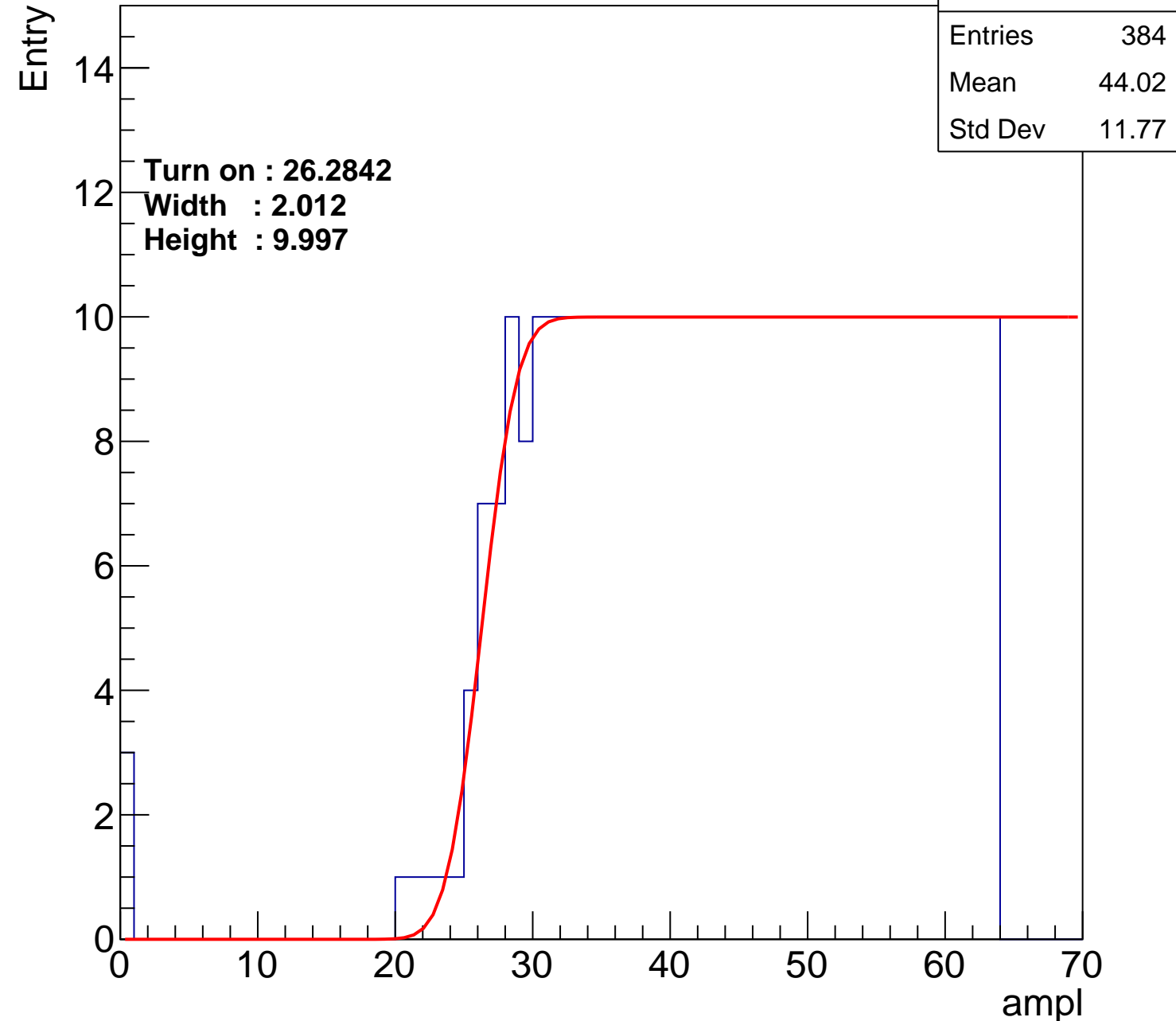
Width : 2.012

Height : 9.997

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch25

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	371
Mean	44.51
Std Dev	11.84

**Turn on : 27.2809**

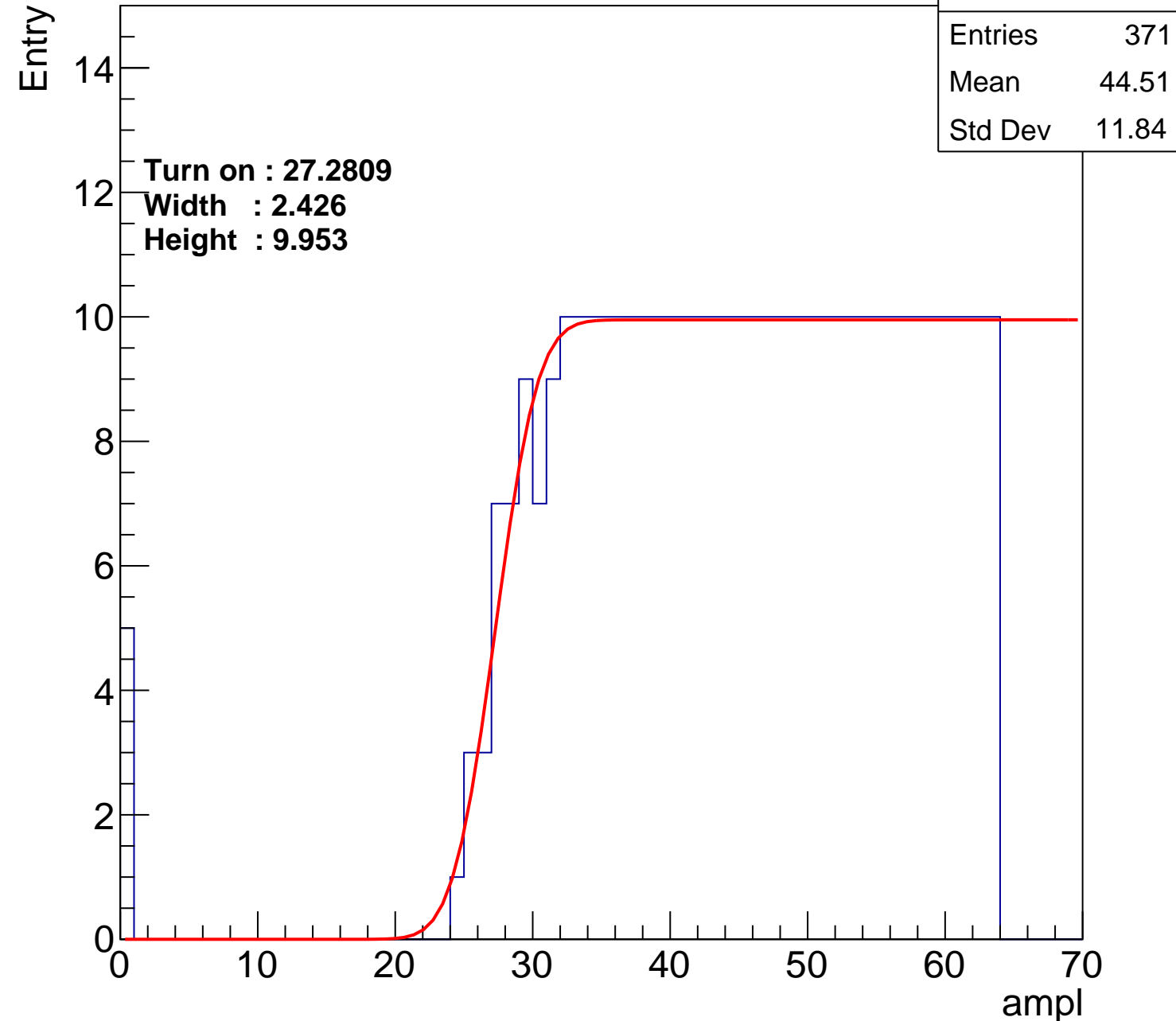
**Width : 2.426**

**Height : 9.953**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch26

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	375
Mean	44.49
Std Dev	11.41

Turn on : 26.8415

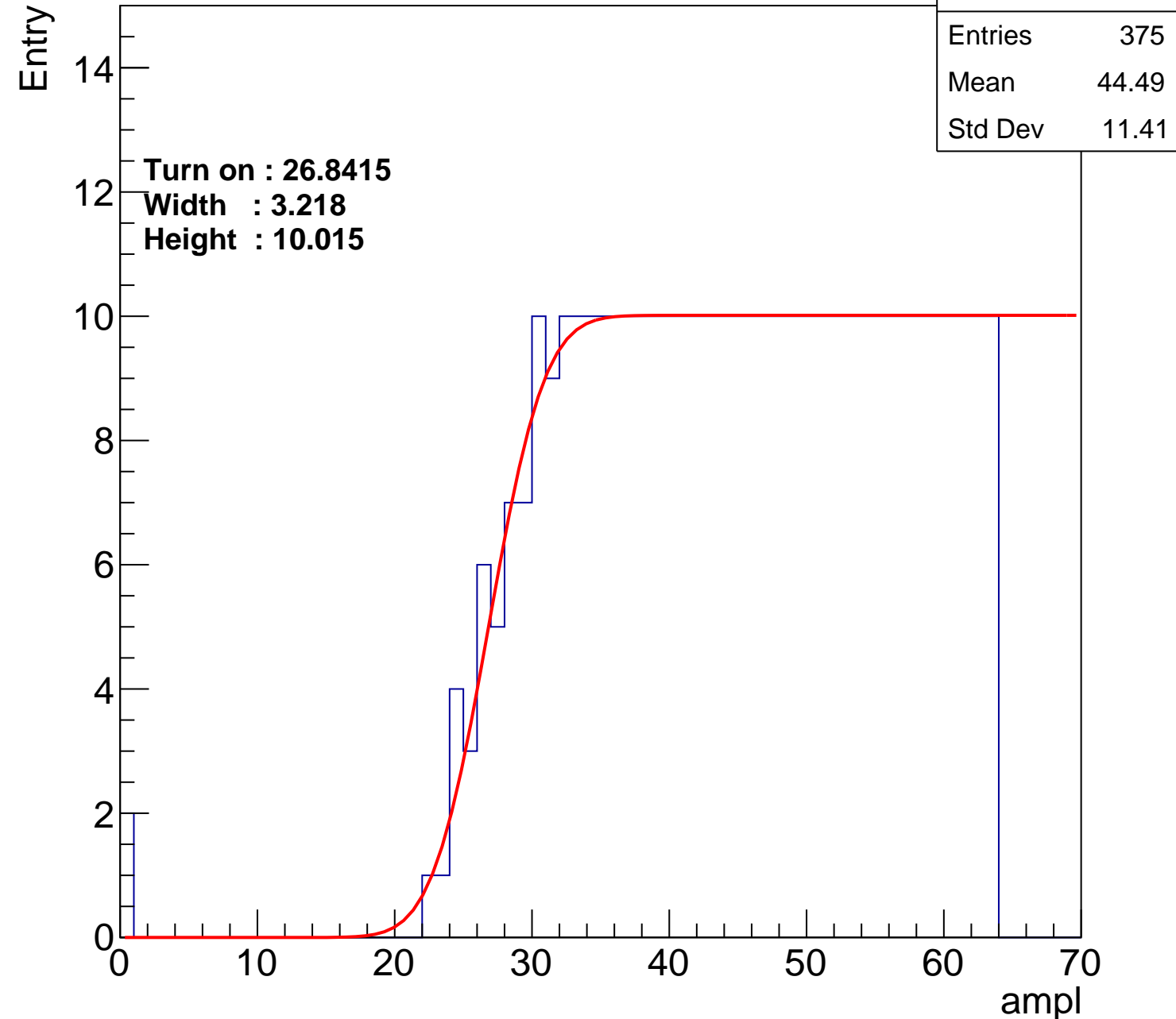
Width : 3.218

Height : 10.015

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch27

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	365
Mean	44.93
Std Dev	11.33

Turn on : 27.4121

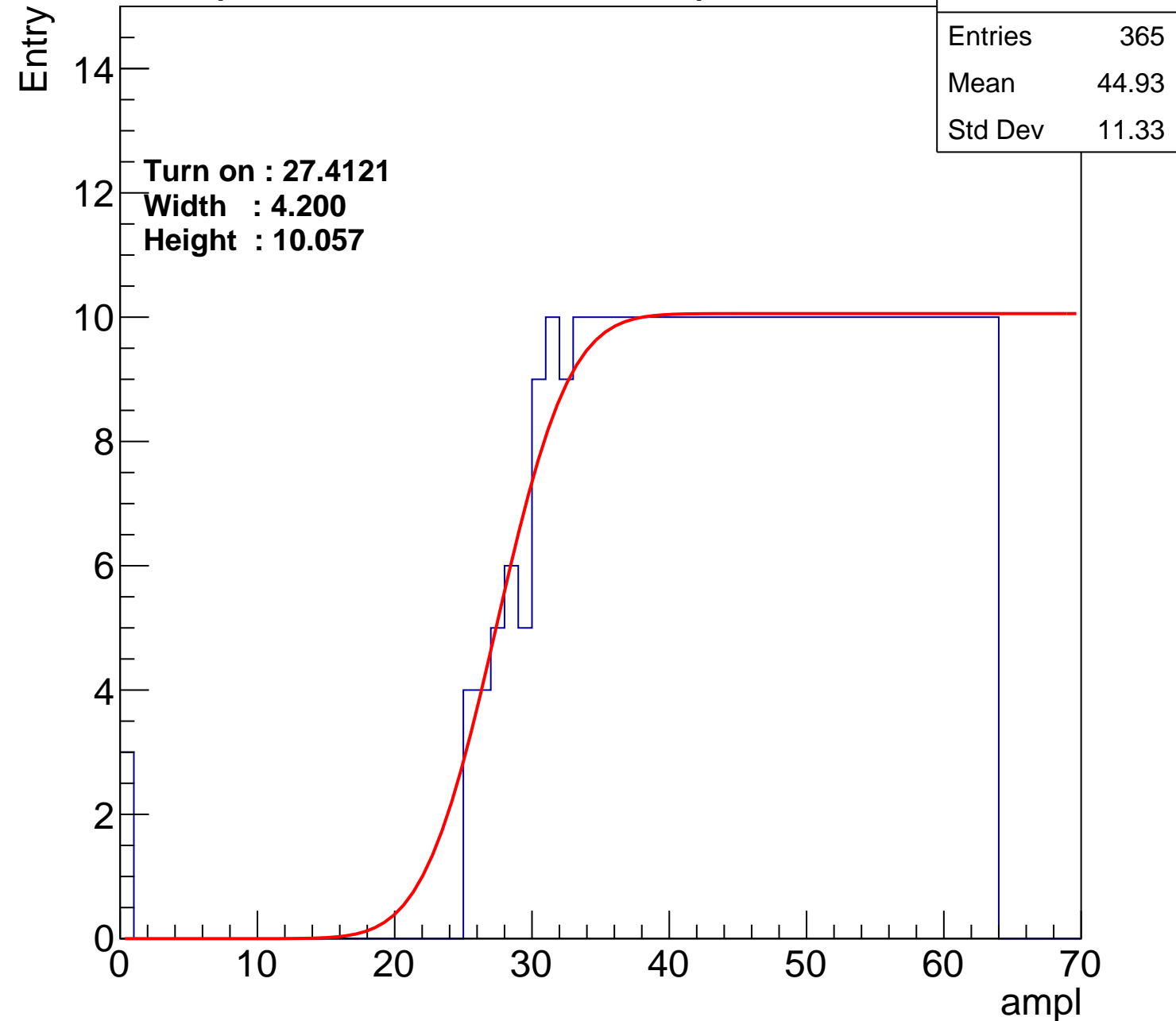
Width : 4.200

Height : 10.057

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch28

calib\_packv5\_042523\_0143.root, FC#0, port D2

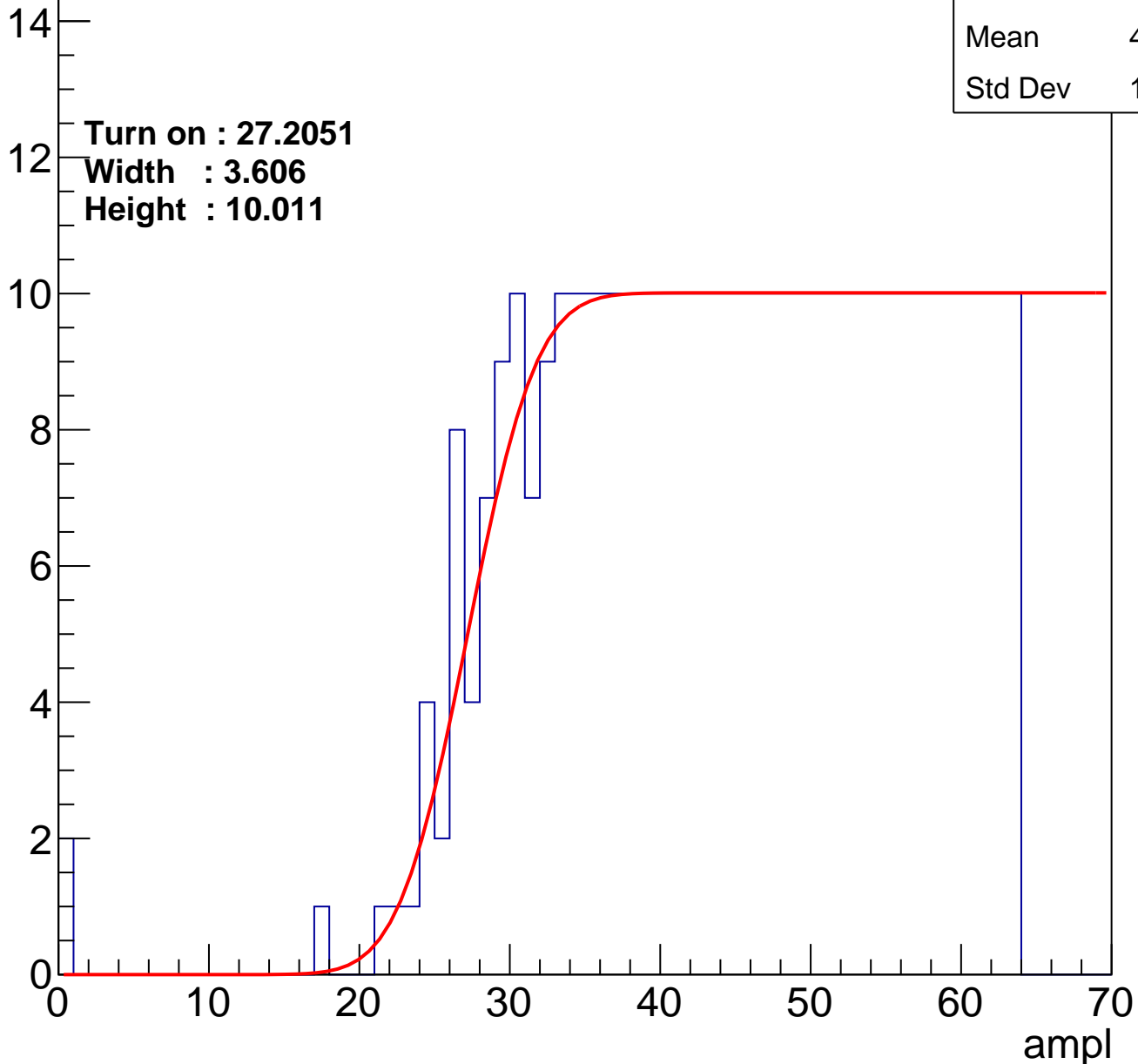
Entries	376
Mean	44.38
Std Dev	11.54

Turn on : 27.2051

Width : 3.606

Height : 10.011

Entry



# B1L101S, U9-ch29

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	363
Mean	45.07
Std Dev	11.12

**Turn on : 27.6031**

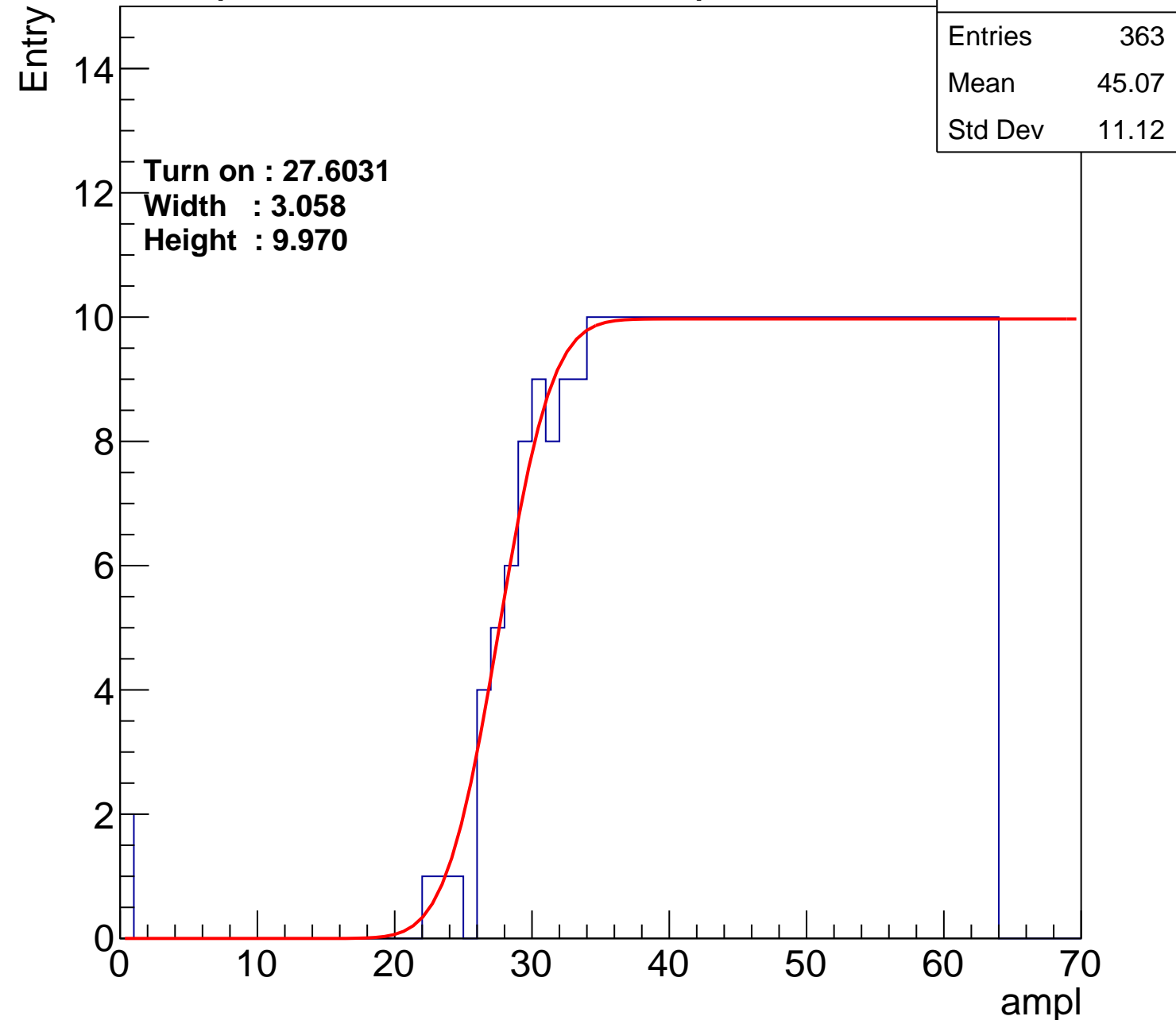
**Width : 3.058**

**Height : 9.970**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch30

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	398
Mean	43.26
Std Dev	12.29

Turn on : 25.4016

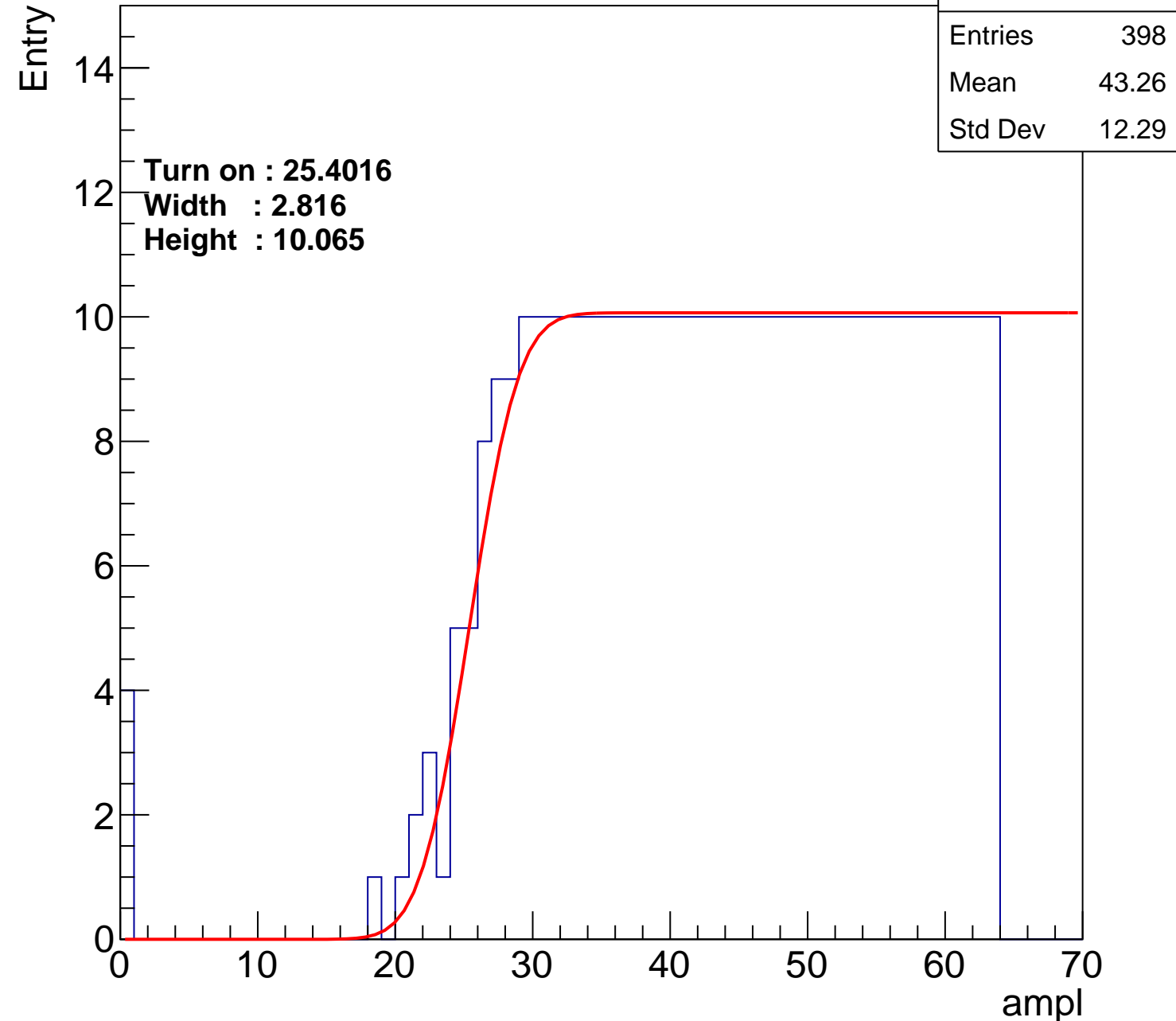
Width : 2.816

Height : 10.065

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L101S, U9-ch31

**calib\_packv5\_042523\_0143.root, FC#0, port D2**

Entries	370
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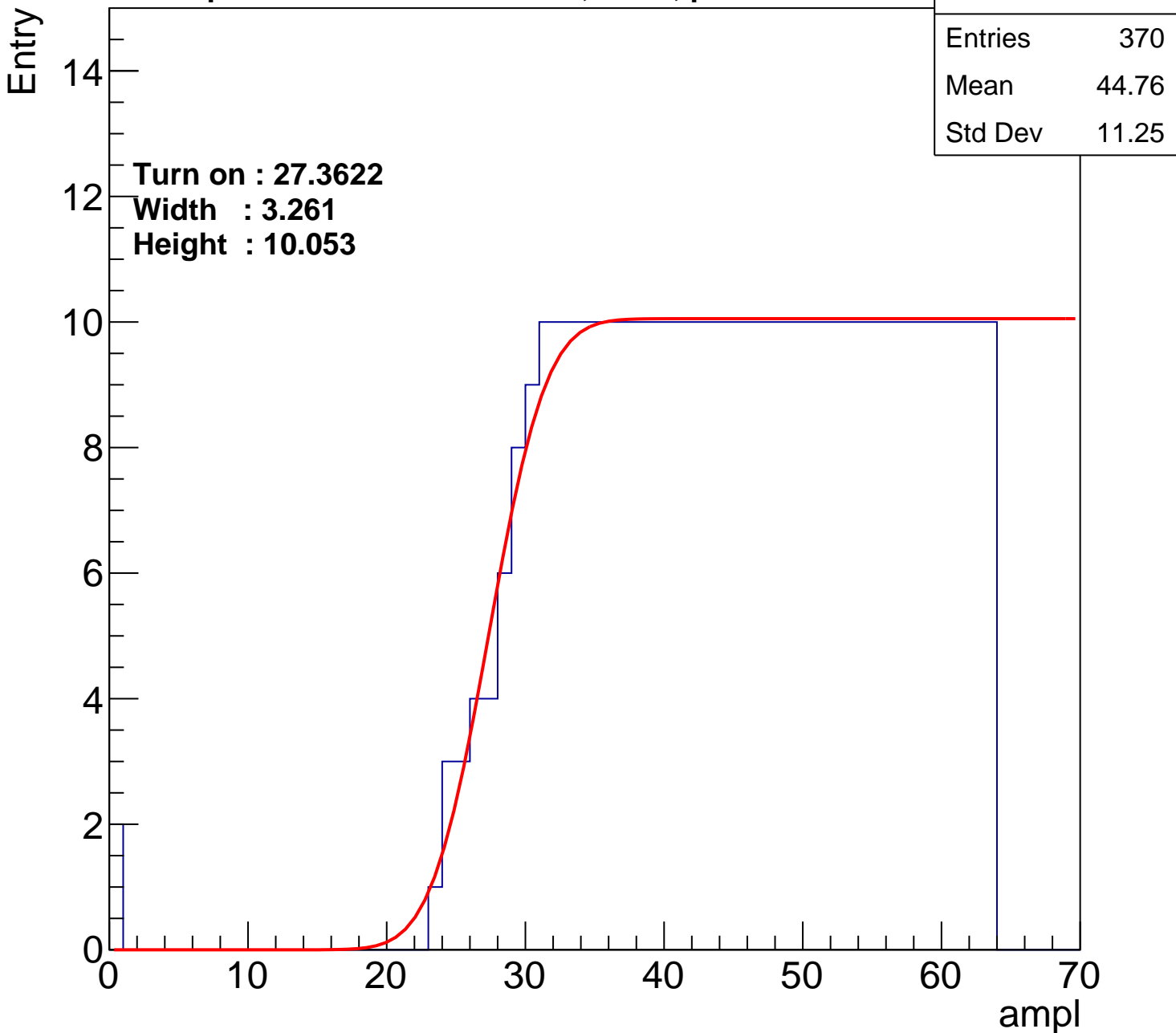
Mean	44.76
------	-------

Std Dev	11.25
---------	-------

**Turn on : 27.3622**

**Width : 3.261**

**Height : 10.053**



# B1L101S, U9-ch32

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	384
Mean	43.83
Std Dev	12.19

Turn on : 26.1799

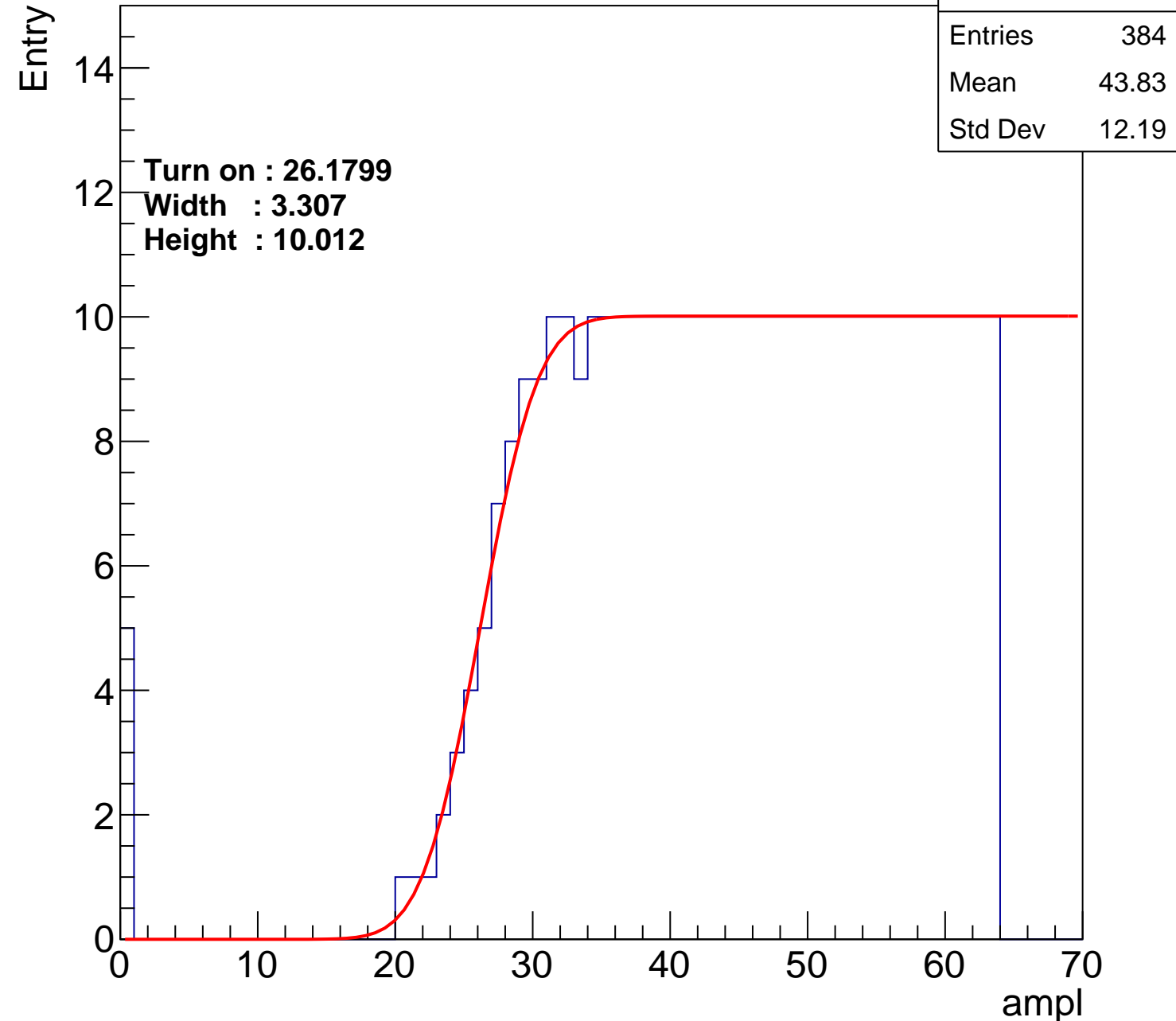
Width : 3.307

Height : 10.012

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch33

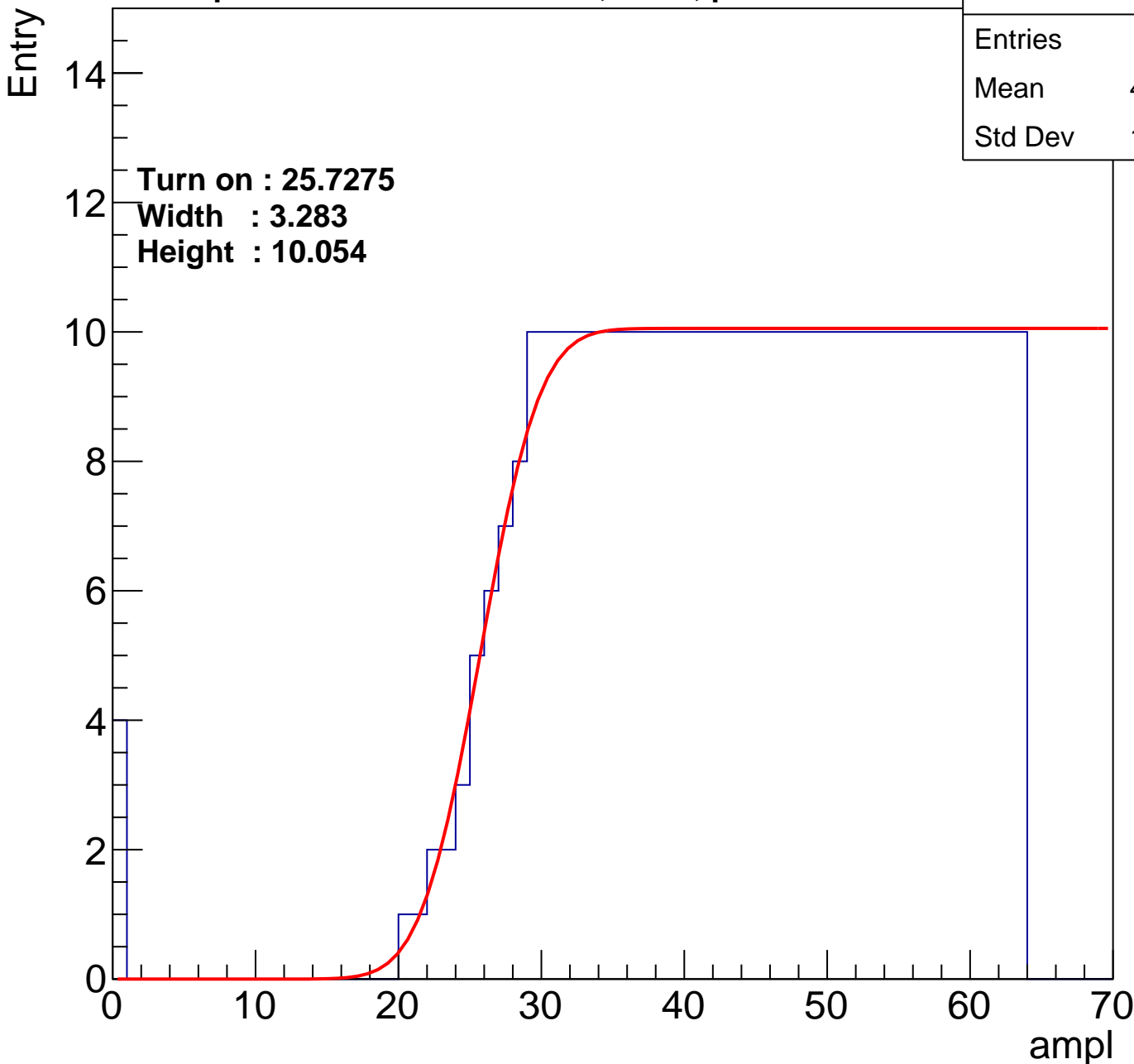
**calib\_packv5\_042523\_0143.root, FC#0, port D2**

Entries	389
Mean	43.69
Std Dev	12.08

**Turn on : 25.7275**

**Width : 3.283**

**Height : 10.054**



# B1L101S, U9-ch34

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	370
Mean	44.65
Std Dev	11.5

Turn on : 27.4349

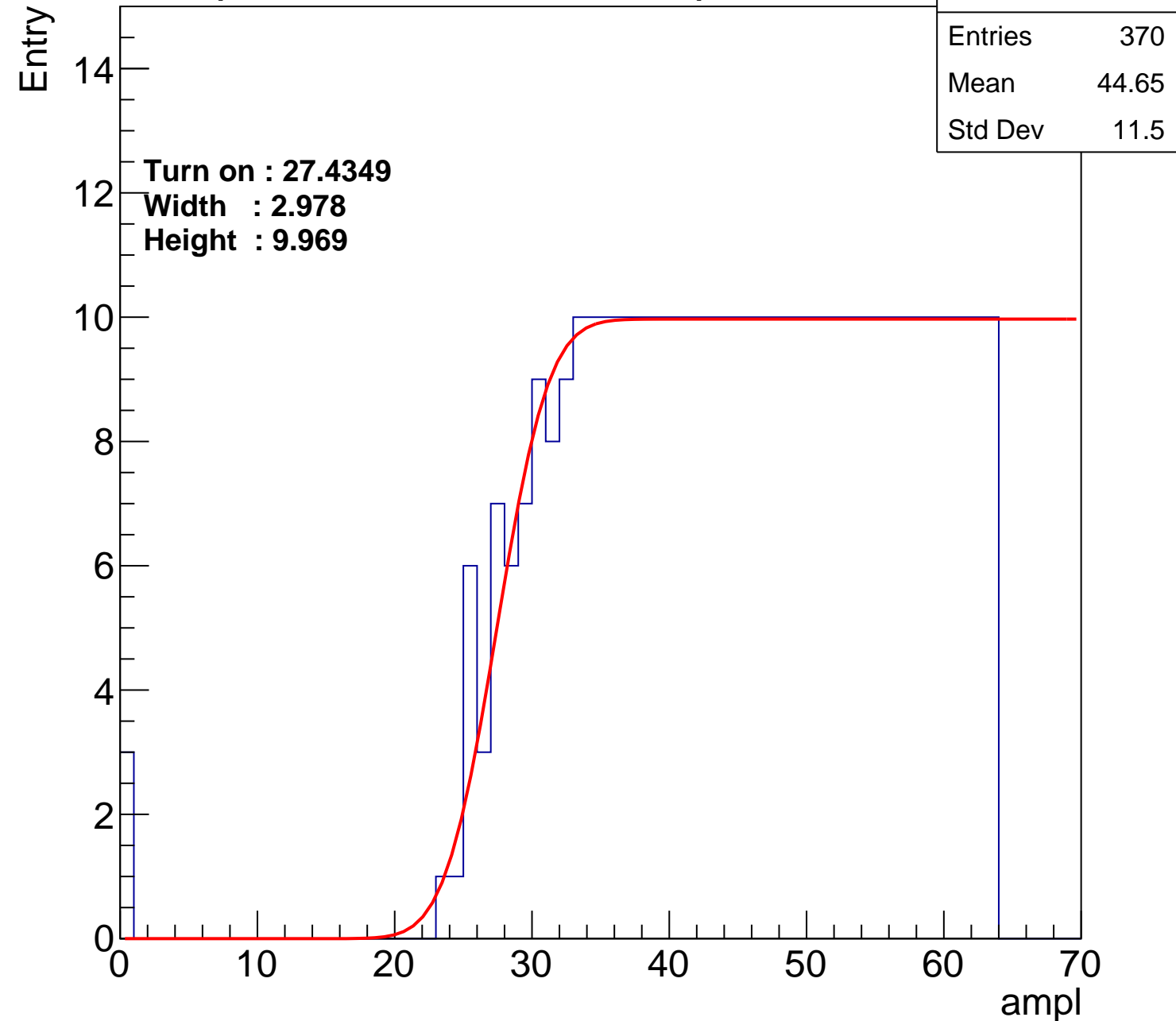
Width : 2.978

Height : 9.969

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch35

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	367
Mean	45.05
Std Dev	10.95

Turn on : 27.2017

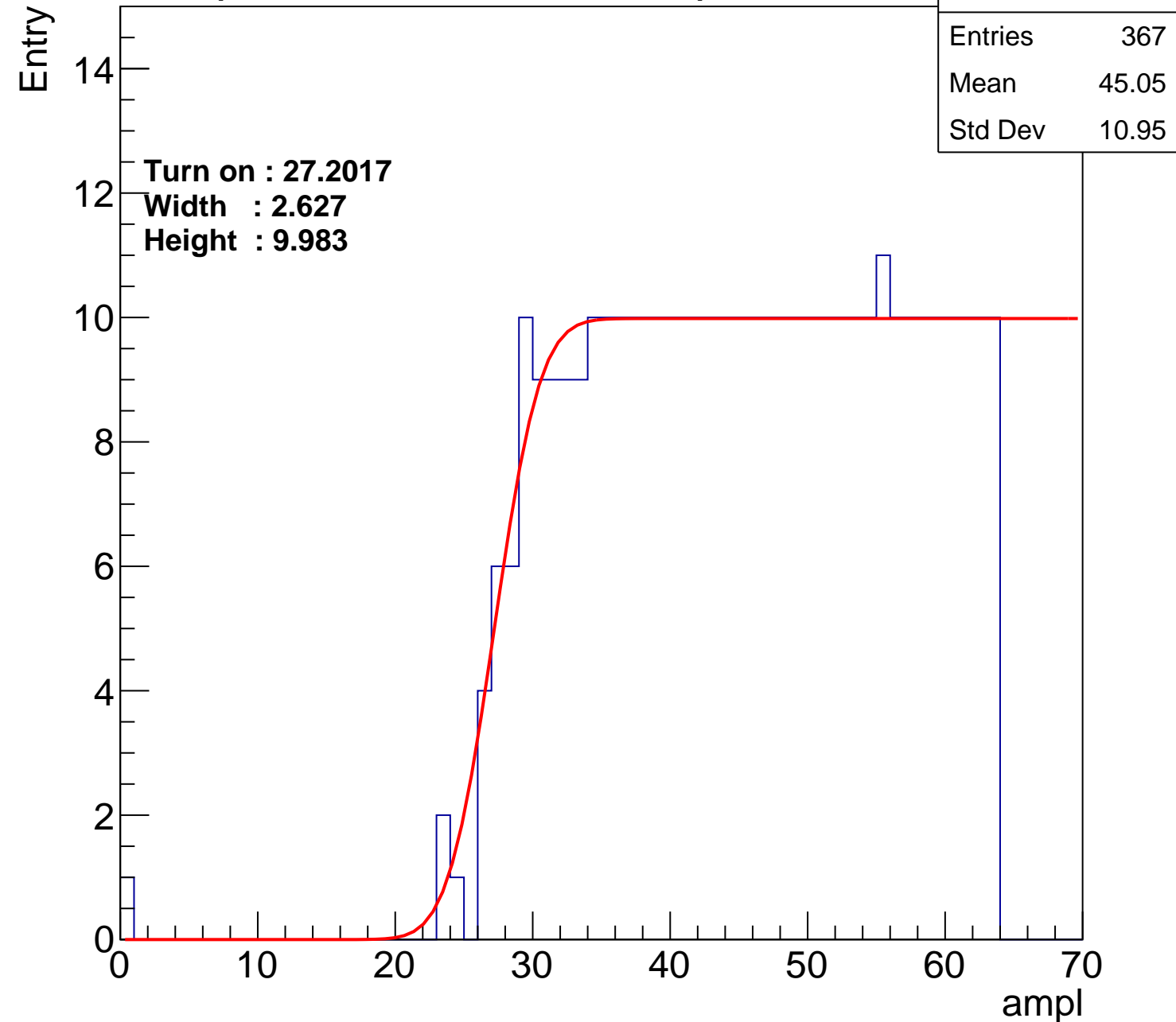
Width : 2.627

Height : 9.983

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch36

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	388
Mean	43.88
Std Dev	11.69

**Turn on : 24.7727**

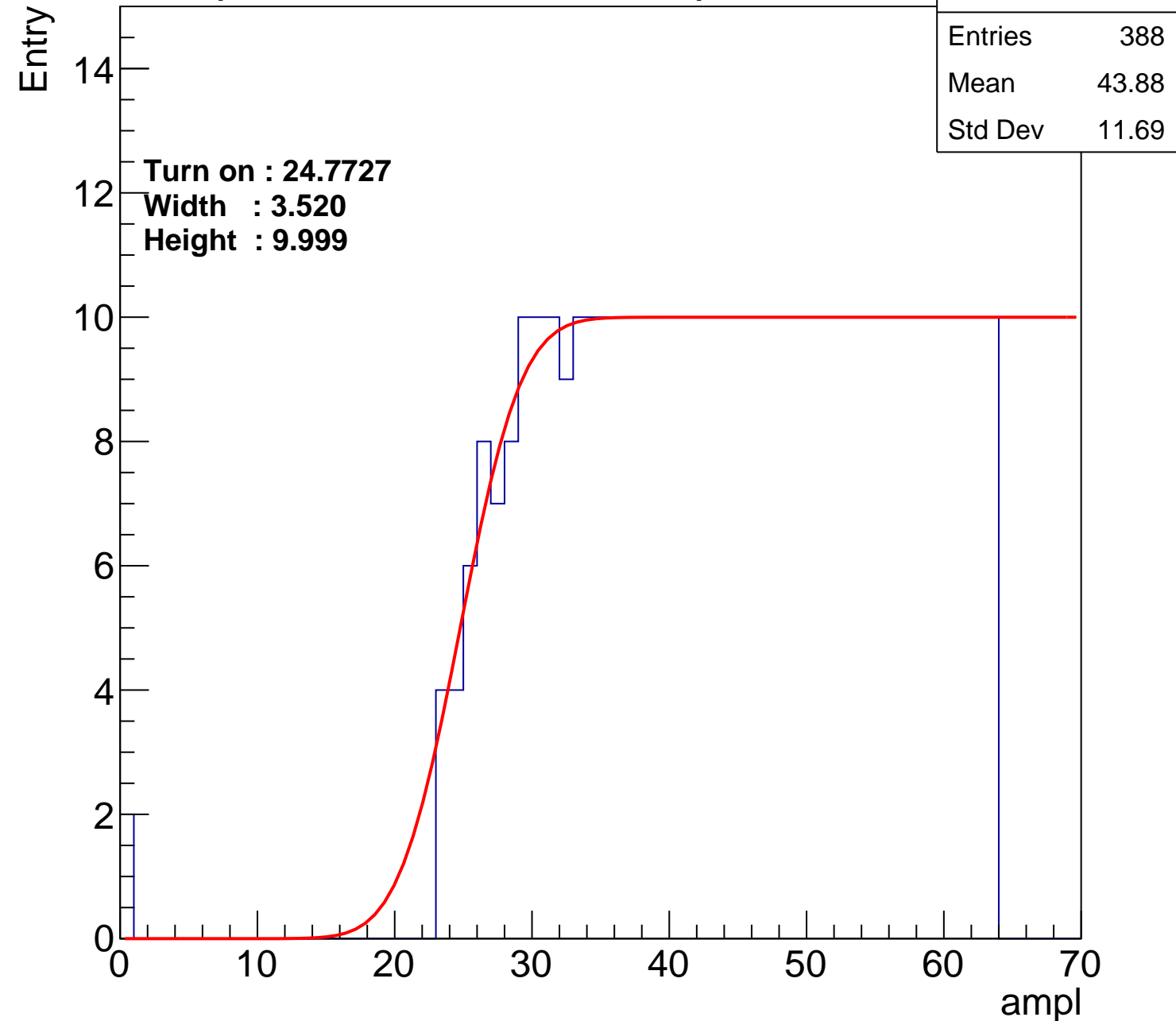
**Width : 3.520**

**Height : 9.999**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch37

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	377
Mean	44.37
Std Dev	11.5

Turn on : 27.0641

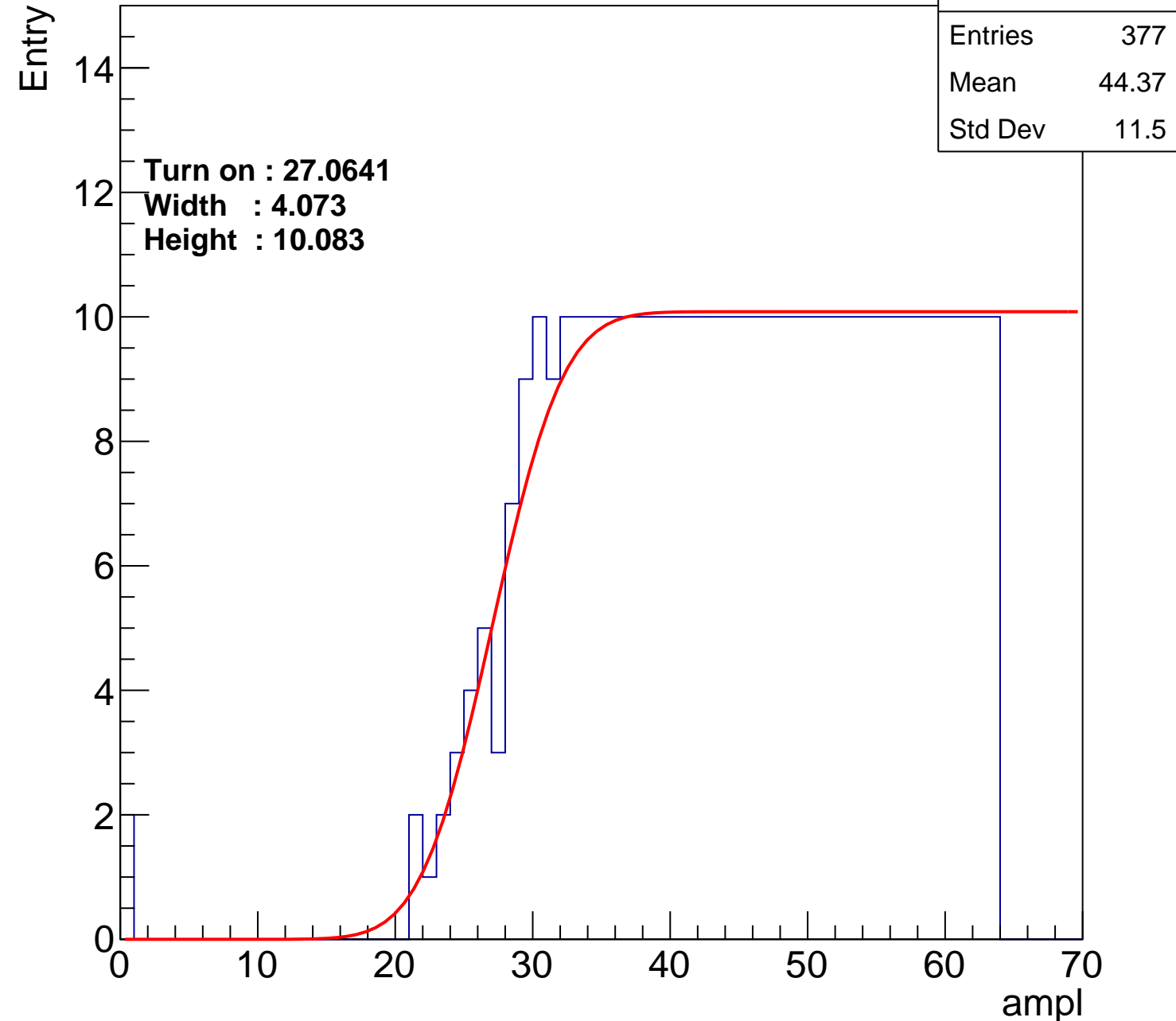
Width : 4.073

Height : 10.083

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch38

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	376
Mean	44.36
Std Dev	11.72

**Turn on : 26.8258**

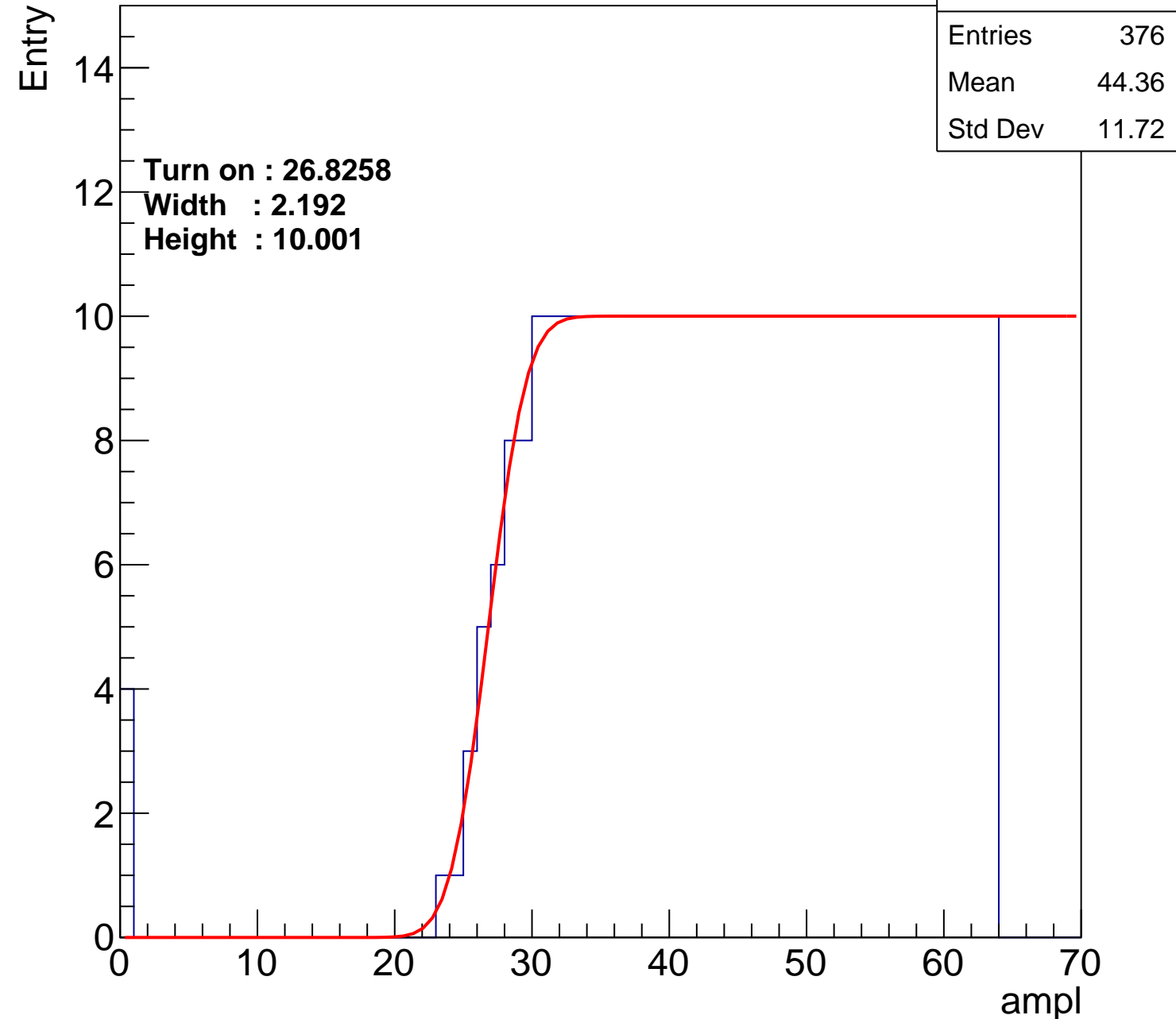
**Width : 2.192**

**Height : 10.001**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L101S, U9-ch39

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	379
Mean	44.1
Std Dev	12.05

Turn on : 26.5026

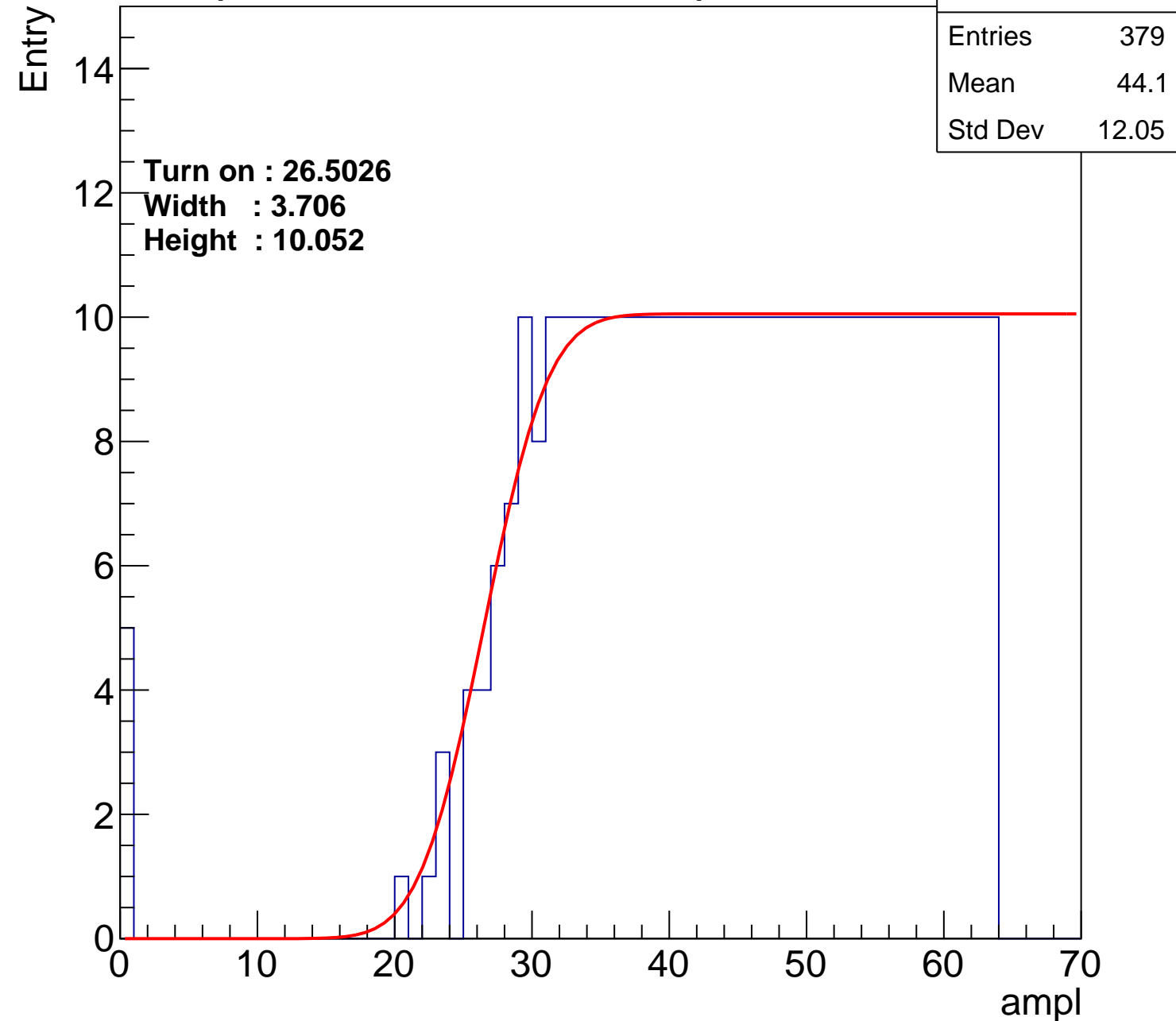
Width : 3.706

Height : 10.052

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch40

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	392
Mean	43.66
Std Dev	11.85

**Turn on : 25.6308**

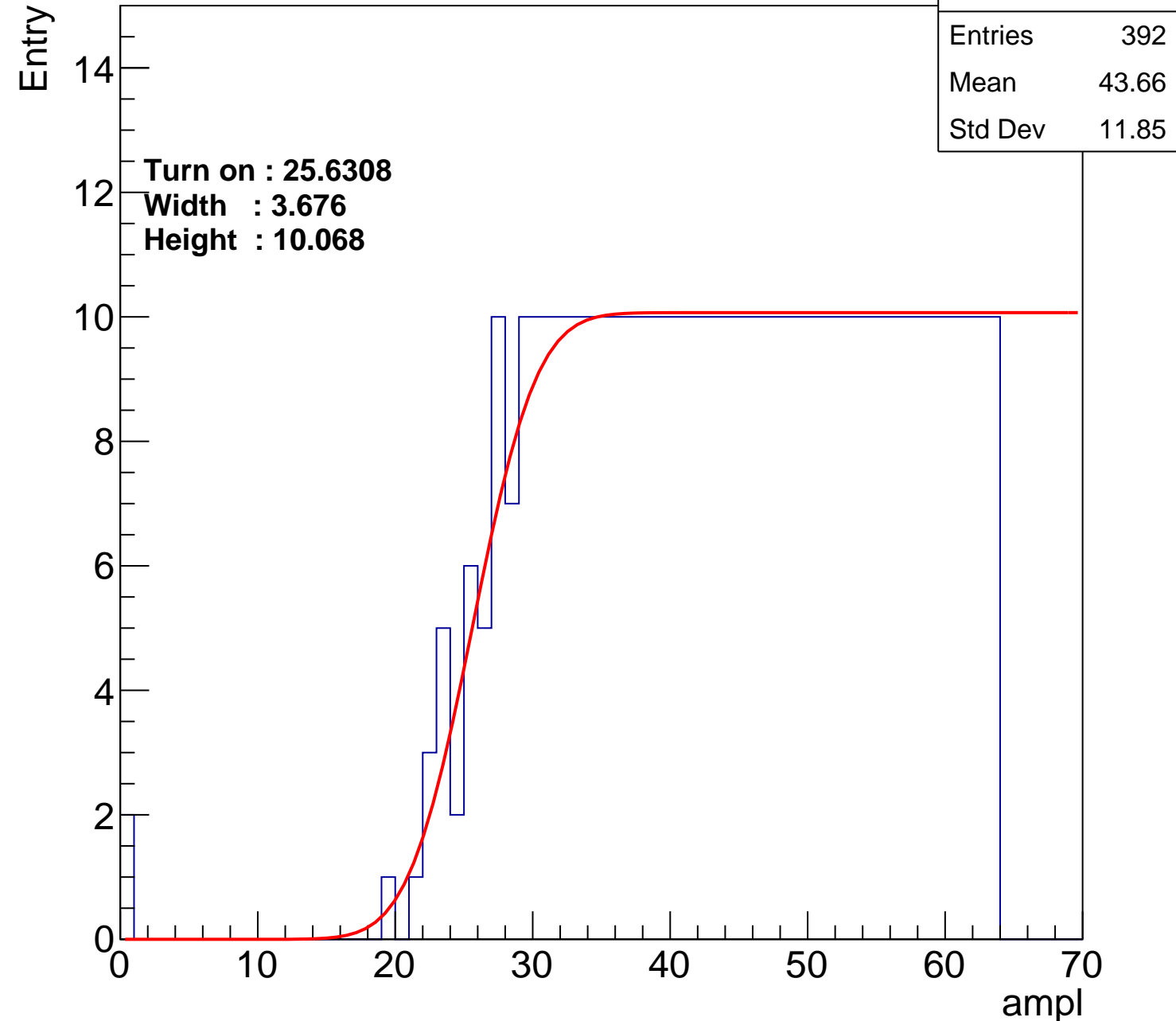
**Width : 3.676**

**Height : 10.068**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch41

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	386
Mean	43.97
Std Dev	11.66

Turn on : 25.7187

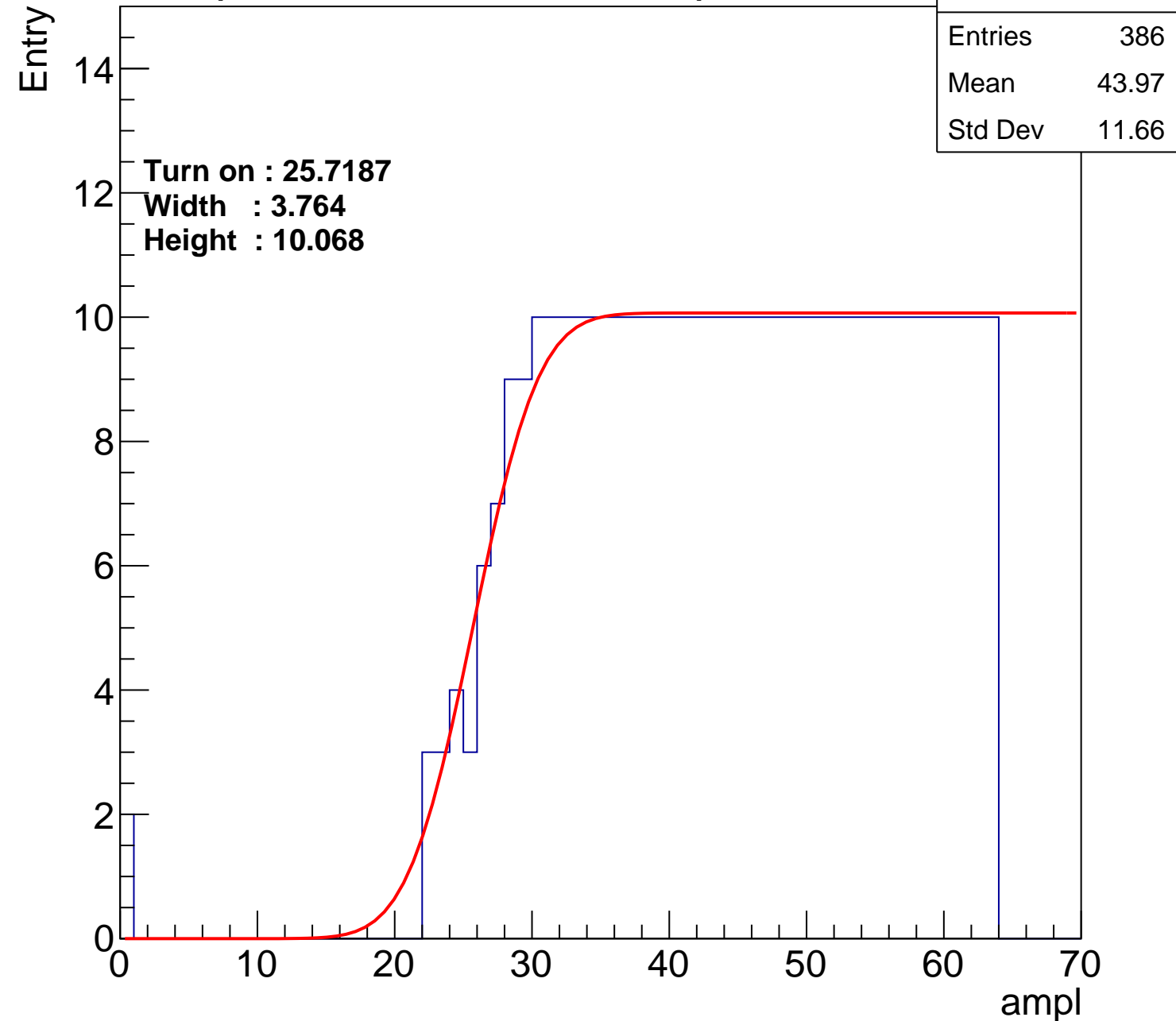
Width : 3.764

Height : 10.068

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch42

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	367
Mean	44.91
Std Dev	11.17

**Turn on : 27.6999**

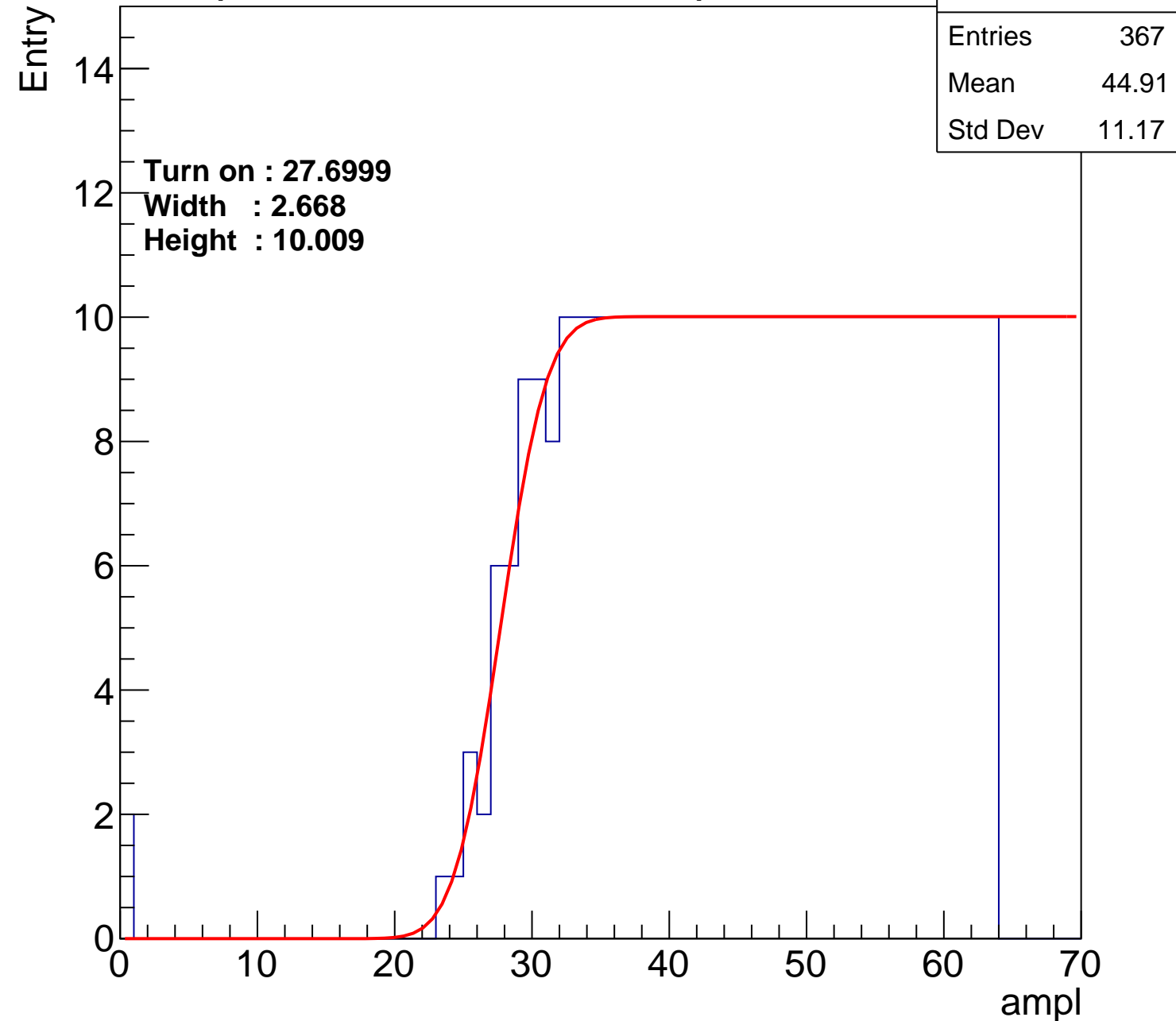
**Width : 2.668**

**Height : 10.009**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch43

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	388
Mean	43.84
Std Dev	11.84

Turn on : 25.6765

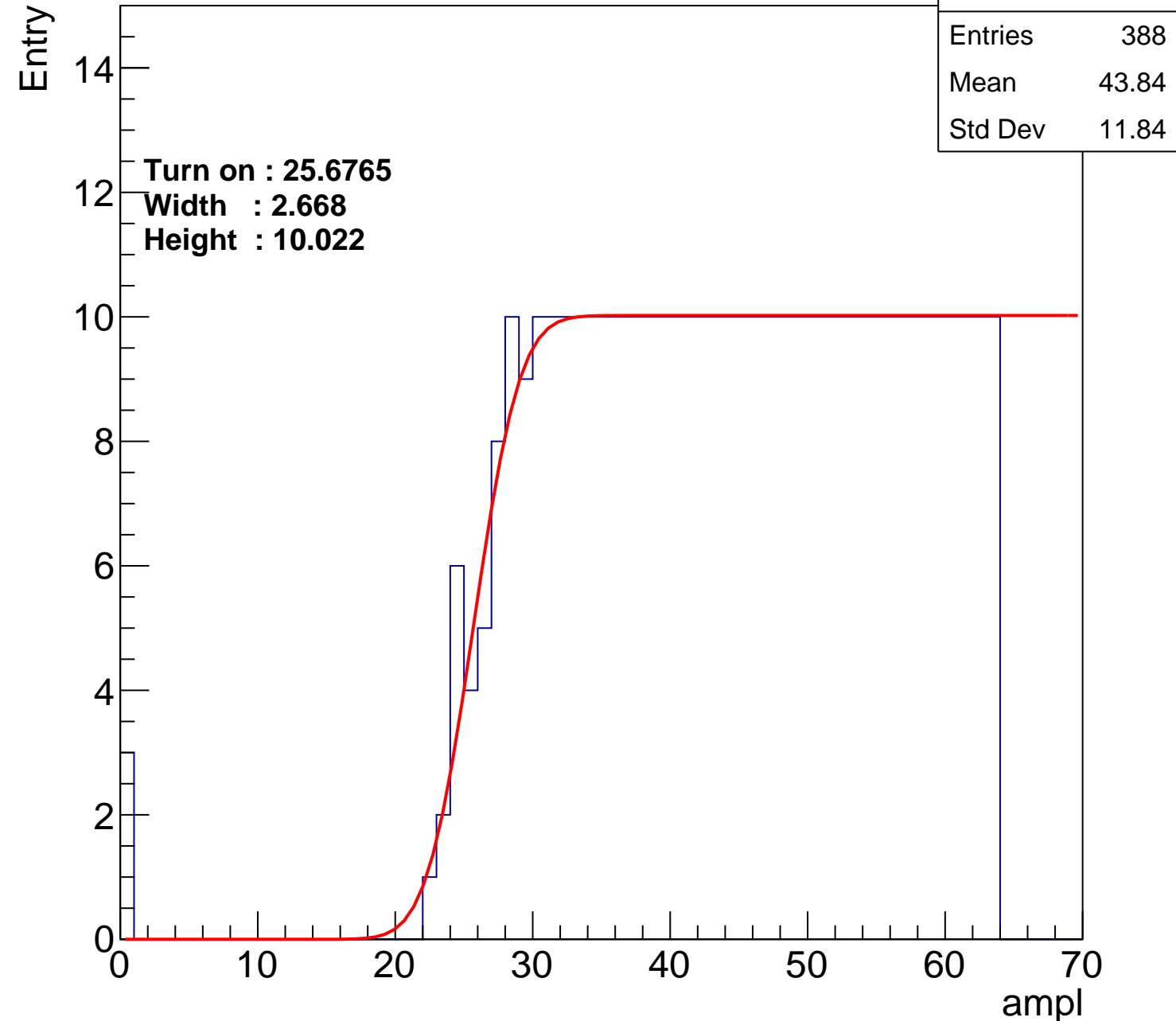
Width : 2.668

Height : 10.022

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch44

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	395
Mean	43.54
Std Dev	11.87

Turn on : 25.1005

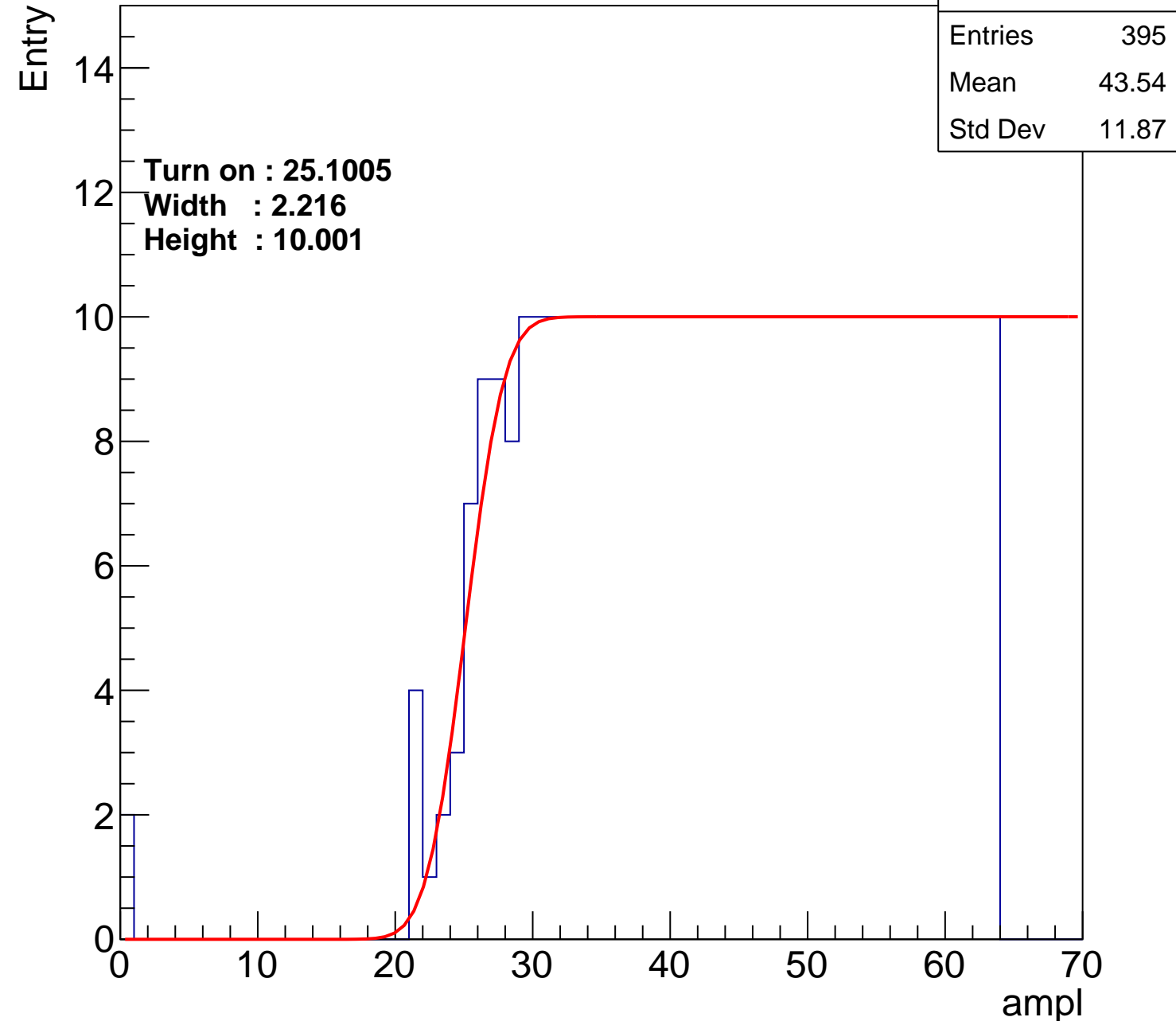
Width : 2.216

Height : 10.001

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch45

calib\_packv5\_042523\_0143.root, FC#0, port D2

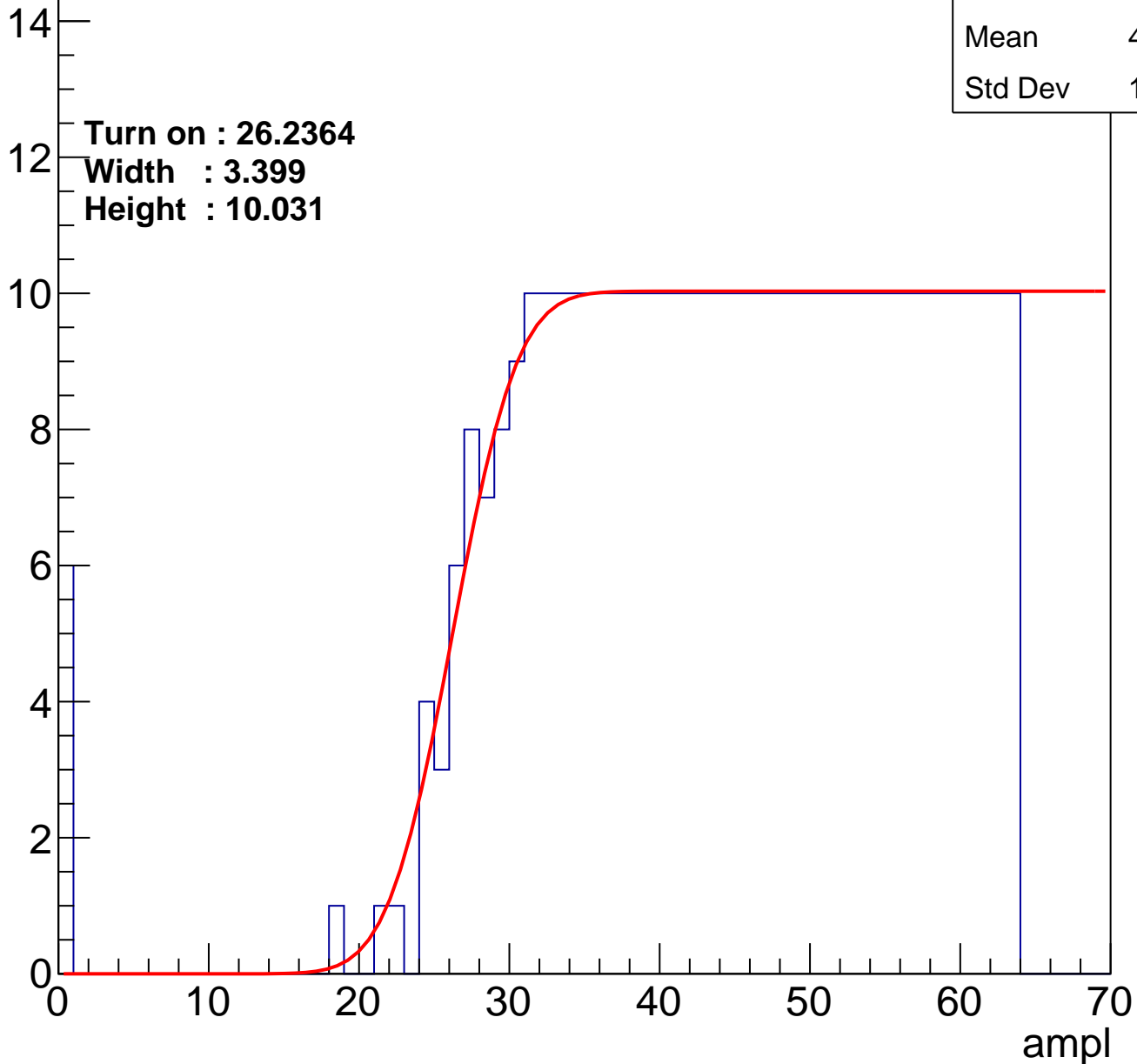
Entries	384
Mean	43.78
Std Dev	12.34

Turn on : 26.2364

Width : 3.399

Height : 10.031

Entry



# B1L101S, U9-ch46

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	377
Mean	44.19
Std Dev	12.02

Turn on : 26.7981

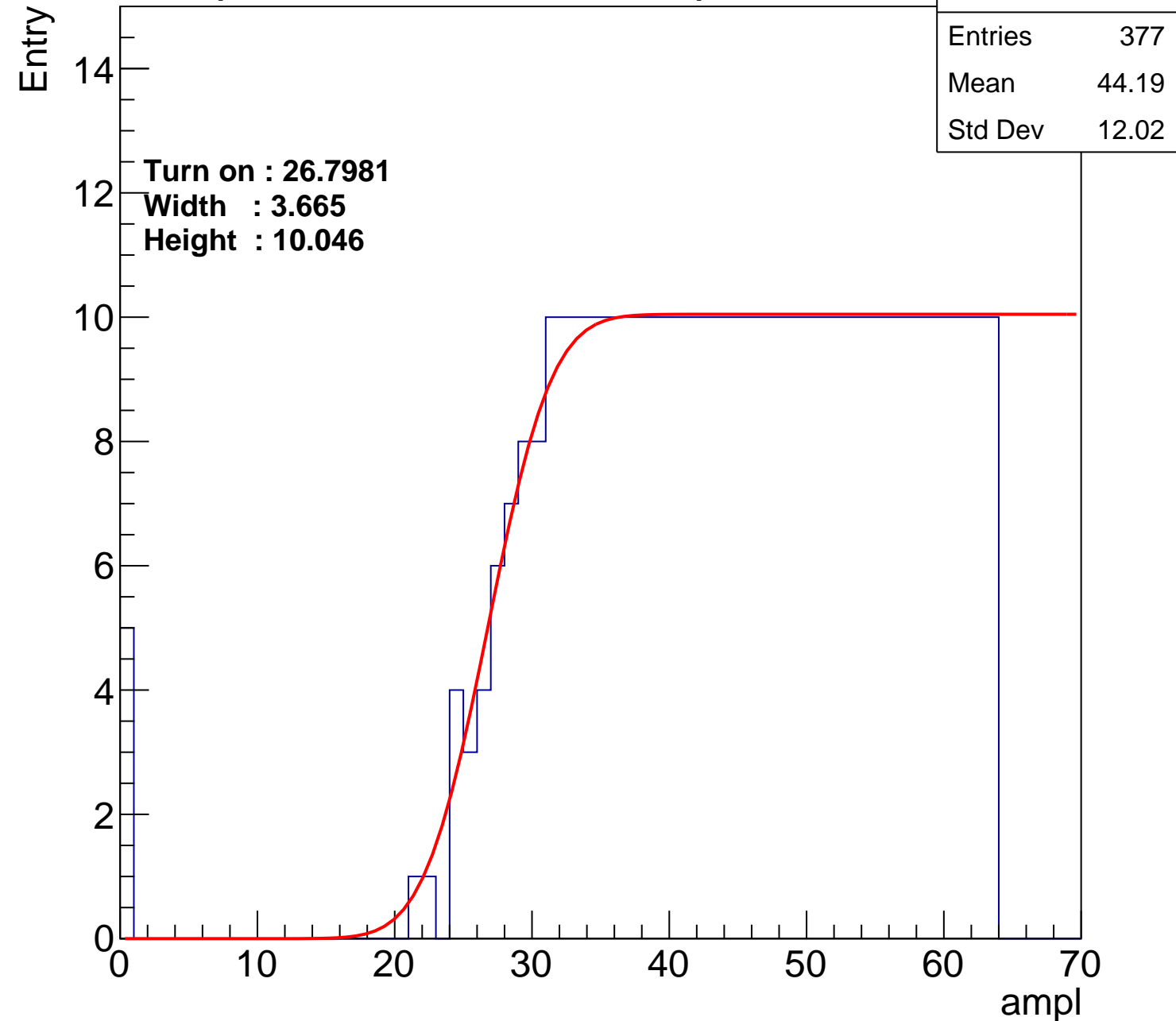
Width : 3.665

Height : 10.046

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L101S, U9-ch47

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	372
Mean	44.63
Std Dev	11.34

Turn on : 26.9020

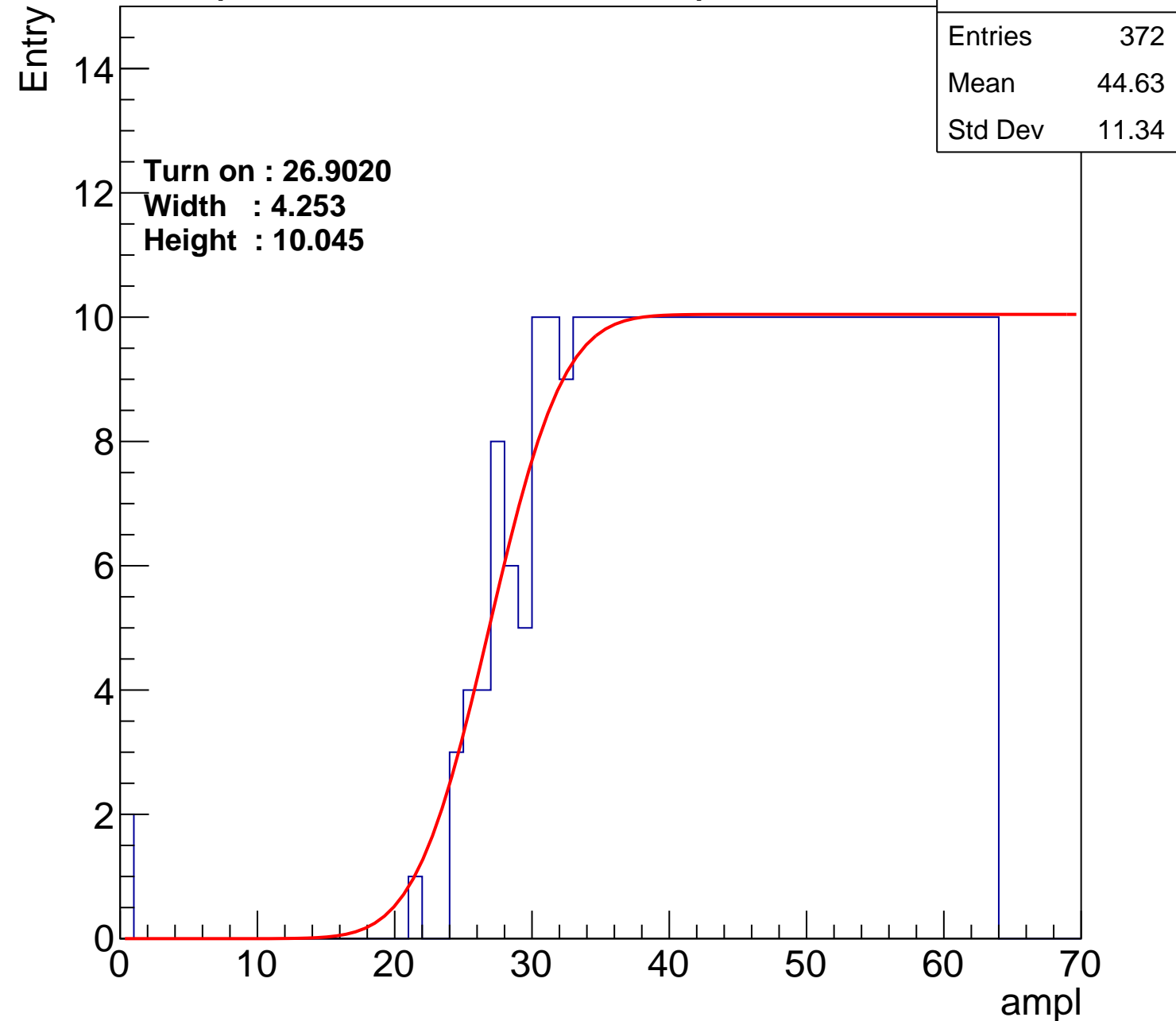
Width : 4.253

Height : 10.045

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch48

calib\_packv5\_042523\_0143.root, FC#0, port D2

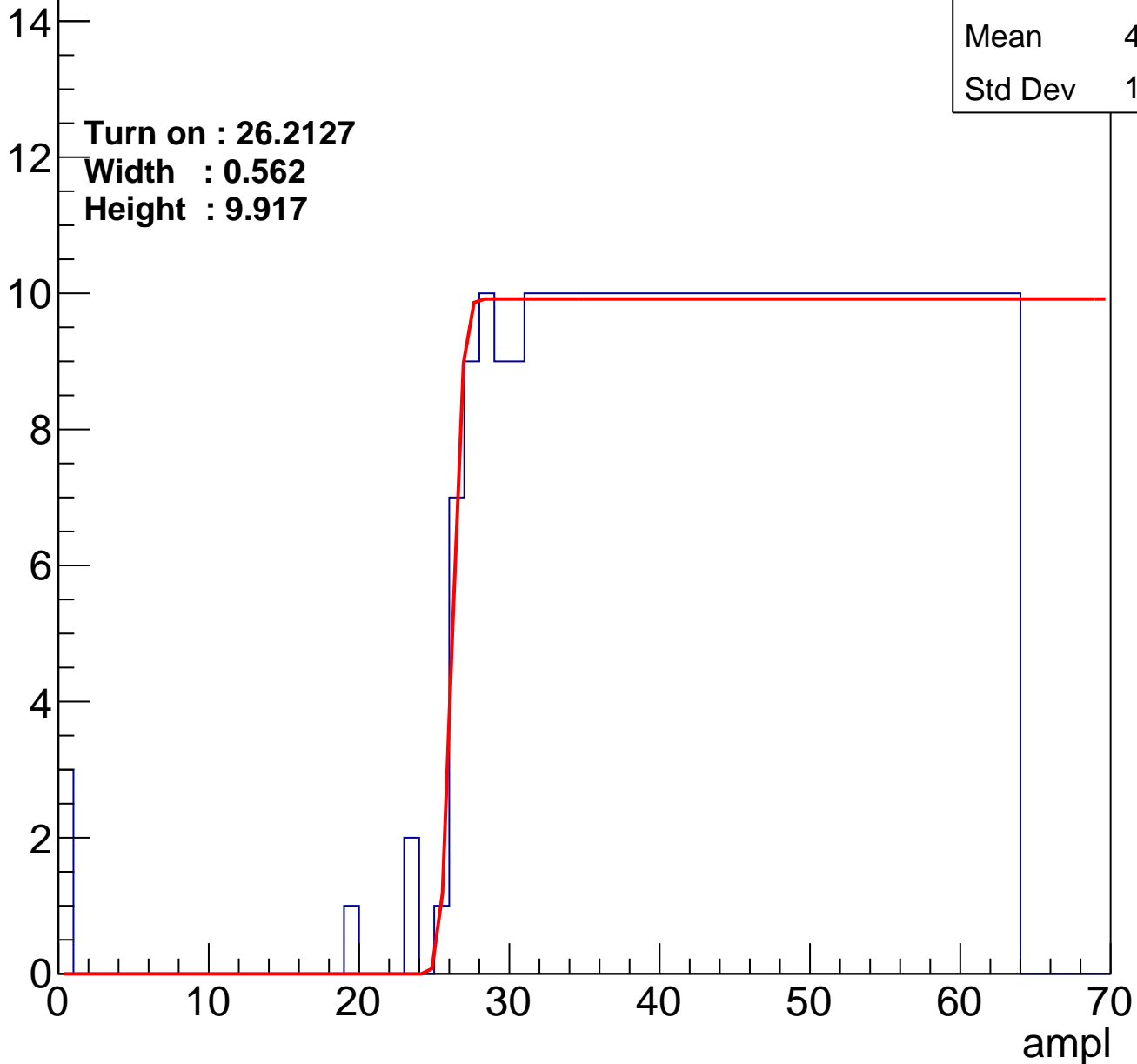
Entries	381
Mean	44.19
Std Dev	11.66

Turn on : 26.2127

Width : 0.562

Height : 9.917

Entry



# B1L101S, U9-ch49

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	366
Mean	44.83
Std Dev	11.53

Turn on : 28.1000

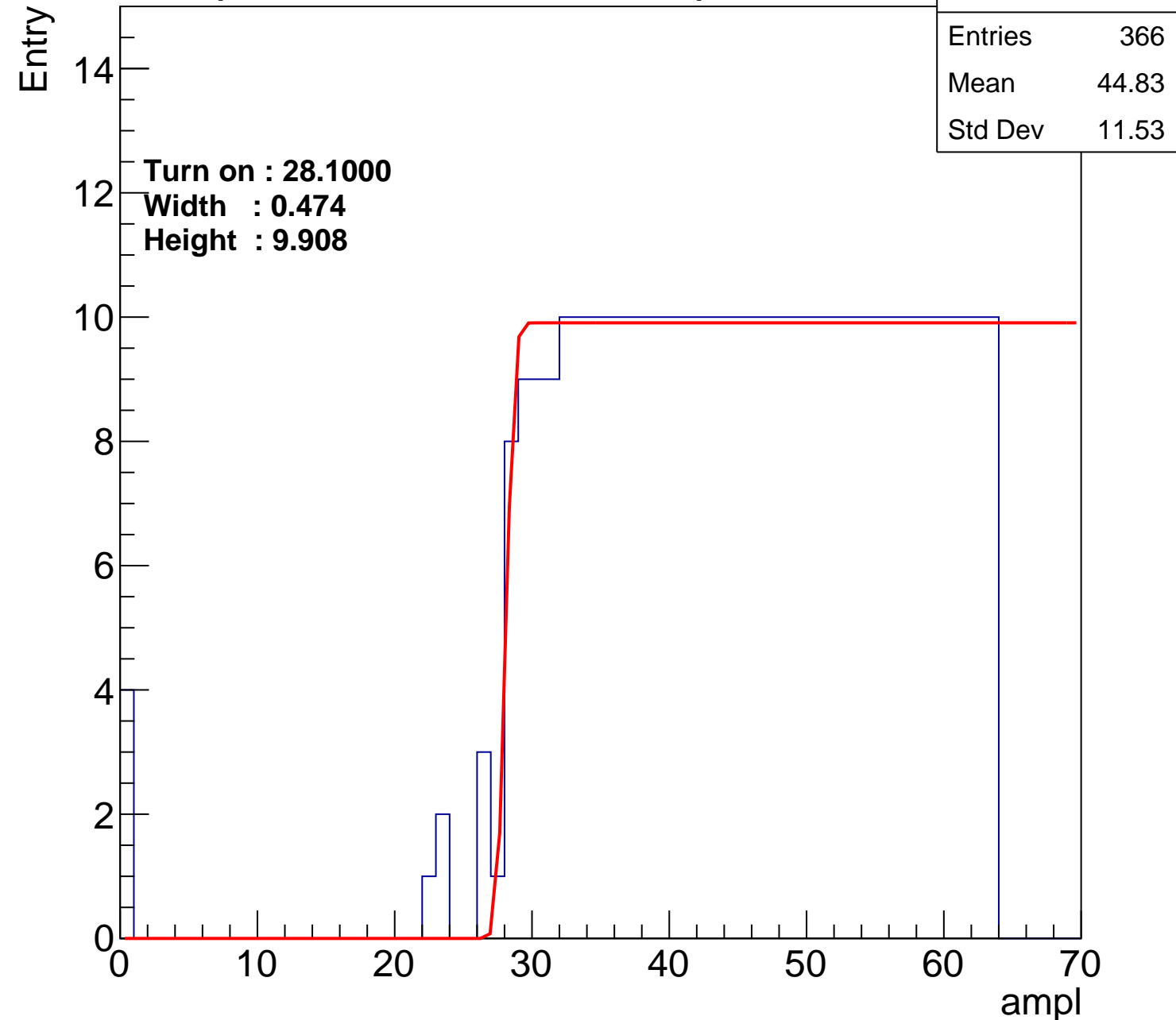
Width : 0.474

Height : 9.908

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch50

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	372
Mean	44.67
Std Dev	11.29

Turn on : 27.0072

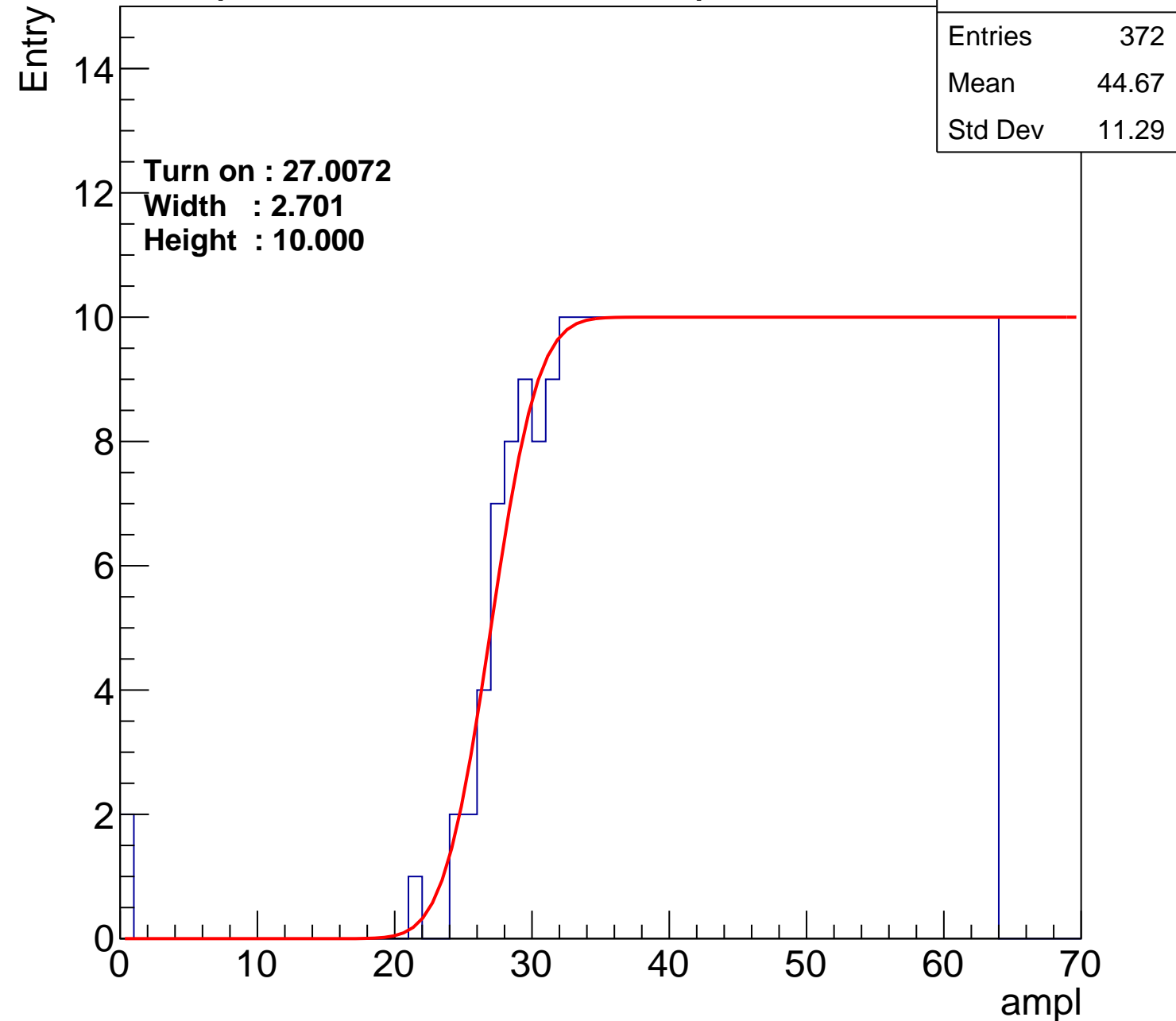
Width : 2.701

Height : 10.000

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch51

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	379
Mean	44.19
Std Dev	11.83

Turn on : 26.4732

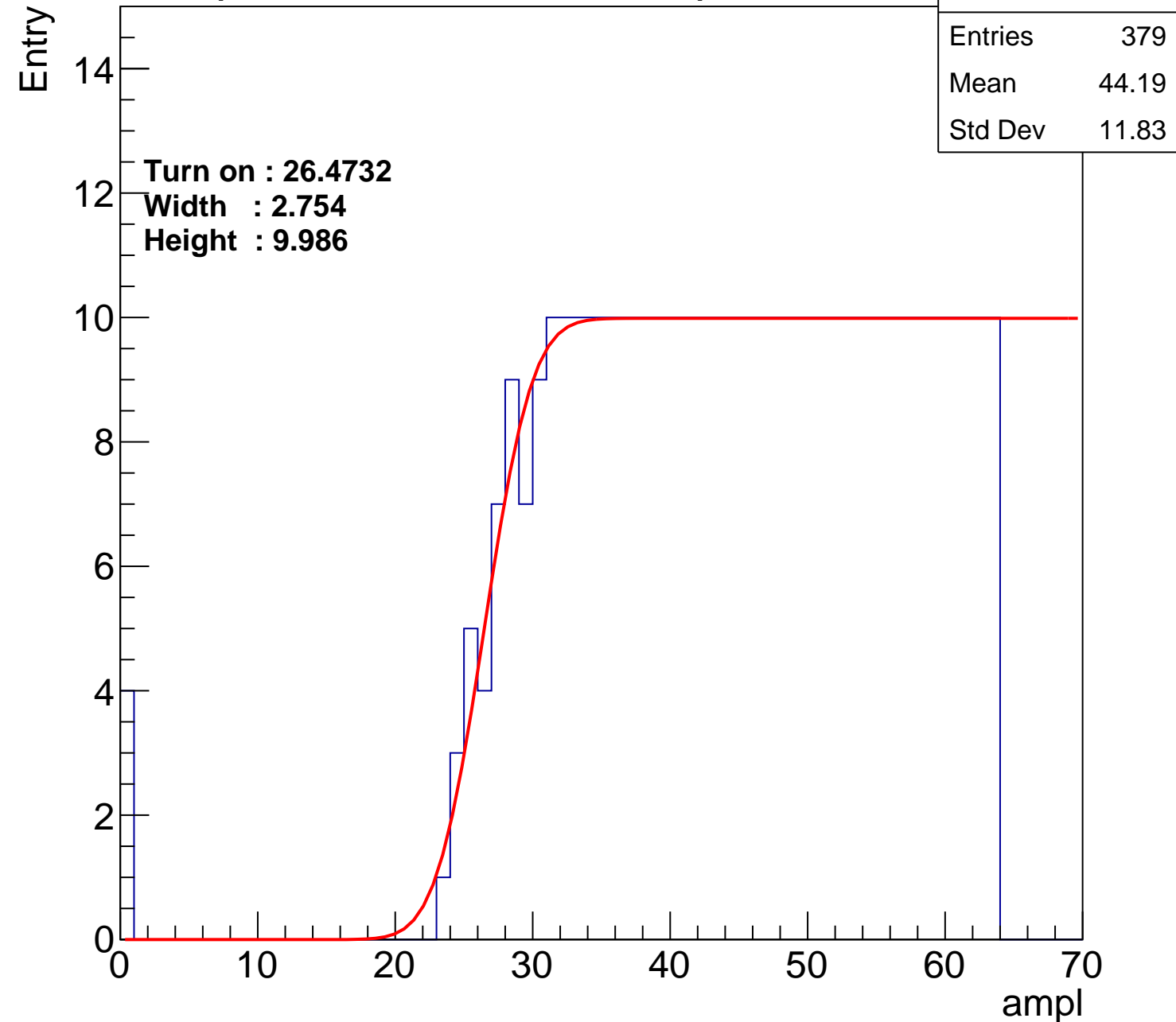
Width : 2.754

Height : 9.986

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch52

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	367
Mean	44.84
Std Dev	11.28

Turn on : 27.5276

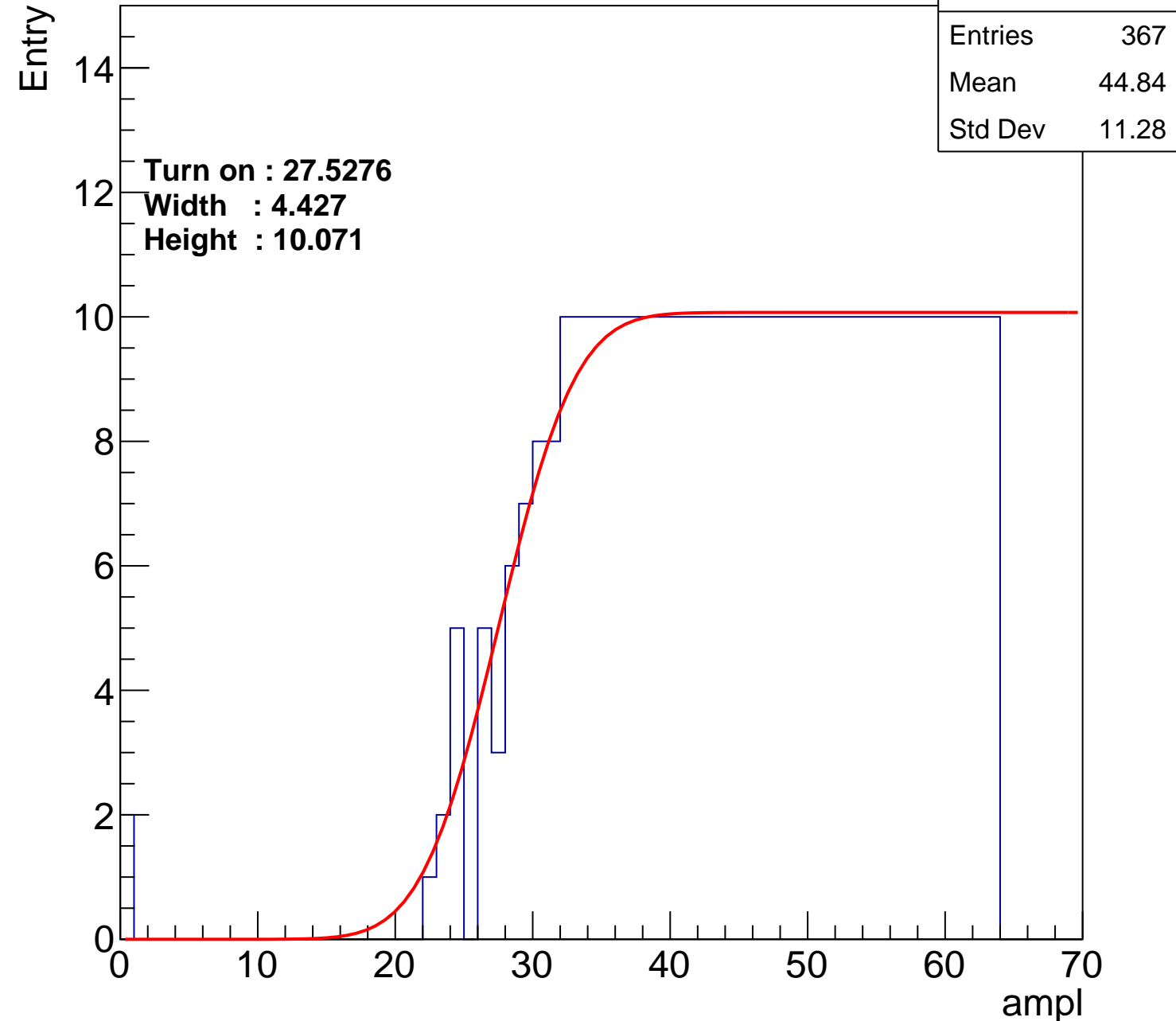
Width : 4.427

Height : 10.071

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch53

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	378
Mean	44.33
Std Dev	11.51

Turn on : 26.4185

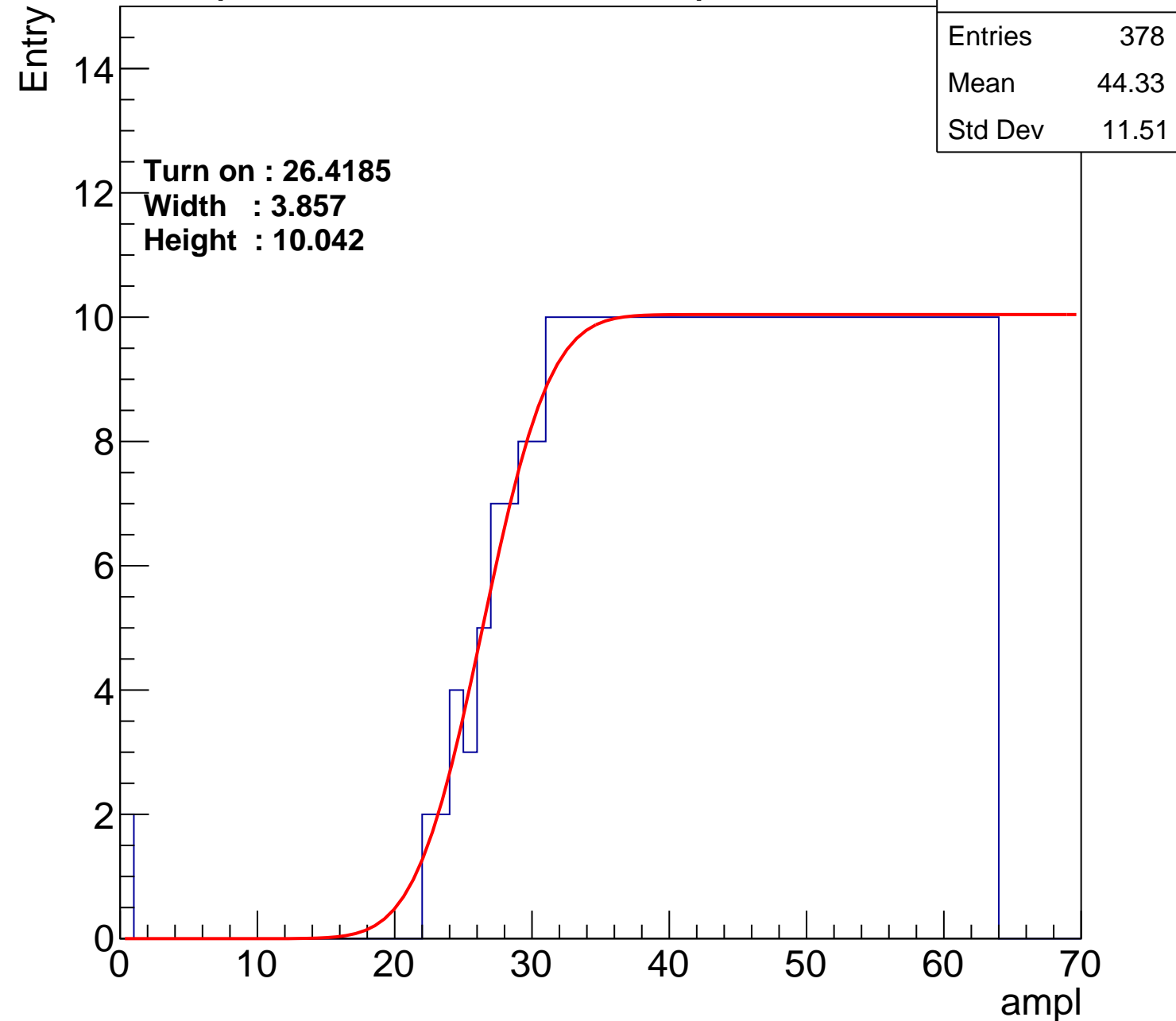
Width : 3.857

Height : 10.042

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch54

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	376
Mean	44.53
Std Dev	11.23

**Turn on : 26.6653**

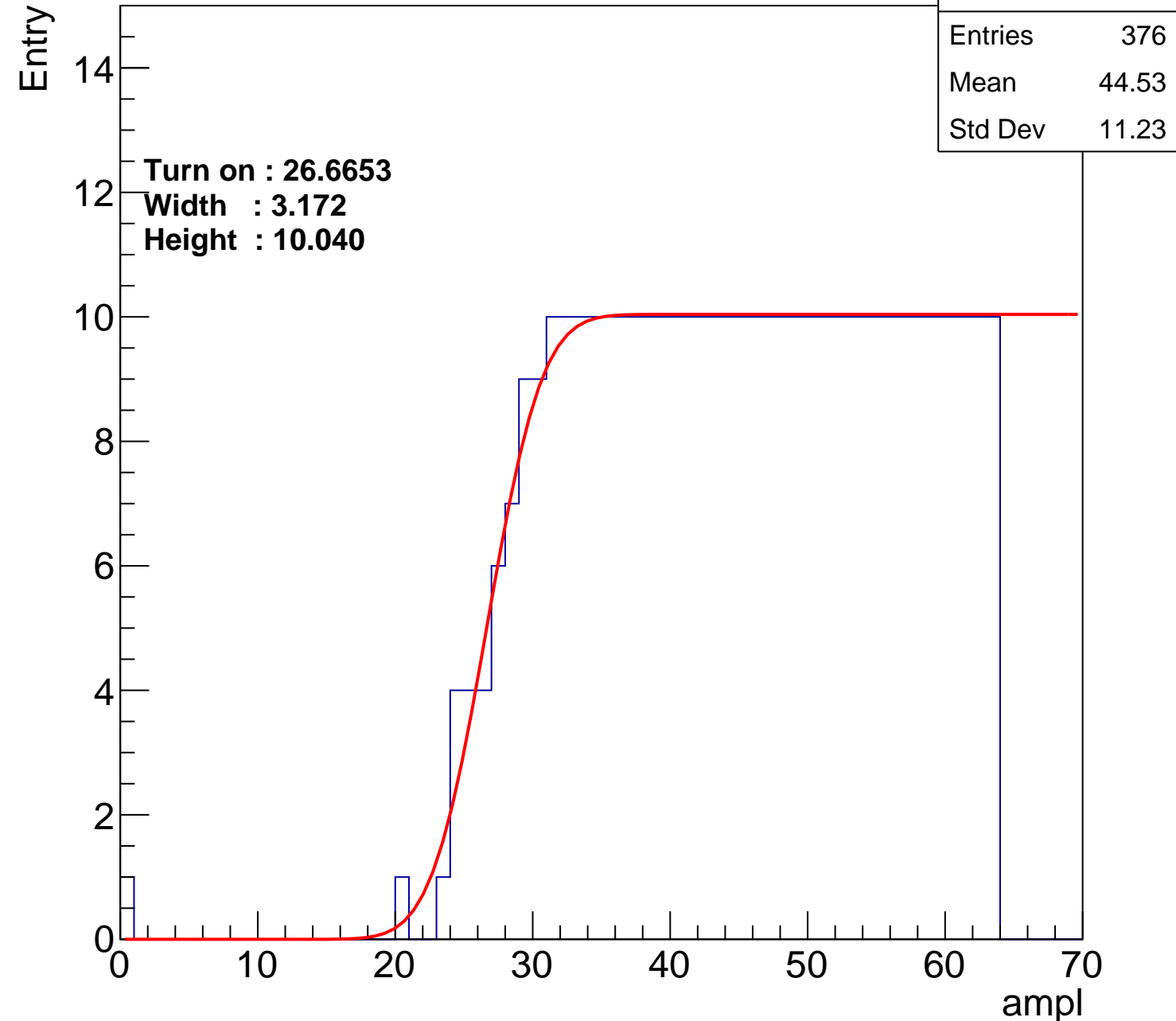
**Width : 3.172**

**Height : 10.040**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L101S, U9-ch55

calib\_packv5\_042523\_0143.root, FC#0, port D2

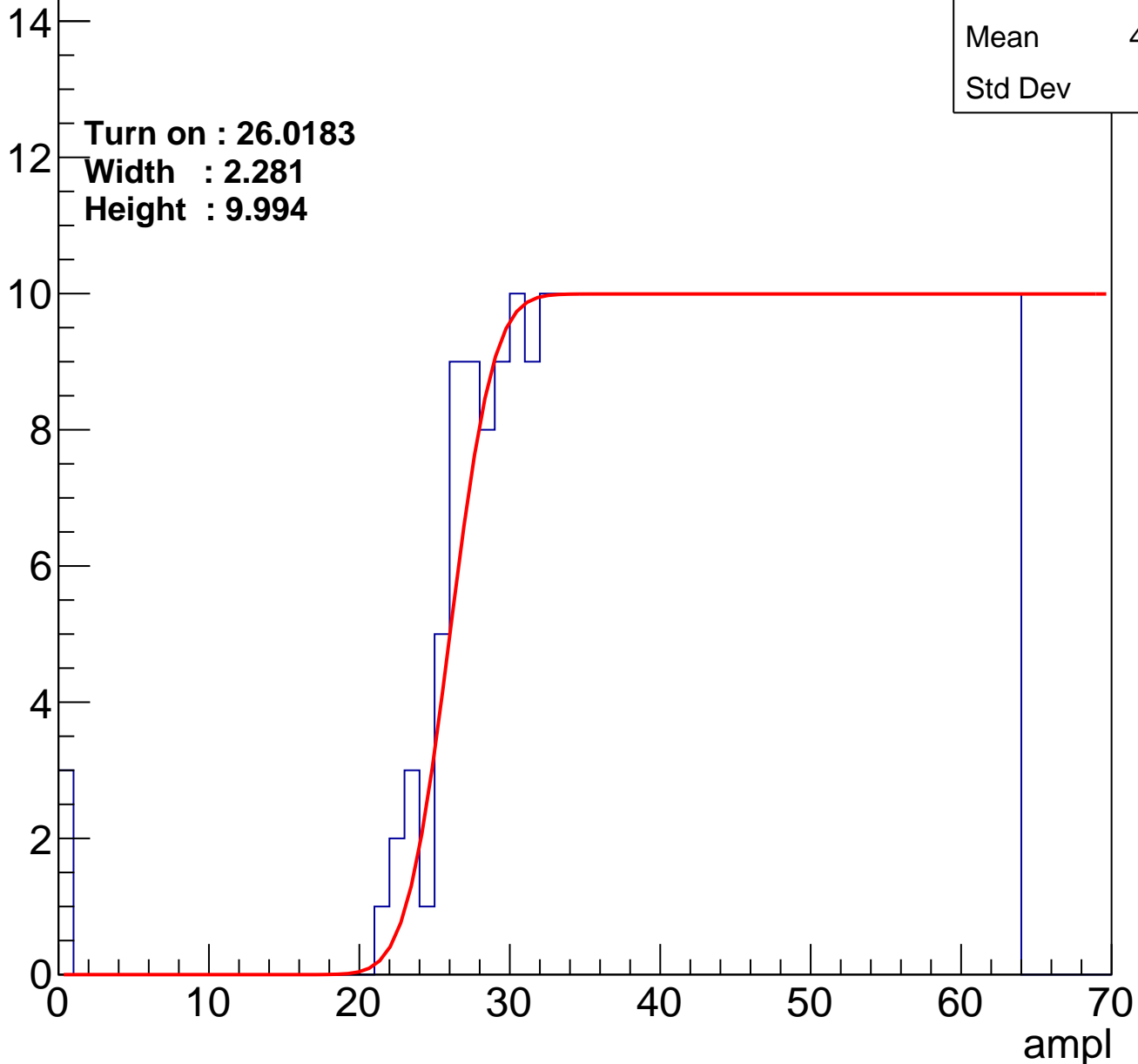
Entries	389
Mean	43.76
Std Dev	11.9

Turn on : 26.0183

Width : 2.281

Height : 9.994

Entry



# B1L101S, U9-ch56

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	377
Mean	44.43
Std Dev	11.35

**Turn on : 26.2467**

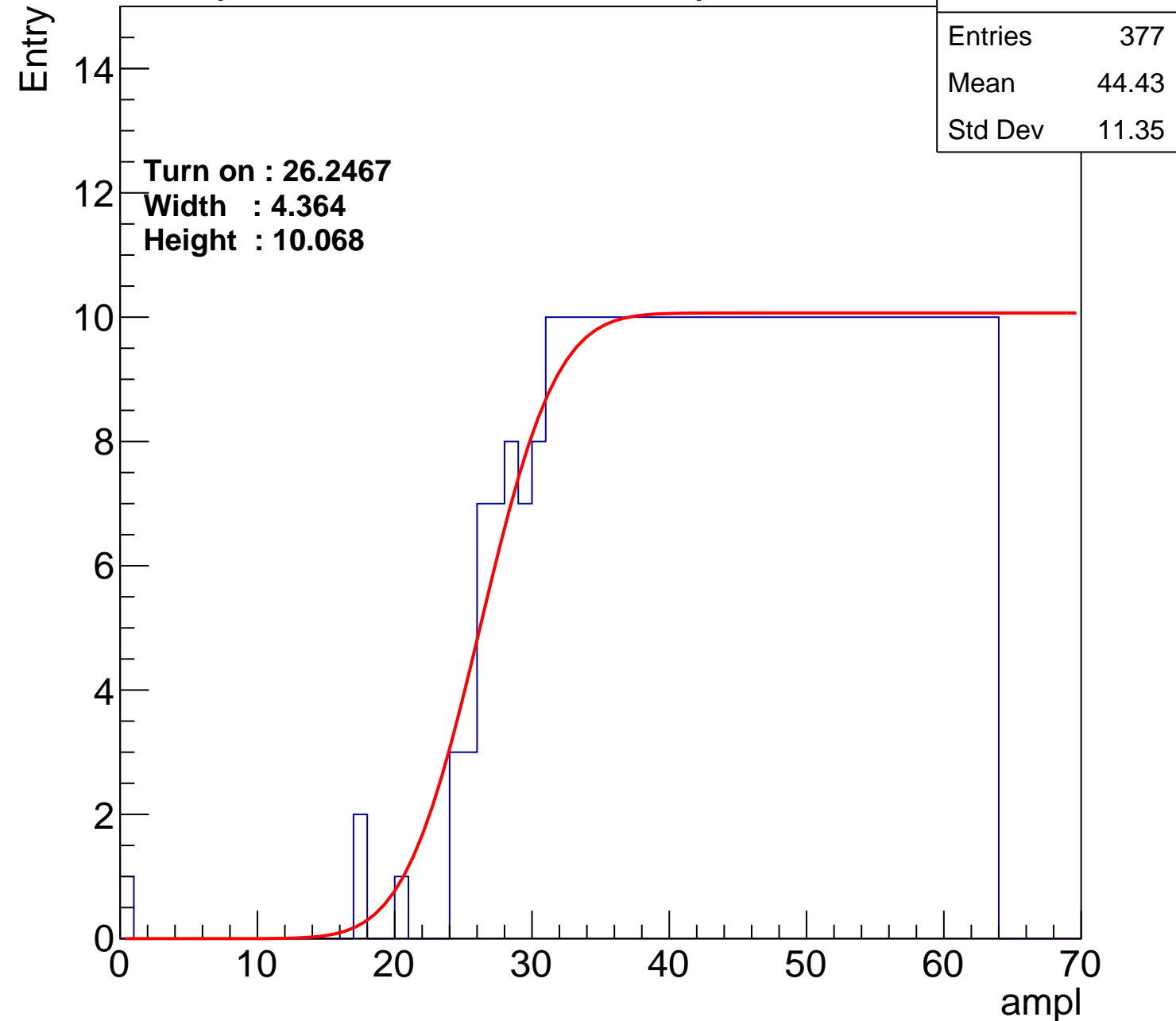
**Width : 4.364**

**Height : 10.068**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch57

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	366
Mean	45.01
Std Dev	10.97

Turn on : 27.7360

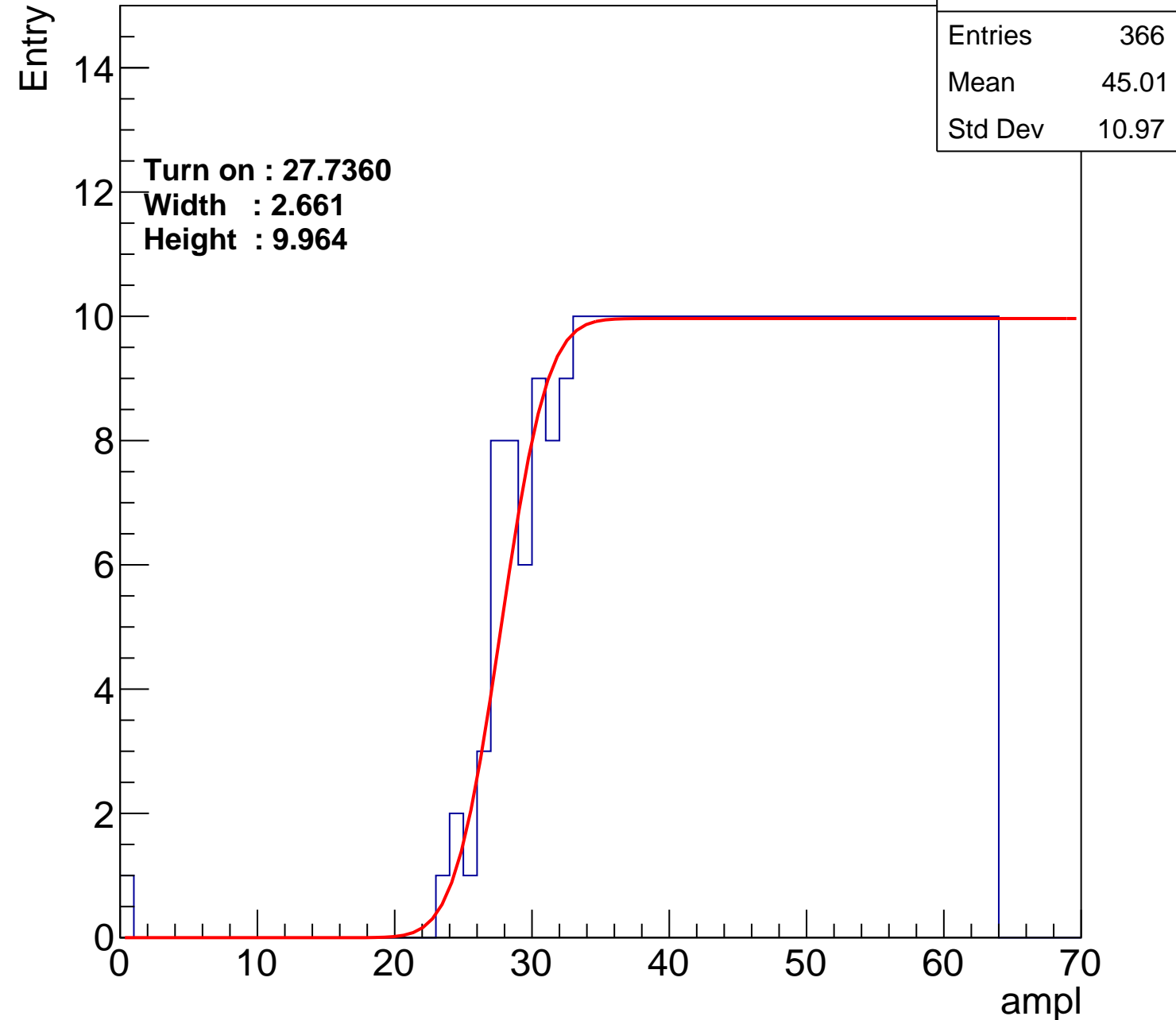
Width : 2.661

Height : 9.964

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch58

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	385
Mean	43.91
Std Dev	11.94

Turn on : 25.8848

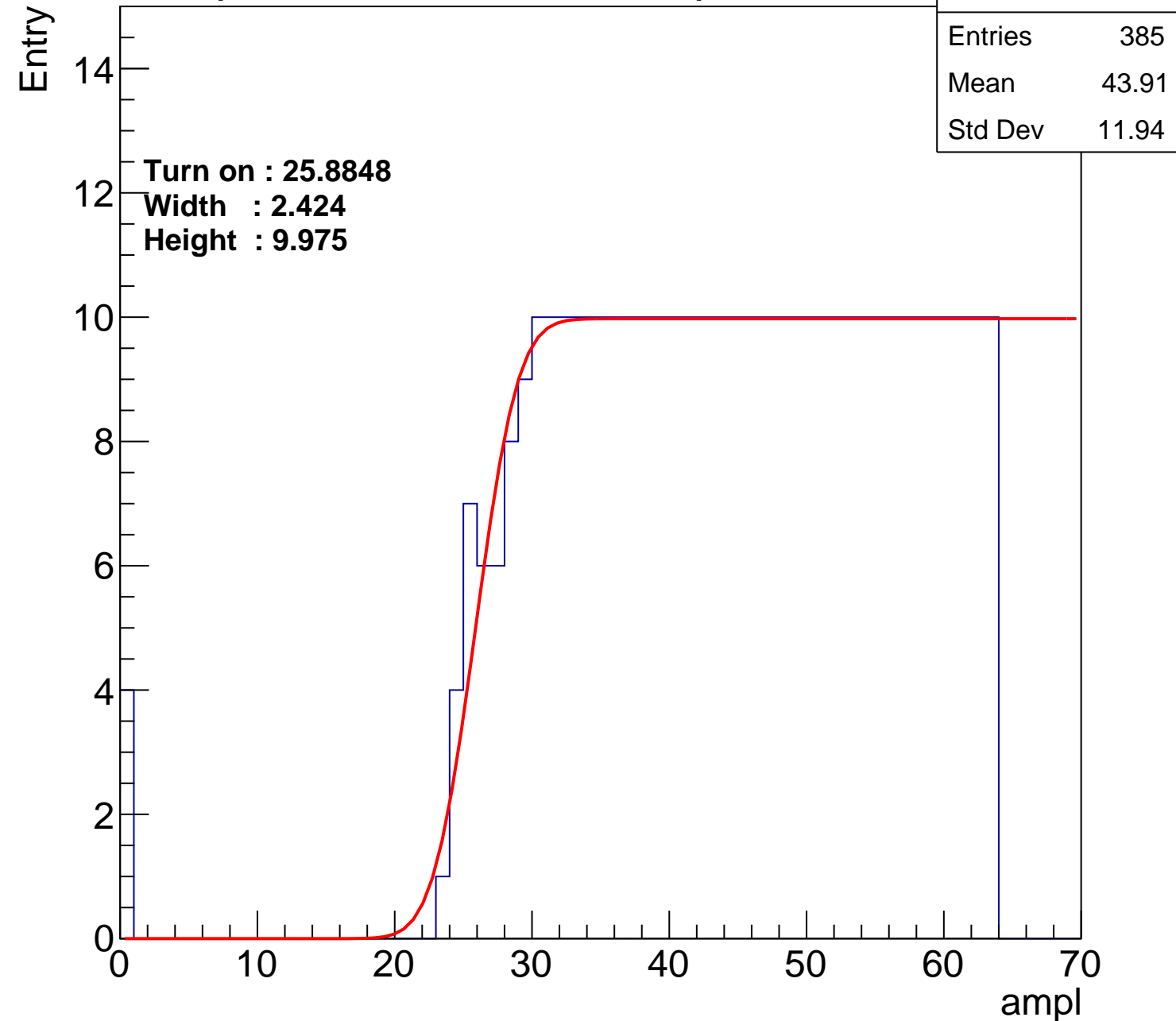
Width : 2.424

Height : 9.975

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch59

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	373
Mean	44.52
Std Dev	11.56

Turn on : 27.3230

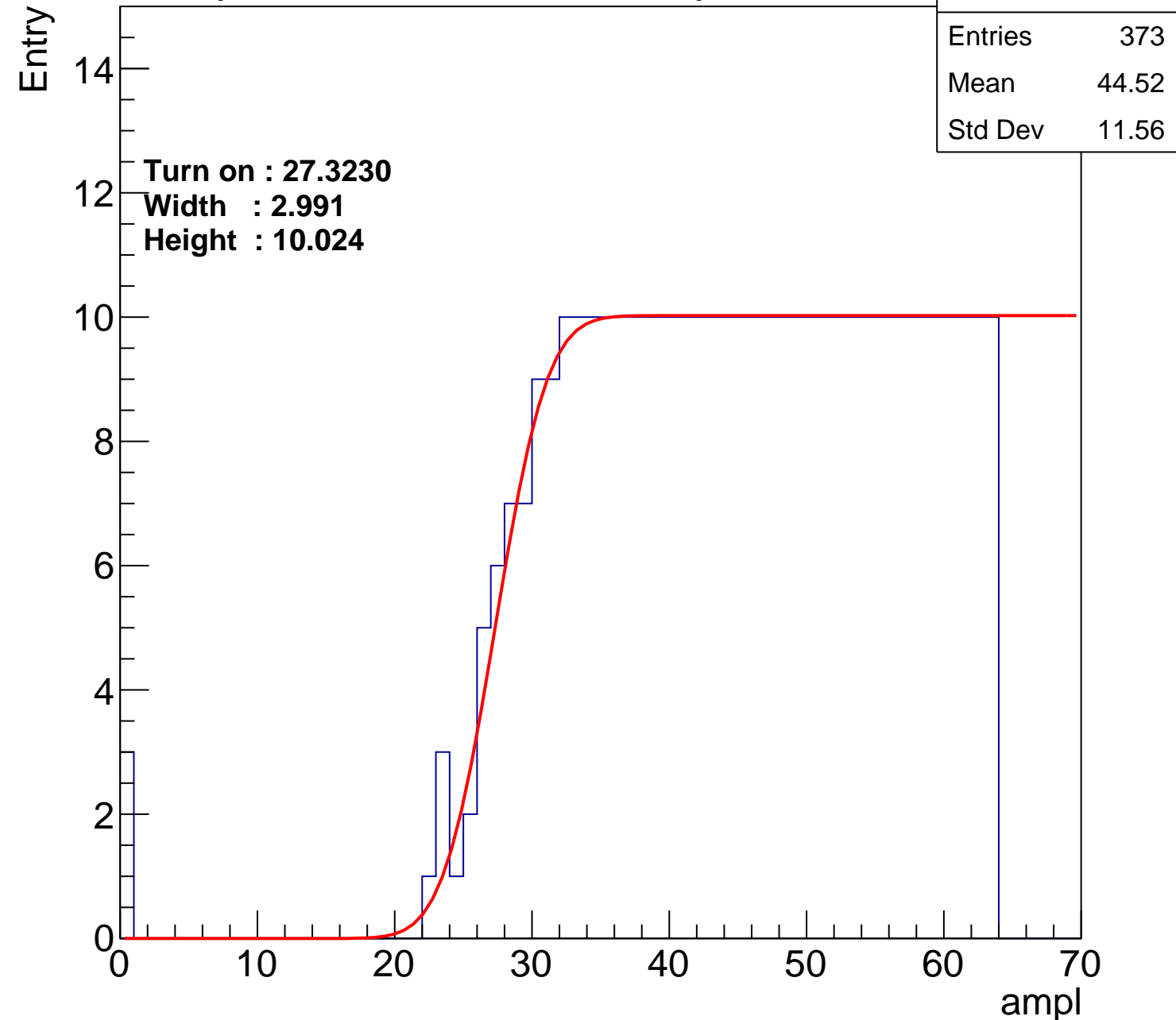
Width : 2.991

Height : 10.024

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch60

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	363
Mean	45.13
Std Dev	11.02

Turn on : 27.6995

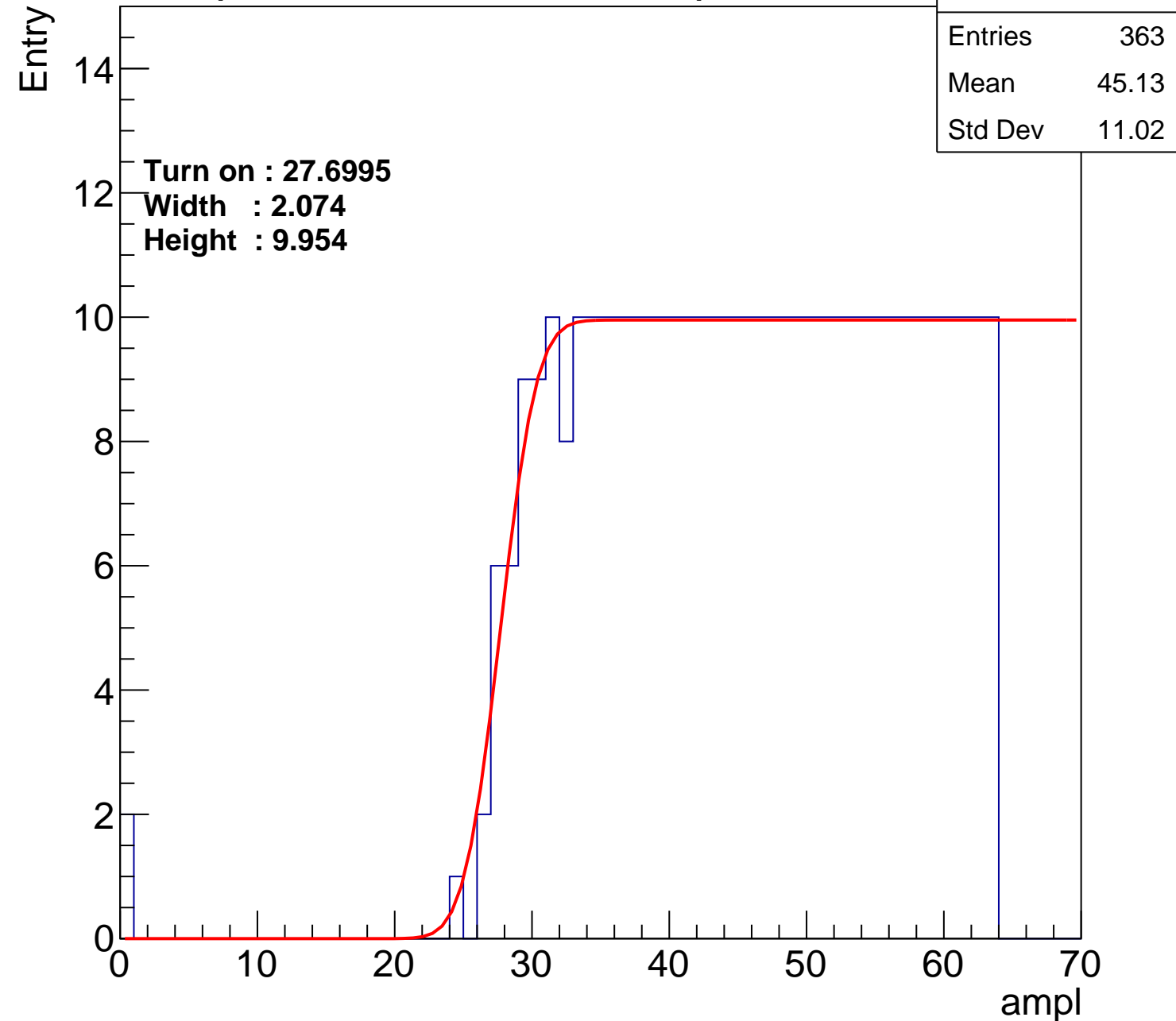
Width : 2.074

Height : 9.954

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch61

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	366
Mean	44.9
Std Dev	11.33

Turn on : 27.7065

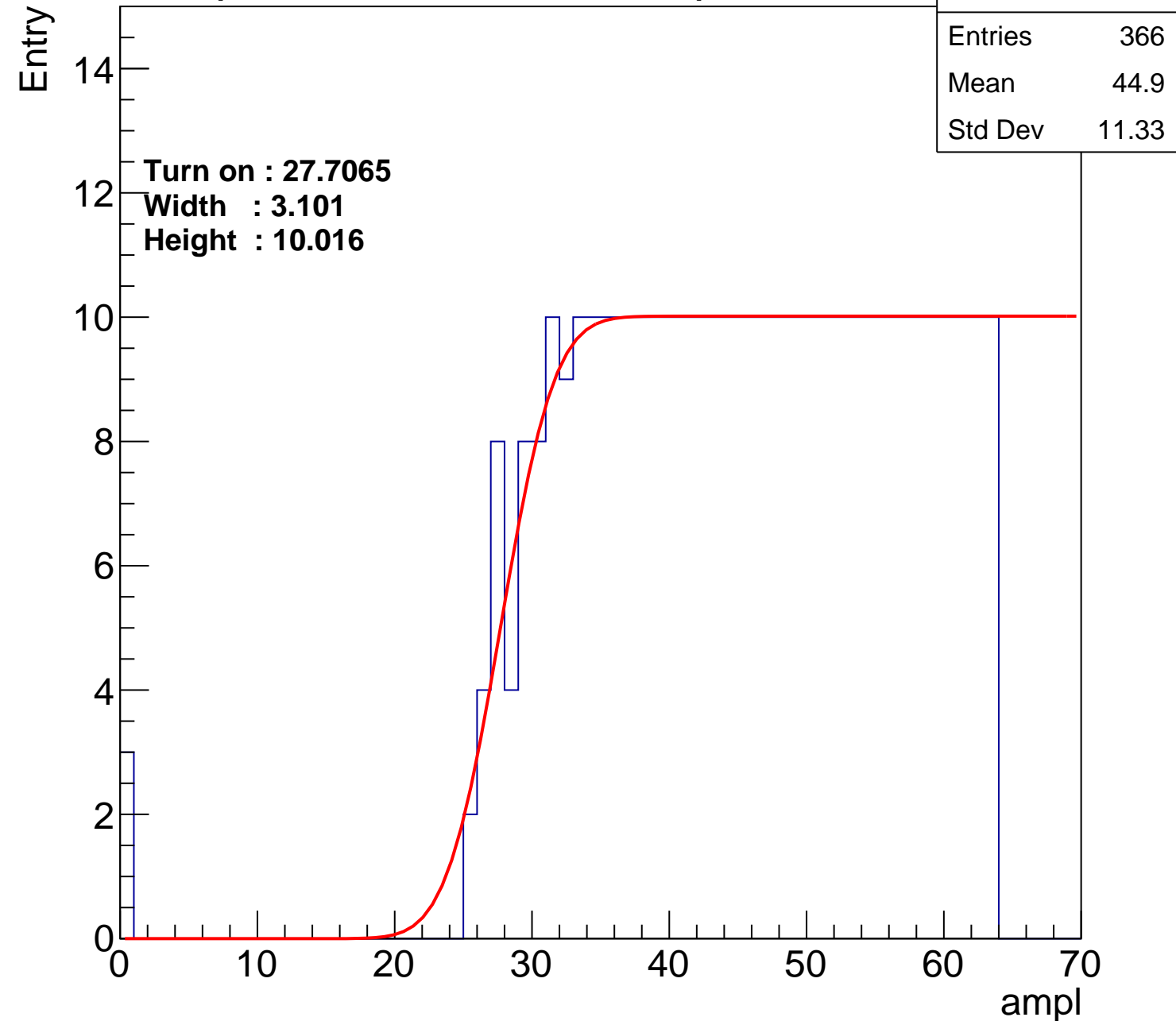
Width : 3.101

Height : 10.016

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch62

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	403
Mean	43.11
Std Dev	12.21

Turn on : 24.2101

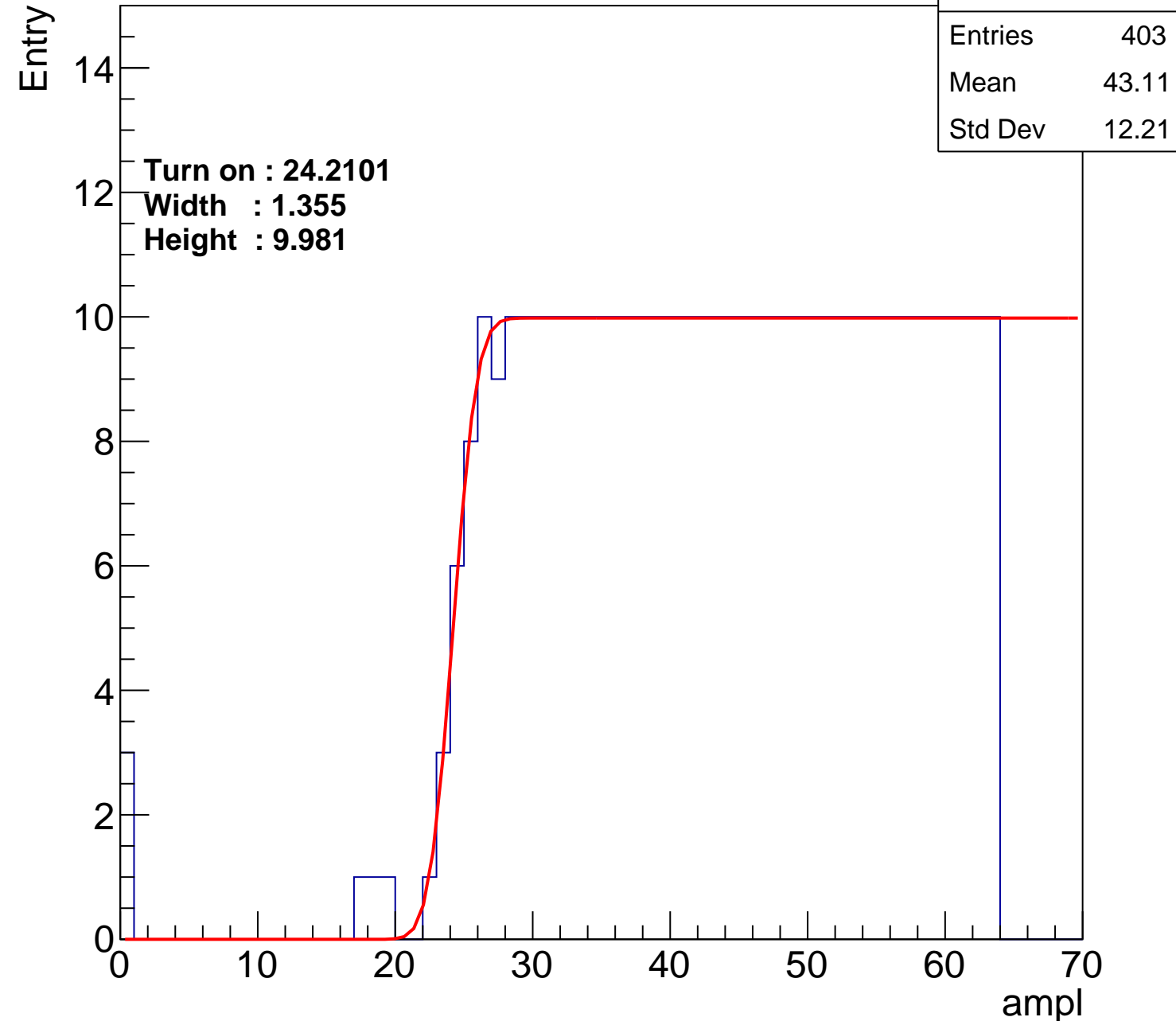
Width : 1.355

Height : 9.981

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L101S, U9-ch63

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	384
Mean	44.15
Std Dev	11.4

Turn on : 25.4219

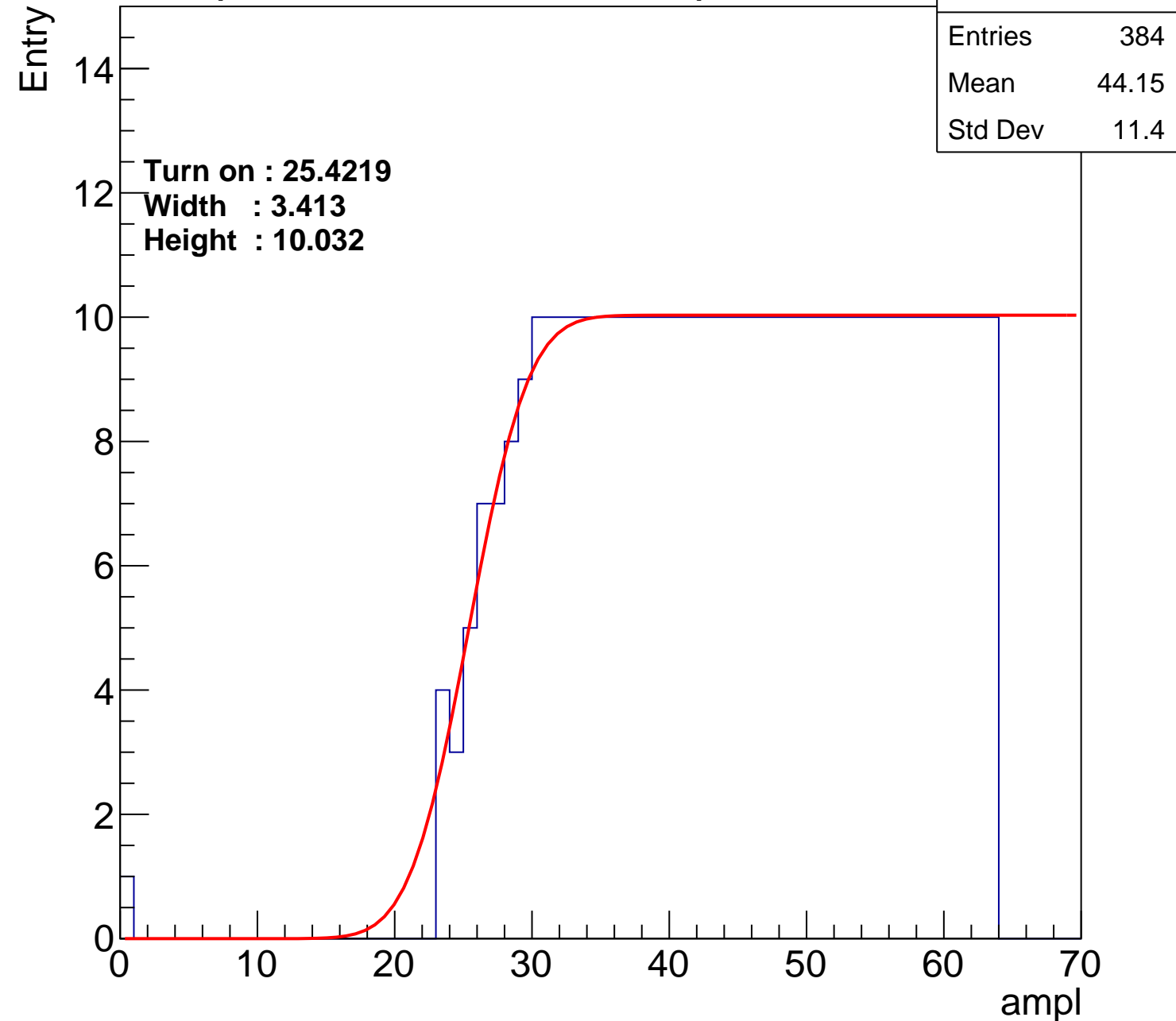
Width : 3.413

Height : 10.032

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch64

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	384
Mean	44.09
Std Dev	11.57

**Turn on : 25.3255**

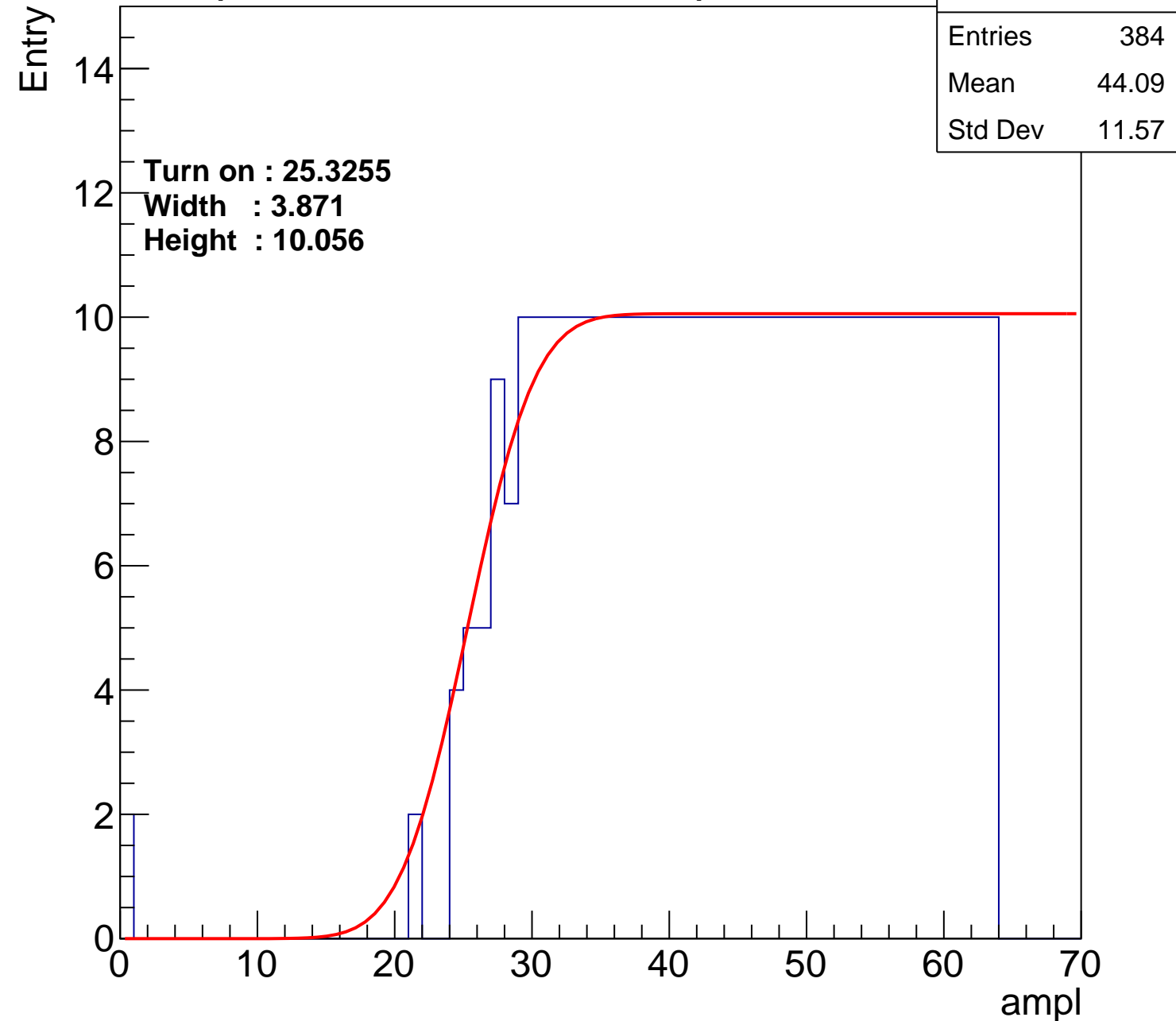
**Width : 3.871**

**Height : 10.056**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch65

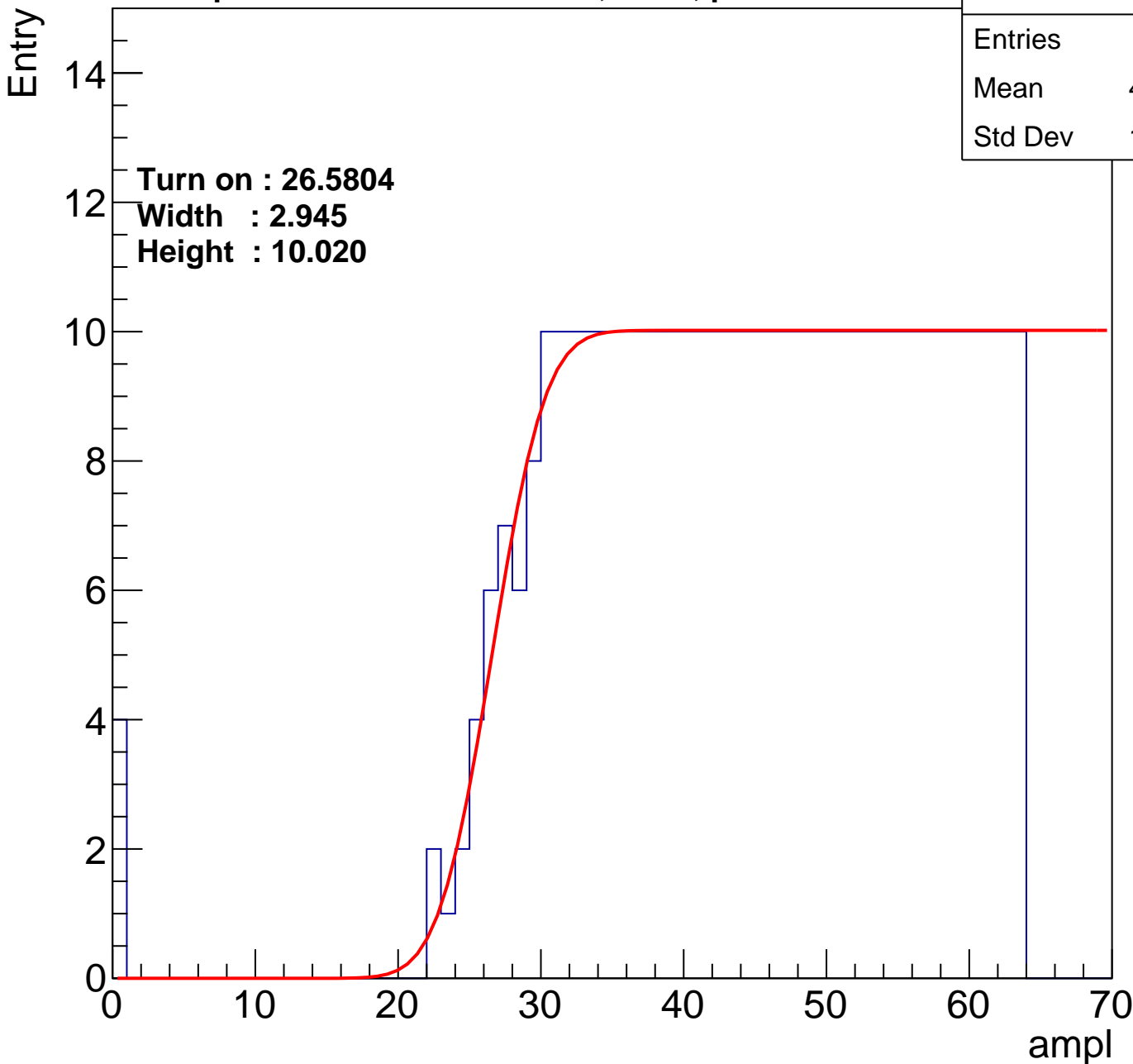
**calib\_packv5\_042523\_0143.root, FC#0, port D2**

Entries	380
Mean	44.13
Std Dev	11.87

**Turn on : 26.5804**

**Width : 2.945**

**Height : 10.020**



# B1L101S, U9-ch66

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	377
Mean	44.34
Std Dev	11.63

**Turn on : 26.5842**

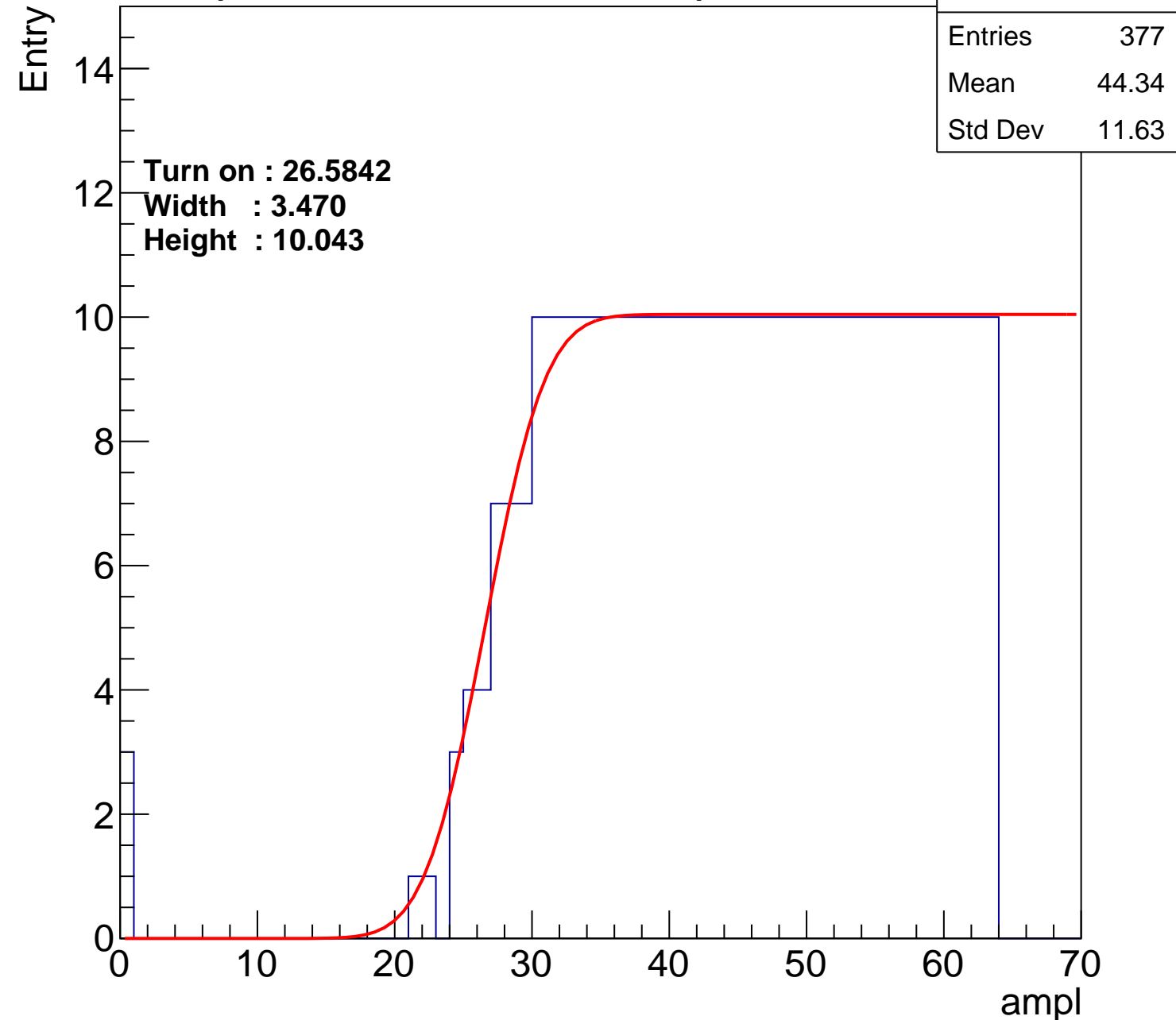
**Width : 3.470**

**Height : 10.043**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch67

calib\_packv5\_042523\_0143.root, FC#0, port D2

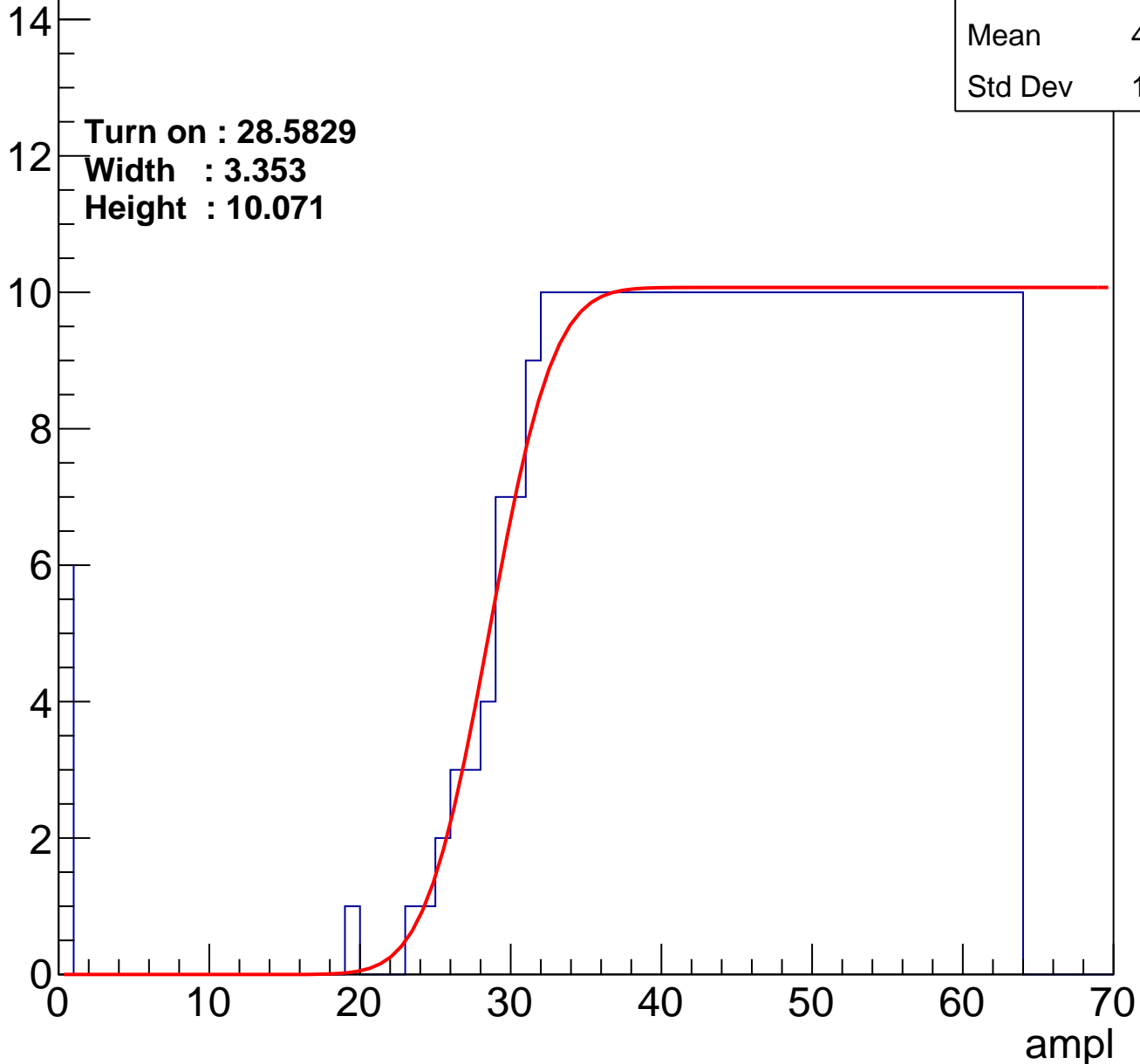
Entries	364
Mean	44.72
Std Dev	11.97

Turn on : 28.5829

Width : 3.353

Height : 10.071

Entry



# B1L101S, U9-ch68

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	379
Mean	44.18
Std Dev	11.85

Turn on : 27.0176

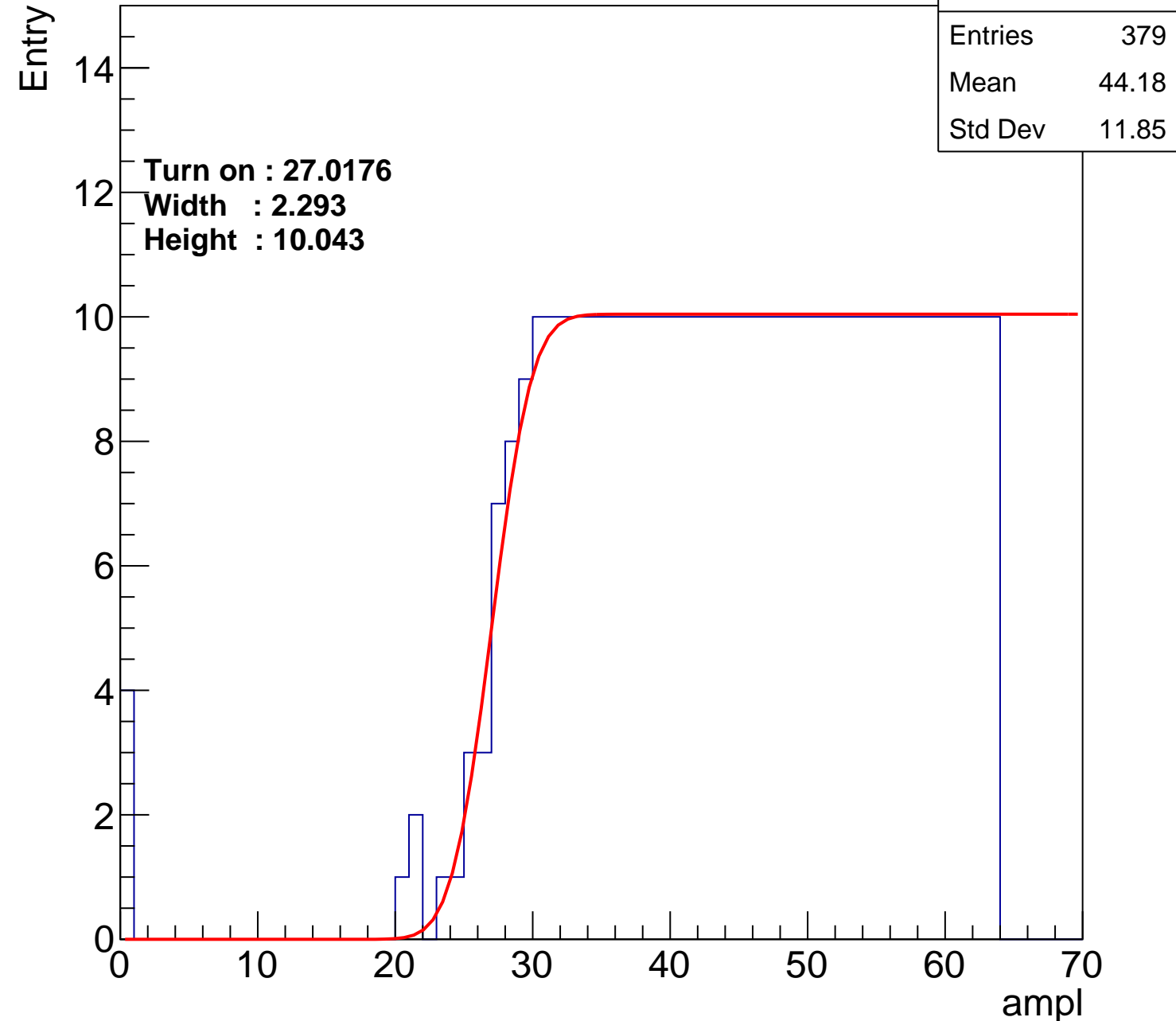
Width : 2.293

Height : 10.043

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch69

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	367
Mean	44.85
Std Dev	11.35

**Turn on : 27.7880**

**Width : 2.691**

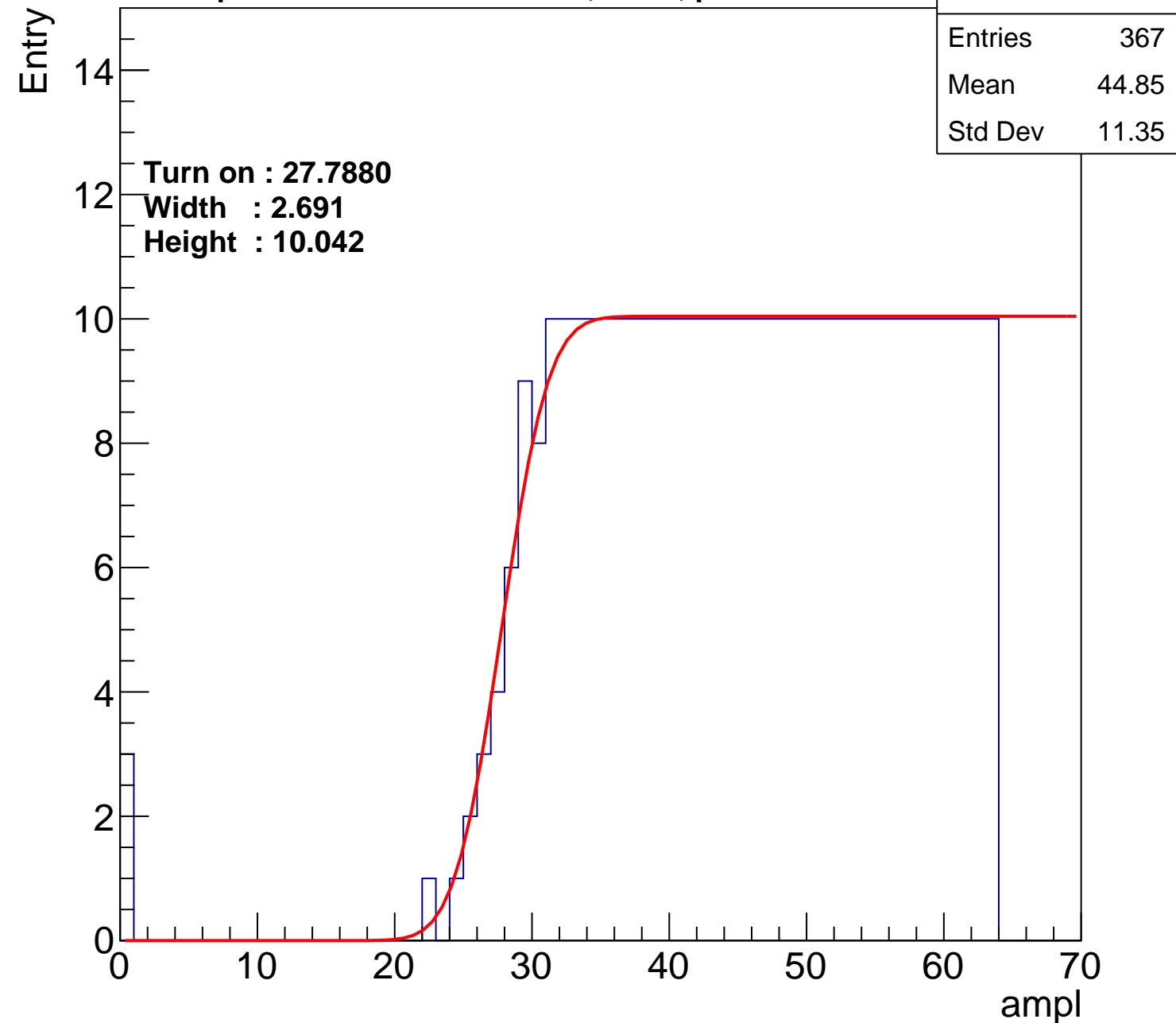
**Height : 10.042**

Entry

14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L101S, U9-ch70

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	379
Mean	44.09
Std Dev	12.06

Turn on : 26.9036

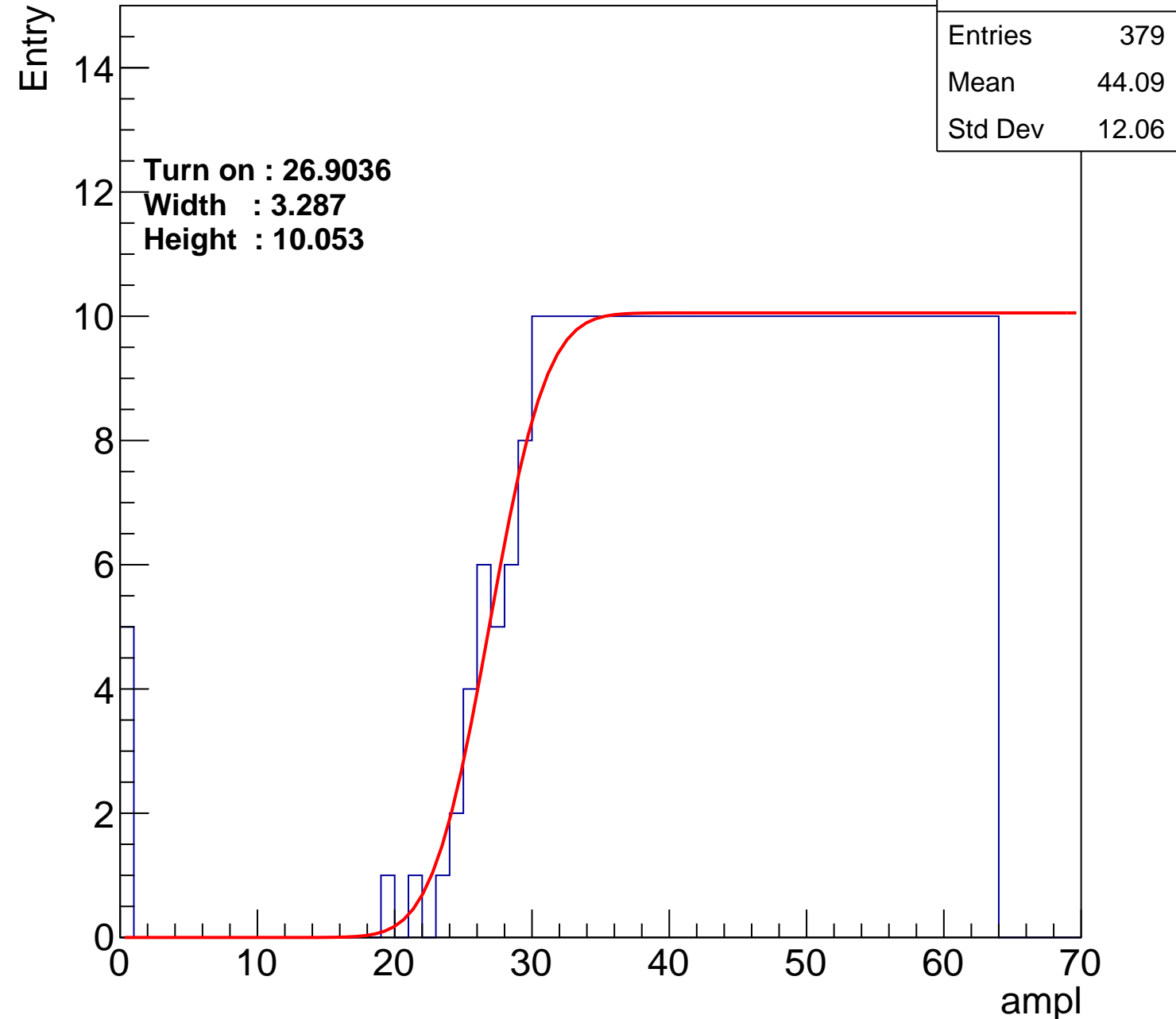
Width : 3.287

Height : 10.053

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L101S, U9-ch71

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	371
Mean	44.72
Std Dev	11.27

**Turn on : 27.6630**

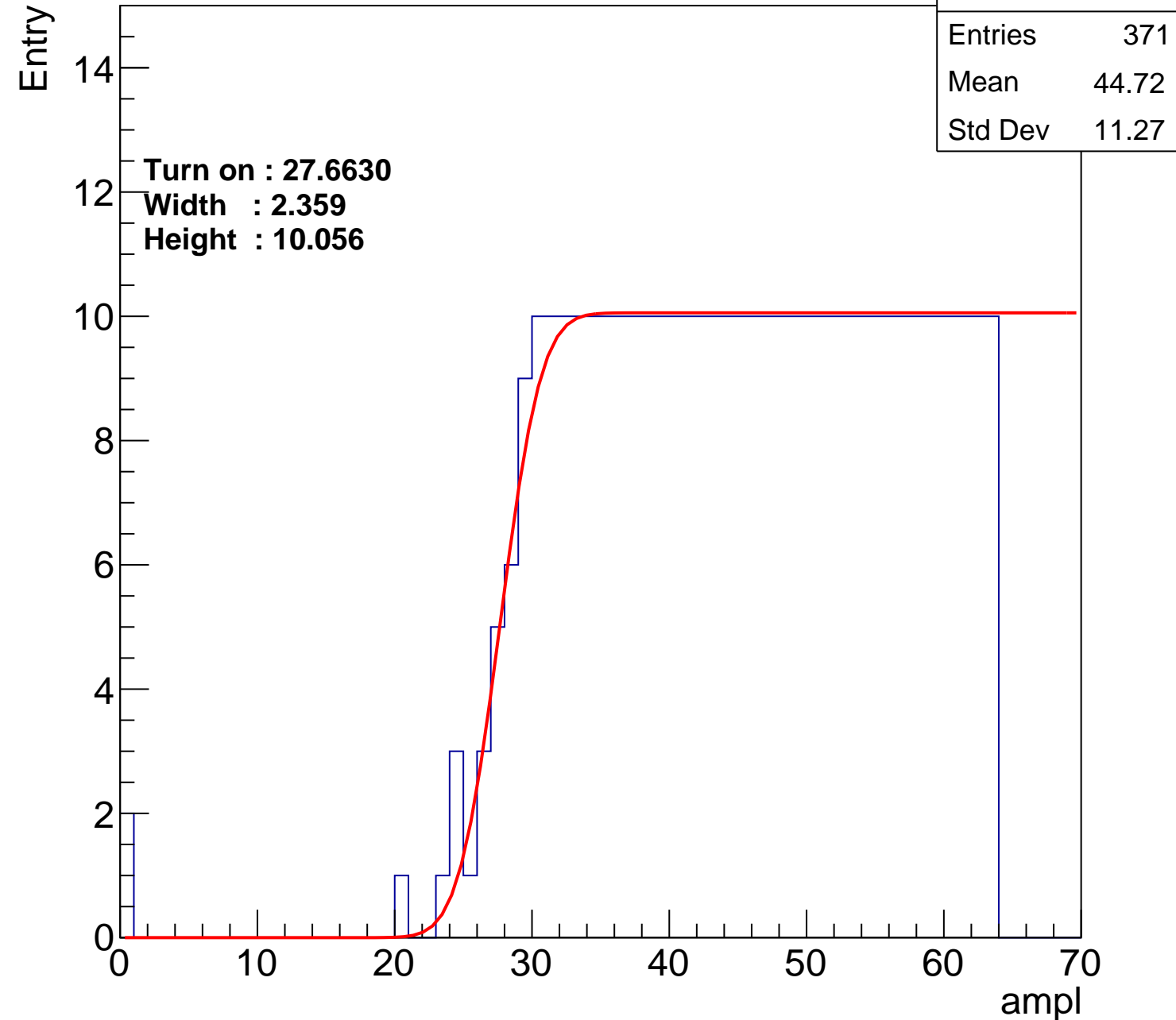
**Width : 2.359**

**Height : 10.056**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch72

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	389
Mean	43.76
Std Dev	11.9

Turn on : 25.7561

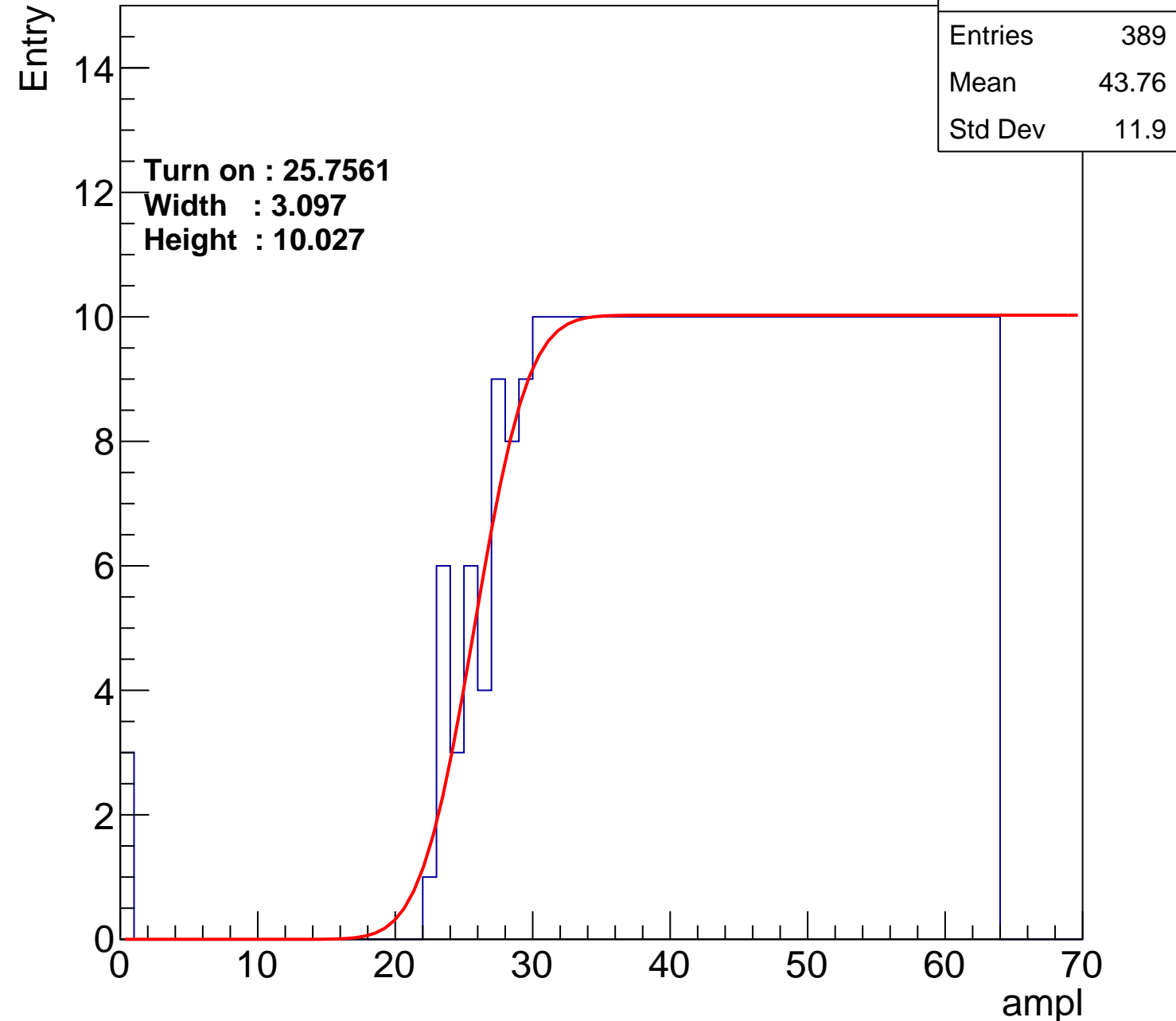
Width : 3.097

Height : 10.027

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch73

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	368
Mean	44.68
Std Dev	11.66

**Turn on : 28.3400**

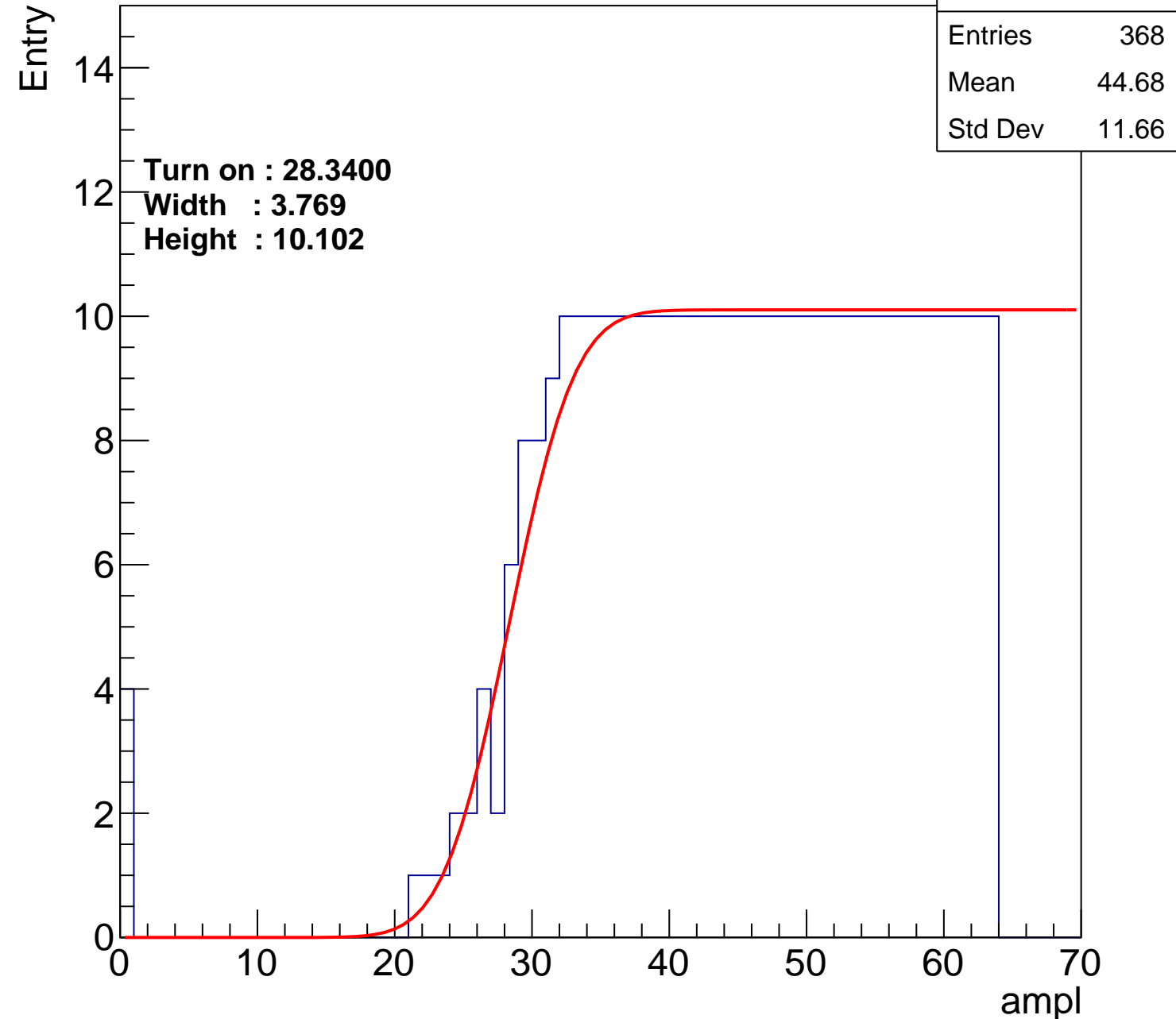
**Width : 3.769**

**Height : 10.102**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch74

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	375
Mean	44.19
Std Dev	12.19

Turn on : 27.1662

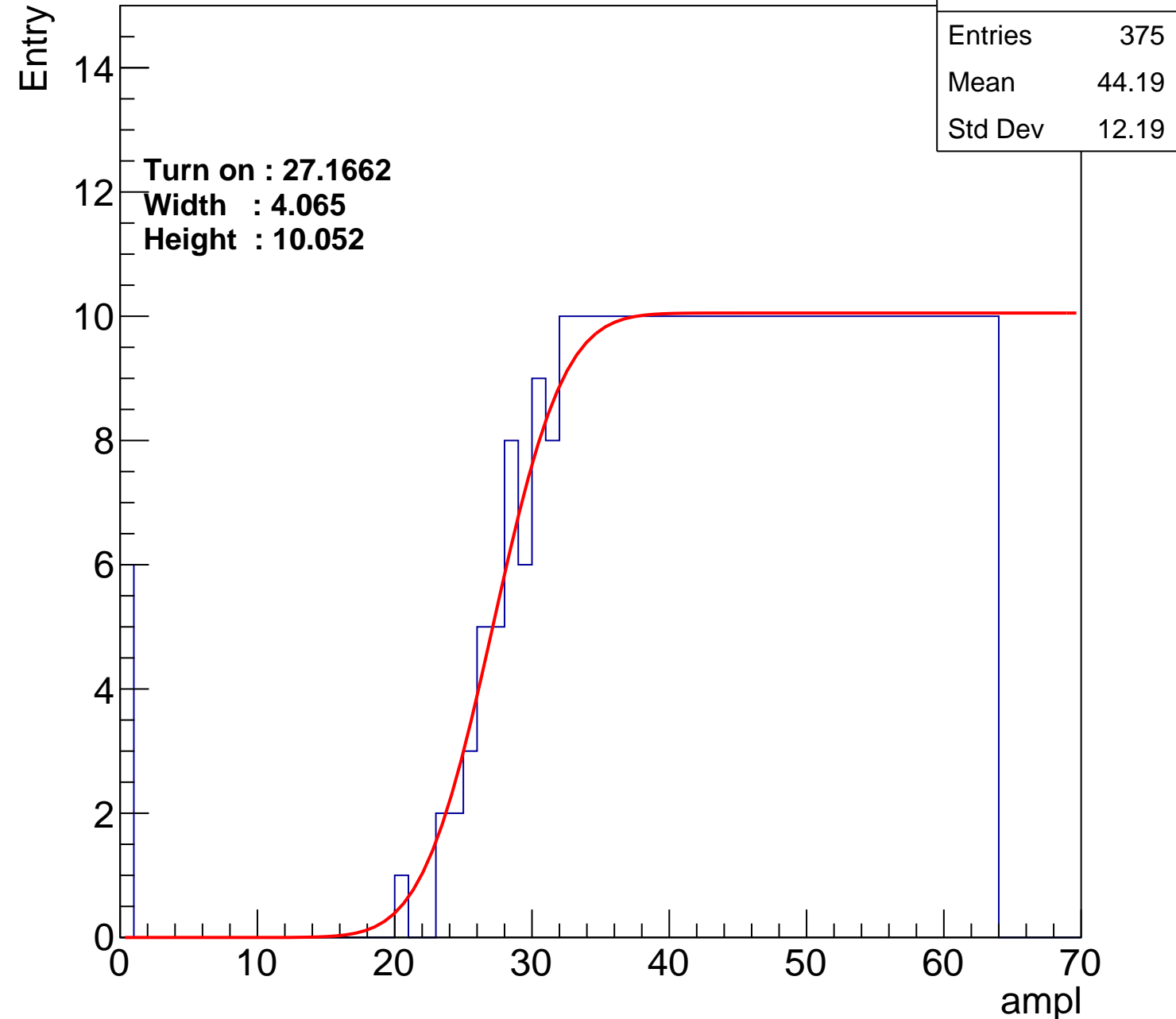
Width : 4.065

Height : 10.052

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch75

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	384
Mean	43.96
Std Dev	11.93

Turn on : 26.1879

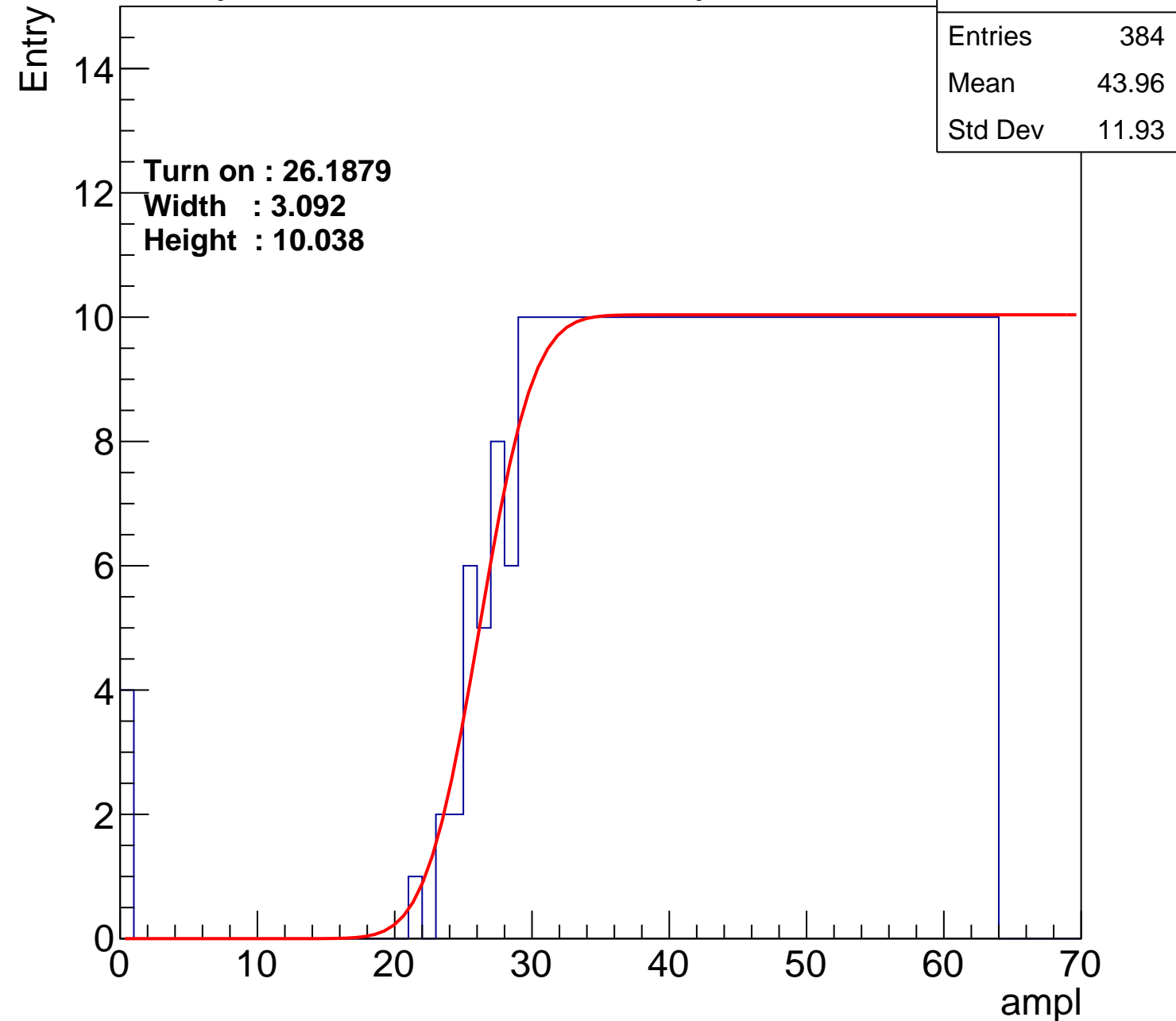
Width : 3.092

Height : 10.038

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch76

calib\_packv5\_042523\_0143.root, FC#0, port D2

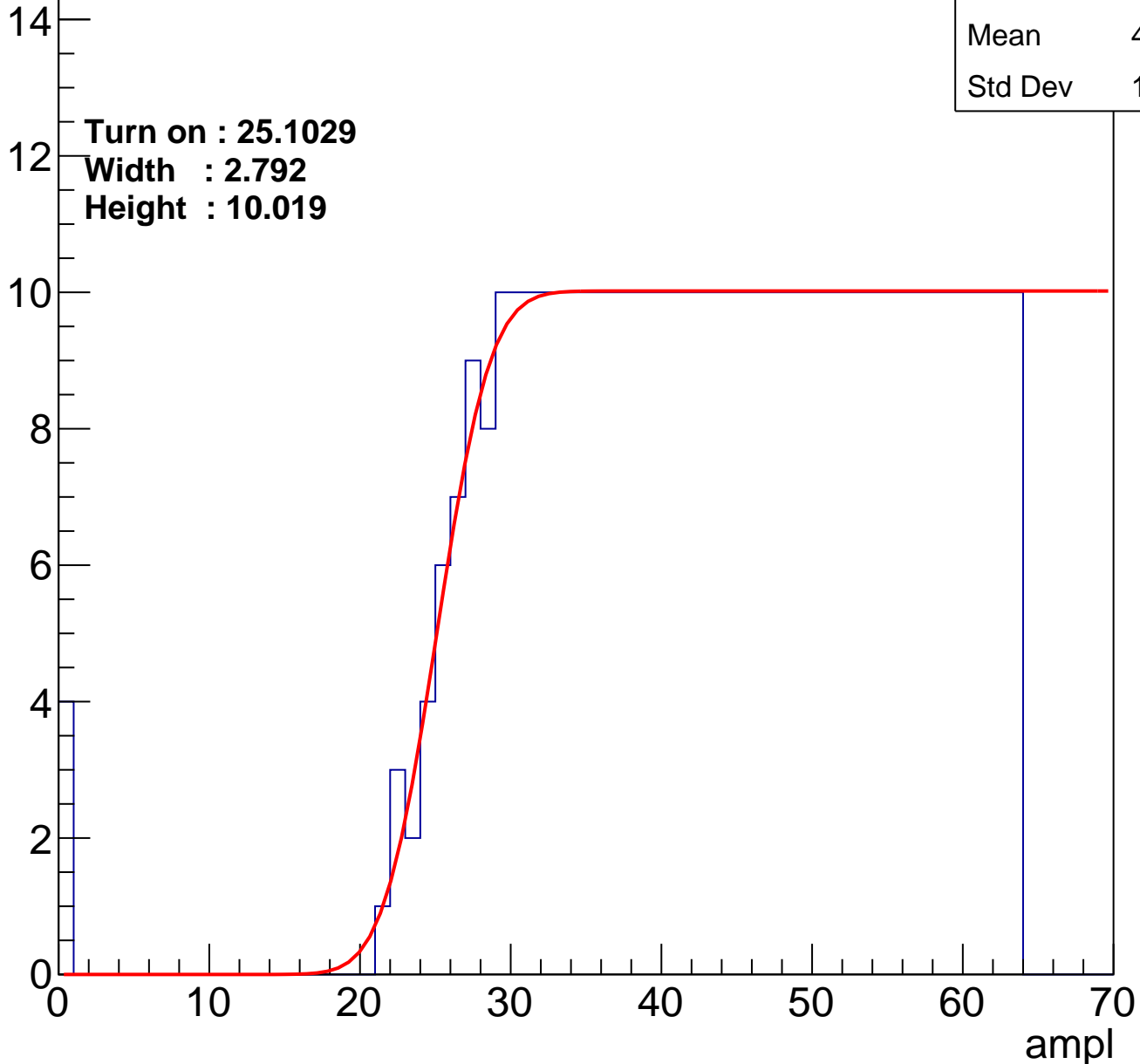
Entries	394
Mean	43.47
Std Dev	12.16

Turn on : 25.1029

Width : 2.792

Height : 10.019

Entry



# B1L101S, U9-ch77

calib\_packv5\_042523\_0143.root, FC#0, port D2

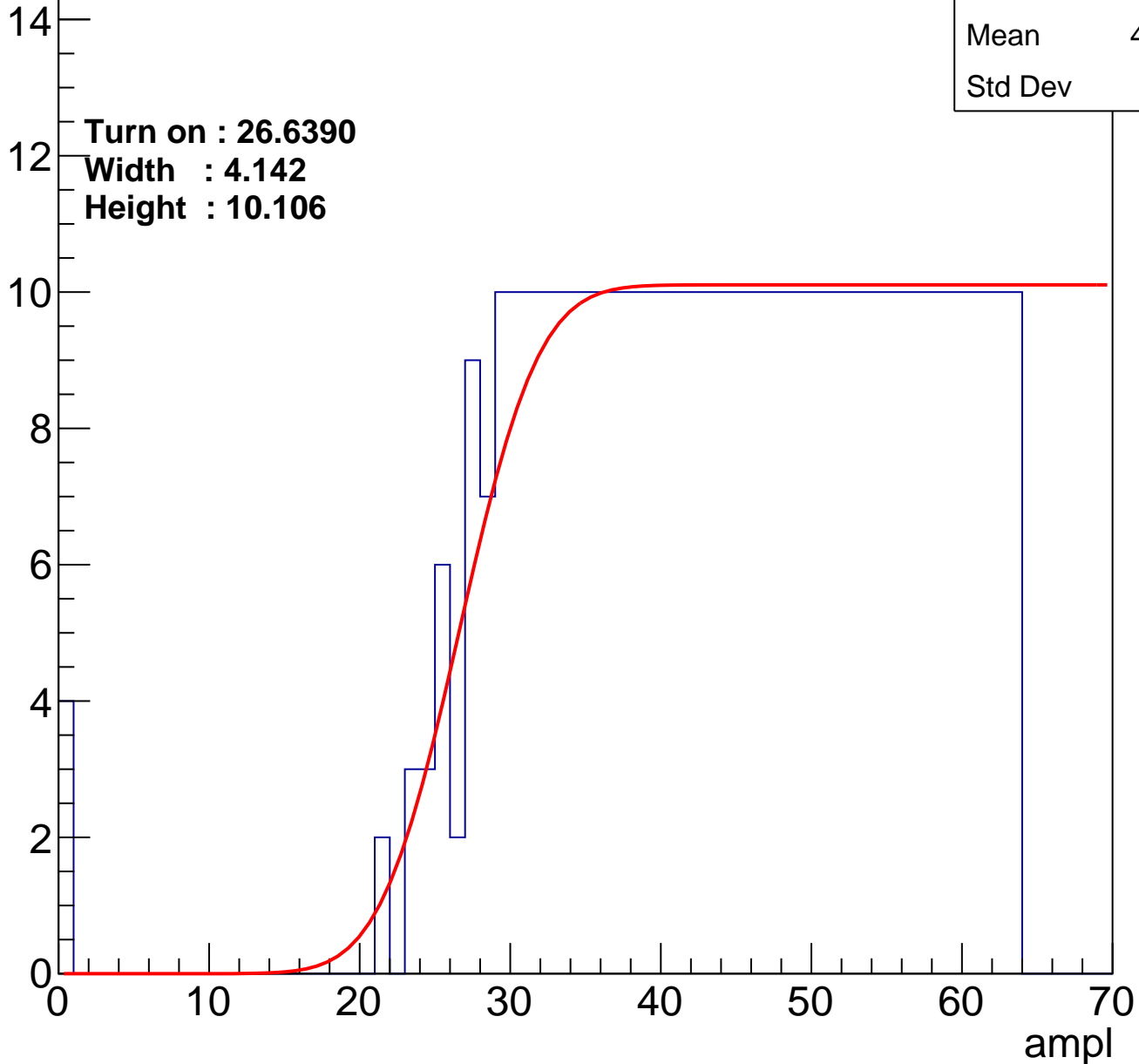
Entries	386
Mean	43.84
Std Dev	12

Turn on : 26.6390

Width : 4.142

Height : 10.106

Entry



# B1L101S, U9-ch78

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	384
Mean	43.92
Std Dev	11.99

Turn on : 26.4513

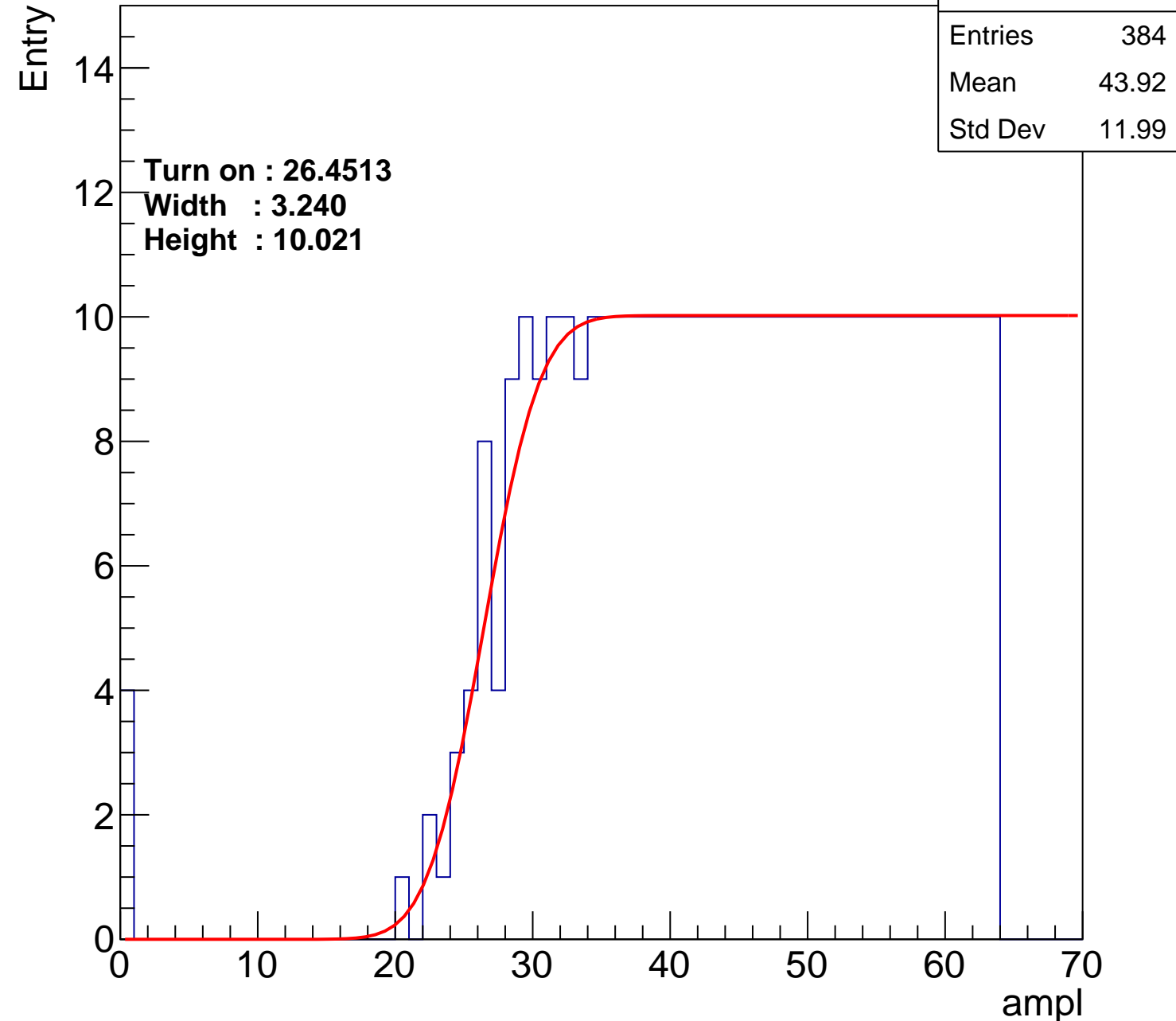
Width : 3.240

Height : 10.021

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L101S, U9-ch79

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	380
Mean	44.37
Std Dev	11.27

**Turn on : 26.3497**

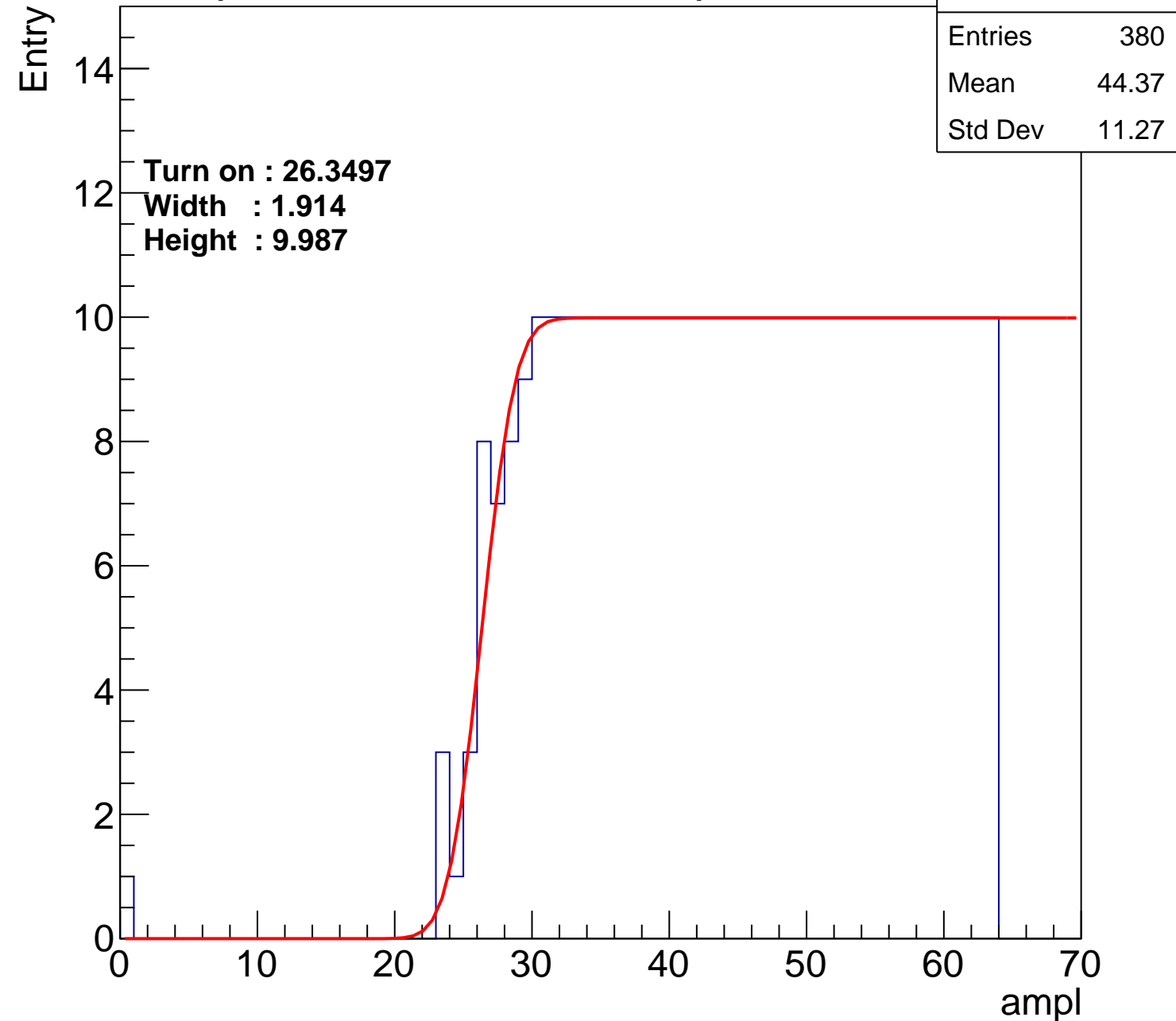
**Width : 1.914**

**Height : 9.987**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch80

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	395
Mean	43.51
Std Dev	11.99

Turn on : 25.4392

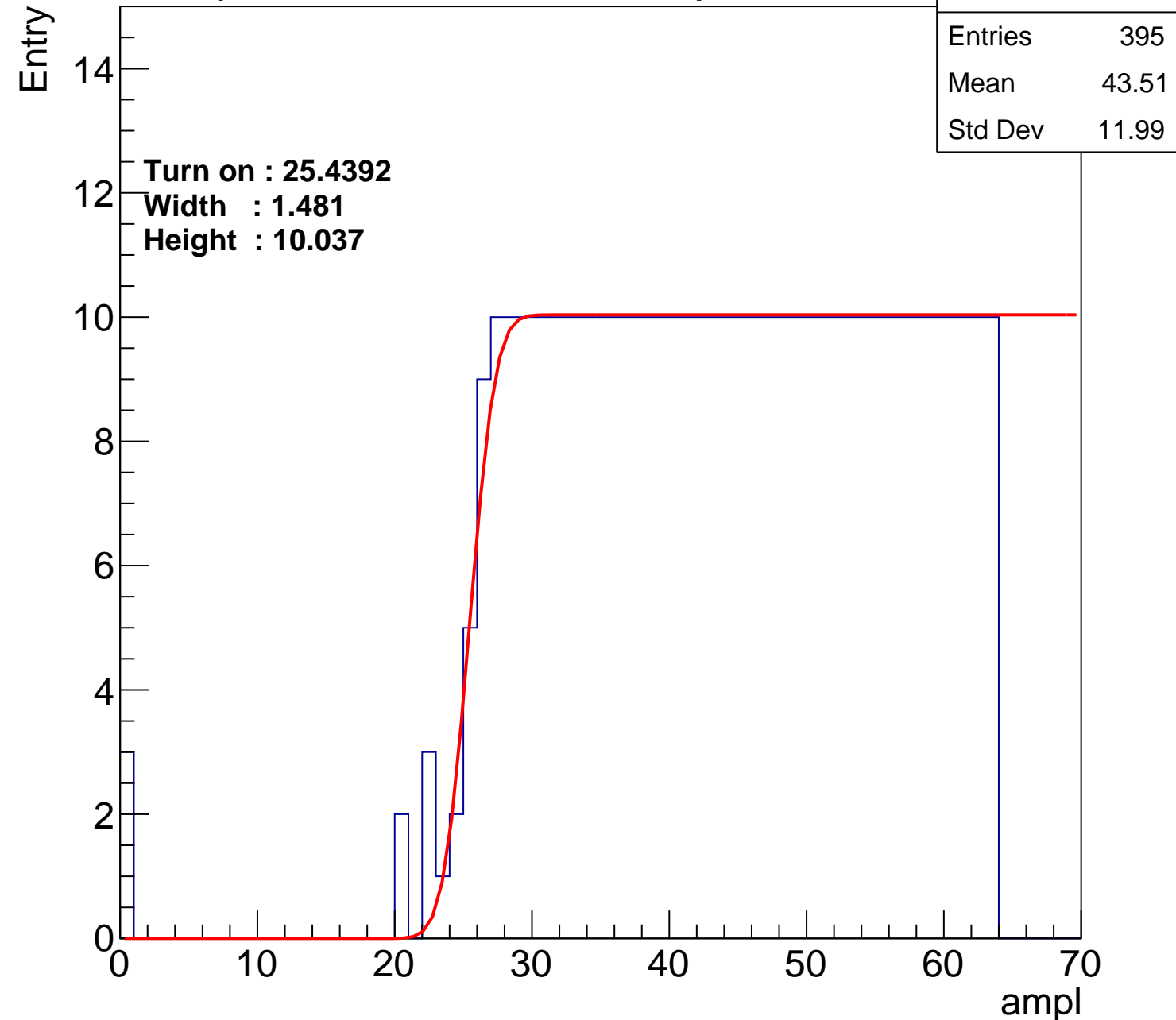
Width : 1.481

Height : 10.037

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch81

calib\_packv5\_042523\_0143.root, FC#0, port D2

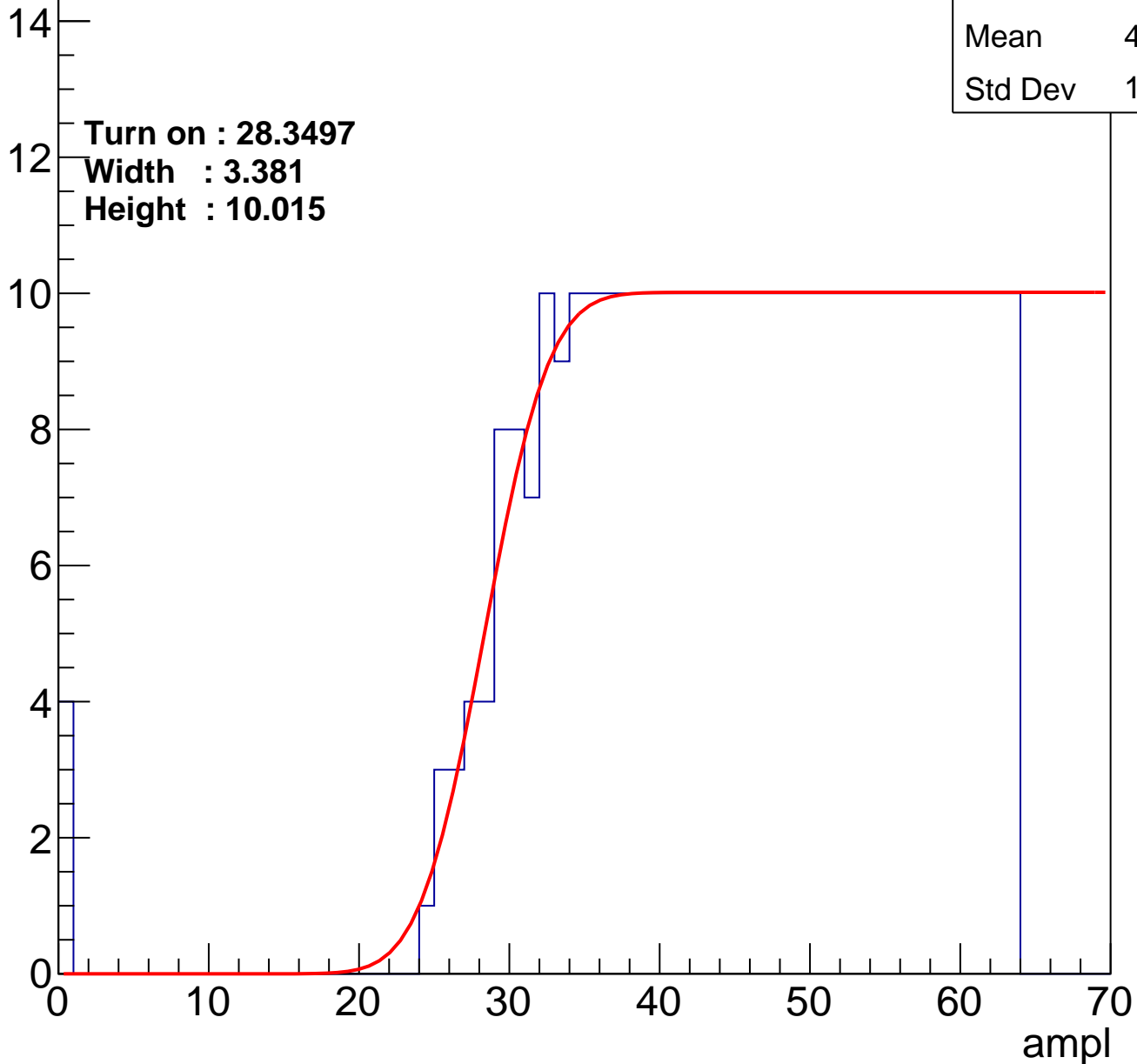
Entries	361
Mean	45.02
Std Dev	11.49

**Turn on : 28.3497**

**Width : 3.381**

**Height : 10.015**

Entry



# B1L101S, U9-ch82

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	391
Mean	43.37
Std Dev	12.71

Turn on : 25.8072

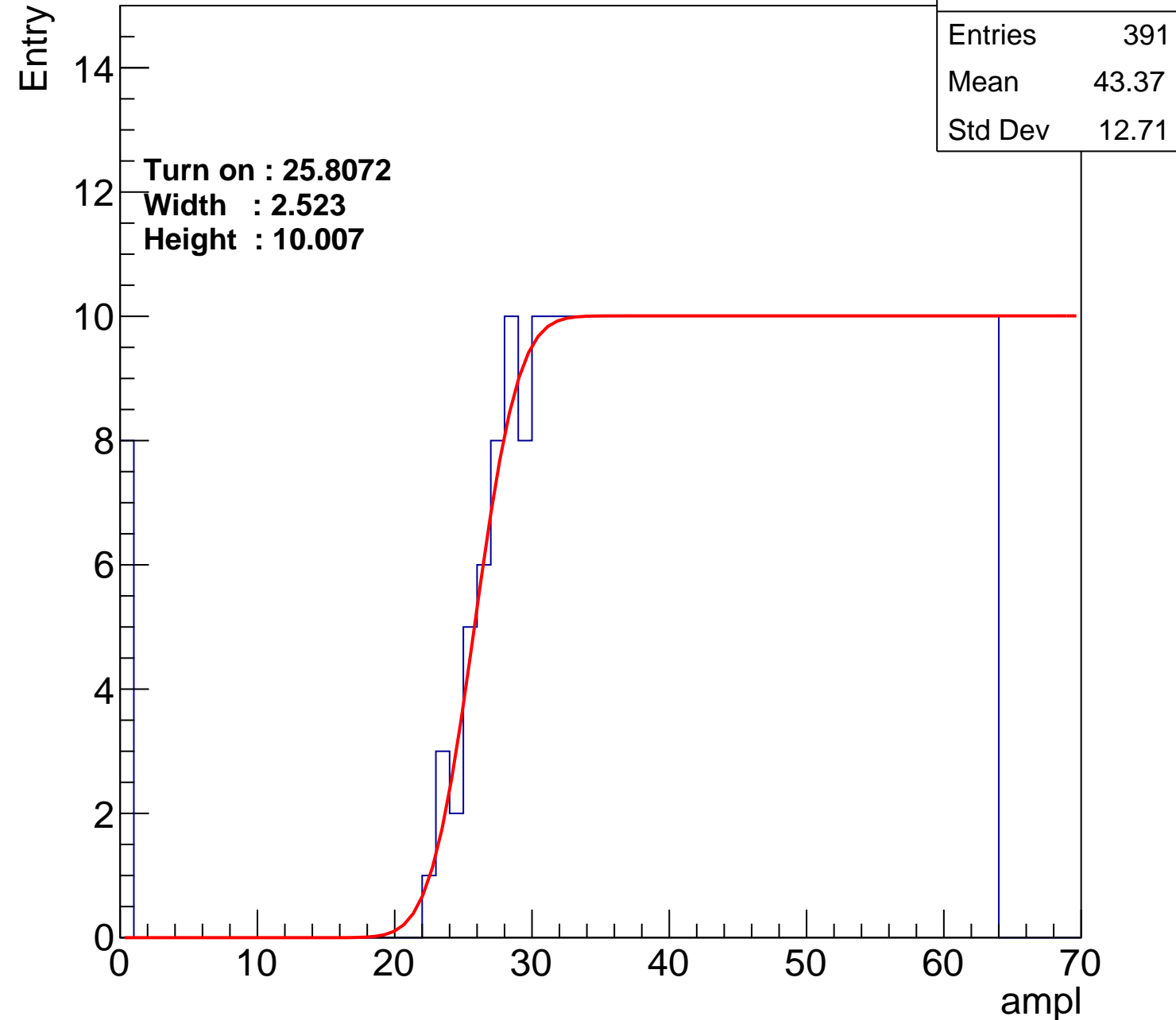
Width : 2.523

Height : 10.007

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch83

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	371
Mean	44.52
Std Dev	11.74

Turn on : 27.5752

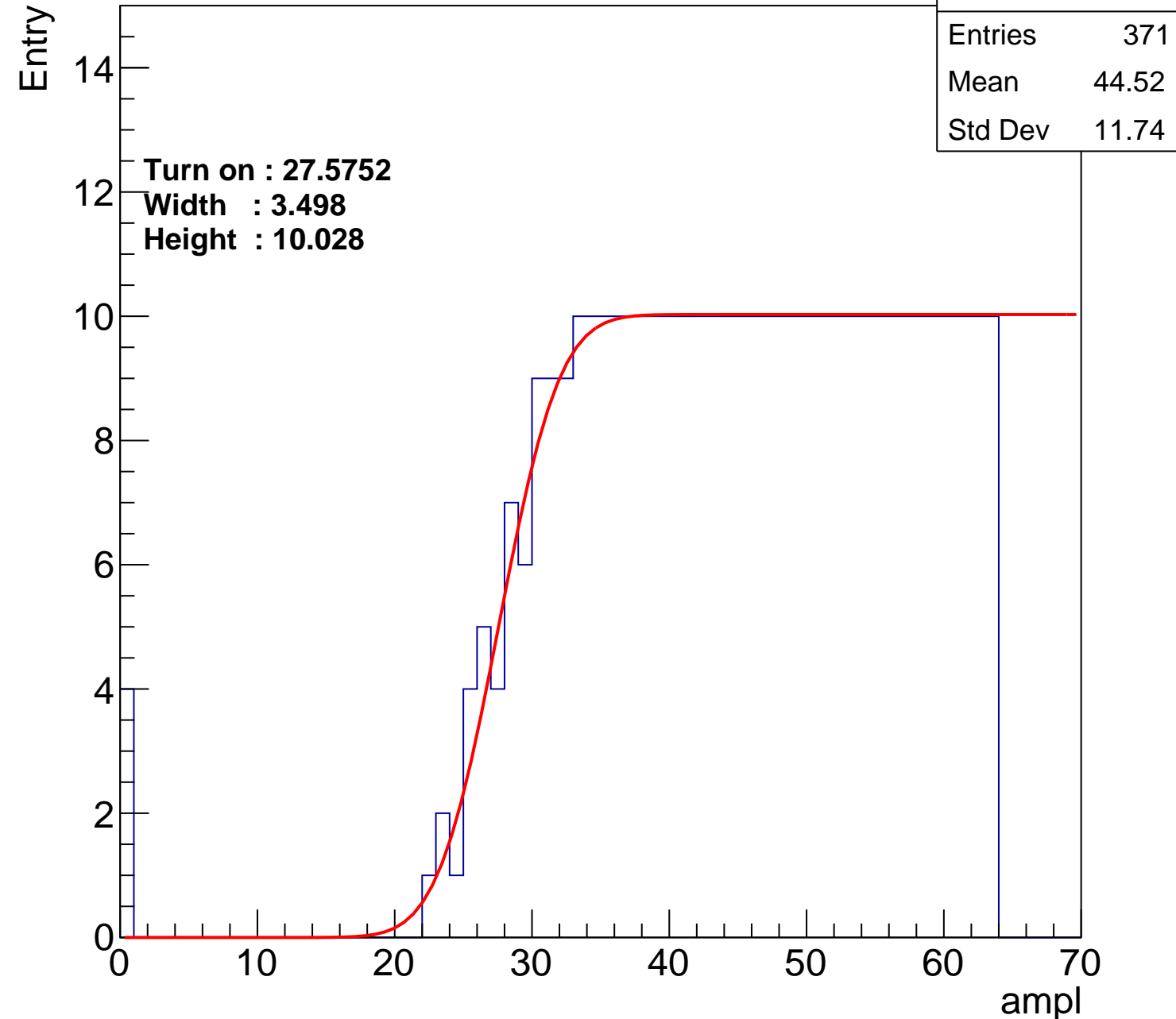
Width : 3.498

Height : 10.028

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch84

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	378
Mean	44.19
Std Dev	11.96

Turn on : 27.0751

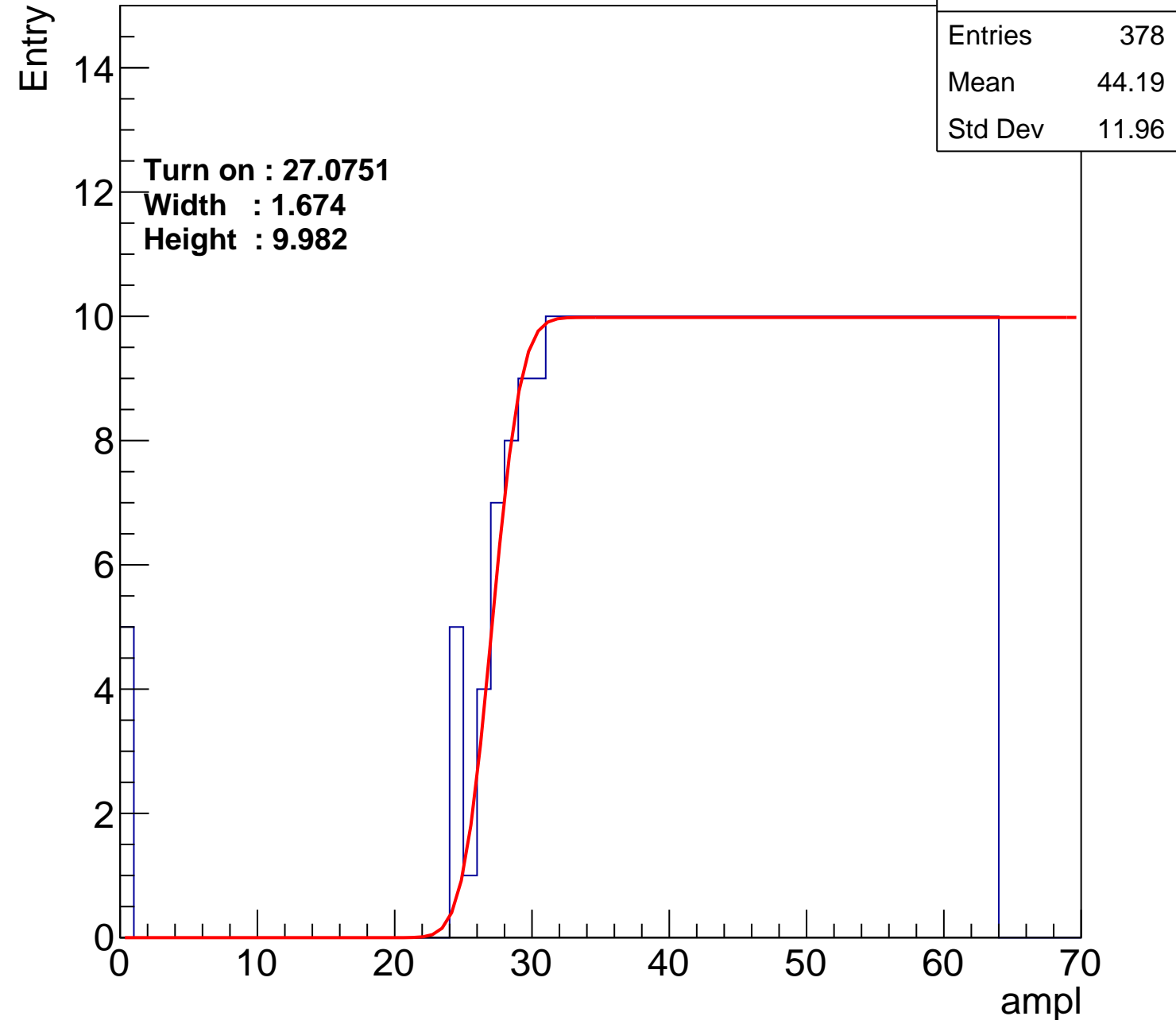
Width : 1.674

Height : 9.982

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch85

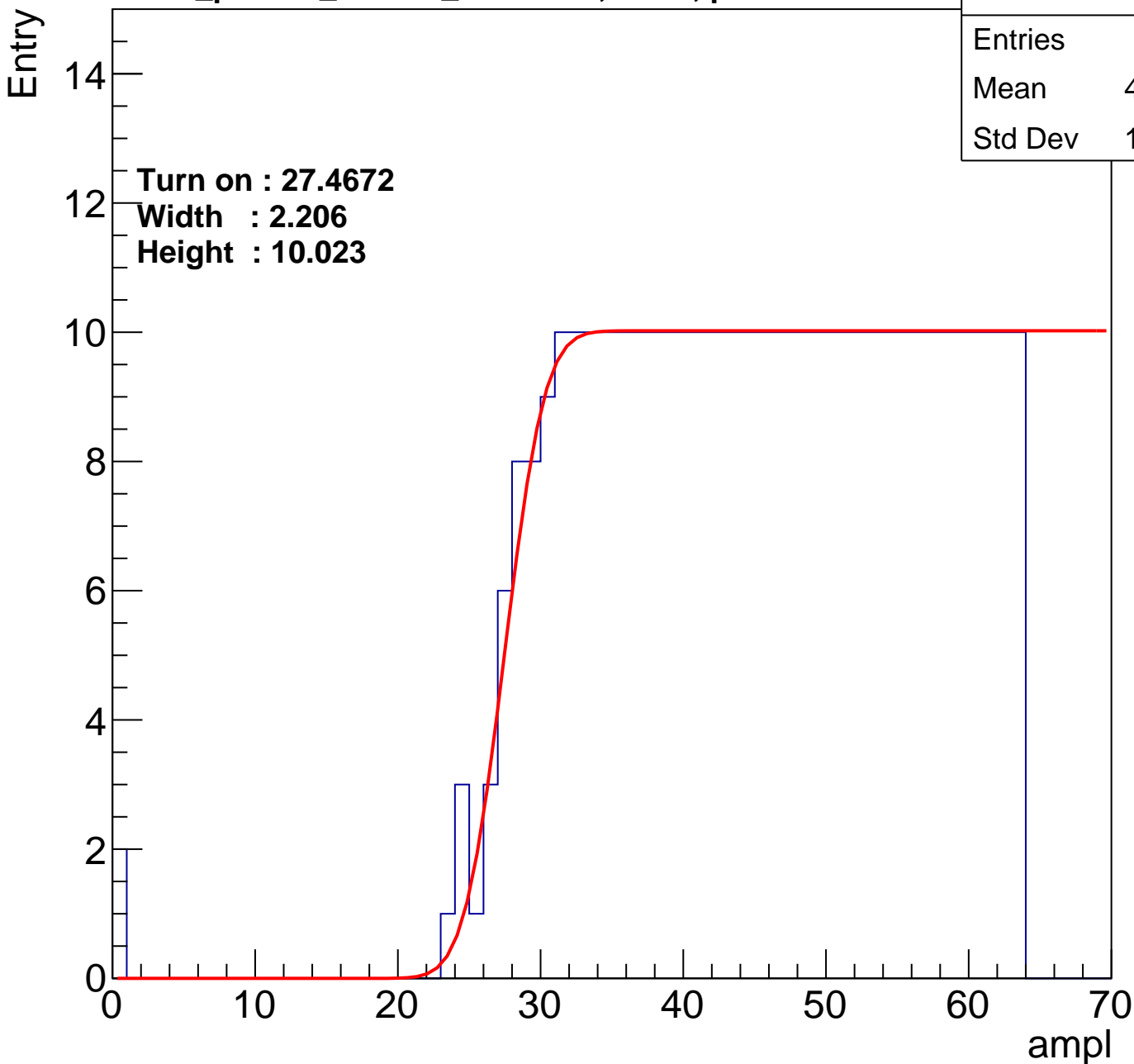
**calib\_packv5\_042523\_0143.root, FC#0, port D2**

Entries	371
Mean	44.73
Std Dev	11.24

**Turn on : 27.4672**

**Width : 2.206**

**Height : 10.023**



# B1L101S, U9-ch86

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	366
Mean	44.99
Std Dev	11.01

Turn on : 28.0973

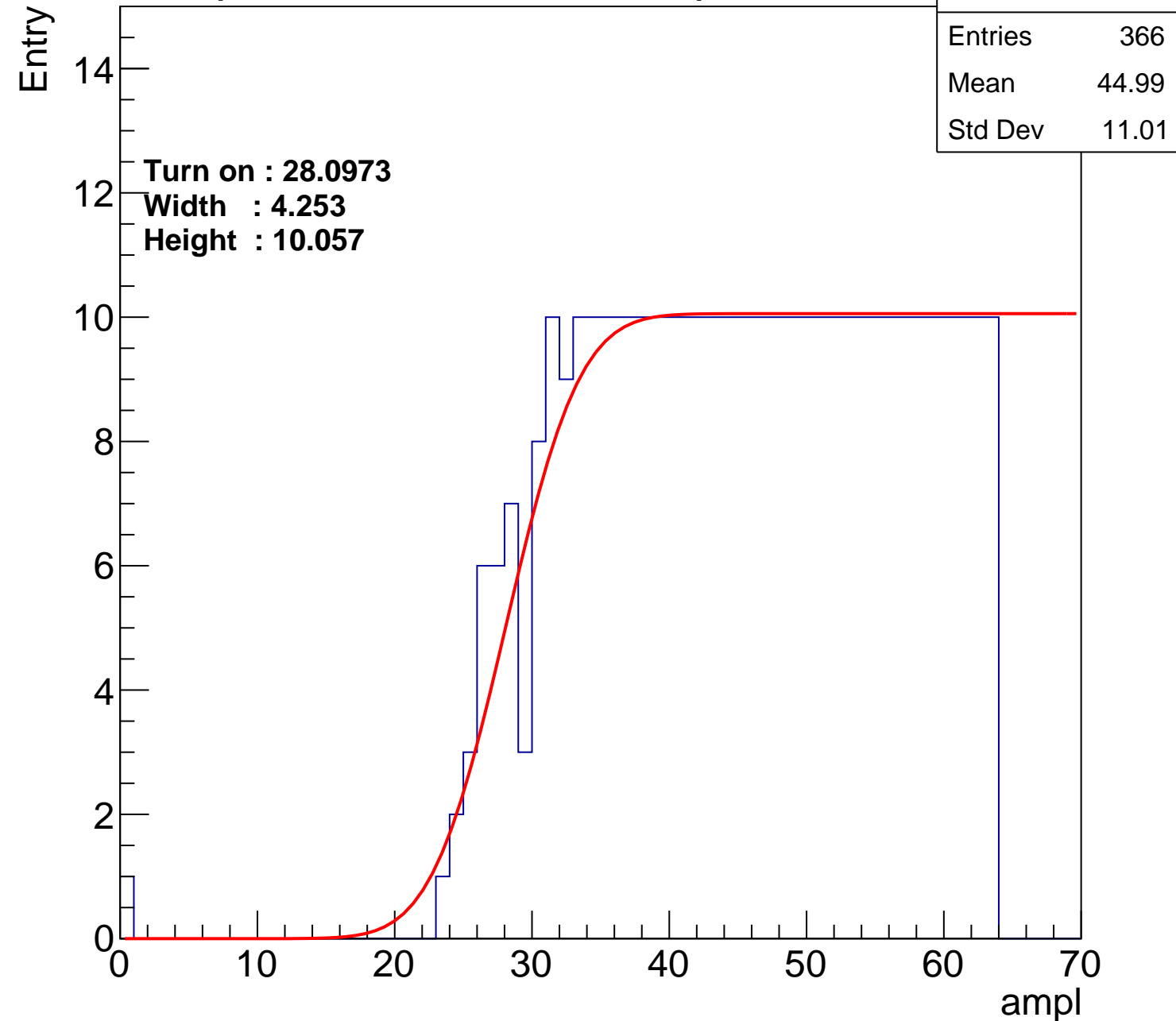
Width : 4.253

Height : 10.057

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L101S, U9-ch87

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	401
Mean	42.88
Std Dev	12.93

Turn on : 24.7391

Width : 2.147

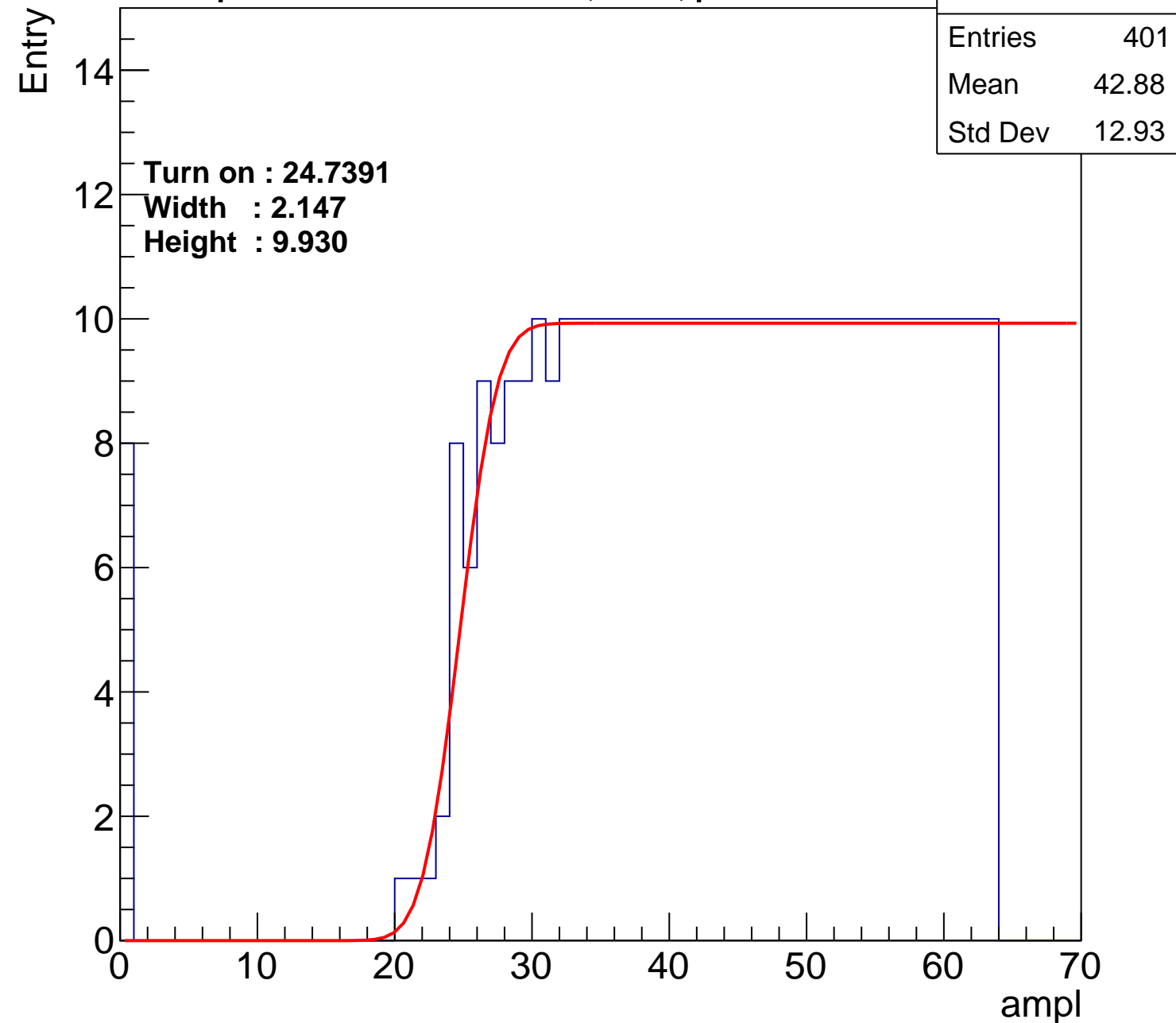
Height : 9.930

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U9-ch88

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	353
Mean	45.5
Std Dev	11.07

Turn on : 28.5660

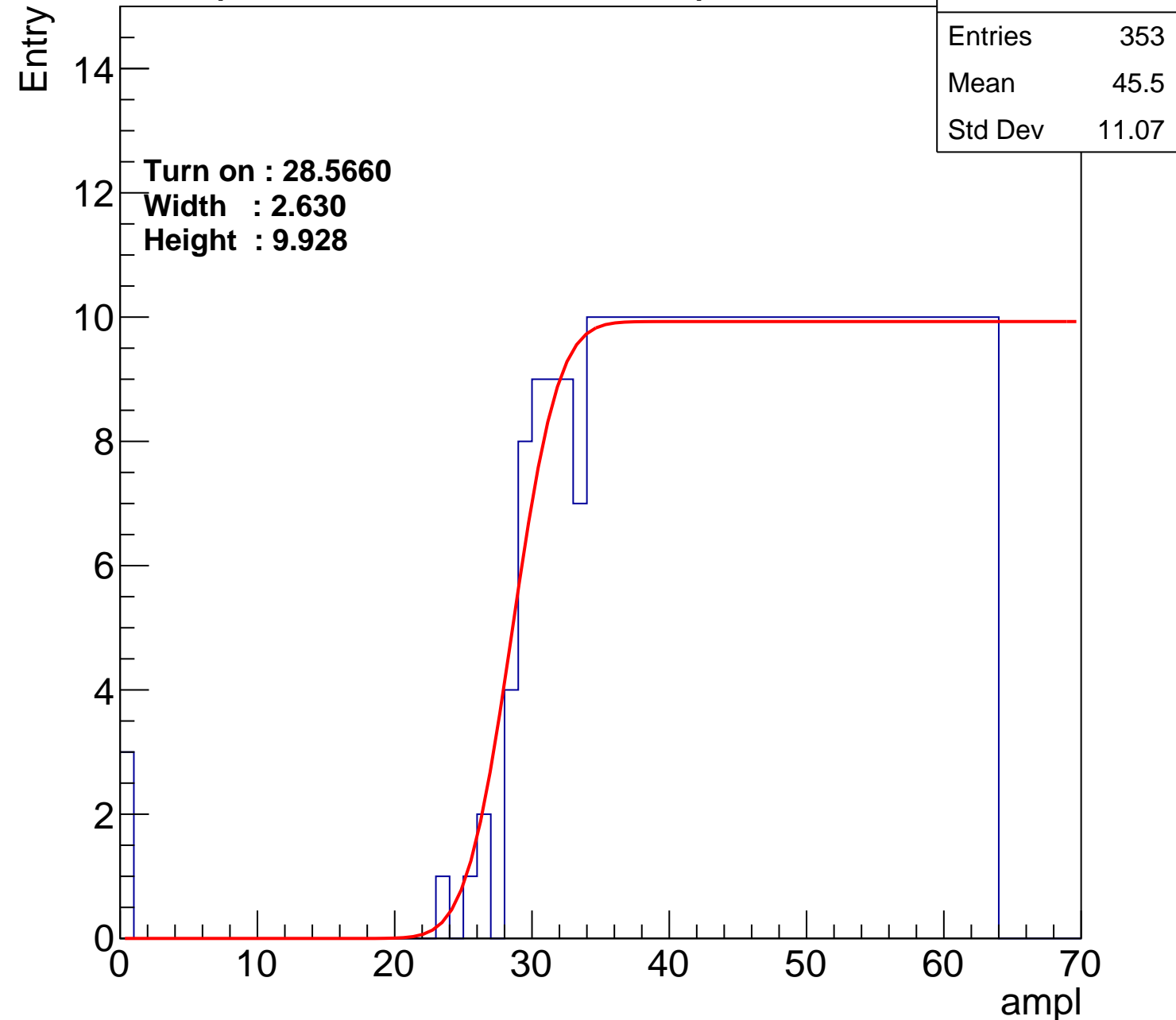
Width : 2.630

Height : 9.928

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch89

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	379
Mean	44.31
Std Dev	11.49

**Turn on : 25.0078**

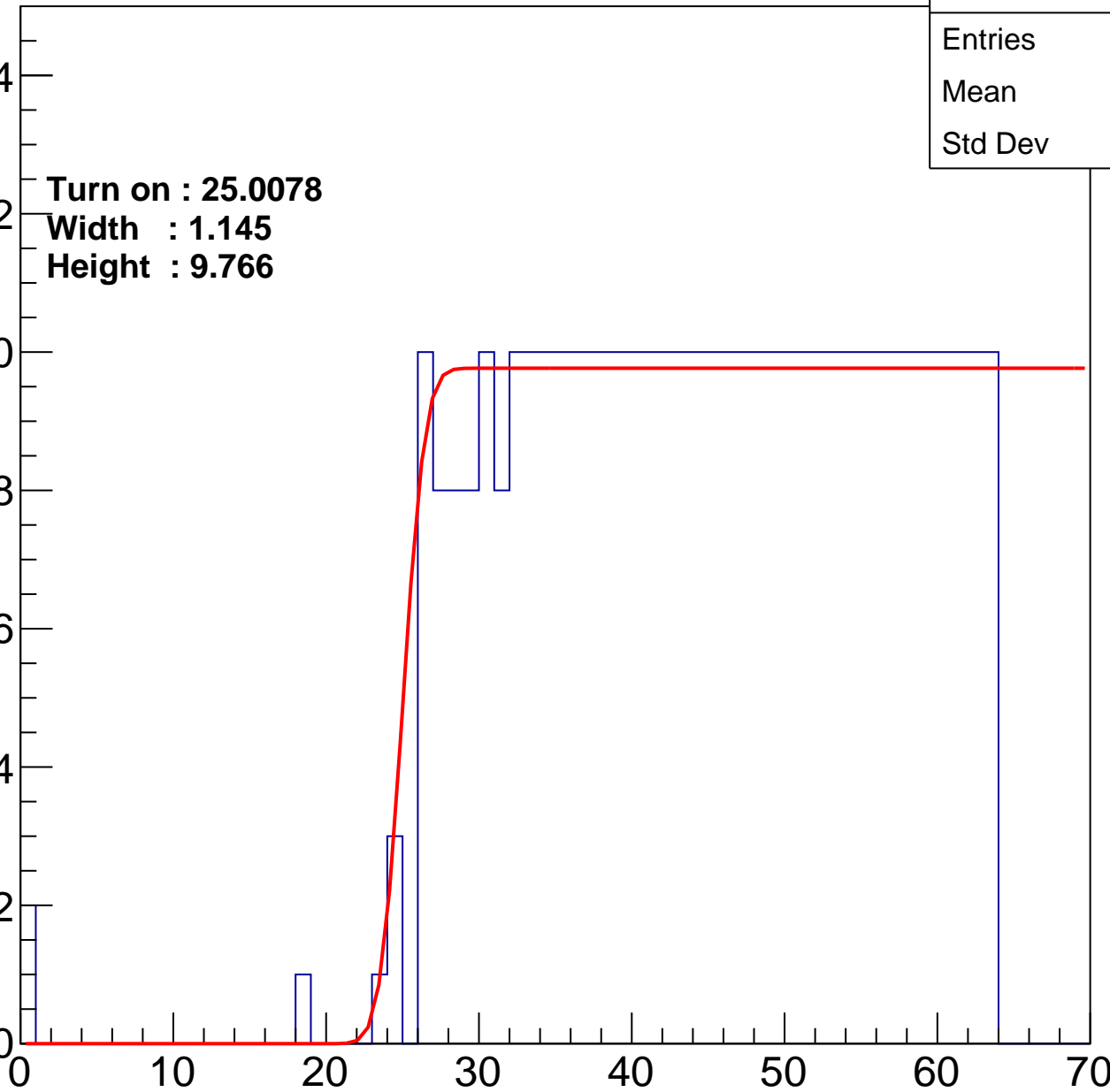
**Width : 1.145**

**Height : 9.766**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch90

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	378
Mean	44.37
Std Dev	11.45

Turn on : 26.3236

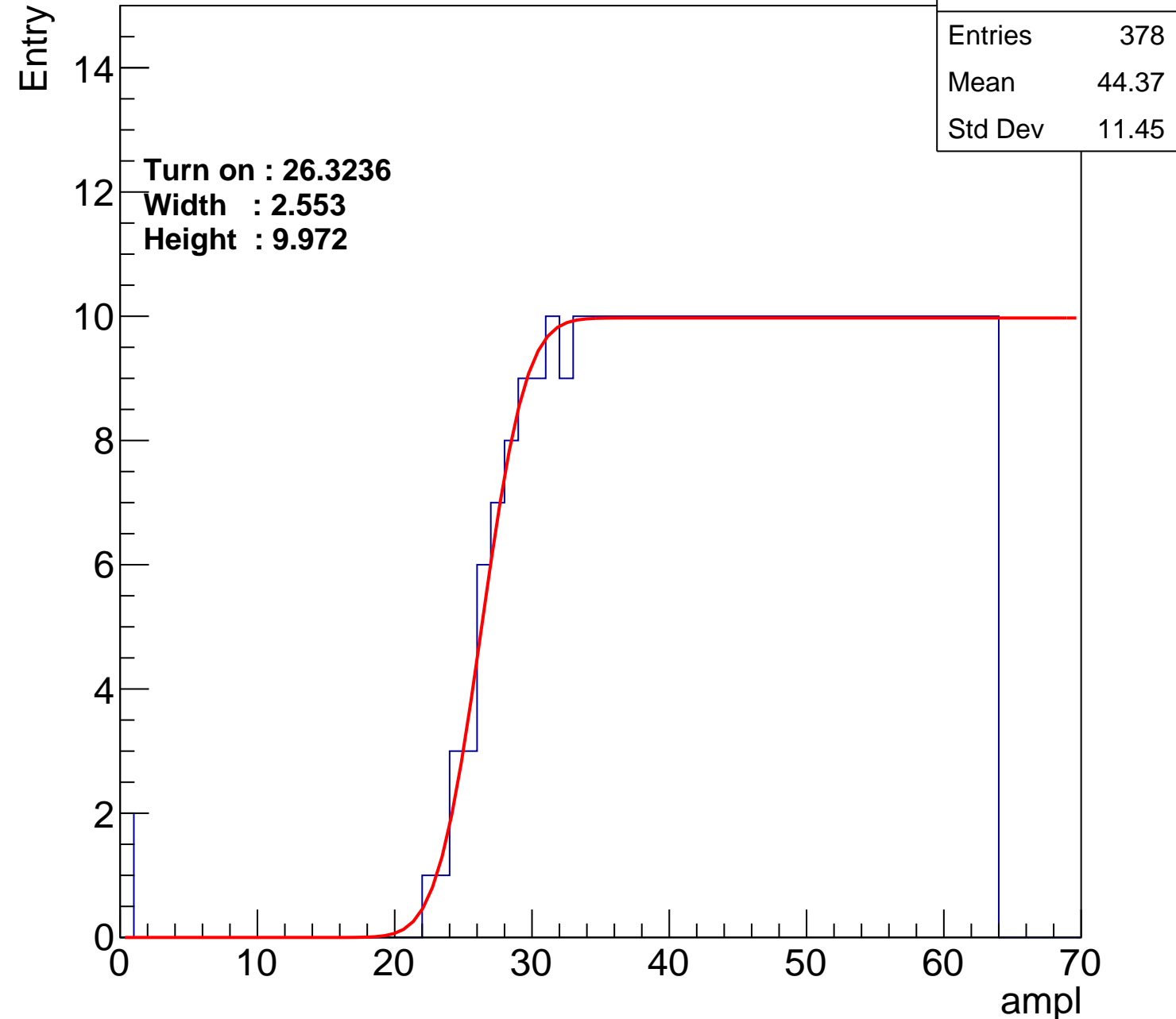
Width : 2.553

Height : 9.972

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch91

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	385
Mean	43.93
Std Dev	11.85

Turn on : 25.7814

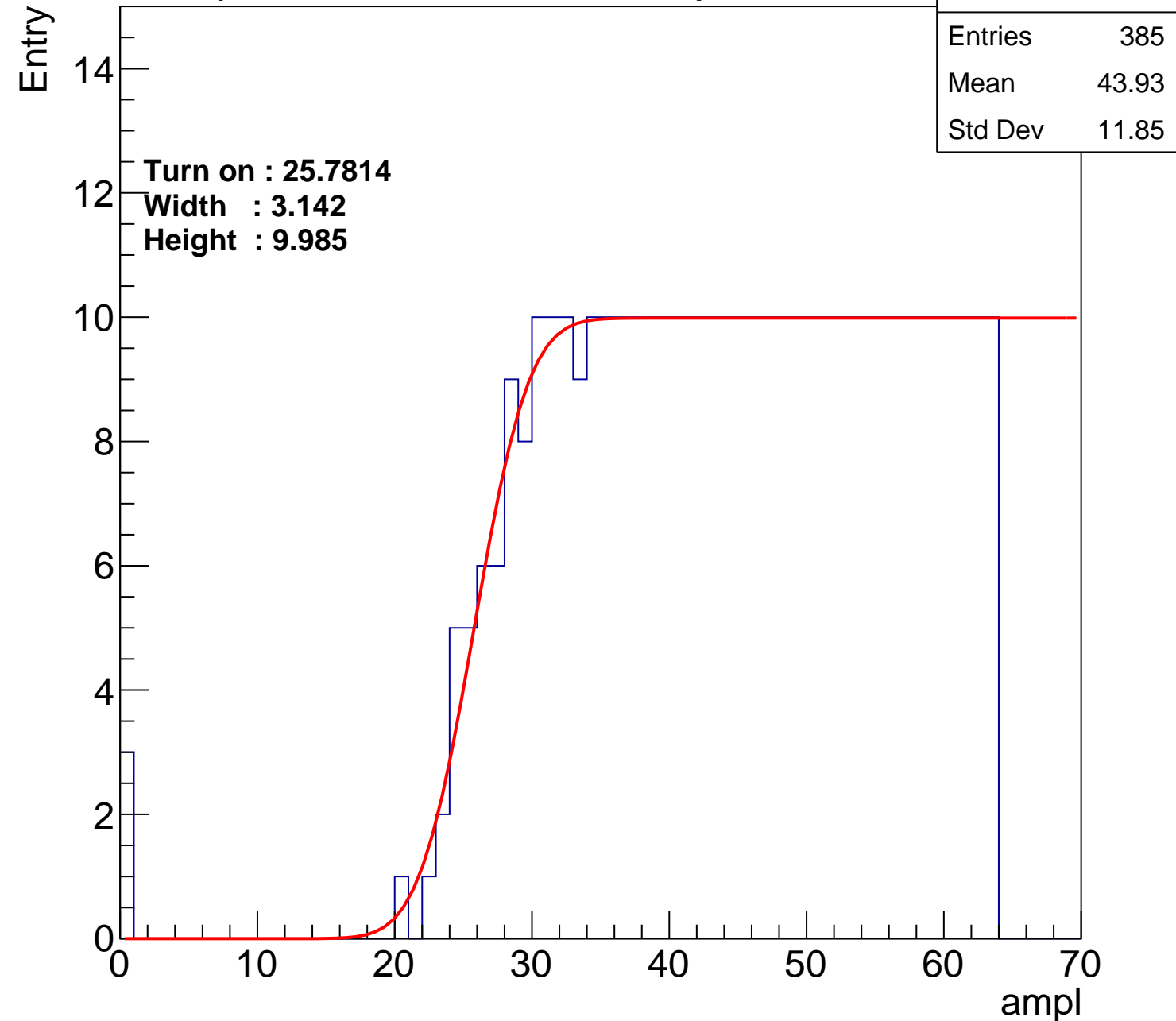
Width : 3.142

Height : 9.985

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch92

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	380
Mean	44.23
Std Dev	11.65

**Turn on : 26.3416**

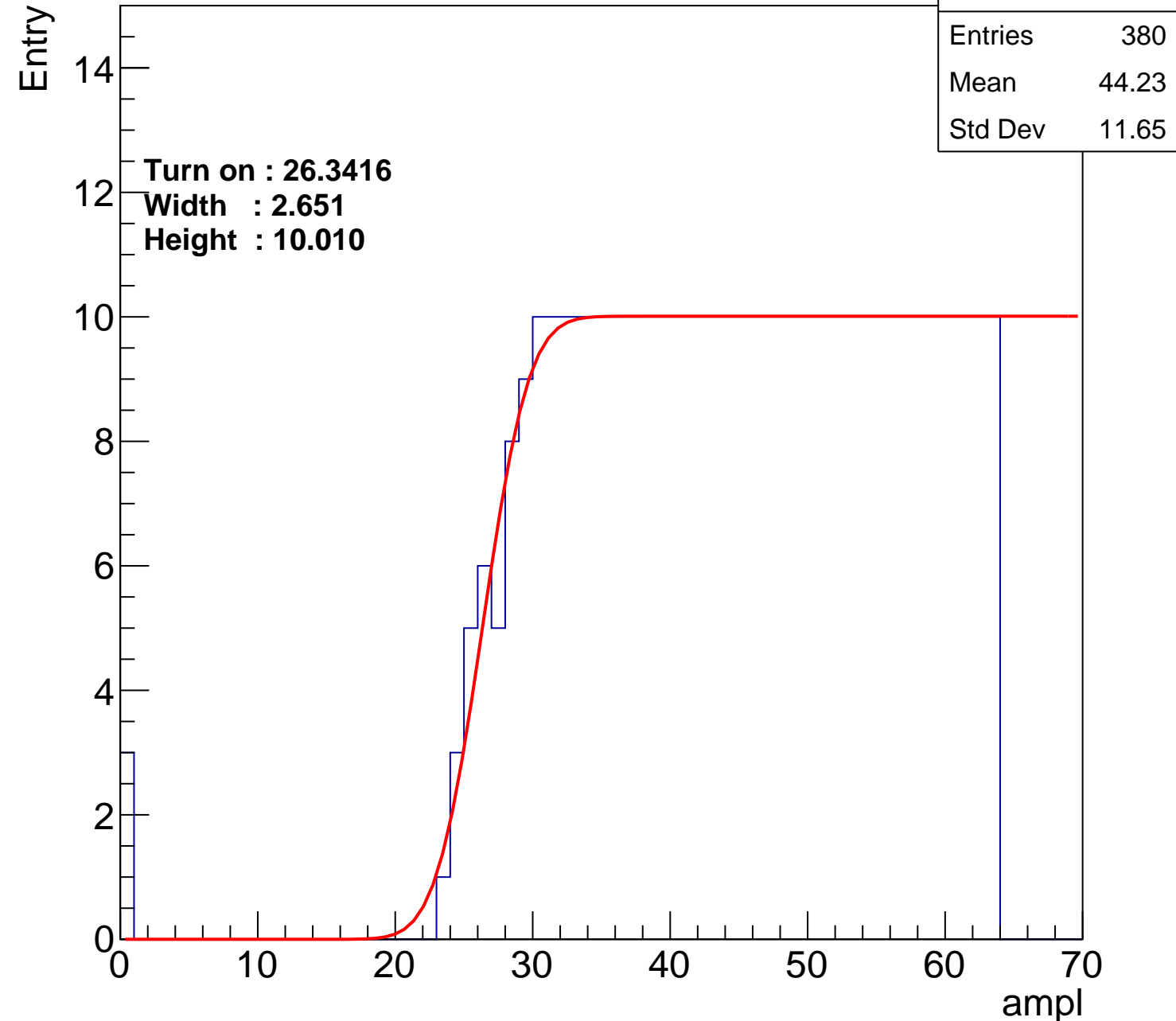
**Width : 2.651**

**Height : 10.010**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch93

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	355
Mean	45.27
Std Dev	11.52

**Turn on : 29.3299**

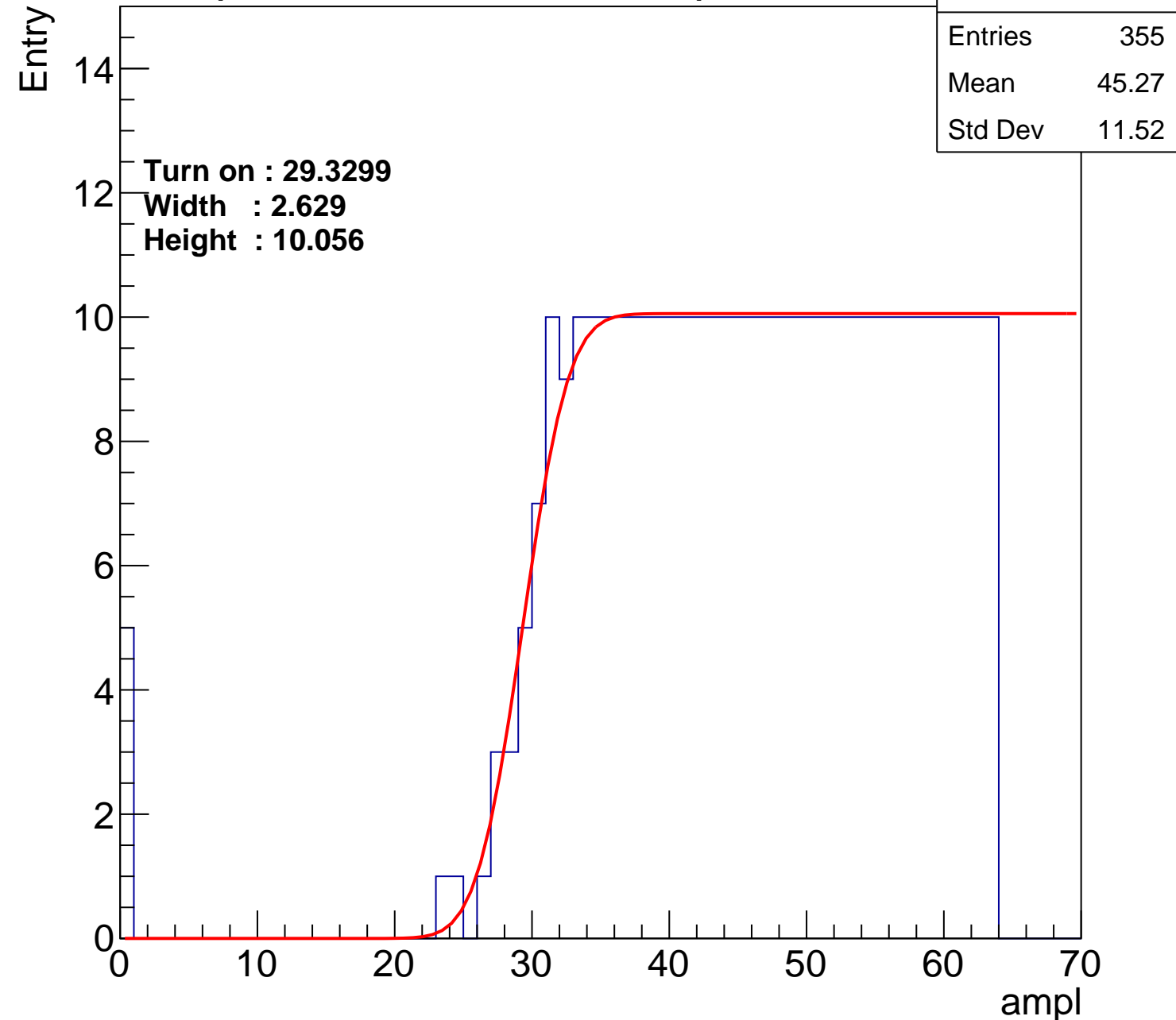
**Width : 2.629**

**Height : 10.056**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch94

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	368
Mean	44.8
Std Dev	11.38

Turn on : 27.1753

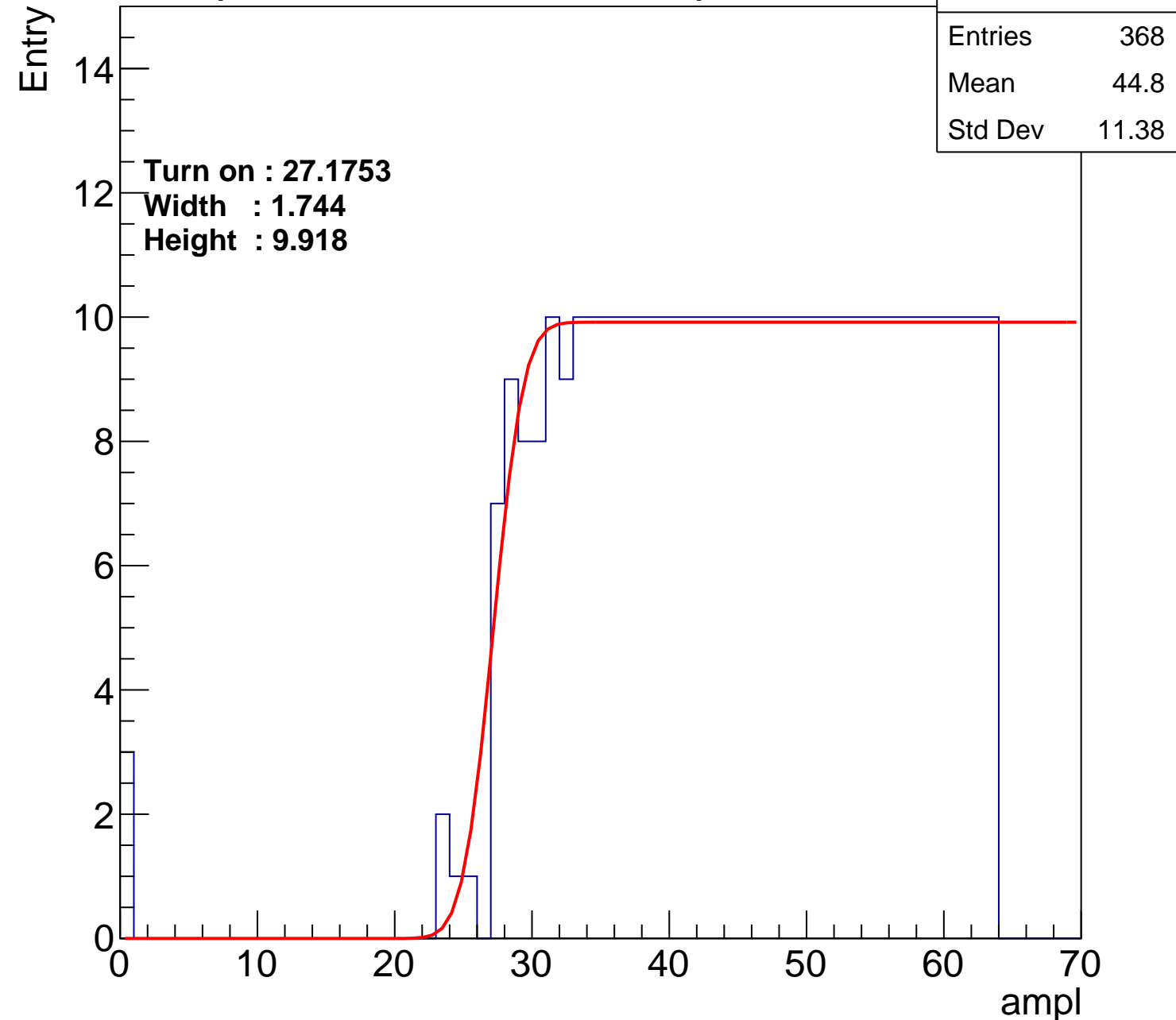
Width : 1.744

Height : 9.918

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L101S, U9-ch95

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	374
Mean	44.63
Std Dev	11.16

Turn on : 27.2025

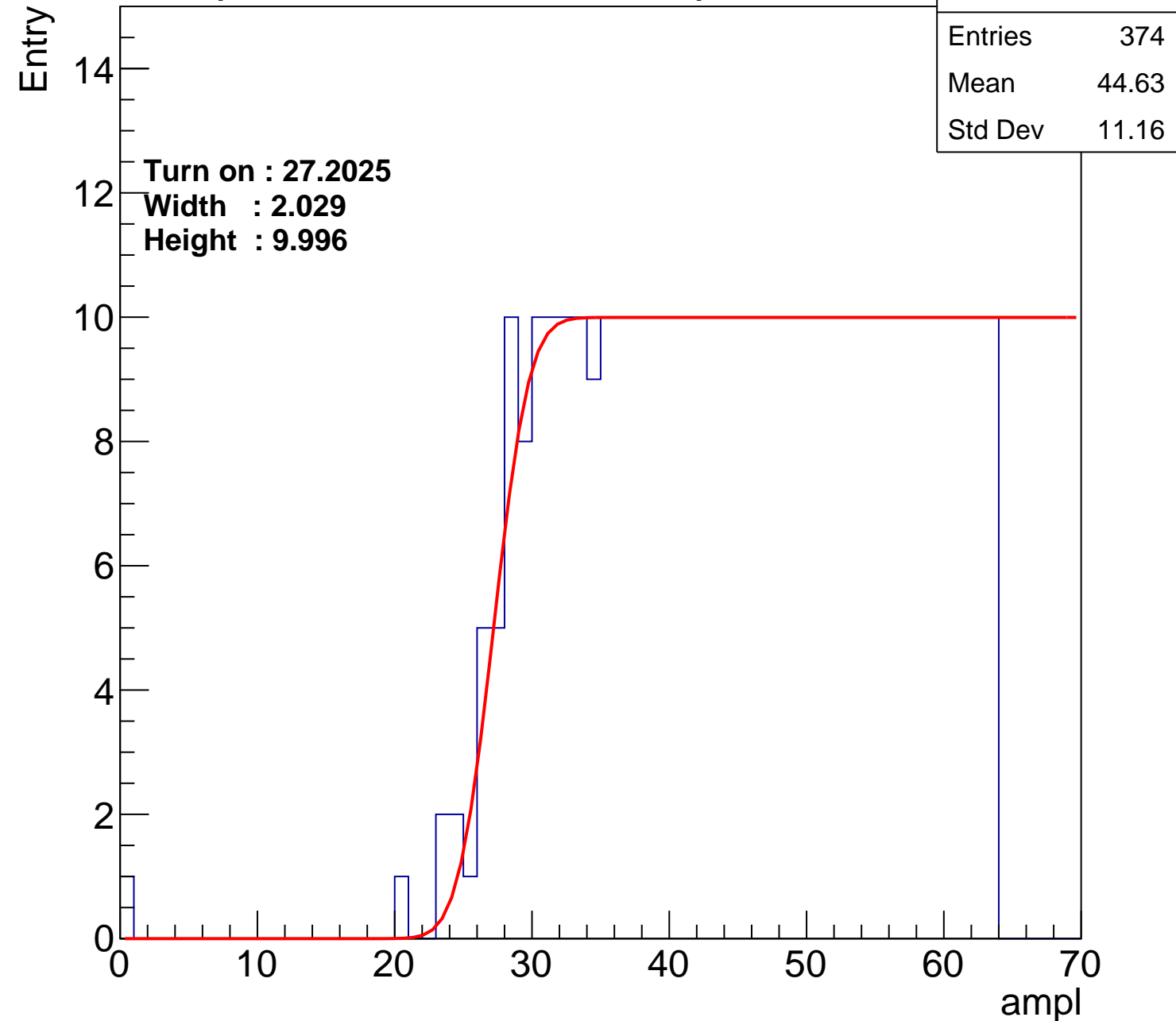
Width : 2.029

Height : 9.996

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch96

calib\_packv5\_042523\_0143.root, FC#0, port D2

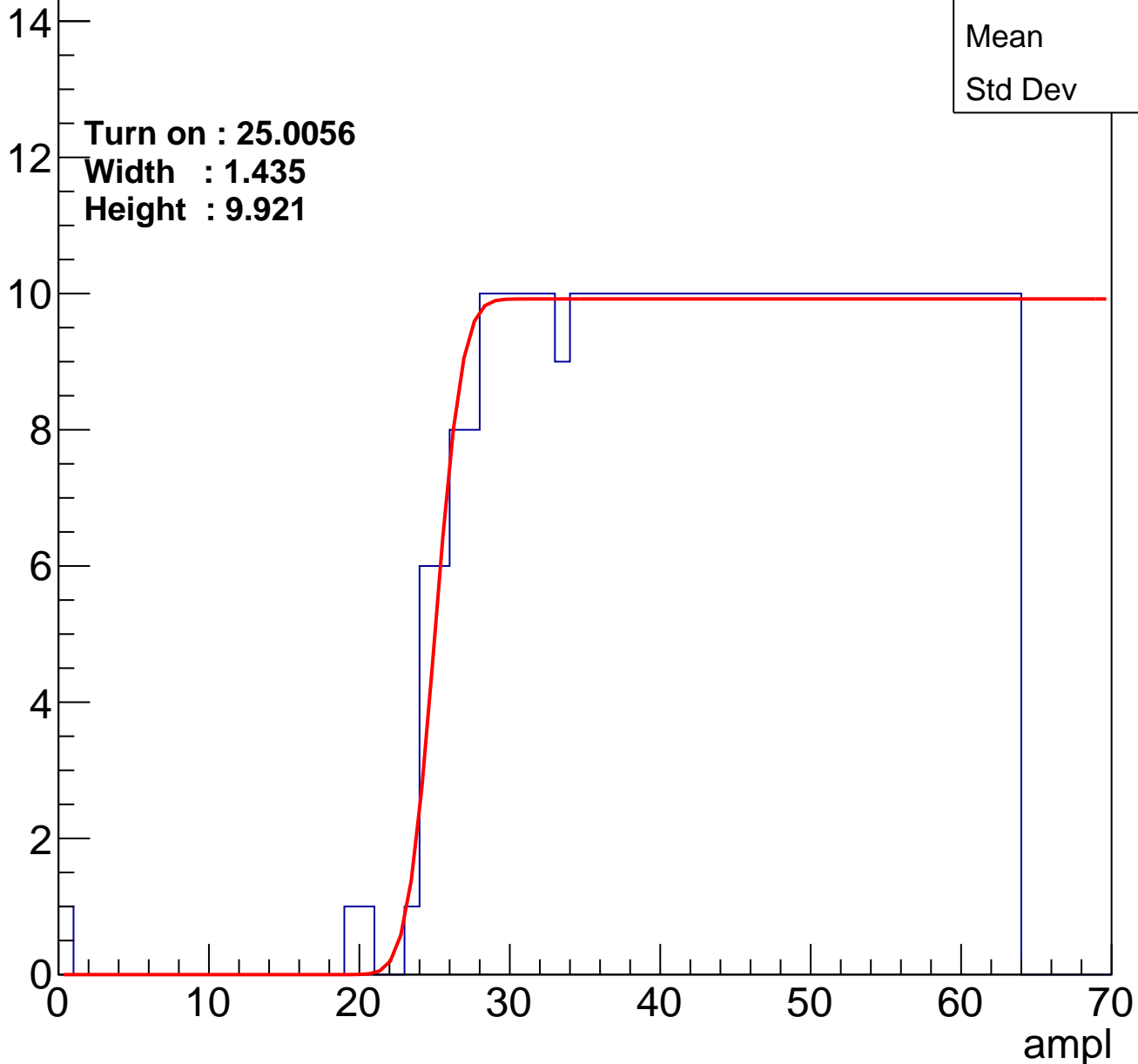
Entries	391
Mean	43.8
Std Dev	11.6

Turn on : 25.0056

Width : 1.435

Height : 9.921

Entry



# B1L101S, U9-ch97

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	376
Mean	44.55
Std Dev	11.19

Turn on : 26.8436

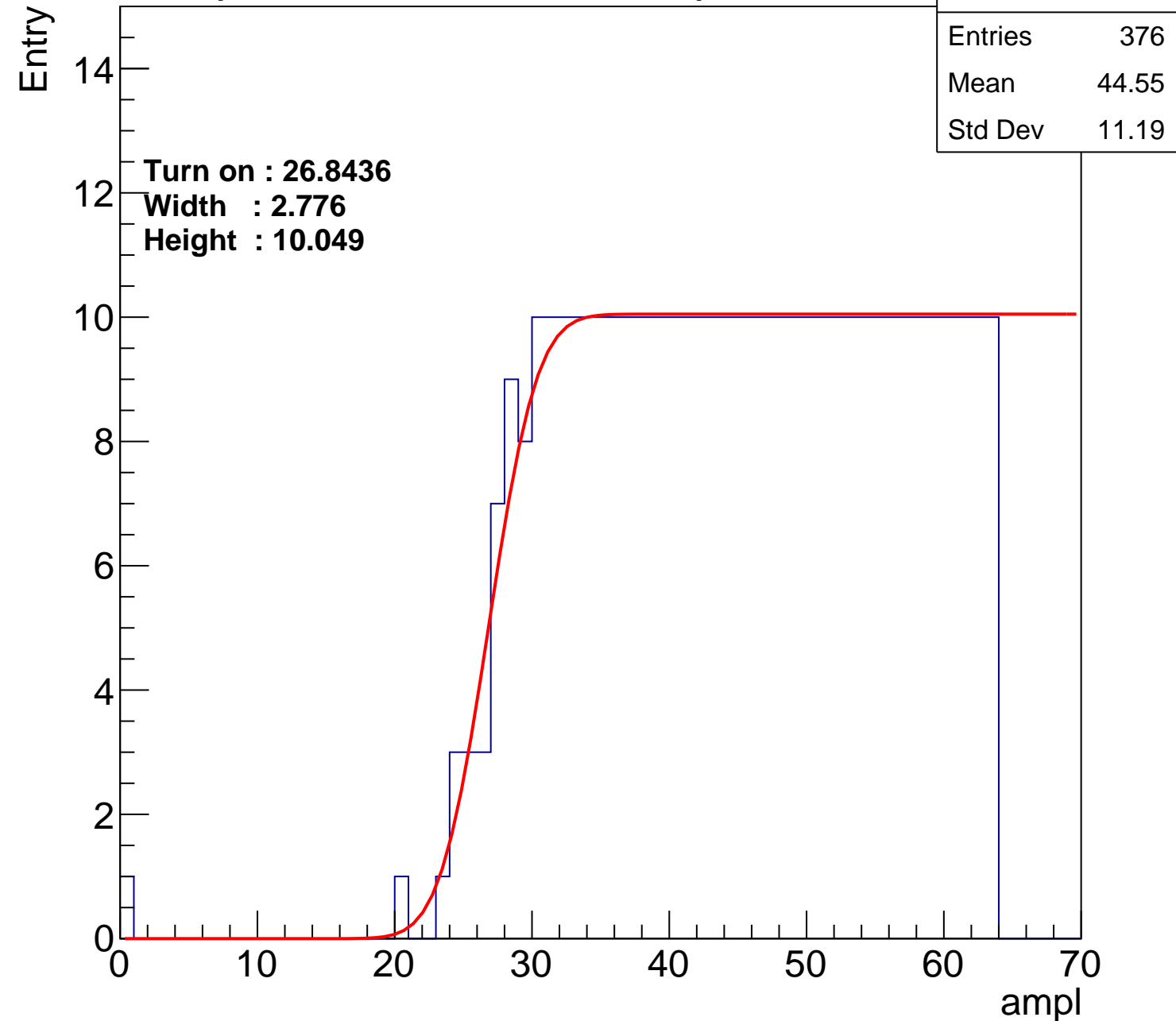
Width : 2.776

Height : 10.049

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch98

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	384
Mean	43.58
Std Dev	12.82

Turn on : 26.7478

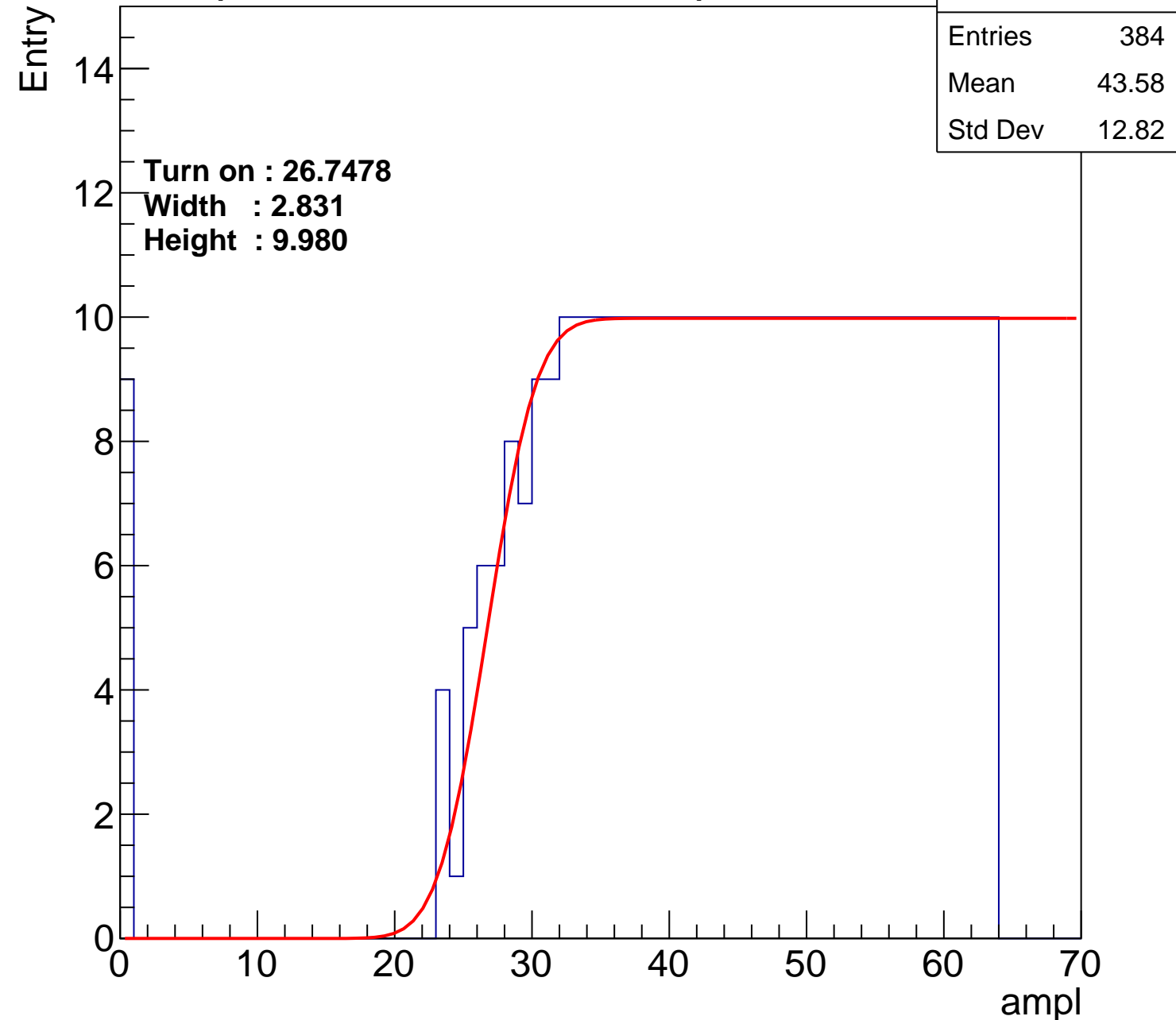
Width : 2.831

Height : 9.980

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch99

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	368
Mean	44.85
Std Dev	11.22

**Turn on : 28.0029**

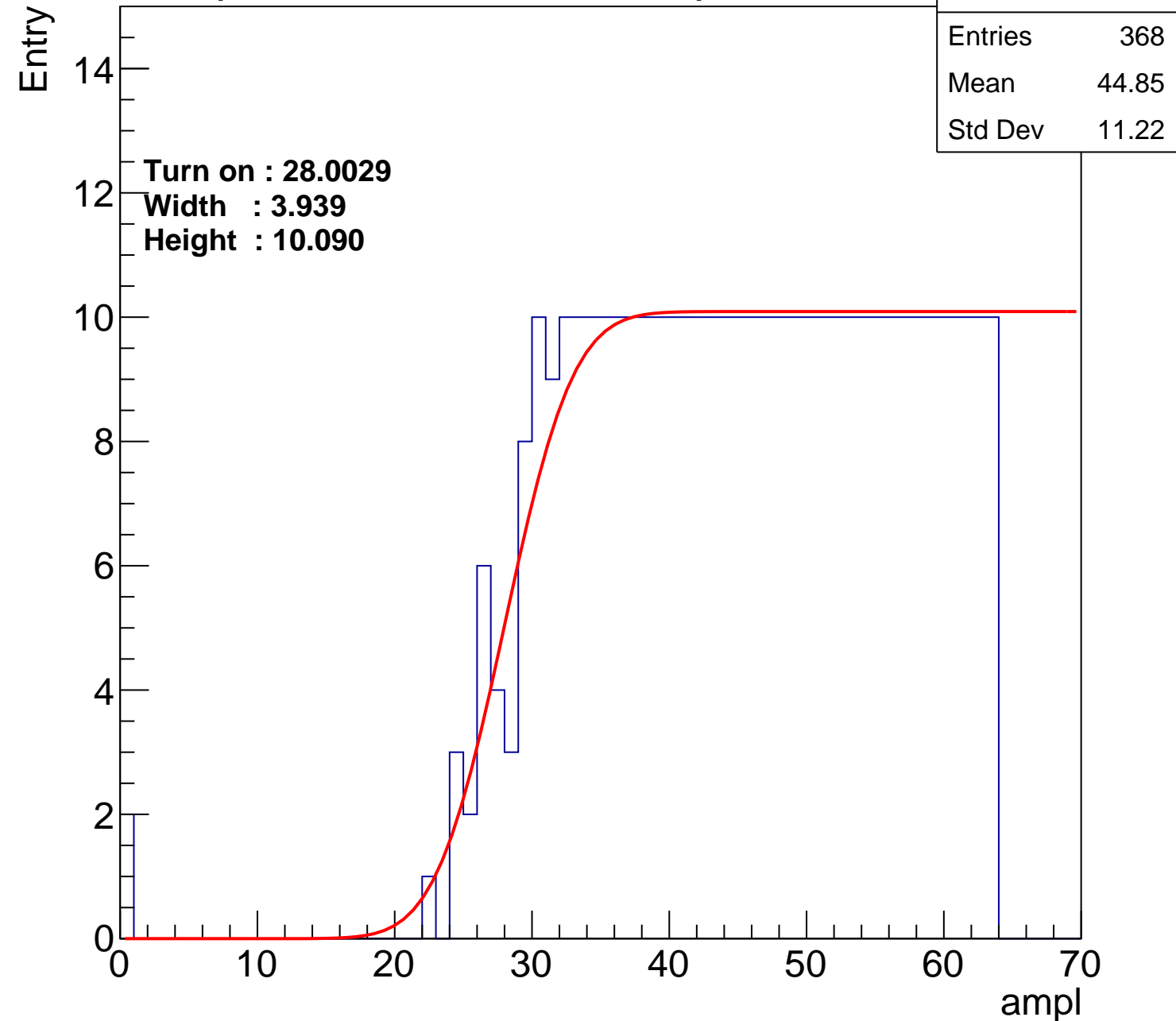
**Width : 3.939**

**Height : 10.090**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch100

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	397
Mean	43.3
Std Dev	12.27

Turn on : 25.0216

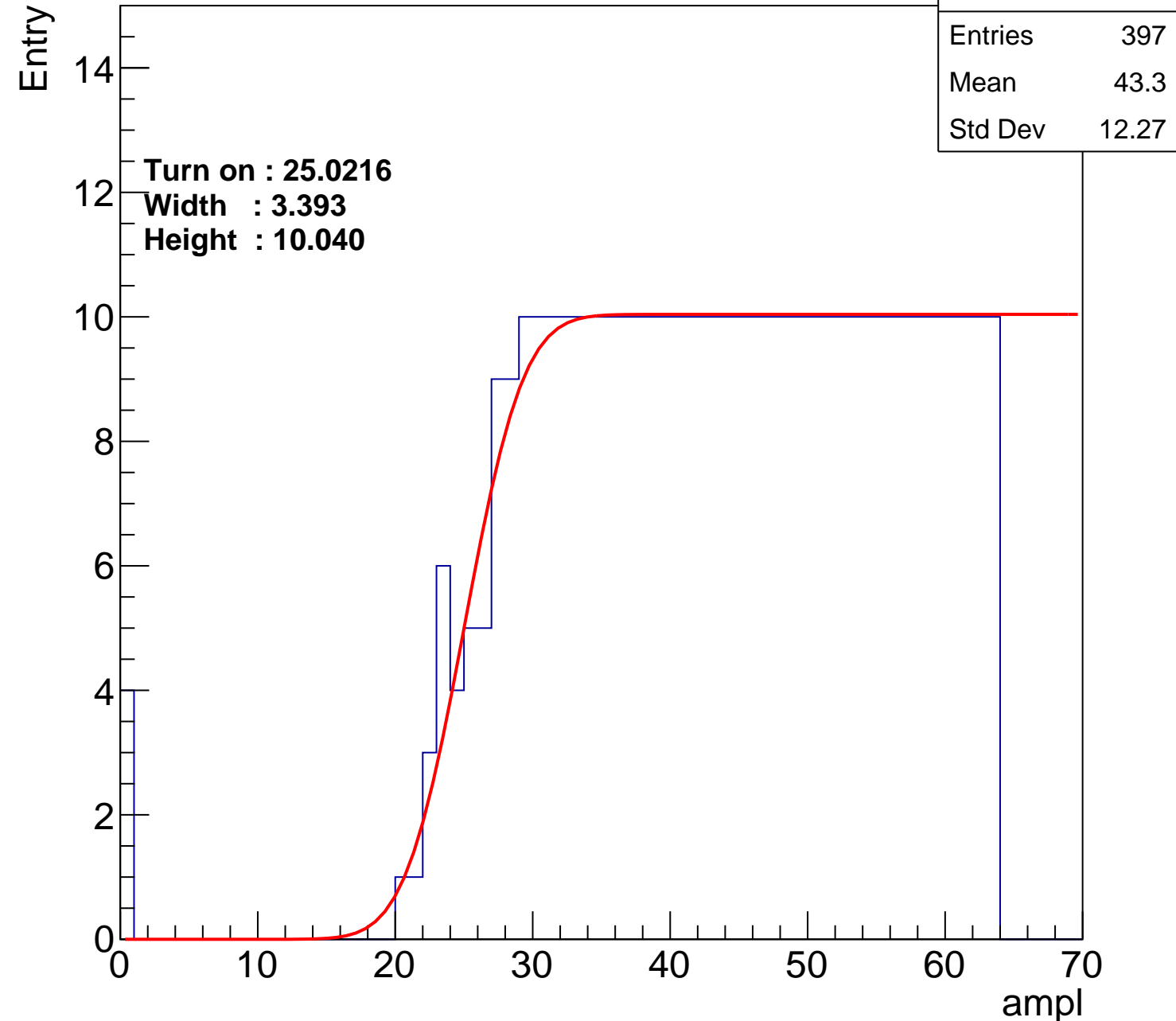
Width : 3.393

Height : 10.040

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch101

**calib\_packv5\_042523\_0143.root, FC#0, port D2**

Entries	380
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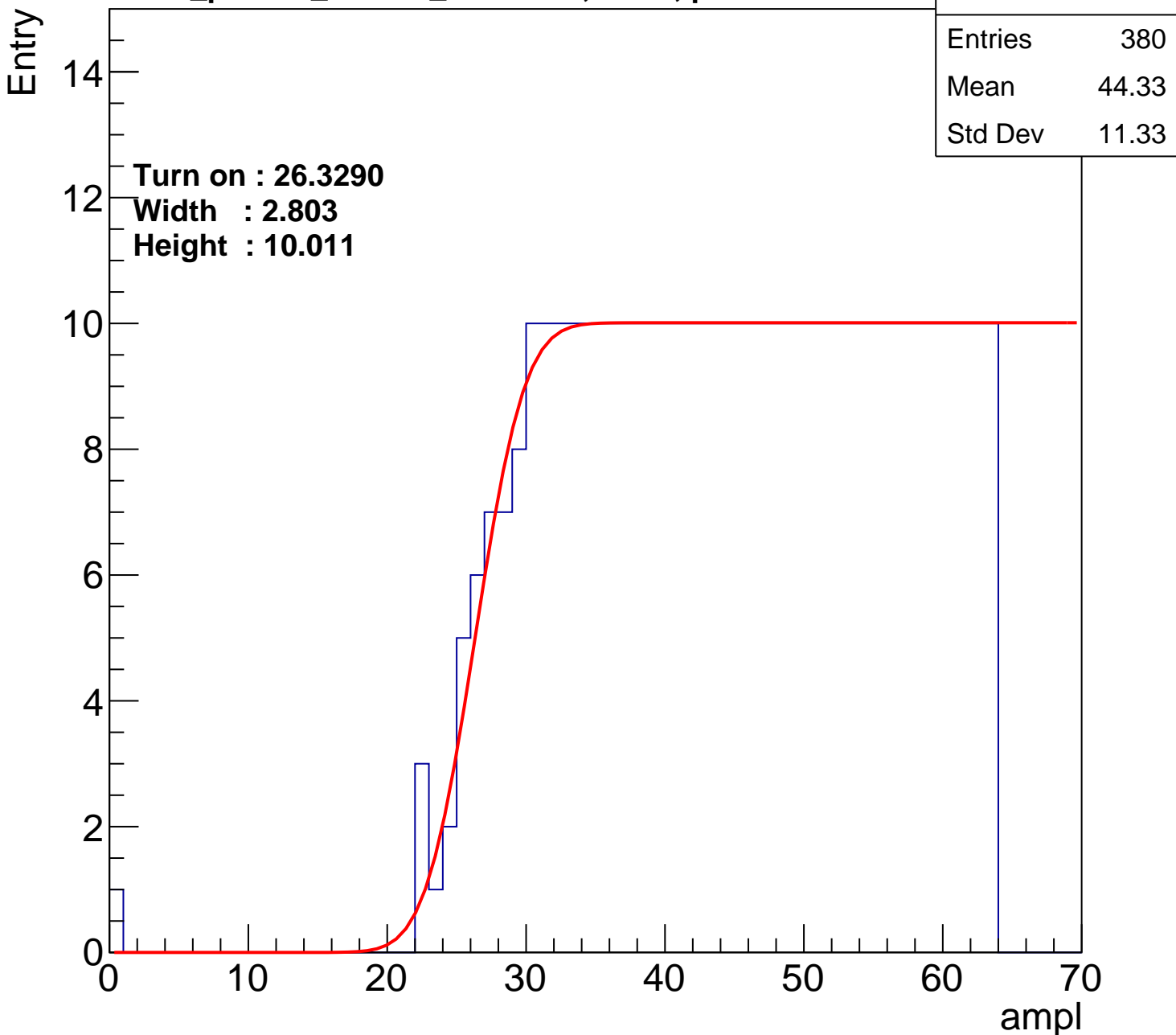
Mean	44.33
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Std Dev	11.33
---------	-------

**Turn on : 26.3290**

**Width : 2.803**

**Height : 10.011**



# B1L101S, U9-ch102

calib\_packv5\_042523\_0143.root, FC#0, port D2

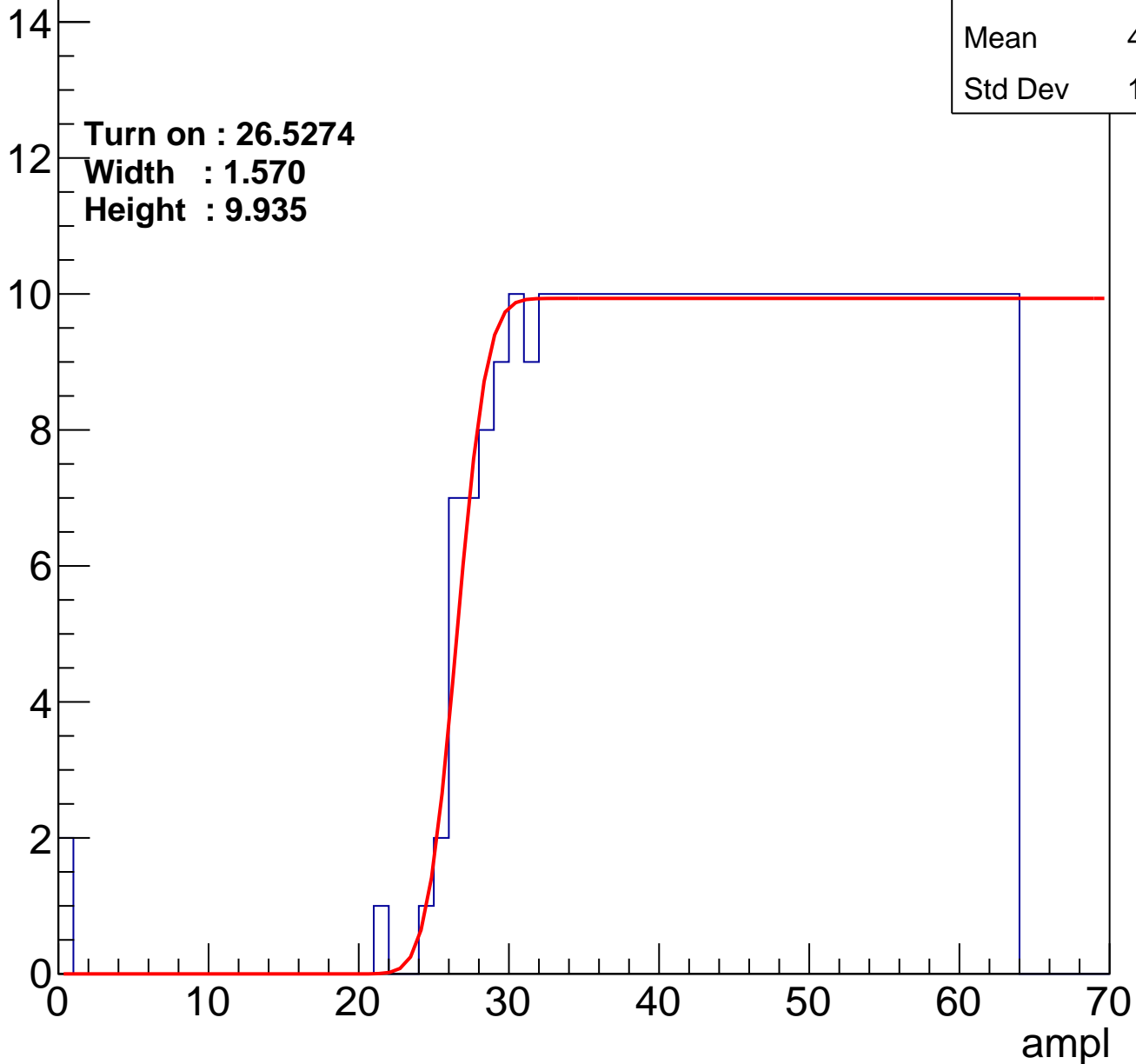
Entry

Entries	376
Mean	44.49
Std Dev	11.35

Turn on : 26.5274

Width : 1.570

Height : 9.935





# B1L101S, U9-ch103

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	359
Mean	45.4
Std Dev	10.72

Turn on : 28.1355

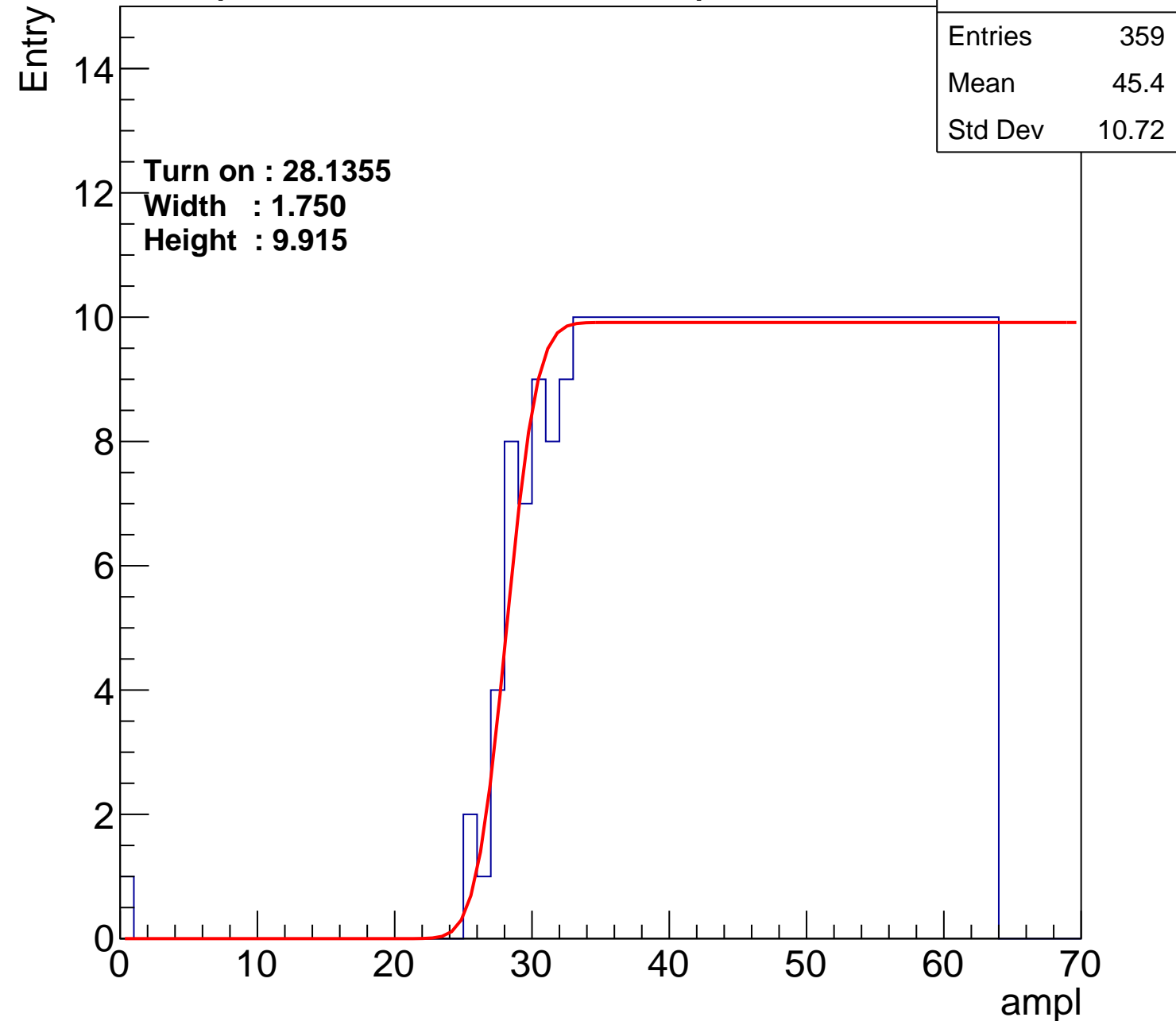
Width : 1.750

Height : 9.915

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch104

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	375
Mean	44.32
Std Dev	11.84

Turn on : 27.2852

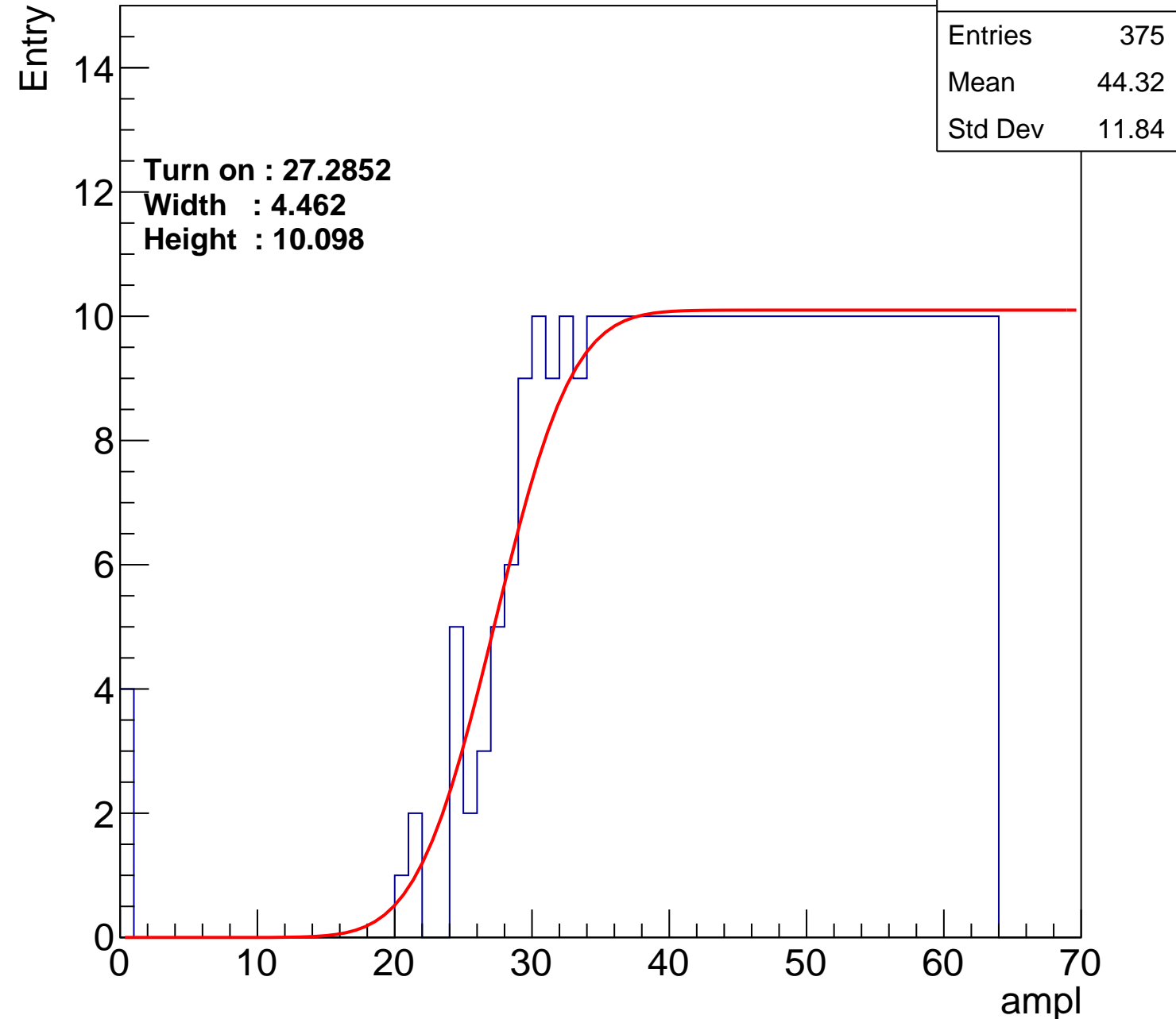
Width : 4.462

Height : 10.098

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch105

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	394
Mean	43.43
Std Dev	12.23

Turn on : 25.4643

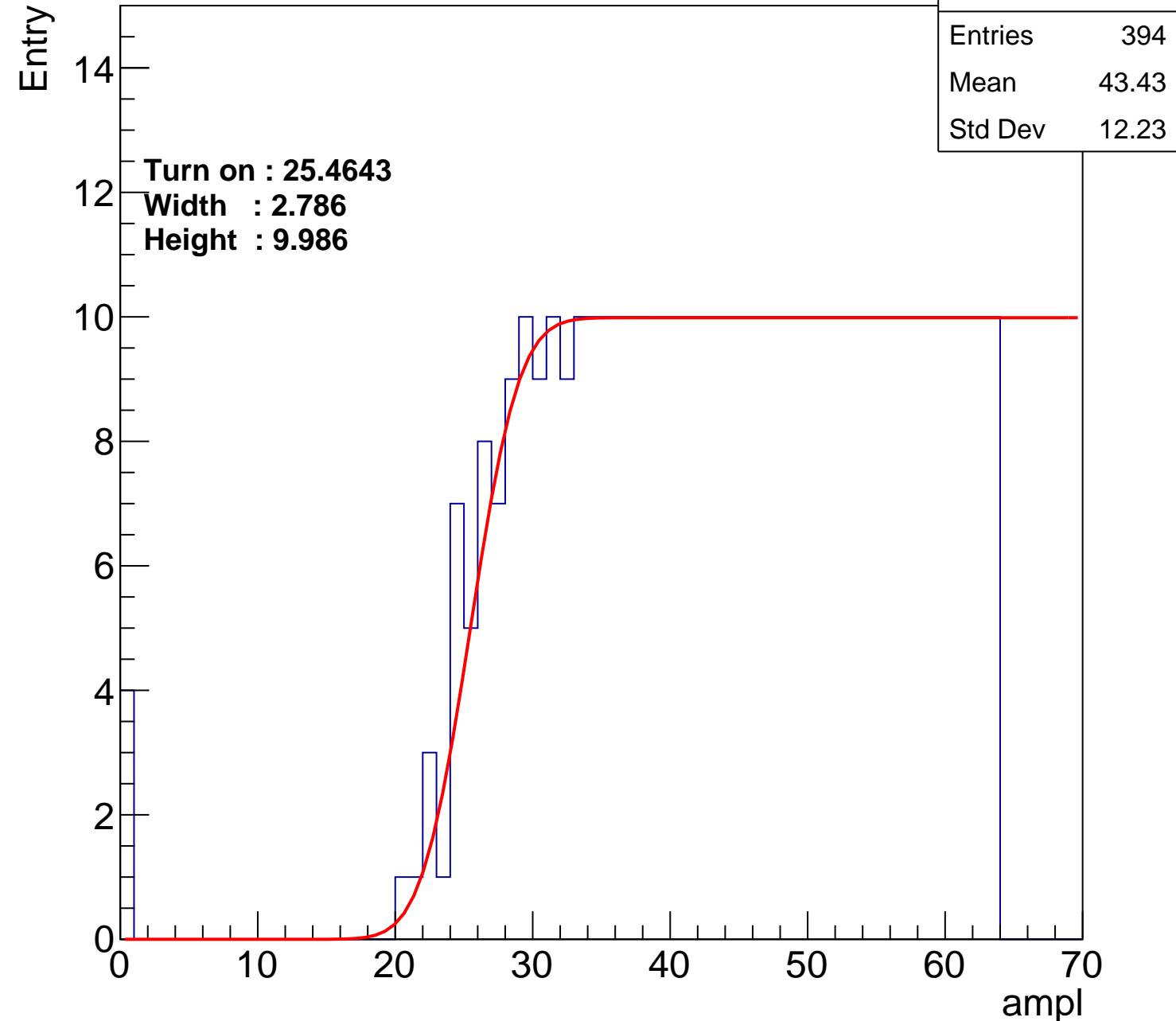
Width : 2.786

Height : 9.986

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch106

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	394
Mean	43.56
Std Dev	11.91

Turn on : 24.9460

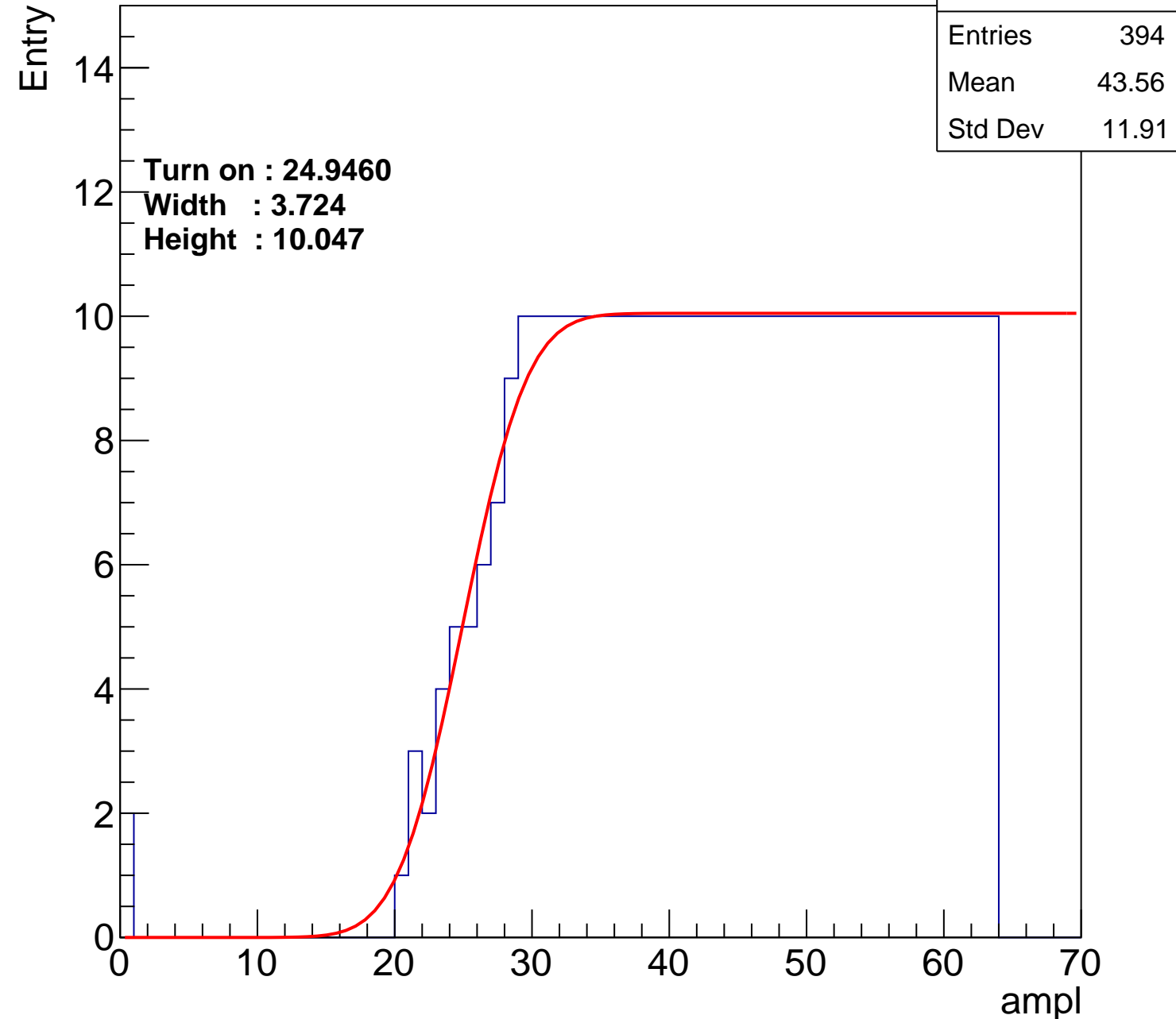
Width : 3.724

Height : 10.047

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch107

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	367
Mean	44.73
Std Dev	11.62

Turn on : 27.9752

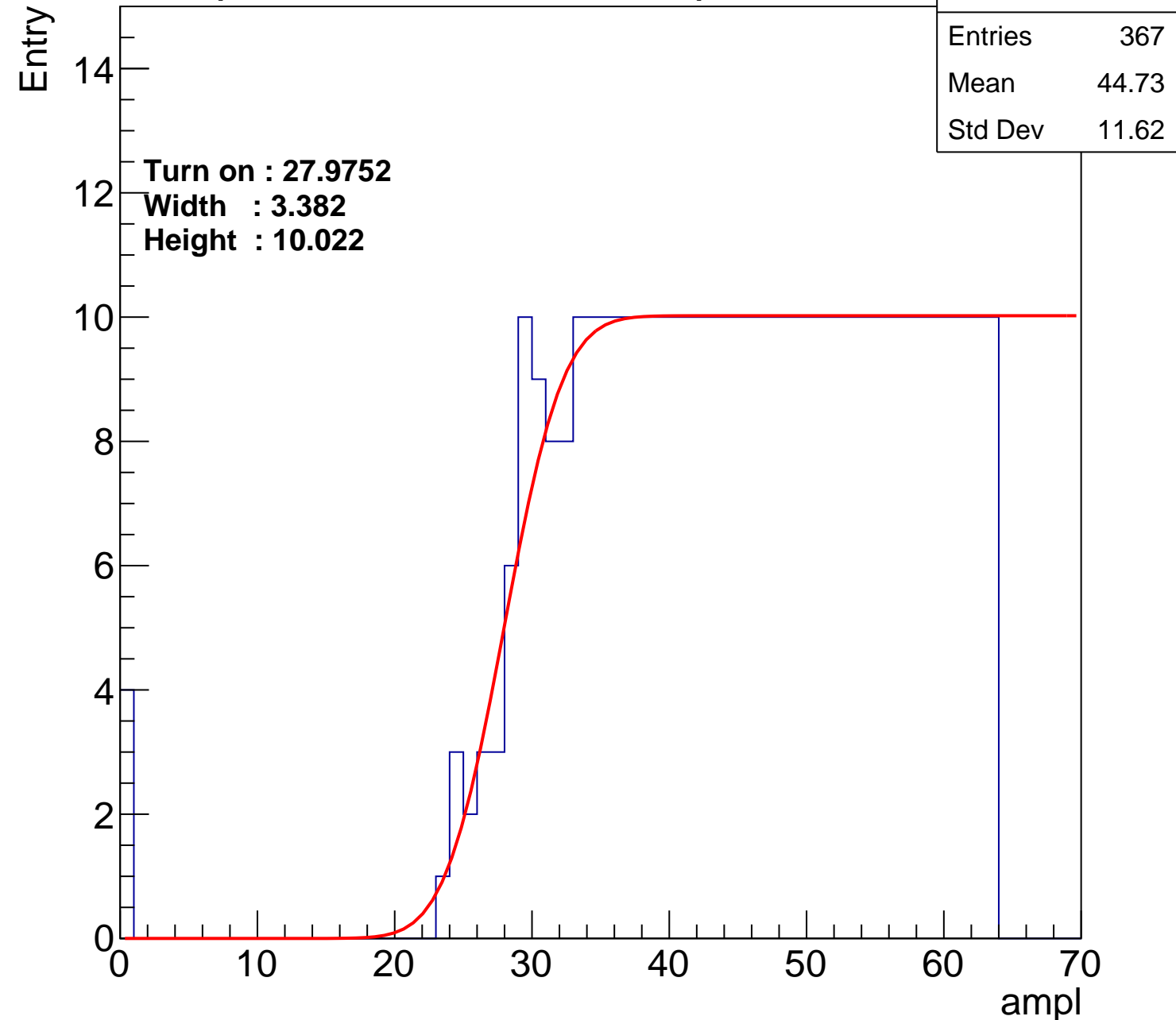
Width : 3.382

Height : 10.022

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch108

calib\_packv5\_042523\_0143.root, FC#0, port D2

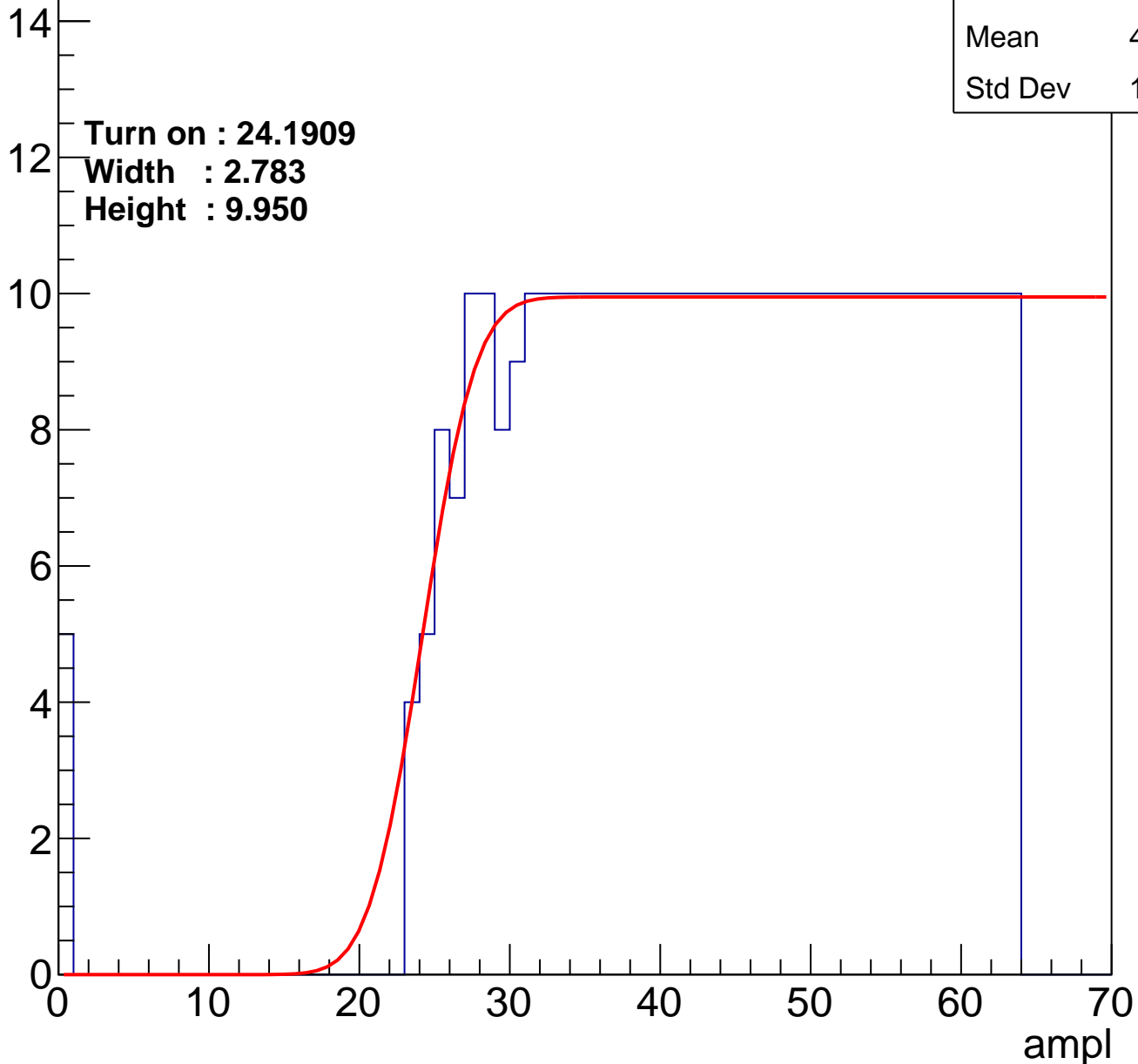
Entries	396
Mean	43.32
Std Dev	12.34

**Turn on : 24.1909**

**Width : 2.783**

**Height : 9.950**

Entry



# B1L101S, U9-ch109

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	353
Mean	45.61
Std Dev	10.79

Turn on : 29.1311

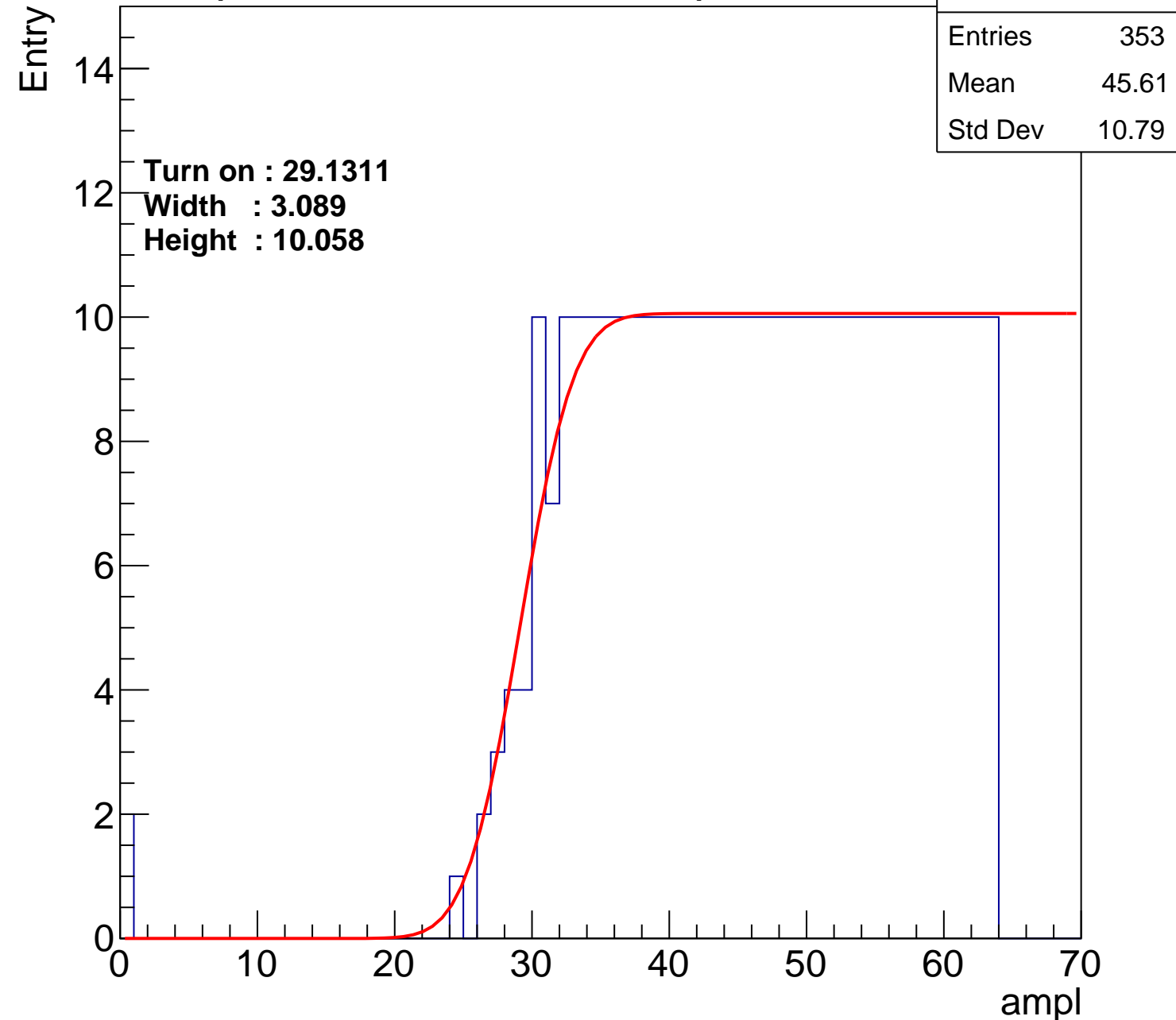
Width : 3.089

Height : 10.058

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch110

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	368
Mean	44.71
Std Dev	11.59

Turn on : 28.0114

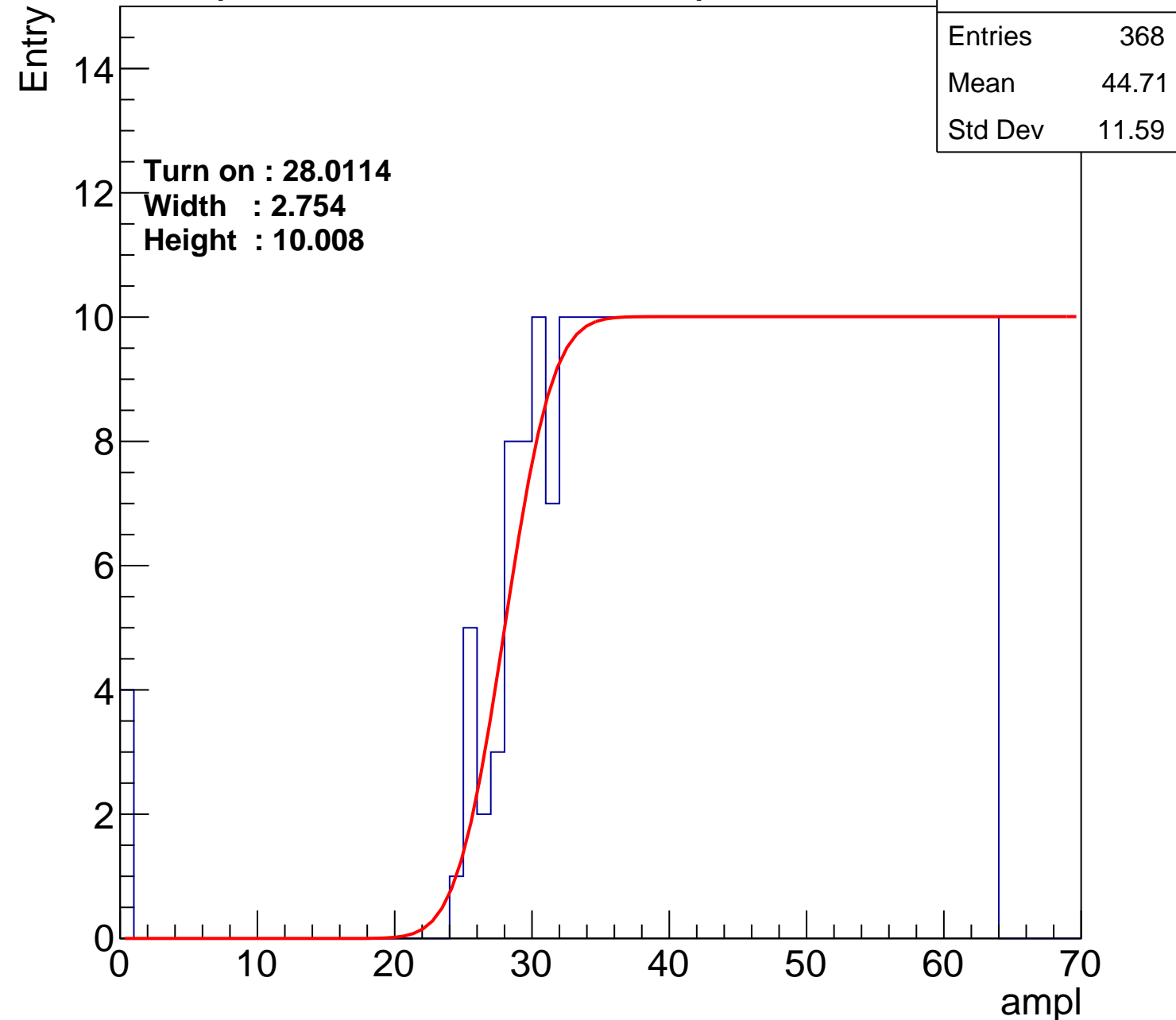
Width : 2.754

Height : 10.008

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L101S, U9-ch111

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	371
Mean	44.77
Std Dev	11.1

Turn on : 27.0121

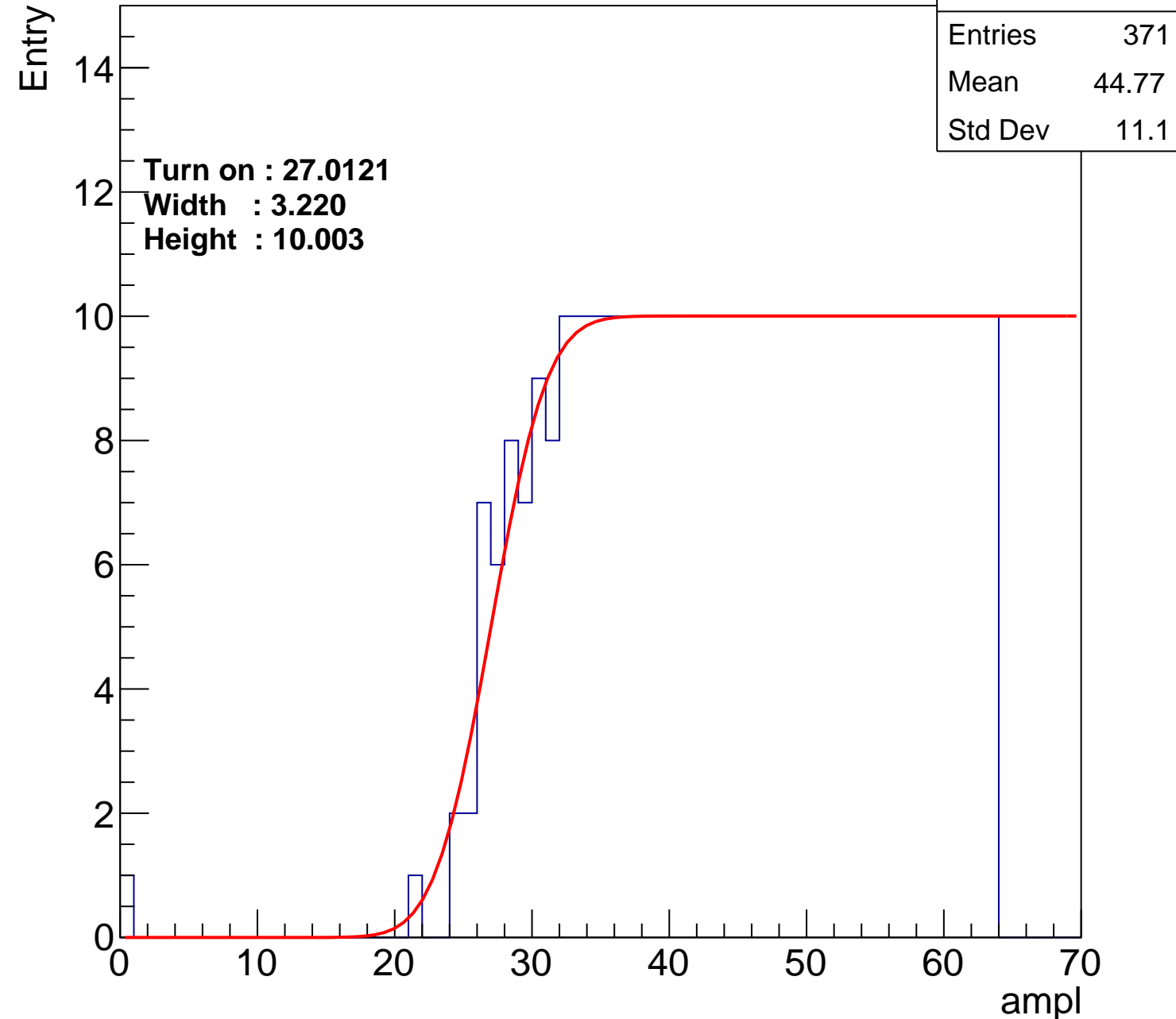
Width : 3.220

Height : 10.003

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch112

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	377
Mean	44.29
Std Dev	11.78

Turn on : 26.9736

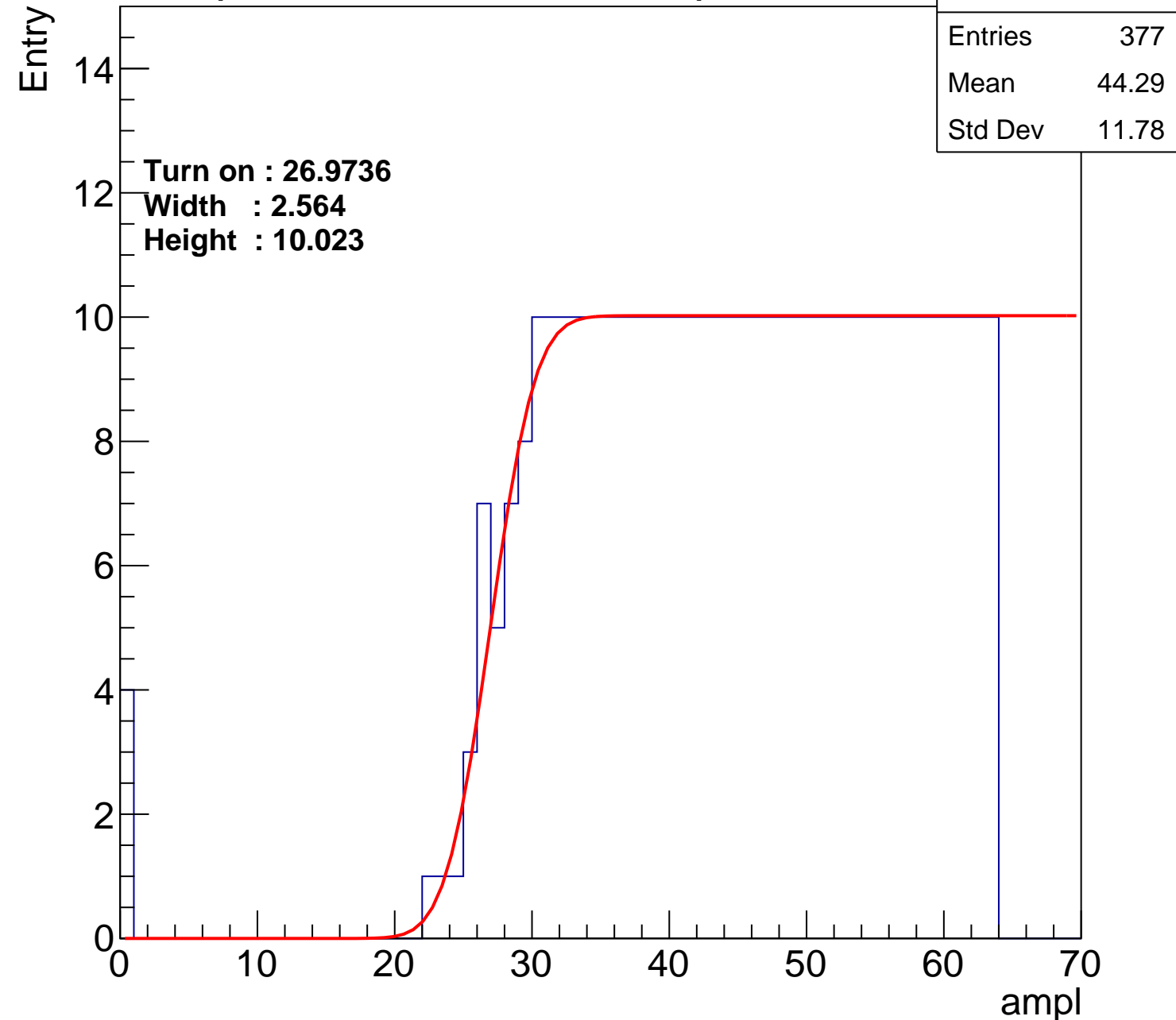
Width : 2.564

Height : 10.023

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch113

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	366
Mean	44.89
Std Dev	11.35

Turn on : 28.0117

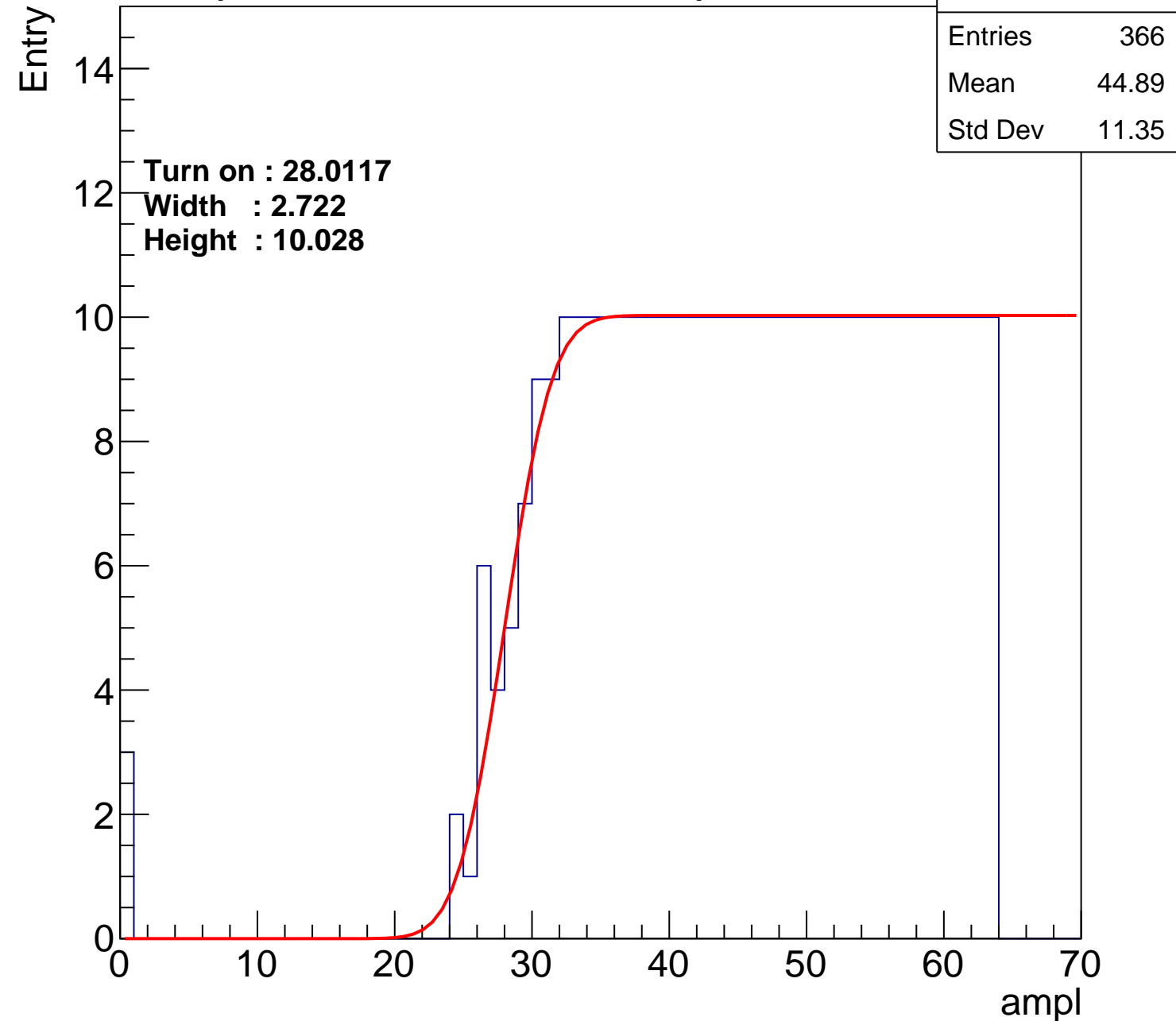
Width : 2.722

Height : 10.028

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch114

calib\_packv5\_042523\_0143.root, FC#0, port D2

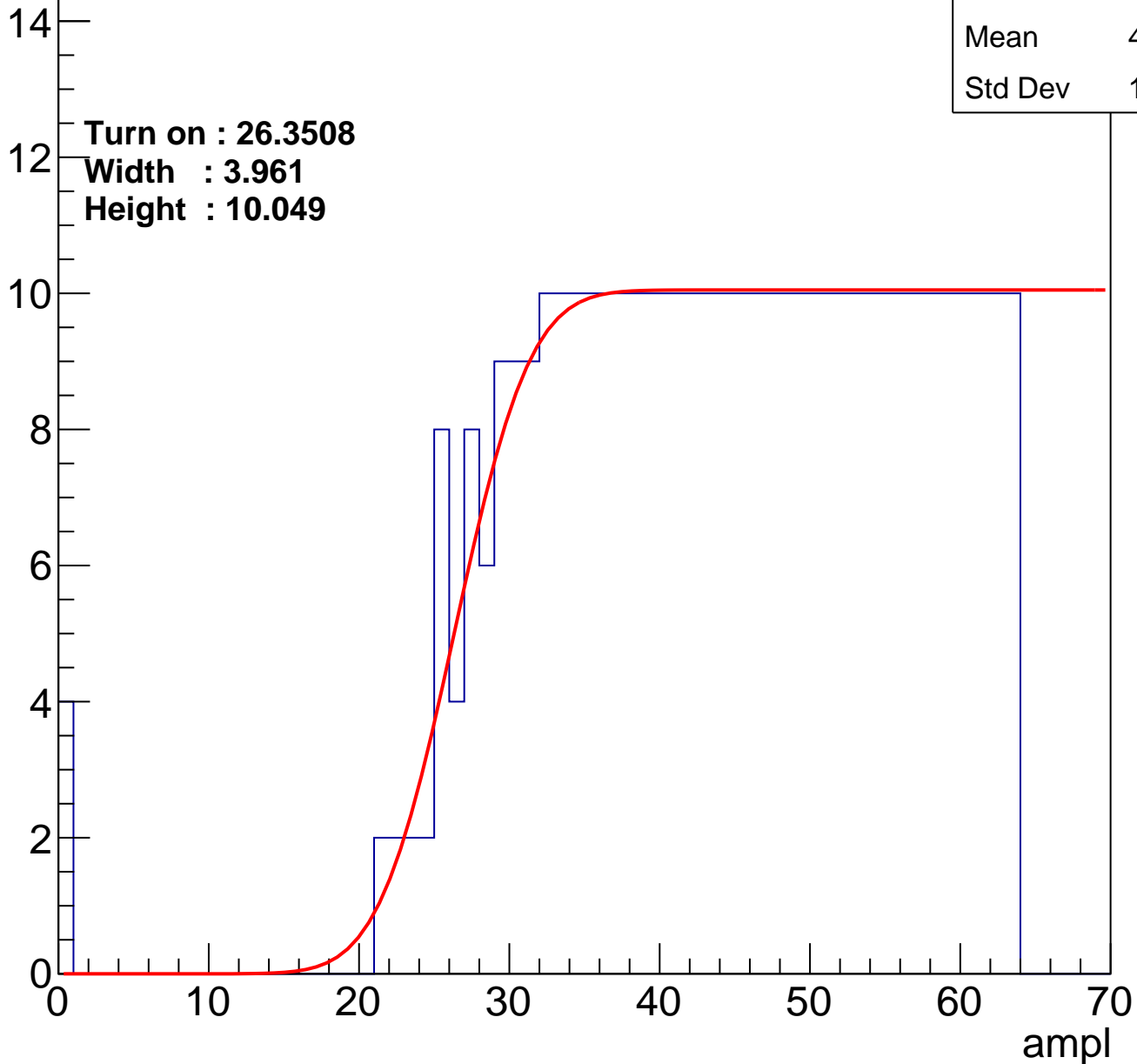
Entries	385
Mean	43.84
Std Dev	12.06

Turn on : 26.3508

Width : 3.961

Height : 10.049

Entry



# B1L101S, U9-ch115

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	373
Mean	44.56
Std Dev	11.42

Turn on : 27.2985

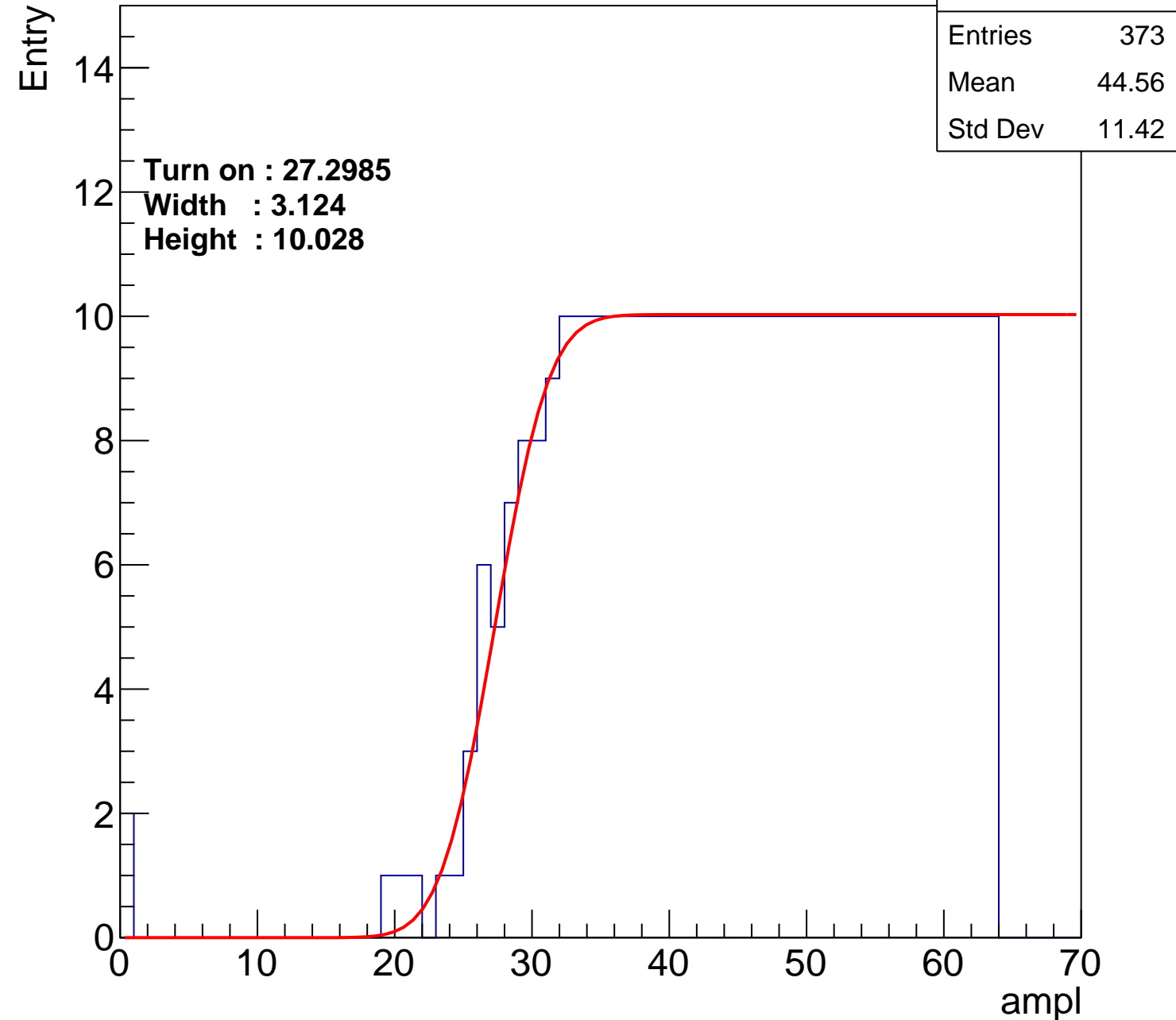
Width : 3.124

Height : 10.028

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch116

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	373
Mean	44.62
Std Dev	11.24

Turn on : 27.4296

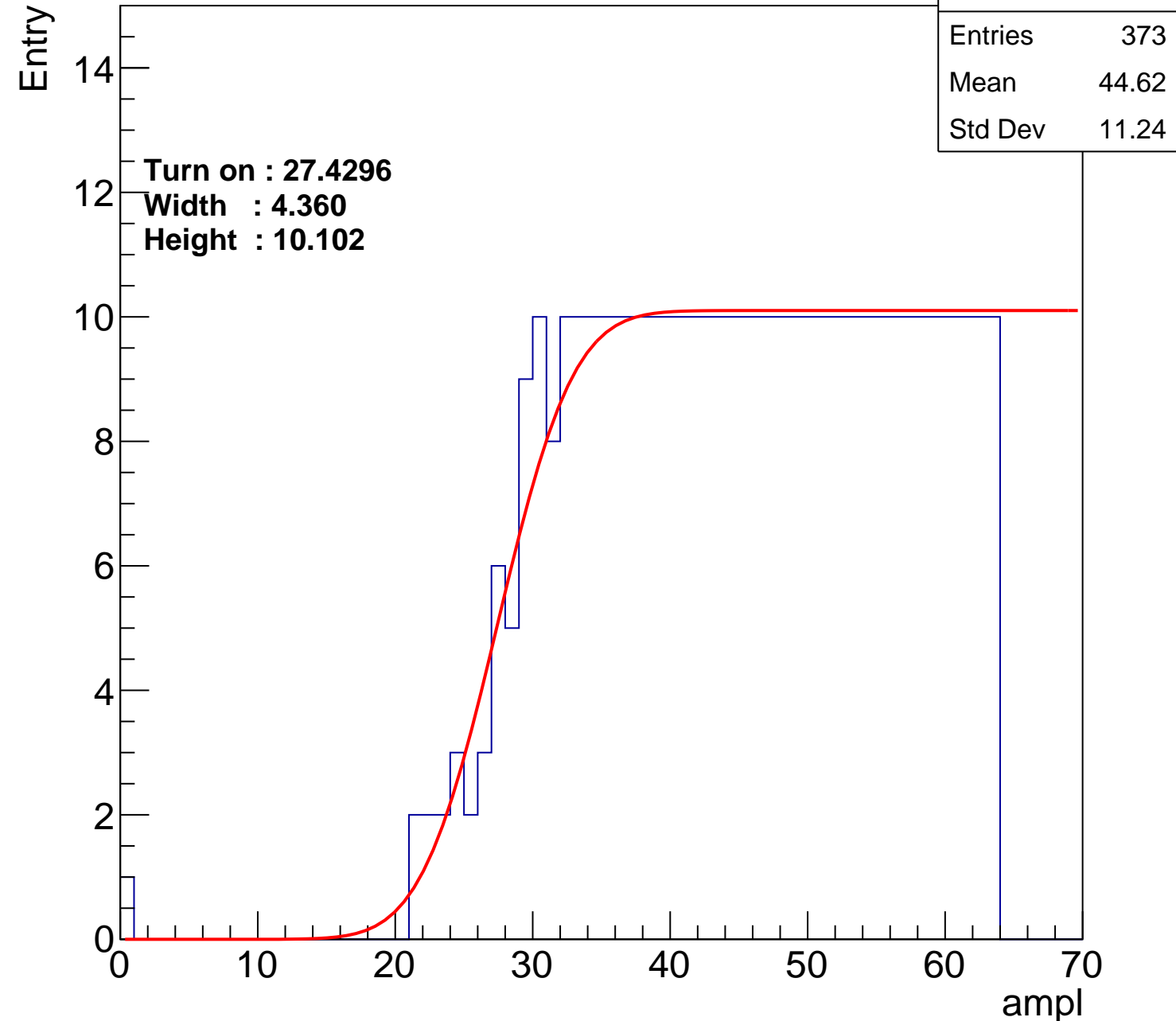
Width : 4.360

Height : 10.102

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch117

calib\_packv5\_042523\_0143.root, FC#0, port D2

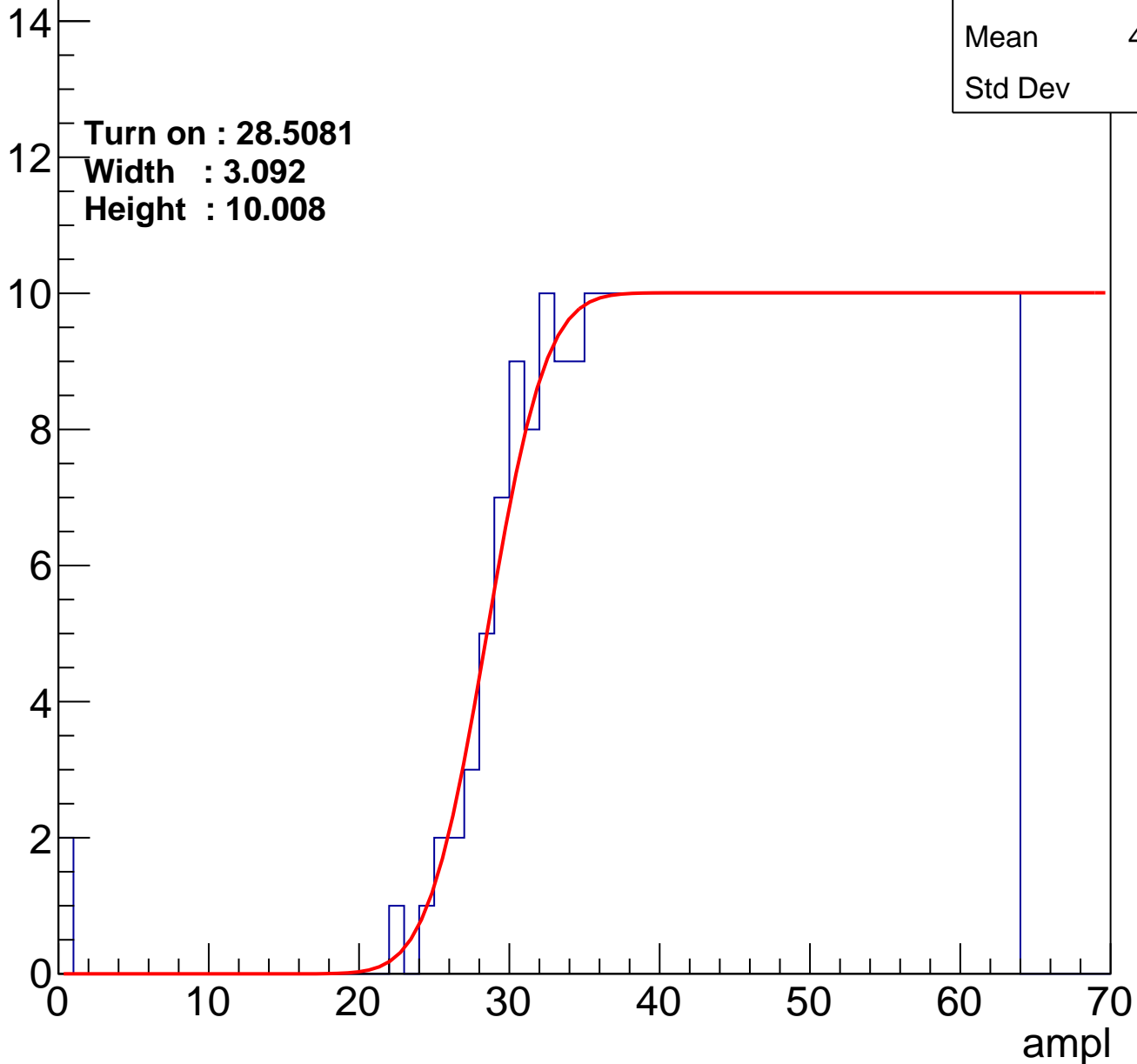
Entries	358
Mean	45.32
Std Dev	11

Turn on : 28.5081

Width : 3.092

Height : 10.008

Entry



# B1L101S, U9-ch118

calib\_packv5\_042523\_0143.root, FC#0, port D2

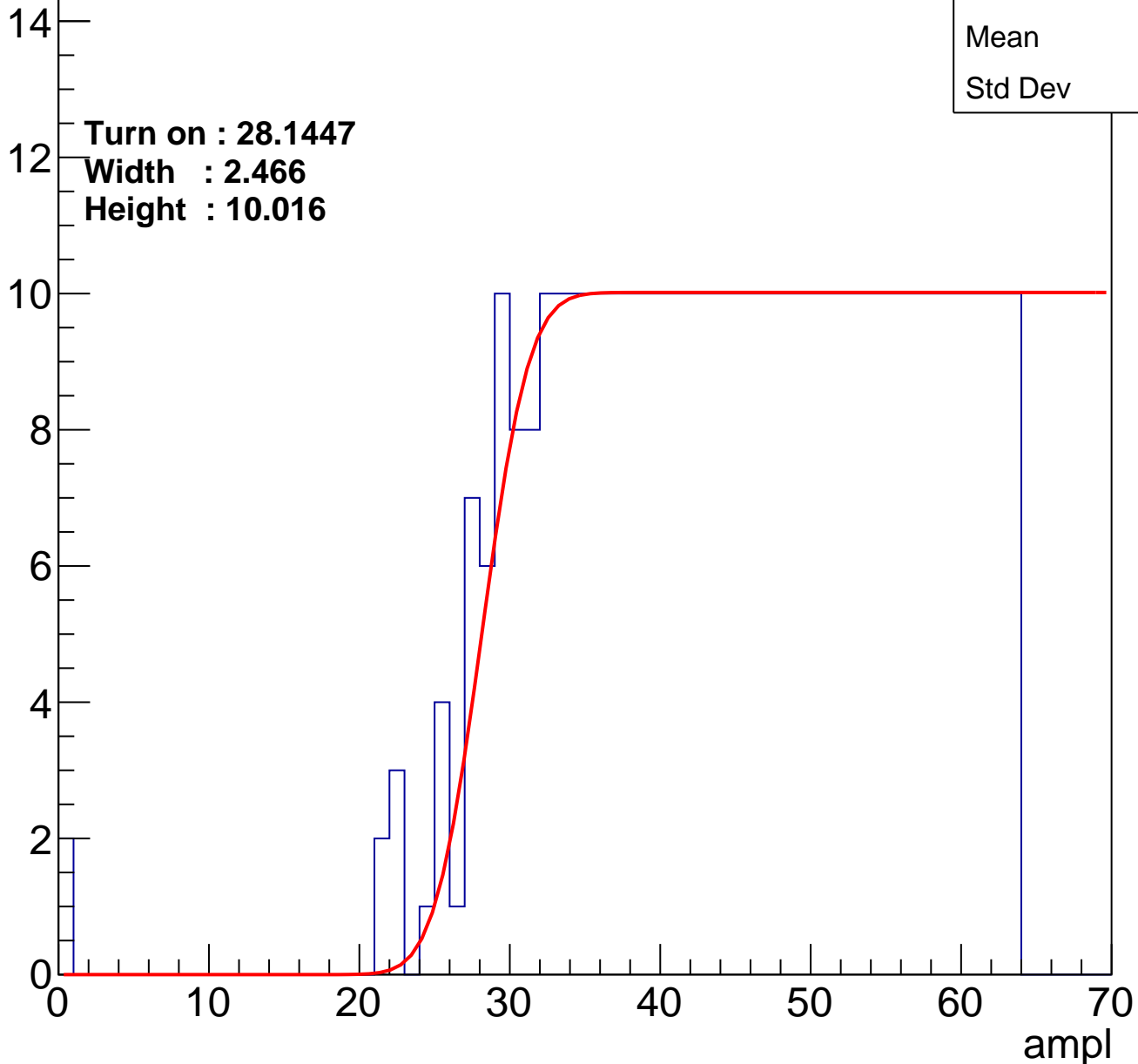
Entries	372
Mean	44.6
Std Dev	11.4

**Turn on : 28.1447**

**Width : 2.466**

**Height : 10.016**

Entry





# B1L101S, U9-ch119

calib\_packv5\_042523\_0143.root, FC#0, port D2

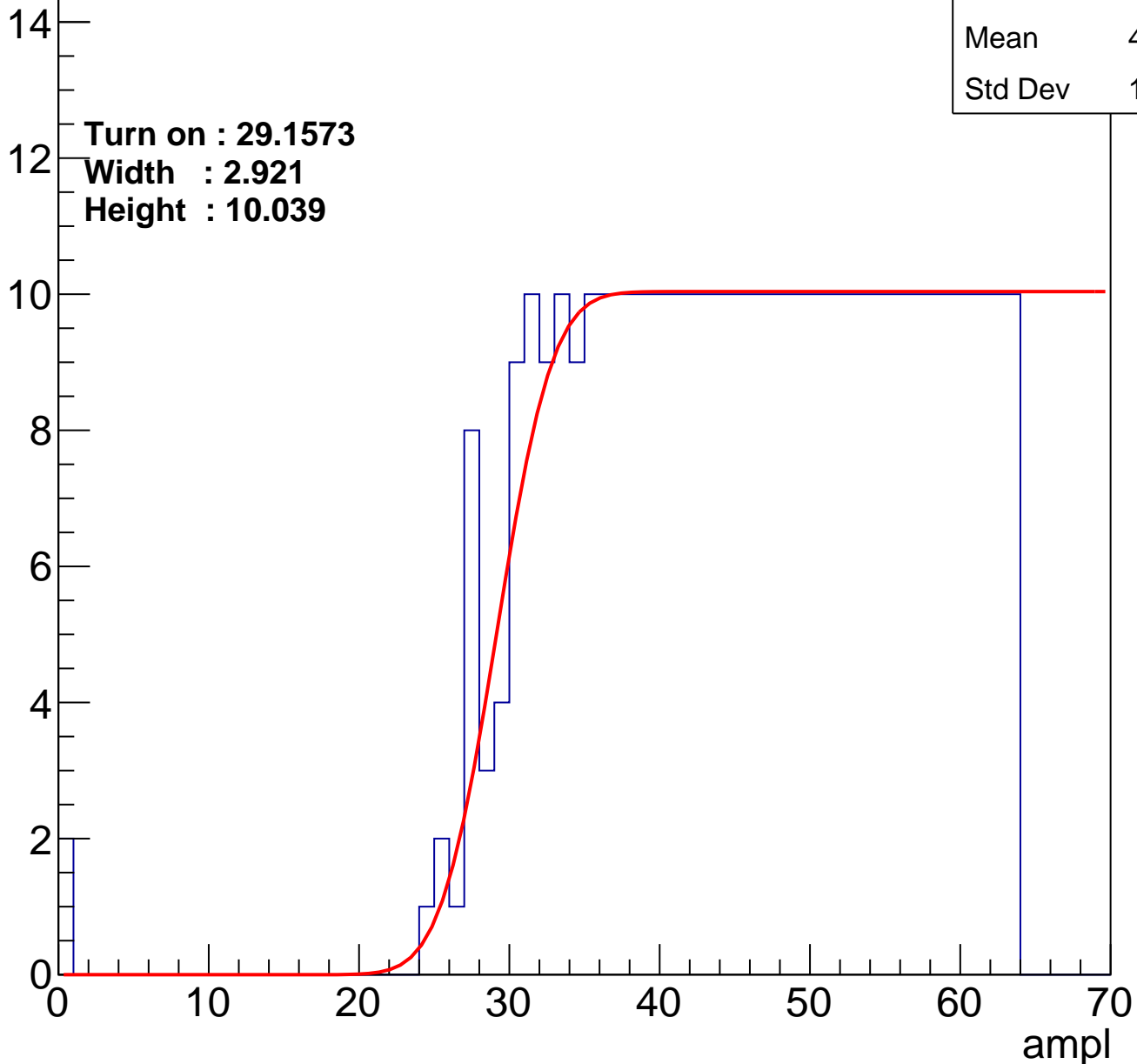
Entry

Entries	358
Mean	45.34
Std Dev	10.97

Turn on : 29.1573

Width : 2.921

Height : 10.039



# B1L101S, U9-ch120

calib\_packv5\_042523\_0143.root, FC#0, port D2

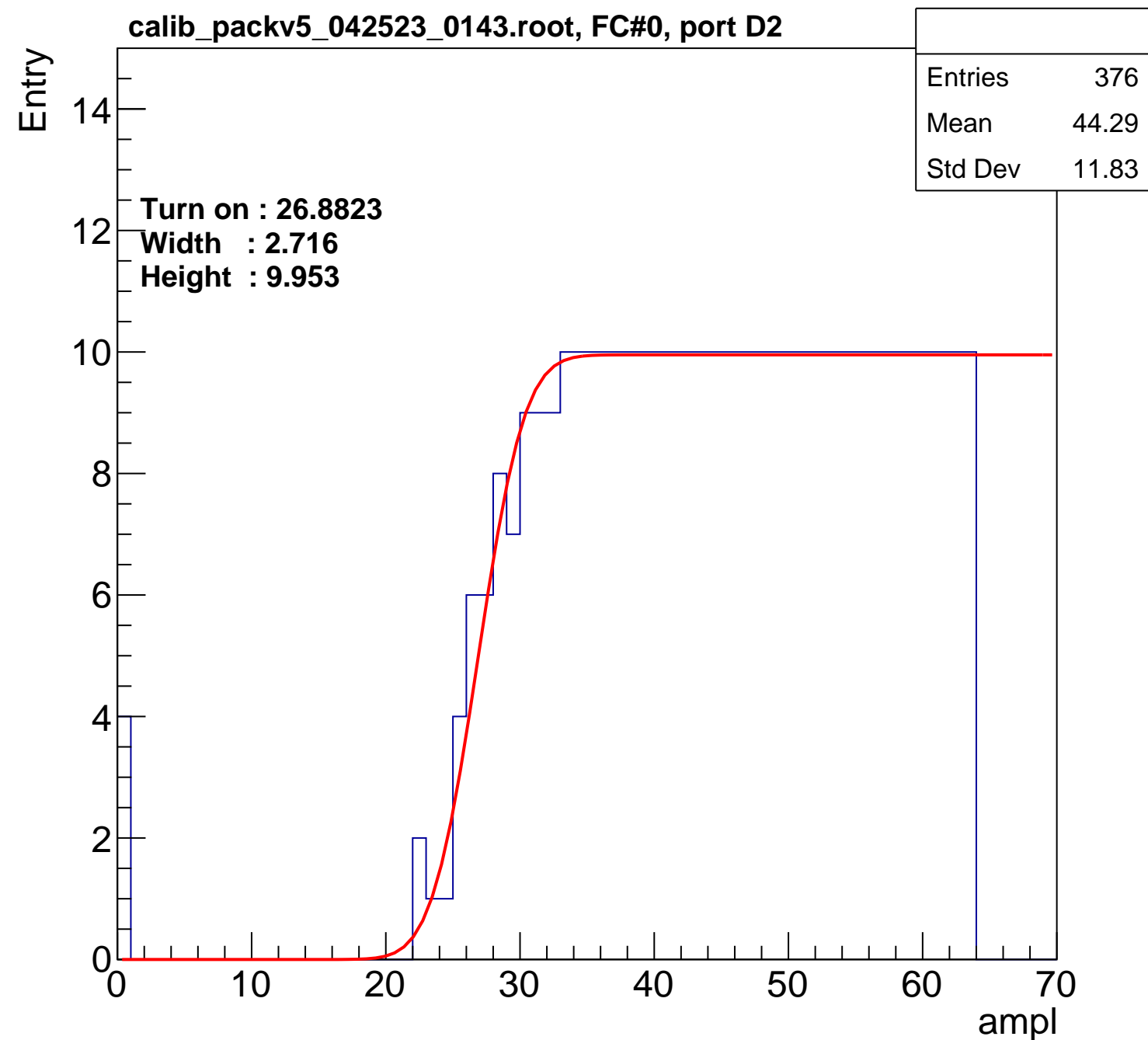
Entry

14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 26.8823**  
**Width : 2.716**  
**Height : 9.953**

Entries	376
Mean	44.29
Std Dev	11.83

ampl



# B1L101S, U9-ch121

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	383
Mean	44.19
Std Dev	11.4

Turn on : 26.5177

Width : 2.730

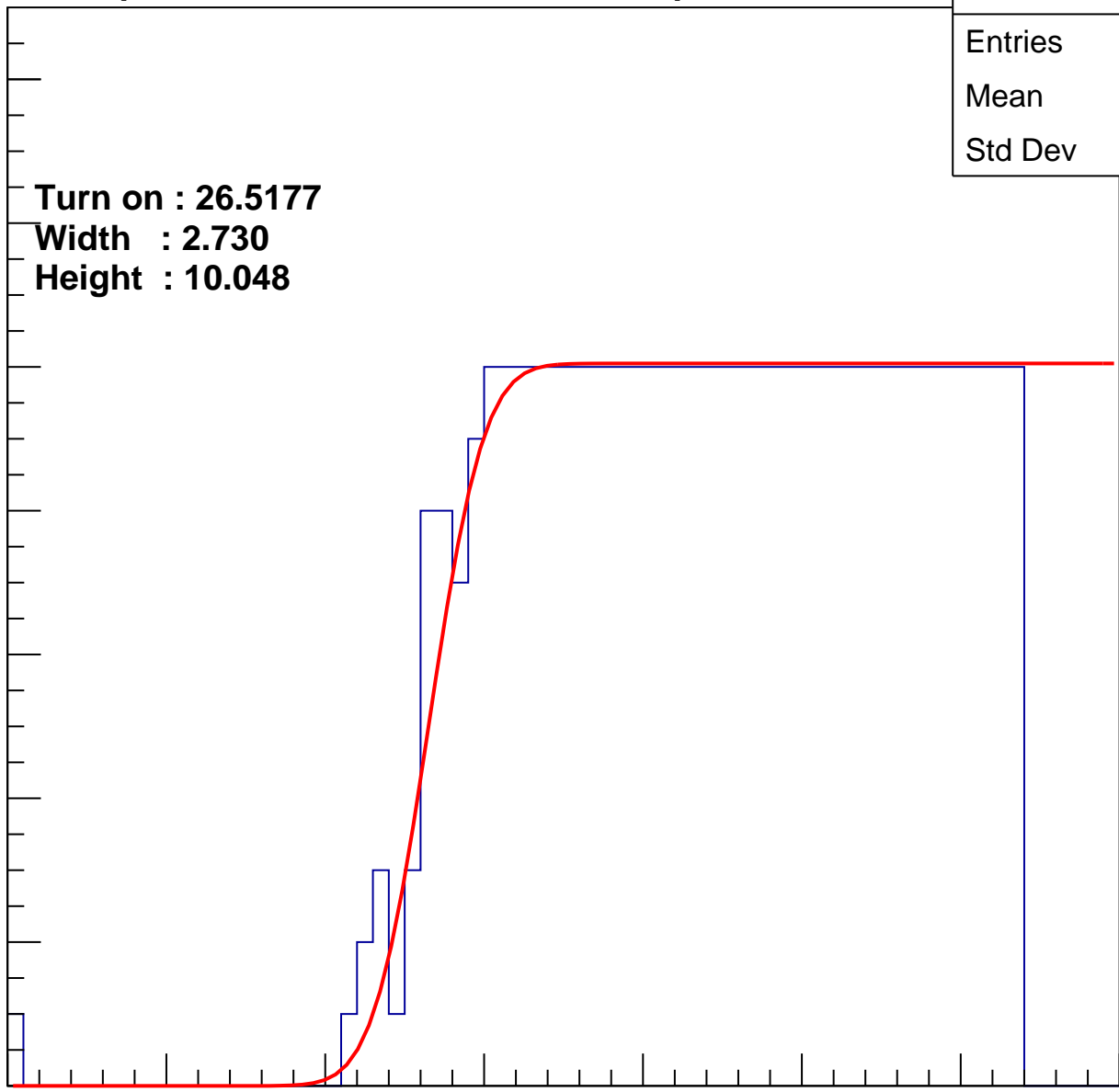
Height : 10.048

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U9-ch122

calib\_packv5\_042523\_0143.root, FC#0, port D2

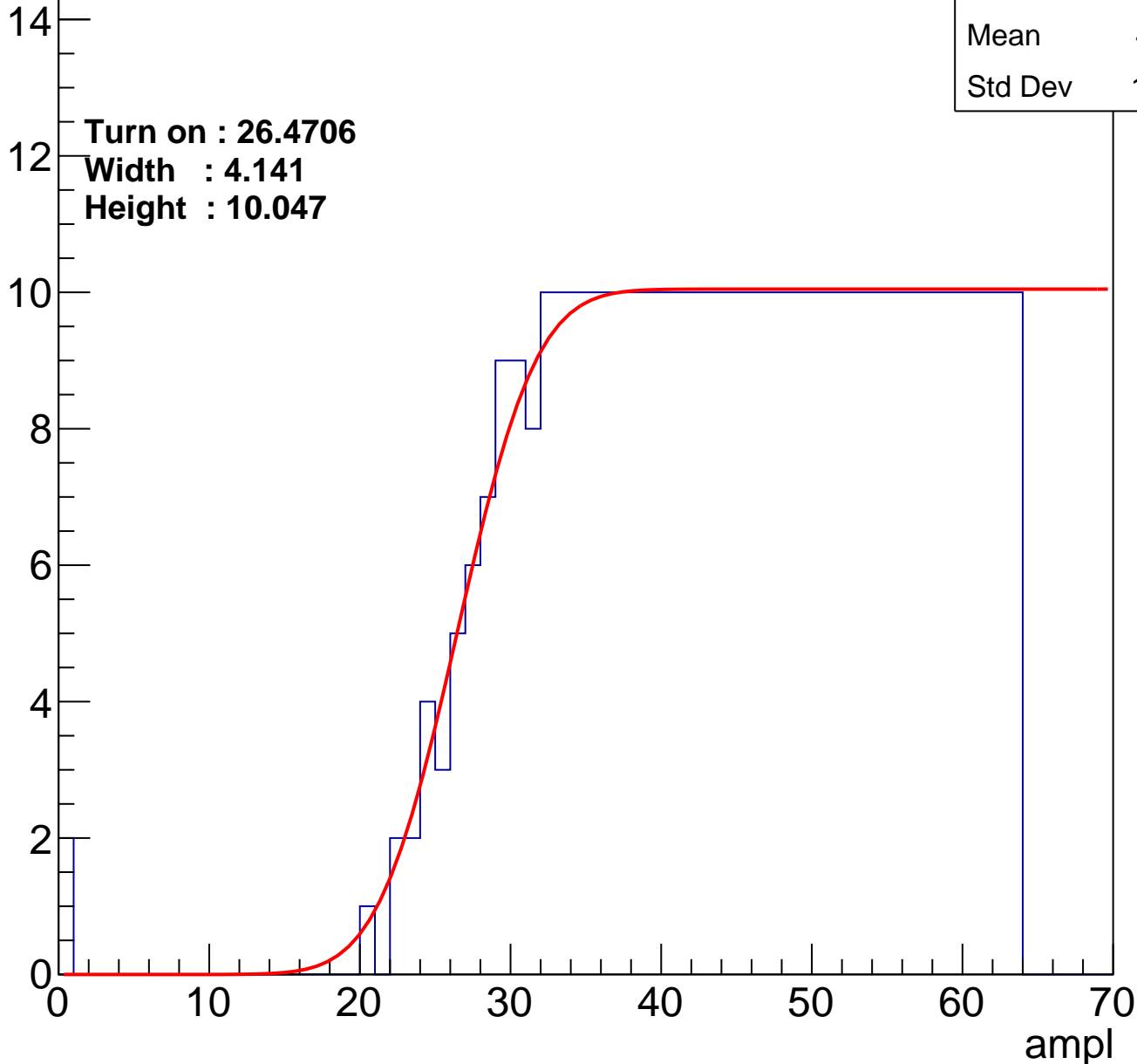
Entries	378
Mean	44.31
Std Dev	11.55

Turn on : 26.4706

Width : 4.141

Height : 10.047

Entry



# B1L101S, U9-ch123

calib\_packv5\_042523\_0143.root, FC#0, port D2

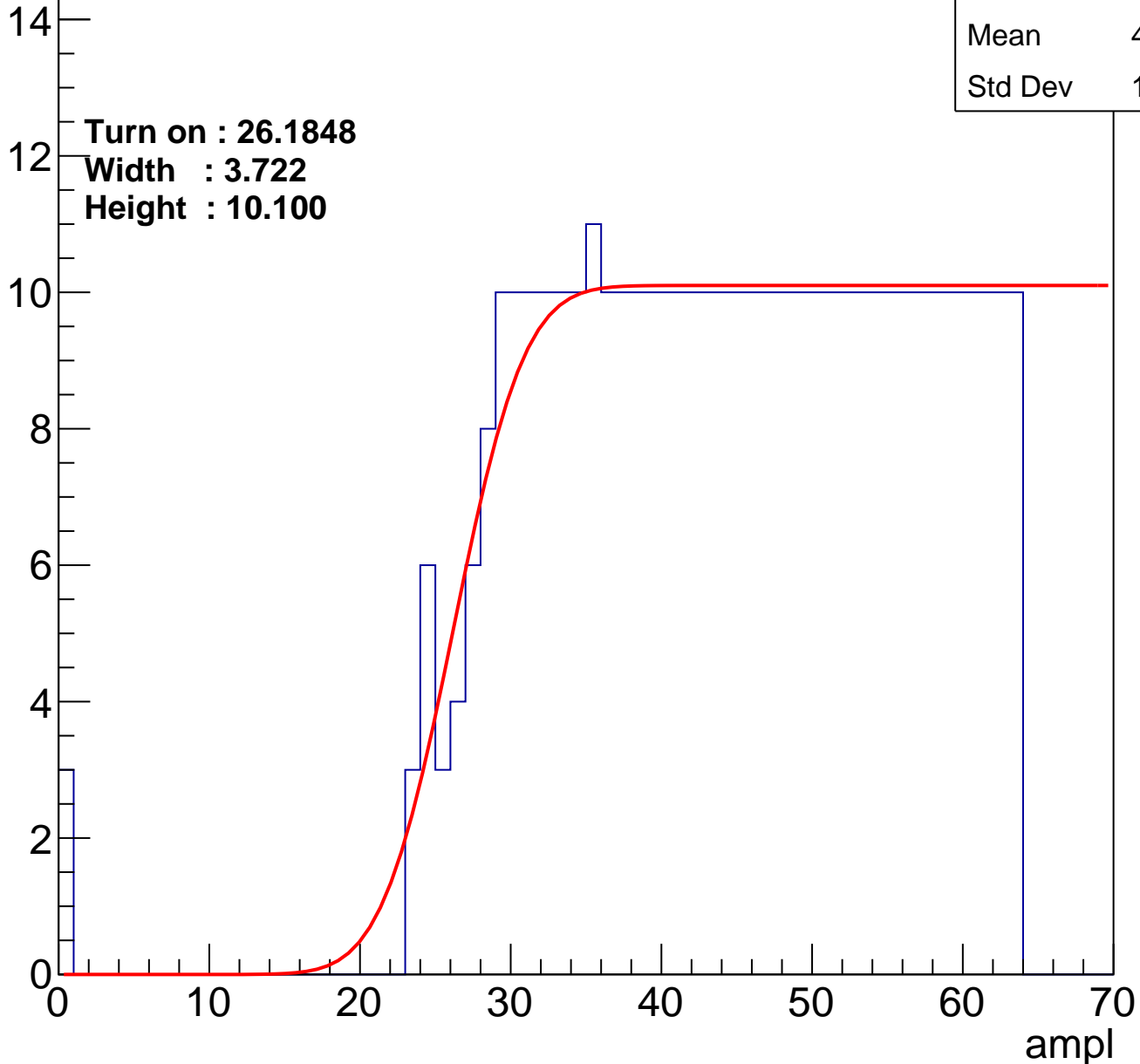
Entries	384
Mean	44.04
Std Dev	11.73

Turn on : 26.1848

Width : 3.722

Height : 10.100

Entry



# B1L101S, U9-ch124

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	356
Mean	45.35
Std Dev	11.14

**Turn on : 28.4293**

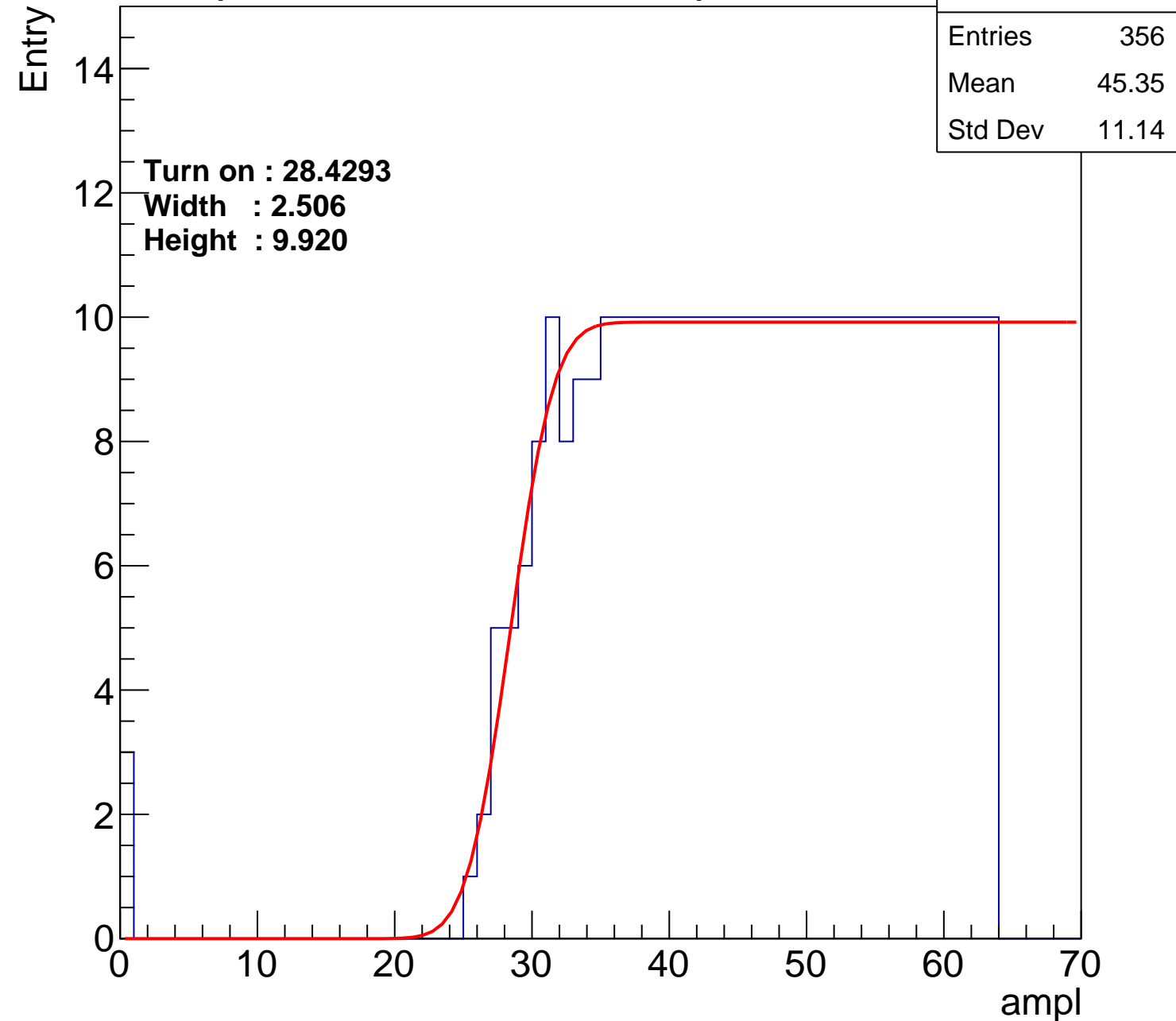
**Width : 2.506**

**Height : 9.920**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch125

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	366
Mean	44.88
Std Dev	11.36

Turn on : 27.9469

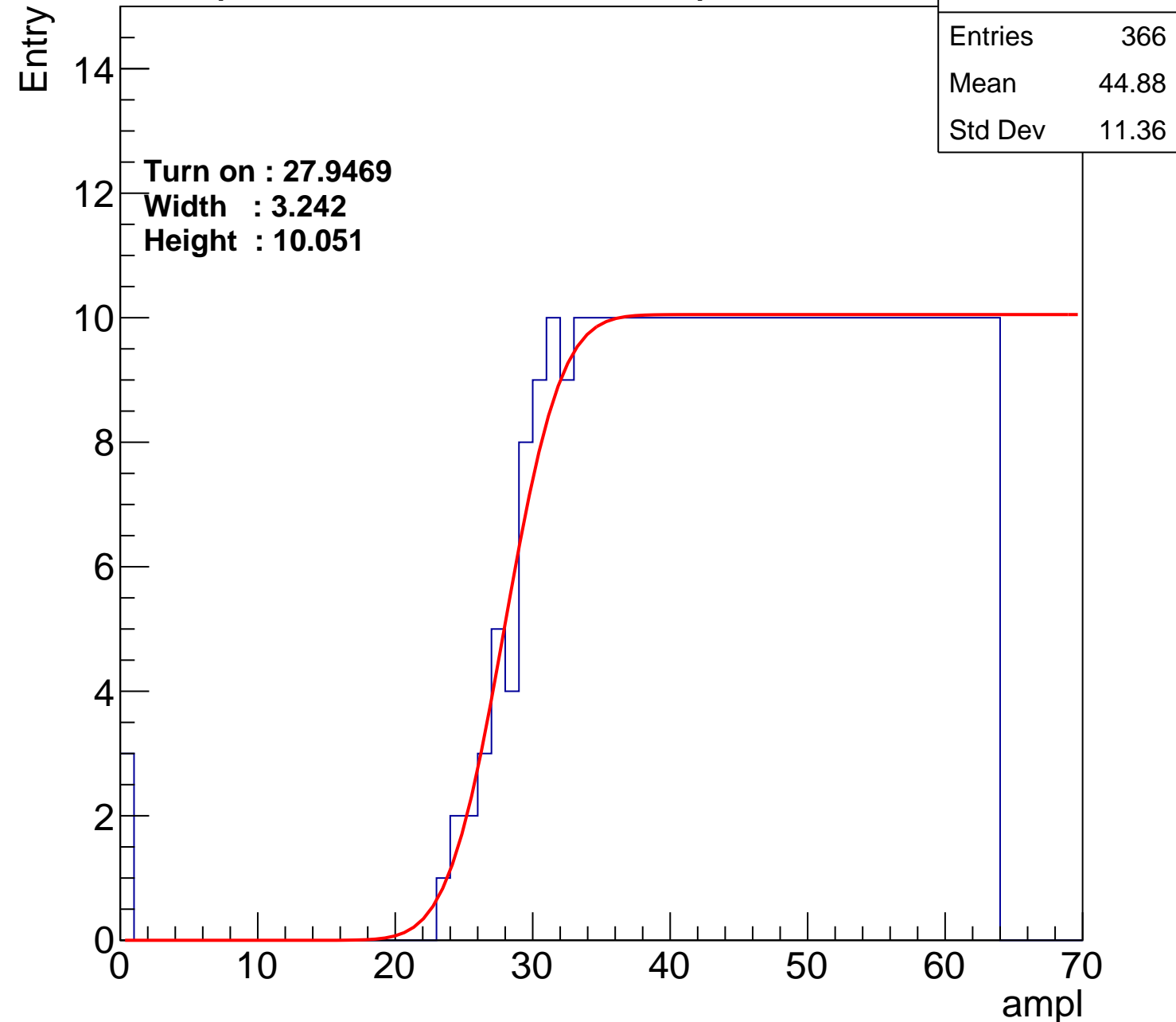
Width : 3.242

Height : 10.051

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch126

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	365
Mean	44.95
Std Dev	11.21

Turn on : 27.8562

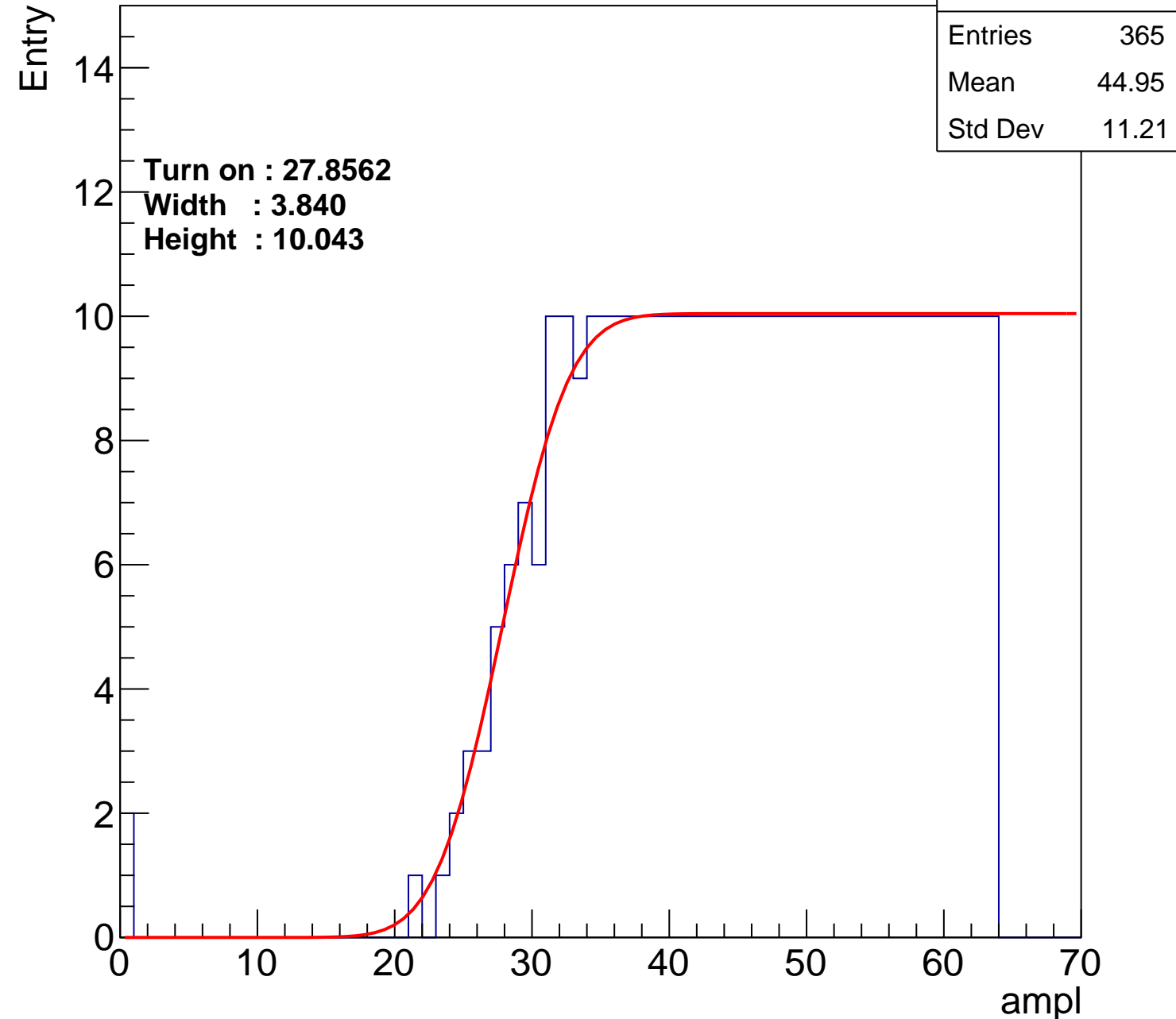
Width : 3.840

Height : 10.043

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L101S, U9-ch127

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	387
Mean	43.91
Std Dev	11.7

Turn on : 25.4412

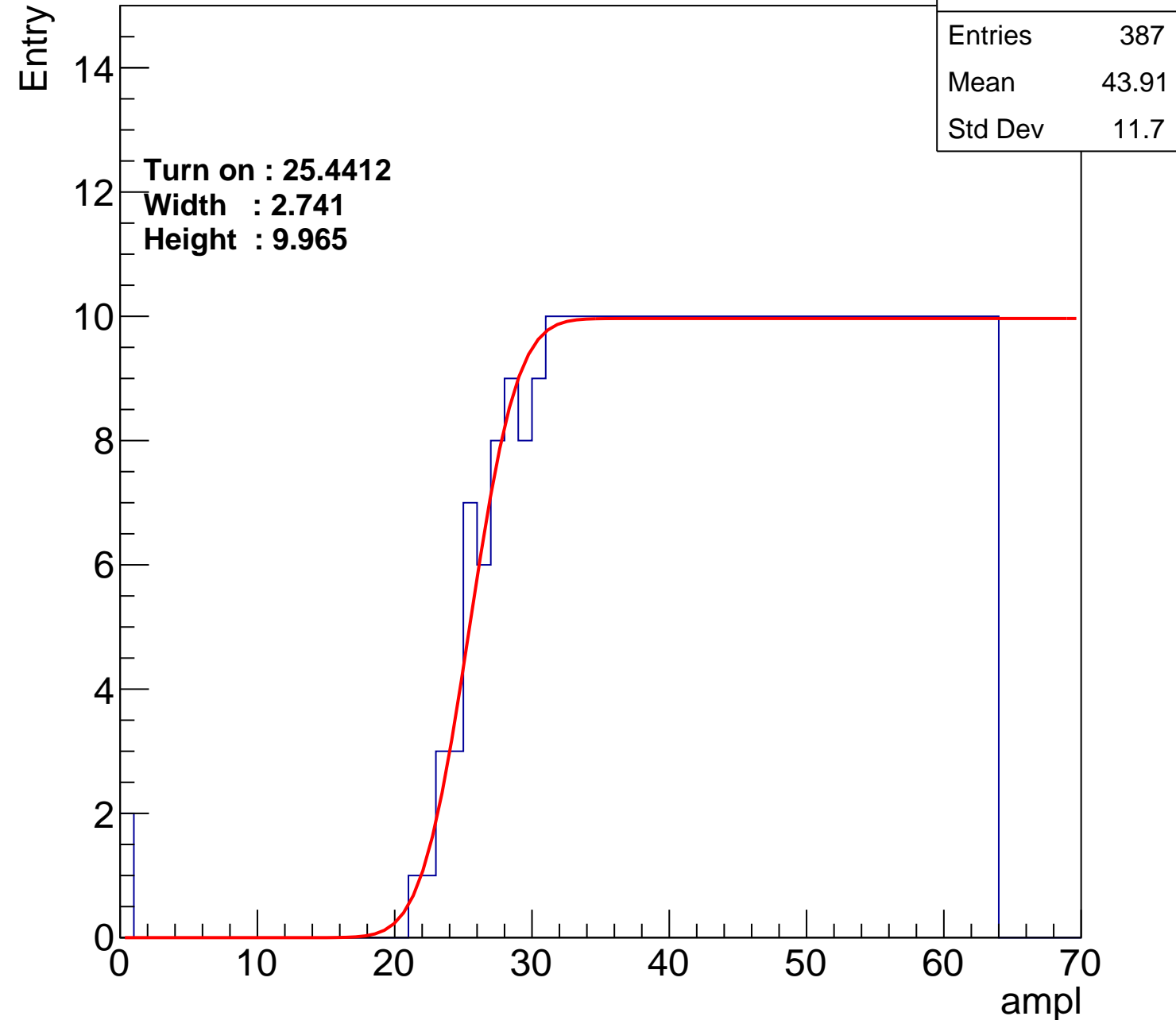
Width : 2.741

Height : 9.965

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch127

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	387
Mean	43.91
Std Dev	11.7

Turn on : 25.4412

Width : 2.741

Height : 9.965

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl

