

B1L103S, U5-ch0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	459
Mean	37.23
Std Dev	18.94

Turn on : 26.1628

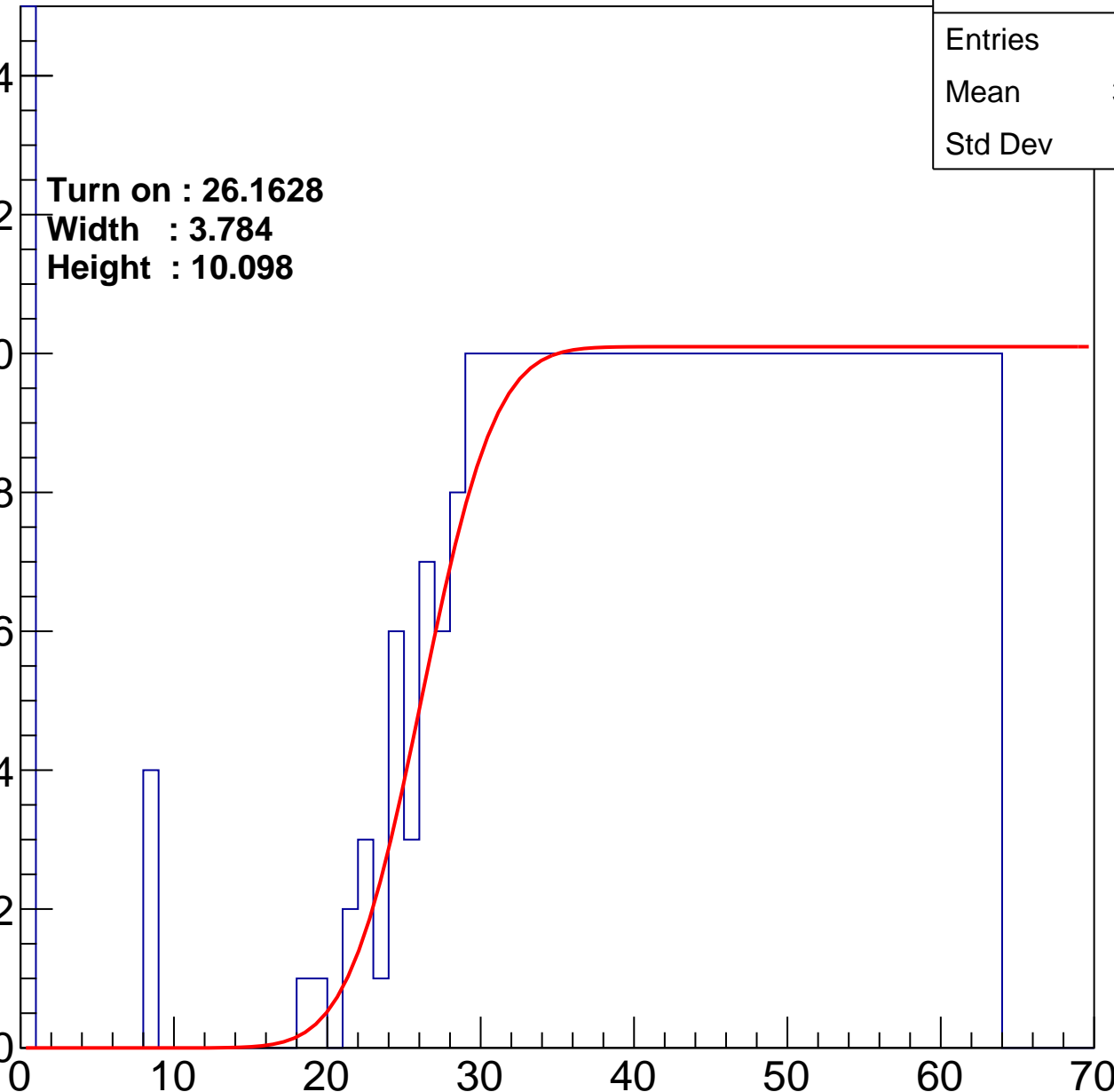
Width : 3.784

Height : 10.098

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	397
Mean	40.66
Std Dev	17.38

Turn on : 28.9427

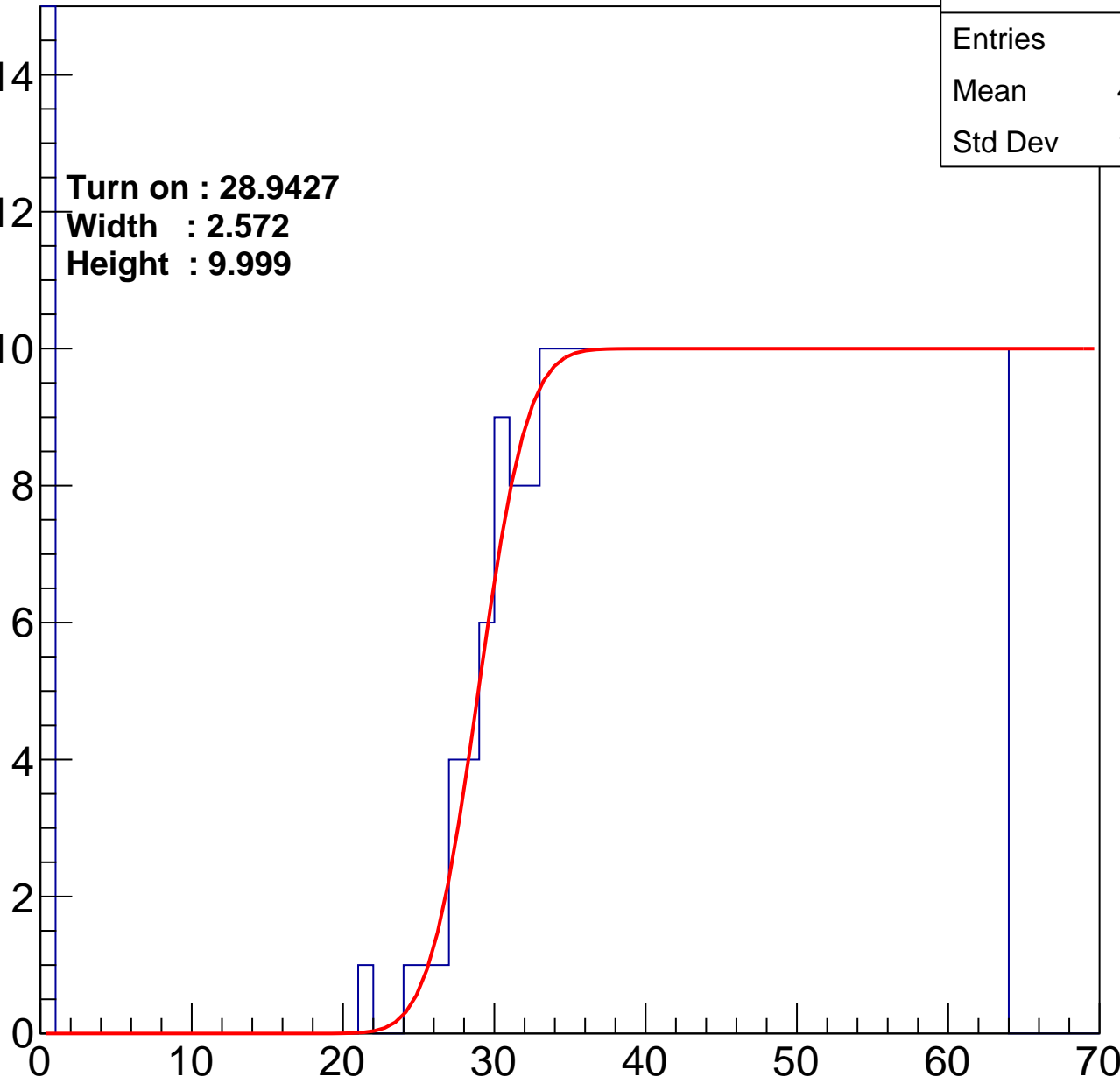
Width : 2.572

Height : 9.999

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	422
Mean	39.7
Std Dev	17.39

Turn on : 26.6961

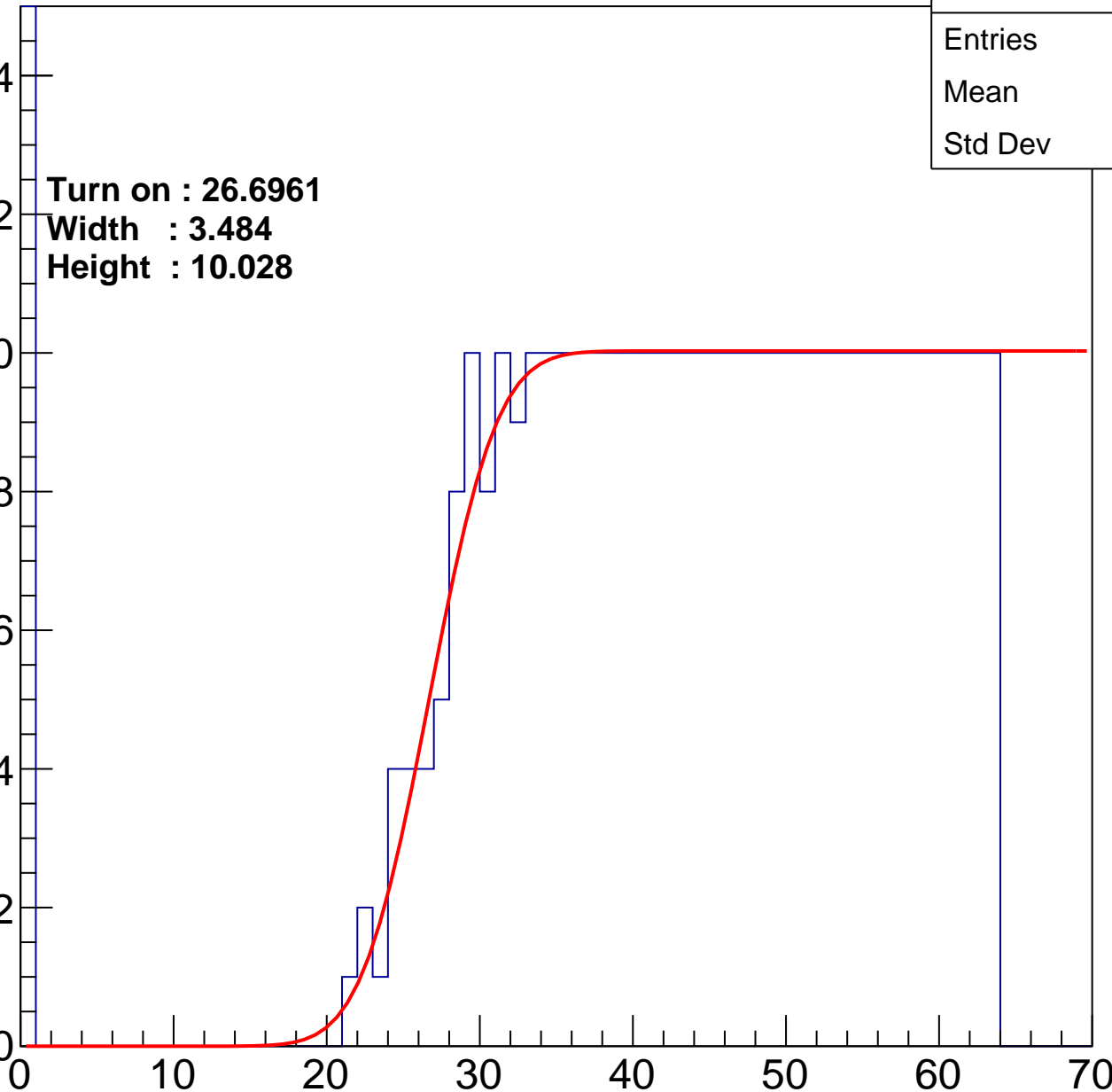
Width : 3.484

Height : 10.028

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	452
Mean	38.38
Std Dev	17.72

Turn on : 24.2759

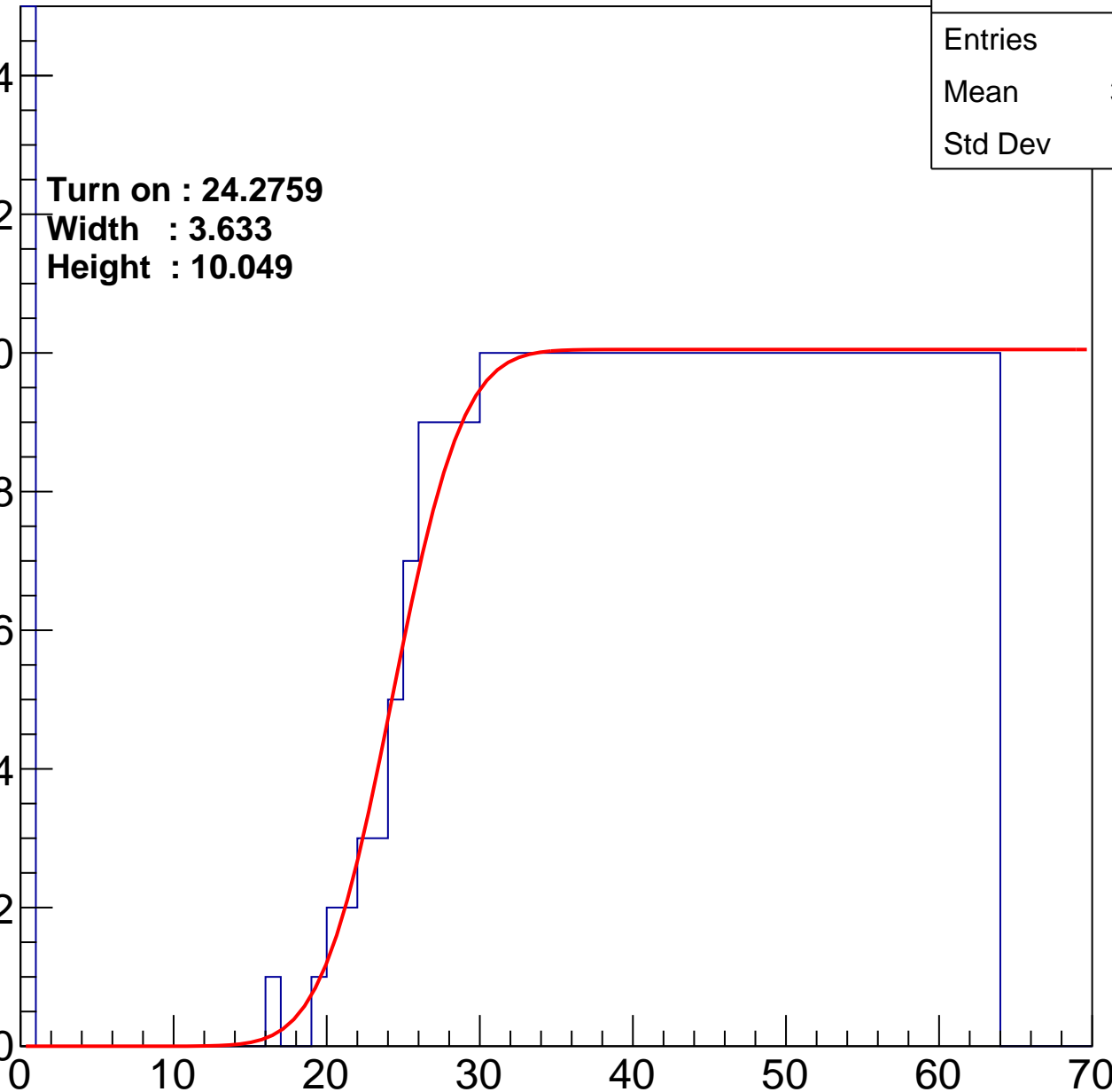
Width : 3.633

Height : 10.049

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch4

calib_packv5_041523_1651.root, FC#0, port C2

Entries	426
Mean	39.39
Std Dev	17.68

Turn on : 26.7262

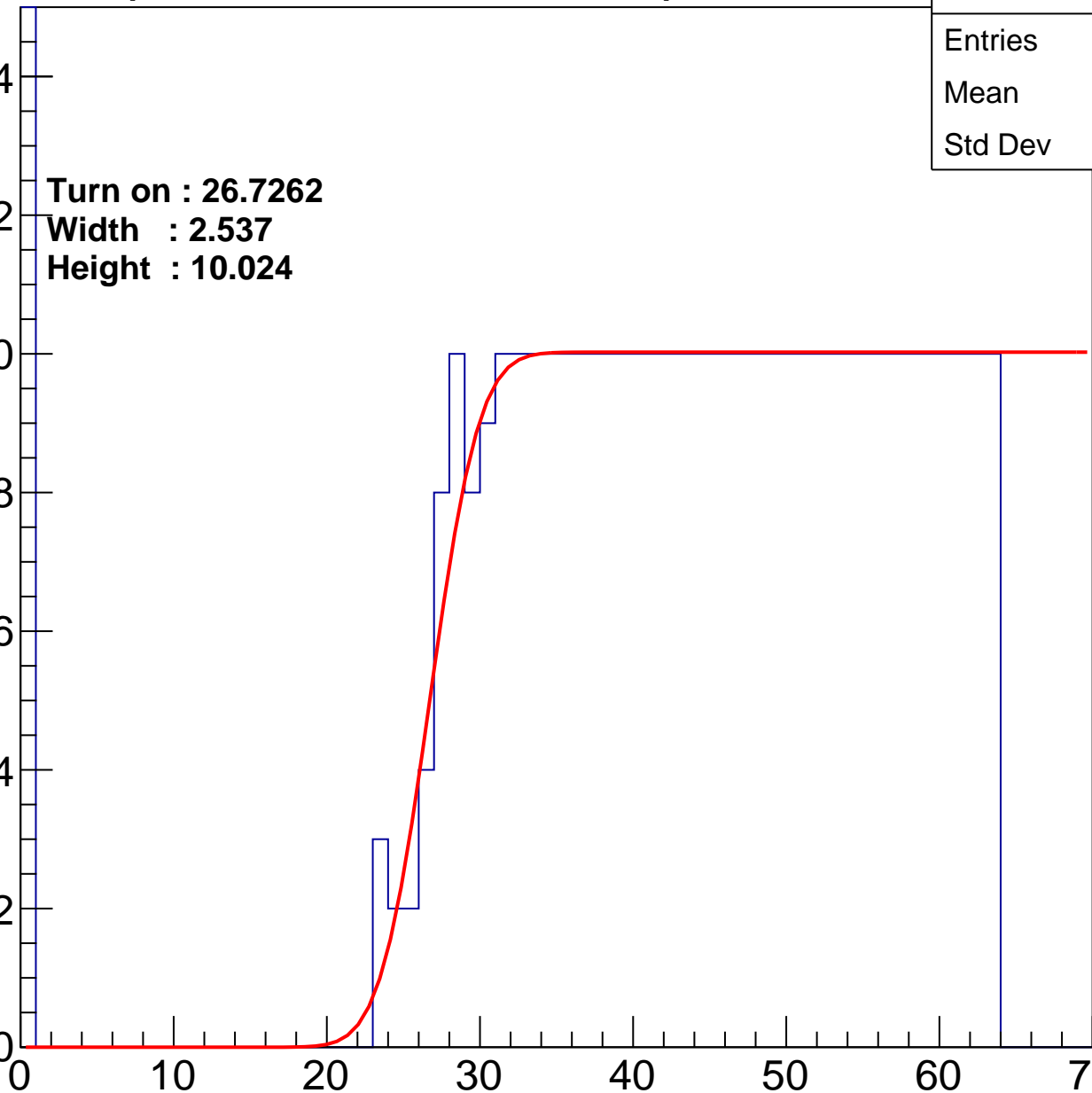
Width : 2.537

Height : 10.024

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch5

calib_packv5_041523_1651.root, FC#0, port C2

Entries	428
Mean	39.49
Std Dev	17.41

Turn on : 26.2082

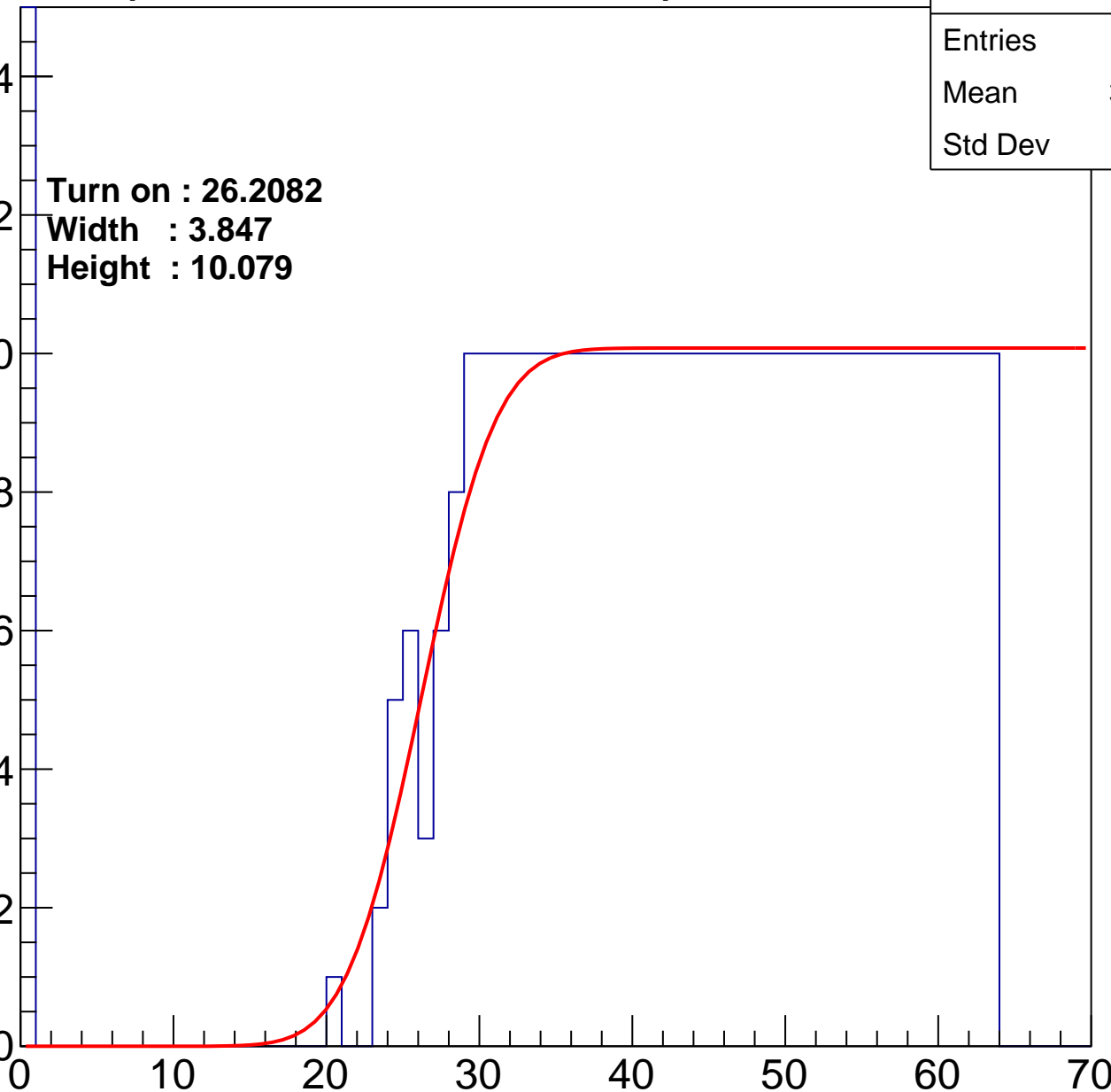
Width : 3.847

Height : 10.079

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch6

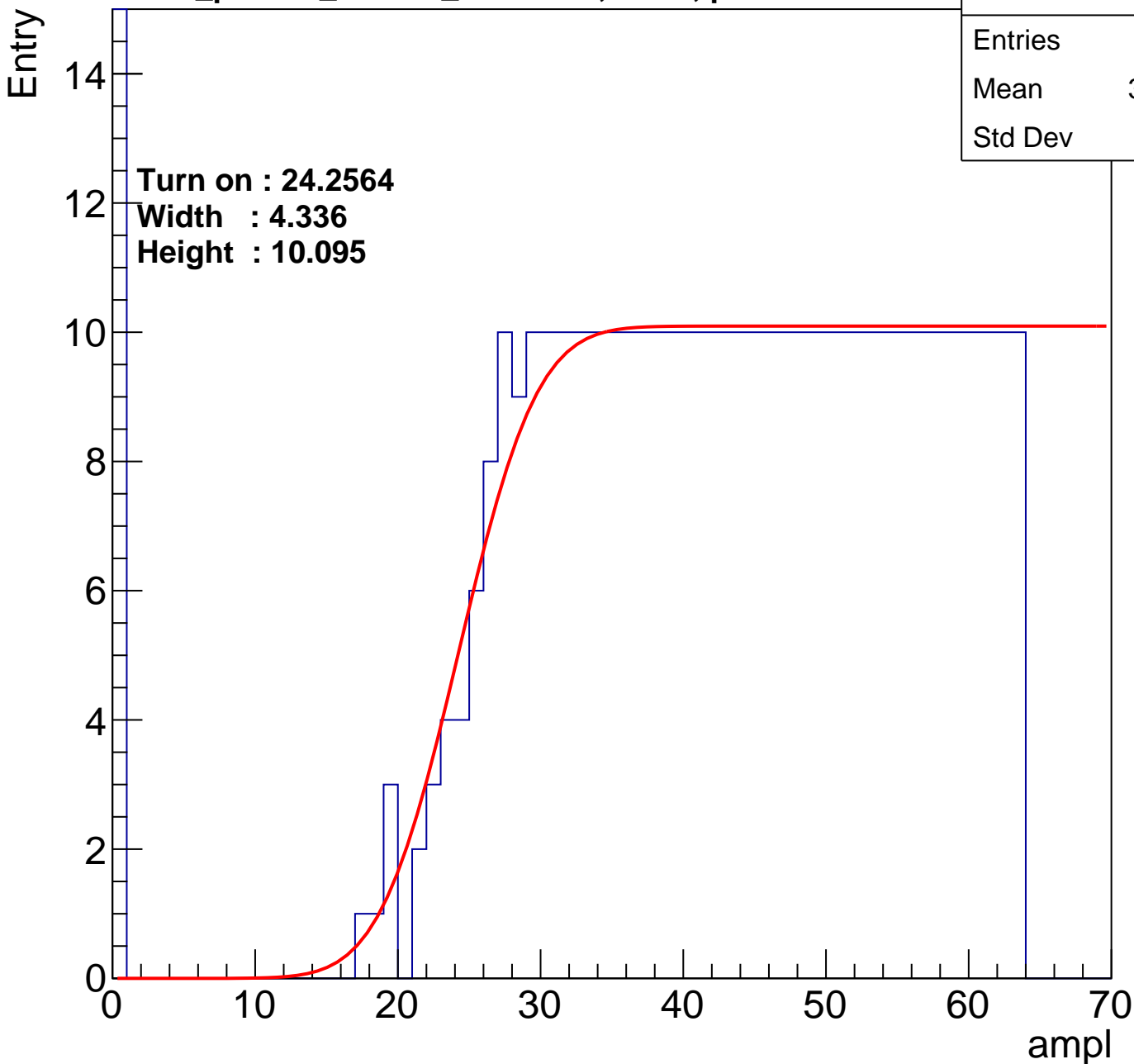
calib_packv5_041523_1651.root, FC#0, port C2

Entries	454
Mean	38.26
Std Dev	17.8

Turn on : 24.2564

Width : 4.336

Height : 10.095



B1L103S, U5-ch7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	430
Mean	38.53
Std Dev	18.64

Turn on : 27.8673

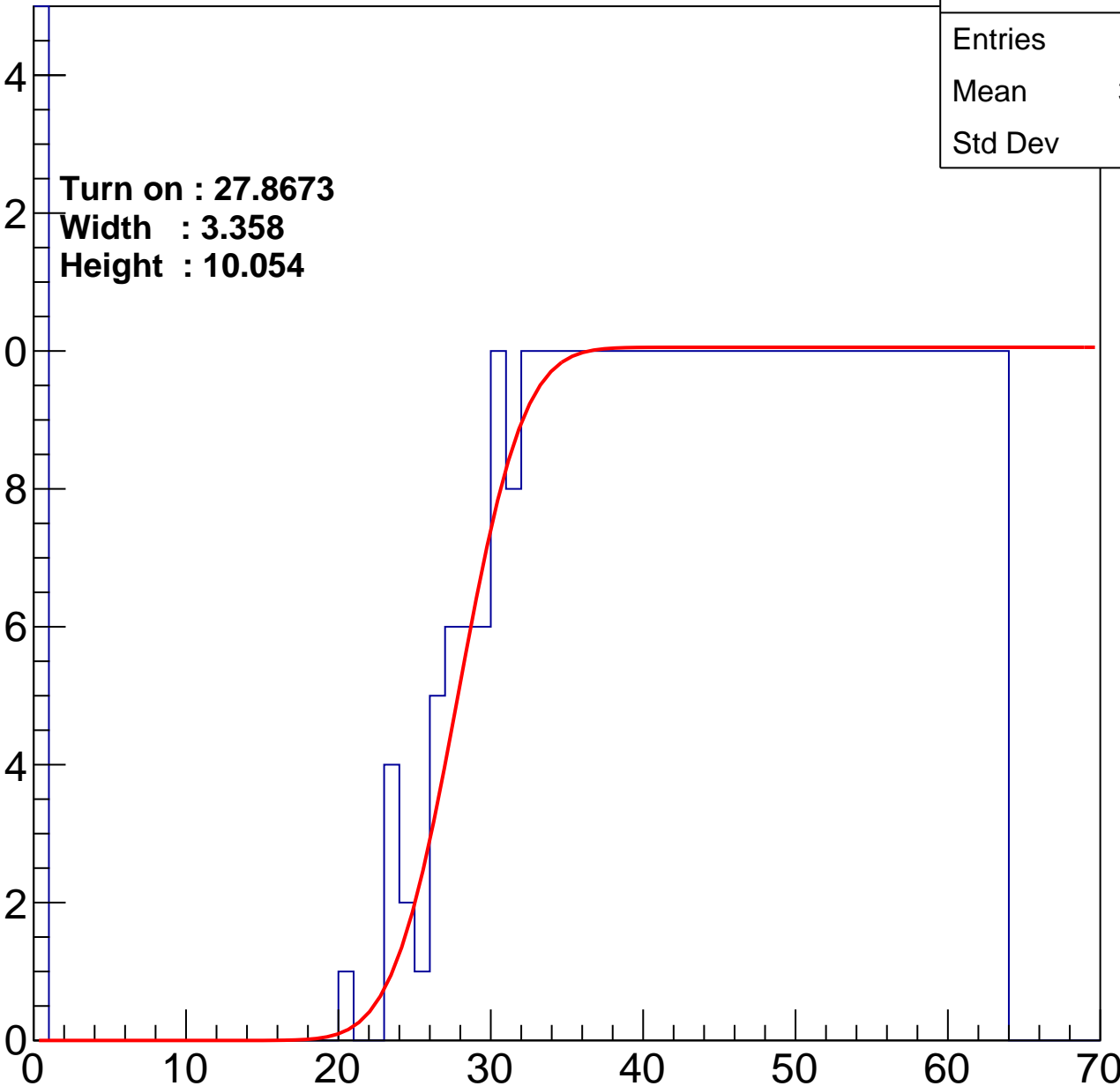
Width : 3.358

Height : 10.054

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch8

calib_packv5_041523_1651.root, FC#0, port C2

Entries	445
Mean	38.09
Std Dev	18.49

Turn on : 26.2028

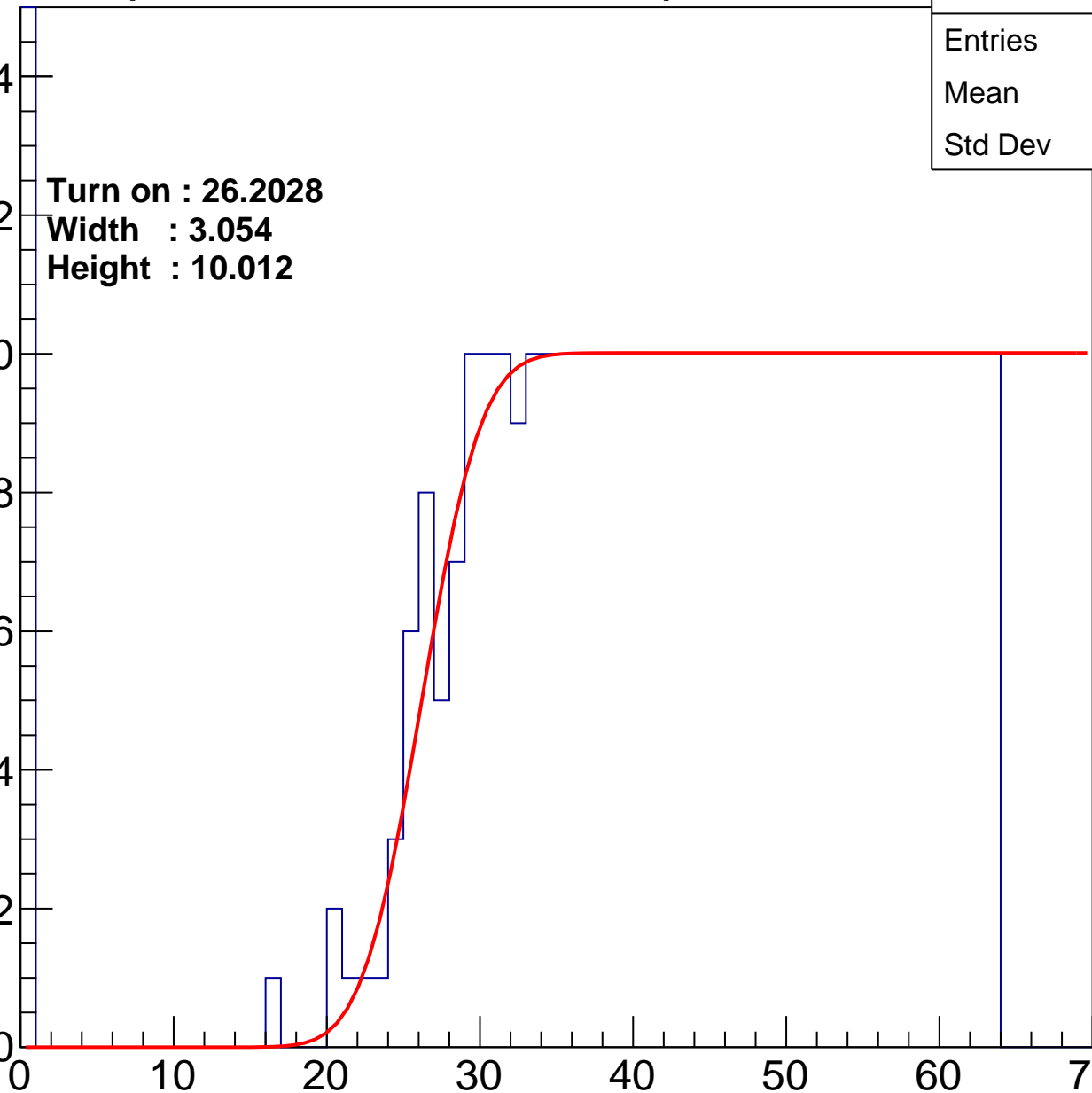
Width : 3.054

Height : 10.012

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch9

calib_packv5_041523_1651.root, FC#0, port C2

Entries	443
Mean	38.44
Std Dev	18.11

Turn on : 25.4952

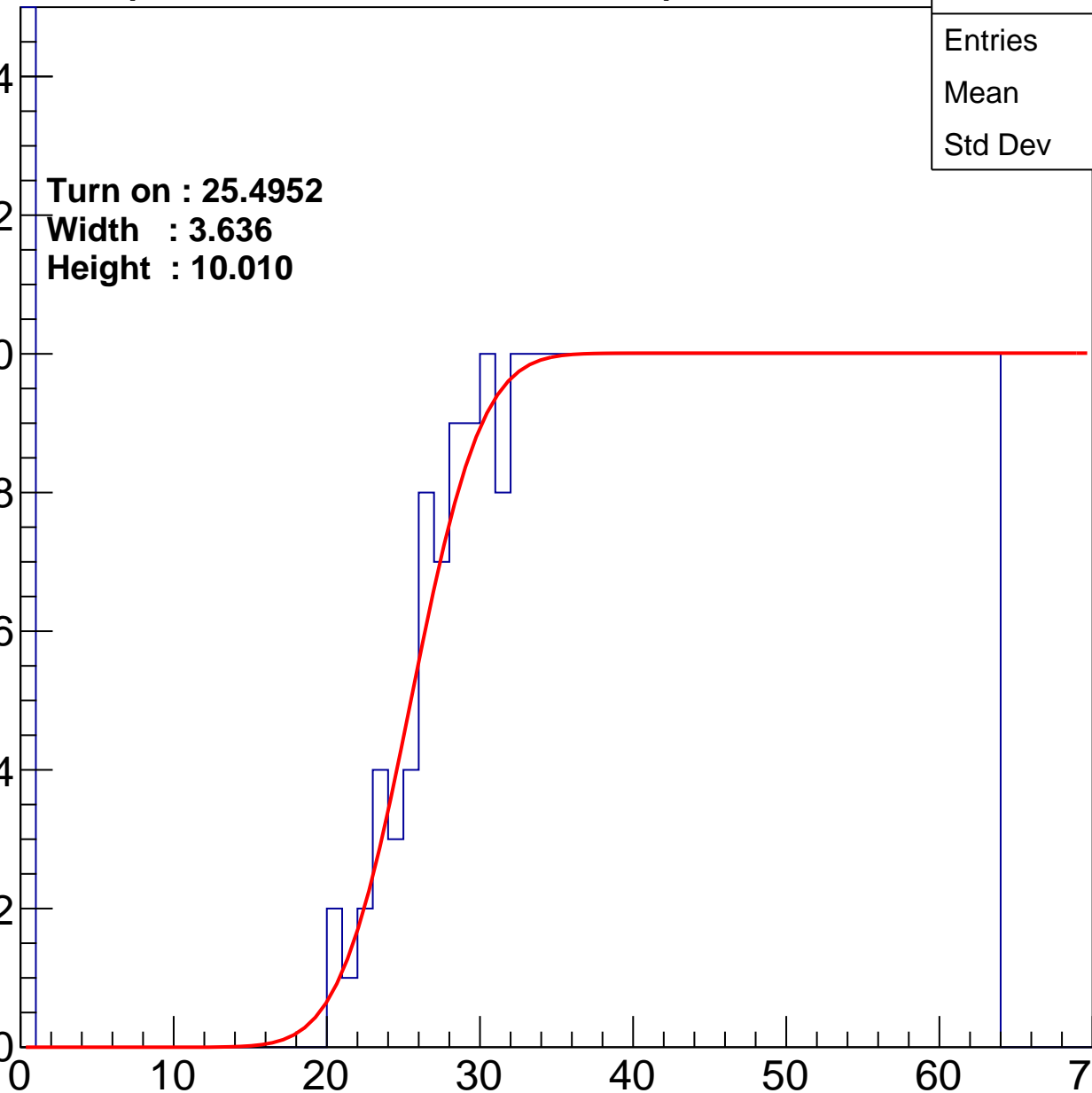
Width : 3.636

Height : 10.010

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch10

calib_packv5_041523_1651.root, FC#0, port C2

Entries	424
Mean	39.68
Std Dev	17.3

Turn on : 26.4694

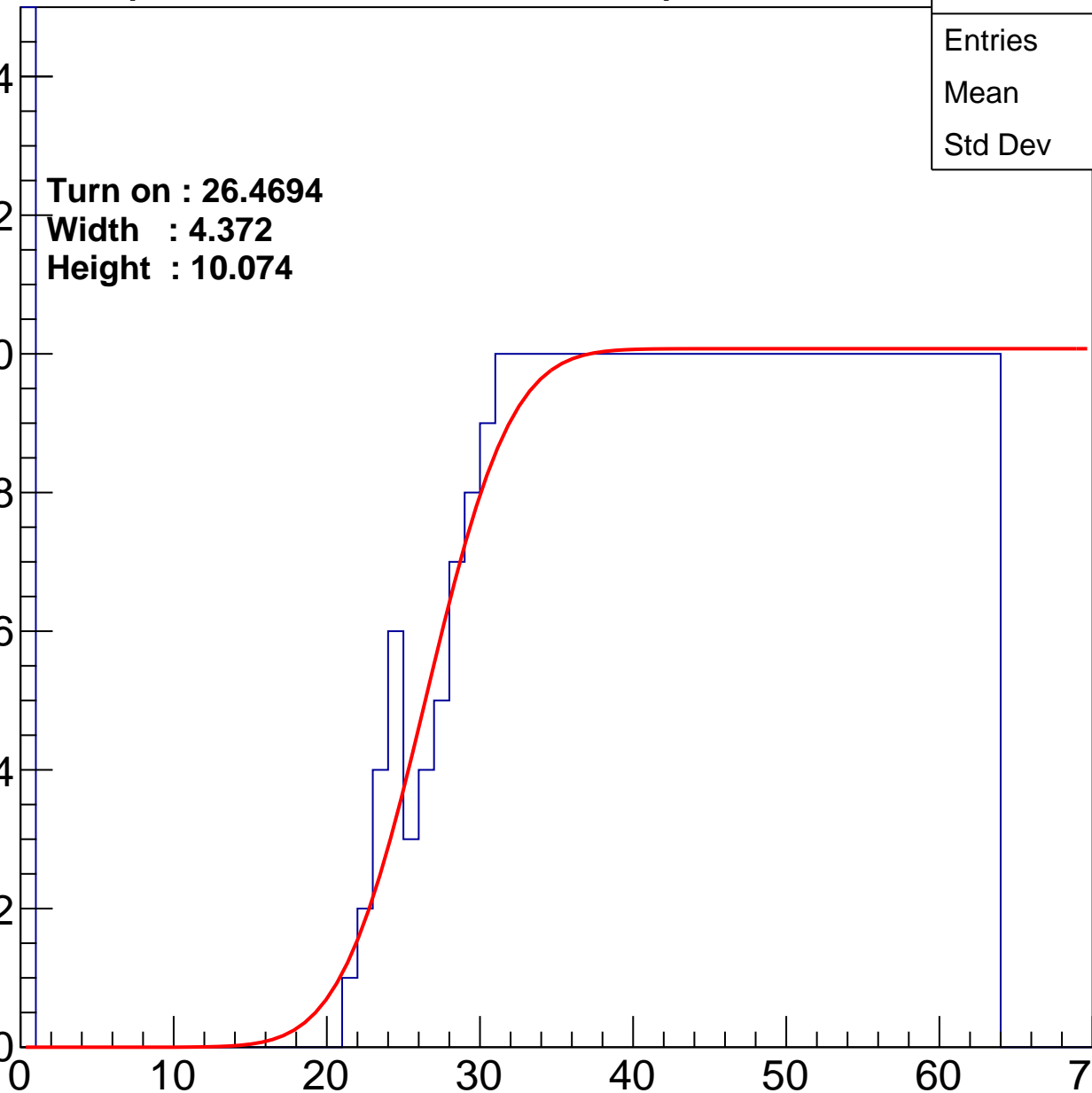
Width : 4.372

Height : 10.074

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch11

calib_packv5_041523_1651.root, FC#0, port C2

Entries	431
Mean	38.85
Std Dev	18.13

Turn on : 26.3602

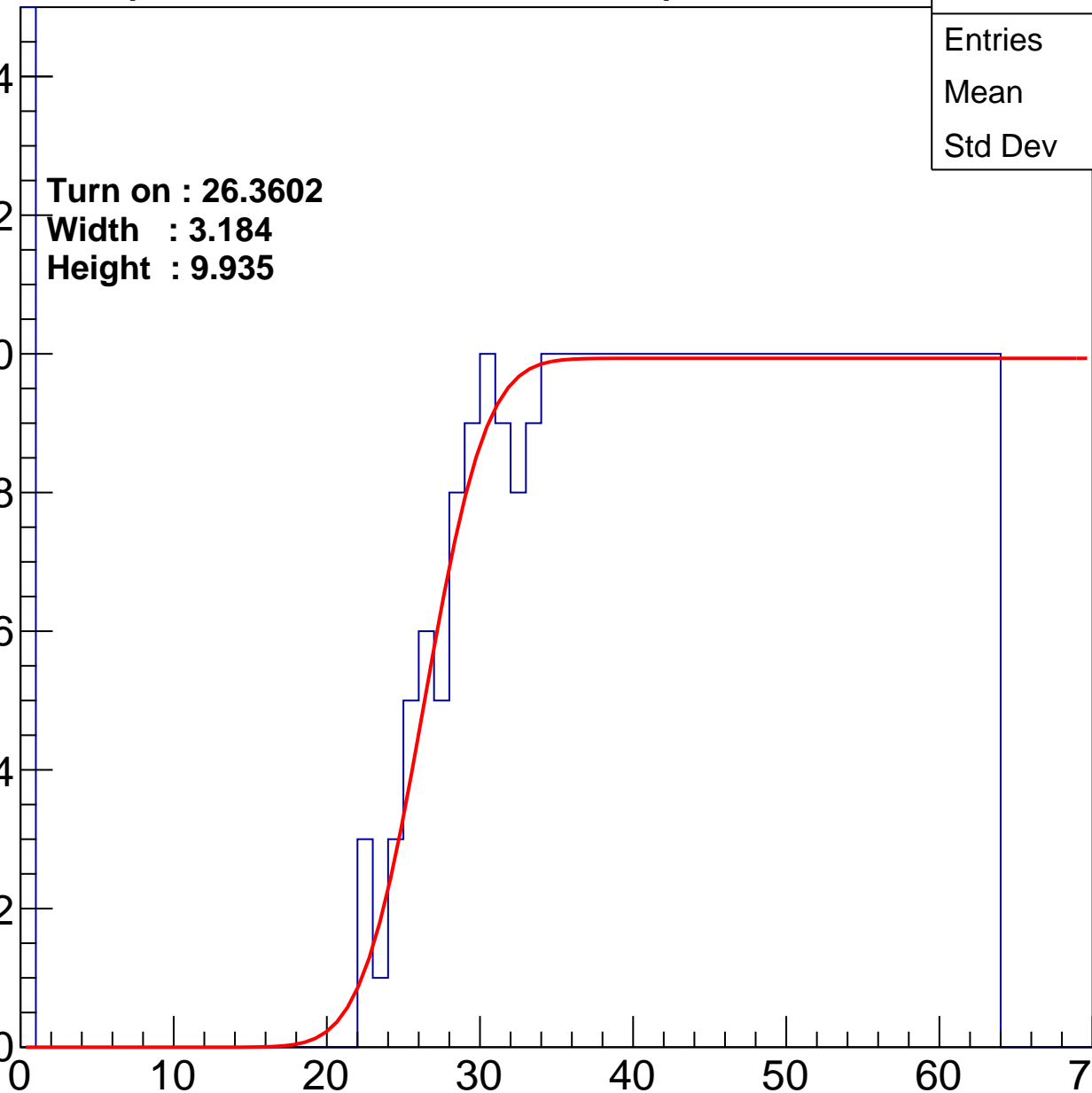
Width : 3.184

Height : 9.935

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch12

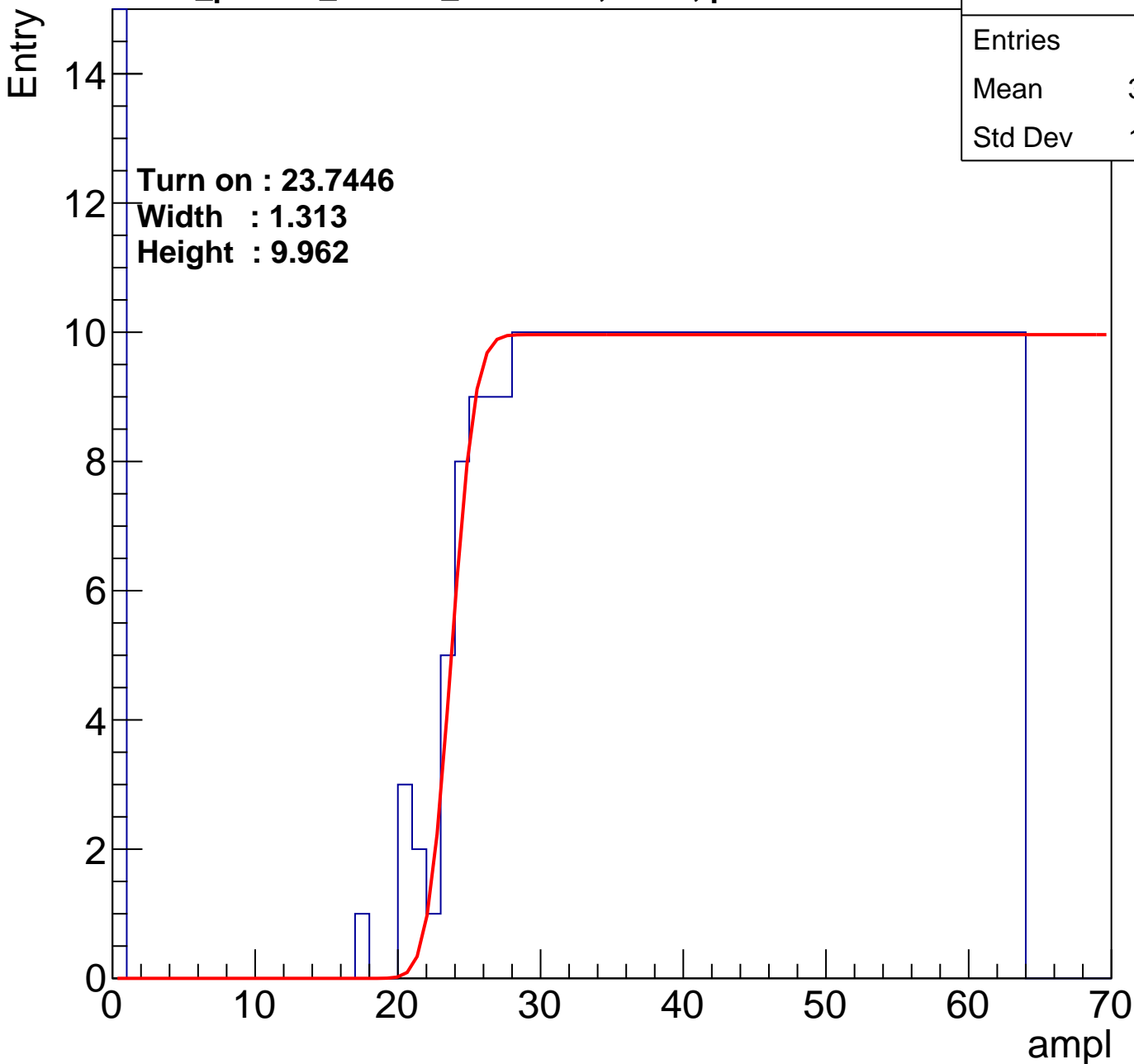
calib_packv5_041523_1651.root, FC#0, port C2

Entries	466
Mean	37.62
Std Dev	18.12

Turn on : 23.7446

Width : 1.313

Height : 9.962



B1L103S, U5-ch13

calib_packv5_041523_1651.root, FC#0, port C2

Entries	437
Mean	38.64
Std Dev	18.19

Turn on : 25.9344

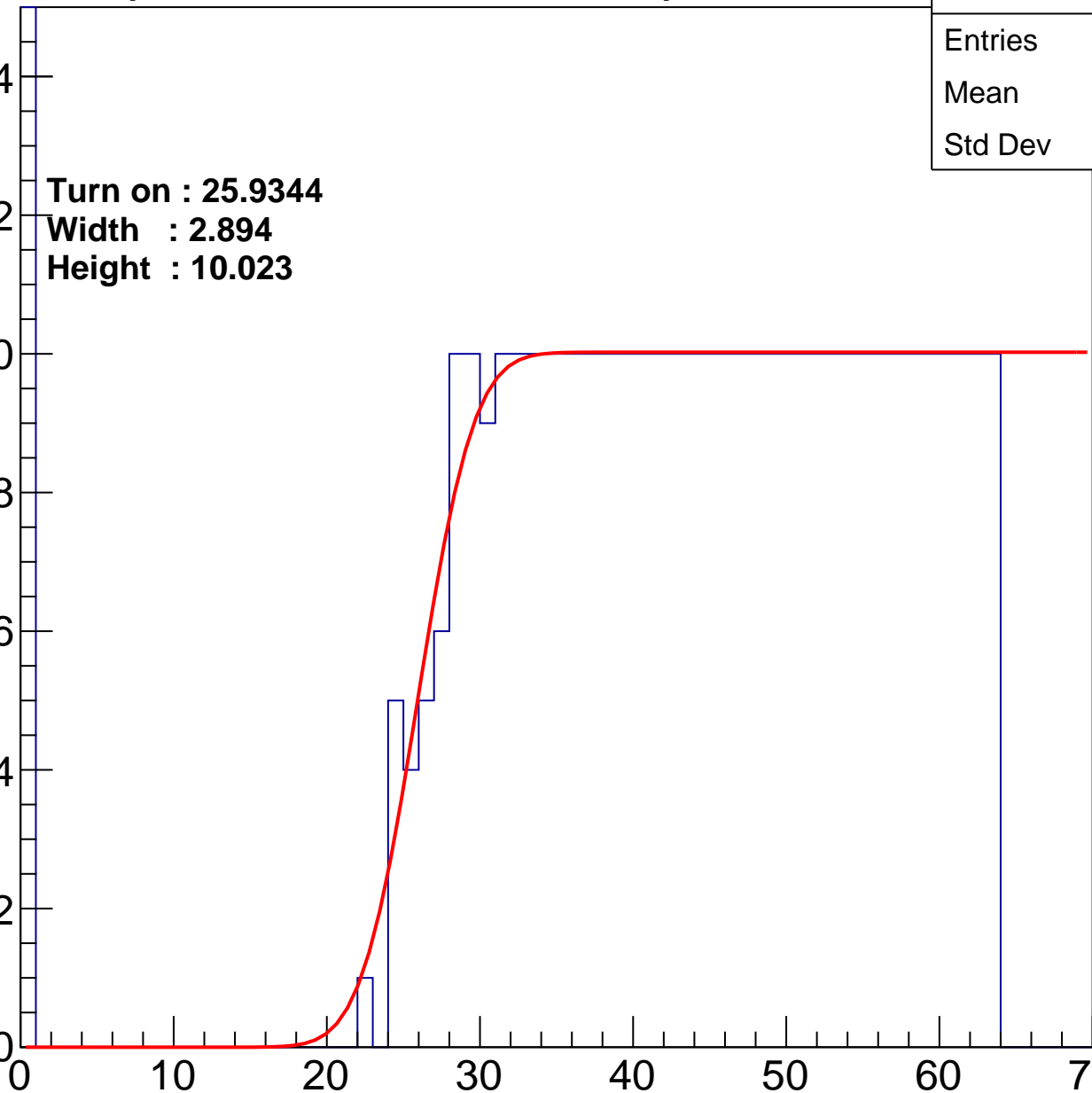
Width : 2.894

Height : 10.023

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch14

calib_packv5_041523_1651.root, FC#0, port C2

Entries	440
Mean	39.31
Std Dev	16.99

Turn on : 24.4027

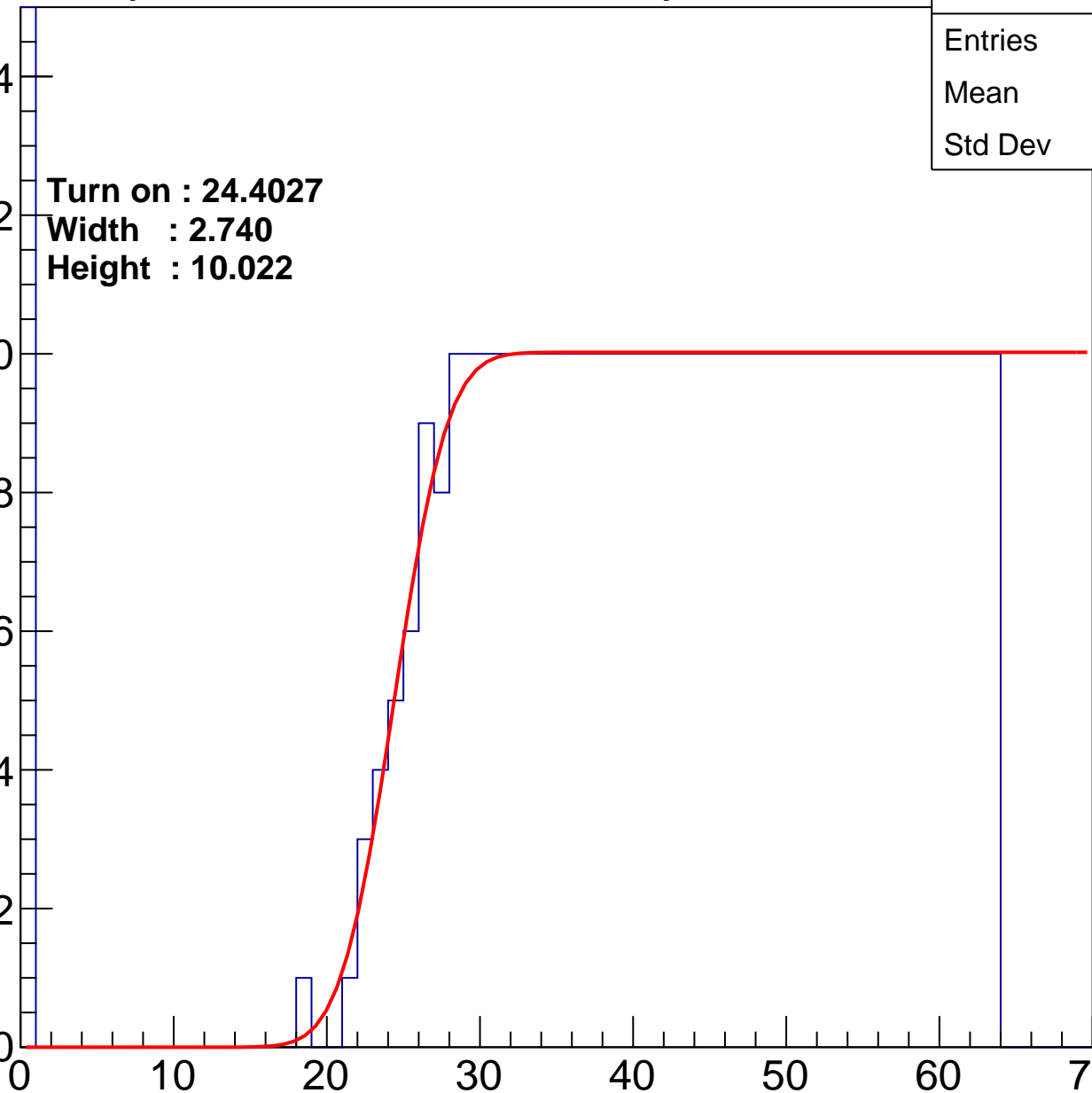
Width : 2.740

Height : 10.022

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch15

calib_packv5_041523_1651.root, FC#0, port C2

Entries	427
Mean	39.88
Std Dev	16.86

Turn on : 25.9277

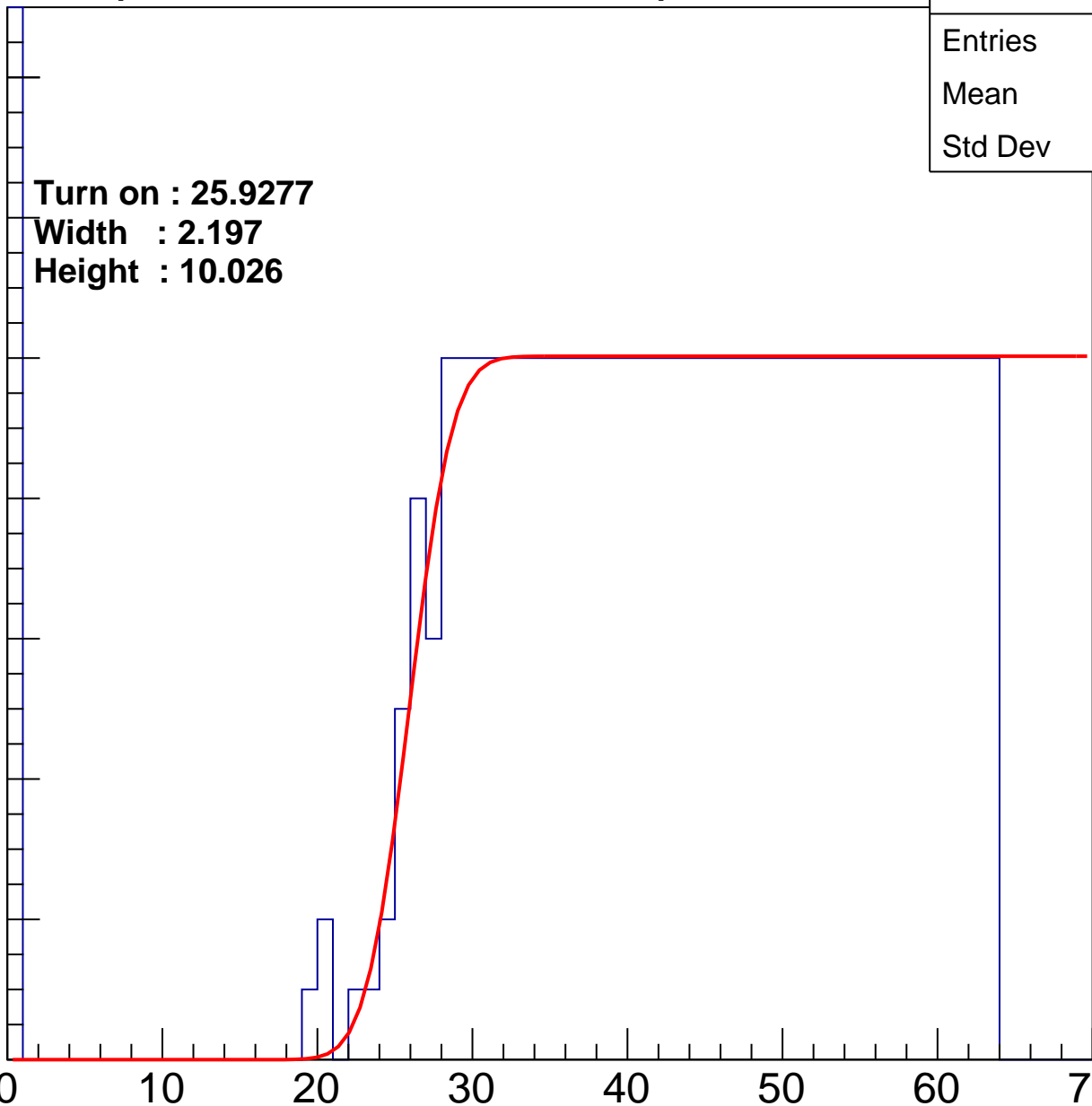
Width : 2.197

Height : 10.026

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch16

calib_packv5_041523_1651.root, FC#0, port C2

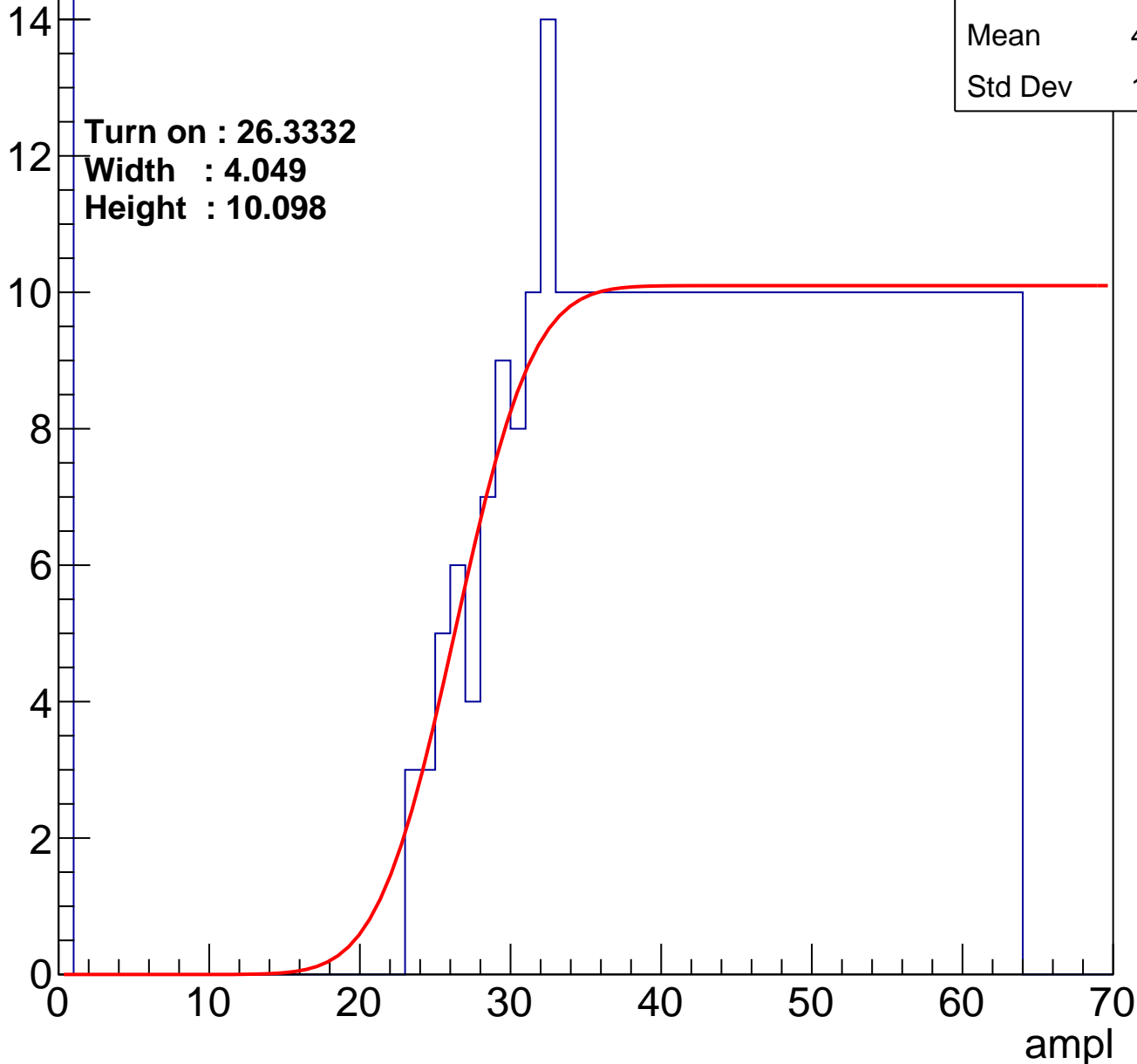
Entries	417
Mean	40.44
Std Dev	16.58

Turn on : 26.3332

Width : 4.049

Height : 10.098

Entry



B1L103S, U5-ch17

calib_packv5_041523_1651.root, FC#0, port C2

Entries	423
Mean	39.15
Std Dev	18.18

Turn on : 27.4900

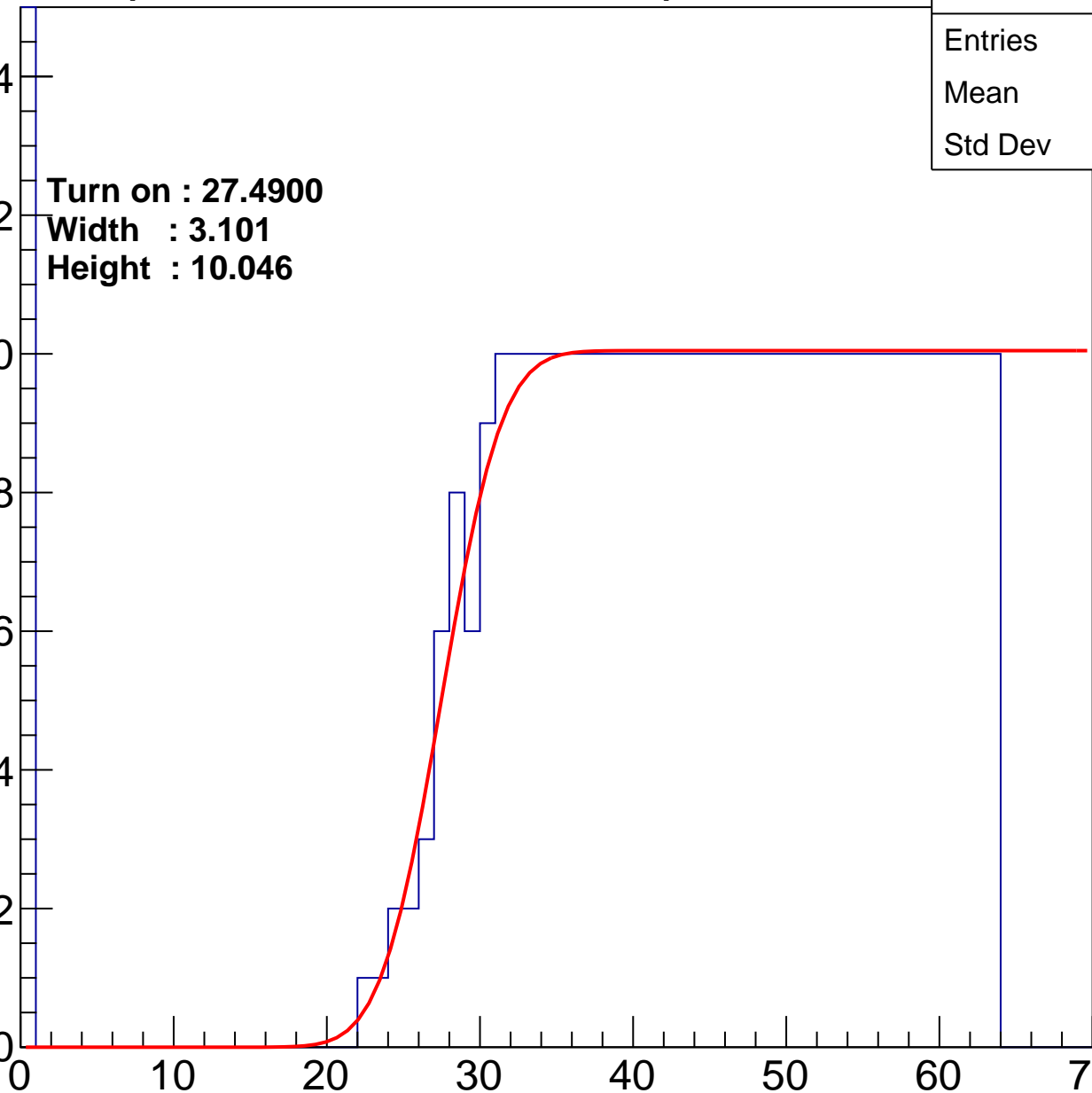
Width : 3.101

Height : 10.046

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch18

calib_packv5_041523_1651.root, FC#0, port C2

Entries	425
Mean	39.53
Std Dev	17.52

Turn on : 26.4196

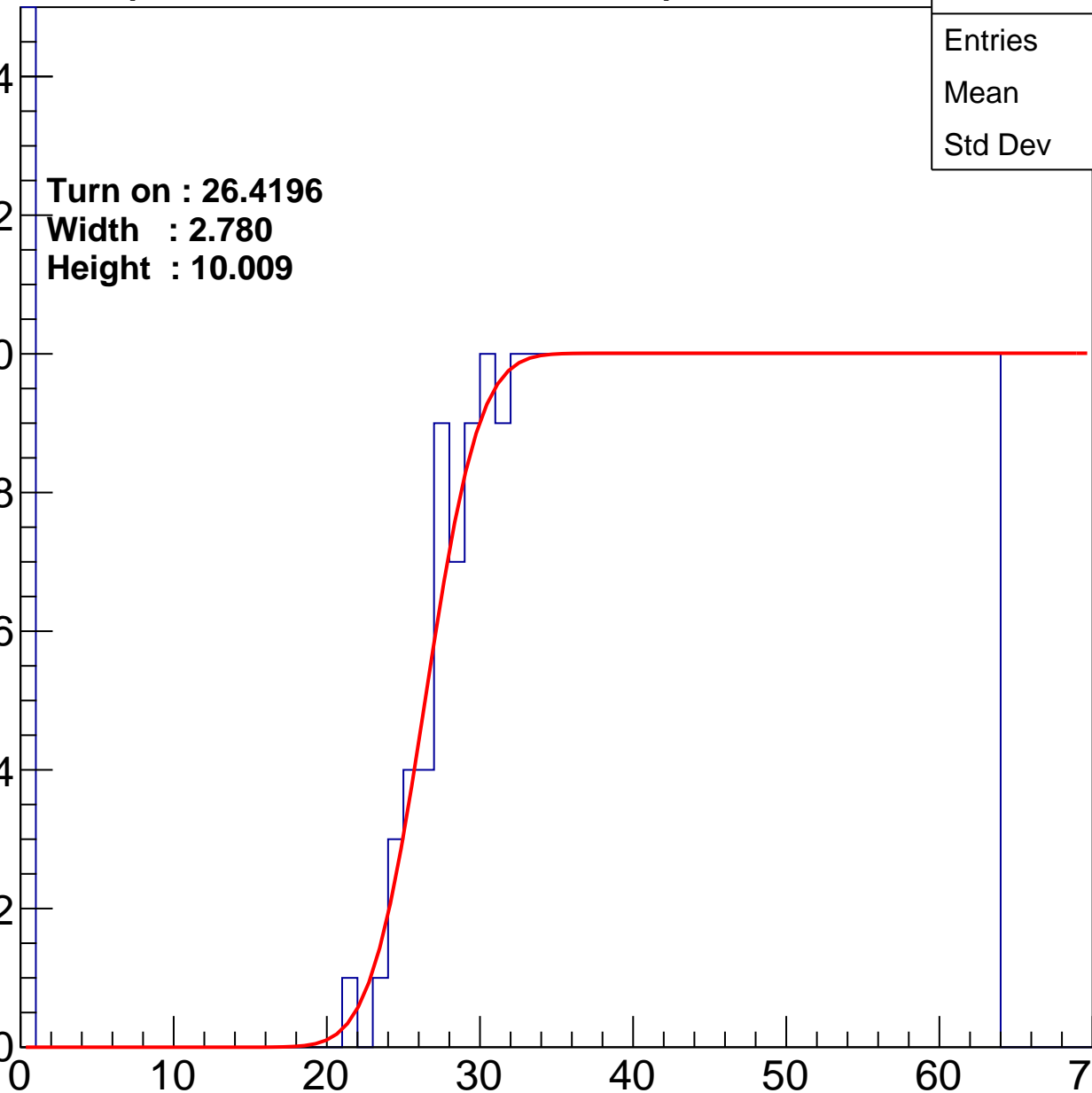
Width : 2.780

Height : 10.009

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch19

calib_packv5_041523_1651.root, FC#0, port C2

Entries	418
Mean	40.83
Std Dev	15.78

Turn on : 24.5677

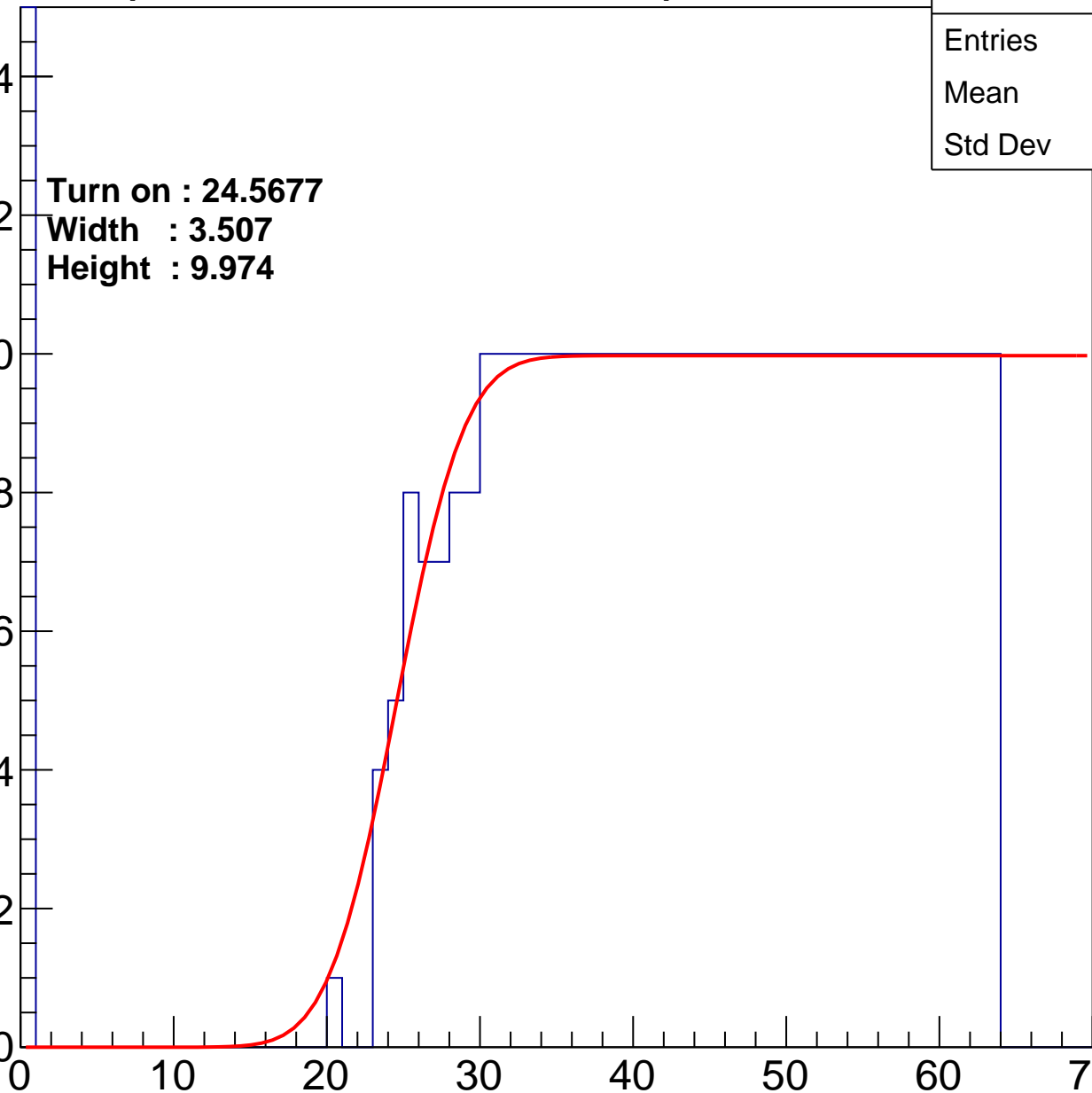
Width : 3.507

Height : 9.974

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch20

calib_packv5_041523_1651.root, FC#0, port C2

Entries	466
Mean	37.33
Std Dev	18.54

Turn on : 24.3047

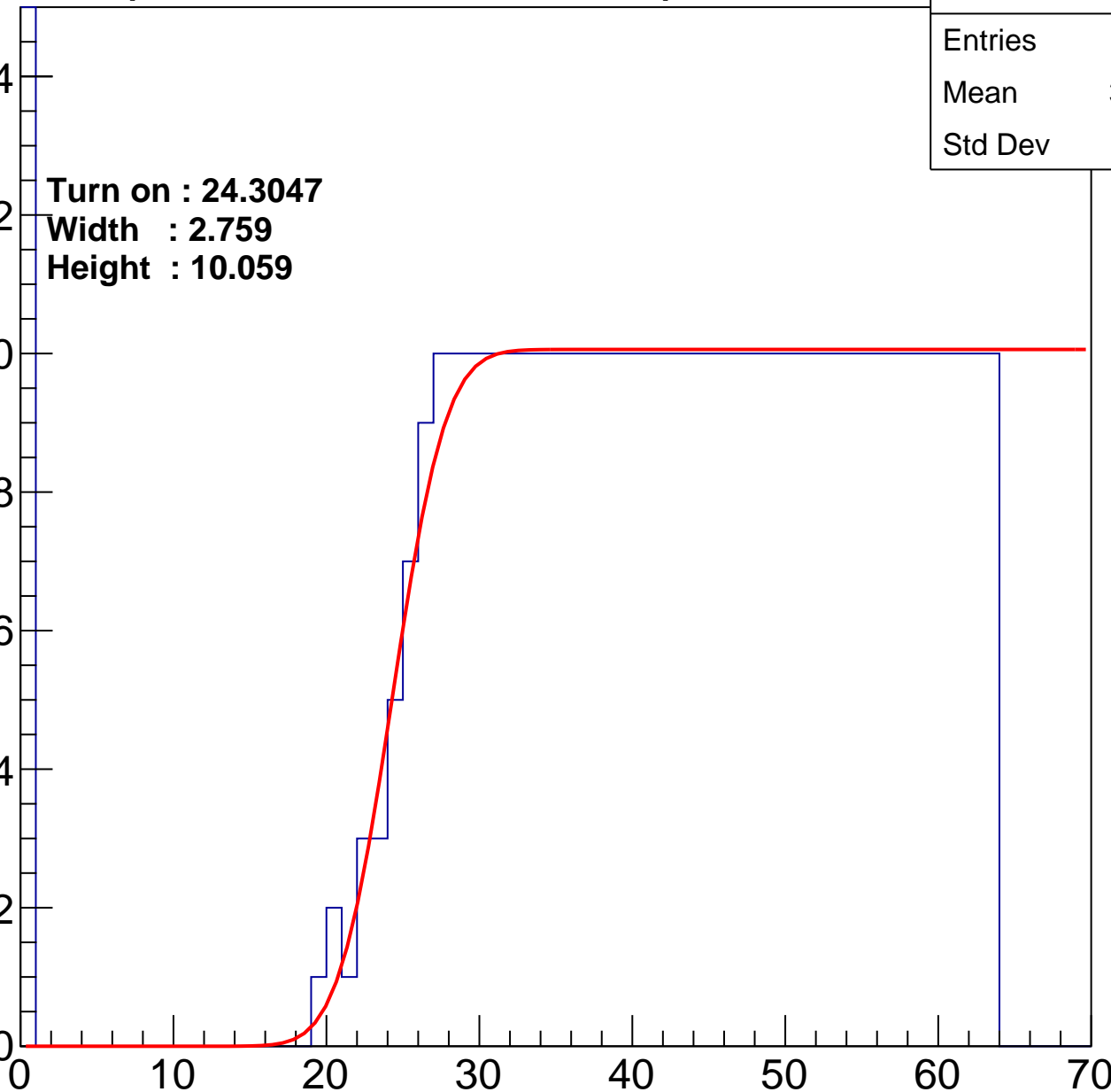
Width : 2.759

Height : 10.059

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch21

calib_packv5_041523_1651.root, FC#0, port C2

Entries	431
Mean	38.55
Std Dev	18.6

Turn on : 27.1842

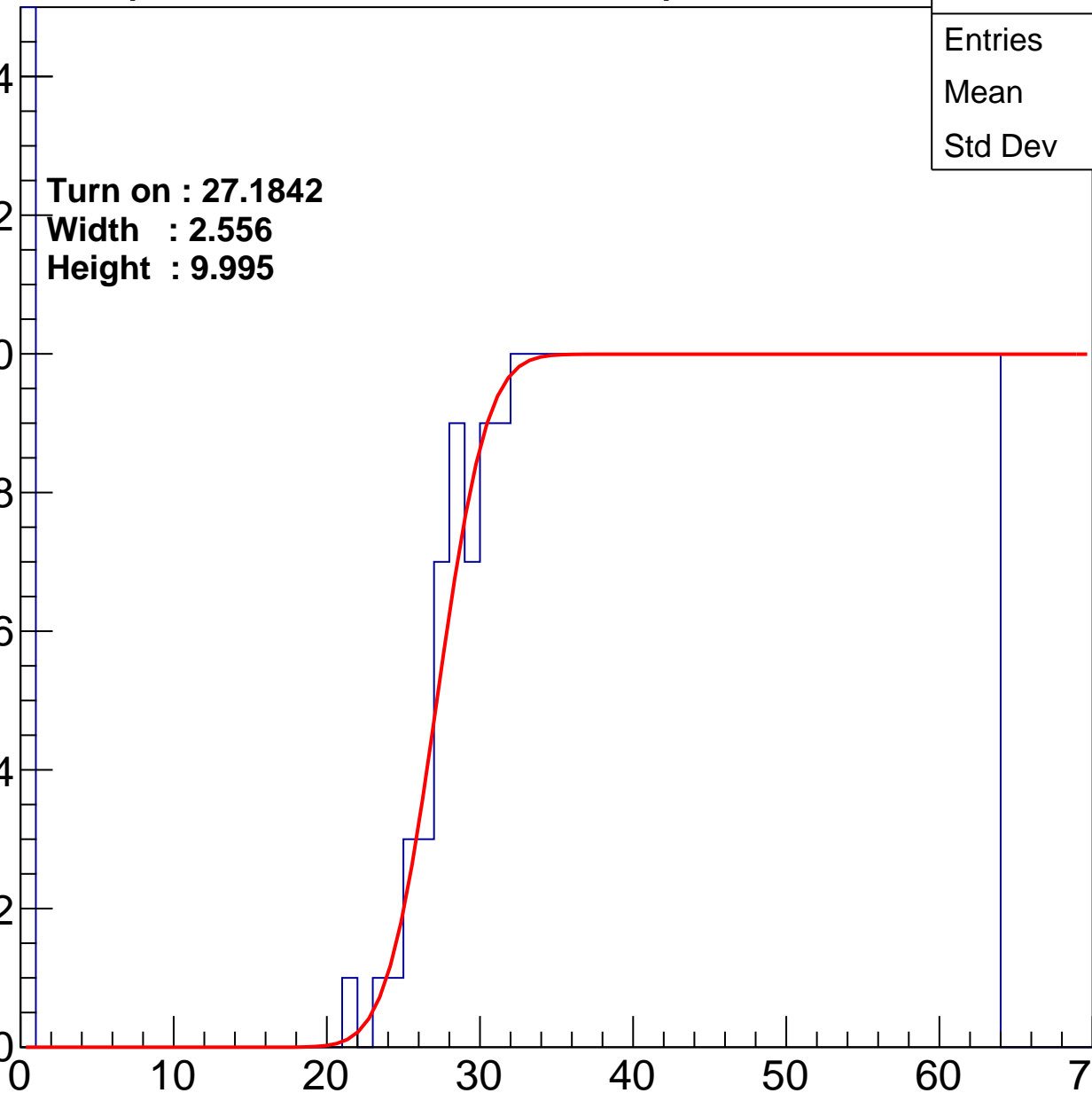
Width : 2.556

Height : 9.995

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch22

calib_packv5_041523_1651.root, FC#0, port C2

Entries	425
Mean	39.91
Std Dev	16.9

Turn on : 25.3703

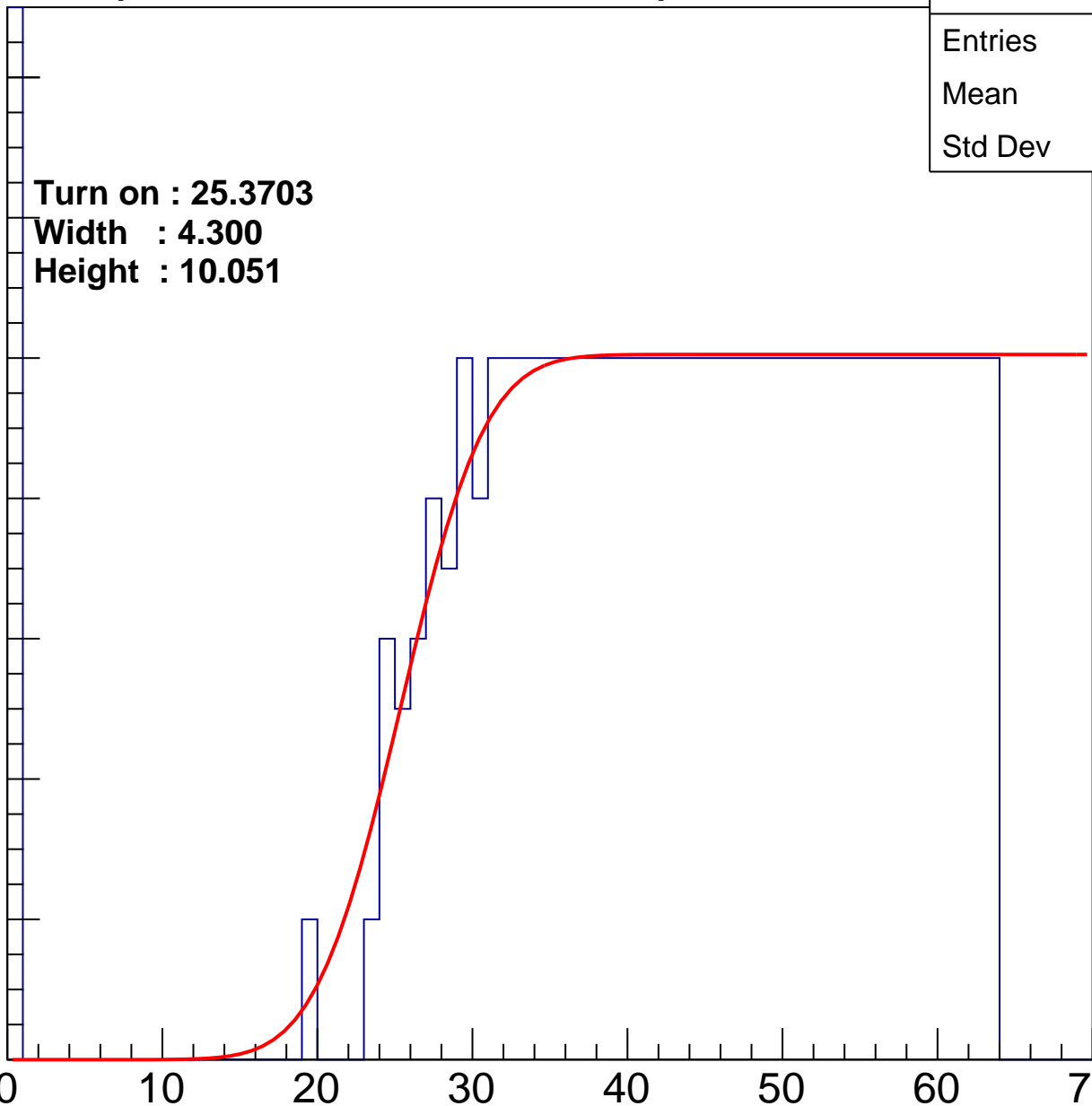
Width : 4.300

Height : 10.051

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch23

calib_packv5_041523_1651.root, FC#0, port C2

Entries	435
Mean	39.09
Std Dev	17.62

Turn on : 25.8745

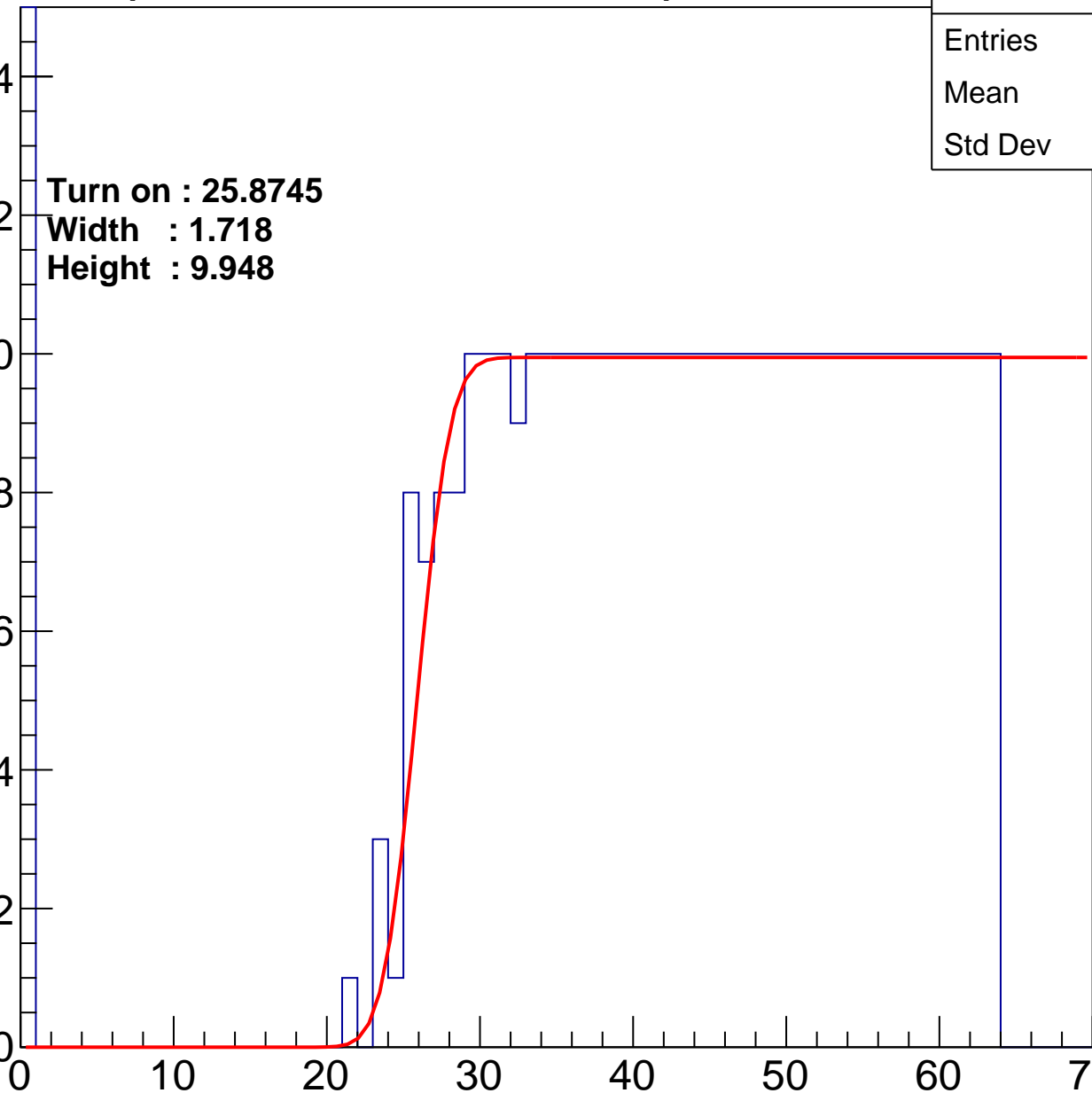
Width : 1.718

Height : 9.948

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch24

calib_packv5_041523_1651.root, FC#0, port C2

Entries	431
Mean	39.16
Std Dev	17.74

Turn on : 26.0012

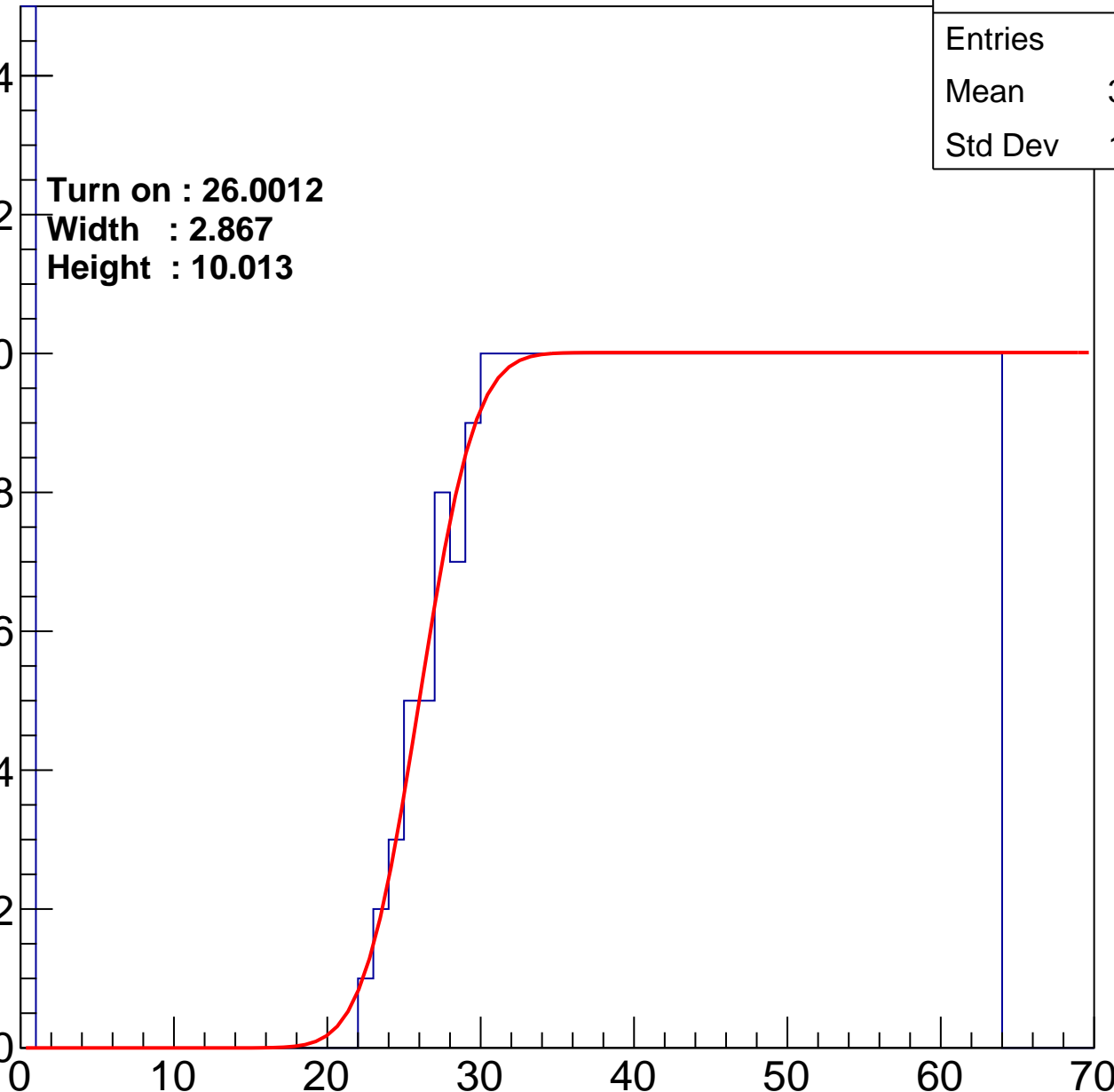
Width : 2.867

Height : 10.013

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch25

calib_packv5_041523_1651.root, FC#0, port C2

Entries	426
Mean	39.67
Std Dev	17.24

Turn on : 26.0177

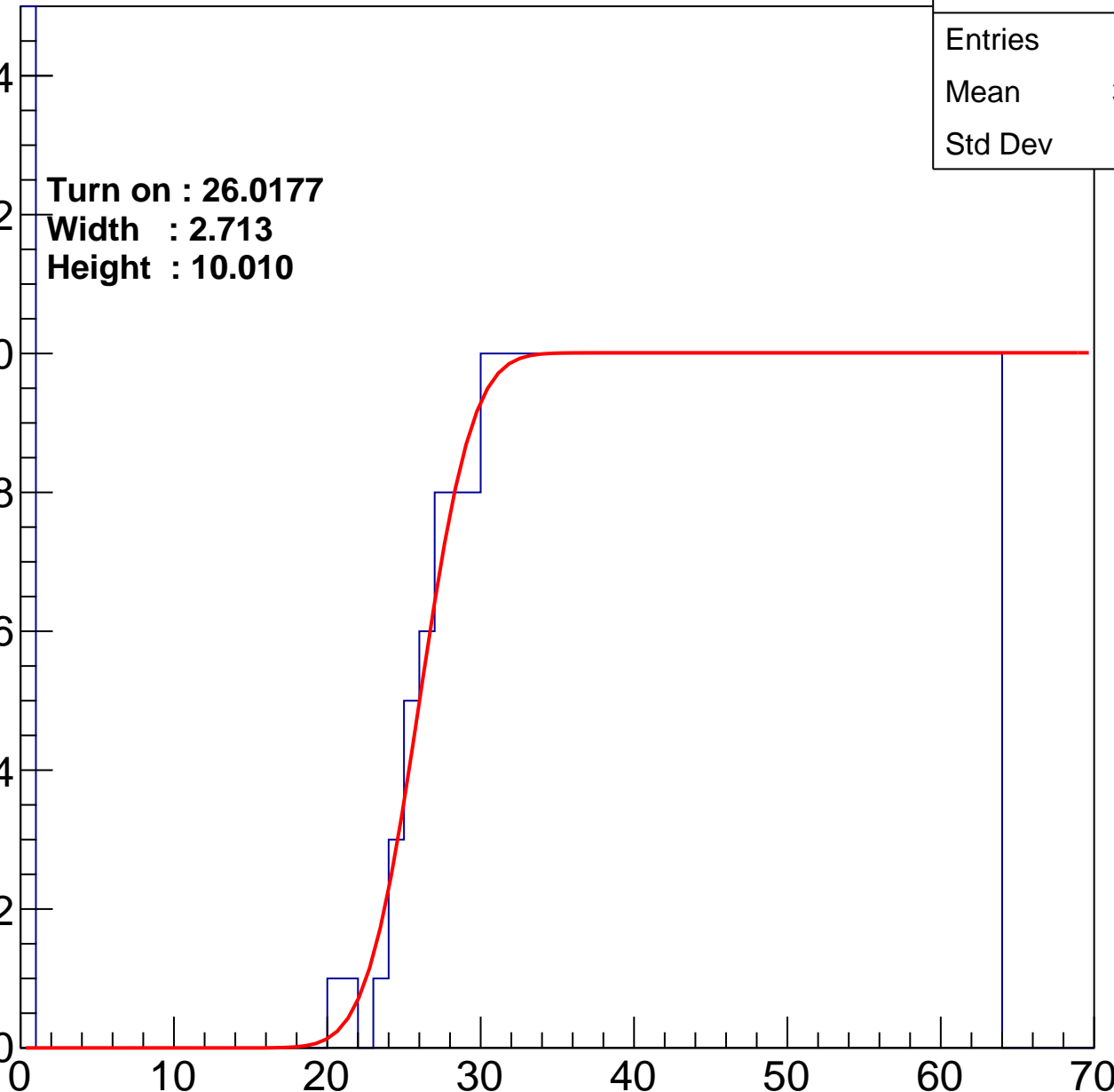
Width : 2.713

Height : 10.010

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch26

calib_packv5_041523_1651.root, FC#0, port C2

Entries	438
Mean	38.72
Std Dev	17.96

Turn on : 25.2741

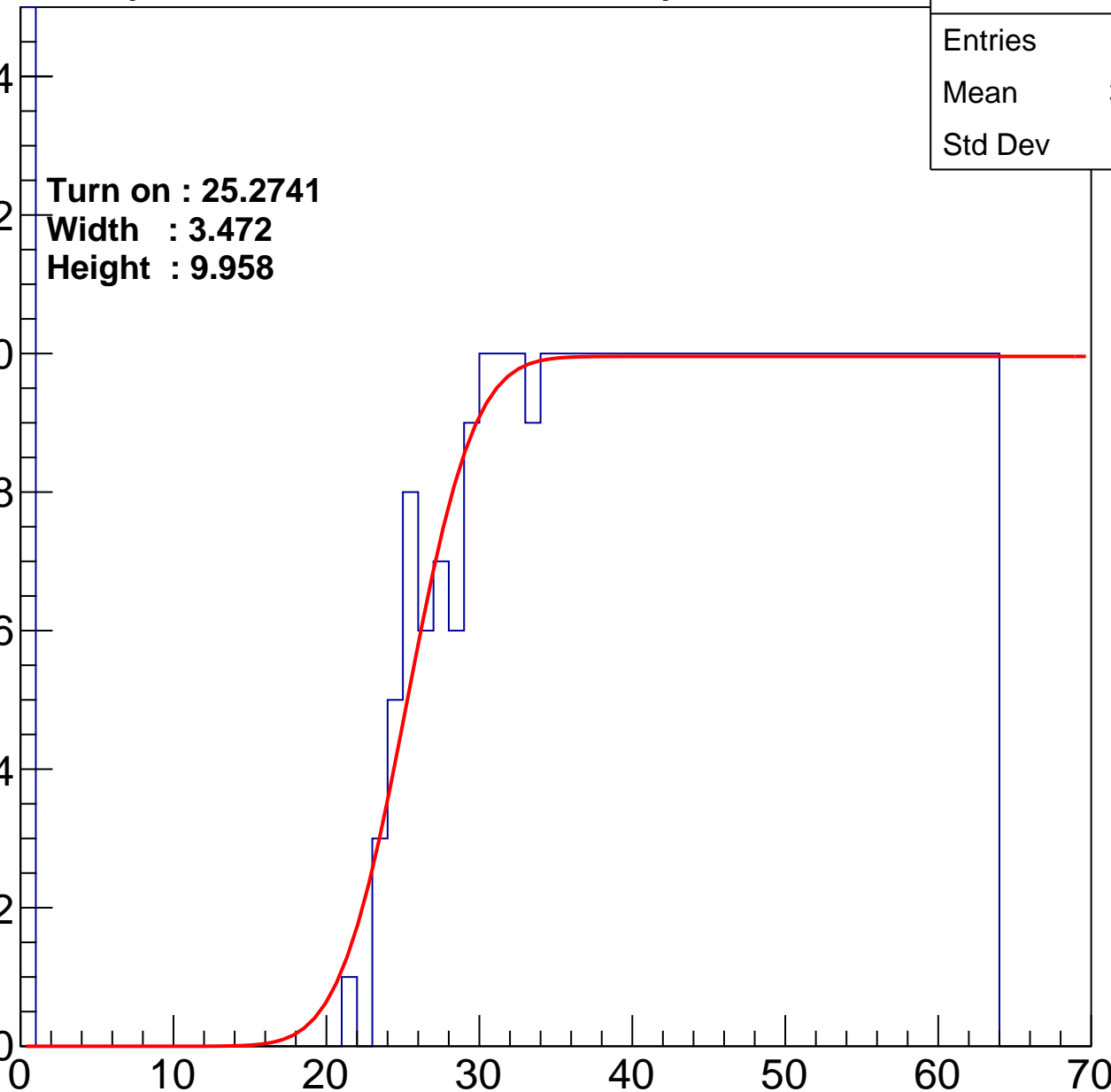
Width : 3.472

Height : 9.958

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch27

calib_packv5_041523_1651.root, FC#0, port C2

Entries	453
Mean	38.53
Std Dev	17.45

Turn on : 23.9510

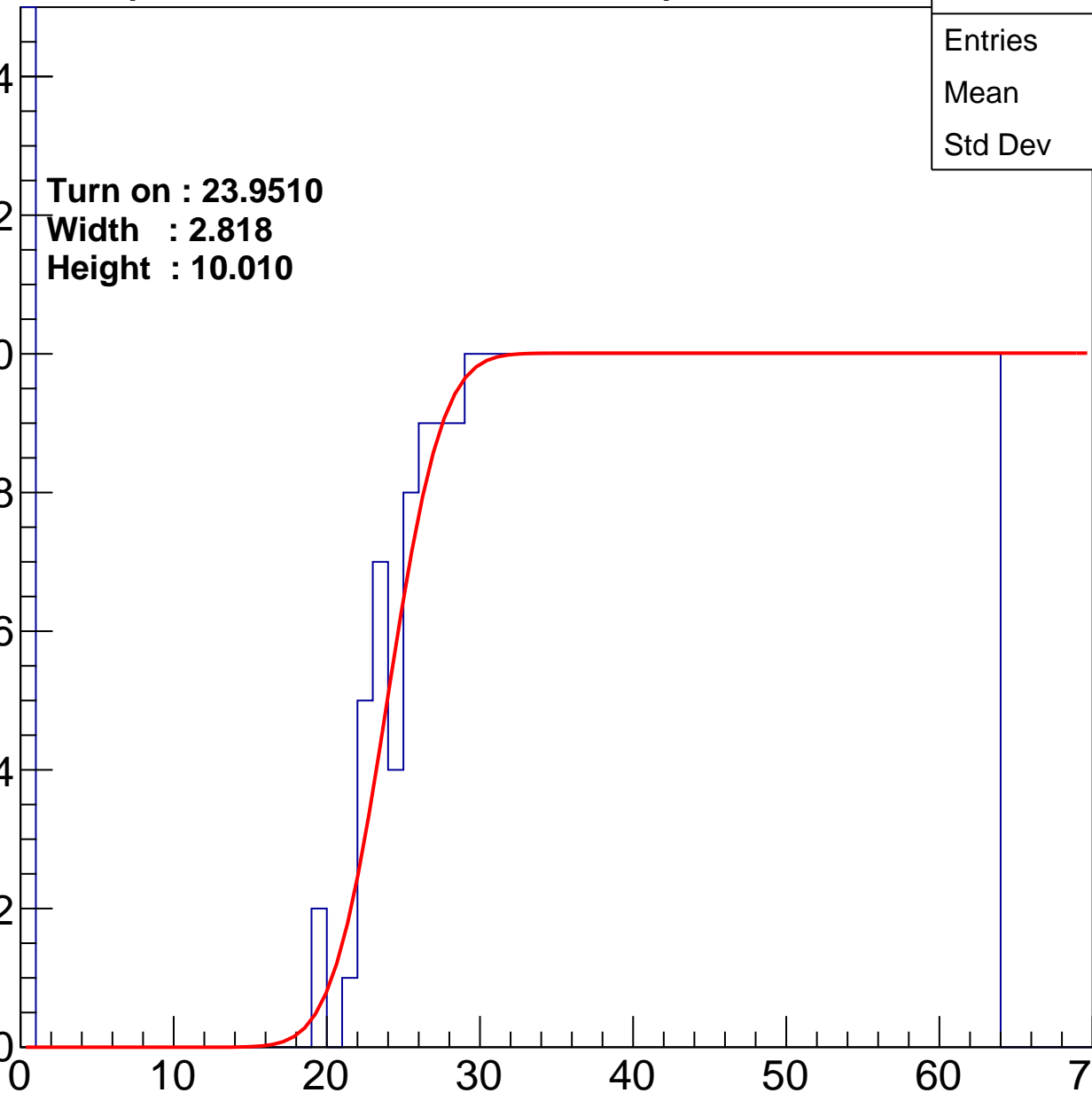
Width : 2.818

Height : 10.010

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch28

calib_packv5_041523_1651.root, FC#0, port C2

Entries	452
Mean	38.8
Std Dev	17.08

Turn on : 24.1711

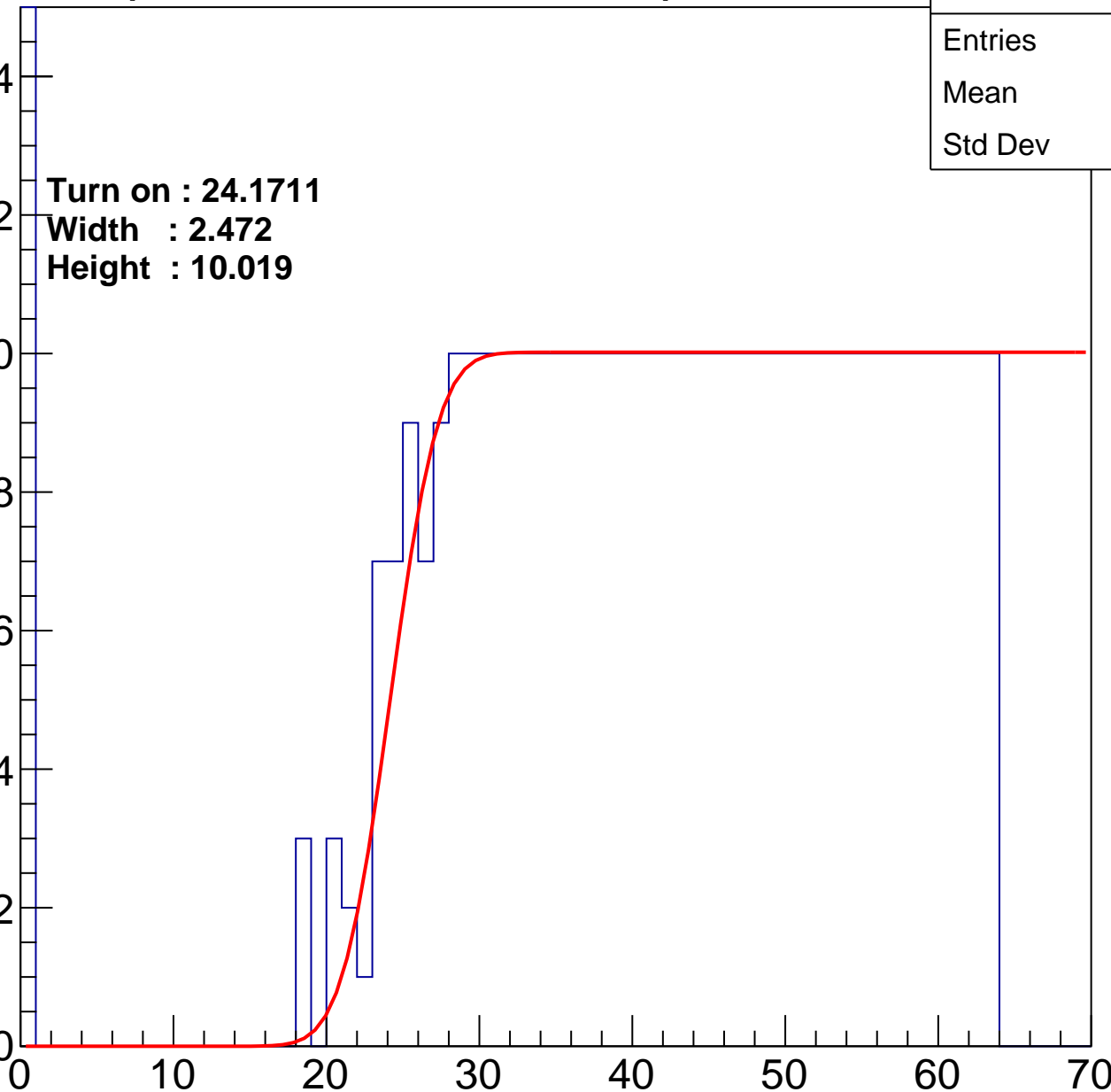
Width : 2.472

Height : 10.019

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch29

calib_packv5_041523_1651.root, FC#0, port C2

Entries	441
Mean	39.01
Std Dev	17.41

Turn on : 24.8053

Width : 2.641

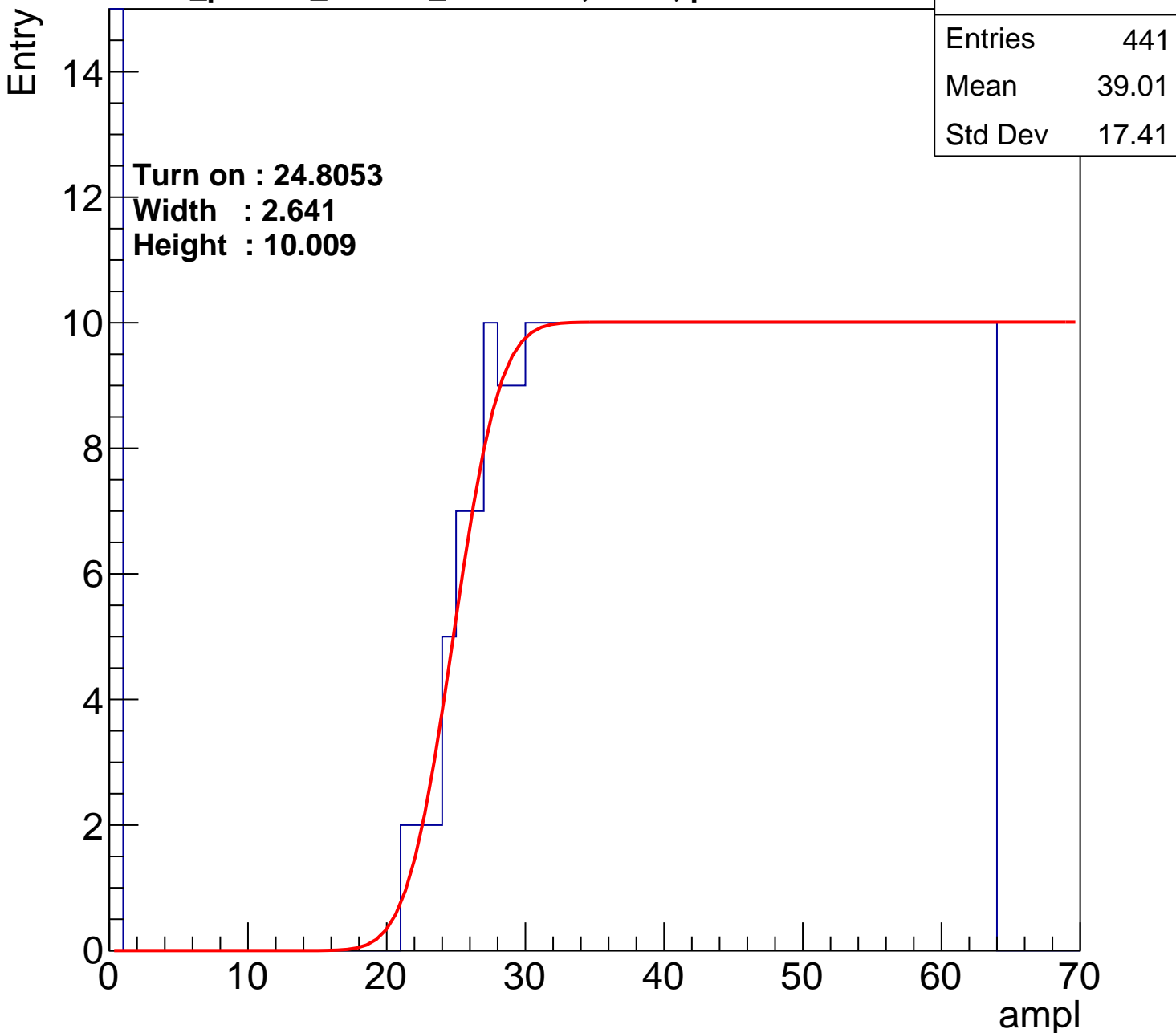
Height : 10.009

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L103S, U5-ch30

calib_packv5_041523_1651.root, FC#0, port C2

Entries	452
Mean	38.47
Std Dev	17.61

Turn on : 24.0202

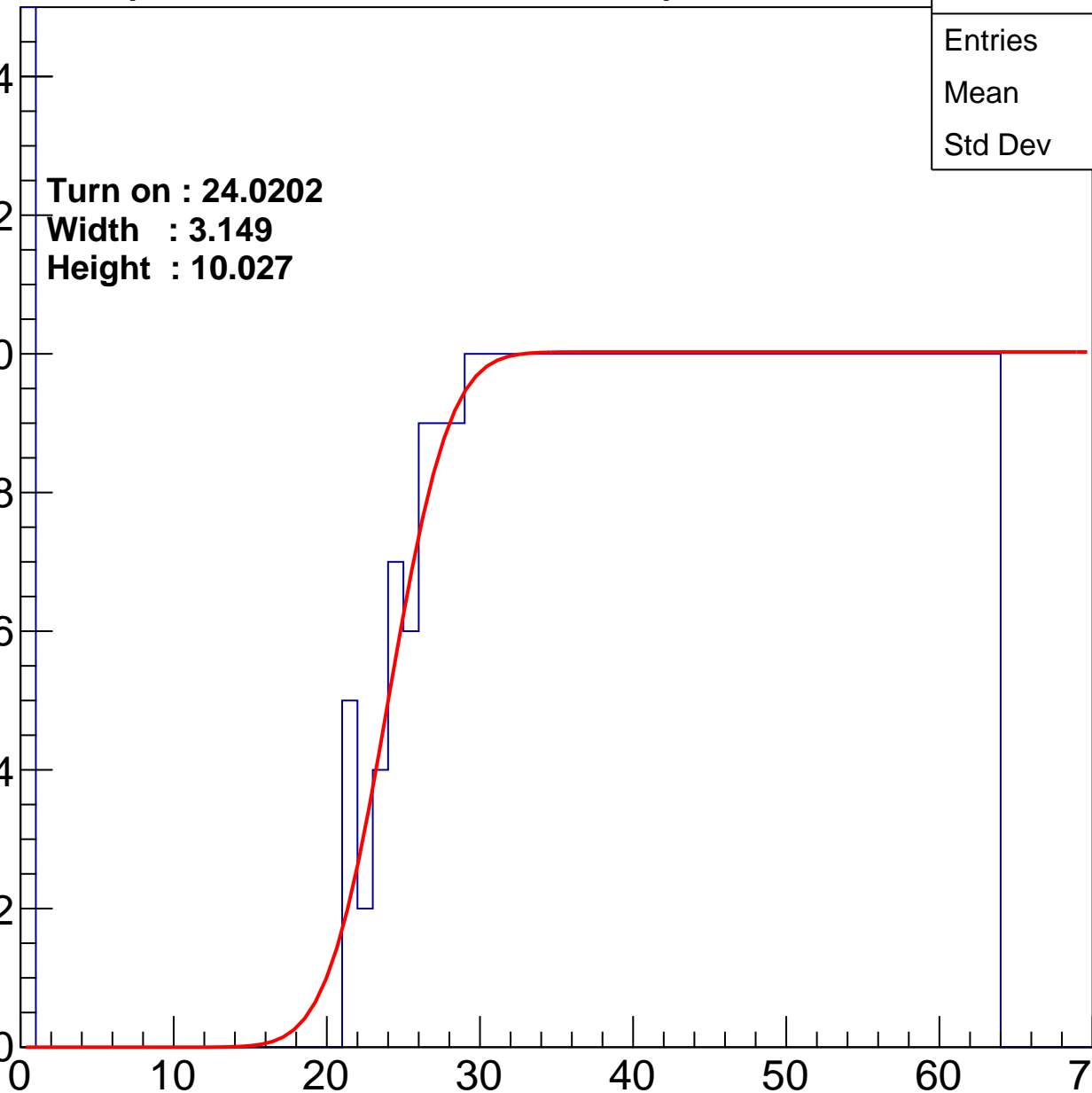
Width : 3.149

Height : 10.027

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch31

calib_packv5_041523_1651.root, FC#0, port C2

Entries	398
Mean	40.86
Std Dev	17.03

Turn on : 28.5524

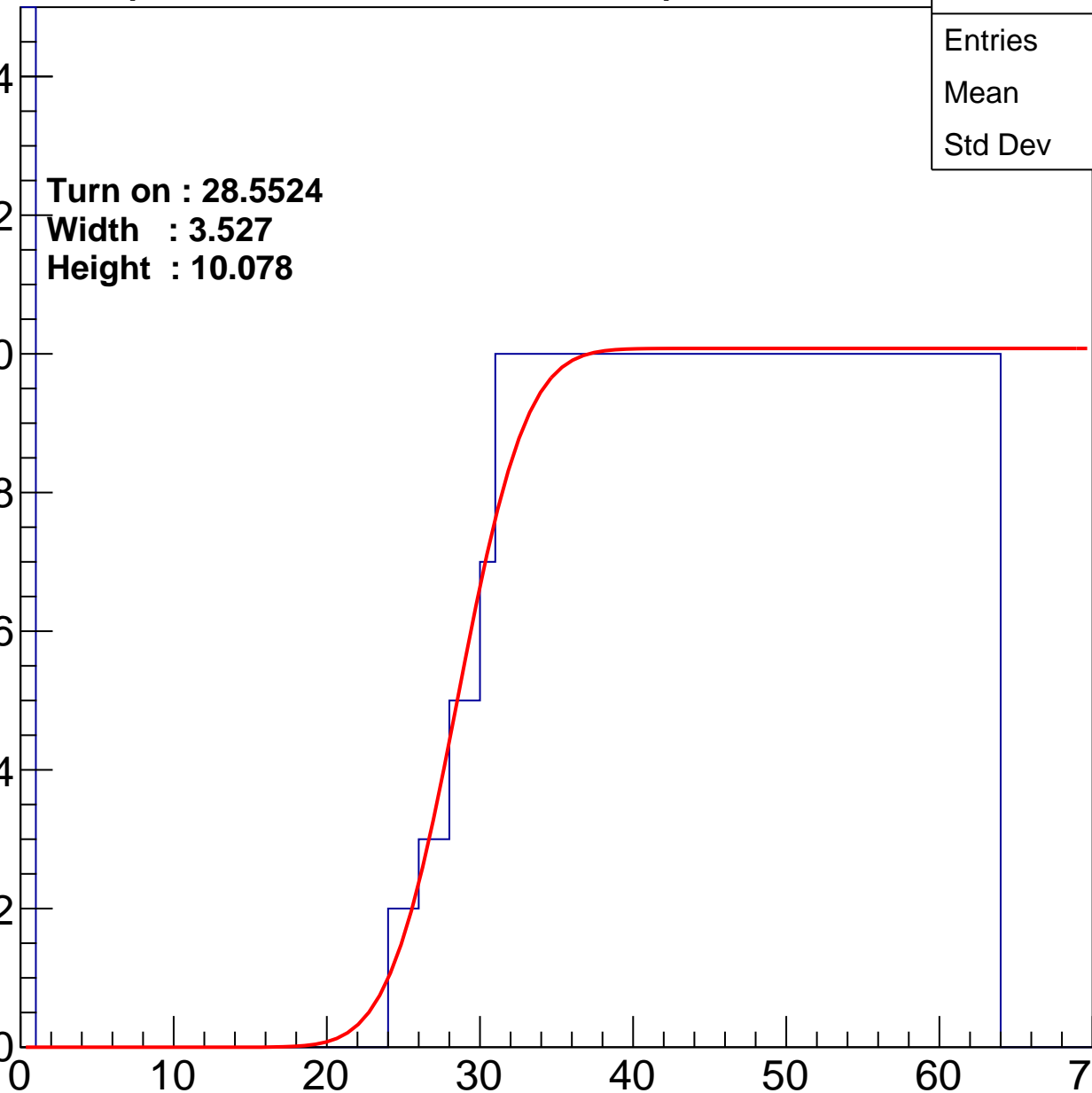
Width : 3.527

Height : 10.078

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch32

calib_packv5_041523_1651.root, FC#0, port C2

Entries	428
Mean	39.4
Std Dev	17.57

Turn on : 26.2006

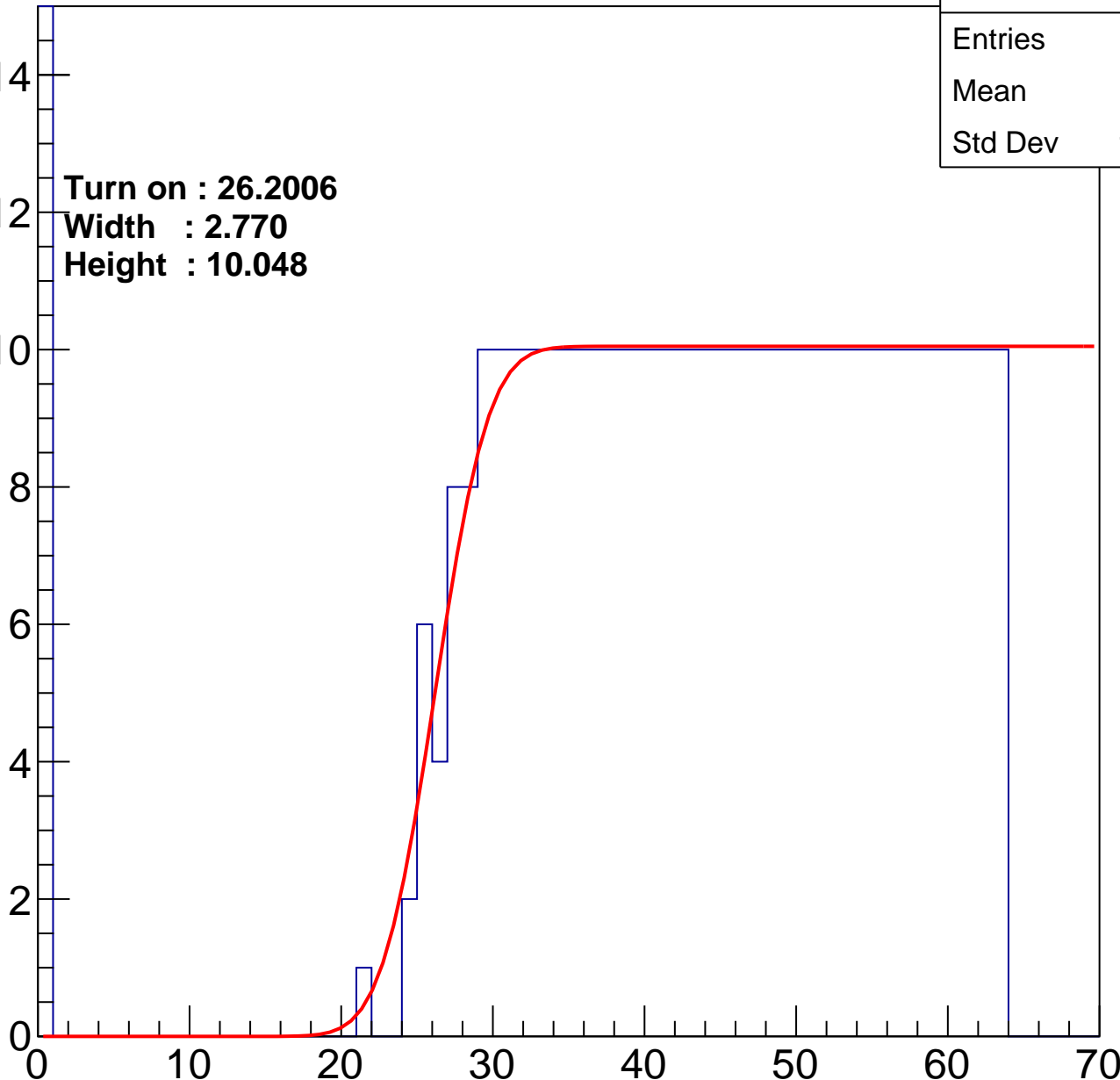
Width : 2.770

Height : 10.048

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch33

calib_packv5_041523_1651.root, FC#0, port C2

Entries	445
Mean	37.72
Std Dev	18.99

Turn on : 26.2701

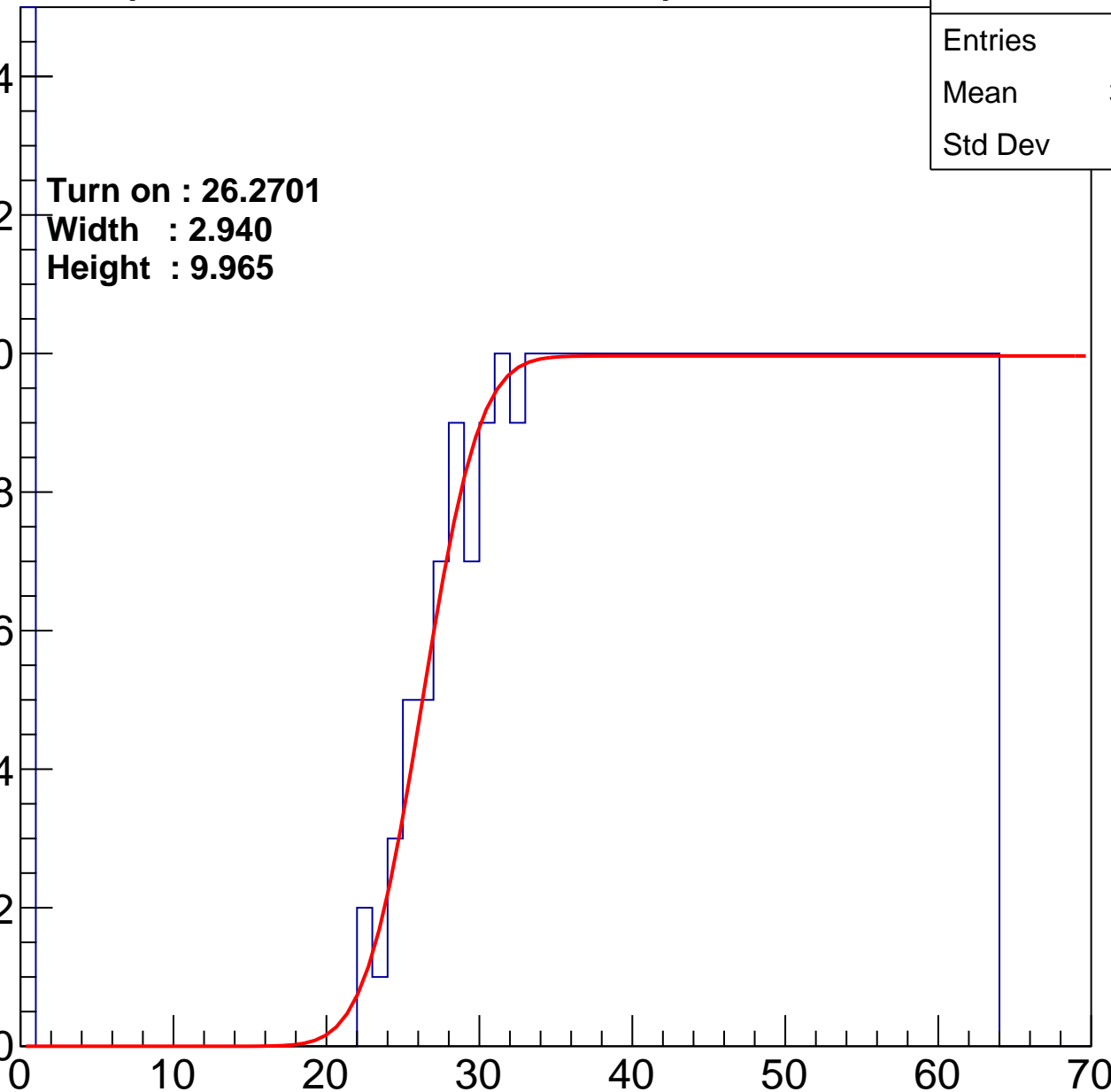
Width : 2.940

Height : 9.965

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch34

calib_packv5_041523_1651.root, FC#0, port C2

Entries	433
Mean	39.13
Std Dev	17.66

Turn on : 25.9760

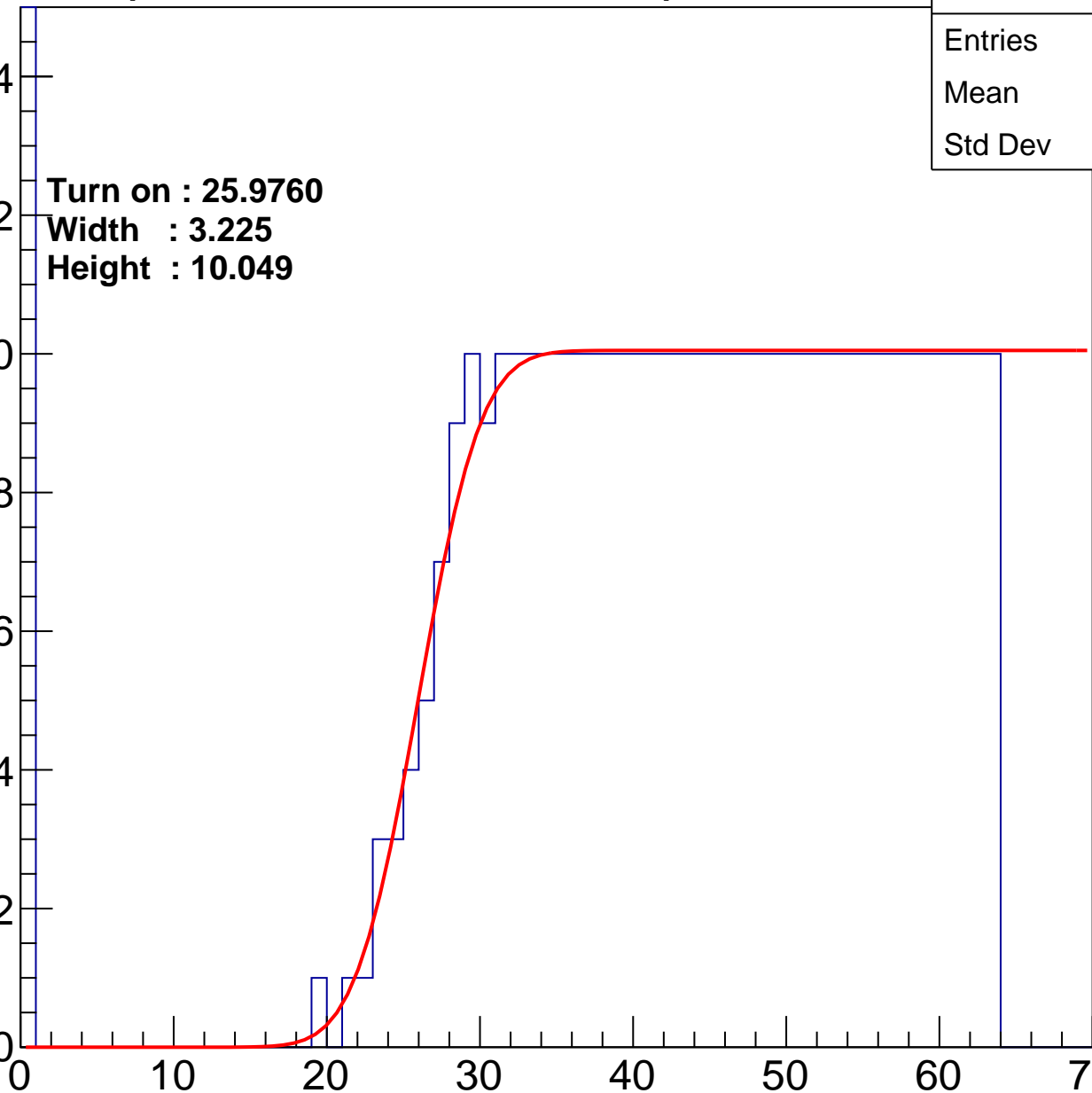
Width : 3.225

Height : 10.049

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch35

calib_packv5_041523_1651.root, FC#0, port C2

Entries	425
Mean	39.62
Std Dev	17.36

Turn on : 25.9853

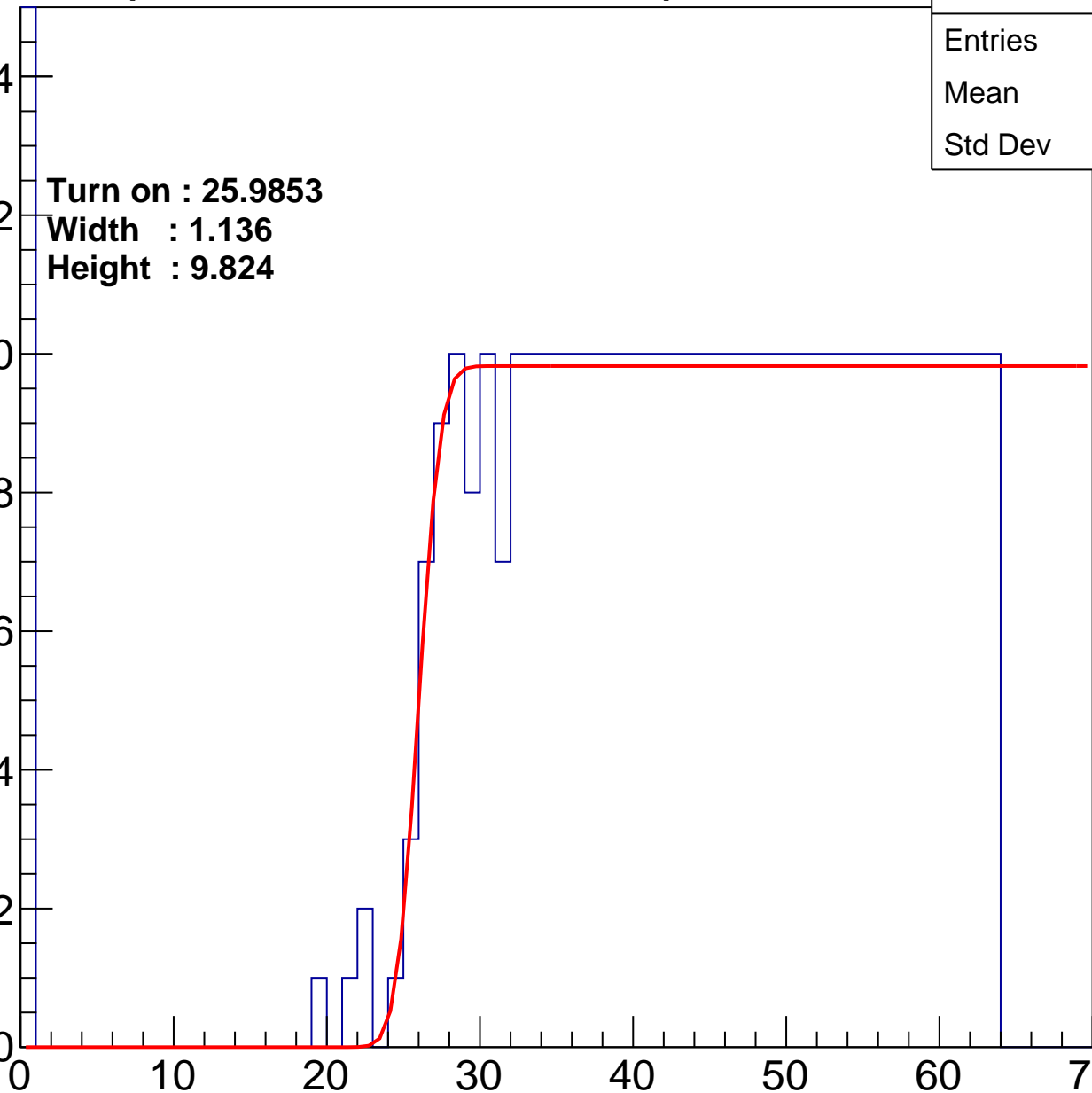
Width : 1.136

Height : 9.824

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch36

calib_packv5_041523_1651.root, FC#0, port C2

Entries	430
Mean	39.79
Std Dev	16.79

Turn on : 25.3800

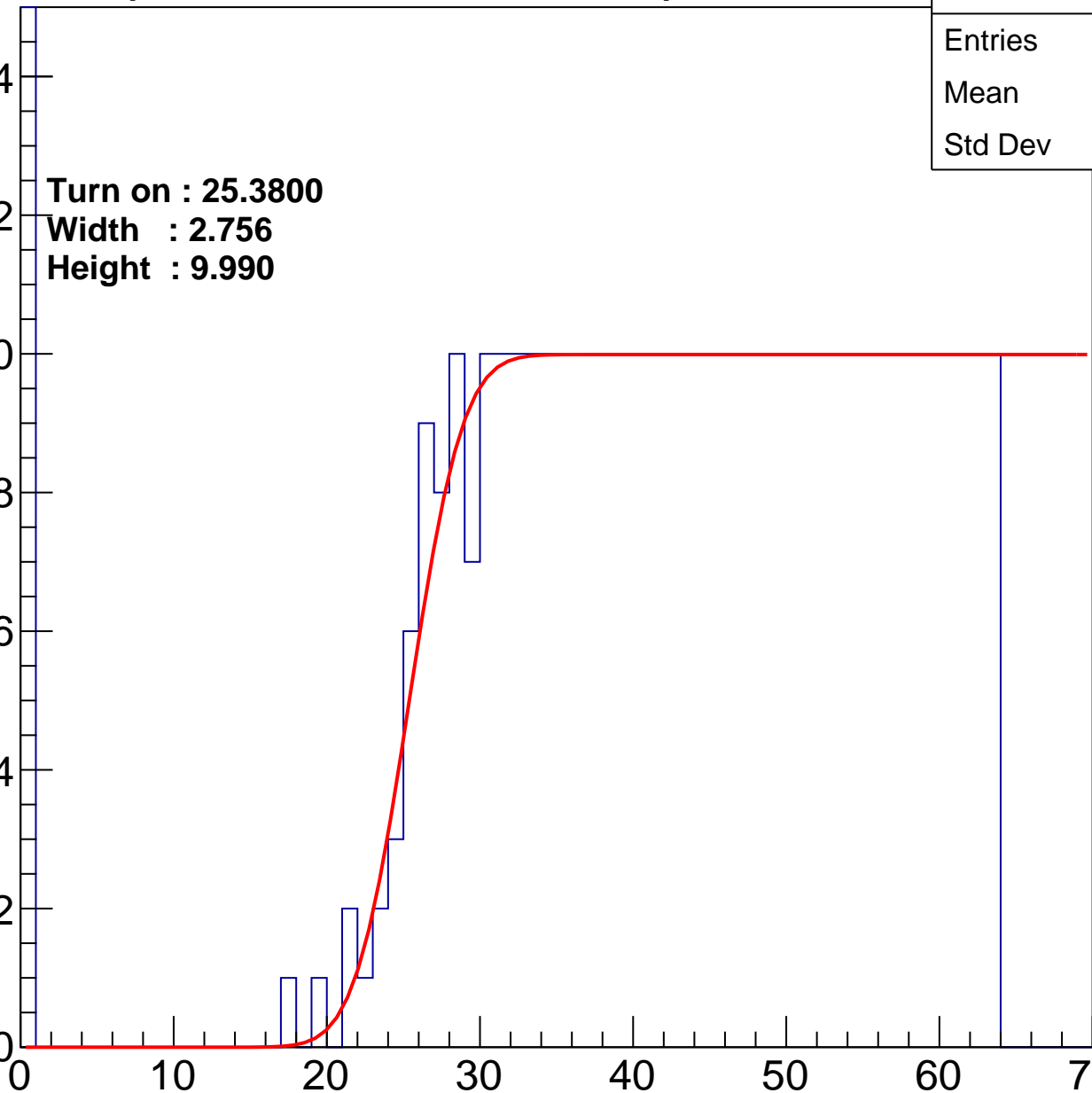
Width : 2.756

Height : 9.990

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch37

calib_packv5_041523_1651.root, FC#0, port C2

Entries	486
Mean	35.88
Std Dev	19.46

Turn on : 23.2545

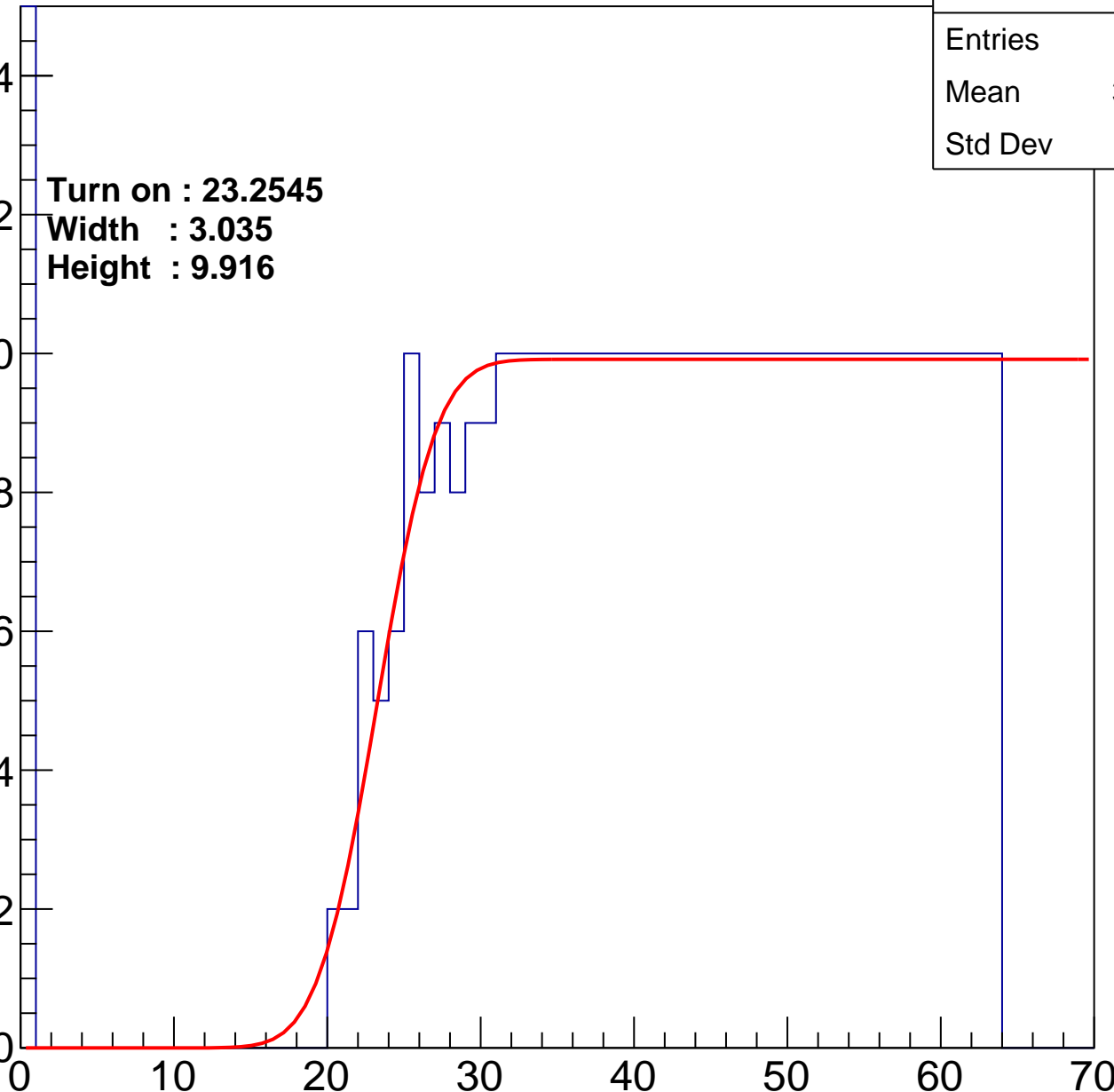
Width : 3.035

Height : 9.916

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch38

calib_packv5_041523_1651.root, FC#0, port C2

Entries	446
Mean	39.07
Std Dev	17.04

Turn on : 24.2036

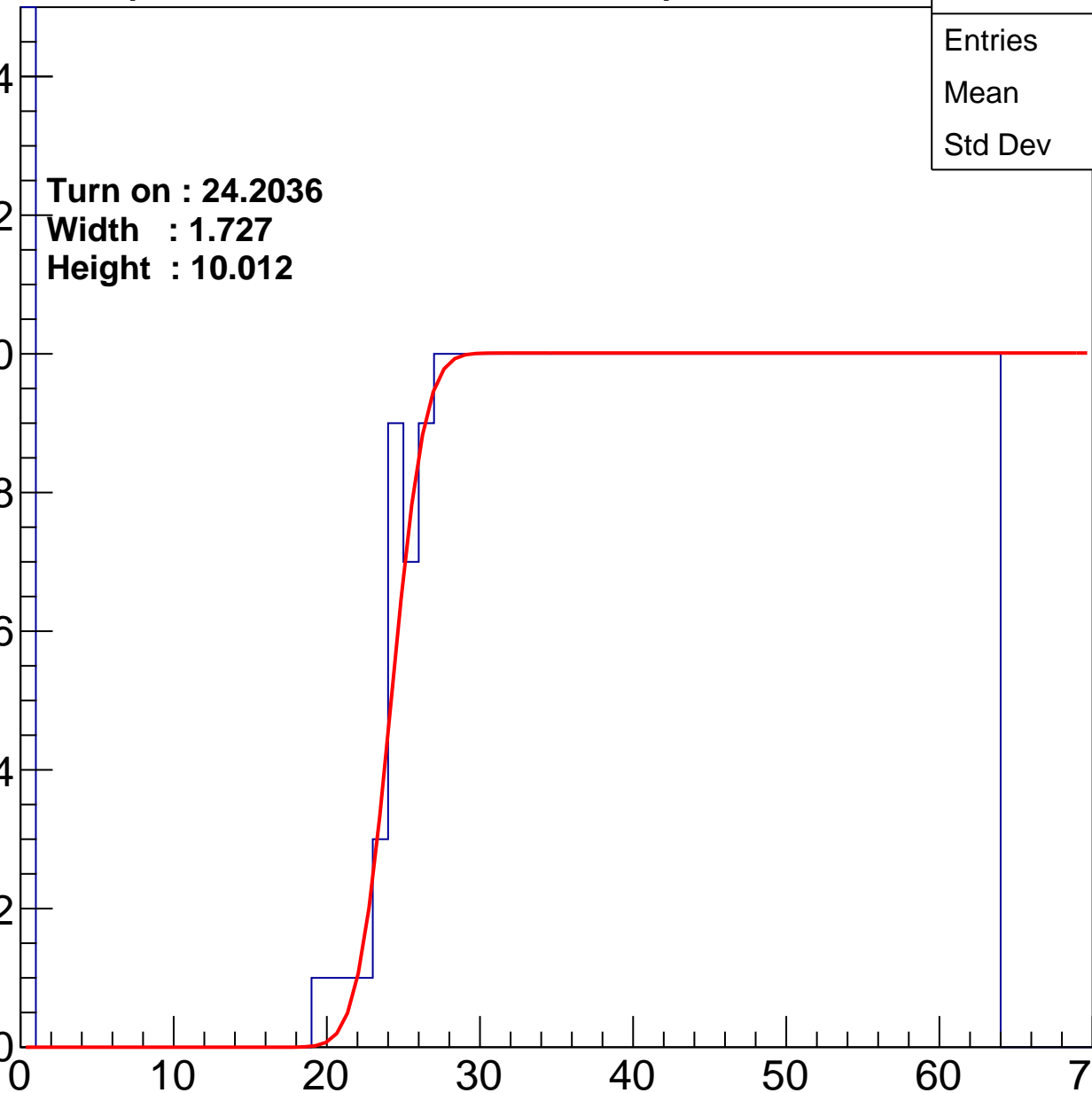
Width : 1.727

Height : 10.012

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch39

calib_packv5_041523_1651.root, FC#0, port C2

Entries	431
Mean	38.72
Std Dev	18.36

Turn on : 27.1731

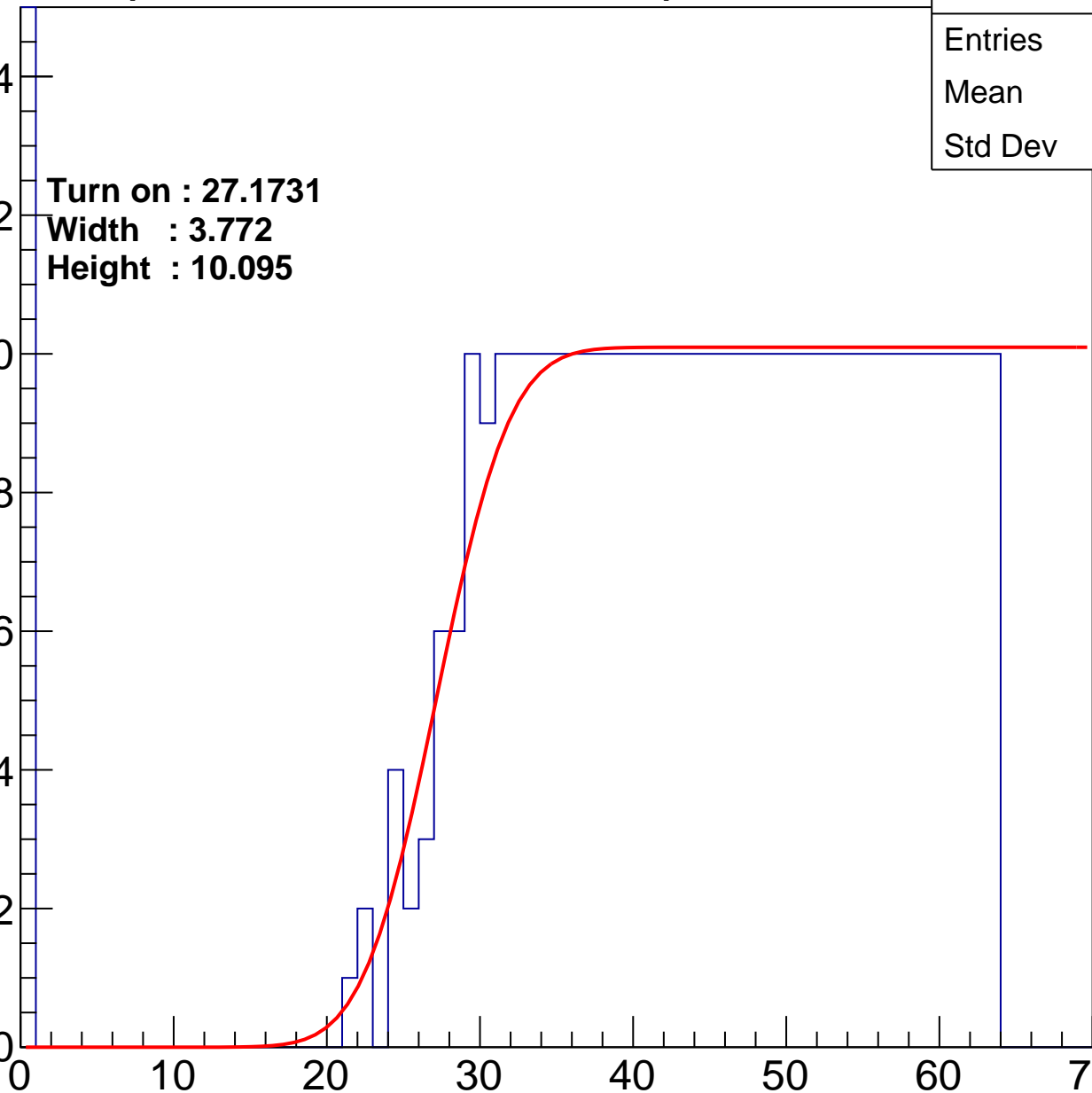
Width : 3.772

Height : 10.095

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch40

calib_packv5_041523_1651.root, FC#0, port C2

Entries	441
Mean	39.24
Std Dev	17.34

Turn on : 25.2939

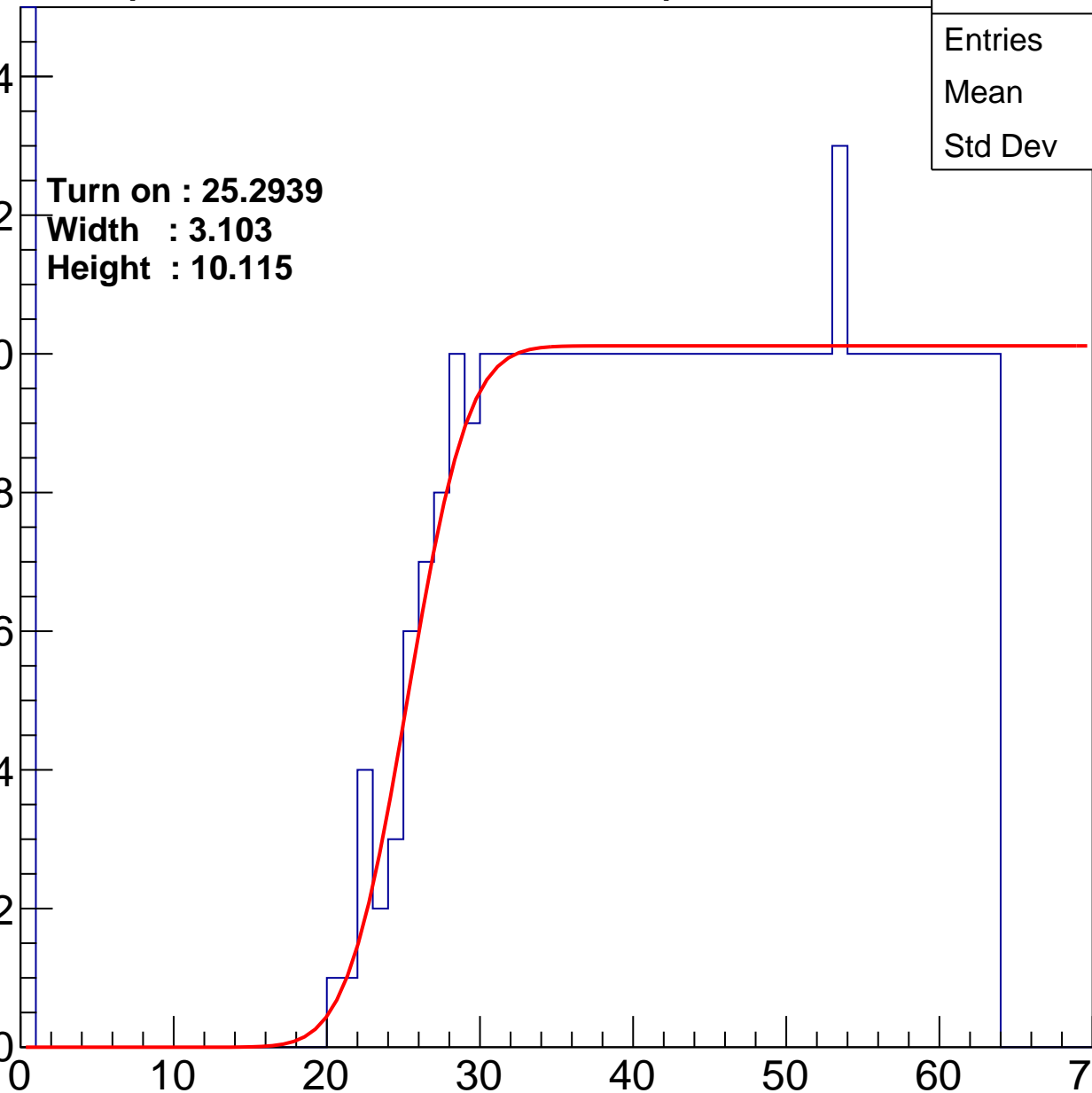
Width : 3.103

Height : 10.115

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch41

calib_packv5_041523_1651.root, FC#0, port C2

Entries	420
Mean	39.5
Std Dev	17.83

Turn on : 26.5919

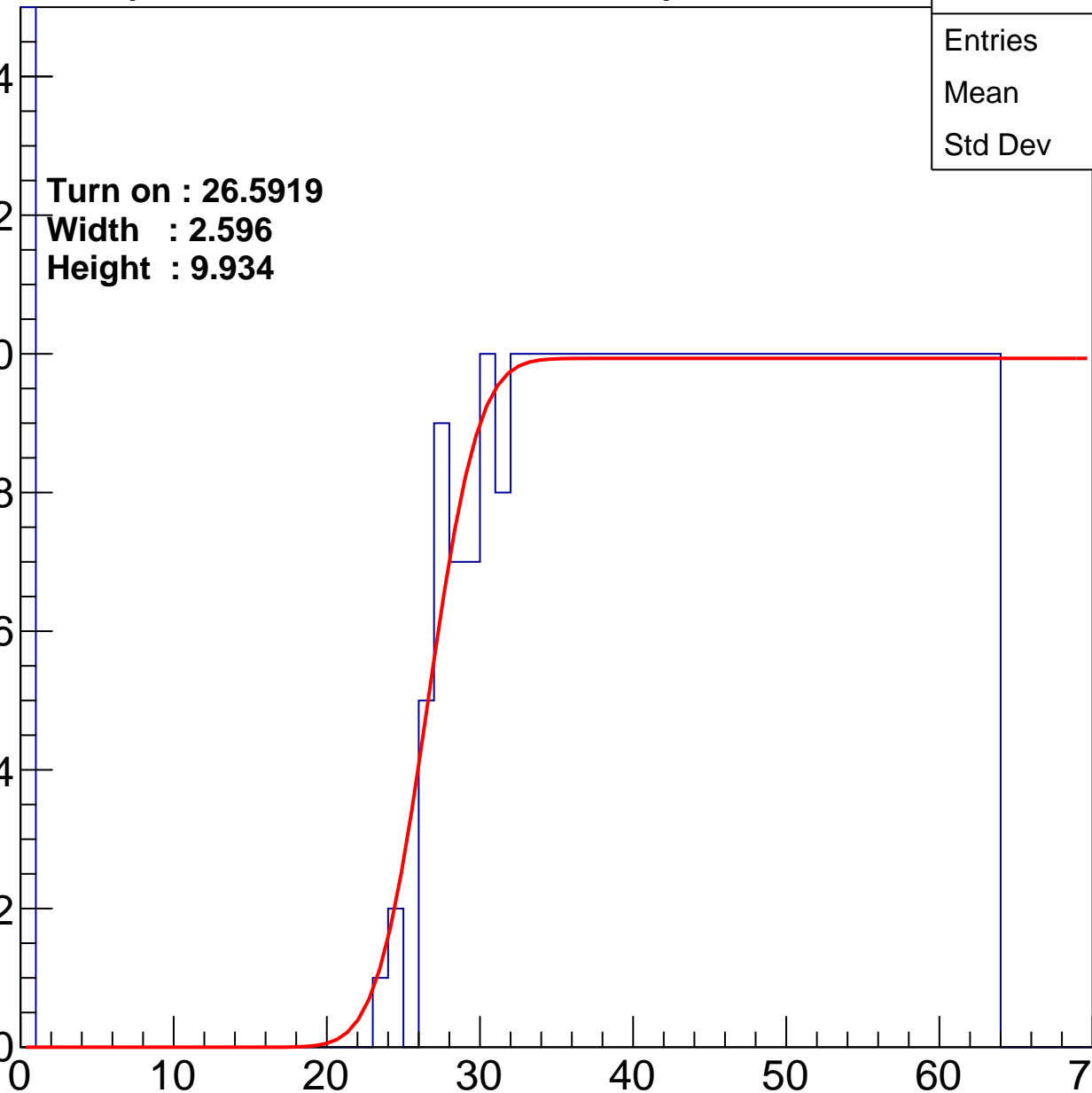
Width : 2.596

Height : 9.934

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch42

calib_packv5_041523_1651.root, FC#0, port C2

Entries	454
Mean	38
Std Dev	18.16

Turn on : 24.4046

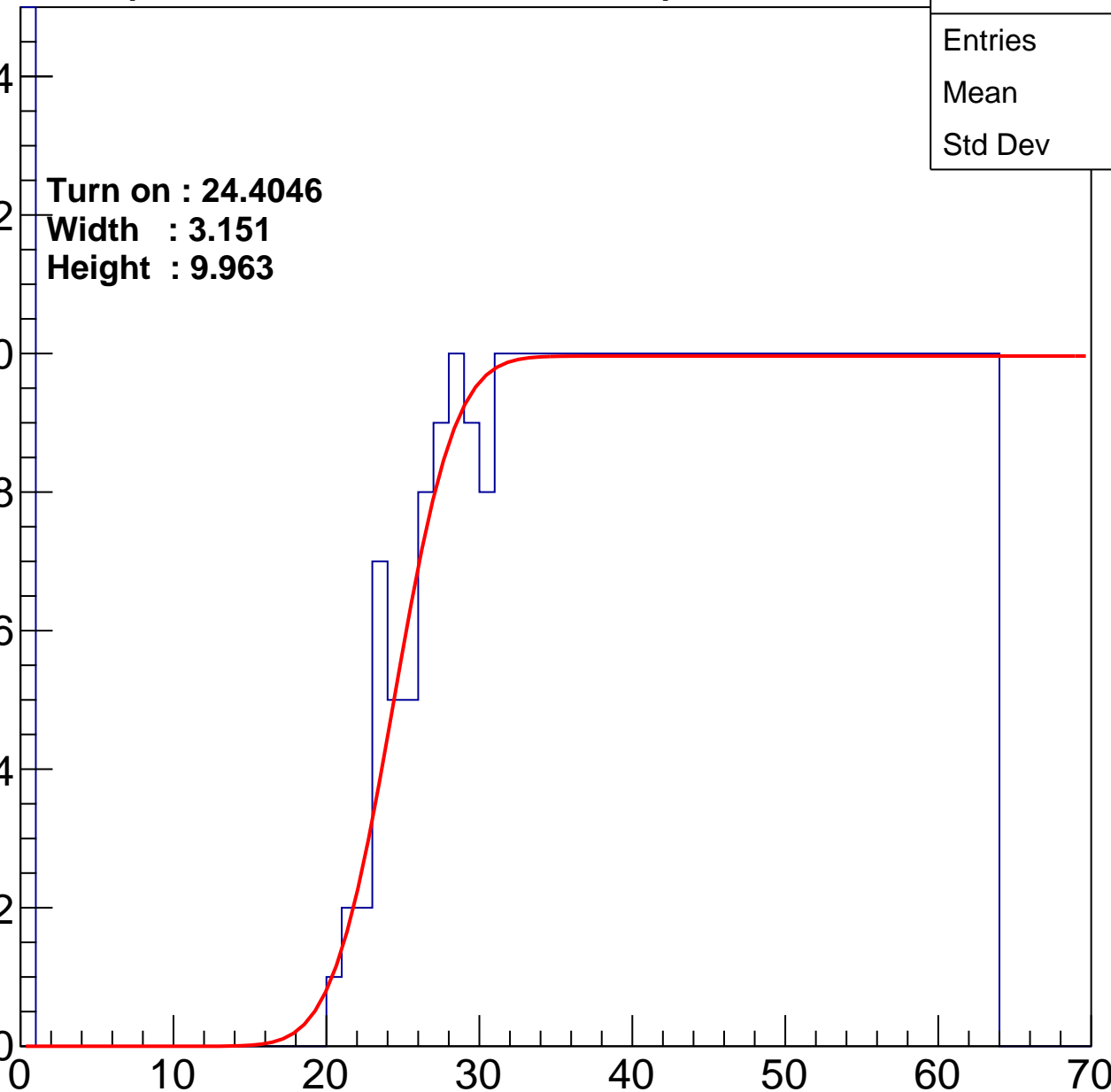
Width : 3.151

Height : 9.963

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch43

calib_packv5_041523_1651.root, FC#0, port C2

Entries	429
Mean	38.99
Std Dev	18.06

Turn on : 27.5238

Width : 3.511

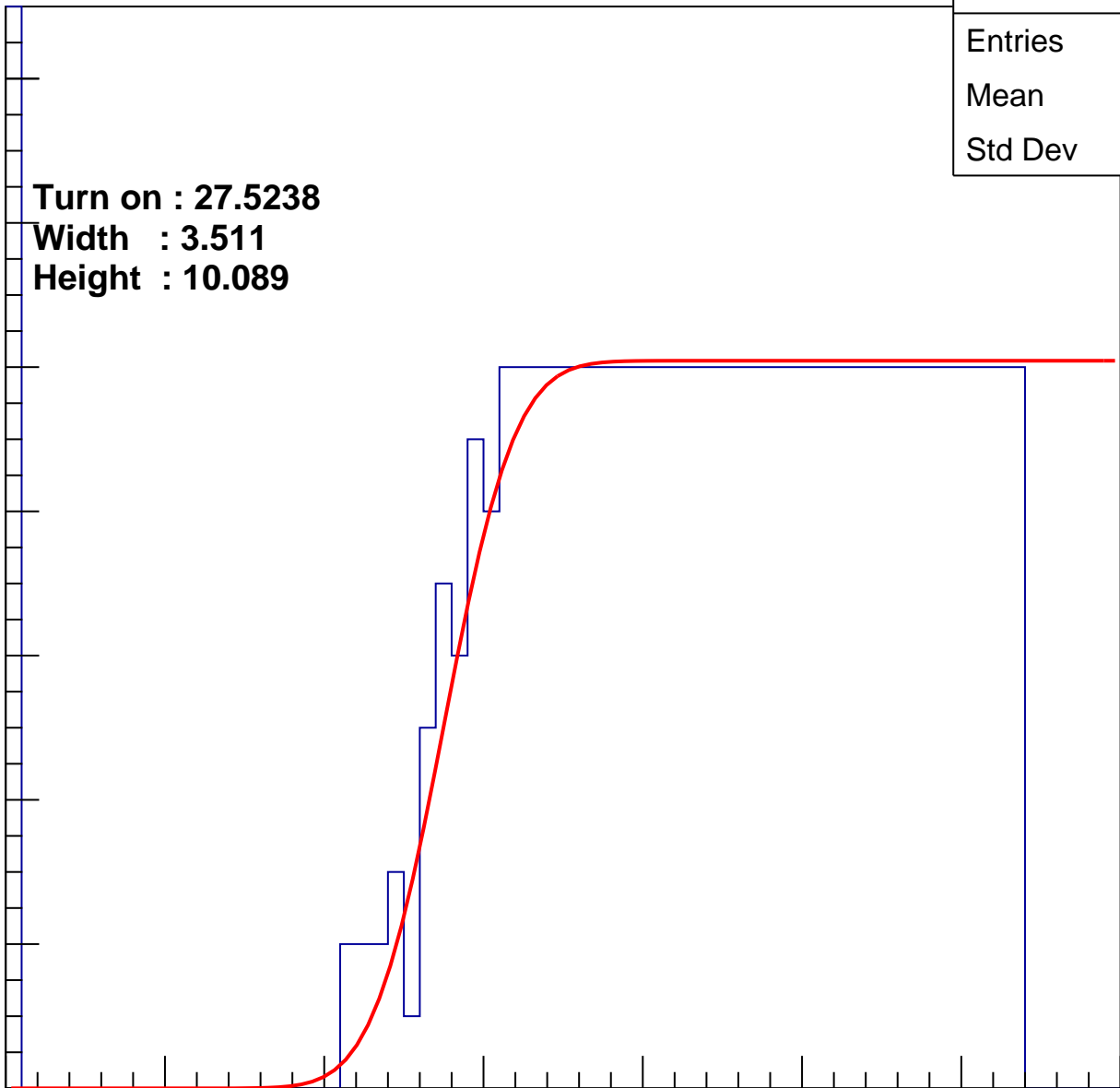
Height : 10.089

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L103S, U5-ch44

calib_packv5_041523_1651.root, FC#0, port C2

Entries	453
Mean	38.9
Std Dev	16.88

Turn on : 23.1024

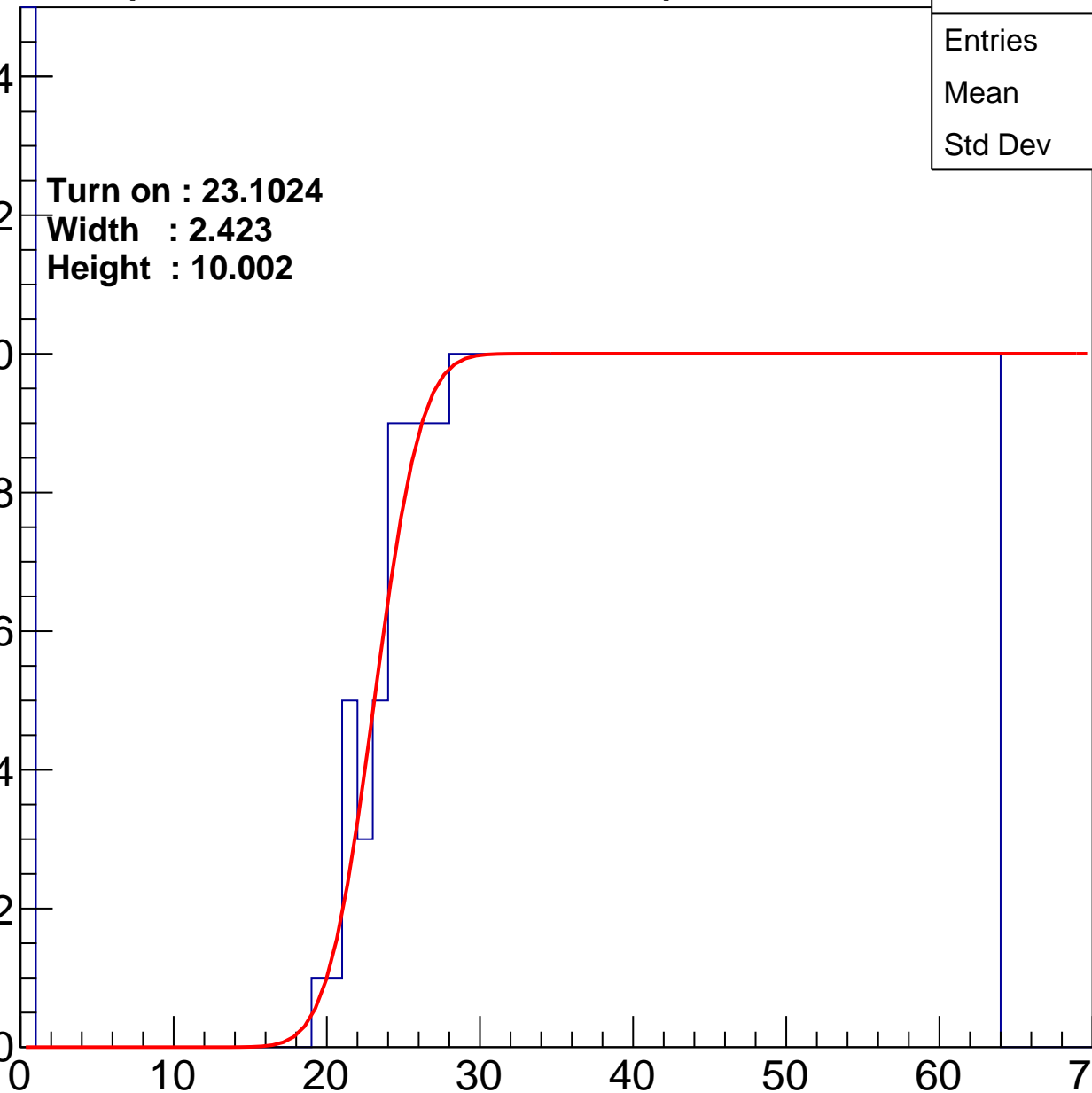
Width : 2.423

Height : 10.002

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch45

calib_packv5_041523_1651.root, FC#0, port C2

Entries	410
Mean	40.19
Std Dev	17.36

Turn on : 27.9435

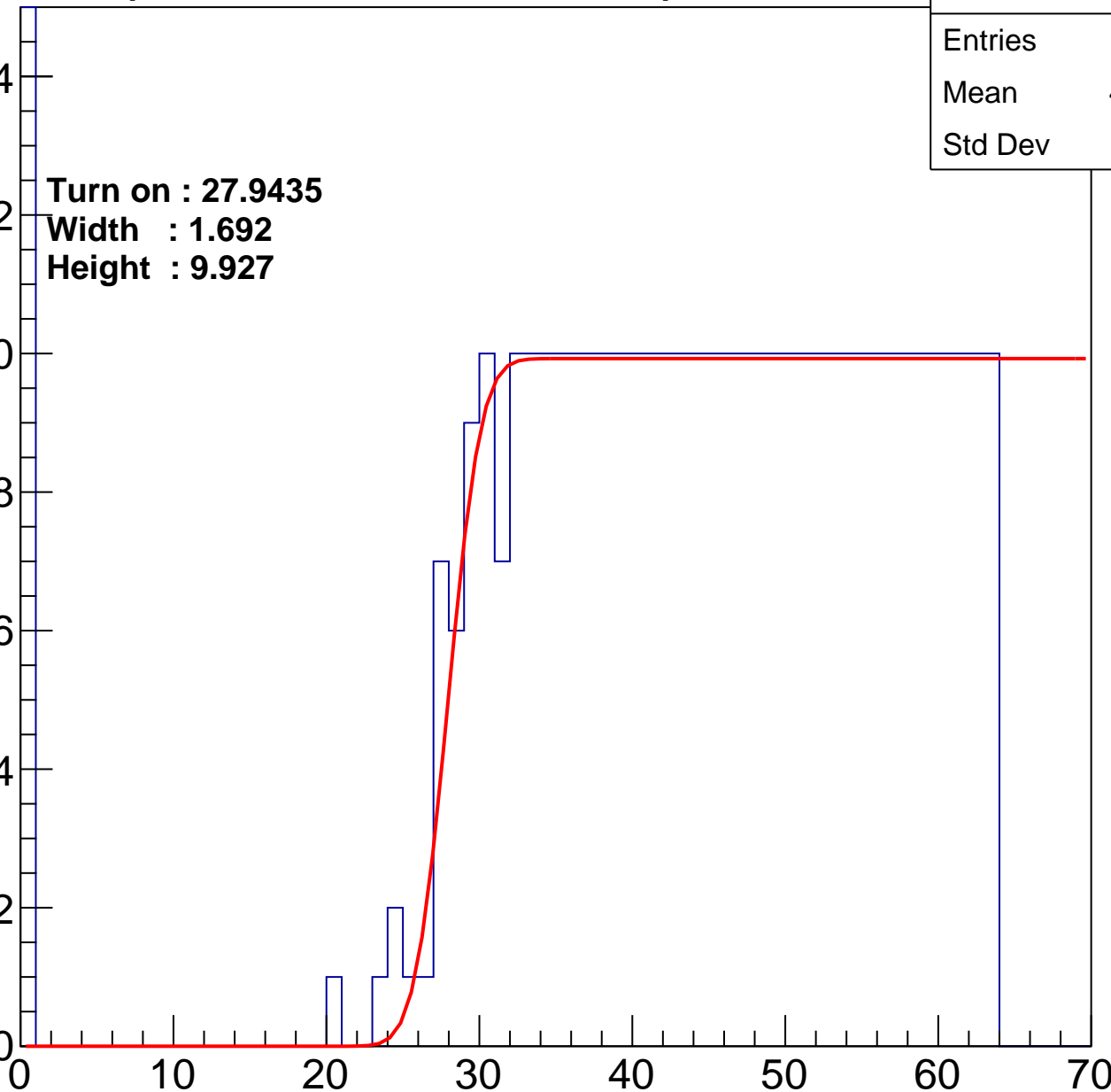
Width : 1.692

Height : 9.927

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch46

calib_packv5_041523_1651.root, FC#0, port C2

Entries	451
Mean	38.87
Std Dev	17.01

Turn on : 23.4789

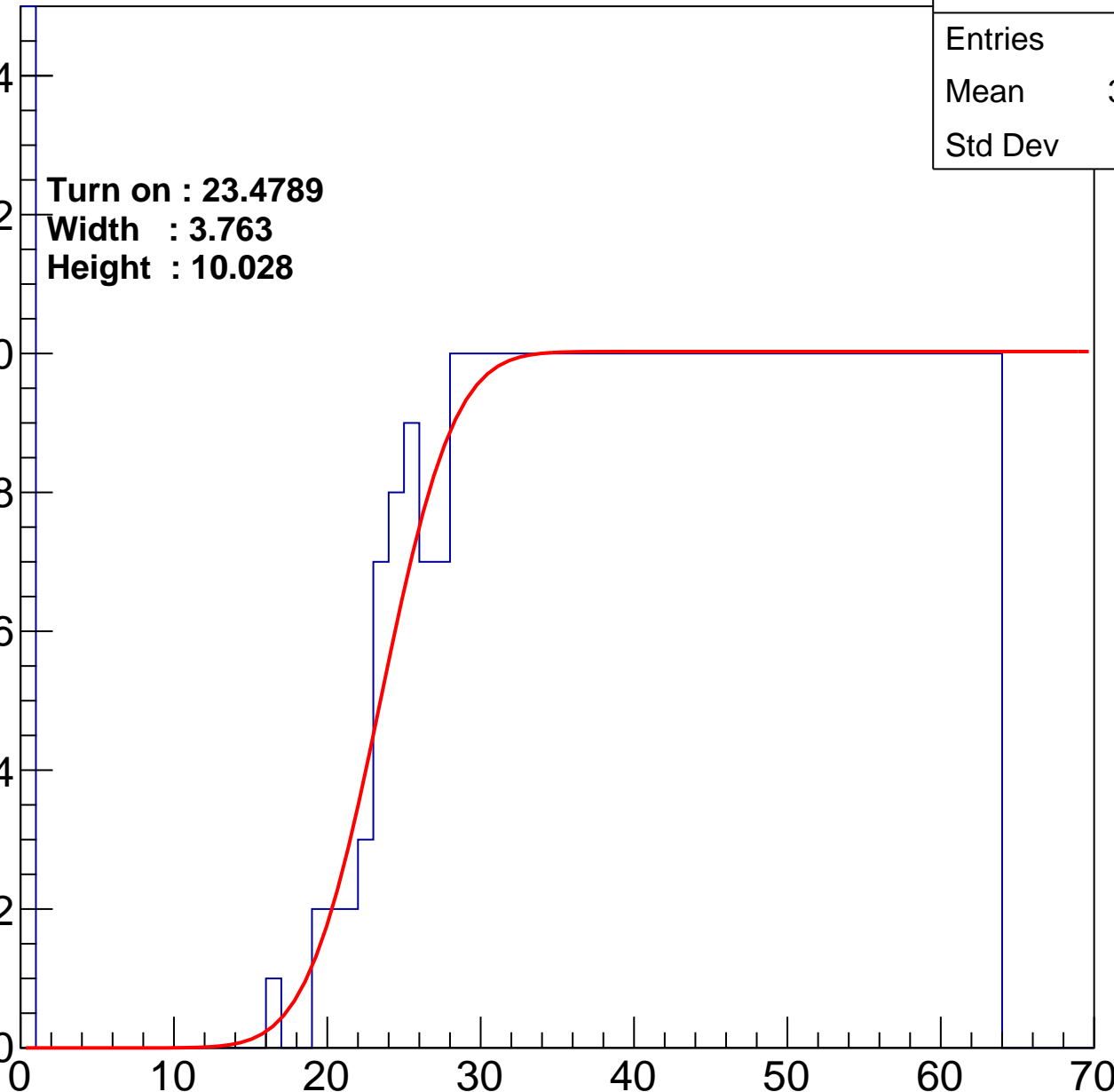
Width : 3.763

Height : 10.028

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch47

calib_packv5_041523_1651.root, FC#0, port C2

Entries	426
Mean	39.12
Std Dev	18.06

Turn on : 27.0288

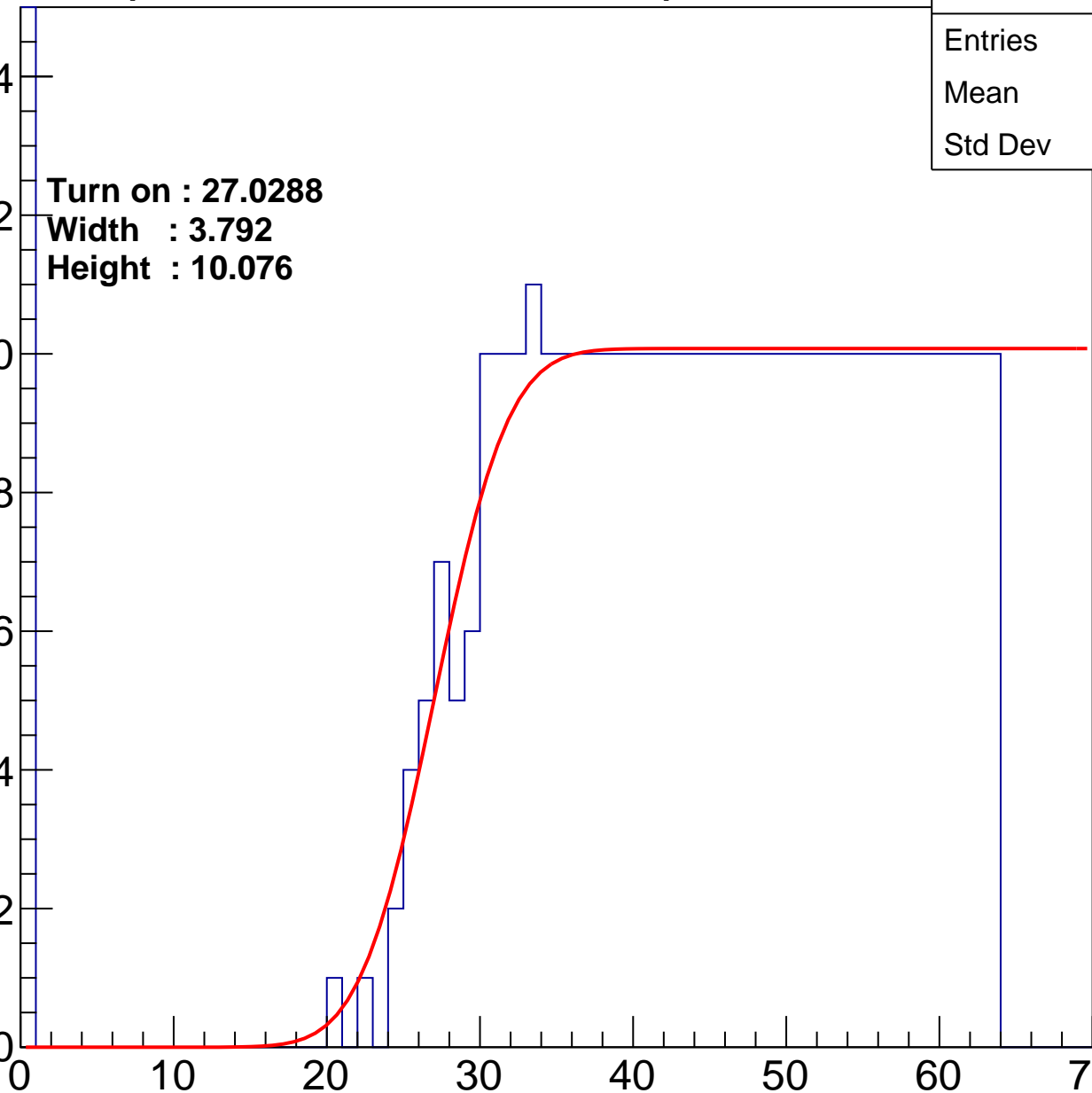
Width : 3.792

Height : 10.076

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch48

calib_packv5_041523_1651.root, FC#0, port C2

Entries	450
Mean	37.71
Std Dev	18.78

Turn on : 25.4151

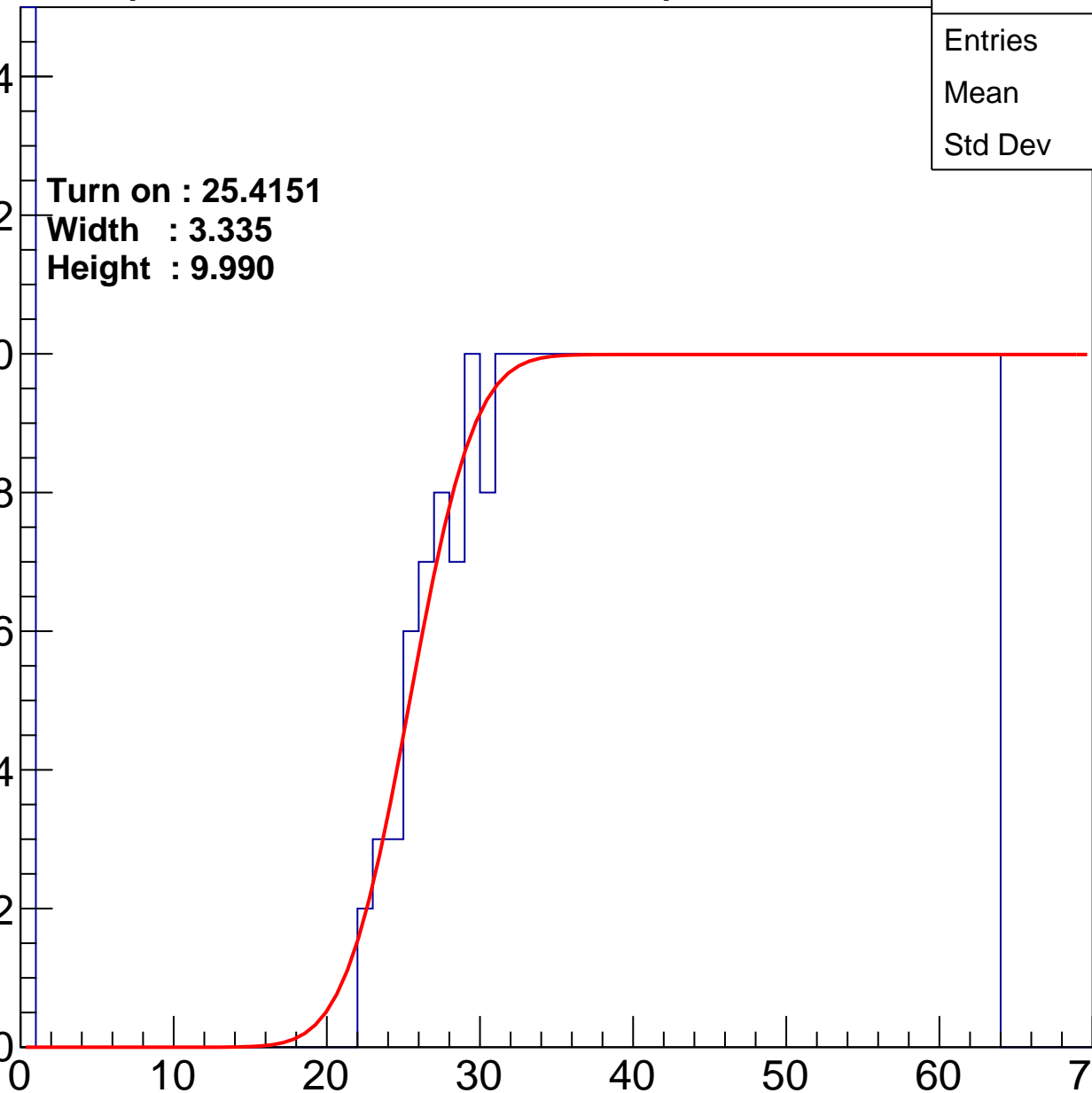
Width : 3.335

Height : 9.990

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch49

calib_packv5_041523_1651.root, FC#0, port C2

Entries	433
Mean	39.13
Std Dev	17.65

Turn on : 26.0276

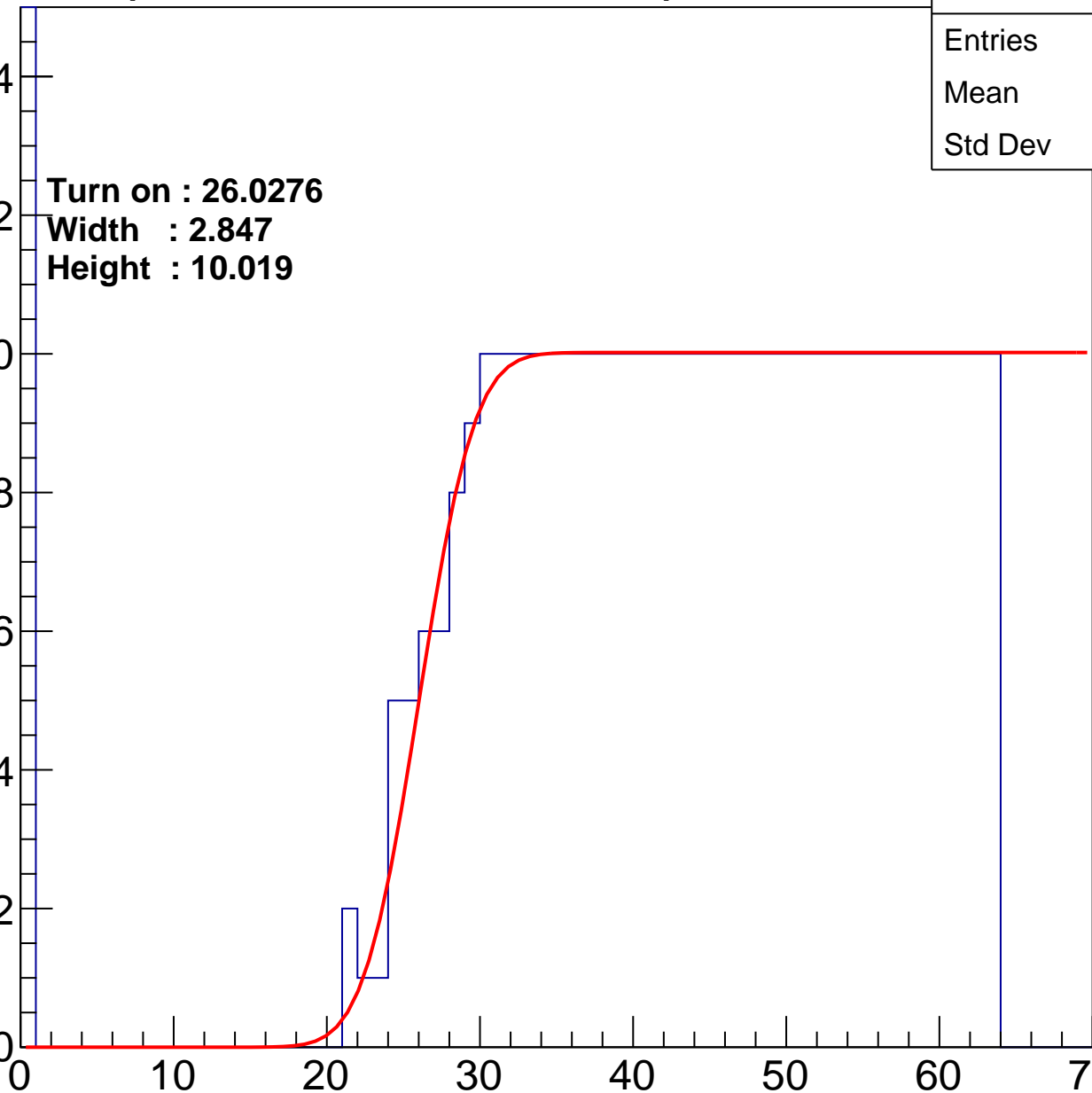
Width : 2.847

Height : 10.019

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch50

calib_packv5_041523_1651.root, FC#0, port C2

Entries	436
Mean	38.83
Std Dev	17.95

Turn on : 25.3200

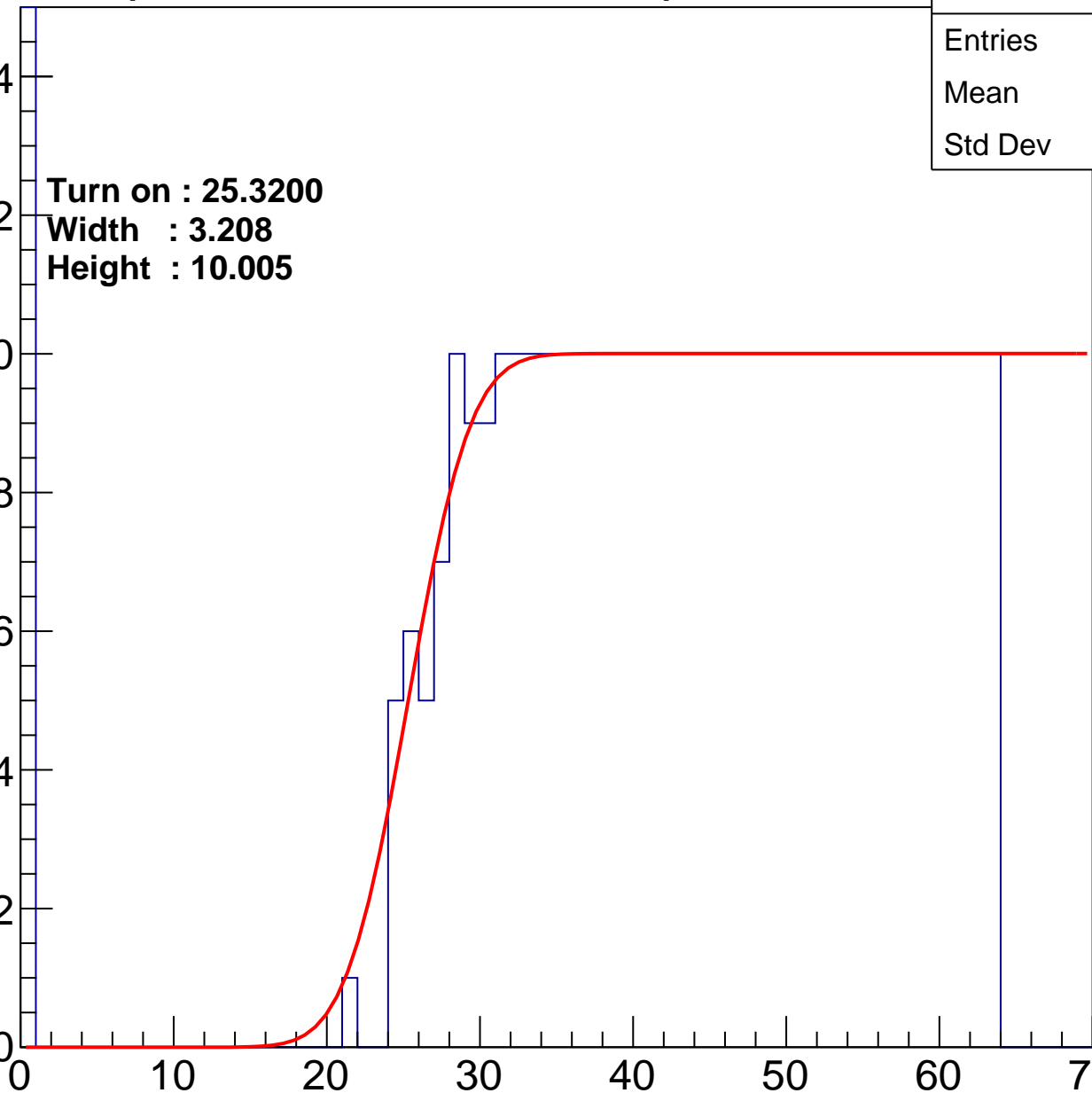
Width : 3.208

Height : 10.005

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch51

calib_packv5_041523_1651.root, FC#0, port C2

Entries	421
Mean	39.29
Std Dev	18.05

Turn on : 27.2695

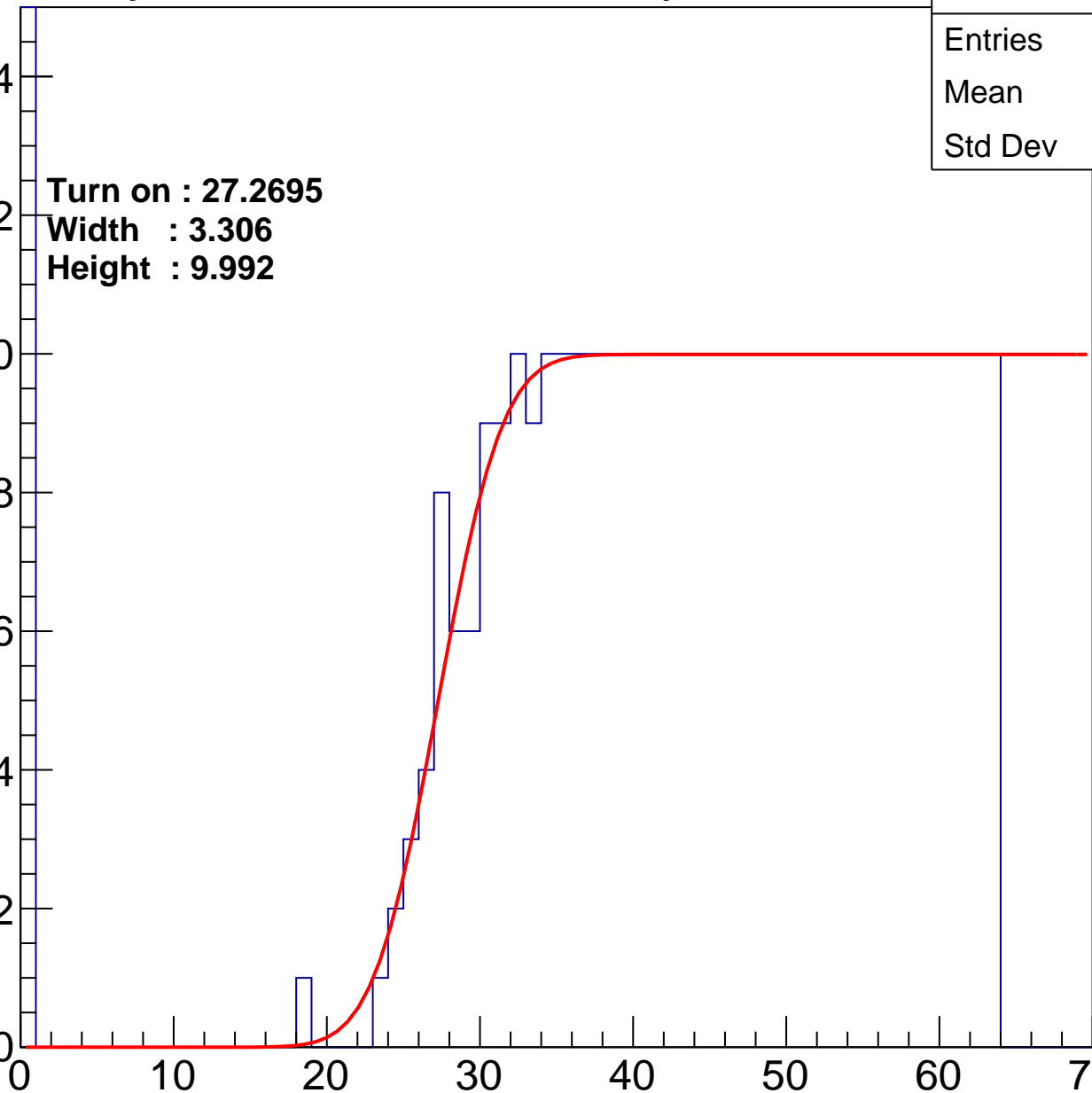
Width : 3.306

Height : 9.992

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch52

calib_packv5_041523_1651.root, FC#0, port C2

Entries	436
Mean	38.92
Std Dev	17.81

Turn on : 25.9205

Width : 2.728

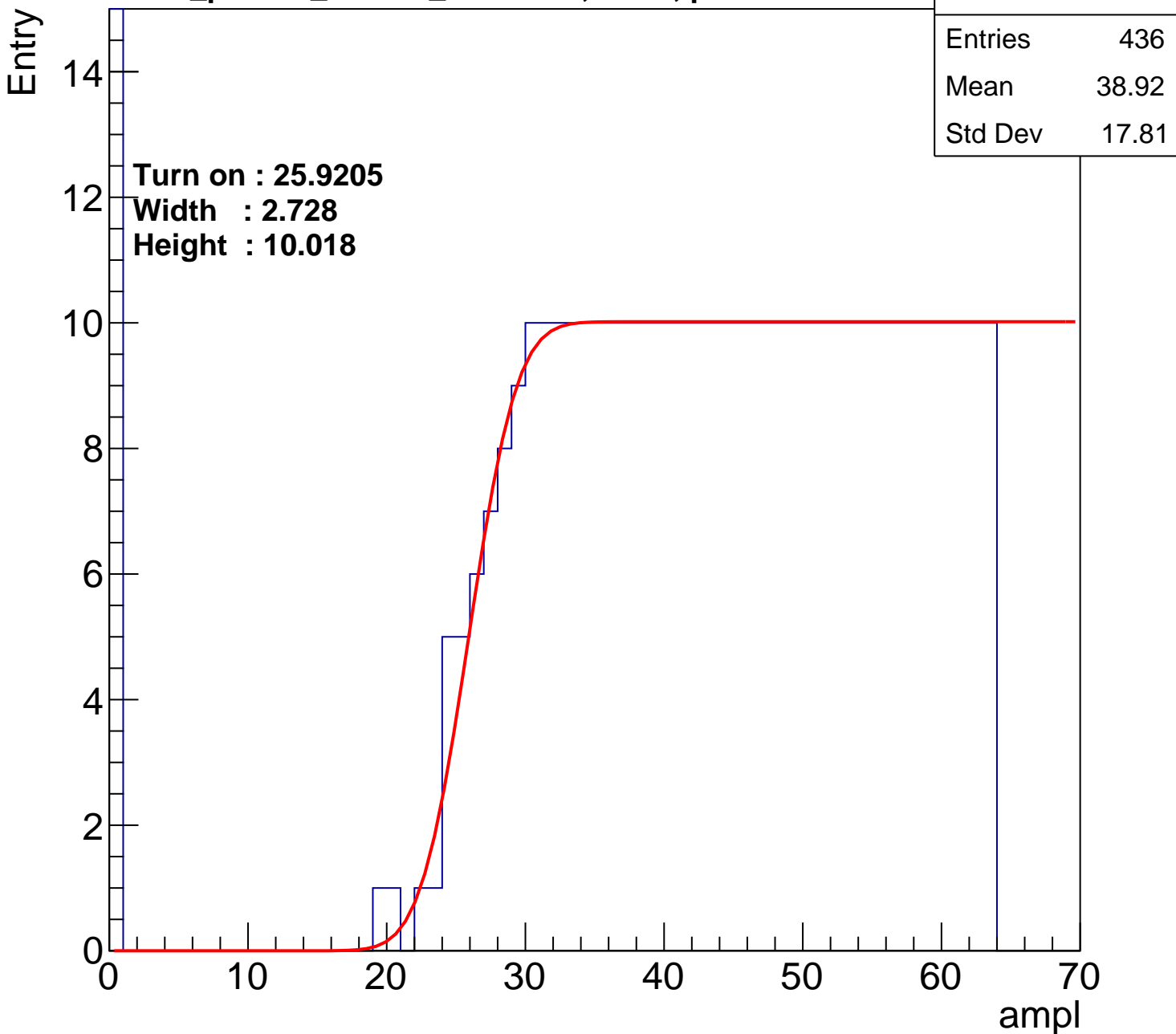
Height : 10.018

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L103S, U5-ch53

calib_packv5_041523_1651.root, FC#0, port C2

Entries	431
Mean	39.3
Std Dev	17.5

Turn on : 26.4183

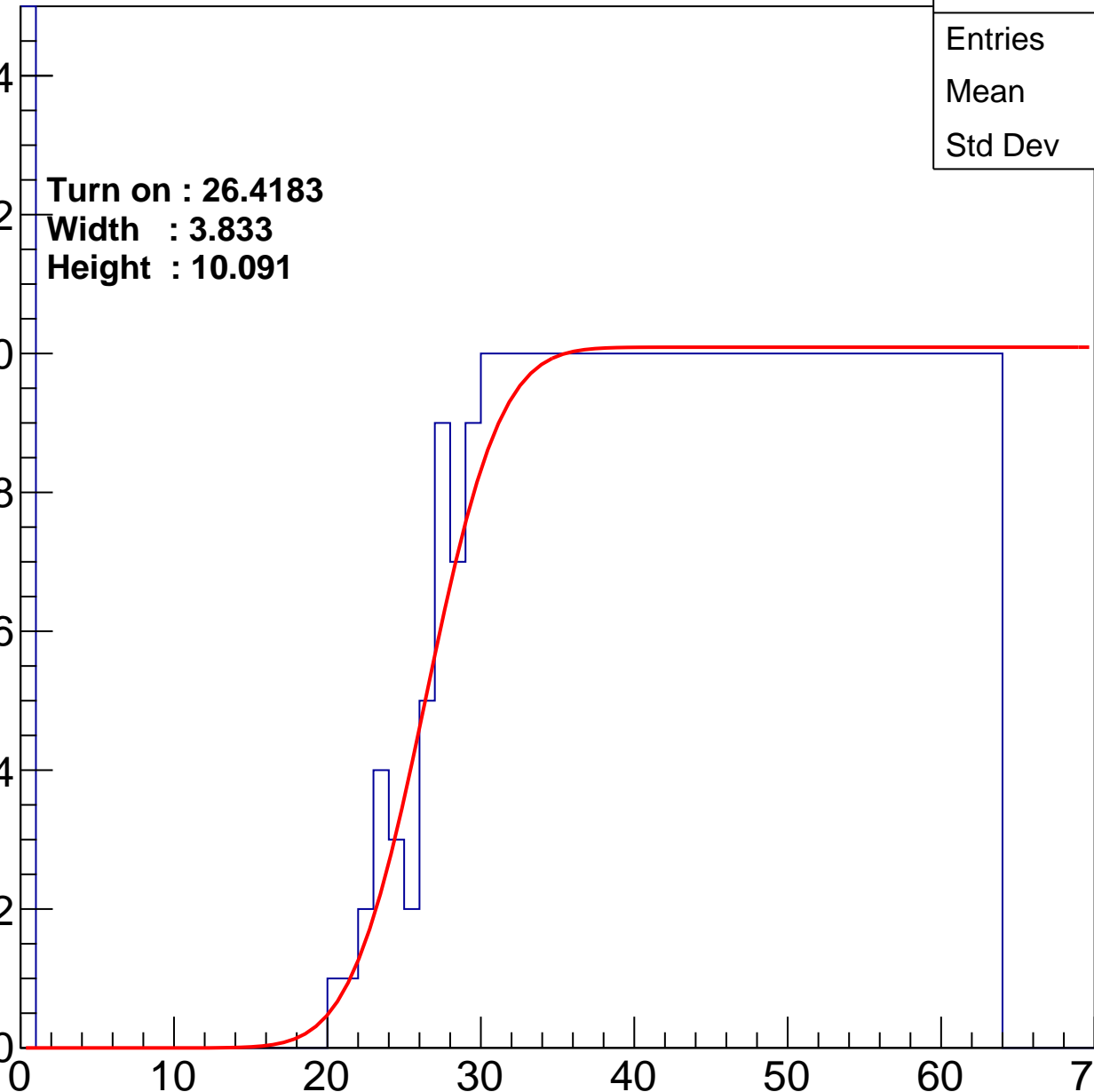
Width : 3.833

Height : 10.091

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch54

calib_packv5_041523_1651.root, FC#0, port C2

Entries	453
Mean	38.8
Std Dev	17.05

Turn on : 23.3318

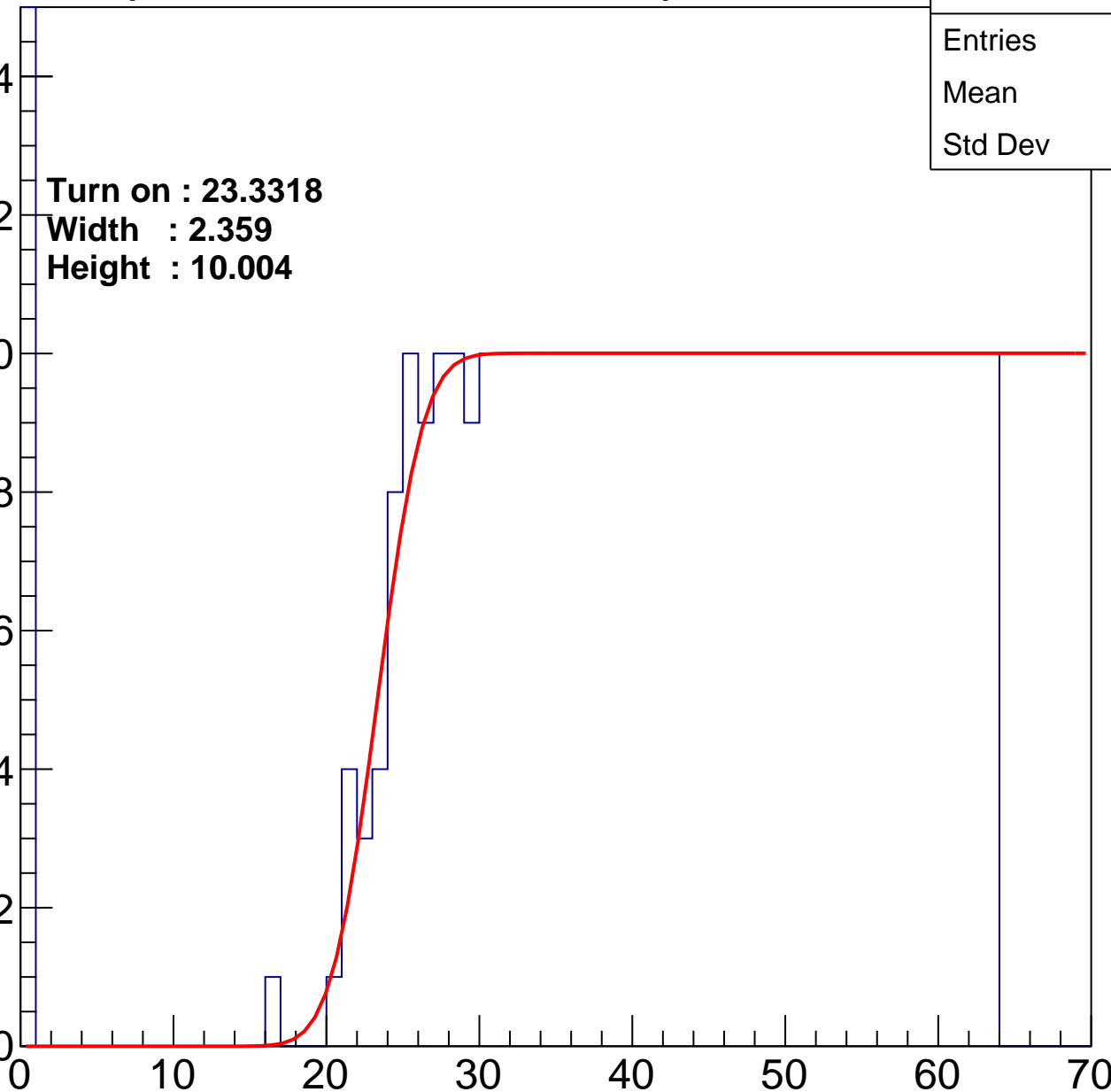
Width : 2.359

Height : 10.004

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch55

calib_packv5_041523_1651.root, FC#0, port C2

Entries	437
Mean	38.44
Std Dev	18.44

Turn on : 26.2650

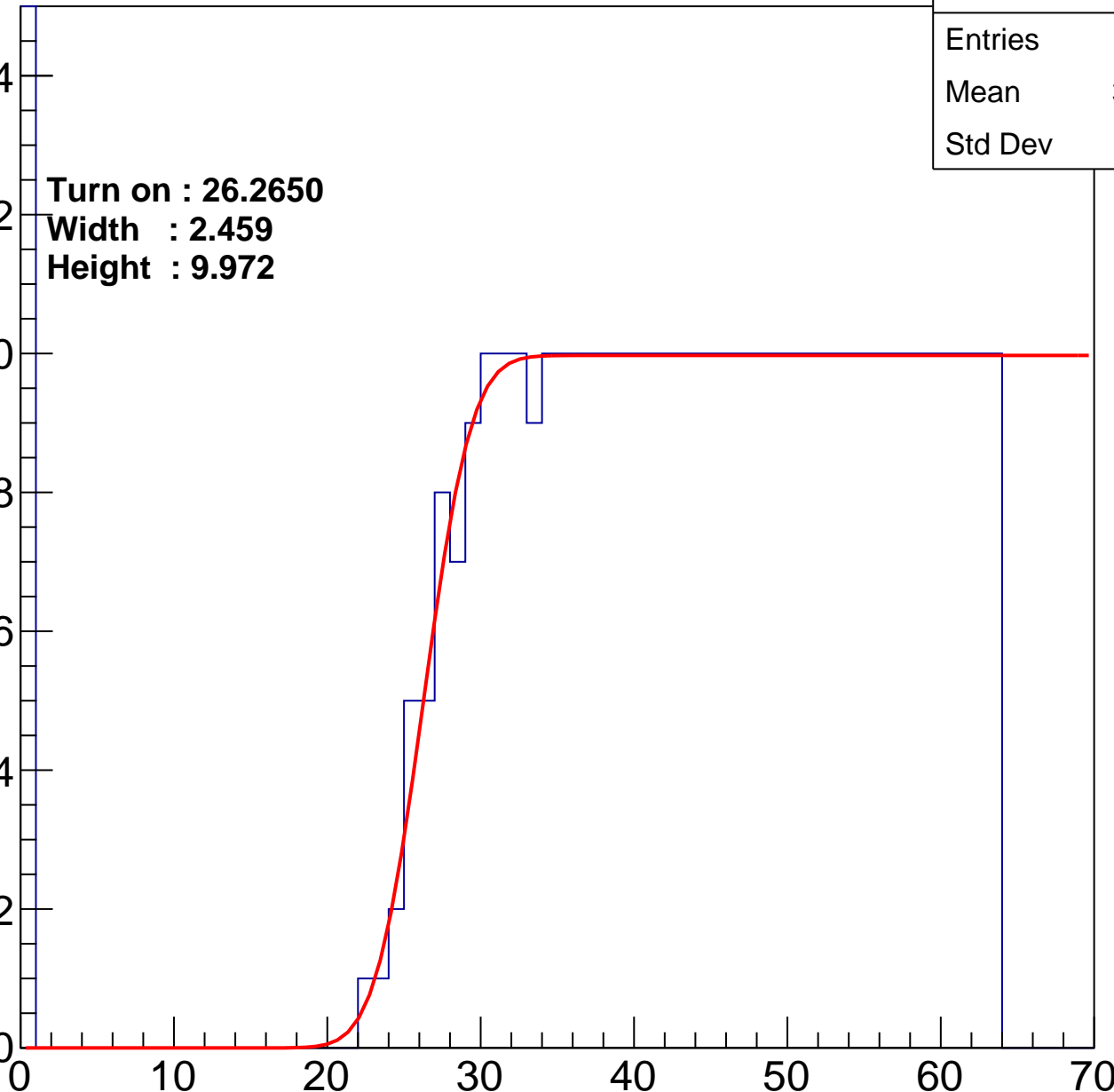
Width : 2.459

Height : 9.972

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch56

calib_packv5_041523_1651.root, FC#0, port C2

Entries	433
Mean	38.78
Std Dev	18.16

Turn on : 26.4729

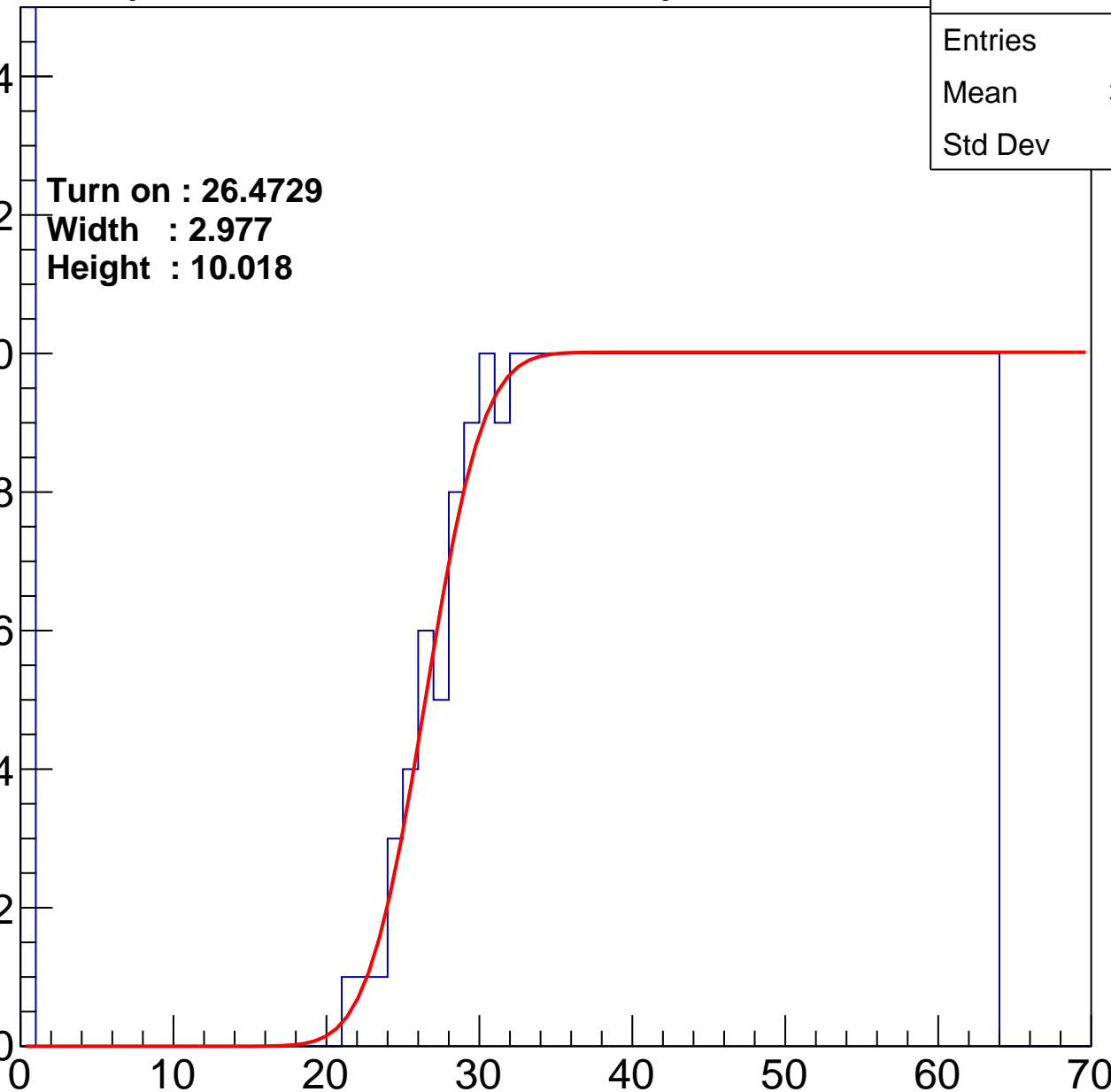
Width : 2.977

Height : 10.018

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch57

calib_packv5_041523_1651.root, FC#0, port C2

Entries	420
Mean	40.26
Std Dev	16.67

Turn on : 26.2293

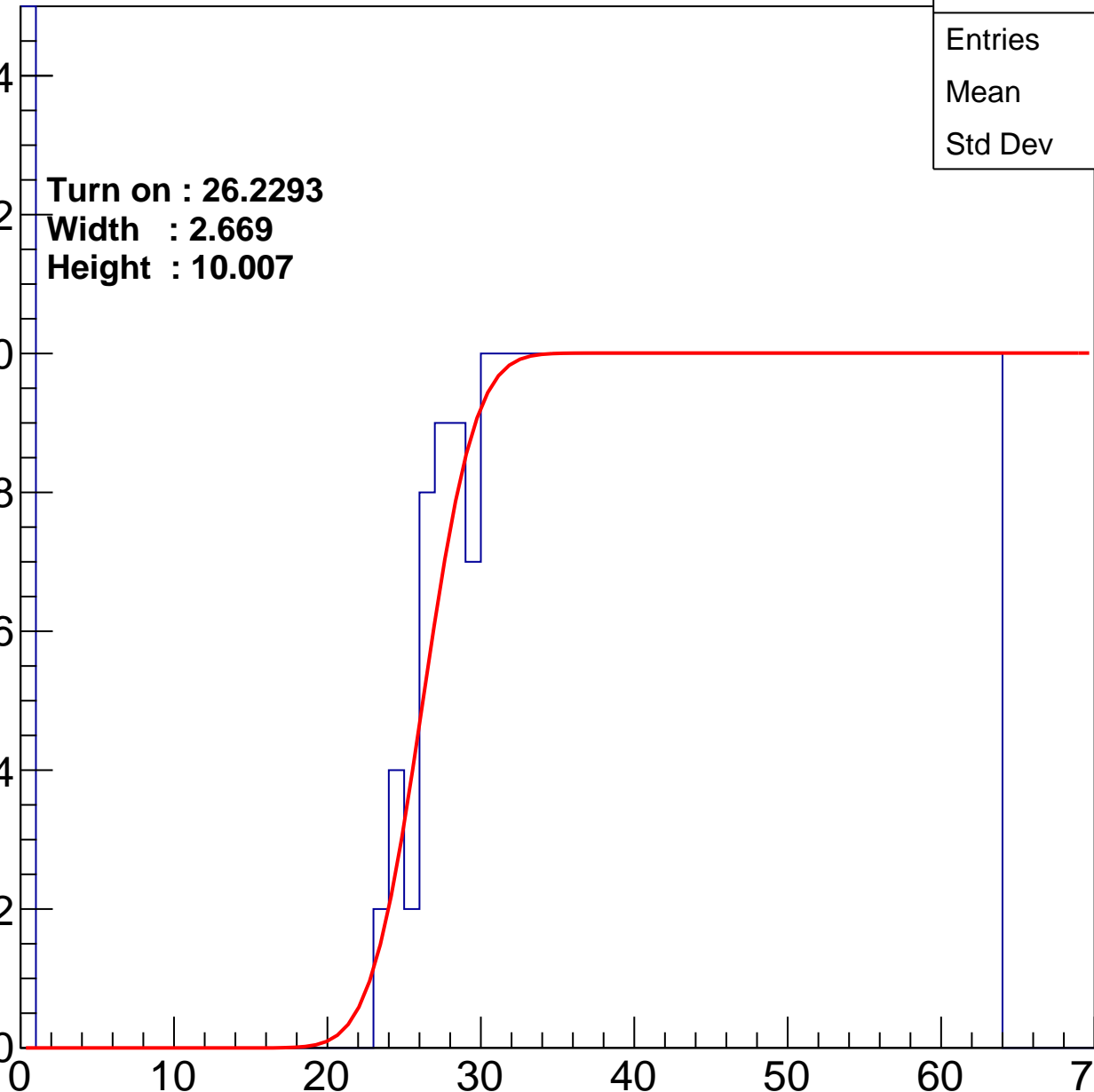
Width : 2.669

Height : 10.007

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch58

calib_packv5_041523_1651.root, FC#0, port C2

Entries	444
Mean	39.02
Std Dev	17.19

Turn on : 24.1299

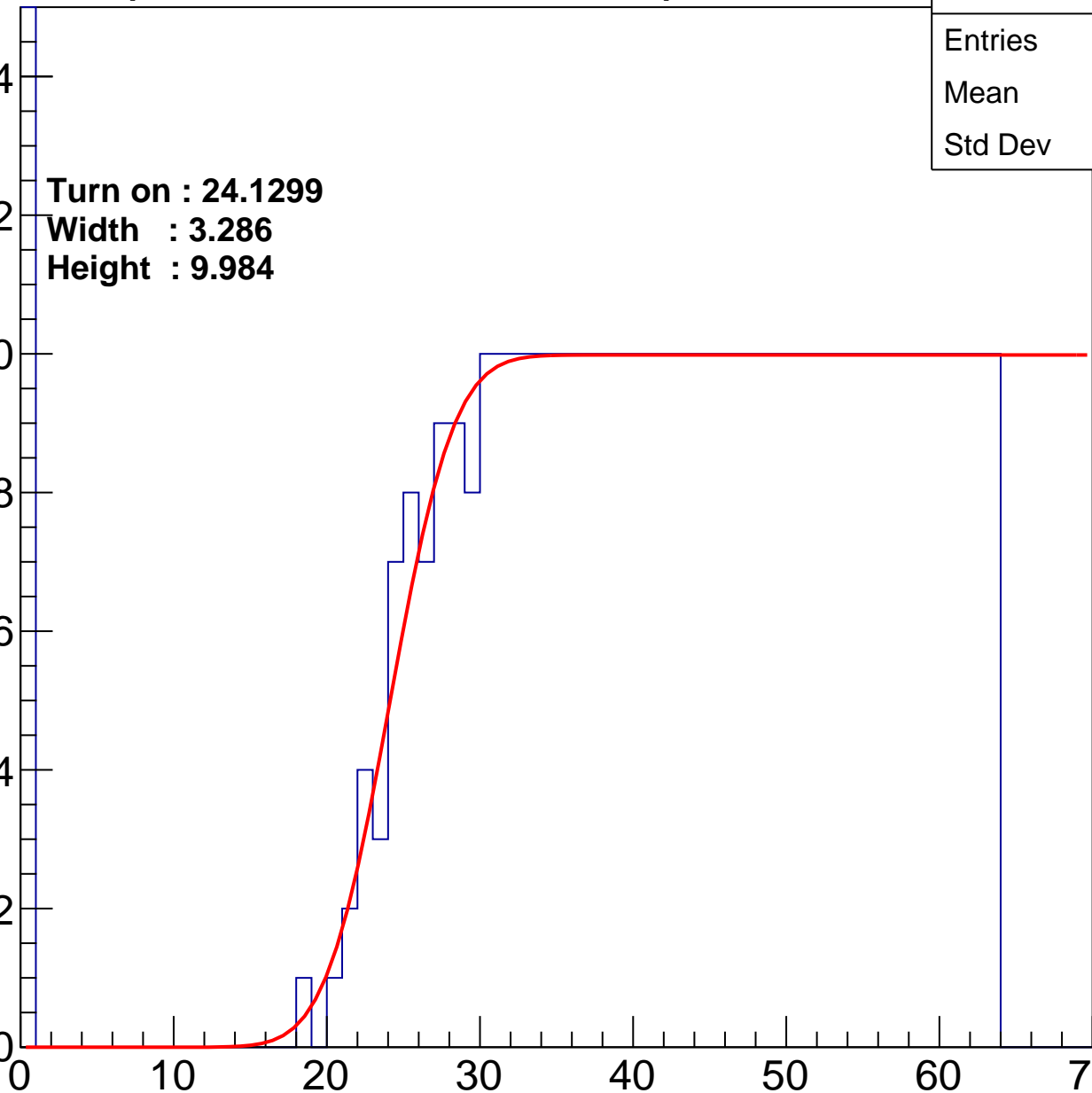
Width : 3.286

Height : 9.984

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch59

calib_packv5_041523_1651.root, FC#0, port C2

Entries	459
Mean	37.78
Std Dev	18.24

Turn on : 24.3304

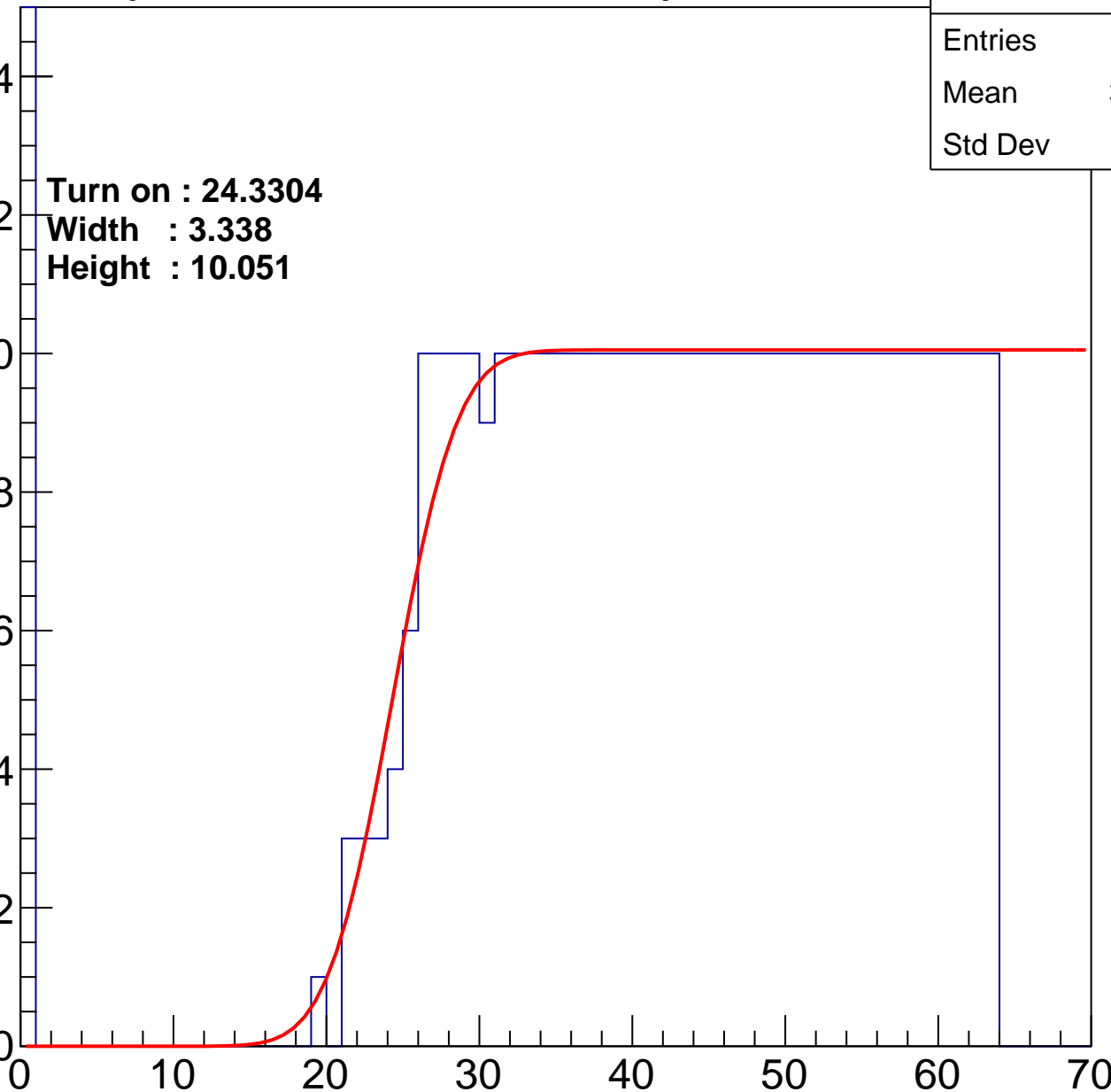
Width : 3.338

Height : 10.051

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch60

calib_packv5_041523_1651.root, FC#0, port C2

Entries	443
Mean	38.16
Std Dev	18.5

Turn on : 26.2174

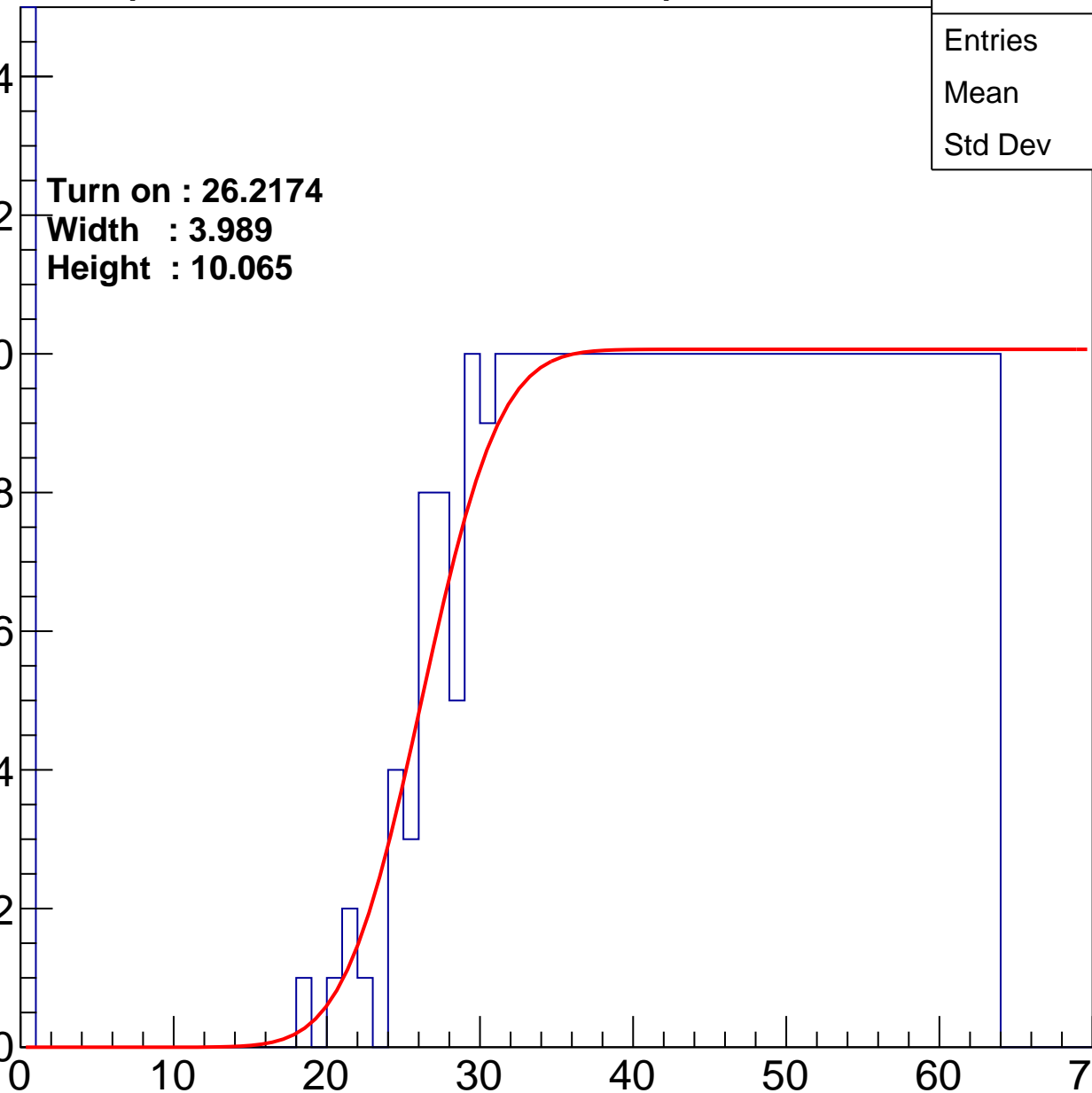
Width : 3.989

Height : 10.065

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch61

calib_packv5_041523_1651.root, FC#0, port C2

Entries	447
Mean	38.32
Std Dev	18.11

Turn on : 25.5219

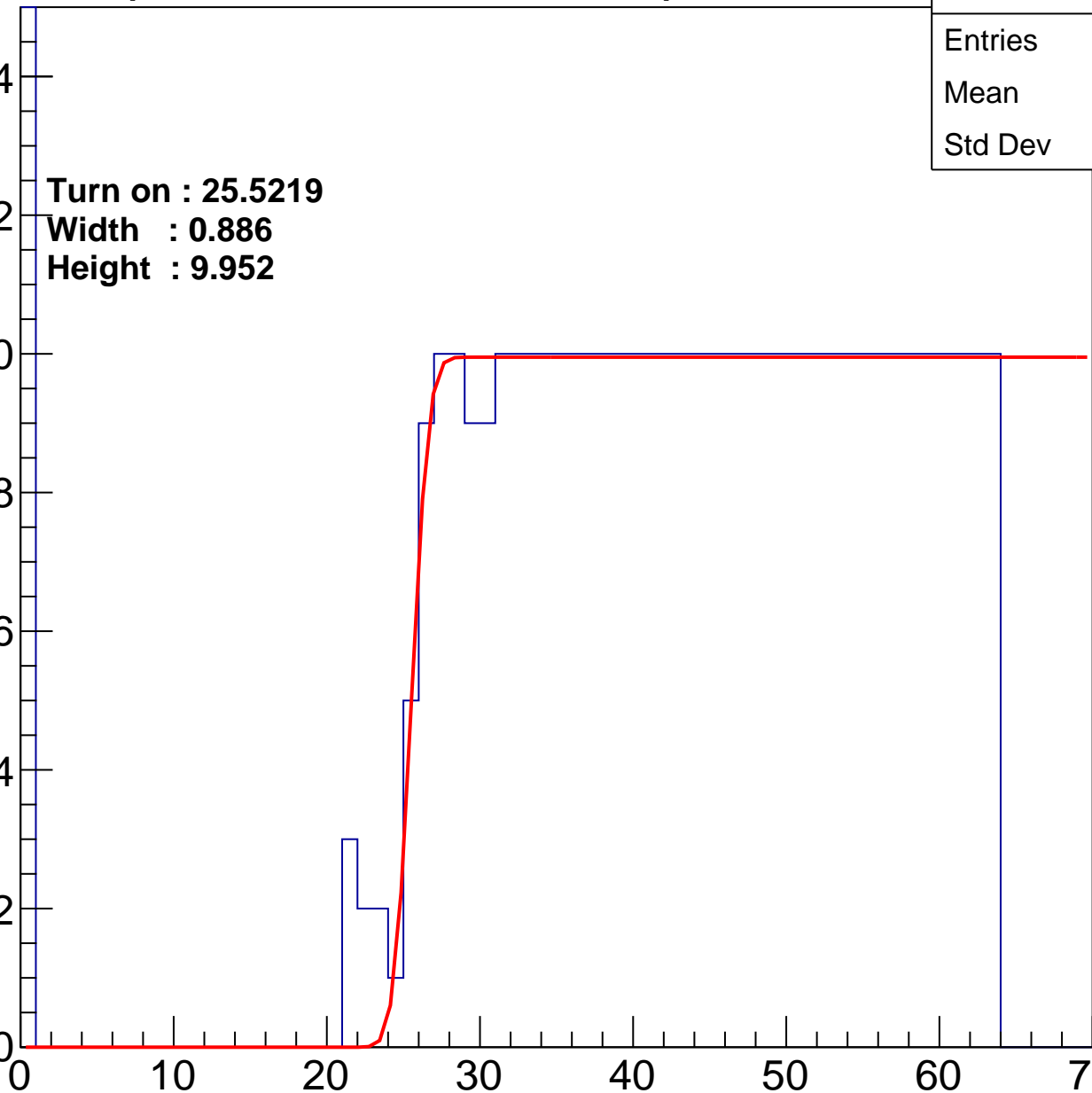
Width : 0.886

Height : 9.952

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch62

calib_packv5_041523_1651.root, FC#0, port C2

Entries	419
Mean	39.74
Std Dev	17.5

Turn on : 26.9727

Width : 3.139

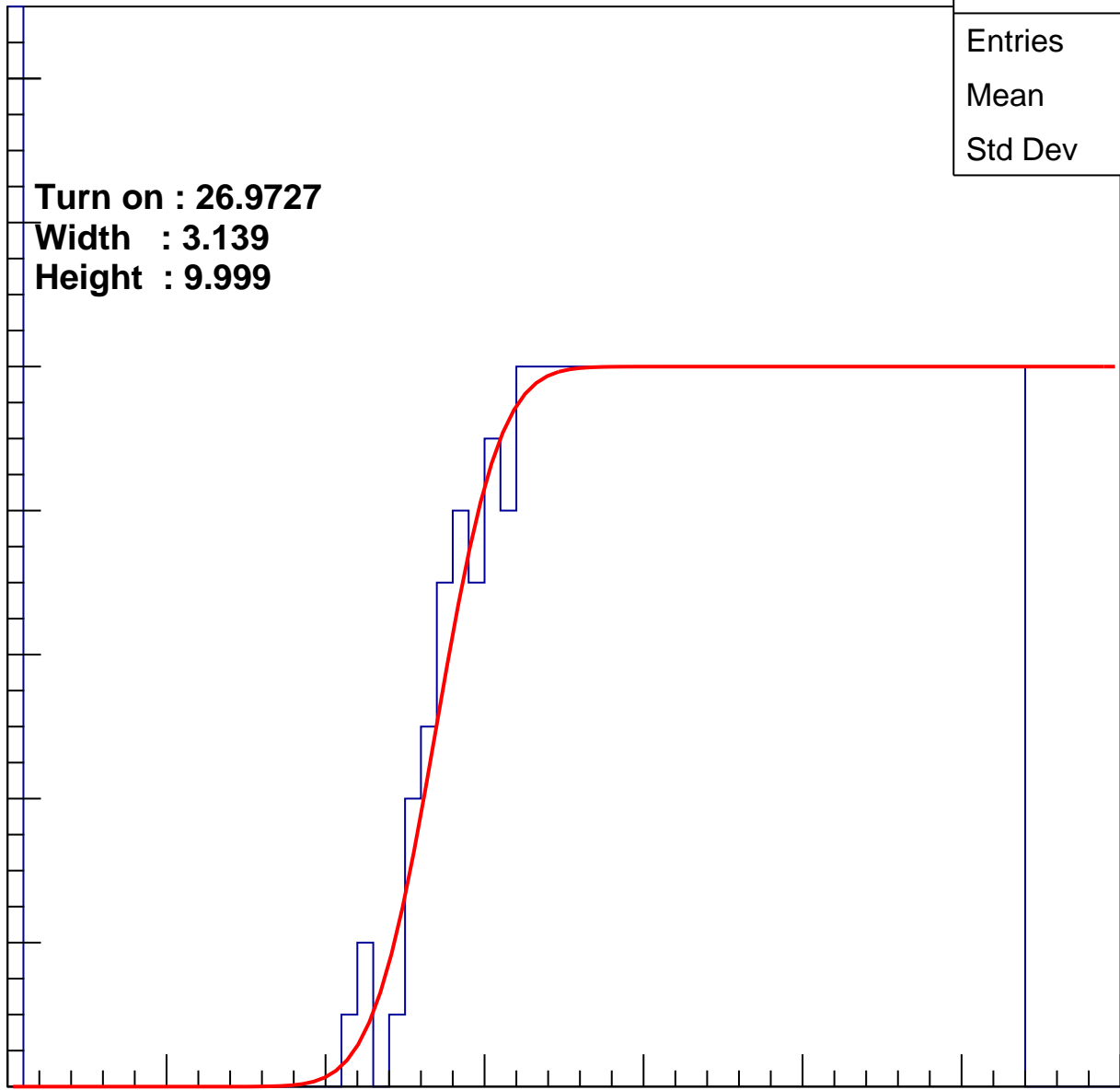
Height : 9.999

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L103S, U5-ch63

calib_packv5_041523_1651.root, FC#0, port C2

Entries	451
Mean	38.47
Std Dev	17.64

Turn on : 24.3625

Width : 3.288

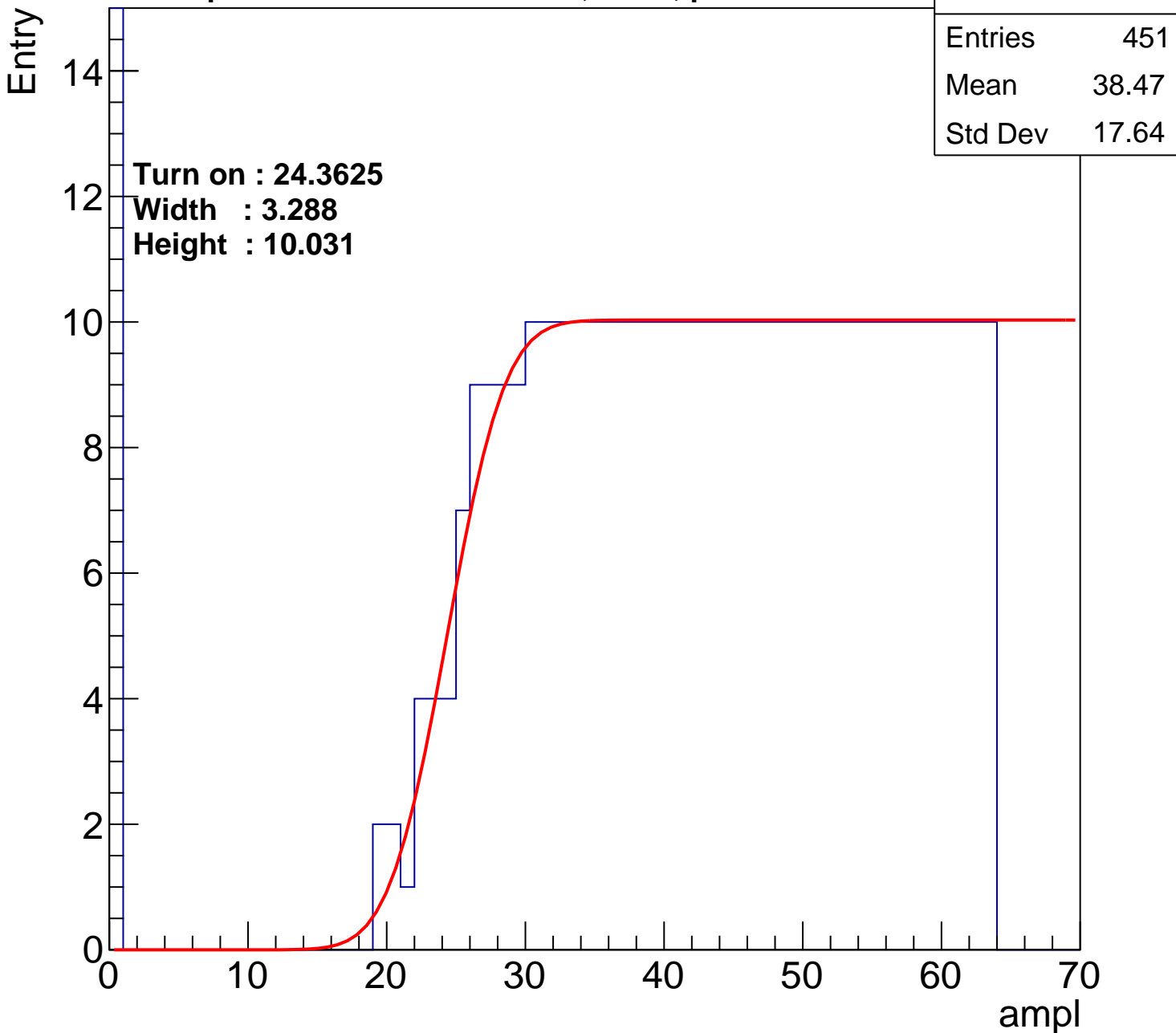
Height : 10.031

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L103S, U5-ch64

calib_packv5_041523_1651.root, FC#0, port C2

Entries	445
Mean	38.56
Std Dev	17.83

Turn on : 25.8353

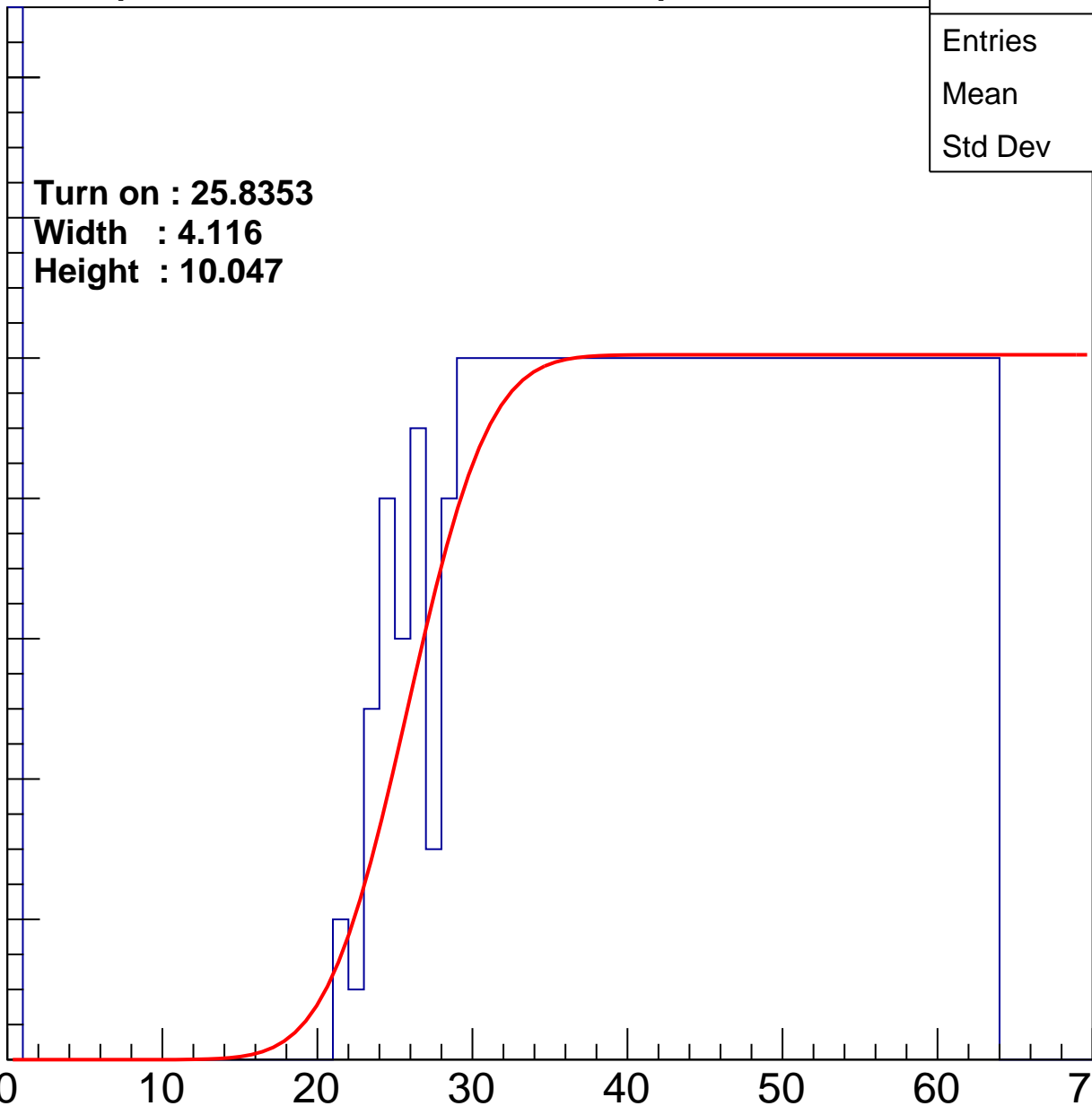
Width : 4.116

Height : 10.047

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch65

calib_packv5_041523_1651.root, FC#0, port C2

Entries	447
Mean	38.09
Std Dev	18.43

Turn on : 25.5917

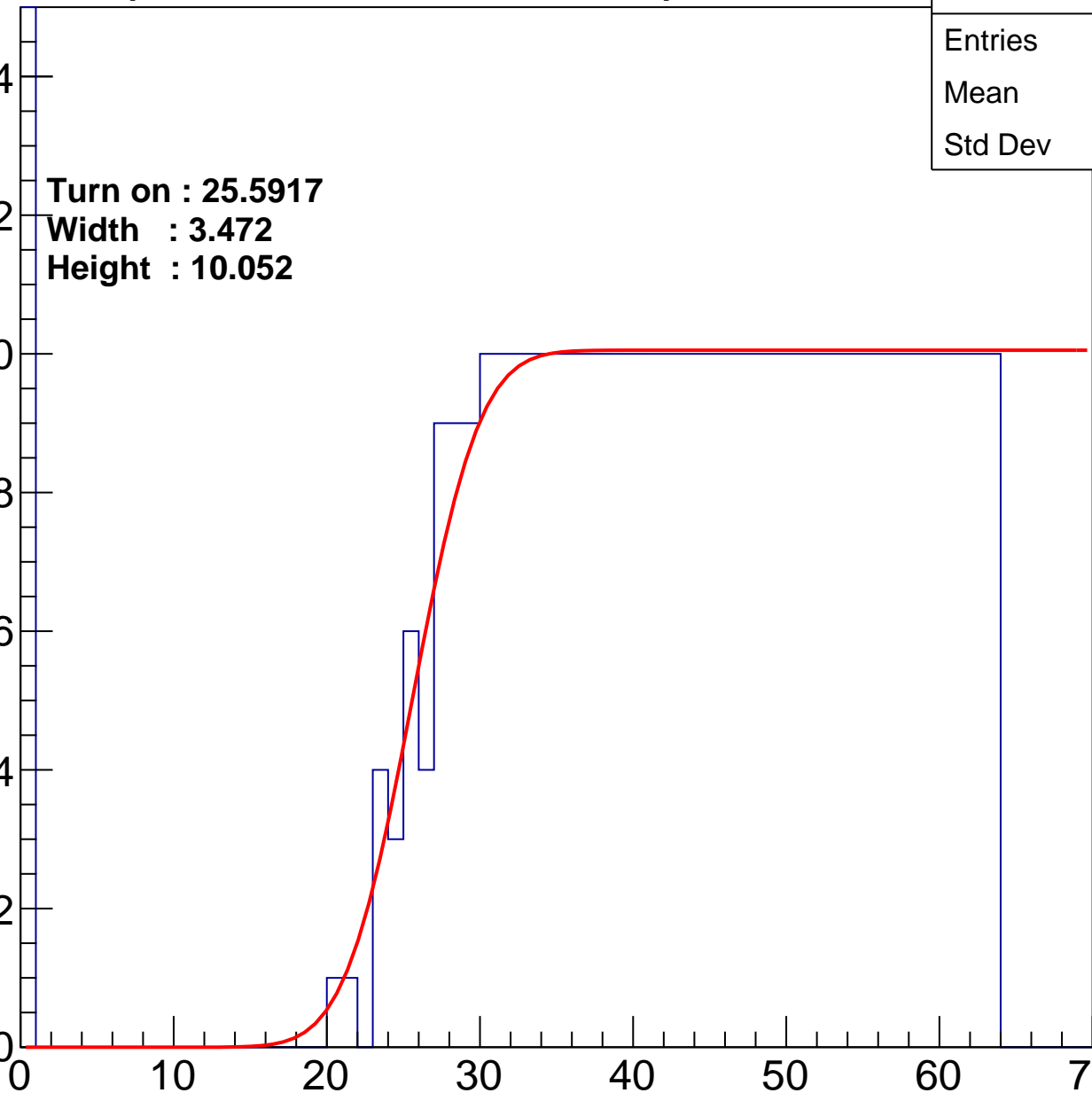
Width : 3.472

Height : 10.052

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch66

calib_packv5_041523_1651.root, FC#0, port C2

Entries	460
Mean	38.45
Std Dev	17.2

Turn on : 22.8418

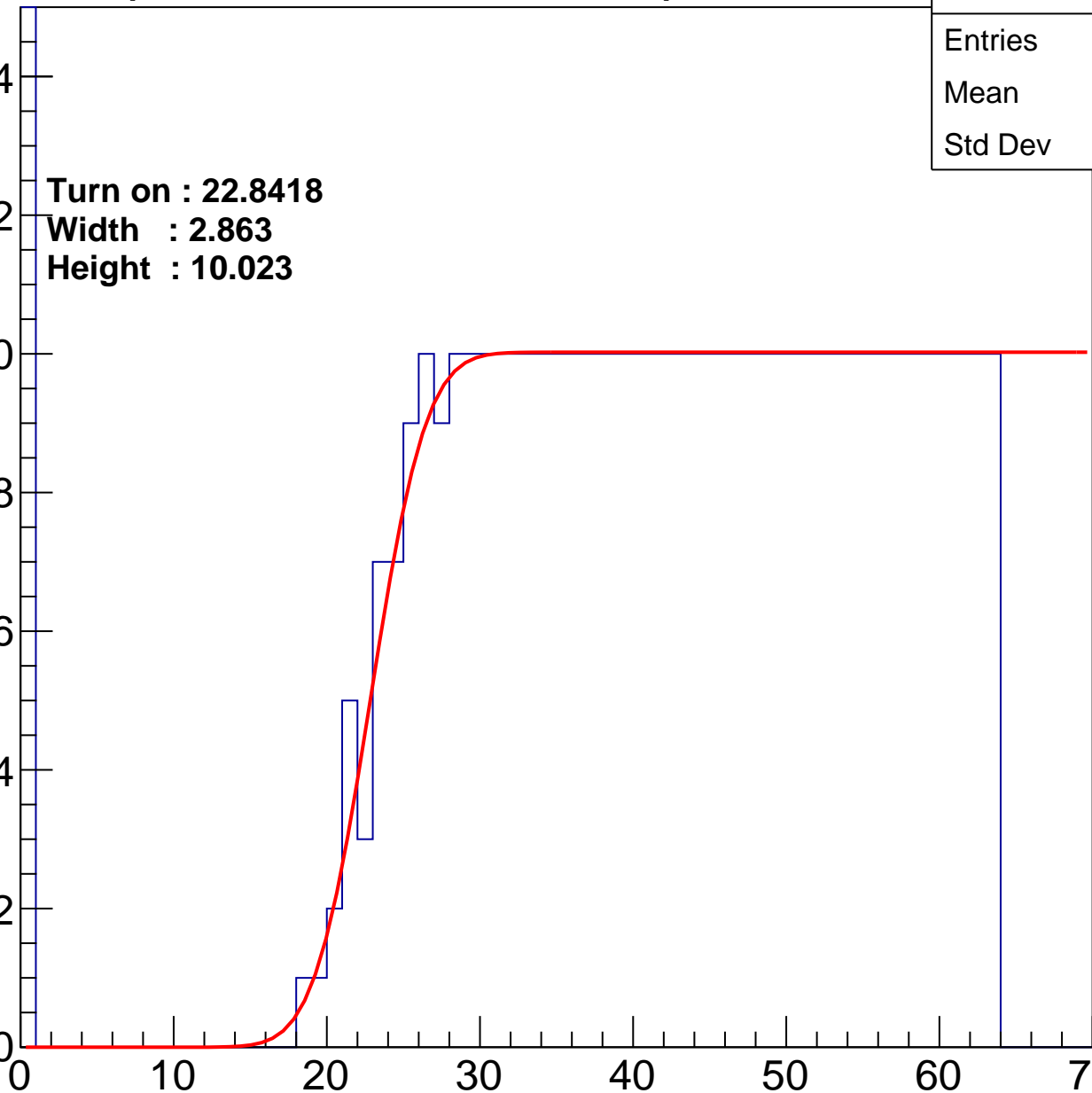
Width : 2.863

Height : 10.023

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch67

calib_packv5_041523_1651.root, FC#0, port C2

Entries	469
Mean	37.71
Std Dev	17.8

Turn on : 22.5906

Width : 4.377

Height : 10.064

Entry

14

12

10

8

6

4

2

0

0

10

20

30

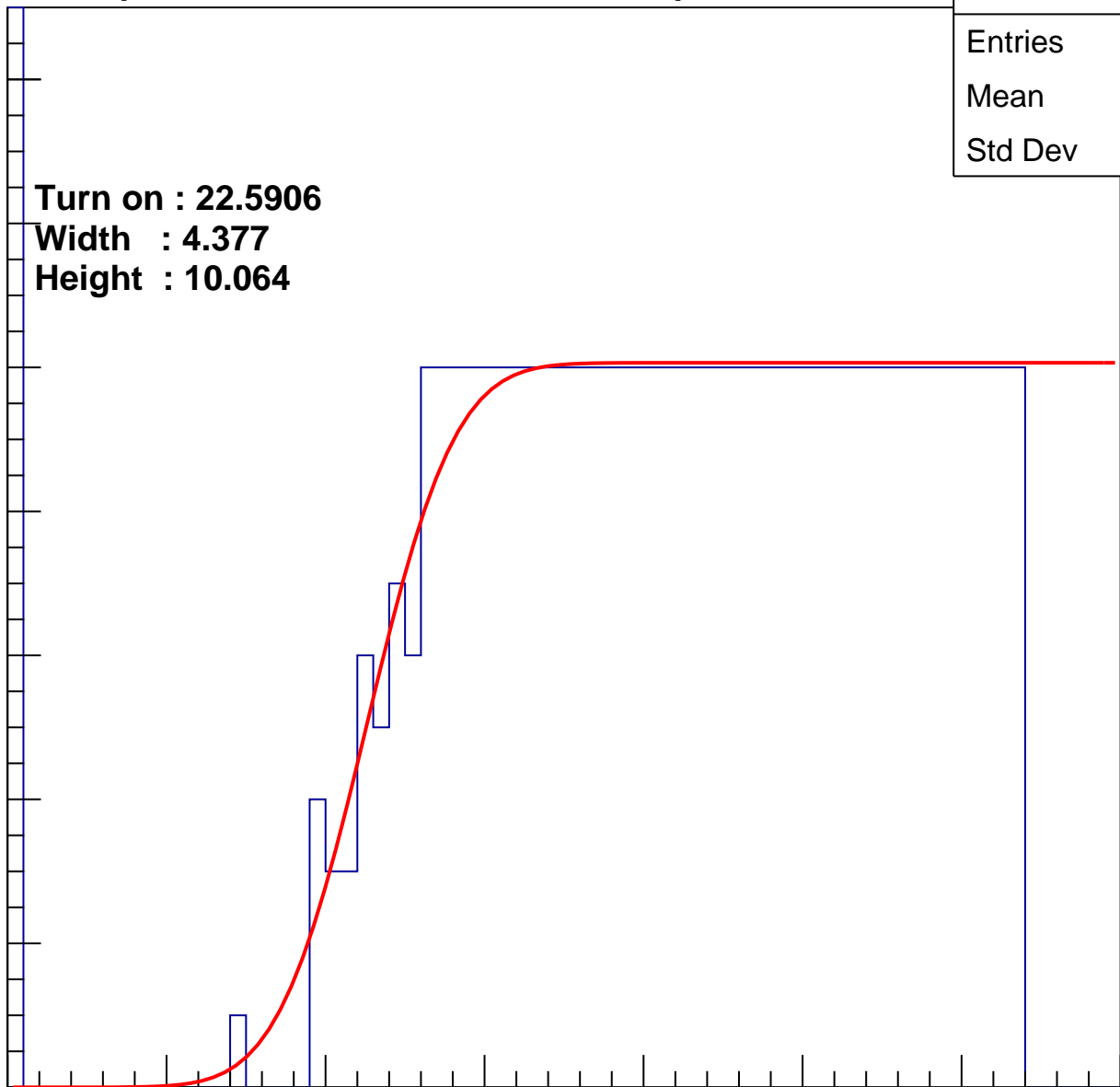
40

50

60

70

ampl



B1L103S, U5-ch68

calib_packv5_041523_1651.root, FC#0, port C2

Entries	442
Mean	38.74
Std Dev	17.76

Turn on : 25.1329

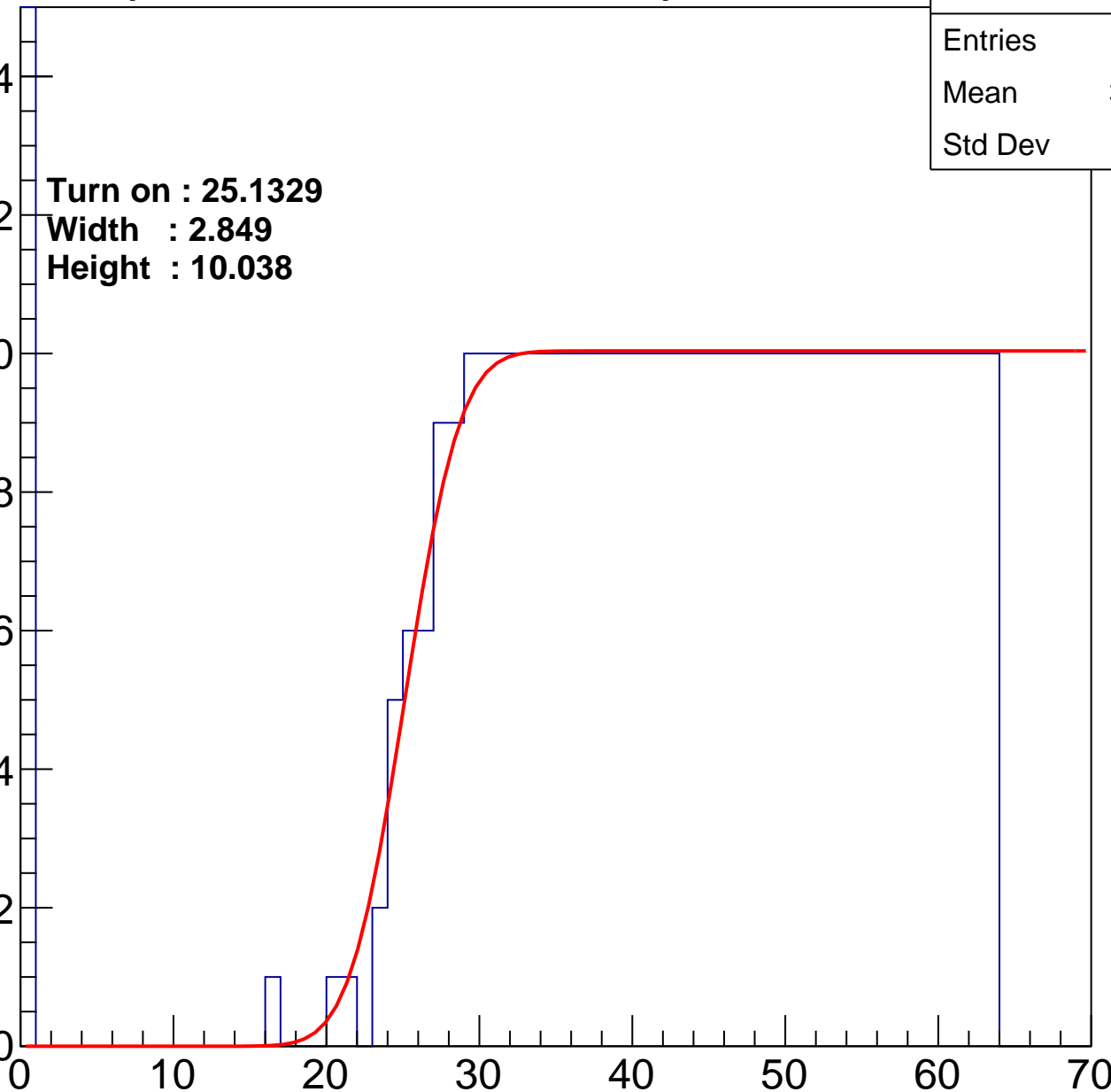
Width : 2.849

Height : 10.038

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch69

calib_packv5_041523_1651.root, FC#0, port C2

Entries	431
Mean	39.07
Std Dev	17.85

Turn on : 26.6275

Width : 2.820

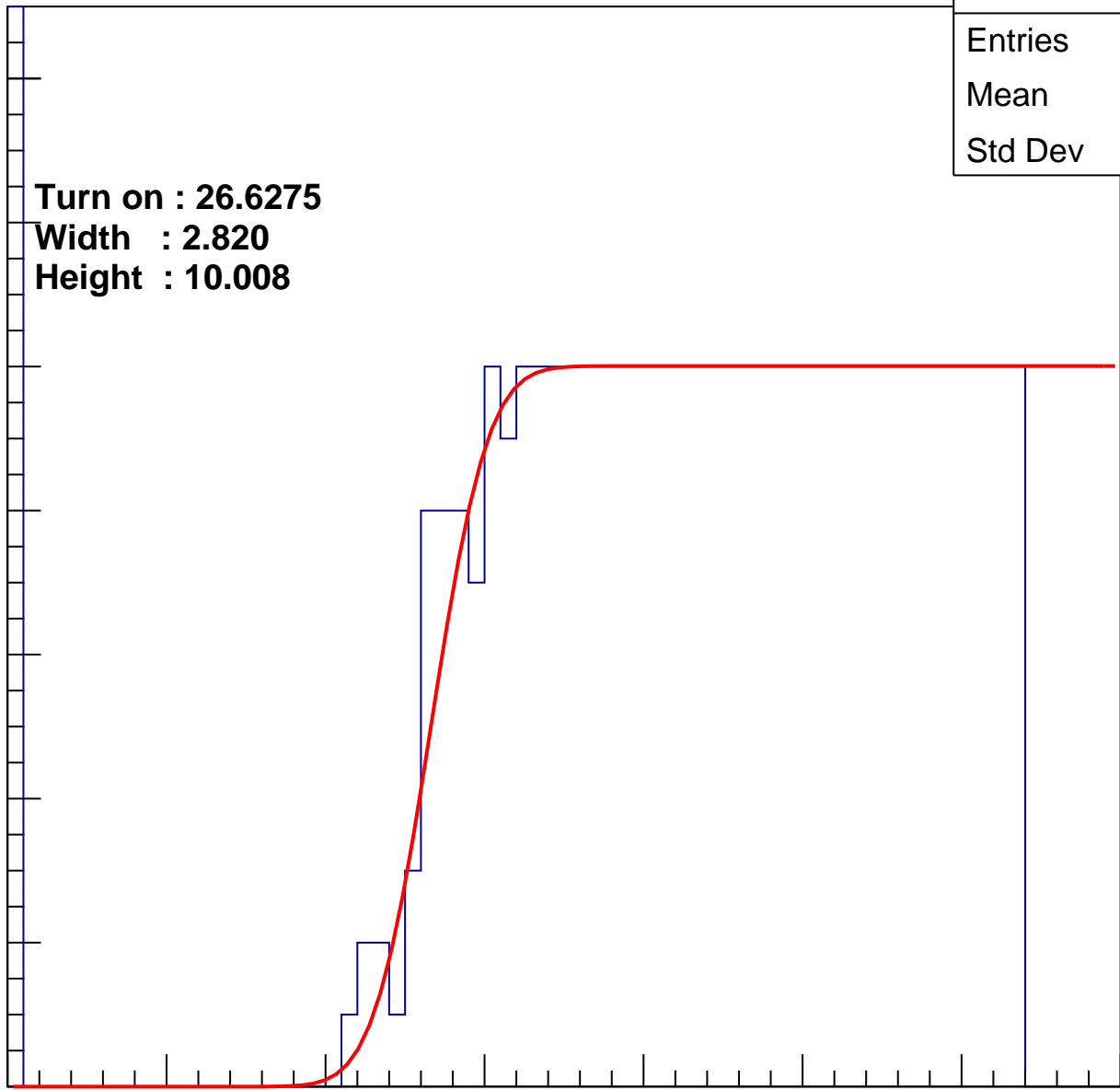
Height : 10.008

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L103S, U5-ch70

calib_packv5_041523_1651.root, FC#0, port C2

Entries	450
Mean	38.16
Std Dev	18.17

Turn on : 25.0535

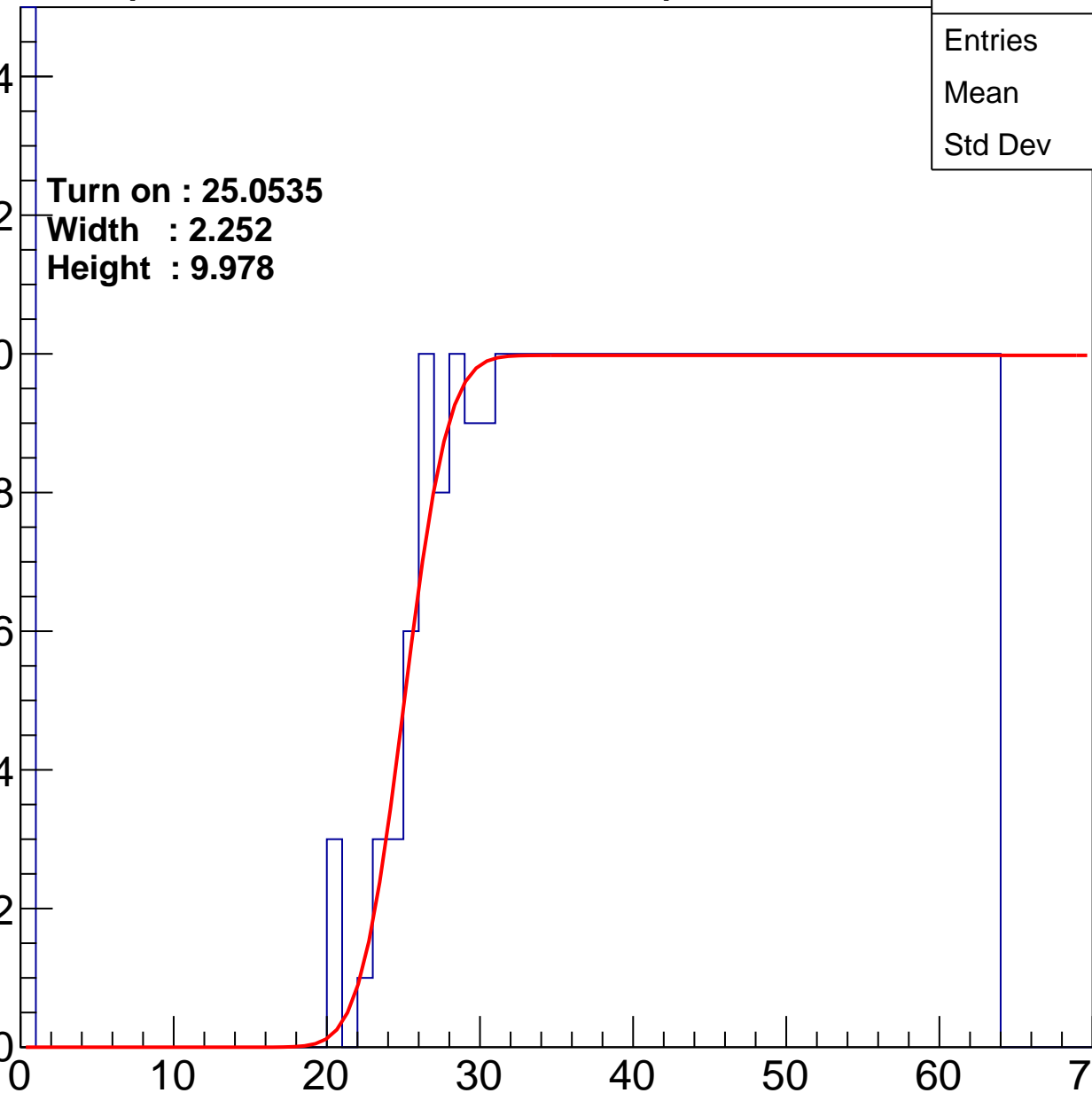
Width : 2.252

Height : 9.978

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch71

calib_packv5_041523_1651.root, FC#0, port C2

Entries	445
Mean	38.4
Std Dev	18.11

Turn on : 25.5290

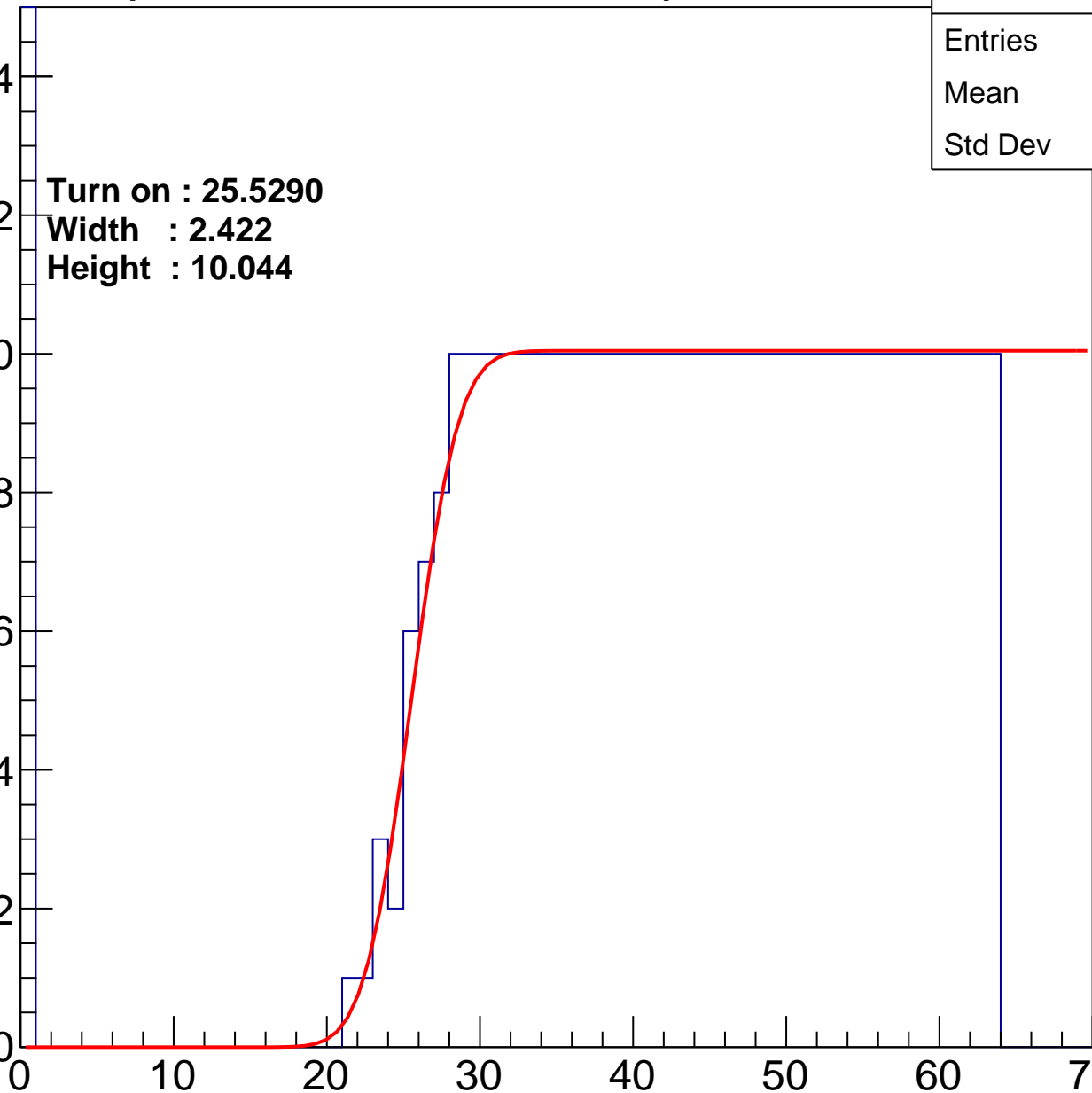
Width : 2.422

Height : 10.044

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch72

calib_packv5_041523_1651.root, FC#0, port C2

Entries	462
Mean	37.81
Std Dev	18.03

Turn on : 23.8561

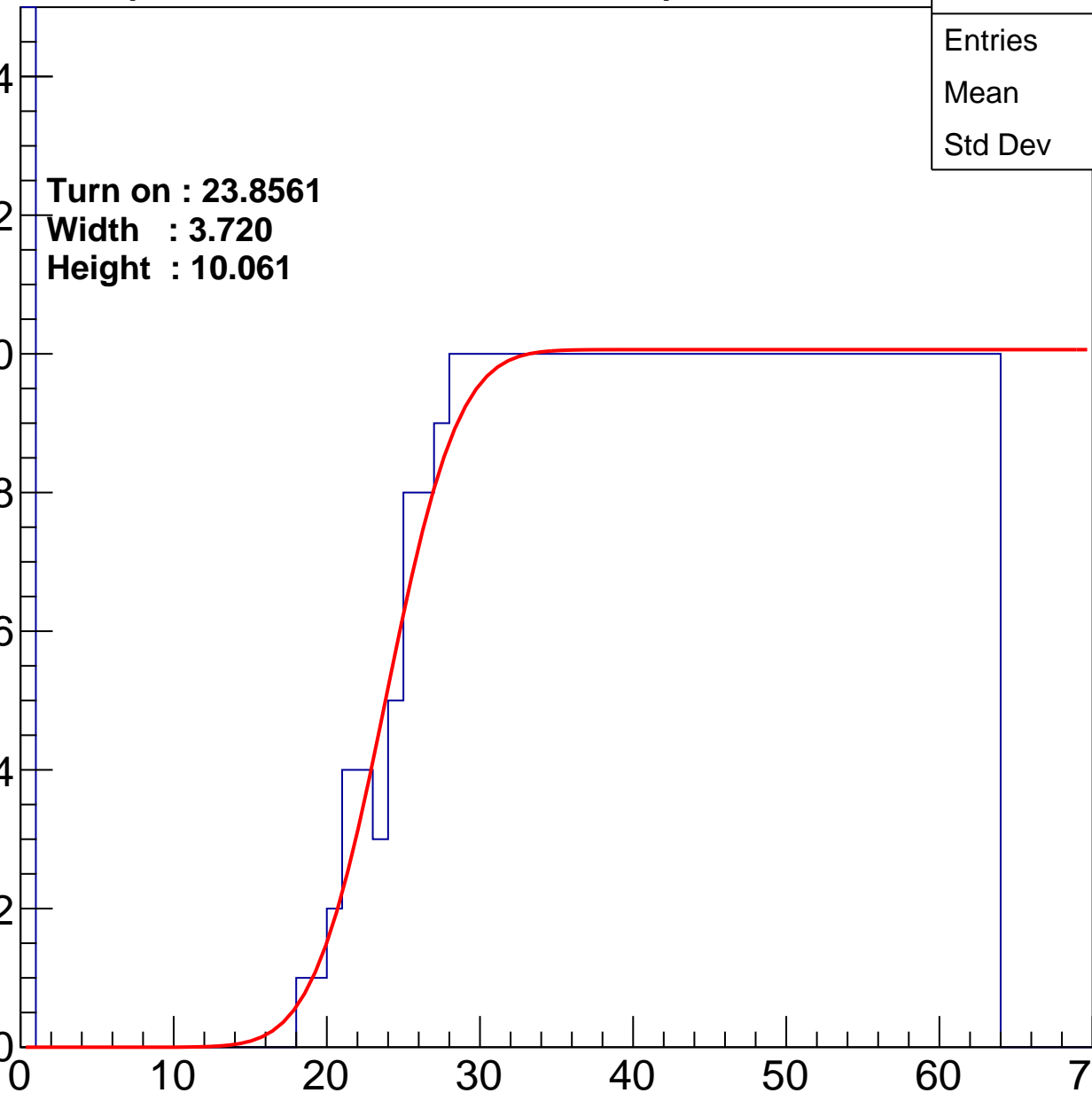
Width : 3.720

Height : 10.061

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch73

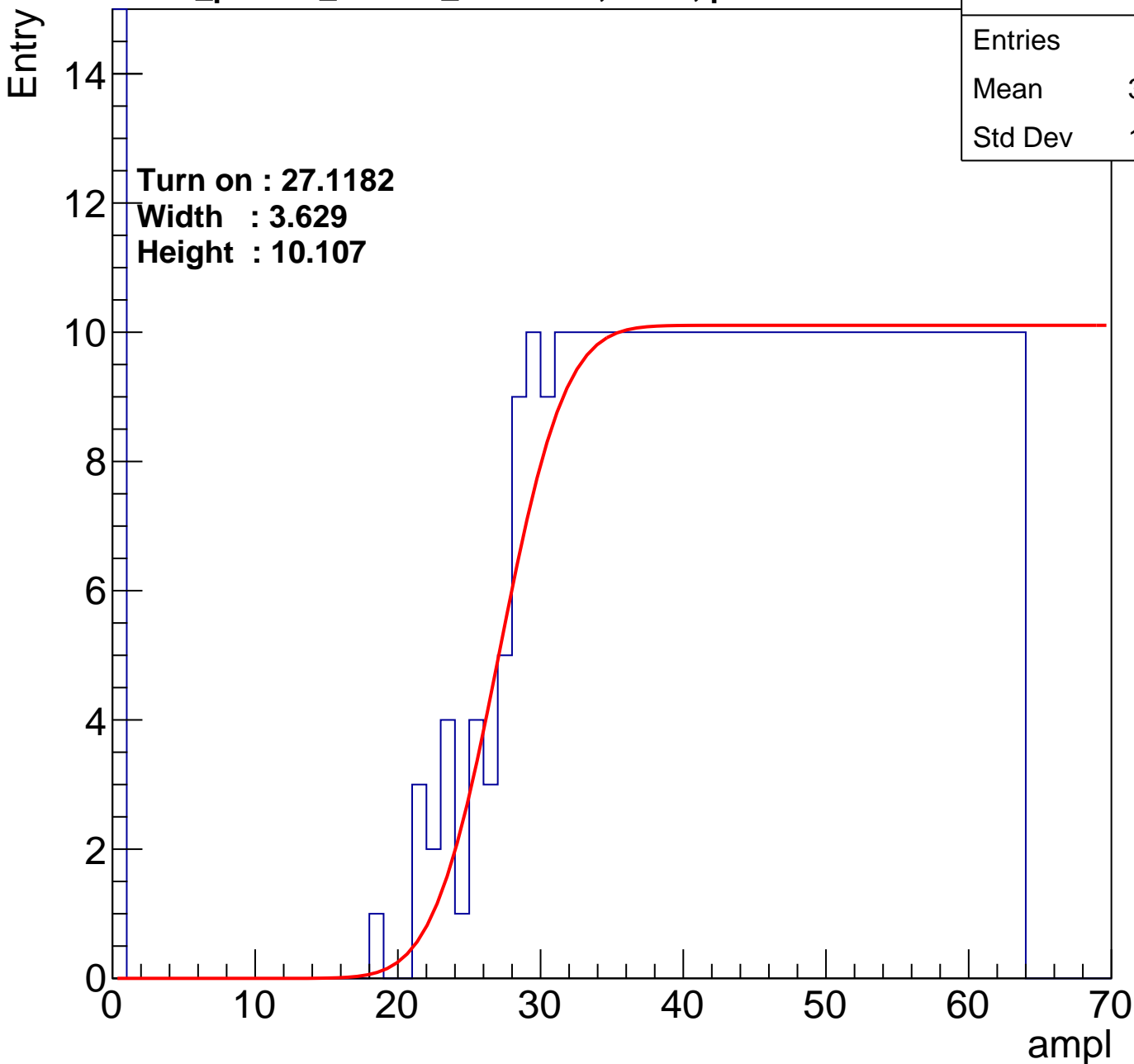
calib_packv5_041523_1651.root, FC#0, port C2

Entries	433
Mean	38.97
Std Dev	17.87

Turn on : 27.1182

Width : 3.629

Height : 10.107



B1L103S, U5-ch74

calib_packv5_041523_1651.root, FC#0, port C2

Entries	448
Mean	38.05
Std Dev	18.42

Turn on : 26.0391

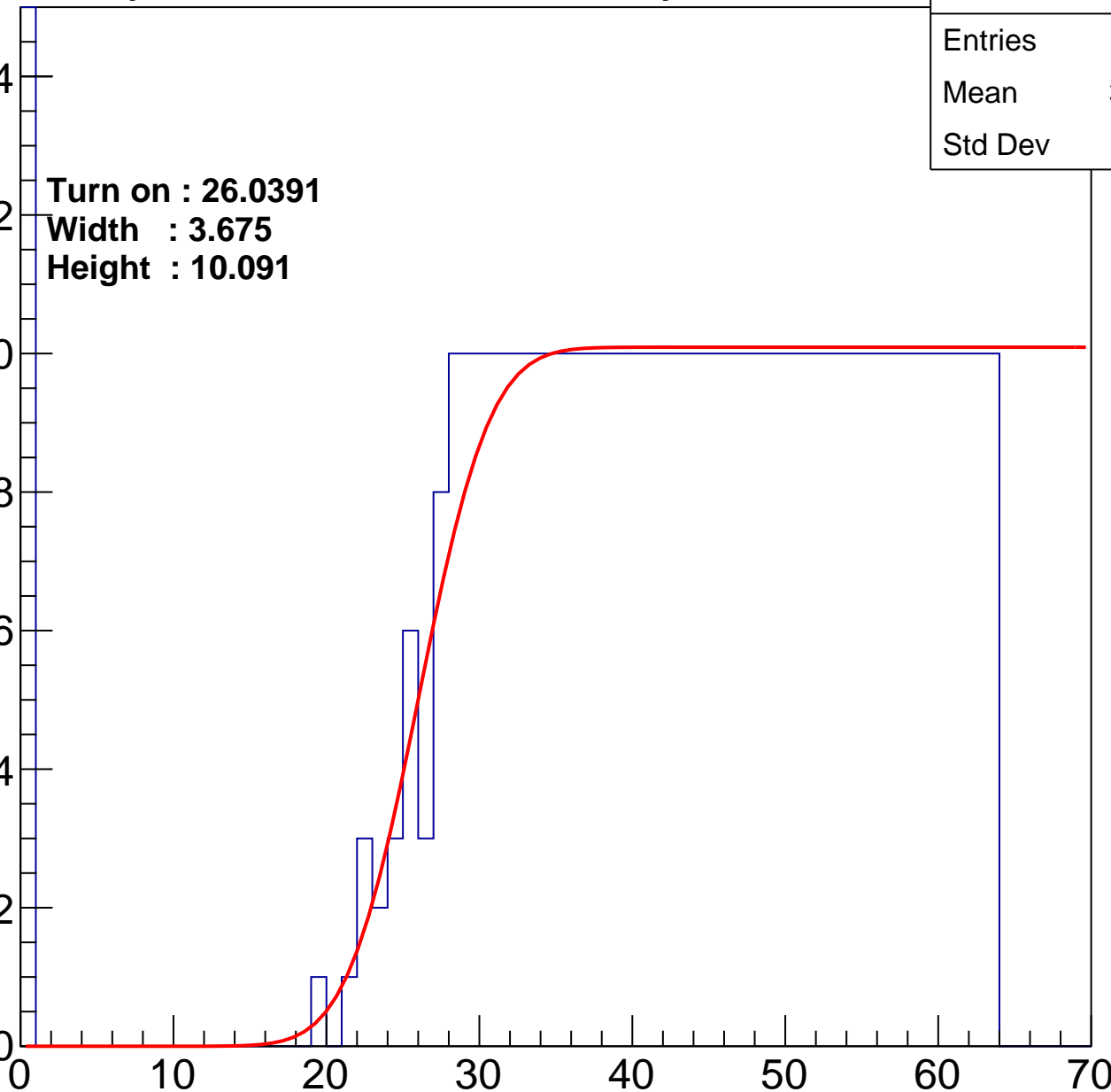
Width : 3.675

Height : 10.091

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch75

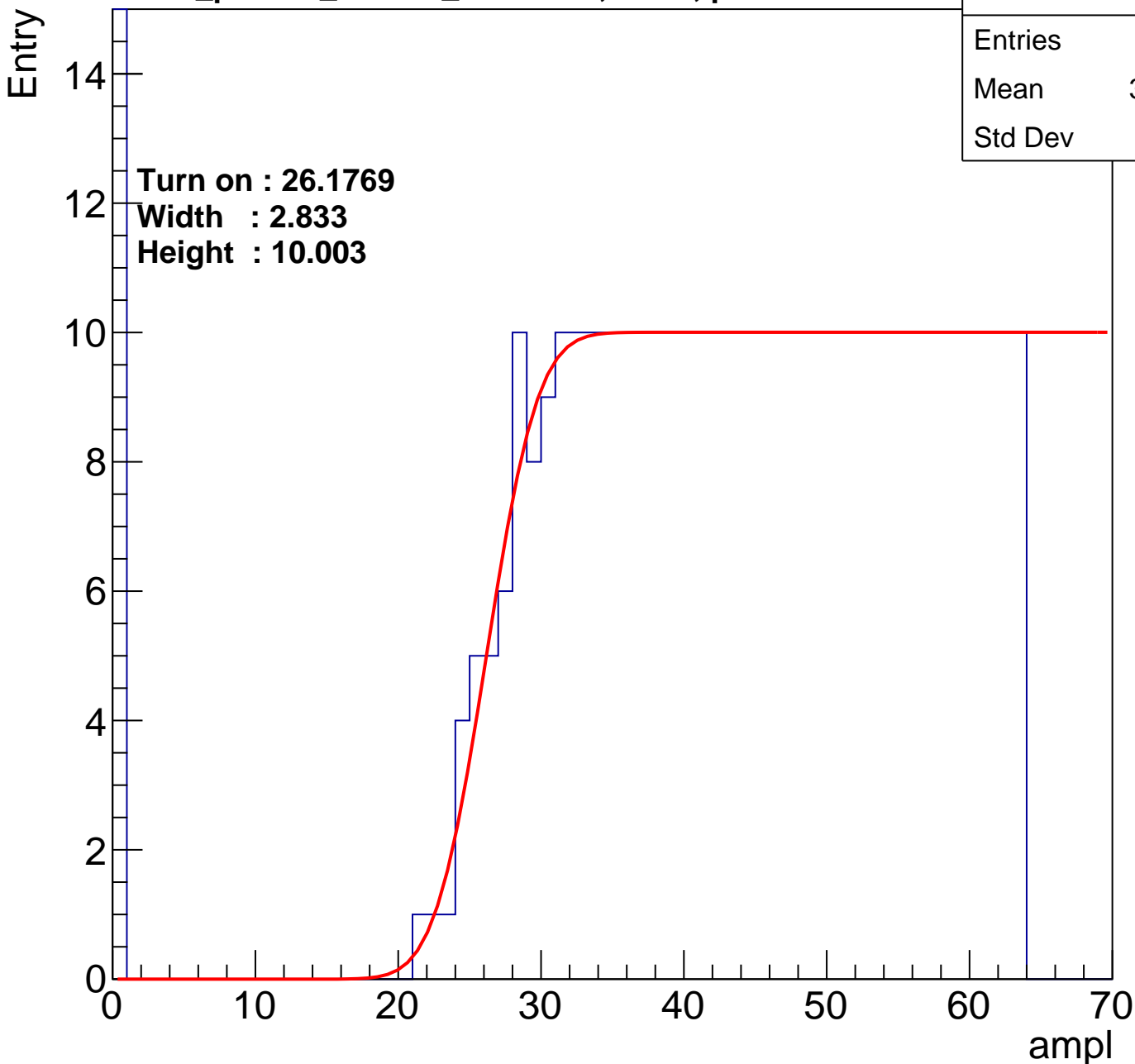
calib_packv5_041523_1651.root, FC#0, port C2

Entries	449
Mean	37.57
Std Dev	19.01

Turn on : 26.1769

Width : 2.833

Height : 10.003



B1L103S, U5-ch76

calib_packv5_041523_1651.root, FC#0, port C2

Entries	445
Mean	39.05
Std Dev	17.09

Turn on : 23.9323

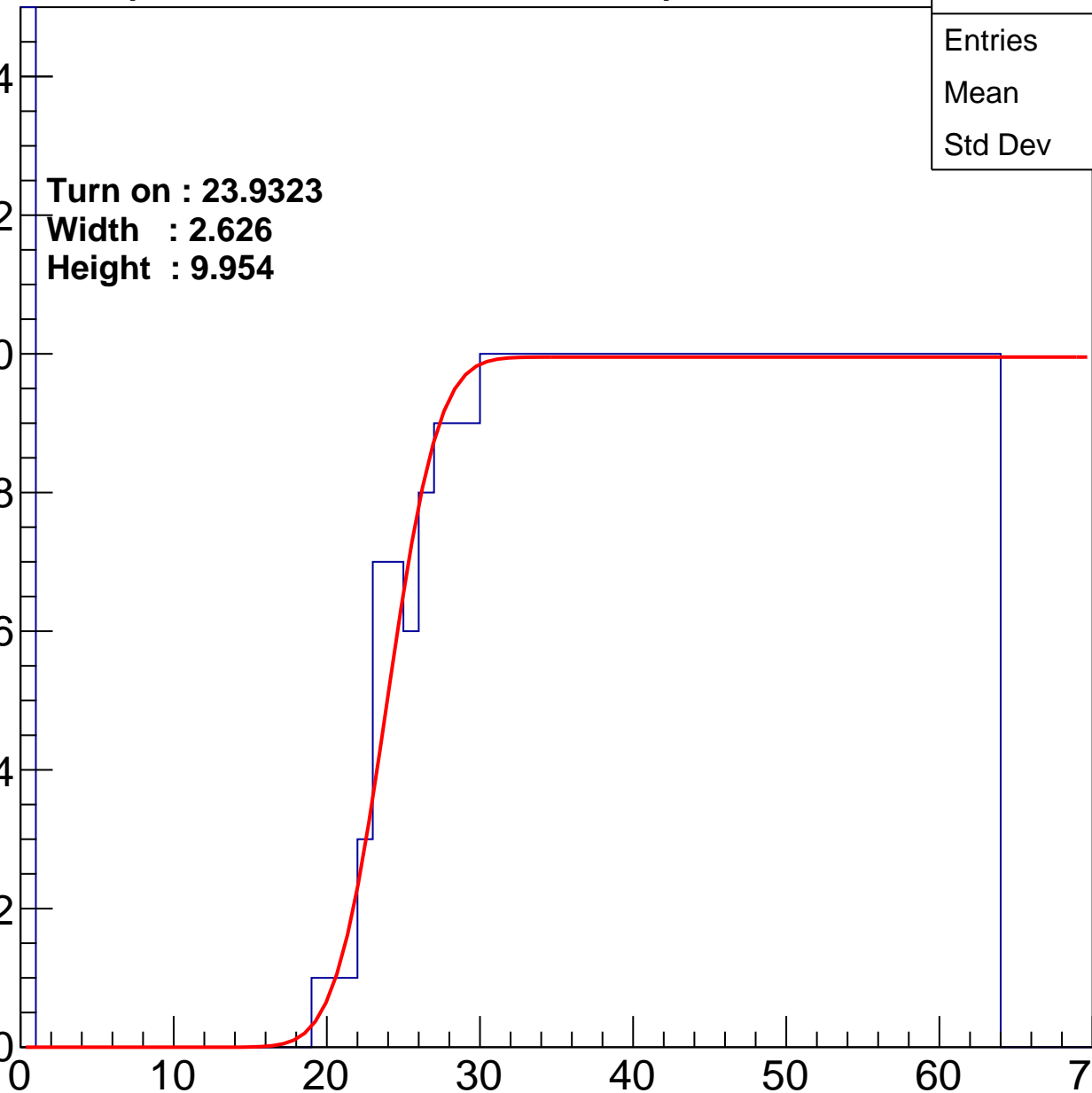
Width : 2.626

Height : 9.954

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch77

calib_packv5_041523_1651.root, FC#0, port C2

Entries	436
Mean	38.16
Std Dev	18.86

Turn on : 26.7276

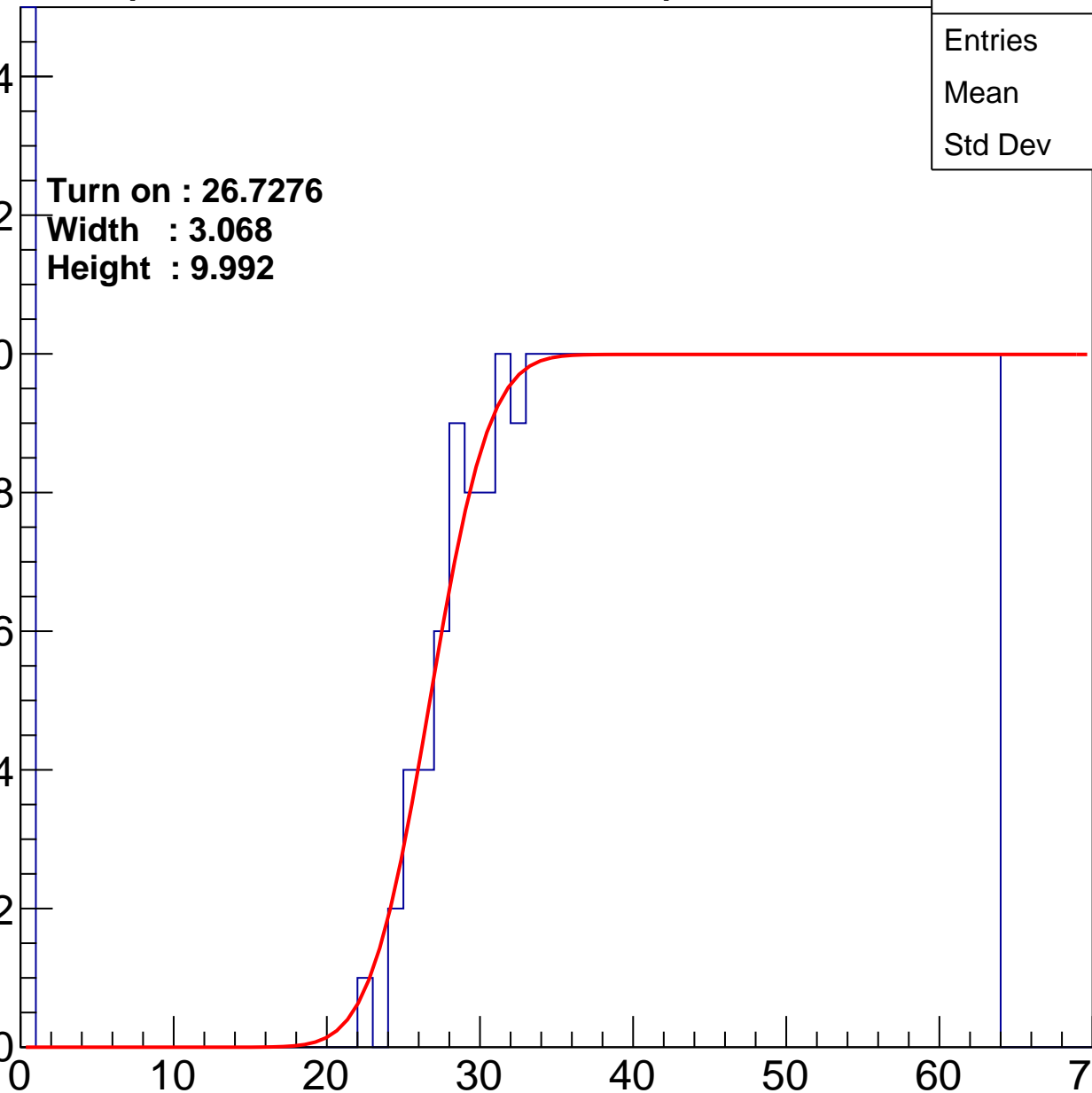
Width : 3.068

Height : 9.992

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch78

calib_packv5_041523_1651.root, FC#0, port C2

Entries	453
Mean	38.72
Std Dev	17.16

Turn on : 24.0108

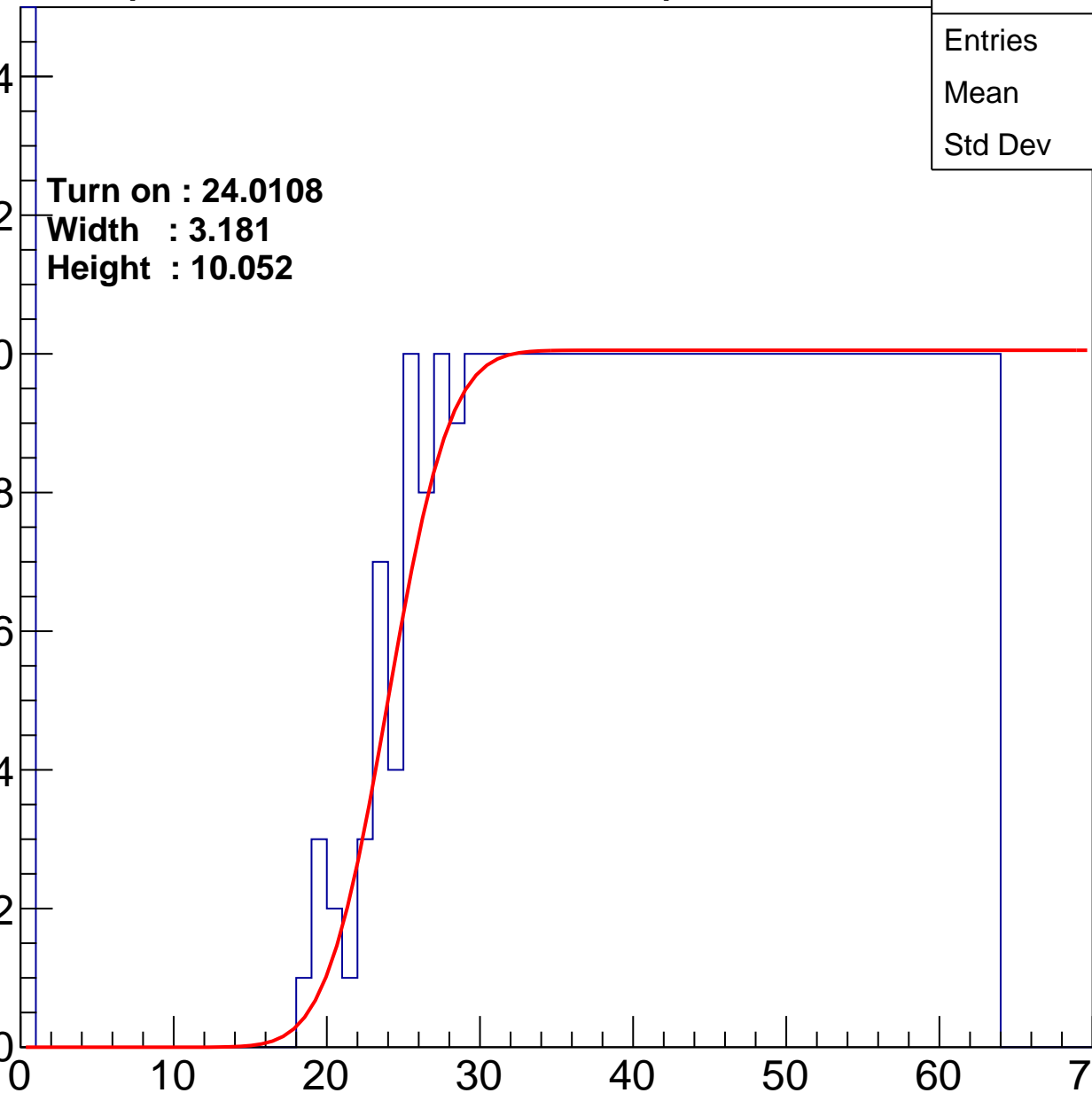
Width : 3.181

Height : 10.052

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch79

calib_packv5_041523_1651.root, FC#0, port C2

Entries	444
Mean	38.17
Std Dev	18.46

Turn on : 25.9626

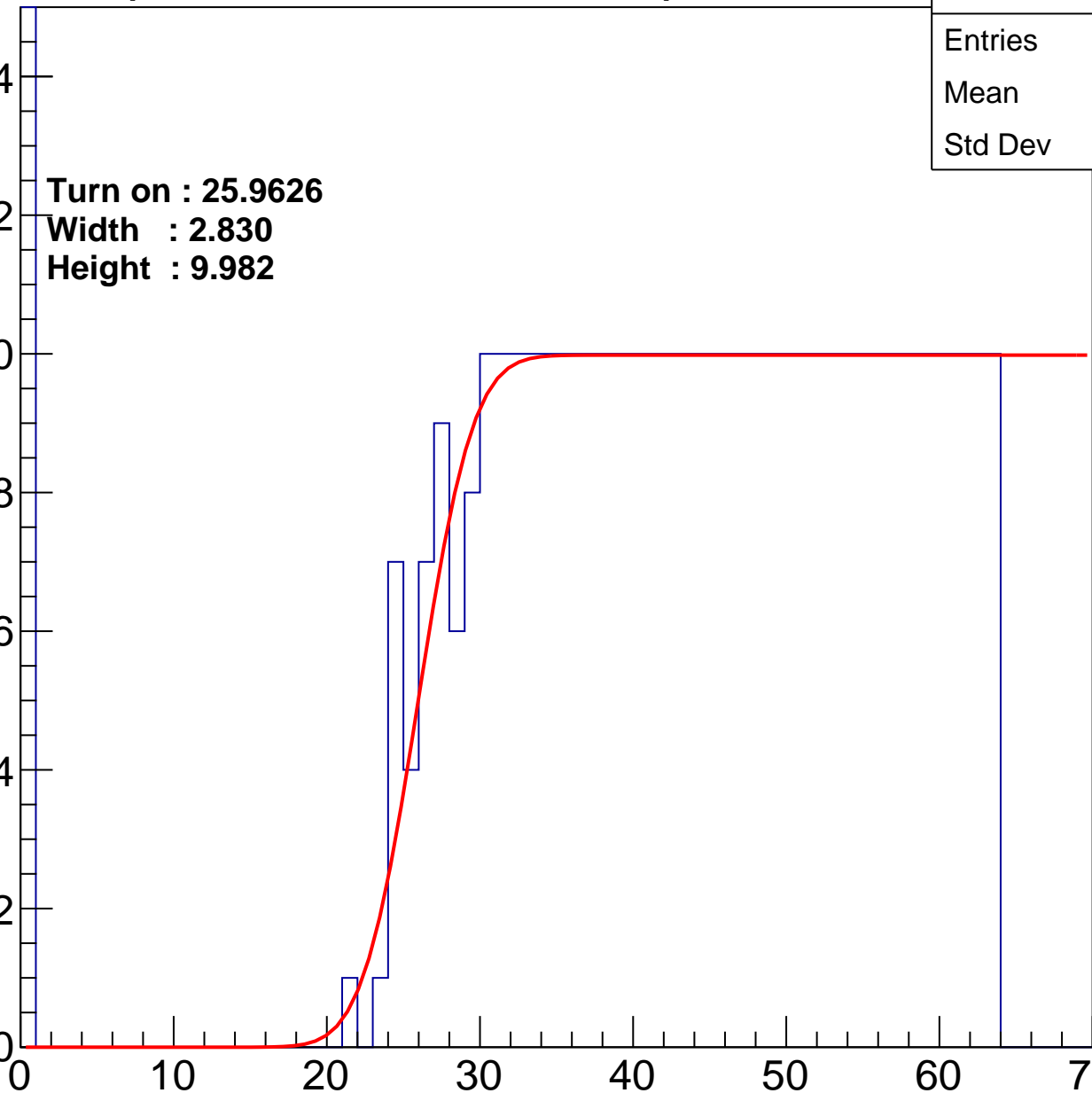
Width : 2.830

Height : 9.982

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch80

calib_packv5_041523_1651.root, FC#0, port C2

Entries	438
Mean	38.57
Std Dev	18.2

Turn on : 26.0225

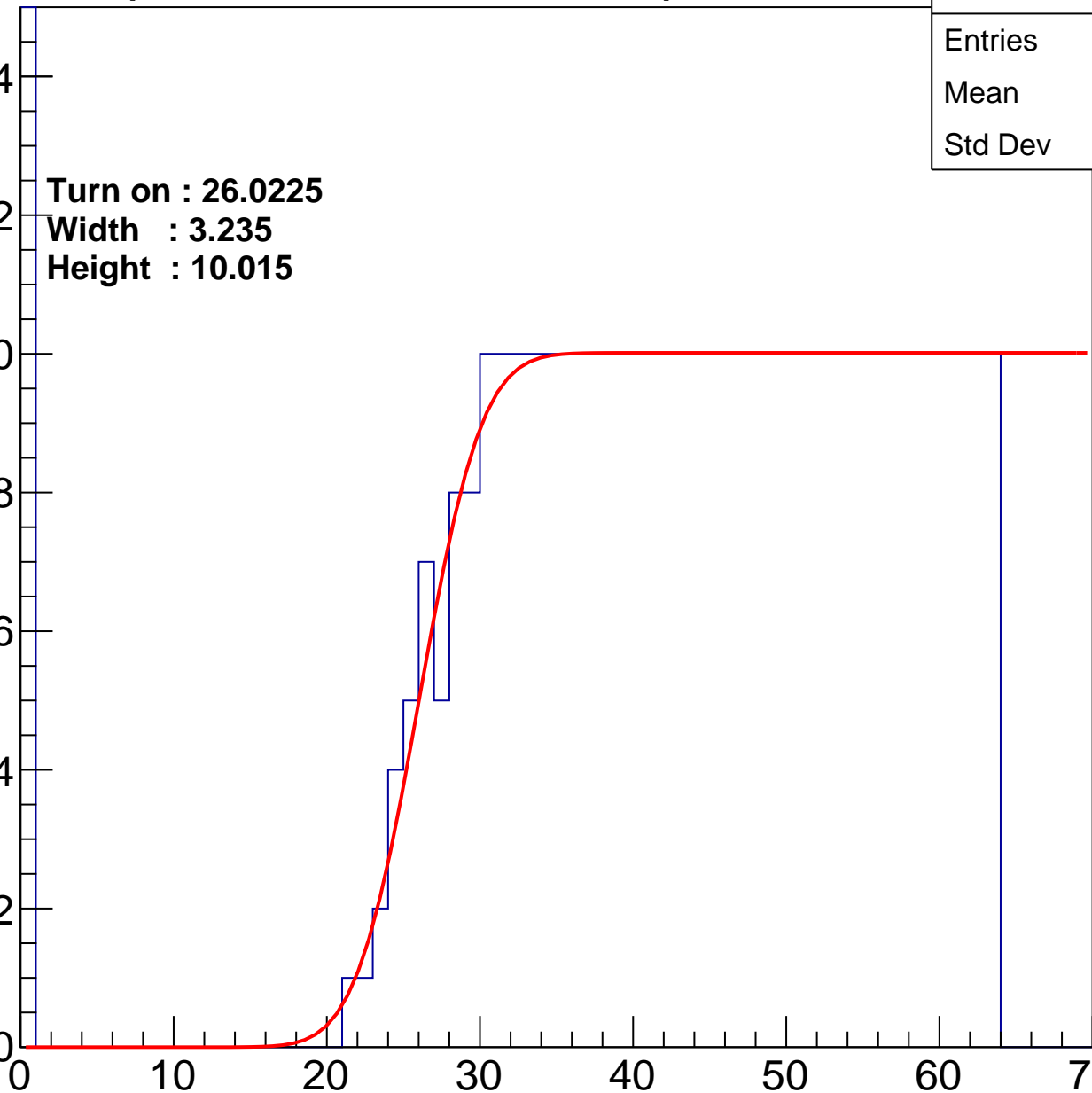
Width : 3.235

Height : 10.015

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch81

calib_packv5_041523_1651.root, FC#0, port C2

Entries	420
Mean	39.09
Std Dev	18.4

Turn on : 27.7608

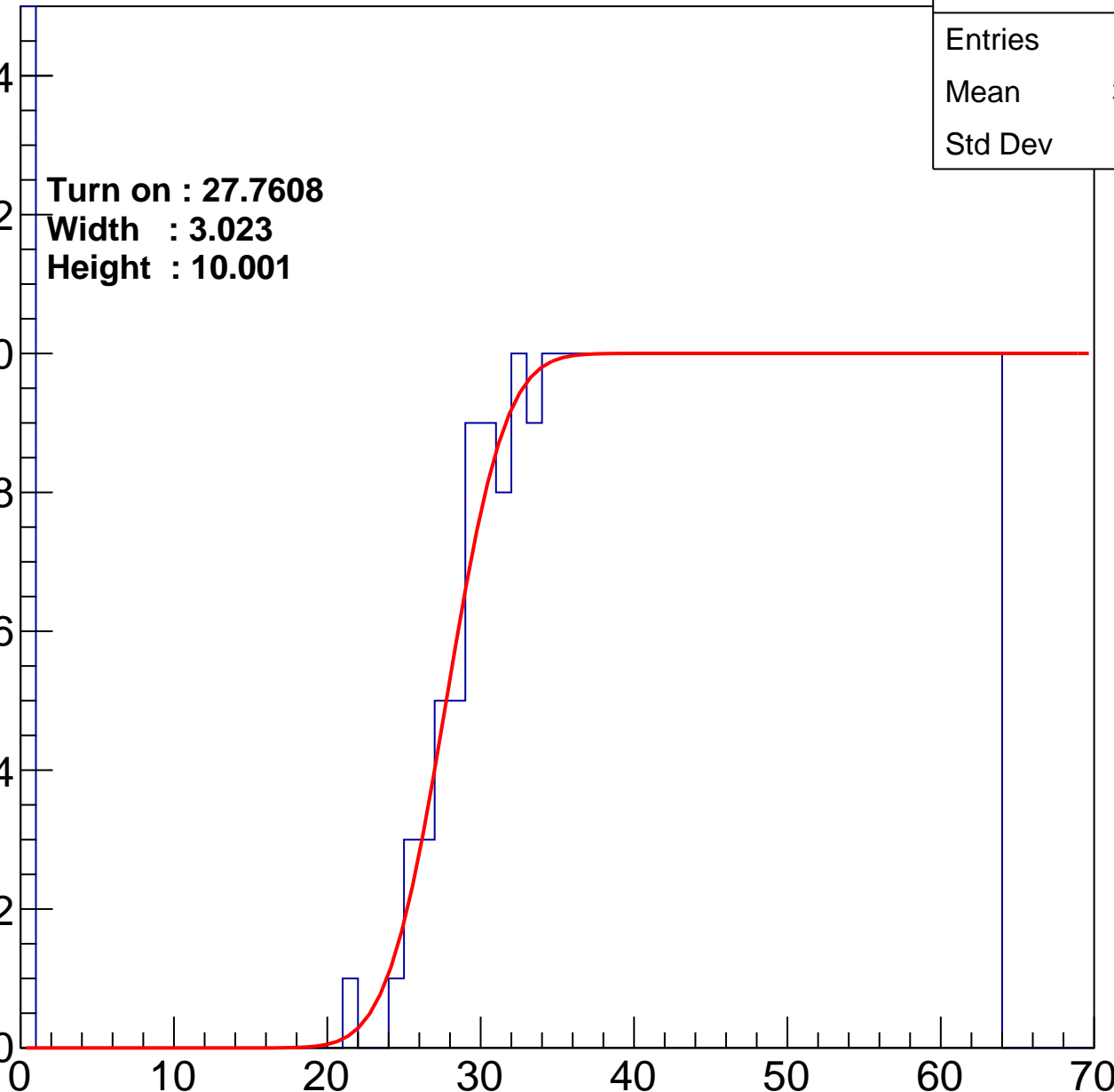
Width : 3.023

Height : 10.001

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch82

calib_packv5_041523_1651.root, FC#0, port C2

Entries	455
Mean	37.48
Std Dev	18.77

Turn on : 25.4611

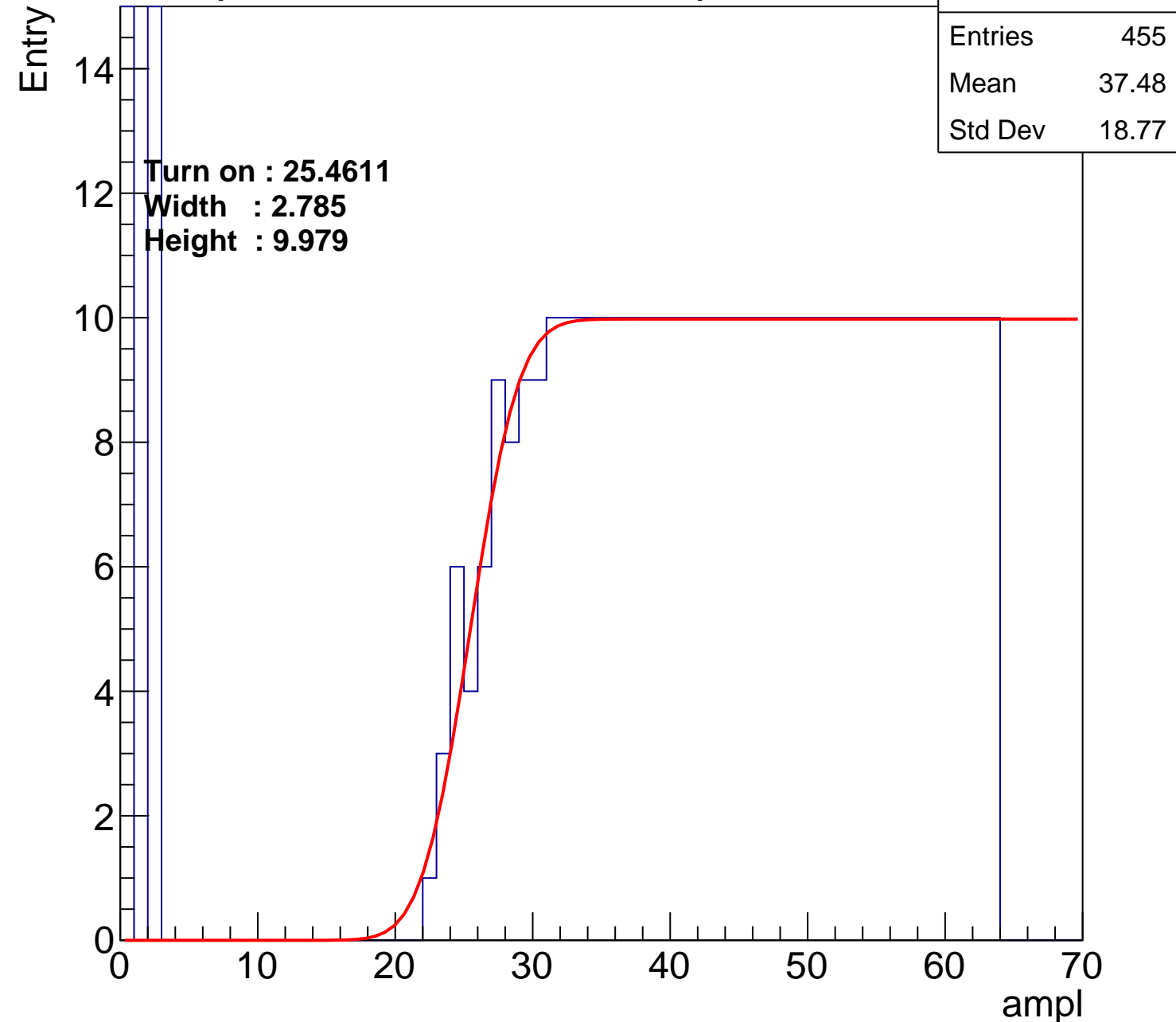
Width : 2.785

Height : 9.979

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch83

calib_packv5_041523_1651.root, FC#0, port C2

Entries	438
Mean	38.05
Std Dev	18.92

Turn on : 27.4609

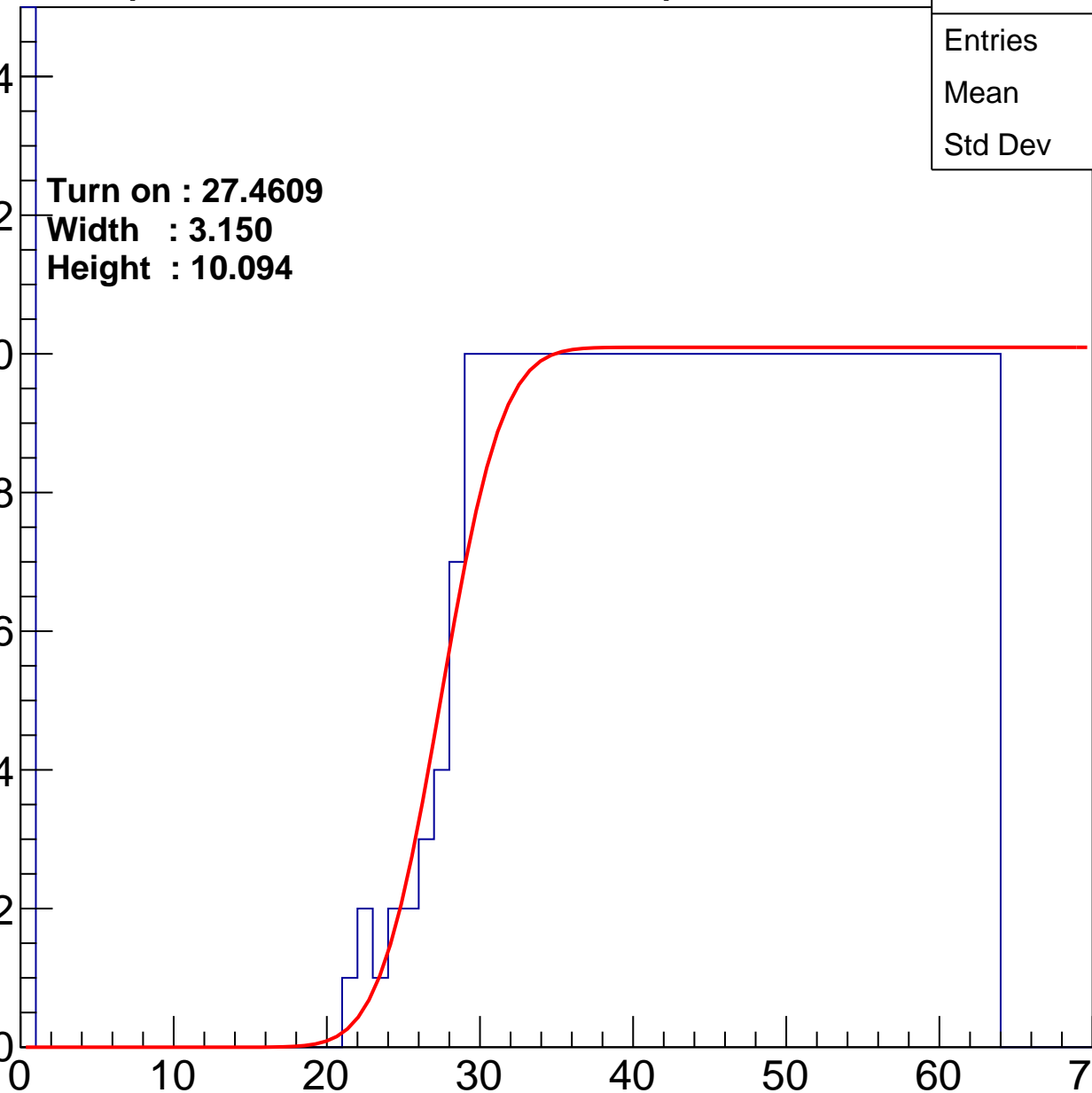
Width : 3.150

Height : 10.094

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch84

calib_packv5_041523_1651.root, FC#0, port C2

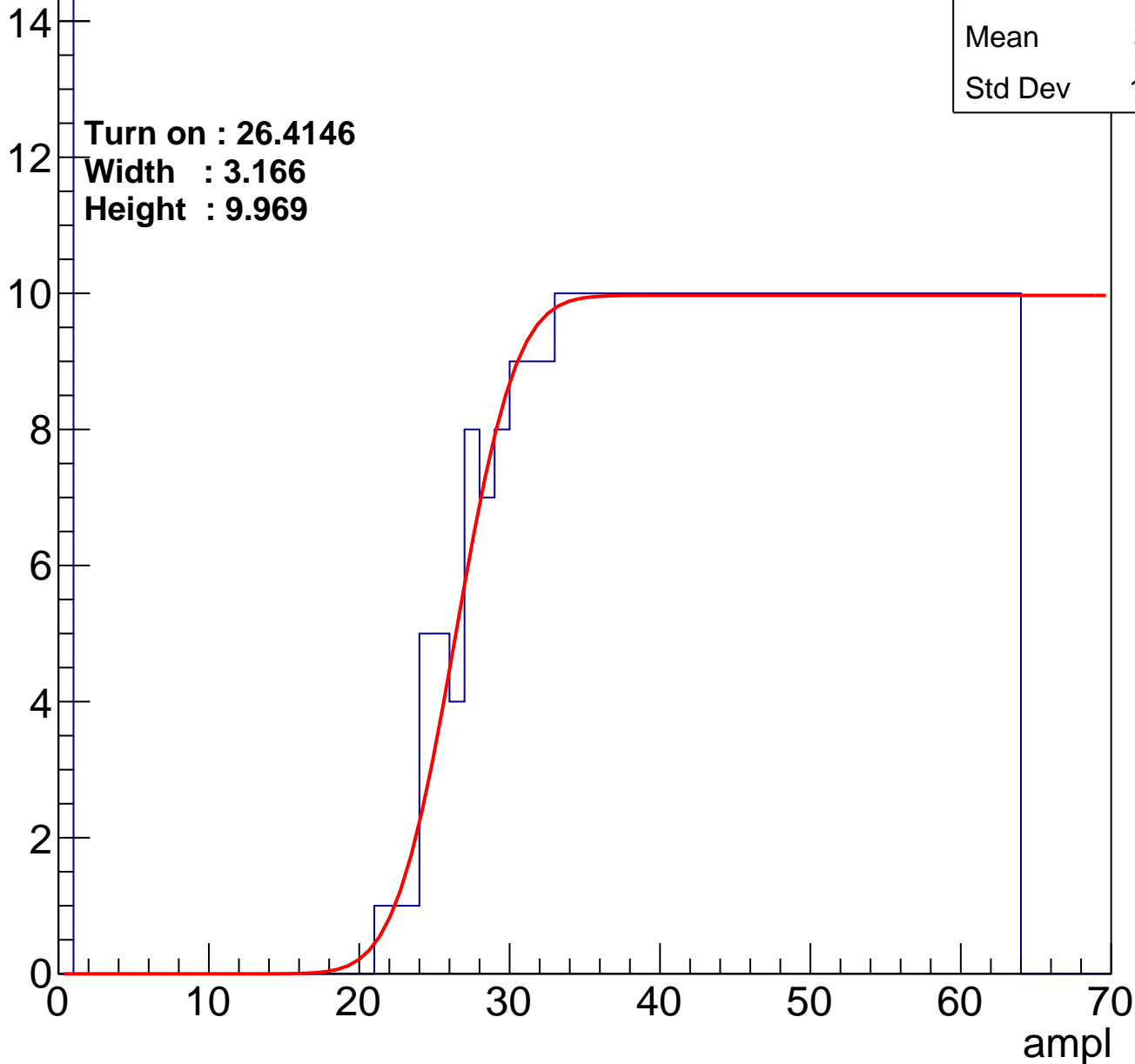
Entry

Entries	430
Mean	39.01
Std Dev	17.96

Turn on : 26.4146

Width : 3.166

Height : 9.969



B1L103S, U5-ch85

calib_packv5_041523_1651.root, FC#0, port C2

Entries	442
Mean	38.09
Std Dev	18.66

Turn on : 26.3527

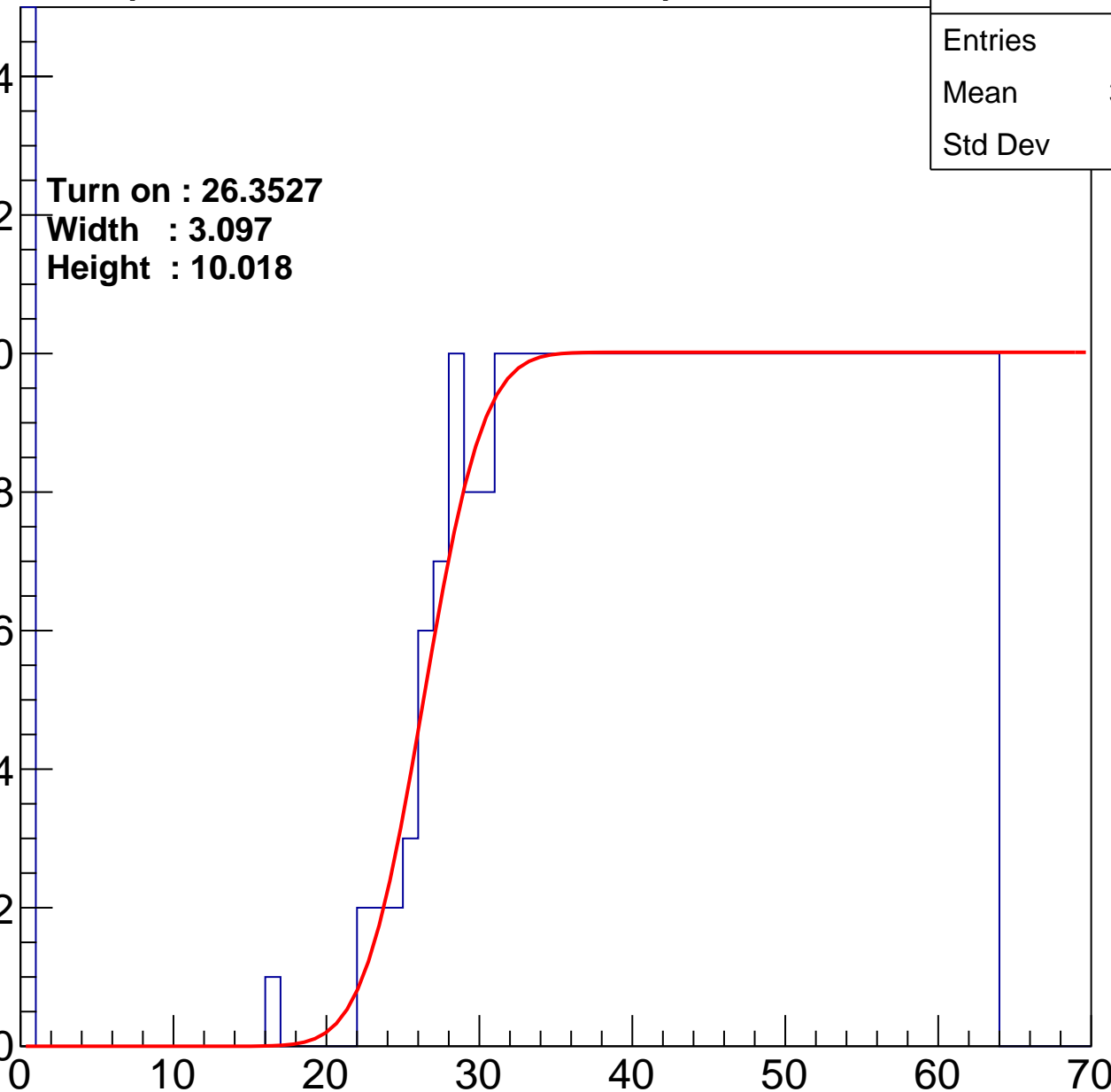
Width : 3.097

Height : 10.018

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch86

calib_packv5_041523_1651.root, FC#0, port C2

Entries	428
Mean	39.81
Std Dev	16.92

Turn on : 25.6570

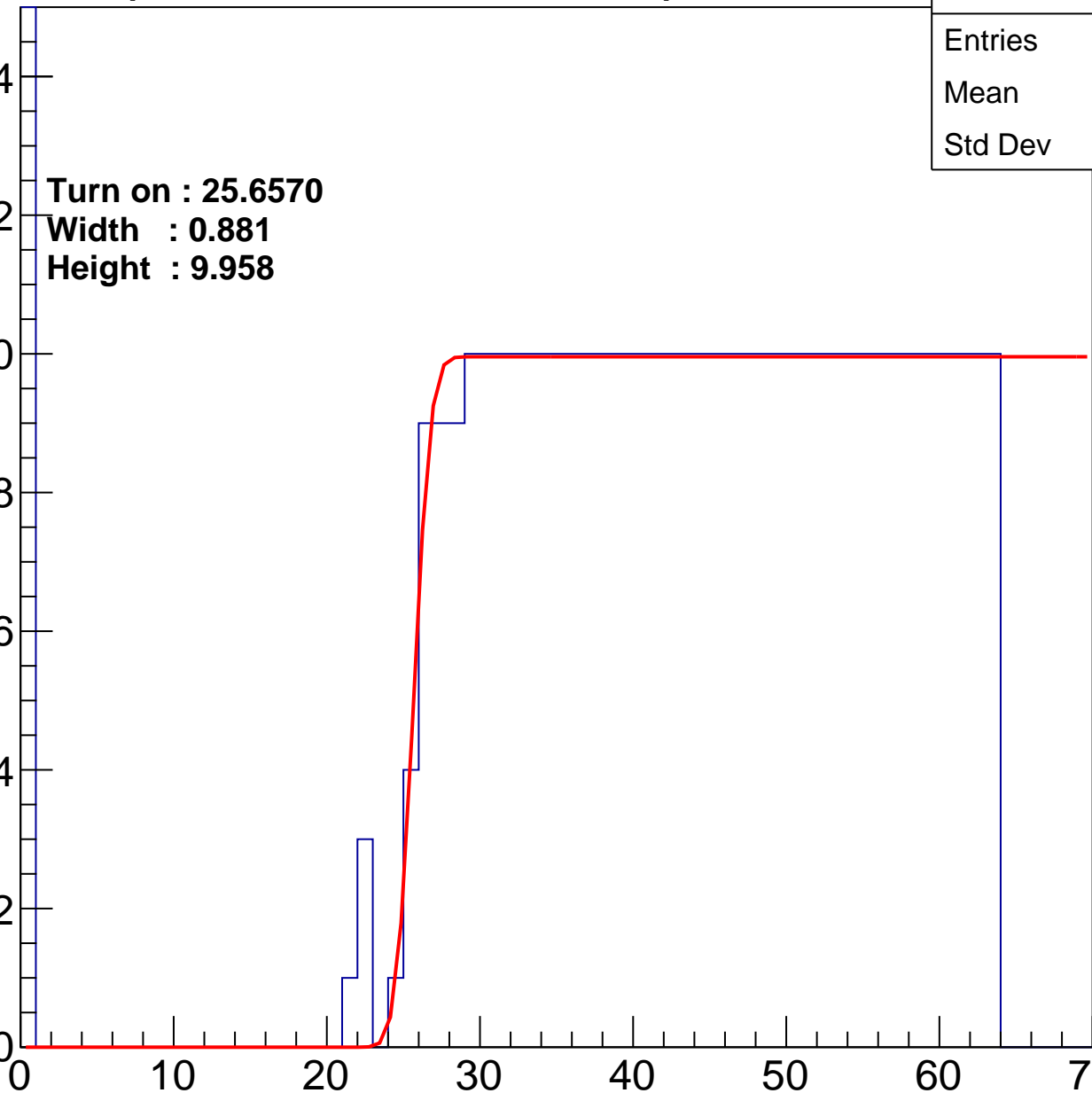
Width : 0.881

Height : 9.958

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch87

calib_packv5_041523_1651.root, FC#0, port C2

Entries	434
Mean	38.86
Std Dev	17.99

Turn on : 26.0127

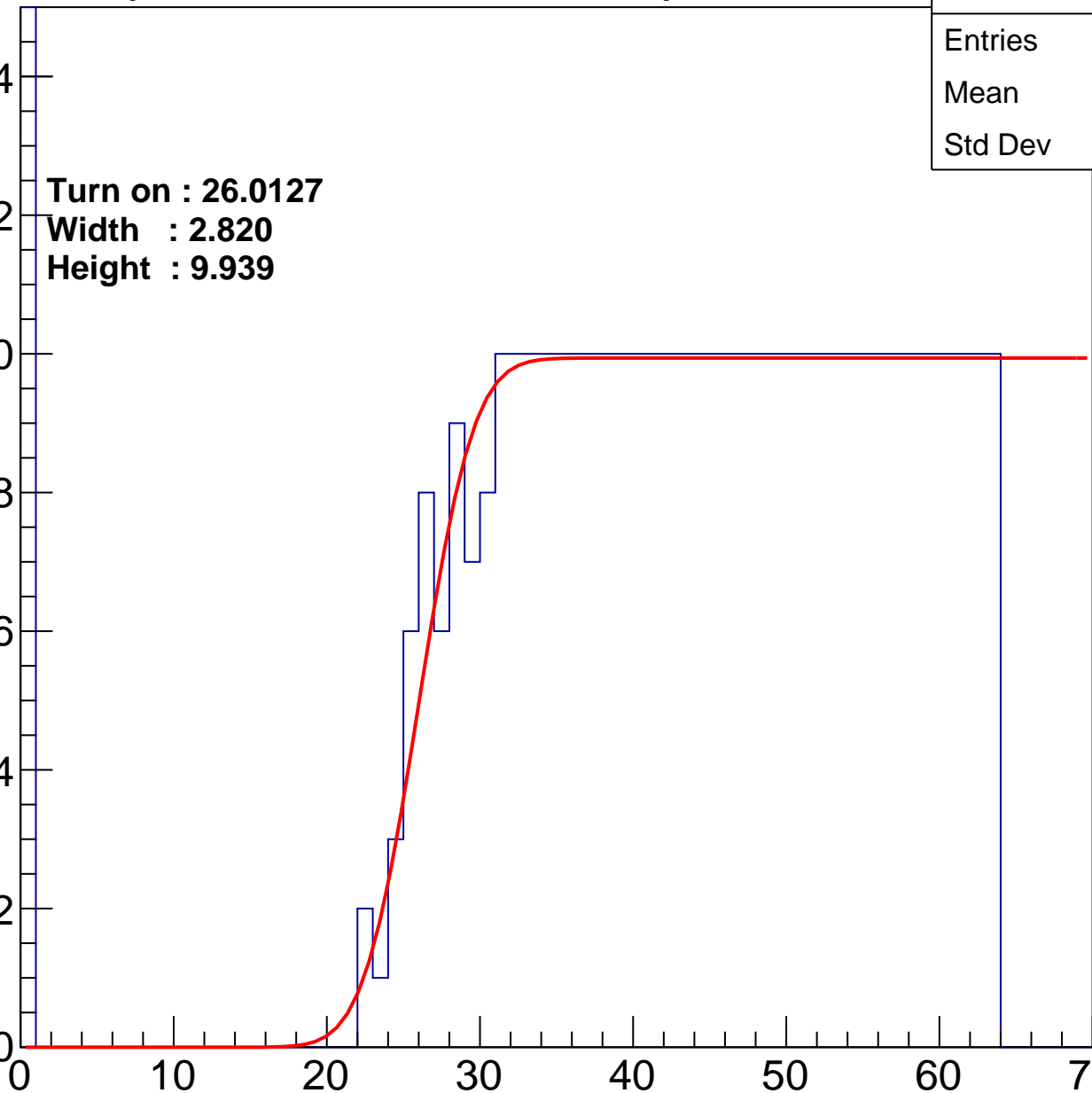
Width : 2.820

Height : 9.939

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch88

calib_packv5_041523_1651.root, FC#0, port C2

Entries	450
Mean	37.84
Std Dev	18.58

Turn on : 25.1114

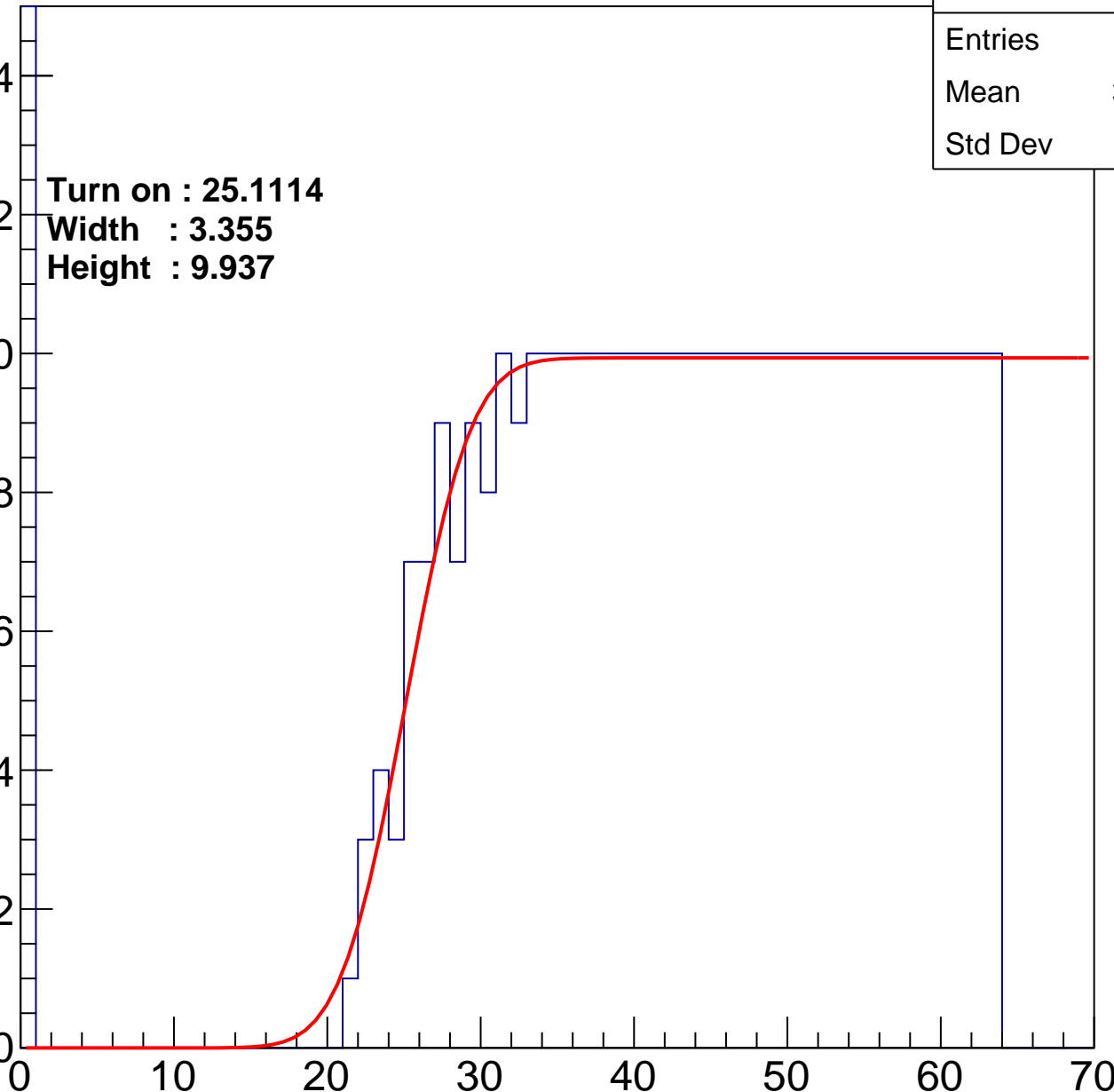
Width : 3.355

Height : 9.937

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch89

calib_packv5_041523_1651.root, FC#0, port C2

Entries	453
Mean	38.08
Std Dev	18.1

Turn on : 24.3993

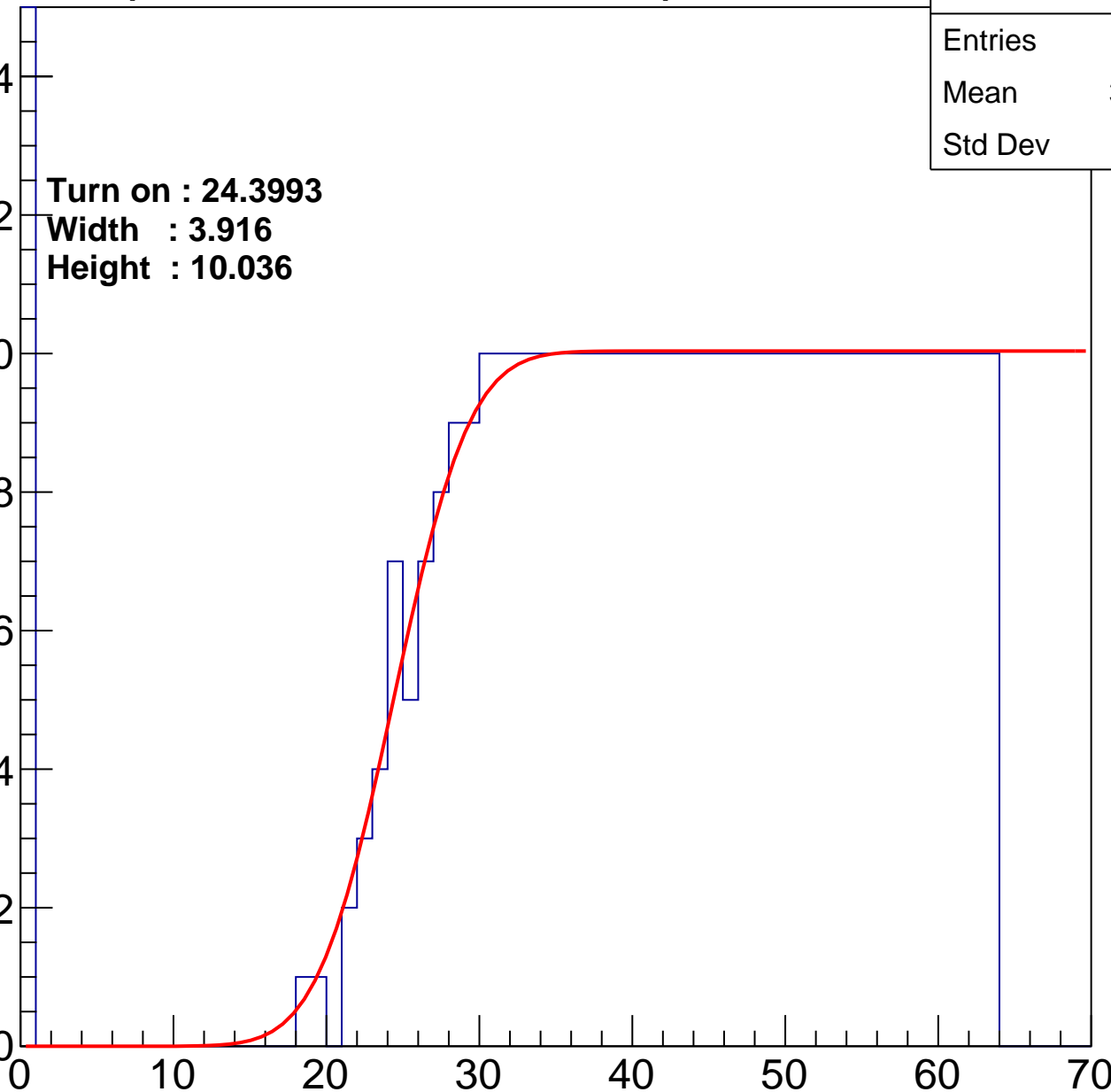
Width : 3.916

Height : 10.036

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch90

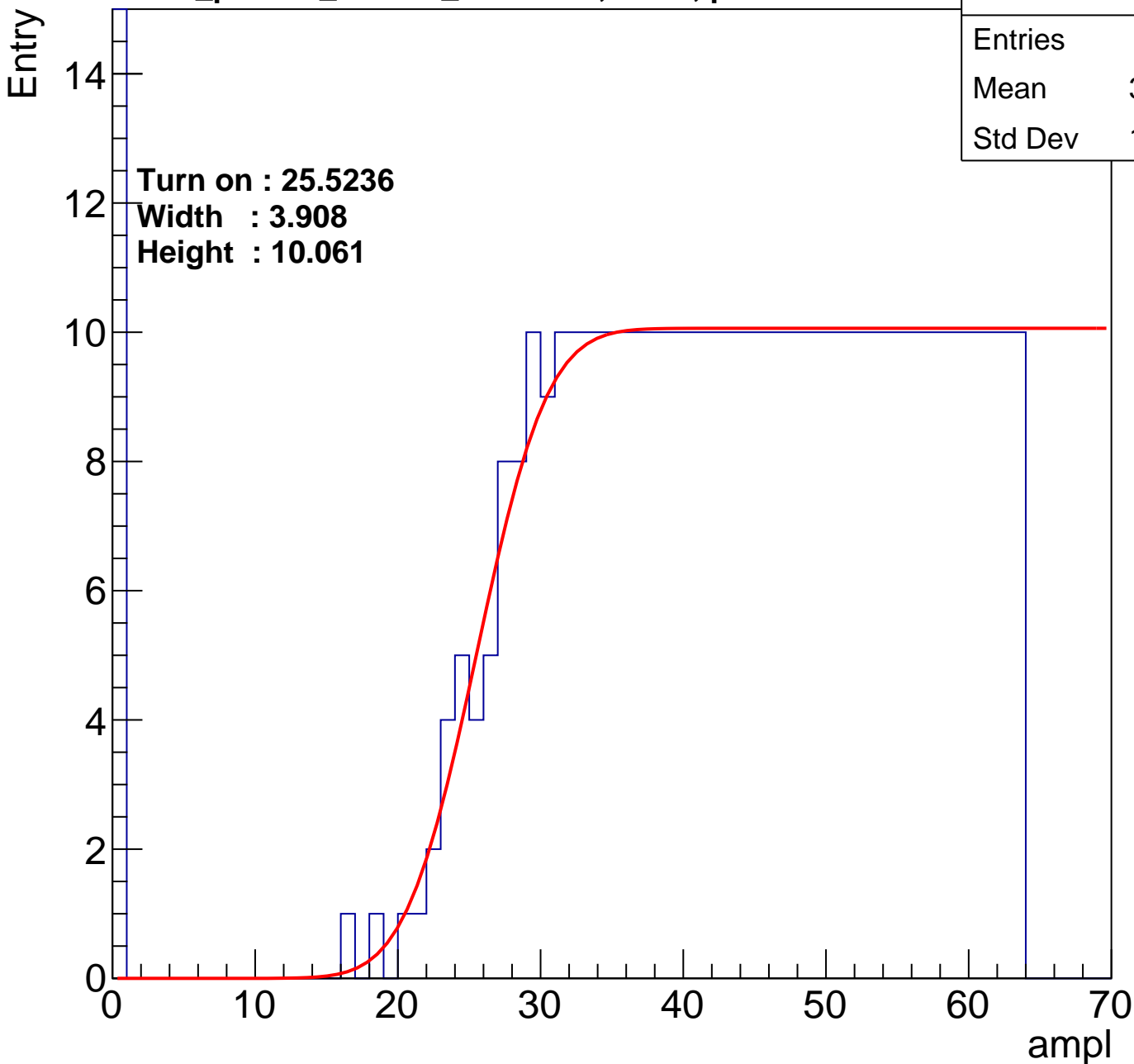
calib_packv5_041523_1651.root, FC#0, port C2

Entries	441
Mean	38.71
Std Dev	17.81

Turn on : 25.5236

Width : 3.908

Height : 10.061



B1L103S, U5-ch91

calib_packv5_041523_1651.root, FC#0, port C2

Entries	432
Mean	38.25
Std Dev	18.89

Turn on : 27.7957

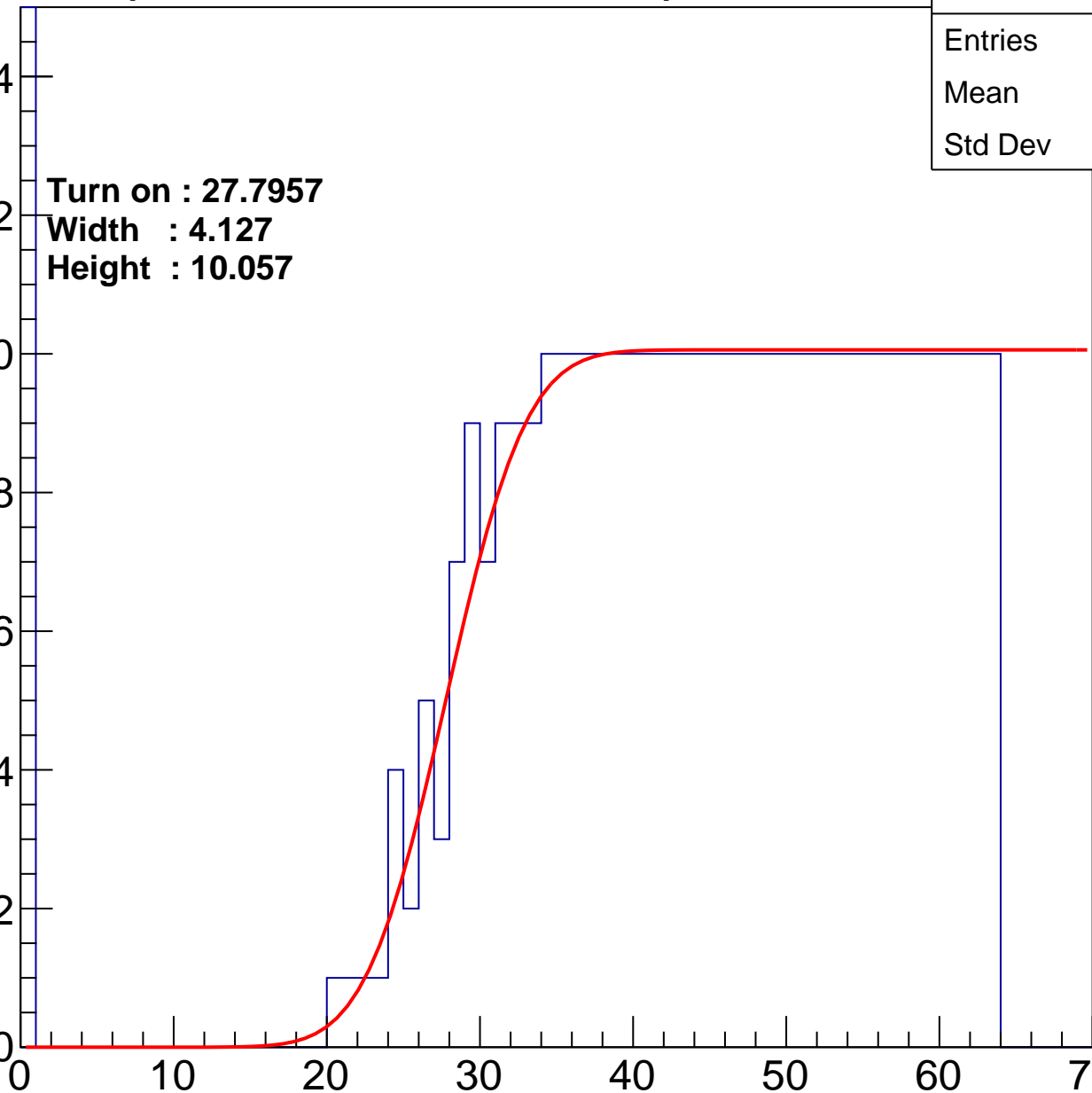
Width : 4.127

Height : 10.057

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch92

calib_packv5_041523_1651.root, FC#0, port C2

Entries	453
Mean	38.31
Std Dev	17.78

Turn on : 23.4252

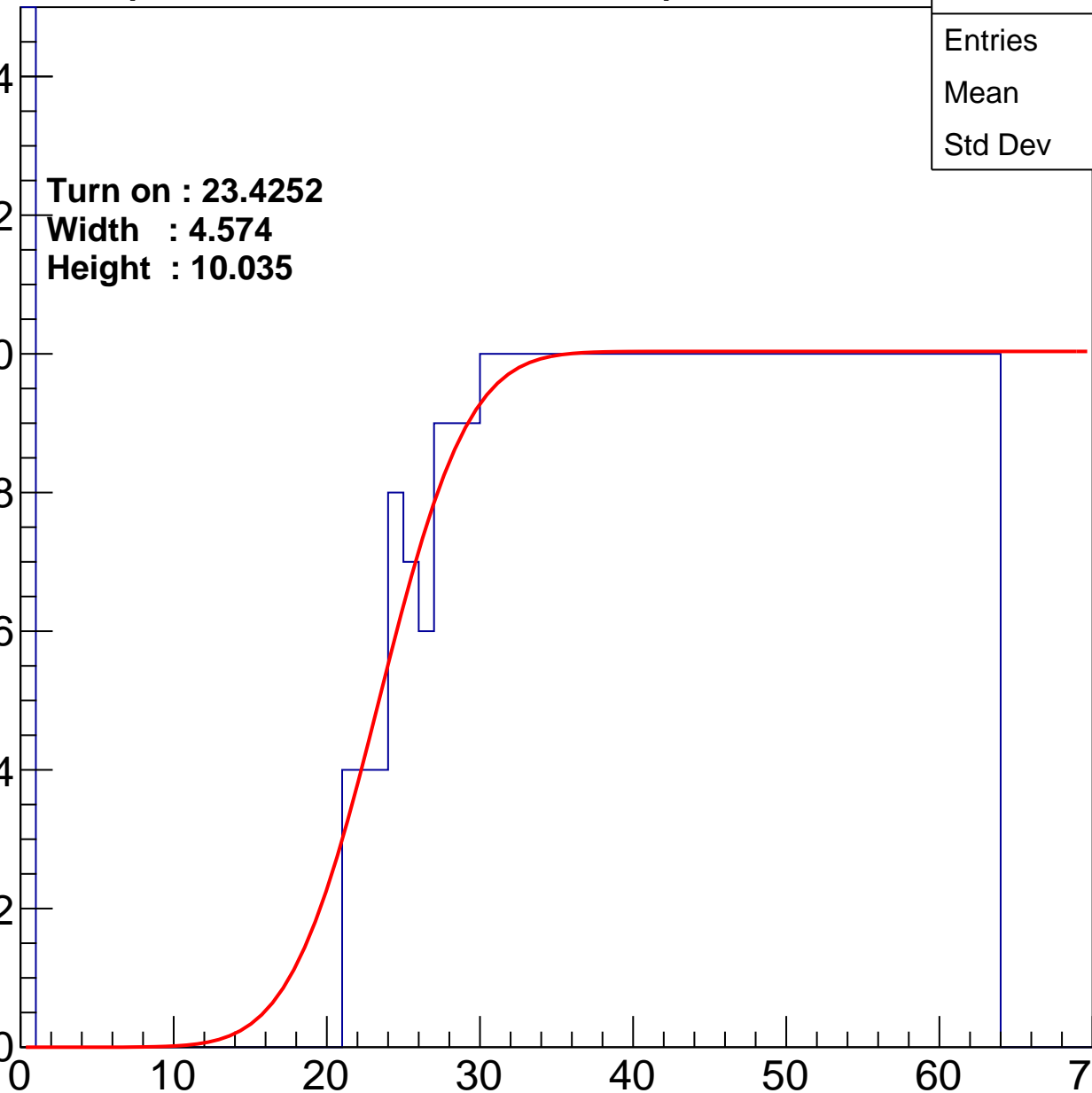
Width : 4.574

Height : 10.035

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch93

calib_packv5_041523_1651.root, FC#0, port C2

Entries	432
Mean	38.78
Std Dev	18.16

Turn on : 27.4233

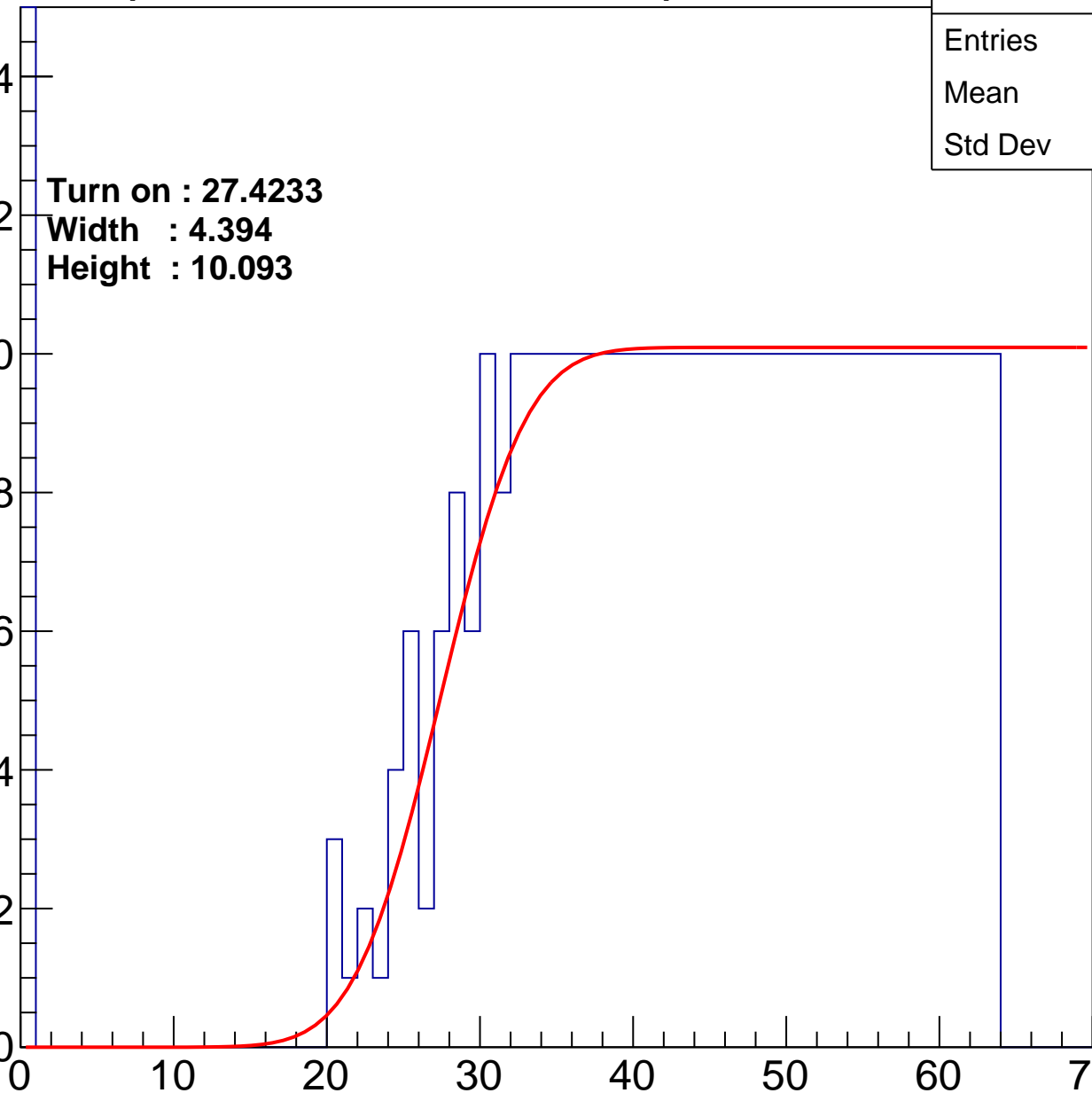
Width : 4.394

Height : 10.093

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch94

calib_packv5_041523_1651.root, FC#0, port C2

Entries	446
Mean	38.34
Std Dev	18.09

Turn on : 23.8309

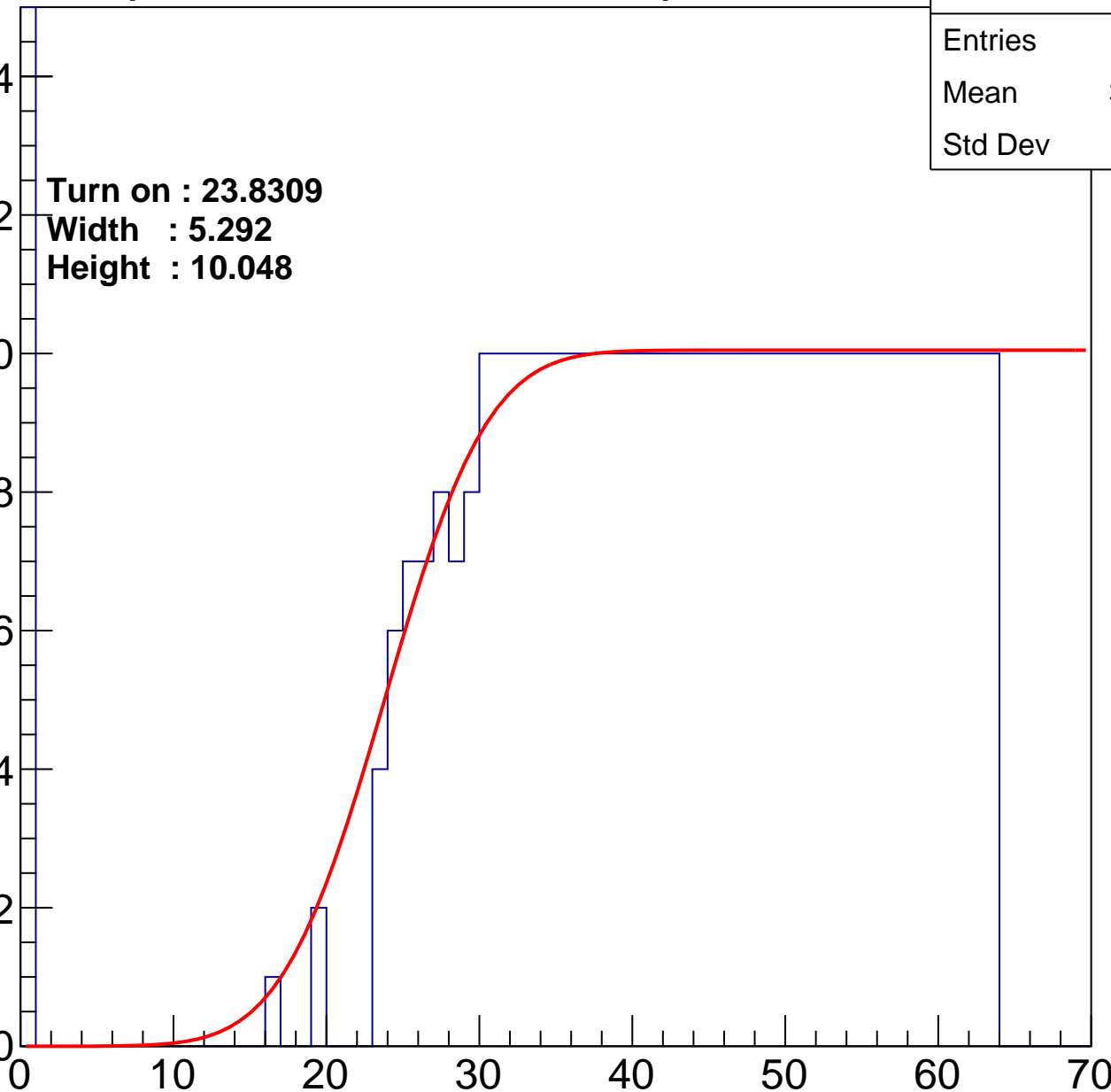
Width : 5.292

Height : 10.048

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch95

calib_packv5_041523_1651.root, FC#0, port C2

Entries	440
Mean	39
Std Dev	17.45

Turn on : 24.8003

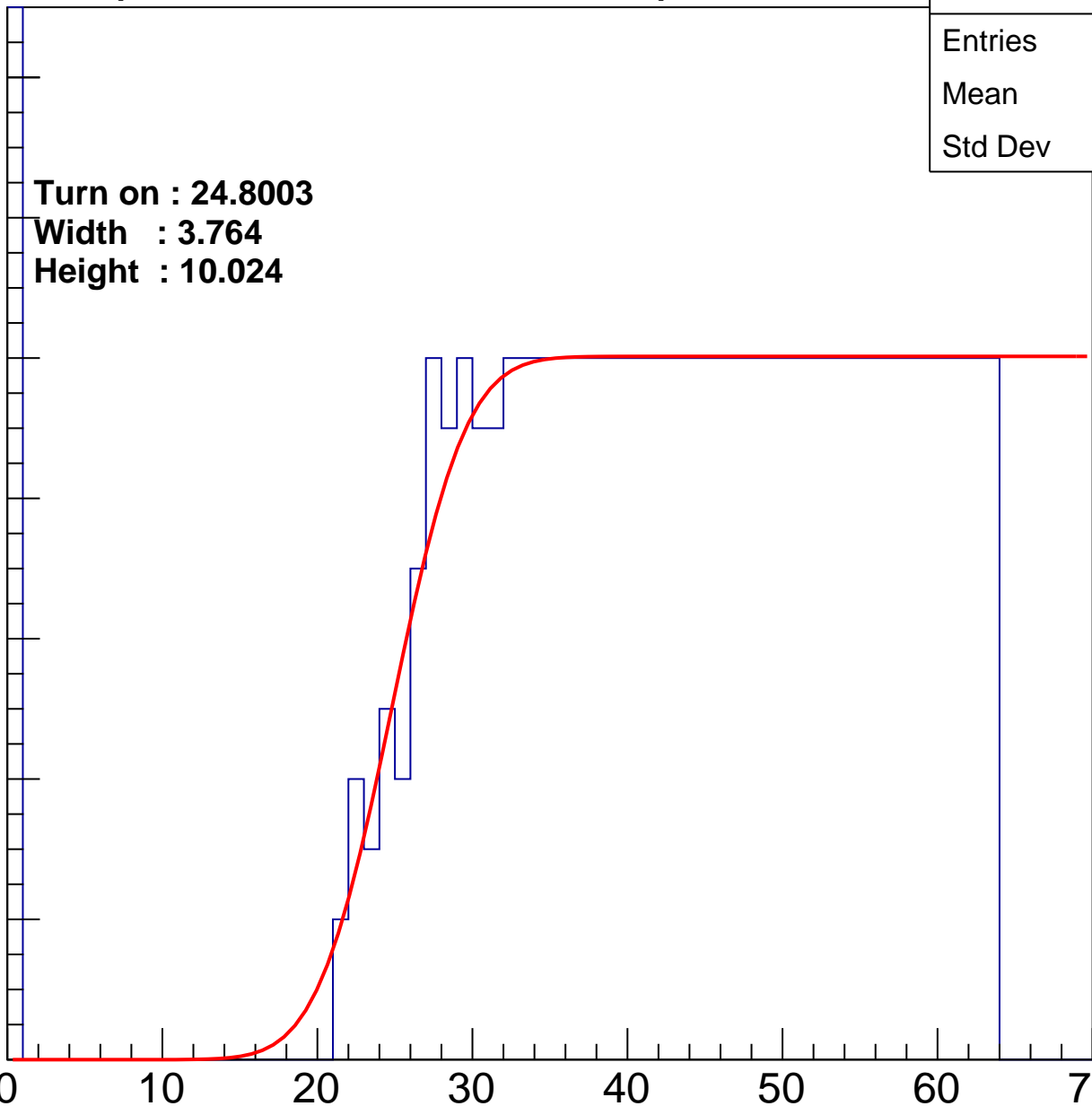
Width : 3.764

Height : 10.024

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch96

calib_packv5_041523_1651.root, FC#0, port C2

Entries	434
Mean	39.87
Std Dev	16.42

Turn on : 24.7802

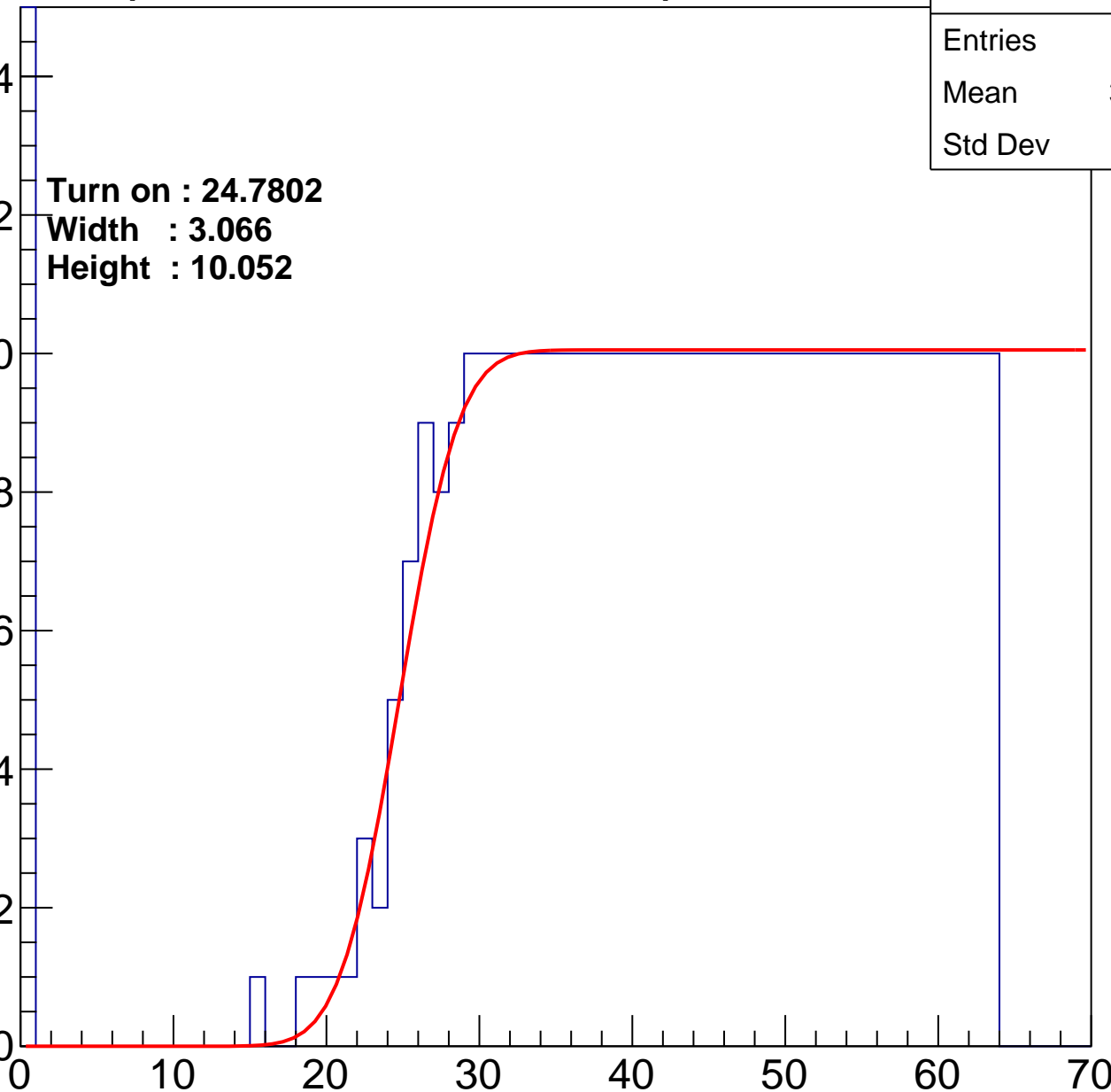
Width : 3.066

Height : 10.052

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch97

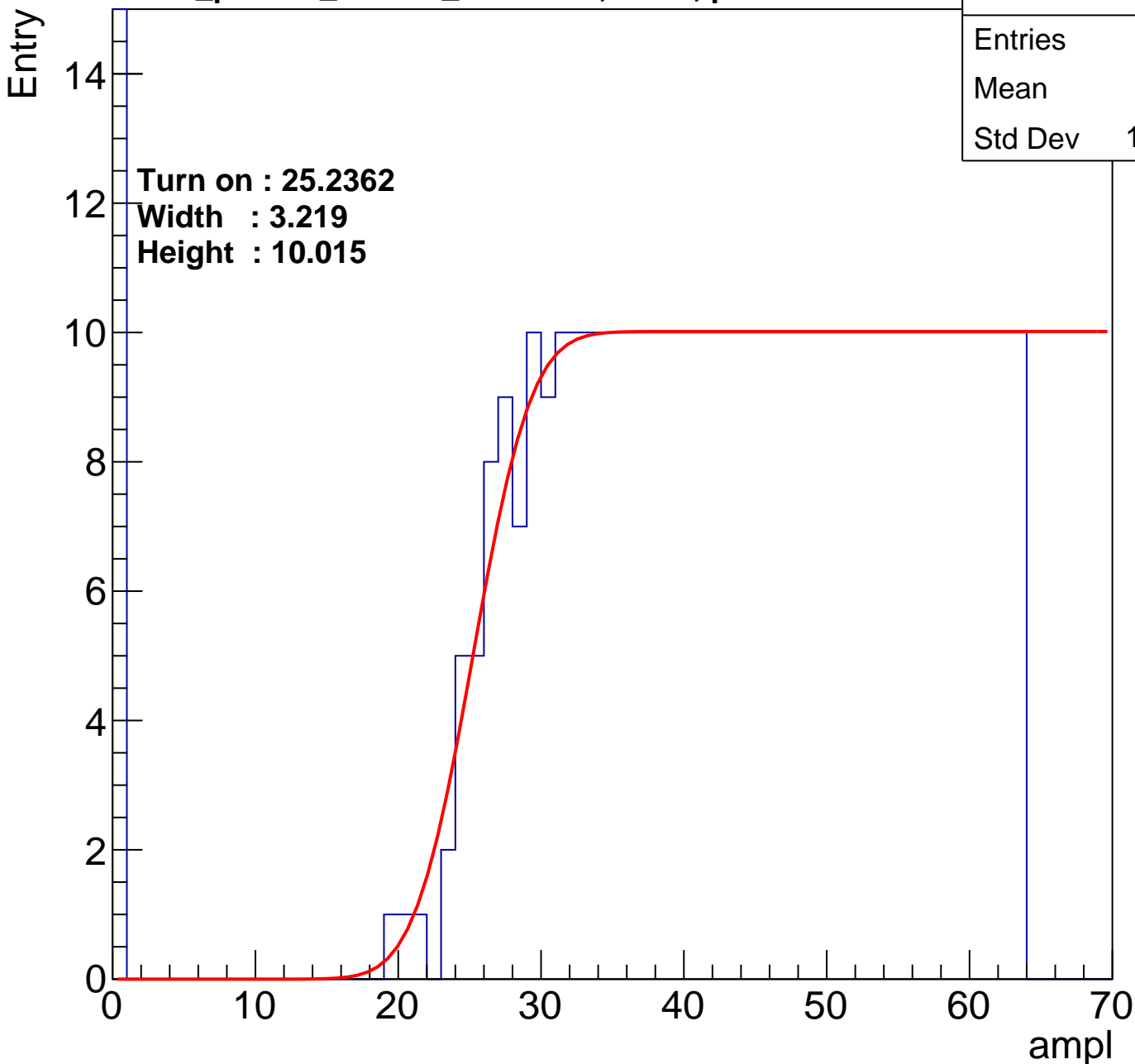
calib_packv5_041523_1651.root, FC#0, port C2

Entries	431
Mean	39.6
Std Dev	17.04

Turn on : 25.2362

Width : 3.219

Height : 10.015



B1L103S, U5-ch98

calib_packv5_041523_1651.root, FC#0, port C2

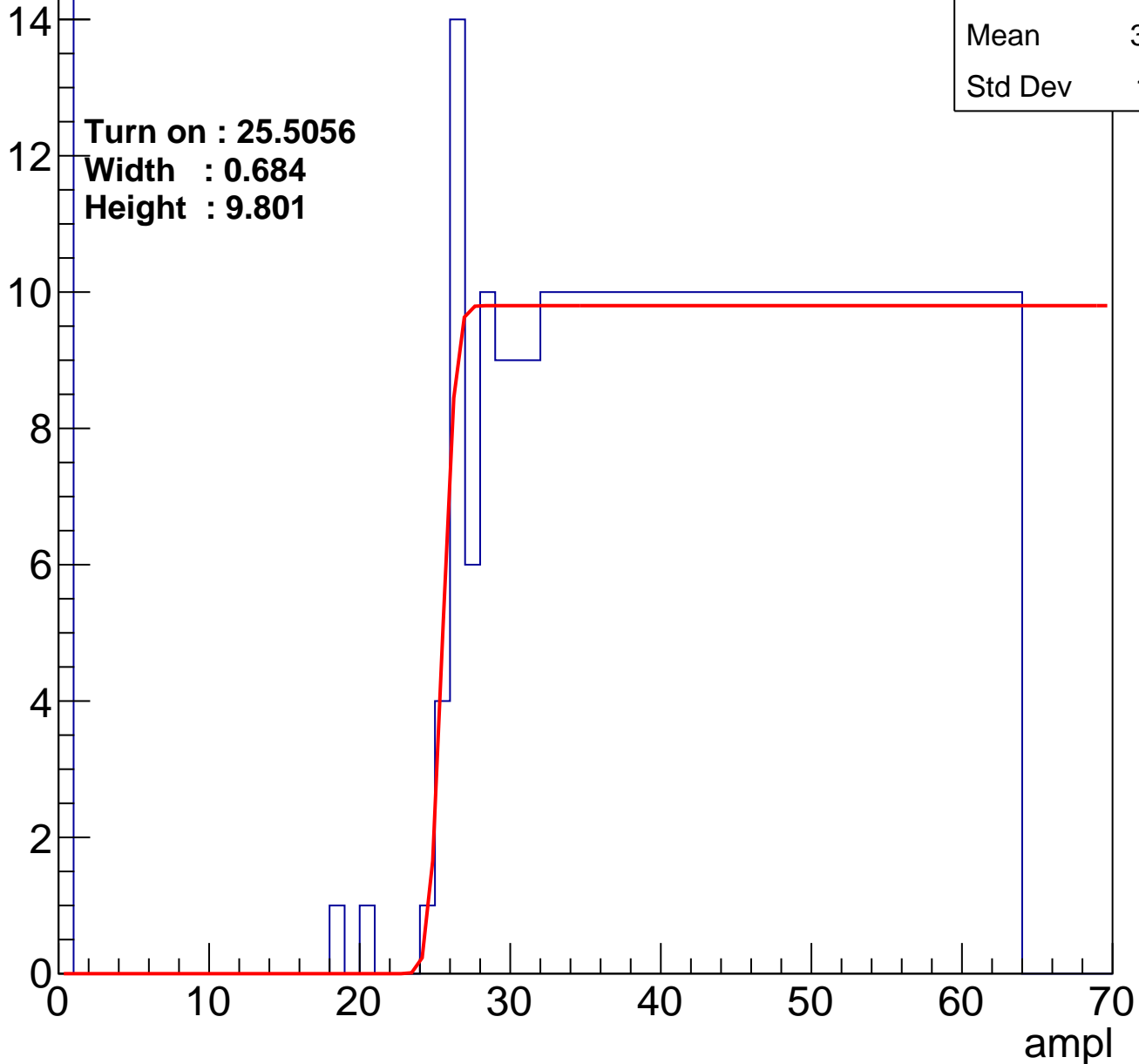
Entry

Entries	446
Mean	38.07
Std Dev	18.51

Turn on : 25.5056

Width : 0.684

Height : 9.801



B1L103S, U5-ch99

calib_packv5_041523_1651.root, FC#0, port C2

Entries	436
Mean	39.74
Std Dev	16.5

Turn on : 23.9034

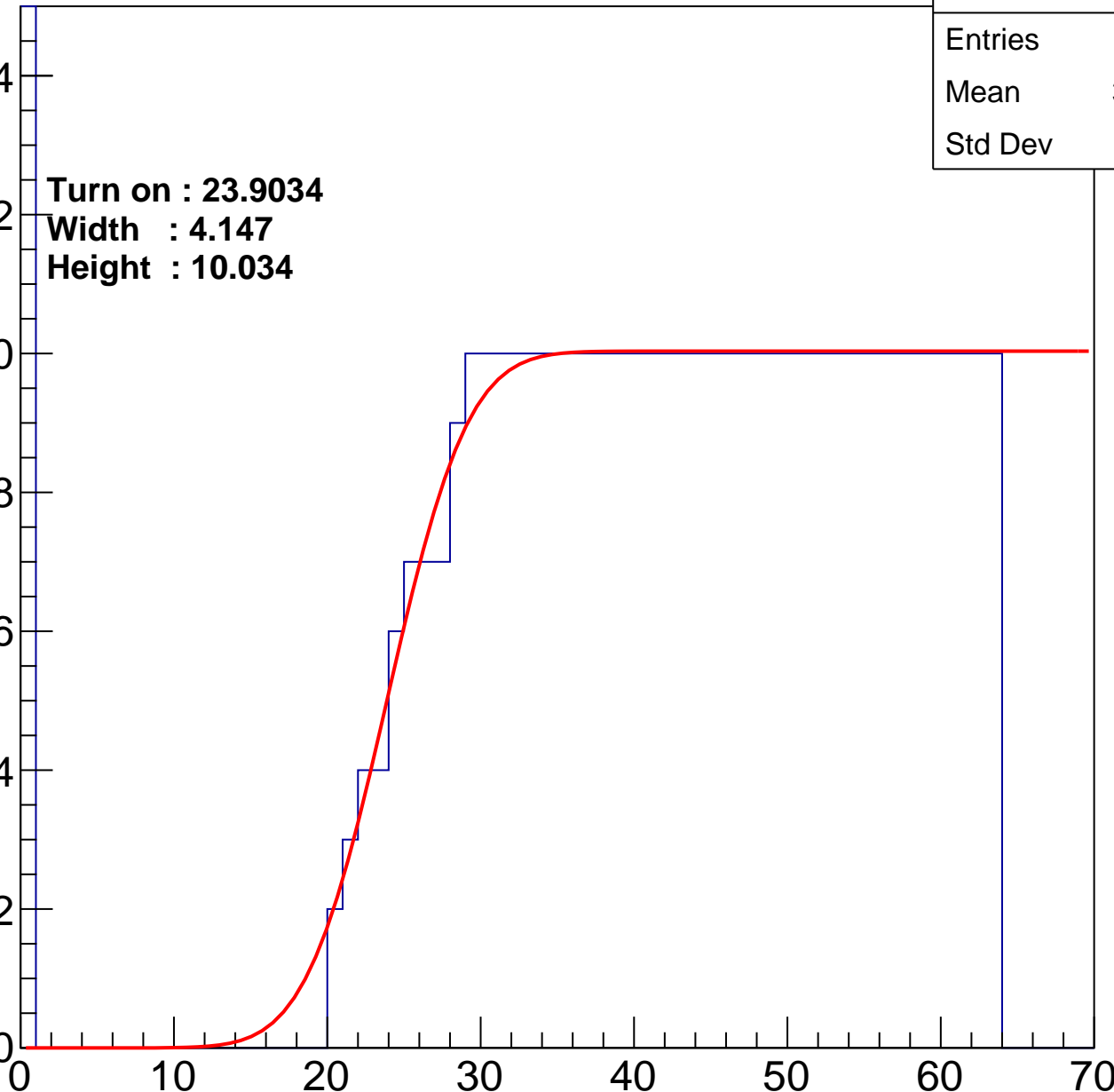
Width : 4.147

Height : 10.034

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch100

calib_packv5_041523_1651.root, FC#0, port C2

Entries	436
Mean	39.09
Std Dev	17.55

Turn on : 25.8348

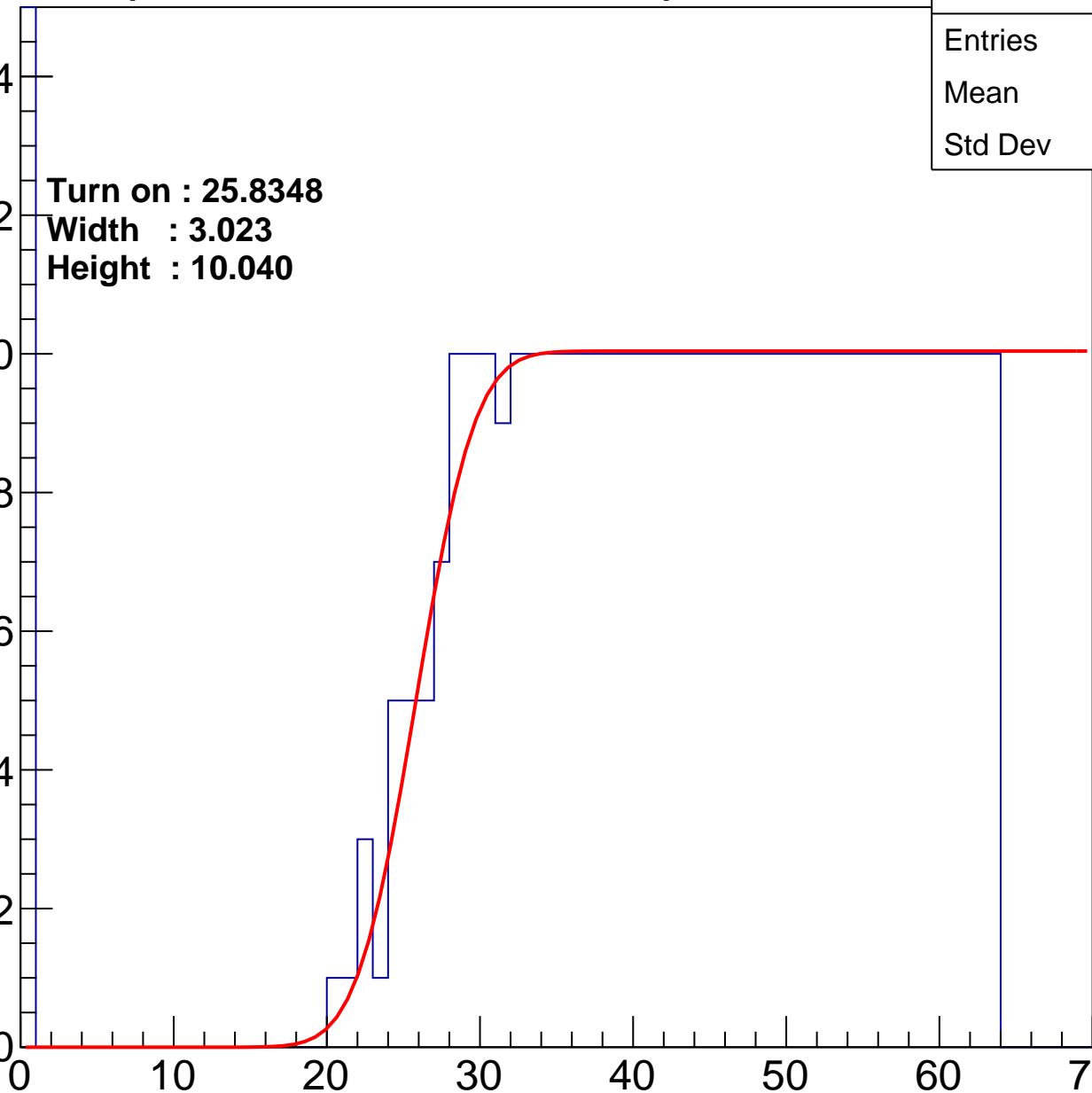
Width : 3.023

Height : 10.040

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch101

calib_packv5_041523_1651.root, FC#0, port C2

Entries	449
Mean	38.11
Std Dev	18.23

Turn on : 24.8286

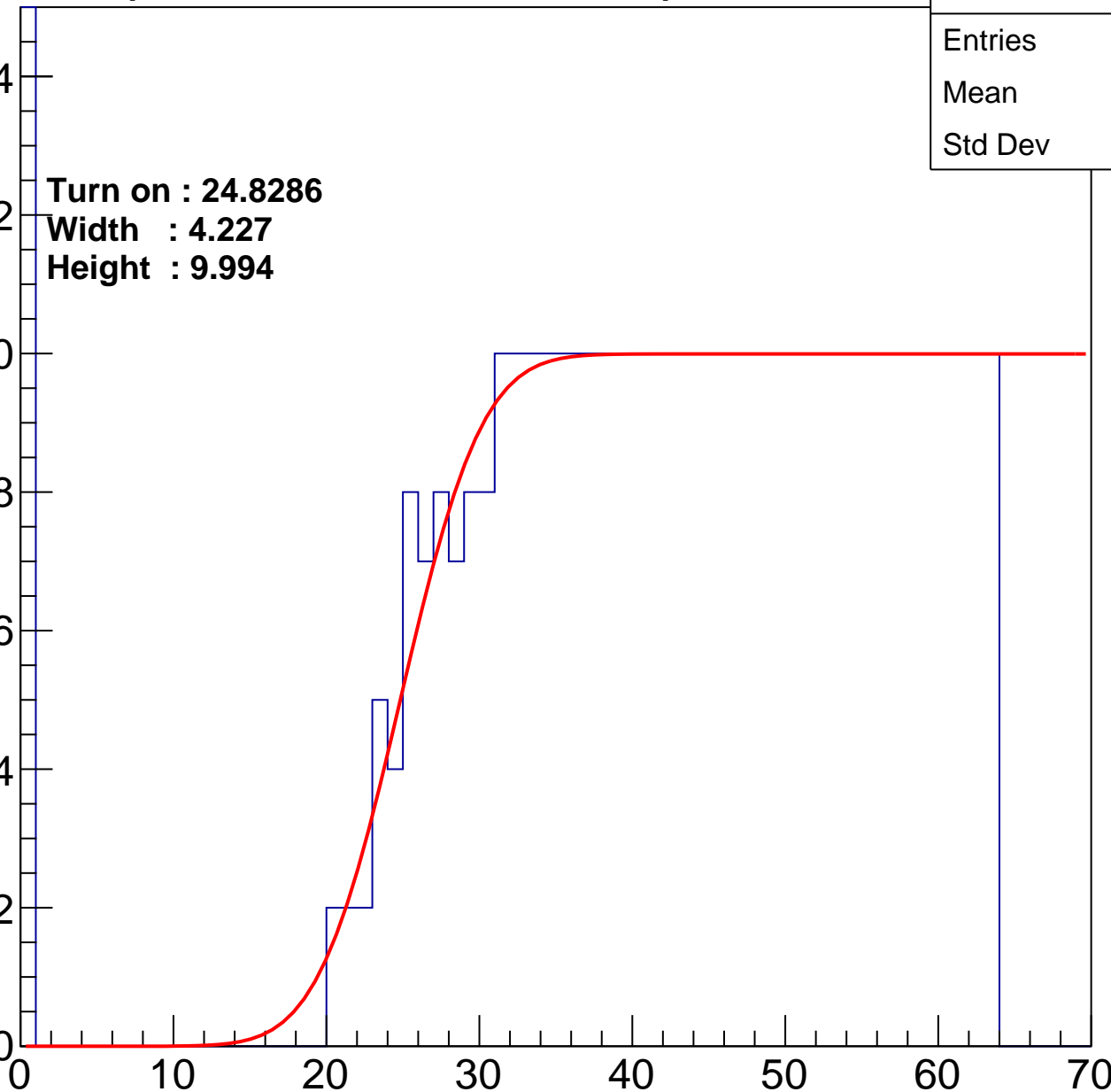
Width : 4.227

Height : 9.994

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch102

calib_packv5_041523_1651.root, FC#0, port C2

Entries	454
Mean	38.07
Std Dev	18.05

Turn on : 24.6547

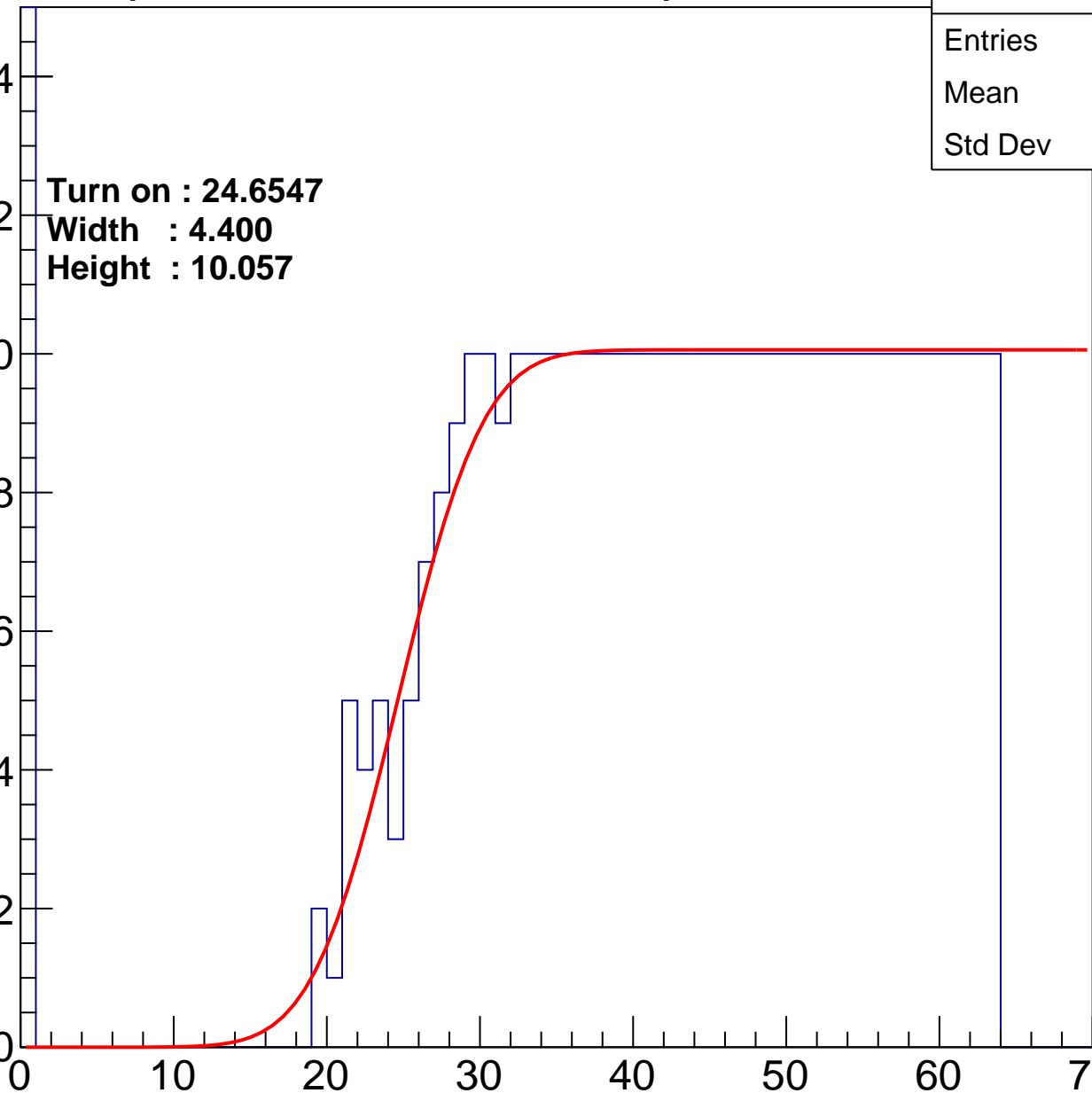
Width : 4.400

Height : 10.057

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch103

calib_packv5_041523_1651.root, FC#0, port C2

Entries	424
Mean	39.94
Std Dev	16.95

Turn on : 26.0471

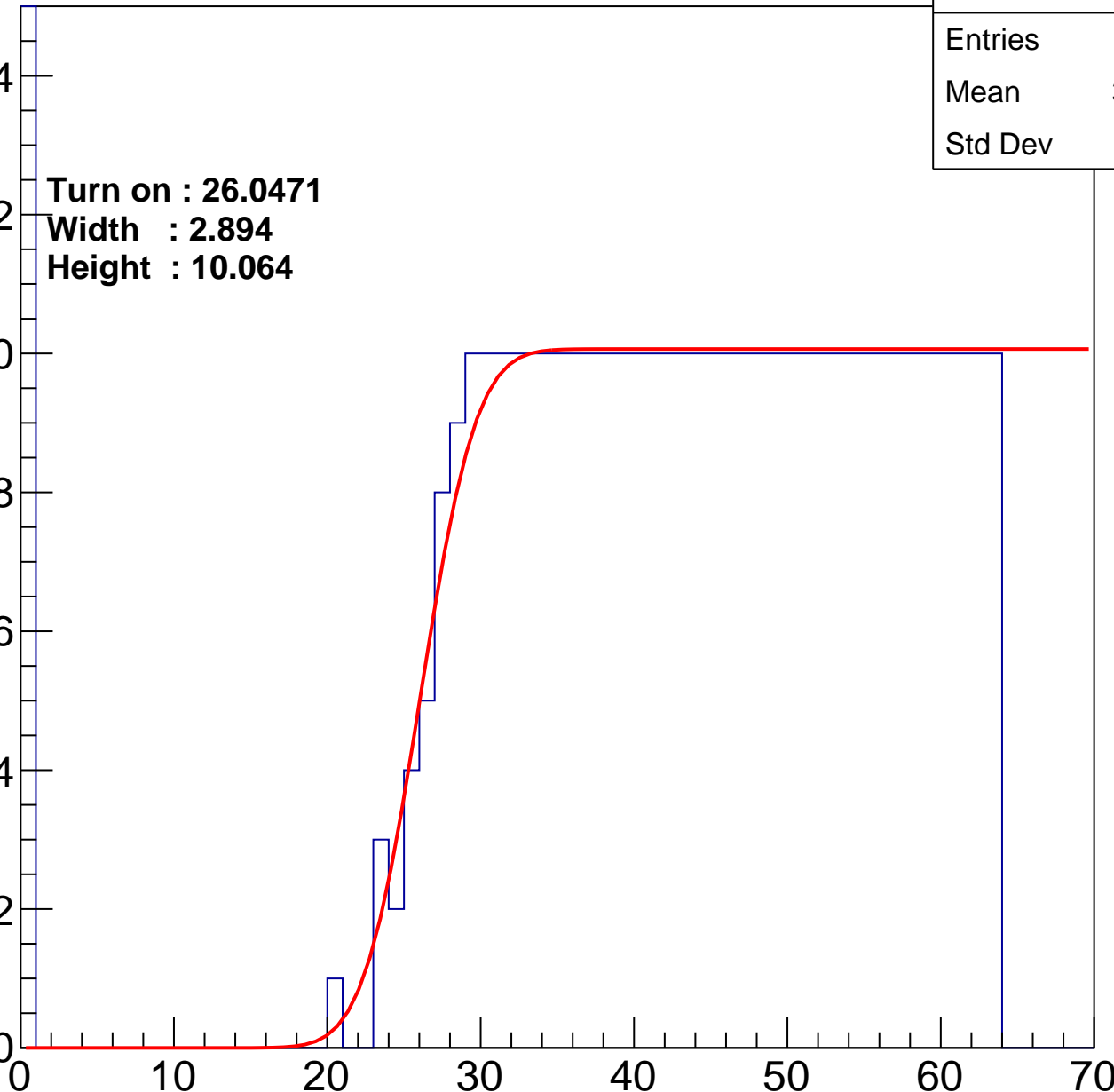
Width : 2.894

Height : 10.064

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch104

calib_packv5_041523_1651.root, FC#0, port C2

Entries	436
Mean	38.84
Std Dev	17.9

Turn on : 25.5330

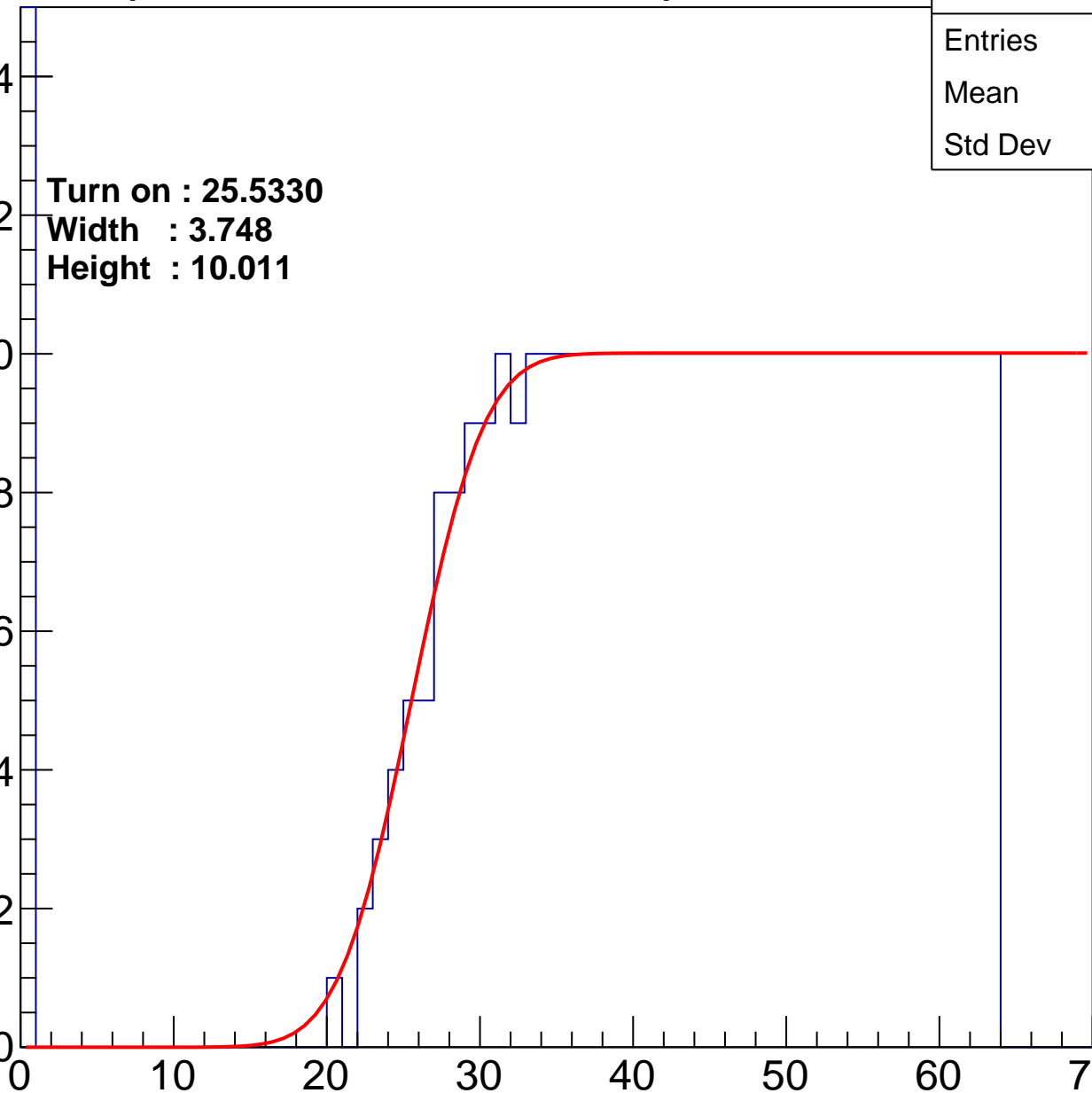
Width : 3.748

Height : 10.011

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch105

calib_packv5_041523_1651.root, FC#0, port C2

Entries	447
Mean	37.98
Std Dev	18.58

Turn on : 25.7414

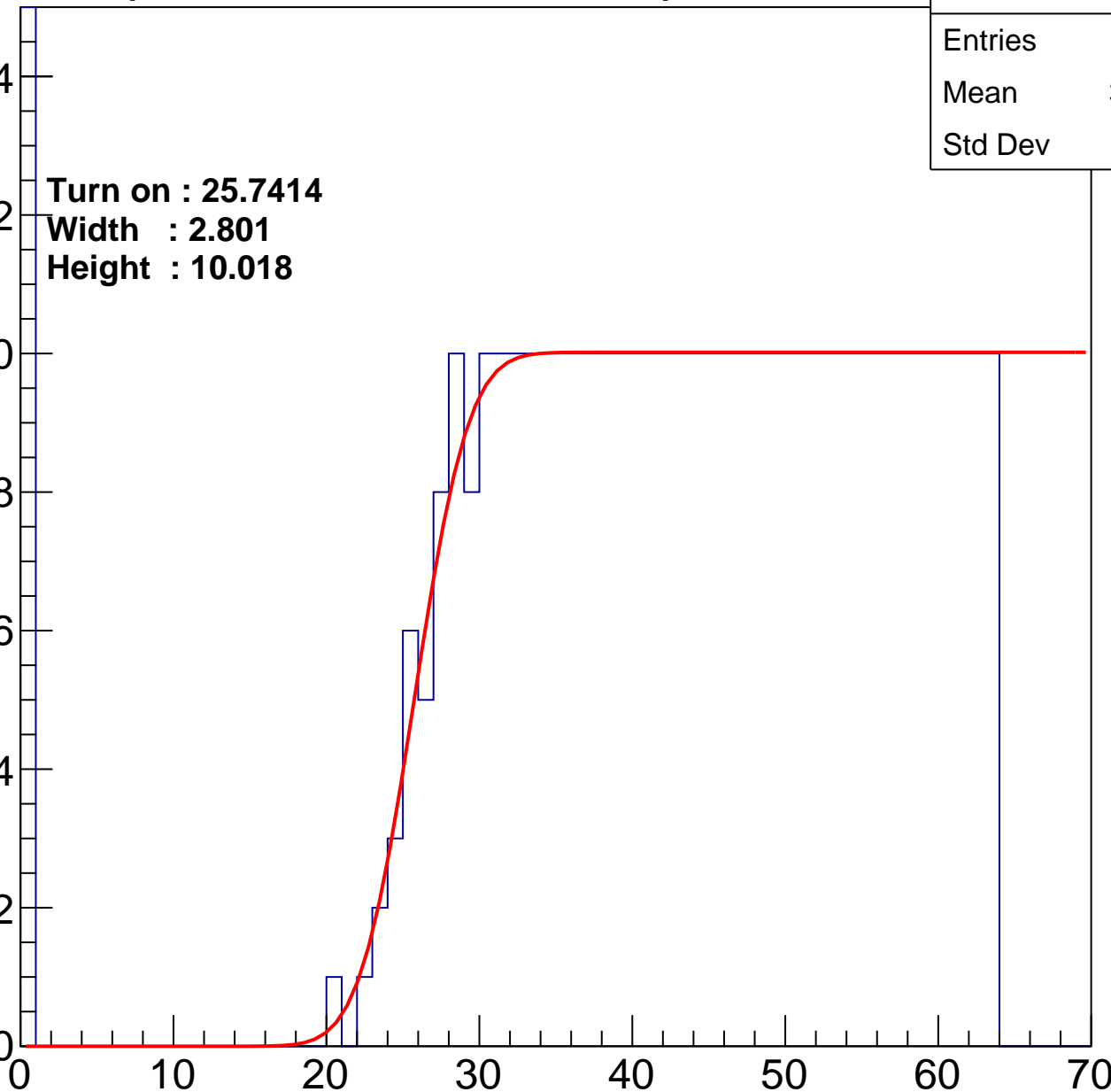
Width : 2.801

Height : 10.018

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch106

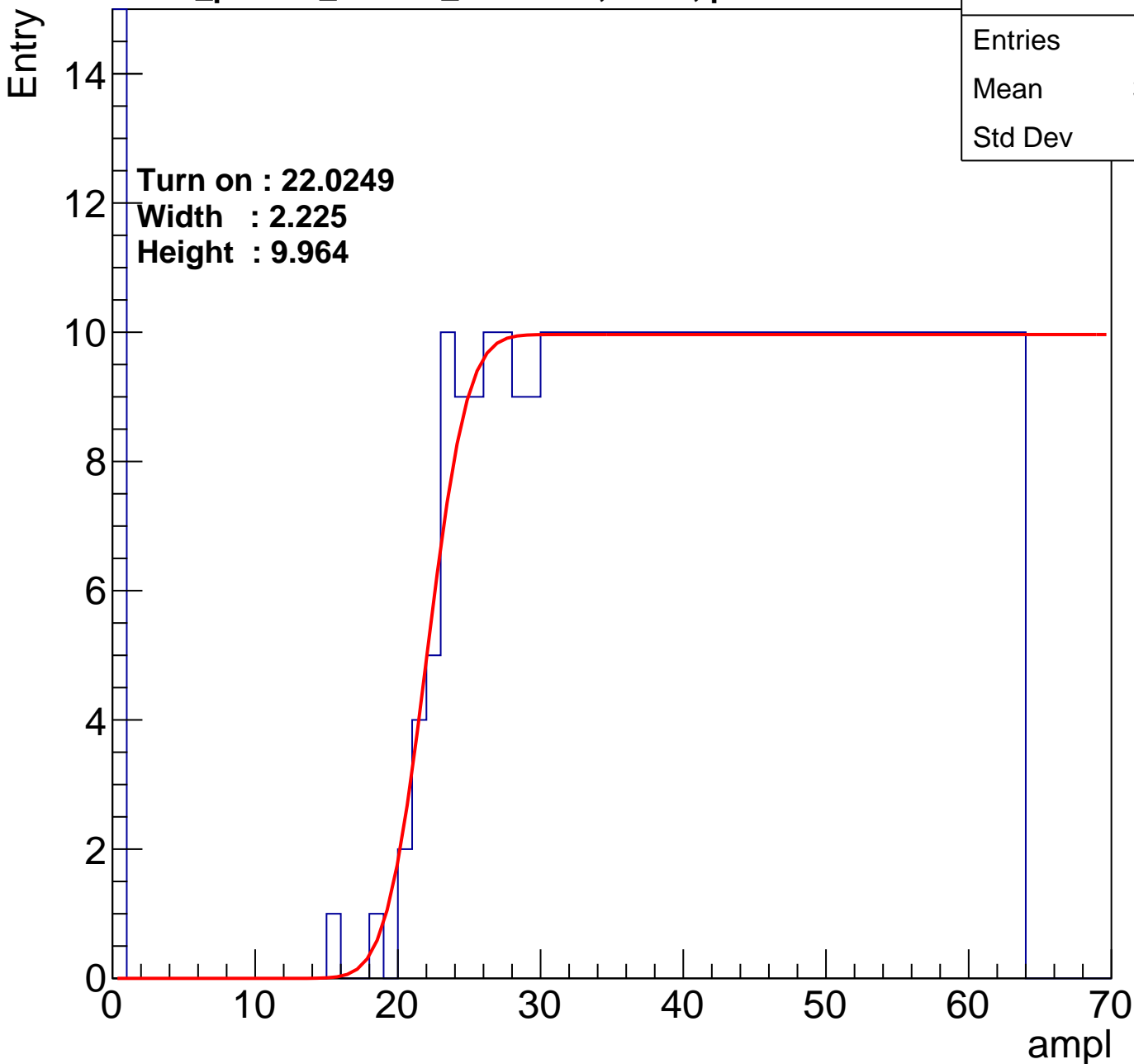
calib_packv5_041523_1651.root, FC#0, port C2

Entries	468
Mean	38.01
Std Dev	17.41

Turn on : 22.0249

Width : 2.225

Height : 9.964



B1L103S, U5-ch107

calib_packv5_041523_1651.root, FC#0, port C2

Entries	445
Mean	38.8
Std Dev	17.49

Turn on : 24.2809

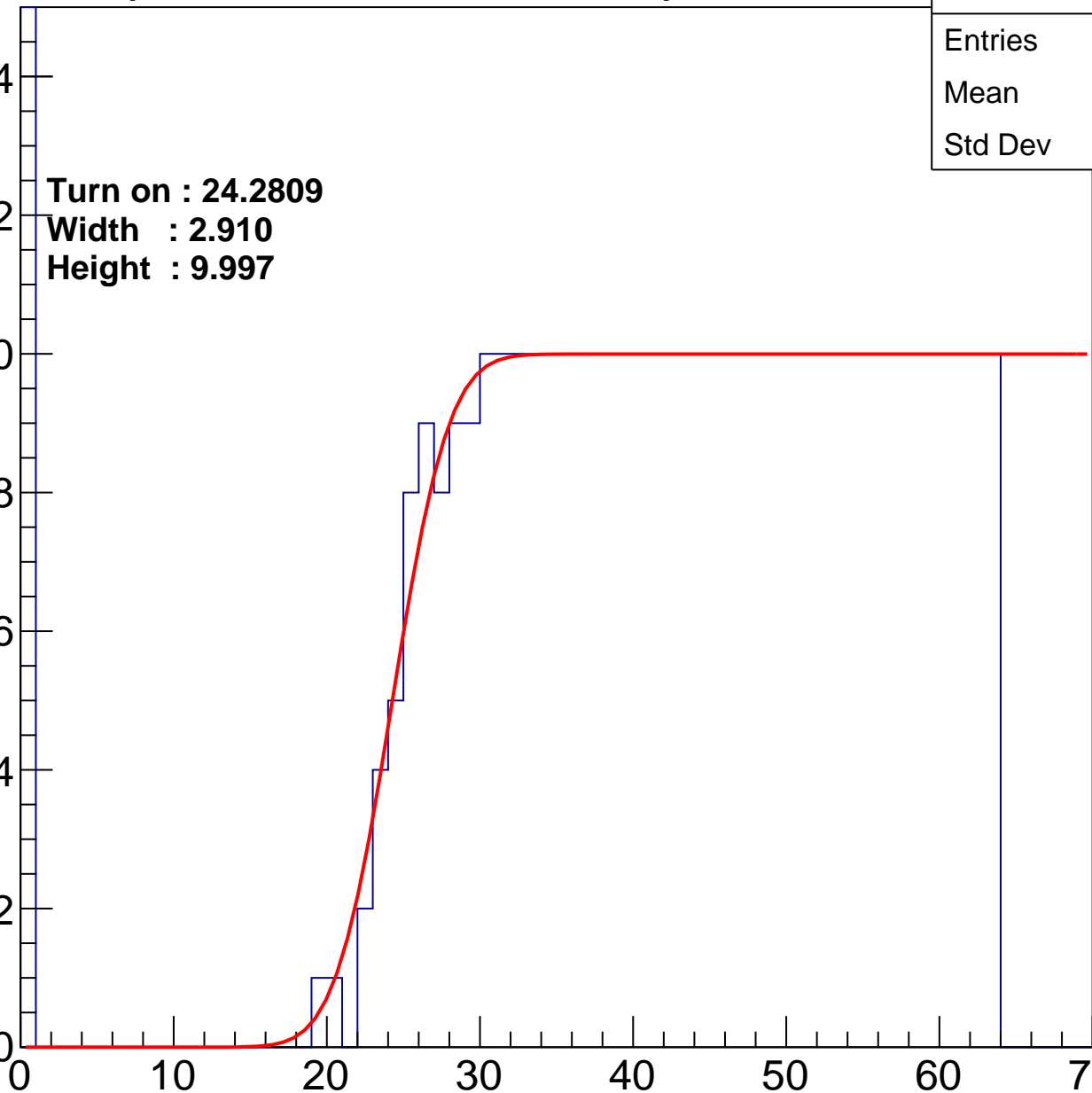
Width : 2.910

Height : 9.997

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch108

calib_packv5_041523_1651.root, FC#0, port C2

Entries	486
Mean	36.41
Std Dev	18.83

Turn on : 22.7177

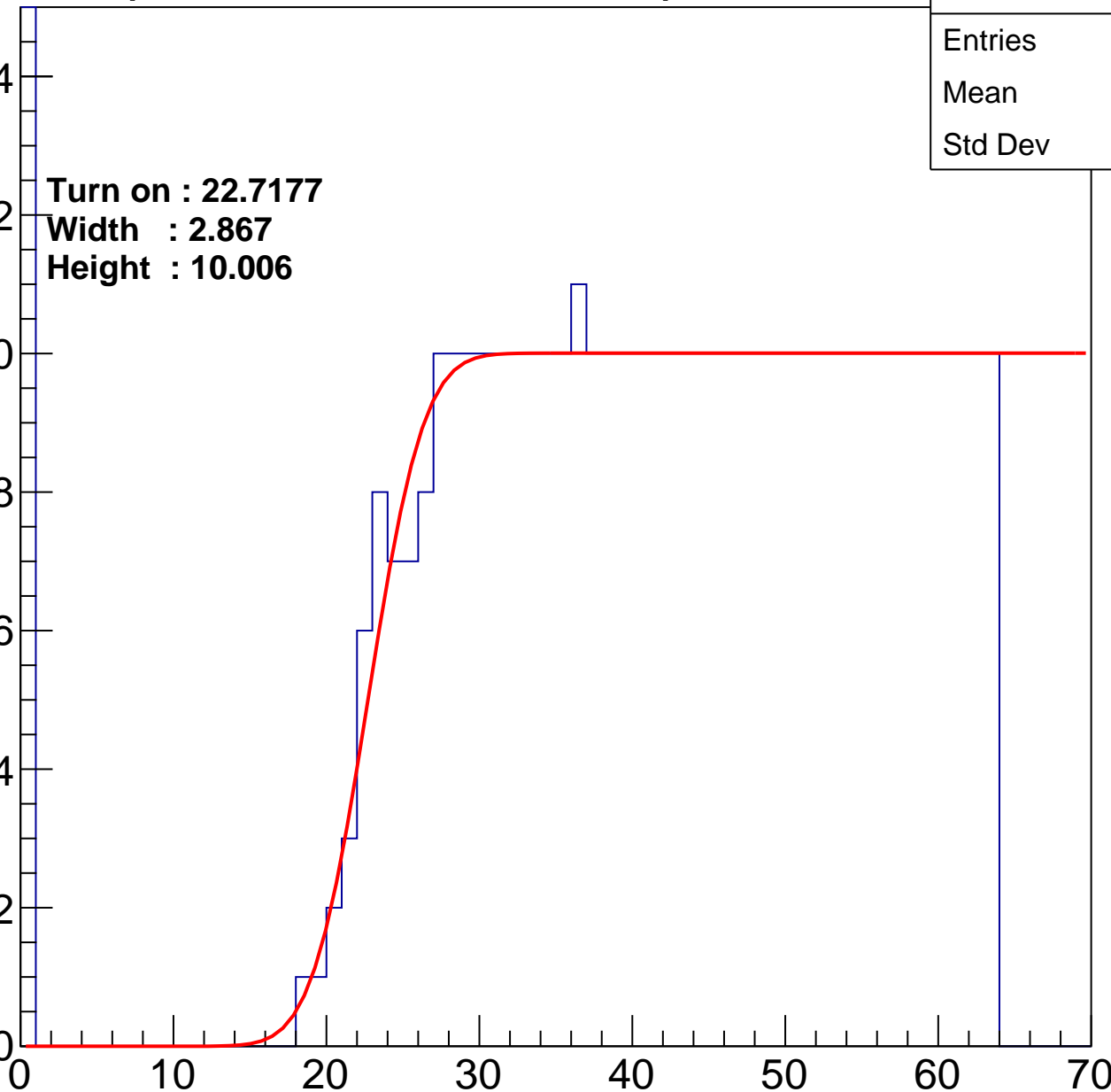
Width : 2.867

Height : 10.006

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch109

calib_packv5_041523_1651.root, FC#0, port C2

Entries	453
Mean	38.2
Std Dev	17.93

Turn on : 23.9298

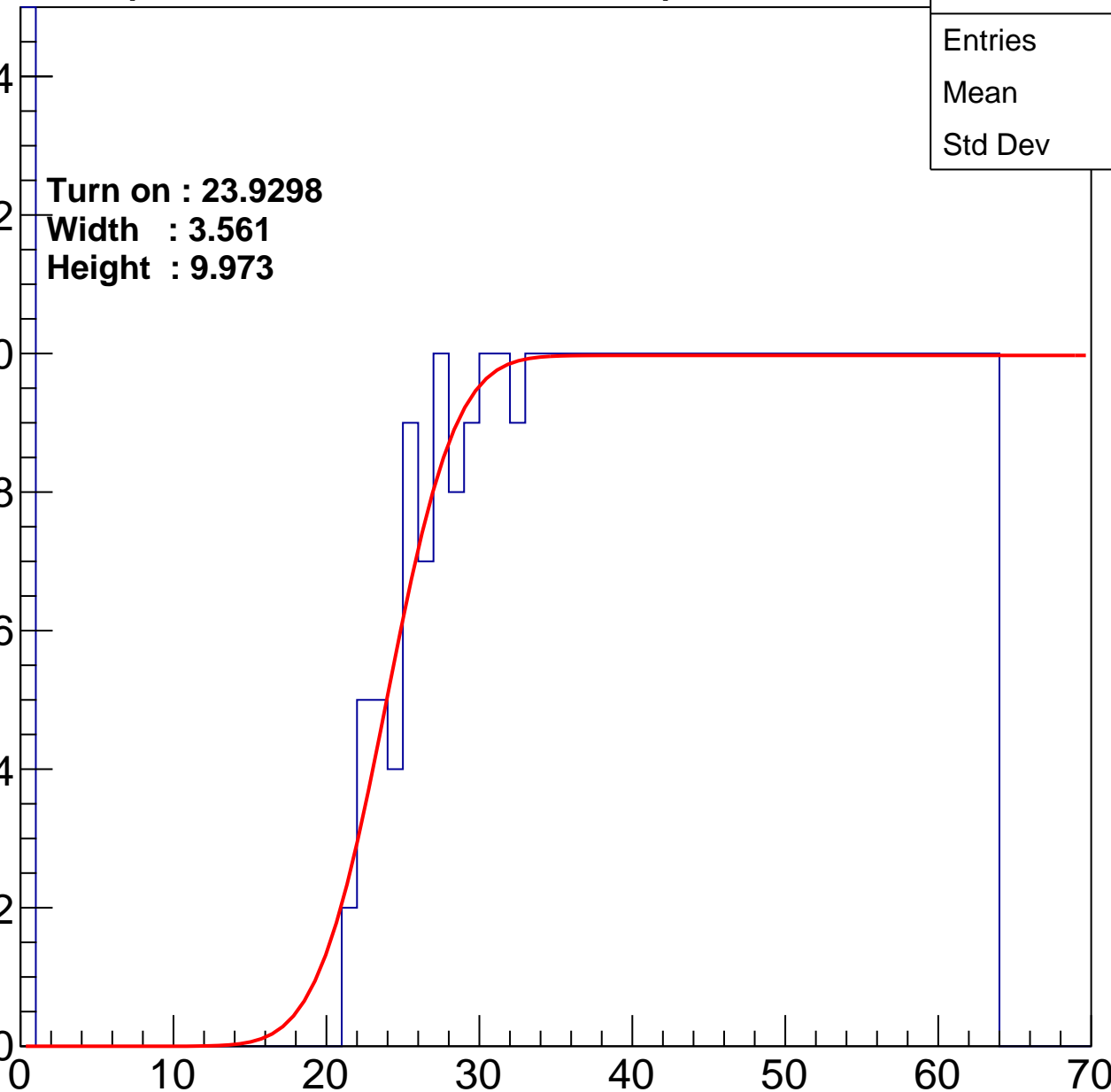
Width : 3.561

Height : 9.973

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch110

calib_packv5_041523_1651.root, FC#0, port C2

Entries	425
Mean	39.86
Std Dev	16.98

Turn on : 25.8103

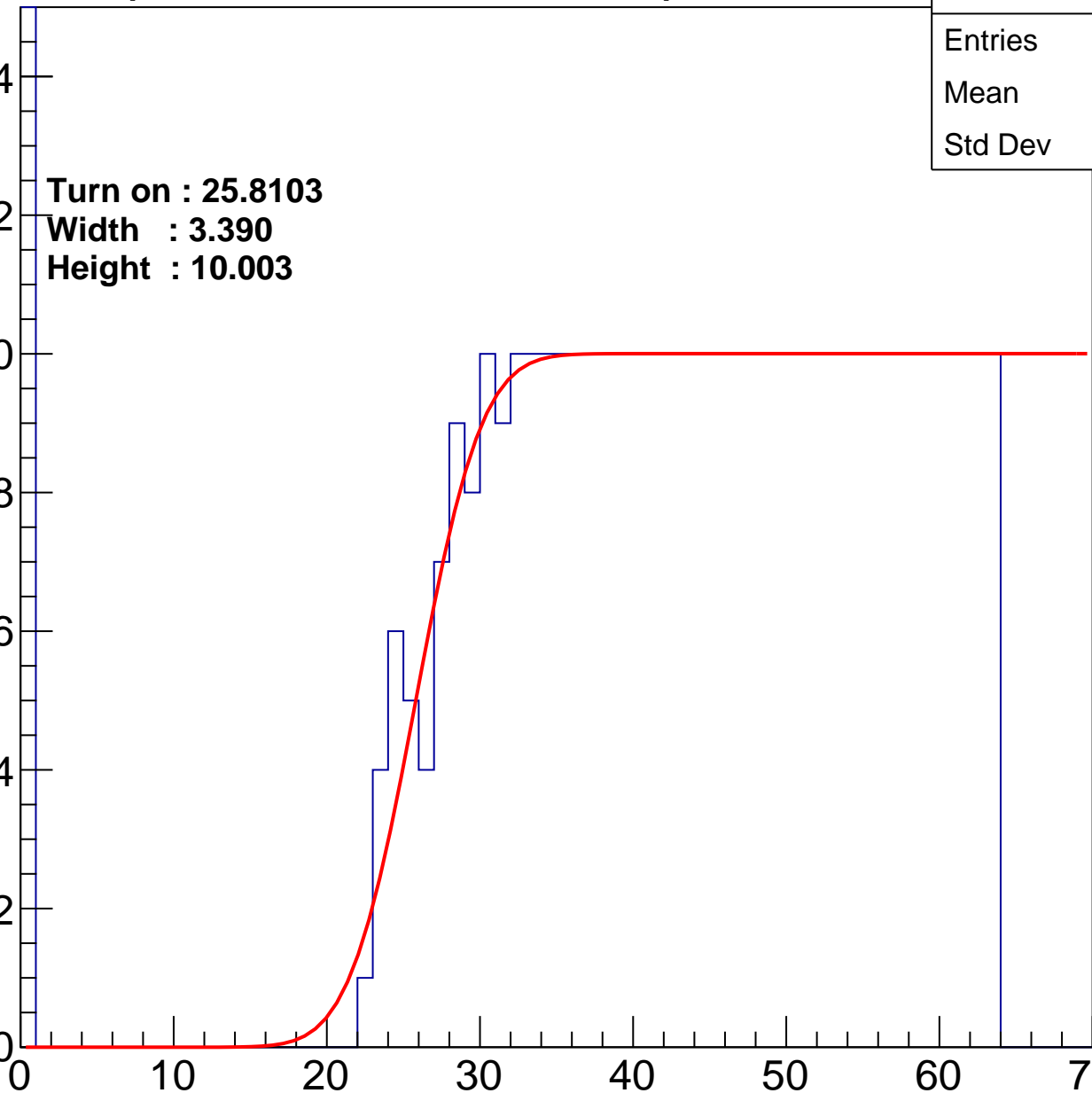
Width : 3.390

Height : 10.003

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch111

calib_packv5_041523_1651.root, FC#0, port C2

Entries	458
Mean	37.17
Std Dev	19.08

Turn on : 25.7554

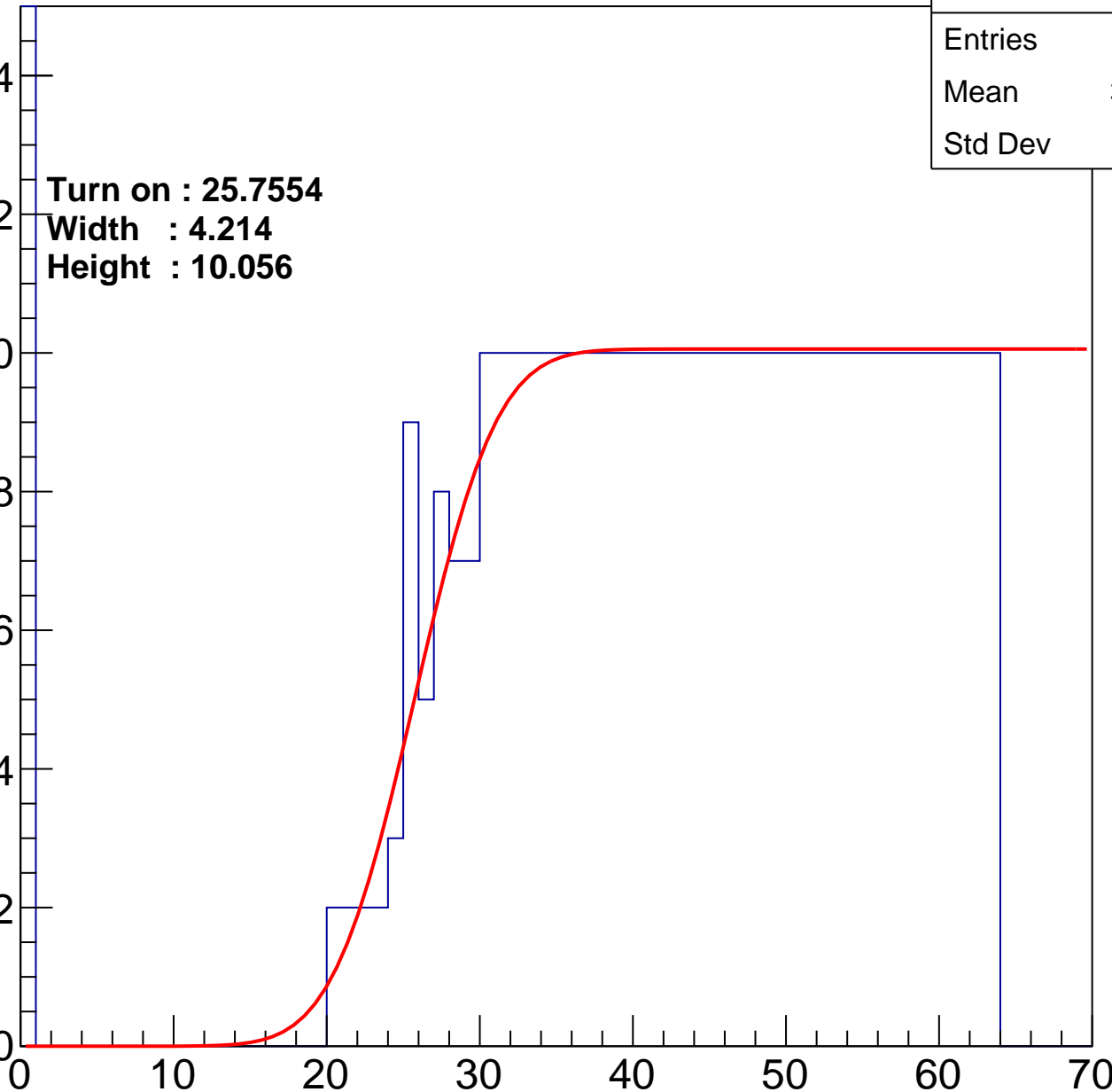
Width : 4.214

Height : 10.056

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch112

calib_packv5_041523_1651.root, FC#0, port C2

Entries	445
Mean	38.4
Std Dev	18.07

Turn on : 25.1628

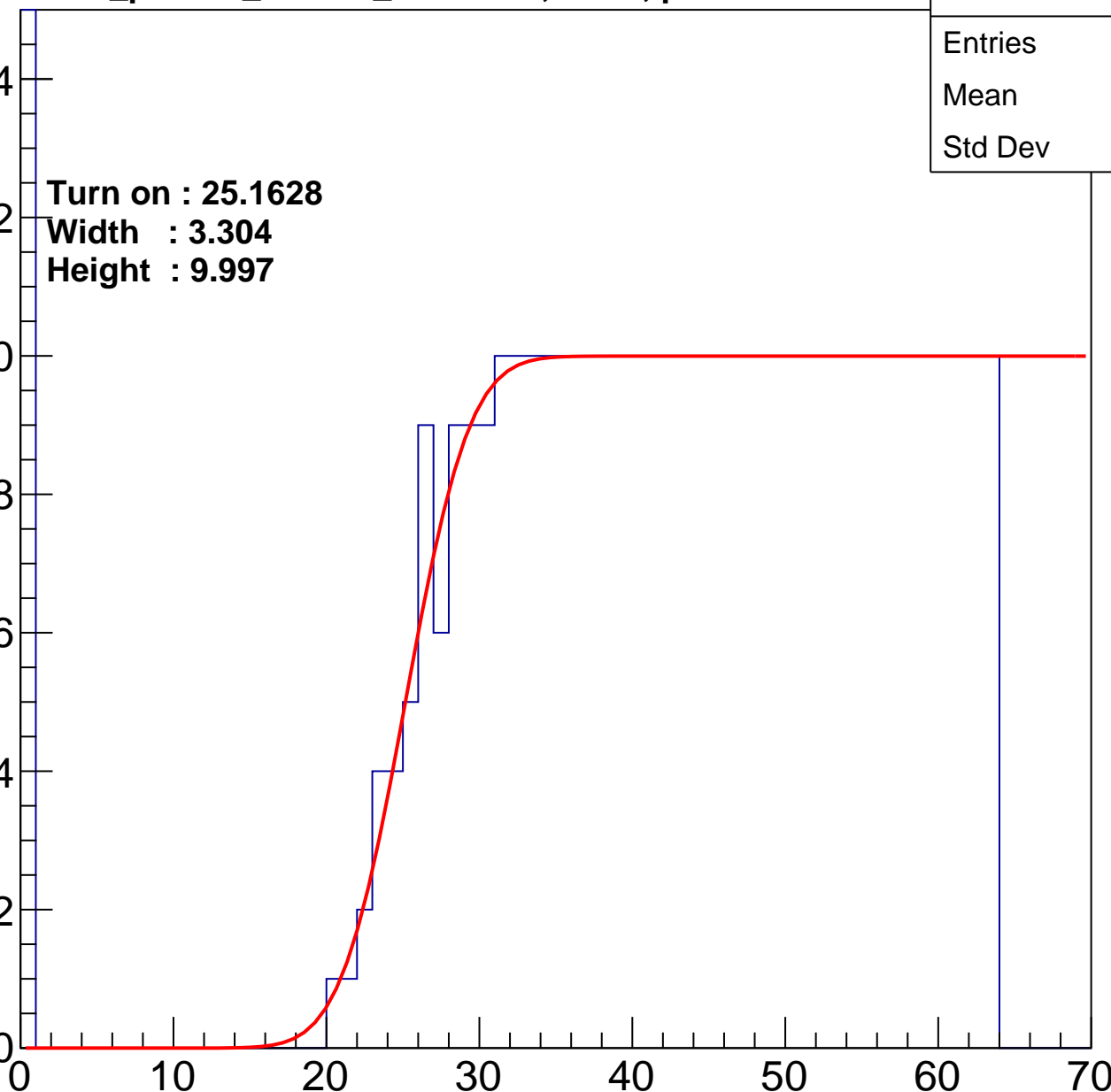
Width : 3.304

Height : 9.997

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch113

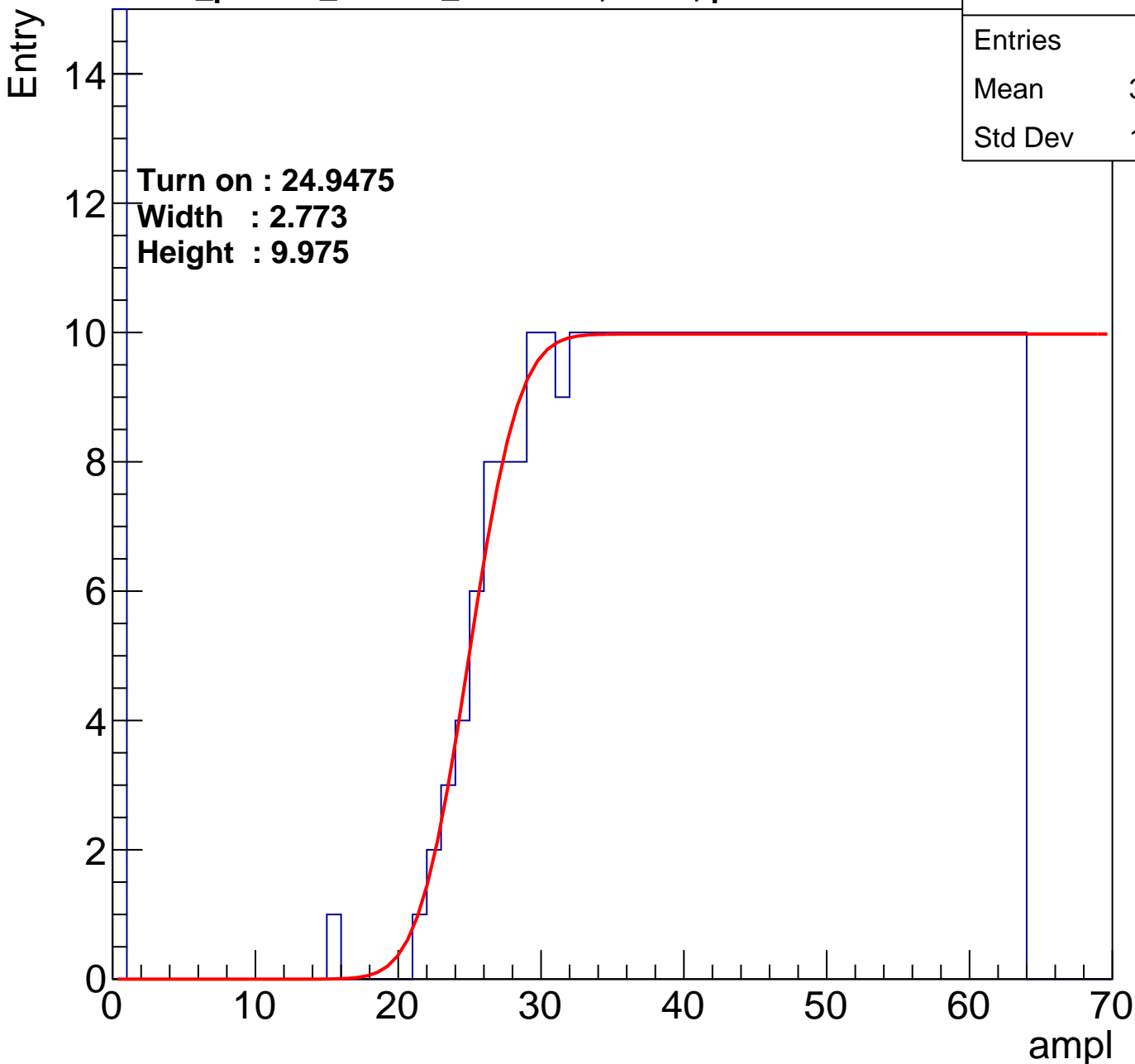
calib_packv5_041523_1651.root, FC#0, port C2

Entries	443
Mean	38.63
Std Dev	17.85

Turn on : 24.9475

Width : 2.773

Height : 9.975



B1L103S, U5-ch114

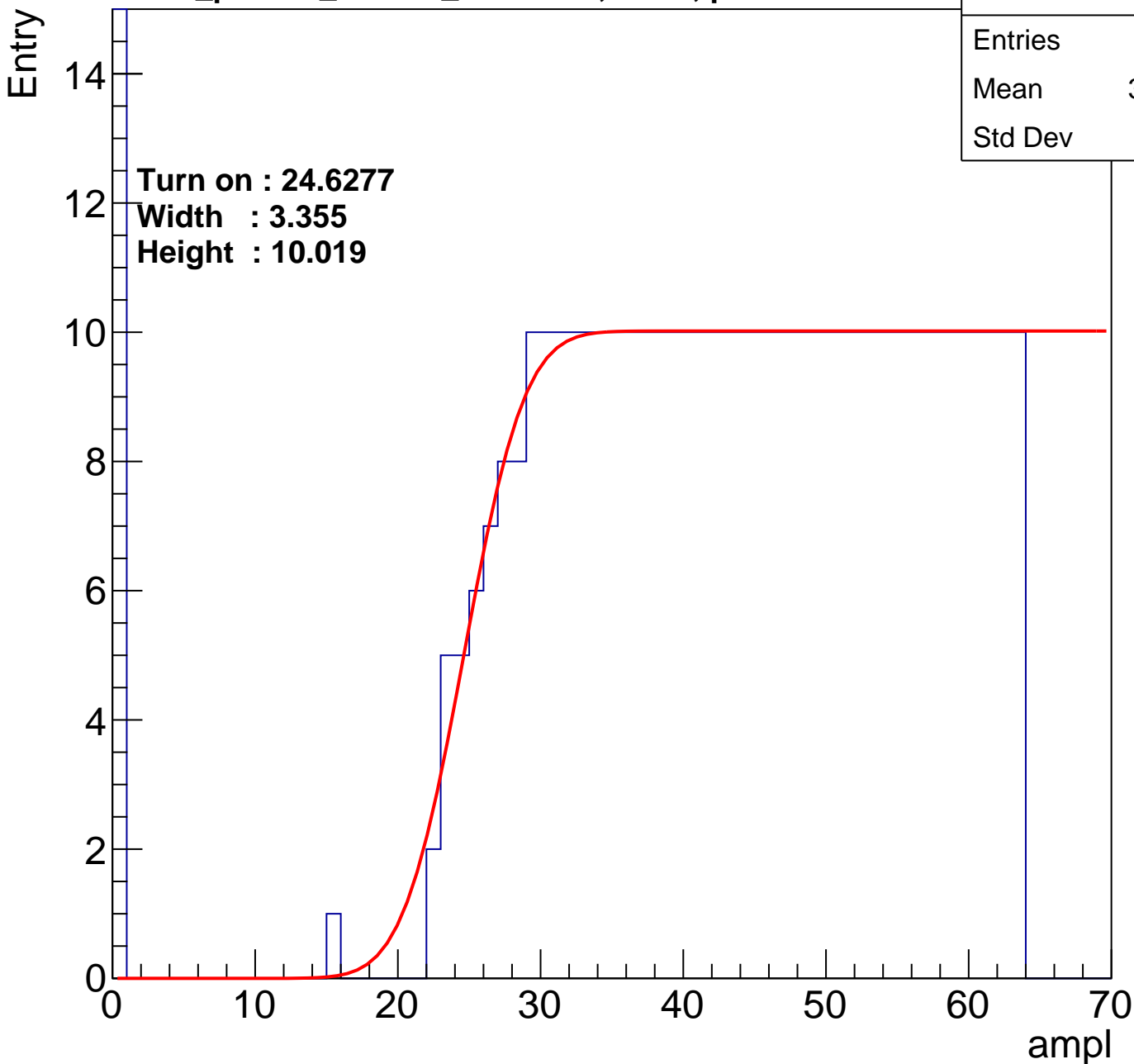
calib_packv5_041523_1651.root, FC#0, port C2

Entries	463
Mean	37.08
Std Dev	19

Turn on : 24.6277

Width : 3.355

Height : 10.019



B1L103S, U5-ch115

calib_packv5_041523_1651.root, FC#0, port C2

Entries	473
Mean	36.3
Std Dev	19.54

Turn on : 25.3521

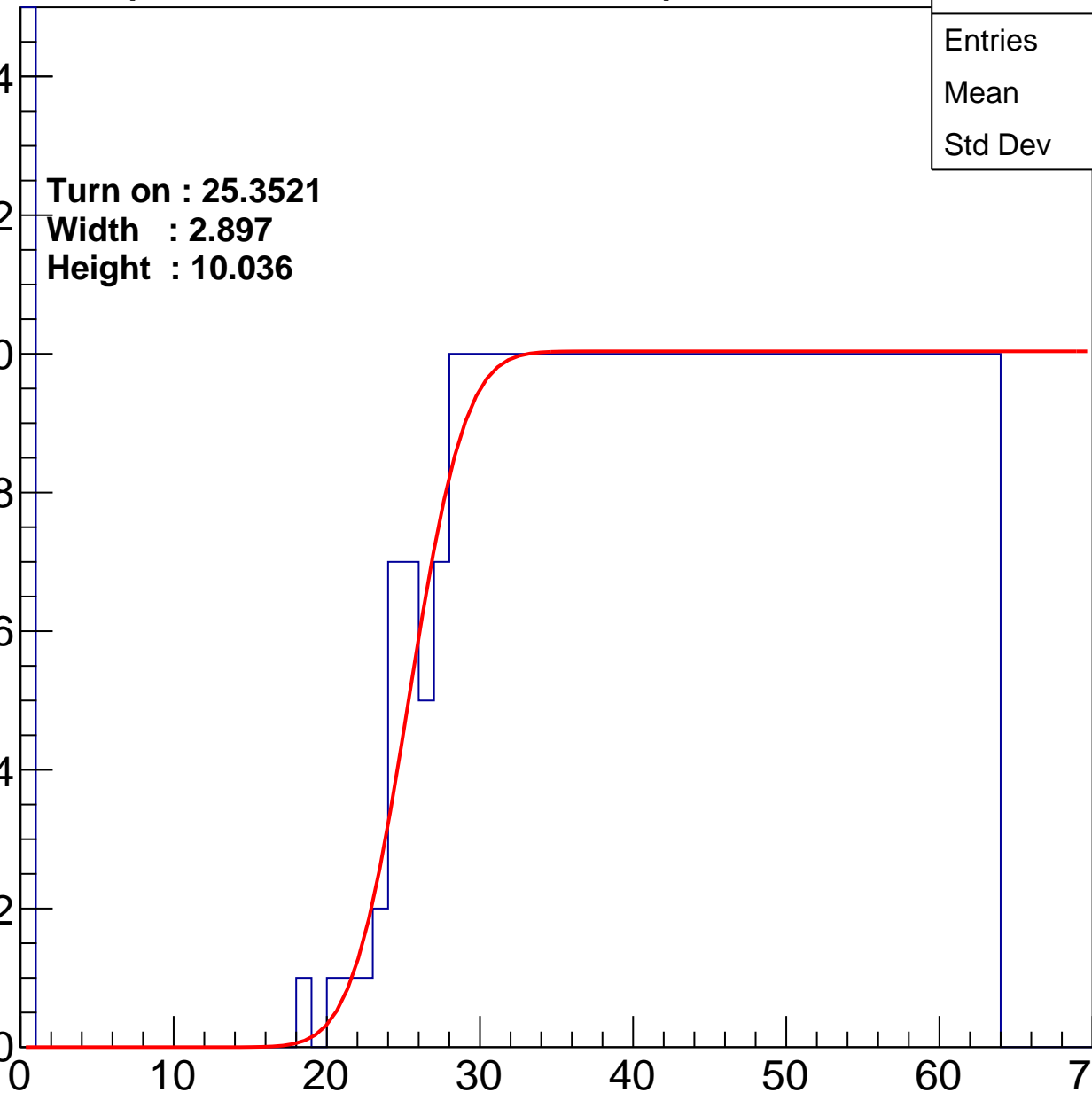
Width : 2.897

Height : 10.036

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch116

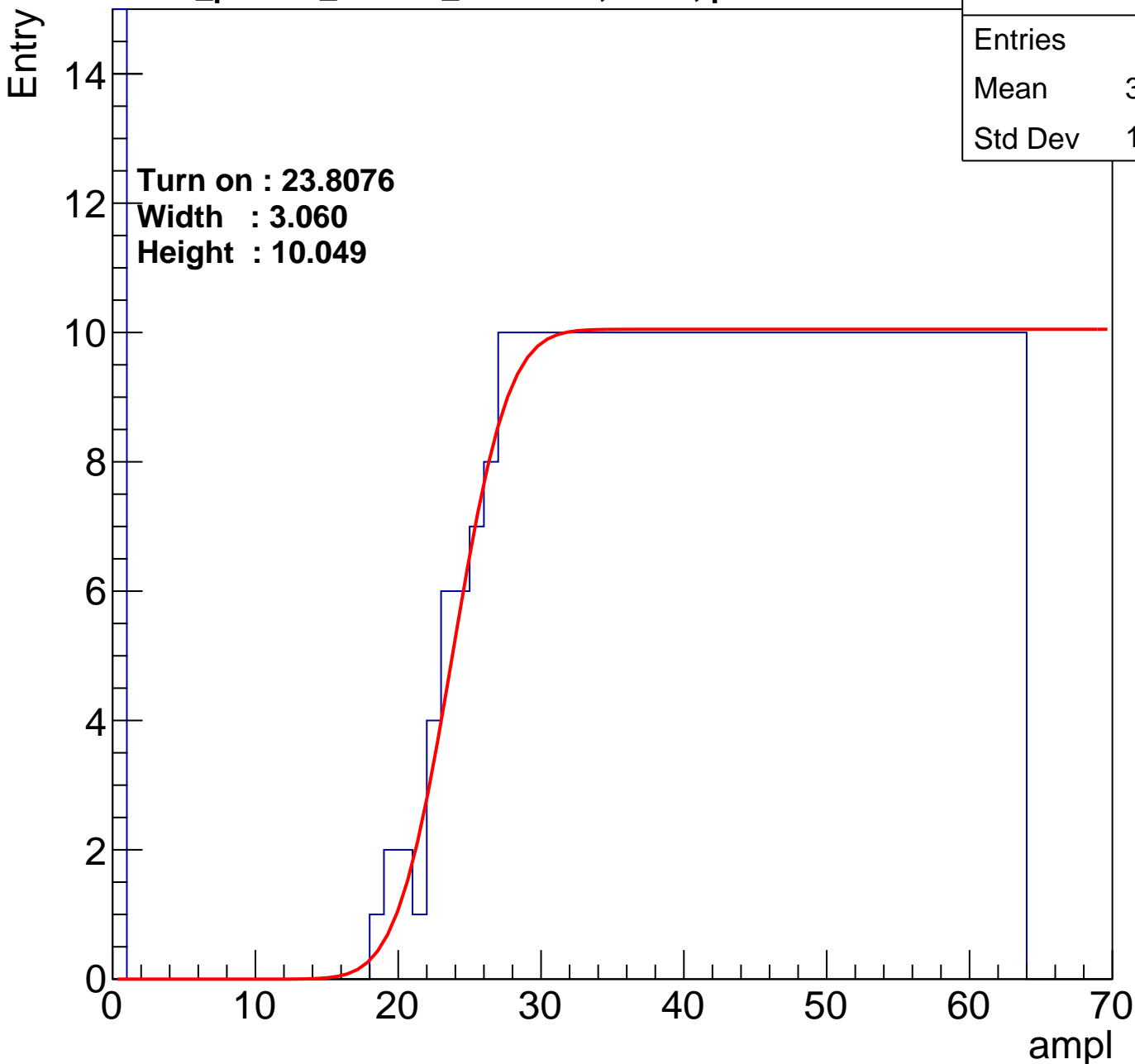
calib_packv5_041523_1651.root, FC#0, port C2

Entries	441
Mean	39.73
Std Dev	16.22

Turn on : 23.8076

Width : 3.060

Height : 10.049



B1L103S, U5-ch117

calib_packv5_041523_1651.root, FC#0, port C2

Entries	418
Mean	39.73
Std Dev	17.59

Turn on : 27.3206

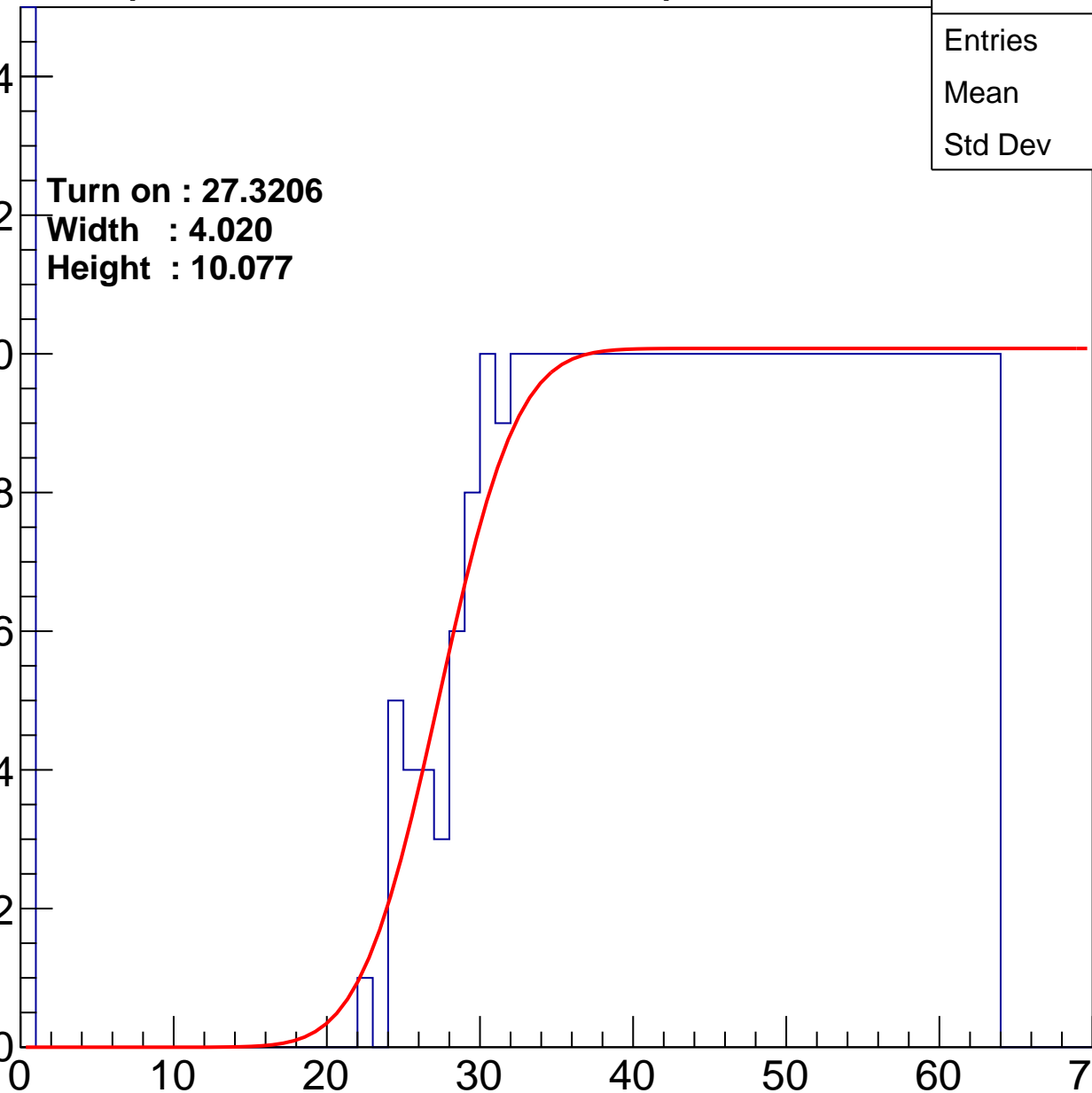
Width : 4.020

Height : 10.077

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch118

calib_packv5_041523_1651.root, FC#0, port C2

Entries	446
Mean	38.92
Std Dev	17.24

Turn on : 24.0553

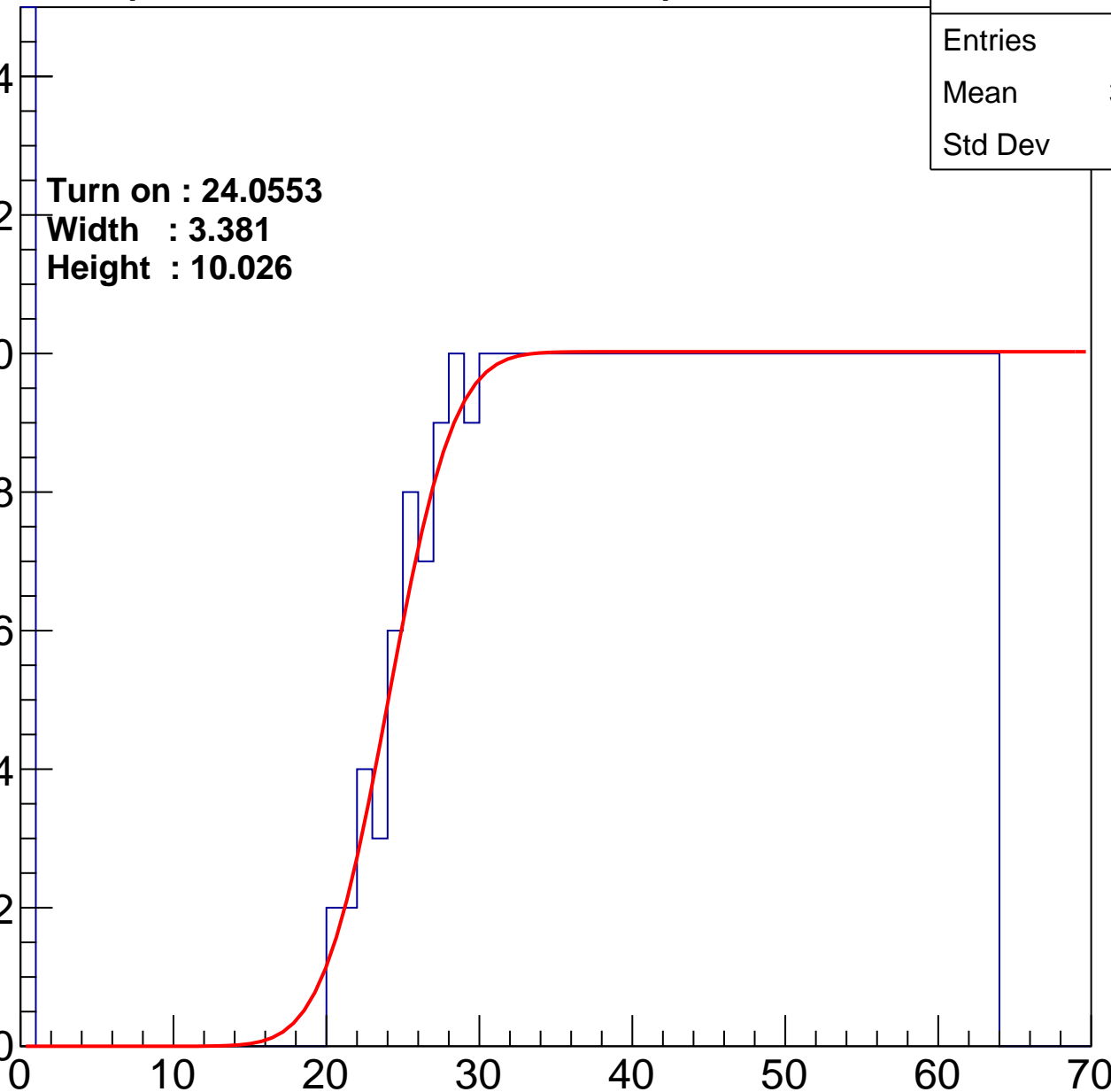
Width : 3.381

Height : 10.026

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch119

calib_packv5_041523_1651.root, FC#0, port C2

Entries	455
Mean	38.32
Std Dev	17.64

Turn on : 24.5162

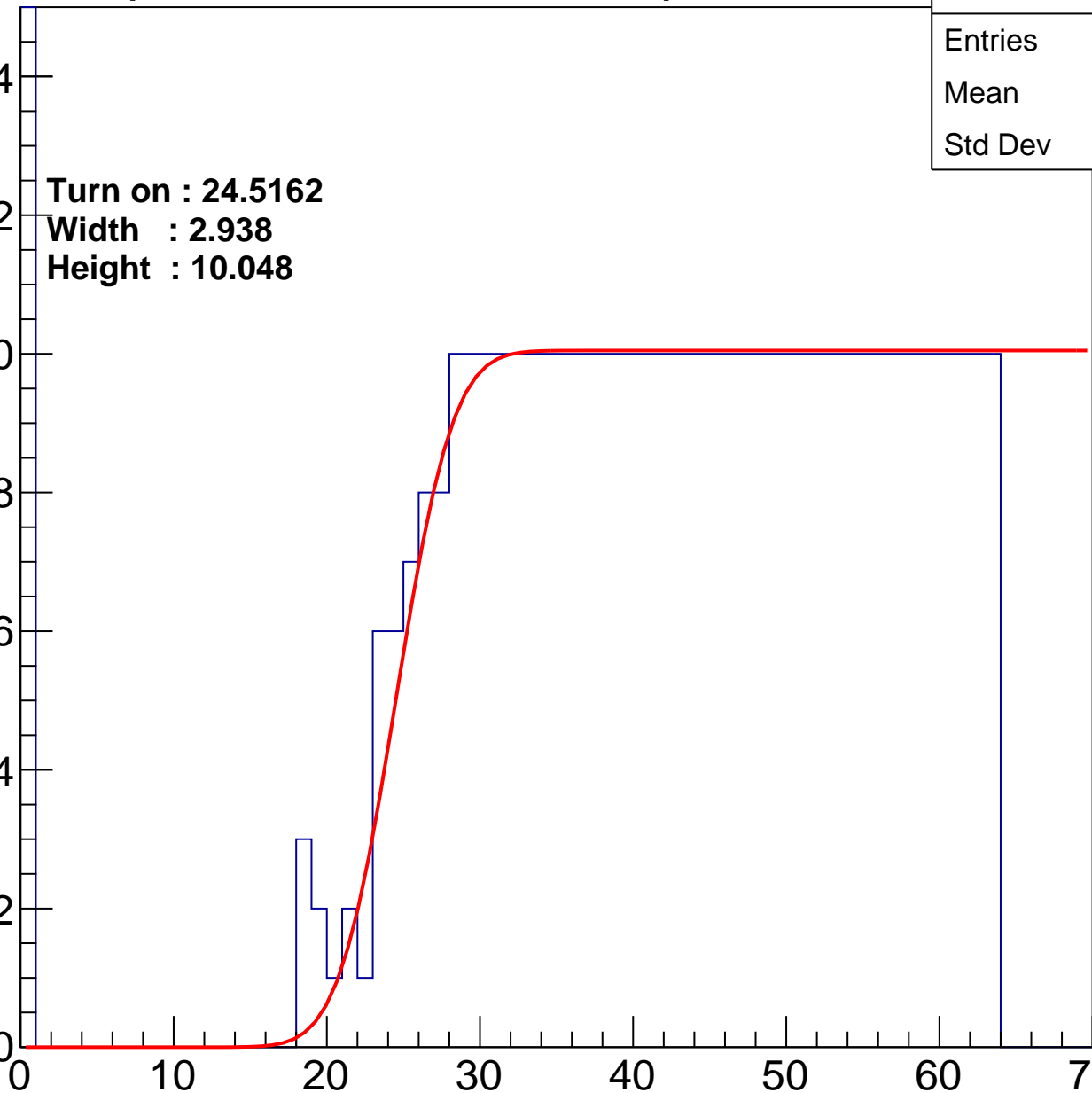
Width : 2.938

Height : 10.048

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch120

calib_packv5_041523_1651.root, FC#0, port C2

Entries	442
Mean	38.64
Std Dev	17.87

Turn on : 25.6769

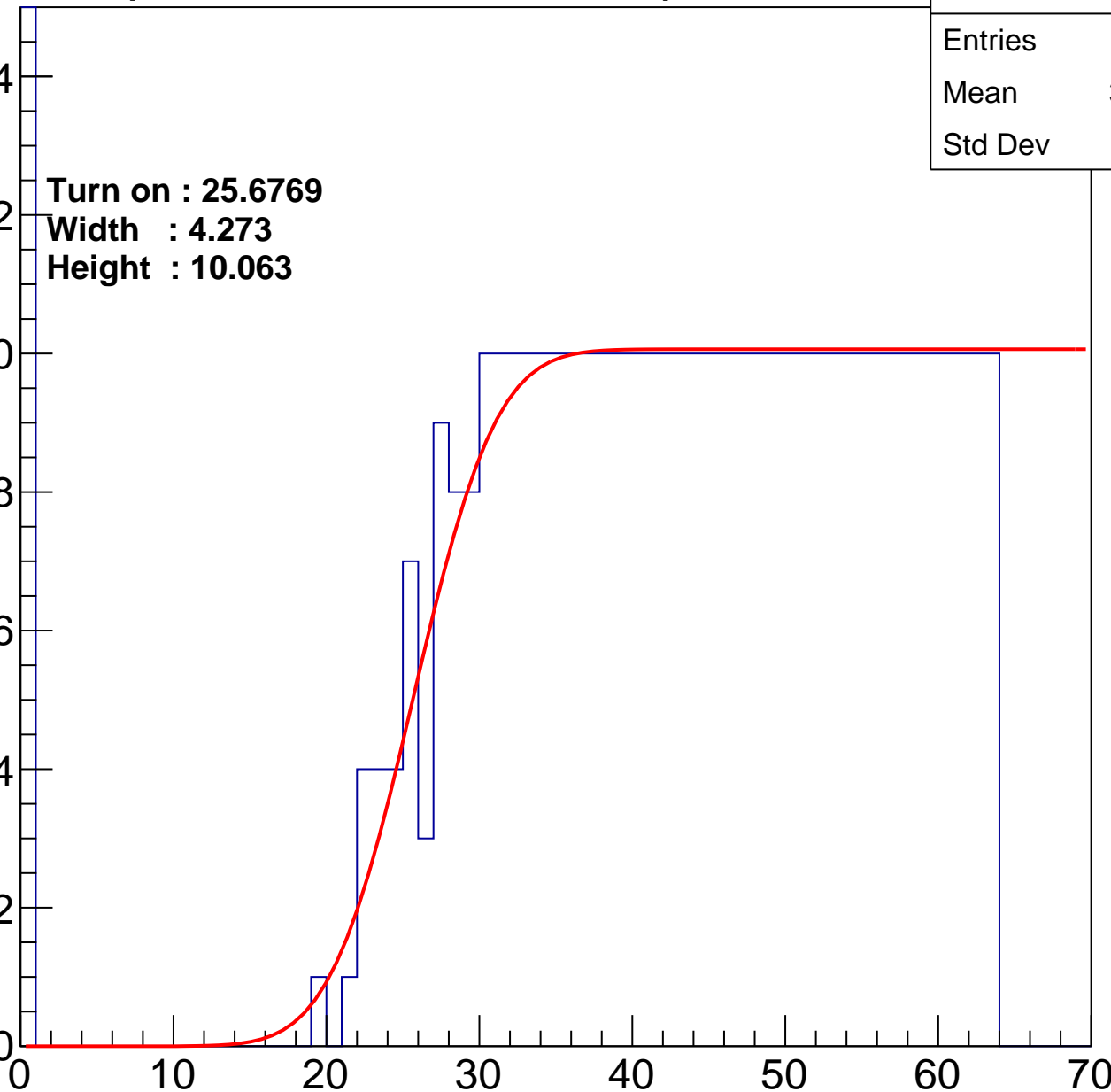
Width : 4.273

Height : 10.063

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch121

calib_packv5_041523_1651.root, FC#0, port C2

Entries	464
Mean	37.45
Std Dev	18.48

Turn on : 23.9973

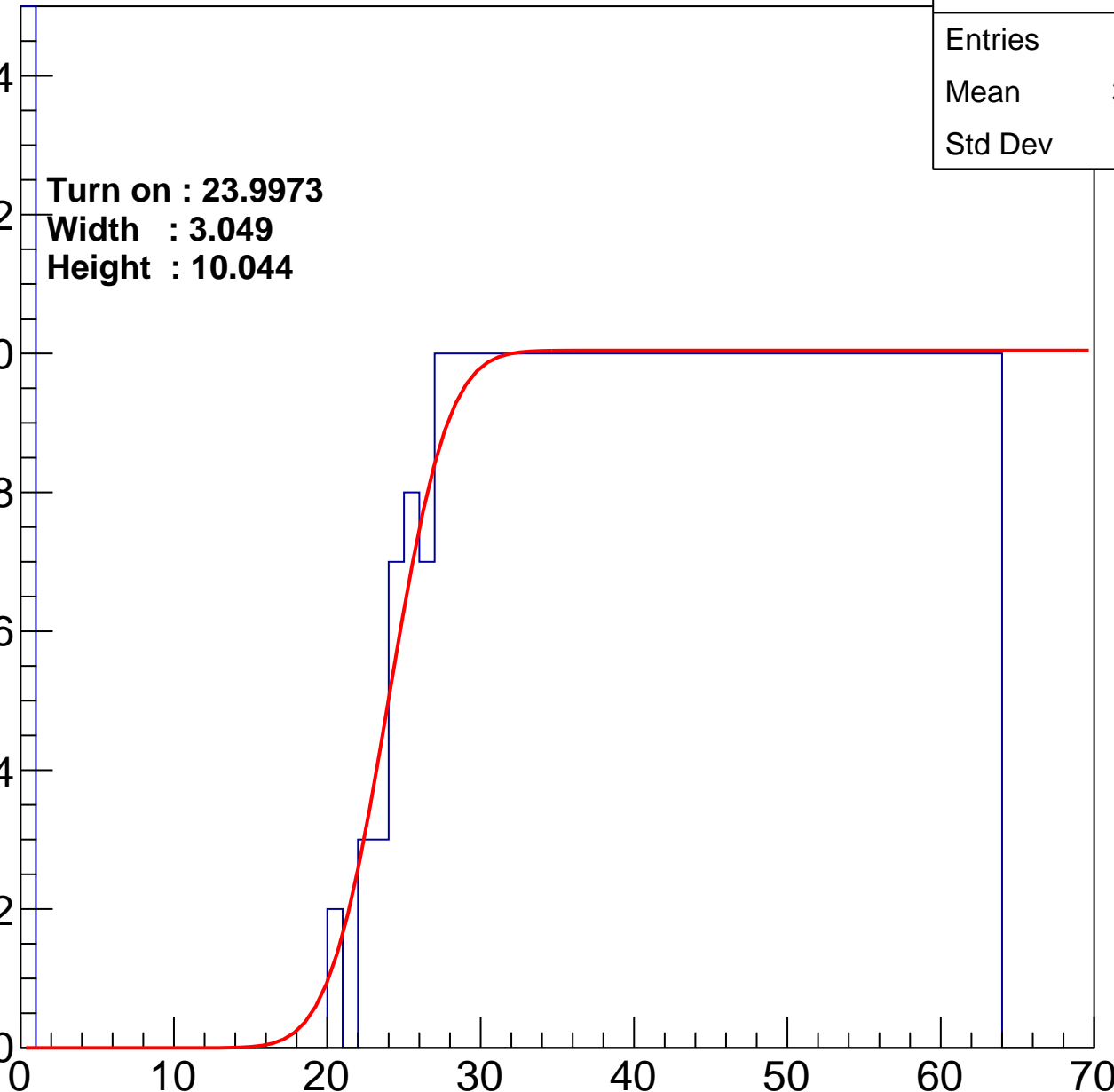
Width : 3.049

Height : 10.044

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch122

calib_packv5_041523_1651.root, FC#0, port C2

Entries	435
Mean	39.41
Std Dev	17.19

Turn on : 25.4179

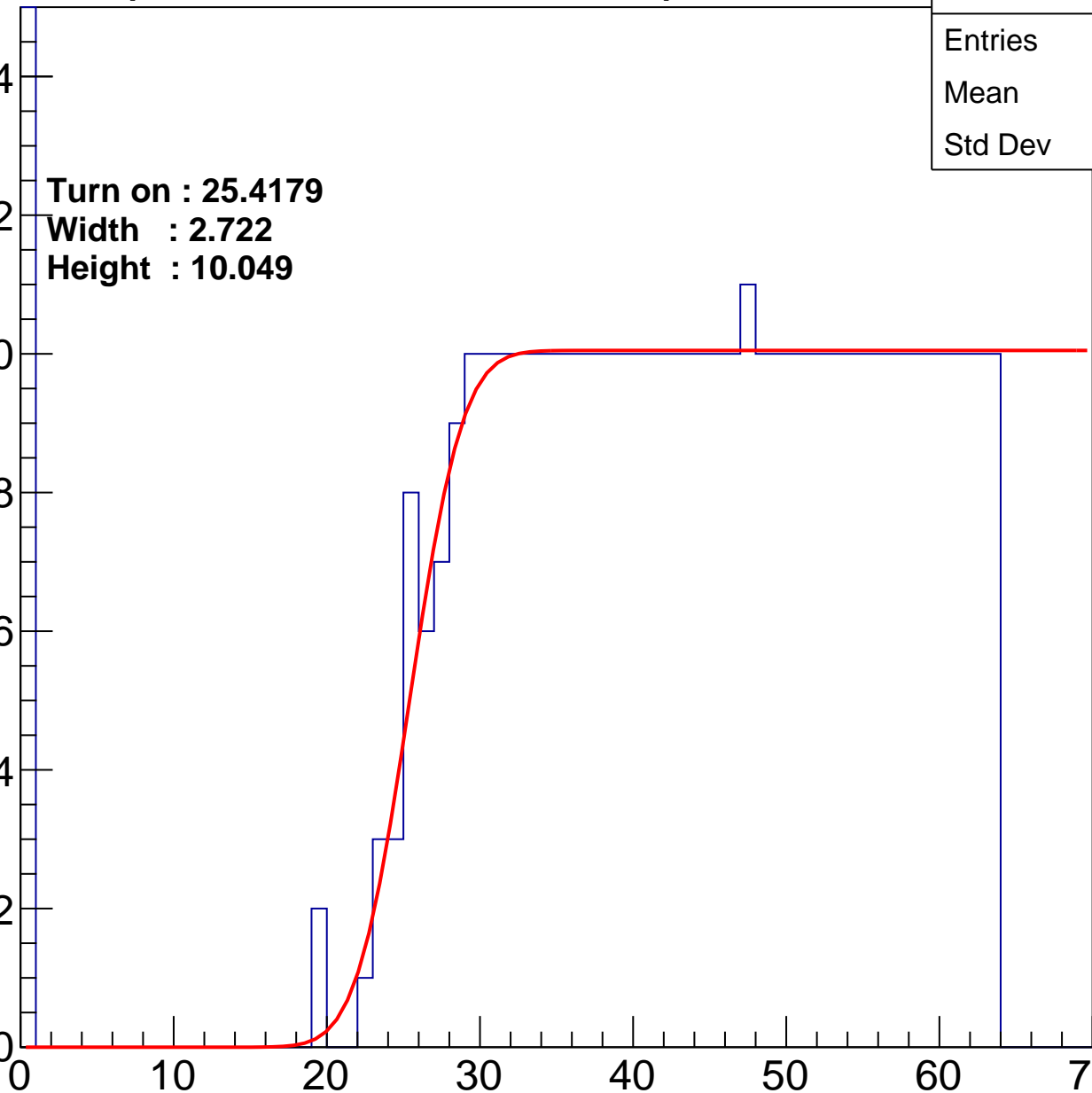
Width : 2.722

Height : 10.049

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch123

calib_packv5_041523_1651.root, FC#0, port C2

Entries	486
Mean	35.83
Std Dev	19.56

Turn on : 23.9222

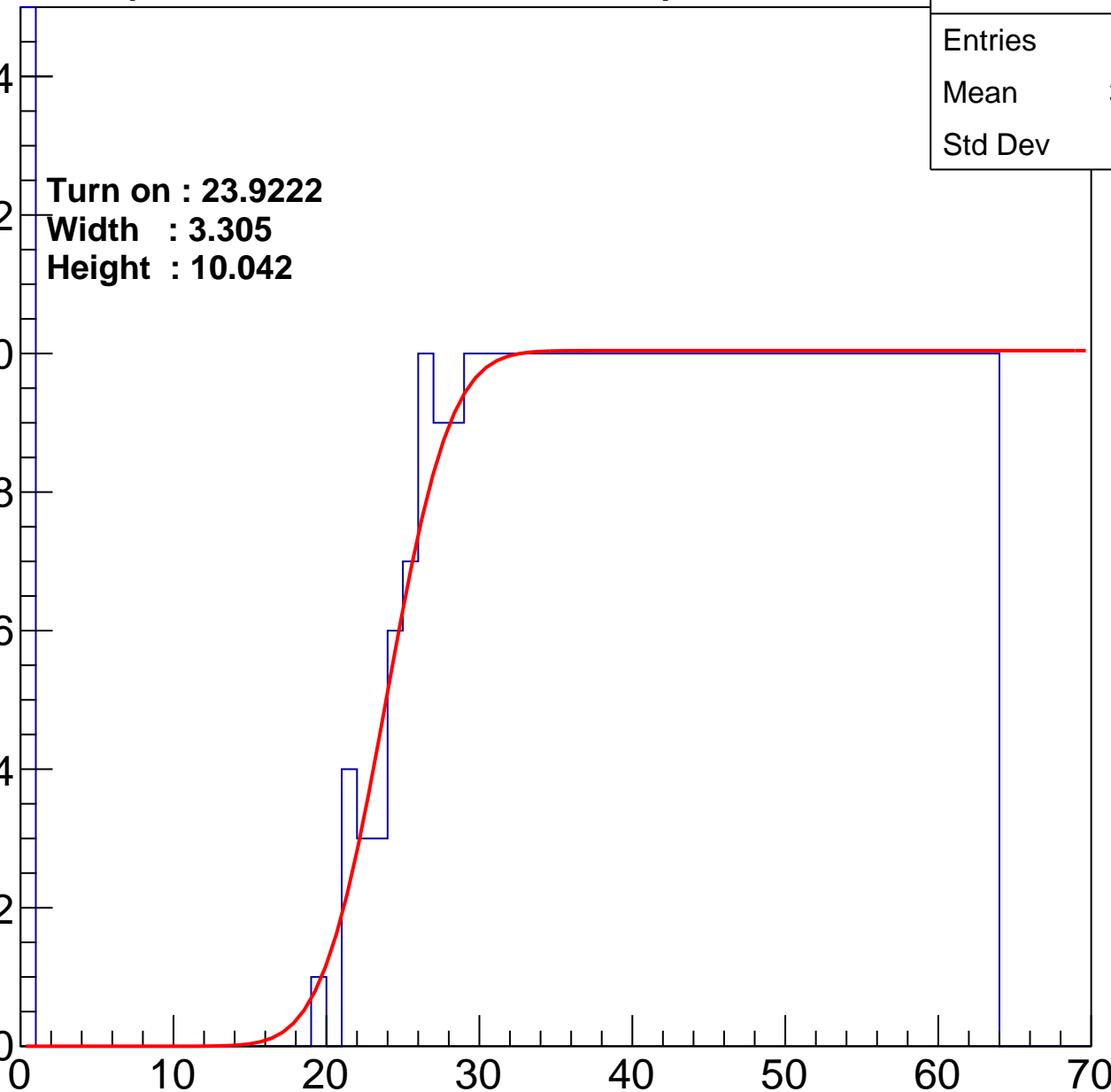
Width : 3.305

Height : 10.042

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch124

calib_packv5_041523_1651.root, FC#0, port C2

Entries	433
Mean	39.42
Std Dev	17.22

Turn on : 26.9117

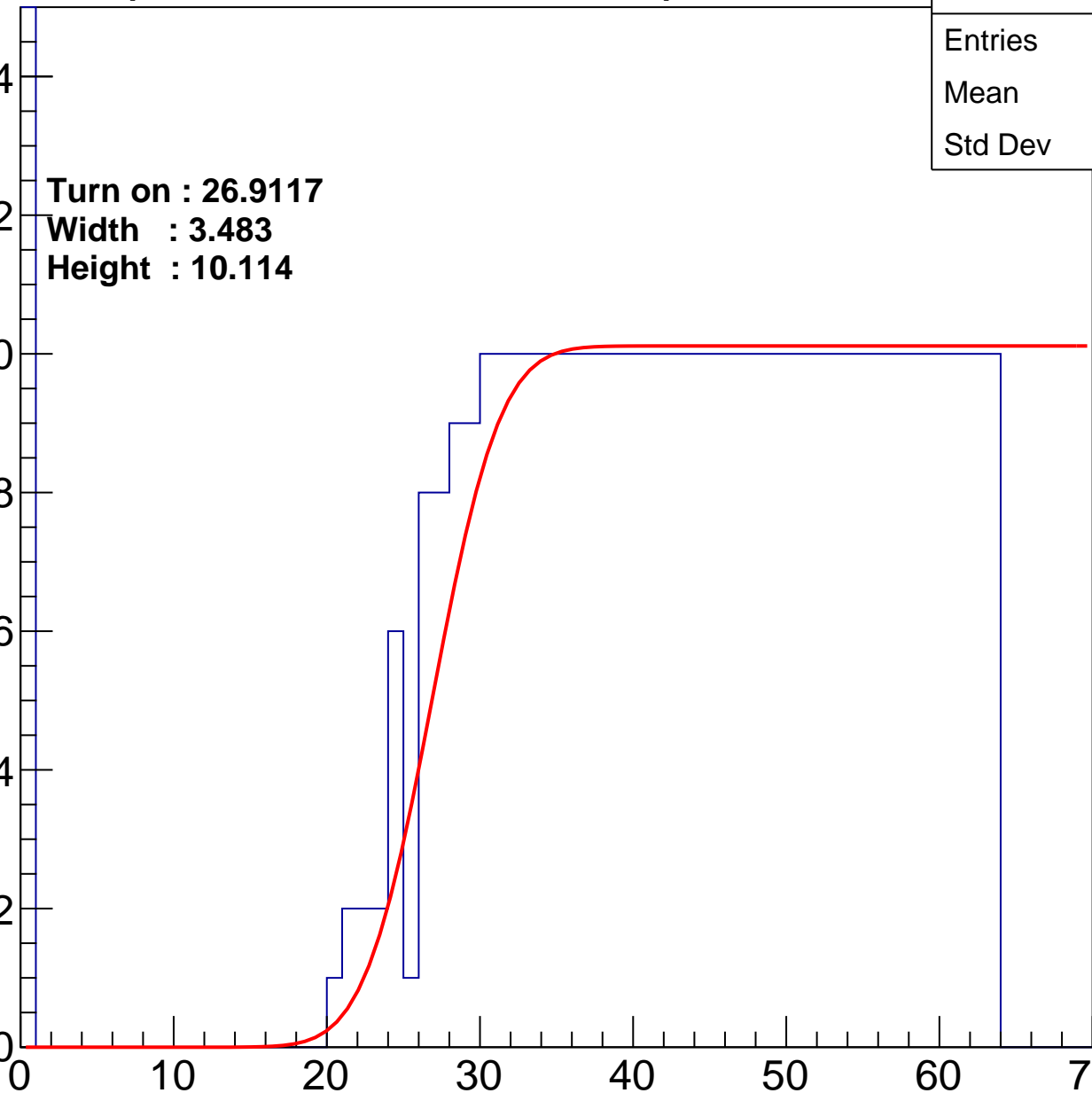
Width : 3.483

Height : 10.114

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch125

calib_packv5_041523_1651.root, FC#0, port C2

Entries	442
Mean	37.96
Std Dev	18.82

Turn on : 27.3442

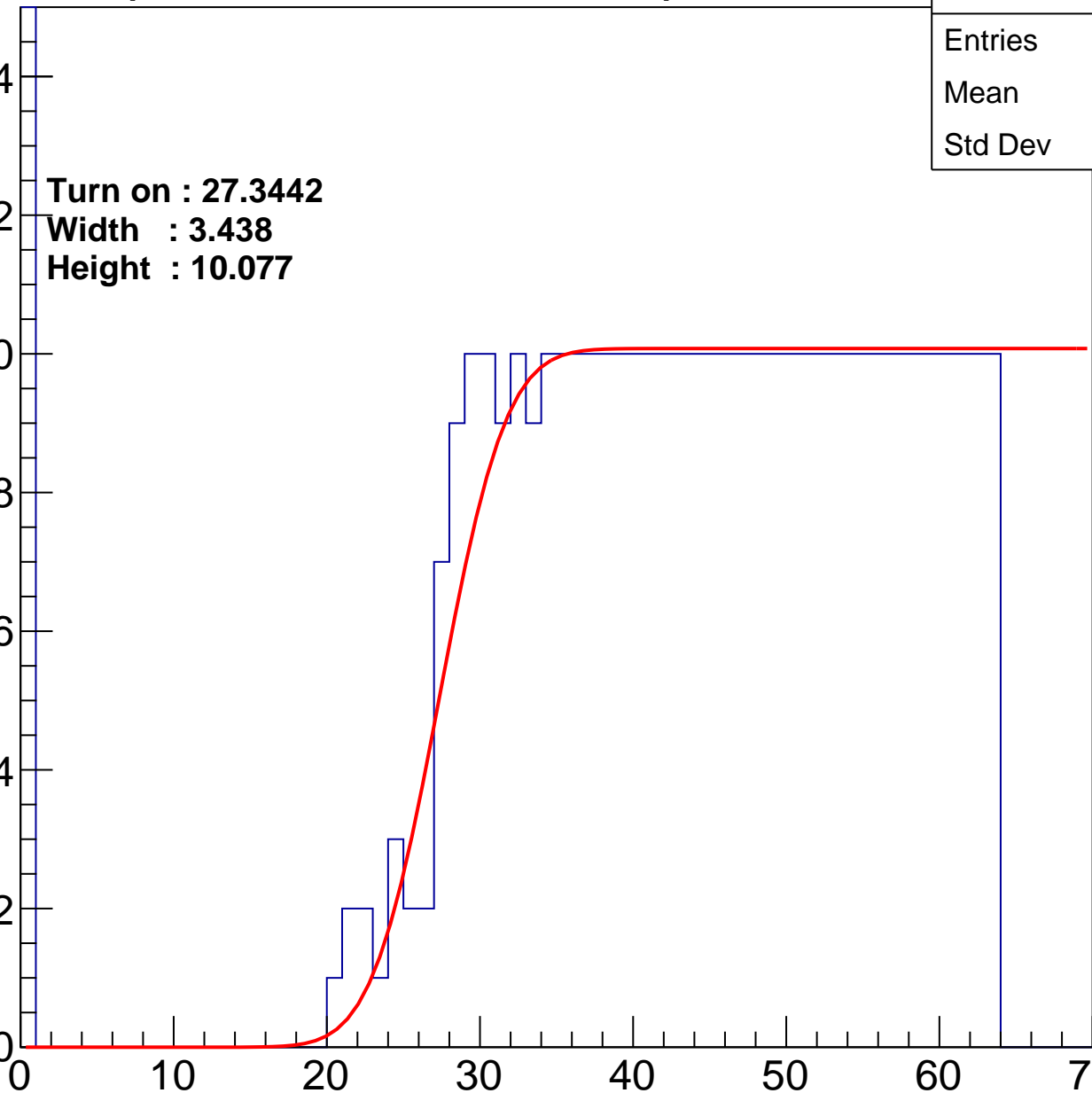
Width : 3.438

Height : 10.077

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch126

calib_packv5_041523_1651.root, FC#0, port C2

Entries	464
Mean	37.66
Std Dev	18.15

Turn on : 23.3474

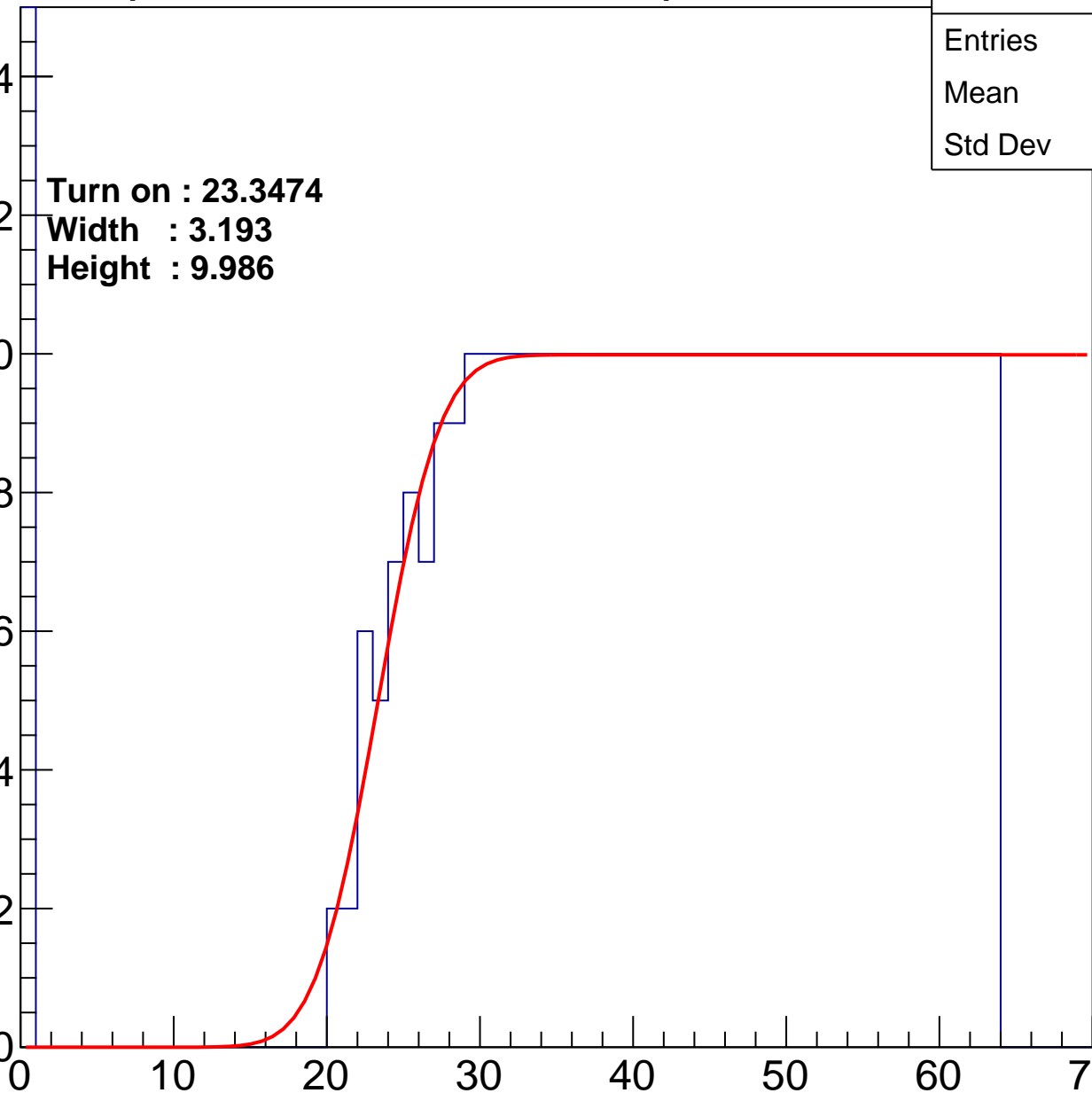
Width : 3.193

Height : 9.986

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch127

calib_packv5_041523_1651.root, FC#0, port C2

Entries	432
Mean	38.96
Std Dev	17.95

Turn on : 26.7176

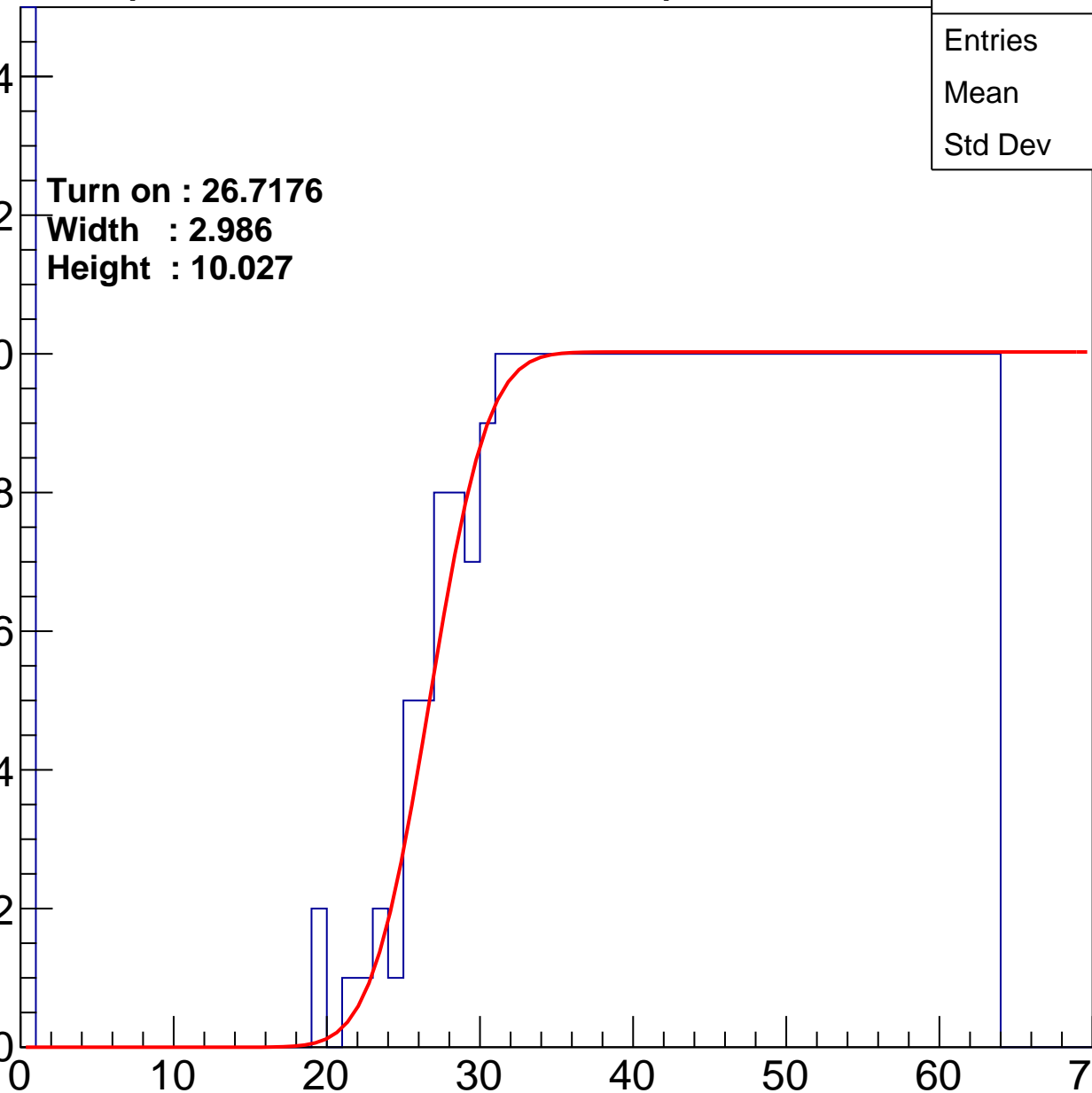
Width : 2.986

Height : 10.027

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U5-ch127

calib_packv5_041523_1651.root, FC#0, port C2

Entries	432
Mean	38.96
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Turn on : 26.7176

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Entry

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