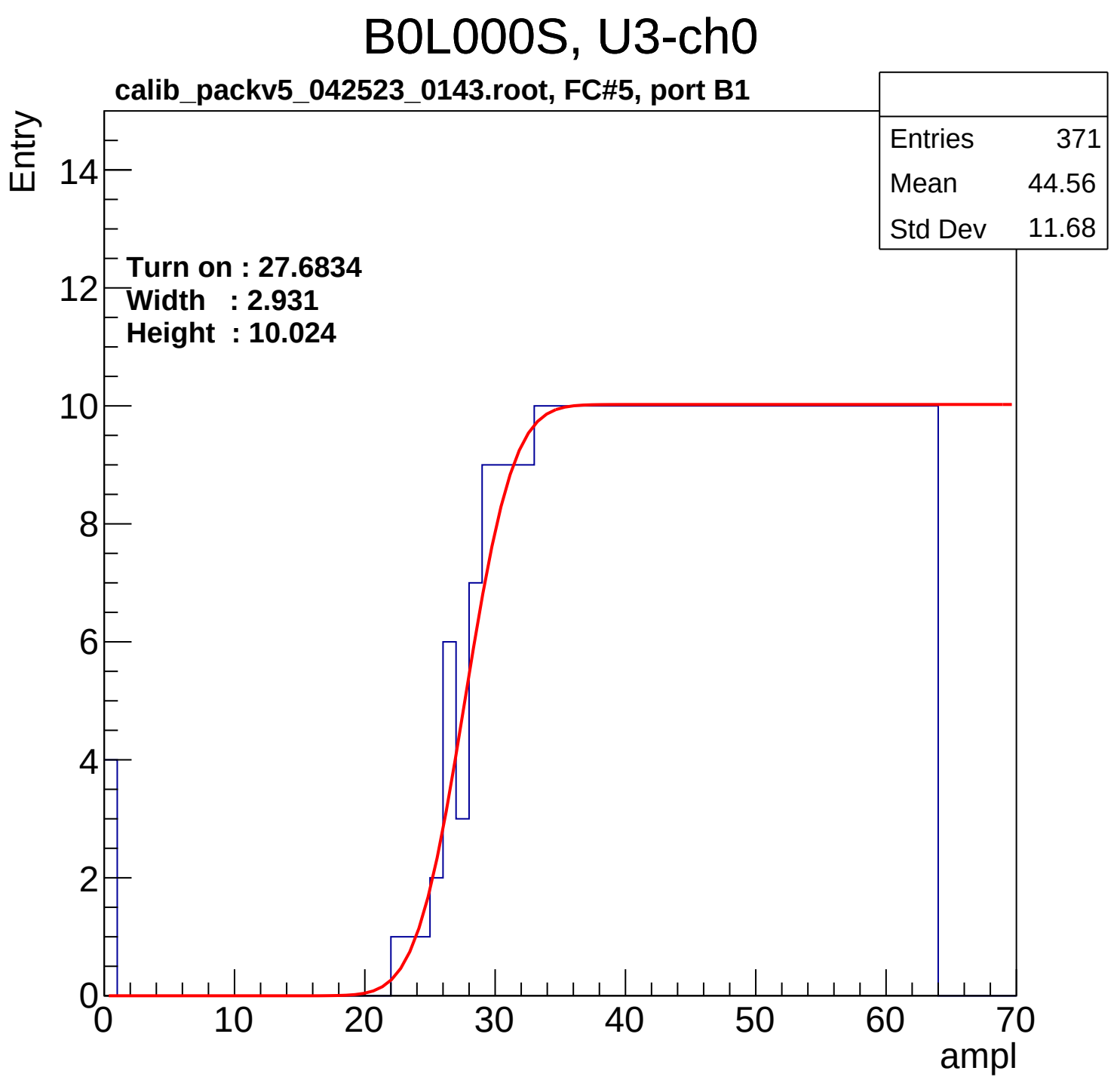
B0L000S, U3-ch0
calib_packv5_042523_0143.root, FC#5, port B1
Entries 371
Mean 44.56
Std Dev 11.68
Turn on : 27.6834
Width : 2.931
Height : 10.024
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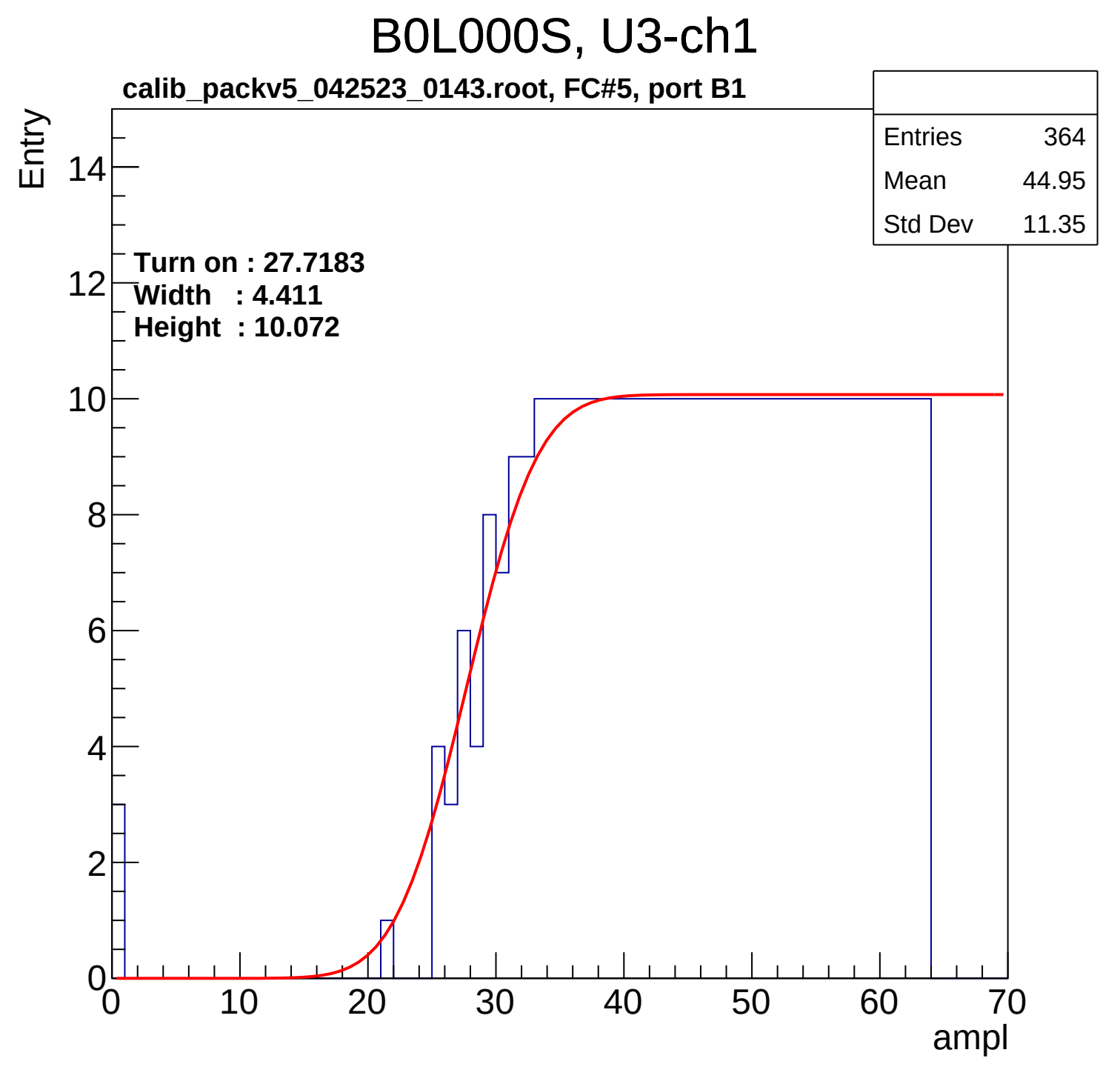
B0L000S, U3-ch1
calib_packv5_042523_0143.root, FC#5, port B1
Entries 364
Mean 44.95
Std Dev 11.35
Turn on : 27.7183
Width : 4.411
Height : 10.072
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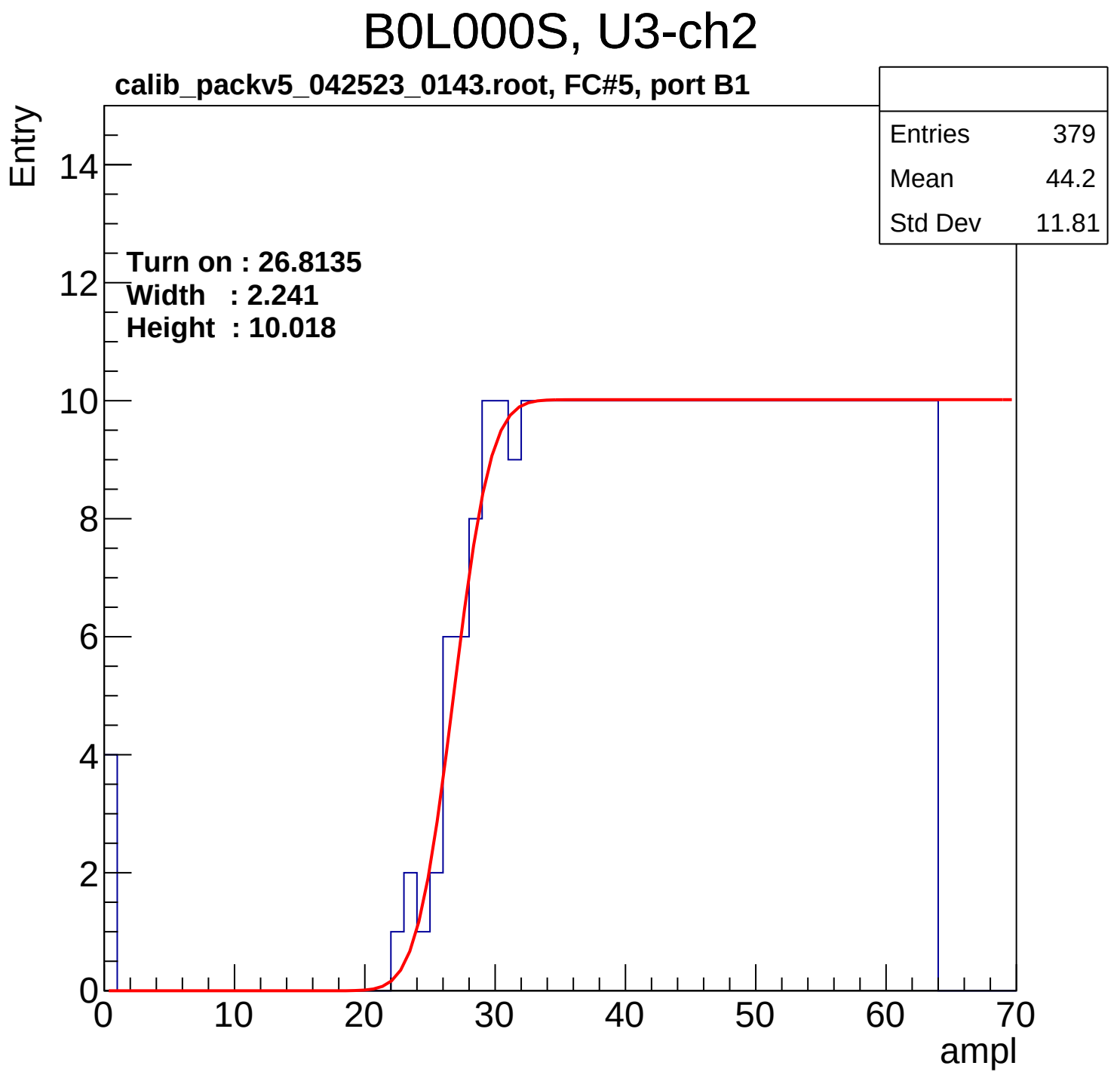
B0L000S, U3-ch2
calib_packv5_042523_0143.root, FC#5, port B1
Entries 379
Mean 44.2
Std Dev 11.81
Turn on : 26.8135
Width : 2.241
Height : 10.018
Entry
ampl
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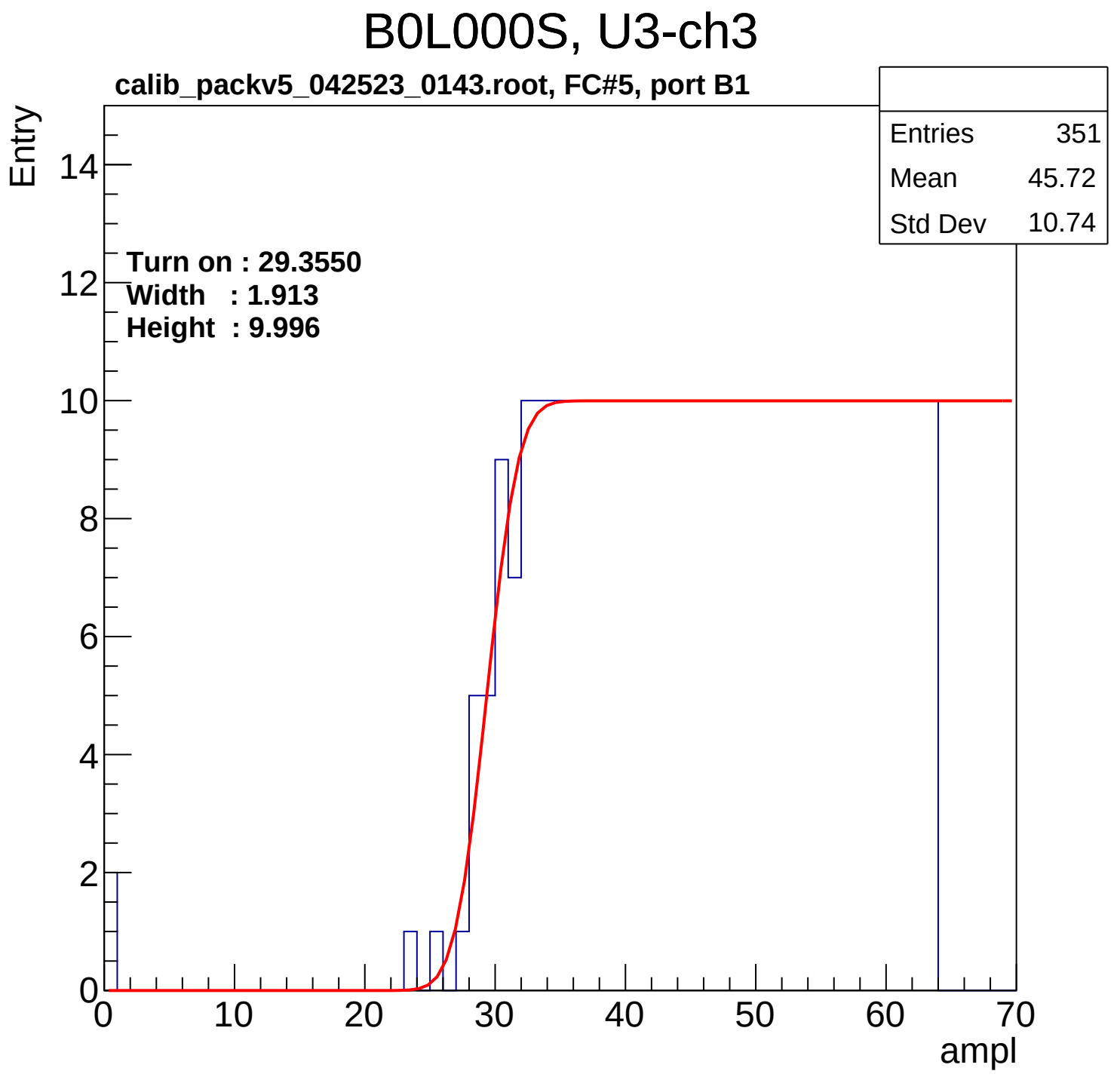
B0L000S, U3-ch3
calib_packv5_042523_0143.root, FC#5, port B1
Entries 351
Mean 45.72
Std Dev 10.74
Turn on : 29.3550
Width : 1.913
Height : 9.996
Entry
ampl
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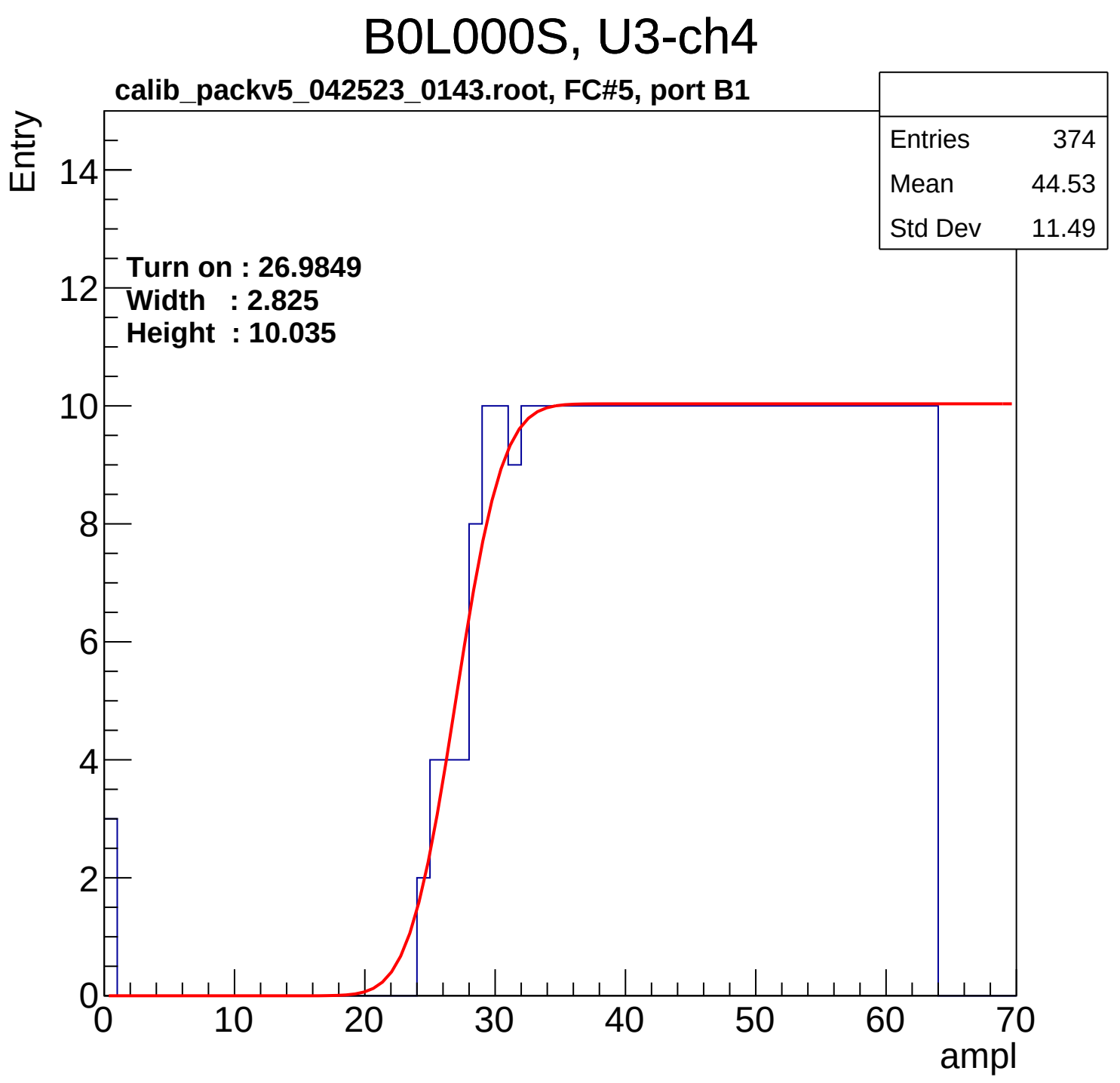
B0L000S, U3-ch4
calib_packv5_042523_0143.root, FC#5, port B1
Entries 374
Mean 44.53
Std Dev 11.49
Turn on : 26.9849
Width : 2.825
Height : 10.035
Entry
ampl
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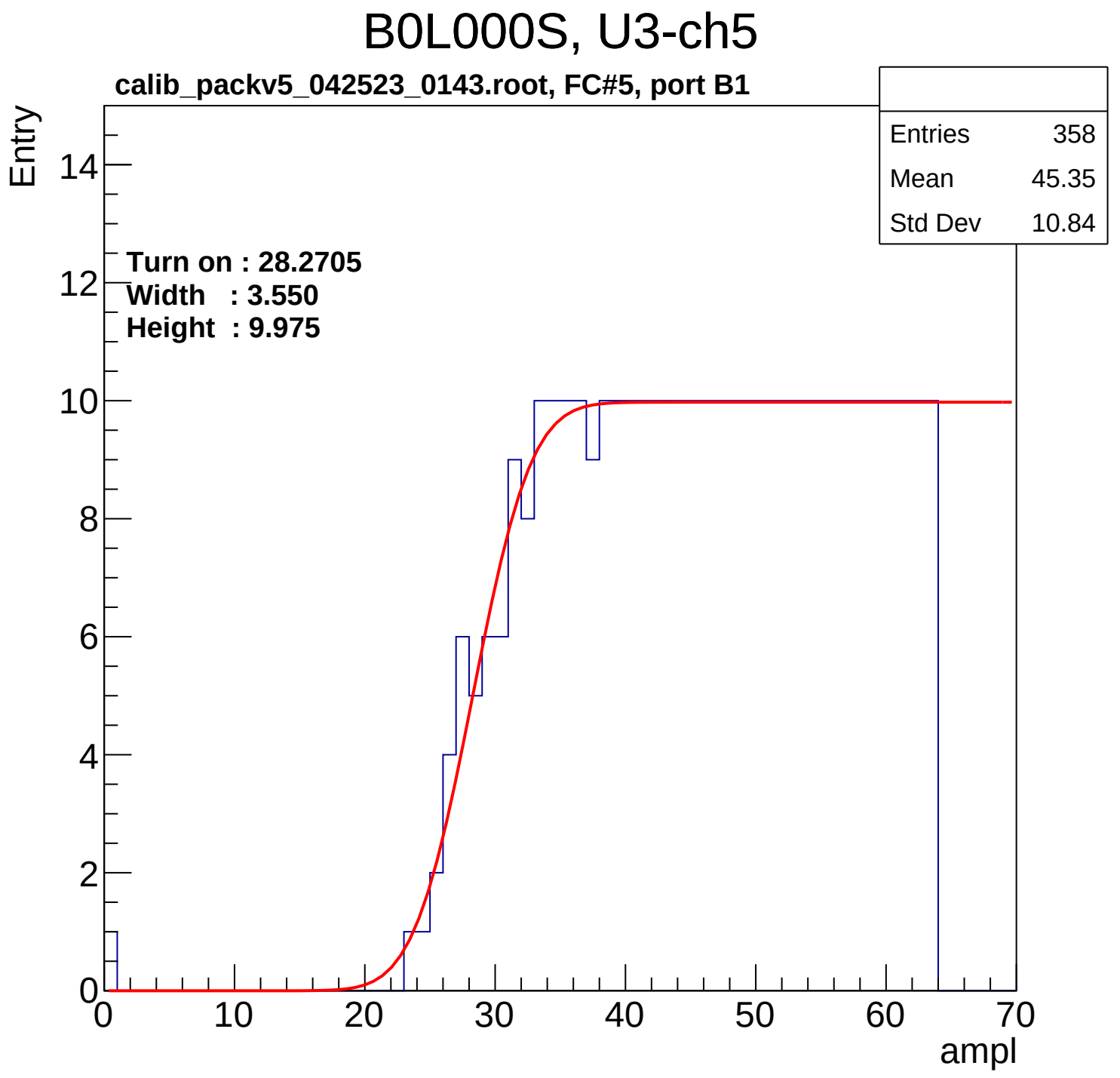
B0L000S, U3-ch5
calib_packv5_042523_0143.root, FC#5, port B1
Entries 358
Mean 45.35
Std Dev 10.84
Turn on : 28.2705
Width : 3.550
Height : 9.975
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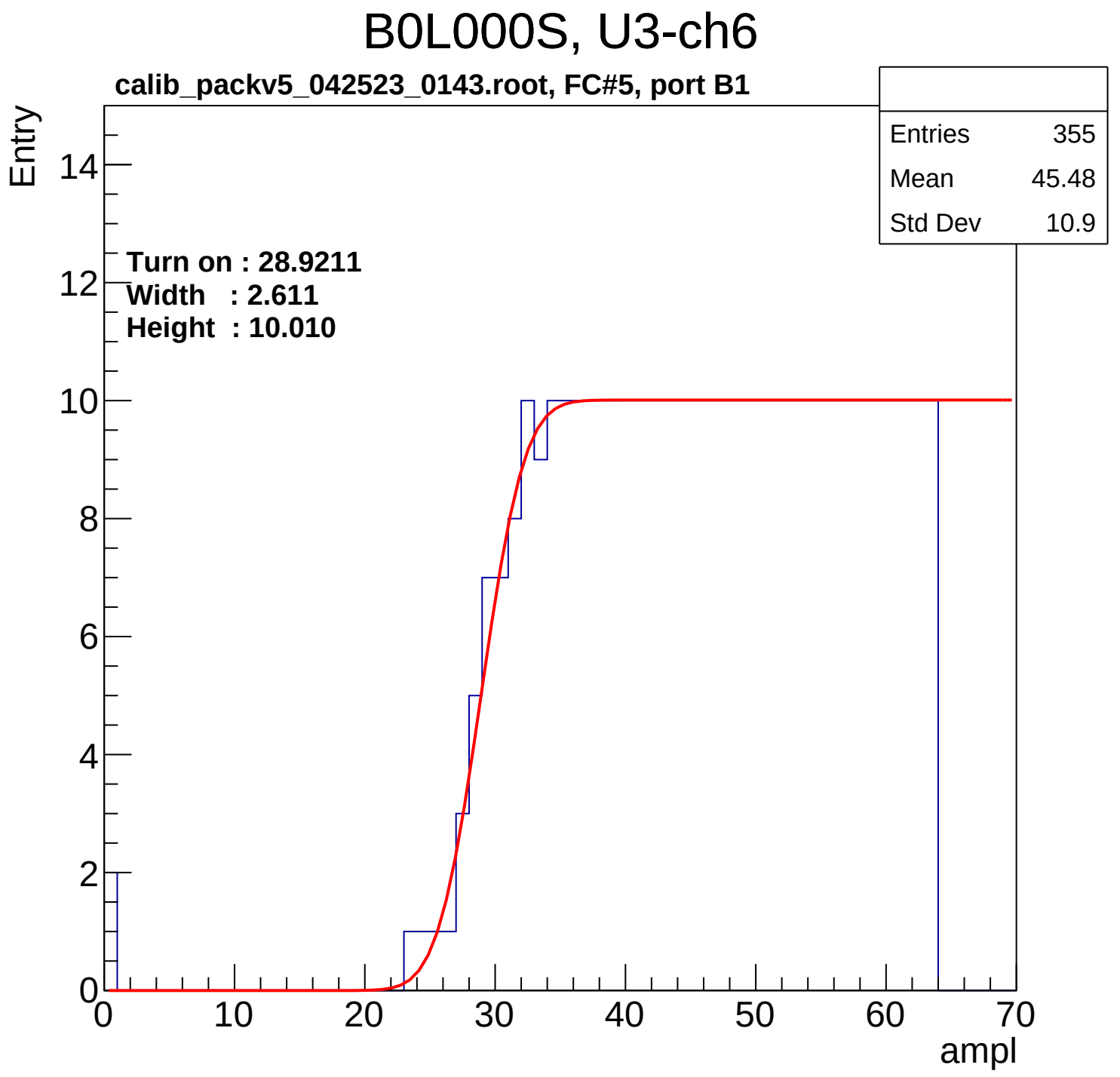
B0L000S, U3-ch6
calib_packv5_042523_0143.root, FC#5, port B1
Entries 355
Mean 45.48
Std Dev 10.9
Turn on : 28.9211
Width : 2.611
Height : 10.010
Entry
ampl
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6
8
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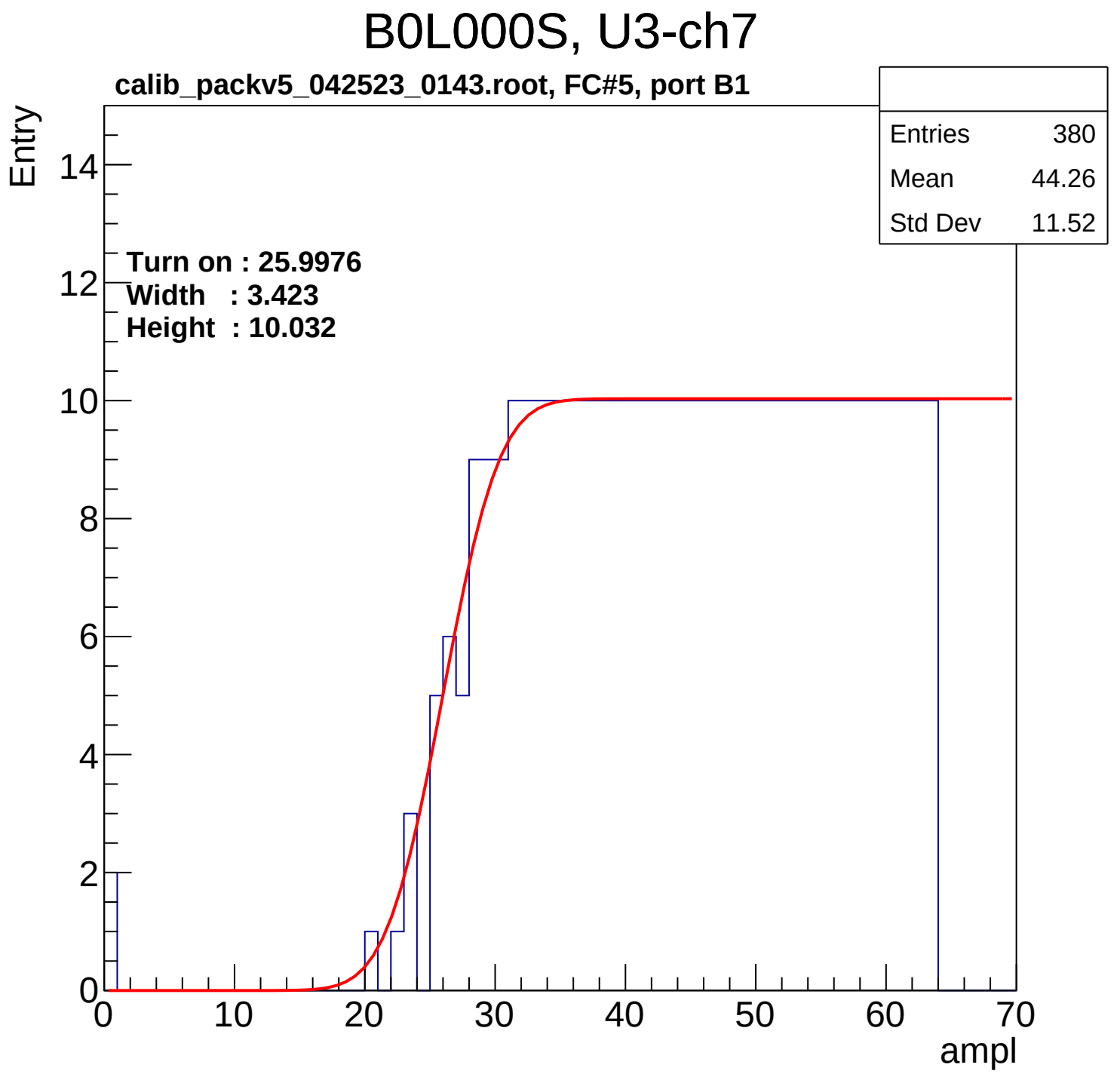
B0L000S, U3-ch7
calib_packv5_042523_0143.root, FC#5, port B1
Entries 380
Mean 44.26
Std Dev 11.52
Turn on : 25.9976
Width : 3.423
Height : 10.032
Entry
ampl
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8
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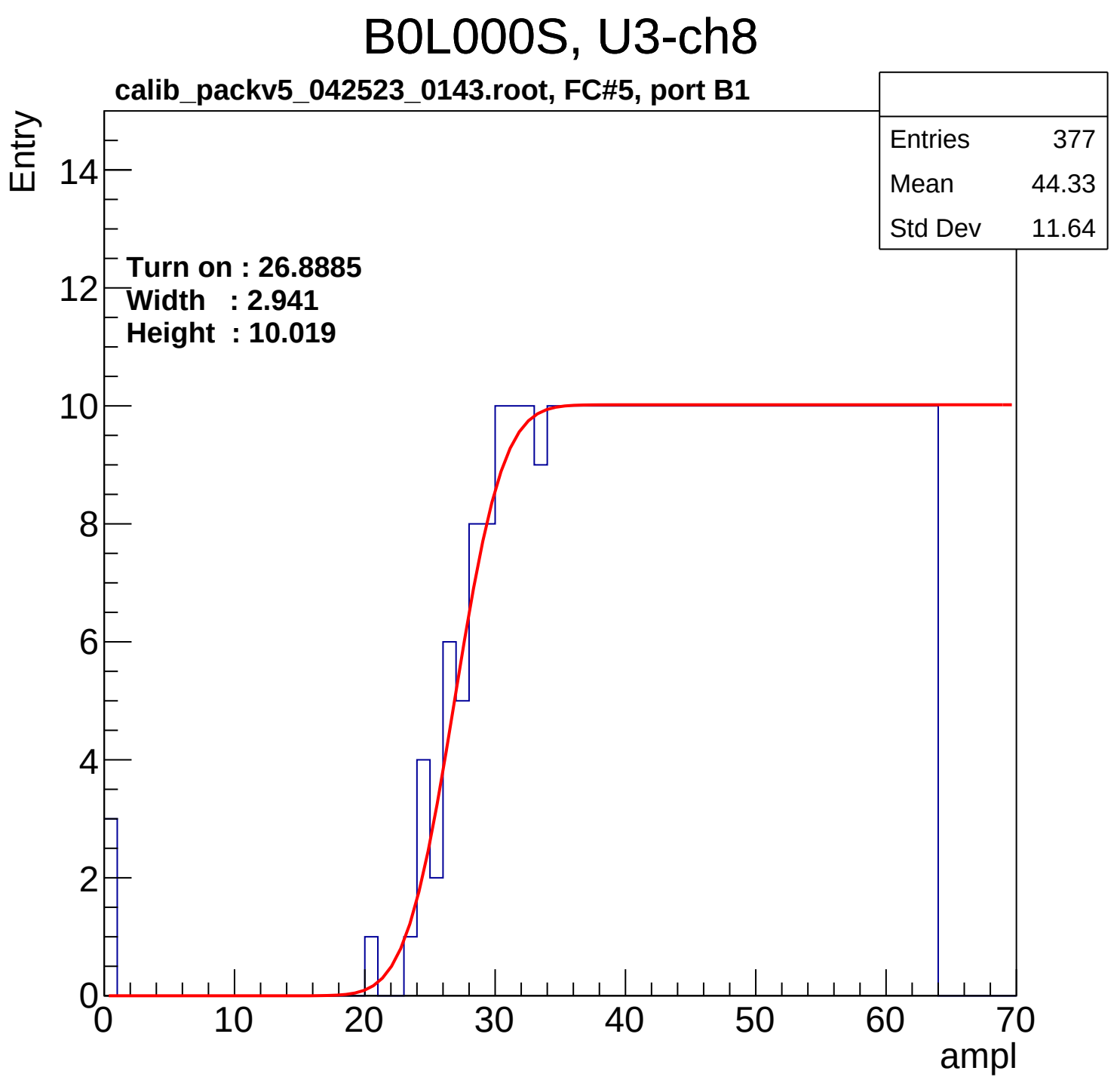
B0L000S, U3-ch8
calib_packv5_042523_0143.root, FC#5, port B1
Entries 377
Mean 44.33
Std Dev 11.64
Turn on : 26.8885
Width : 2.941
Height : 10.019
Entry
ampl
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2
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6
8
10
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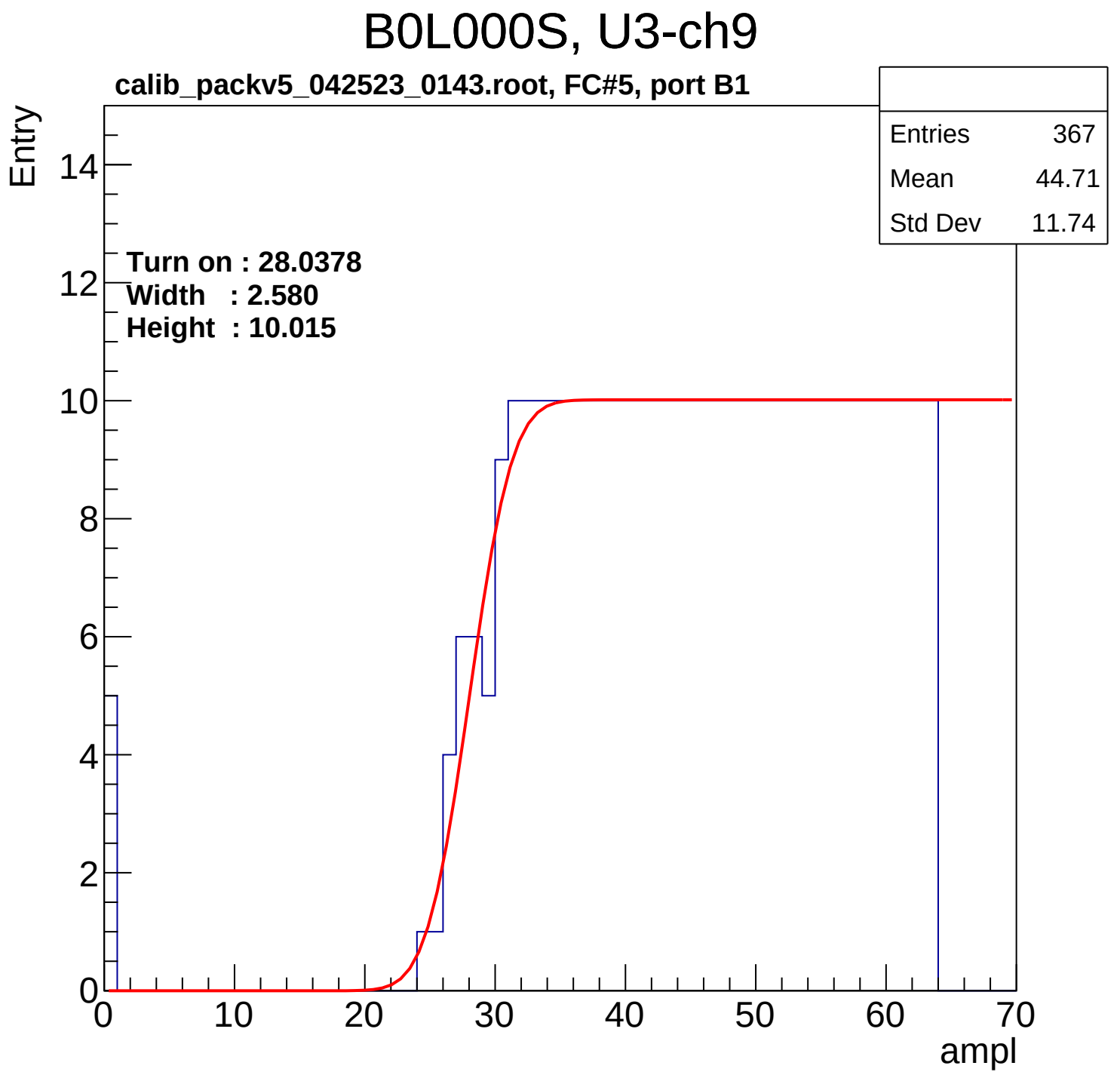
B0L000S, U3-ch9
calib_packv5_042523_0143.root, FC#5, port B1
Entries 367
Mean 44.71
Std Dev 11.74
Turn on : 28.0378
Width : 2.580
Height : 10.015
Entry
ampl
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6
8
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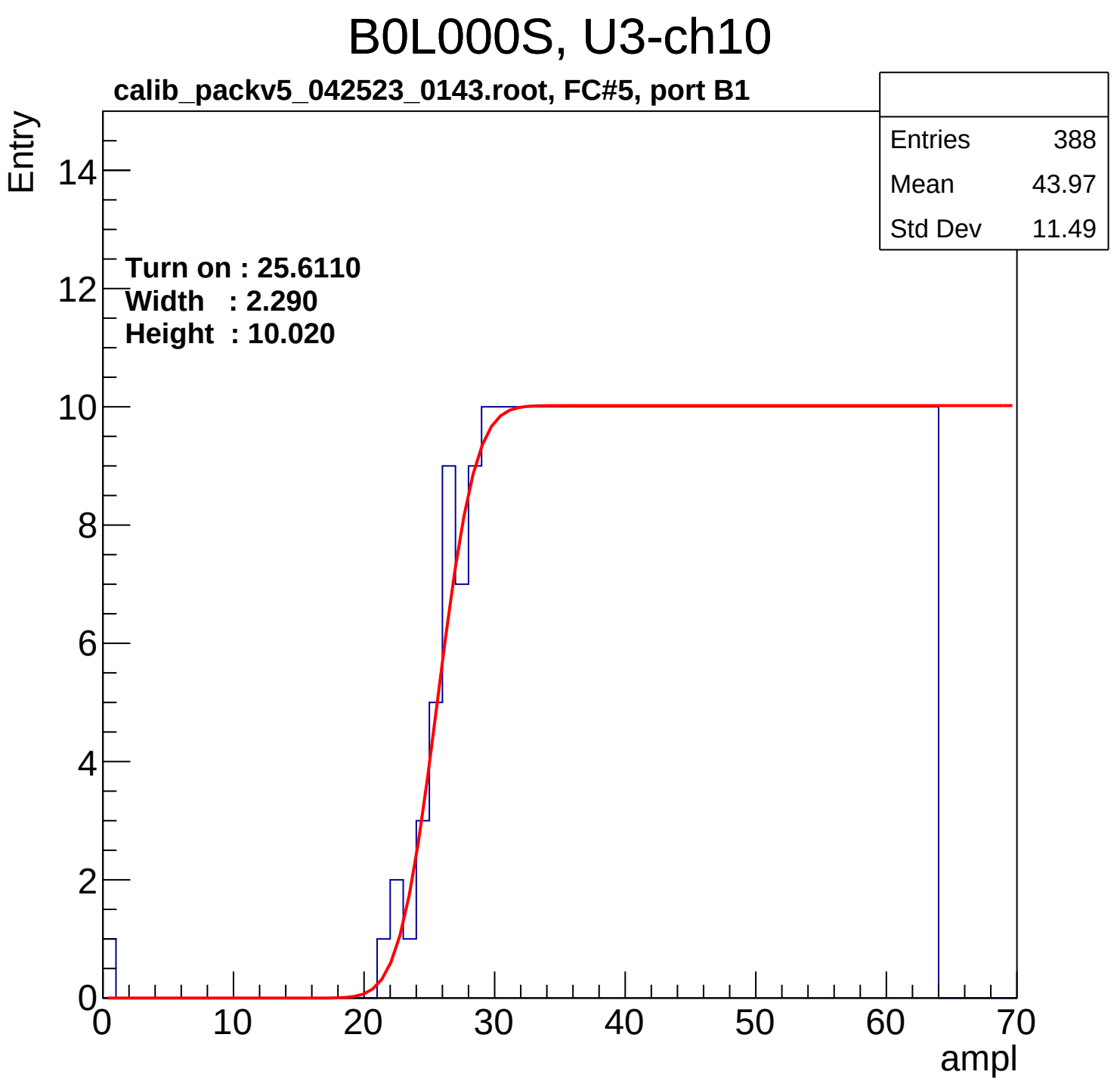
B0L000S, U3-ch10
calib_packv5_042523_0143.root, FC#5, port B1
Entries 388
Mean 43.97
Std Dev 11.49
Turn on : 25.6110
Width : 2.290
Height : 10.020
Entry
ampl
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8
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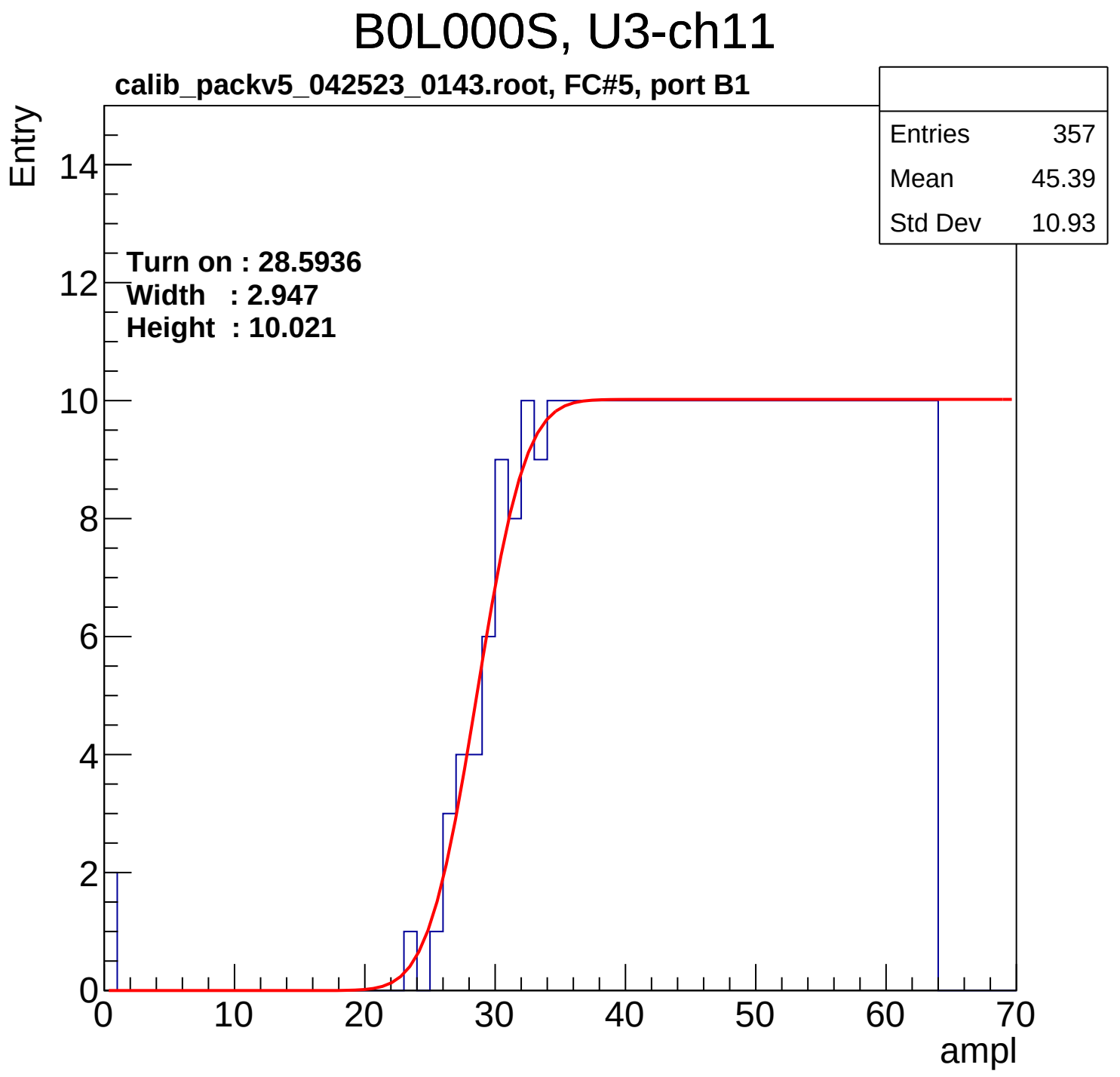
B0L000S, U3-ch11
calib_packv5_042523_0143.root, FC#5, port B1
Entries 357
Mean 45.39
Std Dev 10.93
Turn on : 28.5936
Width : 2.947
Height : 10.021
Entry
ampl
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6
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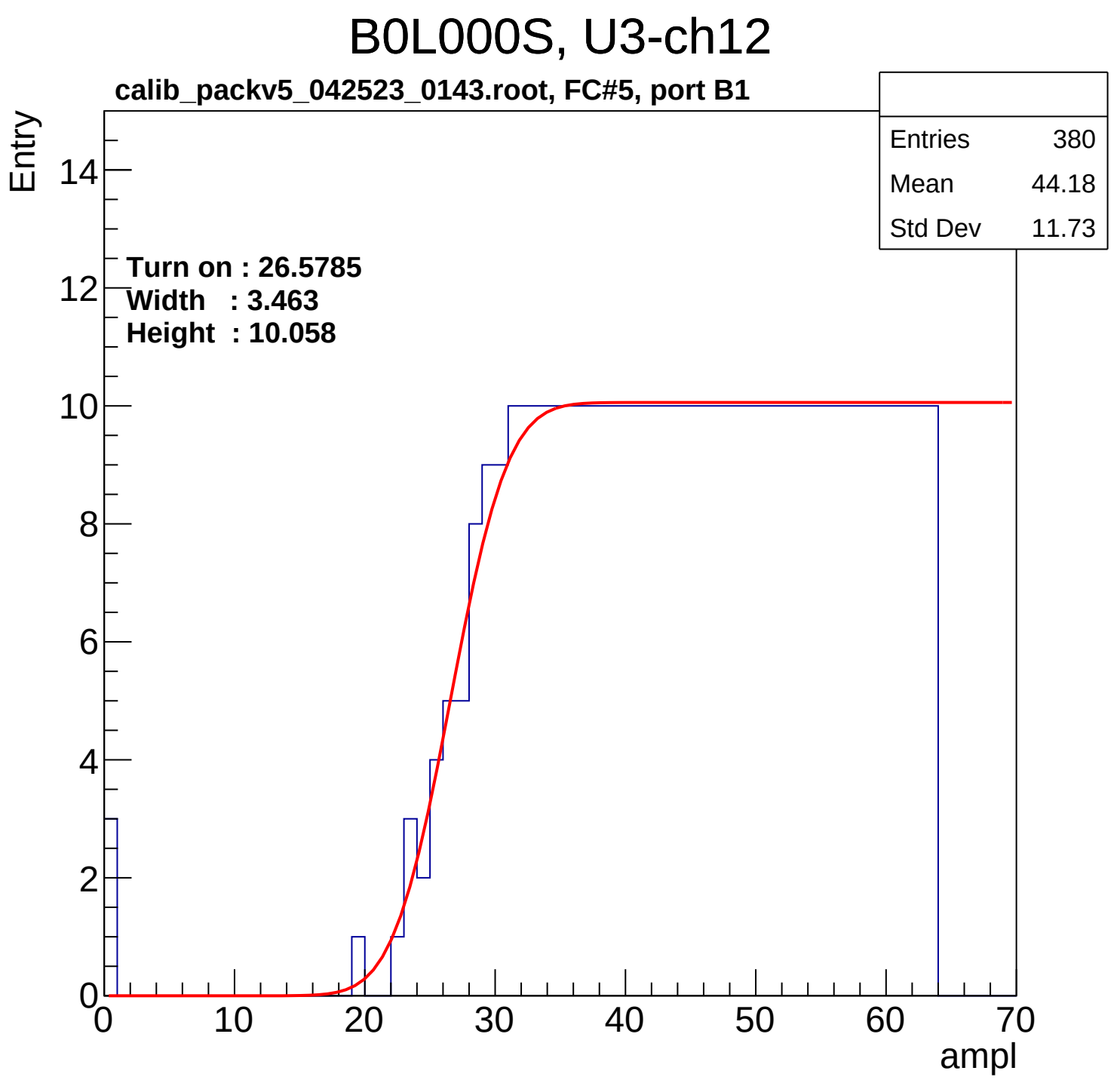
B0L000S, U3-ch12
calib_packv5_042523_0143.root, FC#5, port B1
Entries 380
Mean 44.18
Std Dev 11.73
Turn on : 26.5785
Width : 3.463
Height : 10.058
Entry
ampl
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8
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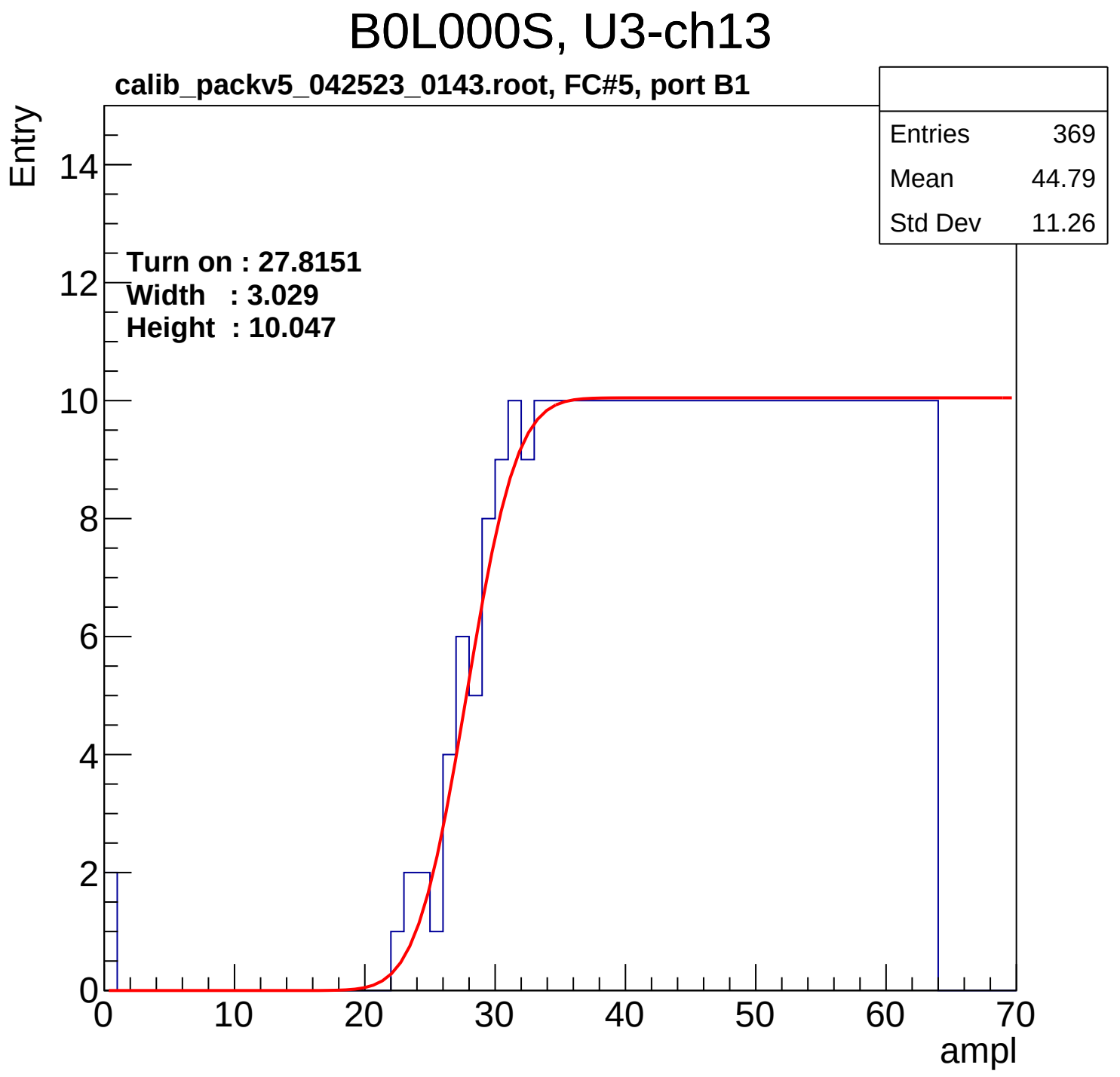
B0L000S, U3-ch13
calib_packv5_042523_0143.root, FC#5, port B1
Entries 369
Mean 44.79
Std Dev 11.26
Turn on : 27.8151
Width : 3.029
Height : 10.047
Entry
ampl
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6
8
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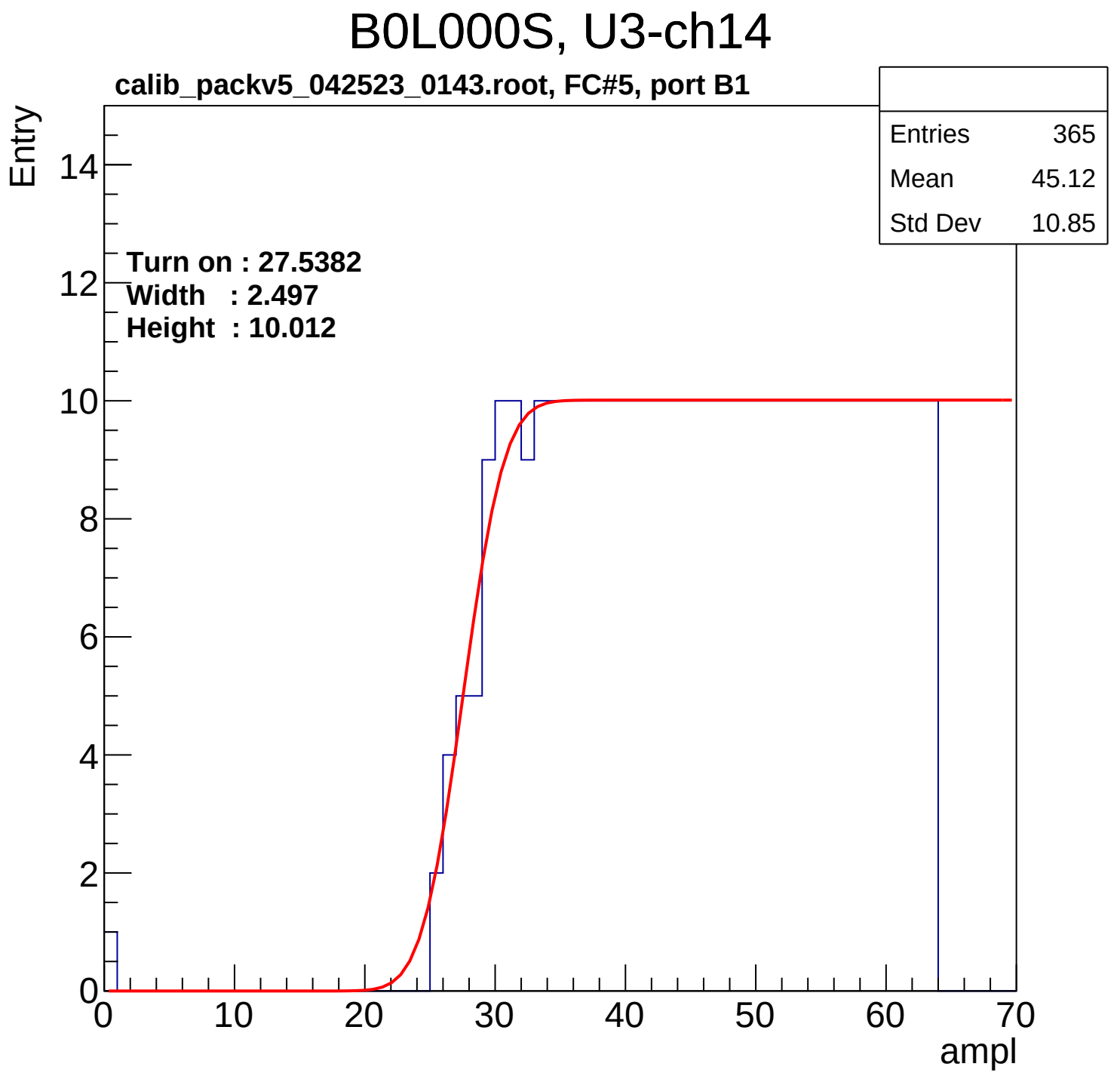
B0L000S, U3-ch14
calib_packv5_042523_0143.root, FC#5, port B1
Entries 365
Mean 45.12
Std Dev 10.85
Turn on : 27.5382
Width : 2.497
Height : 10.012
Entry
ampl
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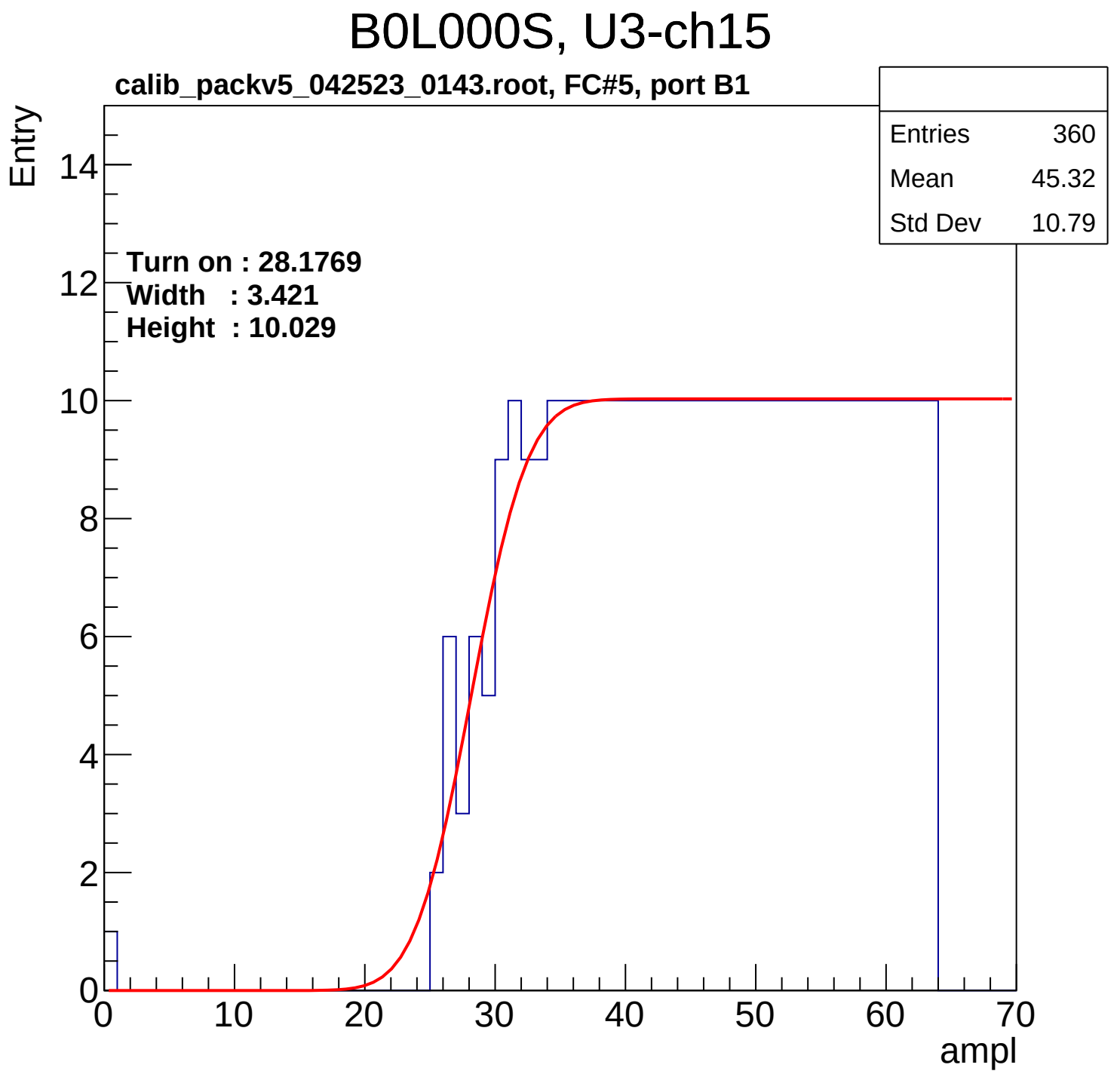
B0L000S, U3-ch15
calib_packv5_042523_0143.root, FC#5, port B1
Entries 360
Mean 45.32
Std Dev 10.79
Turn on : 28.1769
Width : 3.421
Height : 10.029
Entry
ampl
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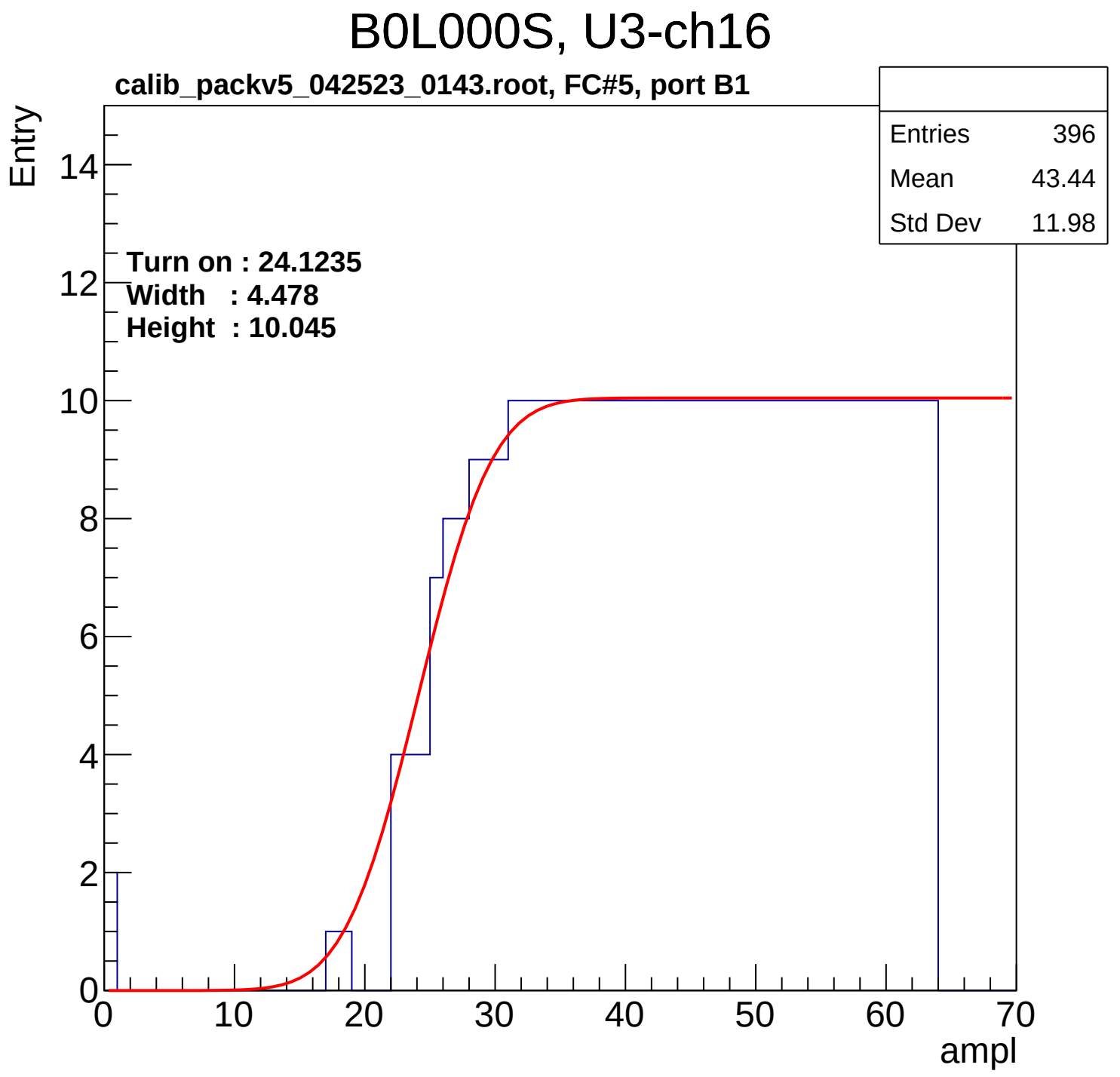
B0L000S, U3-ch16
calib_packv5_042523_0143.root, FC#5, port B1
Entries 396
Mean 43.44
Std Dev 11.98
Turn on : 24.1235
Width : 4.478
Height : 10.045
Entry
ampl
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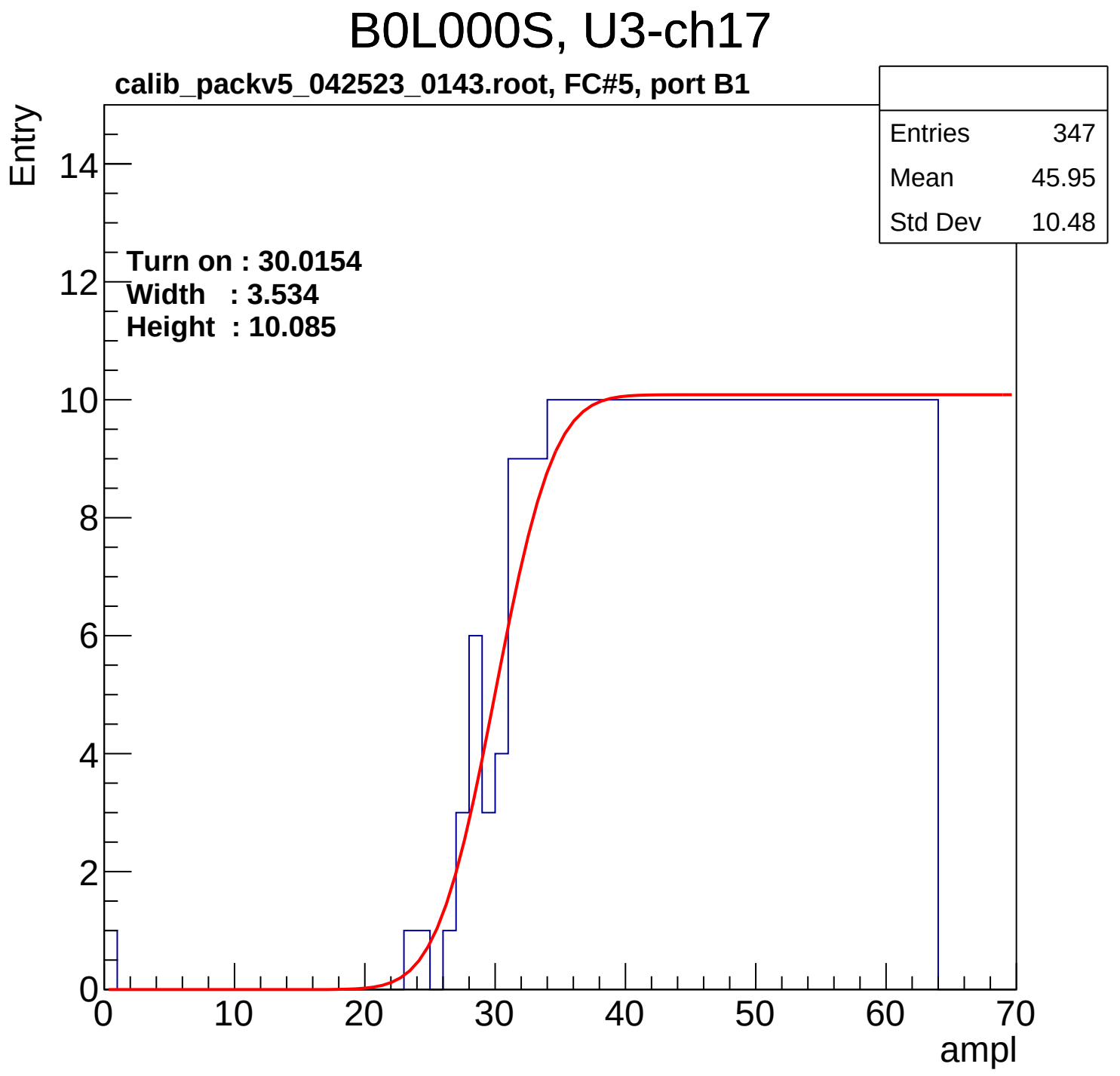
B0L000S, U3-ch17
calib_packv5_042523_0143.root, FC#5, port B1
Entries 347
Mean 45.95
Std Dev 10.48
Turn on : 30.0154
Width : 3.534
Height : 10.085
Entry
ampl
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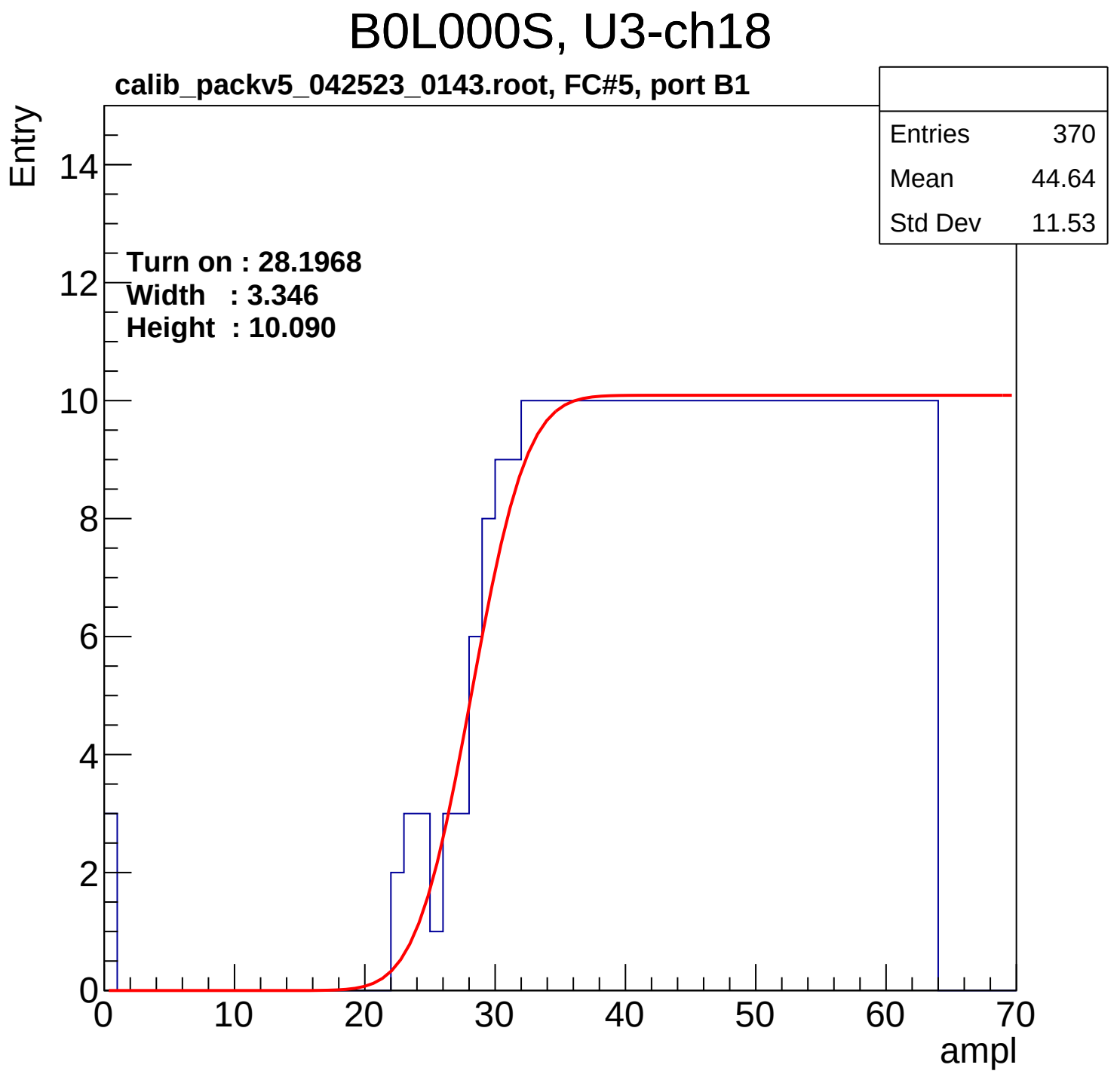
B0L000S, U3-ch18
calib_packv5_042523_0143.root, FC#5, port B1
Entries 370
Mean 44.64
Std Dev 11.53
Turn on : 28.1968
Width : 3.346
Height : 10.090
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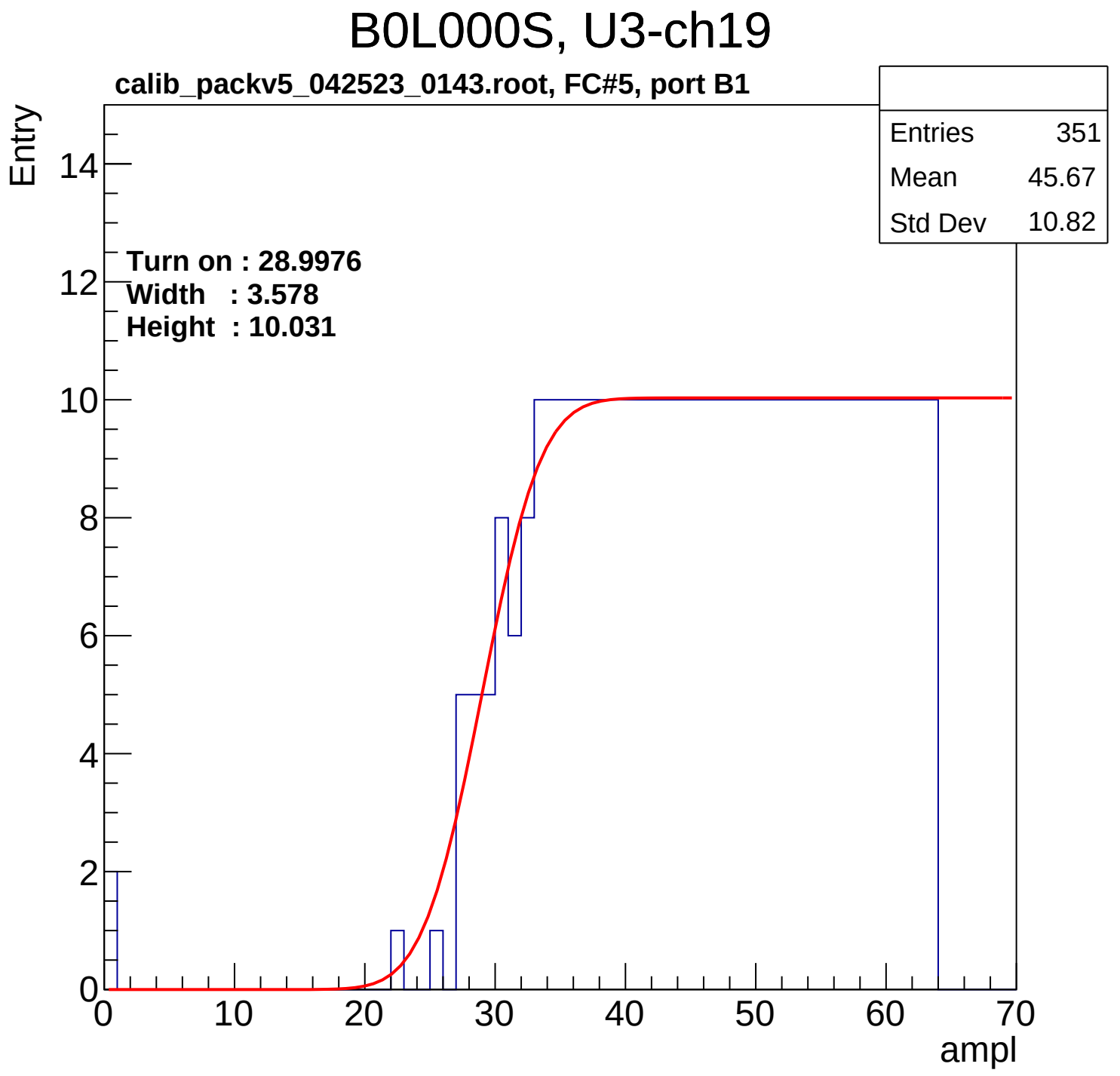
B0L000S, U3-ch19
calib_packv5_042523_0143.root, FC#5, port B1
Entries 351
Mean 45.67
Std Dev 10.82
Turn on : 28.9976
Width : 3.578
Height : 10.031
Entry
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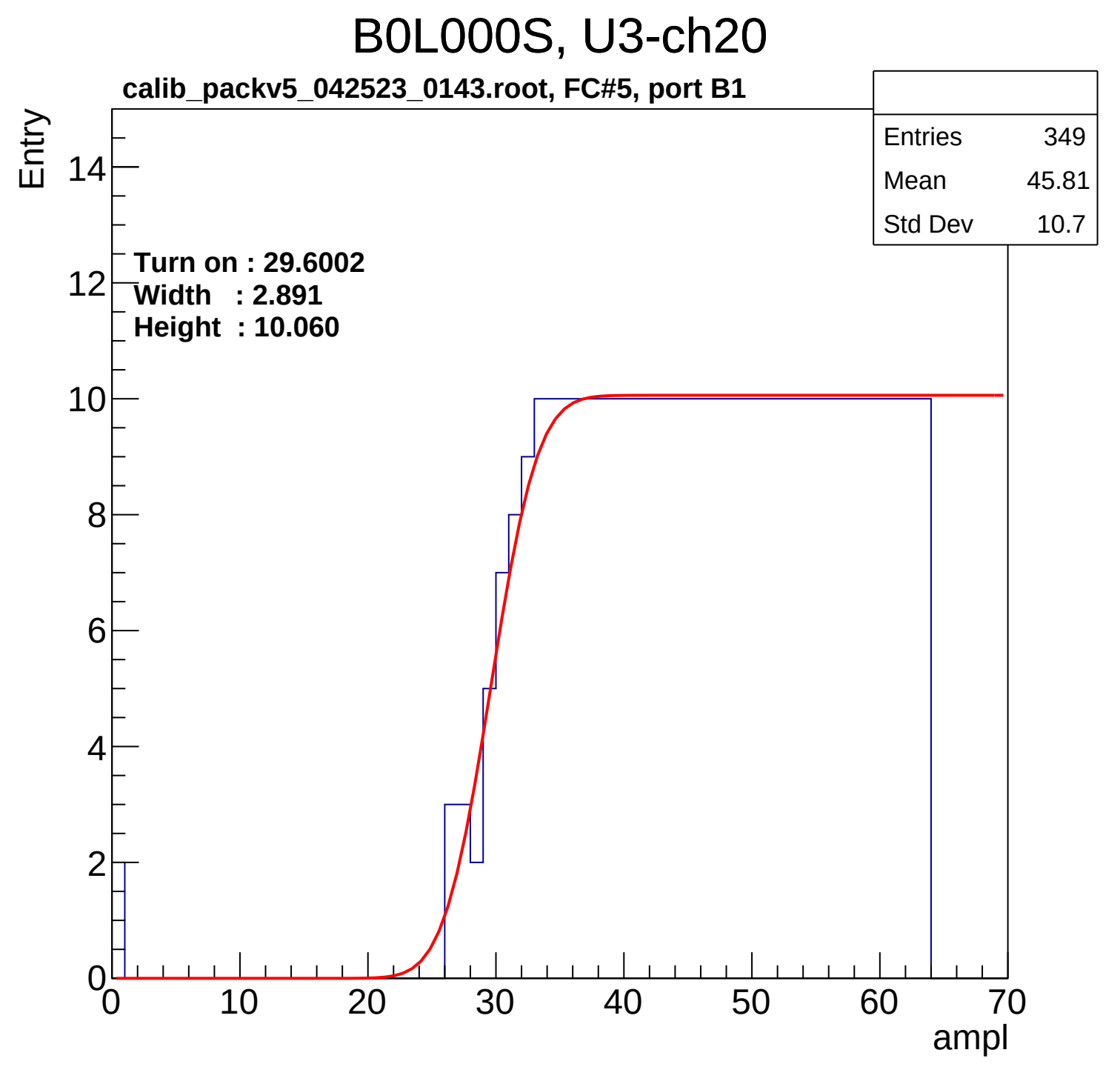
B0L000S, U3-ch20
calib_packv5_042523_0143.root, FC#5, port B1
Entries 349
Mean 45.81
Std Dev 10.7
Turn on : 29.6002
Width : 2.891
Height : 10.060
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ampl
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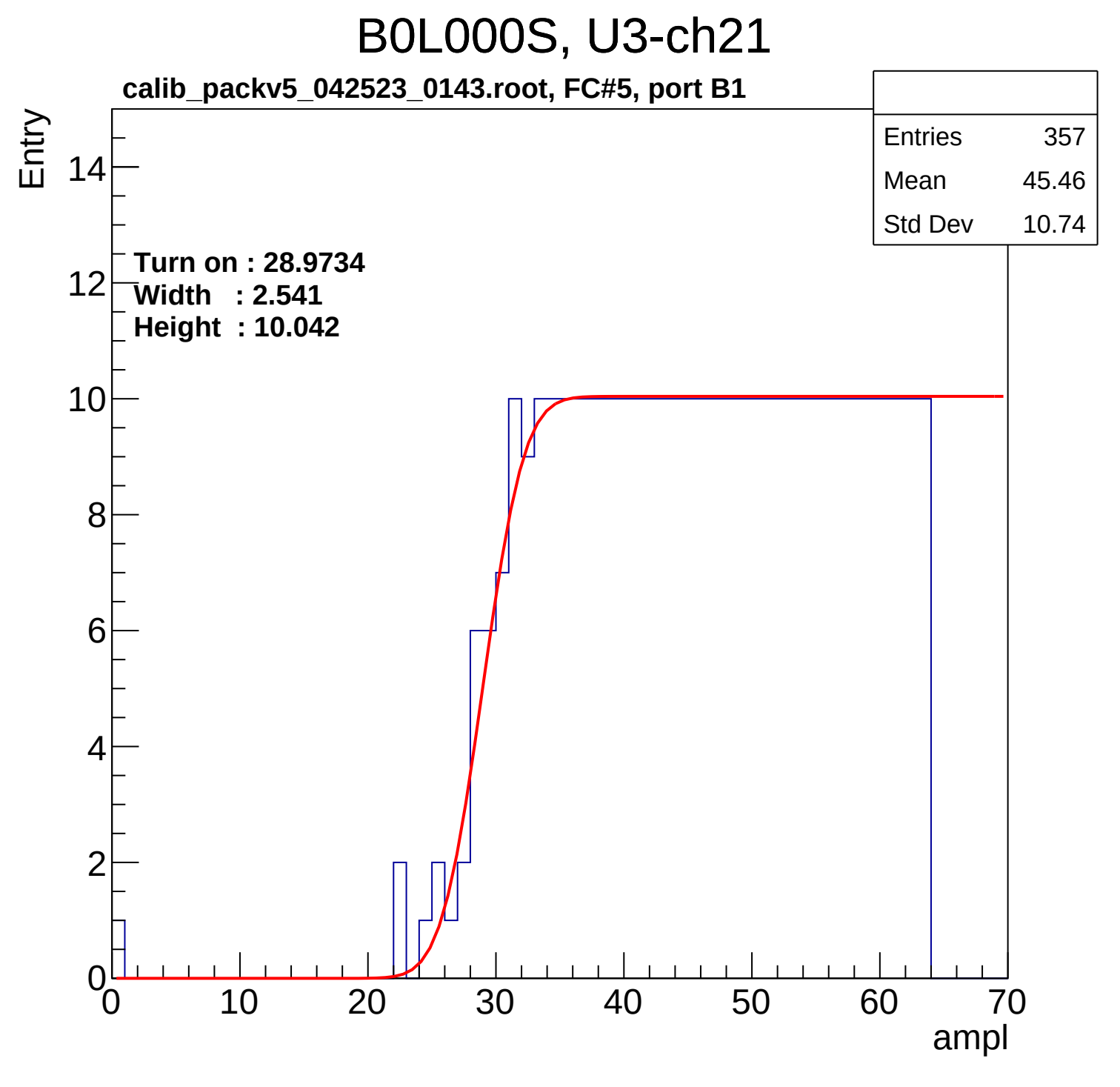
B0L000S, U3-ch21
calib_packv5_042523_0143.root, FC#5, port B1
Entries 357
Mean 45.46
Std Dev 10.74
Turn on : 28.9734
Width : 2.541
Height : 10.042
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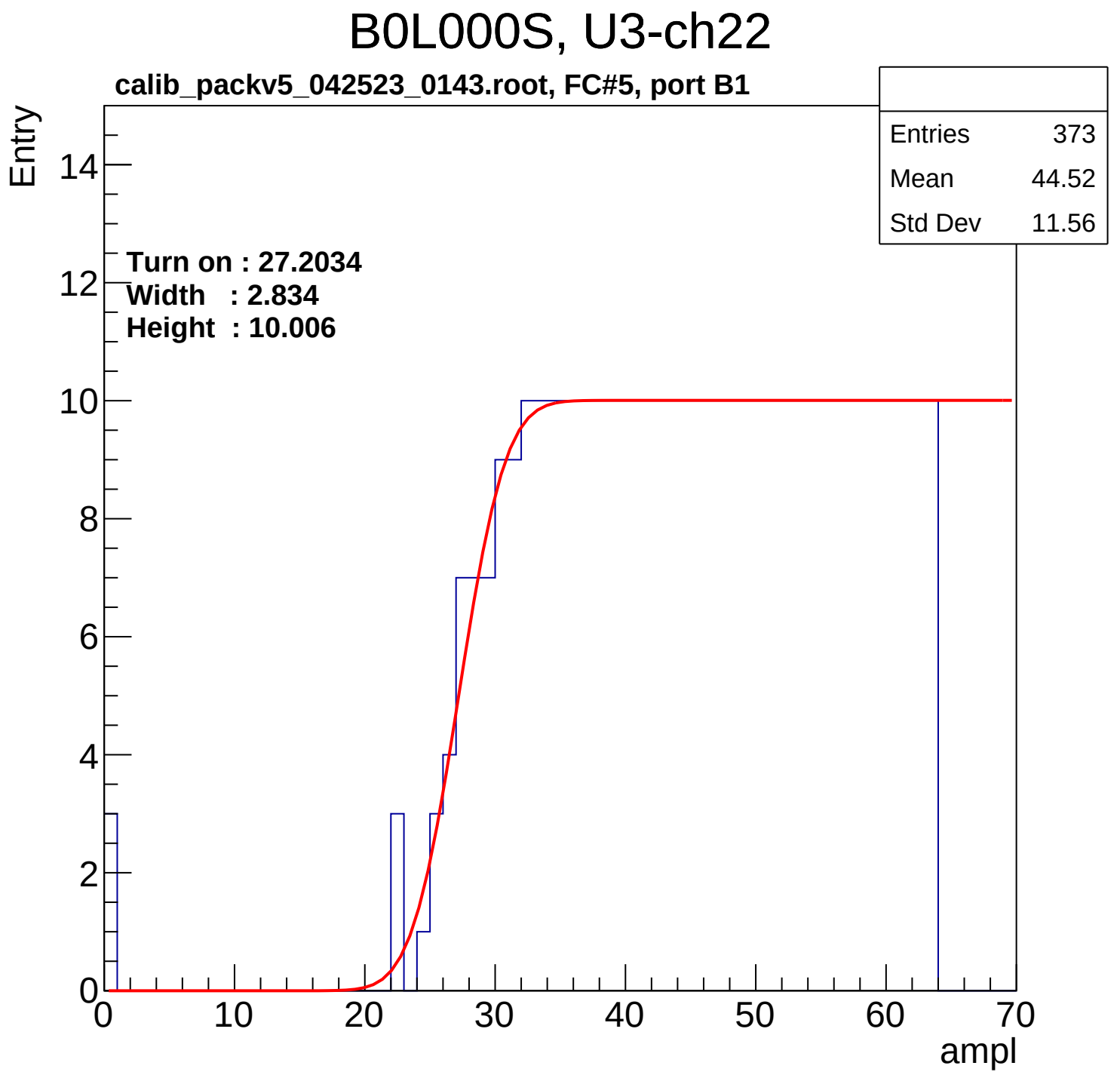
B0L000S, U3-ch22
calib_packv5_042523_0143.root, FC#5, port B1
Entries 373
Mean 44.52
Std Dev 11.56
Turn on : 27.2034
Width : 2.834
Height : 10.006
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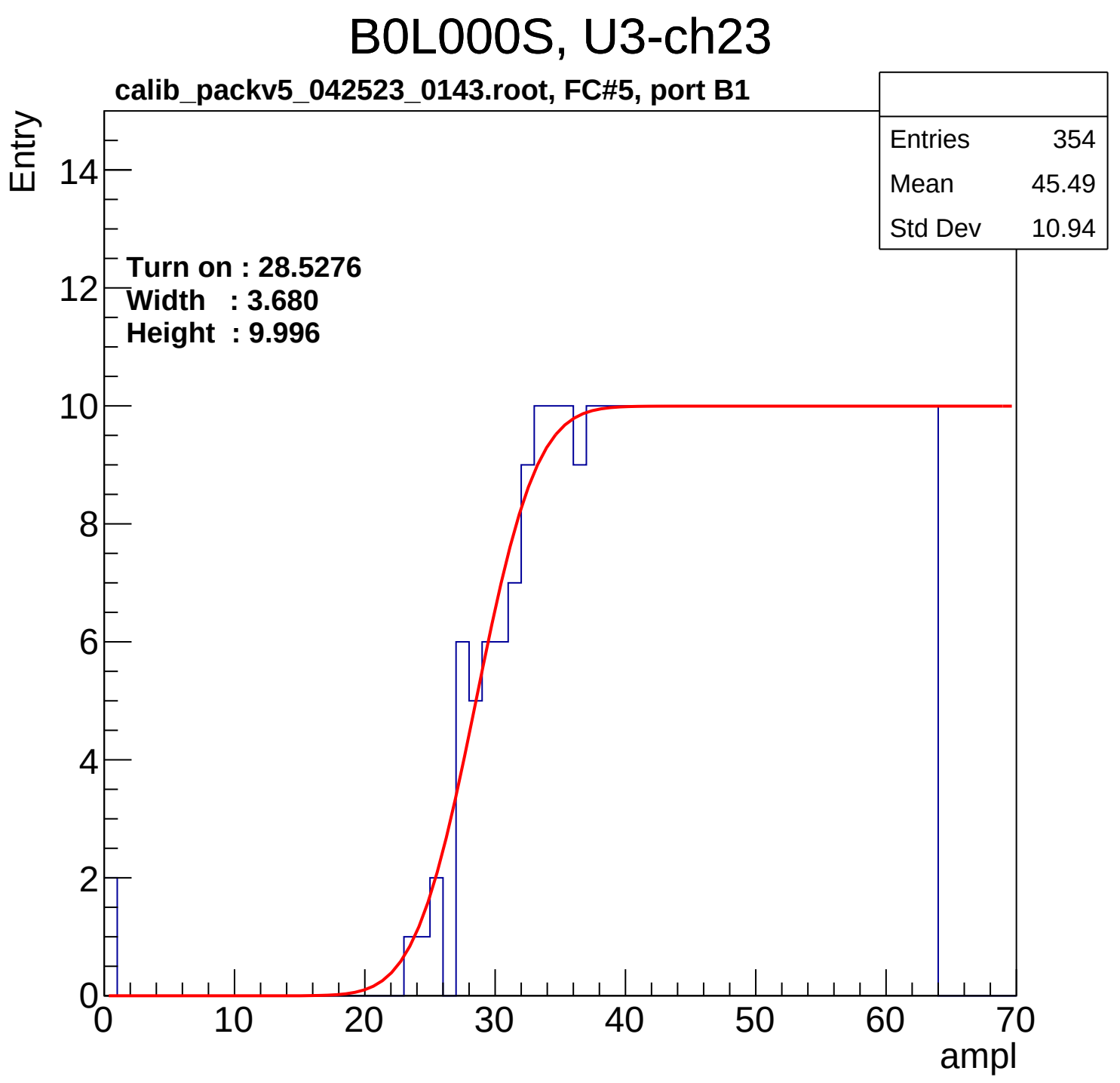
B0L000S, U3-ch23
calib_packv5_042523_0143.root, FC#5, port B1
Entries 354
Mean 45.49
Std Dev 10.94
Turn on : 28.5276
Width : 3.680
Height : 9.996
Entry
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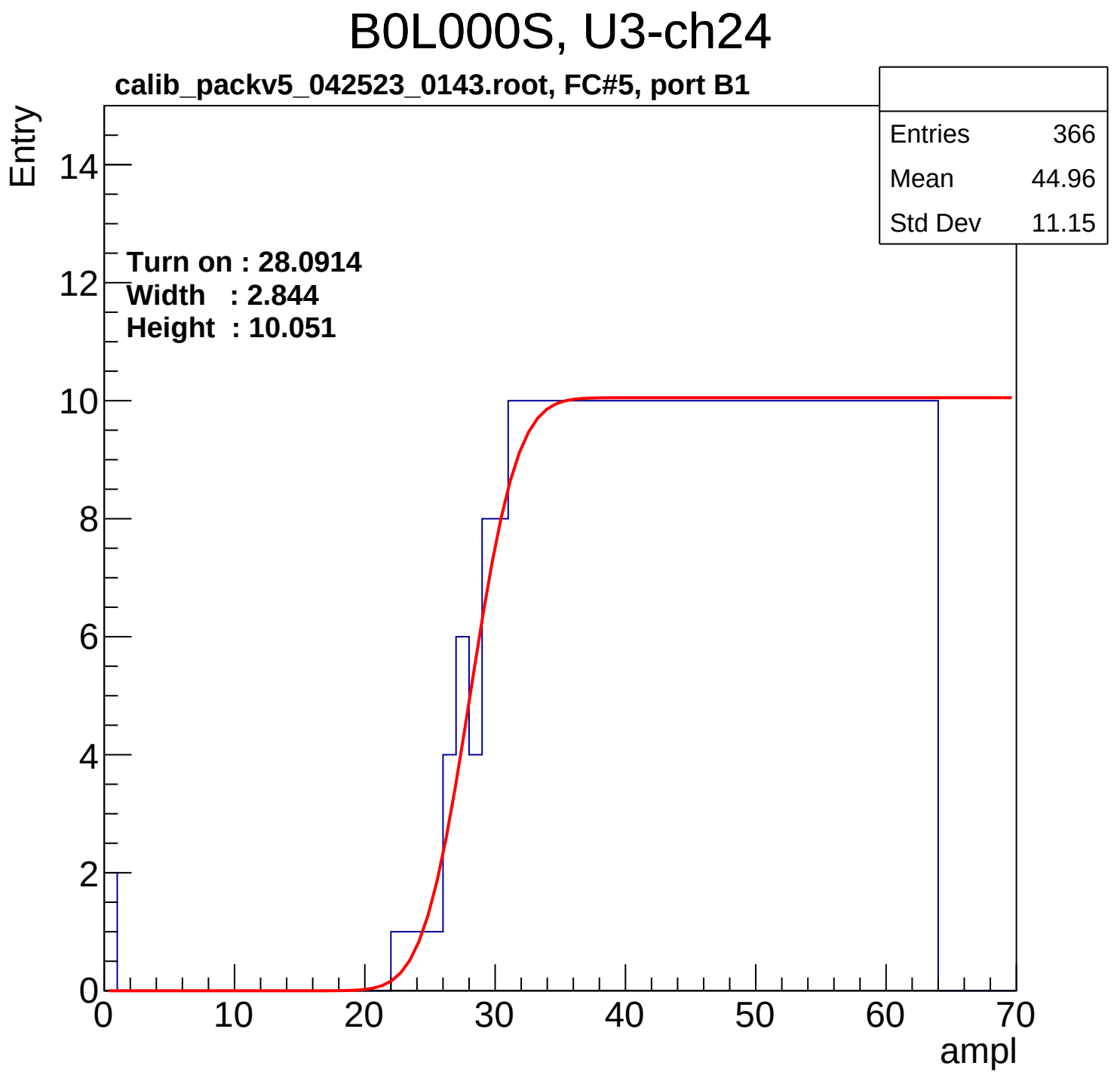
B0L000S, U3-ch24
calib_packv5_042523_0143.root, FC#5, port B1
Entries 366
Mean 44.96
Std Dev 11.15
Turn on : 28.0914
Width : 2.844
Height : 10.051
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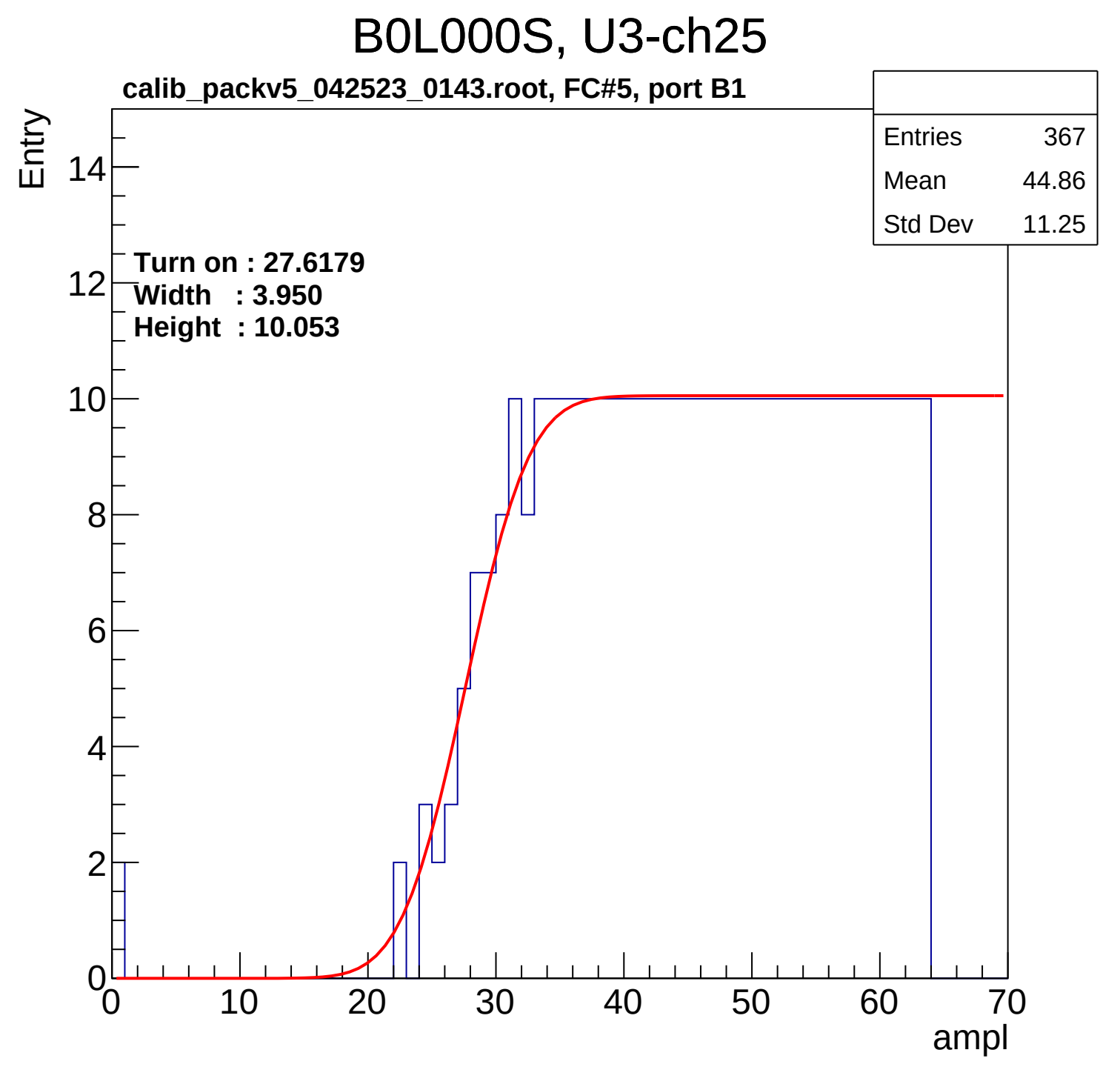
B0L000S, U3-ch25
calib_packv5_042523_0143.root, FC#5, port B1
Entries 367
Mean 44.86
Std Dev 11.25
Turn on : 27.6179
Width : 3.950
Height : 10.053
Entry
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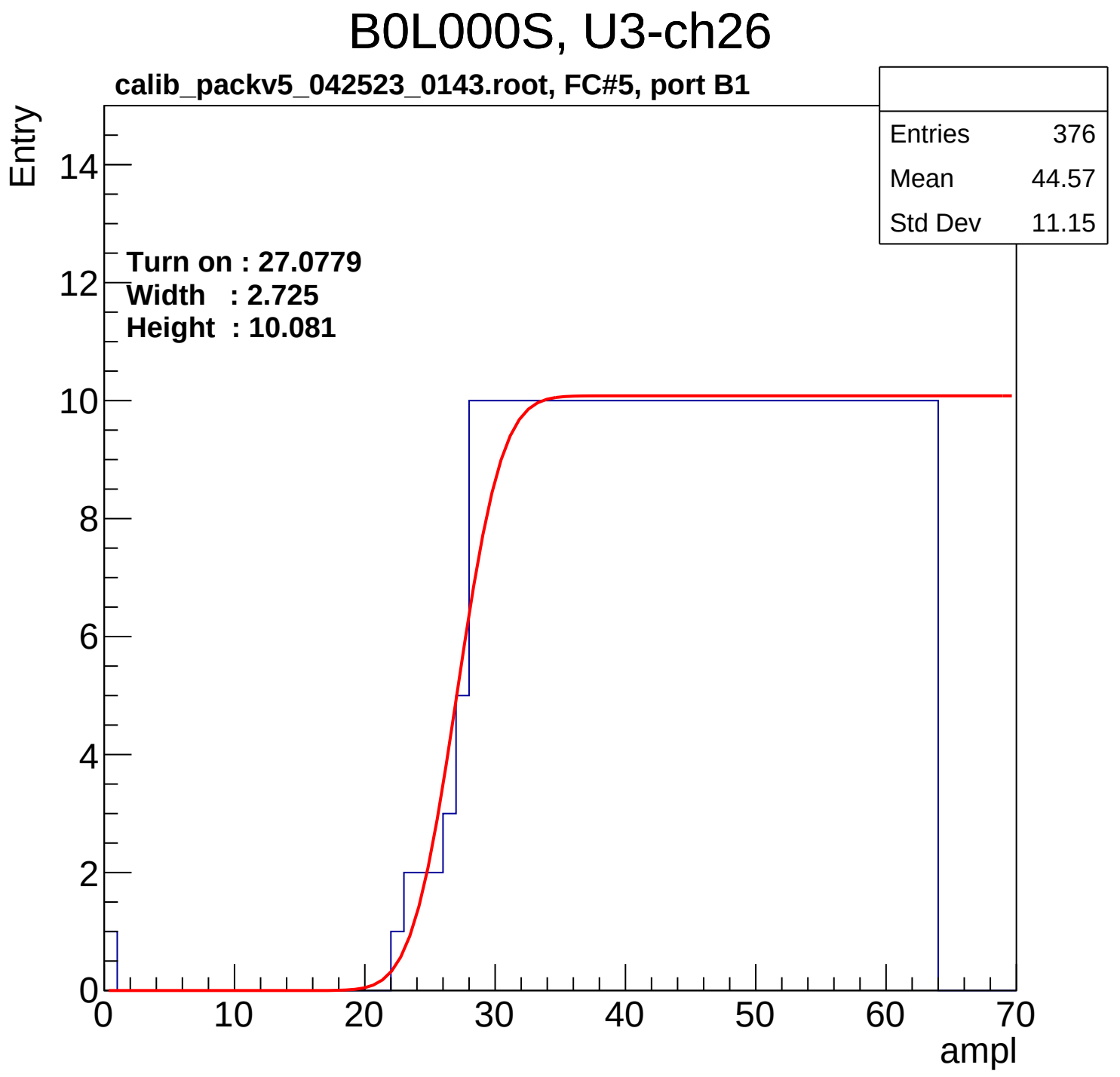
B0L000S, U3-ch26
calib_packv5_042523_0143.root, FC#5, port B1
Entries 376
Mean 44.57
Std Dev 11.15
Turn on : 27.0779
Width : 2.725
Height : 10.081
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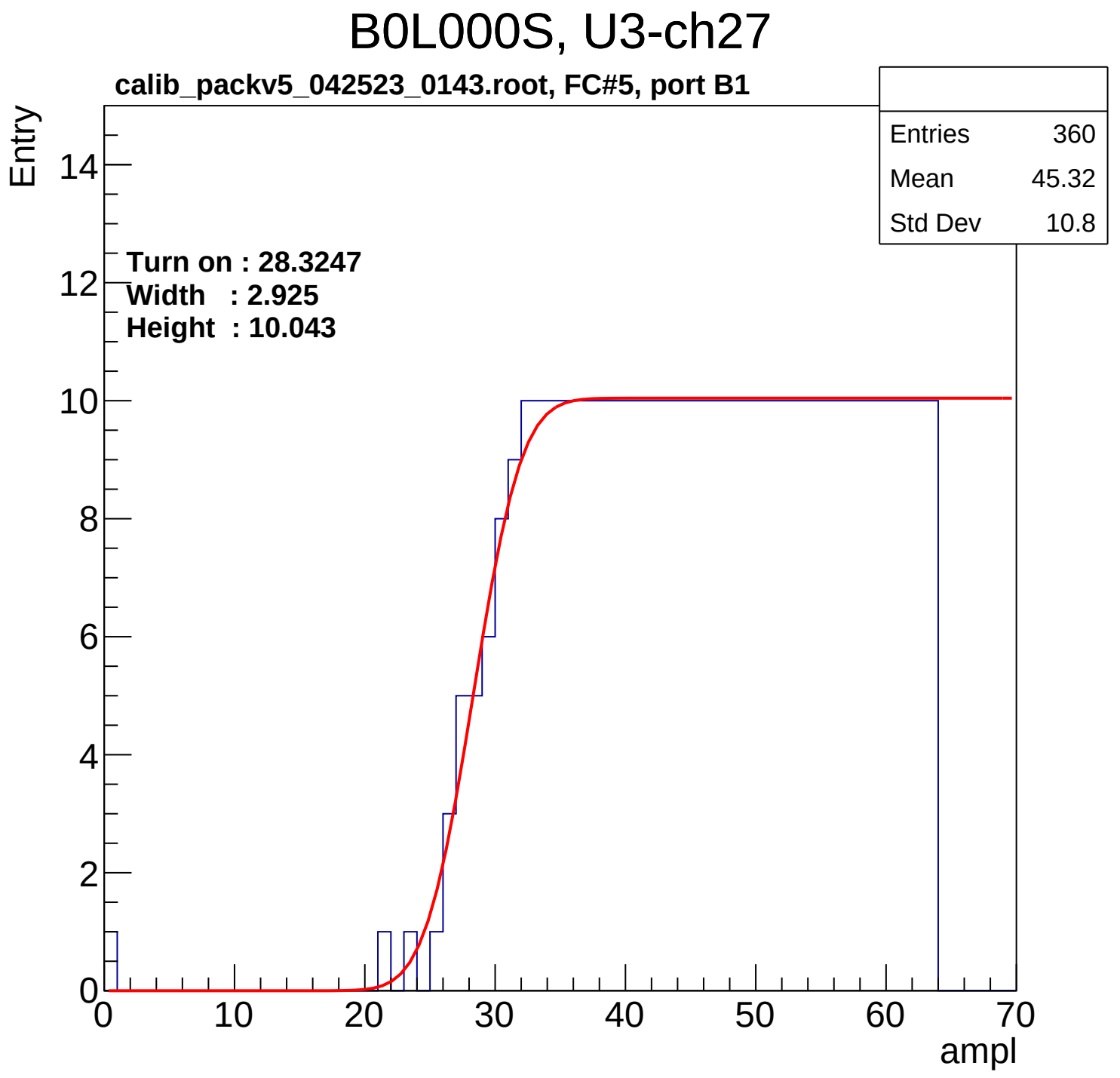
B0L000S, U3-ch27
calib_packv5_042523_0143.root, FC#5, port B1
Entries 360
Mean 45.32
Std Dev 10.8
Turn on : 28.3247
Width : 2.925
Height : 10.043
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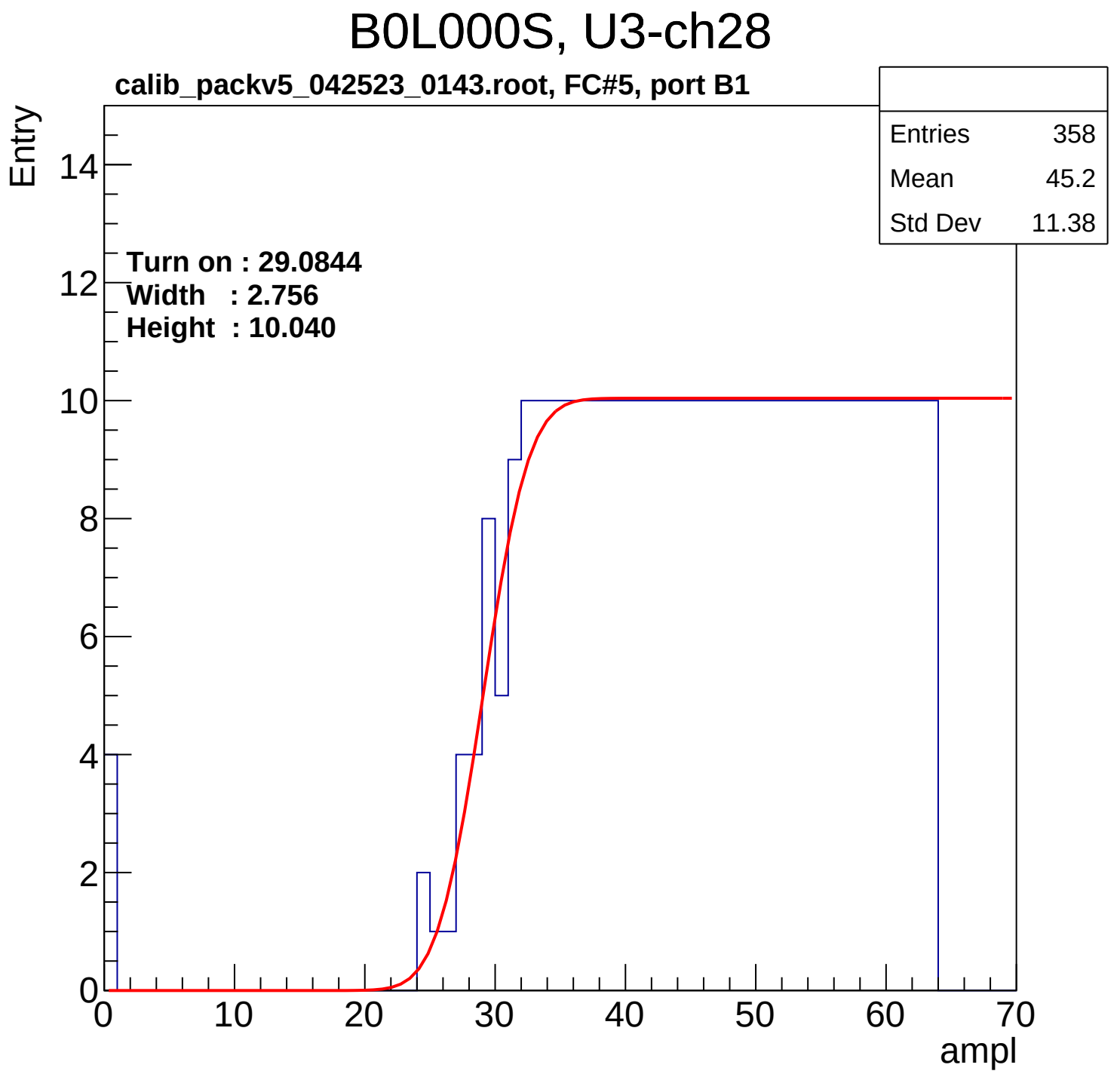
B0L000S, U3-ch28
calib_packv5_042523_0143.root, FC#5, port B1
Entries 358
Mean 45.2
Std Dev 11.38
Turn on : 29.0844
Width : 2.756
Height : 10.040
Entry
ampl
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6
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12
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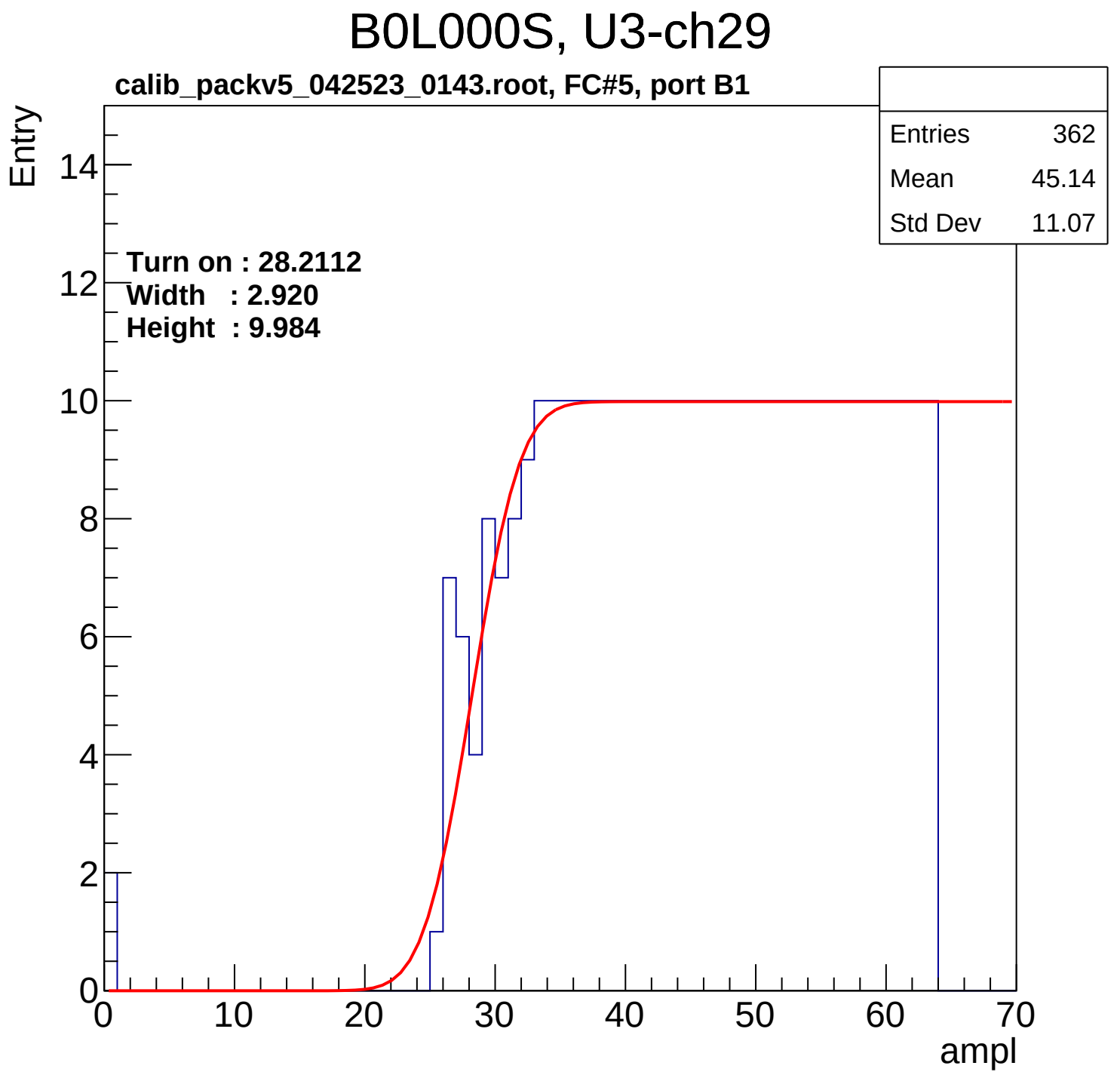
B0L000S, U3-ch29
calib_packv5_042523_0143.root, FC#5, port B1
Entries 362
Mean 45.14
Std Dev 11.07
Turn on : 28.2112
Width : 2.920
Height : 9.984
Entry
ampl
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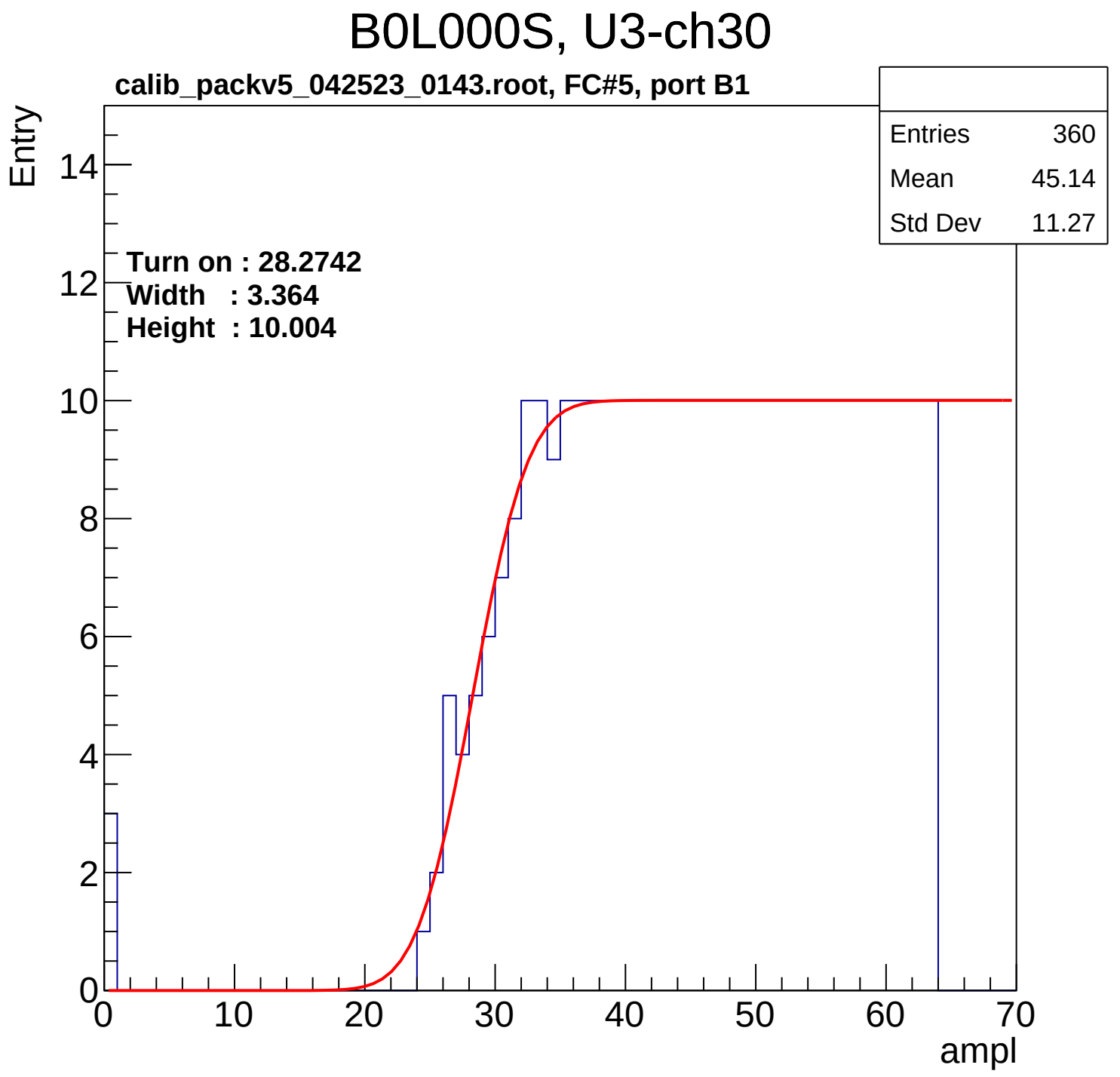
B0L000S, U3-ch30
calib_packv5_042523_0143.root, FC#5, port B1
Entries 360
Mean 45.14
Std Dev 11.27
Turn on : 28.2742
Width : 3.364
Height : 10.004
Entry
ampl
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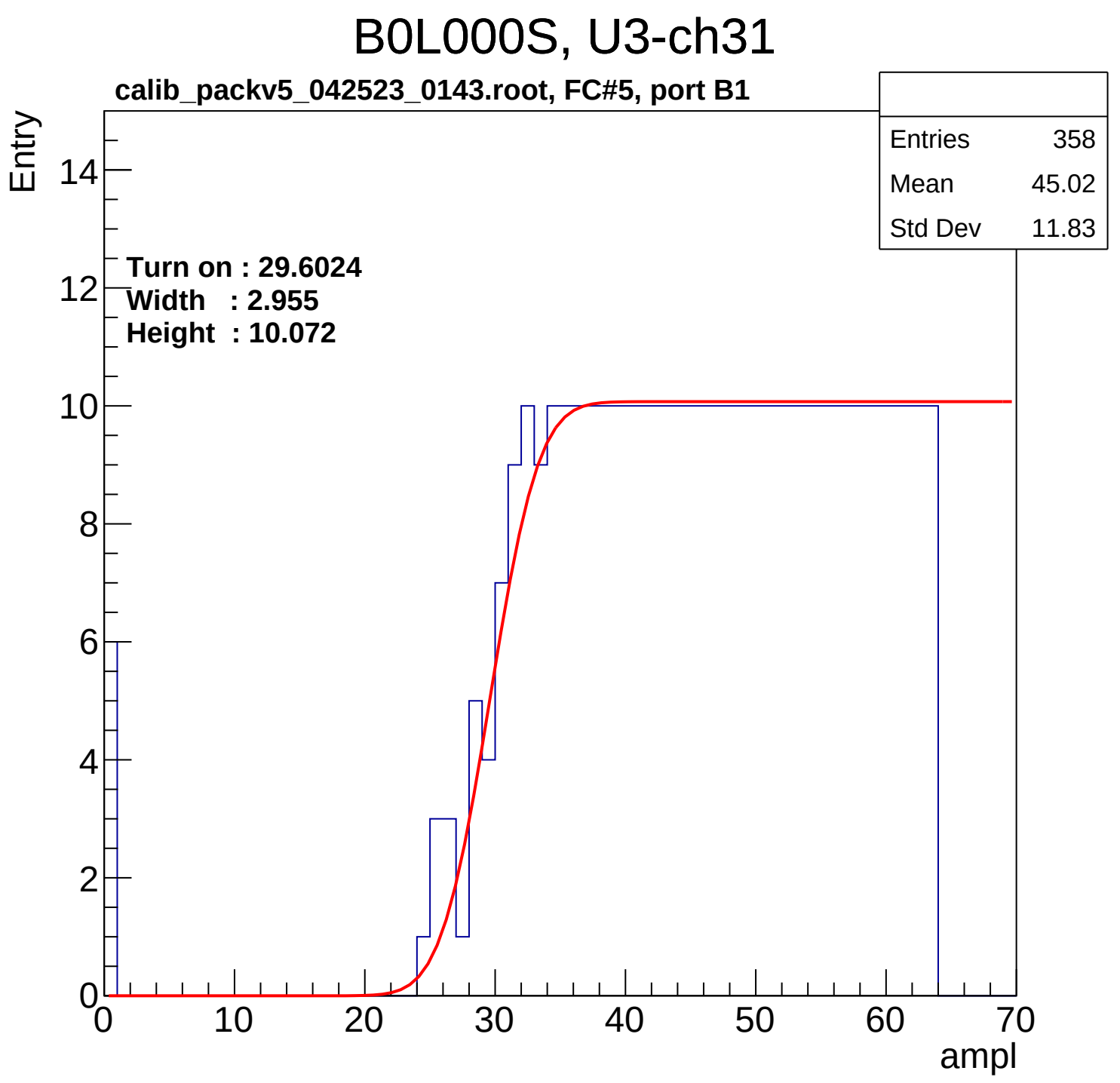
B0L000S, U3-ch31
calib_packv5_042523_0143.root, FC#5, port B1
Entries 358
Mean 45.02
Std Dev 11.83
Turn on : 29.6024
Width : 2.955
Height : 10.072
Entry
ampl
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2
4
6
8
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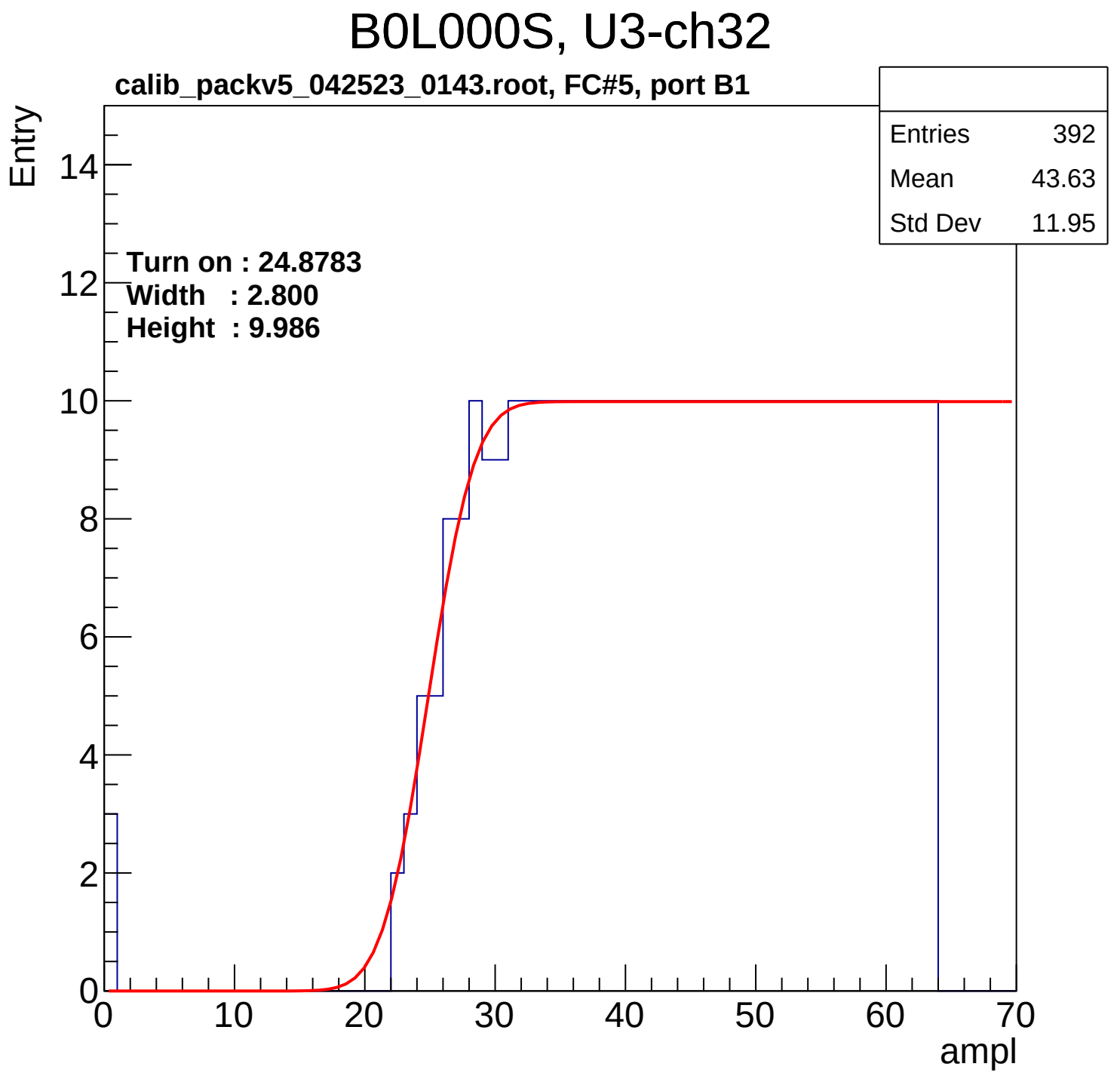
B0L000S, U3-ch32
calib_packv5_042523_0143.root, FC#5, port B1
Entries 392
Mean 43.63
Std Dev 11.95
Turn on : 24.8783
Width : 2.800
Height : 9.986
Entry
ampl
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2
4
6
8
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12
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0
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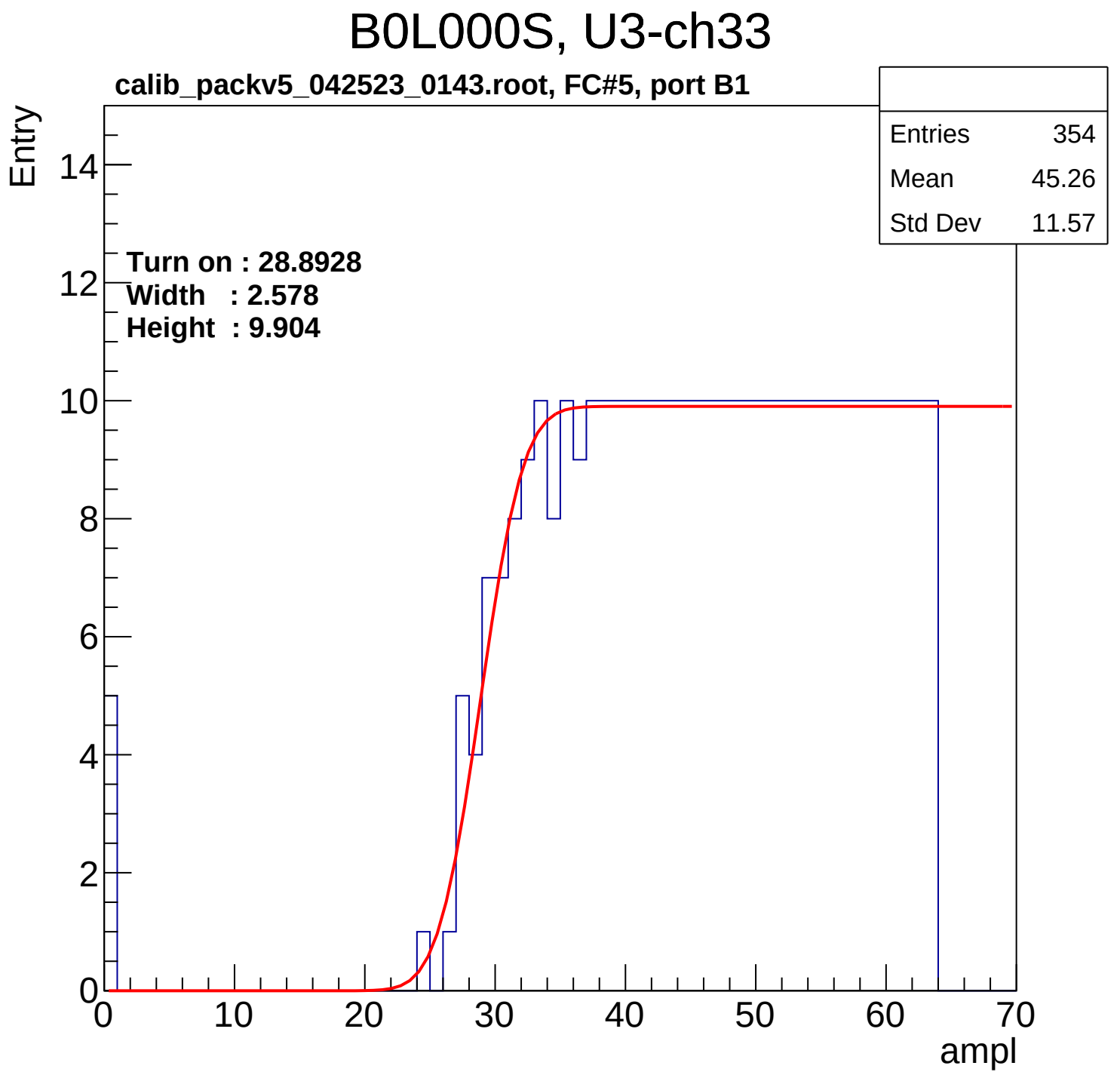
B0L000S, U3-ch33
calib_packv5_042523_0143.root, FC#5, port B1
Entries 354
Mean 45.26
Std Dev 11.57
Turn on : 28.8928
Width : 2.578
Height : 9.904
Entry
ampl
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2
4
6
8
10
12
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0
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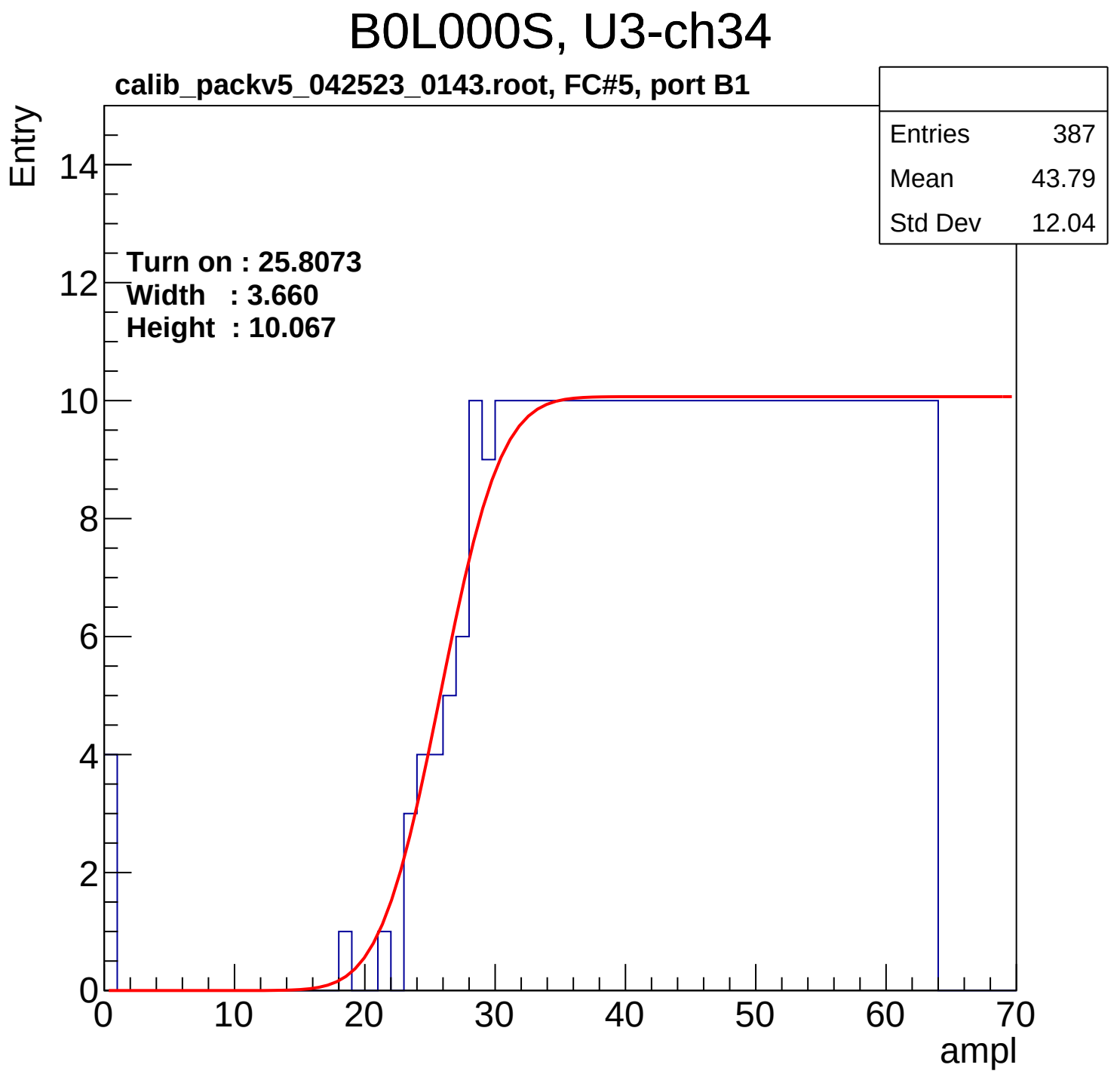
B0L000S, U3-ch34
calib_packv5_042523_0143.root, FC#5, port B1
Entries 387
Mean 43.79
Std Dev 12.04
Turn on : 25.8073
Width : 3.660
Height : 10.067
Entry
ampl
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2
4
6
8
10
12
14
0
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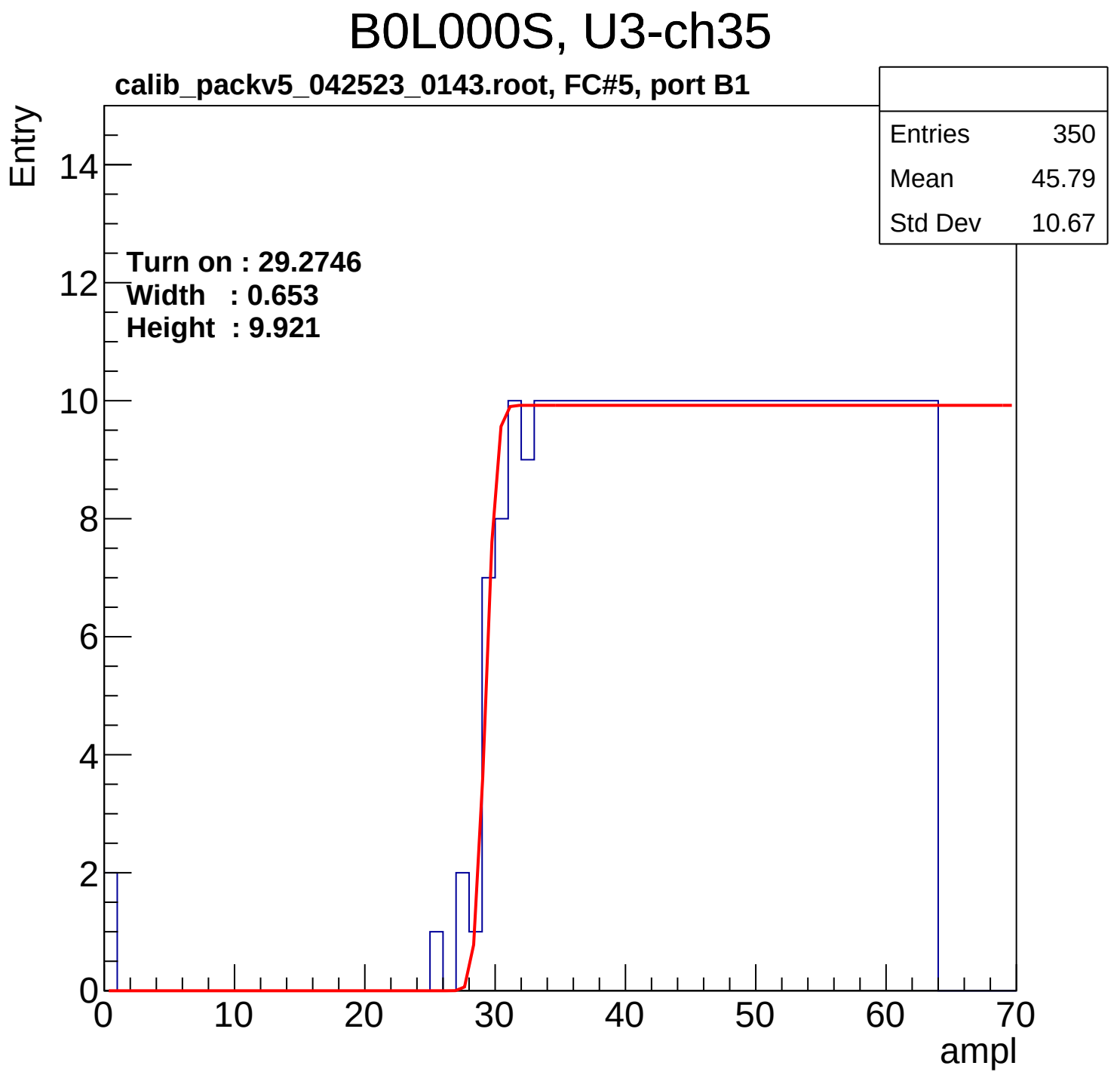
B0L000S, U3-ch35
calib_packv5_042523_0143.root, FC#5, port B1
Entries 350
Mean 45.79
Std Dev 10.67
Turn on : 29.2746
Width : 0.653
Height : 9.921
Entry
ampl
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4
6
8
10
12
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0
10
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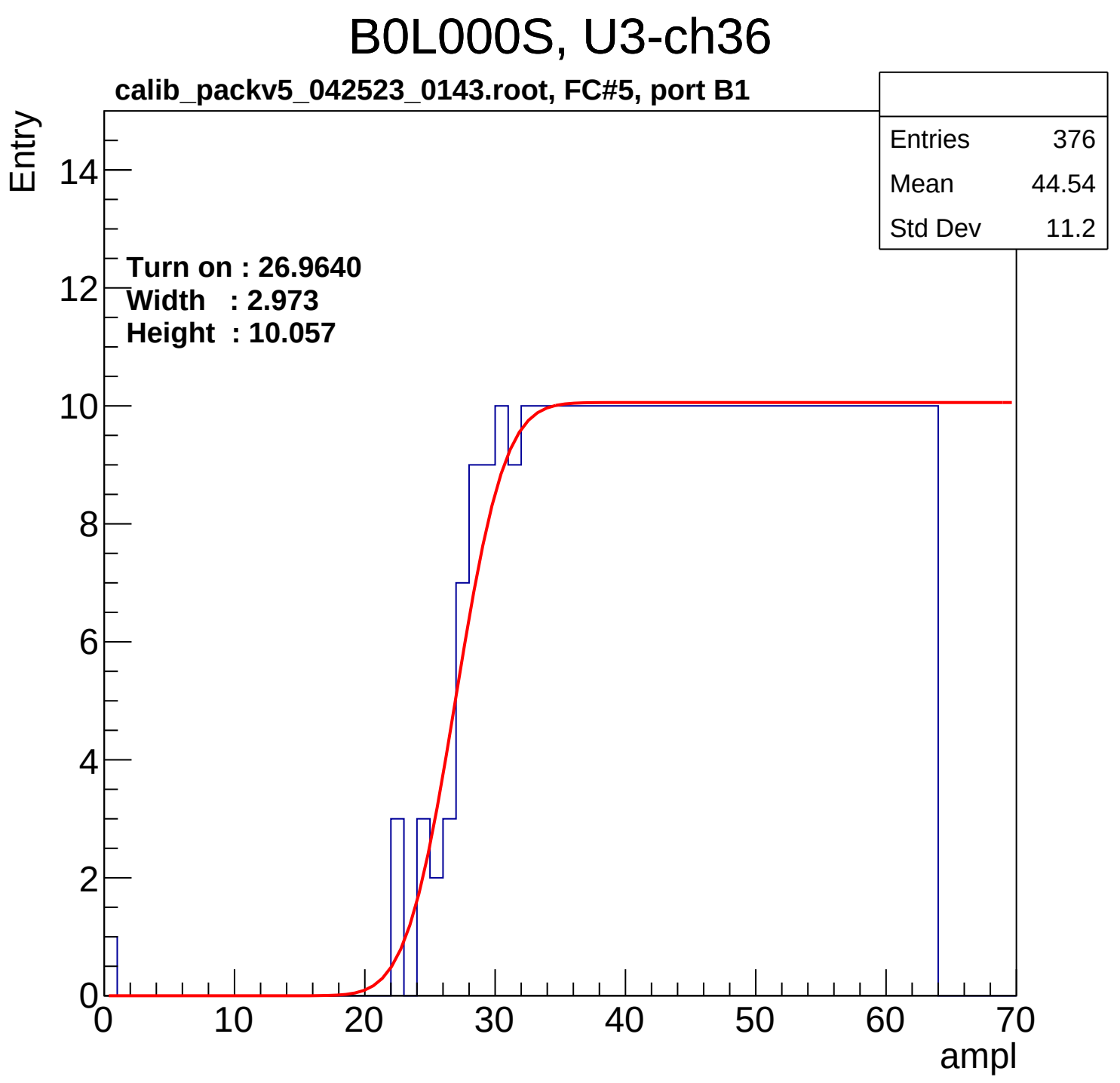
B0L000S, U3-ch36
calib_packv5_042523_0143.root, FC#5, port B1
Entries 376
Mean 44.54
Std Dev 11.2
Turn on : 26.9640
Width : 2.973
Height : 10.057
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
50
60
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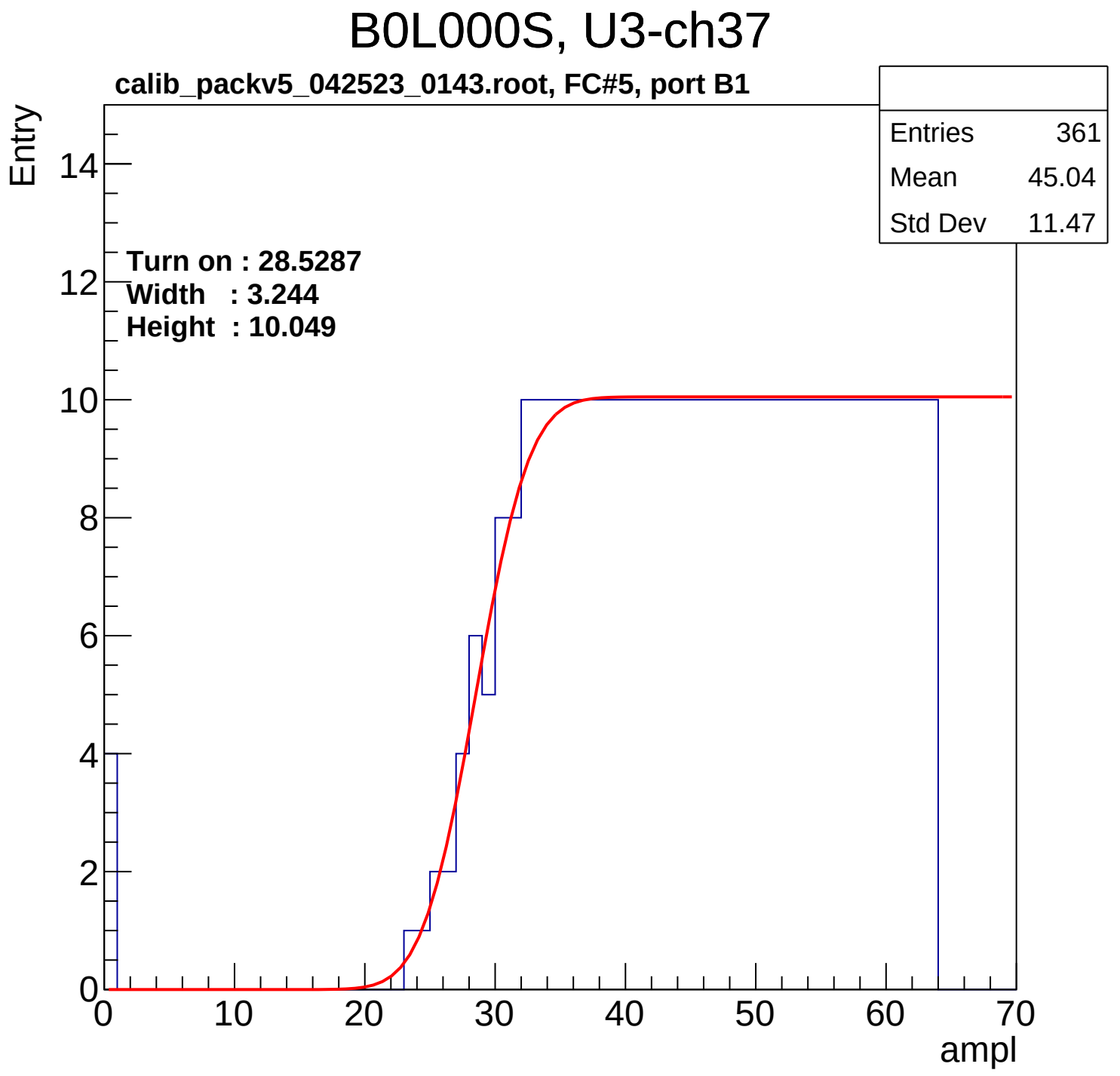
B0L000S, U3-ch37
calib_packv5_042523_0143.root, FC#5, port B1
Entries 361
Mean 45.04
Std Dev 11.47
Turn on : 28.5287
Width : 3.244
Height : 10.049
Entry
ampl
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4
6
8
10
12
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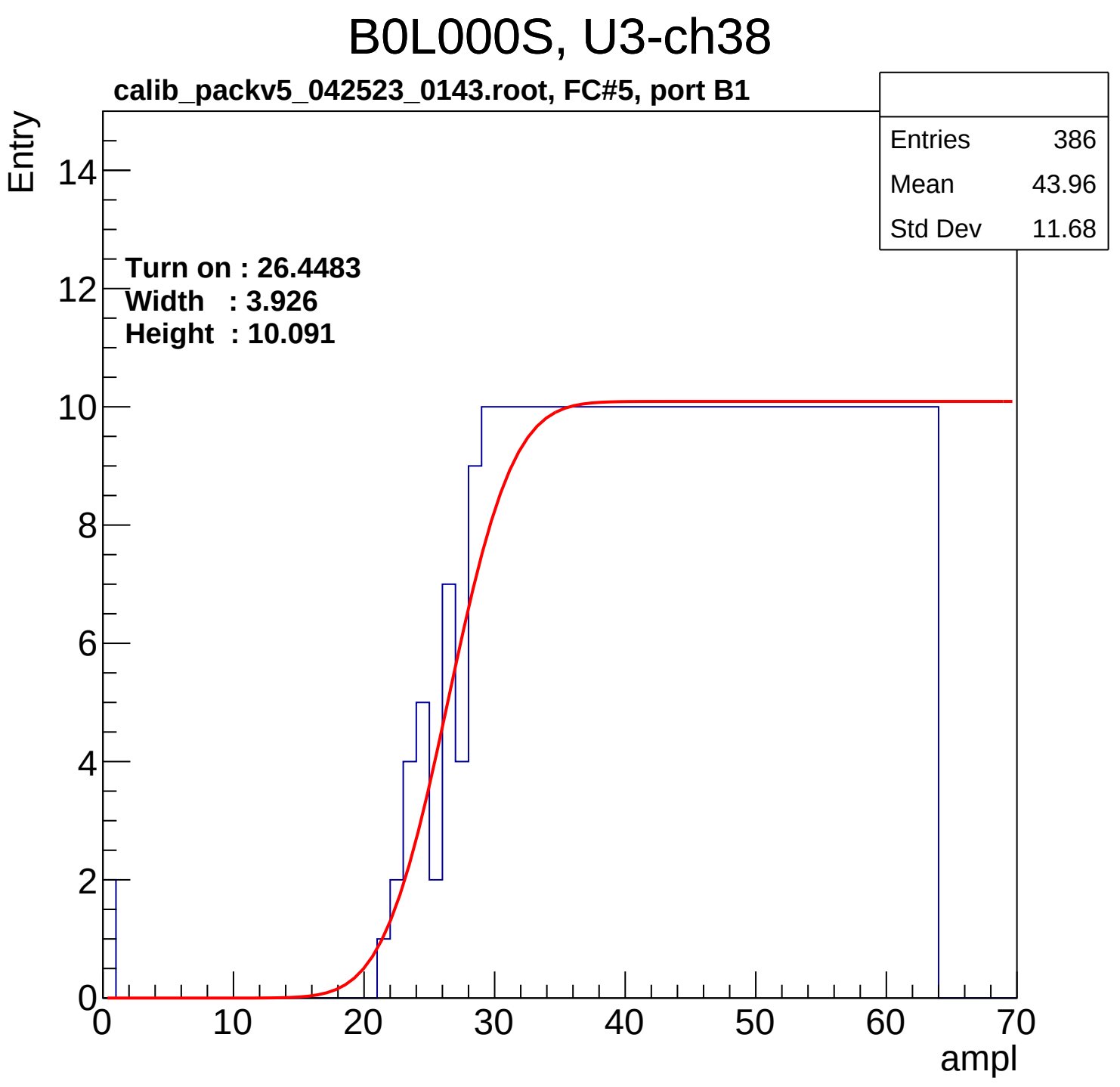
B0L000S, U3-ch38
calib_packv5_042523_0143.root, FC#5, port B1
Entries 386
Mean 43.96
Std Dev 11.68
Turn on : 26.4483
Width : 3.926
Height : 10.091
Entry
ampl
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4
6
8
10
12
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60
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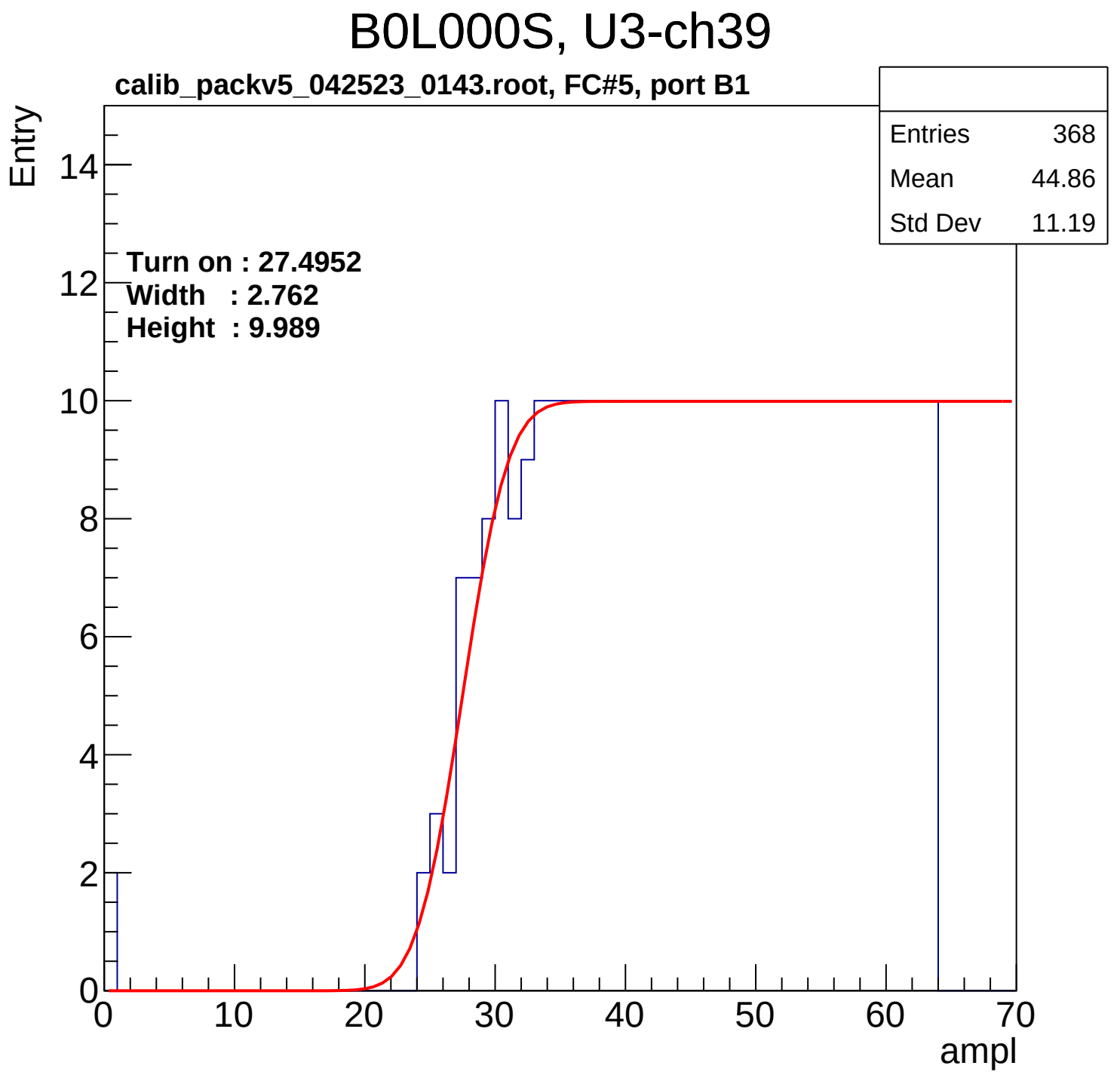
B0L000S, U3-ch39
calib_packv5_042523_0143.root, FC#5, port B1
Entries 368
Mean 44.86
Std Dev 11.19
Turn on : 27.4952
Width : 2.762
Height : 9.989
Entry
ampl
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2
4
6
8
10
12
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0
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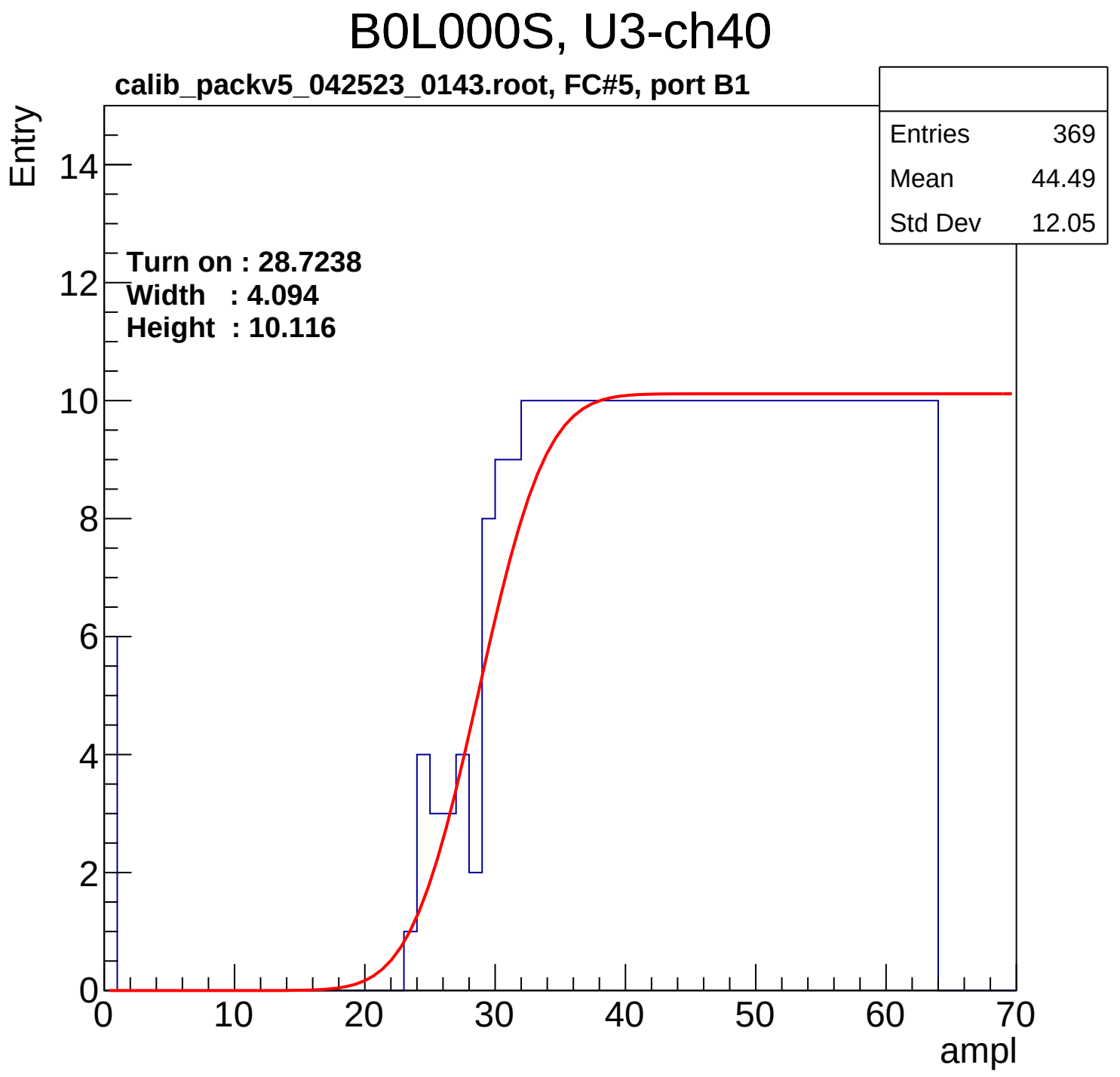
B0L000S, U3-ch40
calib_packv5_042523_0143.root, FC#5, port B1
Entries 369
Mean 44.49
Std Dev 12.05
Turn on : 28.7238
Width : 4.094
Height : 10.116
Entry
ampl
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6
8
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12
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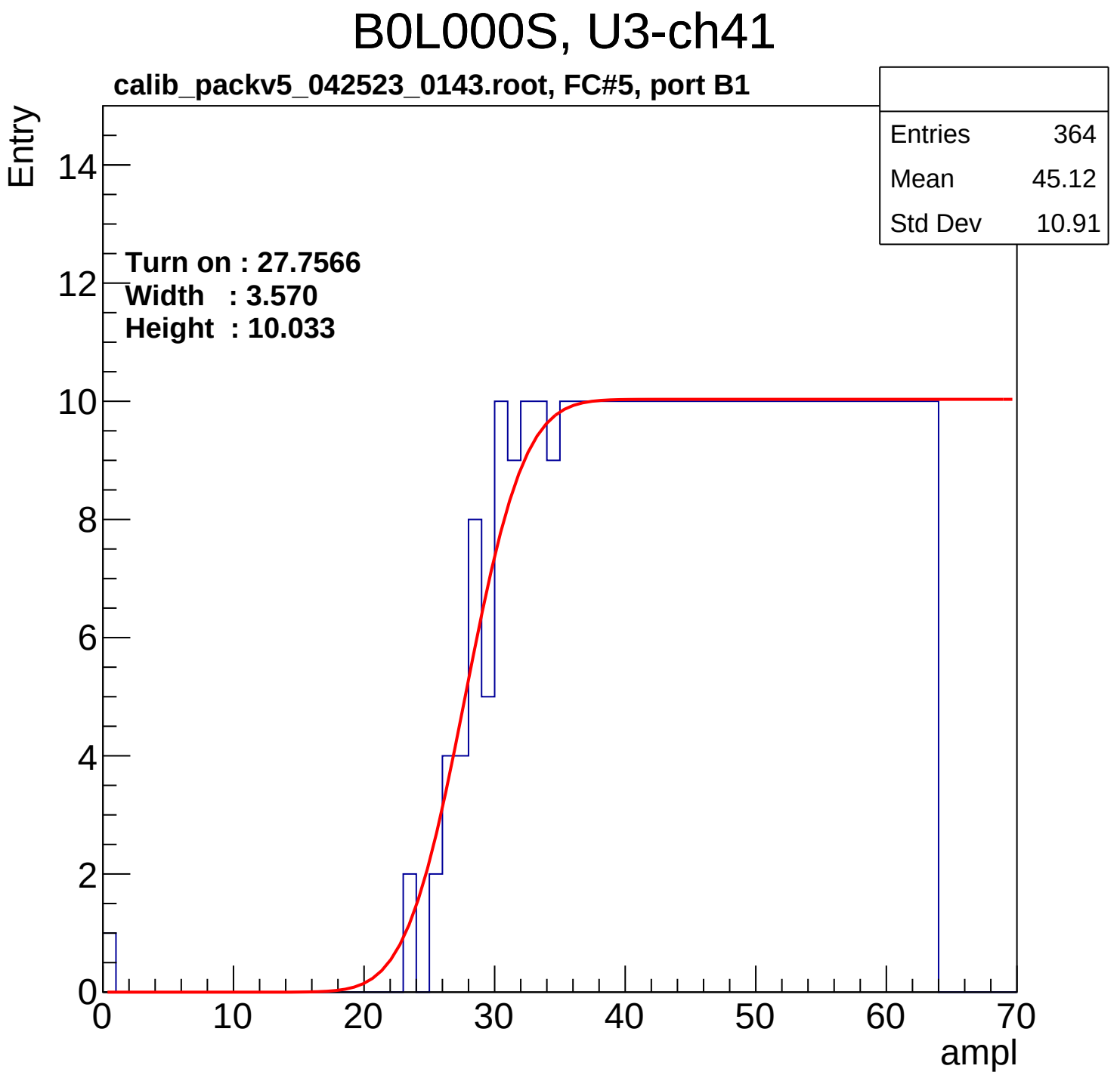
B0L000S, U3-ch41
calib_packv5_042523_0143.root, FC#5, port B1
Entries 364
Mean 45.12
Std Dev 10.91
Turn on : 27.7566
Width : 3.570
Height : 10.033
Entry
ampl
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2
4
6
8
10
12
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0
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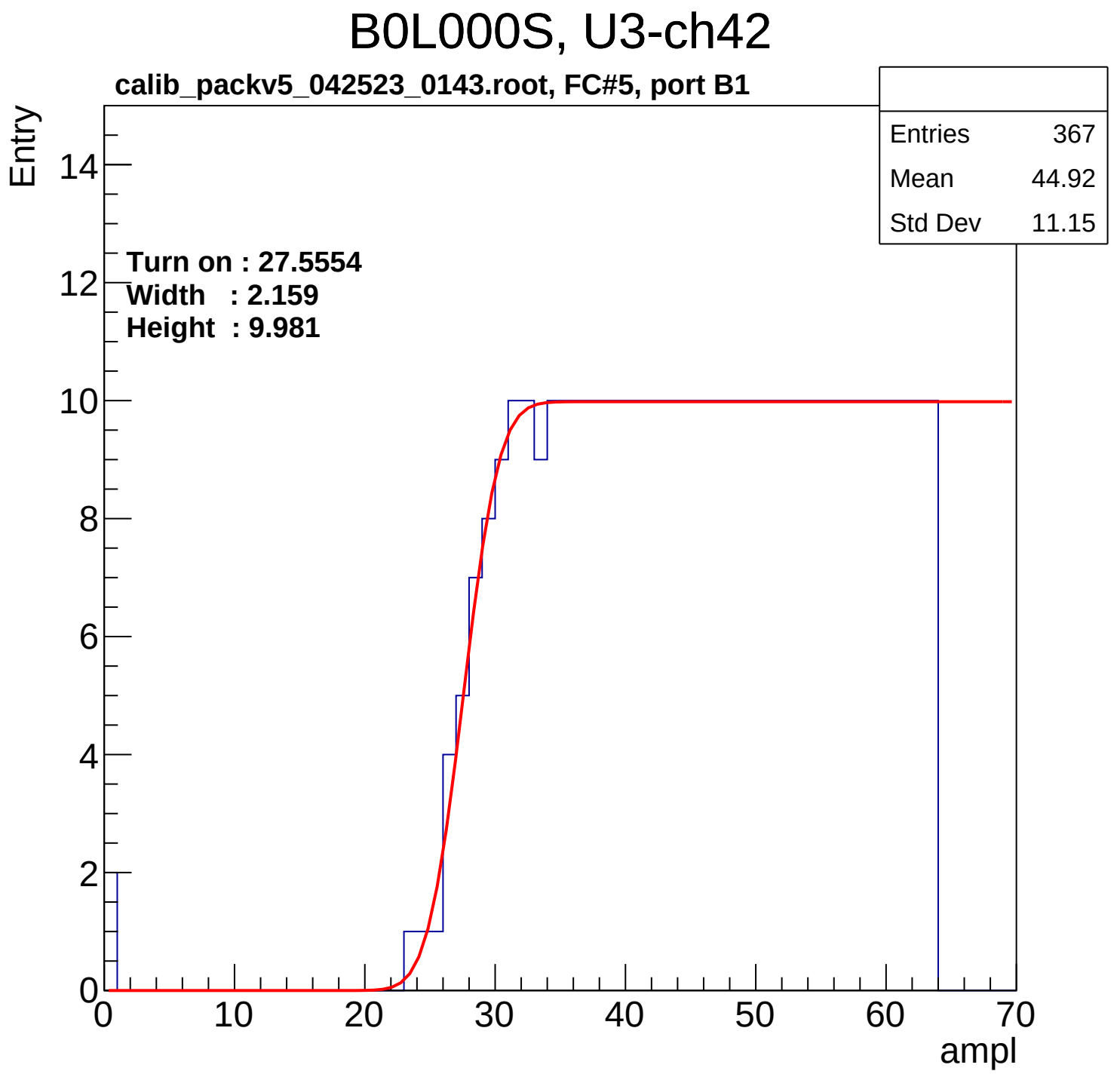
B0L000S, U3-ch42
calib_packv5_042523_0143.root, FC#5, port B1
Entries 367
Mean 44.92
Std Dev 11.15
Turn on : 27.5554
Width : 2.159
Height : 9.981
Entry
ampl
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2
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6
8
10
12
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0
10
20
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60
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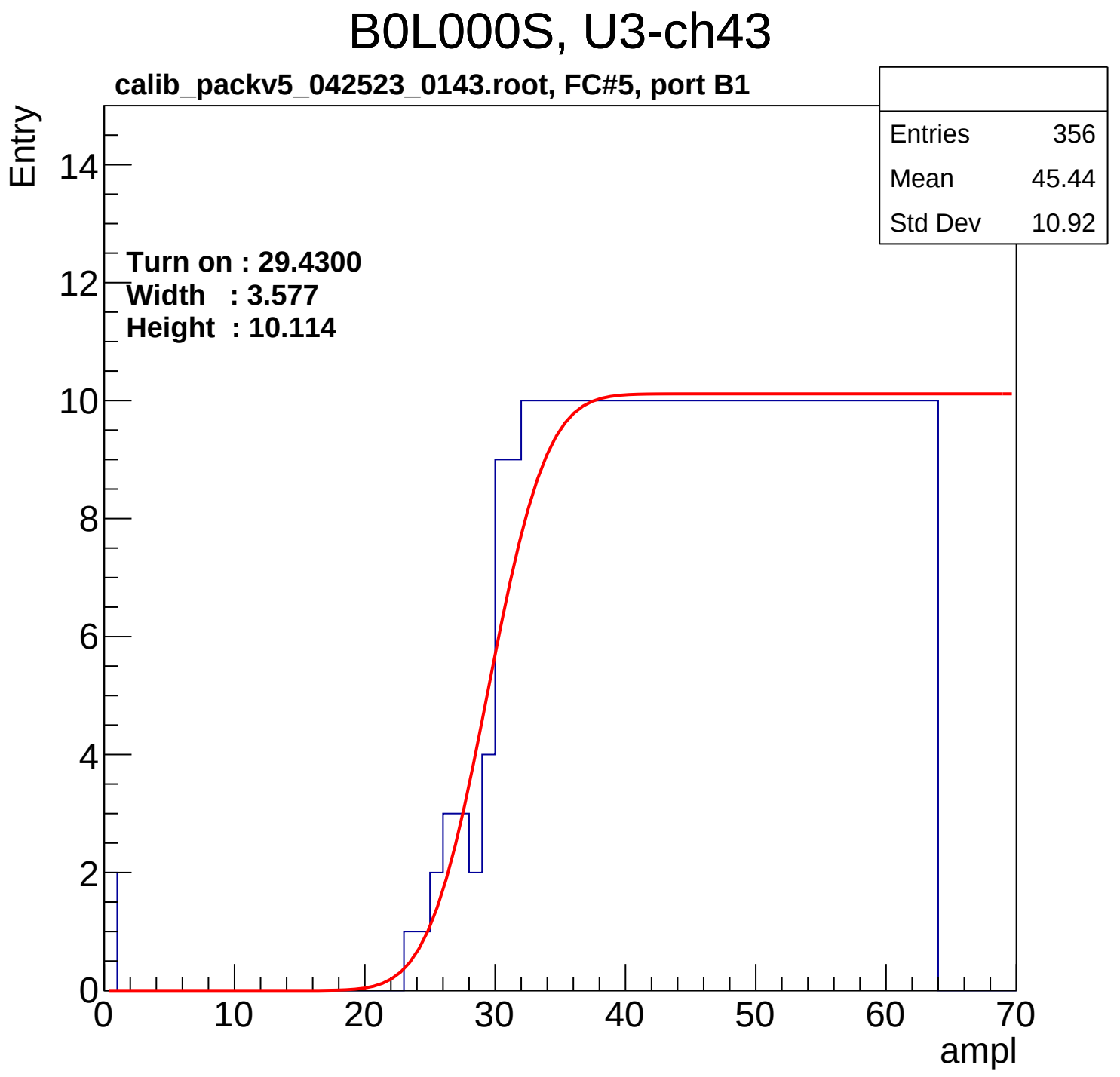
B0L000S, U3-ch43
calib_packv5_042523_0143.root, FC#5, port B1
Entries 356
Mean 45.44
Std Dev 10.92
Turn on : 29.4300
Width : 3.577
Height : 10.114
Entry
ampl
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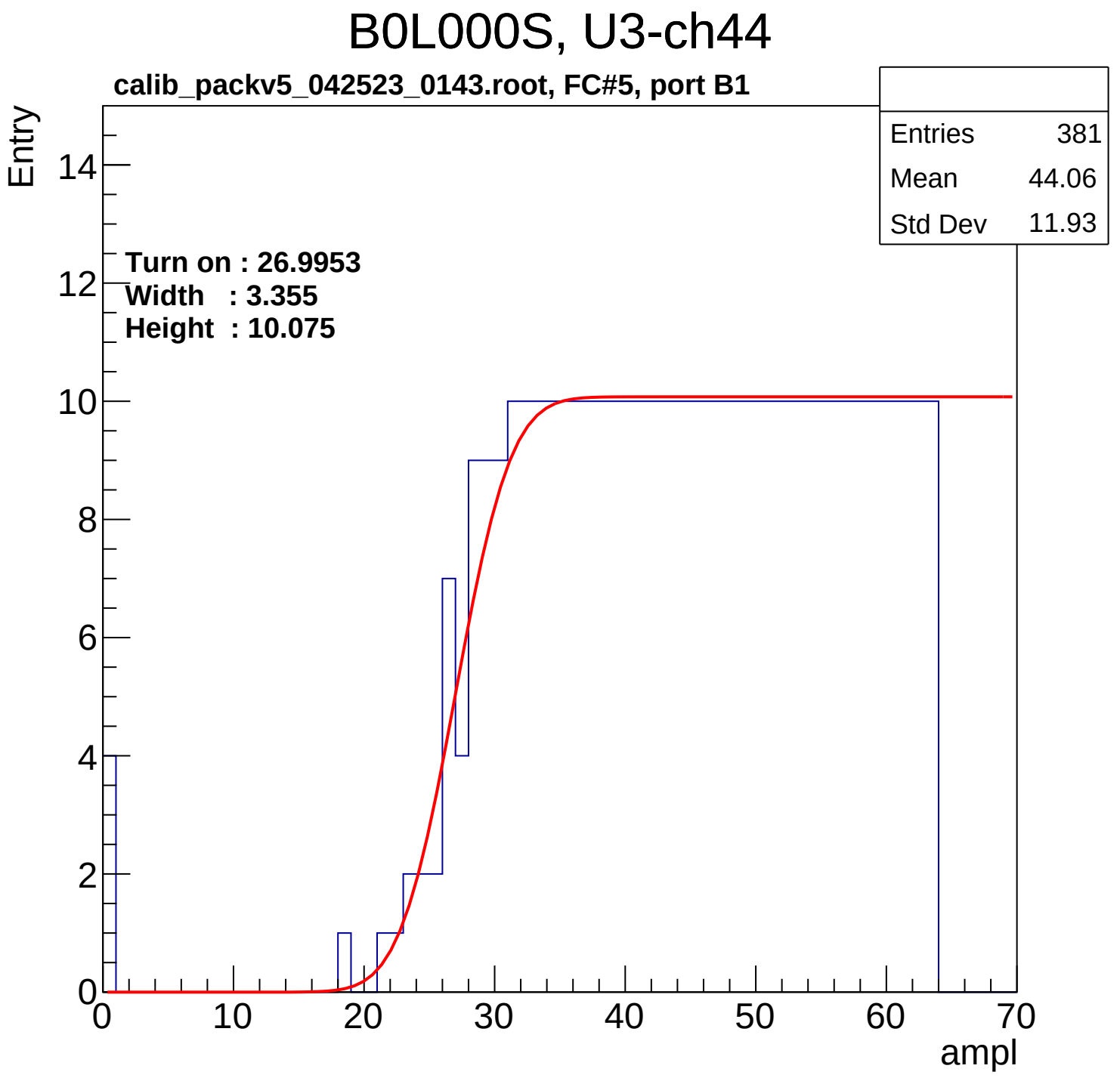
B0L000S, U3-ch44
calib_packv5_042523_0143.root, FC#5, port B1
Entries 381
Mean 44.06
Std Dev 11.93
Turn on : 26.9953
Width : 3.355
Height : 10.075
Entry
ampl
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8
10
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10
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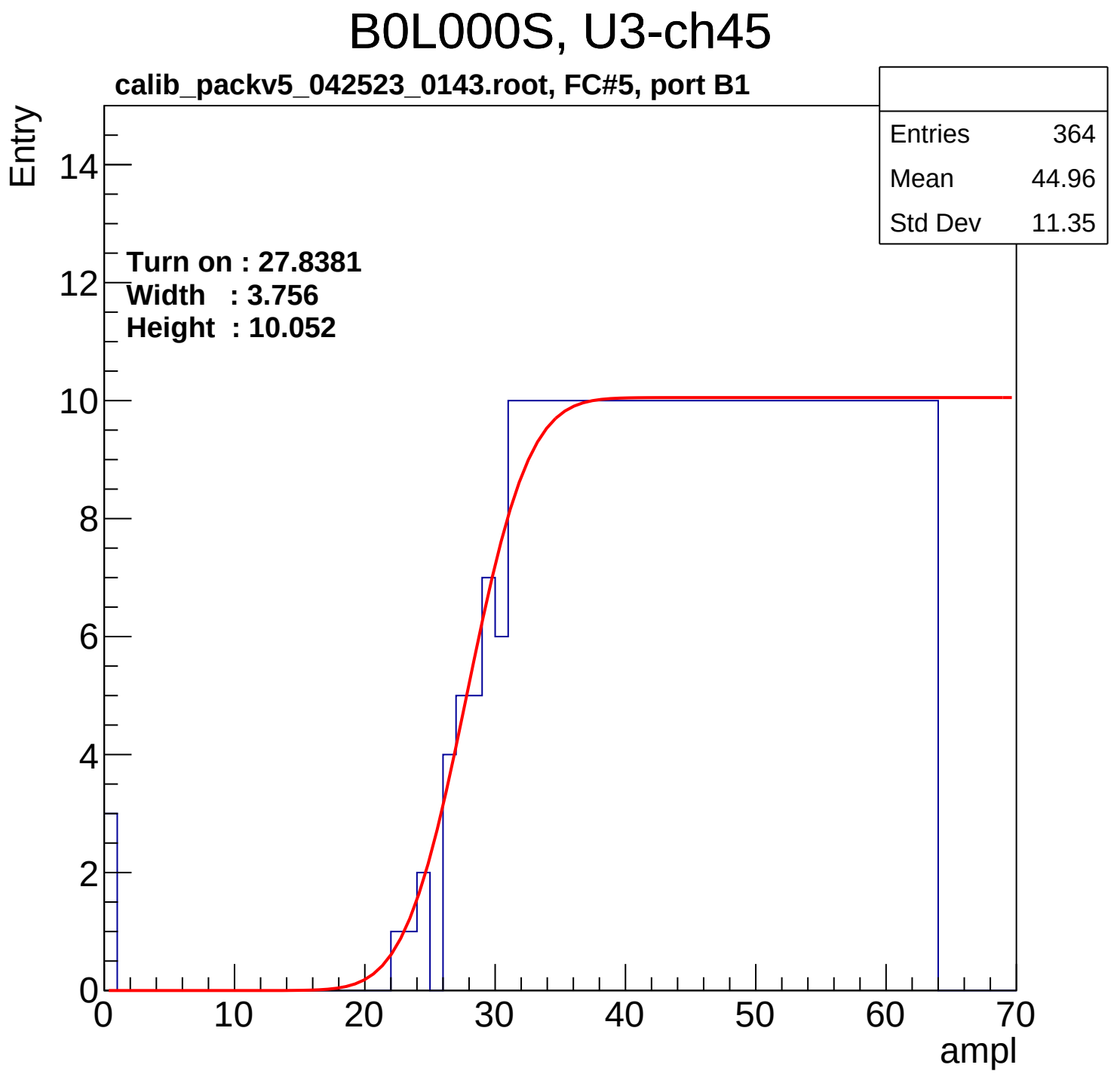
B0L000S, U3-ch45
calib_packv5_042523_0143.root, FC#5, port B1
Entries 364
Mean 44.96
Std Dev 11.35
Turn on : 27.8381
Width : 3.756
Height : 10.052
Entry
ampl
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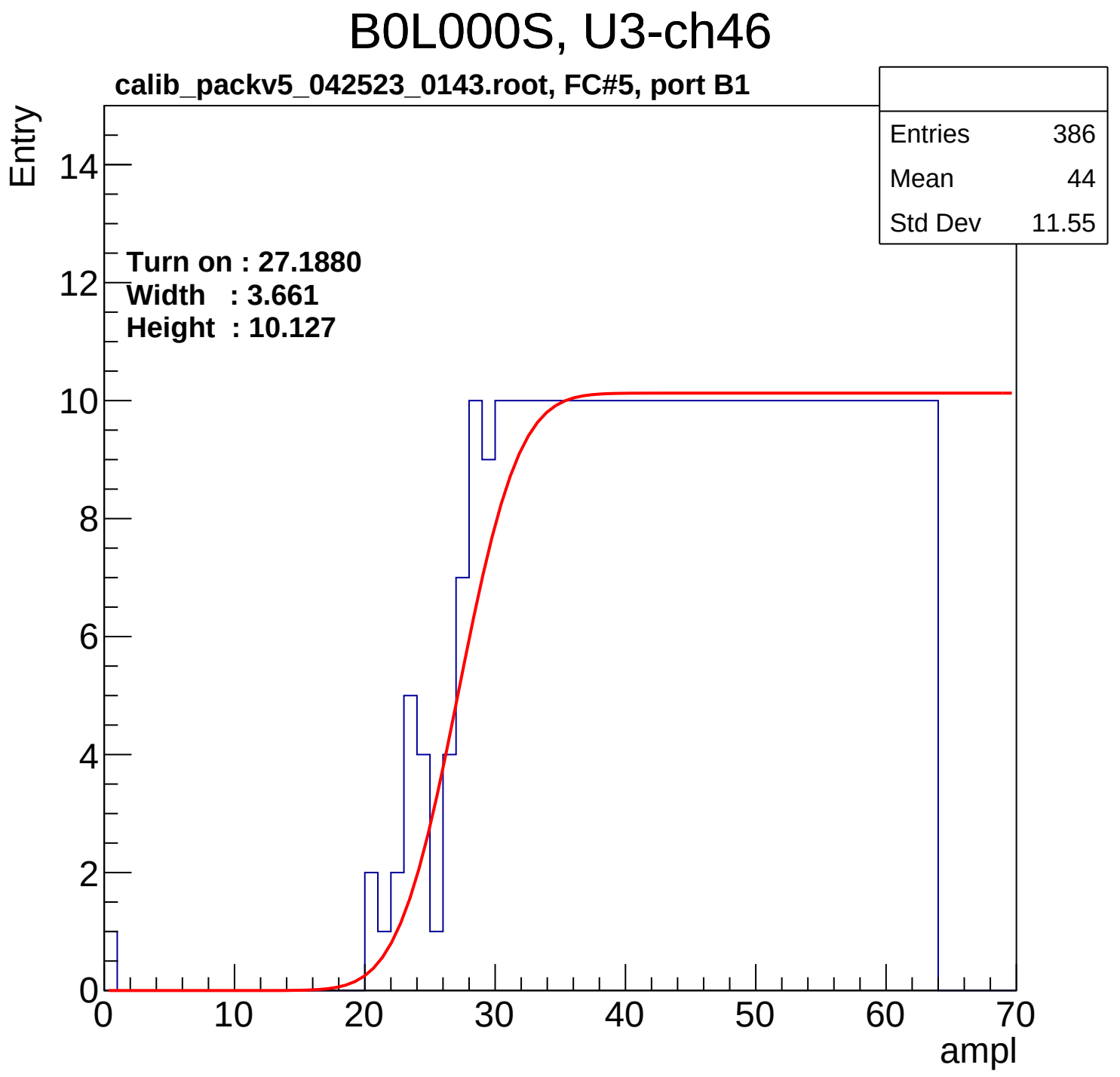
B0L000S, U3-ch46
calib_packv5_042523_0143.root, FC#5, port B1
Entries 386
Mean 44
Std Dev 11.55
Turn on : 27.1880
Width : 3.661
Height : 10.127
Entry
ampl
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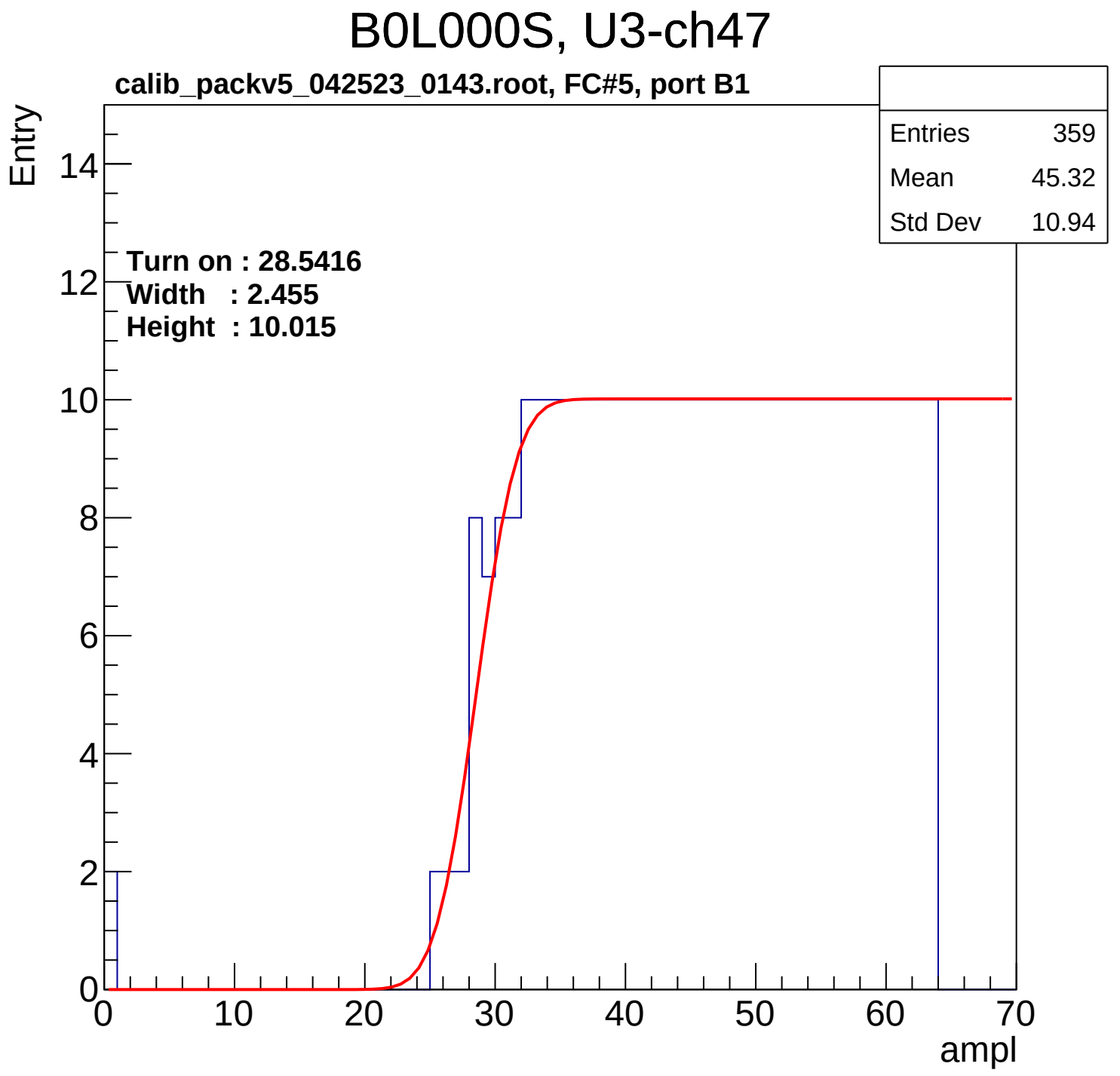
B0L000S, U3-ch47
calib_packv5_042523_0143.root, FC#5, port B1
Entries 359
Mean 45.32
Std Dev 10.94
Turn on : 28.5416
Width : 2.455
Height : 10.015
Entry
ampl
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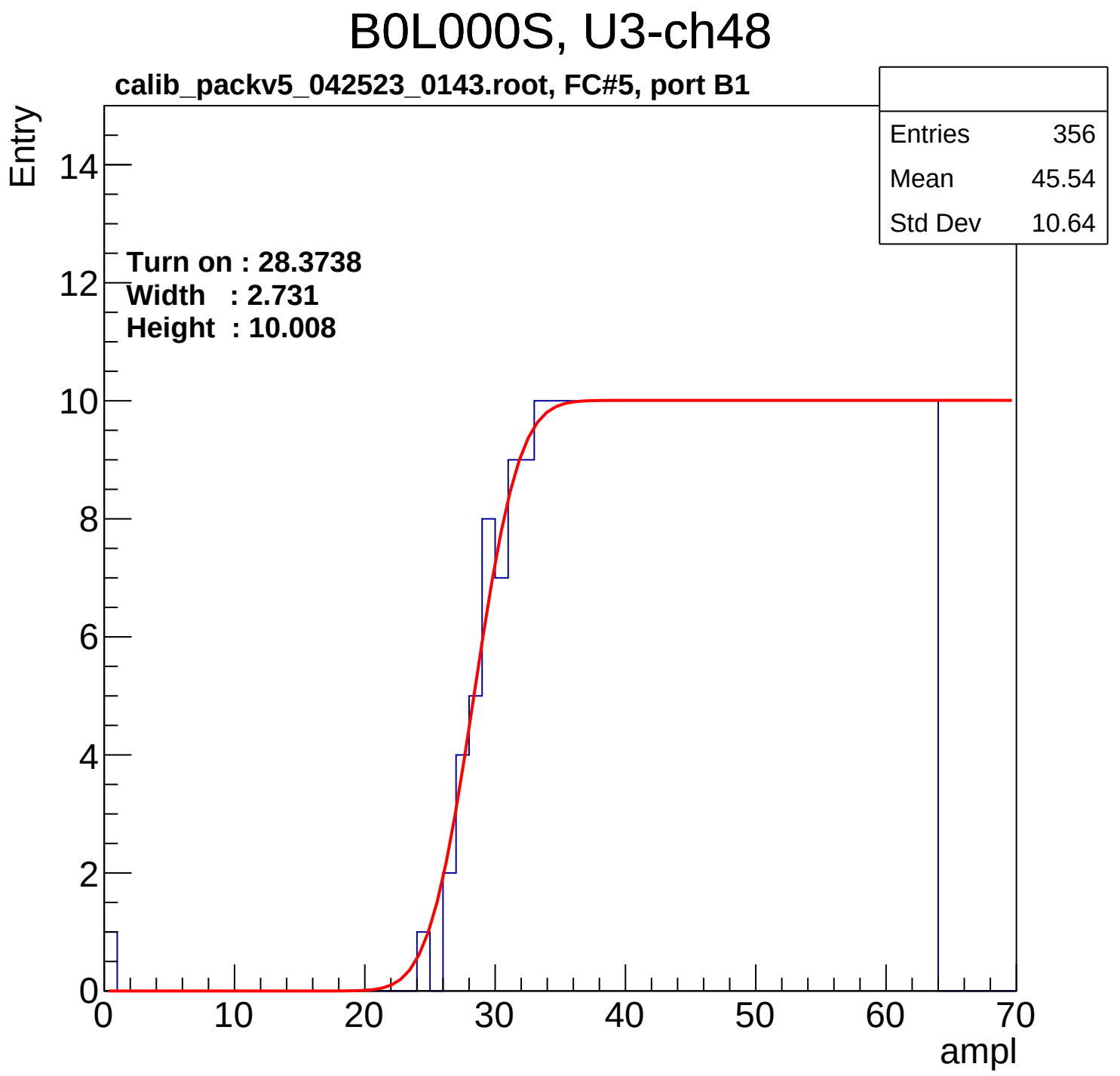
B0L000S, U3-ch48
calib_packv5_042523_0143.root, FC#5, port B1
Entries 356
Mean 45.54
Std Dev 10.64
Turn on : 28.3738
Width : 2.731
Height : 10.008
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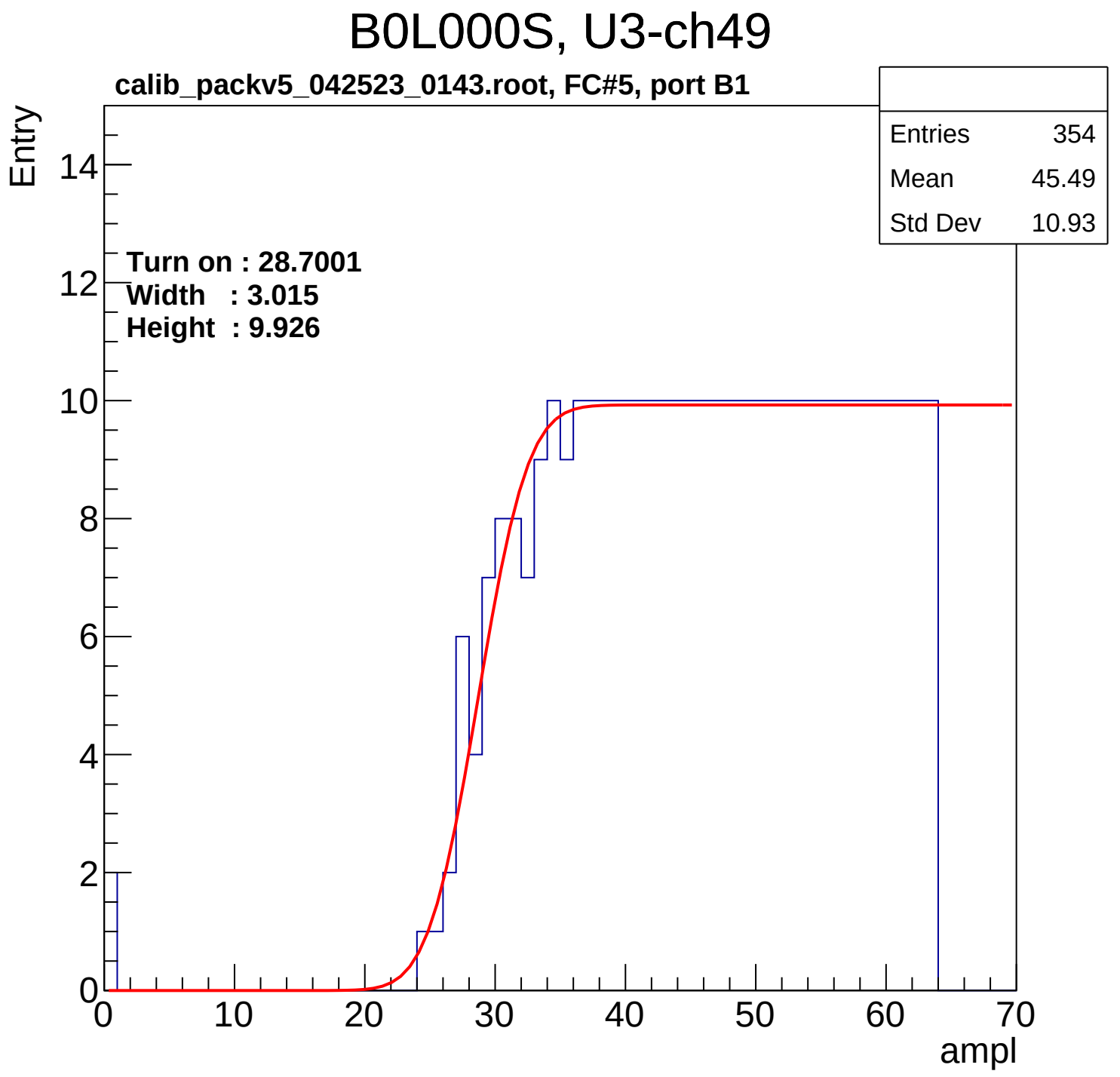
B0L000S, U3-ch49
calib_packv5_042523_0143.root, FC#5, port B1
Entries 354
Mean 45.49
Std Dev 10.93
Turn on : 28.7001
Width : 3.015
Height : 9.926
Entry
ampl
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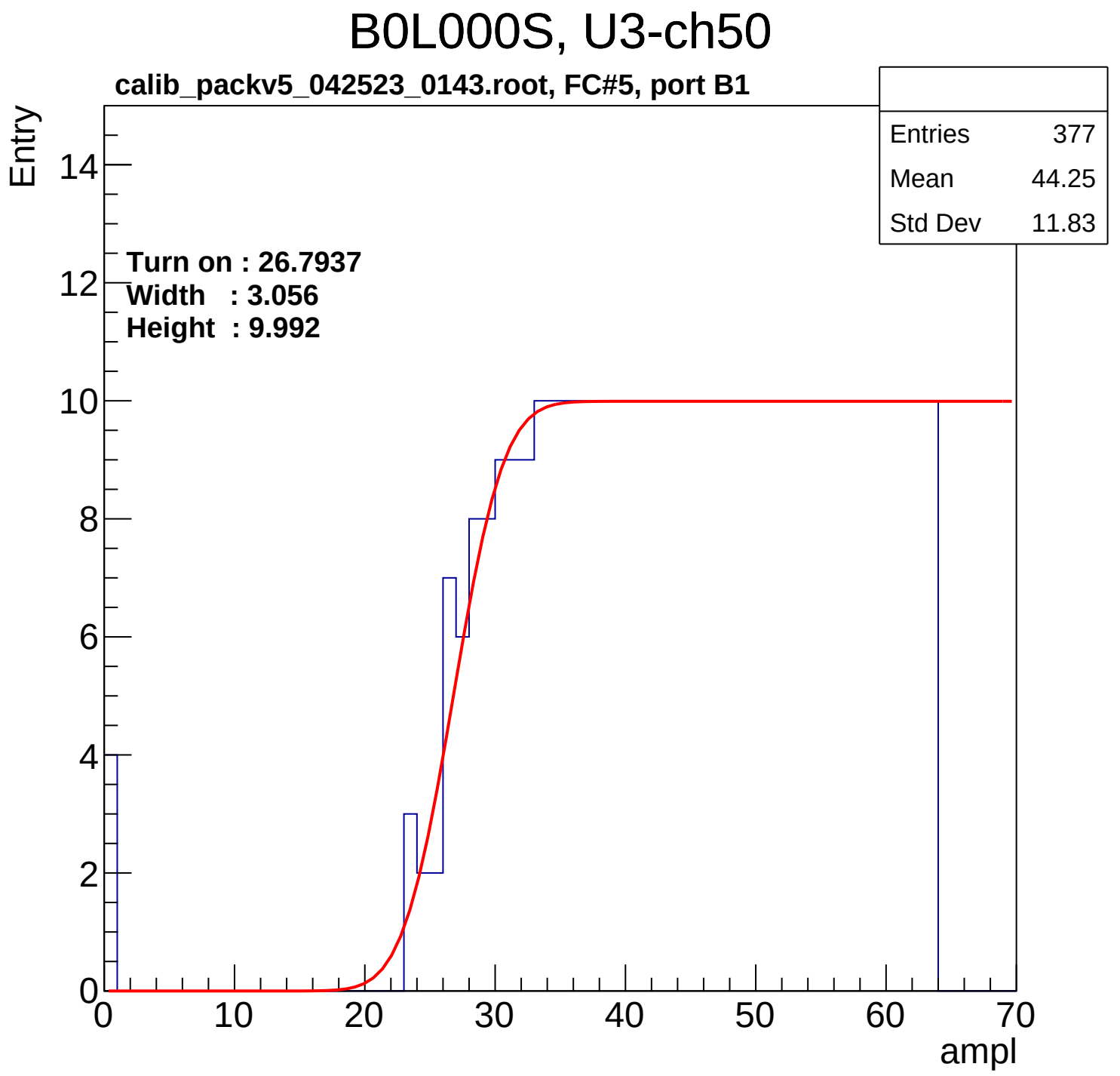
B0L000S, U3-ch50
calib_packv5_042523_0143.root, FC#5, port B1
Entries 377
Mean 44.25
Std Dev 11.83
Turn on : 26.7937
Width : 3.056
Height : 9.992
Entry
ampl
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8
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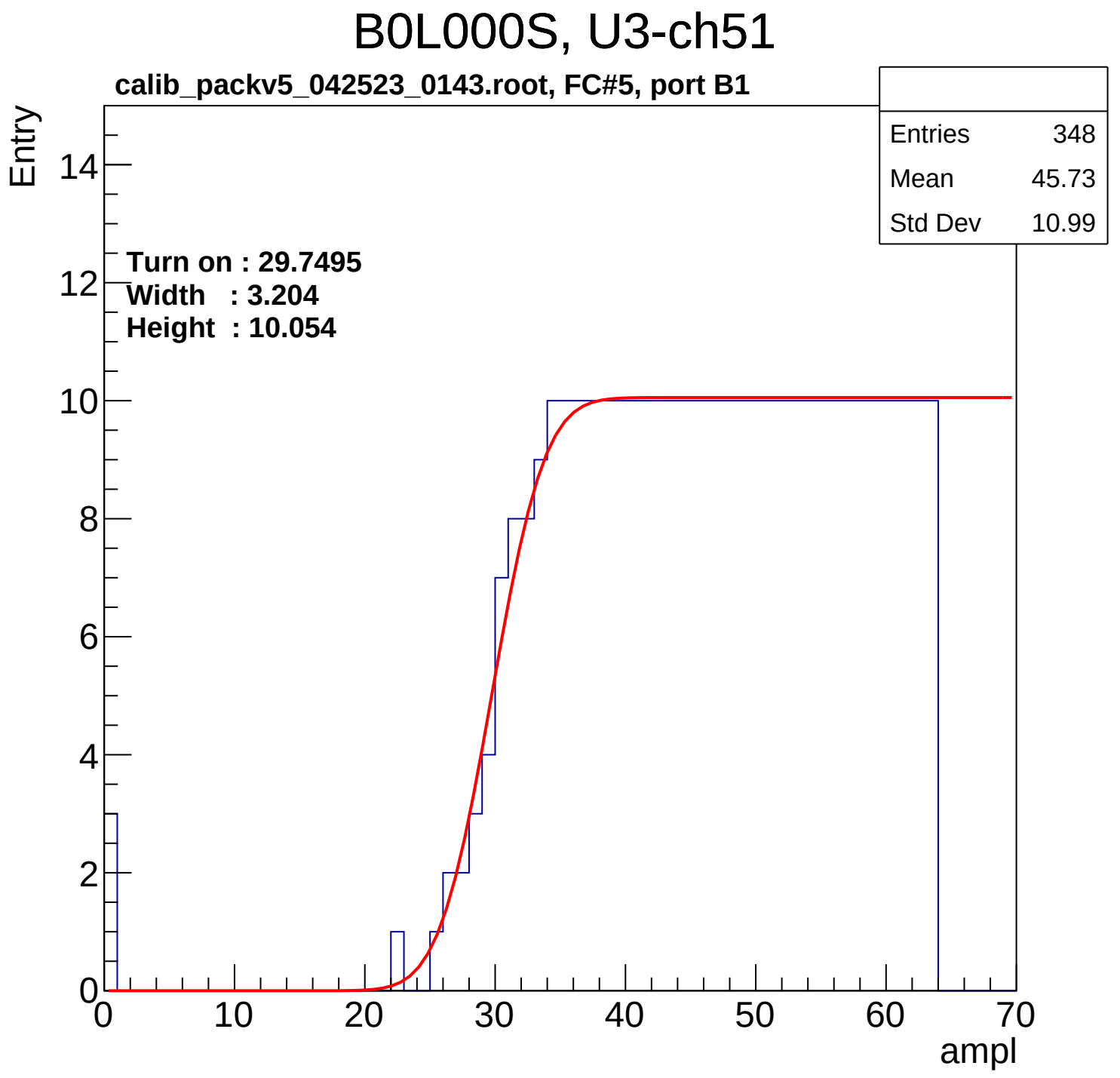
B0L000S, U3-ch51
calib_packv5_042523_0143.root, FC#5, port B1
Entries 348
Mean 45.73
Std Dev 10.99
Turn on : 29.7495
Width : 3.204
Height : 10.054
Entry
ampl
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8
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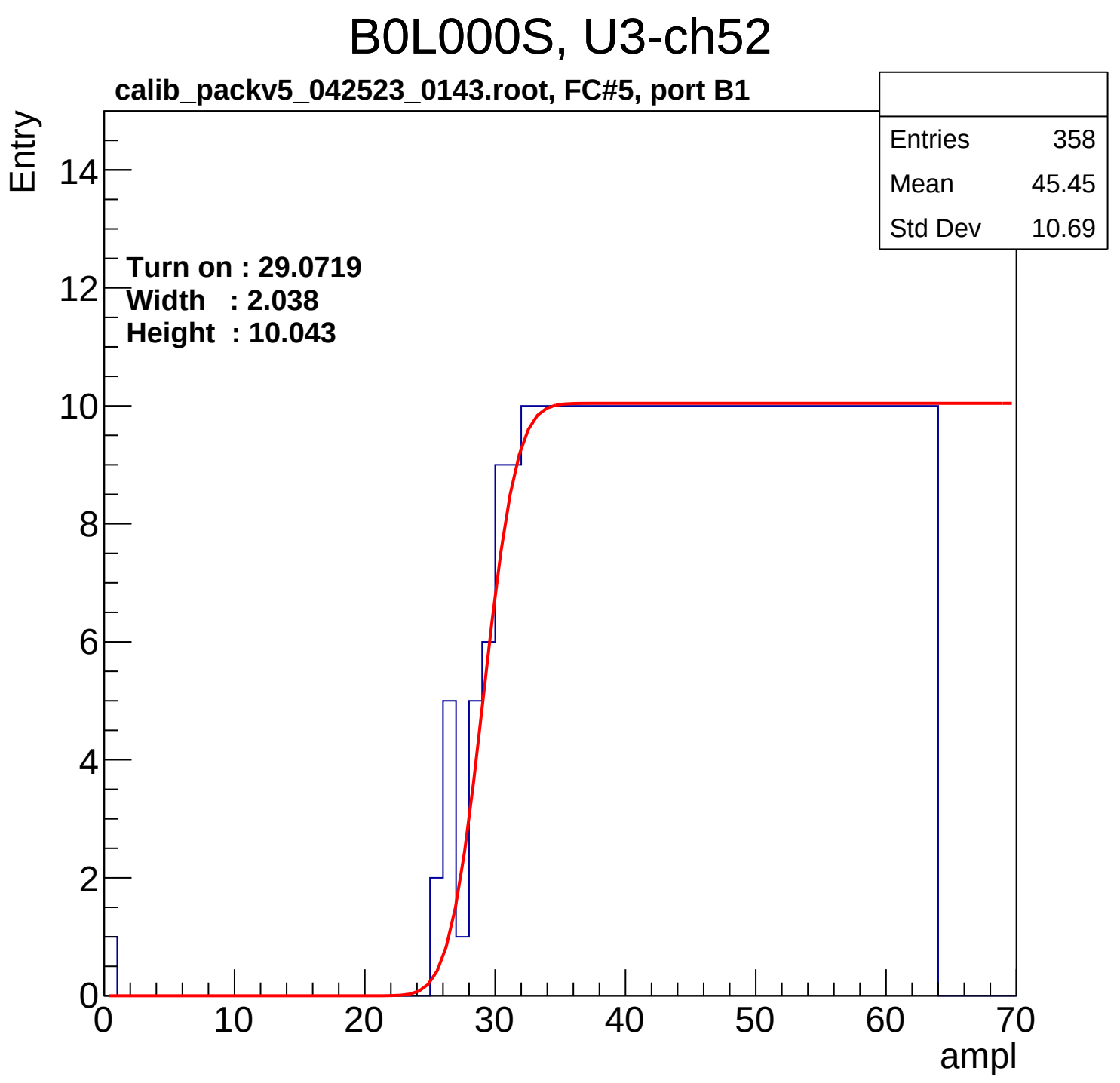
B0L000S, U3-ch52
calib_packv5_042523_0143.root, FC#5, port B1
Entries 358
Mean 45.45
Std Dev 10.69
Turn on : 29.0719
Width : 2.038
Height : 10.043
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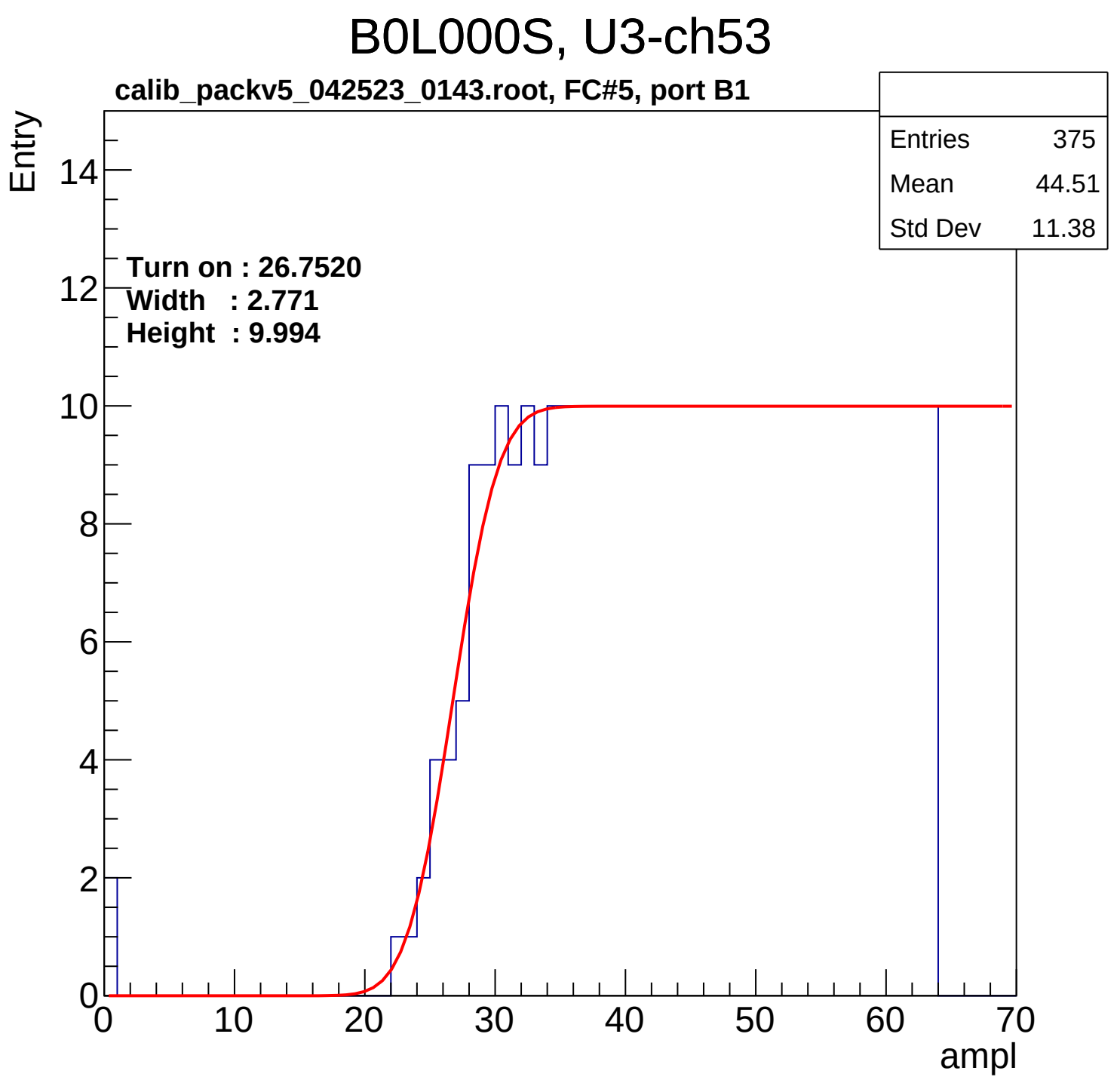
B0L000S, U3-ch53
calib_packv5_042523_0143.root, FC#5, port B1
Entries 375
Mean 44.51
Std Dev 11.38
Turn on : 26.7520
Width : 2.771
Height : 9.994
Entry
ampl
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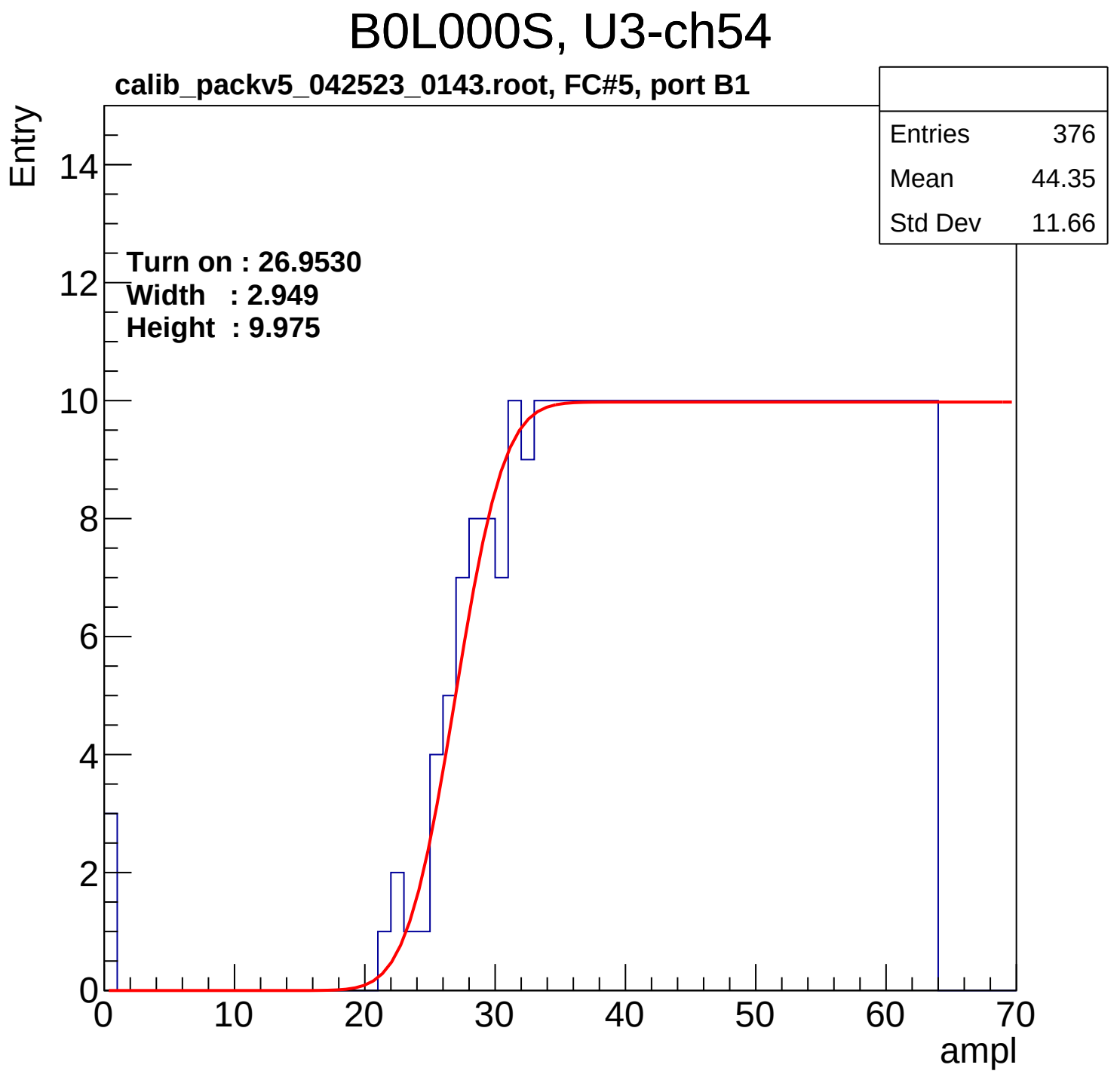
B0L000S, U3-ch54
calib_packv5_042523_0143.root, FC#5, port B1
Entries 376
Mean 44.35
Std Dev 11.66
Turn on : 26.9530
Width : 2.949
Height : 9.975
Entry
ampl
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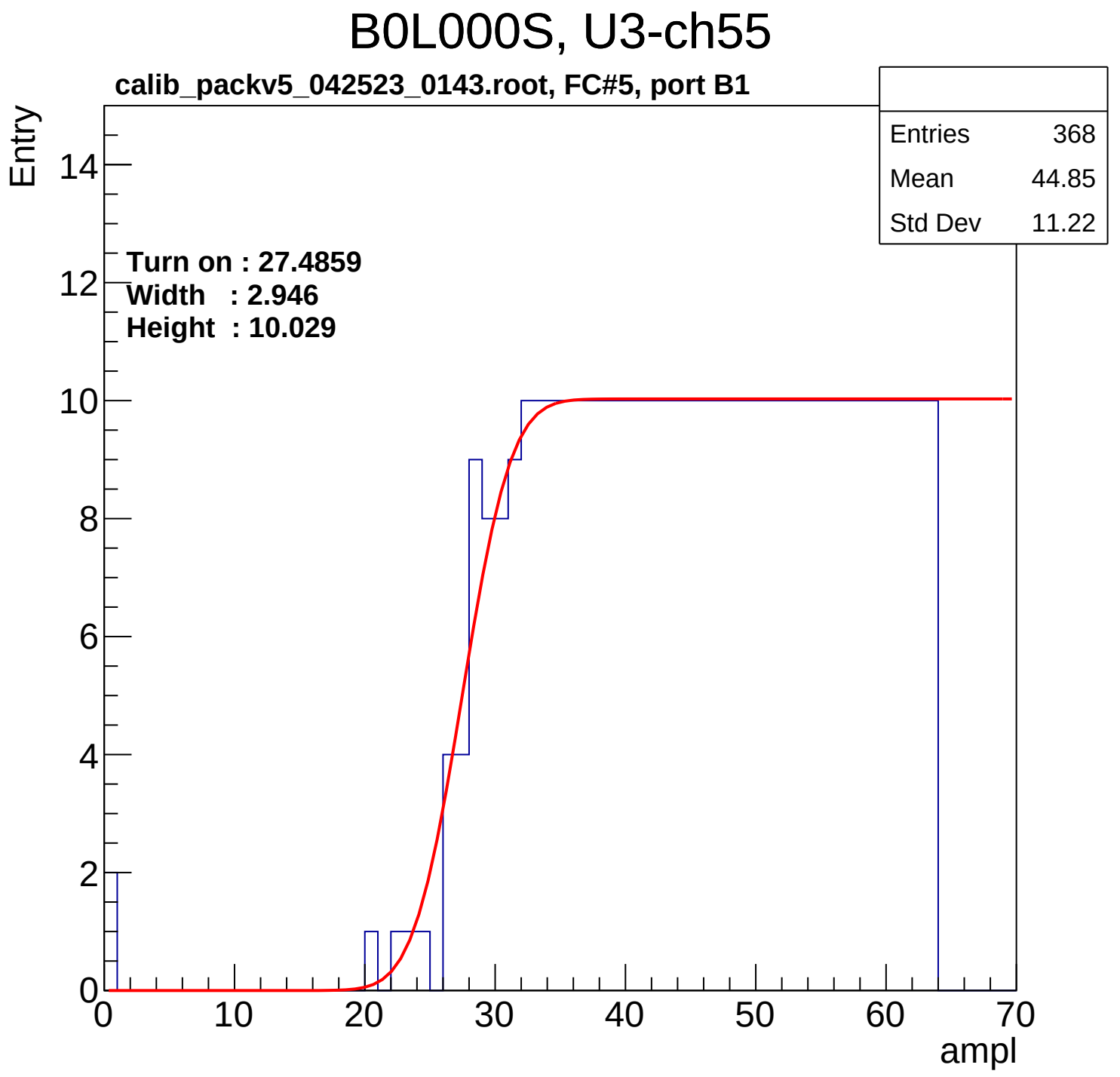
B0L000S, U3-ch55
calib_packv5_042523_0143.root, FC#5, port B1
Entries 368
Mean 44.85
Std Dev 11.22
Turn on : 27.4859
Width : 2.946
Height : 10.029
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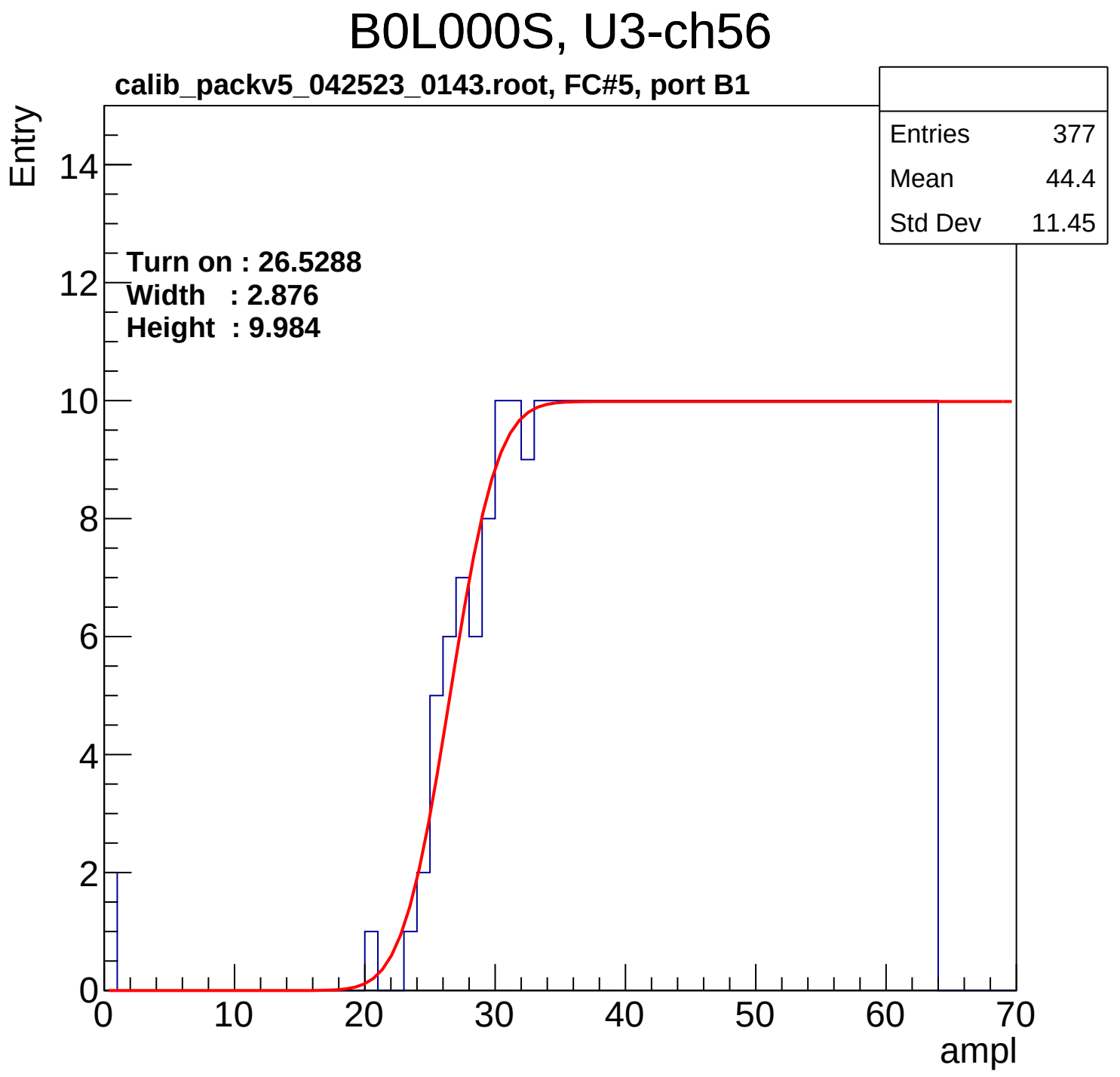
B0L000S, U3-ch56
calib_packv5_042523_0143.root, FC#5, port B1
Entries 377
Mean 44.4
Std Dev 11.45
Turn on : 26.5288
Width : 2.876
Height : 9.984
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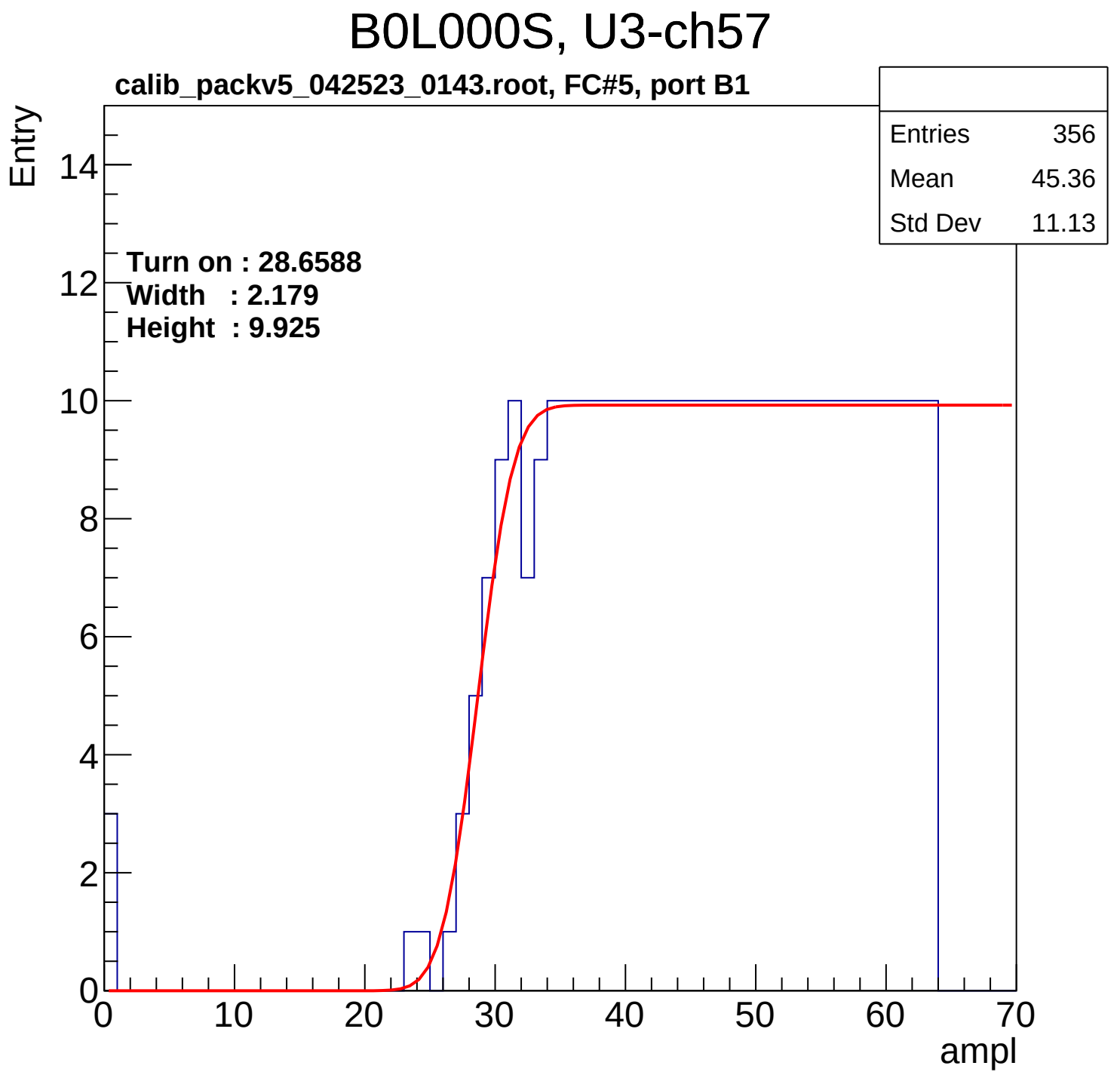
B0L000S, U3-ch57
calib_packv5_042523_0143.root, FC#5, port B1
Entries 356
Mean 45.36
Std Dev 11.13
Turn on : 28.6588
Width : 2.179
Height : 9.925
Entry
ampl
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4
6
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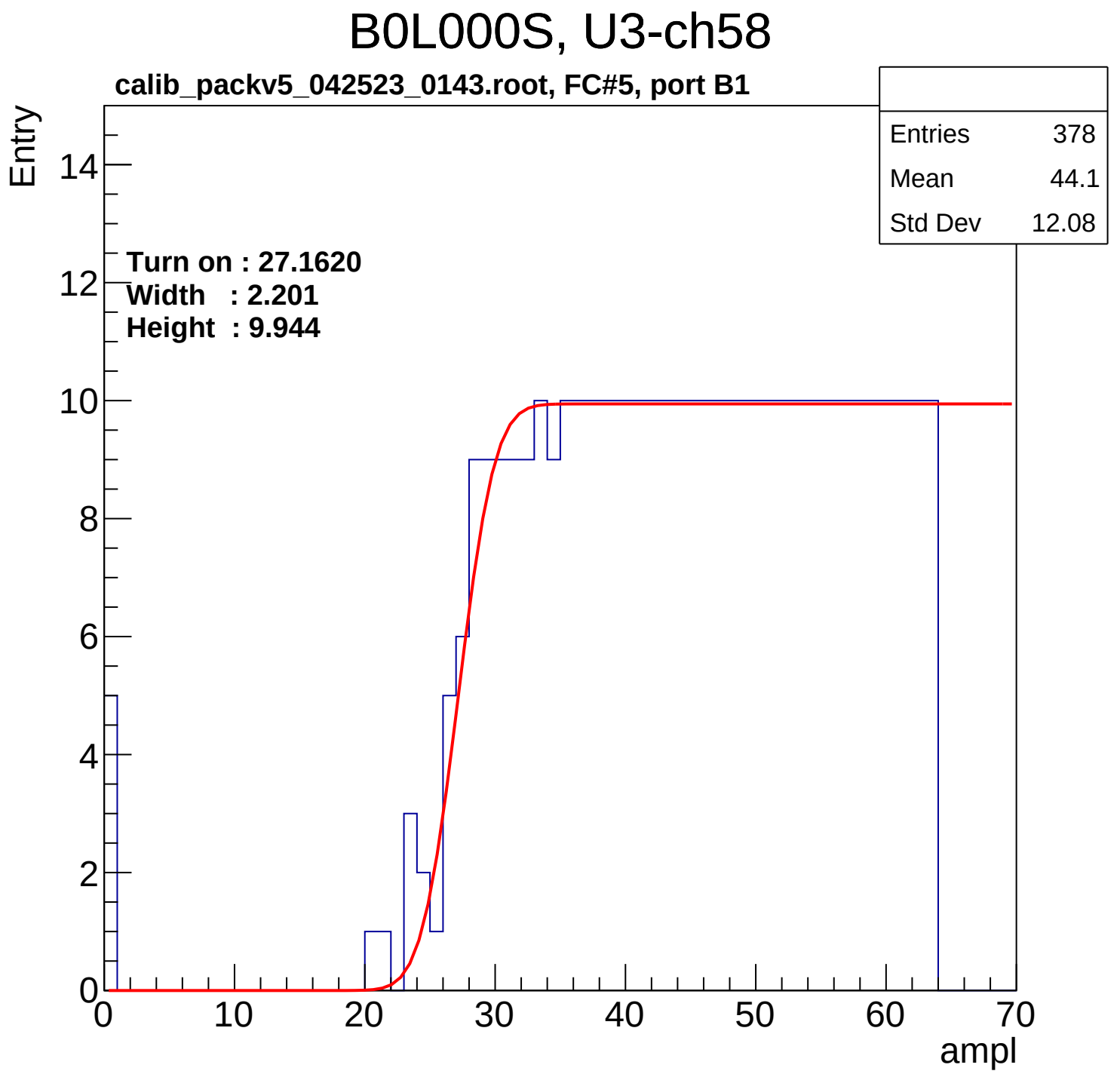
B0L000S, U3-ch58
calib_packv5_042523_0143.root, FC#5, port B1
Entries 378
Mean 44.1
Std Dev 12.08
Turn on : 27.1620
Width : 2.201
Height : 9.944
Entry
ampl
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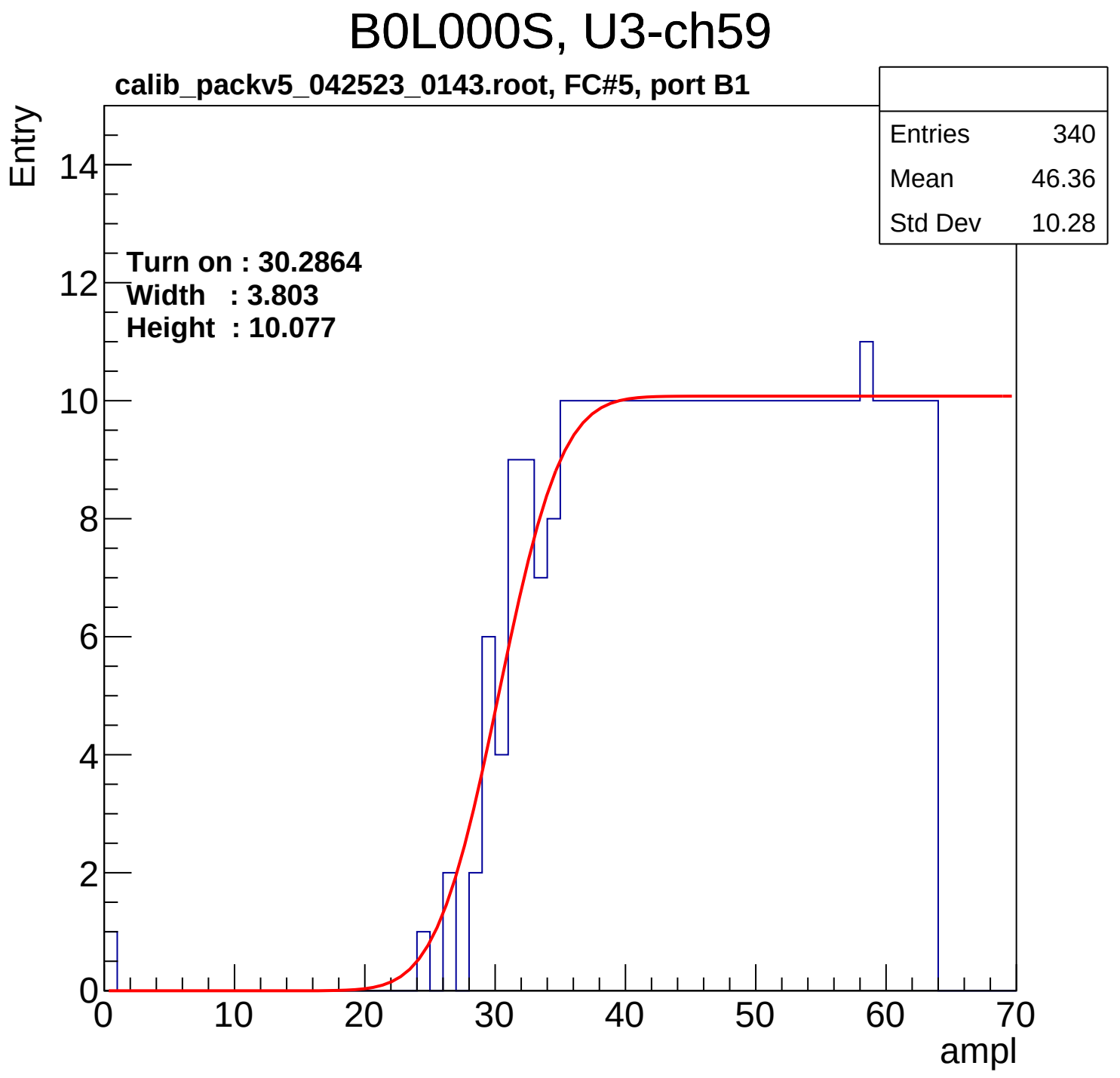
B0L000S, U3-ch59
calib_packv5_042523_0143.root, FC#5, port B1
Entries 340
Mean 46.36
Std Dev 10.28
Turn on : 30.2864
Width : 3.803
Height : 10.077
Entry
ampl
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2
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8
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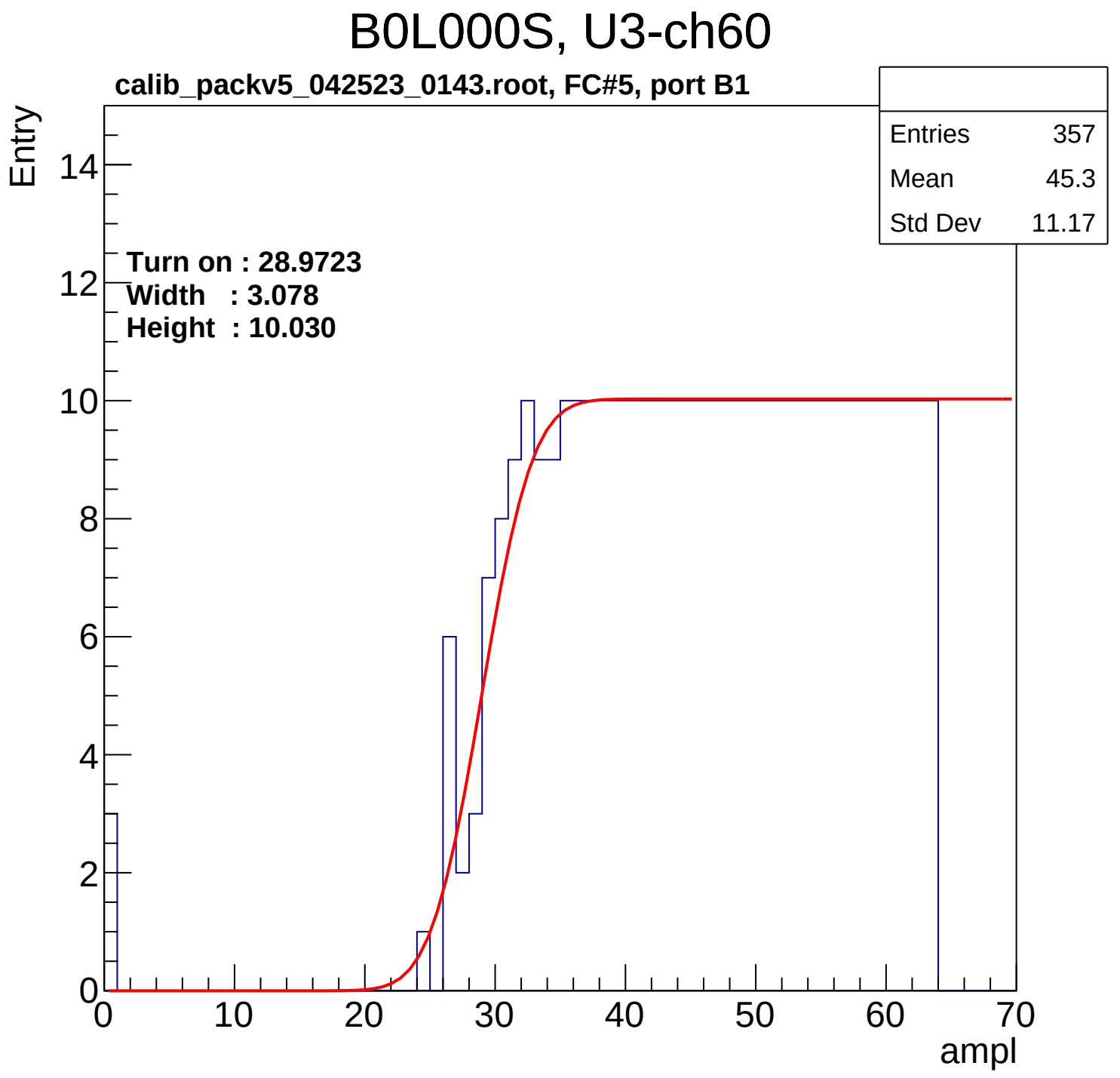
B0L000S, U3-ch60
calib_packv5_042523_0143.root, FC#5, port B1
Entries 357
Mean 45.3
Std Dev 11.17
Turn on : 28.9723
Width : 3.078
Height : 10.030
Entry
ampl
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4
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8
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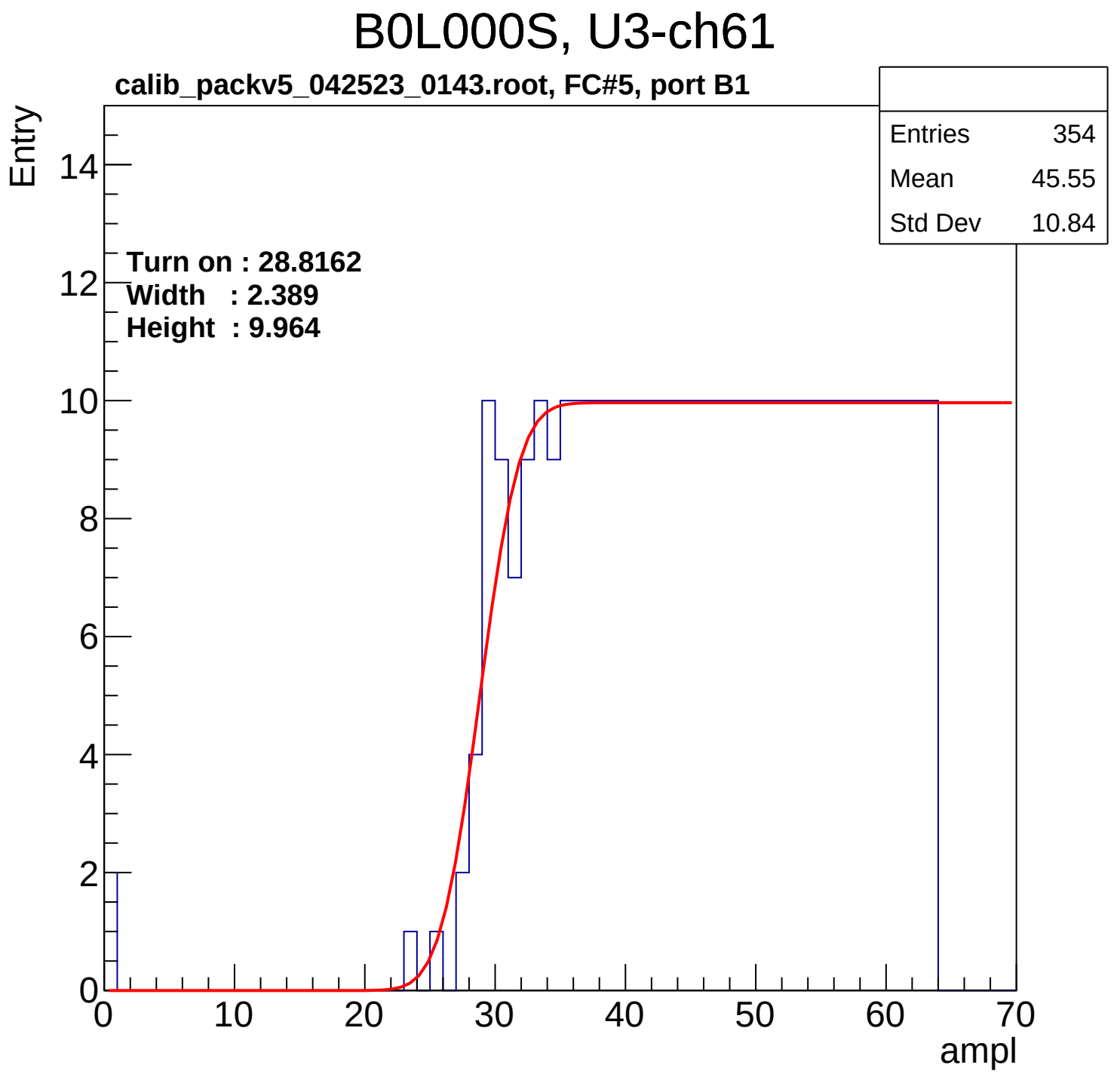
B0L000S, U3-ch61
calib_packv5_042523_0143.root, FC#5, port B1
Entries 354
Mean 45.55
Std Dev 10.84
Turn on : 28.8162
Width : 2.389
Height : 9.964
Entry
ampl
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2
4
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0
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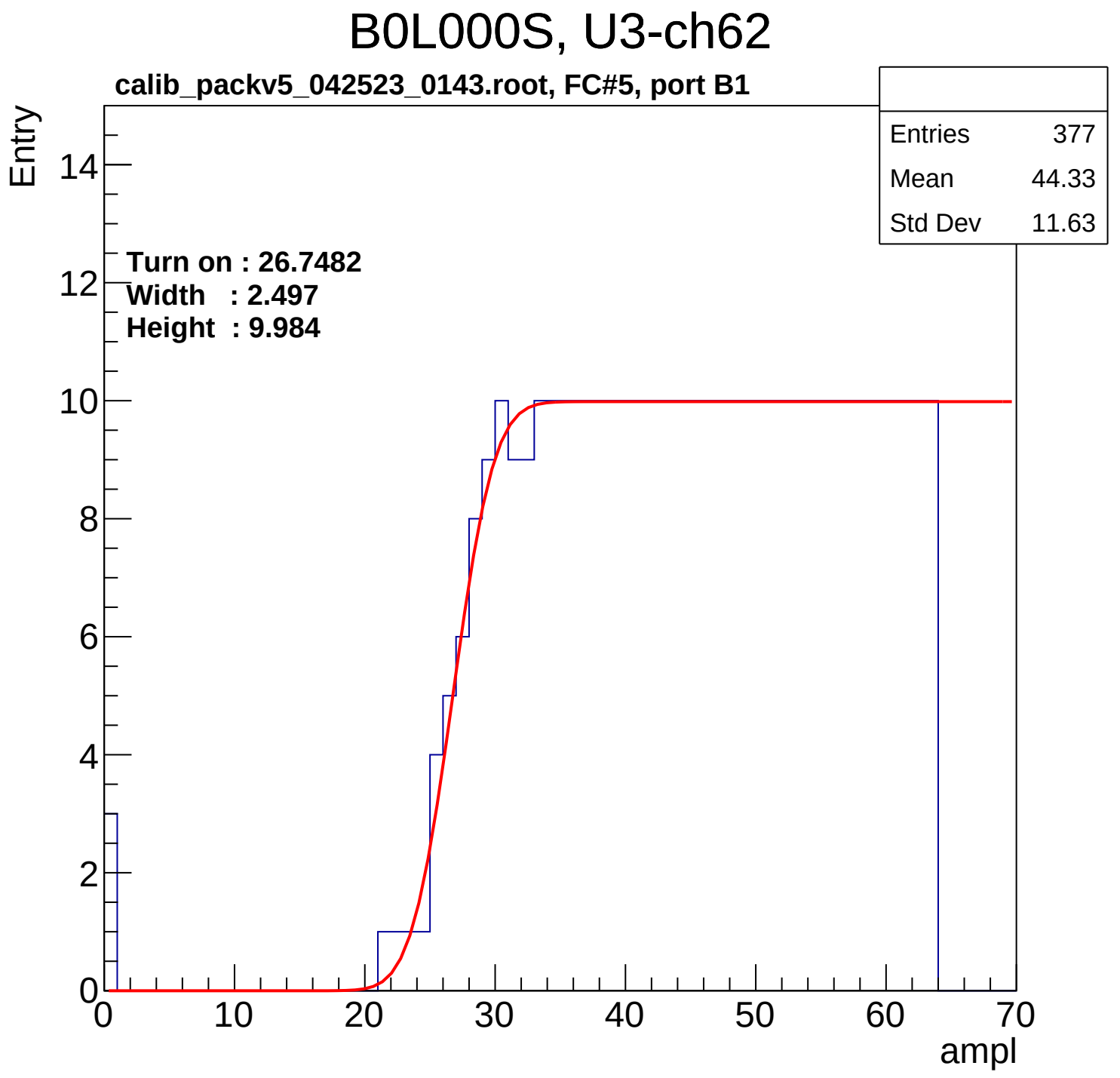
B0L000S, U3-ch62
calib_packv5_042523_0143.root, FC#5, port B1
Entries 377
Mean 44.33
Std Dev 11.63
Turn on : 26.7482
Width : 2.497
Height : 9.984
Entry
ampl
0
2
4
6
8
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12
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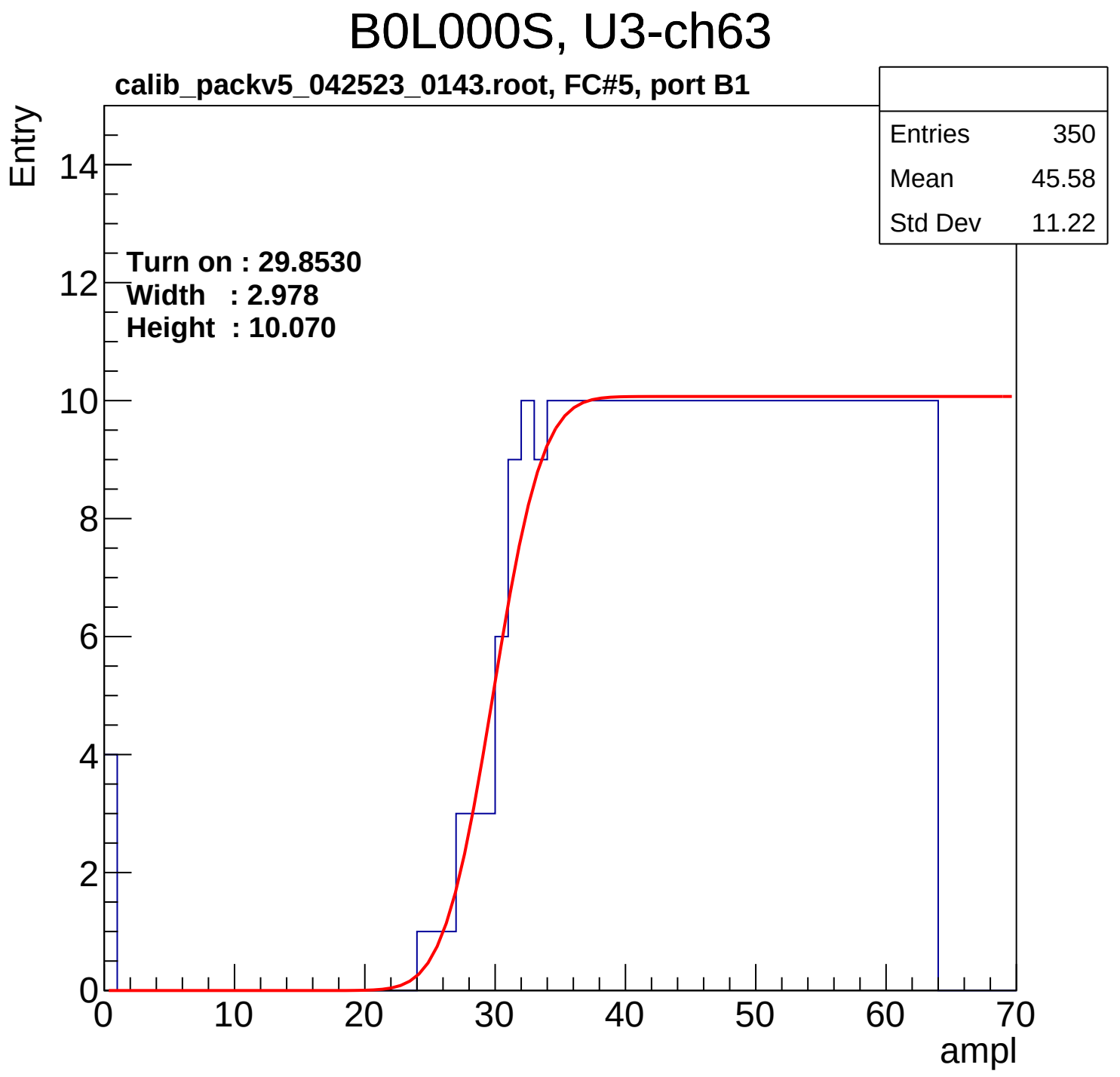
B0L000S, U3-ch63
calib_packv5_042523_0143.root, FC#5, port B1
Entries 350
Mean 45.58
Std Dev 11.22
Turn on : 29.8530
Width : 2.978
Height : 10.070
Entry
ampl
0
2
4
6
8
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12
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0
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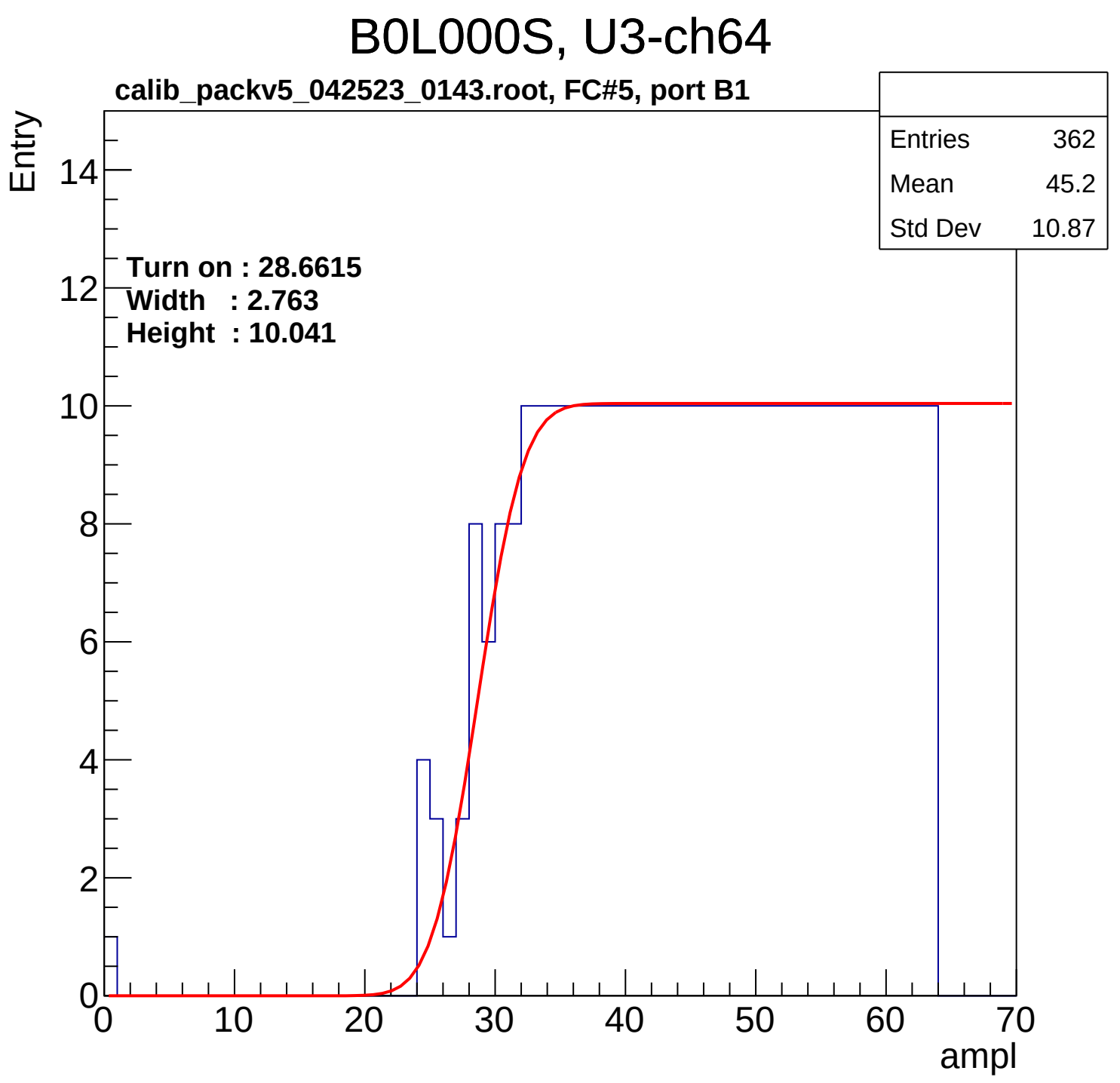
B0L000S, U3-ch64
calib_packv5_042523_0143.root, FC#5, port B1
Entries 362
Mean 45.2
Std Dev 10.87
Turn on : 28.6615
Width : 2.763
Height : 10.041
Entry
ampl
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2
4
6
8
10
12
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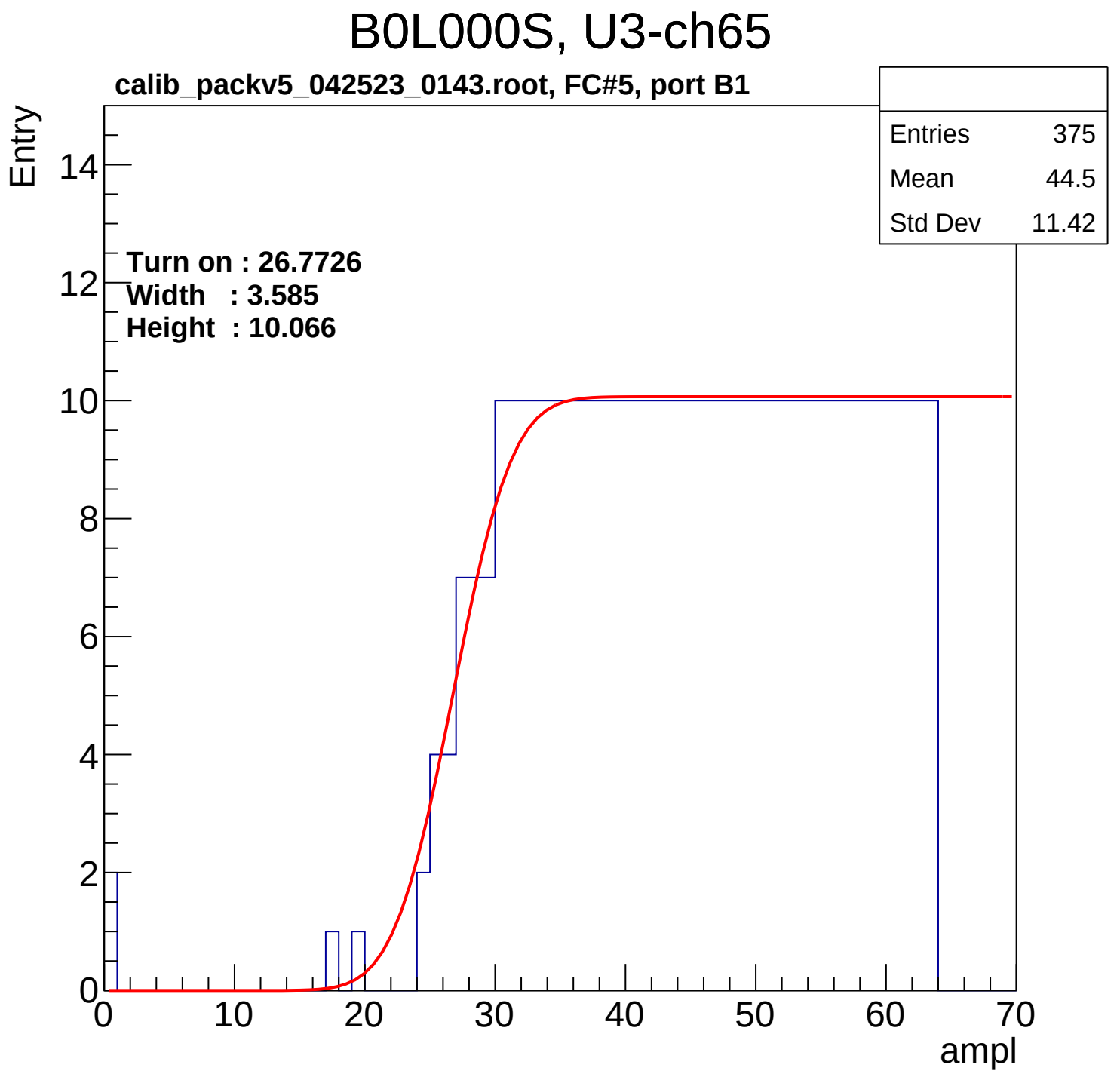
B0L000S, U3-ch65
calib_packv5_042523_0143.root, FC#5, port B1
Entries 375
Mean 44.5
Std Dev 11.42
Turn on : 26.7726
Width : 3.585
Height : 10.066
Entry
ampl
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2
4
6
8
10
12
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0
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60
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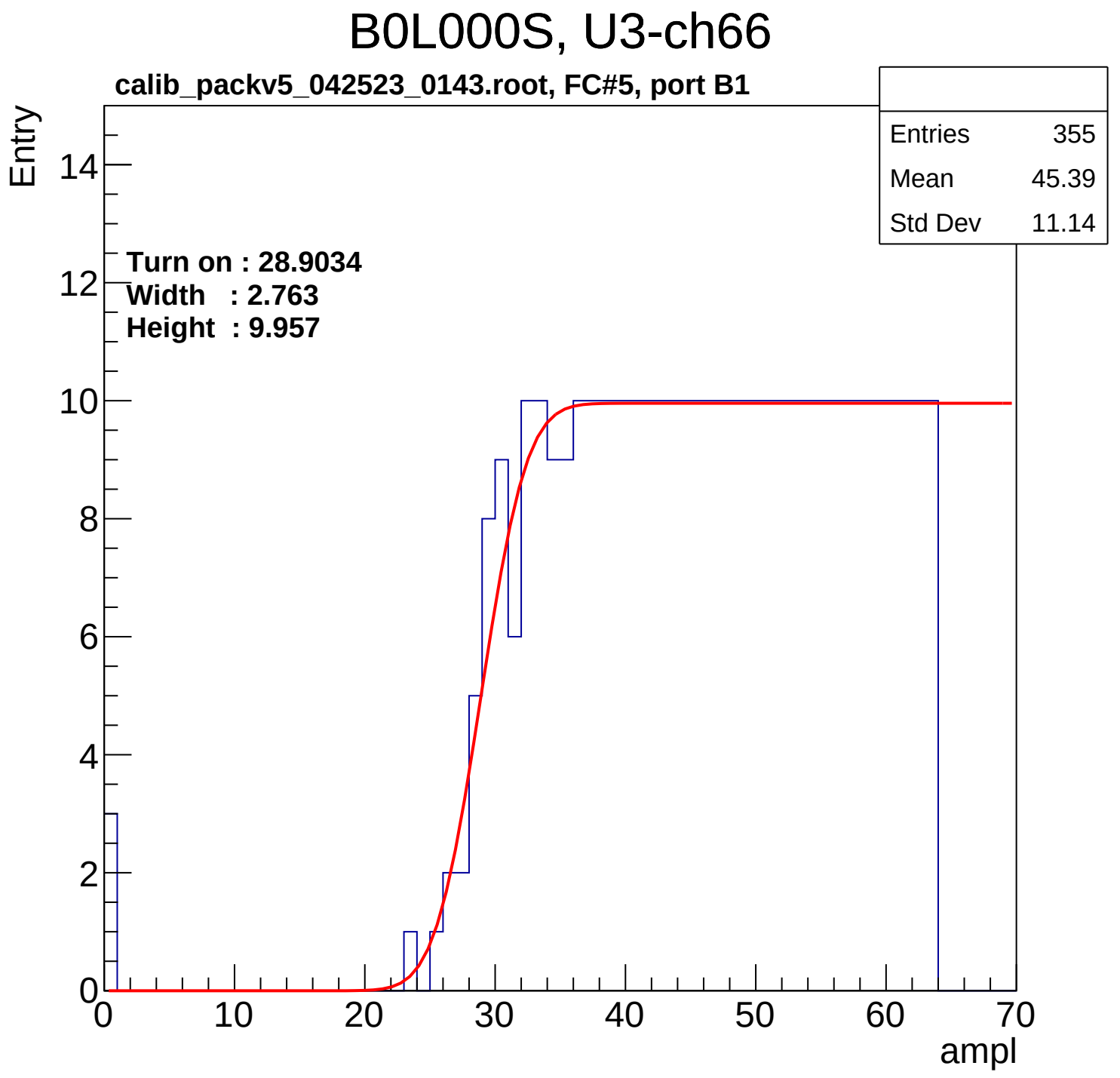
B0L000S, U3-ch66
calib_packv5_042523_0143.root, FC#5, port B1
Entries 355
Mean 45.39
Std Dev 11.14
Turn on : 28.9034
Width : 2.763
Height : 9.957
Entry
ampl
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6
8
10
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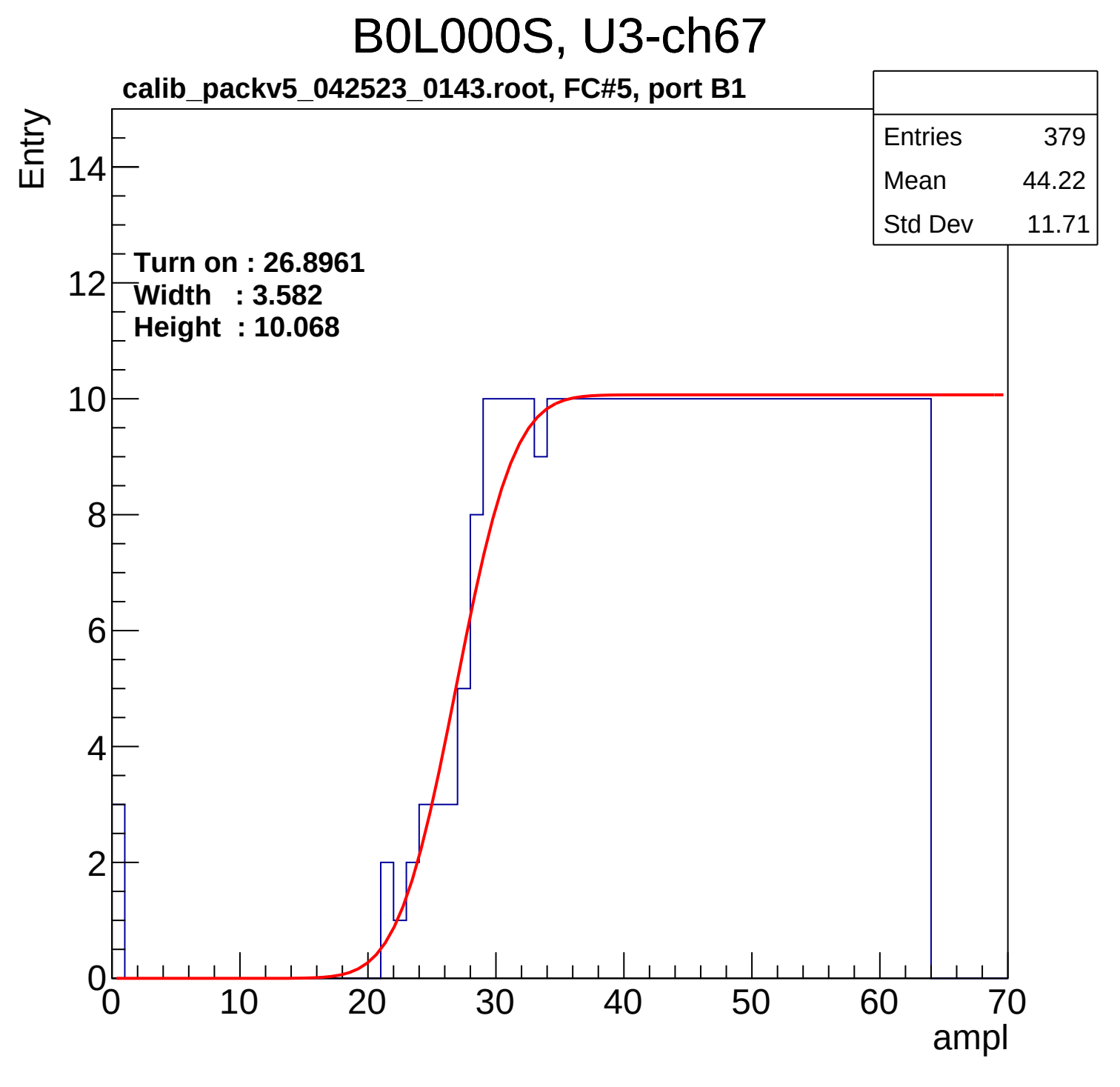
B0L000S, U3-ch67
calib_packv5_042523_0143.root, FC#5, port B1
Entries 379
Mean 44.22
Std Dev 11.71
Turn on : 26.8961
Width : 3.582
Height : 10.068
Entry
ampl
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2
4
6
8
10
12
14
0
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60
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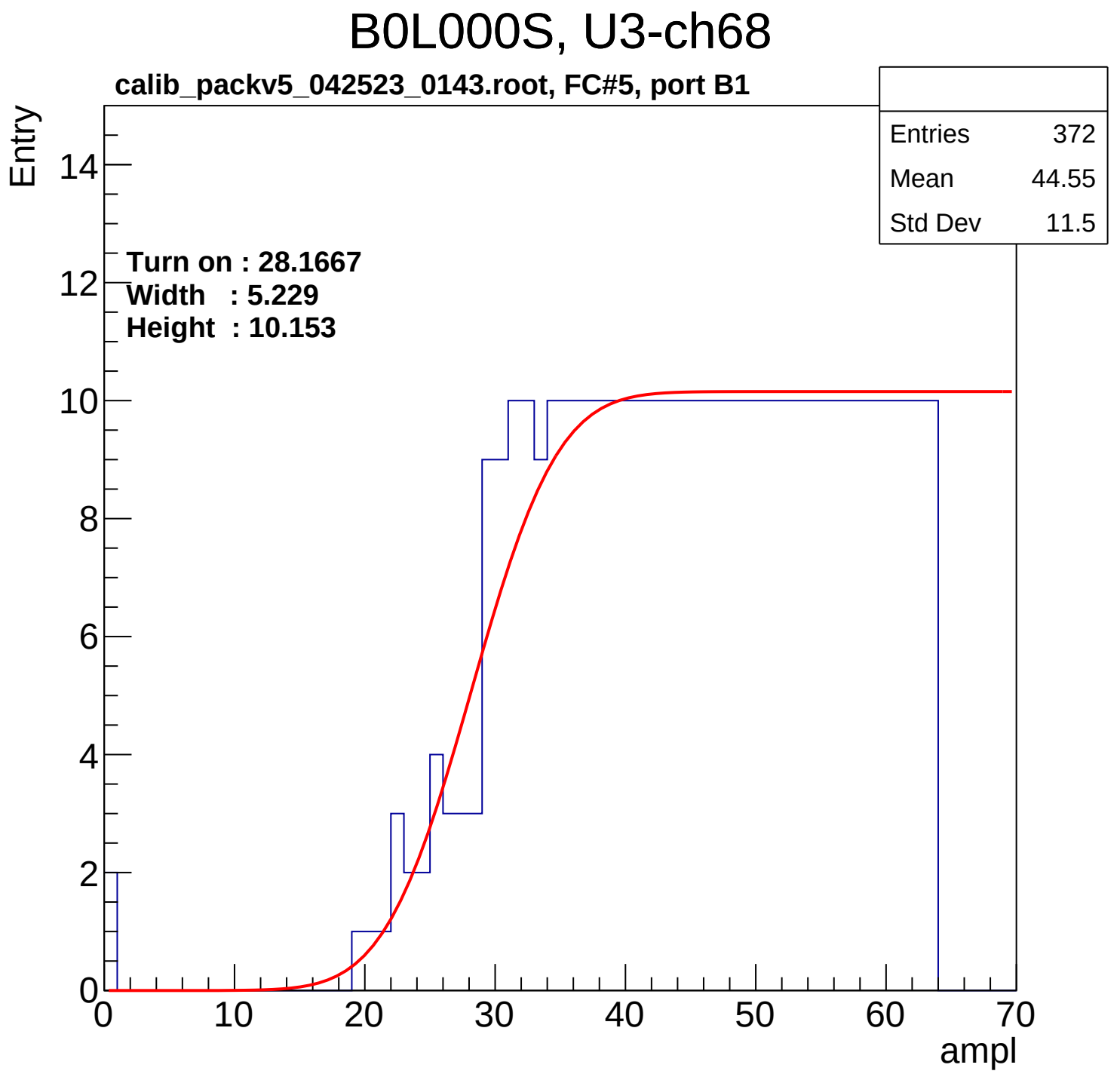
B0L000S, U3-ch68
calib_packv5_042523_0143.root, FC#5, port B1
Entries 372
Mean 44.55
Std Dev 11.5
Turn on : 28.1667
Width : 5.229
Height : 10.153
Entry
ampl
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0
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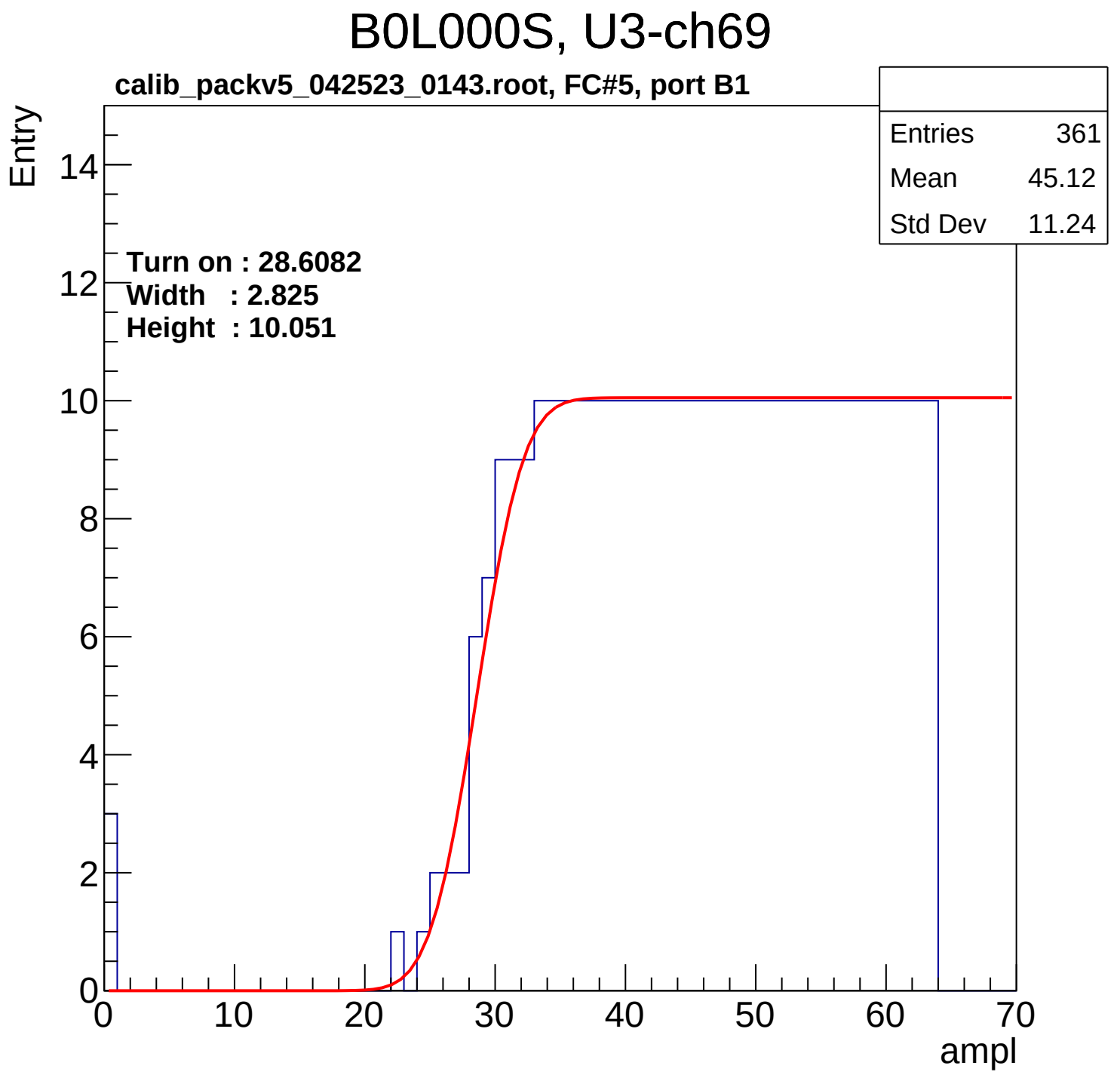
B0L000S, U3-ch69
calib_packv5_042523_0143.root, FC#5, port B1
Entries 361
Mean 45.12
Std Dev 11.24
Turn on : 28.6082
Width : 2.825
Height : 10.051
Entry
ampl
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2
4
6
8
10
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0
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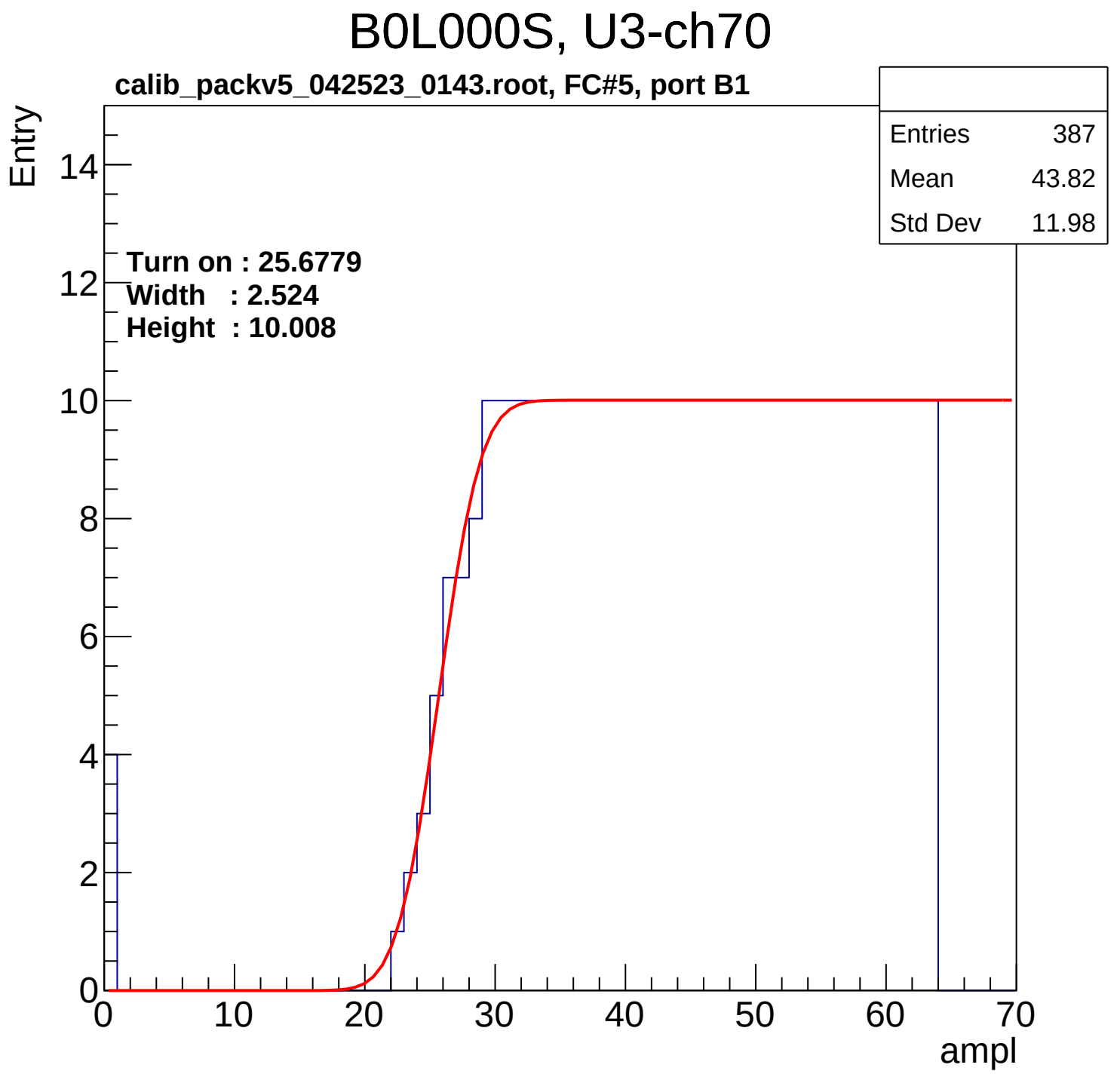
B0L000S, U3-ch70
calib_packv5_042523_0143.root, FC#5, port B1
Entries 387
Mean 43.82
Std Dev 11.98
Turn on : 25.6779
Width : 2.524
Height : 10.008
Entry
ampl
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6
8
10
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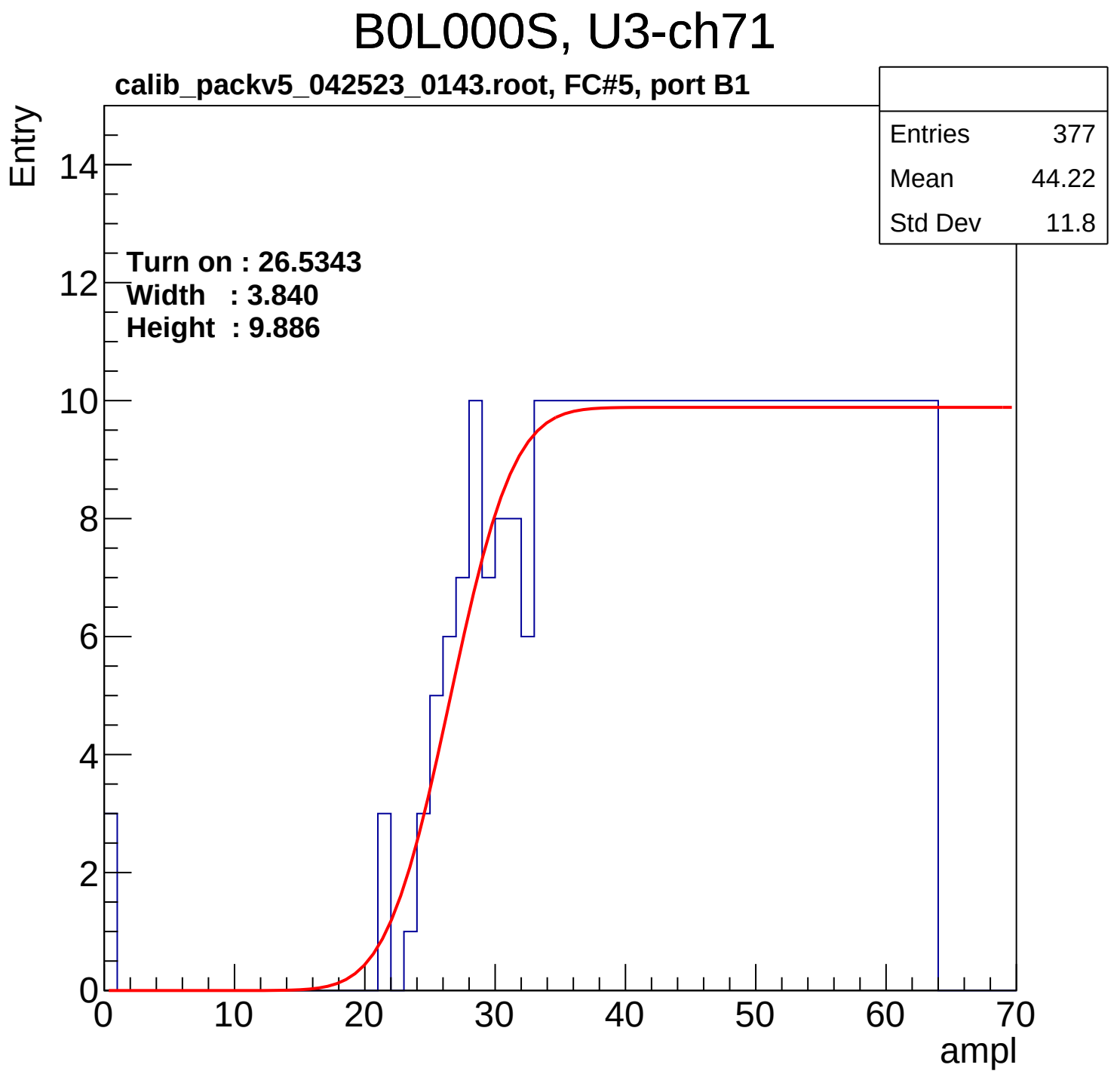
B0L000S, U3-ch71
calib_packv5_042523_0143.root, FC#5, port B1
Entries 377
Mean 44.22
Std Dev 11.8
Turn on : 26.5343
Width : 3.840
Height : 9.886
Entry
ampl
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6
8
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0
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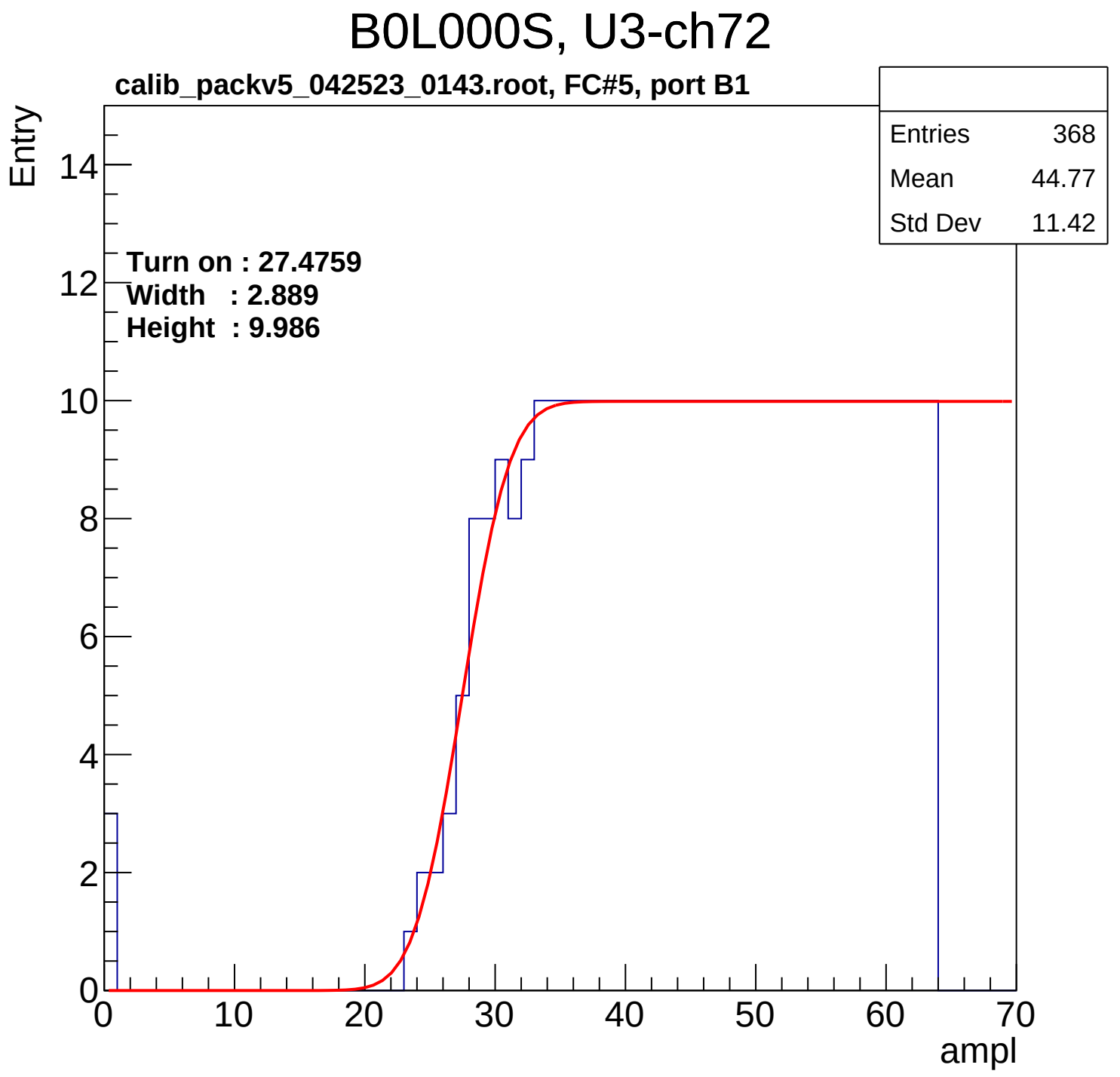
B0L000S, U3-ch72
calib_packv5_042523_0143.root, FC#5, port B1
Entries 368
Mean 44.77
Std Dev 11.42
Turn on : 27.4759
Width : 2.889
Height : 9.986
Entry
ampl
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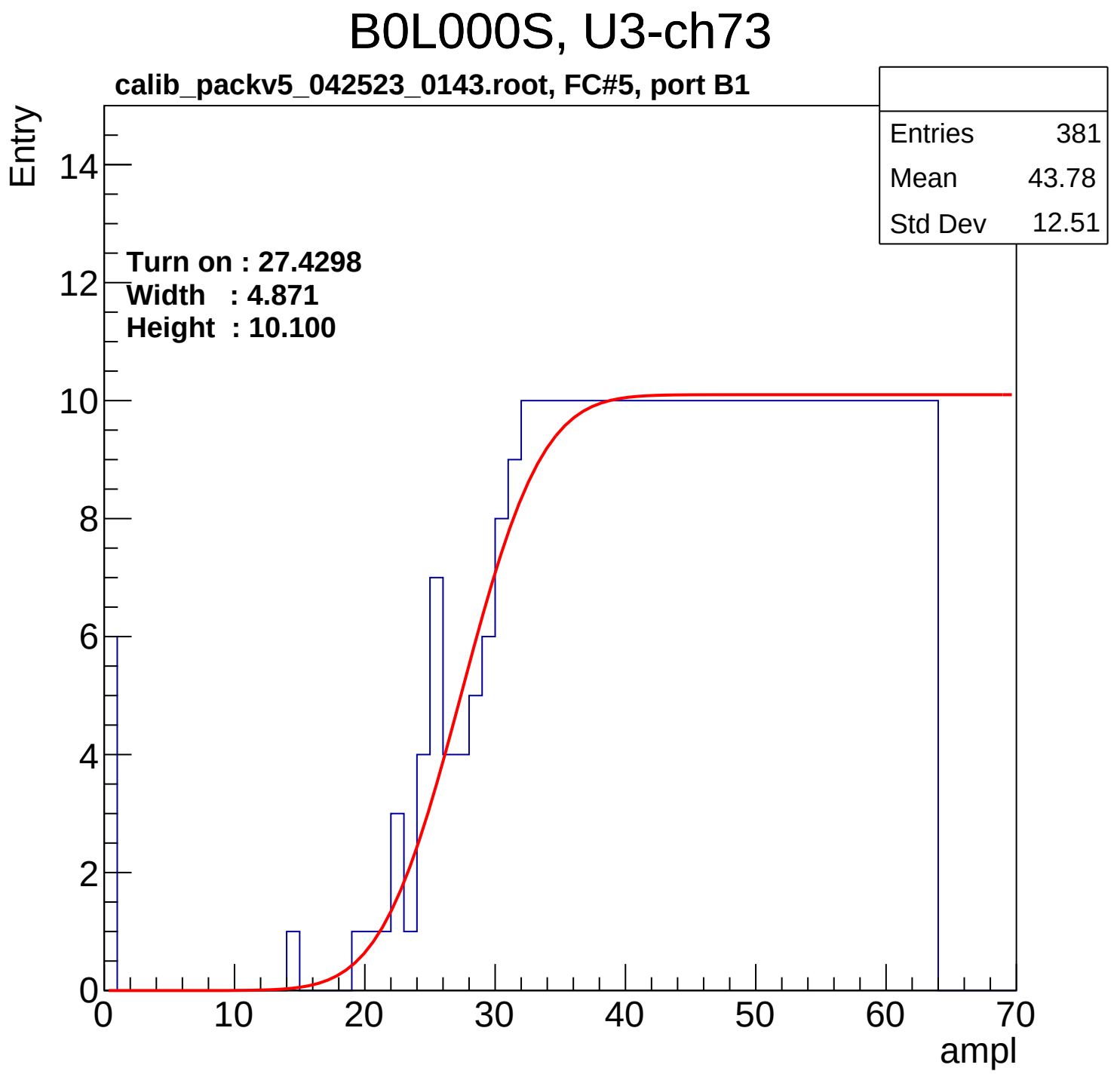
B0L000S, U3-ch73
calib_packv5_042523_0143.root, FC#5, port B1
Entries 381
Mean 43.78
Std Dev 12.51
Turn on : 27.4298
Width : 4.871
Height : 10.100
Entry
ampl
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4
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8
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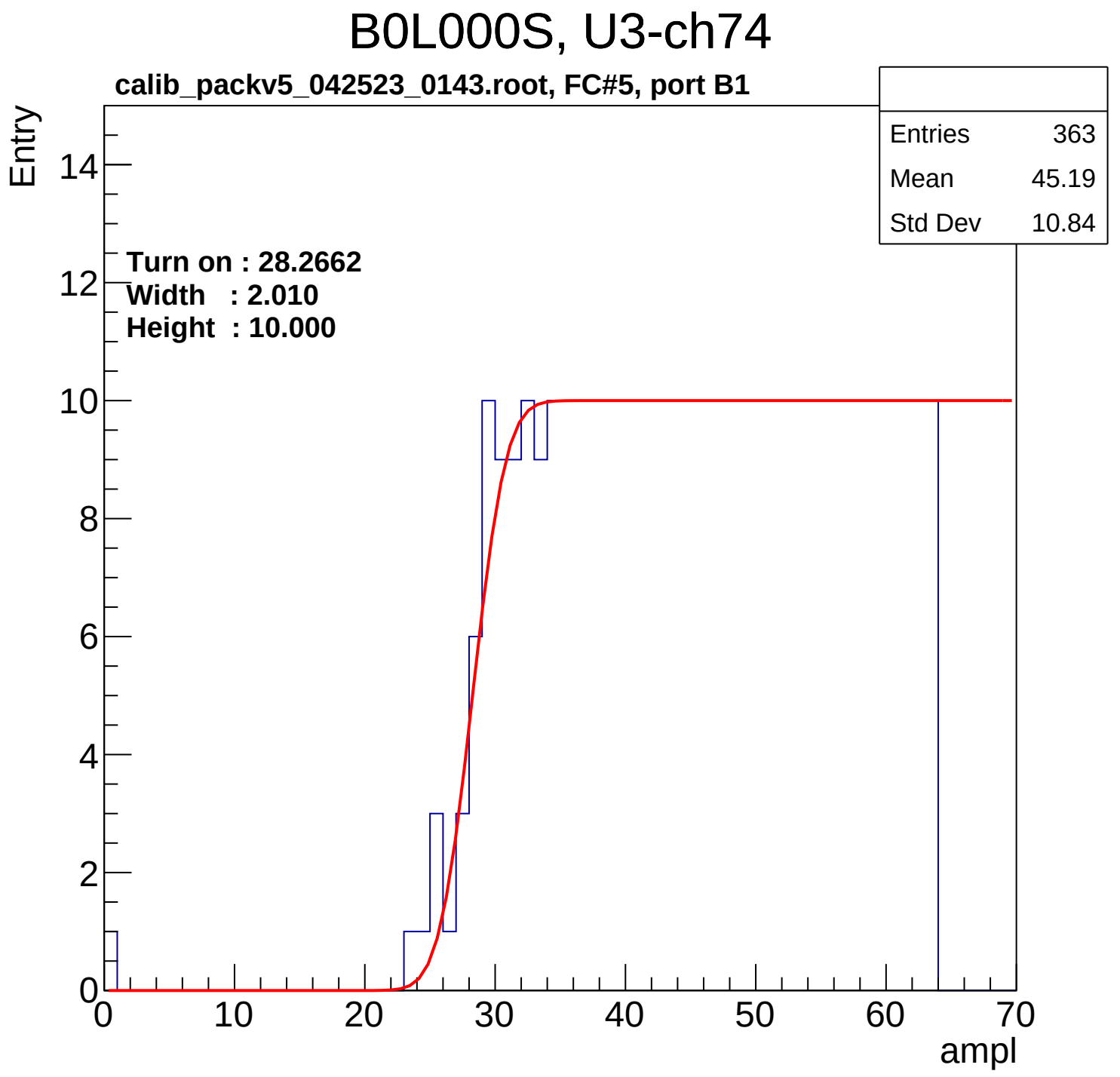
B0L000S, U3-ch74
calib_packv5_042523_0143.root, FC#5, port B1
Entries 363
Mean 45.19
Std Dev 10.84
Turn on : 28.2662
Width : 2.010
Height : 10.000
Entry
ampl
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6
8
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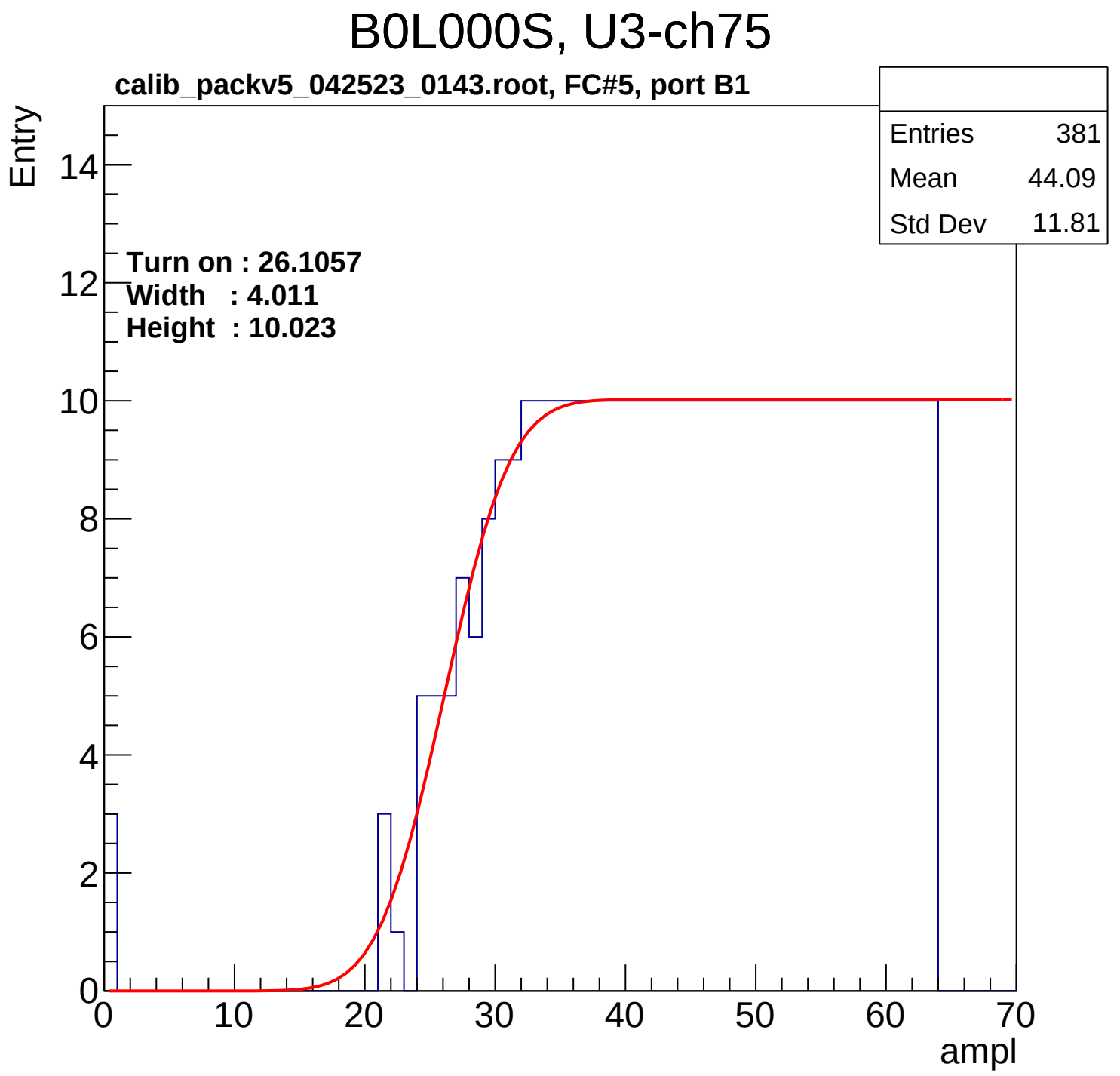
B0L000S, U3-ch75
calib_packv5_042523_0143.root, FC#5, port B1
Entries 381
Mean 44.09
Std Dev 11.81
Turn on : 26.1057
Width : 4.011
Height : 10.023
Entry
ampl
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6
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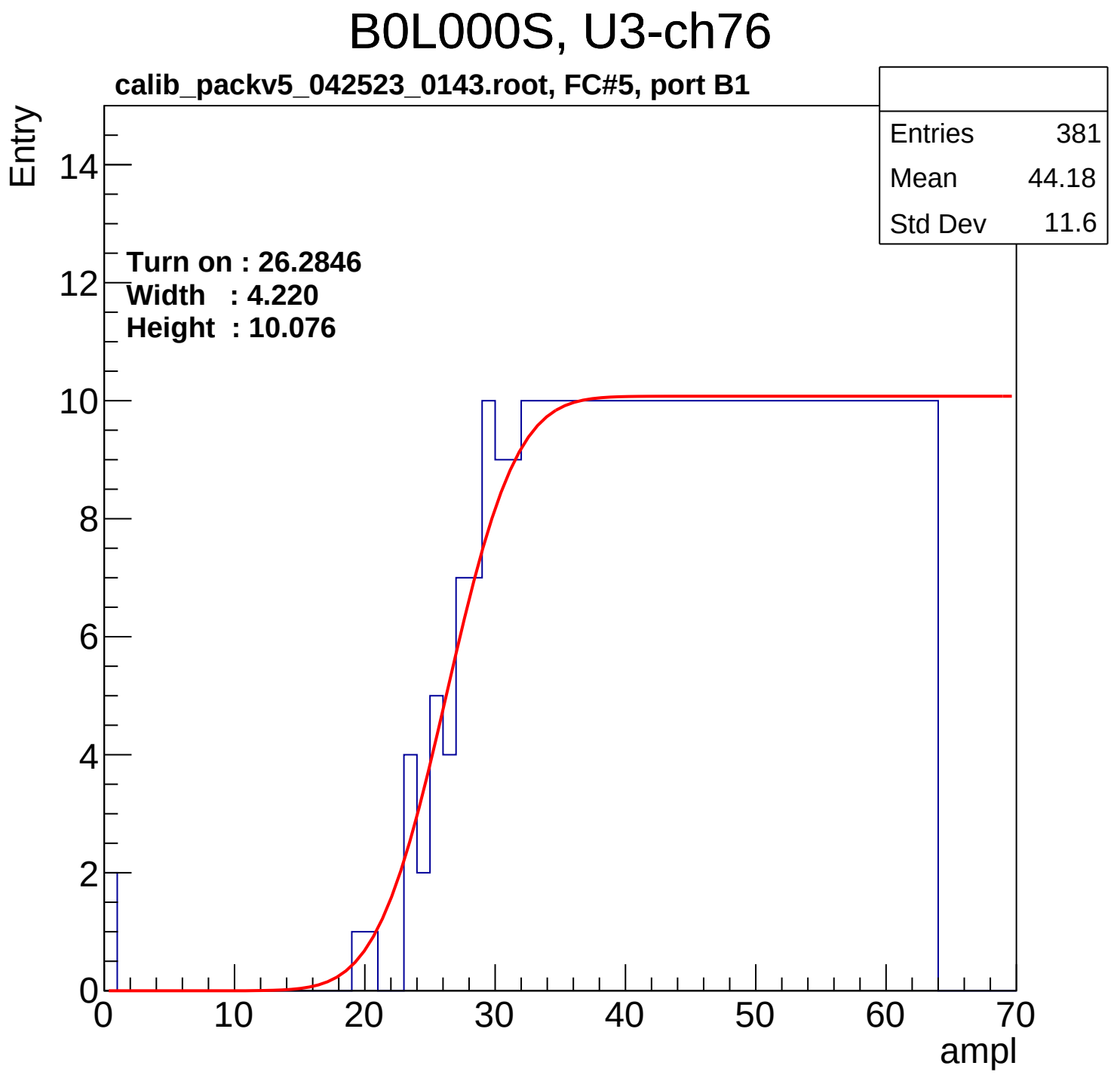
B0L000S, U3-ch76
calib_packv5_042523_0143.root, FC#5, port B1
Entries 381
Mean 44.18
Std Dev 11.6
Turn on : 26.2846
Width : 4.220
Height : 10.076
Entry
ampl
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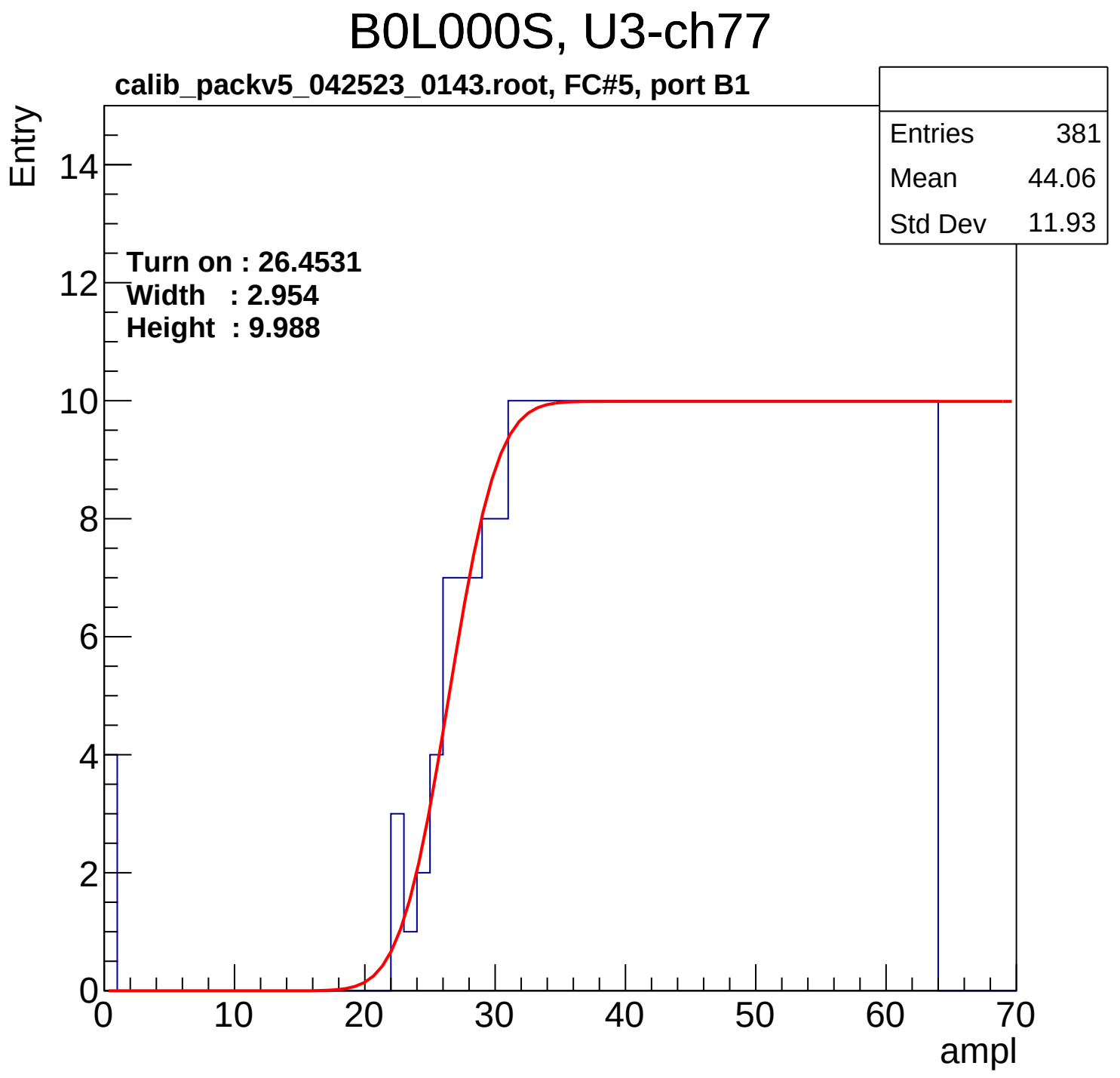
B0L000S, U3-ch77
calib_packv5_042523_0143.root, FC#5, port B1
Entries 381
Mean 44.06
Std Dev 11.93
Turn on : 26.4531
Width : 2.954
Height : 9.988
Entry
ampl
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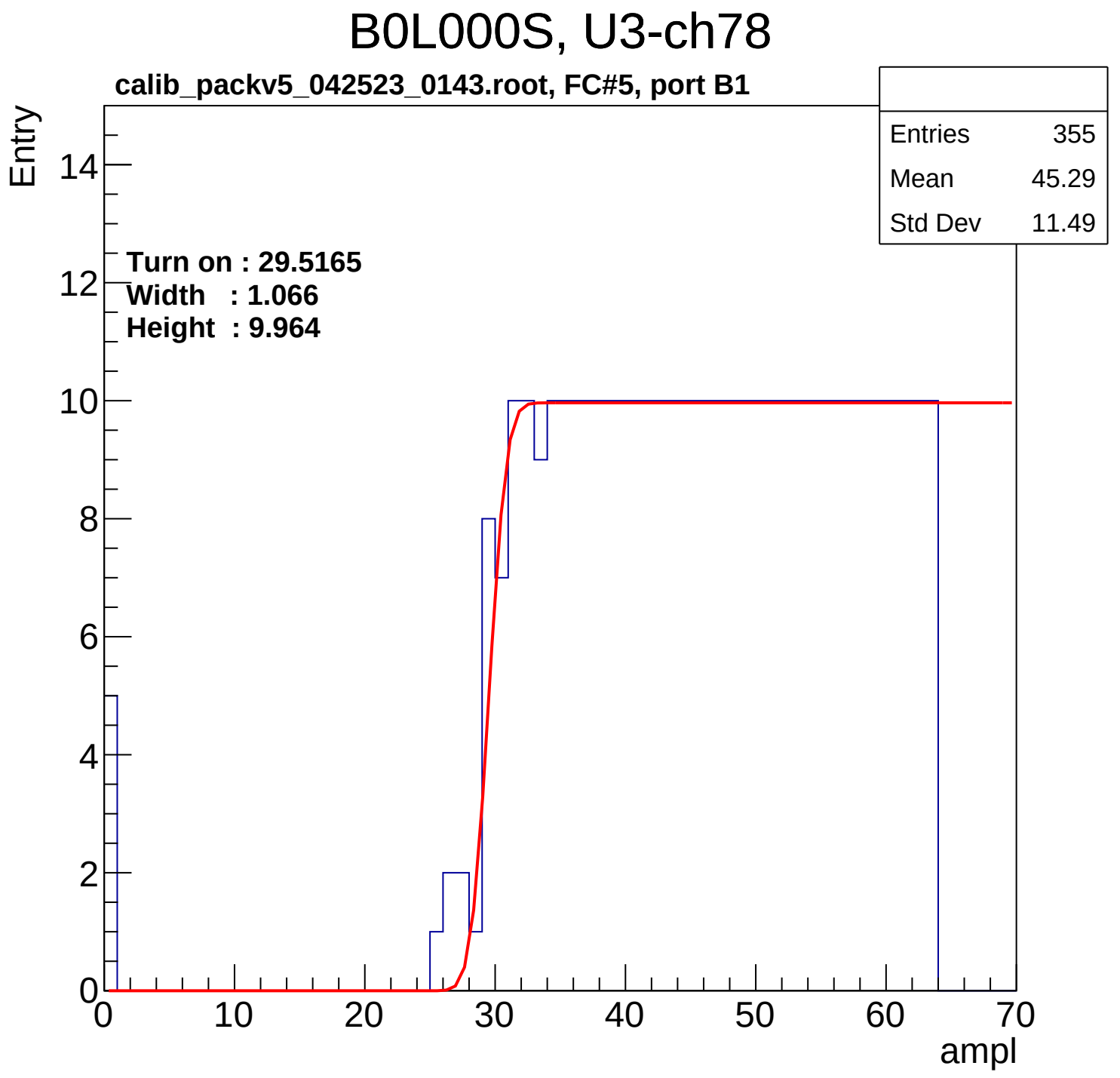
B0L000S, U3-ch78
calib_packv5_042523_0143.root, FC#5, port B1
Entries 355
Mean 45.29
Std Dev 11.49
Turn on : 29.5165
Width : 1.066
Height : 9.964
Entry
ampl
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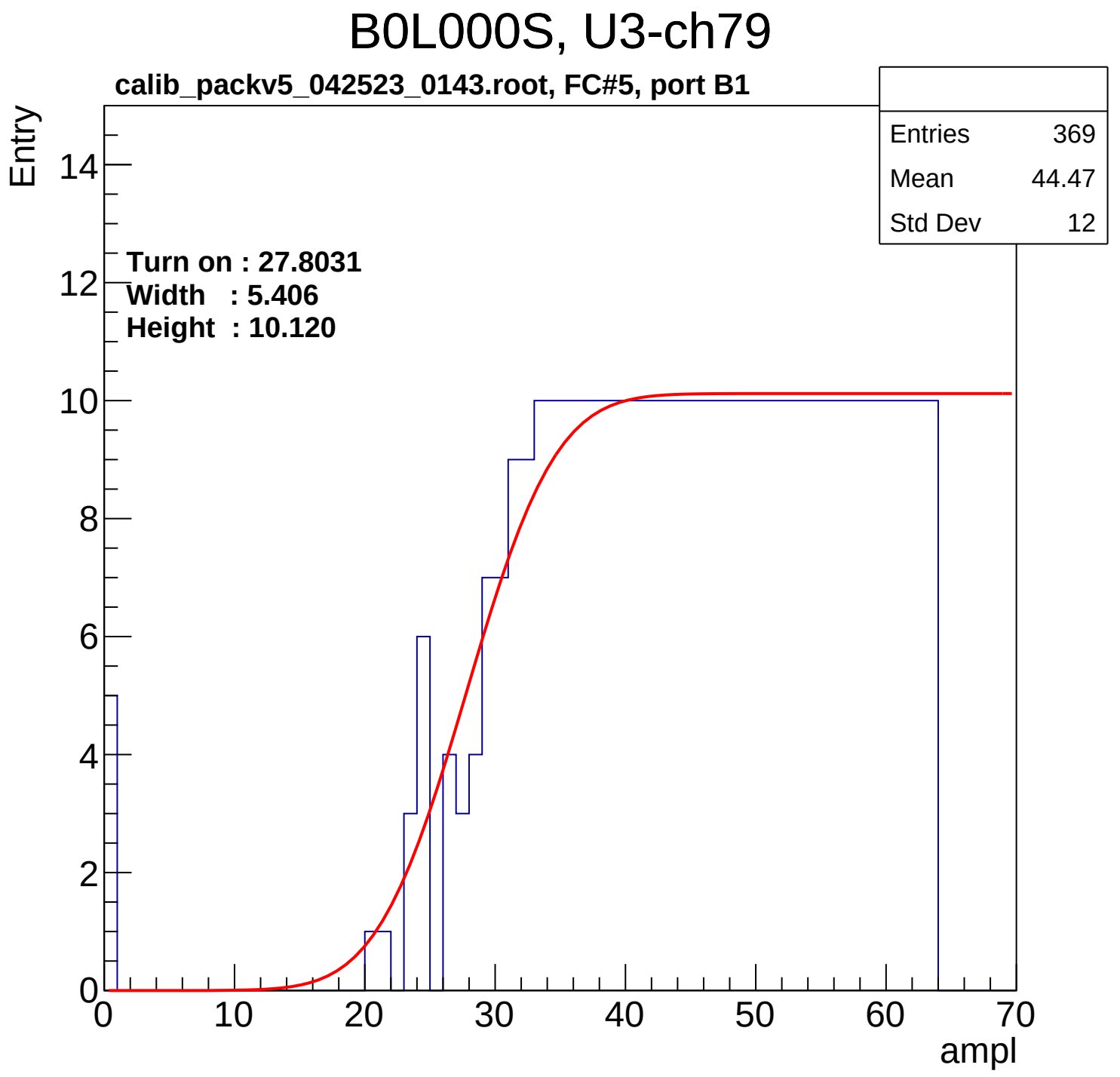
B0L000S, U3-ch79
calib_packv5_042523_0143.root, FC#5, port B1
Entries 369
Mean 44.47
Std Dev 12
Turn on : 27.8031
Width : 5.406
Height : 10.120
Entry
ampl
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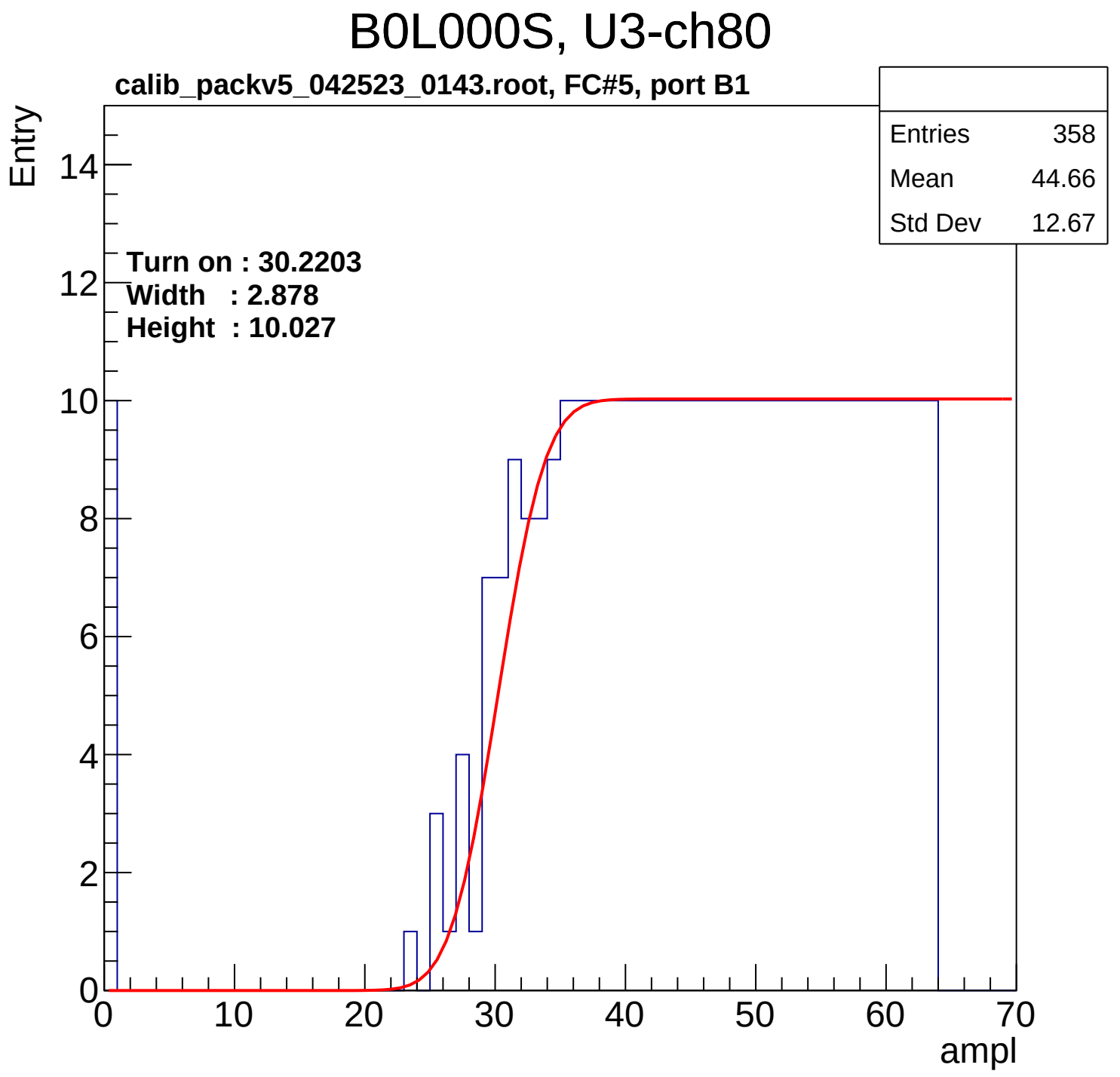
B0L000S, U3-ch80
calib_packv5_042523_0143.root, FC#5, port B1
Entries 358
Mean 44.66
Std Dev 12.67
Turn on : 30.2203
Width : 2.878
Height : 10.027
Entry
ampl
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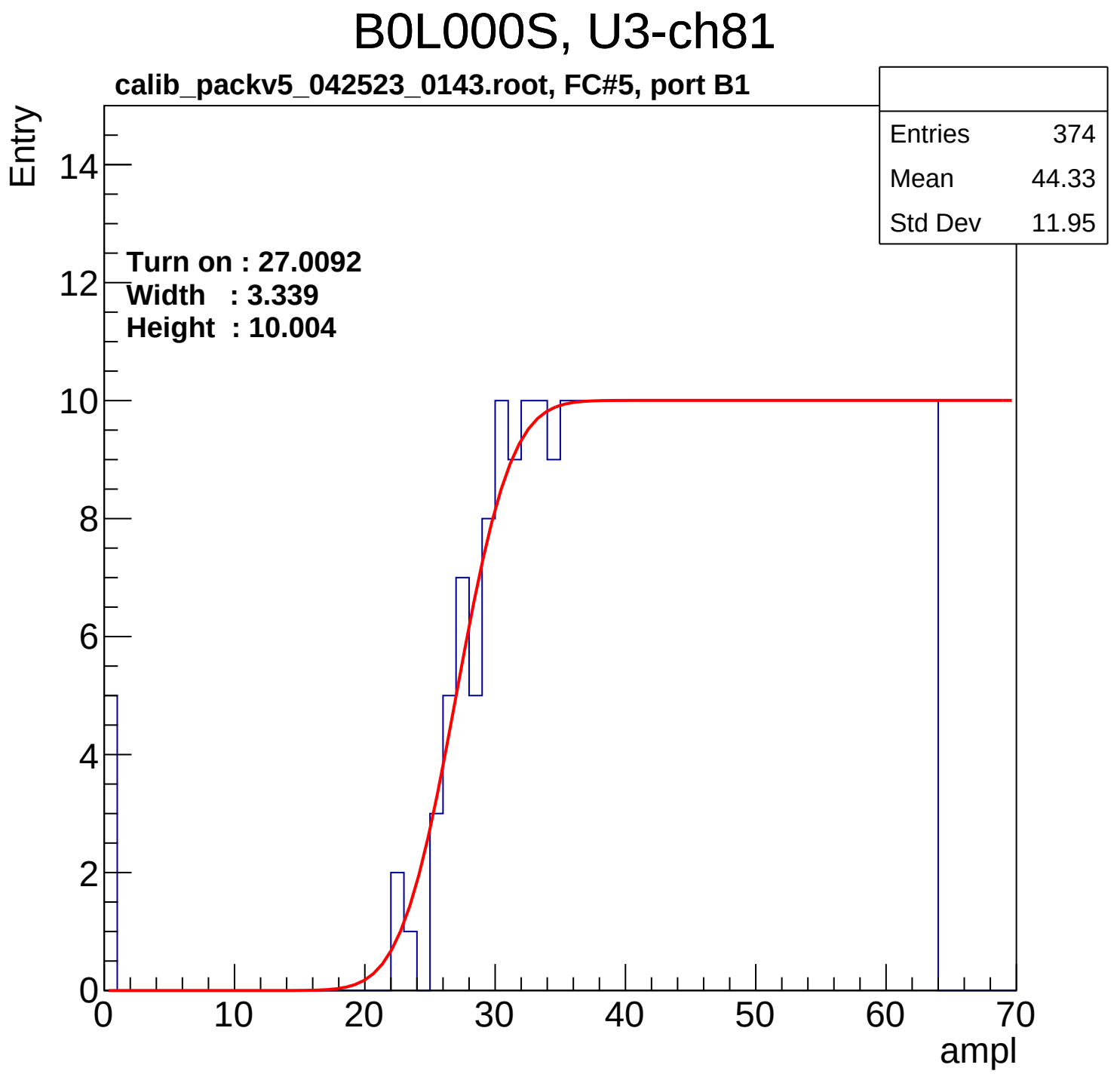
B0L000S, U3-ch81
calib_packv5_042523_0143.root, FC#5, port B1
Entries 374
Mean 44.33
Std Dev 11.95
Turn on : 27.0092
Width : 3.339
Height : 10.004
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ampl
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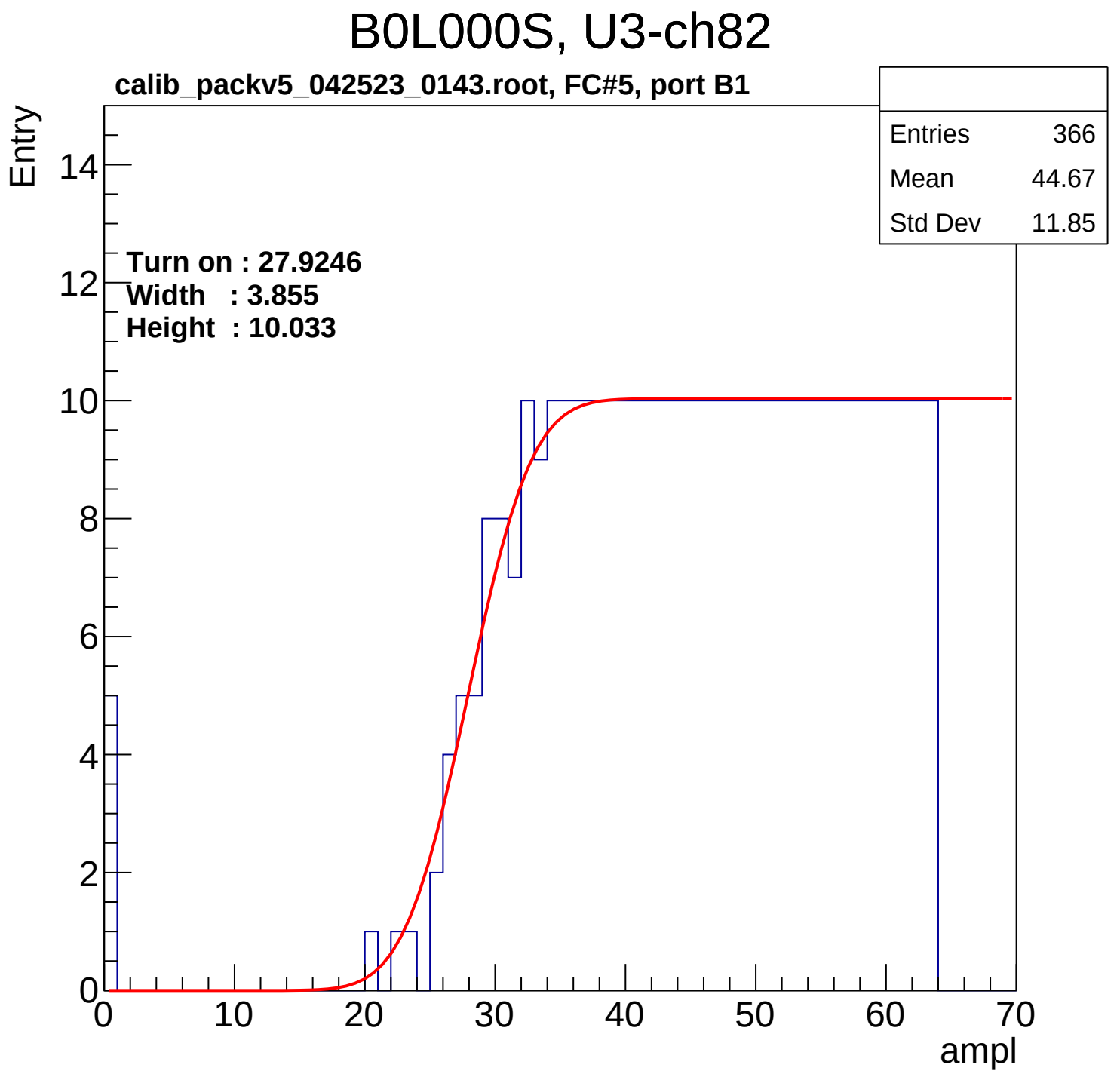
B0L000S, U3-ch82
calib_packv5_042523_0143.root, FC#5, port B1
Entries 366
Mean 44.67
Std Dev 11.85
Turn on : 27.9246
Width : 3.855
Height : 10.033
Entry
ampl
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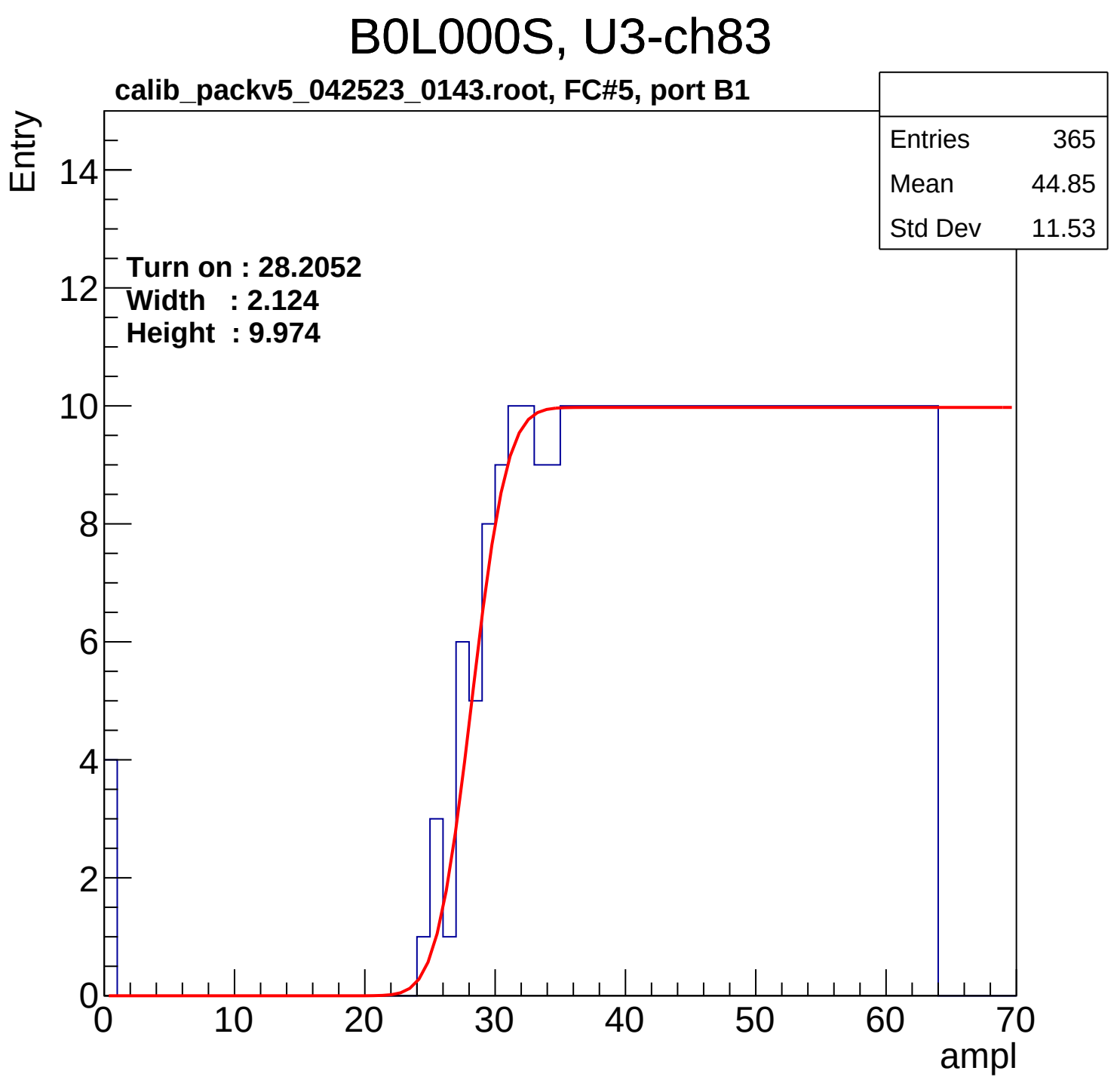
B0L000S, U3-ch83
calib_packv5_042523_0143.root, FC#5, port B1
Entries 365
Mean 44.85
Std Dev 11.53
Turn on : 28.2052
Width : 2.124
Height : 9.974
Entry
ampl
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6
8
10
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0
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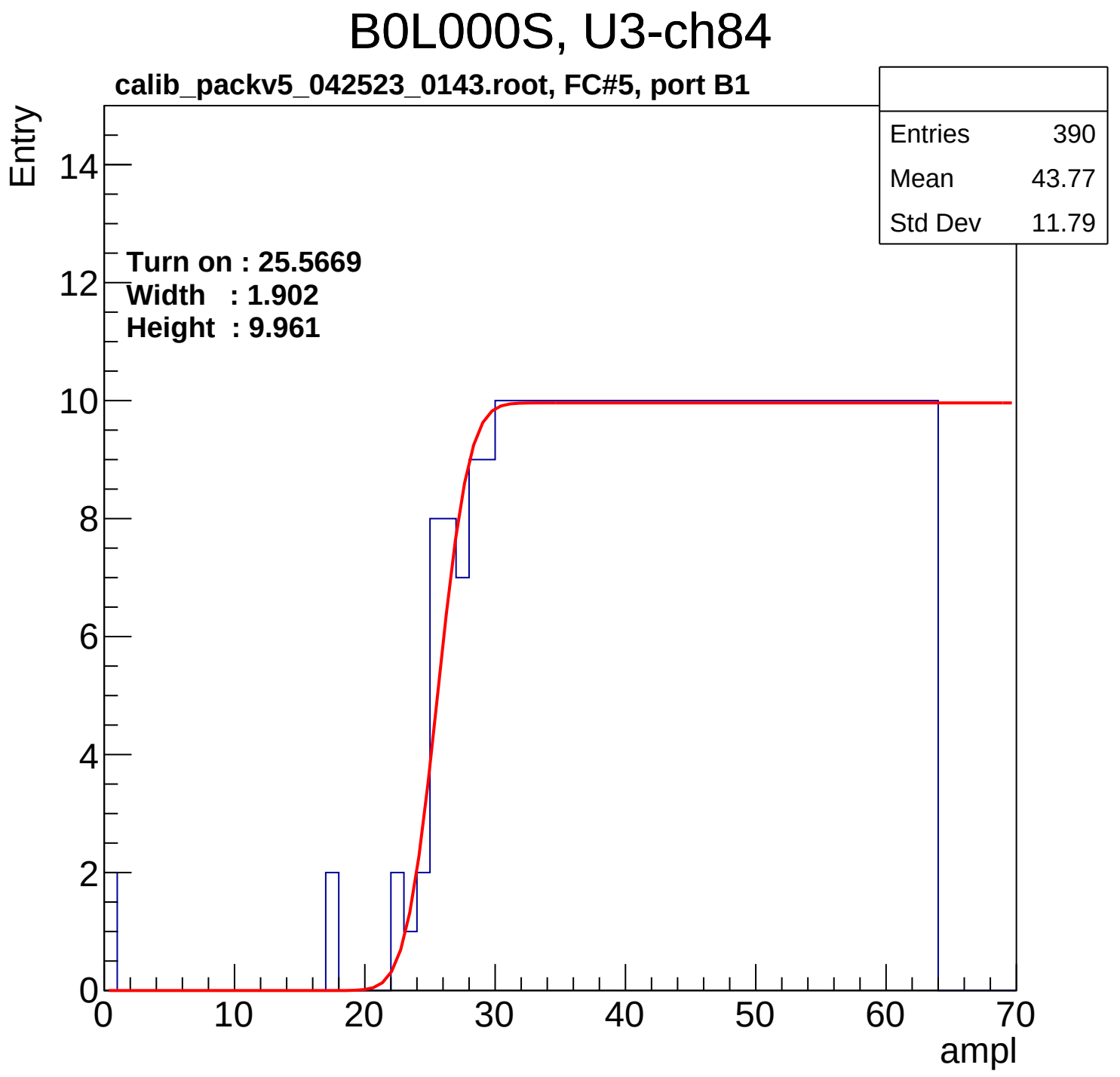
B0L000S, U3-ch84
calib_packv5_042523_0143.root, FC#5, port B1
Entries 390
Mean 43.77
Std Dev 11.79
Turn on : 25.5669
Width : 1.902
Height : 9.961
Entry
ampl
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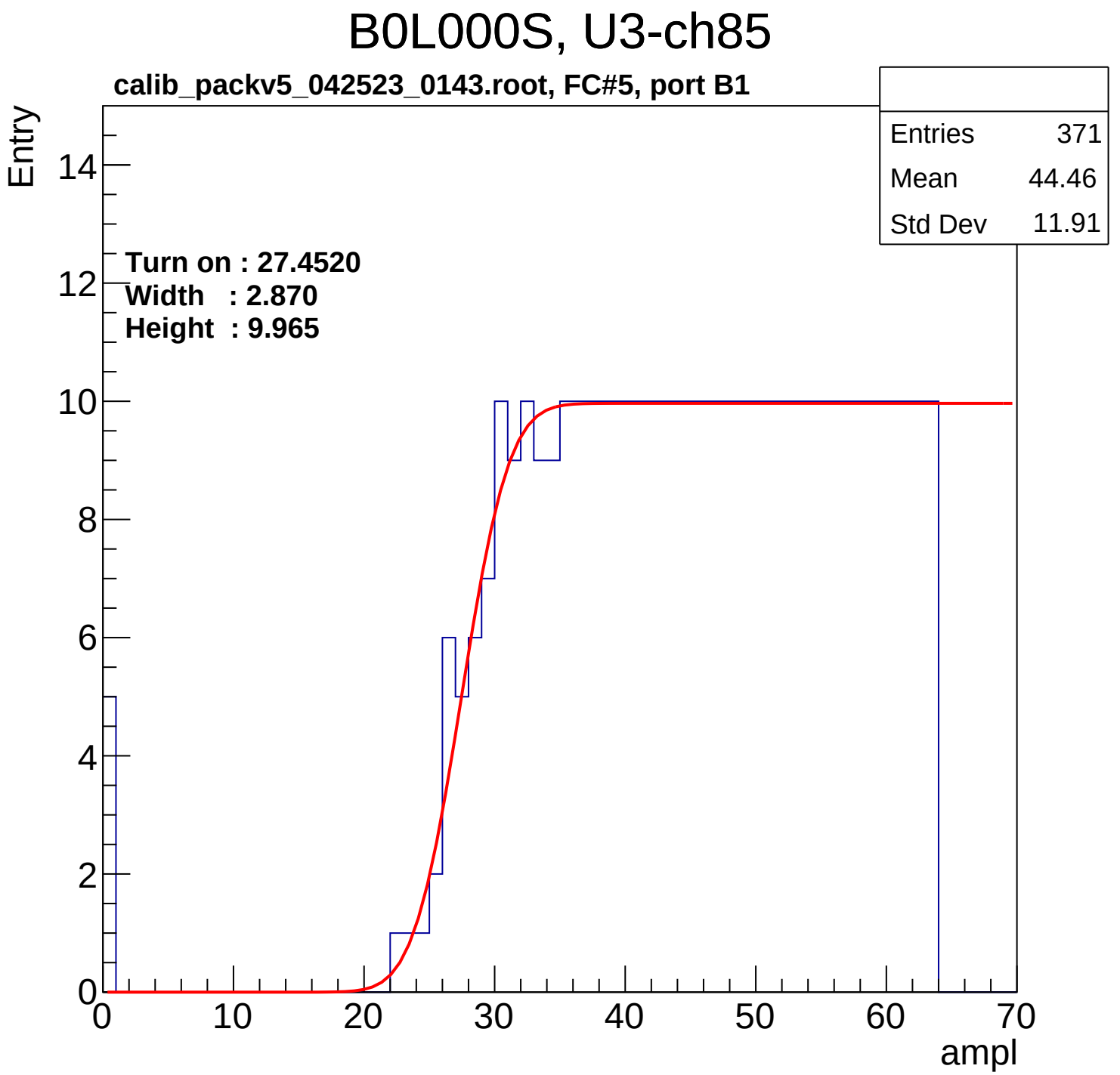
B0L000S, U3-ch85
calib_packv5_042523_0143.root, FC#5, port B1
Entries 371
Mean 44.46
Std Dev 11.91
Turn on : 27.4520
Width : 2.870
Height : 9.965
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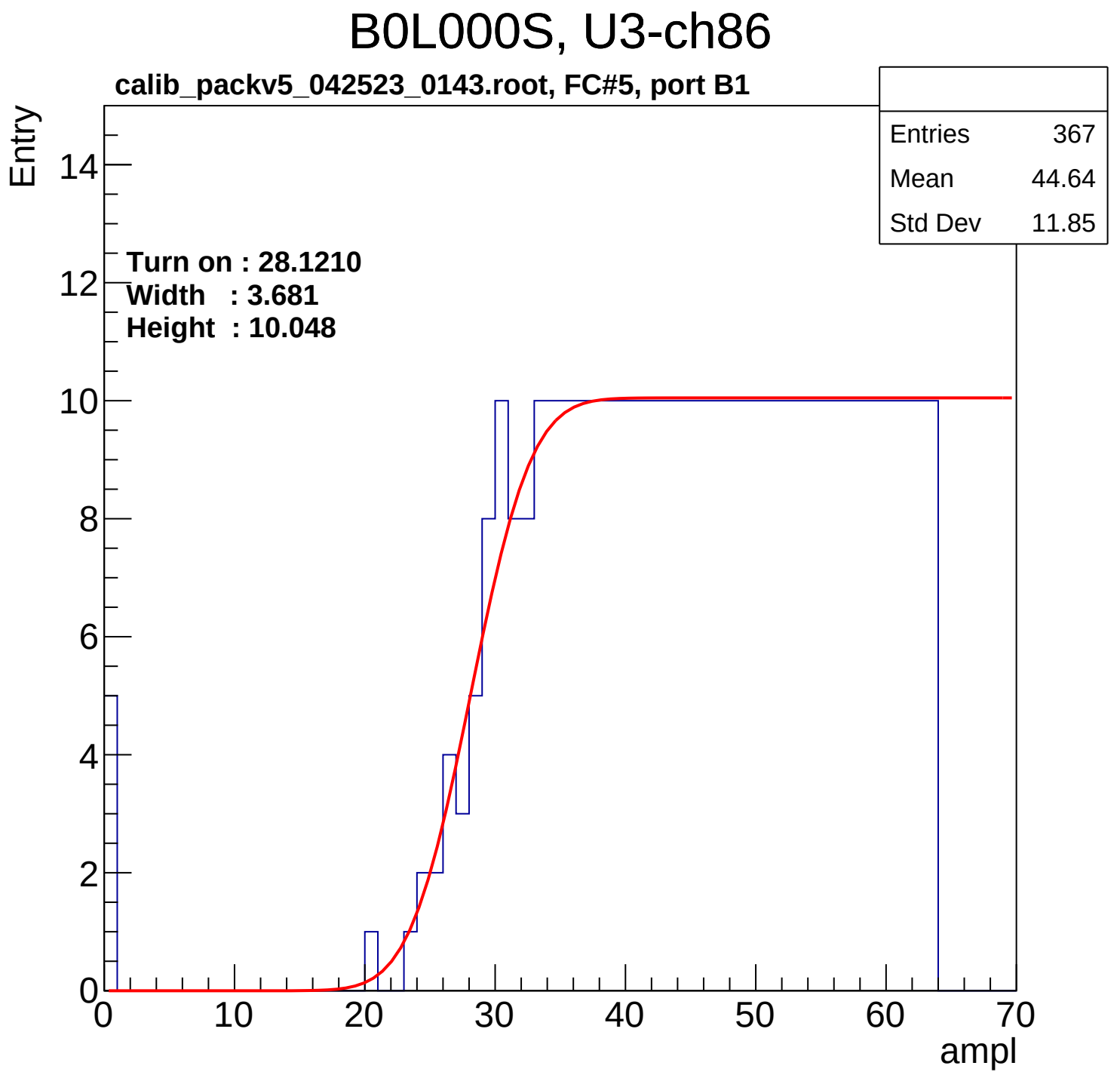
B0L000S, U3-ch86
calib_packv5_042523_0143.root, FC#5, port B1
Entries 367
Mean 44.64
Std Dev 11.85
Turn on : 28.1210
Width : 3.681
Height : 10.048
Entry
ampl
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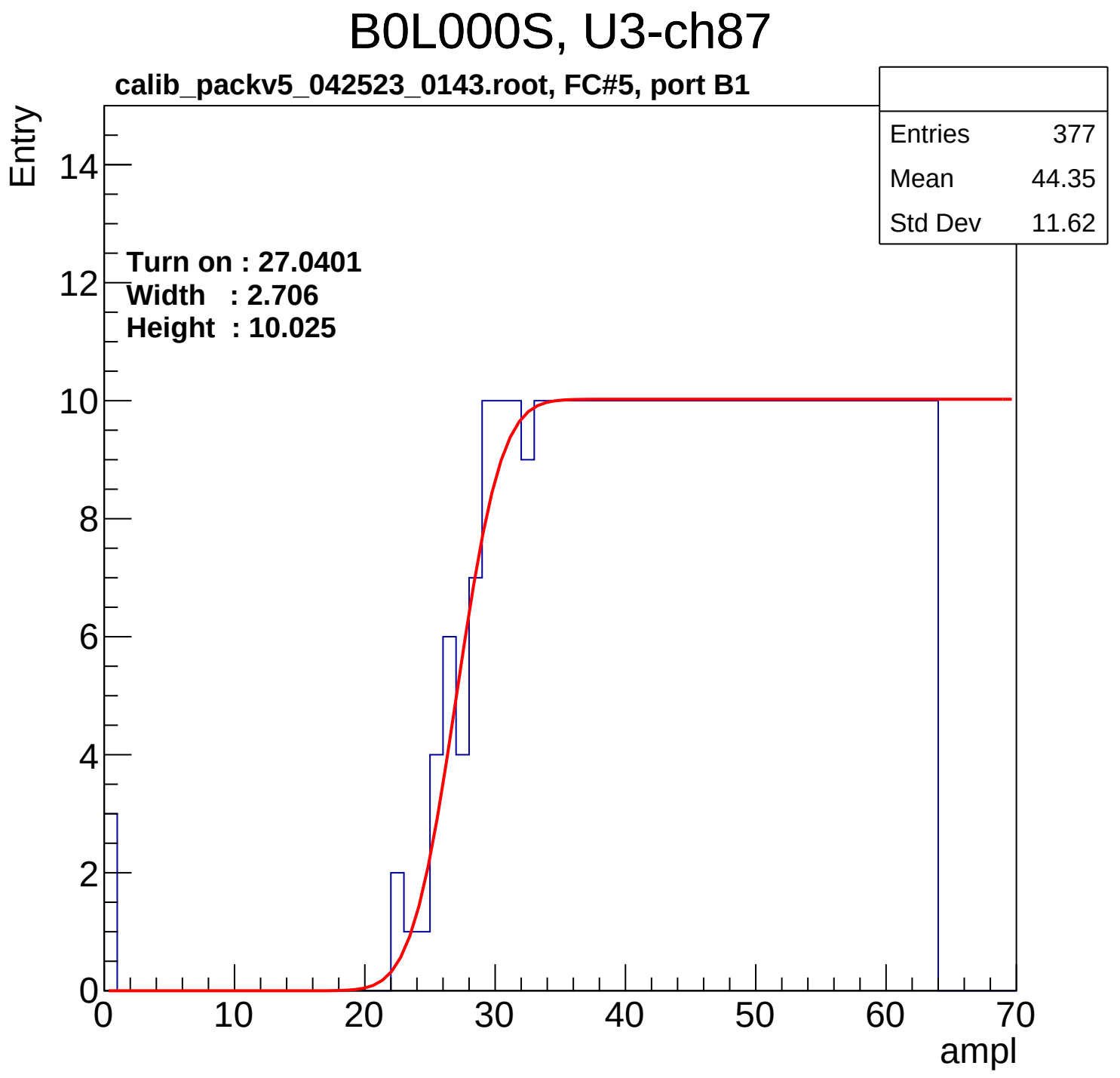
B0L000S, U3-ch87
calib_packv5_042523_0143.root, FC#5, port B1
Entries 377
Mean 44.35
Std Dev 11.62
Turn on : 27.0401
Width : 2.706
Height : 10.025
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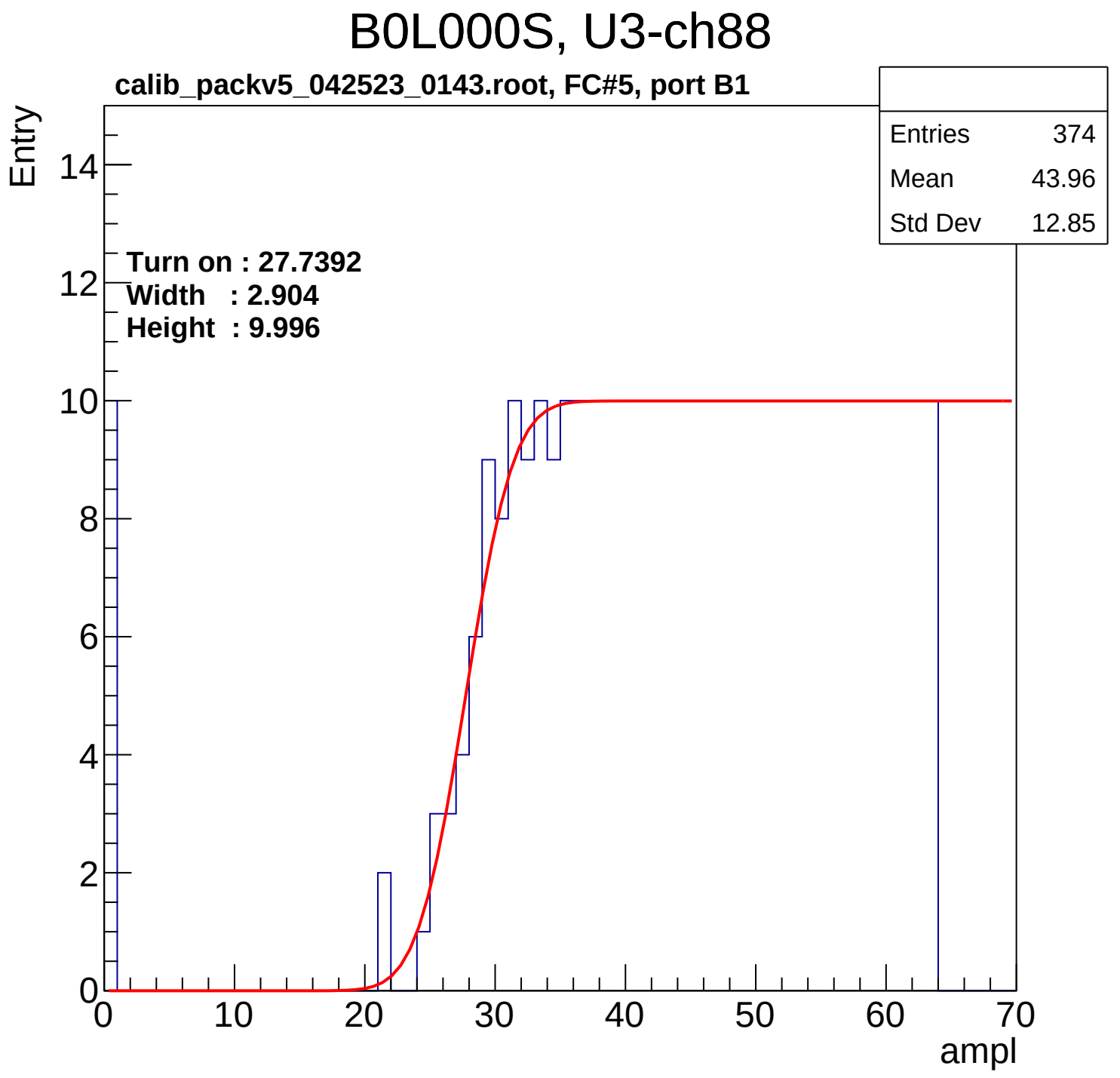
B0L000S, U3-ch88
calib_packv5_042523_0143.root, FC#5, port B1
Entries 374
Mean 43.96
Std Dev 12.85
Turn on : 27.7392
Width : 2.904
Height : 9.996
Entry
ampl
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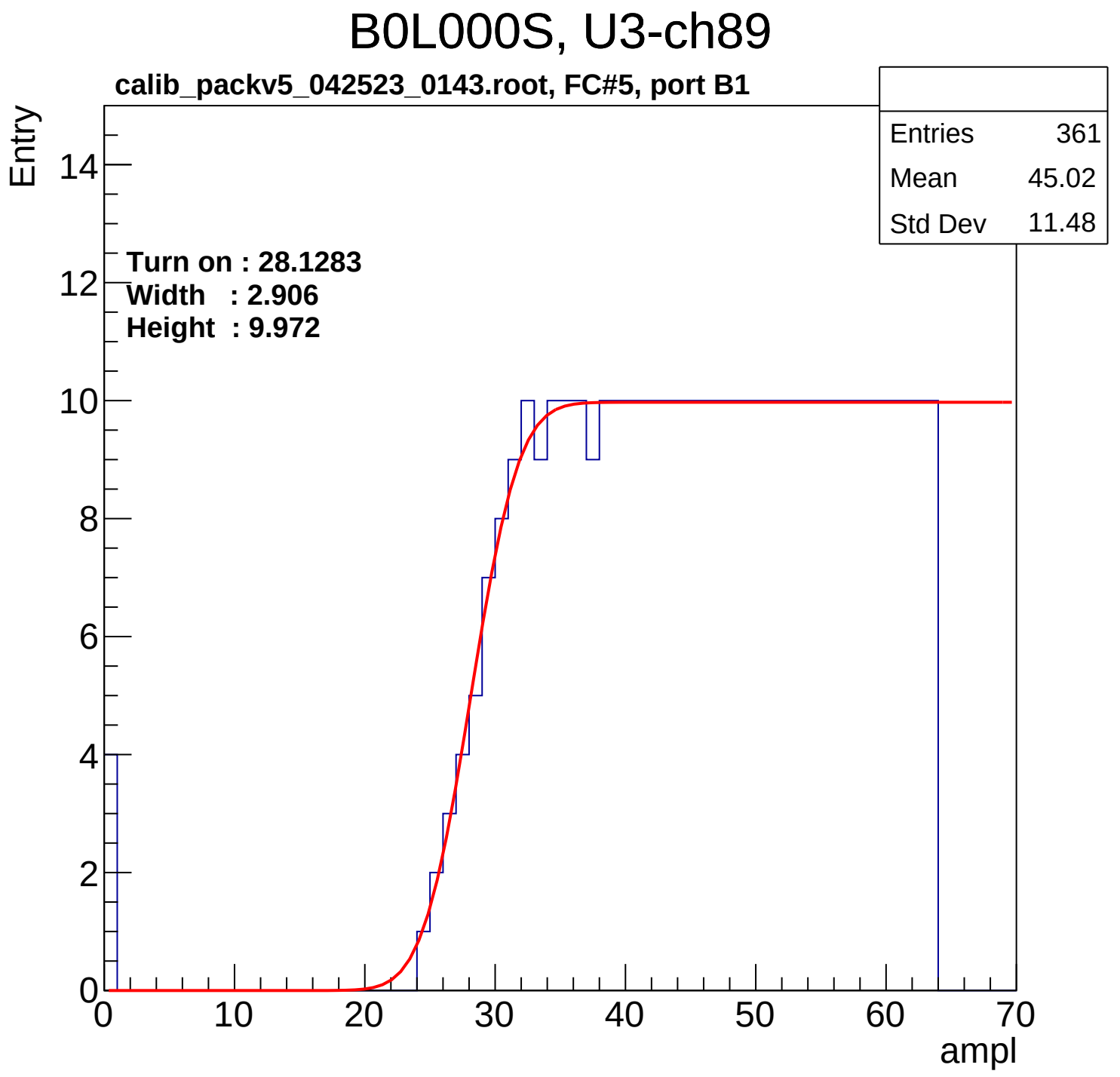
B0L000S, U3-ch89
calib_packv5_042523_0143.root, FC#5, port B1
Entries 361
Mean 45.02
Std Dev 11.48
Turn on : 28.1283
Width : 2.906
Height : 9.972
Entry
ampl
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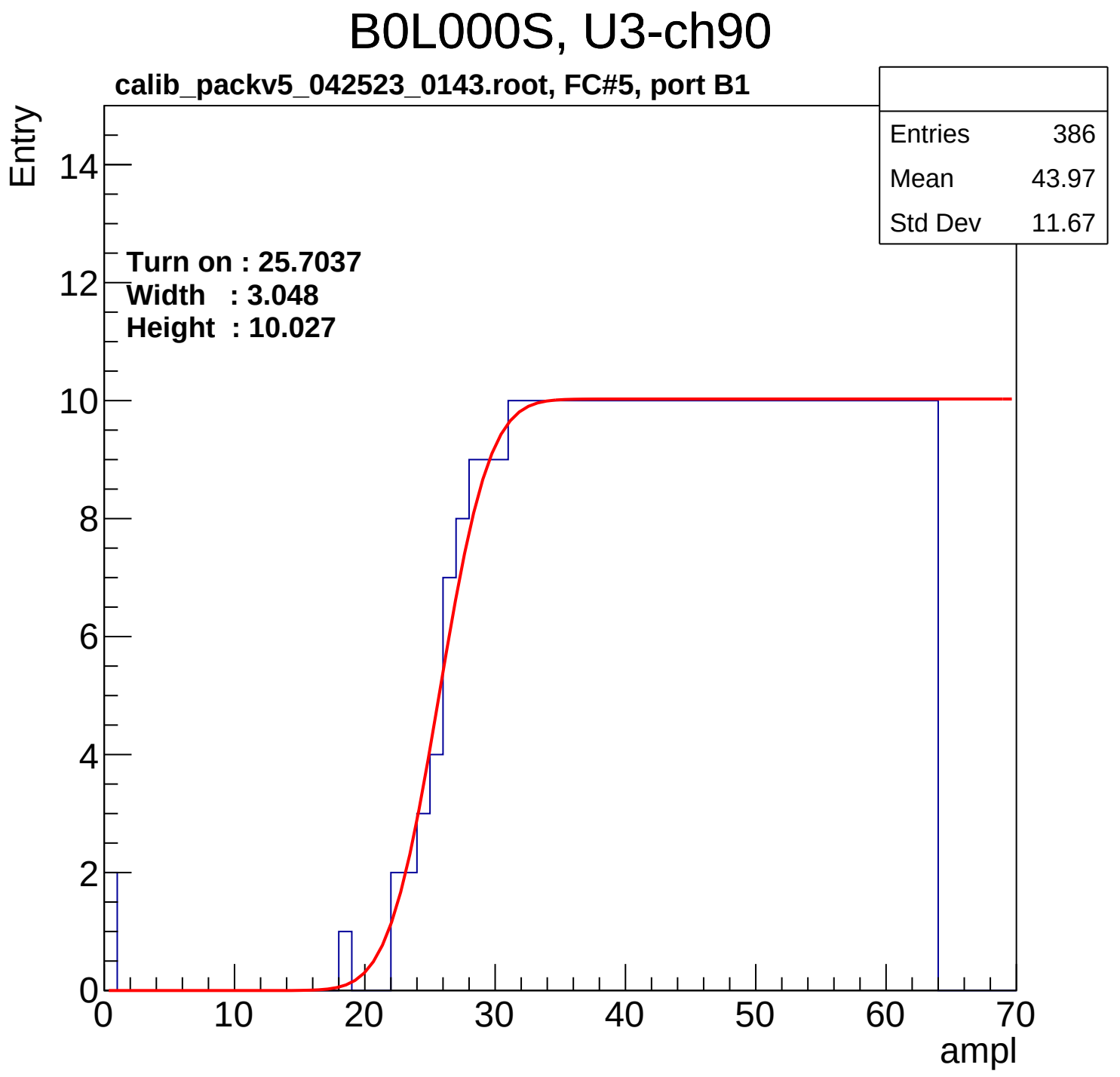
B0L000S, U3-ch90
calib_packv5_042523_0143.root, FC#5, port B1
Entries 386
Mean 43.97
Std Dev 11.67
Turn on : 25.7037
Width : 3.048
Height : 10.027
Entry
ampl
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8
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0
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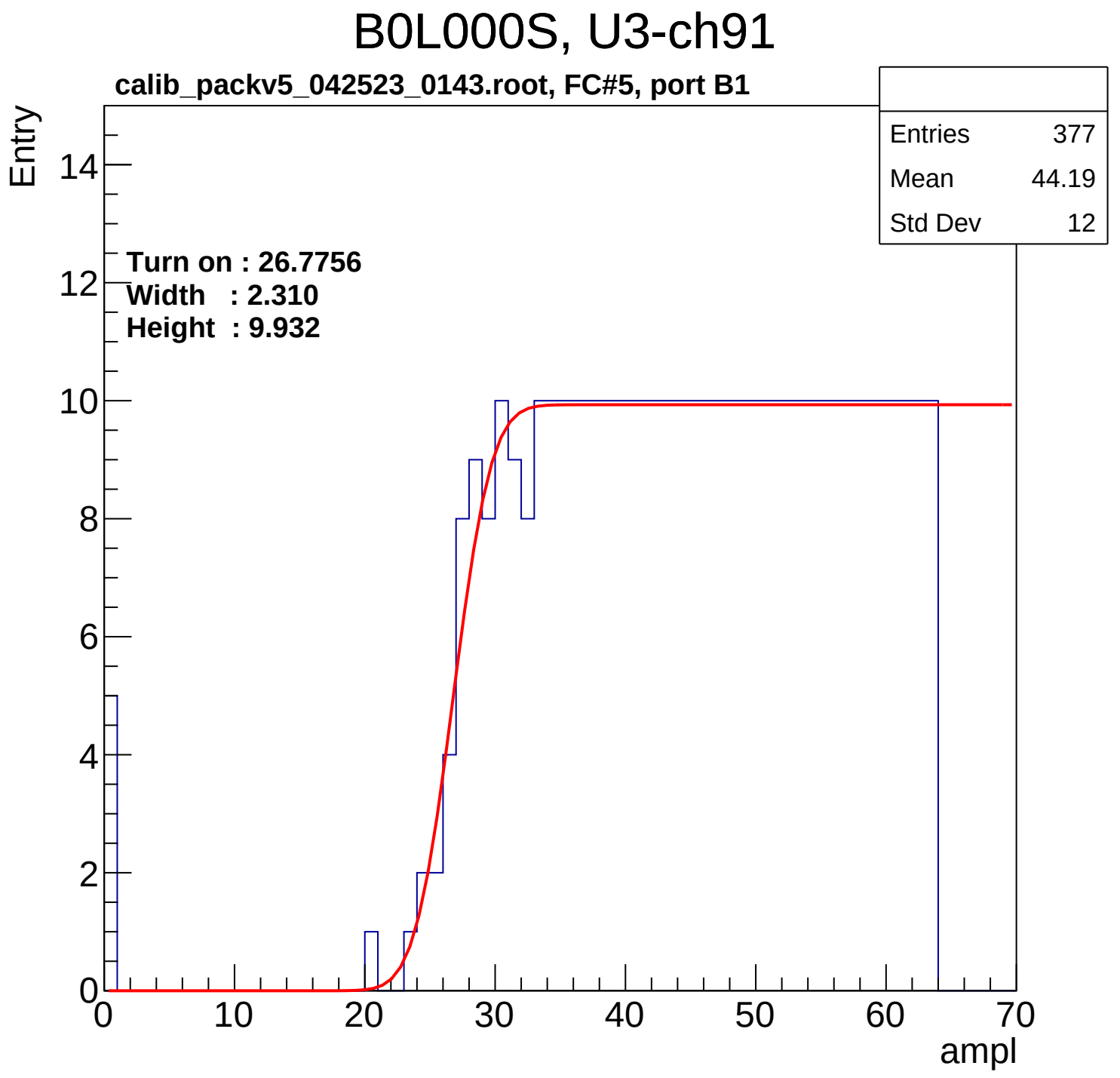
B0L000S, U3-ch91
calib_packv5_042523_0143.root, FC#5, port B1
Entries 377
Mean 44.19
Std Dev 12
Turn on : 26.7756
Width : 2.310
Height : 9.932
Entry
ampl
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2
4
6
8
10
12
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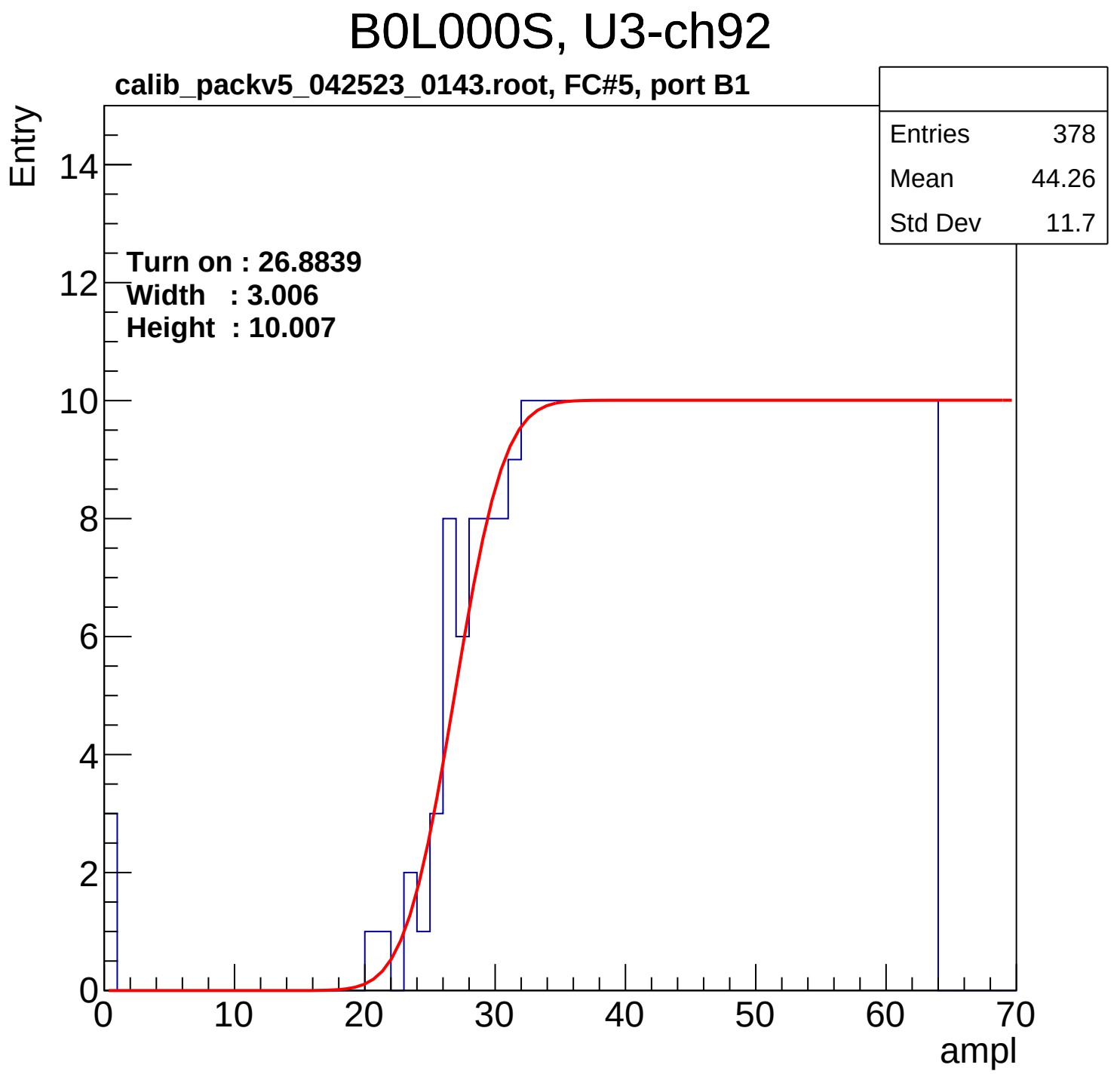
B0L000S, U3-ch92
calib_packv5_042523_0143.root, FC#5, port B1
Entries 378
Mean 44.26
Std Dev 11.7
Turn on : 26.8839
Width : 3.006
Height : 10.007
Entry
ampl
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2
4
6
8
10
12
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0
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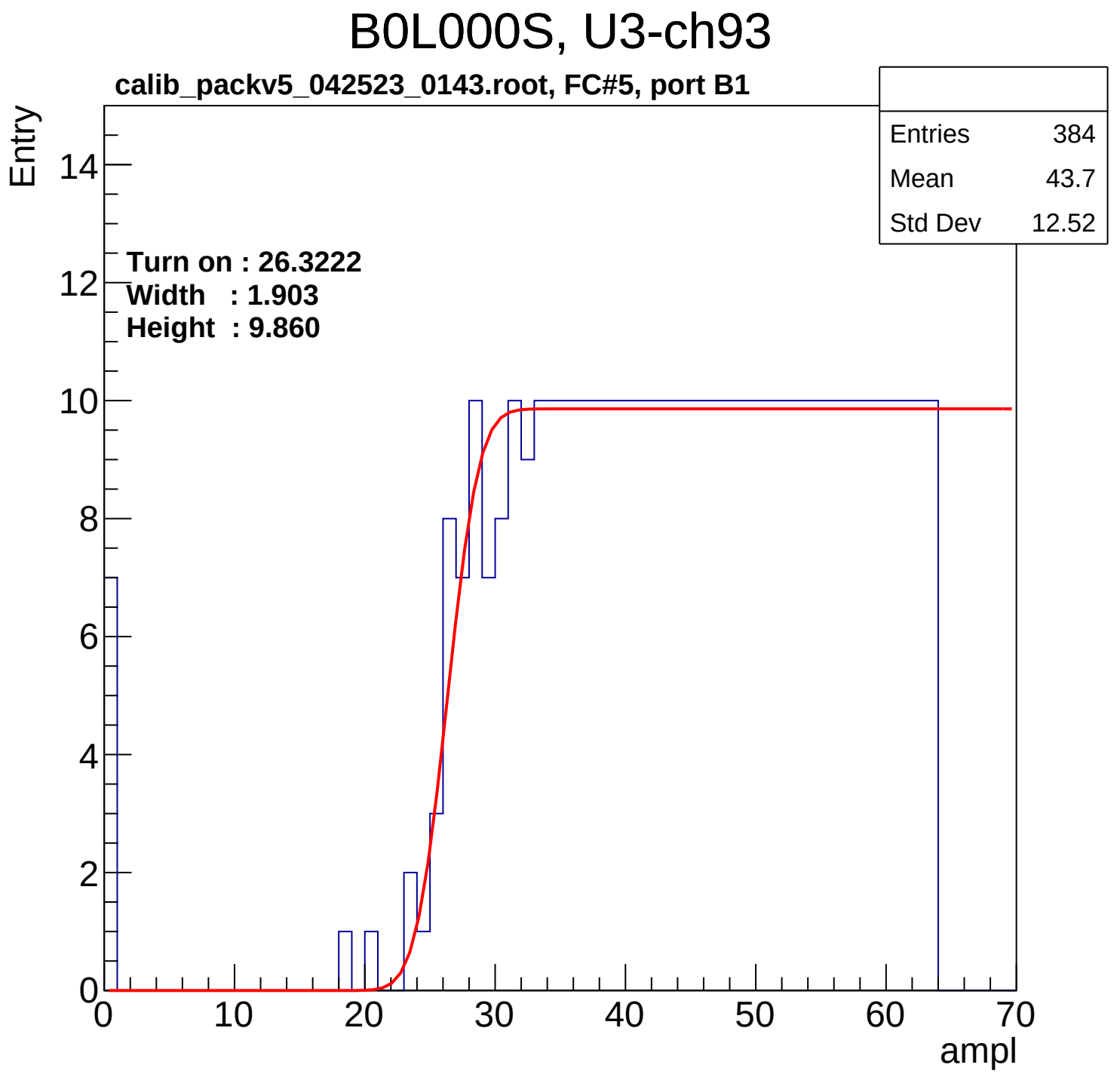
B0L000S, U3-ch93
calib_packv5_042523_0143.root, FC#5, port B1
Entries 384
Mean 43.7
Std Dev 12.52
Turn on : 26.3222
Width : 1.903
Height : 9.860
Entry
ampl
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6
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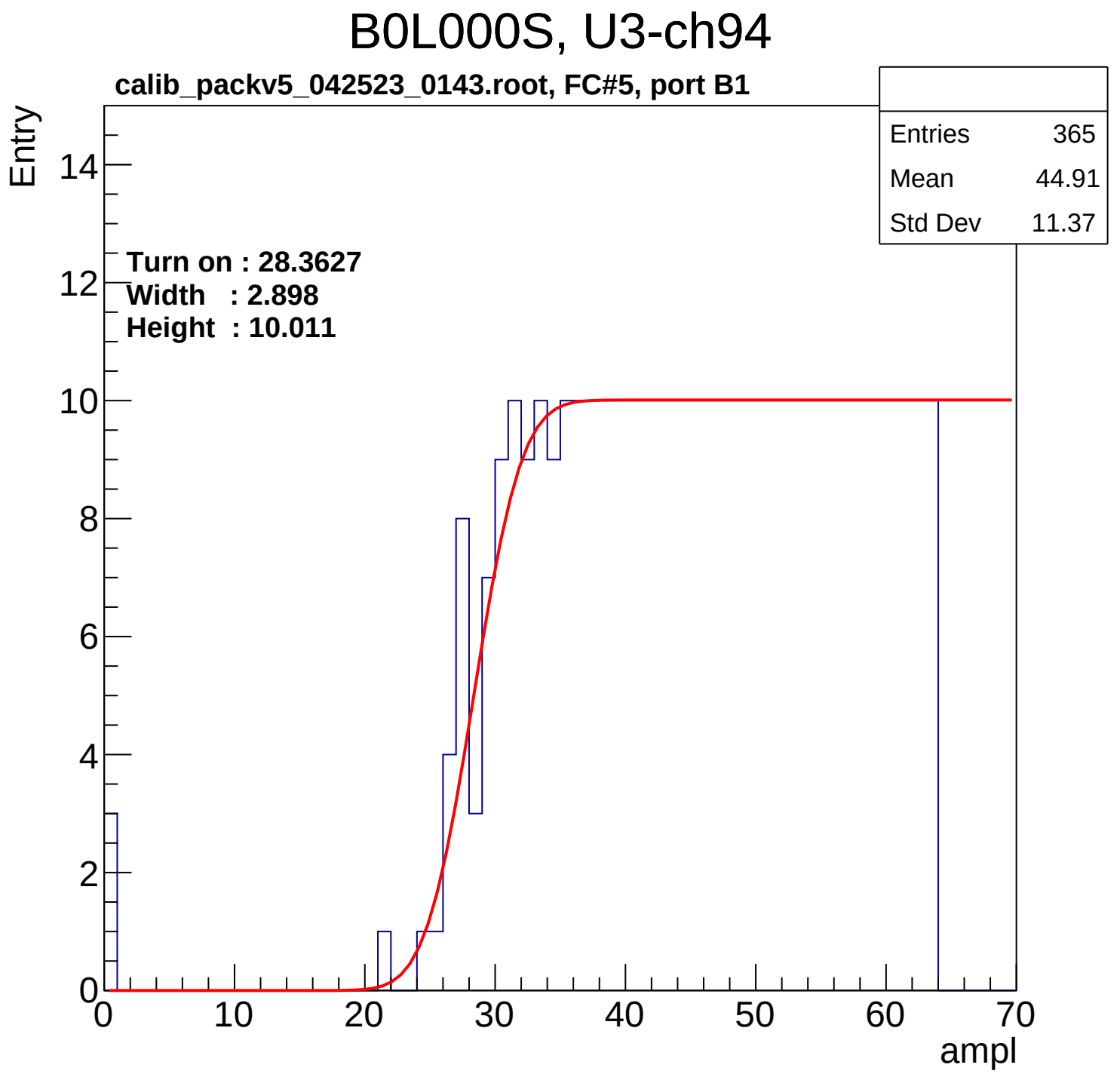
B0L000S, U3-ch94
calib_packv5_042523_0143.root, FC#5, port B1
Entries 365
Mean 44.91
Std Dev 11.37
Turn on : 28.3627
Width : 2.898
Height : 10.011
Entry
ampl
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2
4
6
8
10
12
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0
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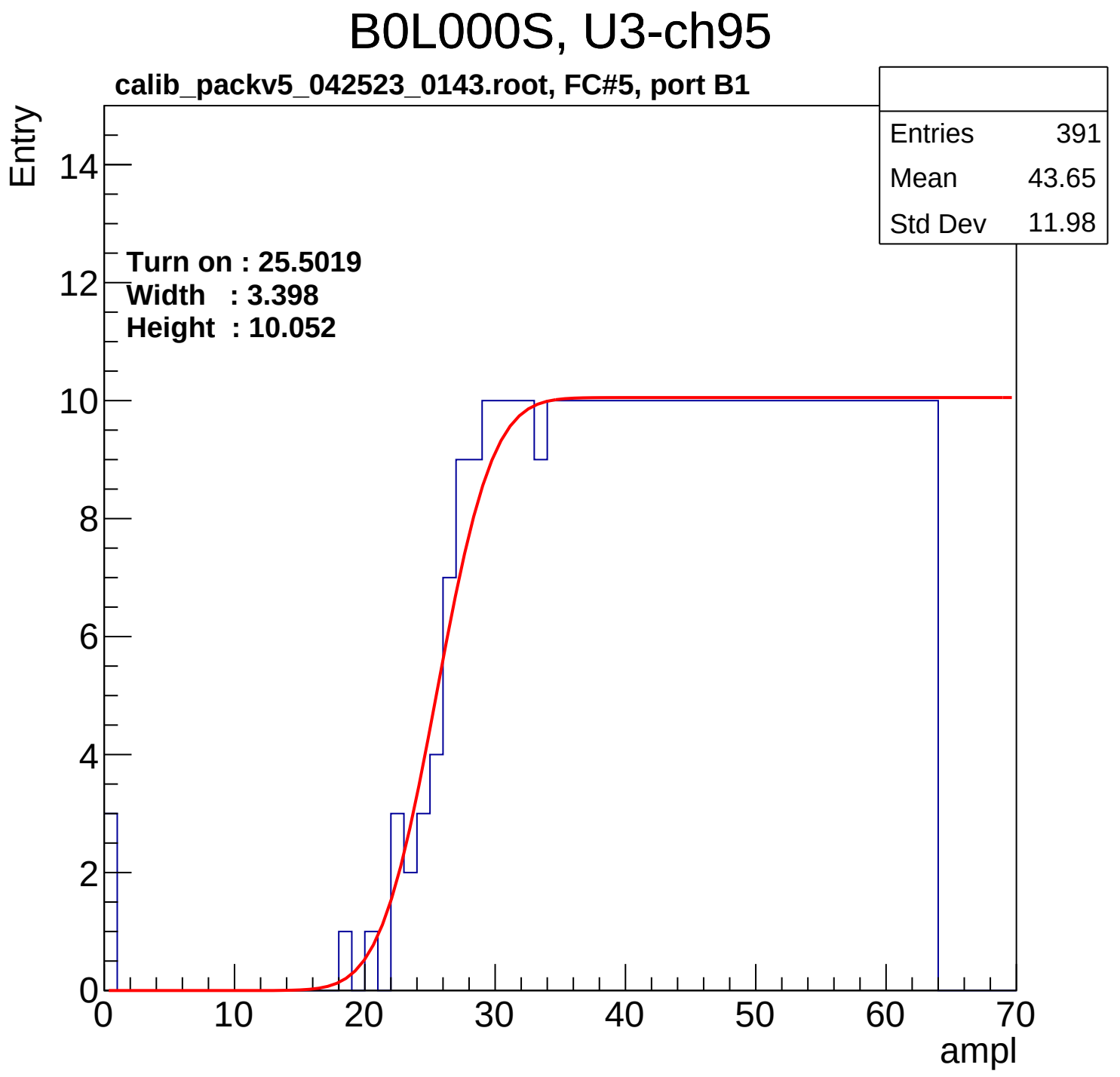
B0L000S, U3-ch95
calib_packv5_042523_0143.root, FC#5, port B1
Entries 391
Mean 43.65
Std Dev 11.98
Turn on : 25.5019
Width : 3.398
Height : 10.052
Entry
ampl
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4
6
8
10
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0
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60
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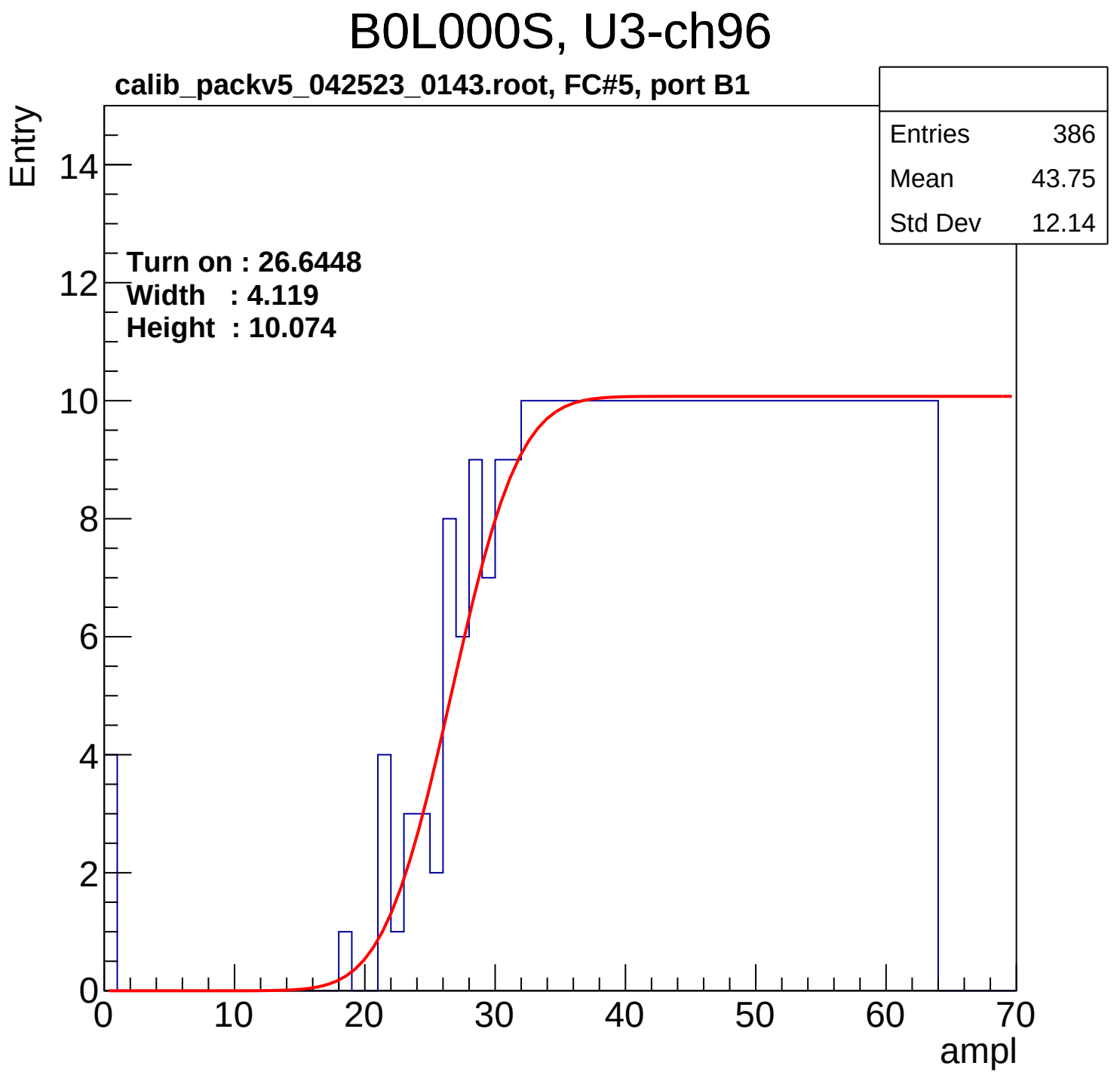
B0L000S, U3-ch96
calib_packv5_042523_0143.root, FC#5, port B1
Entries 386
Mean 43.75
Std Dev 12.14
Turn on : 26.6448
Width : 4.119
Height : 10.074
Entry
ampl
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6
8
10
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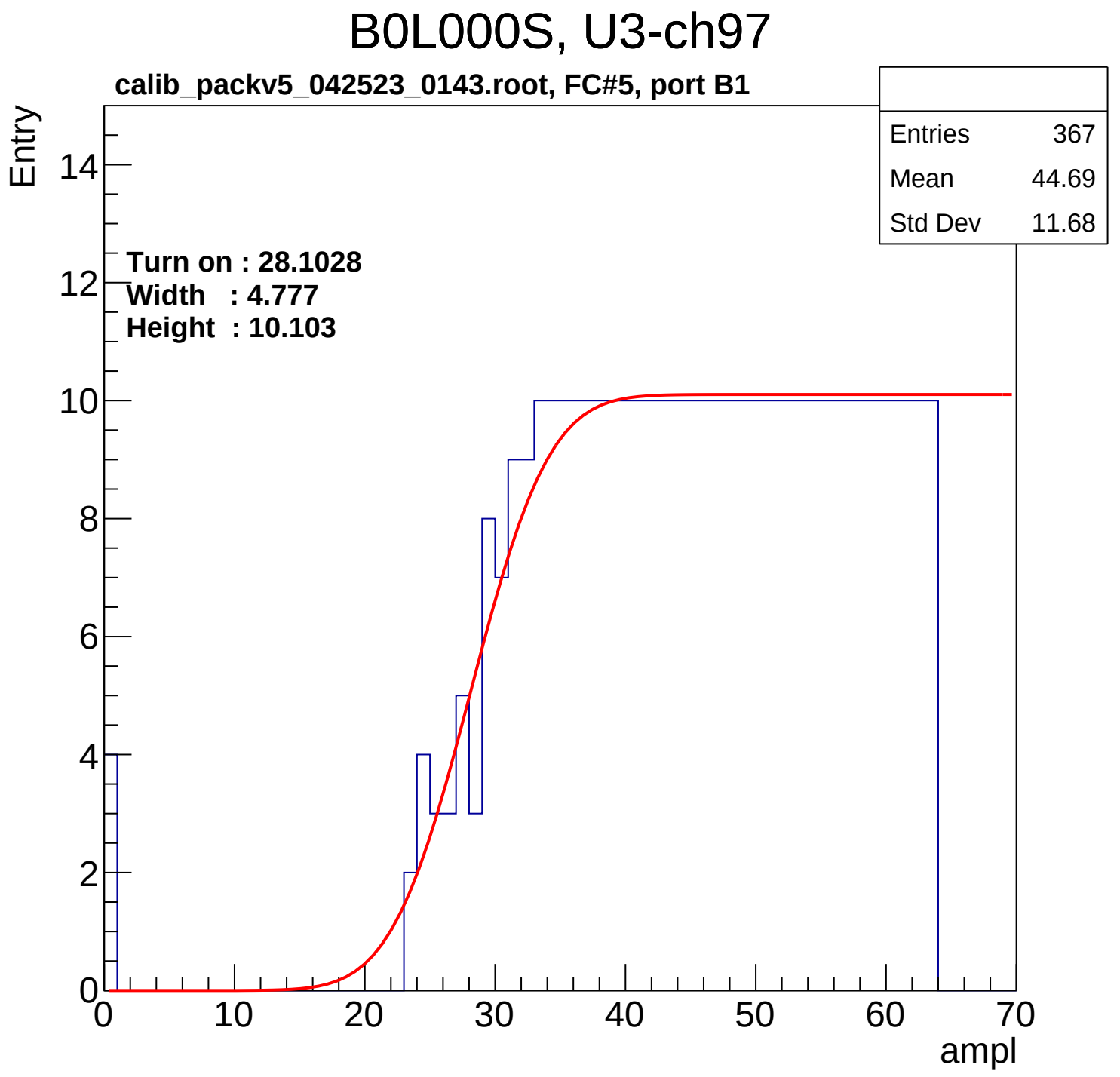
B0L000S, U3-ch97
calib_packv5_042523_0143.root, FC#5, port B1
Entries 367
Mean 44.69
Std Dev 11.68
Turn on : 28.1028
Width : 4.777
Height : 10.103
Entry
ampl
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8
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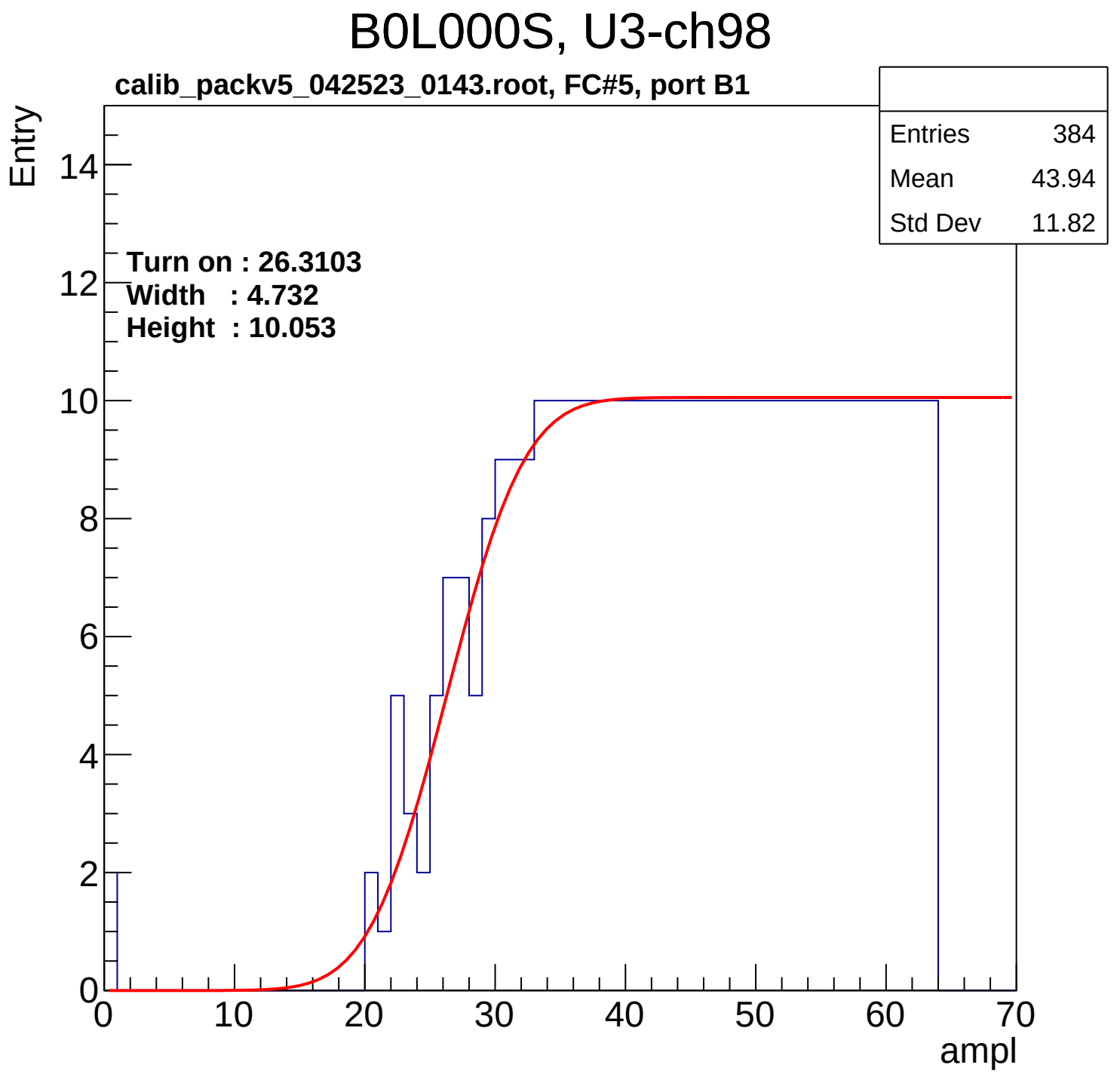
B0L000S, U3-ch98
calib_packv5_042523_0143.root, FC#5, port B1
Entries 384
Mean 43.94
Std Dev 11.82
Turn on : 26.3103
Width : 4.732
Height : 10.053
Entry
ampl
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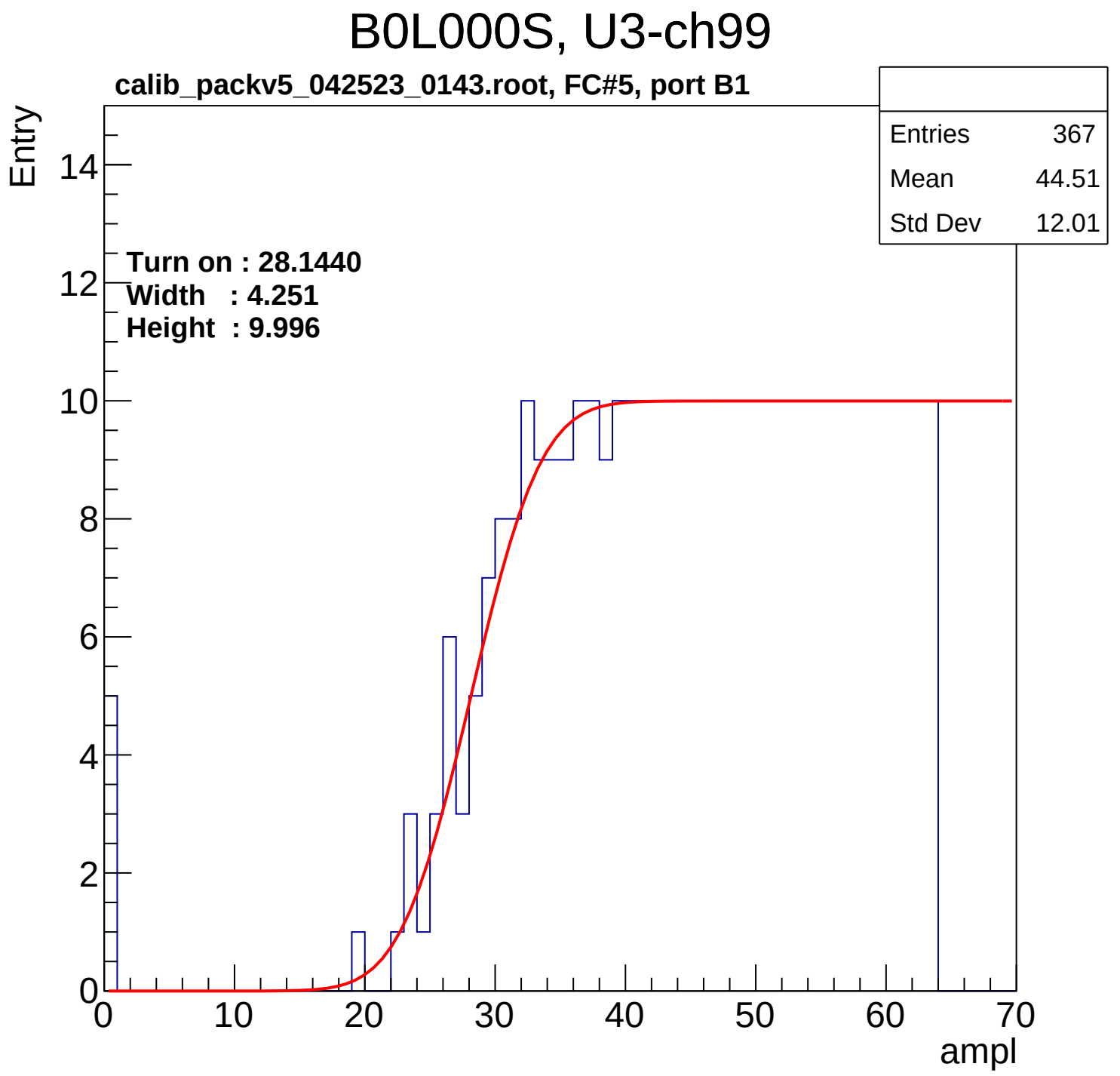
B0L000S, U3-ch99
calib_packv5_042523_0143.root, FC#5, port B1
Entries 367
Mean 44.51
Std Dev 12.01
Turn on : 28.1440
Width : 4.251
Height : 9.996
Entry
ampl
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4
6
8
10
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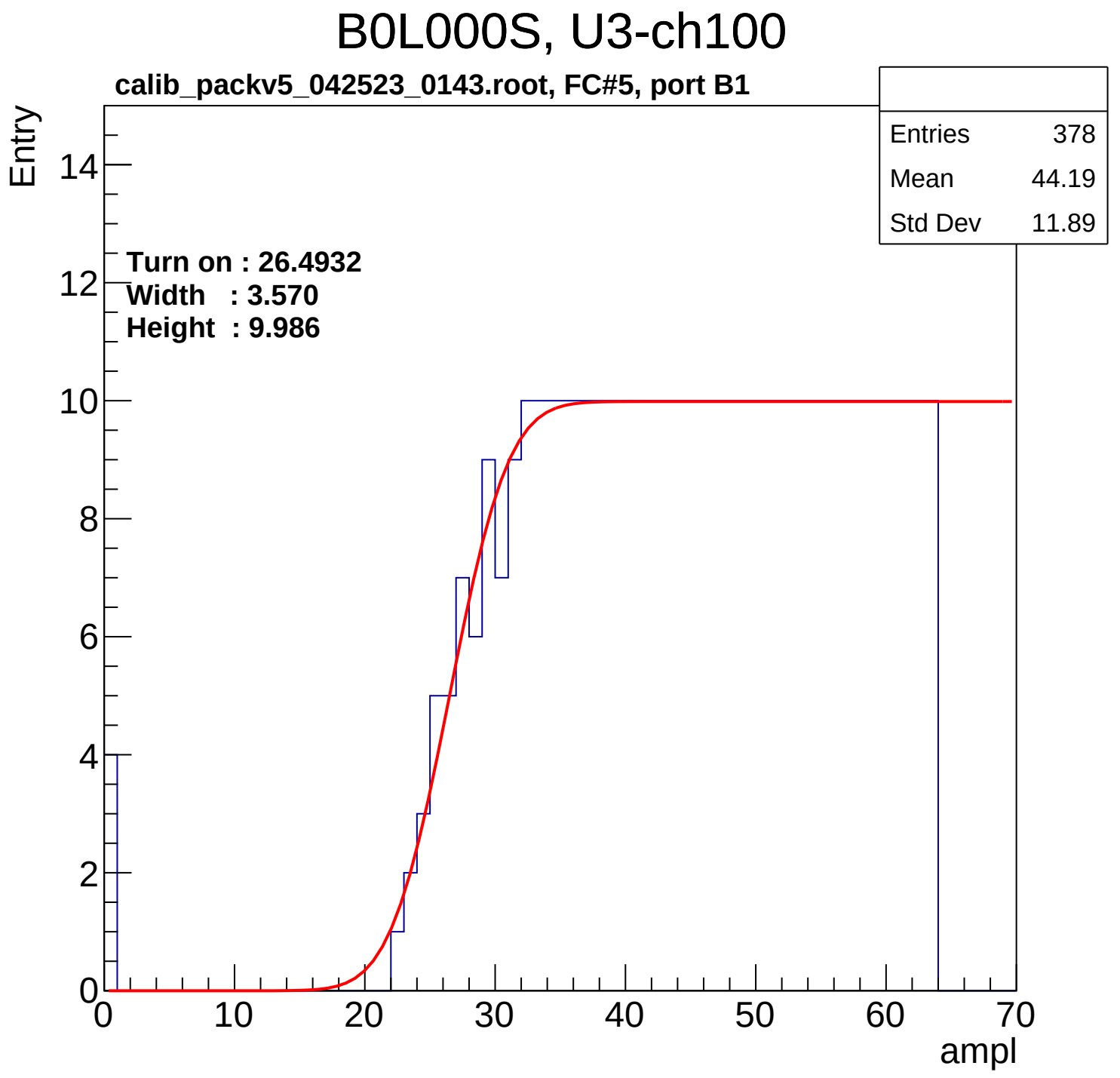
B0L000S, U3-ch100
calib_packv5_042523_0143.root, FC#5, port B1
Entries 378
Mean 44.19
Std Dev 11.89
Turn on : 26.4932
Width : 3.570
Height : 9.986
Entry
ampl
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4
6
8
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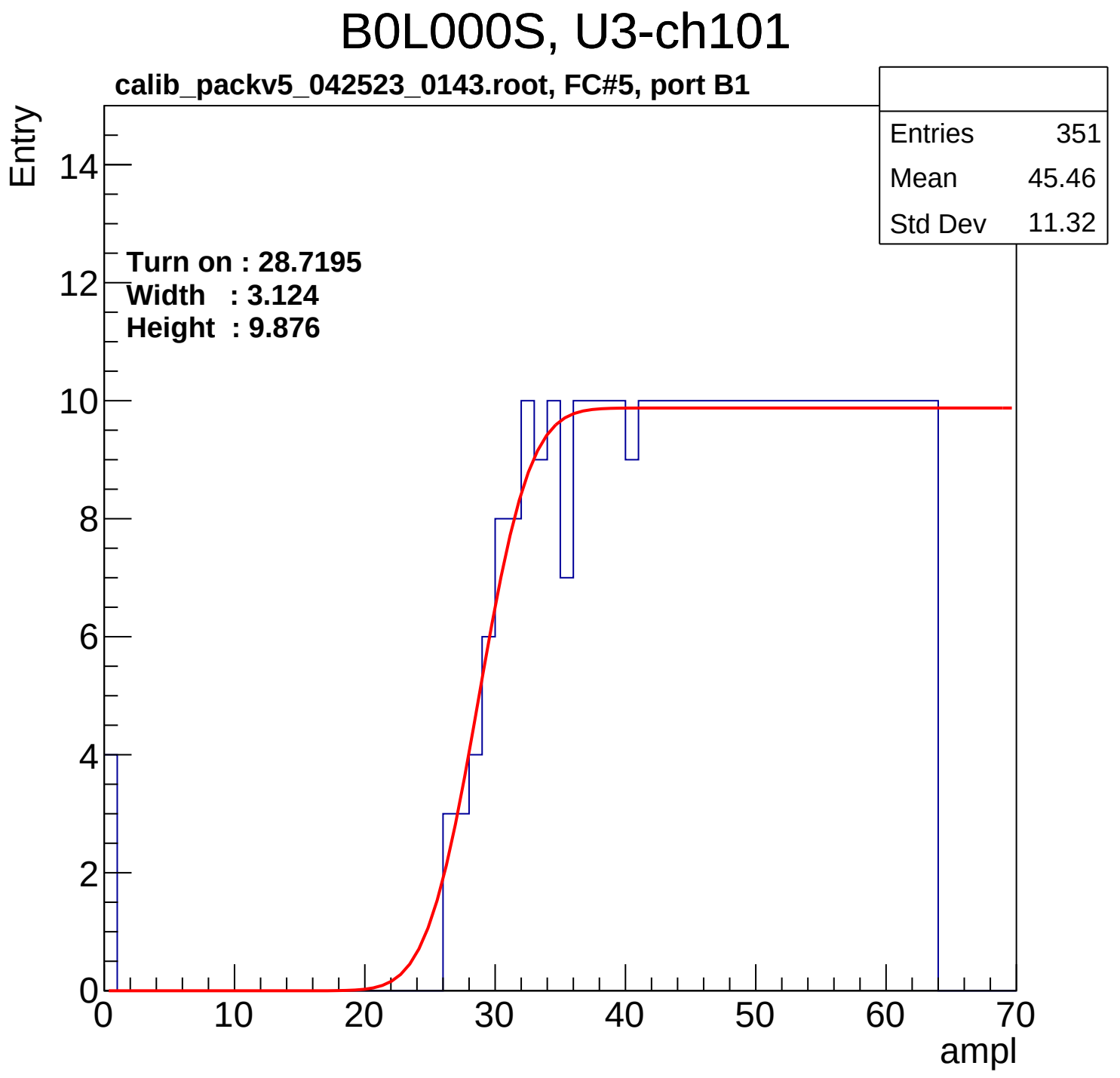
B0L000S, U3-ch101
calib_packv5_042523_0143.root, FC#5, port B1
Entries 351
Mean 45.46
Std Dev 11.32
Turn on : 28.7195
Width : 3.124
Height : 9.876
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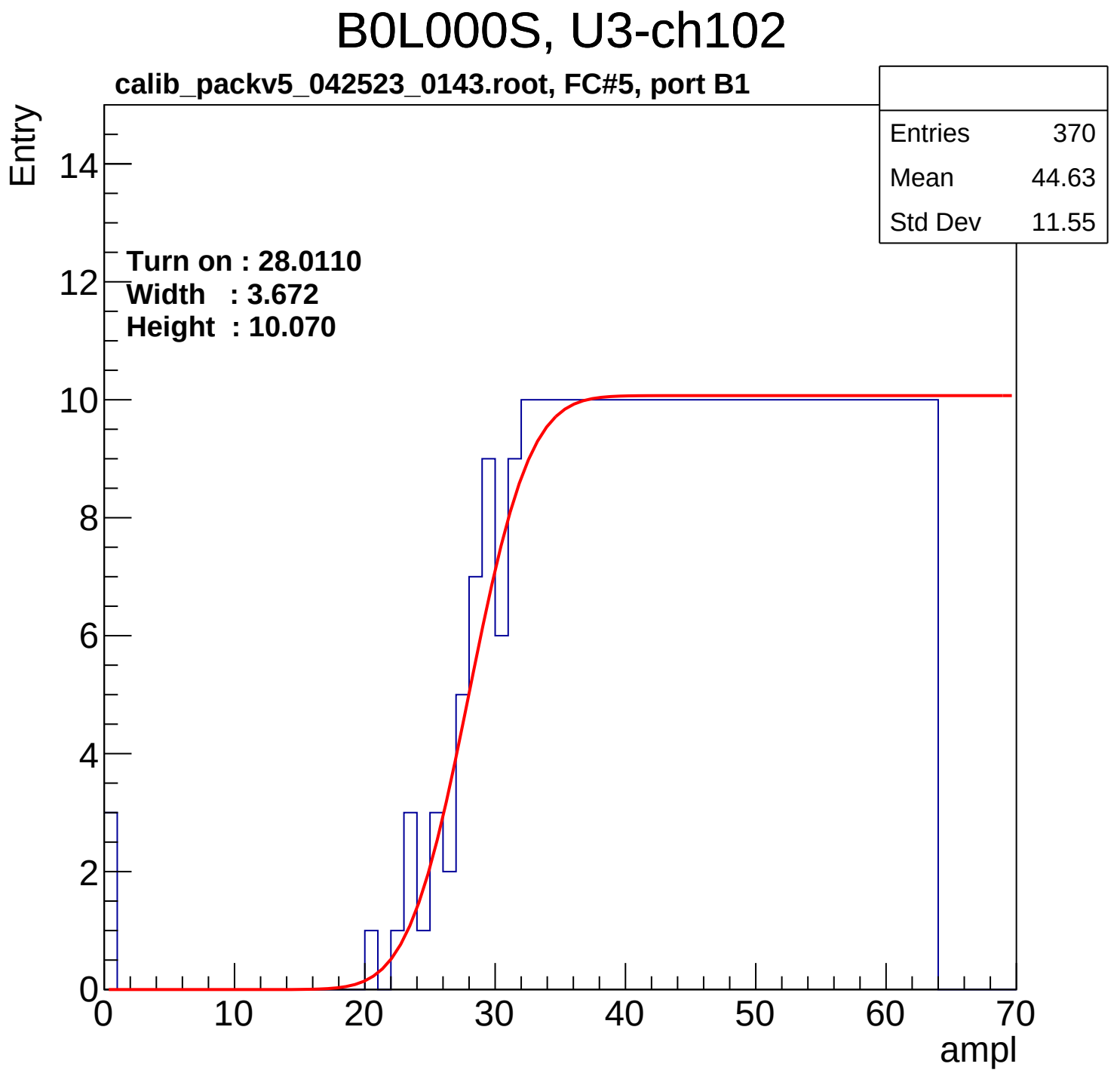
B0L000S, U3-ch102
calib_packv5_042523_0143.root, FC#5, port B1
Entries 370
Mean 44.63
Std Dev 11.55
Turn on : 28.0110
Width : 3.672
Height : 10.070
Entry
ampl
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8
10
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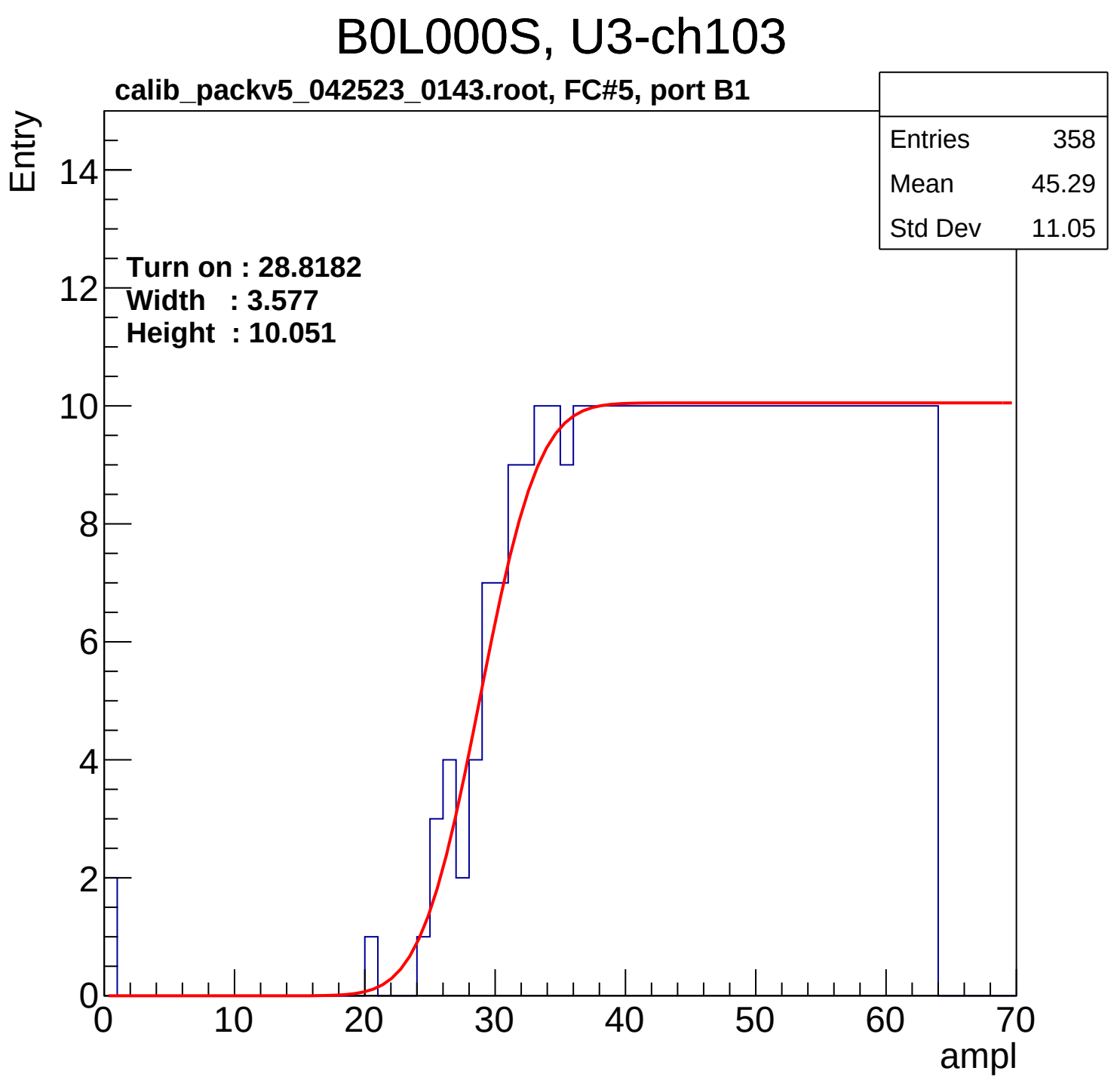
B0L000S, U3-ch103
calib_packv5_042523_0143.root, FC#5, port B1
Entries 358
Mean 45.29
Std Dev 11.05
Turn on : 28.8182
Width : 3.577
Height : 10.051
Entry
ampl
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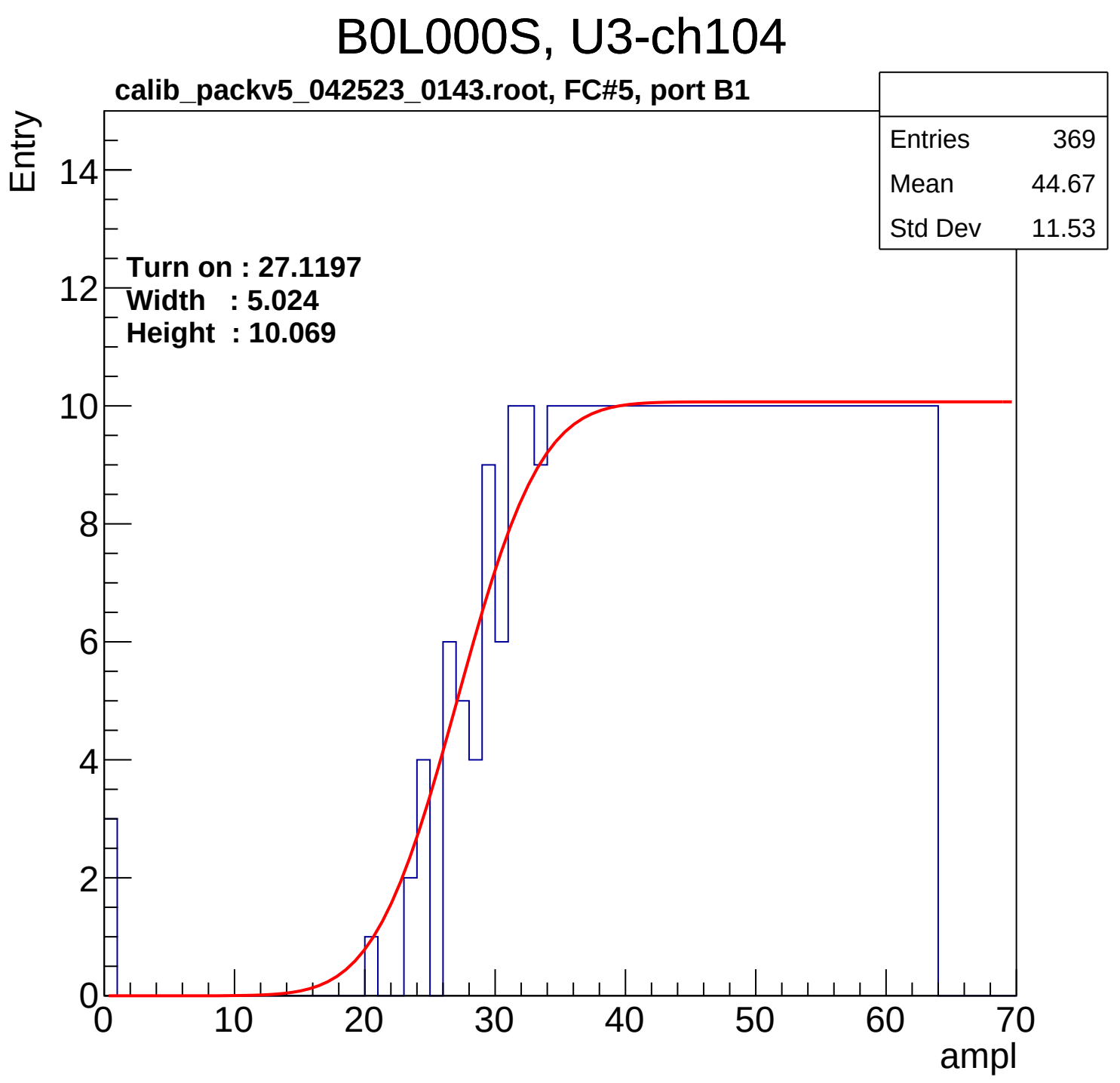
B0L000S, U3-ch104
calib_packv5_042523_0143.root, FC#5, port B1
Entries 369
Mean 44.67
Std Dev 11.53
Turn on : 27.1197
Width : 5.024
Height : 10.069
Entry
ampl
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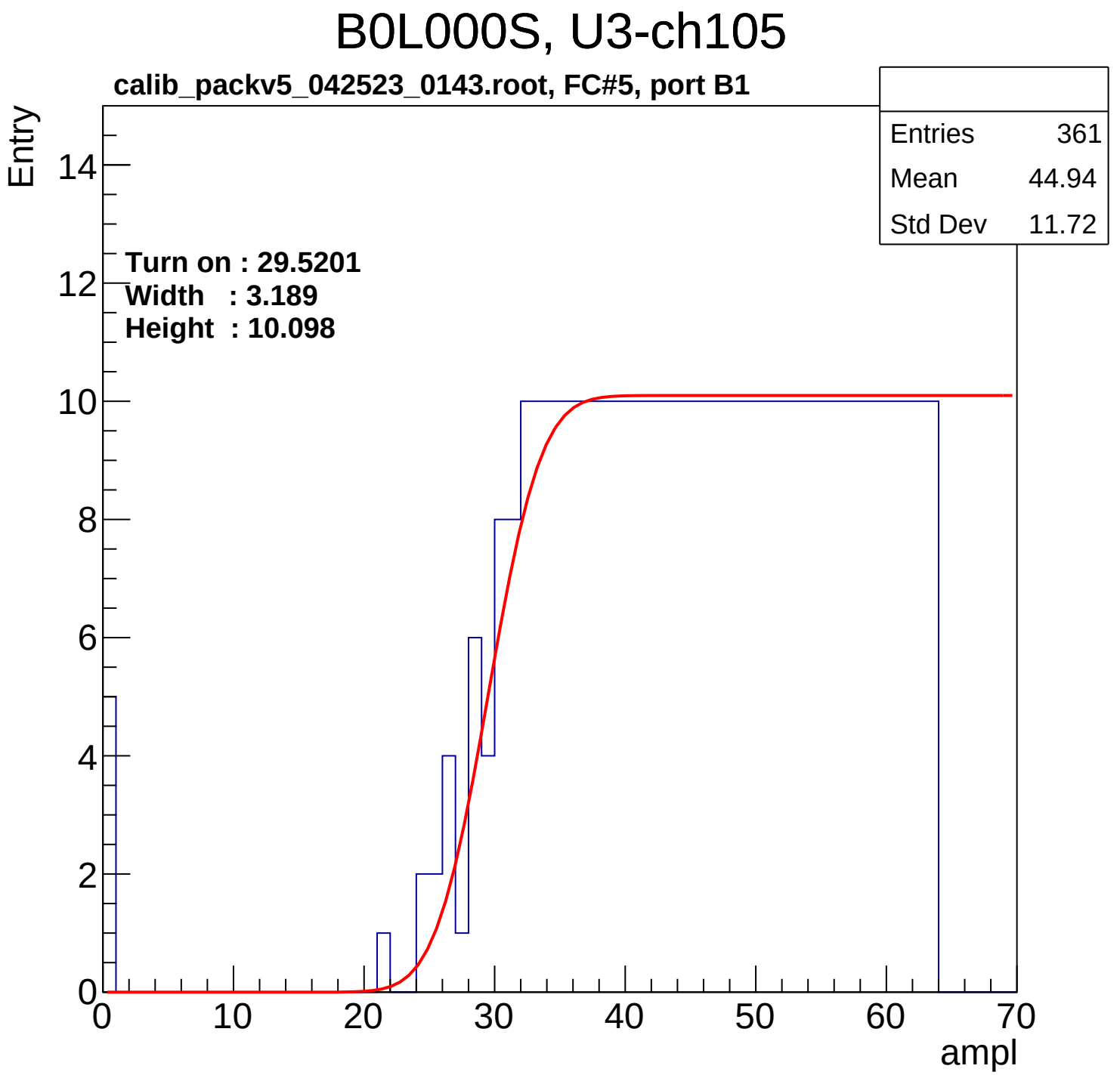
B0L000S, U3-ch105
calib_packv5_042523_0143.root, FC#5, port B1
Entries 361
Mean 44.94
Std Dev 11.72
Turn on : 29.5201
Width : 3.189
Height : 10.098
Entry
ampl
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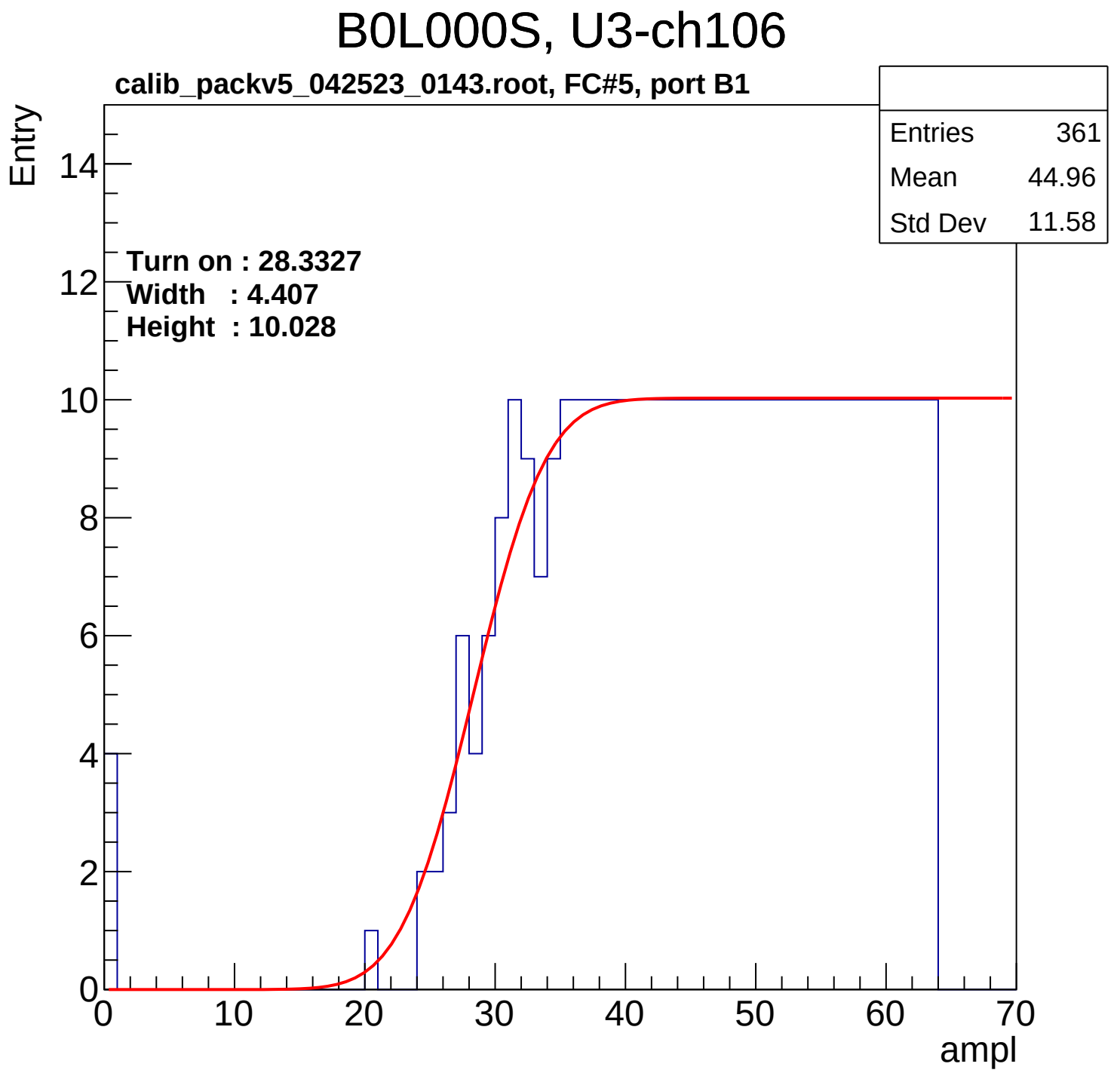
B0L000S, U3-ch106
calib_packv5_042523_0143.root, FC#5, port B1
Entries 361
Mean 44.96
Std Dev 11.58
Turn on : 28.3327
Width : 4.407
Height : 10.028
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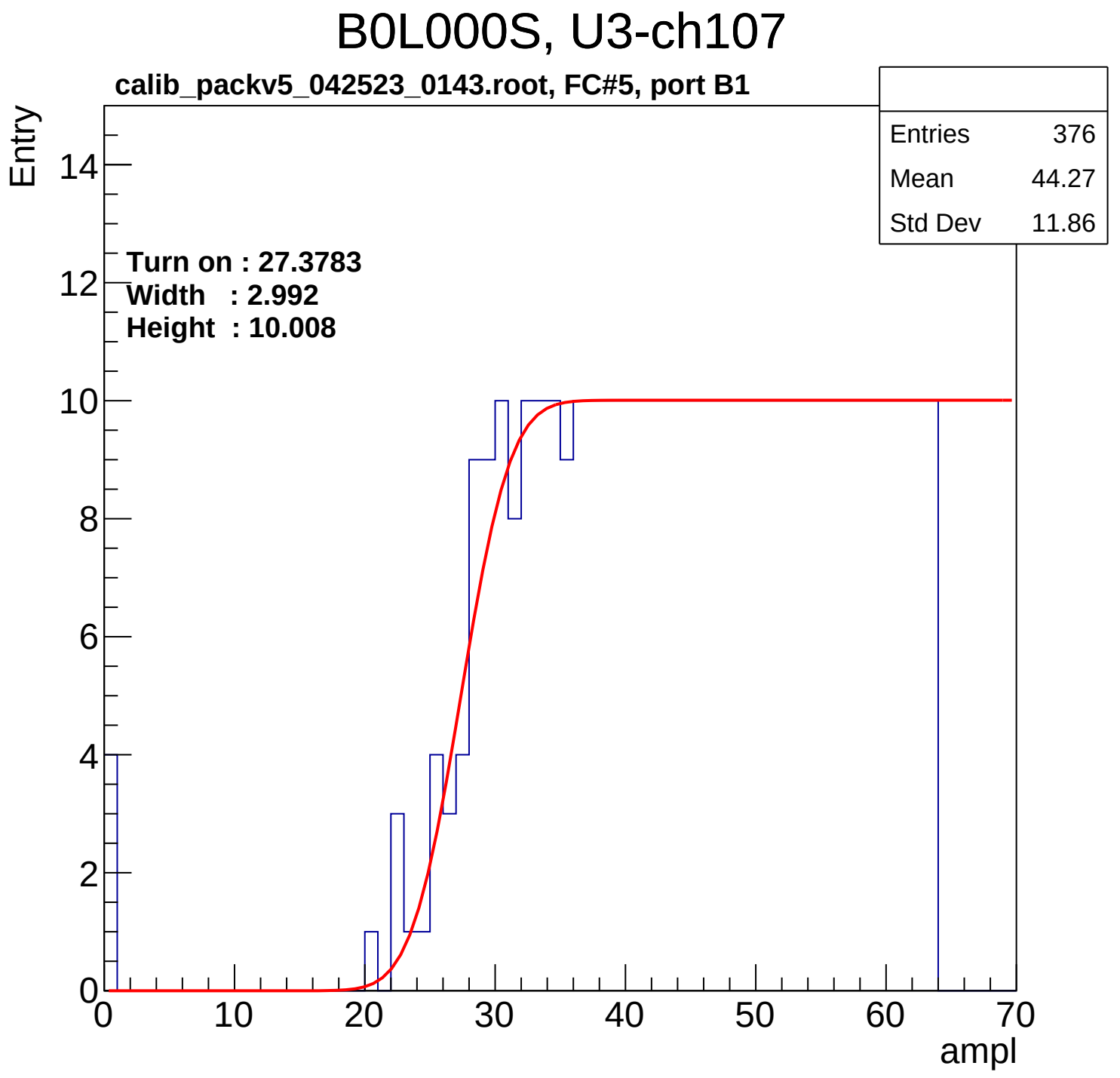
B0L000S, U3-ch107
calib_packv5_042523_0143.root, FC#5, port B1
Entries 376
Mean 44.27
Std Dev 11.86
Turn on : 27.3783
Width : 2.992
Height : 10.008
Entry
ampl
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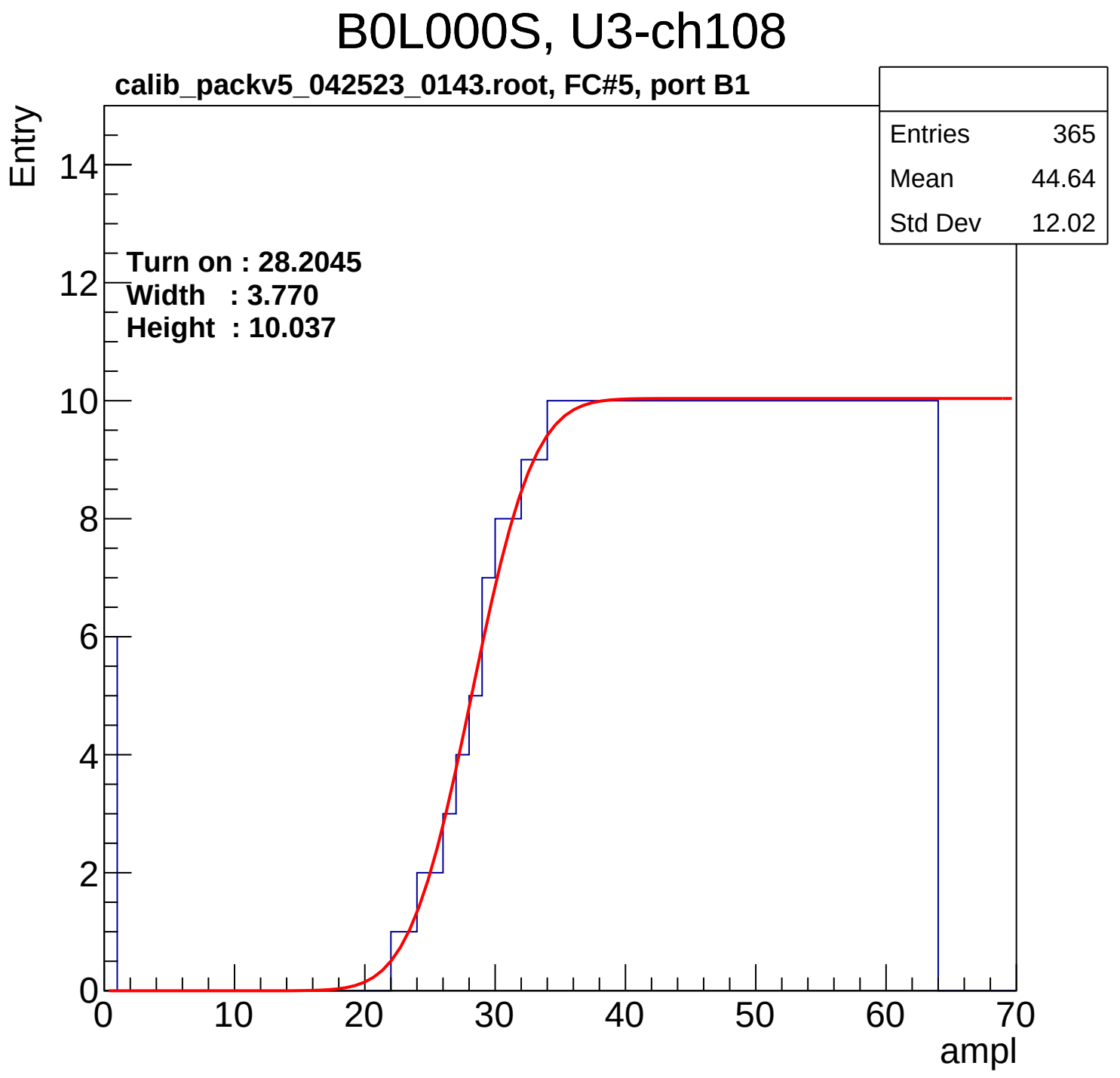
B0L000S, U3-ch108
calib_packv5_042523_0143.root, FC#5, port B1
Entries 365
Mean 44.64
Std Dev 12.02
Turn on : 28.2045
Width : 3.770
Height : 10.037
Entry
ampl
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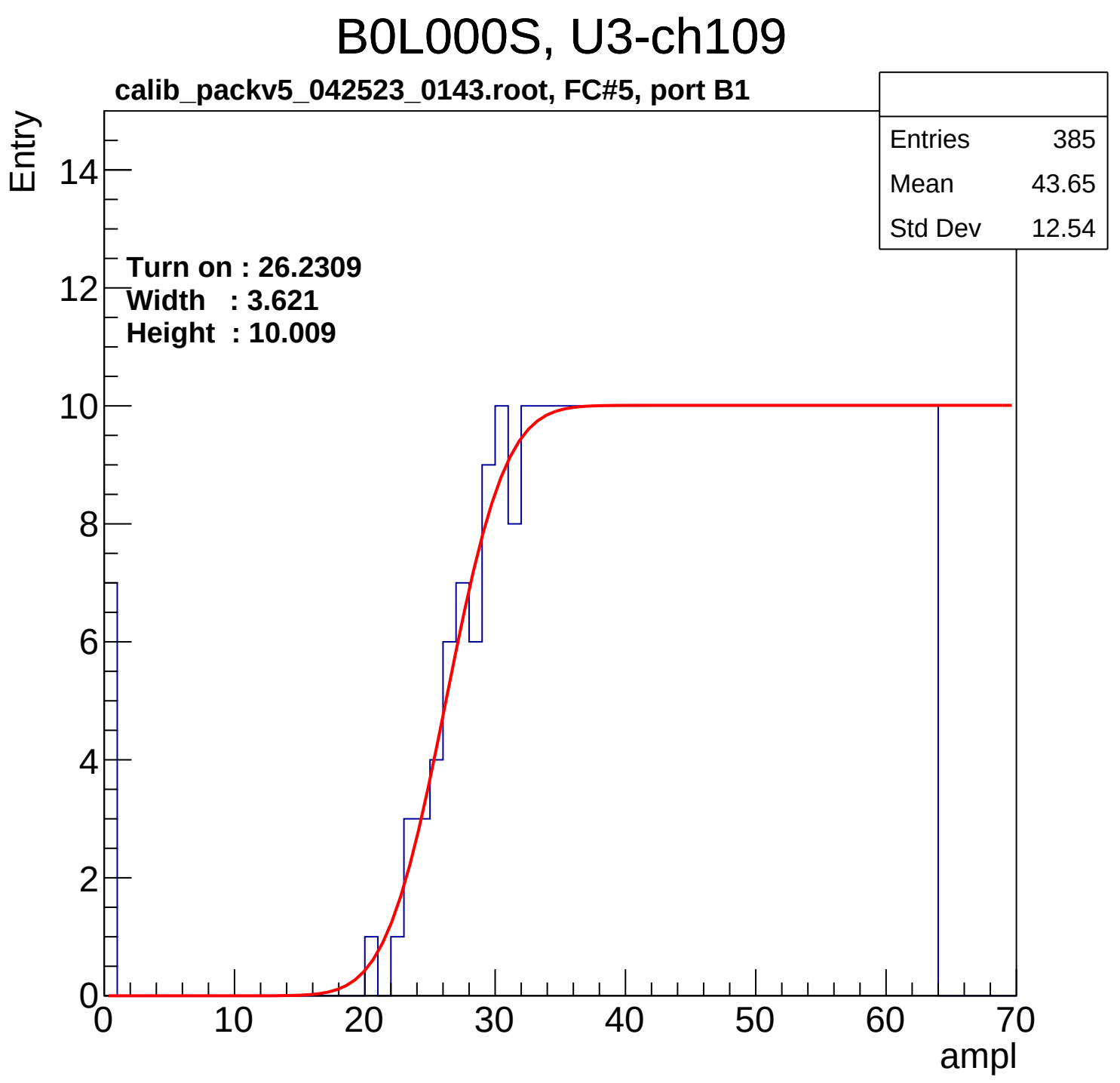
B0L000S, U3-ch109
calib_packv5_042523_0143.root, FC#5, port B1
Entries 385
Mean 43.65
Std Dev 12.54
Turn on : 26.2309
Width : 3.621
Height : 10.009
Entry
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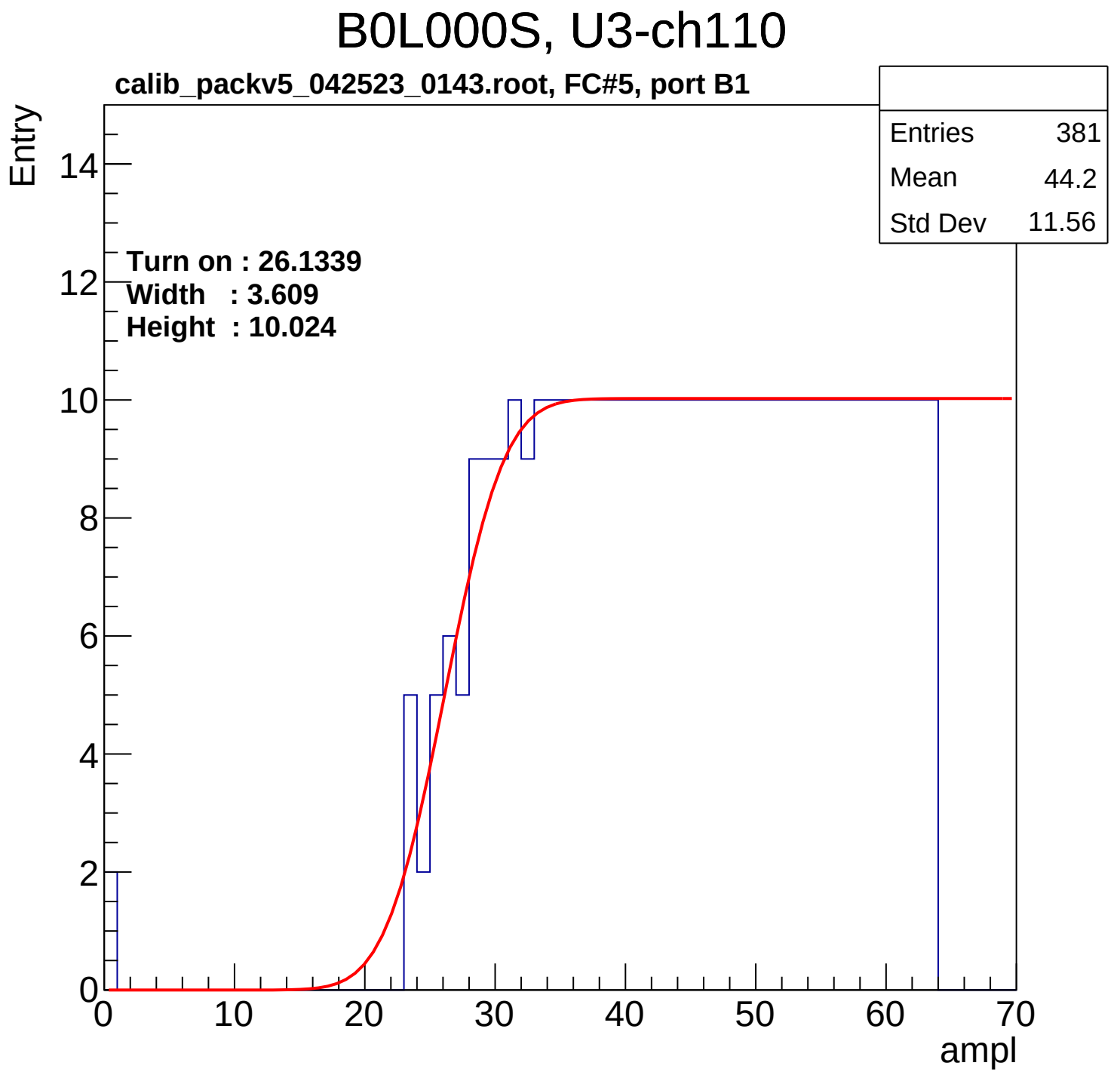
B0L000S, U3-ch110
calib_packv5_042523_0143.root, FC#5, port B1
Entries 381
Mean 44.2
Std Dev 11.56
Turn on : 26.1339
Width : 3.609
Height : 10.024
Entry
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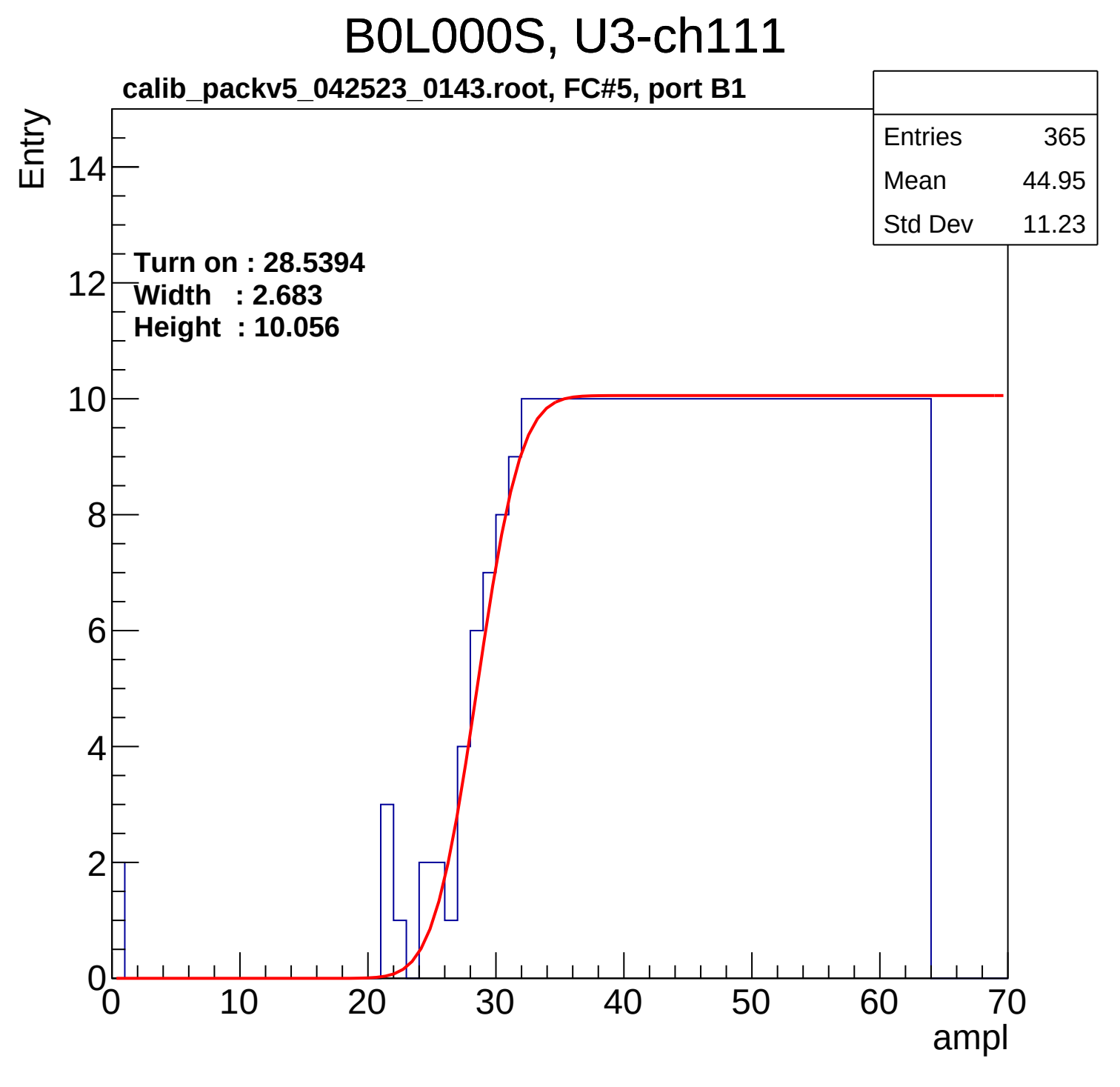
B0L000S, U3-ch111
calib_packv5_042523_0143.root, FC#5, port B1
Entries 365
Mean 44.95
Std Dev 11.23
Turn on : 28.5394
Width : 2.683
Height : 10.056
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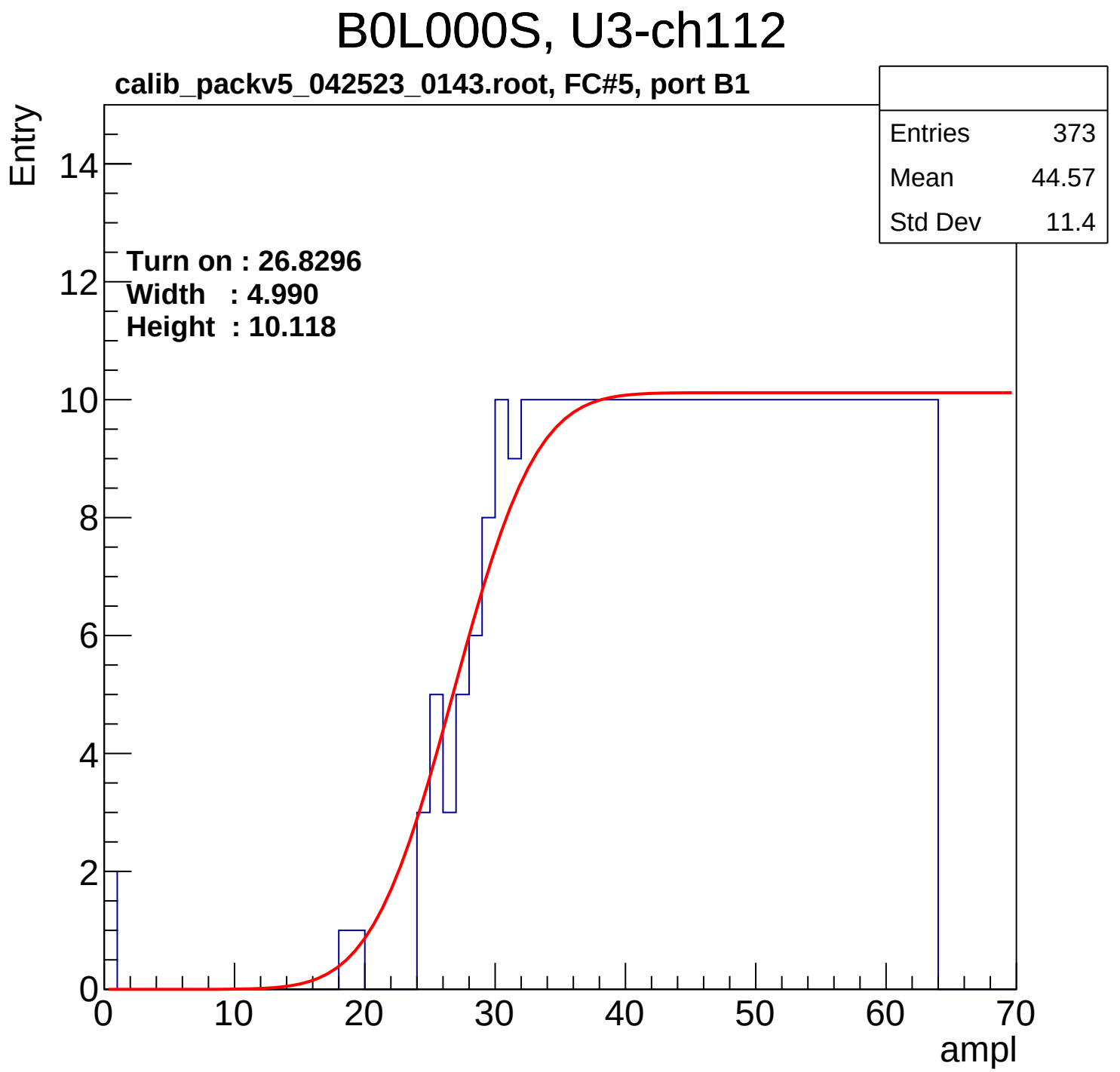
B0L000S, U3-ch112
calib_packv5_042523_0143.root, FC#5, port B1
Entries 373
Mean 44.57
Std Dev 11.4
Turn on : 26.8296
Width : 4.990
Height : 10.118
Entry
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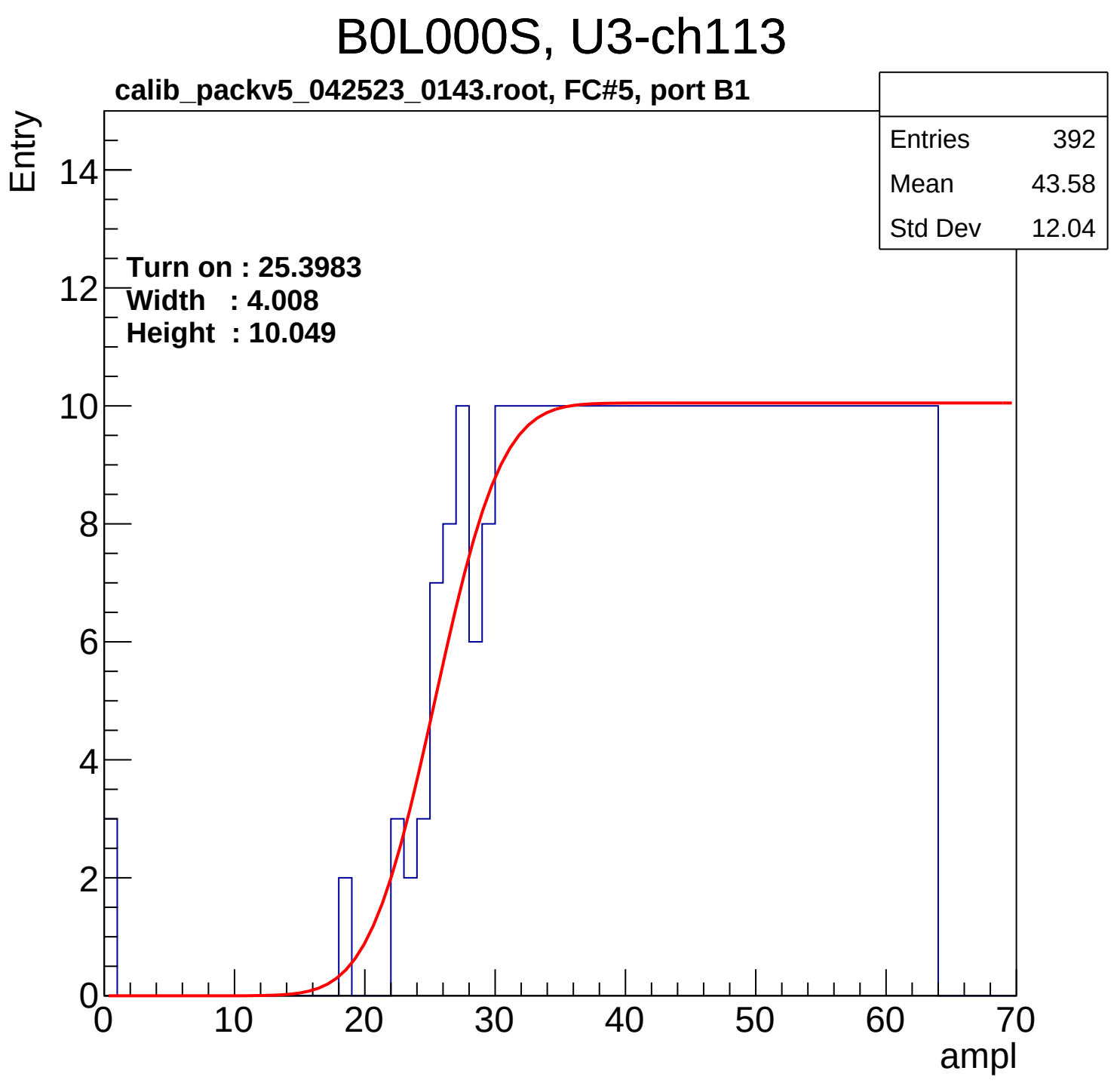
B0L000S, U3-ch113
calib_packv5_042523_0143.root, FC#5, port B1
Entries 392
Mean 43.58
Std Dev 12.04
Turn on : 25.3983
Width : 4.008
Height : 10.049
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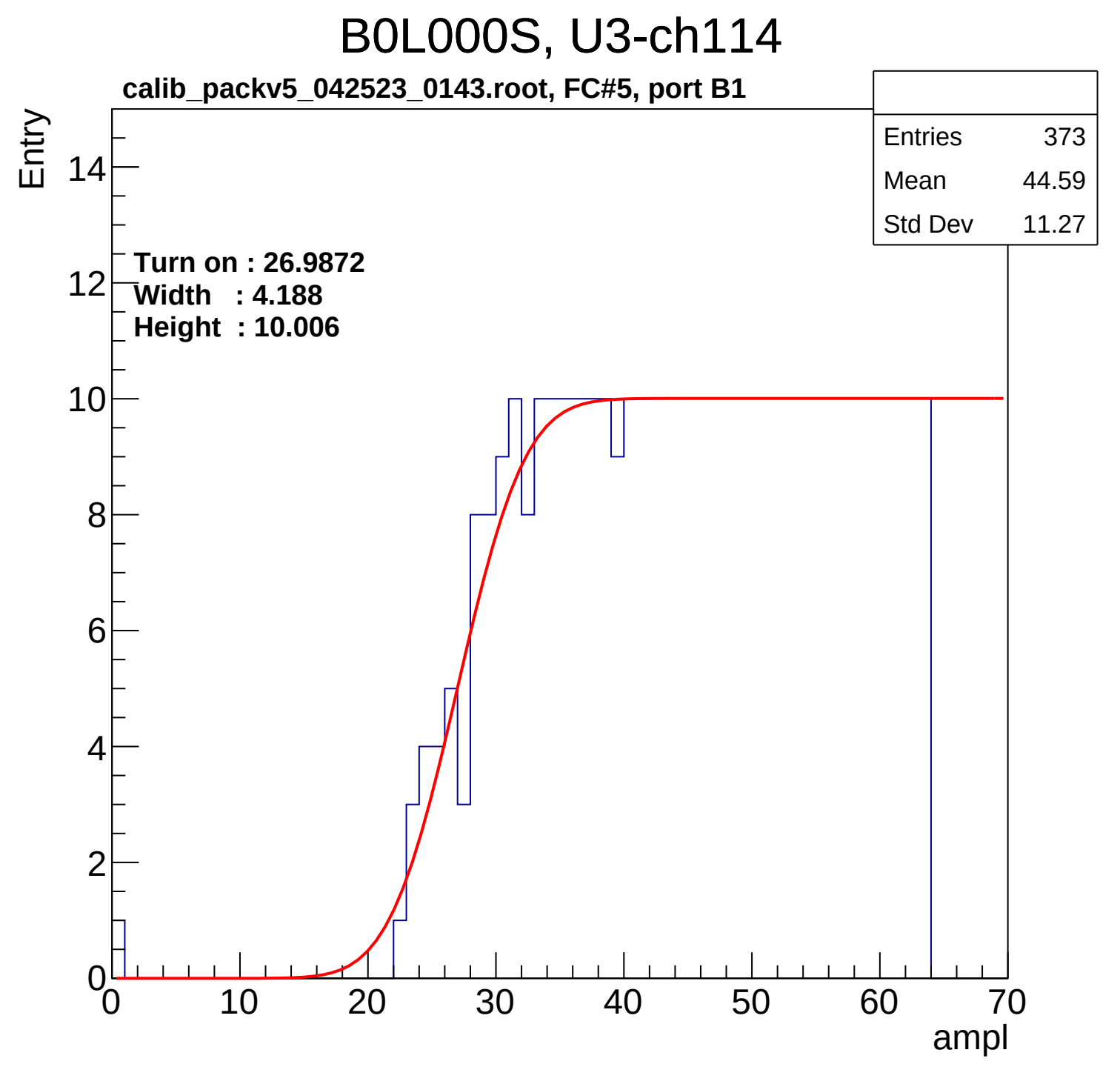
B0L000S, U3-ch114
calib_packv5_042523_0143.root, FC#5, port B1
Entries 373
Mean 44.59
Std Dev 11.27
Turn on : 26.9872
Width : 4.188
Height : 10.006
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ampl
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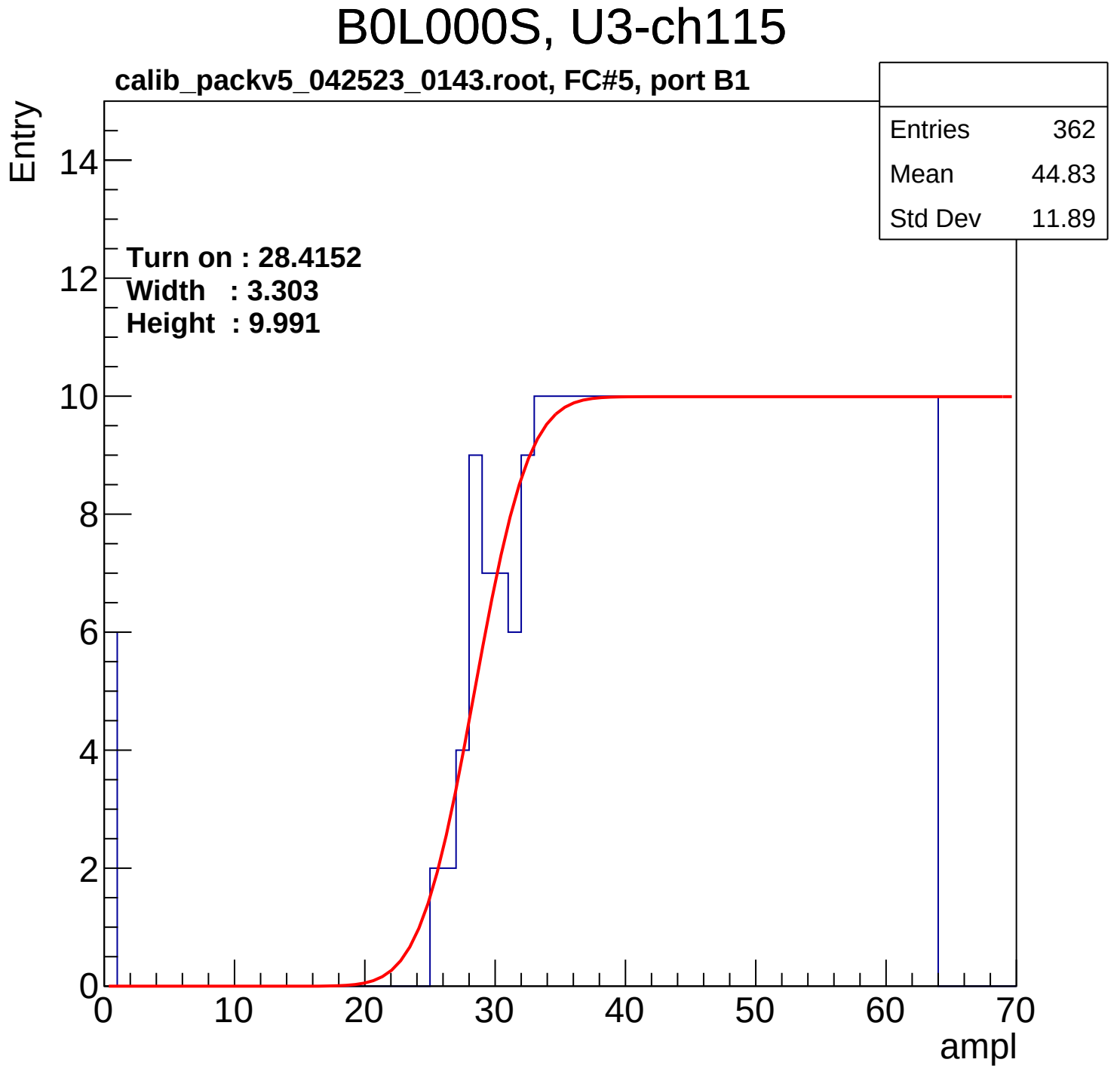
B0L000S, U3-ch115
calib_packv5_042523_0143.root, FC#5, port B1
Entries 362
Mean 44.83
Std Dev 11.89
Turn on : 28.4152
Width : 3.303
Height : 9.991
Entry
ampl
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4
6
8
10
12
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10
20
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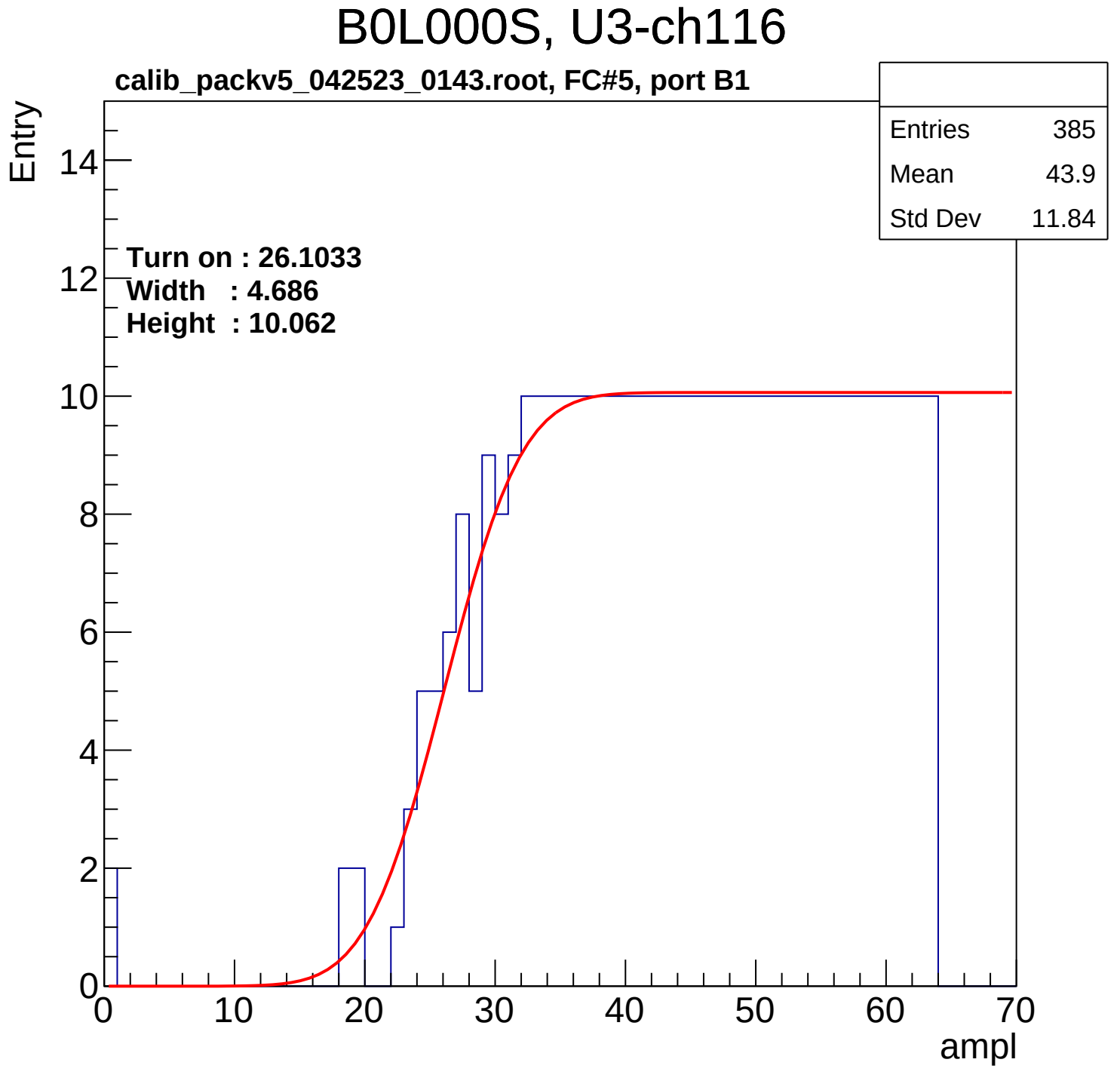
B0L000S, U3-ch116
calib_packv5_042523_0143.root, FC#5, port B1
Entries 385
Mean 43.9
Std Dev 11.84
Turn on : 26.1033
Width : 4.686
Height : 10.062
Entry
ampl
0
2
4
6
8
10
12
14
0
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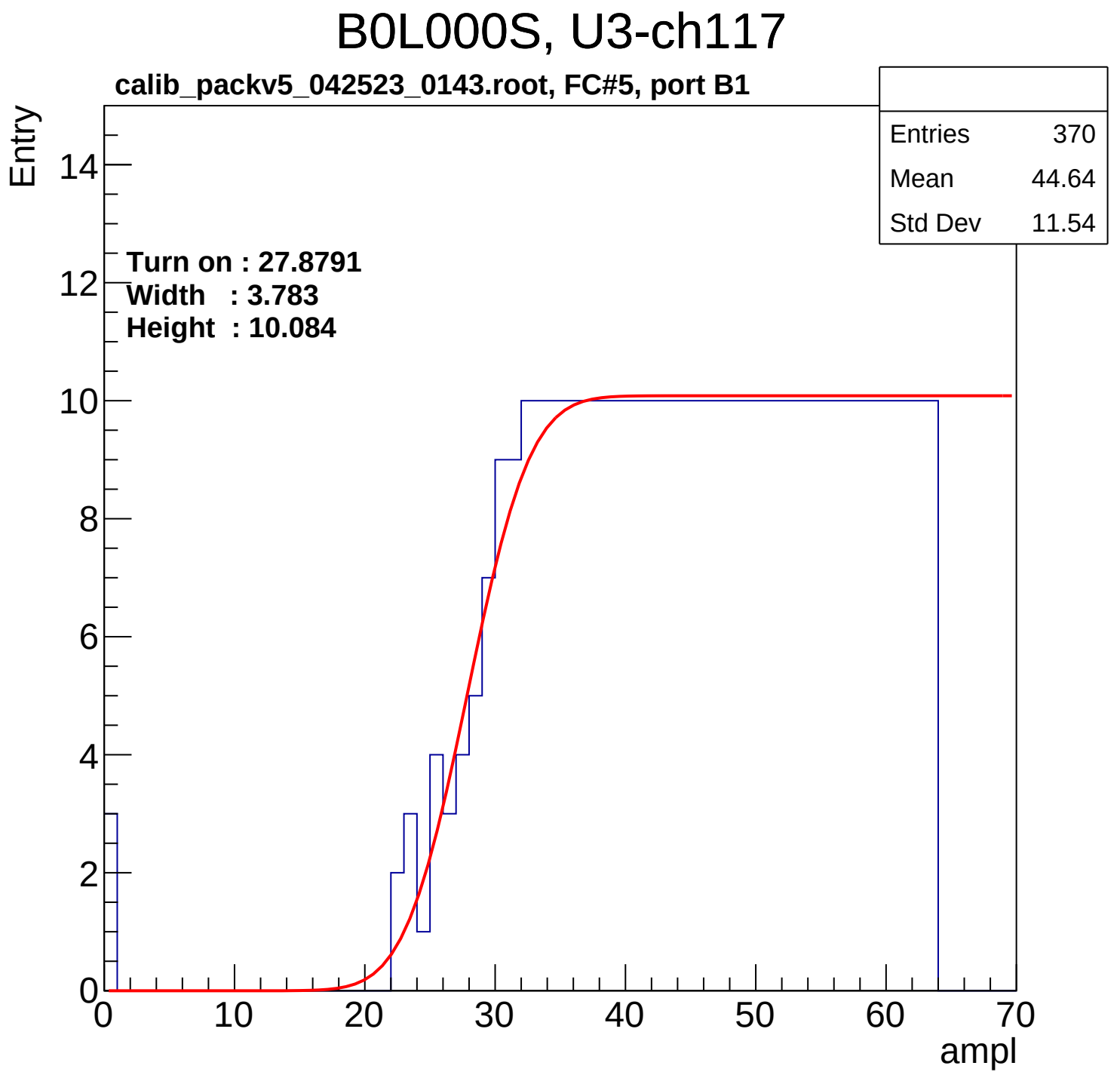
B0L000S, U3-ch117
calib_packv5_042523_0143.root, FC#5, port B1
Entries 370
Mean 44.64
Std Dev 11.54
Turn on : 27.8791
Width : 3.783
Height : 10.084
Entry
ampl
0
2
4
6
8
10
12
14
0
10
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40
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60
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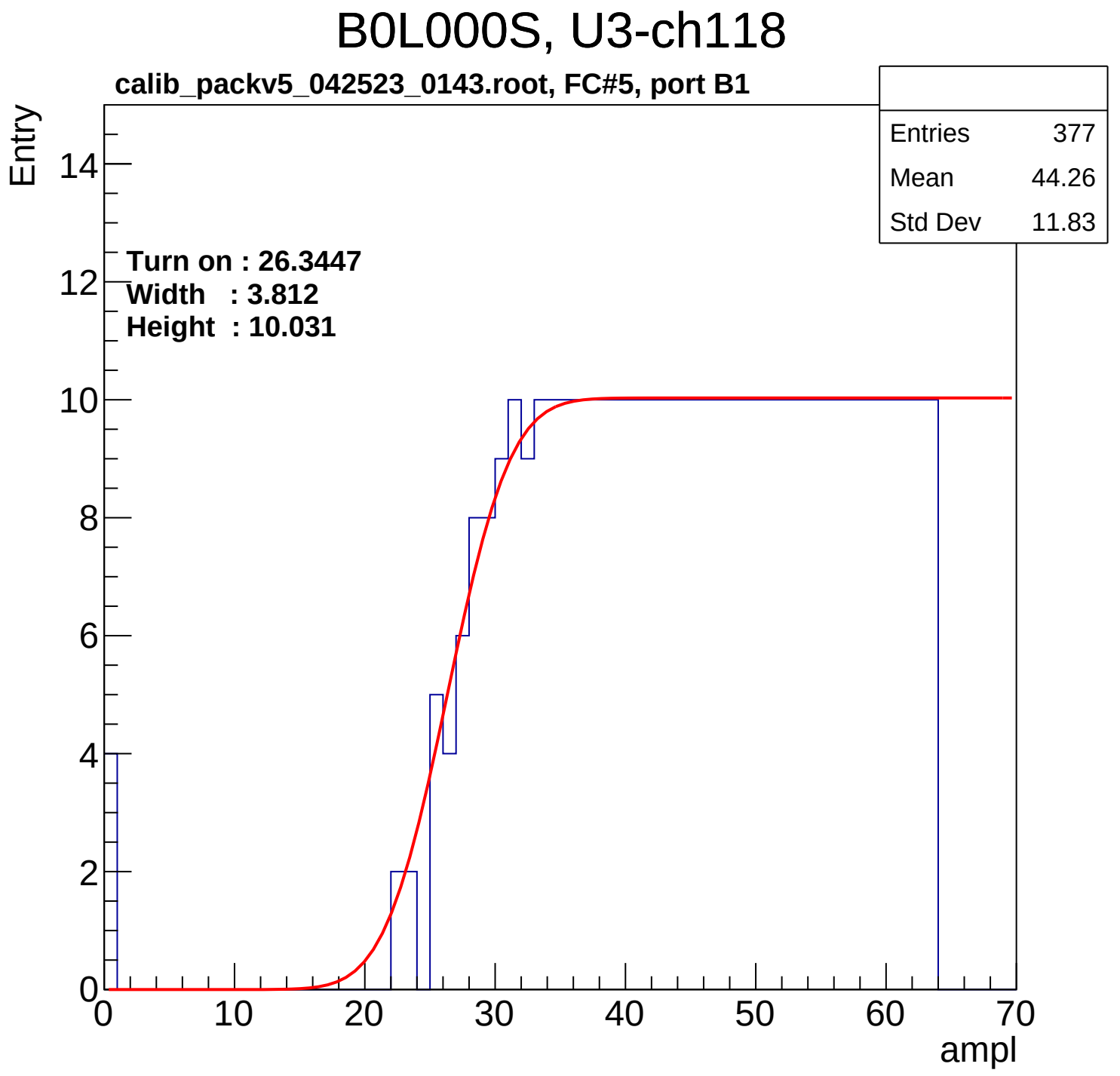
B0L000S, U3-ch118
calib_packv5_042523_0143.root, FC#5, port B1
Entries 377
Mean 44.26
Std Dev 11.83
Turn on : 26.3447
Width : 3.812
Height : 10.031
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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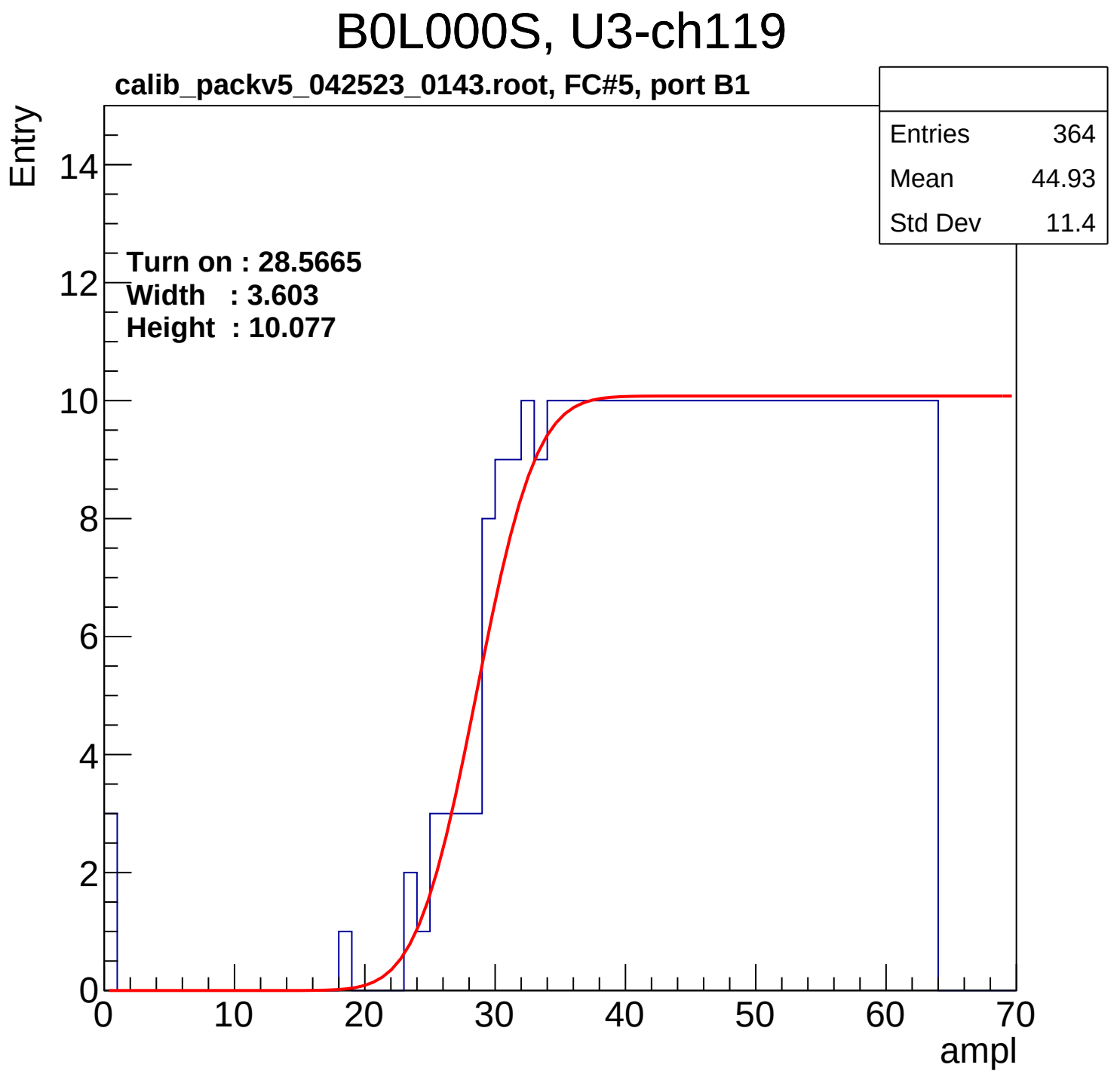
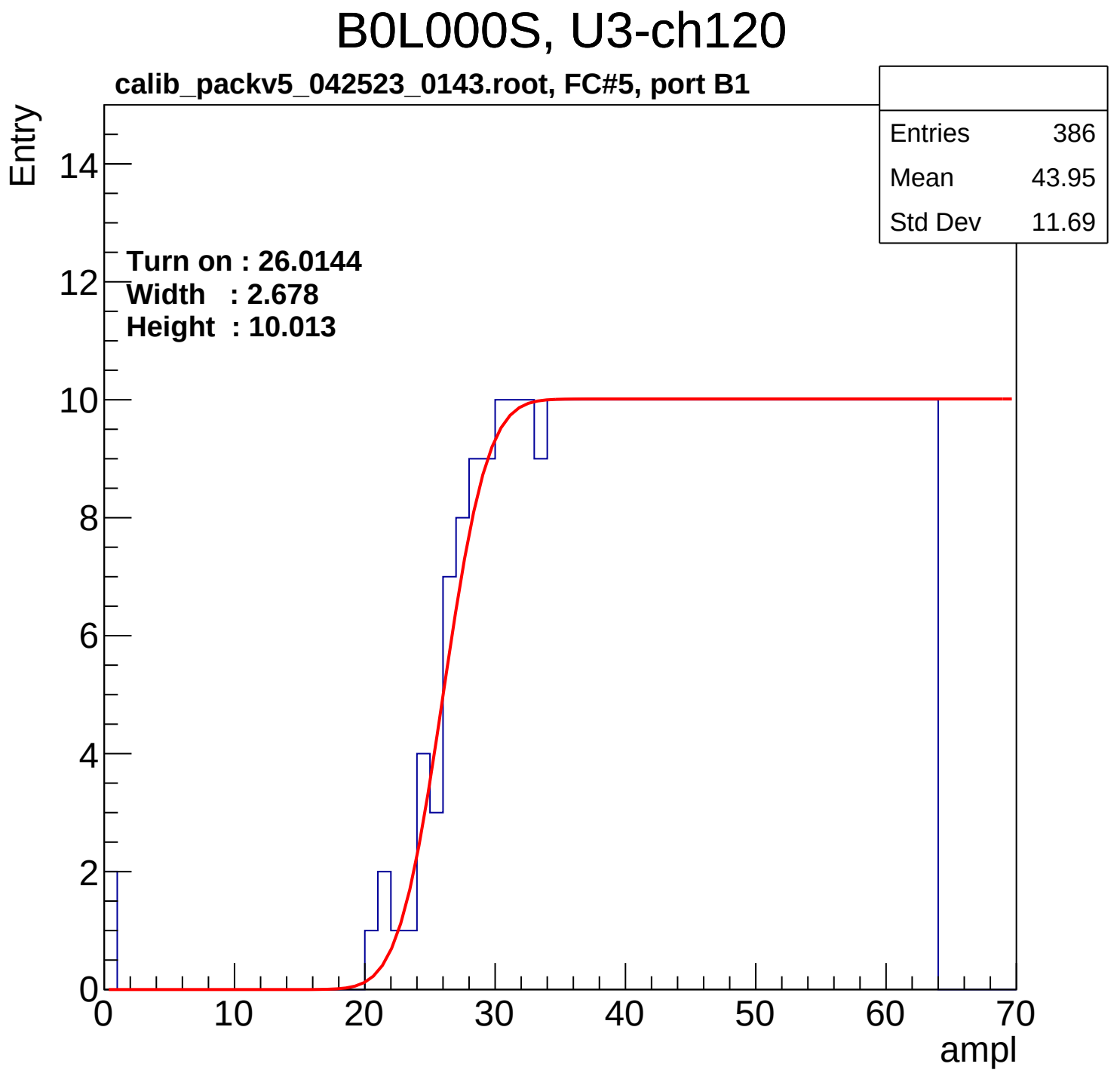
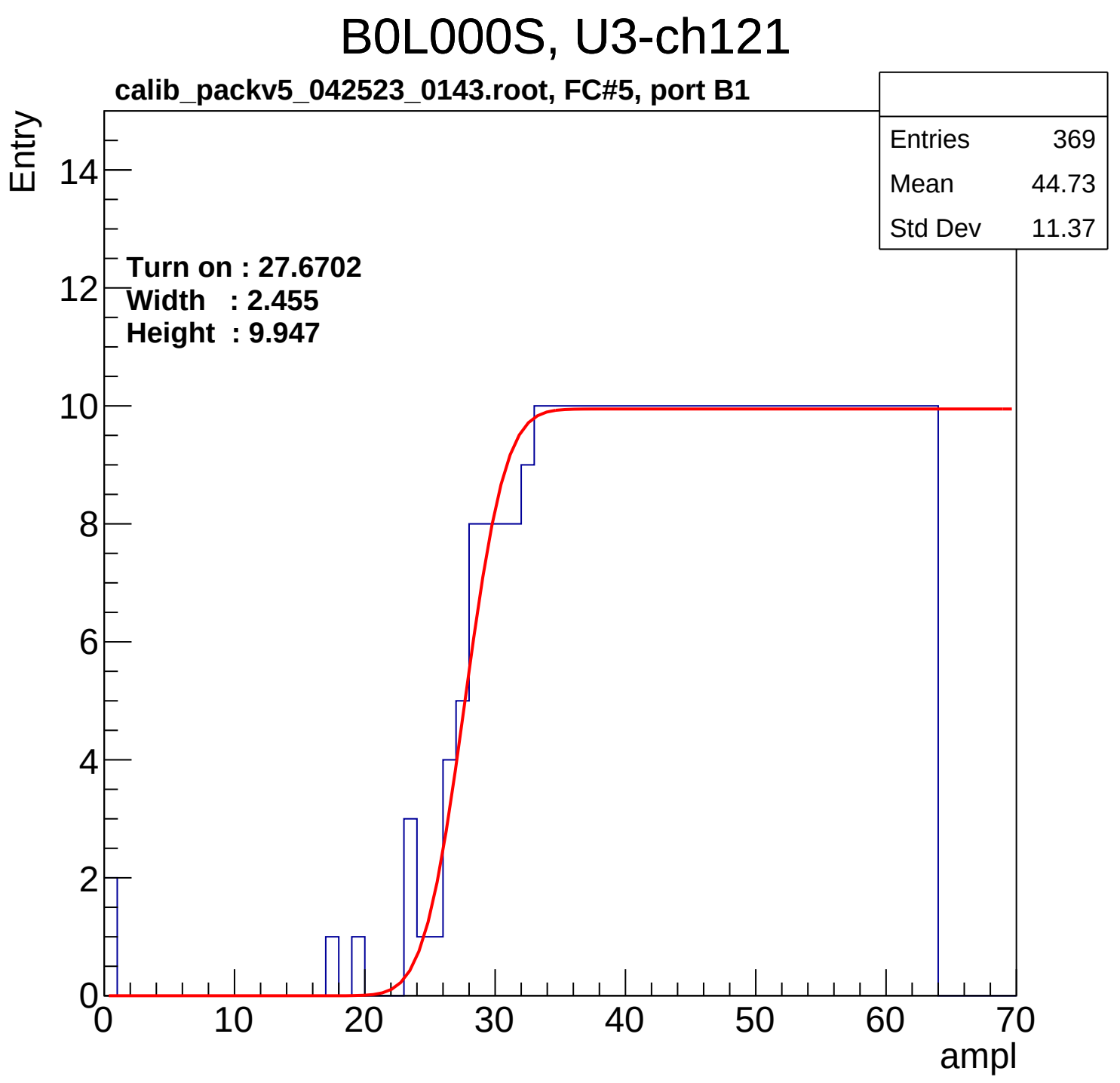
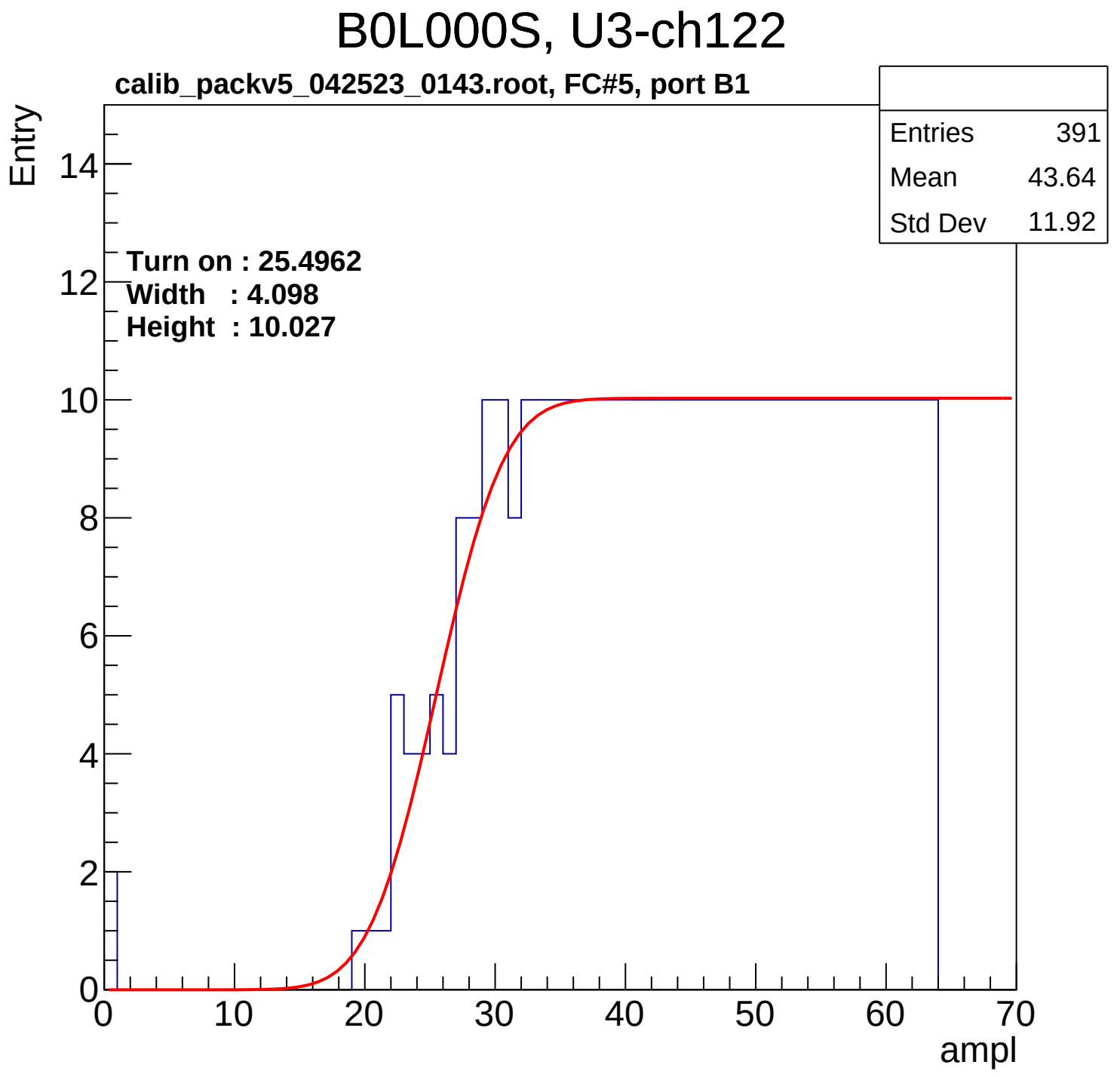

B0L000S, U3-ch119
calib_packv5_042523_0143.root, FC#5, port B1
Entries 364
Mean 44.93
Std Dev 11.4
Turn on : 28.5665
Width : 3.603
Height : 10.077
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L000S, U3-ch120
calib_packv5_042523_0143.root, FC#5, port B1
Entries 386
Mean 43.95
Std Dev 11.69
Turn on : 26.0144
Width : 2.678
Height : 10.013
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L000S, U3-ch121
calib_packv5_042523_0143.root, FC#5, port B1
Entries 369
Mean 44.73
Std Dev 11.37
Turn on : 27.6702
Width : 2.455
Height : 9.947
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L000S, U3-ch122
calib_packv5_042523_0143.root, FC#5, port B1
Entries 391
Mean 43.64
Std Dev 11.92
Turn on : 25.4962
Width : 4.098
Height : 10.027
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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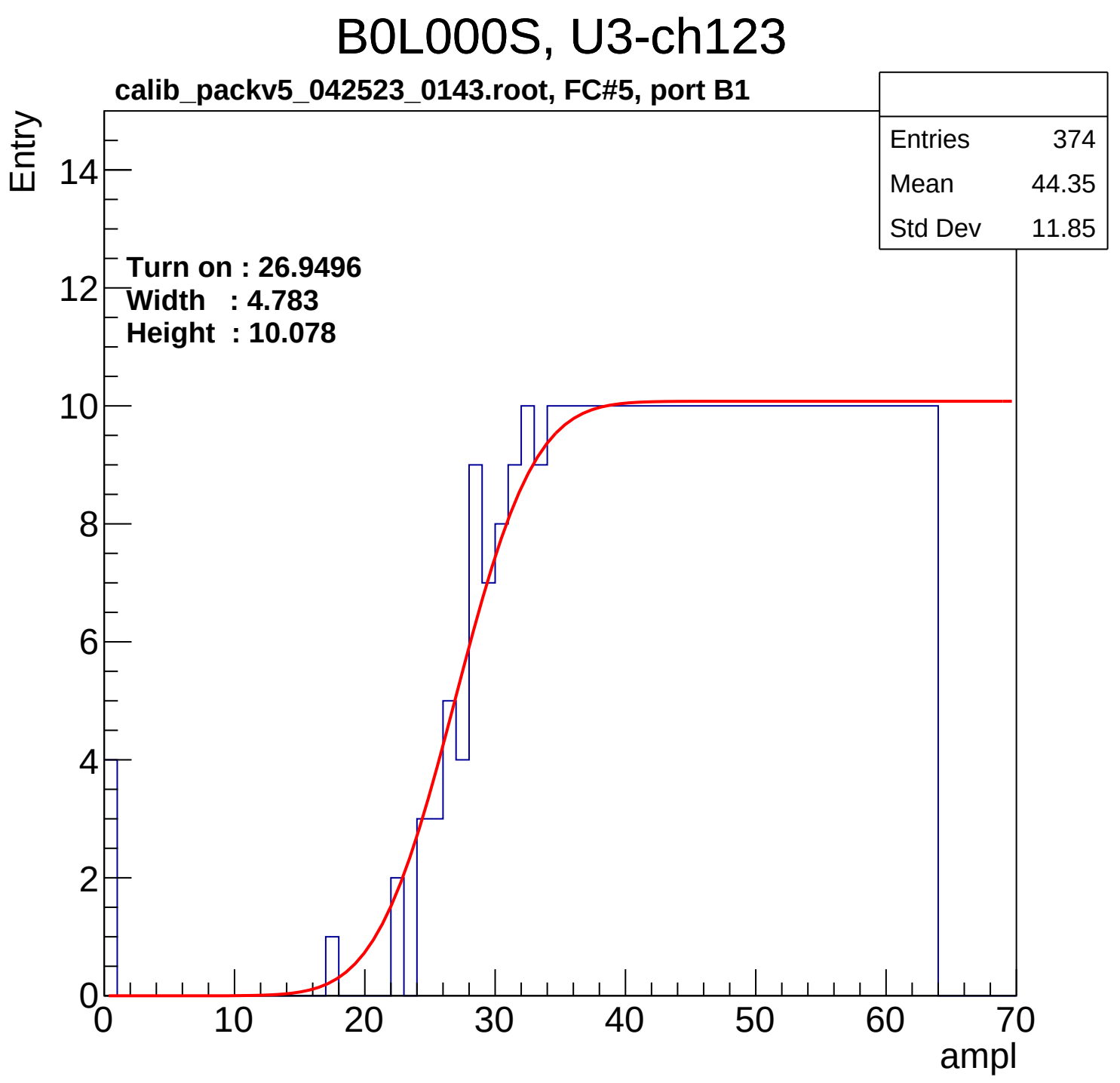
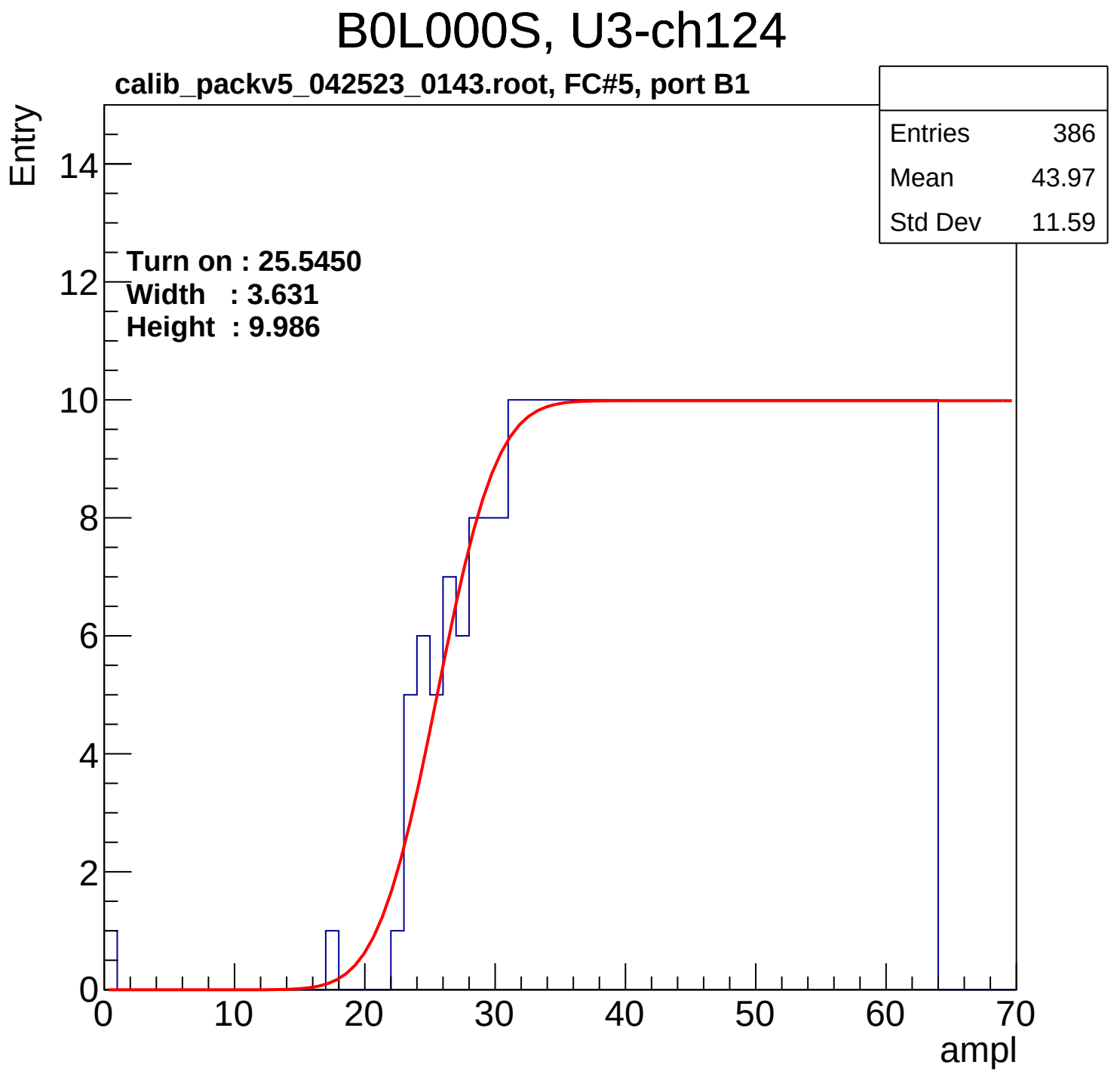
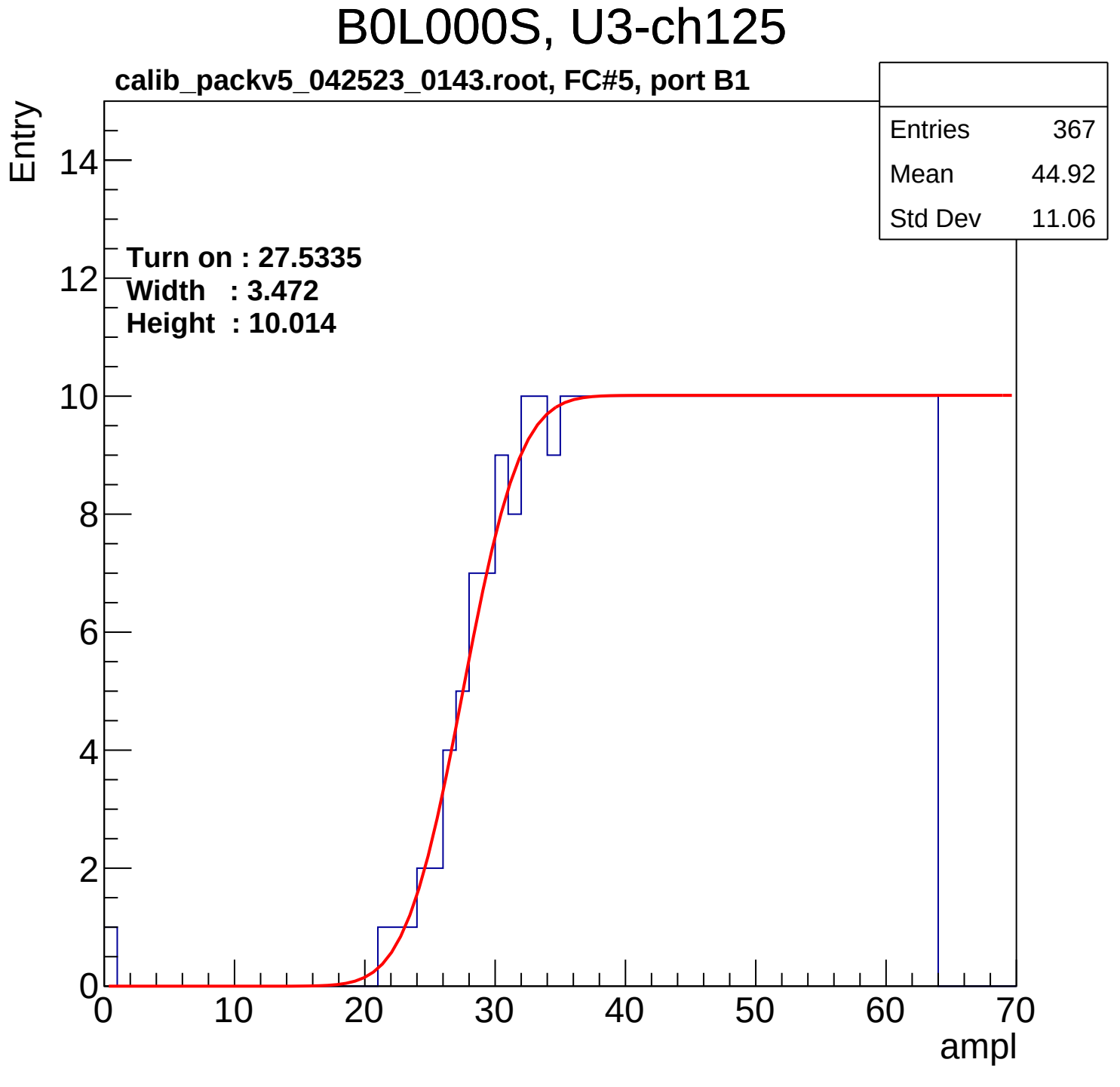
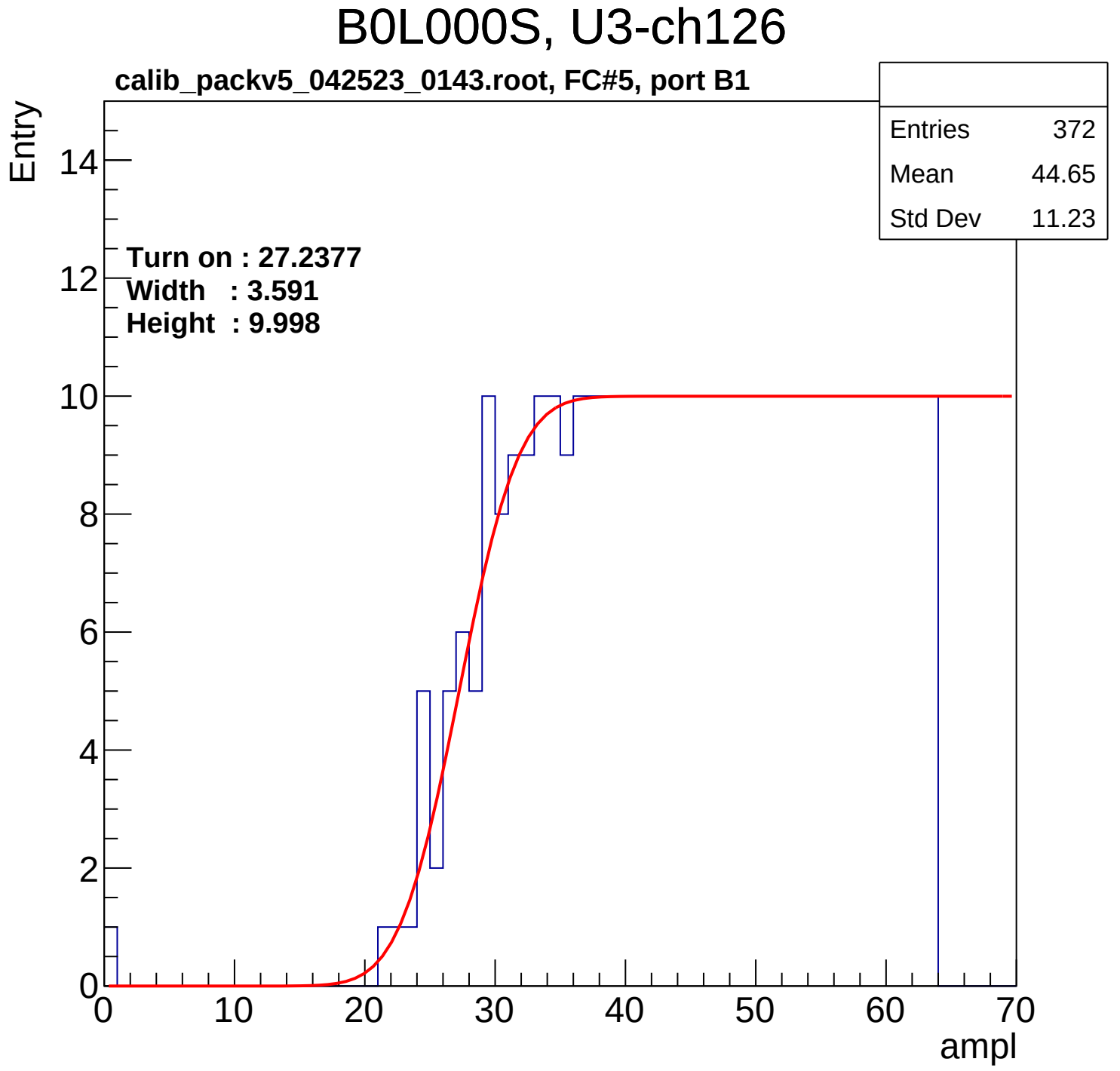
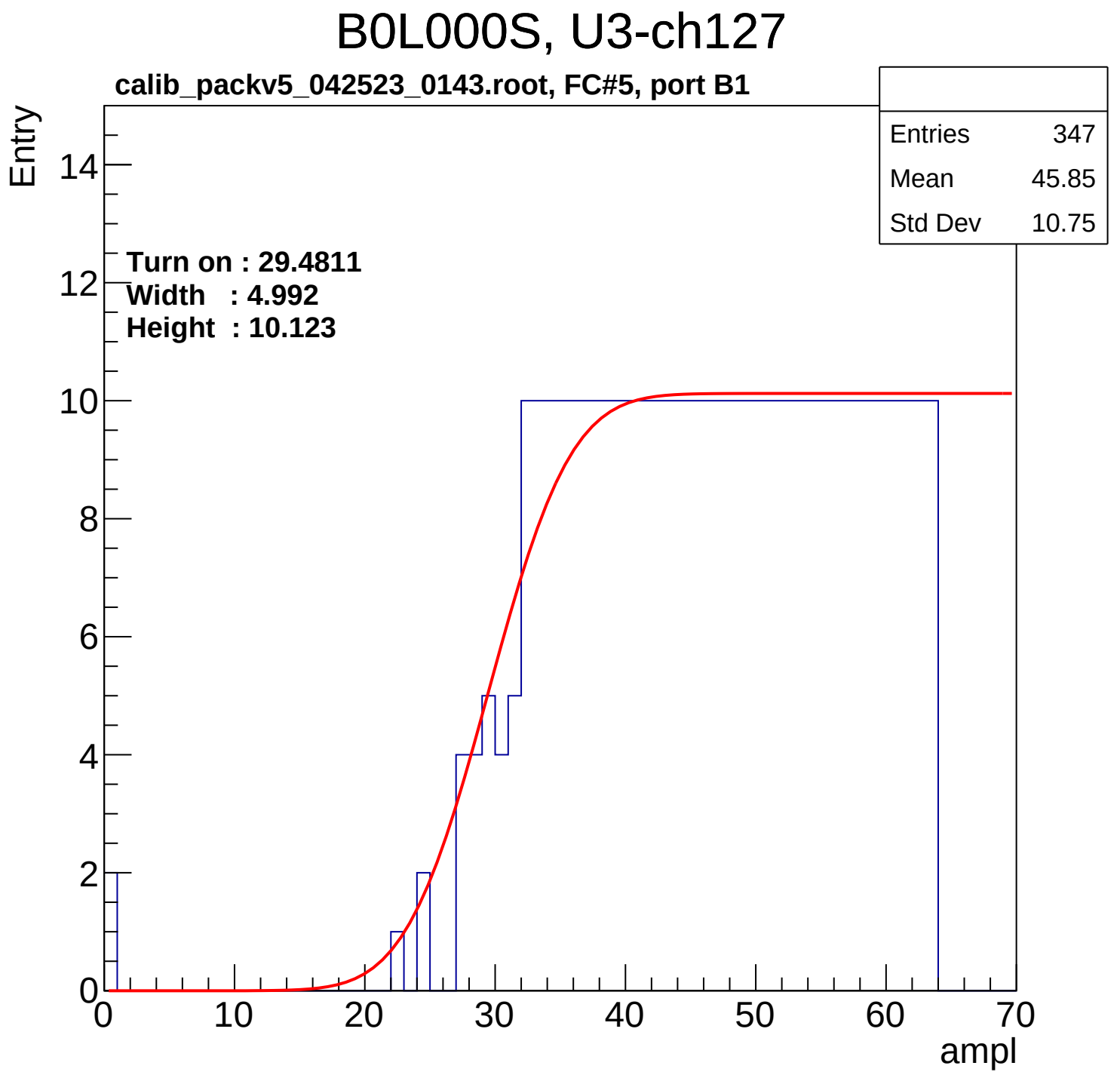
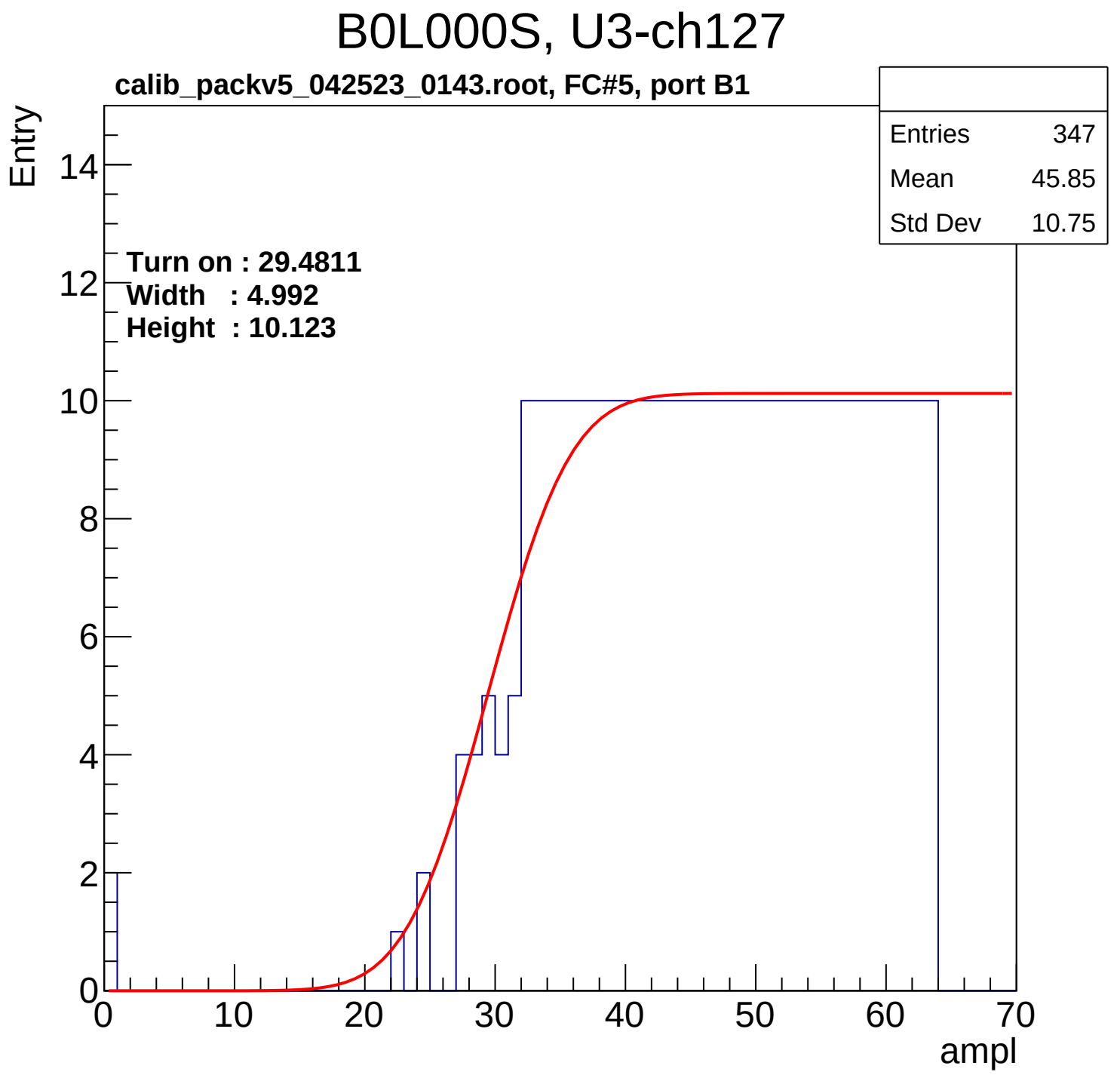

B0L000S, U3-ch123
calib_packv5_042523_0143.root, FC#5, port B1
Entries 374
Mean 44.35
Std Dev 11.85
Turn on : 26.9496
Width : 4.783
Height : 10.078
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L000S, U3-ch124
calib_packv5_042523_0143.root, FC#5, port B1
Entries 386
Mean 43.97
Std Dev 11.59
Turn on : 25.5450
Width : 3.631
Height : 9.986
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L000S, U3-ch125
calib_packv5_042523_0143.root, FC#5, port B1
Entries 367
Mean 44.92
Std Dev 11.06
Turn on : 27.5335
Width : 3.472
Height : 10.014
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L000S, U3-ch126
calib_packv5_042523_0143.root, FC#5, port B1
Entries 372
Mean 44.65
Std Dev 11.23
Turn on : 27.2377
Width : 3.591
Height : 9.998
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L000S, U3-ch127
calib_packv5_042523_0143.root, FC#5, port B1
Entries 347
Mean 45.85
Std Dev 10.75
Turn on : 29.4811
Width : 4.992
Height : 10.123
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L000S, U3-ch127
calib_packv5_042523_0143.root, FC#5, port B1
Entries 347
Mean 45.85
Std Dev 10.75
Turn on : 29.4811
Width : 4.992
Height : 10.123
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70