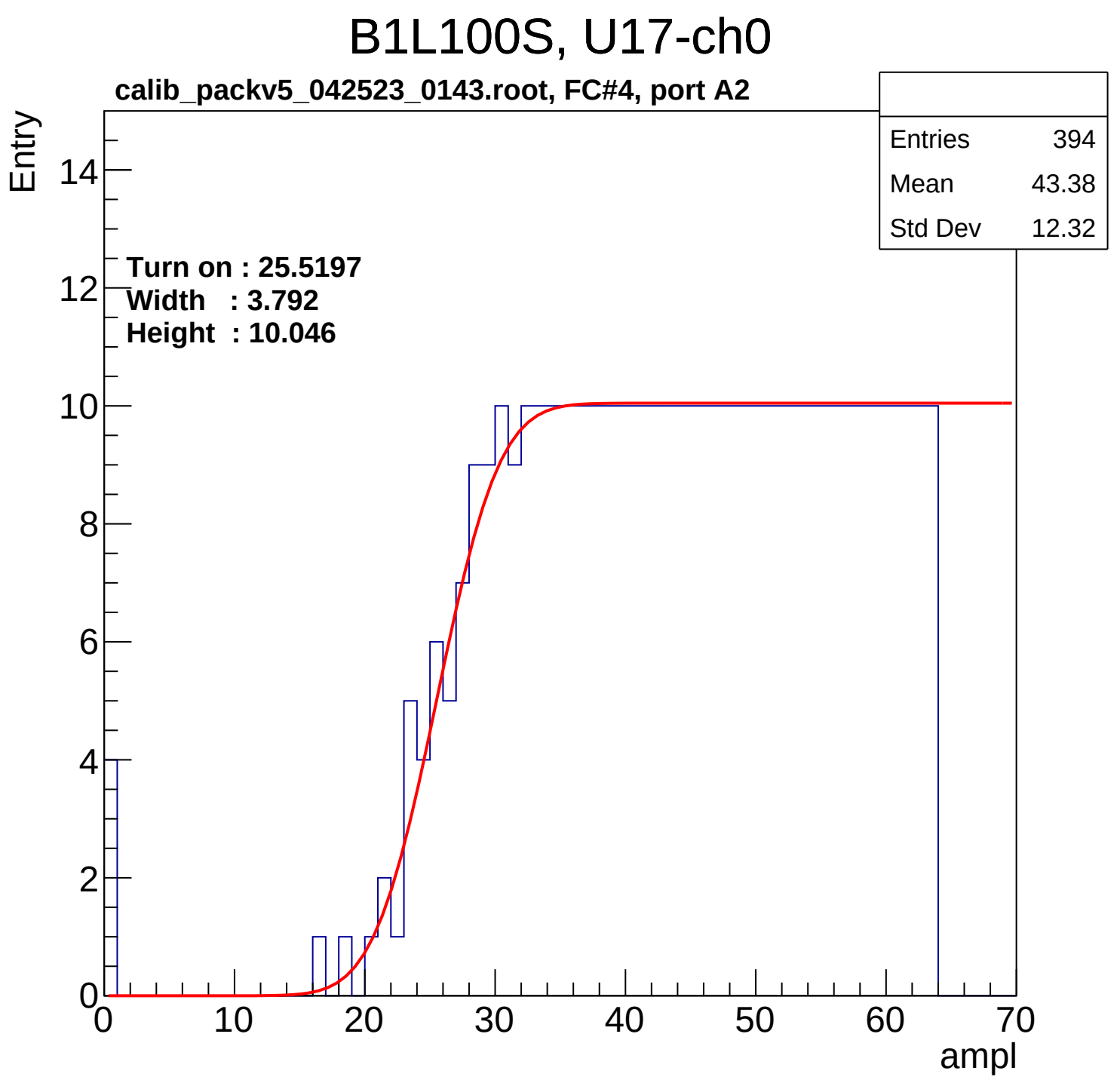
B1L100S, U17-ch0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 394
Mean 43.38
Std Dev 12.32
Turn on : 25.5197
Width : 3.792
Height : 10.046
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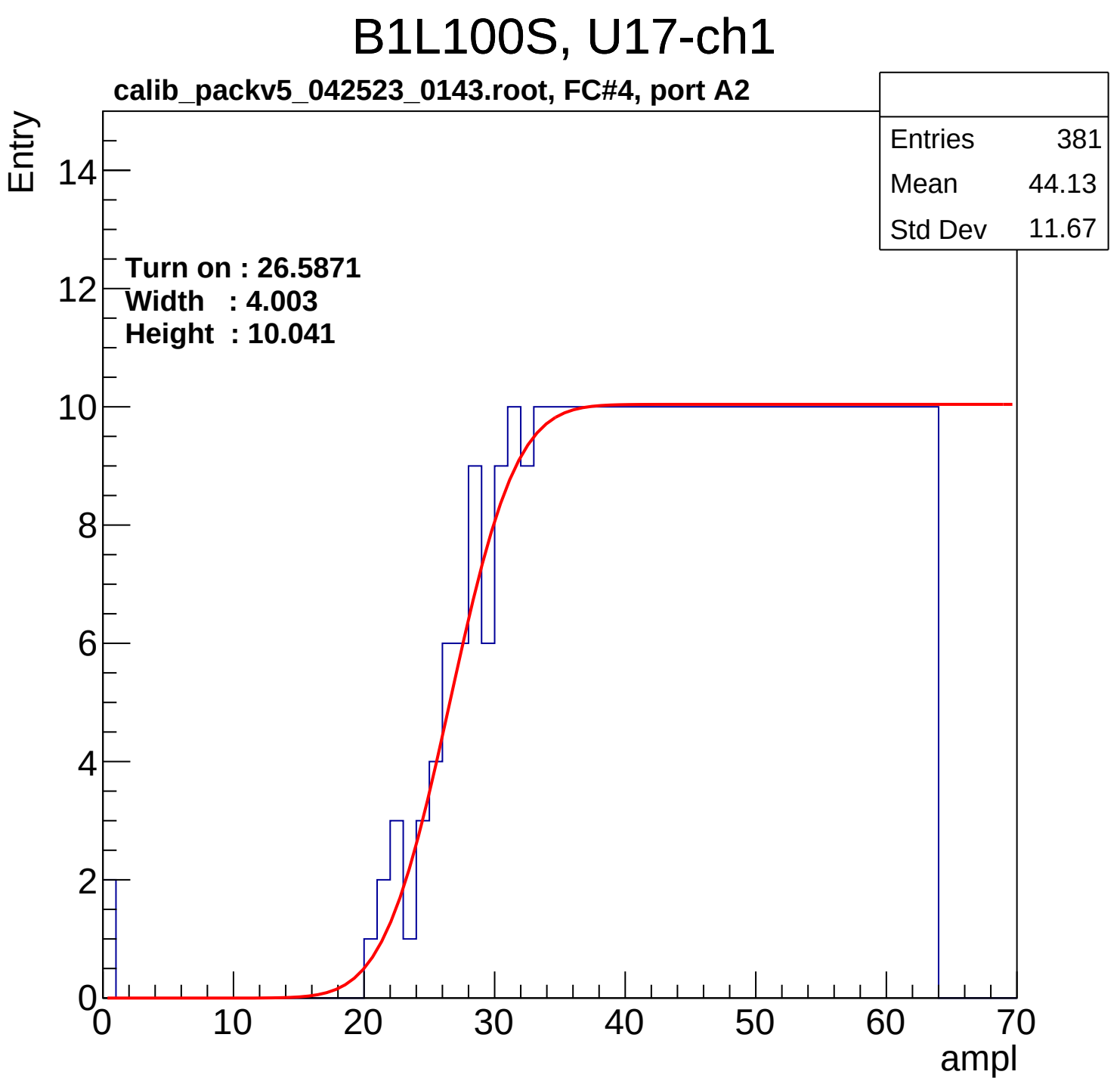
B1L100S, U17-ch1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 381
Mean 44.13
Std Dev 11.67
Turn on : 26.5871
Width : 4.003
Height : 10.041
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ampl
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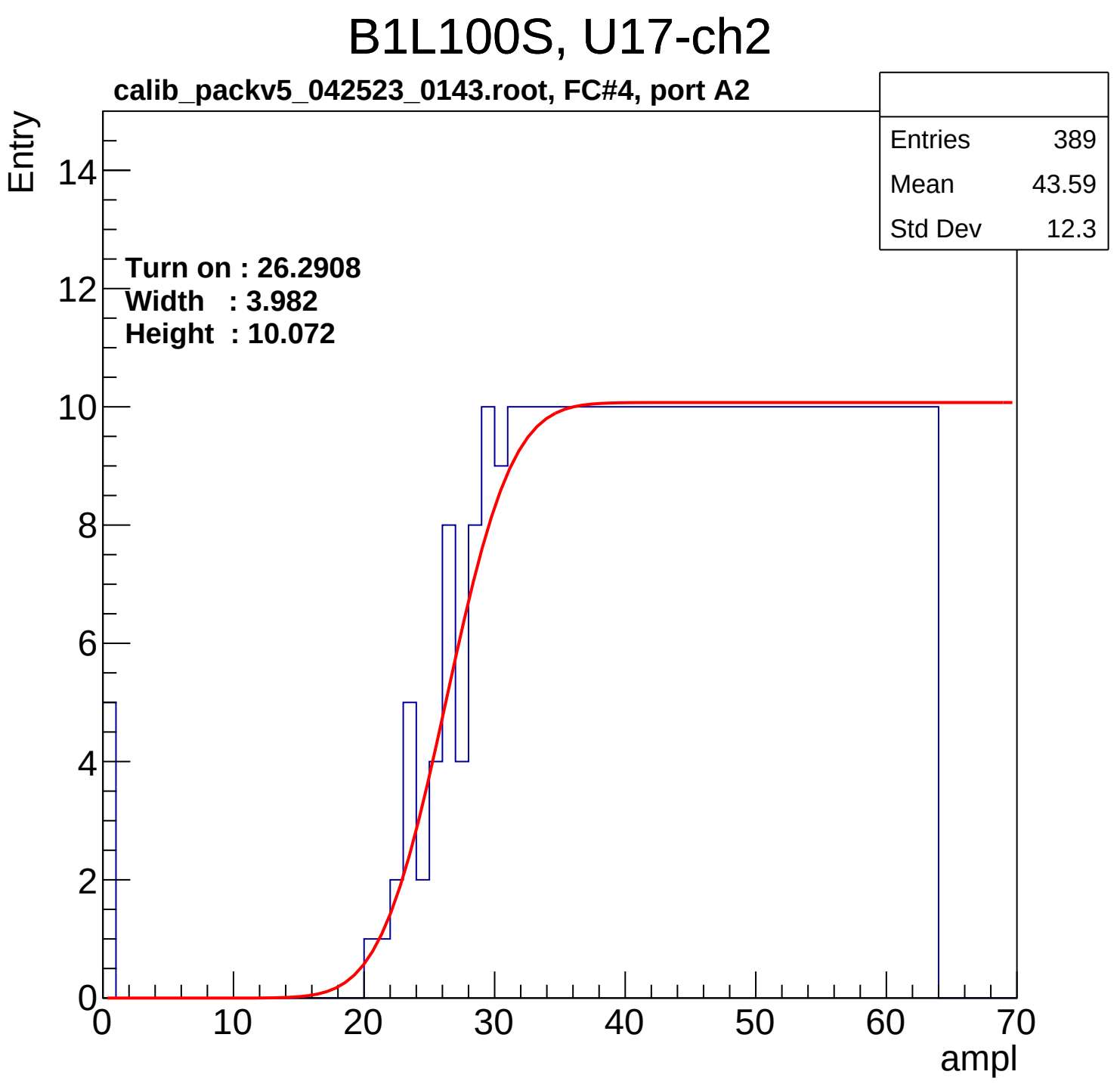
B1L100S, U17-ch2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 389
Mean 43.59
Std Dev 12.3
Turn on : 26.2908
Width : 3.982
Height : 10.072
Entry
ampl
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2
4
6
8
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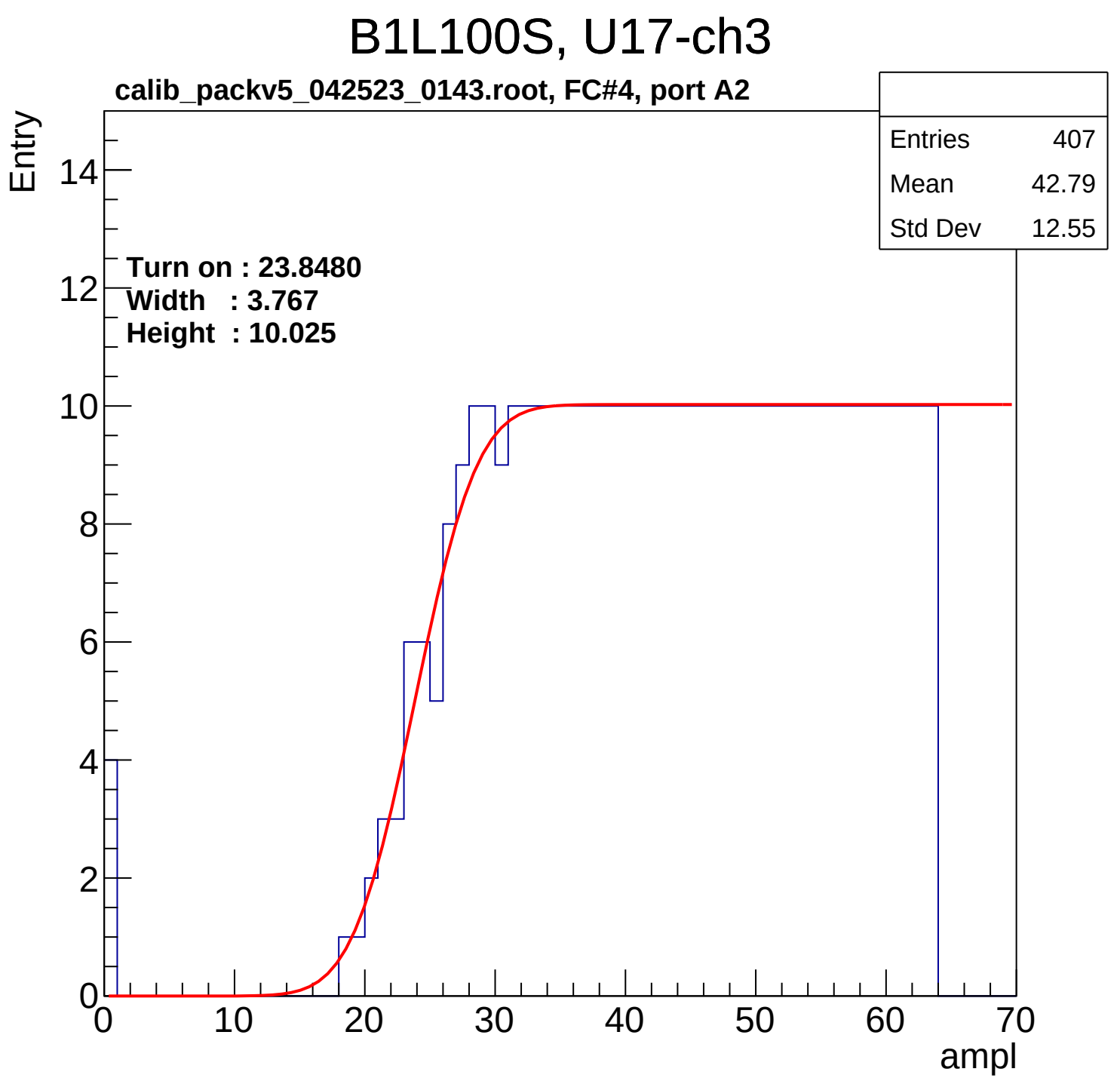
B1L100S, U17-ch3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 407
Mean 42.79
Std Dev 12.55
Turn on : 23.8480
Width : 3.767
Height : 10.025
Entry
ampl
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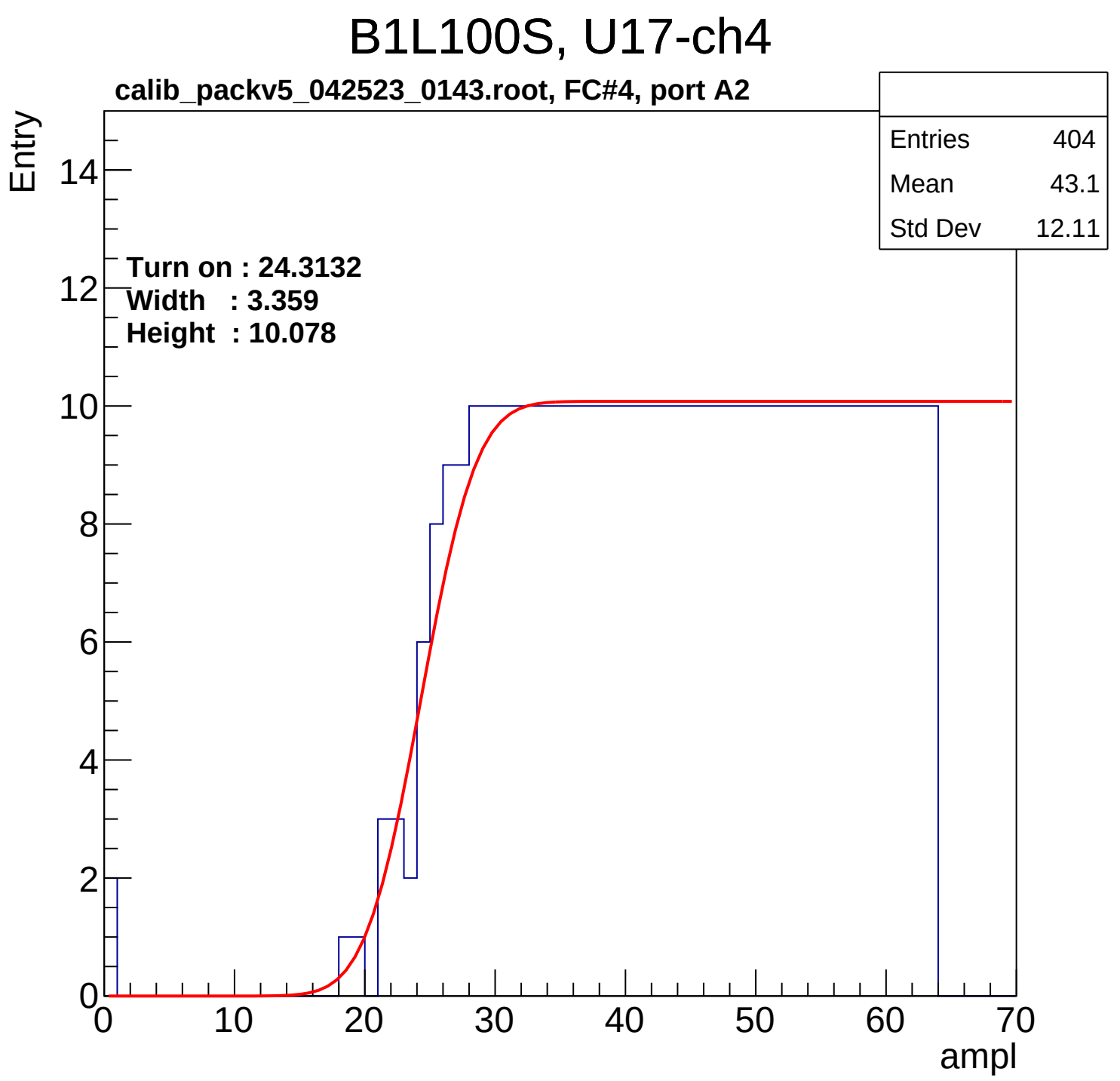
B1L100S, U17-ch4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 404
Mean 43.1
Std Dev 12.11
Turn on : 24.3132
Width : 3.359
Height : 10.078
Entry
ampl
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6
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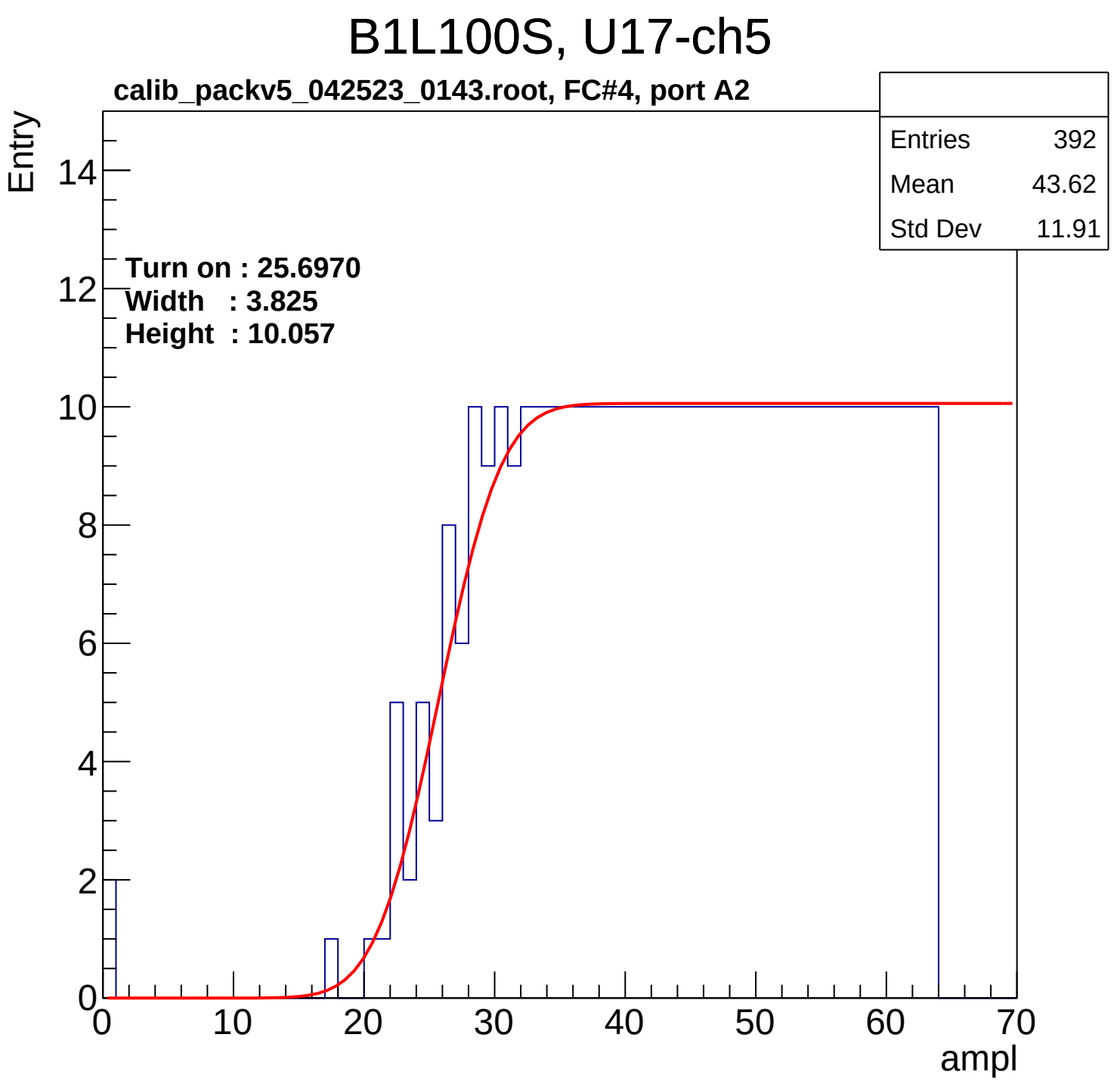
B1L100S, U17-ch5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 392
Mean 43.62
Std Dev 11.91
Turn on : 25.6970
Width : 3.825
Height : 10.057
Entry
ampl
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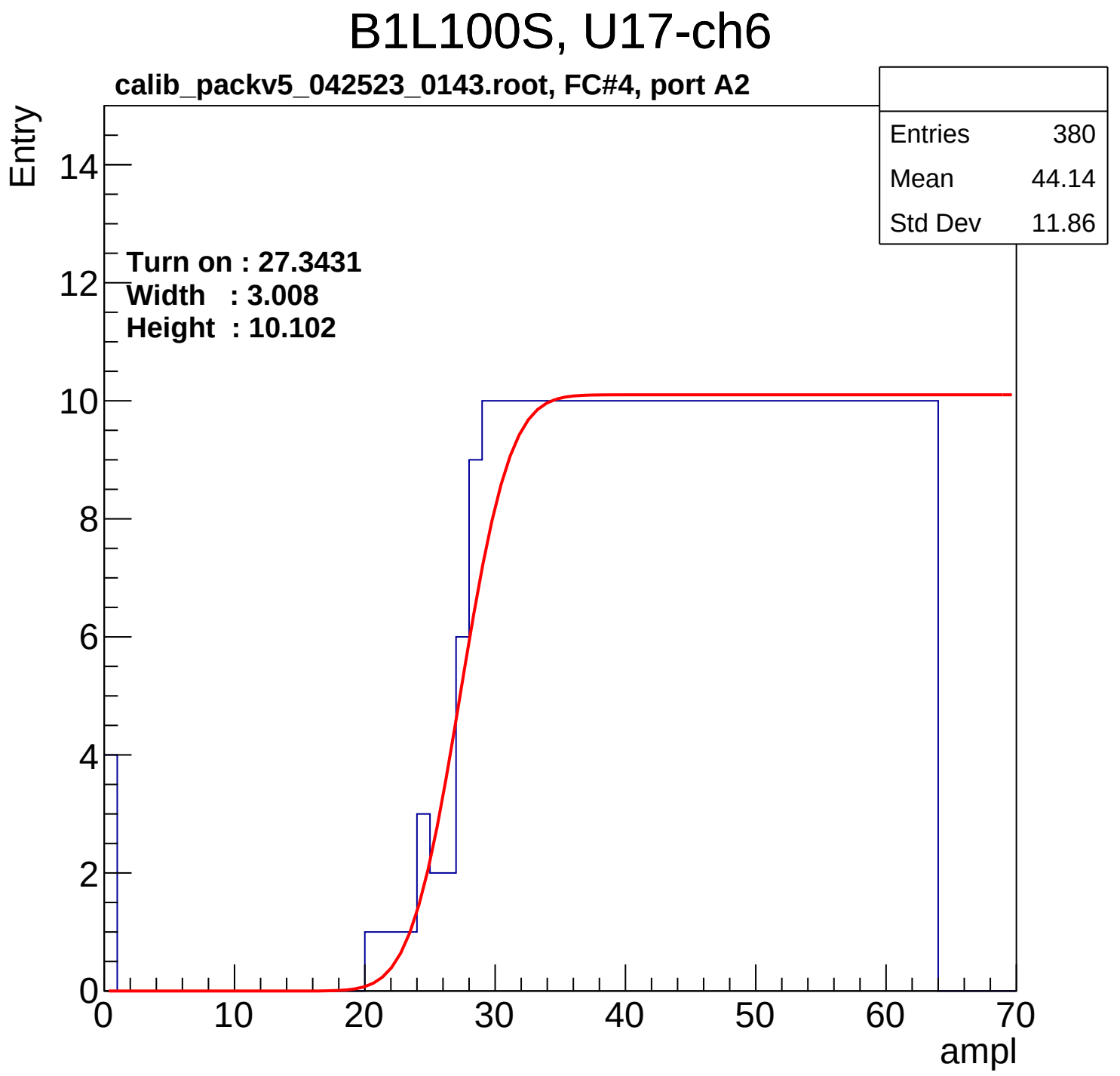
B1L100S, U17-ch6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 380
Mean 44.14
Std Dev 11.86
Turn on : 27.3431
Width : 3.008
Height : 10.102
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ampl
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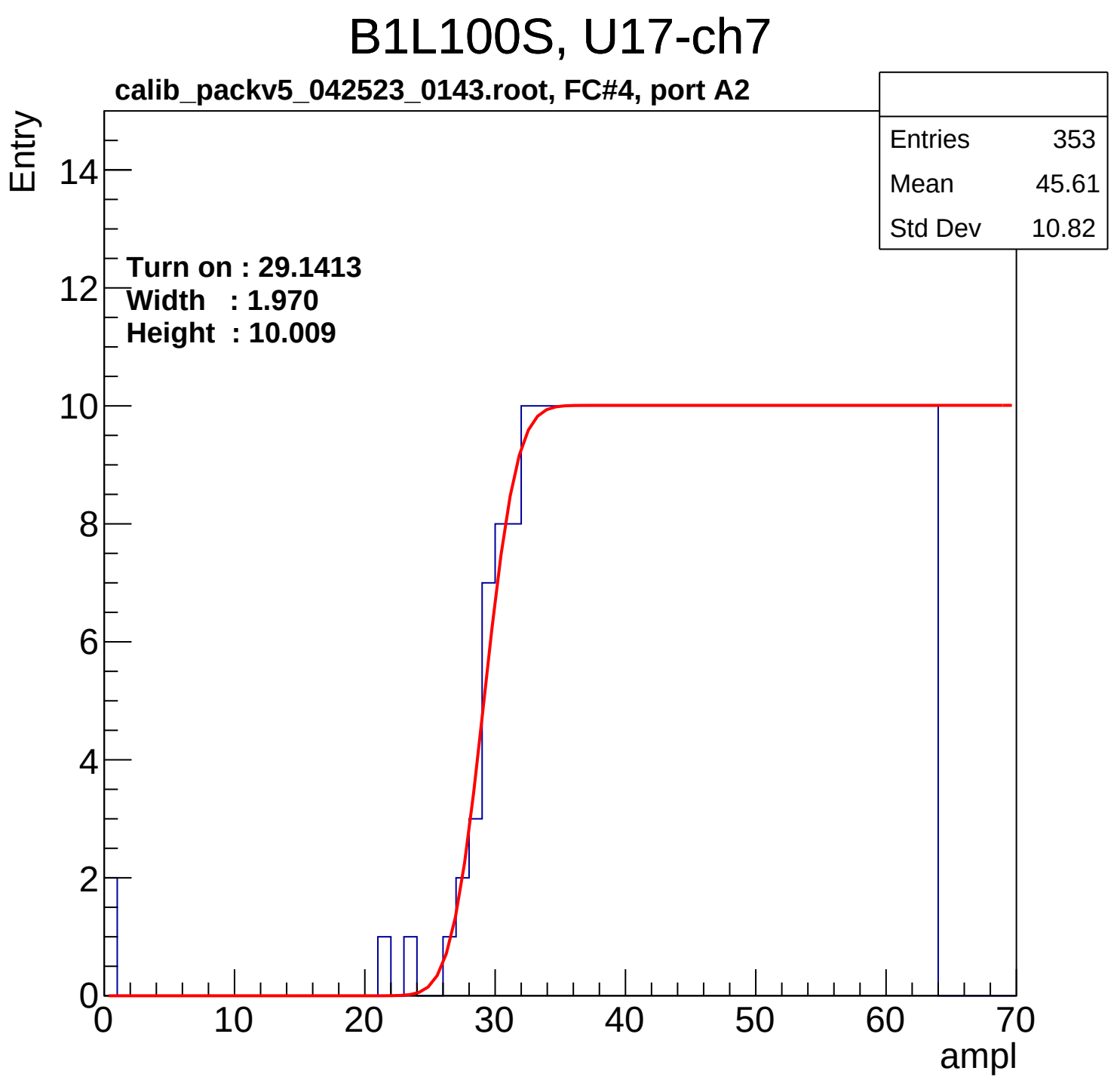
B1L100S, U17-ch7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 353
Mean 45.61
Std Dev 10.82
Turn on : 29.1413
Width : 1.970
Height : 10.009
Entry
ampl
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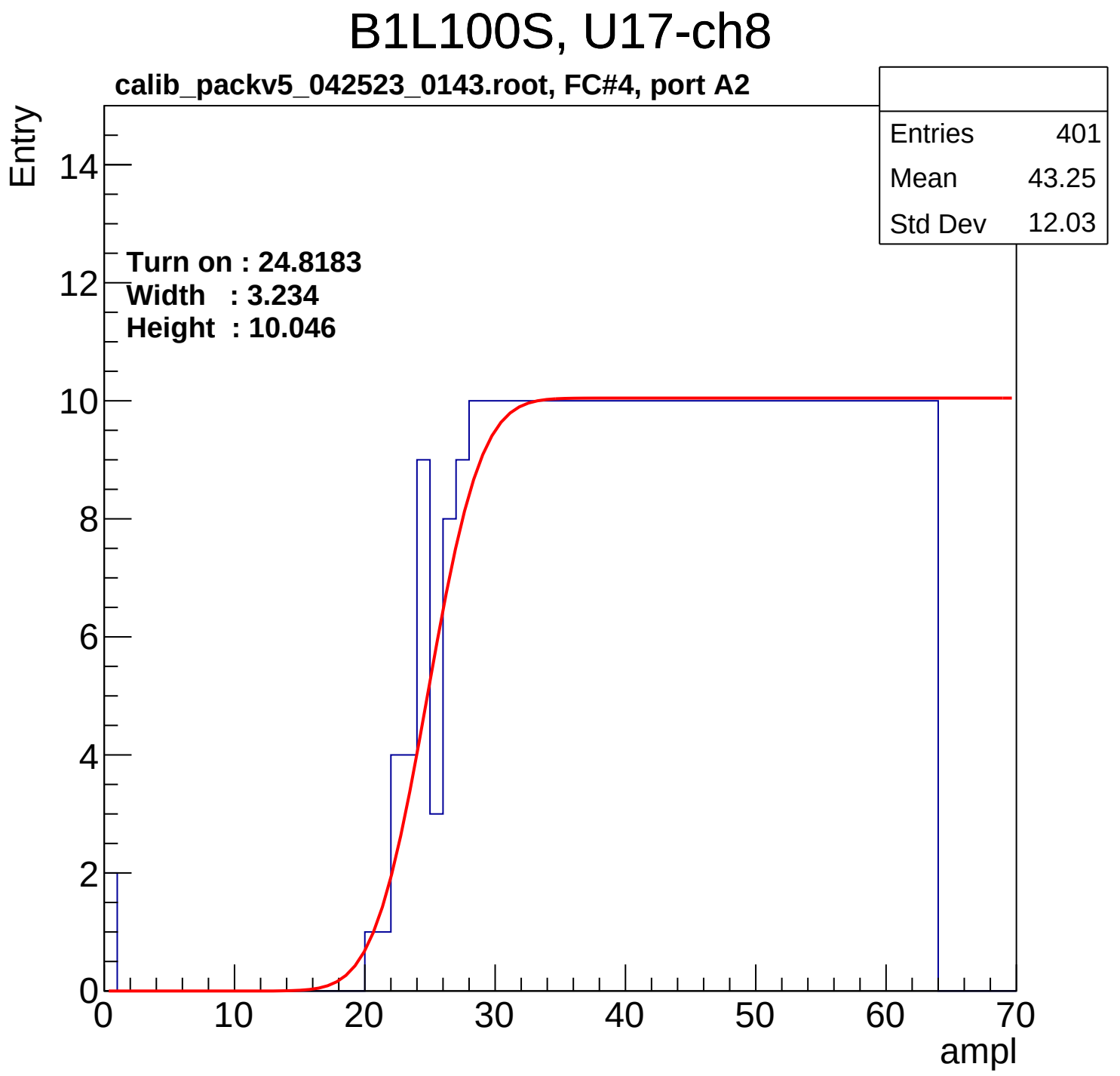
B1L100S, U17-ch8
calib_packv5_042523_0143.root, FC#4, port A2
Entries 401
Mean 43.25
Std Dev 12.03
Turn on : 24.8183
Width : 3.234
Height : 10.046
Entry
ampl
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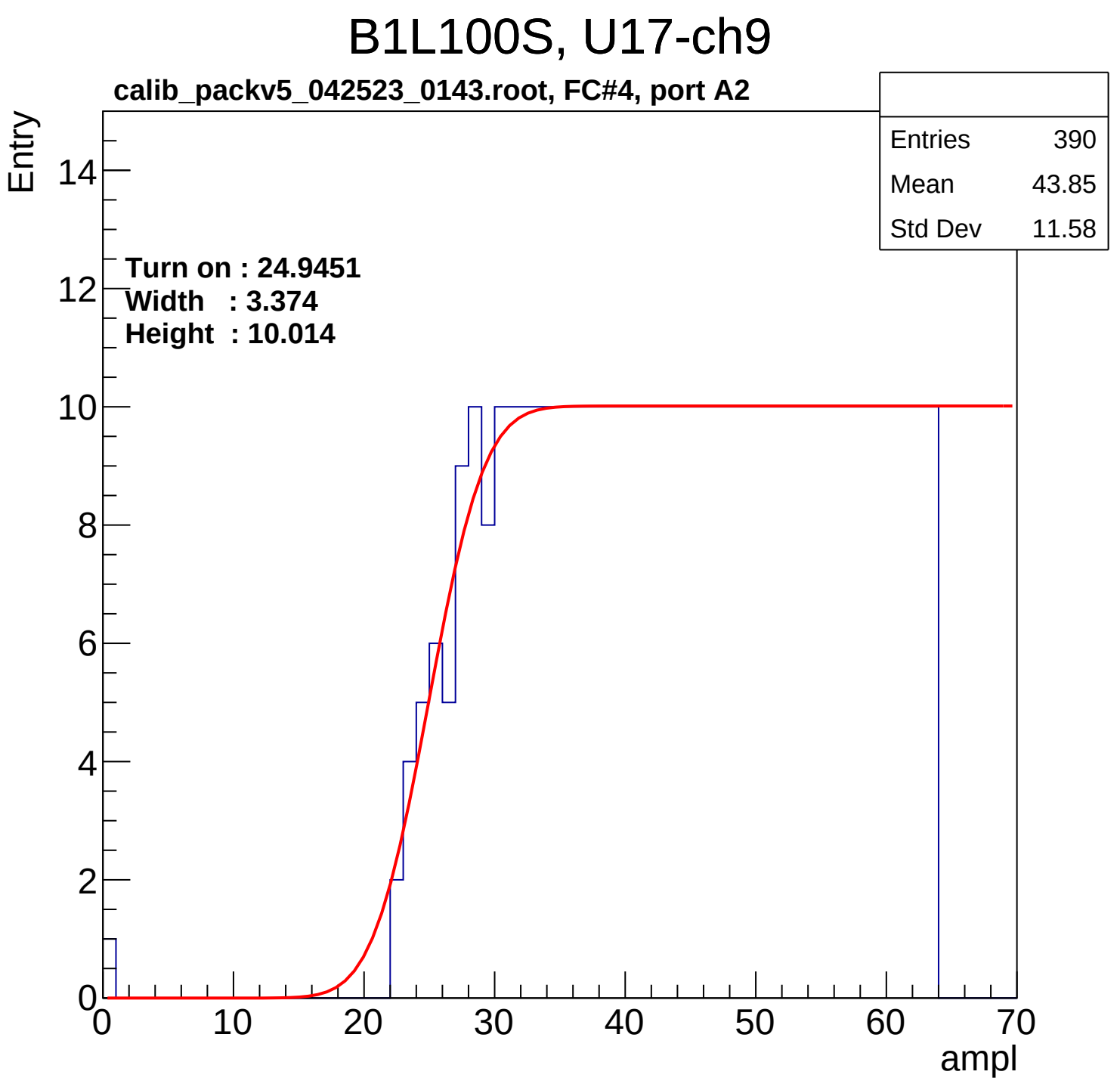
B1L100S, U17-ch9
calib_packv5_042523_0143.root, FC#4, port A2
Entries 390
Mean 43.85
Std Dev 11.58
Turn on : 24.9451
Width : 3.374
Height : 10.014
Entry
ampl
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6
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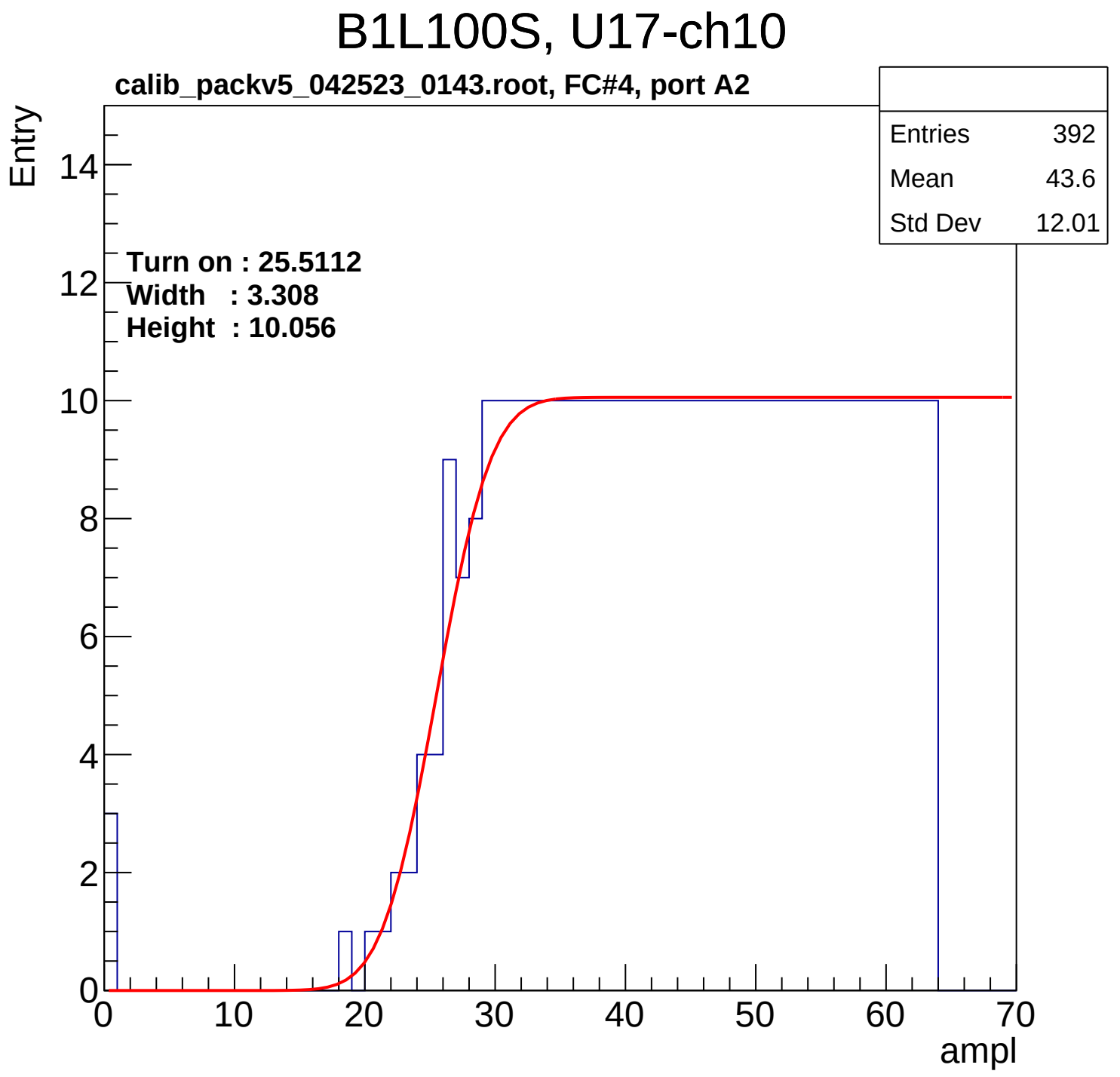
B1L100S, U17-ch10
calib_packv5_042523_0143.root, FC#4, port A2
Entries 392
Mean 43.6
Std Dev 12.01
Turn on : 25.5112
Width : 3.308
Height : 10.056
Entry
ampl
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6
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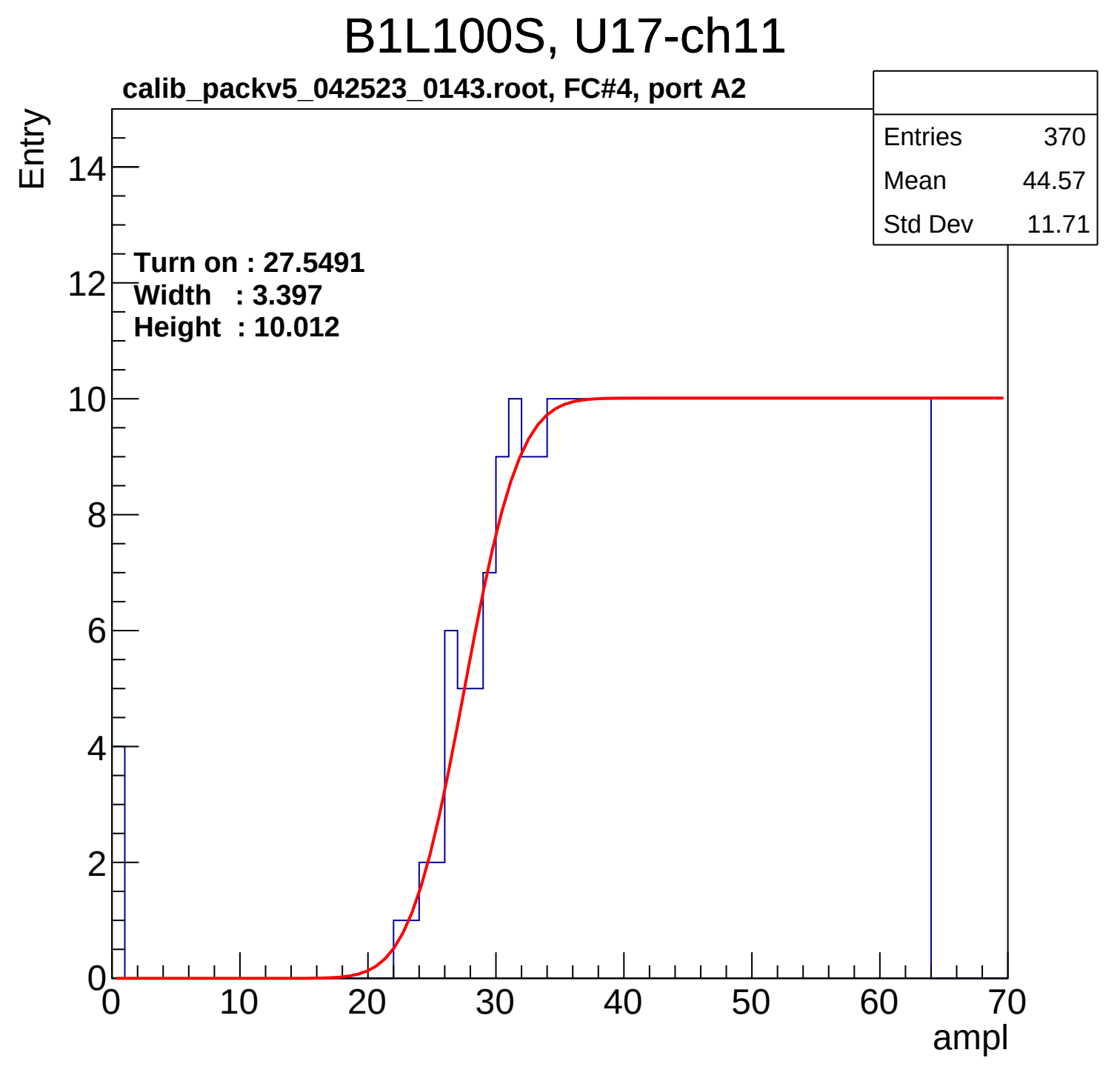
B1L100S, U17-ch11
calib_packv5_042523_0143.root, FC#4, port A2
Entries 370
Mean 44.57
Std Dev 11.71
Turn on : 27.5491
Width : 3.397
Height : 10.012
Entry
ampl
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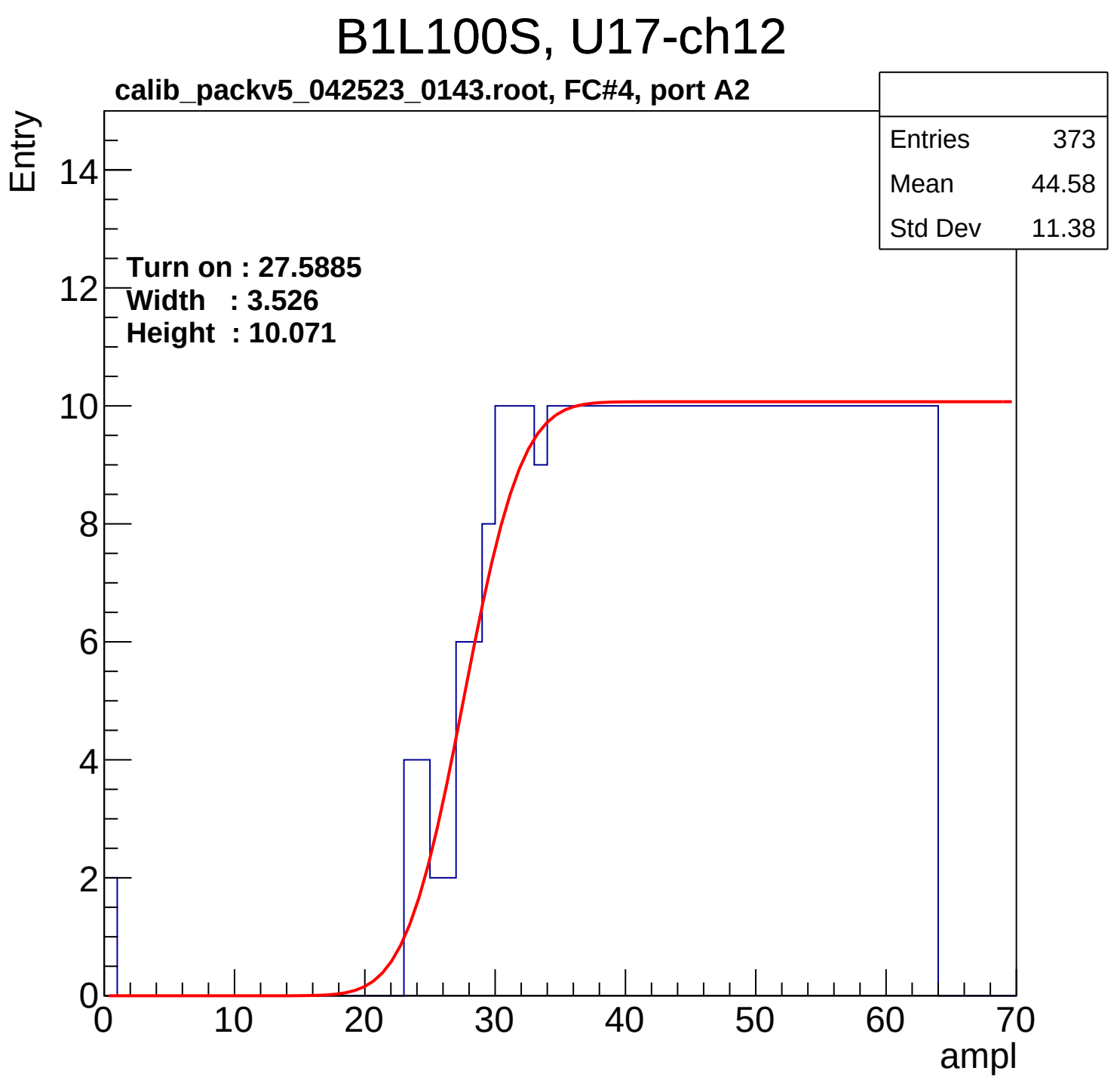
B1L100S, U17-ch12
calib_packv5_042523_0143.root, FC#4, port A2
Entries 373
Mean 44.58
Std Dev 11.38
Turn on : 27.5885
Width : 3.526
Height : 10.071
Entry
ampl
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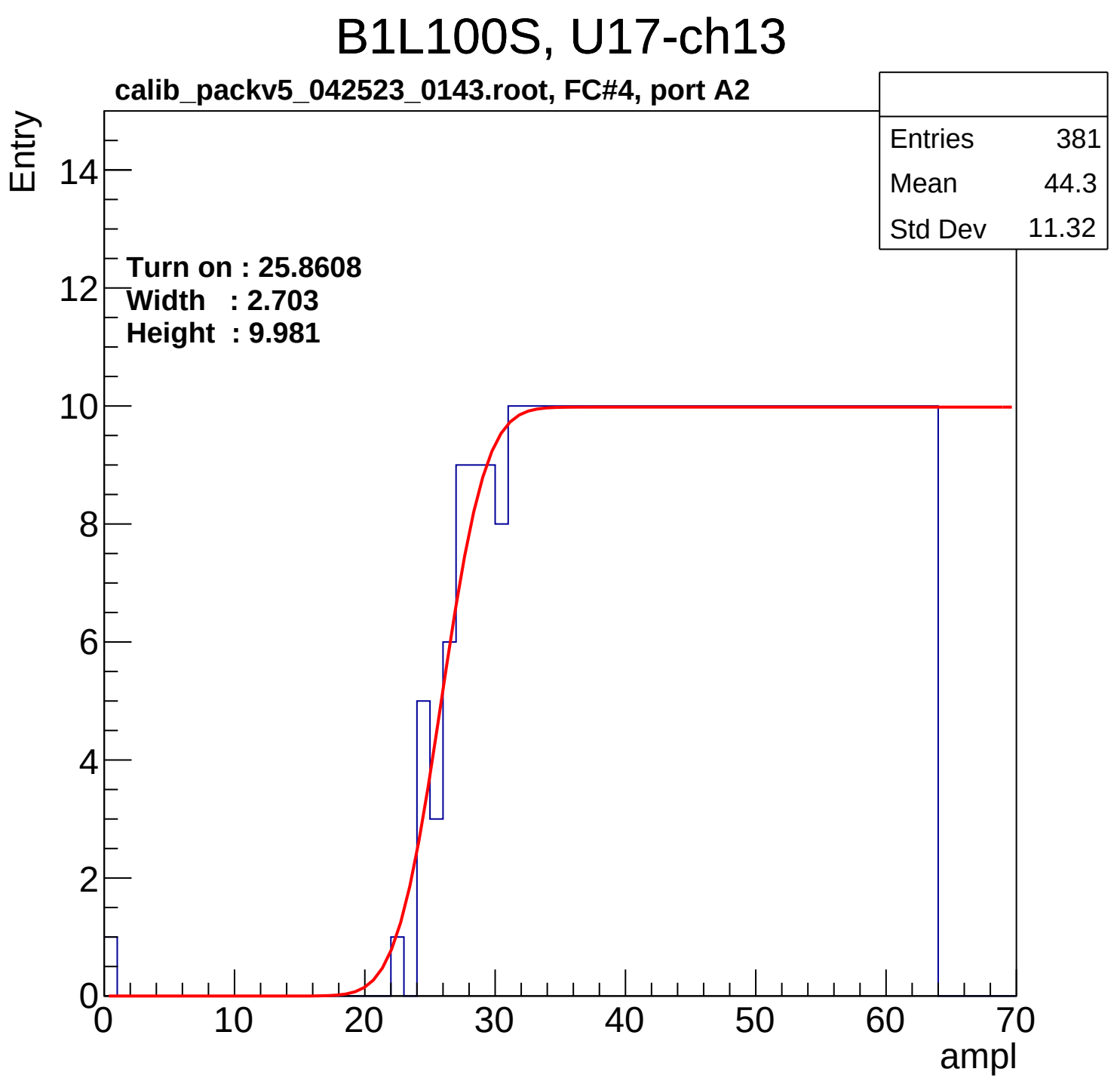
B1L100S, U17-ch13
calib_packv5_042523_0143.root, FC#4, port A2
Entries 381
Mean 44.3
Std Dev 11.32
Turn on : 25.8608
Width : 2.703
Height : 9.981
Entry
ampl
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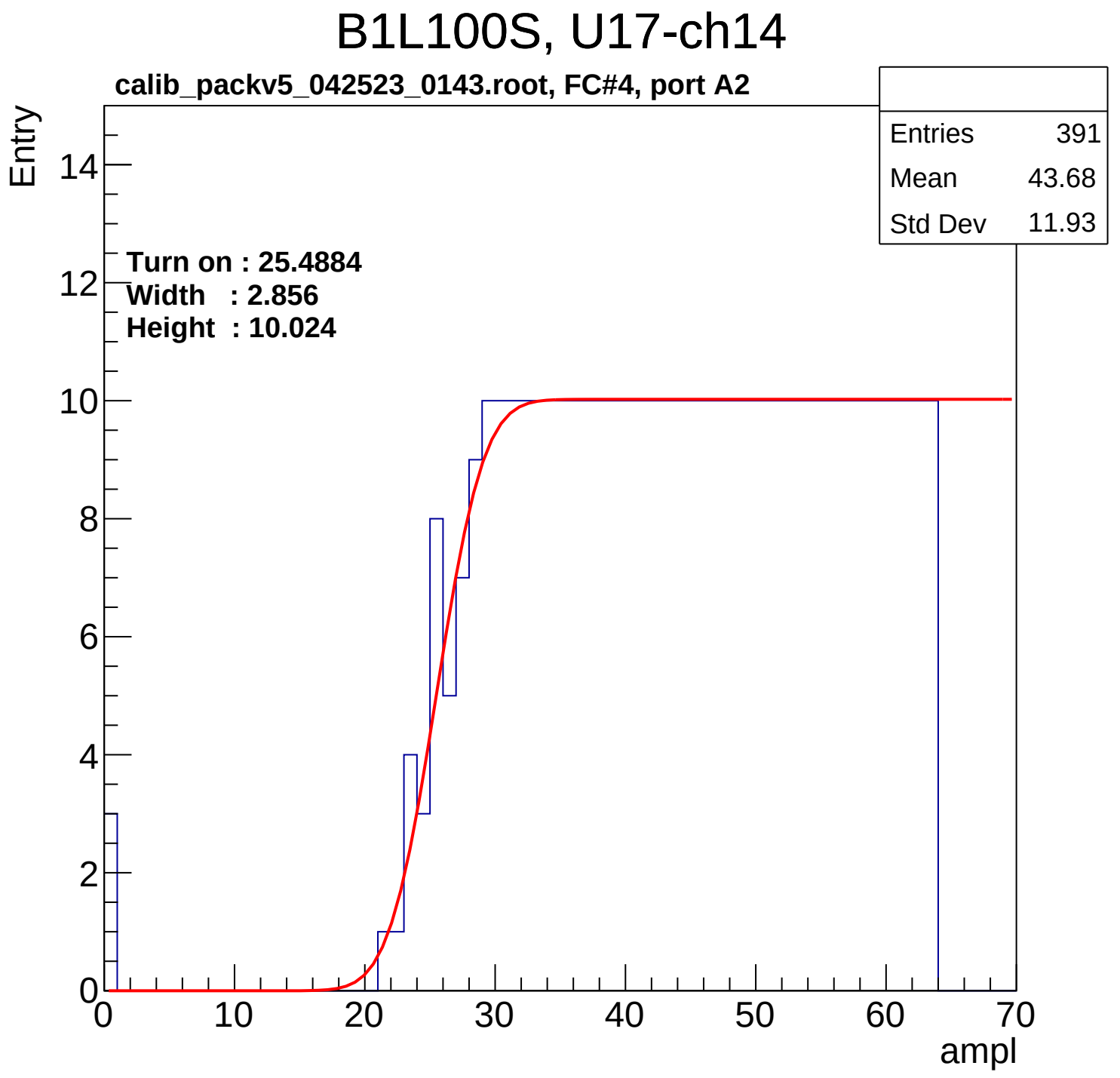
B1L100S, U17-ch14
calib_packv5_042523_0143.root, FC#4, port A2
Entries 391
Mean 43.68
Std Dev 11.93
Turn on : 25.4884
Width : 2.856
Height : 10.024
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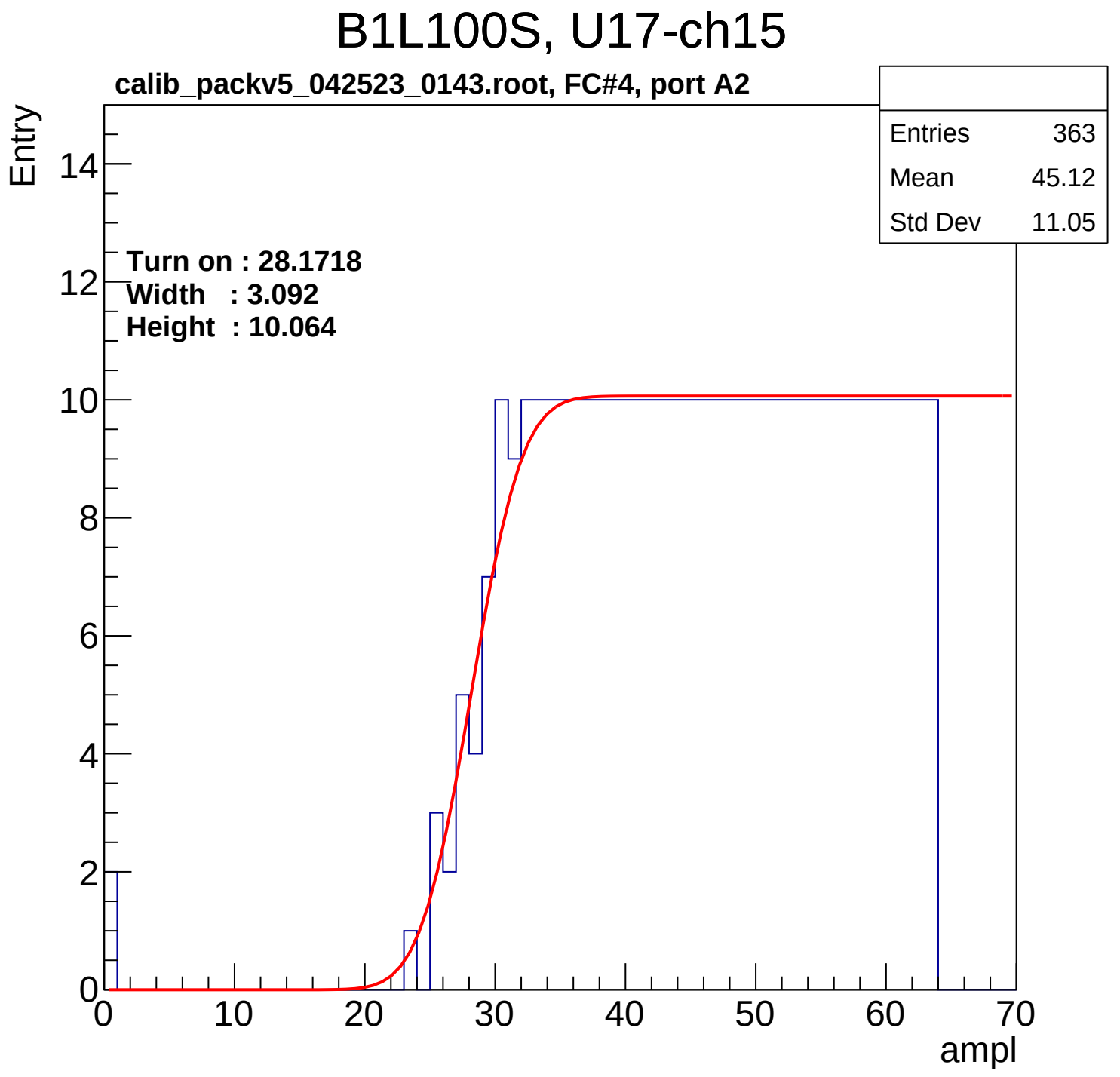
B1L100S, U17-ch15
calib_packv5_042523_0143.root, FC#4, port A2
Entries 363
Mean 45.12
Std Dev 11.05
Turn on : 28.1718
Width : 3.092
Height : 10.064
Entry
ampl
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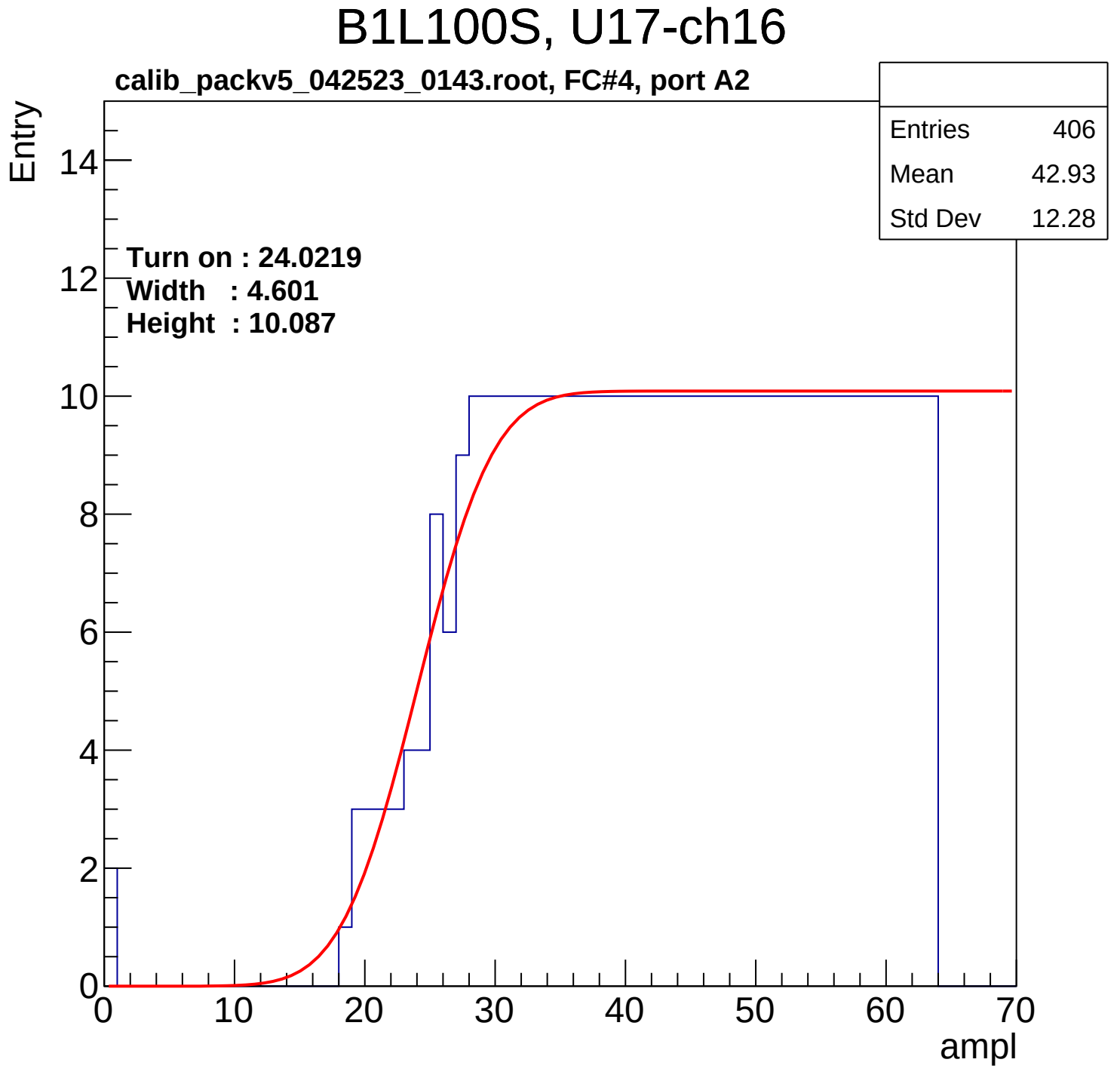
B1L100S, U17-ch16
calib_packv5_042523_0143.root, FC#4, port A2
Entries 406
Mean 42.93
Std Dev 12.28
Turn on : 24.0219
Width : 4.601
Height : 10.087
Entry
ampl
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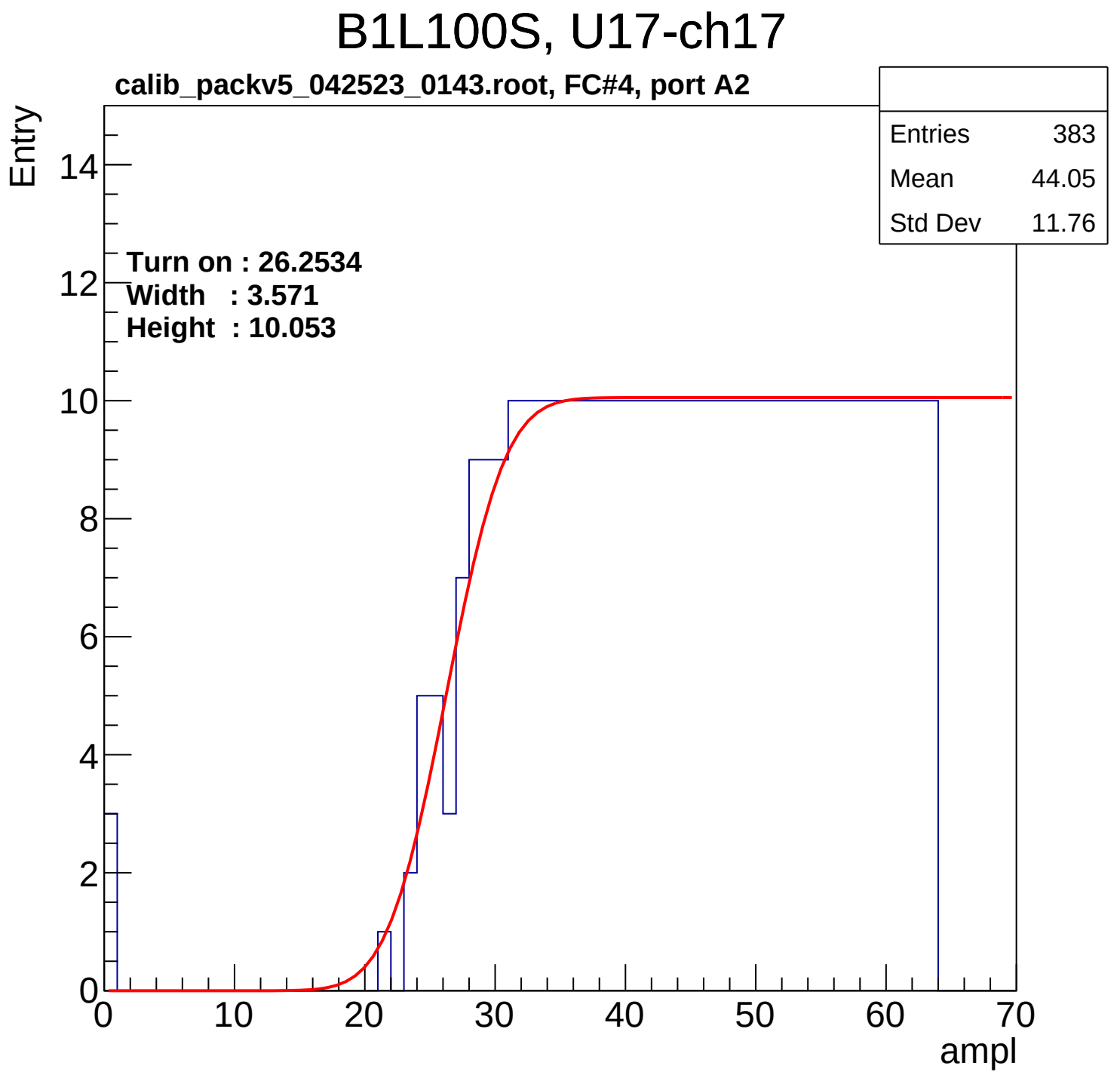
B1L100S, U17-ch17
calib_packv5_042523_0143.root, FC#4, port A2
Entries 383
Mean 44.05
Std Dev 11.76
Turn on : 26.2534
Width : 3.571
Height : 10.053
Entry
ampl
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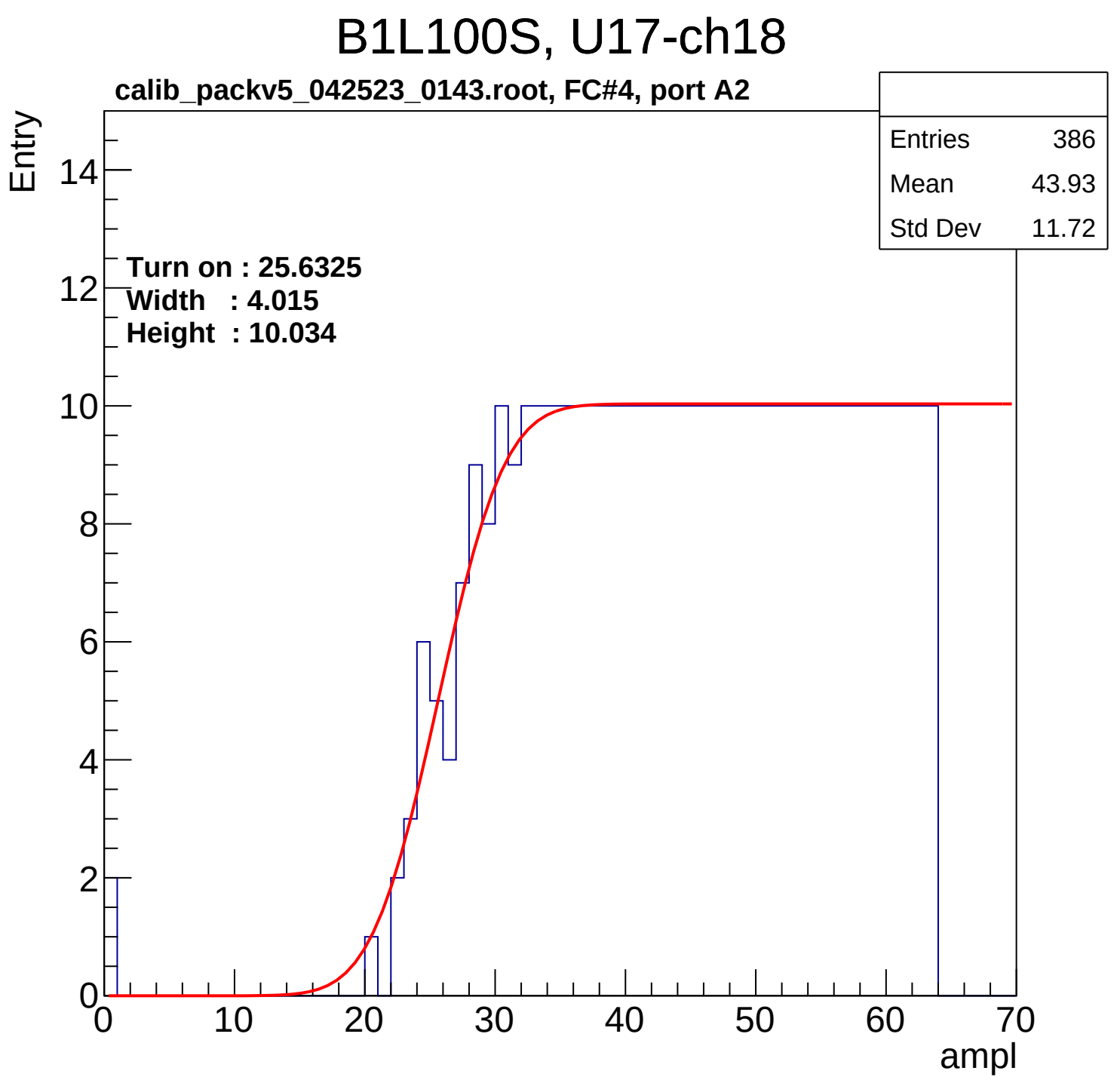
B1L100S, U17-ch18
calib_packv5_042523_0143.root, FC#4, port A2
Entries 386
Mean 43.93
Std Dev 11.72
Turn on : 25.6325
Width : 4.015
Height : 10.034
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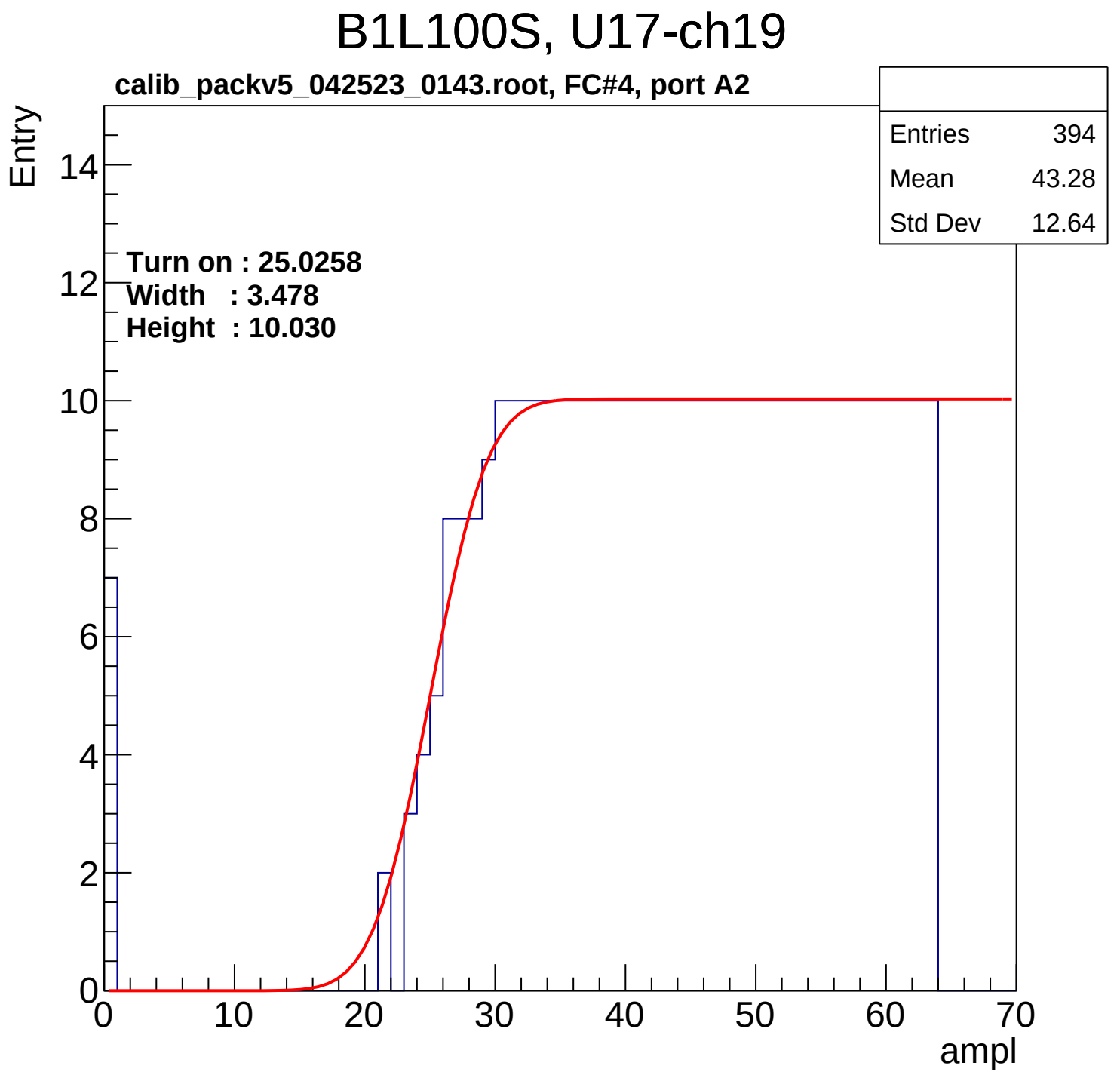
B1L100S, U17-ch19
calib_packv5_042523_0143.root, FC#4, port A2
Entries 394
Mean 43.28
Std Dev 12.64
Turn on : 25.0258
Width : 3.478
Height : 10.030
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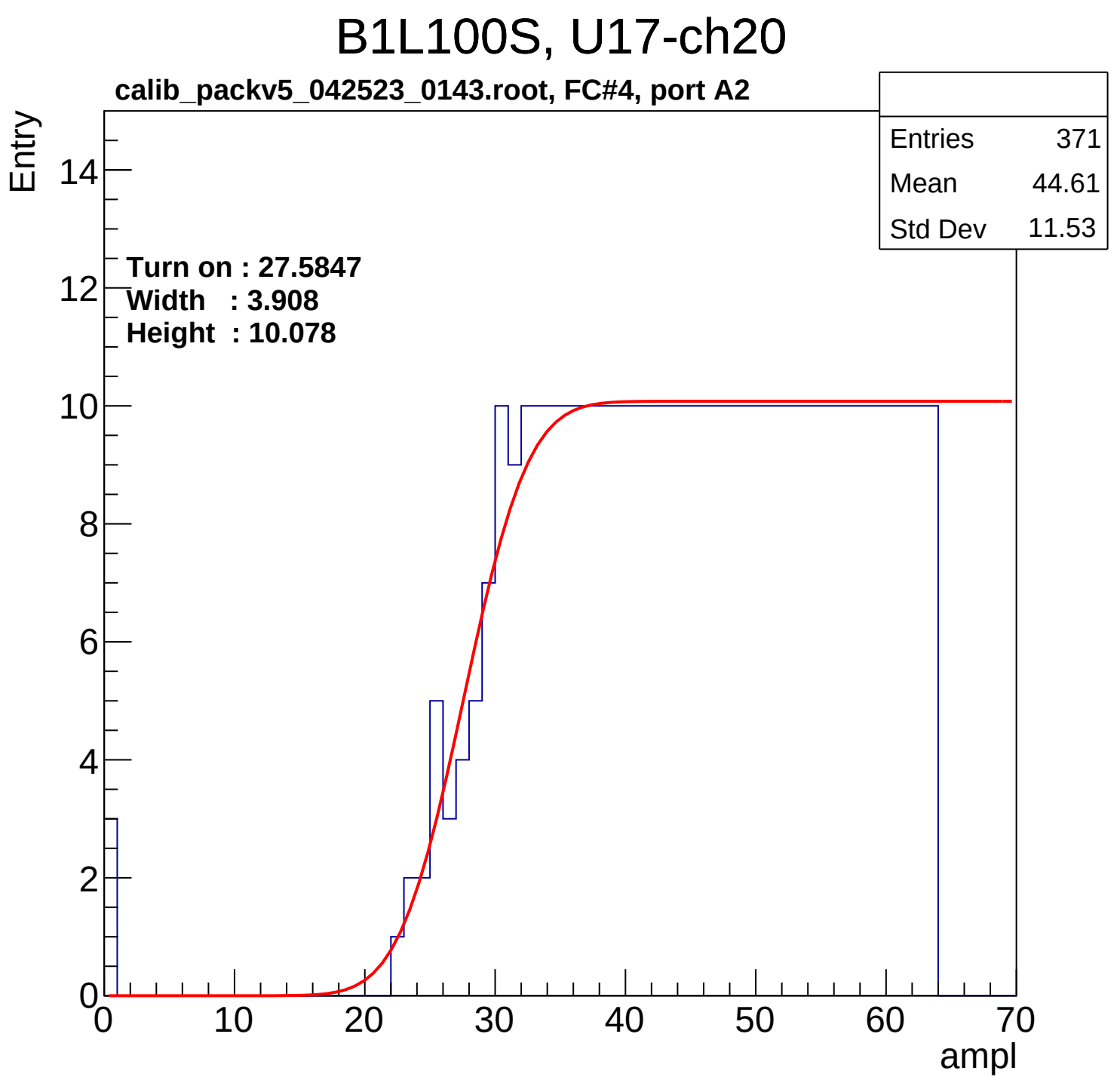
B1L100S, U17-ch20
calib_packv5_042523_0143.root, FC#4, port A2
Entries 371
Mean 44.61
Std Dev 11.53
Turn on : 27.5847
Width : 3.908
Height : 10.078
Entry
ampl
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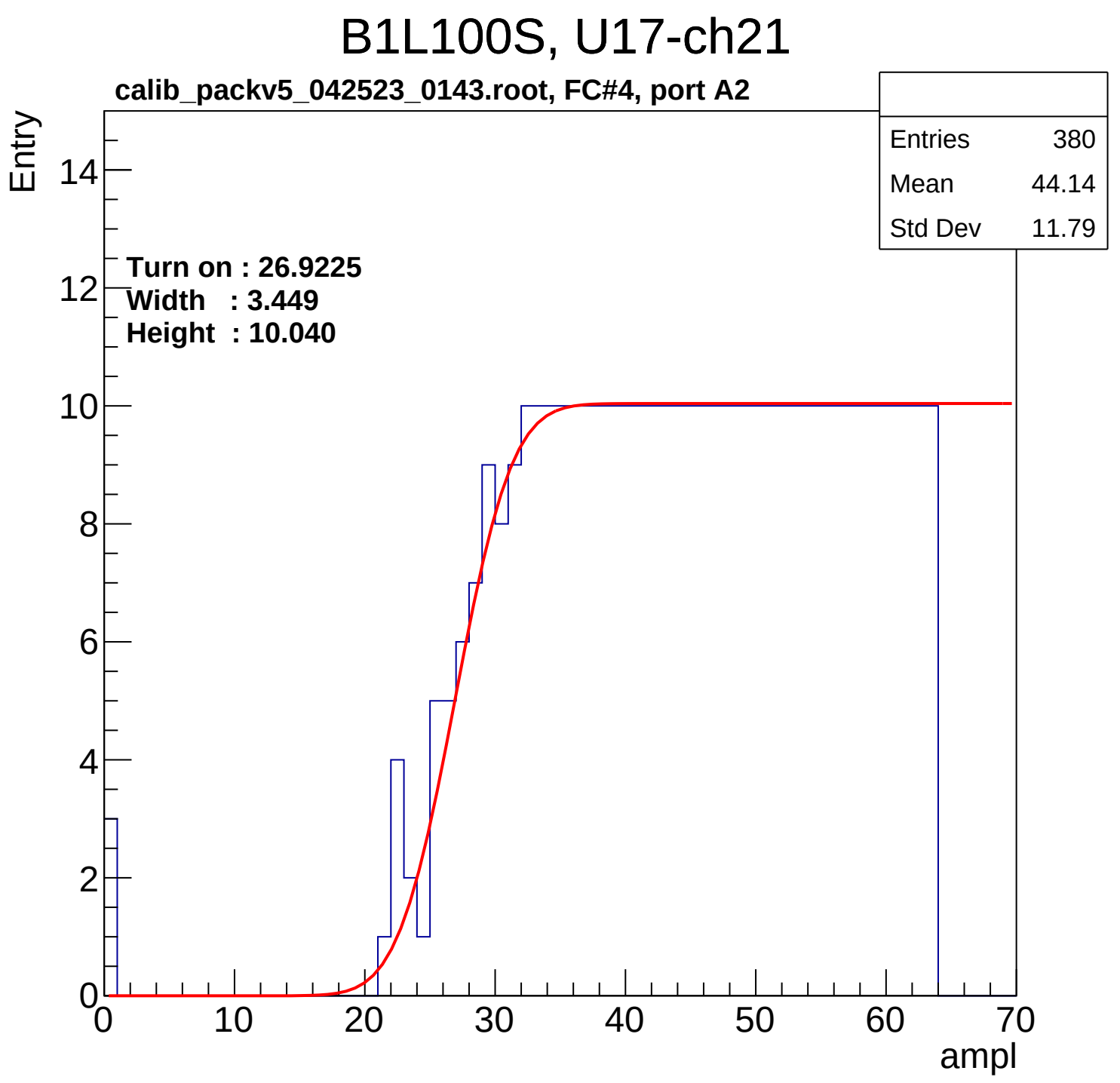
B1L100S, U17-ch21
calib_packv5_042523_0143.root, FC#4, port A2
Entries 380
Mean 44.14
Std Dev 11.79
Turn on : 26.9225
Width : 3.449
Height : 10.040
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ampl
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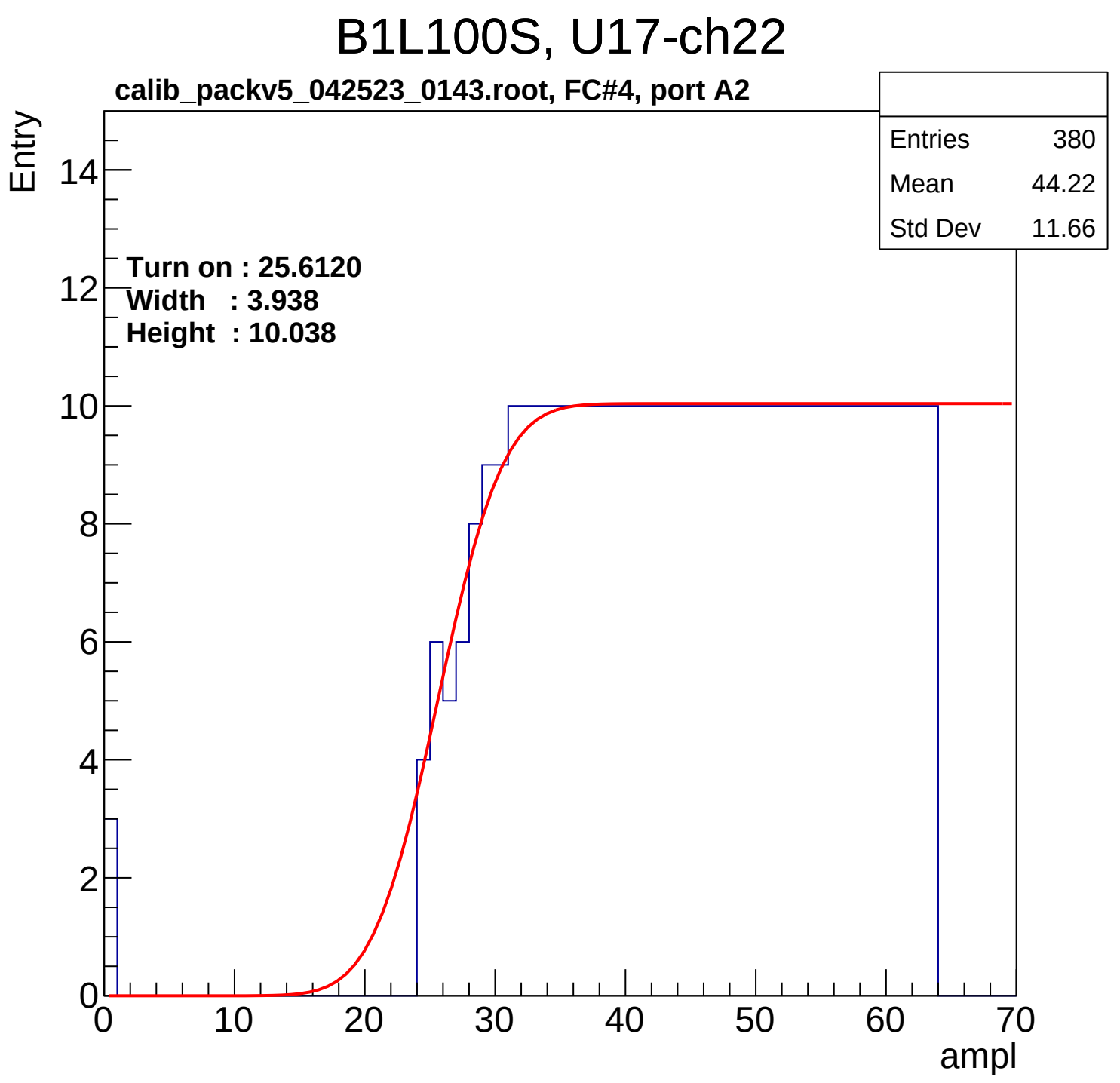
B1L100S, U17-ch22
calib_packv5_042523_0143.root, FC#4, port A2
Entries 380
Mean 44.22
Std Dev 11.66
Turn on : 25.6120
Width : 3.938
Height : 10.038
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ampl
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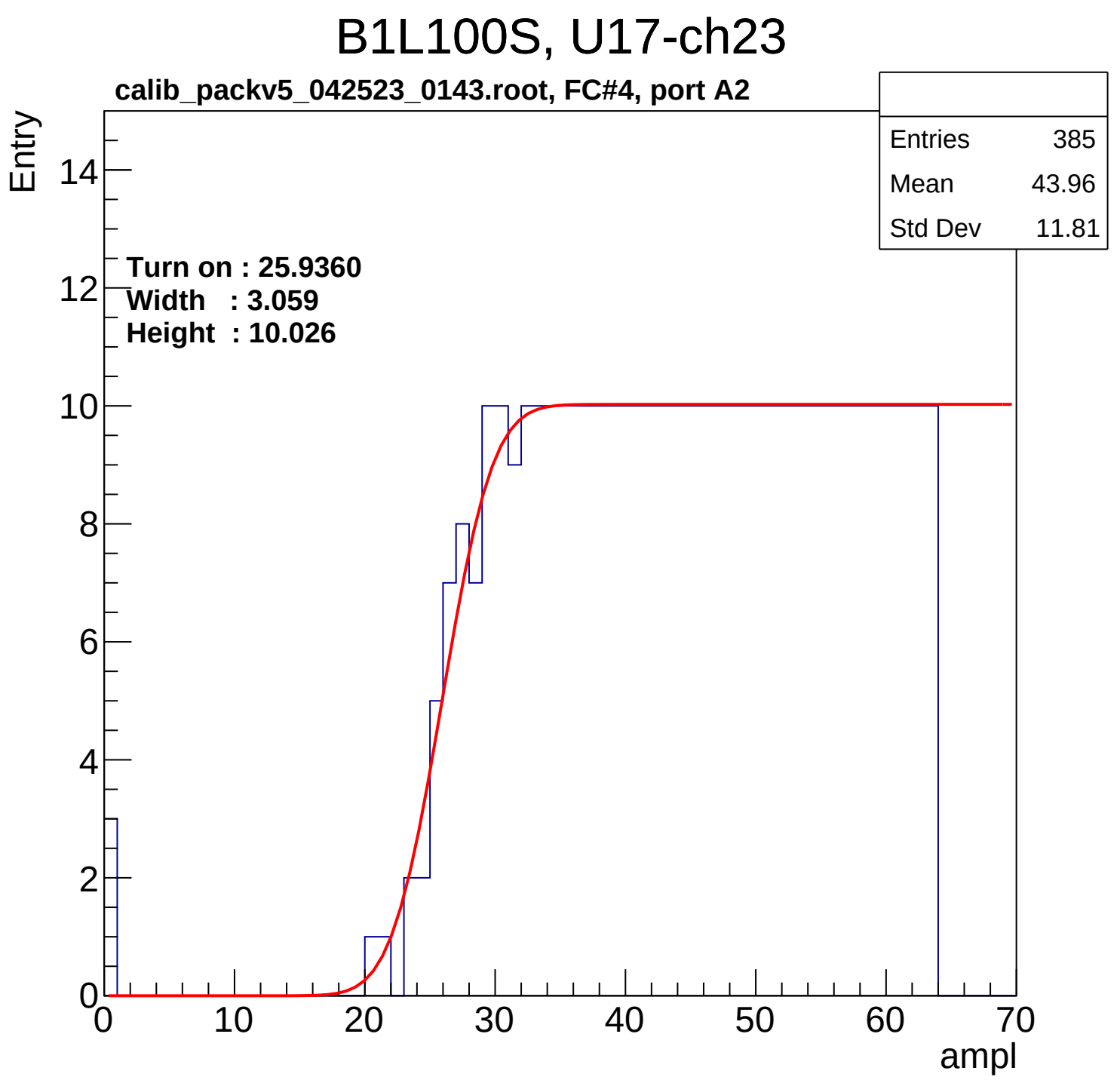
B1L100S, U17-ch23
calib_packv5_042523_0143.root, FC#4, port A2
Entries 385
Mean 43.96
Std Dev 11.81
Turn on : 25.9360
Width : 3.059
Height : 10.026
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ampl
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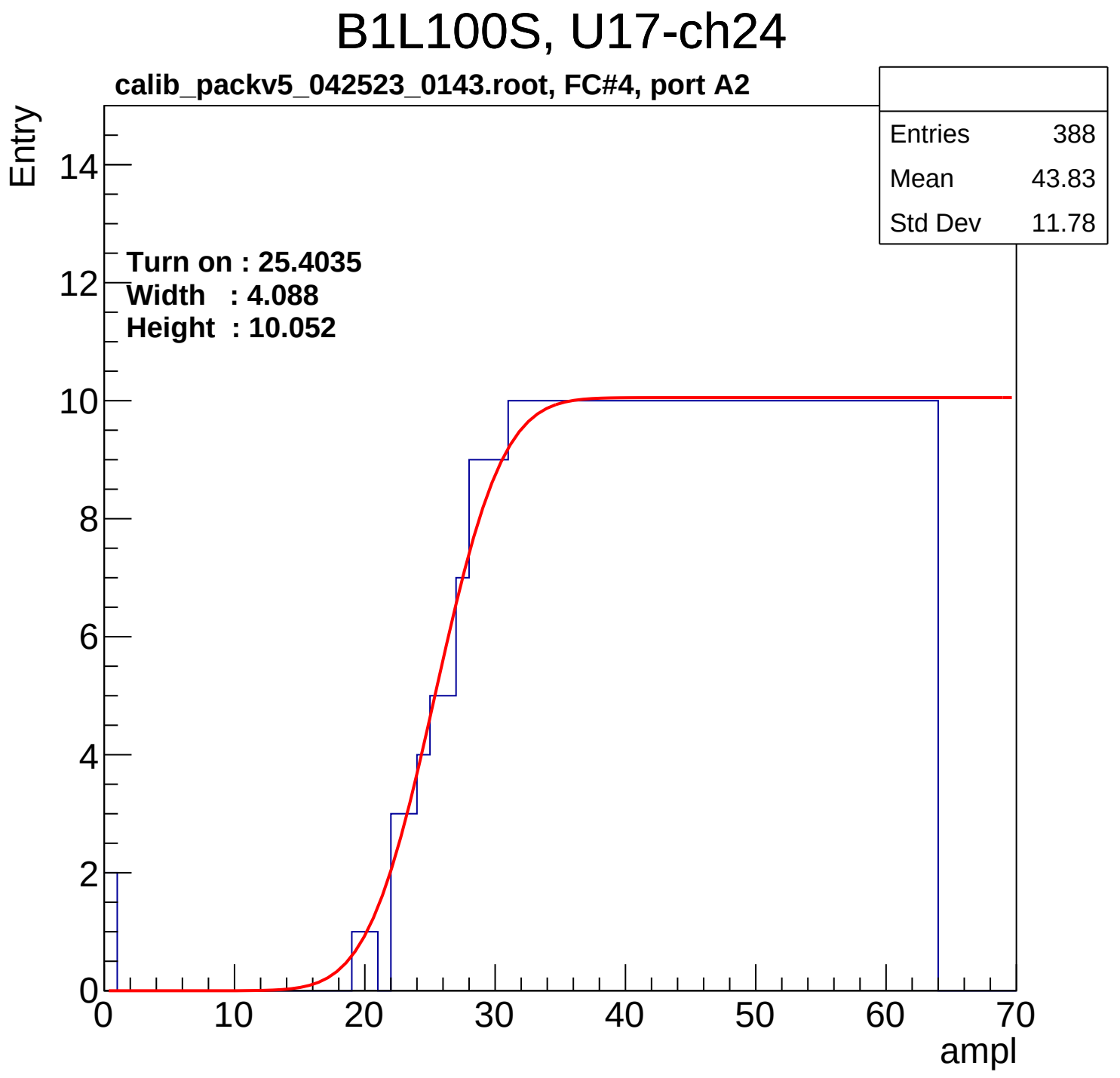
B1L100S, U17-ch24
calib_packv5_042523_0143.root, FC#4, port A2
Entries 388
Mean 43.83
Std Dev 11.78
Turn on : 25.4035
Width : 4.088
Height : 10.052
Entry
ampl
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6
8
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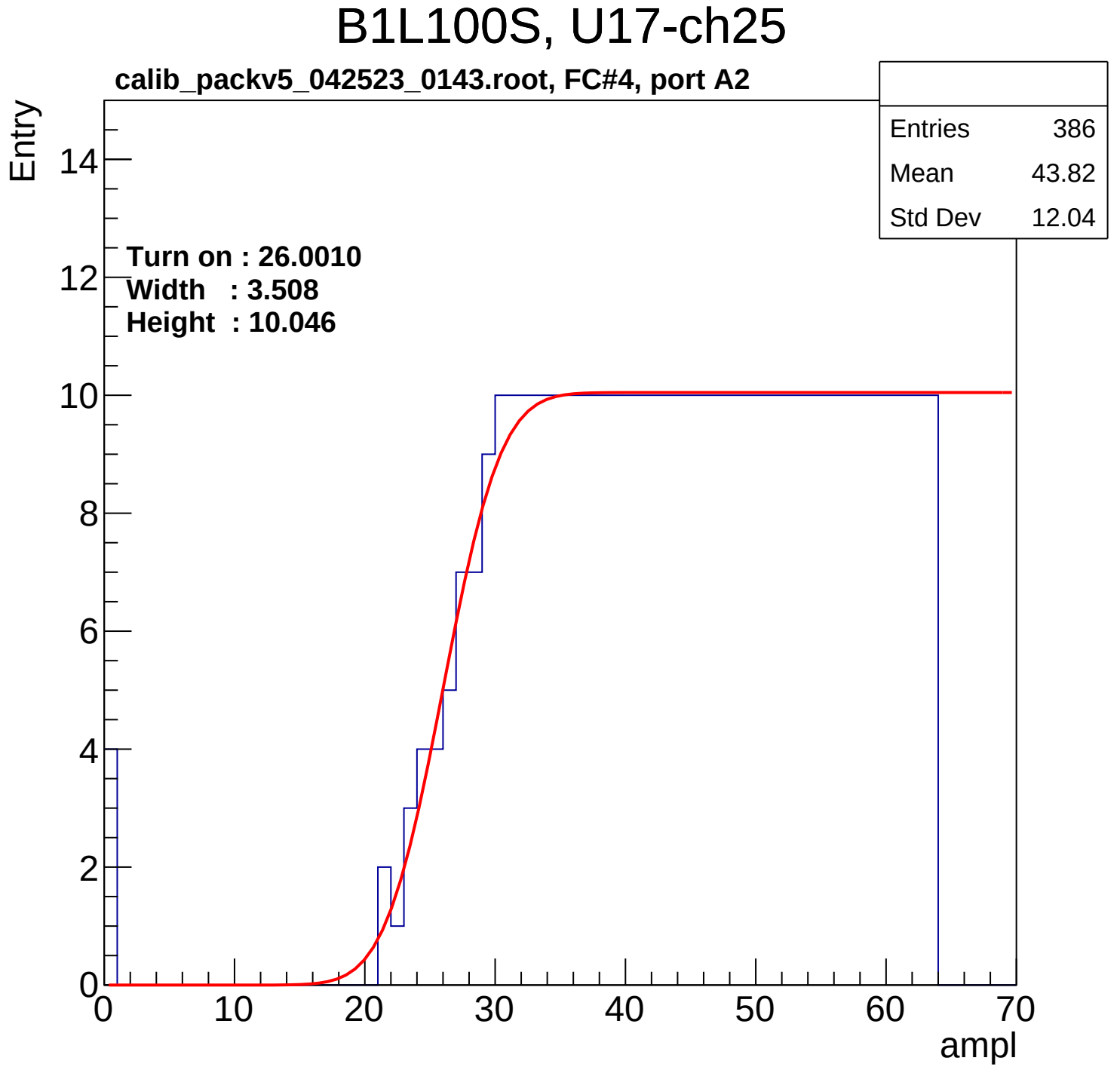
B1L100S, U17-ch25
calib_packv5_042523_0143.root, FC#4, port A2
Entries 386
Mean 43.82
Std Dev 12.04
Turn on : 26.0010
Width : 3.508
Height : 10.046
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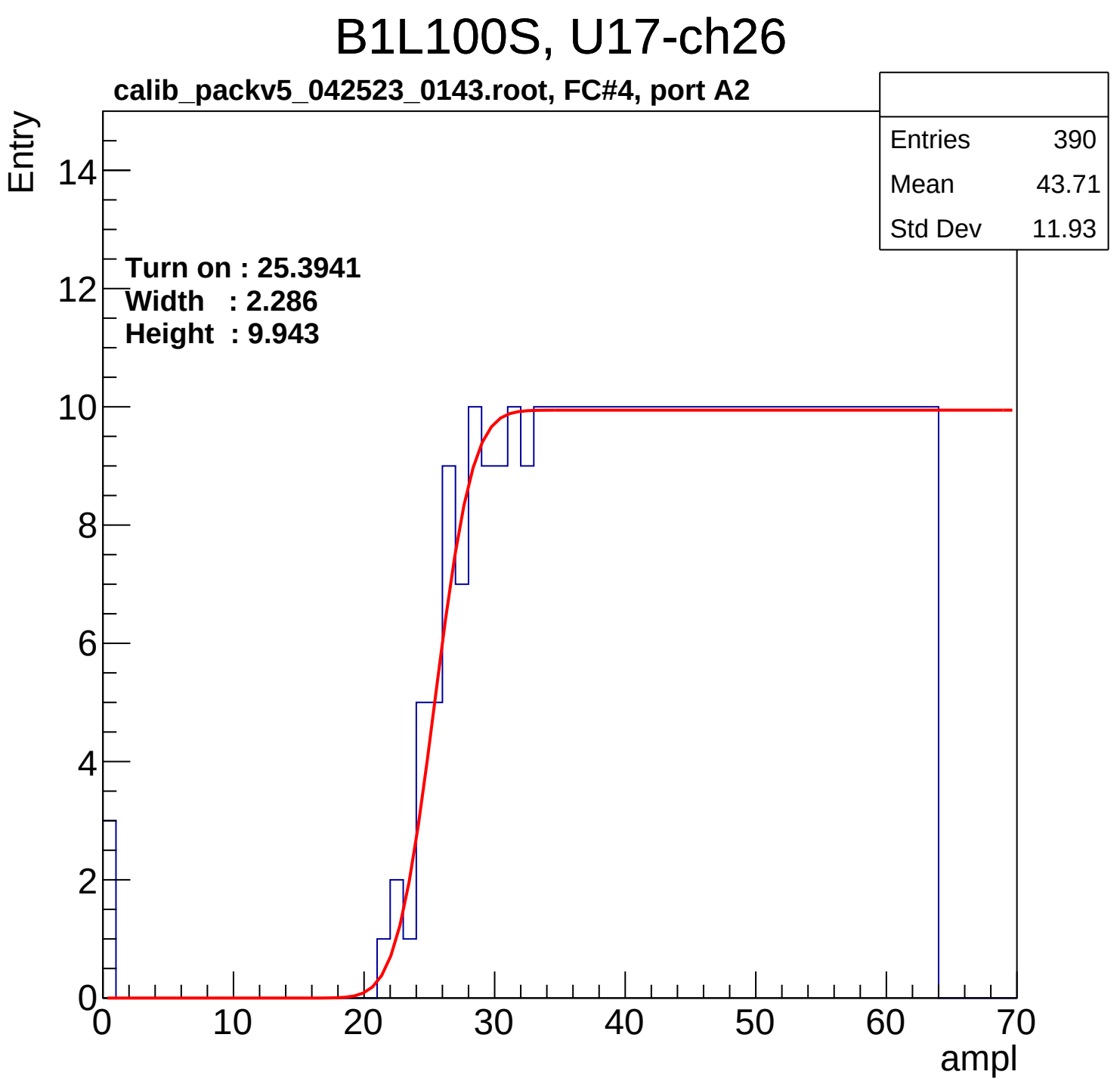
B1L100S, U17-ch26
calib_packv5_042523_0143.root, FC#4, port A2
Entries 390
Mean 43.71
Std Dev 11.93
Turn on : 25.3941
Width : 2.286
Height : 9.943
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ampl
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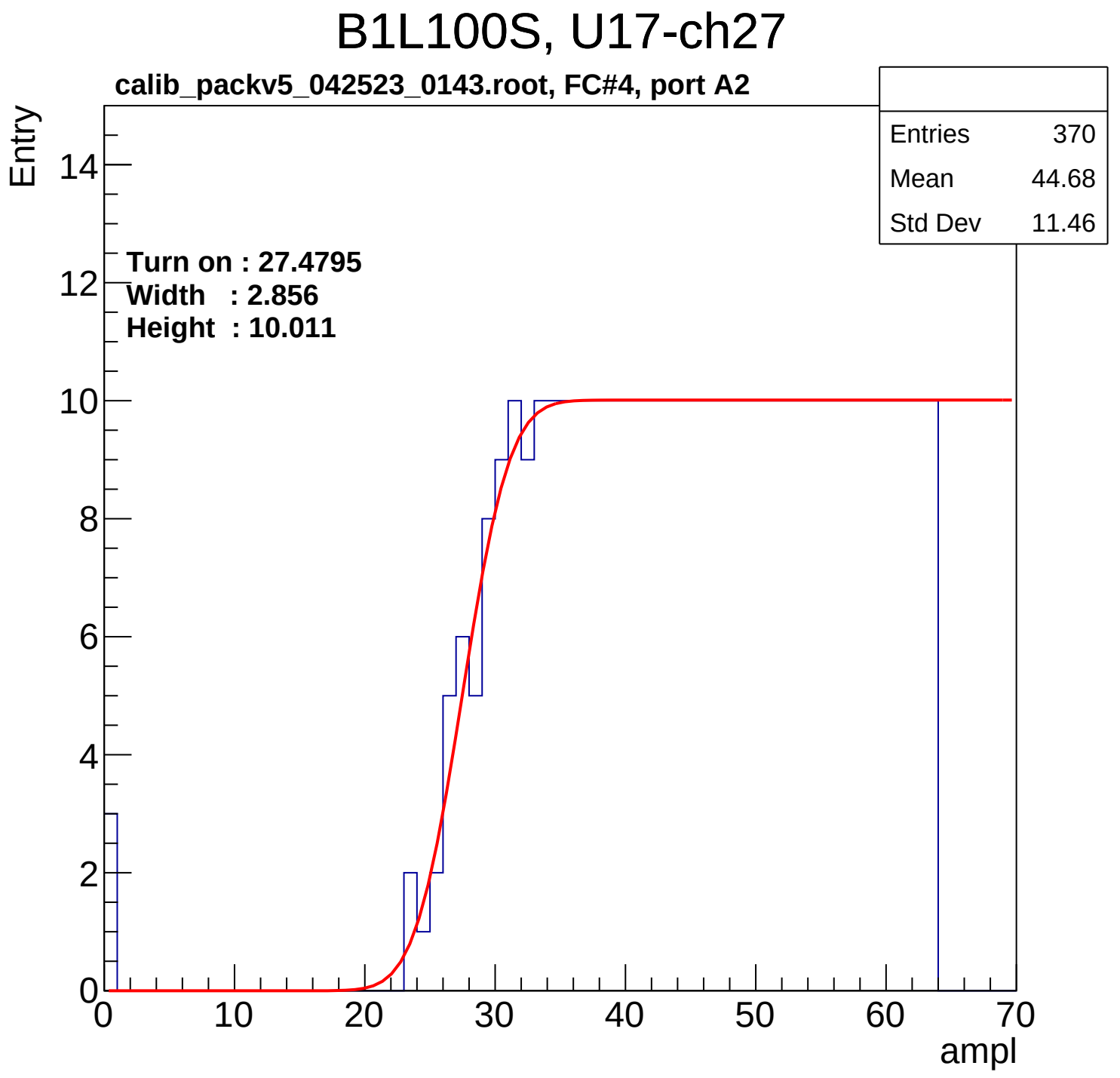
B1L100S, U17-ch27
calib_packv5_042523_0143.root, FC#4, port A2
Entries 370
Mean 44.68
Std Dev 11.46
Turn on : 27.4795
Width : 2.856
Height : 10.011
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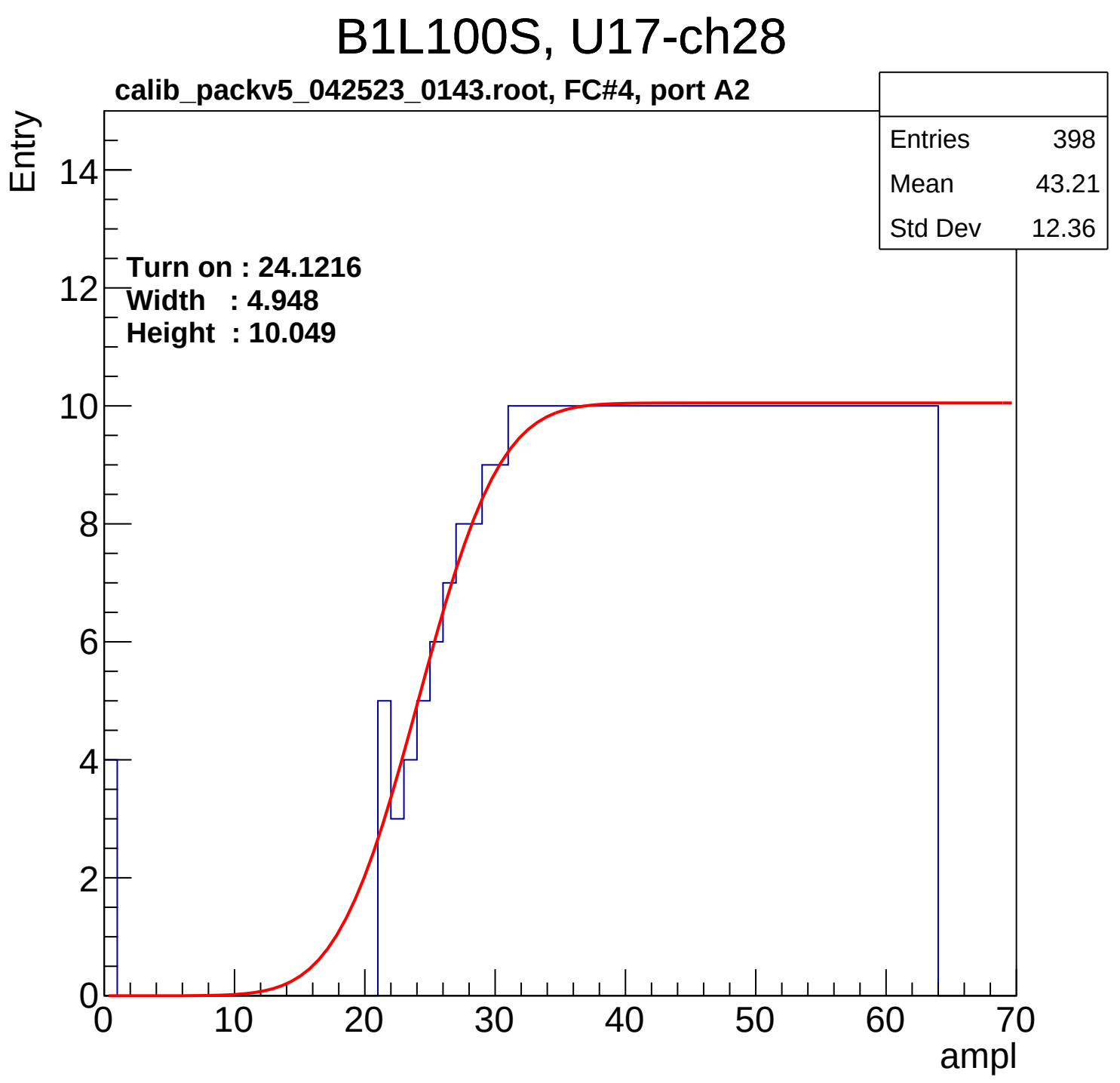
B1L100S, U17-ch28
calib_packv5_042523_0143.root, FC#4, port A2
Entries 398
Mean 43.21
Std Dev 12.36
Turn on : 24.1216
Width : 4.948
Height : 10.049
Entry
ampl
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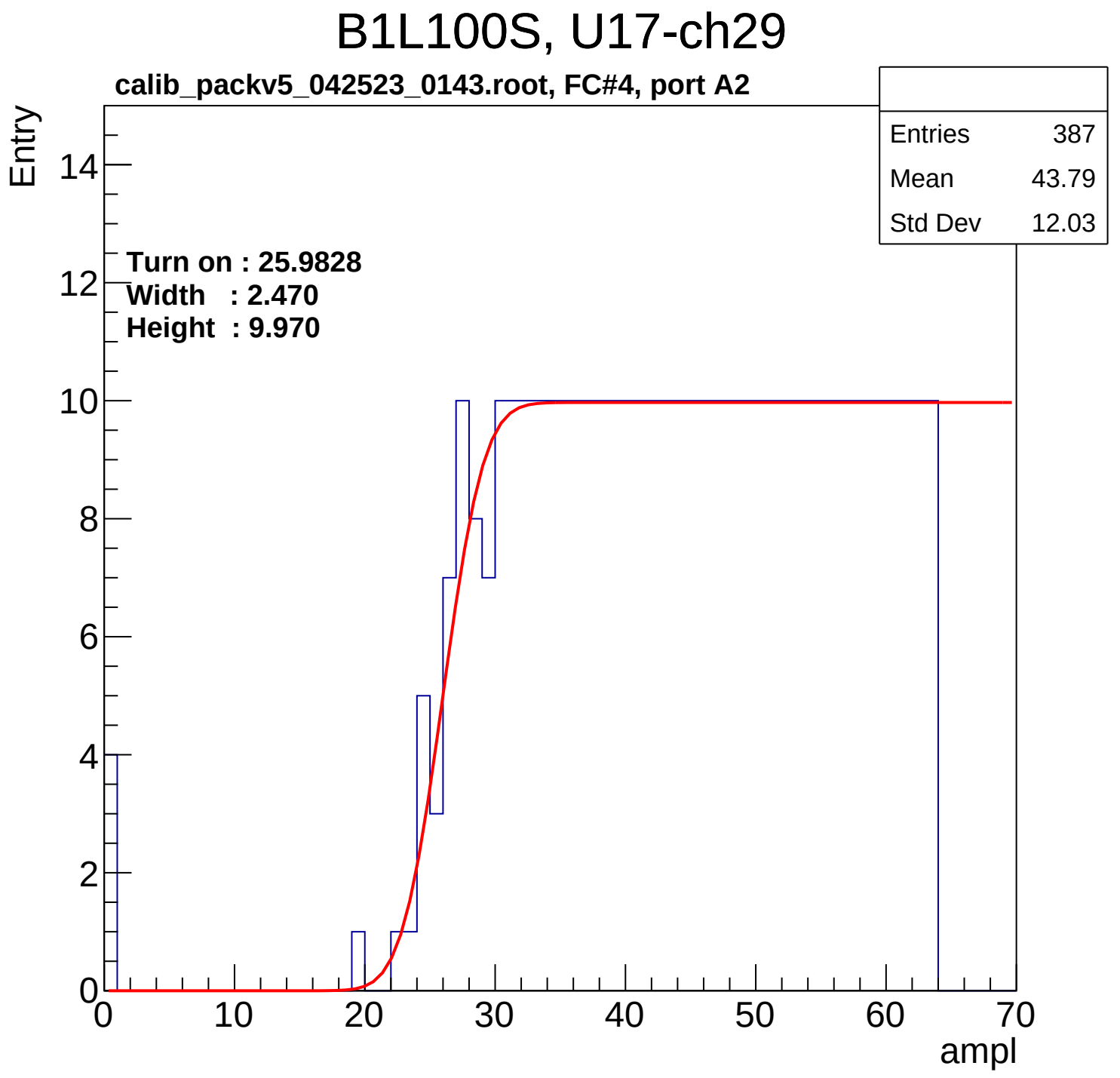
B1L100S, U17-ch29
calib_packv5_042523_0143.root, FC#4, port A2
Entries 387
Mean 43.79
Std Dev 12.03
Turn on : 25.9828
Width : 2.470
Height : 9.970
Entry
ampl
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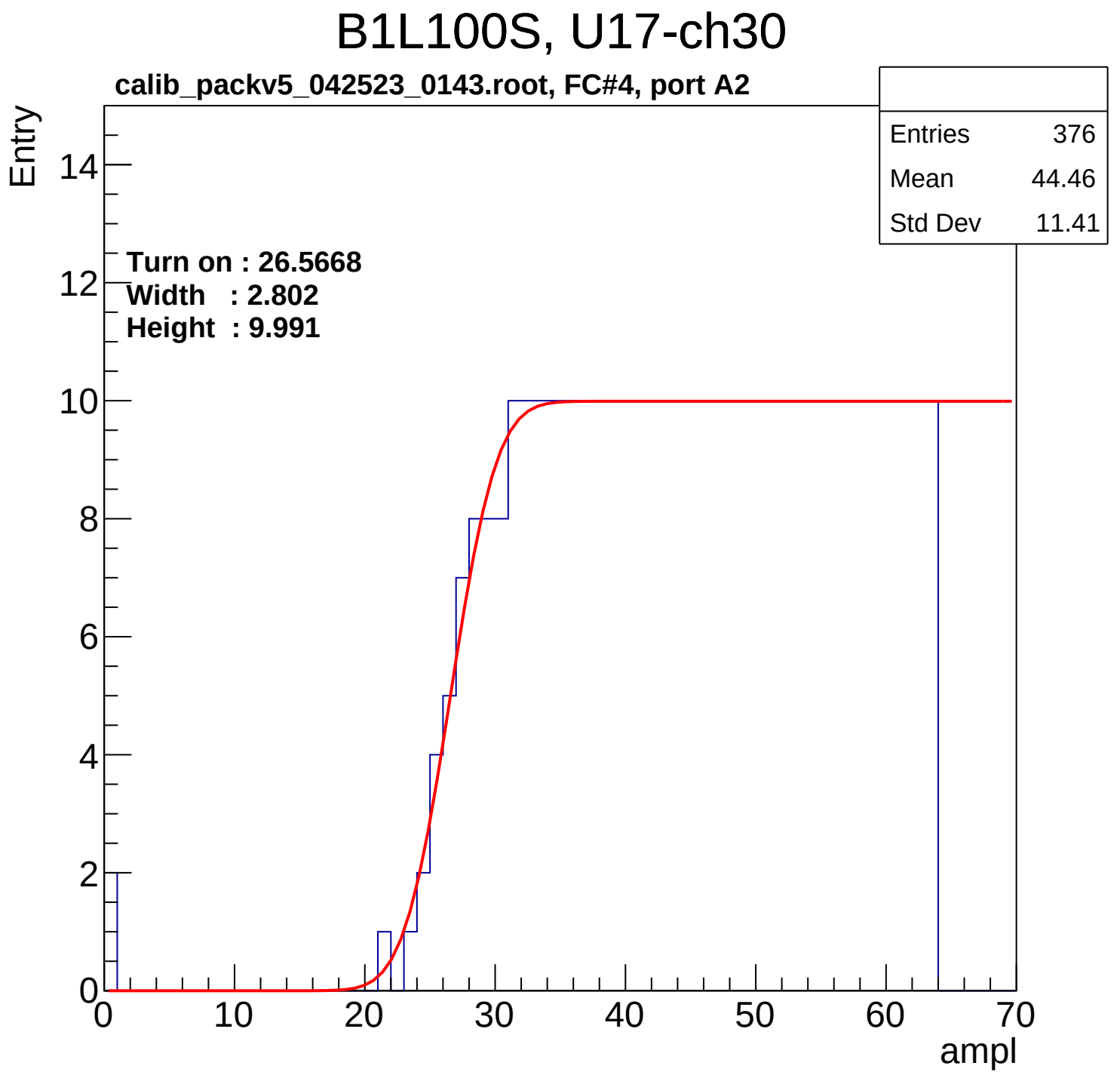
B1L100S, U17-ch30
calib_packv5_042523_0143.root, FC#4, port A2
Entries 376
Mean 44.46
Std Dev 11.41
Turn on : 26.5668
Width : 2.802
Height : 9.991
Entry
ampl
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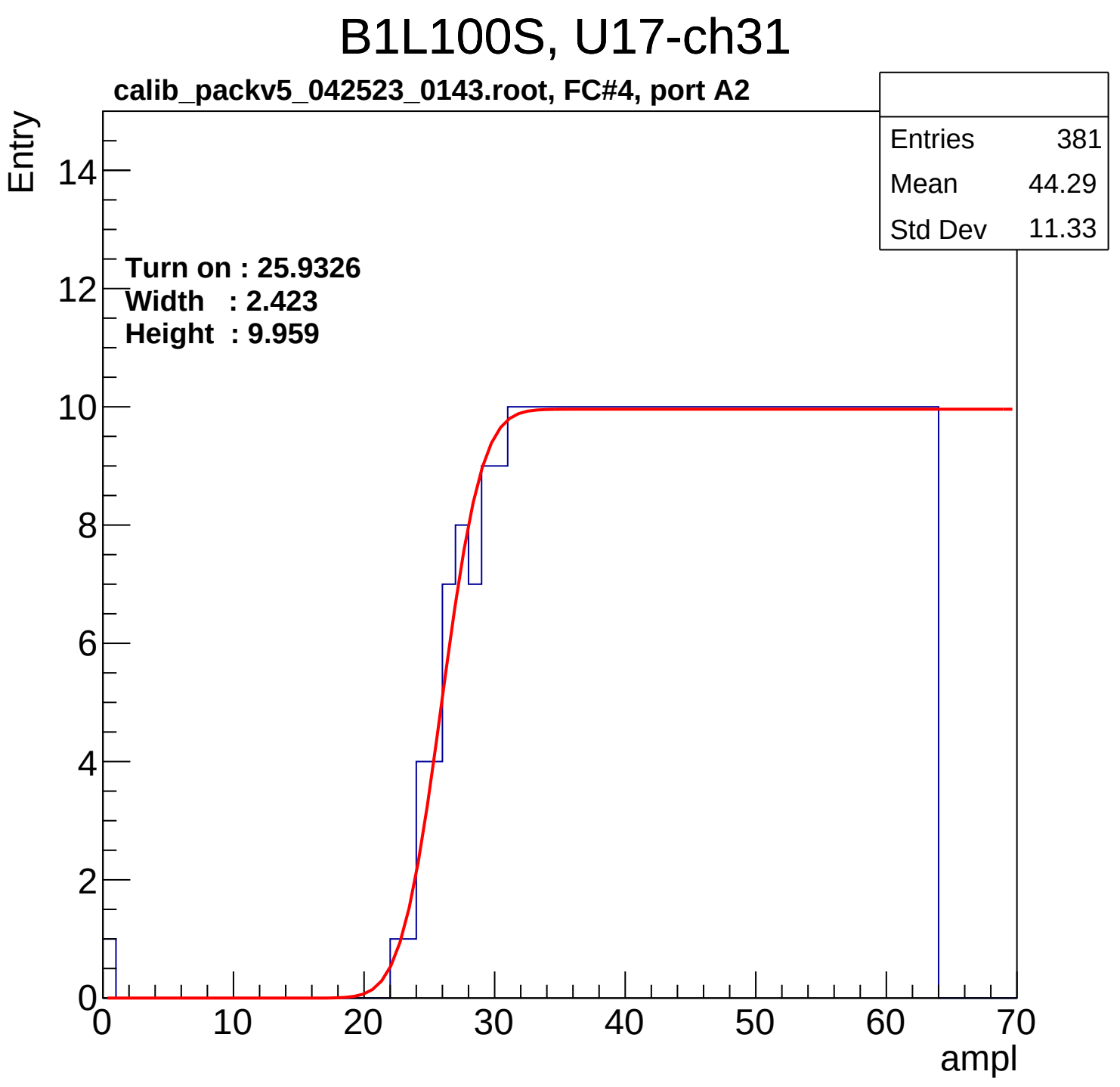
B1L100S, U17-ch31
calib_packv5_042523_0143.root, FC#4, port A2
Entries 381
Mean 44.29
Std Dev 11.33
Turn on : 25.9326
Width : 2.423
Height : 9.959
Entry
ampl
0
2
4
6
8
10
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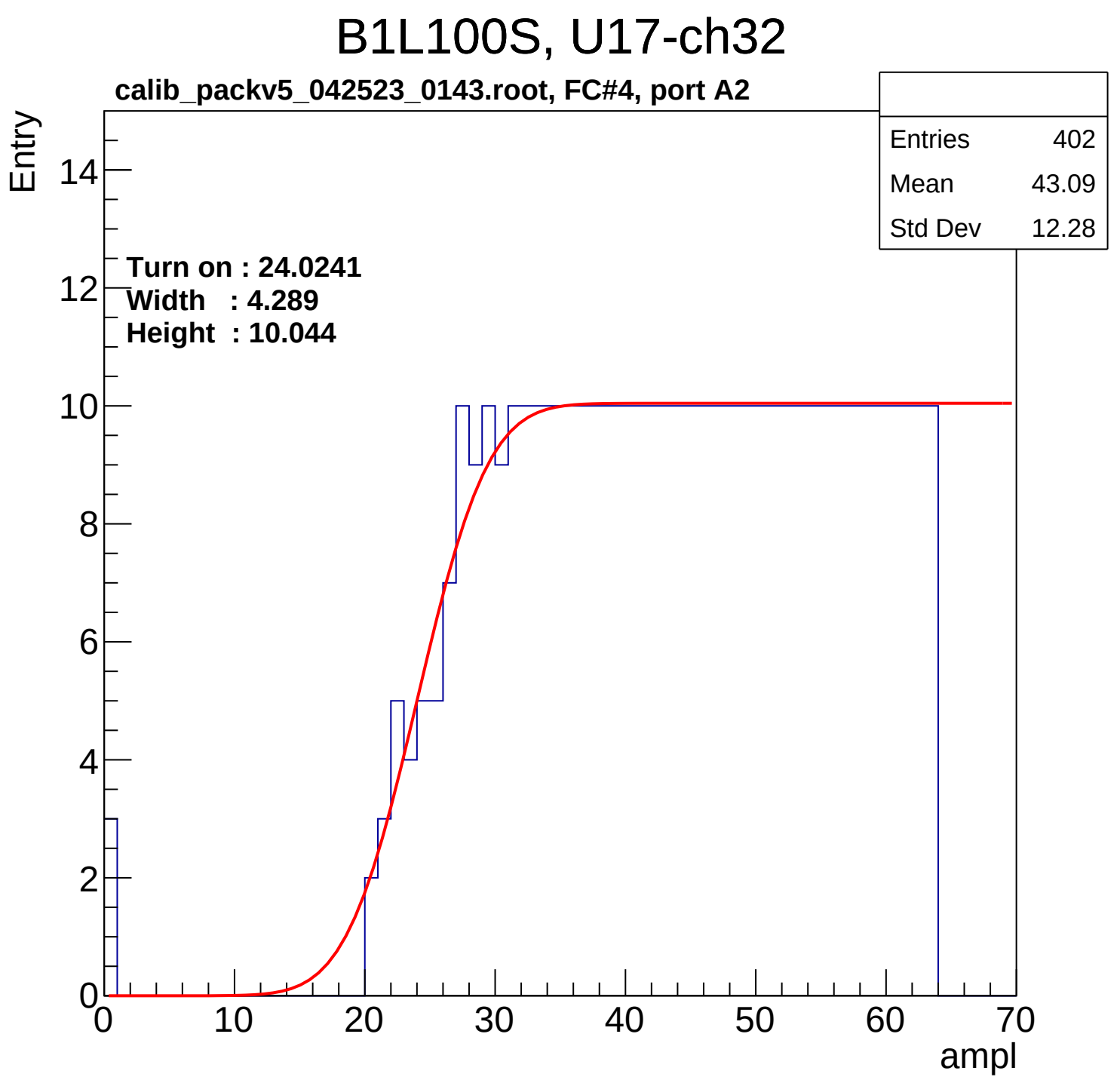
B1L100S, U17-ch32
calib_packv5_042523_0143.root, FC#4, port A2
Entries 402
Mean 43.09
Std Dev 12.28
Turn on : 24.0241
Width : 4.289
Height : 10.044
Entry
ampl
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2
4
6
8
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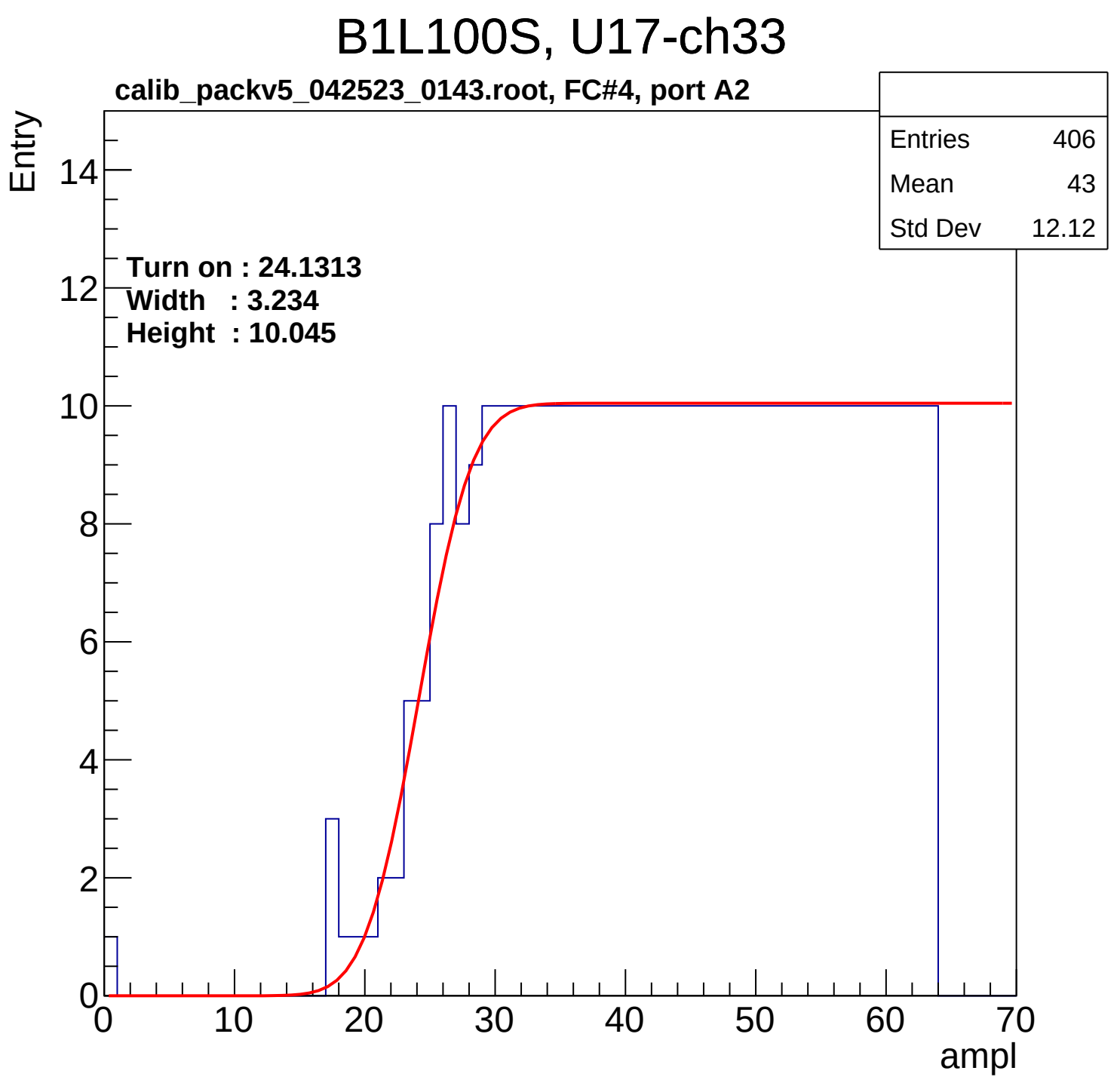
B1L100S, U17-ch33
calib_packv5_042523_0143.root, FC#4, port A2
Entries 406
Mean 43
Std Dev 12.12
Turn on : 24.1313
Width : 3.234
Height : 10.045
Entry
ampl
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2
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0
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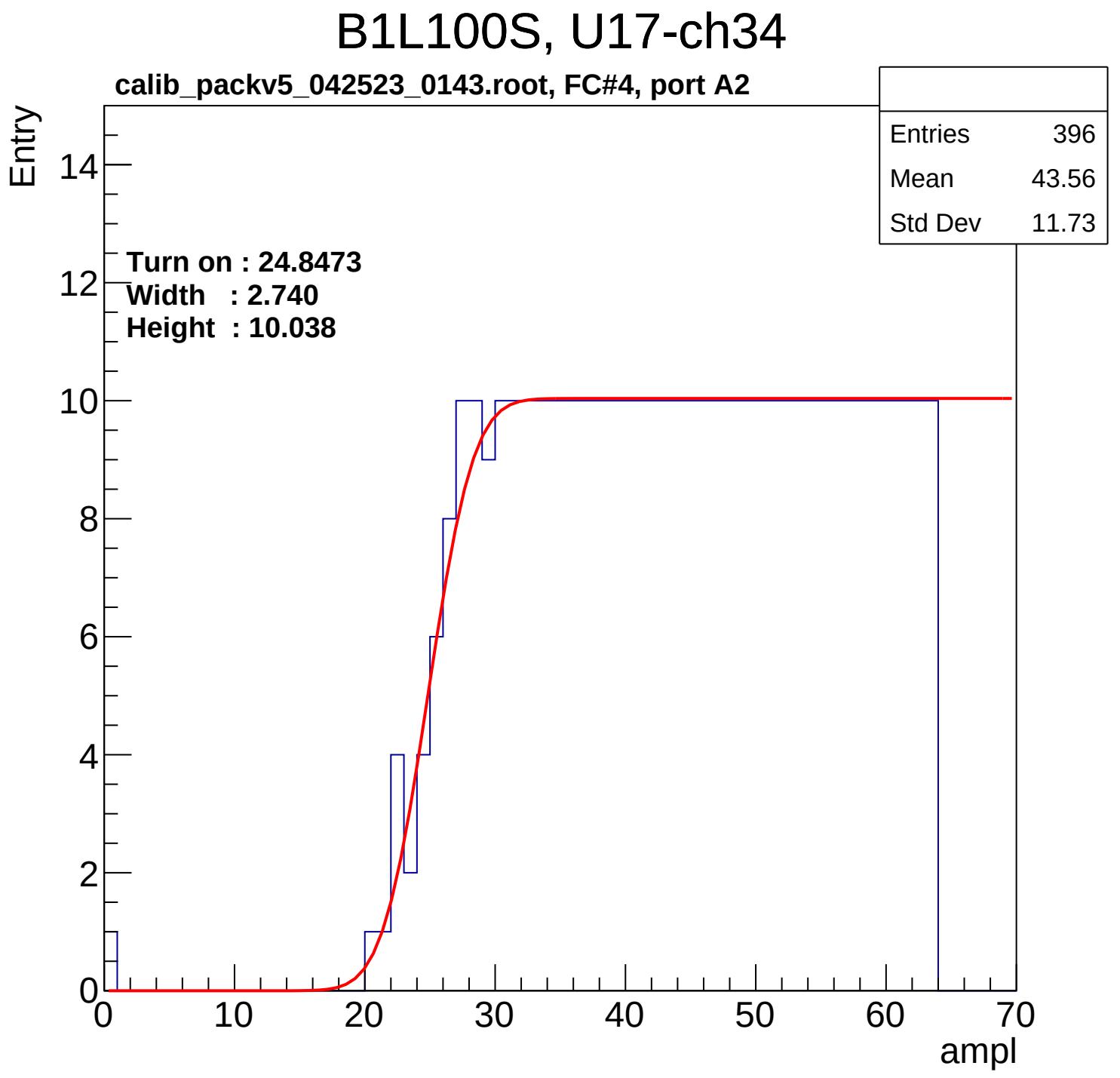
B1L100S, U17-ch34
calib_packv5_042523_0143.root, FC#4, port A2
Entries 396
Mean 43.56
Std Dev 11.73
Turn on : 24.8473
Width : 2.740
Height : 10.038
Entry
ampl
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2
4
6
8
10
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0
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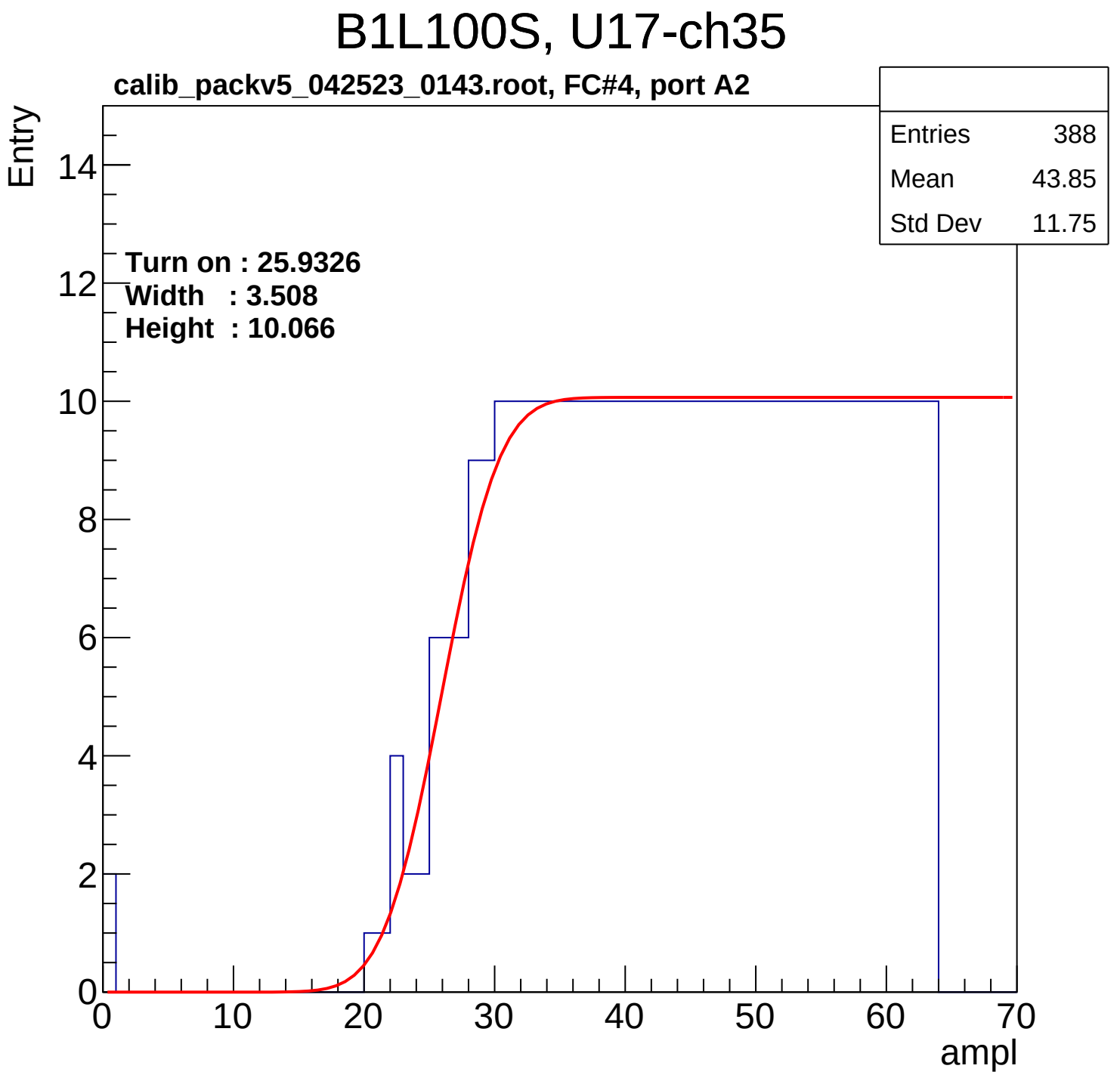
B1L100S, U17-ch35
calib_packv5_042523_0143.root, FC#4, port A2
Entries 388
Mean 43.85
Std Dev 11.75
Turn on : 25.9326
Width : 3.508
Height : 10.066
Entry
ampl
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2
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6
8
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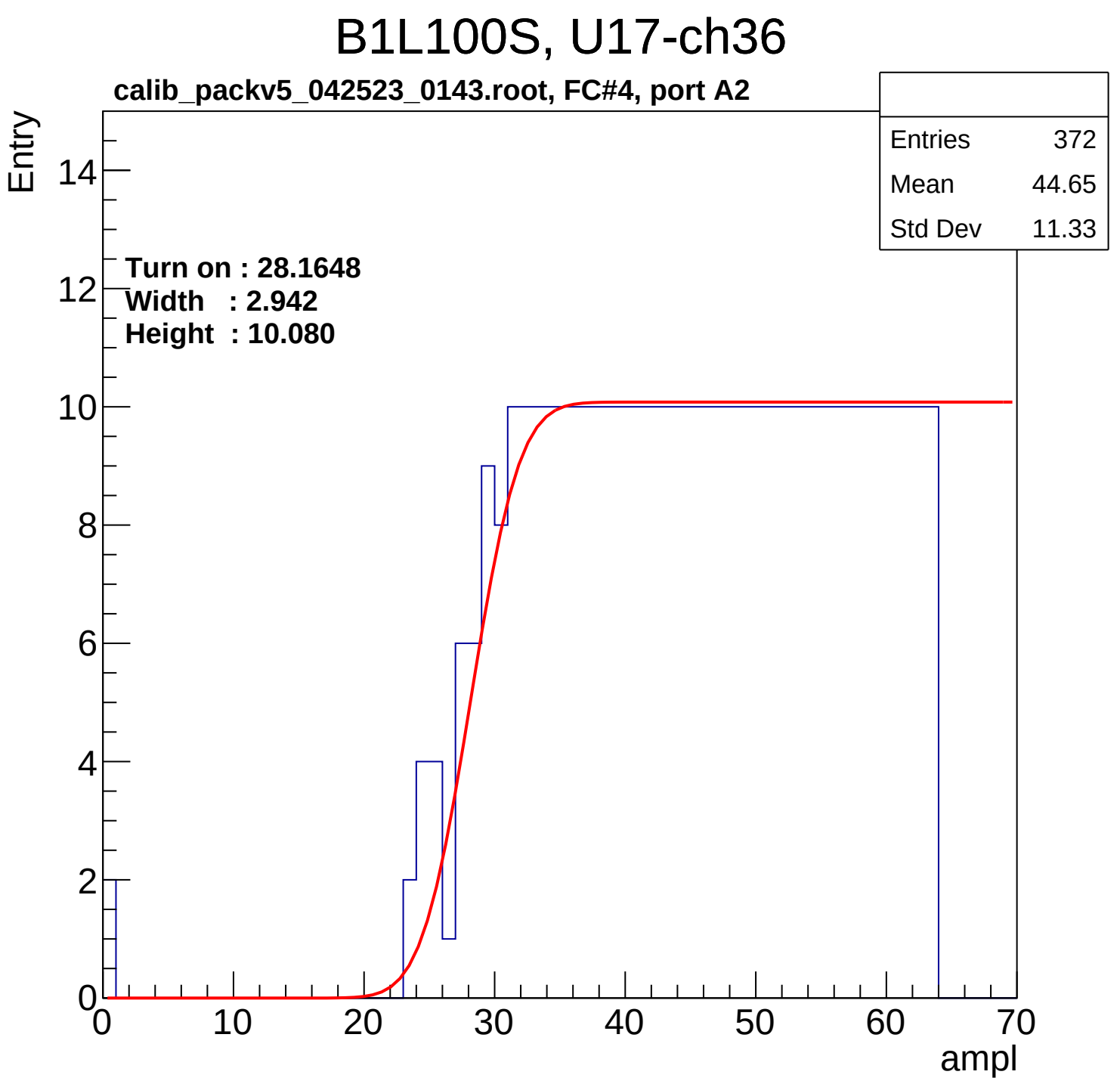
B1L100S, U17-ch36
calib_packv5_042523_0143.root, FC#4, port A2
Entries 372
Mean 44.65
Std Dev 11.33
Turn on : 28.1648
Width : 2.942
Height : 10.080
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
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60
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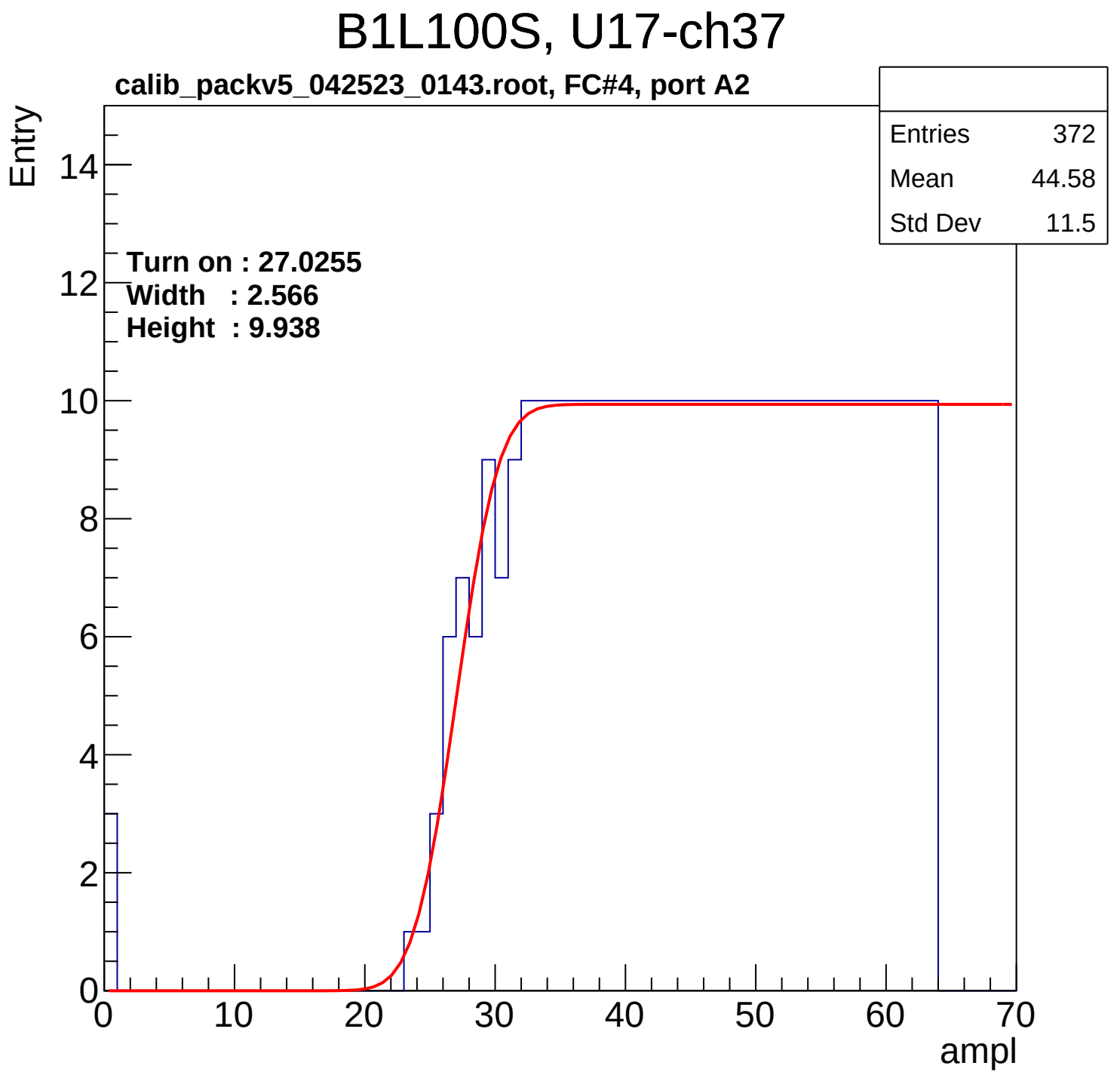
B1L100S, U17-ch37
calib_packv5_042523_0143.root, FC#4, port A2
Entries 372
Mean 44.58
Std Dev 11.5
Turn on : 27.0255
Width : 2.566
Height : 9.938
Entry
ampl
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2
4
6
8
10
12
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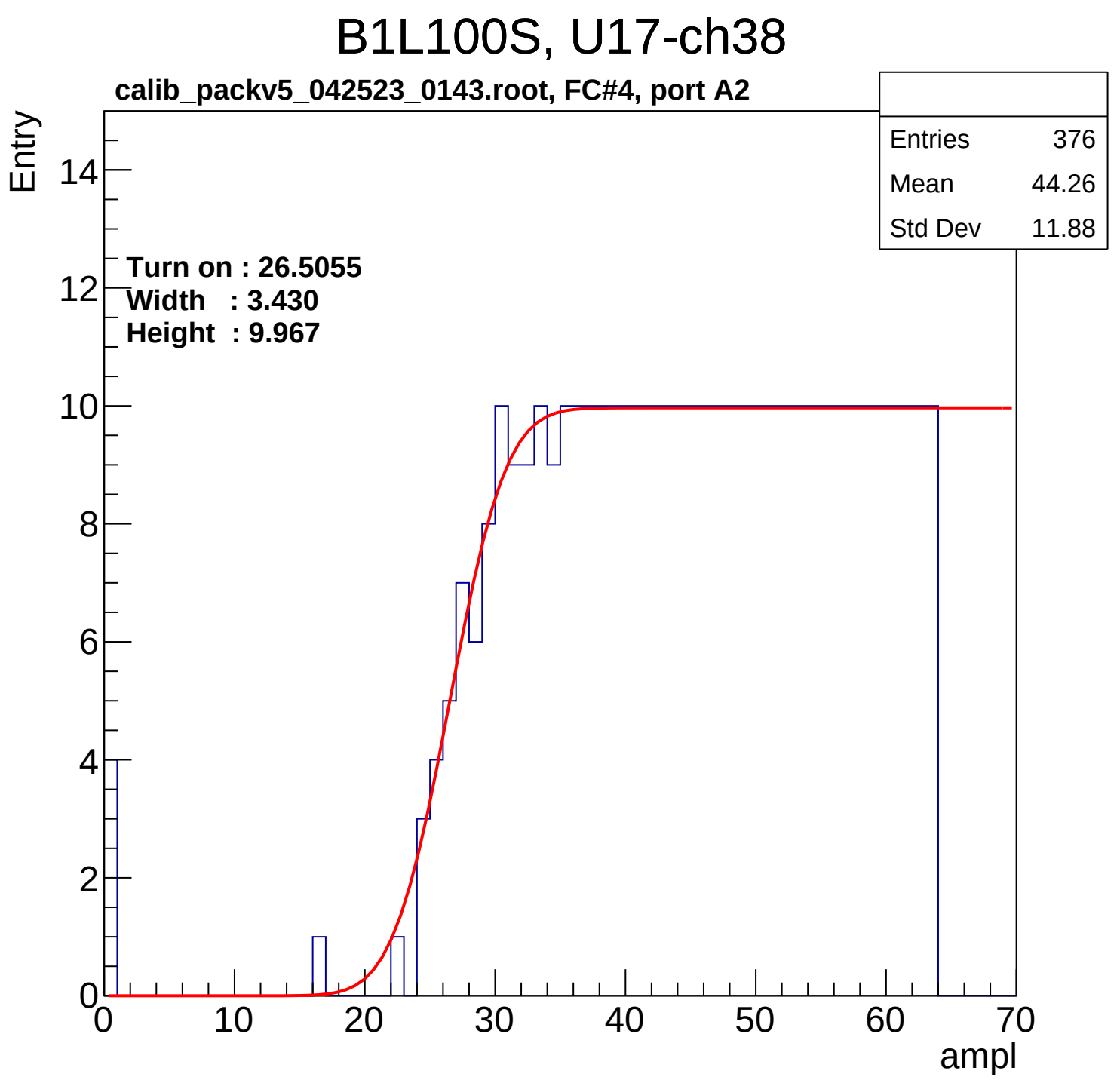
B1L100S, U17-ch38
calib_packv5_042523_0143.root, FC#4, port A2
Entries 376
Mean 44.26
Std Dev 11.88
Turn on : 26.5055
Width : 3.430
Height : 9.967
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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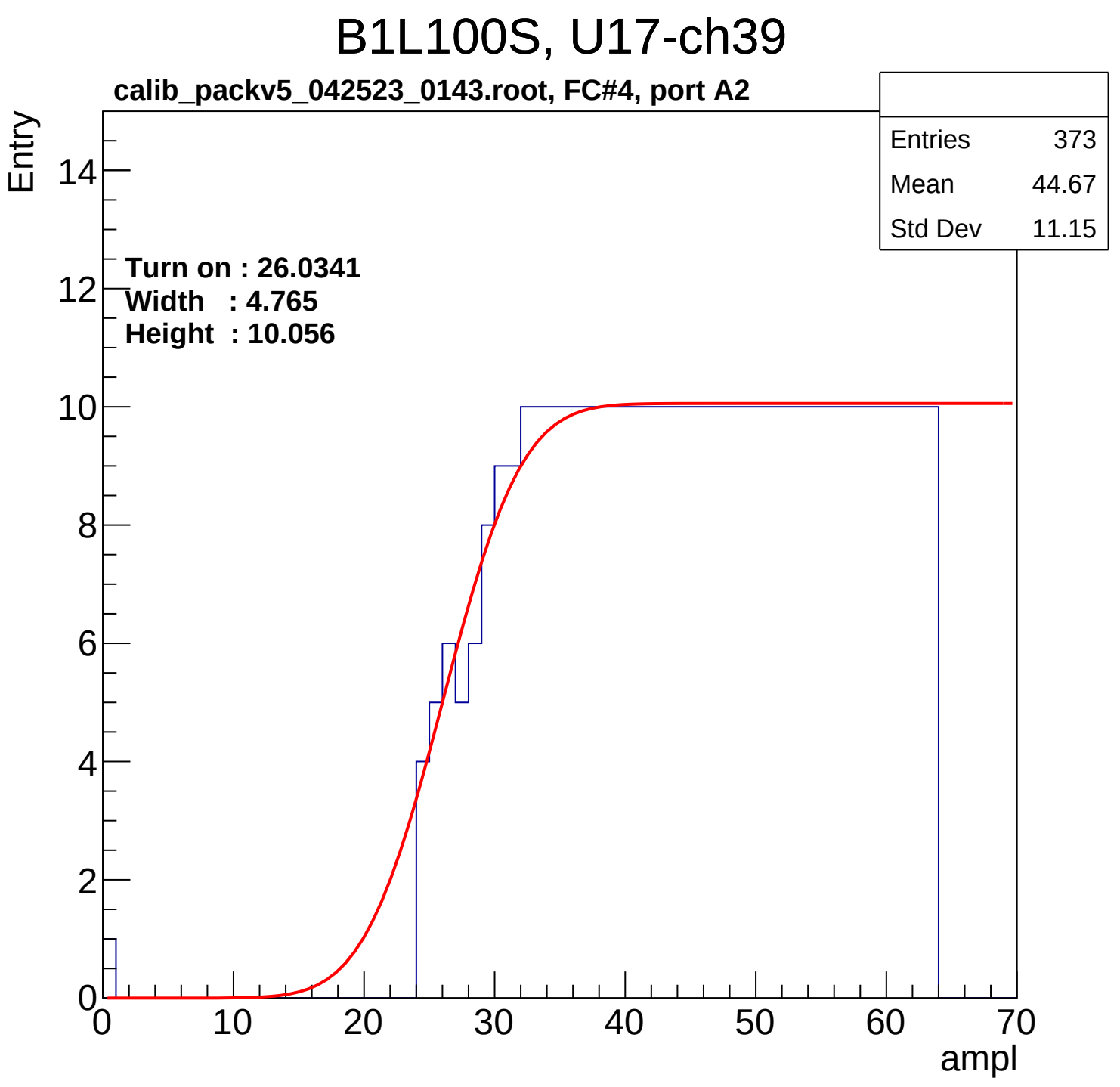
B1L100S, U17-ch39
calib_packv5_042523_0143.root, FC#4, port A2
Entries 373
Mean 44.67
Std Dev 11.15
Turn on : 26.0341
Width : 4.765
Height : 10.056
Entry
ampl
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6
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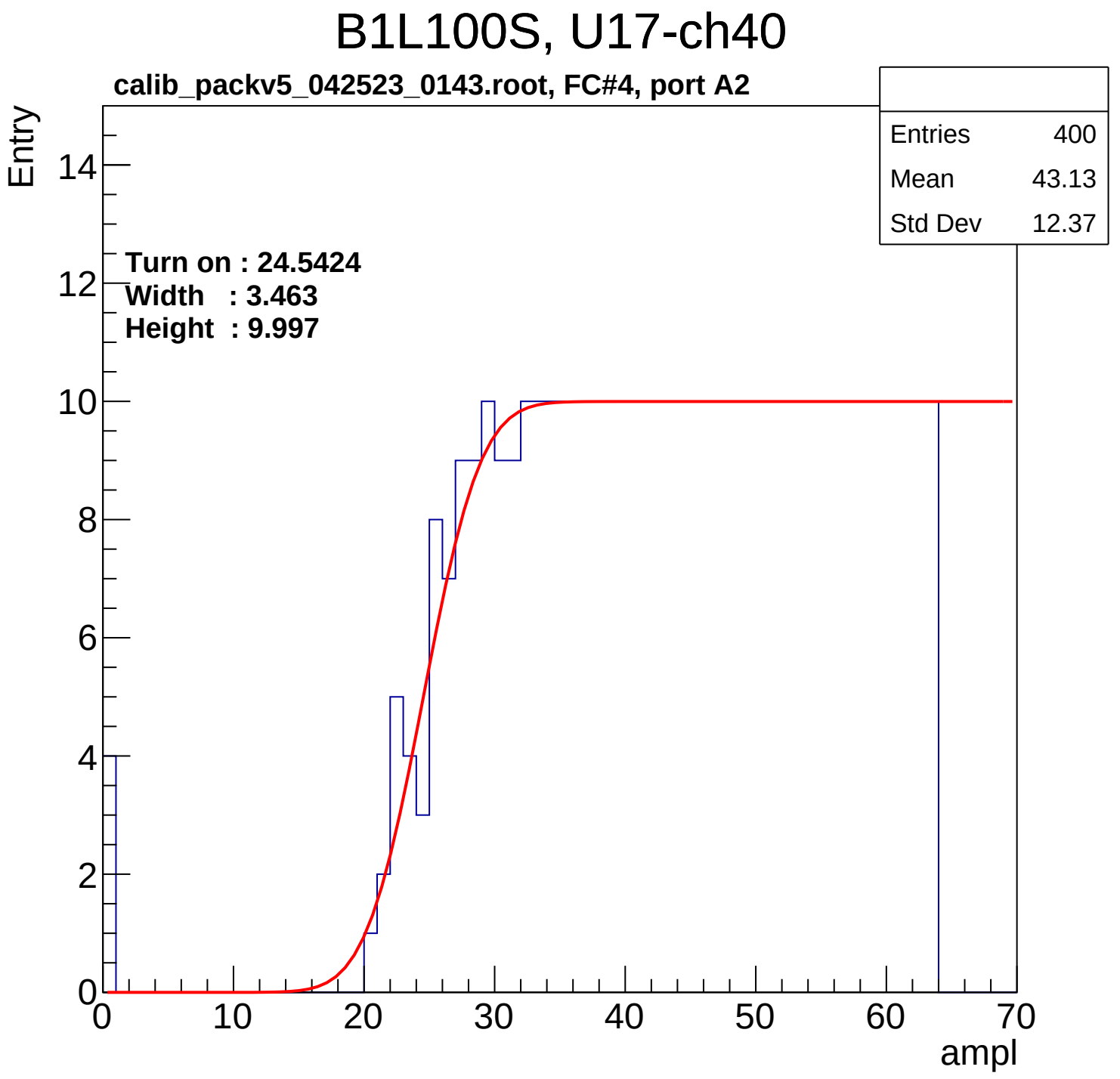
B1L100S, U17-ch40
calib_packv5_042523_0143.root, FC#4, port A2
Entries 400
Mean 43.13
Std Dev 12.37
Turn on : 24.5424
Width : 3.463
Height : 9.997
Entry
ampl
0
2
4
6
8
10
12
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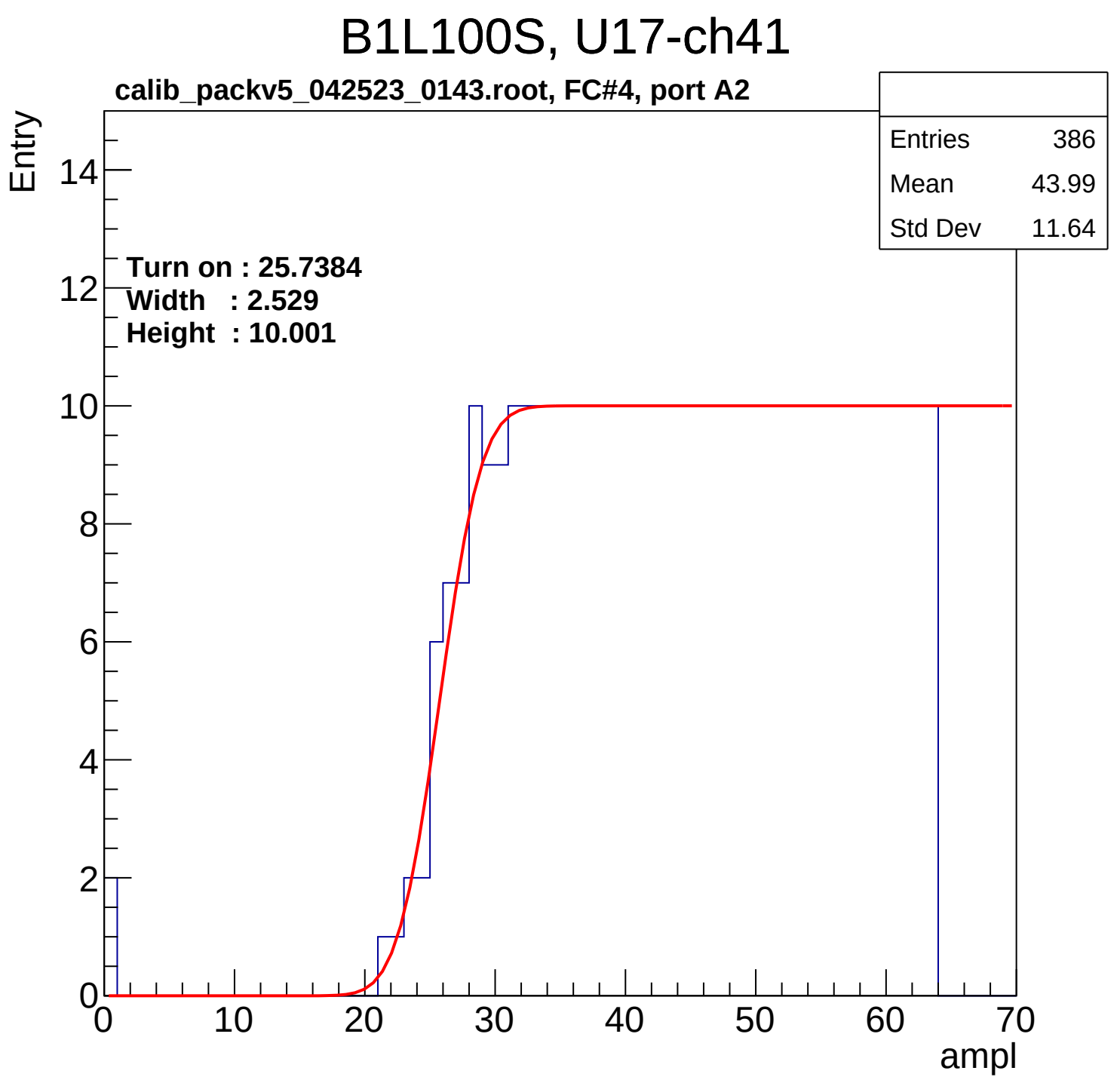
B1L100S, U17-ch41
calib_packv5_042523_0143.root, FC#4, port A2
Entries 386
Mean 43.99
Std Dev 11.64
Turn on : 25.7384
Width : 2.529
Height : 10.001
Entry
ampl
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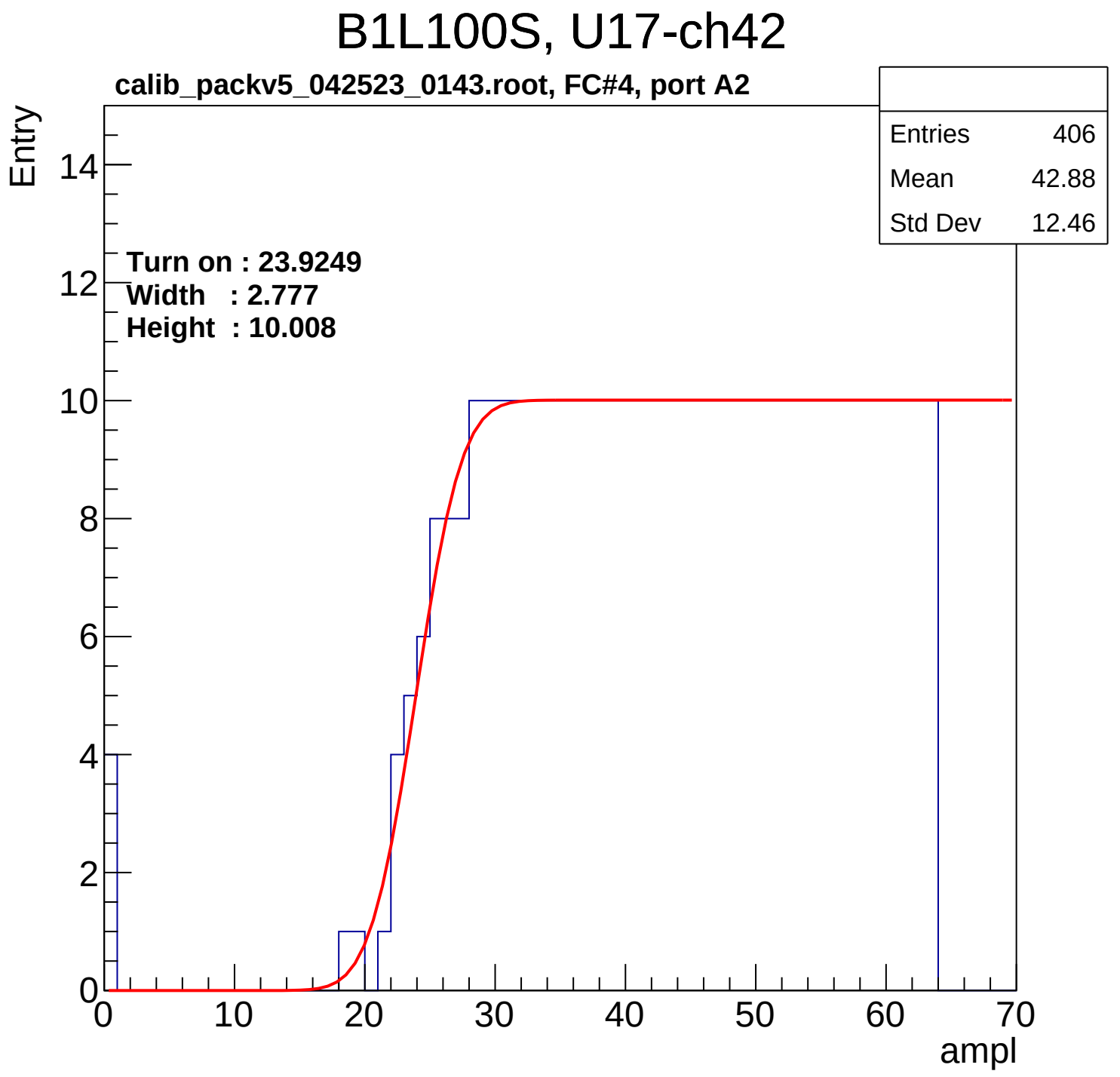
B1L100S, U17-ch42
calib_packv5_042523_0143.root, FC#4, port A2
Entries 406
Mean 42.88
Std Dev 12.46
Turn on : 23.9249
Width : 2.777
Height : 10.008
Entry
ampl
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4
6
8
10
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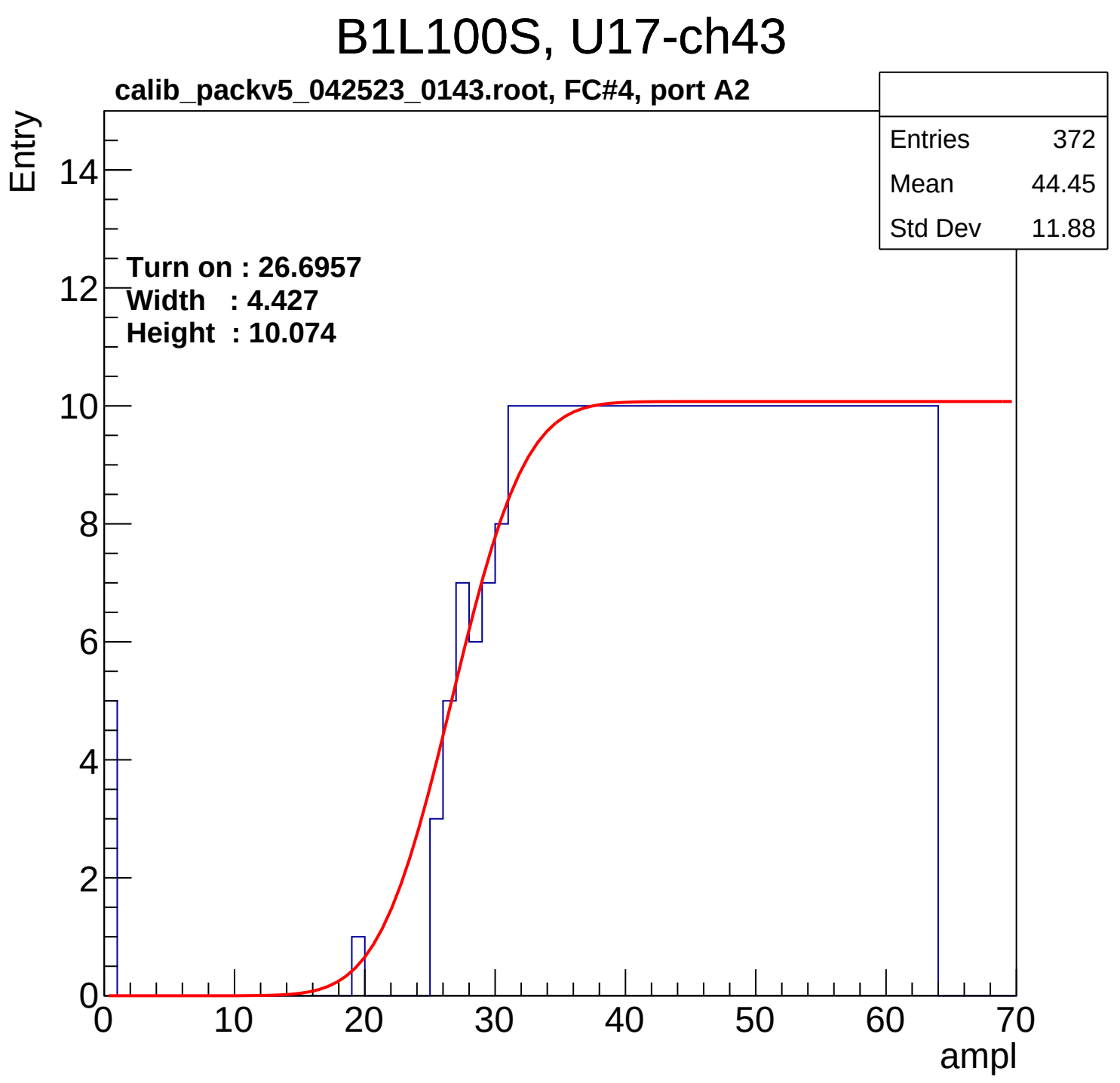
B1L100S, U17-ch43
calib_packv5_042523_0143.root, FC#4, port A2
Entries 372
Mean 44.45
Std Dev 11.88
Turn on : 26.6957
Width : 4.427
Height : 10.074
Entry
ampl
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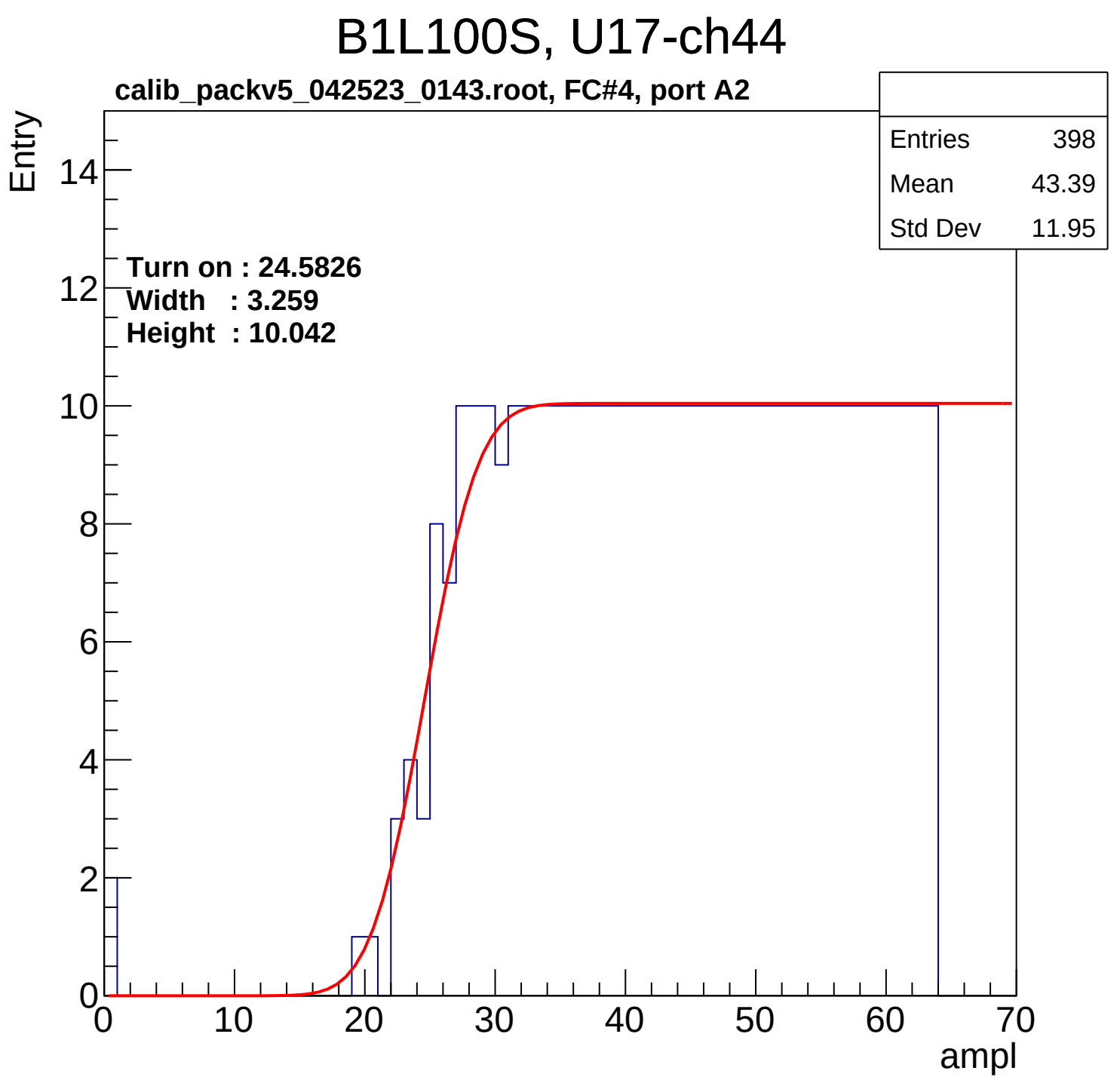
B1L100S, U17-ch44
calib_packv5_042523_0143.root, FC#4, port A2
Entries 398
Mean 43.39
Std Dev 11.95
Turn on : 24.5826
Width : 3.259
Height : 10.042
Entry
ampl
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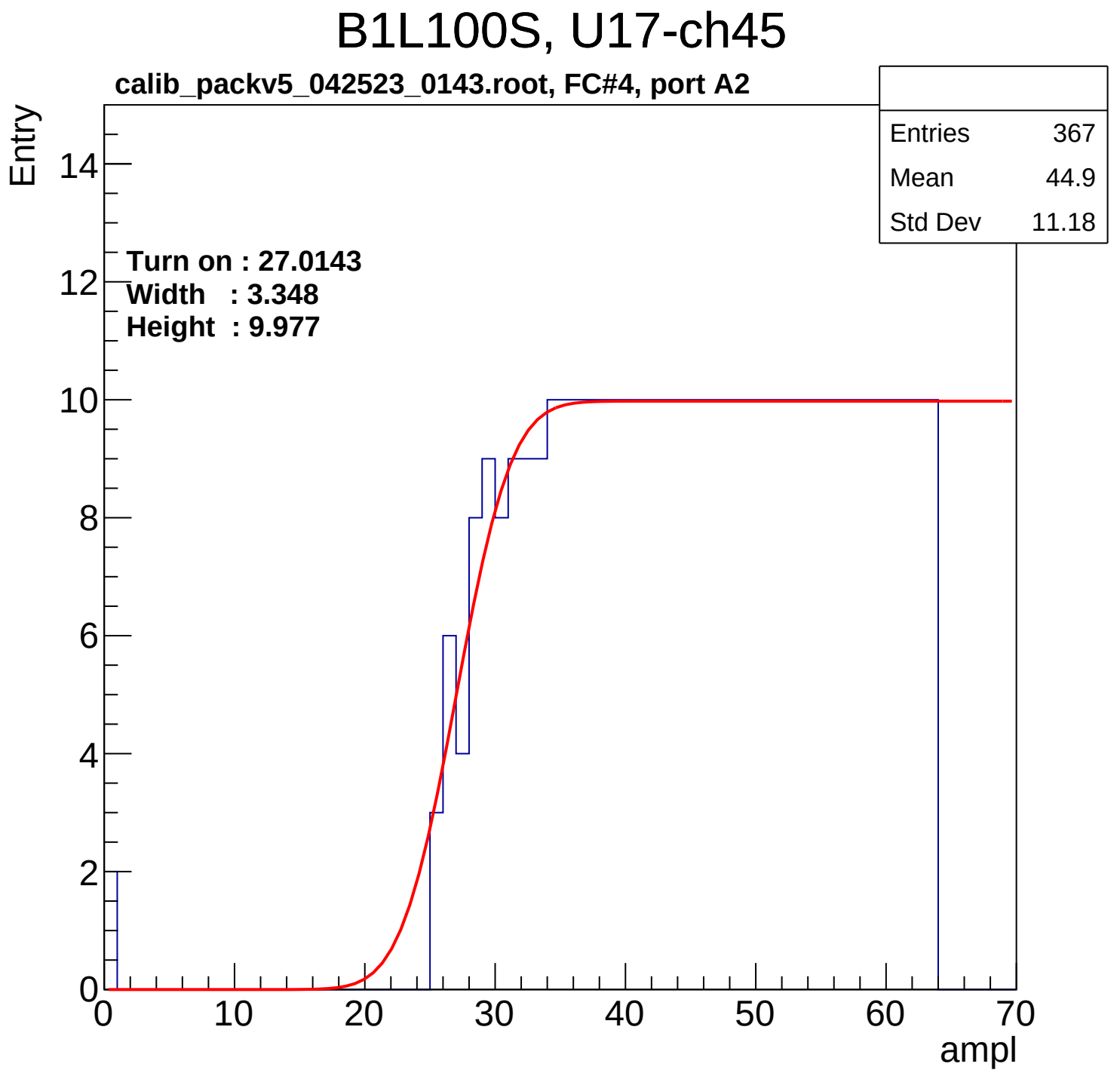
B1L100S, U17-ch45
calib_packv5_042523_0143.root, FC#4, port A2
Entries 367
Mean 44.9
Std Dev 11.18
Turn on : 27.0143
Width : 3.348
Height : 9.977
Entry
ampl
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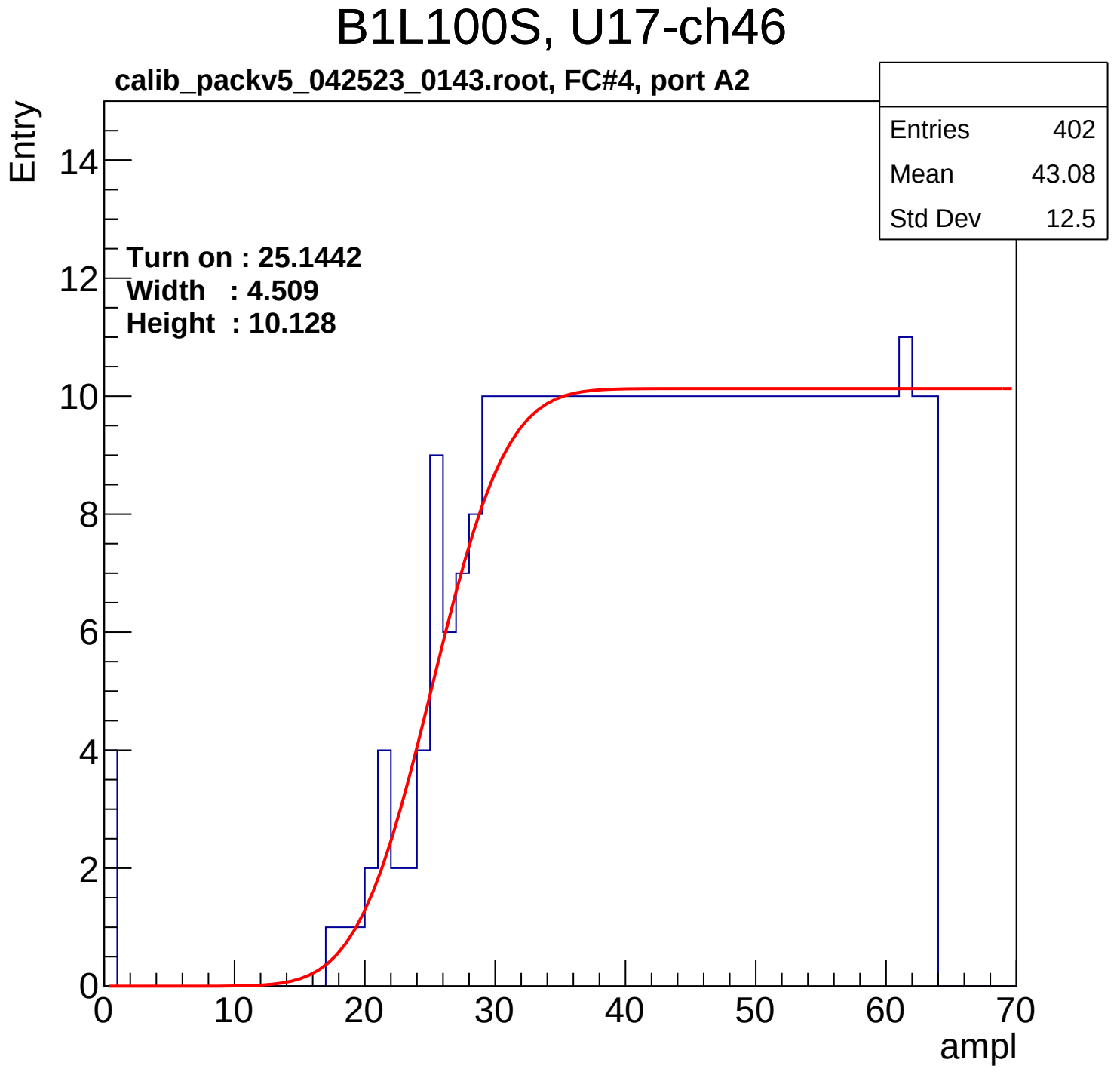
B1L100S, U17-ch46
calib_packv5_042523_0143.root, FC#4, port A2
Entries 402
Mean 43.08
Std Dev 12.5
Turn on : 25.1442
Width : 4.509
Height : 10.128
Entry
ampl
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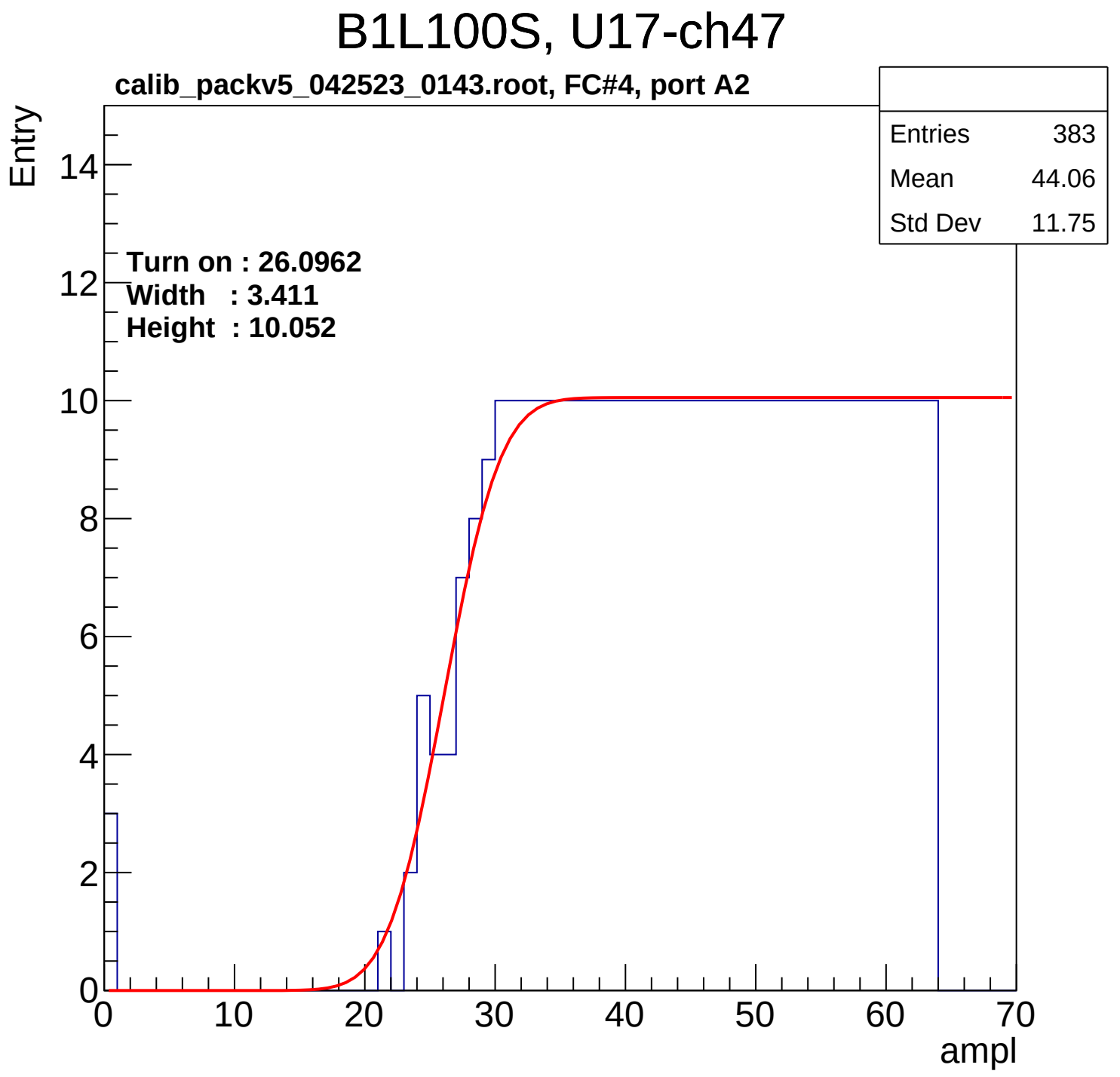
B1L100S, U17-ch47
calib_packv5_042523_0143.root, FC#4, port A2
Entries 383
Mean 44.06
Std Dev 11.75
Turn on : 26.0962
Width : 3.411
Height : 10.052
Entry
ampl
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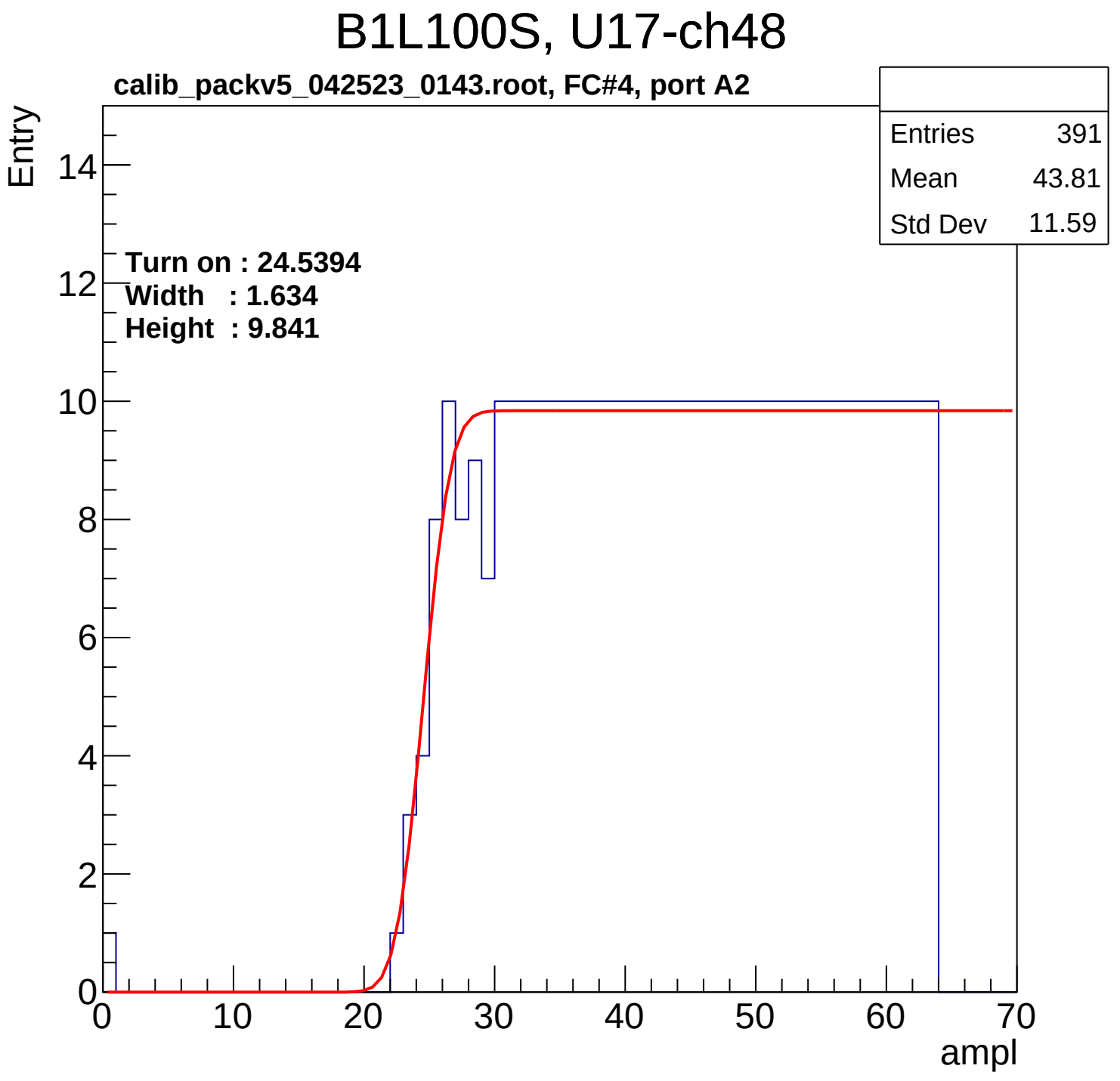
B1L100S, U17-ch48
calib_packv5_042523_0143.root, FC#4, port A2
Entries 391
Mean 43.81
Std Dev 11.59
Turn on : 24.5394
Width : 1.634
Height : 9.841
Entry
ampl
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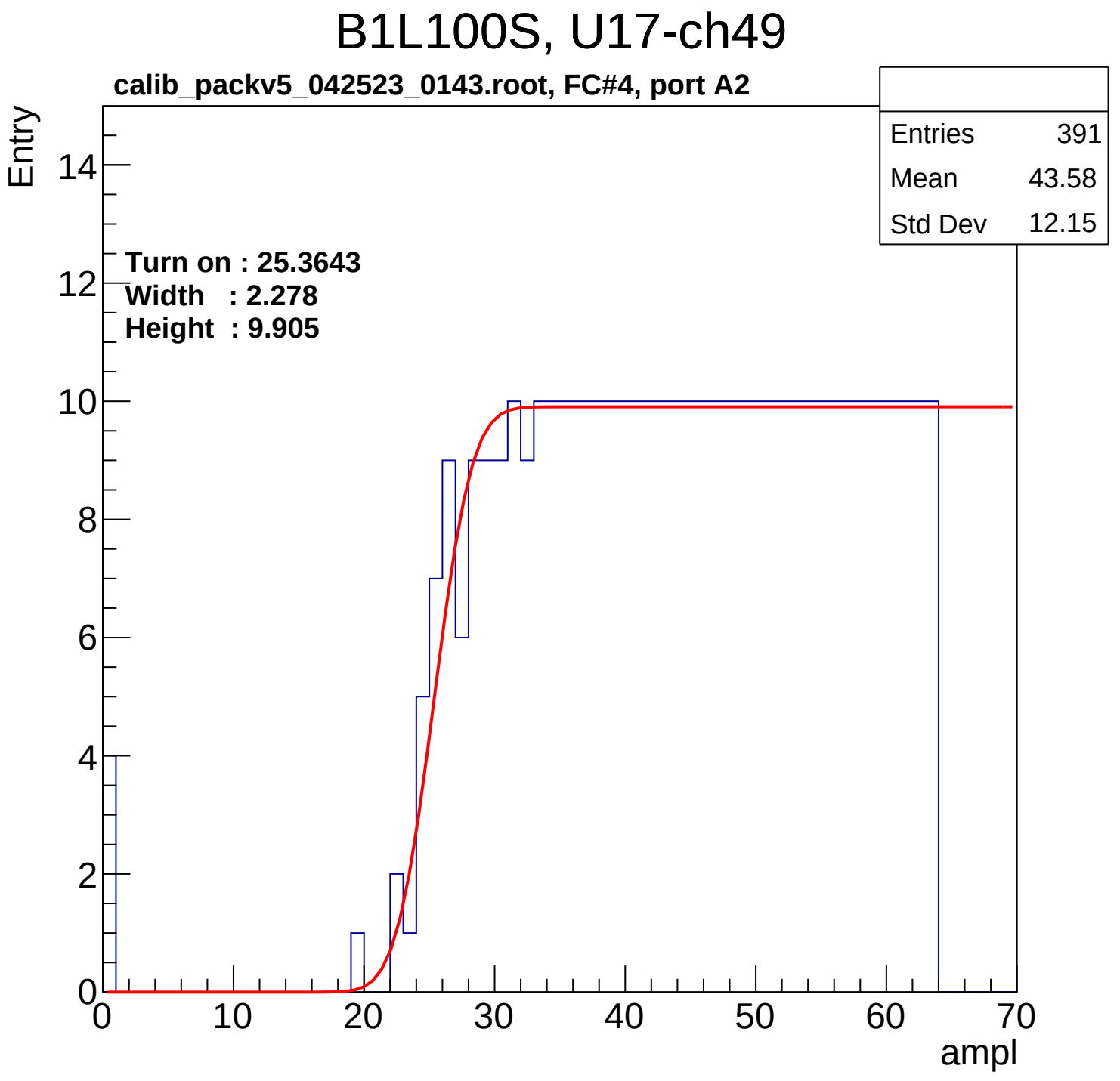
B1L100S, U17-ch49
calib_packv5_042523_0143.root, FC#4, port A2
Entries 391
Mean 43.58
Std Dev 12.15
Turn on : 25.3643
Width : 2.278
Height : 9.905
Entry
ampl
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8
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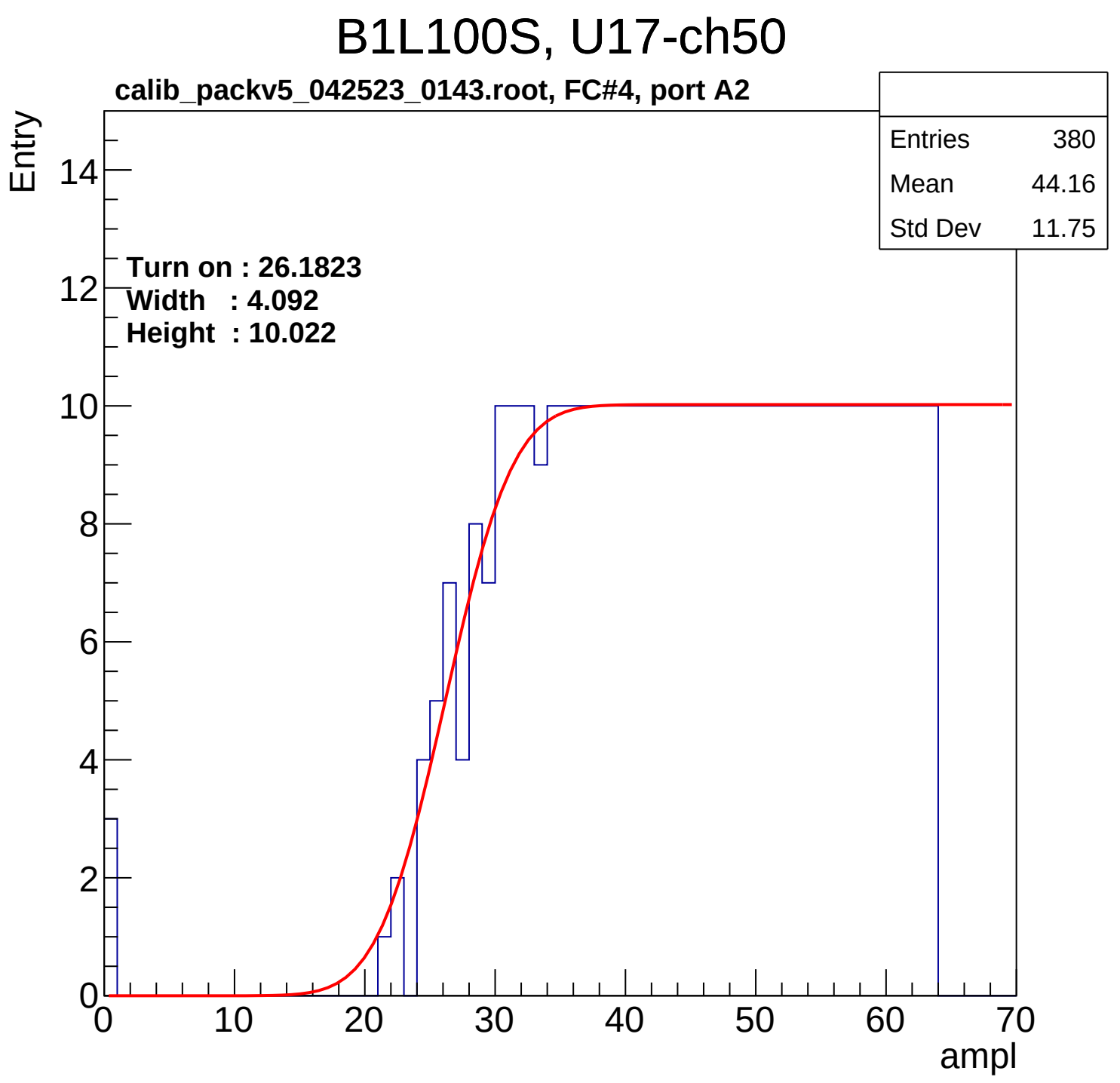
B1L100S, U17-ch50
calib_packv5_042523_0143.root, FC#4, port A2
Entries 380
Mean 44.16
Std Dev 11.75
Turn on : 26.1823
Width : 4.092
Height : 10.022
Entry
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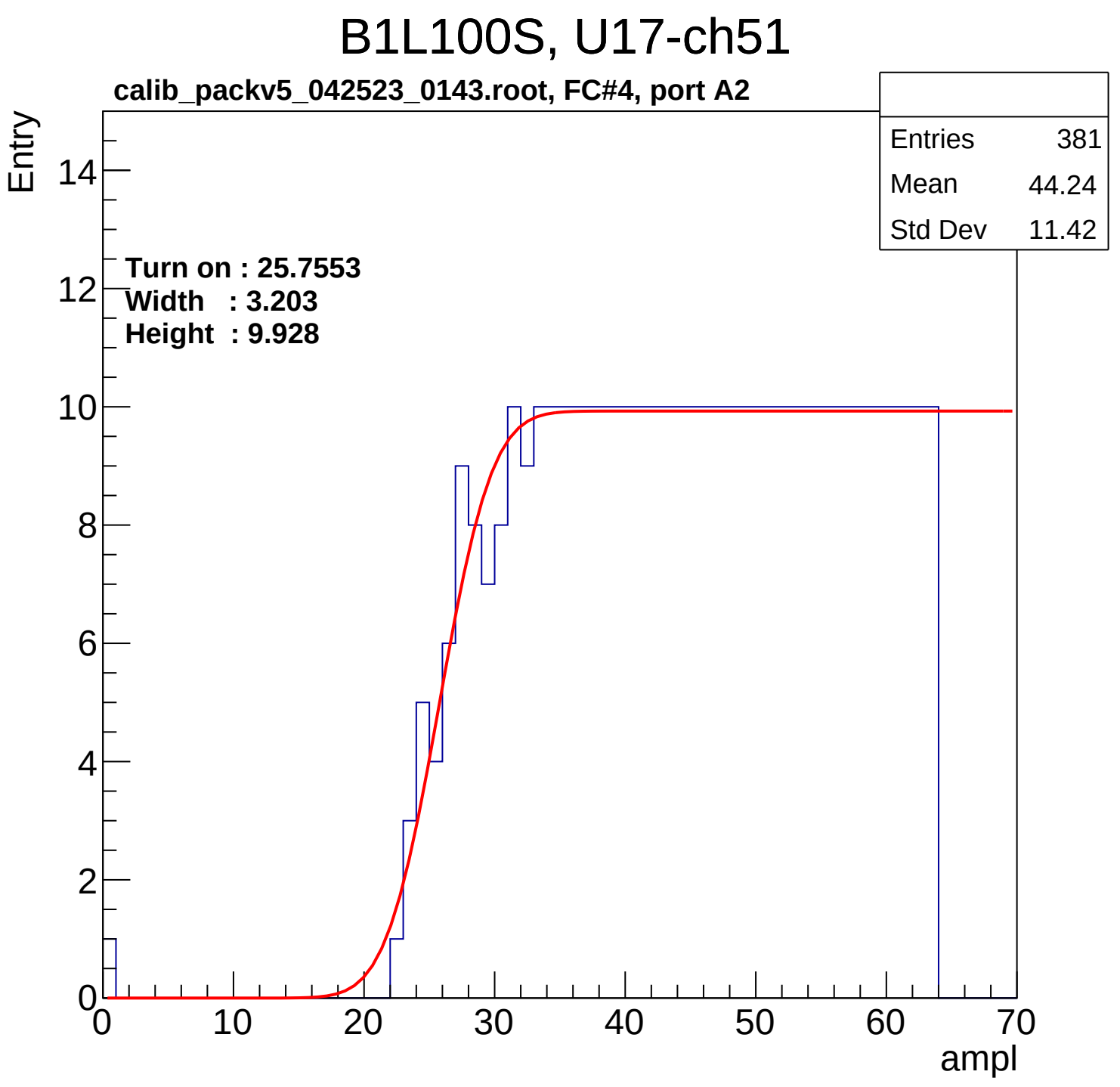
B1L100S, U17-ch51
calib_packv5_042523_0143.root, FC#4, port A2
Entries 381
Mean 44.24
Std Dev 11.42
Turn on : 25.7553
Width : 3.203
Height : 9.928
Entry
ampl
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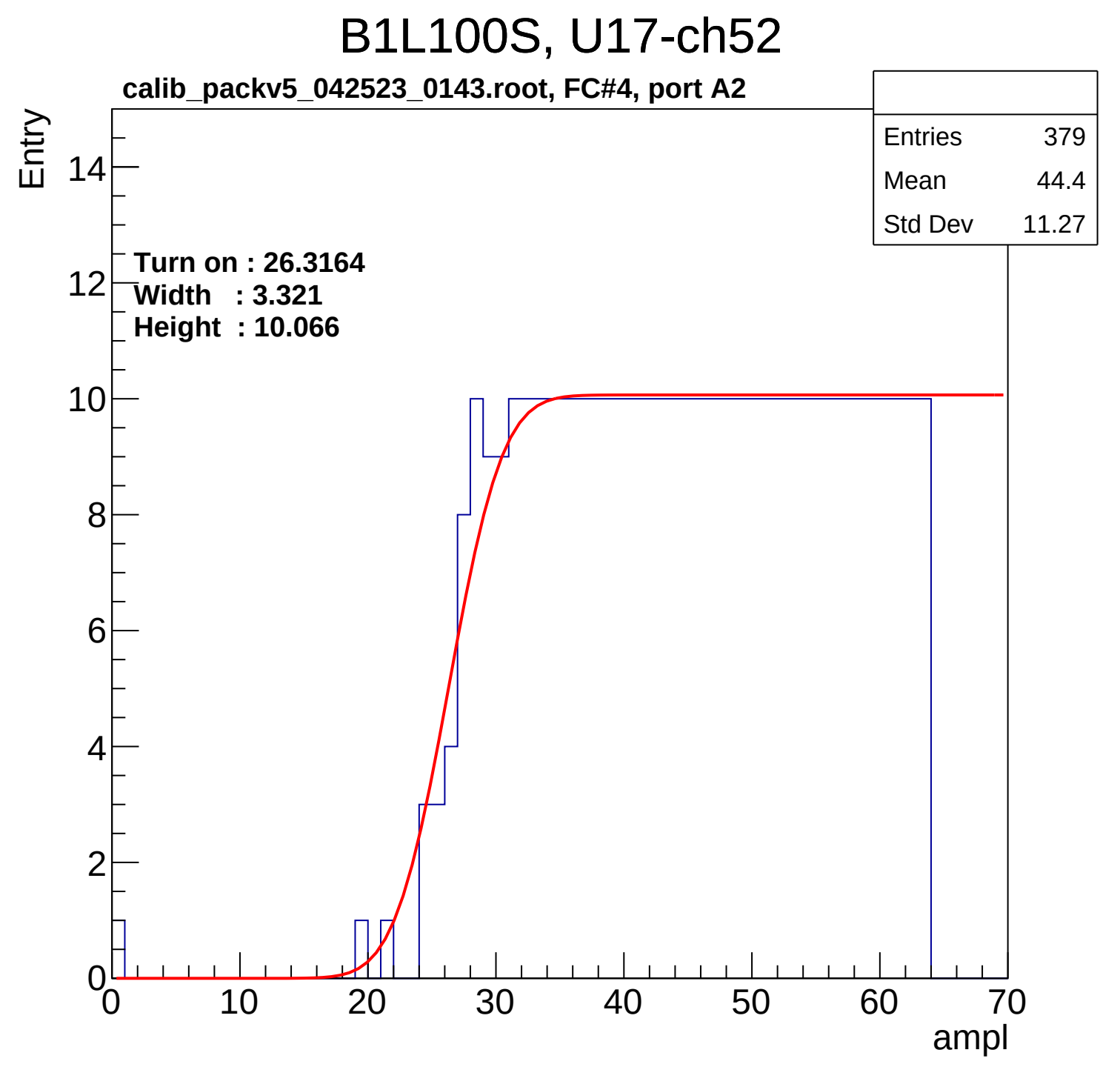
B1L100S, U17-ch52
calib_packv5_042523_0143.root, FC#4, port A2
Entries 379
Mean 44.4
Std Dev 11.27
Turn on : 26.3164
Width : 3.321
Height : 10.066
Entry
ampl
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6
8
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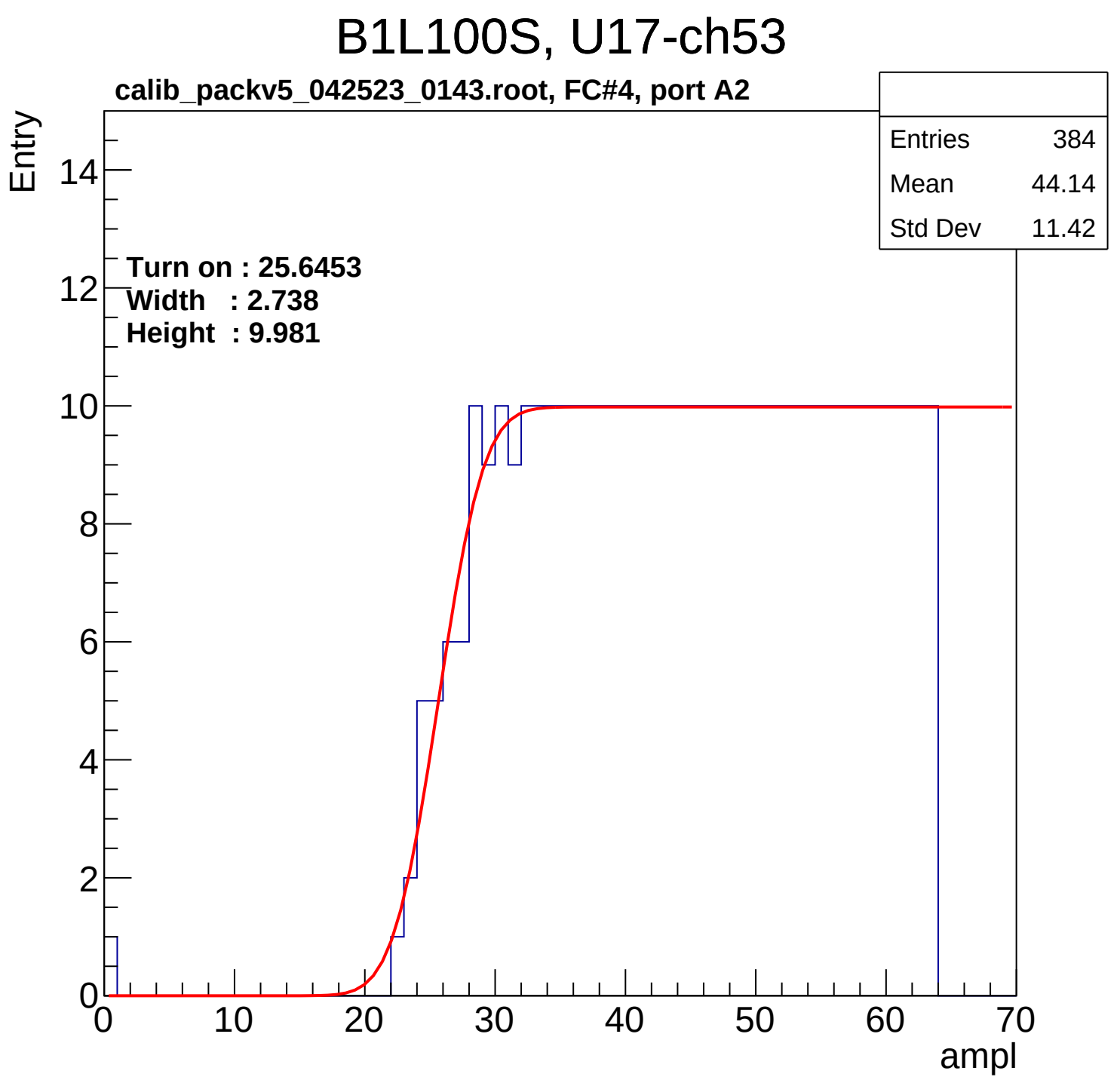
B1L100S, U17-ch53
calib_packv5_042523_0143.root, FC#4, port A2
Entries 384
Mean 44.14
Std Dev 11.42
Turn on : 25.6453
Width : 2.738
Height : 9.981
Entry
ampl
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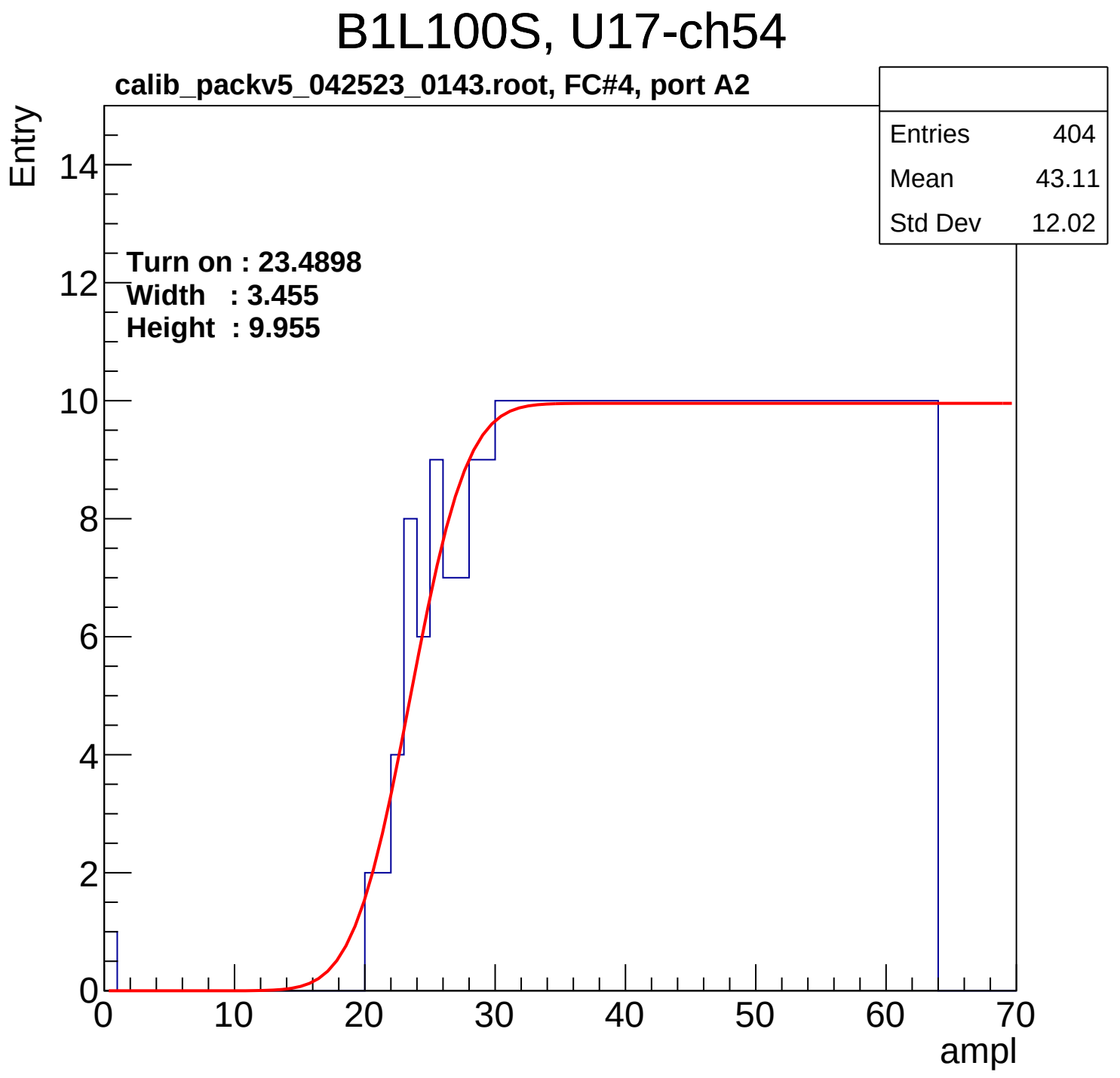
B1L100S, U17-ch54
calib_packv5_042523_0143.root, FC#4, port A2
Entries 404
Mean 43.11
Std Dev 12.02
Turn on : 23.4898
Width : 3.455
Height : 9.955
Entry
ampl
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6
8
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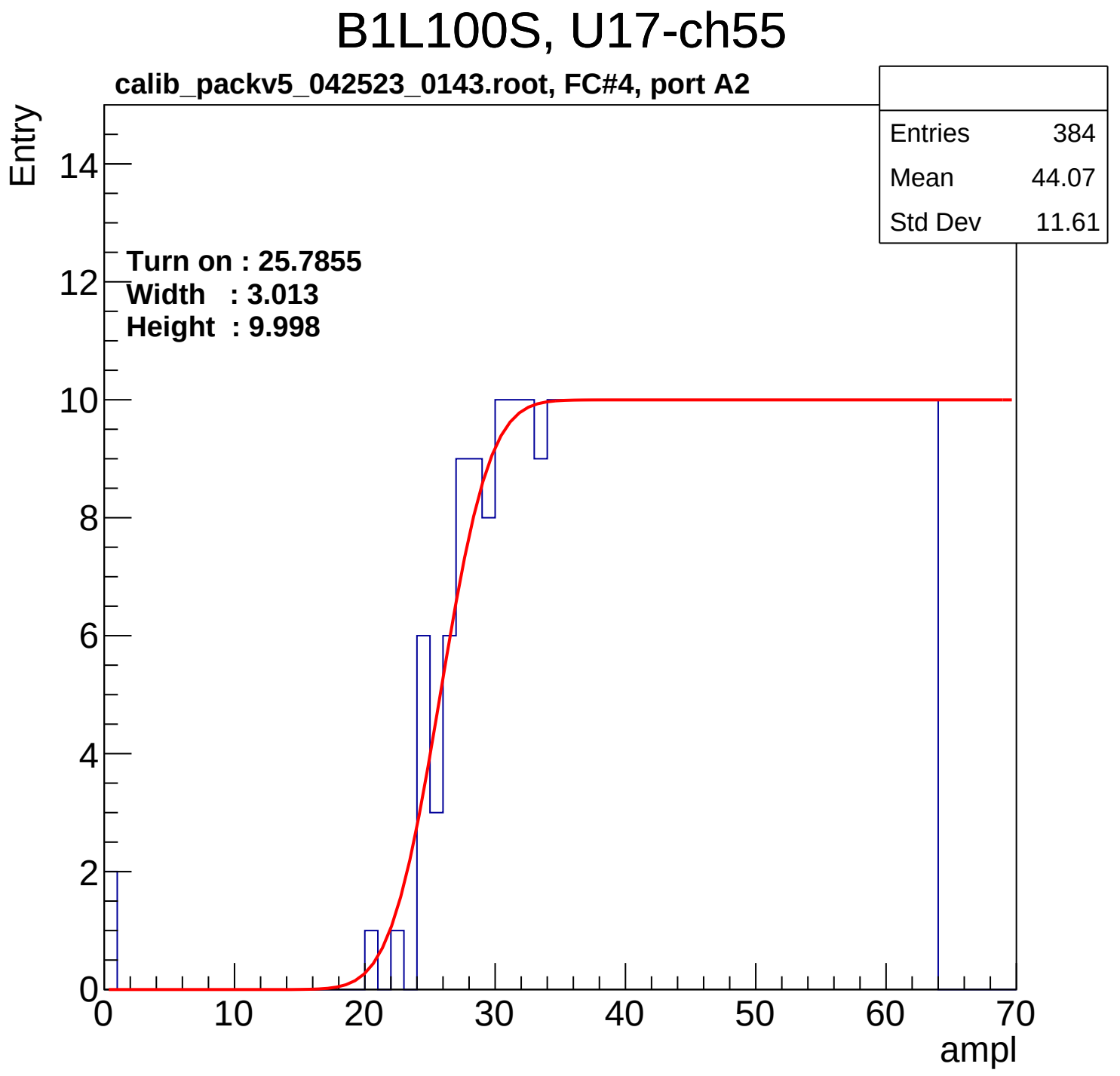
B1L100S, U17-ch55
calib_packv5_042523_0143.root, FC#4, port A2
Entries 384
Mean 44.07
Std Dev 11.61
Turn on : 25.7855
Width : 3.013
Height : 9.998
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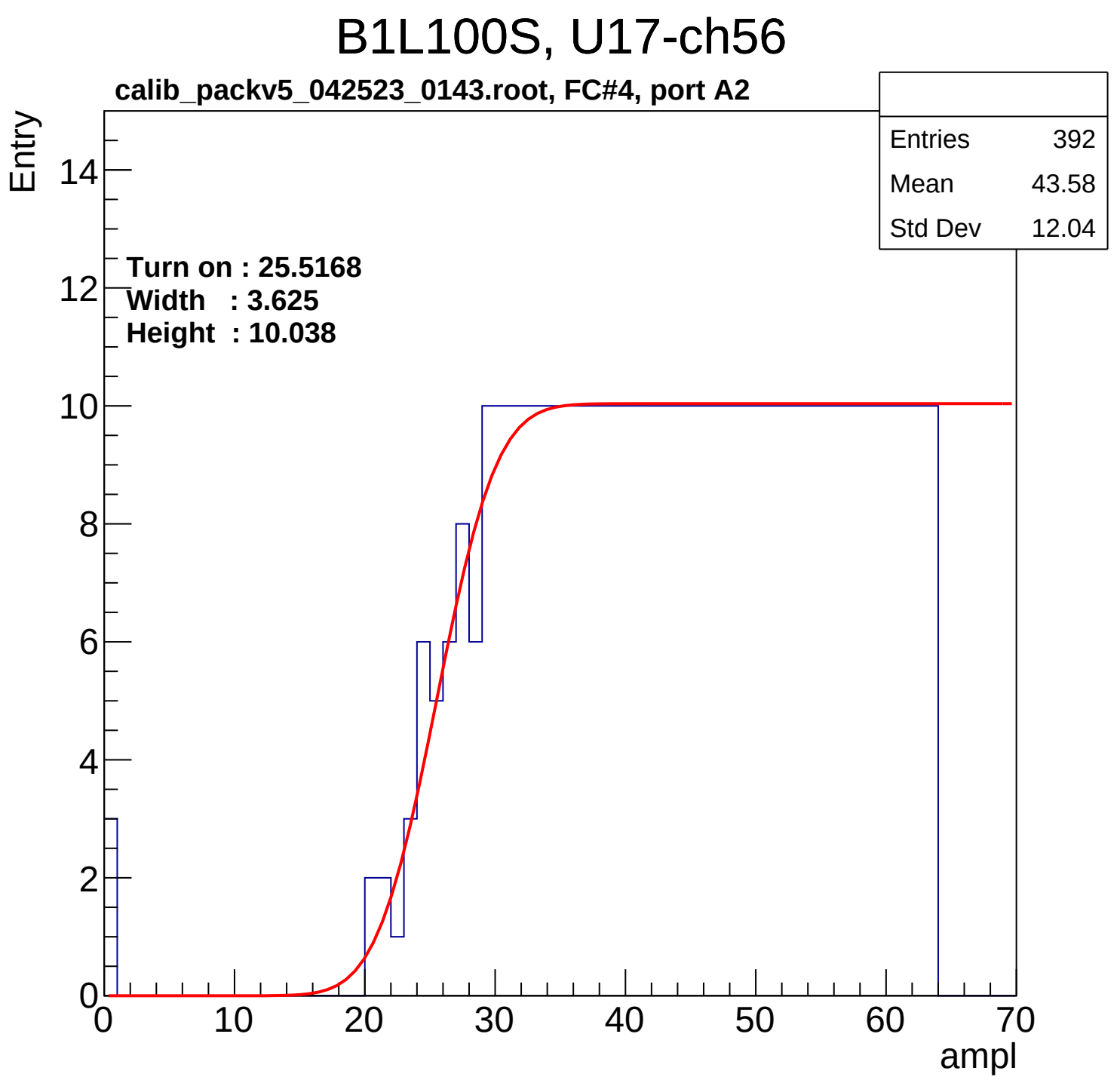
B1L100S, U17-ch56
calib_packv5_042523_0143.root, FC#4, port A2
Entries 392
Mean 43.58
Std Dev 12.04
Turn on : 25.5168
Width : 3.625
Height : 10.038
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ampl
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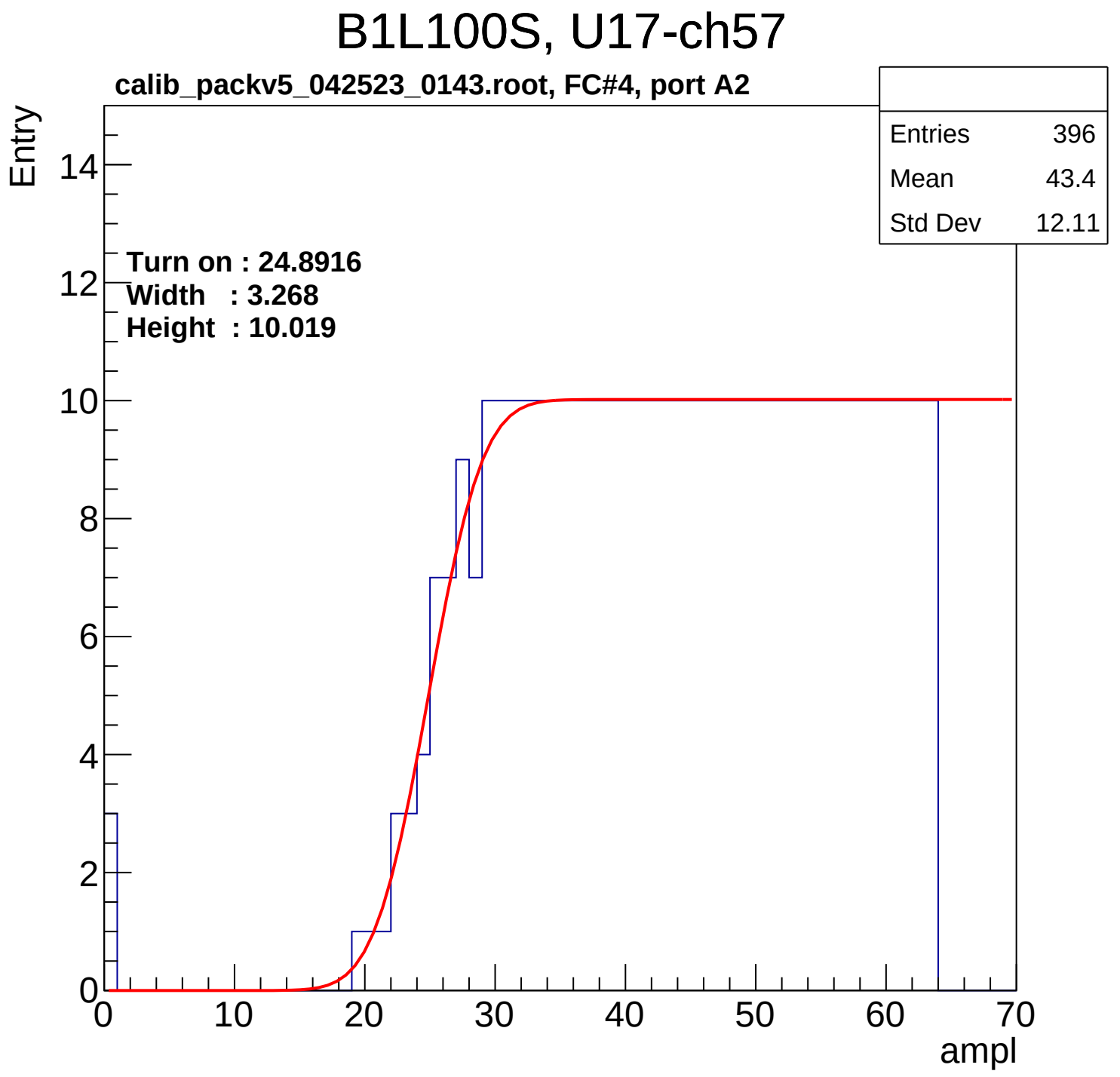
B1L100S, U17-ch57
calib_packv5_042523_0143.root, FC#4, port A2
Entries 396
Mean 43.4
Std Dev 12.11
Turn on : 24.8916
Width : 3.268
Height : 10.019
Entry
ampl
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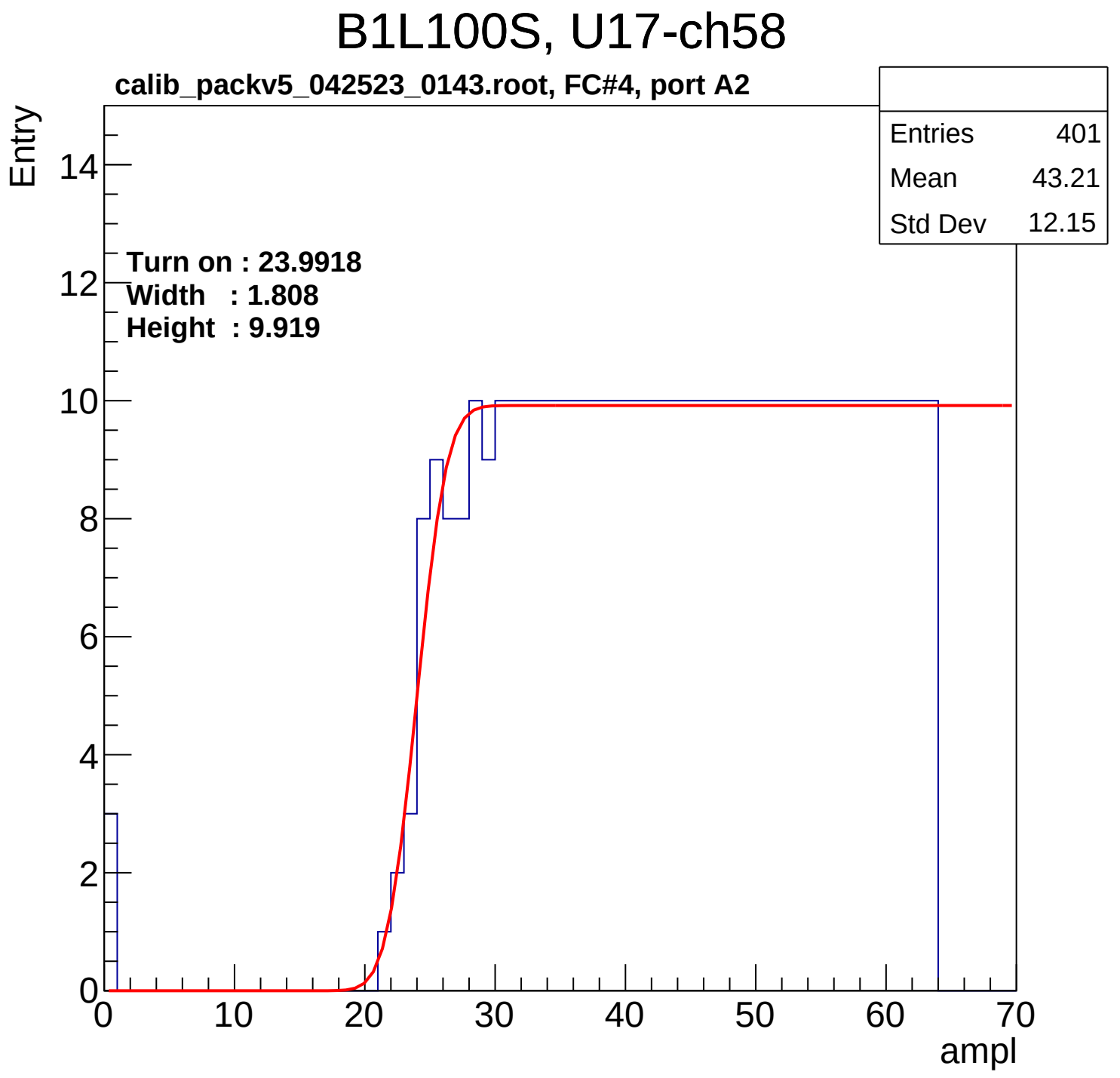
B1L100S, U17-ch58
calib_packv5_042523_0143.root, FC#4, port A2
Entries 401
Mean 43.21
Std Dev 12.15
Turn on : 23.9918
Width : 1.808
Height : 9.919
Entry
ampl
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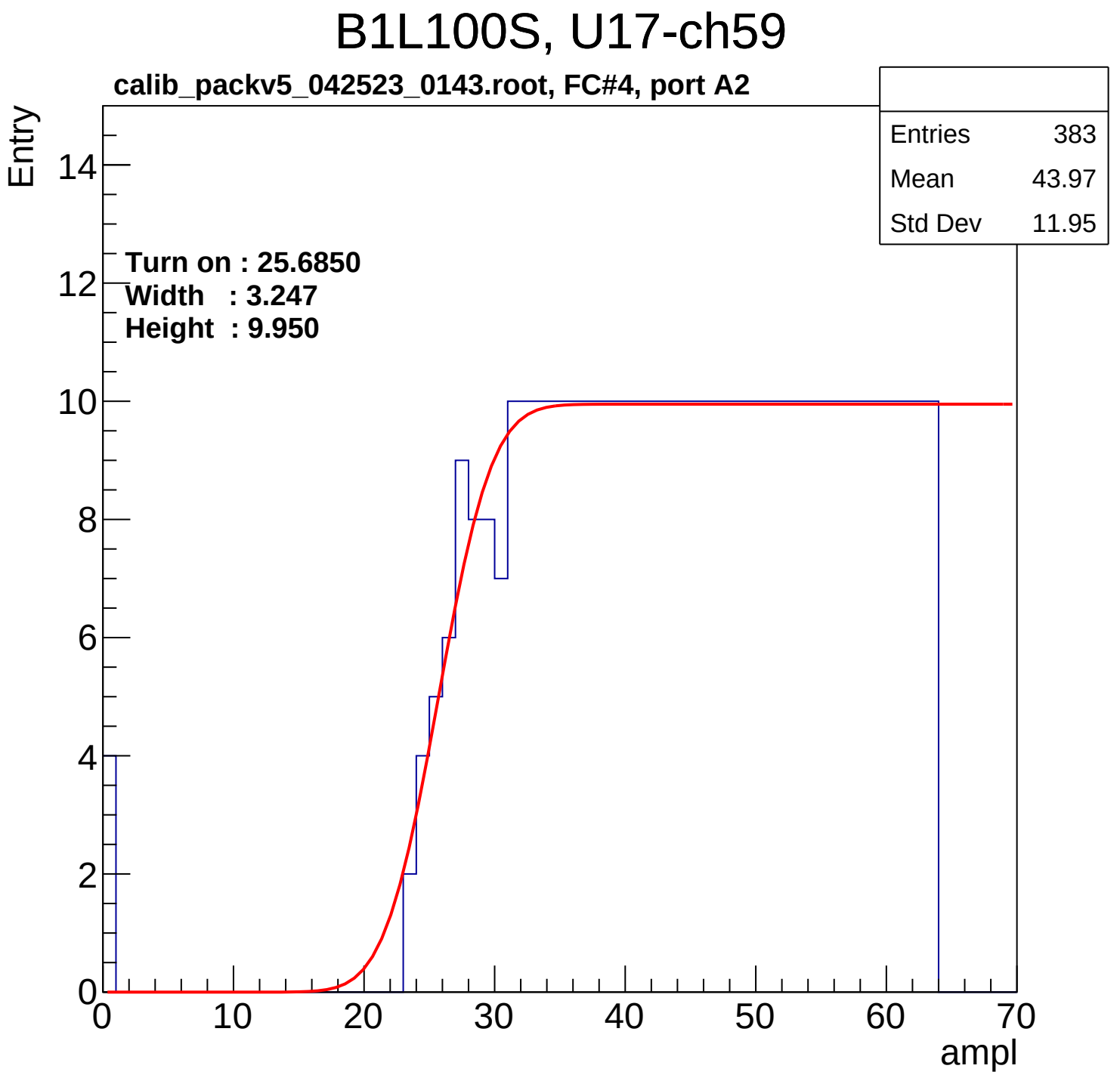
B1L100S, U17-ch59
calib_packv5_042523_0143.root, FC#4, port A2
Entries 383
Mean 43.97
Std Dev 11.95
Turn on : 25.6850
Width : 3.247
Height : 9.950
Entry
ampl
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2
4
6
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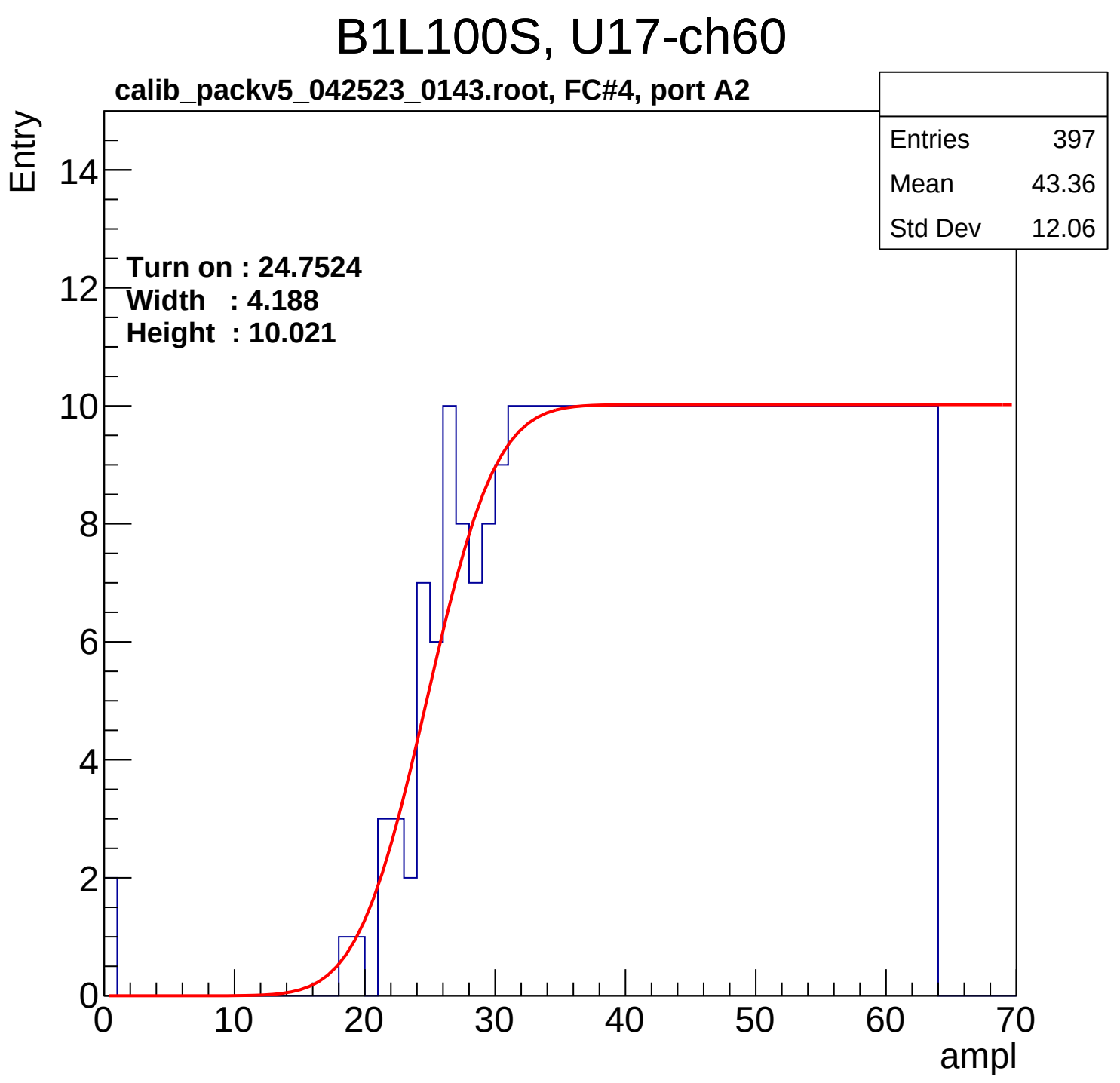
B1L100S, U17-ch60
calib_packv5_042523_0143.root, FC#4, port A2
Entries 397
Mean 43.36
Std Dev 12.06
Turn on : 24.7524
Width : 4.188
Height : 10.021
Entry
ampl
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2
4
6
8
10
12
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0
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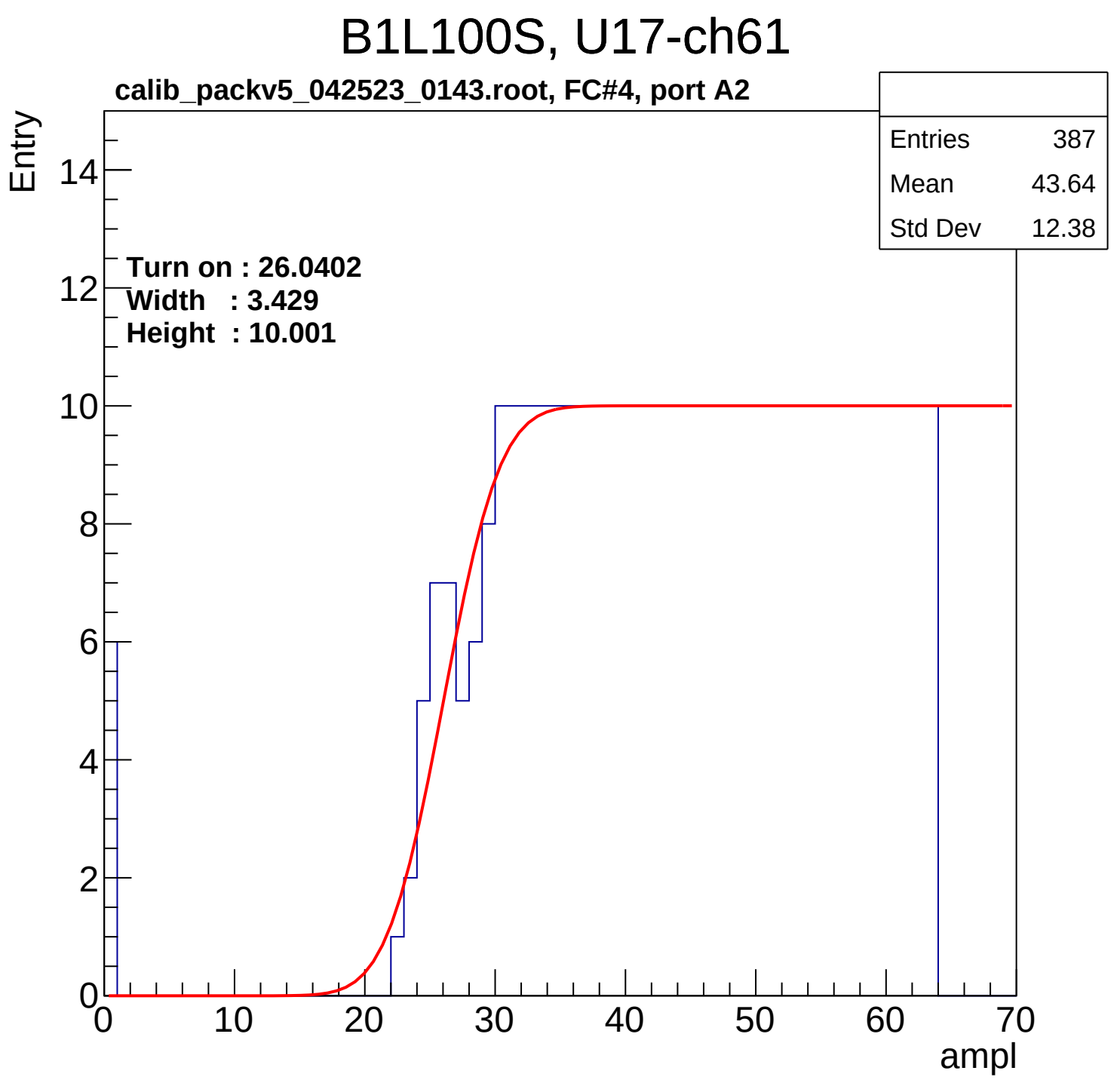
B1L100S, U17-ch61
calib_packv5_042523_0143.root, FC#4, port A2
Entries 387
Mean 43.64
Std Dev 12.38
Turn on : 26.0402
Width : 3.429
Height : 10.001
Entry
ampl
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2
4
6
8
10
12
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0
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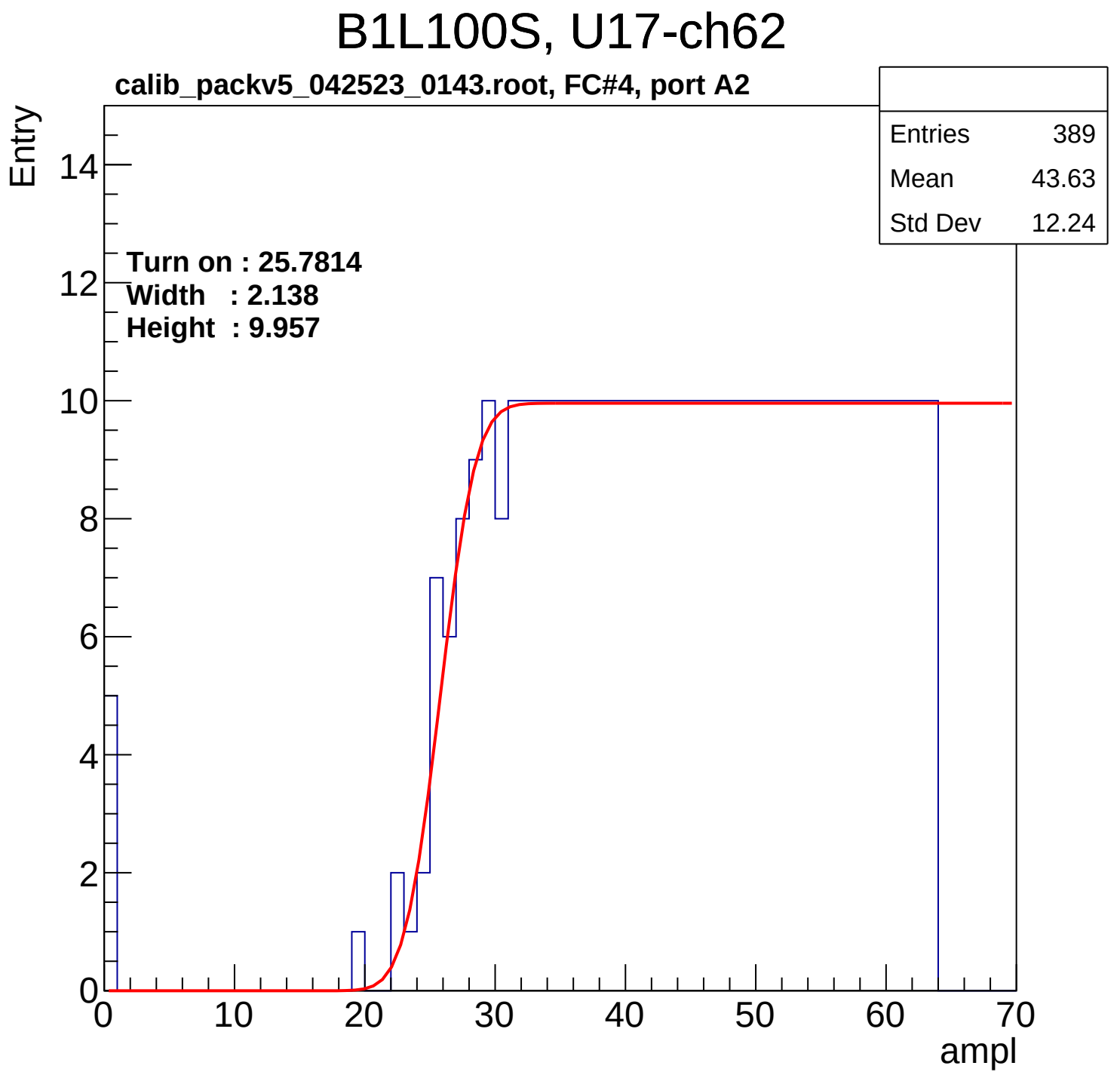
B1L100S, U17-ch62
calib_packv5_042523_0143.root, FC#4, port A2
Entries 389
Mean 43.63
Std Dev 12.24
Turn on : 25.7814
Width : 2.138
Height : 9.957
Entry
ampl
0
2
4
6
8
10
12
14
0
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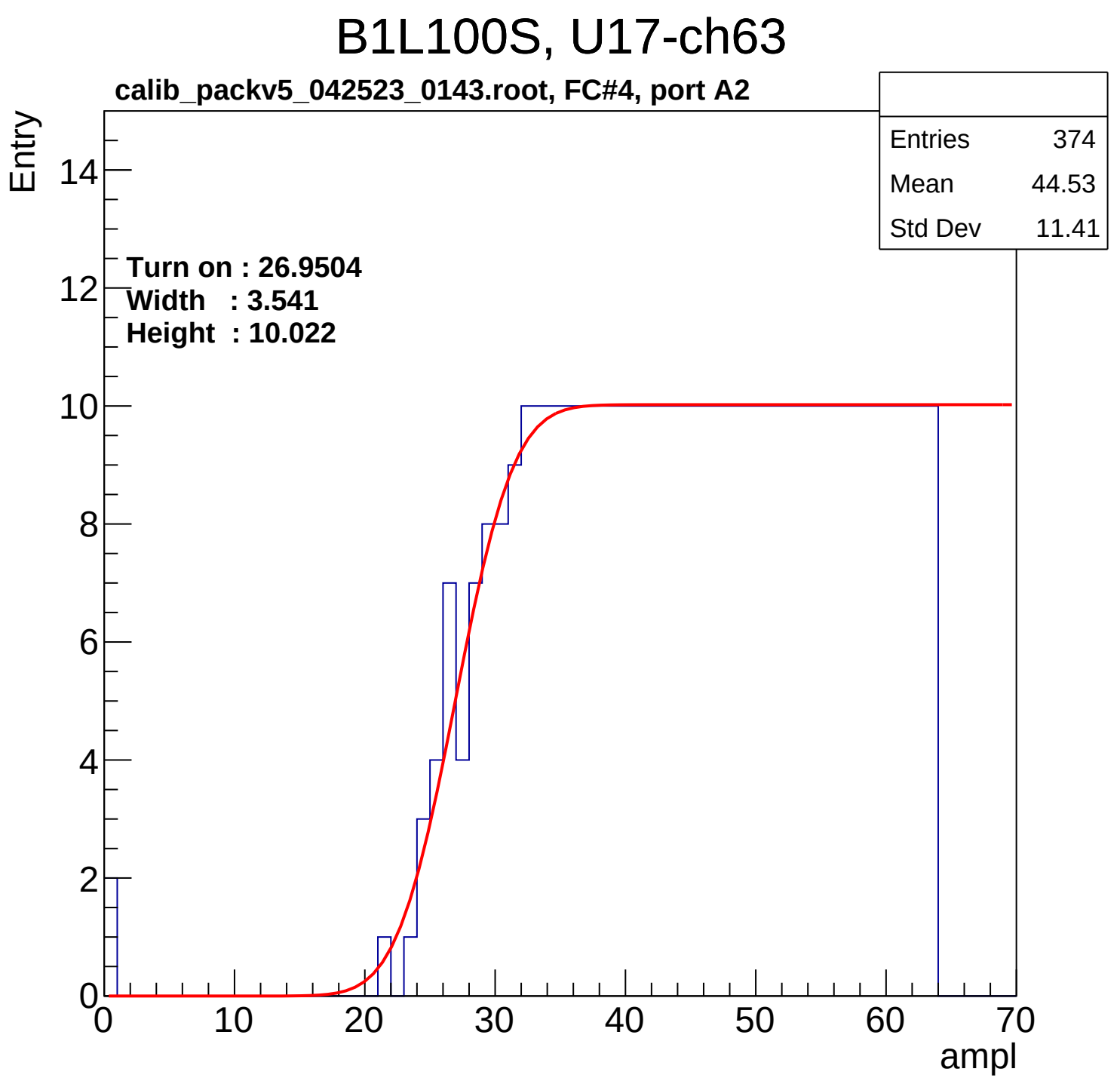
B1L100S, U17-ch63
calib_packv5_042523_0143.root, FC#4, port A2
Entries 374
Mean 44.53
Std Dev 11.41
Turn on : 26.9504
Width : 3.541
Height : 10.022
Entry
ampl
0
2
4
6
8
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12
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0
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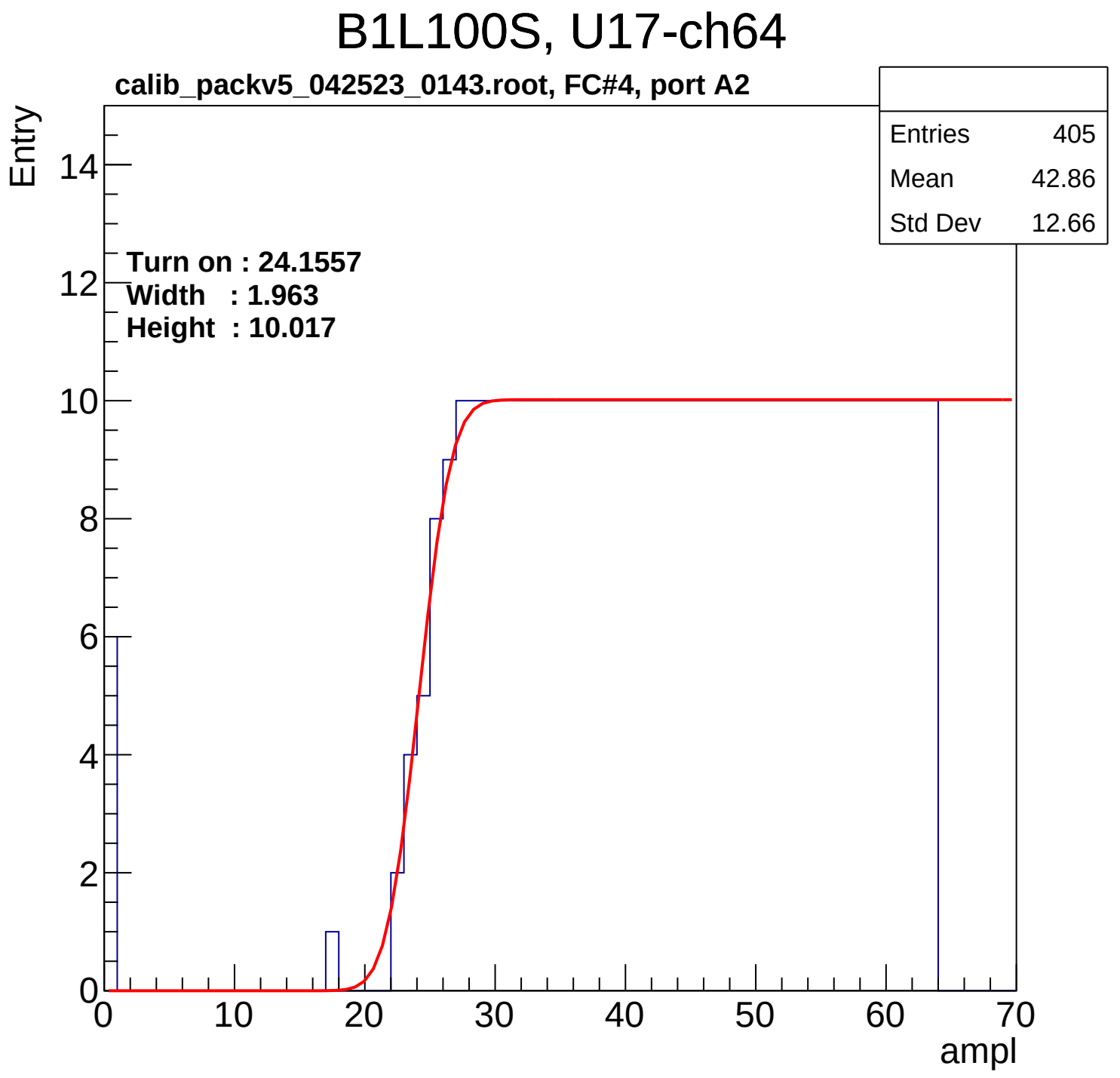
B1L100S, U17-ch64
calib_packv5_042523_0143.root, FC#4, port A2
Entries 405
Mean 42.86
Std Dev 12.66
Turn on : 24.1557
Width : 1.963
Height : 10.017
Entry
ampl
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2
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6
8
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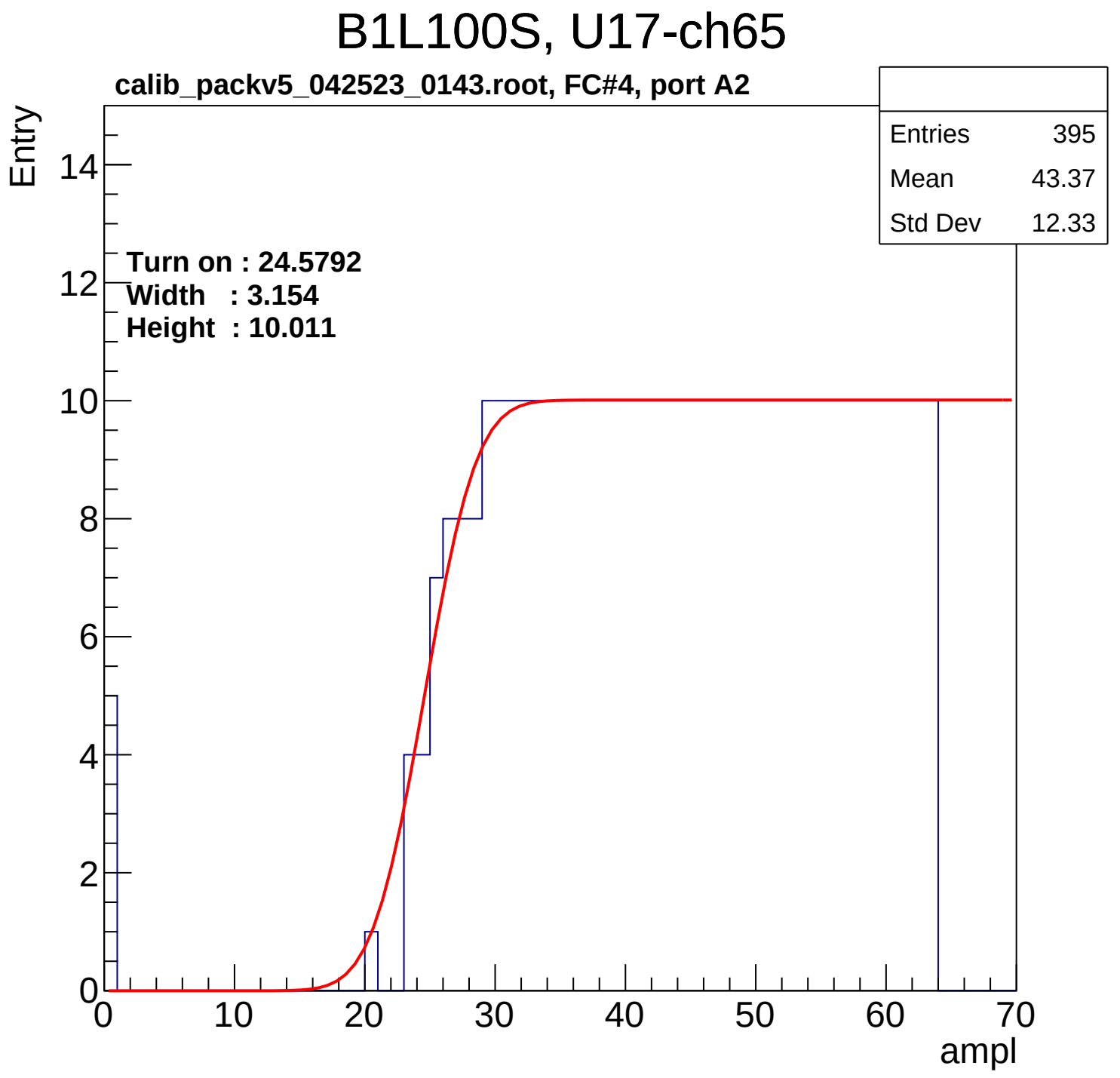
B1L100S, U17-ch65
calib_packv5_042523_0143.root, FC#4, port A2
Entries 395
Mean 43.37
Std Dev 12.33
Turn on : 24.5792
Width : 3.154
Height : 10.011
Entry
ampl
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2
4
6
8
10
12
14
0
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60
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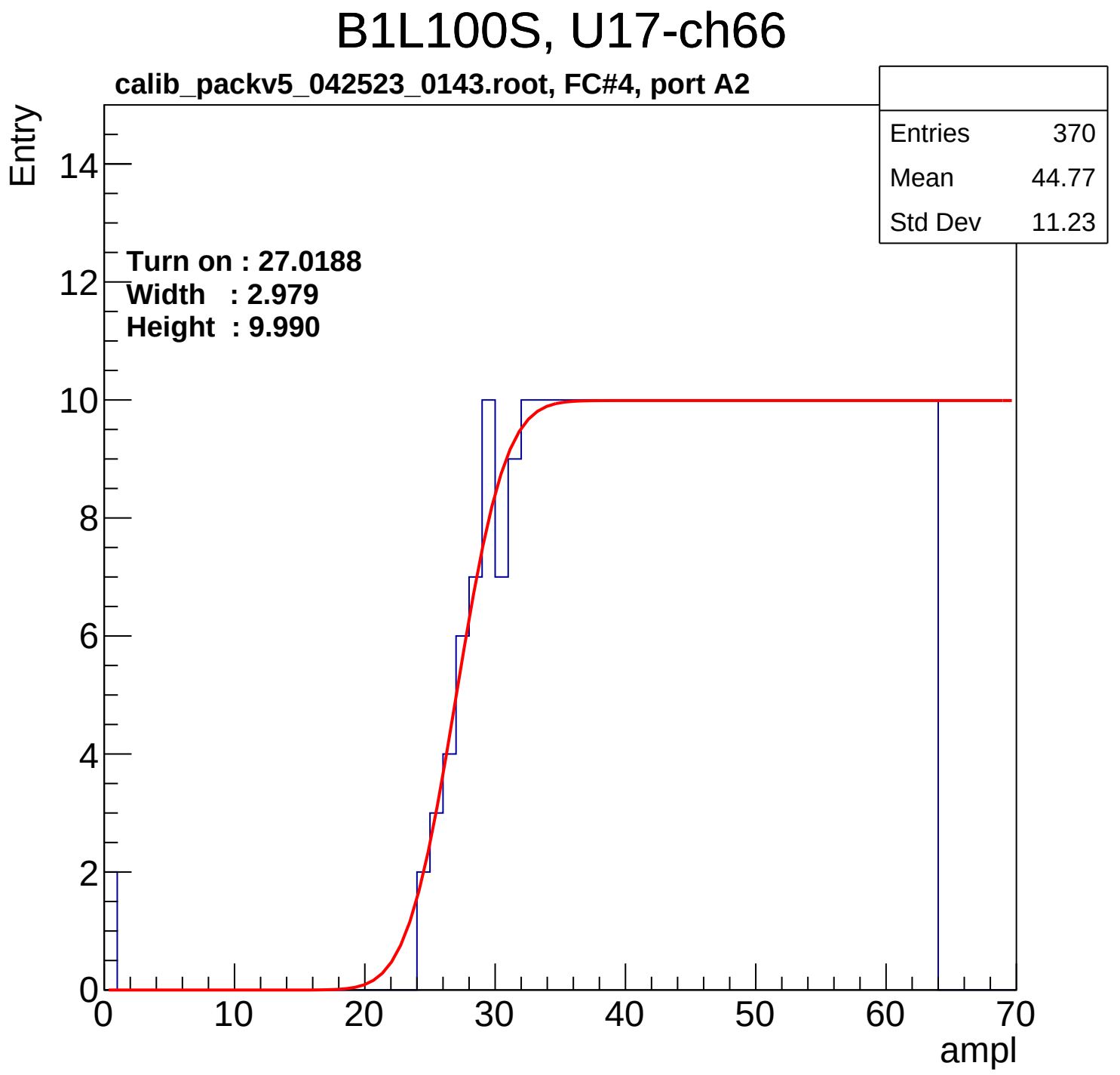
B1L100S, U17-ch66
calib_packv5_042523_0143.root, FC#4, port A2
Entries 370
Mean 44.77
Std Dev 11.23
Turn on : 27.0188
Width : 2.979
Height : 9.990
Entry
ampl
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2
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6
8
10
12
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0
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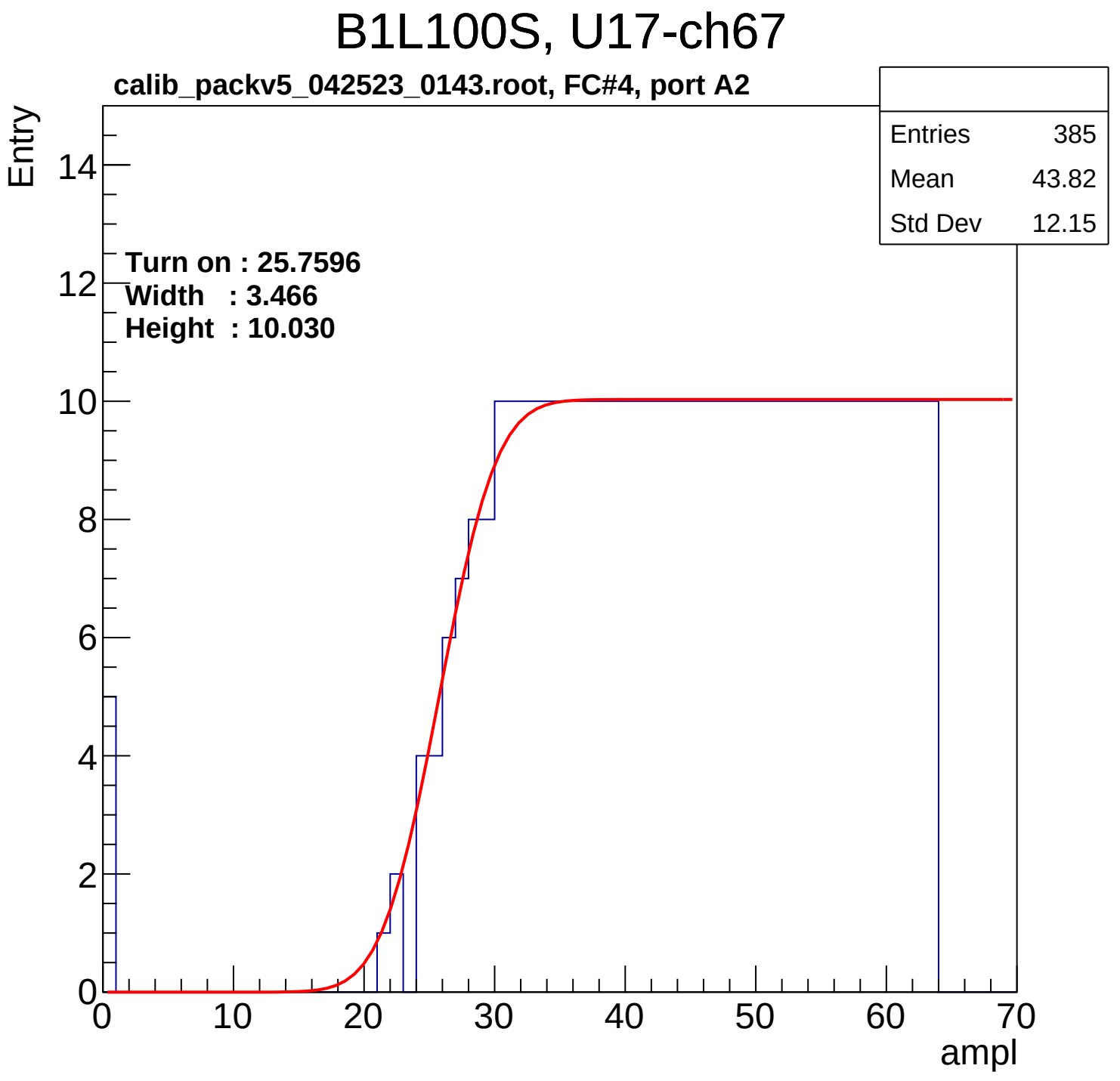
B1L100S, U17-ch67
calib_packv5_042523_0143.root, FC#4, port A2
Entries 385
Mean 43.82
Std Dev 12.15
Turn on : 25.7596
Width : 3.466
Height : 10.030
Entry
ampl
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2
4
6
8
10
12
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0
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60
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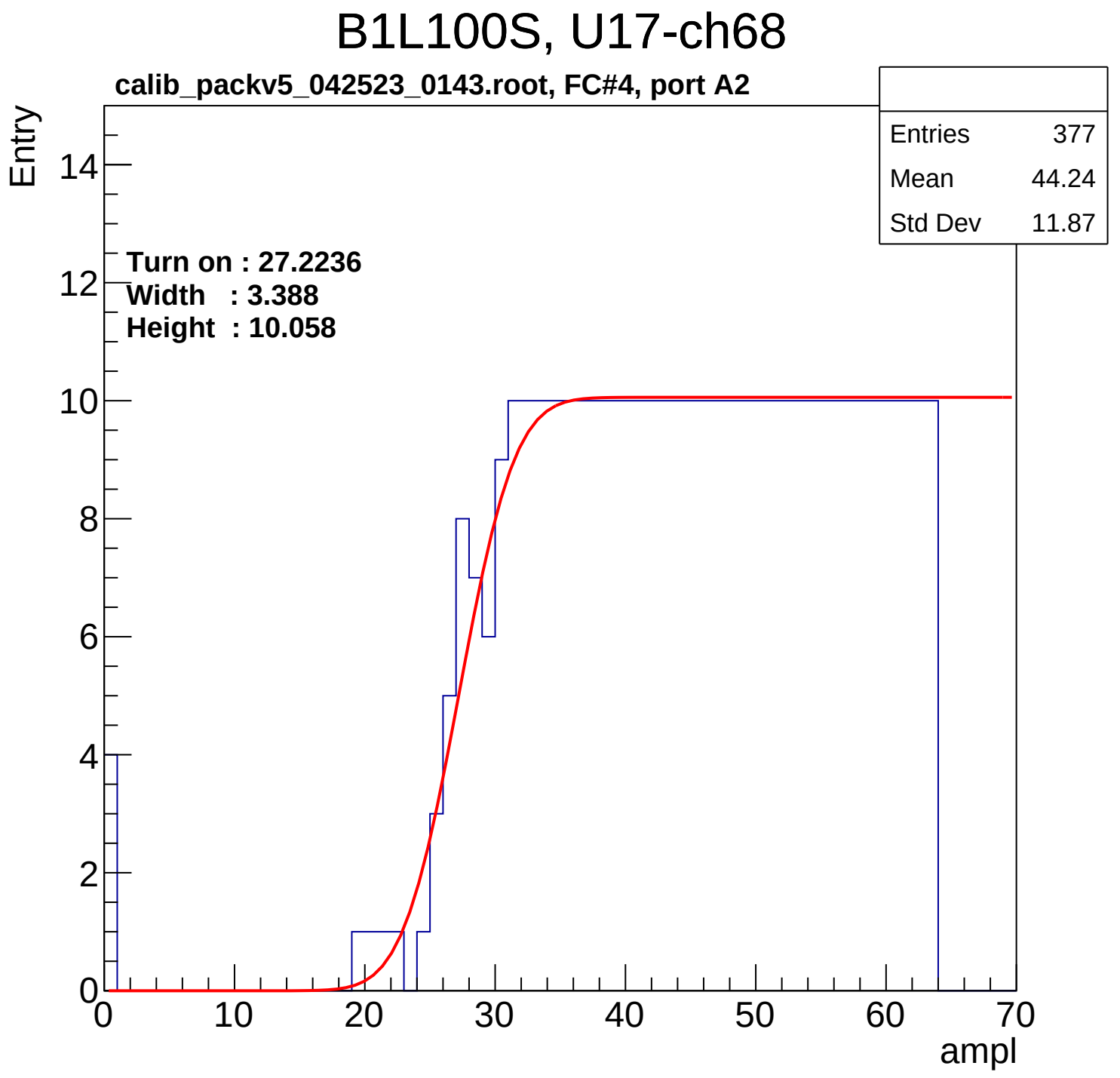
B1L100S, U17-ch68
calib_packv5_042523_0143.root, FC#4, port A2
Entries 377
Mean 44.24
Std Dev 11.87
Turn on : 27.2236
Width : 3.388
Height : 10.058
Entry
ampl
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6
8
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0
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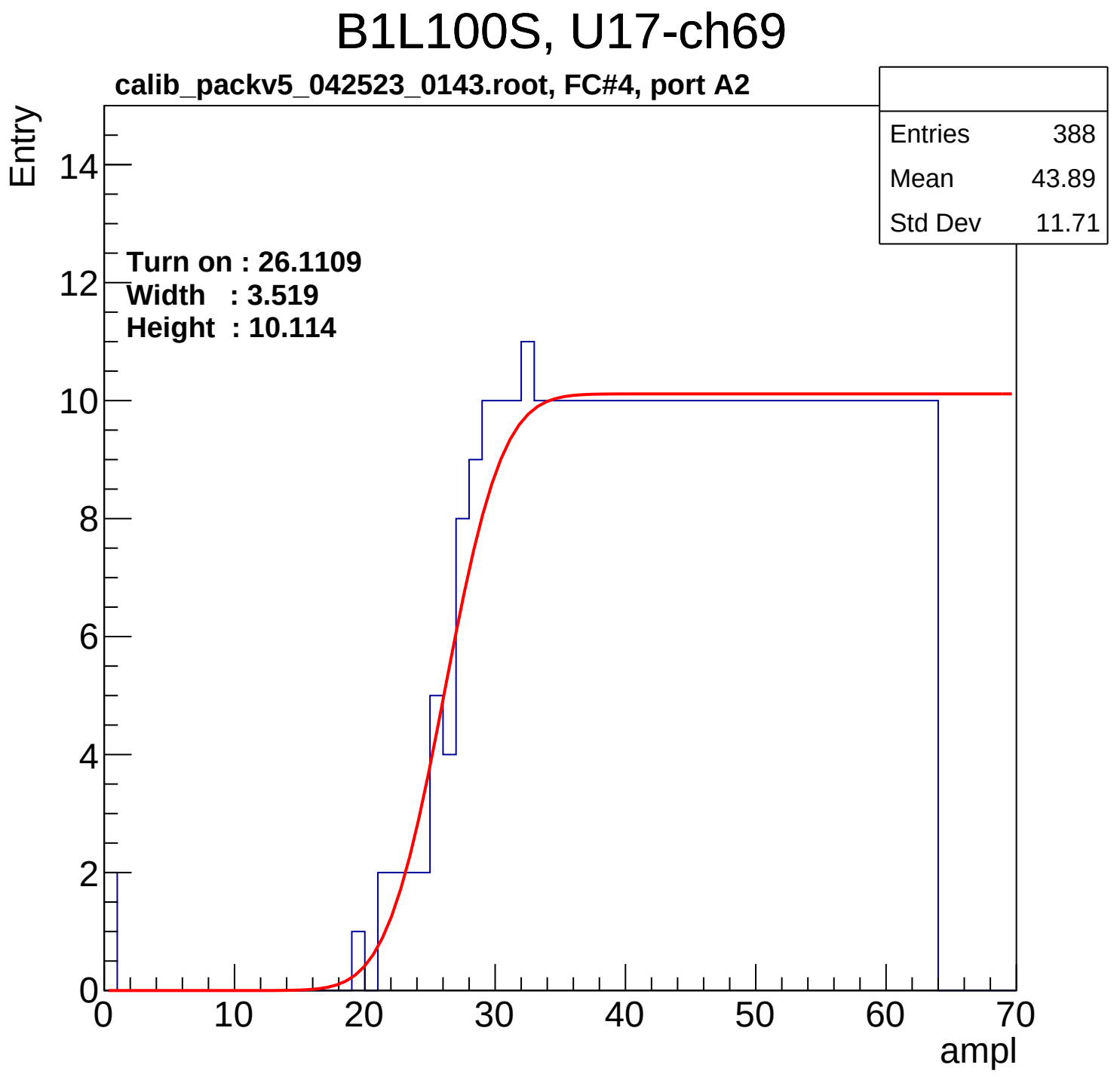
B1L100S, U17-ch69
calib_packv5_042523_0143.root, FC#4, port A2
Entries 388
Mean 43.89
Std Dev 11.71
Turn on : 26.1109
Width : 3.519
Height : 10.114
Entry
ampl
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2
4
6
8
10
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0
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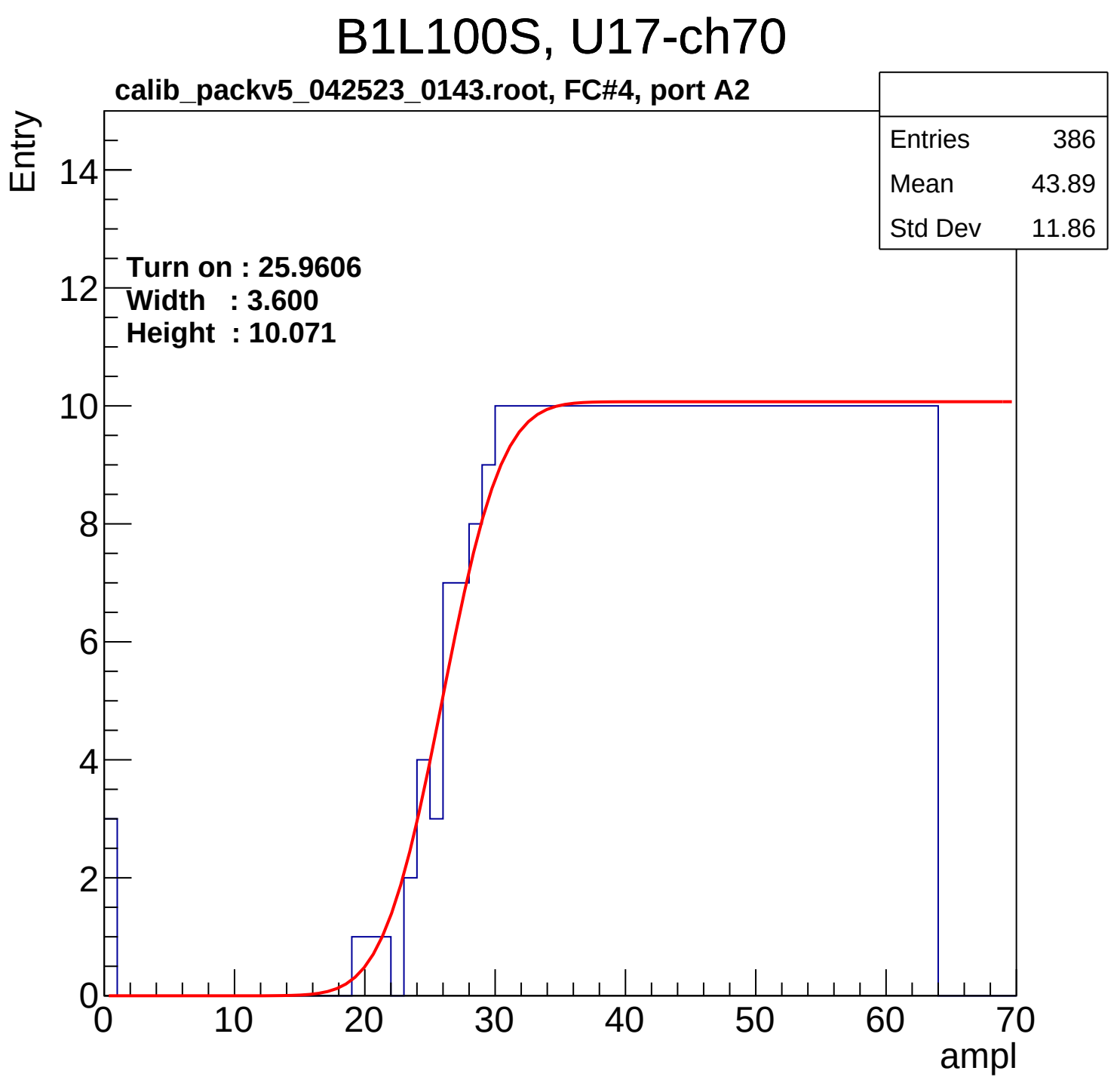
B1L100S, U17-ch70
calib_packv5_042523_0143.root, FC#4, port A2
Entries 386
Mean 43.89
Std Dev 11.86
Turn on : 25.9606
Width : 3.600
Height : 10.071
Entry
ampl
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6
8
10
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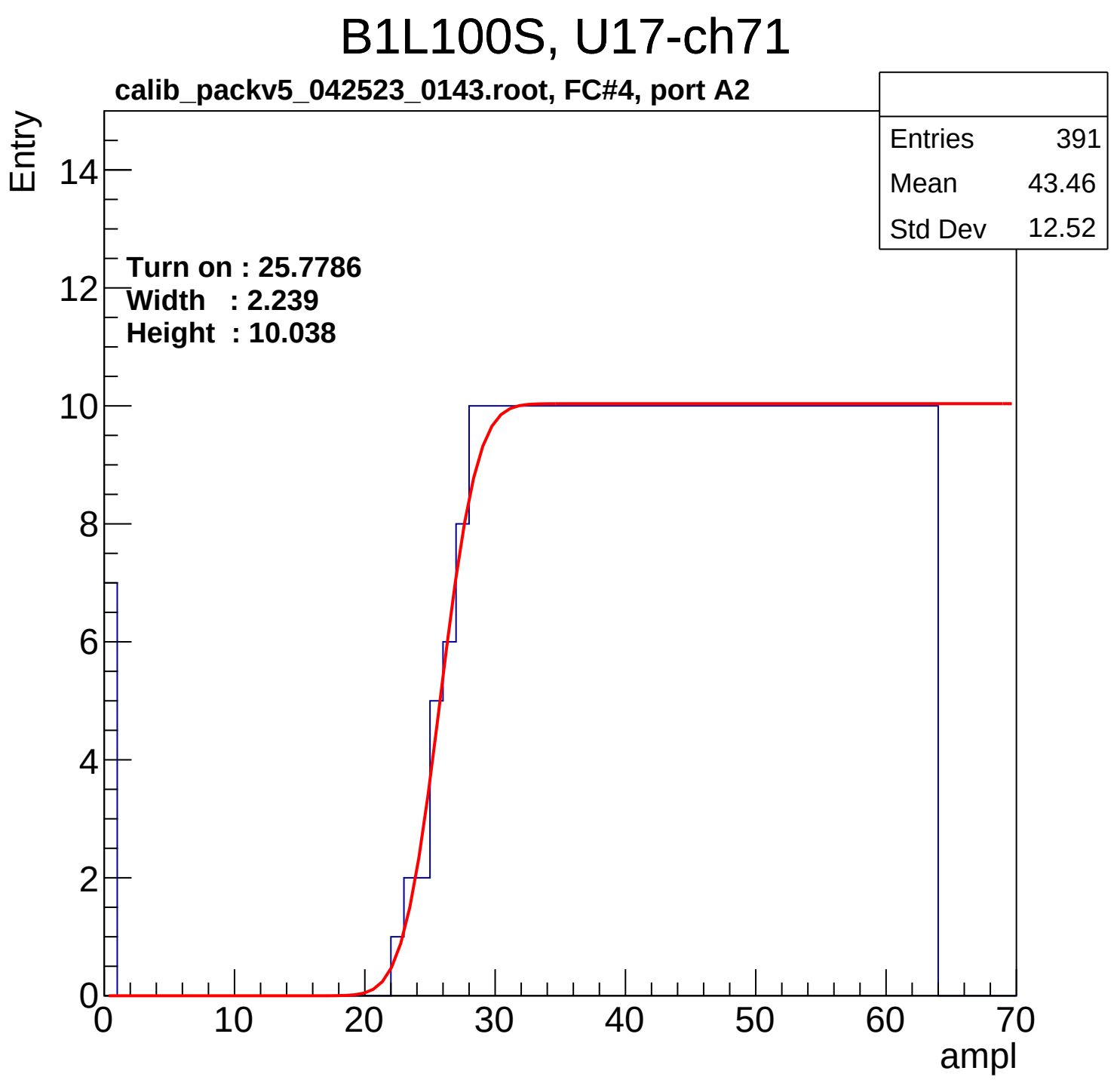
B1L100S, U17-ch71
calib_packv5_042523_0143.root, FC#4, port A2
Entries 391
Mean 43.46
Std Dev 12.52
Turn on : 25.7786
Width : 2.239
Height : 10.038
Entry
ampl
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6
8
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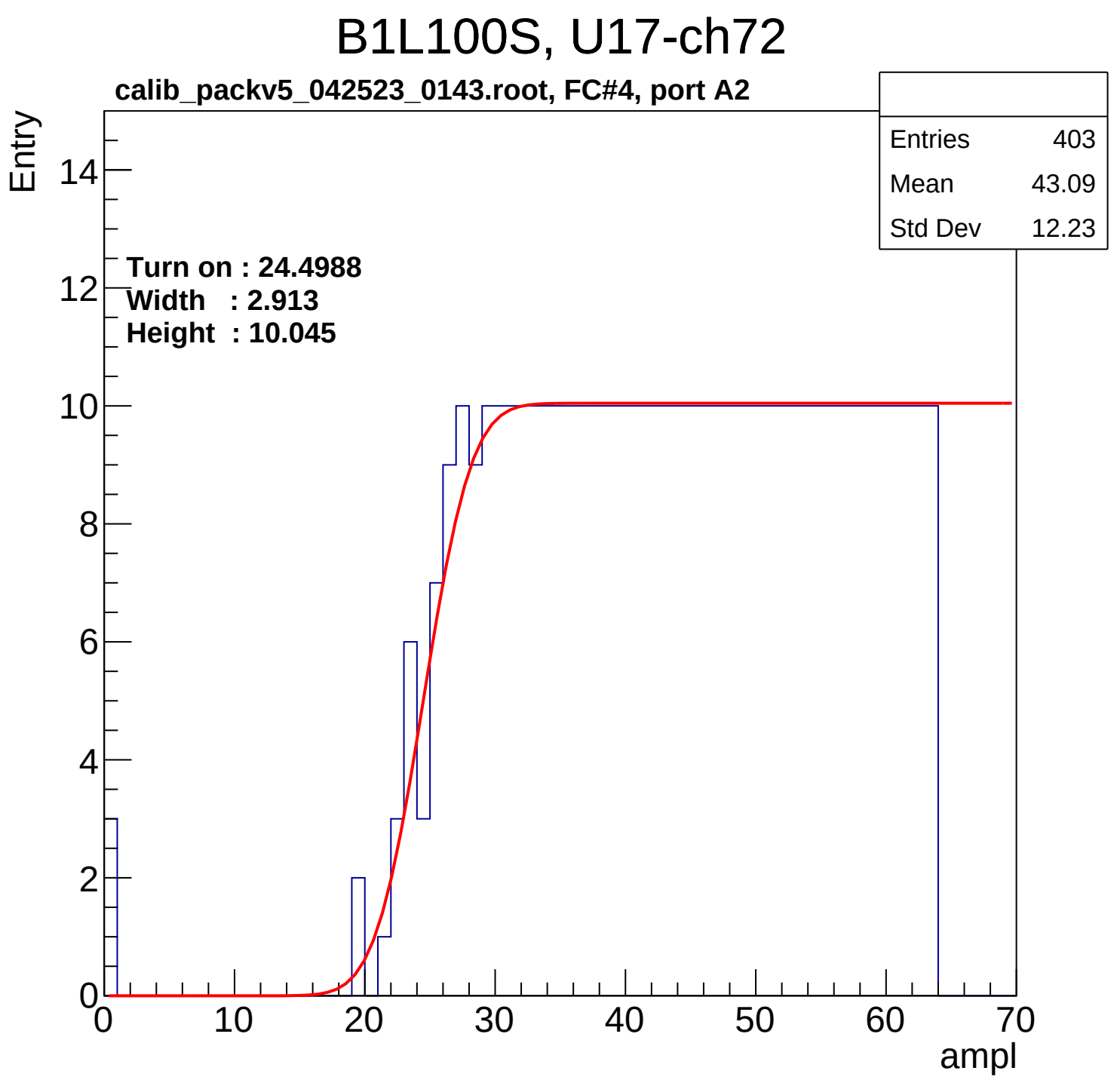
B1L100S, U17-ch72
calib_packv5_042523_0143.root, FC#4, port A2
Entries 403
Mean 43.09
Std Dev 12.23
Turn on : 24.4988
Width : 2.913
Height : 10.045
Entry
ampl
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6
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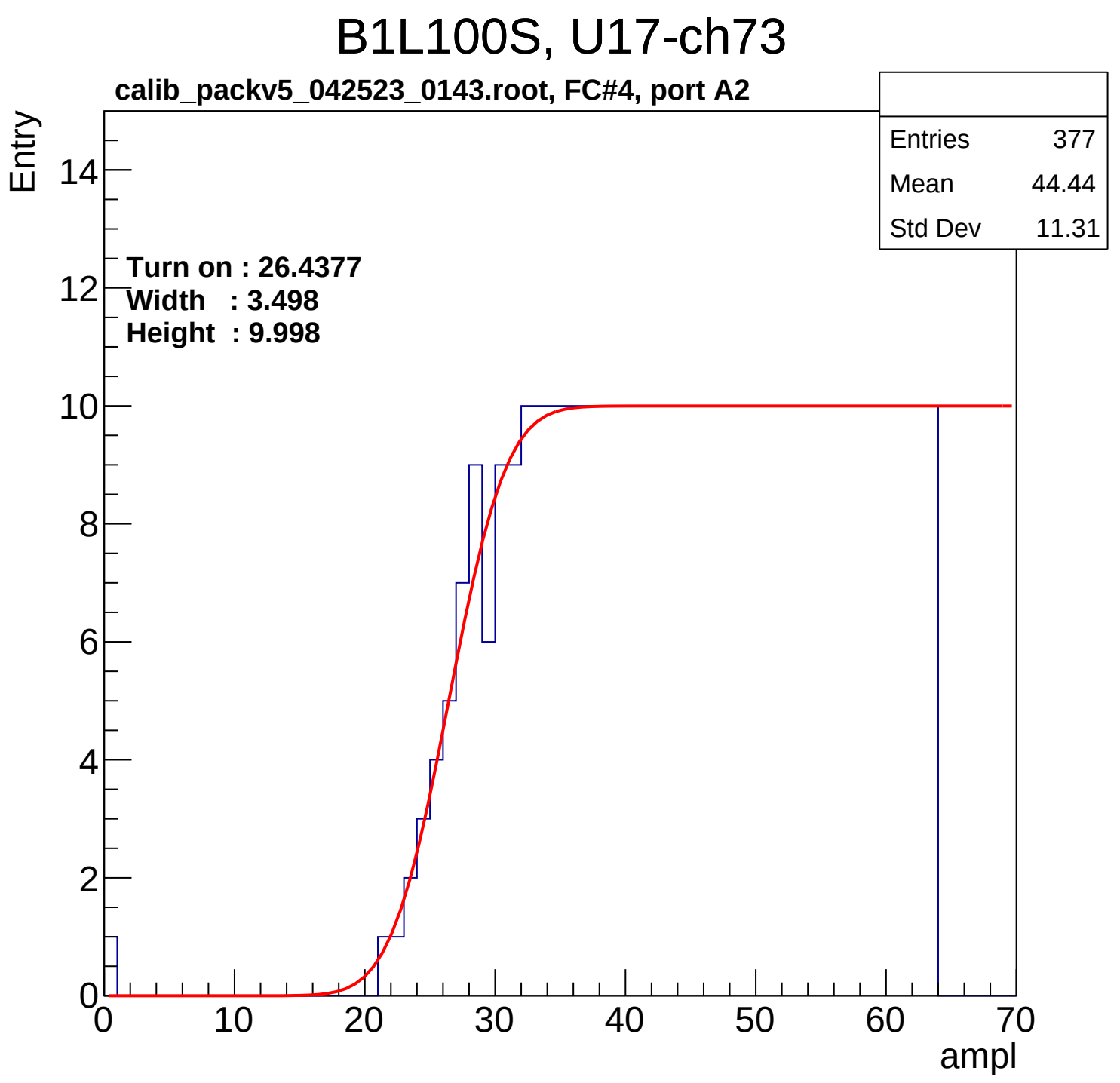
B1L100S, U17-ch73
calib_packv5_042523_0143.root, FC#4, port A2
Entries 377
Mean 44.44
Std Dev 11.31
Turn on : 26.4377
Width : 3.498
Height : 9.998
Entry
ampl
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8
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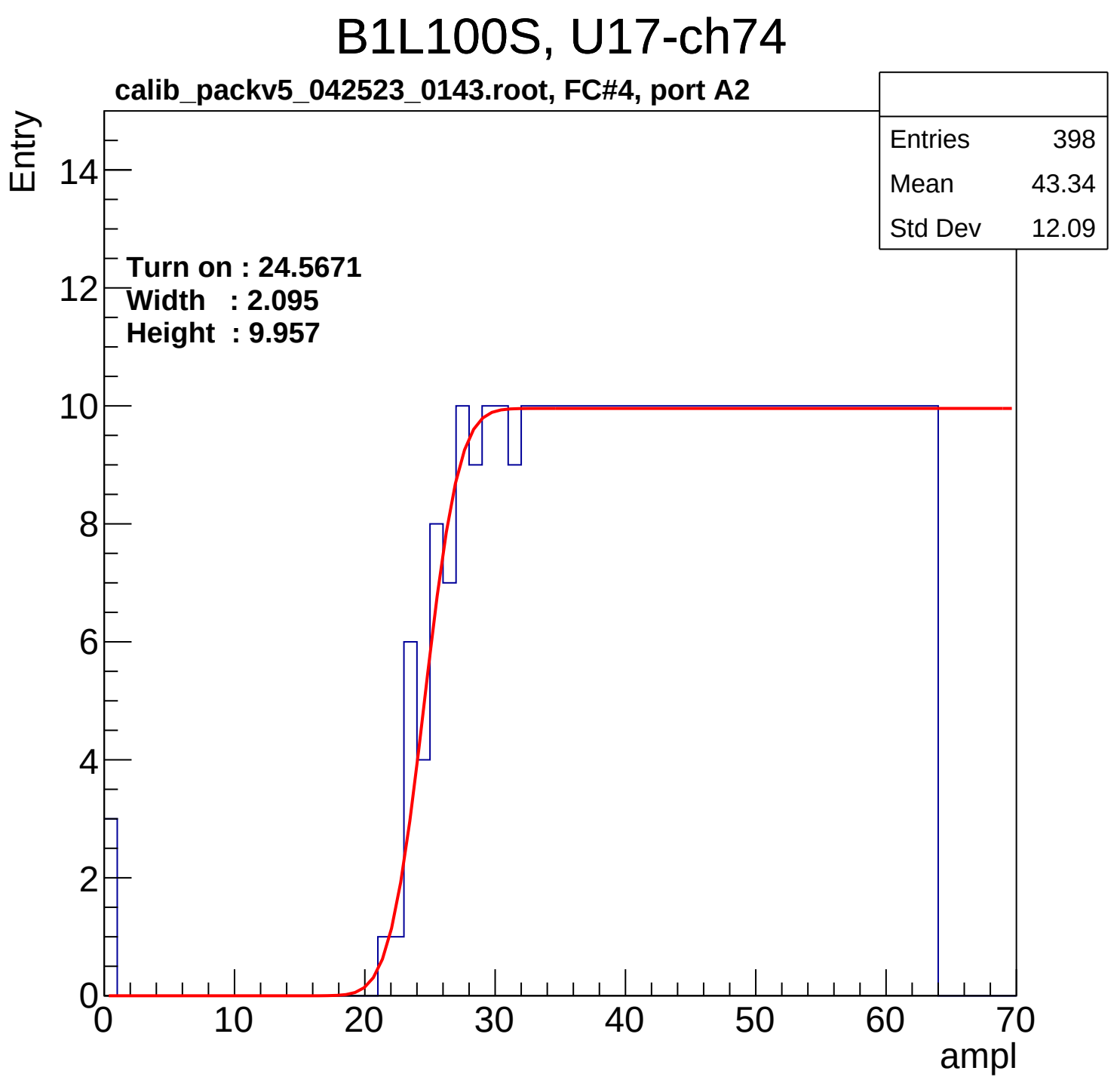
B1L100S, U17-ch74
calib_packv5_042523_0143.root, FC#4, port A2
Entries 398
Mean 43.34
Std Dev 12.09
Turn on : 24.5671
Width : 2.095
Height : 9.957
Entry
ampl
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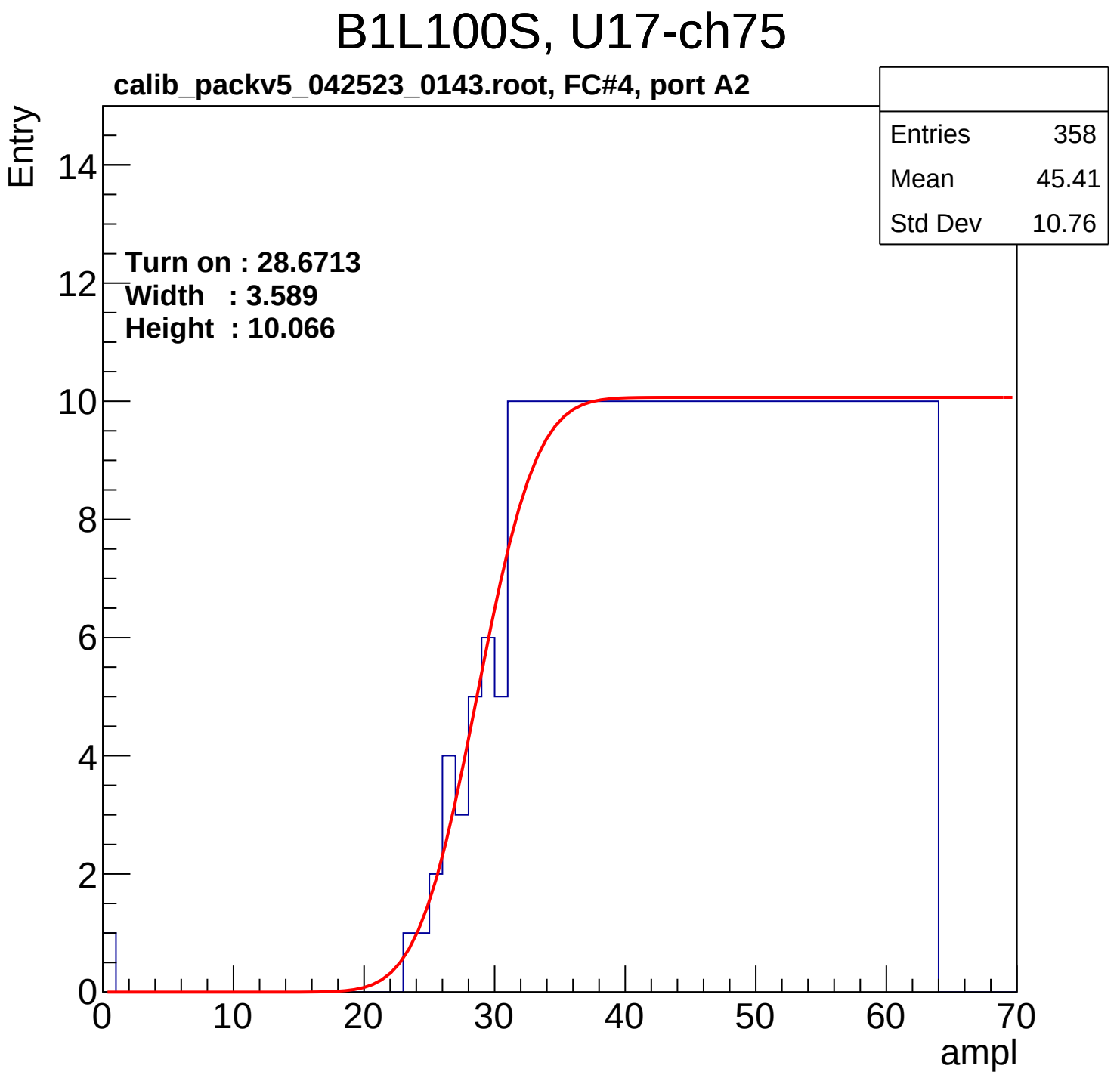
B1L100S, U17-ch75
calib_packv5_042523_0143.root, FC#4, port A2
Entries 358
Mean 45.41
Std Dev 10.76
Turn on : 28.6713
Width : 3.589
Height : 10.066
Entry
ampl
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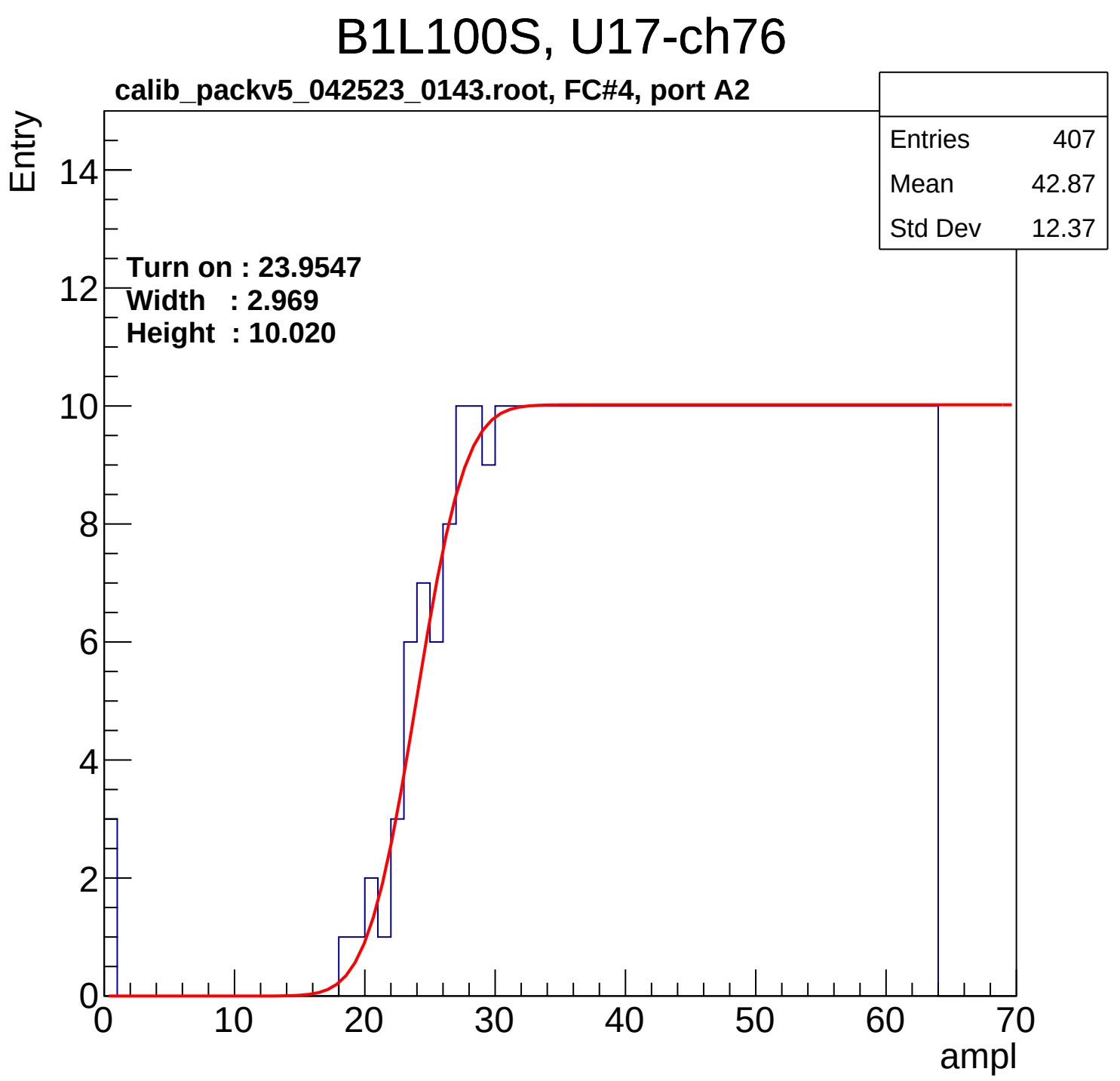
B1L100S, U17-ch76
calib_packv5_042523_0143.root, FC#4, port A2
Entries 407
Mean 42.87
Std Dev 12.37
Turn on : 23.9547
Width : 2.969
Height : 10.020
Entry
ampl
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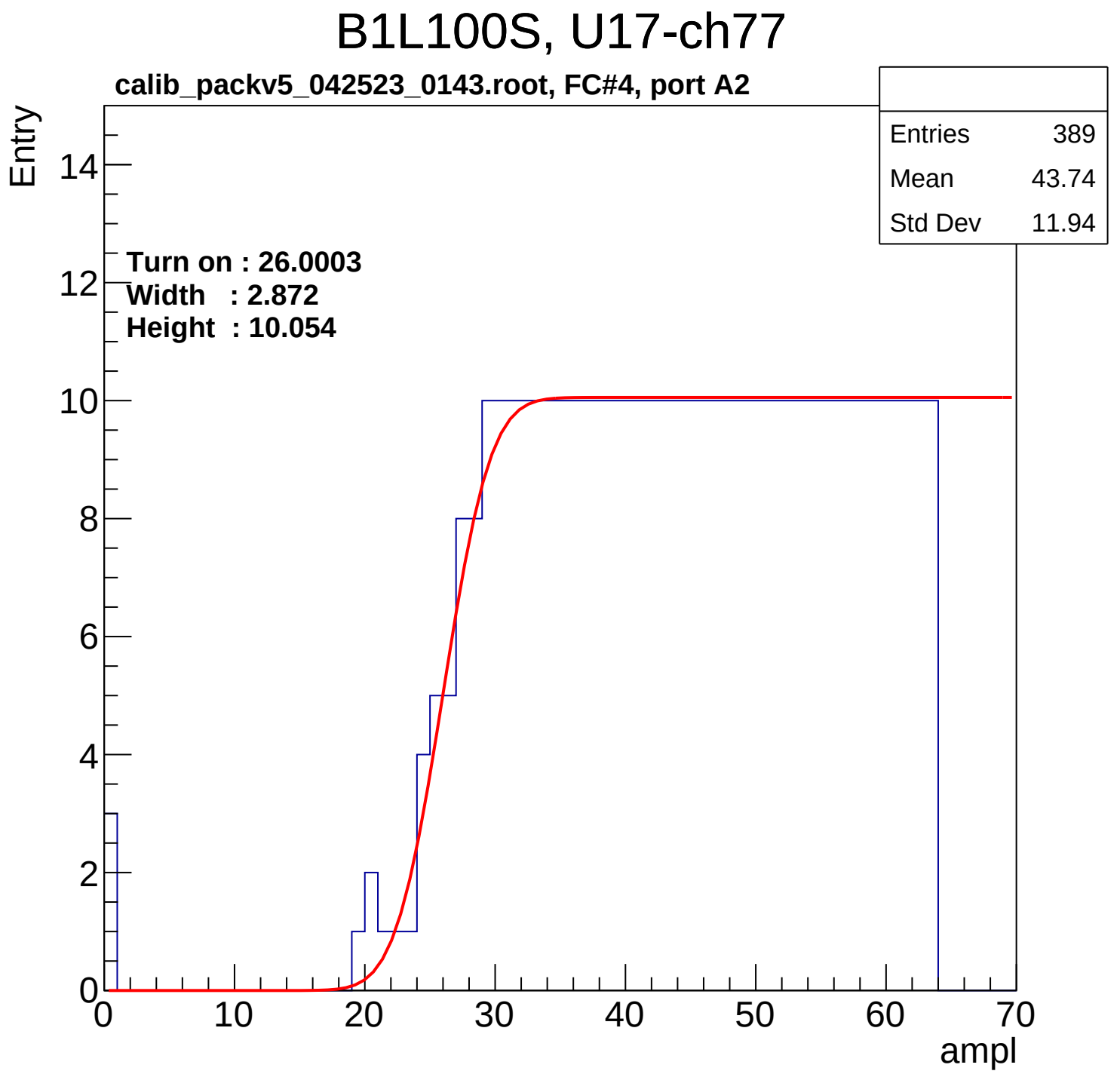
B1L100S, U17-ch77
calib_packv5_042523_0143.root, FC#4, port A2
Entries 389
Mean 43.74
Std Dev 11.94
Turn on : 26.0003
Width : 2.872
Height : 10.054
Entry
ampl
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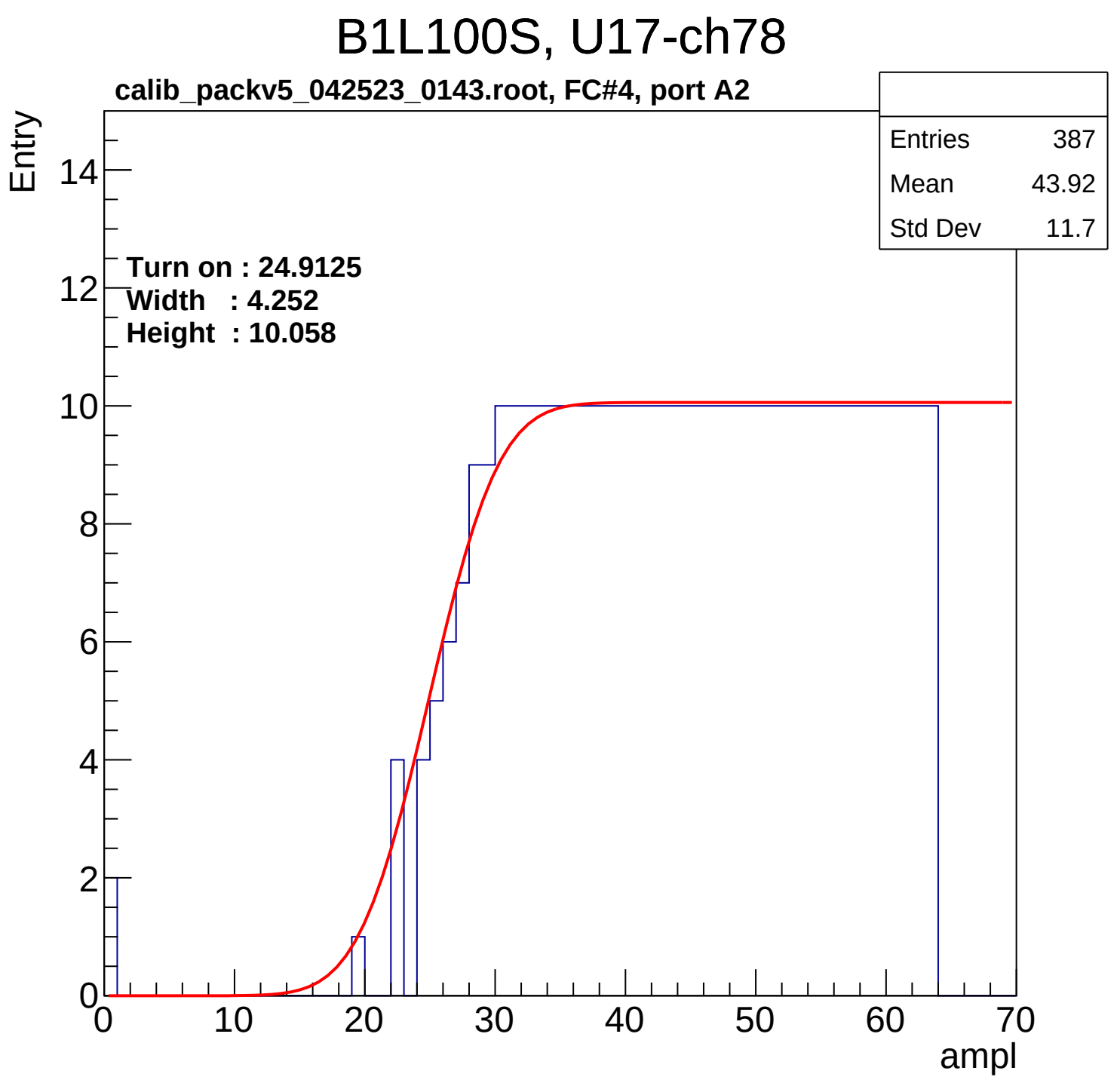
B1L100S, U17-ch78
calib_packv5_042523_0143.root, FC#4, port A2
Entries 387
Mean 43.92
Std Dev 11.7
Turn on : 24.9125
Width : 4.252
Height : 10.058
Entry
ampl
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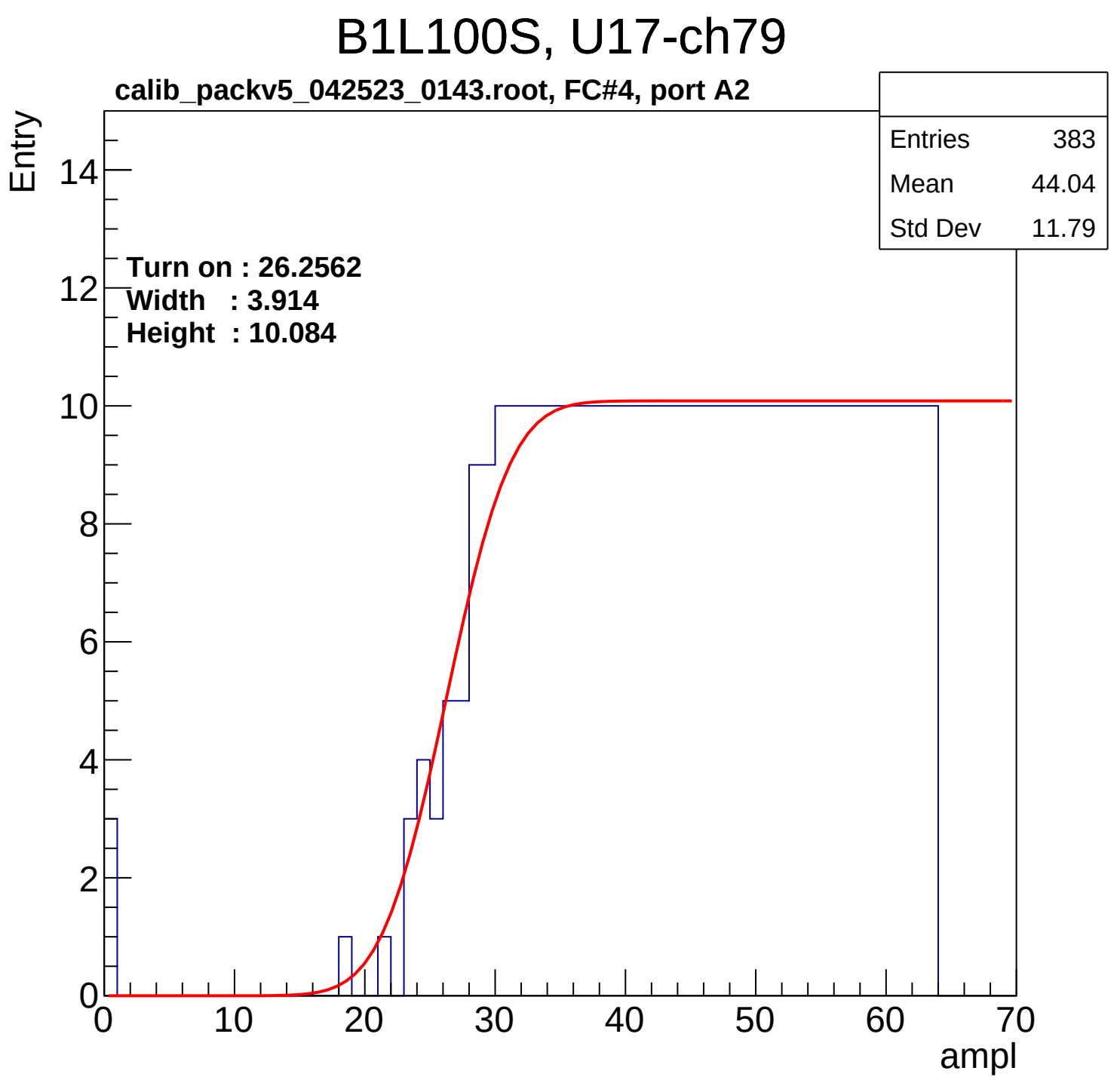
B1L100S, U17-ch79
calib_packv5_042523_0143.root, FC#4, port A2
Entries 383
Mean 44.04
Std Dev 11.79
Turn on : 26.2562
Width : 3.914
Height : 10.084
Entry
ampl
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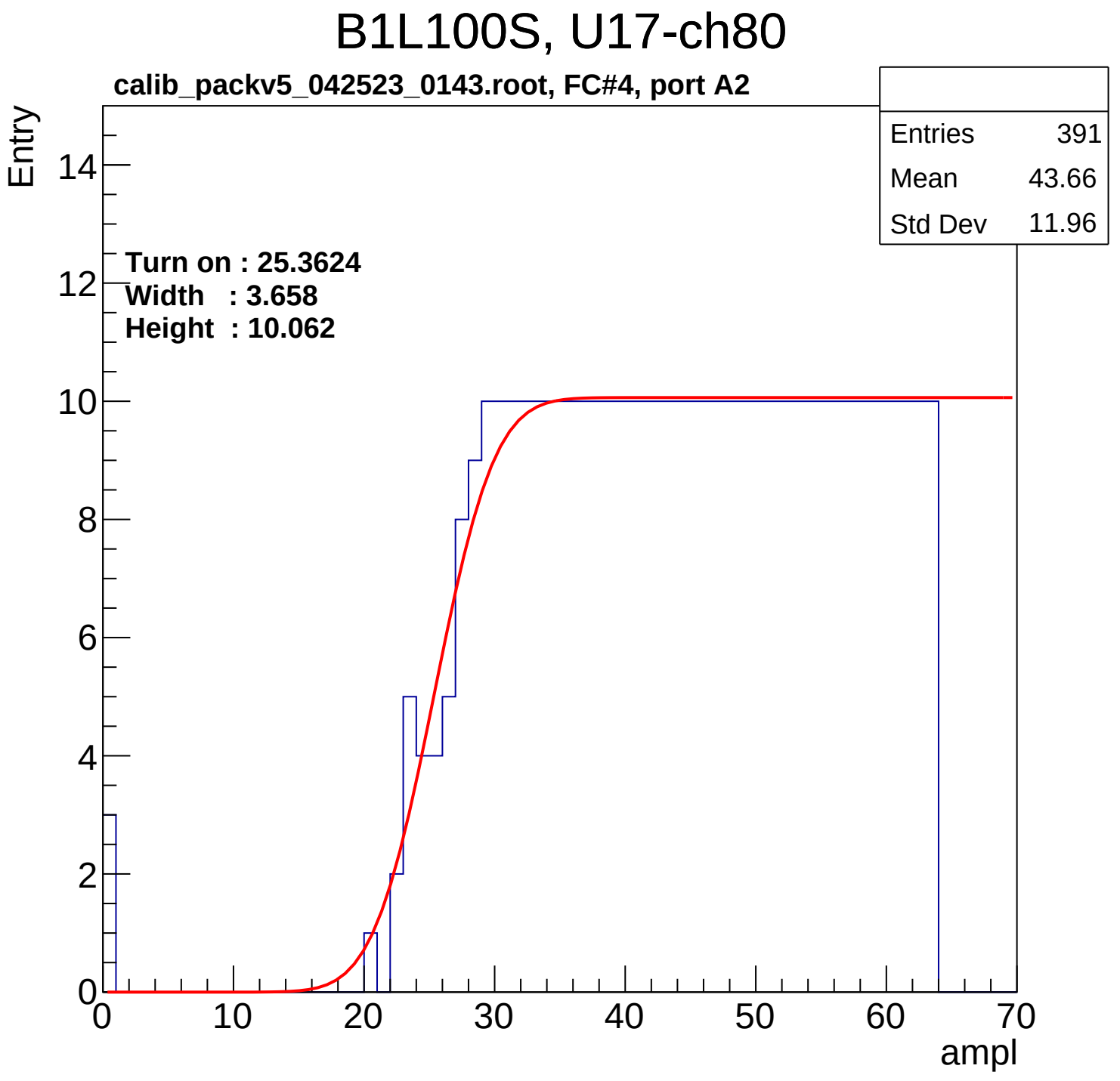
B1L100S, U17-ch80
calib_packv5_042523_0143.root, FC#4, port A2
Entries 391
Mean 43.66
Std Dev 11.96
Turn on : 25.3624
Width : 3.658
Height : 10.062
Entry
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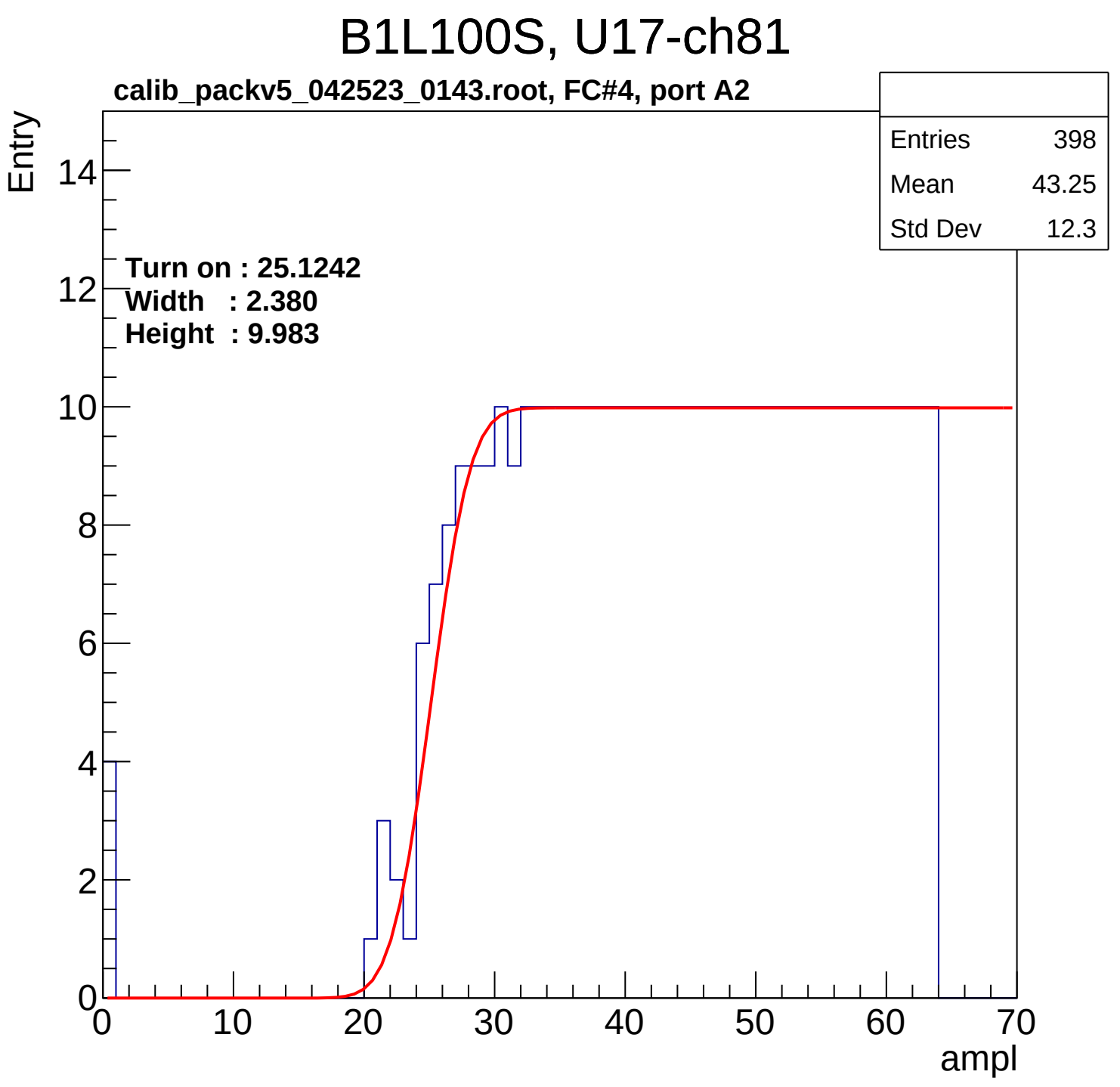
B1L100S, U17-ch81
calib_packv5_042523_0143.root, FC#4, port A2
Entries 398
Mean 43.25
Std Dev 12.3
Turn on : 25.1242
Width : 2.380
Height : 9.983
Entry
ampl
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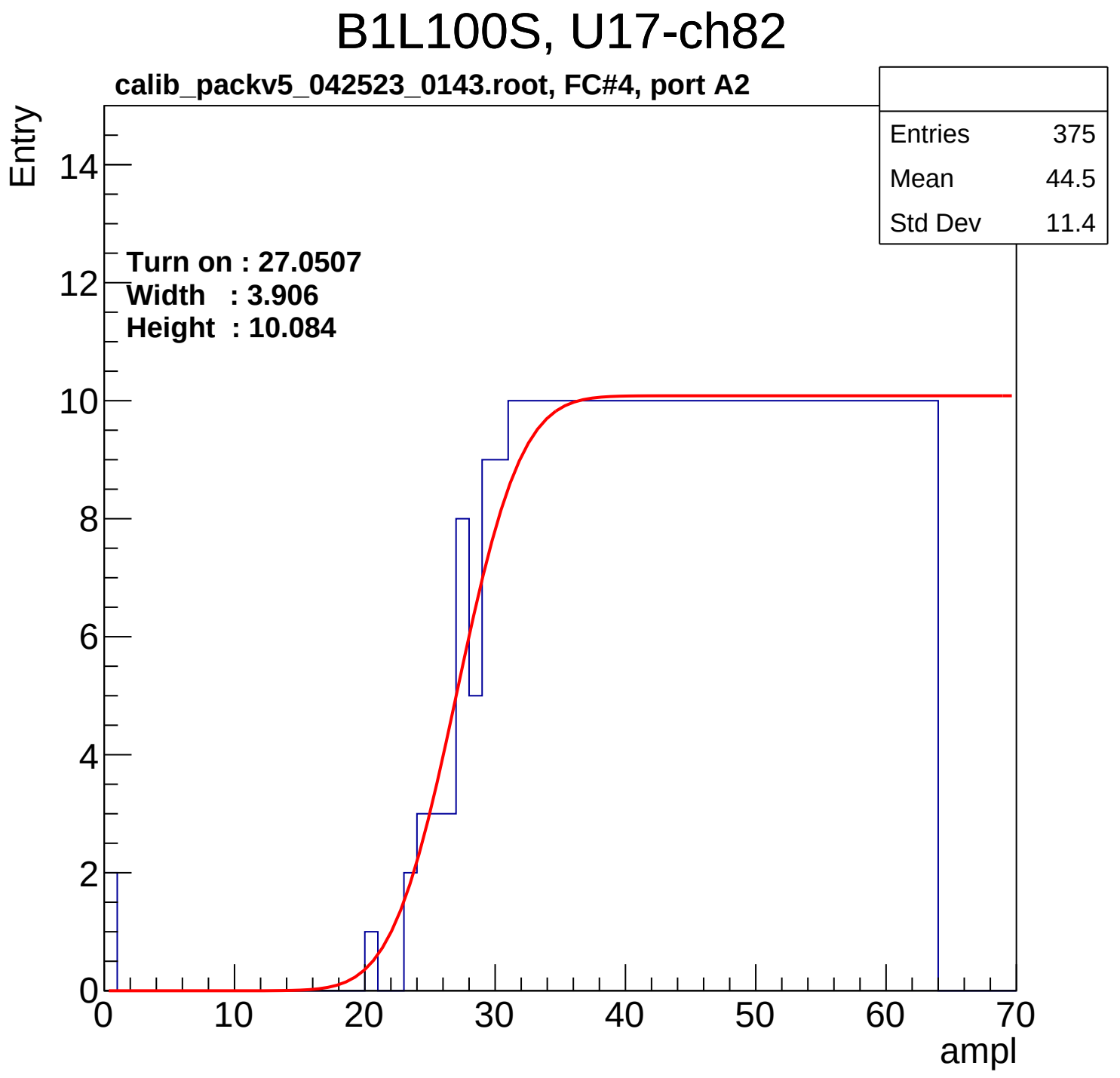
B1L100S, U17-ch82
calib_packv5_042523_0143.root, FC#4, port A2
Entries 375
Mean 44.5
Std Dev 11.4
Turn on : 27.0507
Width : 3.906
Height : 10.084
Entry
ampl
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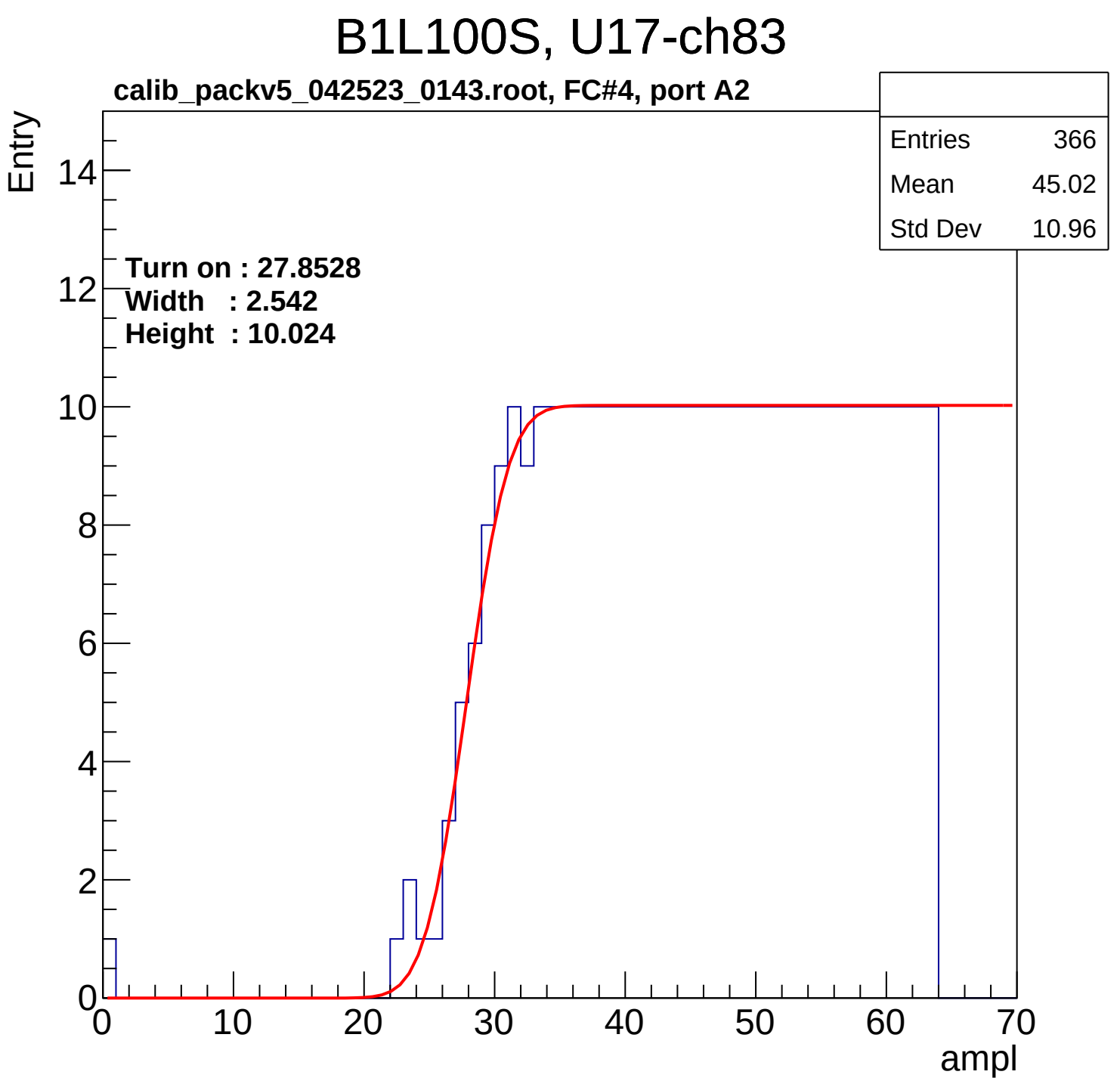
B1L100S, U17-ch83
calib_packv5_042523_0143.root, FC#4, port A2
Entries 366
Mean 45.02
Std Dev 10.96
Turn on : 27.8528
Width : 2.542
Height : 10.024
Entry
ampl
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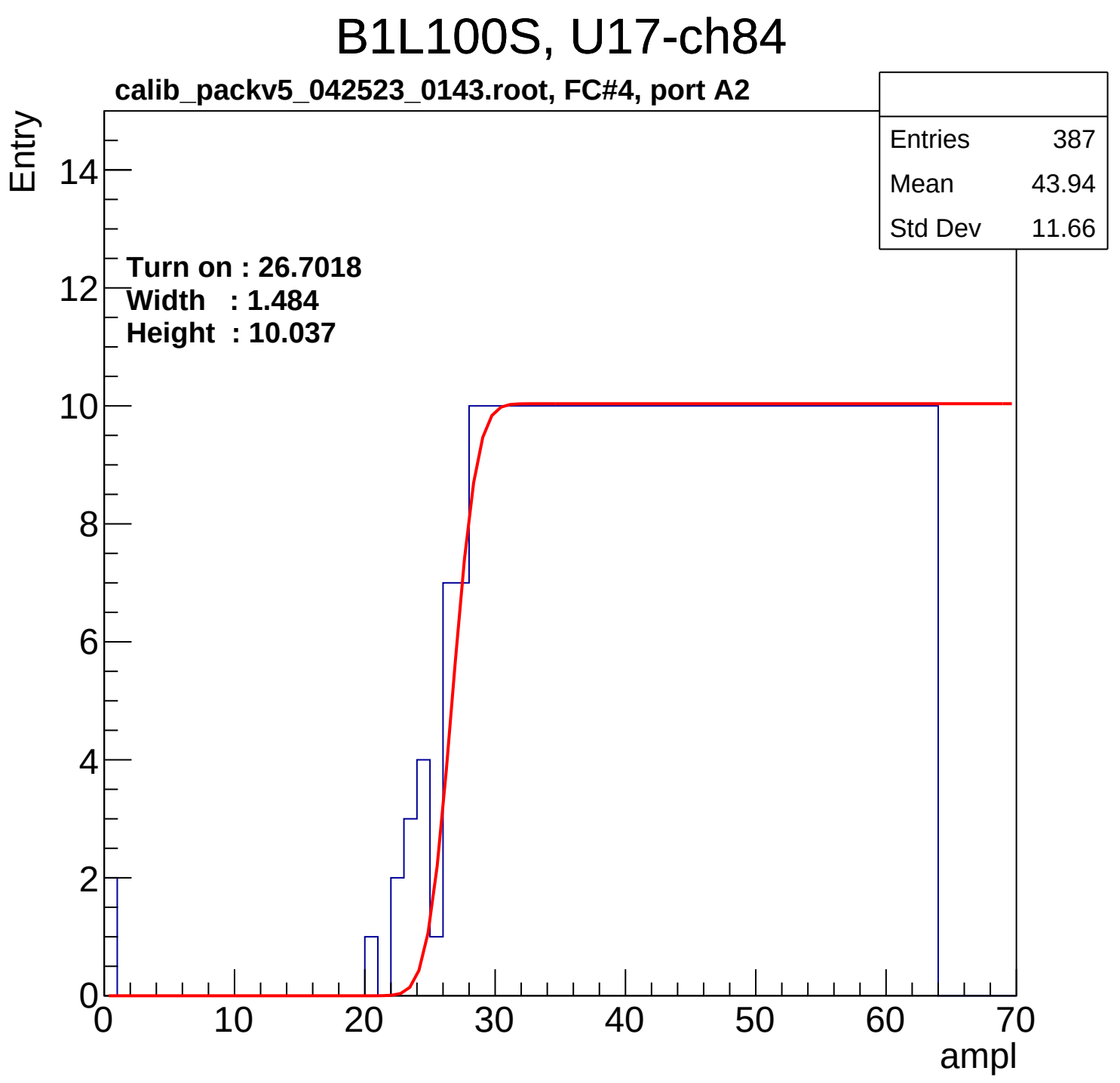
B1L100S, U17-ch84
calib_packv5_042523_0143.root, FC#4, port A2
Entries 387
Mean 43.94
Std Dev 11.66
Turn on : 26.7018
Width : 1.484
Height : 10.037
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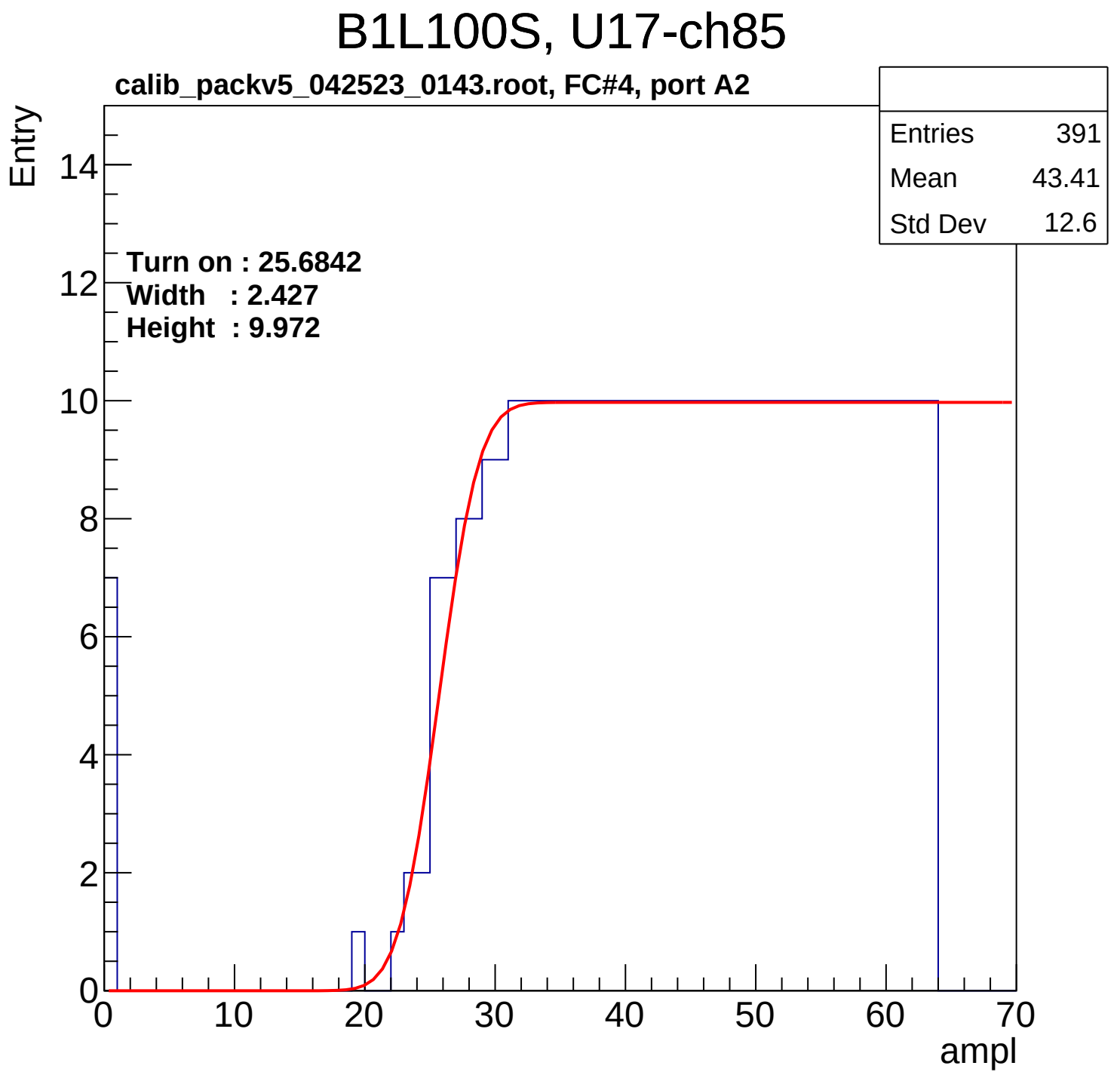
B1L100S, U17-ch85
calib_packv5_042523_0143.root, FC#4, port A2
Entries 391
Mean 43.41
Std Dev 12.6
Turn on : 25.6842
Width : 2.427
Height : 9.972
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ampl
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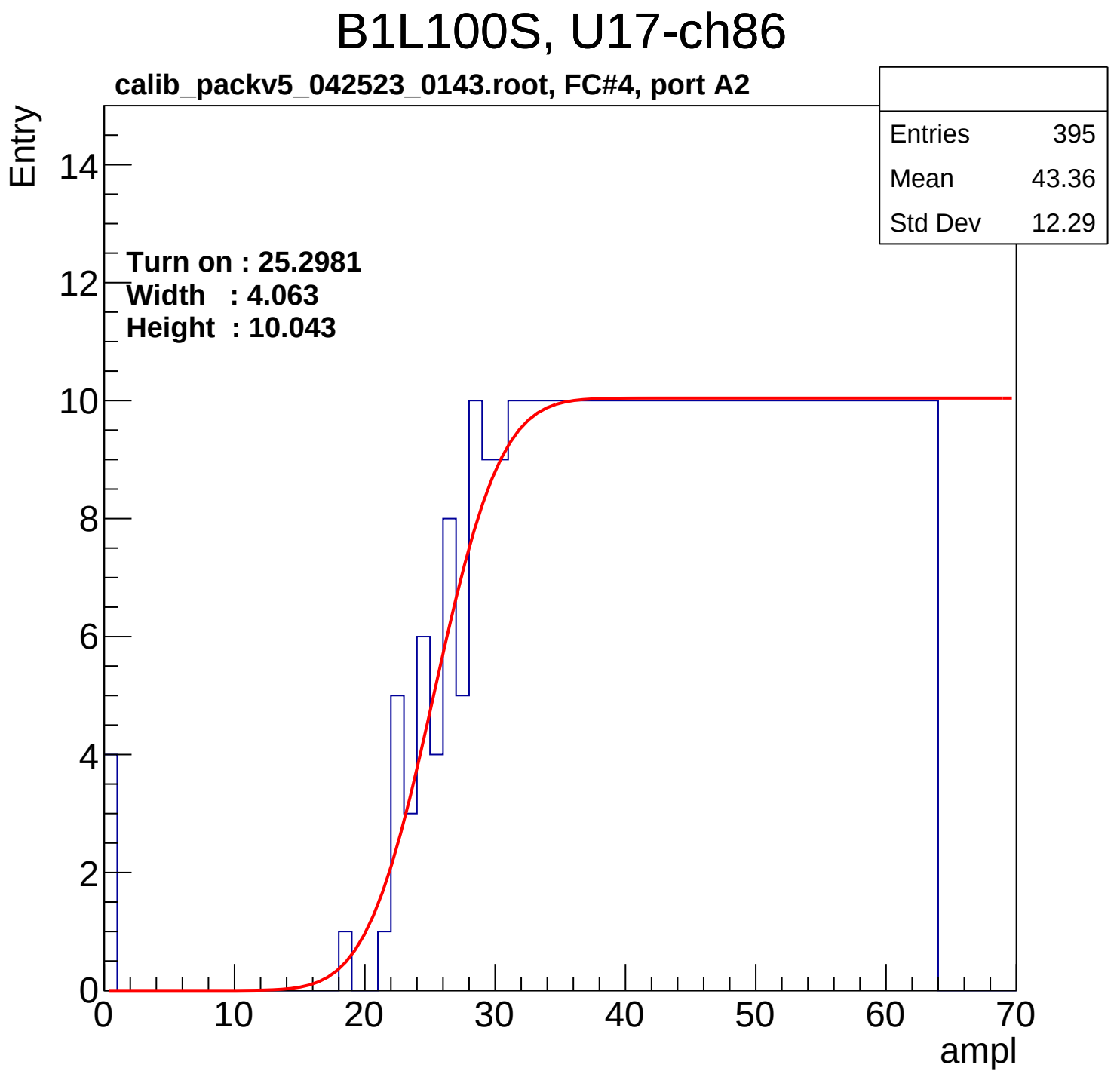
B1L100S, U17-ch86
calib_packv5_042523_0143.root, FC#4, port A2
Entries 395
Mean 43.36
Std Dev 12.29
Turn on : 25.2981
Width : 4.063
Height : 10.043
Entry
ampl
0
2
4
6
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20
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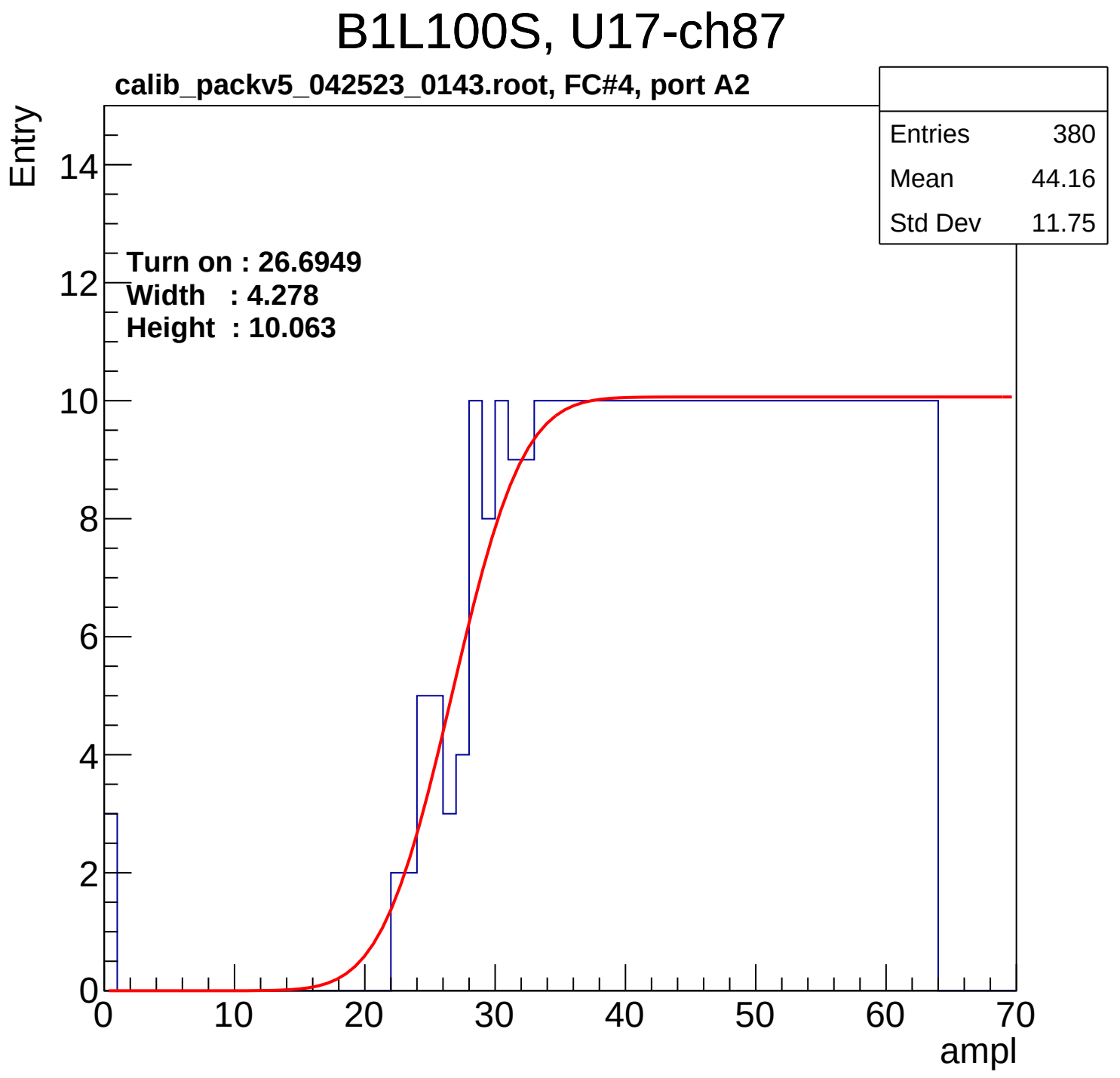
B1L100S, U17-ch87
calib_packv5_042523_0143.root, FC#4, port A2
Entries 380
Mean 44.16
Std Dev 11.75
Turn on : 26.6949
Width : 4.278
Height : 10.063
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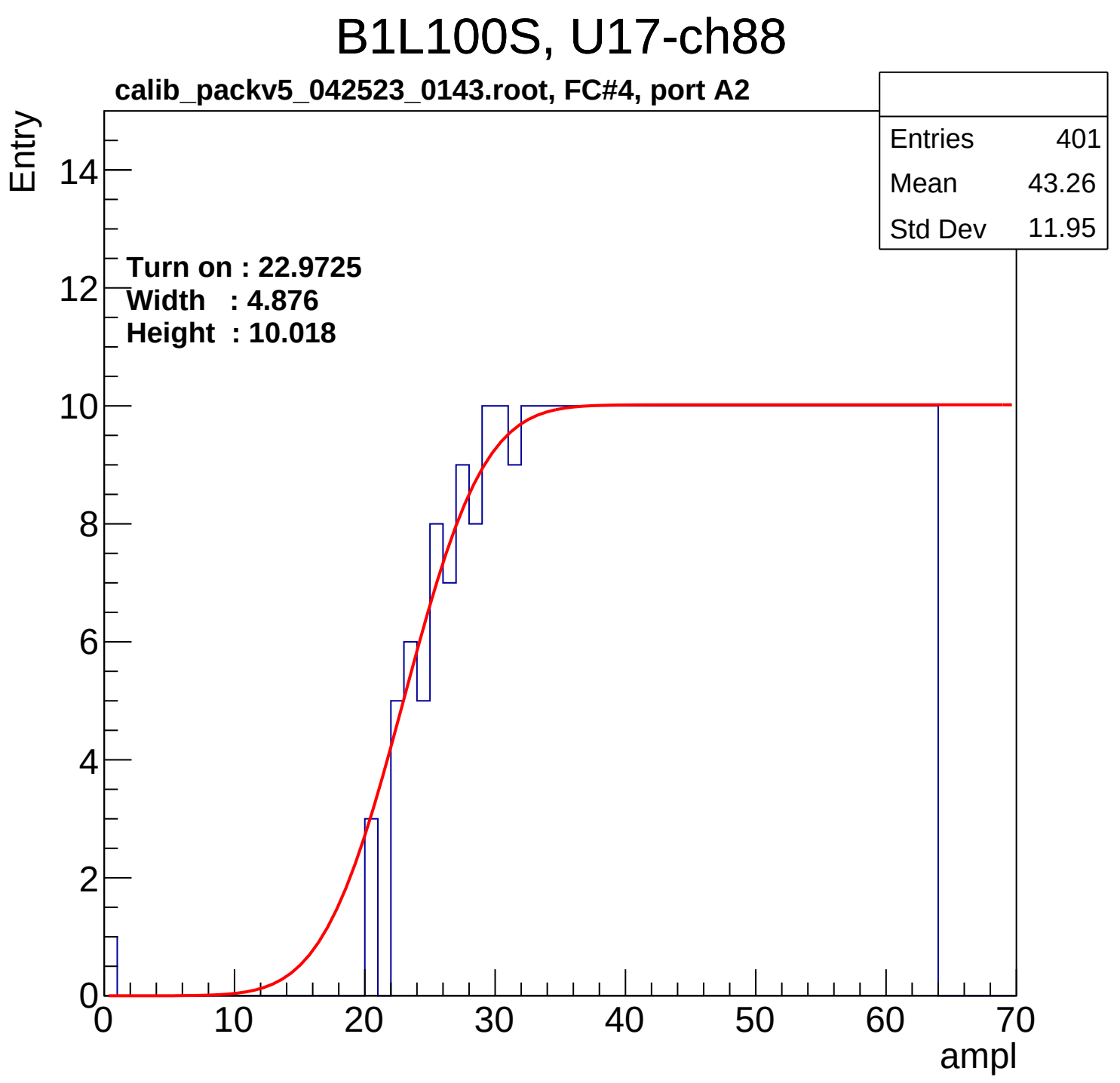
B1L100S, U17-ch88
calib_packv5_042523_0143.root, FC#4, port A2
Entries 401
Mean 43.26
Std Dev 11.95
Turn on : 22.9725
Width : 4.876
Height : 10.018
Entry
ampl
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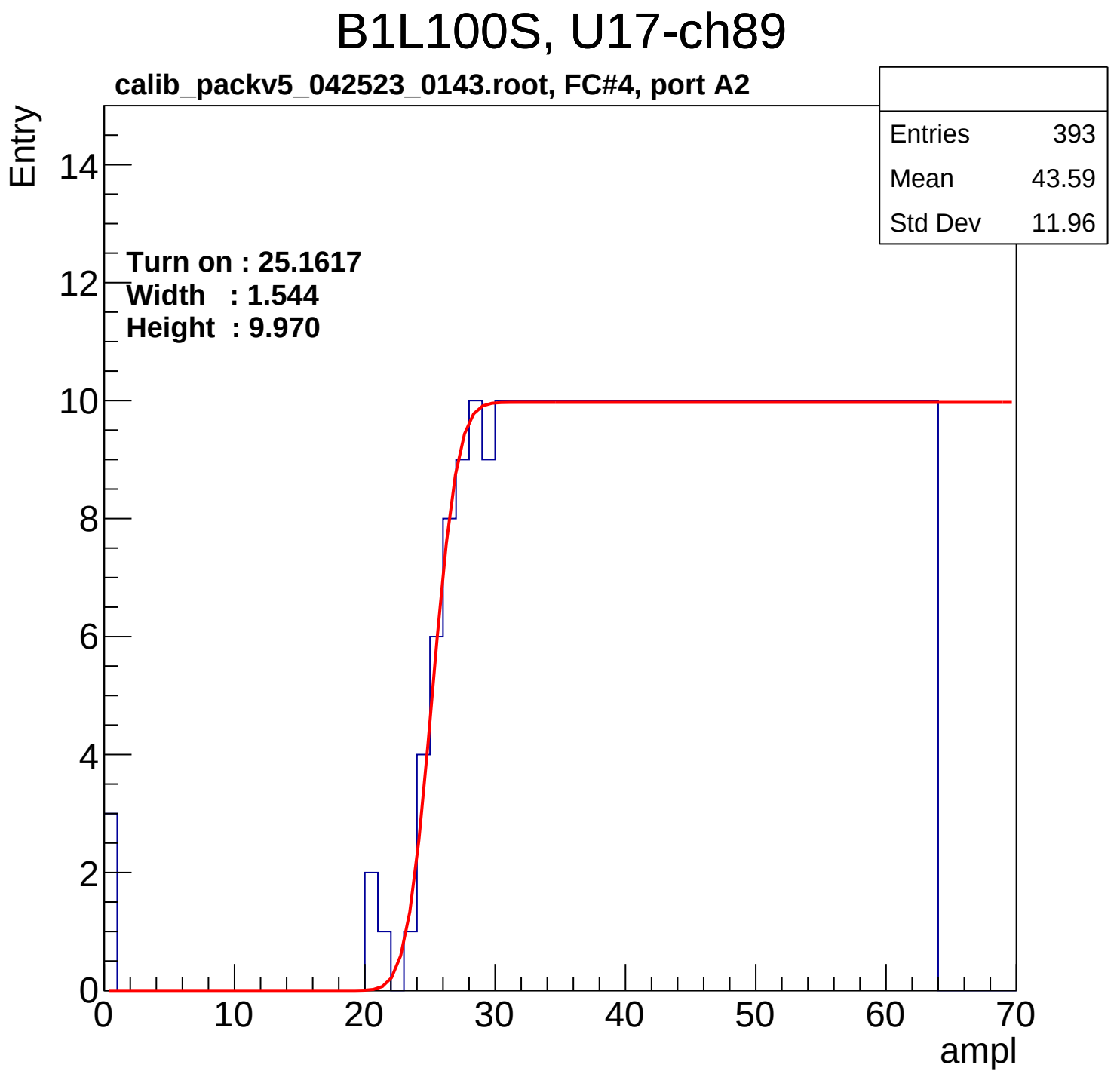
B1L100S, U17-ch89
calib_packv5_042523_0143.root, FC#4, port A2
Entries 393
Mean 43.59
Std Dev 11.96
Turn on : 25.1617
Width : 1.544
Height : 9.970
Entry
ampl
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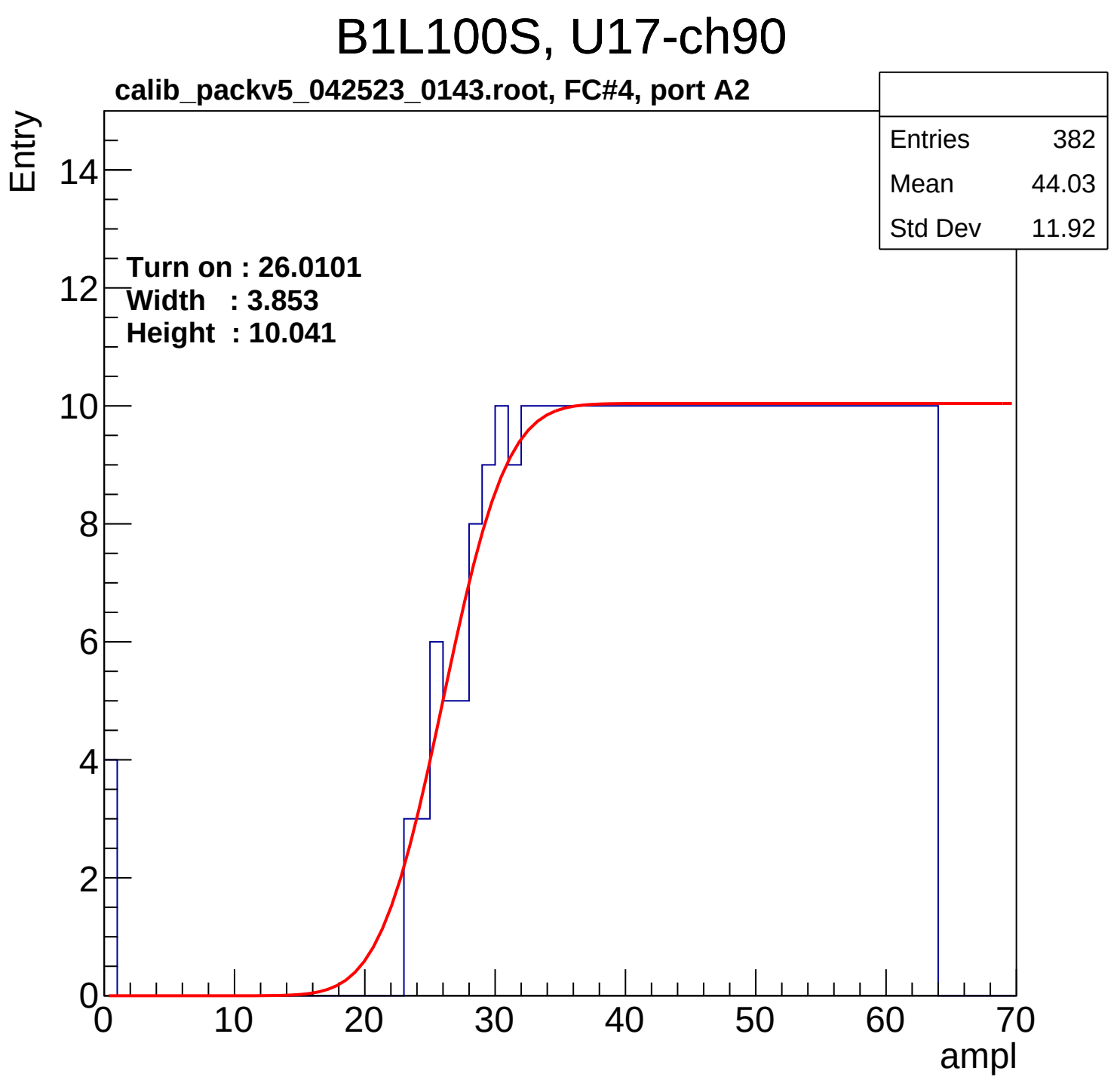
B1L100S, U17-ch90
calib_packv5_042523_0143.root, FC#4, port A2
Entries 382
Mean 44.03
Std Dev 11.92
Turn on : 26.0101
Width : 3.853
Height : 10.041
Entry
ampl
0
2
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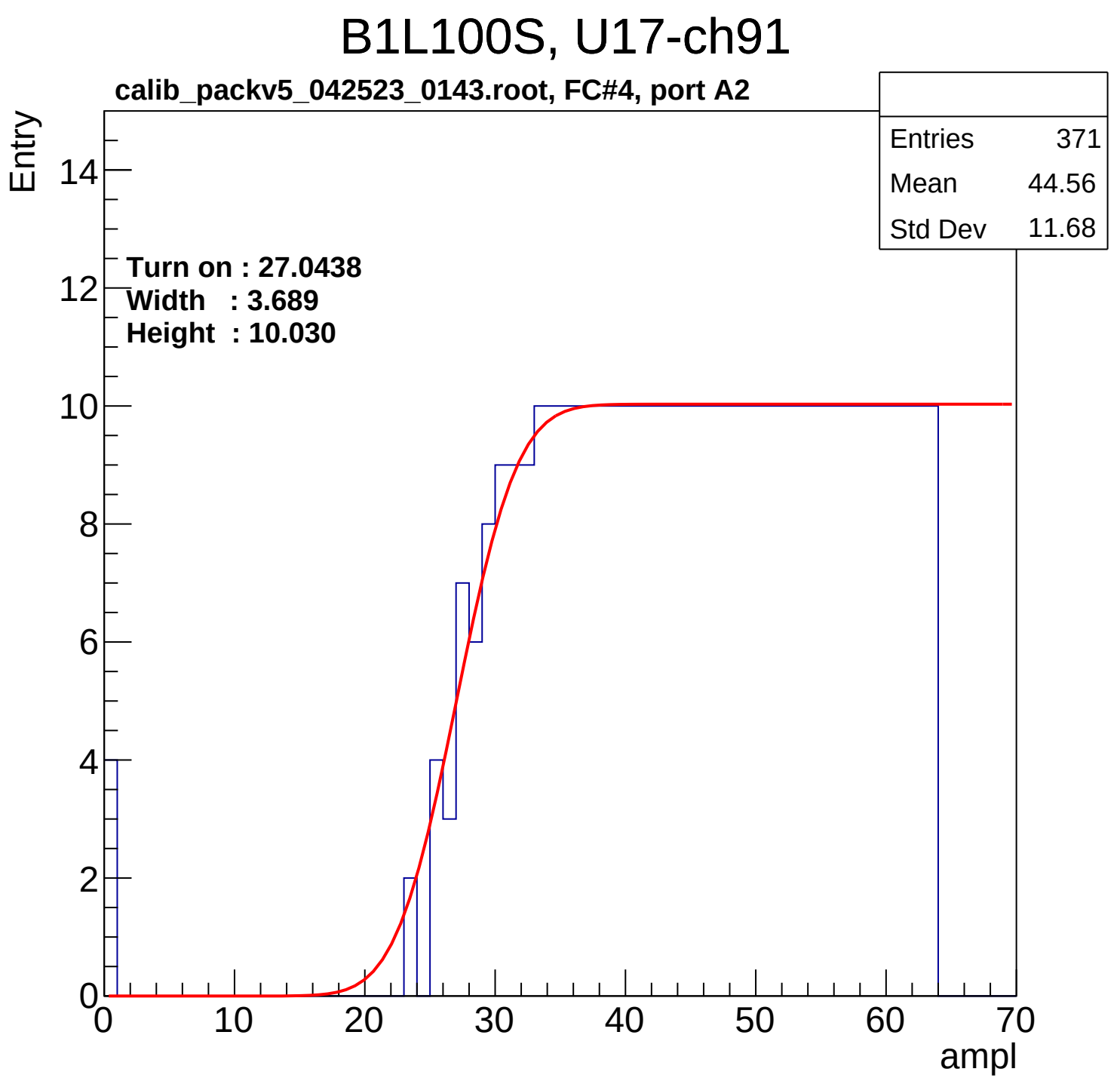
B1L100S, U17-ch91
calib_packv5_042523_0143.root, FC#4, port A2
Entries 371
Mean 44.56
Std Dev 11.68
Turn on : 27.0438
Width : 3.689
Height : 10.030
Entry
ampl
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6
8
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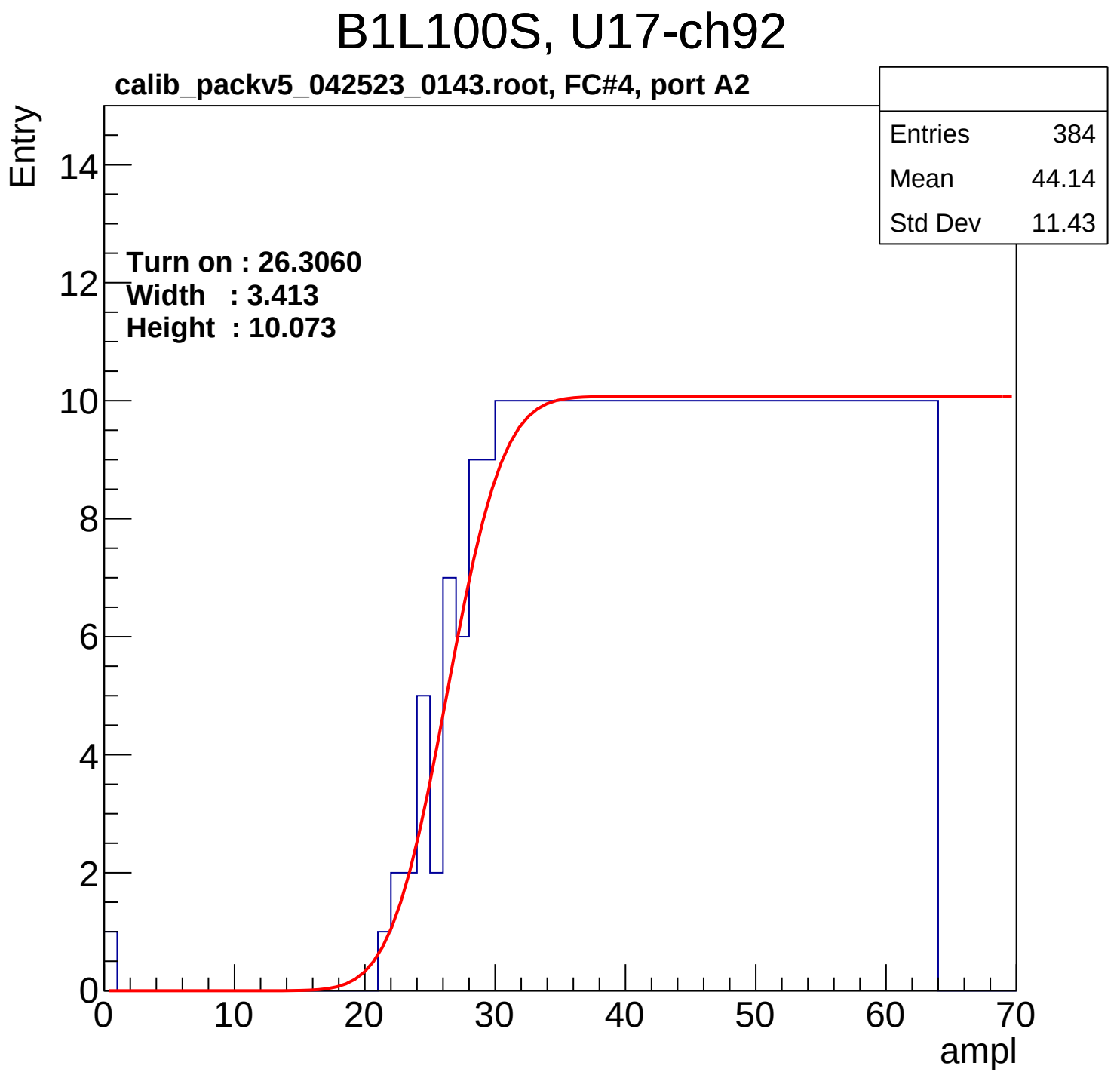
B1L100S, U17-ch92
calib_packv5_042523_0143.root, FC#4, port A2
Entries 384
Mean 44.14
Std Dev 11.43
Turn on : 26.3060
Width : 3.413
Height : 10.073
Entry
ampl
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2
4
6
8
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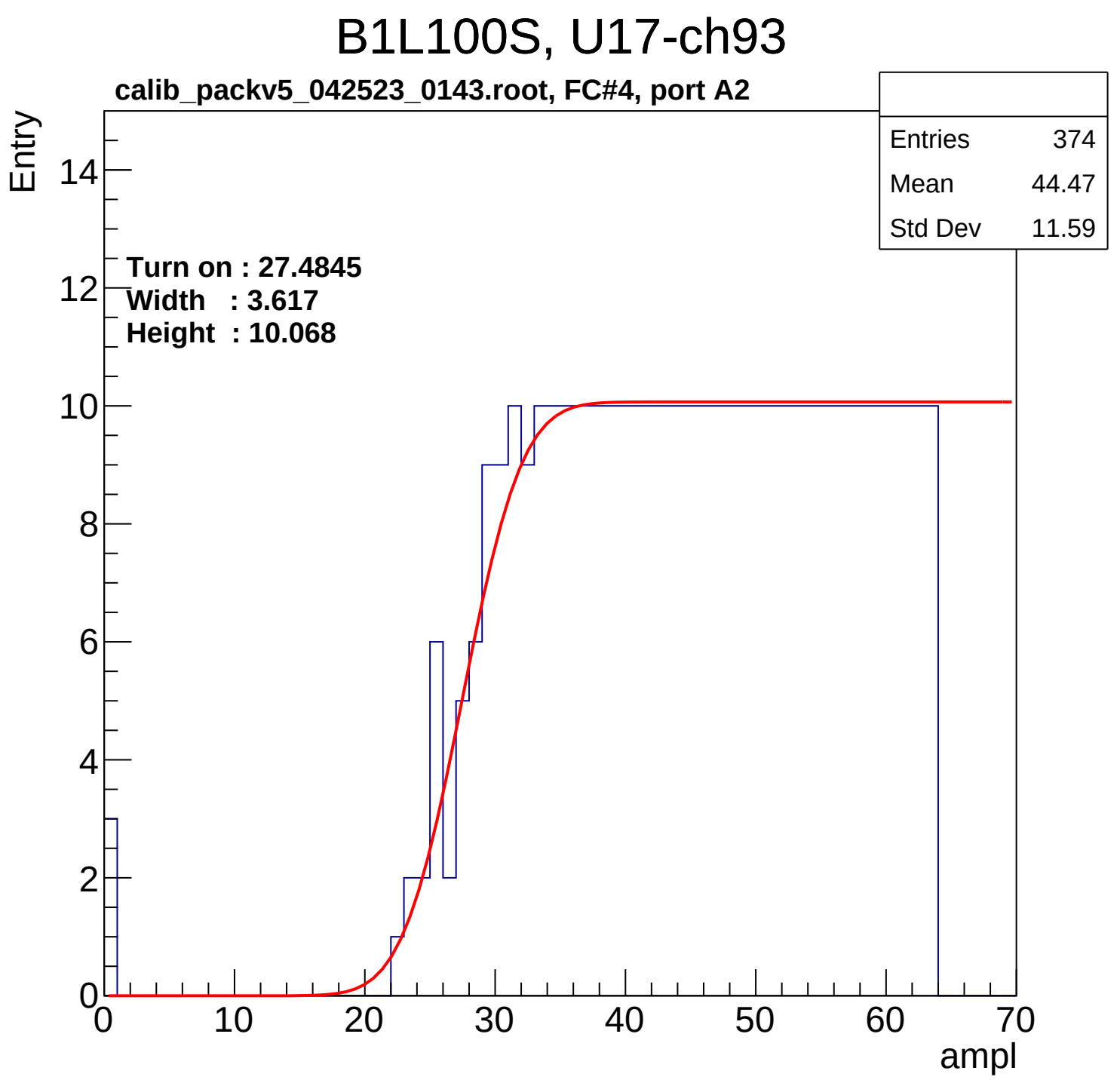
B1L100S, U17-ch93
calib_packv5_042523_0143.root, FC#4, port A2
Entries 374
Mean 44.47
Std Dev 11.59
Turn on : 27.4845
Width : 3.617
Height : 10.068
Entry
ampl
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6
8
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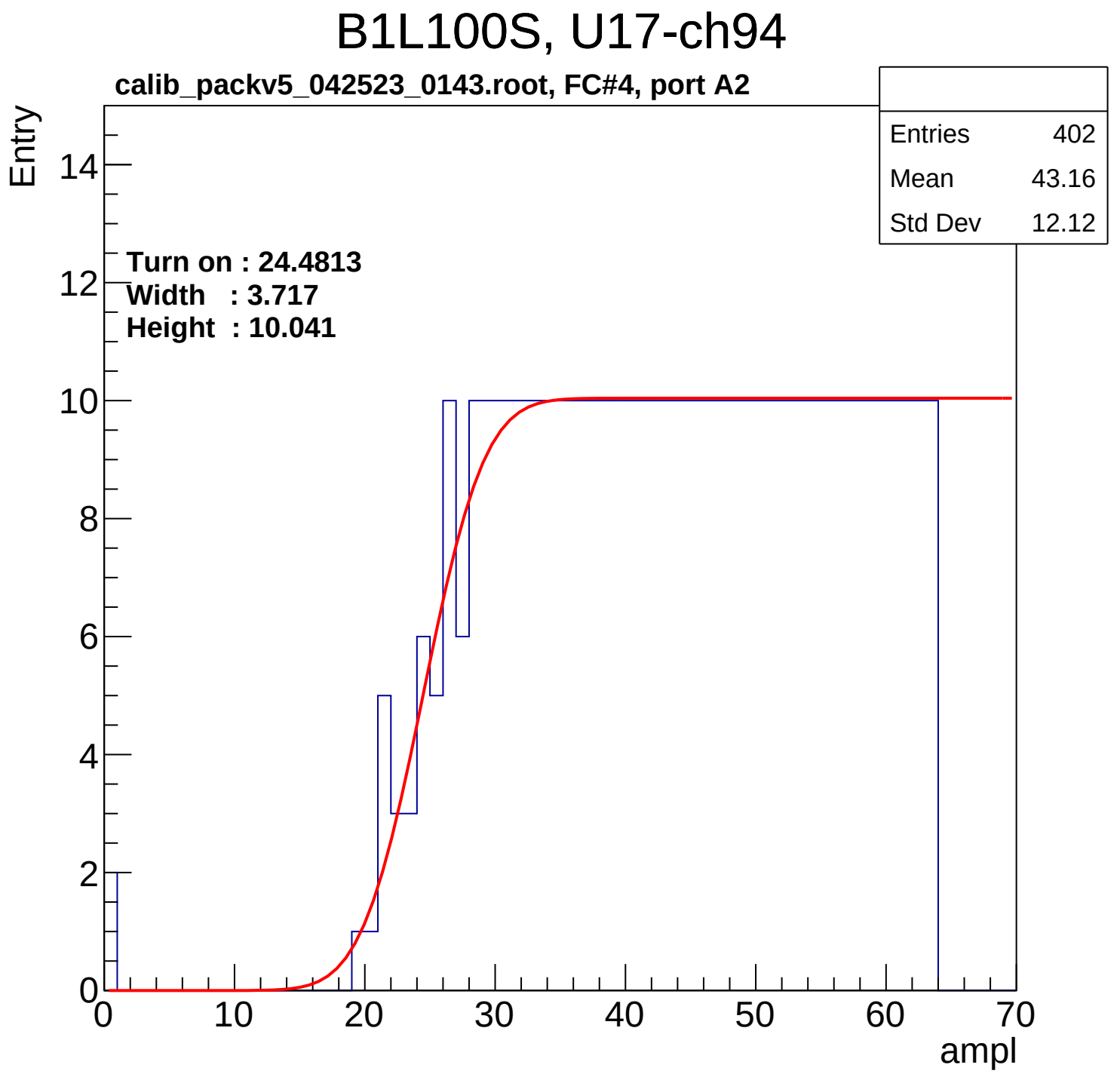
B1L100S, U17-ch94
calib_packv5_042523_0143.root, FC#4, port A2
Entries 402
Mean 43.16
Std Dev 12.12
Turn on : 24.4813
Width : 3.717
Height : 10.041
Entry
ampl
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2
4
6
8
10
12
14
0
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20
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60
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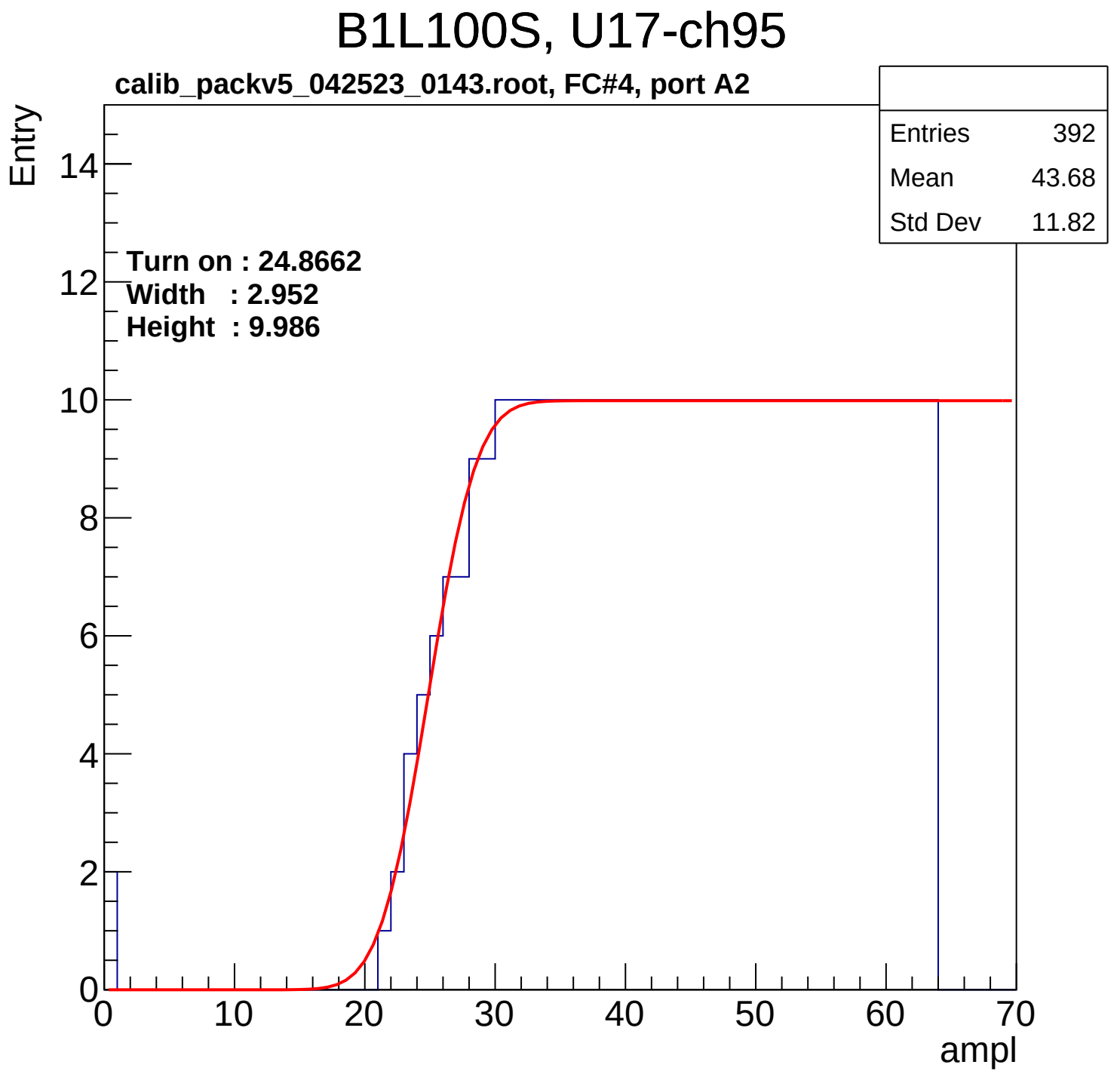
B1L100S, U17-ch95
calib_packv5_042523_0143.root, FC#4, port A2
Entries 392
Mean 43.68
Std Dev 11.82
Turn on : 24.8662
Width : 2.952
Height : 9.986
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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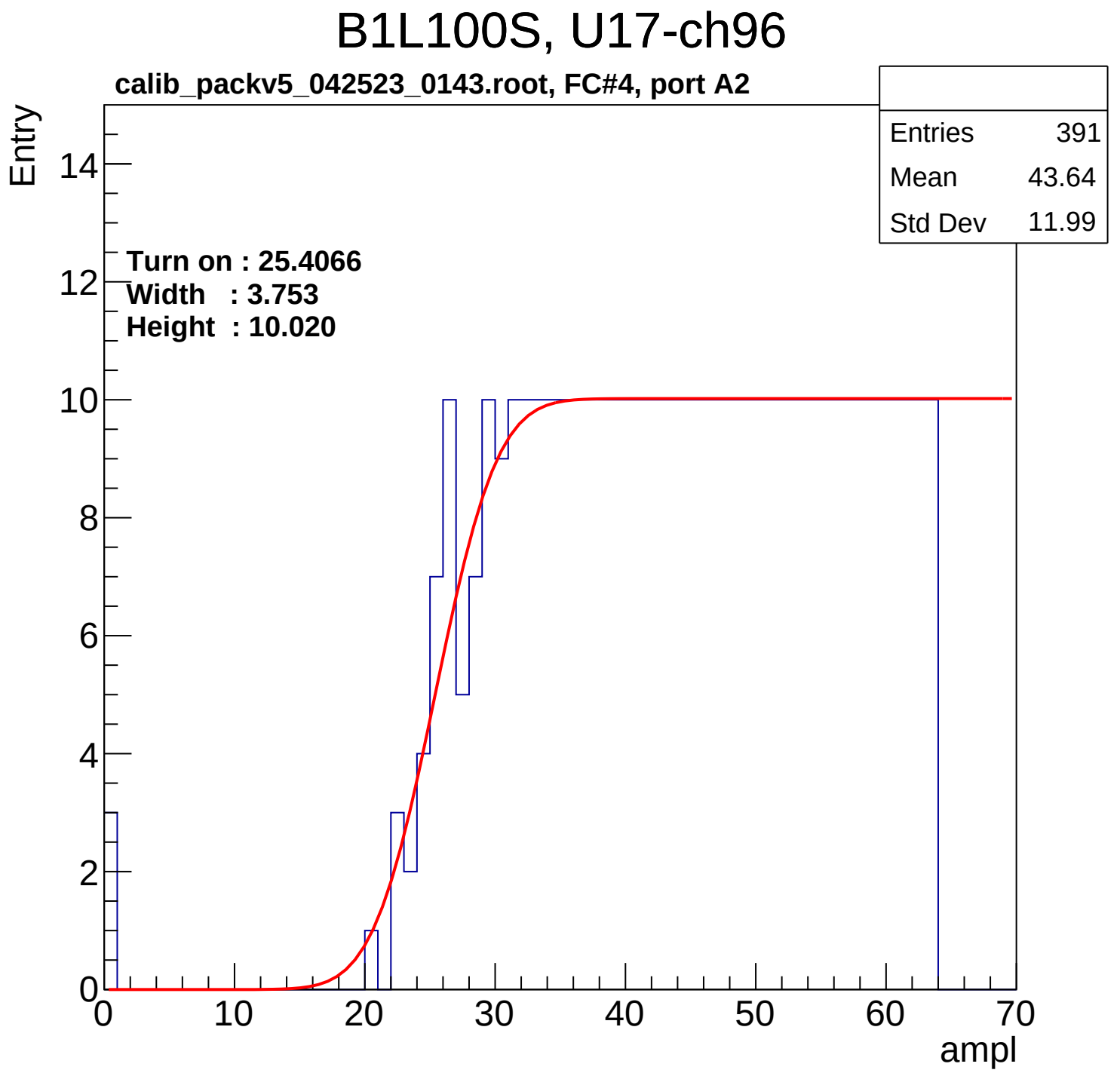
B1L100S, U17-ch96
calib_packv5_042523_0143.root, FC#4, port A2
Entries 391
Mean 43.64
Std Dev 11.99
Turn on : 25.4066
Width : 3.753
Height : 10.020
Entry
ampl
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2
4
6
8
10
12
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0
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60
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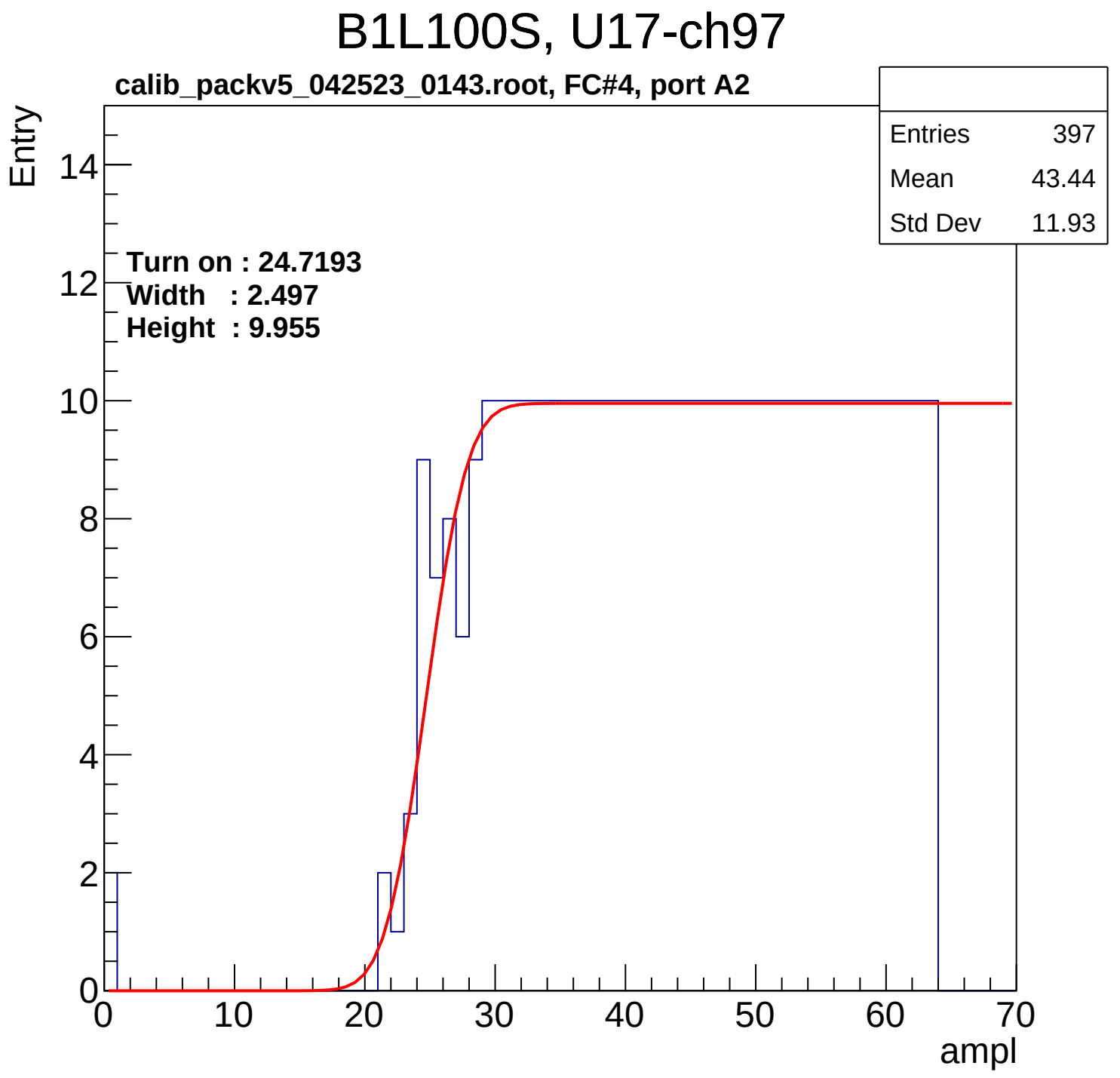
B1L100S, U17-ch97
calib_packv5_042523_0143.root, FC#4, port A2
Entries 397
Mean 43.44
Std Dev 11.93
Turn on : 24.7193
Width : 2.497
Height : 9.955
Entry
ampl
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2
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6
8
10
12
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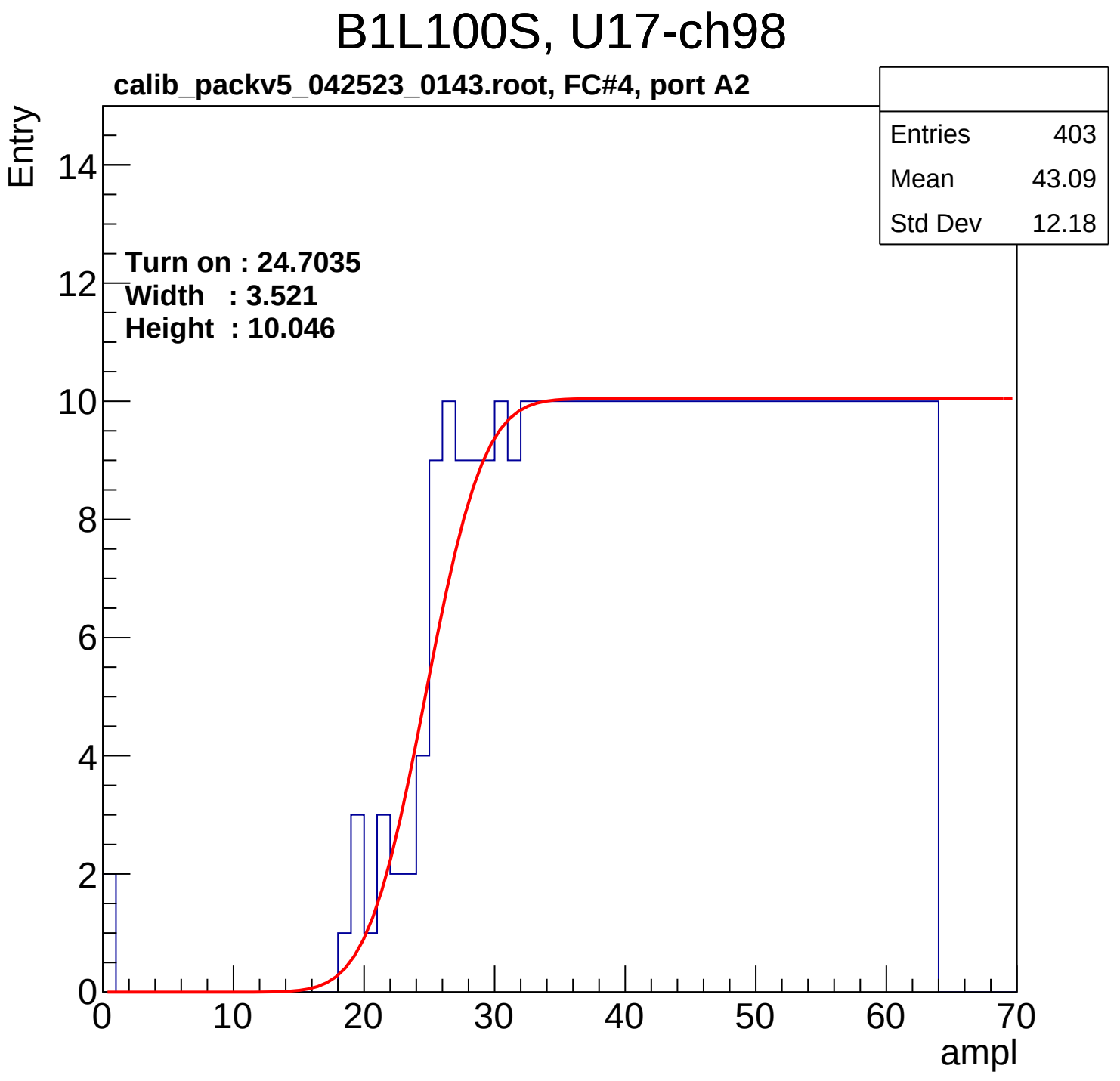
B1L100S, U17-ch98
calib_packv5_042523_0143.root, FC#4, port A2
Entries 403
Mean 43.09
Std Dev 12.18
Turn on : 24.7035
Width : 3.521
Height : 10.046
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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60
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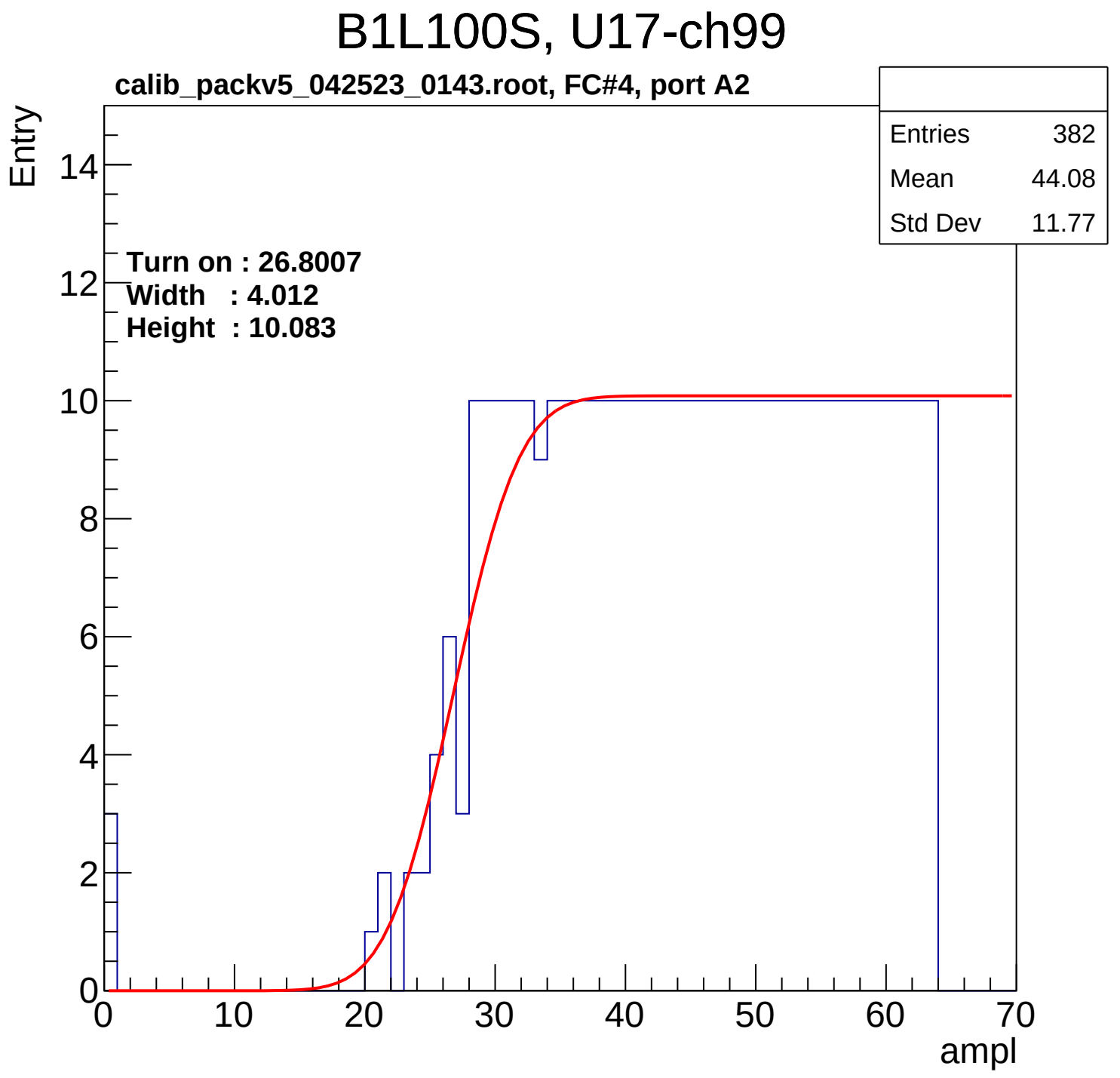
B1L100S, U17-ch99
calib_packv5_042523_0143.root, FC#4, port A2
Entries 382
Mean 44.08
Std Dev 11.77
Turn on : 26.8007
Width : 4.012
Height : 10.083
Entry
ampl
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2
4
6
8
10
12
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0
10
20
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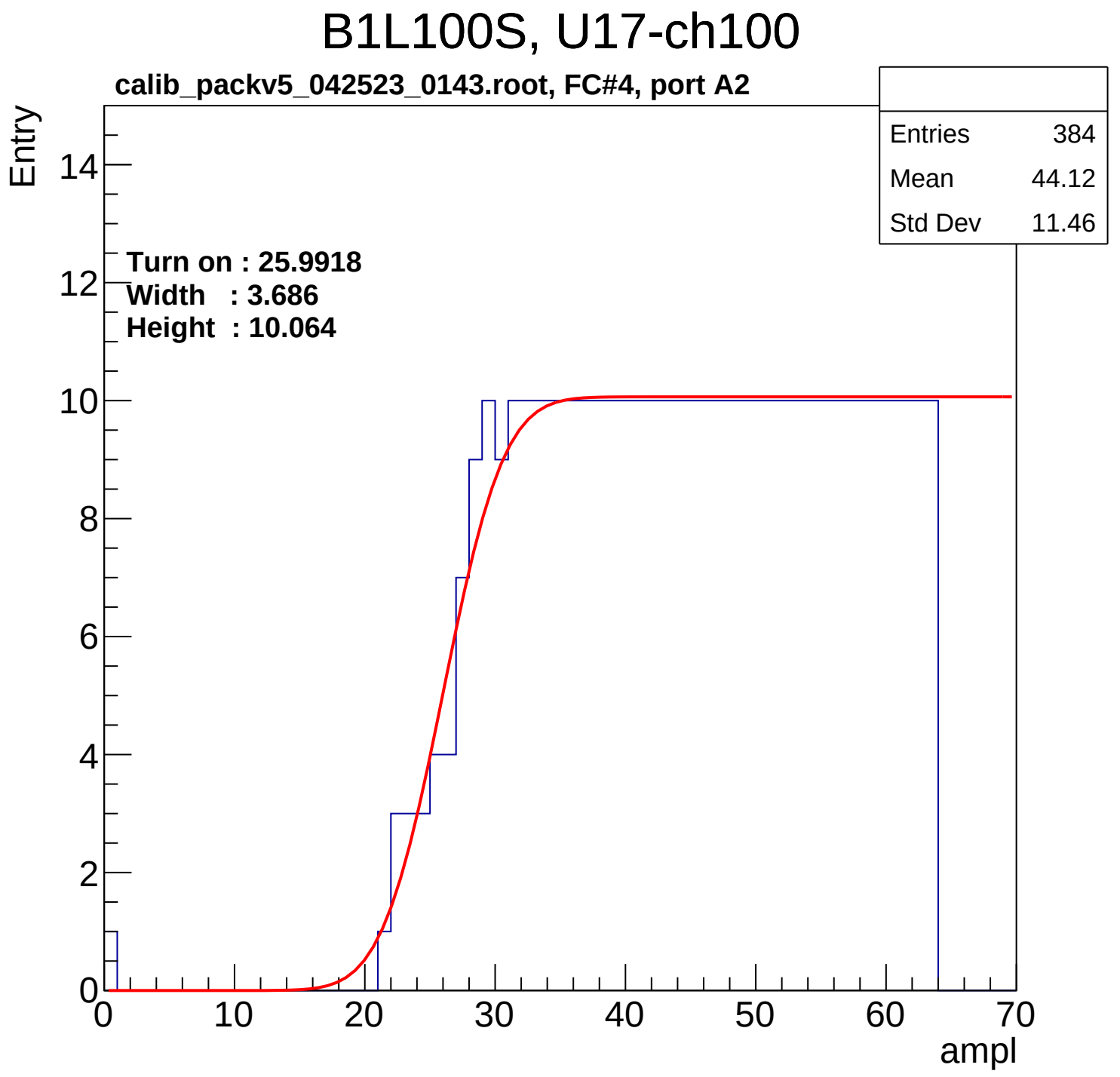
B1L100S, U17-ch100
calib_packv5_042523_0143.root, FC#4, port A2
Entries 384
Mean 44.12
Std Dev 11.46
Turn on : 25.9918
Width : 3.686
Height : 10.064
Entry
ampl
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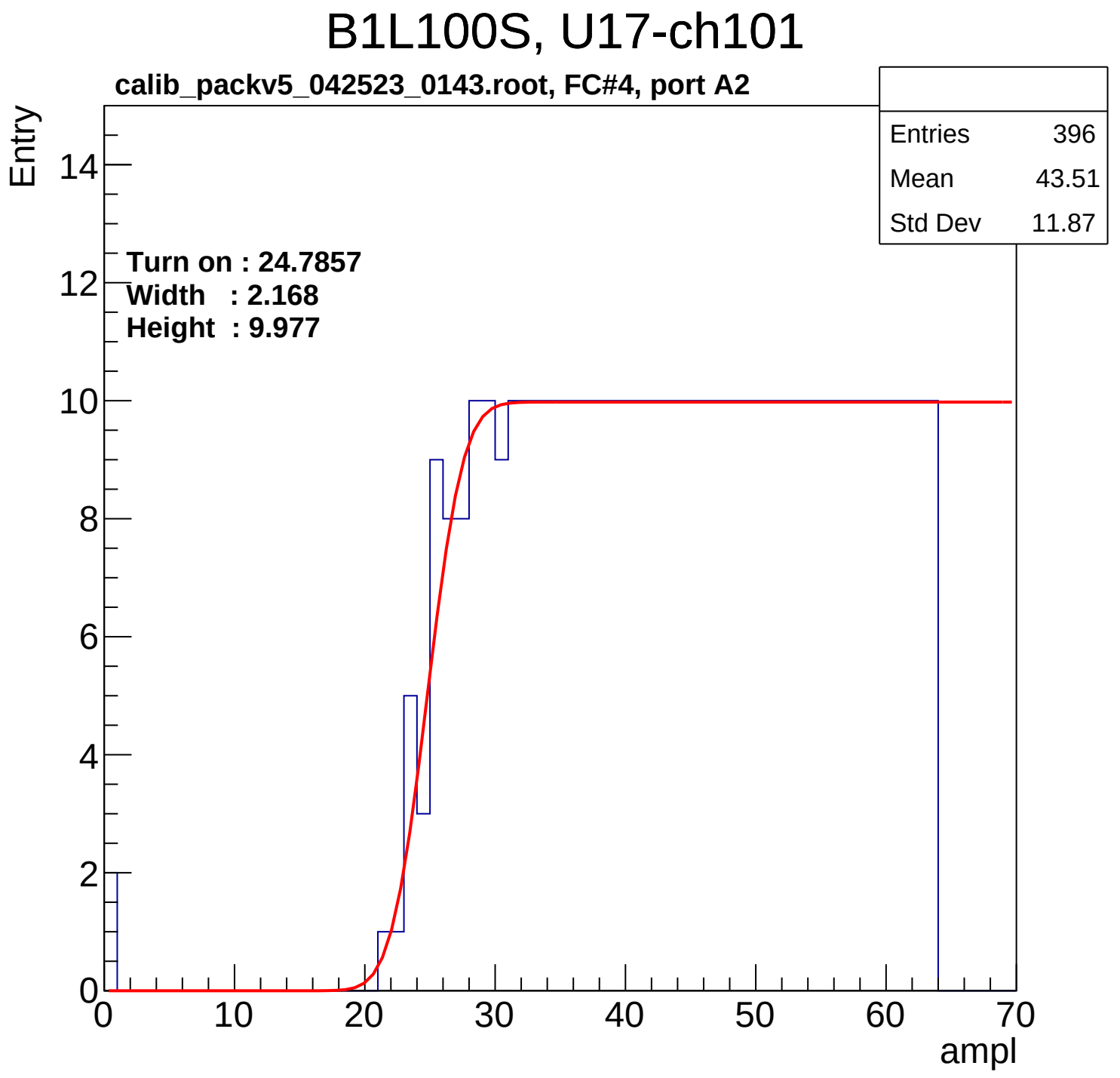
B1L100S, U17-ch101
calib_packv5_042523_0143.root, FC#4, port A2
Entries 396
Mean 43.51
Std Dev 11.87
Turn on : 24.7857
Width : 2.168
Height : 9.977
Entry
ampl
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4
6
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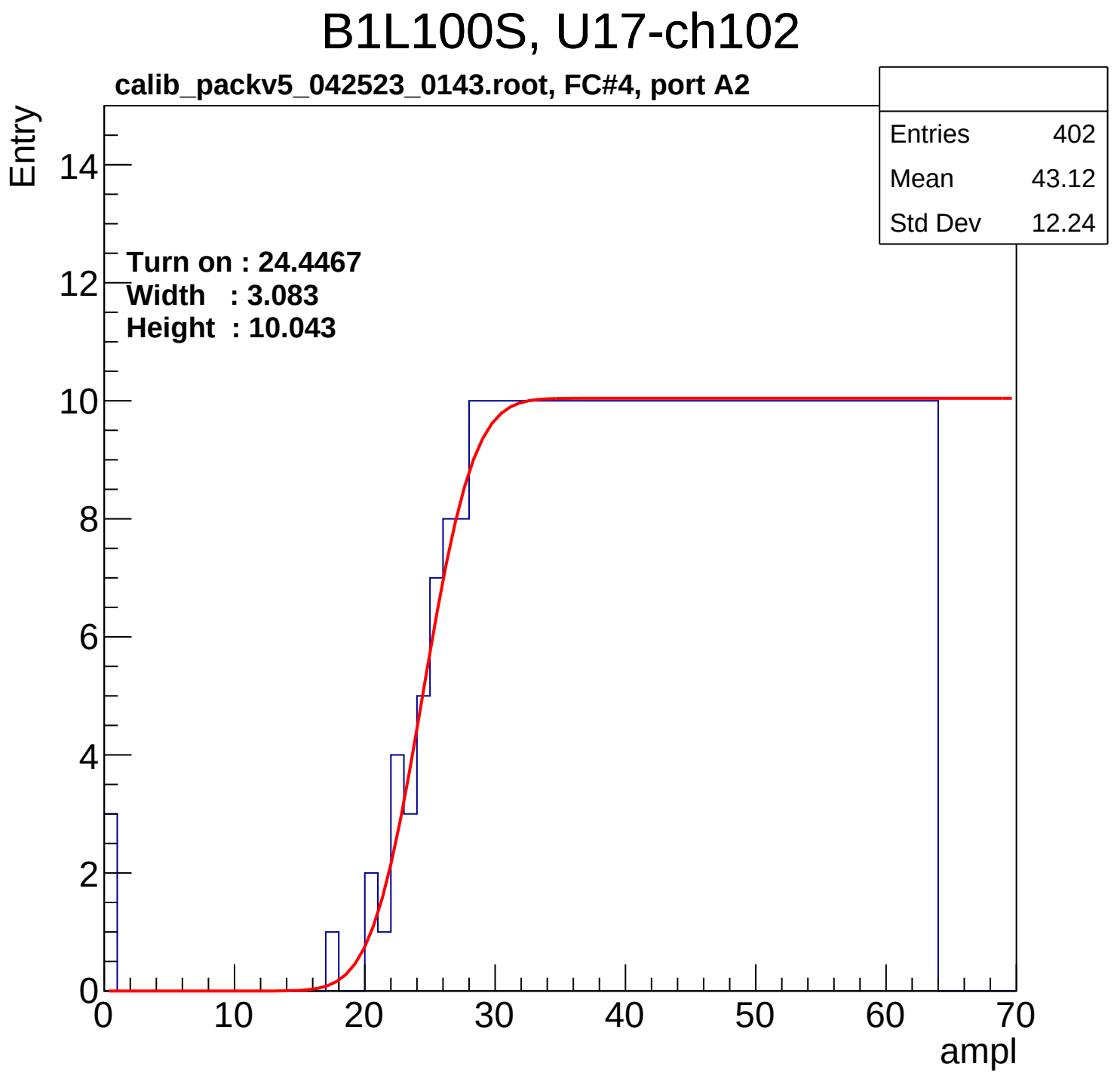
B1L100S, U17-ch102
calib_packv5_042523_0143.root, FC#4, port A2
Entries 402
Mean 43.12
Std Dev 12.24
Turn on : 24.4467
Width : 3.083
Height : 10.043
Entry
ampl
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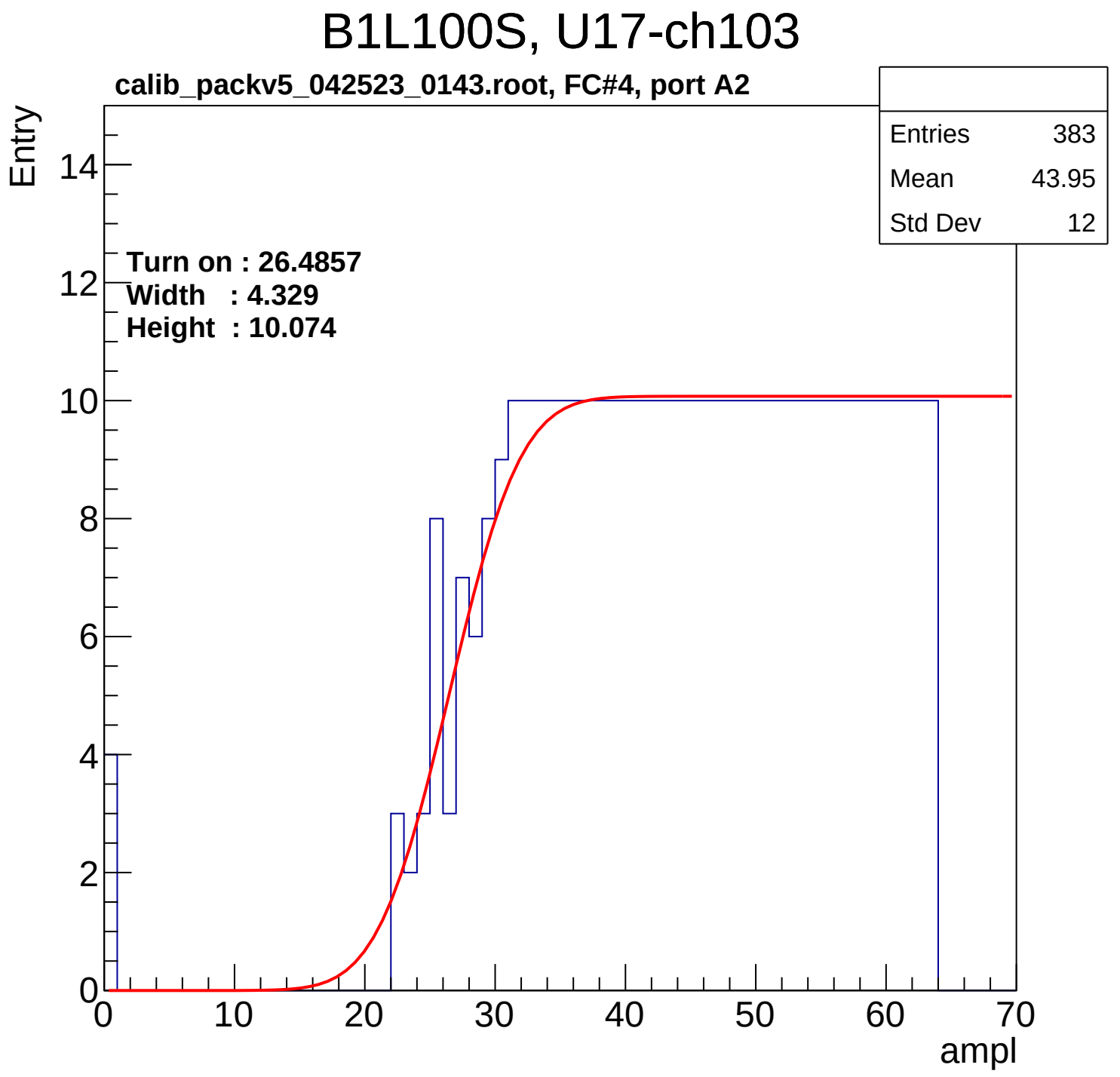
B1L100S, U17-ch103
calib_packv5_042523_0143.root, FC#4, port A2
Entries 383
Mean 43.95
Std Dev 12
Turn on : 26.4857
Width : 4.329
Height : 10.074
Entry
ampl
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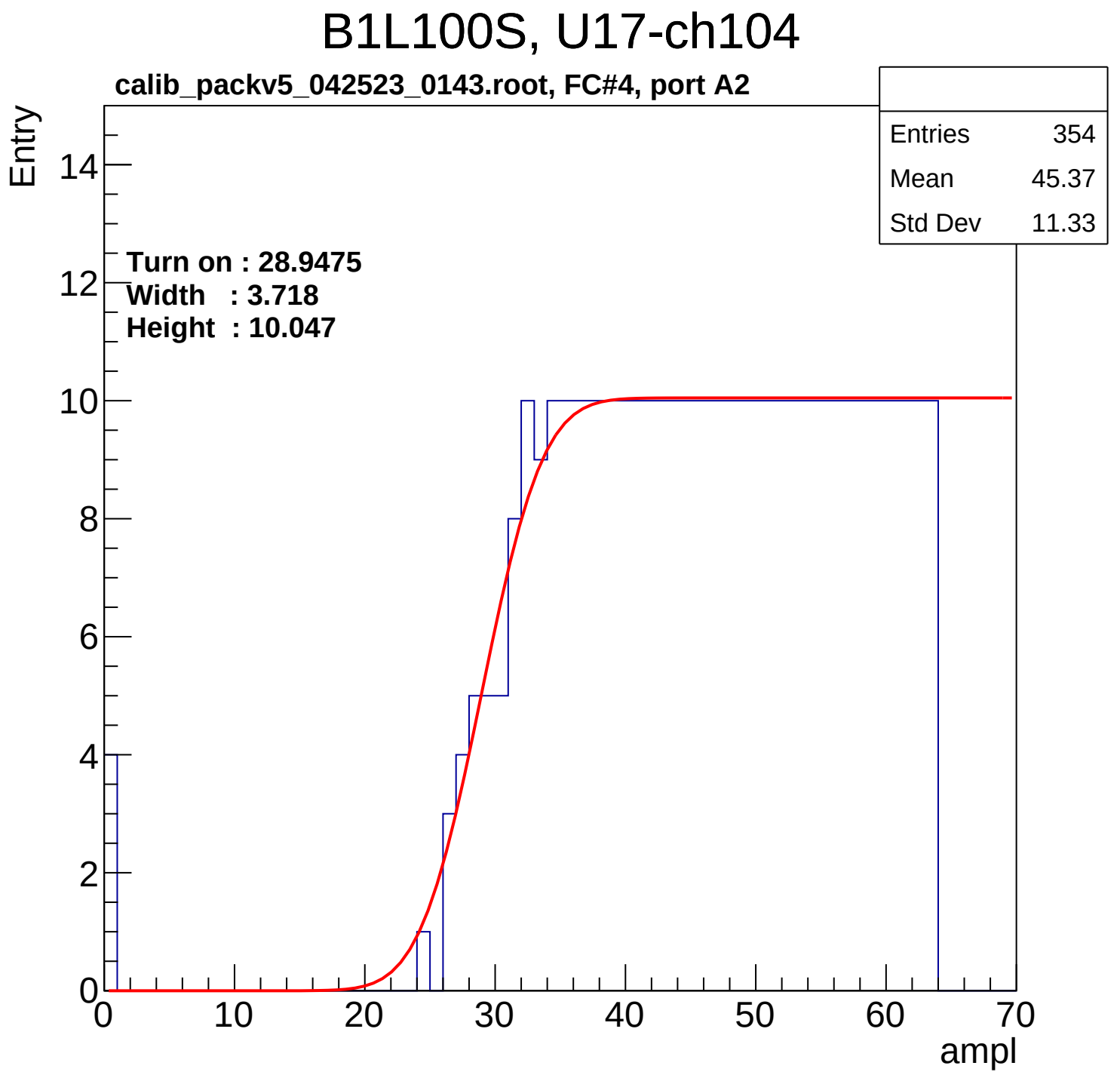
B1L100S, U17-ch104
calib_packv5_042523_0143.root, FC#4, port A2
Entries 354
Mean 45.37
Std Dev 11.33
Turn on : 28.9475
Width : 3.718
Height : 10.047
Entry
ampl
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2
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6
8
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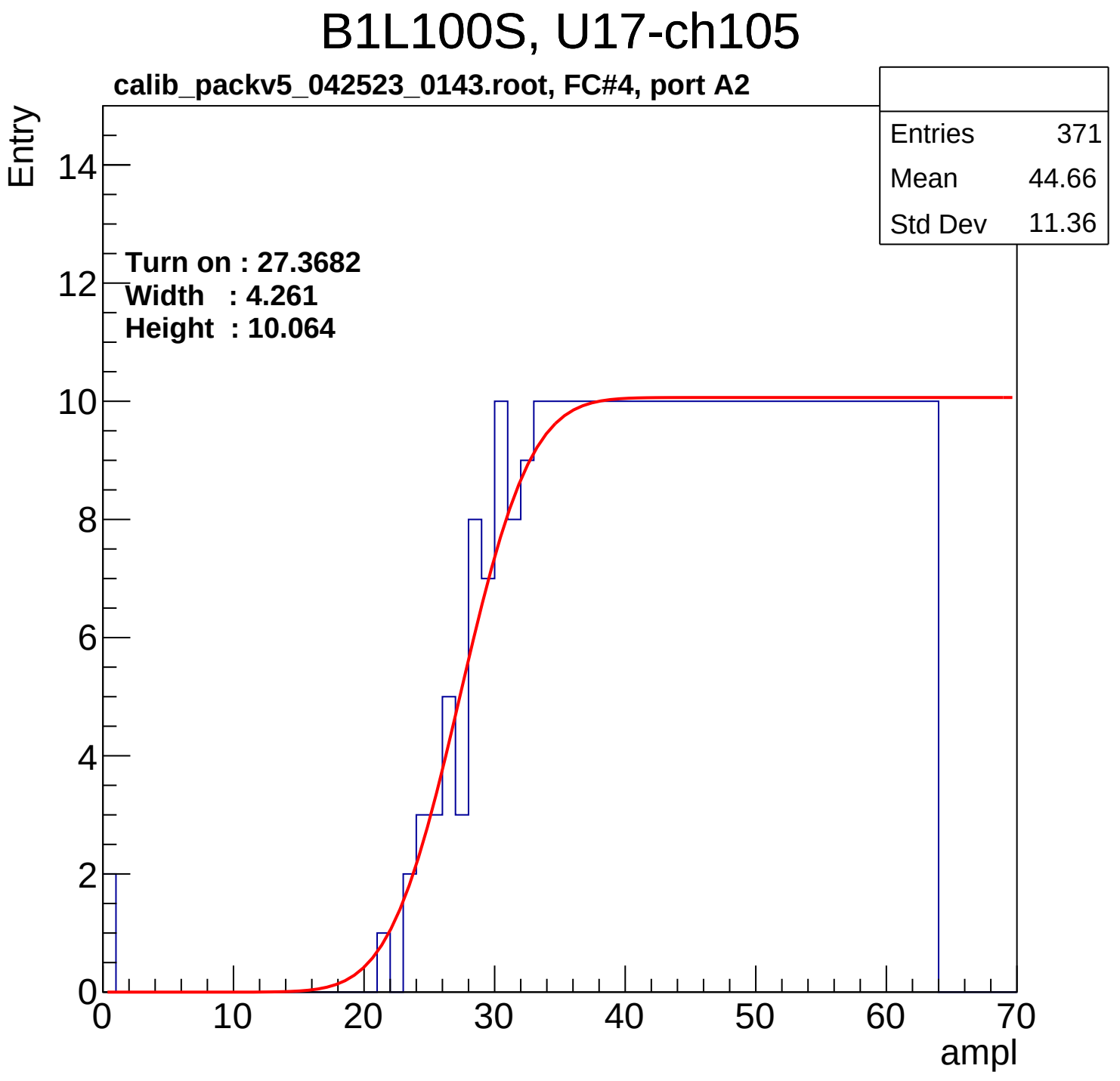
B1L100S, U17-ch105
calib_packv5_042523_0143.root, FC#4, port A2
Entries 371
Mean 44.66
Std Dev 11.36
Turn on : 27.3682
Width : 4.261
Height : 10.064
Entry
ampl
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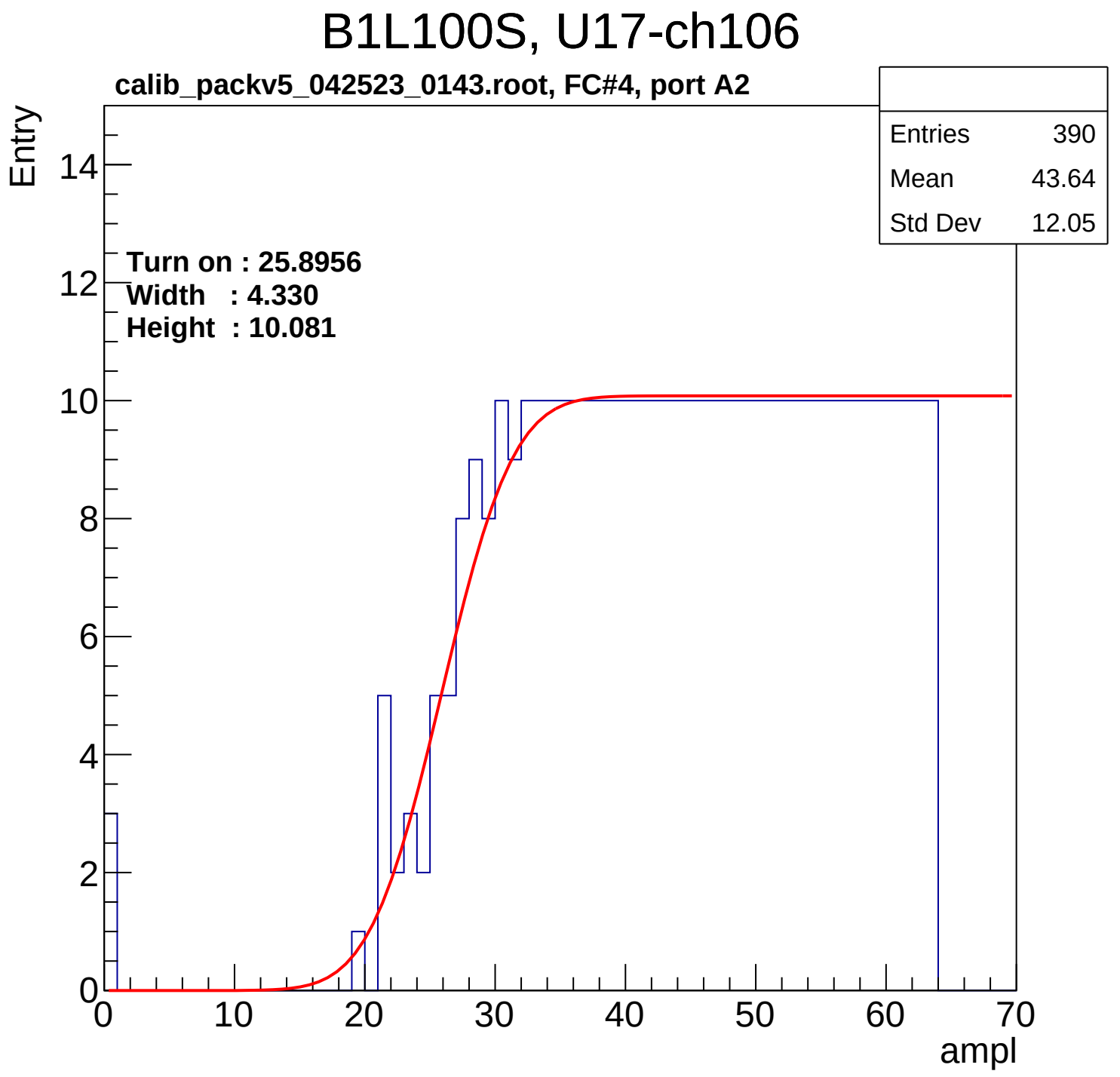
B1L100S, U17-ch106
calib_packv5_042523_0143.root, FC#4, port A2
Entries 390
Mean 43.64
Std Dev 12.05
Turn on : 25.8956
Width : 4.330
Height : 10.081
Entry
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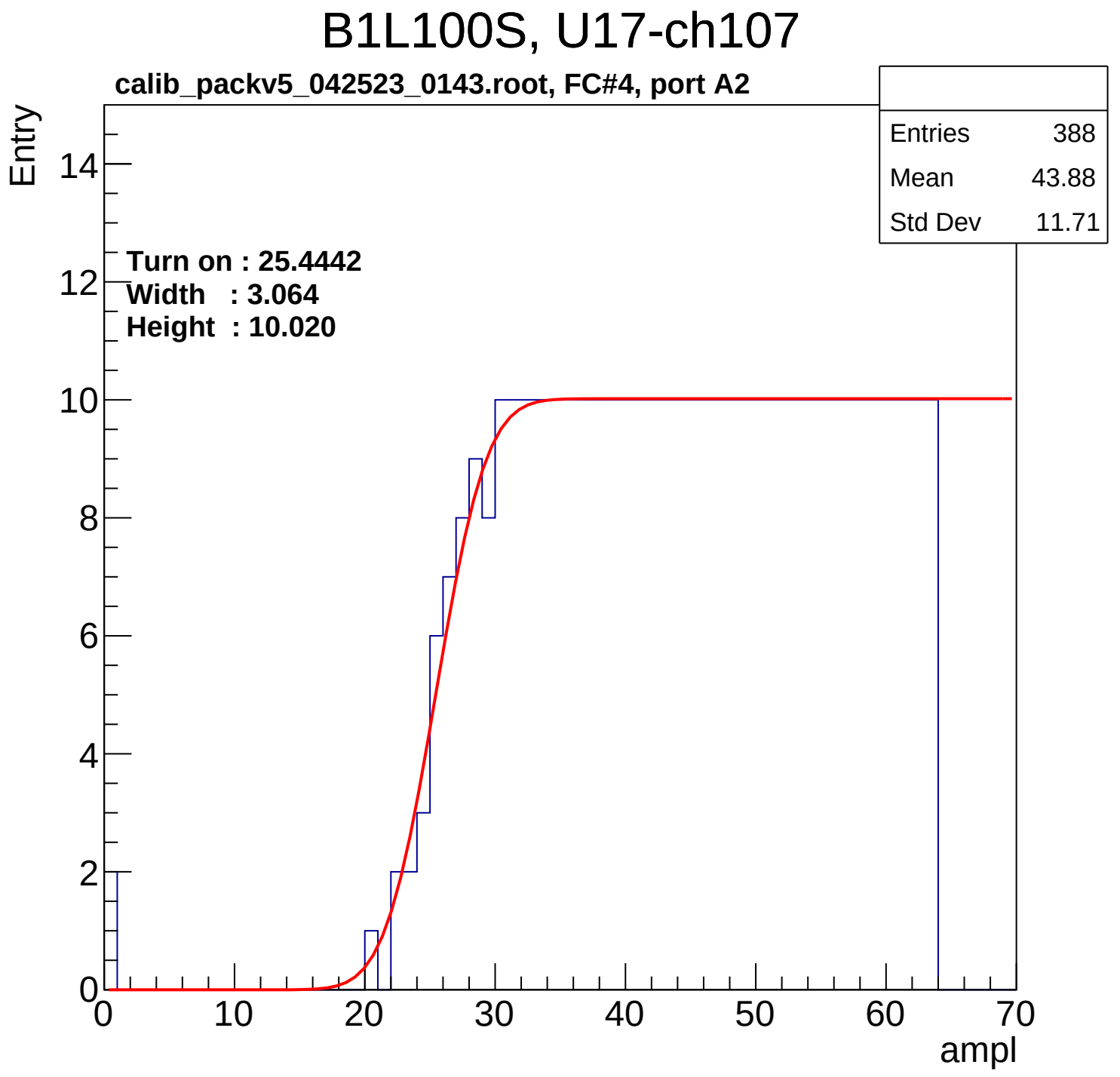
B1L100S, U17-ch107
calib_packv5_042523_0143.root, FC#4, port A2
Entries 388
Mean 43.88
Std Dev 11.71
Turn on : 25.4442
Width : 3.064
Height : 10.020
Entry
ampl
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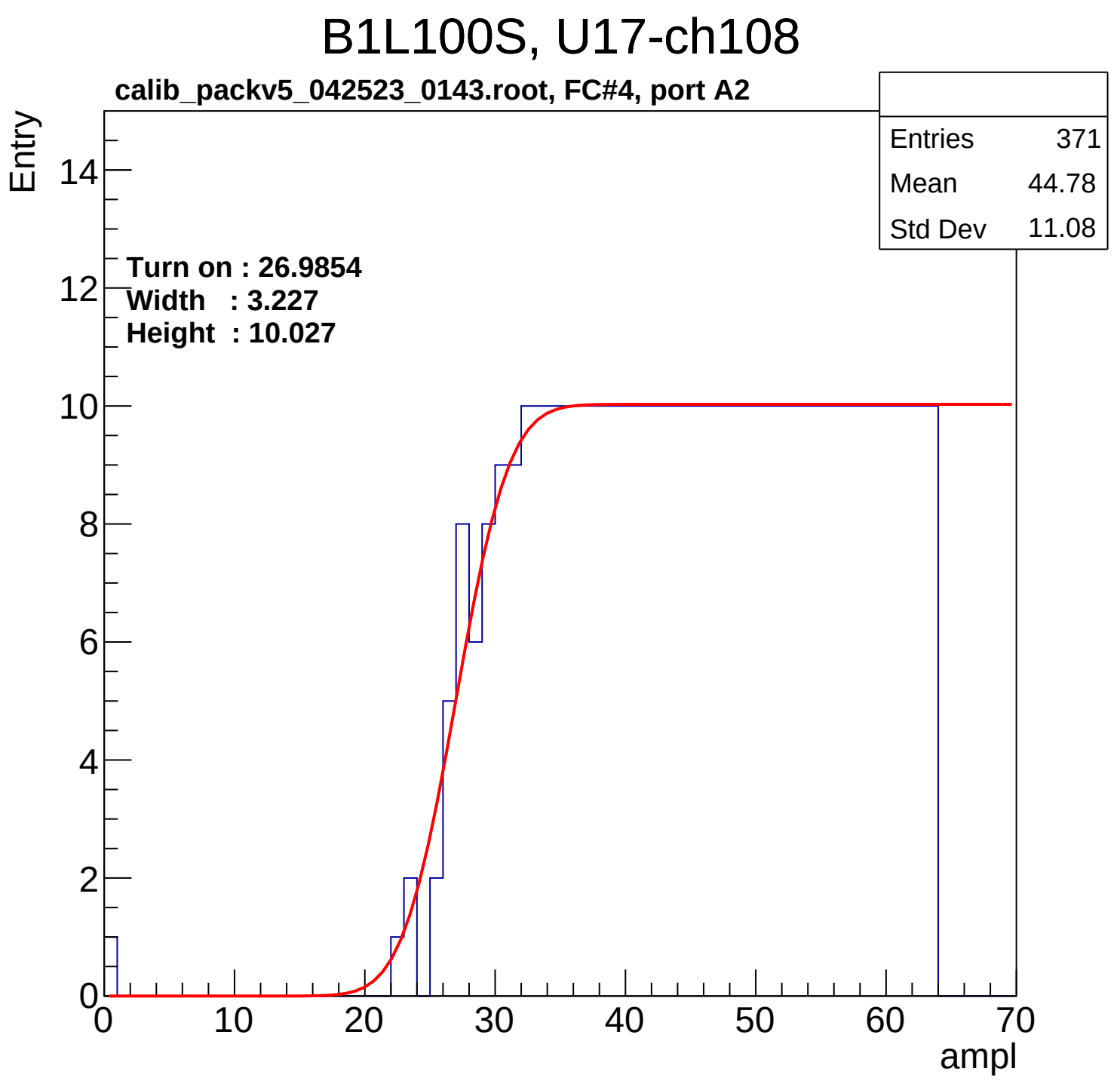
B1L100S, U17-ch108
calib_packv5_042523_0143.root, FC#4, port A2
Entries 371
Mean 44.78
Std Dev 11.08
Turn on : 26.9854
Width : 3.227
Height : 10.027
Entry
ampl
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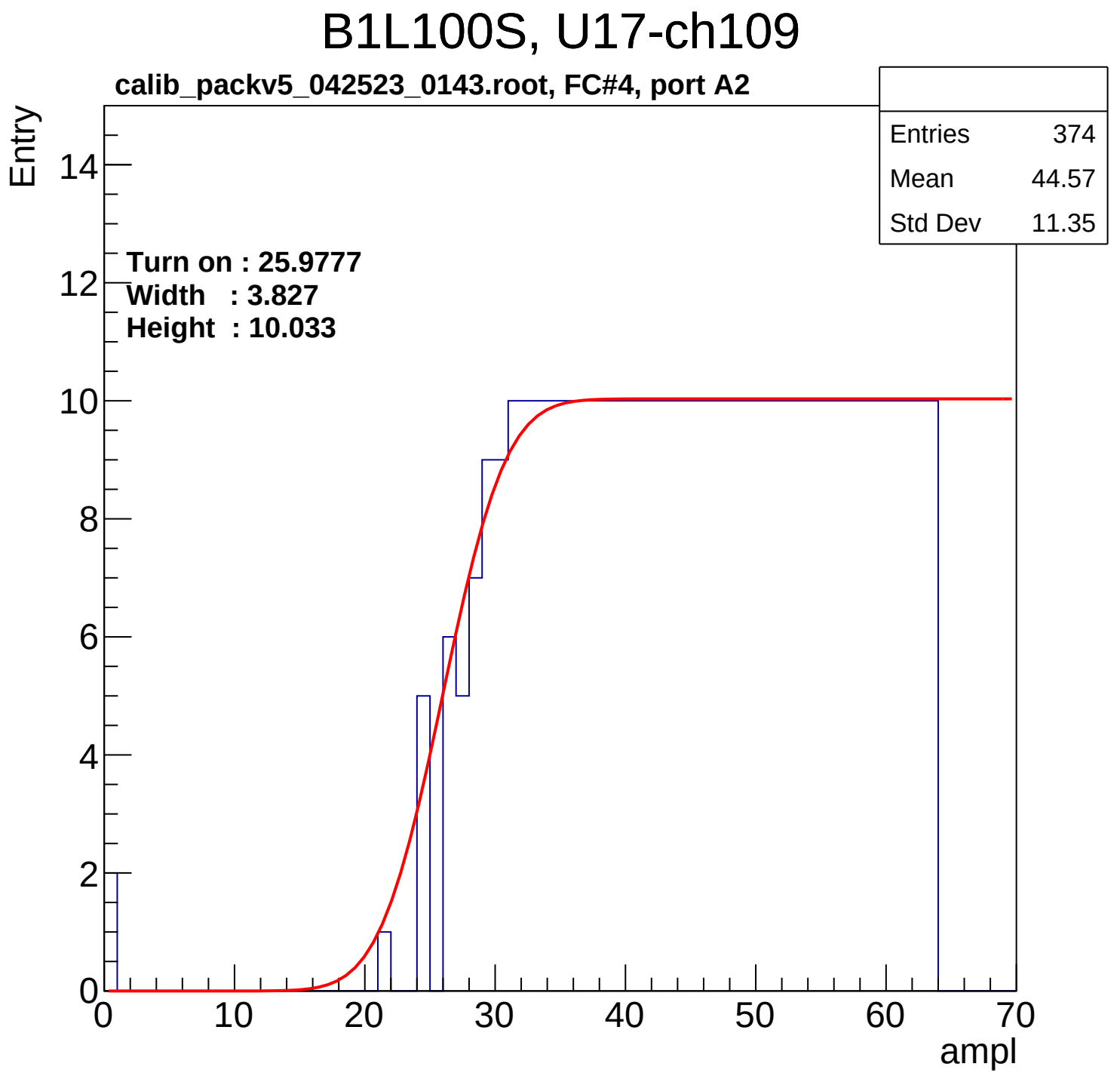
B1L100S, U17-ch109
calib_packv5_042523_0143.root, FC#4, port A2
Entries 374
Mean 44.57
Std Dev 11.35
Turn on : 25.9777
Width : 3.827
Height : 10.033
Entry
ampl
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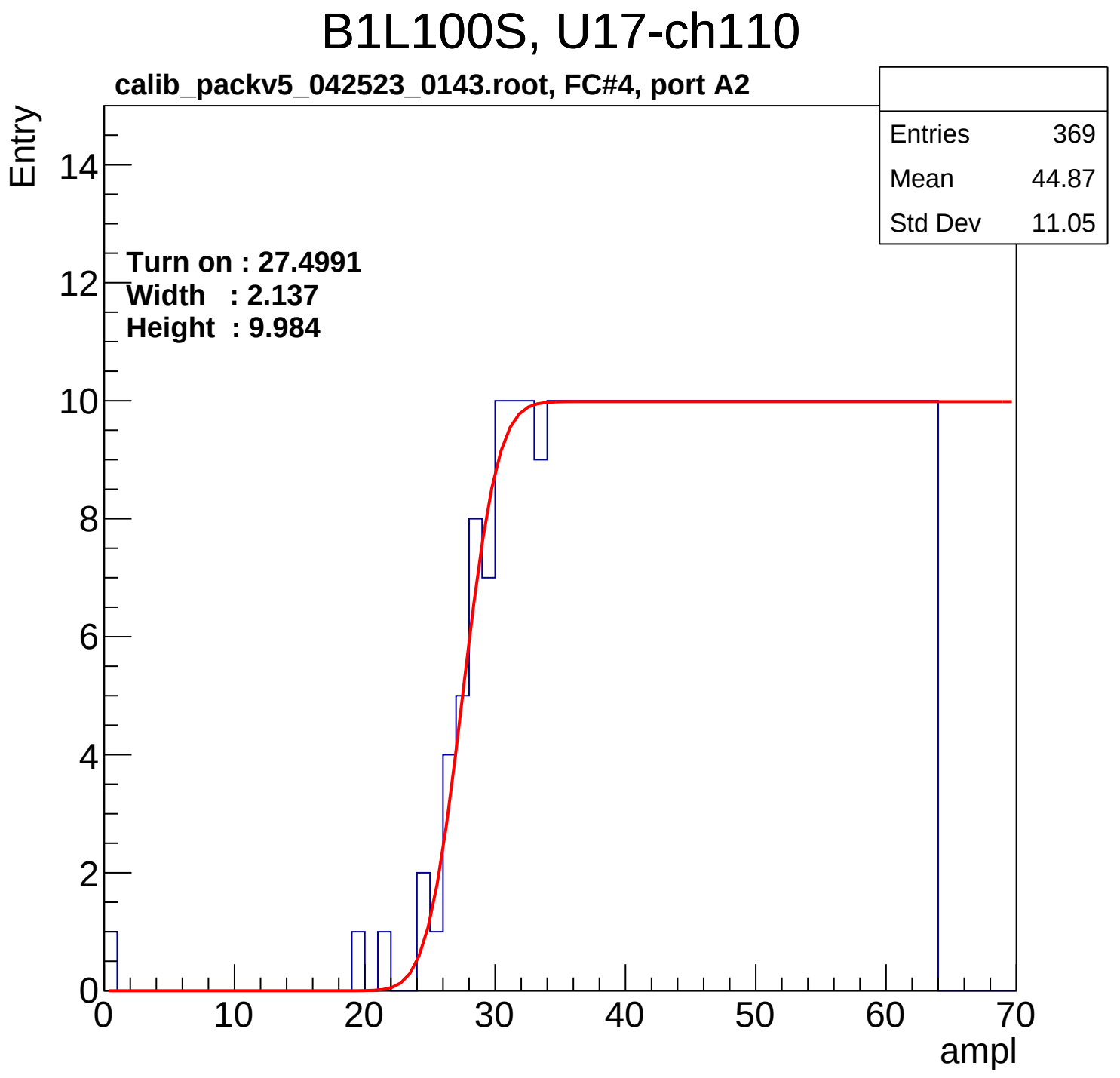
B1L100S, U17-ch110
calib_packv5_042523_0143.root, FC#4, port A2
Entries 369
Mean 44.87
Std Dev 11.05
Turn on : 27.4991
Width : 2.137
Height : 9.984
Entry
ampl
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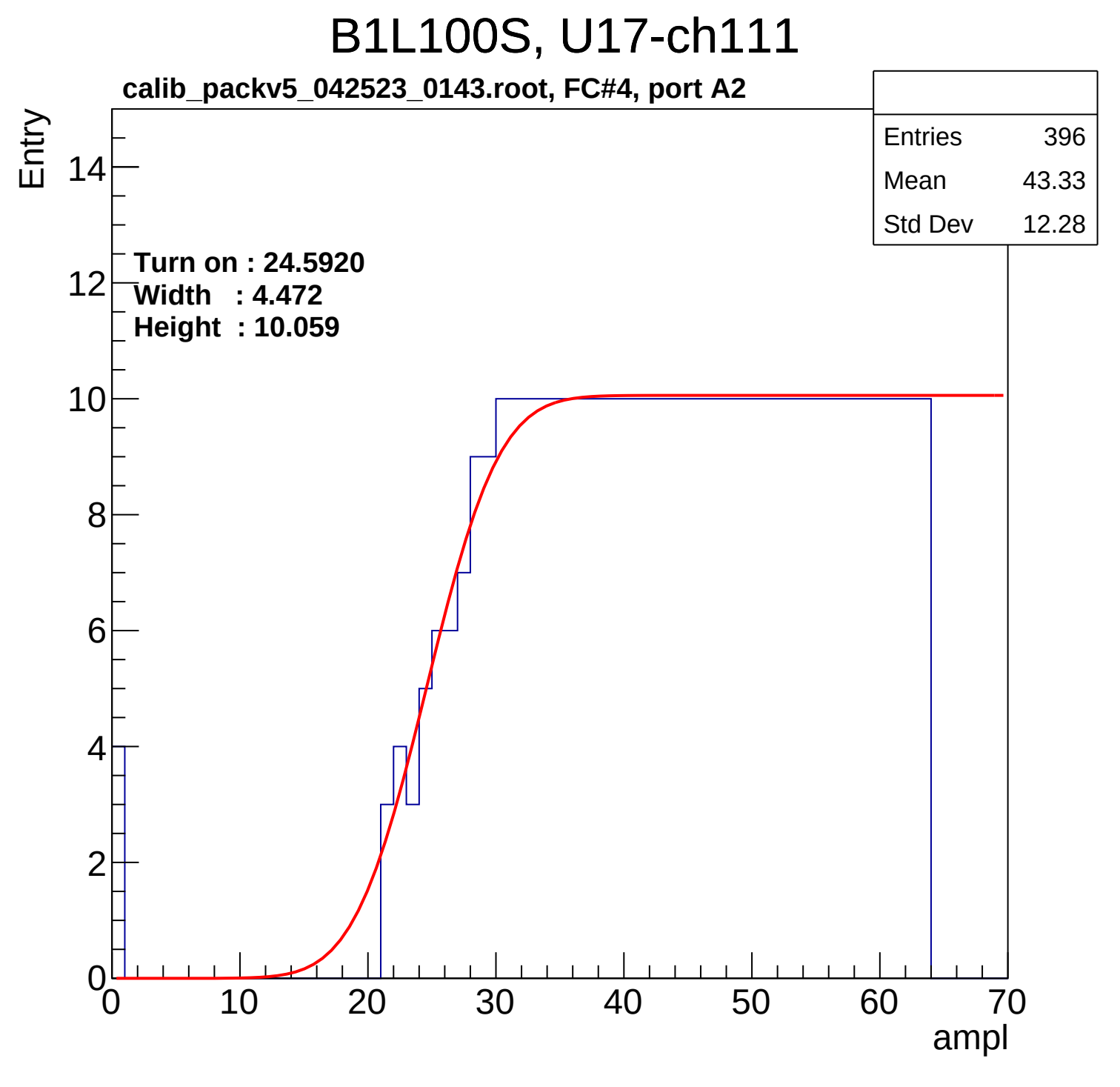
B1L100S, U17-ch111
calib_packv5_042523_0143.root, FC#4, port A2
Entries 396
Mean 43.33
Std Dev 12.28
Turn on : 24.5920
Width : 4.472
Height : 10.059
Entry
ampl
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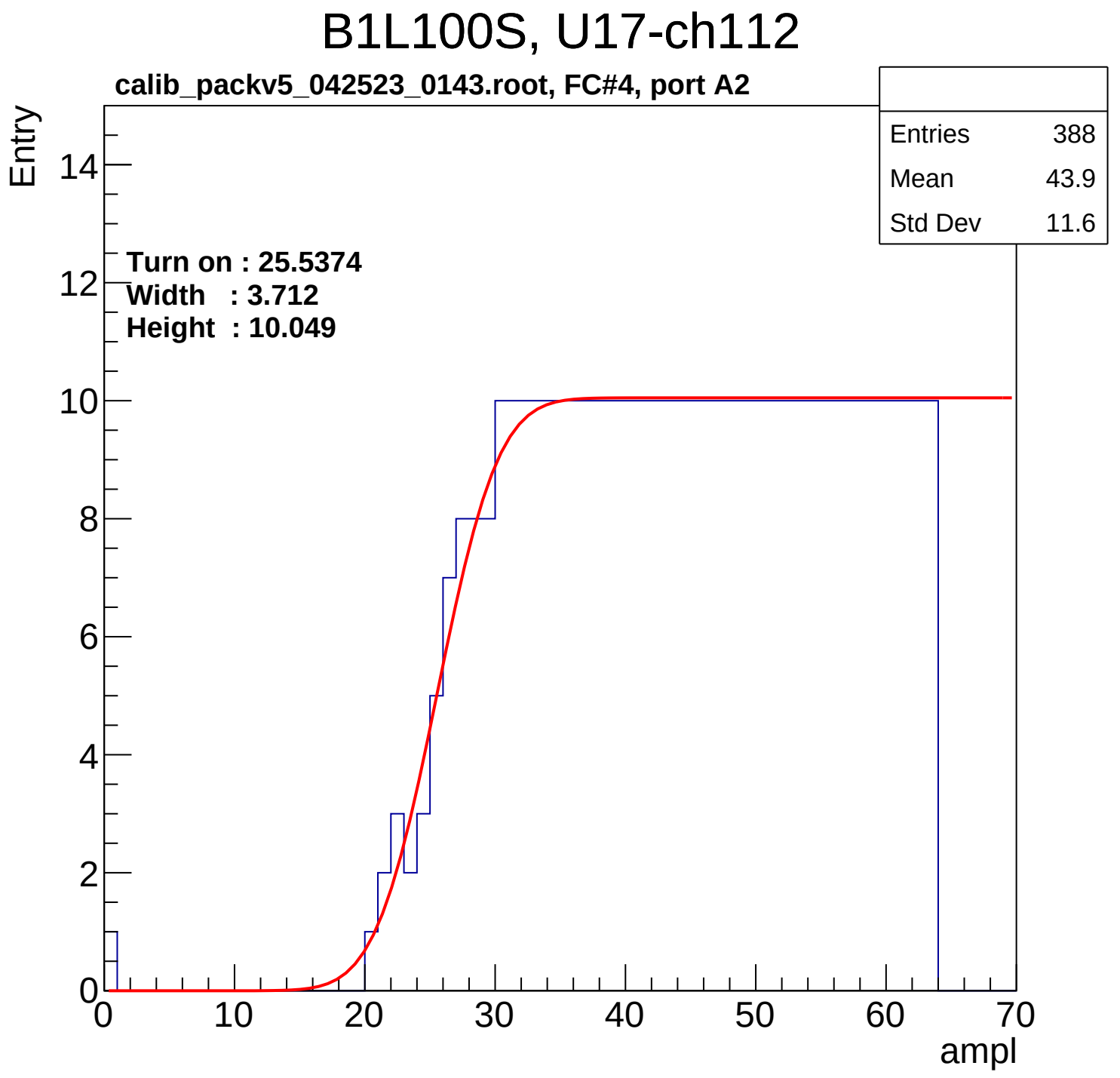
B1L100S, U17-ch112
calib_packv5_042523_0143.root, FC#4, port A2
Entries 388
Mean 43.9
Std Dev 11.6
Turn on : 25.5374
Width : 3.712
Height : 10.049
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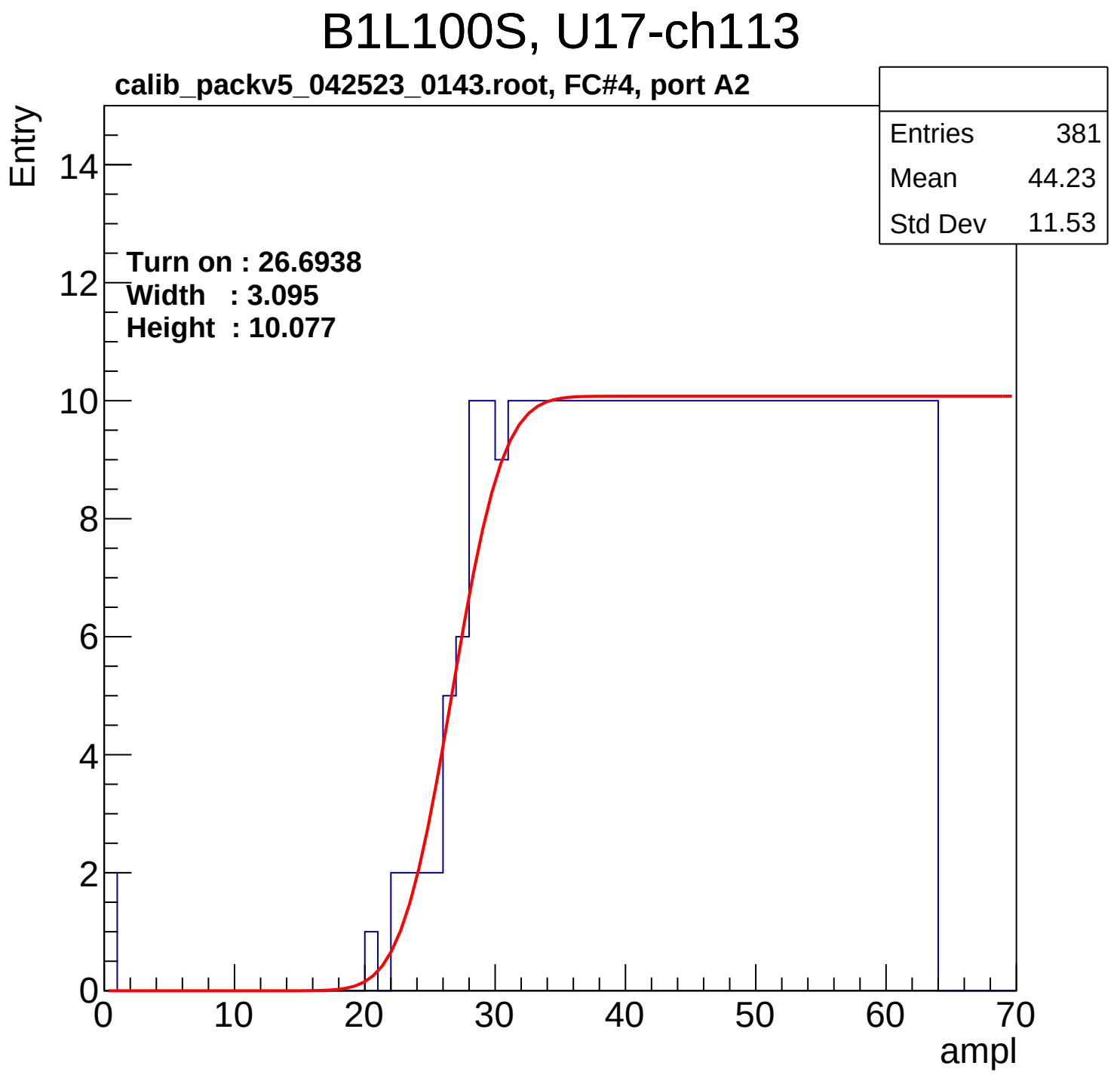
B1L100S, U17-ch113
calib_packv5_042523_0143.root, FC#4, port A2
Entries 381
Mean 44.23
Std Dev 11.53
Turn on : 26.6938
Width : 3.095
Height : 10.077
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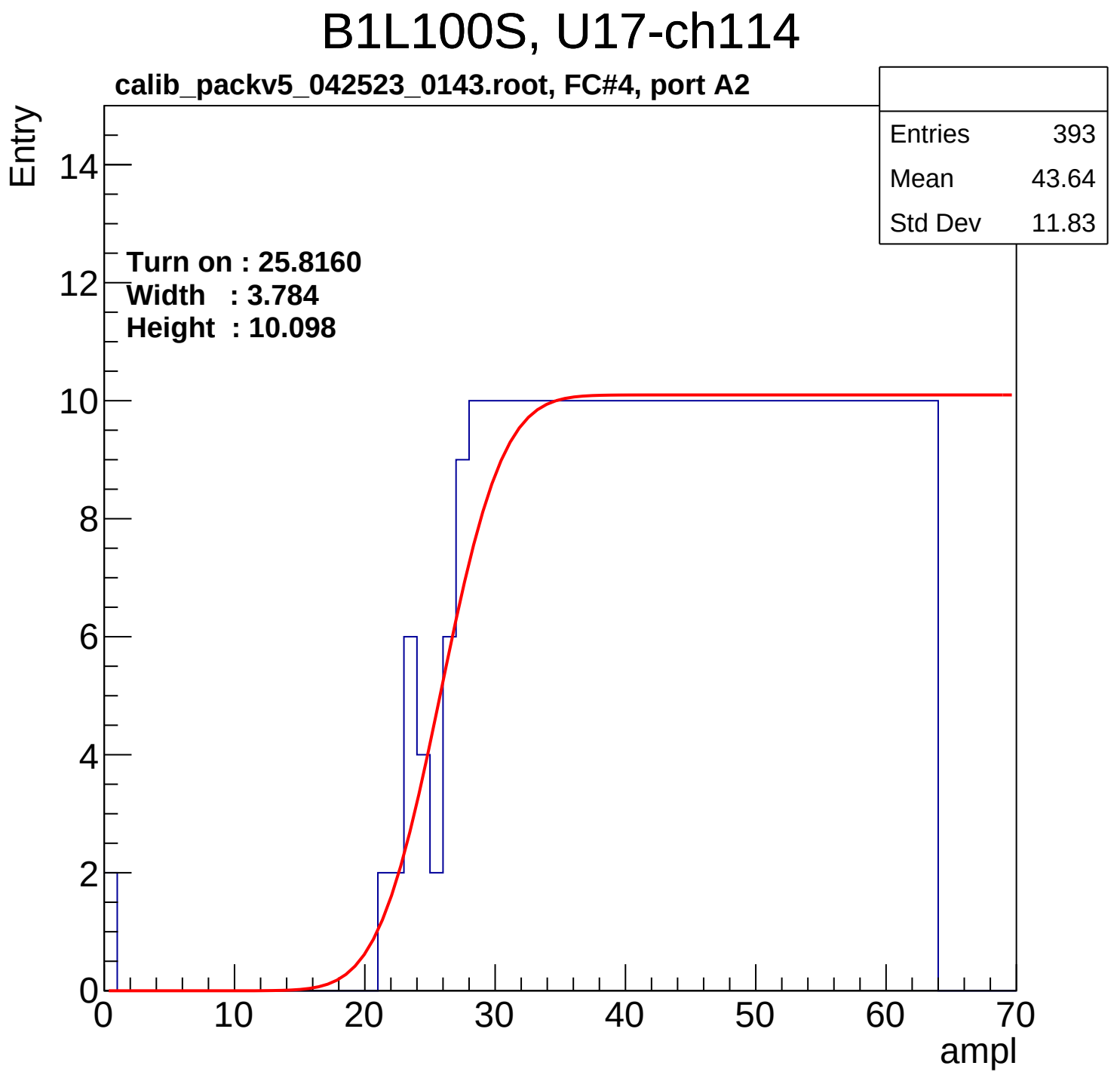
B1L100S, U17-ch114
calib_packv5_042523_0143.root, FC#4, port A2
Entries 393
Mean 43.64
Std Dev 11.83
Turn on : 25.8160
Width : 3.784
Height : 10.098
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ampl
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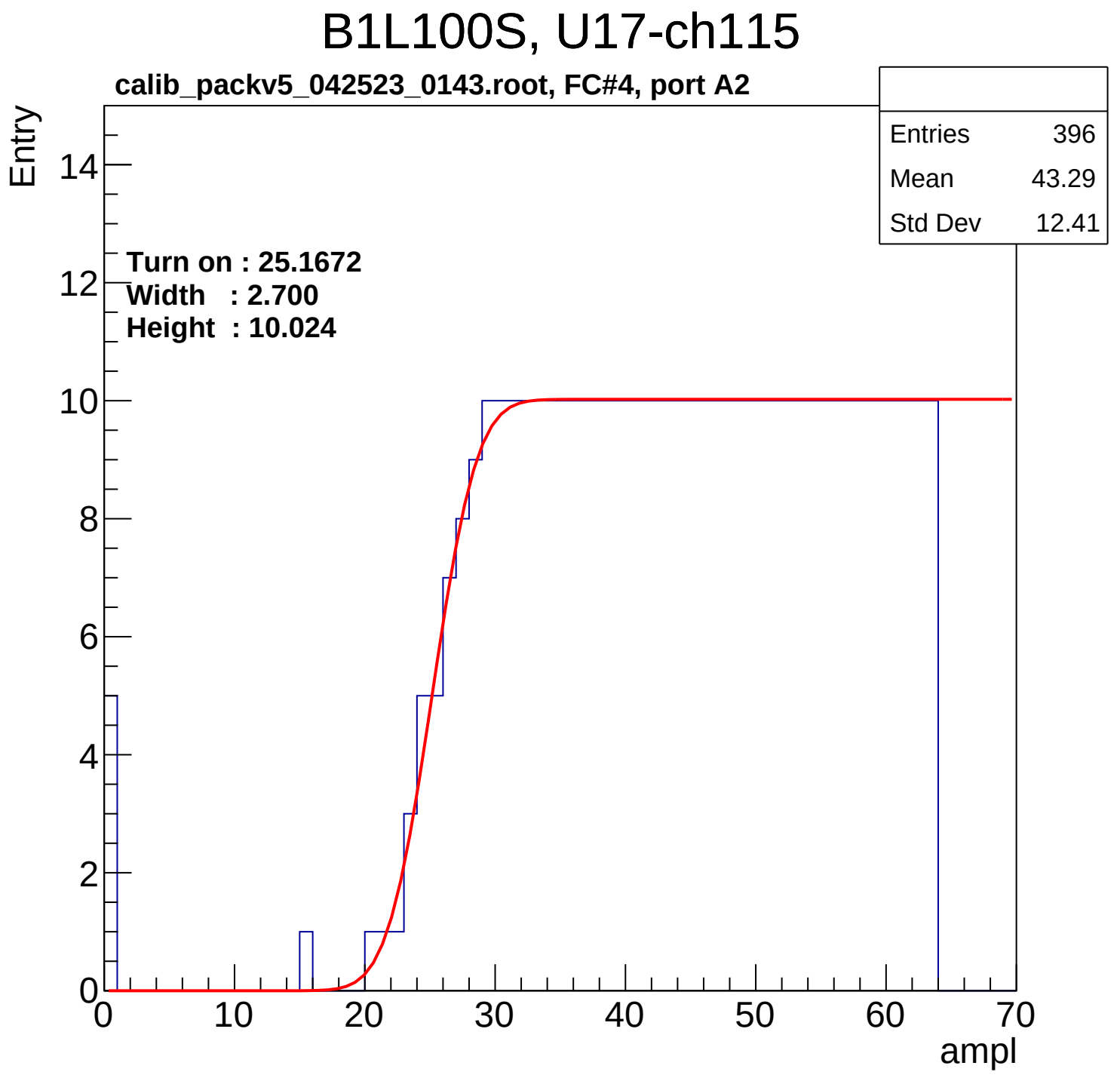
B1L100S, U17-ch115
calib_packv5_042523_0143.root, FC#4, port A2
Entries 396
Mean 43.29
Std Dev 12.41
Turn on : 25.1672
Width : 2.700
Height : 10.024
Entry
ampl
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4
6
8
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10
20
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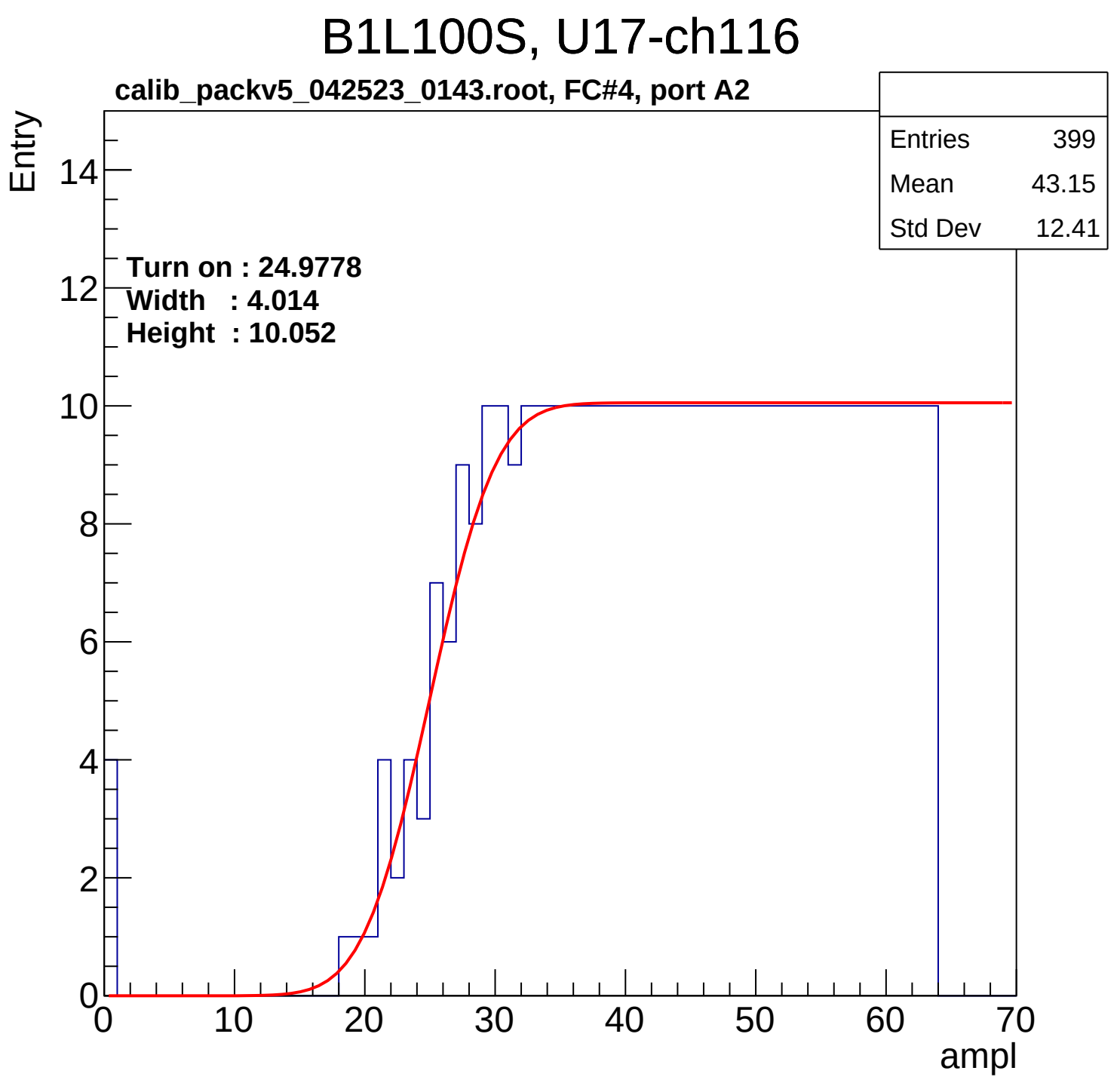
B1L100S, U17-ch116
calib_packv5_042523_0143.root, FC#4, port A2
Entries 399
Mean 43.15
Std Dev 12.41
Turn on : 24.9778
Width : 4.014
Height : 10.052
Entry
ampl
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2
4
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8
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0
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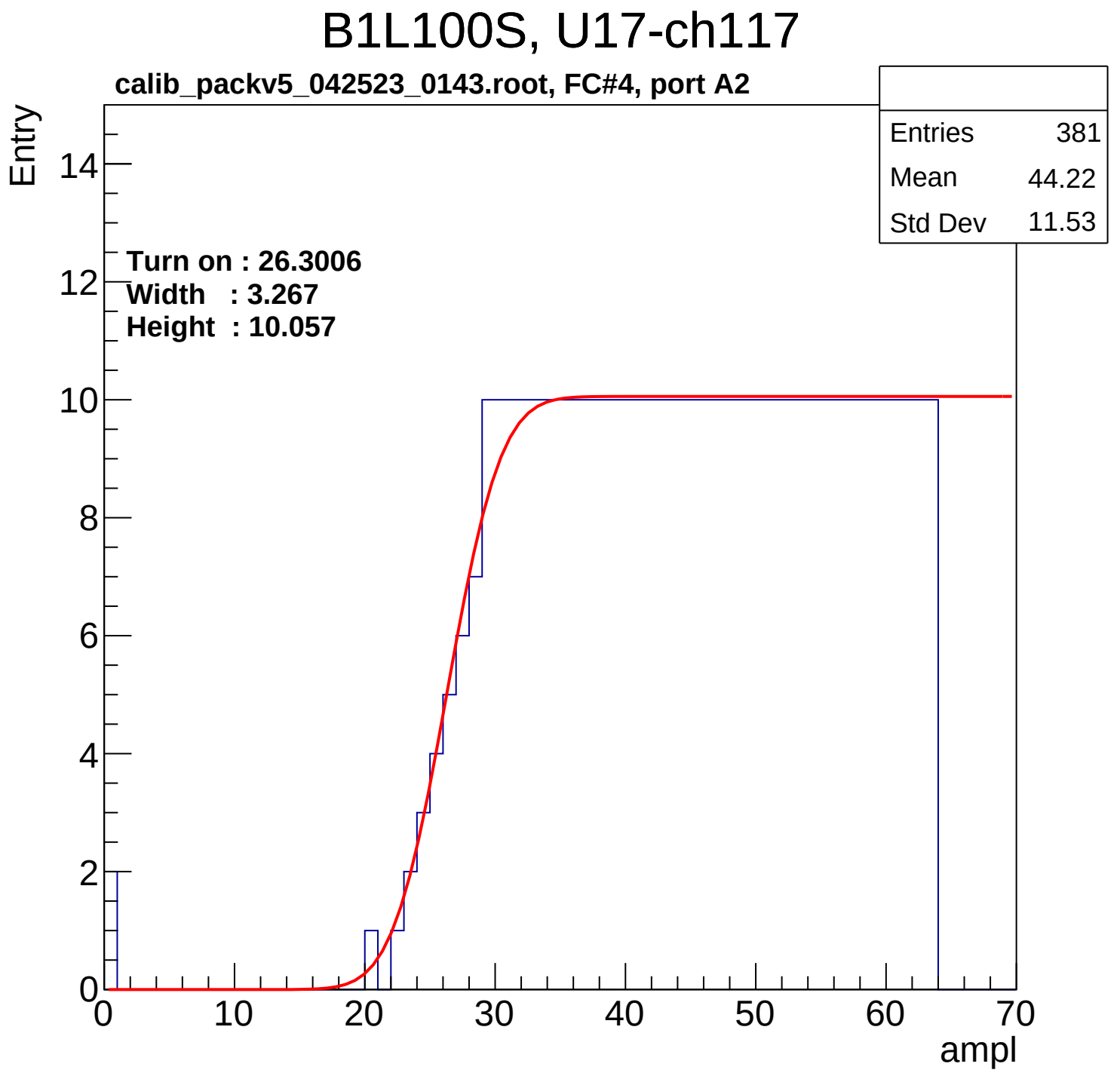
B1L100S, U17-ch117
calib_packv5_042523_0143.root, FC#4, port A2
Entries 381
Mean 44.22
Std Dev 11.53
Turn on : 26.3006
Width : 3.267
Height : 10.057
Entry
ampl
0
2
4
6
8
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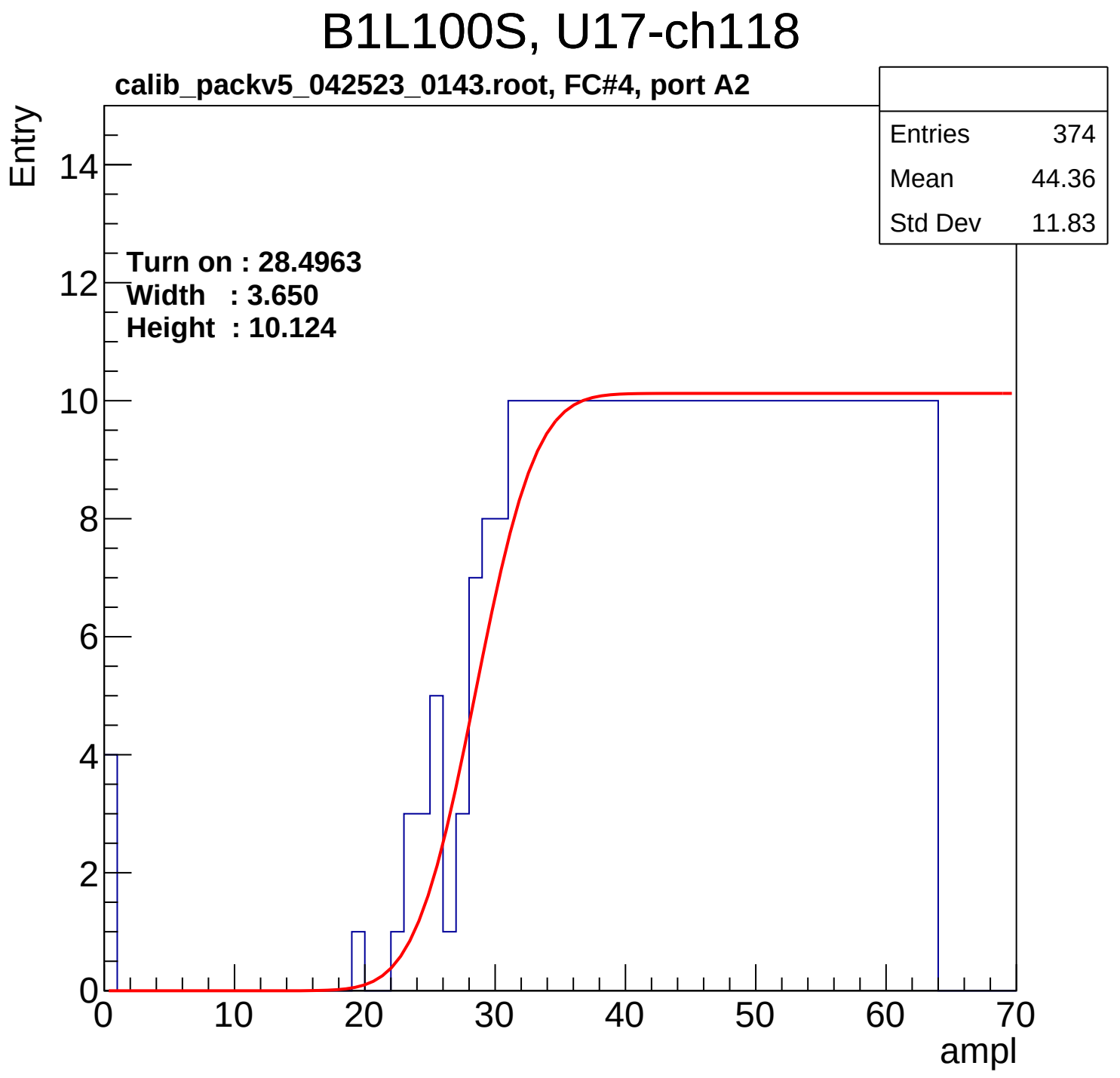
B1L100S, U17-ch118
calib_packv5_042523_0143.root, FC#4, port A2
Entries 374
Mean 44.36
Std Dev 11.83
Turn on : 28.4963
Width : 3.650
Height : 10.124
Entry
ampl
0
2
4
6
8
10
12
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0
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20
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40
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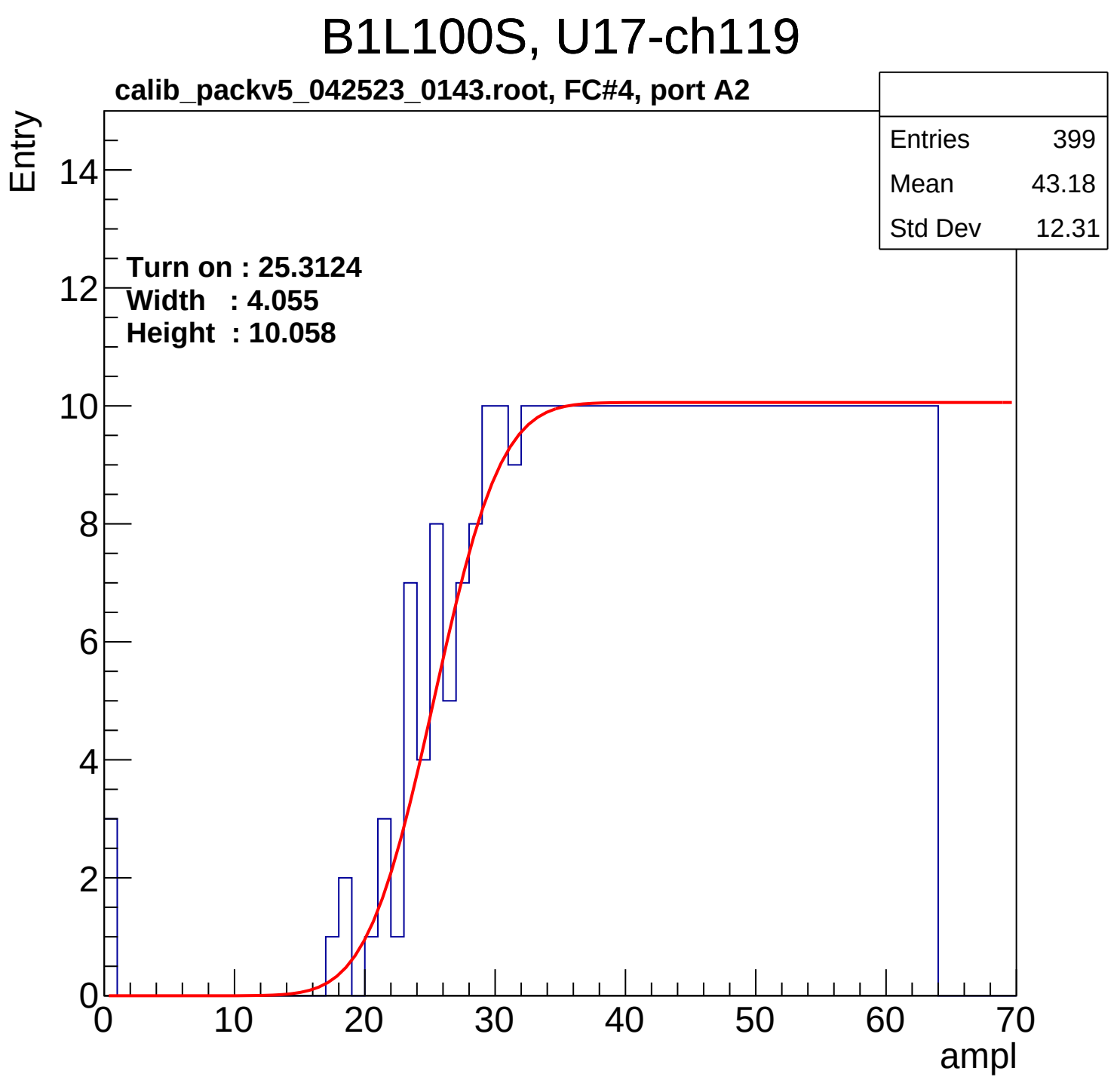
B1L100S, U17-ch119
calib_packv5_042523_0143.root, FC#4, port A2
Entries 399
Mean 43.18
Std Dev 12.31
Turn on : 25.3124
Width : 4.055
Height : 10.058
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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60
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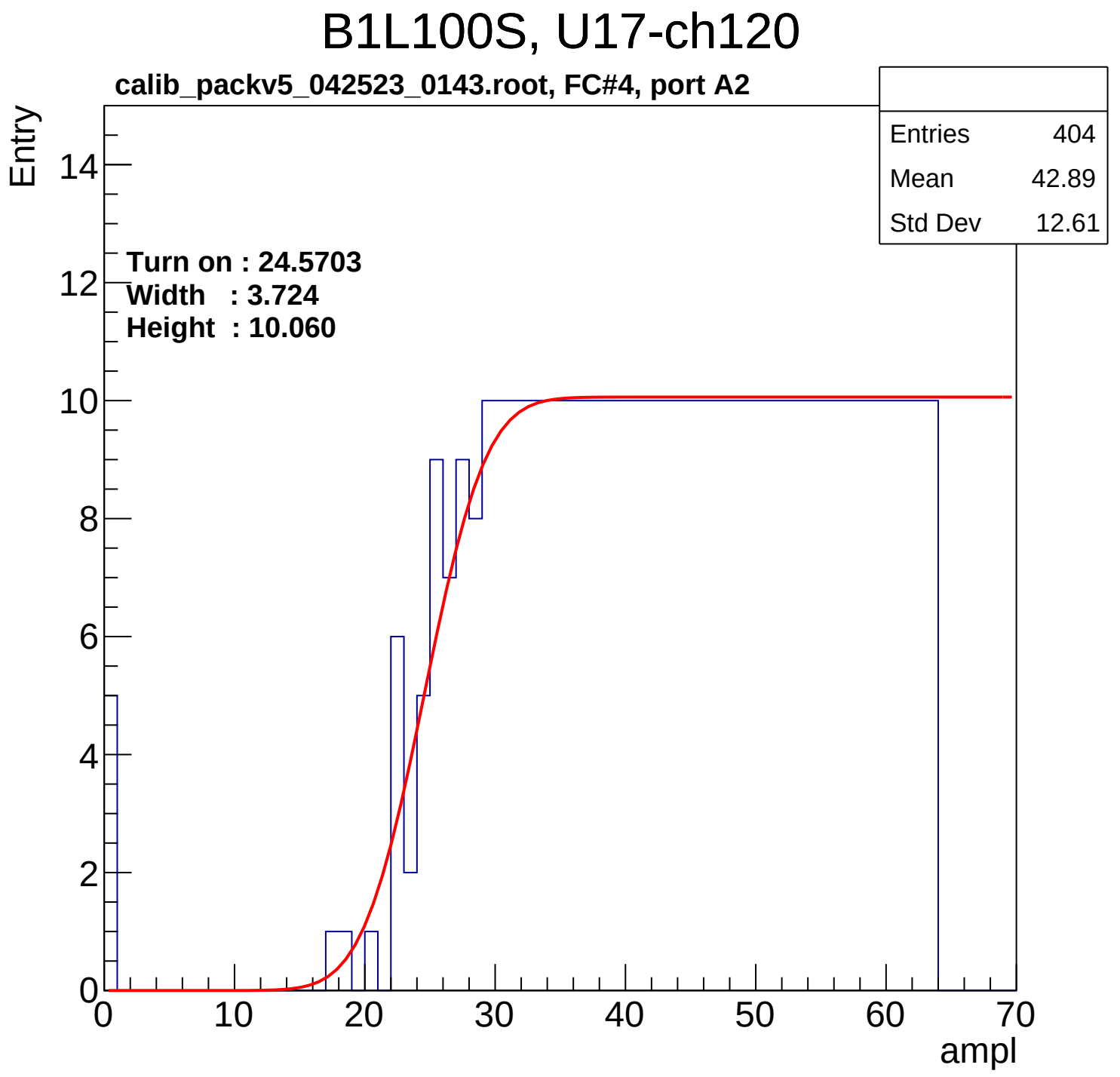
B1L100S, U17-ch120
calib_packv5_042523_0143.root, FC#4, port A2
Entries 404
Mean 42.89
Std Dev 12.61
Turn on : 24.5703
Width : 3.724
Height : 10.060
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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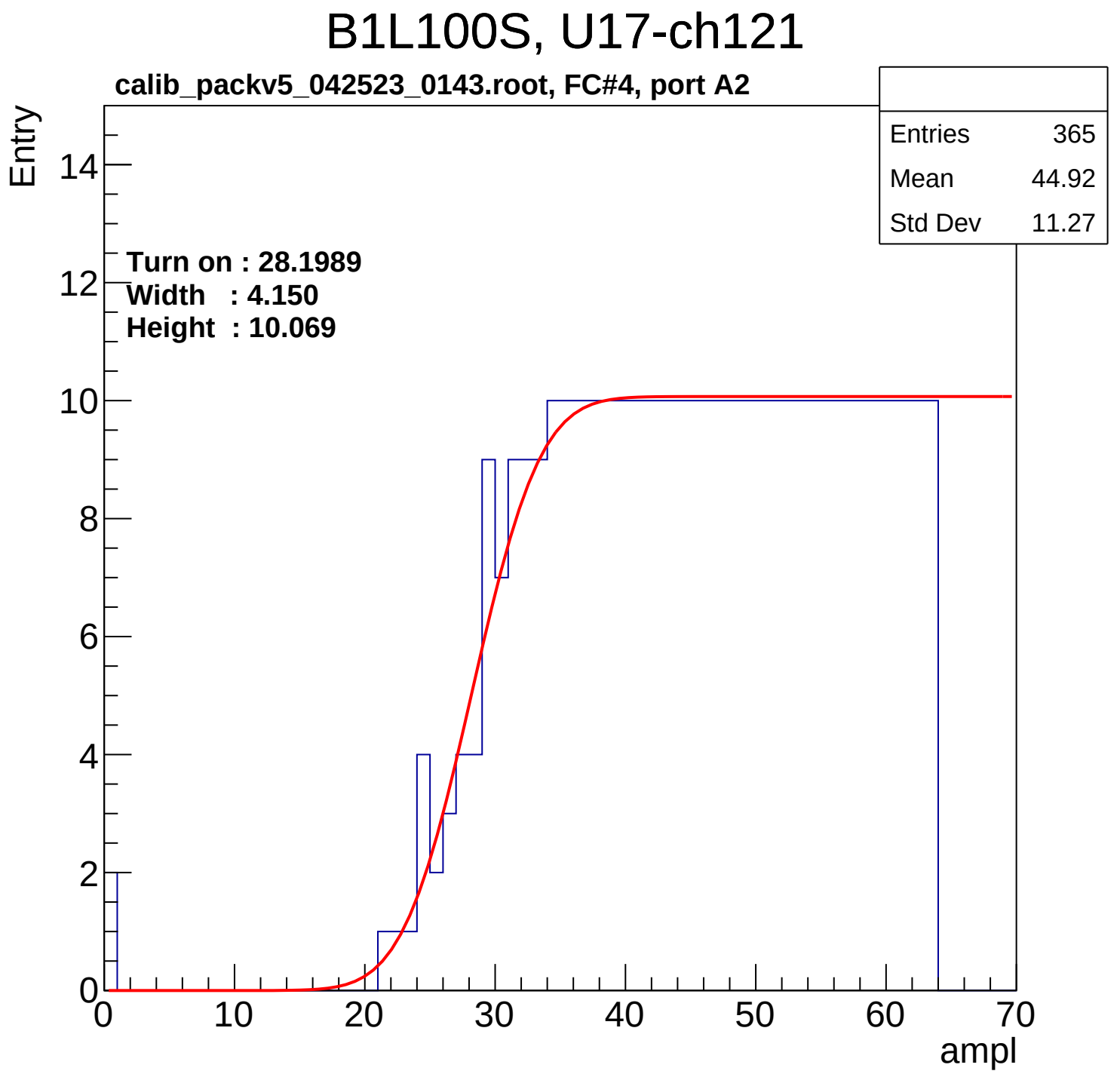
B1L100S, U17-ch121
calib_packv5_042523_0143.root, FC#4, port A2
Entries 365
Mean 44.92
Std Dev 11.27
Turn on : 28.1989
Width : 4.150
Height : 10.069
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
50
60
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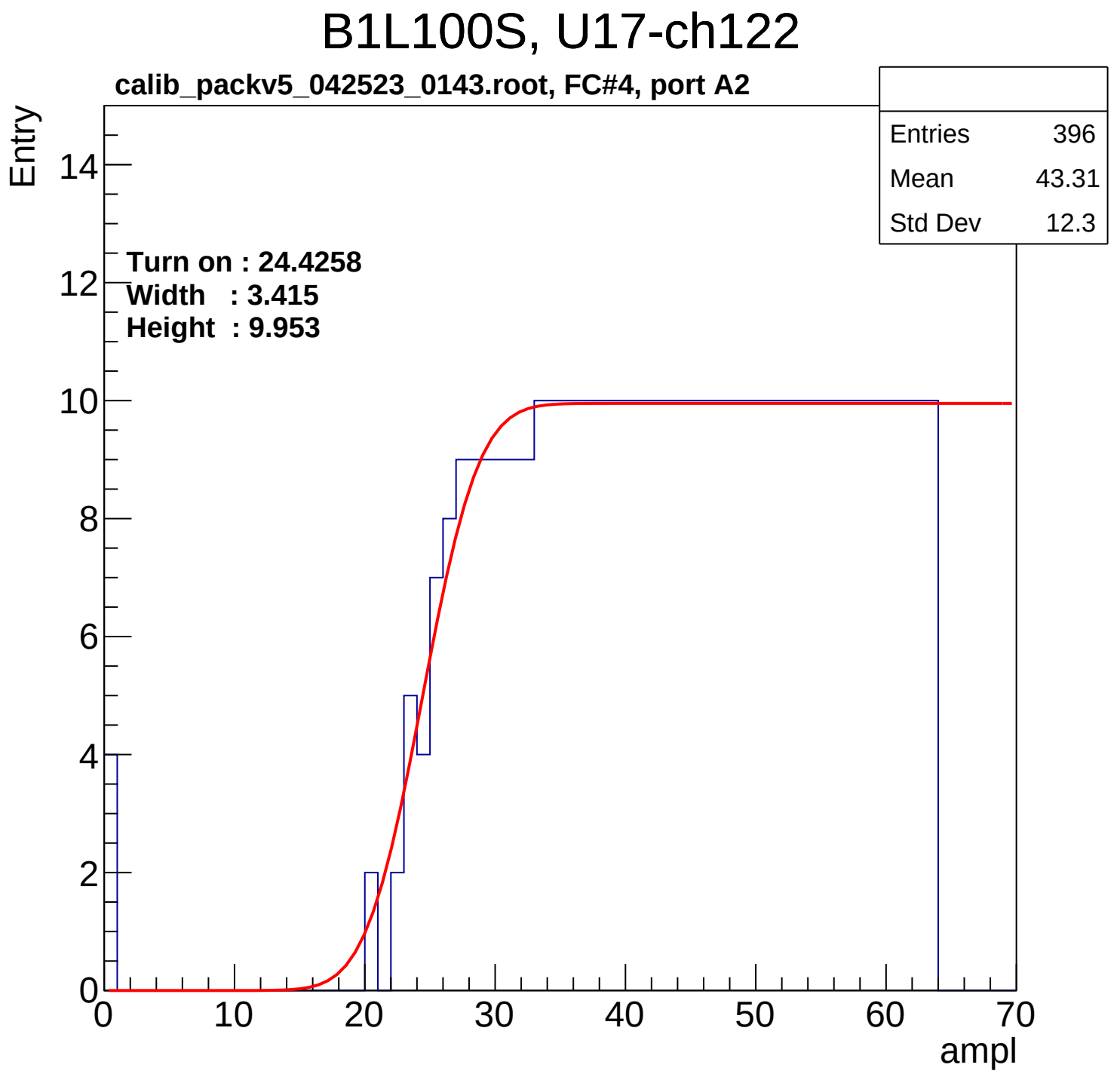
B1L100S, U17-ch122
calib_packv5_042523_0143.root, FC#4, port A2
Entries 396
Mean 43.31
Std Dev 12.3
Turn on : 24.4258
Width : 3.415
Height : 9.953
Entry
ampl
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2
4
6
8
10
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0
10
20
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40
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60
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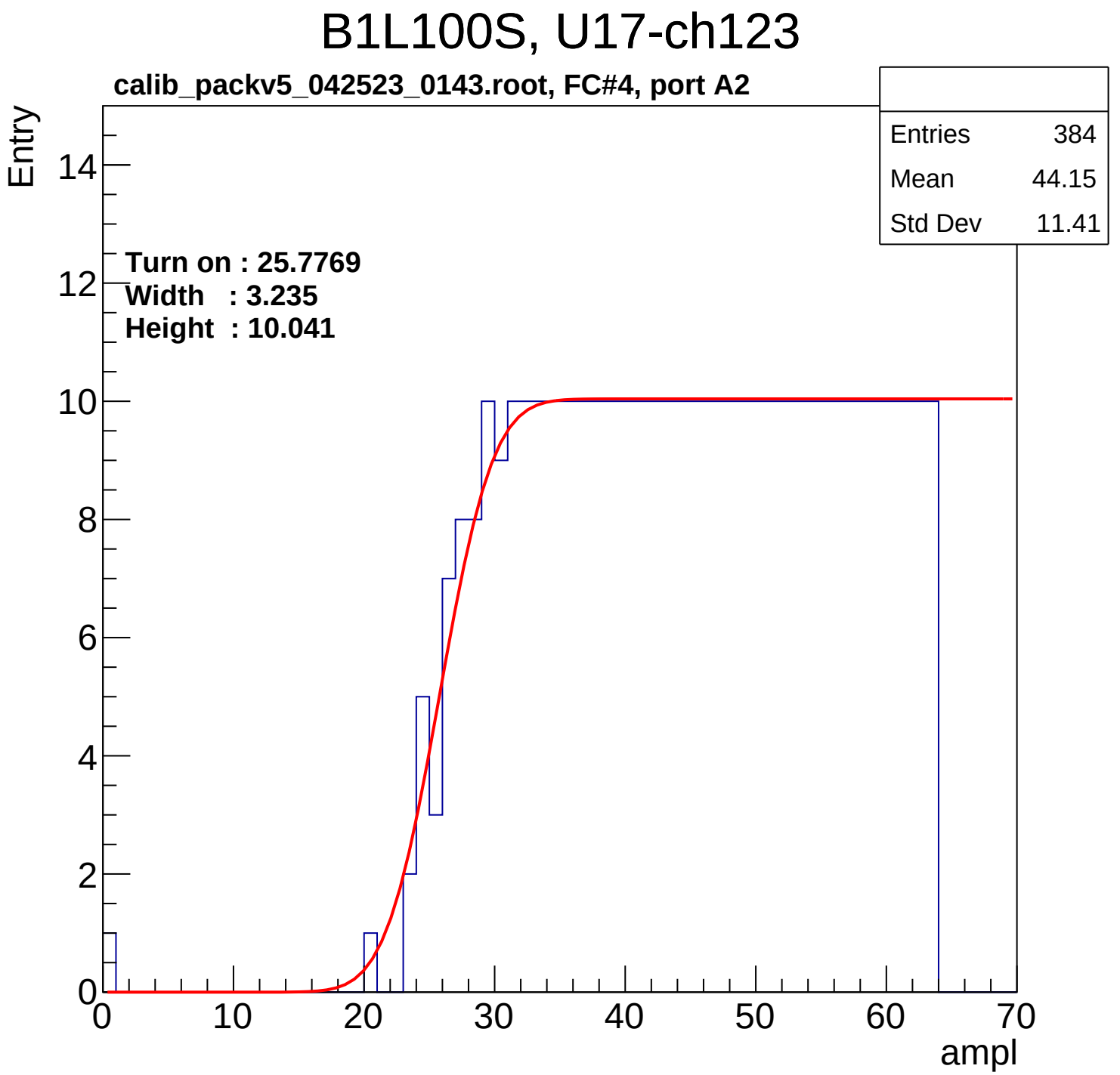
B1L100S, U17-ch123
calib_packv5_042523_0143.root, FC#4, port A2
Entries 384
Mean 44.15
Std Dev 11.41
Turn on : 25.7769
Width : 3.235
Height : 10.041
Entry
ampl
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4
6
8
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40
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60
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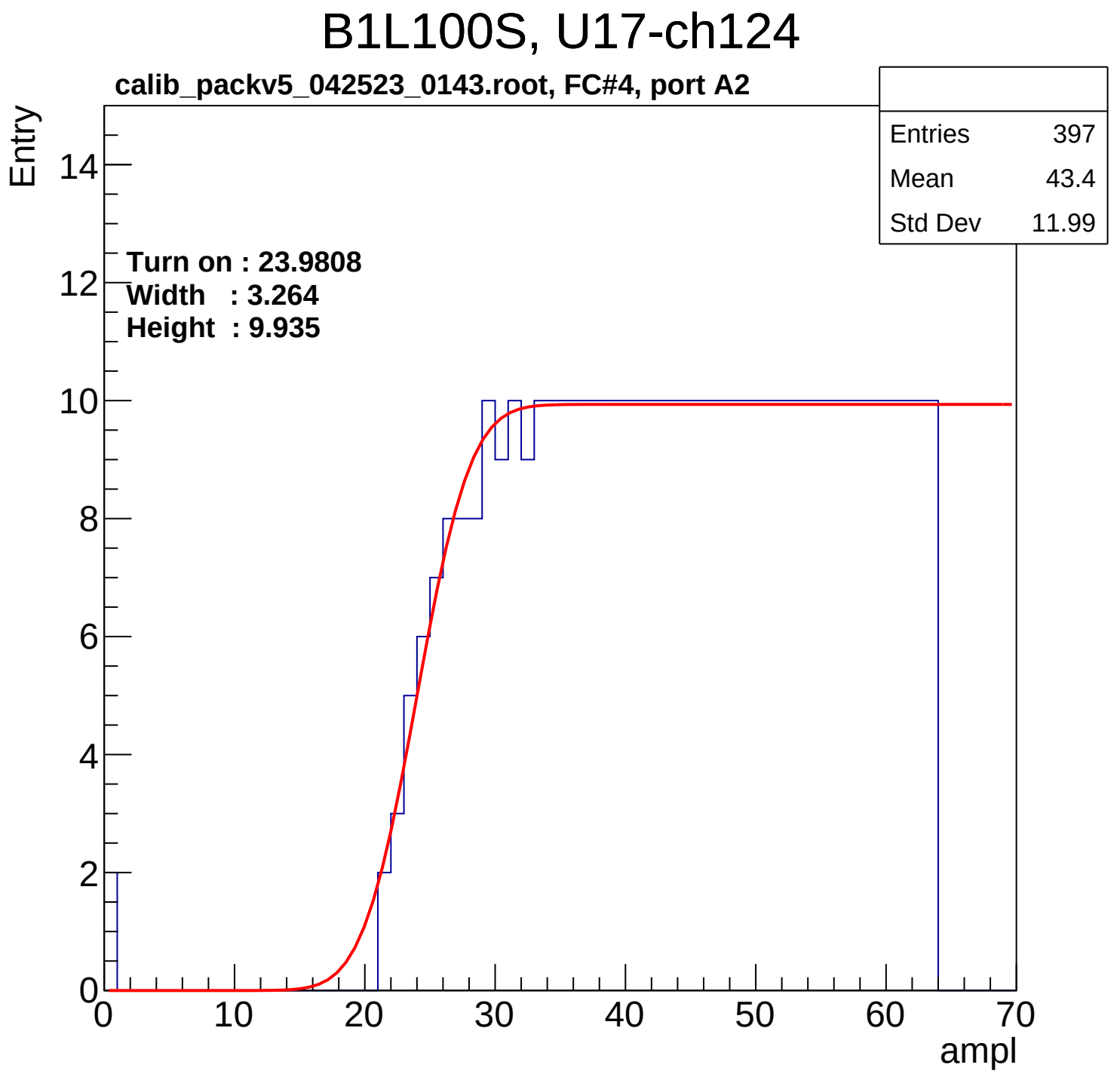
B1L100S, U17-ch124
calib_packv5_042523_0143.root, FC#4, port A2
Entries 397
Mean 43.4
Std Dev 11.99
Turn on : 23.9808
Width : 3.264
Height : 9.935
Entry
ampl
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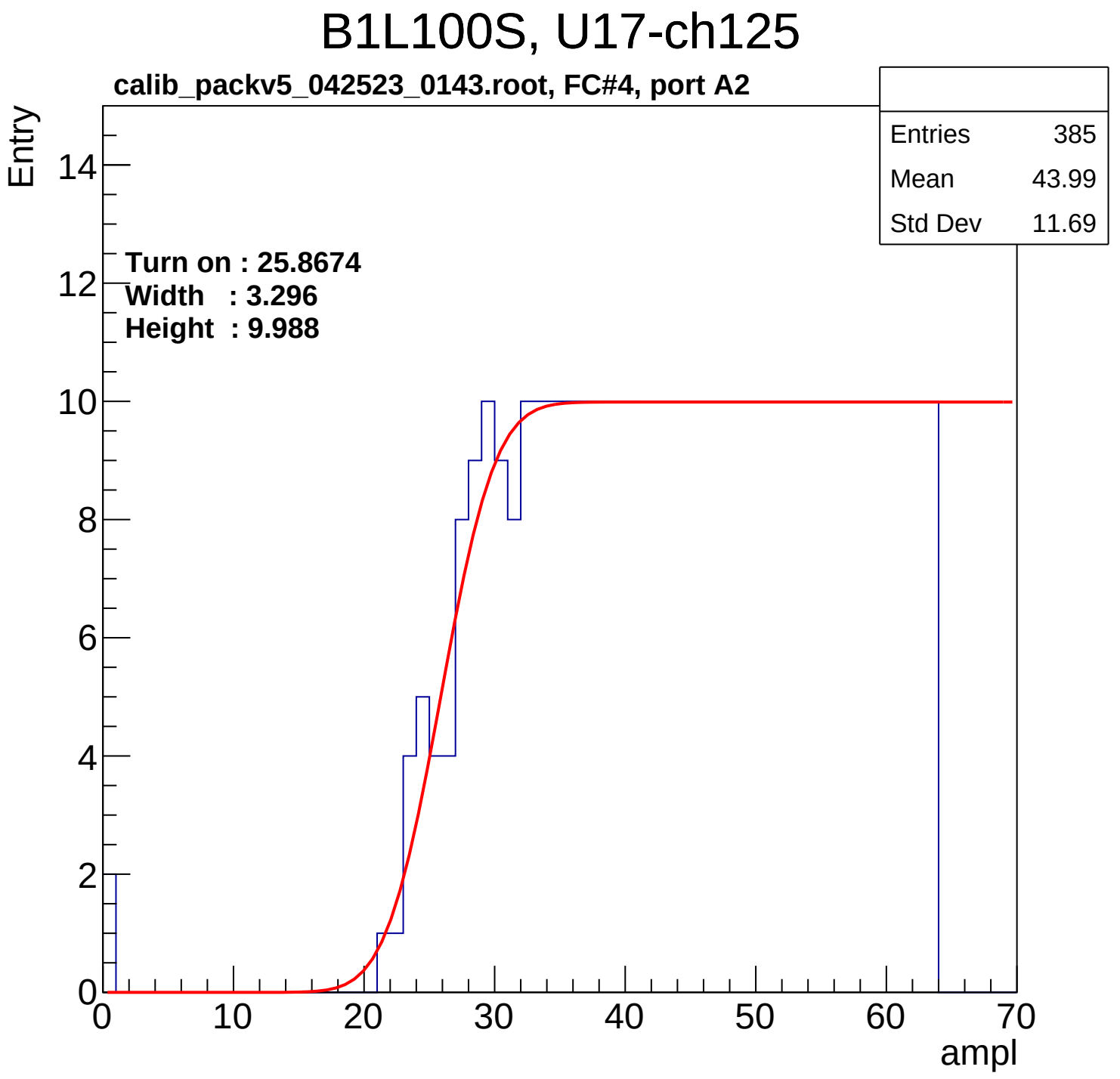
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L100S, U17-ch125
calib_packv5_042523_0143.root, FC#4, port A2
Entries 385
Mean 43.99
Std Dev 11.69
Turn on : 25.8674
Width : 3.296
Height : 9.988
Entry
ampl
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2
4
6
8
10
12
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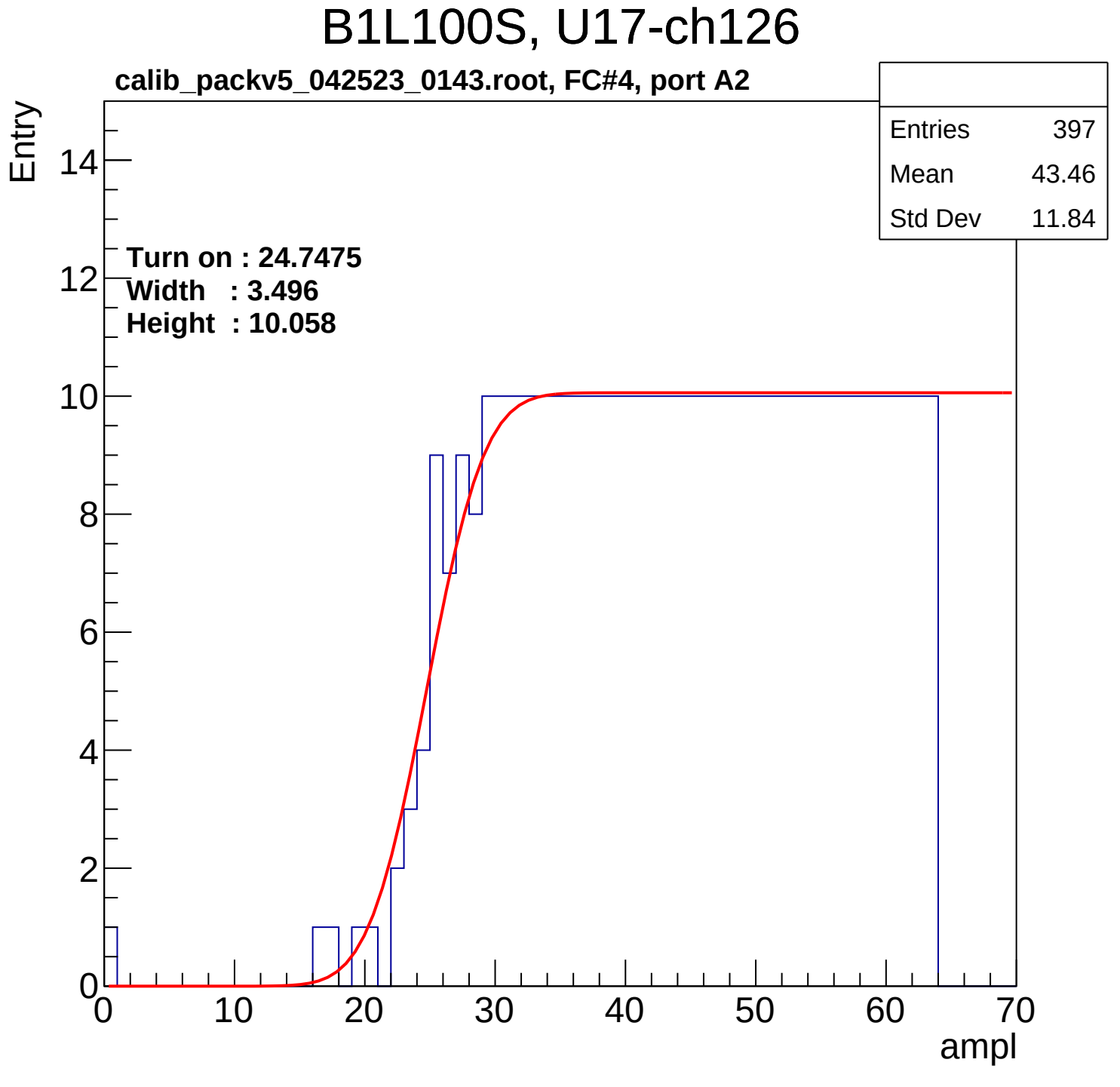
0
10
20
30
40
50
60
70


B1L100S, U17-ch126
calib_packv5_042523_0143.root, FC#4, port A2
Entries 397
Mean 43.46
Std Dev 11.84
Turn on : 24.7475
Width : 3.496
Height : 10.058
Entry
ampl
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6
8
10
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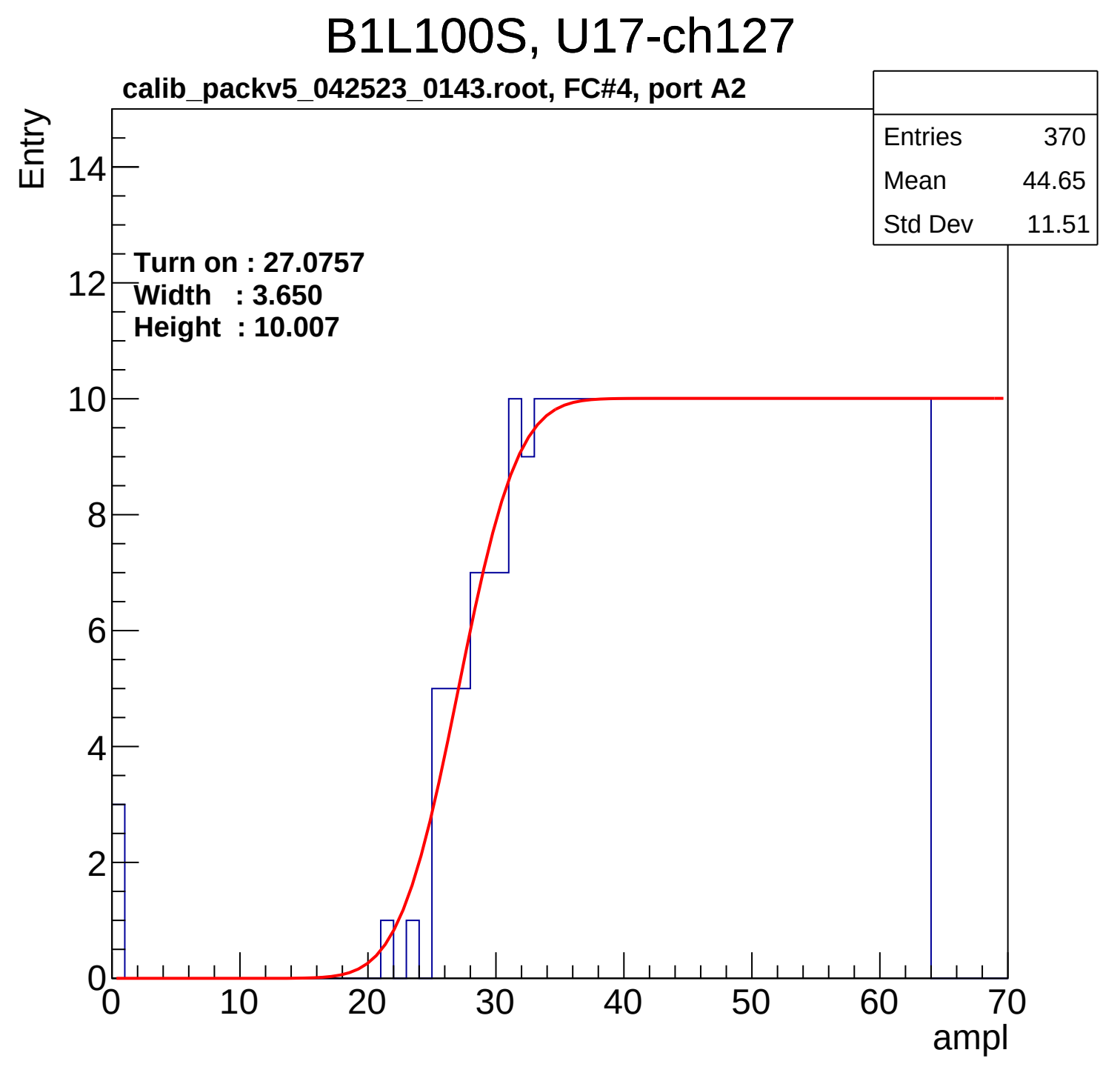
B1L100S, U17-ch127
calib_packv5_042523_0143.root, FC#4, port A2
Entries 370
Mean 44.65
Std Dev 11.51
Turn on : 27.0757
Width : 3.650
Height : 10.007
Entry
ampl
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6
8
10
12
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0
10
20
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60
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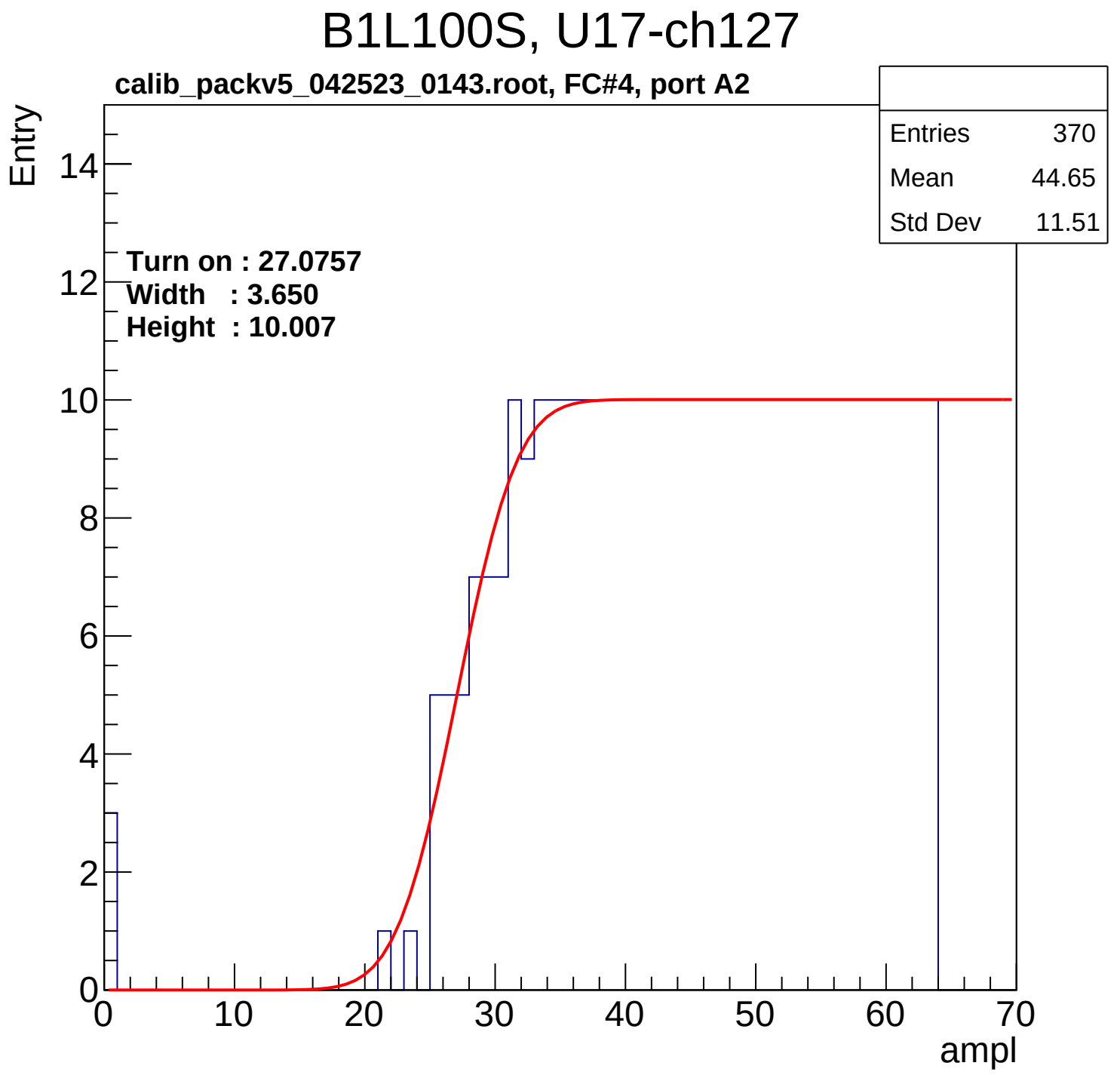
B1L100S, U17-ch127
calib_packv5_042523_0143.root, FC#4, port A2
Entries 370
Mean 44.65
Std Dev 11.51
Turn on : 27.0757
Width : 3.650
Height : 10.007
Entry
ampl
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2
4
6
8
10
12
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0
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20
30
40
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