

B1L103S, U12-ch0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	464
Mean	37.37
Std Dev	18.49

Turn on : 24.4662

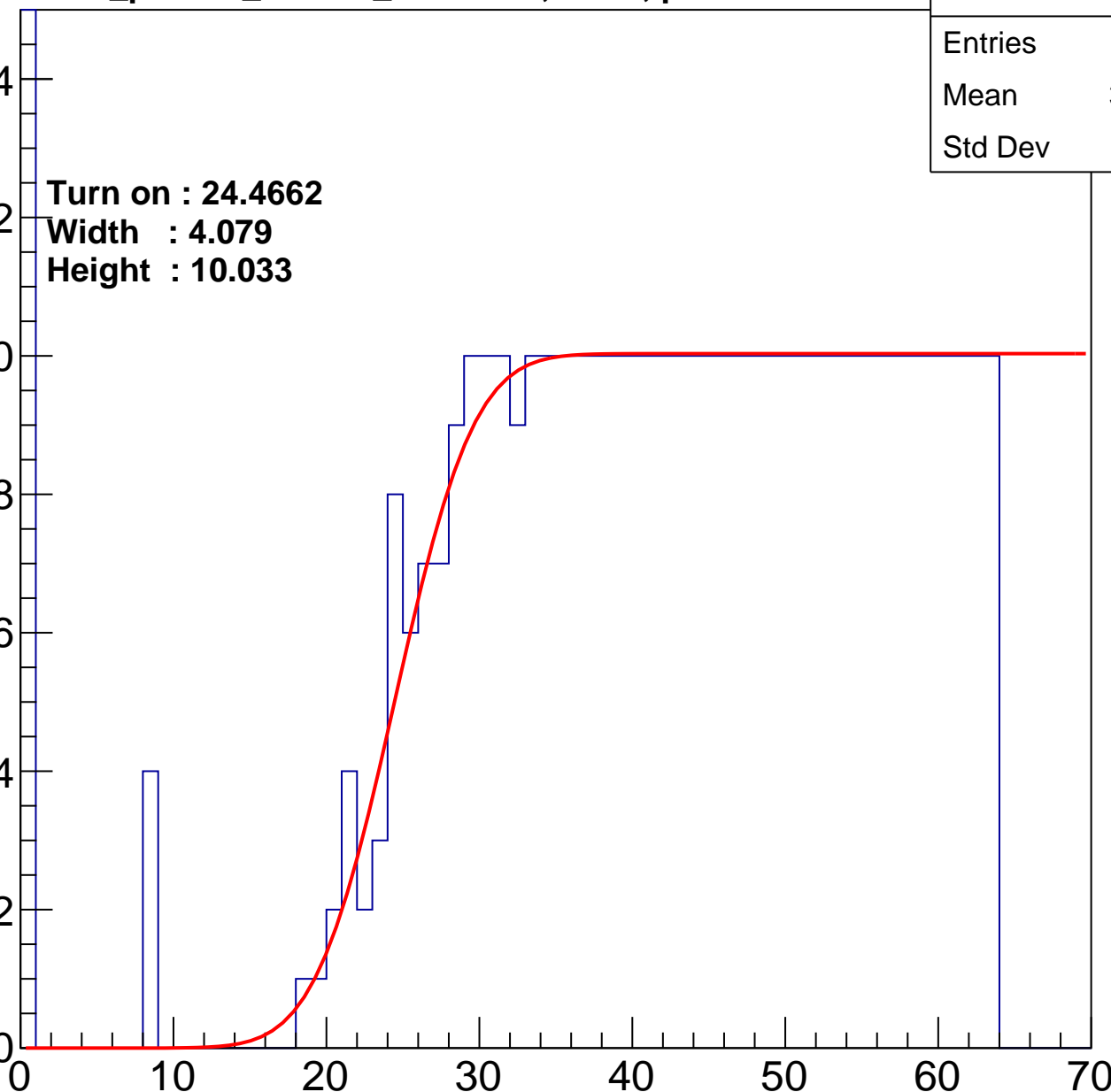
Width : 4.079

Height : 10.033

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	419
Mean	40.46
Std Dev	16.39

Turn on : 26.1008

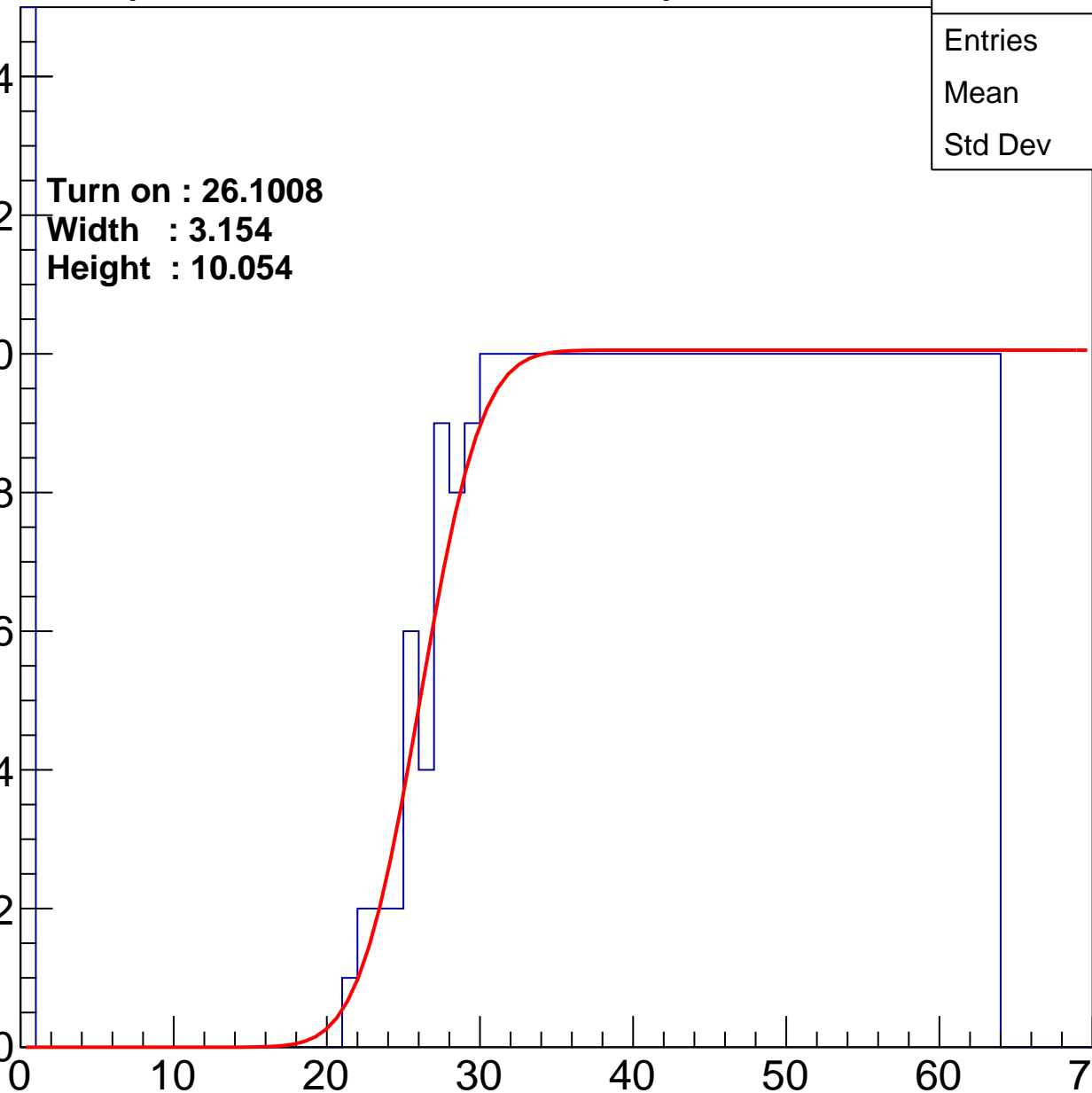
Width : 3.154

Height : 10.054

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	411
Mean	41
Std Dev	15.98

Turn on : 25.8638

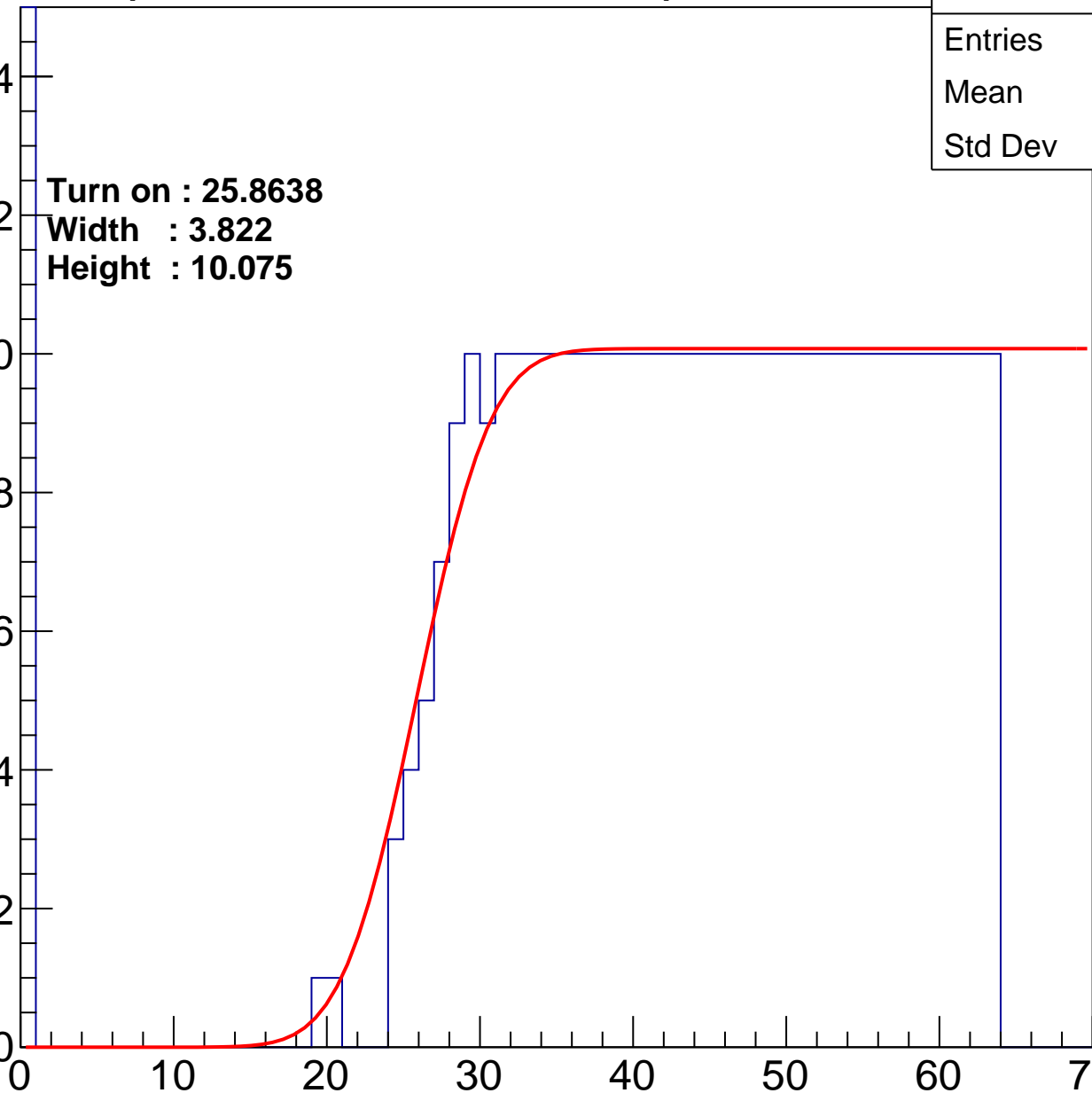
Width : 3.822

Height : 10.075

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	396
Mean	41.46
Std Dev	16.15

Turn on : 28.0933

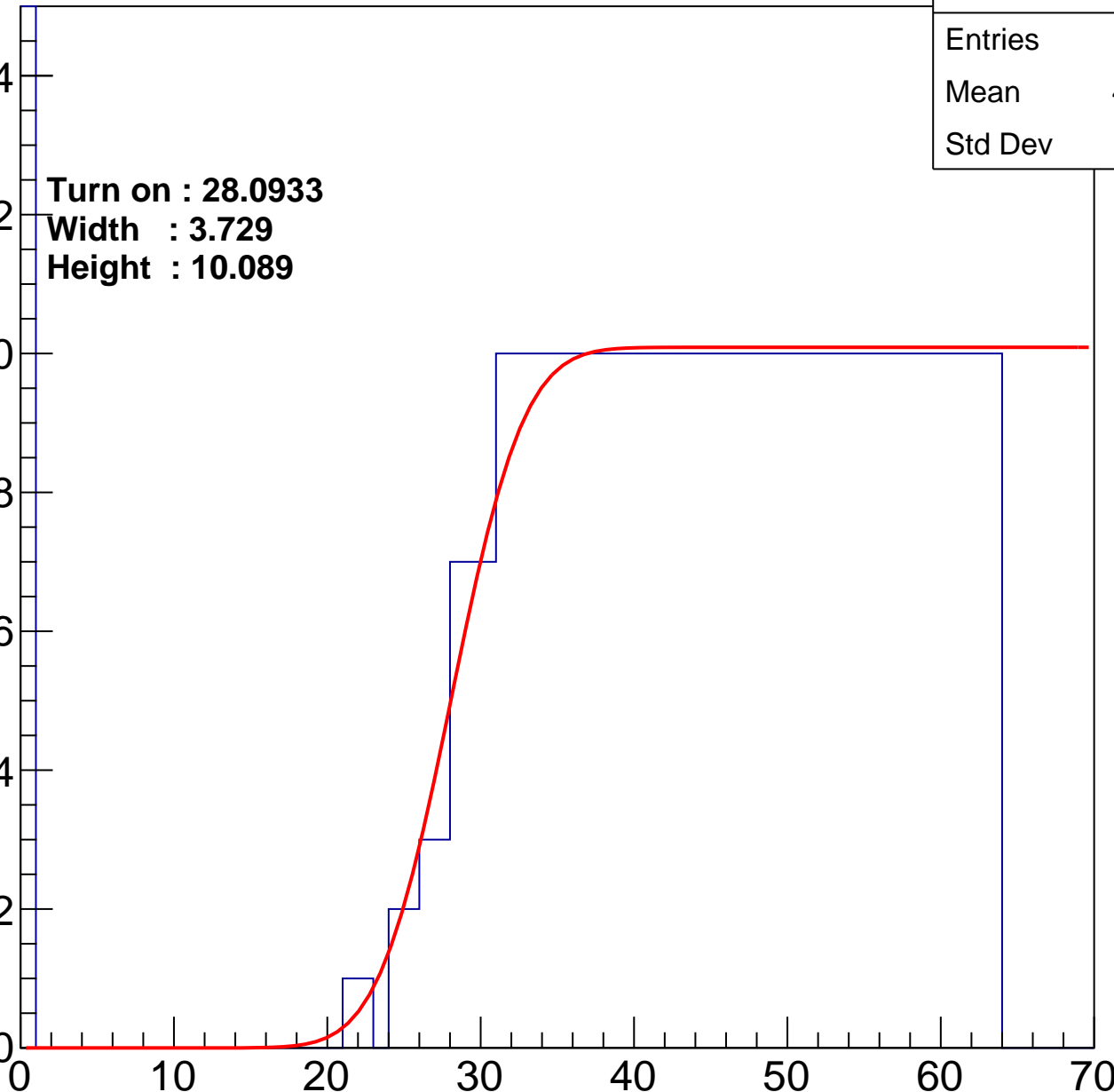
Width : 3.729

Height : 10.089

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch4

calib_packv5_041523_1651.root, FC#0, port C2

Entries	424
Mean	40.04
Std Dev	16.78

Turn on : 25.9586

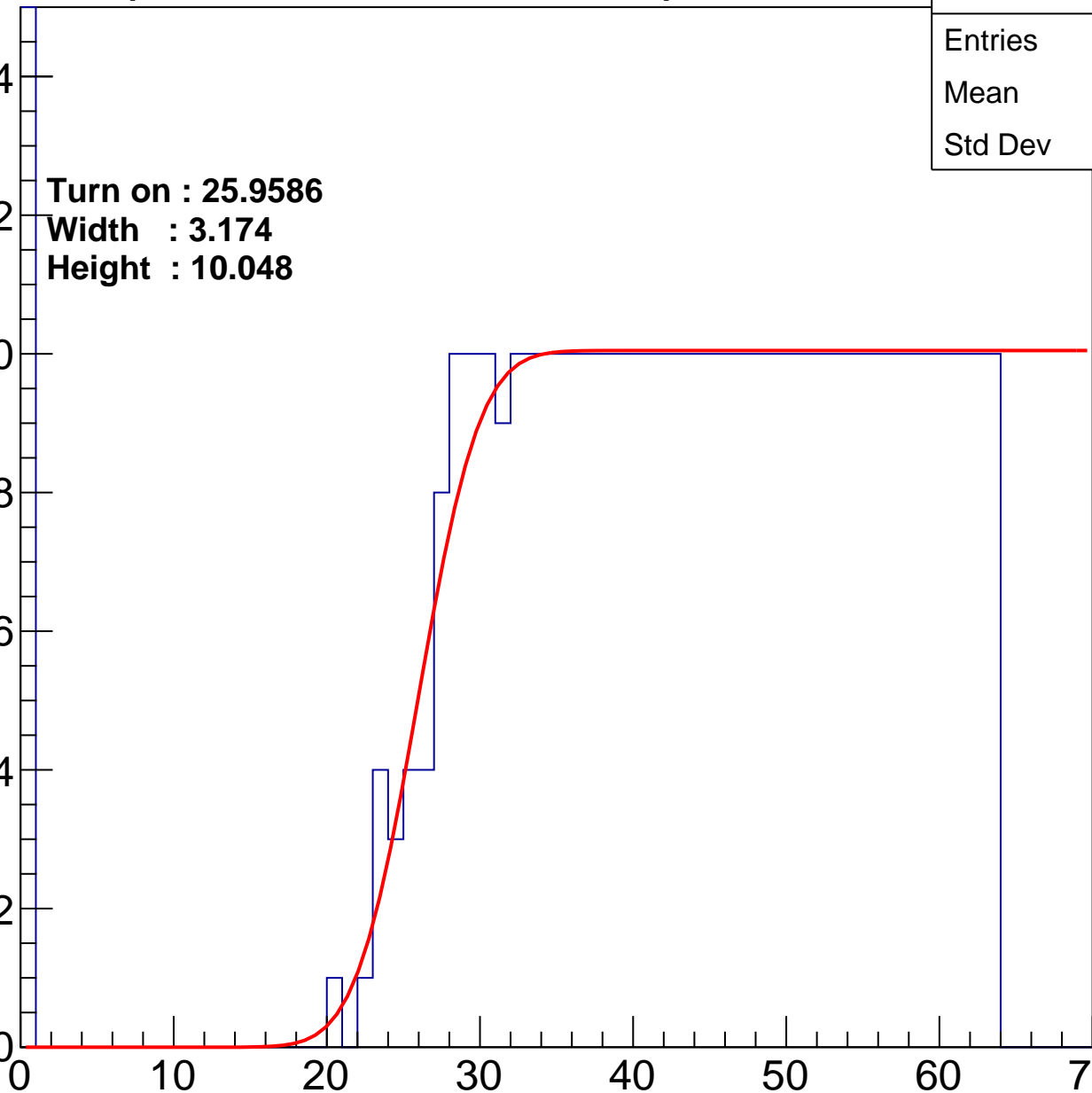
Width : 3.174

Height : 10.048

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch5

calib_packv5_041523_1651.root, FC#0, port C2

Entries	408
Mean	40.97
Std Dev	16.21

Turn on : 25.9112

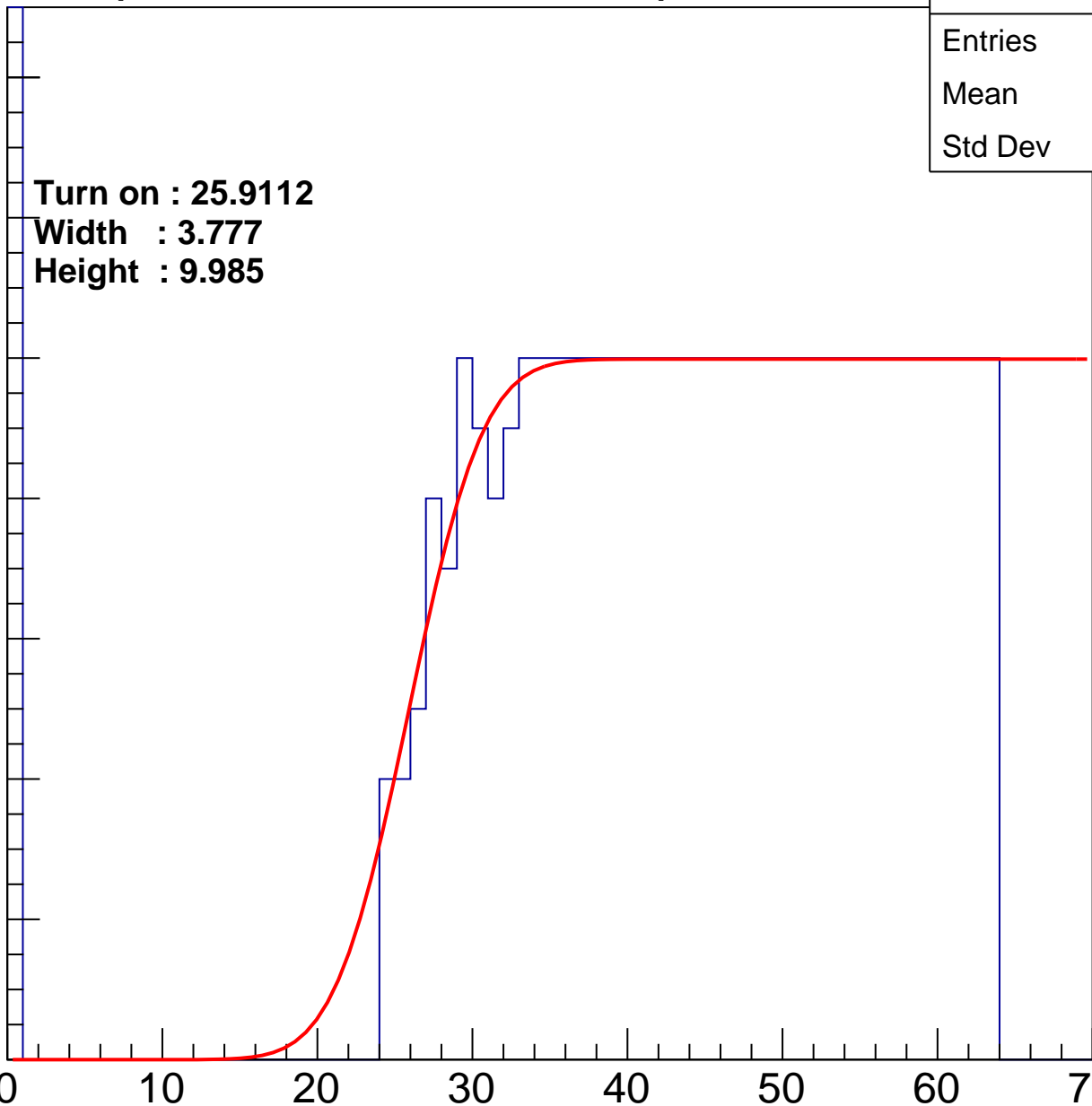
Width : 3.777

Height : 9.985

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch6

calib_packv5_041523_1651.root, FC#0, port C2

Entries	452
Mean	37.74
Std Dev	18.62

Turn on : 25.1869

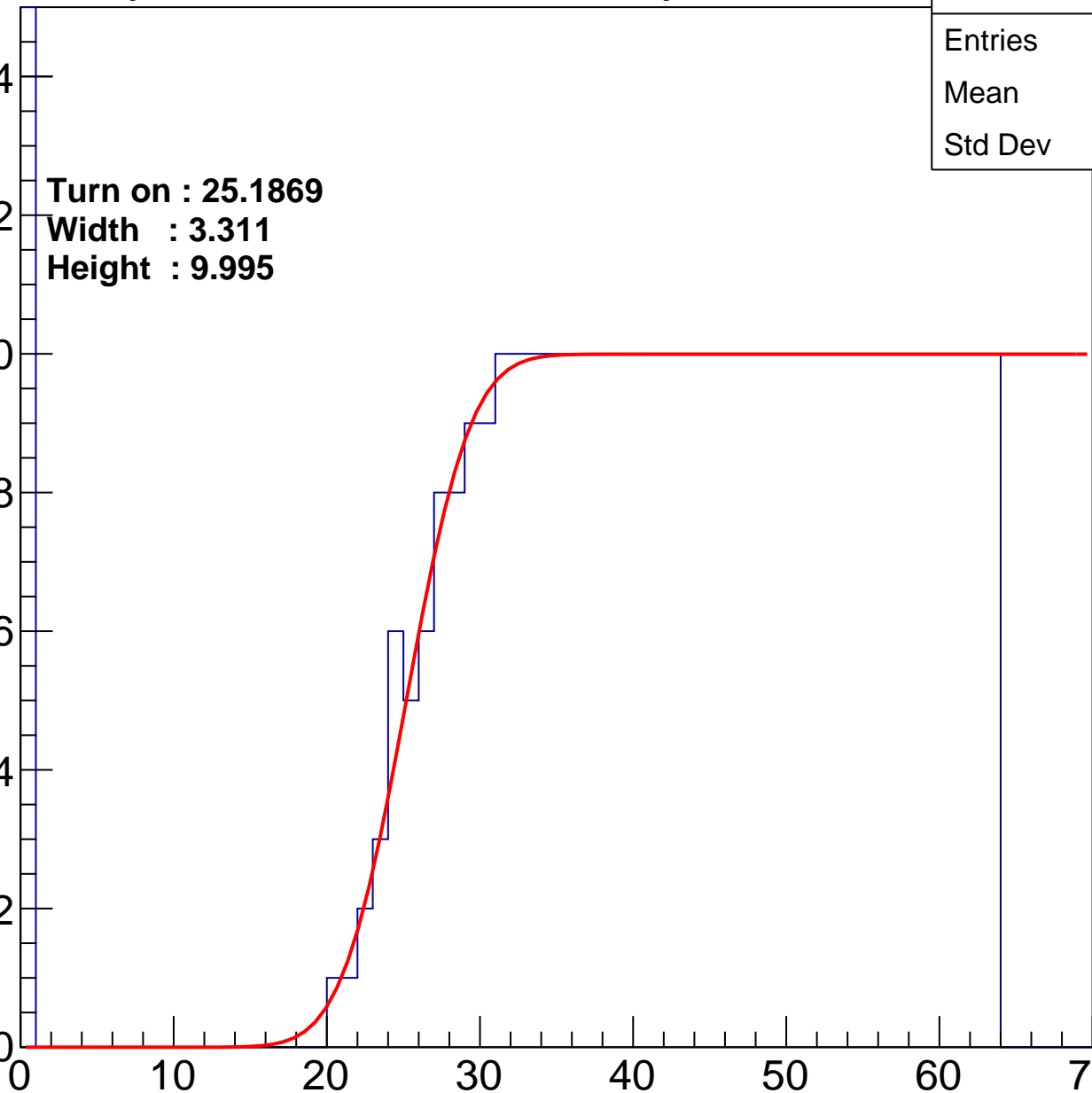
Width : 3.311

Height : 9.995

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	418
Mean	39.49
Std Dev	17.91

Turn on : 27.5458

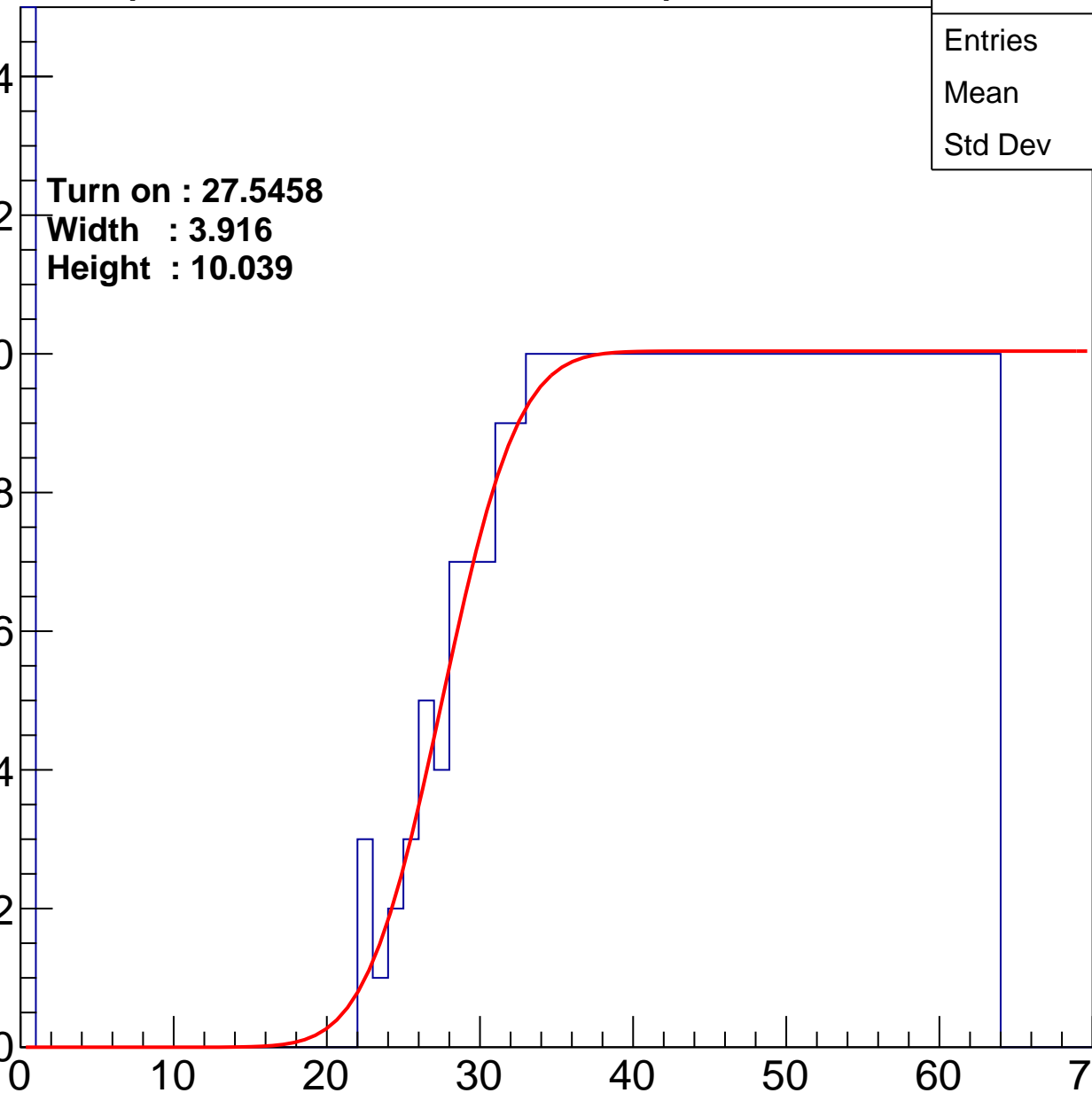
Width : 3.916

Height : 10.039

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch8

calib_packv5_041523_1651.root, FC#0, port C2

Entries	423
Mean	40.05
Std Dev	16.8

Turn on : 26.1557

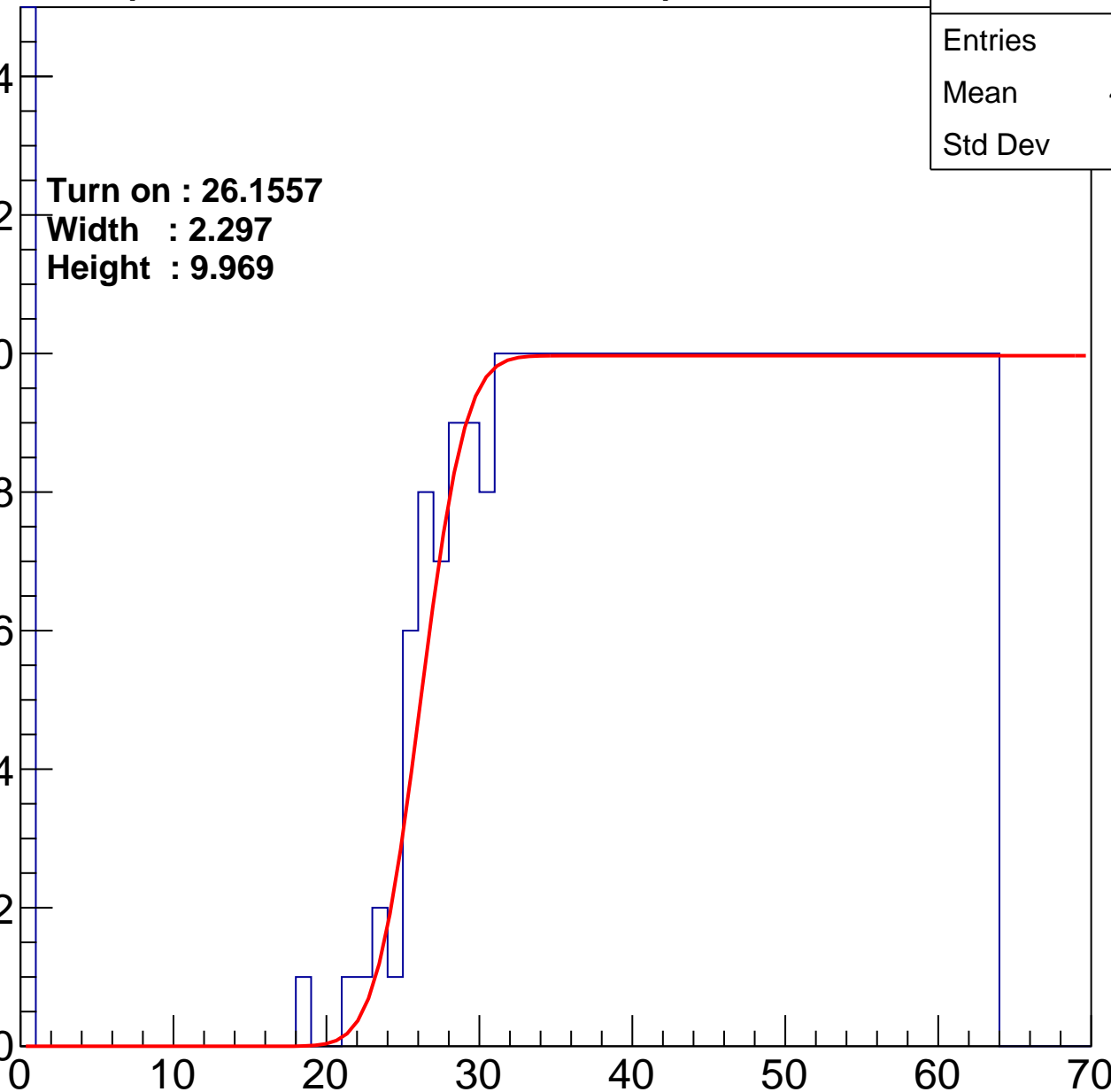
Width : 2.297

Height : 9.969

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch9

calib_packv5_041523_1651.root, FC#0, port C2

Entries	413
Mean	40.02
Std Dev	17.43

Turn on : 27.3985

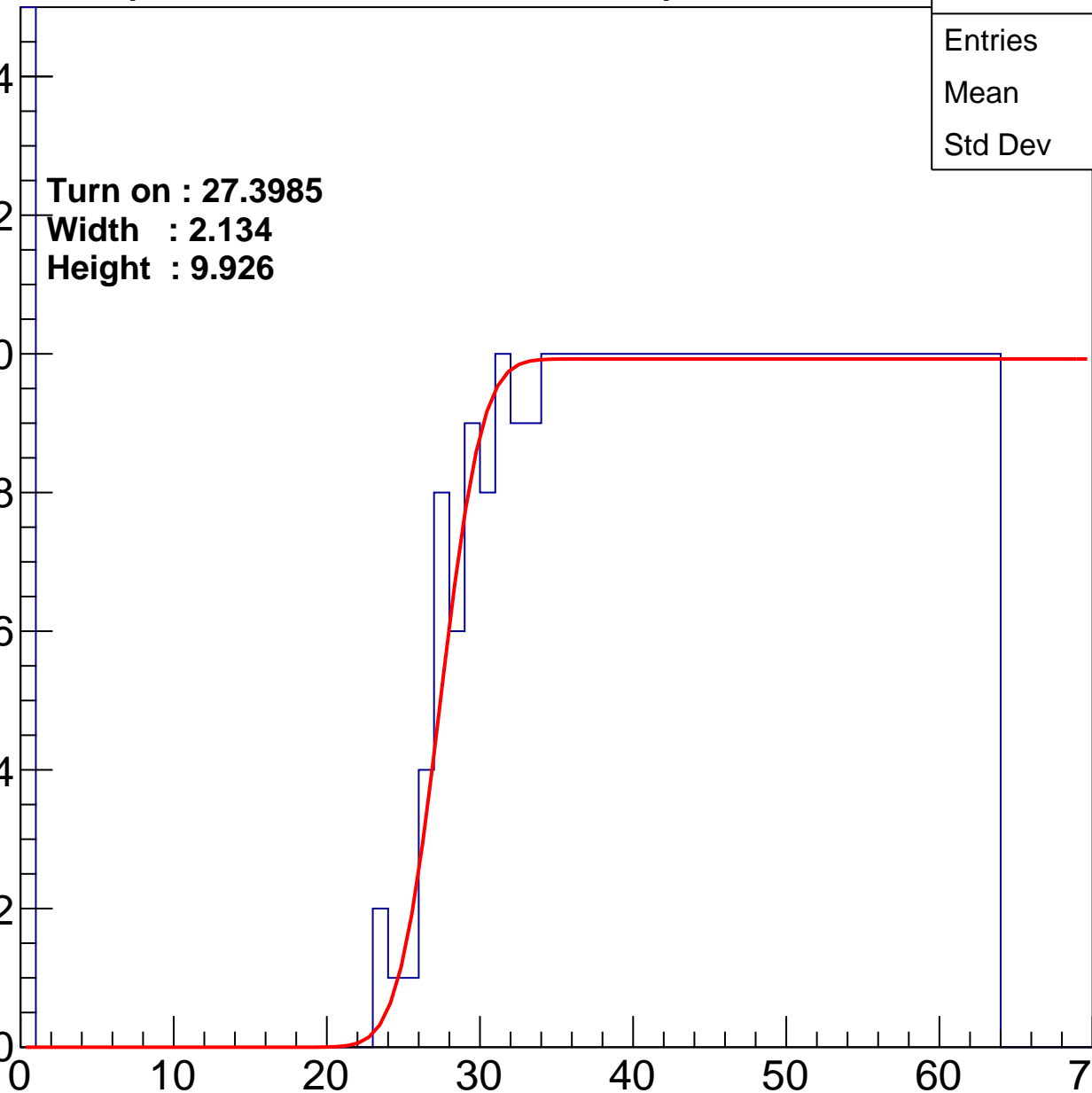
Width : 2.134

Height : 9.926

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch10

calib_packv5_041523_1651.root, FC#0, port C2

Entries	405
Mean	40.65
Std Dev	16.9

Turn on : 27.6289

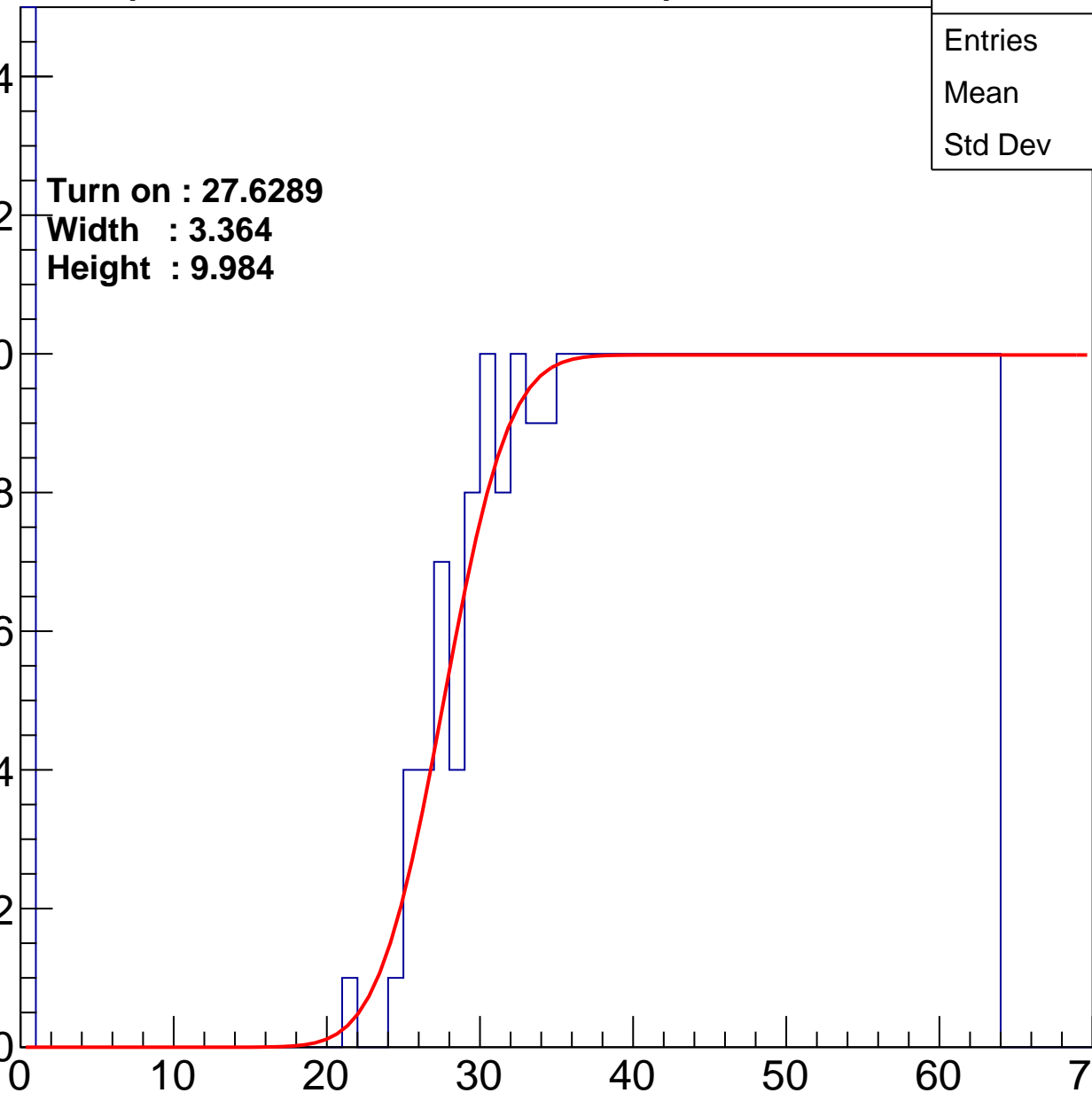
Width : 3.364

Height : 9.984

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch11

calib_packv5_041523_1651.root, FC#0, port C2

Entries	411
Mean	40.26
Std Dev	17.17

Turn on : 27.7340

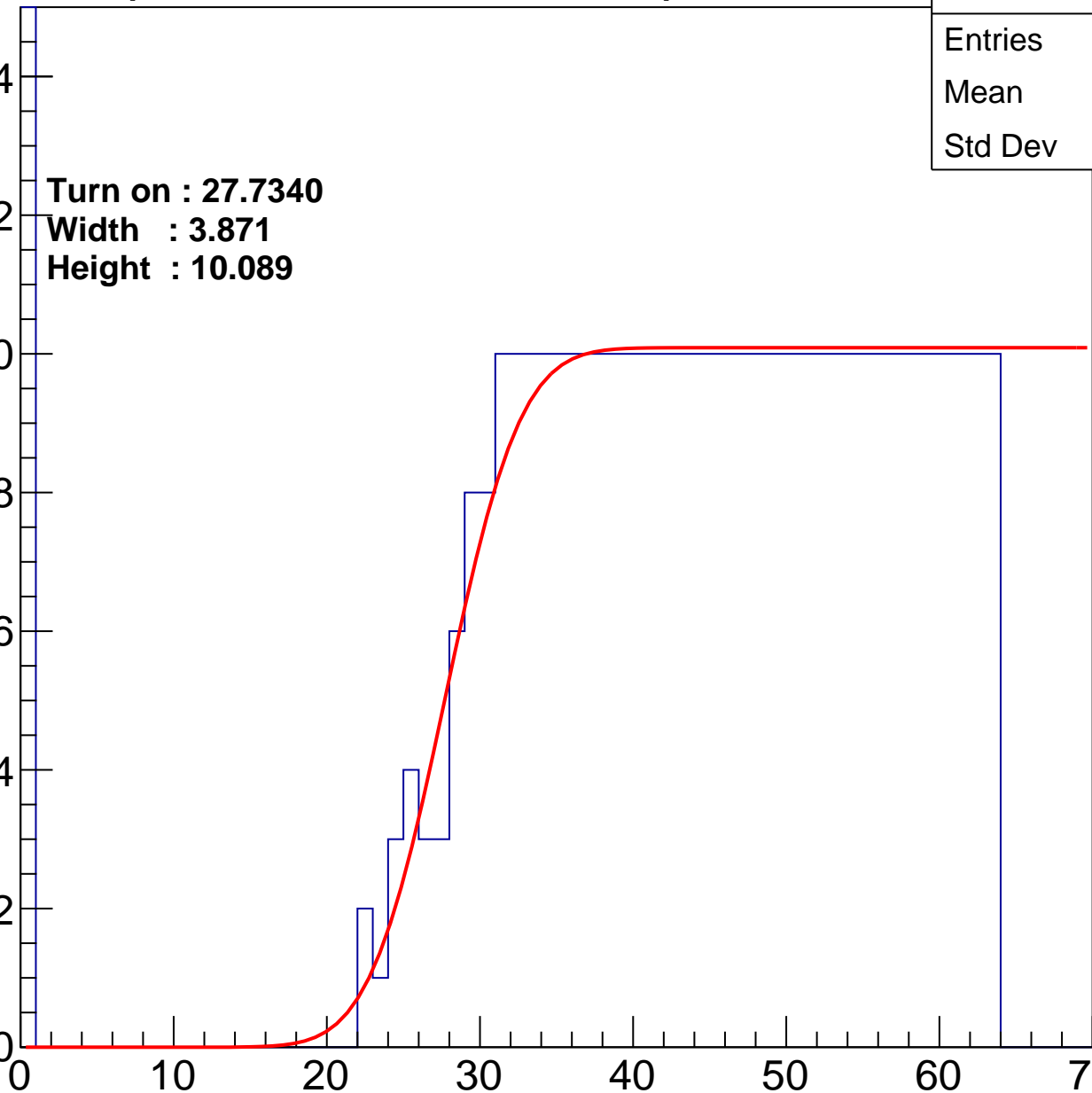
Width : 3.871

Height : 10.089

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch12

calib_packv5_041523_1651.root, FC#0, port C2

Entries	409
Mean	40.77
Std Dev	16.51

Turn on : 26.7622

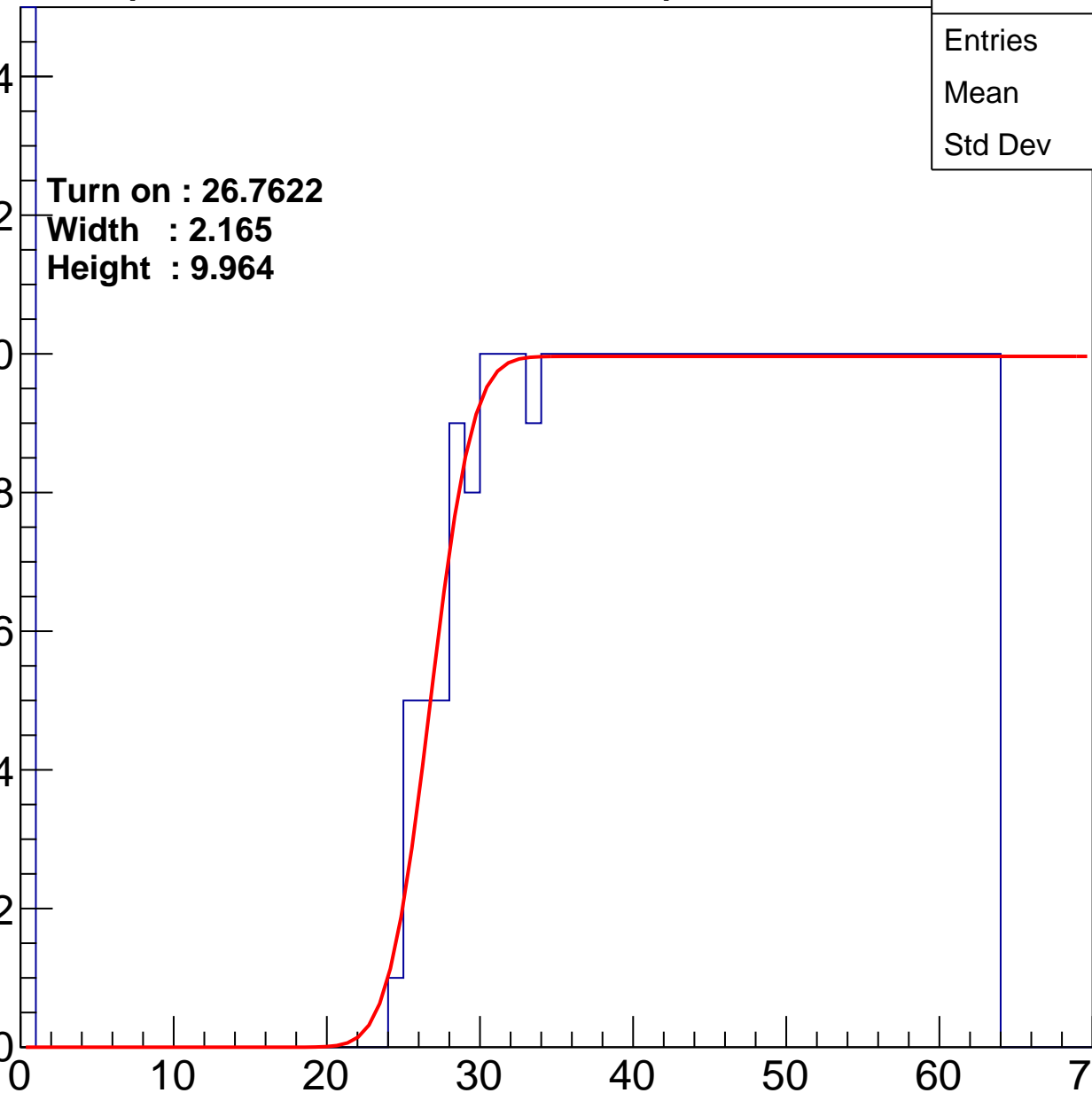
Width : 2.165

Height : 9.964

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch13

calib_packv5_041523_1651.root, FC#0, port C2

Entries	419
Mean	39.96
Std Dev	17.19

Turn on : 26.9753

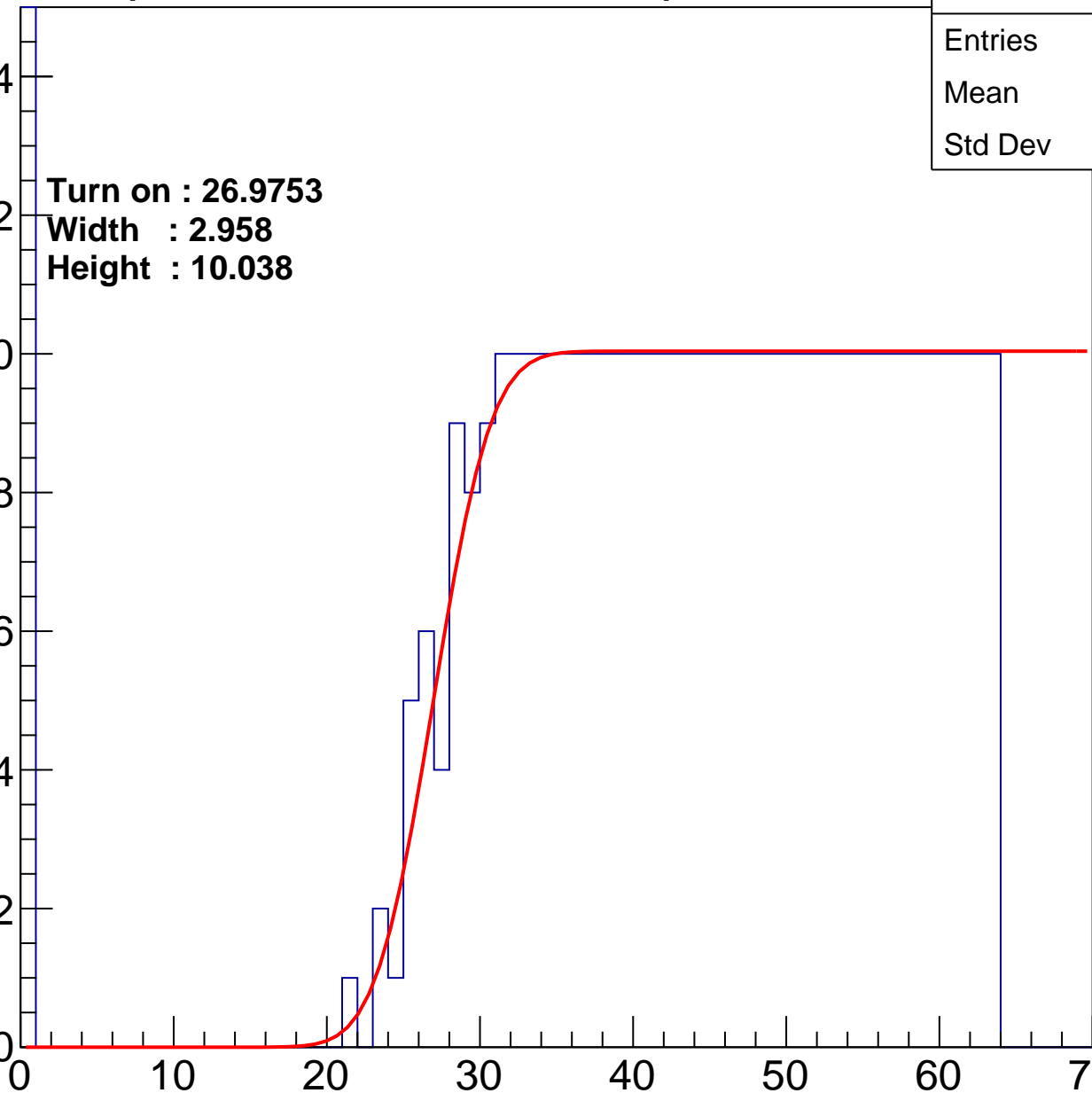
Width : 2.958

Height : 10.038

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch14

calib_packv5_041523_1651.root, FC#0, port C2

Entries	405
Mean	40.1
Std Dev	17.74

Turn on : 28.5892

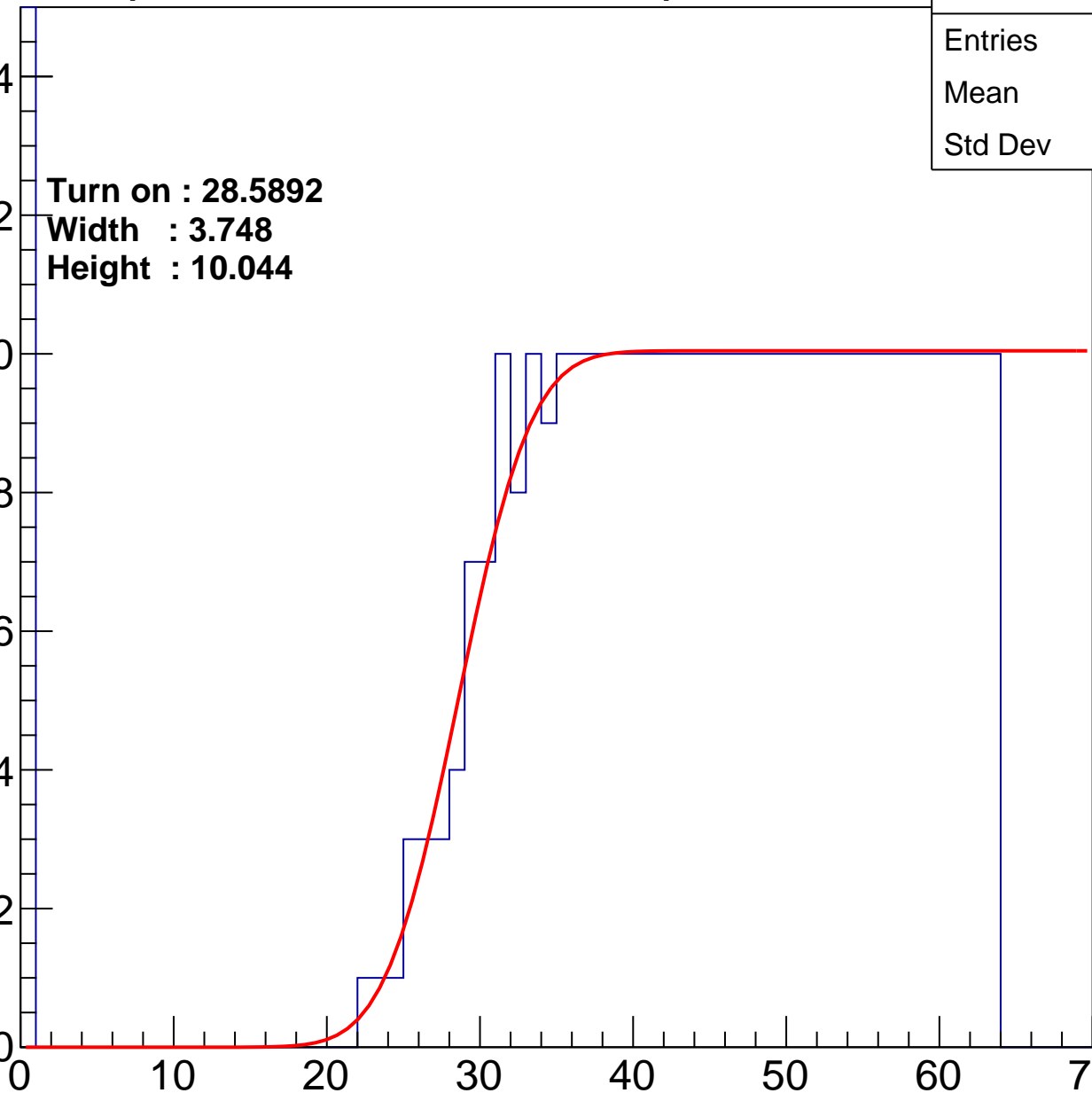
Width : 3.748

Height : 10.044

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch15

calib_packv5_041523_1651.root, FC#0, port C2

Entries	391
Mean	42.08
Std Dev	15.41

Turn on : 28.0074

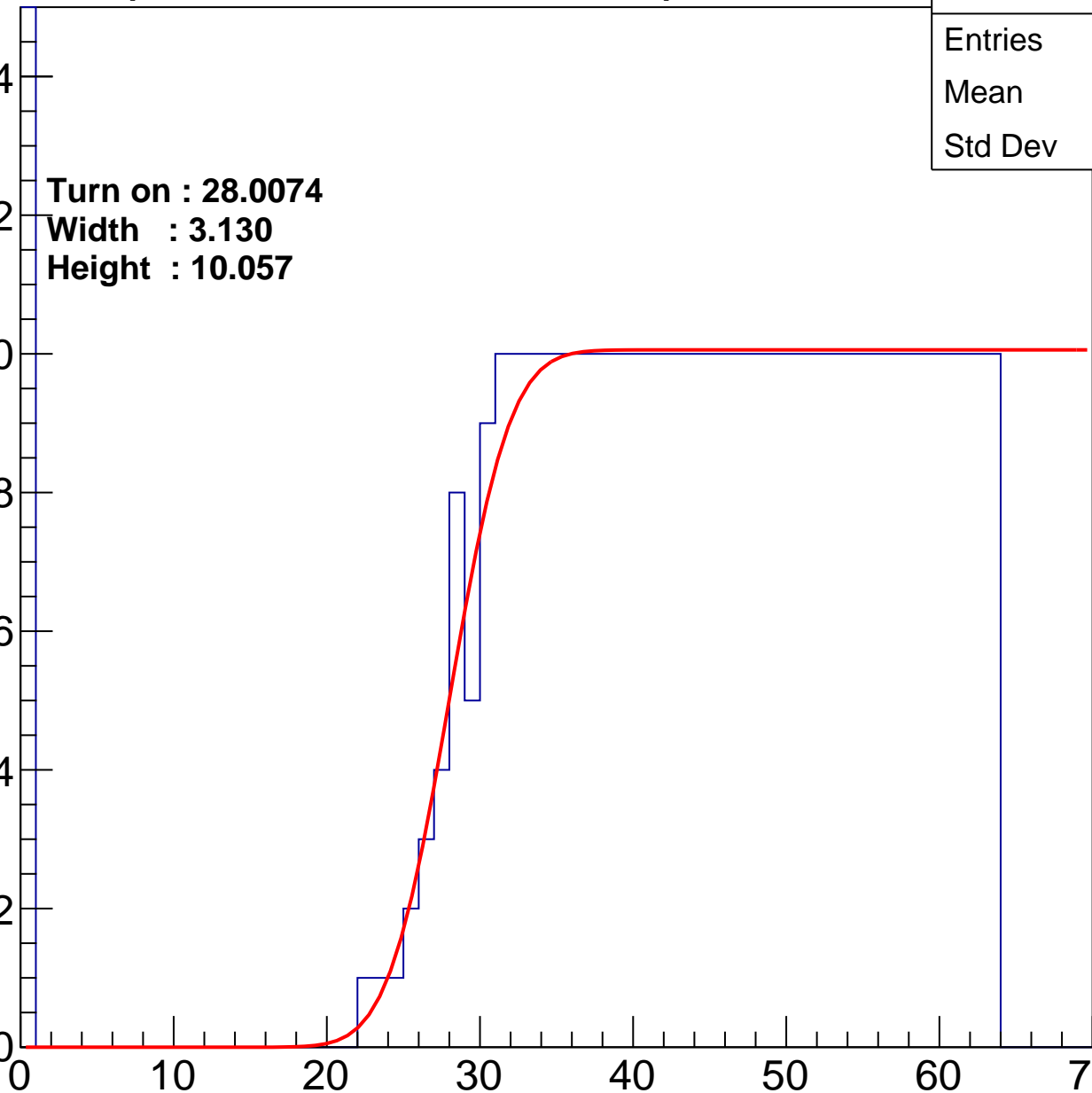
Width : 3.130

Height : 10.057

Entry

14
12
10
8
6
4
2
0

ampl

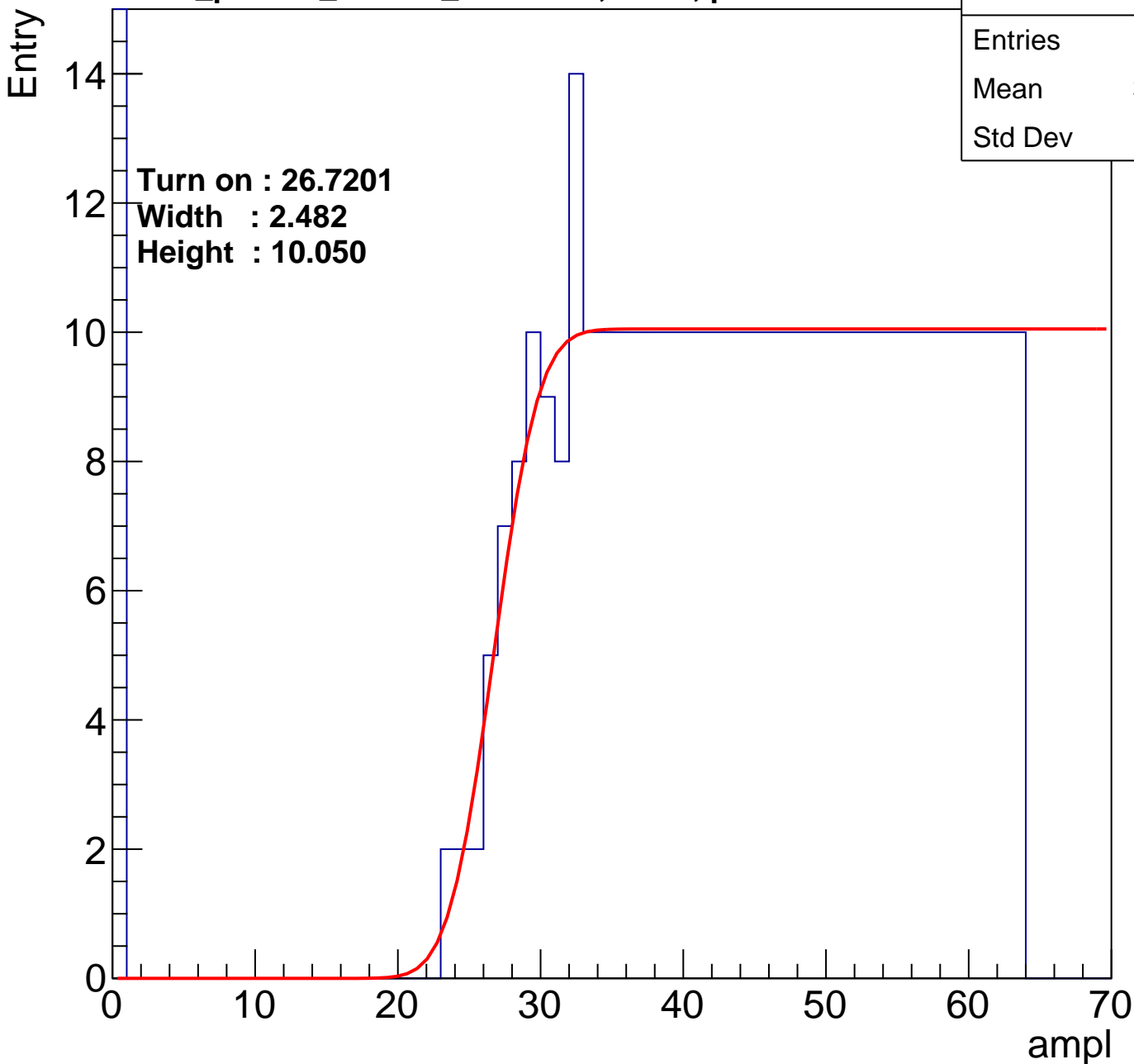


B1L103S, U12-ch16

calib_packv5_041523_1651.root, FC#0, port C2

Entries	429
Mean	39.21
Std Dev	17.81

Turn on : 26.7201
Width : 2.482
Height : 10.050



B1L103S, U12-ch17

calib_packv5_041523_1651.root, FC#0, port C2

Entries	399
Mean	41.08
Std Dev	16.6

Turn on : 27.7924

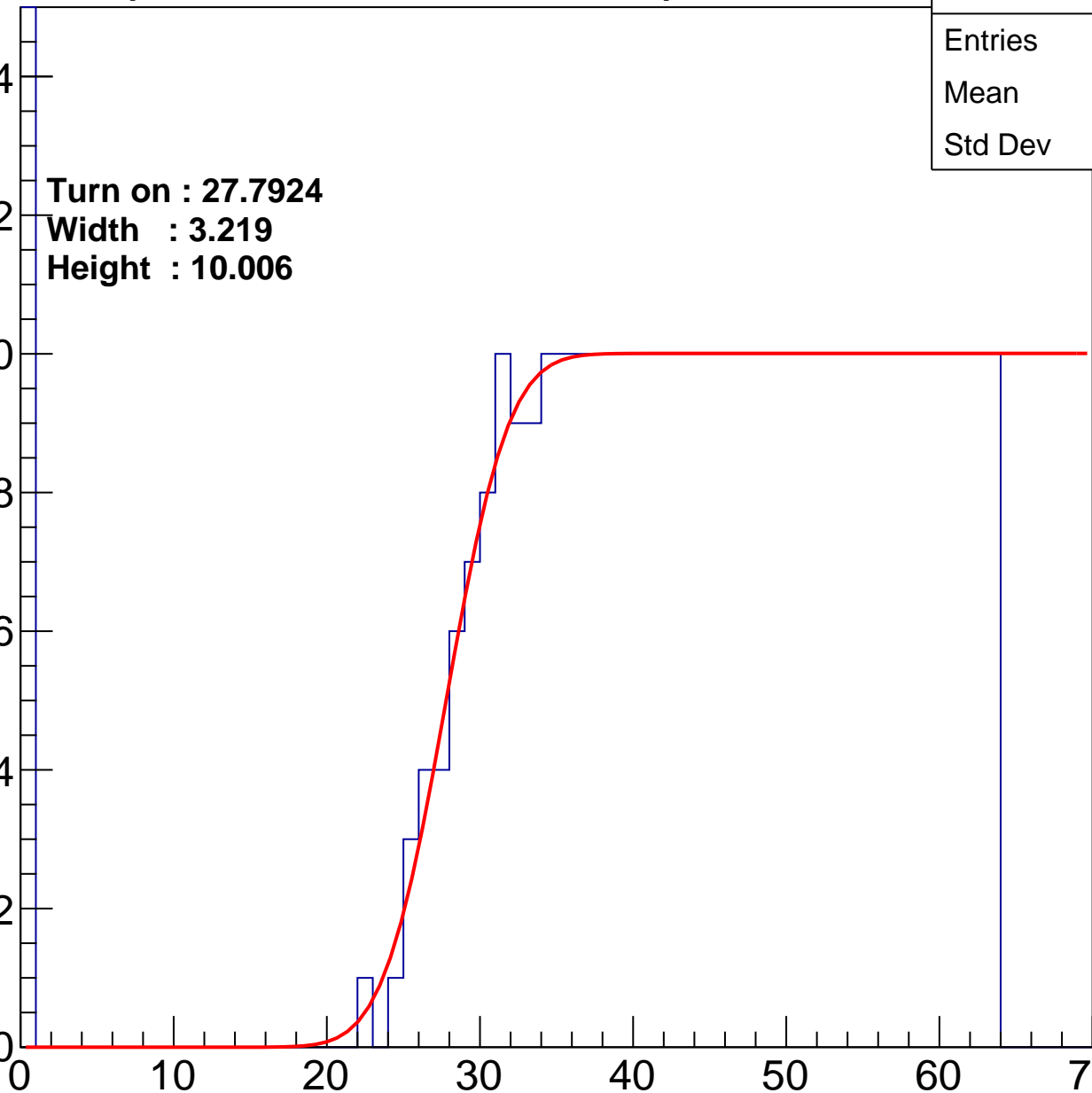
Width : 3.219

Height : 10.006

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch18

calib_packv5_041523_1651.root, FC#0, port C2

Entries	440
Mean	39.2
Std Dev	17.17

Turn on : 24.8774

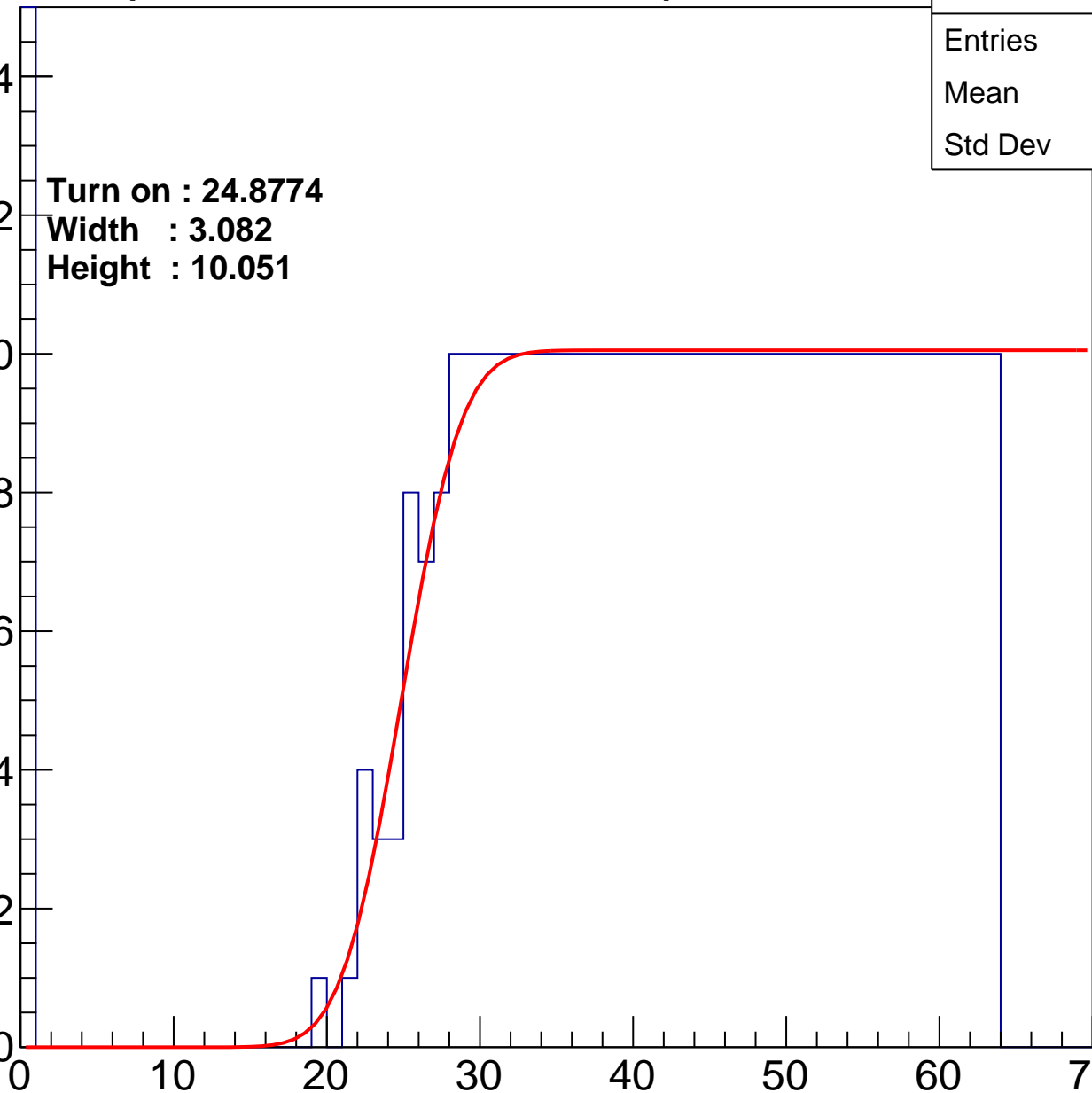
Width : 3.082

Height : 10.051

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch19

calib_packv5_041523_1651.root, FC#0, port C2

Entries	412
Mean	40.24
Std Dev	17.15

Turn on : 26.8173

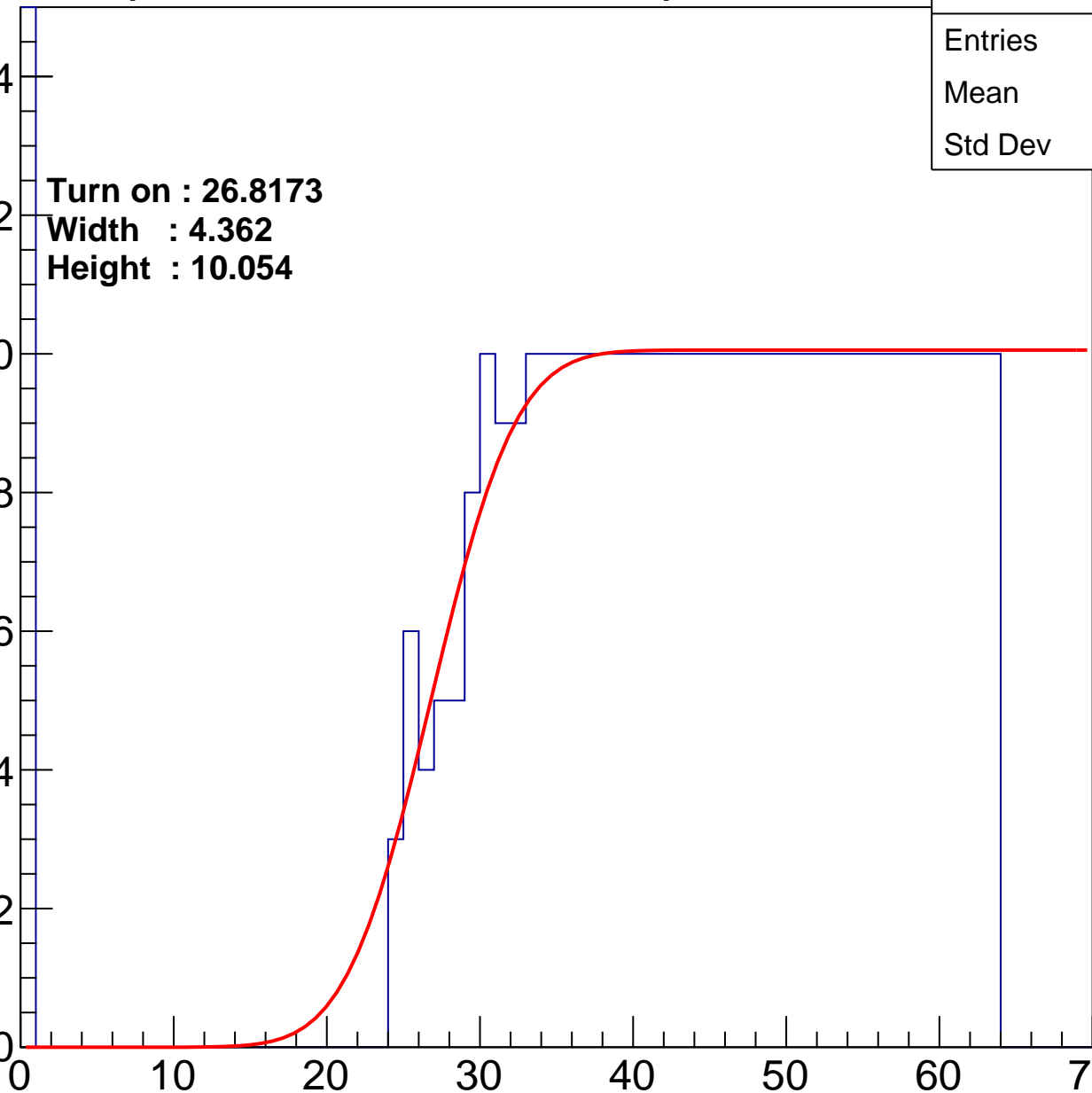
Width : 4.362

Height : 10.054

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch20

calib_packv5_041523_1651.root, FC#0, port C2

Entries	404
Mean	40.83
Std Dev	16.69

Turn on : 27.7245

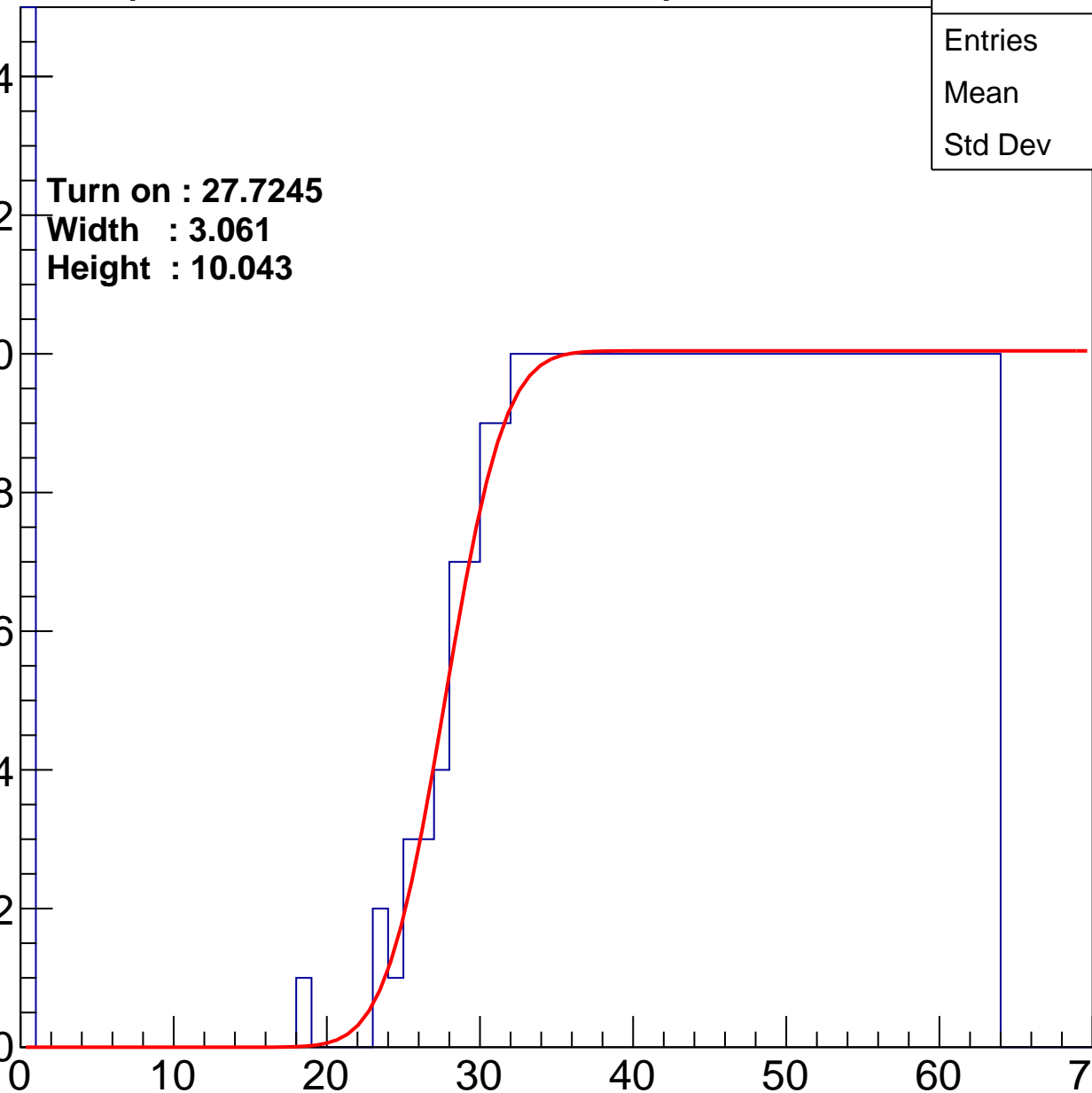
Width : 3.061

Height : 10.043

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch21

calib_packv5_041523_1651.root, FC#0, port C2

Entries	397
Mean	41.31
Std Dev	16.36

Turn on : 28.3956

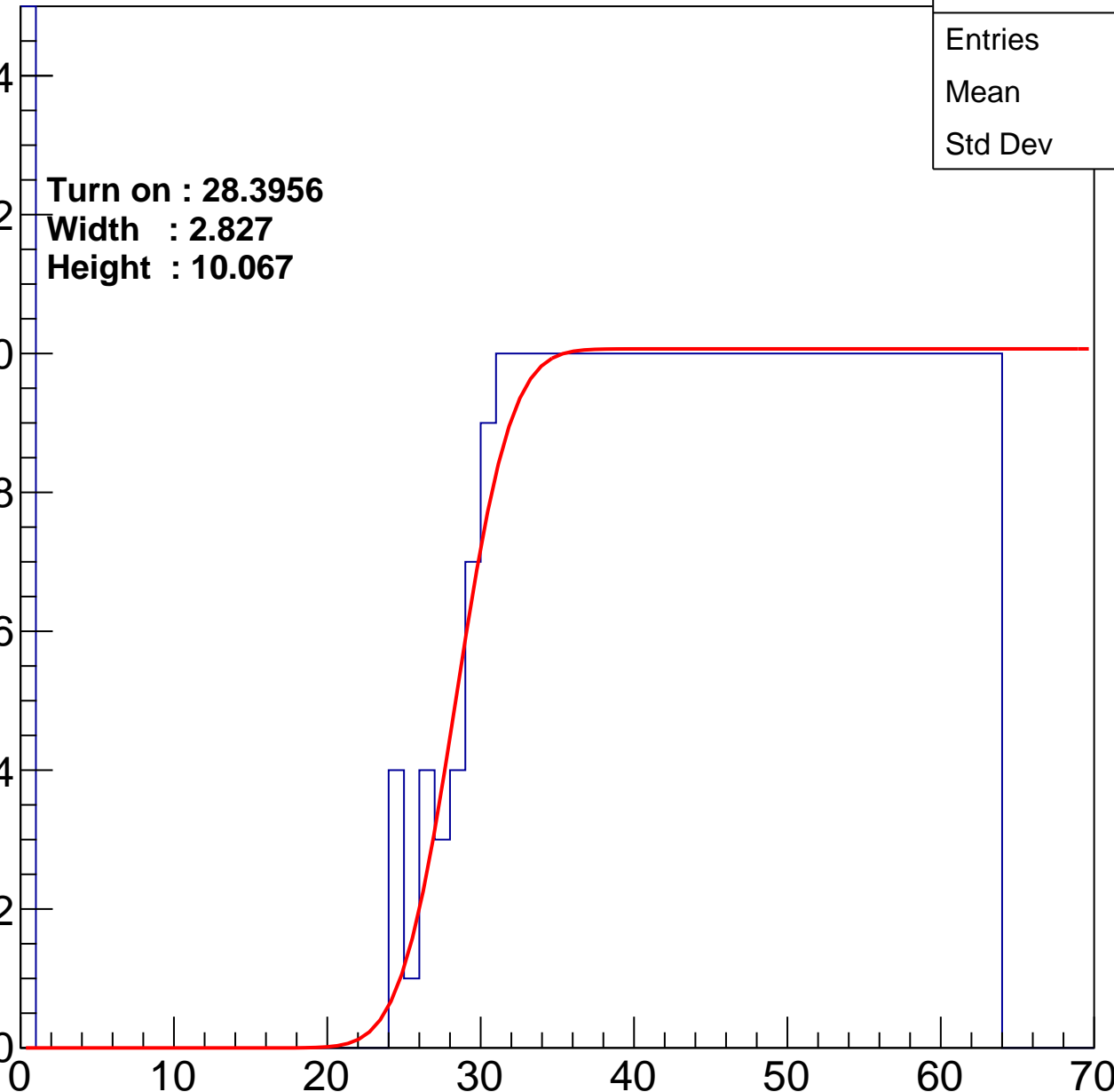
Width : 2.827

Height : 10.067

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch22

calib_packv5_041523_1651.root, FC#0, port C2

Entries	412
Mean	40.27
Std Dev	17.12

Turn on : 26.2952

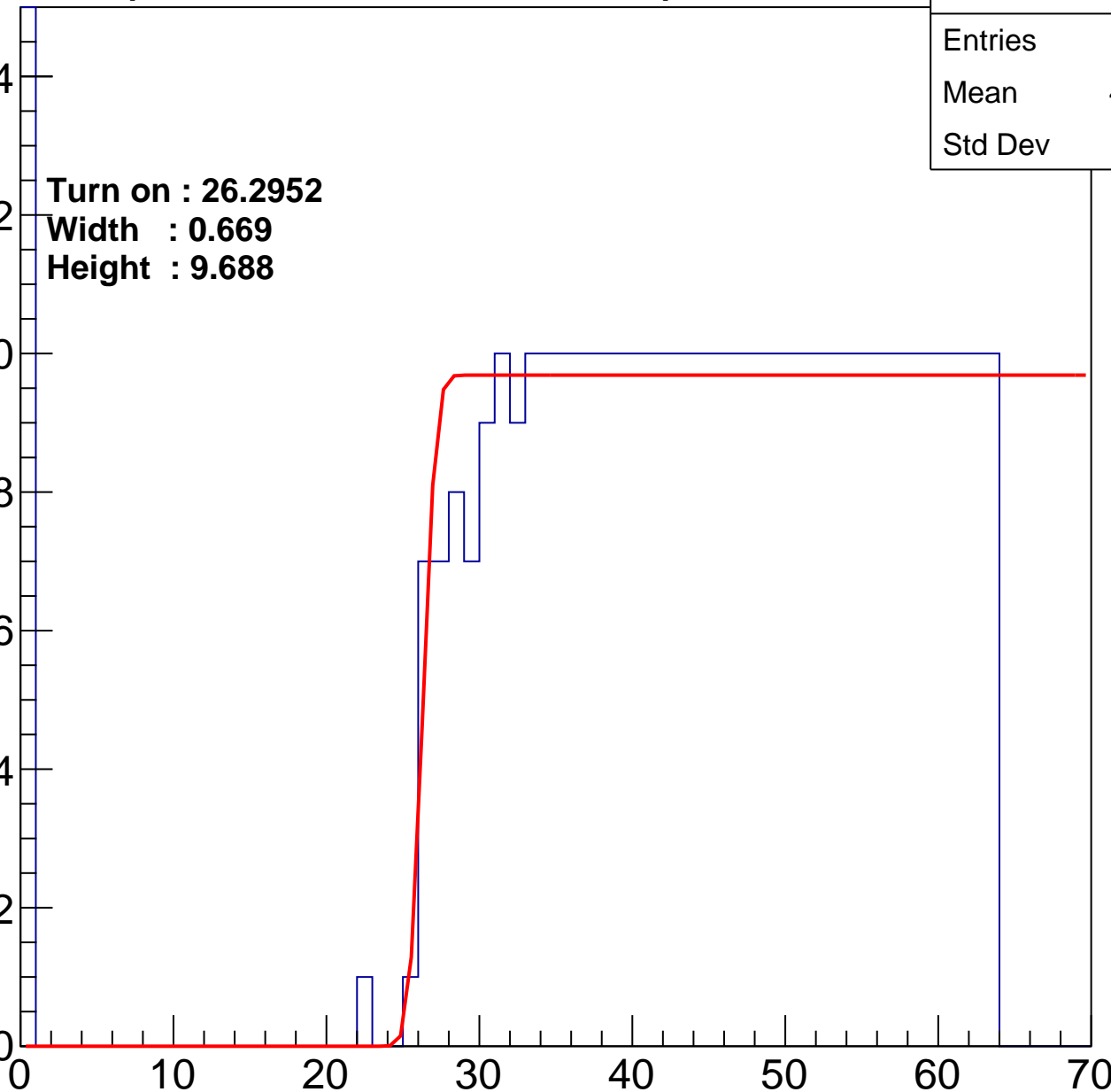
Width : 0.669

Height : 9.688

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch23

calib_packv5_041523_1651.root, FC#0, port C2

Entries	394
Mean	41.58
Std Dev	16.12

Turn on : 28.3805

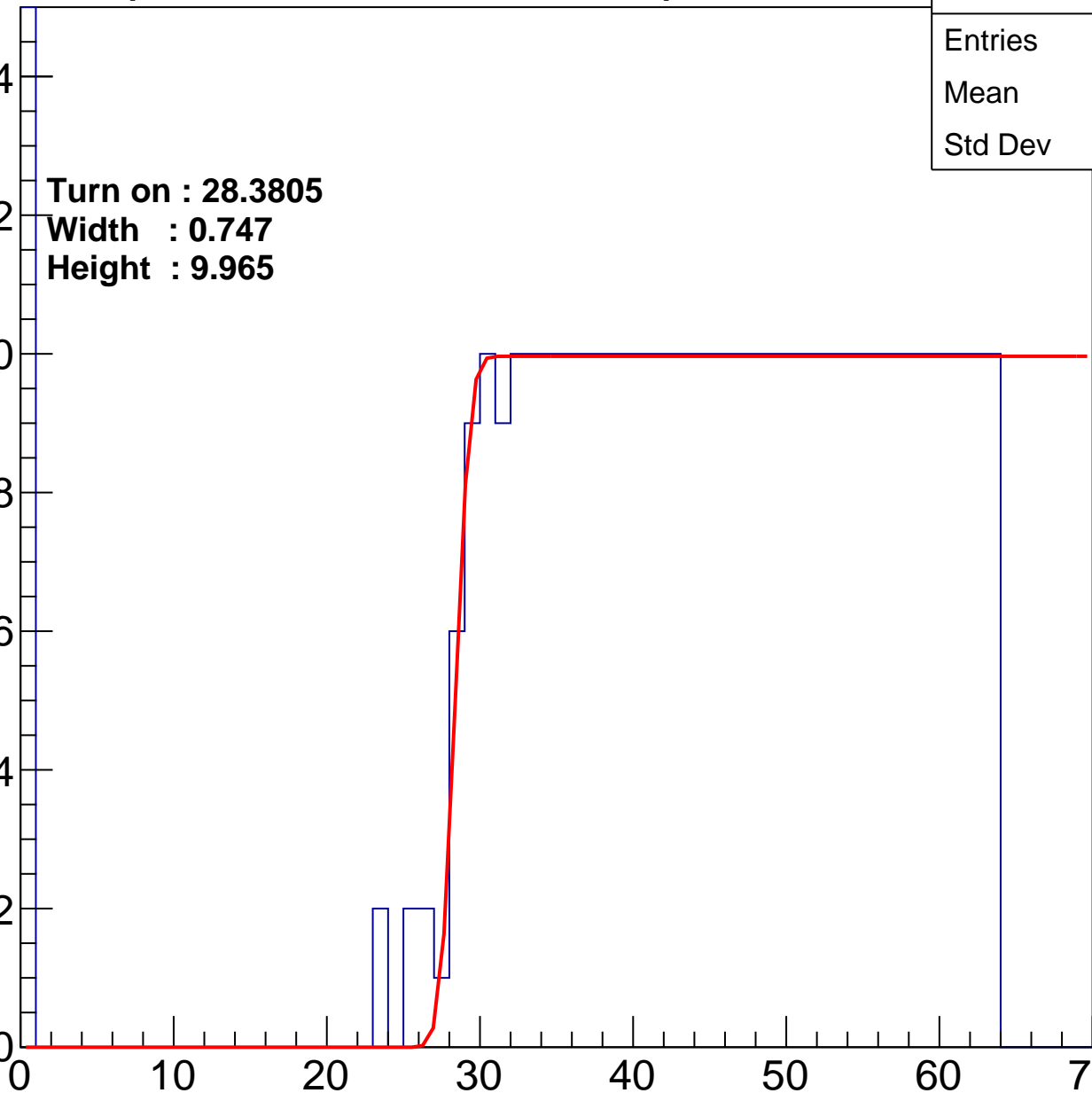
Width : 0.747

Height : 9.965

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch24

calib_packv5_041523_1651.root, FC#0, port C2

Entries	395
Mean	41.27
Std Dev	16.52

Turn on : 28.5449

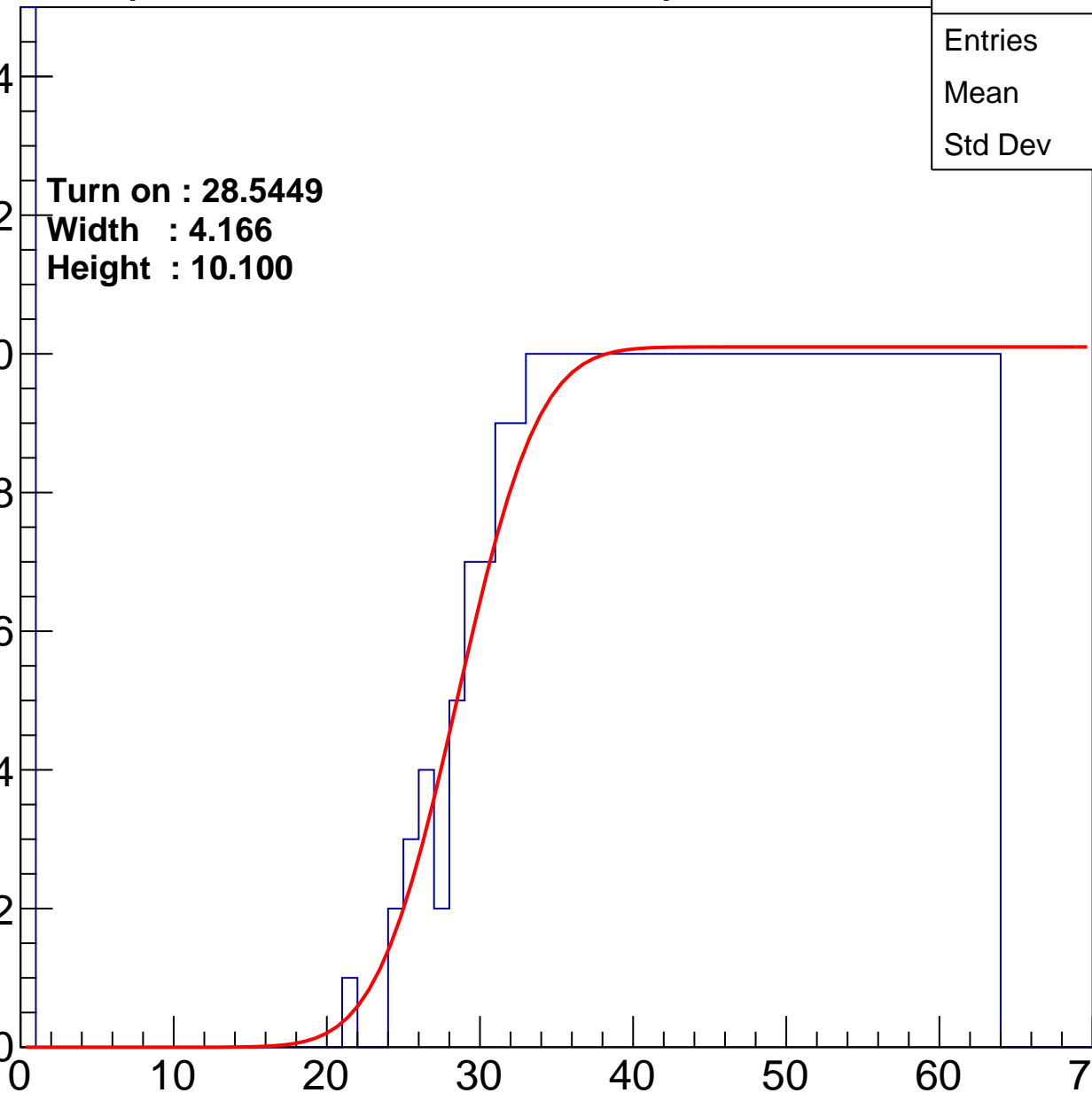
Width : 4.166

Height : 10.100

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch25

calib_packv5_041523_1651.root, FC#0, port C2

Entries	438
Mean	39.36
Std Dev	17.02

Turn on : 24.6322

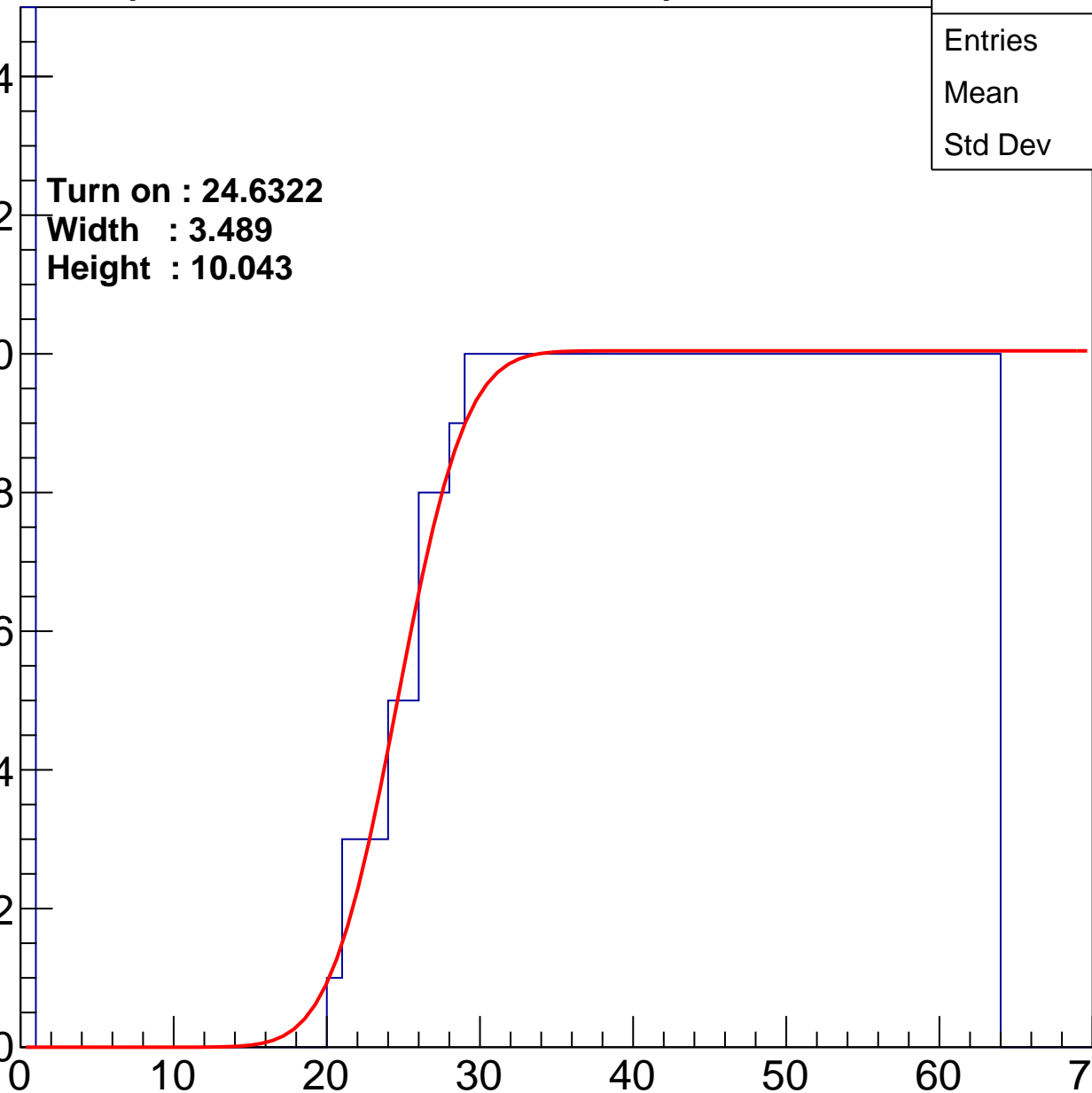
Width : 3.489

Height : 10.043

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch26

calib_packv5_041523_1651.root, FC#0, port C2

Entries	417
Mean	40.88
Std Dev	15.77

Turn on : 25.8181

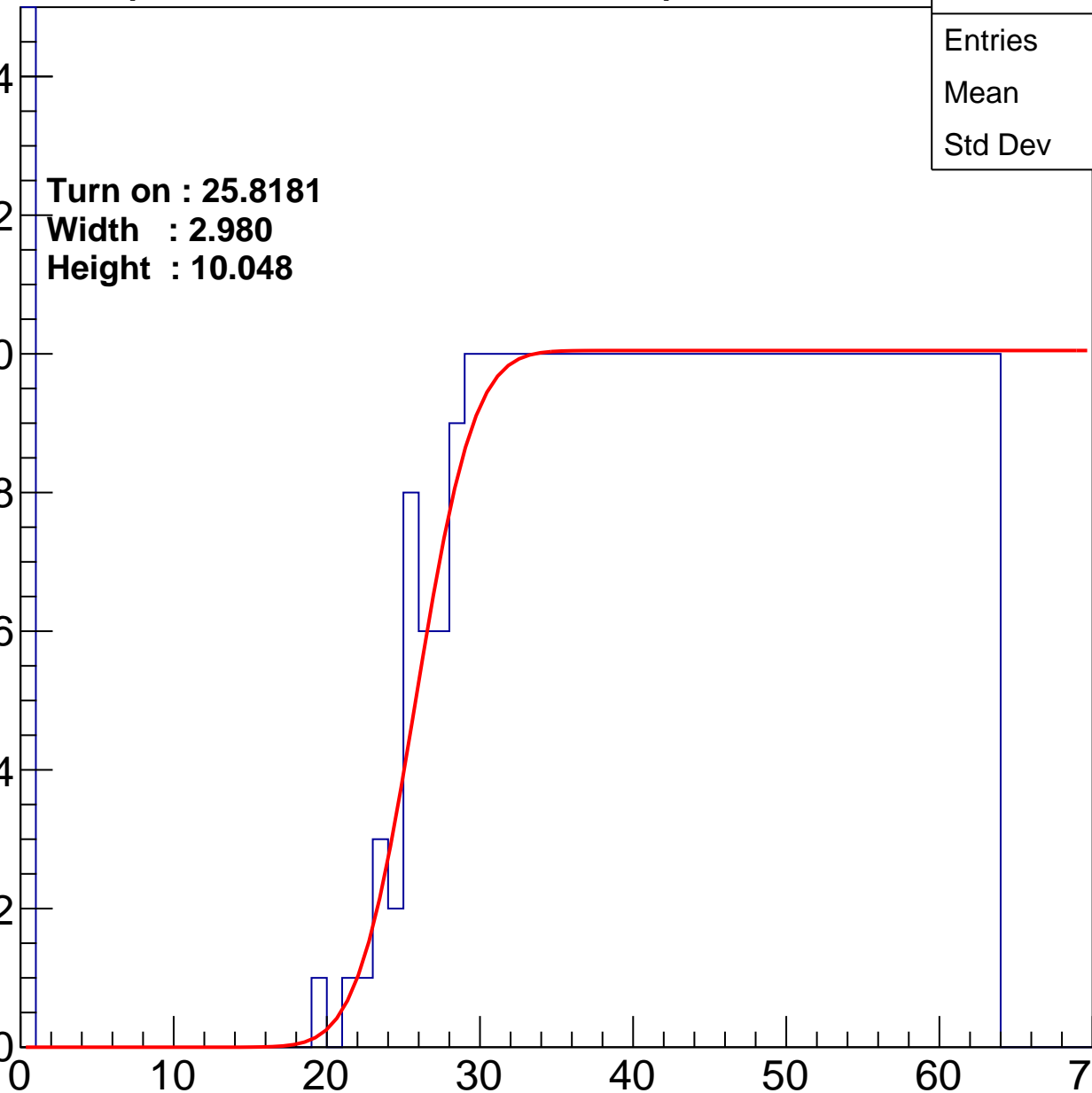
Width : 2.980

Height : 10.048

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch27

calib_packv5_041523_1651.root, FC#0, port C2

Entries	424
Mean	39.58
Std Dev	17.47

Turn on : 26.8917

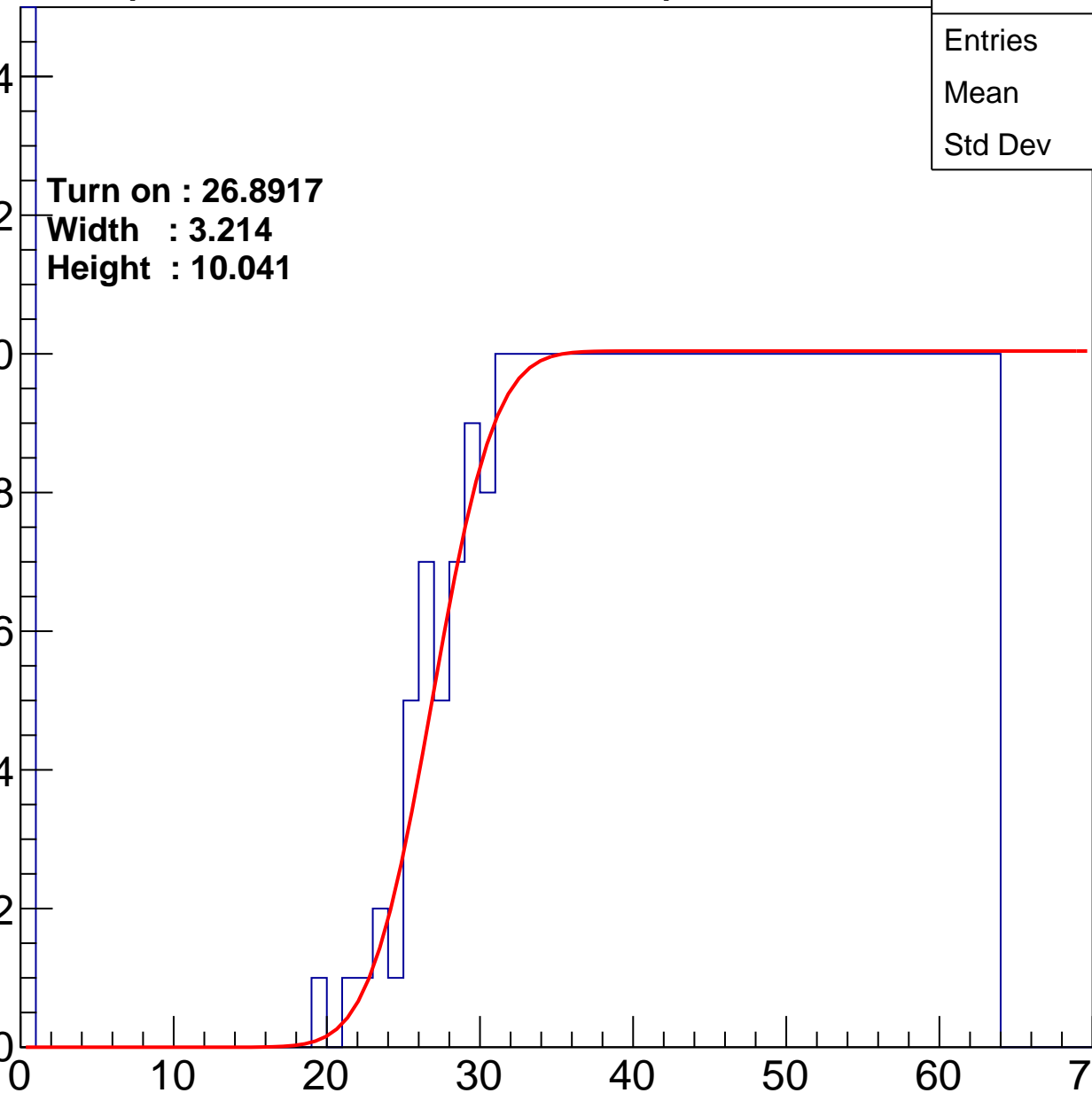
Width : 3.214

Height : 10.041

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch28

calib_packv5_041523_1651.root, FC#0, port C2

Entries	402
Mean	40.96
Std Dev	16.6

Turn on : 27.9155

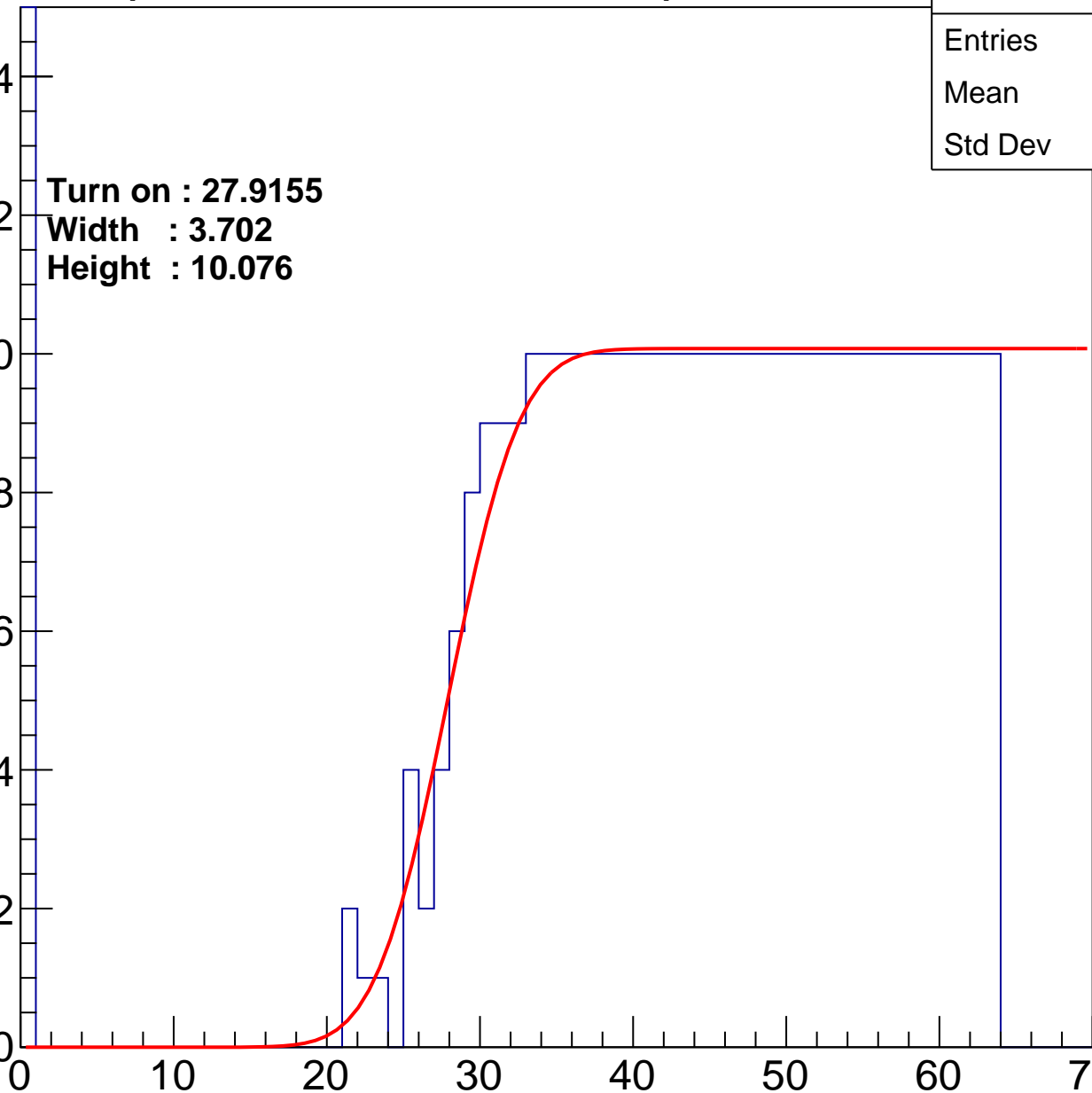
Width : 3.702

Height : 10.076

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch29

calib_packv5_041523_1651.root, FC#0, port C2

Entries	419
Mean	39.36
Std Dev	18.11

Turn on : 27.7297

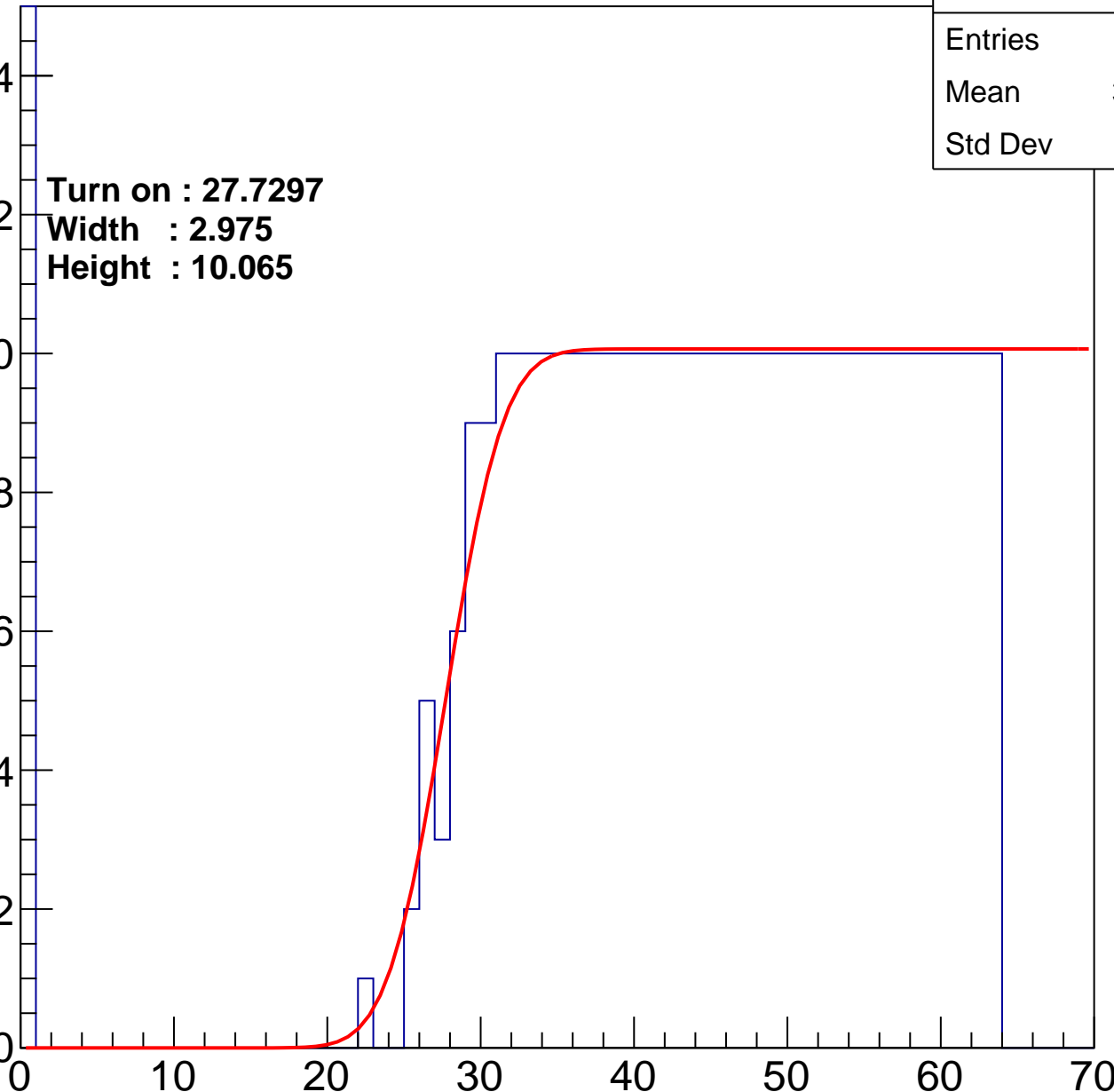
Width : 2.975

Height : 10.065

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch30

calib_packv5_041523_1651.root, FC#0, port C2

Entries	396
Mean	41.23
Std Dev	16.58

Turn on : 28.4595

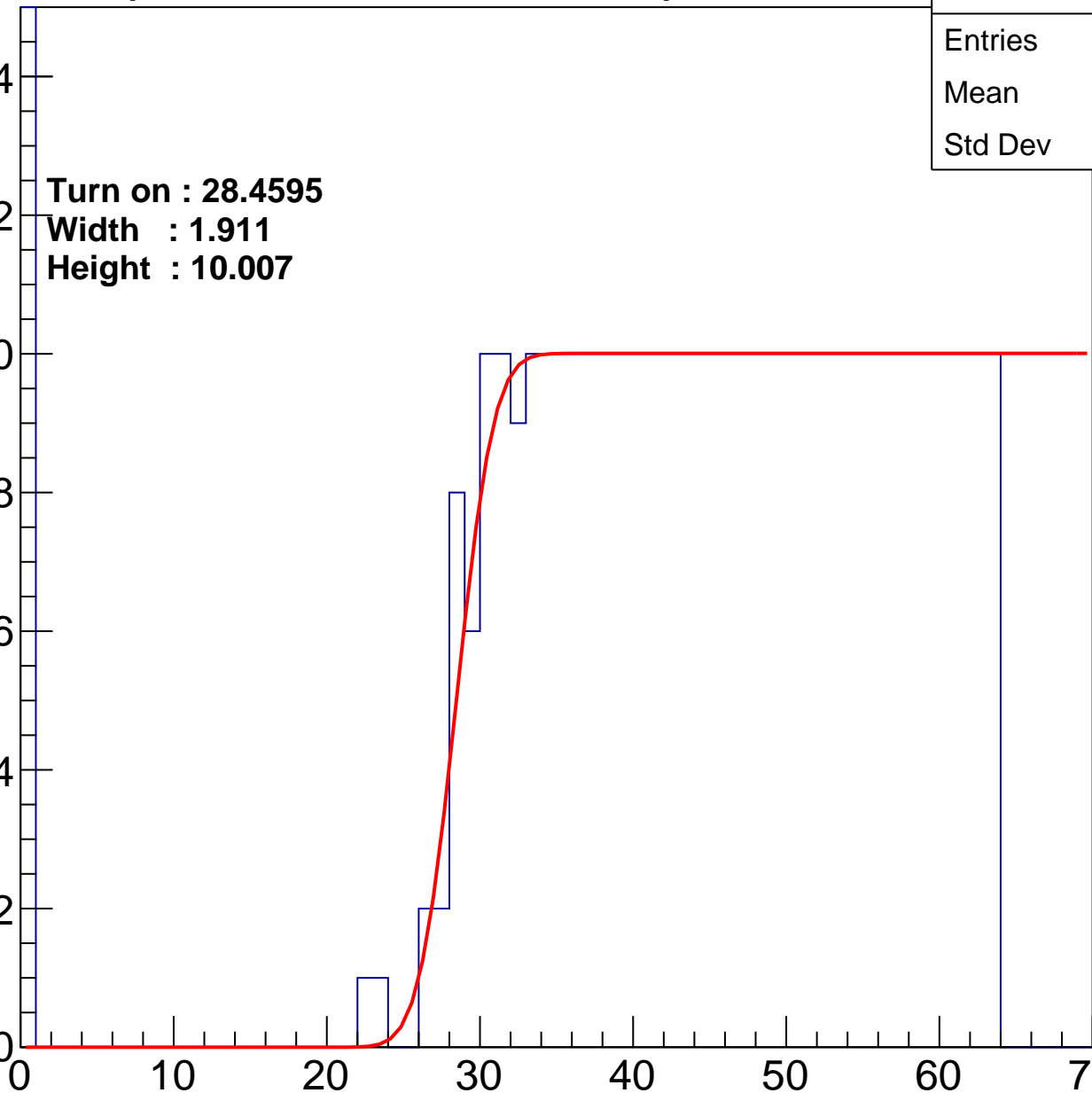
Width : 1.911

Height : 10.007

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch31

calib_packv5_041523_1651.root, FC#0, port C2

Entries	393
Mean	41.73
Std Dev	15.9

Turn on : 28.1713

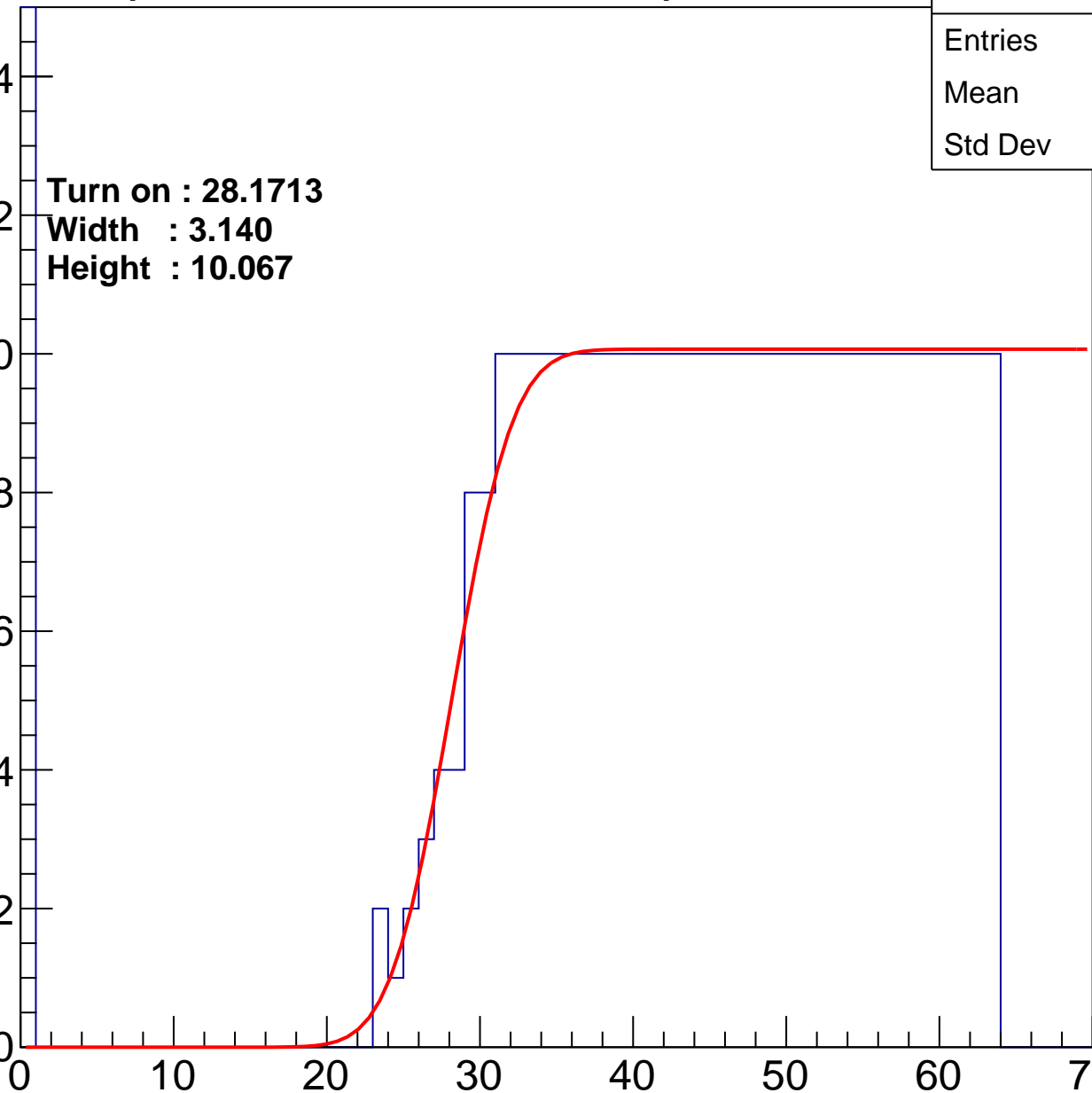
Width : 3.140

Height : 10.067

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch32

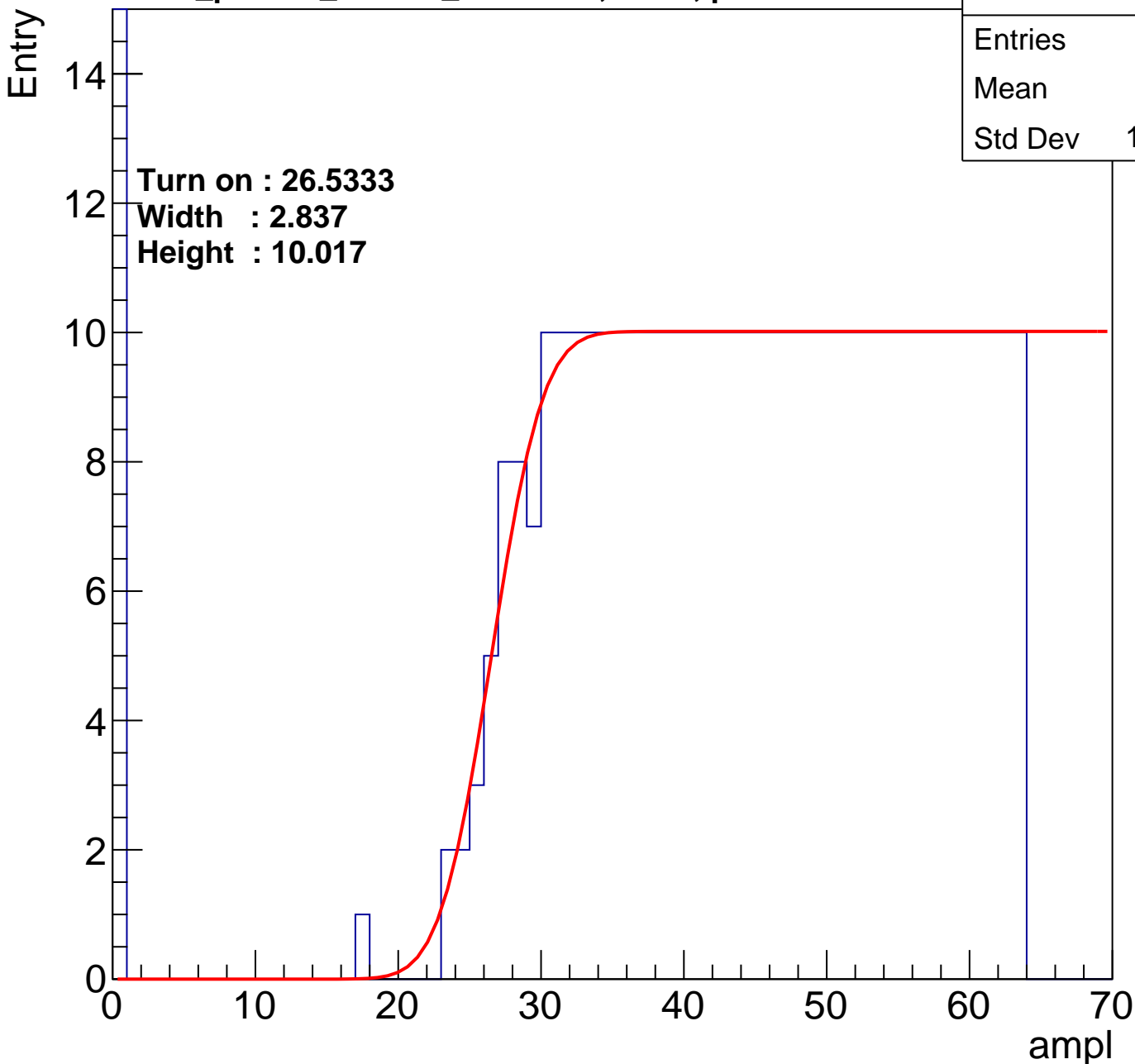
calib_packv5_041523_1651.root, FC#0, port C2

Entries	411
Mean	40.8
Std Dev	16.32

Turn on : 26.5333

Width : 2.837

Height : 10.017



B1L103S, U12-ch33

calib_packv5_041523_1651.root, FC#0, port C2

Entries	394
Mean	41.54
Std Dev	16.16

Turn on : 28.2974

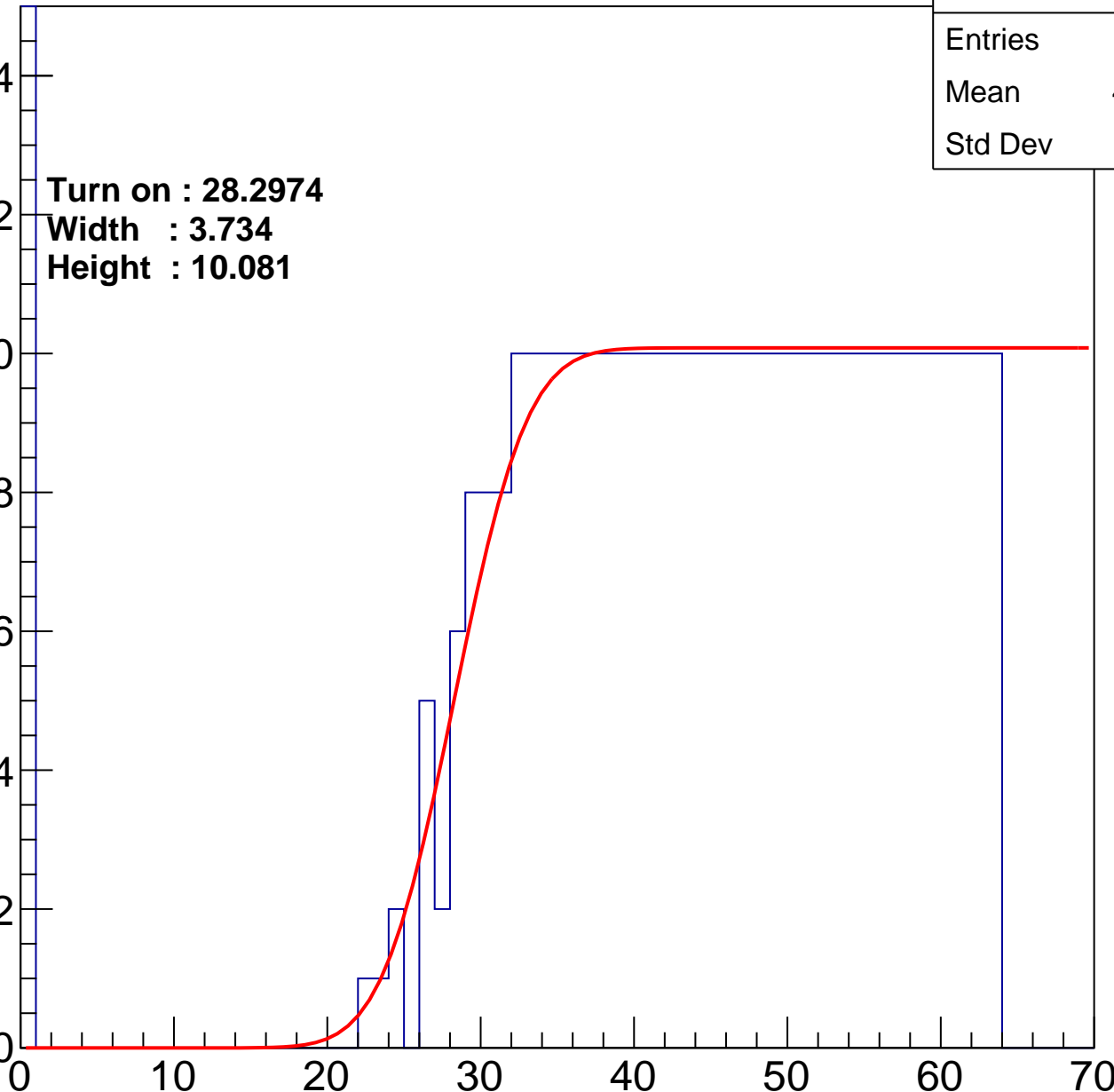
Width : 3.734

Height : 10.081

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch34

calib_packv5_041523_1651.root, FC#0, port C2

Entries	423
Mean	39.63
Std Dev	17.5

Turn on : 26.4131

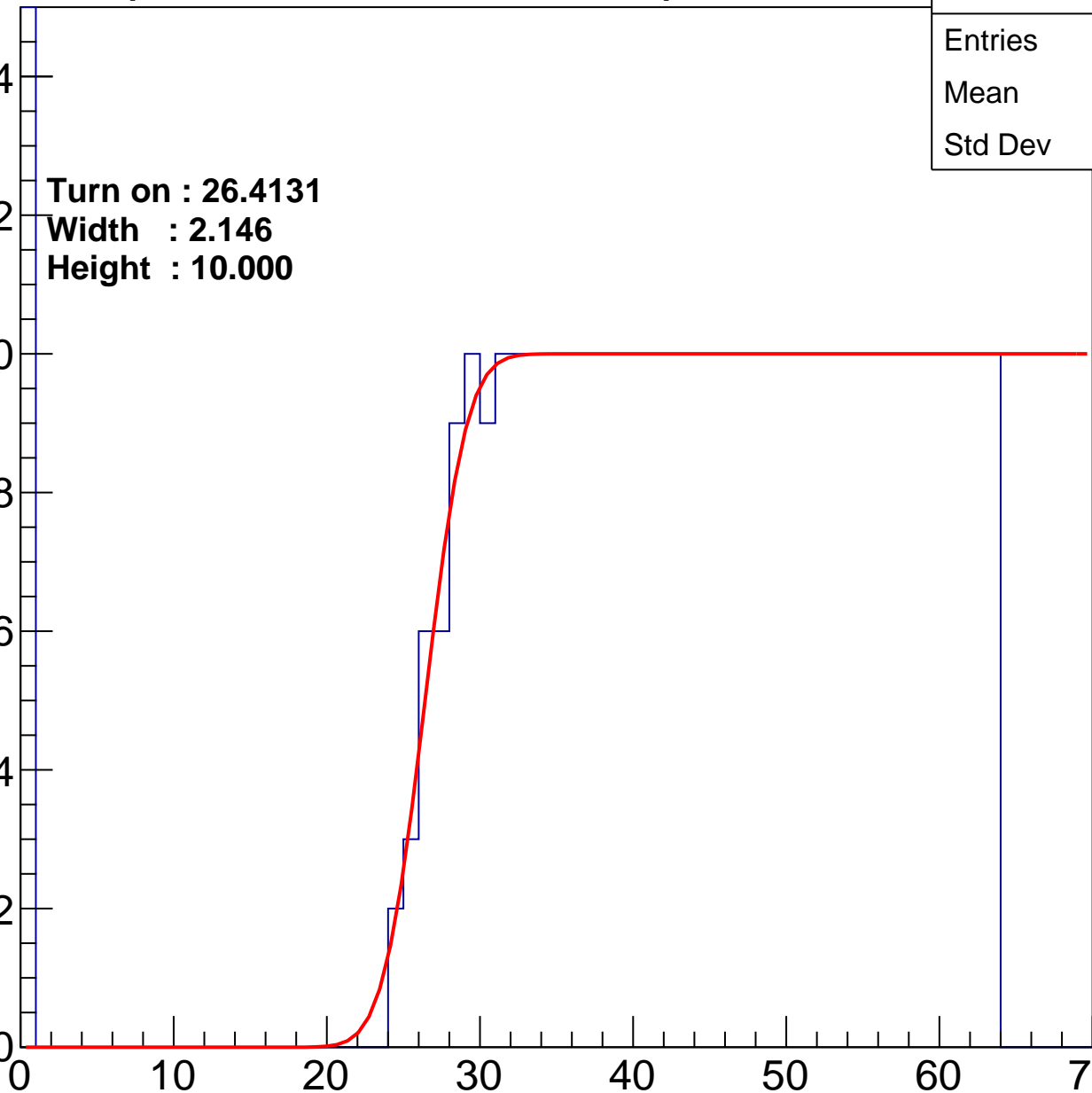
Width : 2.146

Height : 10.000

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch35

calib_packv5_041523_1651.root, FC#0, port C2

Entries	407
Mean	40.29
Std Dev	17.38

Turn on : 27.7761

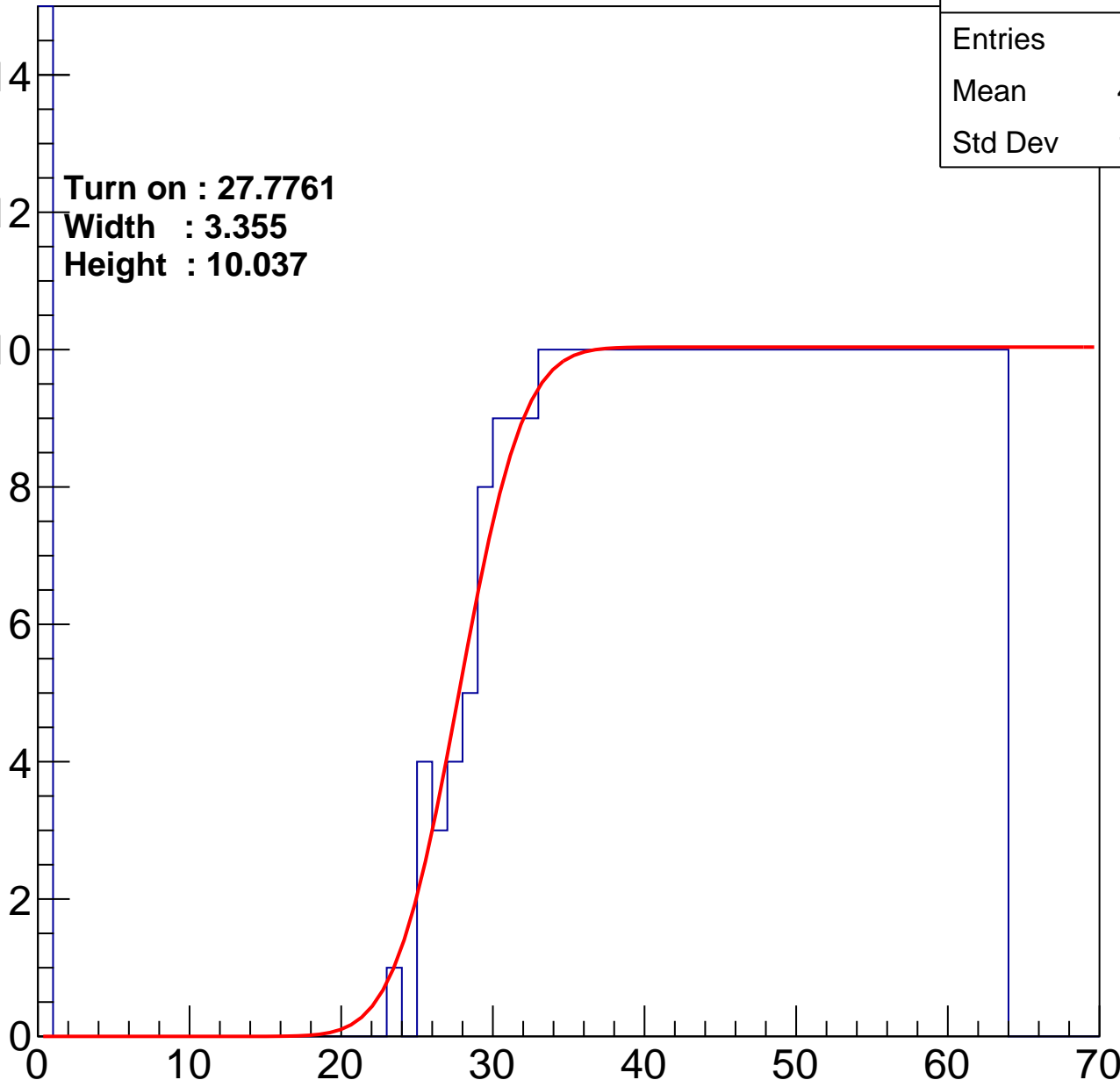
Width : 3.355

Height : 10.037

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch36

calib_packv5_041523_1651.root, FC#0, port C2

Entries	439
Mean	38.72
Std Dev	17.89

Turn on : 25.3572

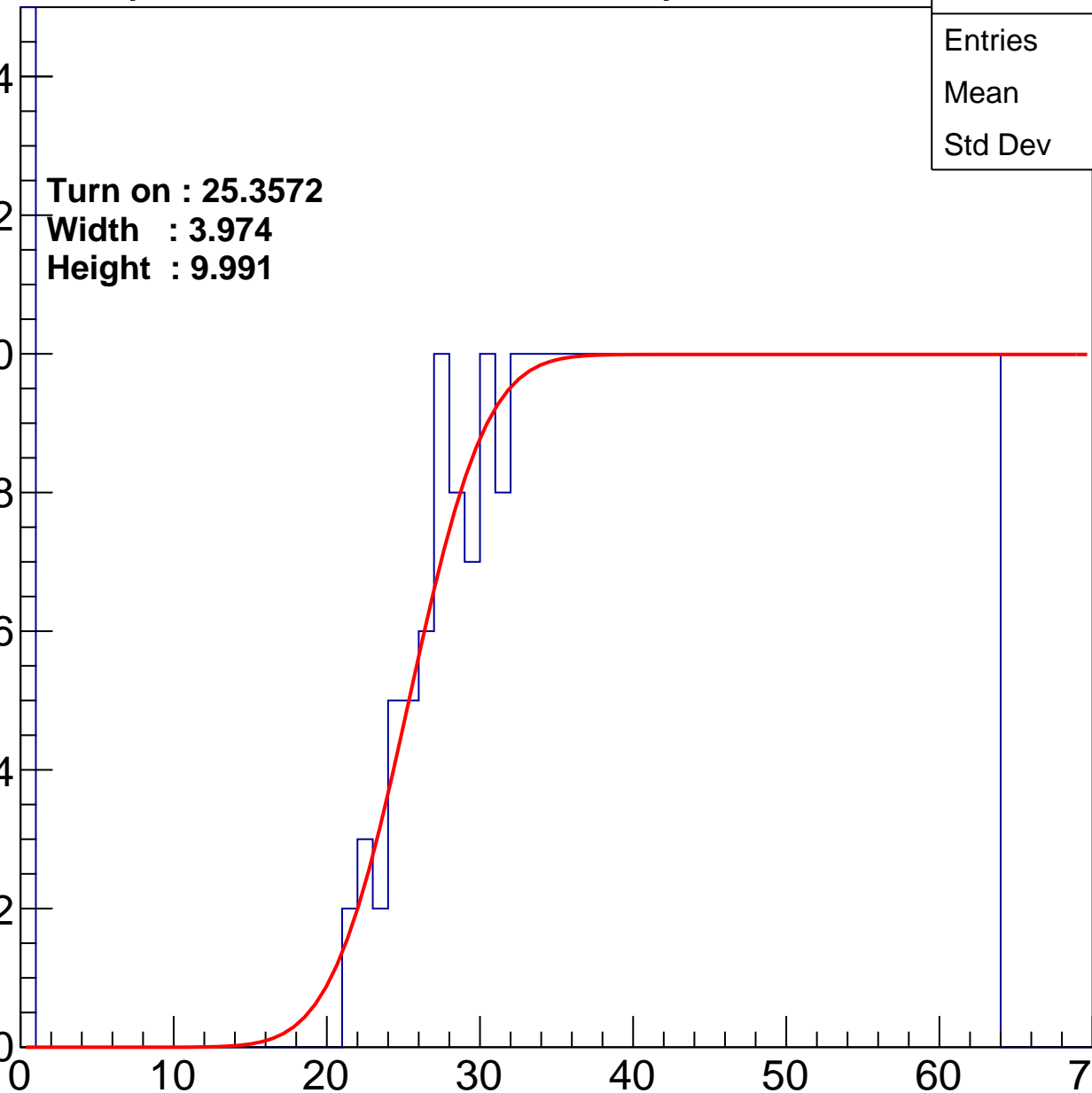
Width : 3.974

Height : 9.991

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch37

calib_packv5_041523_1651.root, FC#0, port C2

Entries	412
Mean	40.52
Std Dev	16.72

Turn on : 26.6259

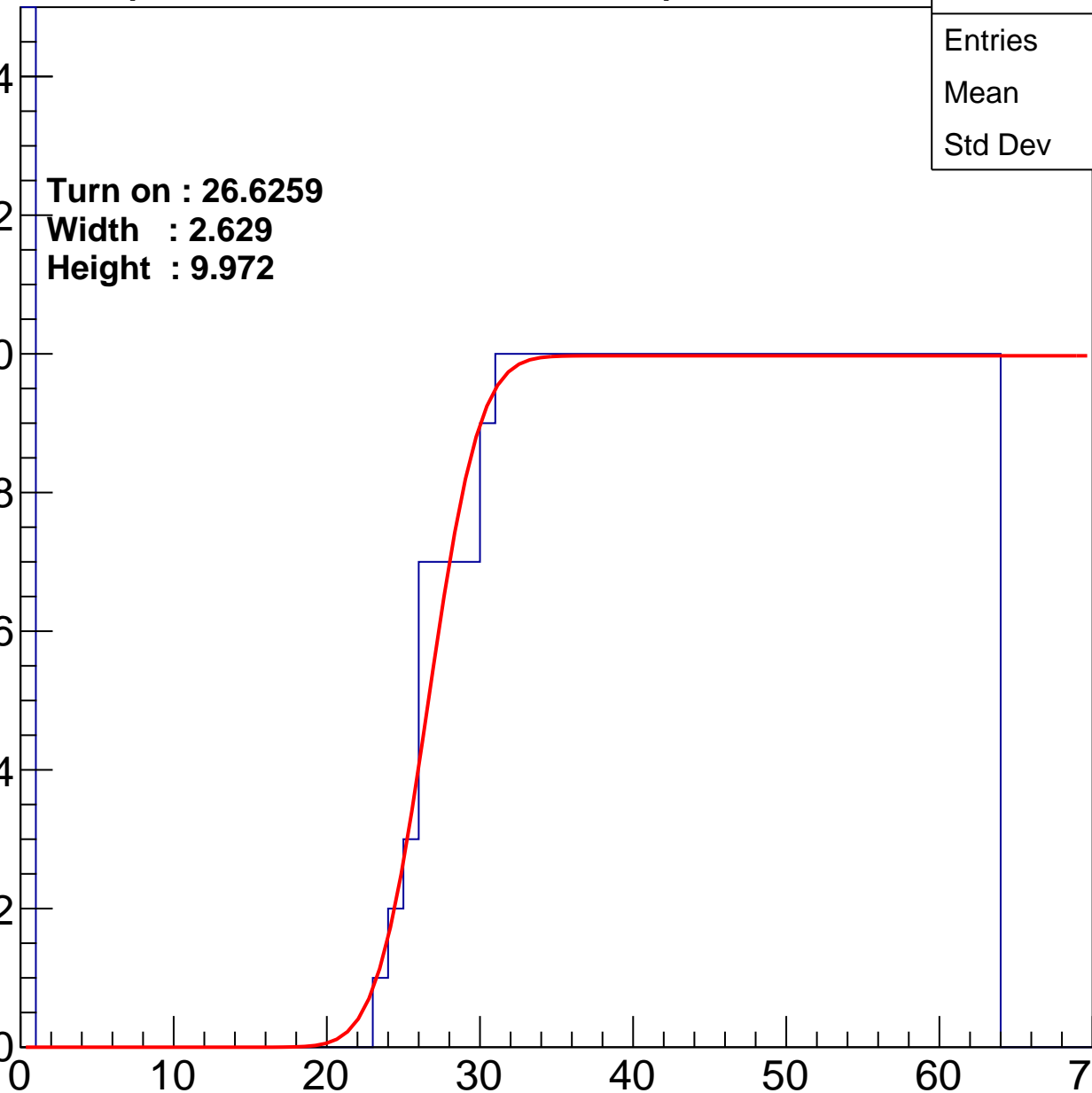
Width : 2.629

Height : 9.972

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch38

calib_packv5_041523_1651.root, FC#0, port C2

Entries	416
Mean	39.62
Std Dev	17.88

Turn on : 27.5741

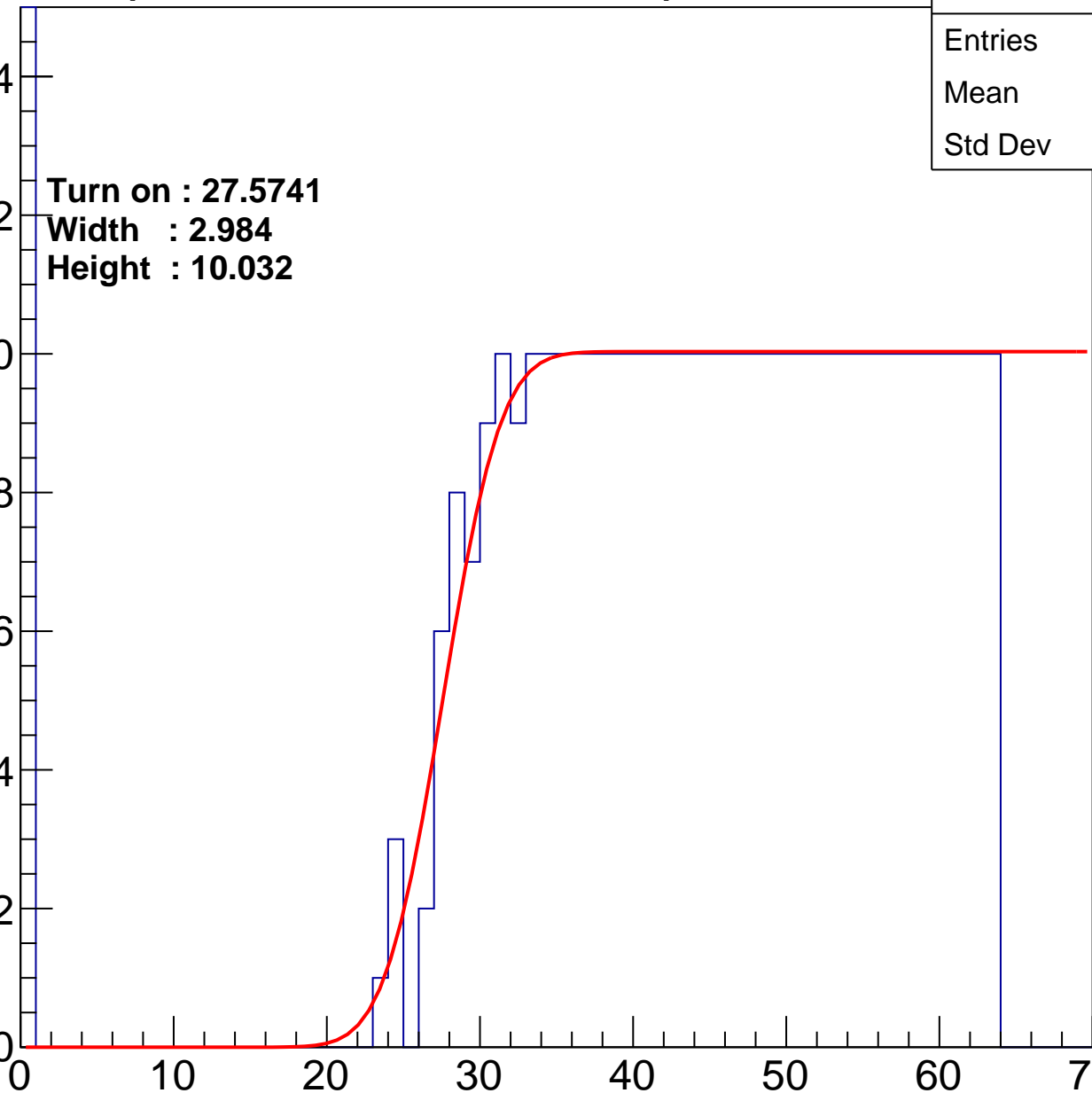
Width : 2.984

Height : 10.032

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch39

calib_packv5_041523_1651.root, FC#0, port C2

Entries	432
Mean	39.2
Std Dev	17.63

Turn on : 26.1712

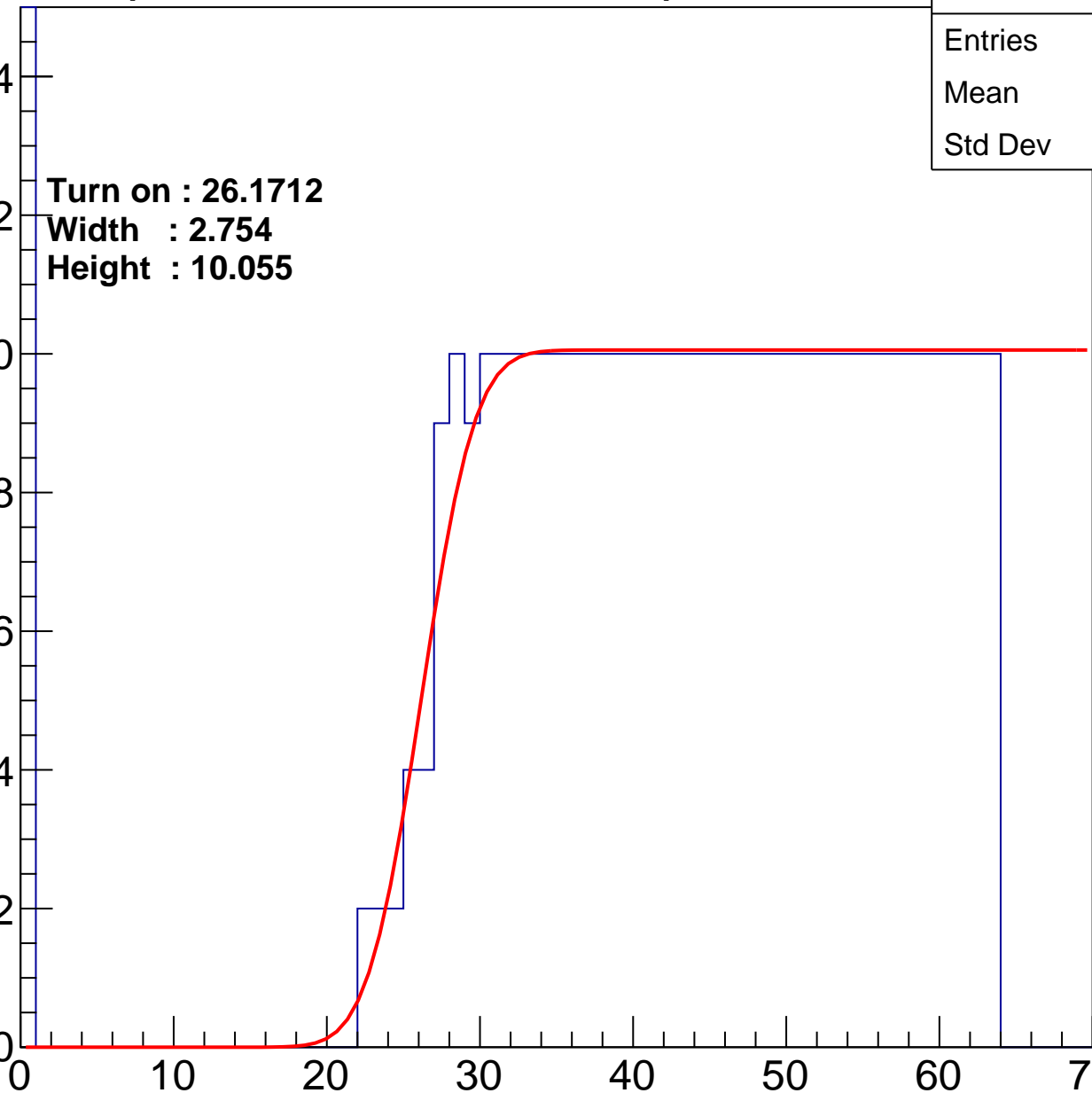
Width : 2.754

Height : 10.055

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch40

calib_packv5_041523_1651.root, FC#0, port C2

Entries	439
Mean	39.53
Std Dev	16.9

Turn on : 24.5229

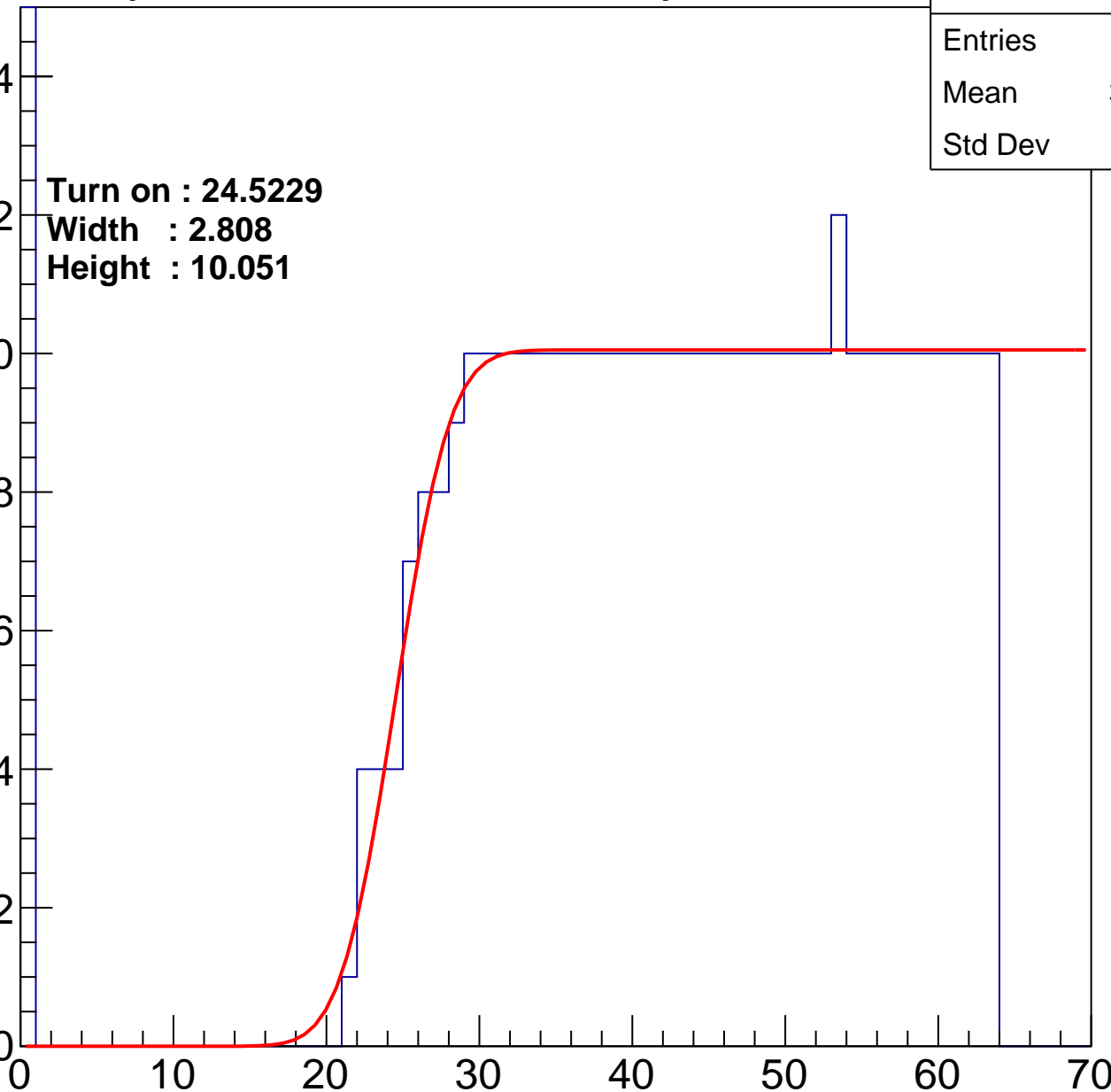
Width : 2.808

Height : 10.051

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch41

calib_packv5_041523_1651.root, FC#0, port C2

Entries	404
Mean	41.17
Std Dev	16.12

Turn on : 27.2111

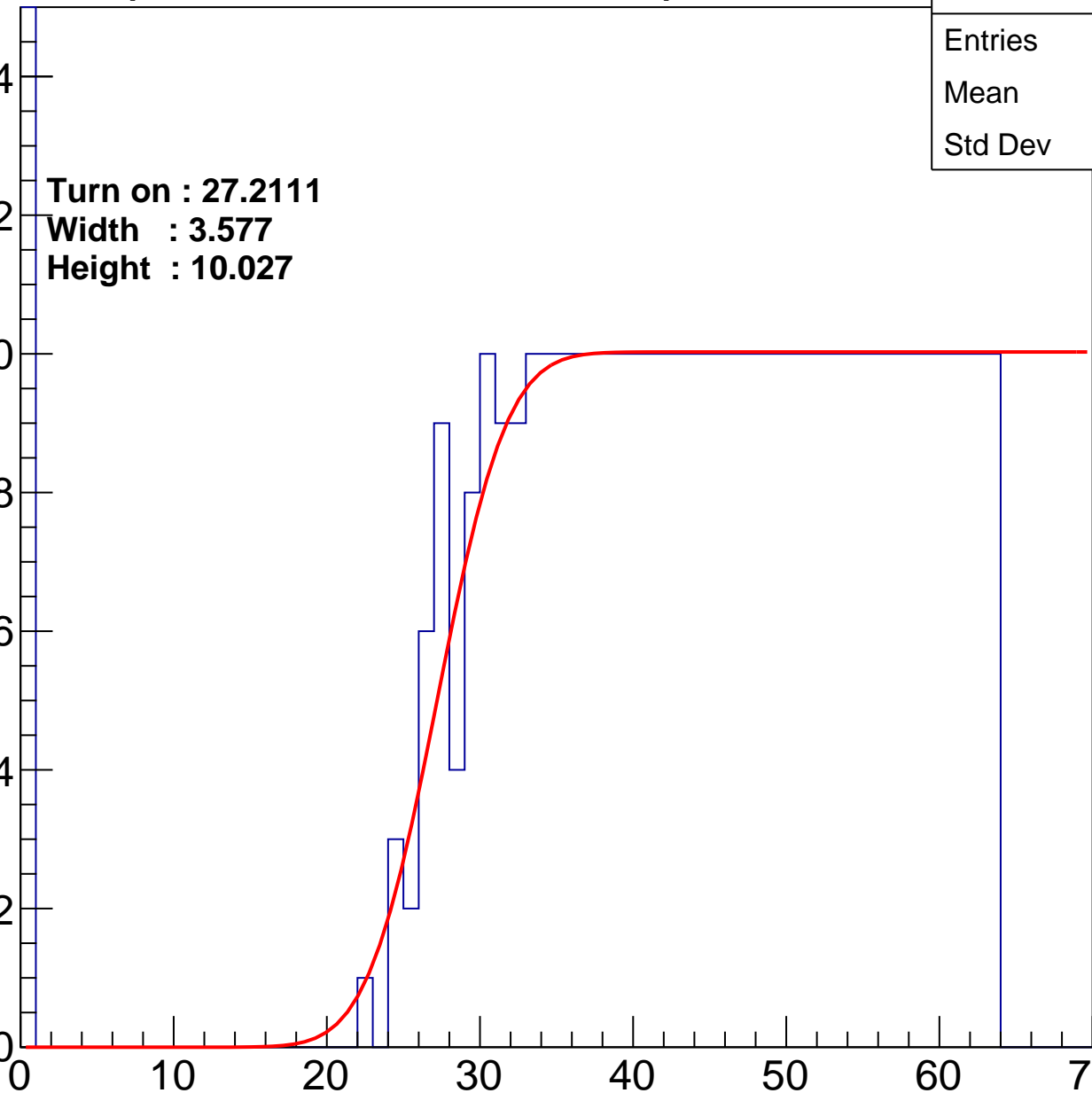
Width : 3.577

Height : 10.027

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch42

calib_packv5_041523_1651.root, FC#0, port C2

Entries	440
Mean	39.38
Std Dev	16.89

Turn on : 24.3943

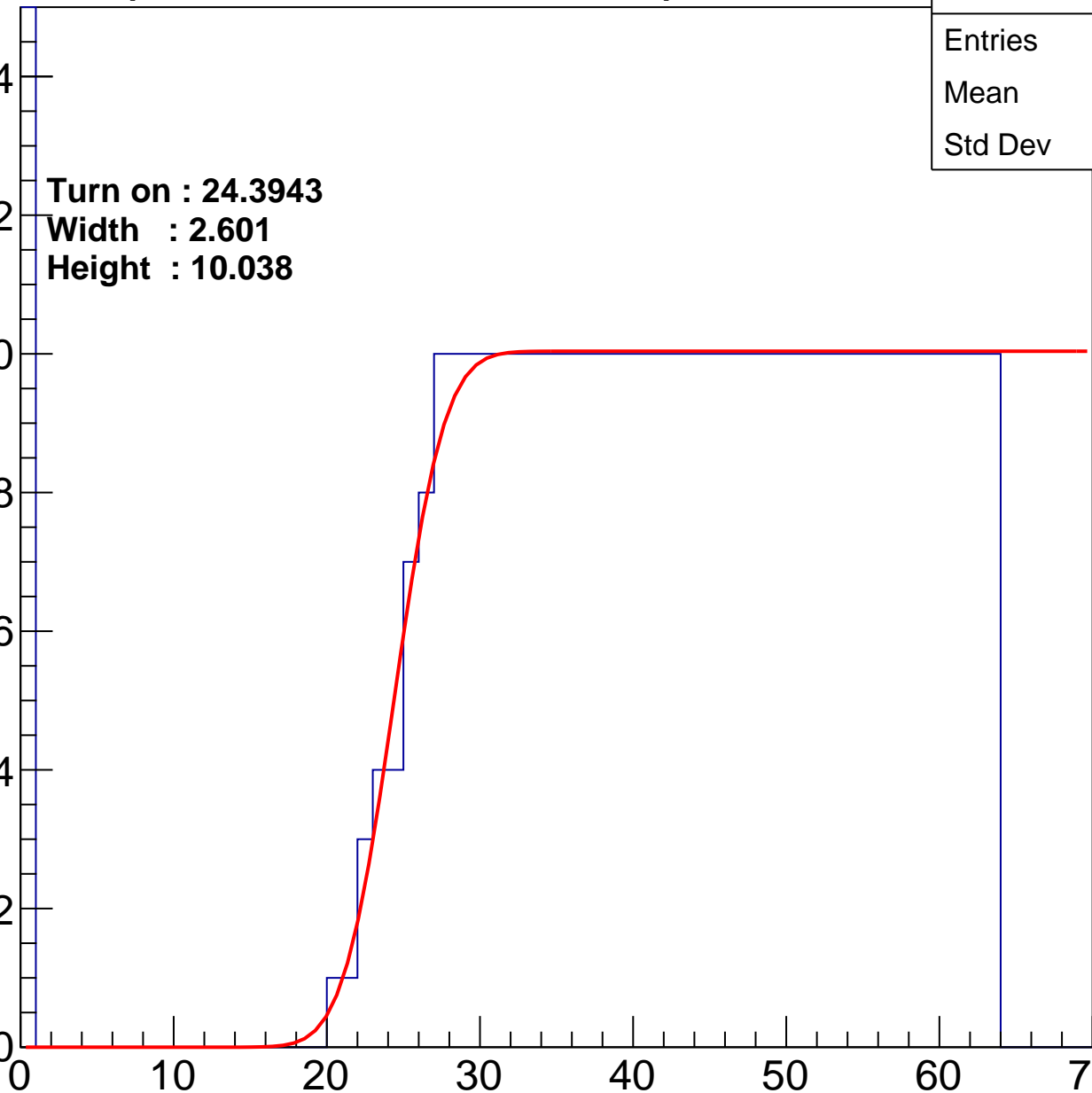
Width : 2.601

Height : 10.038

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch43

calib_packv5_041523_1651.root, FC#0, port C2

Entries	417
Mean	39.79
Std Dev	17.58

Turn on : 27.3395

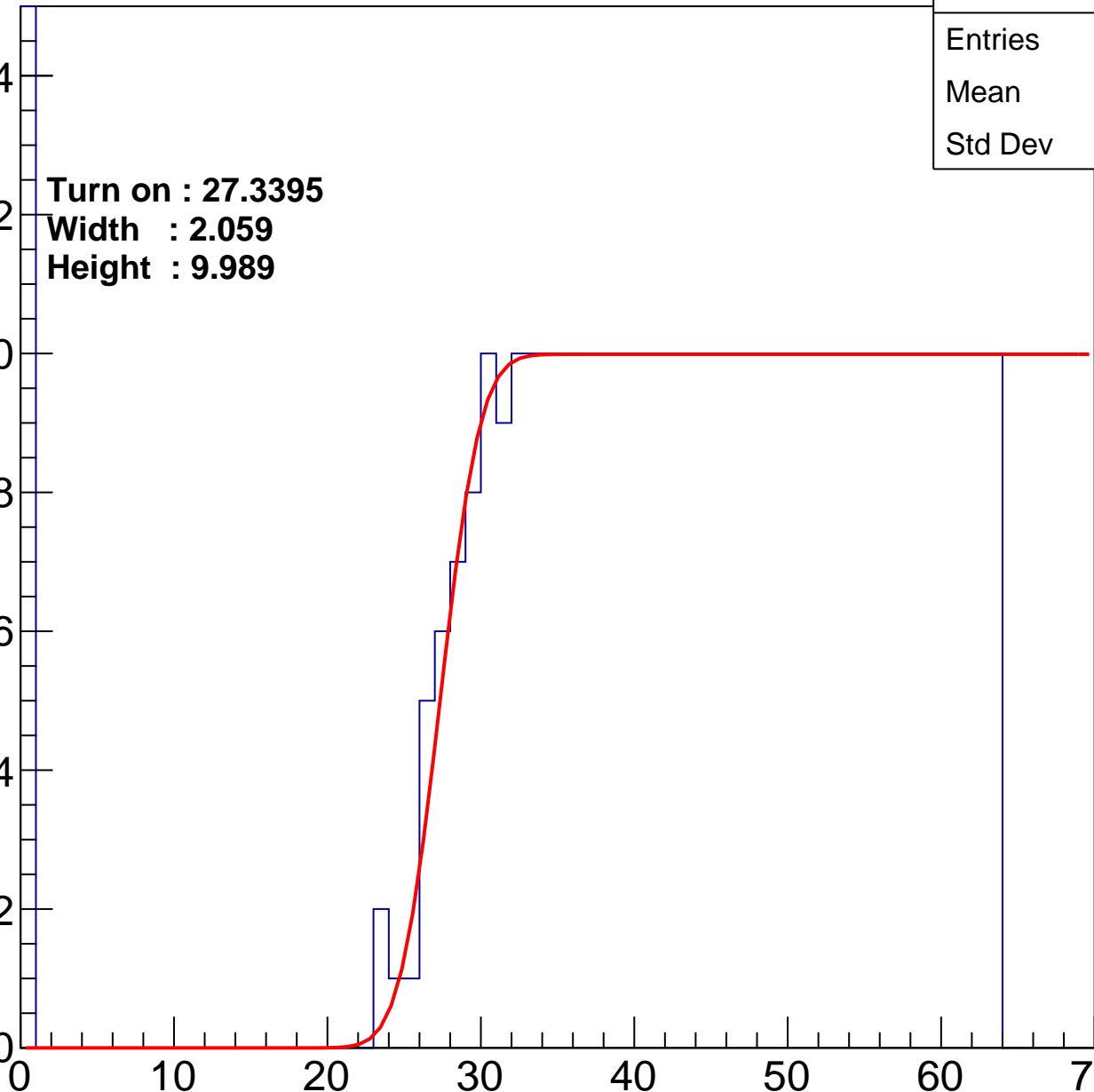
Width : 2.059

Height : 9.989

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch44

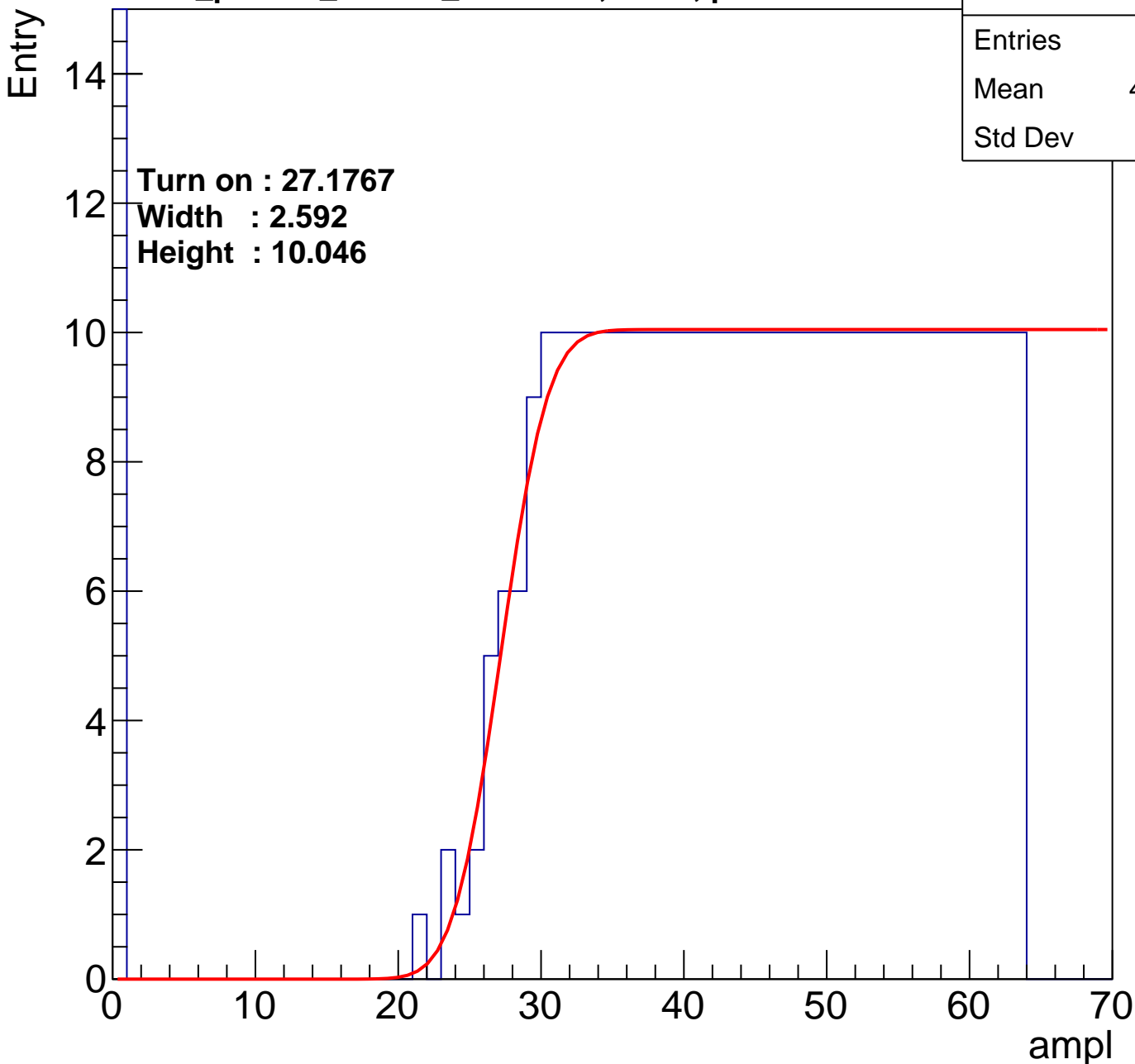
calib_packv5_041523_1651.root, FC#0, port C2

Entries	416
Mean	40.08
Std Dev	17.2

Turn on : 27.1767

Width : 2.592

Height : 10.046



B1L103S, U12-ch45

calib_packv5_041523_1651.root, FC#0, port C2

Entries	431
Mean	39.01
Std Dev	17.93

Turn on : 26.2046

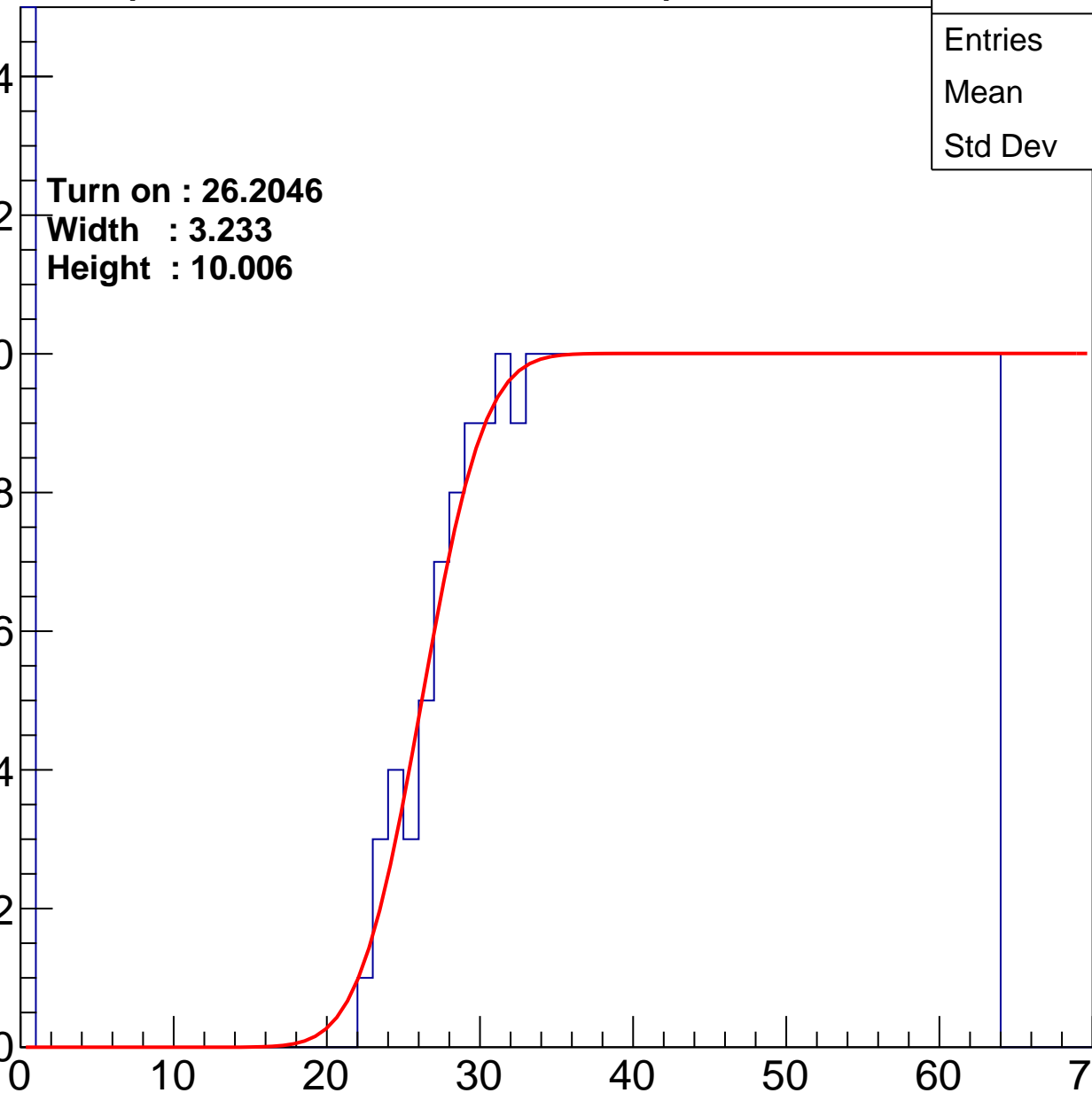
Width : 3.233

Height : 10.006

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch46

calib_packv5_041523_1651.root, FC#0, port C2

Entries	424
Mean	39.7
Std Dev	17.33

Turn on : 26.1474

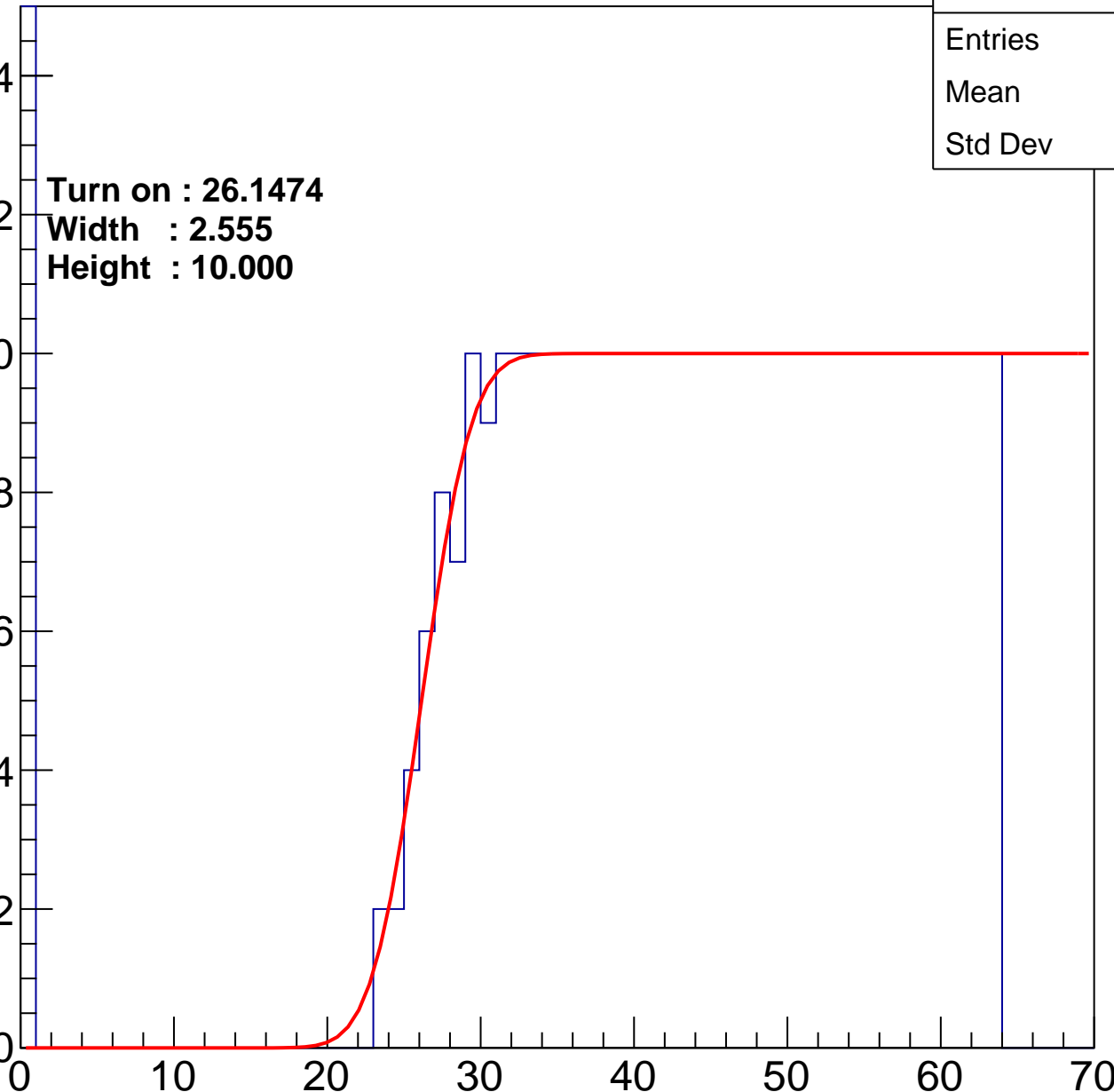
Width : 2.555

Height : 10.000

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch47

calib_packv5_041523_1651.root, FC#0, port C2

Entries	407
Mean	39.76
Std Dev	18.17

Turn on : 28.6197

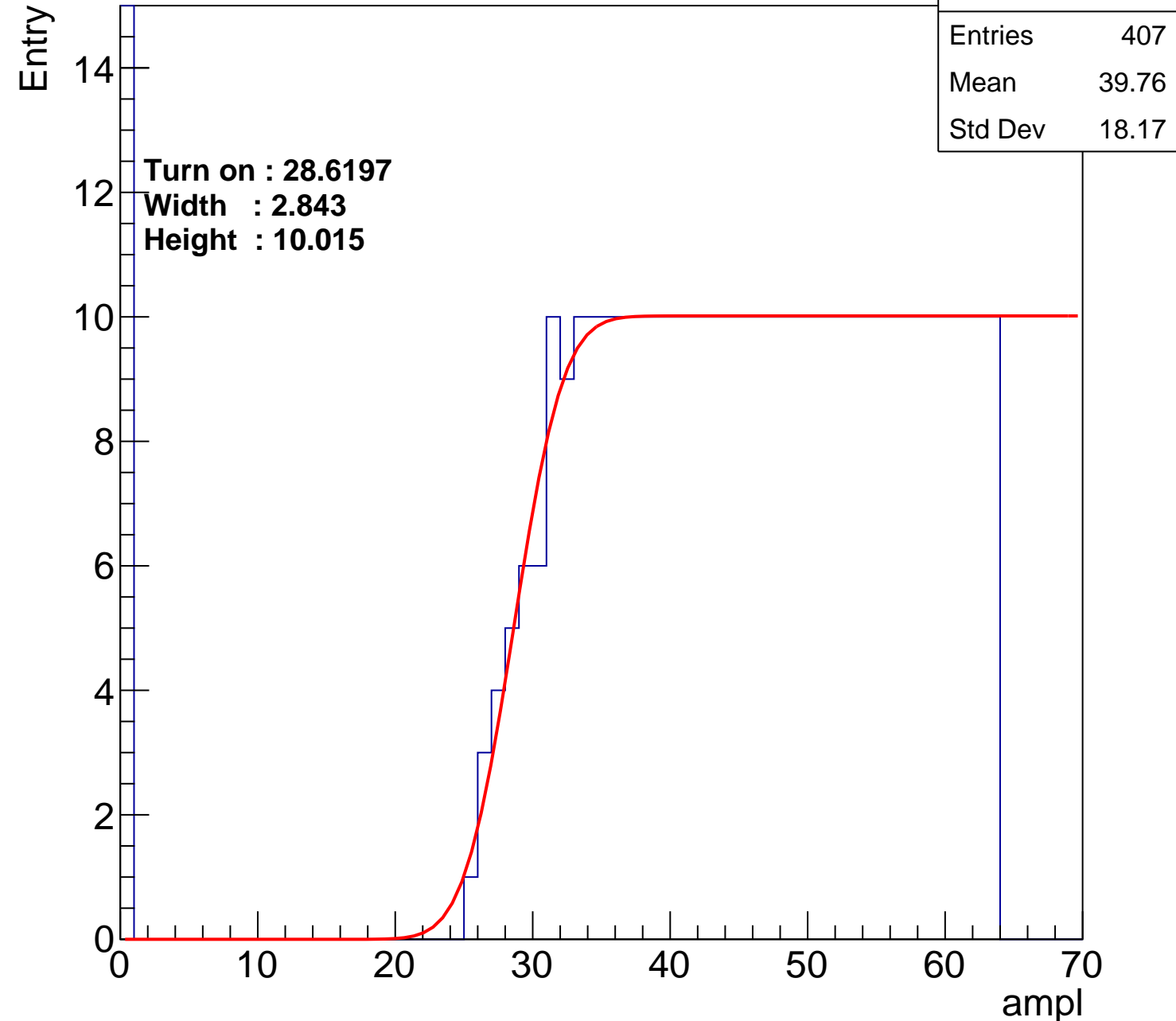
Width : 2.843

Height : 10.015

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch48

calib_packv5_041523_1651.root, FC#0, port C2

Entries	426
Mean	40.02
Std Dev	16.67

Turn on : 24.6031

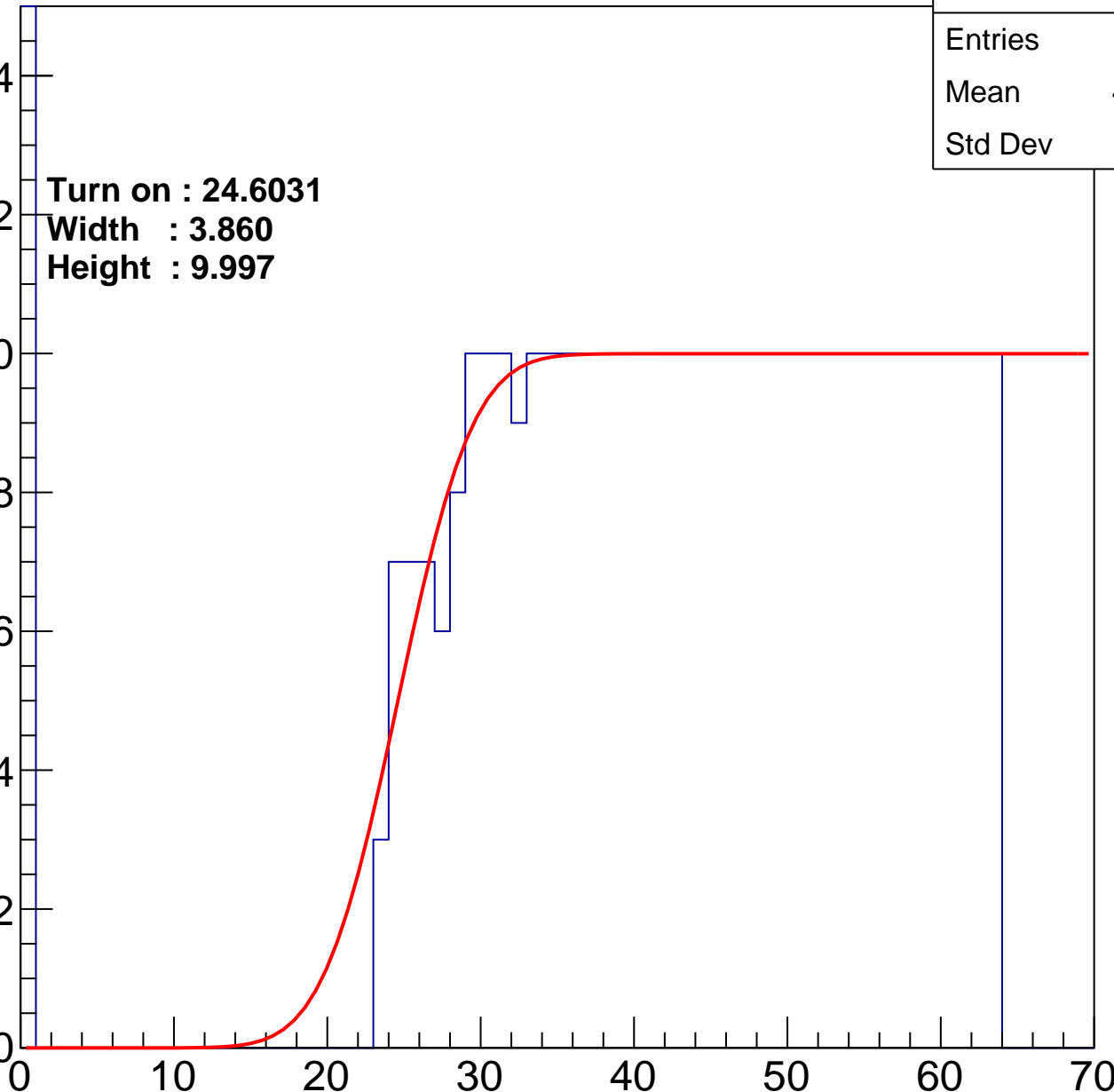
Width : 3.860

Height : 9.997

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch49

calib_packv5_041523_1651.root, FC#0, port C2

Entries	433
Mean	39.28
Std Dev	17.45

Turn on : 25.5294

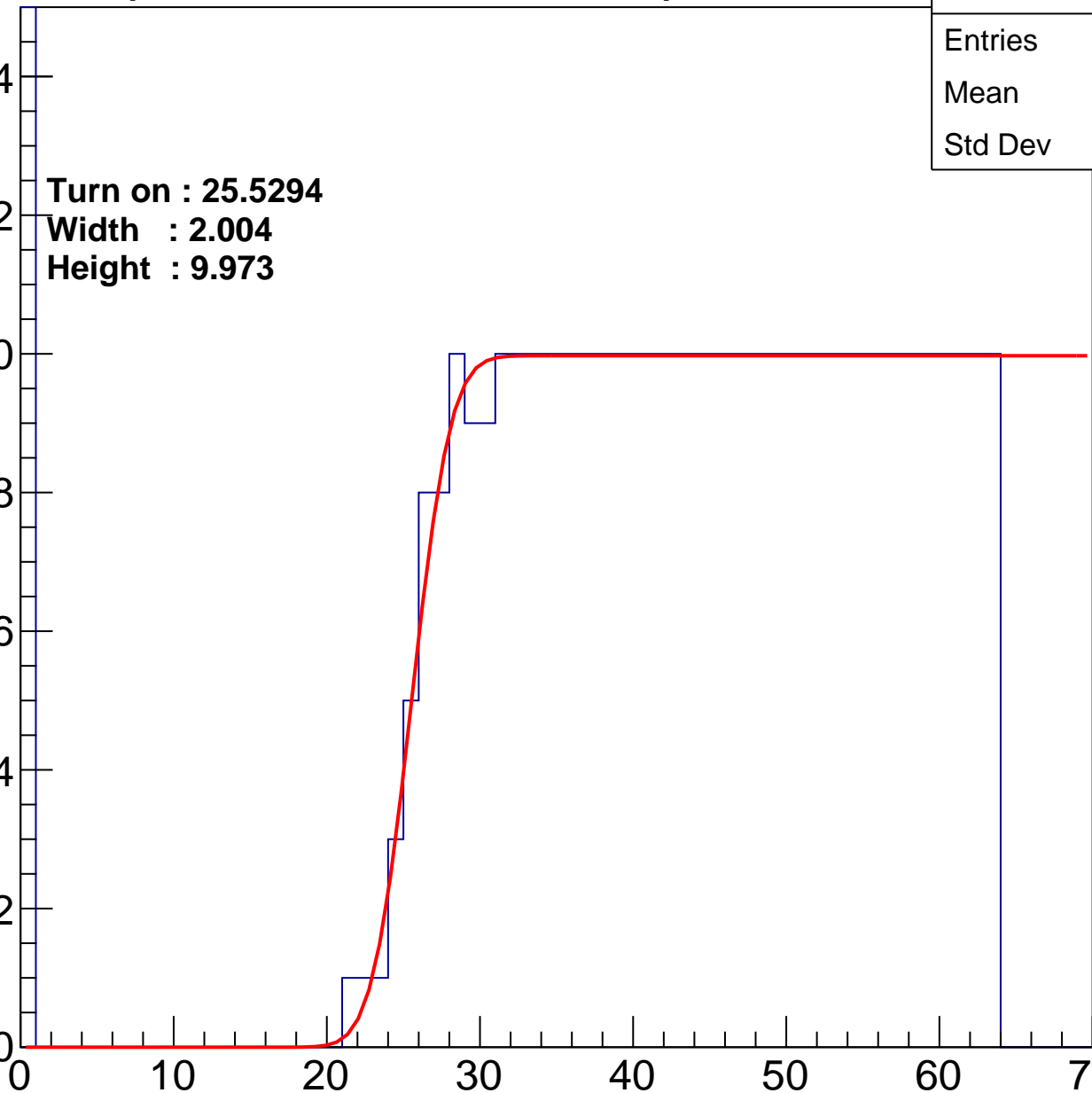
Width : 2.004

Height : 9.973

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch50

calib_packv5_041523_1651.root, FC#0, port C2

Entries	426
Mean	39.07
Std Dev	18.1

Turn on : 27.3613

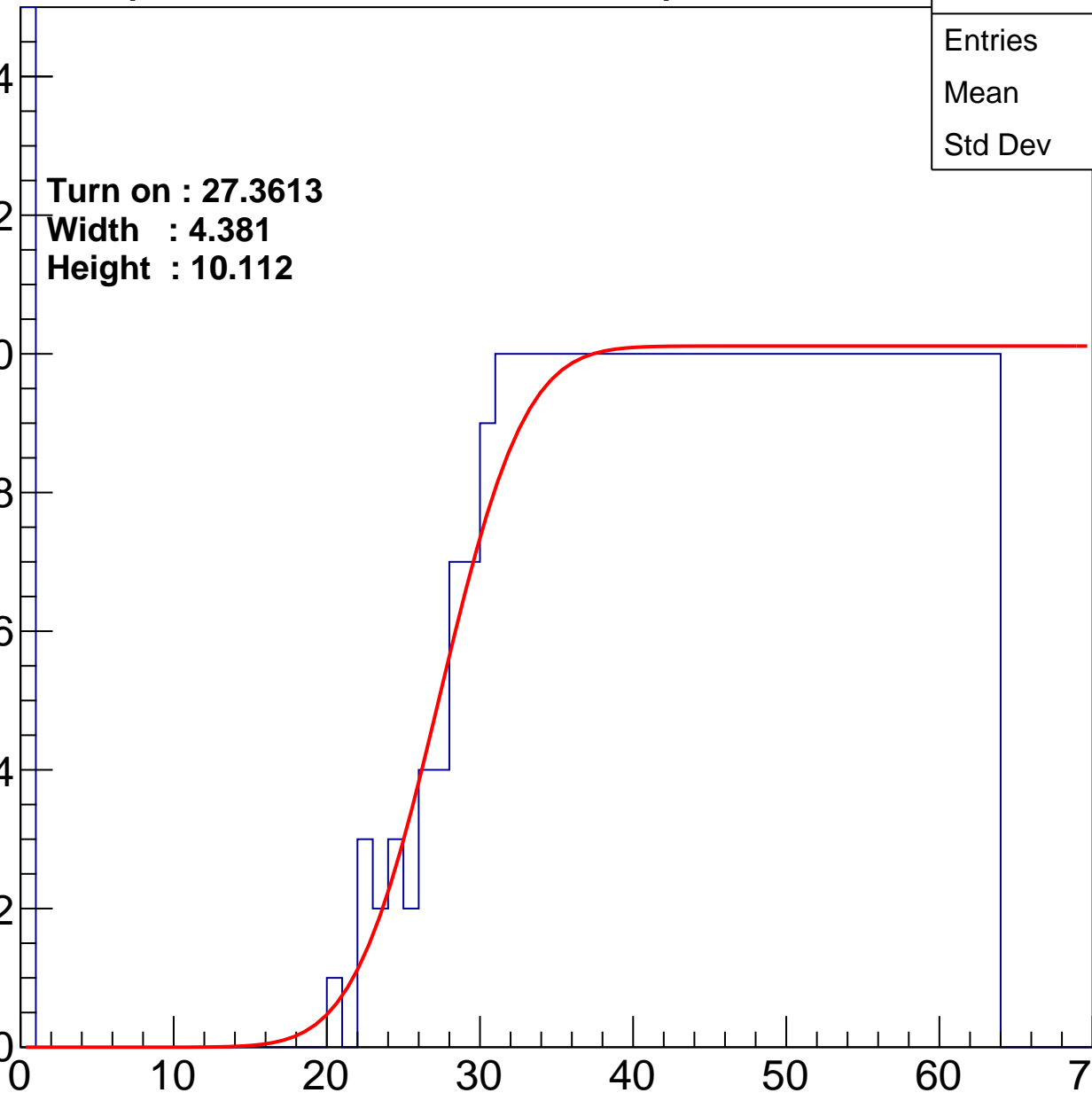
Width : 4.381

Height : 10.112

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch51

calib_packv5_041523_1651.root, FC#0, port C2

Entries	413
Mean	40.06
Std Dev	17.41

Turn on : 27.3456

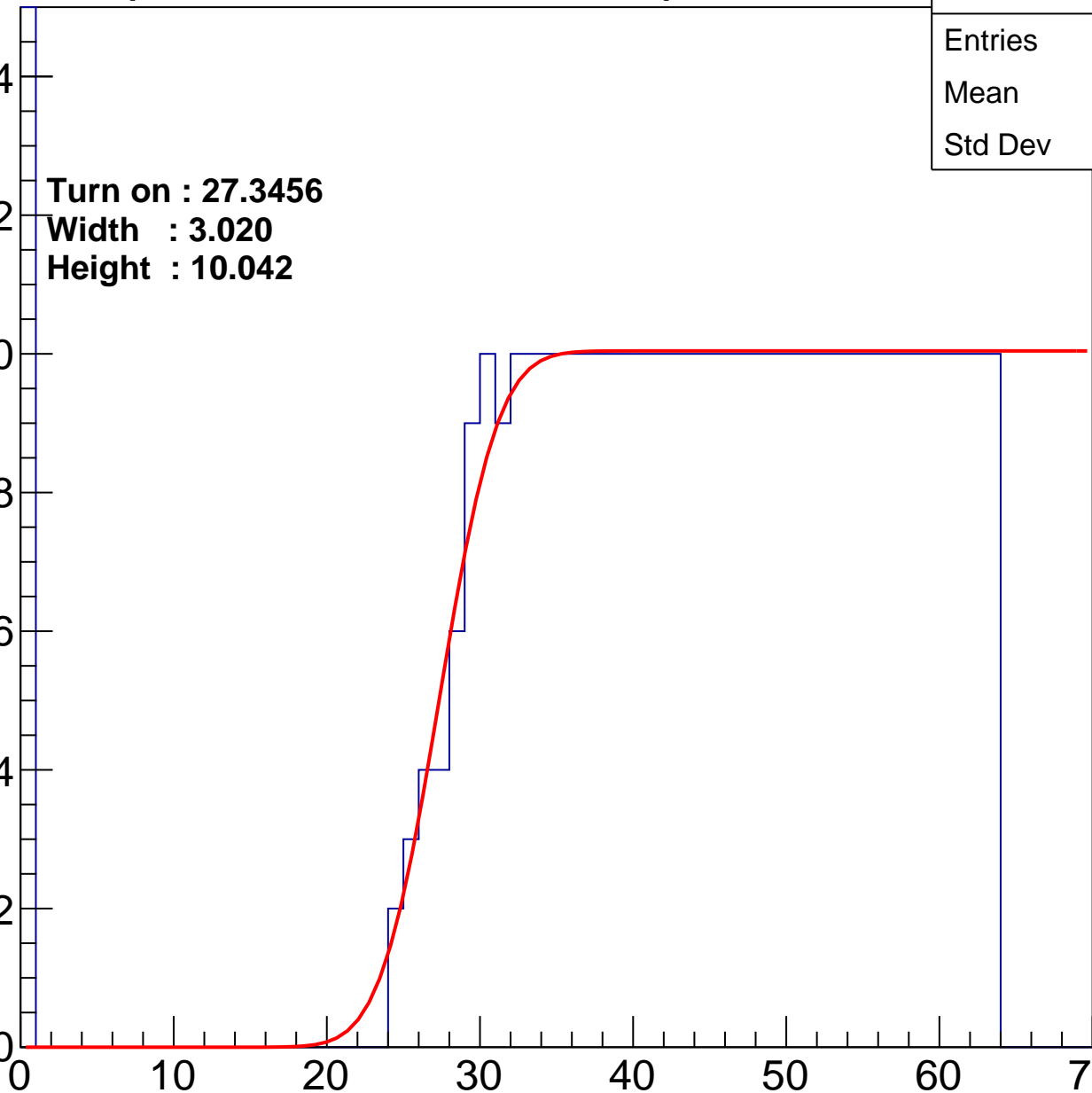
Width : 3.020

Height : 10.042

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch52

calib_packv5_041523_1651.root, FC#0, port C2

Entries	421
Mean	38.85
Std Dev	18.67

Turn on : 28.6810

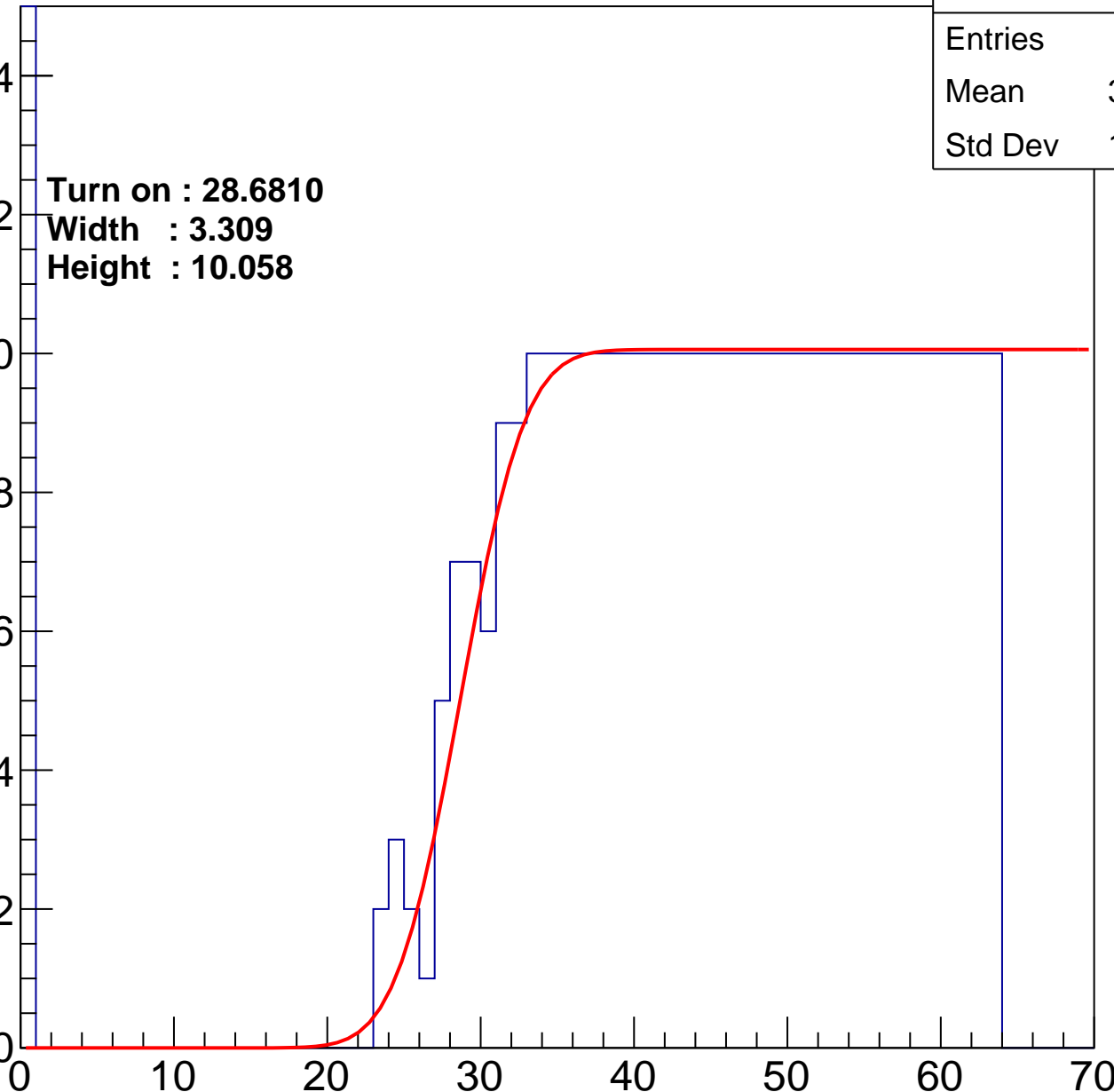
Width : 3.309

Height : 10.058

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch53

calib_packv5_041523_1651.root, FC#0, port C2

Entries	389
Mean	41.45
Std Dev	16.64

Turn on : 29.0521

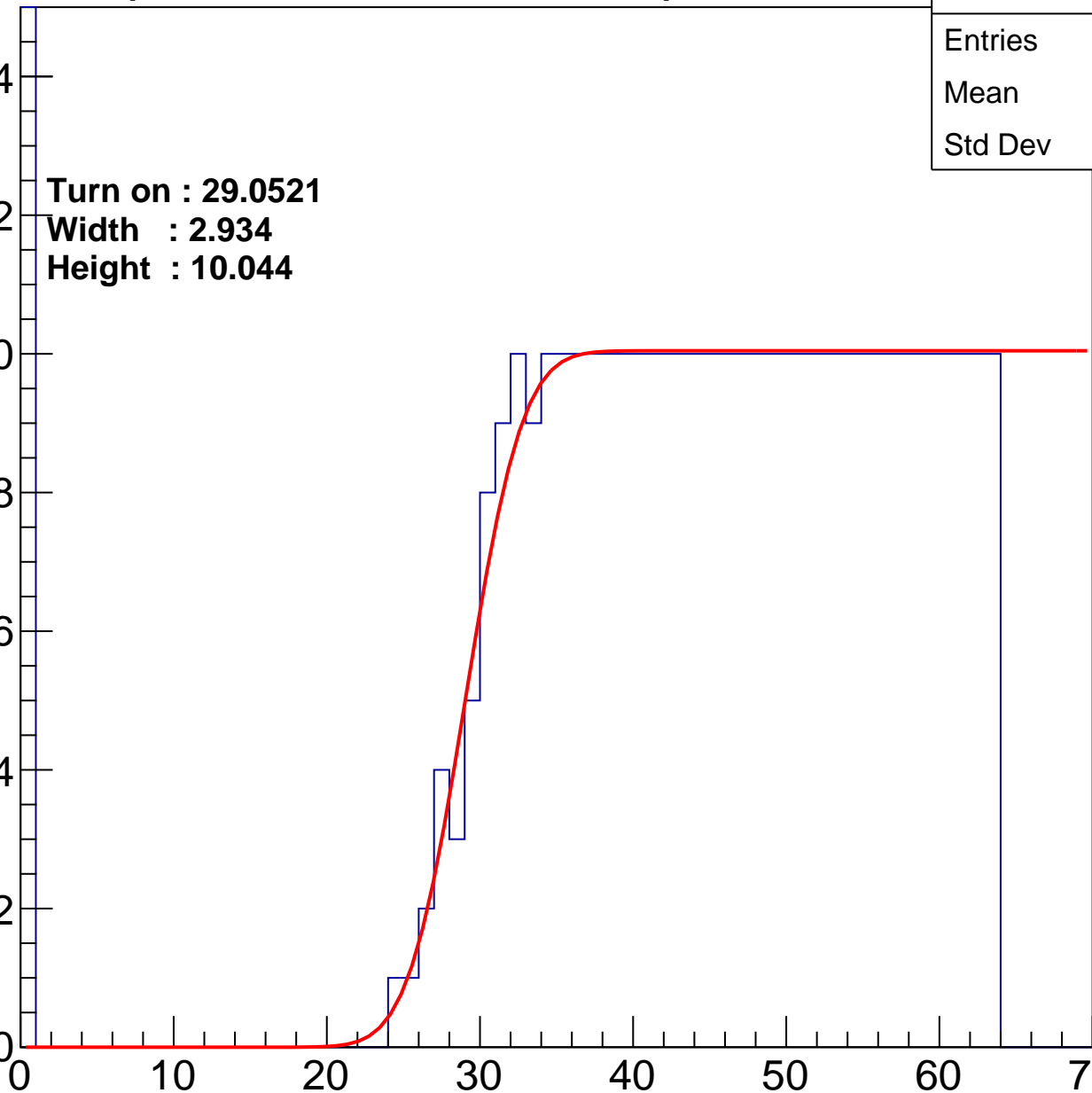
Width : 2.934

Height : 10.044

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch54

calib_packv5_041523_1651.root, FC#0, port C2

Entries	426
Mean	40.21
Std Dev	16.33

Turn on : 25.6296

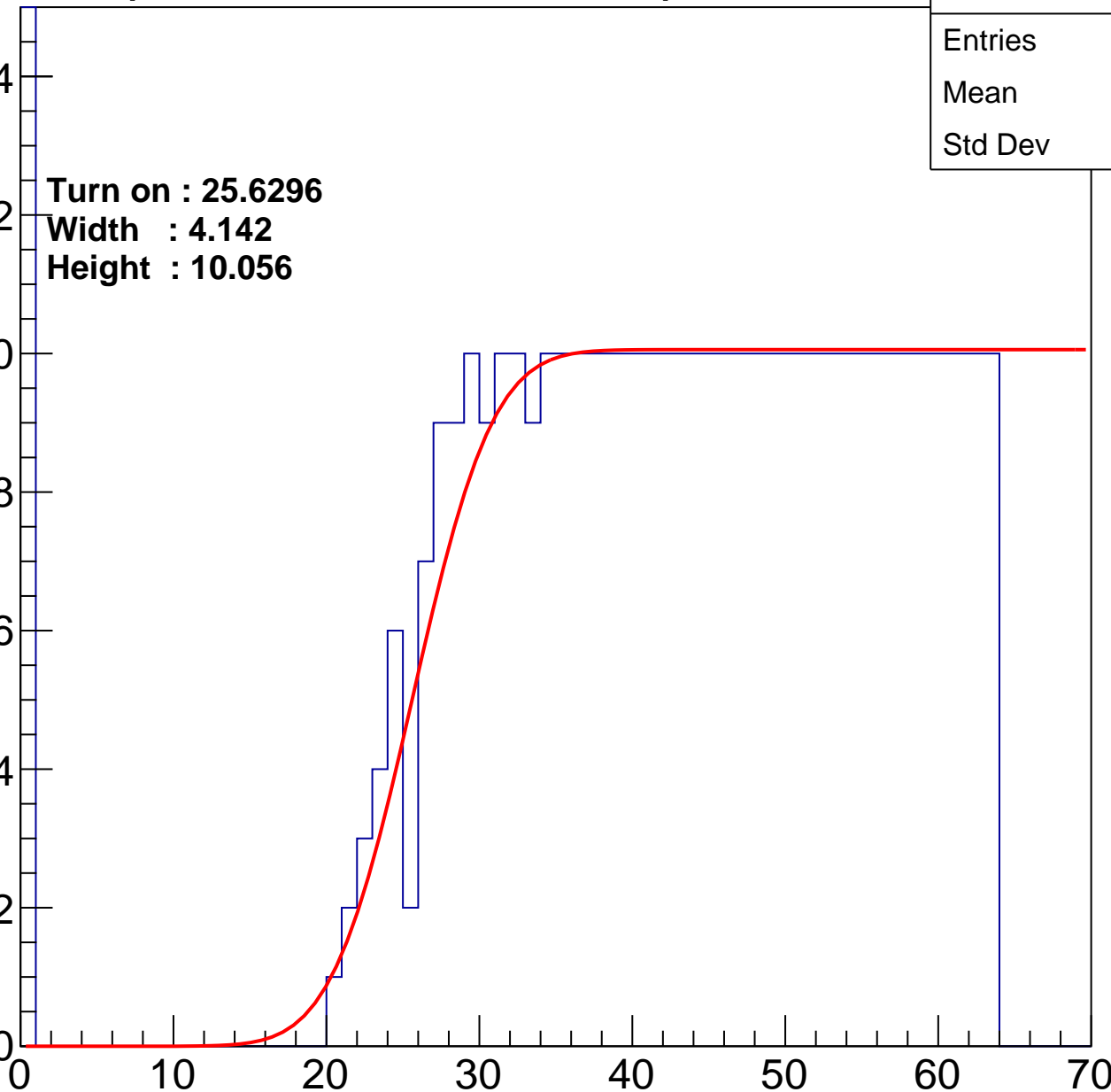
Width : 4.142

Height : 10.056

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch55

calib_packv5_041523_1651.root, FC#0, port C2

Entries	434
Mean	38.66
Std Dev	18.3

Turn on : 26.2614

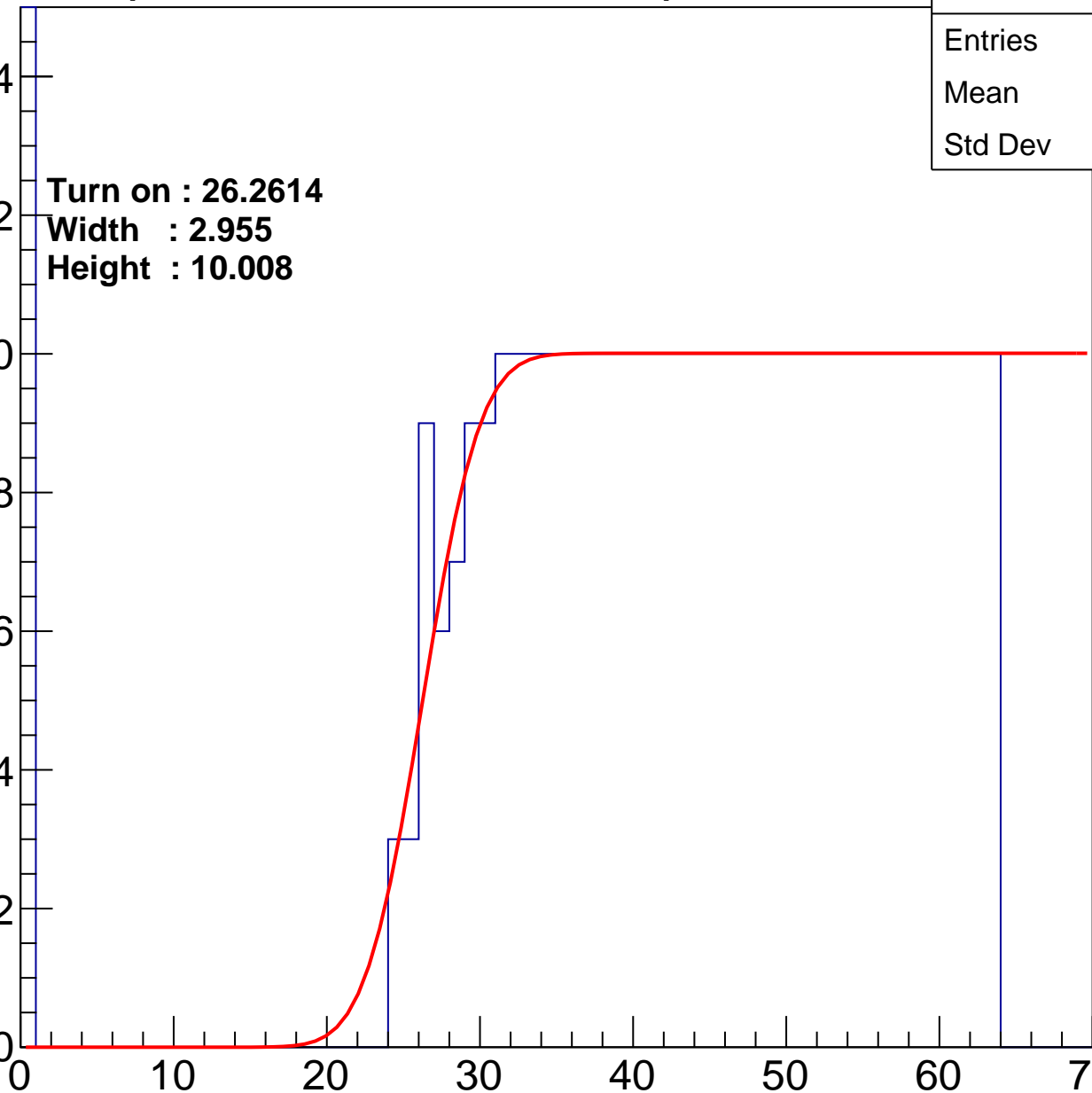
Width : 2.955

Height : 10.008

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch56

calib_packv5_041523_1651.root, FC#0, port C2

Entries	428
Mean	38.97
Std Dev	18.15

Turn on : 26.7922

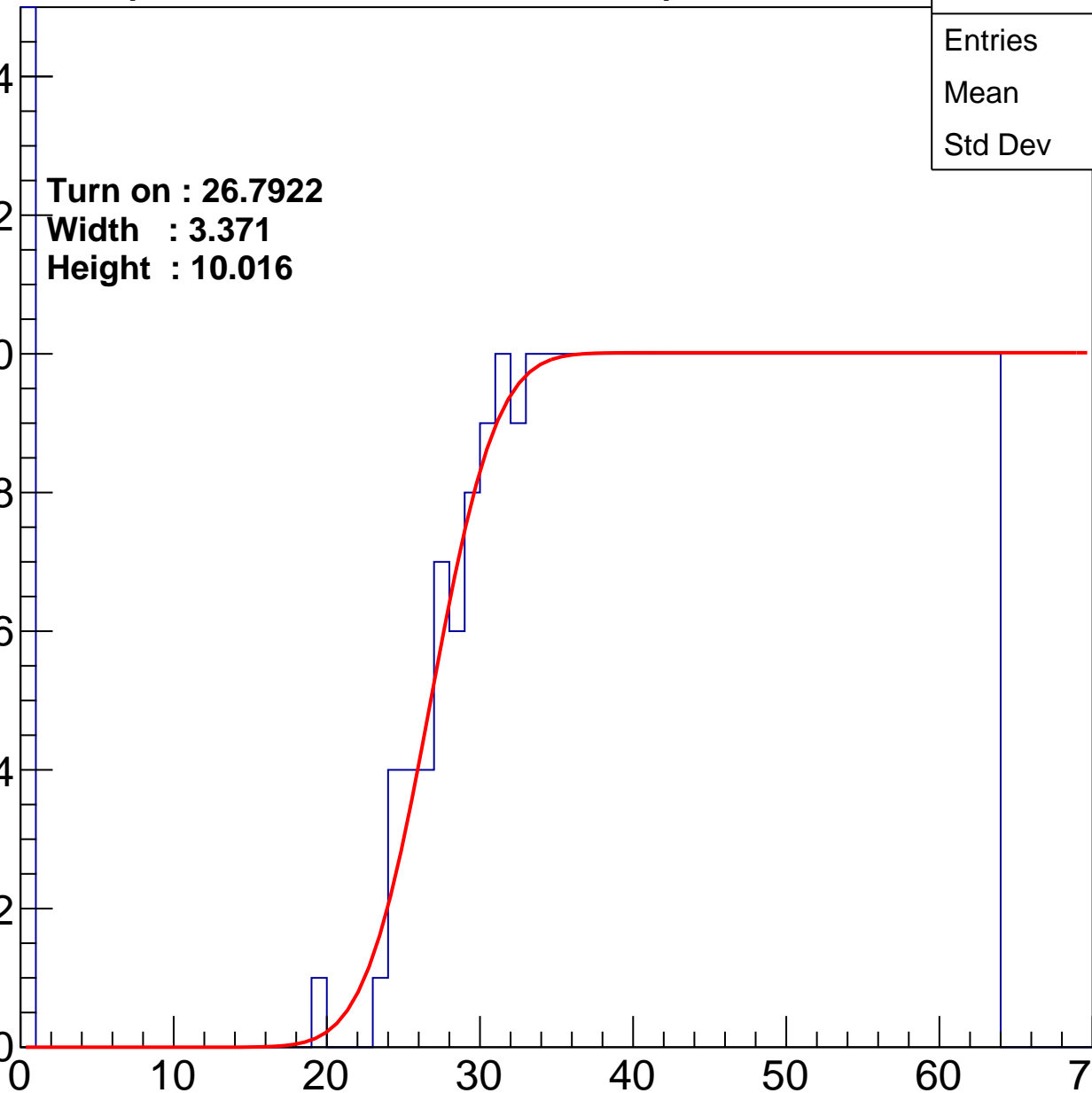
Width : 3.371

Height : 10.016

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch57

calib_packv5_041523_1651.root, FC#0, port C2

Entries	437
Mean	38.88
Std Dev	17.79

Turn on : 25.6741

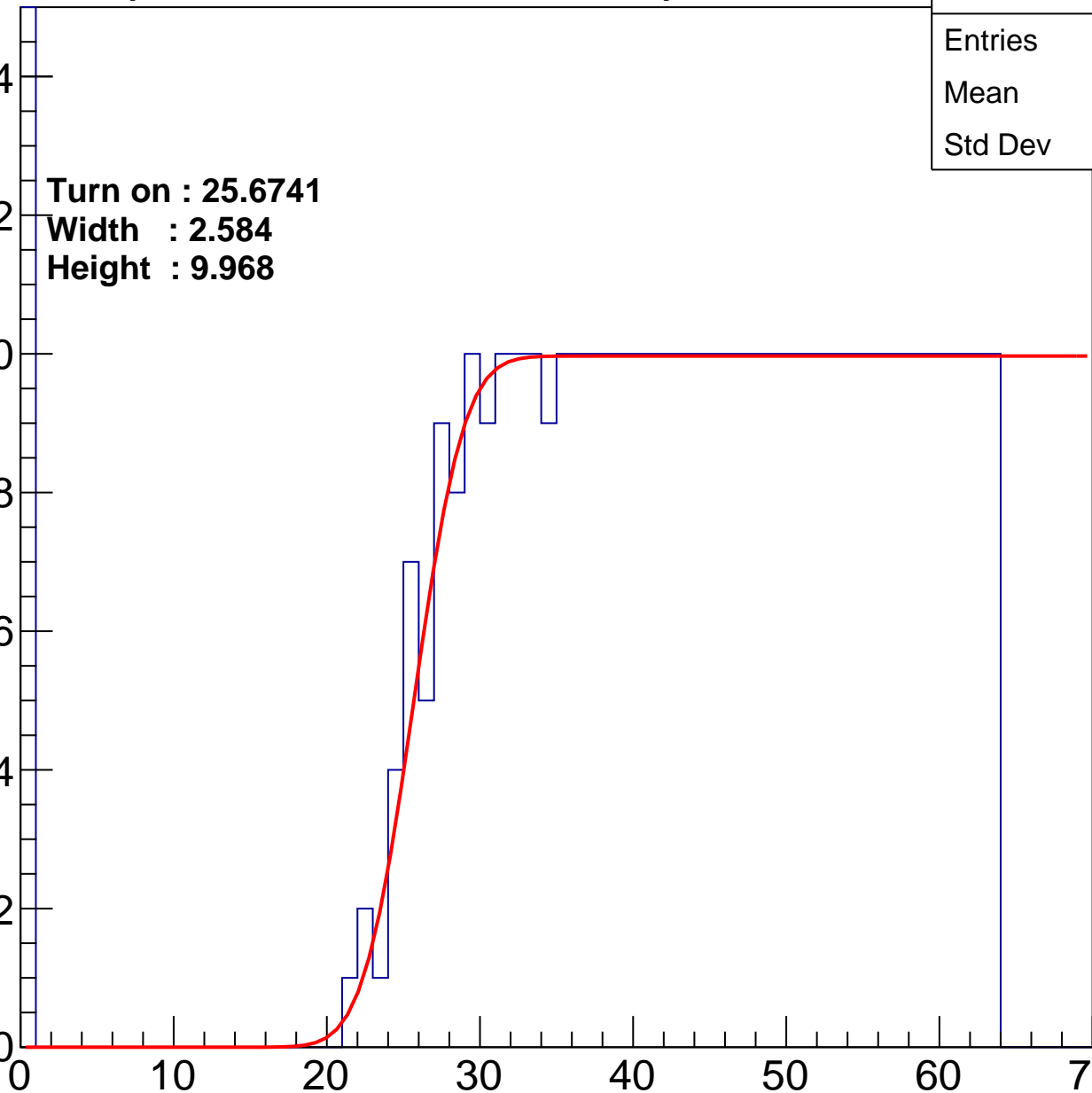
Width : 2.584

Height : 9.968

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch58

calib_packv5_041523_1651.root, FC#0, port C2

Entries	433
Mean	39.42
Std Dev	17.21

Turn on : 25.4588

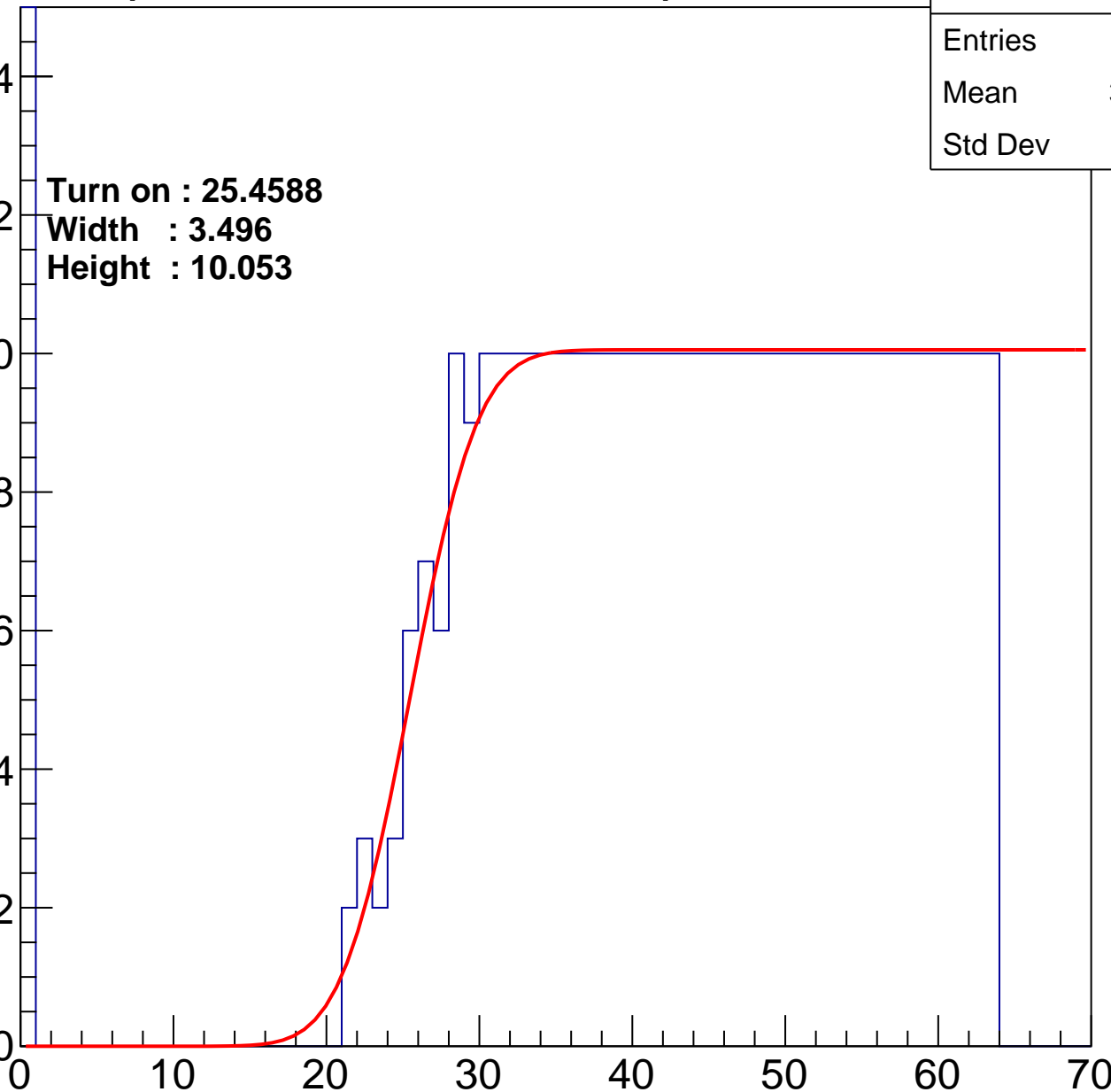
Width : 3.496

Height : 10.053

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch59

calib_packv5_041523_1651.root, FC#0, port C2

Entries	411
Mean	40.28
Std Dev	17.16

Turn on : 27.6176

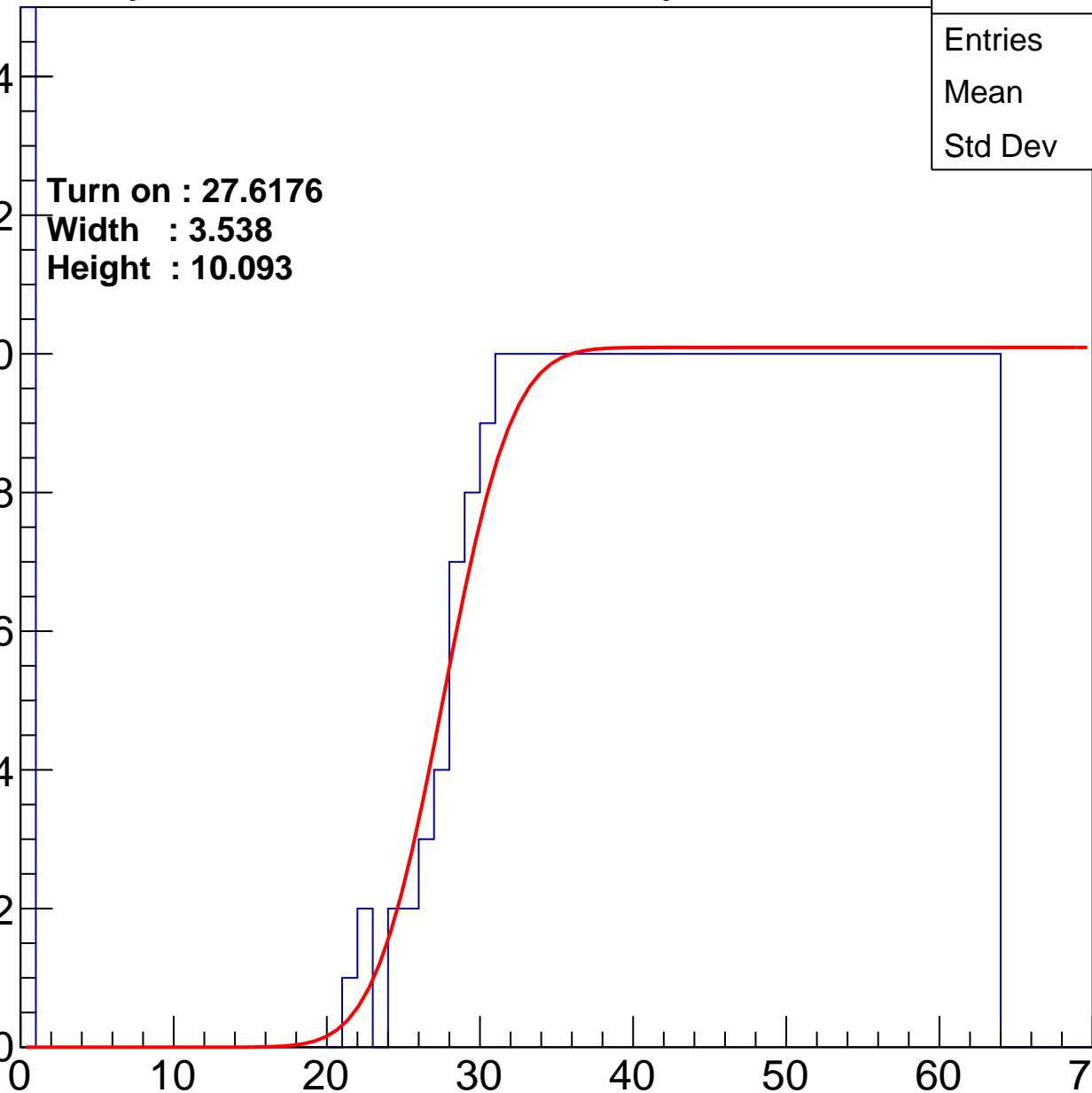
Width : 3.538

Height : 10.093

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch60

calib_packv5_041523_1651.root, FC#0, port C2

Entries	413
Mean	40.15
Std Dev	17.24

Turn on : 27.1328

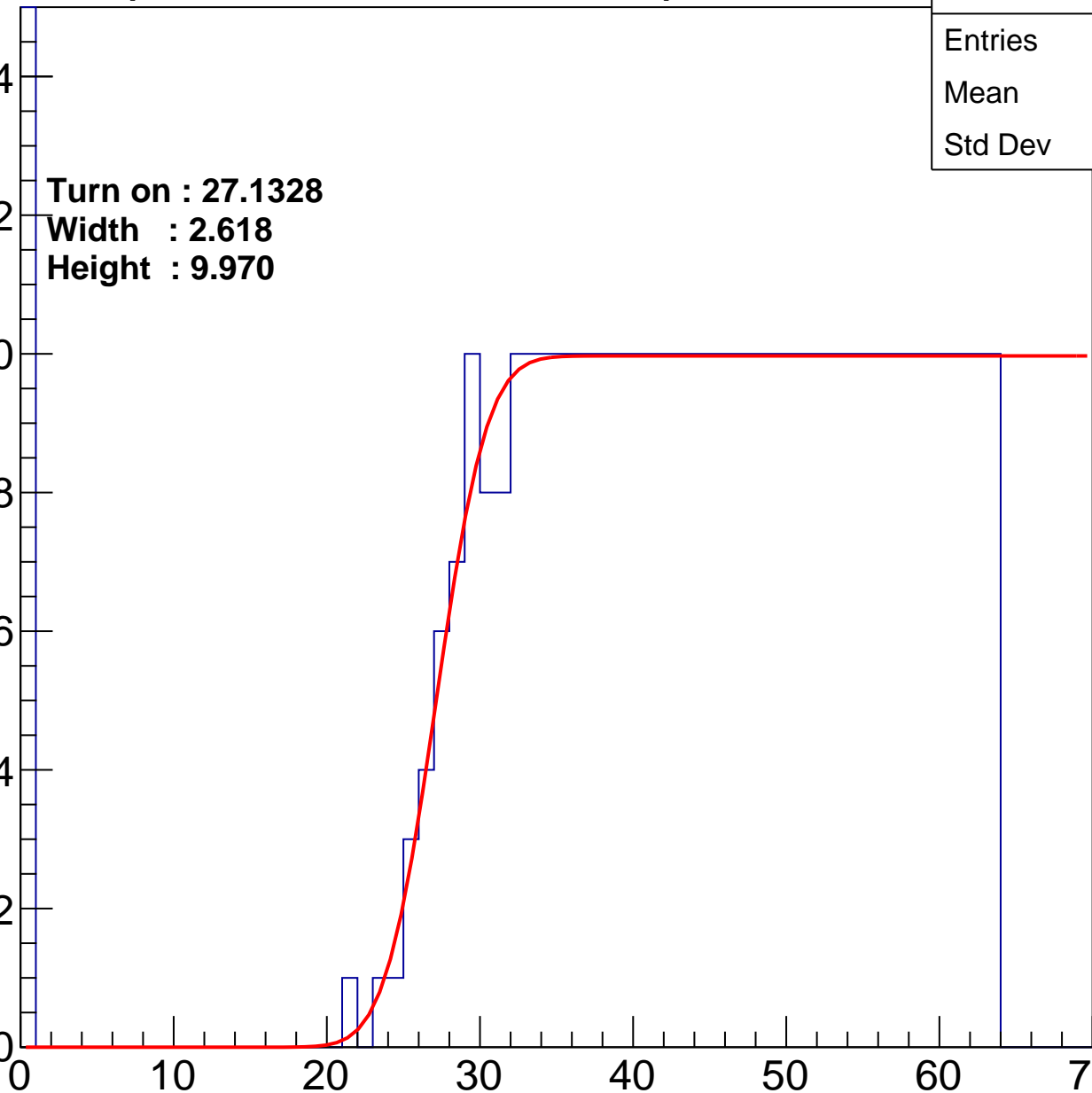
Width : 2.618

Height : 9.970

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch61

calib_packv5_041523_1651.root, FC#0, port C2

Entries	428
Mean	38.67
Std Dev	18.61

Turn on : 27.1525

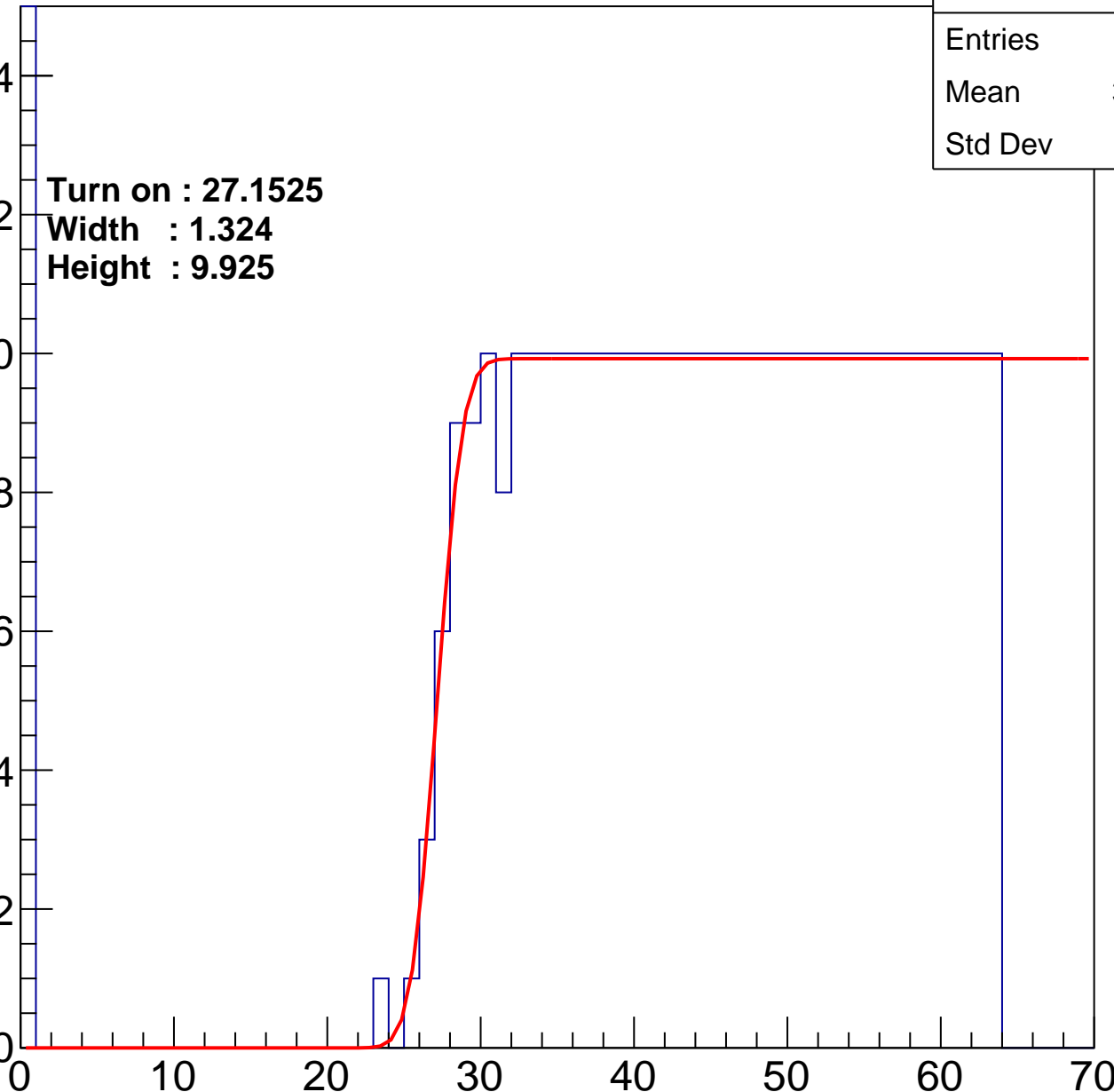
Width : 1.324

Height : 9.925

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch62

calib_packv5_041523_1651.root, FC#0, port C2

Entries	423
Mean	39.76
Std Dev	17.27

Turn on : 26.7462

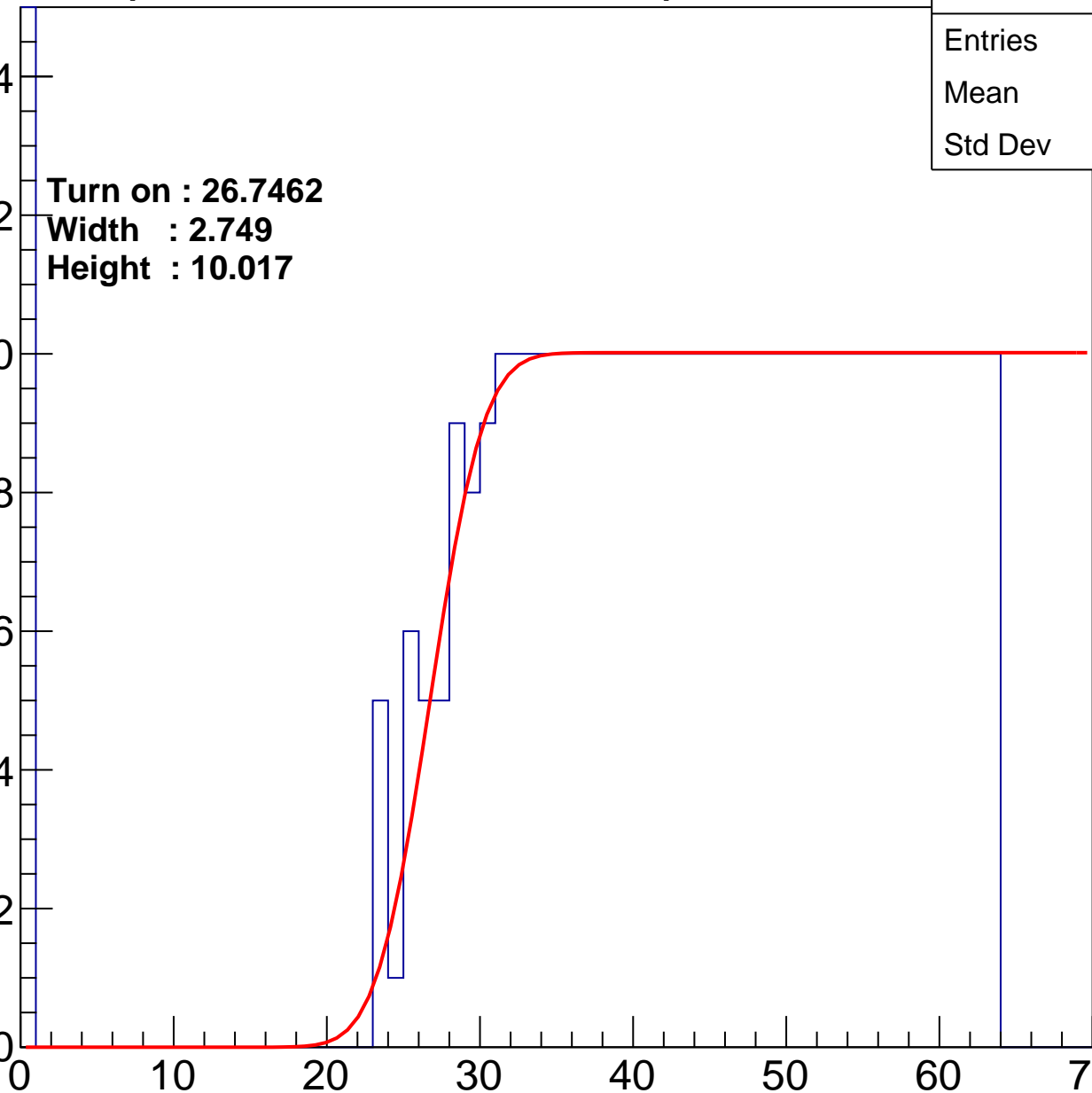
Width : 2.749

Height : 10.017

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch63

calib_packv5_041523_1651.root, FC#0, port C2

Entries	403
Mean	40.93
Std Dev	16.64

Turn on : 27.9125

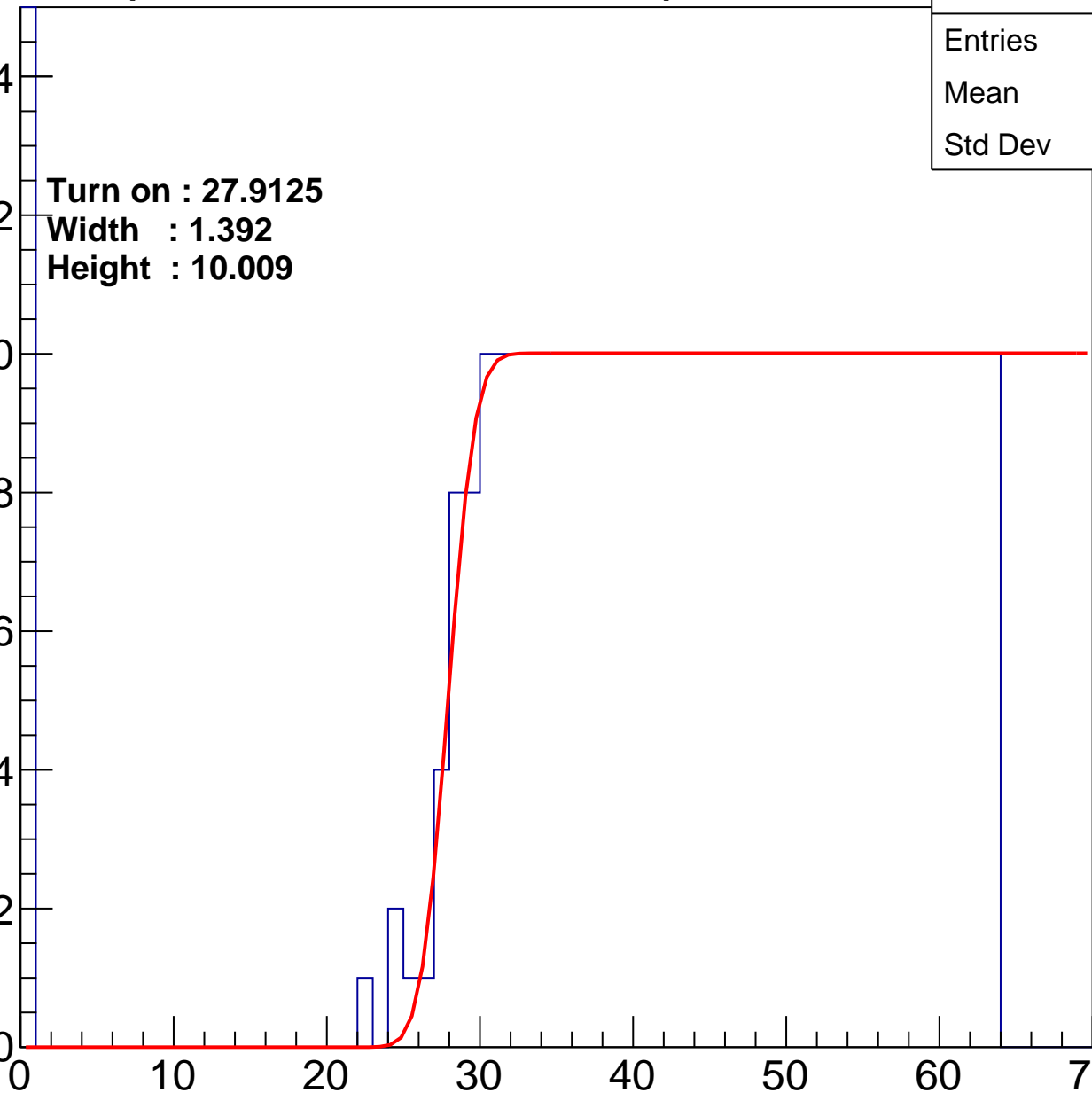
Width : 1.392

Height : 10.009

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch64

calib_packv5_041523_1651.root, FC#0, port C2

Entries	441
Mean	38.88
Std Dev	17.59

Turn on : 25.3797

Width : 2.453

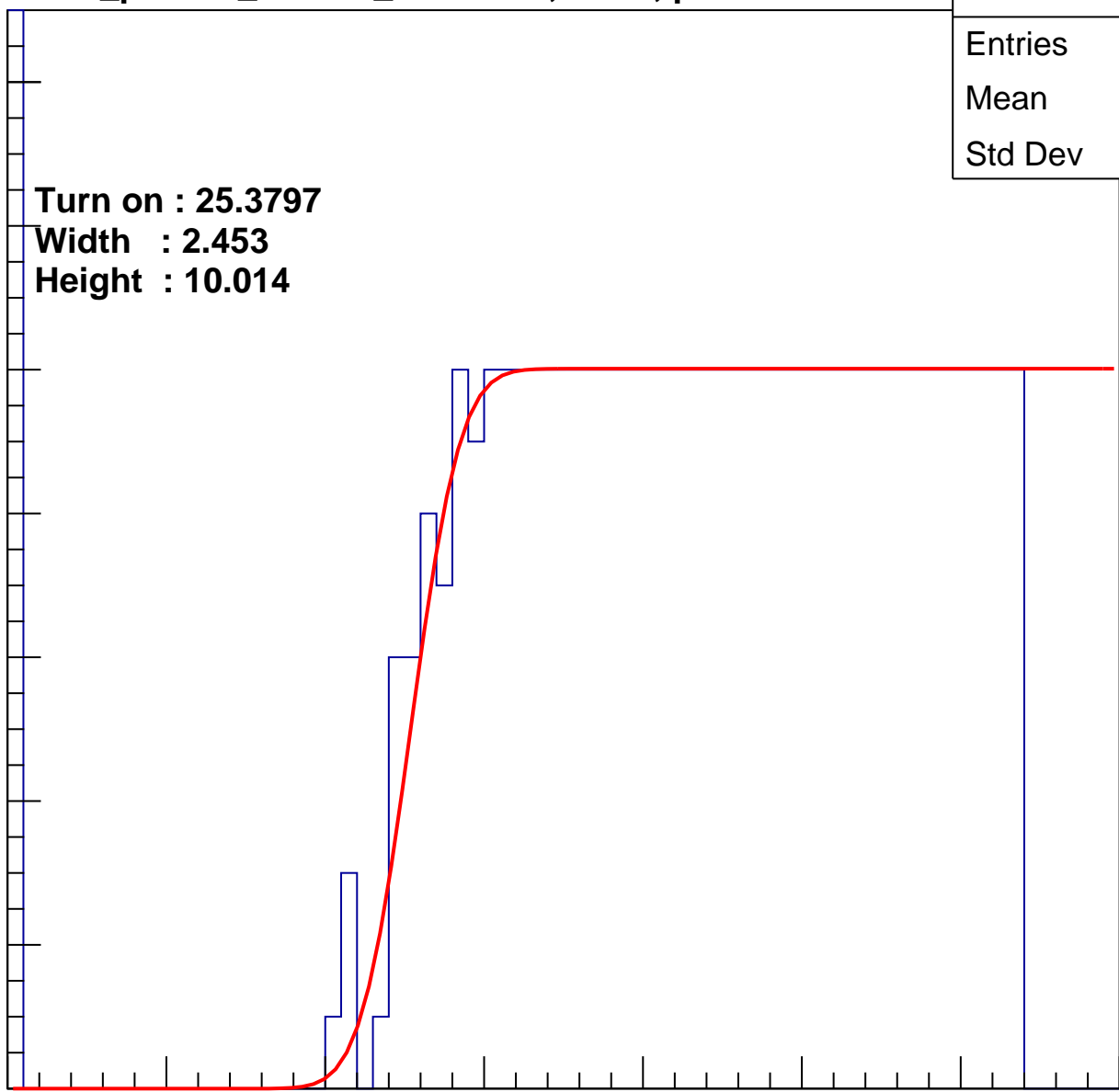
Height : 10.014

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L103S, U12-ch65

calib_packv5_041523_1651.root, FC#0, port C2

Entries	420
Mean	39.59
Std Dev	17.73

Turn on : 27.1750

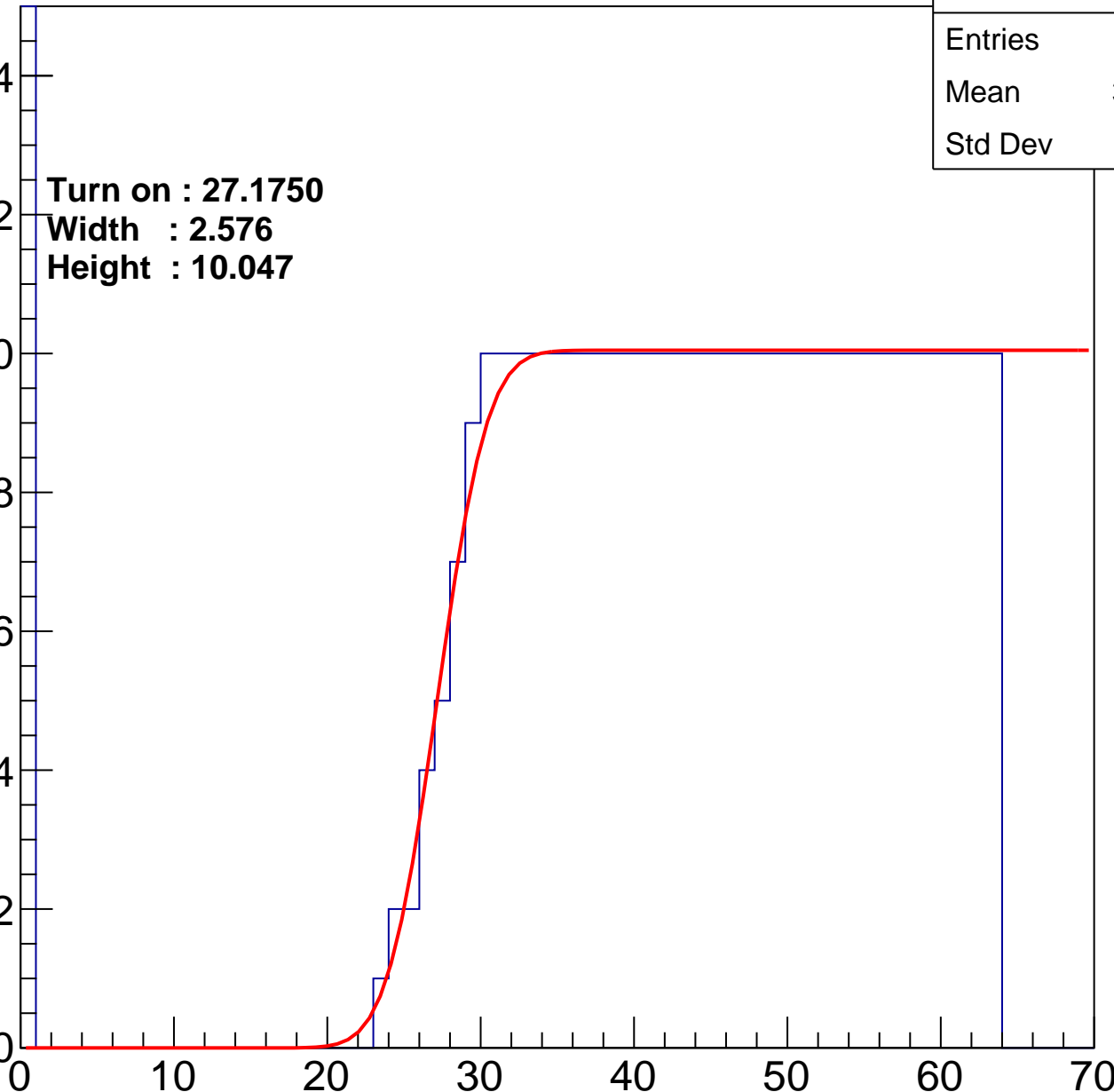
Width : 2.576

Height : 10.047

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch66

calib_packv5_041523_1651.root, FC#0, port C2

Entries	449
Mean	38.55
Std Dev	17.64

Turn on : 24.2225

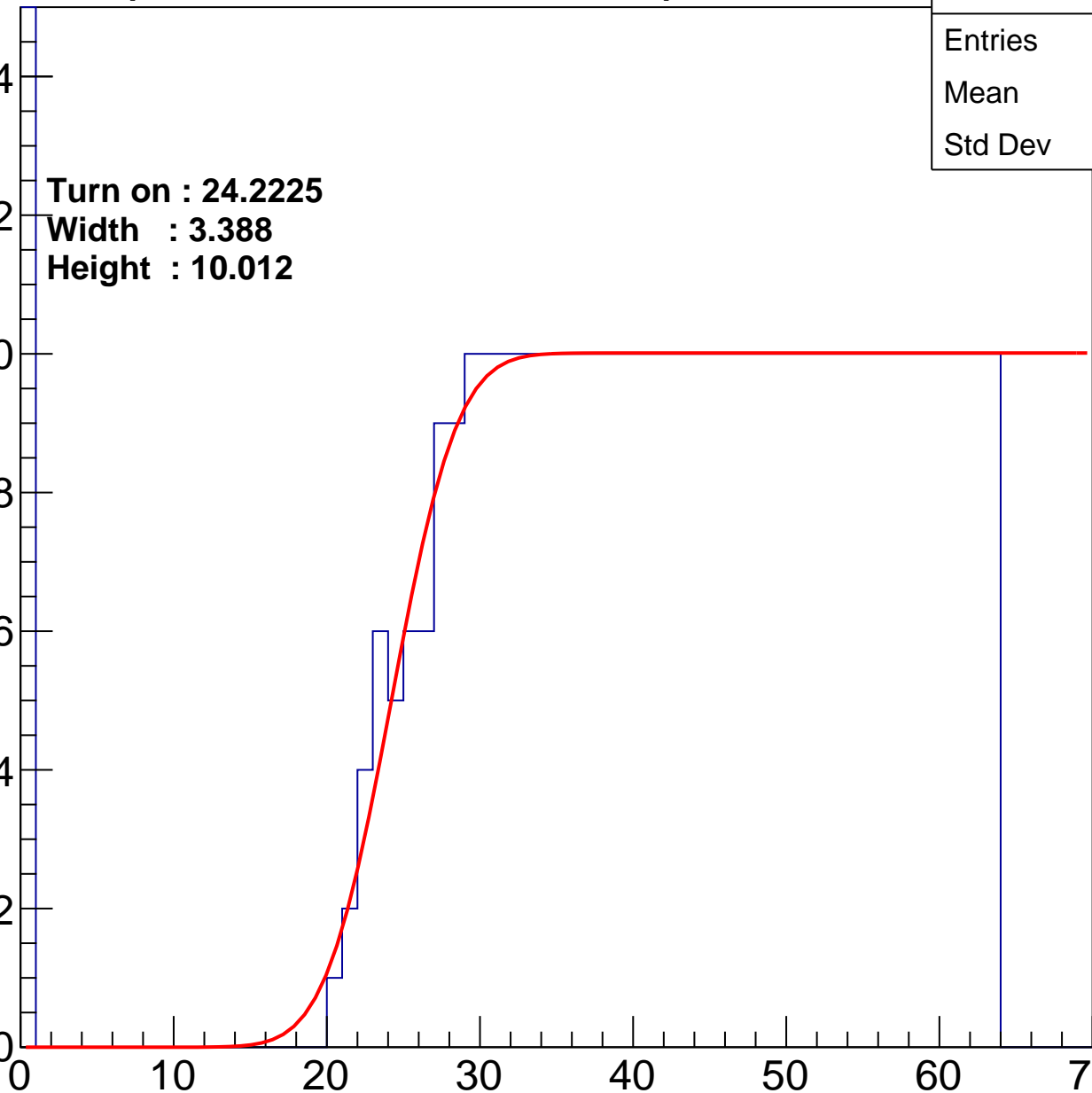
Width : 3.388

Height : 10.012

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch67

calib_packv5_041523_1651.root, FC#0, port C2

Entries	421
Mean	39.56
Std Dev	17.71

Turn on : 27.1874

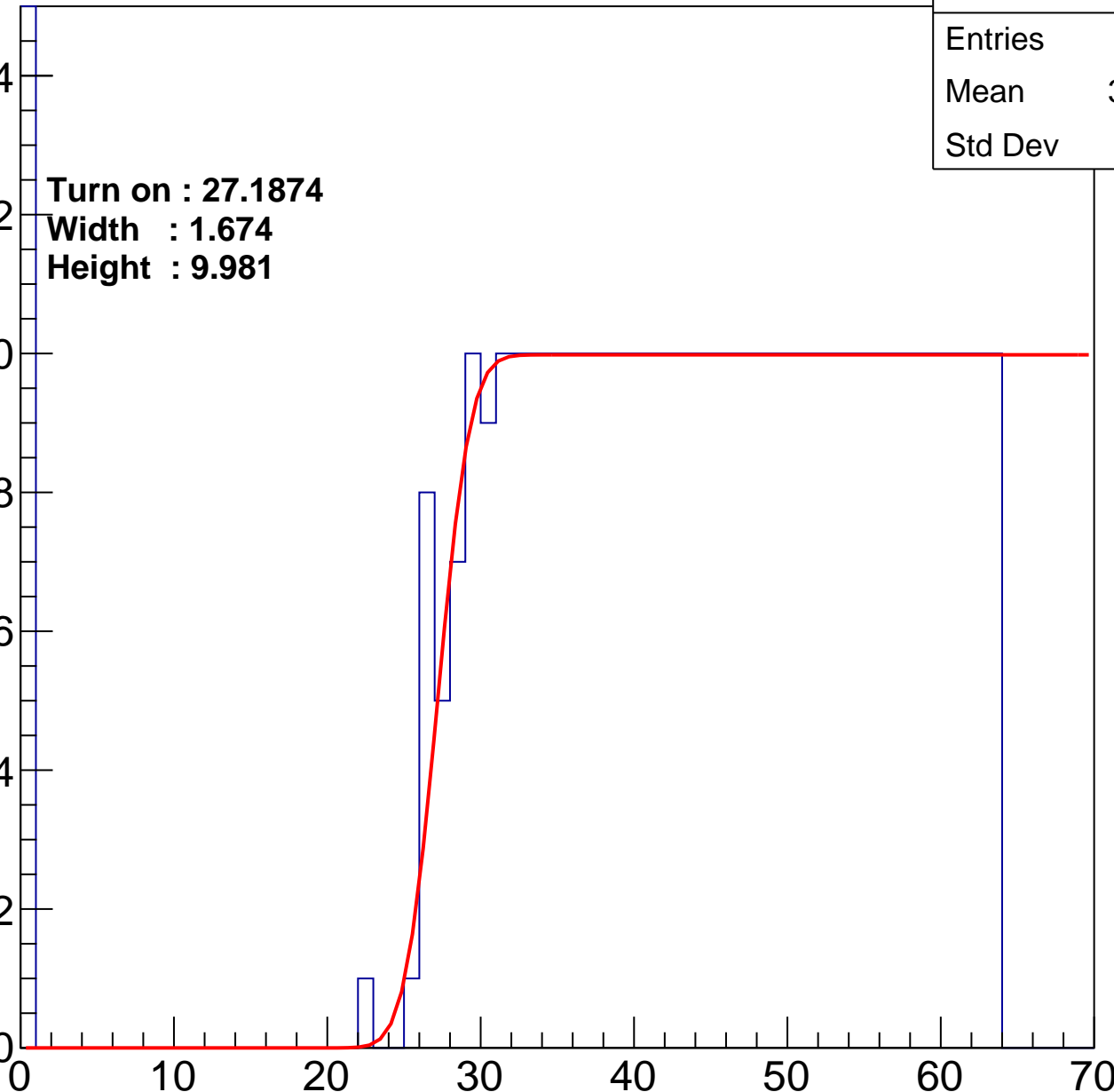
Width : 1.674

Height : 9.981

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch68

calib_packv5_041523_1651.root, FC#0, port C2

Entries	430
Mean	39.29
Std Dev	17.59

Turn on : 26.1765

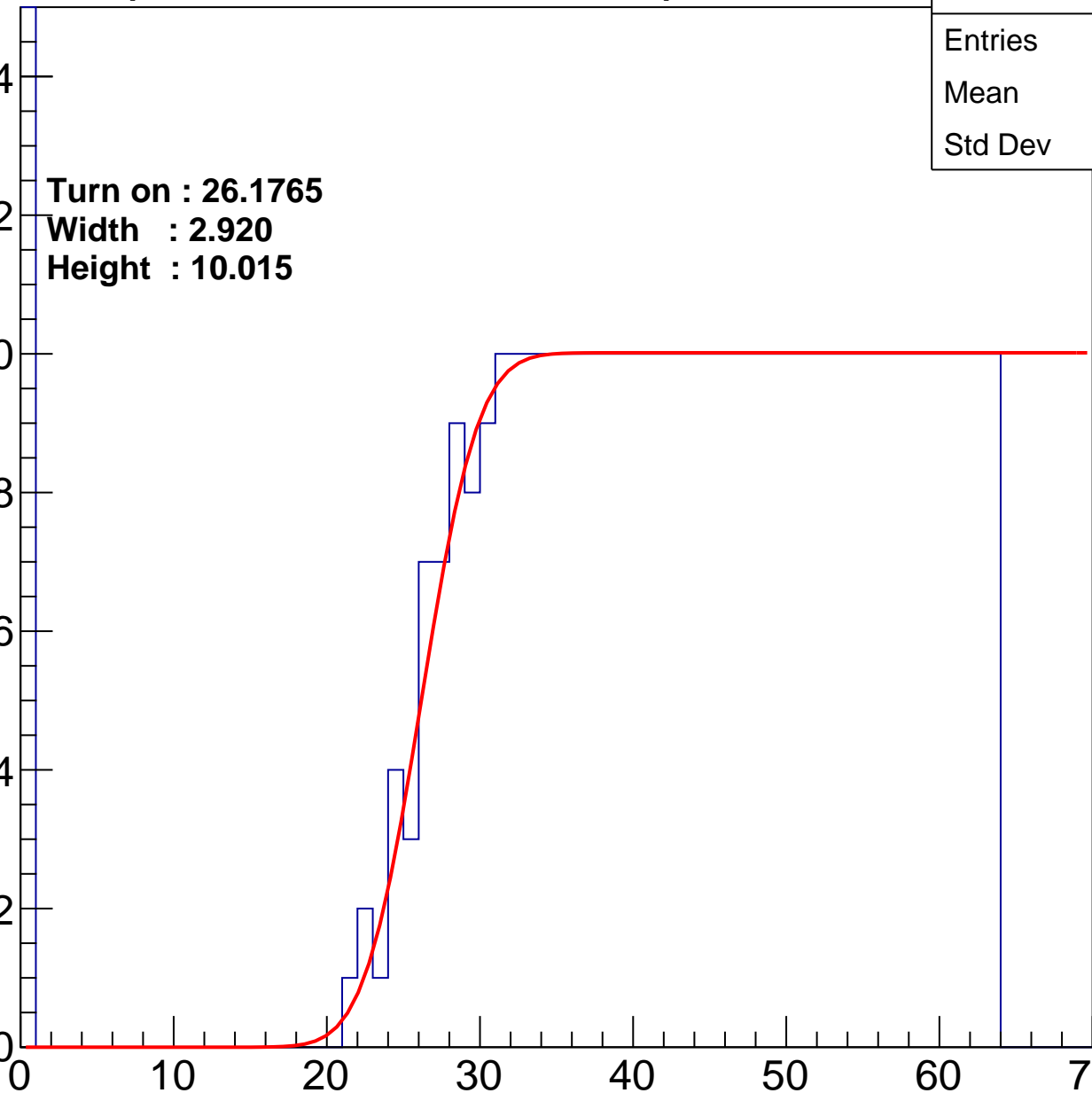
Width : 2.920

Height : 10.015

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch69

calib_packv5_041523_1651.root, FC#0, port C2

Entries	413
Mean	40.18
Std Dev	17.22

Turn on : 27.4730

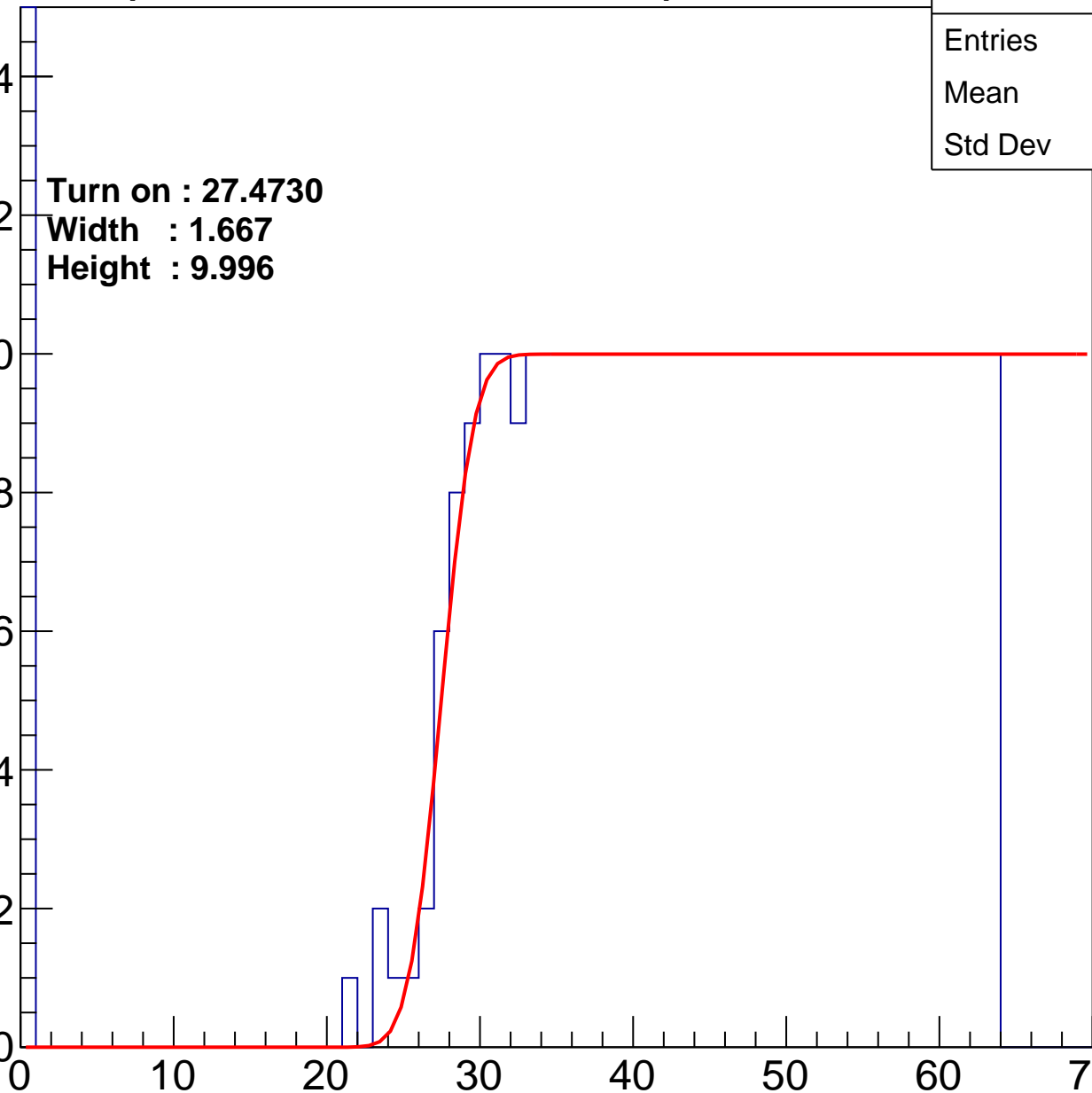
Width : 1.667

Height : 9.996

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch70

calib_packv5_041523_1651.root, FC#0, port C2

Entries	418
Mean	39.78
Std Dev	17.51

Turn on : 27.0568

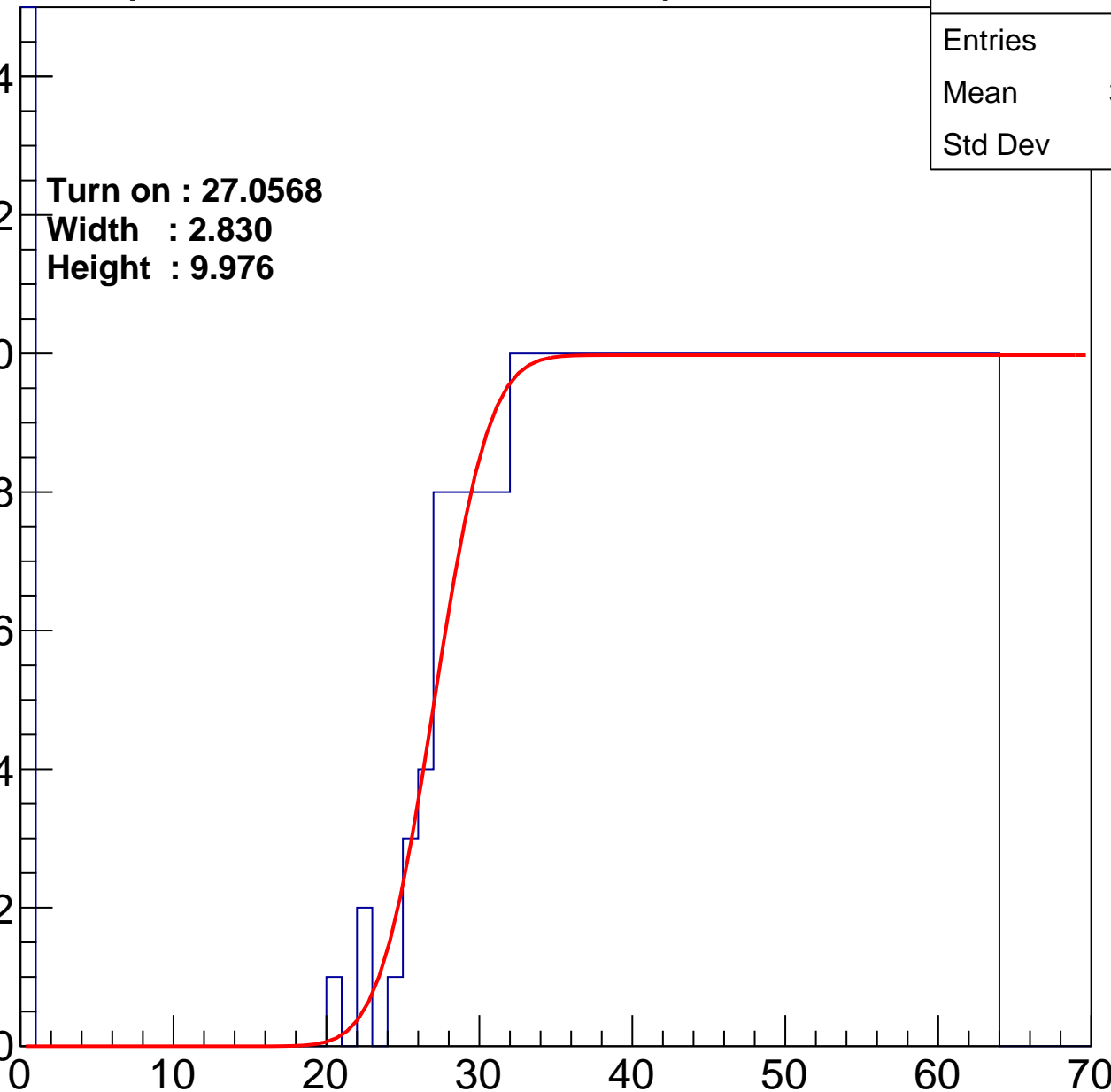
Width : 2.830

Height : 9.976

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch71

calib_packv5_041523_1651.root, FC#0, port C2

Entries	419
Mean	39.97
Std Dev	17.18

Turn on : 26.4581

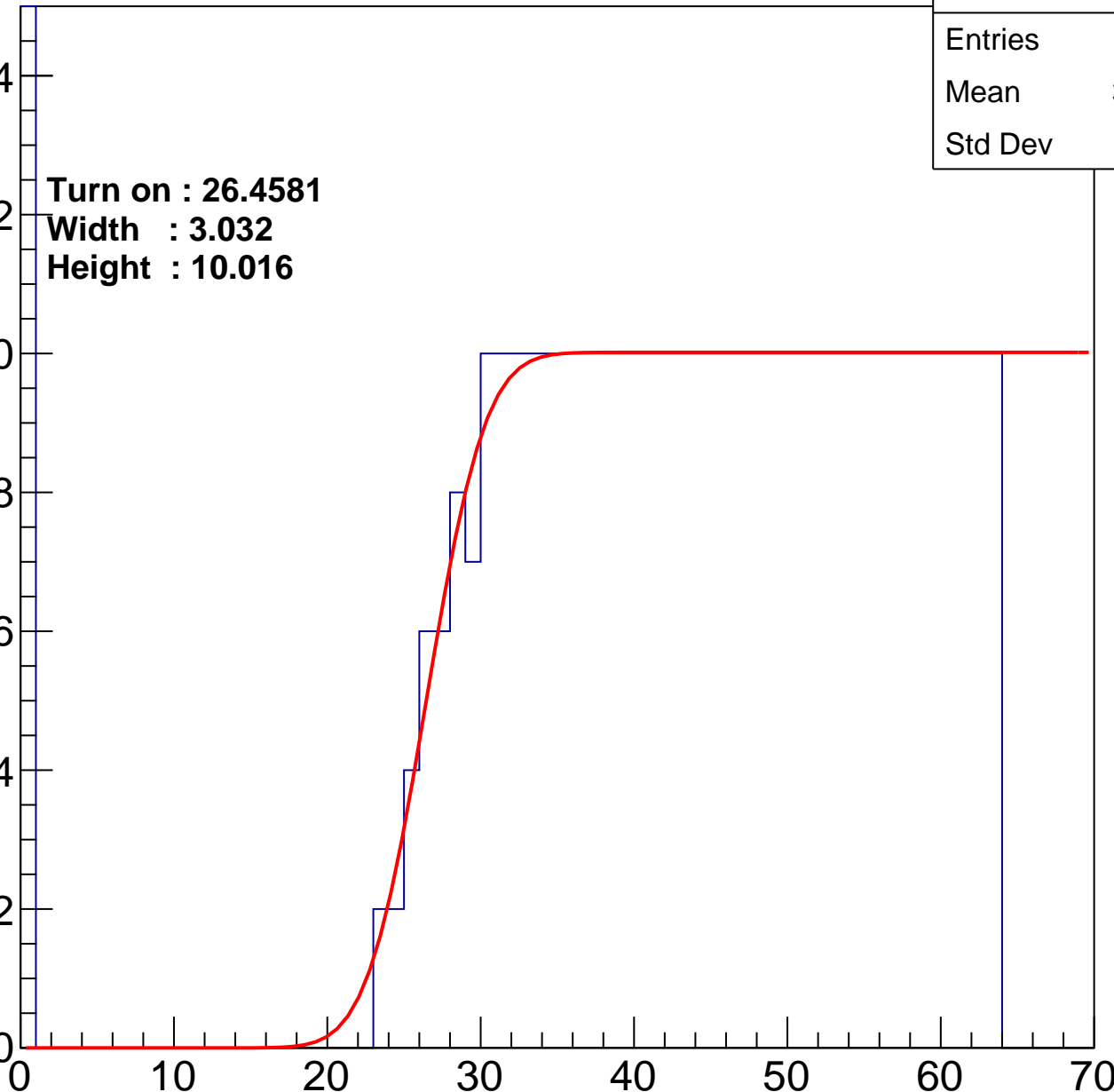
Width : 3.032

Height : 10.016

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch72

calib_packv5_041523_1651.root, FC#0, port C2

Entries	436
Mean	38.95
Std Dev	17.78

Turn on : 25.6316

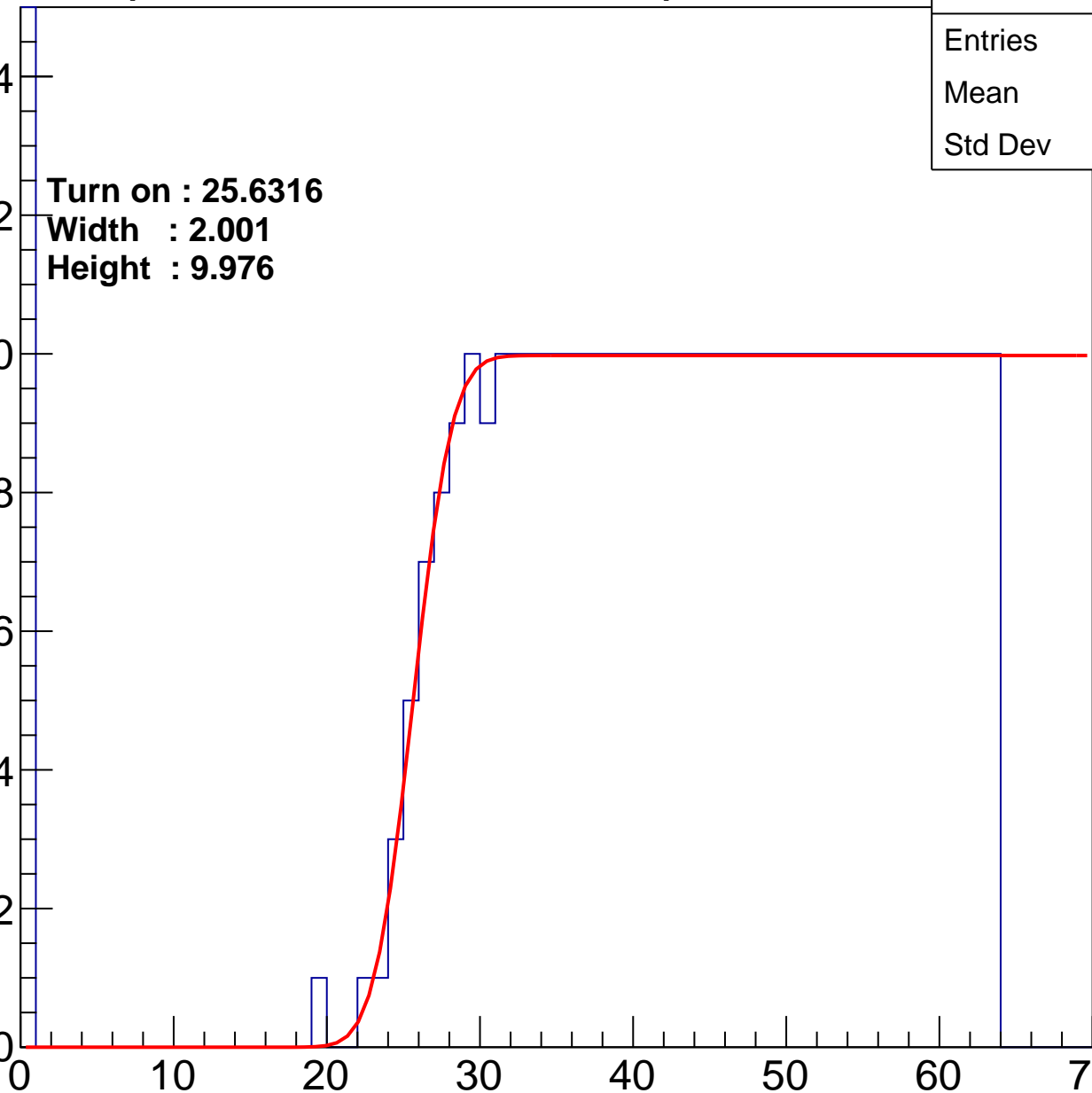
Width : 2.001

Height : 9.976

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch73

calib_packv5_041523_1651.root, FC#0, port C2

Entries	435
Mean	39.76
Std Dev	16.56

Turn on : 24.6531

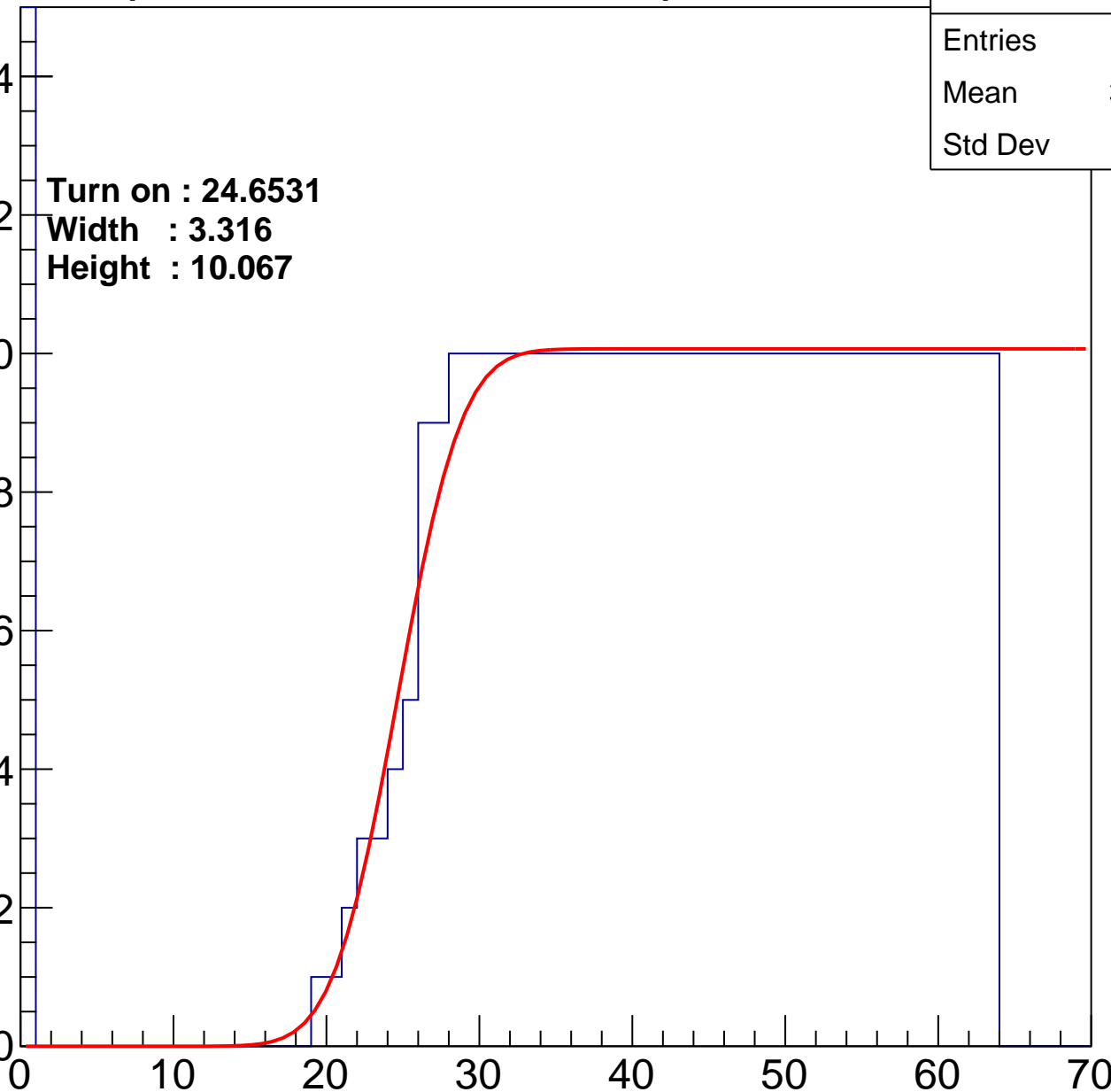
Width : 3.316

Height : 10.067

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch74

calib_packv5_041523_1651.root, FC#0, port C2

Entries	451
Mean	38.16
Std Dev	18.1

Turn on : 25.0691

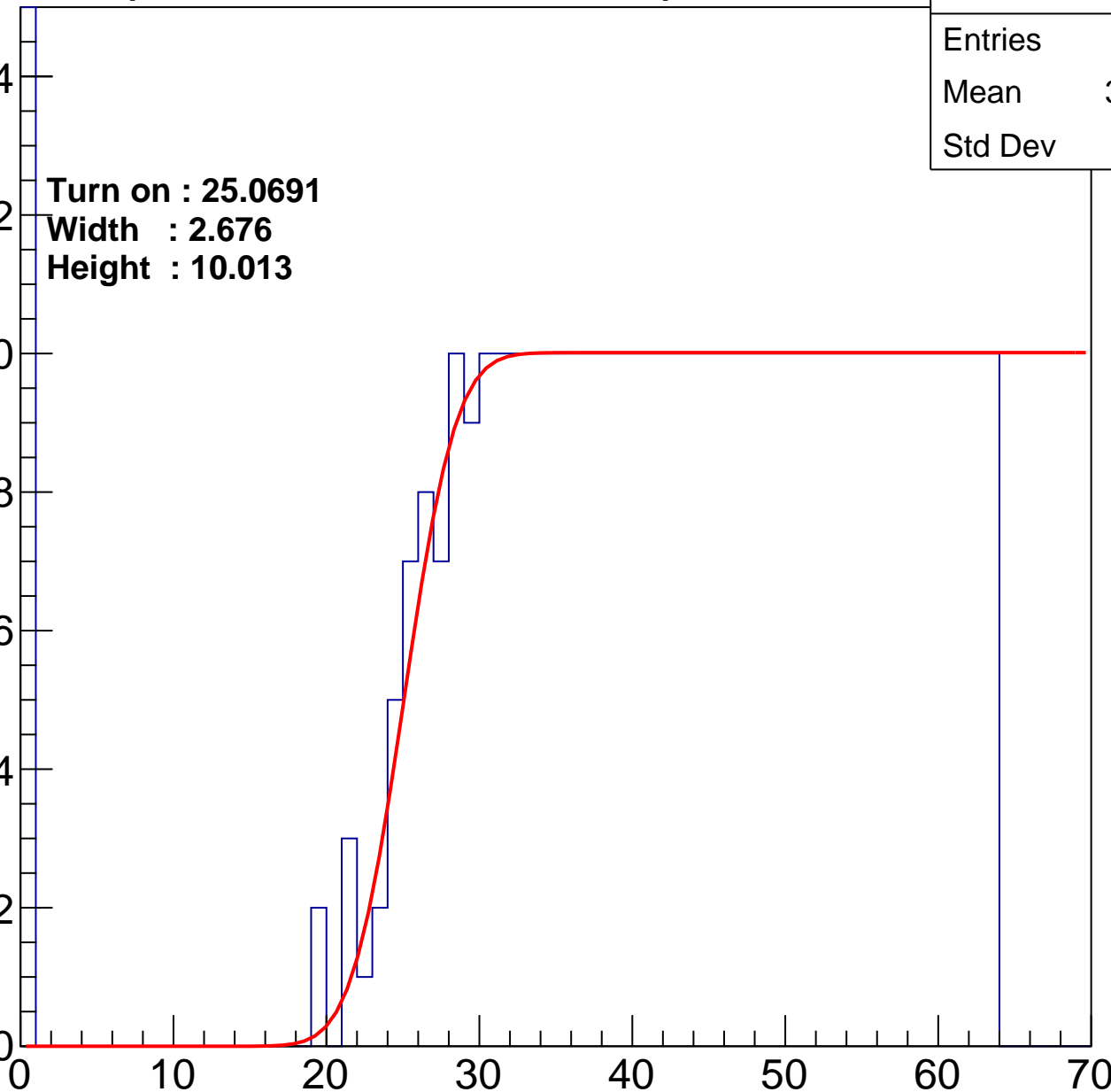
Width : 2.676

Height : 10.013

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch75

calib_packv5_041523_1651.root, FC#0, port C2

Entries	411
Mean	40.42
Std Dev	16.94

Turn on : 27.4470

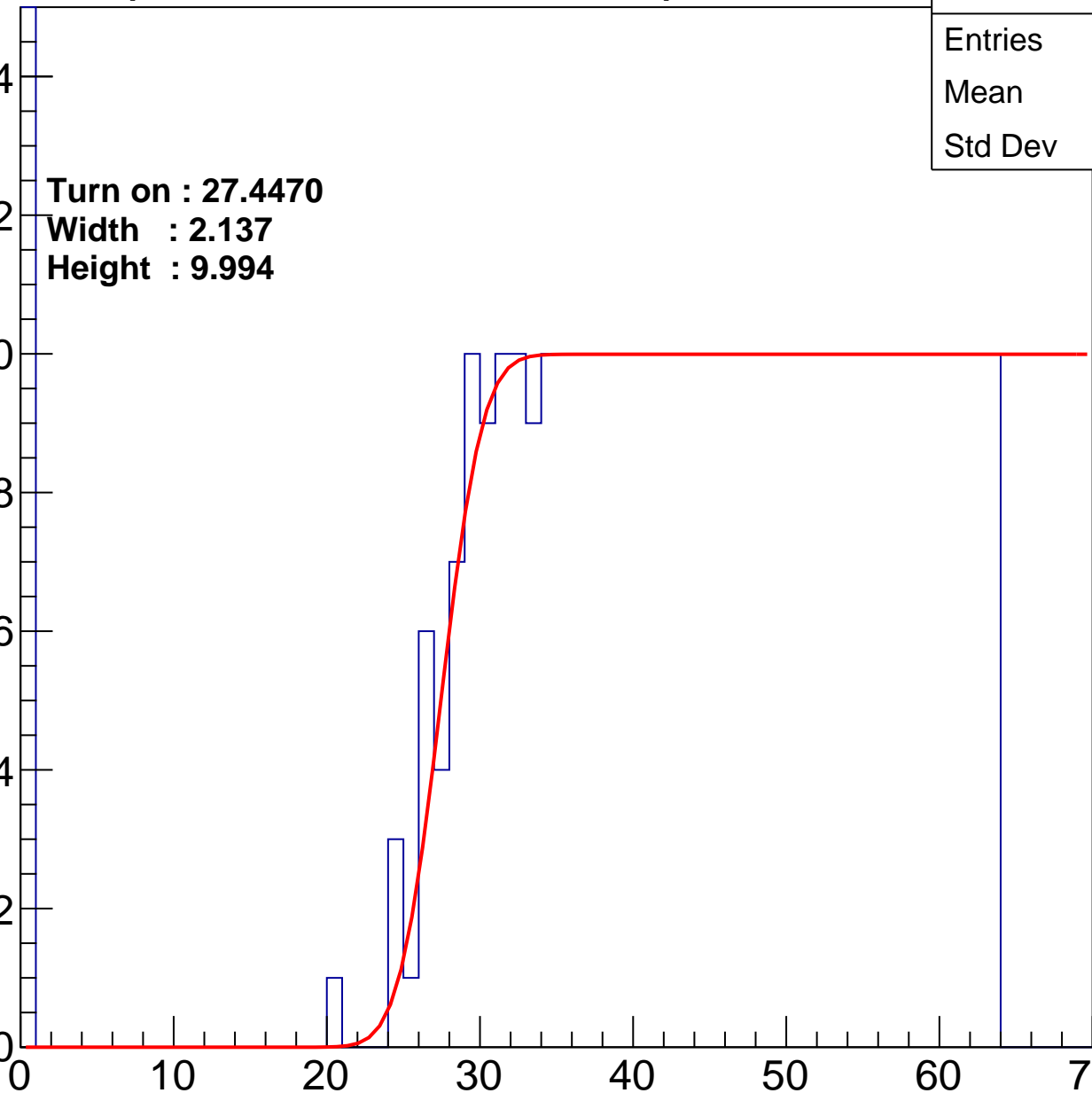
Width : 2.137

Height : 9.994

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch76

calib_packv5_041523_1651.root, FC#0, port C2

Entries	454
Mean	38.01
Std Dev	18.16

Turn on : 24.1187

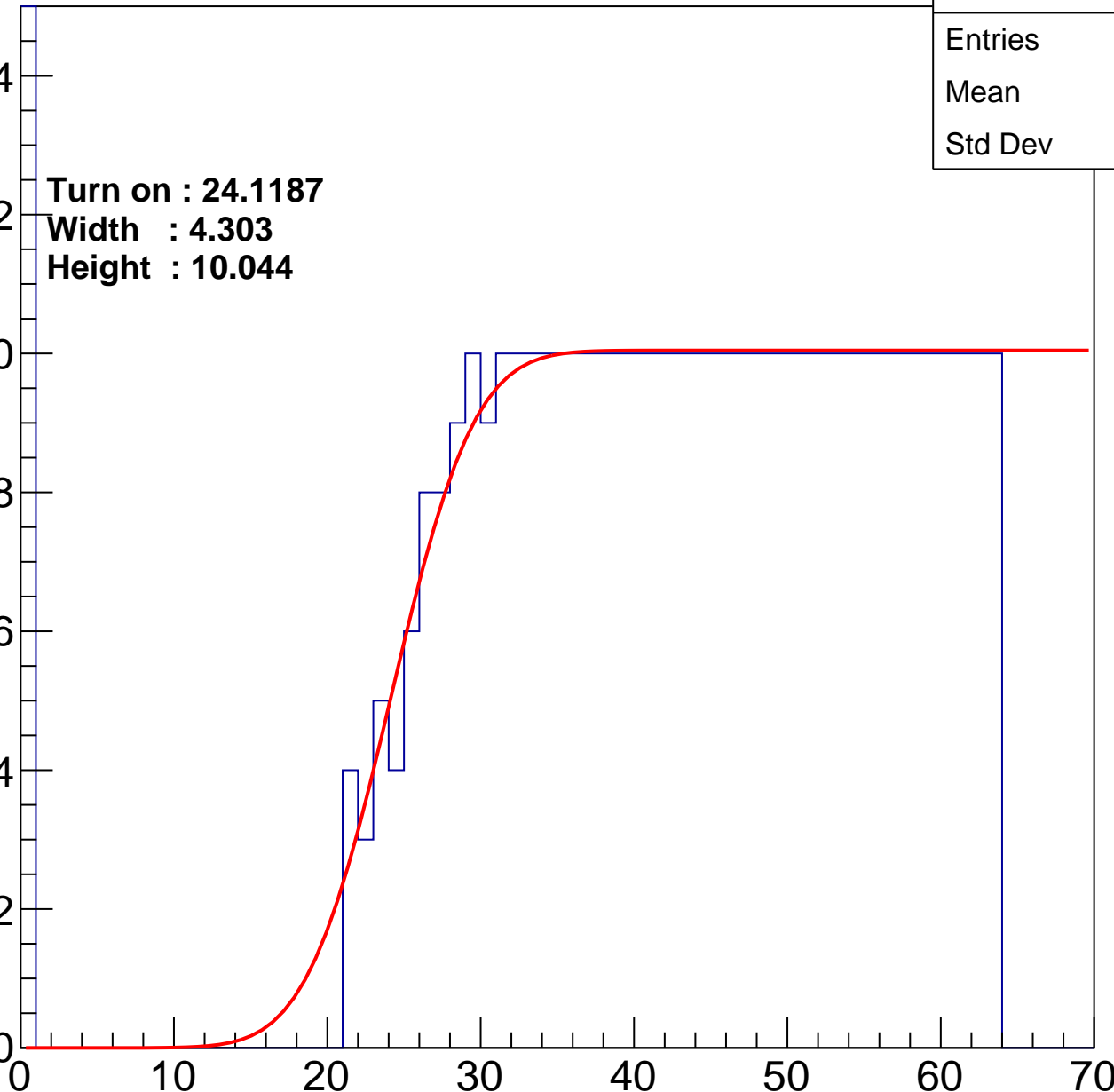
Width : 4.303

Height : 10.044

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch77

calib_packv5_041523_1651.root, FC#0, port C2

Entries	414
Mean	40.33
Std Dev	16.91

Turn on : 27.1717

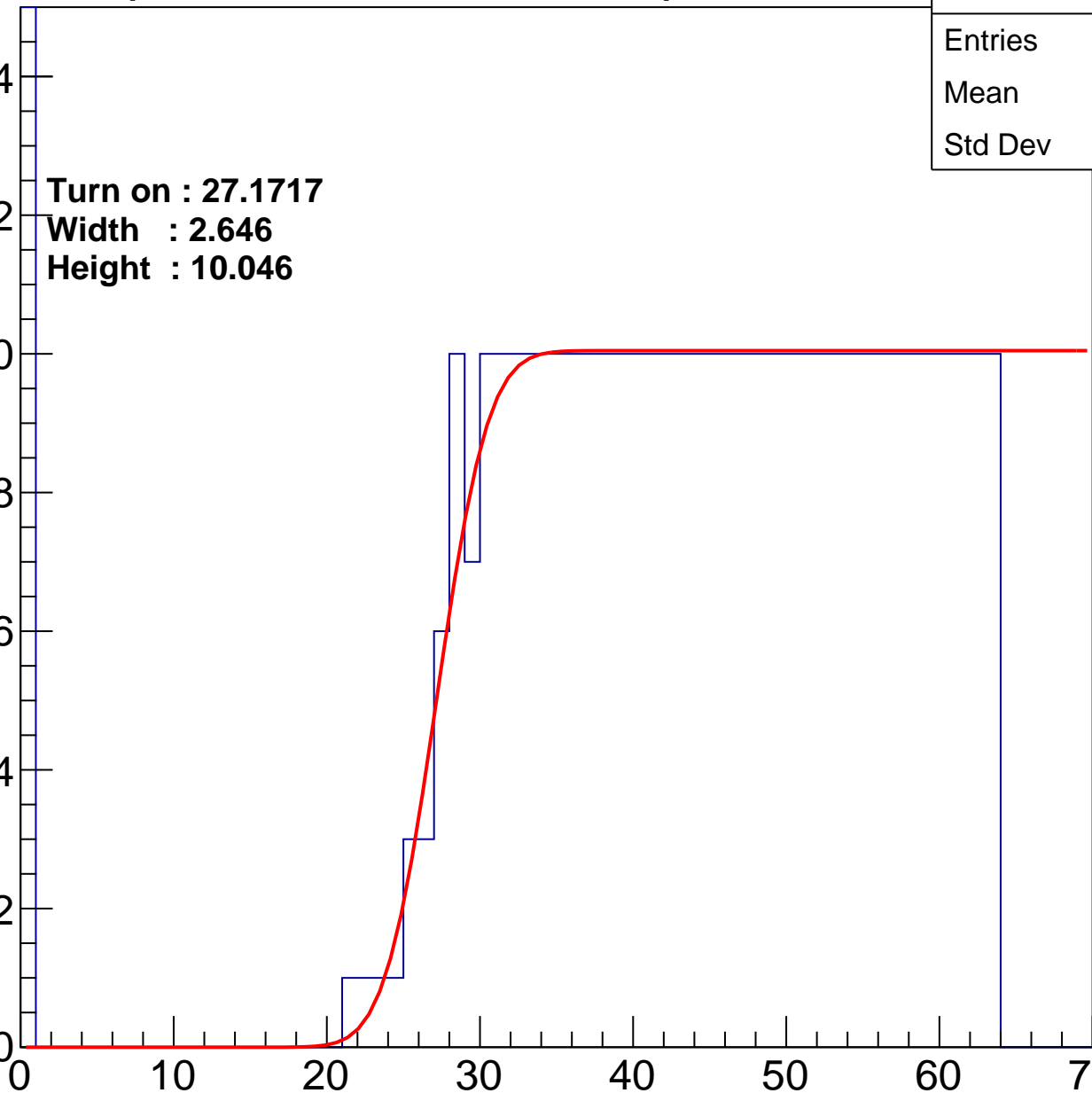
Width : 2.646

Height : 10.046

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch78

calib_packv5_041523_1651.root, FC#0, port C2

Entries	444
Mean	39
Std Dev	17.24

Turn on : 24.3277

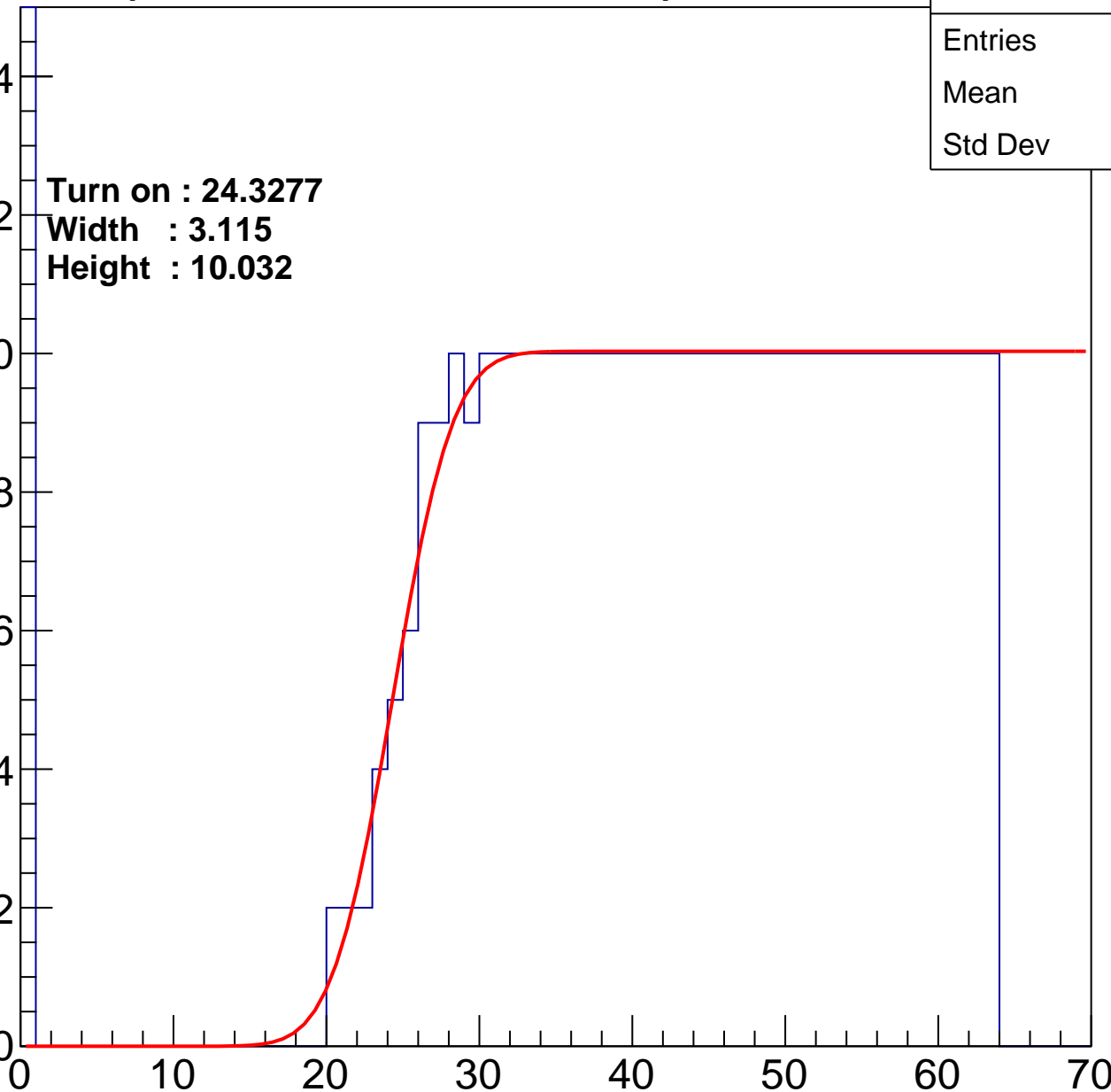
Width : 3.115

Height : 10.032

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch79

calib_packv5_041523_1651.root, FC#0, port C2

Entries	428
Mean	39.4
Std Dev	17.53

Turn on : 26.5395

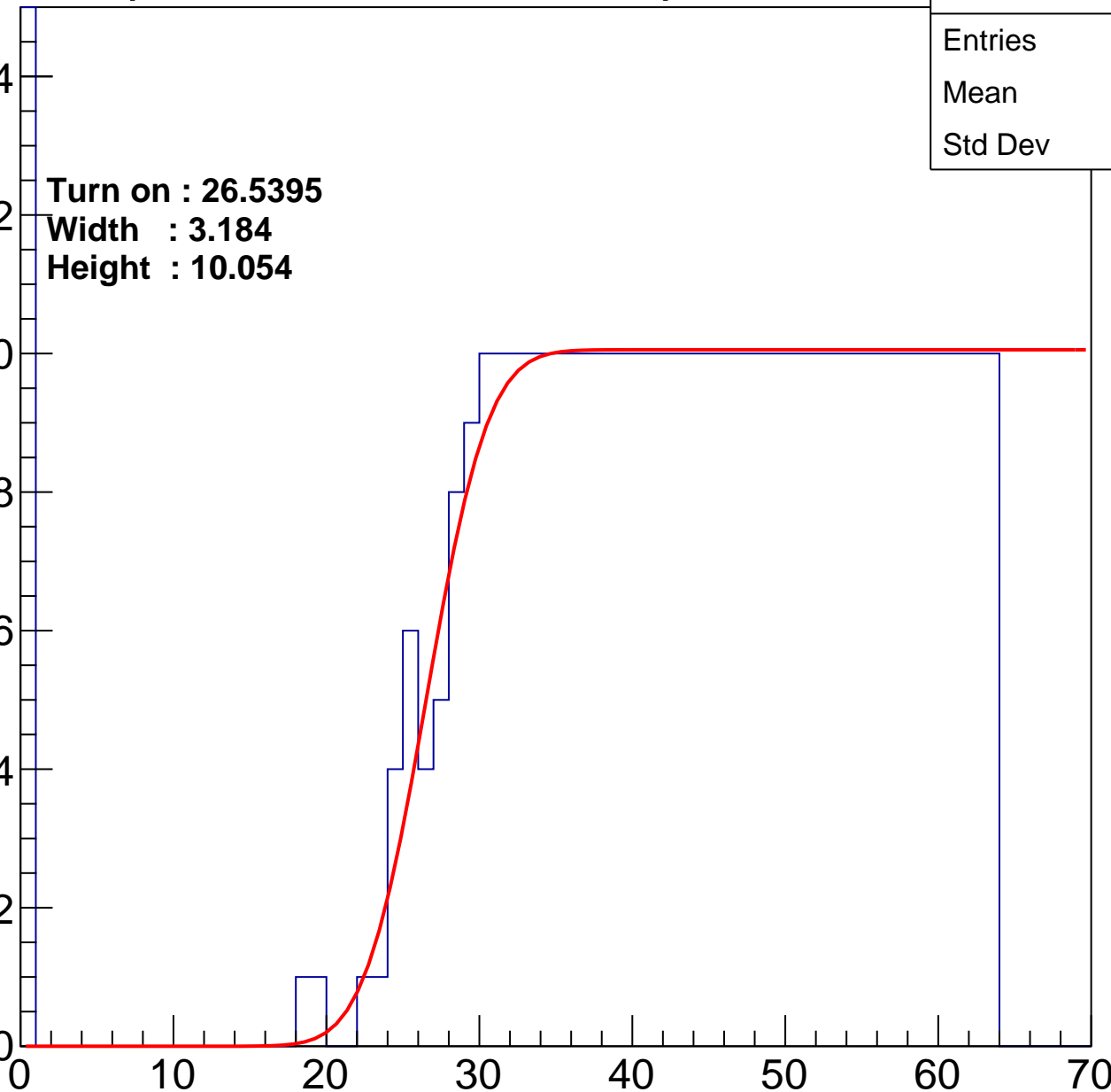
Width : 3.184

Height : 10.054

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch80

calib_packv5_041523_1651.root, FC#0, port C2

Entries	433
Mean	39.25
Std Dev	17.48

Turn on : 25.6926

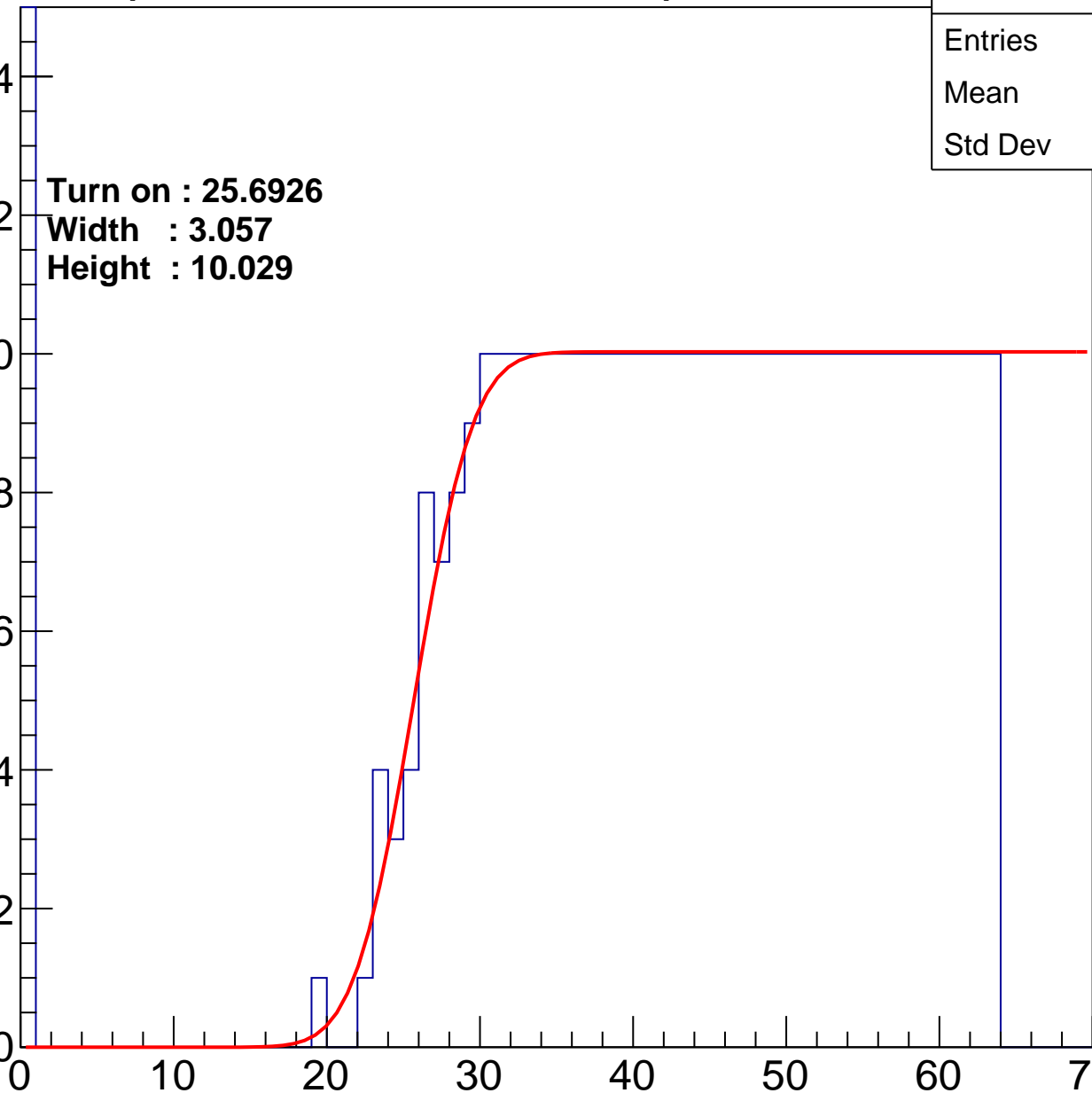
Width : 3.057

Height : 10.029

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch81

calib_packv5_041523_1651.root, FC#0, port C2

Entries	457
Mean	37.53
Std Dev	18.7

Turn on : 25.5127

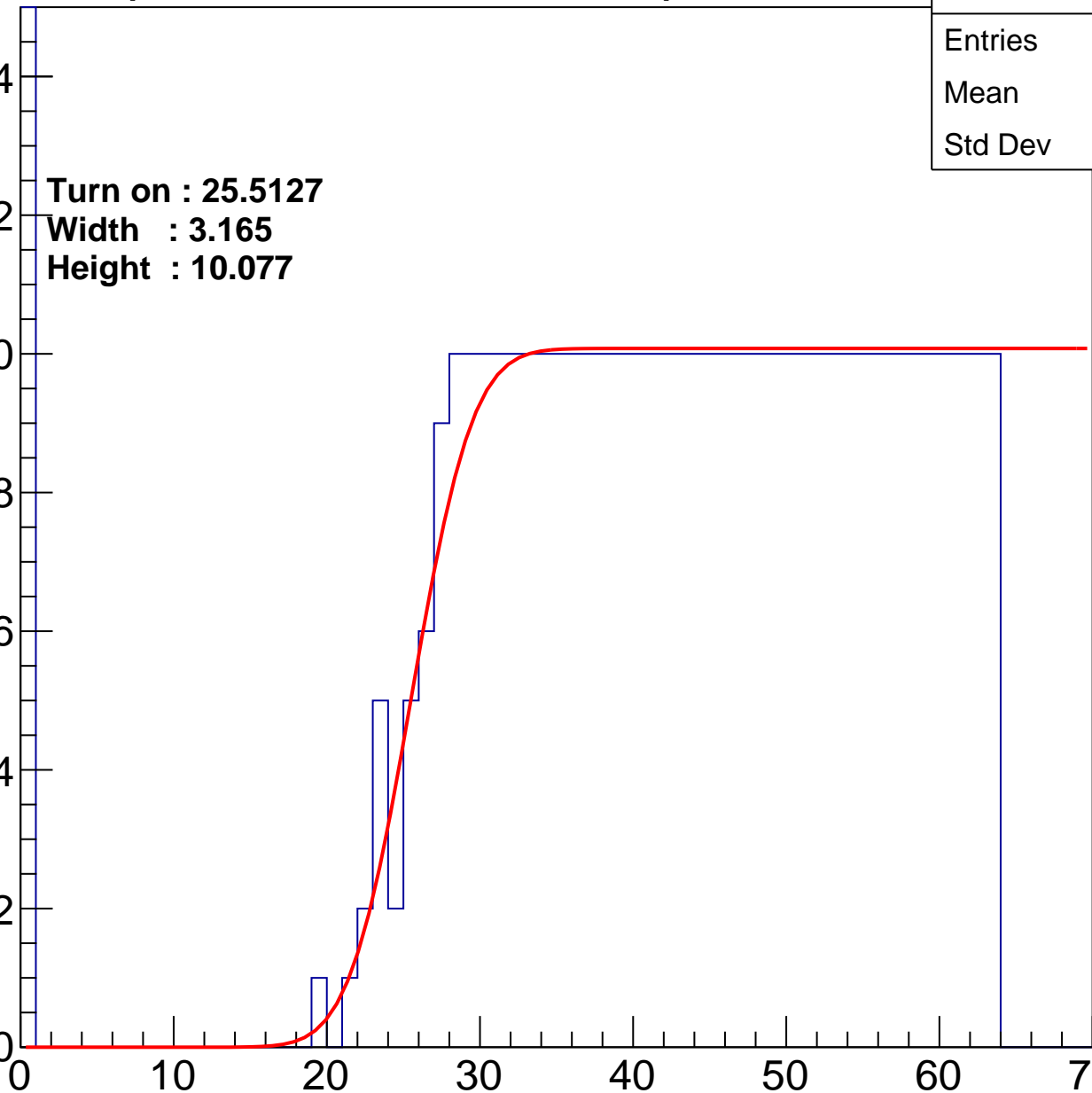
Width : 3.165

Height : 10.077

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch82

calib_packv5_041523_1651.root, FC#0, port C2

Entries	532
Mean	32.37
Std Dev	21.4

Turn on : 25.4619

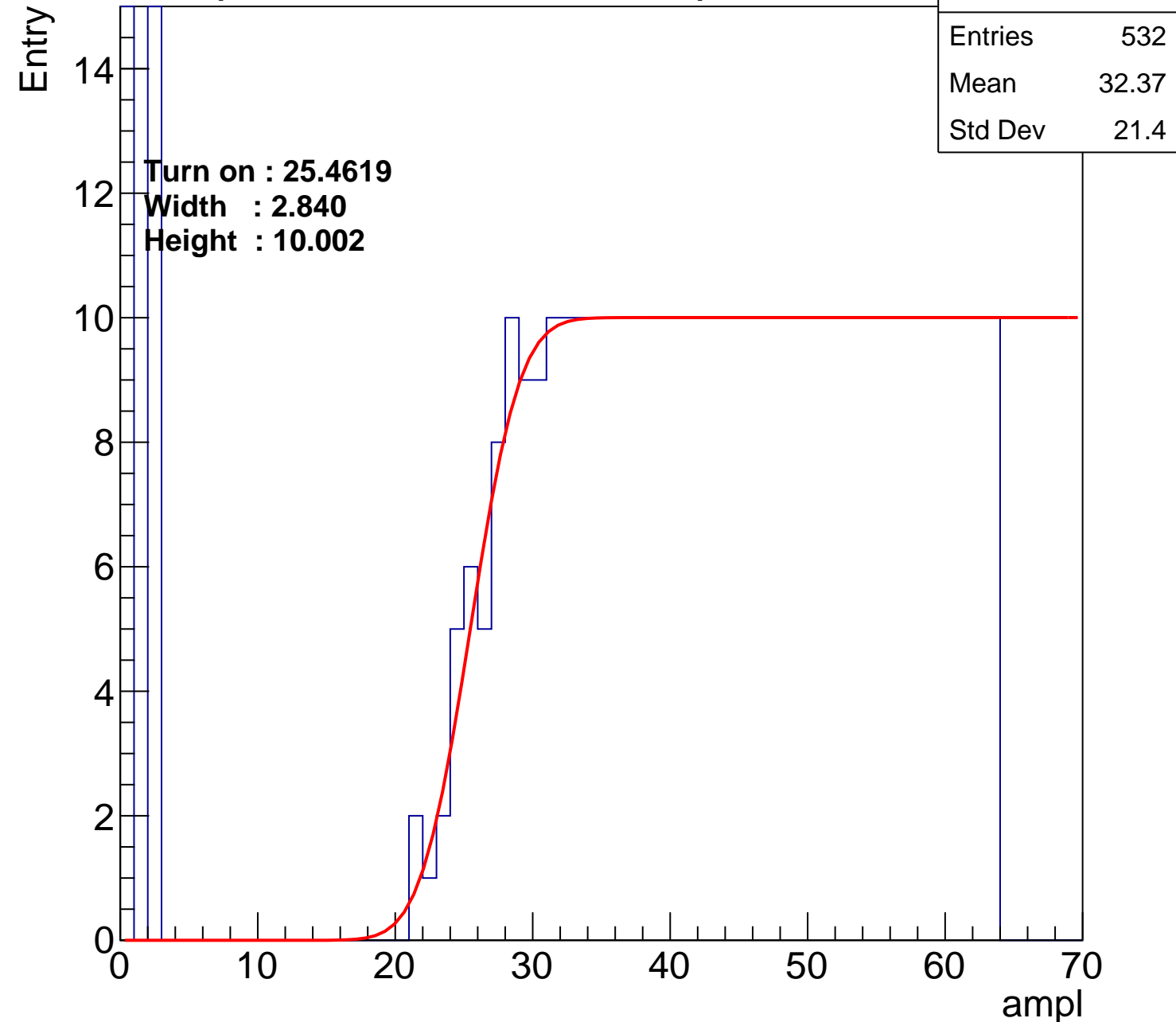
Width : 2.840

Height : 10.002

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch83

calib_packv5_041523_1651.root, FC#0, port C2

Entries	420
Mean	39.7
Std Dev	17.5

Turn on : 26.6440

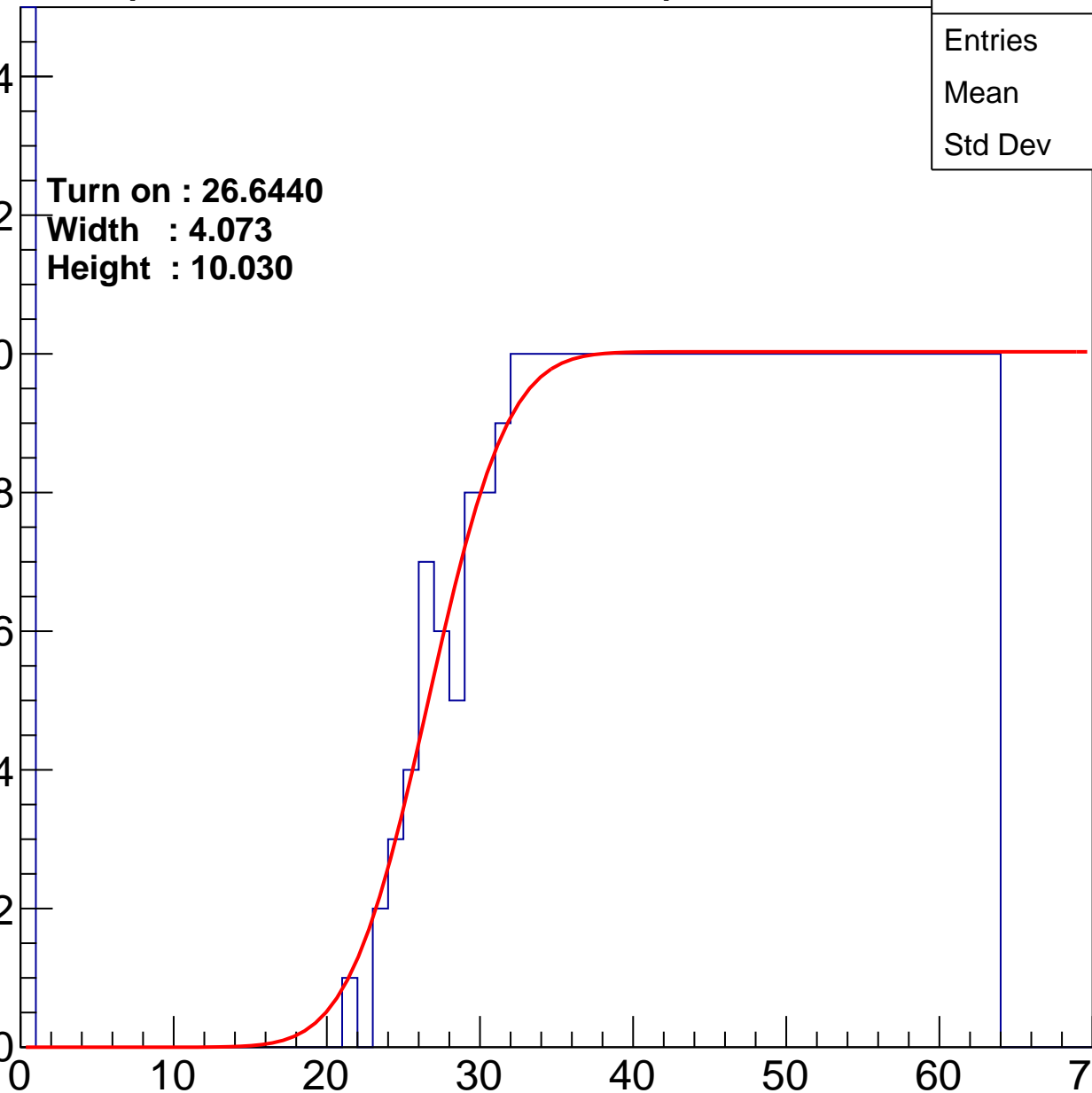
Width : 4.073

Height : 10.030

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch84

calib_packv5_041523_1651.root, FC#0, port C2

Entries	458
Mean	38.38
Std Dev	17.42

Turn on : 22.9423

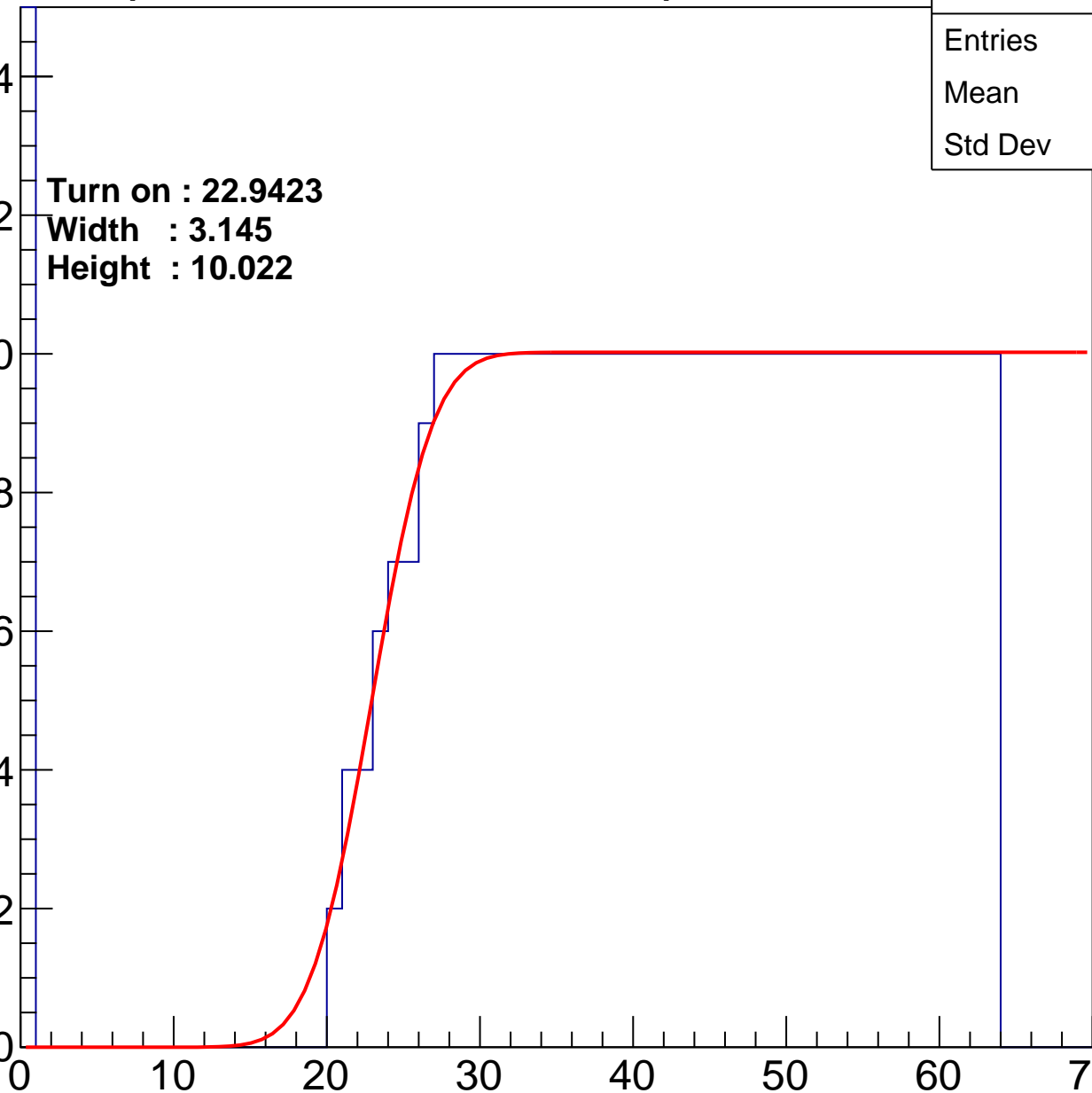
Width : 3.145

Height : 10.022

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch85

calib_packv5_041523_1651.root, FC#0, port C2

Entries	420
Mean	39.48
Std Dev	17.81

Turn on : 27.3377

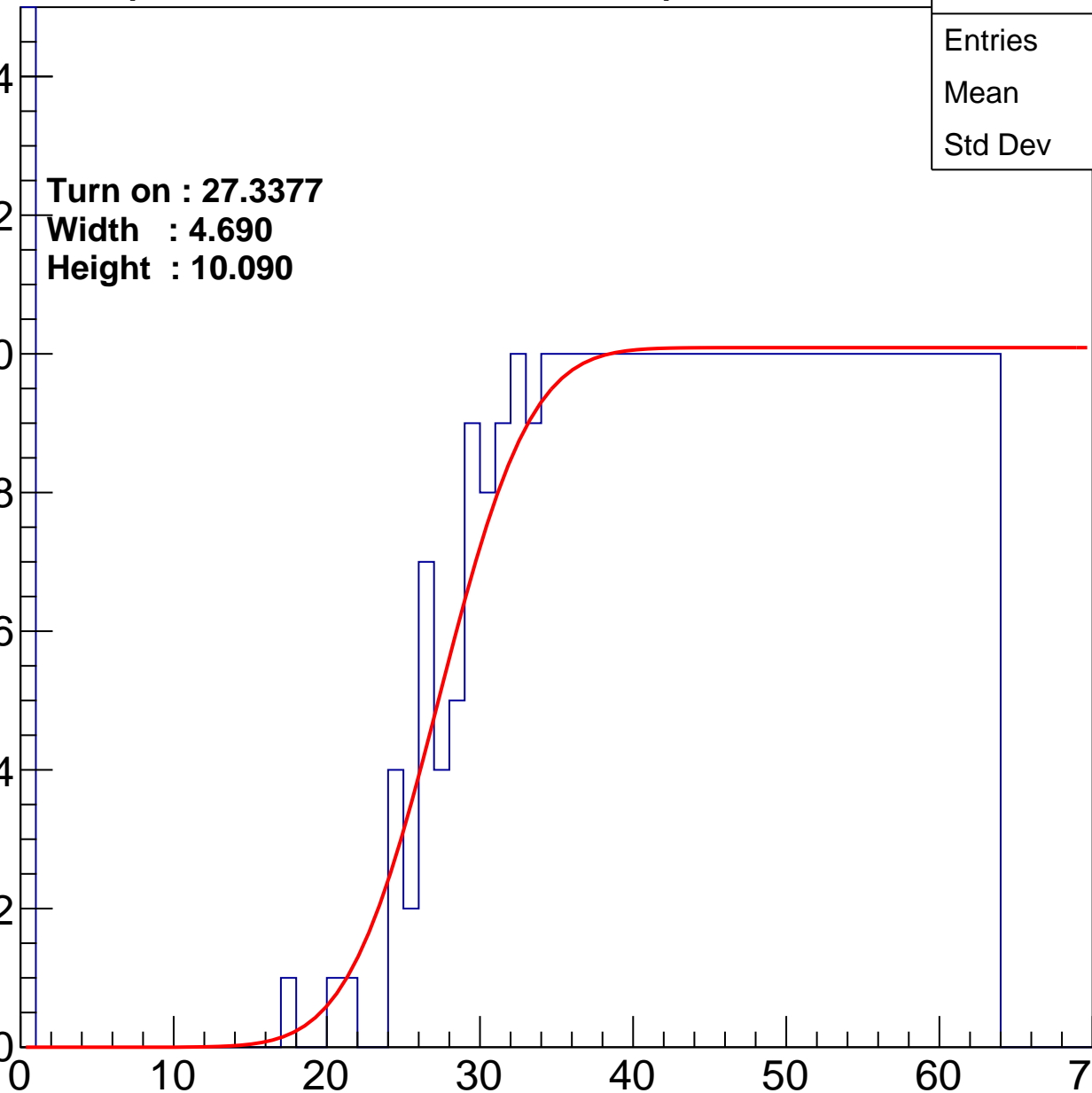
Width : 4.690

Height : 10.090

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch86

calib_packv5_041523_1651.root, FC#0, port C2

Entries	423
Mean	39.83
Std Dev	17.16

Turn on : 26.3243

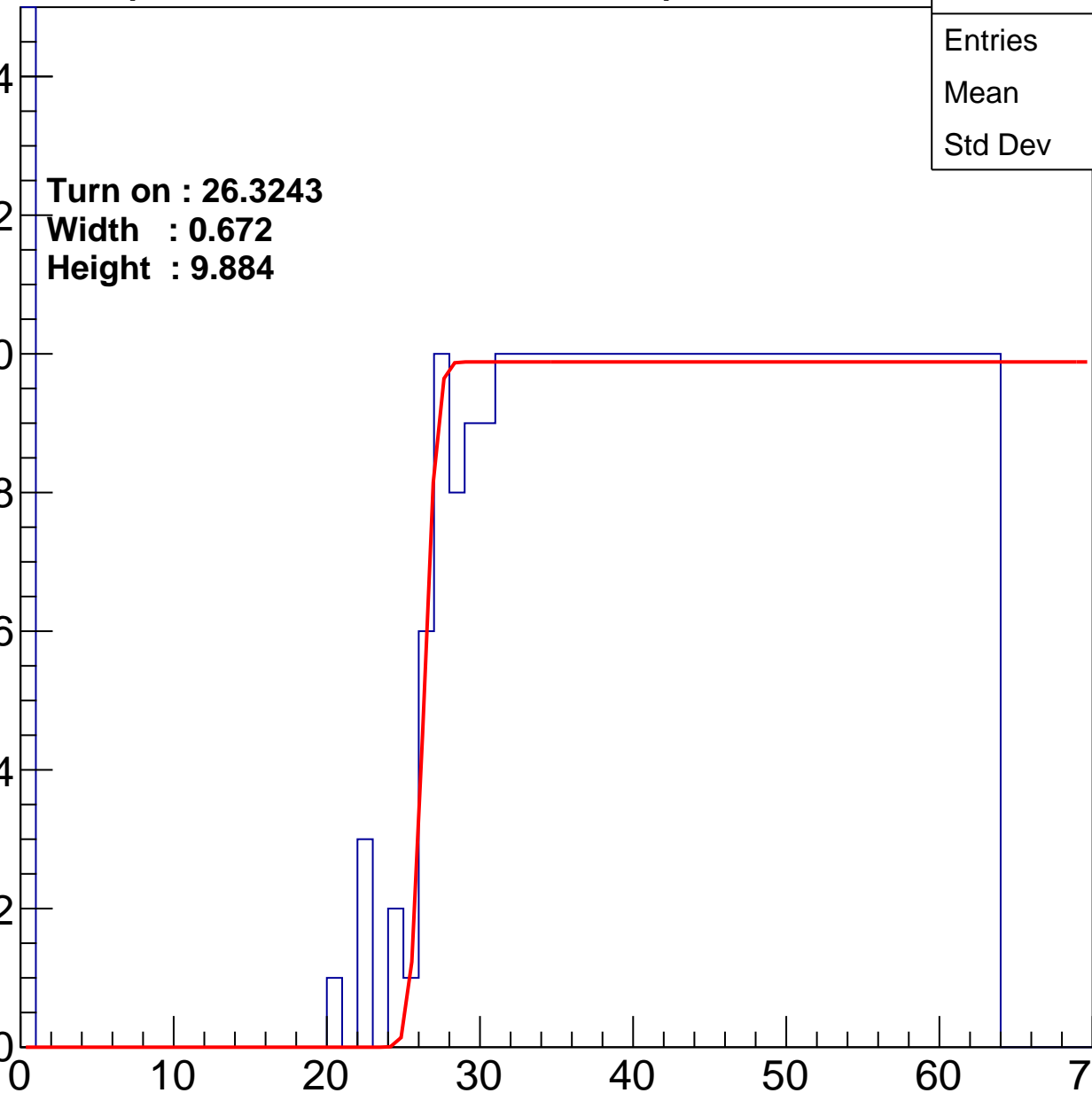
Width : 0.672

Height : 9.884

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch87

calib_packv5_041523_1651.root, FC#0, port C2

Entries	418
Mean	39.72
Std Dev	17.6

Turn on : 27.1818

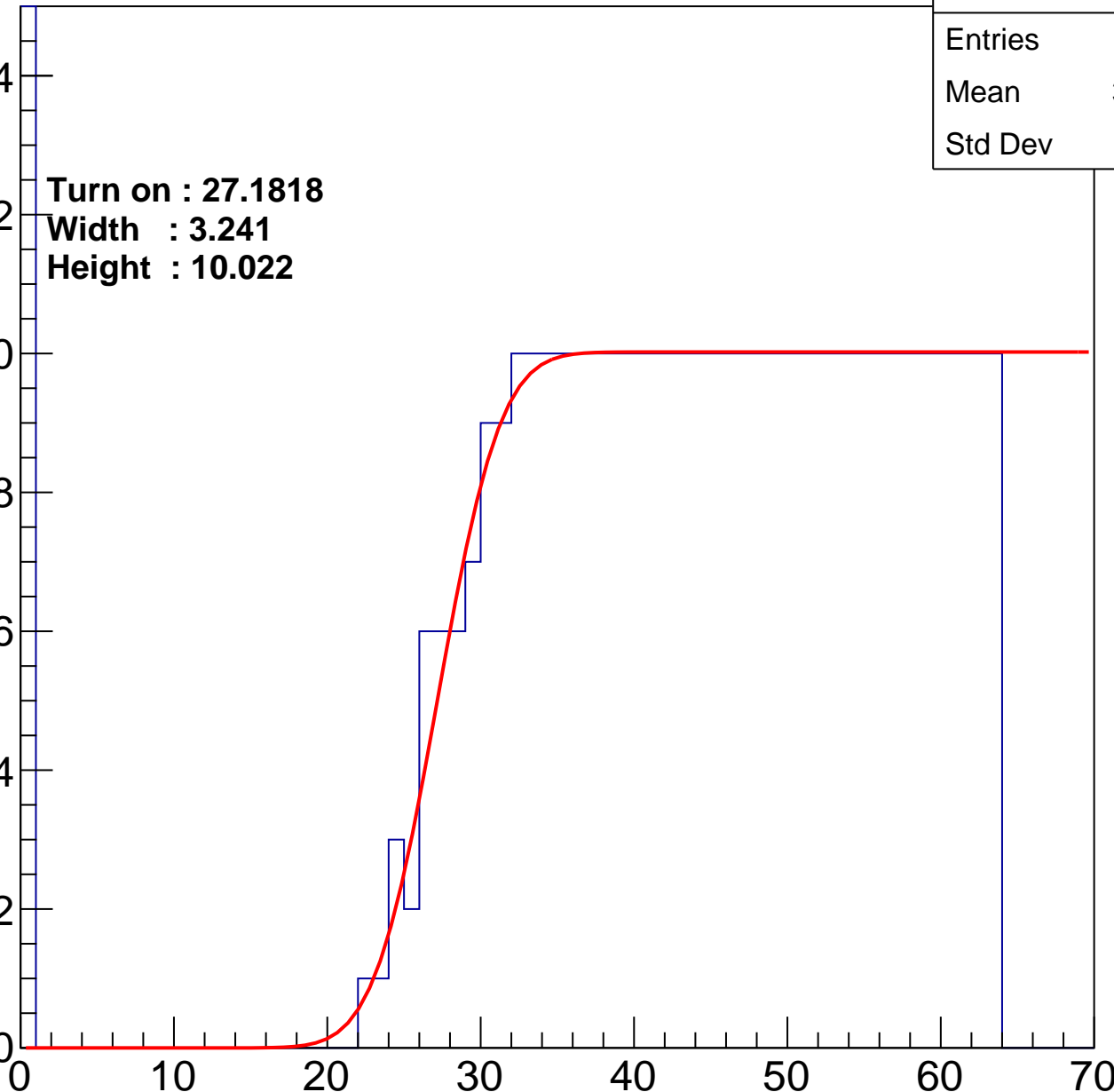
Width : 3.241

Height : 10.022

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch88

calib_packv5_041523_1651.root, FC#0, port C2

Entries	447
Mean	38.4
Std Dev	17.97

Turn on : 24.5326

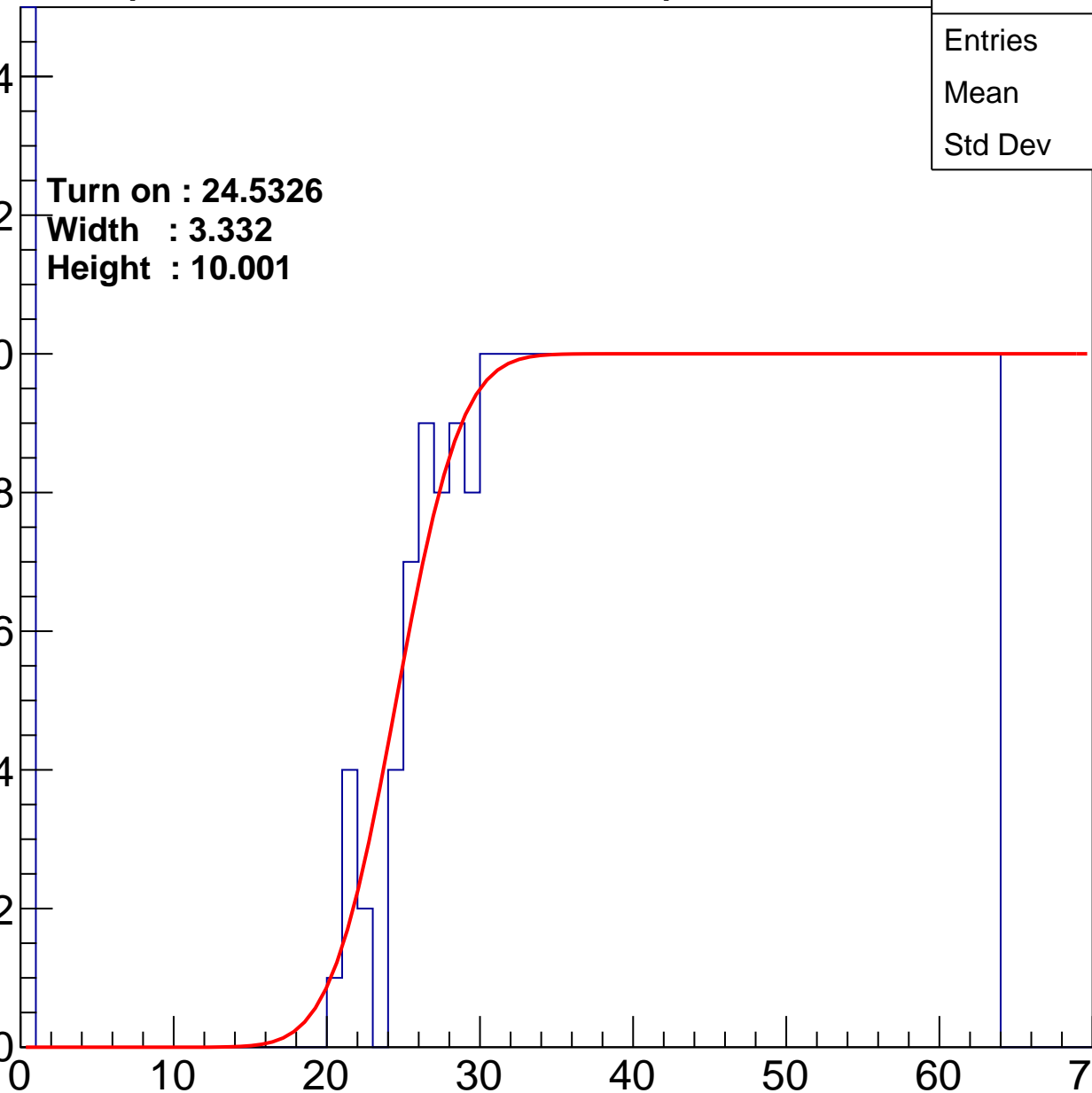
Width : 3.332

Height : 10.001

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch89

calib_packv5_041523_1651.root, FC#0, port C2

Entries	461
Mean	37.77
Std Dev	18.16

Turn on : 23.6822

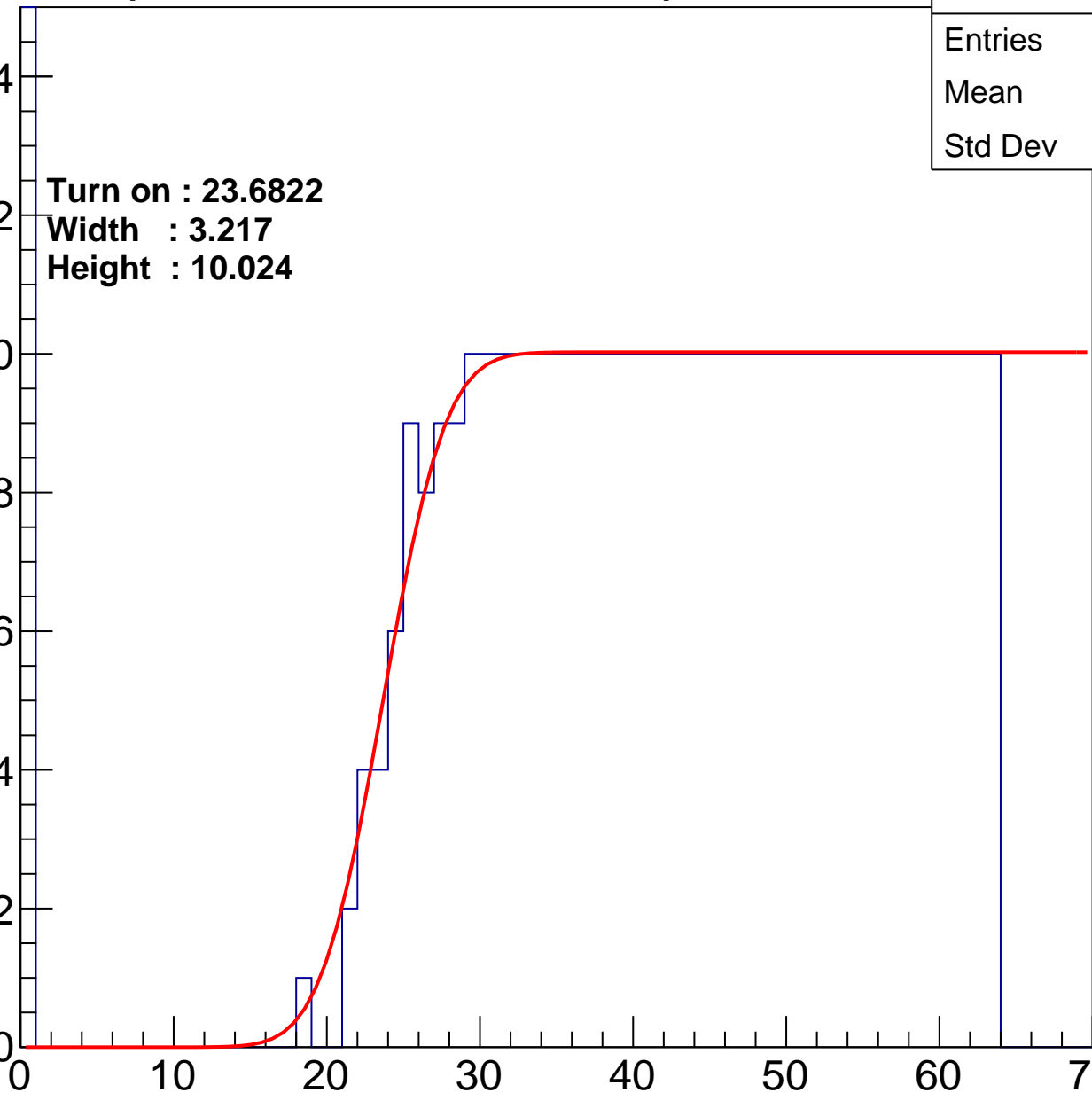
Width : 3.217

Height : 10.024

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch90

calib_packv5_041523_1651.root, FC#0, port C2

Entries	440
Mean	39.2
Std Dev	17.13

Turn on : 24.7730

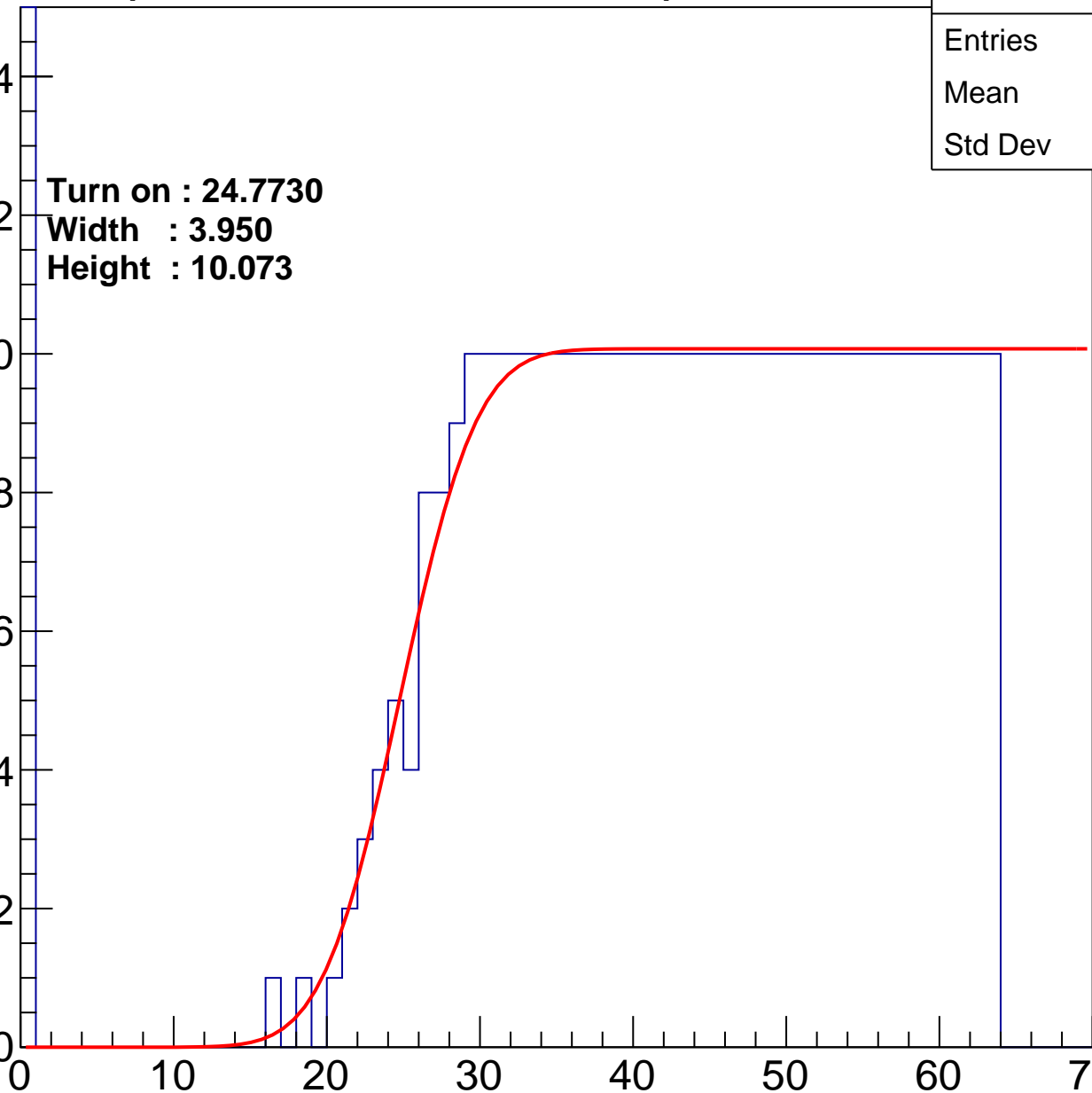
Width : 3.950

Height : 10.073

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch91

calib_packv5_041523_1651.root, FC#0, port C2

Entries	398
Mean	41.07
Std Dev	16.64

Turn on : 27.9631

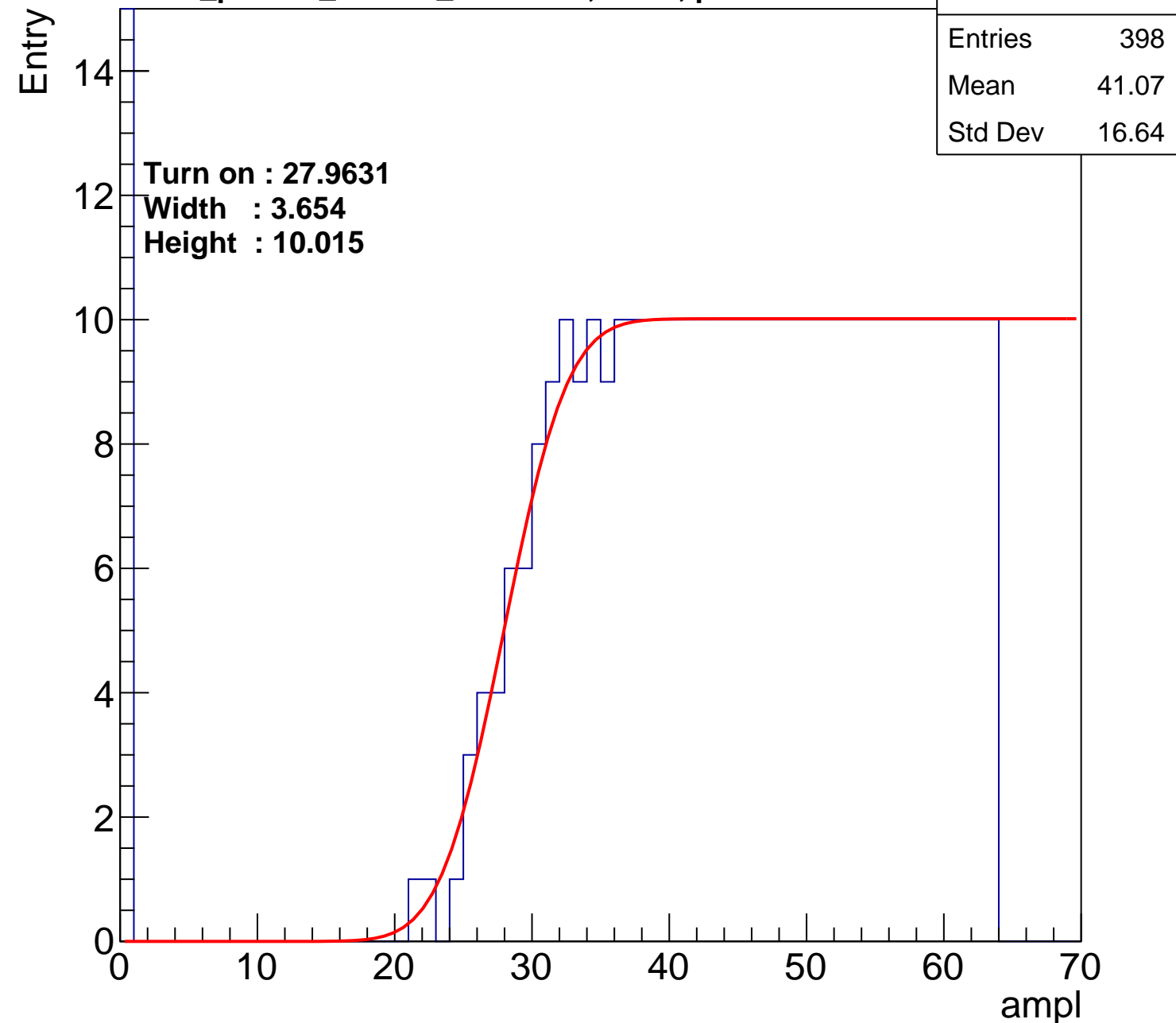
Width : 3.654

Height : 10.015

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch92

calib_packv5_041523_1651.root, FC#0, port C2

Entries	468
Mean	37.56
Std Dev	18.07

Turn on : 22.5625

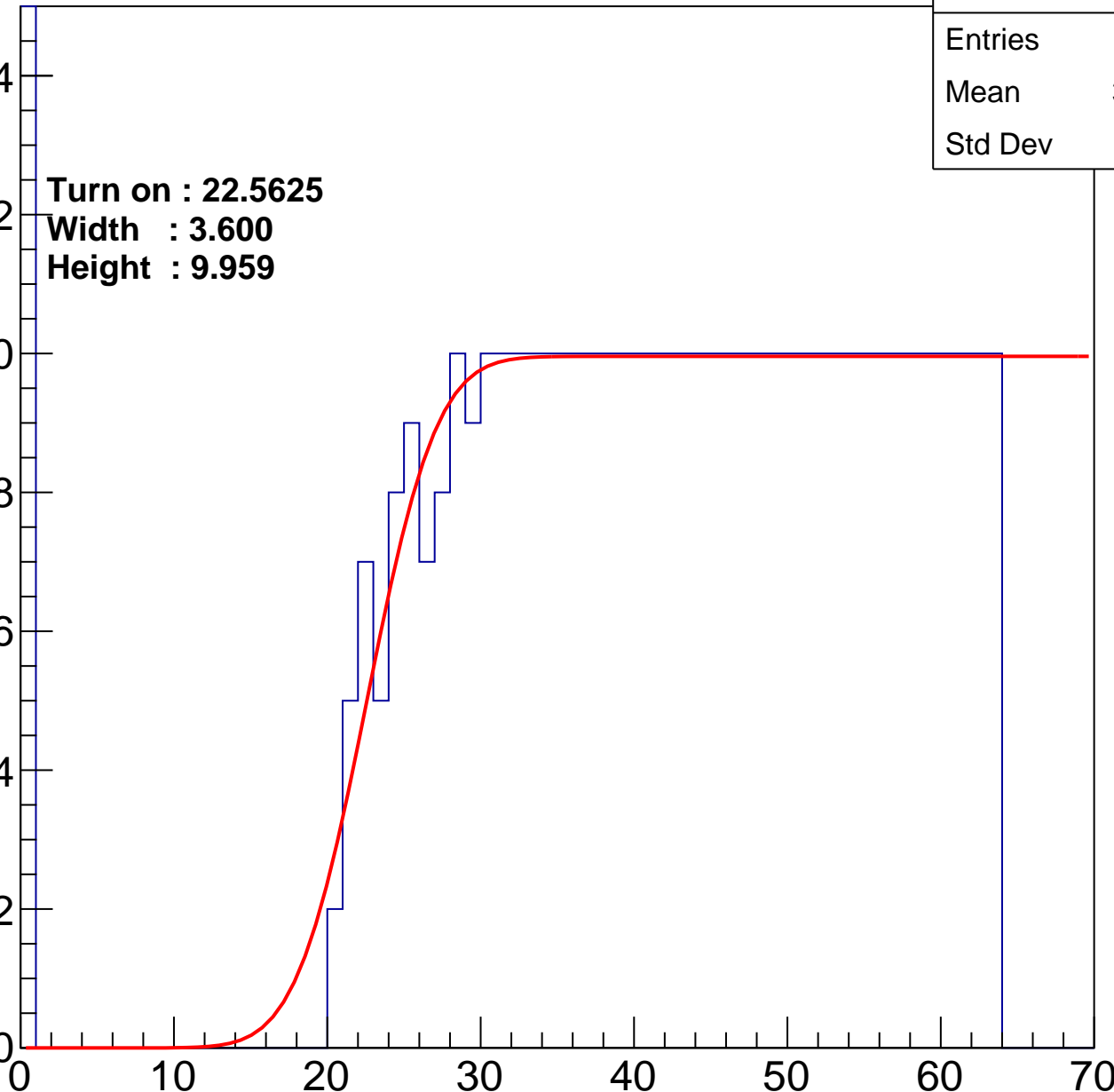
Width : 3.600

Height : 9.959

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch93

calib_packv5_041523_1651.root, FC#0, port C2

Entries	423
Mean	40.05
Std Dev	16.8

Turn on : 26.1510

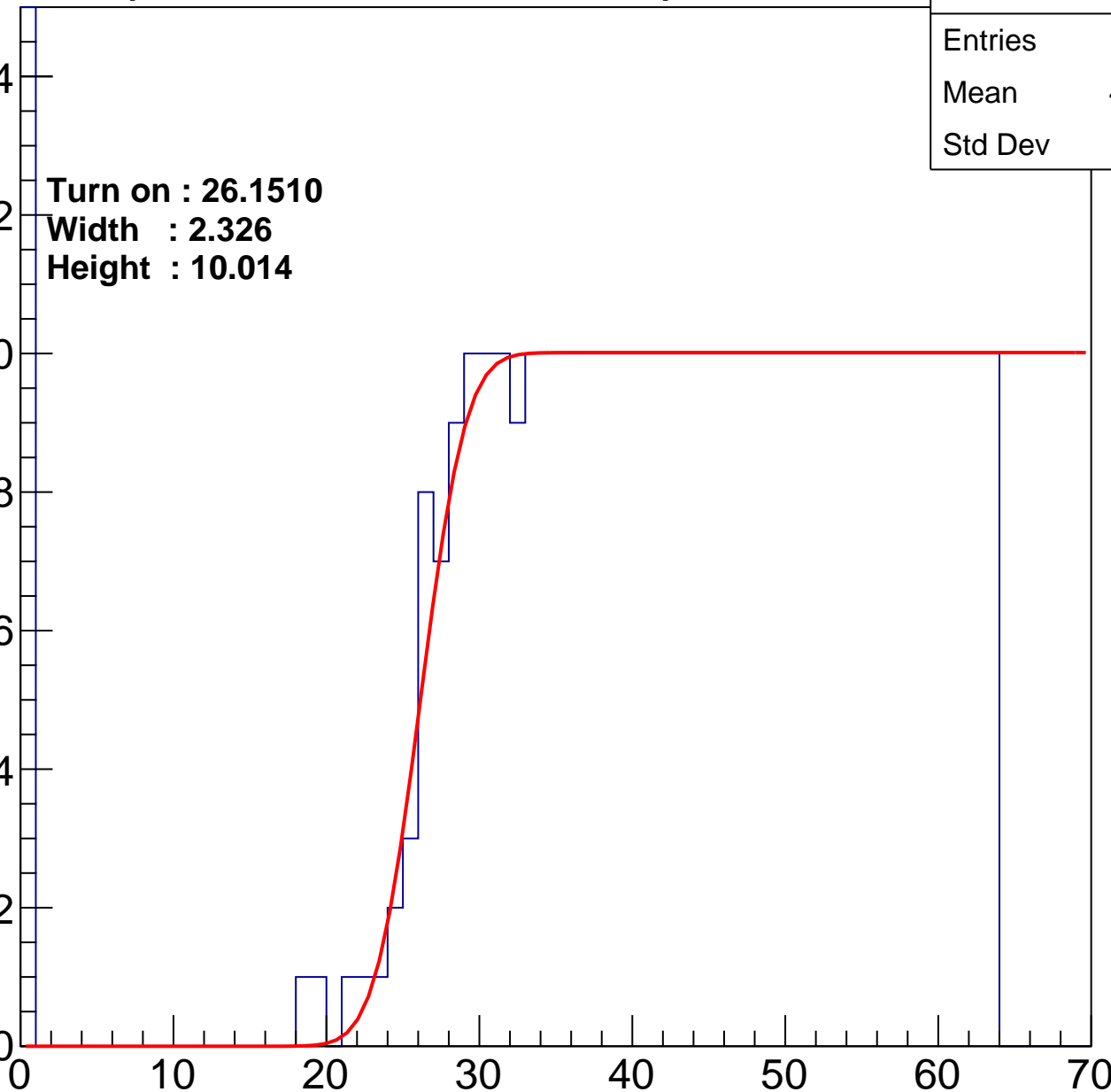
Width : 2.326

Height : 10.014

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch94

calib_packv5_041523_1651.root, FC#0, port C2

Entries	449
Mean	38.65
Std Dev	17.52

Turn on : 24.3914

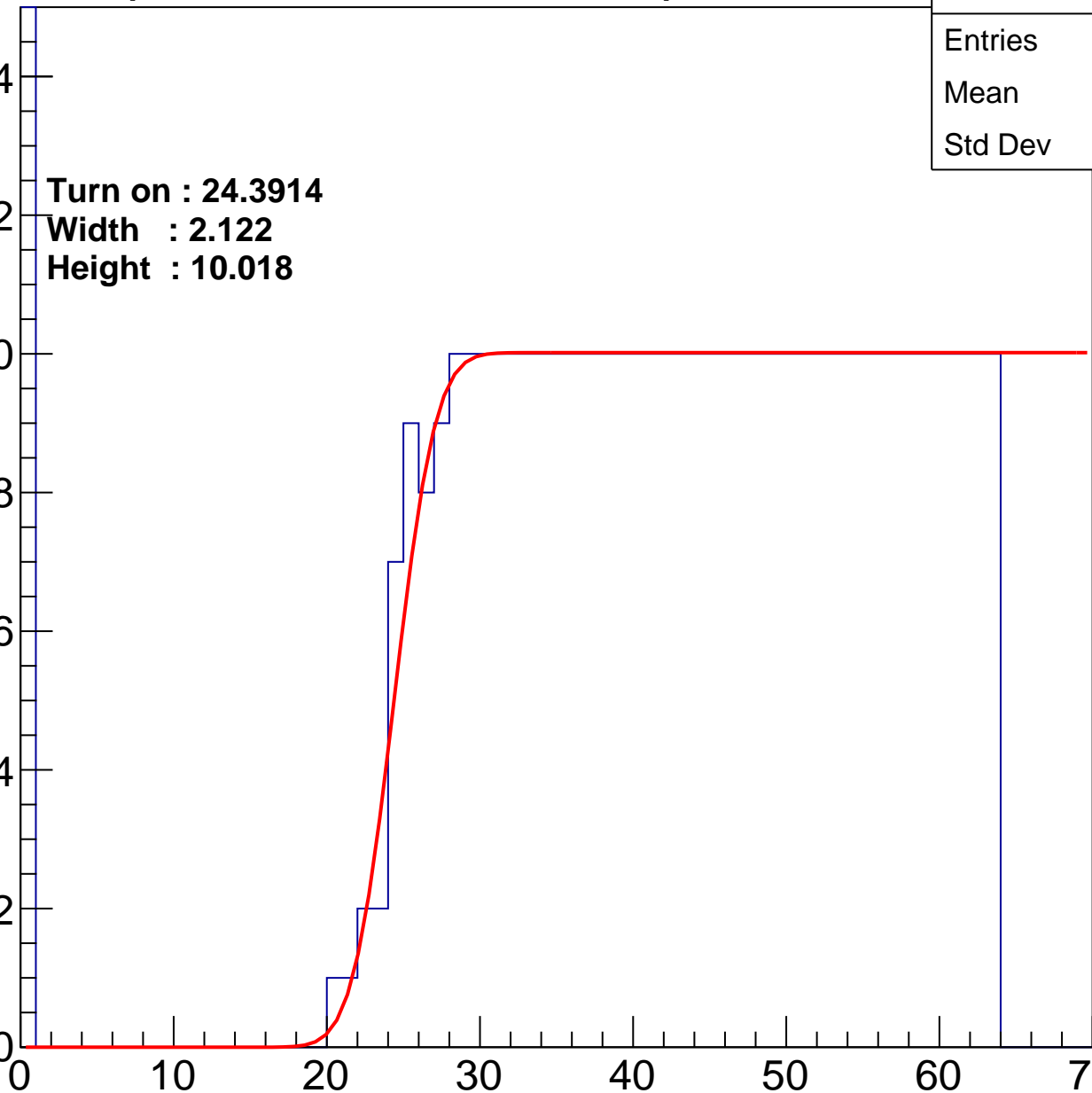
Width : 2.122

Height : 10.018

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch95

calib_packv5_041523_1651.root, FC#0, port C2

Entries	429
Mean	39.2
Std Dev	17.77

Turn on : 26.5941

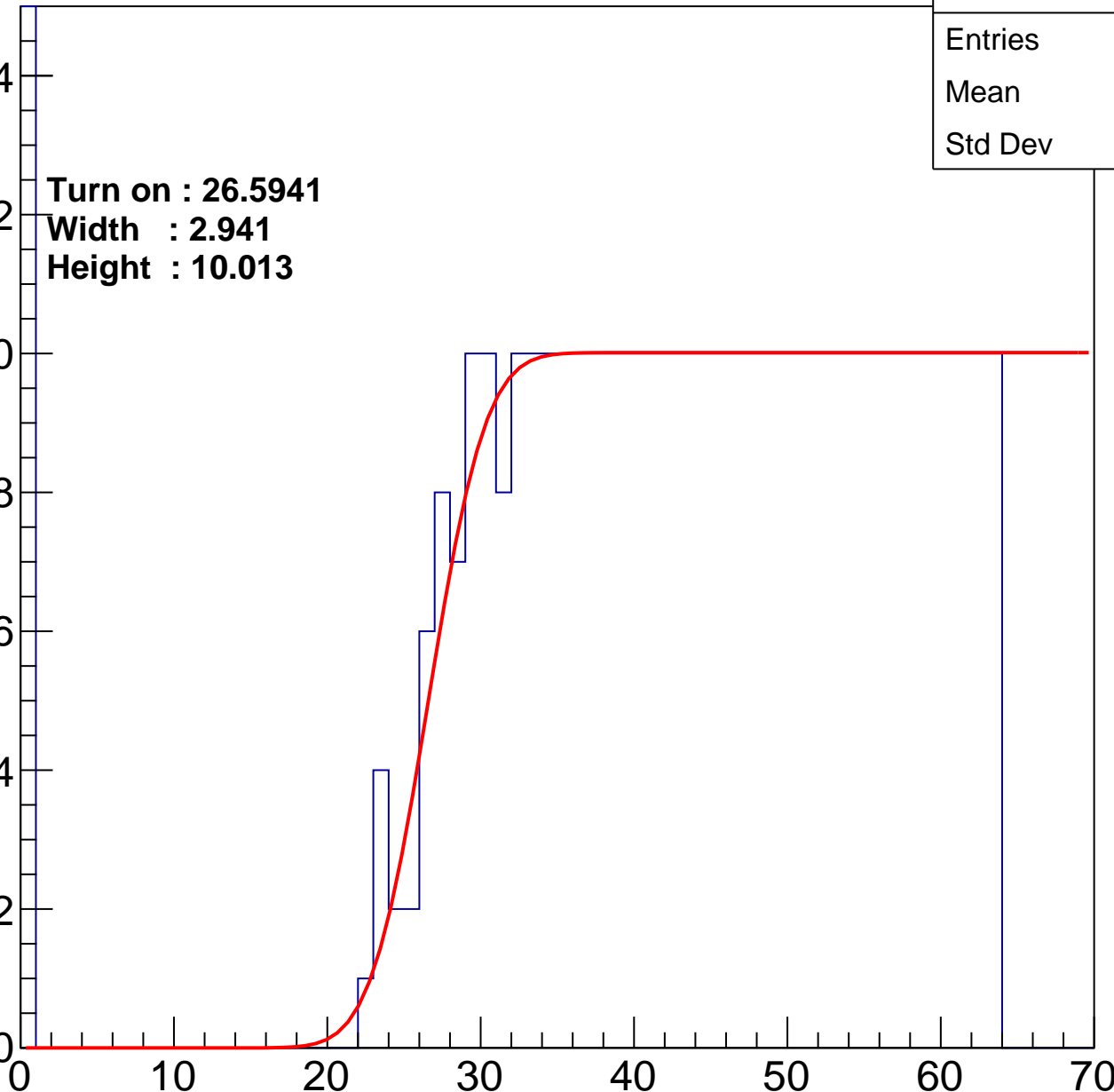
Width : 2.941

Height : 10.013

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch96

calib_packv5_041523_1651.root, FC#0, port C2

Entries	428
Mean	39.58
Std Dev	17.25

Turn on : 26.0567

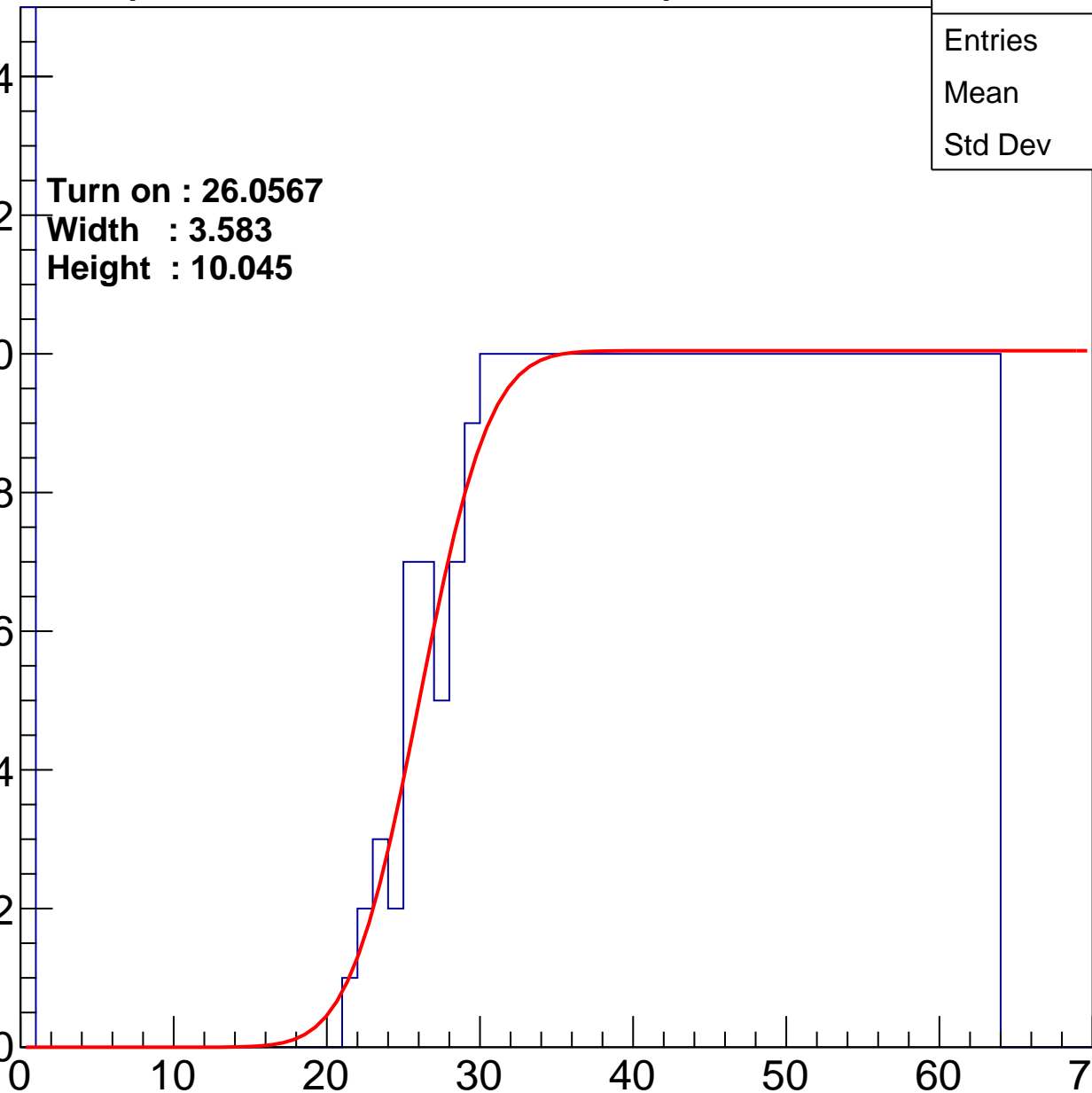
Width : 3.583

Height : 10.045

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch97

calib_packv5_041523_1651.root, FC#0, port C2

Entries	421
Mean	39.89
Std Dev	17.18

Turn on : 26.3799

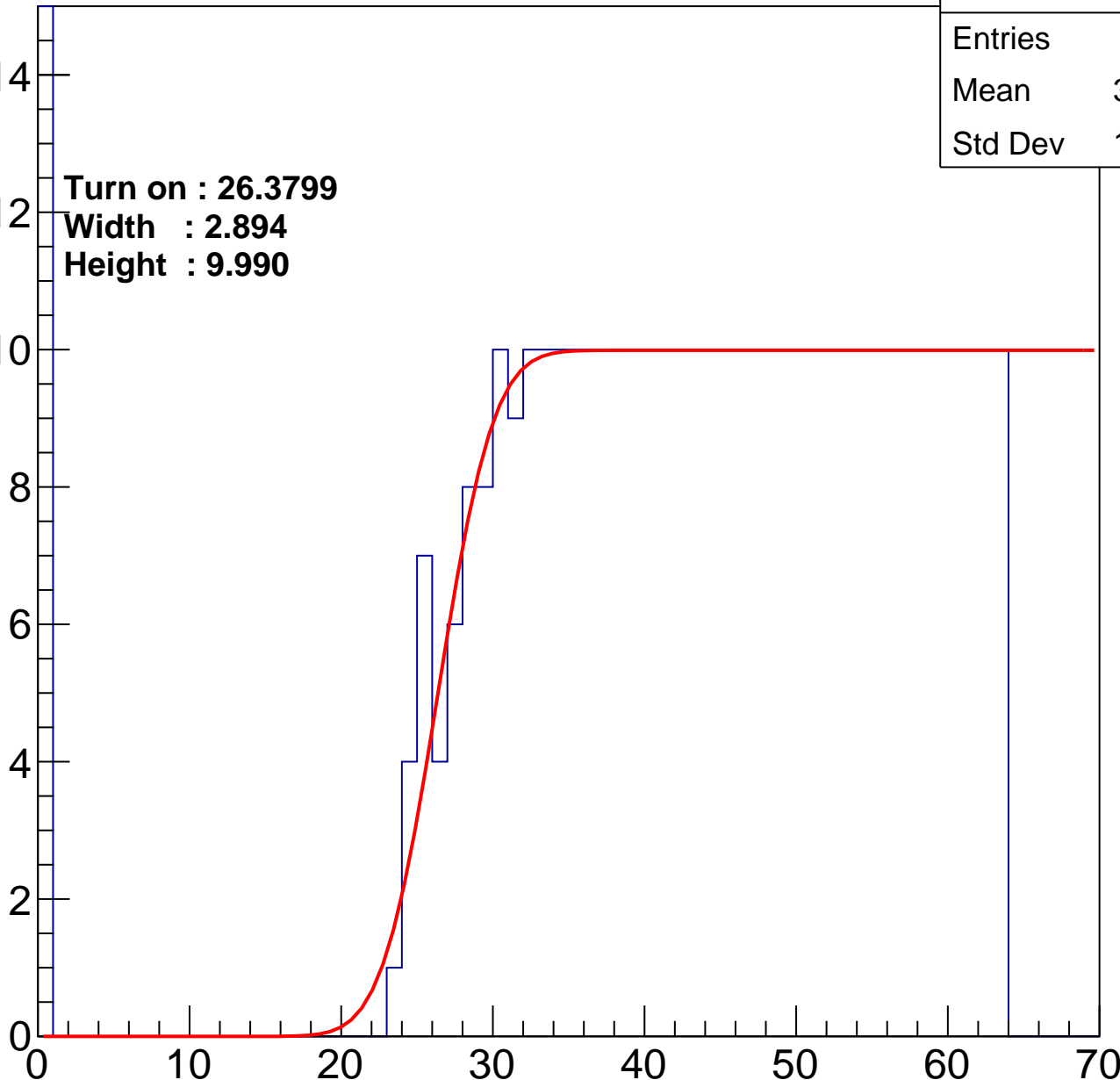
Width : 2.894

Height : 9.990

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch98

calib_packv5_041523_1651.root, FC#0, port C2

Entries	452
Mean	38.19
Std Dev	18.01

Turn on : 25.3622

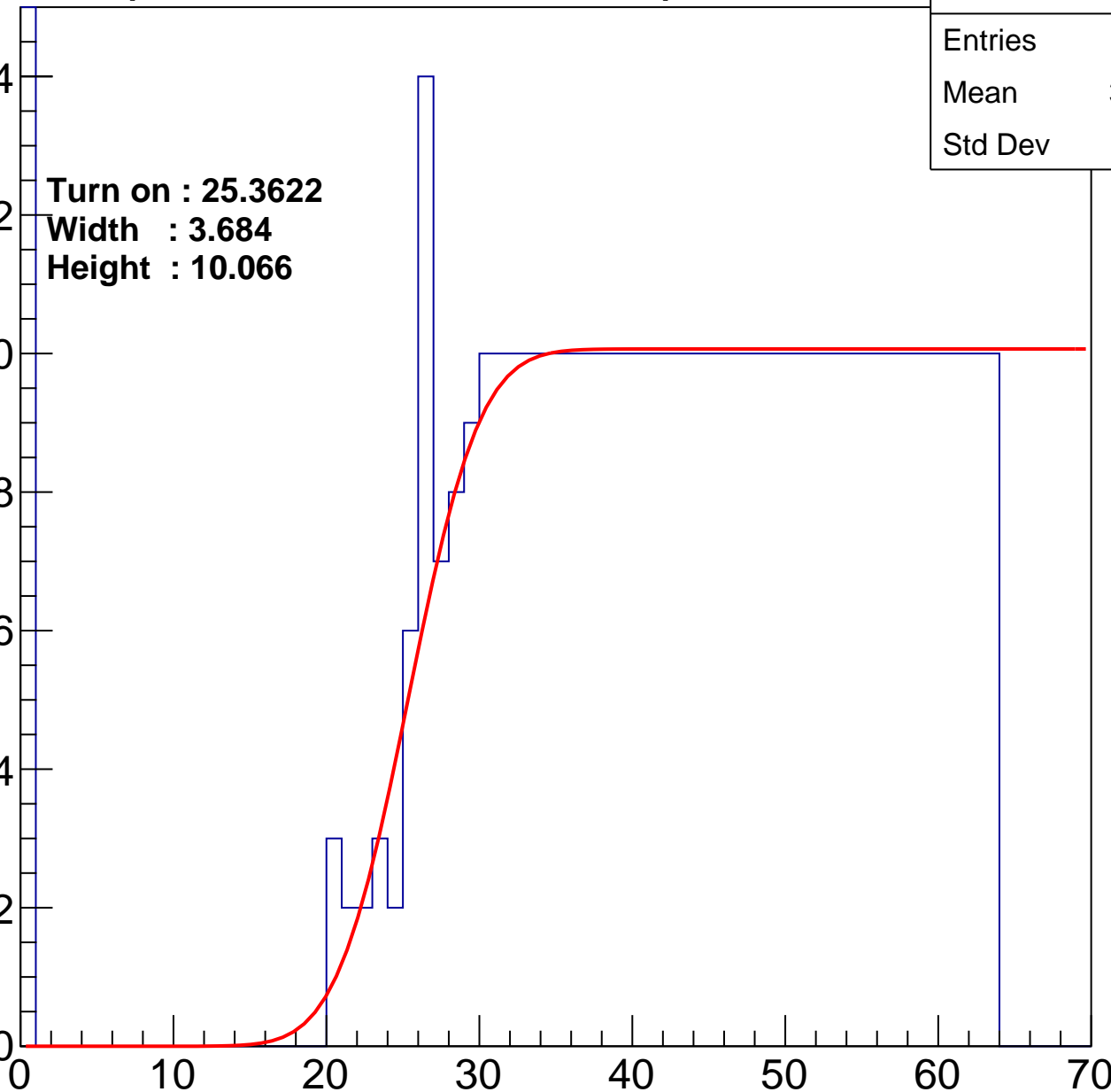
Width : 3.684

Height : 10.066

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch99

calib_packv5_041523_1651.root, FC#0, port C2

Entries	436
Mean	38.88
Std Dev	17.83

Turn on : 25.8536

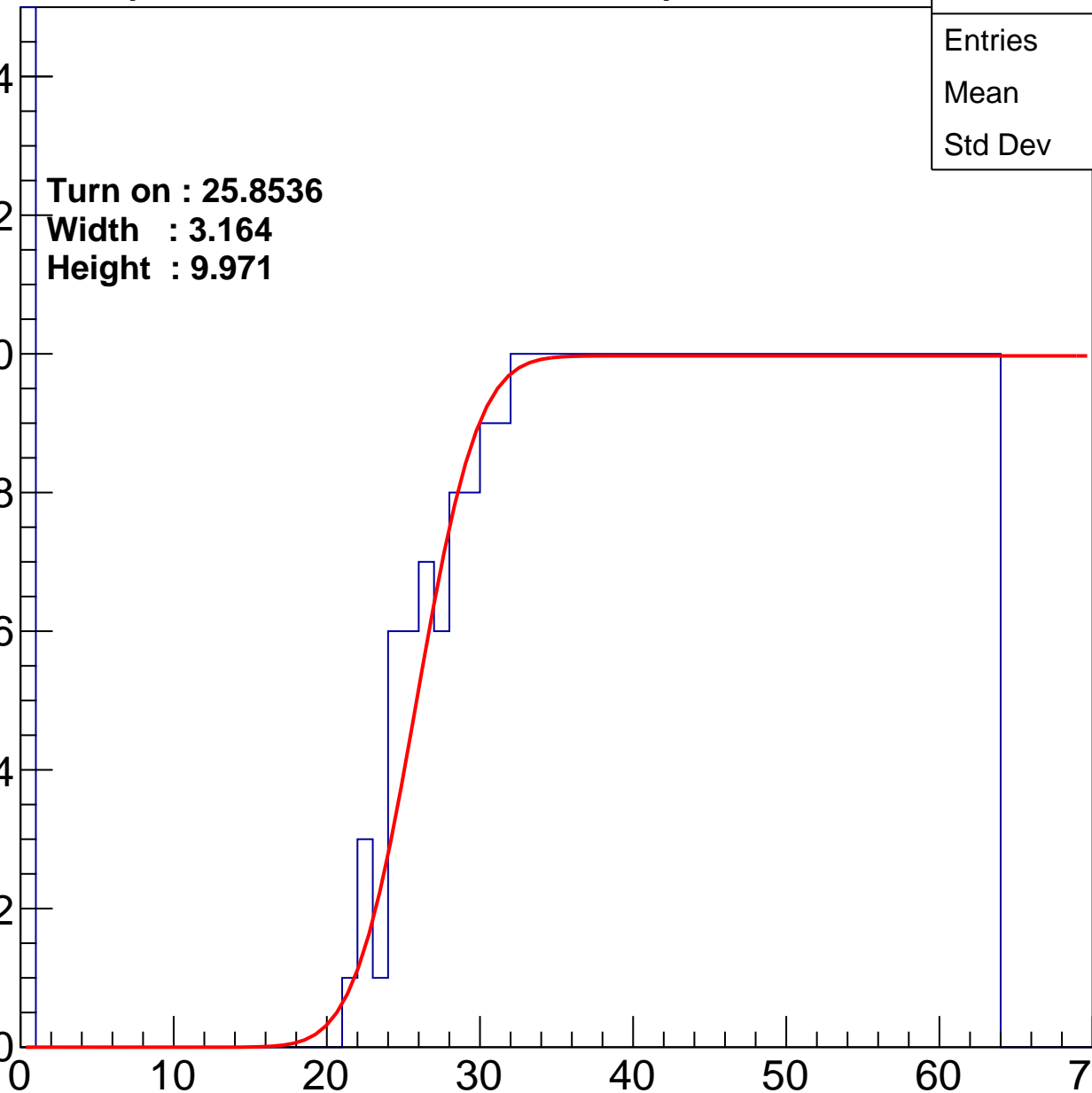
Width : 3.164

Height : 9.971

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch100

calib_packv5_041523_1651.root, FC#0, port C2

Entries	421
Mean	40.38
Std Dev	16.39

Turn on : 25.1666

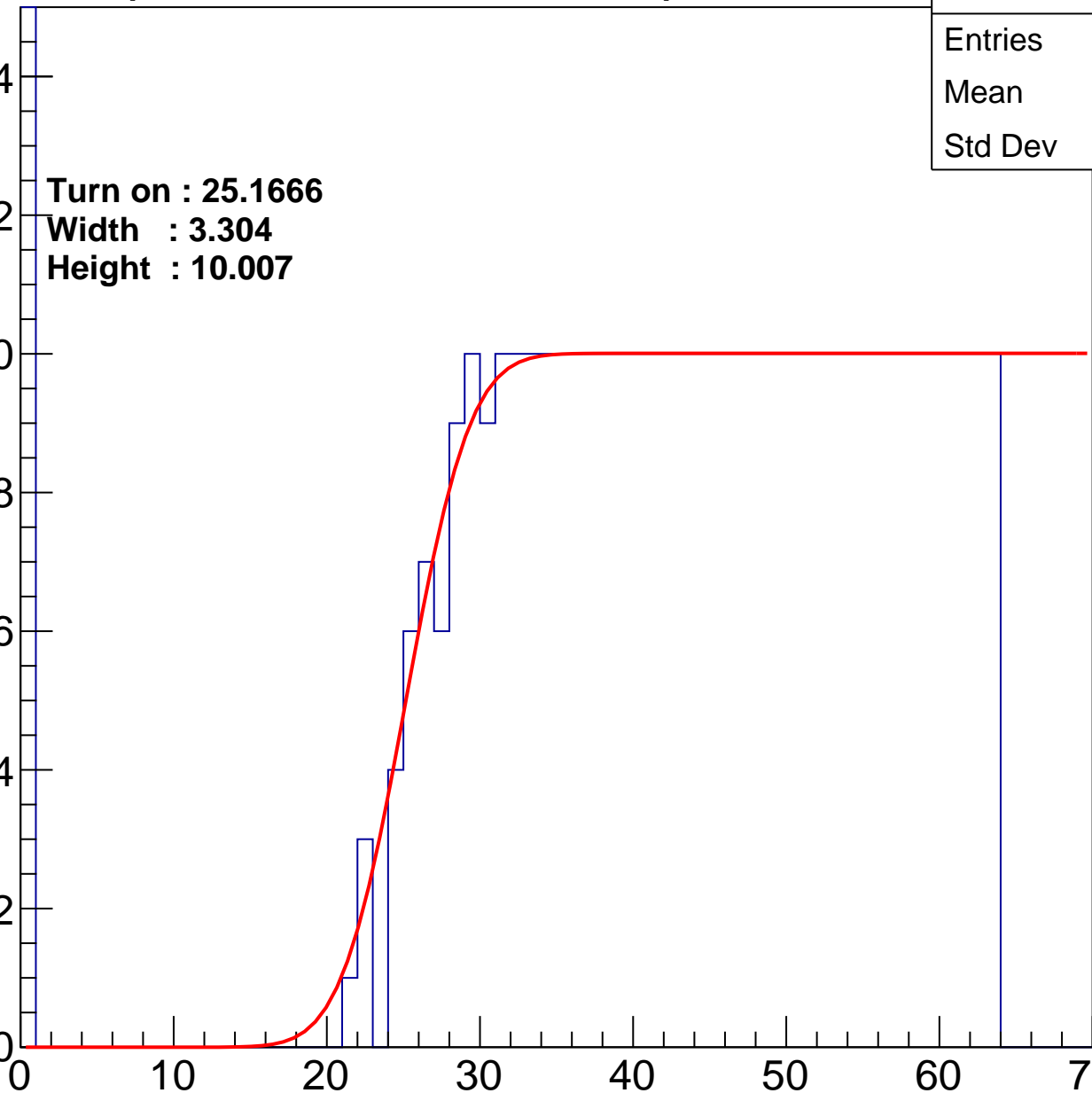
Width : 3.304

Height : 10.007

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch101

calib_packv5_041523_1651.root, FC#0, port C2

Entries	441
Mean	38.89
Std Dev	17.58

Turn on : 25.4189

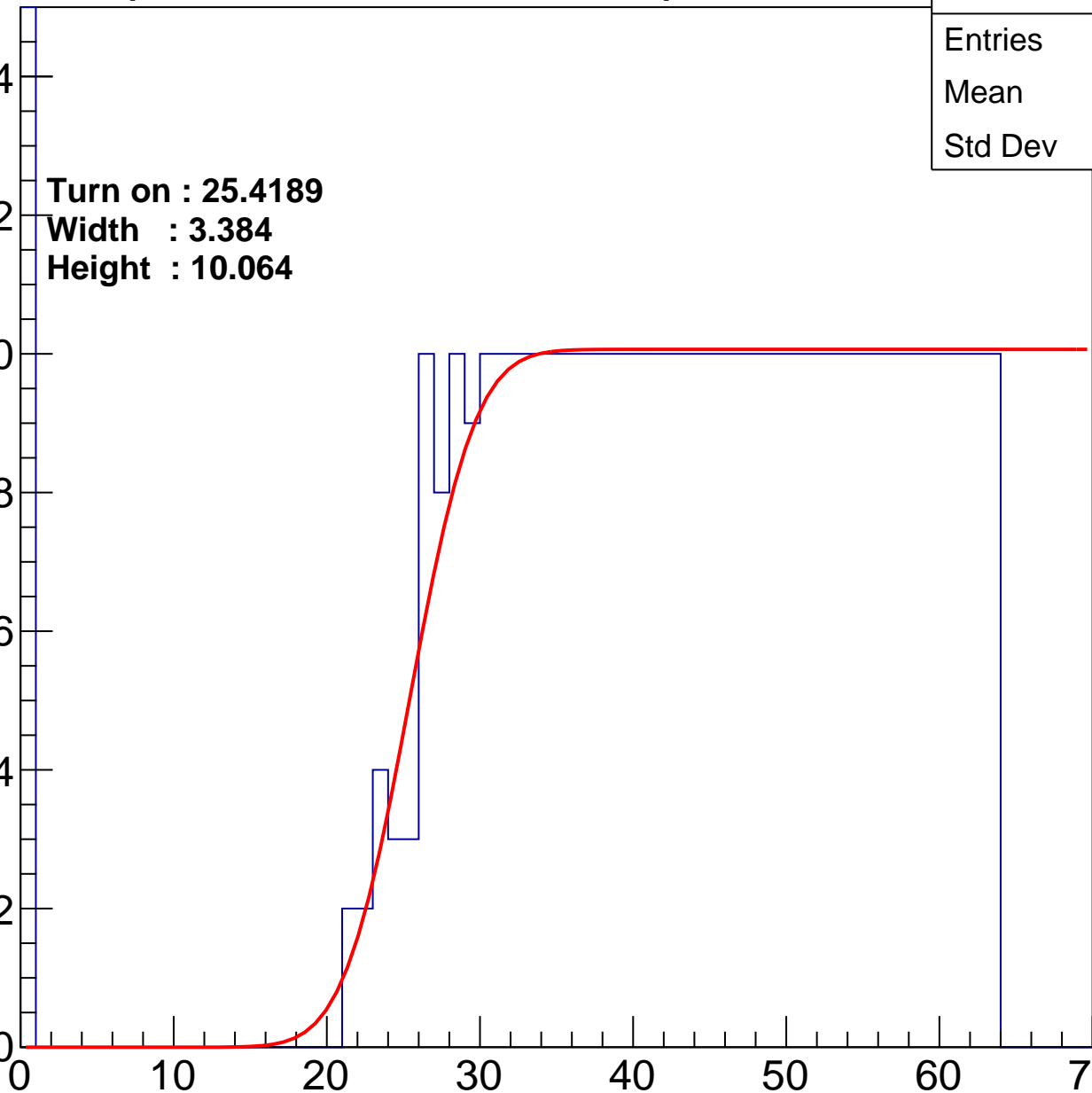
Width : 3.384

Height : 10.064

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch102

calib_packv5_041523_1651.root, FC#0, port C2

Entries	421
Mean	39.71
Std Dev	17.47

Turn on : 27.0275

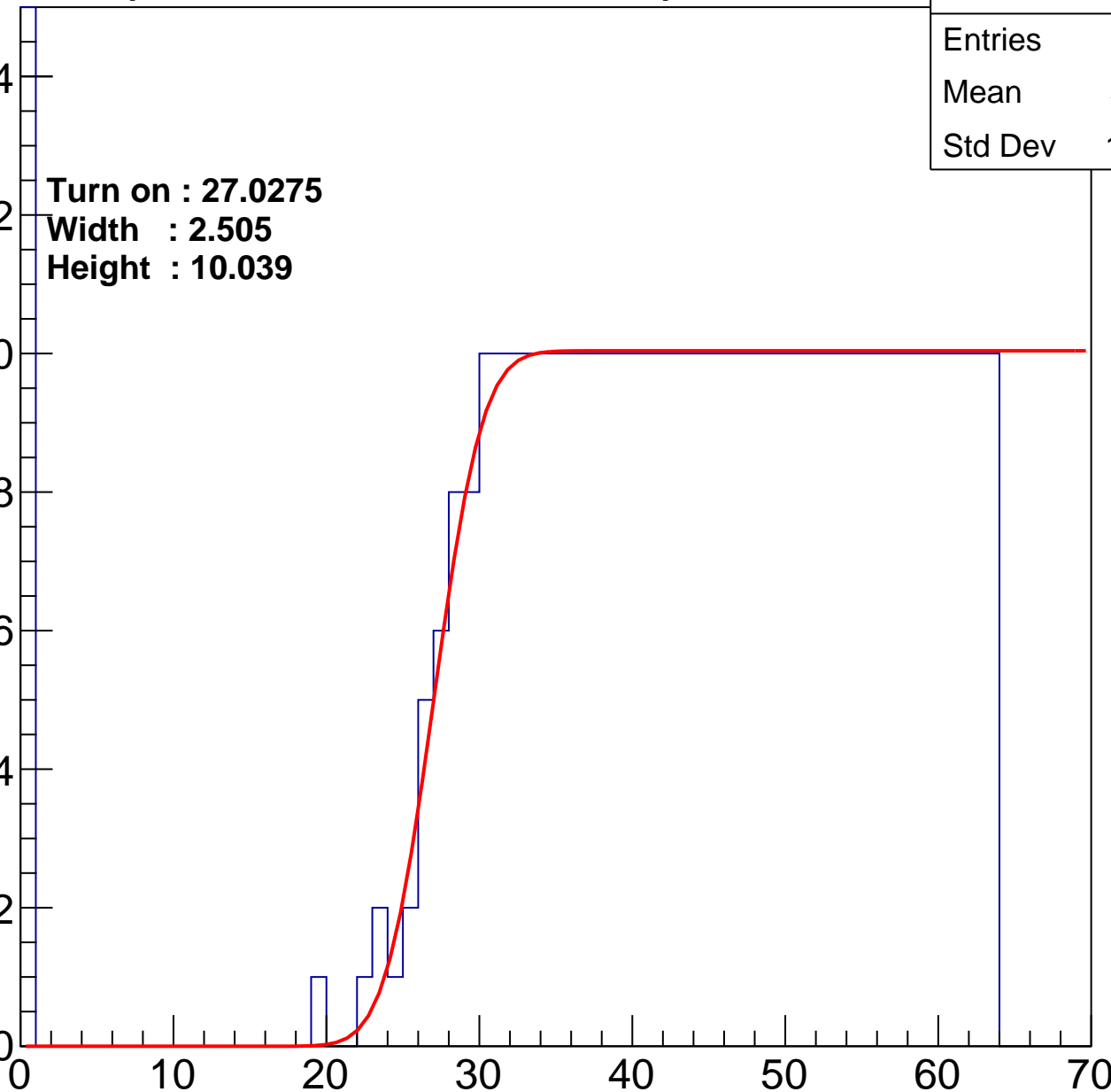
Width : 2.505

Height : 10.039

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch103

calib_packv5_041523_1651.root, FC#0, port C2

Entries	429
Mean	40.09
Std Dev	16.38

Turn on : 24.8220

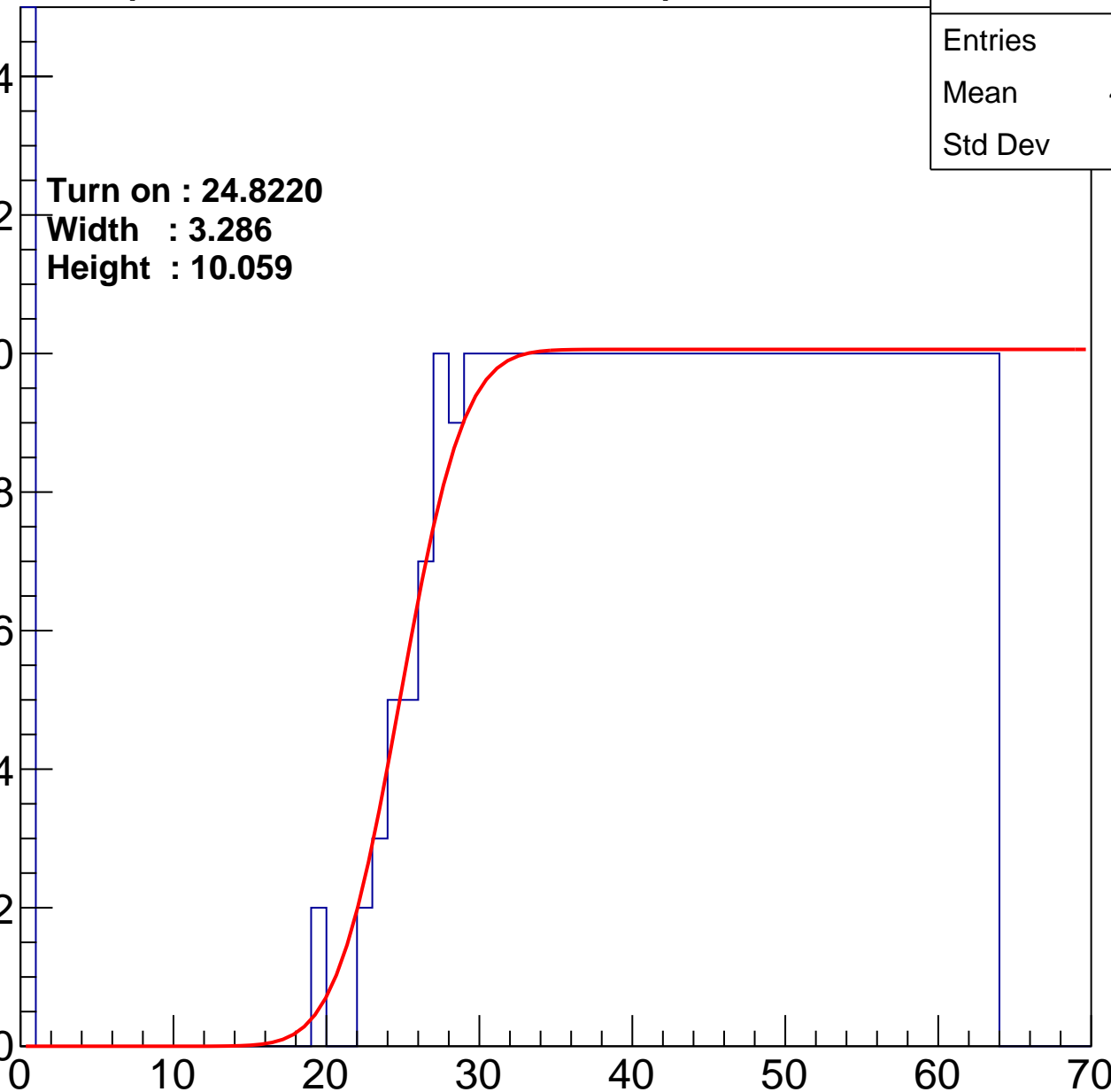
Width : 3.286

Height : 10.059

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch104

calib_packv5_041523_1651.root, FC#0, port C2

Entries	466
Mean	36.99
Std Dev	18.97

Turn on : 24.5865

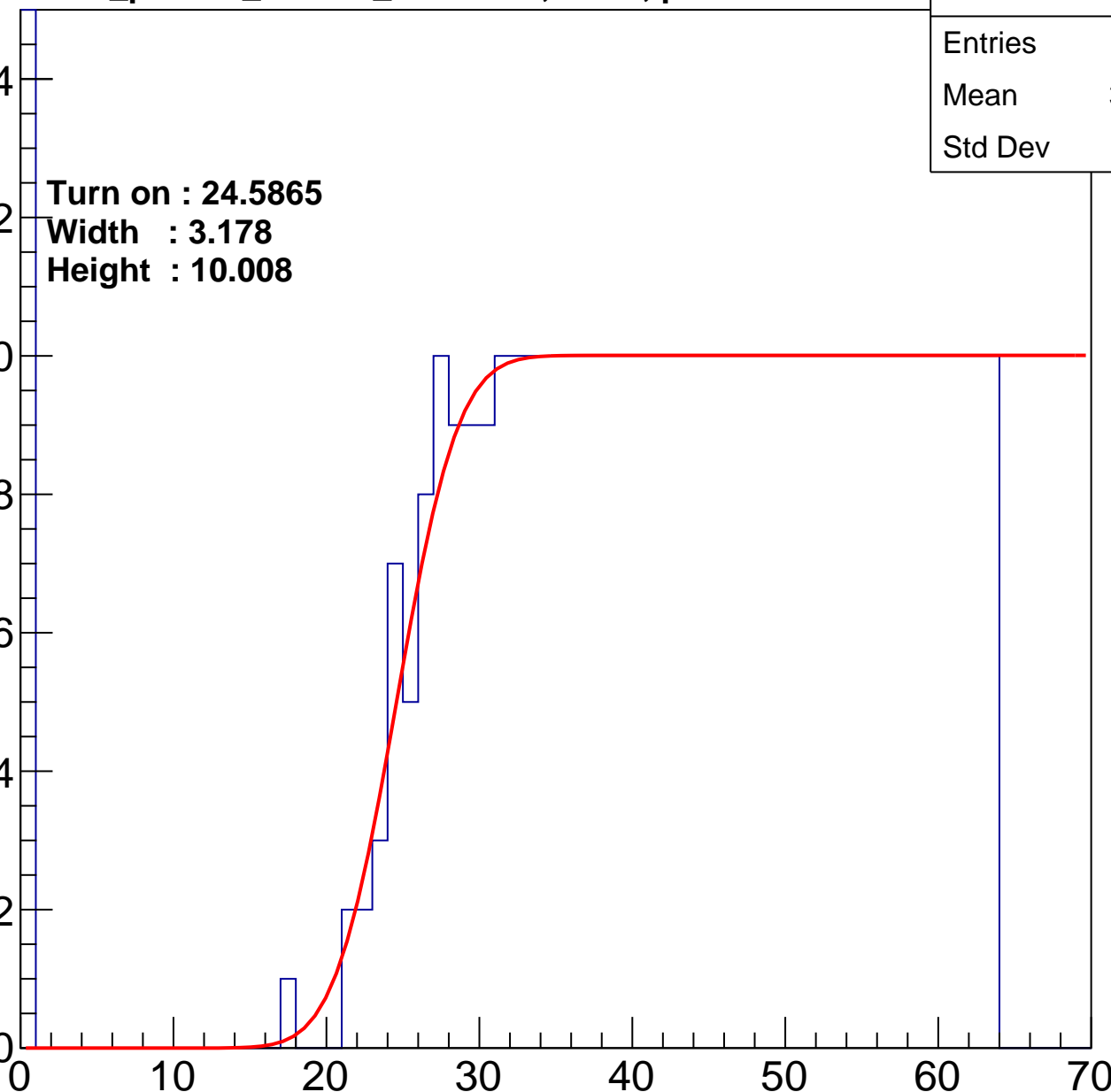
Width : 3.178

Height : 10.008

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch105

calib_packv5_041523_1651.root, FC#0, port C2

Entries	409
Mean	40.19
Std Dev	17.39

Turn on : 27.8885

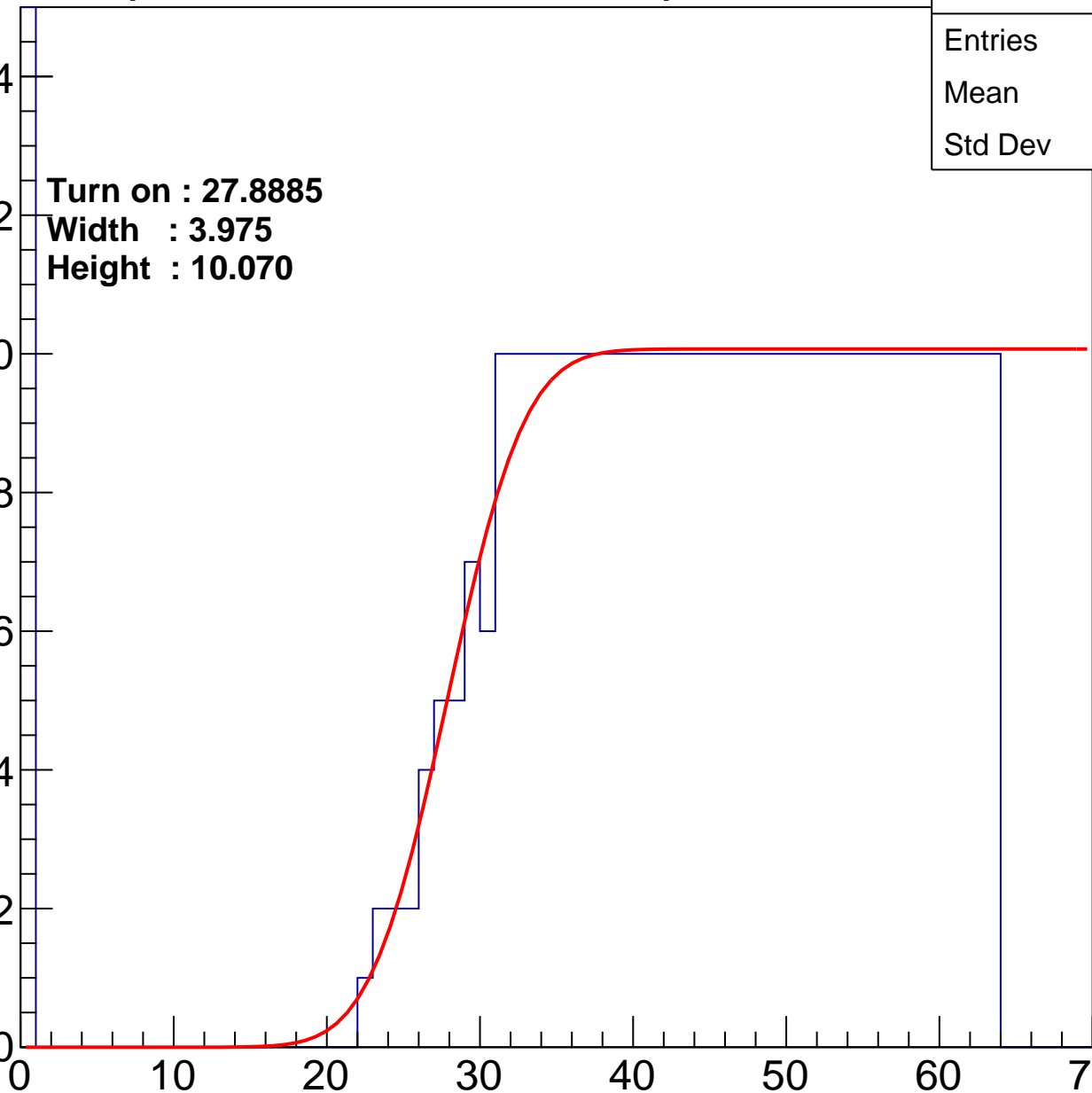
Width : 3.975

Height : 10.070

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch106

calib_packv5_041523_1651.root, FC#0, port C2

Entries	444
Mean	38.91
Std Dev	17.37

Turn on : 24.0377

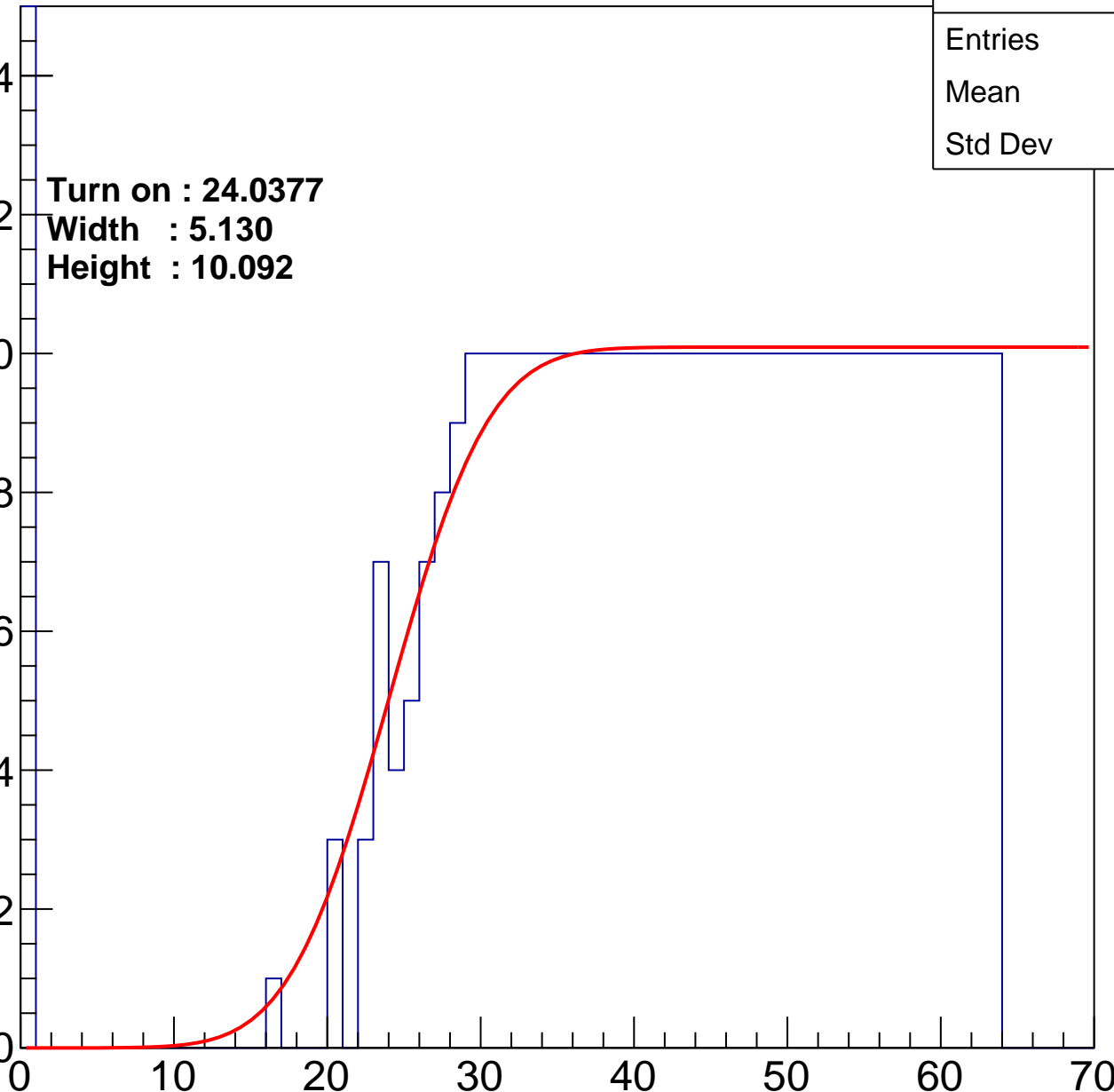
Width : 5.130

Height : 10.092

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch107

calib_packv5_041523_1651.root, FC#0, port C2

Entries	421
Mean	39.98
Std Dev	17.02

Turn on : 26.5910

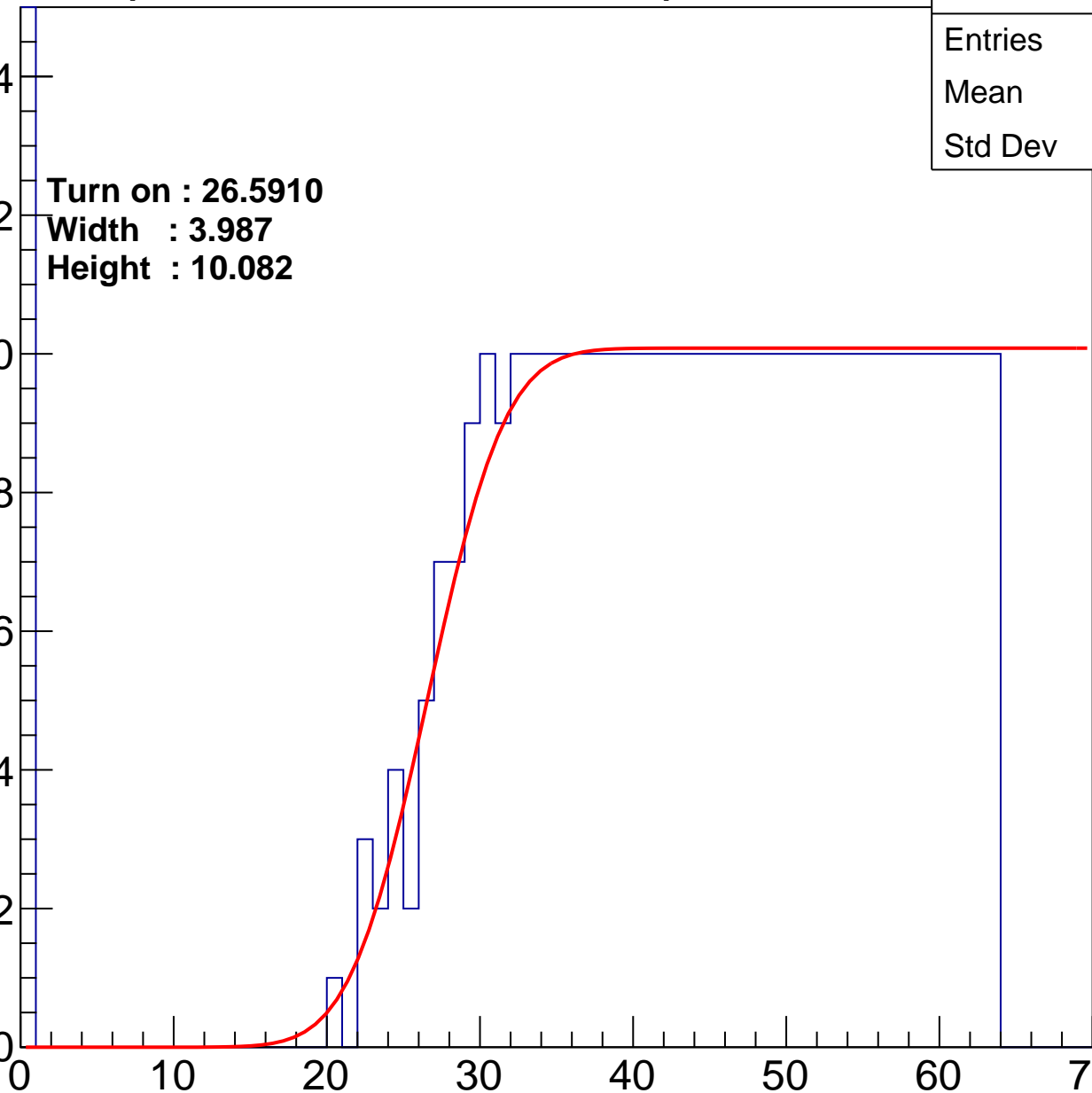
Width : 3.987

Height : 10.082

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch108

calib_packv5_041523_1651.root, FC#0, port C2

Entries	451
Mean	37.47
Std Dev	19.06

Turn on : 26.8951

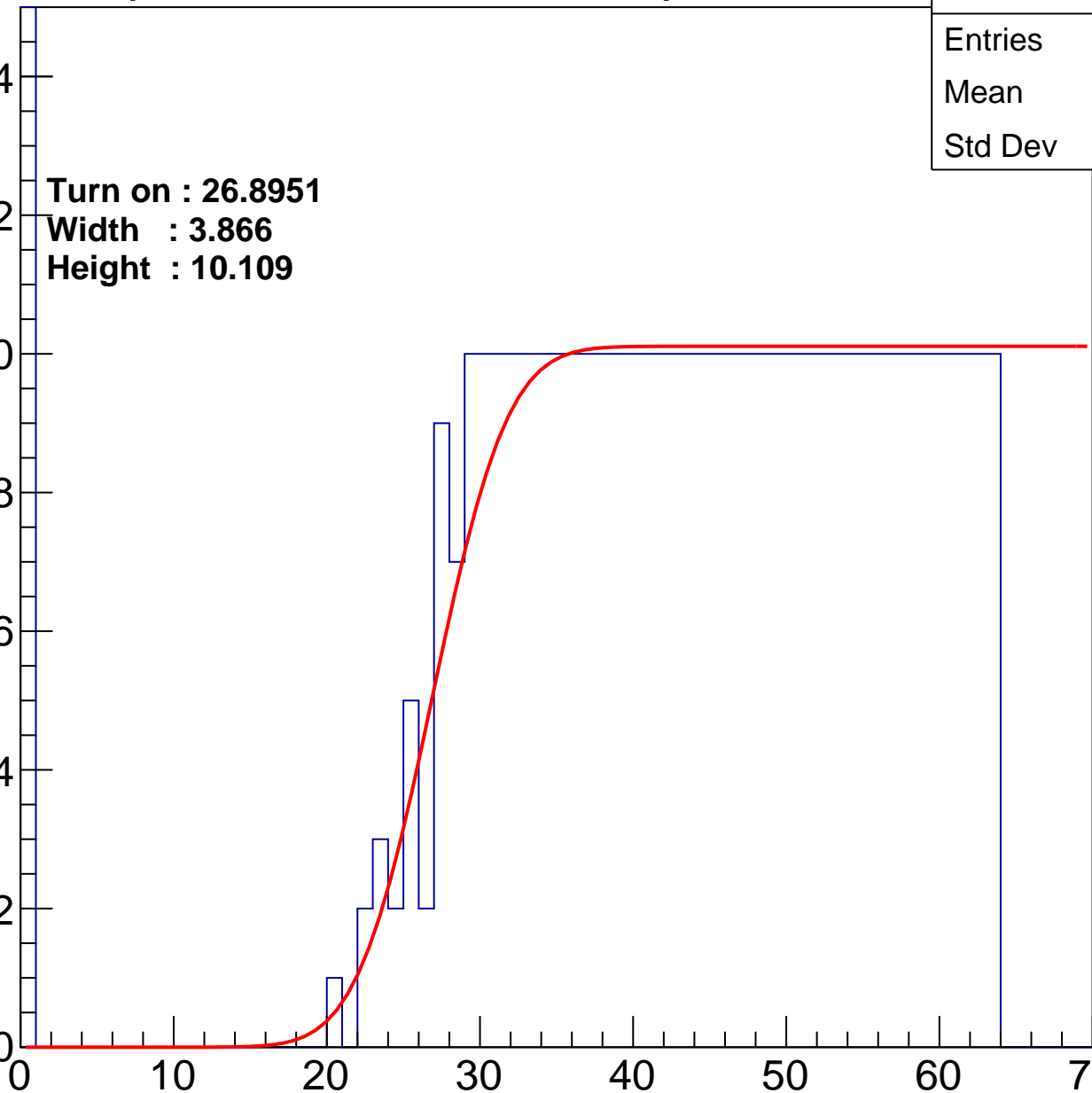
Width : 3.866

Height : 10.109

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch109

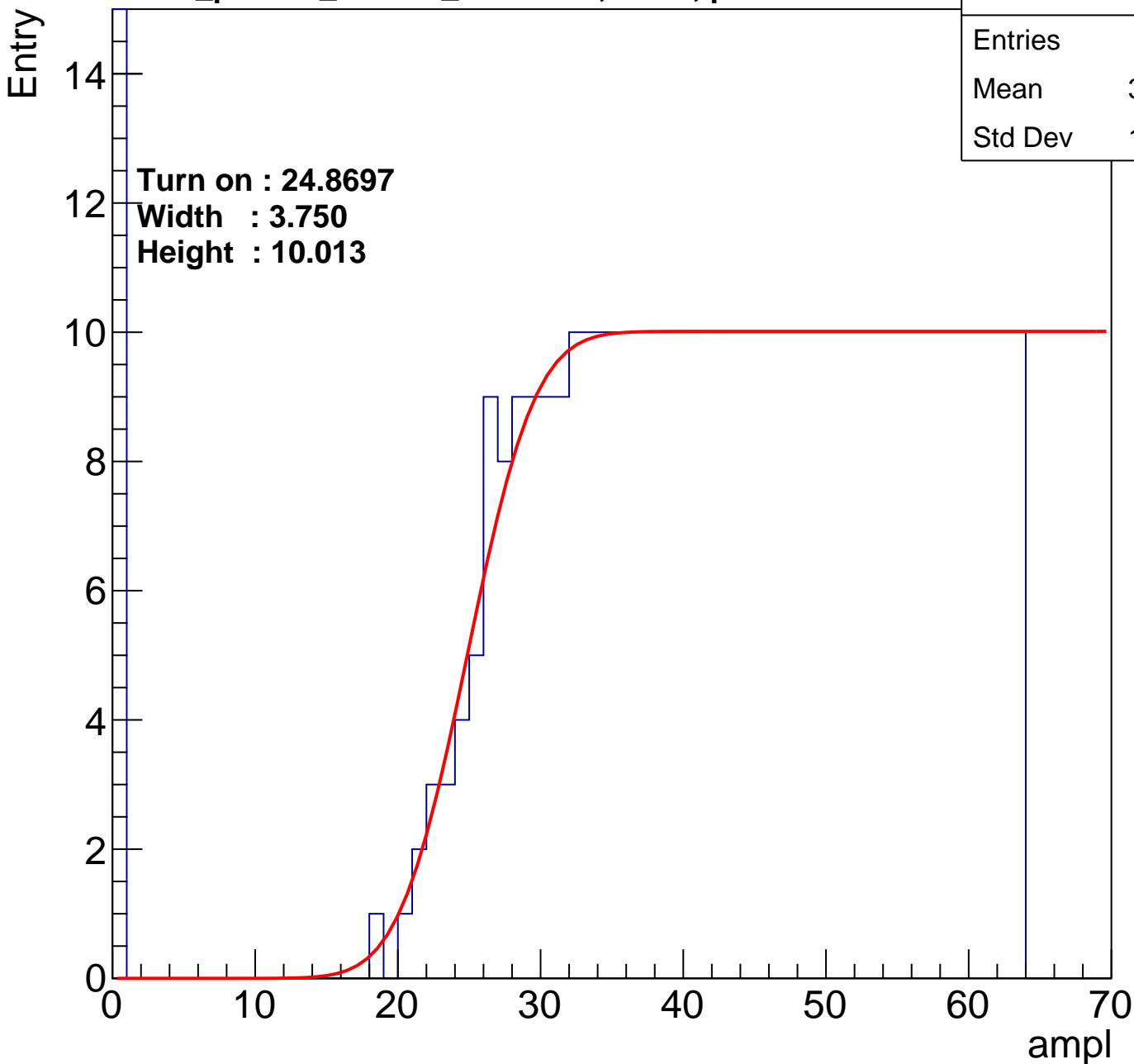
calib_packv5_041523_1651.root, FC#0, port C2

Entries	445
Mean	38.53
Std Dev	17.85

Turn on : 24.8697

Width : 3.750

Height : 10.013



B1L103S, U12-ch110

calib_packv5_041523_1651.root, FC#0, port C2

Entries	439
Mean	39.36
Std Dev	16.94

Turn on : 24.5037

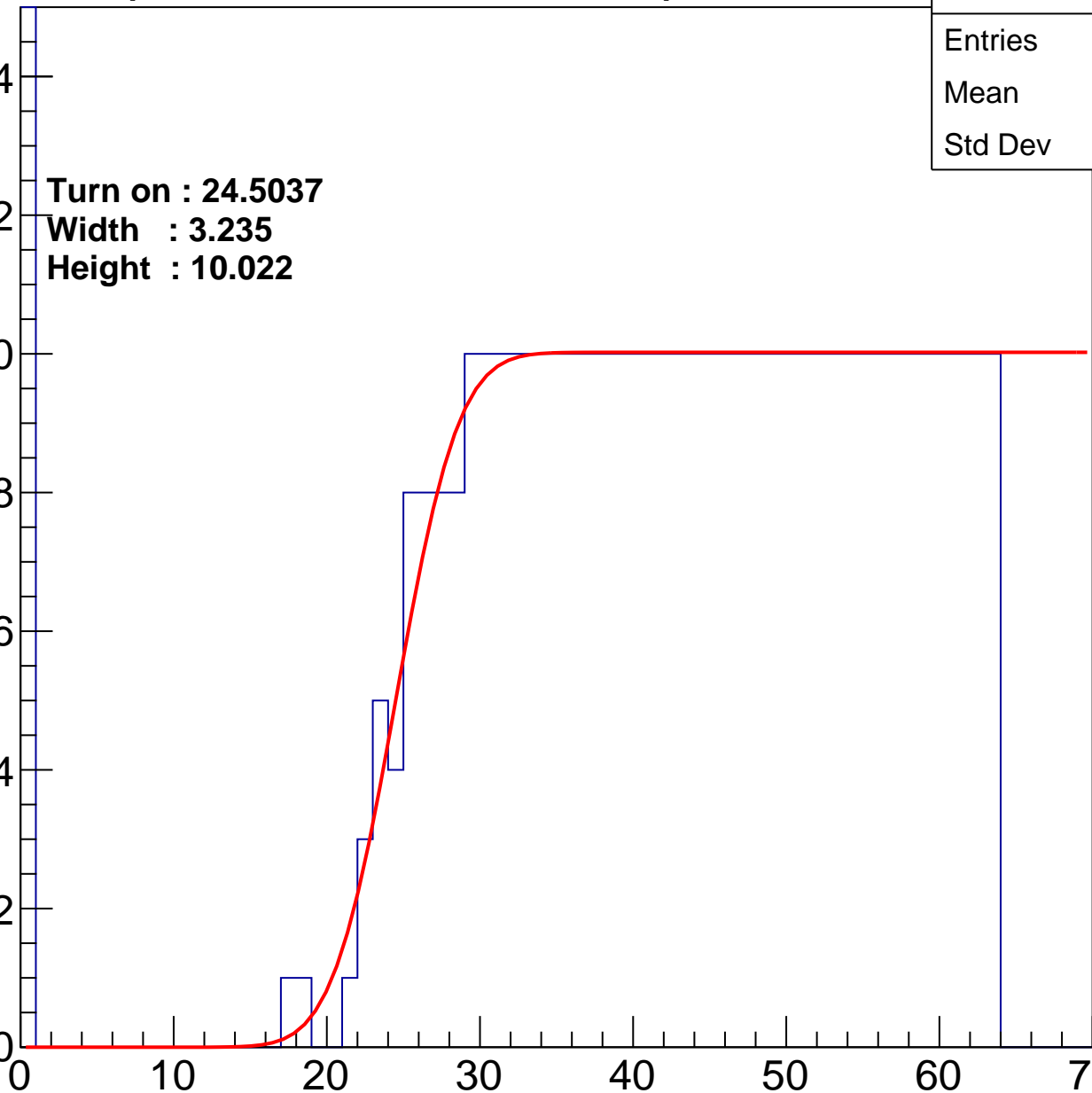
Width : 3.235

Height : 10.022

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch111

calib_packv5_041523_1651.root, FC#0, port C2

Entries	426
Mean	38.4
Std Dev	19.02

Turn on : 27.9787

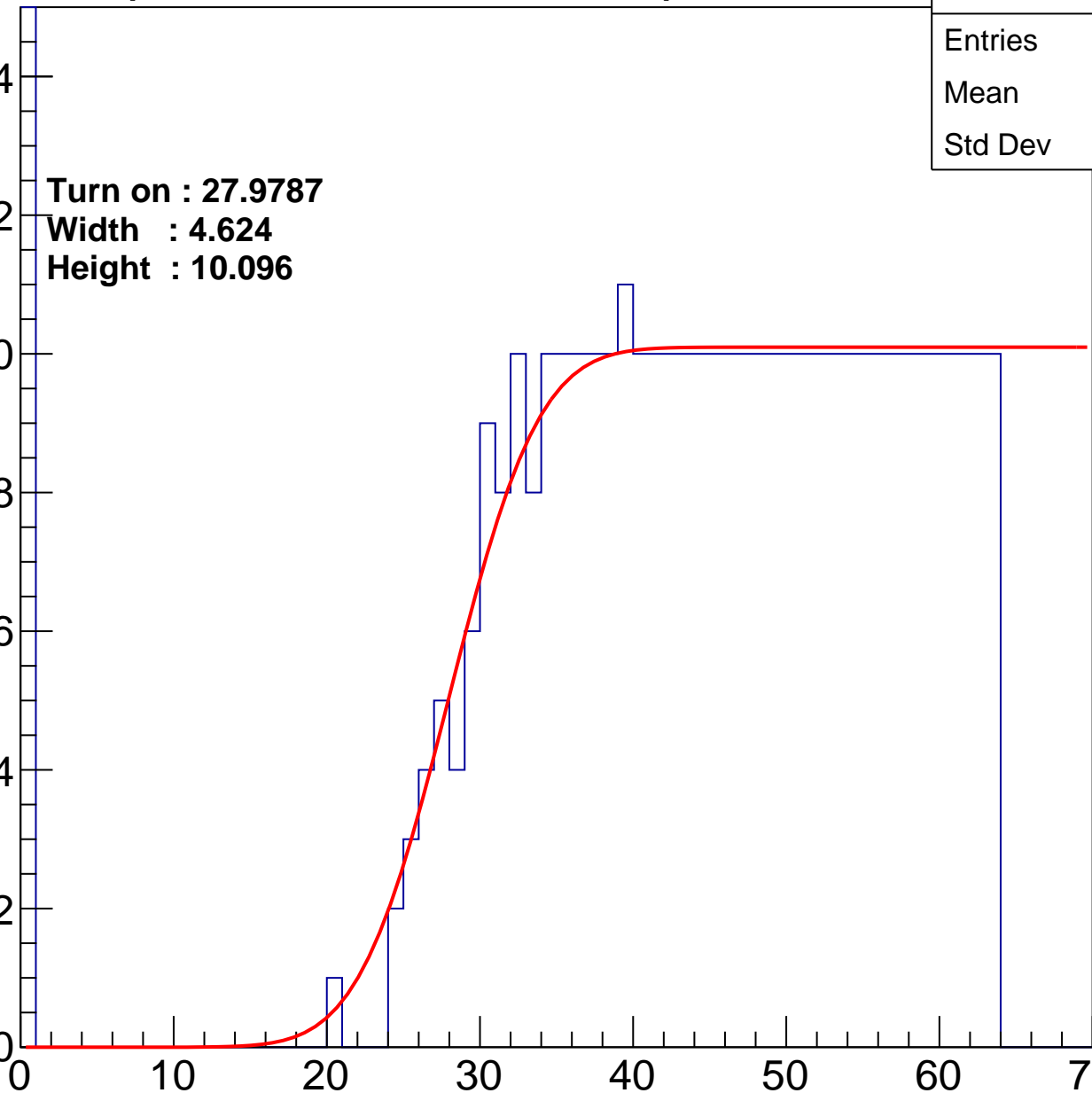
Width : 4.624

Height : 10.096

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch112

calib_packv5_041523_1651.root, FC#0, port C2

Entries	453
Mean	38.05
Std Dev	18.16

Turn on : 24.6296

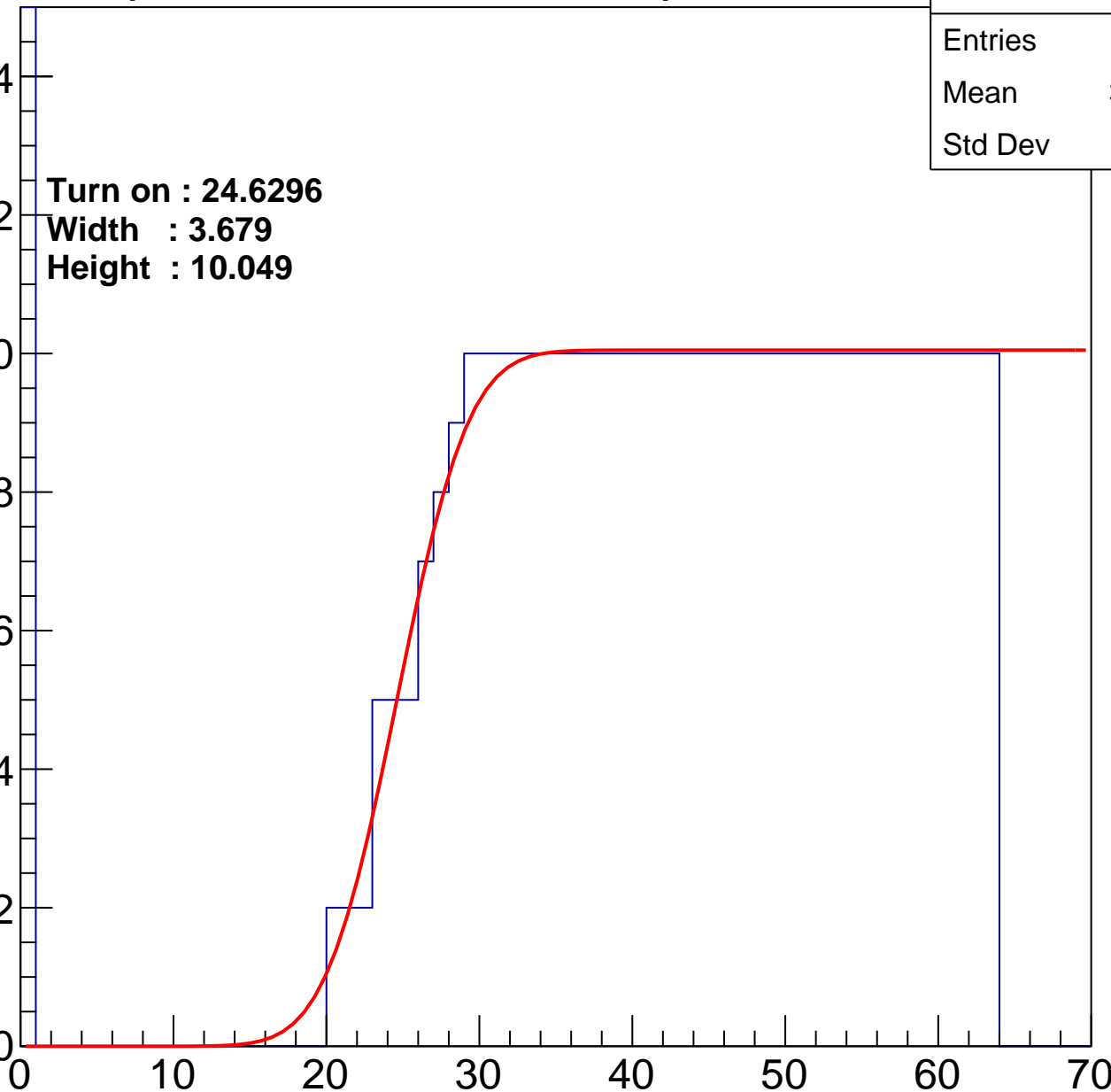
Width : 3.679

Height : 10.049

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch113

calib_packv5_041523_1651.root, FC#0, port C2

Entries	443
Mean	38.28
Std Dev	18.38

Turn on : 26.9233

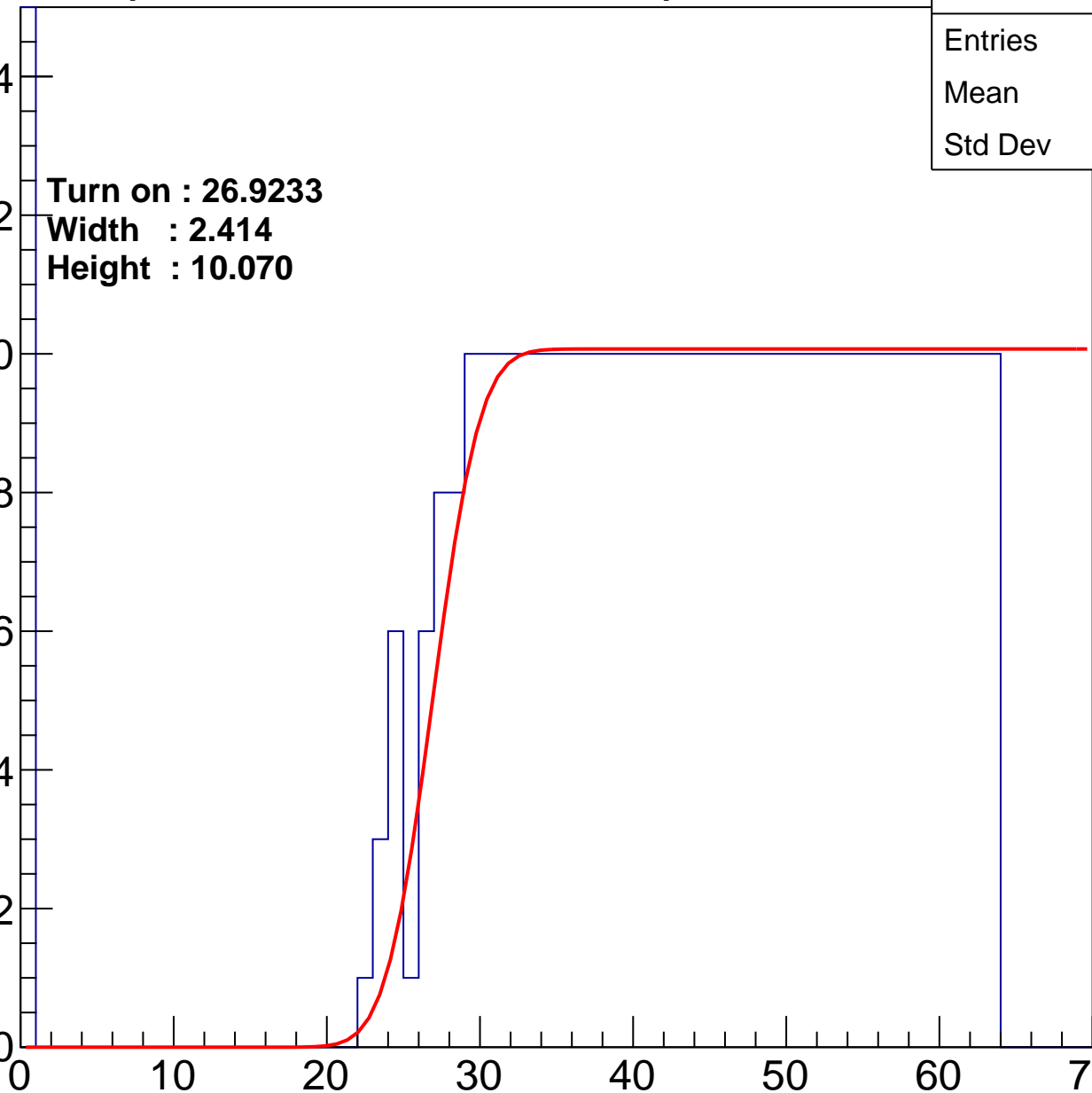
Width : 2.414

Height : 10.070

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch114

calib_packv5_041523_1651.root, FC#0, port C2

Entries	409
Mean	40.11
Std Dev	17.55

Turn on : 27.9116

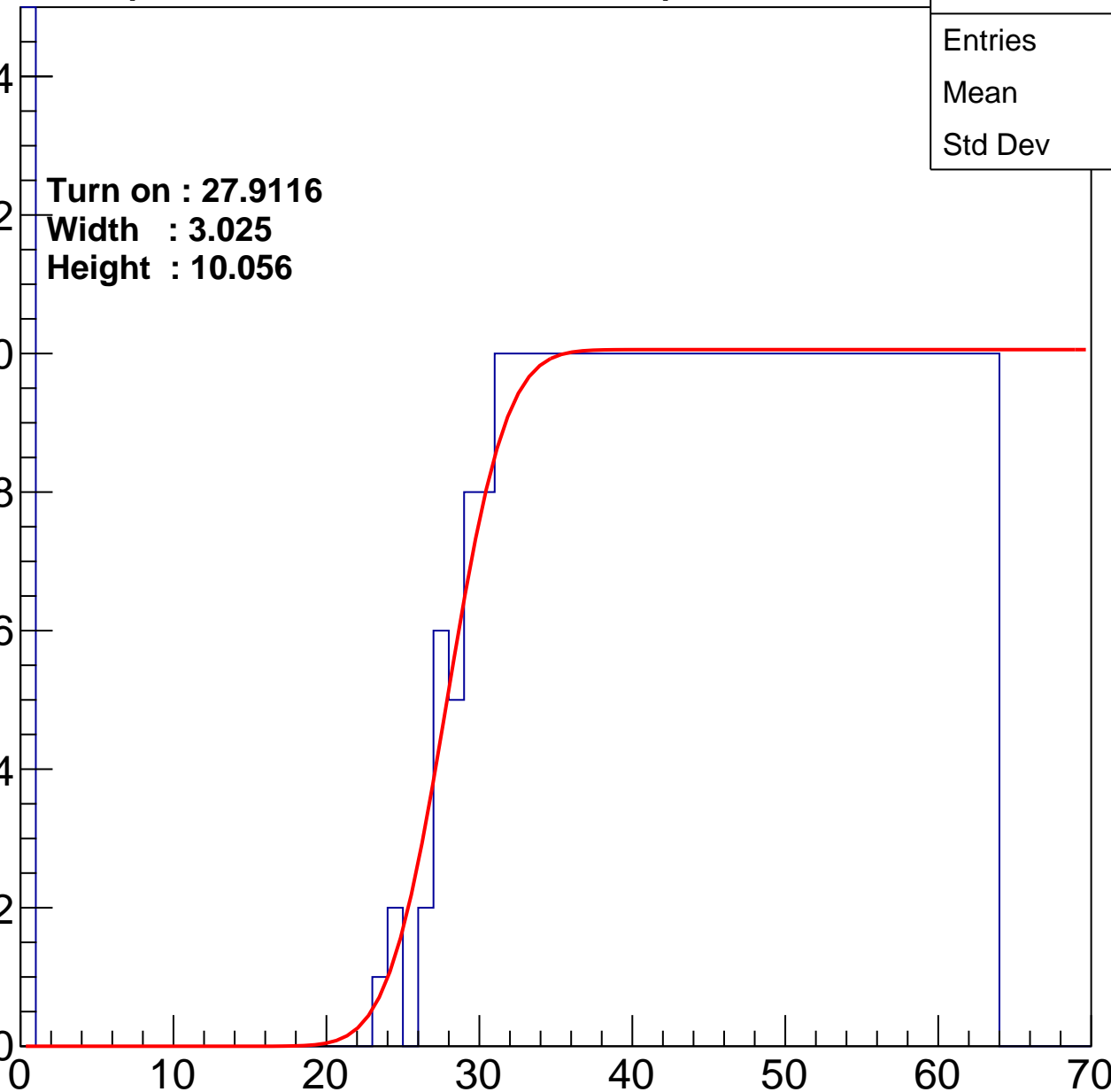
Width : 3.025

Height : 10.056

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch115

calib_packv5_041523_1651.root, FC#0, port C2

Entries	439
Mean	38.22
Std Dev	18.61

Turn on : 26.4755

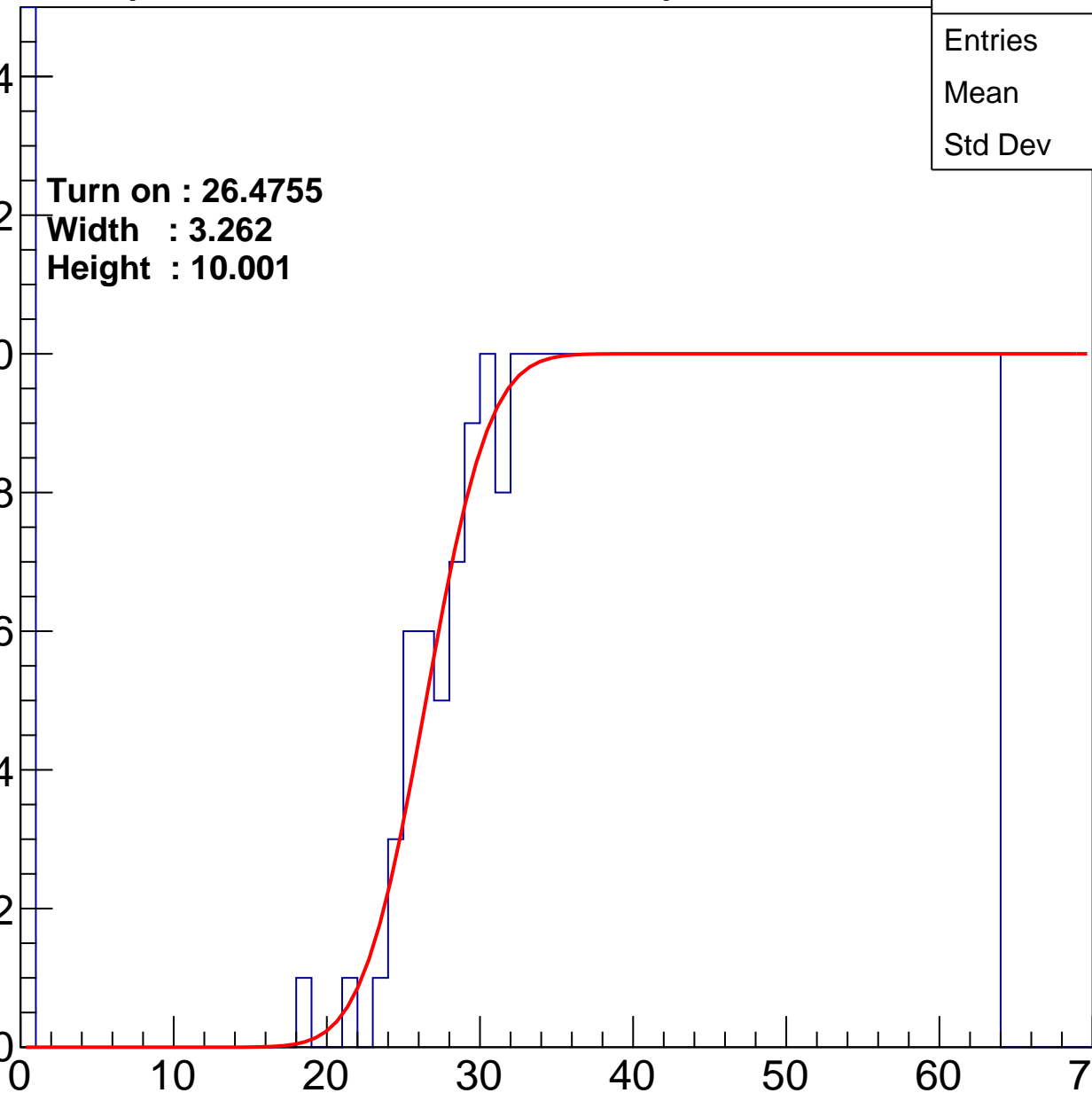
Width : 3.262

Height : 10.001

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch116

calib_packv5_041523_1651.root, FC#0, port C2

Entries	413
Mean	40.33
Std Dev	16.94

Turn on : 27.1551

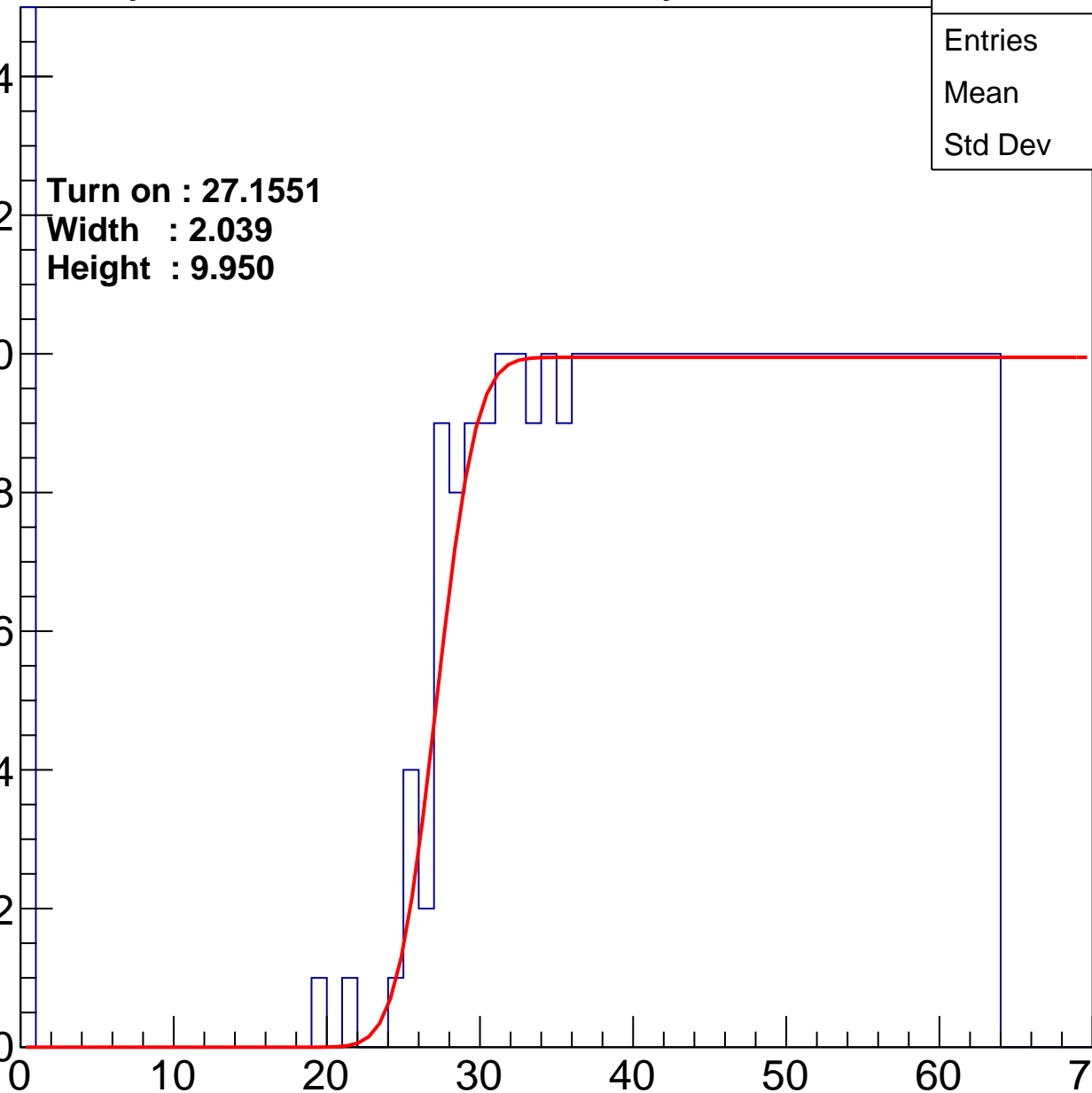
Width : 2.039

Height : 9.950

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch117

calib_packv5_041523_1651.root, FC#0, port C2

Entries	430
Mean	39.35
Std Dev	17.49

Turn on : 25.6636

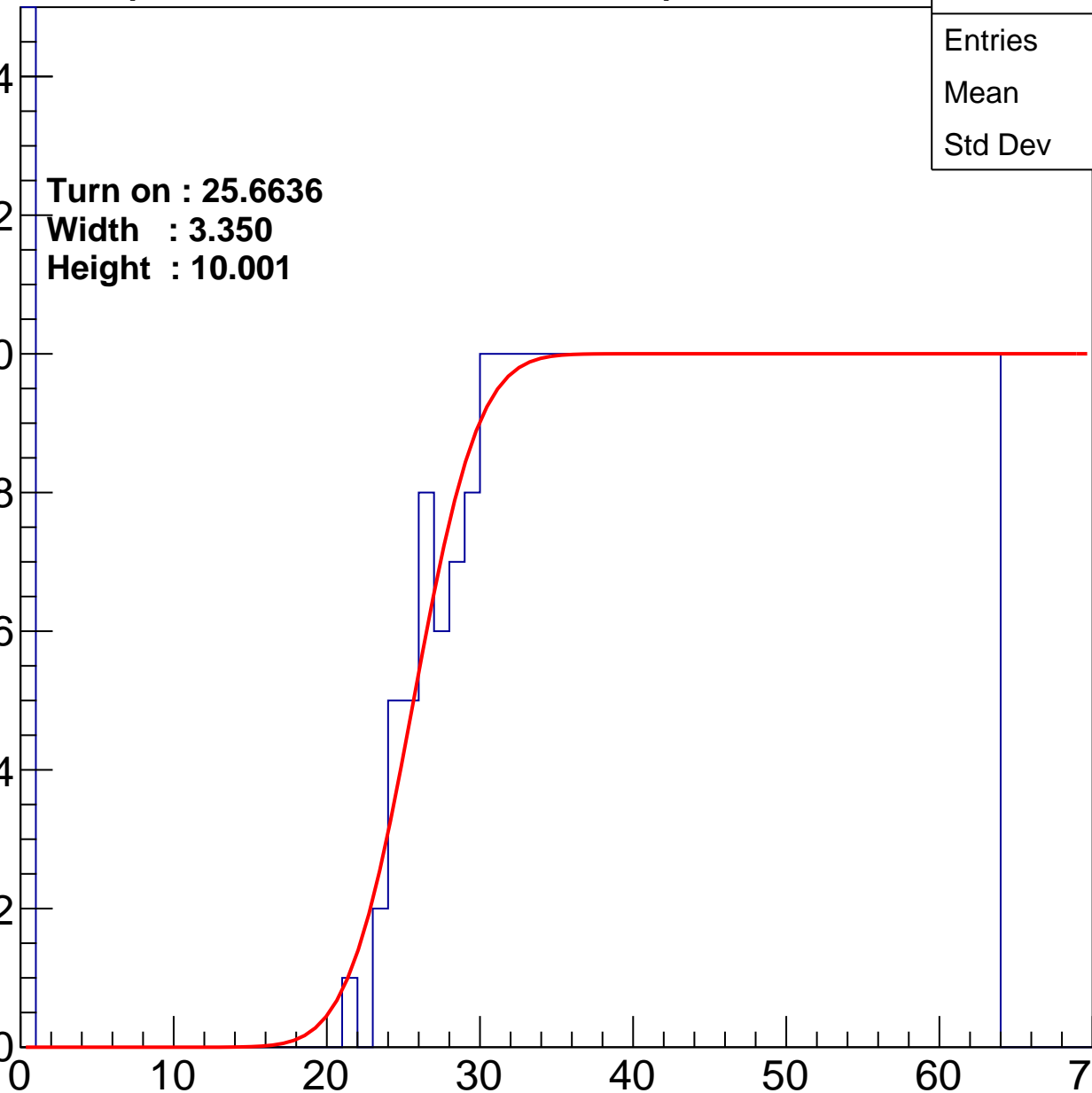
Width : 3.350

Height : 10.001

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch118

calib_packv5_041523_1651.root, FC#0, port C2

Entries	443
Mean	39.8
Std Dev	15.96

Turn on : 23.2937

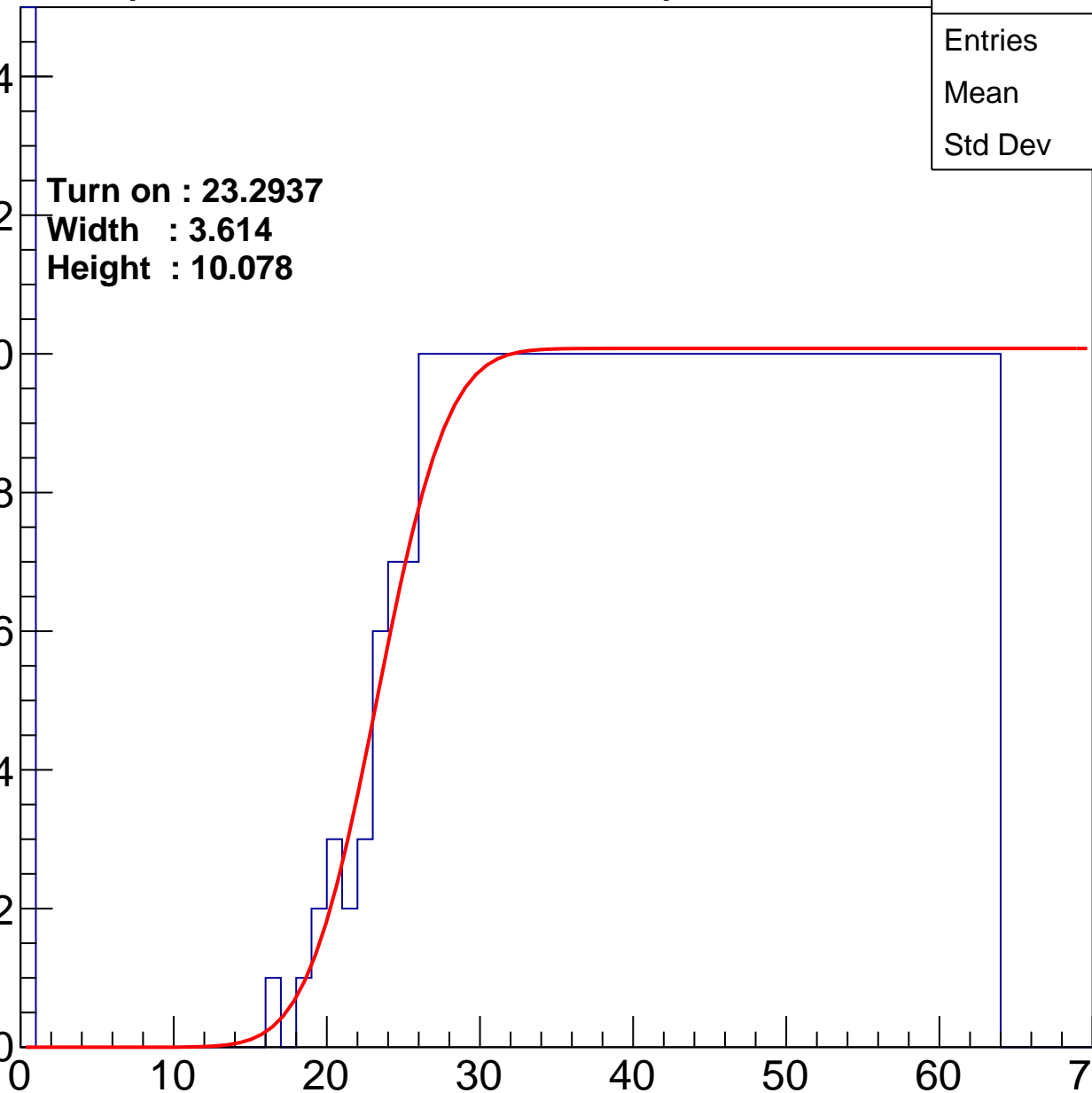
Width : 3.614

Height : 10.078

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch119

calib_packv5_041523_1651.root, FC#0, port C2

Entries	445
Mean	38.08
Std Dev	18.53

Turn on : 25.9913

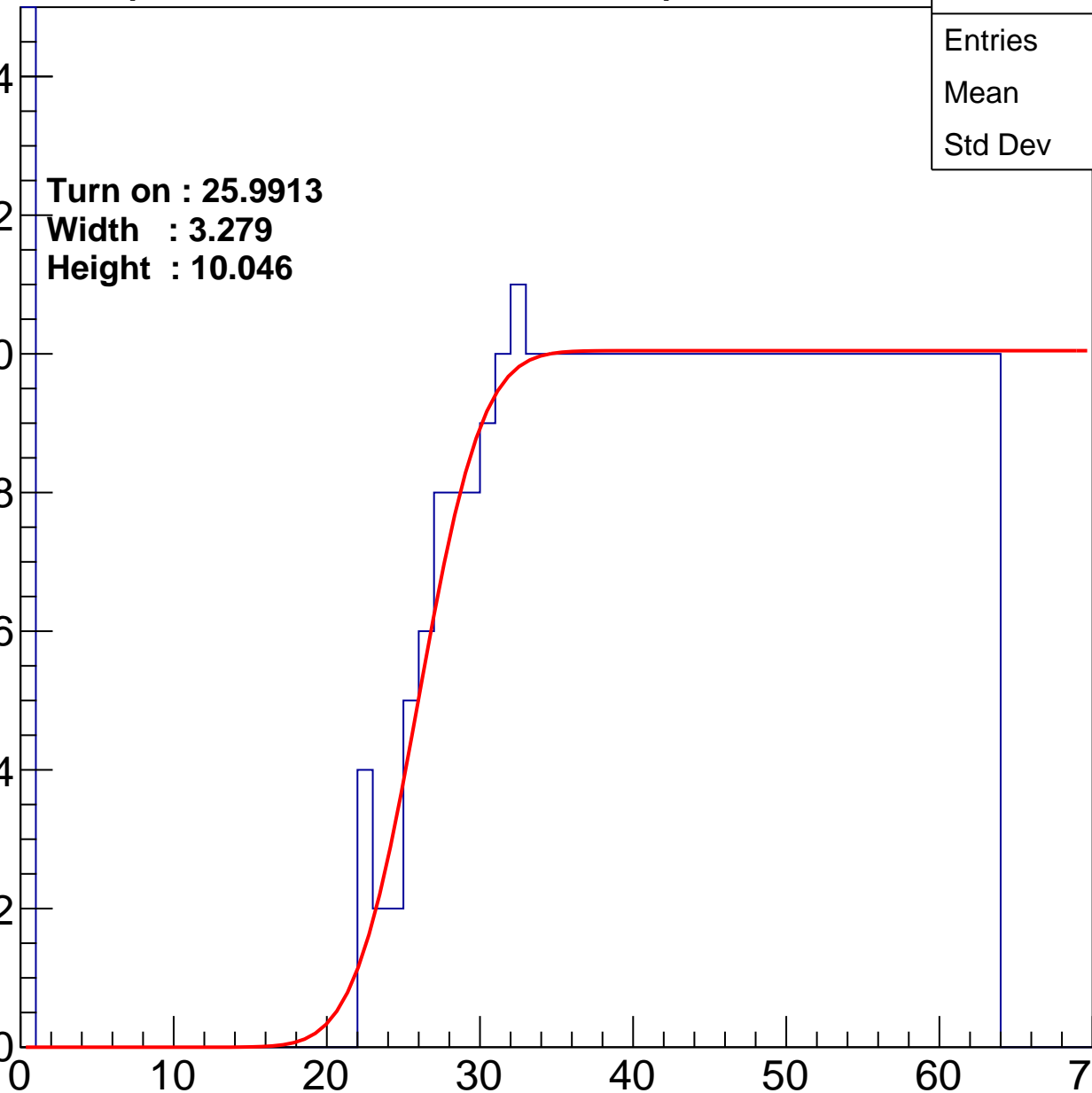
Width : 3.279

Height : 10.046

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch120

calib_packv5_041523_1651.root, FC#0, port C2

Entries	434
Mean	39.24
Std Dev	17.41

Turn on : 25.6549

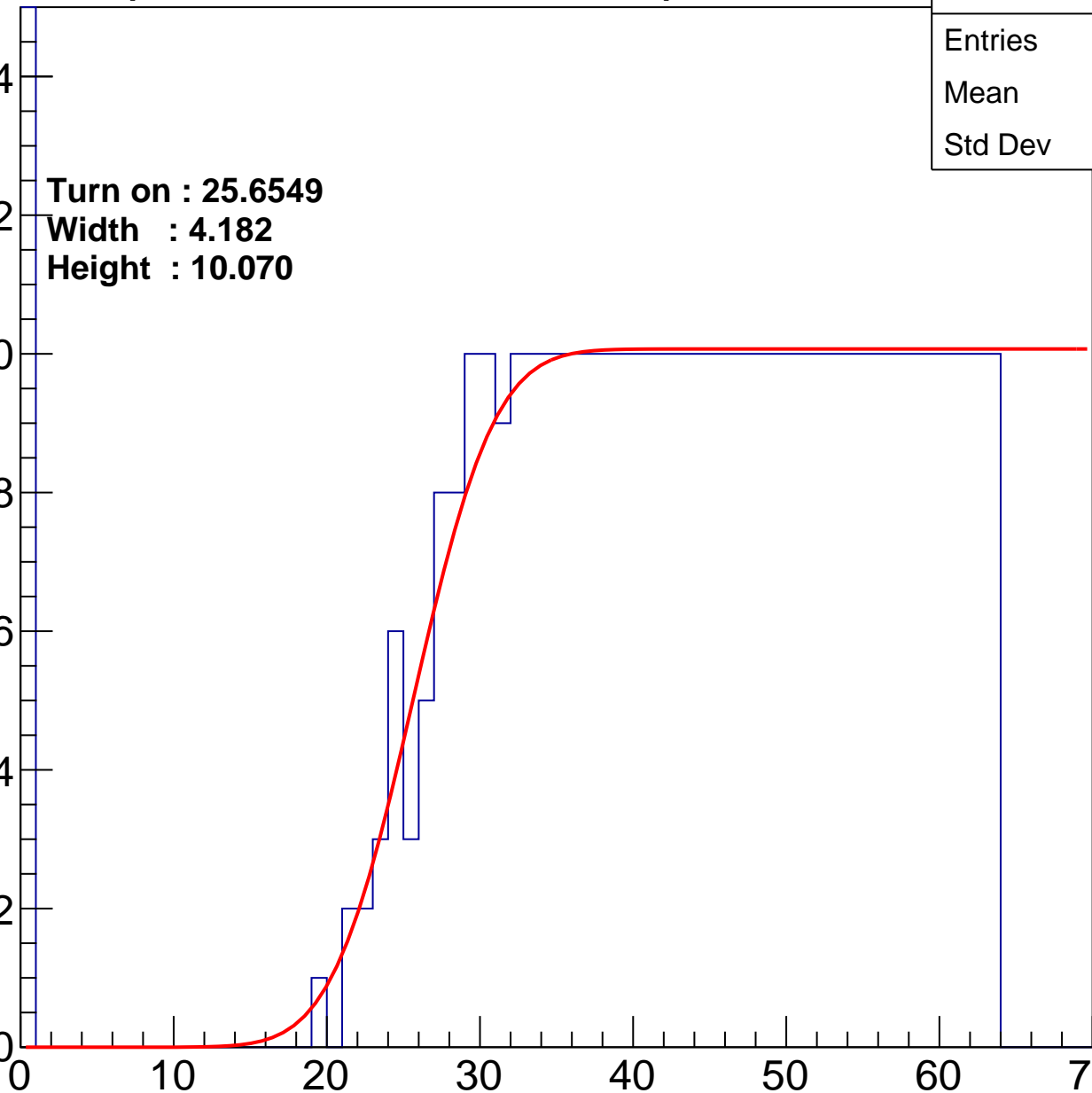
Width : 4.182

Height : 10.070

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch121

calib_packv5_041523_1651.root, FC#0, port C2

Entries	416
Mean	40.28
Std Dev	16.84

Turn on : 26.9358

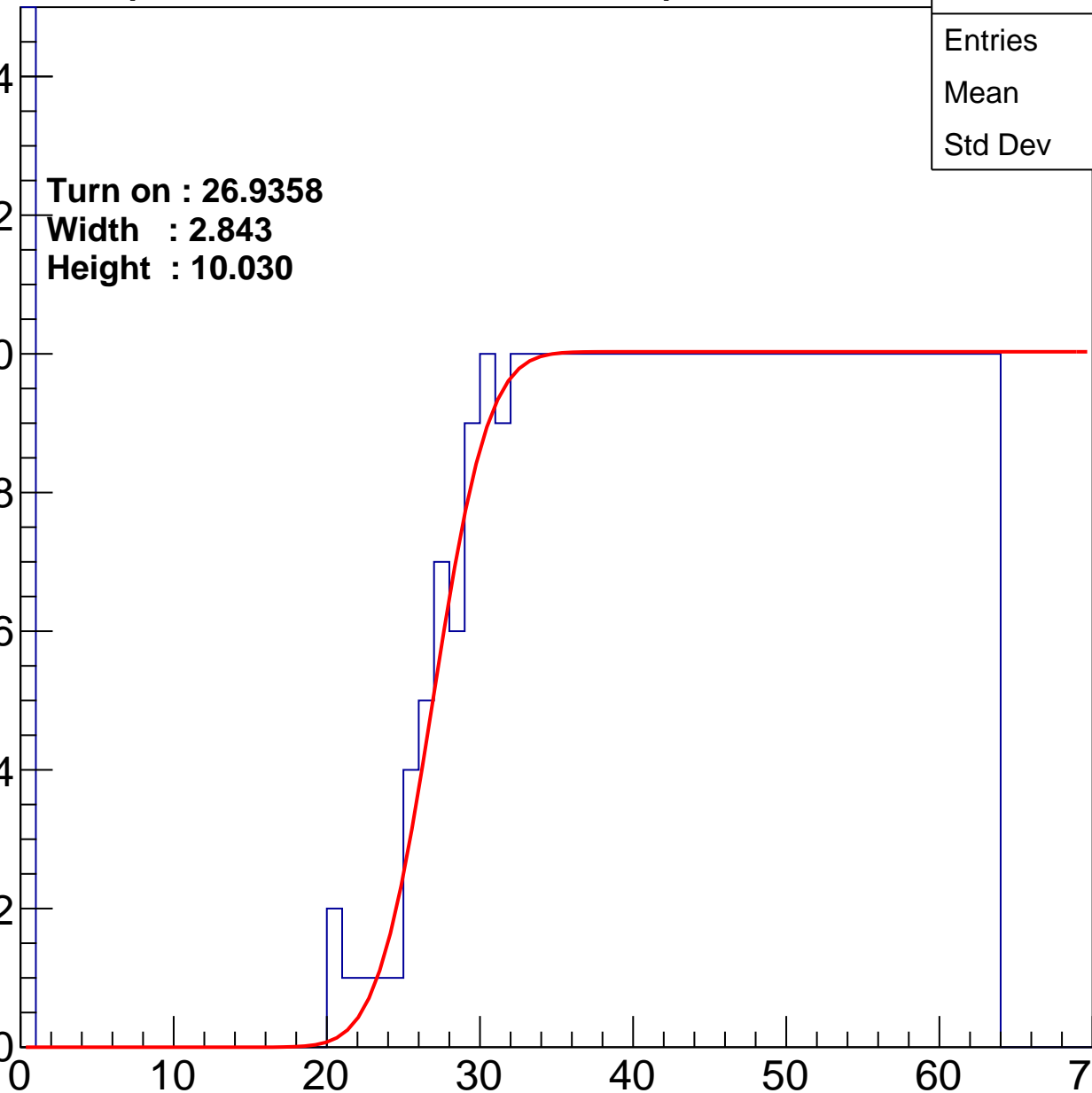
Width : 2.843

Height : 10.030

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch122

calib_packv5_041523_1651.root, FC#0, port C2

Entries	449
Mean	37.98
Std Dev	18.51

Turn on : 25.4986

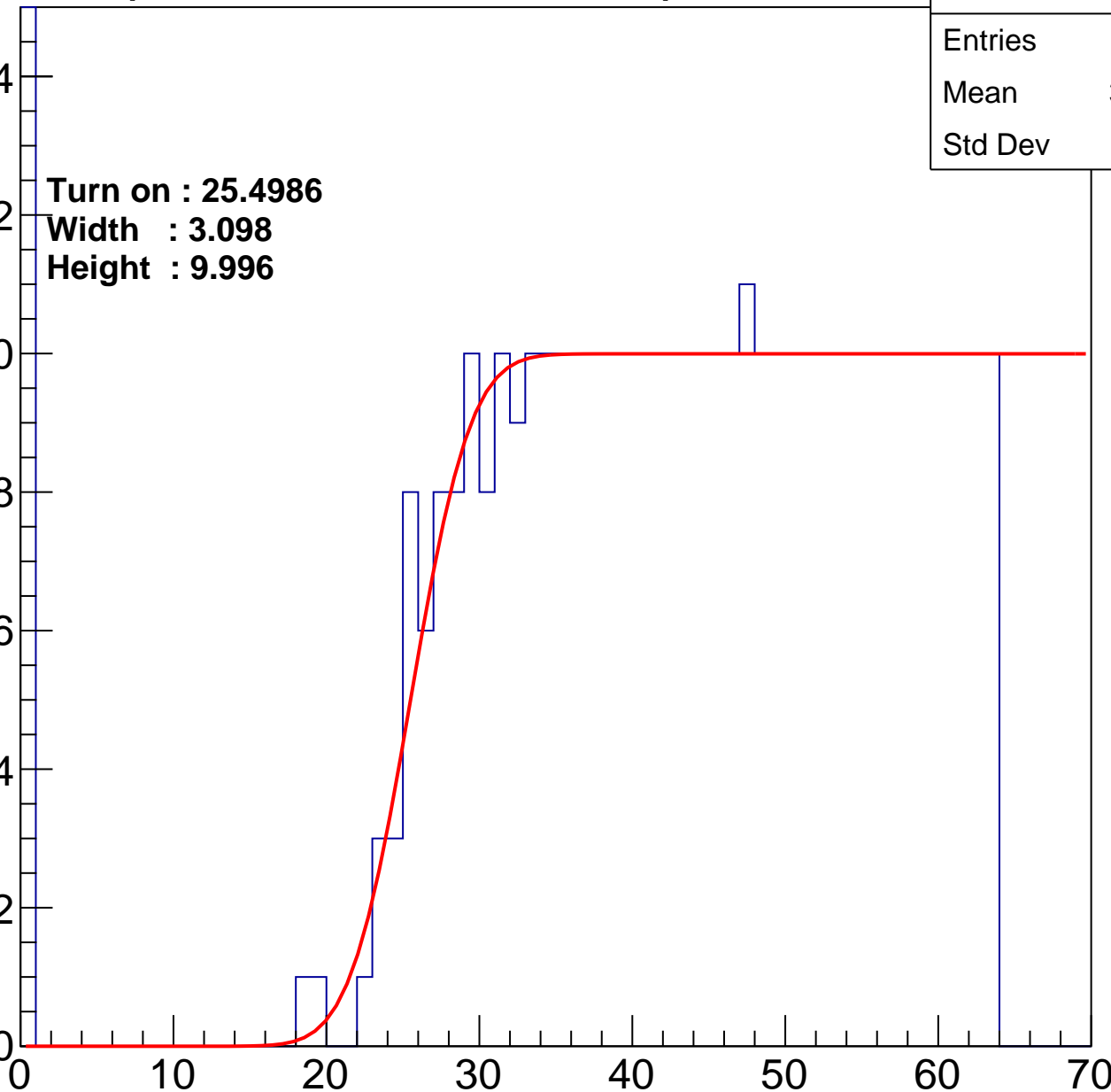
Width : 3.098

Height : 9.996

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch123

calib_packv5_041523_1651.root, FC#0, port C2

Entries	432
Mean	39.22
Std Dev	17.57

Turn on : 25.5896

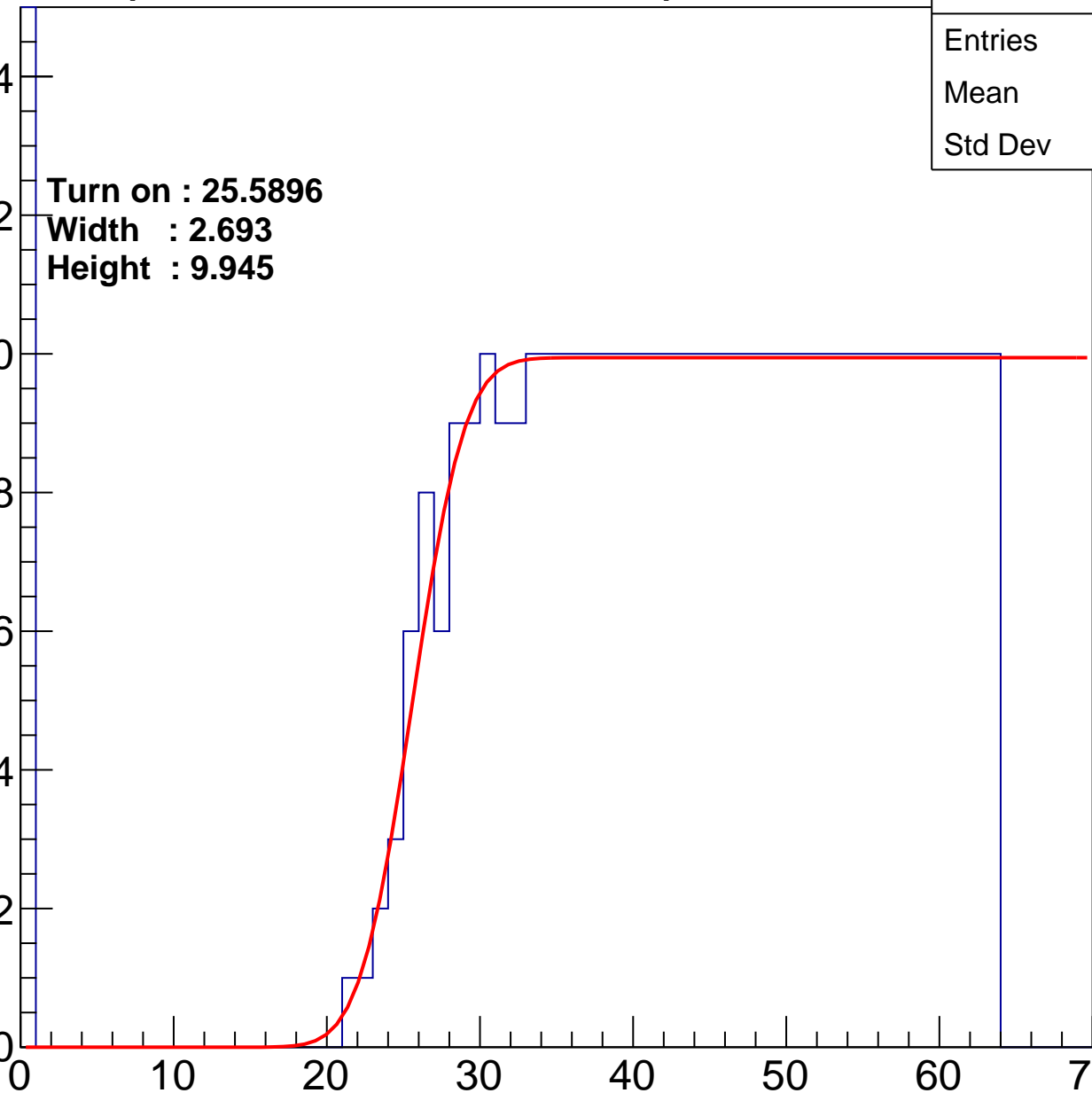
Width : 2.693

Height : 9.945

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch124

calib_packv5_041523_1651.root, FC#0, port C2

Entries	434
Mean	39.39
Std Dev	17.17

Turn on : 25.4608

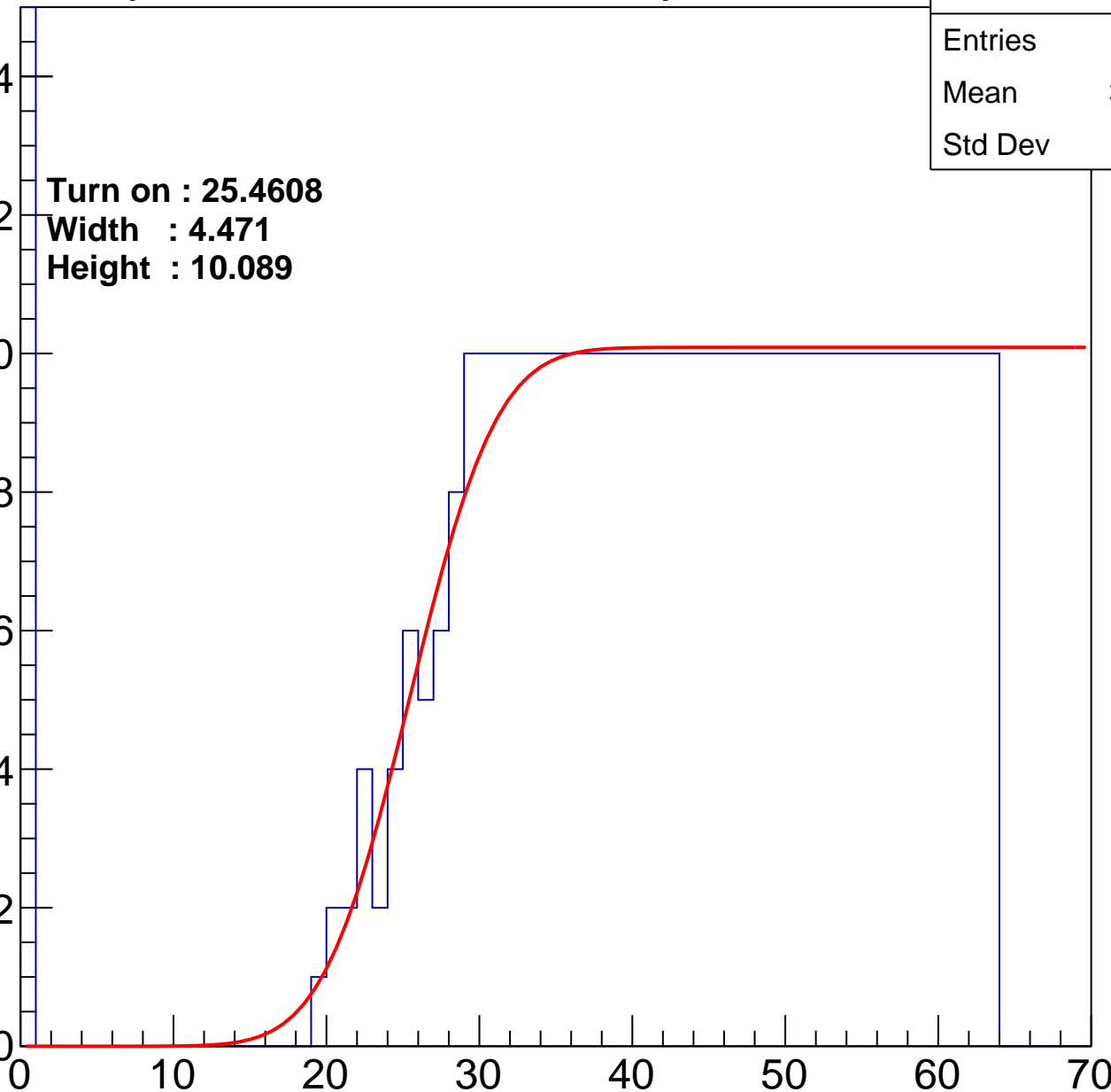
Width : 4.471

Height : 10.089

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch125

calib_packv5_041523_1651.root, FC#0, port C2

Entries	416
Mean	39.93
Std Dev	17.41

Turn on : 27.0294

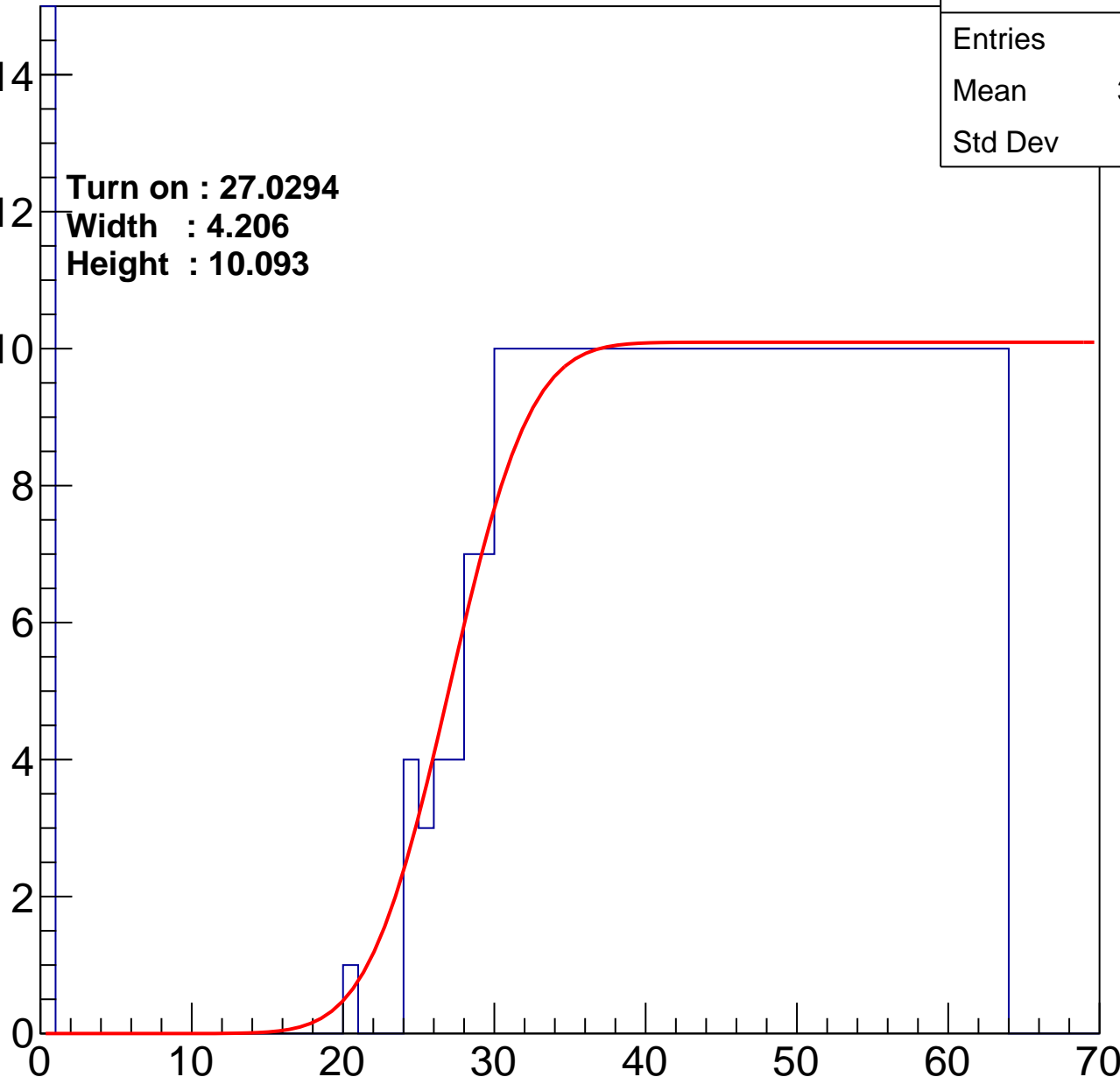
Width : 4.206

Height : 10.093

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch126

calib_packv5_041523_1651.root, FC#0, port C2

Entries	467
Mean	37.54
Std Dev	18.13

Turn on : 23.7643

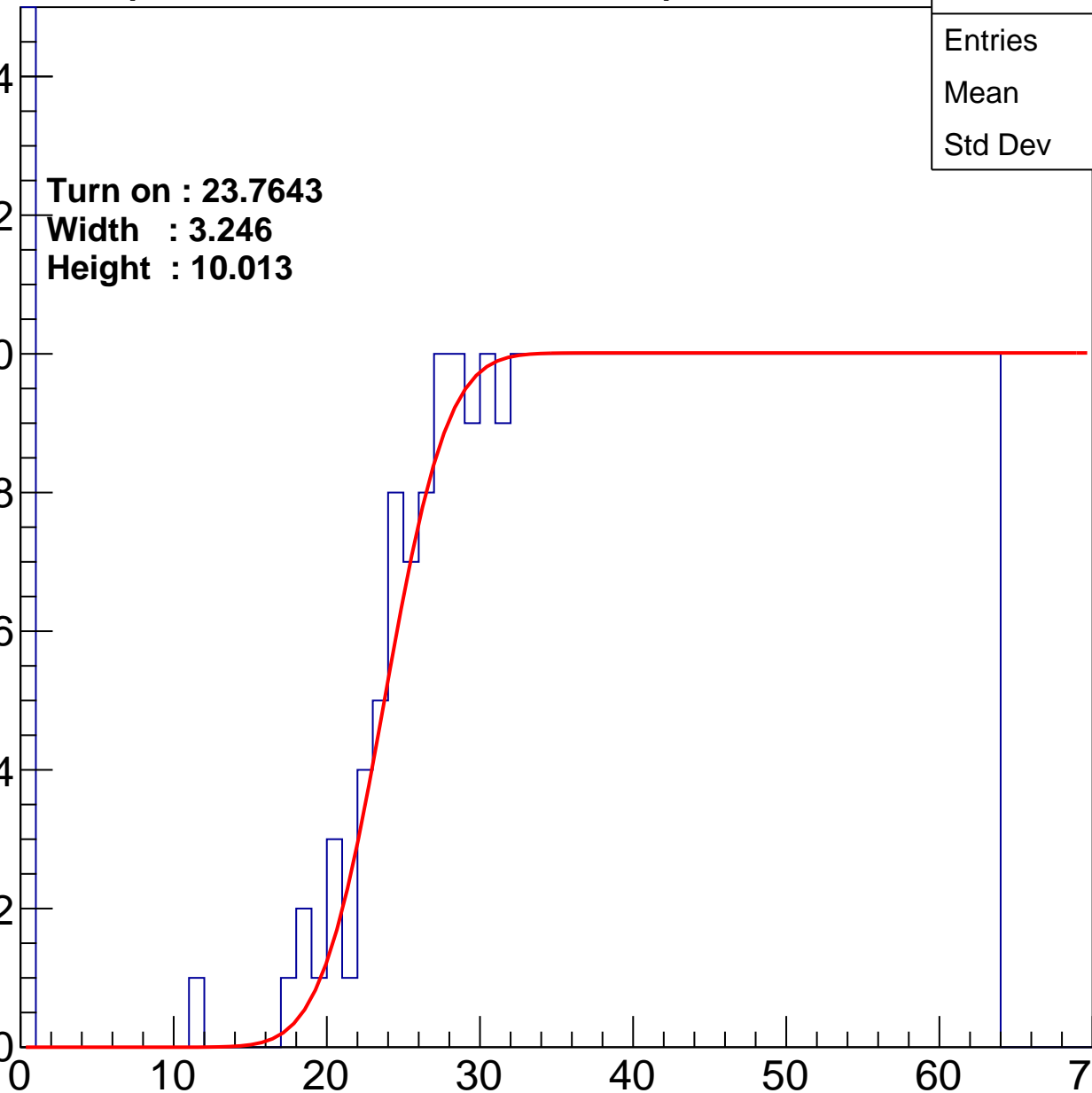
Width : 3.246

Height : 10.013

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch127

calib_packv5_041523_1651.root, FC#0, port C2

Entries	451
Mean	38.06
Std Dev	18.22

Turn on : 24.9621

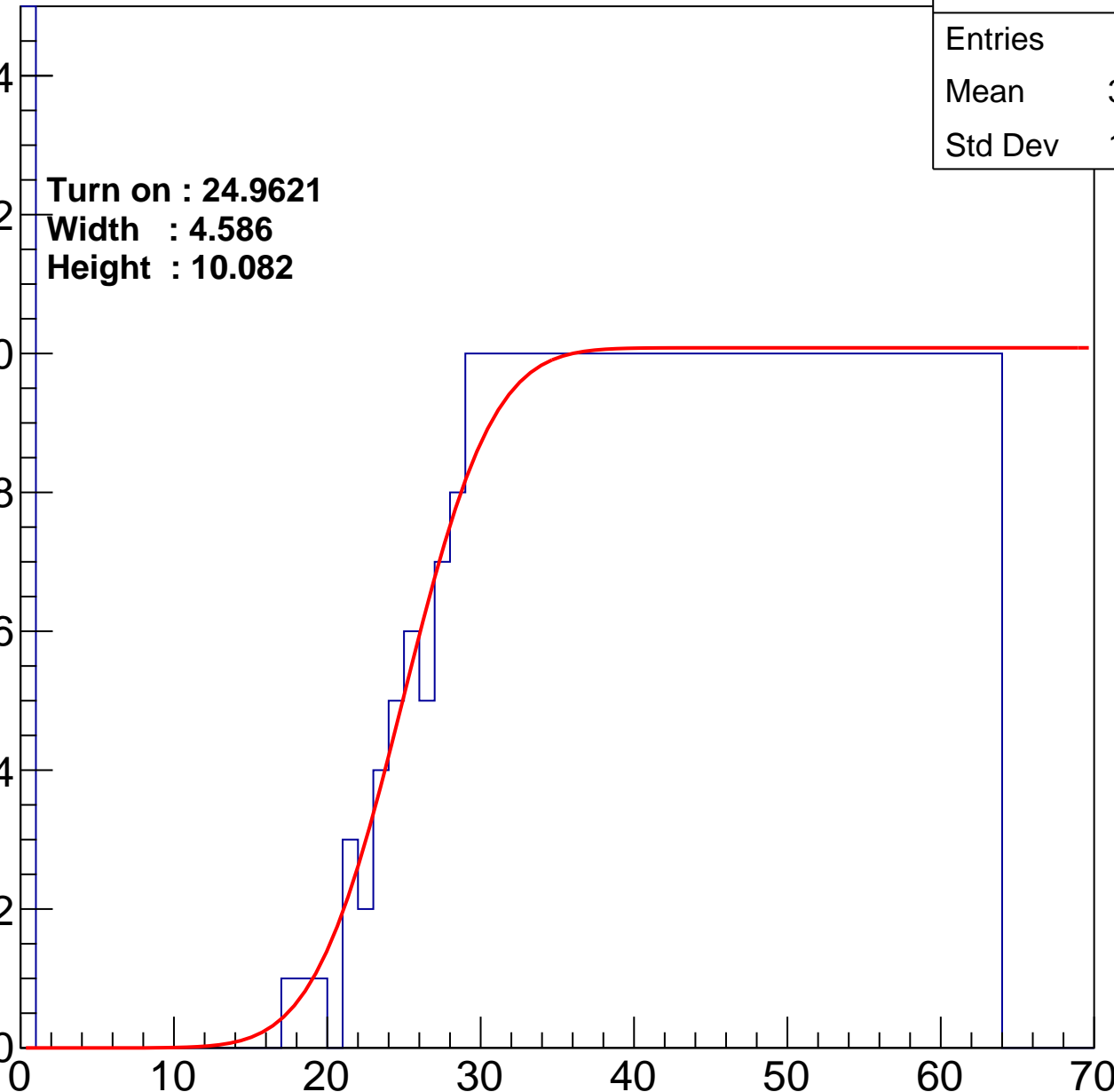
Width : 4.586

Height : 10.082

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U12-ch127

calib_packv5_041523_1651.root, FC#0, port C2

Entries	451
Mean	38.06
Std Dev	18.22

Turn on : 24.9621

Width : 4.586

Height : 10.082

Entry

14
12
10
8
6
4
2
0

ampl

