

B1L101S, U15-ch0

calib_packv5_042523_0143.root, FC#0, port D2

Entries	389
Mean	43.8
Std Dev	11.77

Turn on : 25.2831

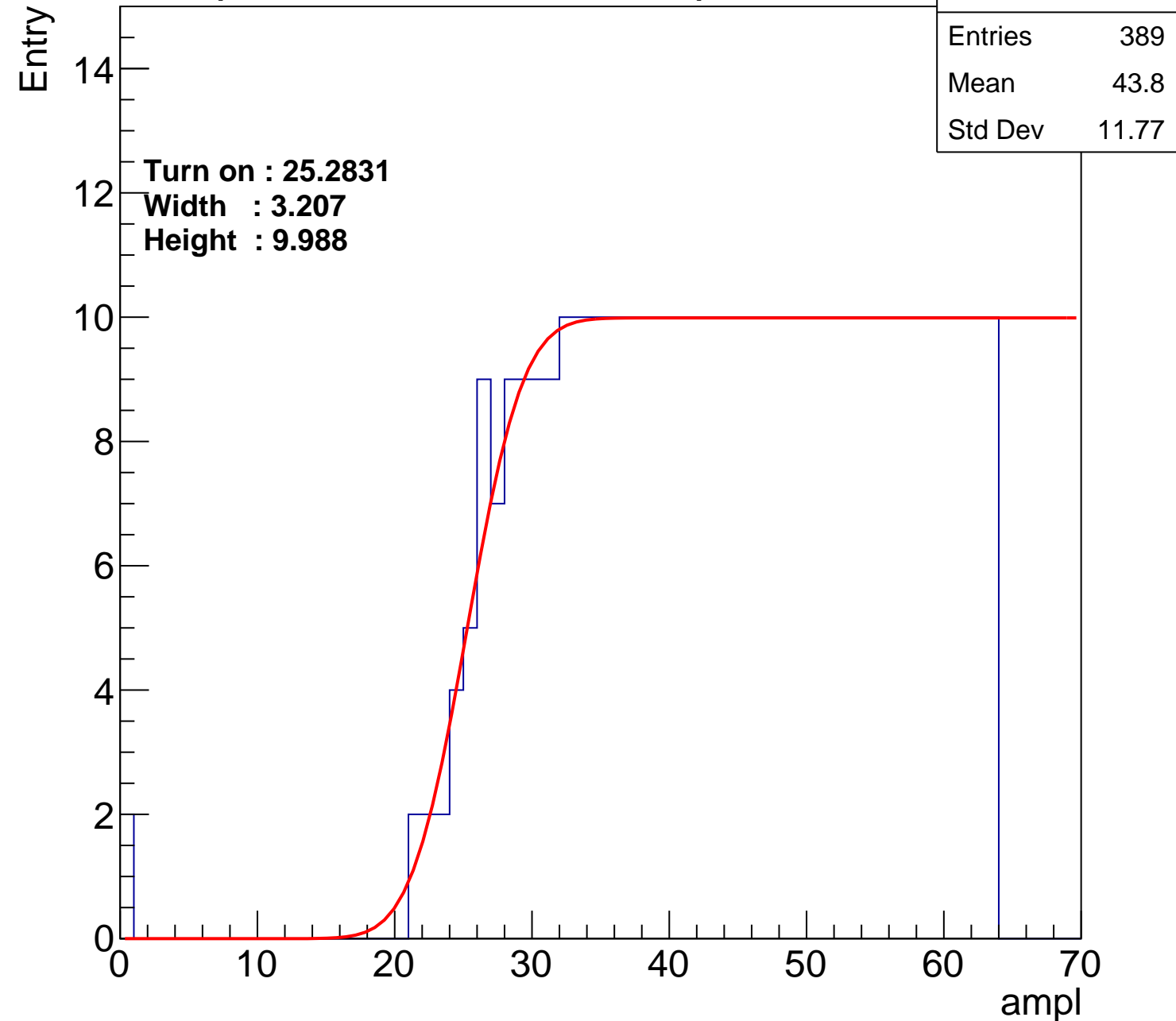
Width : 3.207

Height : 9.988

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch1

calib_packv5_042523_0143.root, FC#0, port D2

Entries	370
Mean	44.67
Std Dev	11.48

Turn on : 28.1496

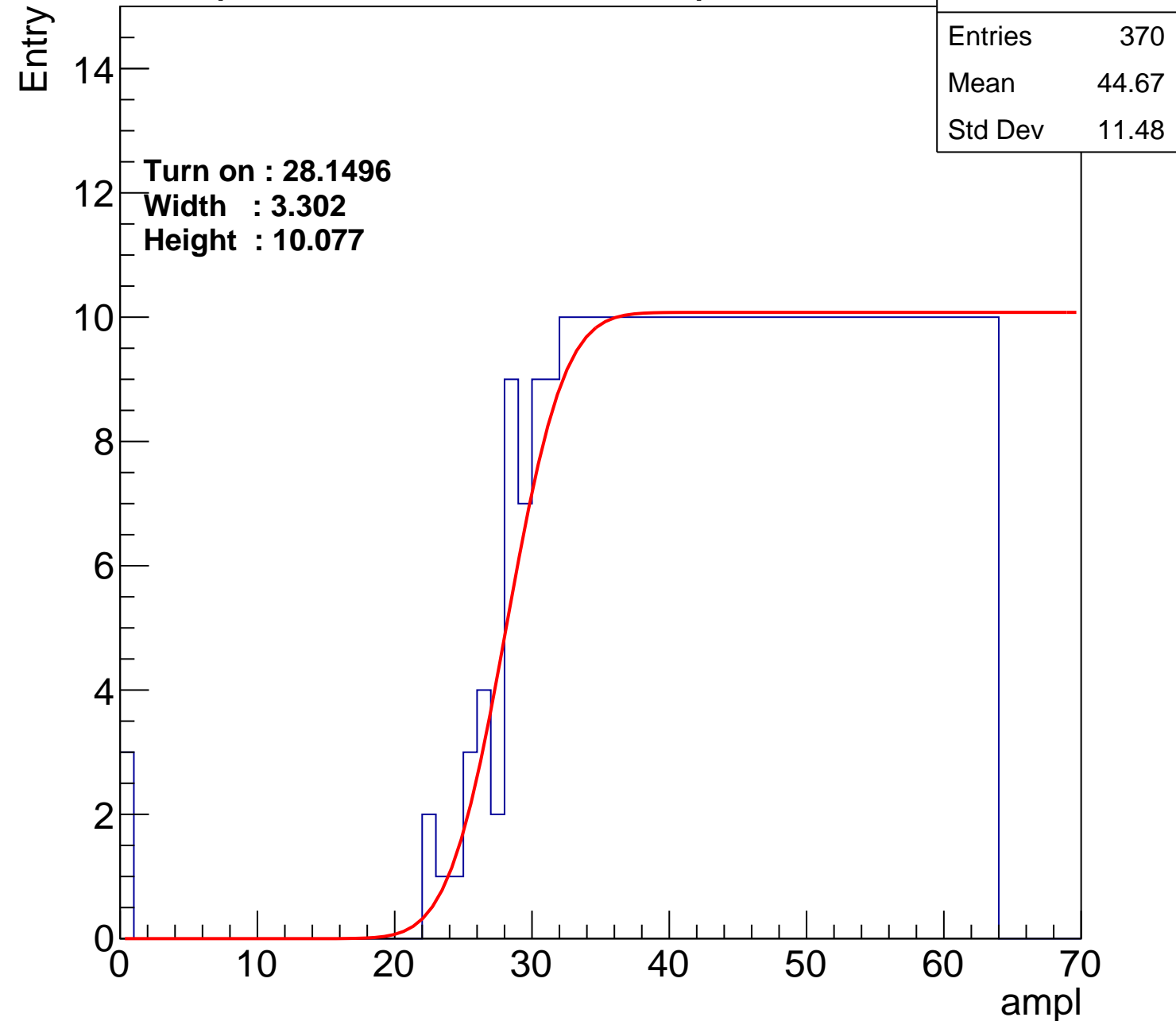
Width : 3.302

Height : 10.077

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch2

calib_packv5_042523_0143.root, FC#0, port D2

Entries	382
Mean	43.95
Std Dev	12.11

Turn on : 26.6317

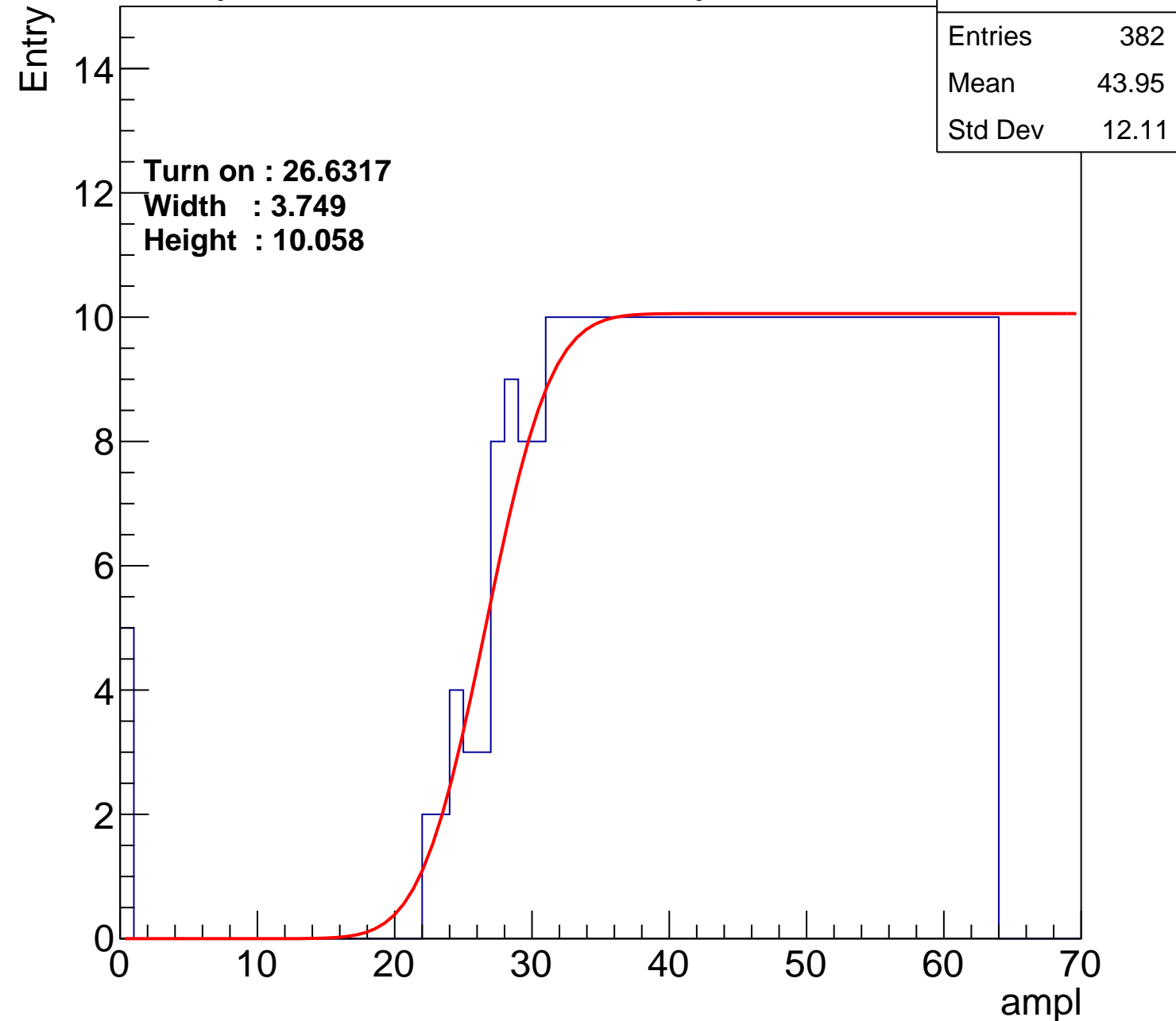
Width : 3.749

Height : 10.058

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch3

calib_packv5_042523_0143.root, FC#0, port D2

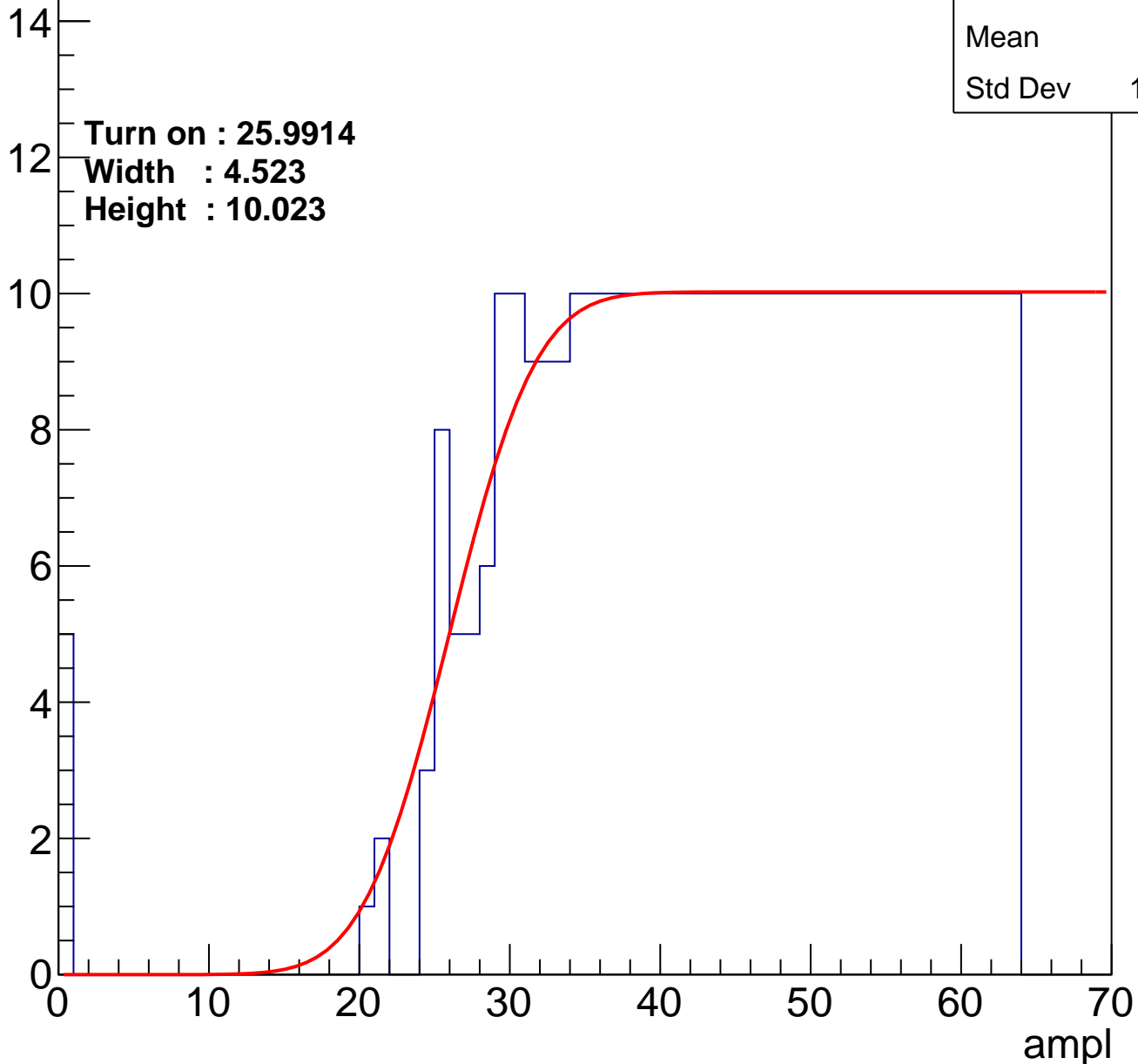
Entries	382
Mean	43.9
Std Dev	12.18

Turn on : 25.9914

Width : 4.523

Height : 10.023

Entry



B1L101S, U15-ch4

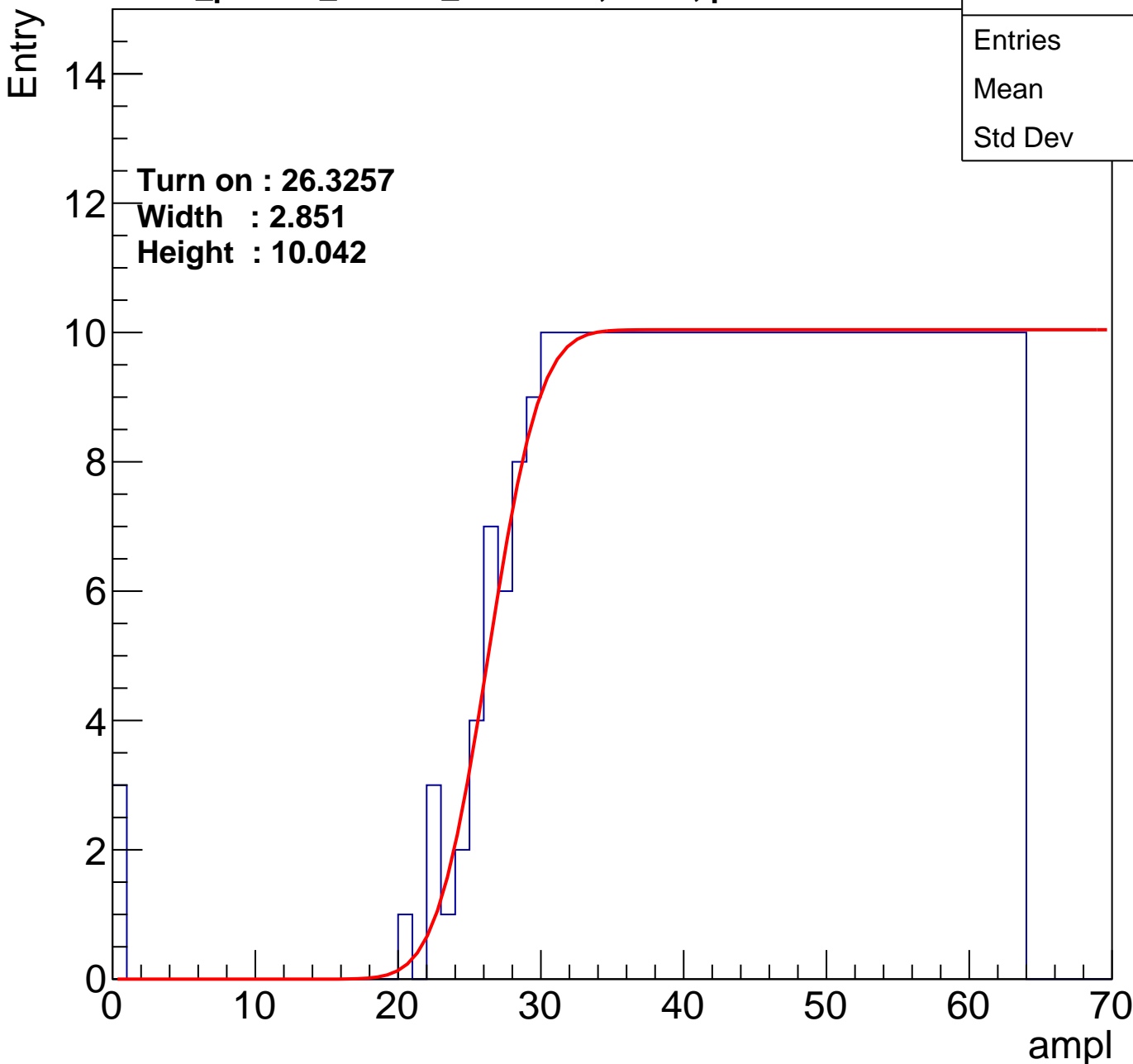
calib_packv5_042523_0143.root, FC#0, port D2

Turn on : 26.3257

Width : 2.851

Height : 10.042

Entries	384
Mean	44
Std Dev	11.8



B1L101S, U15-ch5

calib_packv5_042523_0143.root, FC#0, port D2

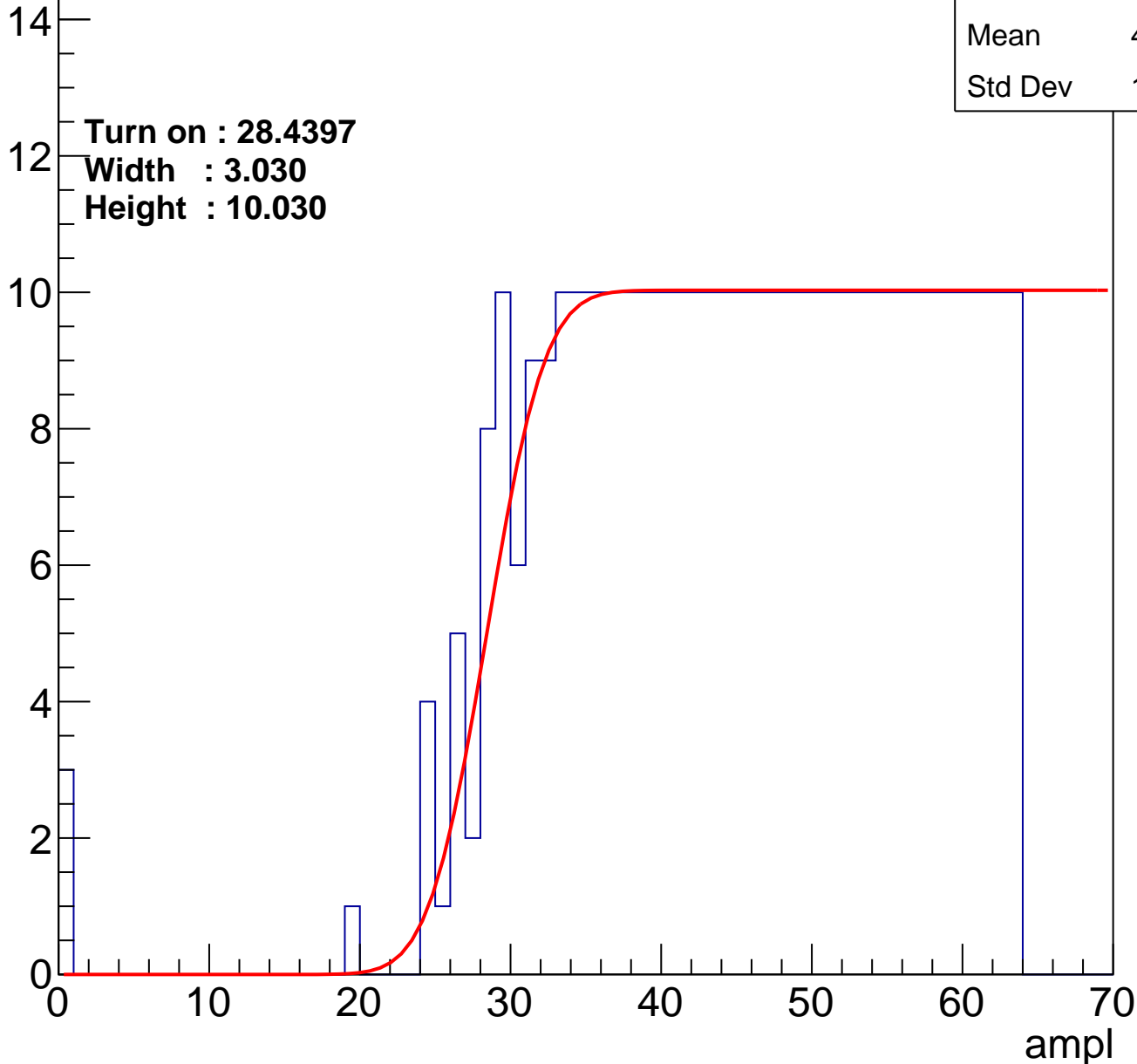
Entries	368
Mean	44.74
Std Dev	11.47

Turn on : 28.4397

Width : 3.030

Height : 10.030

Entry



B1L101S, U15-ch6

calib_packv5_042523_0143.root, FC#0, port D2

Entries	368
Mean	44.59
Std Dev	11.88

Turn on : 28.5071

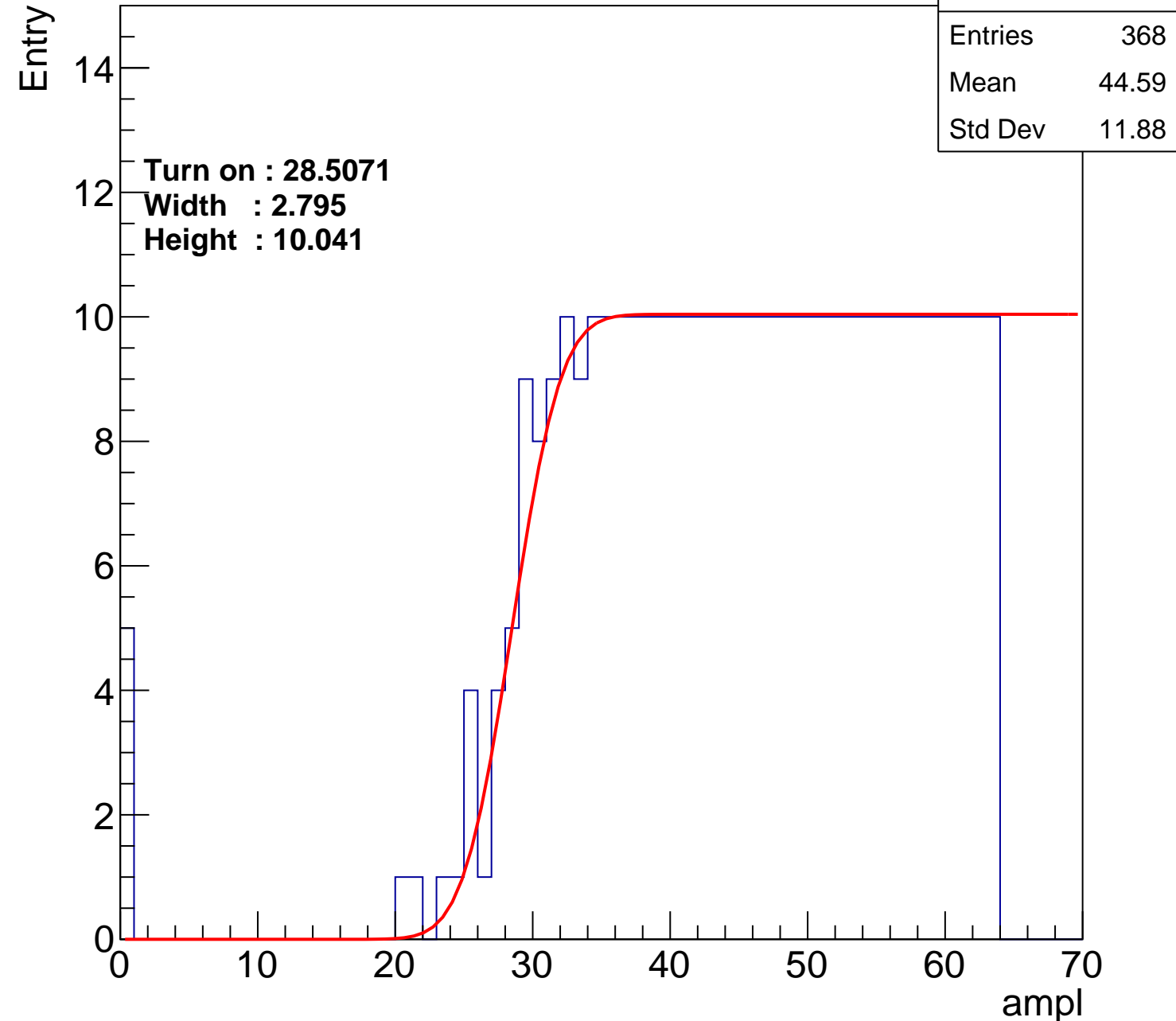
Width : 2.795

Height : 10.041

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch7

calib_packv5_042523_0143.root, FC#0, port D2

Entries	366
Mean	44.96
Std Dev	11.14

Turn on : 27.9632

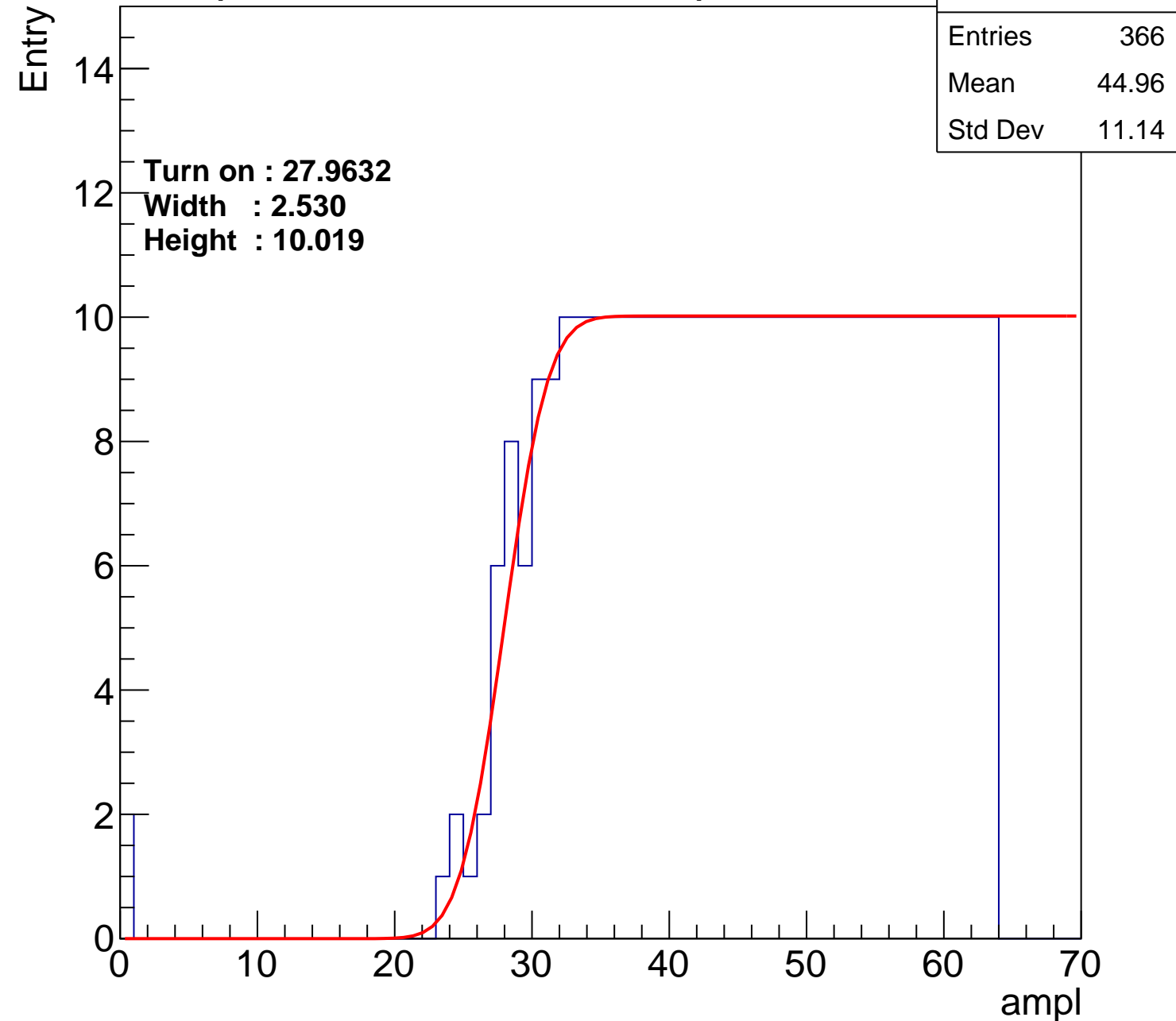
Width : 2.530

Height : 10.019

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch8

calib_packv5_042523_0143.root, FC#0, port D2

Entries	374
Mean	44.54
Std Dev	11.38

Turn on : 27.1726

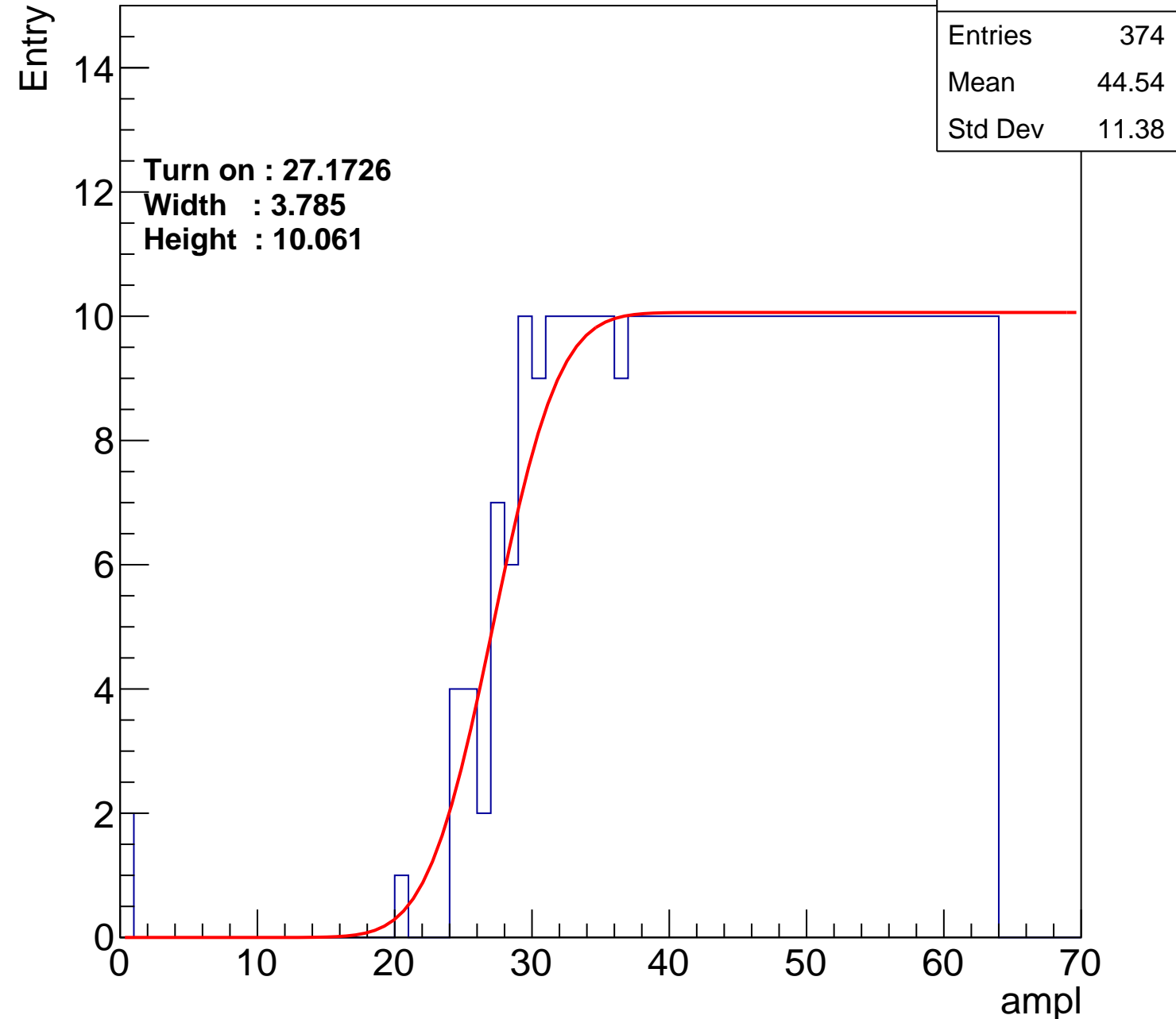
Width : 3.785

Height : 10.061

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch9

calib_packv5_042523_0143.root, FC#0, port D2

Entries	372
Mean	44.48
Std Dev	11.75

Turn on : 28.0645

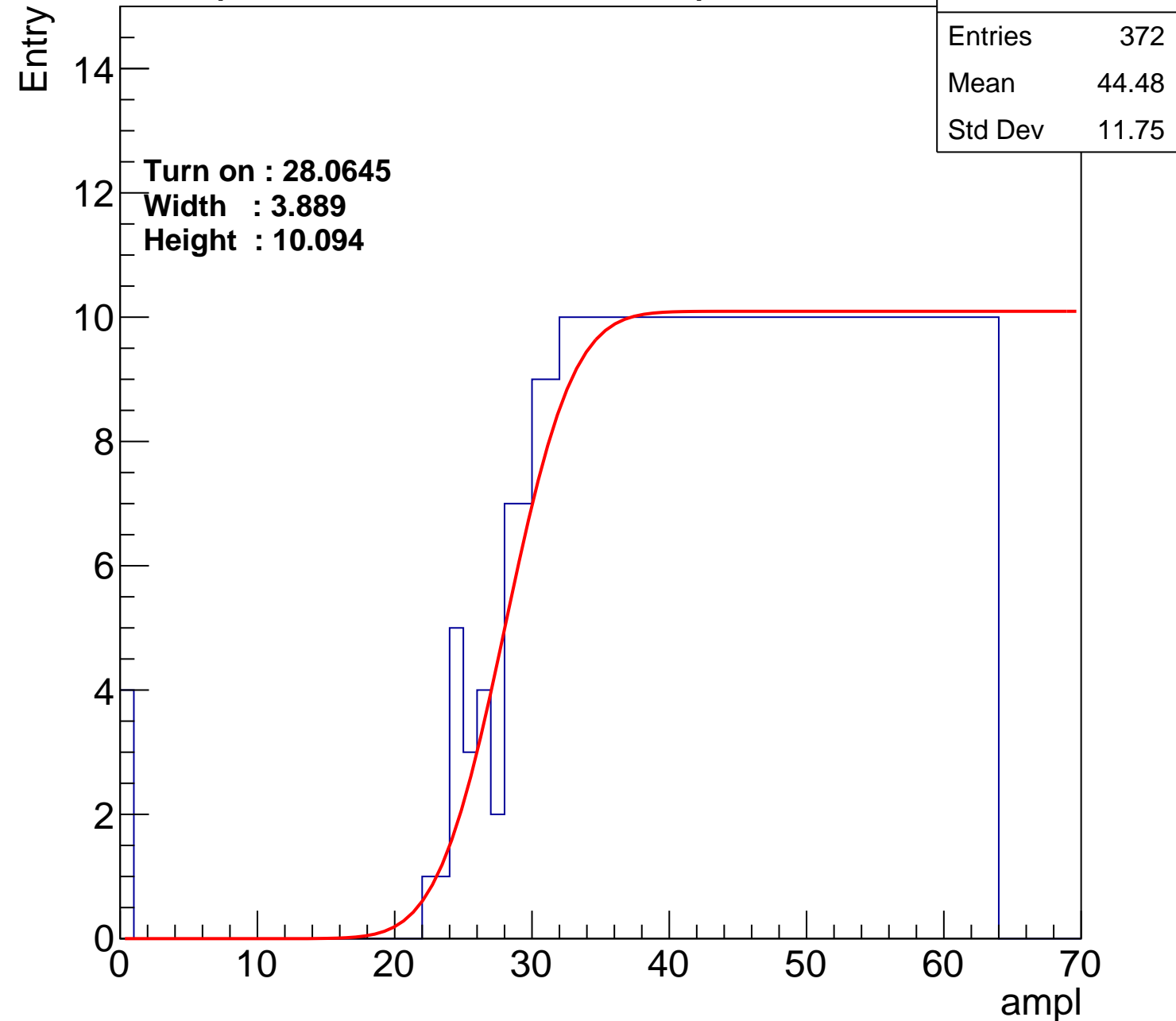
Width : 3.889

Height : 10.094

Entry

14
12
10
8
6
4
2
0

ampl

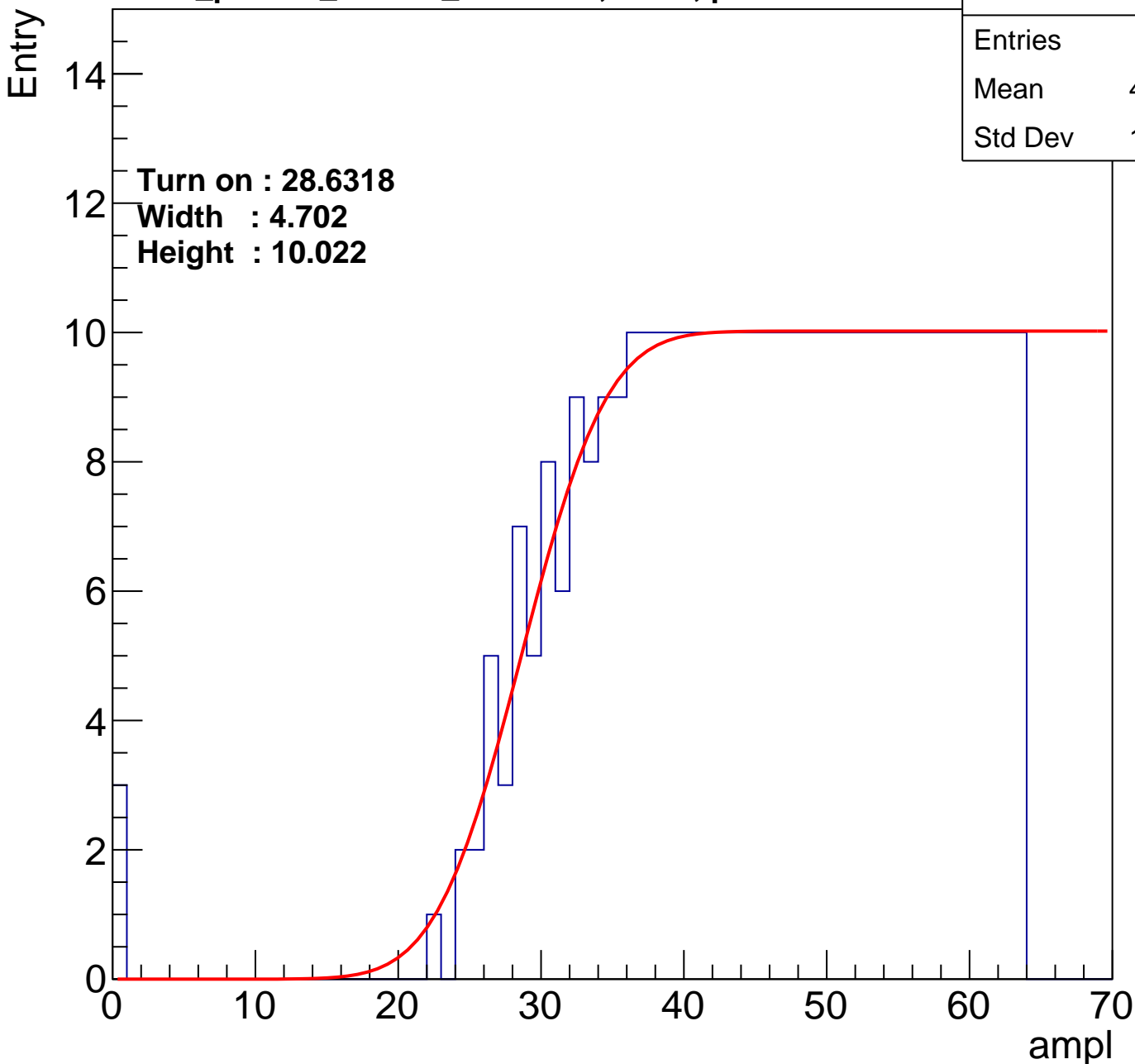


calib_packv5_042523_0143.root, FC#0, port D2

calib_packv5_042523_0143.root, FC#0, port D2

Entries	357
Mean	45.18
Std Dev	11.34

Height : 10.022



B1L101S, U15-ch11

calib_packv5_042523_0143.root, FC#0, port D2

Entries	358
Mean	45.15
Std Dev	11.44

Turn on : 28.8658

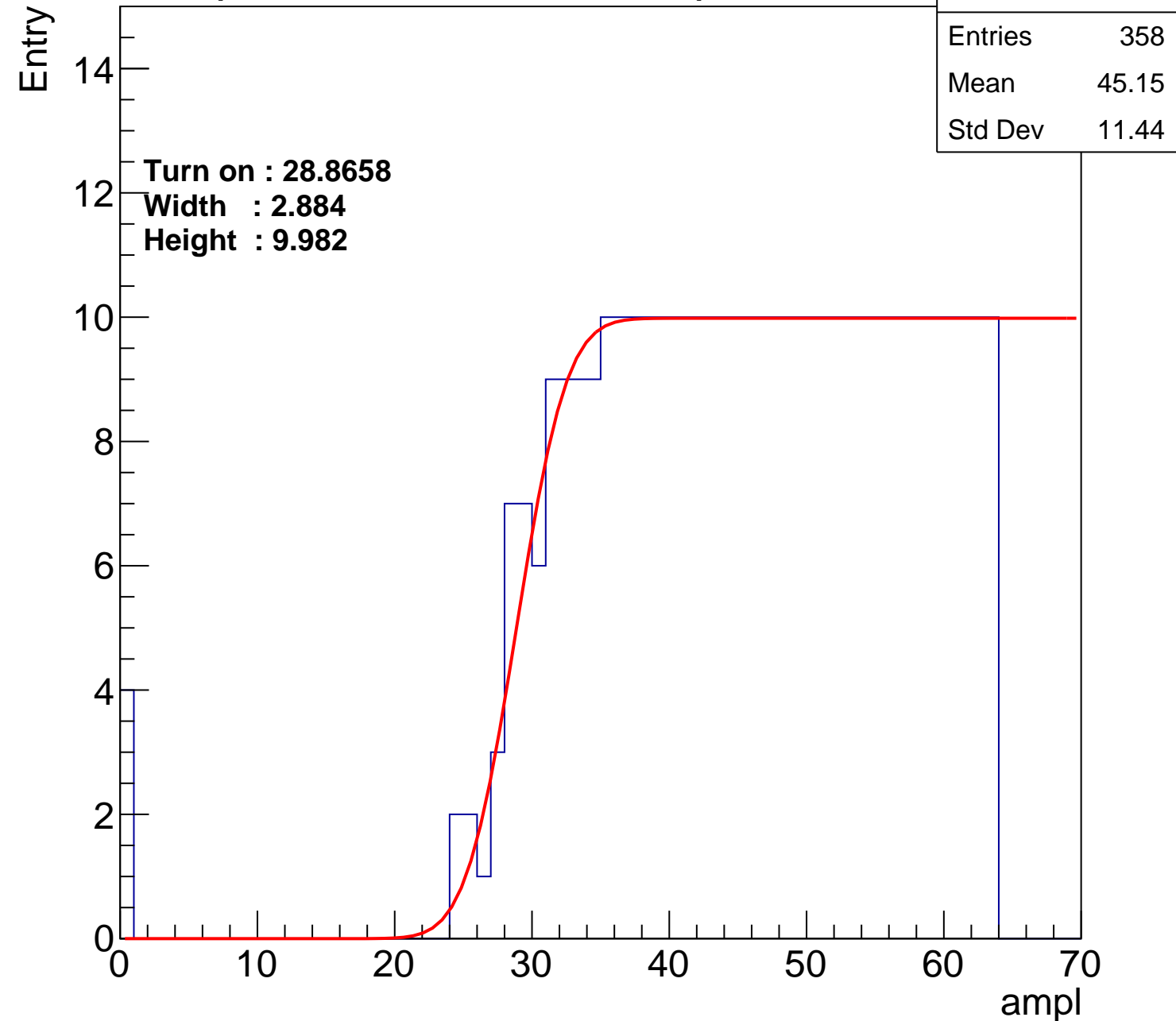
Width : 2.884

Height : 9.982

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch12

calib_packv5_042523_0143.root, FC#0, port D2

Entries	376
Mean	44.43
Std Dev	11.55

Turn on : 26.8024

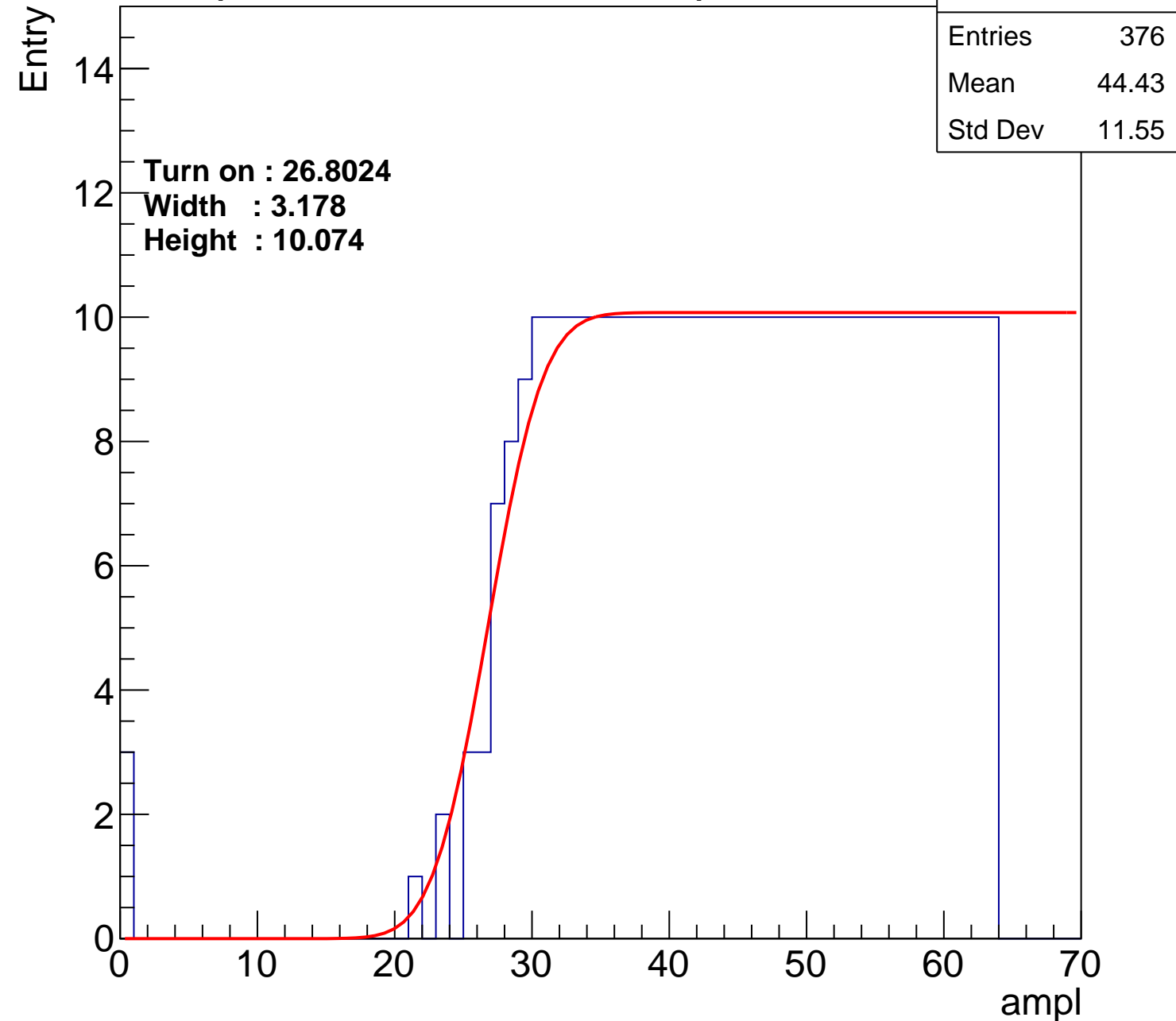
Width : 3.178

Height : 10.074

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch13

calib_packv5_042523_0143.root, FC#0, port D2

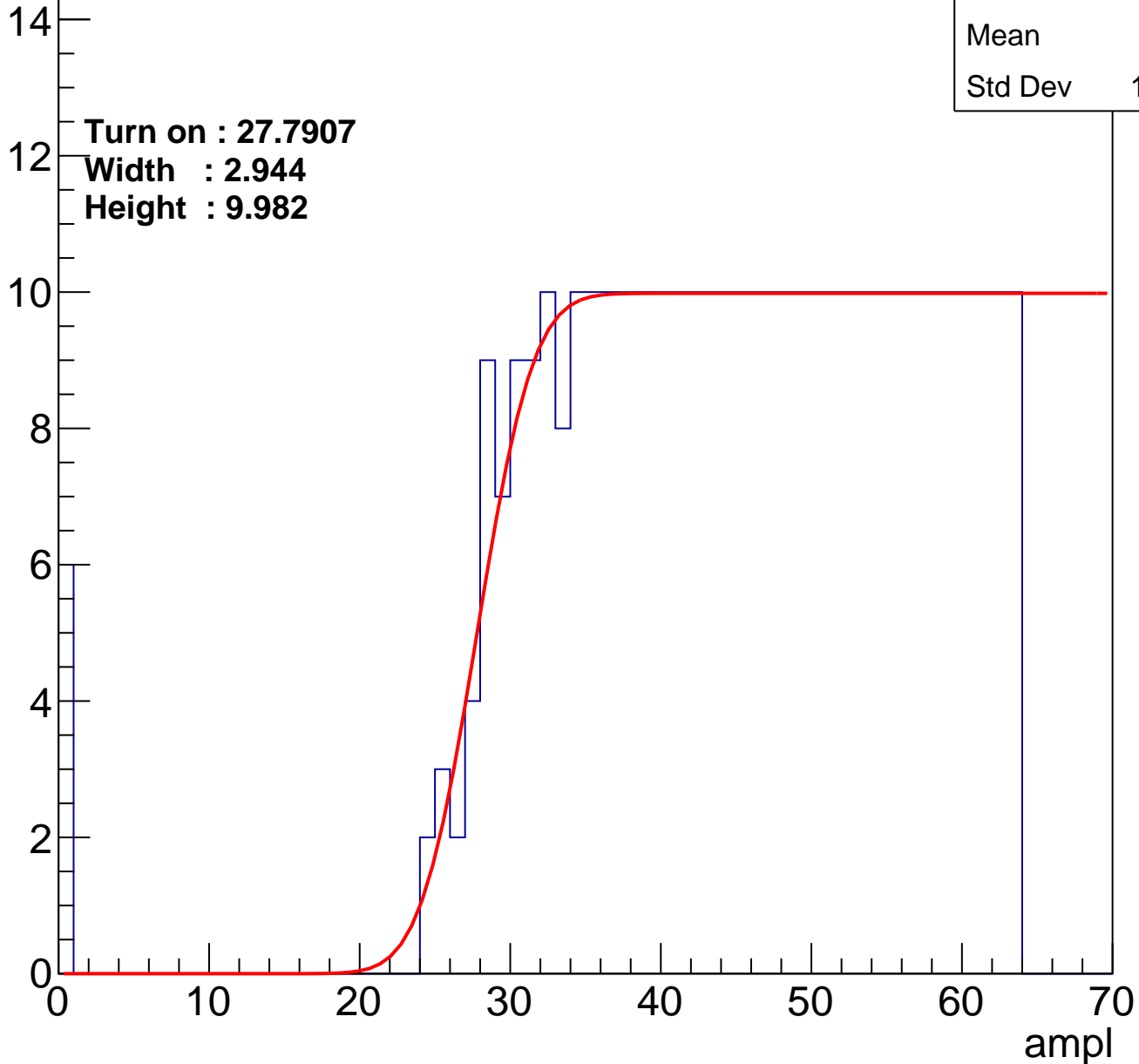
Entries	369
Mean	44.5
Std Dev	12.02

Turn on : 27.7907

Width : 2.944

Height : 9.982

Entry



B1L101S, U15-ch14

calib_packv5_042523_0143.root, FC#0, port D2

Entries	381
Mean	43.88
Std Dev	12.4

Turn on : 26.6707

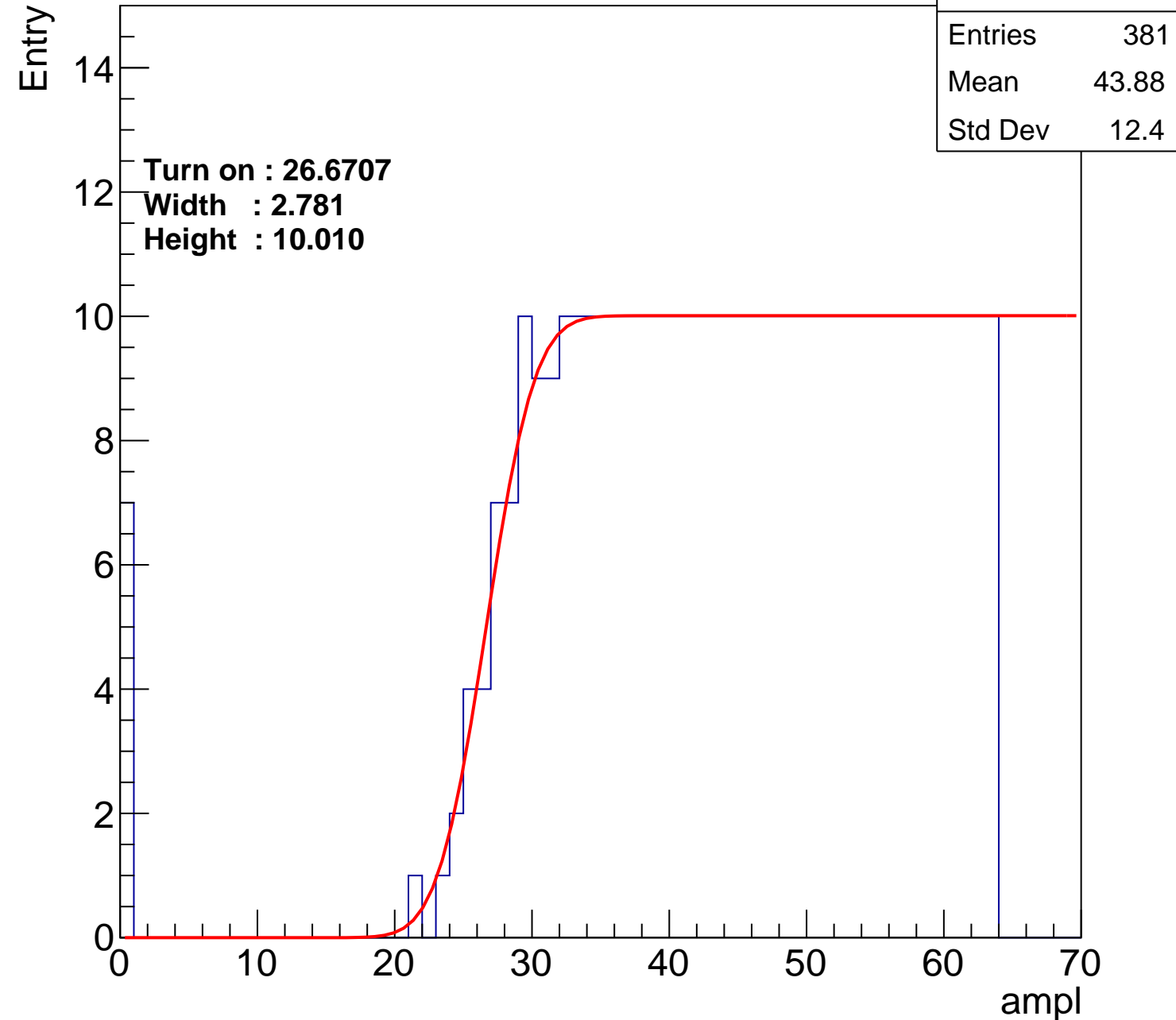
Width : 2.781

Height : 10.010

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch15

calib_packv5_042523_0143.root, FC#0, port D2

Entries	369
Mean	44.77
Std Dev	11.28

Turn on : 27.6357

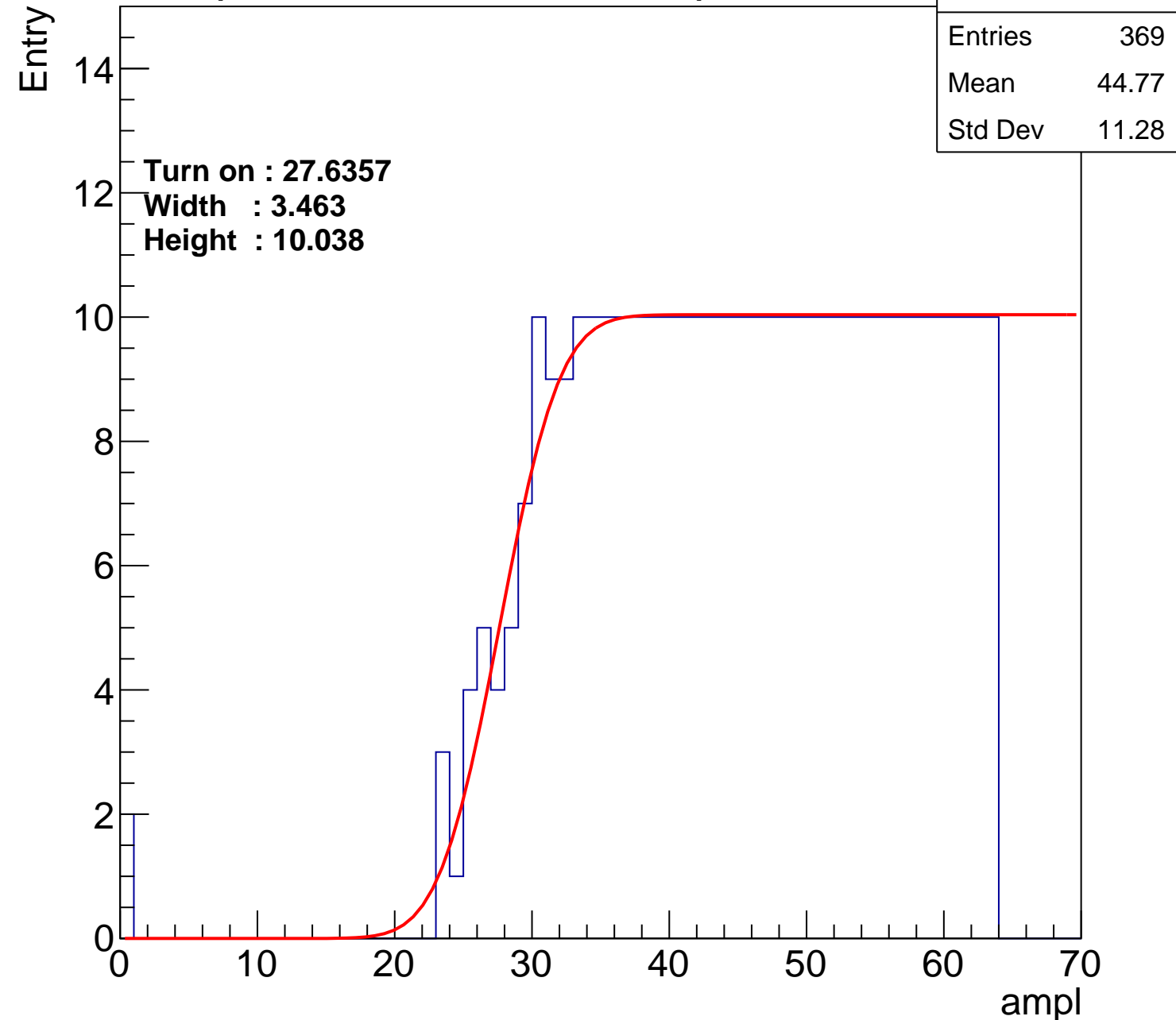
Width : 3.463

Height : 10.038

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch16

calib_packv5_042523_0143.root, FC#0, port D2

Entries	398
Mean	43.24
Std Dev	12.32

Turn on : 24.6385

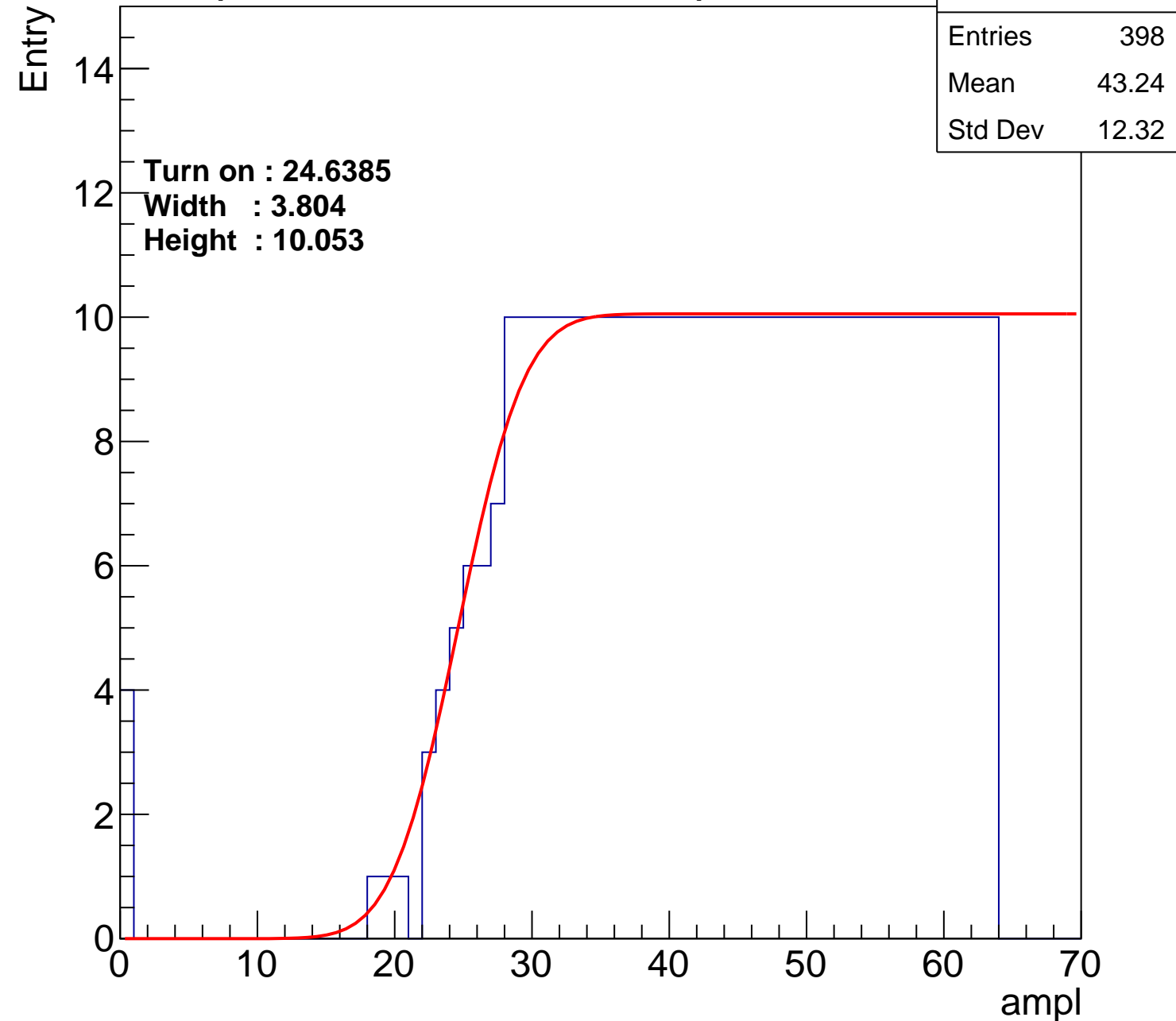
Width : 3.804

Height : 10.053

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch17

calib_packv5_042523_0143.root, FC#0, port D2

Entries	383
Mean	44.01
Std Dev	11.83

Turn on : 27.0253

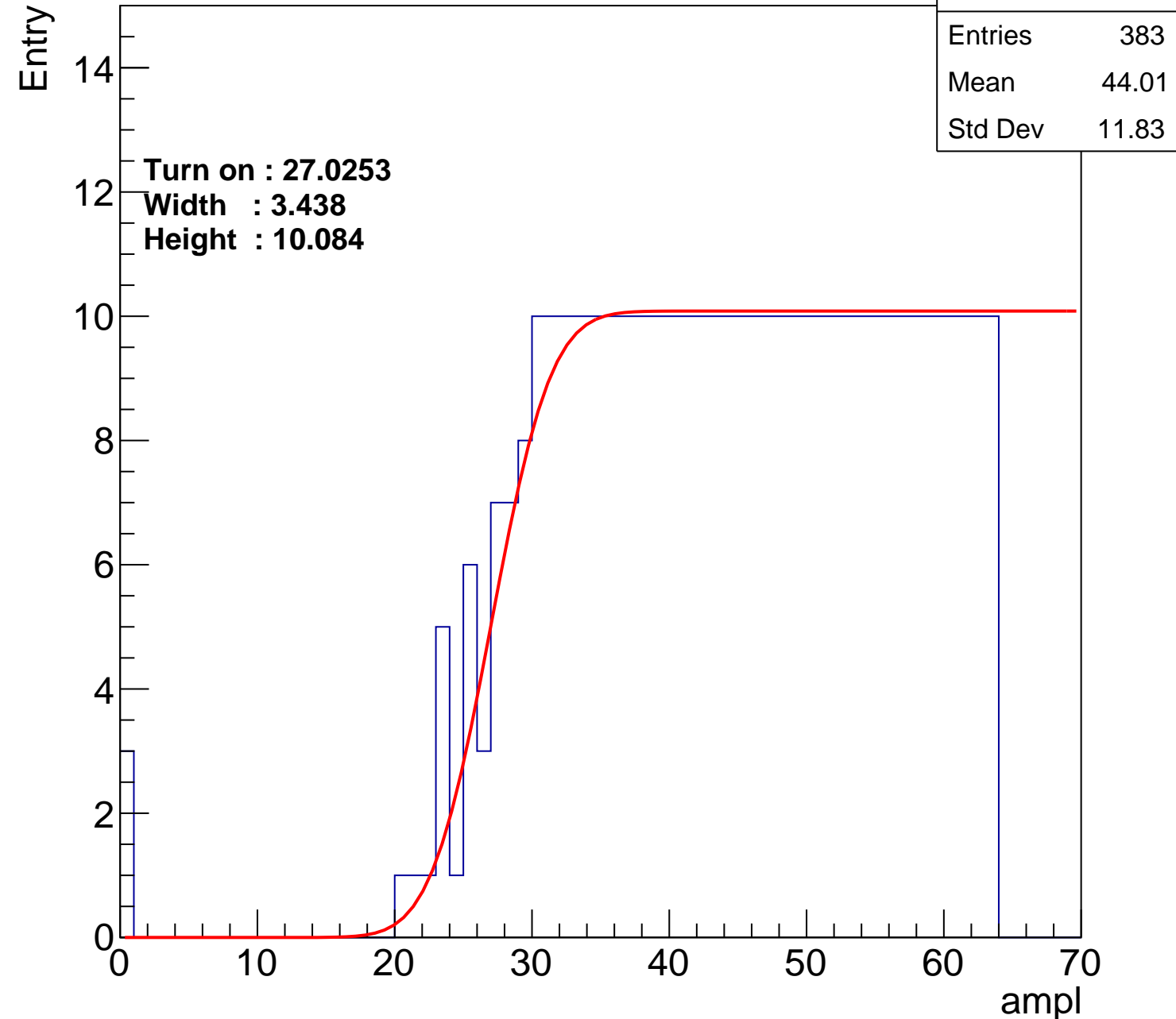
Width : 3.438

Height : 10.084

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch18

calib_packv5_042523_0143.root, FC#0, port D2

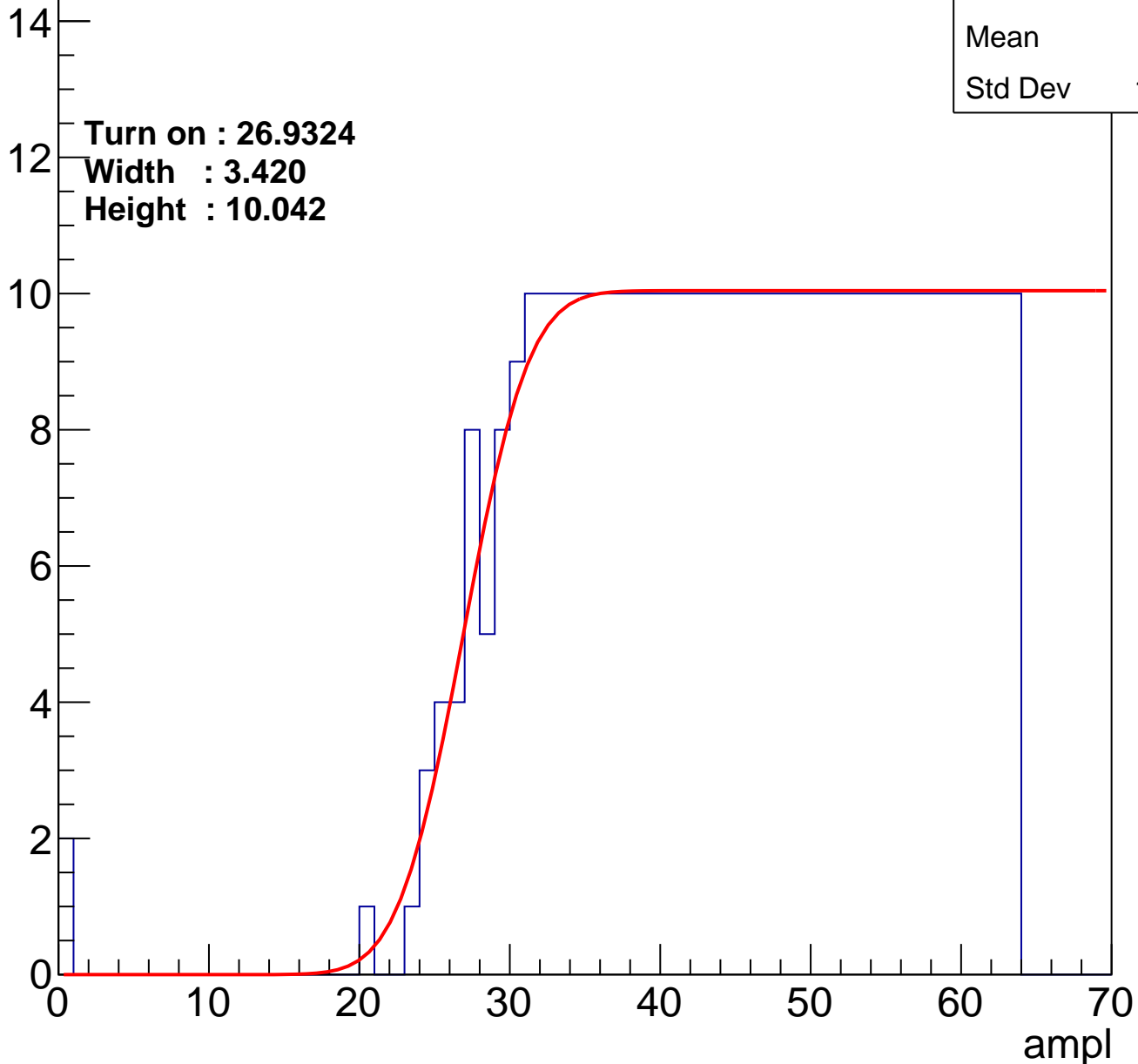
Entries	375
Mean	44.5
Std Dev	11.41

Turn on : 26.9324

Width : 3.420

Height : 10.042

Entry



B1L101S, U15-ch19

calib_packv5_042523_0143.root, FC#0, port D2

Entries	361
Mean	45.12
Std Dev	11.24

Turn on : 28.4504

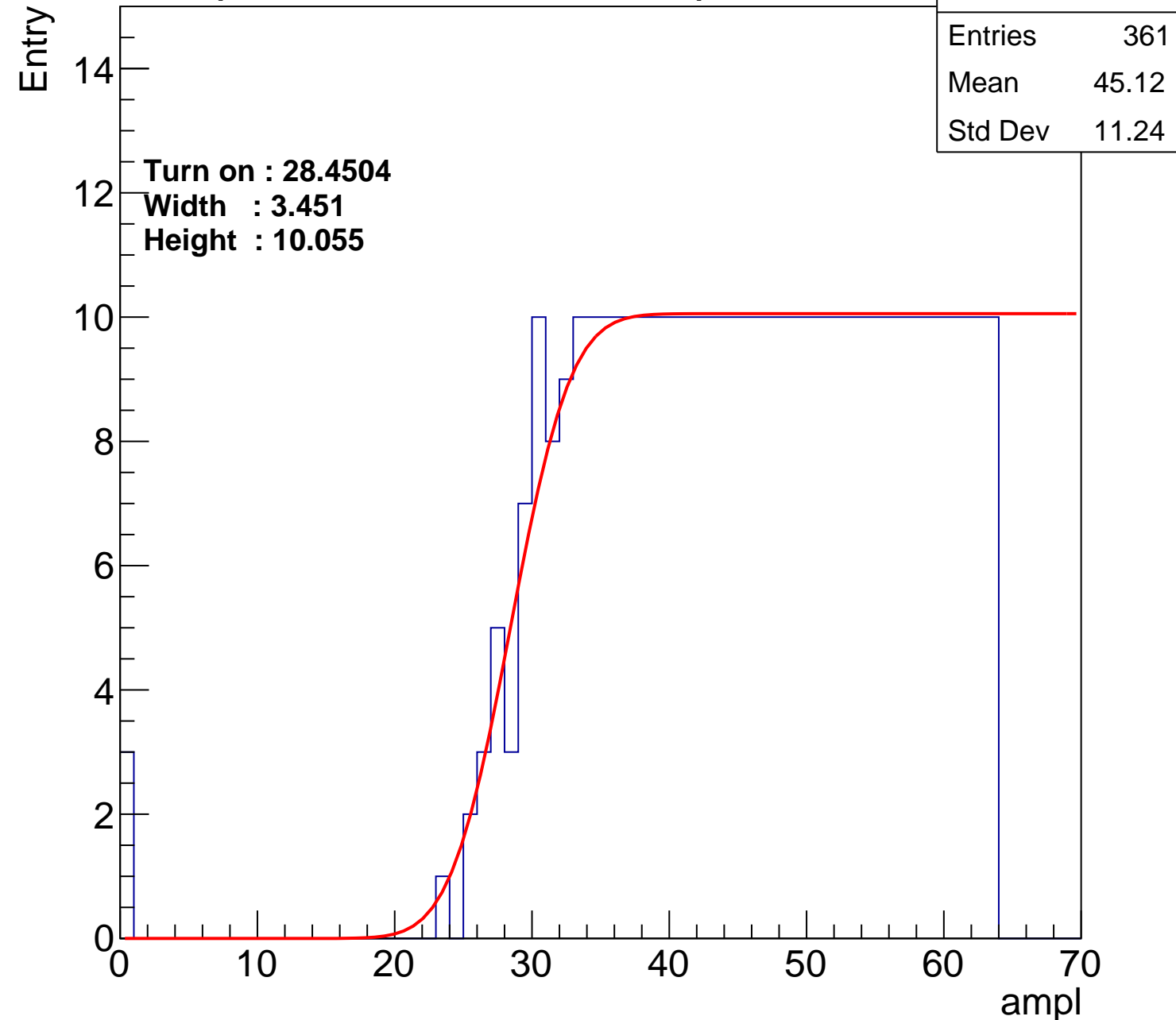
Width : 3.451

Height : 10.055

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch20

calib_packv5_042523_0143.root, FC#0, port D2

Entries	359
Mean	45.13
Std Dev	11.43

Turn on : 28.6966

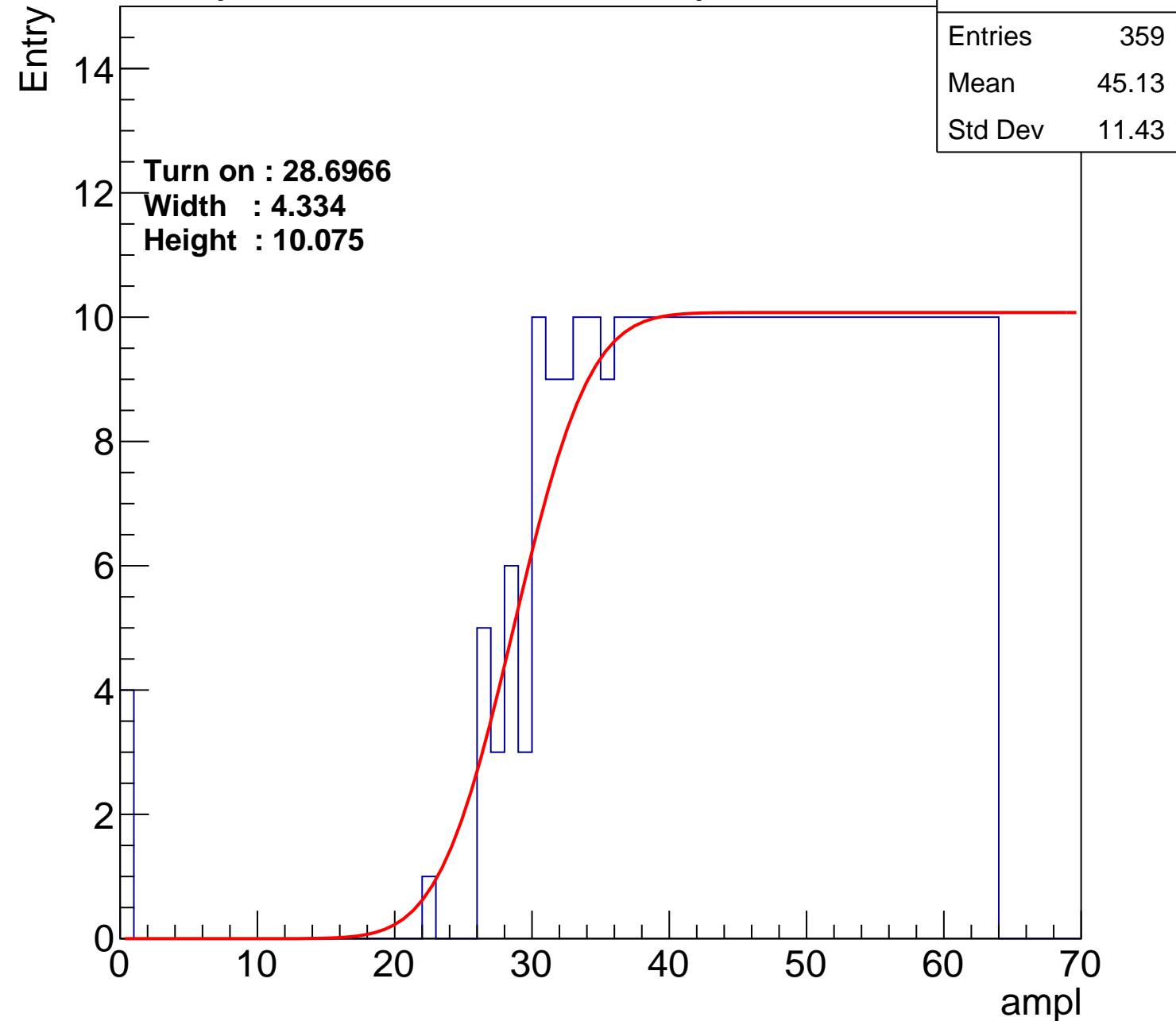
Width : 4.334

Height : 10.075

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch21

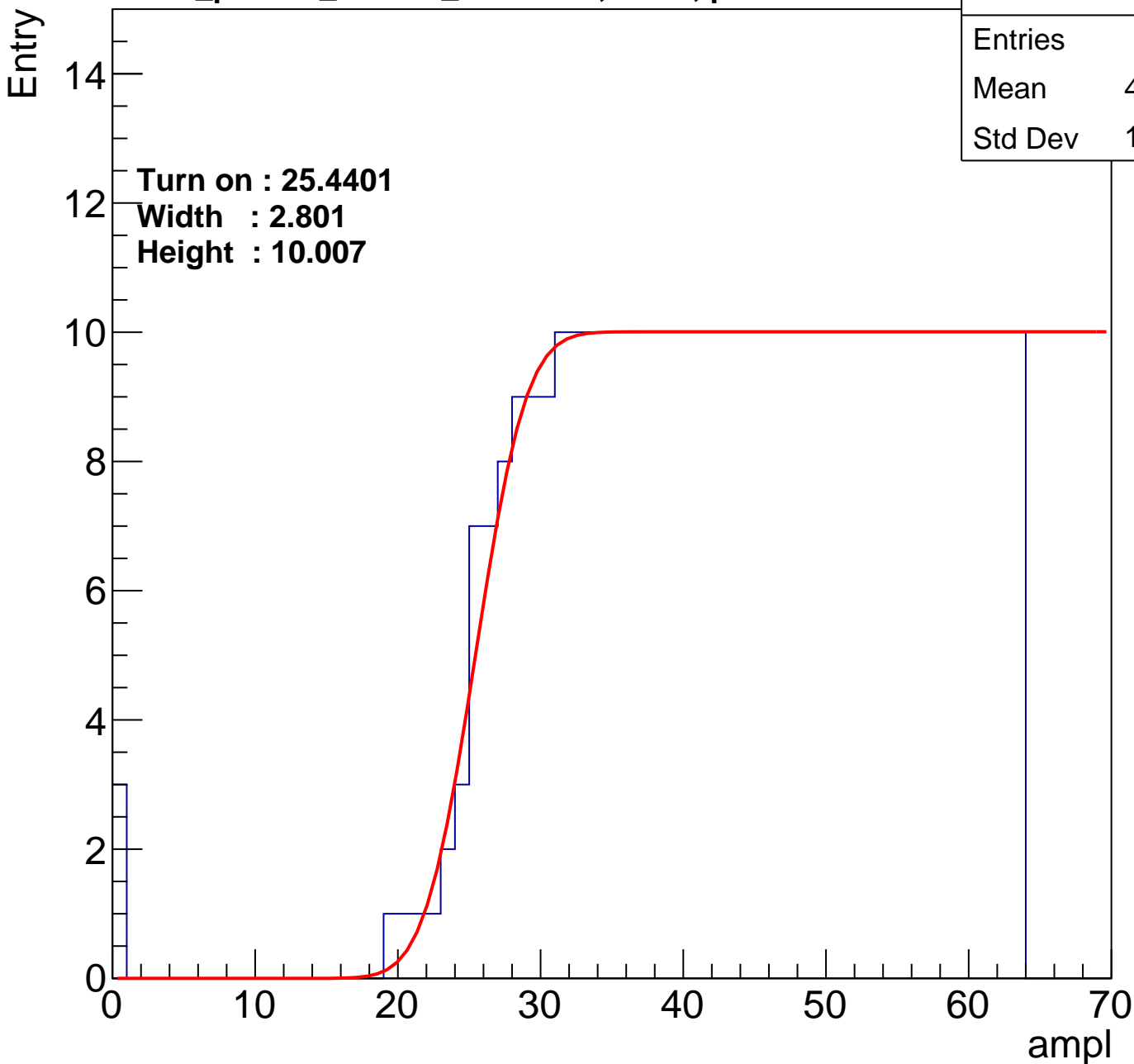
calib_packv5_042523_0143.root, FC#0, port D2

Entries	391
Mean	43.65
Std Dev	11.98

Turn on : 25.4401

Width : 2.801

Height : 10.007



B1L101S, U15-ch22

calib_packv5_042523_0143.root, FC#0, port D2

Entries	363
Mean	45.07
Std Dev	11.14

Turn on : 29.1894

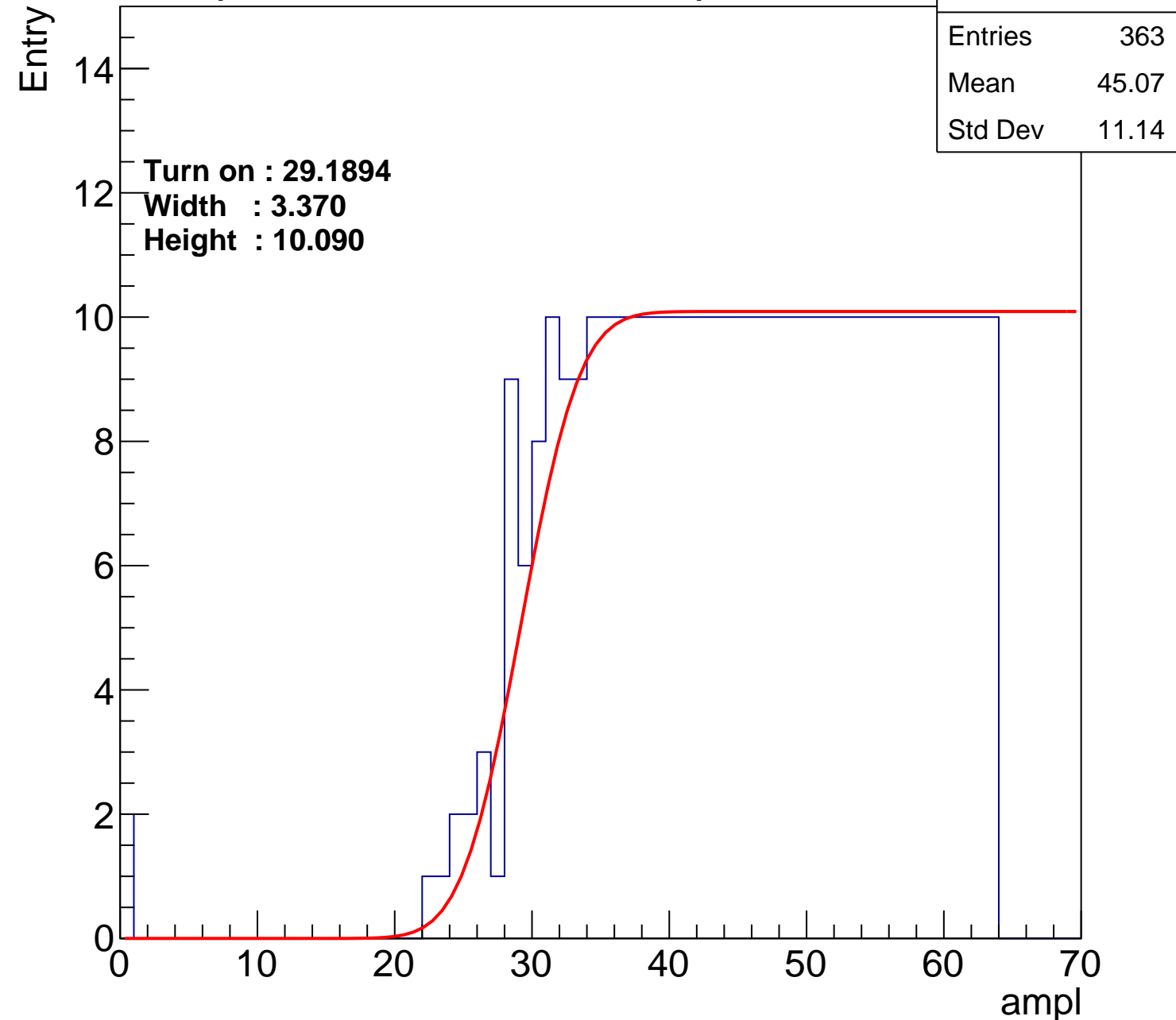
Width : 3.370

Height : 10.090

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch23

calib_packv5_042523_0143.root, FC#0, port D2

Entries	375
Mean	44.54
Std Dev	11.33

Turn on : 26.7415

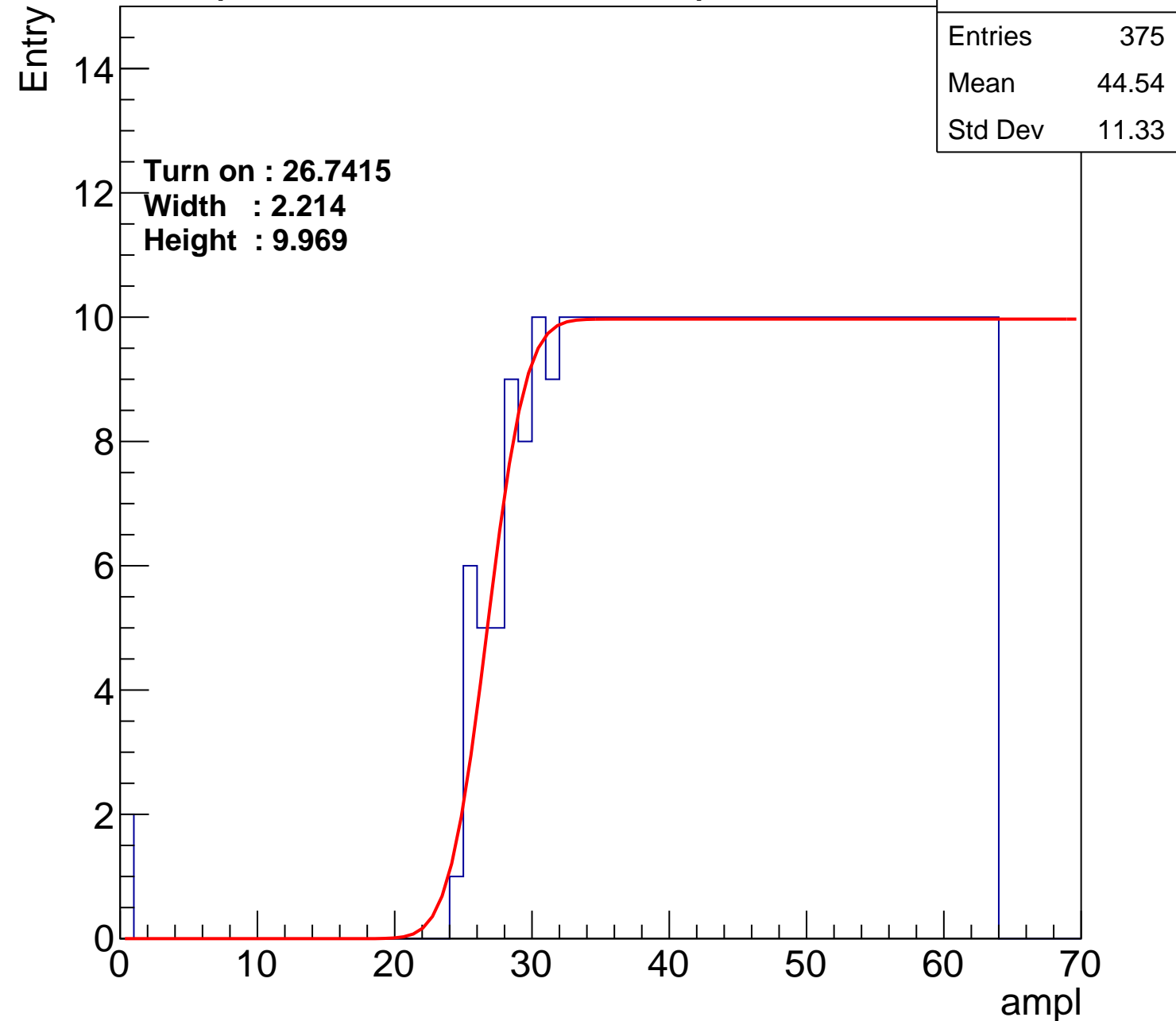
Width : 2.214

Height : 9.969

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch24

calib_packv5_042523_0143.root, FC#0, port D2

Entries	376
Mean	44.36
Std Dev	11.65

Turn on : 27.0598

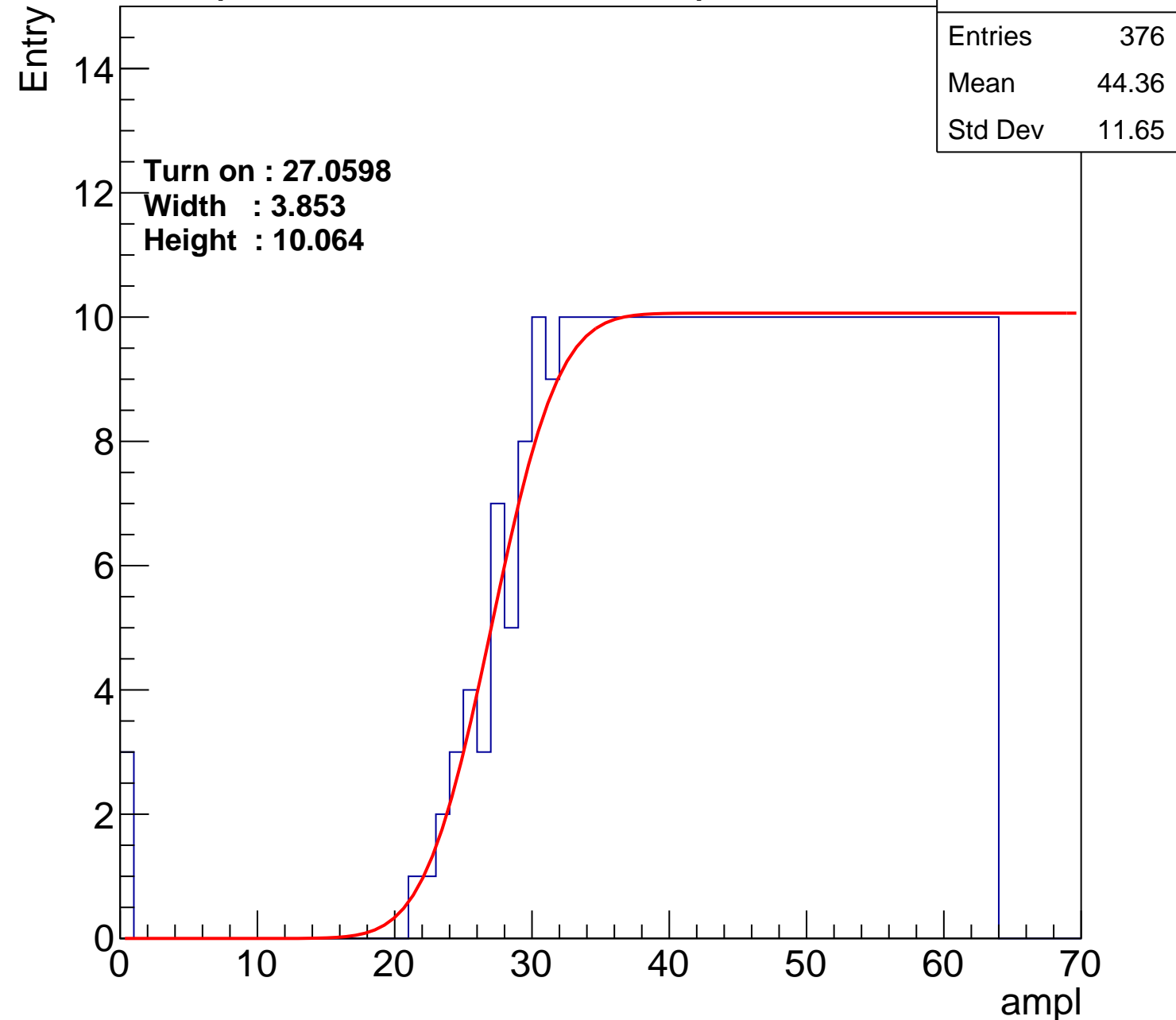
Width : 3.853

Height : 10.064

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch25

calib_packv5_042523_0143.root, FC#0, port D2

Entries	391
Mean	43.54
Std Dev	12.28

Turn on : 26.0200

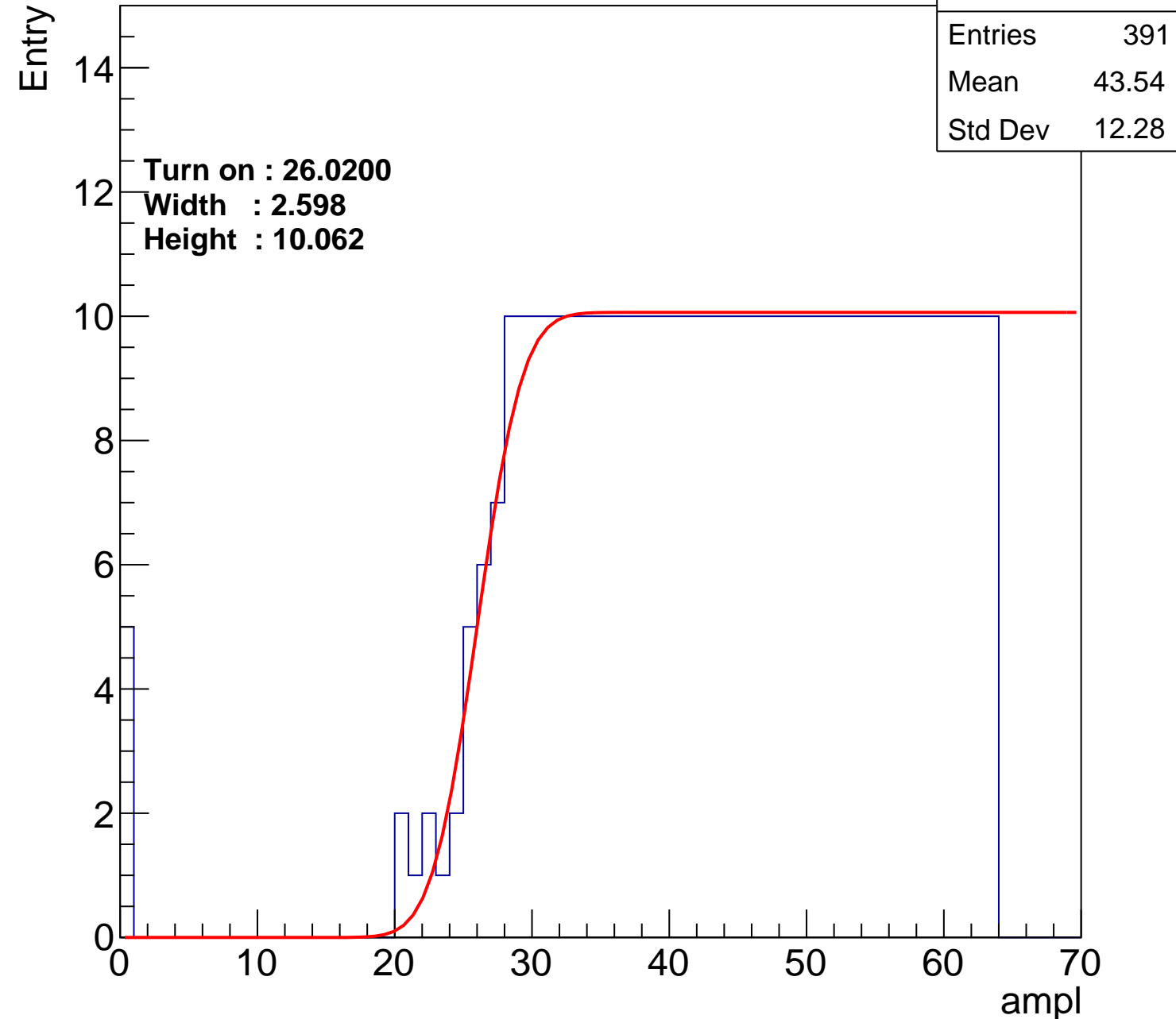
Width : 2.598

Height : 10.062

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch26

calib_packv5_042523_0143.root, FC#0, port D2

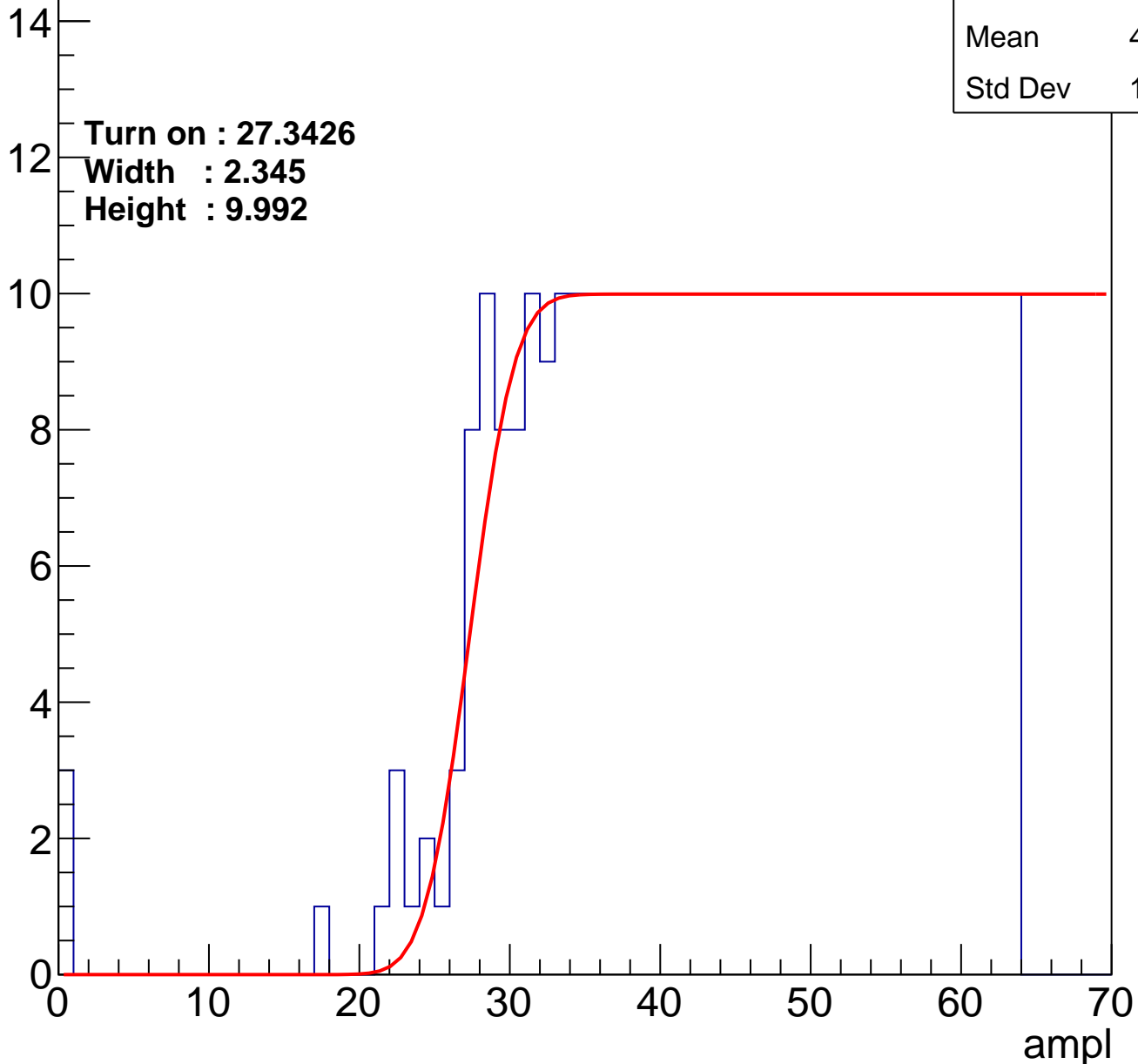
Entries	378
Mean	44.24
Std Dev	11.74

Turn on : 27.3426

Width : 2.345

Height : 9.992

Entry



B1L101S, U15-ch27

calib_packv5_042523_0143.root, FC#0, port D2

Entries	370
Mean	44.77
Std Dev	11.15

Turn on : 27.5770

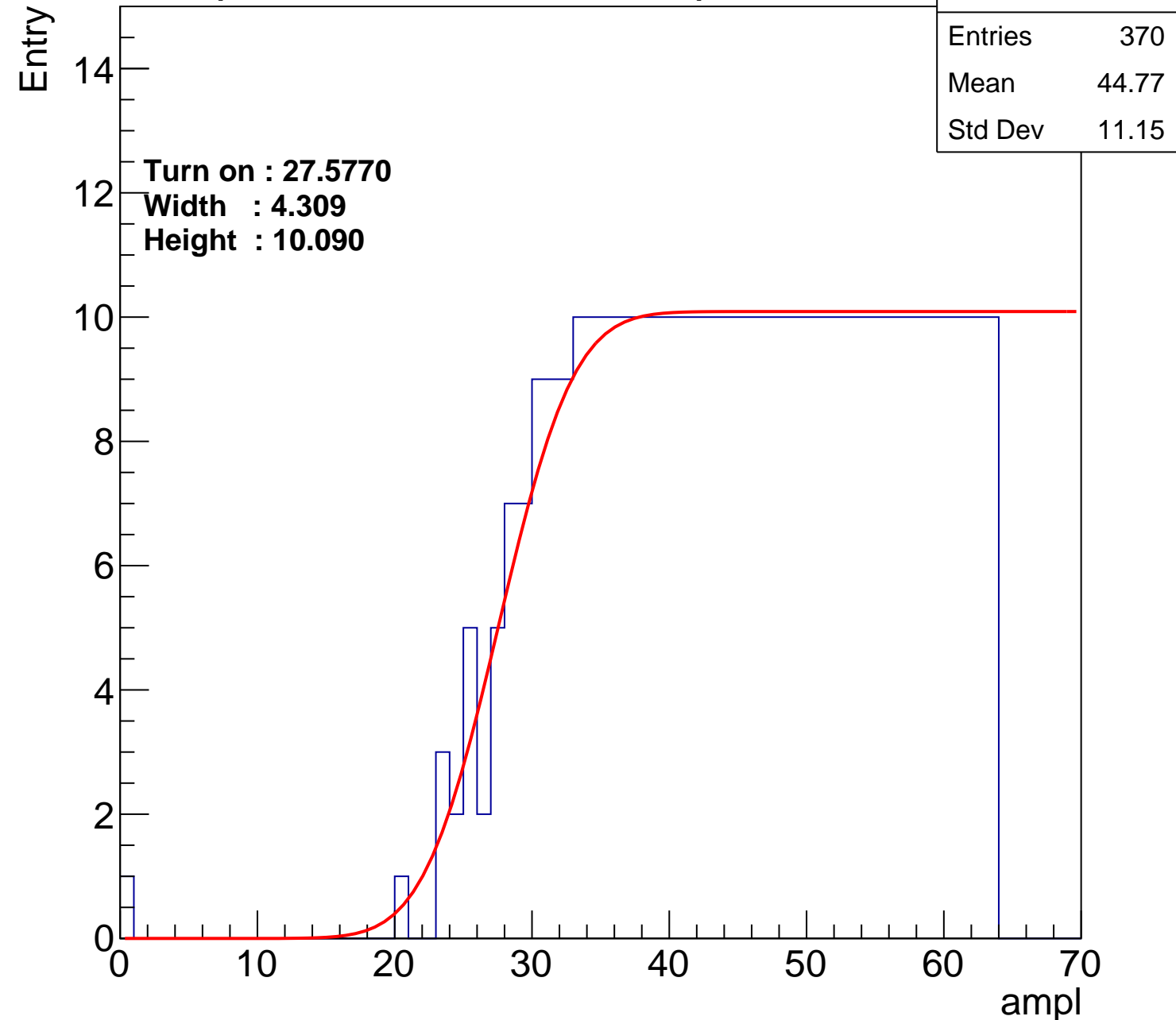
Width : 4.309

Height : 10.090

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch28

calib_packv5_042523_0143.root, FC#0, port D2

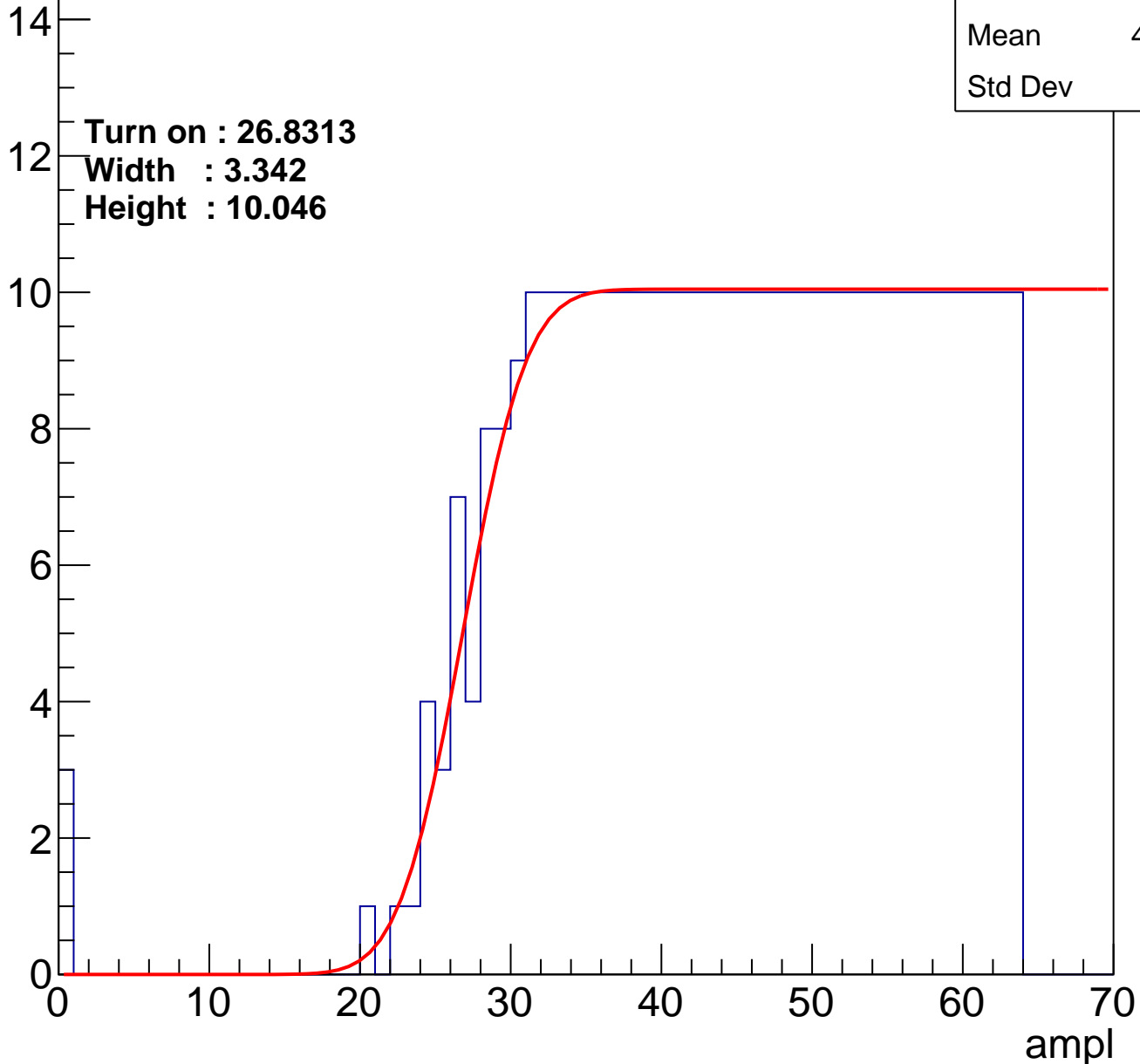
Entries	379
Mean	44.23
Std Dev	11.7

Turn on : 26.8313

Width : 3.342

Height : 10.046

Entry



B1L101S, U15-ch29

calib_packv5_042523_0143.root, FC#0, port D2

Entries	367
Mean	44.75
Std Dev	11.6

Turn on : 27.9380

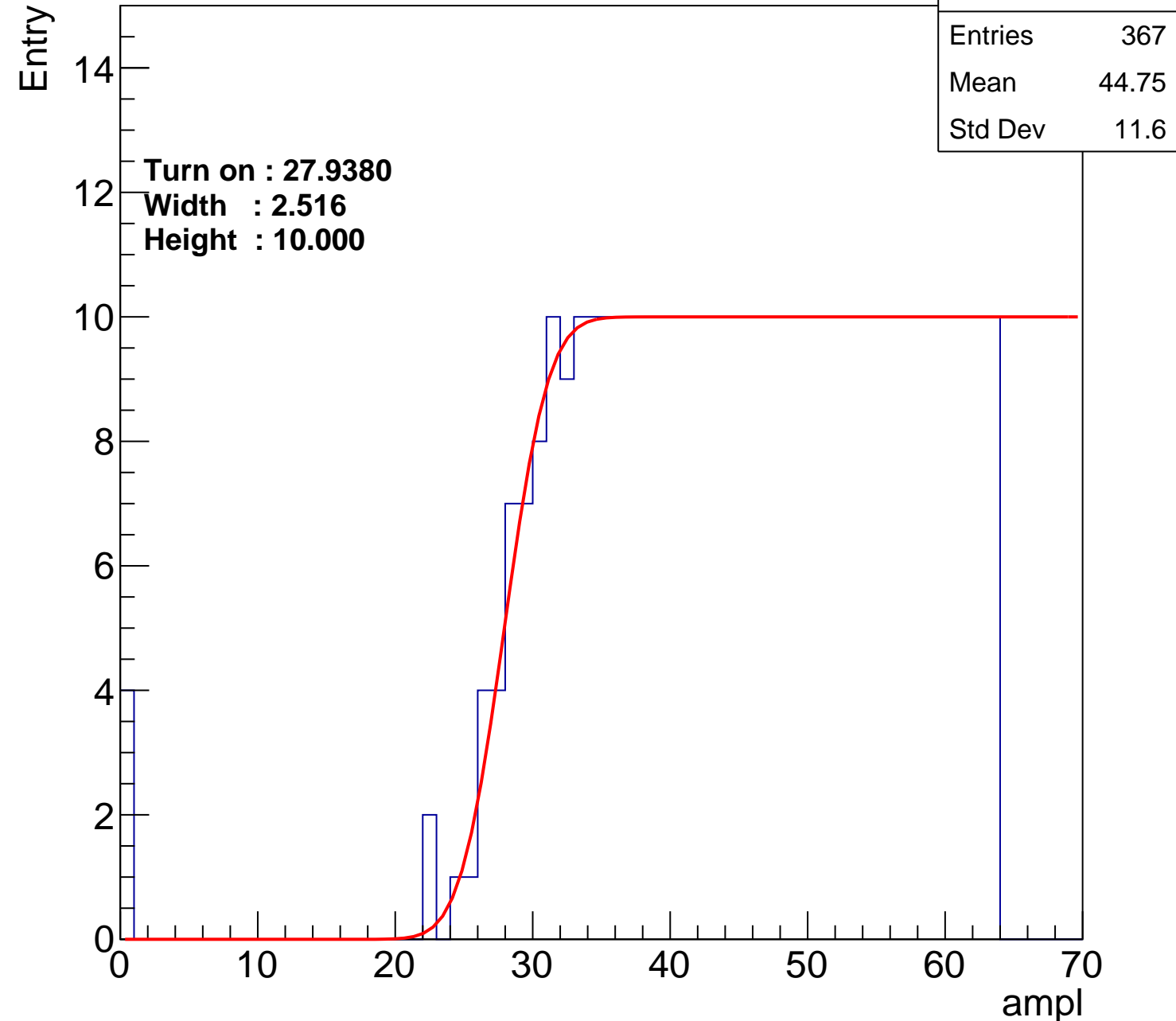
Width : 2.516

Height : 10.000

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch30

calib_packv5_042523_0143.root, FC#0, port D2

Entries	381
Mean	44.12
Std Dev	11.84

Turn on : 26.6749

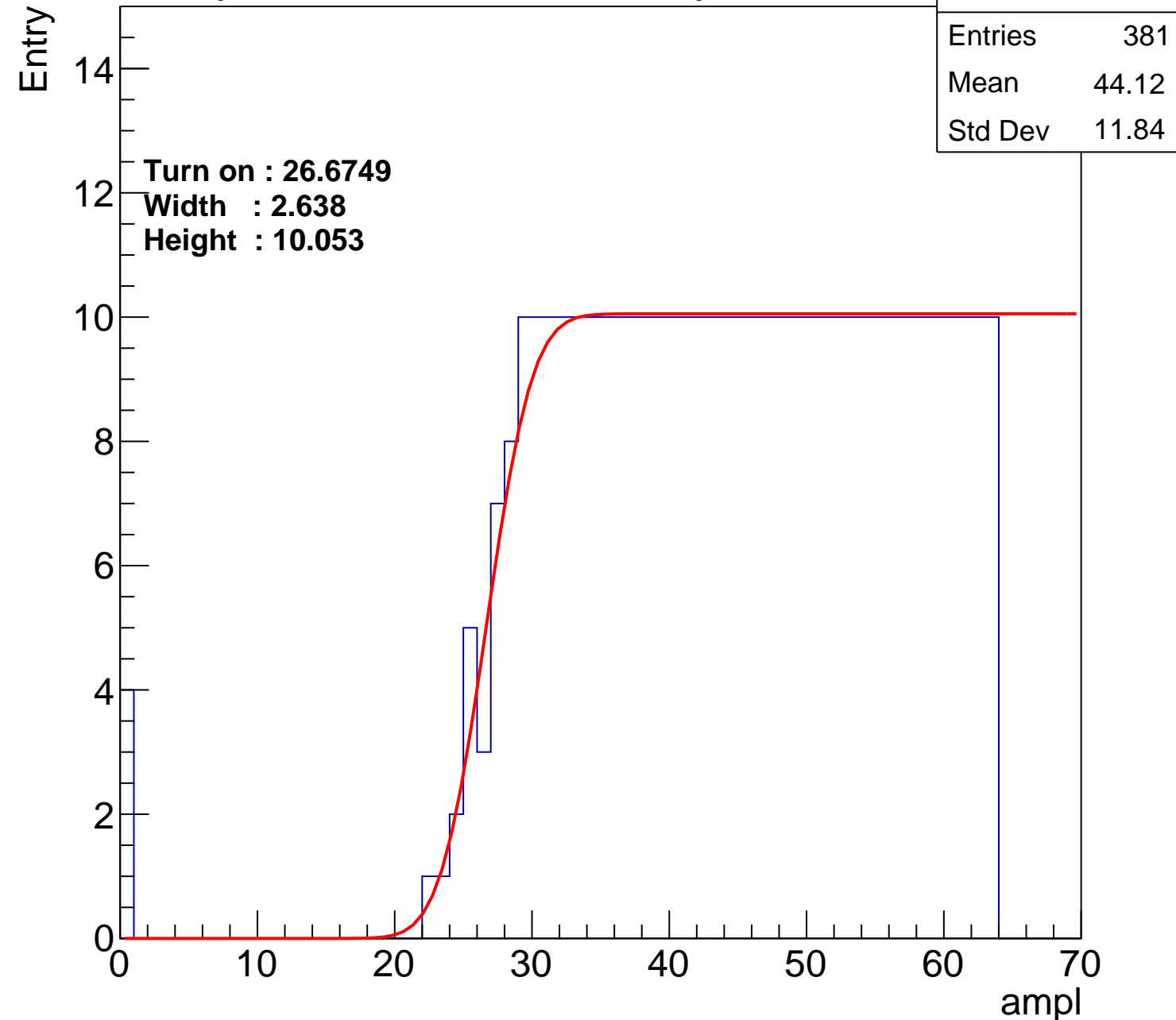
Width : 2.638

Height : 10.053

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch31

calib_packv5_042523_0143.root, FC#0, port D2

Entries	364
Mean	45.1
Std Dev	10.92

Turn on : 27.8942

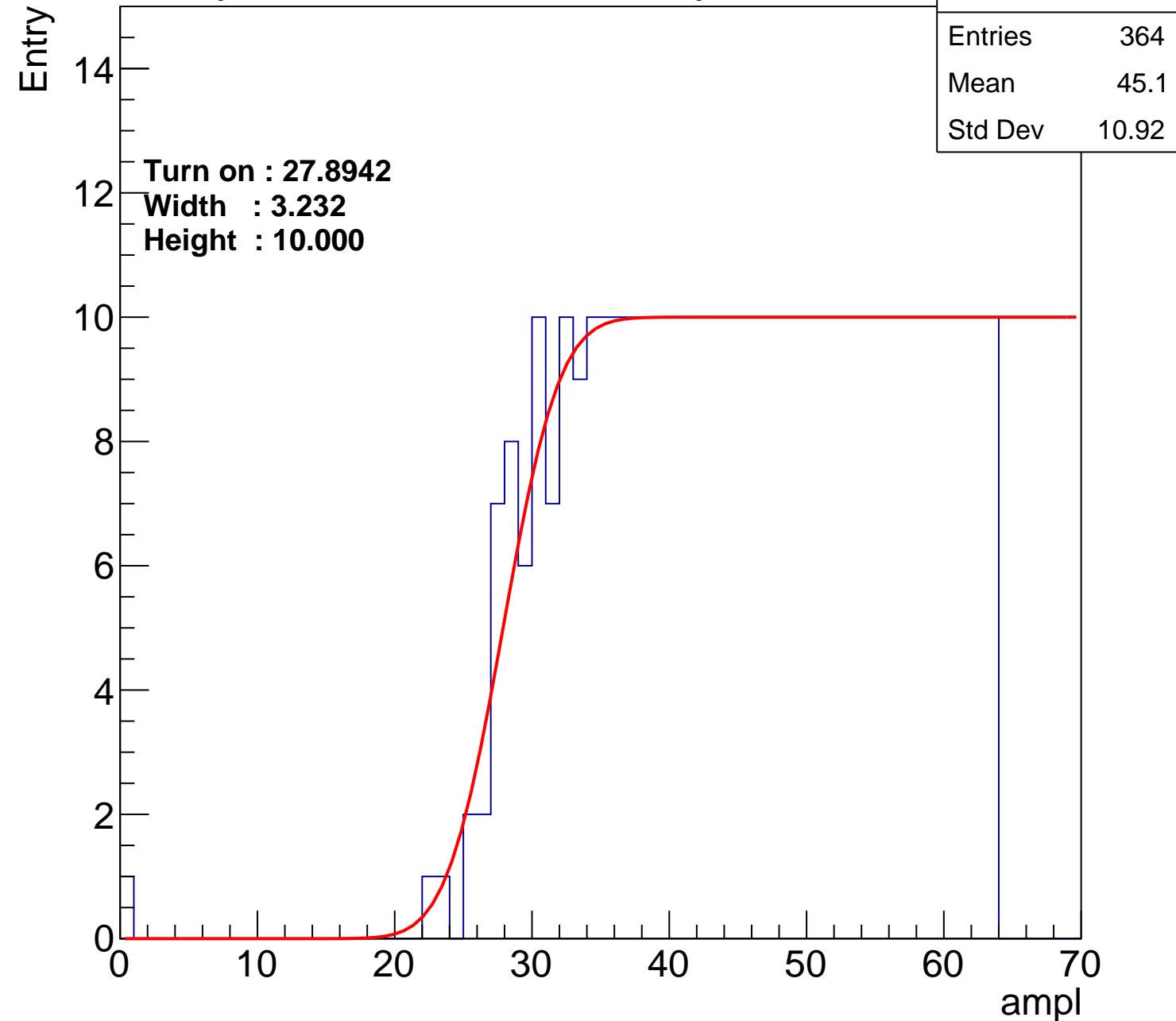
Width : 3.232

Height : 10.000

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch32

calib_packv5_042523_0143.root, FC#0, port D2

Entries	381
Mean	44.13
Std Dev	11.75

Turn on : 26.8732

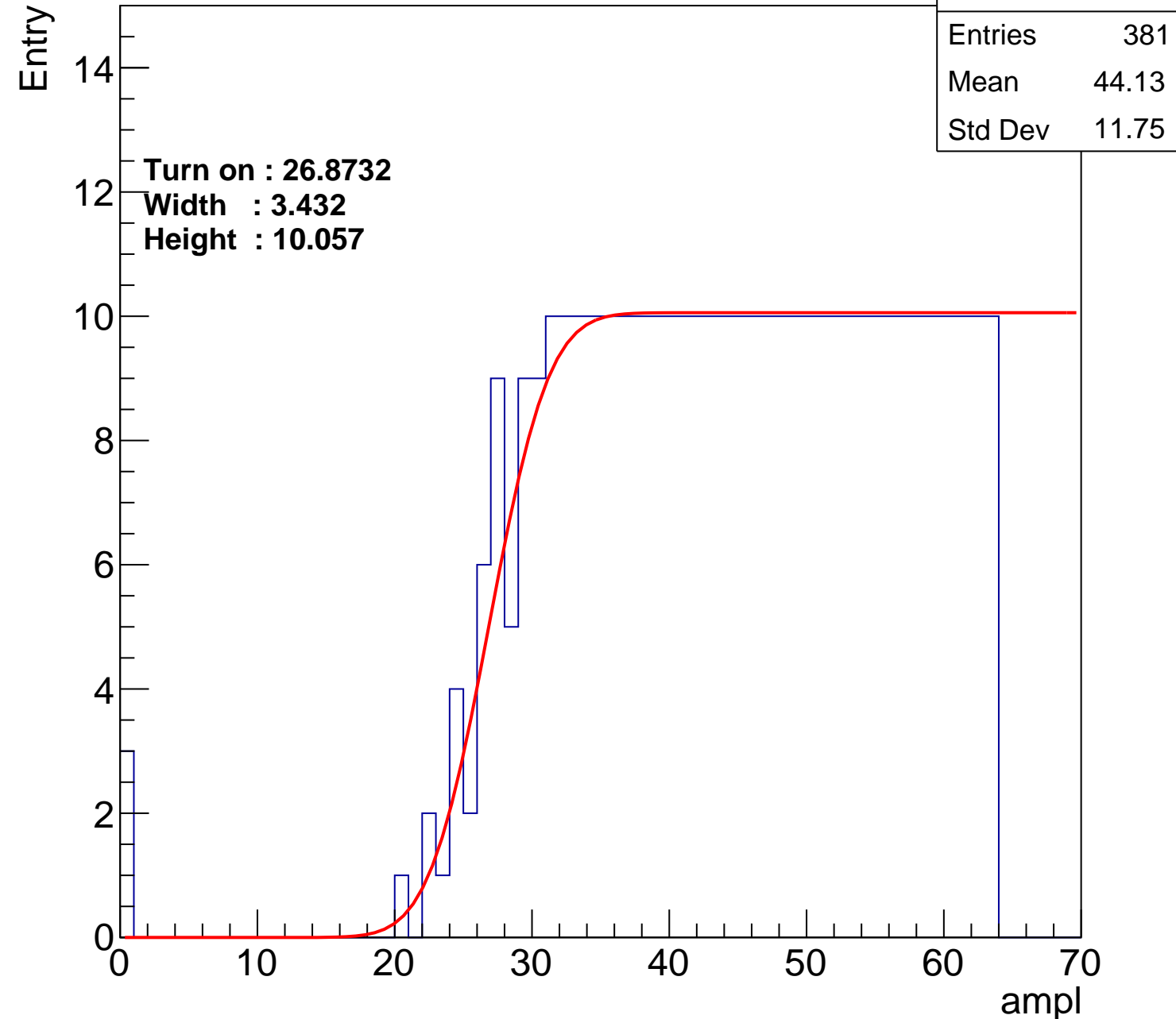
Width : 3.432

Height : 10.057

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch33

calib_packv5_042523_0143.root, FC#0, port D2

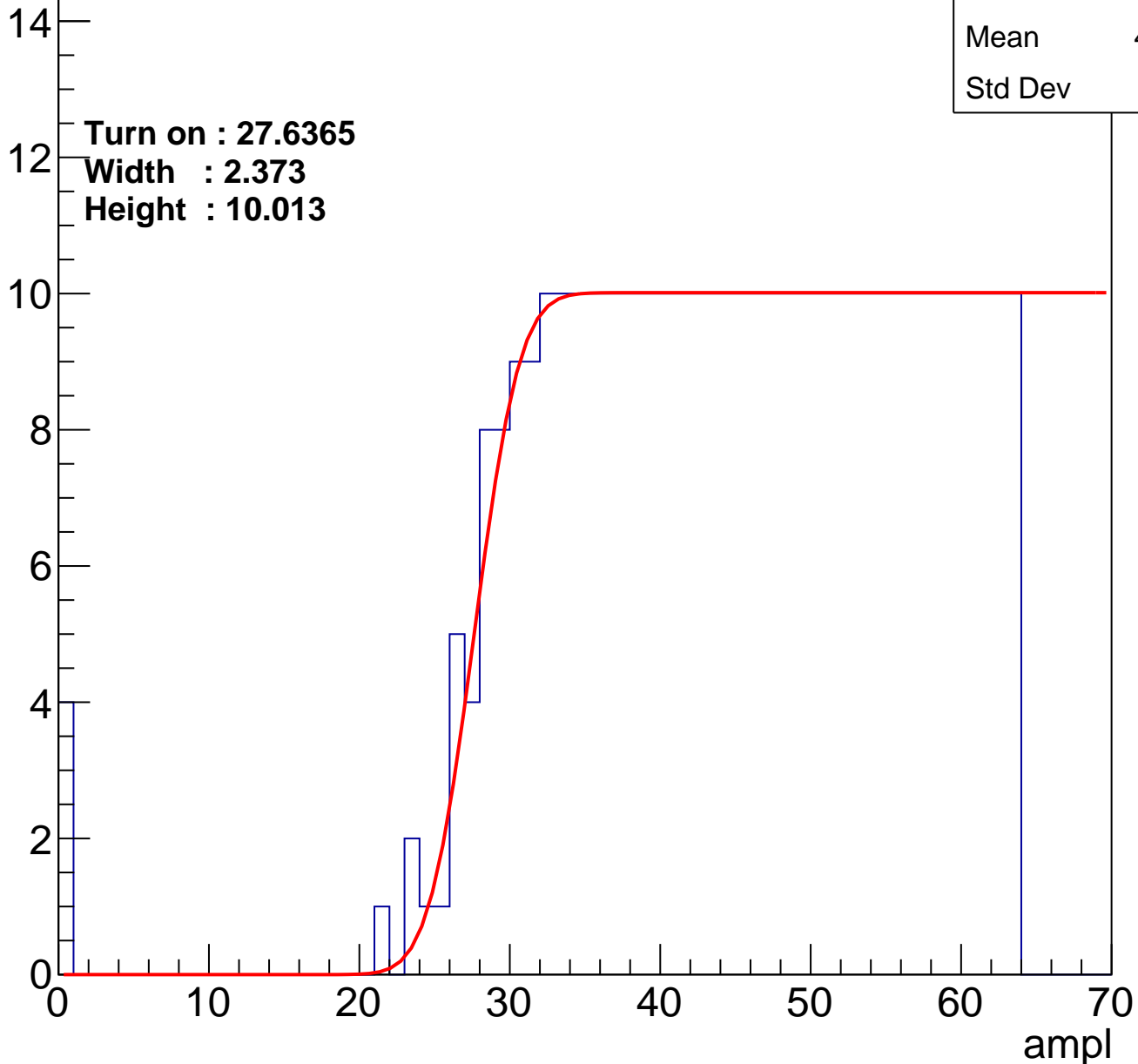
Entries	372
Mean	44.51
Std Dev	11.7

Turn on : 27.6365

Width : 2.373

Height : 10.013

Entry



B1L101S, U15-ch34

calib_packv5_042523_0143.root, FC#0, port D2

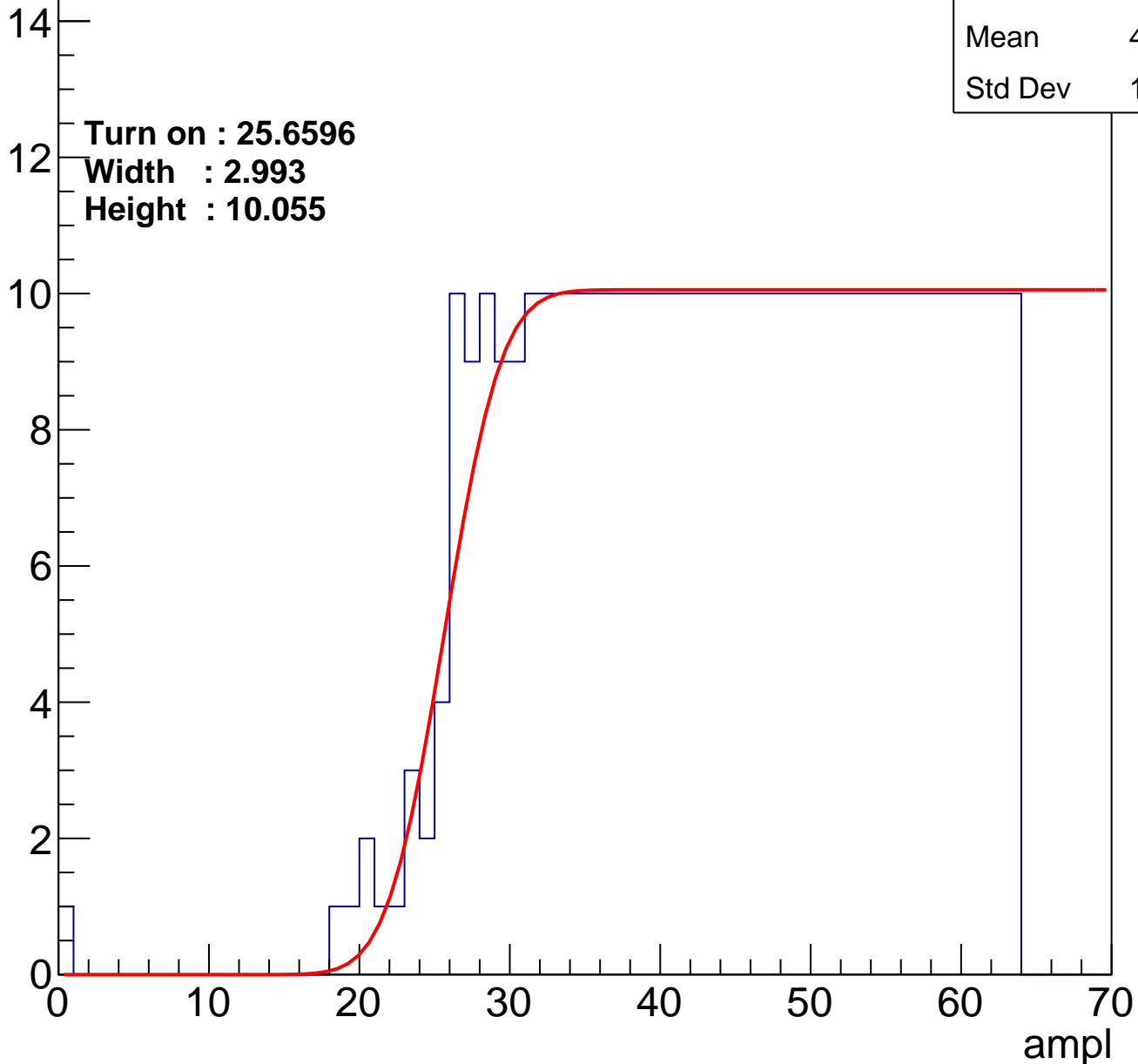
Entries	393
Mean	43.67
Std Dev	11.72

Turn on : 25.6596

Width : 2.993

Height : 10.055

Entry



B1L101S, U15-ch35

calib_packv5_042523_0143.root, FC#0, port D2

Entries	381
Mean	44.18
Std Dev	11.67

Turn on : 26.3713

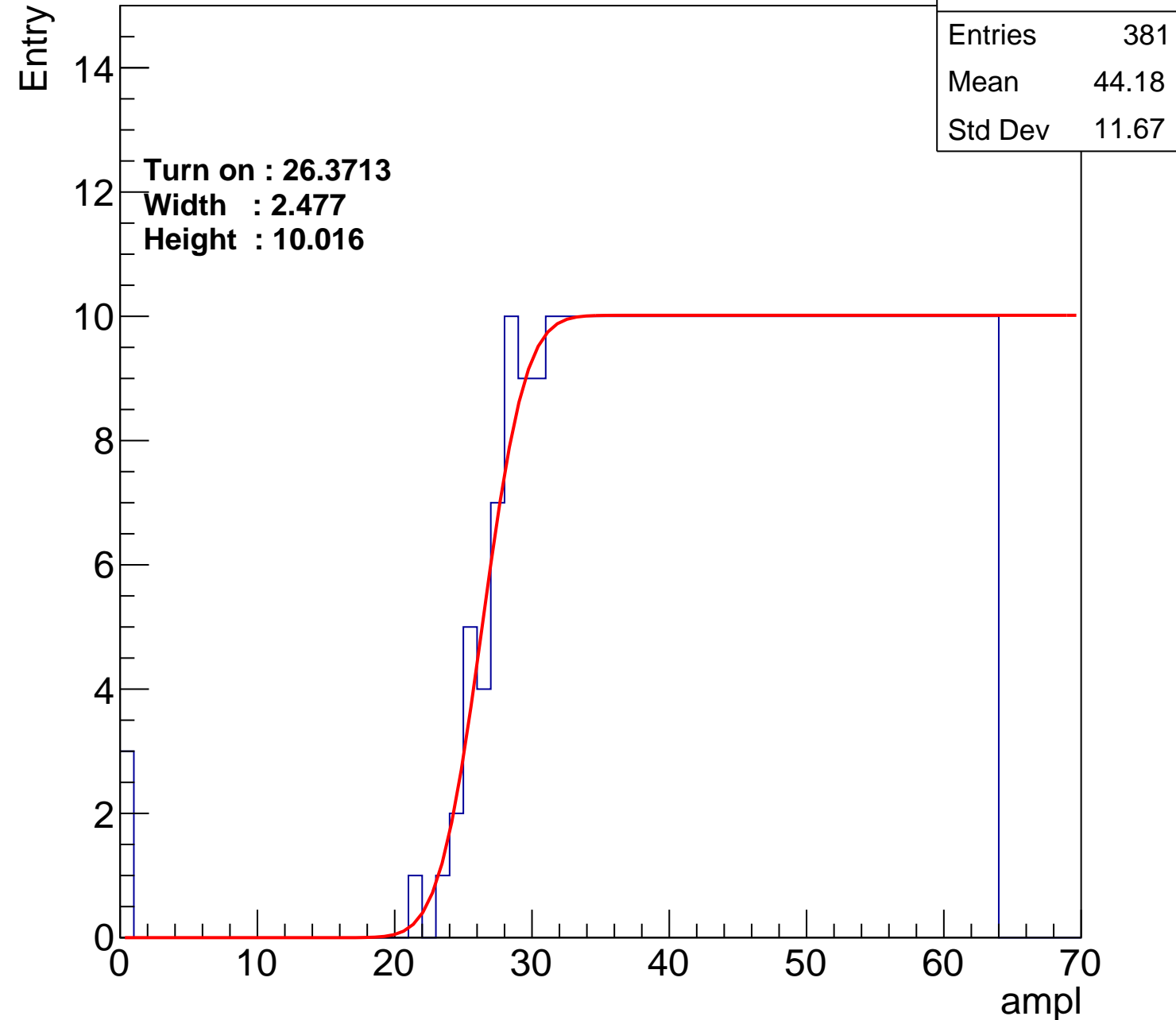
Width : 2.477

Height : 10.016

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch36

calib_packv5_042523_0143.root, FC#0, port D2

Entries	371
Mean	44.6
Std Dev	11.54

Turn on : 28.3018

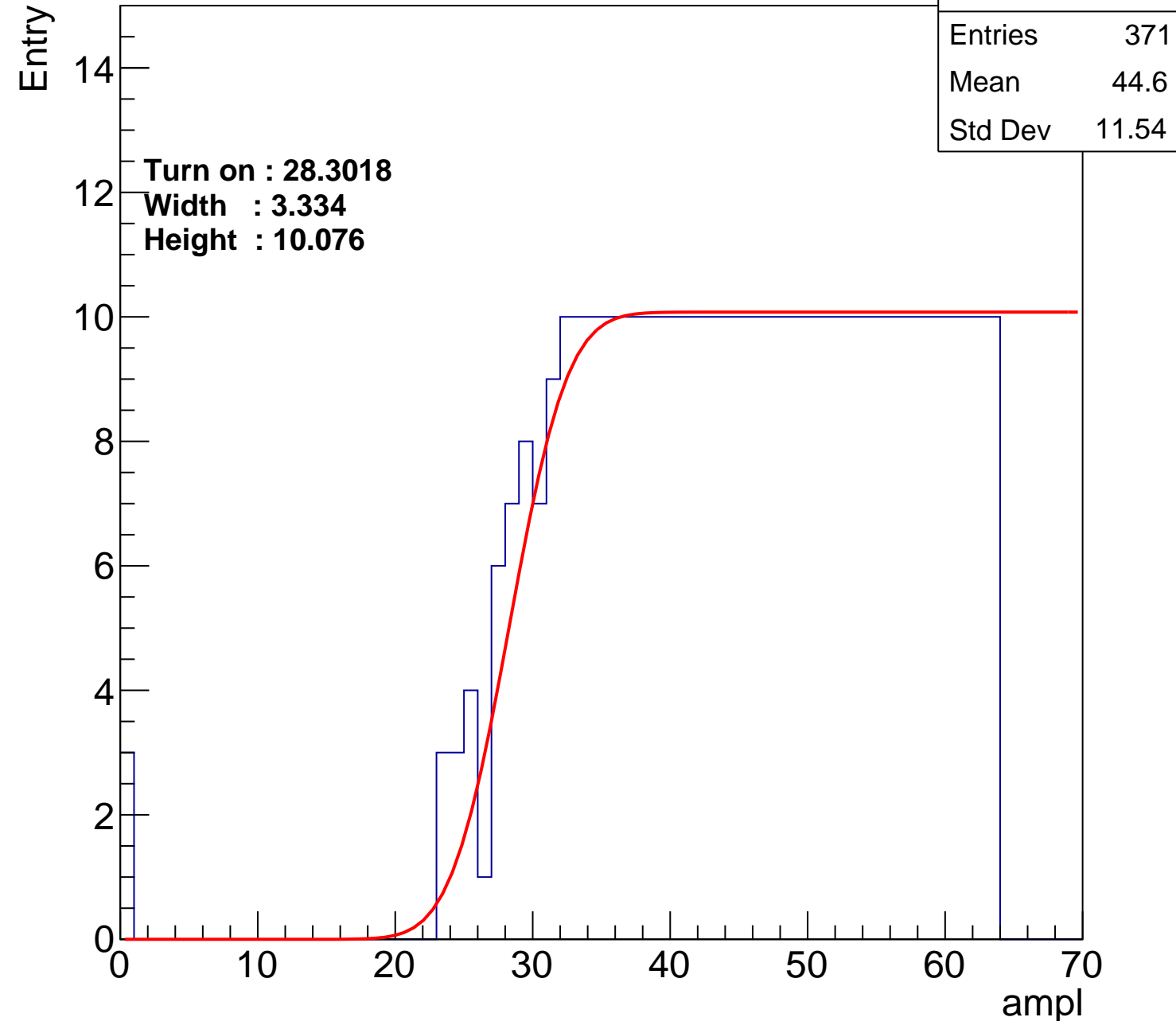
Width : 3.334

Height : 10.076

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch37

calib_packv5_042523_0143.root, FC#0, port D2

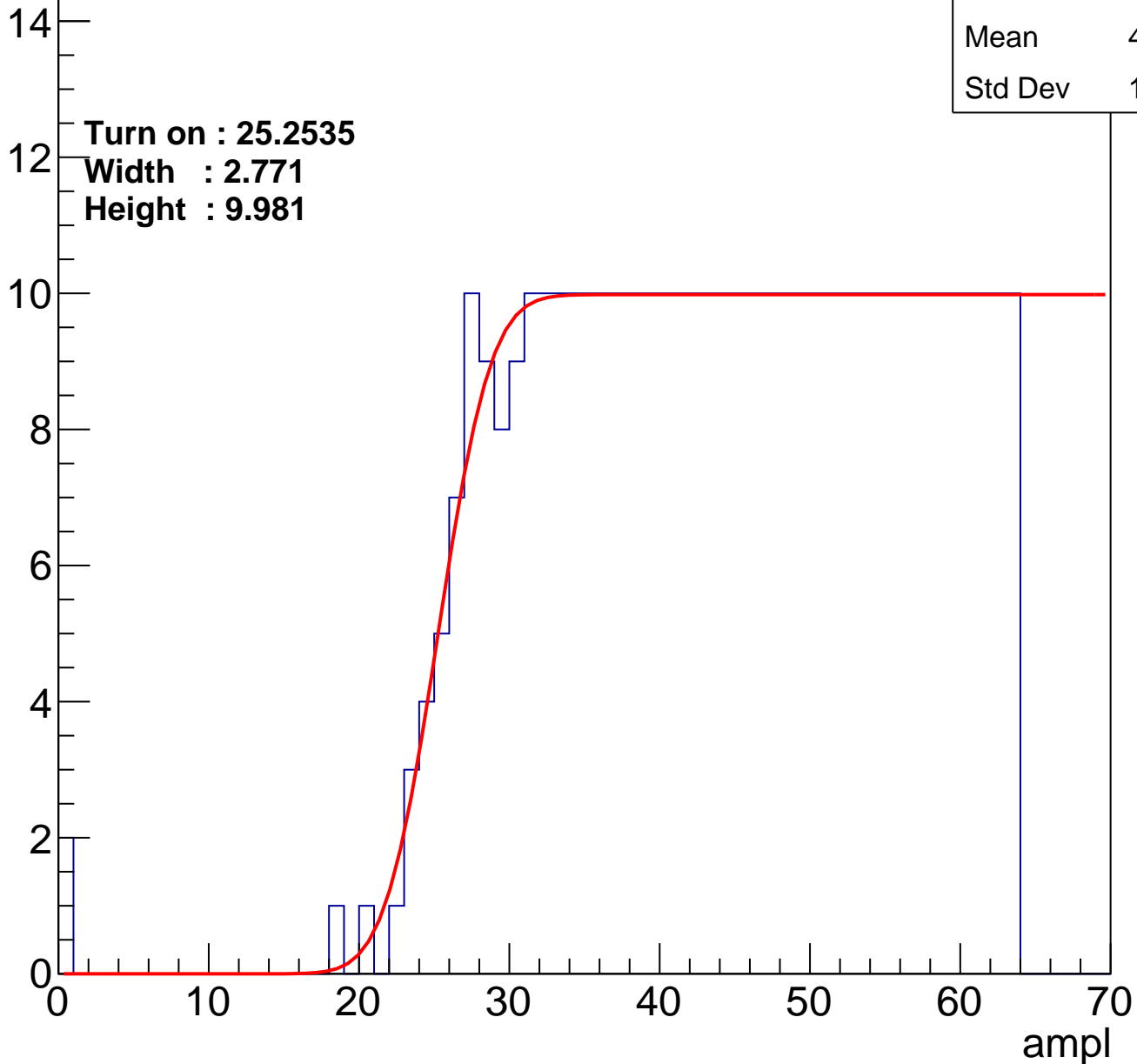
Entries	390
Mean	43.76
Std Dev	11.79

Turn on : 25.2535

Width : 2.771

Height : 9.981

Entry



calib_packv5_042523_0143.root, FC#0, port D2

Entries	384
Mean	43.94
Std Dev	11.96

Mean	43.94
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Std Dev	11.96
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Width : 2.620

Height : 10.023



B1L101S, U15-ch39

calib_packv5_042523_0143.root, FC#0, port D2

Entries	394
Mean	43.47
Std Dev	12.16

Turn on : 24.9182

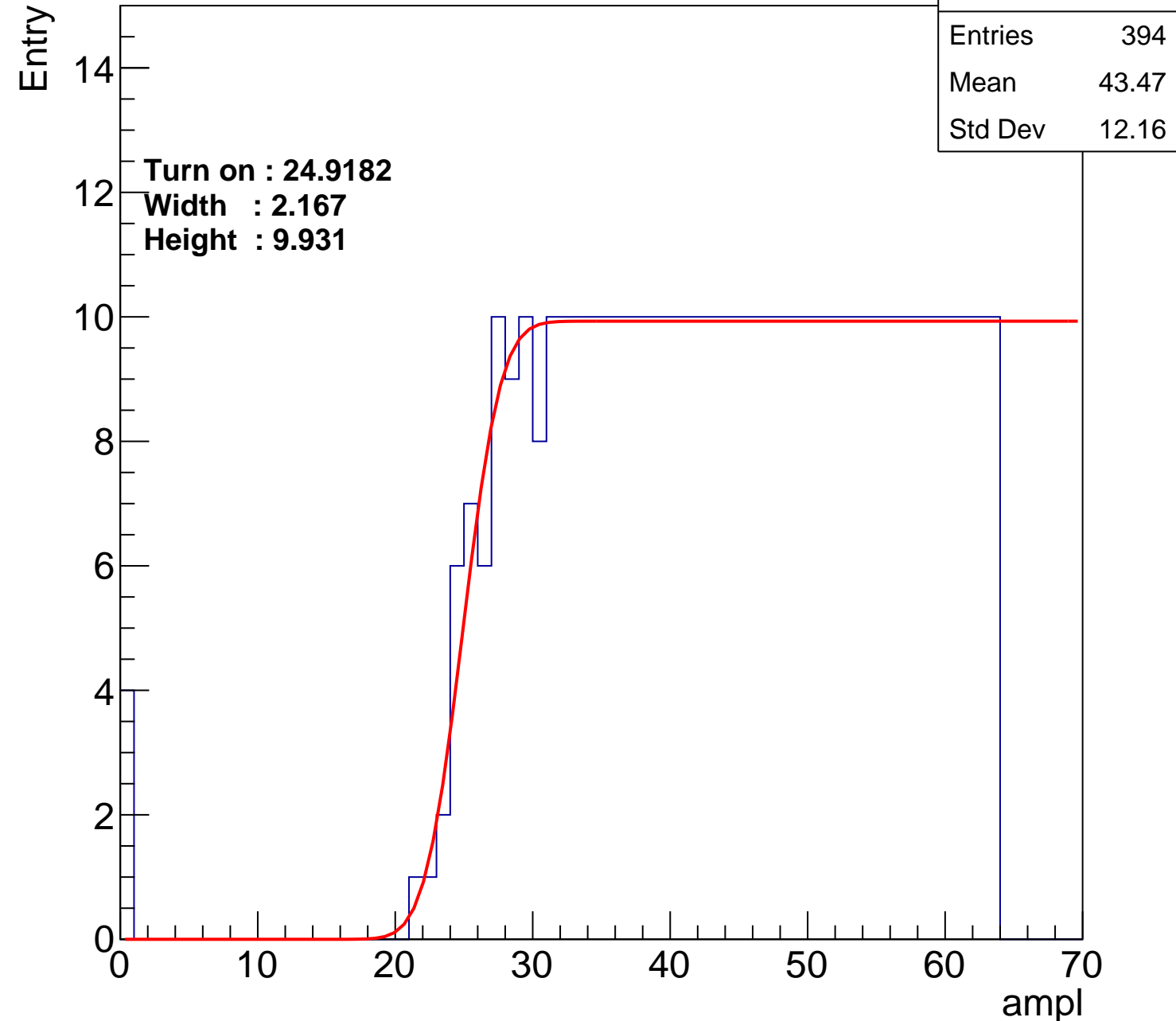
Width : 2.167

Height : 9.931

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch40

calib_packv5_042523_0143.root, FC#0, port D2

Entries	363
Mean	44.91
Std Dev	11.55

Turn on : 27.9567

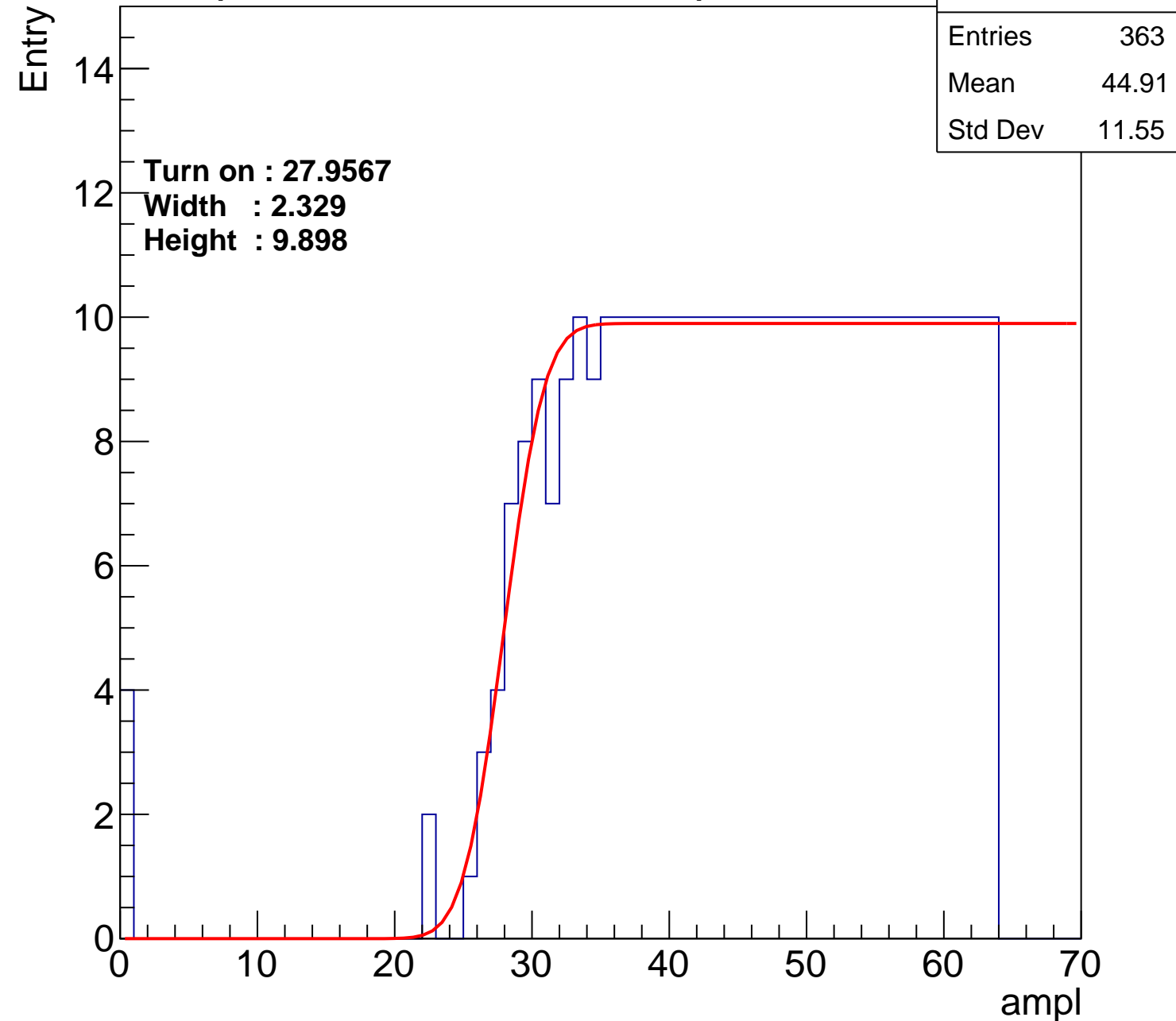
Width : 2.329

Height : 9.898

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch41

calib_packv5_042523_0143.root, FC#0, port D2

Entries	360
Mean	45.33
Std Dev	10.79

Turn on : 28.7950

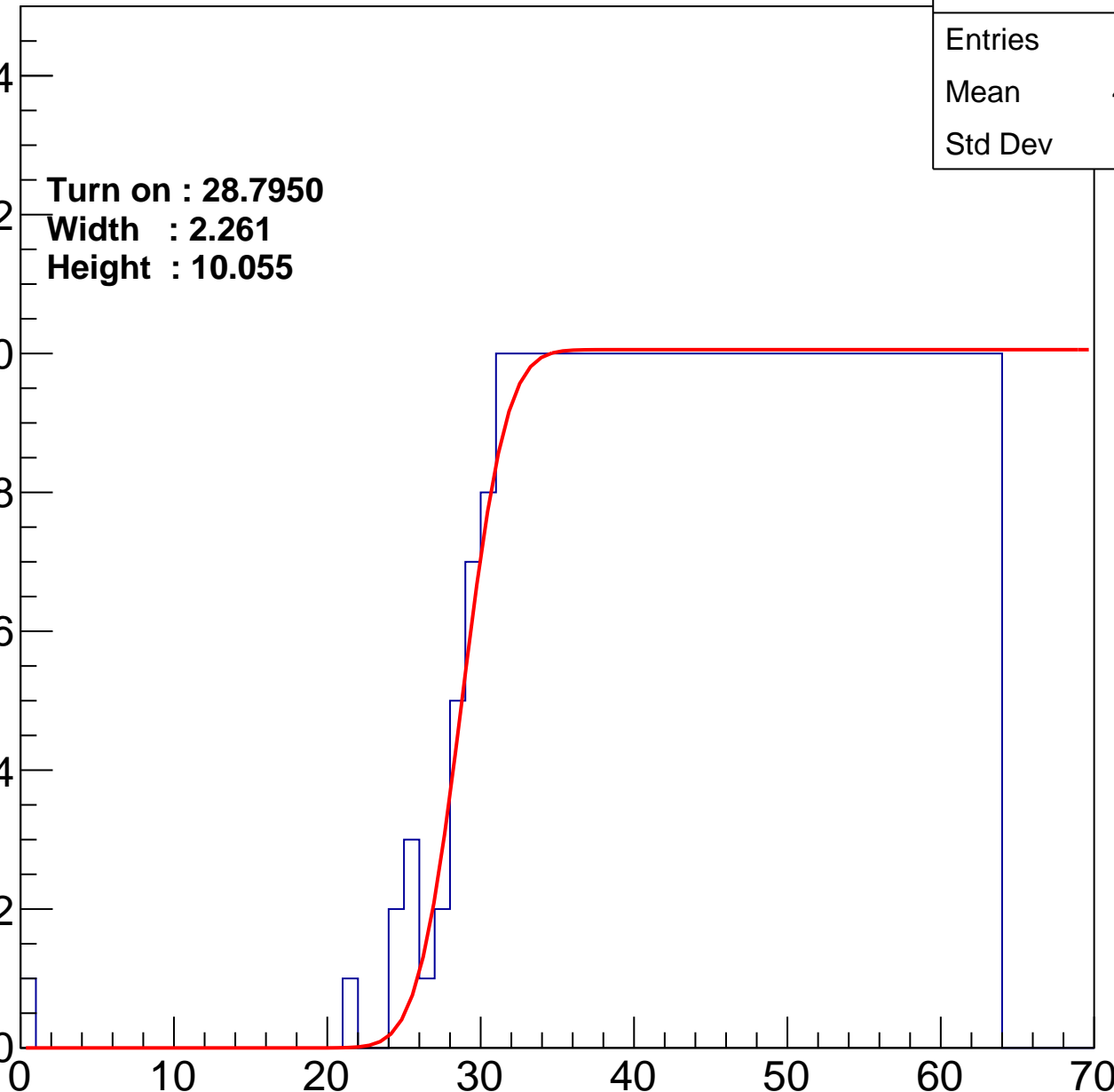
Width : 2.261

Height : 10.055

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch42

calib_packv5_042523_0143.root, FC#0, port D2

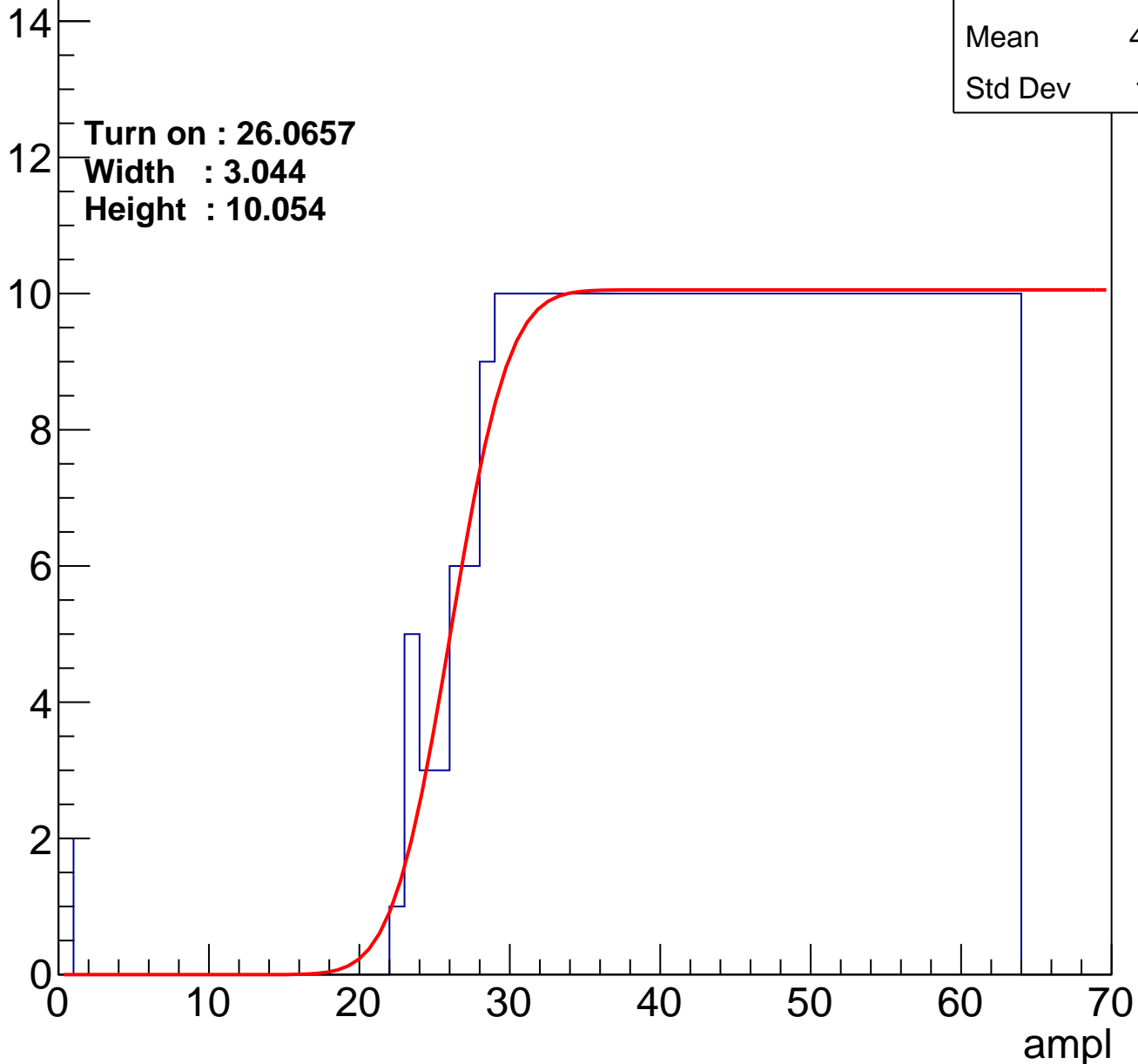
Entries	385
Mean	44.04
Std Dev	11.61

Turn on : 26.0657

Width : 3.044

Height : 10.054

Entry



B1L101S, U15-ch43

calib_packv5_042523_0143.root, FC#0, port D2

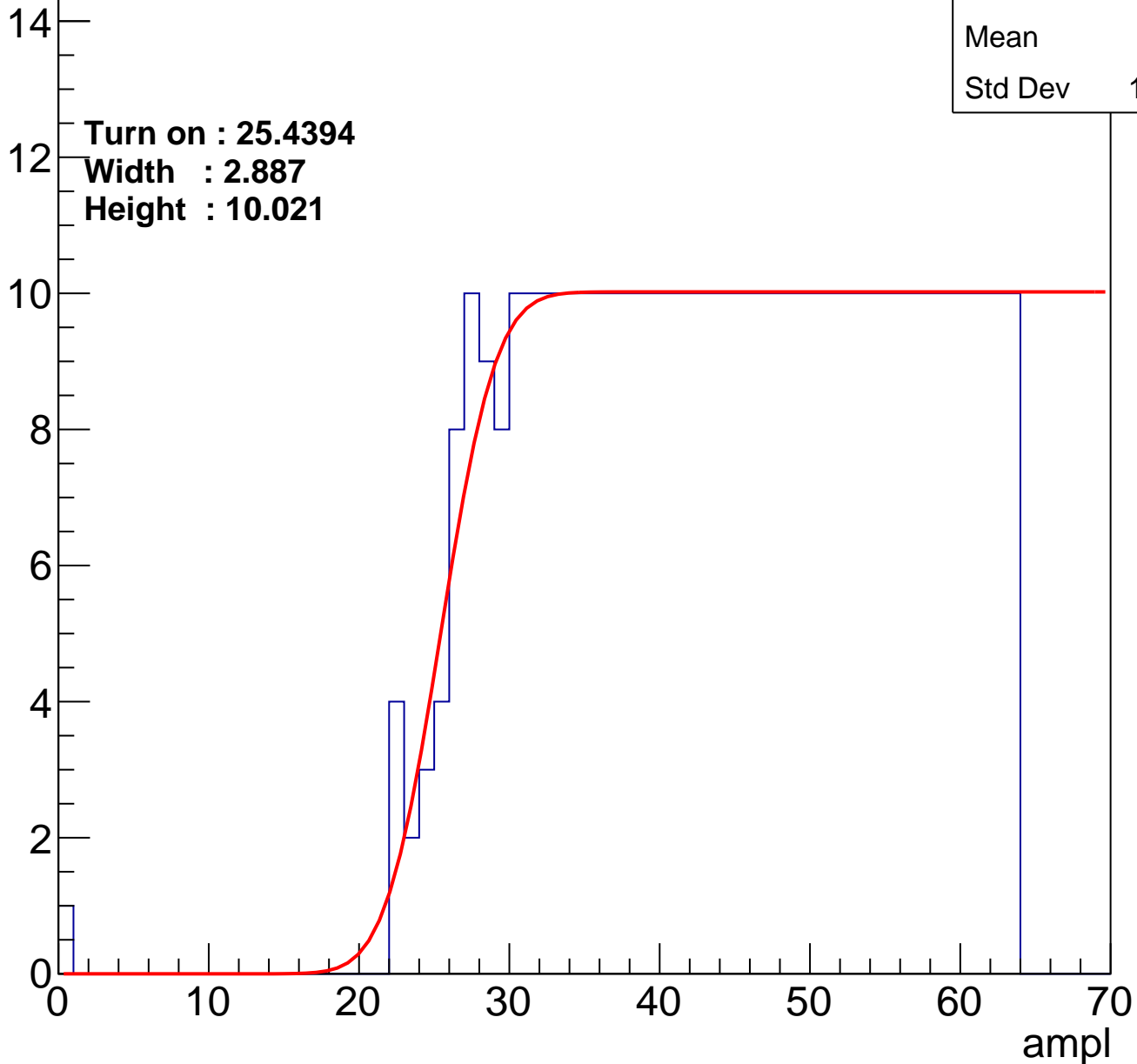
Entries	389
Mean	43.9
Std Dev	11.54

Turn on : 25.4394

Width : 2.887

Height : 10.021

Entry



B1L101S, U15-ch44

calib_packv5_042523_0143.root, FC#0, port D2

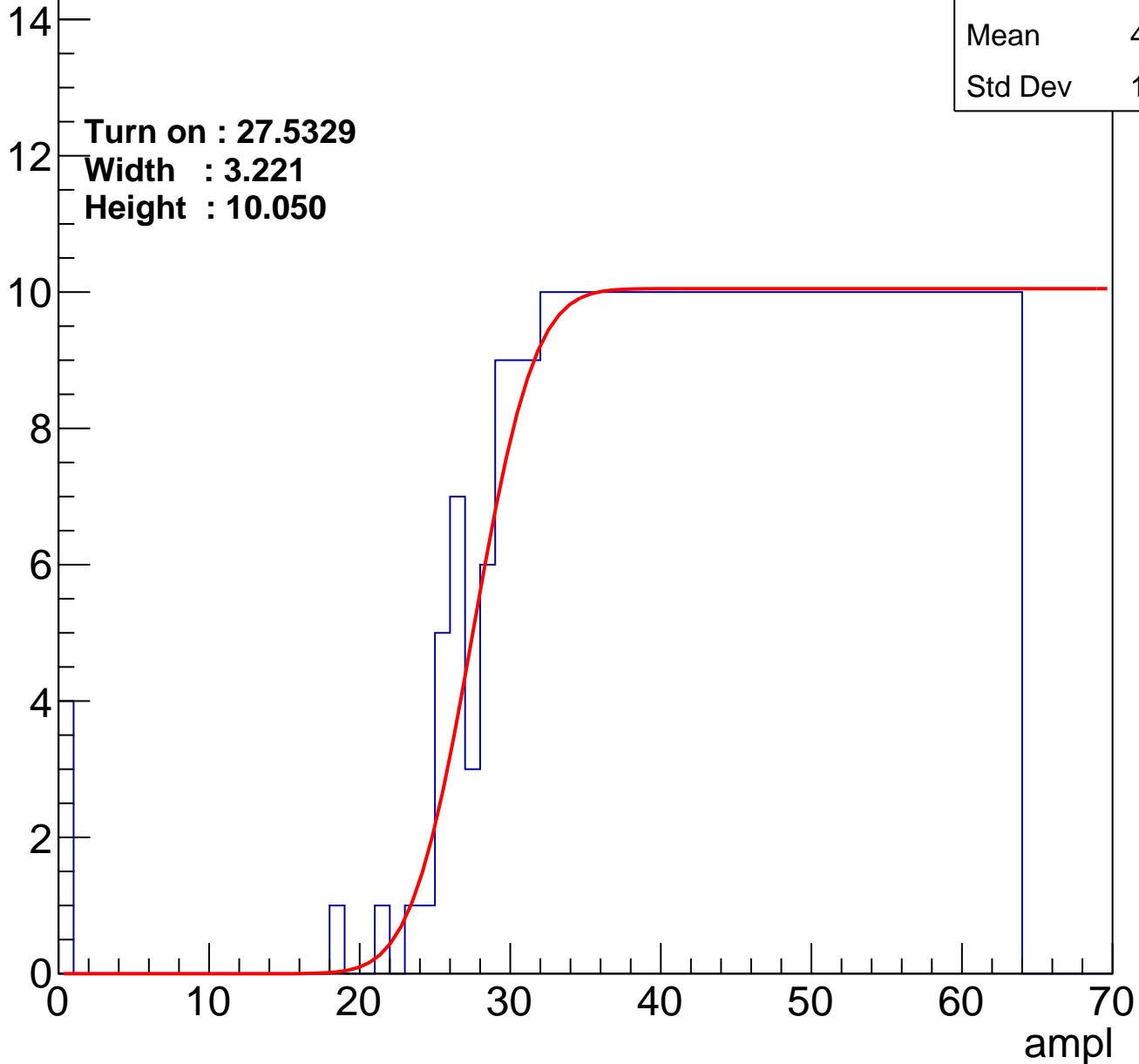
Entries	376
Mean	44.29
Std Dev	11.84

Turn on : 27.5329

Width : 3.221

Height : 10.050

Entry



B1L101S, U15-ch45

calib_packv5_042523_0143.root, FC#0, port D2

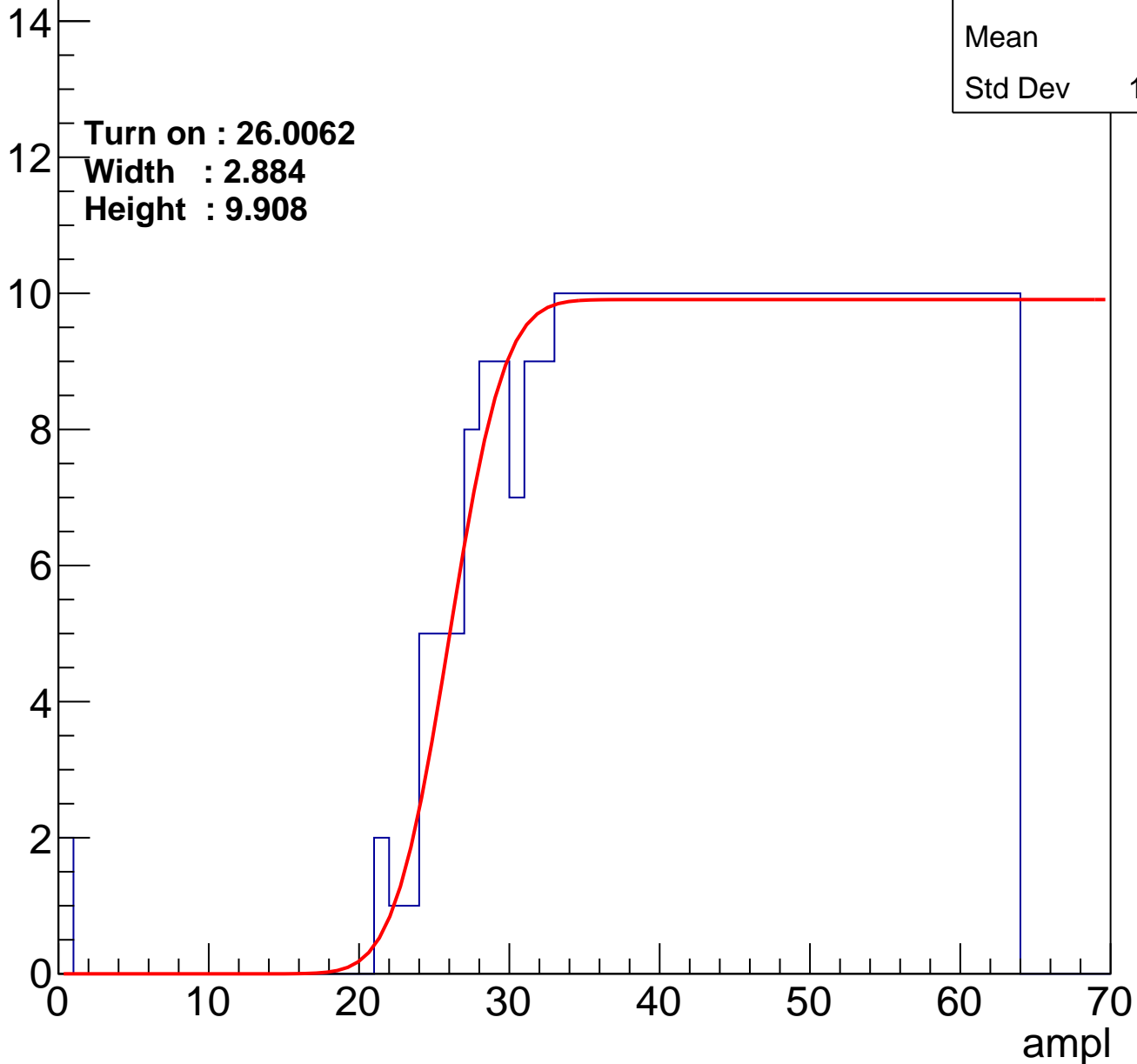
Entries	382
Mean	44.1
Std Dev	11.65

Turn on : 26.0062

Width : 2.884

Height : 9.908

Entry



B1L101S, U15-ch46

calib_packv5_042523_0143.root, FC#0, port D2

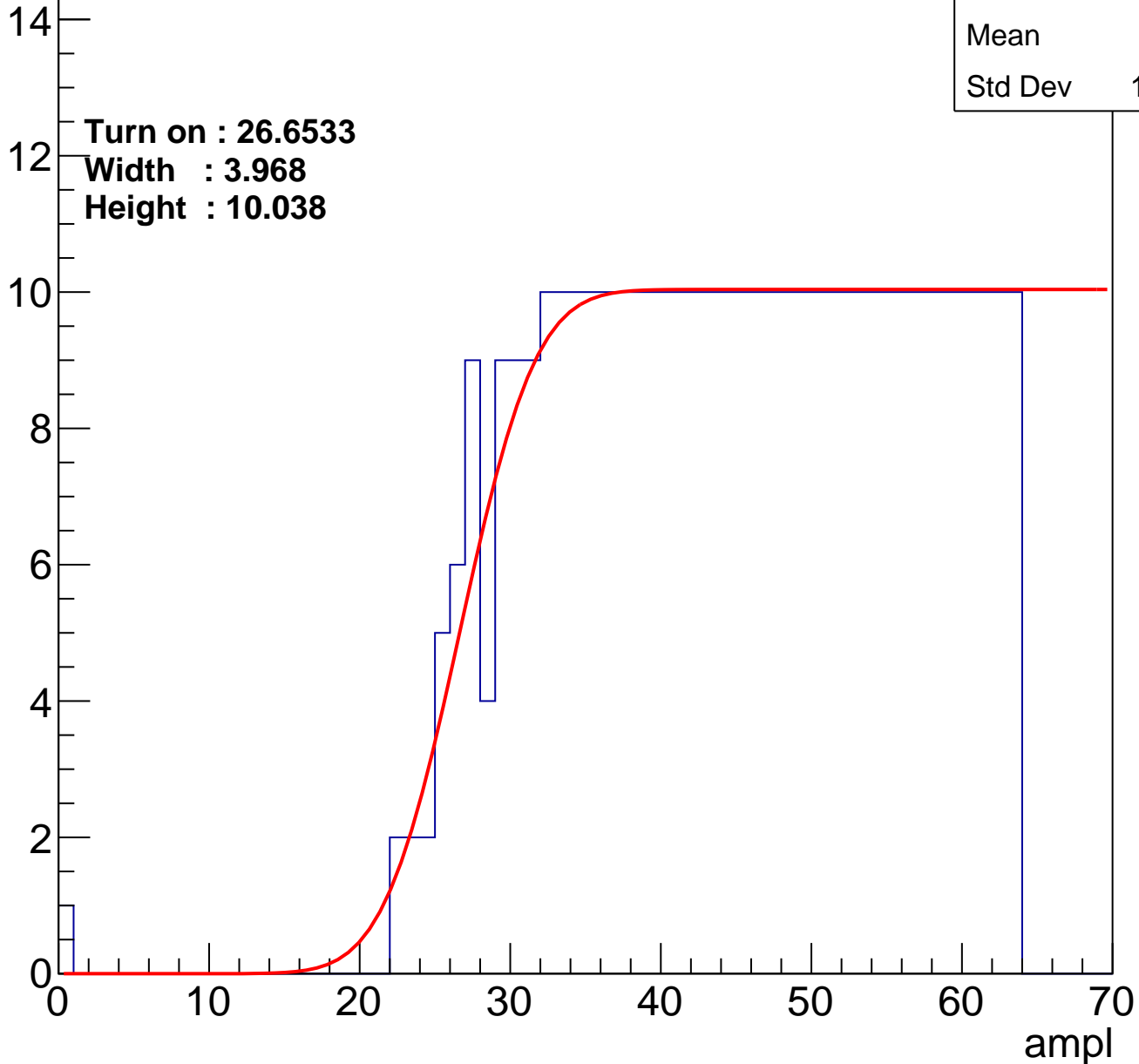
Entries	378
Mean	44.4
Std Dev	11.32

Turn on : 26.6533

Width : 3.968

Height : 10.038

Entry



B1L101S, U15-ch47

calib_packv5_042523_0143.root, FC#0, port D2

Entries	365
Mean	44.95
Std Dev	11.31

Turn on : 27.5760

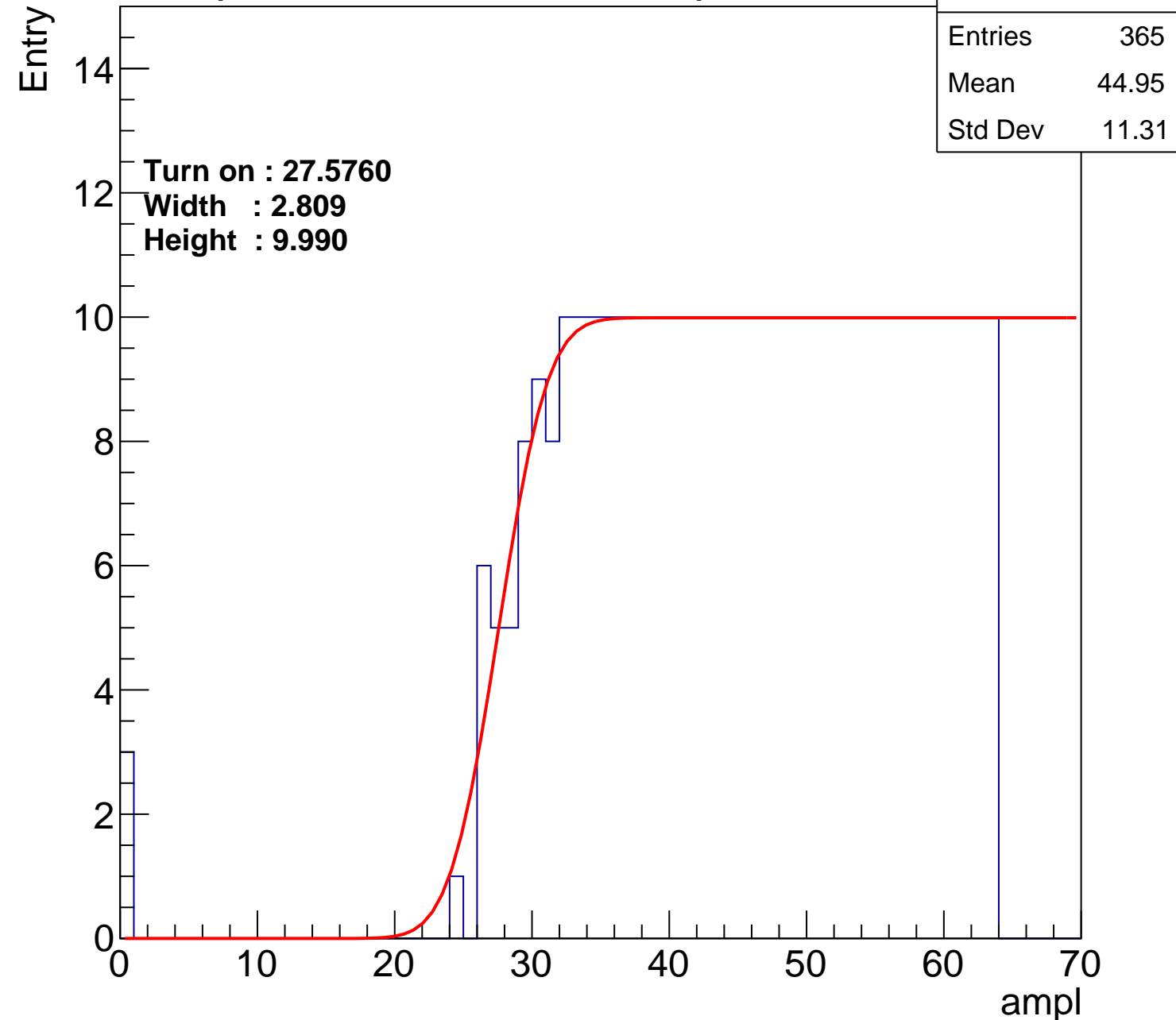
Width : 2.809

Height : 9.990

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch48

calib_packv5_042523_0143.root, FC#0, port D2

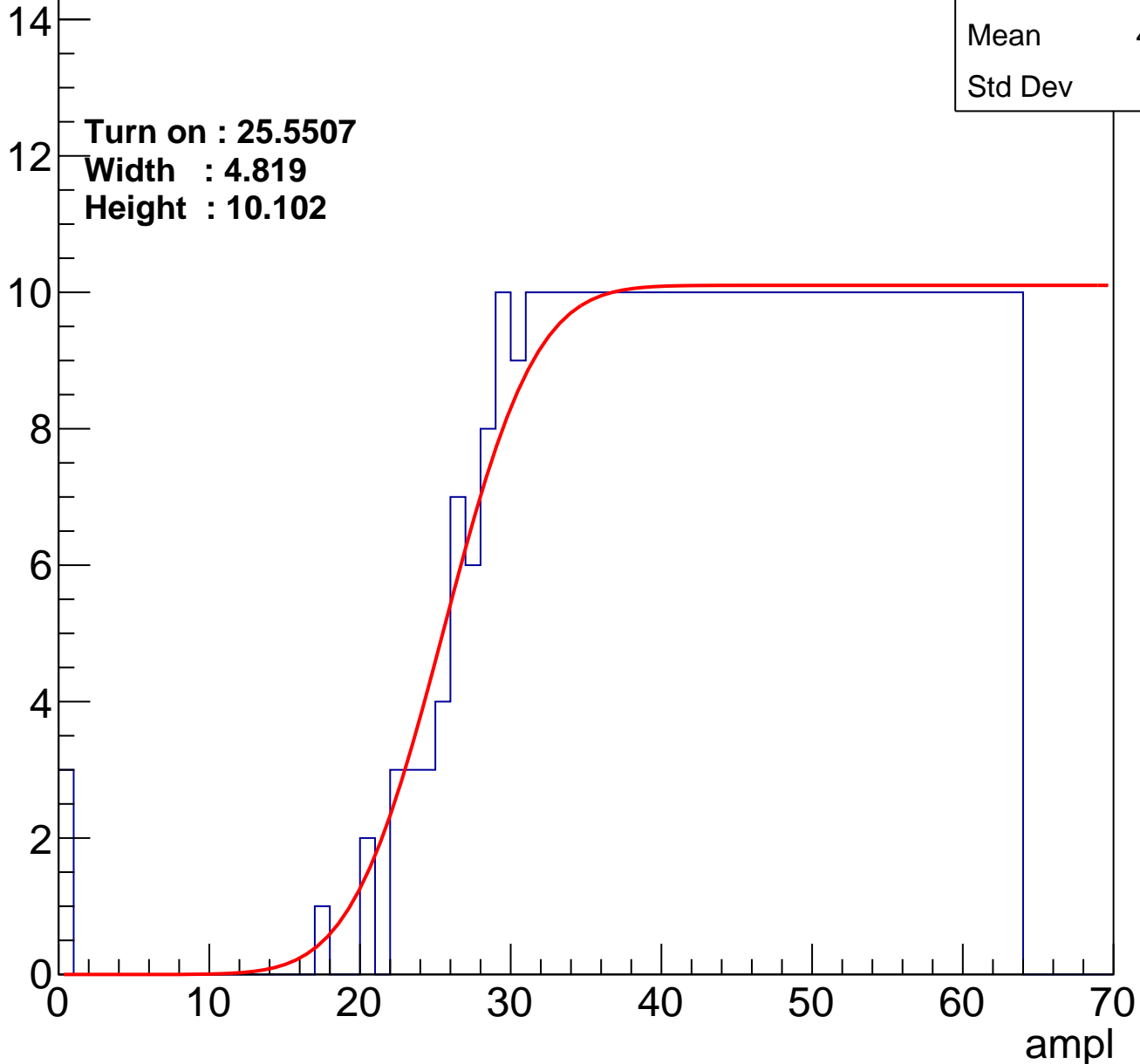
Entries	389
Mean	43.71
Std Dev	12

Turn on : 25.5507

Width : 4.819

Height : 10.102

Entry



B1L101S, U15-ch49

calib_packv5_042523_0143.root, FC#0, port D2

Entries	370
Mean	44.51
Std Dev	11.89

Turn on : 27.8784

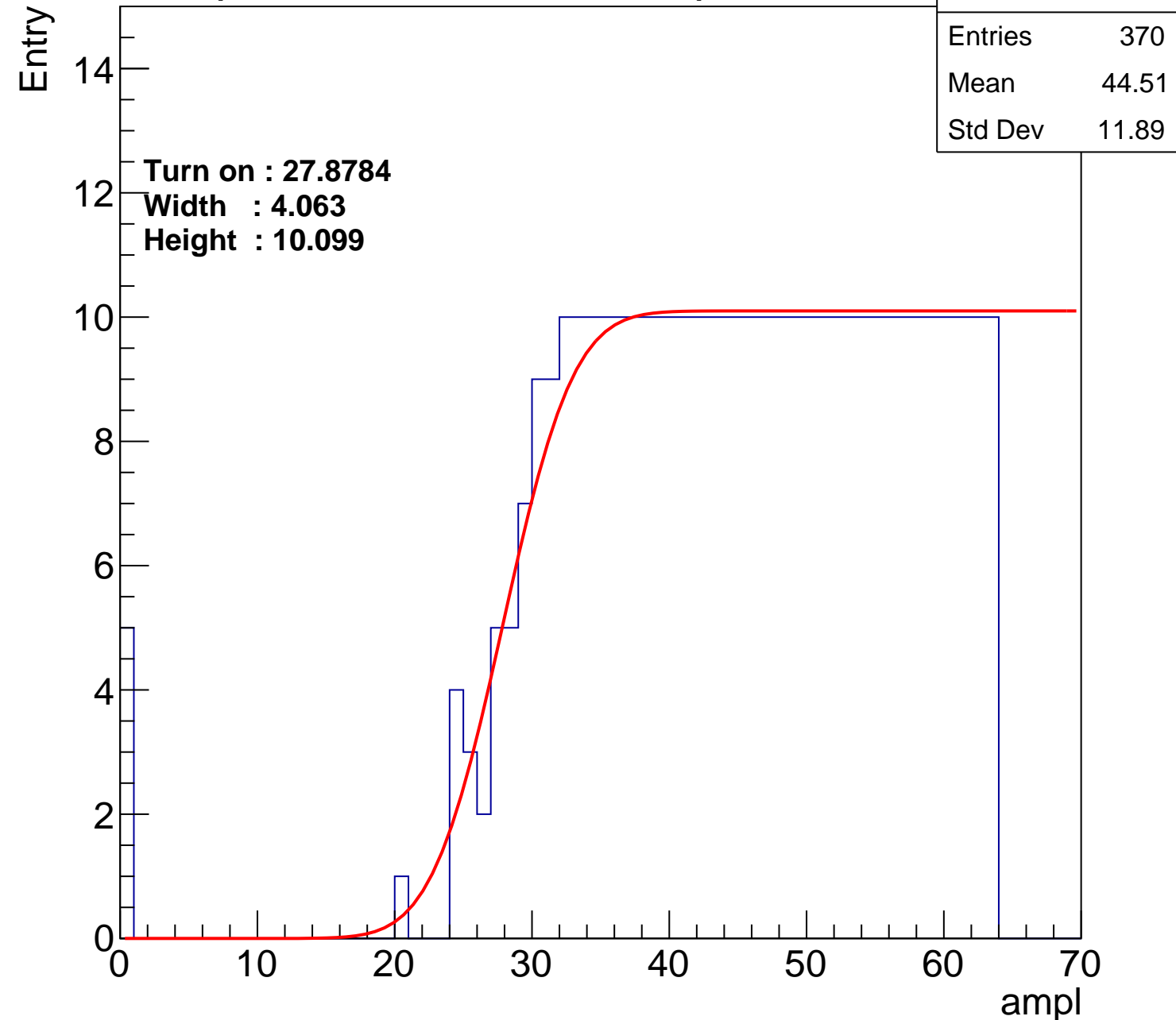
Width : 4.063

Height : 10.099

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch50

calib_packv5_042523_0143.root, FC#0, port D2

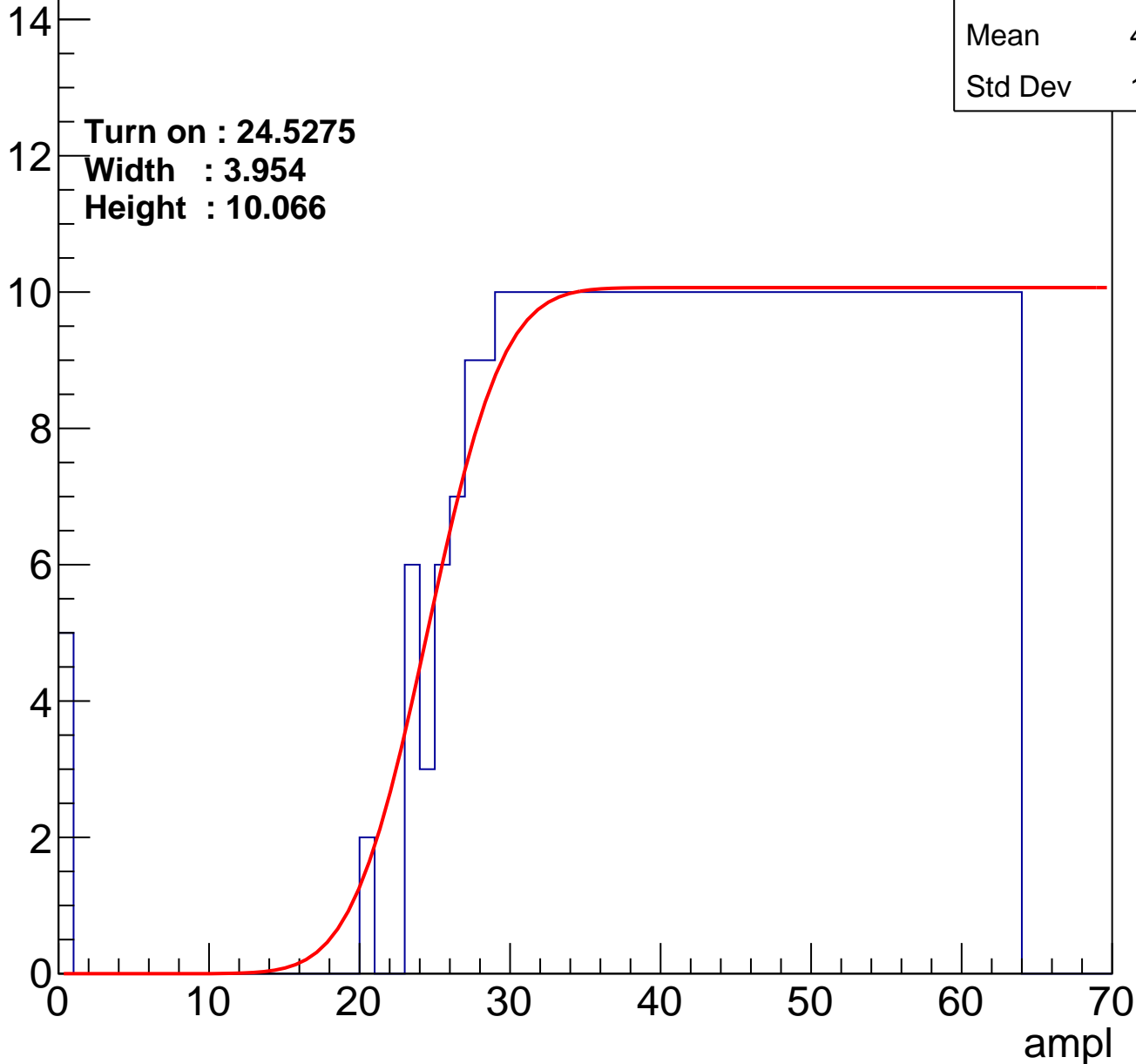
Entries	397
Mean	43.27
Std Dev	12.39

Turn on : 24.5275

Width : 3.954

Height : 10.066

Entry



B1L101S, U15-ch51

calib_packv5_042523_0143.root, FC#0, port D2

Entries	372
Mean	44.58
Std Dev	11.51

Turn on : 27.1656

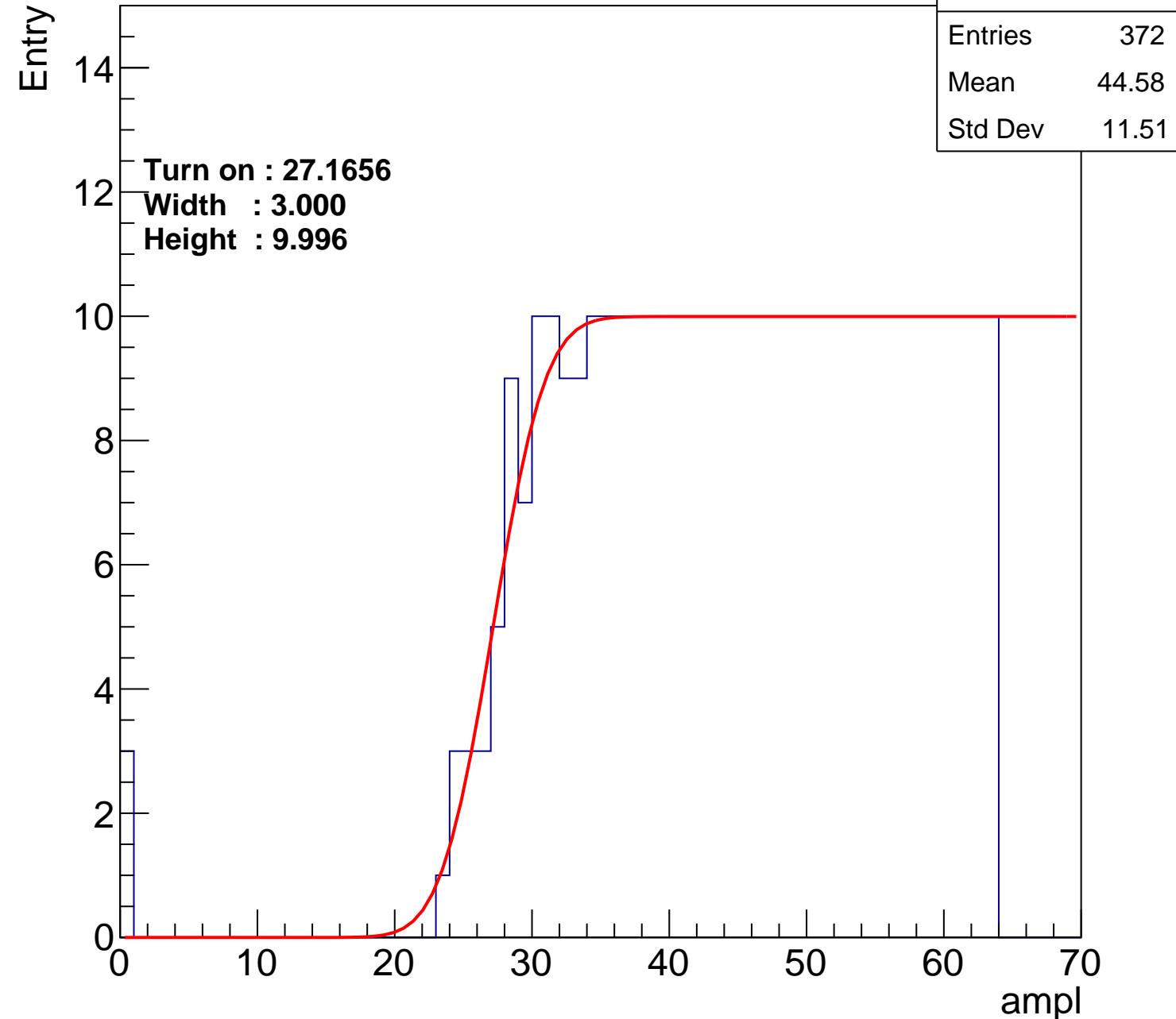
Width : 3.000

Height : 9.996

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch52

calib_packv5_042523_0143.root, FC#0, port D2

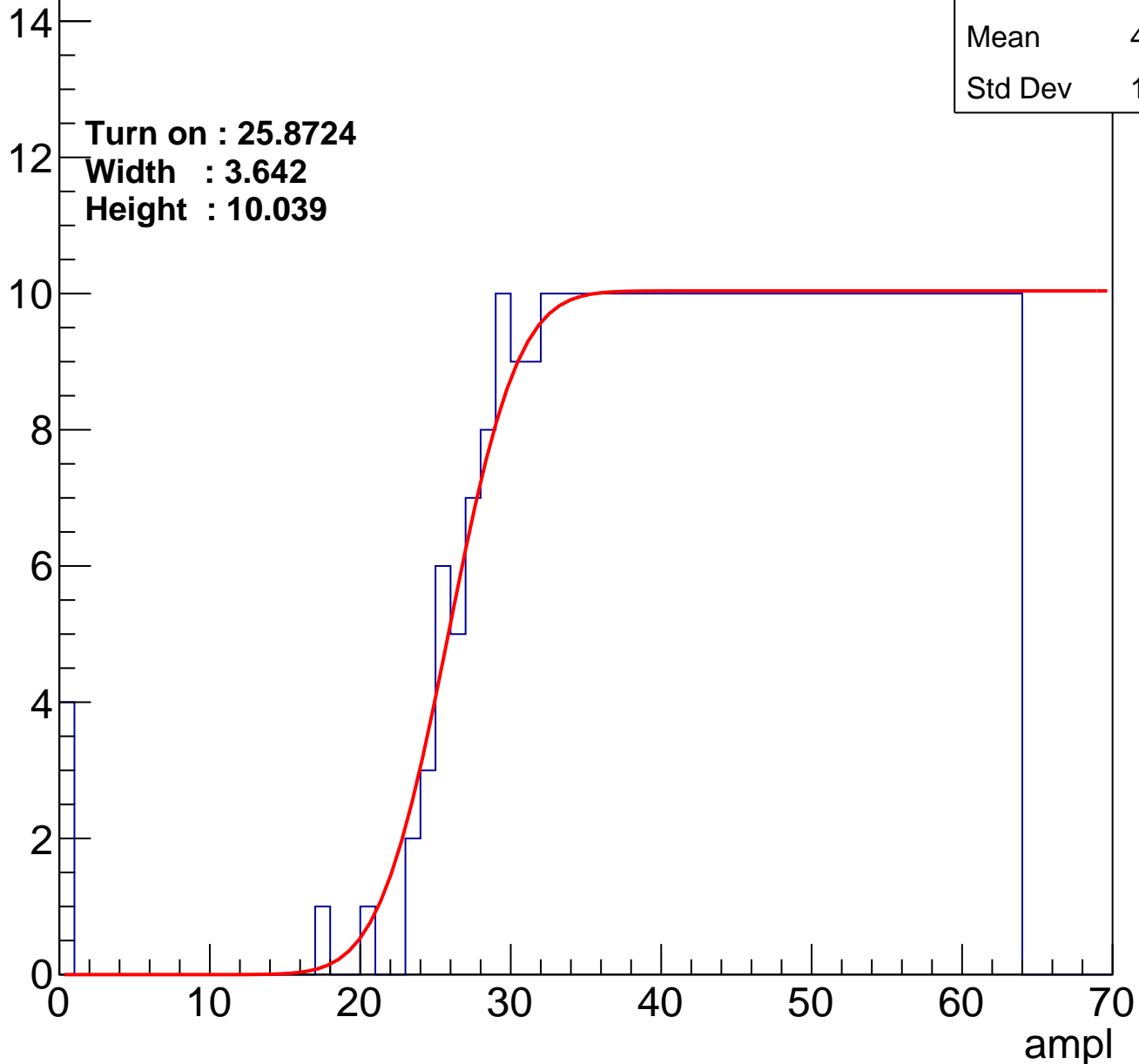
Entries	385
Mean	43.86
Std Dev	12.03

Turn on : 25.8724

Width : 3.642

Height : 10.039

Entry



B1L101S, U15-ch53

calib_packv5_042523_0143.root, FC#0, port D2

Entries	375
Mean	44.22
Std Dev	12.15

Turn on : 27.6810

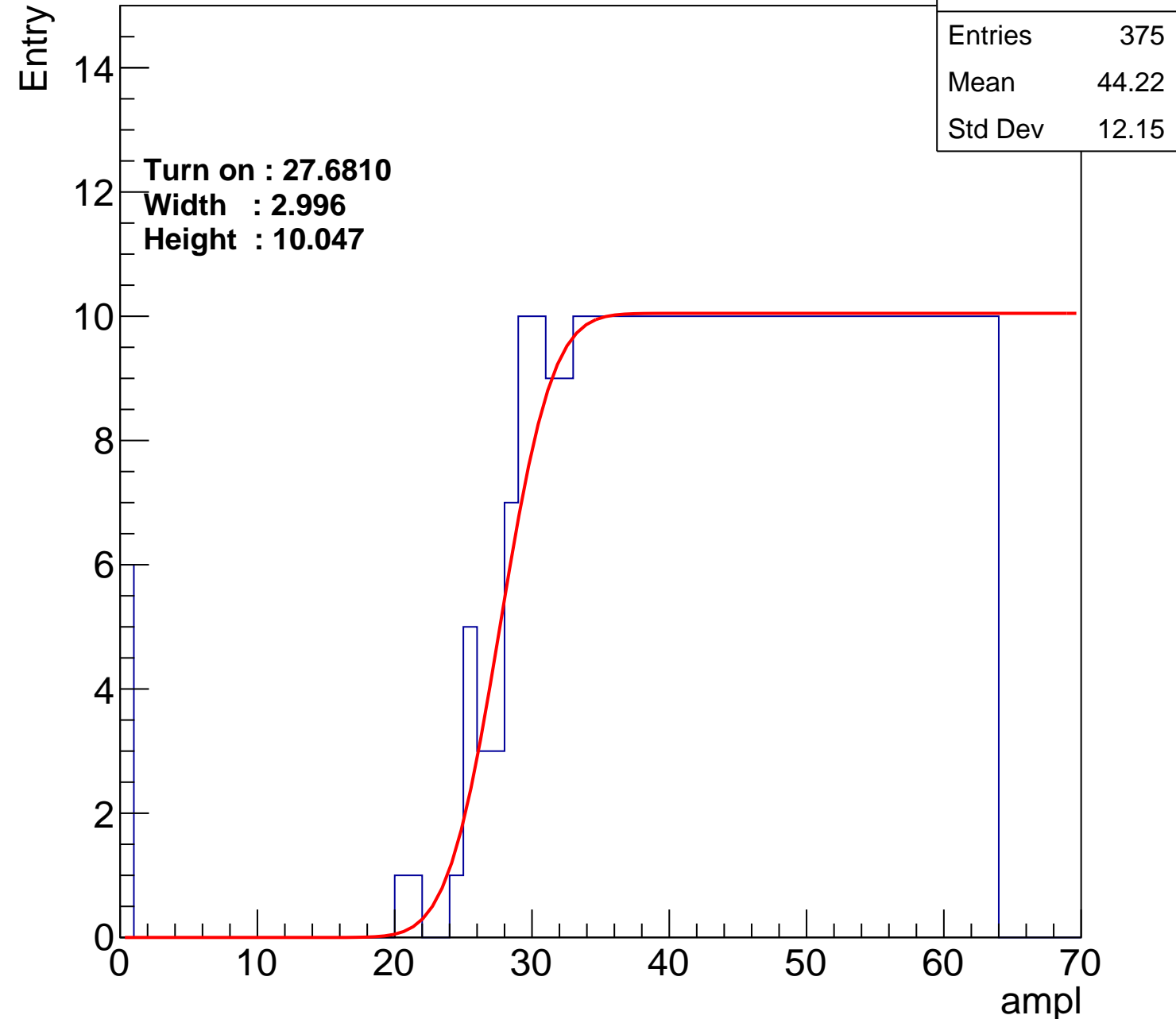
Width : 2.996

Height : 10.047

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch54

calib_packv5_042523_0143.root, FC#0, port D2

Entries	365
Mean	44.75
Std Dev	11.8

Turn on : 27.5929

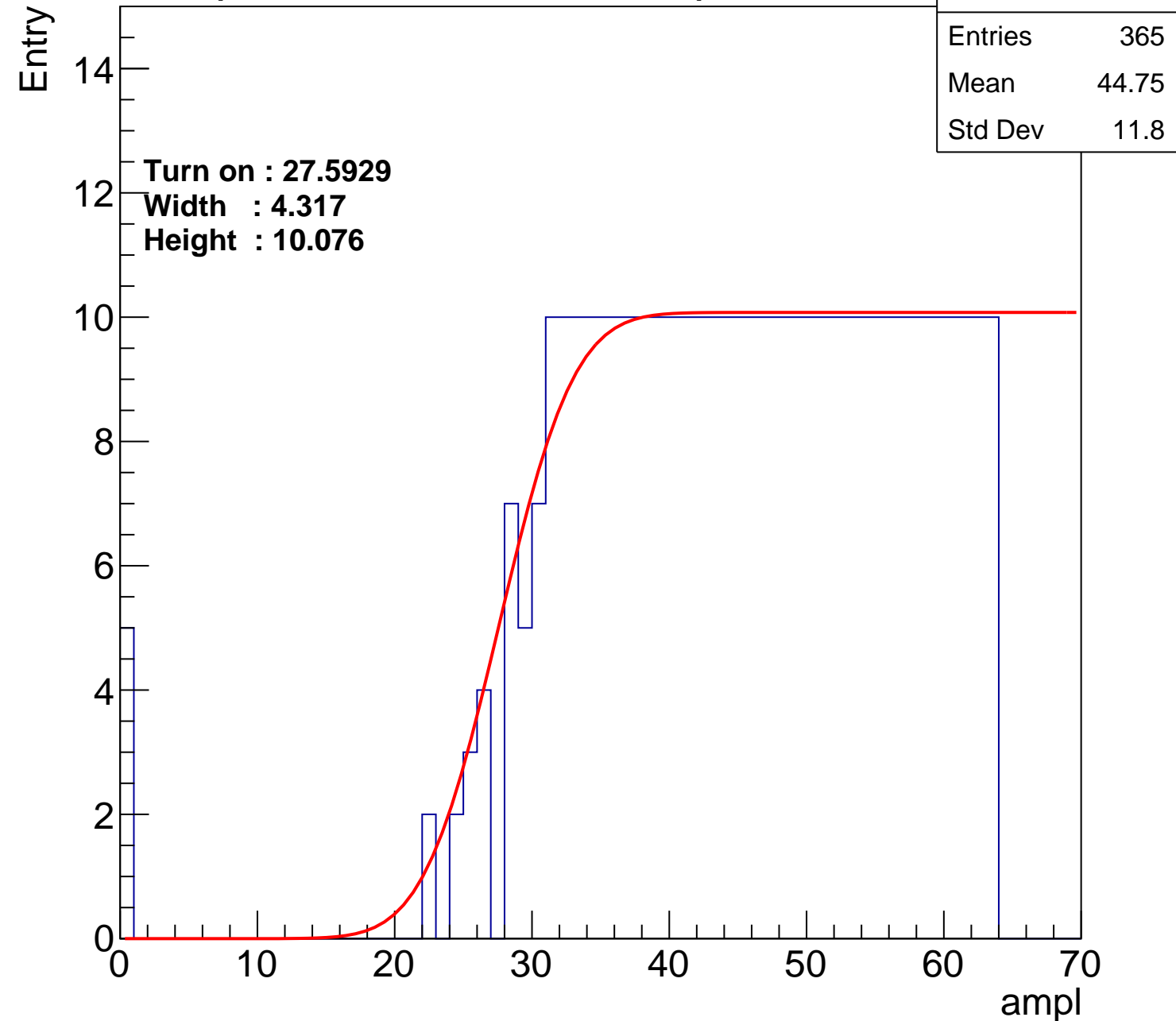
Width : 4.317

Height : 10.076

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch55

calib_packv5_042523_0143.root, FC#0, port D2

Entries	361
Mean	45.17
Std Dev	11.07

Turn on : 27.9338

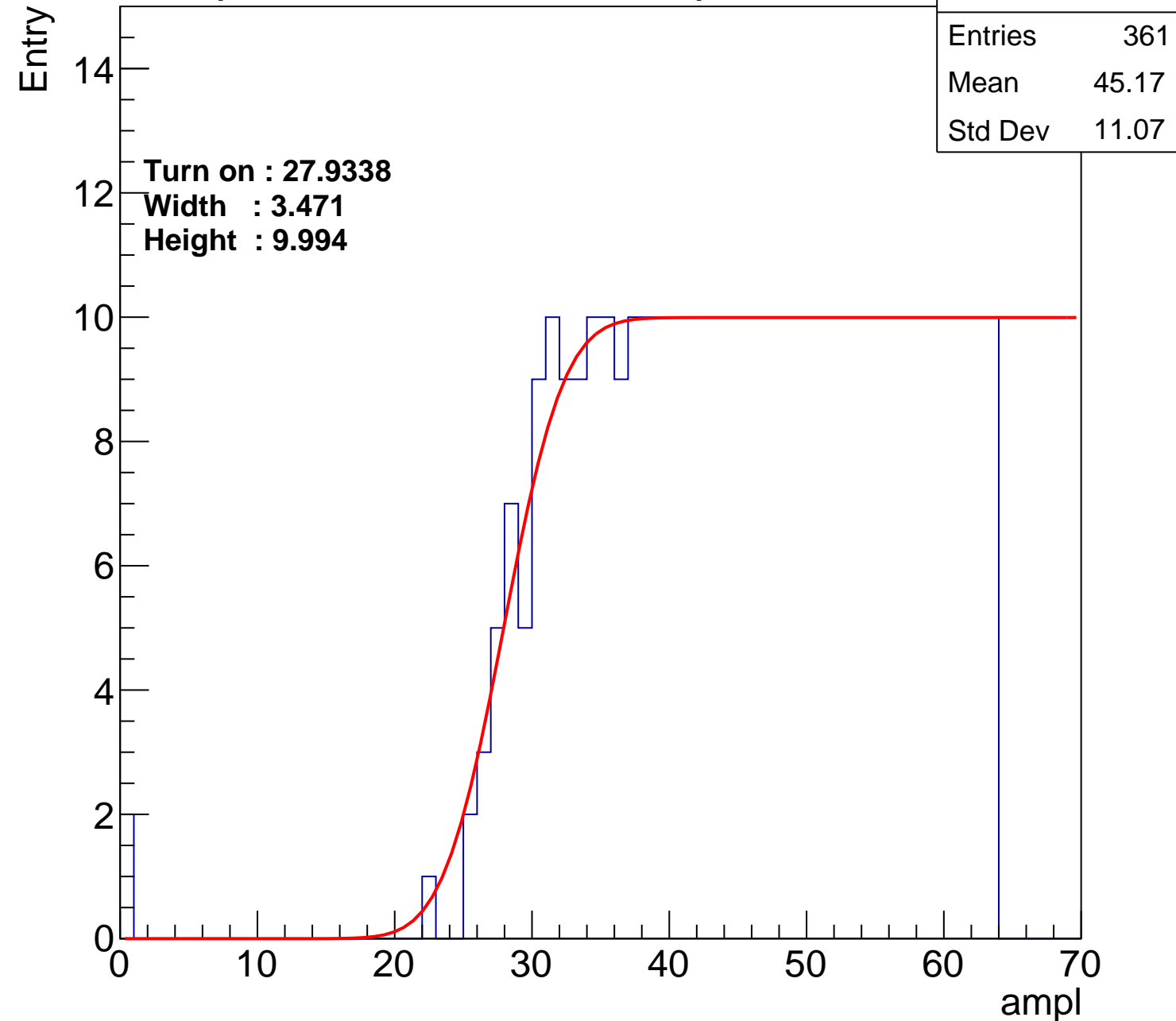
Width : 3.471

Height : 9.994

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch56

calib_packv5_042523_0143.root, FC#0, port D2

Entries	371
Mean	44.45
Std Dev	11.94

Turn on : 27.7976

Width : 2.342

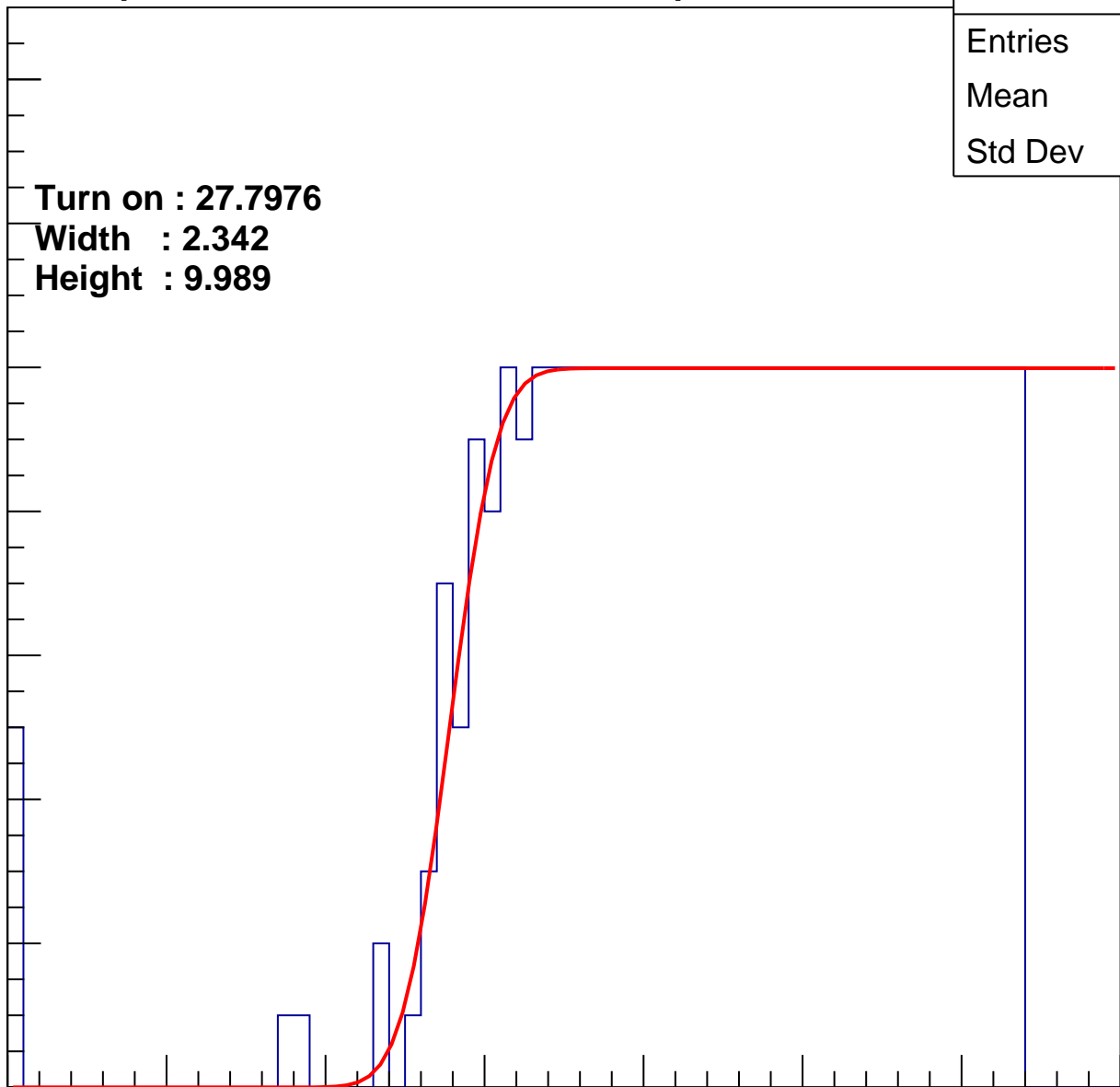
Height : 9.989

Entry

14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl



B1L101S, U15-ch57

calib_packv5_042523_0143.root, FC#0, port D2

Entries	361
Mean	45.09
Std Dev	11.29

Turn on : 28.2883

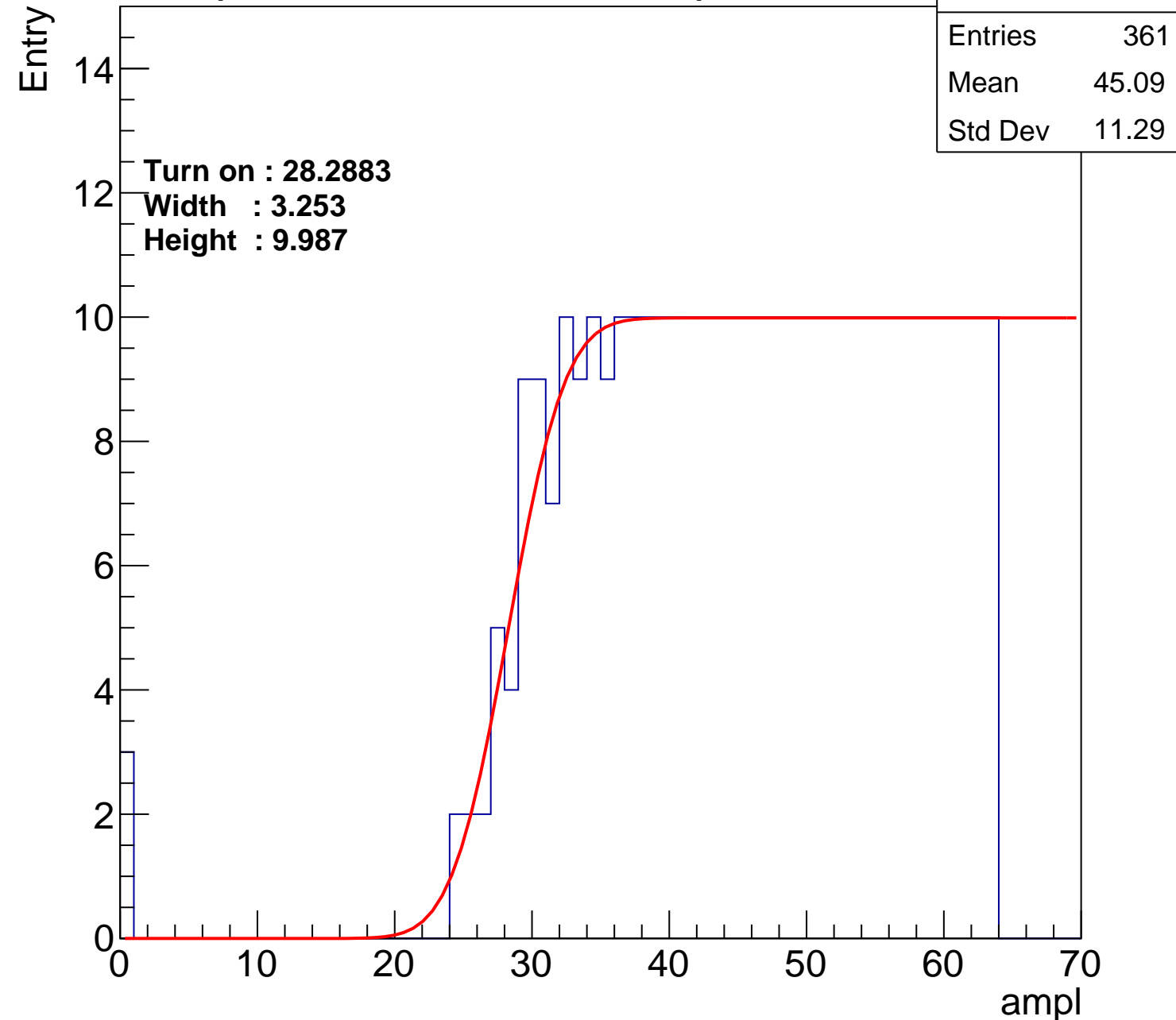
Width : 3.253

Height : 9.987

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch58

calib_packv5_042523_0143.root, FC#0, port D2

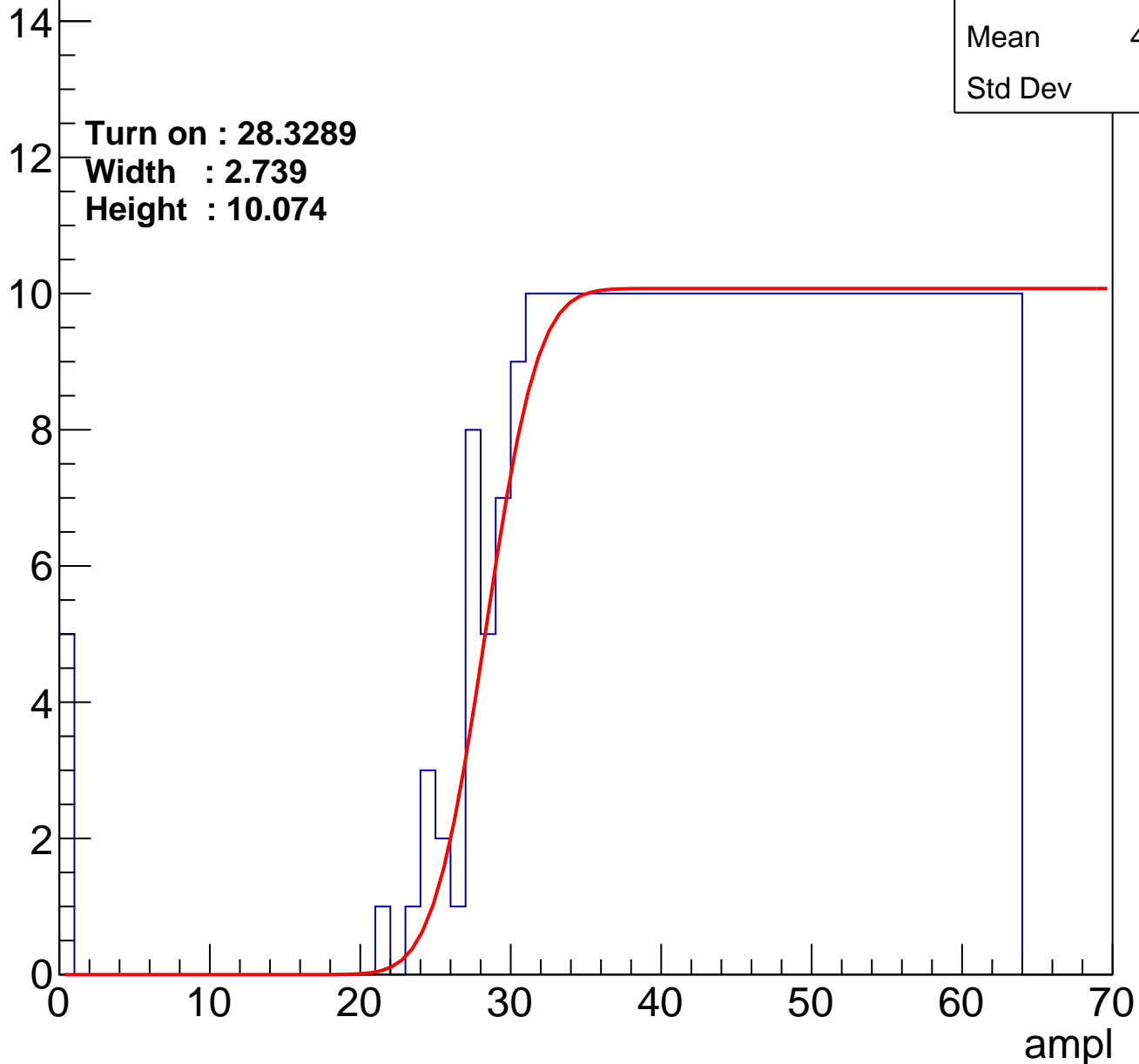
Entries	372
Mean	44.44
Std Dev	11.9

Turn on : 28.3289

Width : 2.739

Height : 10.074

Entry



B1L101S, U15-ch59

calib_packv5_042523_0143.root, FC#0, port D2

Entries	387
Mean	43.74
Std Dev	12.17

Turn on : 25.4766

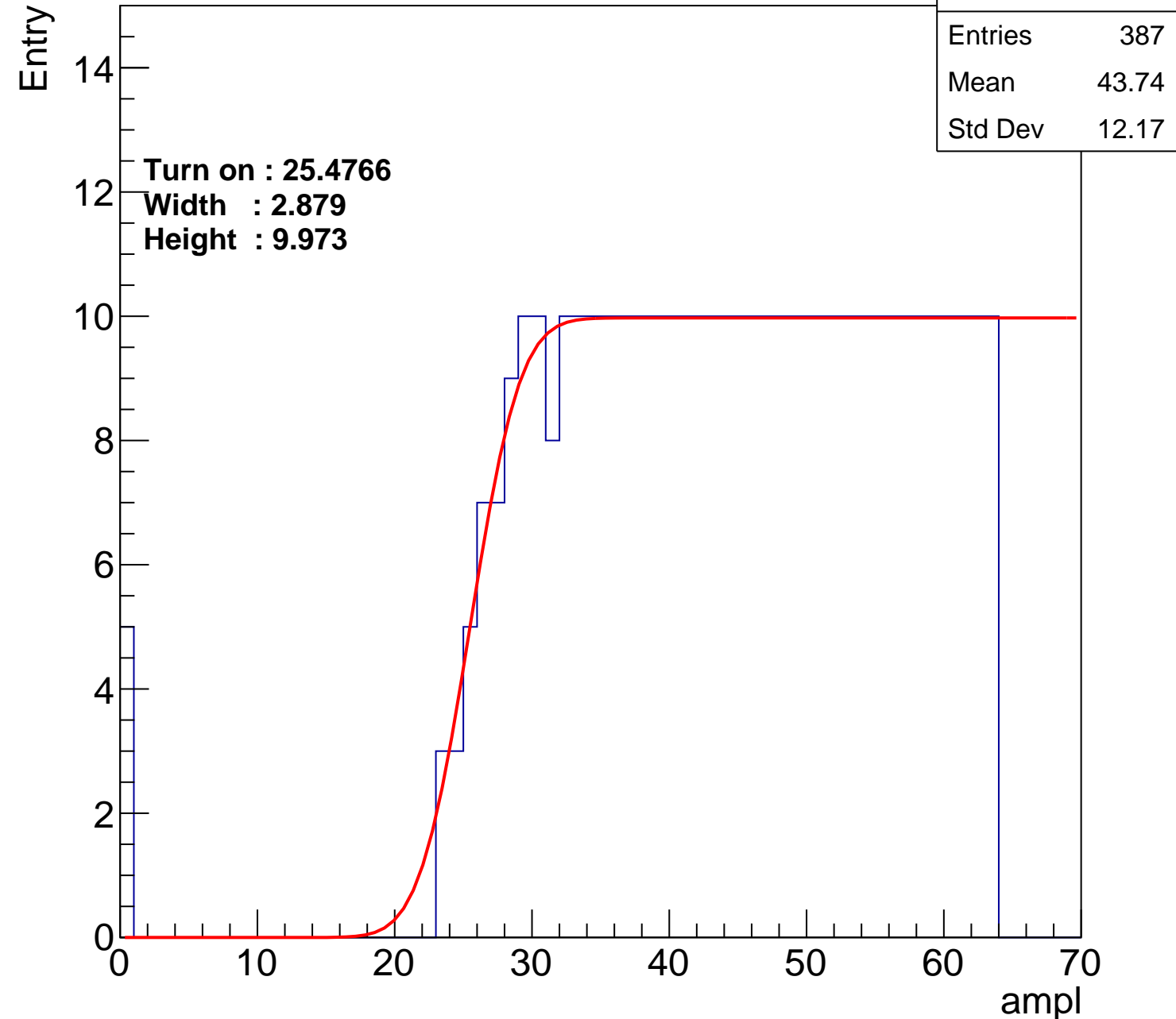
Width : 2.879

Height : 9.973

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch60

calib_packv5_042523_0143.root, FC#0, port D2

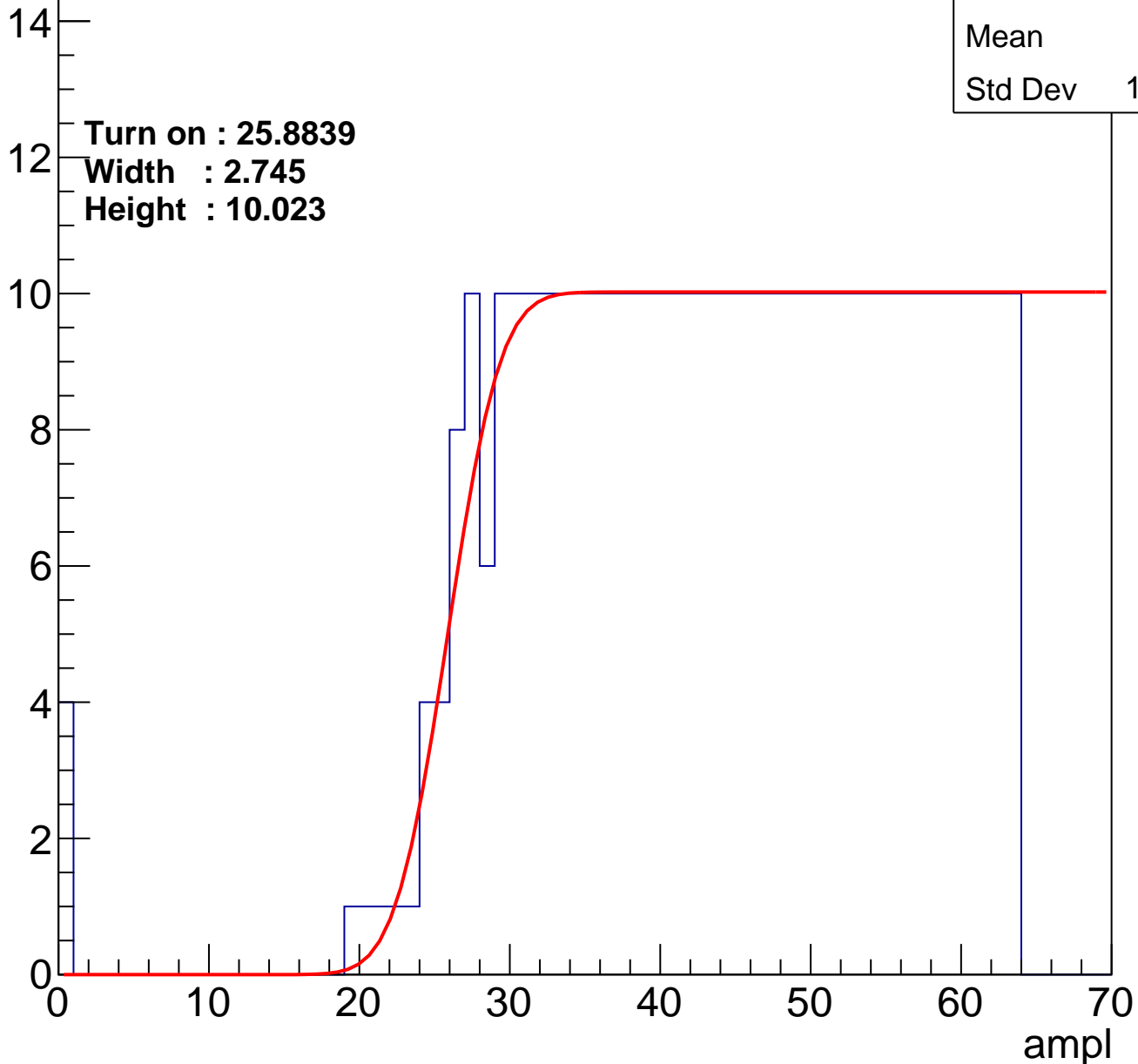
Entries	391
Mean	43.6
Std Dev	12.13

Turn on : 25.8839

Width : 2.745

Height : 10.023

Entry



B1L101S, U15-ch61

calib_packv5_042523_0143.root, FC#0, port D2

Entries	376
Mean	44.19
Std Dev	12.14

Turn on : 27.6878

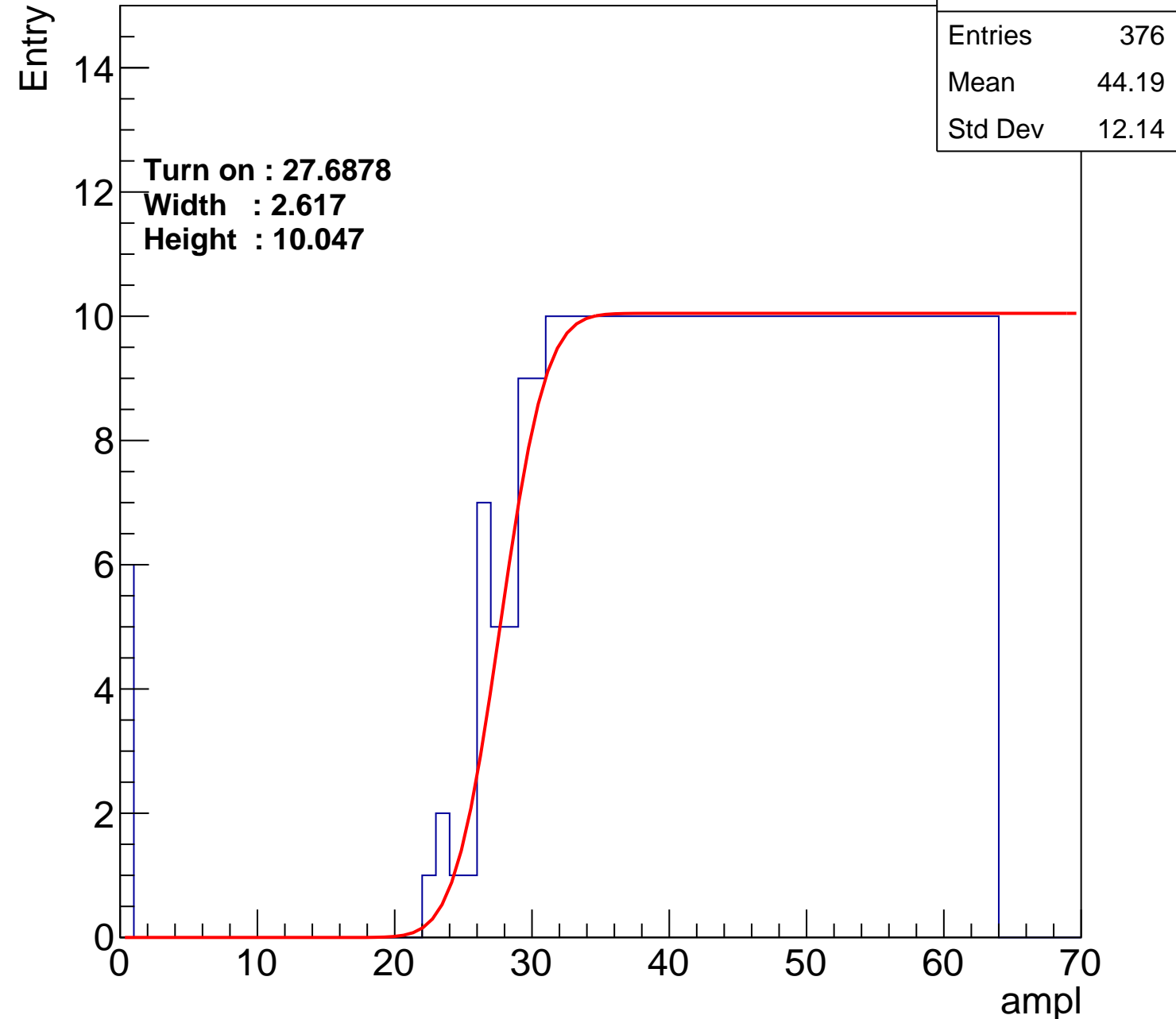
Width : 2.617

Height : 10.047

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch62

calib_packv5_042523_0143.root, FC#0, port D2

Entries	382
Mean	43.98
Std Dev	12.06

Turn on : 26.0465

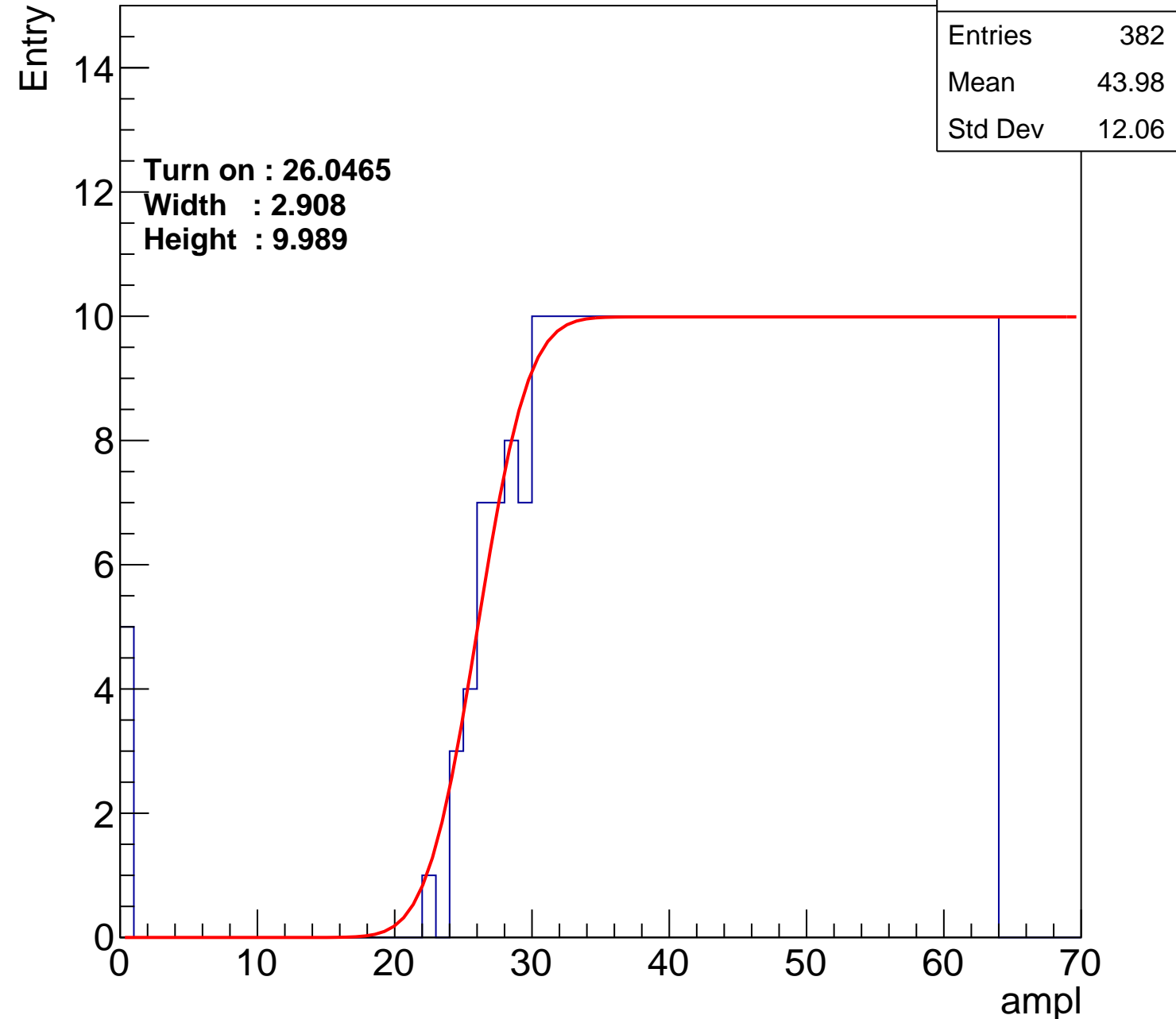
Width : 2.908

Height : 9.989

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch63

calib_packv5_042523_0143.root, FC#0, port D2

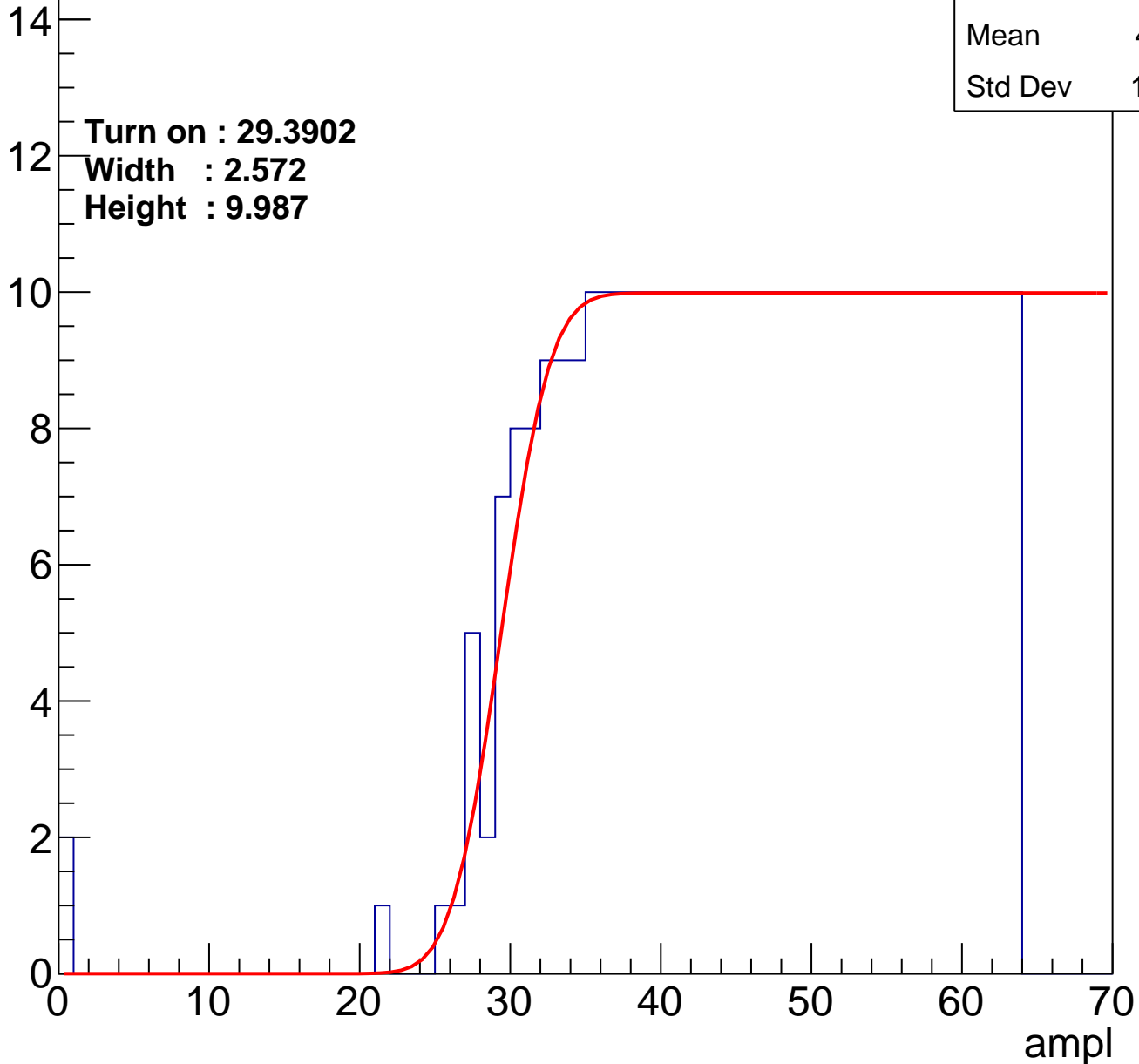
Entries	352
Mean	45.61
Std Dev	10.85

Turn on : 29.3902

Width : 2.572

Height : 9.987

Entry



B1L101S, U15-ch64

calib_packv5_042523_0143.root, FC#0, port D2

Entries	387
Mean	43.7
Std Dev	12.23

Turn on : 26.1149

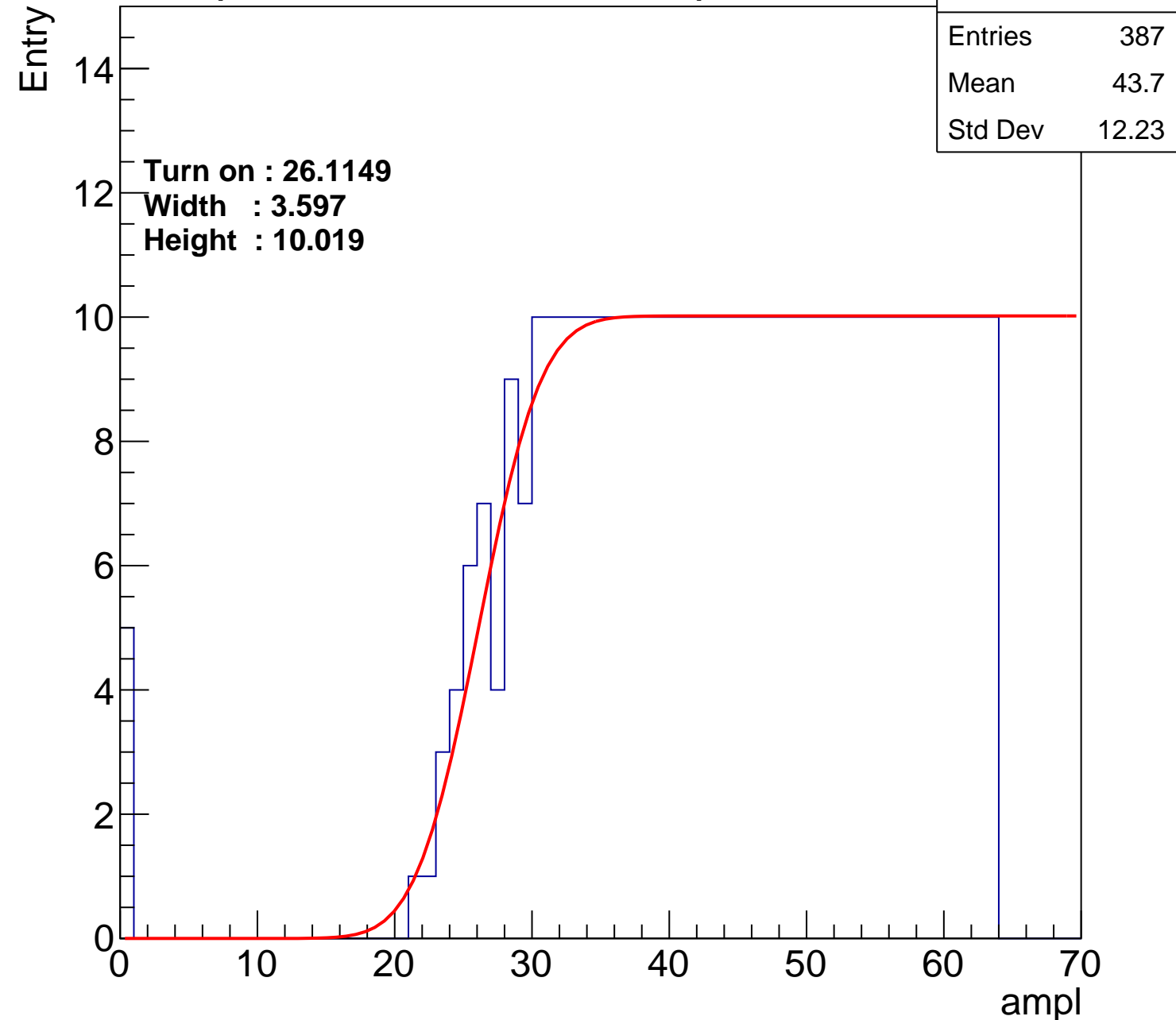
Width : 3.597

Height : 10.019

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch65

calib_packv5_042523_0143.root, FC#0, port D2

Entries	361
Mean	45.13
Std Dev	11.23

Turn on : 28.1393

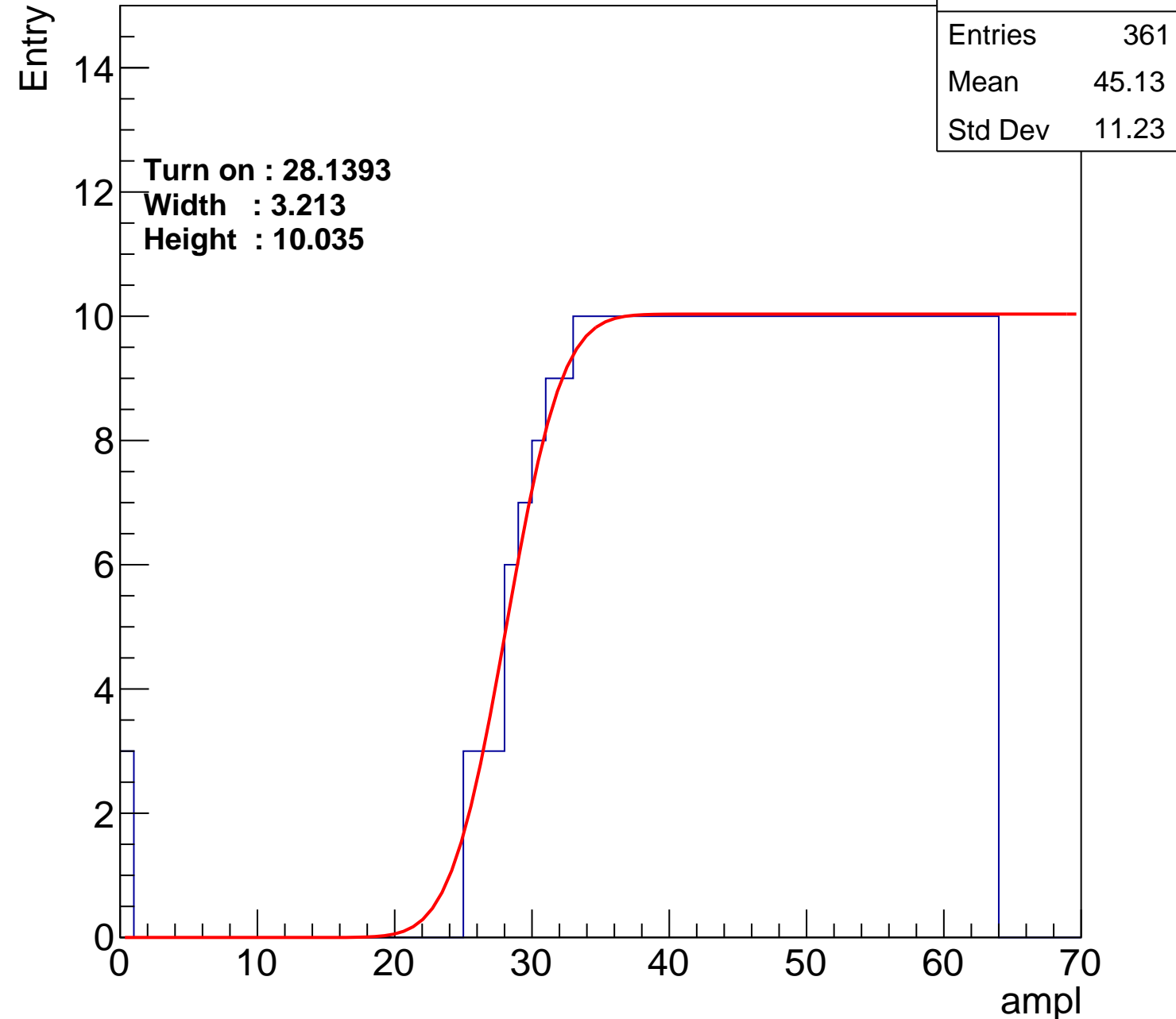
Width : 3.213

Height : 10.035

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch66

calib_packv5_042523_0143.root, FC#0, port D2

Entries	393
Mean	43.42
Std Dev	12.36

Turn on : 25.2475

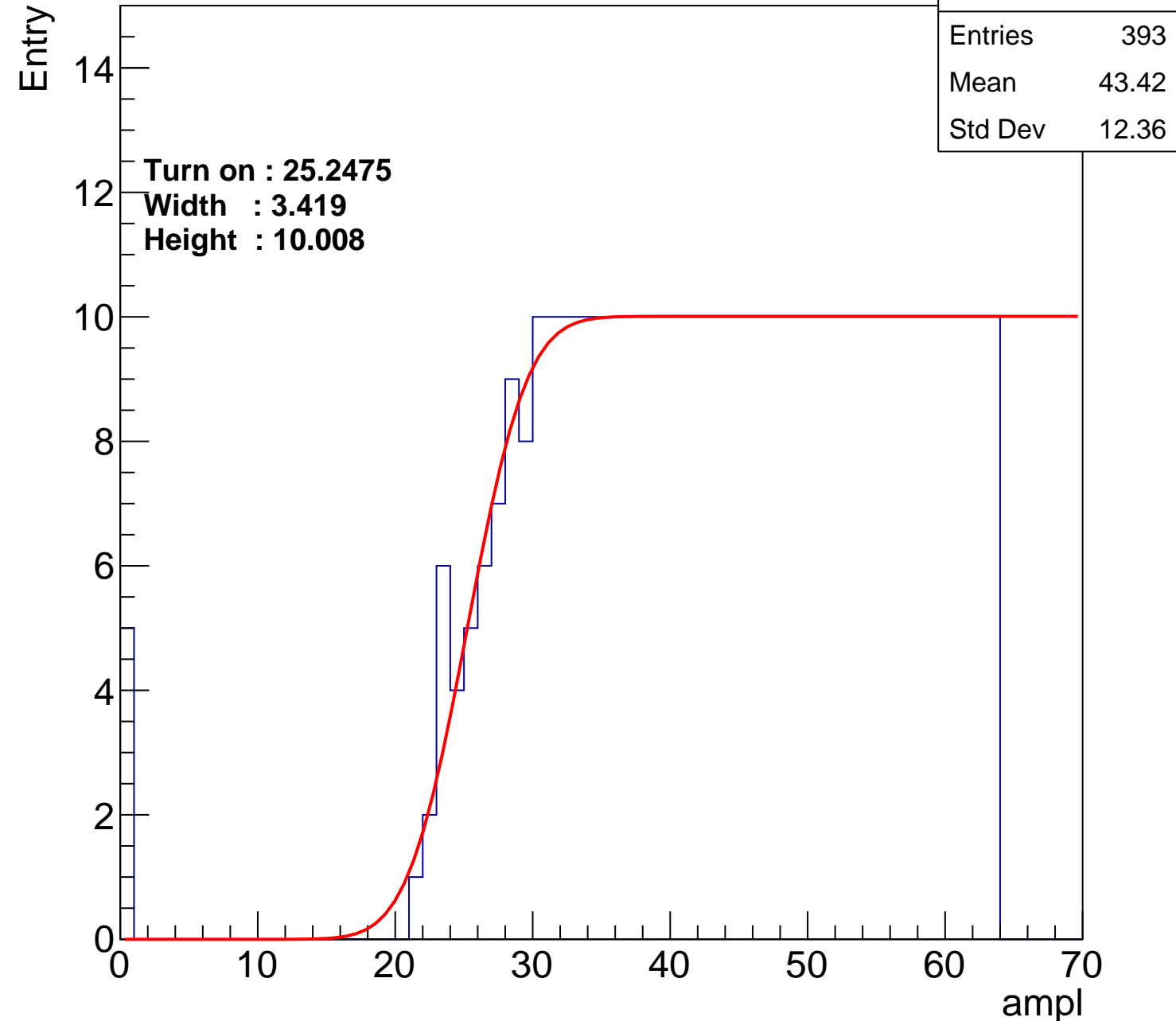
Width : 3.419

Height : 10.008

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch67

calib_packv5_042523_0143.root, FC#0, port D2

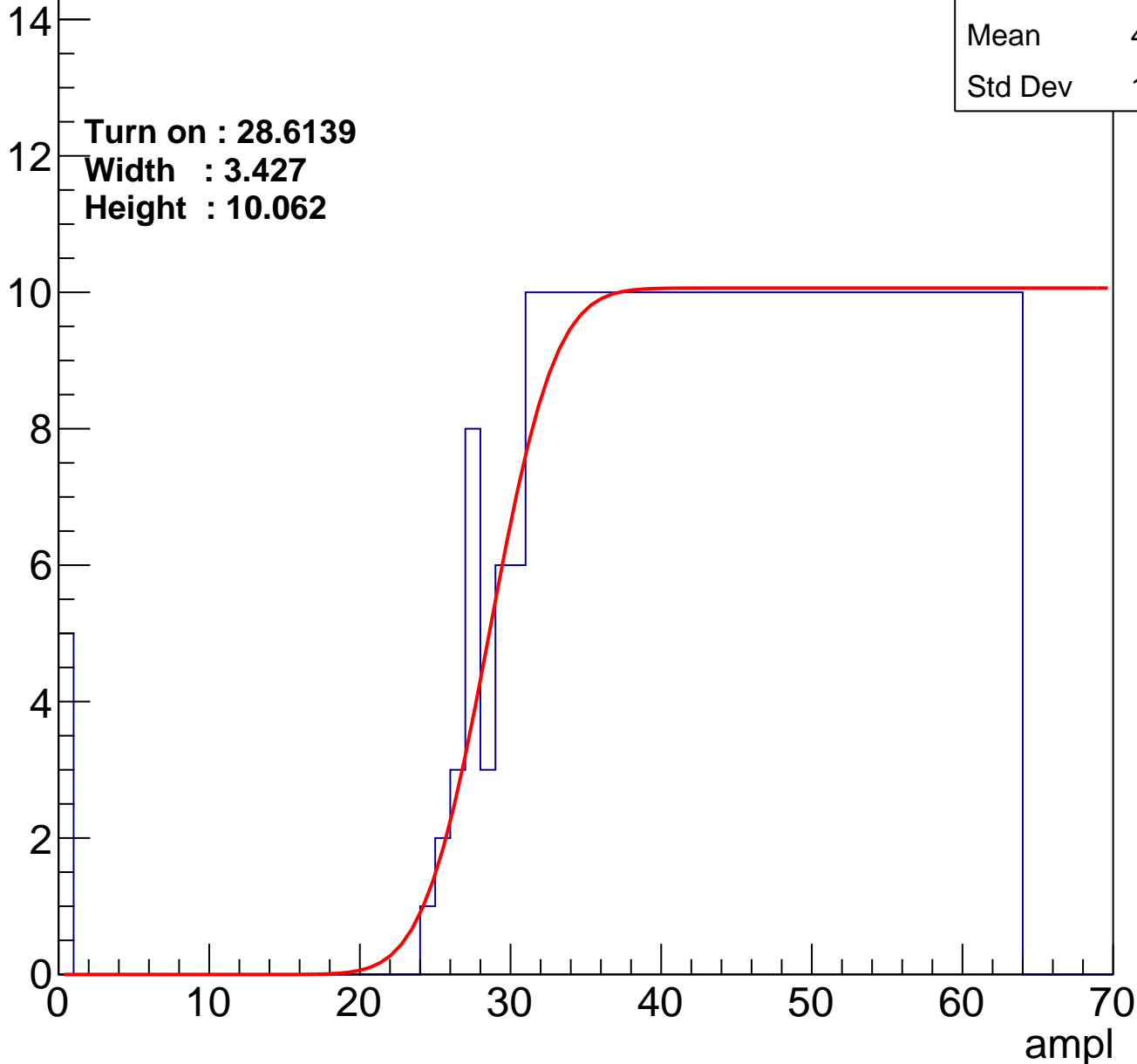
Entries	364
Mean	44.82
Std Dev	11.72

Turn on : 28.6139

Width : 3.427

Height : 10.062

Entry



B1L101S, U15-ch68

calib_packv5_042523_0143.root, FC#0, port D2

Entries	357
Mean	45.36
Std Dev	10.98

Turn on : 28.8718

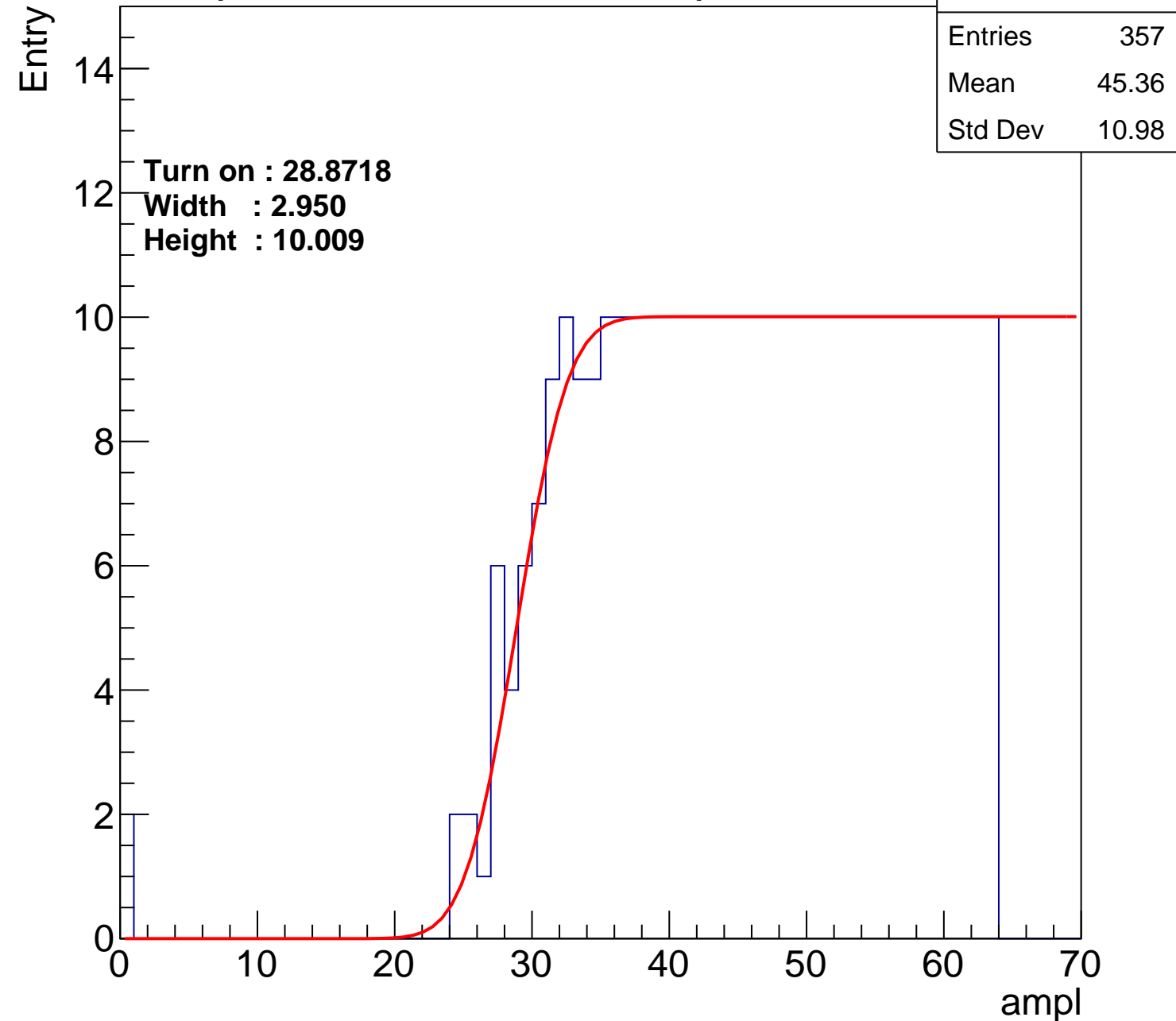
Width : 2.950

Height : 10.009

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch69

calib_packv5_042523_0143.root, FC#0, port D2

Entries	374
Mean	44.37
Std Dev	11.89

Turn on : 27.1728

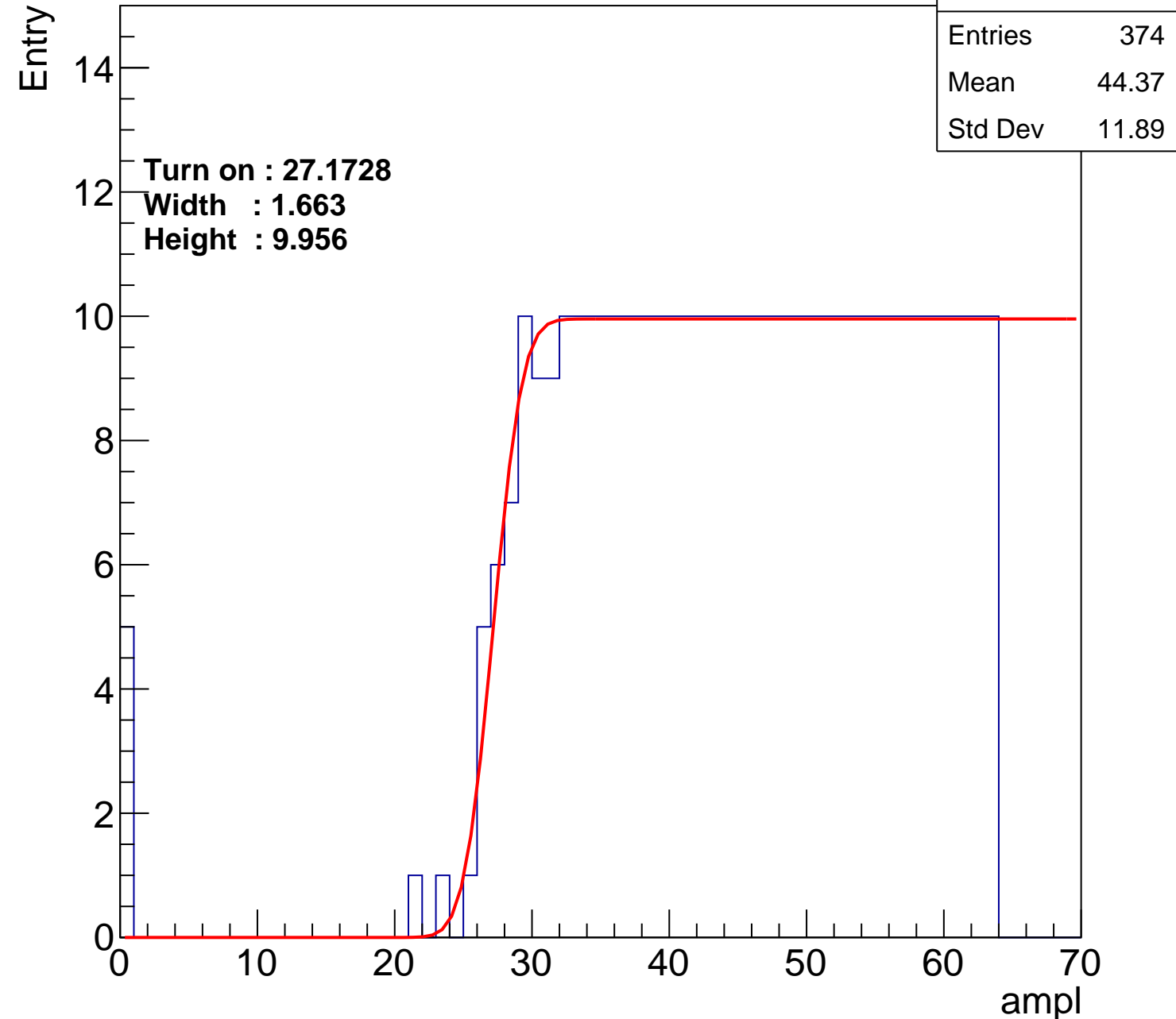
Width : 1.663

Height : 9.956

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch70

calib_packv5_042523_0143.root, FC#0, port D2

Entries	377
Mean	44.36
Std Dev	11.51

Turn on : 26.3234

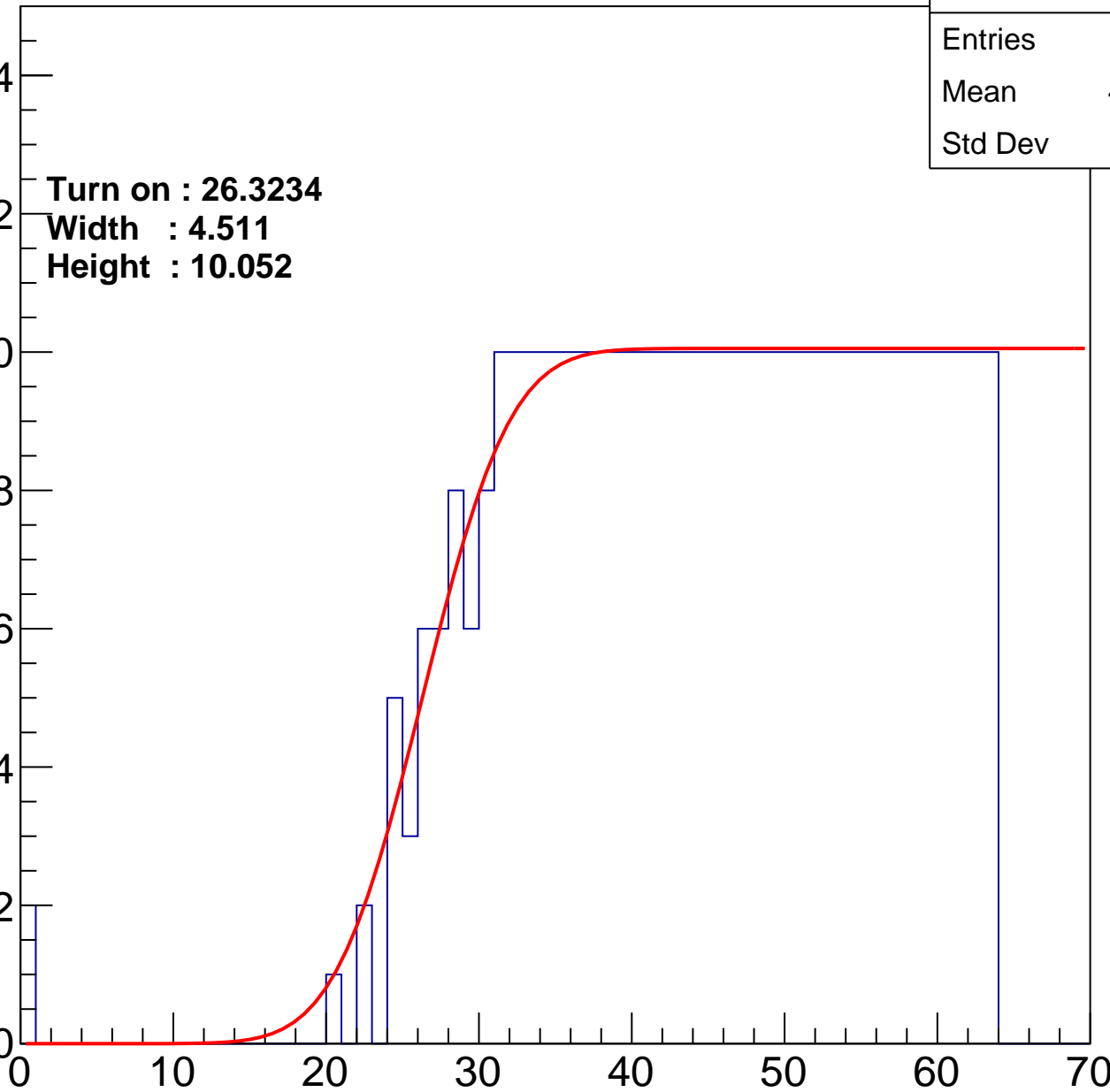
Width : 4.511

Height : 10.052

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch71

calib_packv5_042523_0143.root, FC#0, port D2

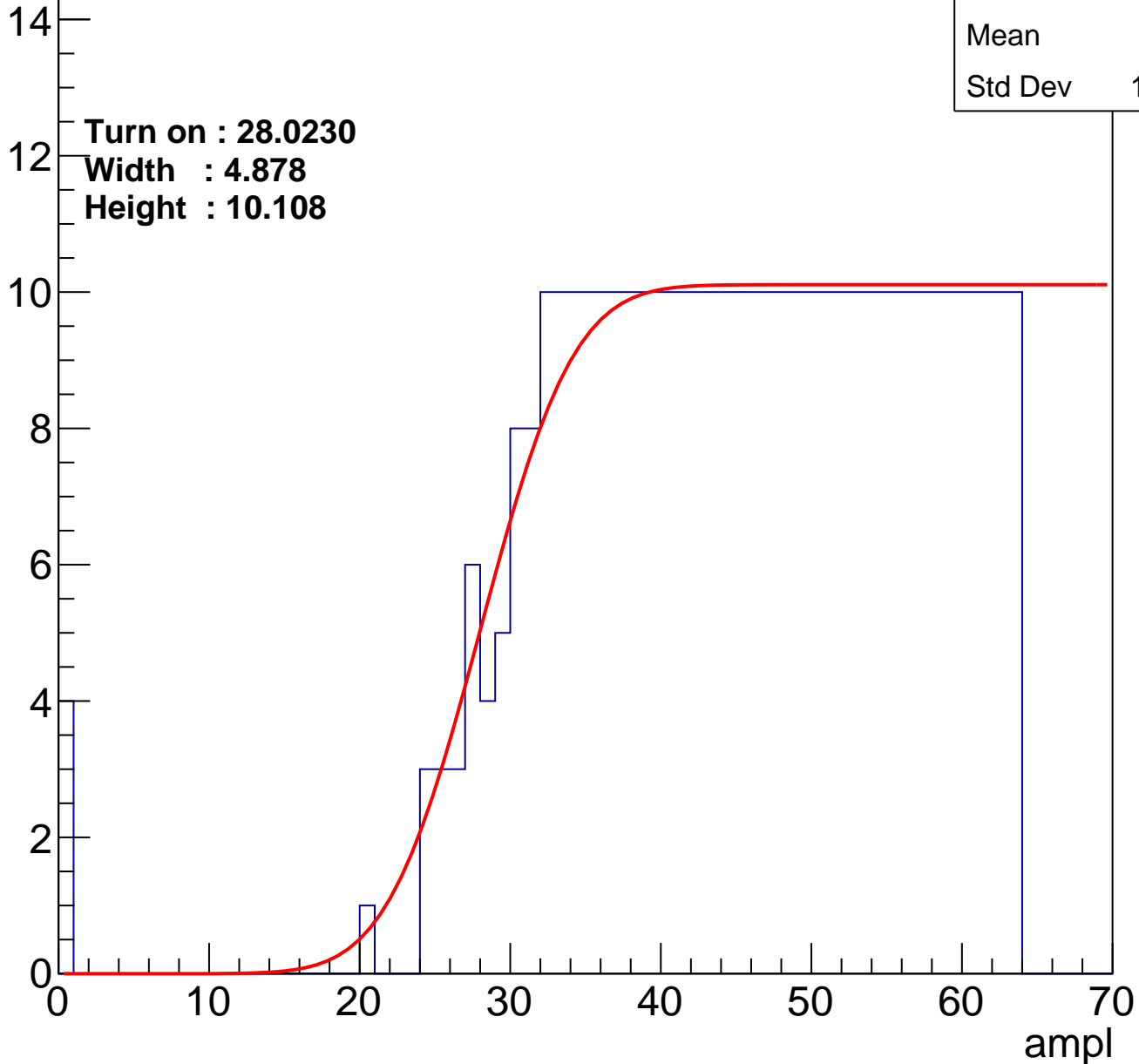
Entries	365
Mean	44.8
Std Dev	11.63

Turn on : 28.0230

Width : 4.878

Height : 10.108

Entry



B1L101S, U15-ch72

calib_packv5_042523_0143.root, FC#0, port D2

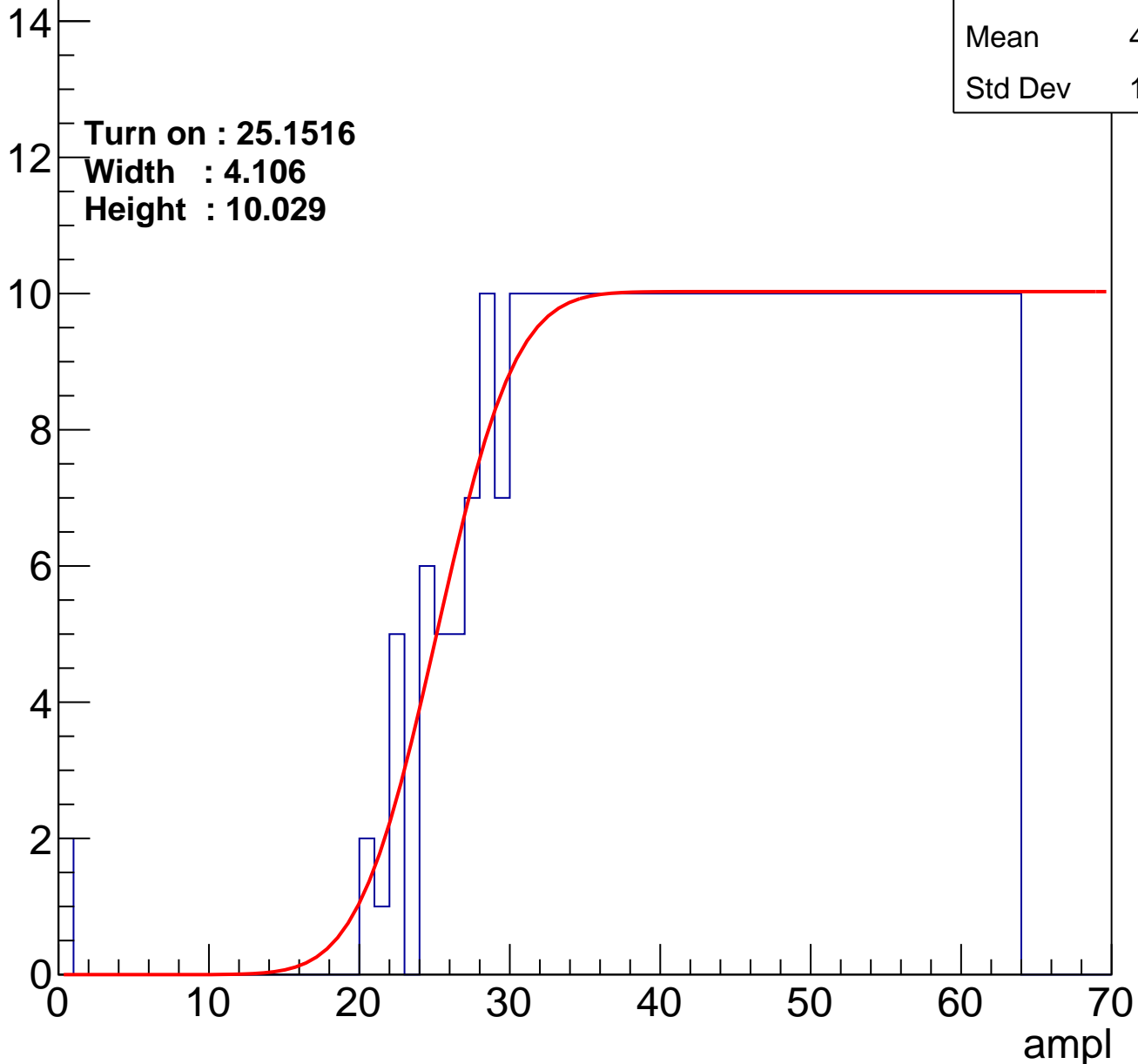
Entries	390
Mean	43.72
Std Dev	11.85

Turn on : 25.1516

Width : 4.106

Height : 10.029

Entry



B1L101S, U15-ch73

calib_packv5_042523_0143.root, FC#0, port D2

Entries	379
Mean	44.16
Std Dev	11.89

Turn on : 26.7765

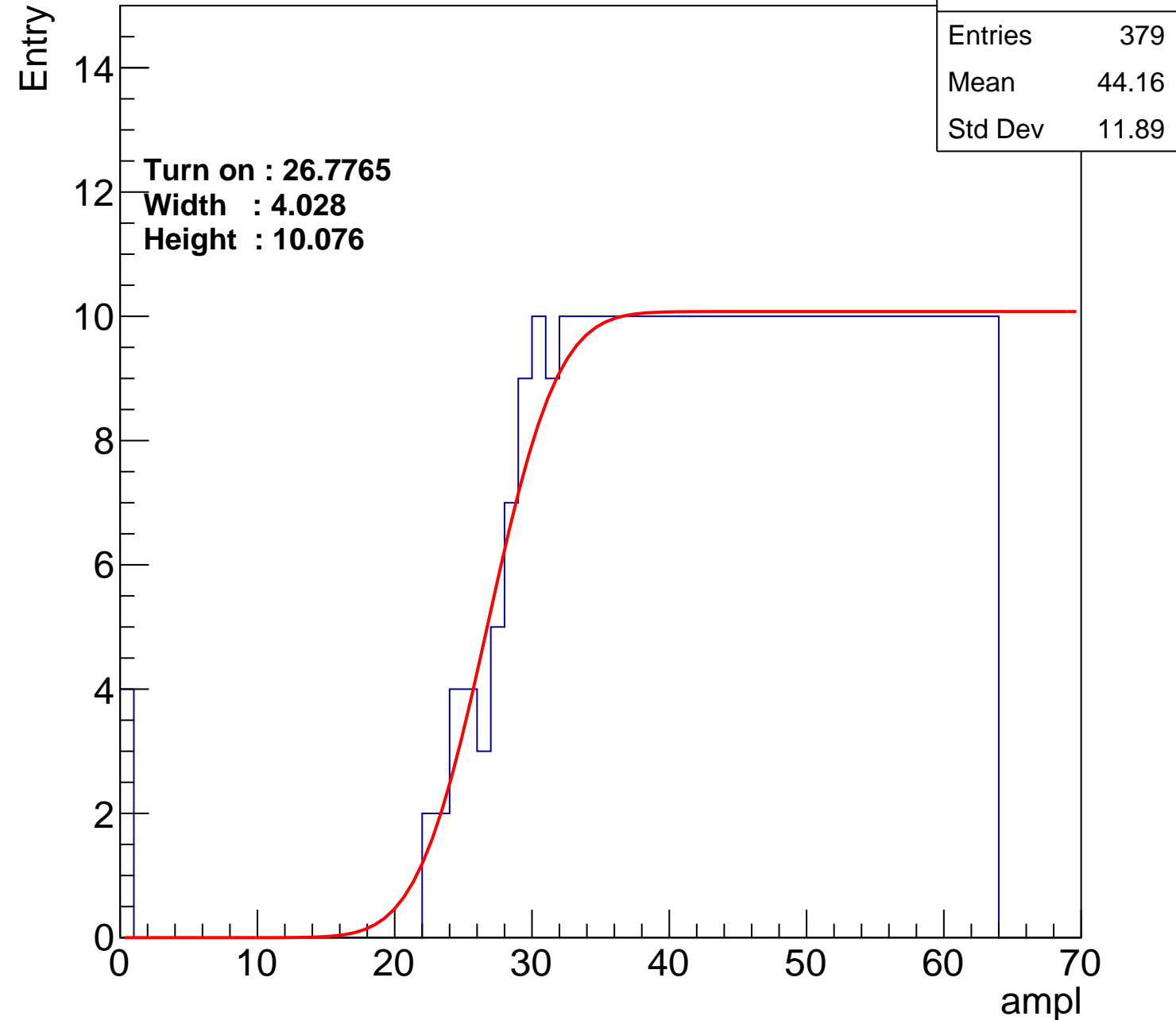
Width : 4.028

Height : 10.076

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch74

calib_packv5_042523_0143.root, FC#0, port D2

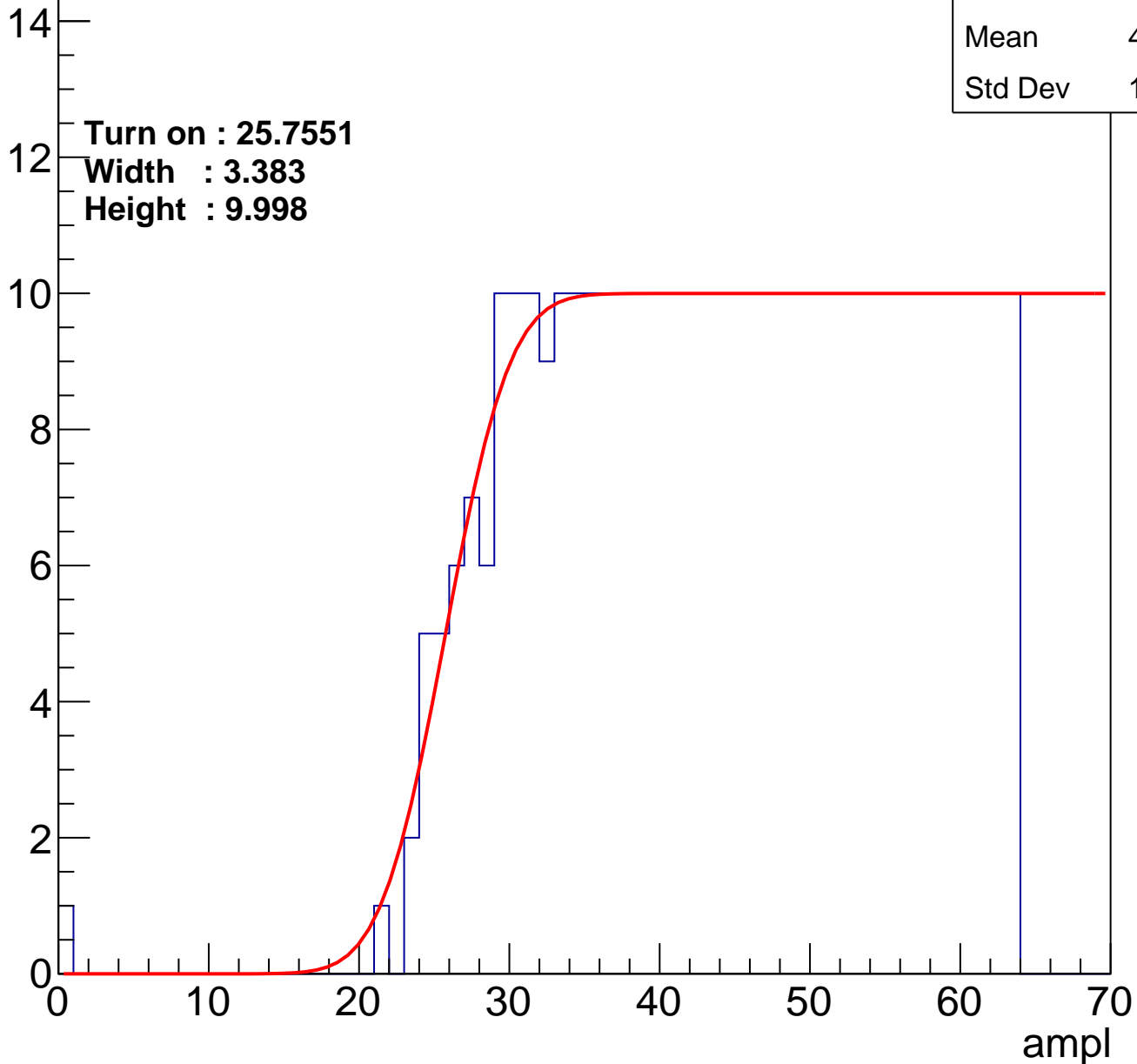
Entries	382
Mean	44.22
Std Dev	11.39

Turn on : 25.7551

Width : 3.383

Height : 9.998

Entry



B1L101S, U15-ch75

calib_packv5_042523_0143.root, FC#0, port D2

Entries	374
Mean	44.65
Std Dev	11.14

Turn on : 27.1361

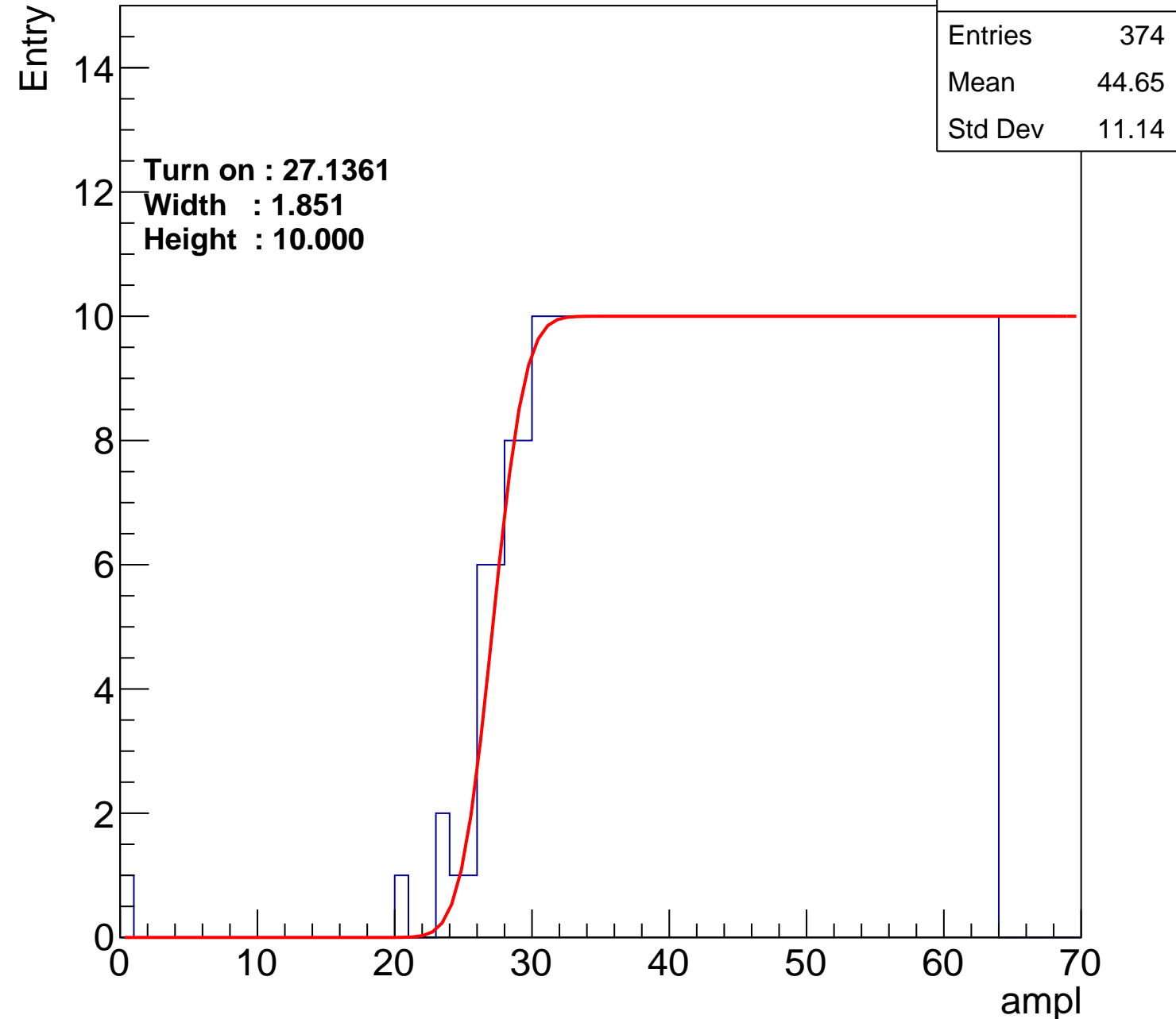
Width : 1.851

Height : 10.000

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch76

calib_packv5_042523_0143.root, FC#0, port D2

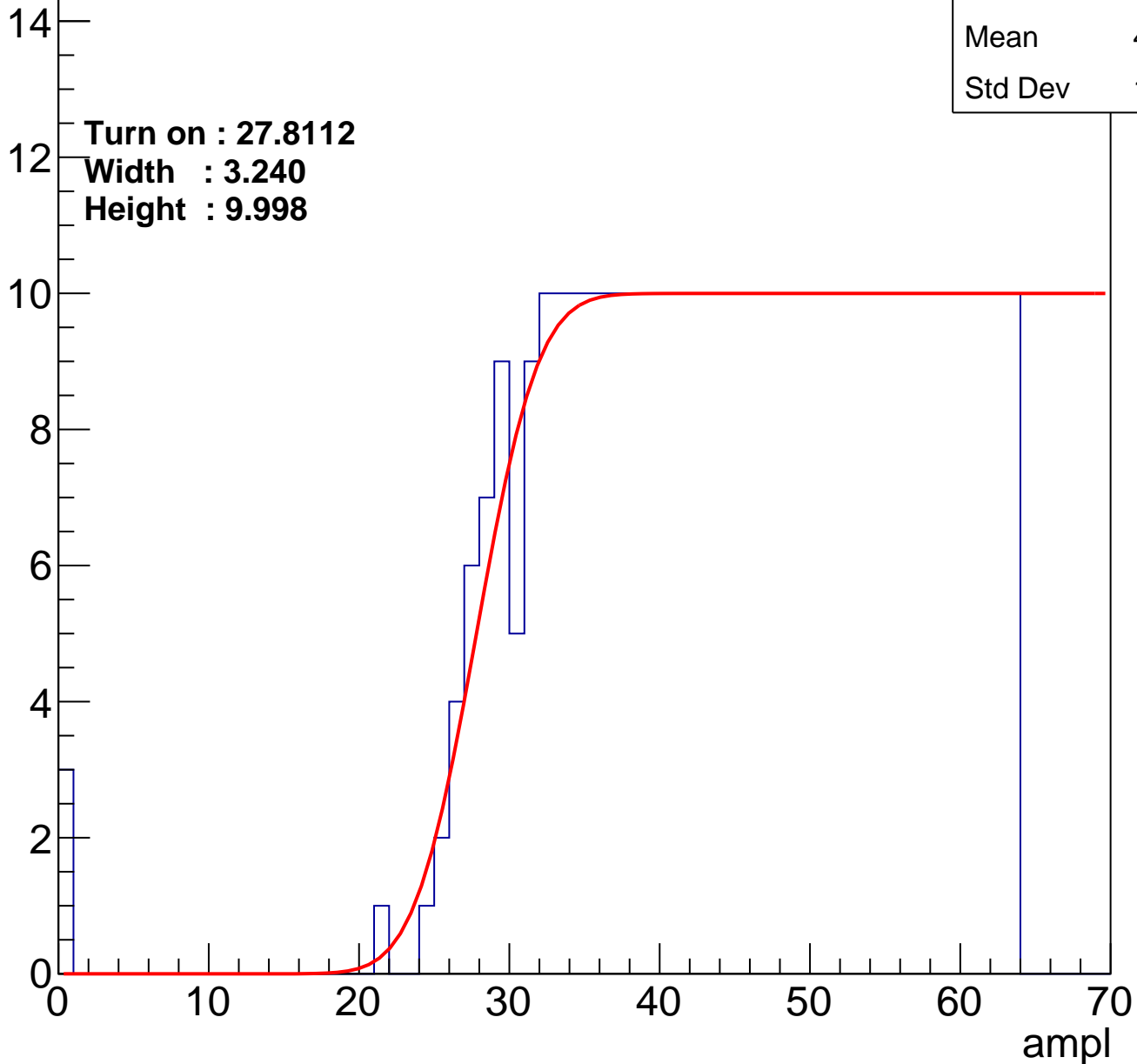
Entries	367
Mean	44.81
Std Dev	11.41

Turn on : 27.8112

Width : 3.240

Height : 9.998

Entry



B1L101S, U15-ch77

calib_packv5_042523_0143.root, FC#0, port D2

Entries	371
Mean	44.57
Std Dev	11.58

Turn on : 27.5738

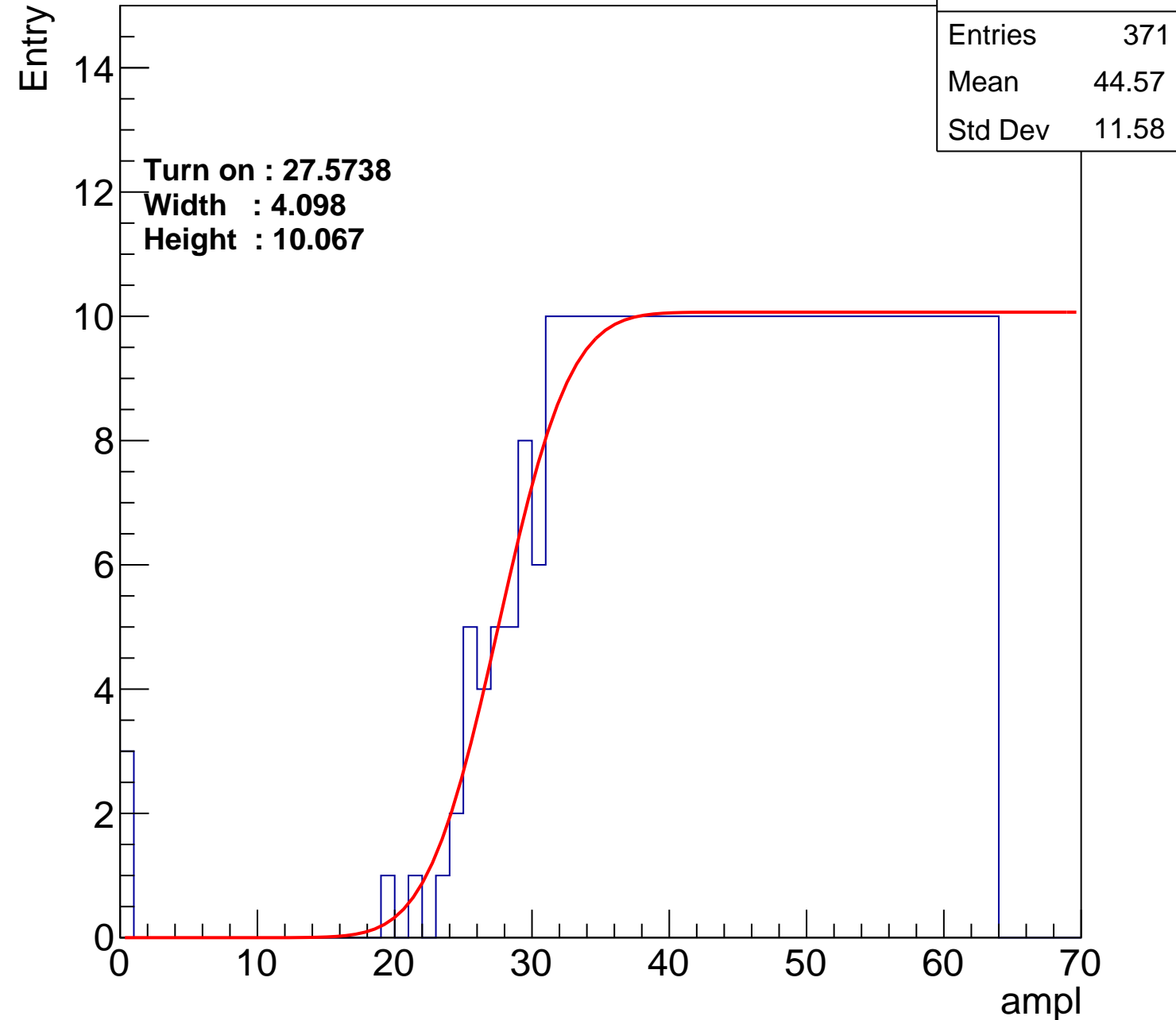
Width : 4.098

Height : 10.067

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch78

calib_packv5_042523_0143.root, FC#0, port D2

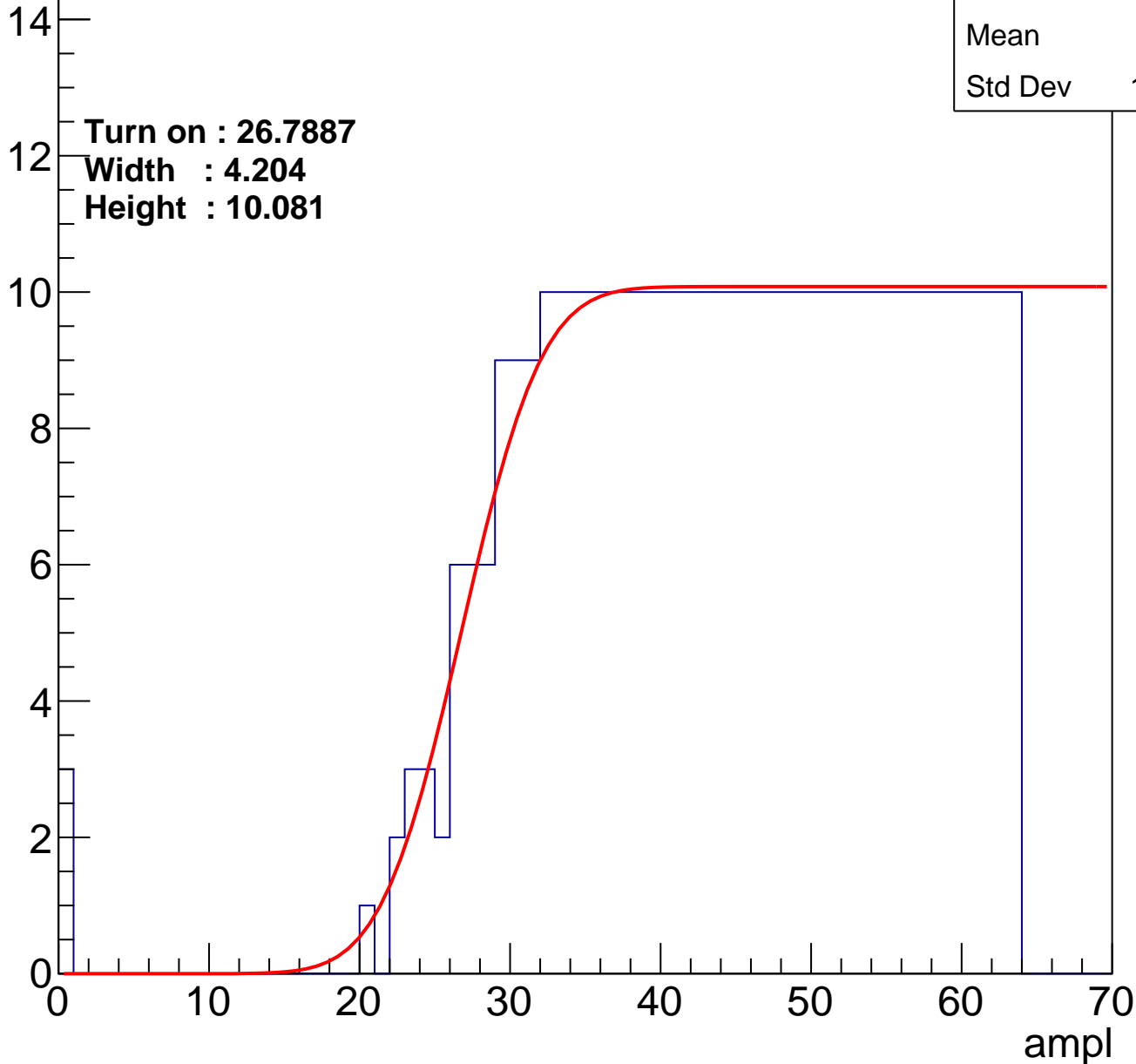
Entries	379
Mean	44.2
Std Dev	11.75

Turn on : 26.7887

Width : 4.204

Height : 10.081

Entry



B1L101S, U15-ch79

calib_packv5_042523_0143.root, FC#0, port D2

Entries	364
Mean	44.94
Std Dev	11.38

Turn on : 28.1979

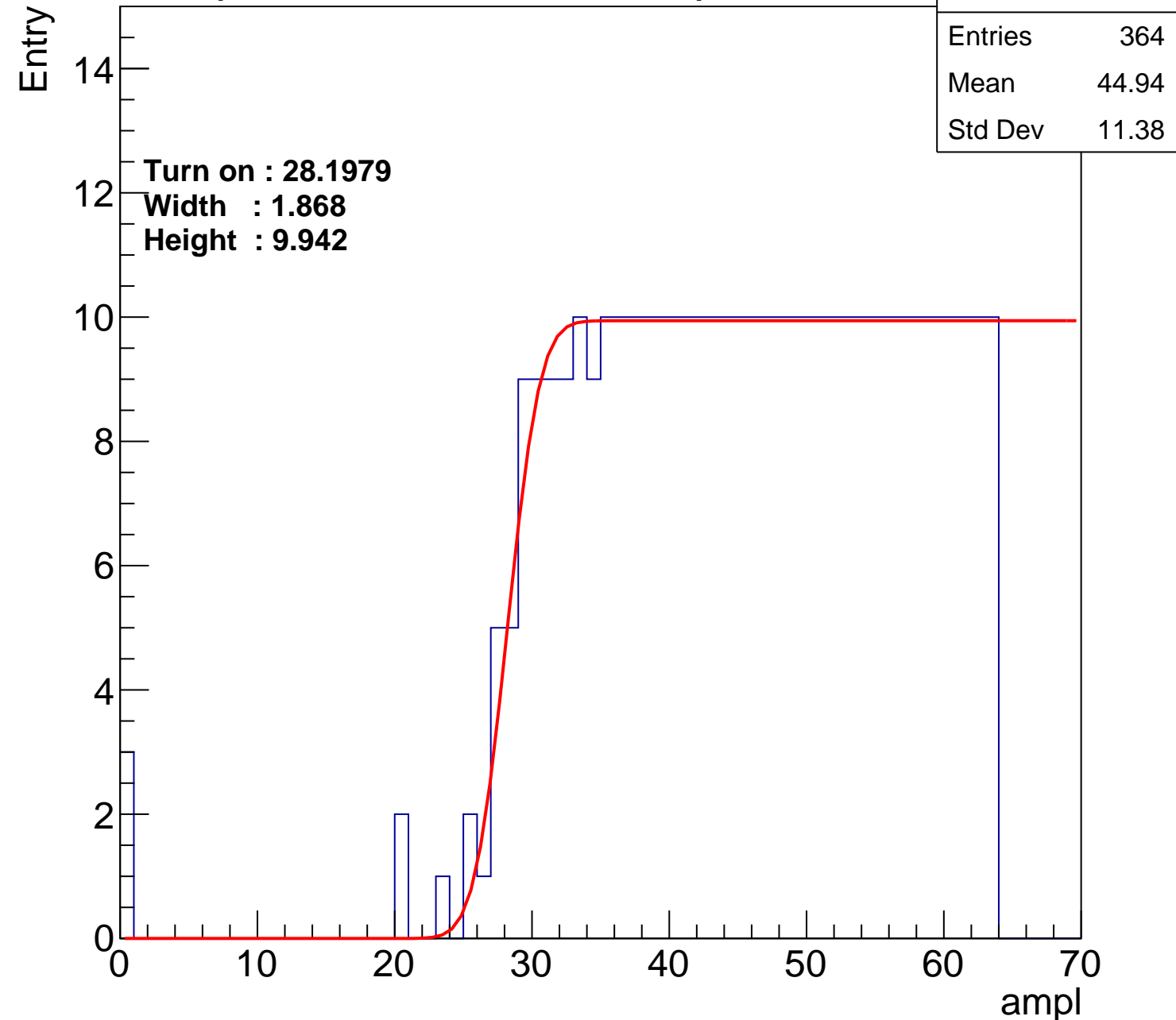
Width : 1.868

Height : 9.942

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch80

calib_packv5_042523_0143.root, FC#0, port D2

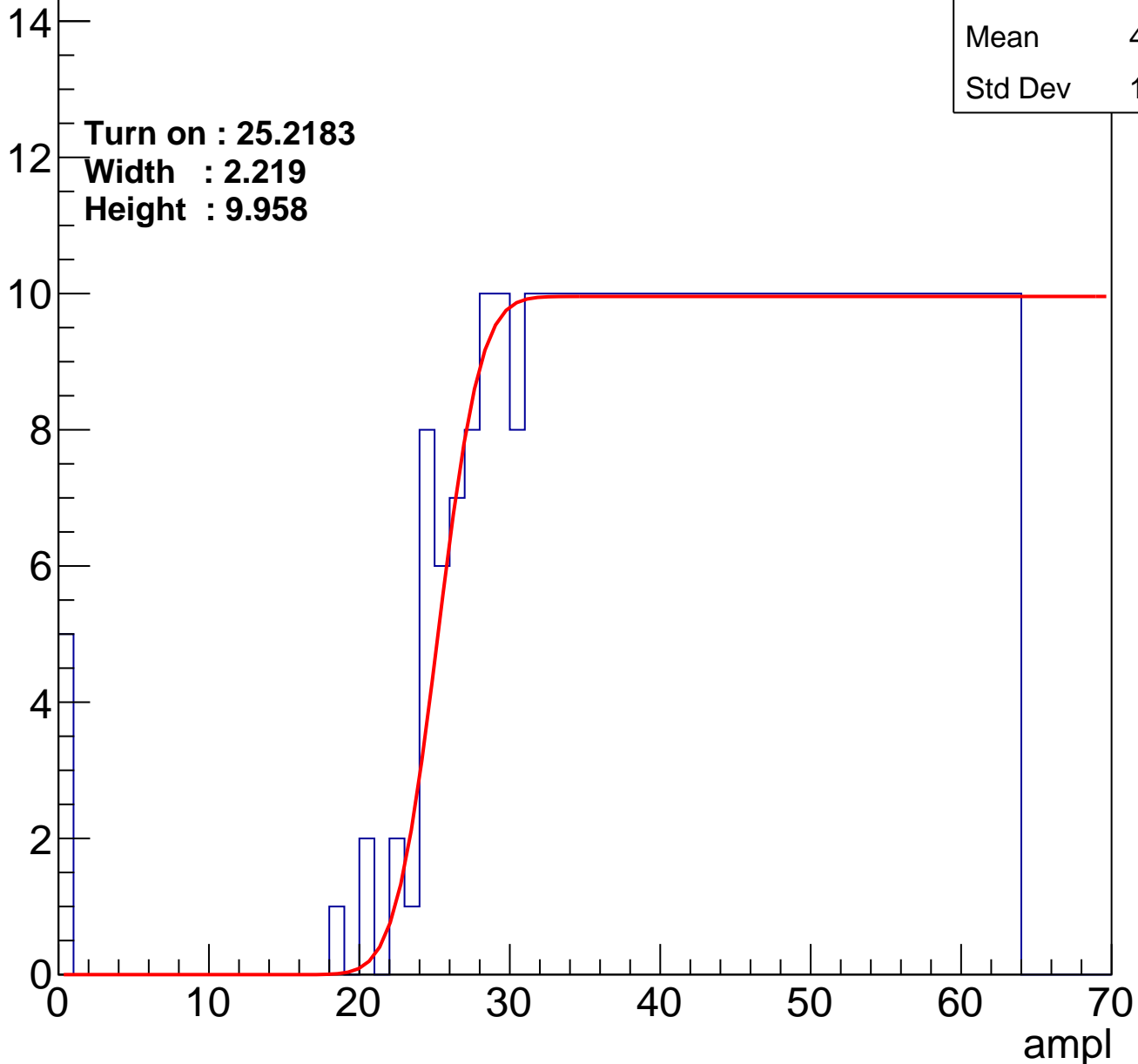
Entries	398
Mean	43.18
Std Dev	12.47

Turn on : 25.2183

Width : 2.219

Height : 9.958

Entry



B1L101S, U15-ch81

calib_packv5_042523_0143.root, FC#0, port D2

Entries	375
Mean	44.35
Std Dev	11.79

Turn on : 26.9749

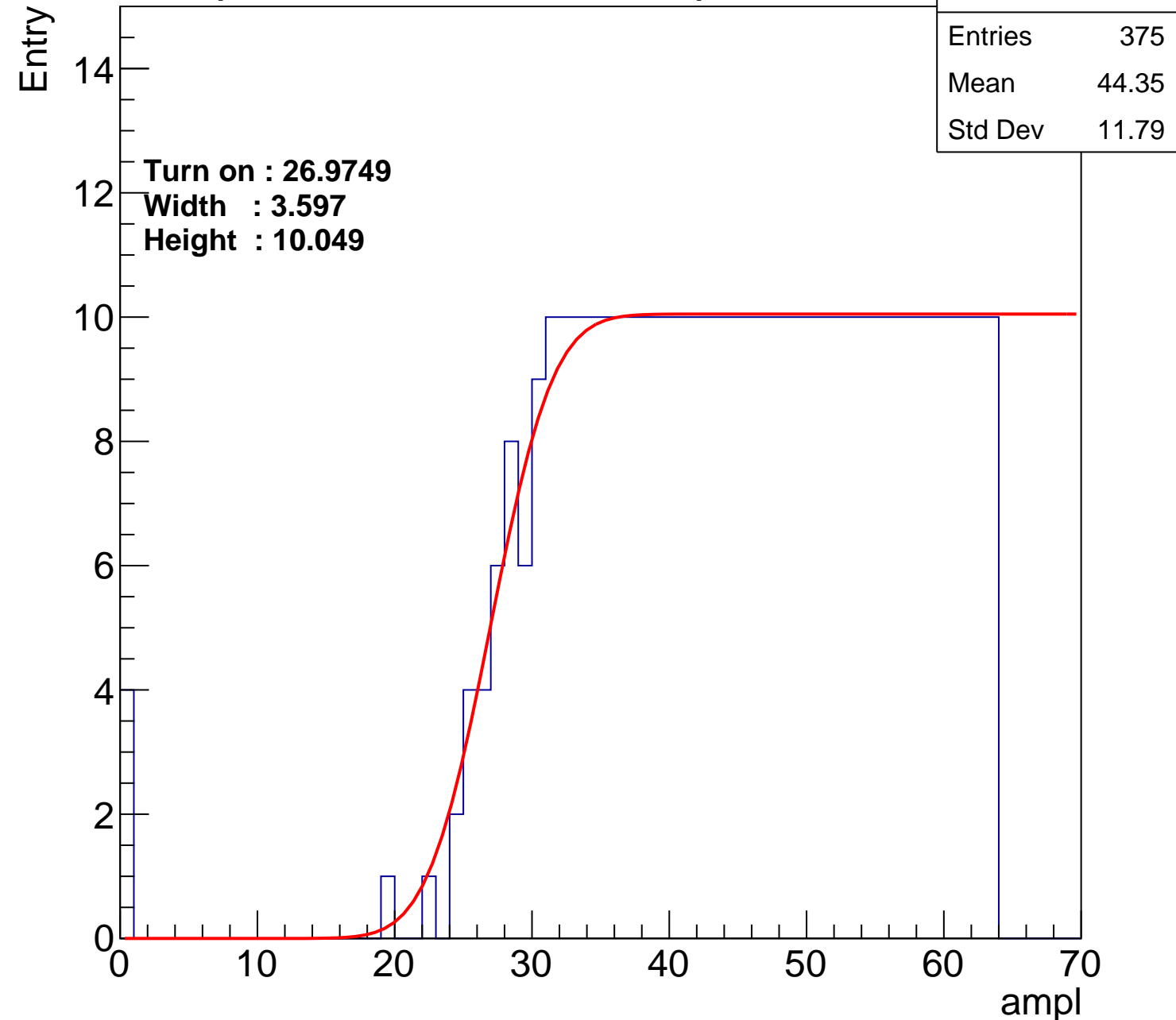
Width : 3.597

Height : 10.049

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch82

calib_packv5_042523_0143.root, FC#0, port D2

Entries	389
Mean	43.81
Std Dev	11.76

Turn on : 25.3070

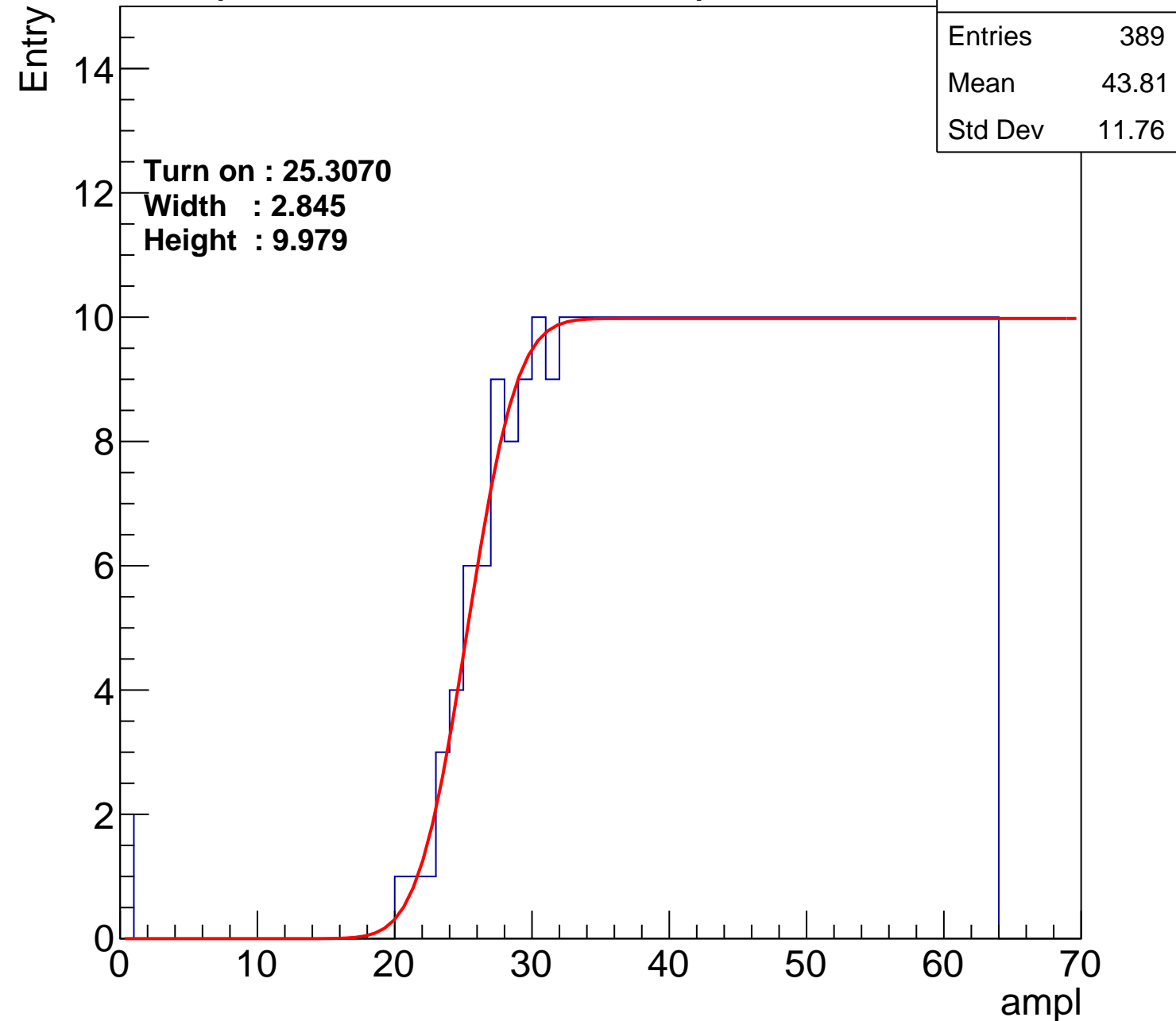
Width : 2.845

Height : 9.979

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch83

calib_packv5_042523_0143.root, FC#0, port D2

Entries	372
Mean	44.52
Std Dev	11.7

Turn on : 27.1784

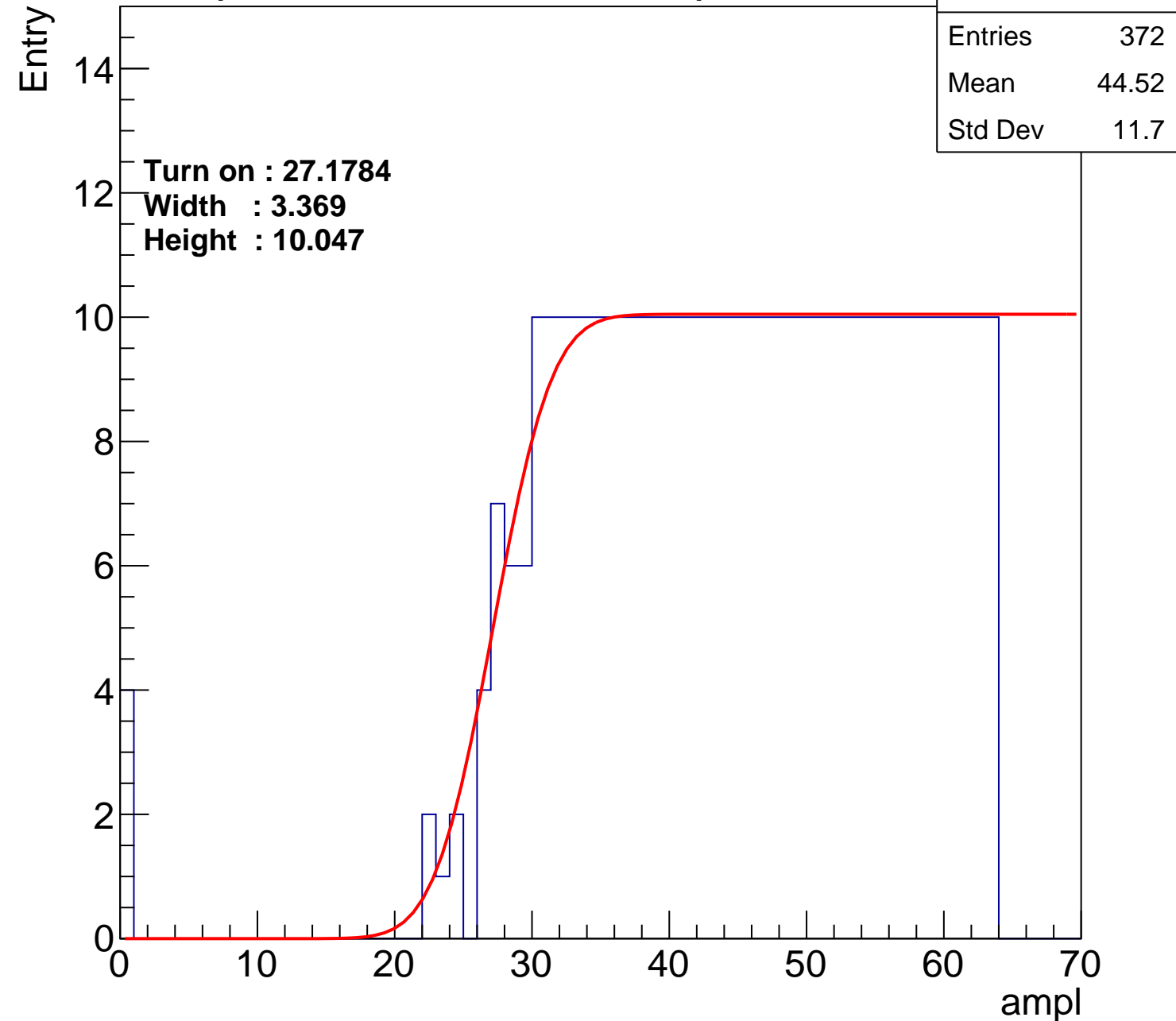
Width : 3.369

Height : 10.047

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch84

calib_packv5_042523_0143.root, FC#0, port D2

Entries	375
Mean	44.47
Std Dev	11.44

Turn on : 27.0788

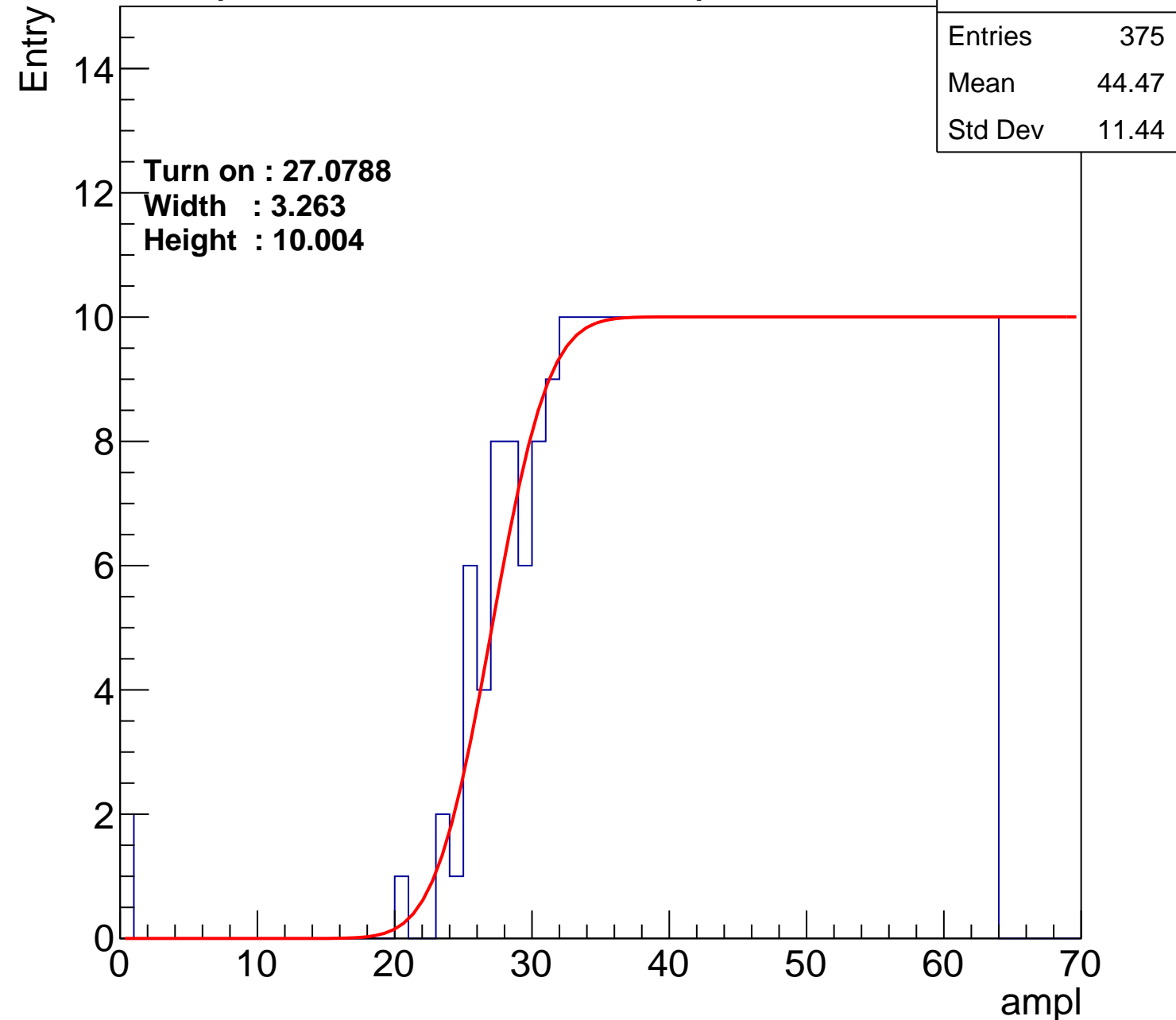
Width : 3.263

Height : 10.004

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch85

calib_packv5_042523_0143.root, FC#0, port D2

Entries	361
Mean	45.18
Std Dev	11.05

Turn on : 28.2083

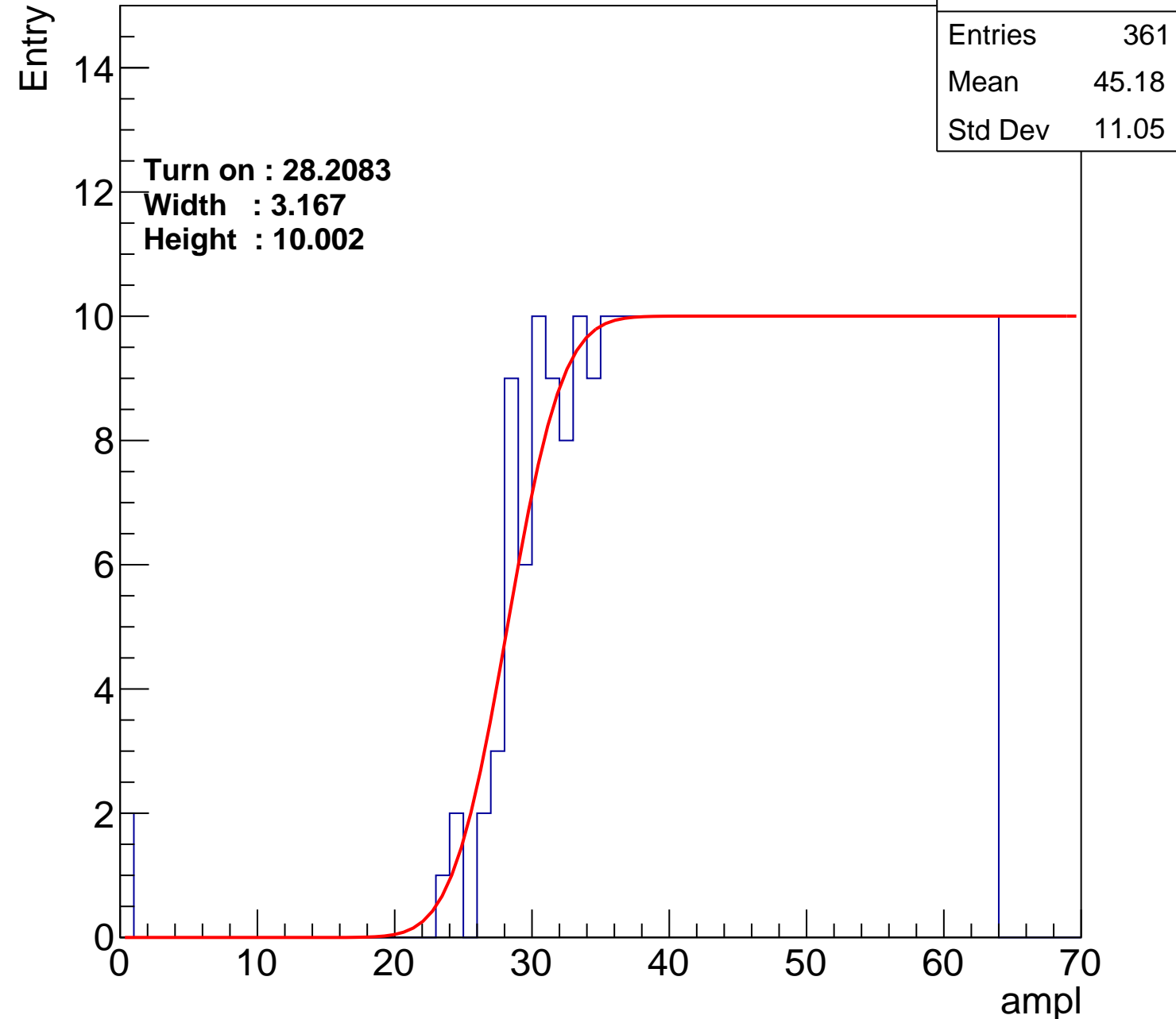
Width : 3.167

Height : 10.002

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch86

calib_packv5_042523_0143.root, FC#0, port D2

Entries	378
Mean	44.33
Std Dev	11.52

Turn on : 26.7800

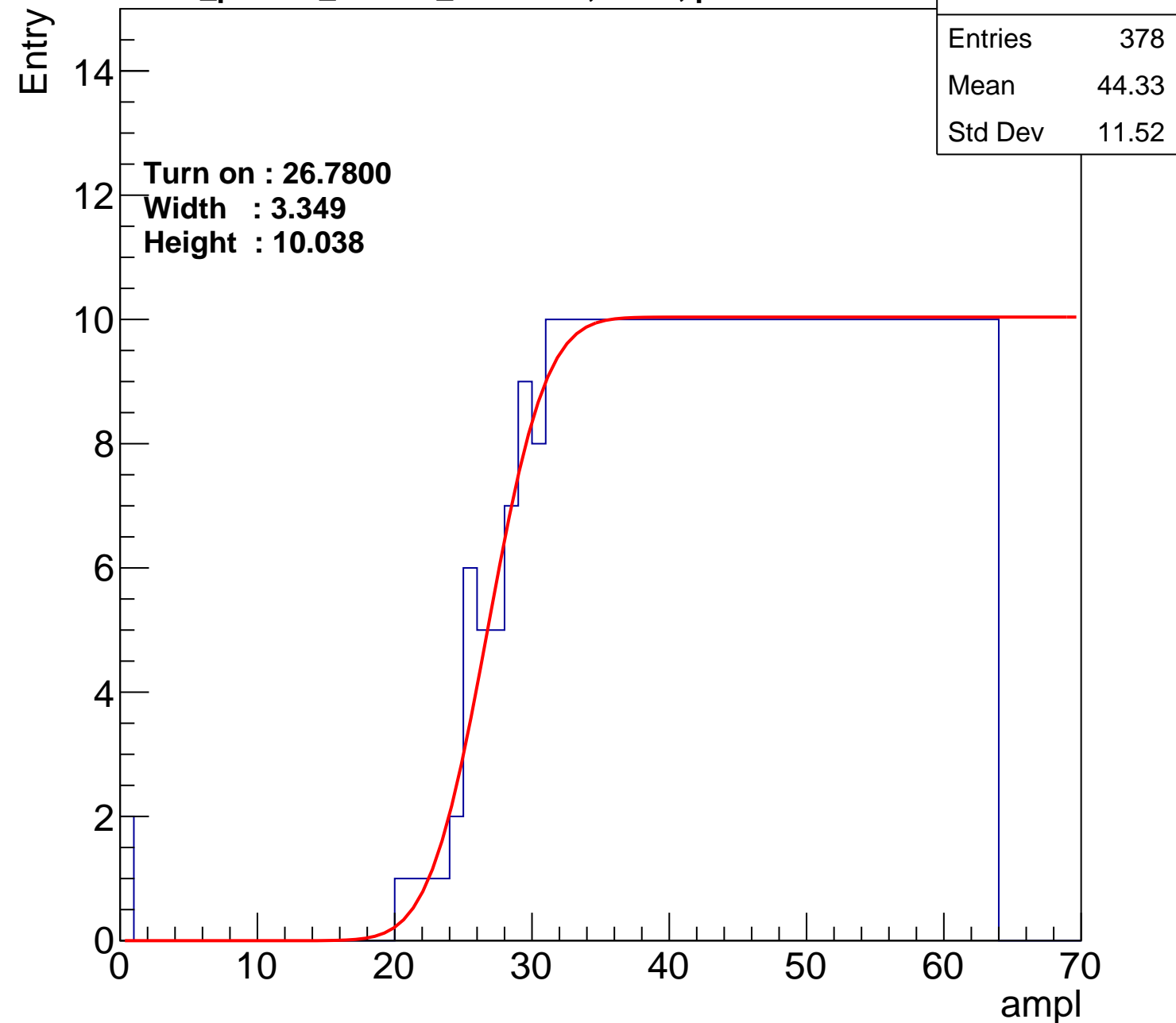
Width : 3.349

Height : 10.038

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch87

calib_packv5_042523_0143.root, FC#0, port D2

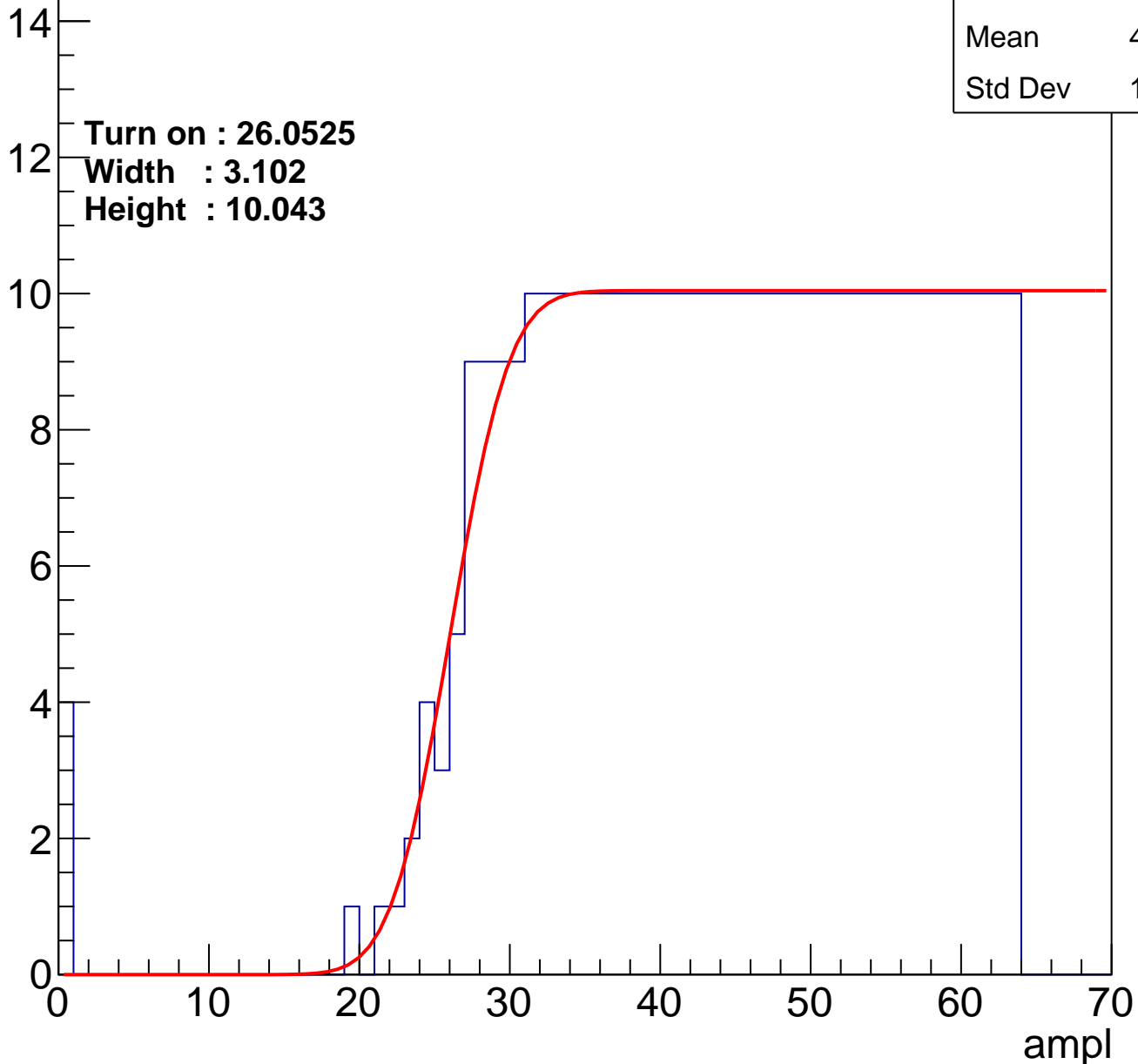
Entries	387
Mean	43.79
Std Dev	12.04

Turn on : 26.0525

Width : 3.102

Height : 10.043

Entry



B1L101S, U15-ch88

calib_packv5_042523_0143.root, FC#0, port D2

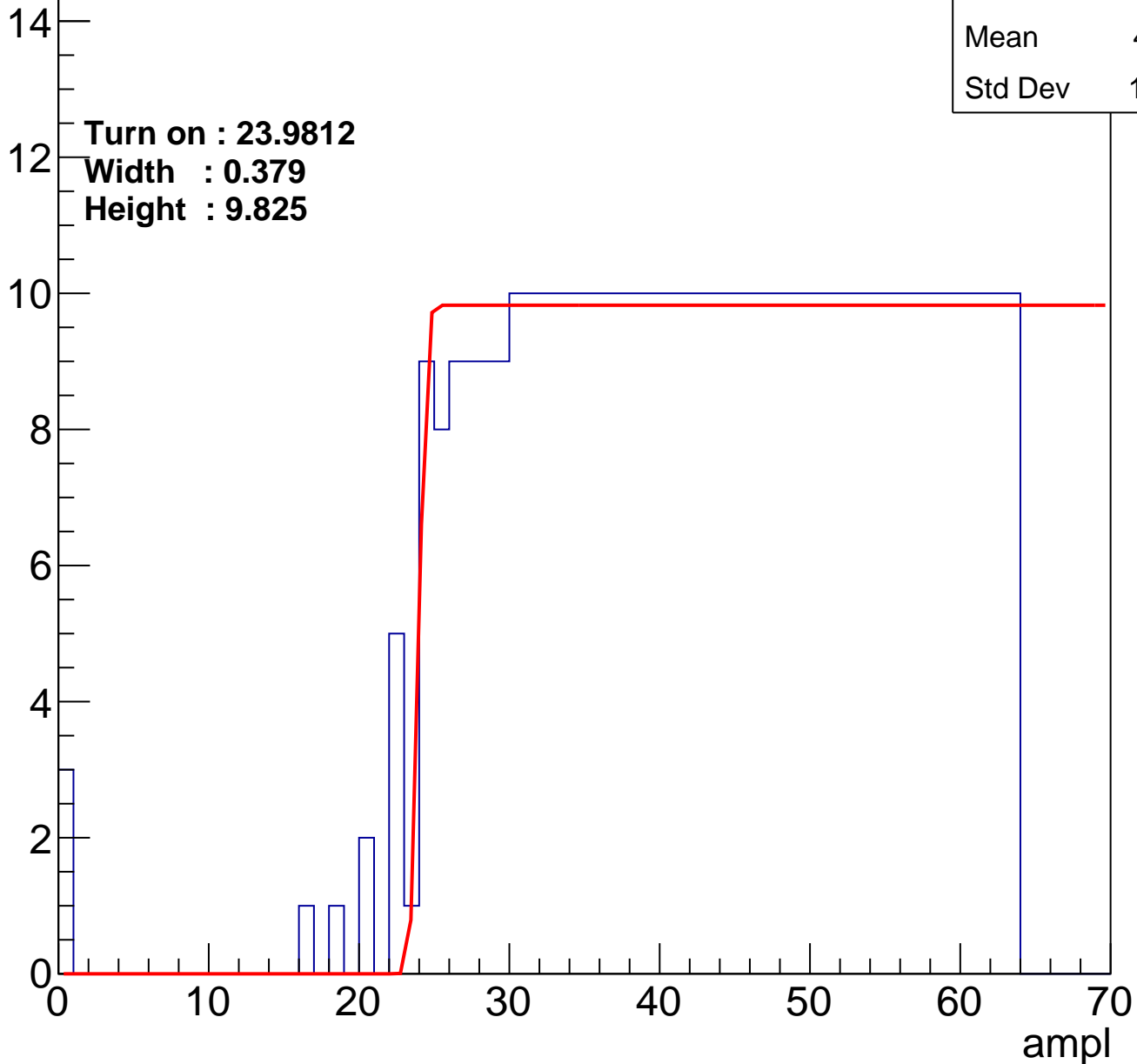
Entry

Entries	406
Mean	42.91
Std Dev	12.36

Turn on : 23.9812

Width : 0.379

Height : 9.825



B1L101S, U15-ch89

calib_packv5_042523_0143.root, FC#0, port D2

Entries	368
Mean	44.81
Std Dev	11.28

Turn on : 28.0340

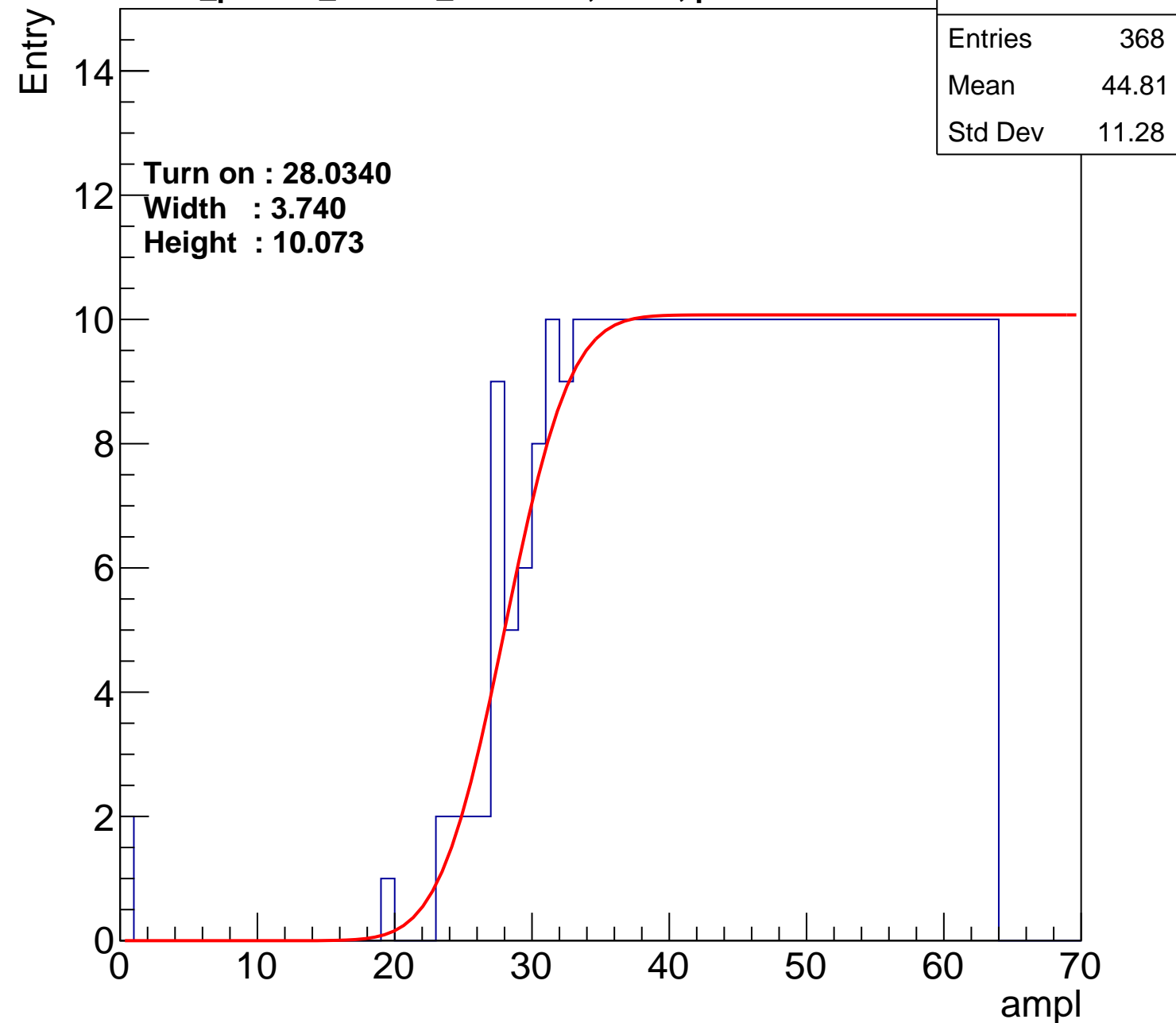
Width : 3.740

Height : 10.073

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch90

calib_packv5_042523_0143.root, FC#0, port D2

Entries	378
Mean	44.1
Std Dev	12.25

Turn on : 26.9474

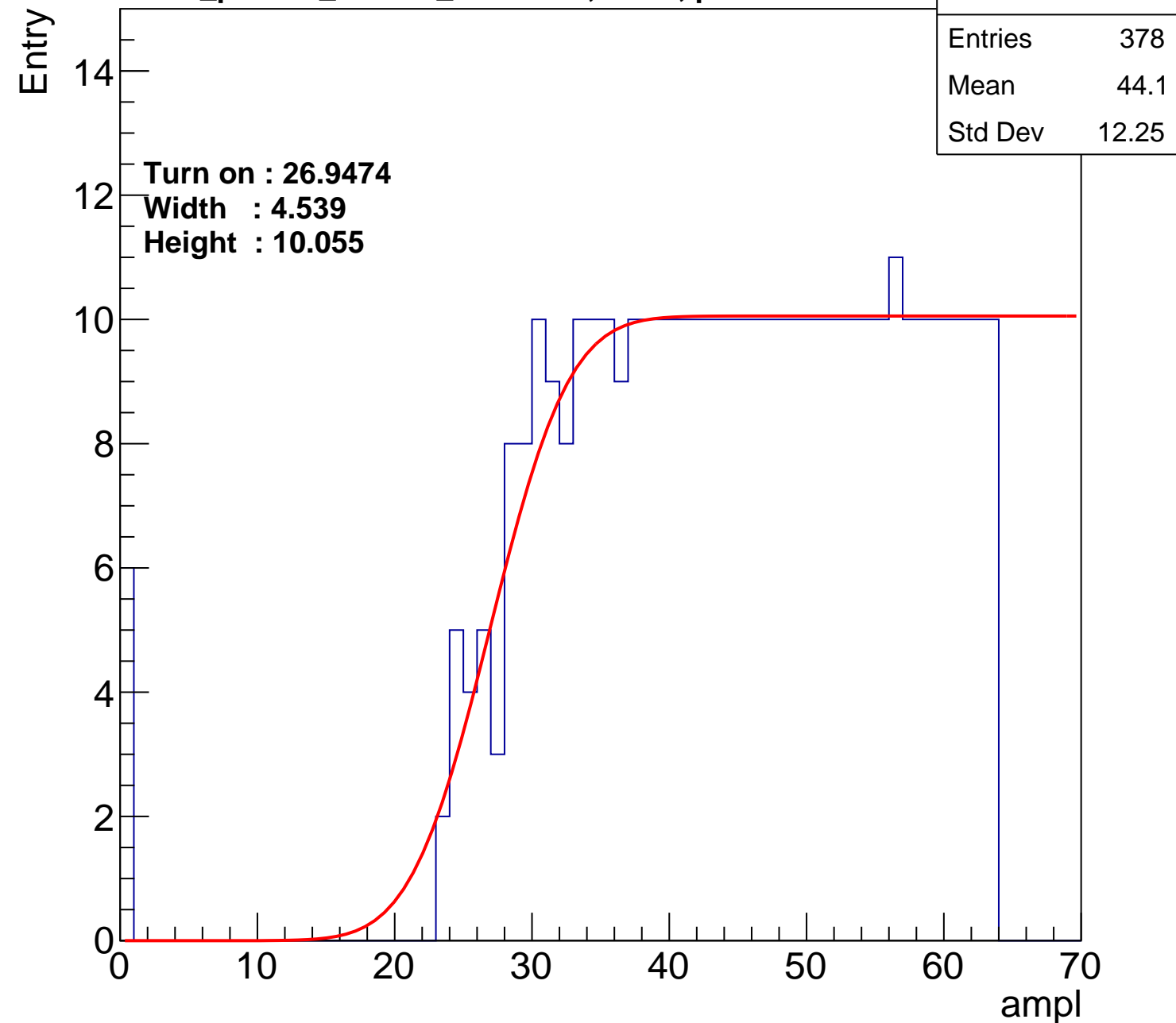
Width : 4.539

Height : 10.055

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch91

calib_packv5_042523_0143.root, FC#0, port D2

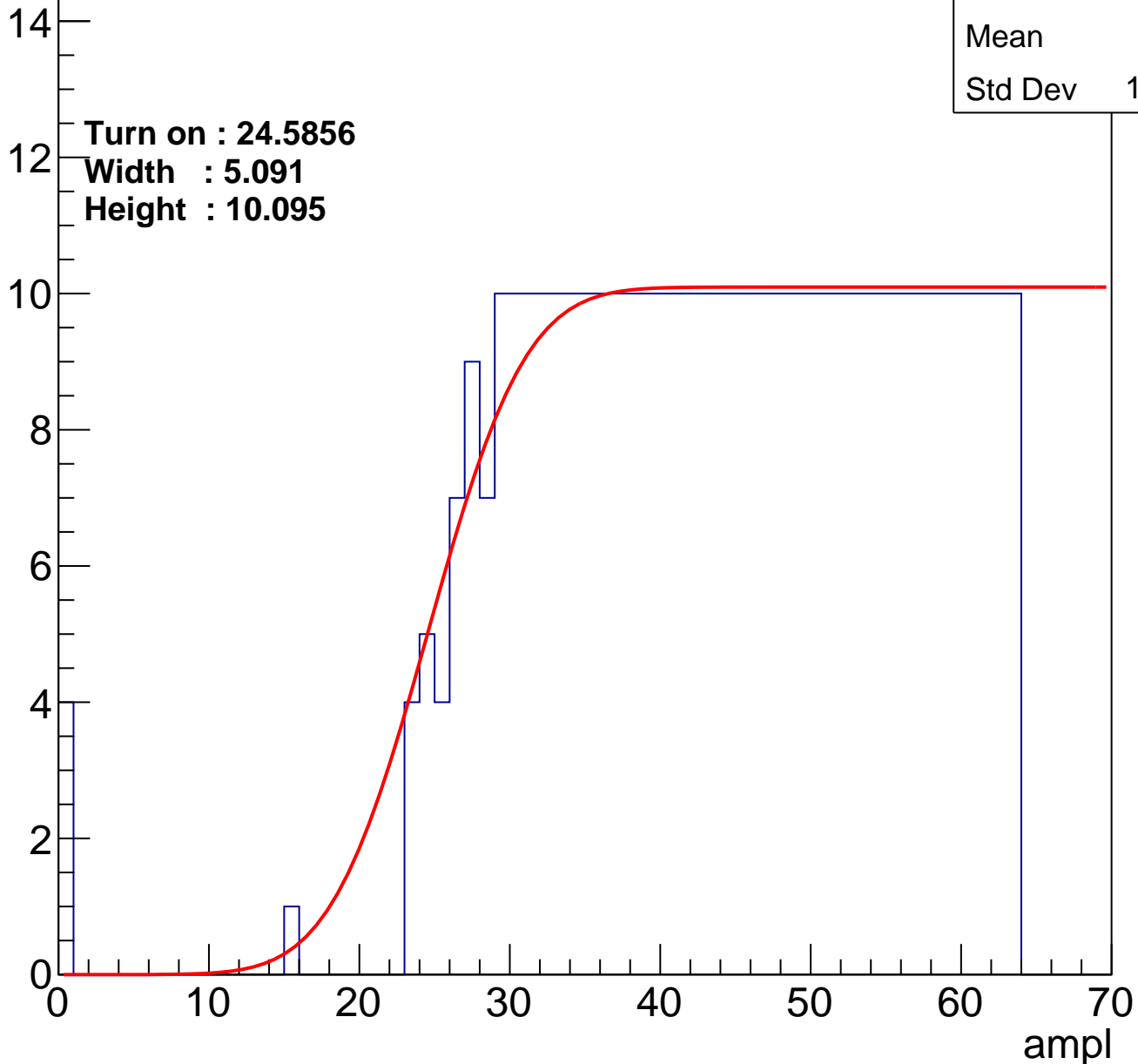
Entries	391
Mean	43.6
Std Dev	12.13

Turn on : 24.5856

Width : 5.091

Height : 10.095

Entry



B1L101S, U15-ch92

calib_packv5_042523_0143.root, FC#0, port D2

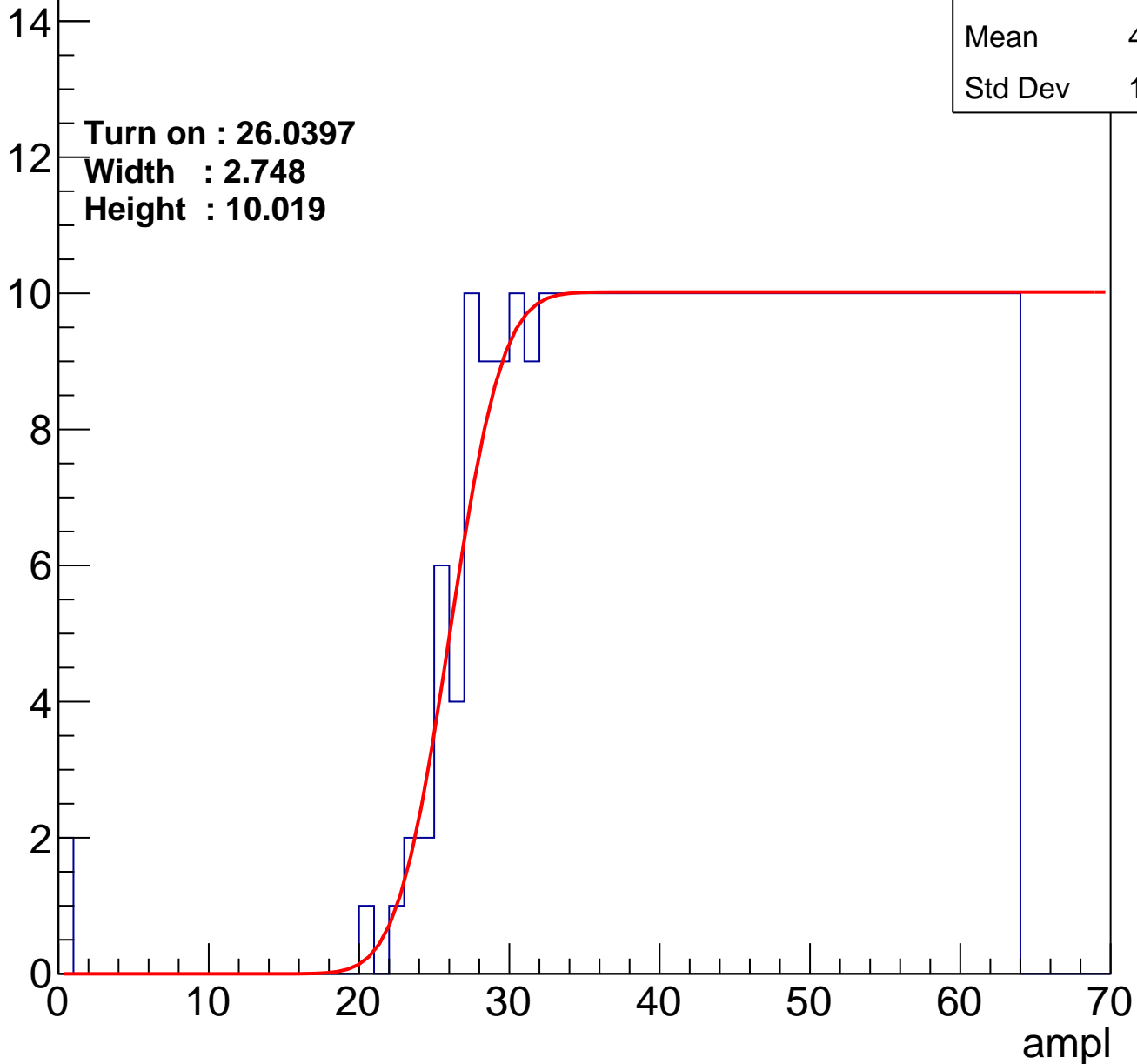
Entries	385
Mean	44.03
Std Dev	11.62

Turn on : 26.0397

Width : 2.748

Height : 10.019

Entry



B1L101S, U15-ch93

calib_packv5_042523_0143.root, FC#0, port D2

Entries	365
Mean	44.92
Std Dev	11.27

Turn on : 27.4987

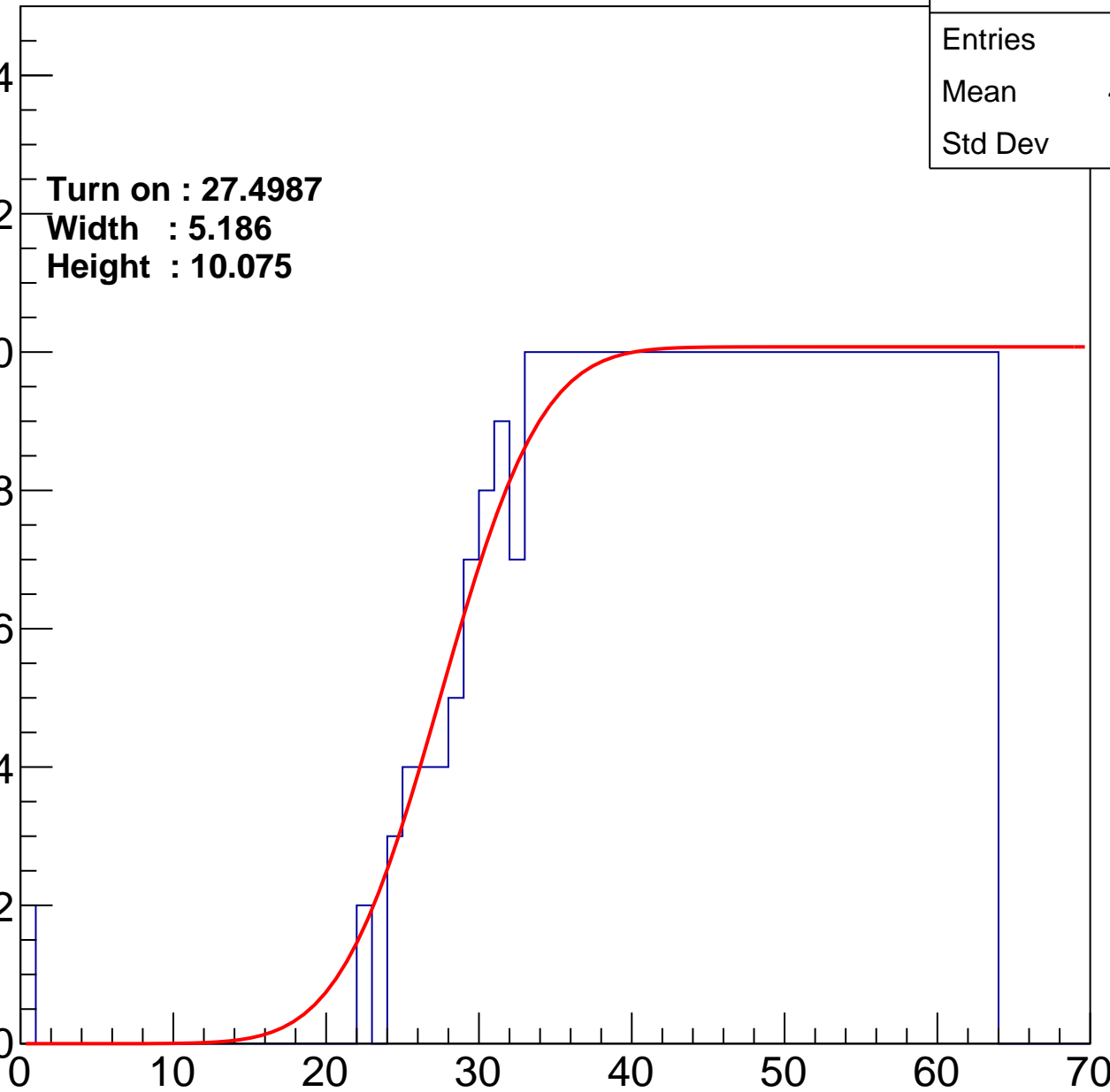
Width : 5.186

Height : 10.075

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch94

calib_packv5_042523_0143.root, FC#0, port D2

Entries	381
Mean	44.12
Std Dev	11.77

Turn on : 26.9146

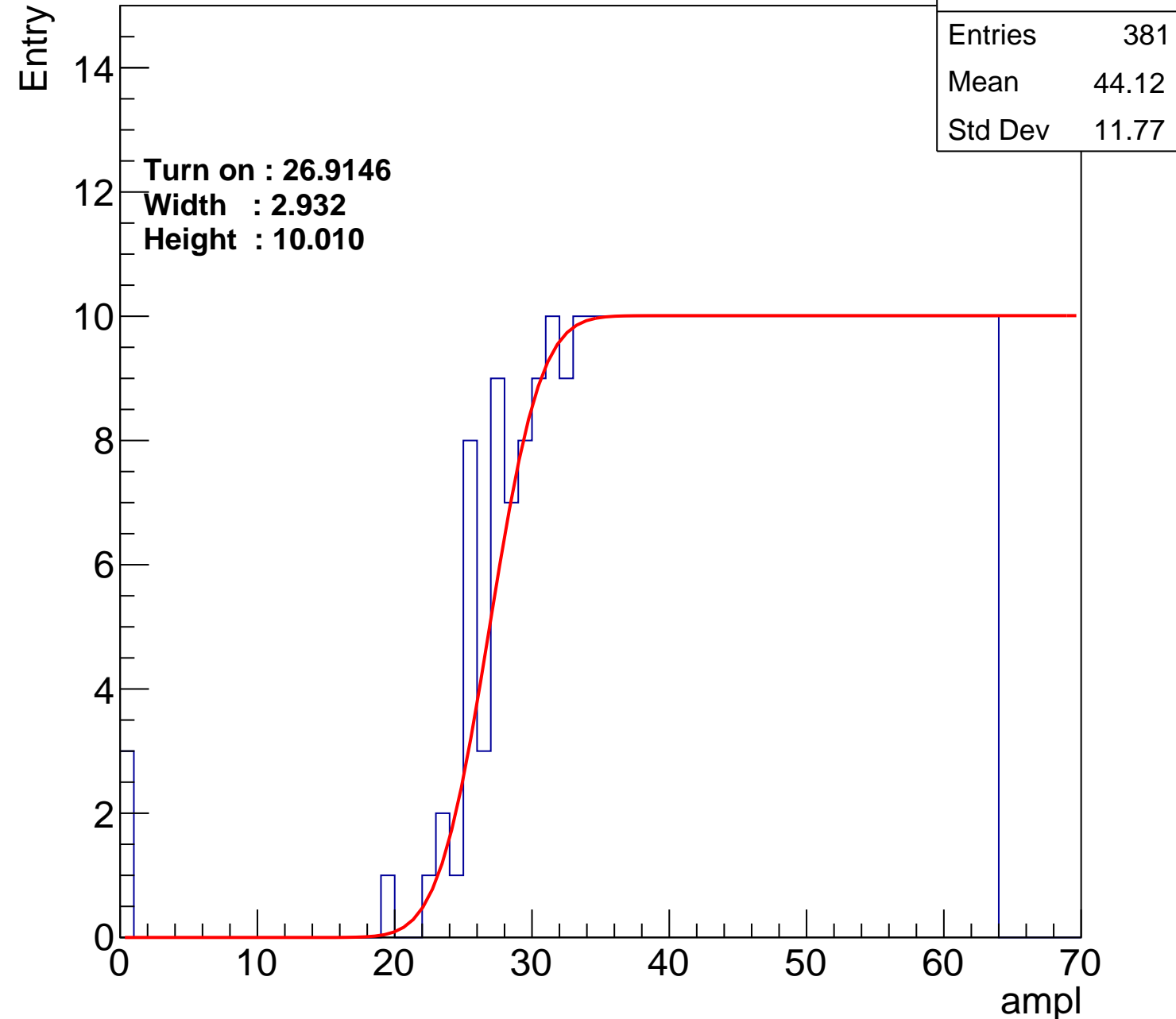
Width : 2.932

Height : 10.010

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch95

calib_packv5_042523_0143.root, FC#0, port D2

Entries	379
Mean	44.19
Std Dev	11.84

Turn on : 27.0295

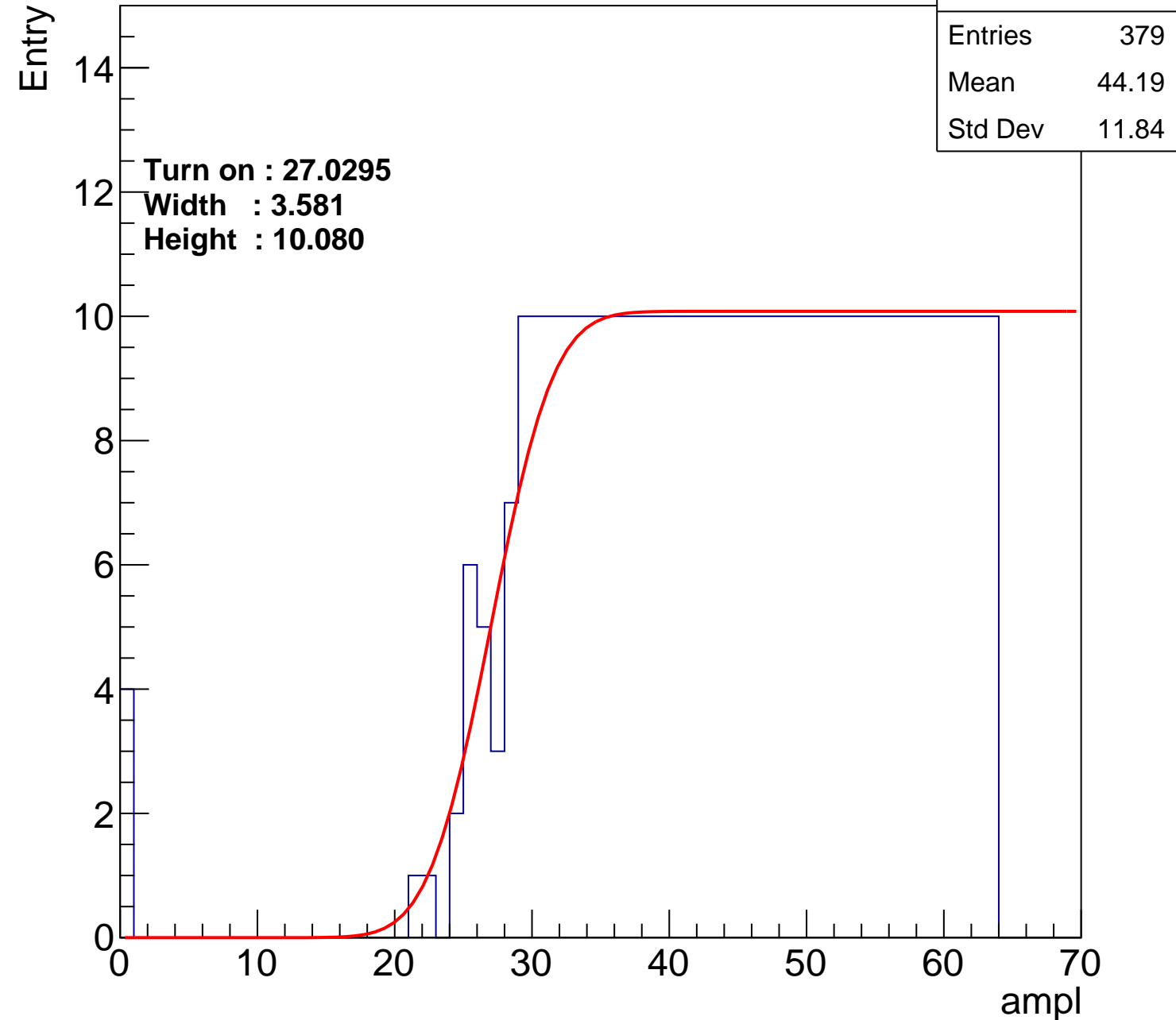
Width : 3.581

Height : 10.080

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch96

calib_packv5_042523_0143.root, FC#0, port D2

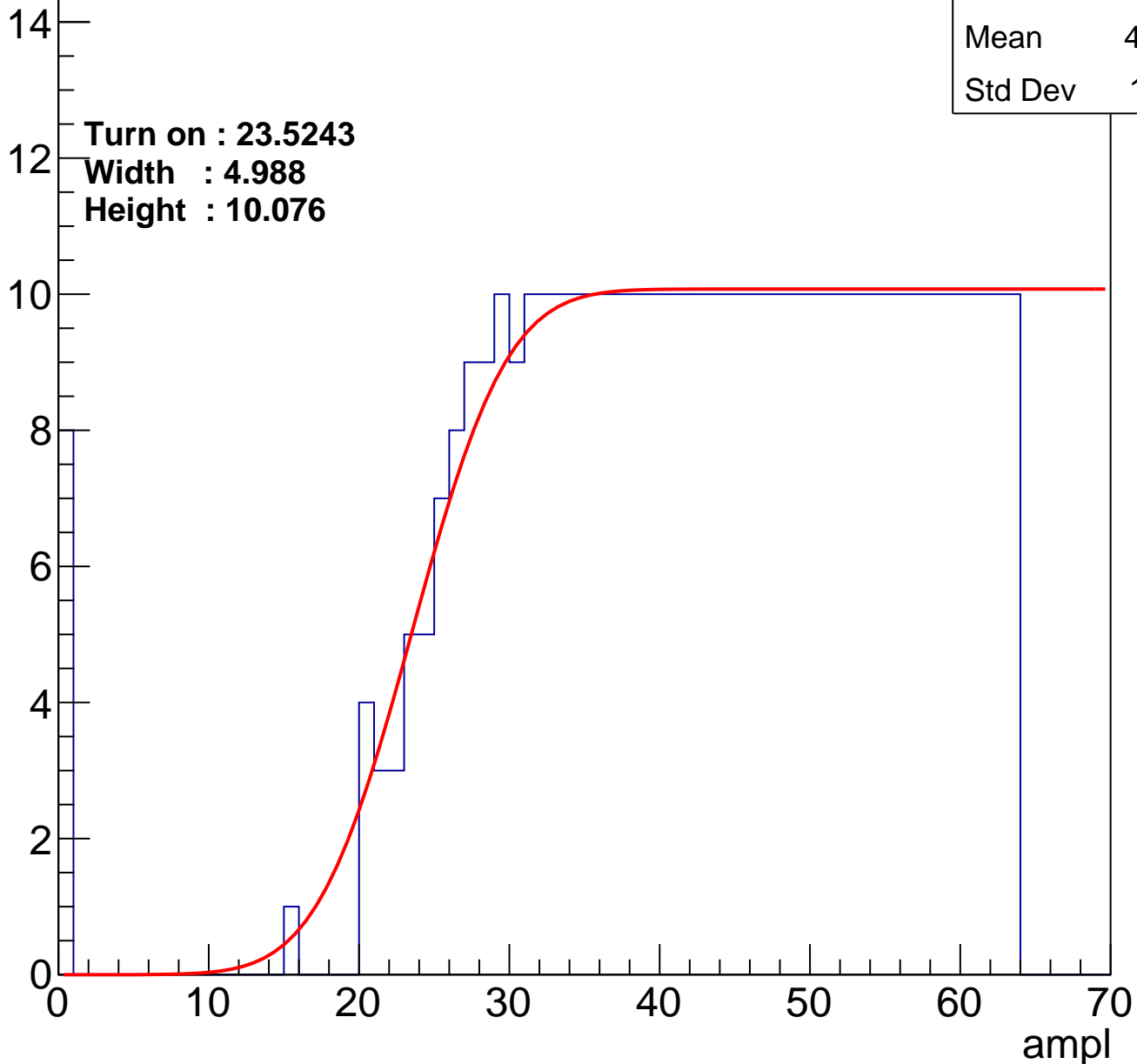
Entries	411
Mean	42.35
Std Dev	13.21

Turn on : 23.5243

Width : 4.988

Height : 10.076

Entry



B1L101S, U15-ch97

calib_packv5_042523_0143.root, FC#0, port D2

Entries	387
Mean	43.77
Std Dev	12.01

Turn on : 26.0019

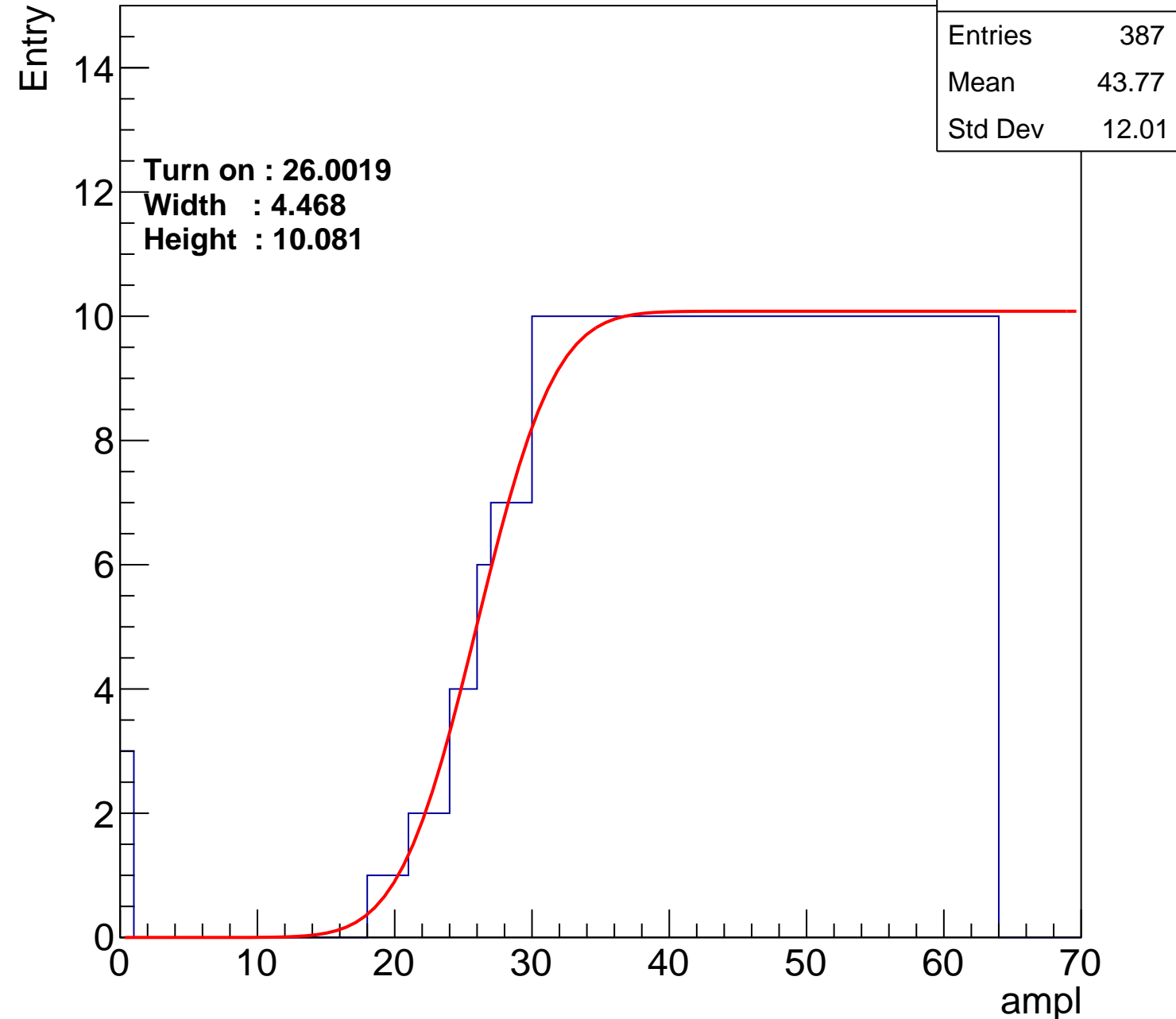
Width : 4.468

Height : 10.081

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch98

calib_packv5_042523_0143.root, FC#0, port D2

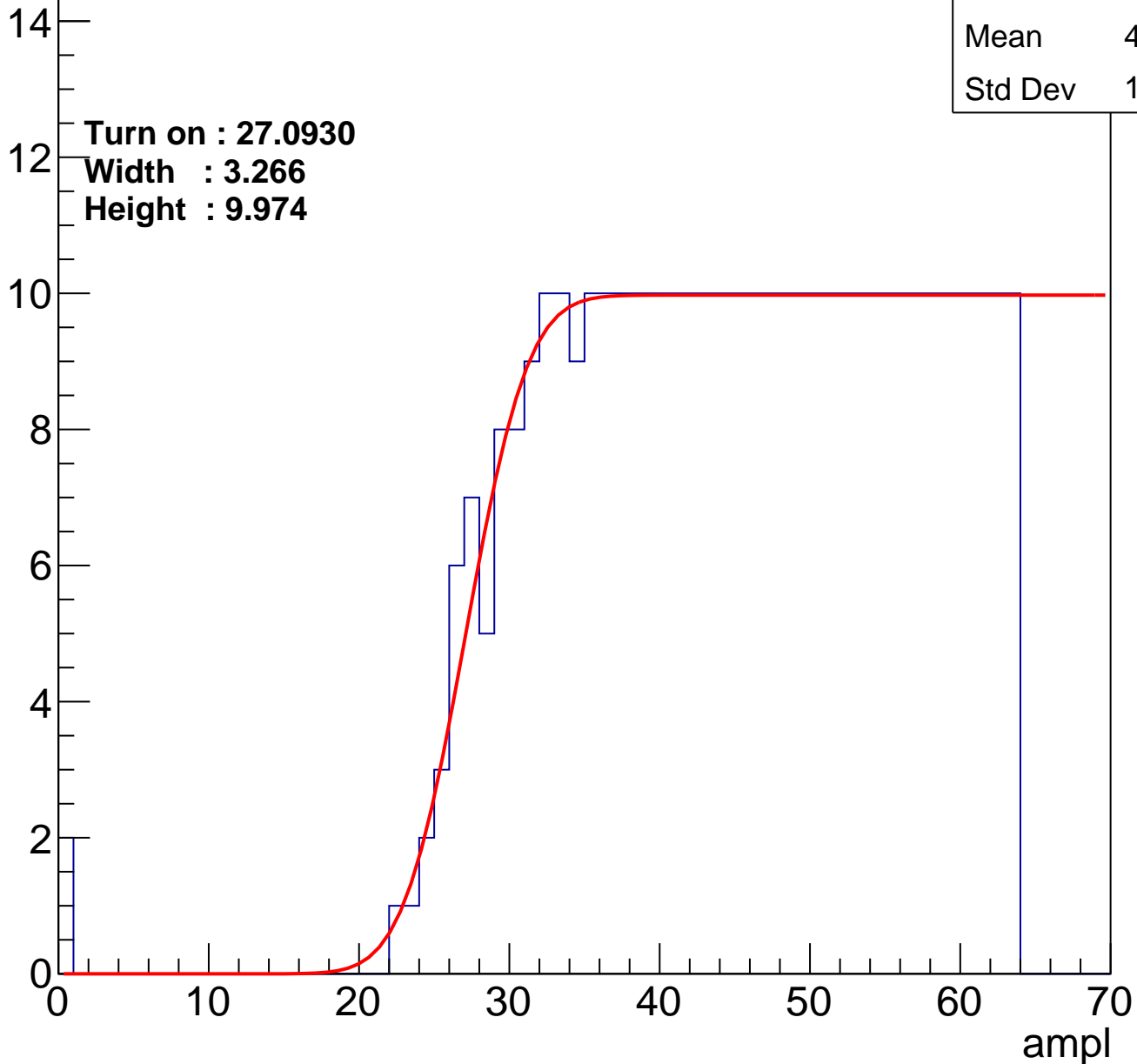
Entries	371
Mean	44.66
Std Dev	11.35

Turn on : 27.0930

Width : 3.266

Height : 9.974

Entry



B1L101S, U15-ch99

calib_packv5_042523_0143.root, FC#0, port D2

Entries	373
Mean	44.26
Std Dev	12.26

Turn on : 27.7249

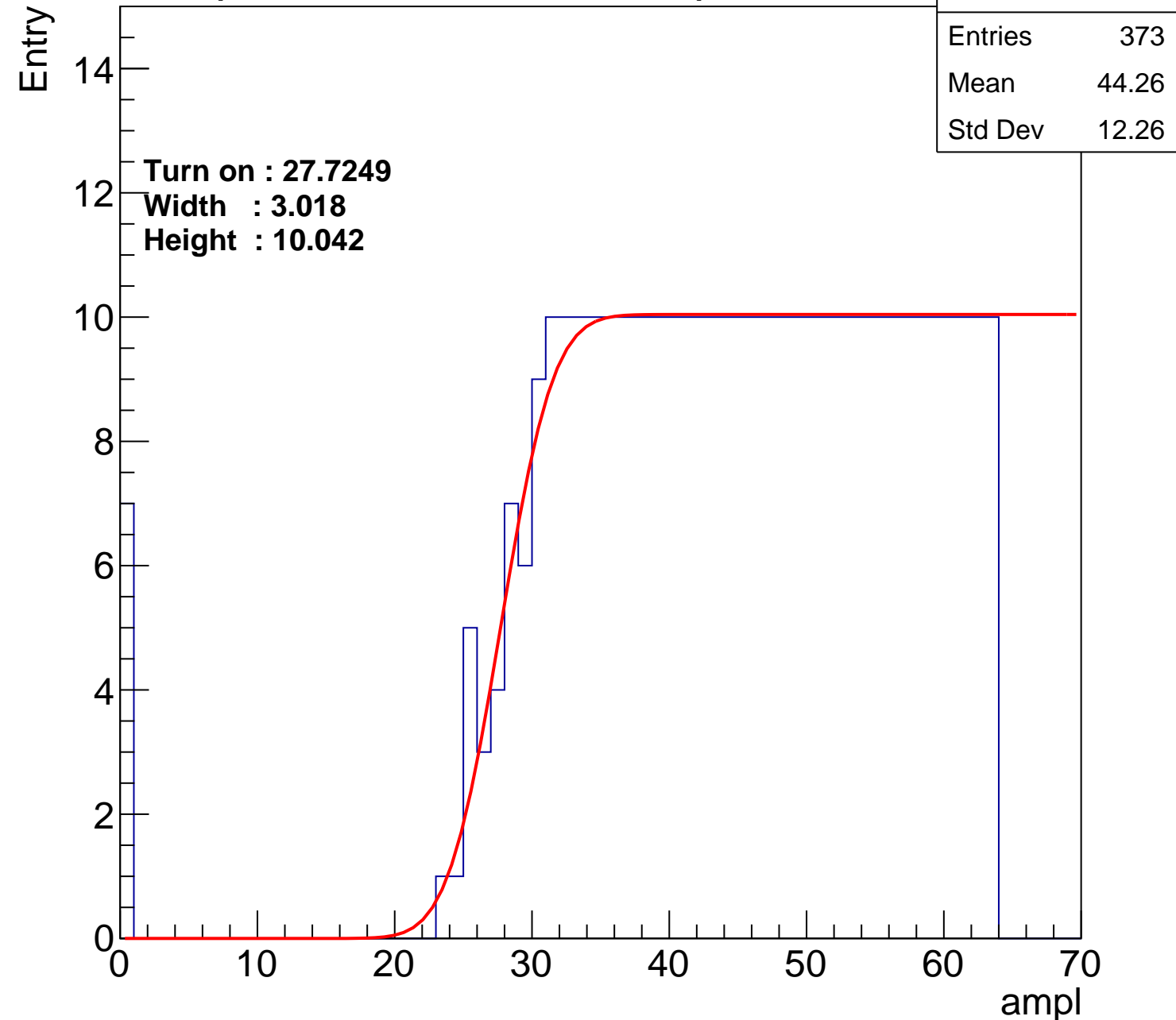
Width : 3.018

Height : 10.042

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch100

calib_packv5_042523_0143.root, FC#0, port D2

Entries	378
Mean	43.92
Std Dev	12.57

Turn on : 27.7532

Width : 3.477

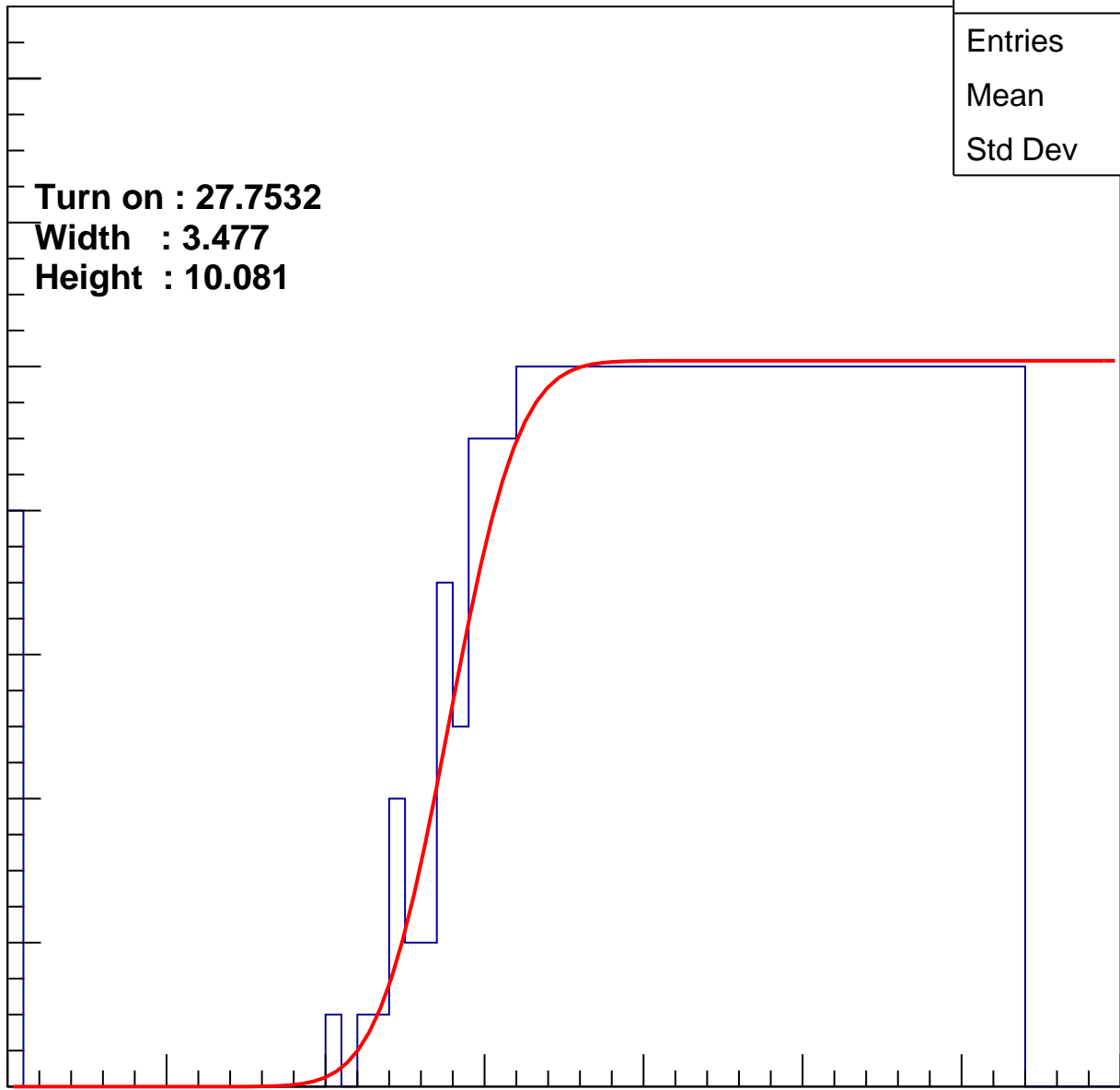
Height : 10.081

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L101S, U15-ch101

calib_packv5_042523_0143.root, FC#0, port D2

Entries	368
Mean	44.88
Std Dev	11.08

Turn on : 27.4492

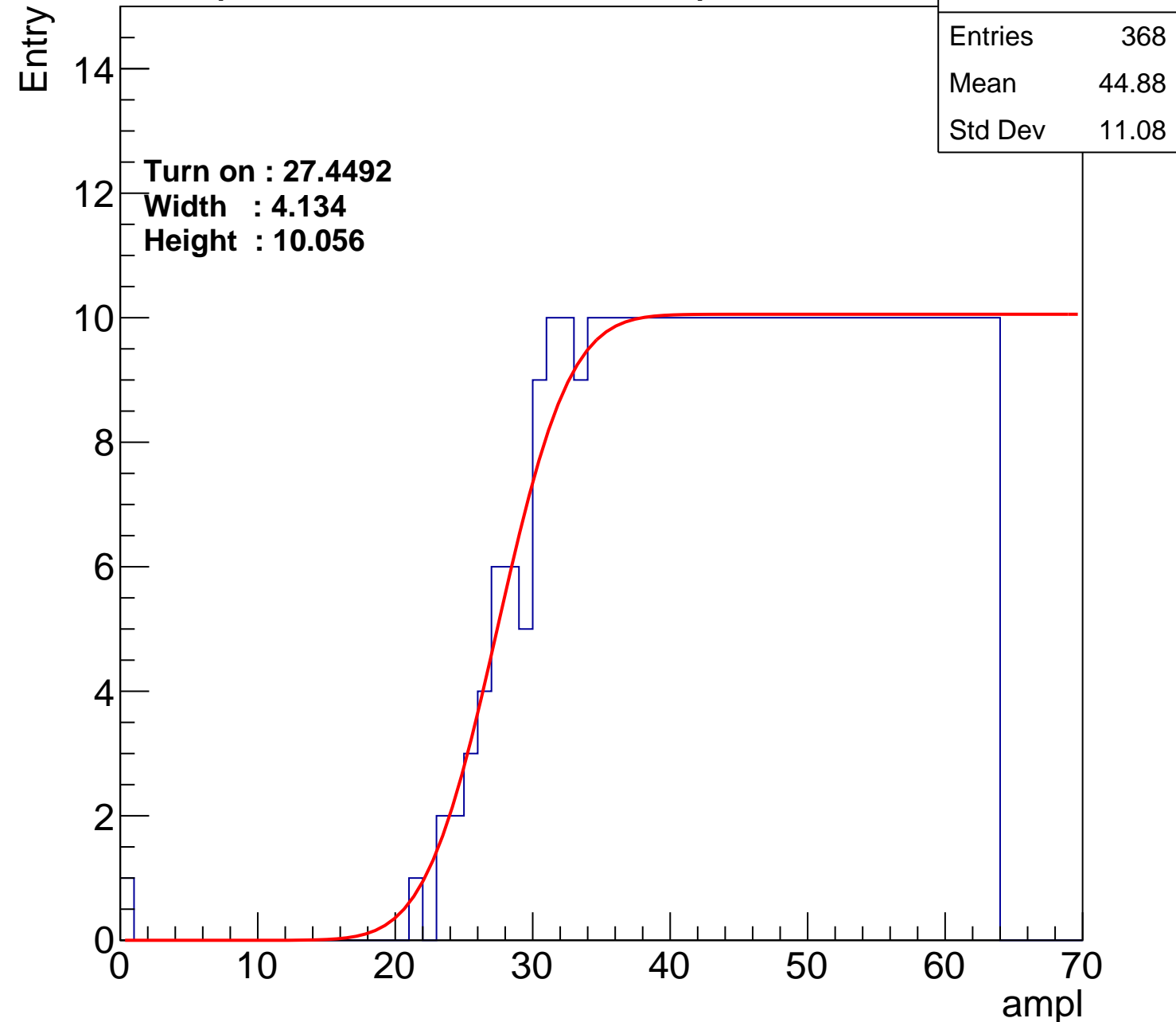
Width : 4.134

Height : 10.056

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch102

calib_packv5_042523_0143.root, FC#0, port D2

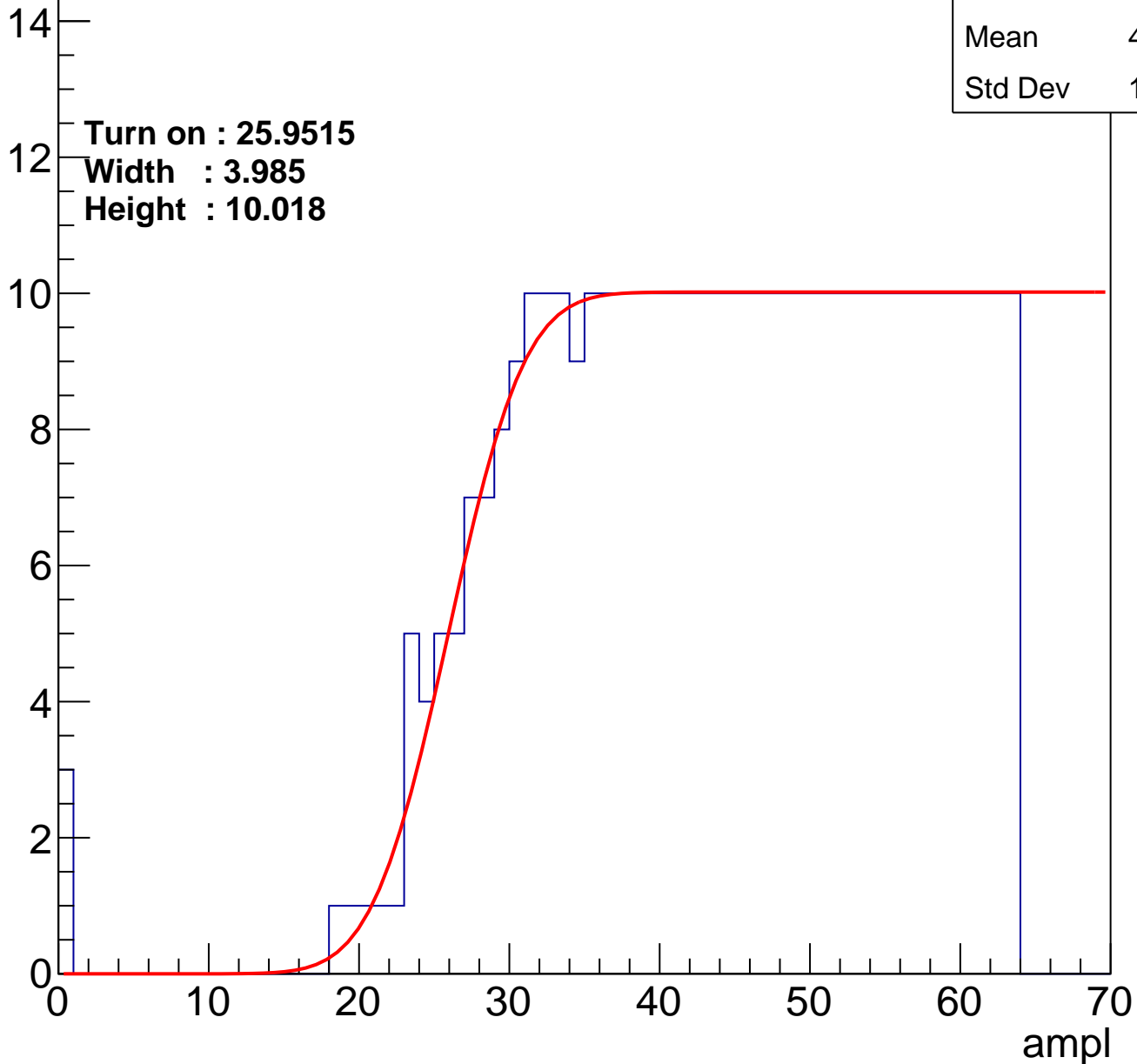
Entries	387
Mean	43.74
Std Dev	12.04

Turn on : 25.9515

Width : 3.985

Height : 10.018

Entry



B1L101S, U15-ch103

calib_packv5_042523_0143.root, FC#0, port D2

Entries	369
Mean	44.88
Std Dev	11.03

Turn on : 27.4563

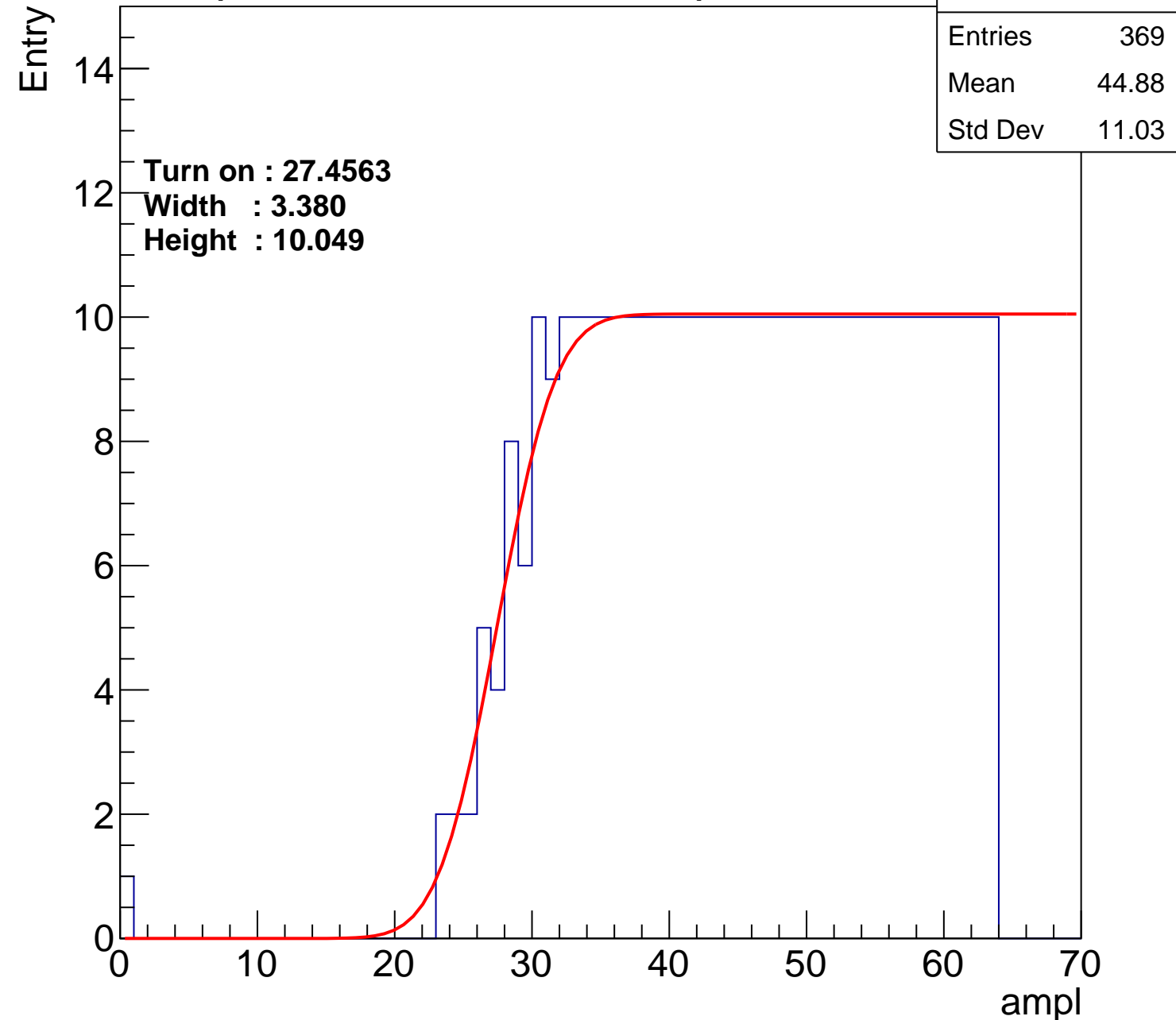
Width : 3.380

Height : 10.049

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch104

calib_packv5_042523_0143.root, FC#0, port D2

Entries	391
Mean	43.64
Std Dev	12

Turn on : 25.4627

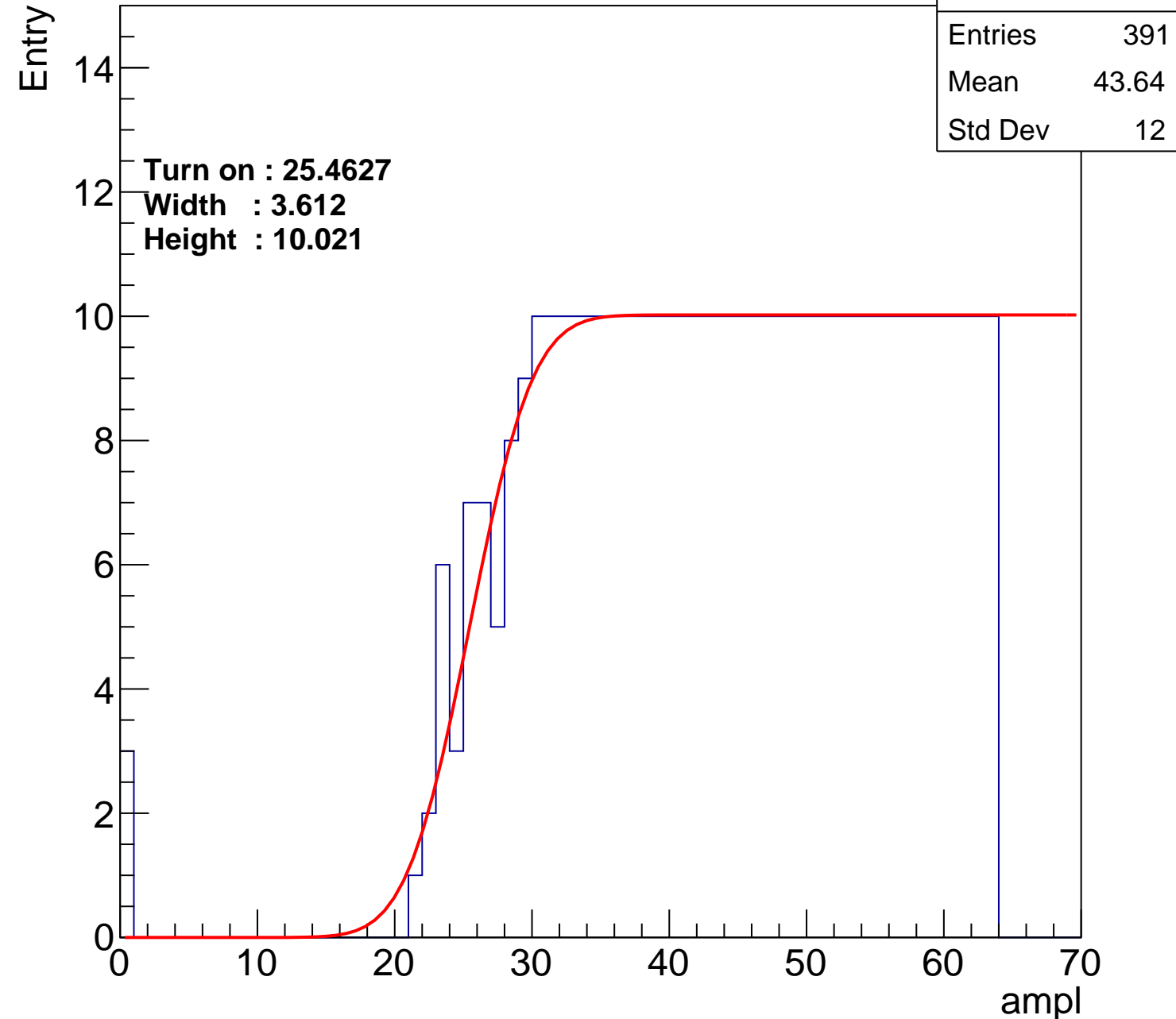
Width : 3.612

Height : 10.021

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch105

calib_packv5_042523_0143.root, FC#0, port D2

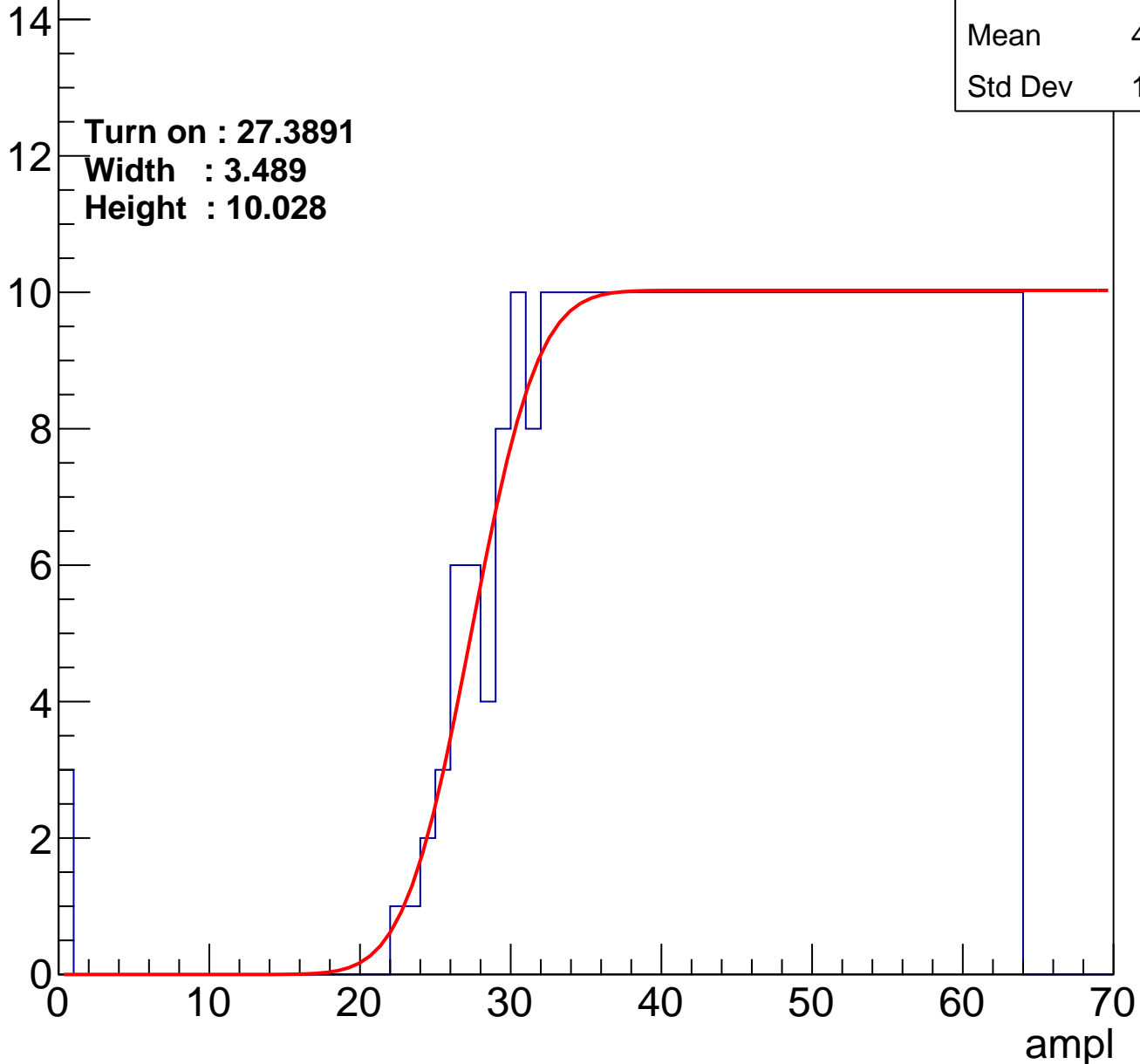
Entries	372
Mean	44.56
Std Dev	11.54

Turn on : 27.3891

Width : 3.489

Height : 10.028

Entry



B1L101S, U15-ch106

calib_packv5_042523_0143.root, FC#0, port D2

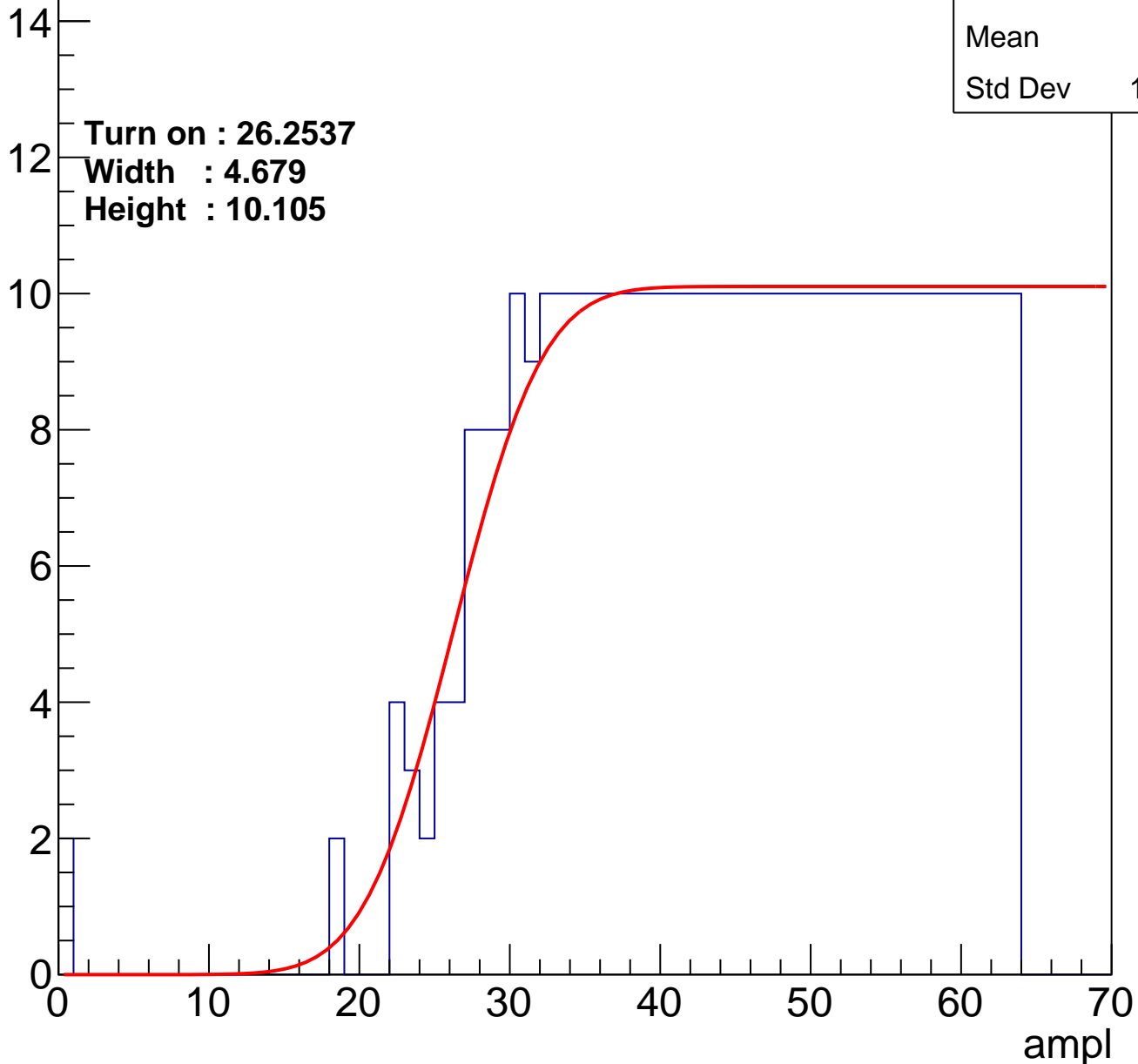
Entries	384
Mean	44
Std Dev	11.73

Turn on : 26.2537

Width : 4.679

Height : 10.105

Entry



B1L101S, U15-ch107

calib_packv5_042523_0143.root, FC#0, port D2

Entries	384
Mean	44.01
Std Dev	11.71

Turn on : 26.3355

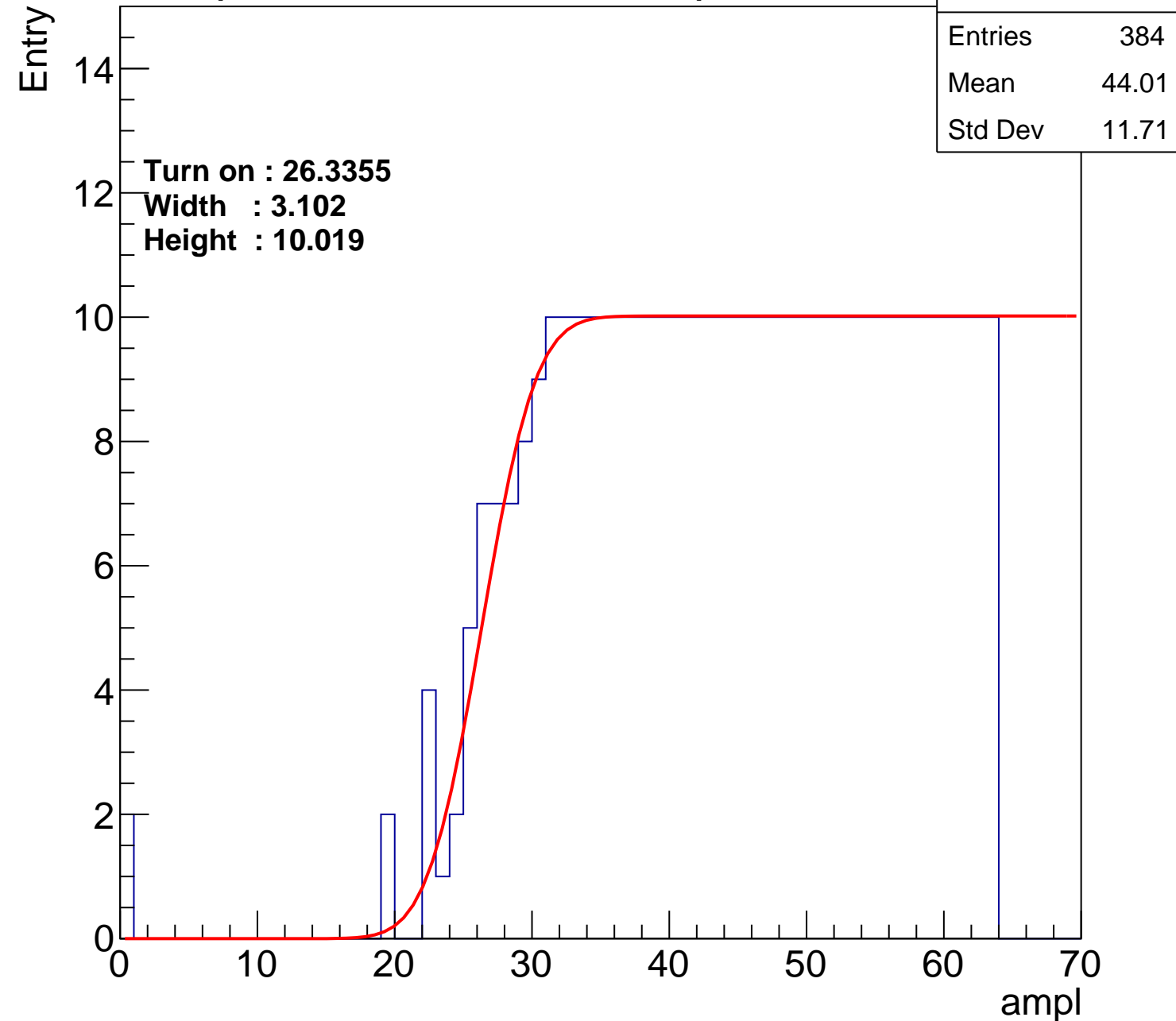
Width : 3.102

Height : 10.019

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch108

calib_packv5_042523_0143.root, FC#0, port D2

Entries	379
Mean	44.11
Std Dev	11.95

Turn on : 26.9110

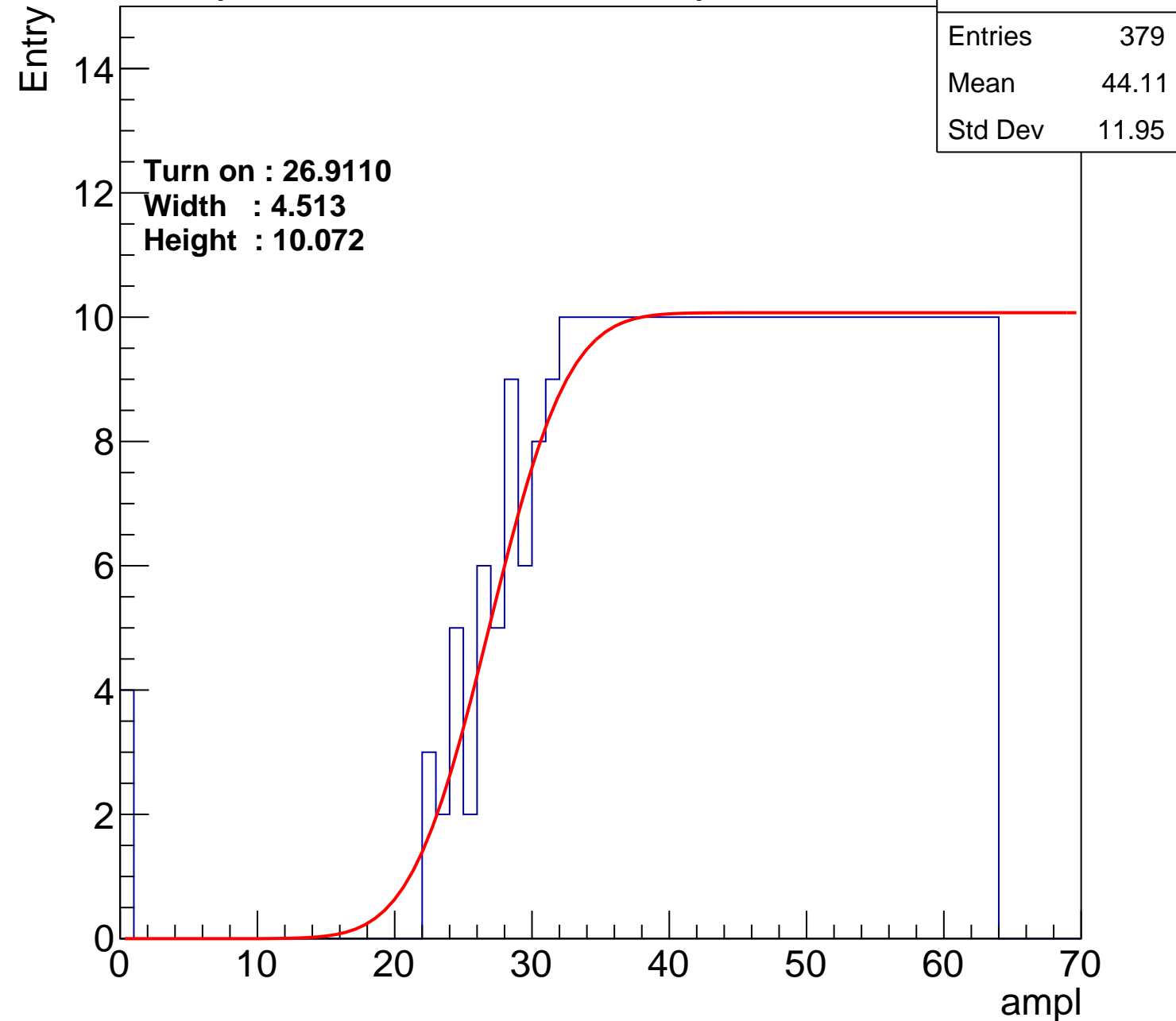
Width : 4.513

Height : 10.072

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch109

calib_packv5_042523_0143.root, FC#0, port D2

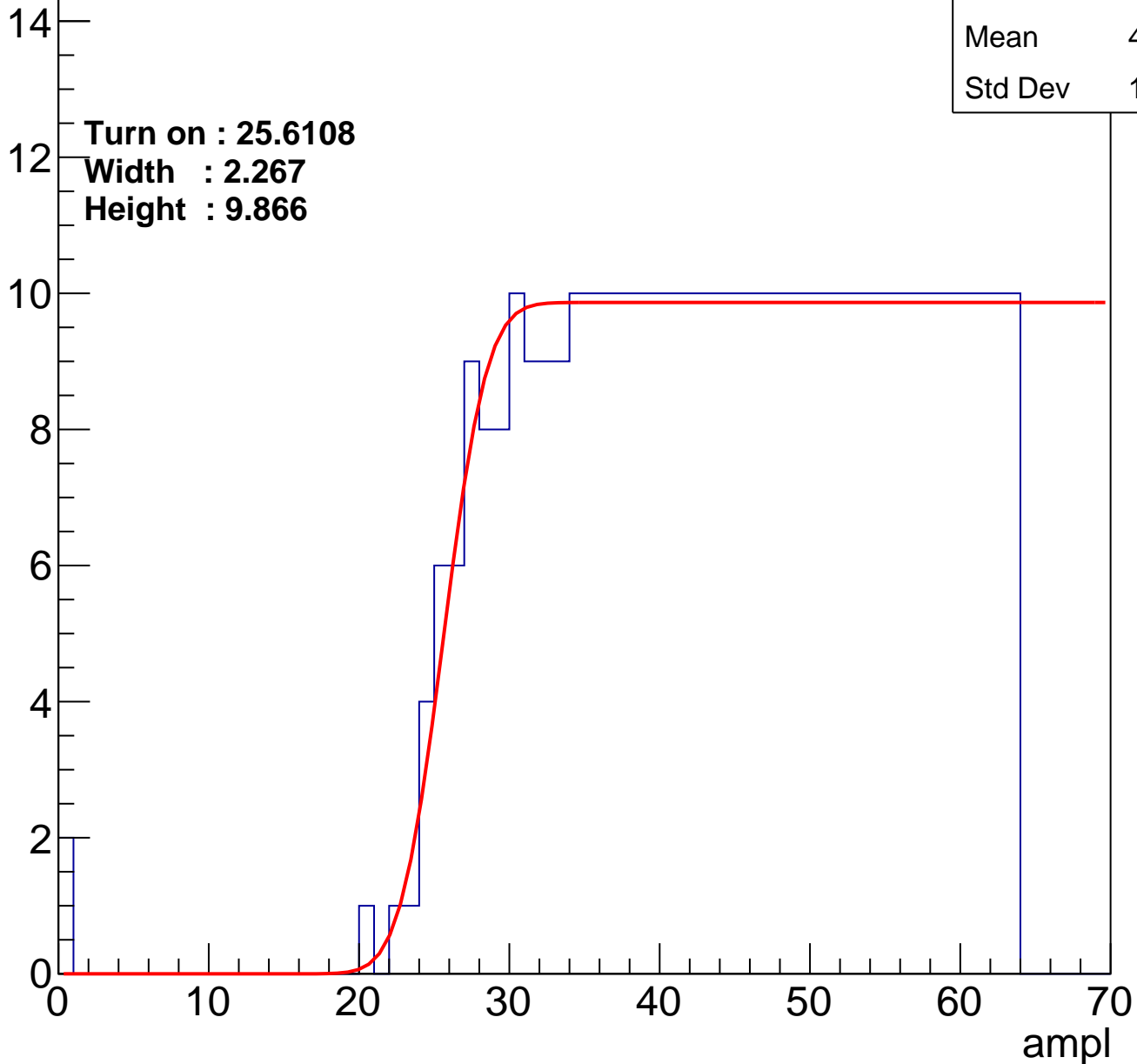
Entries	383
Mean	44.07
Std Dev	11.65

Turn on : 25.6108

Width : 2.267

Height : 9.866

Entry



B1L101S, U15-ch110

calib_packv5_042523_0143.root, FC#0, port D2

Entries	379
Mean	44.05
Std Dev	12.11

Turn on : 27.1322

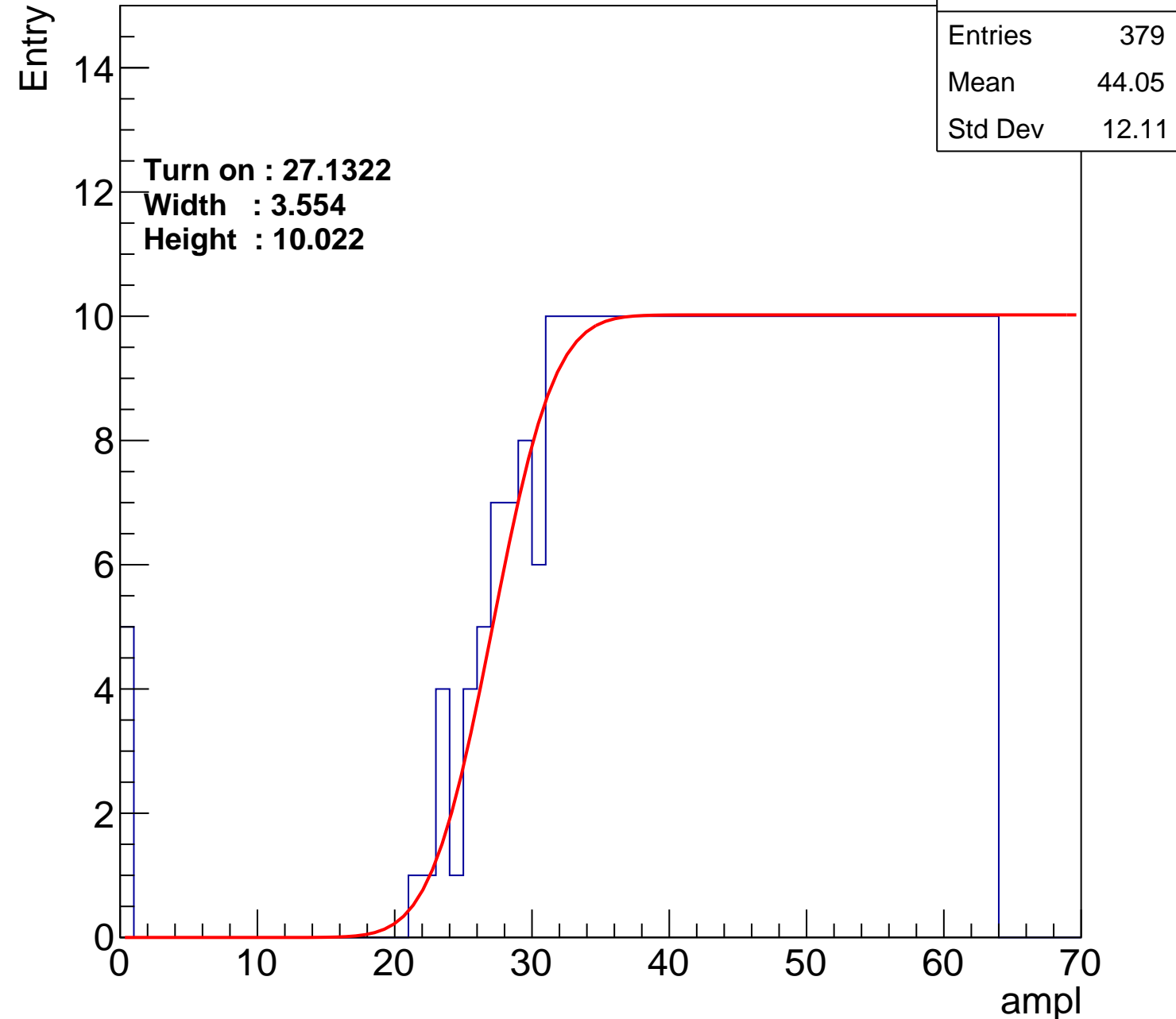
Width : 3.554

Height : 10.022

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch111

calib_packv5_042523_0143.root, FC#0, port D2

Entries	388
Mean	43.78
Std Dev	11.93

Turn on : 25.3450

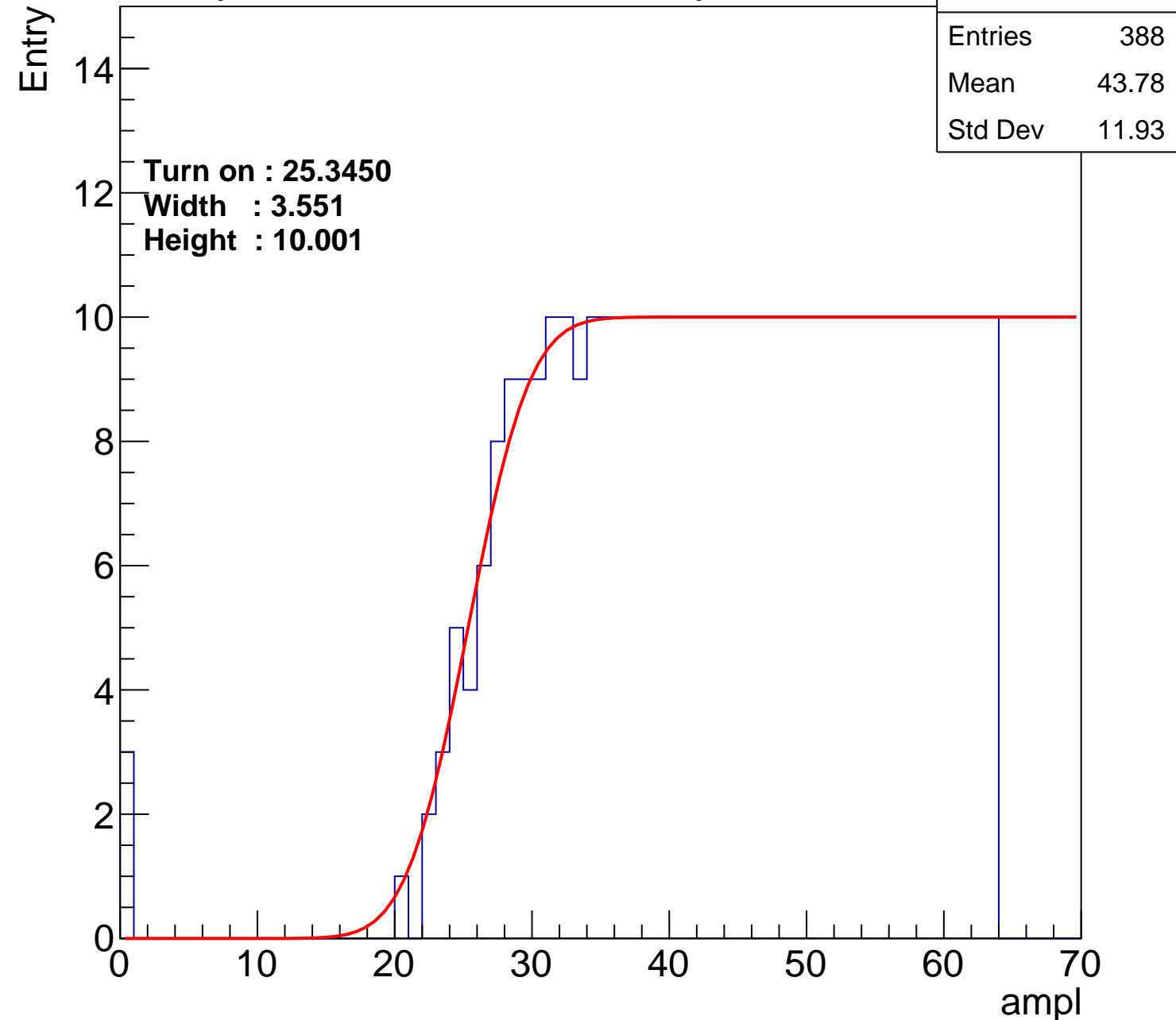
Width : 3.551

Height : 10.001

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch112

calib_packv5_042523_0143.root, FC#0, port D2

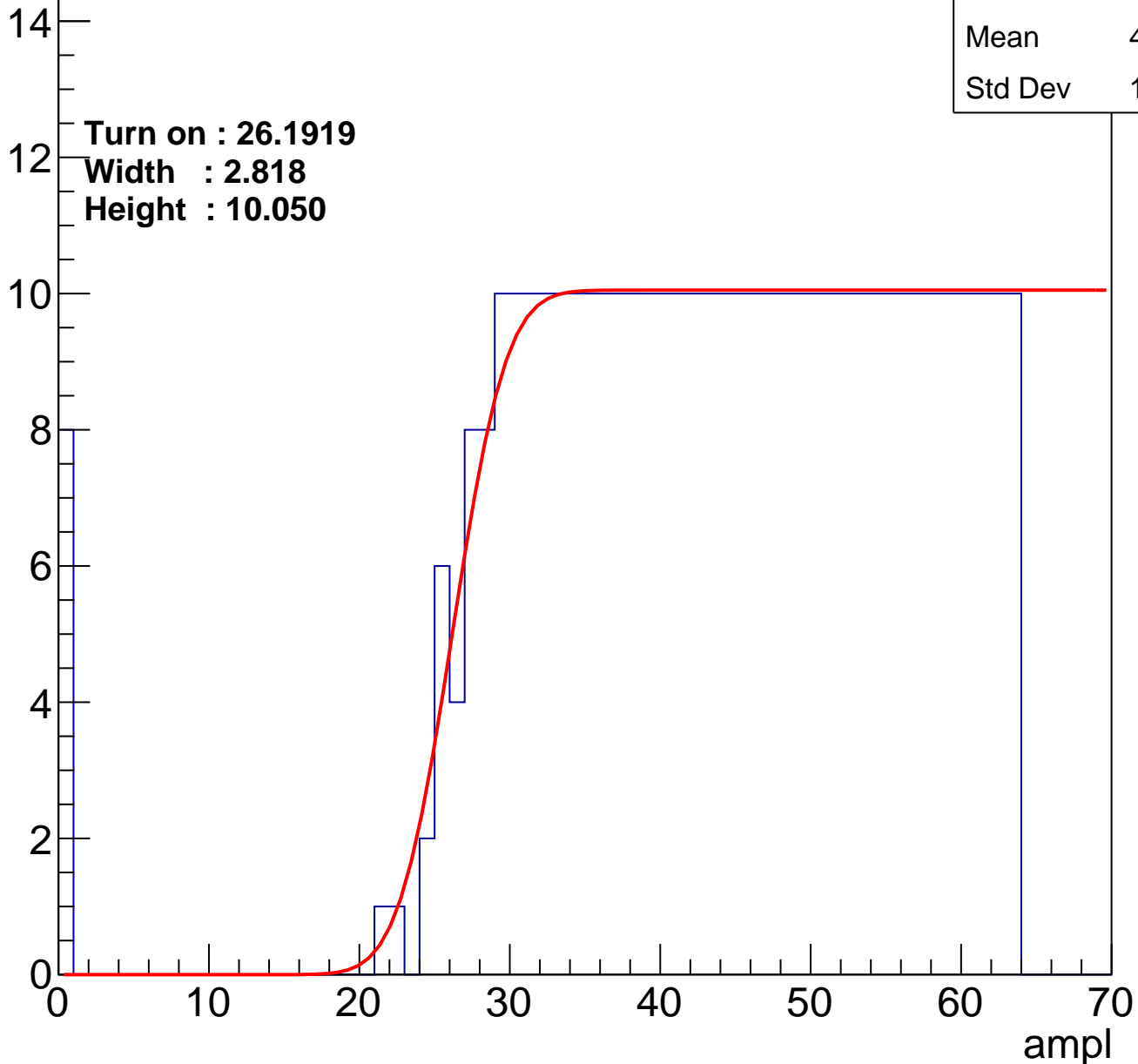
Entries	388
Mean	43.52
Std Dev	12.65

Turn on : 26.1919

Width : 2.818

Height : 10.050

Entry



B1L101S, U15-ch113

calib_packv5_042523_0143.root, FC#0, port D2

Entries	370
Mean	44.55
Std Dev	11.75

Turn on : 26.4798

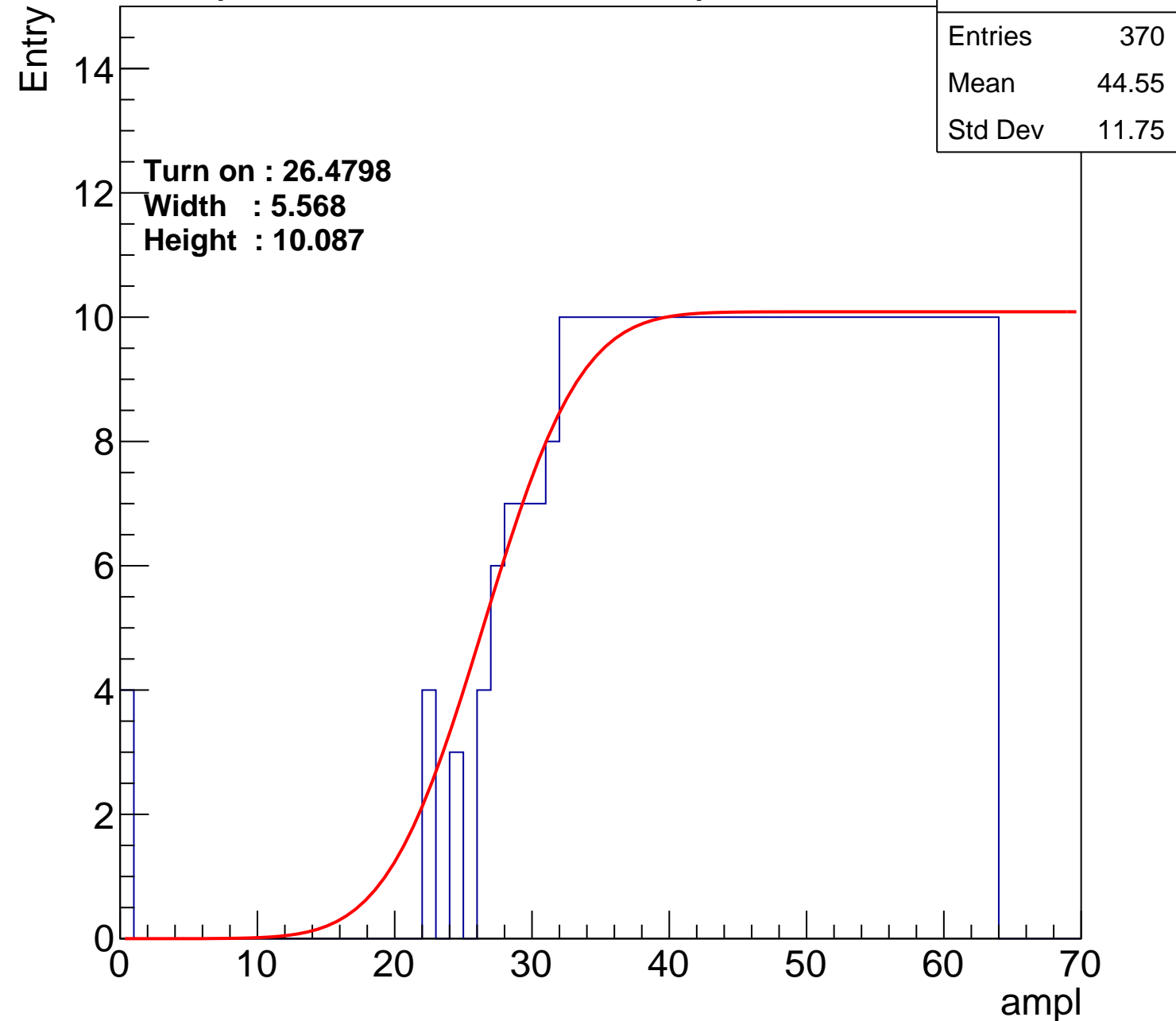
Width : 5.568

Height : 10.087

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch114

calib_packv5_042523_0143.root, FC#0, port D2

Entries	400
Mean	42.79
Std Dev	13.17

Turn on : 25.4127

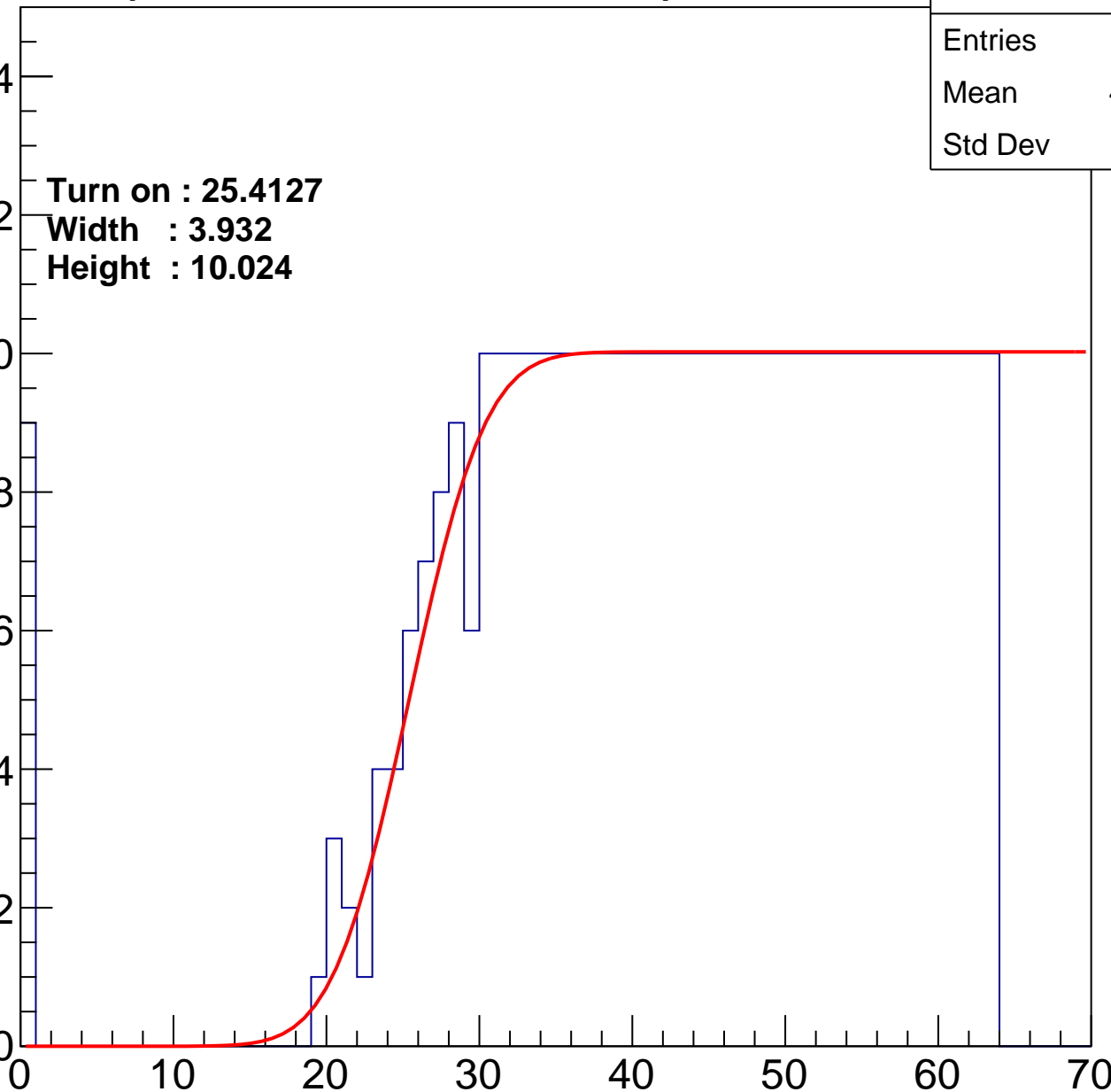
Width : 3.932

Height : 10.024

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch115

calib_packv5_042523_0143.root, FC#0, port D2

Entries	382
Mean	44.06
Std Dev	11.8

Turn on : 26.3474

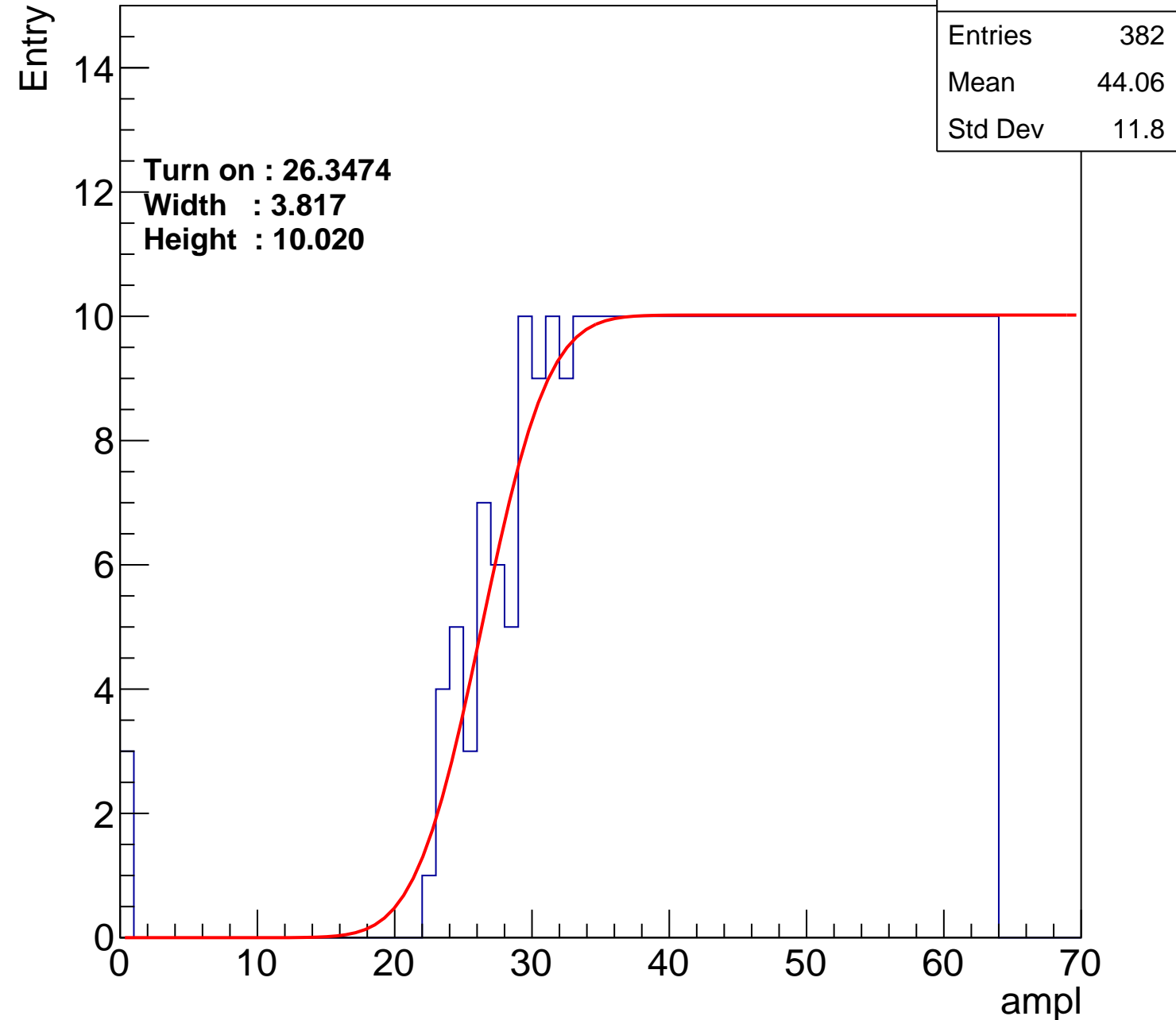
Width : 3.817

Height : 10.020

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch116

calib_packv5_042523_0143.root, FC#0, port D2

Entries	366
Mean	44.74
Std Dev	11.66

Turn on : 28.3988

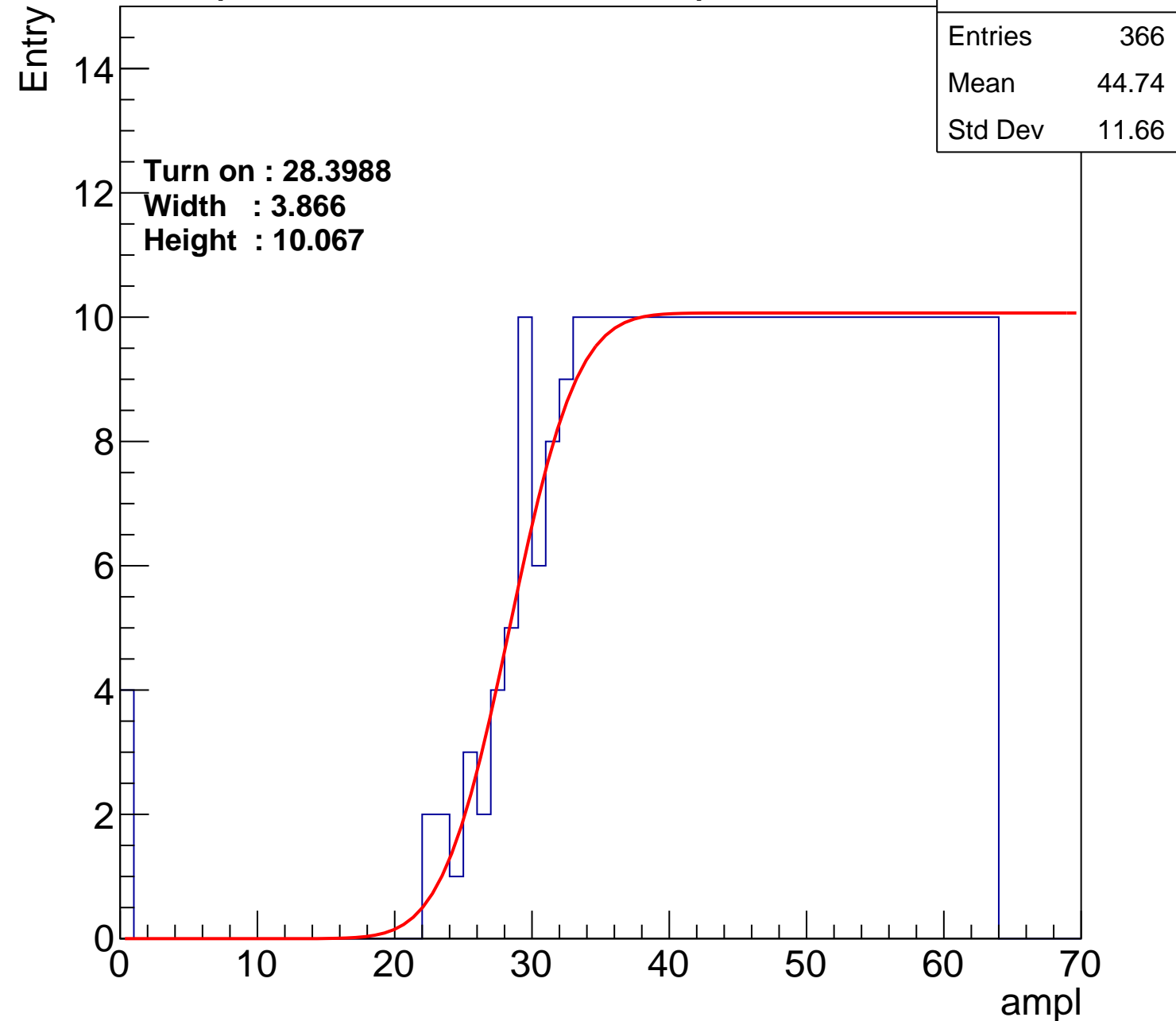
Width : 3.866

Height : 10.067

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch117

calib_packv5_042523_0143.root, FC#0, port D2

Entries	368
Mean	44.71
Std Dev	11.6

Turn on : 27.7404

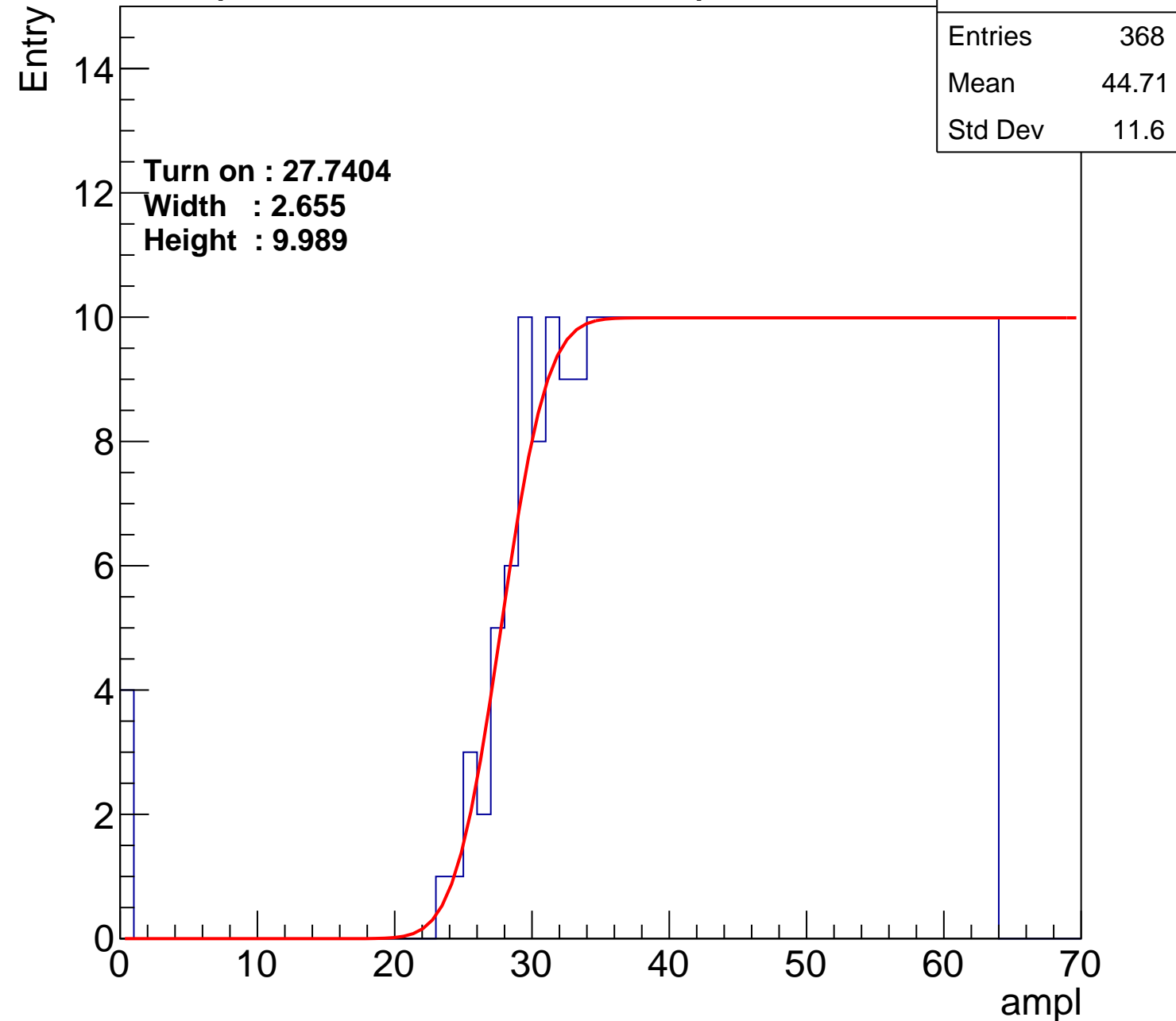
Width : 2.655

Height : 9.989

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch118

calib_packv5_042523_0143.root, FC#0, port D2

Entries	387
Mean	43.93
Std Dev	11.67

Turn on : 25.5218

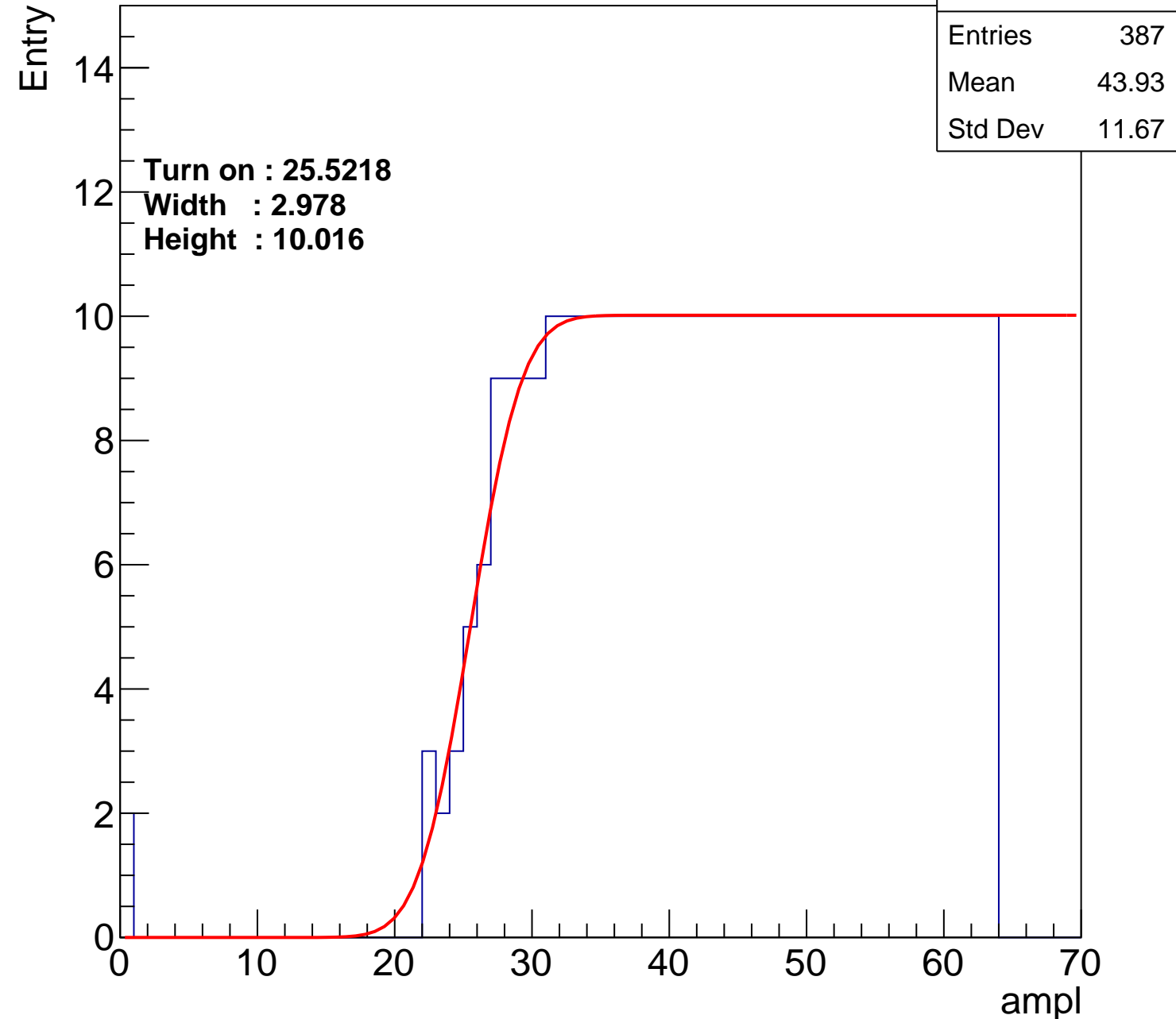
Width : 2.978

Height : 10.016

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch119

calib_packv5_042523_0143.root, FC#0, port D2

Entries	363
Mean	45.15
Std Dev	10.91

Turn on : 27.9912

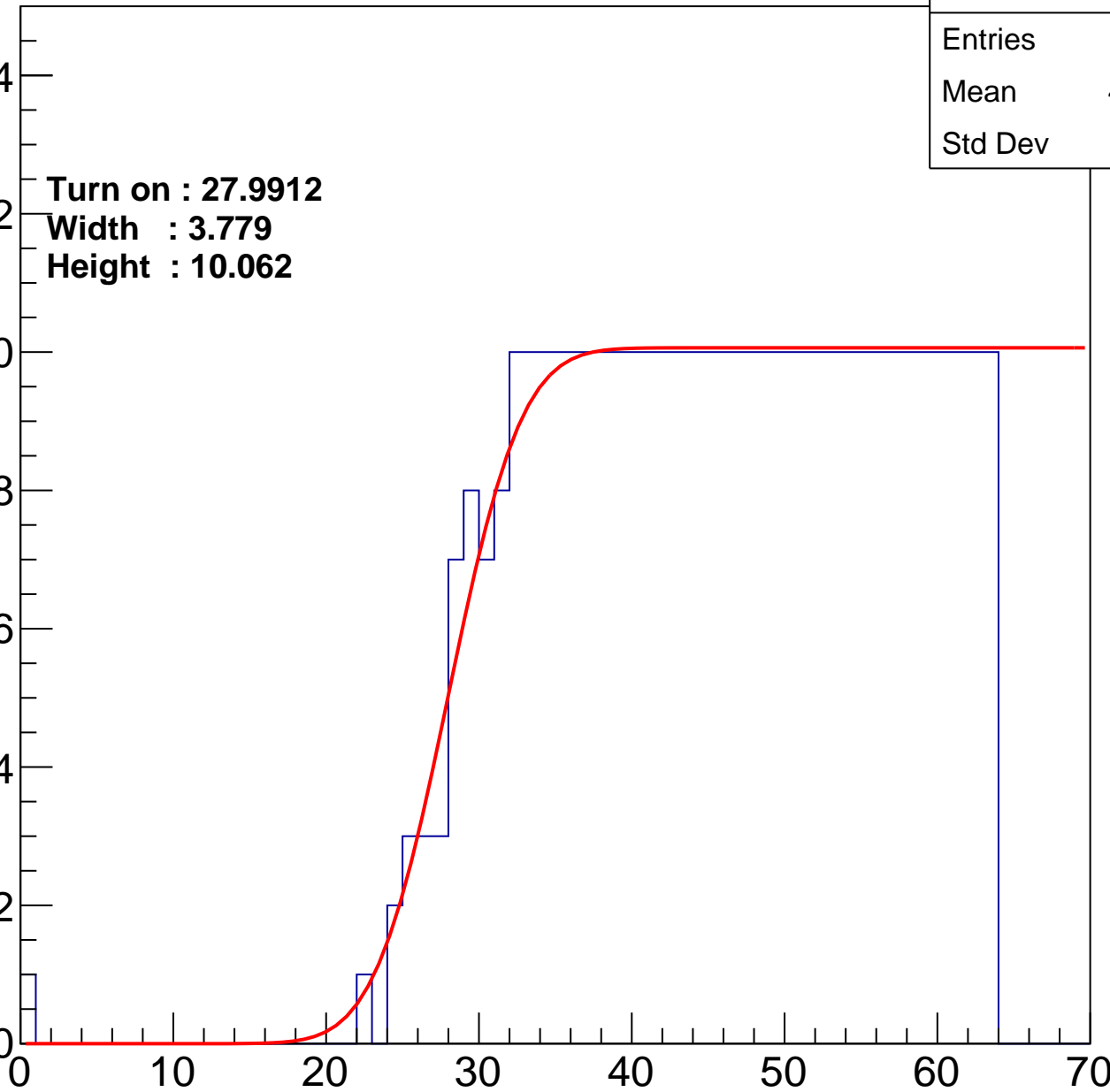
Width : 3.779

Height : 10.062

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch120

calib_packv5_042523_0143.root, FC#0, port D2

Entries	399
Mean	43.05
Std Dev	12.67

Turn on : 24.8136

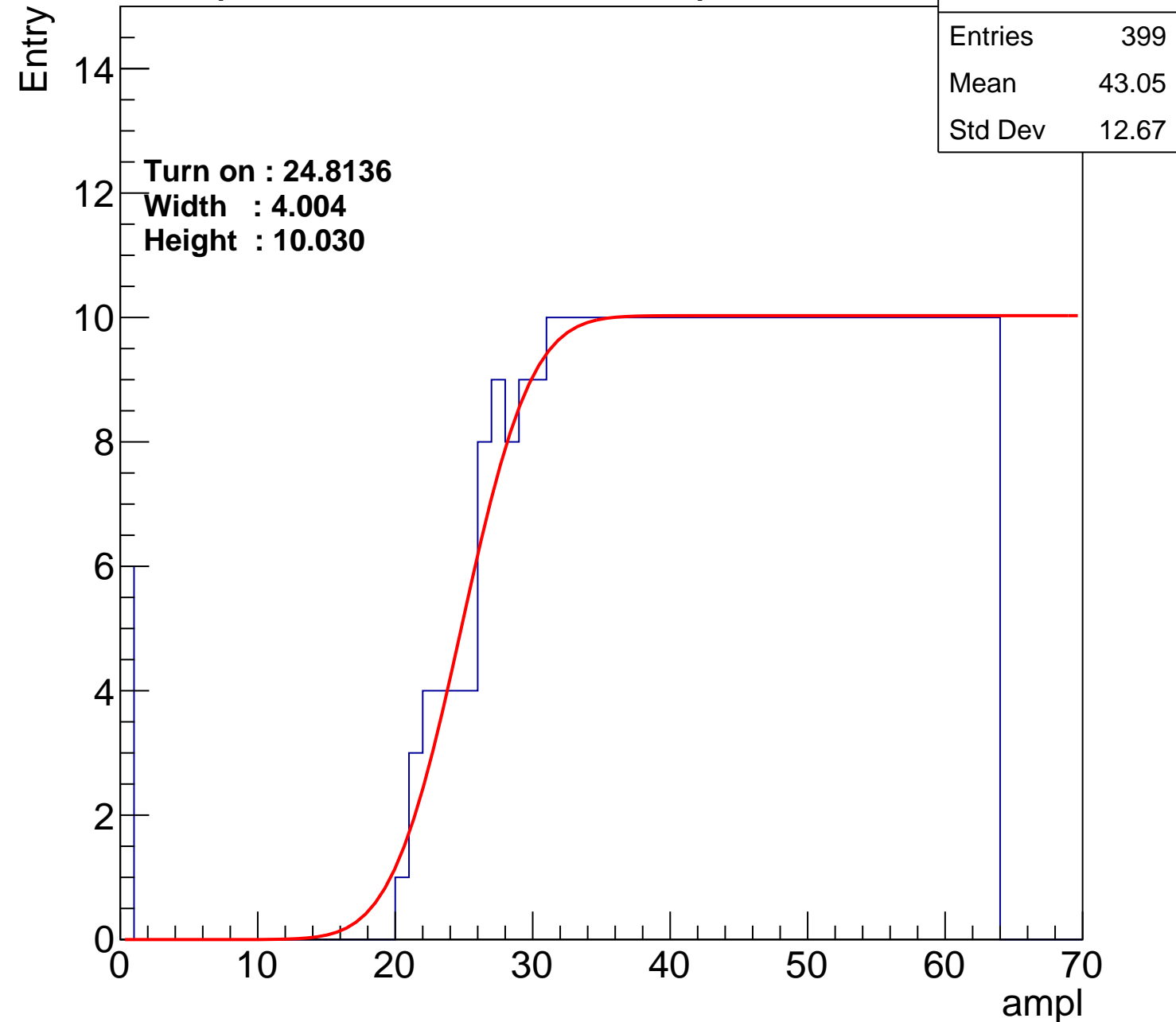
Width : 4.004

Height : 10.030

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch121

calib_packv5_042523_0143.root, FC#0, port D2

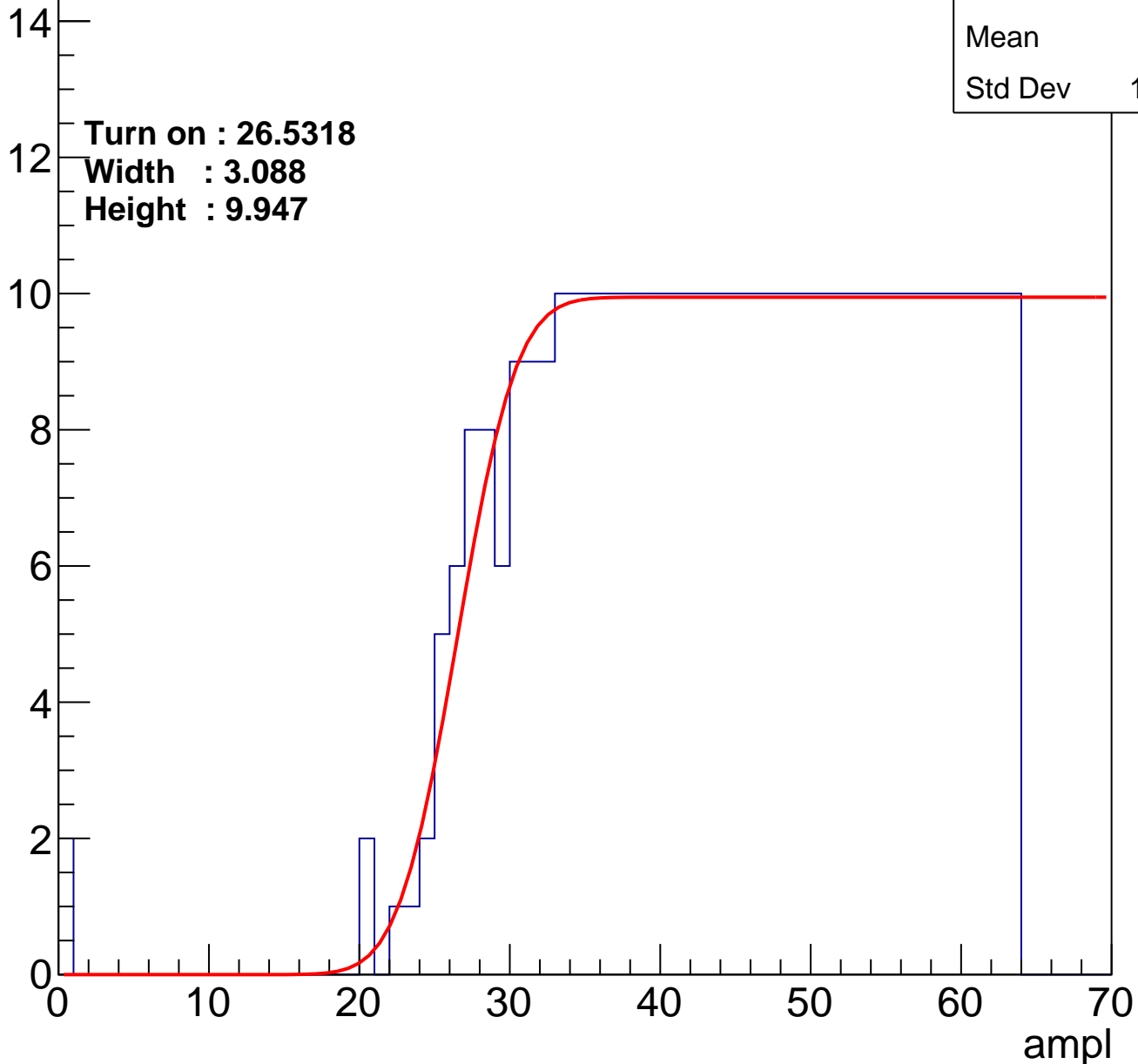
Entries	378
Mean	44.3
Std Dev	11.56

Turn on : 26.5318

Width : 3.088

Height : 9.947

Entry



B1L101S, U15-ch122

calib_packv5_042523_0143.root, FC#0, port D2

Entries	367
Mean	44.93
Std Dev	11.04

Turn on : 27.6749

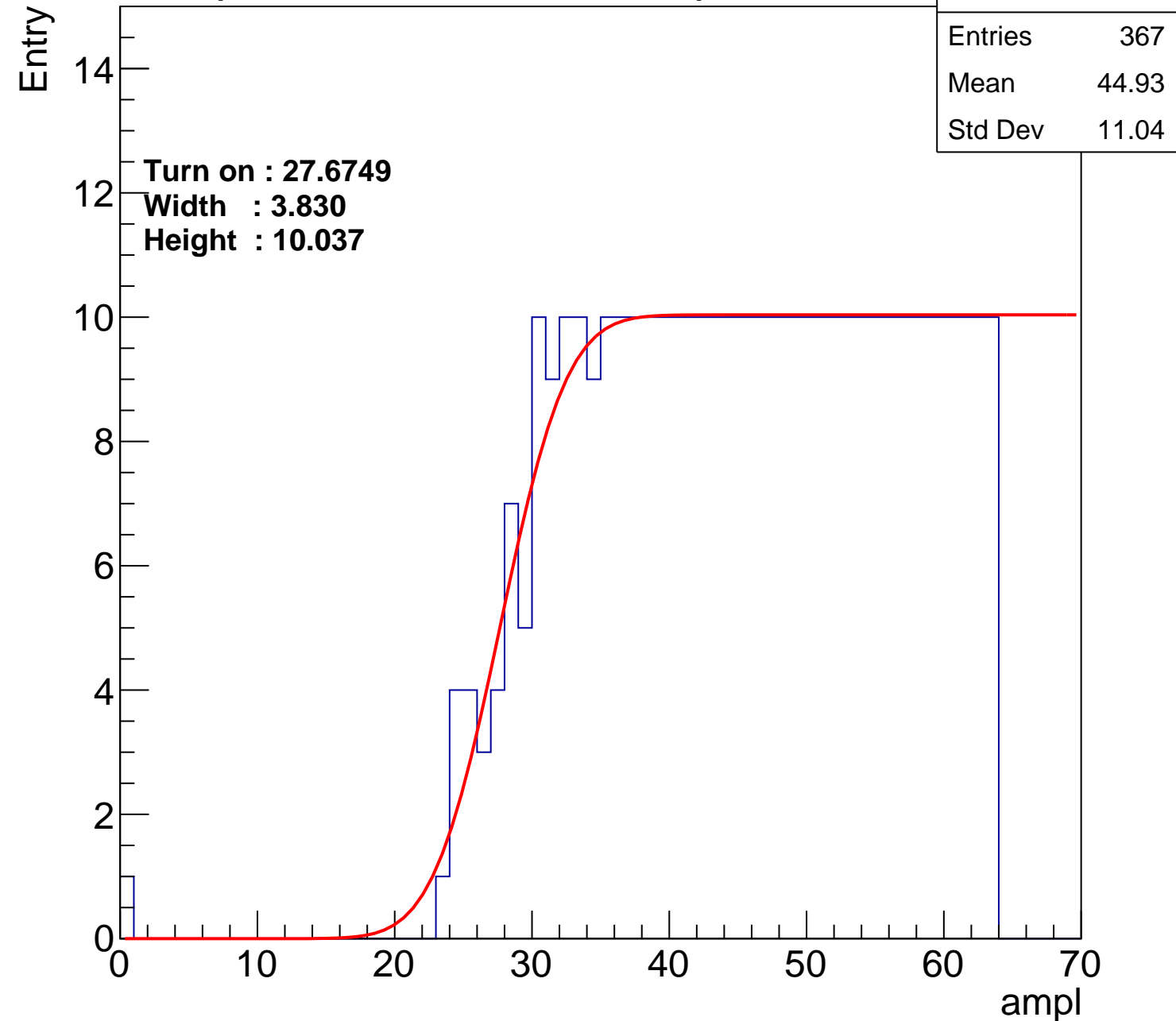
Width : 3.830

Height : 10.037

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch123

calib_packv5_042523_0143.root, FC#0, port D2

Entries	396
Mean	43.2
Std Dev	12.67

Turn on : 25.8959

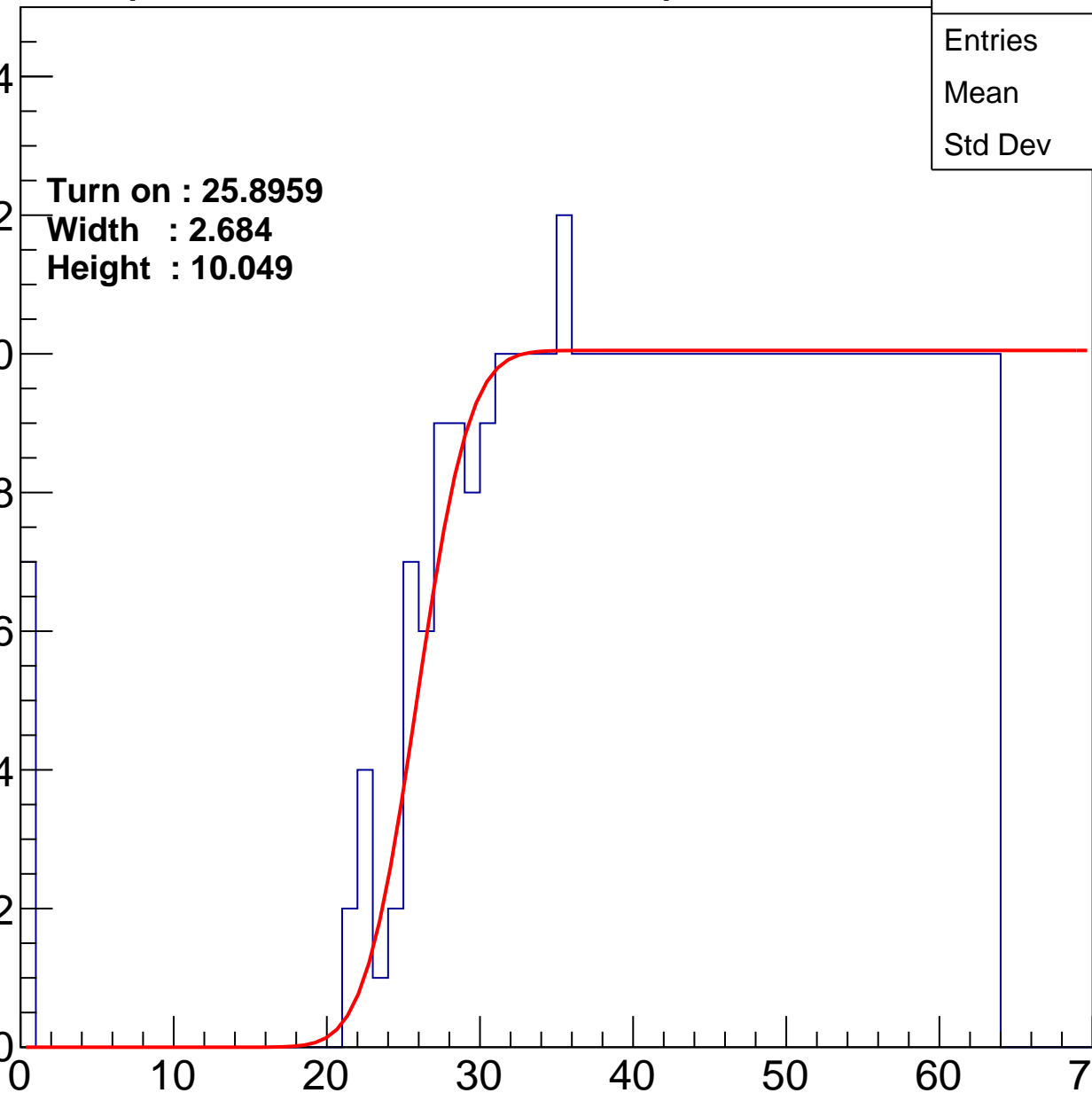
Width : 2.684

Height : 10.049

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch124

calib_packv5_042523_0143.root, FC#0, port D2

Entries	390
Mean	43.68
Std Dev	11.98

Turn on : 25.3513

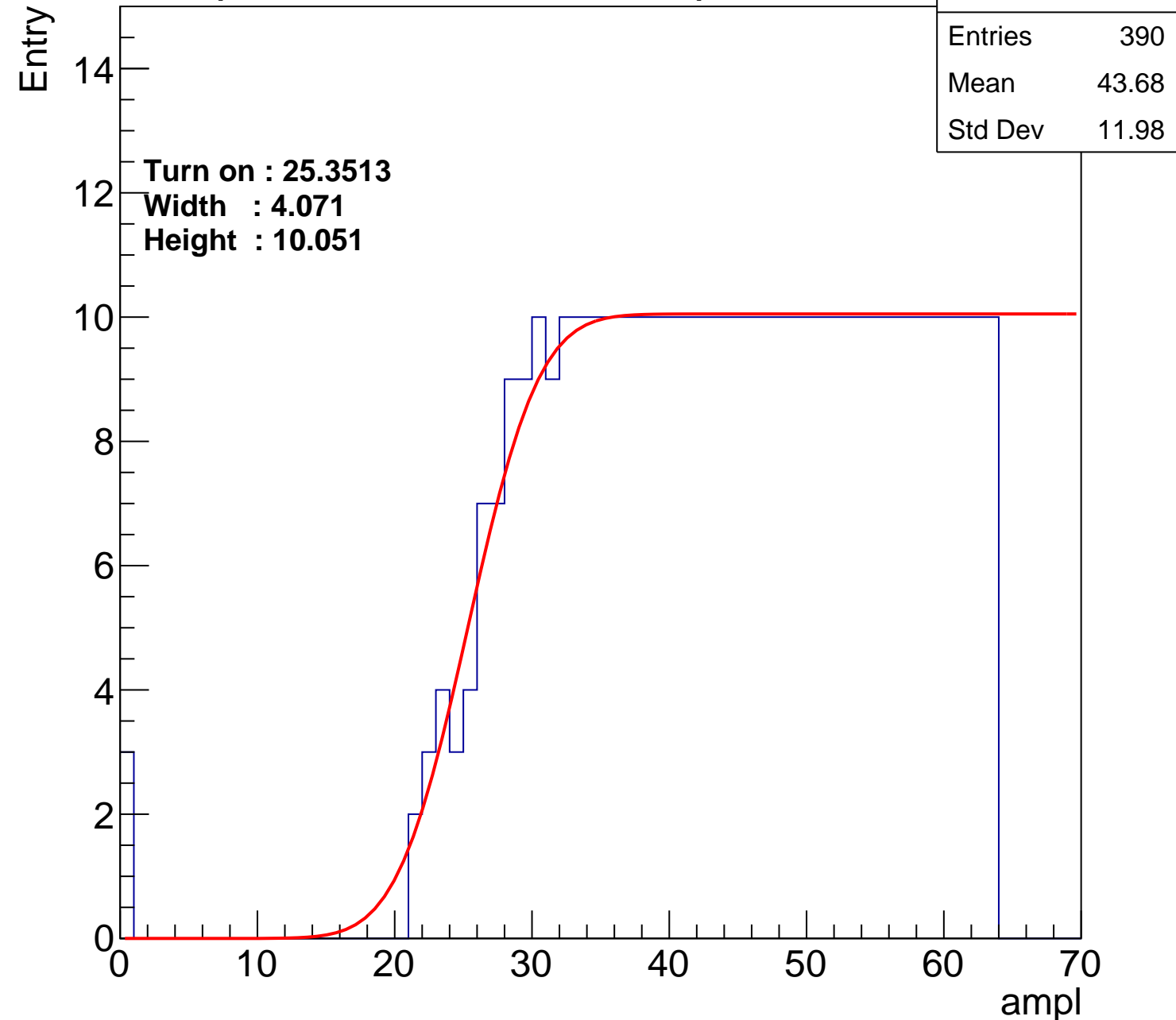
Width : 4.071

Height : 10.051

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch125

calib_packv5_042523_0143.root, FC#0, port D2

Entries	380
Mean	44.13
Std Dev	11.79

Turn on : 26.7156

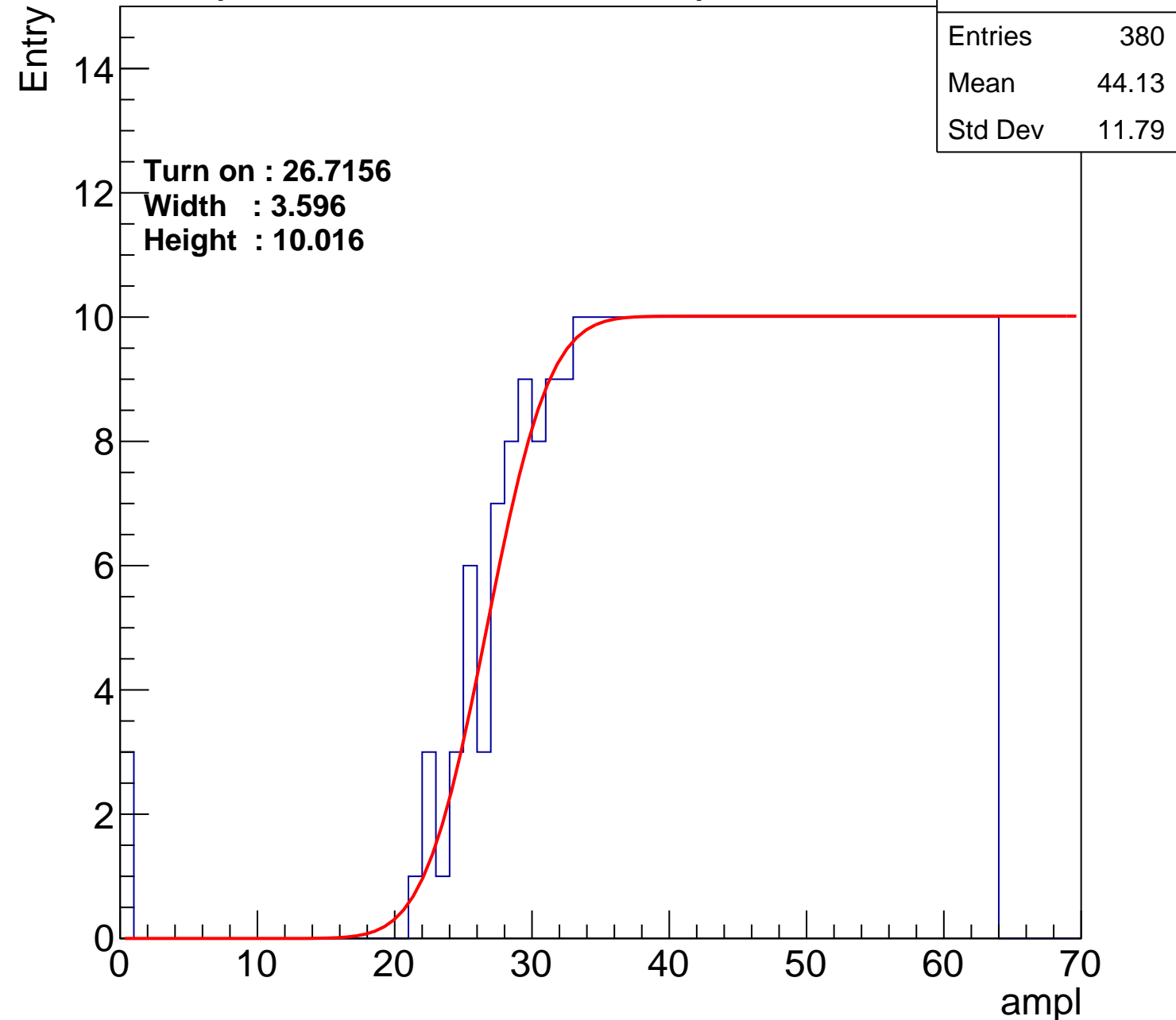
Width : 3.596

Height : 10.016

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch126

calib_packv5_042523_0143.root, FC#0, port D2

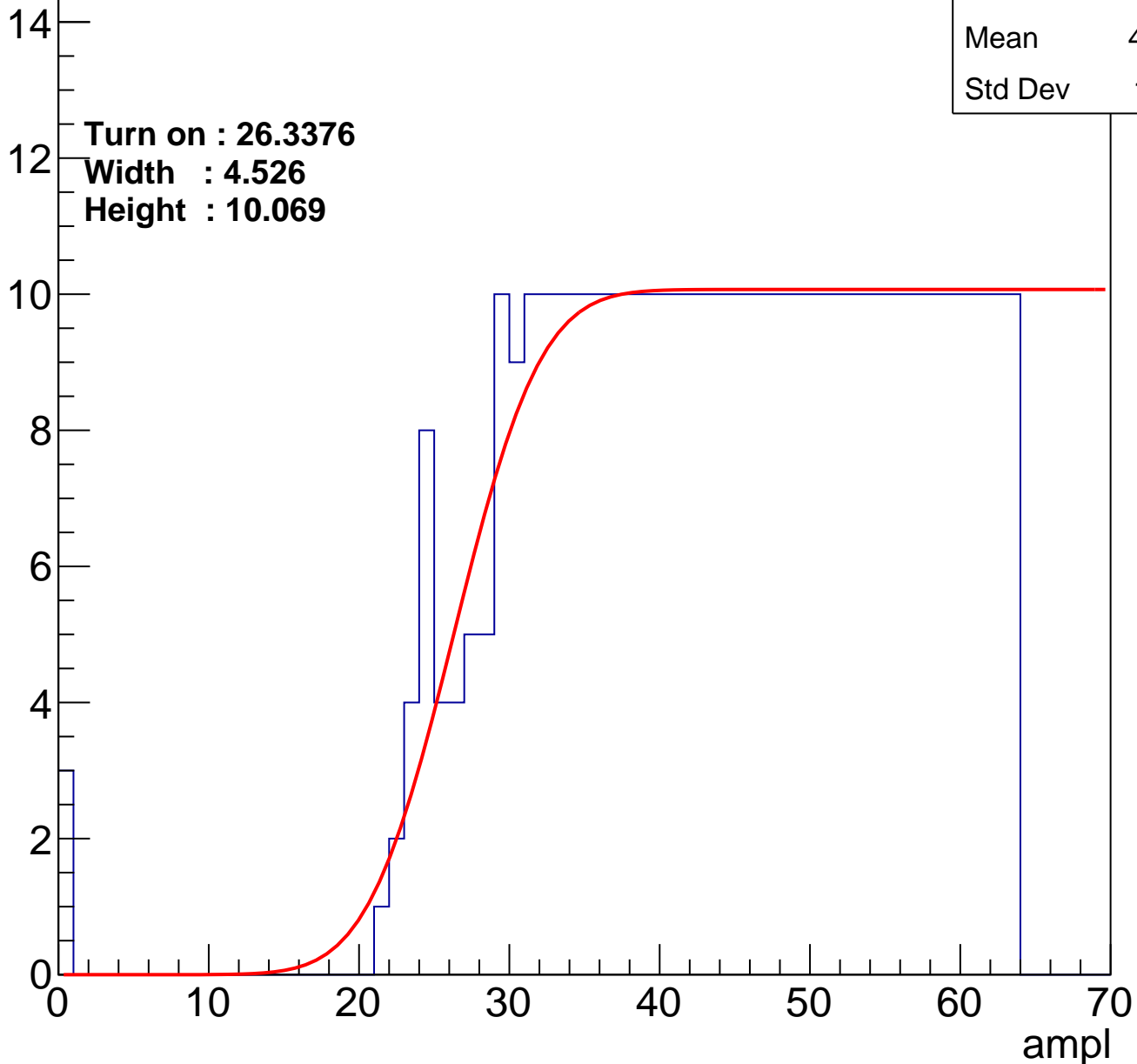
Entries	385
Mean	43.89
Std Dev	11.91

Turn on : 26.3376

Width : 4.526

Height : 10.069

Entry



B1L101S, U15-ch127

calib_packv5_042523_0143.root, FC#0, port D2

Entries	379
Mean	44.15
Std Dev	11.88

Turn on : 26.4466

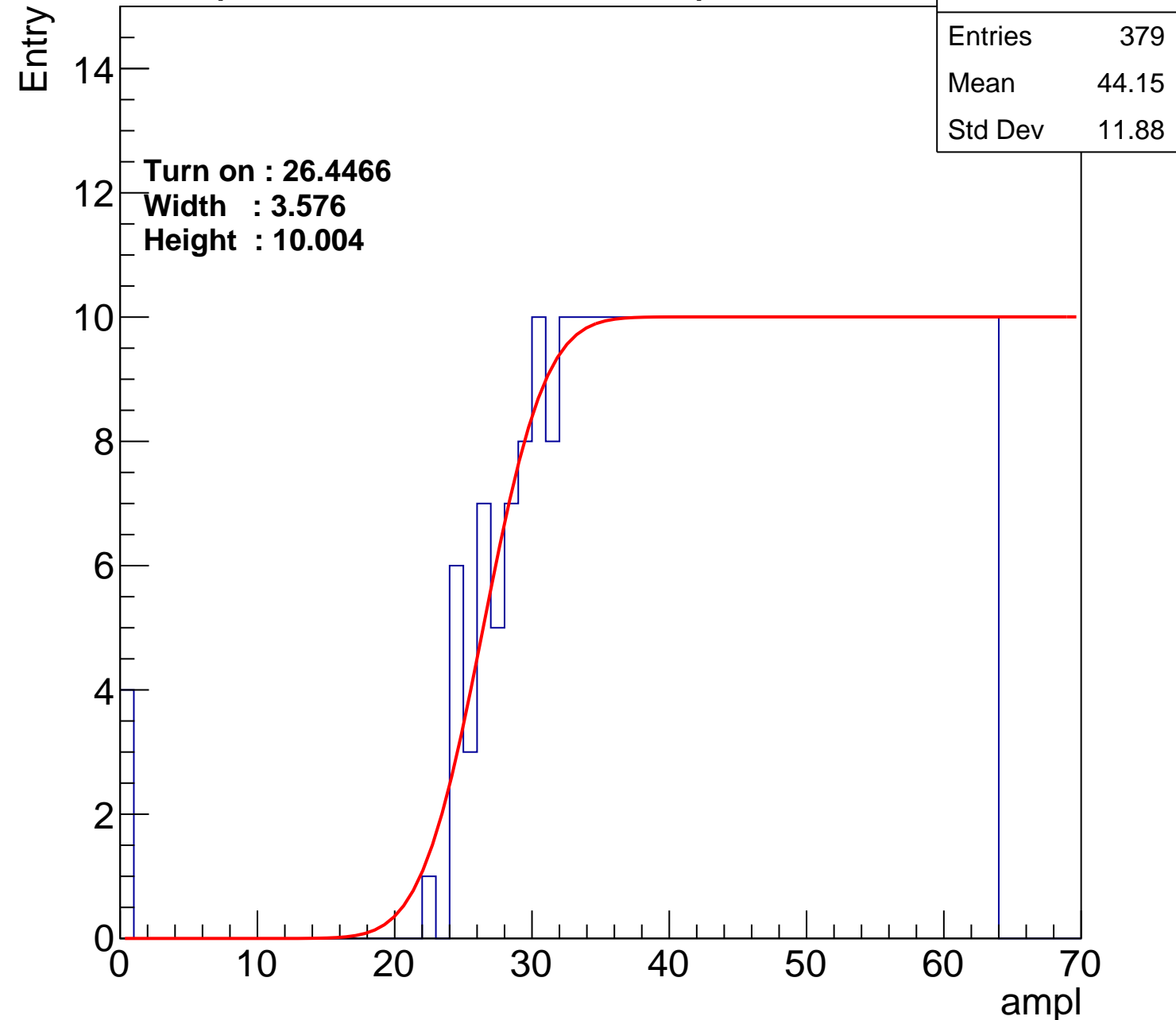
Width : 3.576

Height : 10.004

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U15-ch127

calib_packv5_042523_0143.root, FC#0, port D2

Entries	379
Mean	44.15
Std Dev	11.88

Turn on : 26.4466

Width : 3.576

Height : 10.004

Entry

14
12
10
8
6
4
2
0

ampl

