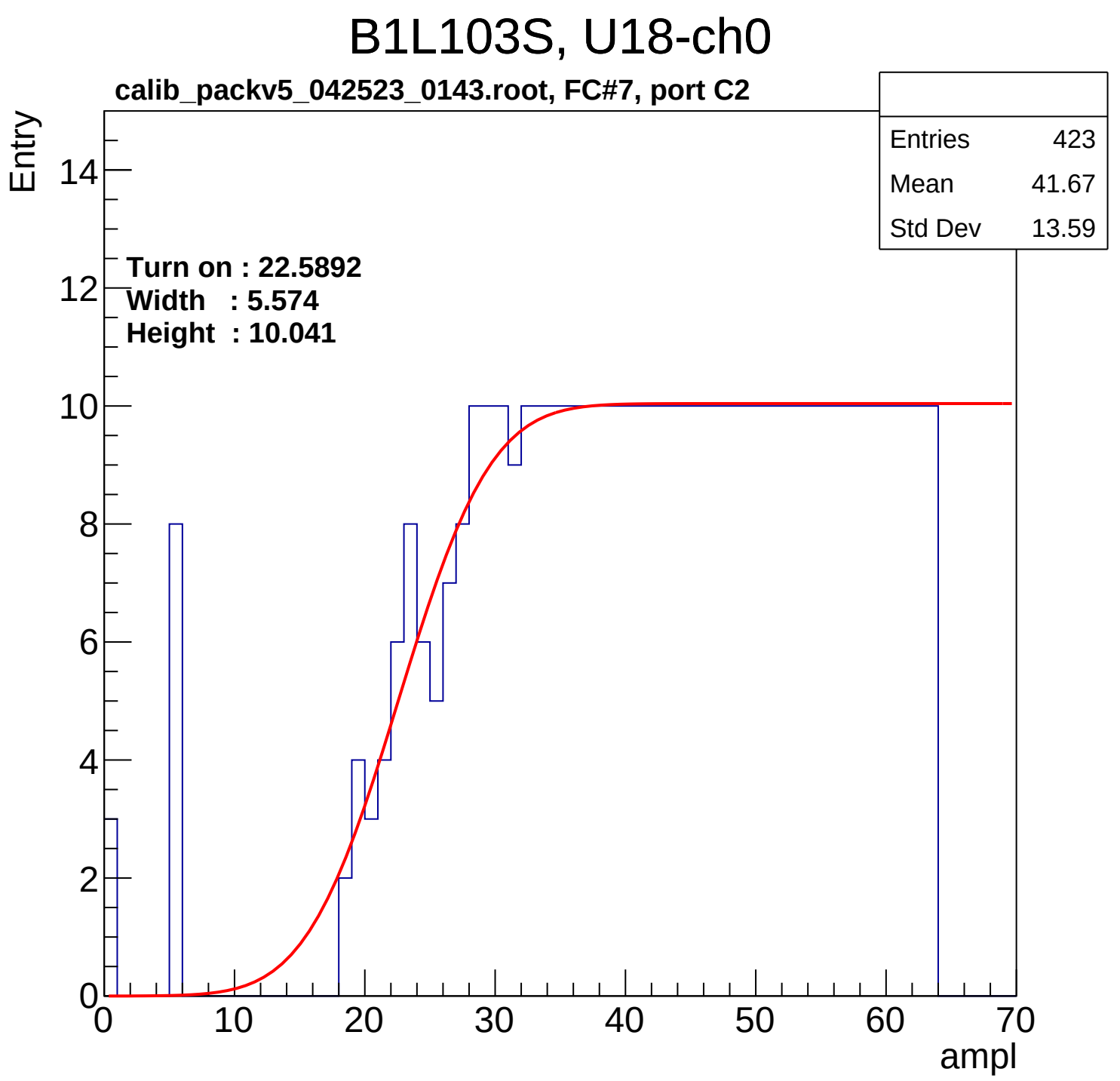
B1L103S, U18-ch0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 423
Mean 41.67
Std Dev 13.59
Turn on : 22.5892
Width : 5.574
Height : 10.041
Entry
ampl
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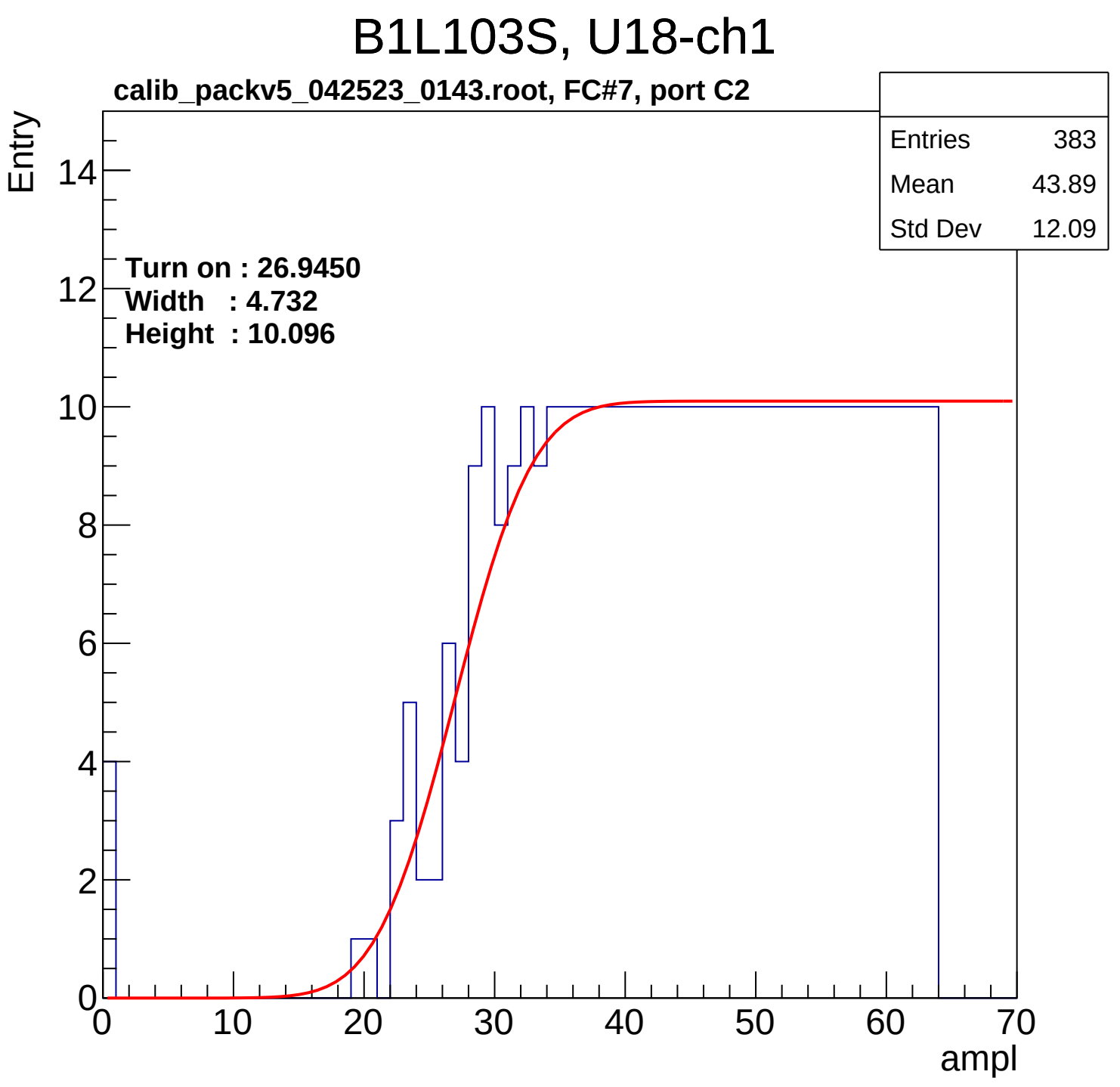
B1L103S, U18-ch1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 383
Mean 43.89
Std Dev 12.09
Turn on : 26.9450
Width : 4.732
Height : 10.096
Entry
ampl
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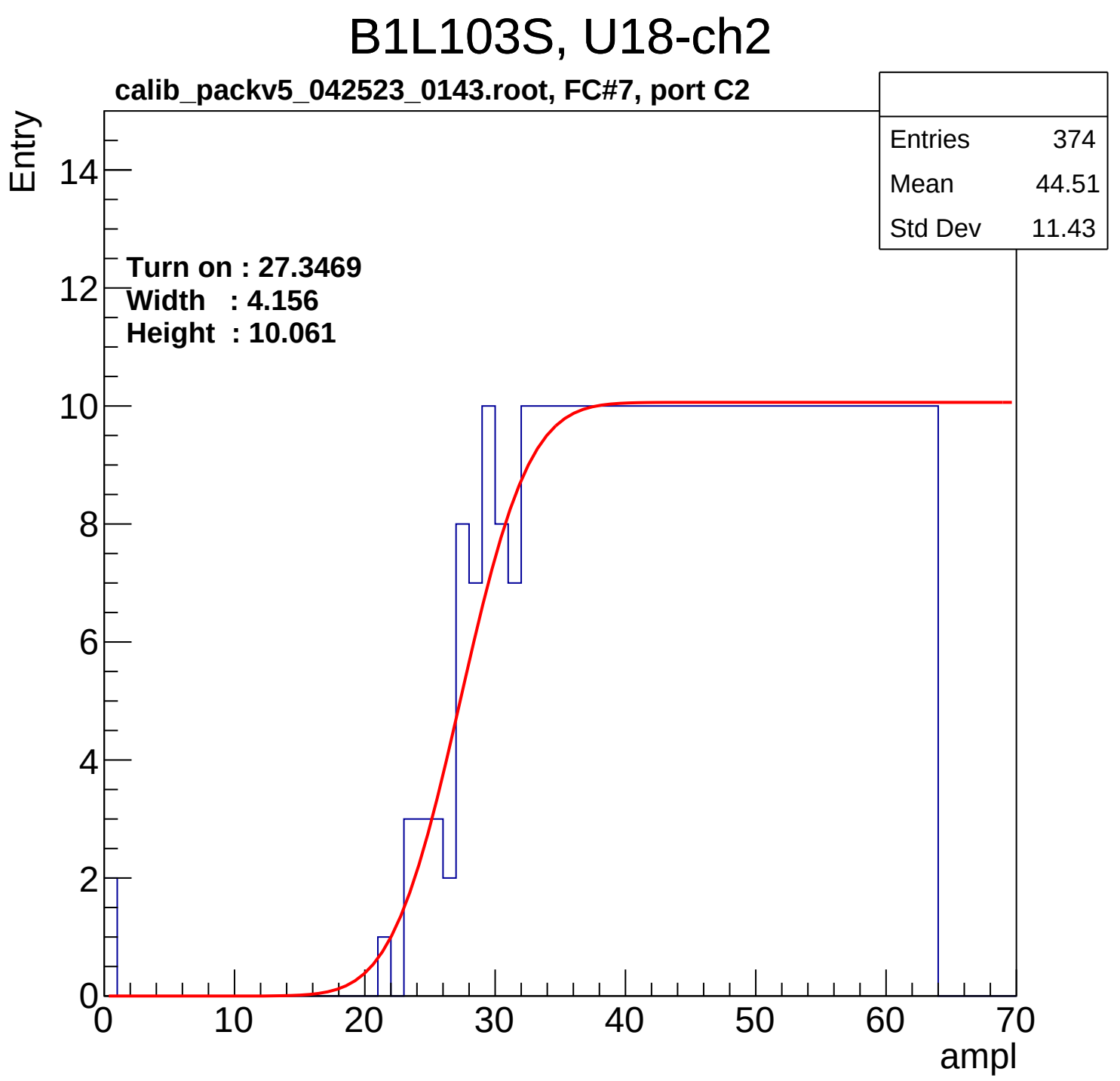
B1L103S, U18-ch2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 374
Mean 44.51
Std Dev 11.43
Turn on : 27.3469
Width : 4.156
Height : 10.061
Entry
ampl
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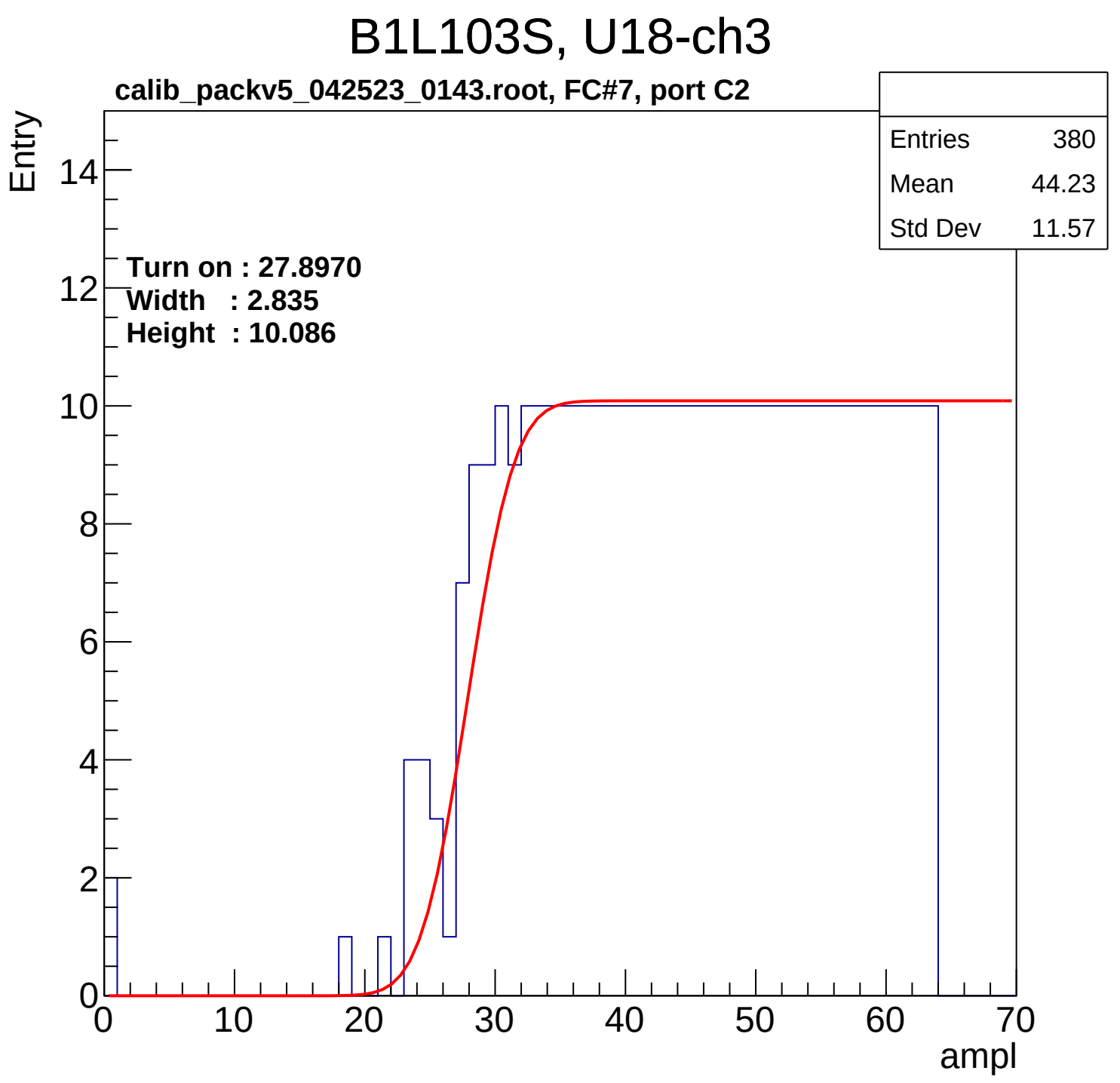
B1L103S, U18-ch3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 380
Mean 44.23
Std Dev 11.57
Turn on : 27.8970
Width : 2.835
Height : 10.086
Entry
ampl
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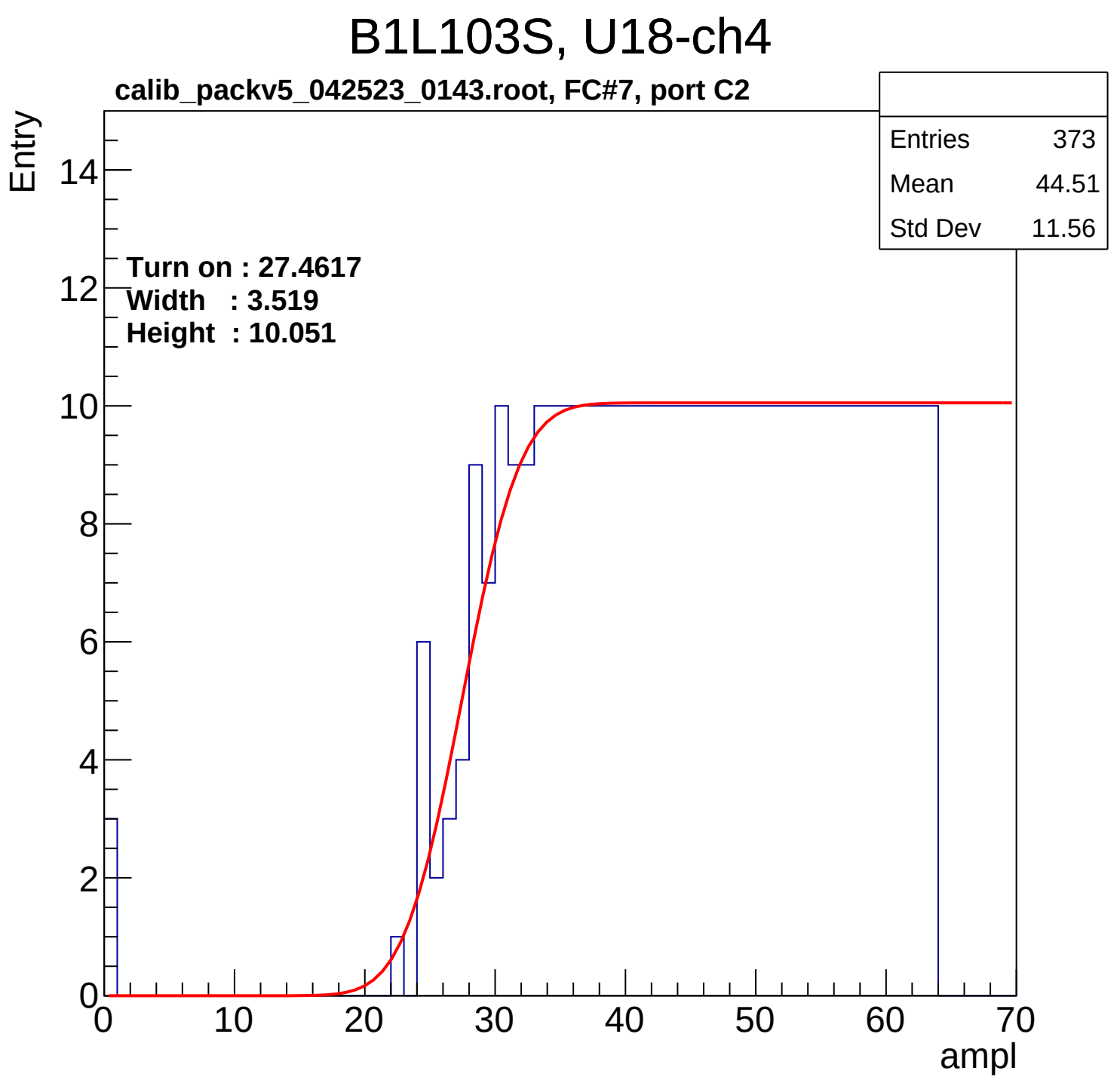
B1L103S, U18-ch4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 373
Mean 44.51
Std Dev 11.56
Turn on : 27.4617
Width : 3.519
Height : 10.051
Entry
ampl
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2
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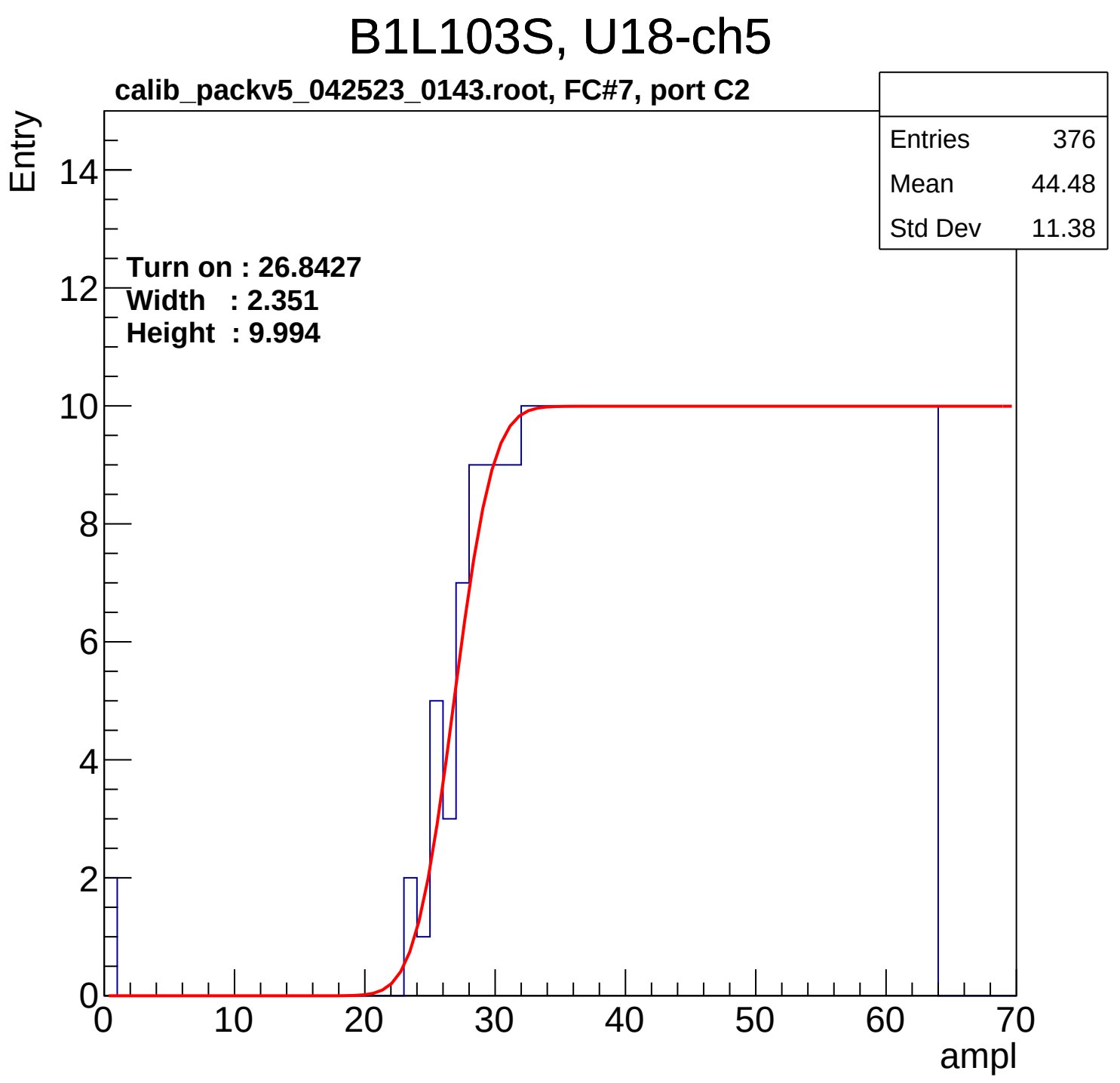
B1L103S, U18-ch5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 376
Mean 44.48
Std Dev 11.38
Turn on : 26.8427
Width : 2.351
Height : 9.994
Entry
ampl
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2
4
6
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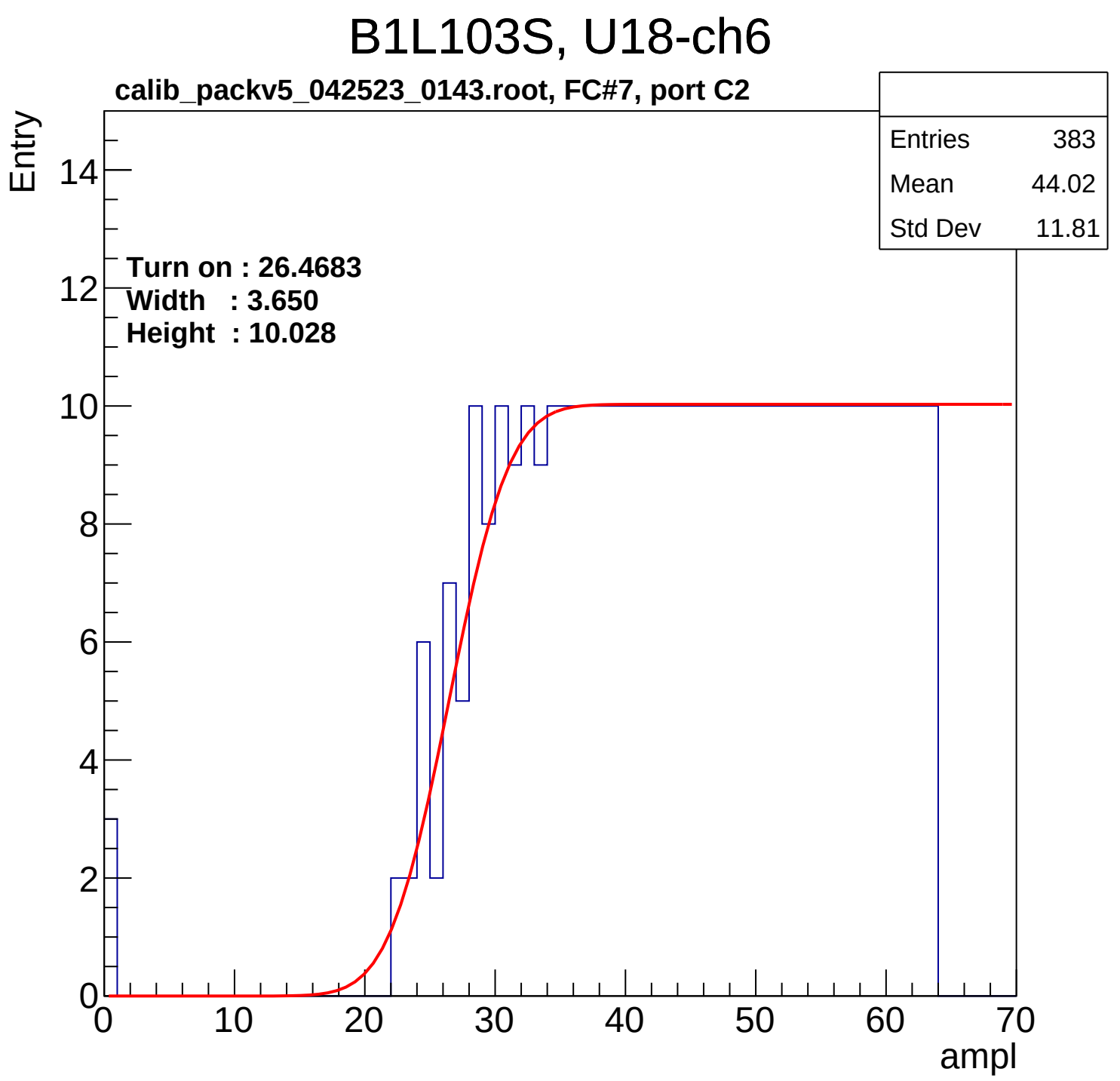
B1L103S, U18-ch6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 383
Mean 44.02
Std Dev 11.81
Turn on : 26.4683
Width : 3.650
Height : 10.028
Entry
ampl
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4
6
8
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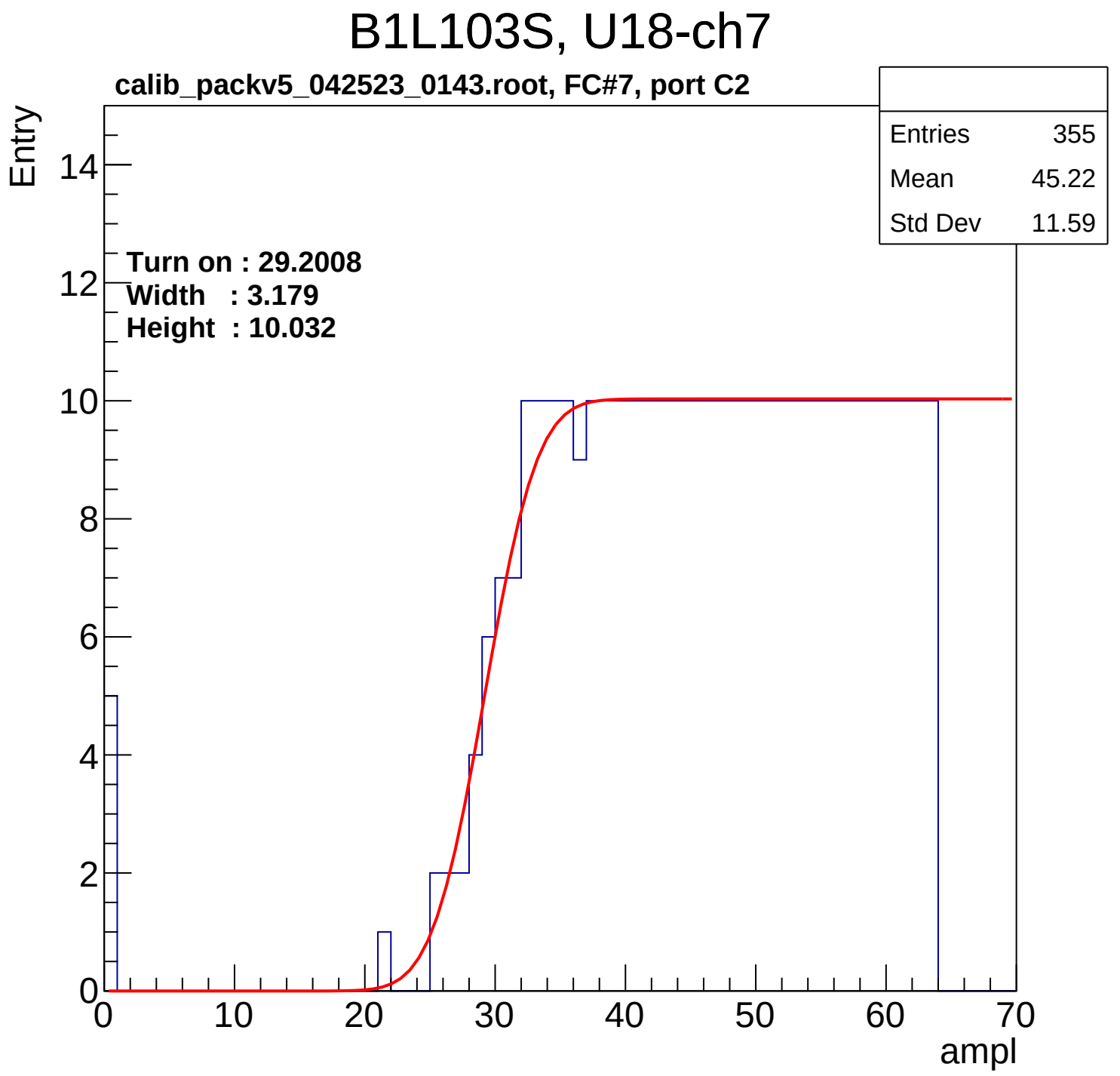
B1L103S, U18-ch7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 355
Mean 45.22
Std Dev 11.59
Turn on : 29.2008
Width : 3.179
Height : 10.032
Entry
ampl
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8
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0
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60
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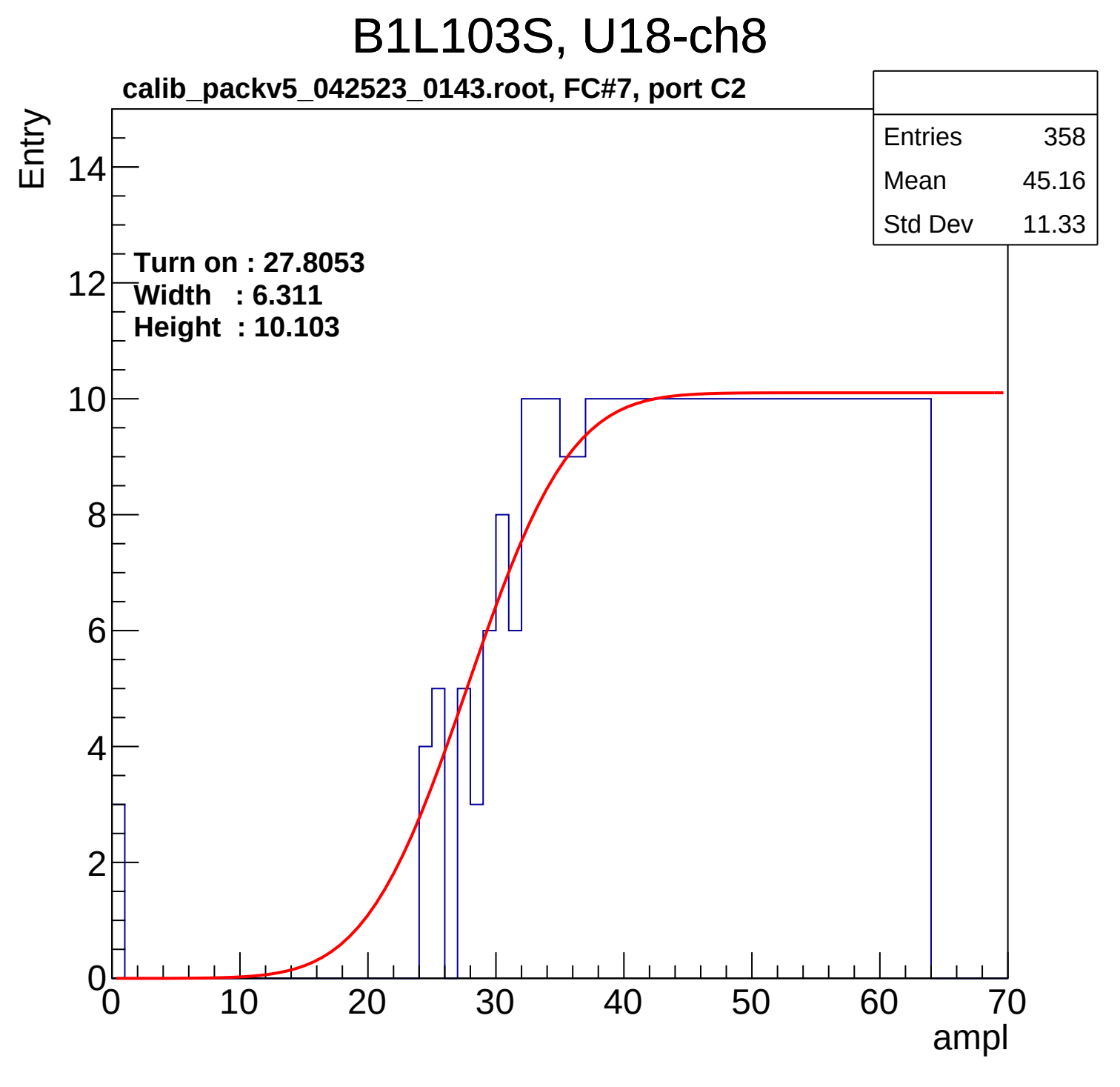
B1L103S, U18-ch8
calib_packv5_042523_0143.root, FC#7, port C2
Entries 358
Mean 45.16
Std Dev 11.33
Turn on : 27.8053
Width : 6.311
Height : 10.103
Entry
ampl
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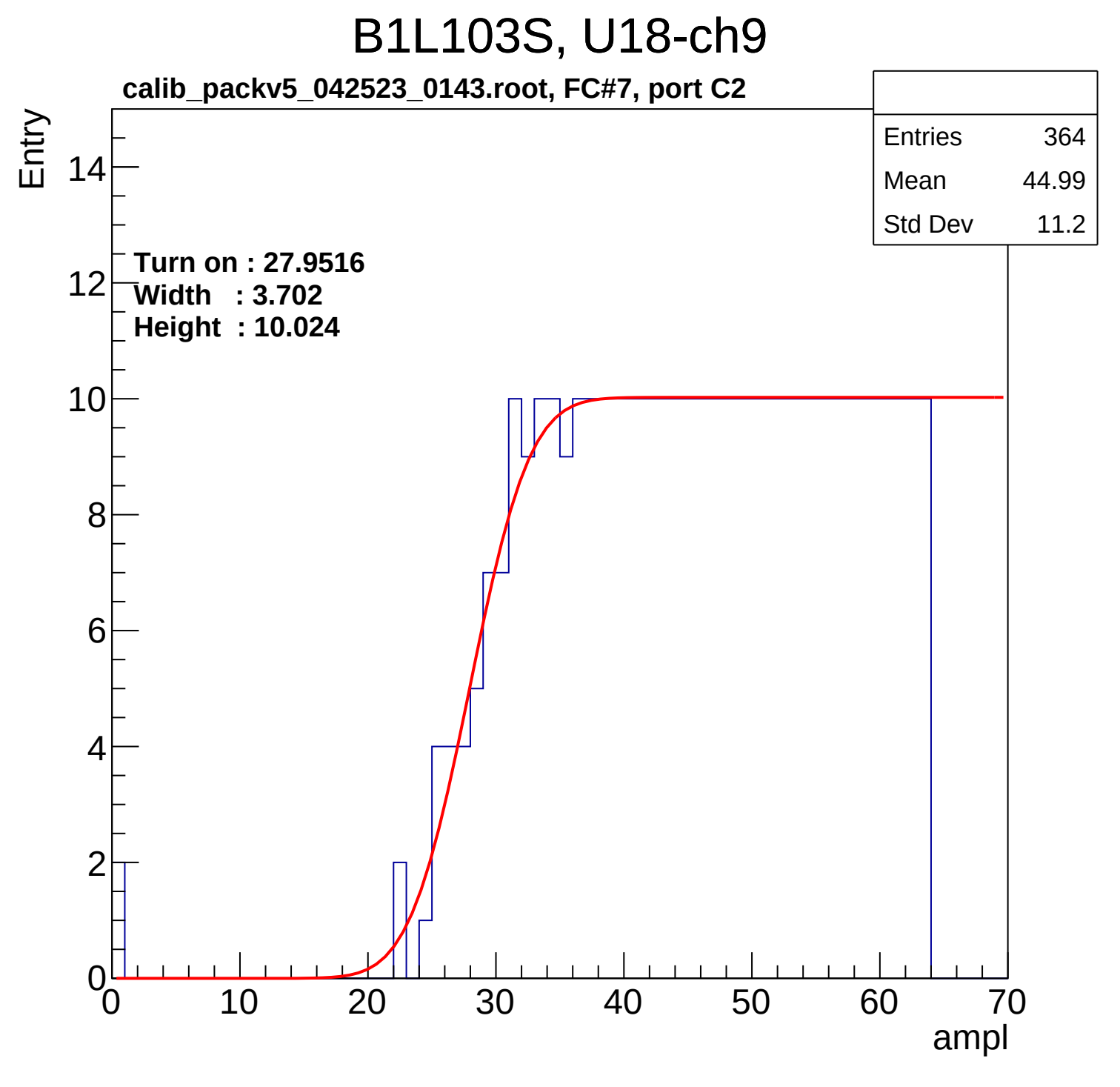
B1L103S, U18-ch9
calib_packv5_042523_0143.root, FC#7, port C2
Entries 364
Mean 44.99
Std Dev 11.2
Turn on : 27.9516
Width : 3.702
Height : 10.024
Entry
ampl
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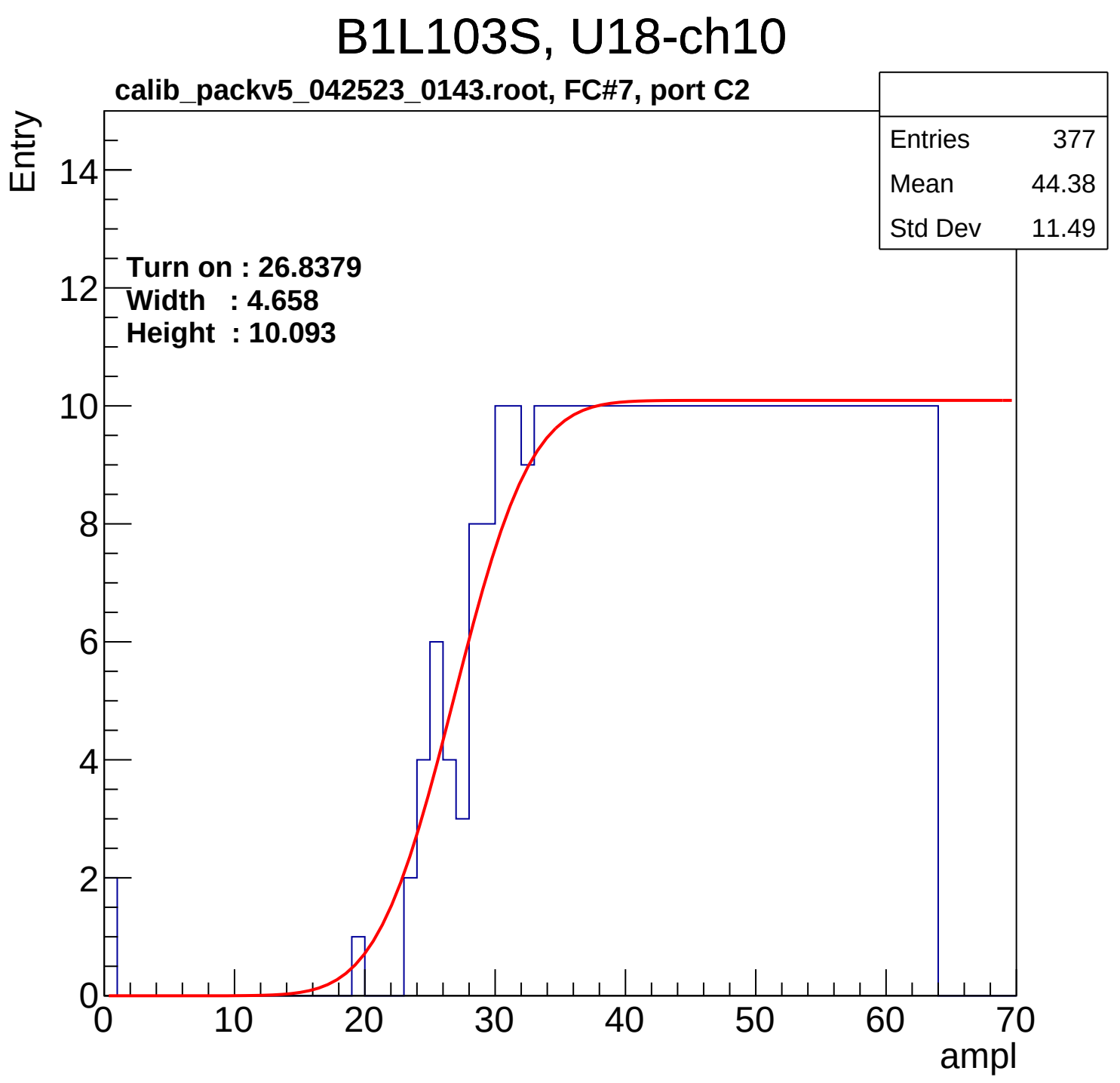
B1L103S, U18-ch10
calib_packv5_042523_0143.root, FC#7, port C2
Entries 377
Mean 44.38
Std Dev 11.49
Turn on : 26.8379
Width : 4.658
Height : 10.093
Entry
ampl
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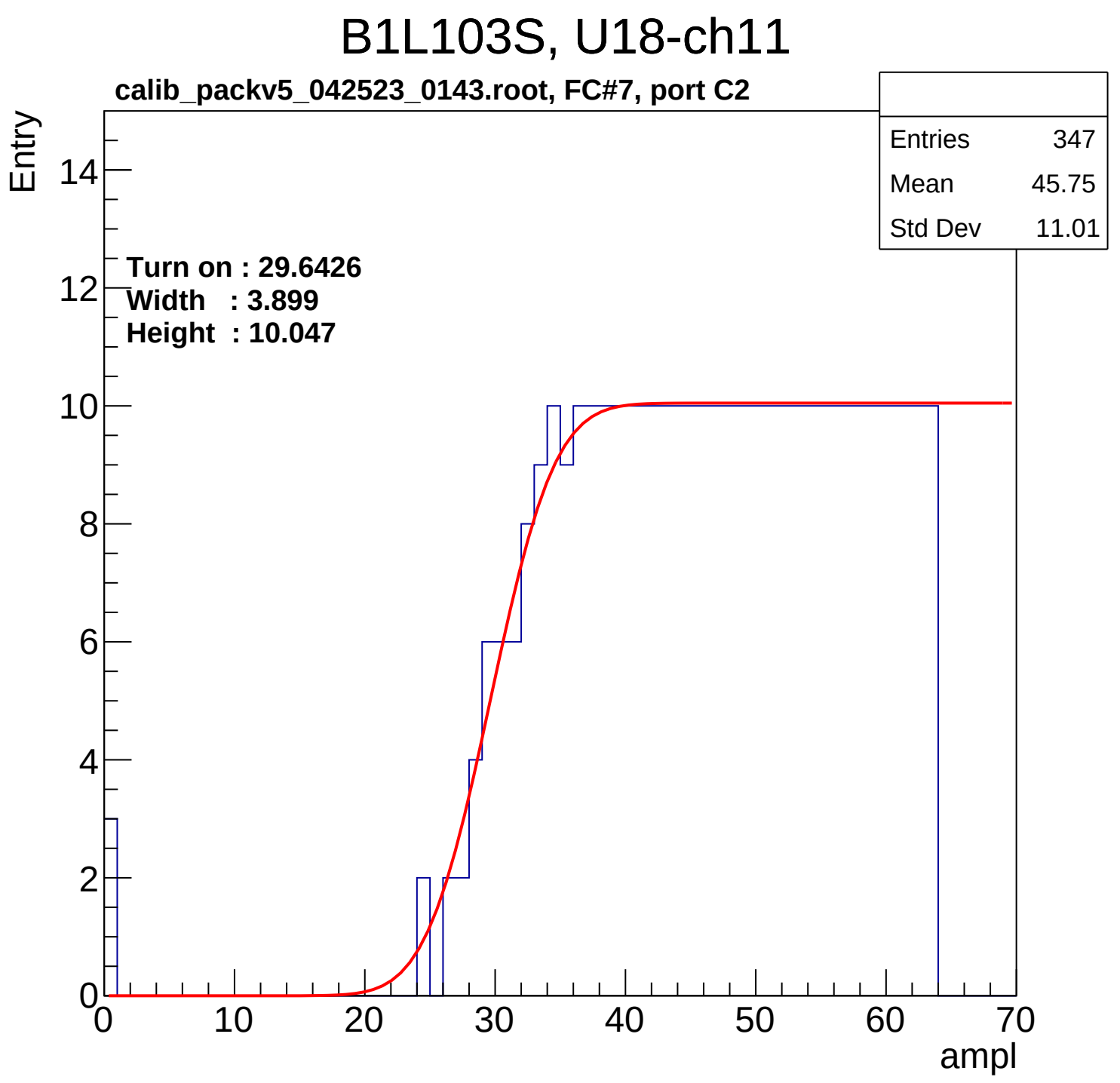
B1L103S, U18-ch11
calib_packv5_042523_0143.root, FC#7, port C2
Entries 347
Mean 45.75
Std Dev 11.01
Turn on : 29.6426
Width : 3.899
Height : 10.047
Entry
ampl
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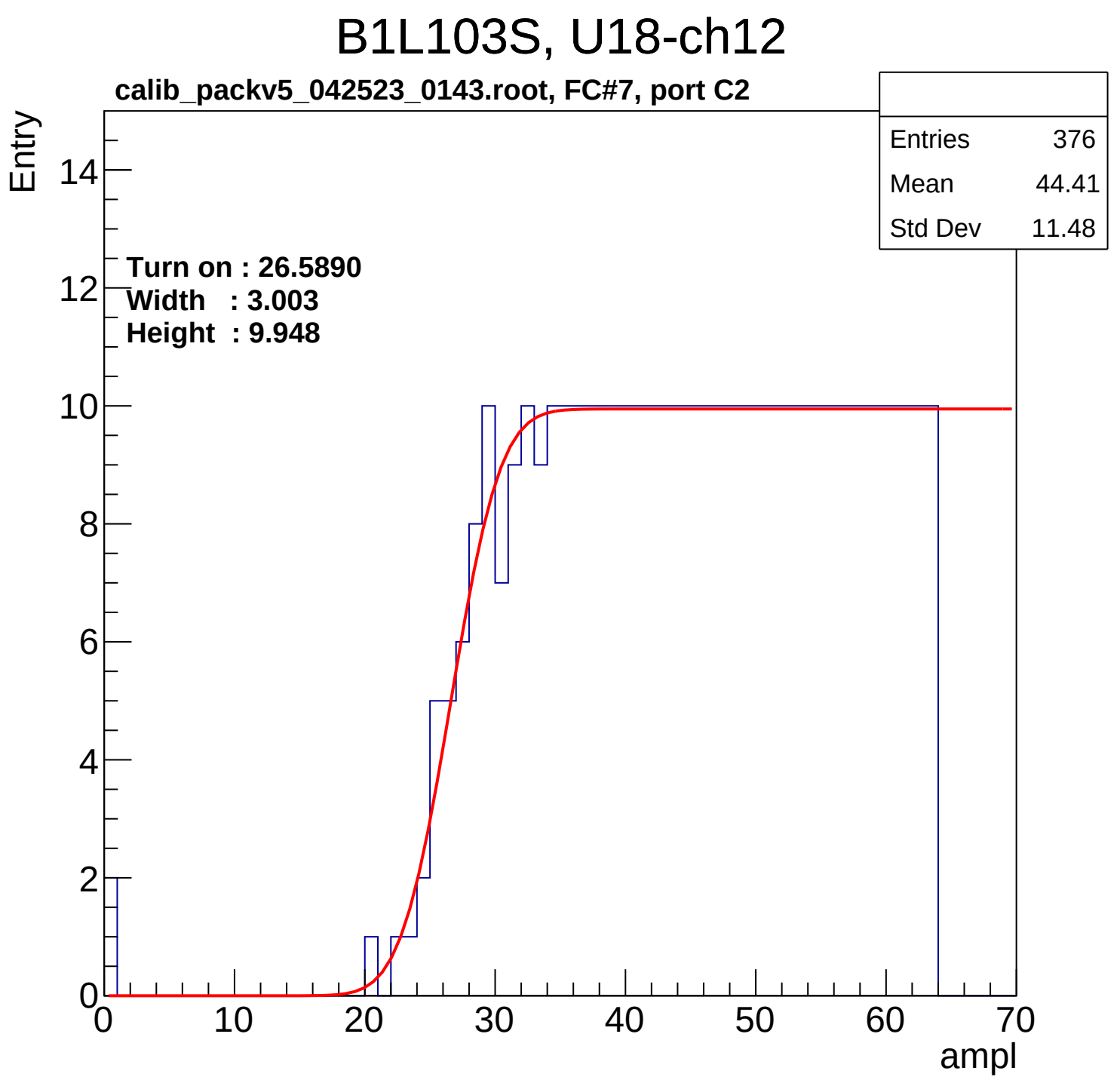
B1L103S, U18-ch12
calib_packv5_042523_0143.root, FC#7, port C2
Entries 376
Mean 44.41
Std Dev 11.48
Turn on : 26.5890
Width : 3.003
Height : 9.948
Entry
ampl
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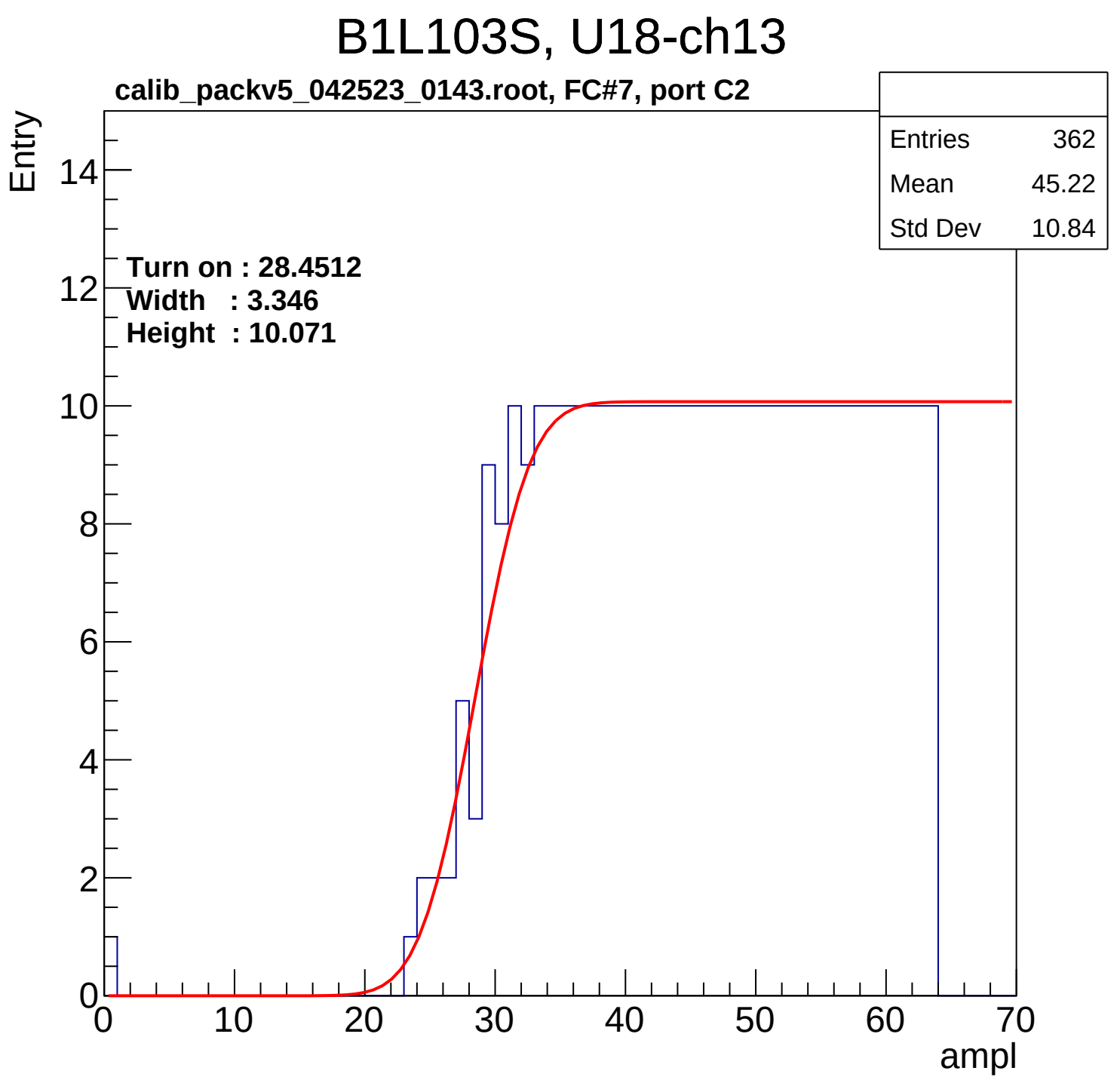
B1L103S, U18-ch13
calib_packv5_042523_0143.root, FC#7, port C2
Entries 362
Mean 45.22
Std Dev 10.84
Turn on : 28.4512
Width : 3.346
Height : 10.071
Entry
ampl
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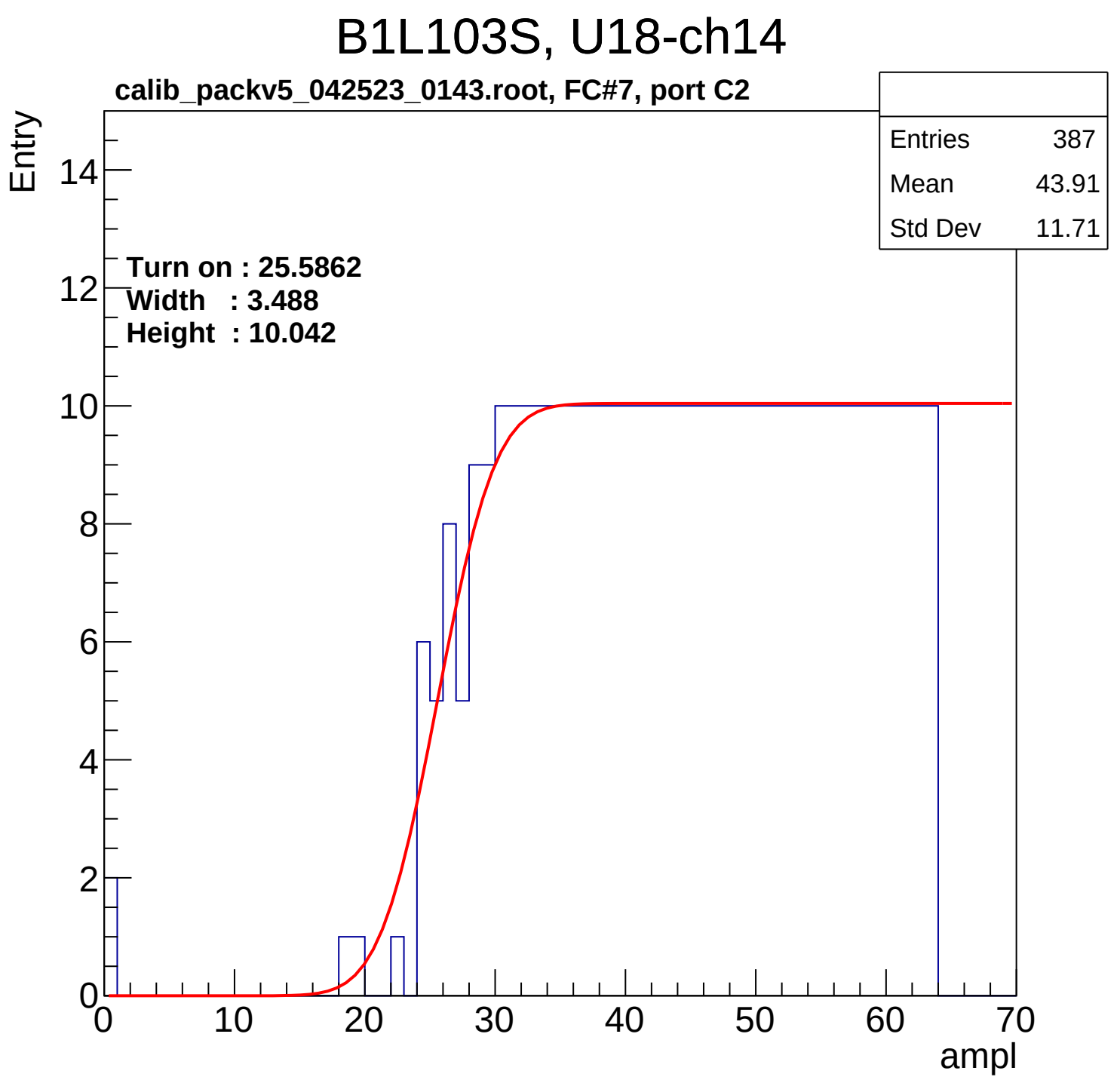
B1L103S, U18-ch14
calib_packv5_042523_0143.root, FC#7, port C2
Entries 387
Mean 43.91
Std Dev 11.71
Turn on : 25.5862
Width : 3.488
Height : 10.042
Entry
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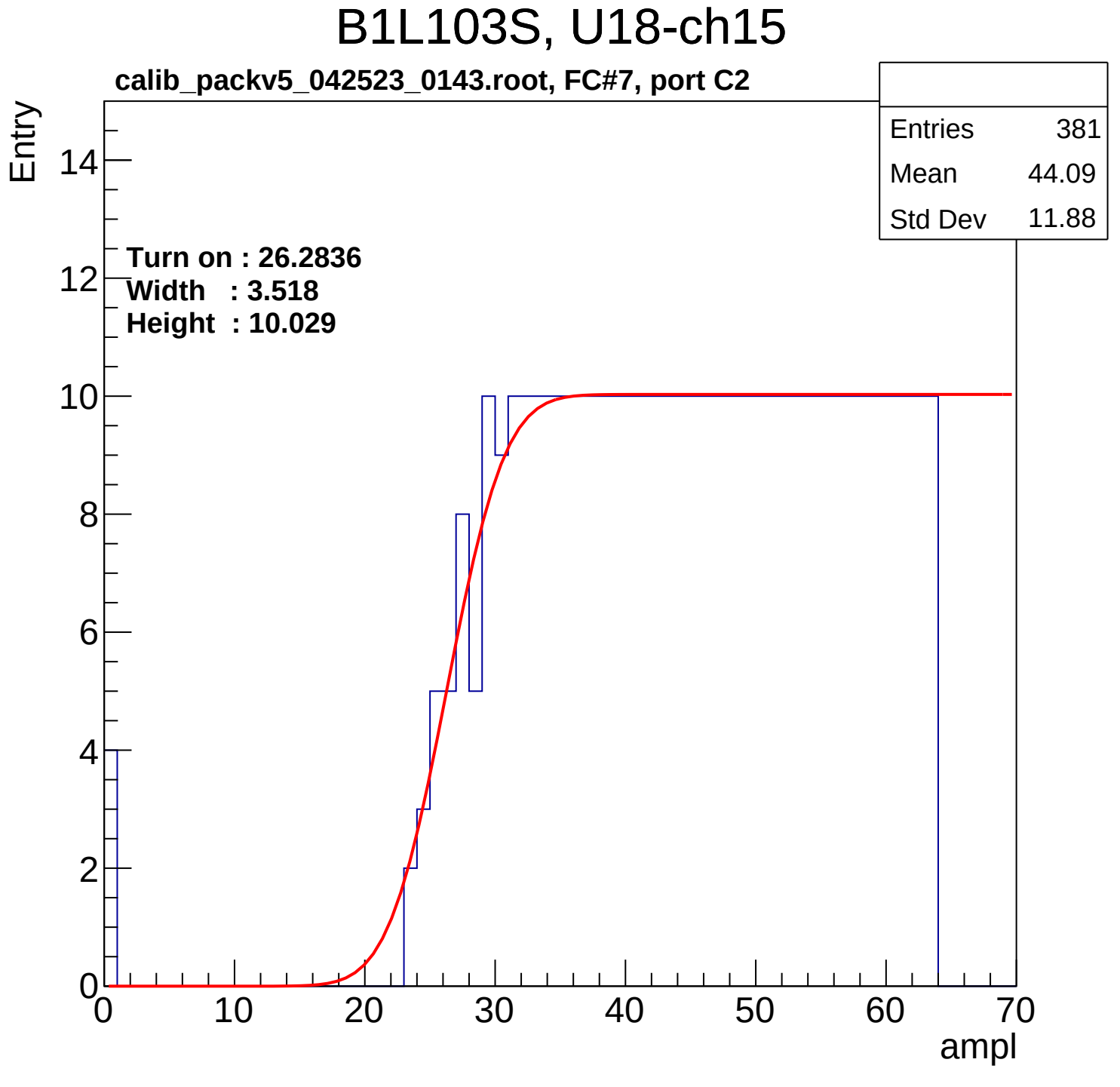
B1L103S, U18-ch15
calib_packv5_042523_0143.root, FC#7, port C2
Entries 381
Mean 44.09
Std Dev 11.88
Turn on : 26.2836
Width : 3.518
Height : 10.029
Entry
ampl
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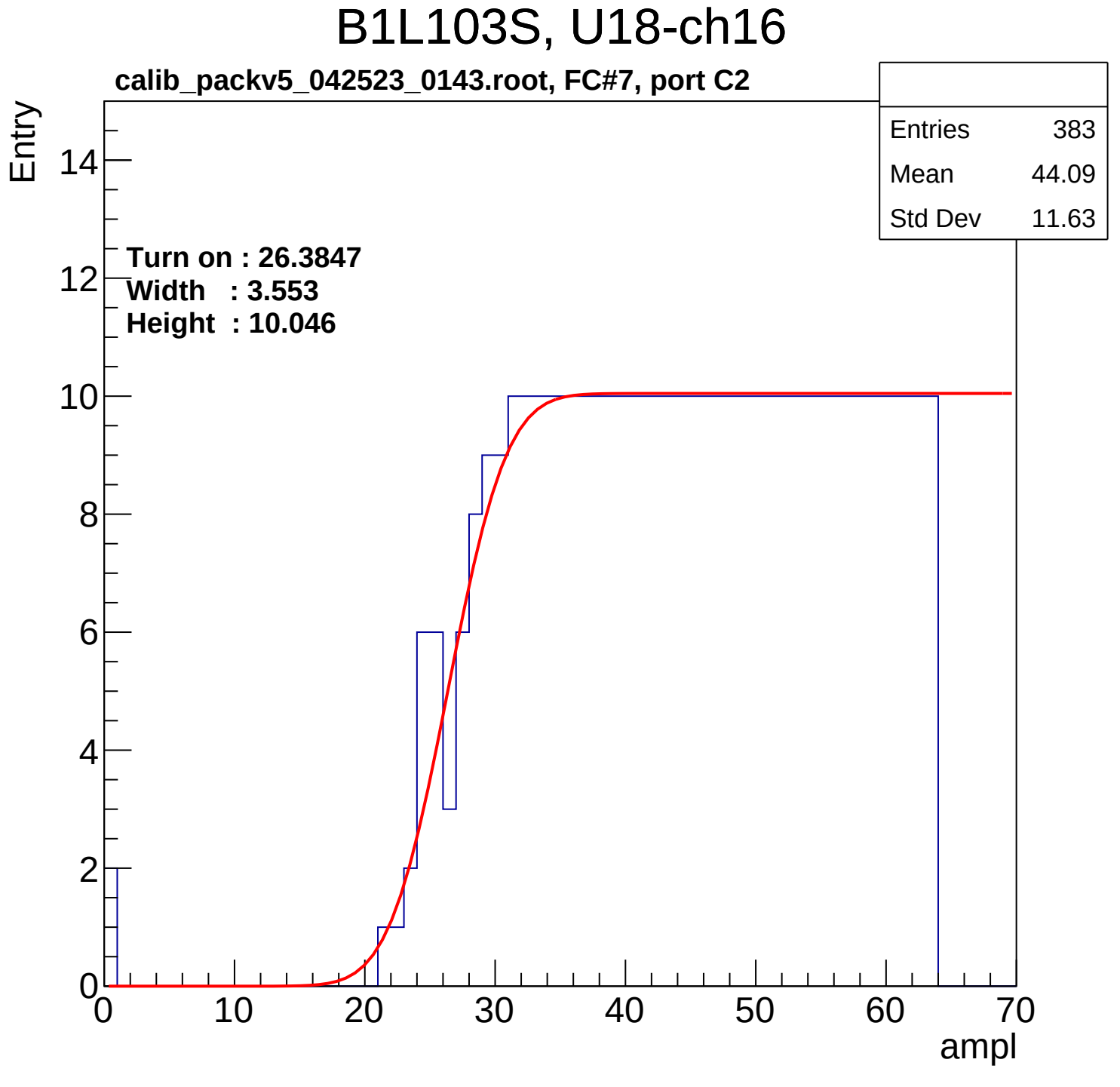
B1L103S, U18-ch16
calib_packv5_042523_0143.root, FC#7, port C2
Entries 383
Mean 44.09
Std Dev 11.63
Turn on : 26.3847
Width : 3.553
Height : 10.046
Entry
ampl
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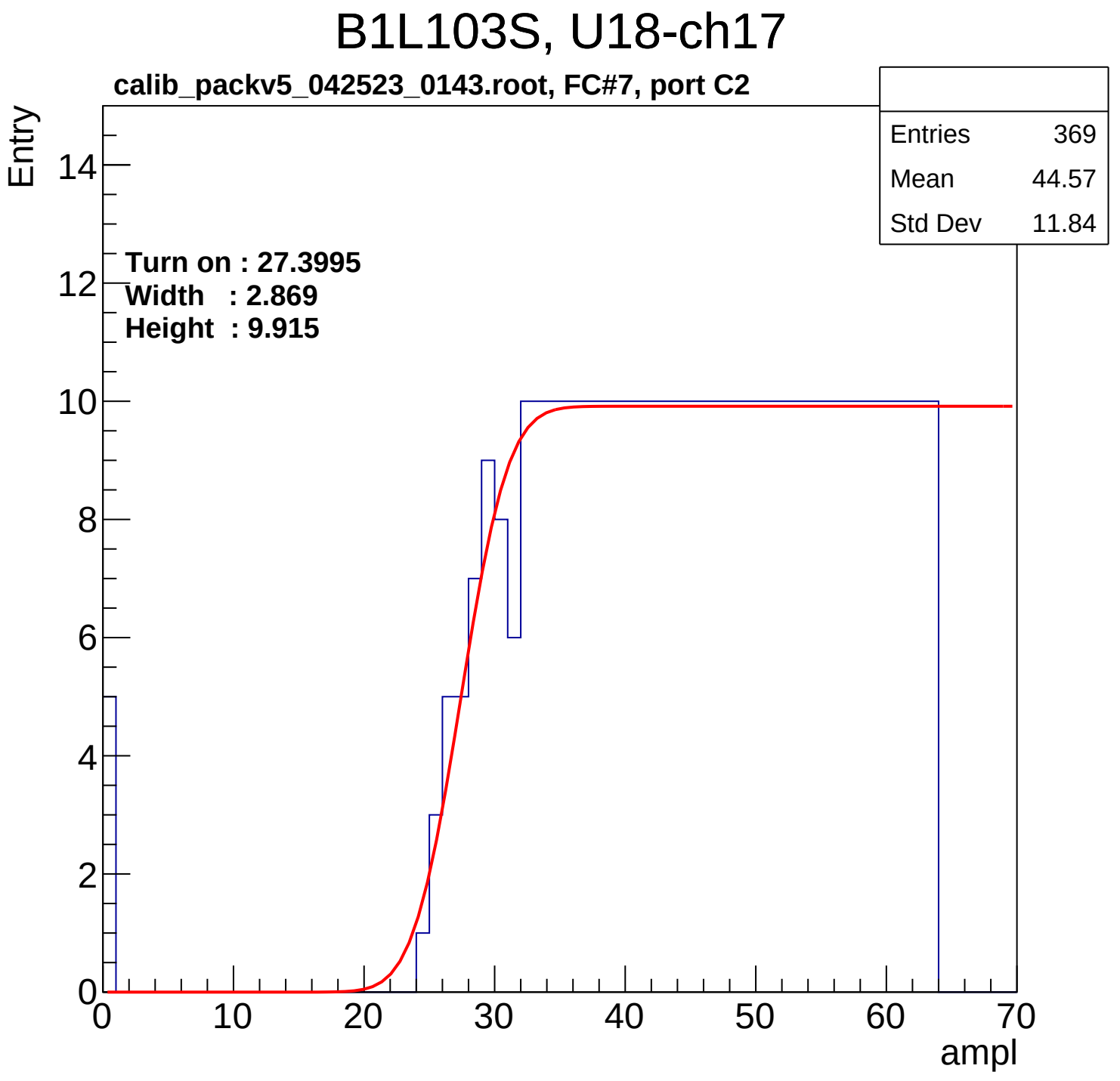
B1L103S, U18-ch17
calib_packv5_042523_0143.root, FC#7, port C2
Entries 369
Mean 44.57
Std Dev 11.84
Turn on : 27.3995
Width : 2.869
Height : 9.915
Entry
ampl
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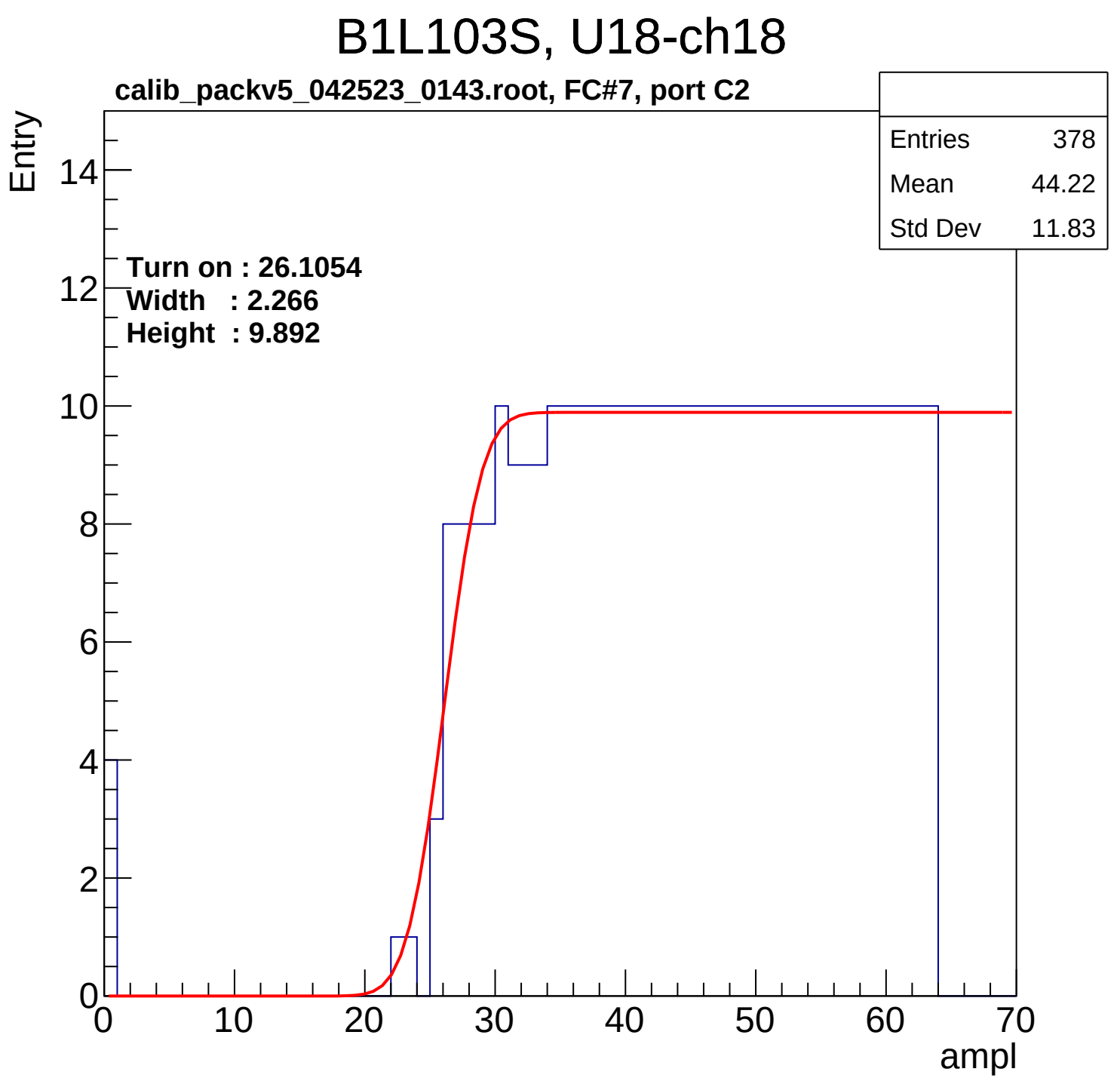
B1L103S, U18-ch18
calib_packv5_042523_0143.root, FC#7, port C2
Entries 378
Mean 44.22
Std Dev 11.83
Turn on : 26.1054
Width : 2.266
Height : 9.892
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ampl
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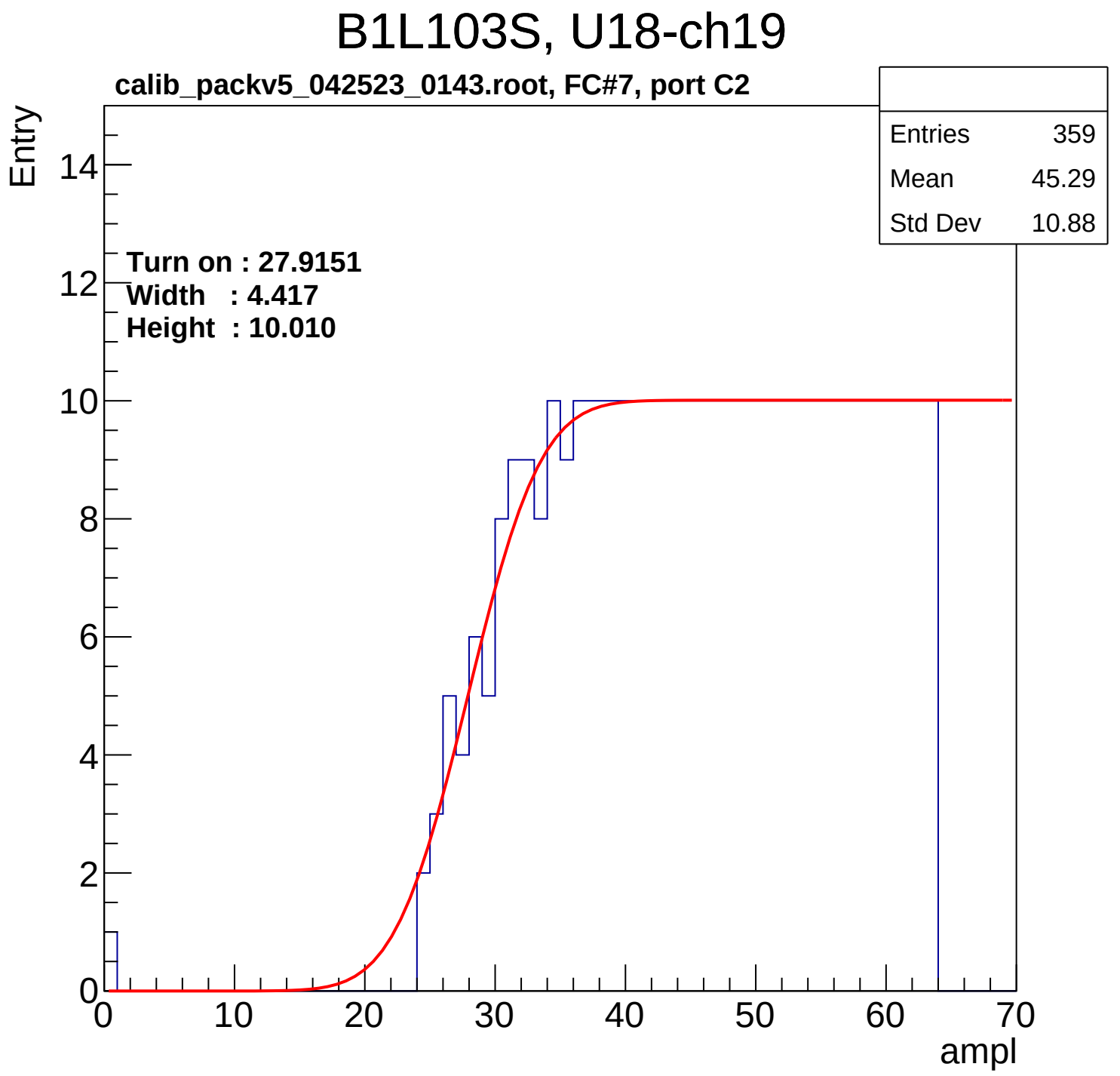
B1L103S, U18-ch19
calib_packv5_042523_0143.root, FC#7, port C2
Entries 359
Mean 45.29
Std Dev 10.88
Turn on : 27.9151
Width : 4.417
Height : 10.010
Entry
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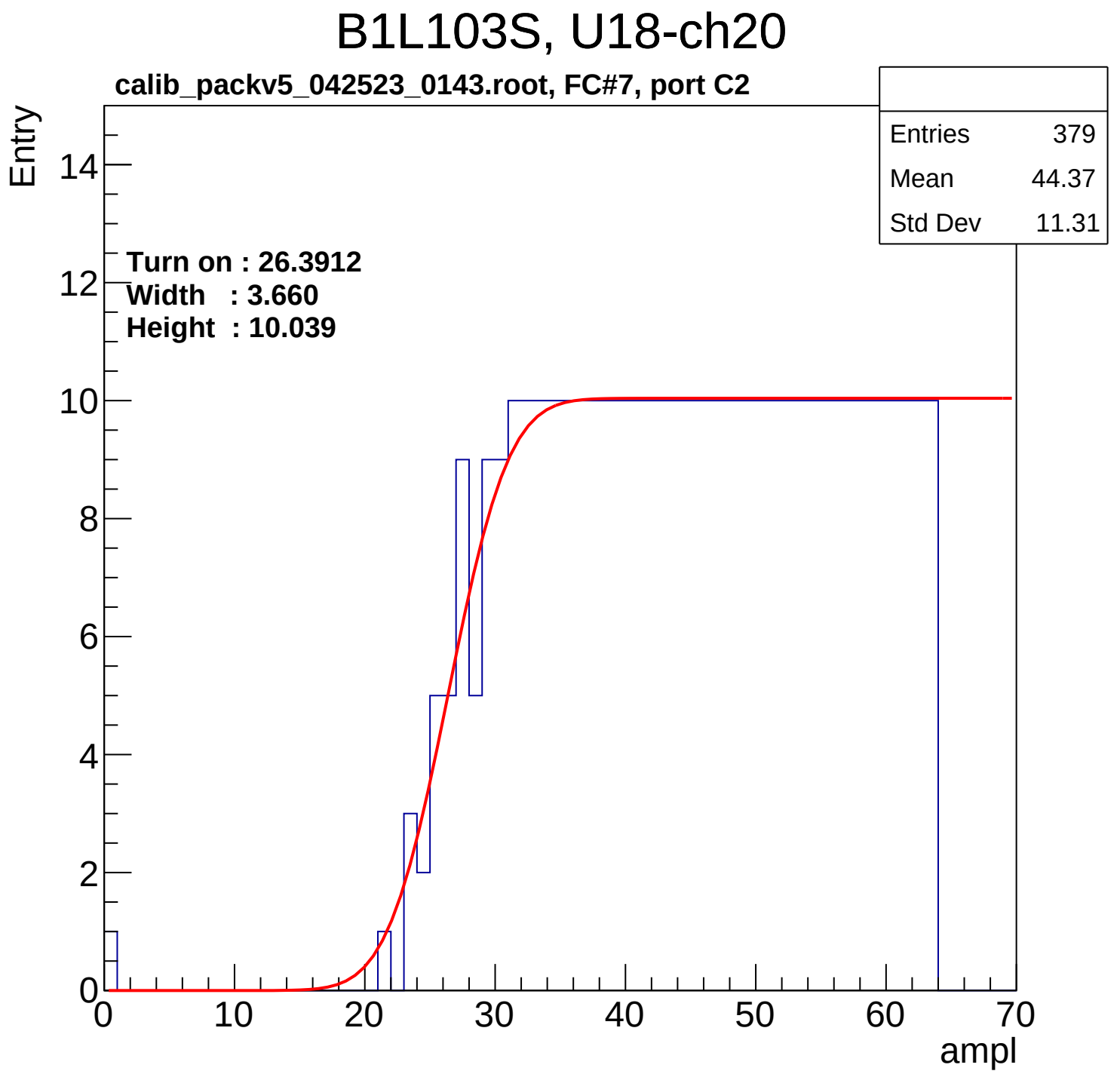
B1L103S, U18-ch20
calib_packv5_042523_0143.root, FC#7, port C2
Entries 379
Mean 44.37
Std Dev 11.31
Turn on : 26.3912
Width : 3.660
Height : 10.039
Entry
ampl
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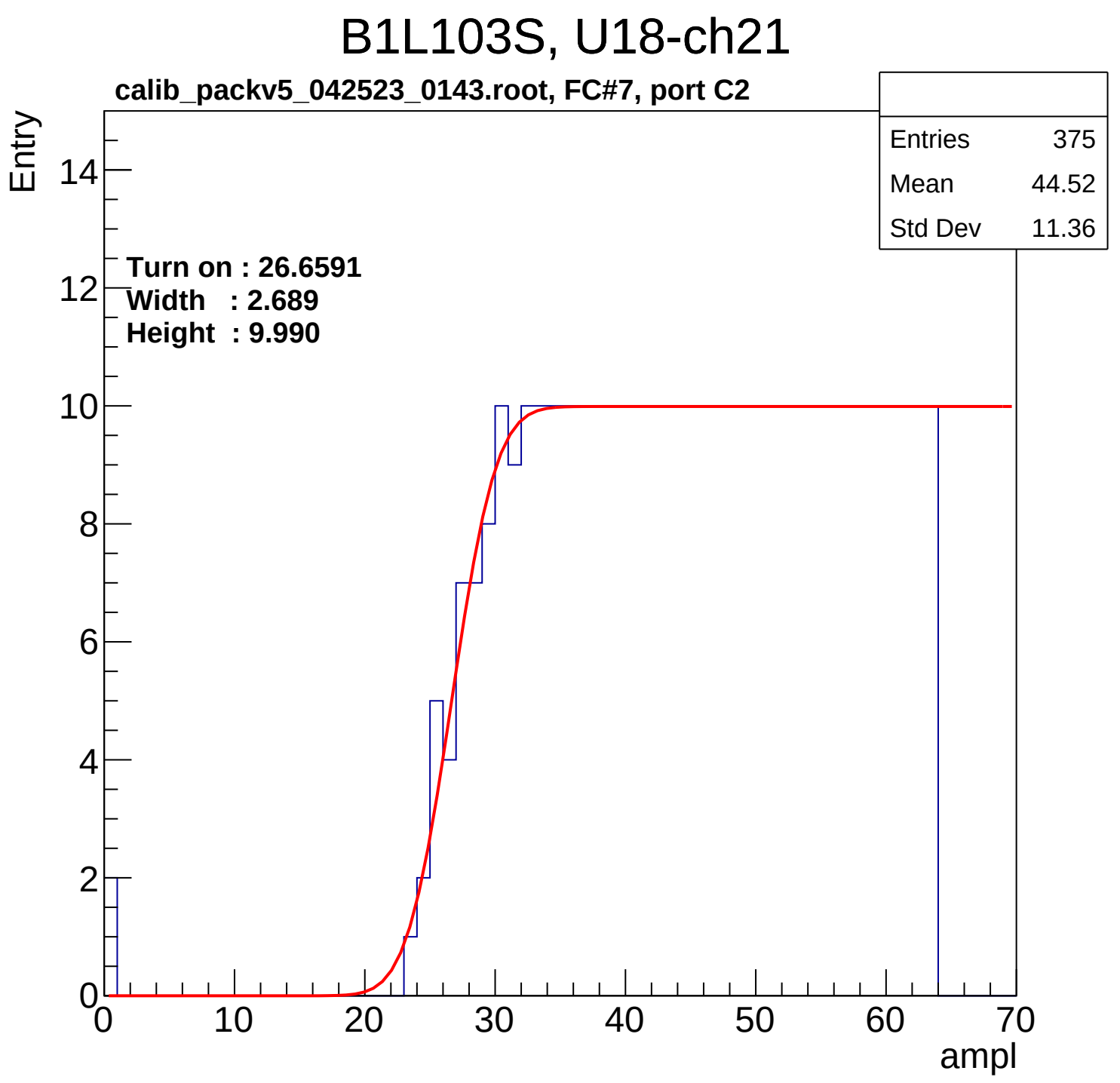
B1L103S, U18-ch21
calib_packv5_042523_0143.root, FC#7, port C2
Entries 375
Mean 44.52
Std Dev 11.36
Turn on : 26.6591
Width : 2.689
Height : 9.990
Entry
ampl
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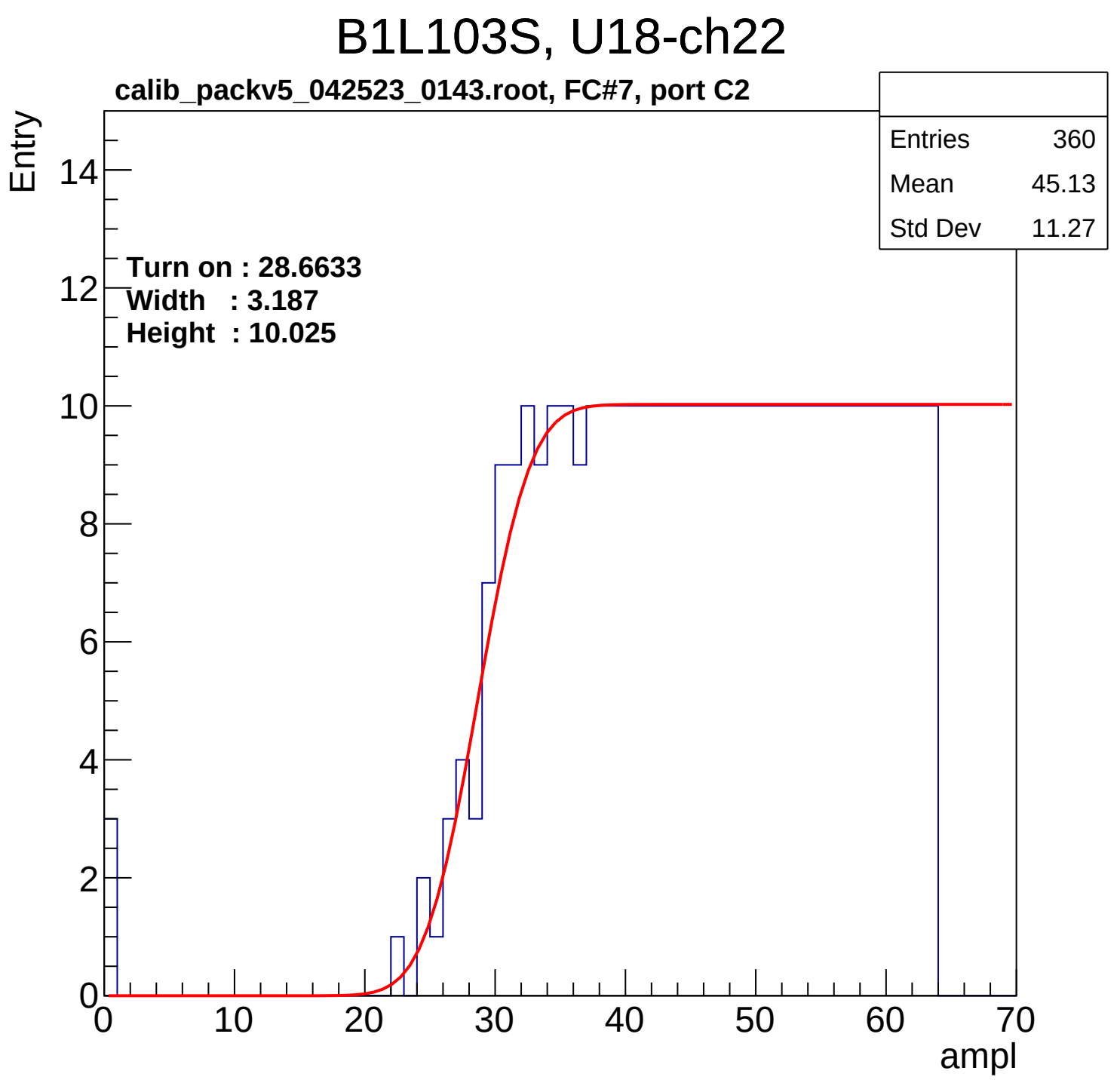
B1L103S, U18-ch22
calib_packv5_042523_0143.root, FC#7, port C2
Entries 360
Mean 45.13
Std Dev 11.27
Turn on : 28.6633
Width : 3.187
Height : 10.025
Entry
ampl
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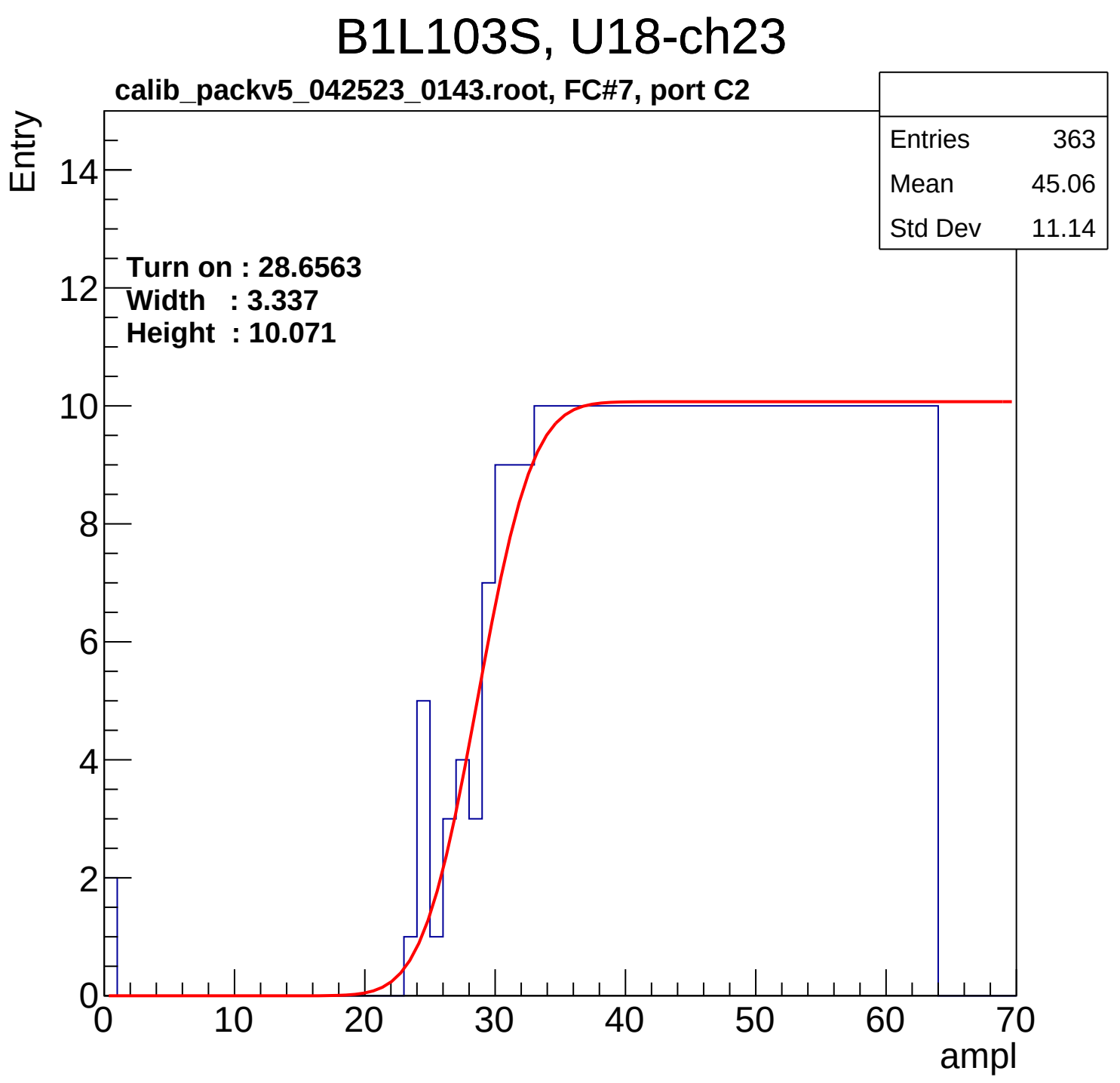
B1L103S, U18-ch23
calib_packv5_042523_0143.root, FC#7, port C2
Entries 363
Mean 45.06
Std Dev 11.14
Turn on : 28.6563
Width : 3.337
Height : 10.071
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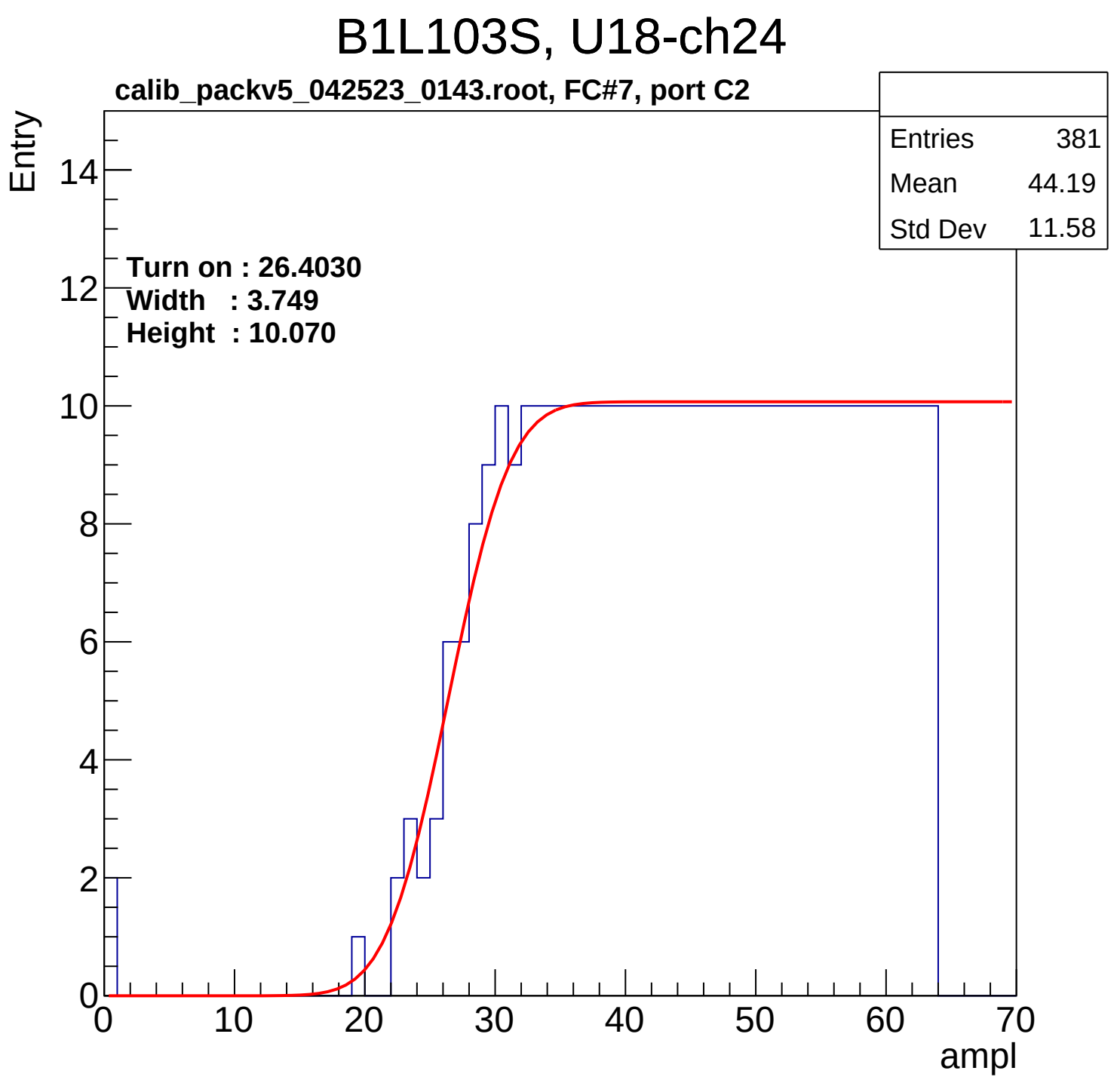
B1L103S, U18-ch24
calib_packv5_042523_0143.root, FC#7, port C2
Entries 381
Mean 44.19
Std Dev 11.58
Turn on : 26.4030
Width : 3.749
Height : 10.070
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ampl
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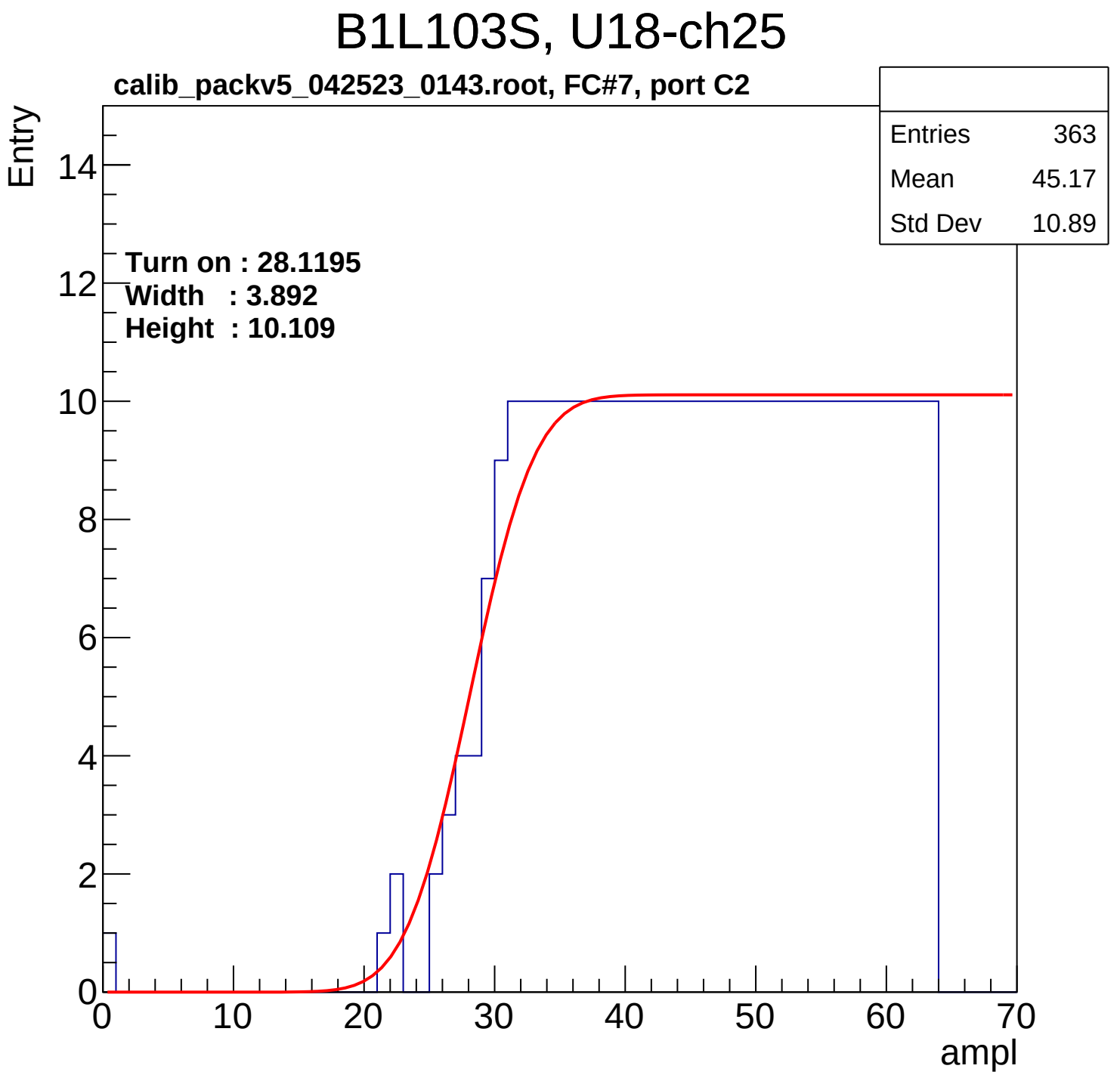
B1L103S, U18-ch25
calib_packv5_042523_0143.root, FC#7, port C2
Entries 363
Mean 45.17
Std Dev 10.89
Turn on : 28.1195
Width : 3.892
Height : 10.109
Entry
ampl
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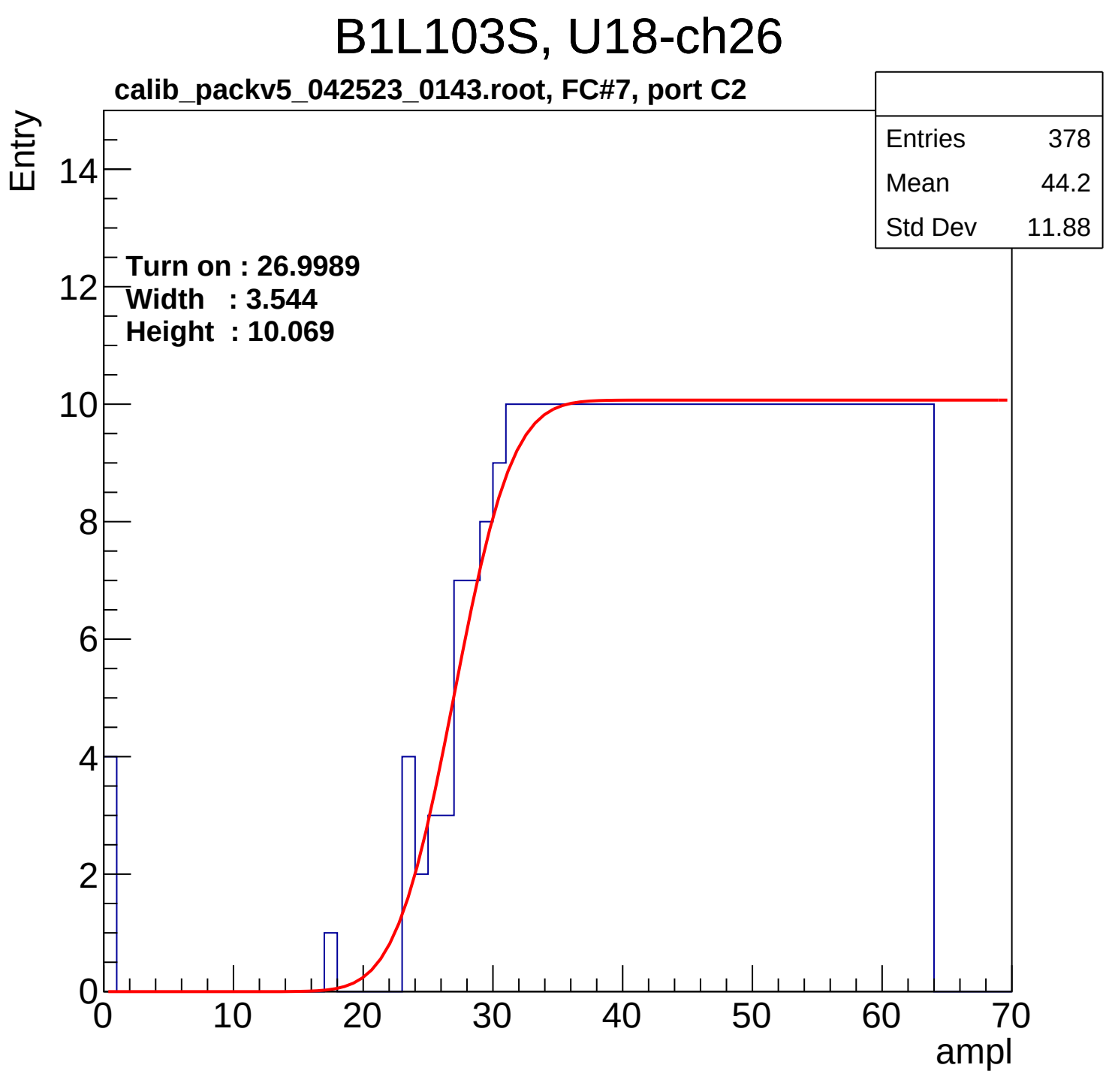
B1L103S, U18-ch26
calib_packv5_042523_0143.root, FC#7, port C2
Entries 378
Mean 44.2
Std Dev 11.88
Turn on : 26.9989
Width : 3.544
Height : 10.069
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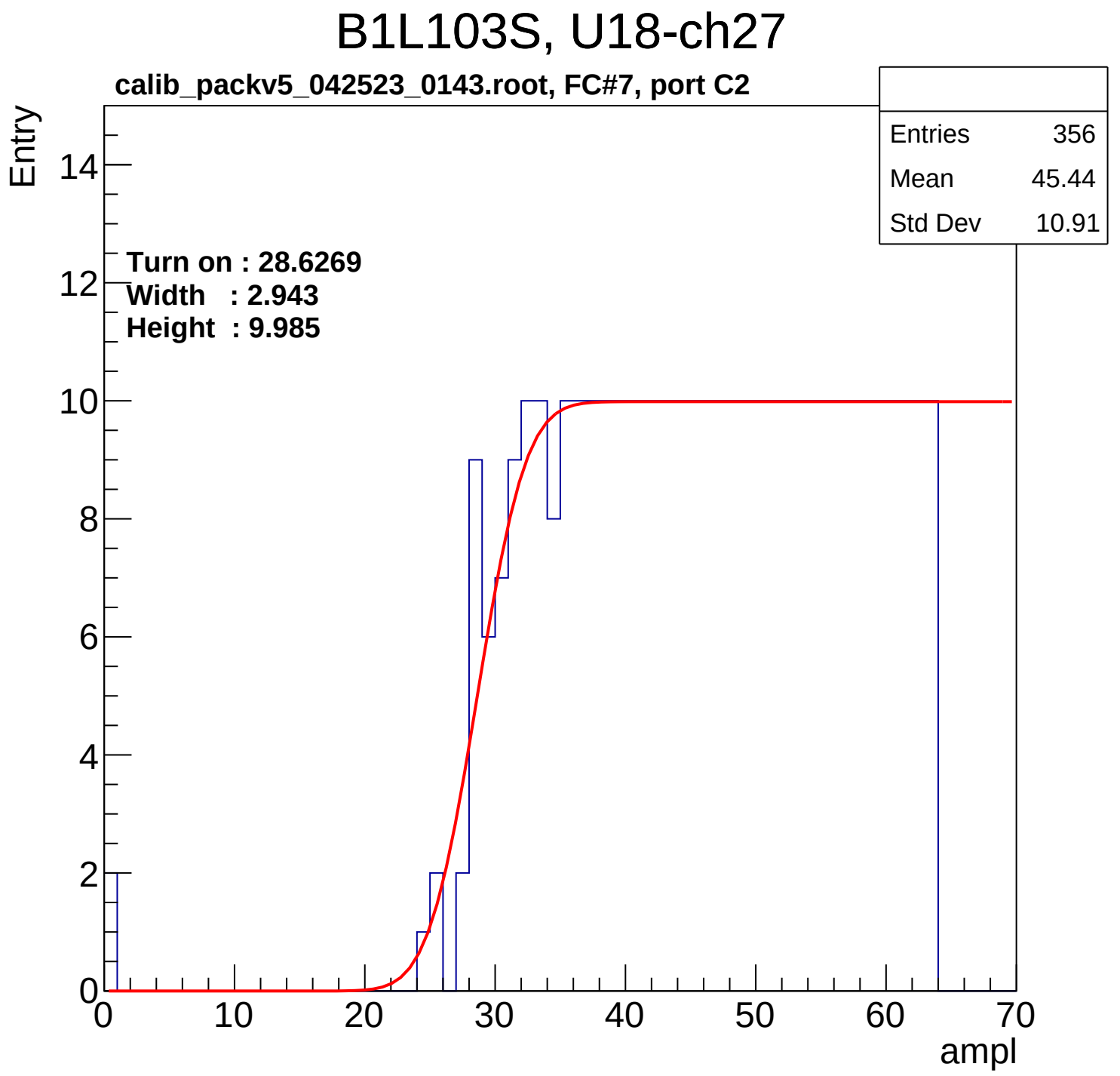
B1L103S, U18-ch27
calib_packv5_042523_0143.root, FC#7, port C2
Entries 356
Mean 45.44
Std Dev 10.91
Turn on : 28.6269
Width : 2.943
Height : 9.985
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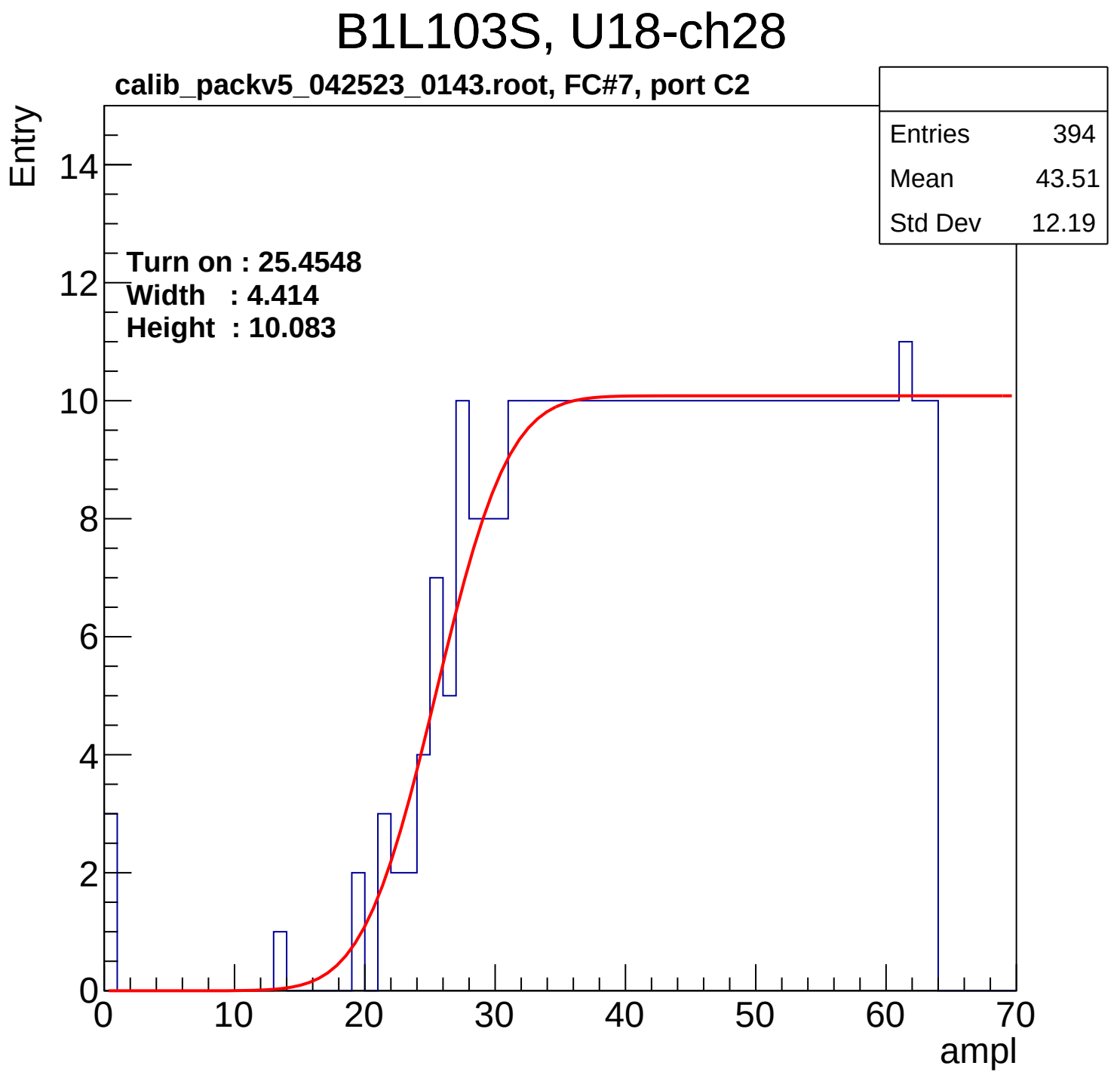
B1L103S, U18-ch28
calib_packv5_042523_0143.root, FC#7, port C2
Entries 394
Mean 43.51
Std Dev 12.19
Turn on : 25.4548
Width : 4.414
Height : 10.083
Entry
ampl
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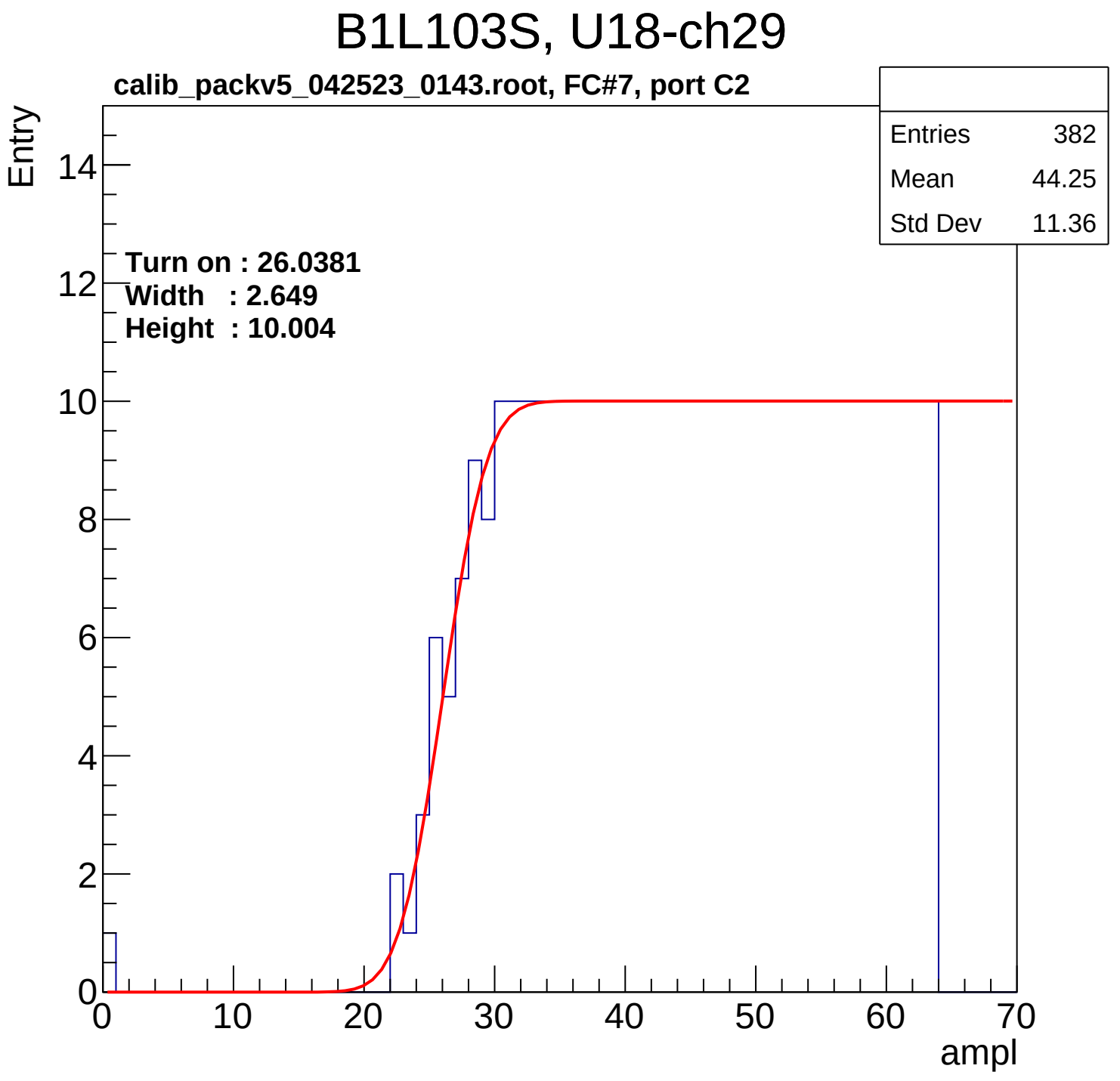
B1L103S, U18-ch29
calib_packv5_042523_0143.root, FC#7, port C2
Entries 382
Mean 44.25
Std Dev 11.36
Turn on : 26.0381
Width : 2.649
Height : 10.004
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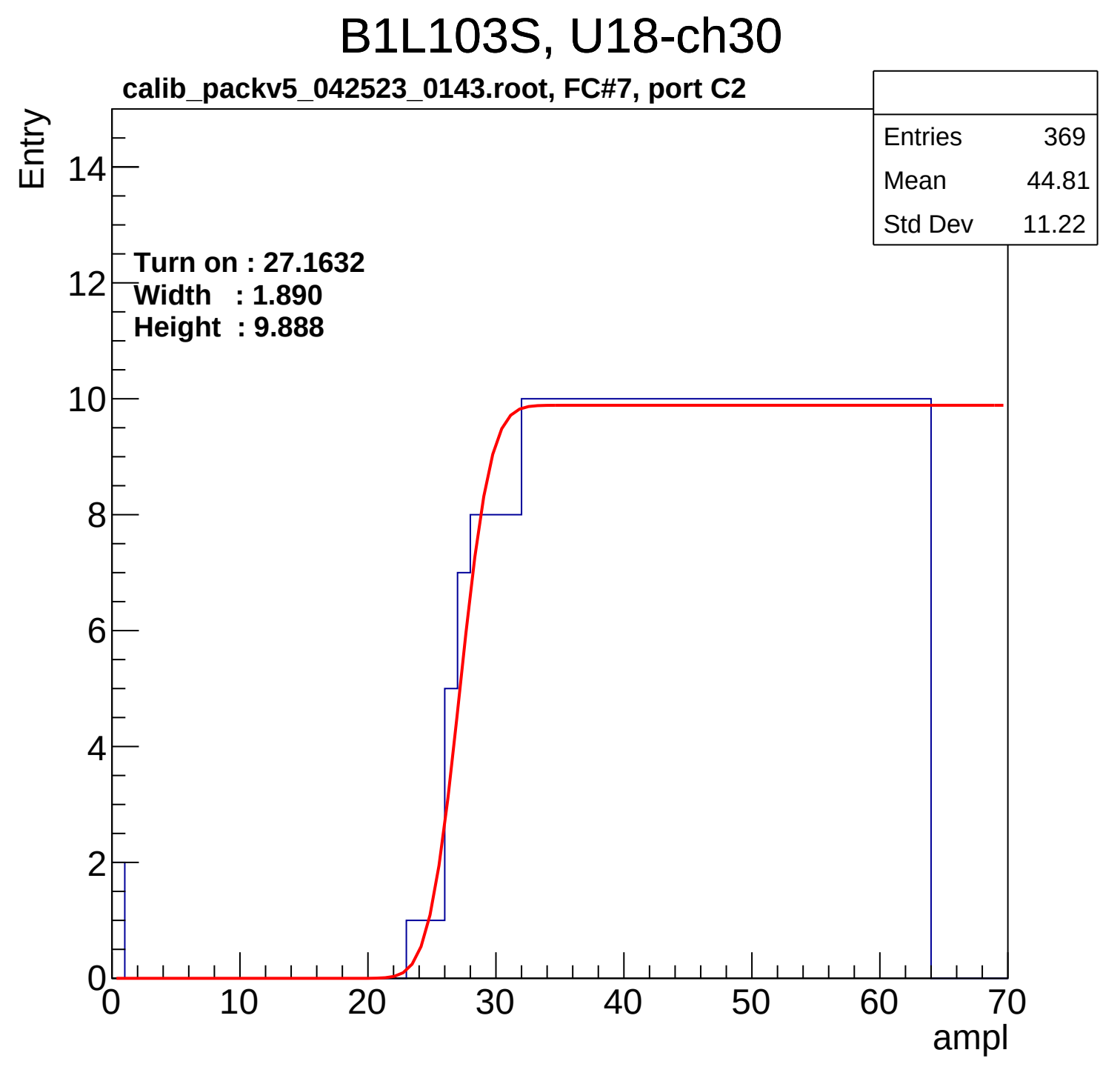
B1L103S, U18-ch30
calib_packv5_042523_0143.root, FC#7, port C2
Entries 369
Mean 44.81
Std Dev 11.22
Turn on : 27.1632
Width : 1.890
Height : 9.888
Entry
ampl
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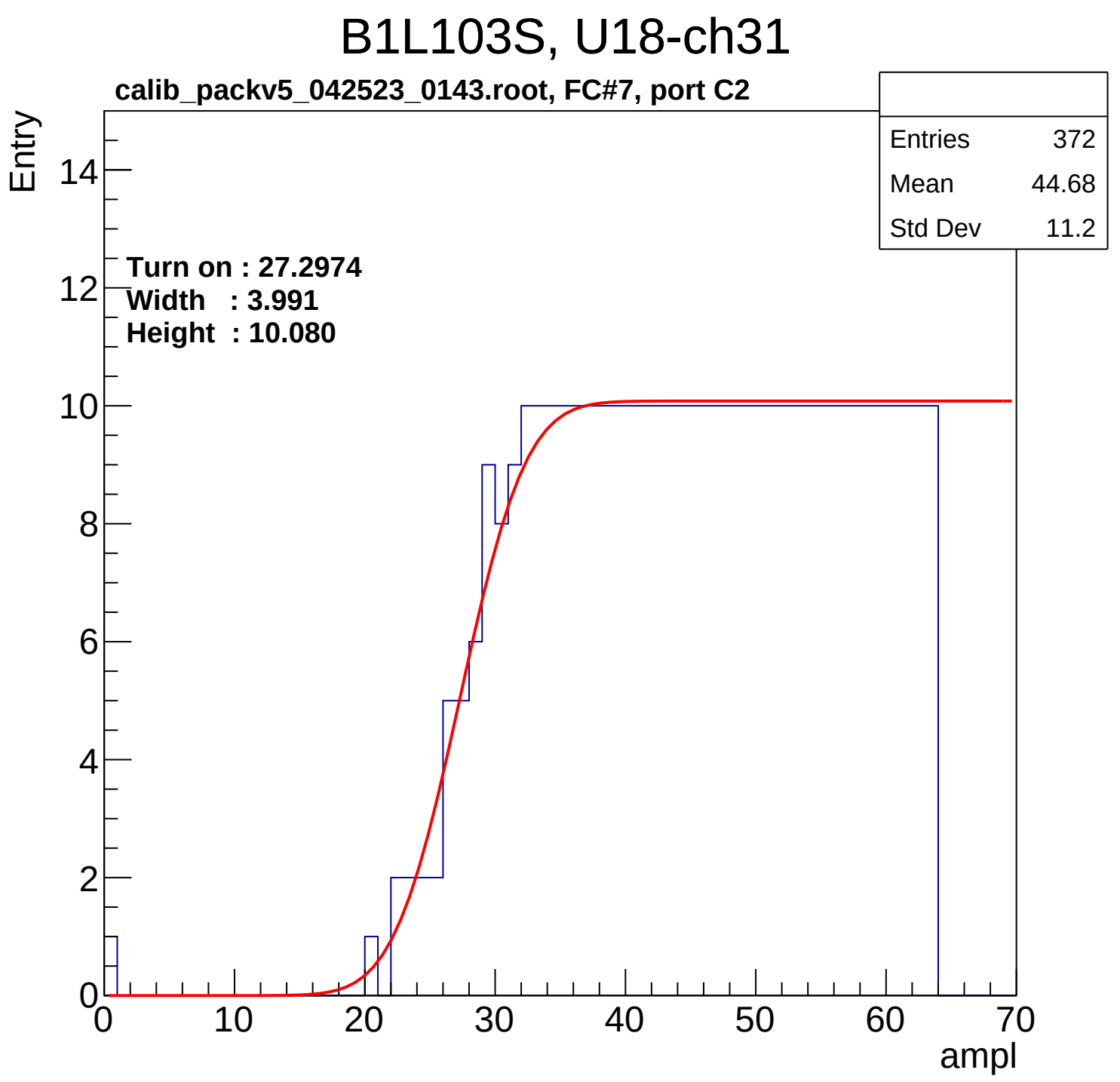
B1L103S, U18-ch31
calib_packv5_042523_0143.root, FC#7, port C2
Entries 372
Mean 44.68
Std Dev 11.2
Turn on : 27.2974
Width : 3.991
Height : 10.080
Entry
ampl
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2
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8
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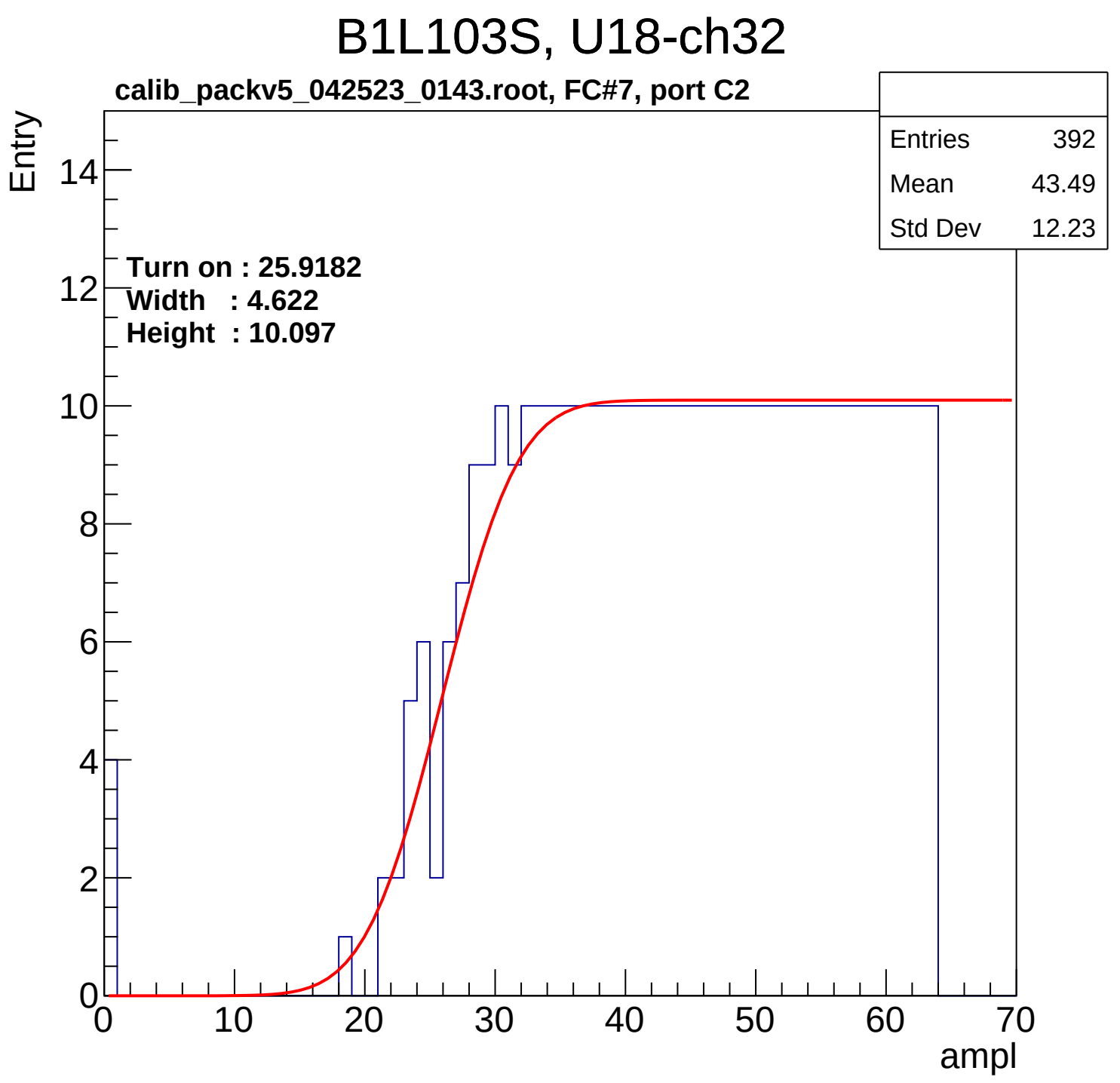
B1L103S, U18-ch32
calib_packv5_042523_0143.root, FC#7, port C2
Entries 392
Mean 43.49
Std Dev 12.23
Turn on : 25.9182
Width : 4.622
Height : 10.097
Entry
ampl
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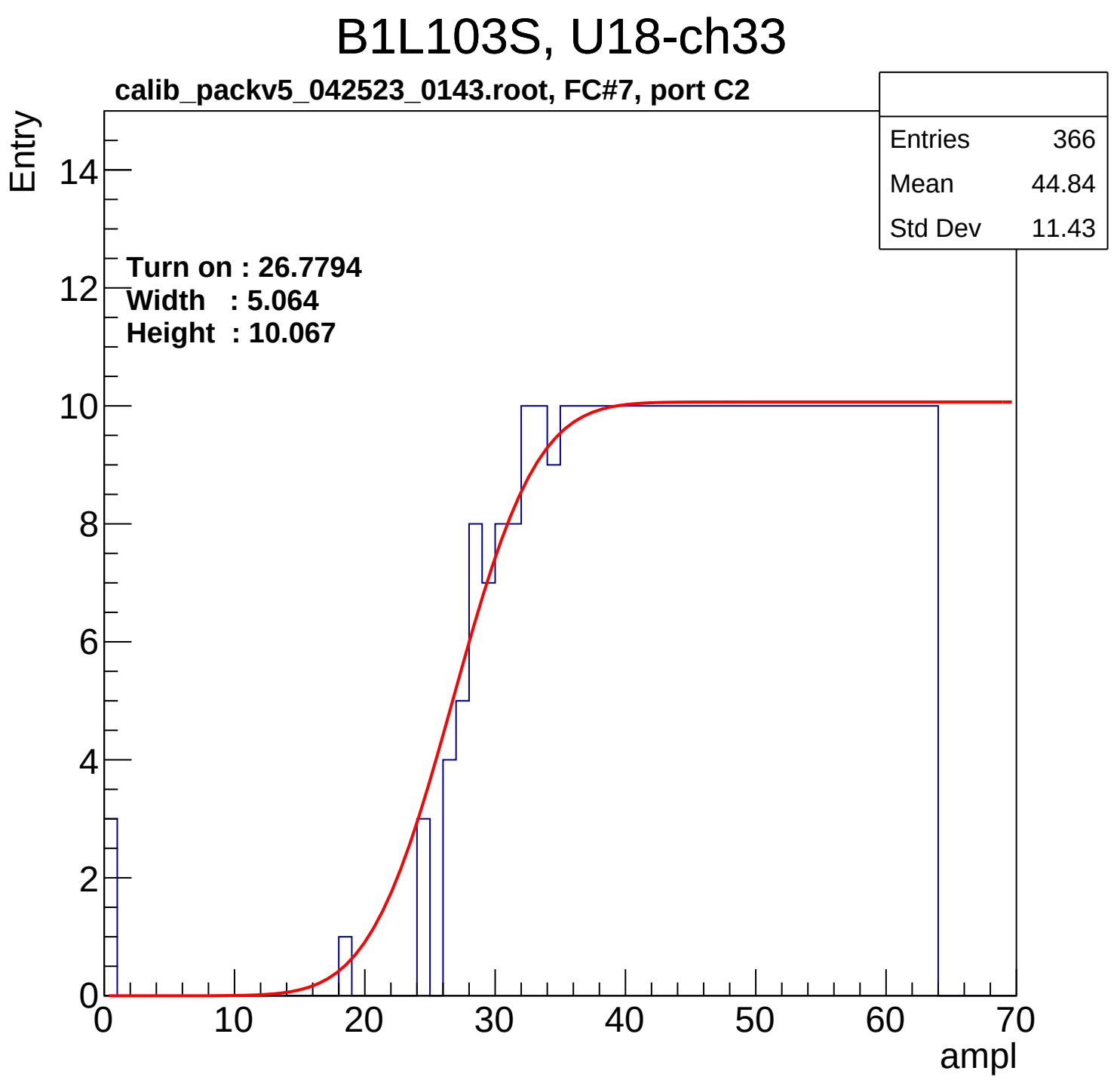
B1L103S, U18-ch33
calib_packv5_042523_0143.root, FC#7, port C2
Entries 366
Mean 44.84
Std Dev 11.43
Turn on : 26.7794
Width : 5.064
Height : 10.067
Entry
ampl
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2
4
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8
10
12
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0
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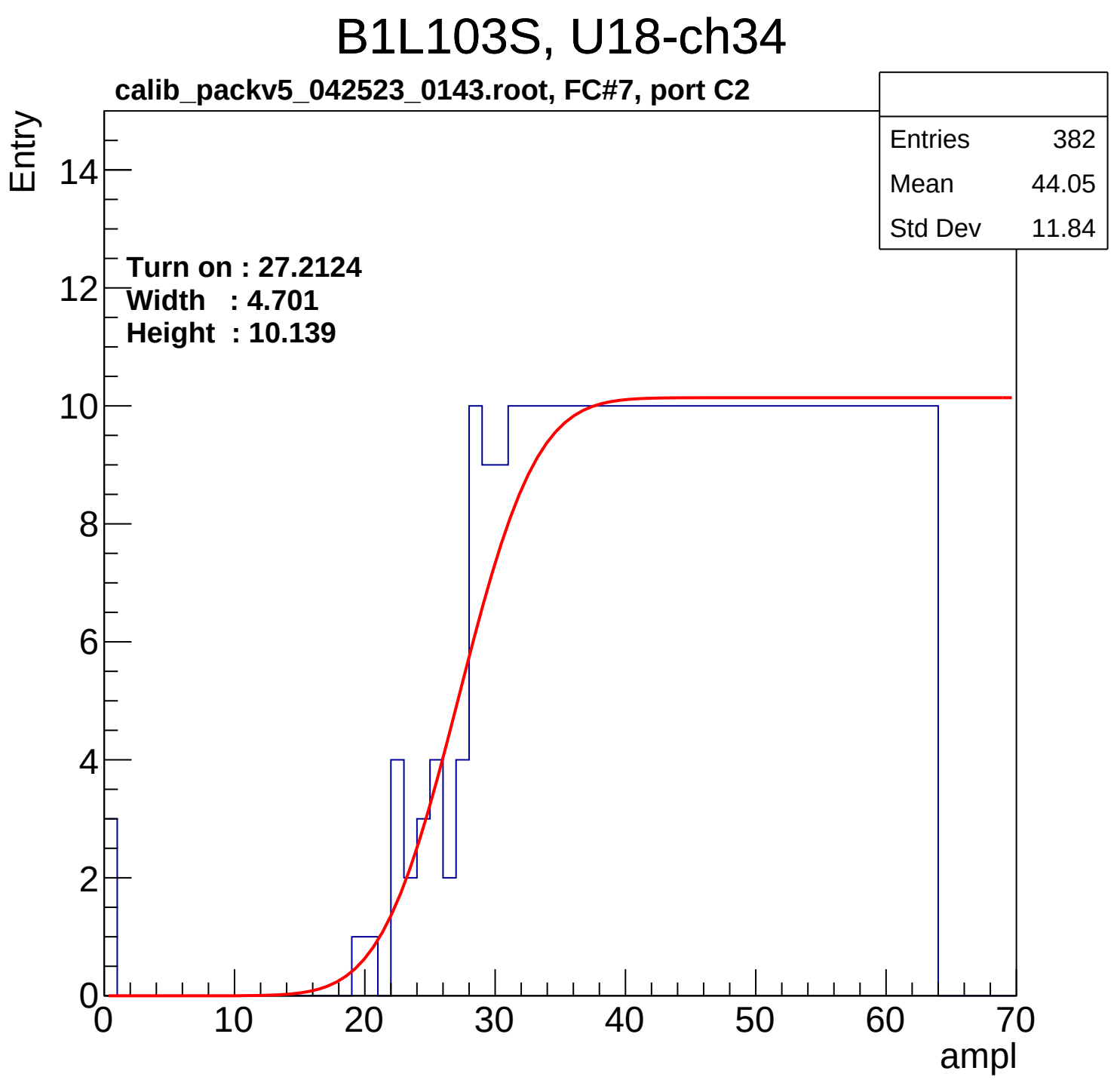
B1L103S, U18-ch34
calib_packv5_042523_0143.root, FC#7, port C2
Entries 382
Mean 44.05
Std Dev 11.84
Turn on : 27.2124
Width : 4.701
Height : 10.139
Entry
ampl
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2
4
6
8
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0
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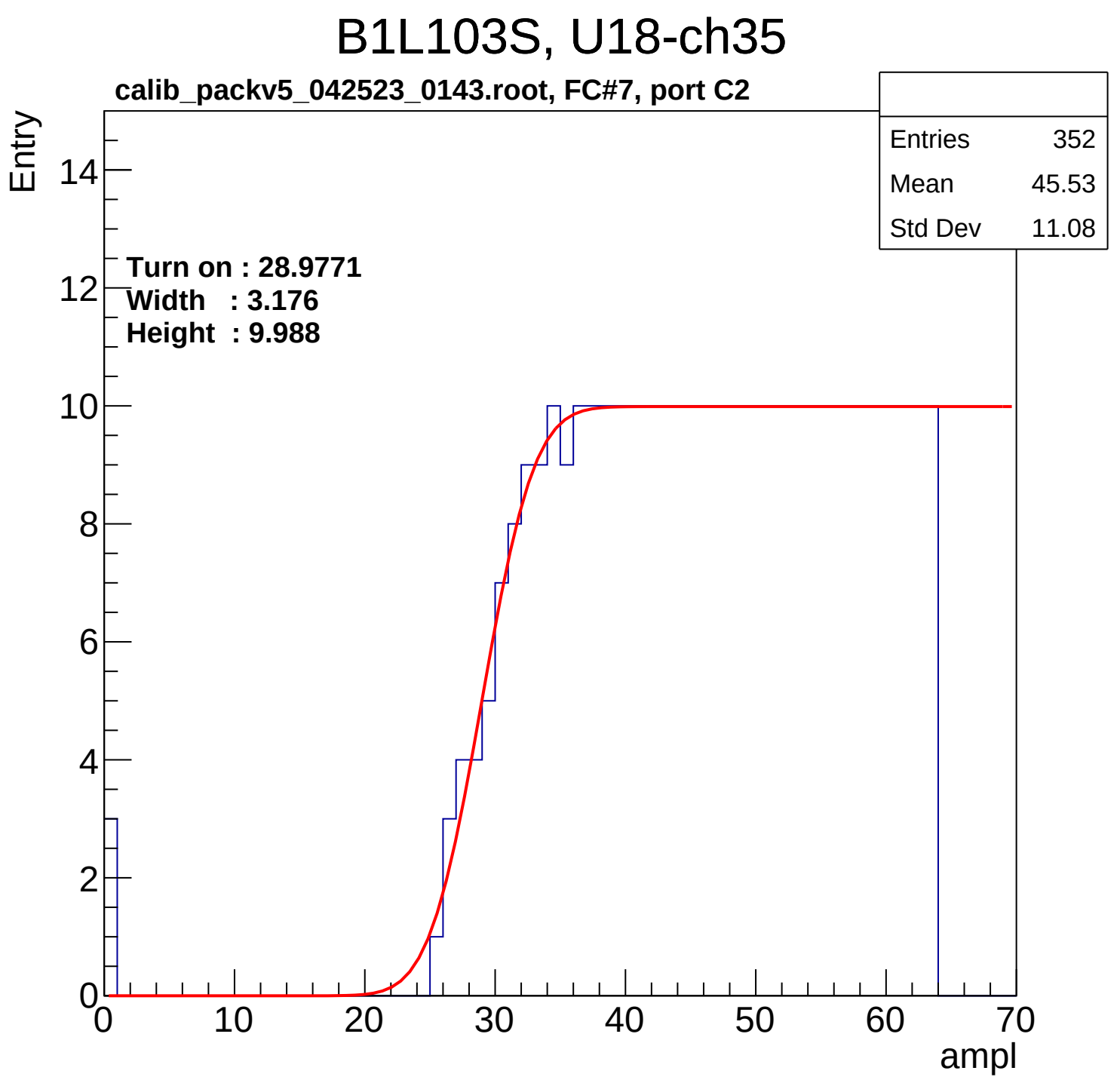
B1L103S, U18-ch35
calib_packv5_042523_0143.root, FC#7, port C2
Entries 352
Mean 45.53
Std Dev 11.08
Turn on : 28.9771
Width : 3.176
Height : 9.988
Entry
ampl
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4
6
8
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12
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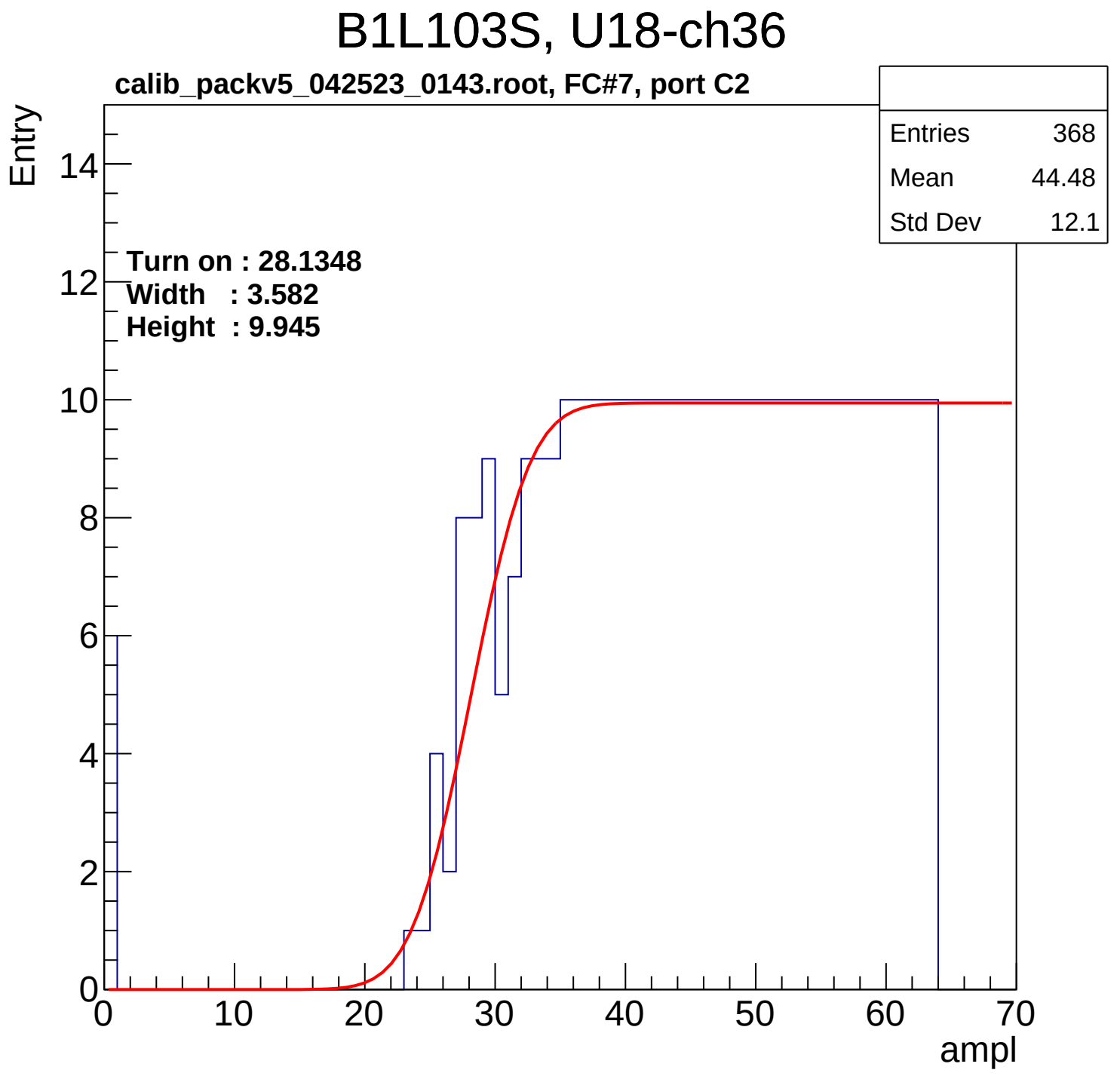
B1L103S, U18-ch36
calib_packv5_042523_0143.root, FC#7, port C2
Entries 368
Mean 44.48
Std Dev 12.1
Turn on : 28.1348
Width : 3.582
Height : 9.945
Entry
ampl
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2
4
6
8
10
12
14
0
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20
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40
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60
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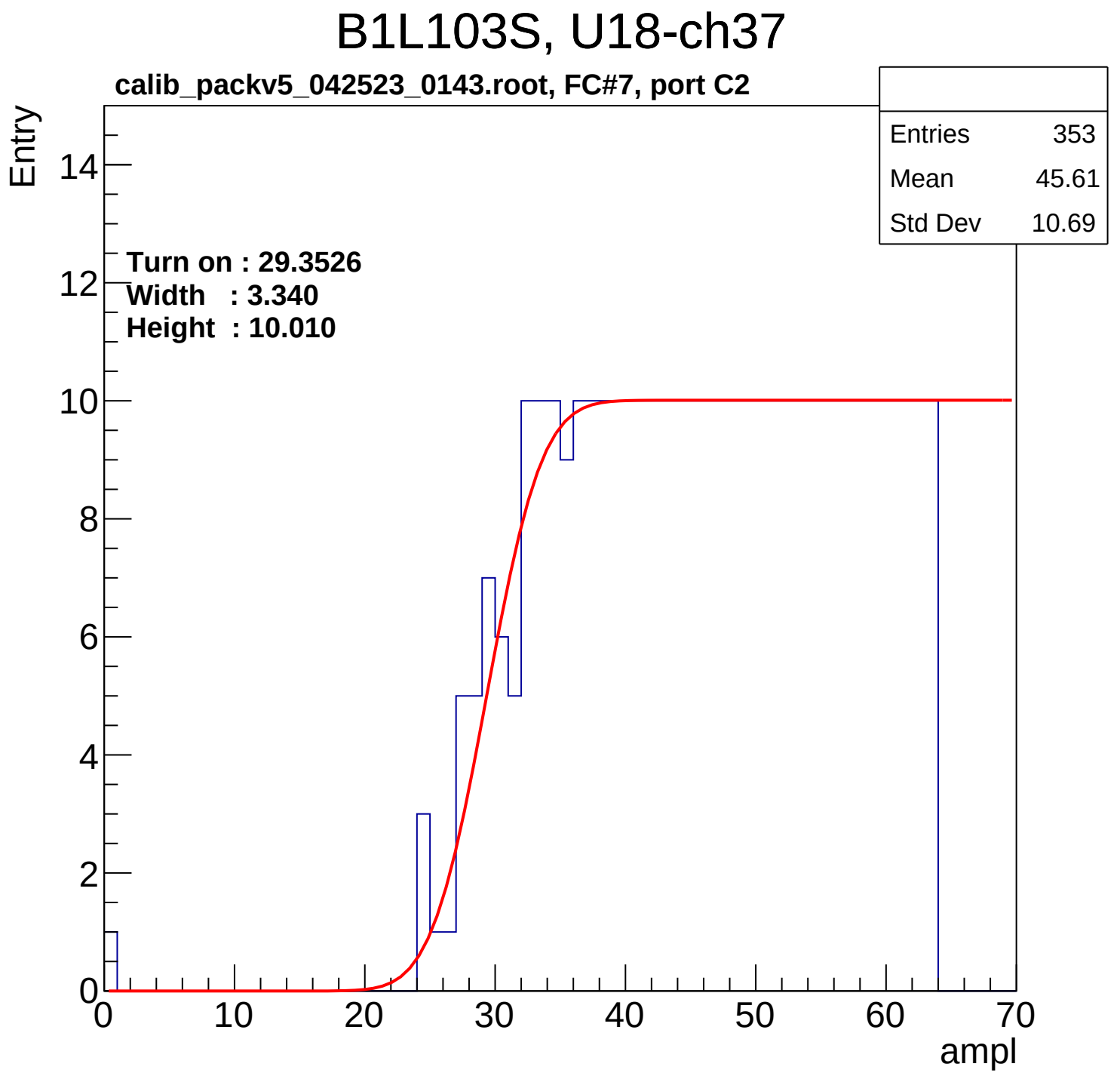
B1L103S, U18-ch37
calib_packv5_042523_0143.root, FC#7, port C2
Entries 353
Mean 45.61
Std Dev 10.69
Turn on : 29.3526
Width : 3.340
Height : 10.010
Entry
ampl
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2
4
6
8
10
12
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0
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60
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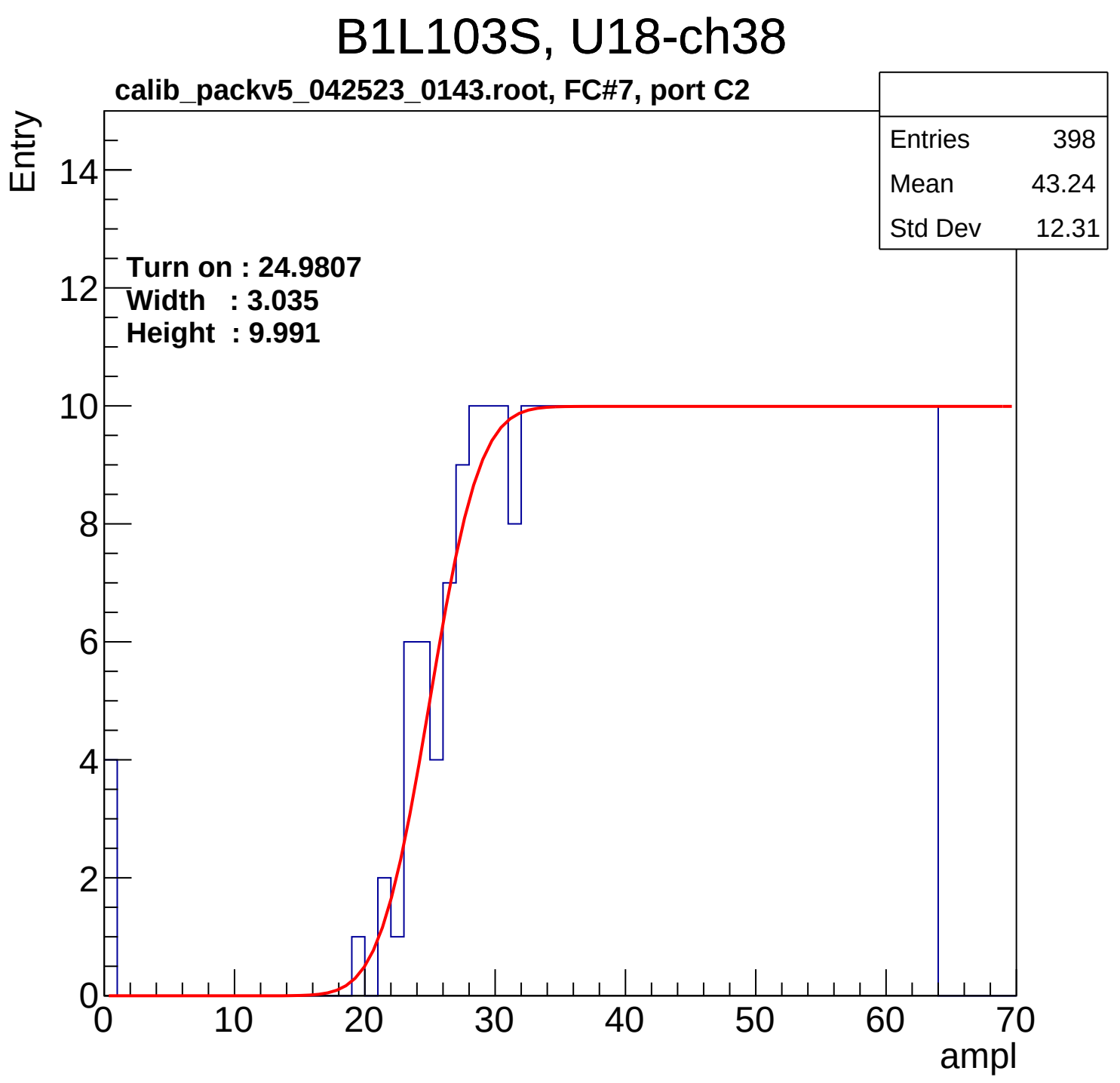
B1L103S, U18-ch38
calib_packv5_042523_0143.root, FC#7, port C2
Entries 398
Mean 43.24
Std Dev 12.31
Turn on : 24.9807
Width : 3.035
Height : 9.991
Entry
ampl
0
2
4
6
8
10
12
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60
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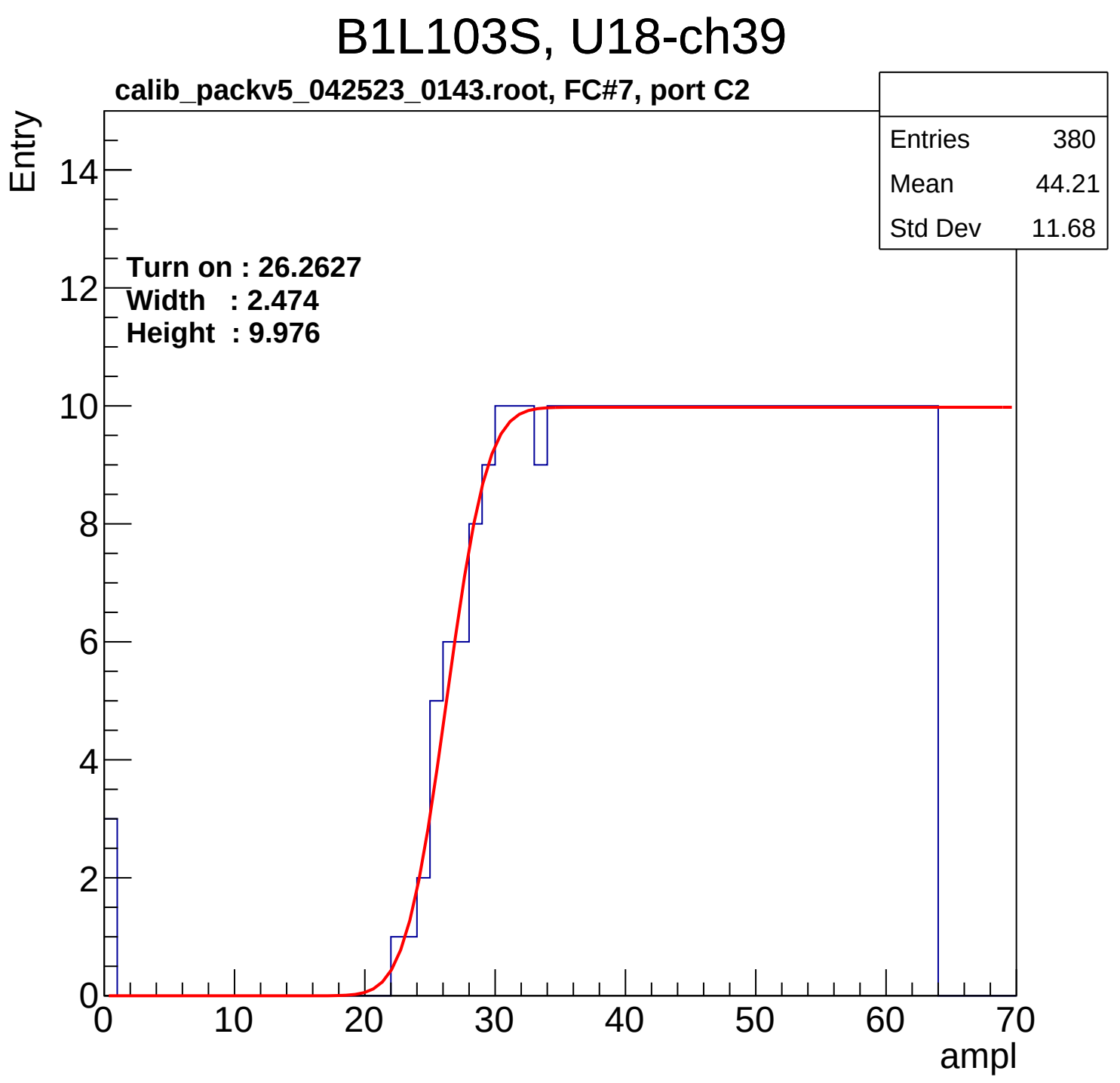
B1L103S, U18-ch39
calib_packv5_042523_0143.root, FC#7, port C2
Entries 380
Mean 44.21
Std Dev 11.68
Turn on : 26.2627
Width : 2.474
Height : 9.976
Entry
ampl
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6
8
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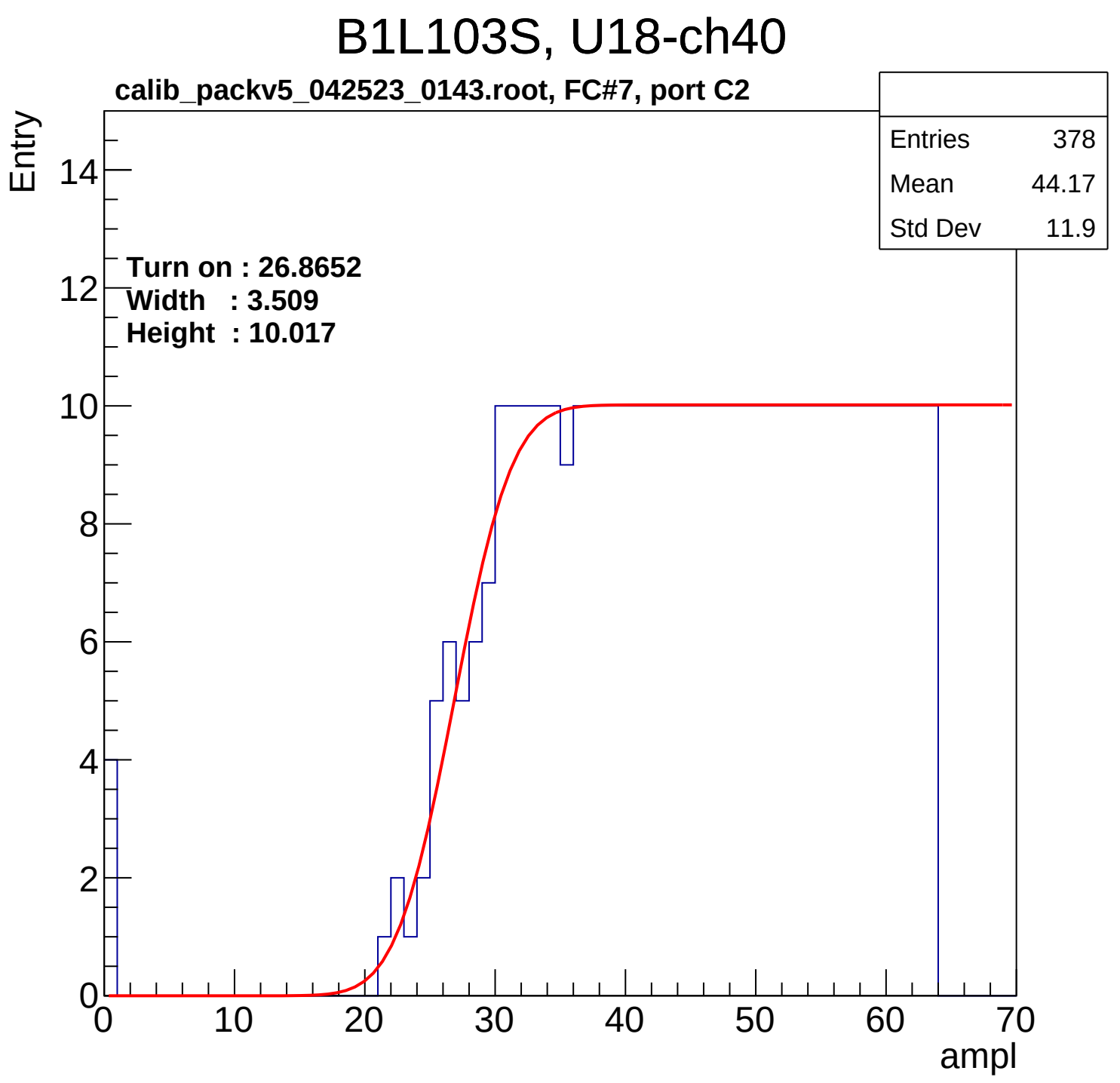
B1L103S, U18-ch40
calib_packv5_042523_0143.root, FC#7, port C2
Entries 378
Mean 44.17
Std Dev 11.9
Turn on : 26.8652
Width : 3.509
Height : 10.017
Entry
ampl
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4
6
8
10
12
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0
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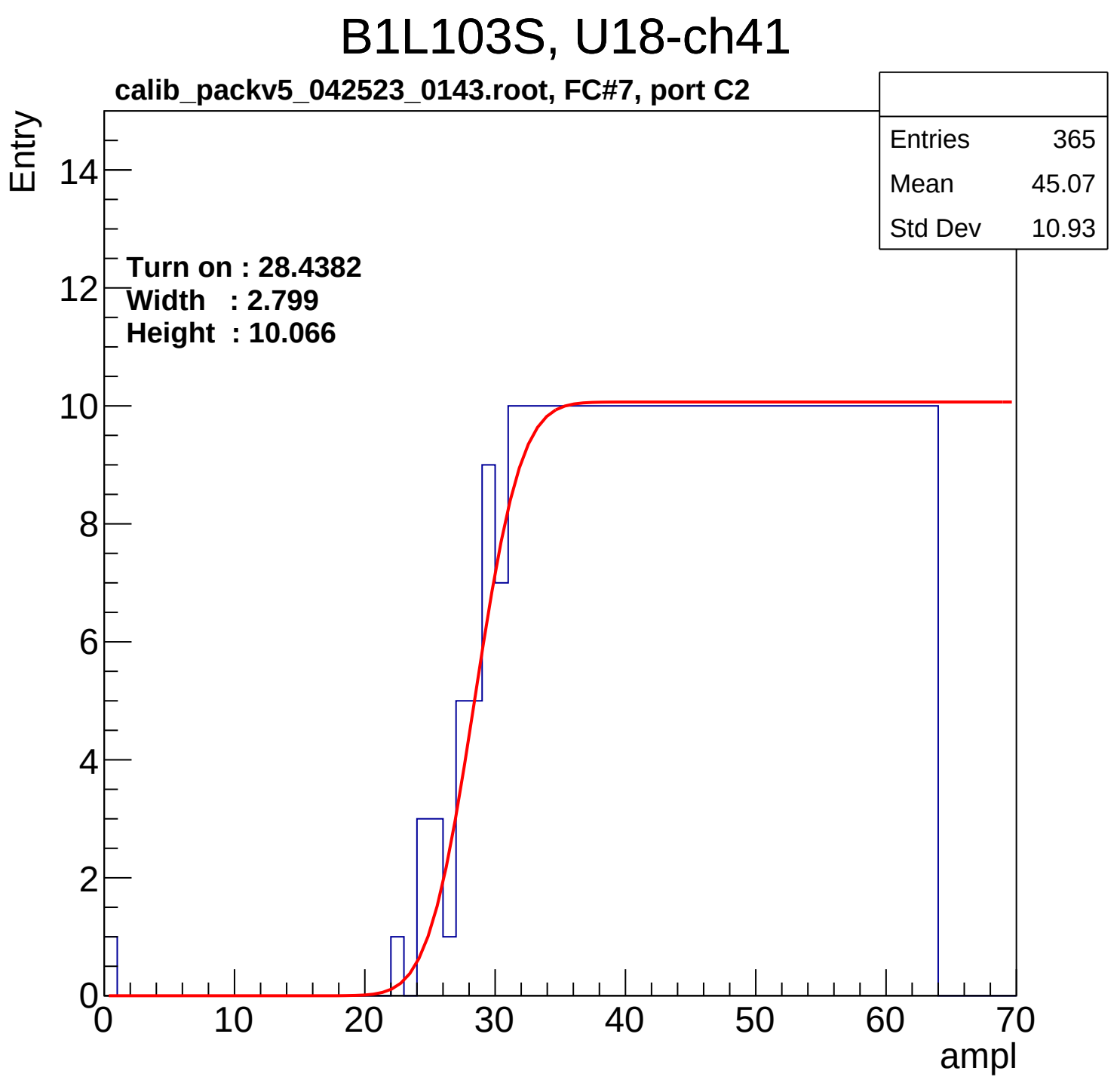
B1L103S, U18-ch41
calib_packv5_042523_0143.root, FC#7, port C2
Entries 365
Mean 45.07
Std Dev 10.93
Turn on : 28.4382
Width : 2.799
Height : 10.066
Entry
ampl
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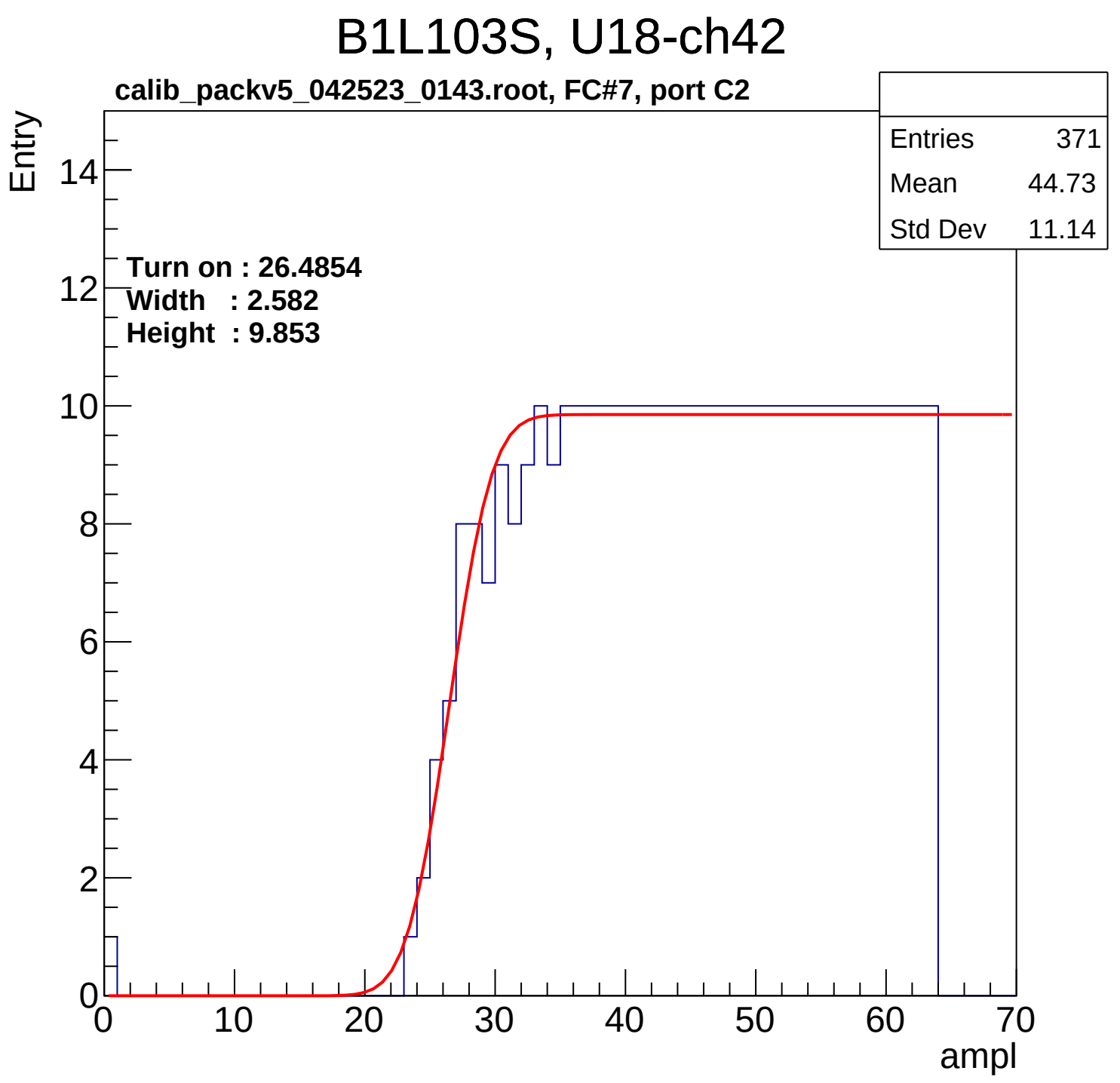
B1L103S, U18-ch42
calib_packv5_042523_0143.root, FC#7, port C2
Entries 371
Mean 44.73
Std Dev 11.14
Turn on : 26.4854
Width : 2.582
Height : 9.853
Entry
ampl
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2
4
6
8
10
12
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0
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20
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60
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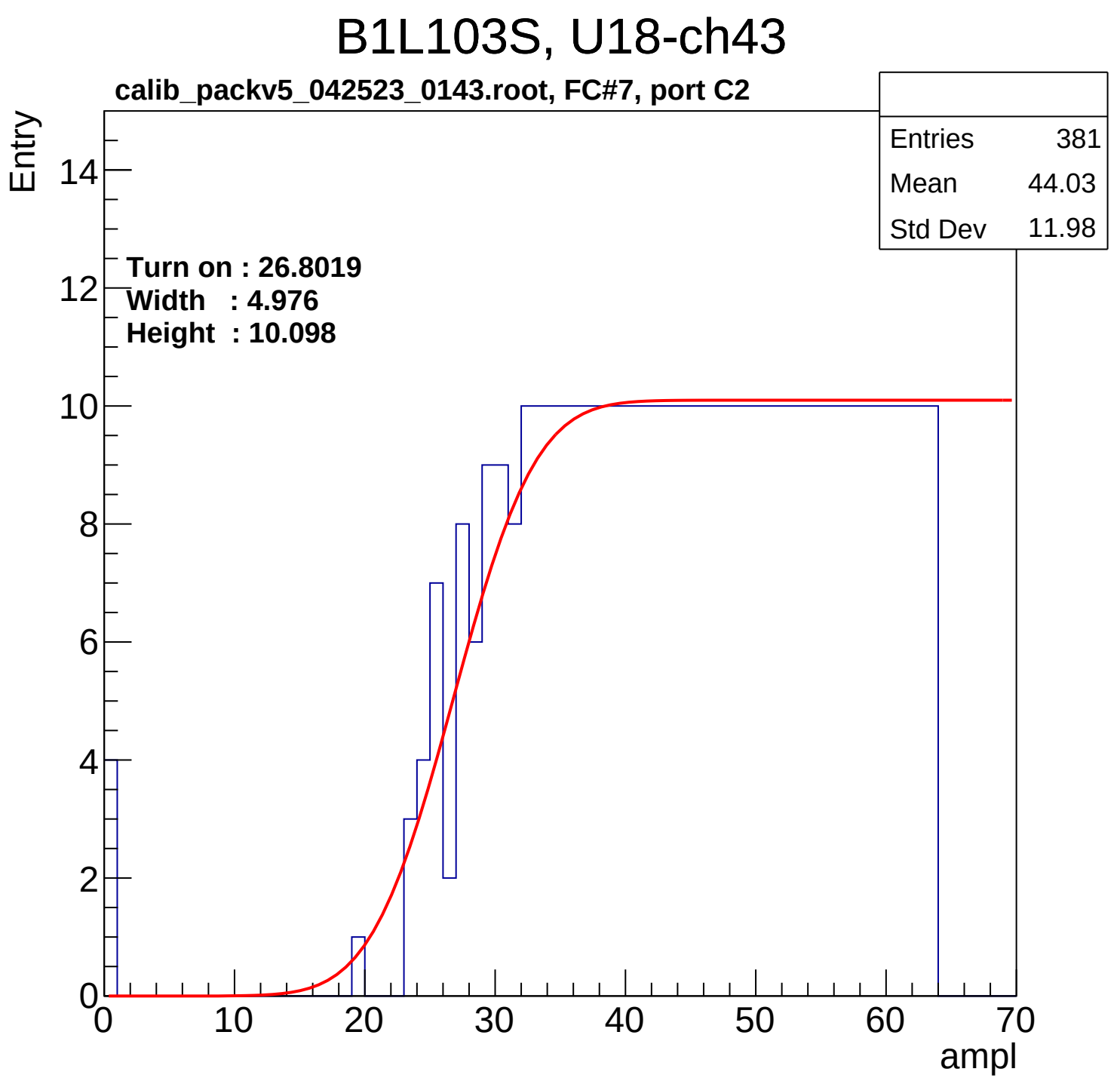
B1L103S, U18-ch43
calib_packv5_042523_0143.root, FC#7, port C2
Entries 381
Mean 44.03
Std Dev 11.98
Turn on : 26.8019
Width : 4.976
Height : 10.098
Entry
ampl
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6
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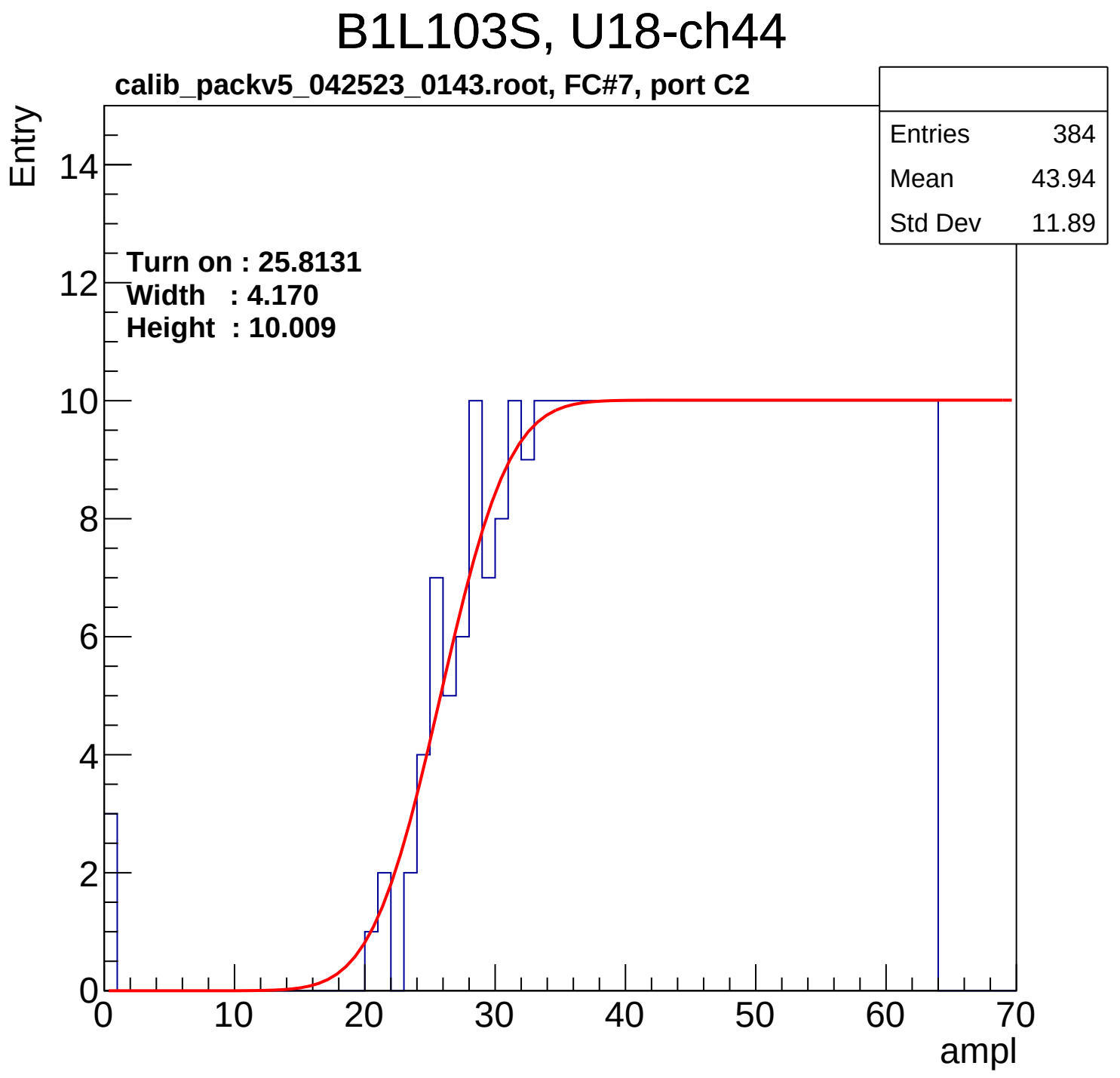
B1L103S, U18-ch44
calib_packv5_042523_0143.root, FC#7, port C2
Entries 384
Mean 43.94
Std Dev 11.89
Turn on : 25.8131
Width : 4.170
Height : 10.009
Entry
ampl
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8
10
12
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20
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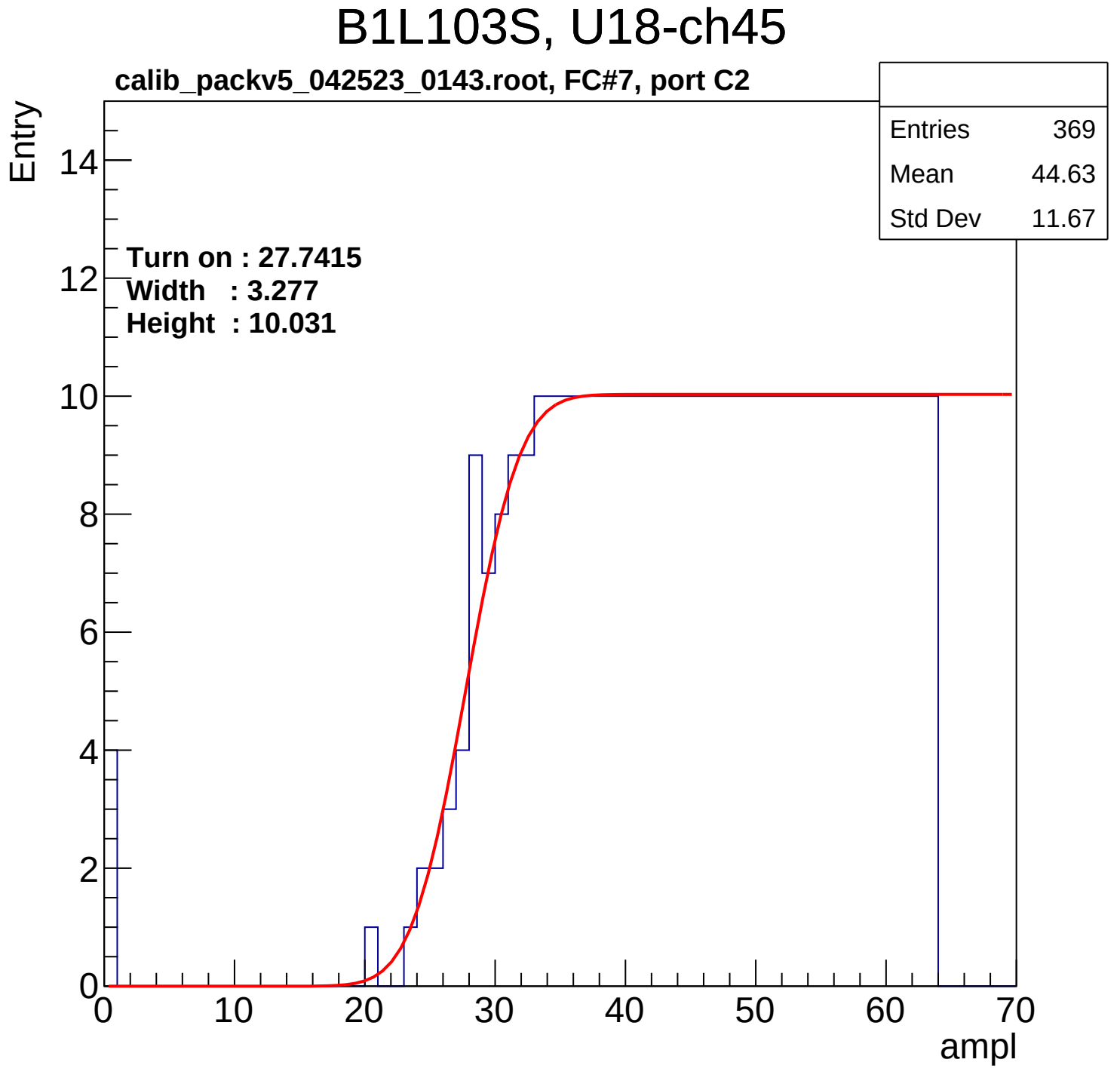
B1L103S, U18-ch45
calib_packv5_042523_0143.root, FC#7, port C2
Entries 369
Mean 44.63
Std Dev 11.67
Turn on : 27.7415
Width : 3.277
Height : 10.031
Entry
ampl
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8
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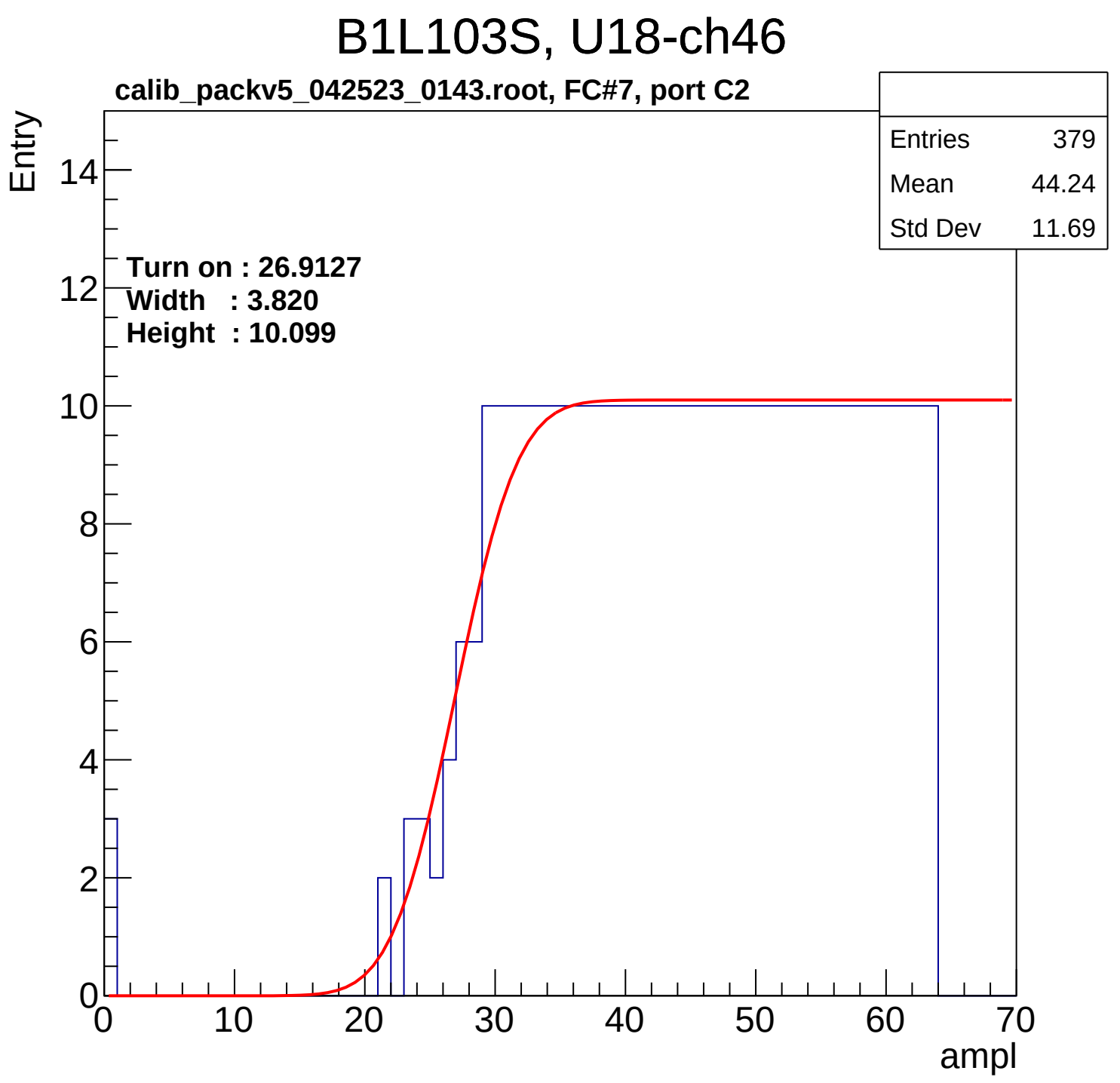
B1L103S, U18-ch46
calib_packv5_042523_0143.root, FC#7, port C2
Entries 379
Mean 44.24
Std Dev 11.69
Turn on : 26.9127
Width : 3.820
Height : 10.099
Entry
ampl
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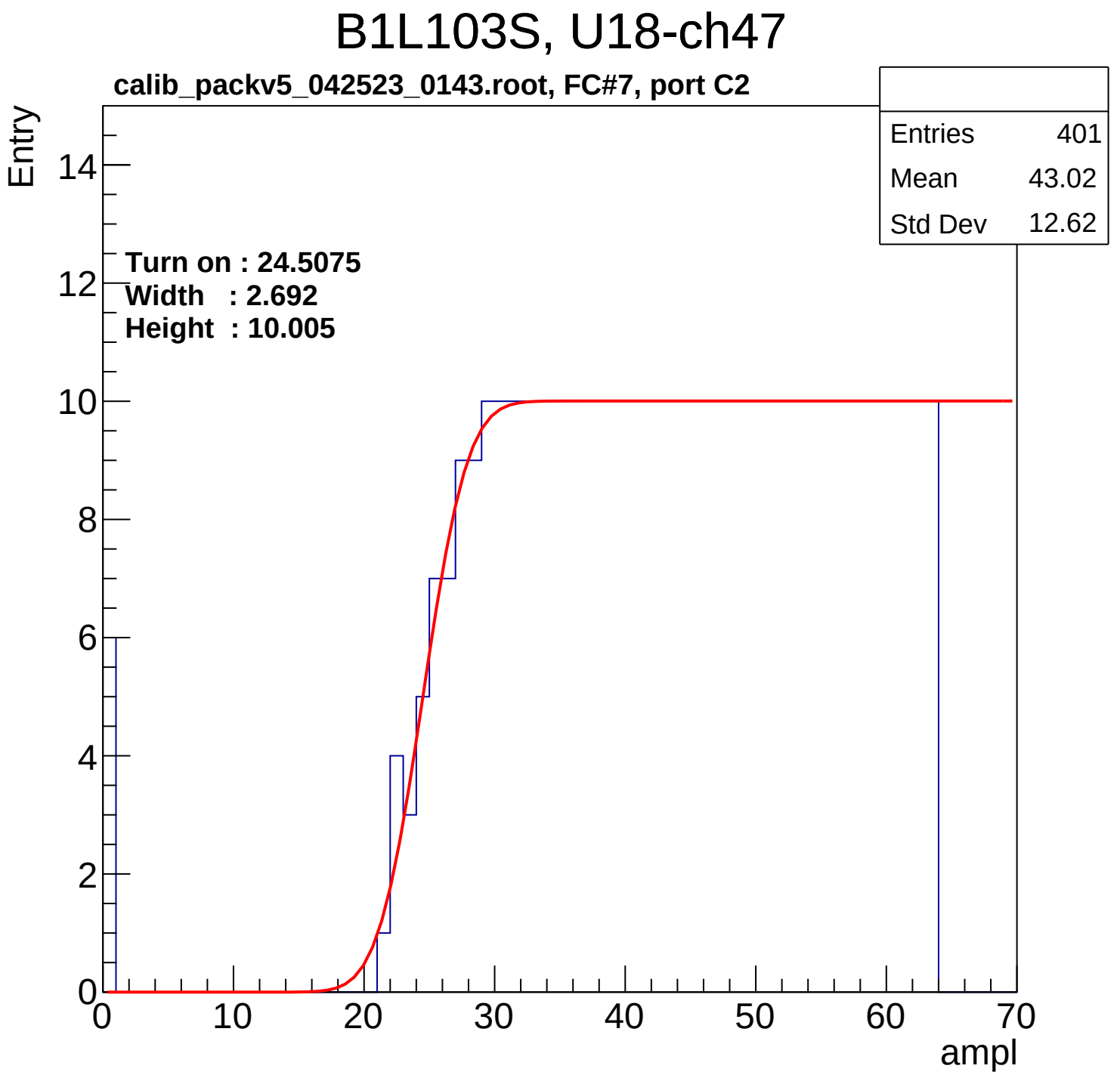
B1L103S, U18-ch47
calib_packv5_042523_0143.root, FC#7, port C2
Entries 401
Mean 43.02
Std Dev 12.62
Turn on : 24.5075
Width : 2.692
Height : 10.005
Entry
ampl
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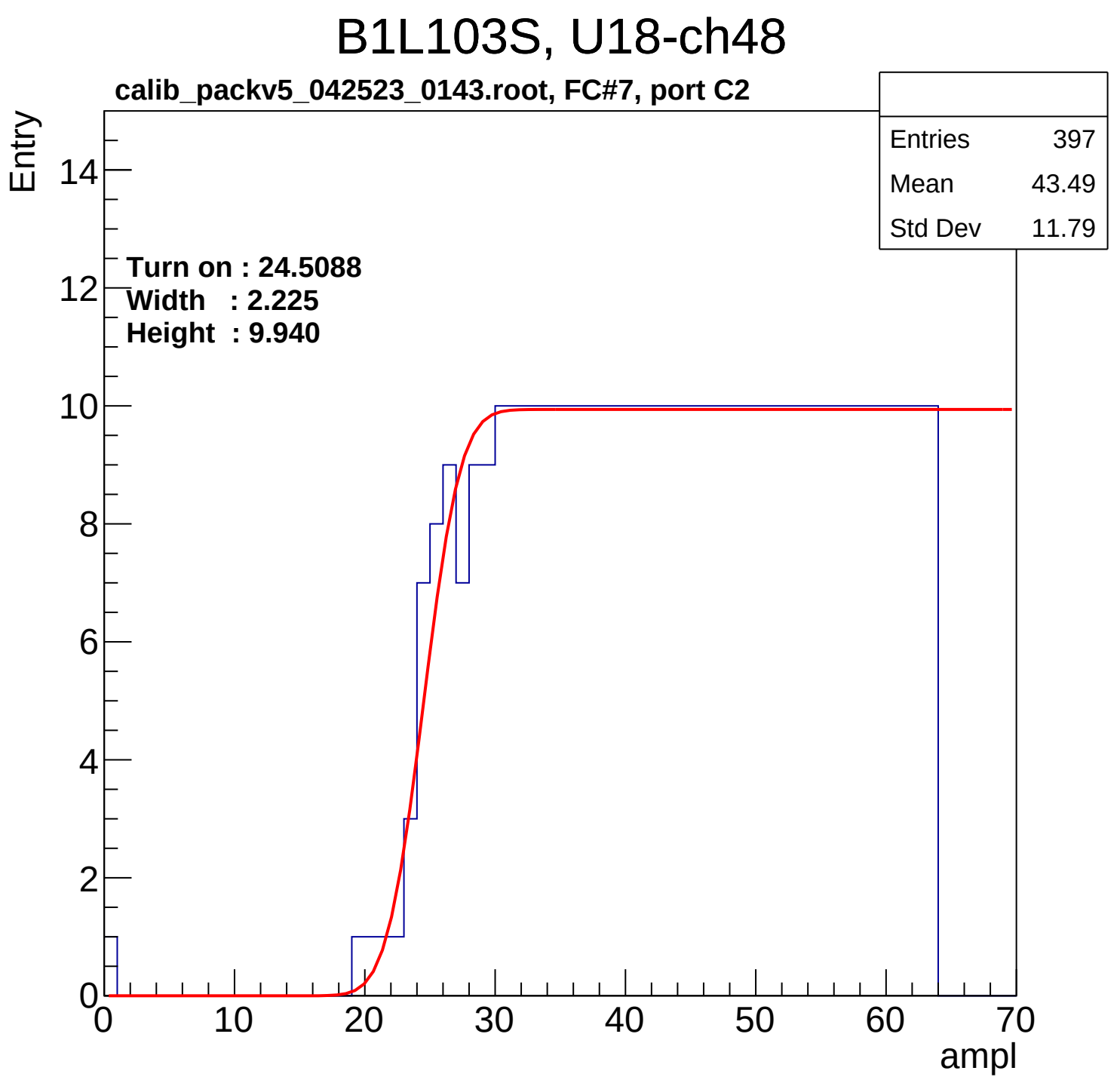
B1L103S, U18-ch48
calib_packv5_042523_0143.root, FC#7, port C2
Entries 397
Mean 43.49
Std Dev 11.79
Turn on : 24.5088
Width : 2.225
Height : 9.940
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ampl
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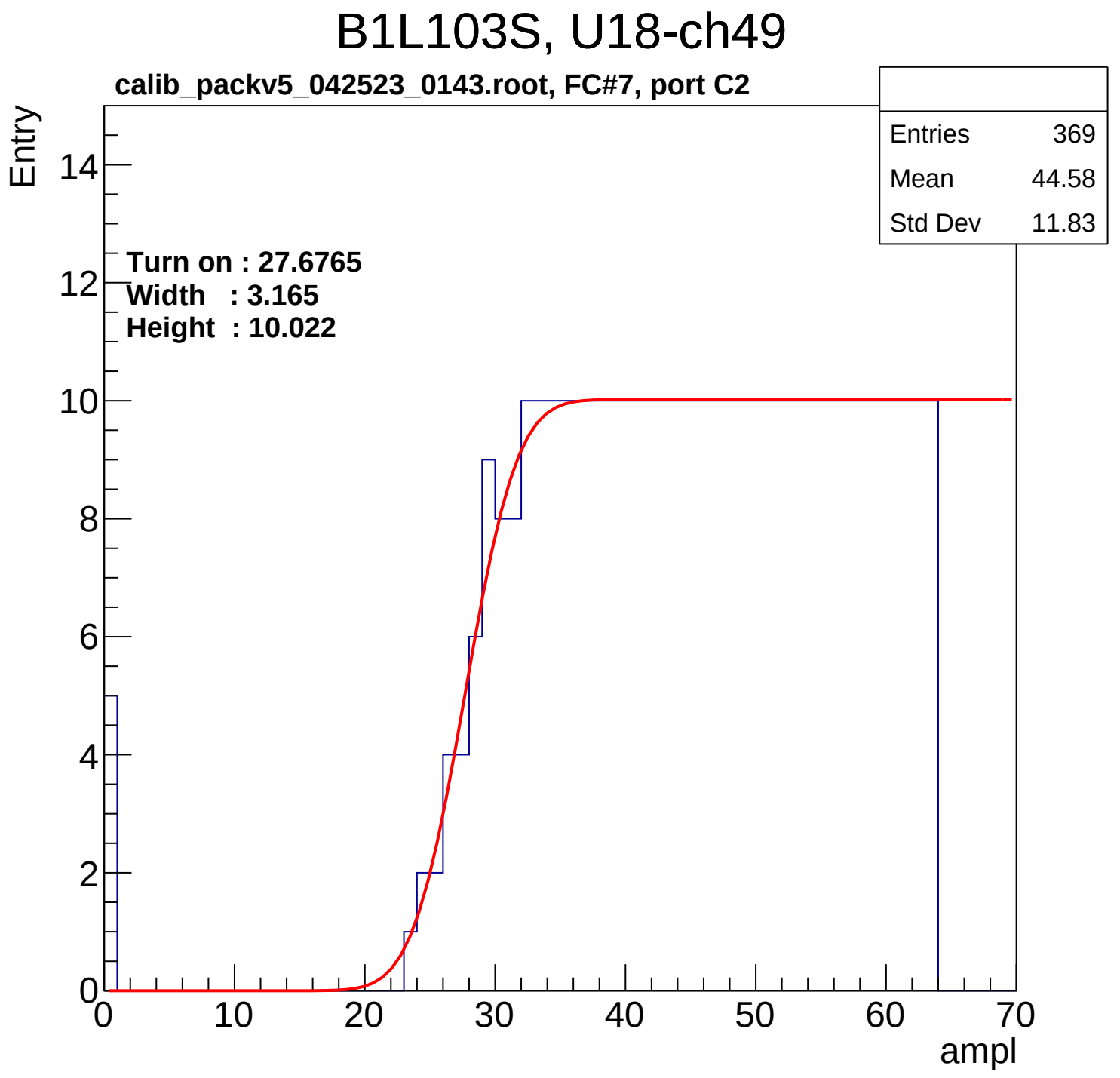
B1L103S, U18-ch49
calib_packv5_042523_0143.root, FC#7, port C2
Entries 369
Mean 44.58
Std Dev 11.83
Turn on : 27.6765
Width : 3.165
Height : 10.022
Entry
ampl
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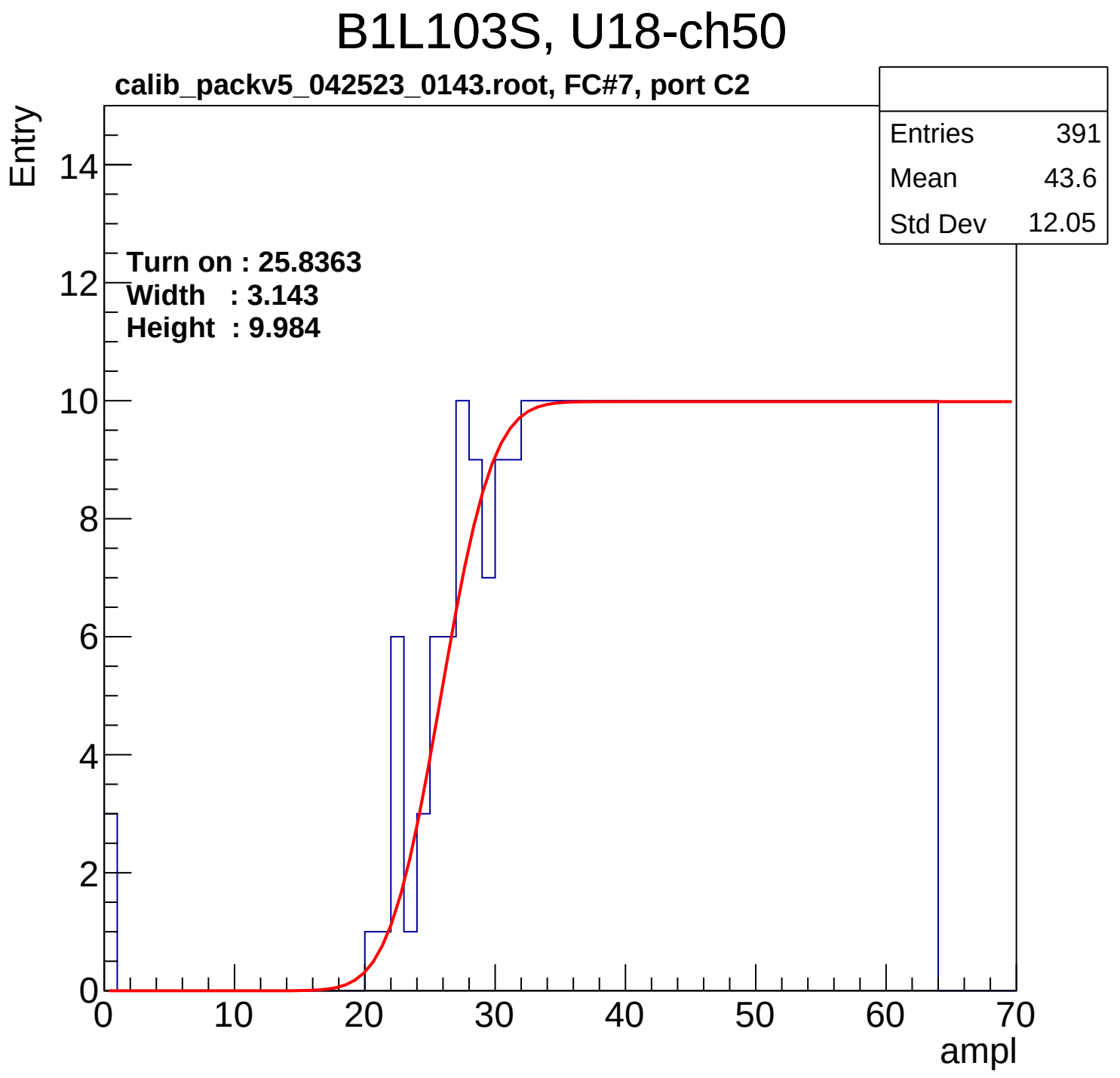
B1L103S, U18-ch50
calib_packv5_042523_0143.root, FC#7, port C2
Entries 391
Mean 43.6
Std Dev 12.05
Turn on : 25.8363
Width : 3.143
Height : 9.984
Entry
ampl
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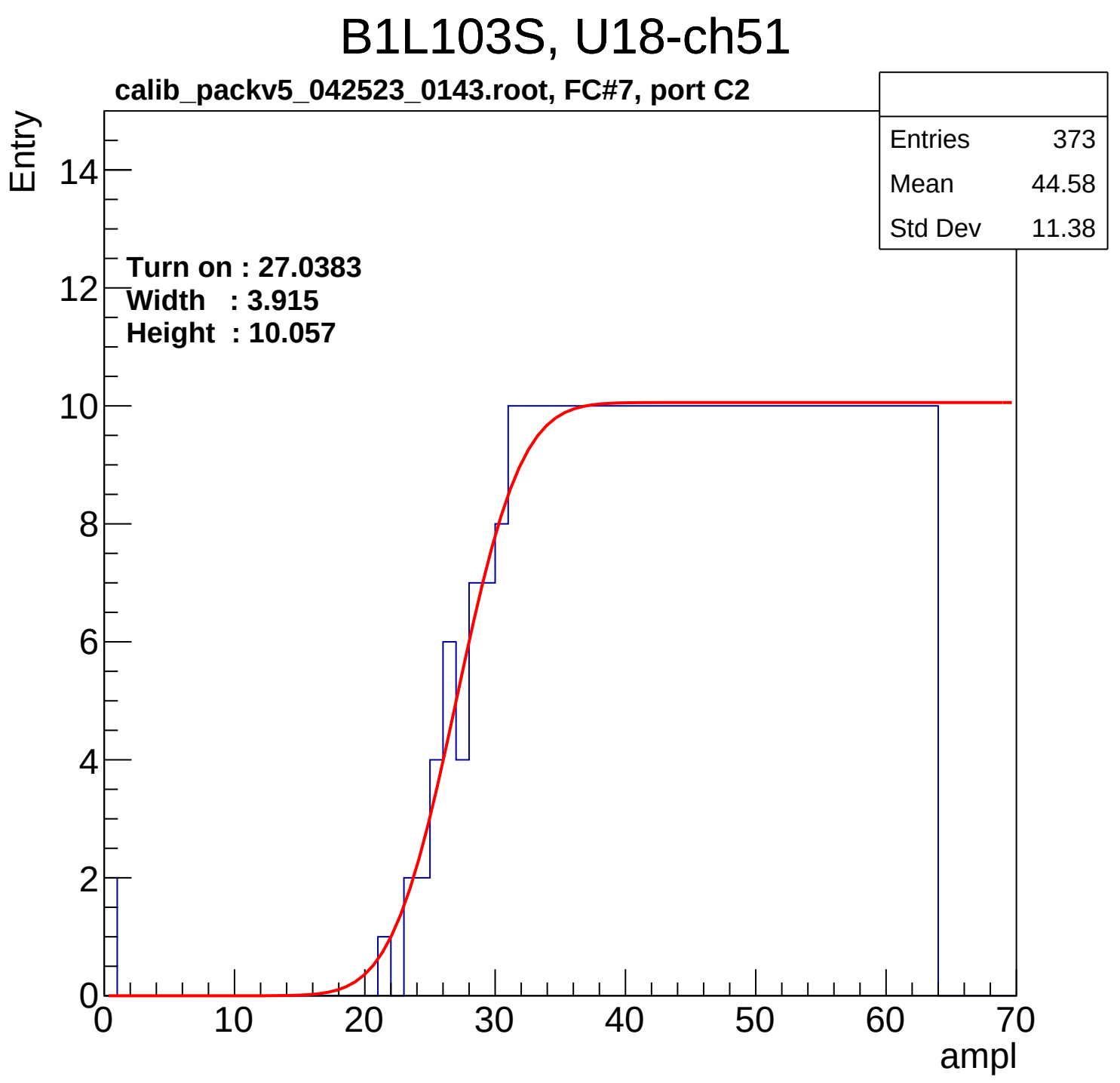
B1L103S, U18-ch51
calib_packv5_042523_0143.root, FC#7, port C2
Entries 373
Mean 44.58
Std Dev 11.38
Turn on : 27.0383
Width : 3.915
Height : 10.057
Entry
ampl
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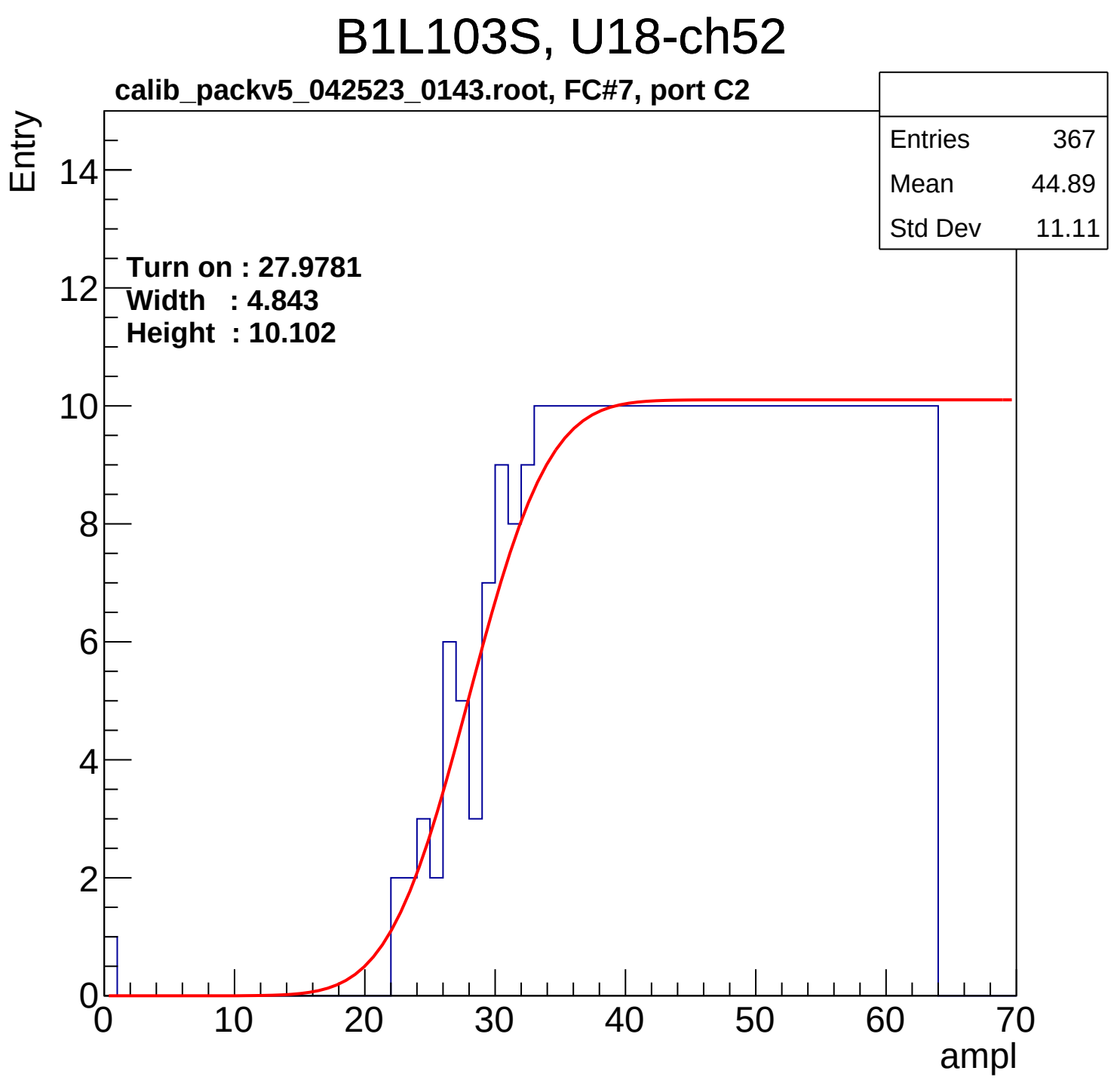
B1L103S, U18-ch52
calib_packv5_042523_0143.root, FC#7, port C2
Entries 367
Mean 44.89
Std Dev 11.11
Turn on : 27.9781
Width : 4.843
Height : 10.102
Entry
ampl
0
2
4
6
8
10
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60
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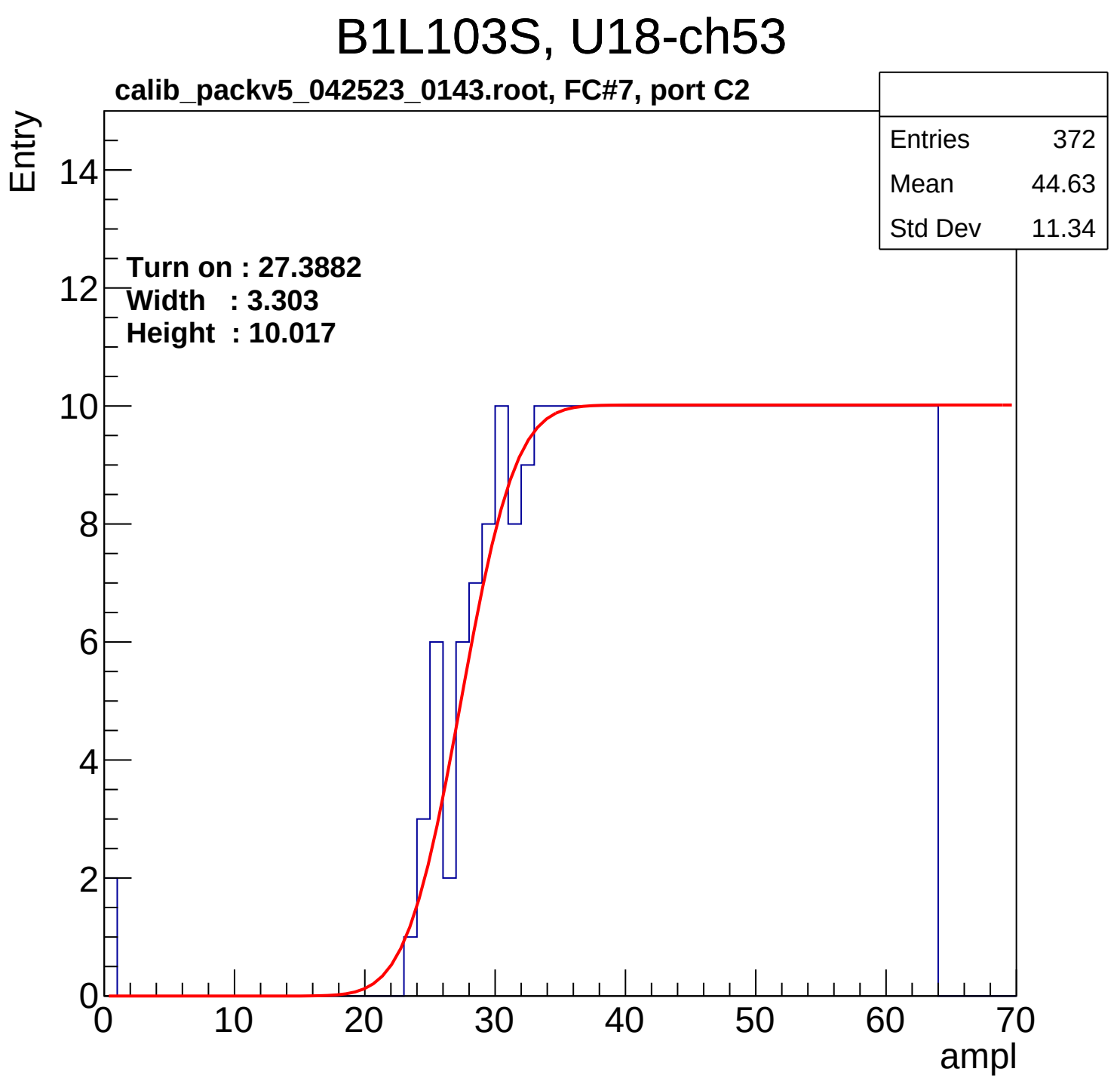
B1L103S, U18-ch53
calib_packv5_042523_0143.root, FC#7, port C2
Entries 372
Mean 44.63
Std Dev 11.34
Turn on : 27.3882
Width : 3.303
Height : 10.017
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ampl
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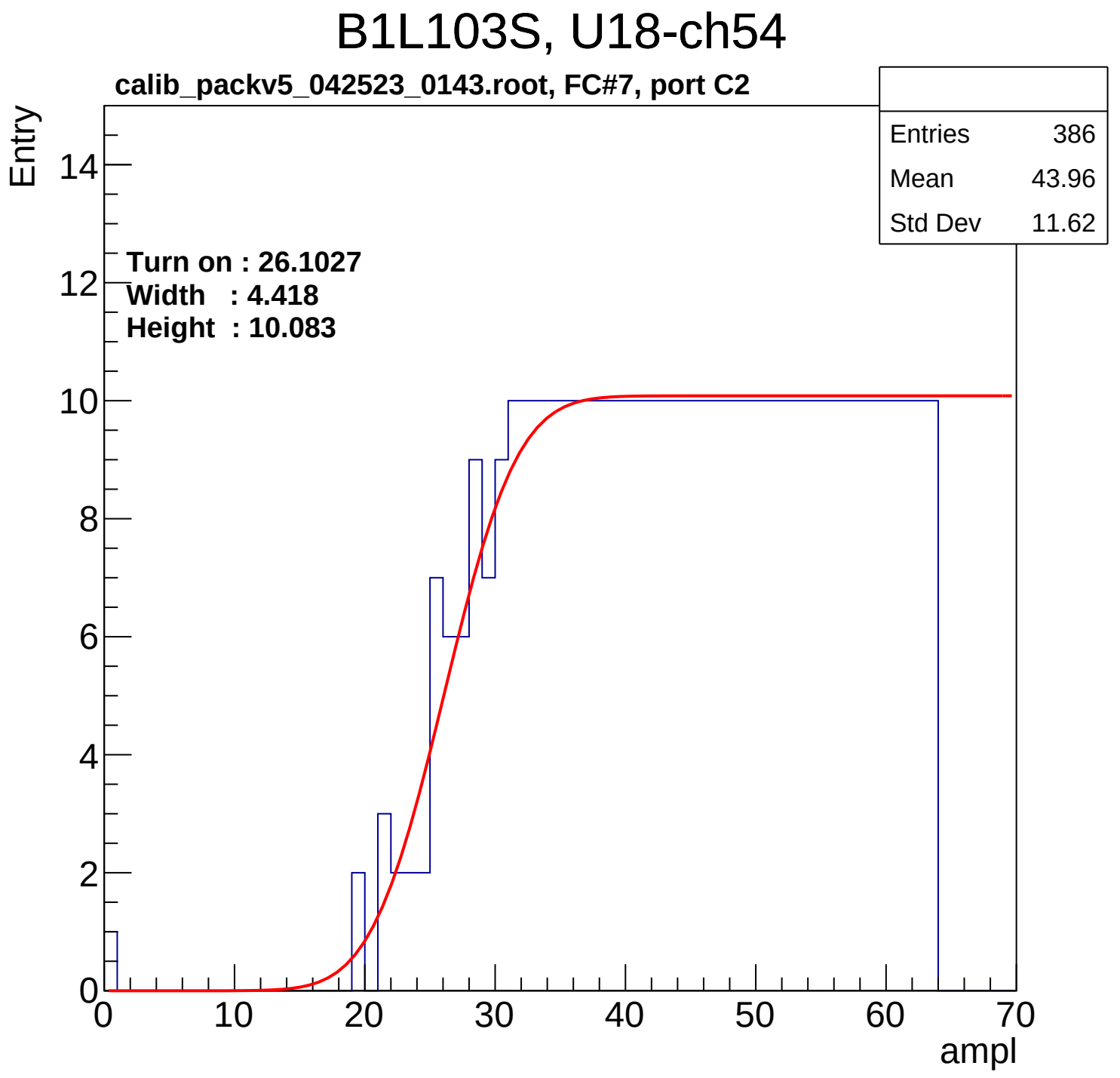
B1L103S, U18-ch54
calib_packv5_042523_0143.root, FC#7, port C2
Entries 386
Mean 43.96
Std Dev 11.62
Turn on : 26.1027
Width : 4.418
Height : 10.083
Entry
ampl
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4
6
8
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60
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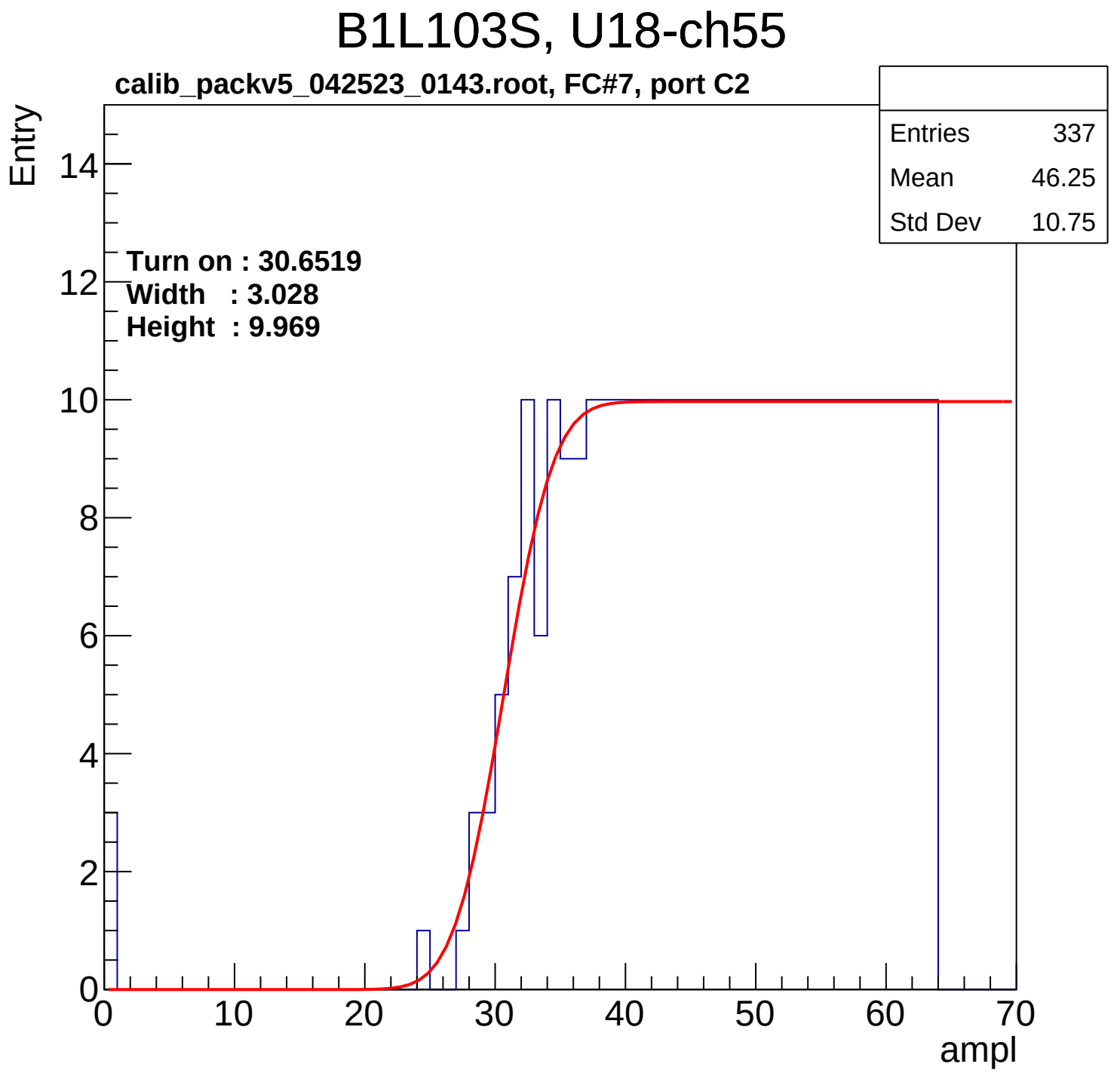
B1L103S, U18-ch55
calib_packv5_042523_0143.root, FC#7, port C2
Entries 337
Mean 46.25
Std Dev 10.75
Turn on : 30.6519
Width : 3.028
Height : 9.969
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ampl
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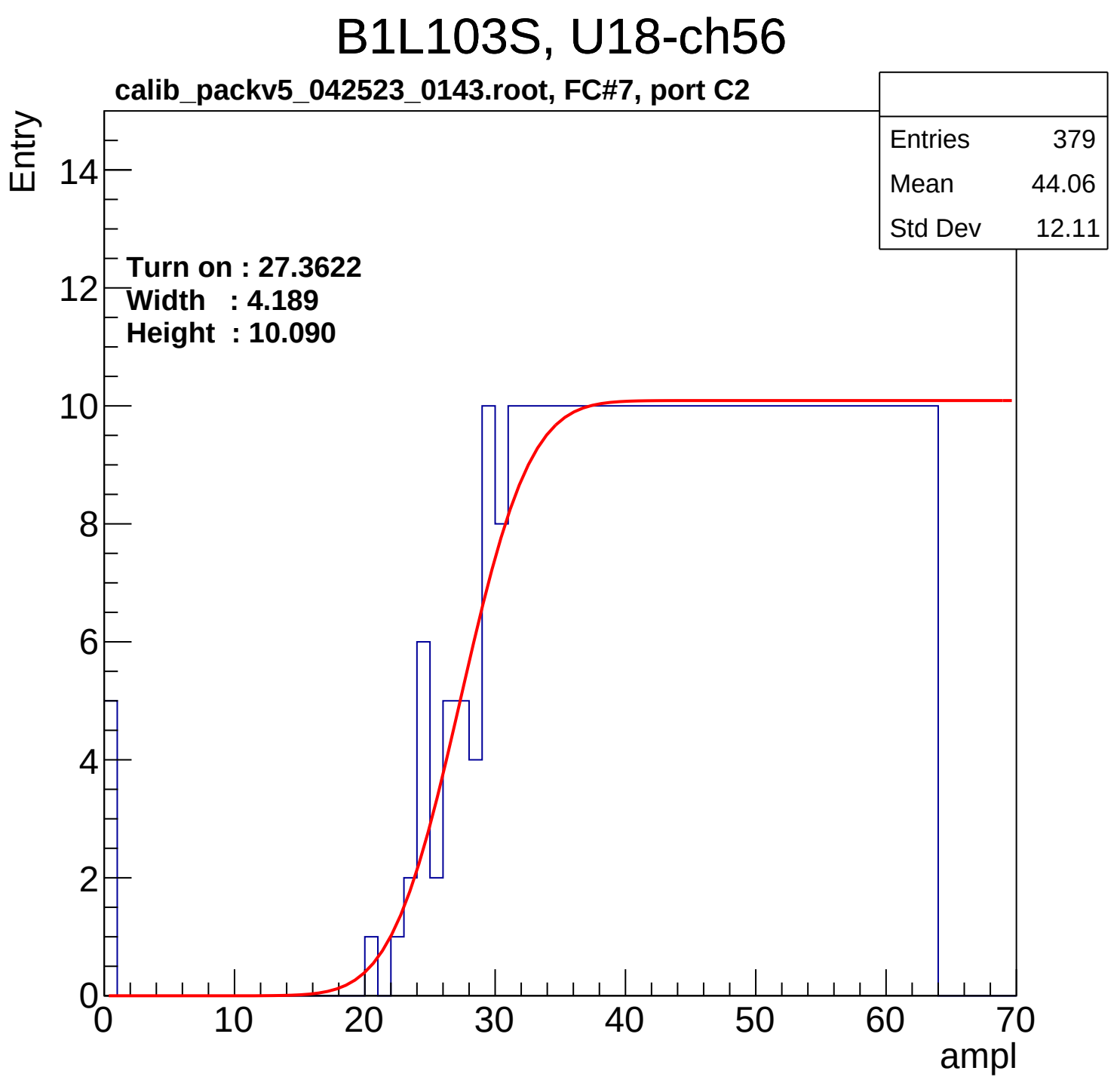
B1L103S, U18-ch56
calib_packv5_042523_0143.root, FC#7, port C2
Entries 379
Mean 44.06
Std Dev 12.11
Turn on : 27.3622
Width : 4.189
Height : 10.090
Entry
ampl
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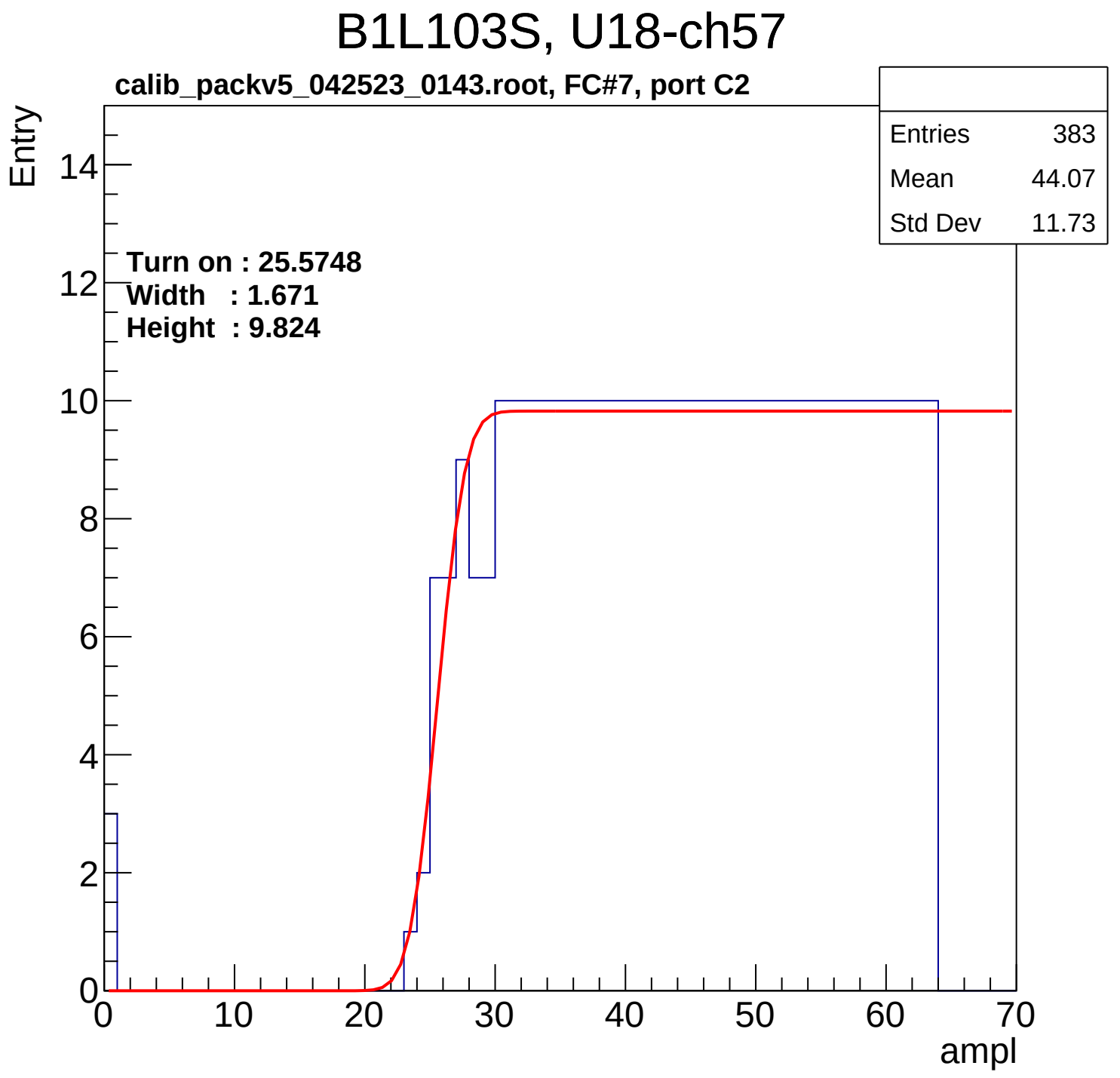
B1L103S, U18-ch57
calib_packv5_042523_0143.root, FC#7, port C2
Entries 383
Mean 44.07
Std Dev 11.73
Turn on : 25.5748
Width : 1.671
Height : 9.824
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
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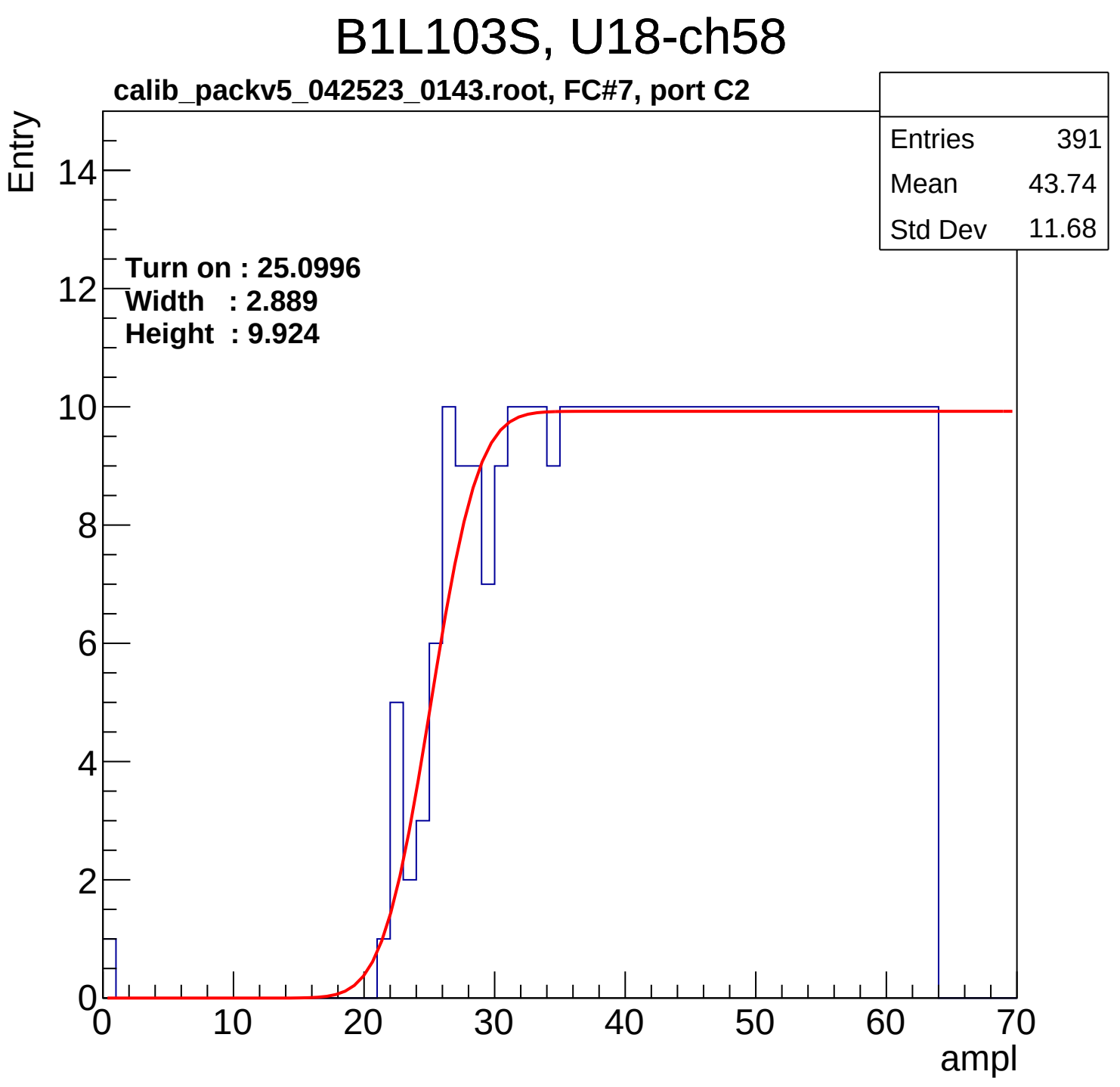
B1L103S, U18-ch58
calib_packv5_042523_0143.root, FC#7, port C2
Entries 391
Mean 43.74
Std Dev 11.68
Turn on : 25.0996
Width : 2.889
Height : 9.924
Entry
ampl
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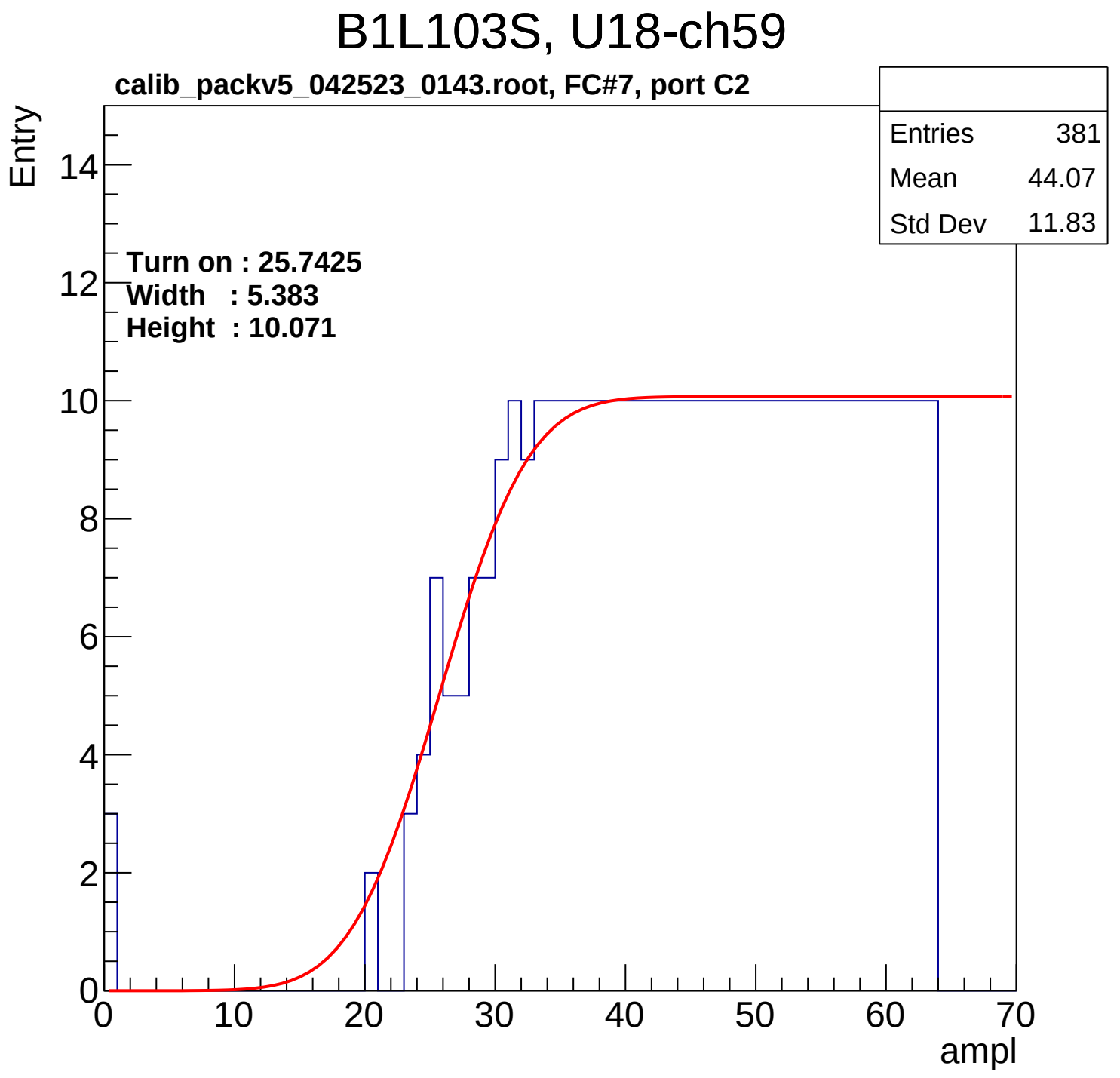
B1L103S, U18-ch59
calib_packv5_042523_0143.root, FC#7, port C2
Entries 381
Mean 44.07
Std Dev 11.83
Turn on : 25.7425
Width : 5.383
Height : 10.071
Entry
ampl
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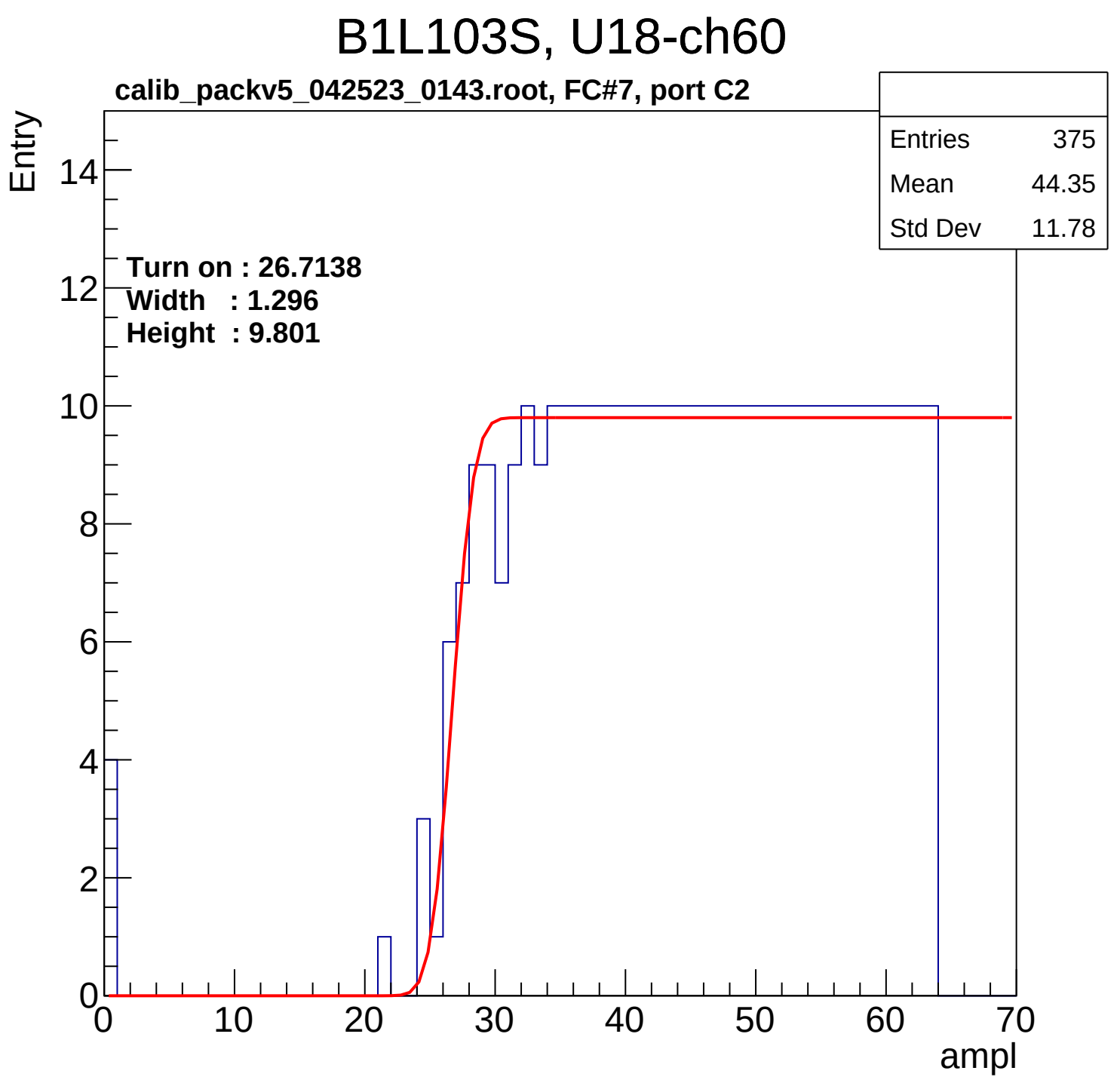
B1L103S, U18-ch60
calib_packv5_042523_0143.root, FC#7, port C2
Entries 375
Mean 44.35
Std Dev 11.78
Turn on : 26.7138
Width : 1.296
Height : 9.801
Entry
ampl
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8
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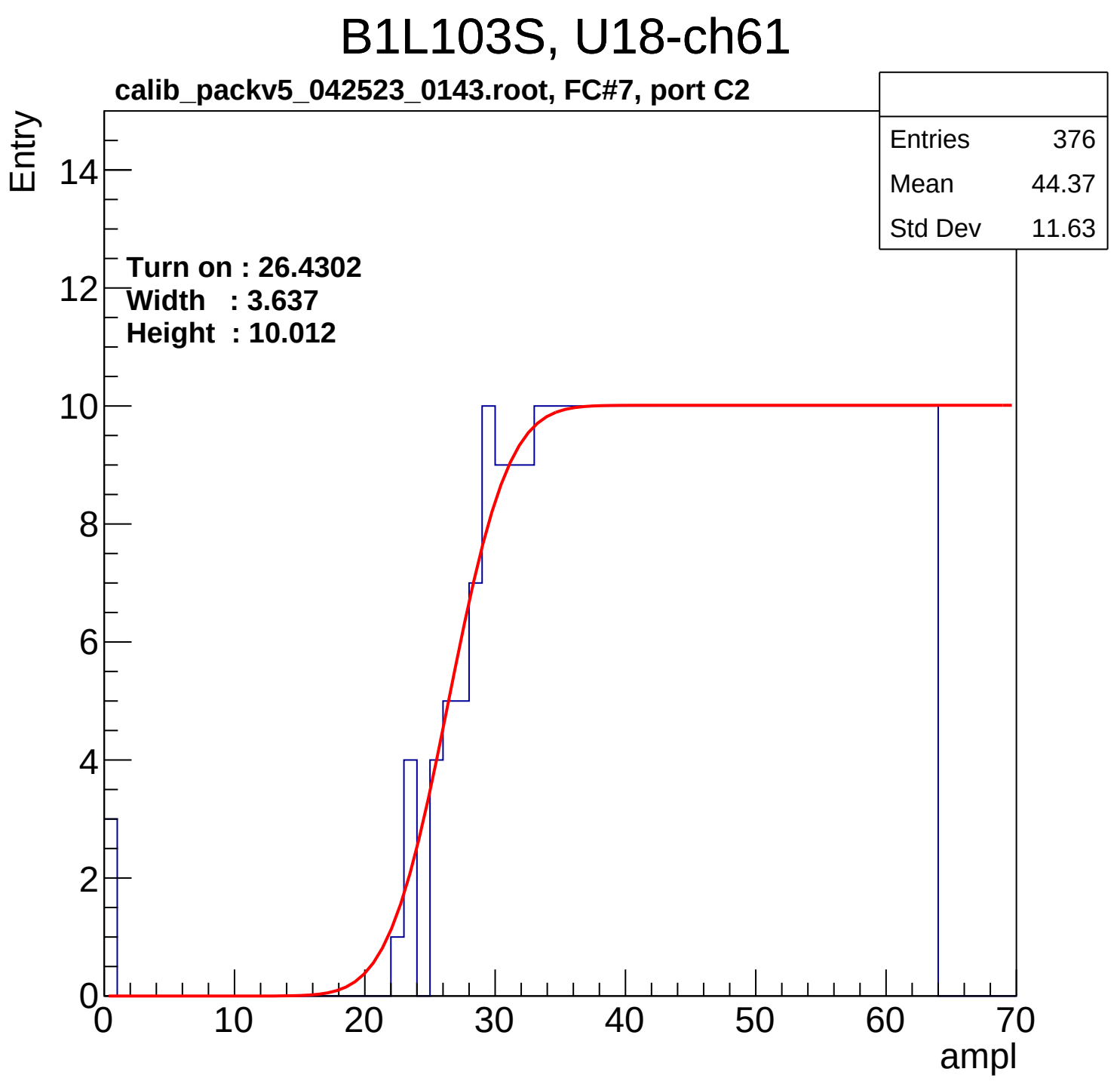
B1L103S, U18-ch61
calib_packv5_042523_0143.root, FC#7, port C2
Entries 376
Mean 44.37
Std Dev 11.63
Turn on : 26.4302
Width : 3.637
Height : 10.012
Entry
ampl
0
2
4
6
8
10
12
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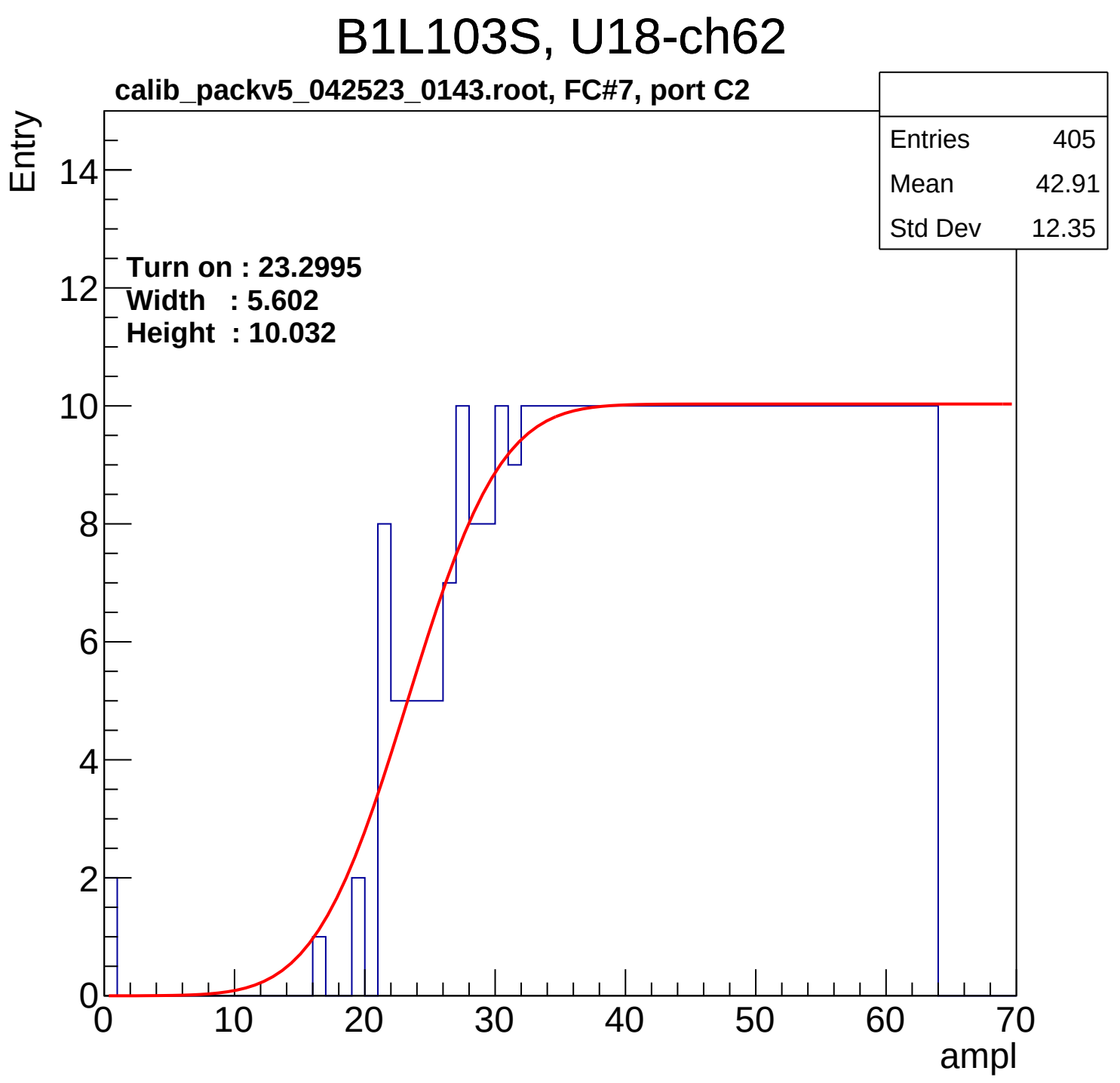
B1L103S, U18-ch62
calib_packv5_042523_0143.root, FC#7, port C2
Entries 405
Mean 42.91
Std Dev 12.35
Turn on : 23.2995
Width : 5.602
Height : 10.032
Entry
ampl
0
2
4
6
8
10
12
14
0
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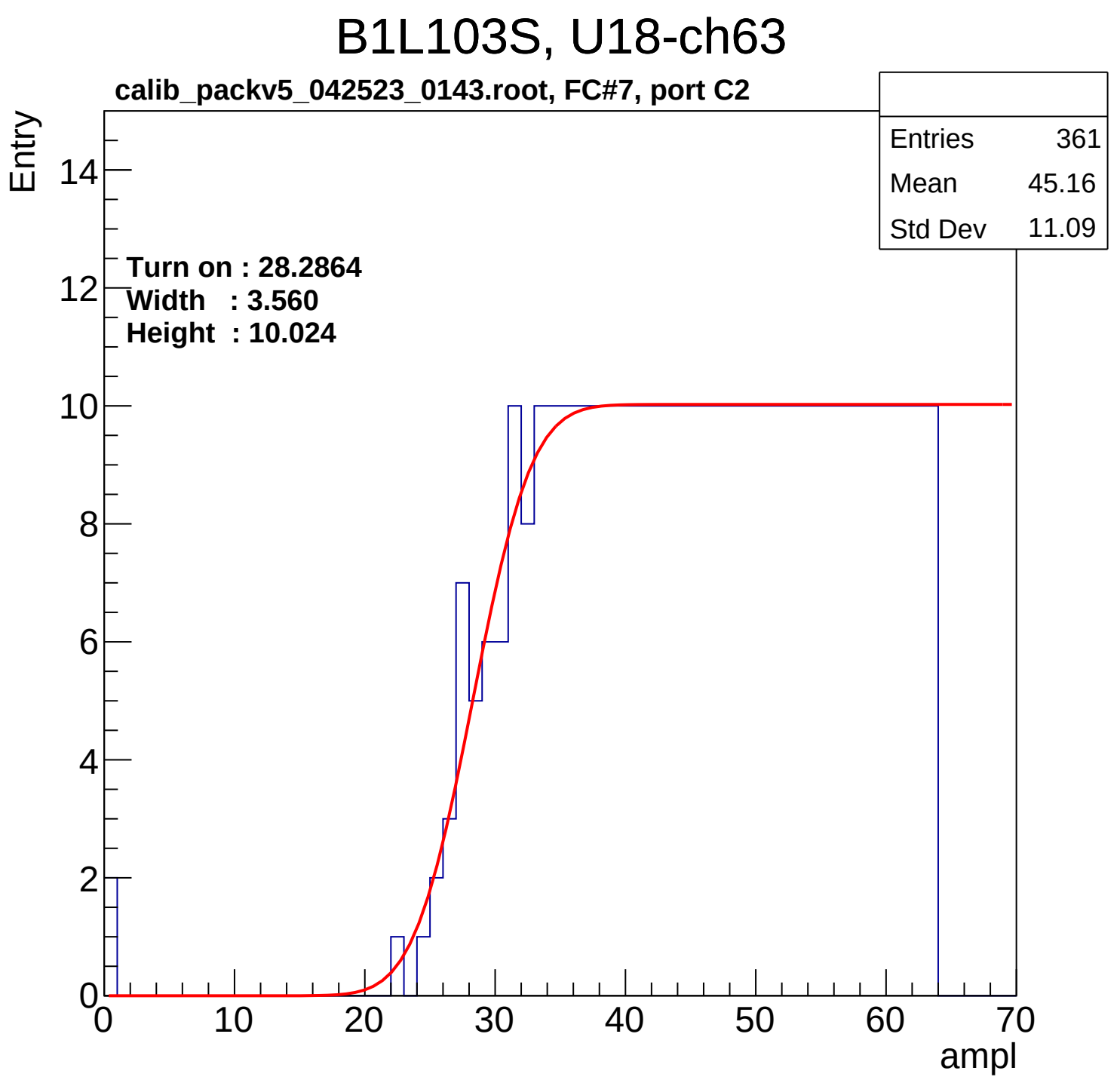
B1L103S, U18-ch63
calib_packv5_042523_0143.root, FC#7, port C2
Entries 361
Mean 45.16
Std Dev 11.09
Turn on : 28.2864
Width : 3.560
Height : 10.024
Entry
ampl
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2
4
6
8
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12
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0
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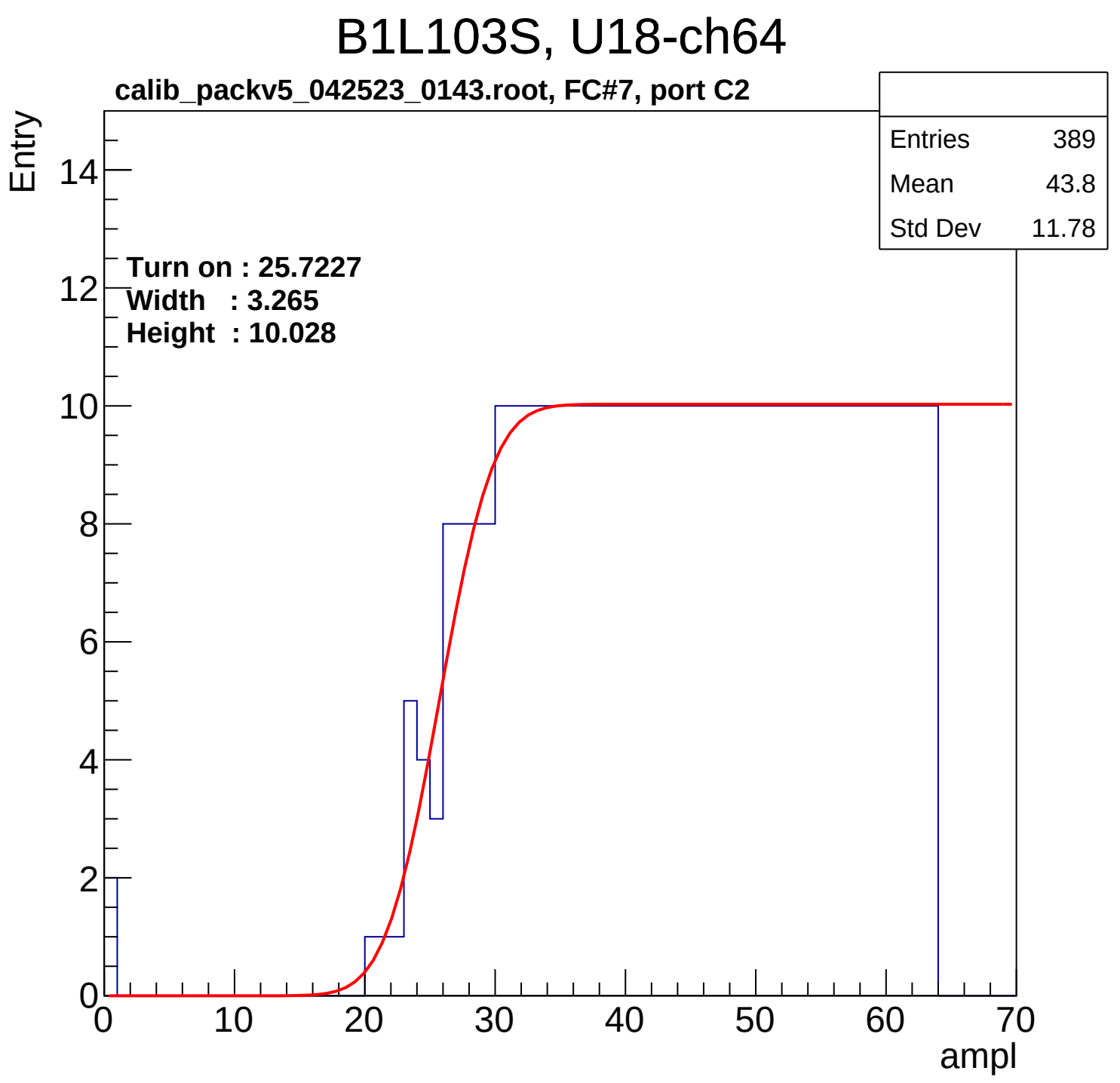
B1L103S, U18-ch64
calib_packv5_042523_0143.root, FC#7, port C2
Entries 389
Mean 43.8
Std Dev 11.78
Turn on : 25.7227
Width : 3.265
Height : 10.028
Entry
ampl
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2
4
6
8
10
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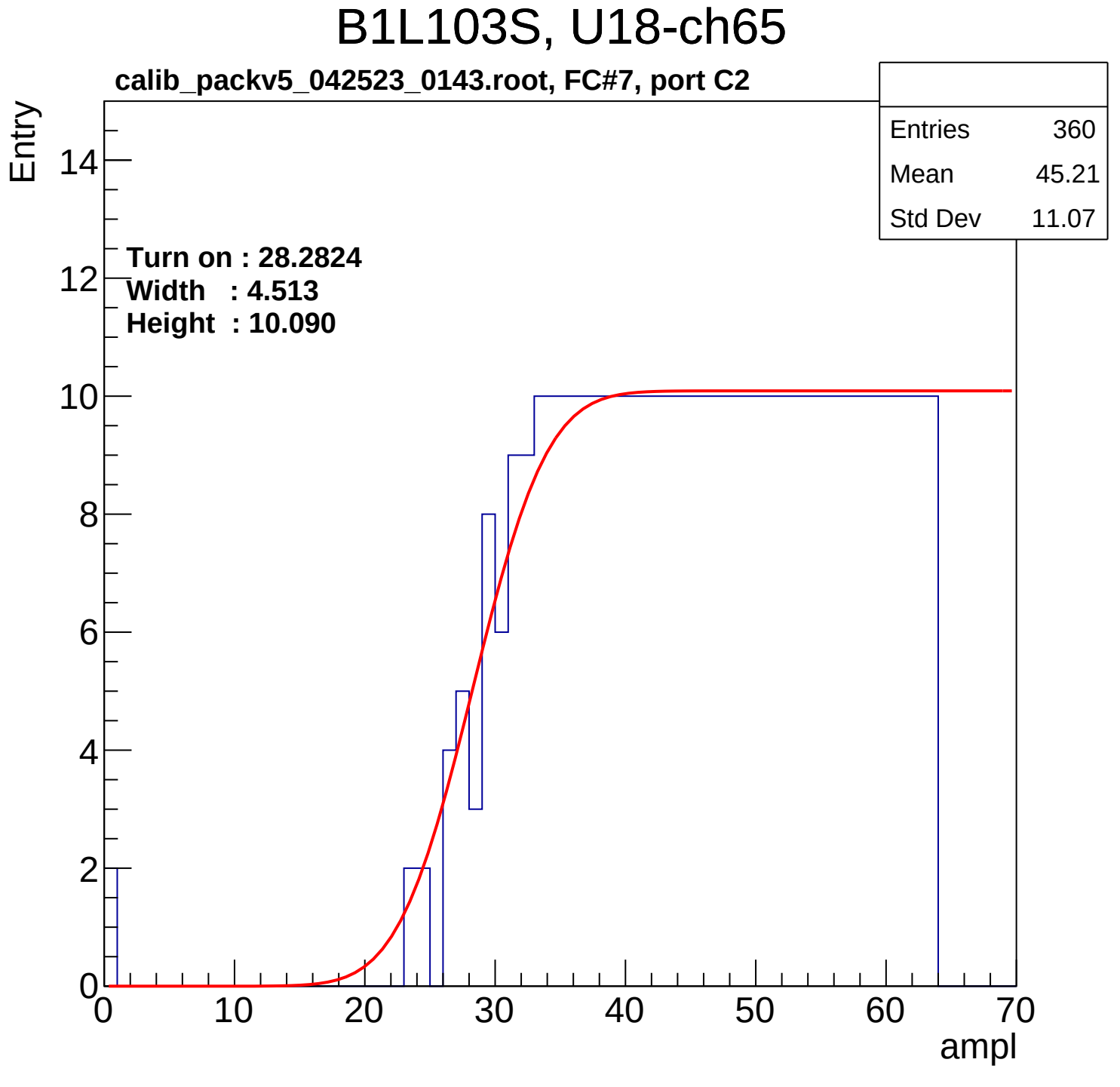
B1L103S, U18-ch65
calib_packv5_042523_0143.root, FC#7, port C2
Entries 360
Mean 45.21
Std Dev 11.07
Turn on : 28.2824
Width : 4.513
Height : 10.090
Entry
ampl
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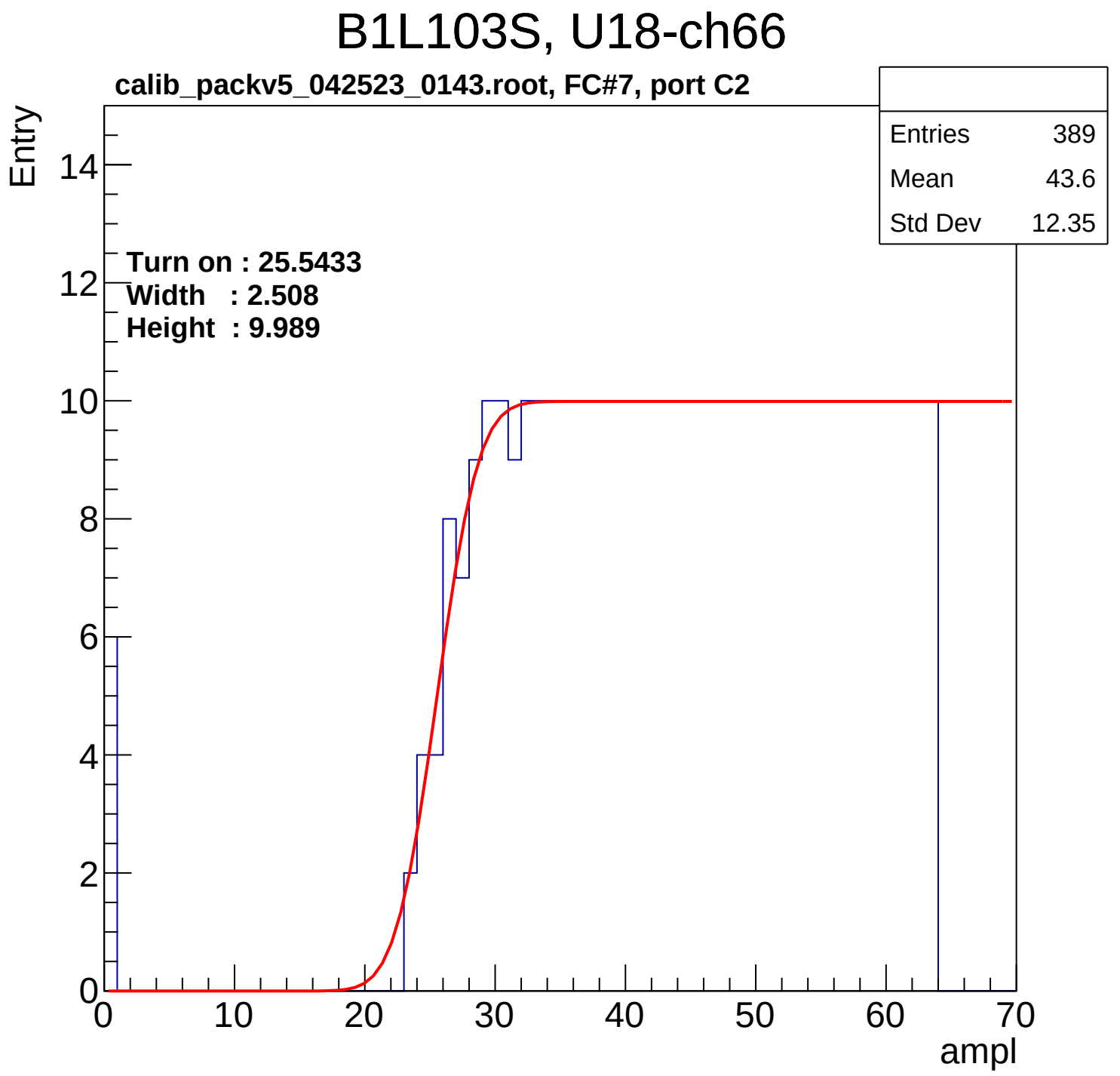
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U18-ch66
calib_packv5_042523_0143.root, FC#7, port C2
Entries 389
Mean 43.6
Std Dev 12.35
Turn on : 25.5433
Width : 2.508
Height : 9.989
Entry
ampl
0
2
4
6
8
10
12
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0
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20
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40
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60
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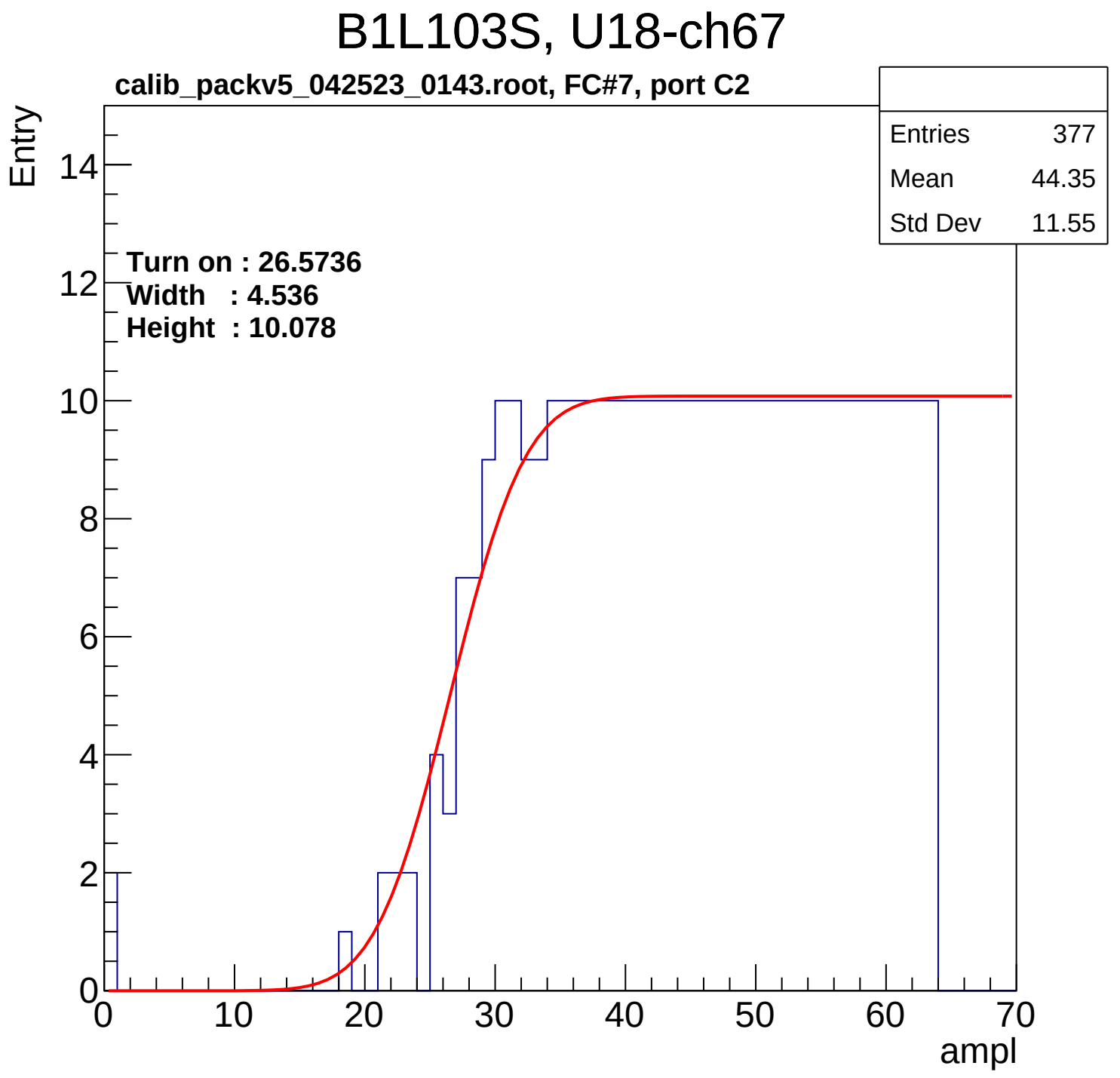
B1L103S, U18-ch67
calib_packv5_042523_0143.root, FC#7, port C2
Entries 377
Mean 44.35
Std Dev 11.55
Turn on : 26.5736
Width : 4.536
Height : 10.078
Entry
ampl
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2
4
6
8
10
12
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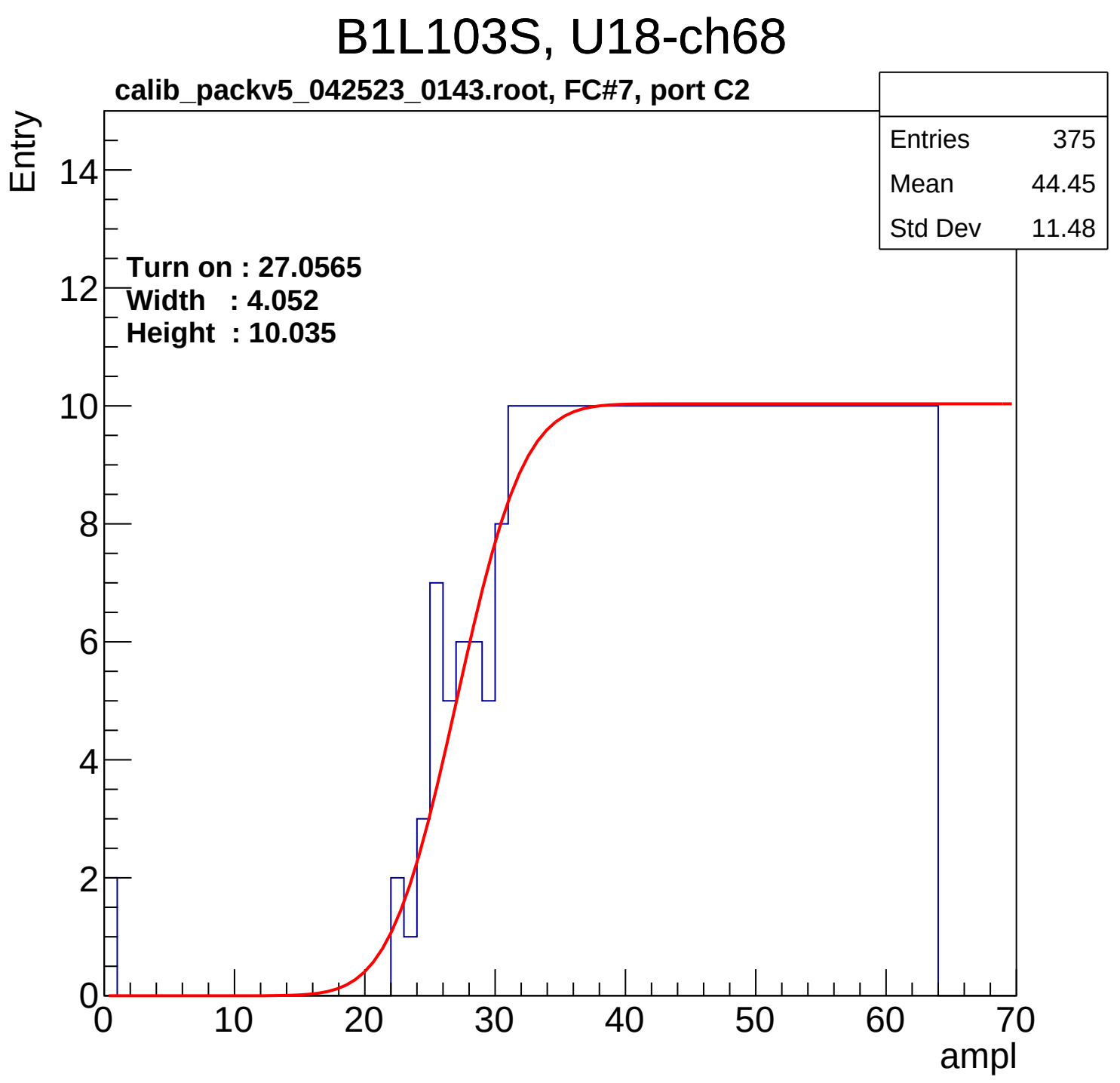
B1L103S, U18-ch68
calib_packv5_042523_0143.root, FC#7, port C2
Entries 375
Mean 44.45
Std Dev 11.48
Turn on : 27.0565
Width : 4.052
Height : 10.035
Entry
ampl
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6
8
10
12
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0
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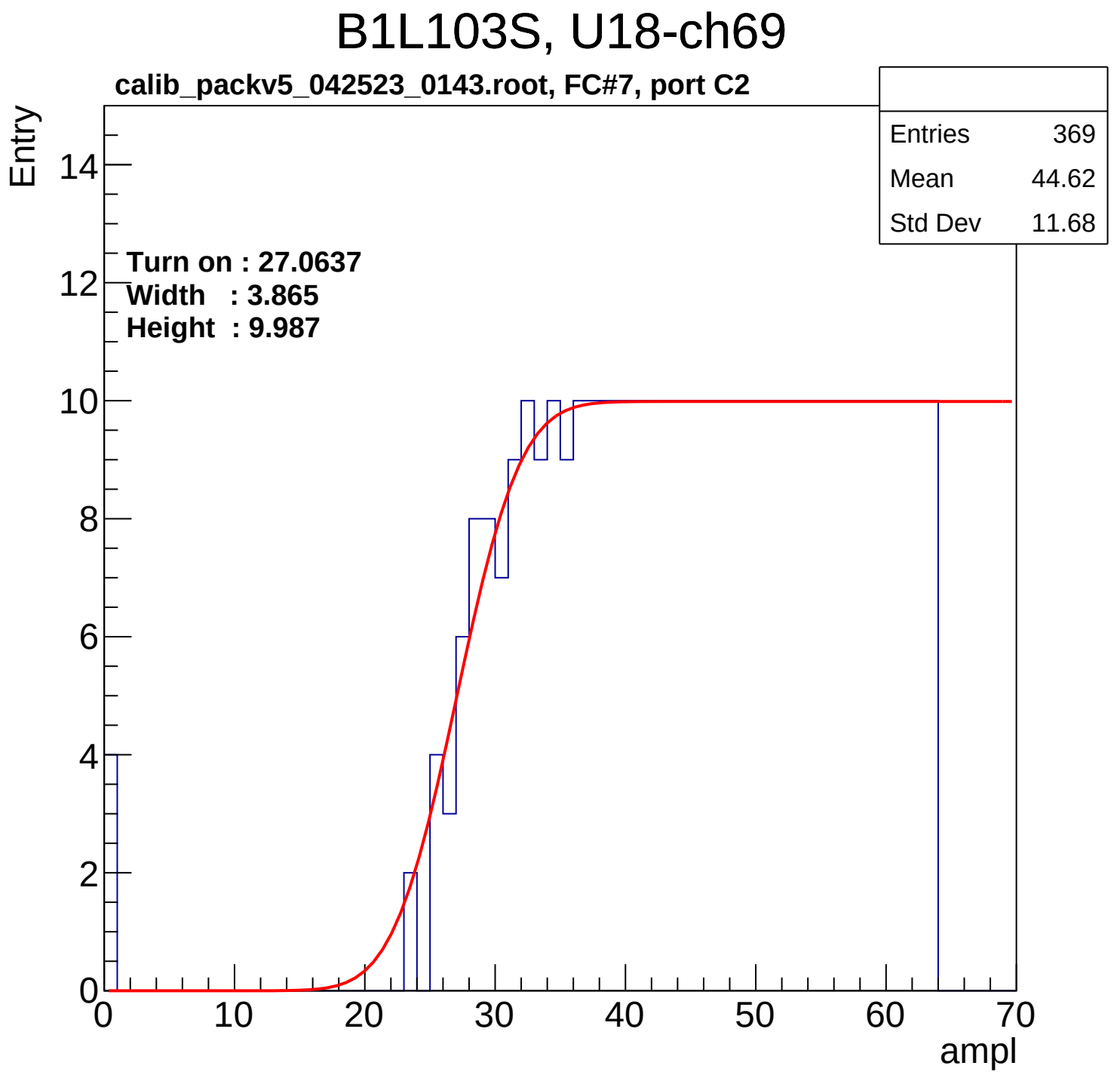
B1L103S, U18-ch69
calib_packv5_042523_0143.root, FC#7, port C2
Entries 369
Mean 44.62
Std Dev 11.68
Turn on : 27.0637
Width : 3.865
Height : 9.987
Entry
ampl
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6
8
10
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60
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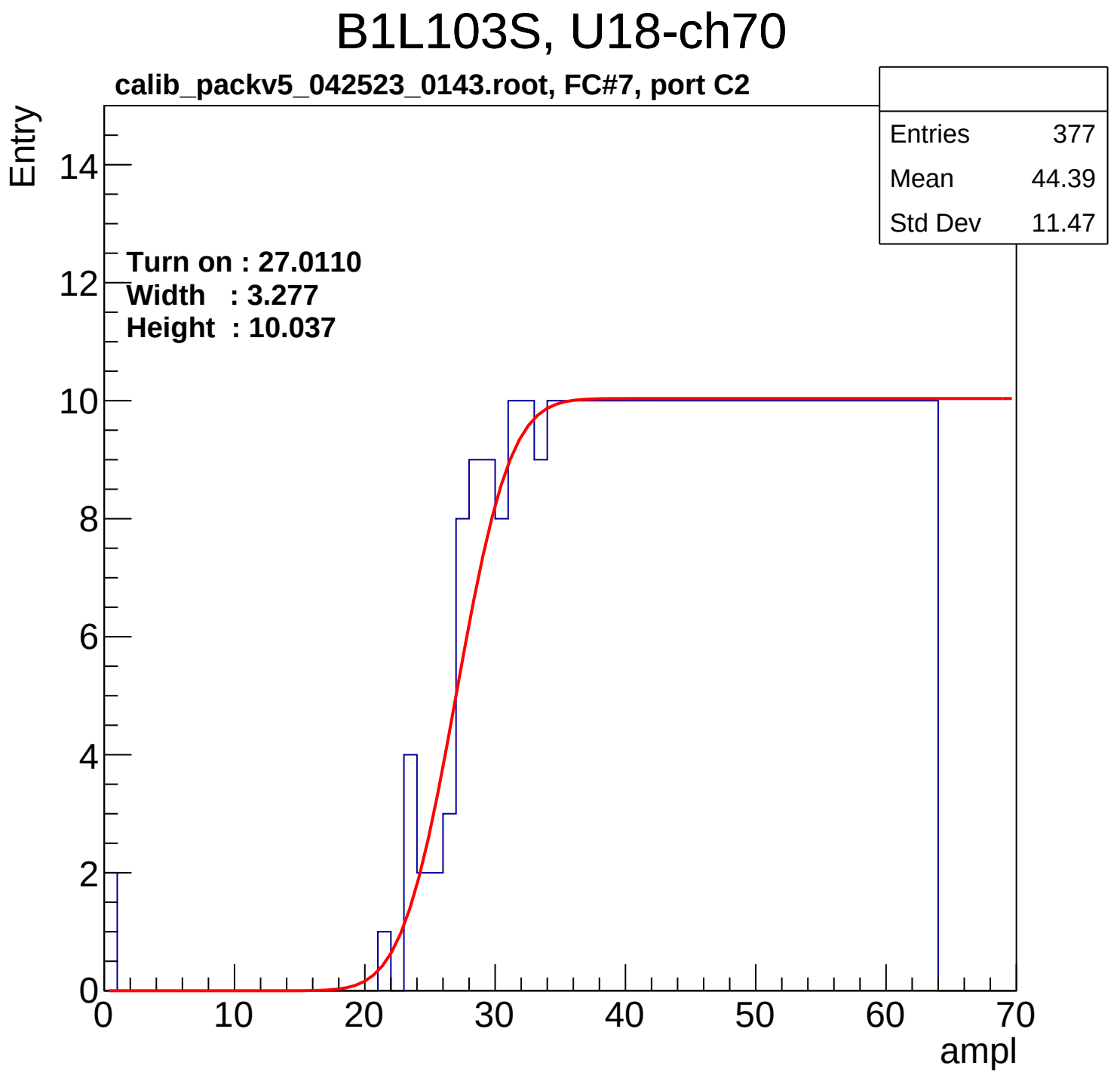
B1L103S, U18-ch70
calib_packv5_042523_0143.root, FC#7, port C2
Entries 377
Mean 44.39
Std Dev 11.47
Turn on : 27.0110
Width : 3.277
Height : 10.037
Entry
ampl
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6
8
10
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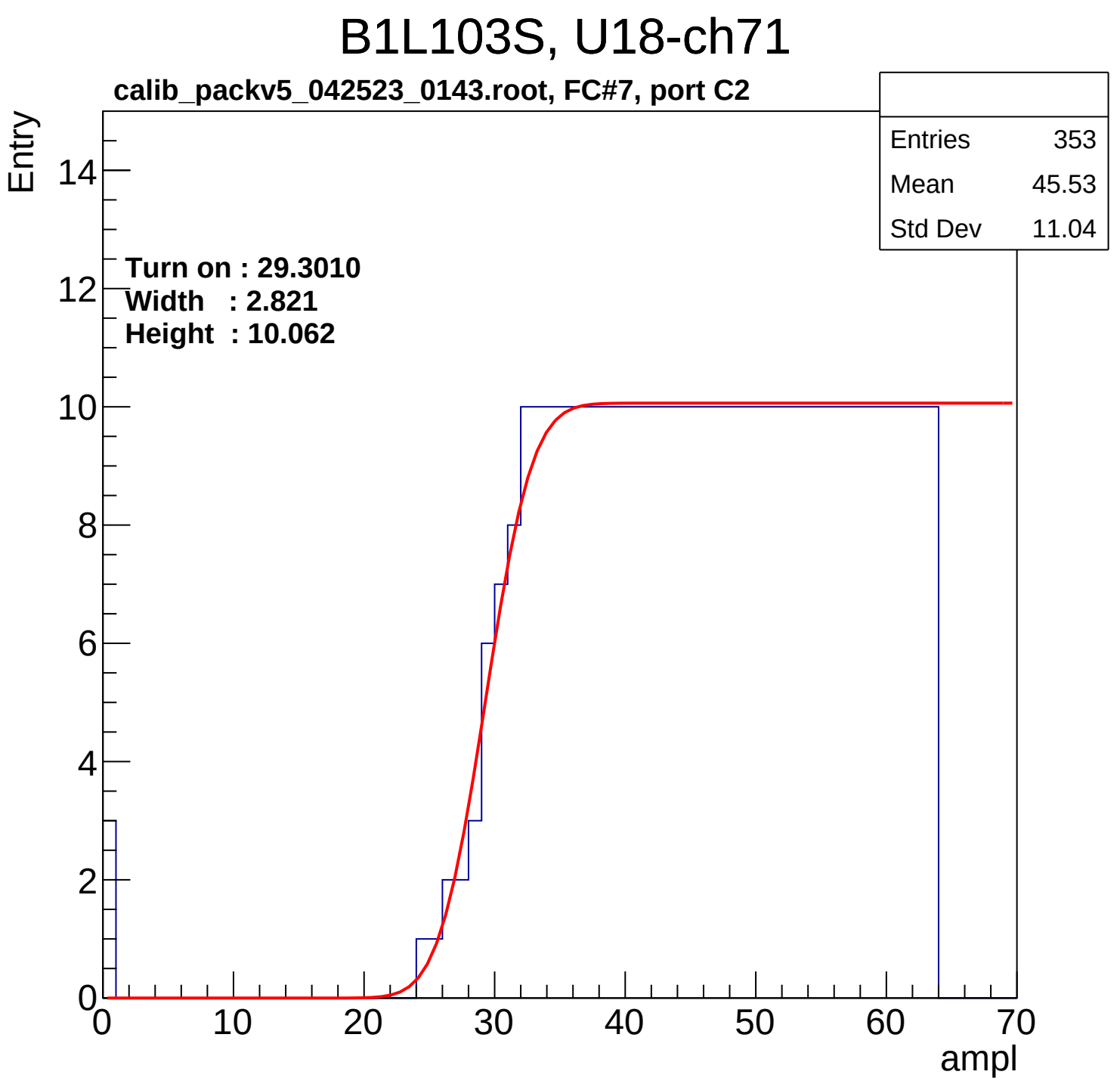
B1L103S, U18-ch71
calib_packv5_042523_0143.root, FC#7, port C2
Entries 353
Mean 45.53
Std Dev 11.04
Turn on : 29.3010
Width : 2.821
Height : 10.062
Entry
ampl
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6
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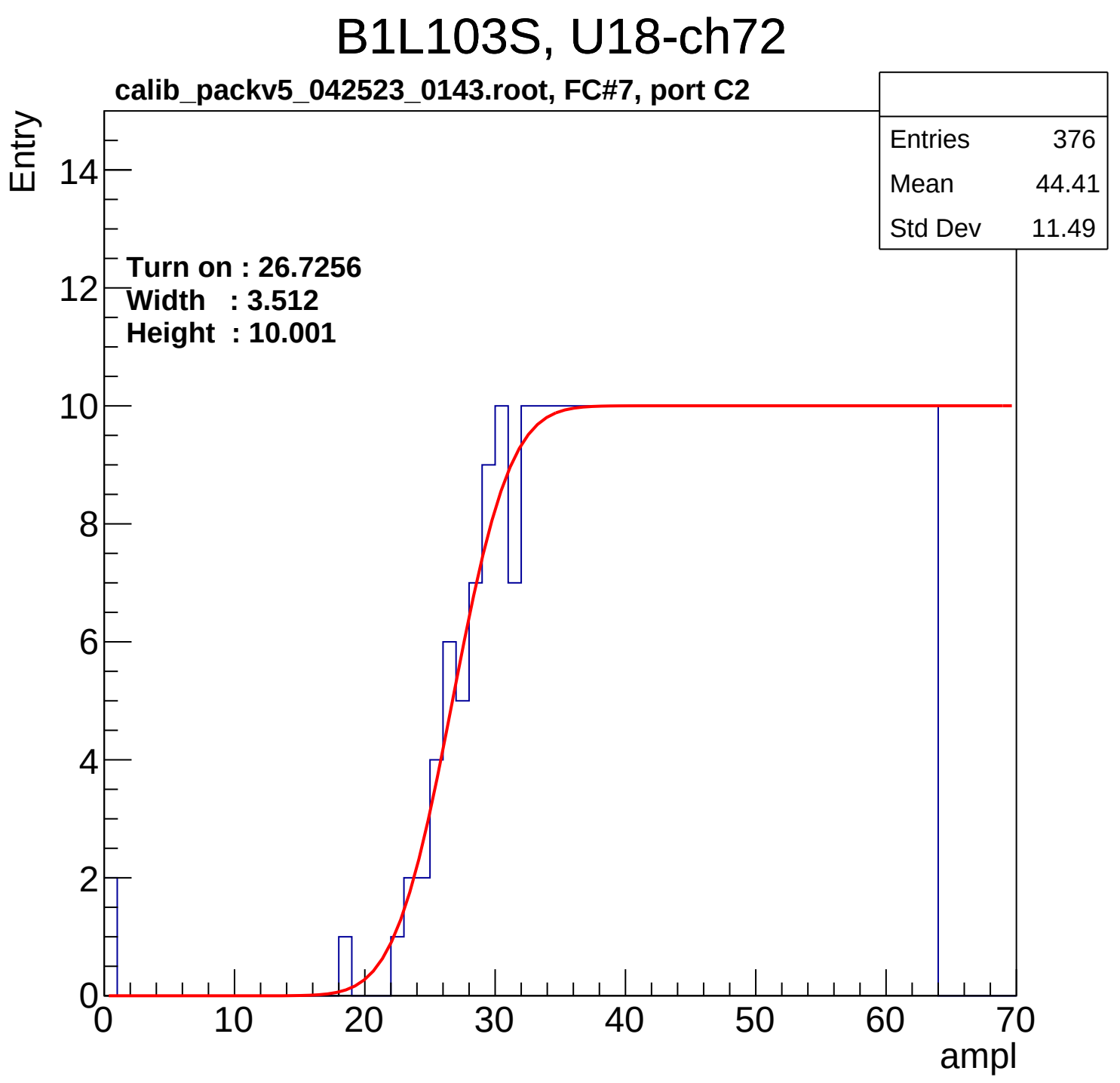
B1L103S, U18-ch72
calib_packv5_042523_0143.root, FC#7, port C2
Entries 376
Mean 44.41
Std Dev 11.49
Turn on : 26.7256
Width : 3.512
Height : 10.001
Entry
ampl
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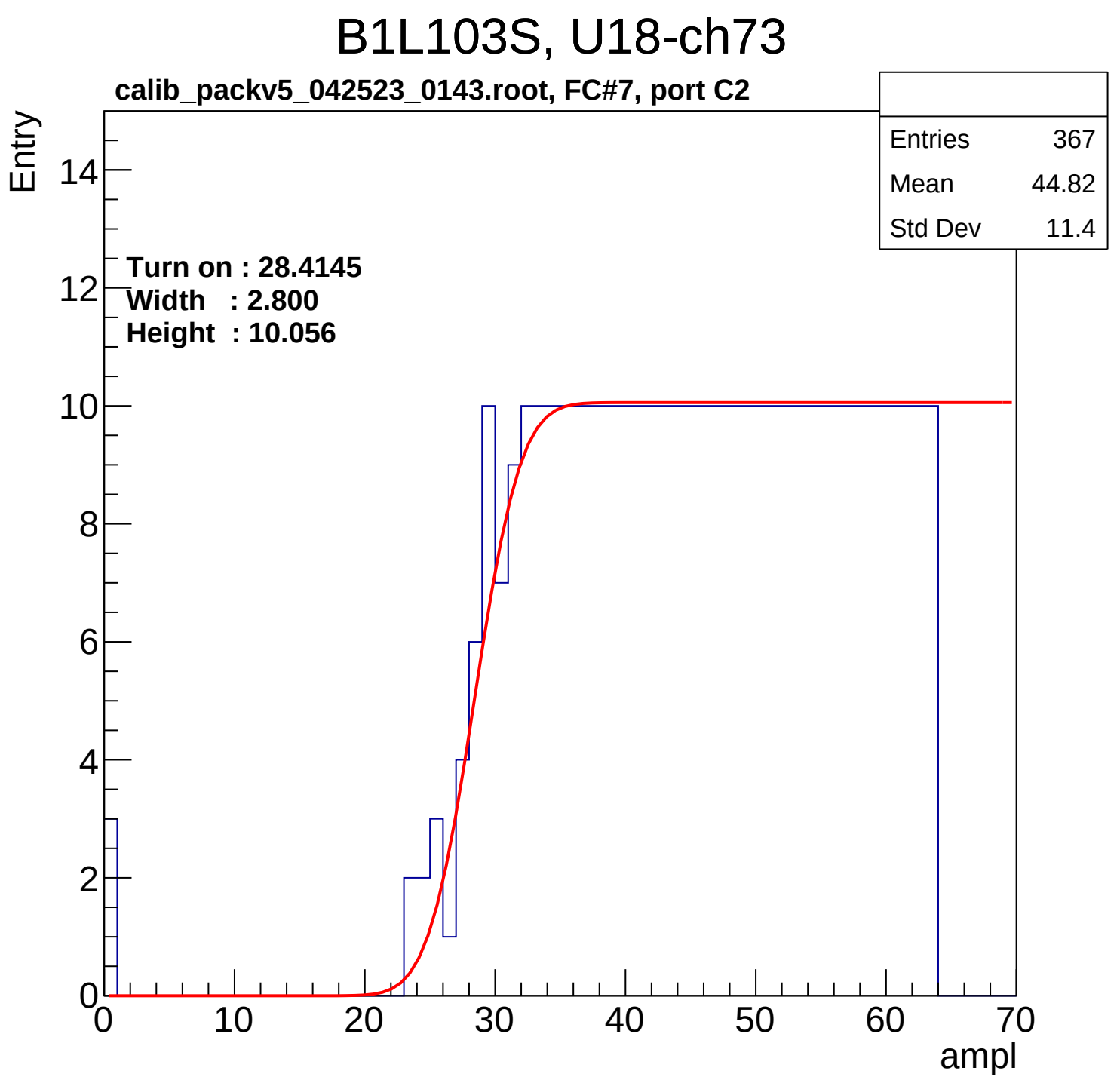
B1L103S, U18-ch73
calib_packv5_042523_0143.root, FC#7, port C2
Entries 367
Mean 44.82
Std Dev 11.4
Turn on : 28.4145
Width : 2.800
Height : 10.056
Entry
ampl
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8
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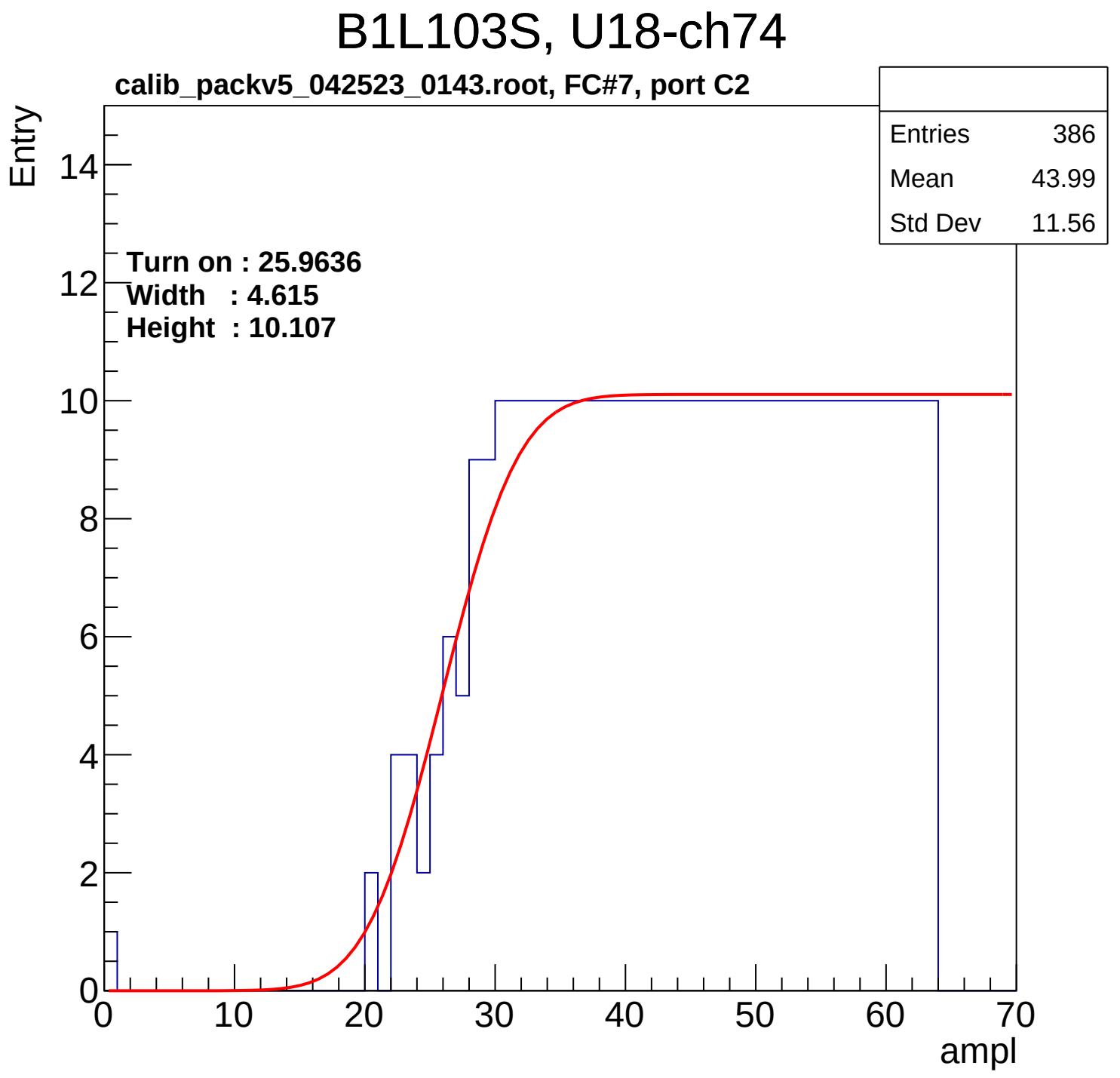
B1L103S, U18-ch74
calib_packv5_042523_0143.root, FC#7, port C2
Entries 386
Mean 43.99
Std Dev 11.56
Turn on : 25.9636
Width : 4.615
Height : 10.107
Entry
ampl
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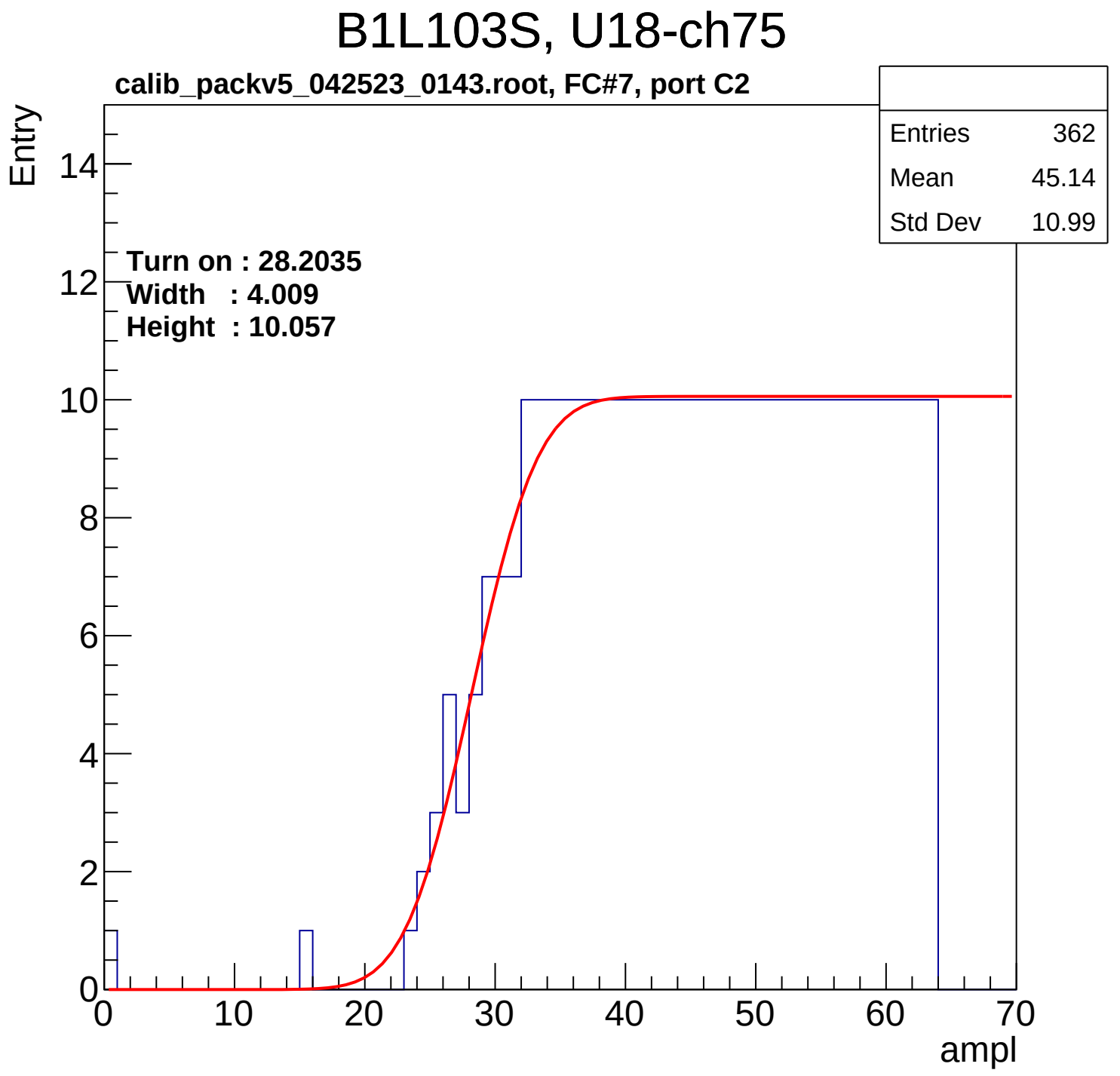
B1L103S, U18-ch75
calib_packv5_042523_0143.root, FC#7, port C2
Entries 362
Mean 45.14
Std Dev 10.99
Turn on : 28.2035
Width : 4.009
Height : 10.057
Entry
ampl
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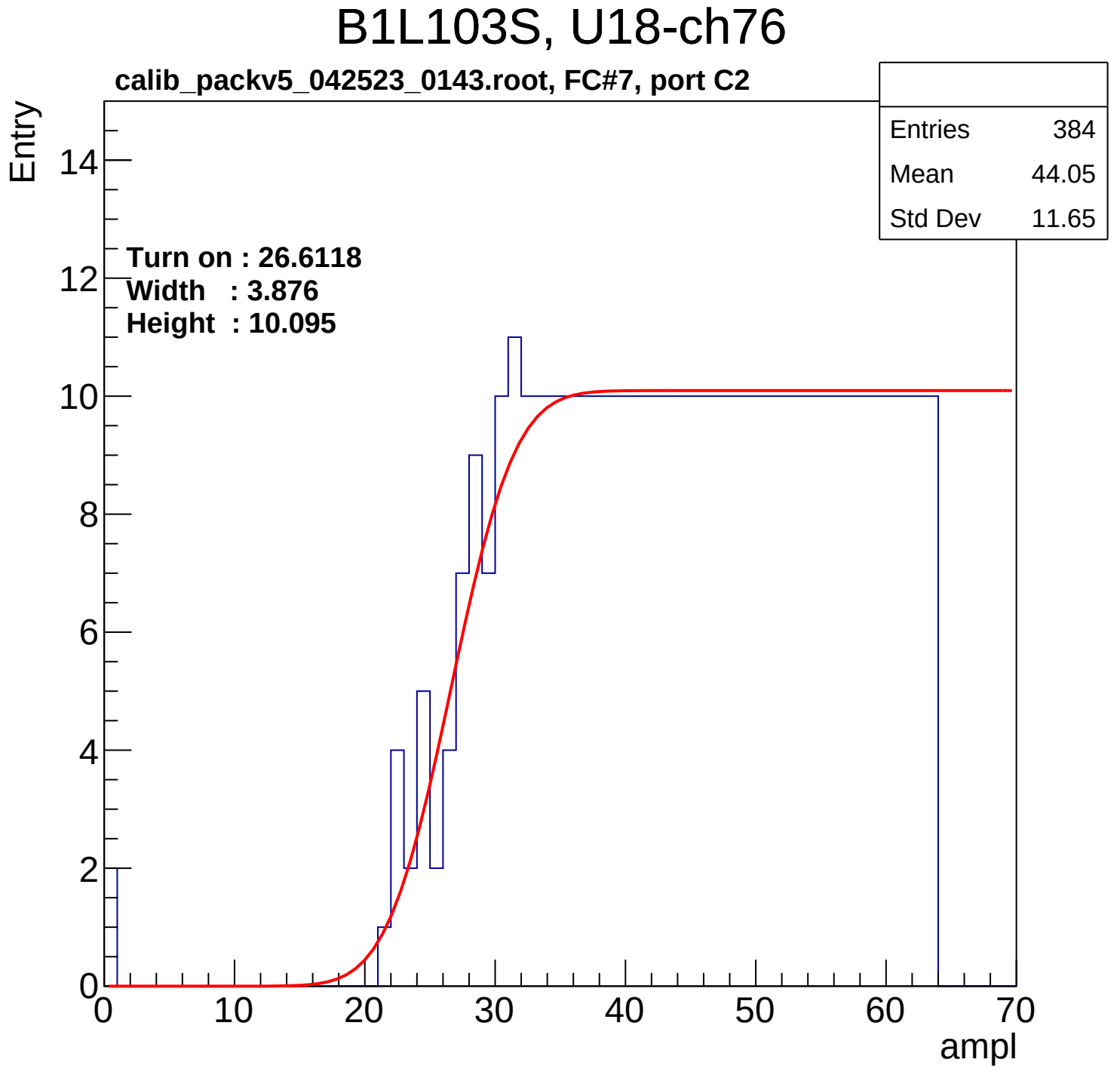
B1L103S, U18-ch76
calib_packv5_042523_0143.root, FC#7, port C2
Entries 384
Mean 44.05
Std Dev 11.65
Turn on : 26.6118
Width : 3.876
Height : 10.095
Entry
ampl
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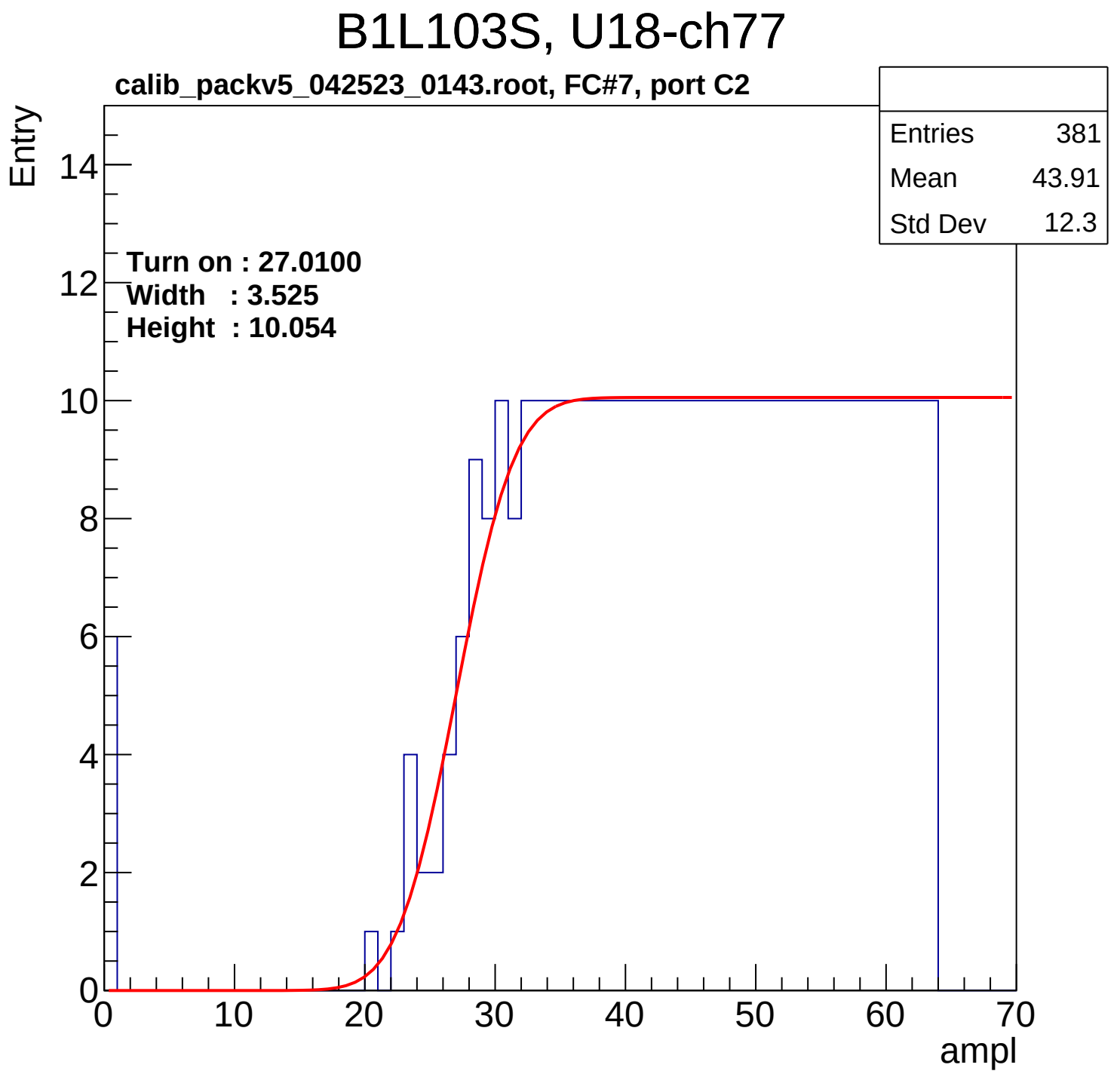
B1L103S, U18-ch77
calib_packv5_042523_0143.root, FC#7, port C2
Entries 381
Mean 43.91
Std Dev 12.3
Turn on : 27.0100
Width : 3.525
Height : 10.054
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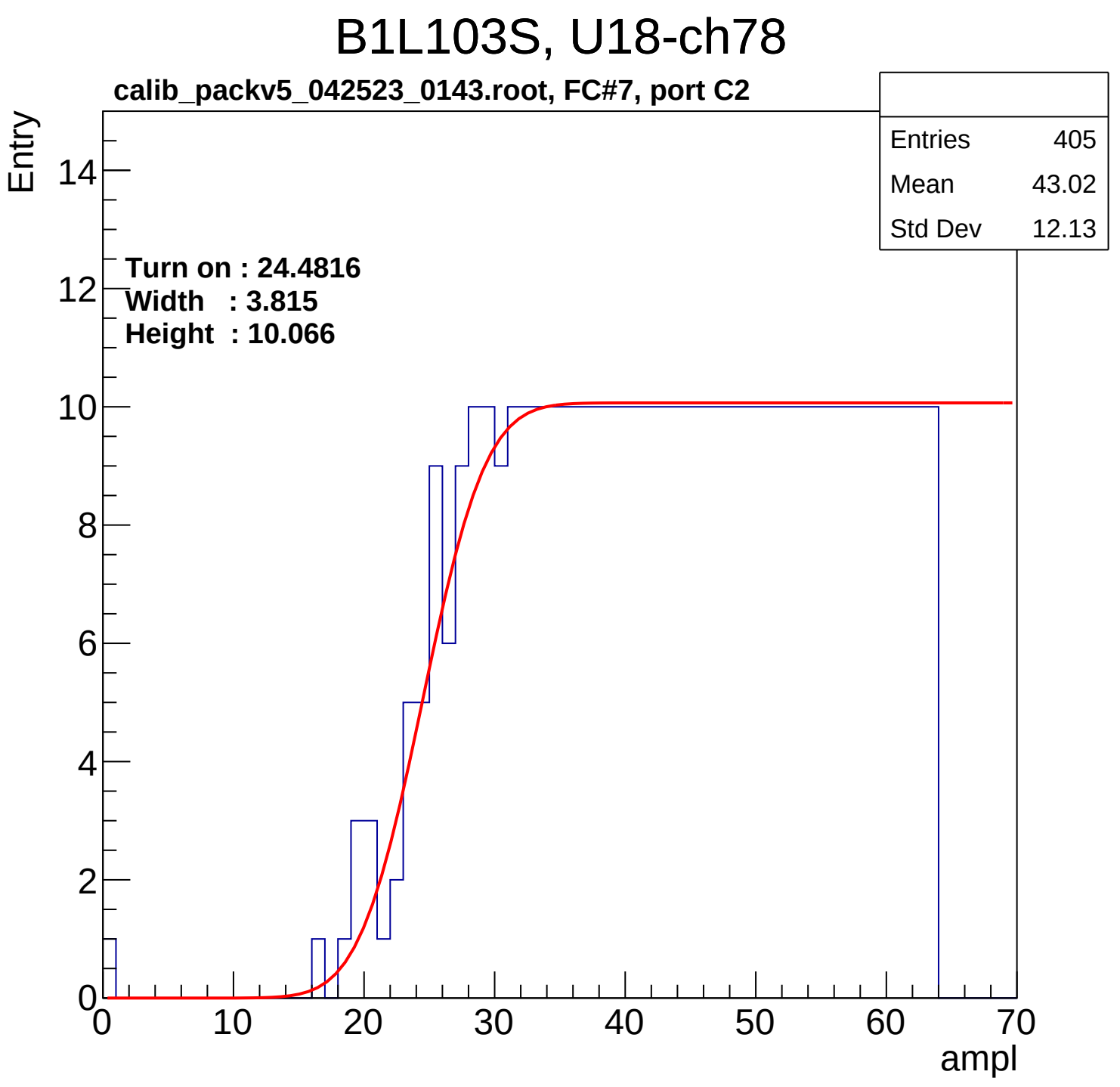
B1L103S, U18-ch78
calib_packv5_042523_0143.root, FC#7, port C2
Entries 405
Mean 43.02
Std Dev 12.13
Turn on : 24.4816
Width : 3.815
Height : 10.066
Entry
ampl
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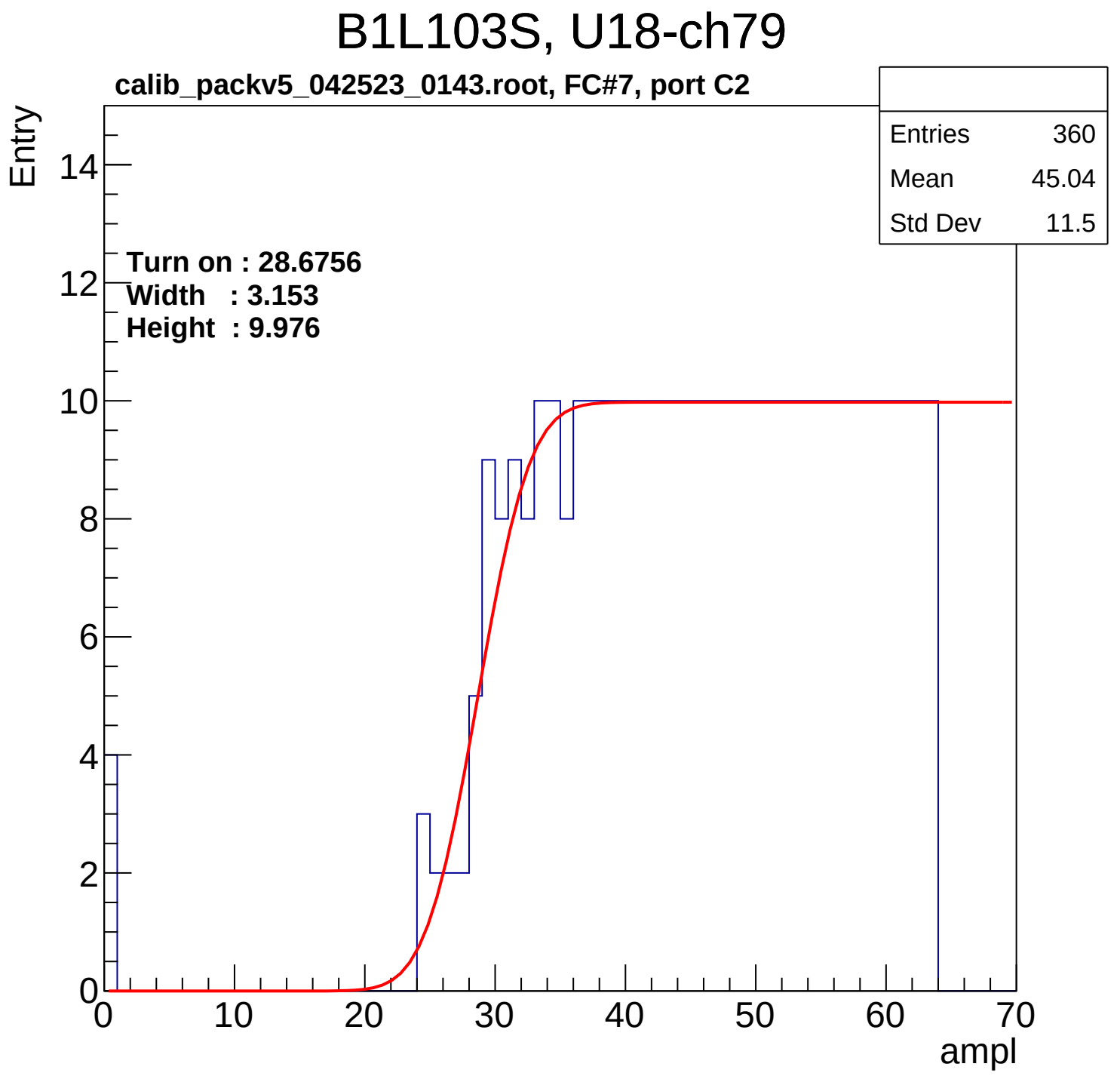
B1L103S, U18-ch79
calib_packv5_042523_0143.root, FC#7, port C2
Entries 360
Mean 45.04
Std Dev 11.5
Turn on : 28.6756
Width : 3.153
Height : 9.976
Entry
ampl
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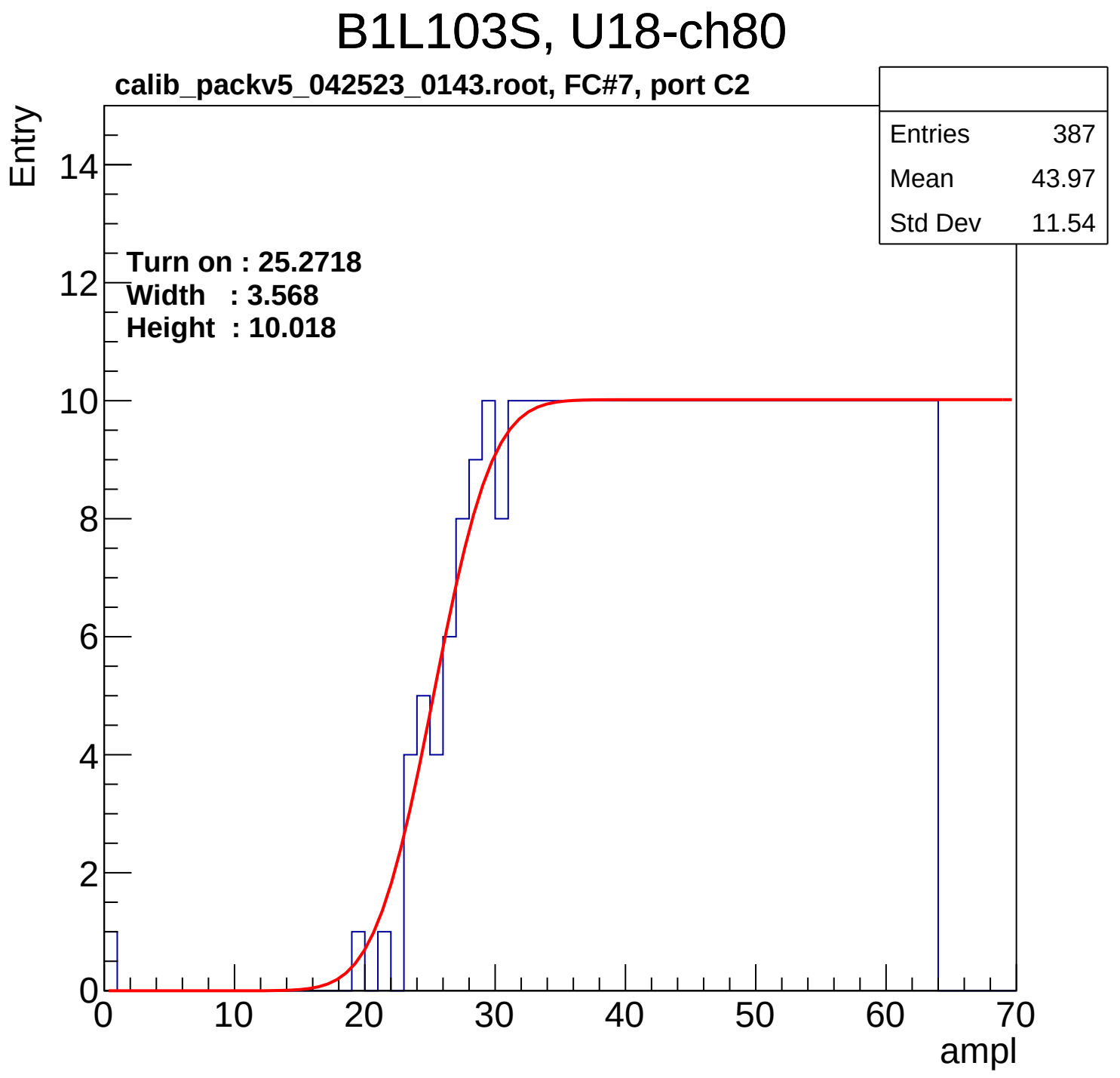
B1L103S, U18-ch80
calib_packv5_042523_0143.root, FC#7, port C2
Entries 387
Mean 43.97
Std Dev 11.54
Turn on : 25.2718
Width : 3.568
Height : 10.018
Entry
ampl
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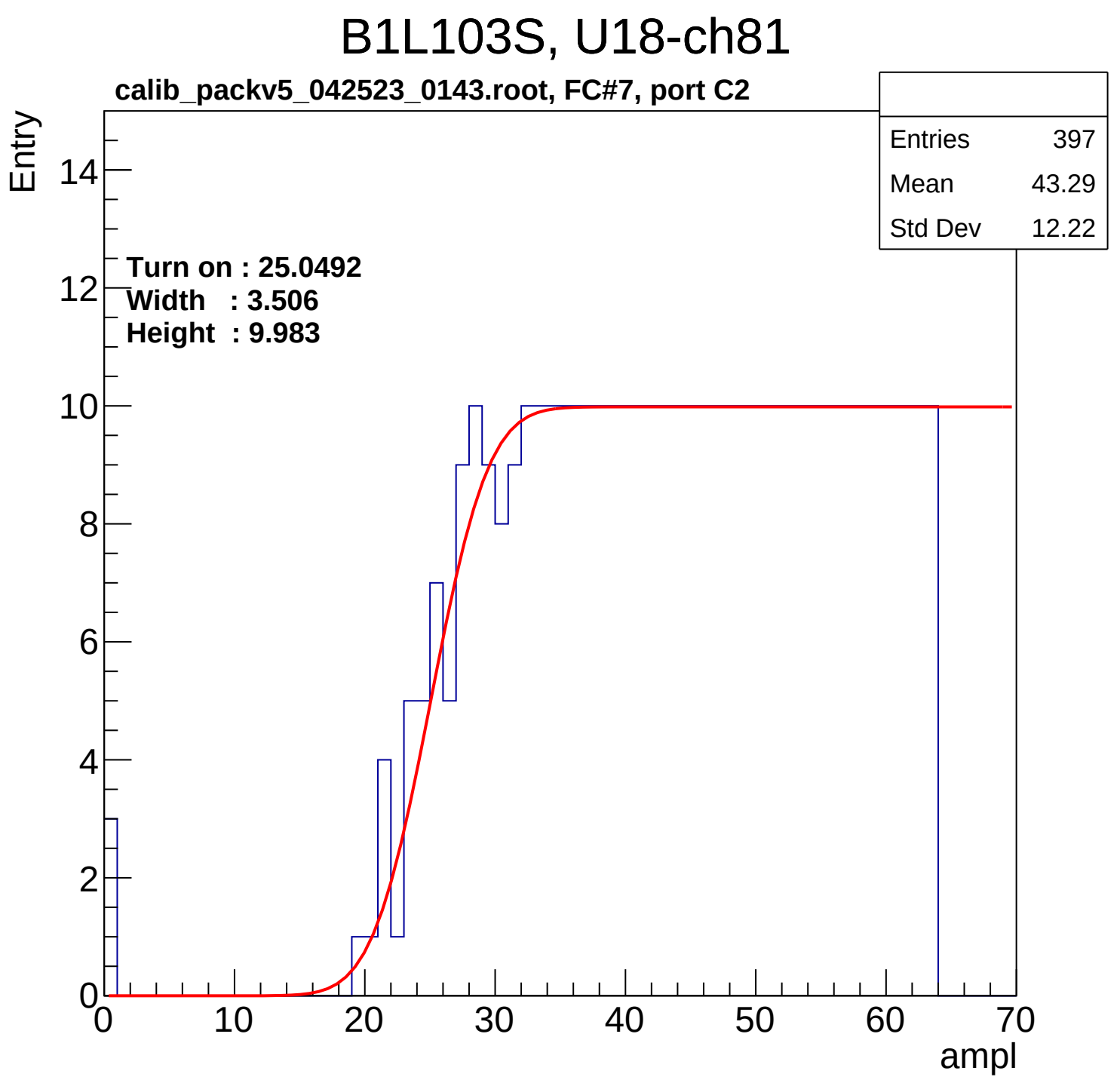
B1L103S, U18-ch81
calib_packv5_042523_0143.root, FC#7, port C2
Entries 397
Mean 43.29
Std Dev 12.22
Turn on : 25.0492
Width : 3.506
Height : 9.983
Entry
ampl
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6
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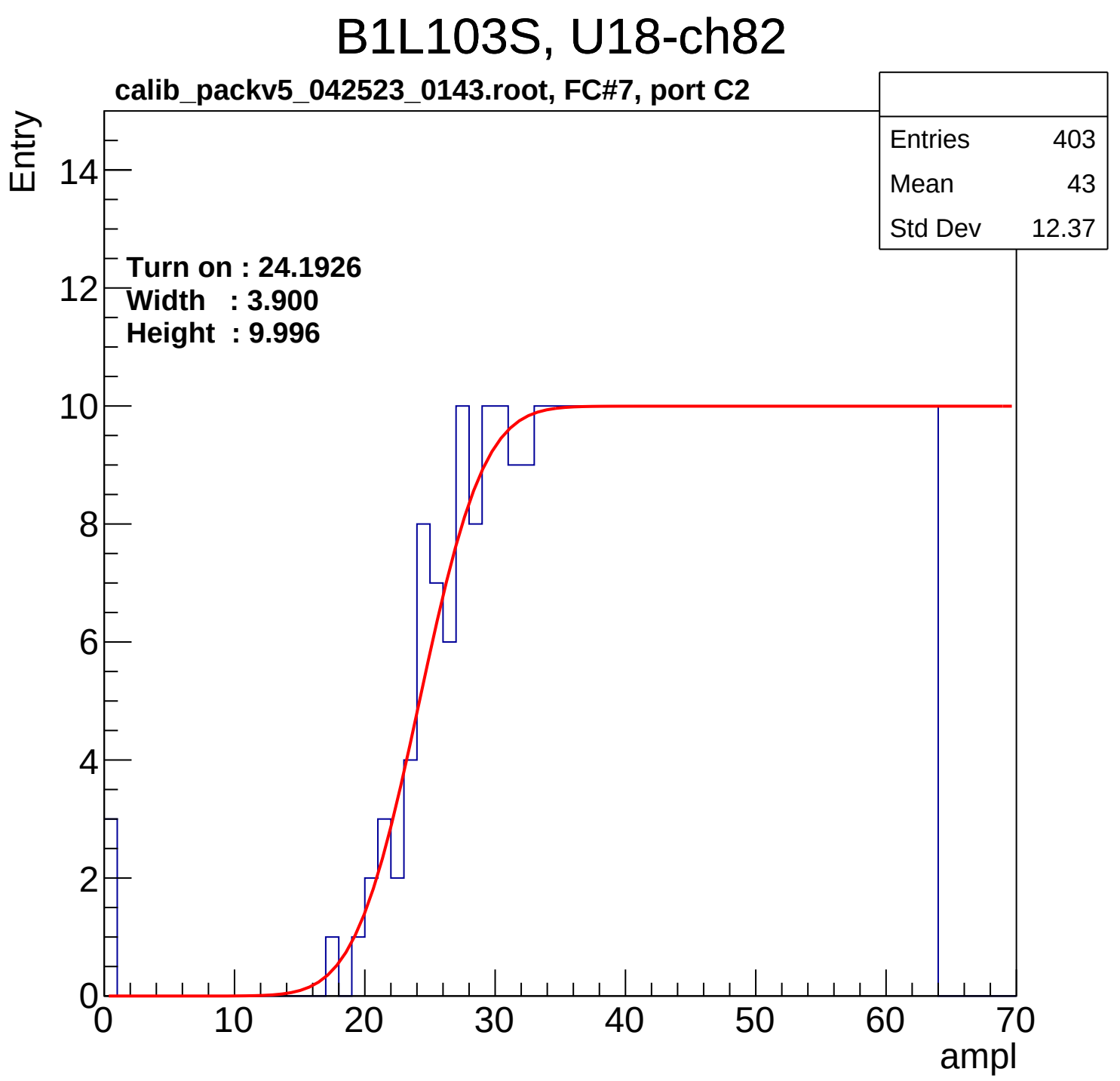
B1L103S, U18-ch82
calib_packv5_042523_0143.root, FC#7, port C2
Entries 403
Mean 43
Std Dev 12.37
Turn on : 24.1926
Width : 3.900
Height : 9.996
Entry
ampl
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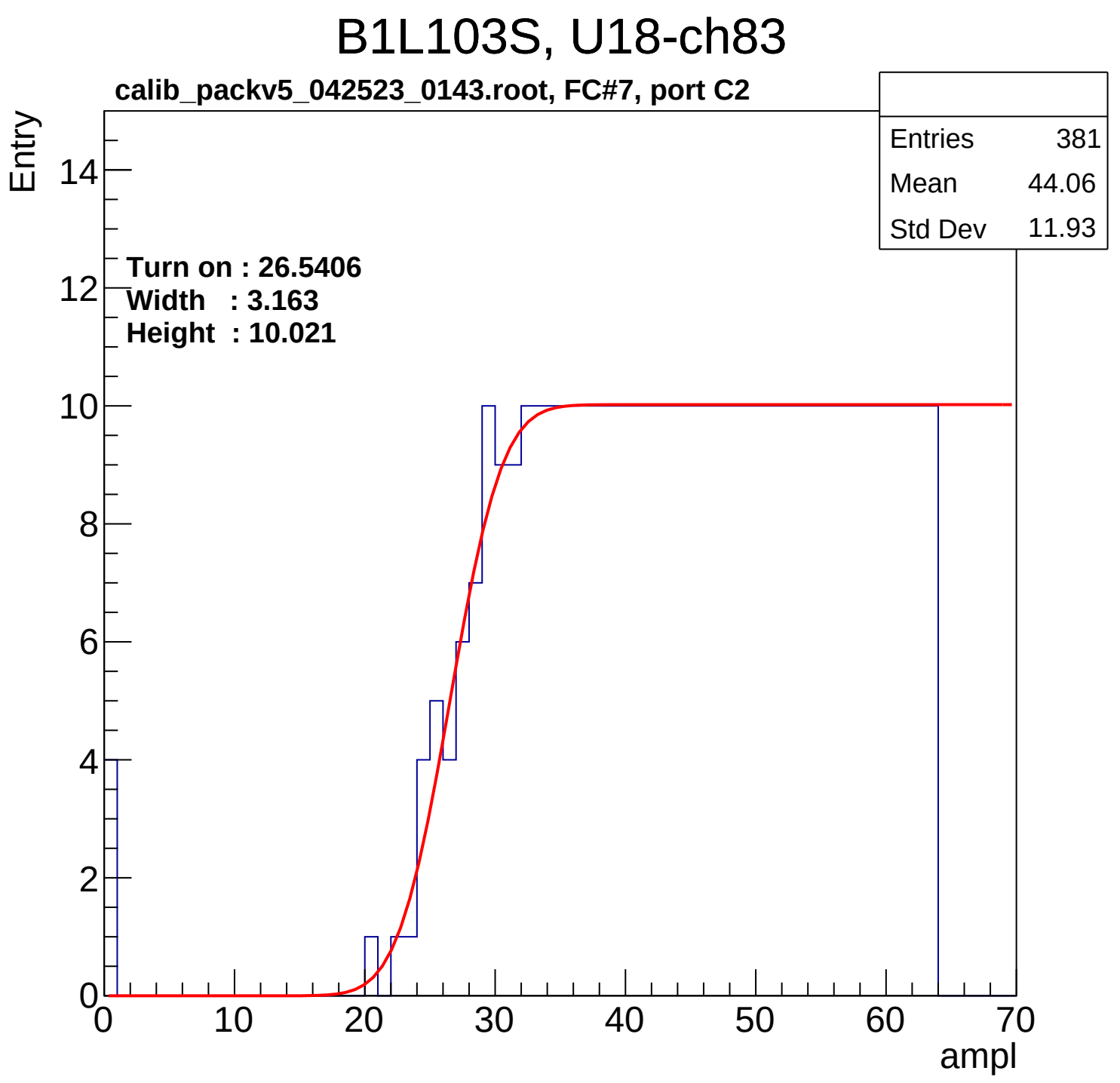
B1L103S, U18-ch83
calib_packv5_042523_0143.root, FC#7, port C2
Entries 381
Mean 44.06
Std Dev 11.93
Turn on : 26.5406
Width : 3.163
Height : 10.021
Entry
ampl
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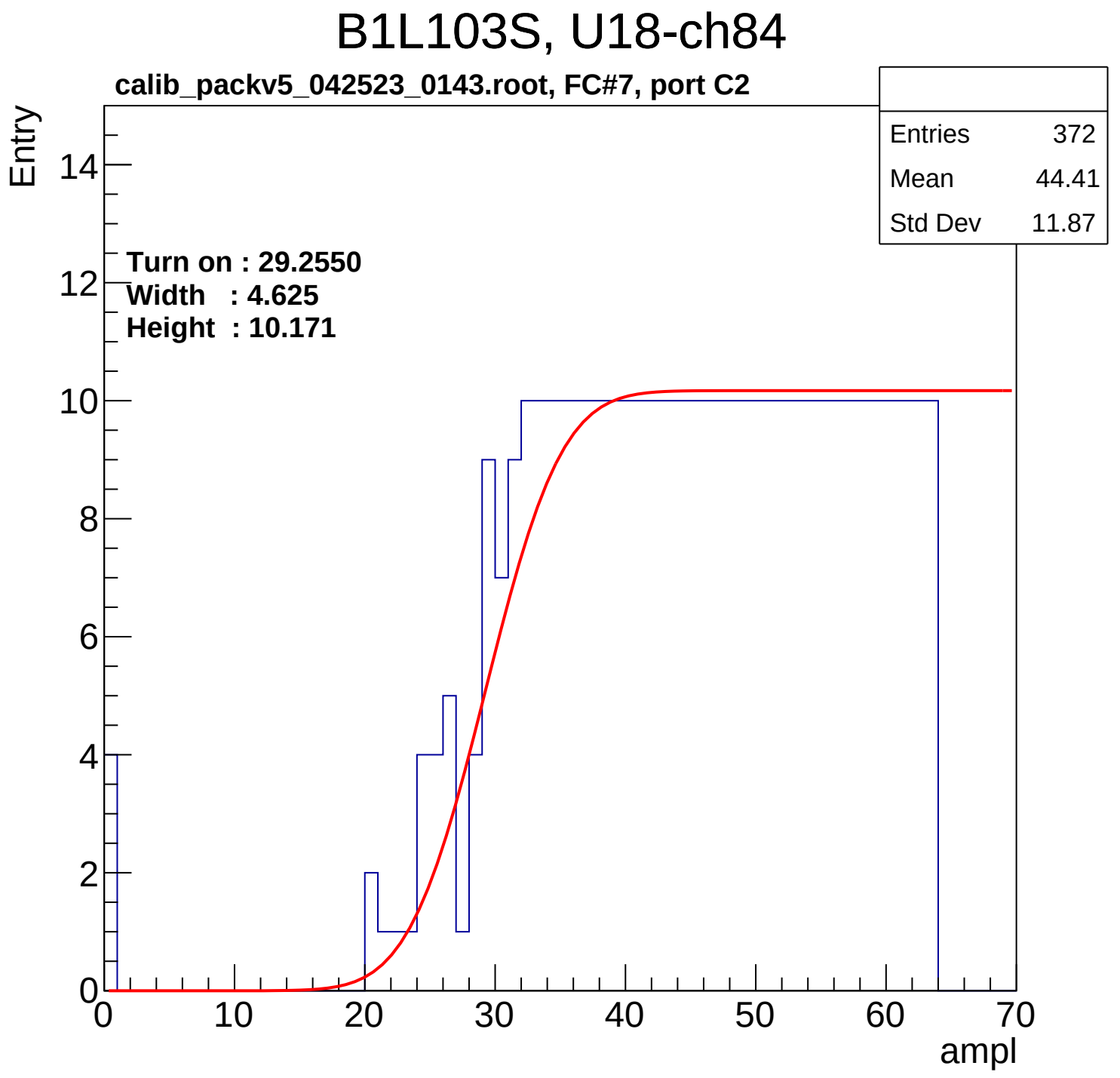
B1L103S, U18-ch84
calib_packv5_042523_0143.root, FC#7, port C2
Entries 372
Mean 44.41
Std Dev 11.87
Turn on : 29.2550
Width : 4.625
Height : 10.171
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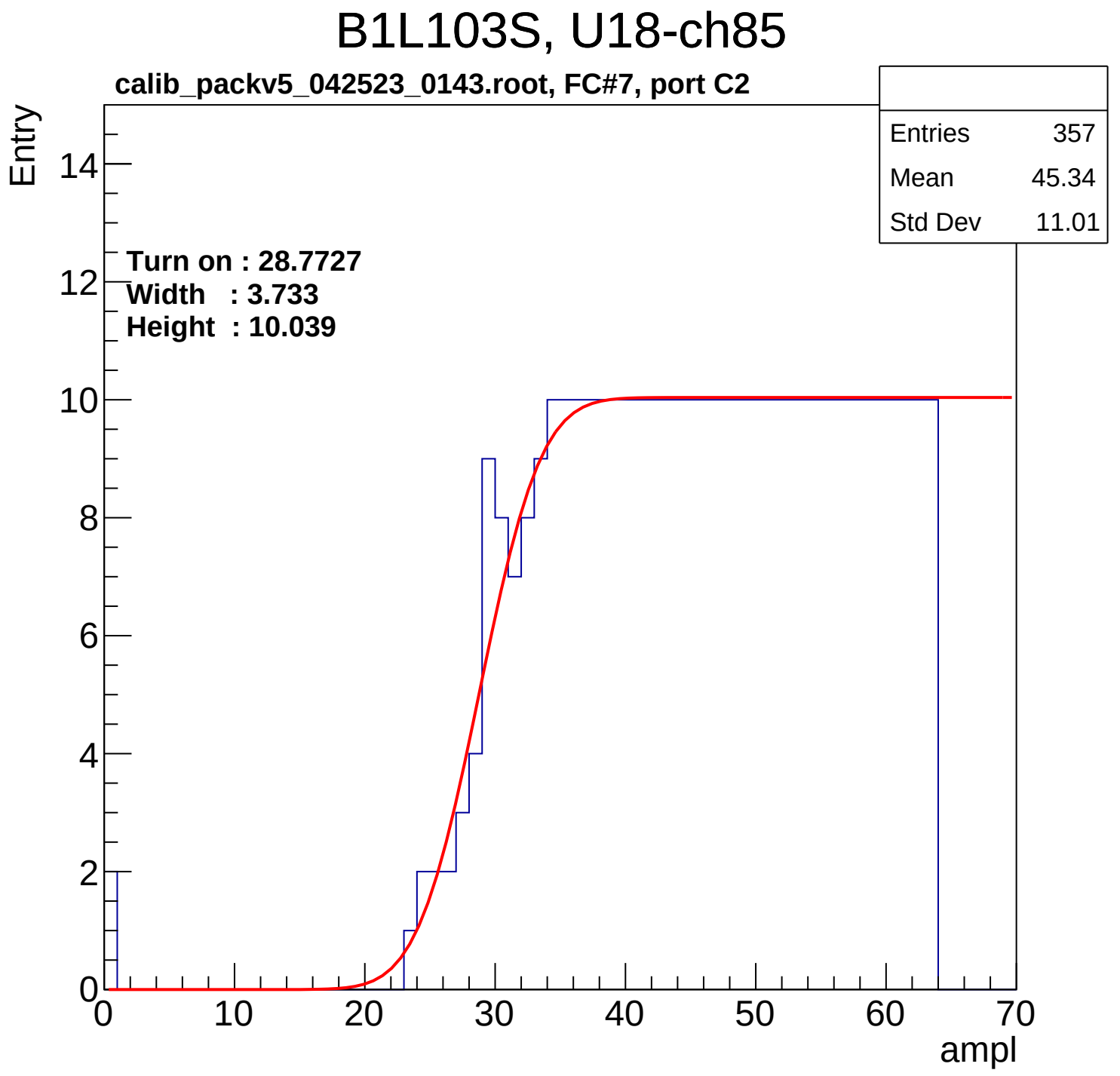
B1L103S, U18-ch85
calib_packv5_042523_0143.root, FC#7, port C2
Entries 357
Mean 45.34
Std Dev 11.01
Turn on : 28.7727
Width : 3.733
Height : 10.039
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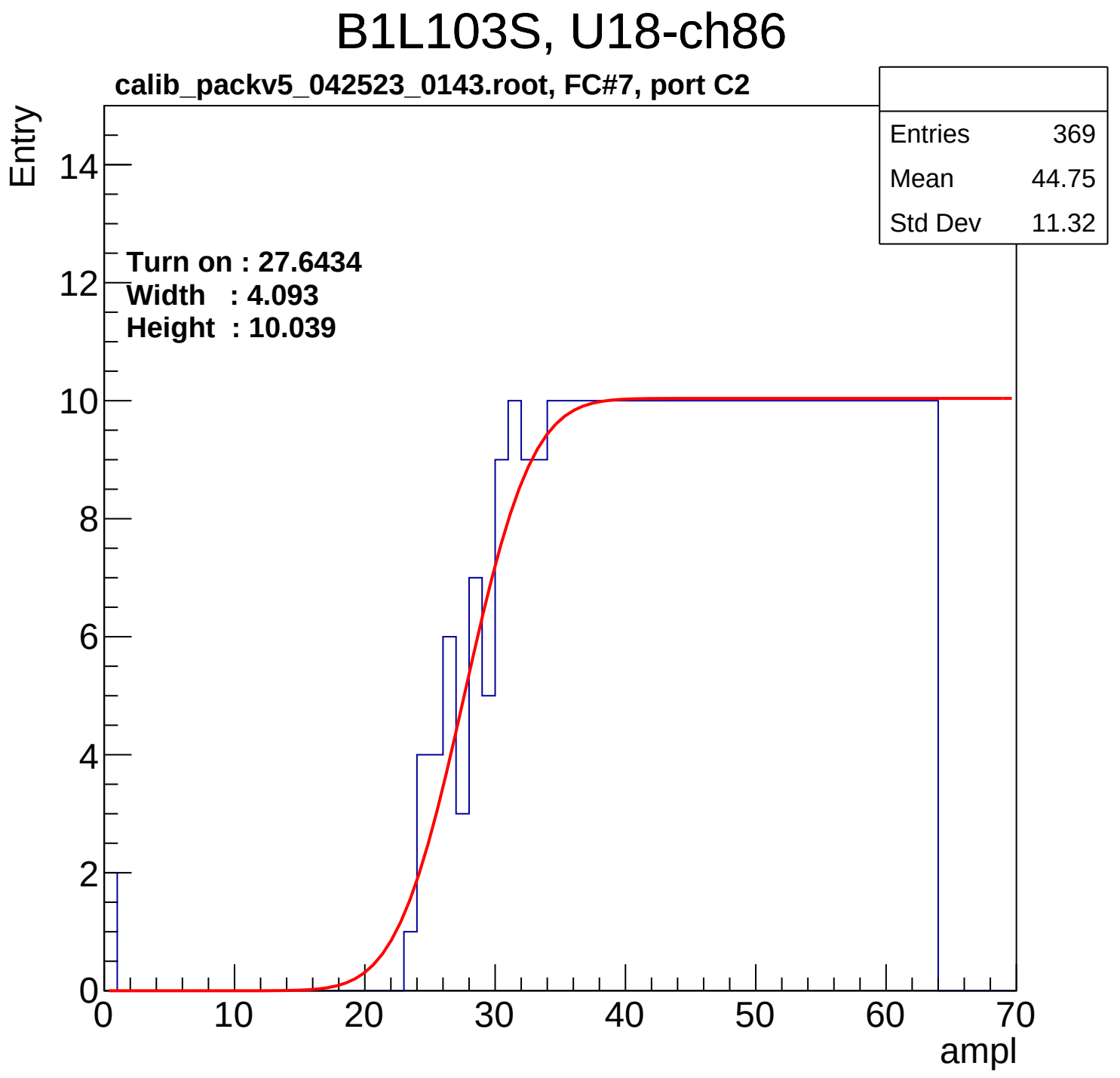
B1L103S, U18-ch86
calib_packv5_042523_0143.root, FC#7, port C2
Entries 369
Mean 44.75
Std Dev 11.32
Turn on : 27.6434
Width : 4.093
Height : 10.039
Entry
ampl
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20
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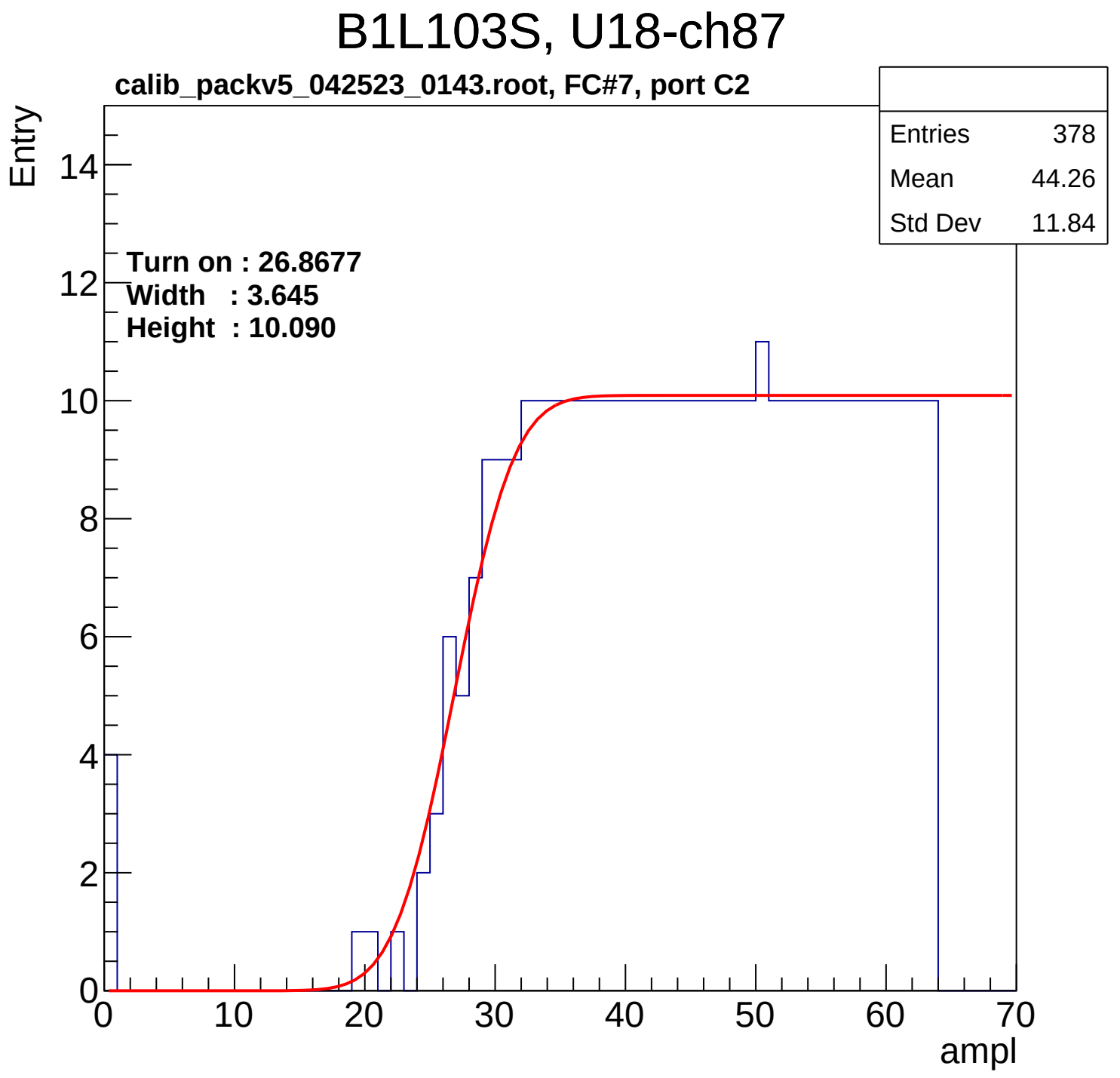
B1L103S, U18-ch87
calib_packv5_042523_0143.root, FC#7, port C2
Entries 378
Mean 44.26
Std Dev 11.84
Turn on : 26.8677
Width : 3.645
Height : 10.090
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ampl
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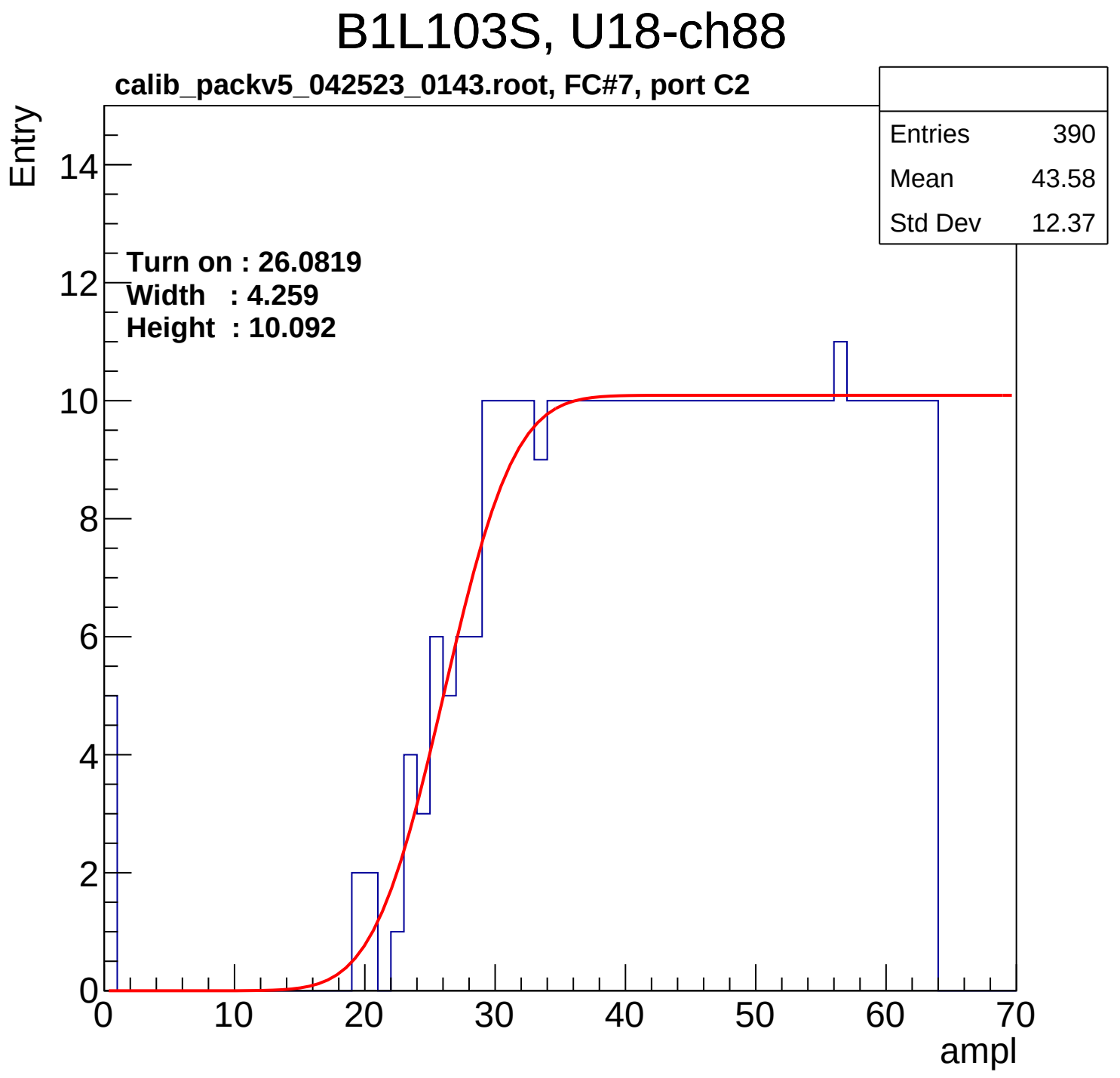
B1L103S, U18-ch88
calib_packv5_042523_0143.root, FC#7, port C2
Entries 390
Mean 43.58
Std Dev 12.37
Turn on : 26.0819
Width : 4.259
Height : 10.092
Entry
ampl
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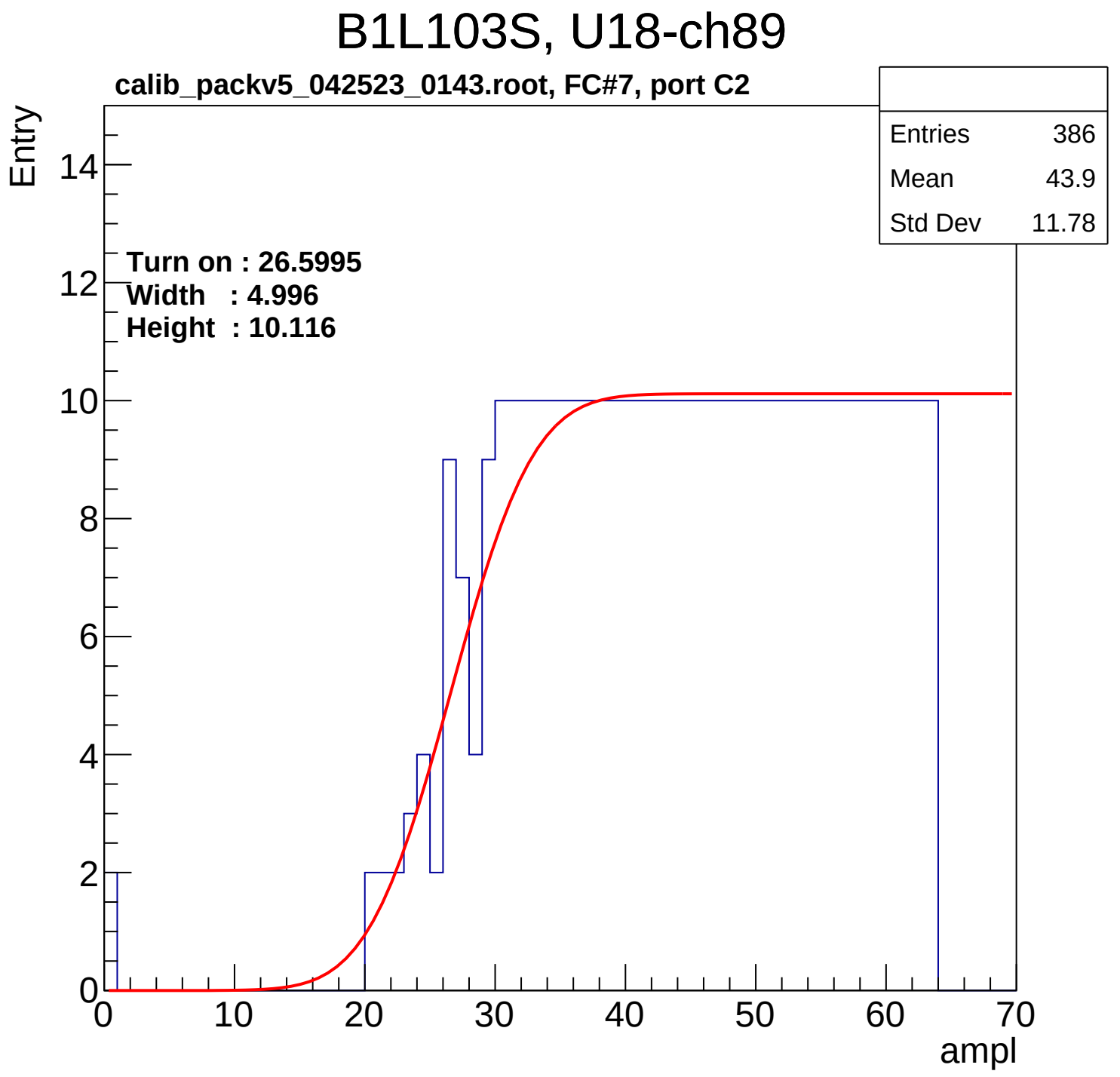
B1L103S, U18-ch89
calib_packv5_042523_0143.root, FC#7, port C2
Entries 386
Mean 43.9
Std Dev 11.78
Turn on : 26.5995
Width : 4.996
Height : 10.116
Entry
ampl
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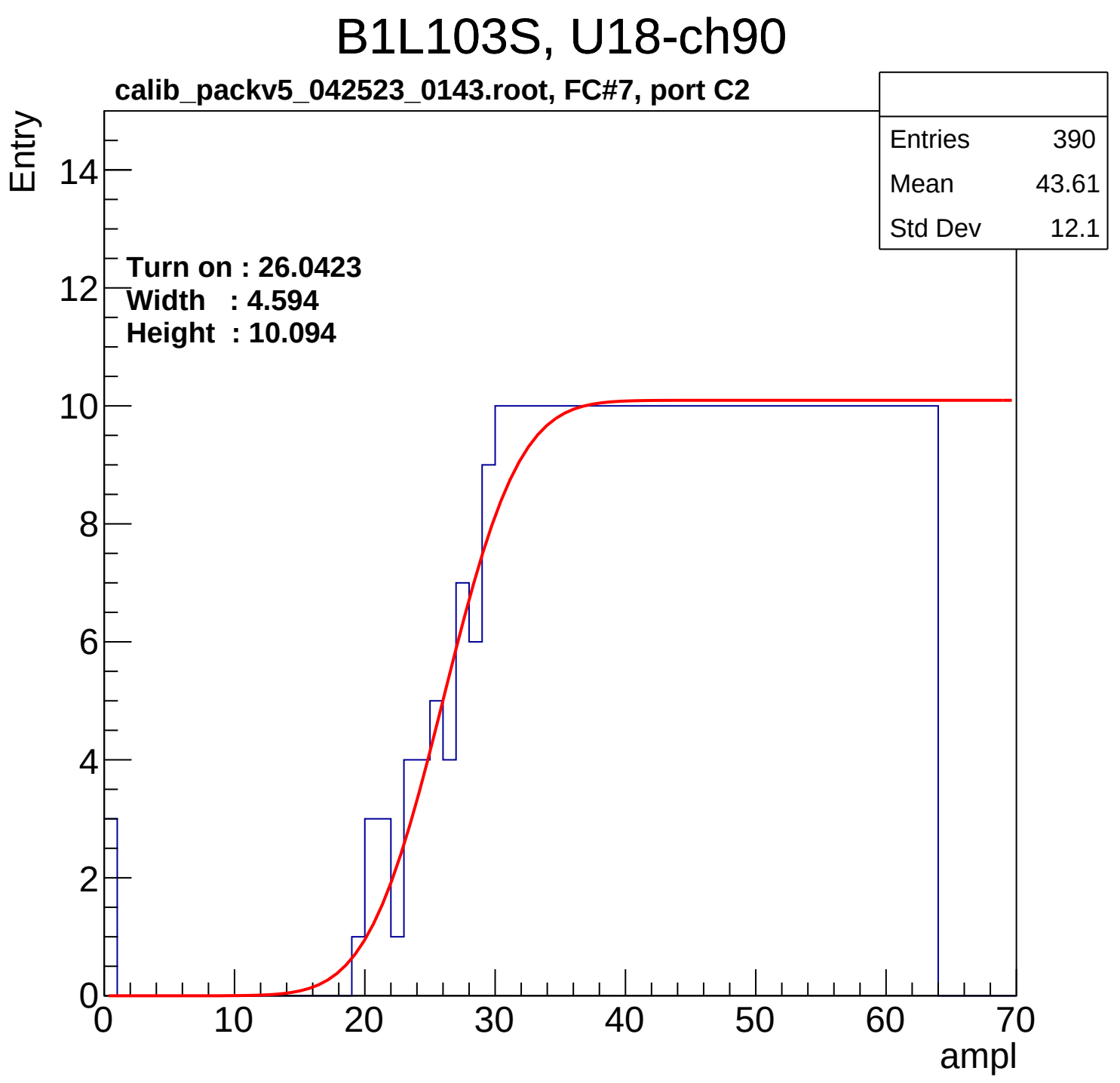
B1L103S, U18-ch90
calib_packv5_042523_0143.root, FC#7, port C2
Entries 390
Mean 43.61
Std Dev 12.1
Turn on : 26.0423
Width : 4.594
Height : 10.094
Entry
ampl
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8
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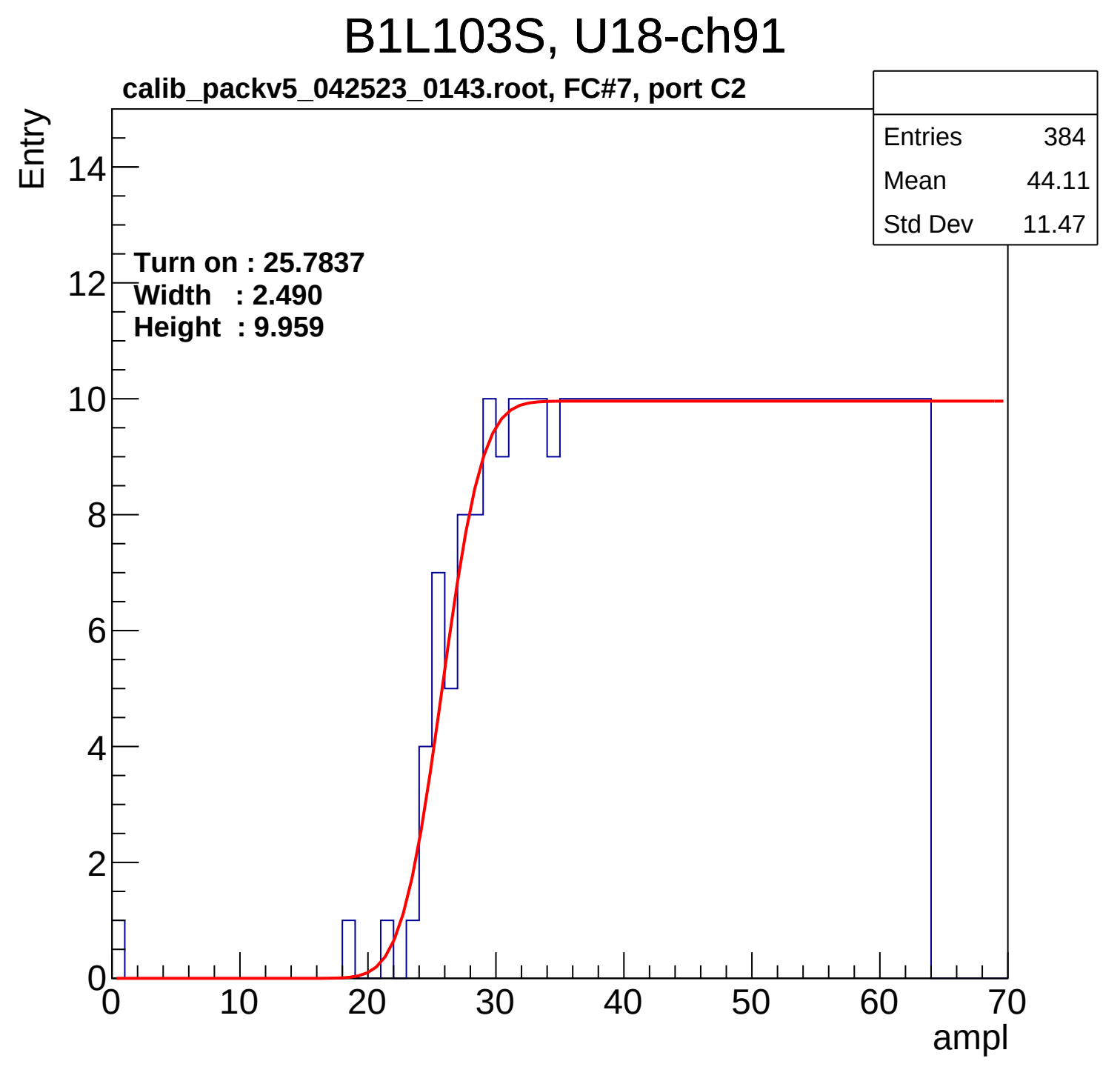
B1L103S, U18-ch91
calib_packv5_042523_0143.root, FC#7, port C2
Entries 384
Mean 44.11
Std Dev 11.47
Turn on : 25.7837
Width : 2.490
Height : 9.959
Entry
ampl
0
2
4
6
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10
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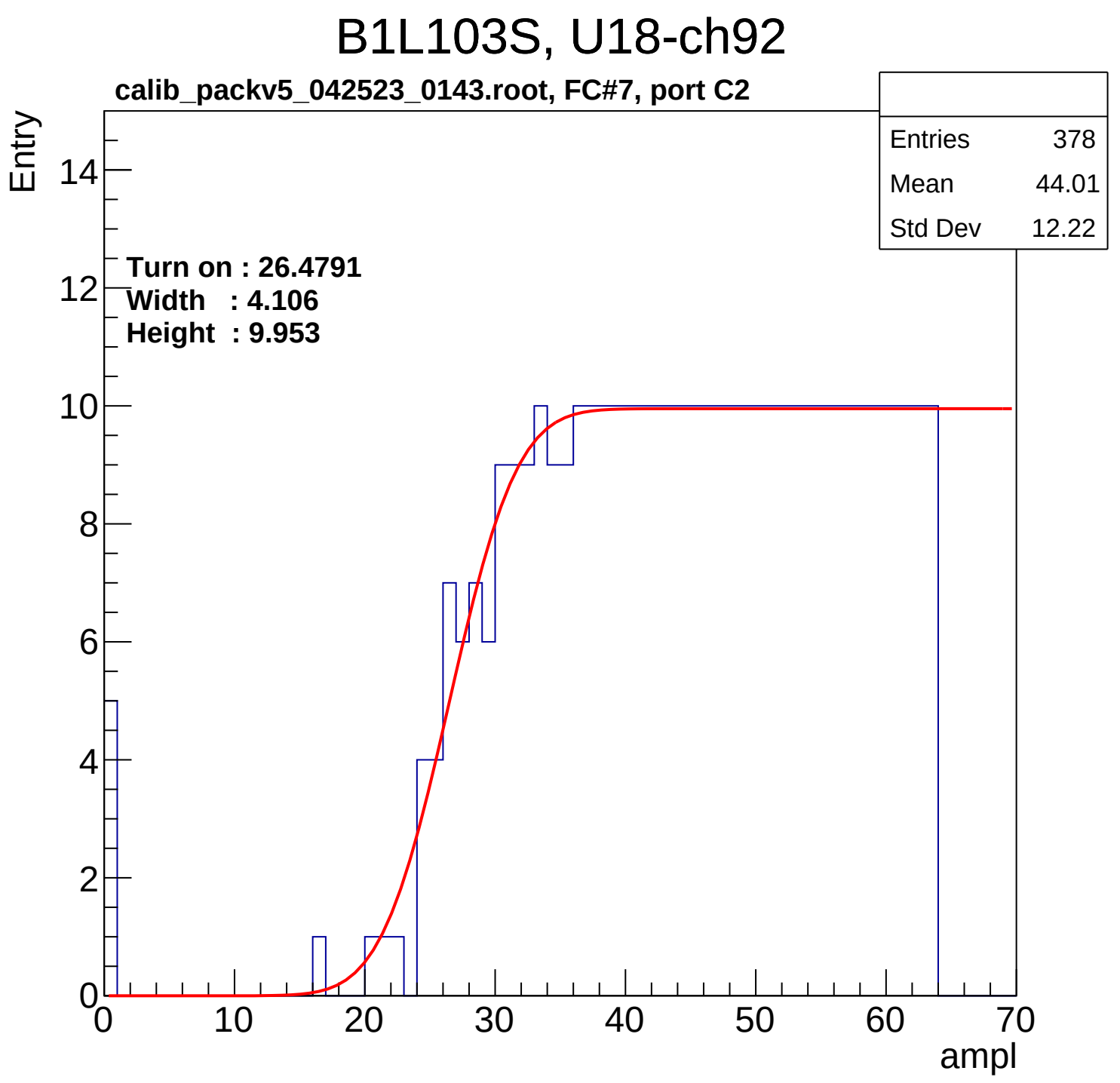
B1L103S, U18-ch92
calib_packv5_042523_0143.root, FC#7, port C2
Entries 378
Mean 44.01
Std Dev 12.22
Turn on : 26.4791
Width : 4.106
Height : 9.953
Entry
ampl
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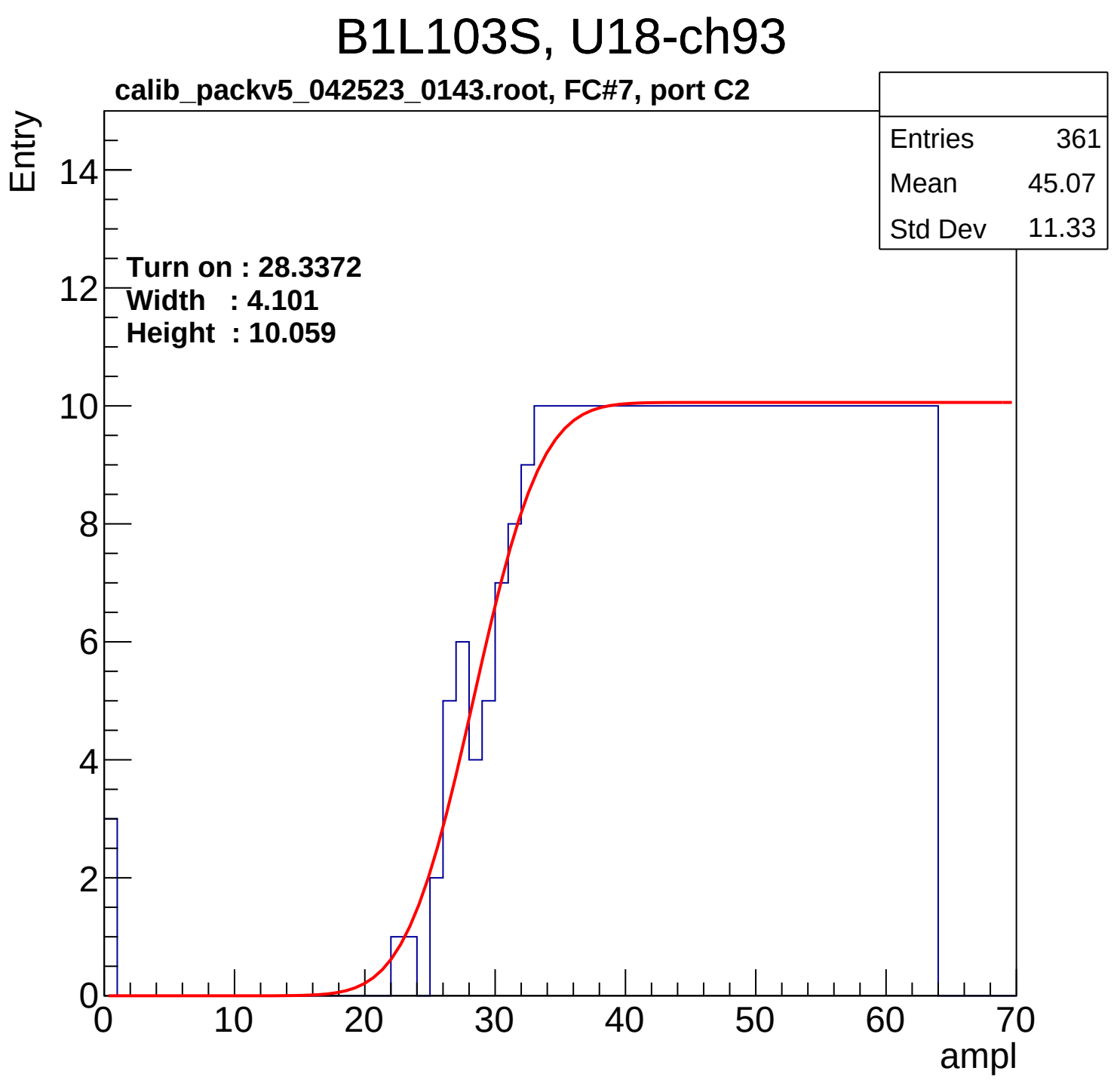
B1L103S, U18-ch93
calib_packv5_042523_0143.root, FC#7, port C2
Entries 361
Mean 45.07
Std Dev 11.33
Turn on : 28.3372
Width : 4.101
Height : 10.059
Entry
ampl
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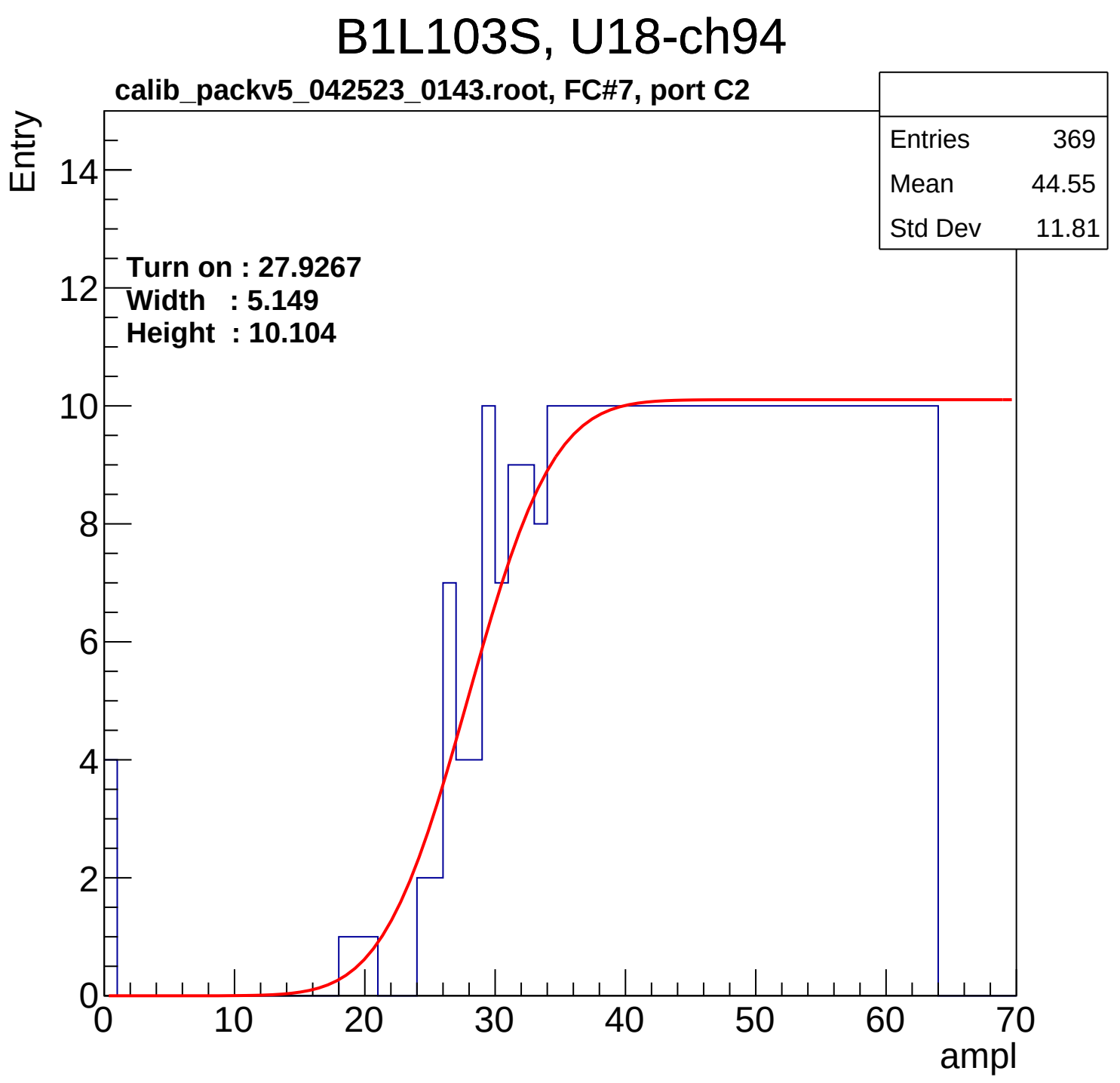
B1L103S, U18-ch94
calib_packv5_042523_0143.root, FC#7, port C2
Entries 369
Mean 44.55
Std Dev 11.81
Turn on : 27.9267
Width : 5.149
Height : 10.104
Entry
ampl
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2
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6
8
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0
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60
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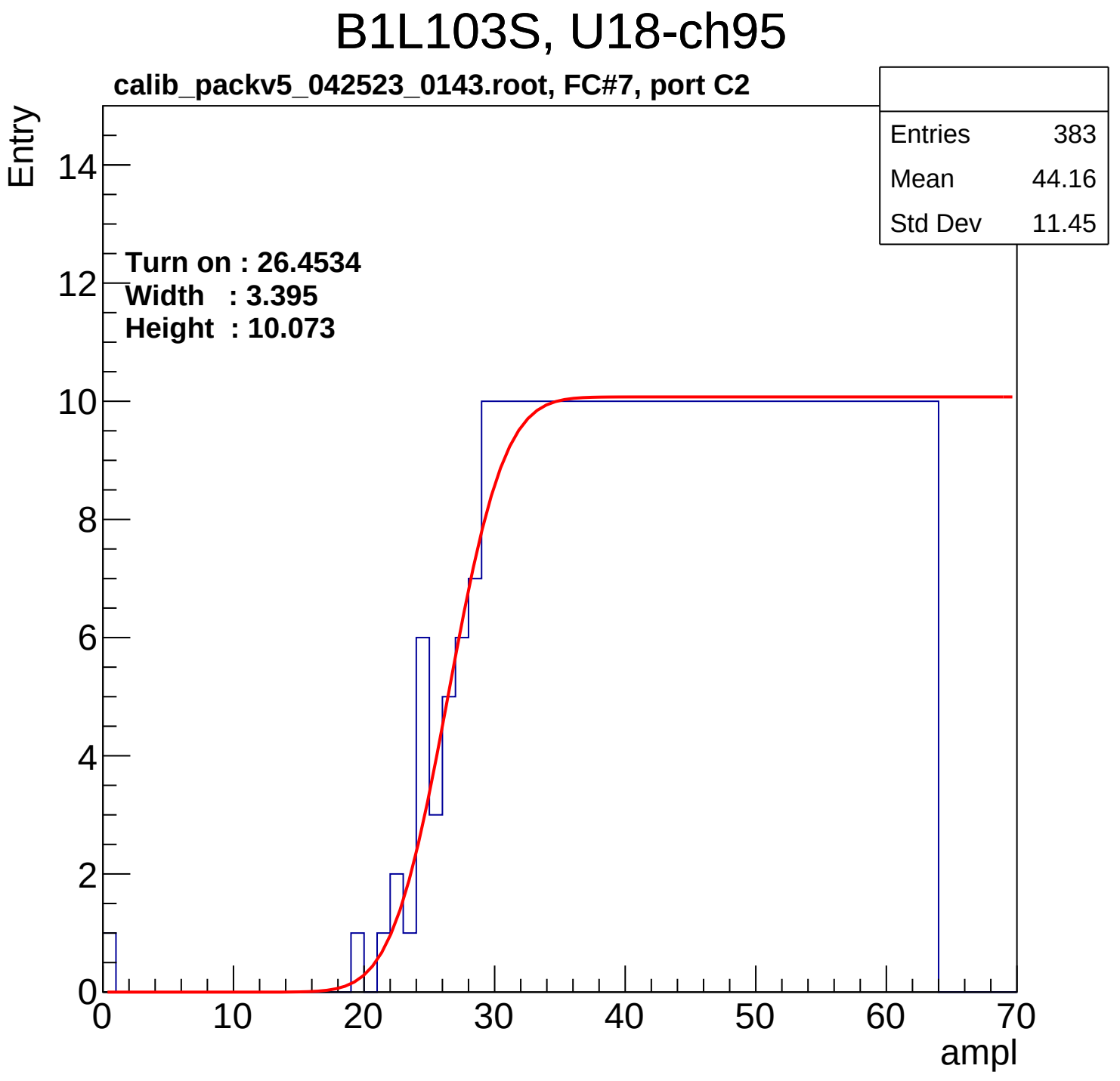
B1L103S, U18-ch95
calib_packv5_042523_0143.root, FC#7, port C2
Entries 383
Mean 44.16
Std Dev 11.45
Turn on : 26.4534
Width : 3.395
Height : 10.073
Entry
ampl
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2
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6
8
10
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0
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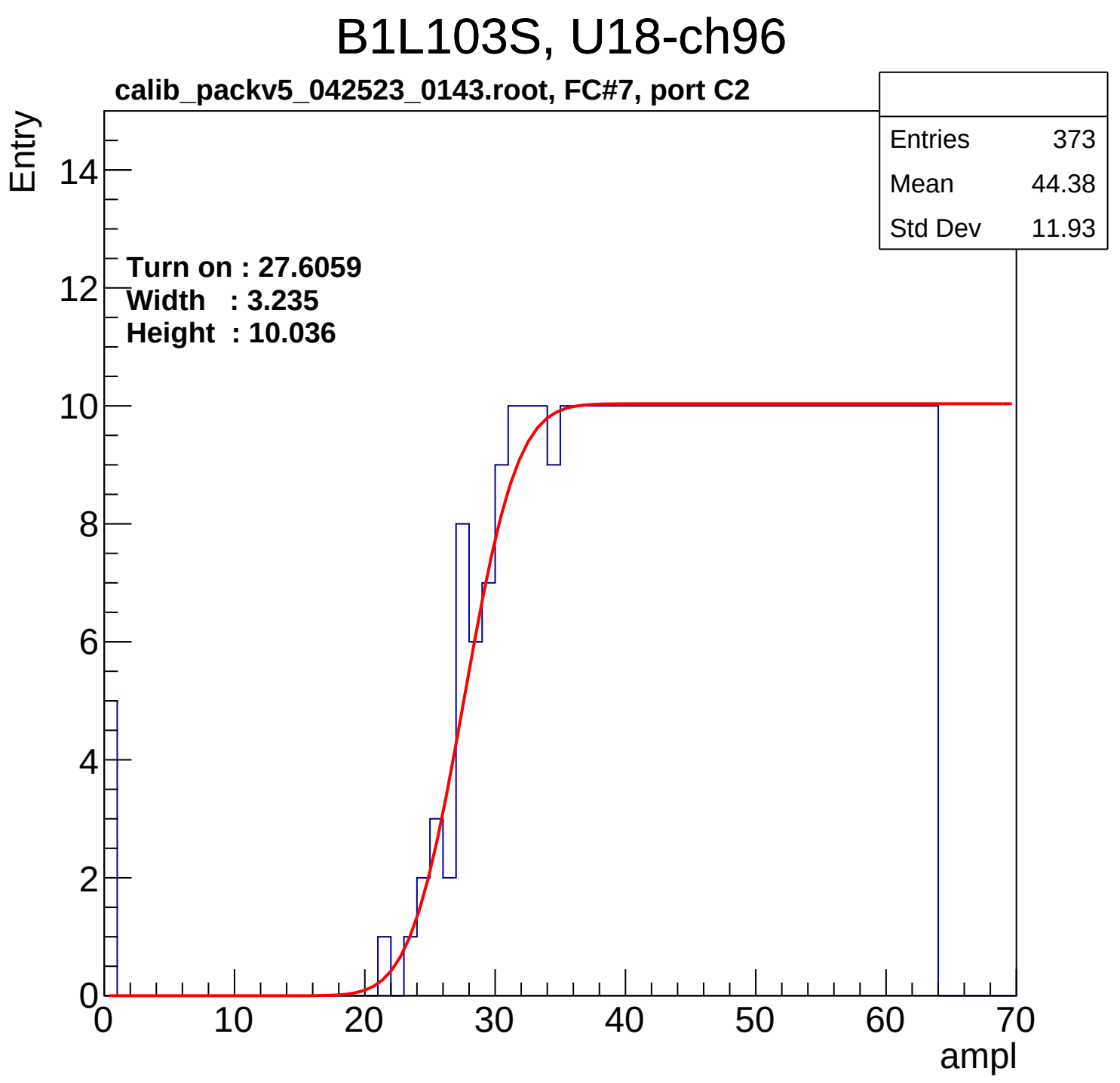
B1L103S, U18-ch96
calib_packv5_042523_0143.root, FC#7, port C2
Entries 373
Mean 44.38
Std Dev 11.93
Turn on : 27.6059
Width : 3.235
Height : 10.036
Entry
ampl
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8
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12
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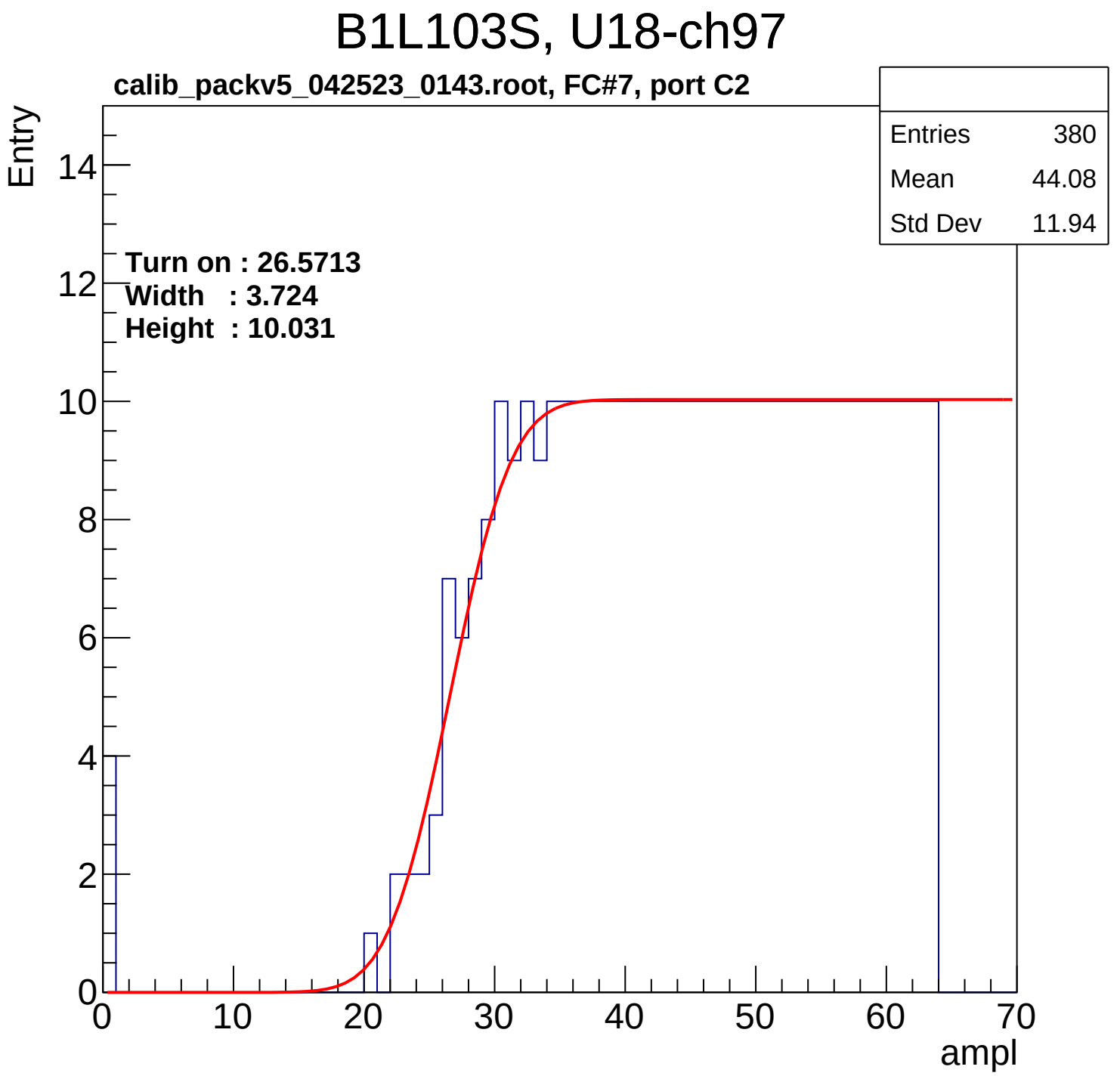
B1L103S, U18-ch97
calib_packv5_042523_0143.root, FC#7, port C2
Entries 380
Mean 44.08
Std Dev 11.94
Turn on : 26.5713
Width : 3.724
Height : 10.031
Entry
ampl
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6
8
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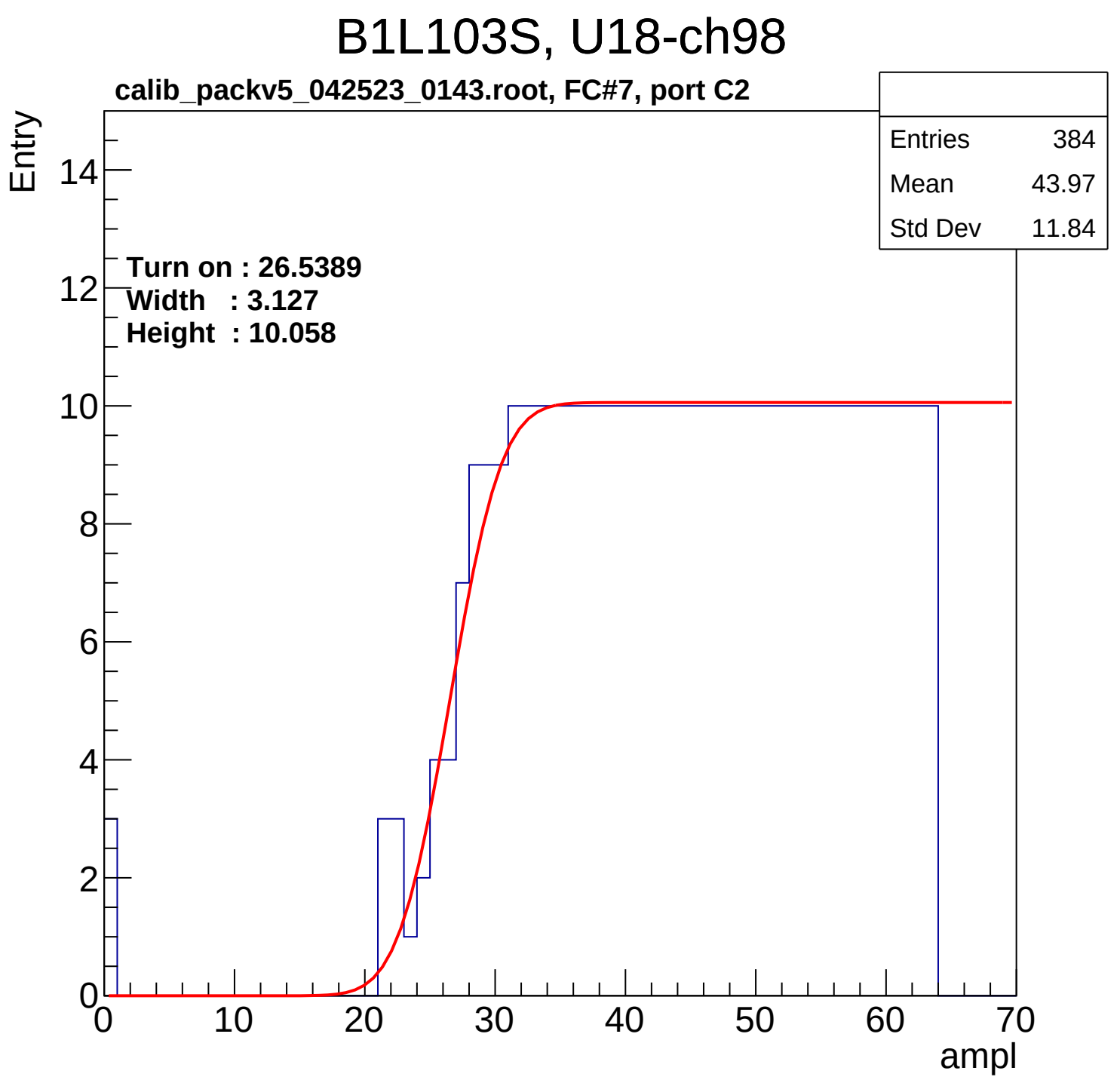
B1L103S, U18-ch98
calib_packv5_042523_0143.root, FC#7, port C2
Entries 384
Mean 43.97
Std Dev 11.84
Turn on : 26.5389
Width : 3.127
Height : 10.058
Entry
ampl
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10
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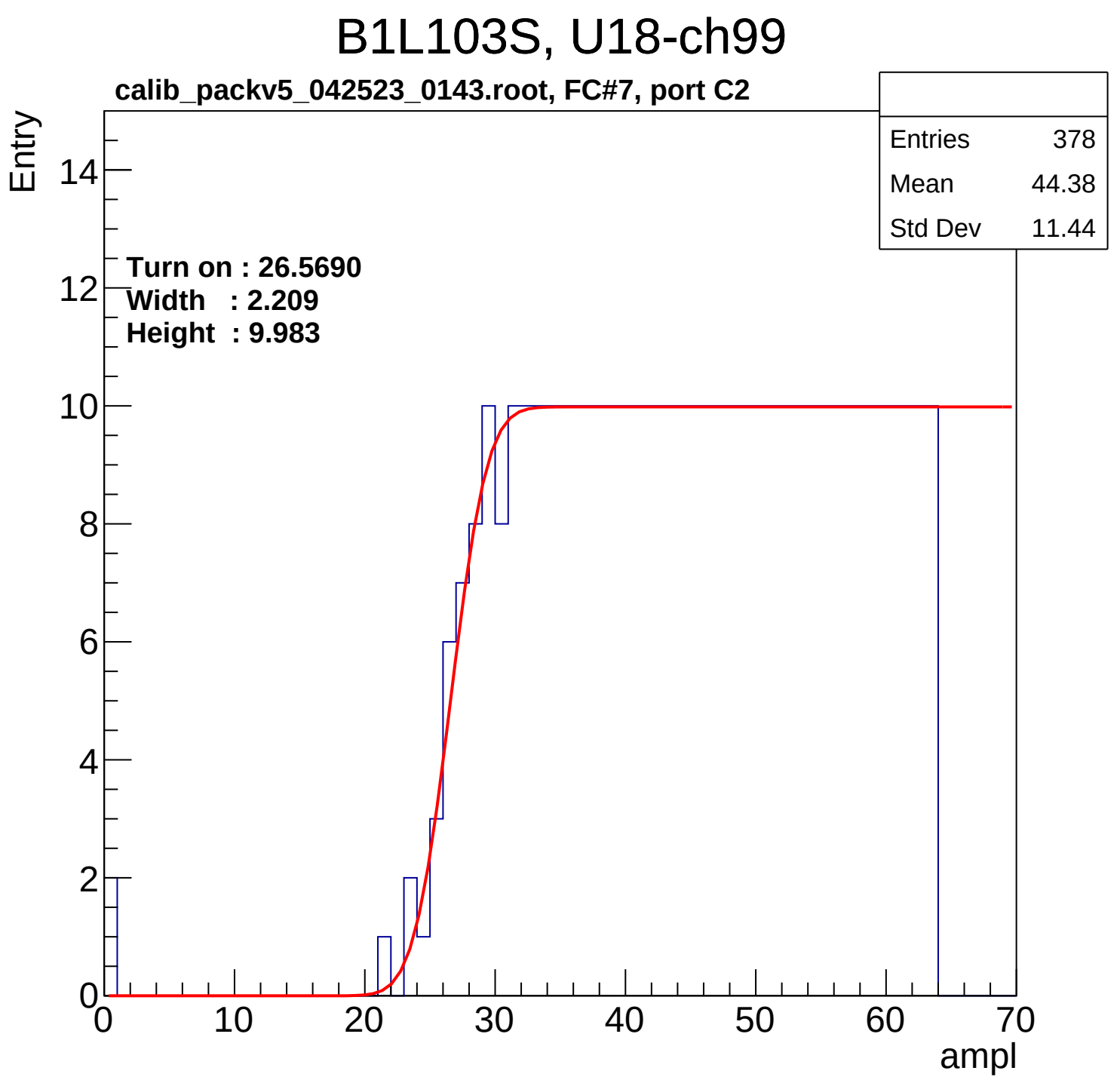
B1L103S, U18-ch99
calib_packv5_042523_0143.root, FC#7, port C2
Entries 378
Mean 44.38
Std Dev 11.44
Turn on : 26.5690
Width : 2.209
Height : 9.983
Entry
ampl
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2
4
6
8
10
12
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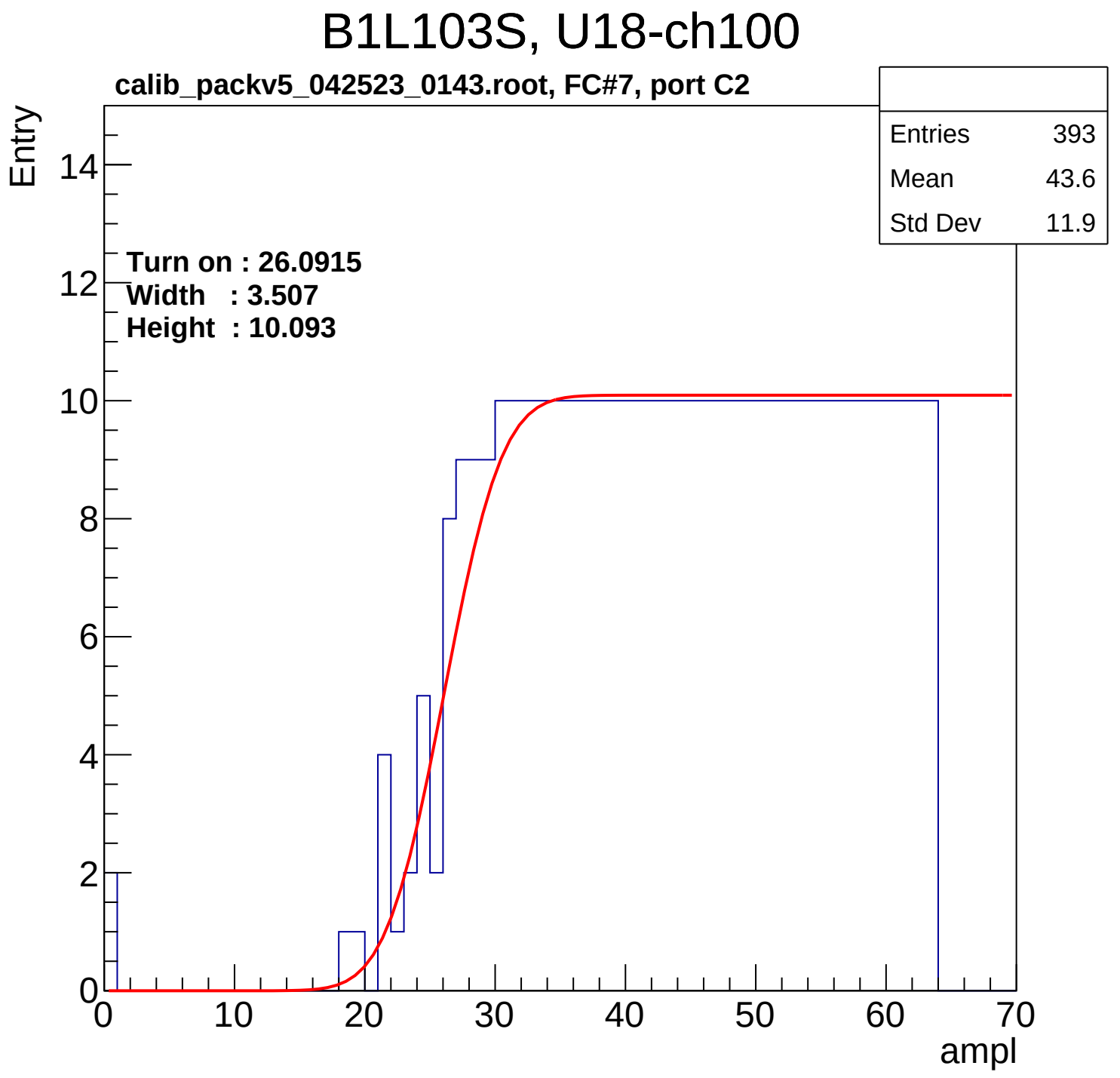
B1L103S, U18-ch100
calib_packv5_042523_0143.root, FC#7, port C2
Entries 393
Mean 43.6
Std Dev 11.9
Turn on : 26.0915
Width : 3.507
Height : 10.093
Entry
ampl
0
2
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6
8
10
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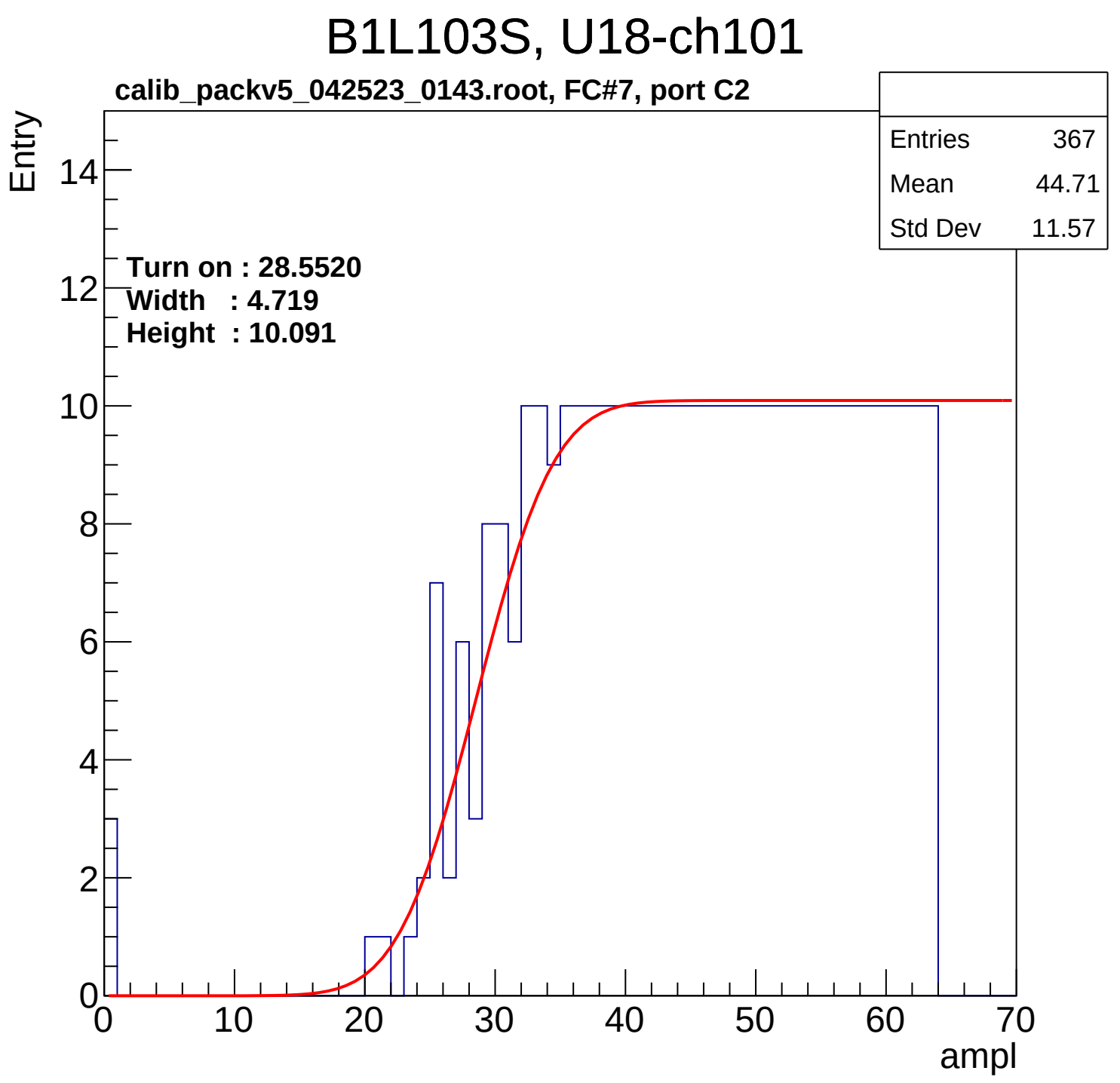
B1L103S, U18-ch101
calib_packv5_042523_0143.root, FC#7, port C2
Entries 367
Mean 44.71
Std Dev 11.57
Turn on : 28.5520
Width : 4.719
Height : 10.091
Entry
ampl
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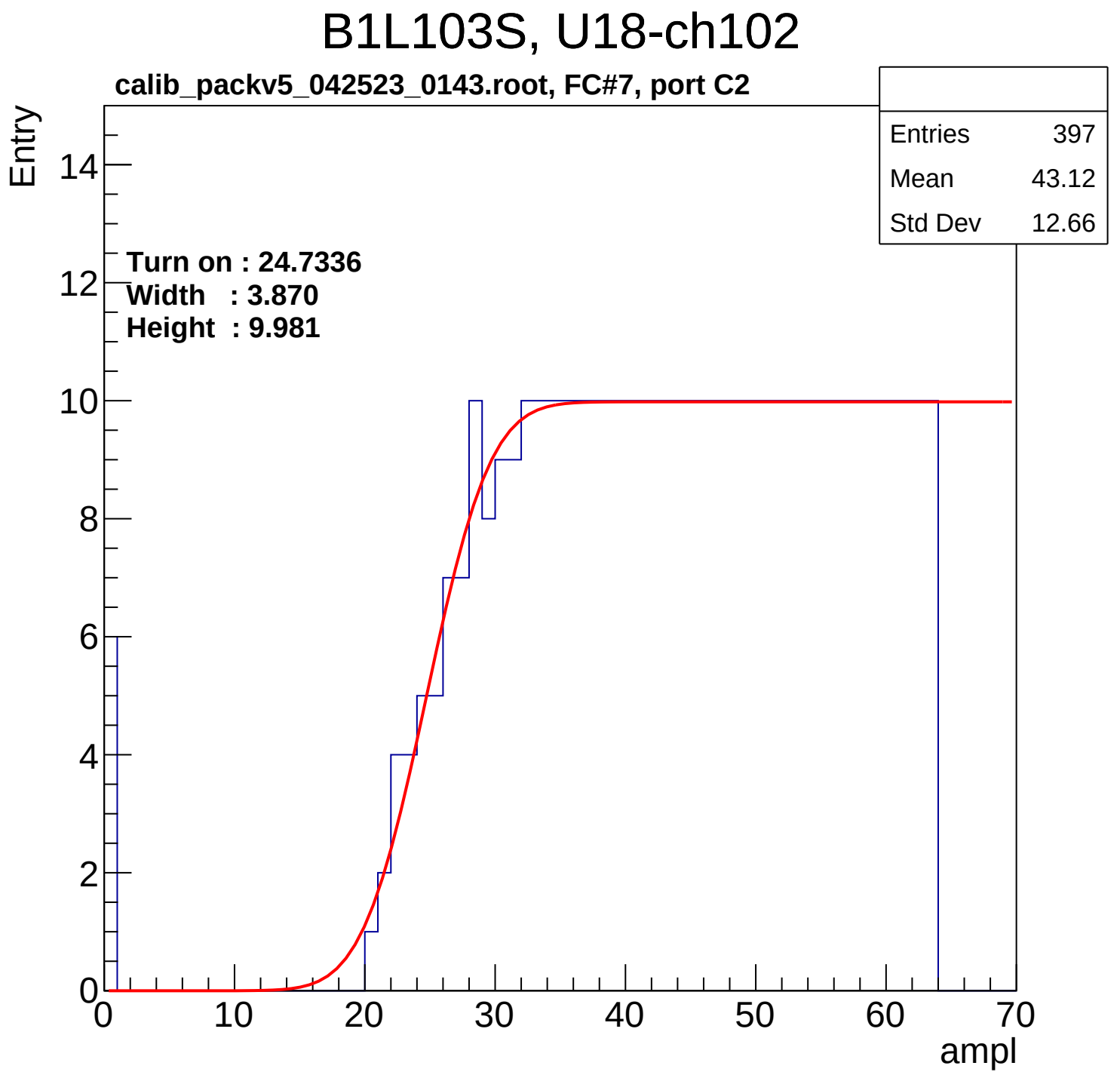
B1L103S, U18-ch102
calib_packv5_042523_0143.root, FC#7, port C2
Entries 397
Mean 43.12
Std Dev 12.66
Turn on : 24.7336
Width : 3.870
Height : 9.981
Entry
ampl
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6
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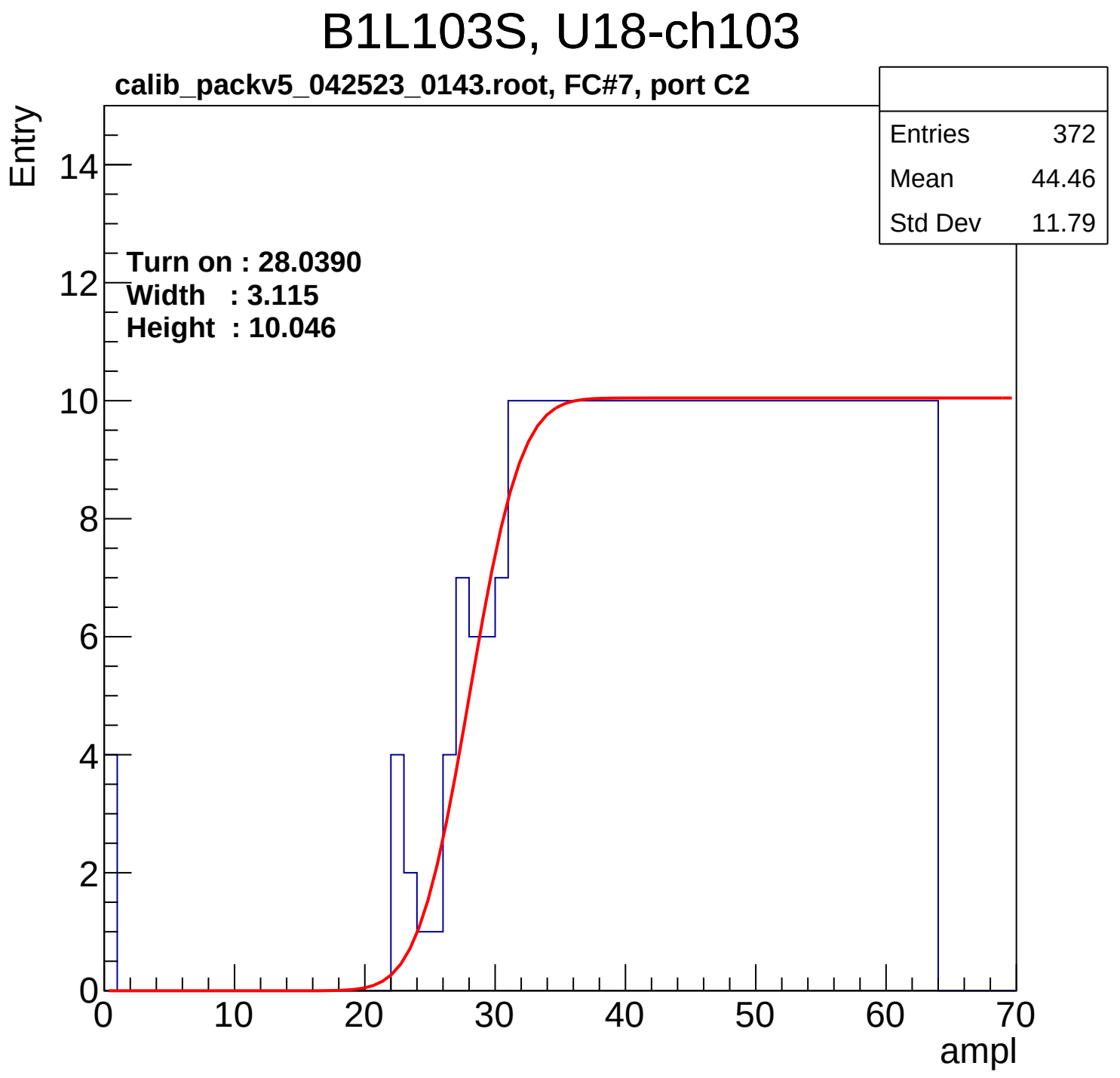
B1L103S, U18-ch103
calib_packv5_042523_0143.root, FC#7, port C2
Entries 372
Mean 44.46
Std Dev 11.79
Turn on : 28.0390
Width : 3.115
Height : 10.046
Entry
ampl
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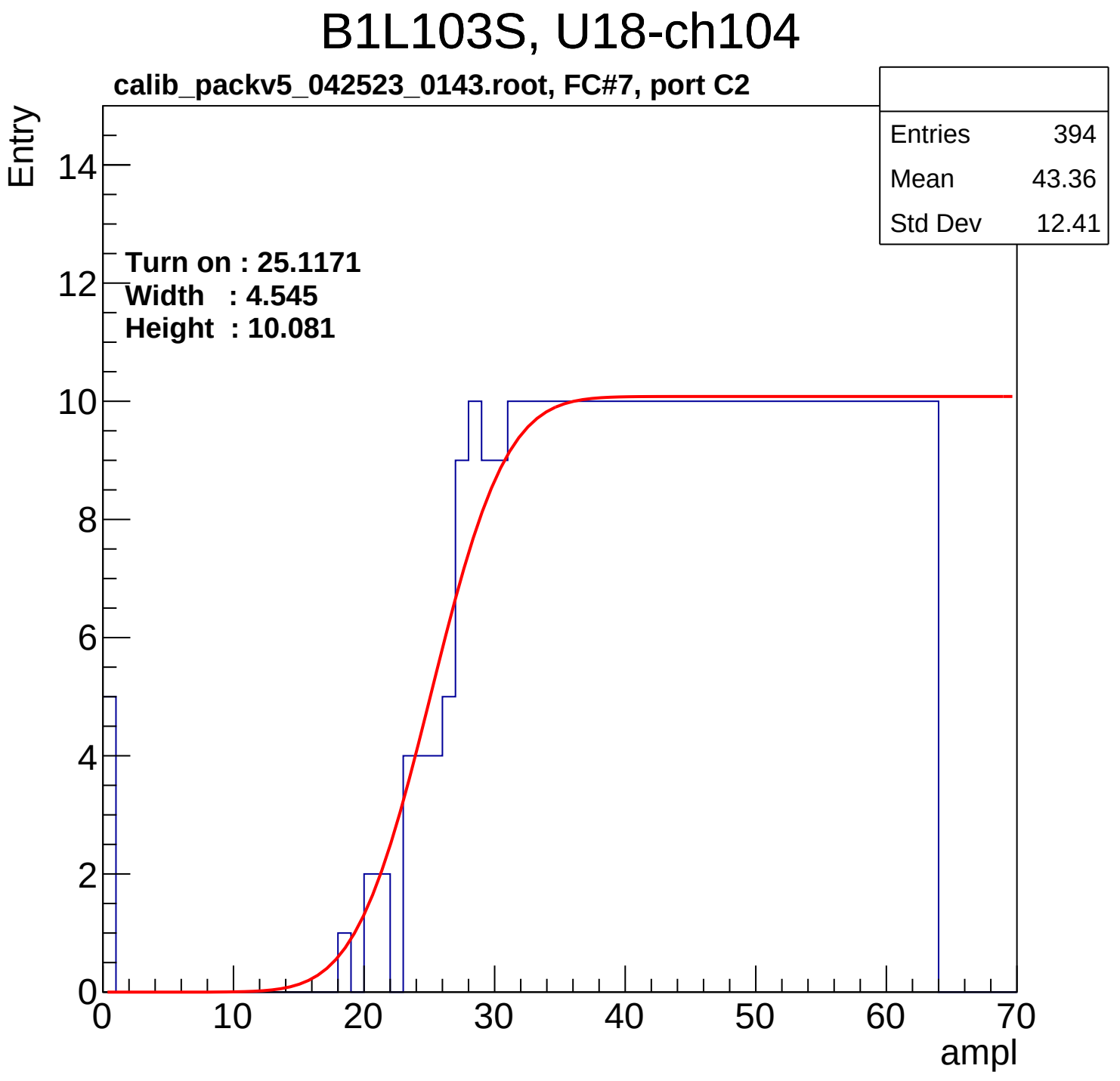
B1L103S, U18-ch104
calib_packv5_042523_0143.root, FC#7, port C2
Entries 394
Mean 43.36
Std Dev 12.41
Turn on : 25.1171
Width : 4.545
Height : 10.081
Entry
ampl
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2
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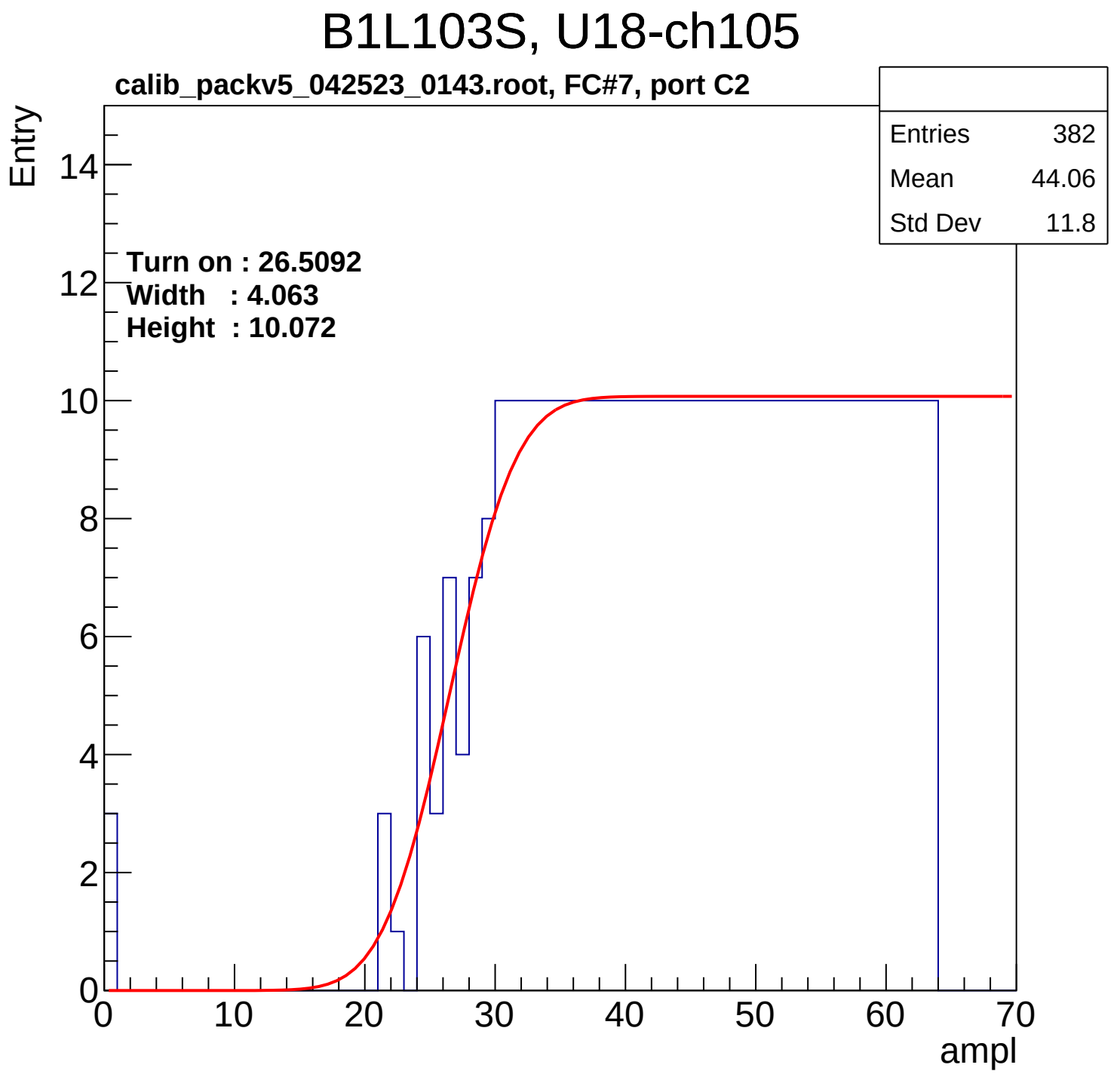
B1L103S, U18-ch105
calib_packv5_042523_0143.root, FC#7, port C2
Entries 382
Mean 44.06
Std Dev 11.8
Turn on : 26.5092
Width : 4.063
Height : 10.072
Entry
ampl
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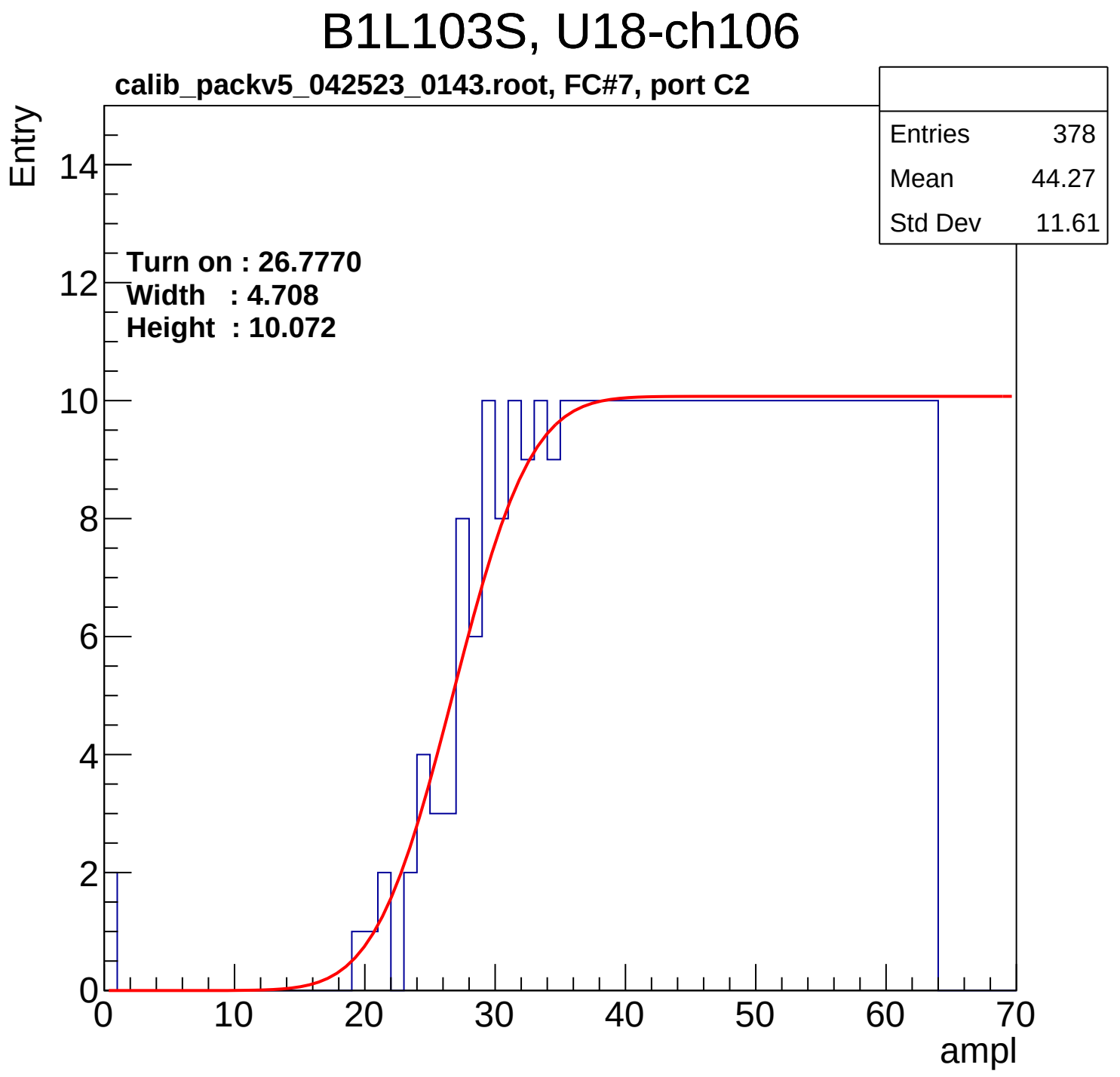
B1L103S, U18-ch106
calib_packv5_042523_0143.root, FC#7, port C2
Entries 378
Mean 44.27
Std Dev 11.61
Turn on : 26.7770
Width : 4.708
Height : 10.072
Entry
ampl
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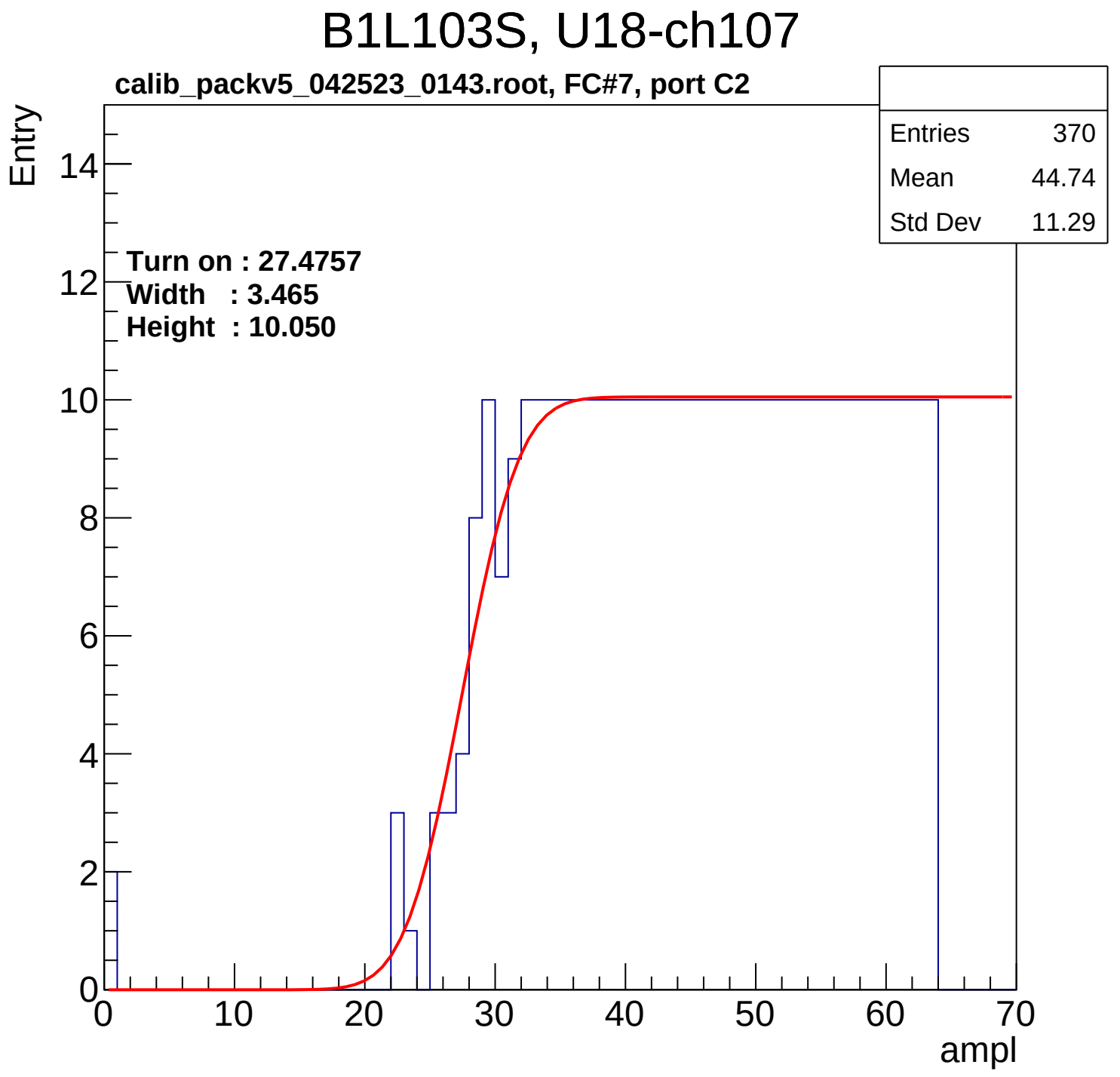
B1L103S, U18-ch107
calib_packv5_042523_0143.root, FC#7, port C2
Entries 370
Mean 44.74
Std Dev 11.29
Turn on : 27.4757
Width : 3.465
Height : 10.050
Entry
ampl
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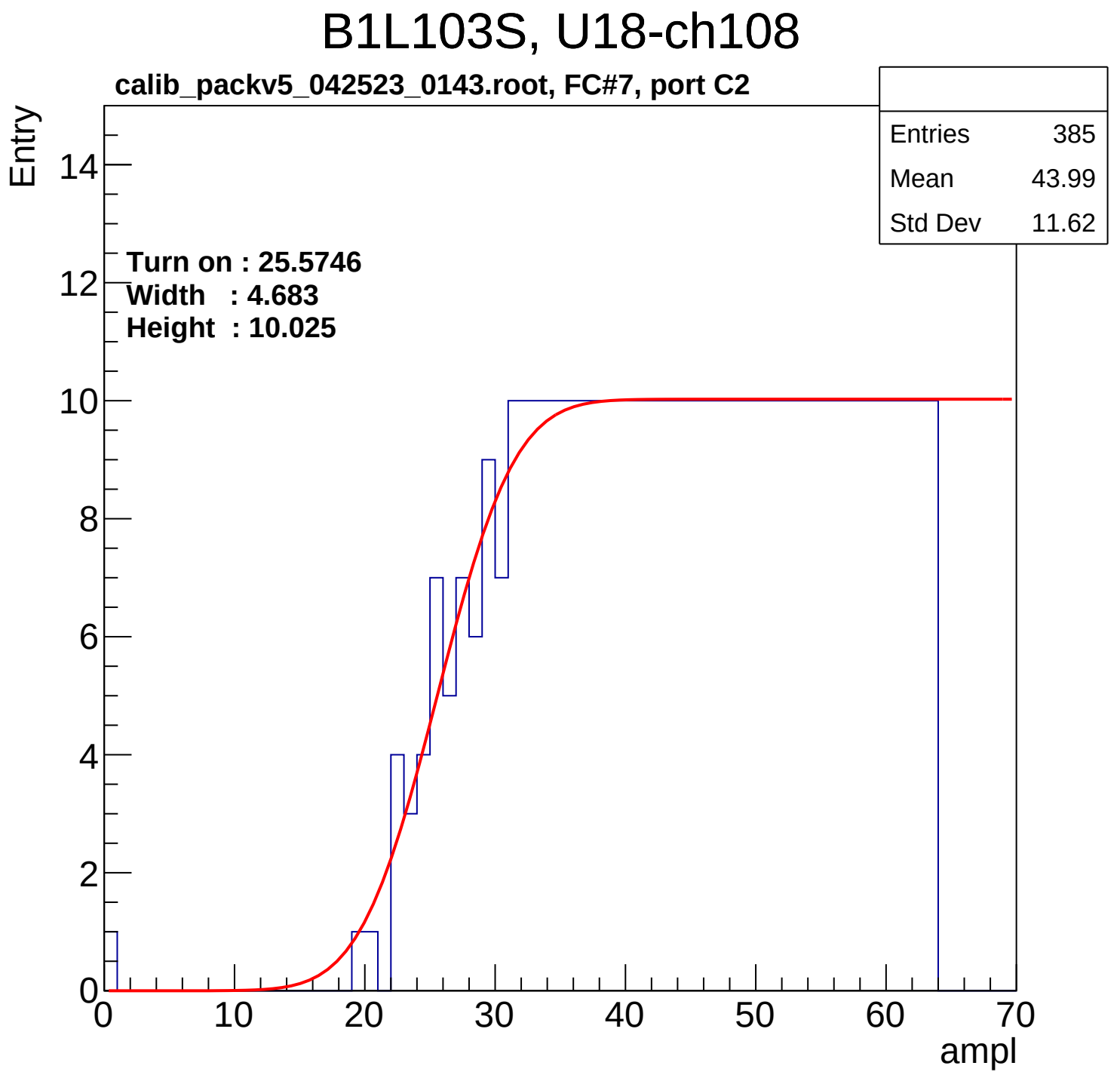
B1L103S, U18-ch108
calib_packv5_042523_0143.root, FC#7, port C2
Entries 385
Mean 43.99
Std Dev 11.62
Turn on : 25.5746
Width : 4.683
Height : 10.025
Entry
ampl
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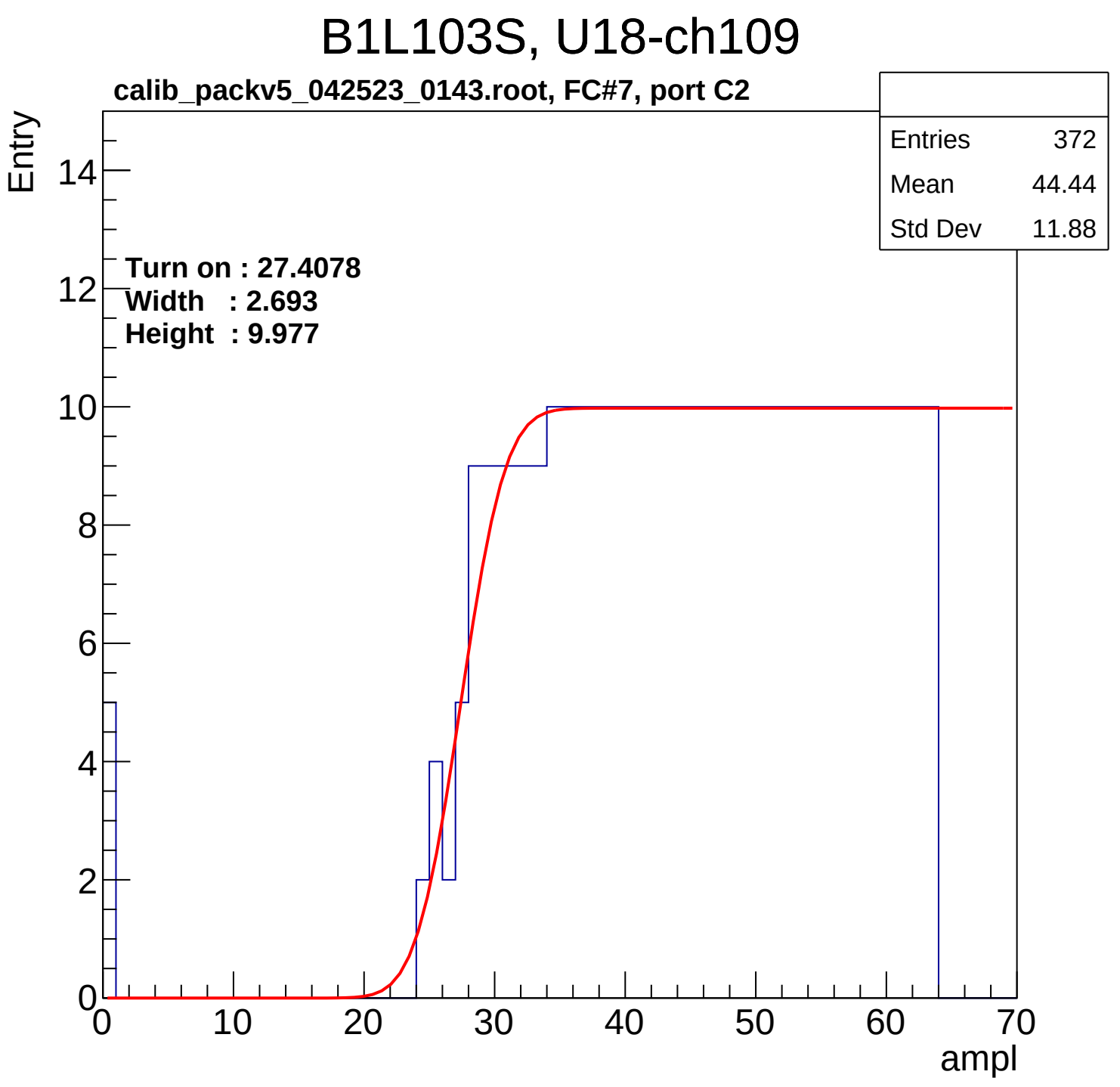
B1L103S, U18-ch109
calib_packv5_042523_0143.root, FC#7, port C2
Entries 372
Mean 44.44
Std Dev 11.88
Turn on : 27.4078
Width : 2.693
Height : 9.977
Entry
ampl
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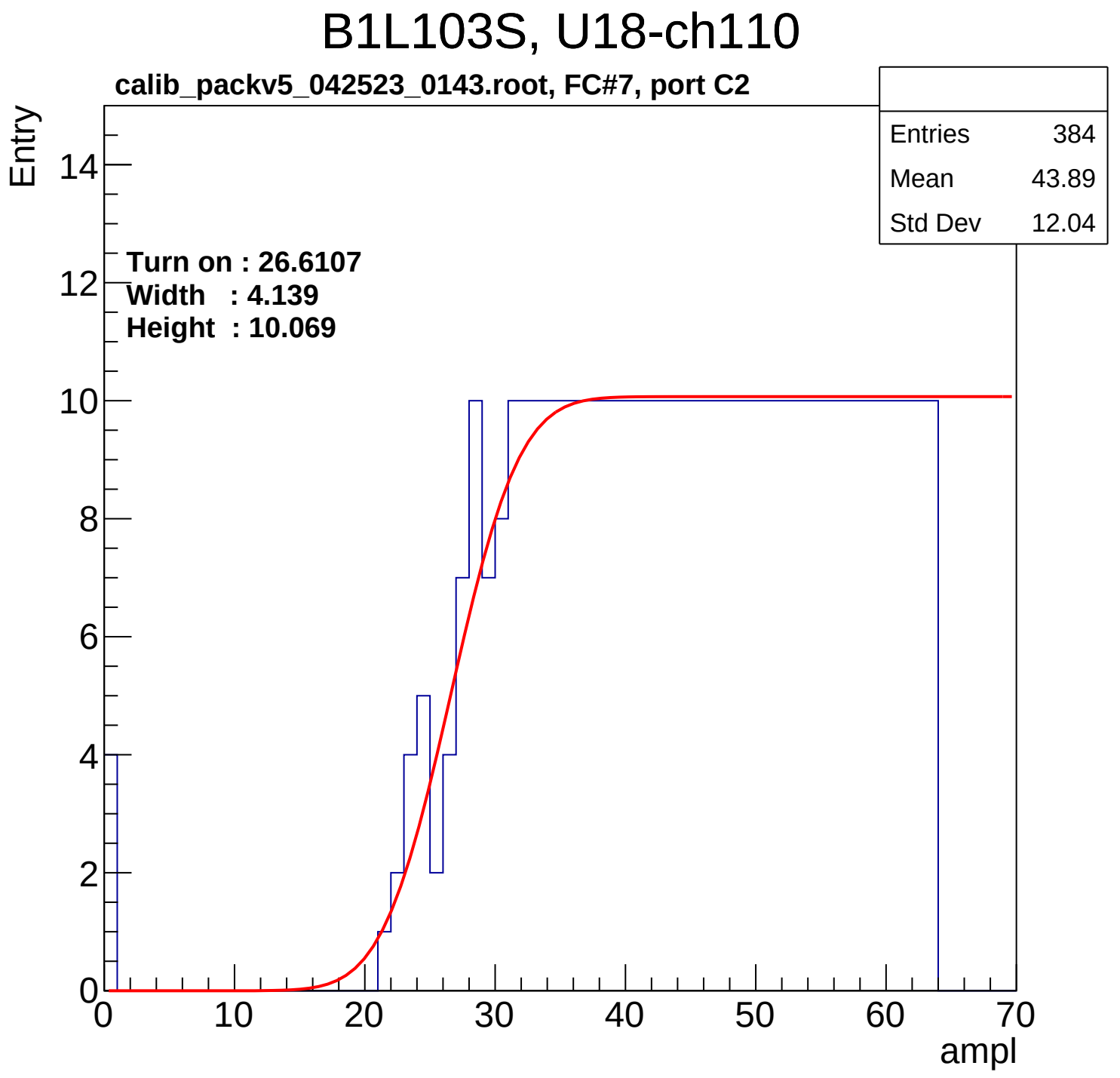
B1L103S, U18-ch110
calib_packv5_042523_0143.root, FC#7, port C2
Entries 384
Mean 43.89
Std Dev 12.04
Turn on : 26.6107
Width : 4.139
Height : 10.069
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ampl
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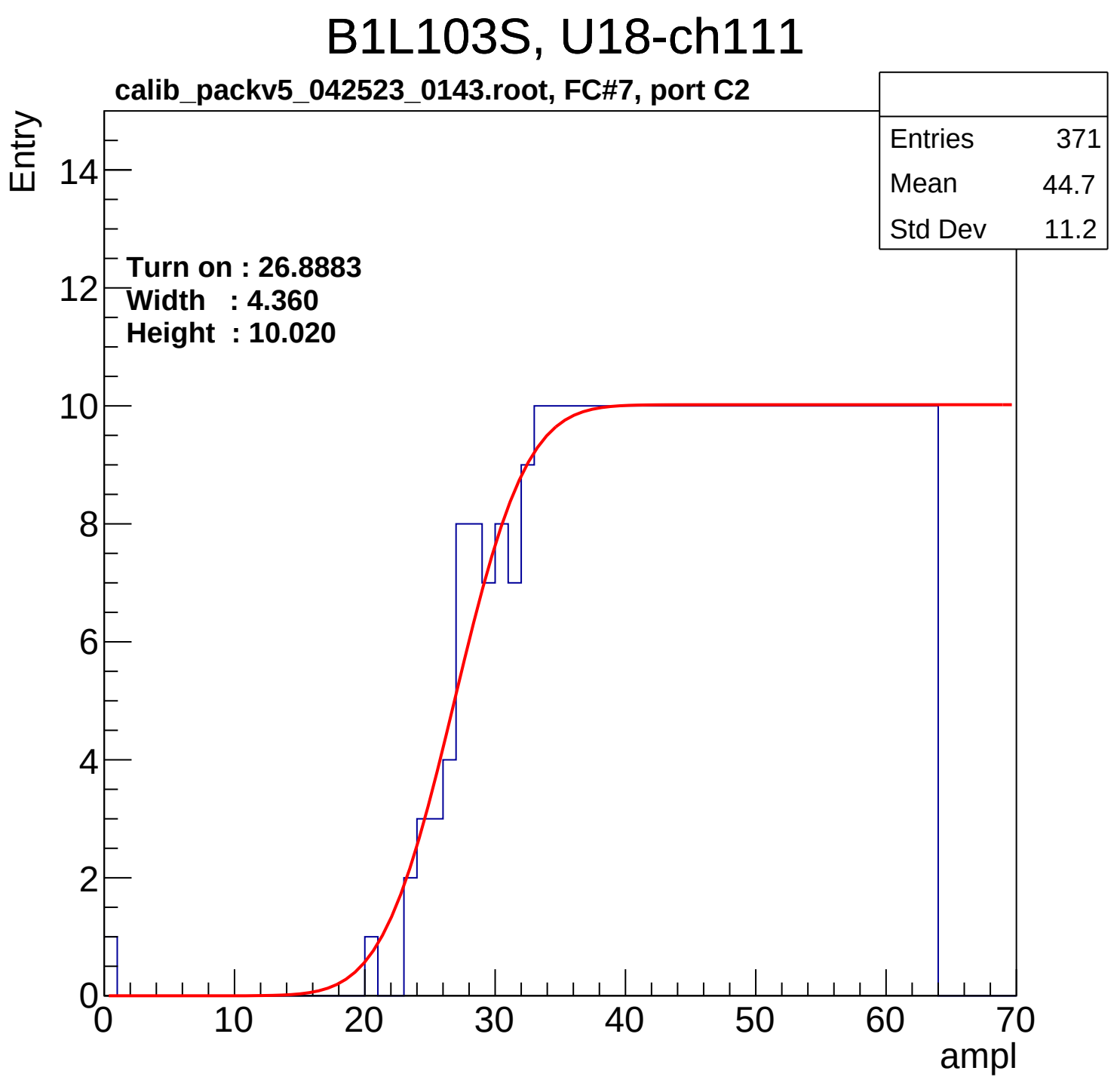
B1L103S, U18-ch111
calib_packv5_042523_0143.root, FC#7, port C2
Entries 371
Mean 44.7
Std Dev 11.2
Turn on : 26.8883
Width : 4.360
Height : 10.020
Entry
ampl
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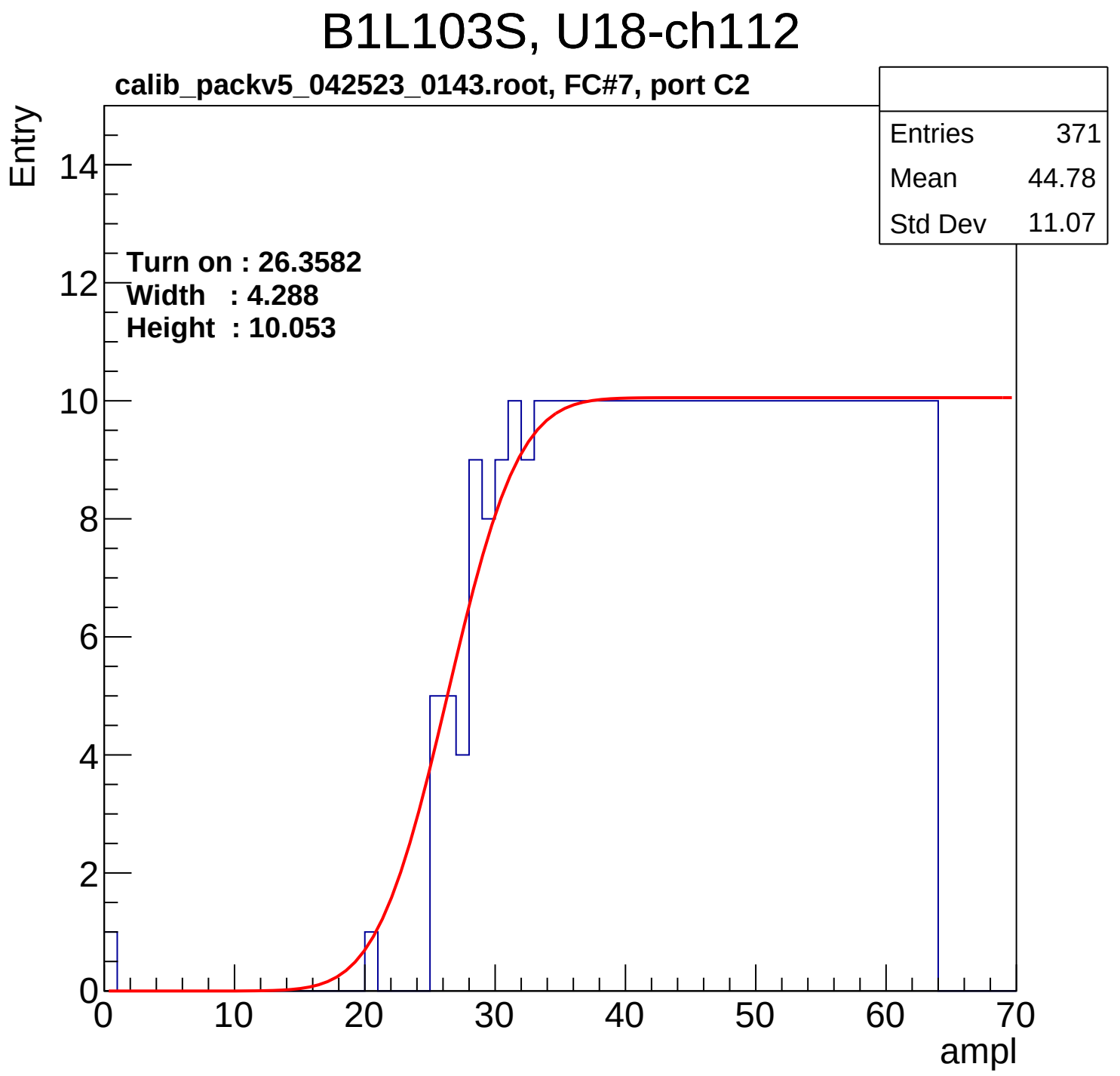
B1L103S, U18-ch112
calib_packv5_042523_0143.root, FC#7, port C2
Entries 371
Mean 44.78
Std Dev 11.07
Turn on : 26.3582
Width : 4.288
Height : 10.053
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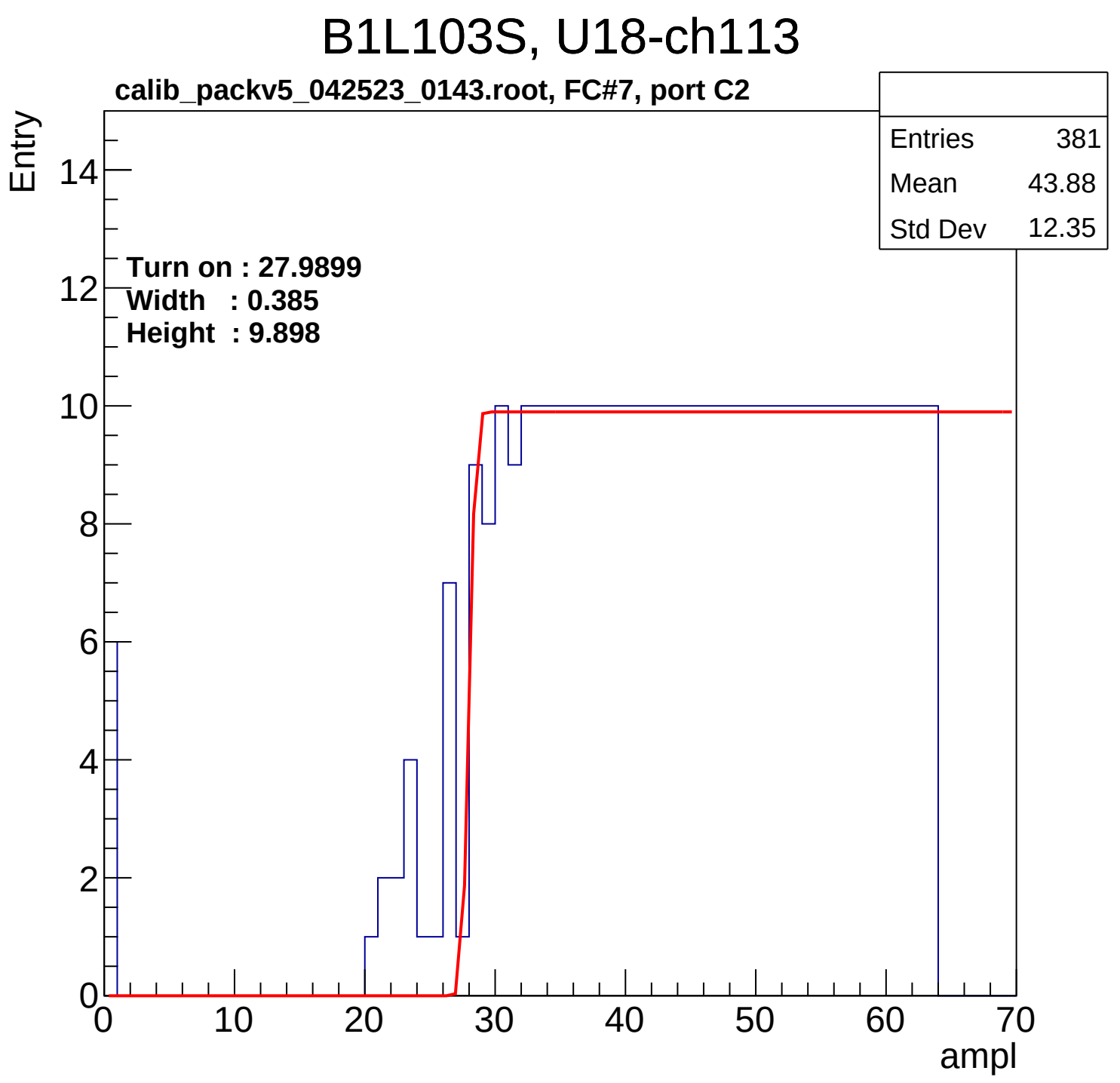
B1L103S, U18-ch113
calib_packv5_042523_0143.root, FC#7, port C2
Entries 381
Mean 43.88
Std Dev 12.35
Turn on : 27.9899
Width : 0.385
Height : 9.898
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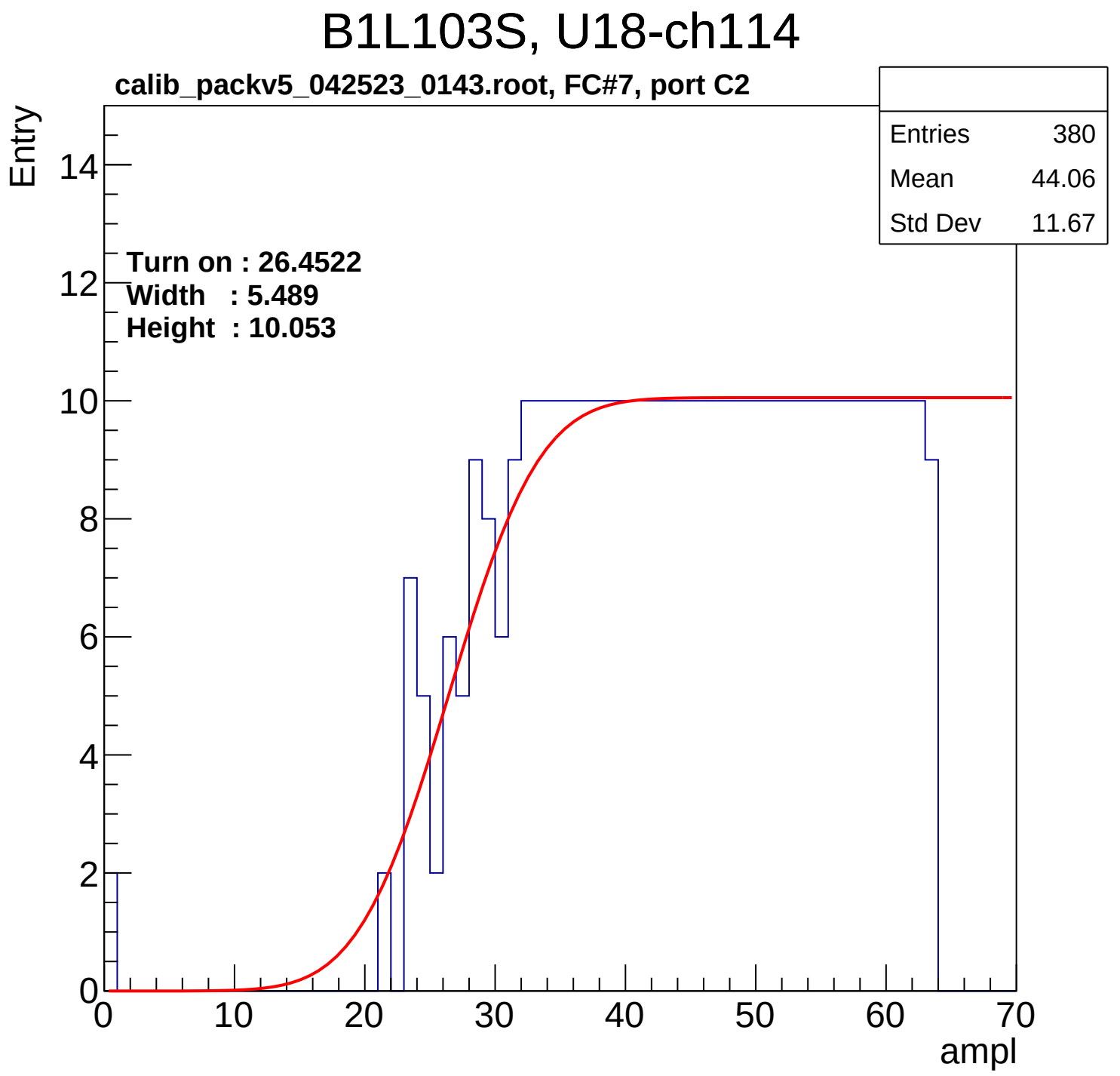
B1L103S, U18-ch114
calib_packv5_042523_0143.root, FC#7, port C2
Entries 380
Mean 44.06
Std Dev 11.67
Turn on : 26.4522
Width : 5.489
Height : 10.053
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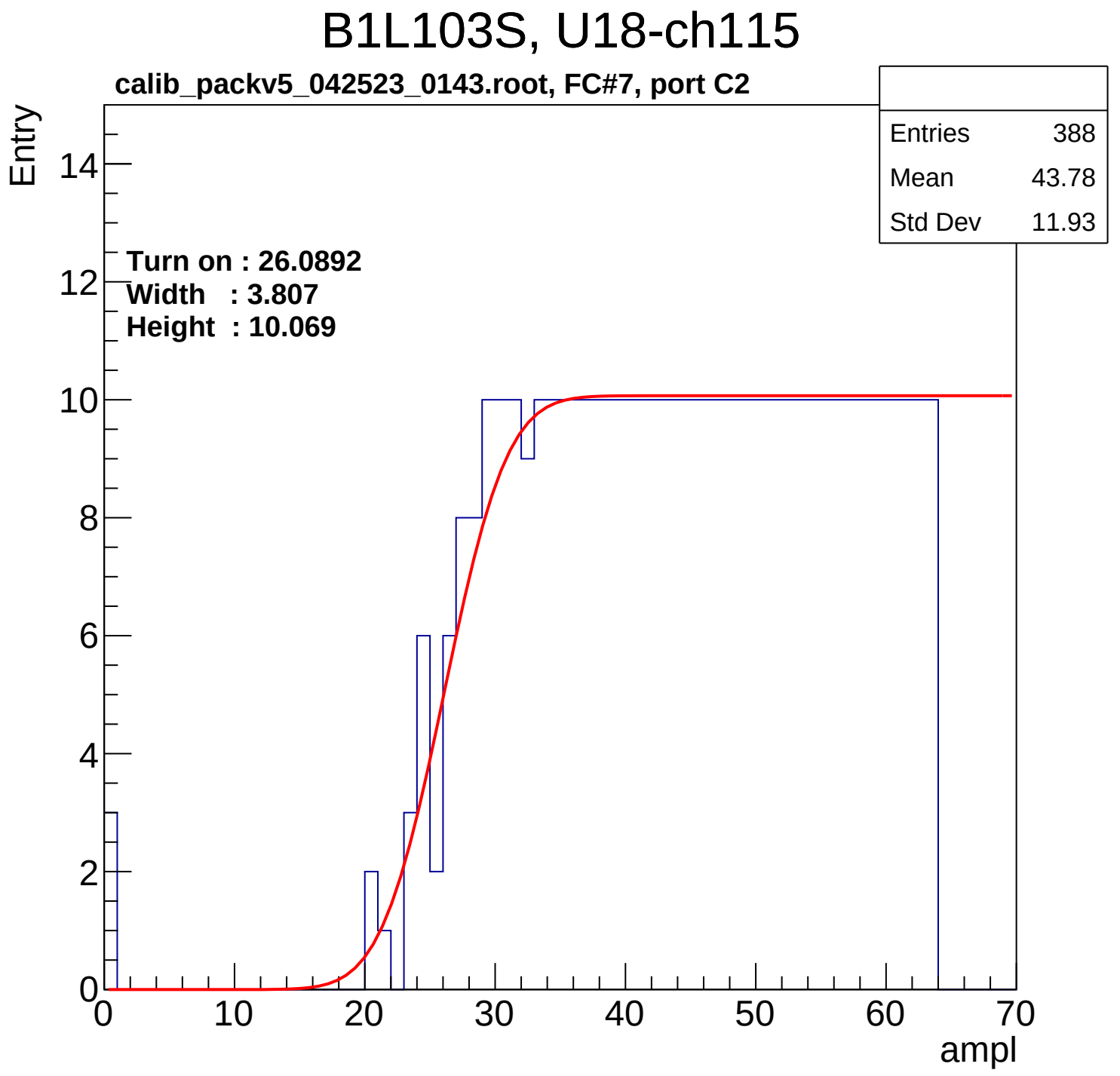
B1L103S, U18-ch115
calib_packv5_042523_0143.root, FC#7, port C2
Entries 388
Mean 43.78
Std Dev 11.93
Turn on : 26.0892
Width : 3.807
Height : 10.069
Entry
ampl
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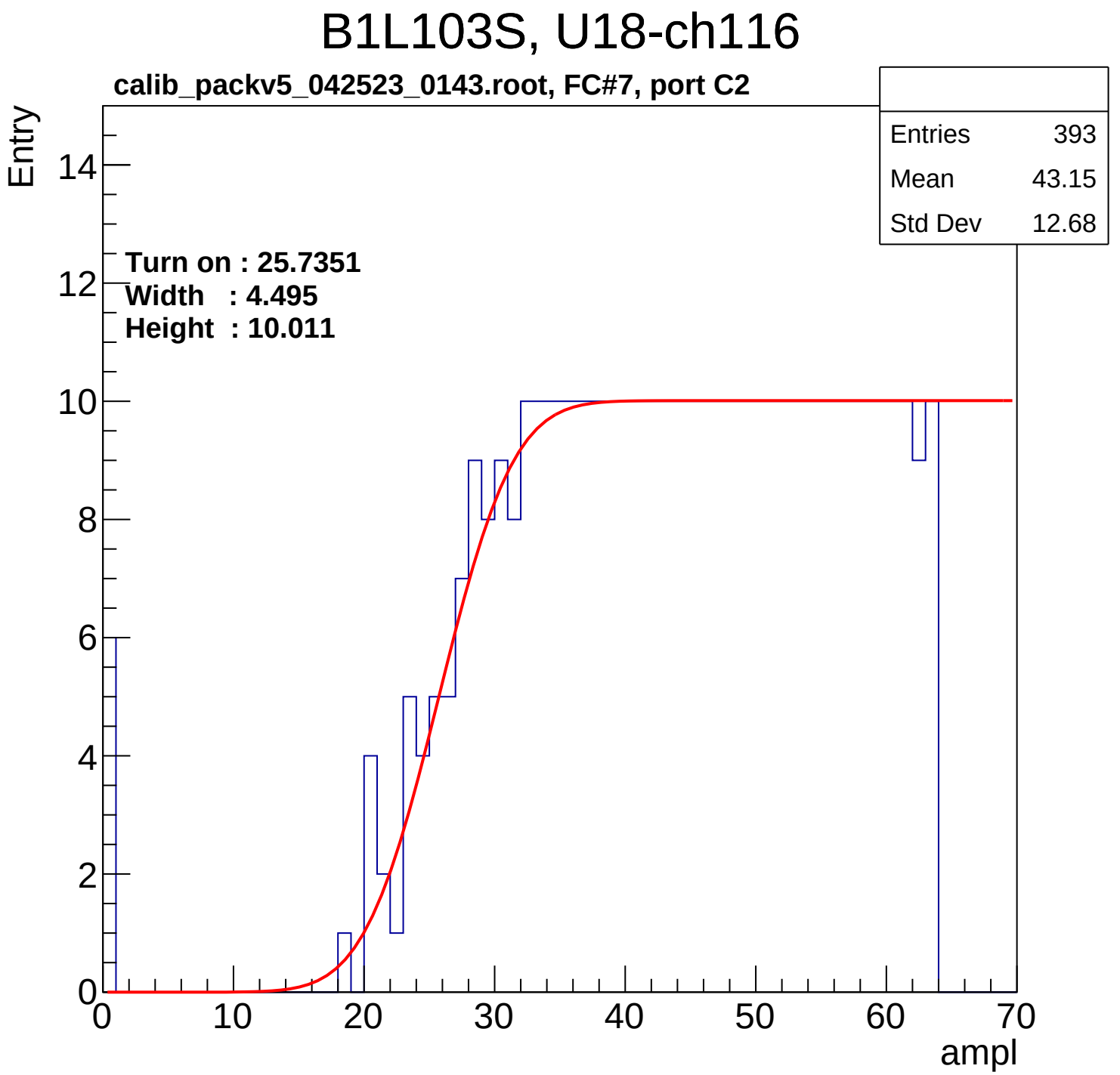
B1L103S, U18-ch116
calib_packv5_042523_0143.root, FC#7, port C2
Entries 393
Mean 43.15
Std Dev 12.68
Turn on : 25.7351
Width : 4.495
Height : 10.011
Entry
ampl
0
2
4
6
8
10
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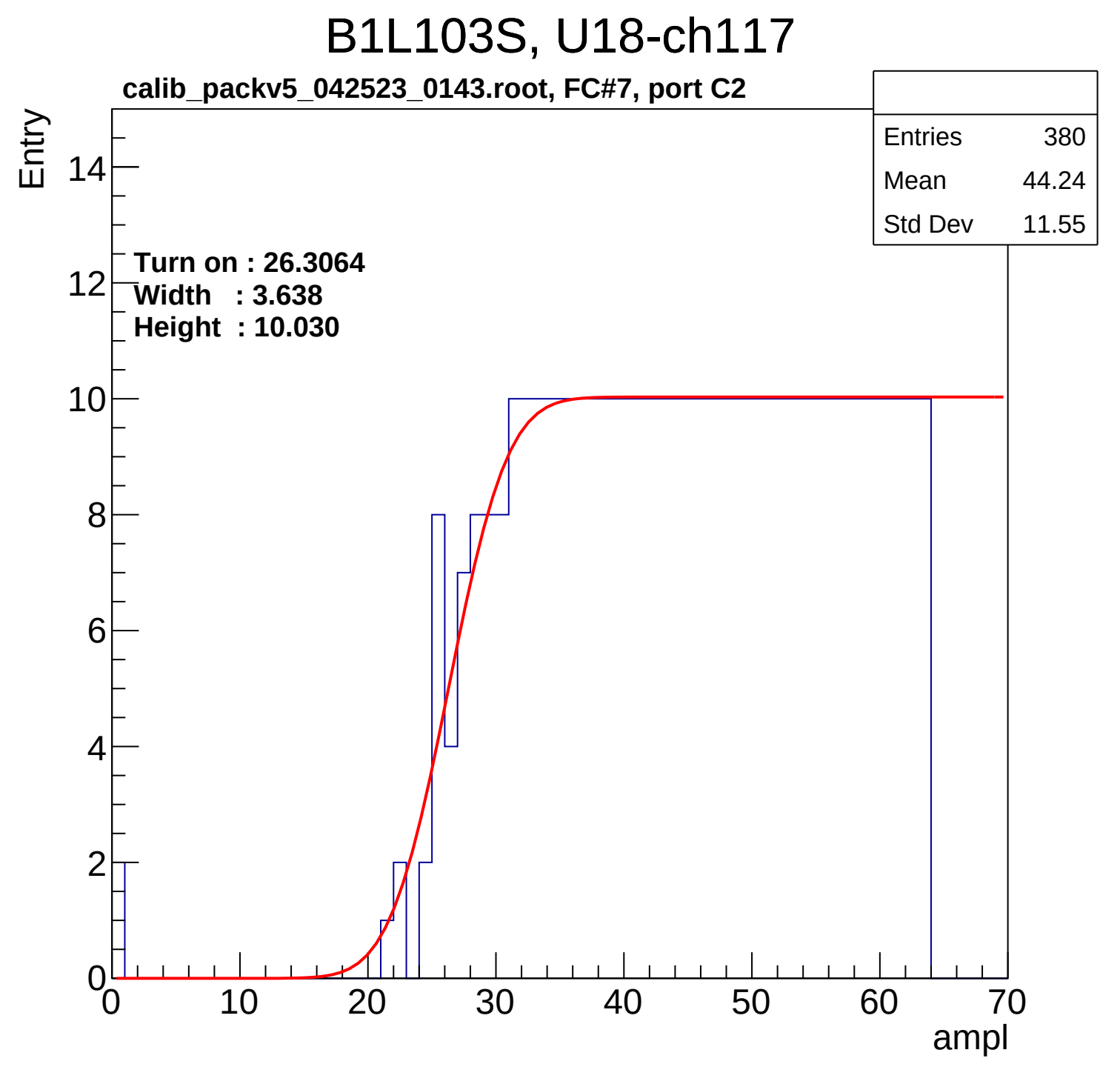
B1L103S, U18-ch117
calib_packv5_042523_0143.root, FC#7, port C2
Entries 380
Mean 44.24
Std Dev 11.55
Turn on : 26.3064
Width : 3.638
Height : 10.030
Entry
ampl
0
2
4
6
8
10
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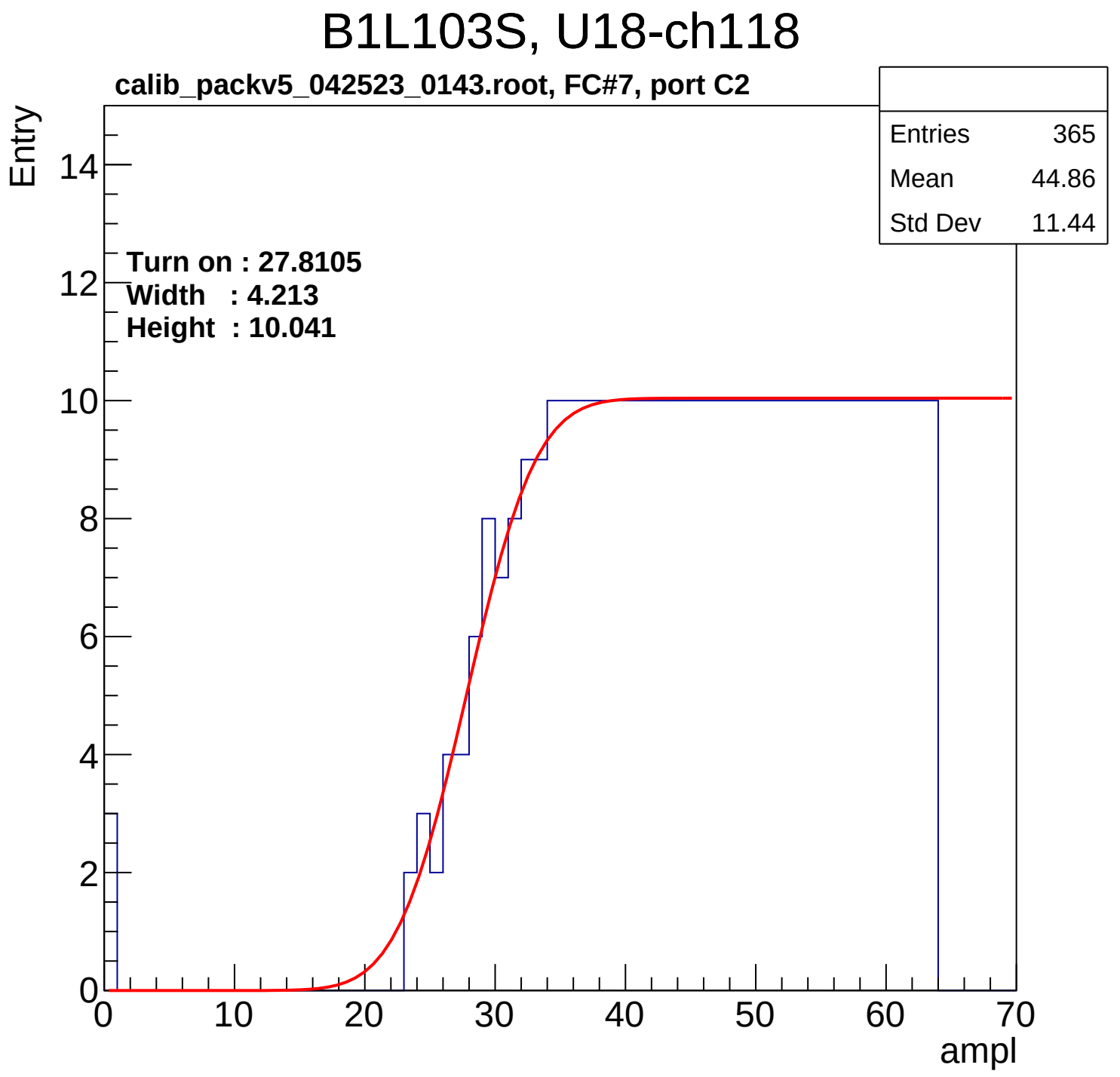
B1L103S, U18-ch118
calib_packv5_042523_0143.root, FC#7, port C2
Entries 365
Mean 44.86
Std Dev 11.44
Turn on : 27.8105
Width : 4.213
Height : 10.041
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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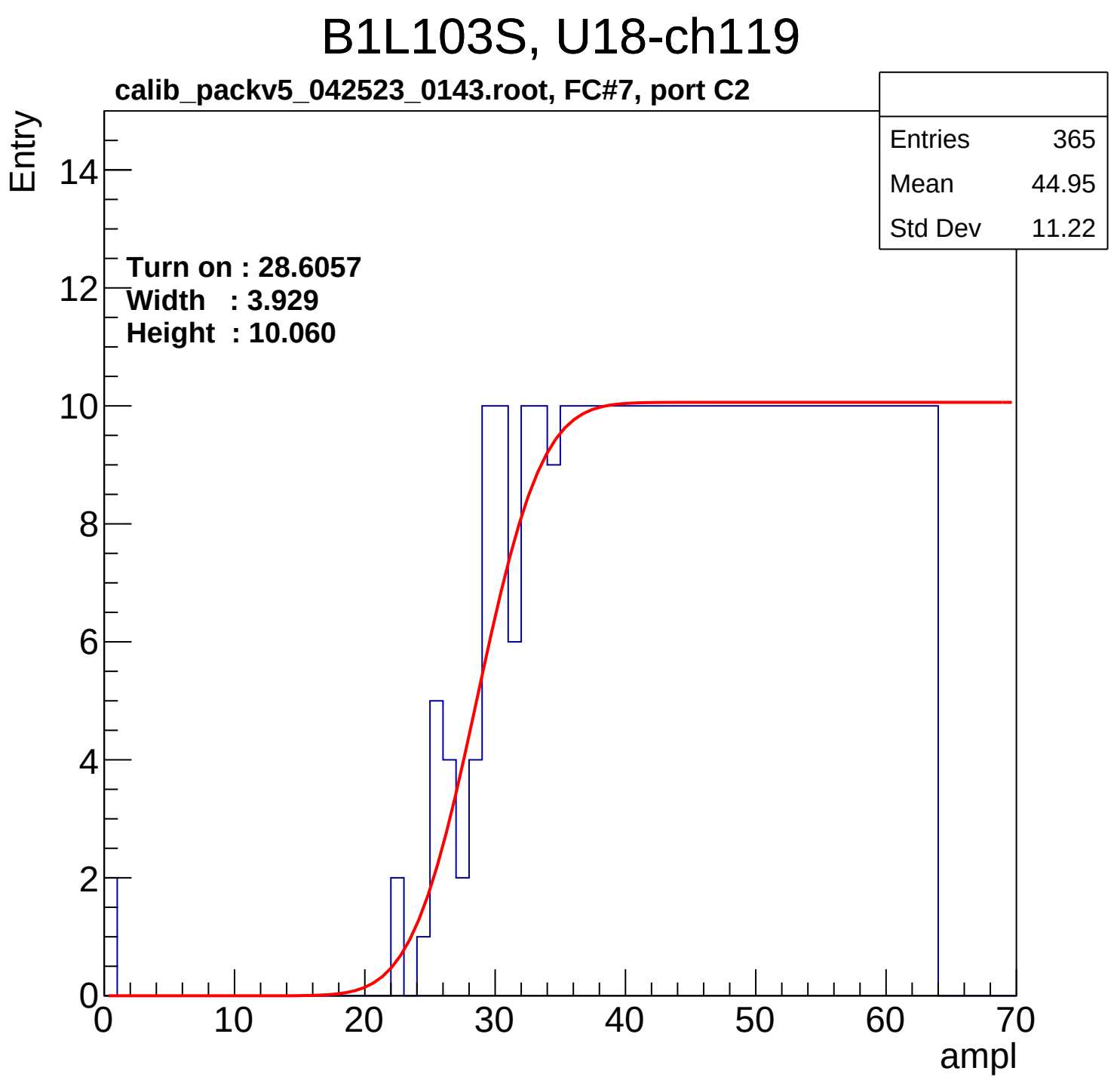
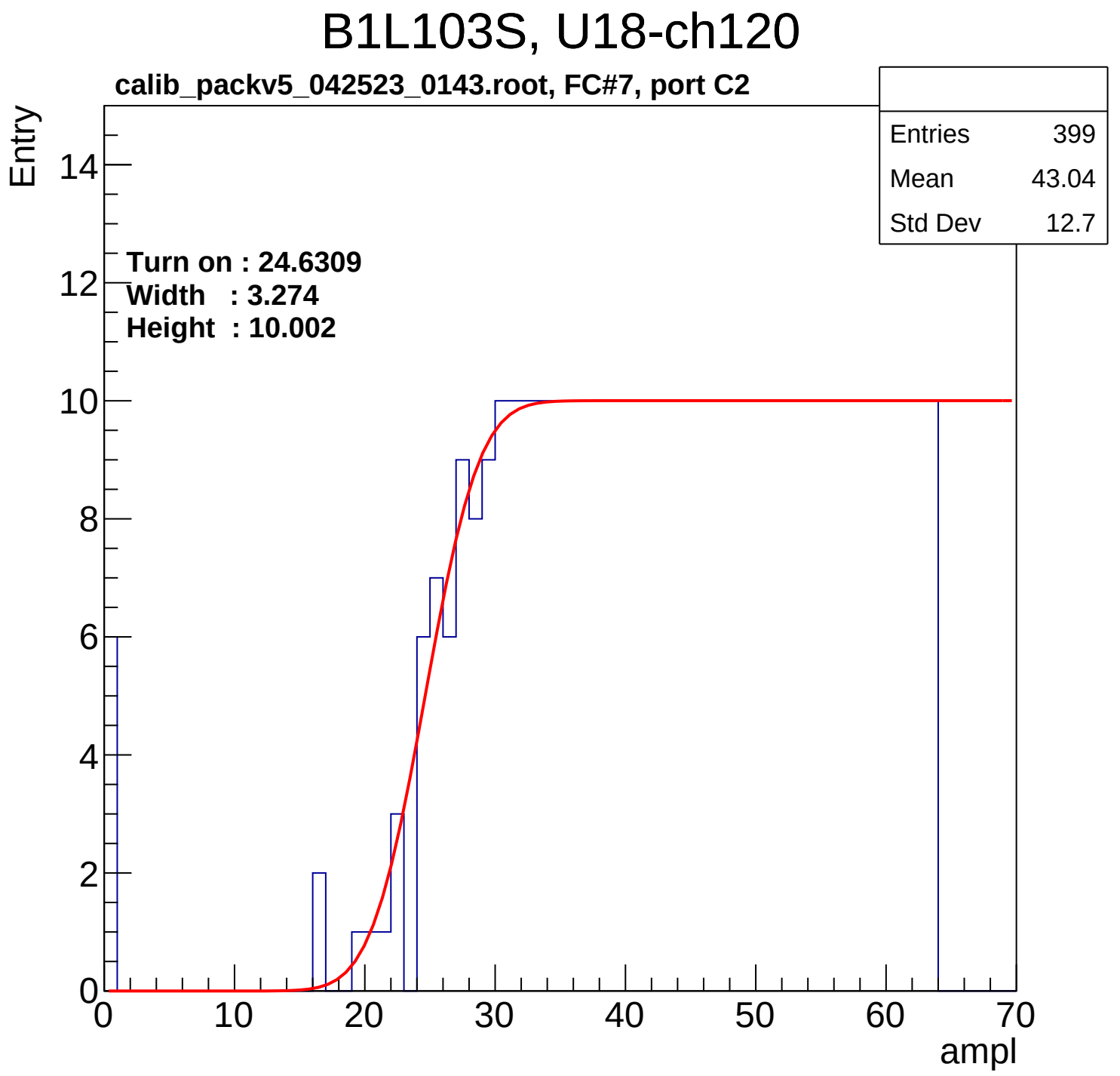

B1L103S, U18-ch119
calib_packv5_042523_0143.root, FC#7, port C2
Entries 365
Mean 44.95
Std Dev 11.22
Turn on : 28.6057
Width : 3.929
Height : 10.060
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U18-ch120
calib_packv5_042523_0143.root, FC#7, port C2
Entries 399
Mean 43.04
Std Dev 12.7
Turn on : 24.6309
Width : 3.274
Height : 10.002
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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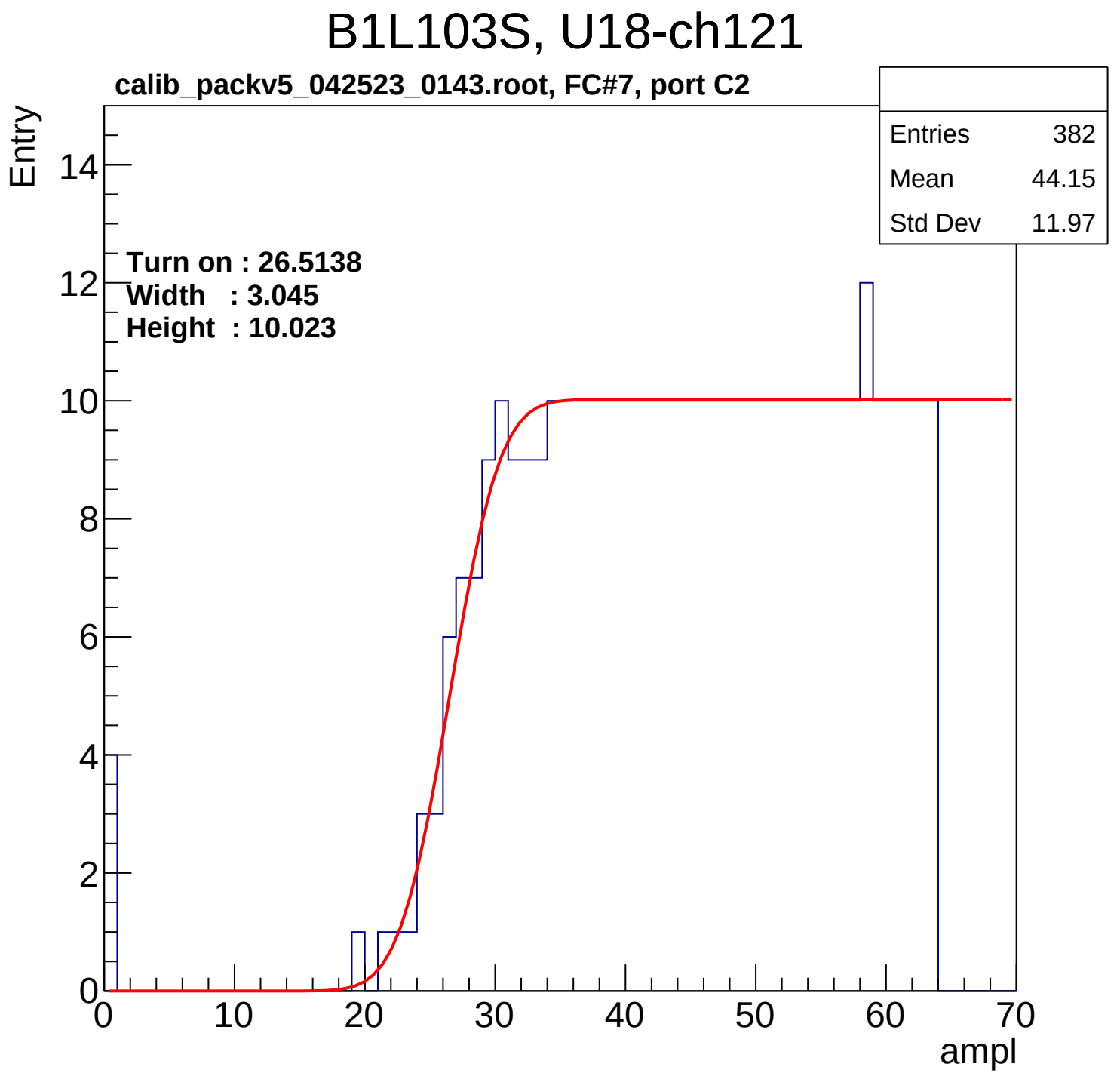
B1L103S, U18-ch121
calib_packv5_042523_0143.root, FC#7, port C2
Entries 382
Mean 44.15
Std Dev 11.97
Turn on : 26.5138
Width : 3.045
Height : 10.023
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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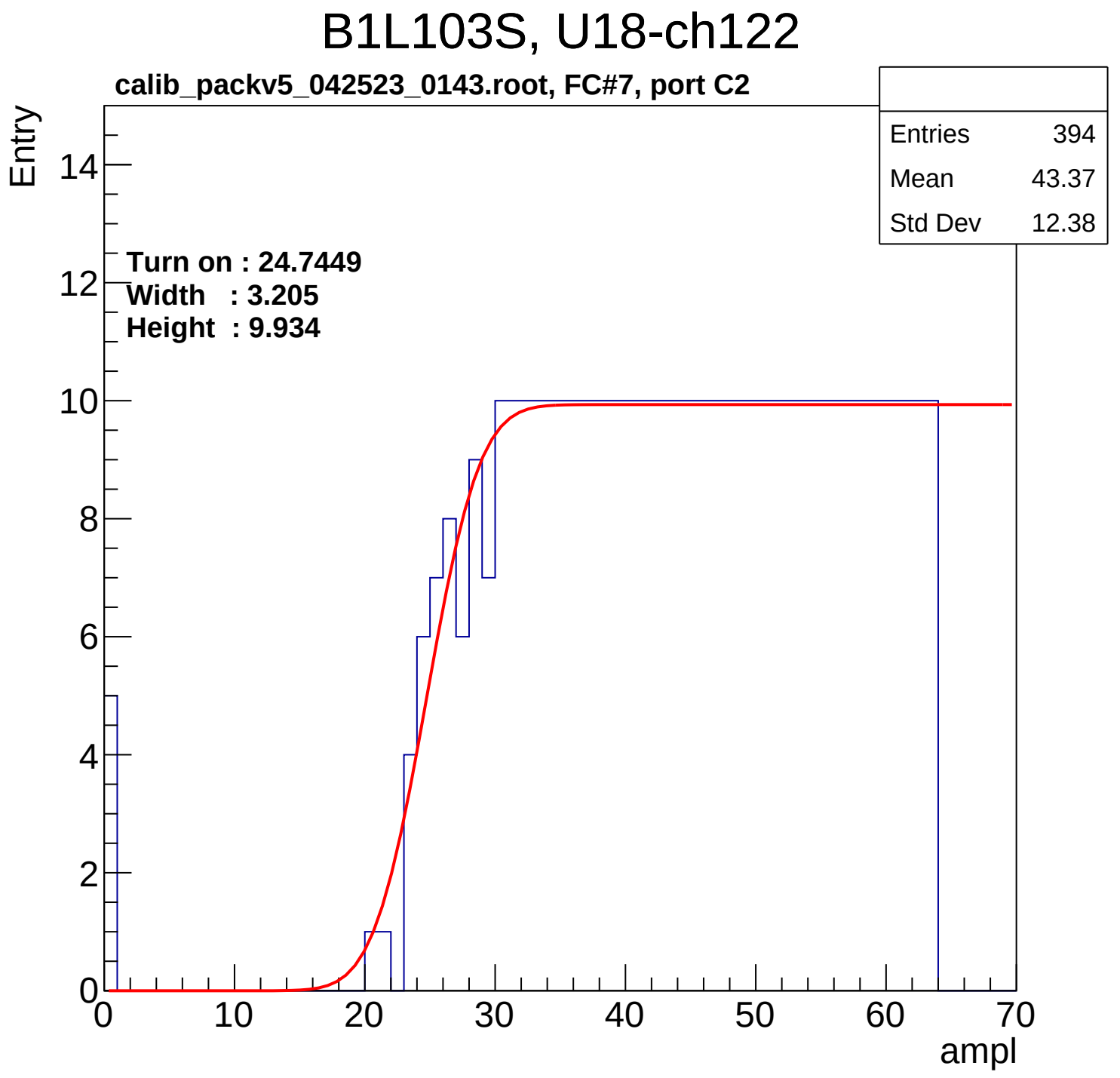
B1L103S, U18-ch122
calib_packv5_042523_0143.root, FC#7, port C2
Entries 394
Mean 43.37
Std Dev 12.38
Turn on : 24.7449
Width : 3.205
Height : 9.934
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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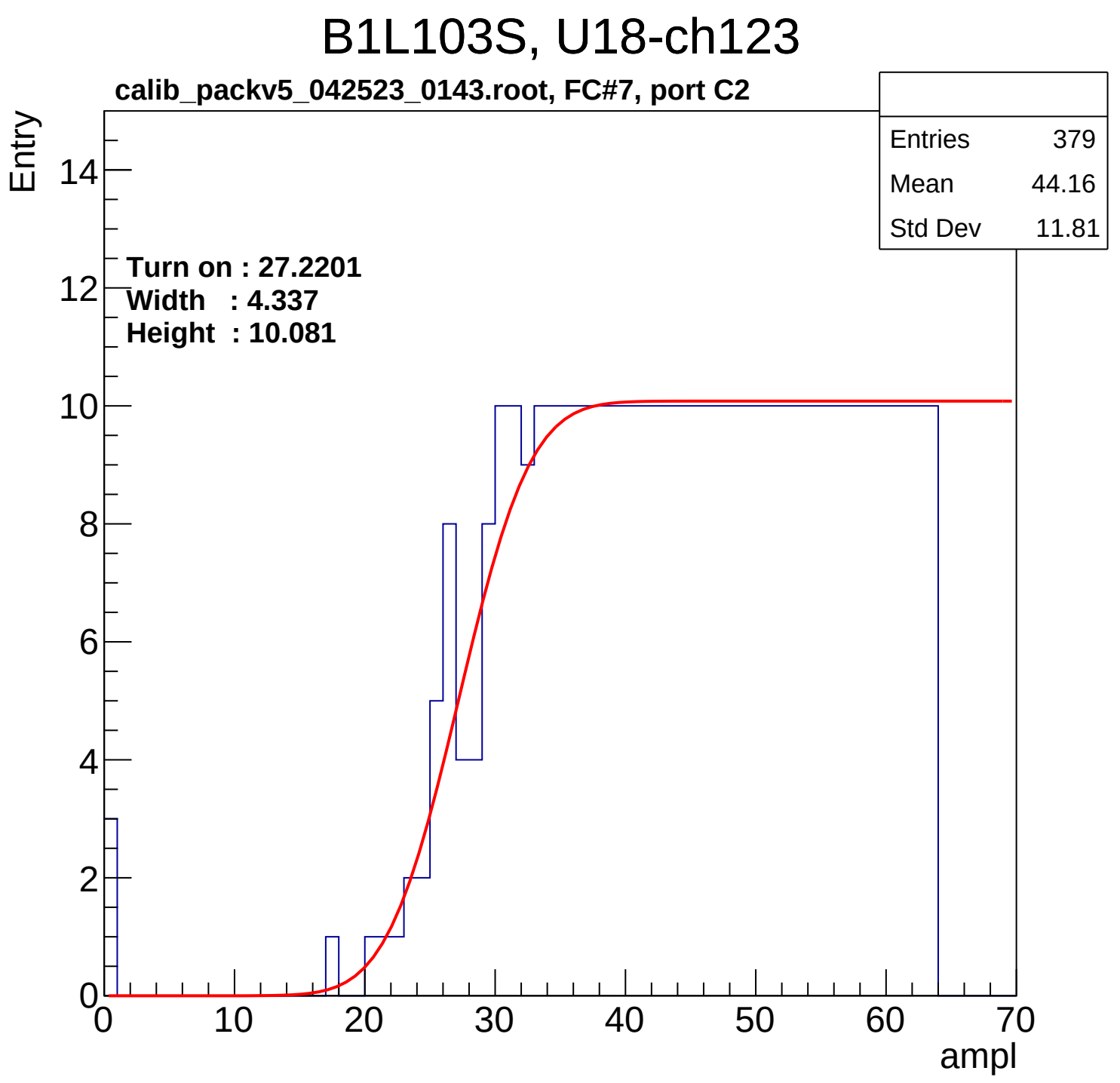
B1L103S, U18-ch123
calib_packv5_042523_0143.root, FC#7, port C2
Entries 379
Mean 44.16
Std Dev 11.81
Turn on : 27.2201
Width : 4.337
Height : 10.081
Entry
ampl
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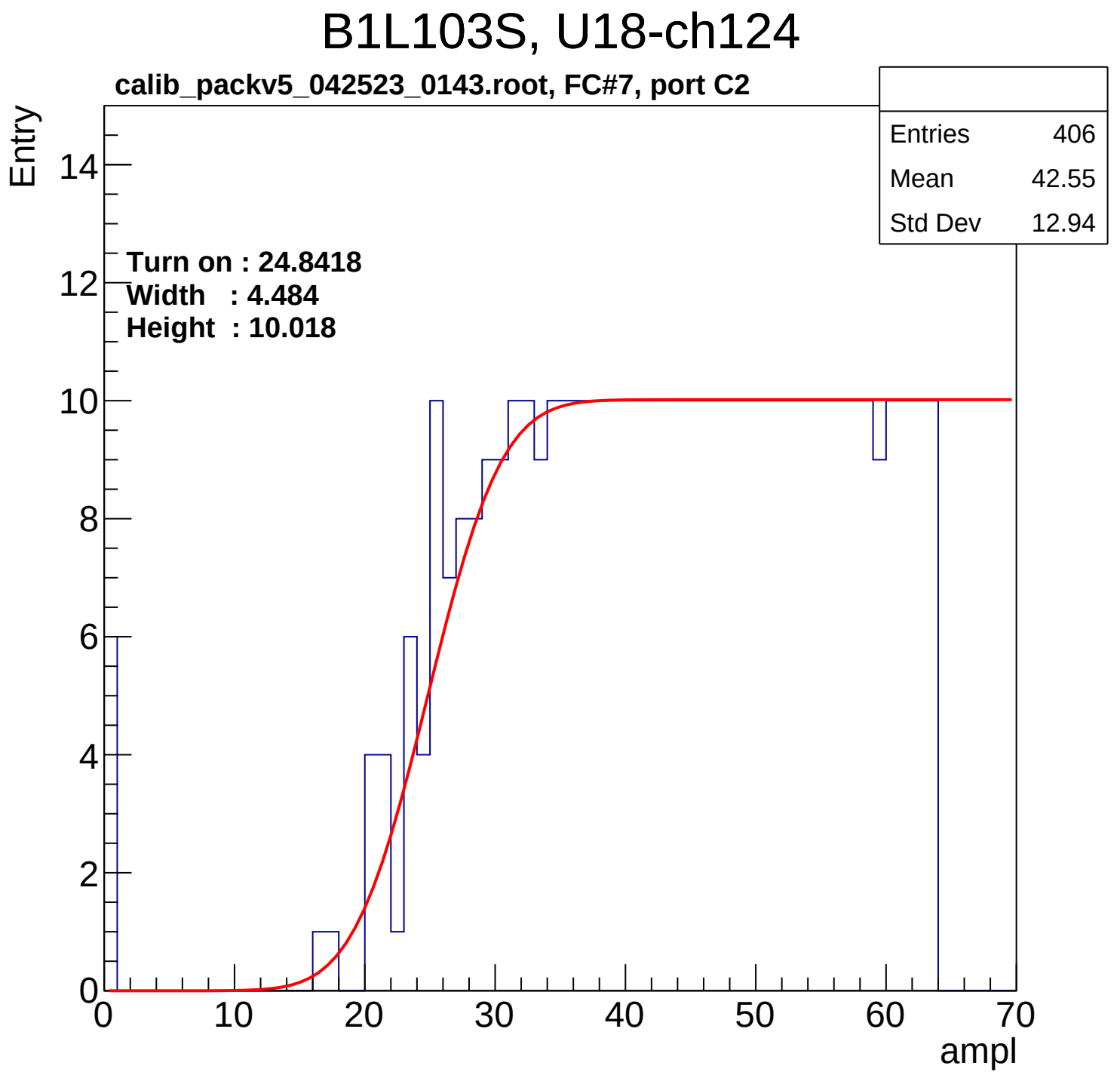
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U18-ch124
calib_packv5_042523_0143.root, FC#7, port C2
Entries 406
Mean 42.55
Std Dev 12.94
Turn on : 24.8418
Width : 4.484
Height : 10.018
Entry
ampl
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2
4
6
8
10
12
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0
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20
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40
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60
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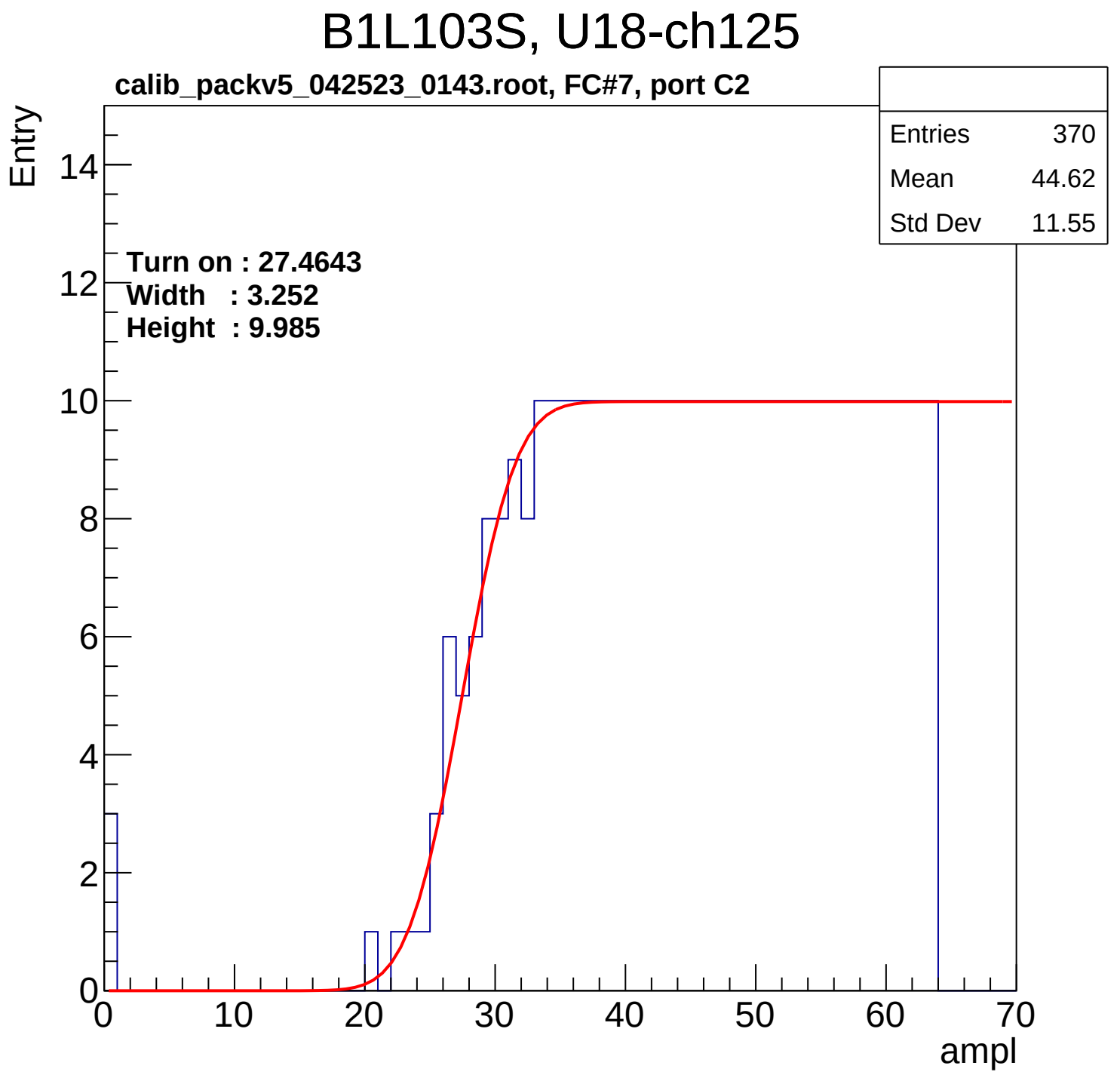
B1L103S, U18-ch125
calib_packv5_042523_0143.root, FC#7, port C2
Entries 370
Mean 44.62
Std Dev 11.55
Turn on : 27.4643
Width : 3.252
Height : 9.985
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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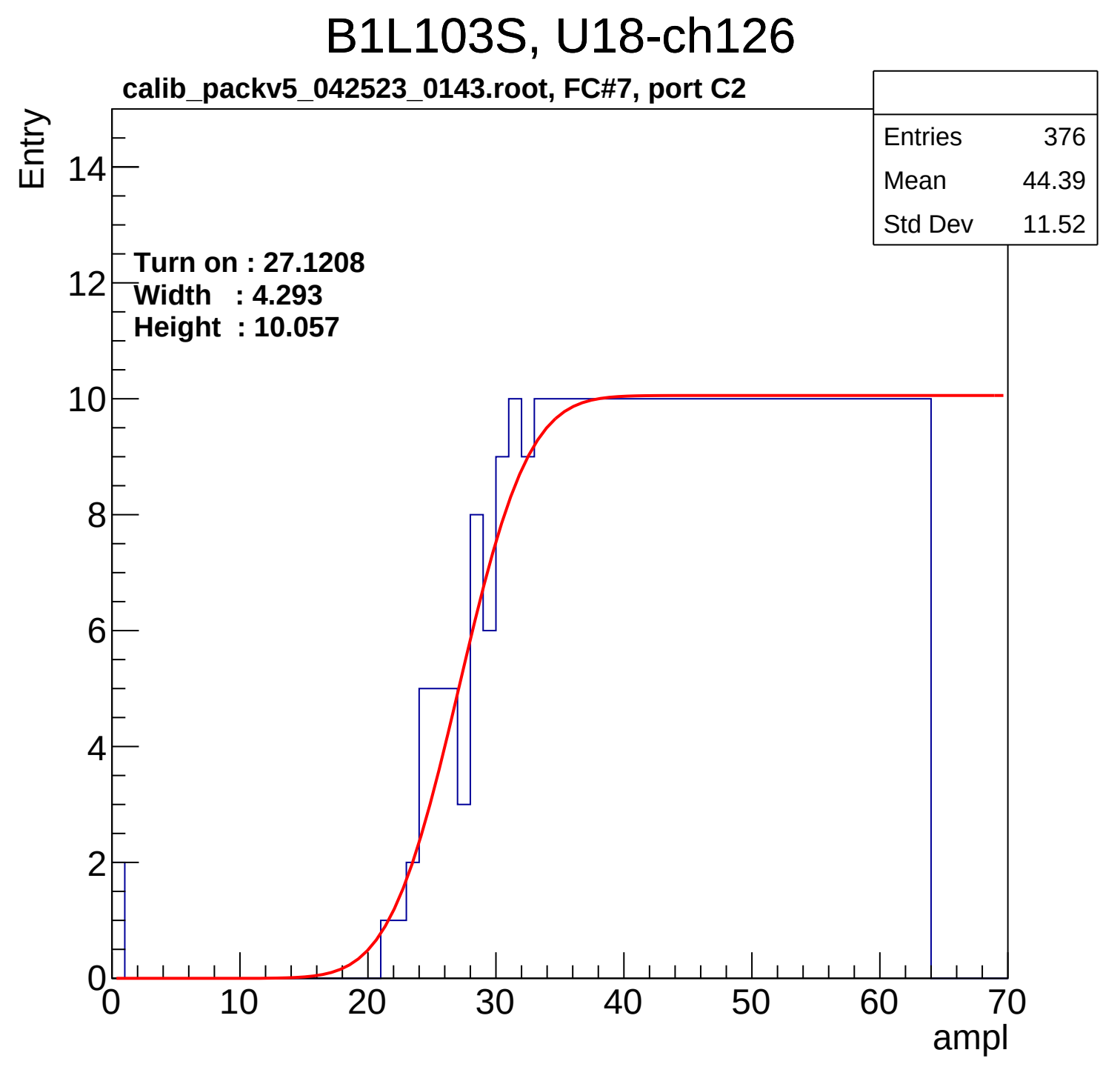
40
50
60
70


B1L103S, U18-ch126
calib_packv5_042523_0143.root, FC#7, port C2
Entries 376
Mean 44.39
Std Dev 11.52
Turn on : 27.1208
Width : 4.293
Height : 10.057
Entry
ampl
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2
4
6
8
10
12
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0
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20
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60
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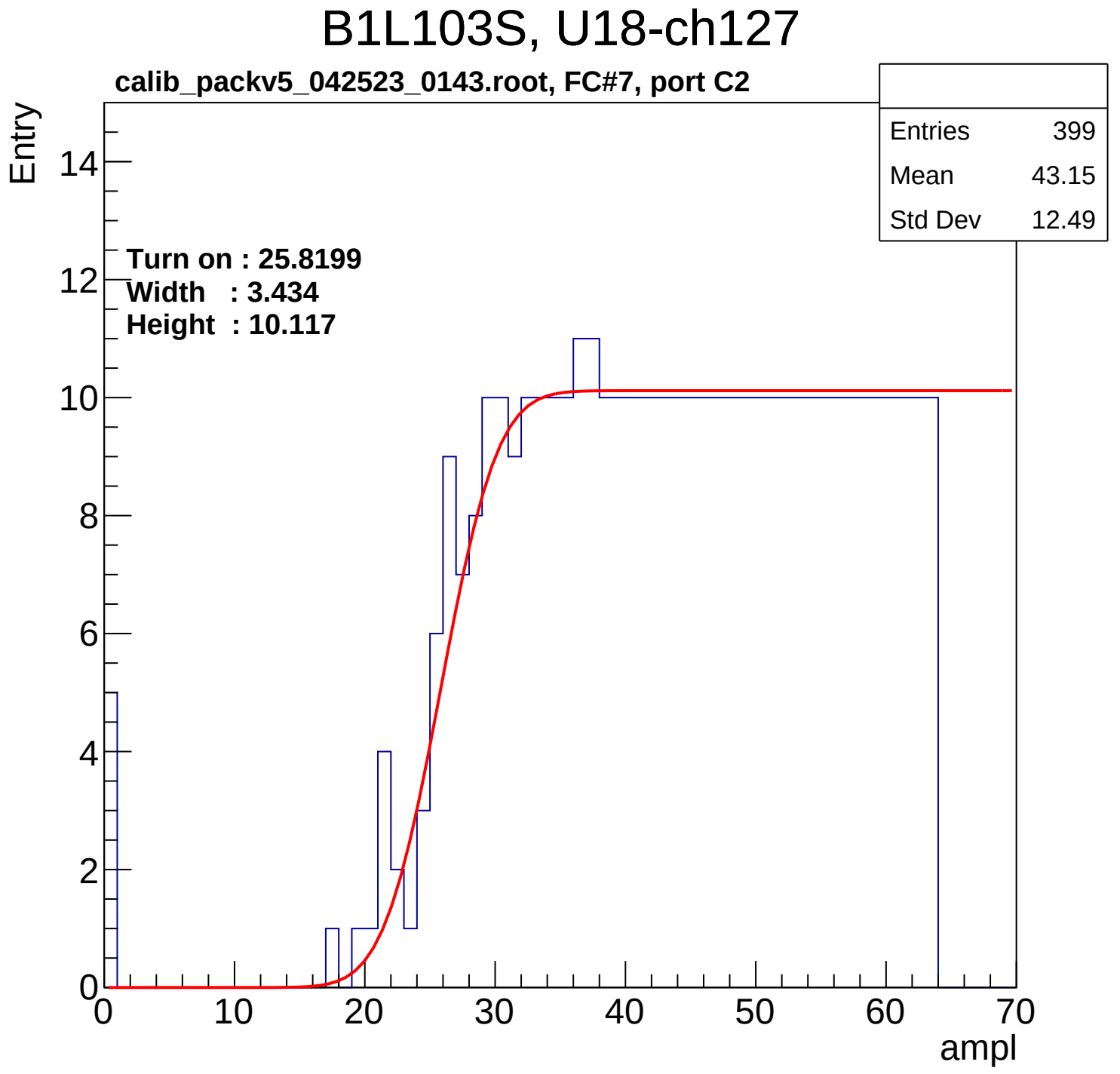
B1L103S, U18-ch127
calib_packv5_042523_0143.root, FC#7, port C2
Entries 399
Mean 43.15
Std Dev 12.49
Turn on : 25.8199
Width : 3.434
Height : 10.117
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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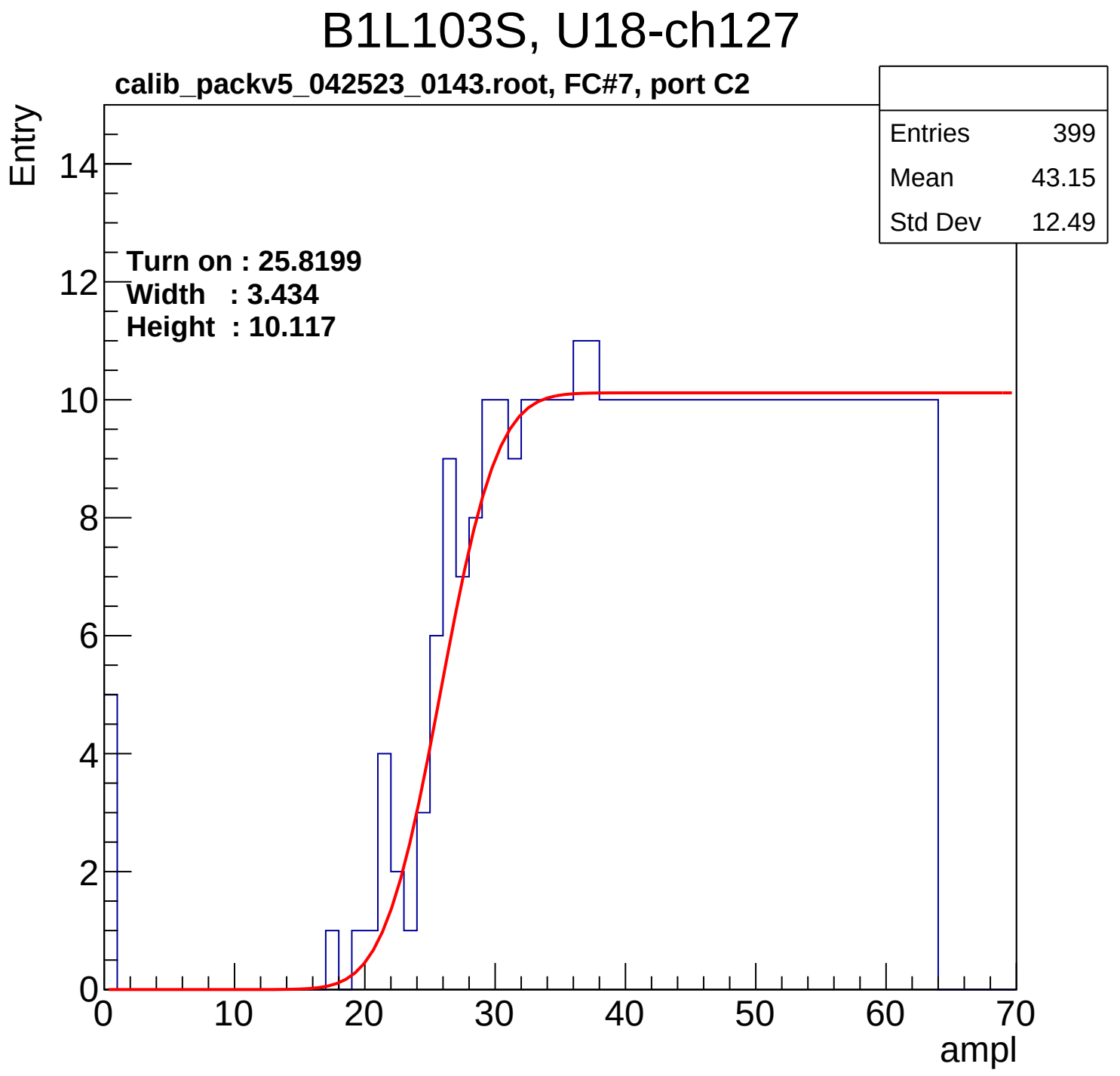
B1L103S, U18-ch127
calib_packv5_042523_0143.root, FC#7, port C2
Entries 399
Mean 43.15
Std Dev 12.49
Turn on : 25.8199
Width : 3.434
Height : 10.117
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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50
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