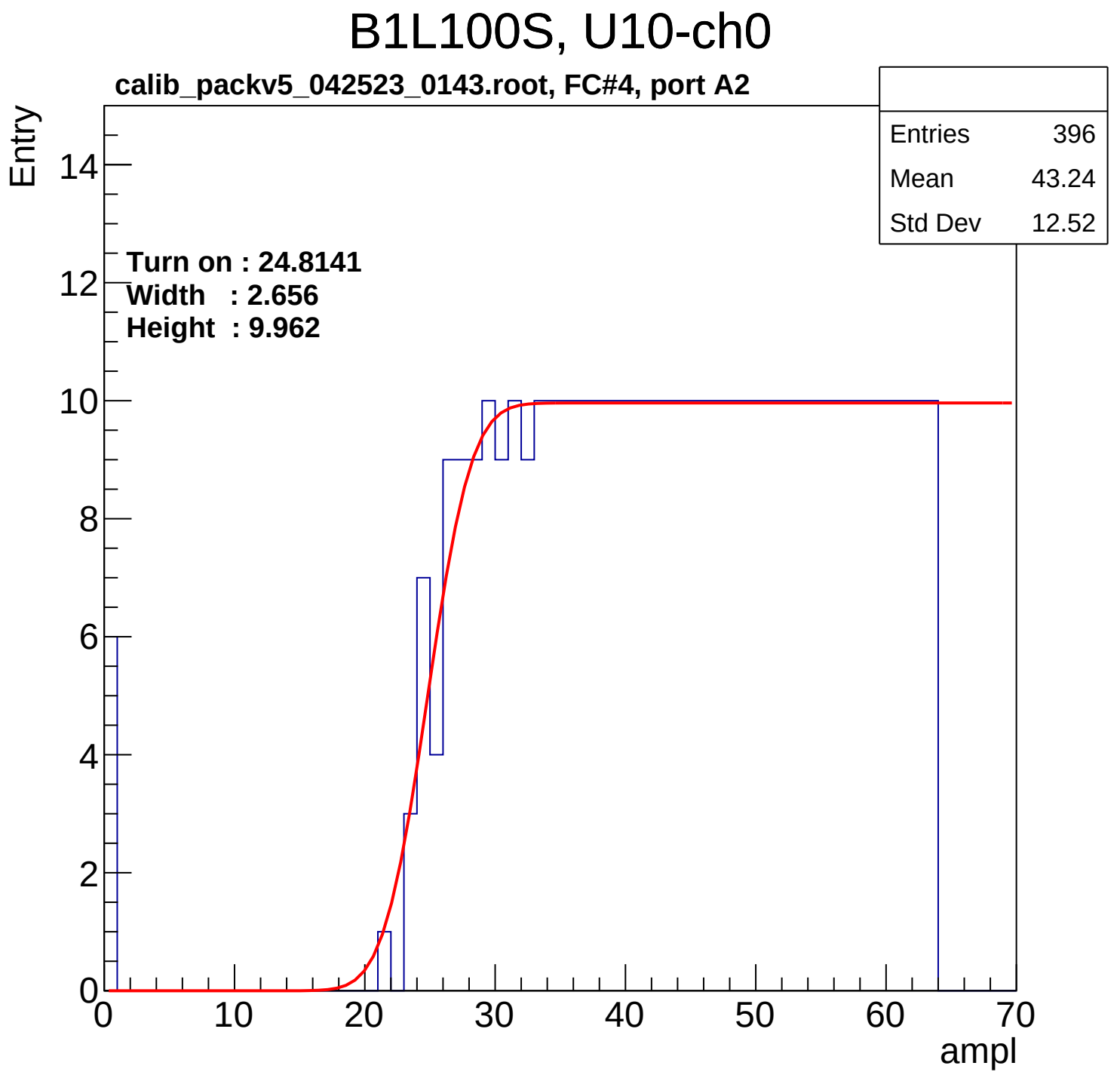
B1L100S, U10-ch0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 396
Mean 43.24
Std Dev 12.52
Turn on : 24.8141
Width : 2.656
Height : 9.962
Entry
ampl
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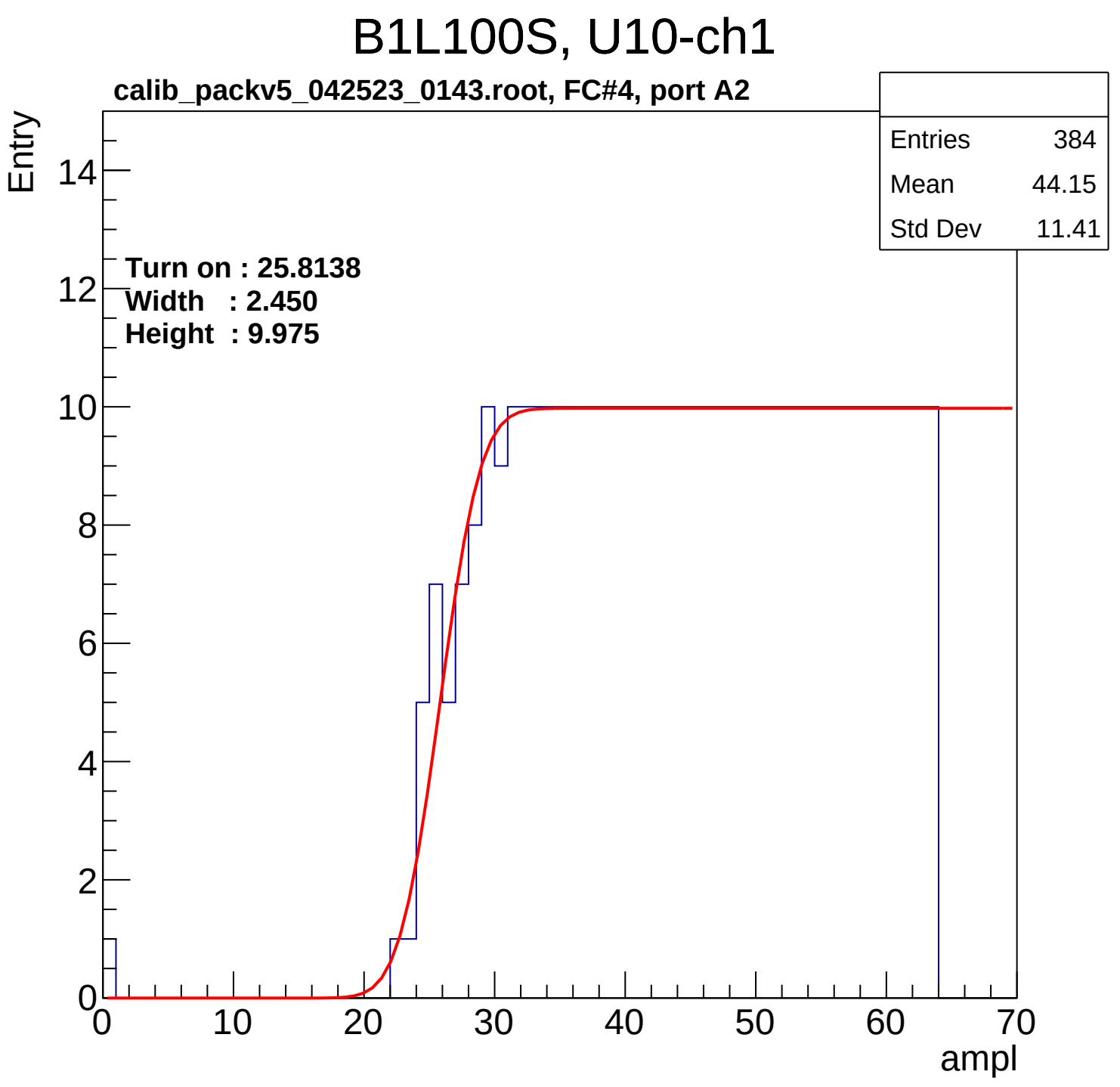
B1L100S, U10-ch1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 384
Mean 44.15
Std Dev 11.41
Turn on : 25.8138
Width : 2.450
Height : 9.975
Entry
ampl
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4
6
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0
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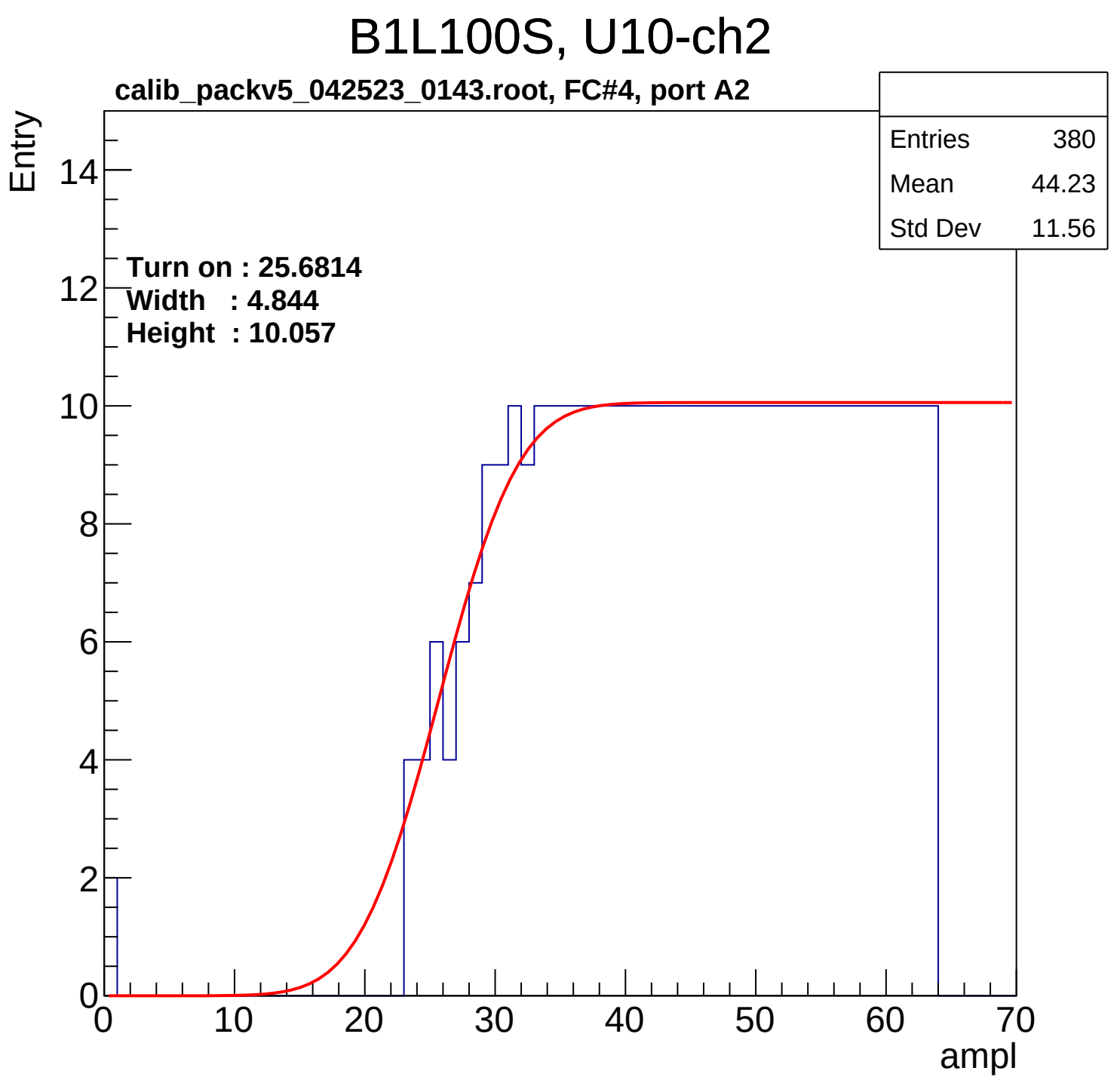
B1L100S, U10-ch2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 380
Mean 44.23
Std Dev 11.56
Turn on : 25.6814
Width : 4.844
Height : 10.057
Entry
ampl
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4
6
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0
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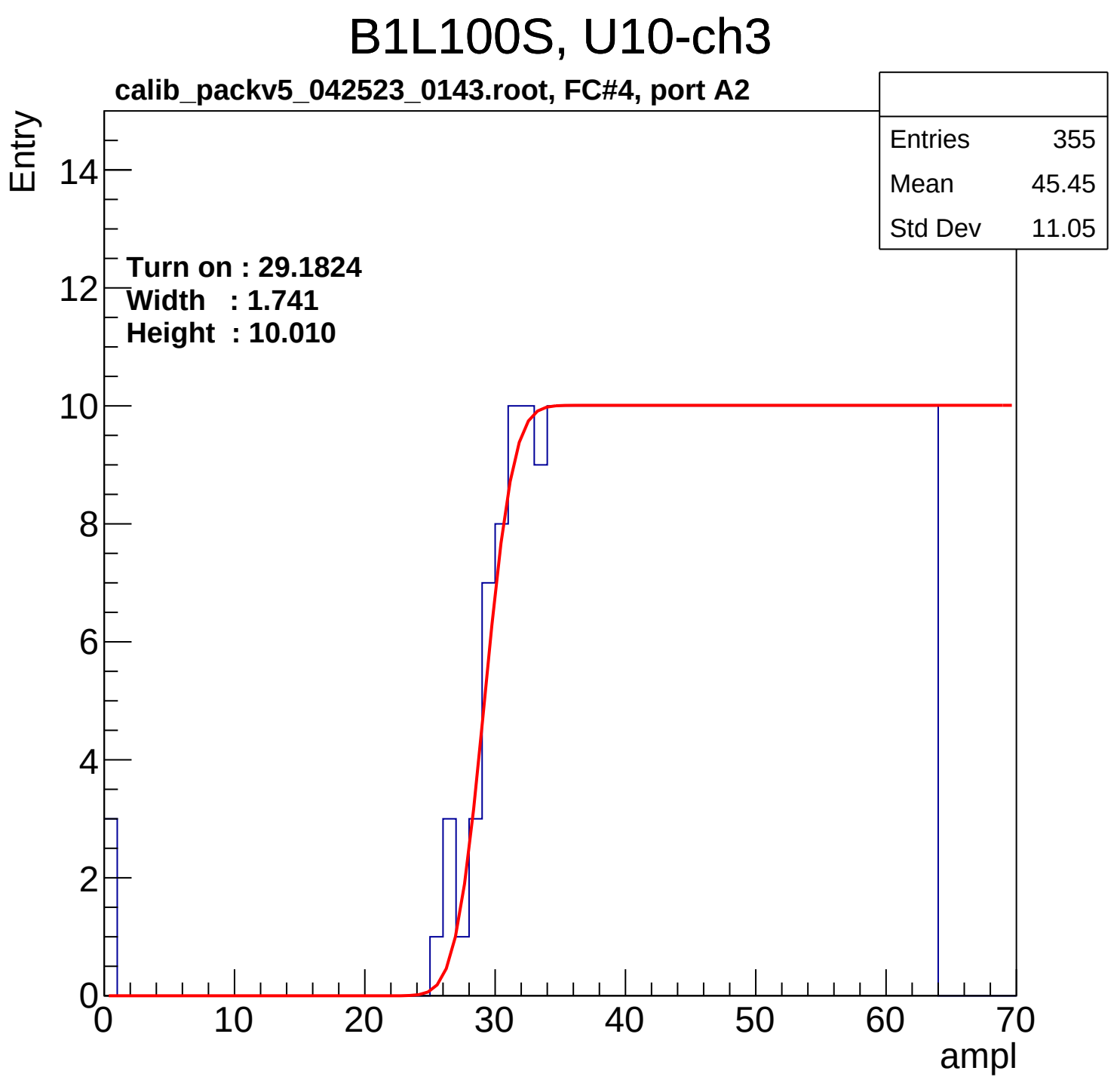
B1L100S, U10-ch3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 355
Mean 45.45
Std Dev 11.05
Turn on : 29.1824
Width : 1.741
Height : 10.010
Entry
ampl
0
2
4
6
8
10
12
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0
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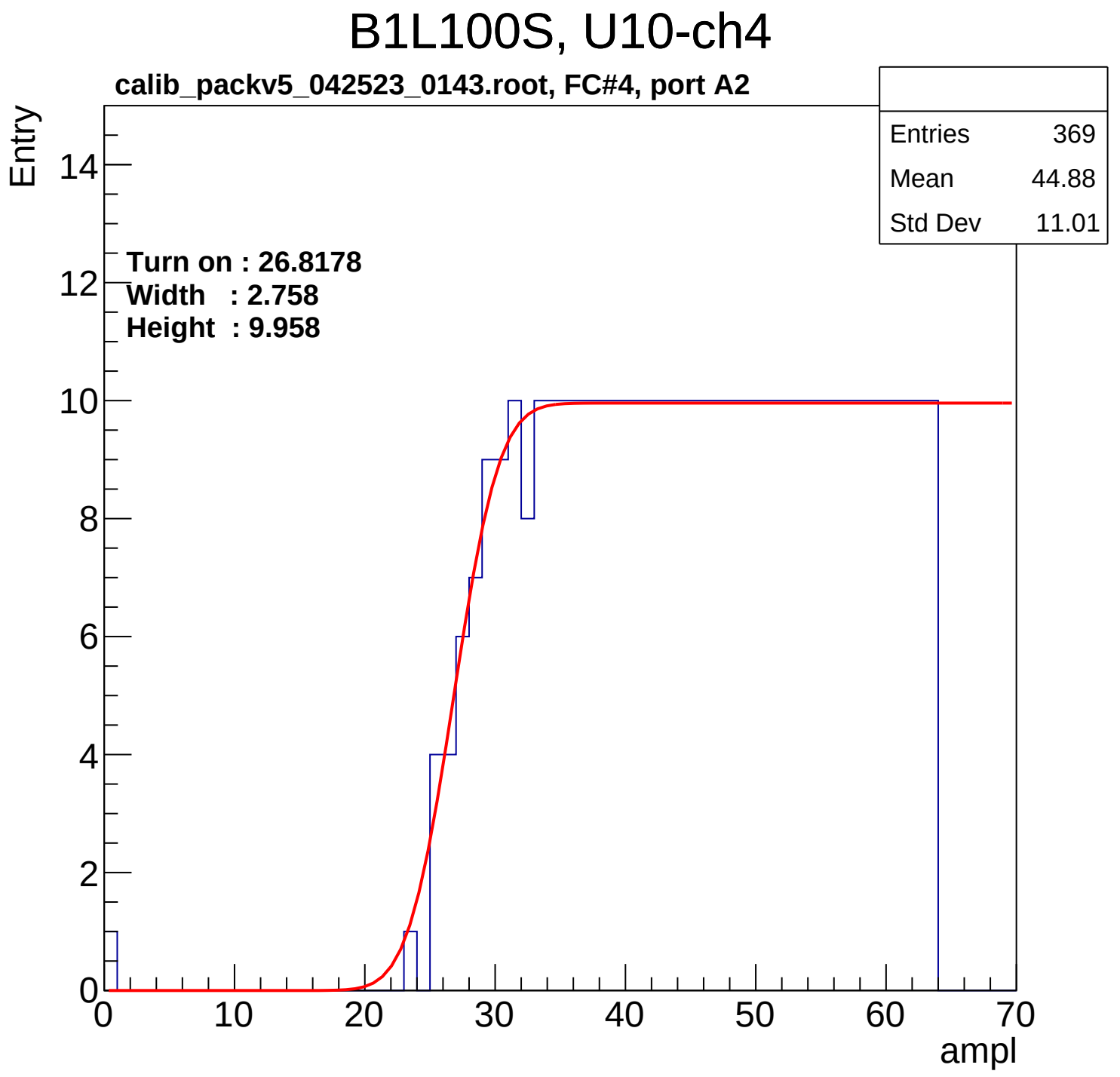
B1L100S, U10-ch4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 369
Mean 44.88
Std Dev 11.01
Turn on : 26.8178
Width : 2.758
Height : 9.958
Entry
ampl
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2
4
6
8
10
12
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0
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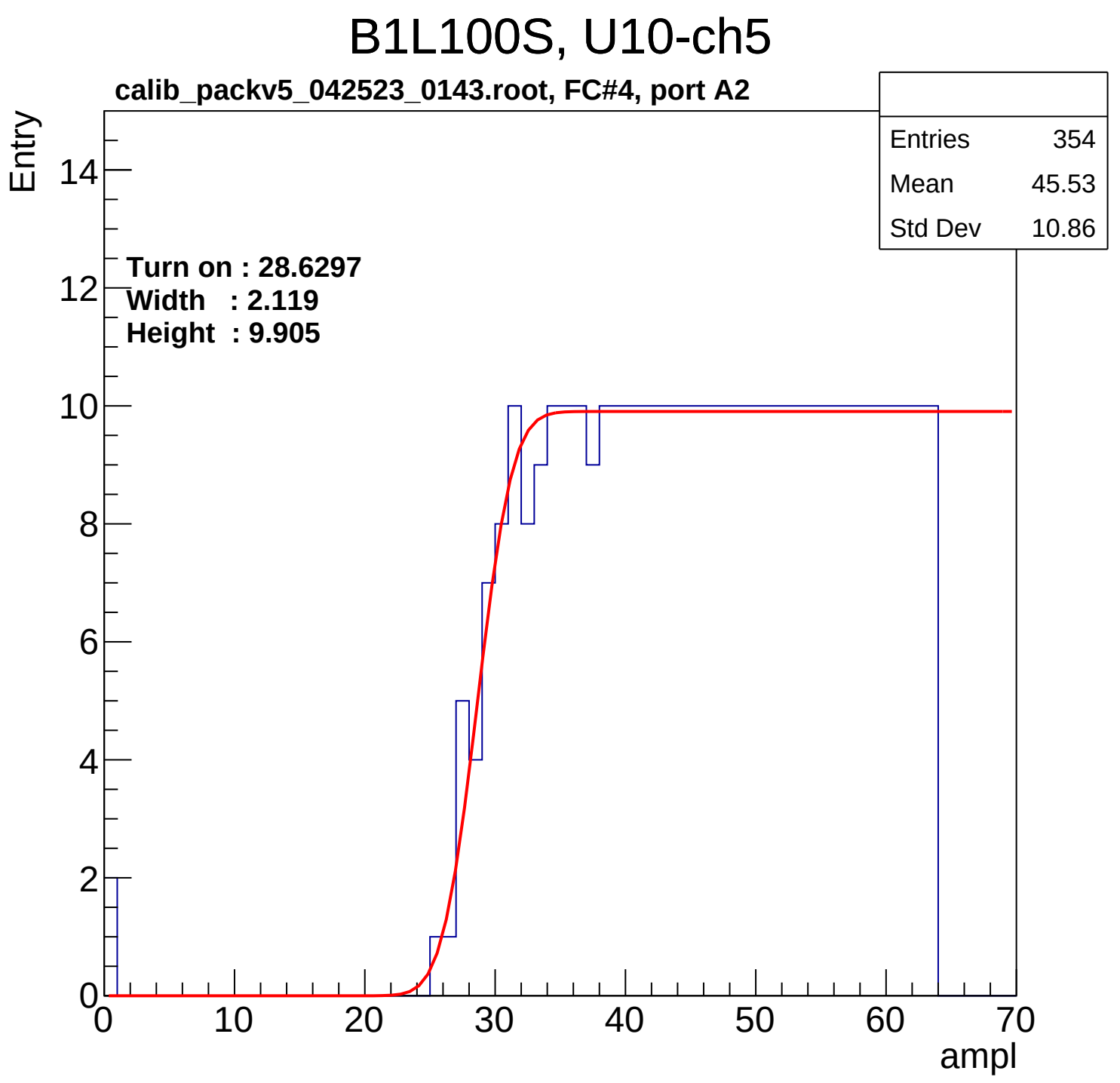
B1L100S, U10-ch5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 354
Mean 45.53
Std Dev 10.86
Turn on : 28.6297
Width : 2.119
Height : 9.905
Entry
ampl
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2
4
6
8
10
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0
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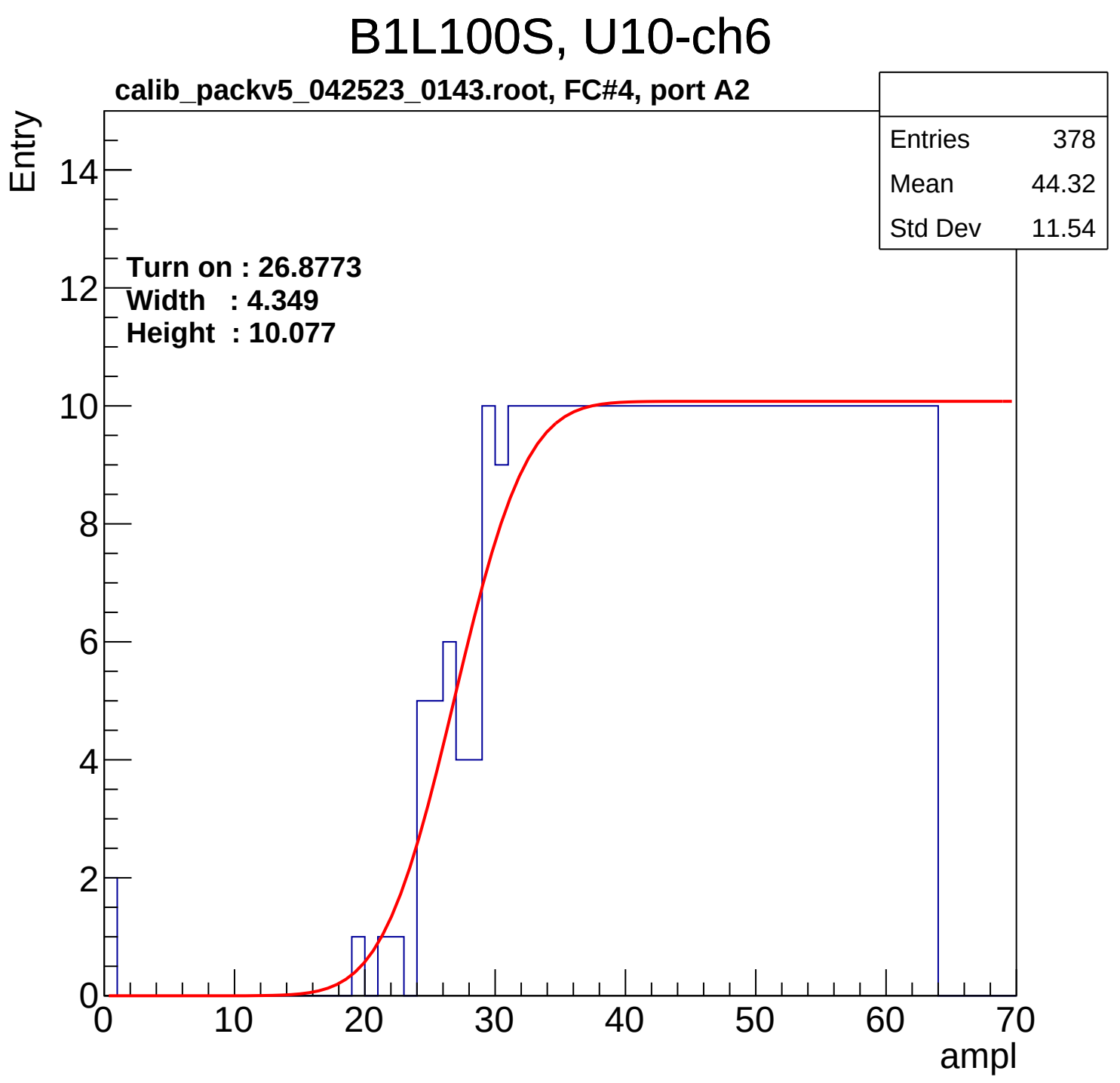
B1L100S, U10-ch6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 378
Mean 44.32
Std Dev 11.54
Turn on : 26.8773
Width : 4.349
Height : 10.077
Entry
ampl
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2
4
6
8
10
12
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0
10
20
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40
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60
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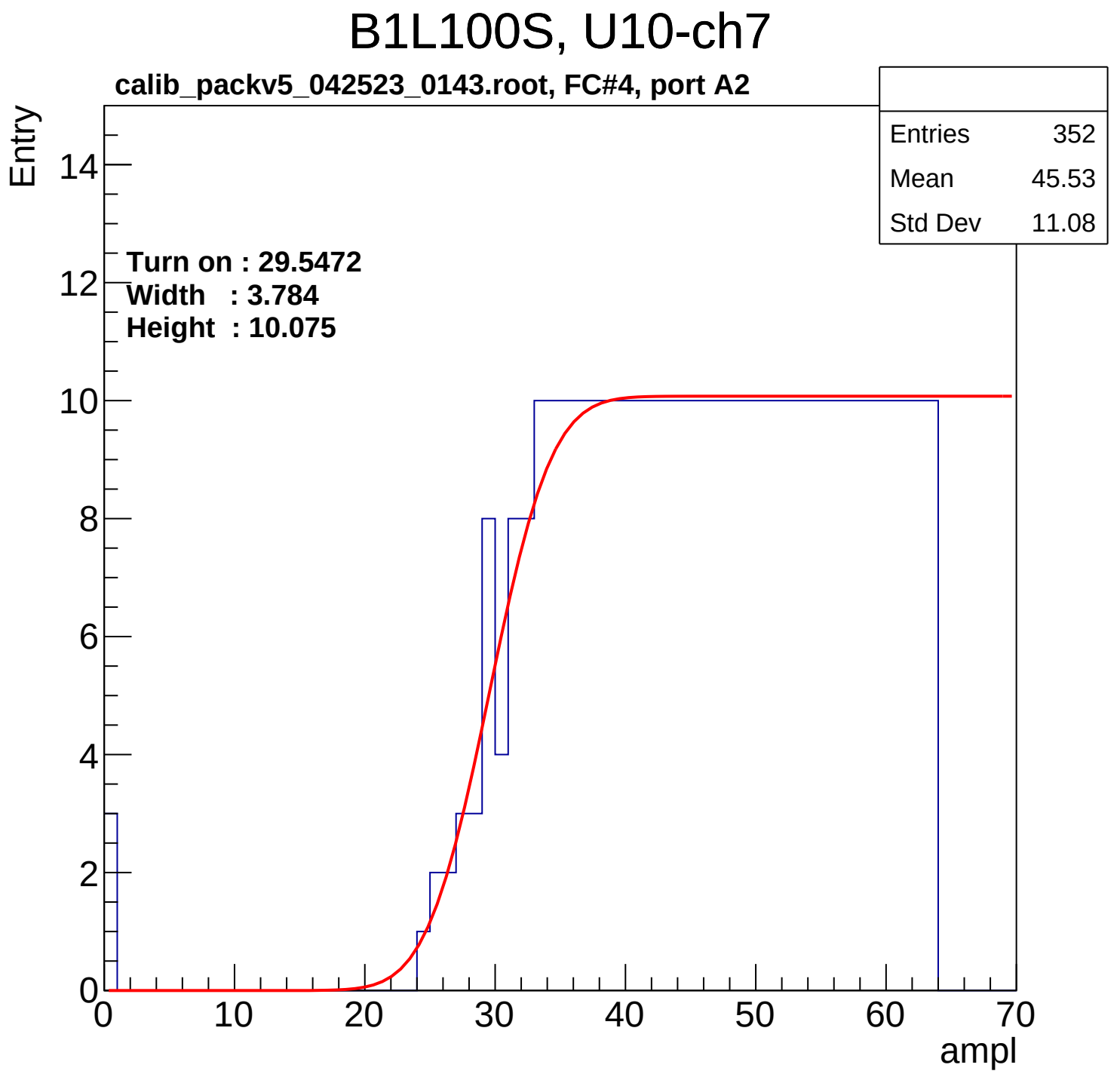
B1L100S, U10-ch7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 352
Mean 45.53
Std Dev 11.08
Turn on : 29.5472
Width : 3.784
Height : 10.075
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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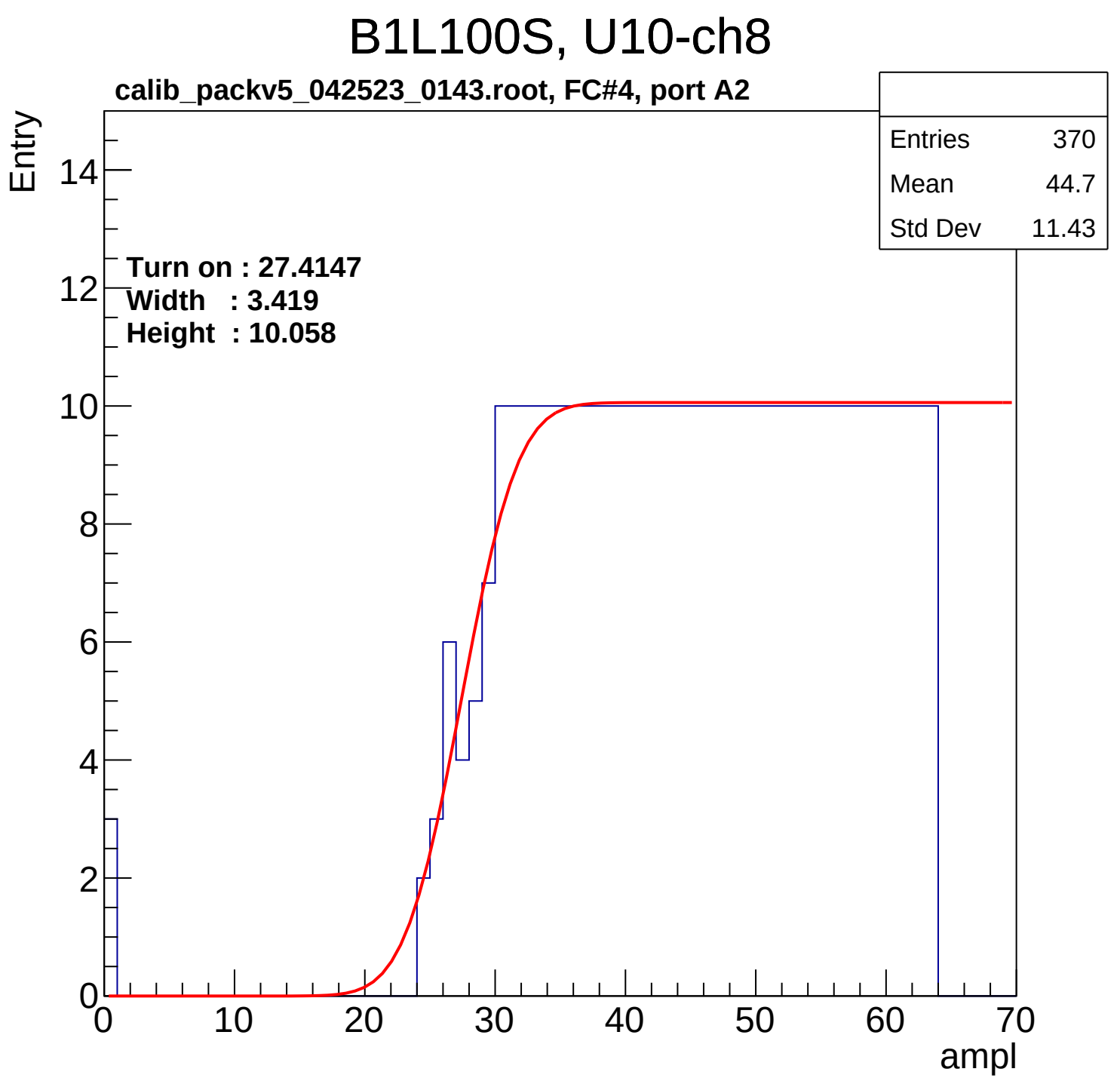
B1L100S, U10-ch8
calib_packv5_042523_0143.root, FC#4, port A2
Entries 370
Mean 44.7
Std Dev 11.43
Turn on : 27.4147
Width : 3.419
Height : 10.058
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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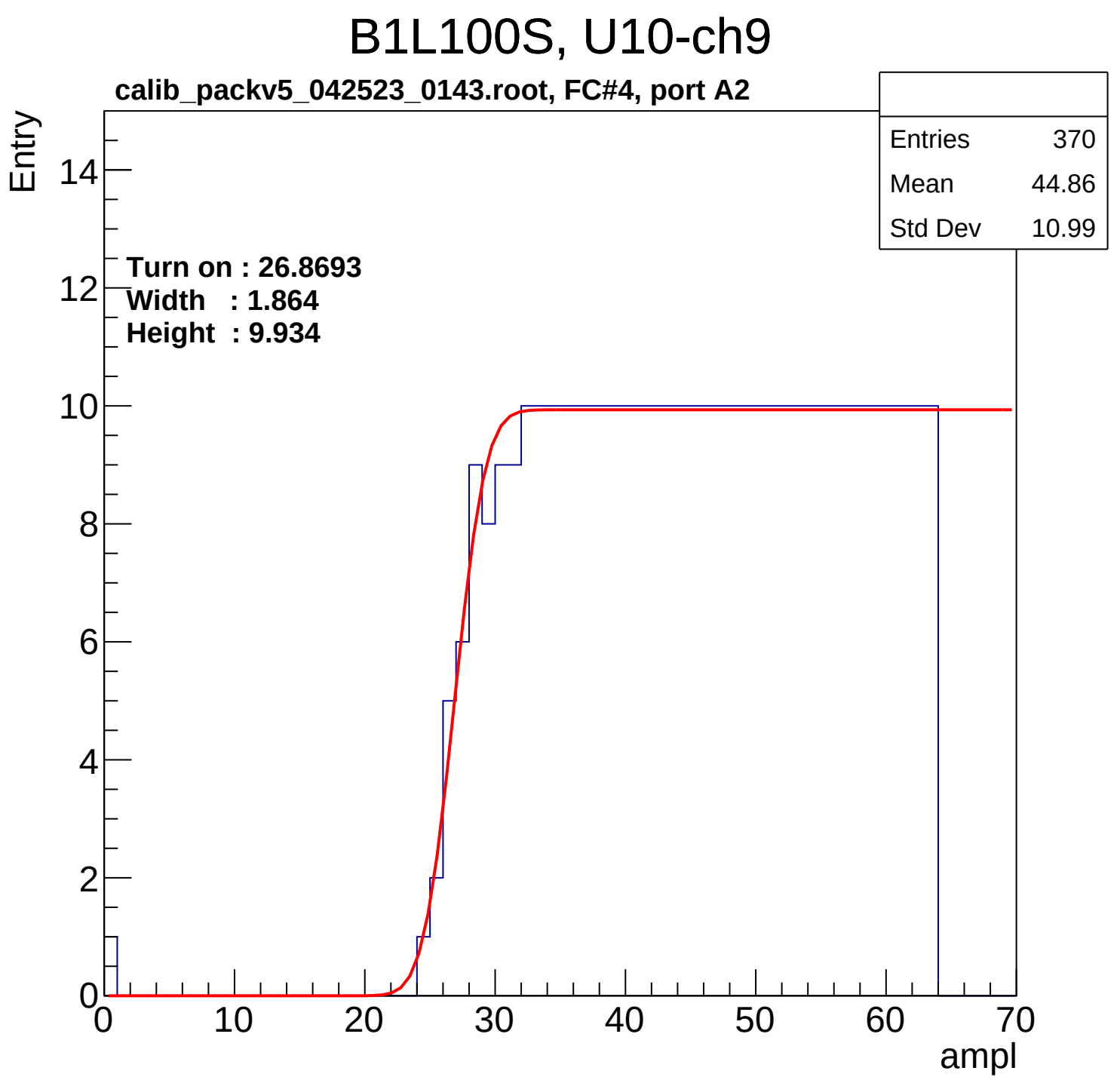
B1L100S, U10-ch9
calib_packv5_042523_0143.root, FC#4, port A2
Entries 370
Mean 44.86
Std Dev 10.99
Turn on : 26.8693
Width : 1.864
Height : 9.934
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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60
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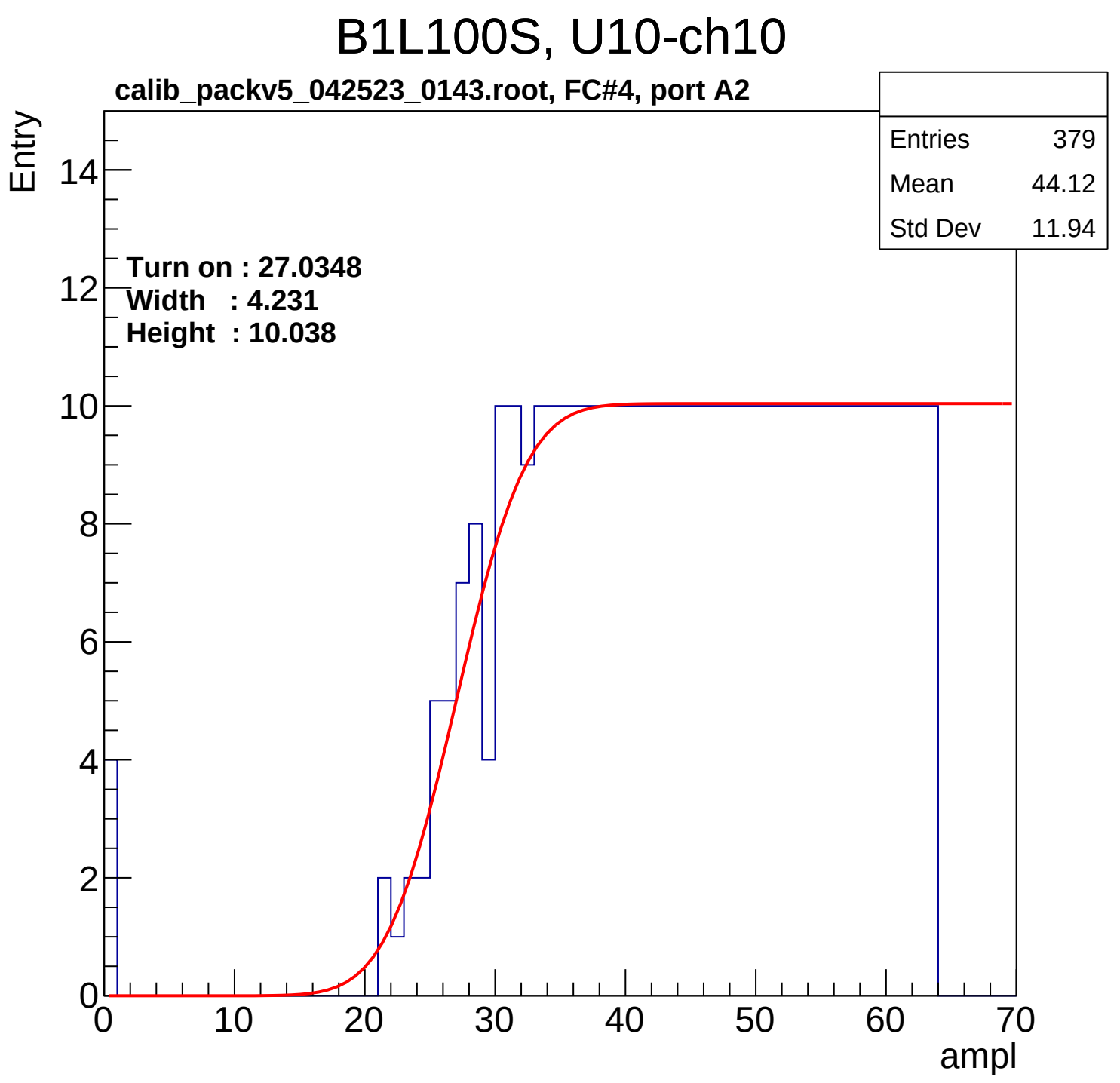
B1L100S, U10-ch10
calib_packv5_042523_0143.root, FC#4, port A2
Entries 379
Mean 44.12
Std Dev 11.94
Turn on : 27.0348
Width : 4.231
Height : 10.038
Entry
ampl
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2
4
6
8
10
12
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0
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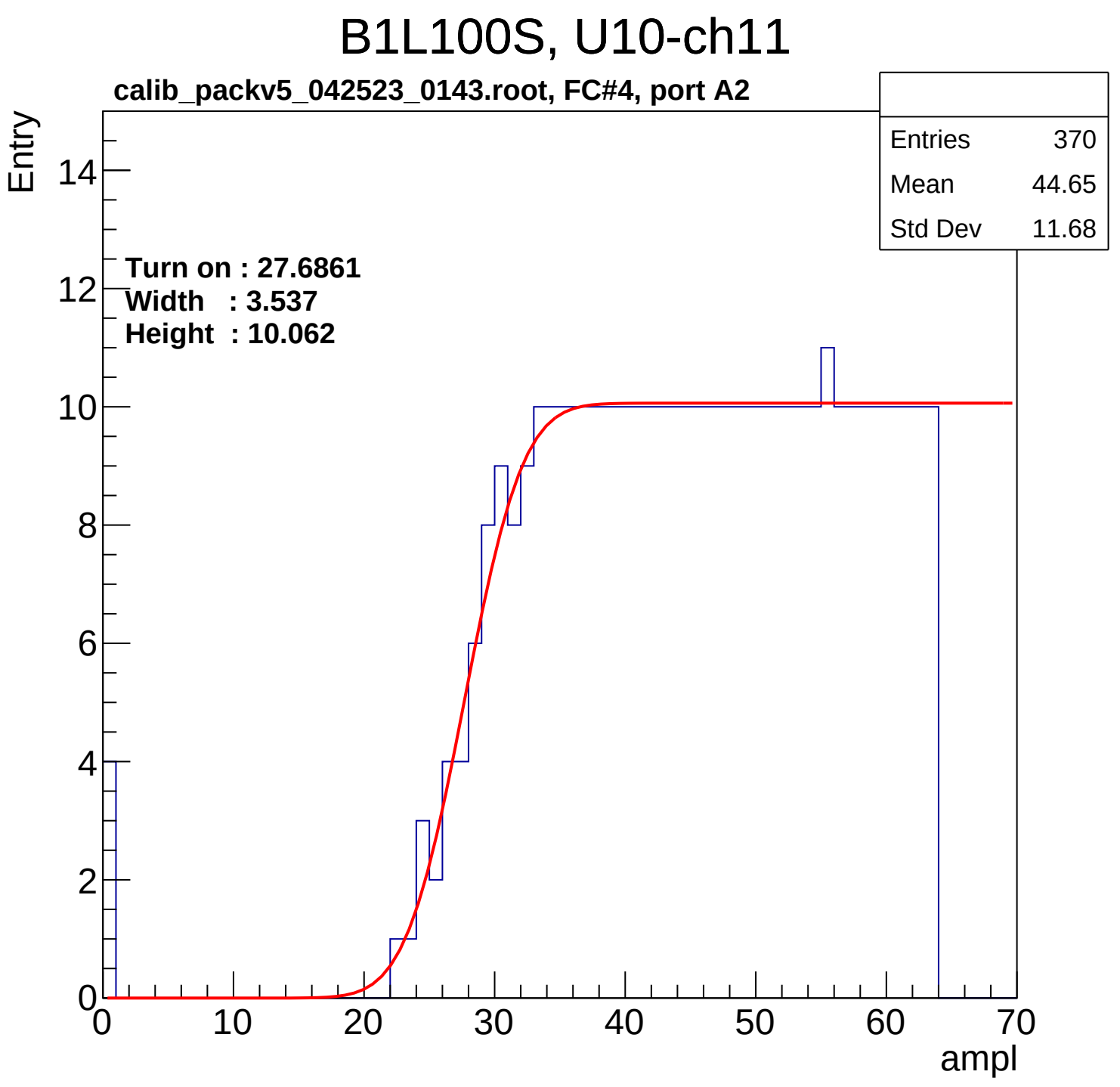
B1L100S, U10-ch11
calib_packv5_042523_0143.root, FC#4, port A2
Entries 370
Mean 44.65
Std Dev 11.68
Turn on : 27.6861
Width : 3.537
Height : 10.062
Entry
ampl
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4
6
8
10
12
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0
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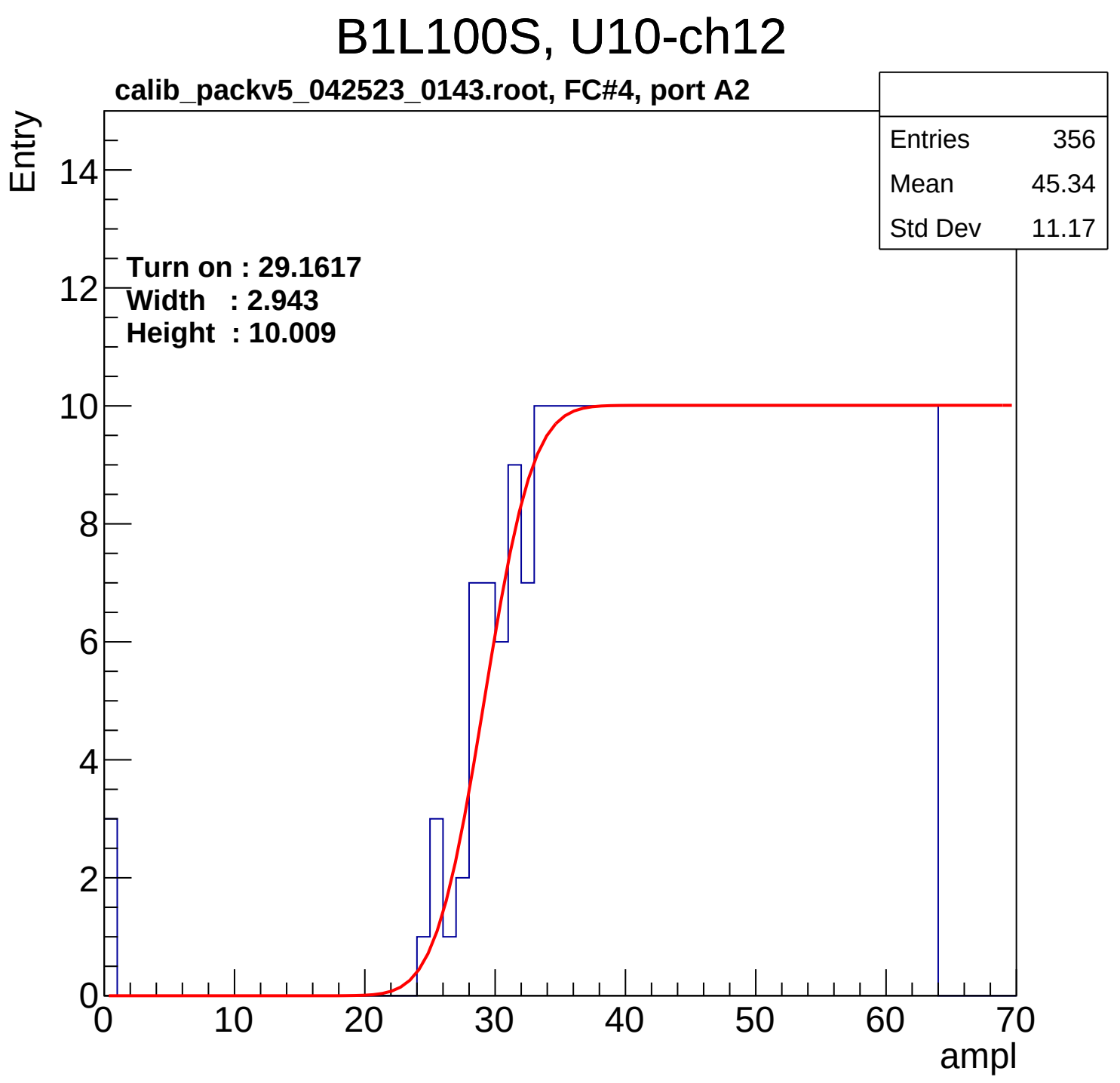
B1L100S, U10-ch12
calib_packv5_042523_0143.root, FC#4, port A2
Entries 356
Mean 45.34
Std Dev 11.17
Turn on : 29.1617
Width : 2.943
Height : 10.009
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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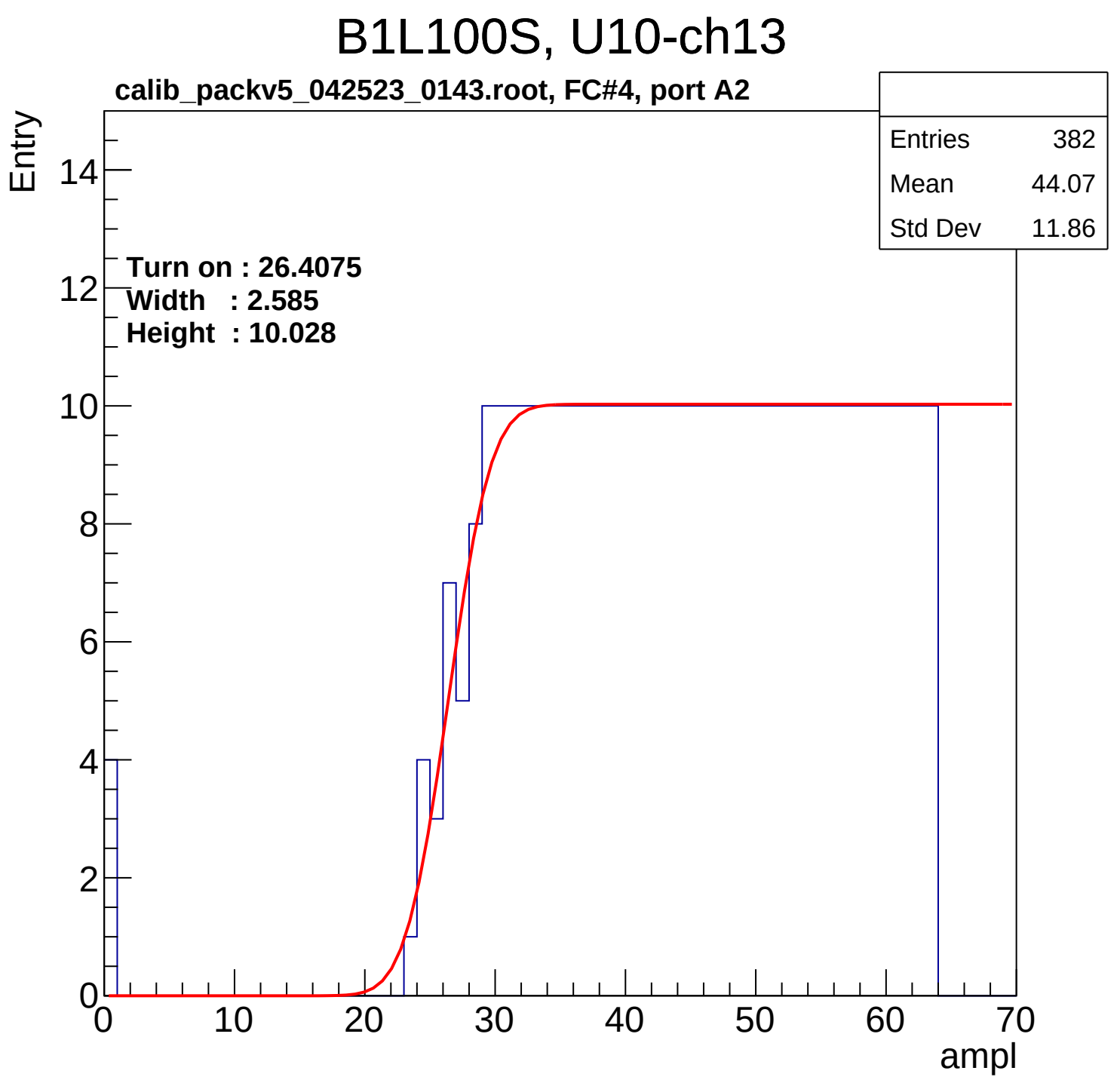
B1L100S, U10-ch13
calib_packv5_042523_0143.root, FC#4, port A2
Entries 382
Mean 44.07
Std Dev 11.86
Turn on : 26.4075
Width : 2.585
Height : 10.028
Entry
ampl
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2
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6
8
10
12
14
0
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60
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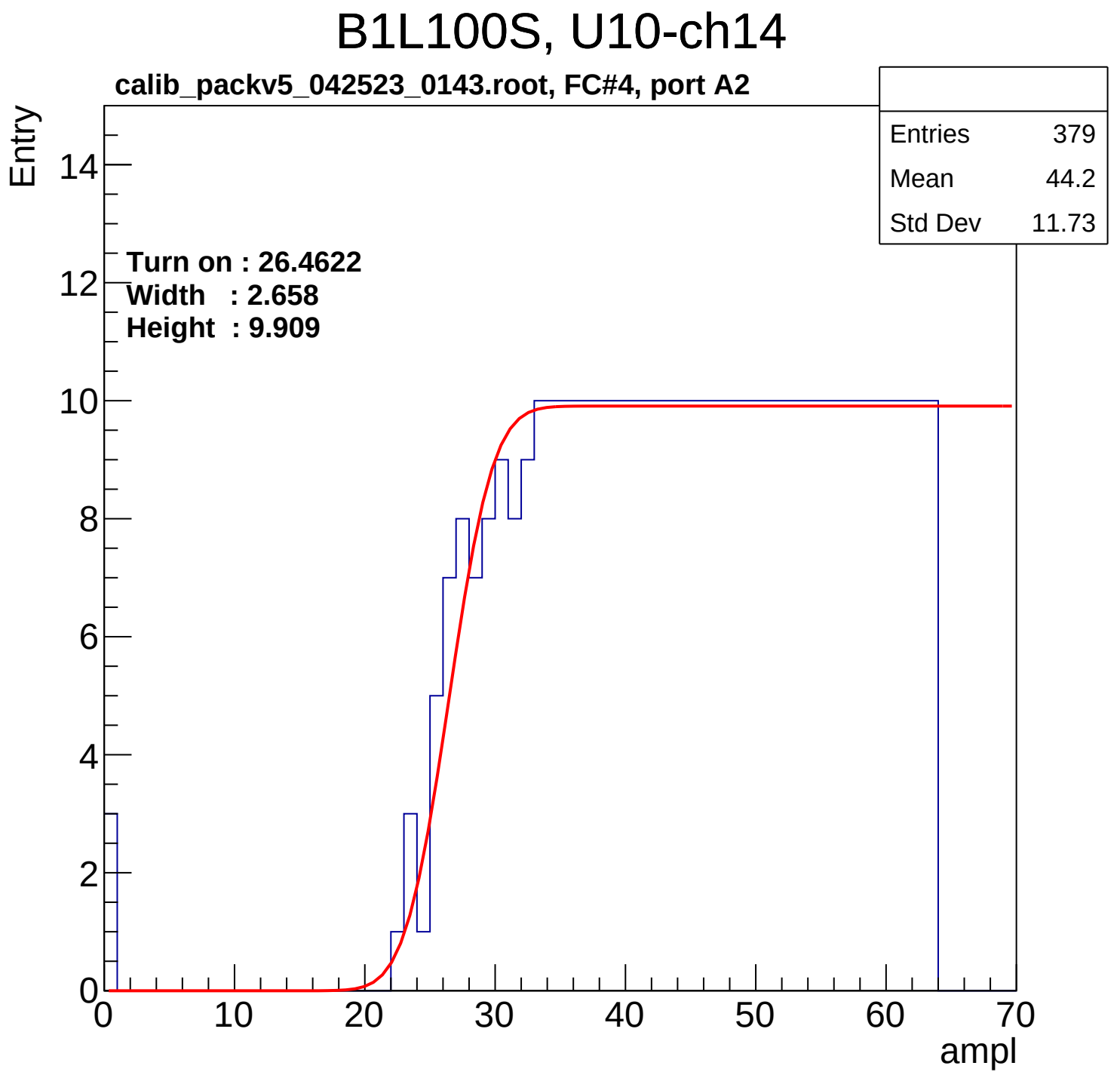
B1L100S, U10-ch14
calib_packv5_042523_0143.root, FC#4, port A2
Entries 379
Mean 44.2
Std Dev 11.73
Turn on : 26.4622
Width : 2.658
Height : 9.909
Entry
ampl
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6
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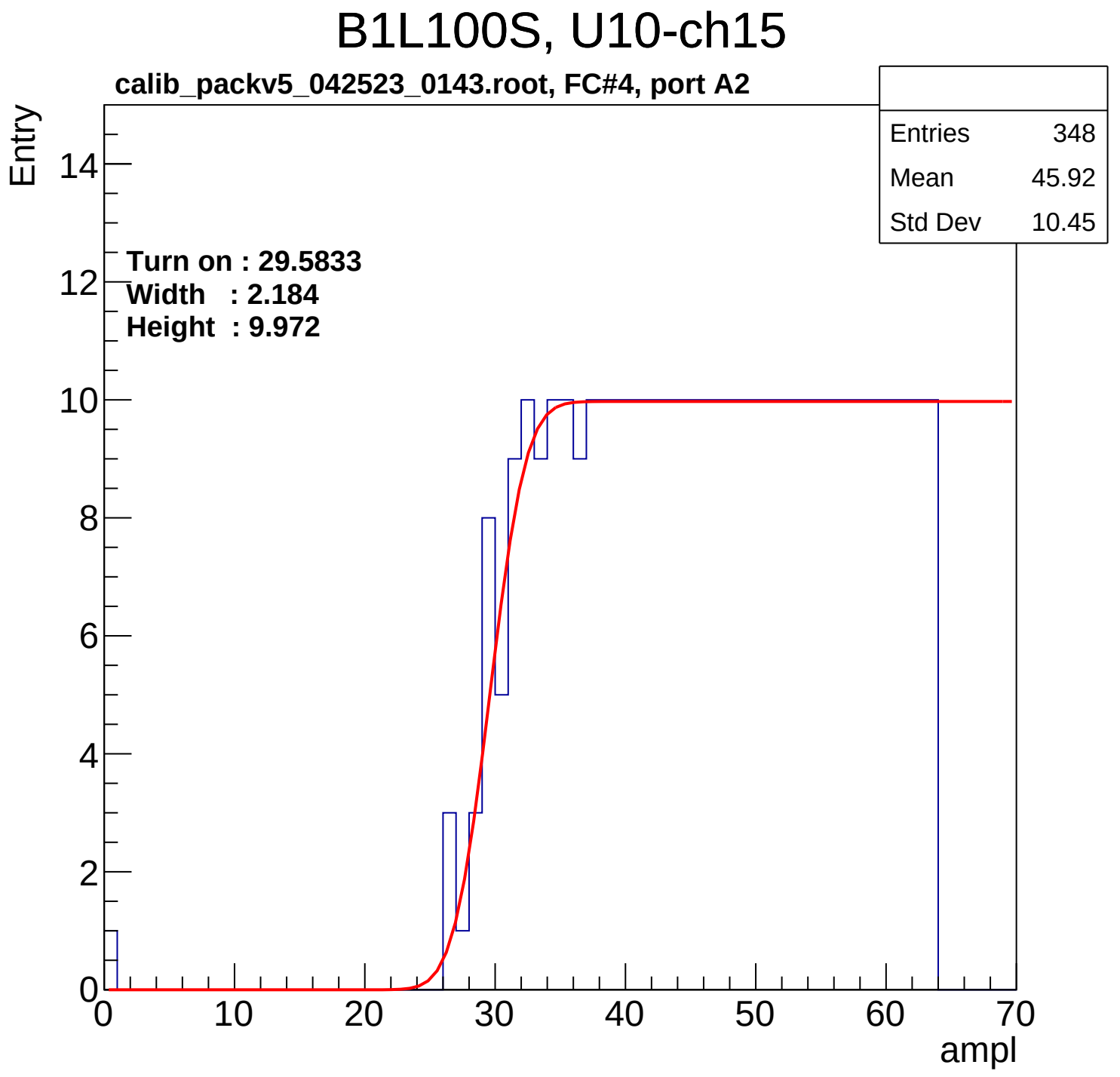
B1L100S, U10-ch15
calib_packv5_042523_0143.root, FC#4, port A2
Entries 348
Mean 45.92
Std Dev 10.45
Turn on : 29.5833
Width : 2.184
Height : 9.972
Entry
ampl
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8
10
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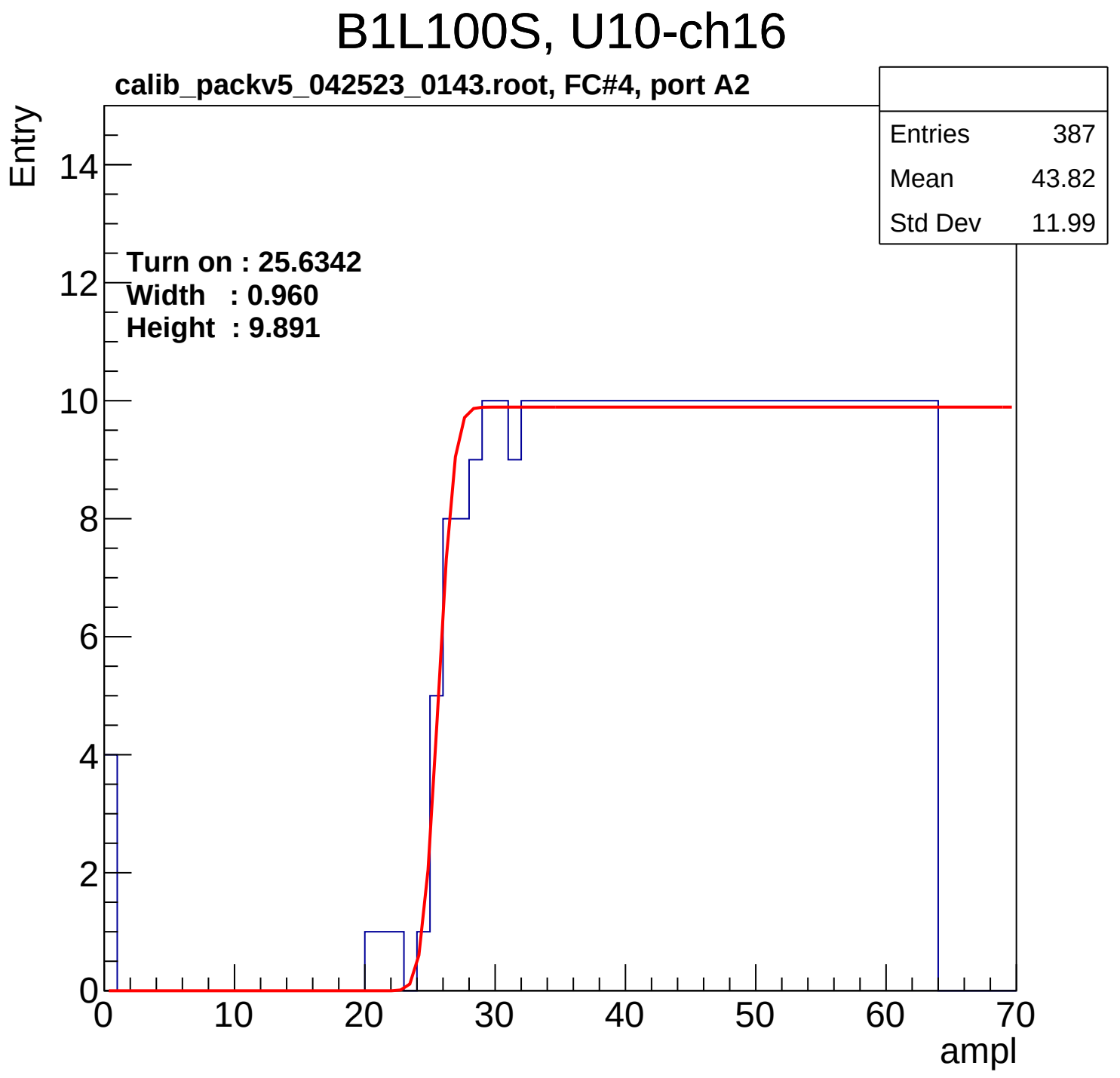
B1L100S, U10-ch16
calib_packv5_042523_0143.root, FC#4, port A2
Entries 387
Mean 43.82
Std Dev 11.99
Turn on : 25.6342
Width : 0.960
Height : 9.891
Entry
ampl
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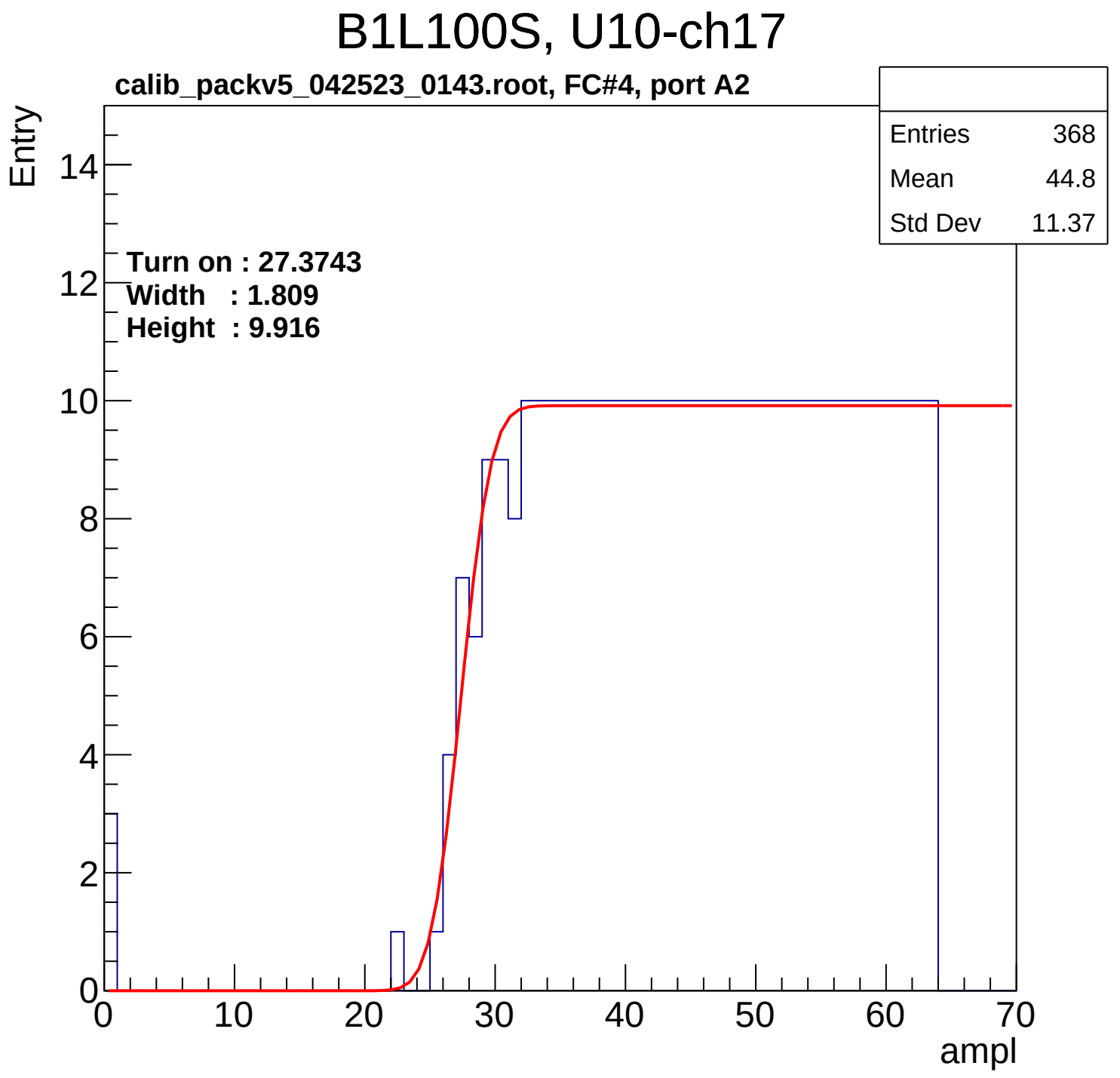
B1L100S, U10-ch17
calib_packv5_042523_0143.root, FC#4, port A2
Entries 368
Mean 44.8
Std Dev 11.37
Turn on : 27.3743
Width : 1.809
Height : 9.916
Entry
ampl
0
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8
10
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0
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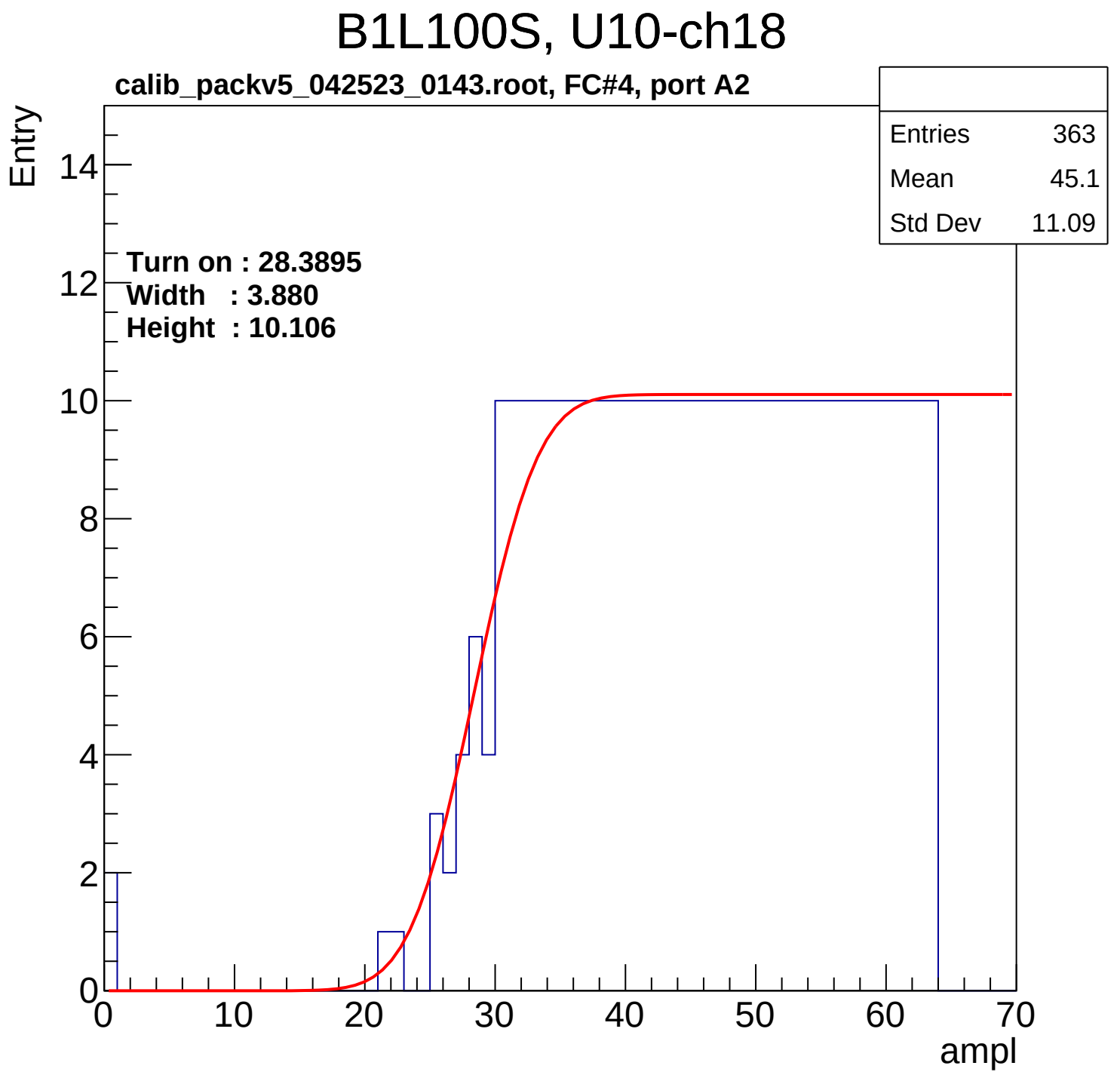
B1L100S, U10-ch18
calib_packv5_042523_0143.root, FC#4, port A2
Entries 363
Mean 45.1
Std Dev 11.09
Turn on : 28.3895
Width : 3.880
Height : 10.106
Entry
ampl
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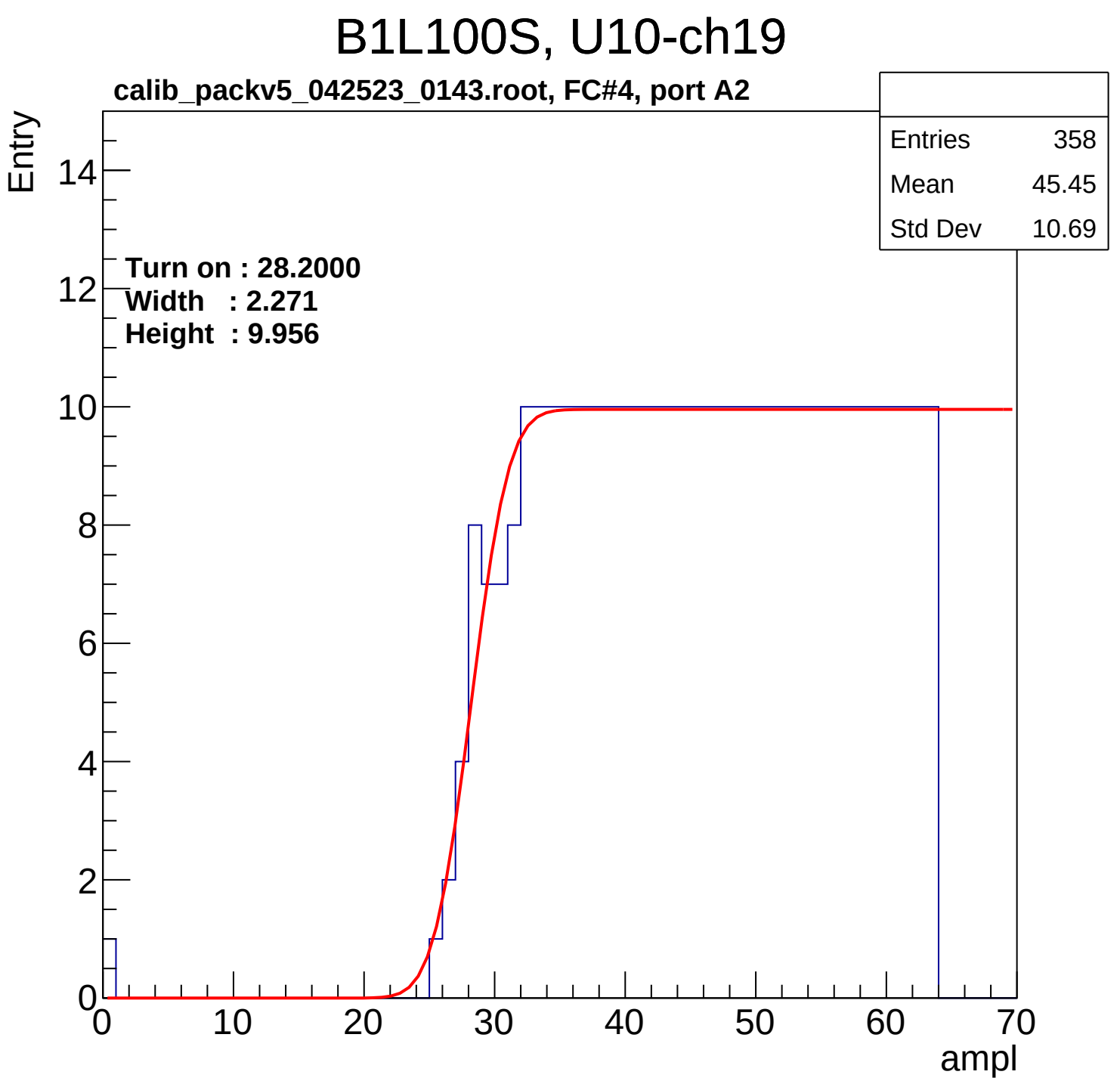
B1L100S, U10-ch19
calib_packv5_042523_0143.root, FC#4, port A2
Entries 358
Mean 45.45
Std Dev 10.69
Turn on : 28.2000
Width : 2.271
Height : 9.956
Entry
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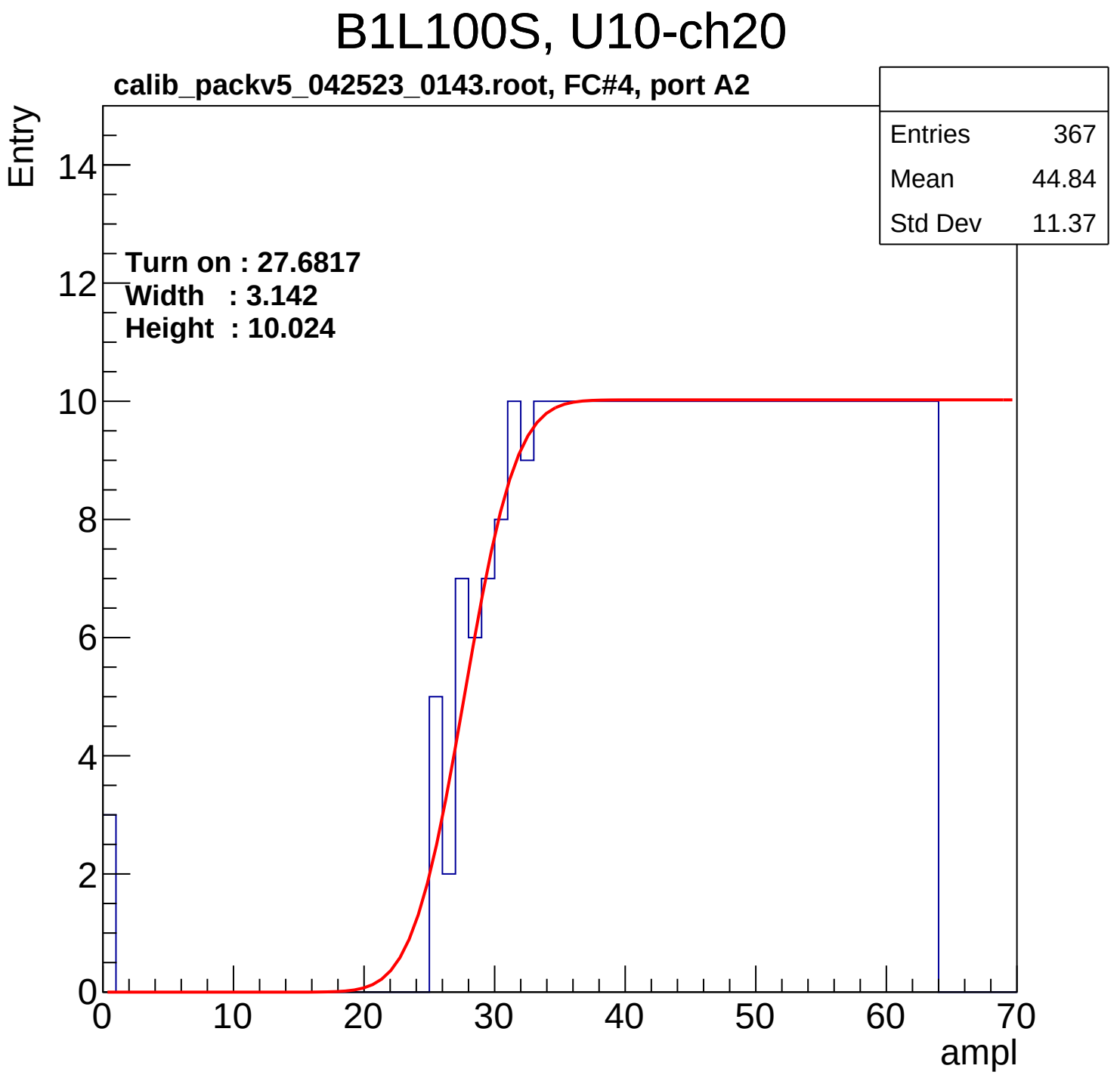
B1L100S, U10-ch20
calib_packv5_042523_0143.root, FC#4, port A2
Entries 367
Mean 44.84
Std Dev 11.37
Turn on : 27.6817
Width : 3.142
Height : 10.024
Entry
ampl
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2
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6
8
10
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0
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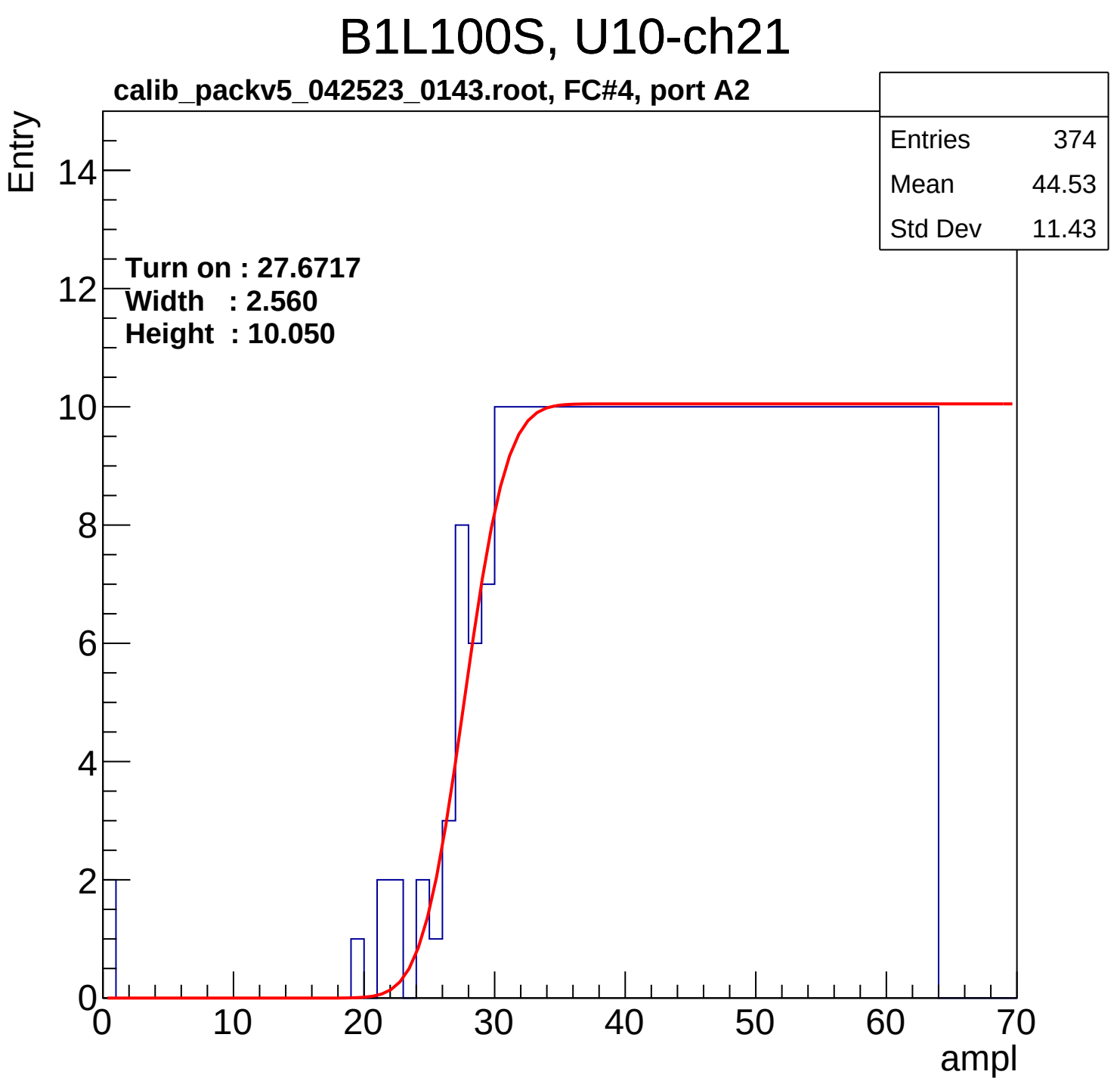
B1L100S, U10-ch21
calib_packv5_042523_0143.root, FC#4, port A2
Entries 374
Mean 44.53
Std Dev 11.43
Turn on : 27.6717
Width : 2.560
Height : 10.050
Entry
ampl
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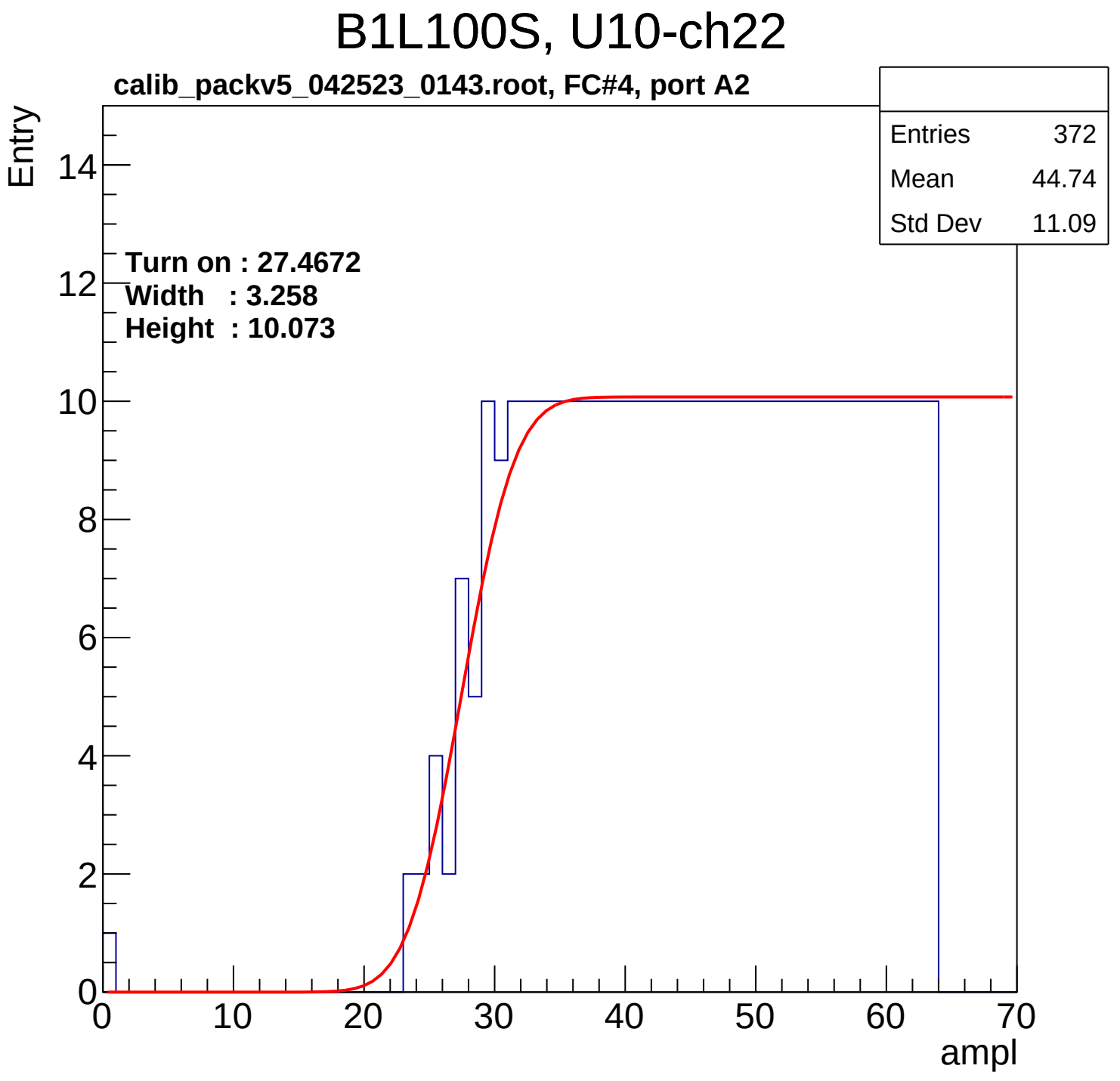
B1L100S, U10-ch22
calib_packv5_042523_0143.root, FC#4, port A2
Entries 372
Mean 44.74
Std Dev 11.09
Turn on : 27.4672
Width : 3.258
Height : 10.073
Entry
ampl
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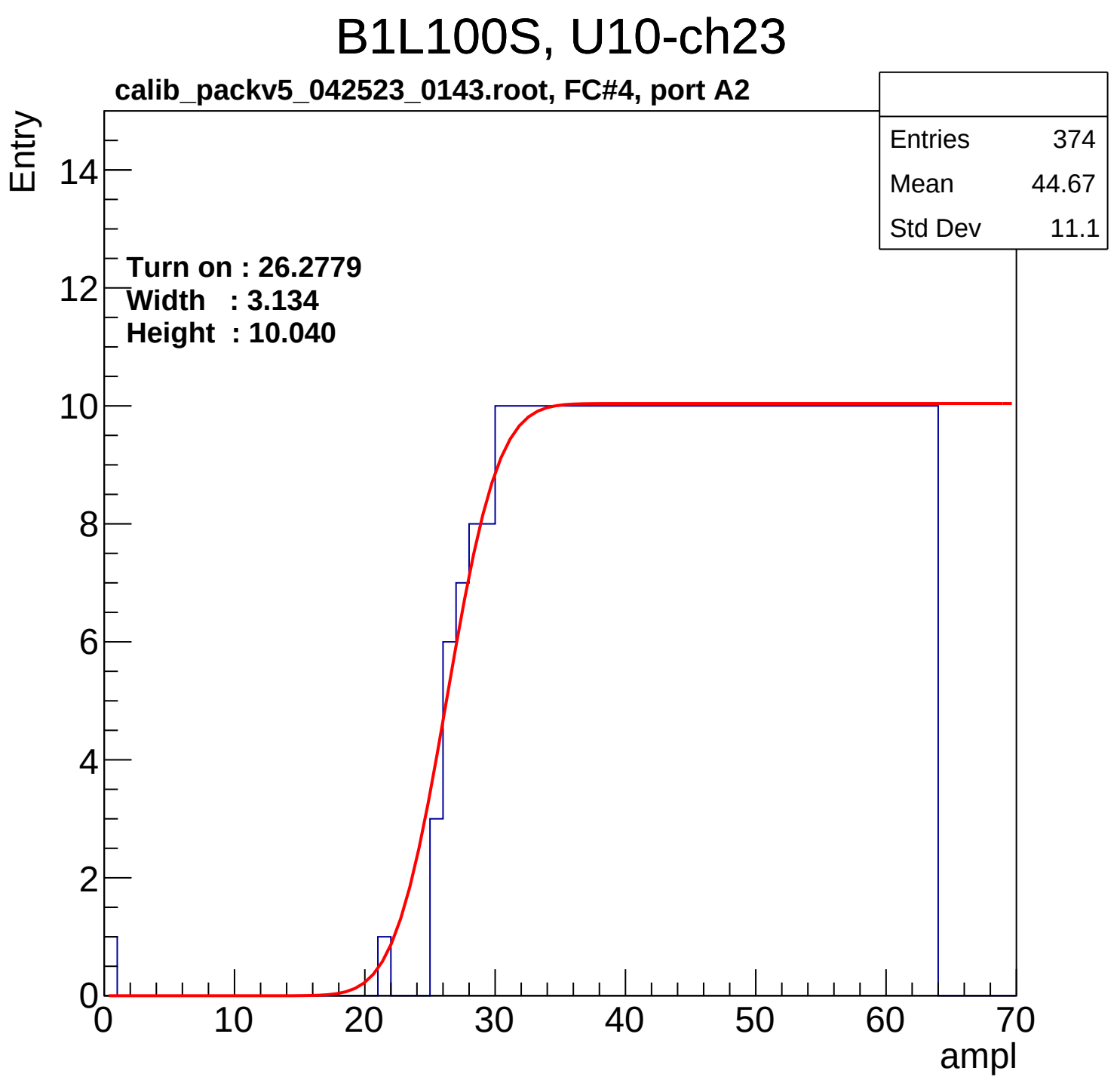
B1L100S, U10-ch23
calib_packv5_042523_0143.root, FC#4, port A2
Entries 374
Mean 44.67
Std Dev 11.1
Turn on : 26.2779
Width : 3.134
Height : 10.040
Entry
ampl
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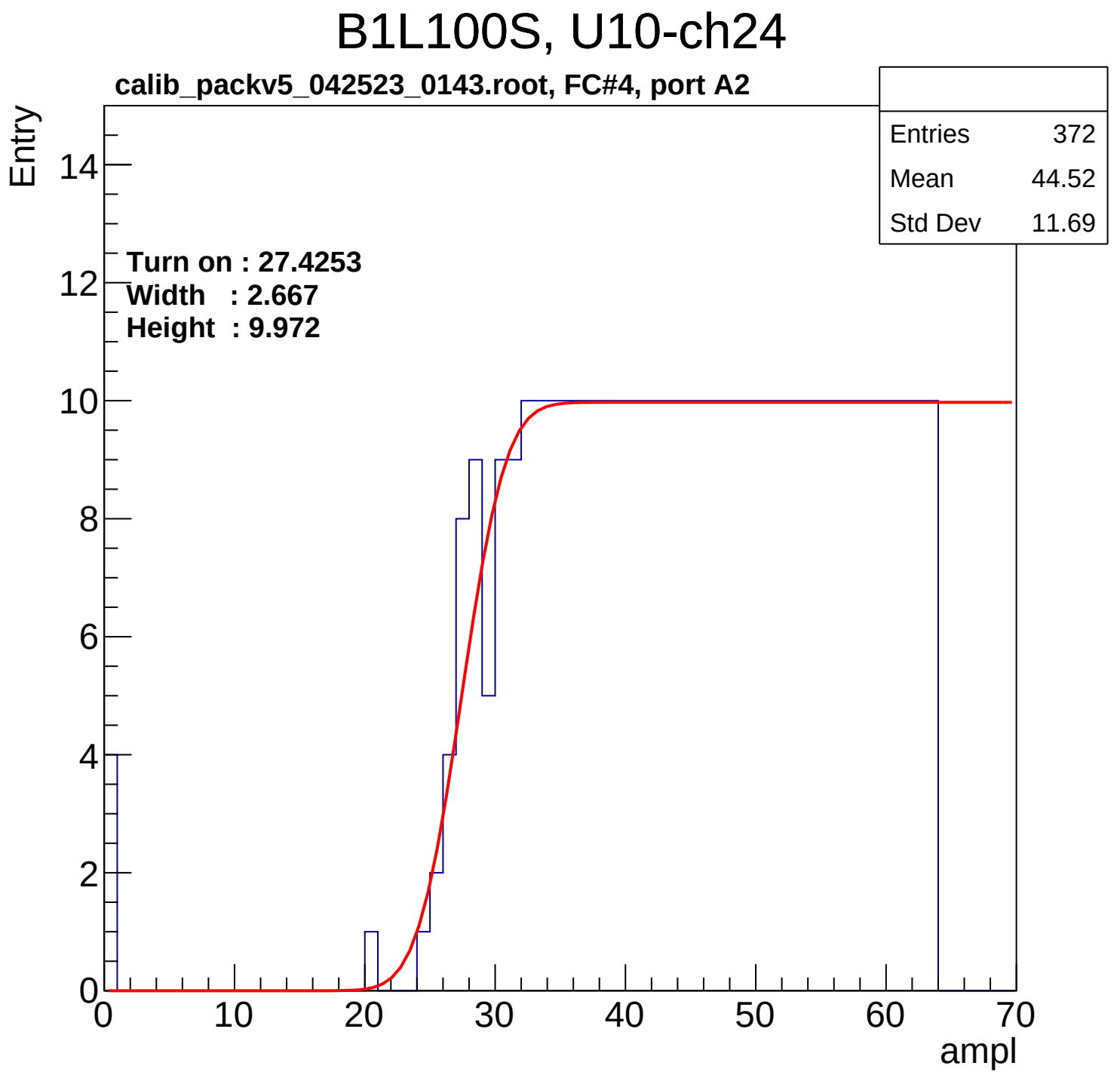
B1L100S, U10-ch24
calib_packv5_042523_0143.root, FC#4, port A2
Entries 372
Mean 44.52
Std Dev 11.69
Turn on : 27.4253
Width : 2.667
Height : 9.972
Entry
ampl
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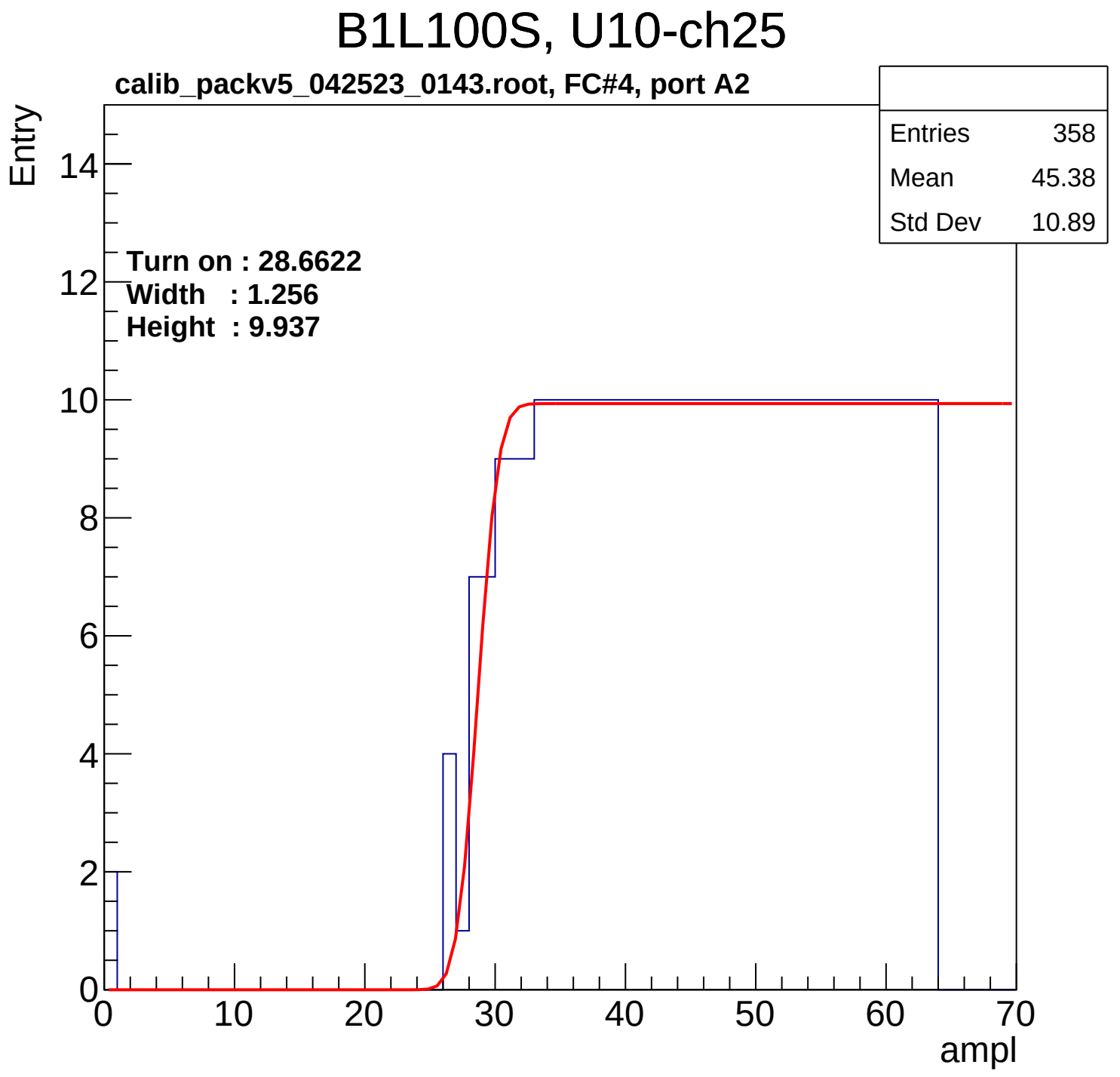
B1L100S, U10-ch25
calib_packv5_042523_0143.root, FC#4, port A2
Entries 358
Mean 45.38
Std Dev 10.89
Turn on : 28.6622
Width : 1.256
Height : 9.937
Entry
ampl
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6
8
10
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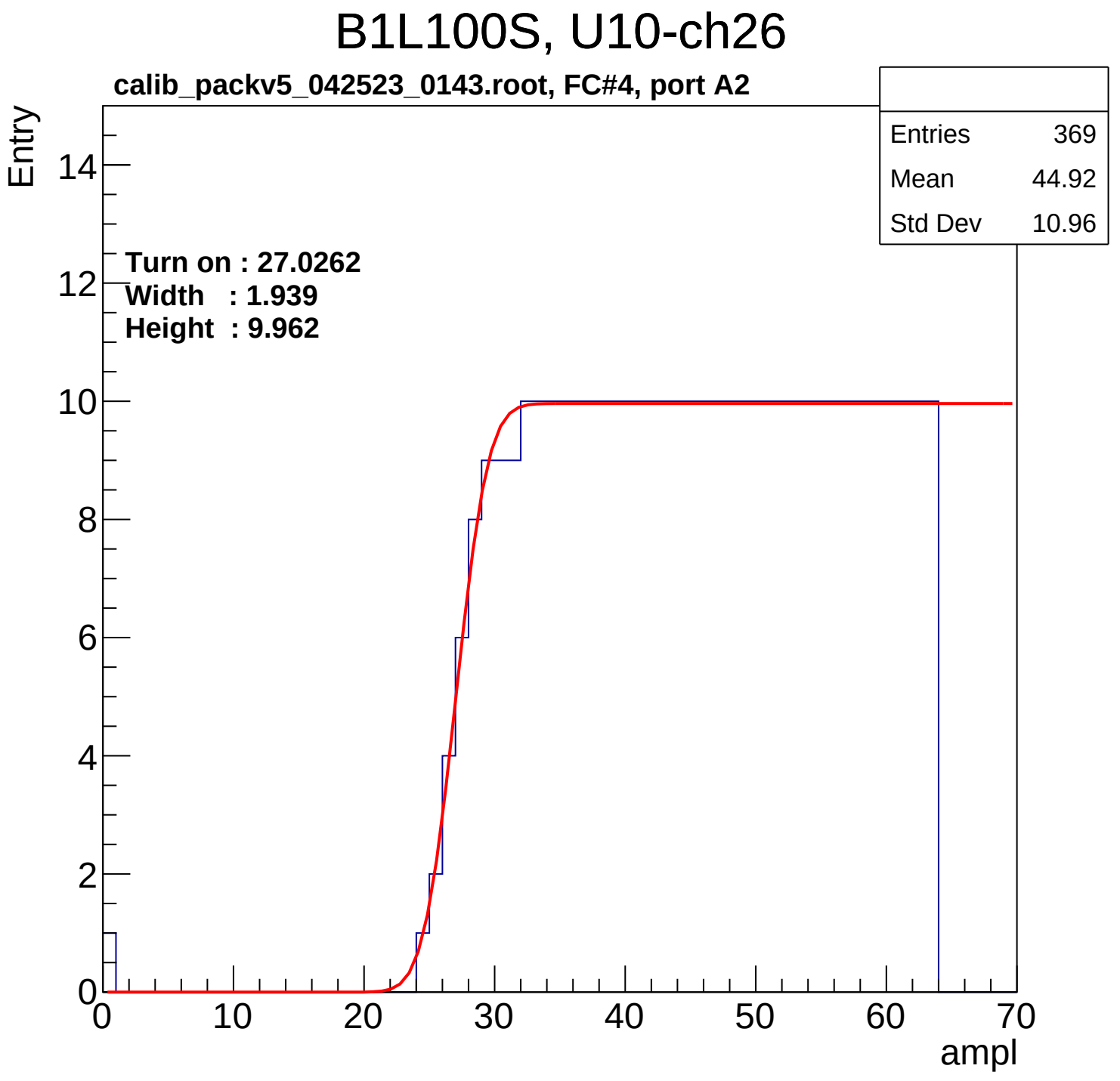
B1L100S, U10-ch26
calib_packv5_042523_0143.root, FC#4, port A2
Entries 369
Mean 44.92
Std Dev 10.96
Turn on : 27.0262
Width : 1.939
Height : 9.962
Entry
ampl
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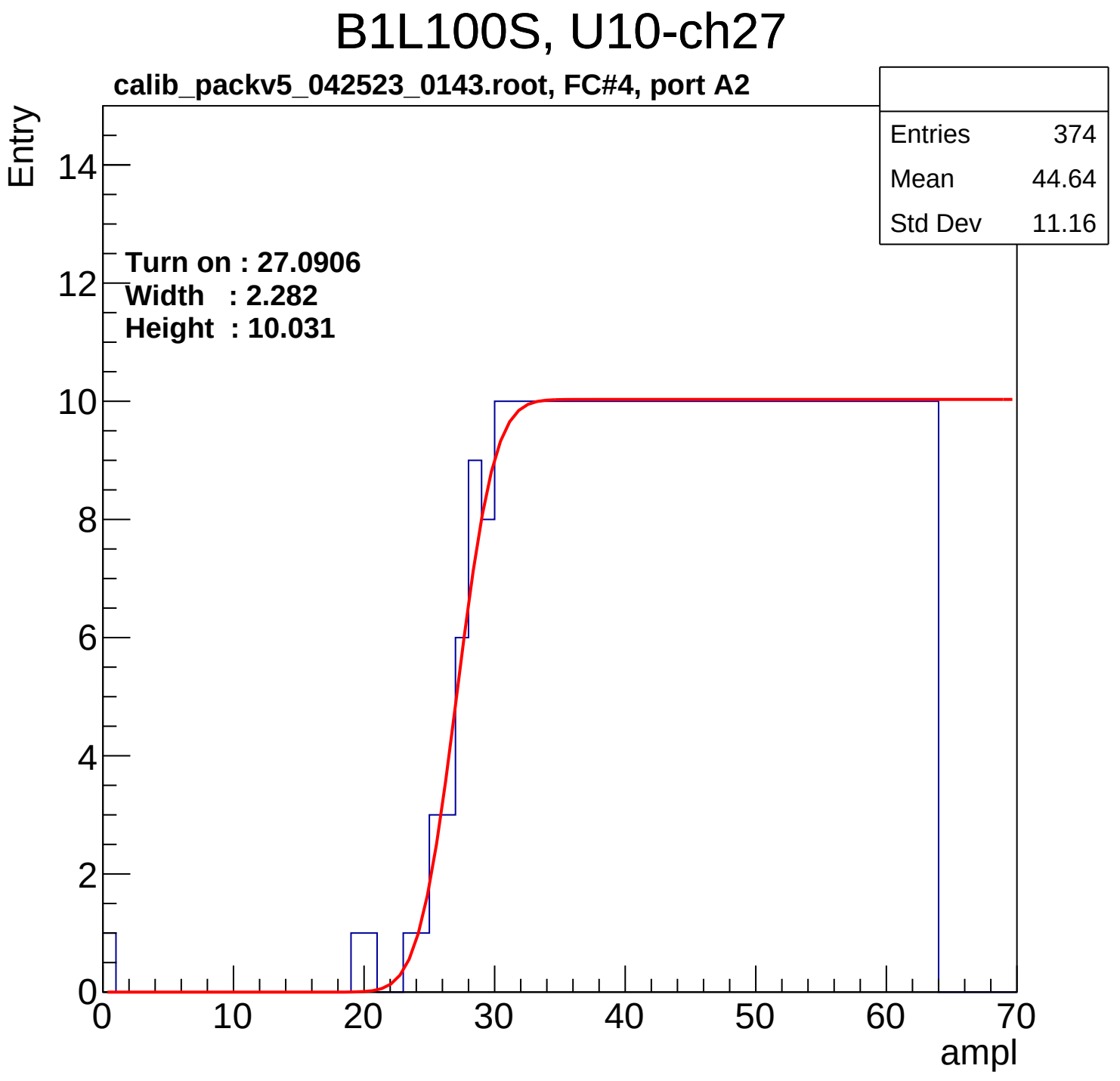
B1L100S, U10-ch27
calib_packv5_042523_0143.root, FC#4, port A2
Entries 374
Mean 44.64
Std Dev 11.16
Turn on : 27.0906
Width : 2.282
Height : 10.031
Entry
ampl
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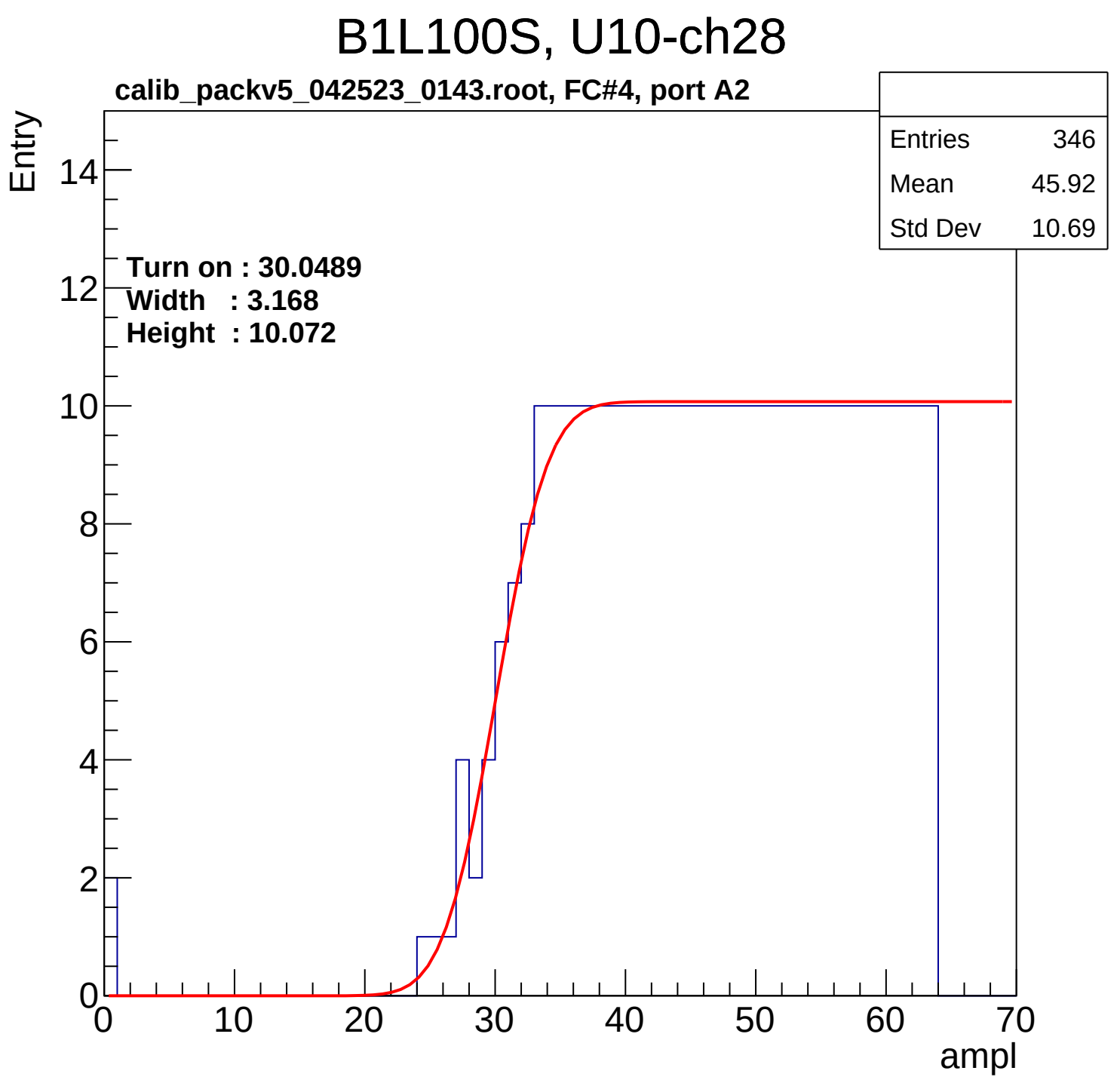
B1L100S, U10-ch28
calib_packv5_042523_0143.root, FC#4, port A2
Entries 346
Mean 45.92
Std Dev 10.69
Turn on : 30.0489
Width : 3.168
Height : 10.072
Entry
ampl
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4
6
8
10
12
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10
20
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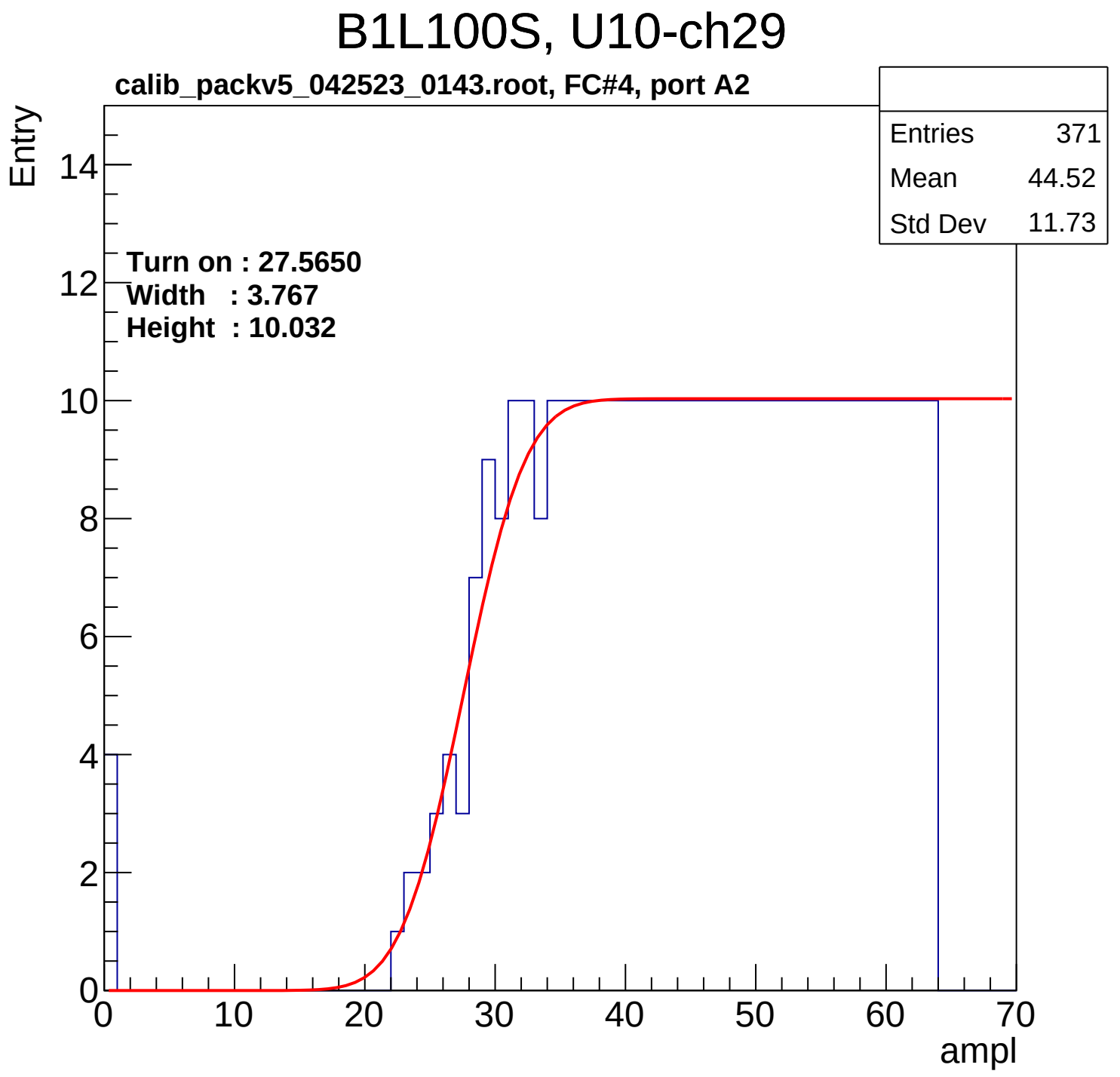
B1L100S, U10-ch29
calib_packv5_042523_0143.root, FC#4, port A2
Entries 371
Mean 44.52
Std Dev 11.73
Turn on : 27.5650
Width : 3.767
Height : 10.032
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ampl
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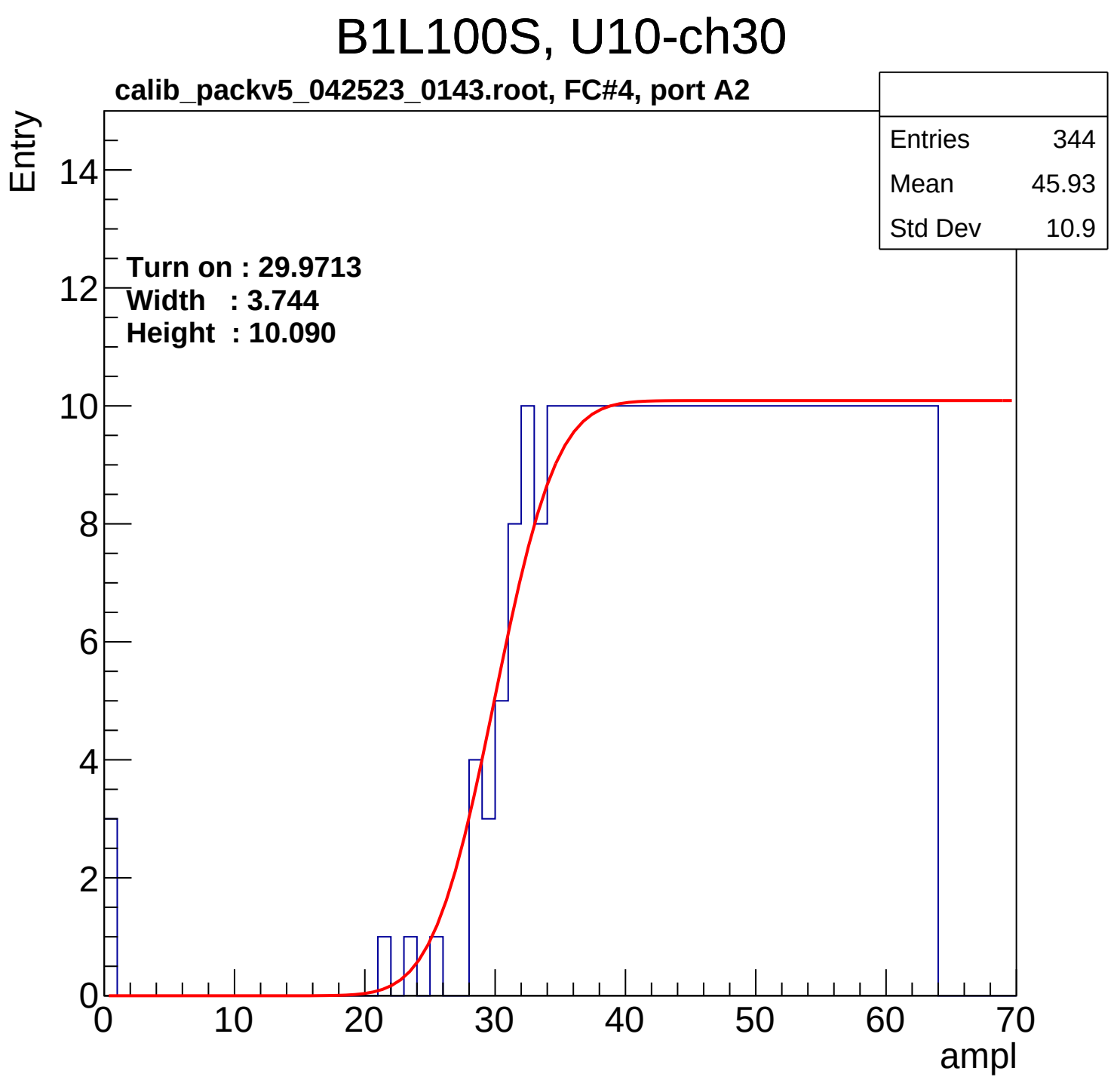
B1L100S, U10-ch30
calib_packv5_042523_0143.root, FC#4, port A2
Entries 344
Mean 45.93
Std Dev 10.9
Turn on : 29.9713
Width : 3.744
Height : 10.090
Entry
ampl
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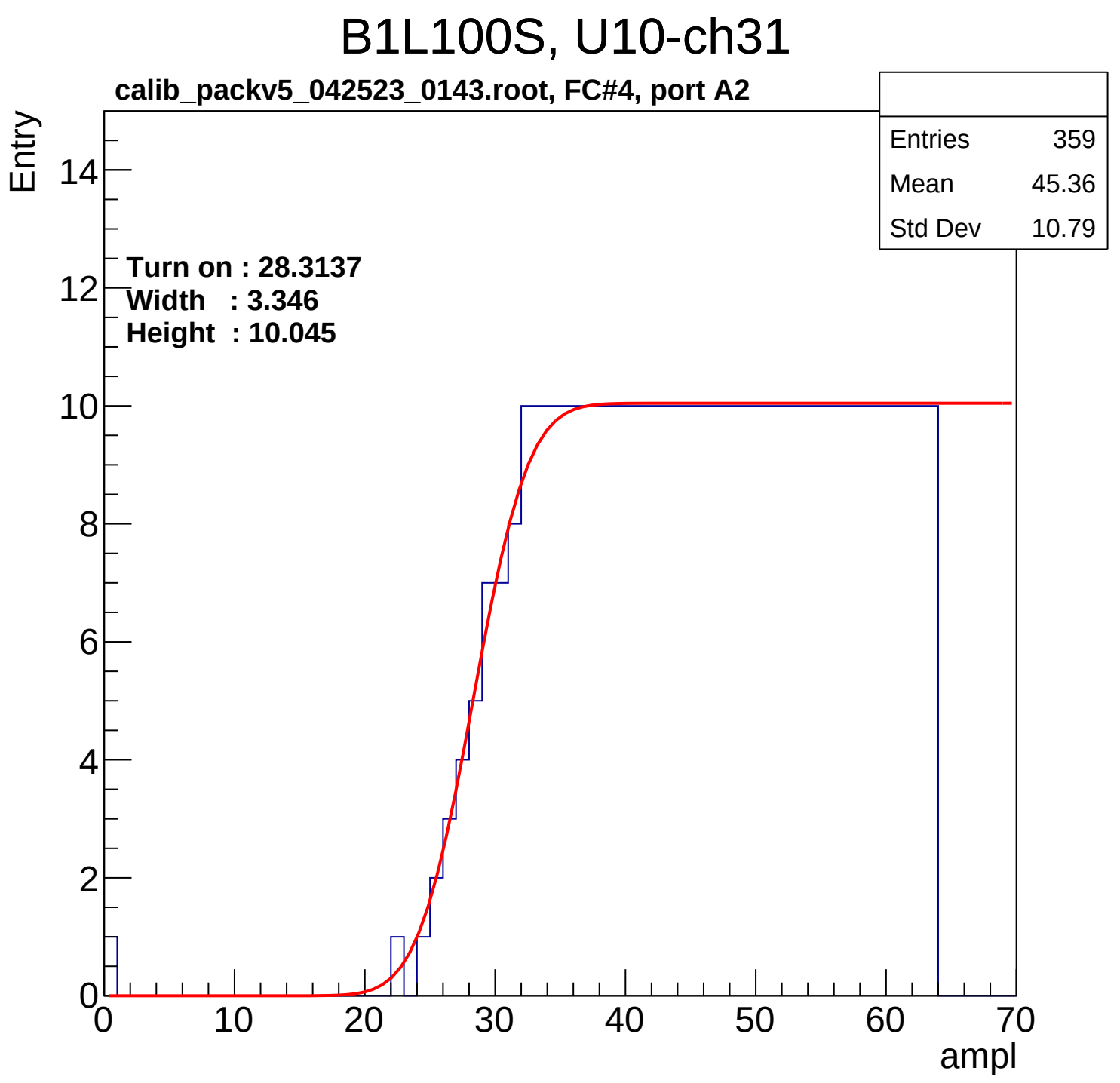
B1L100S, U10-ch31
calib_packv5_042523_0143.root, FC#4, port A2
Entries 359
Mean 45.36
Std Dev 10.79
Turn on : 28.3137
Width : 3.346
Height : 10.045
Entry
ampl
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4
6
8
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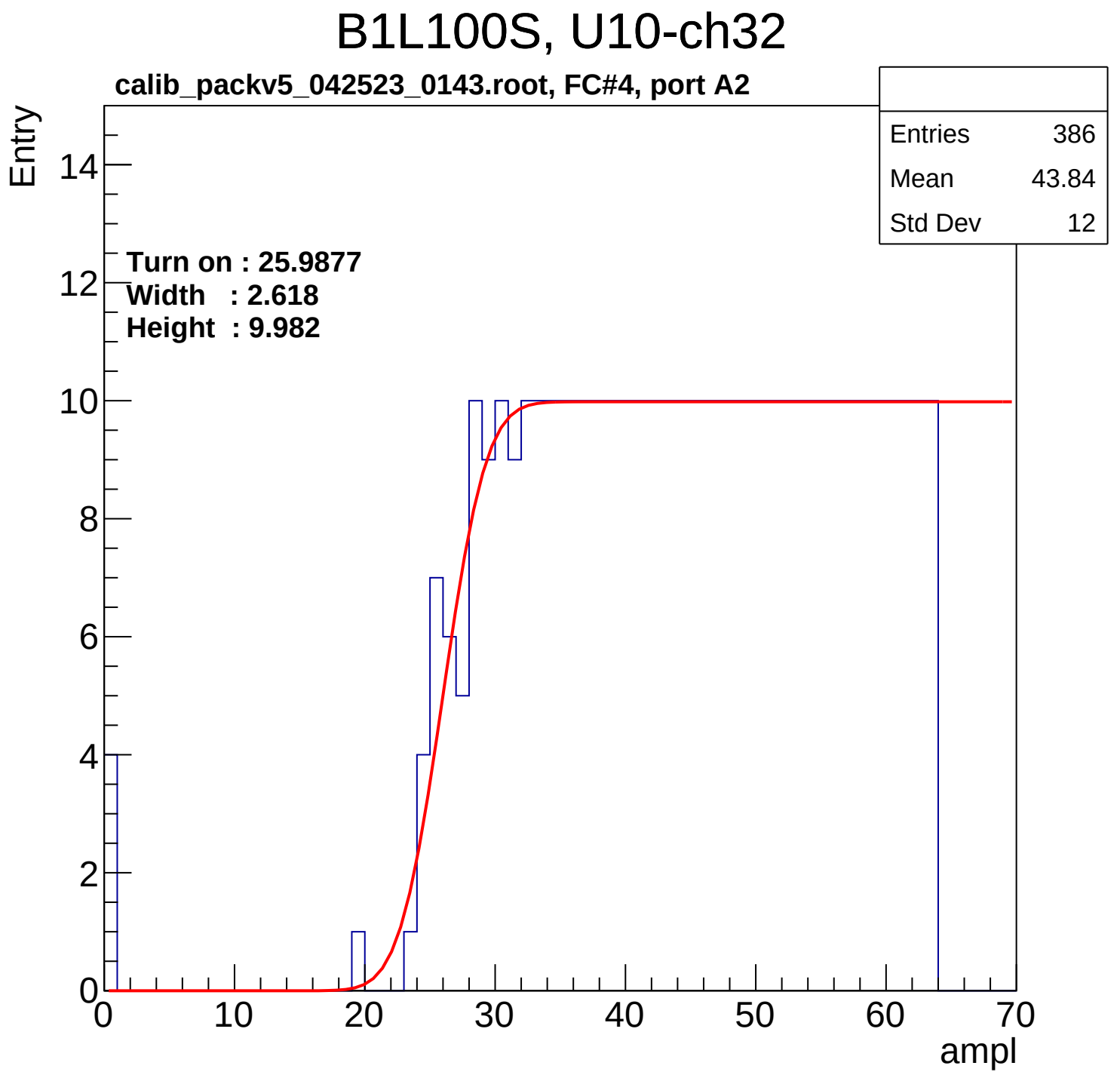
B1L100S, U10-ch32
calib_packv5_042523_0143.root, FC#4, port A2
Entries 386
Mean 43.84
Std Dev 12
Turn on : 25.9877
Width : 2.618
Height : 9.982
Entry
ampl
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4
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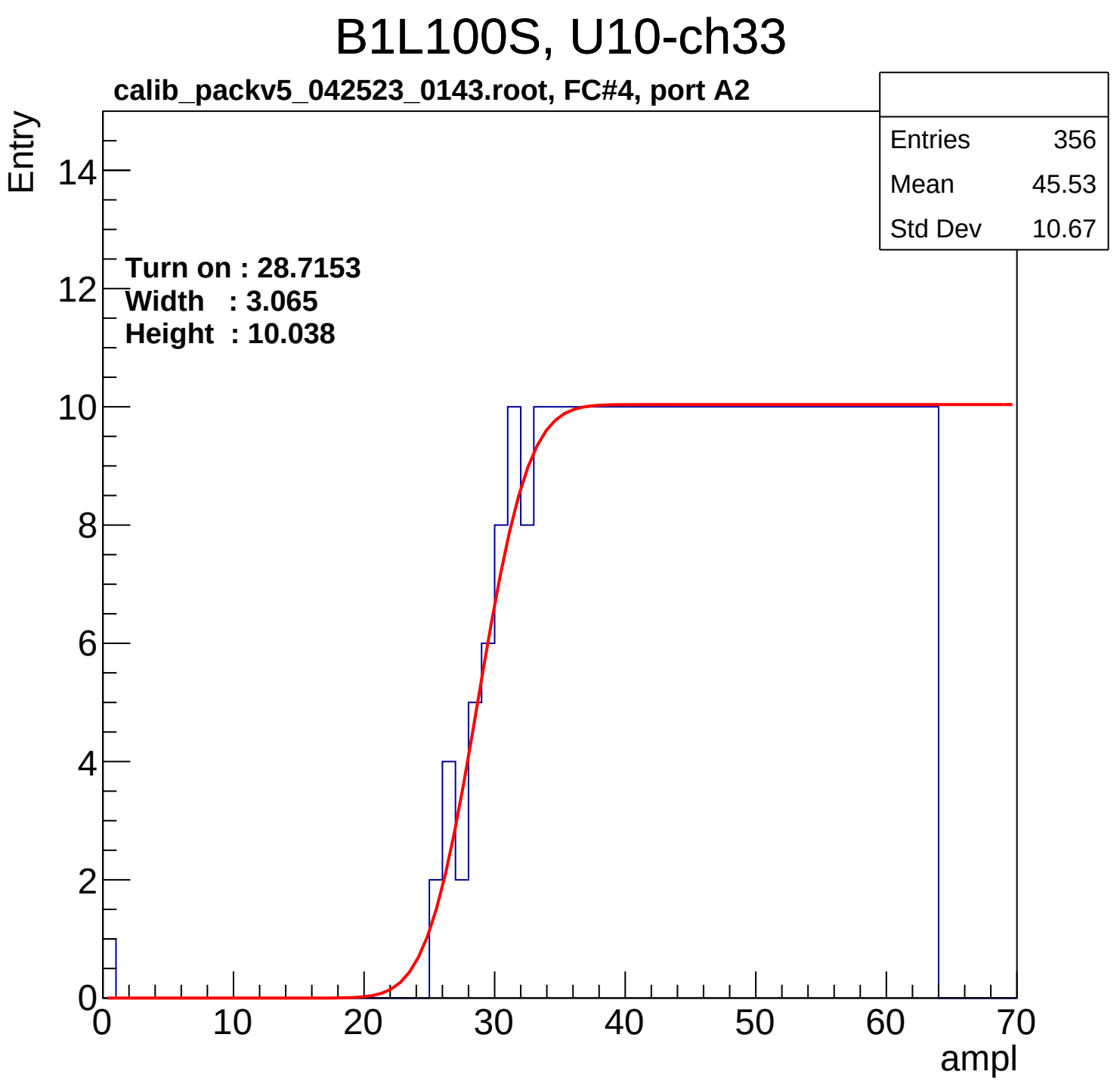
B1L100S, U10-ch33
calib_packv5_042523_0143.root, FC#4, port A2
Entries 356
Mean 45.53
Std Dev 10.67
Turn on : 28.7153
Width : 3.065
Height : 10.038
Entry
ampl
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4
6
8
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12
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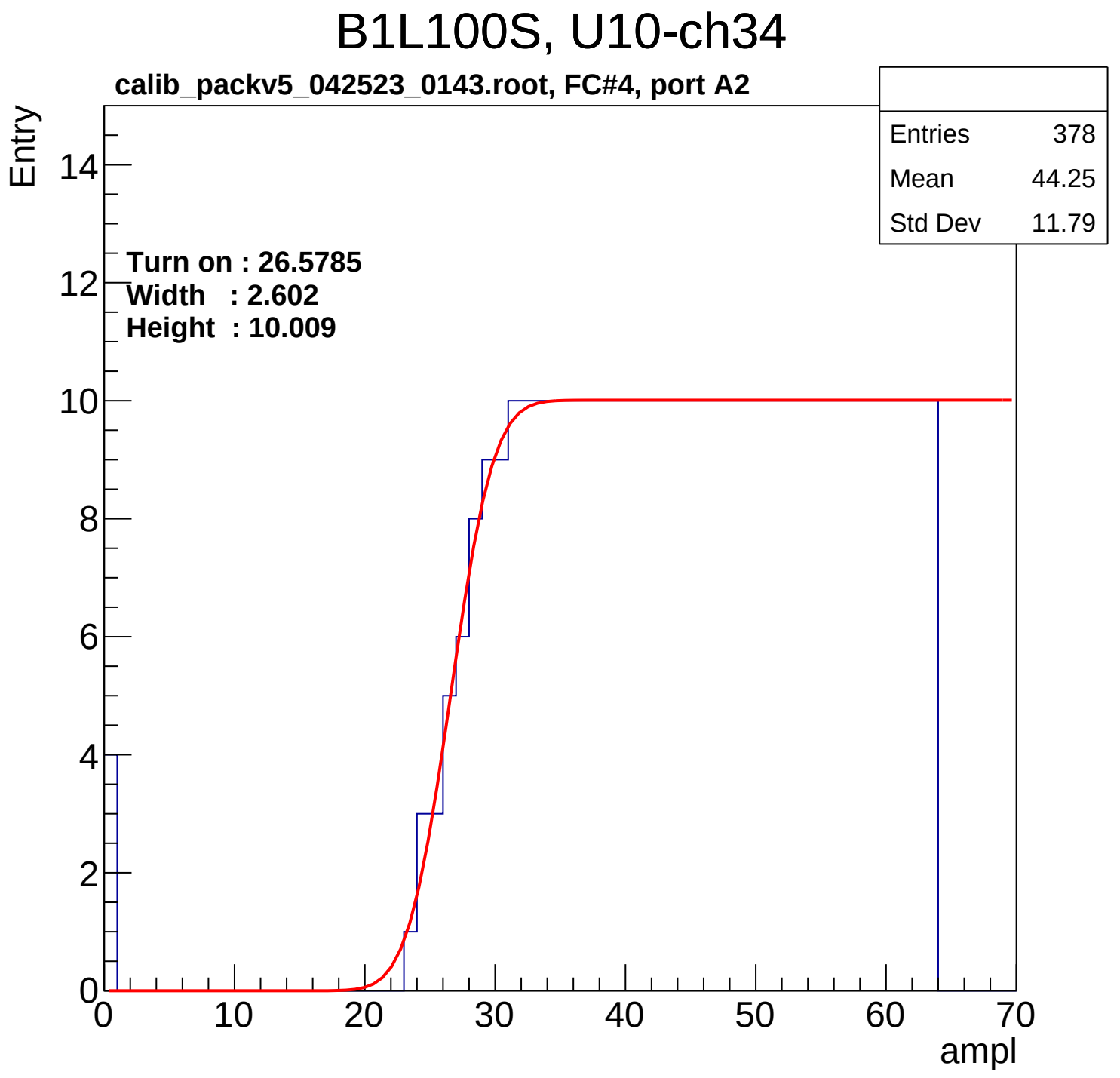
B1L100S, U10-ch34
calib_packv5_042523_0143.root, FC#4, port A2
Entries 378
Mean 44.25
Std Dev 11.79
Turn on : 26.5785
Width : 2.602
Height : 10.009
Entry
ampl
0
2
4
6
8
10
12
14
0
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60
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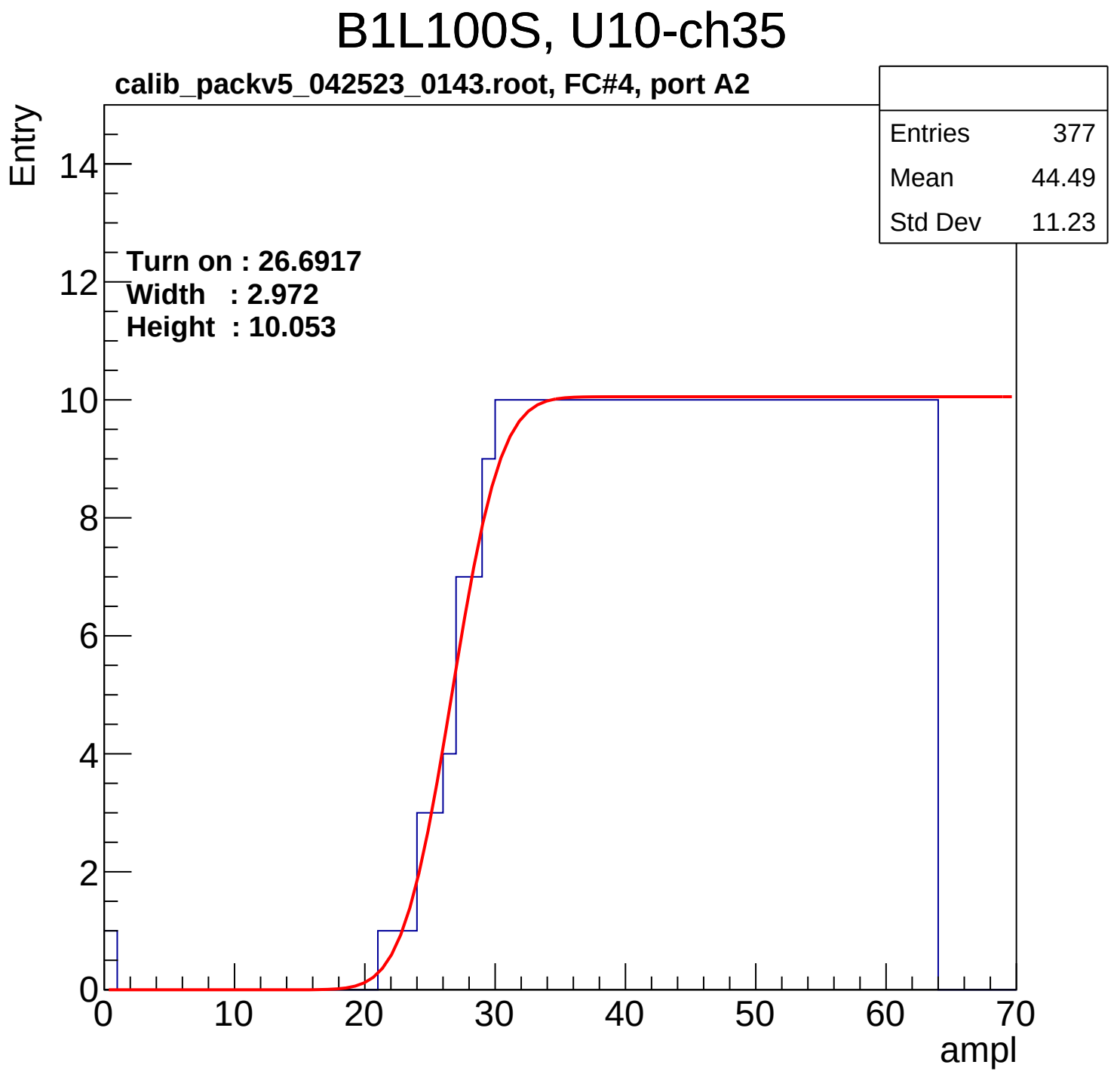
B1L100S, U10-ch35
calib_packv5_042523_0143.root, FC#4, port A2
Entries 377
Mean 44.49
Std Dev 11.23
Turn on : 26.6917
Width : 2.972
Height : 10.053
Entry
ampl
0
2
4
6
8
10
12
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0
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40
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60
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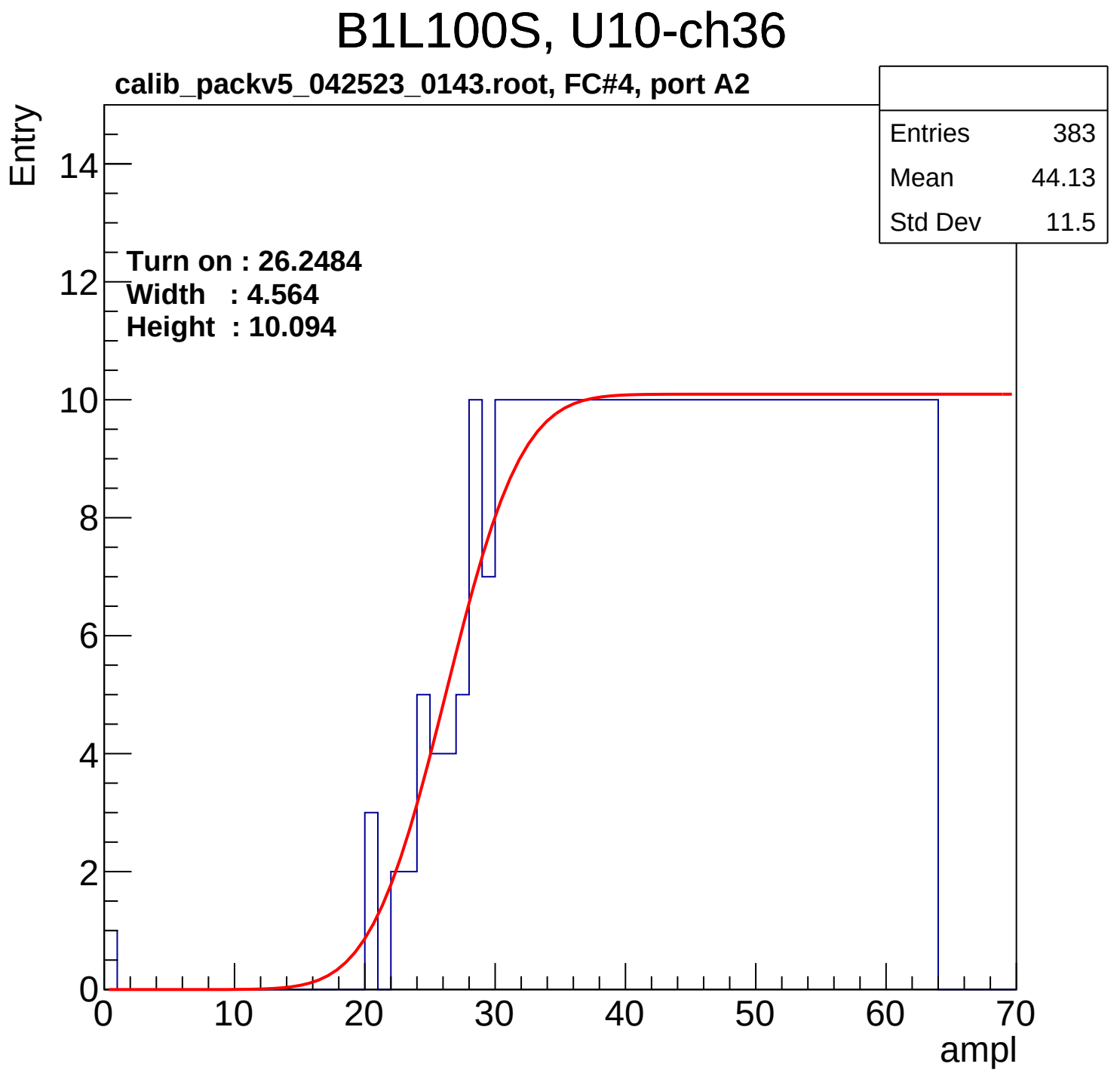
B1L100S, U10-ch36
calib_packv5_042523_0143.root, FC#4, port A2
Entries 383
Mean 44.13
Std Dev 11.5
Turn on : 26.2484
Width : 4.564
Height : 10.094
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
50
60
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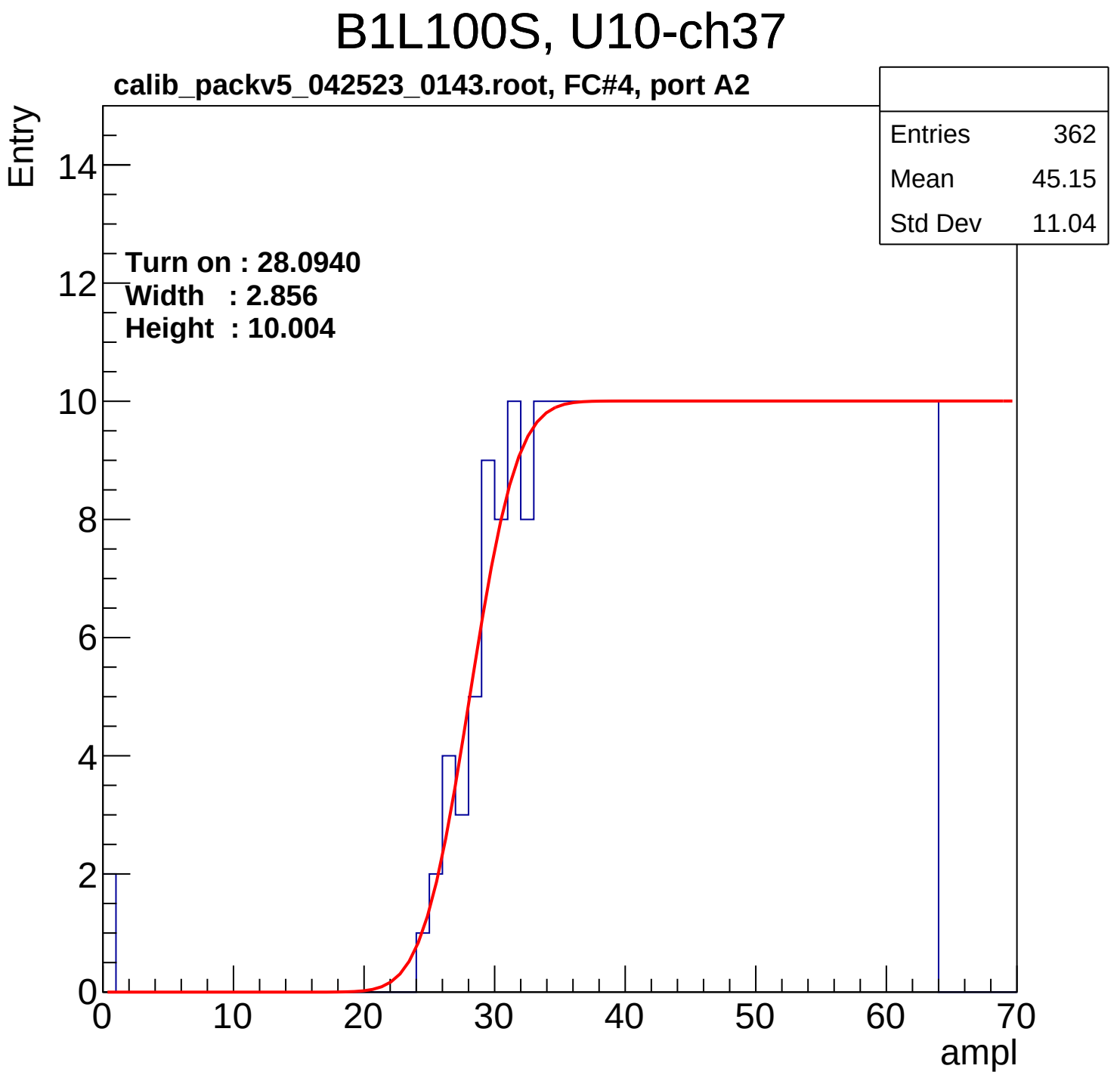
B1L100S, U10-ch37
calib_packv5_042523_0143.root, FC#4, port A2
Entries 362
Mean 45.15
Std Dev 11.04
Turn on : 28.0940
Width : 2.856
Height : 10.004
Entry
ampl
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2
4
6
8
10
12
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0
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20
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60
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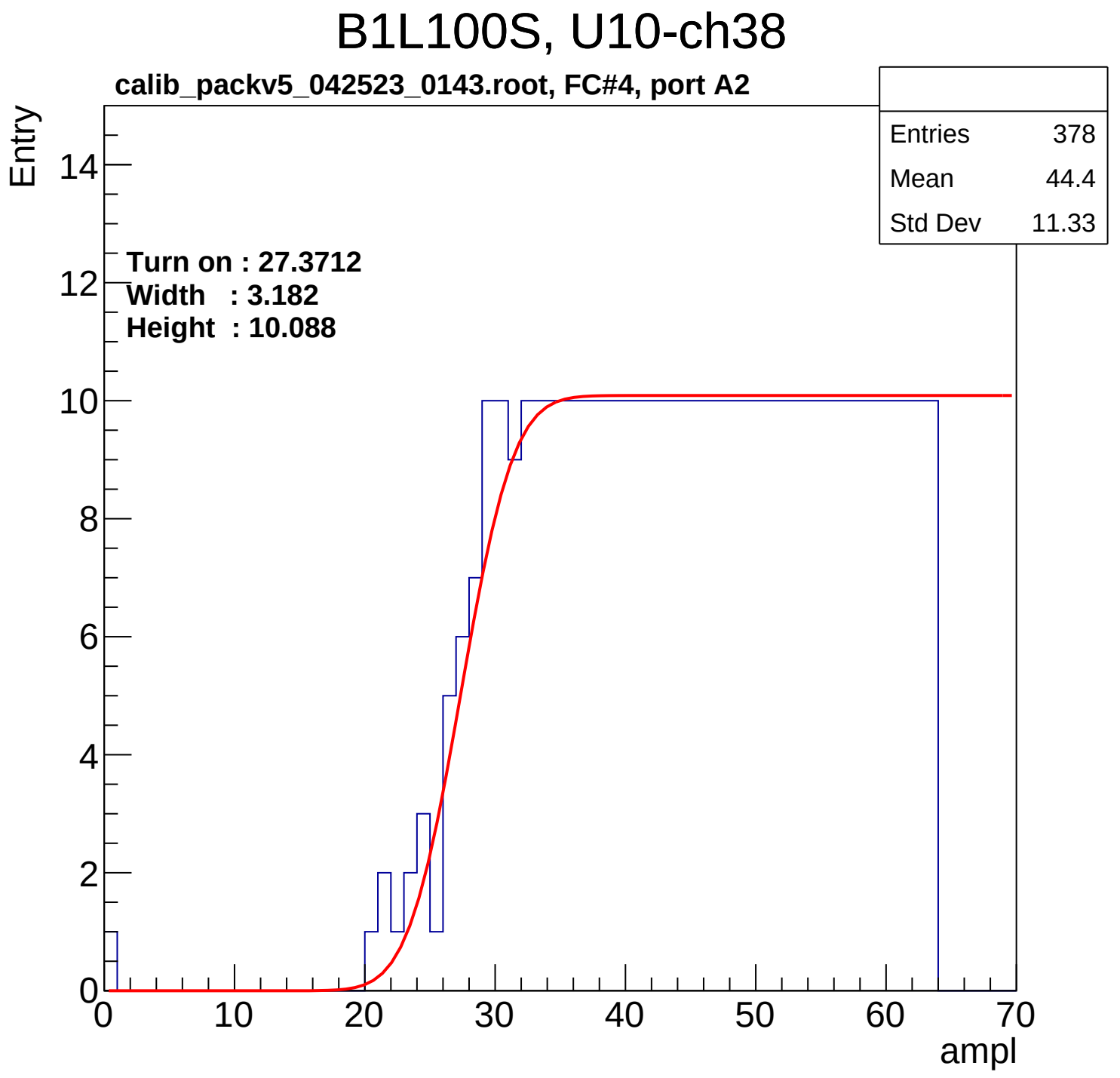
B1L100S, U10-ch38
calib_packv5_042523_0143.root, FC#4, port A2
Entries 378
Mean 44.4
Std Dev 11.33
Turn on : 27.3712
Width : 3.182
Height : 10.088
Entry
ampl
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2
4
6
8
10
12
14
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60
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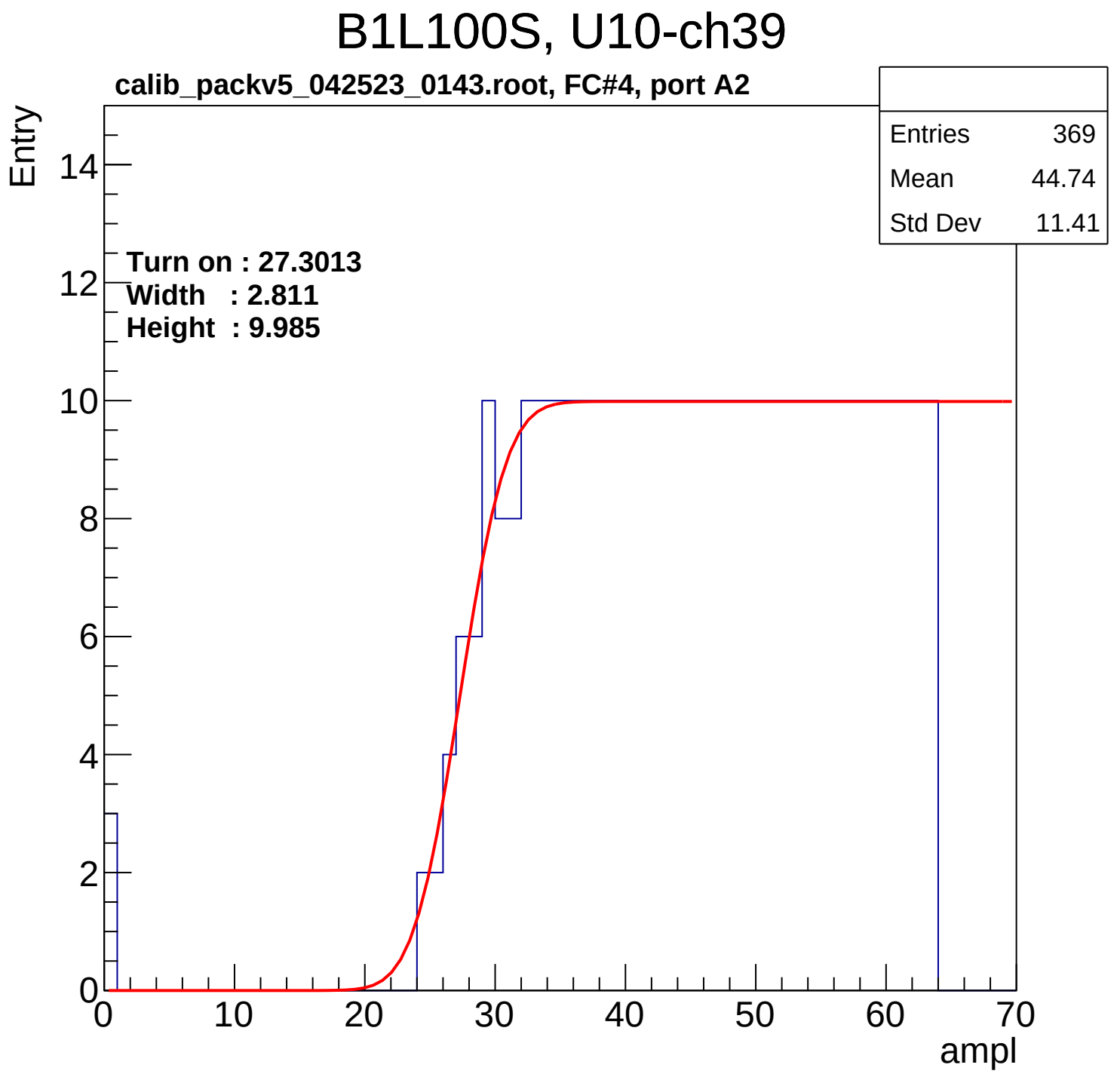
B1L100S, U10-ch39
calib_packv5_042523_0143.root, FC#4, port A2
Entries 369
Mean 44.74
Std Dev 11.41
Turn on : 27.3013
Width : 2.811
Height : 9.985
Entry
ampl
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4
6
8
10
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0
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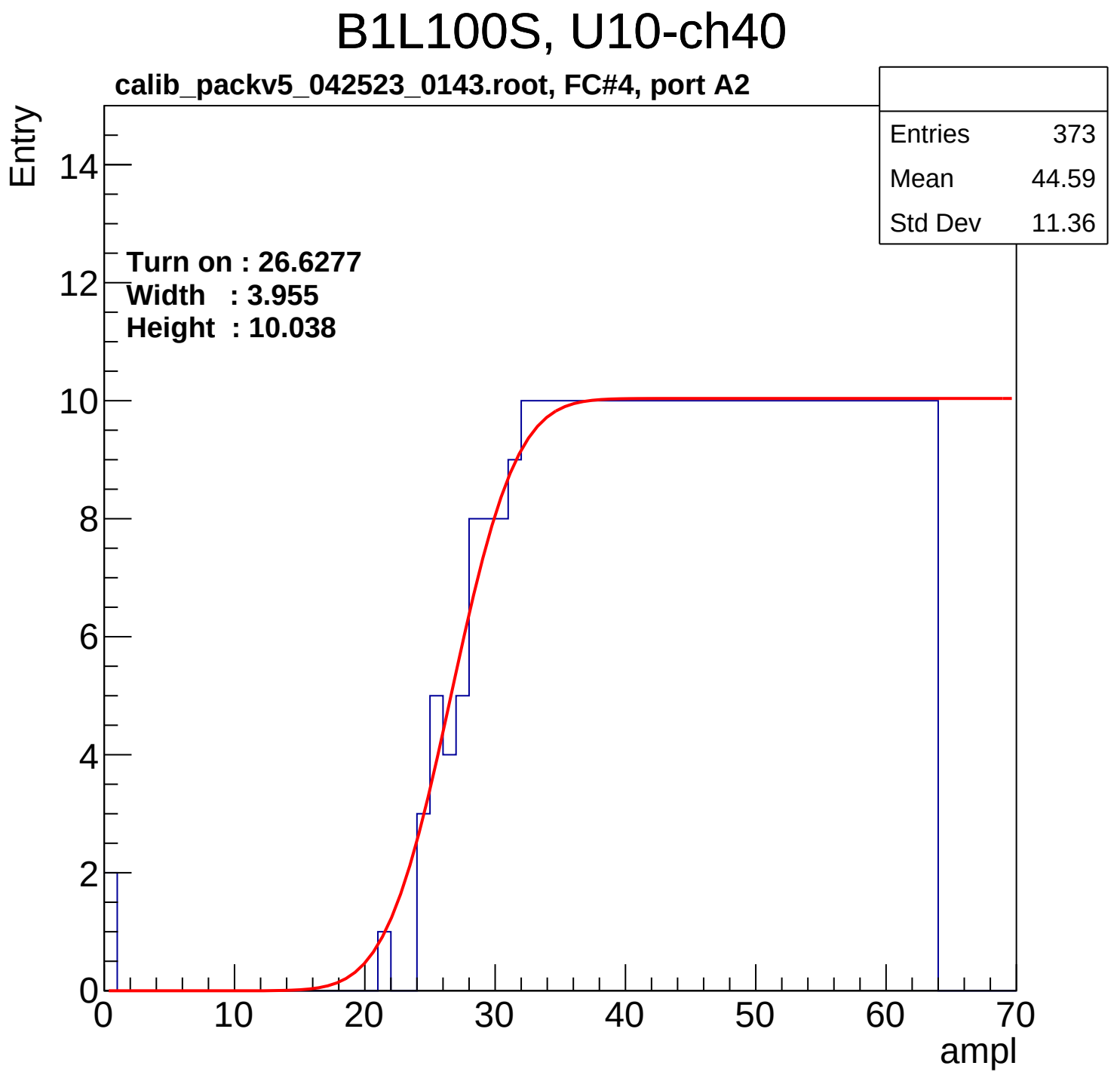
B1L100S, U10-ch40
calib_packv5_042523_0143.root, FC#4, port A2
Entries 373
Mean 44.59
Std Dev 11.36
Turn on : 26.6277
Width : 3.955
Height : 10.038
Entry
ampl
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6
8
10
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0
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20
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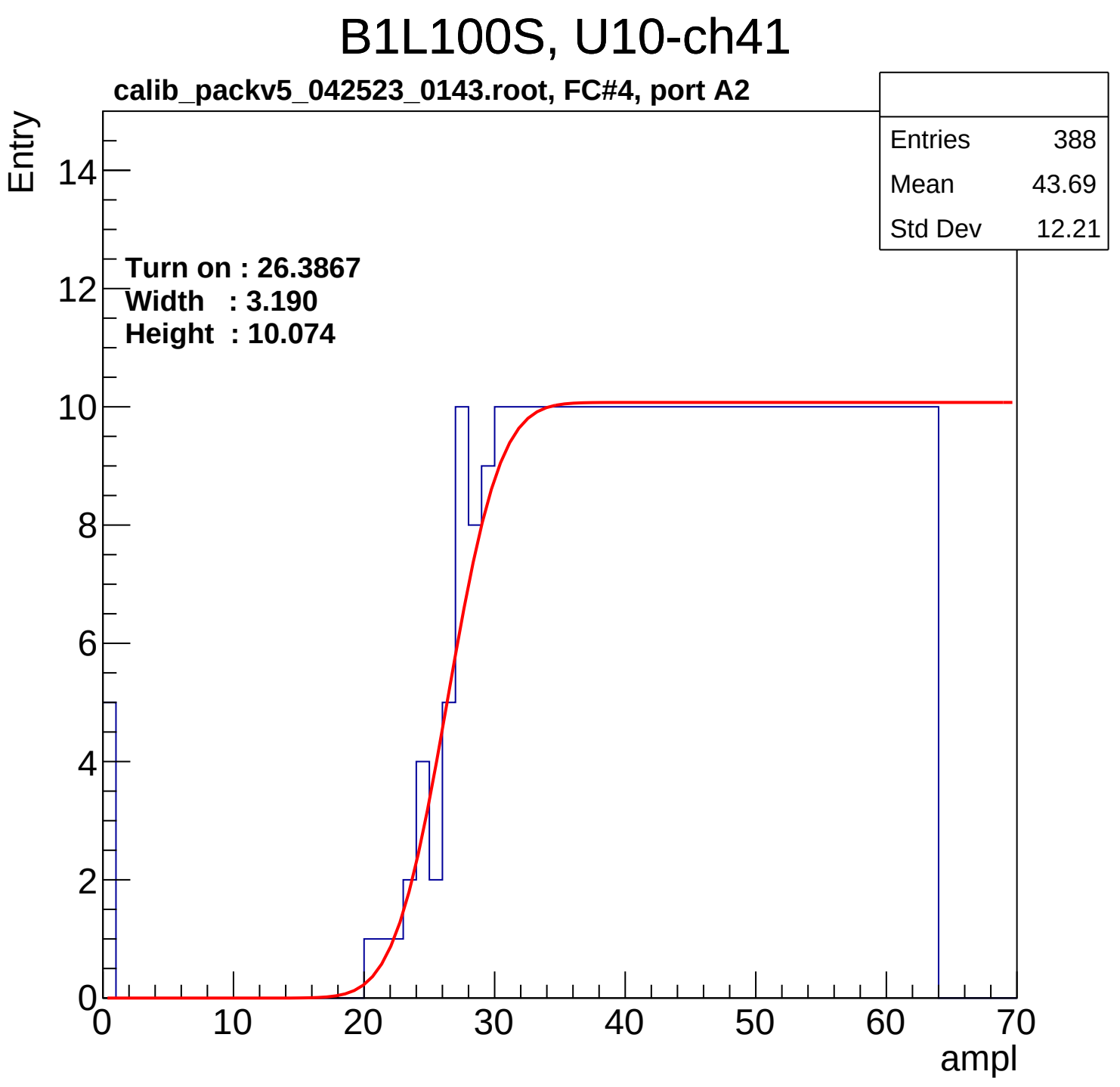
B1L100S, U10-ch41
calib_packv5_042523_0143.root, FC#4, port A2
Entries 388
Mean 43.69
Std Dev 12.21
Turn on : 26.3867
Width : 3.190
Height : 10.074
Entry
ampl
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6
8
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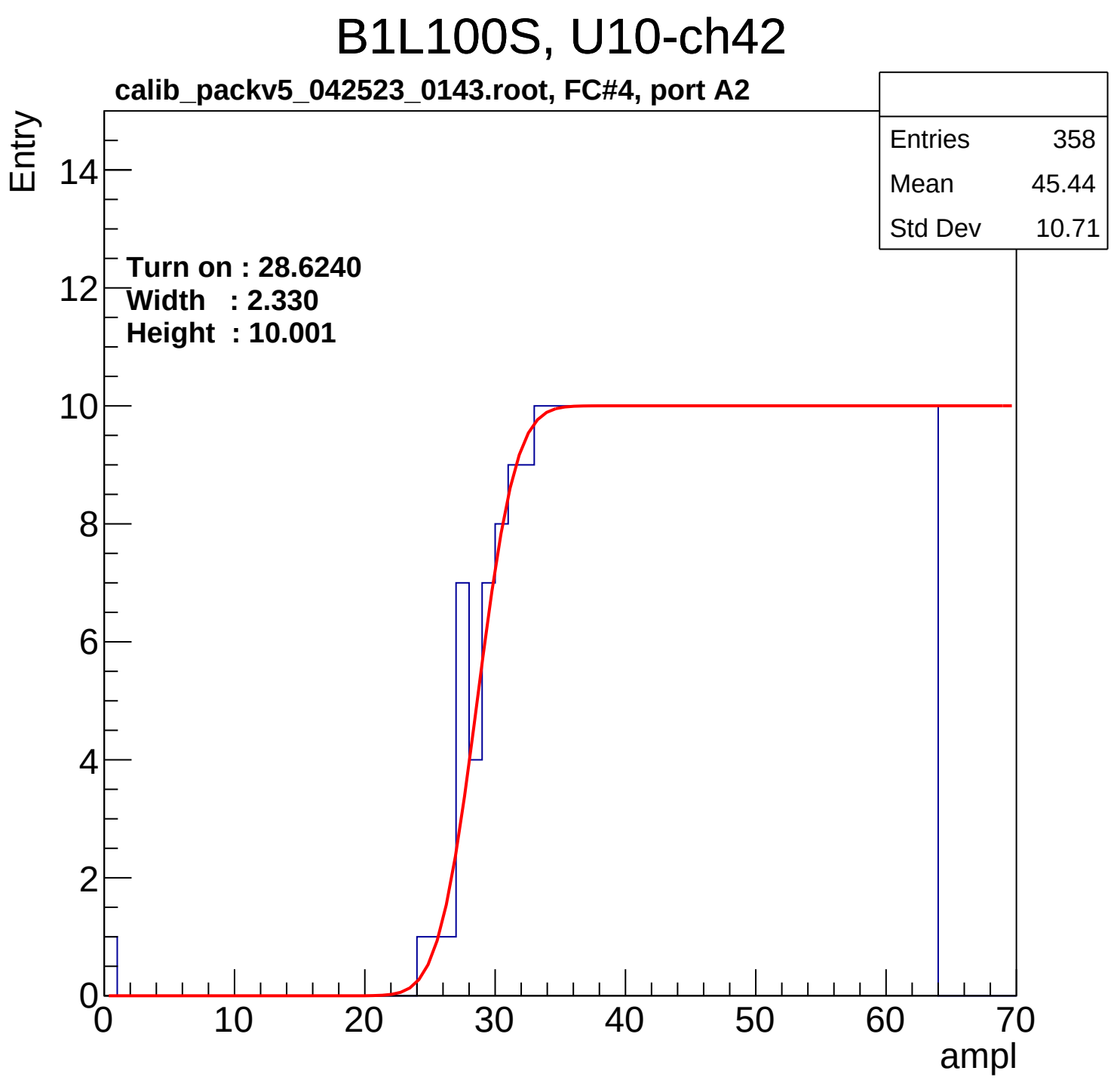
B1L100S, U10-ch42
calib_packv5_042523_0143.root, FC#4, port A2
Entries 358
Mean 45.44
Std Dev 10.71
Turn on : 28.6240
Width : 2.330
Height : 10.001
Entry
ampl
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2
4
6
8
10
12
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0
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20
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60
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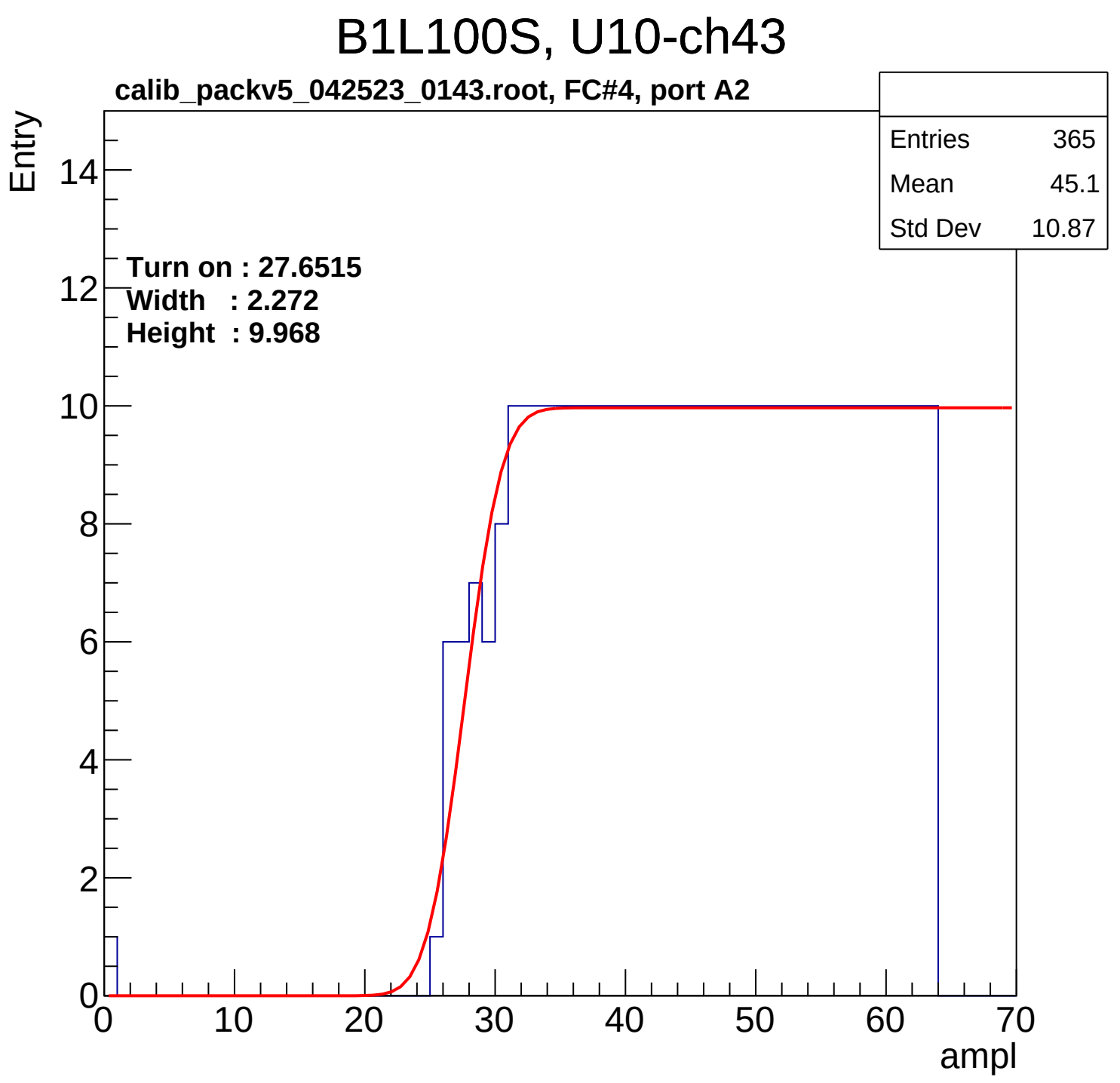
B1L100S, U10-ch43
calib_packv5_042523_0143.root, FC#4, port A2
Entries 365
Mean 45.1
Std Dev 10.87
Turn on : 27.6515
Width : 2.272
Height : 9.968
Entry
ampl
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6
8
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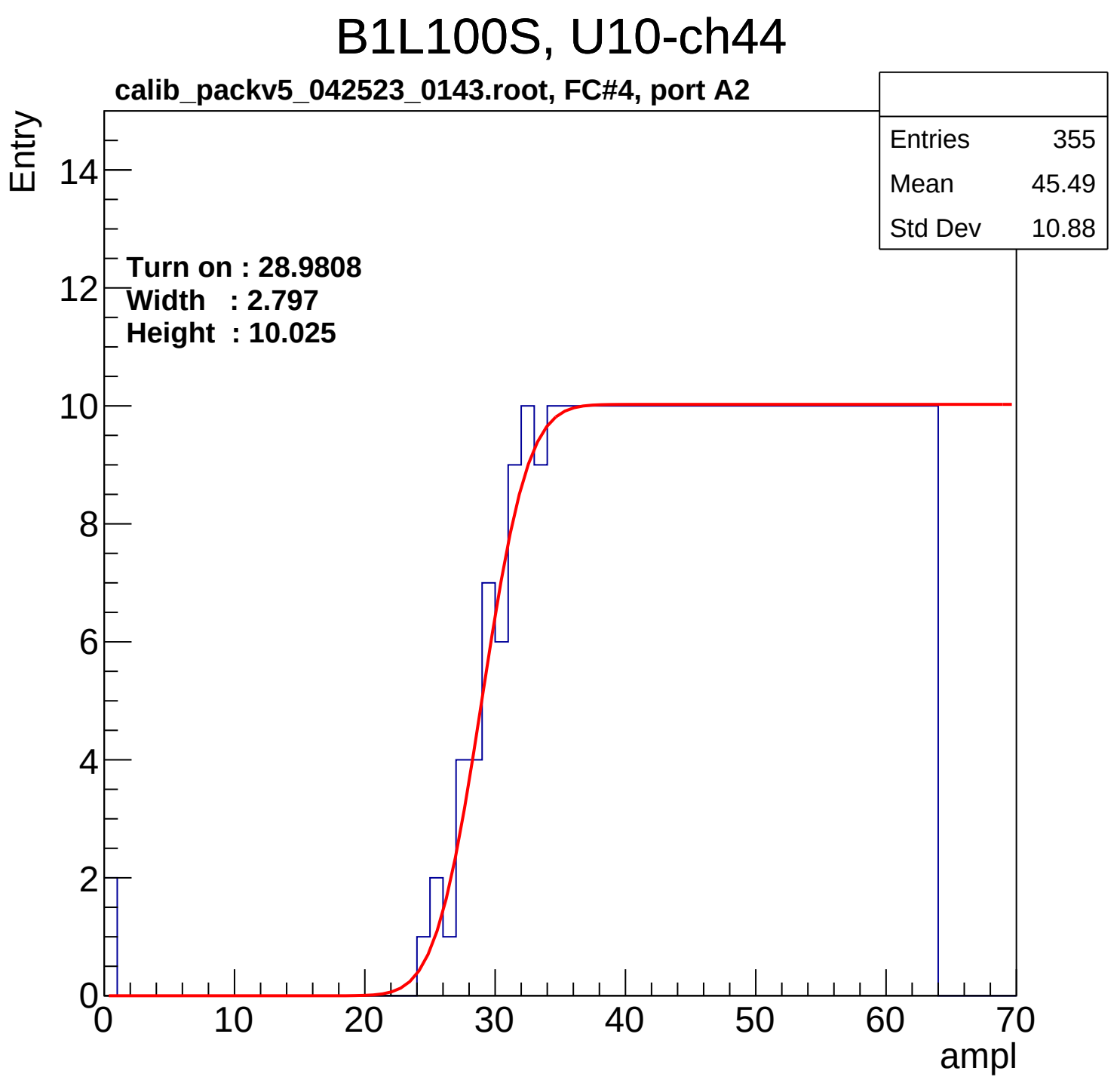
B1L100S, U10-ch44
calib_packv5_042523_0143.root, FC#4, port A2
Entries 355
Mean 45.49
Std Dev 10.88
Turn on : 28.9808
Width : 2.797
Height : 10.025
Entry
ampl
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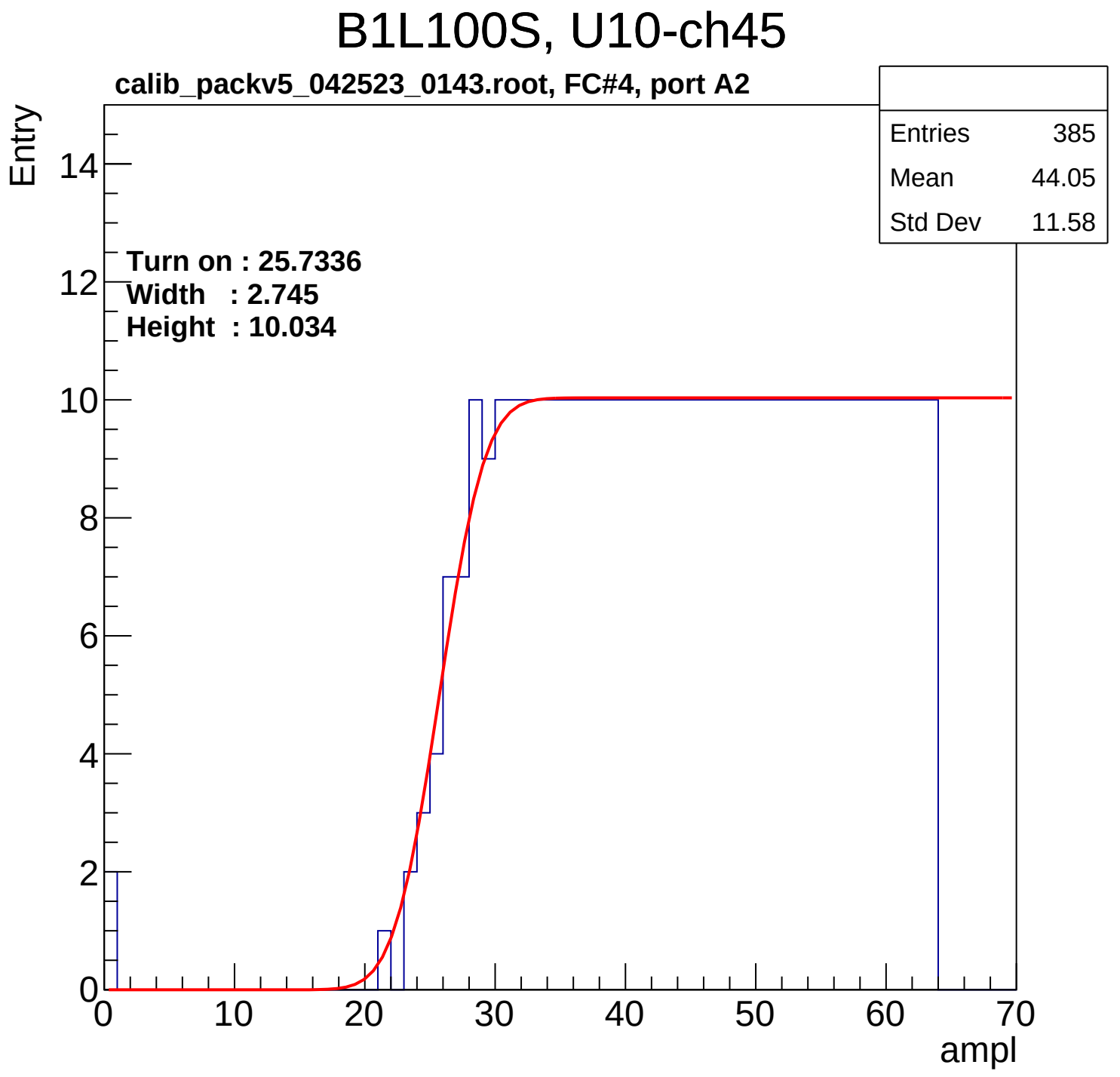
B1L100S, U10-ch45
calib_packv5_042523_0143.root, FC#4, port A2
Entries 385
Mean 44.05
Std Dev 11.58
Turn on : 25.7336
Width : 2.745
Height : 10.034
Entry
ampl
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6
8
10
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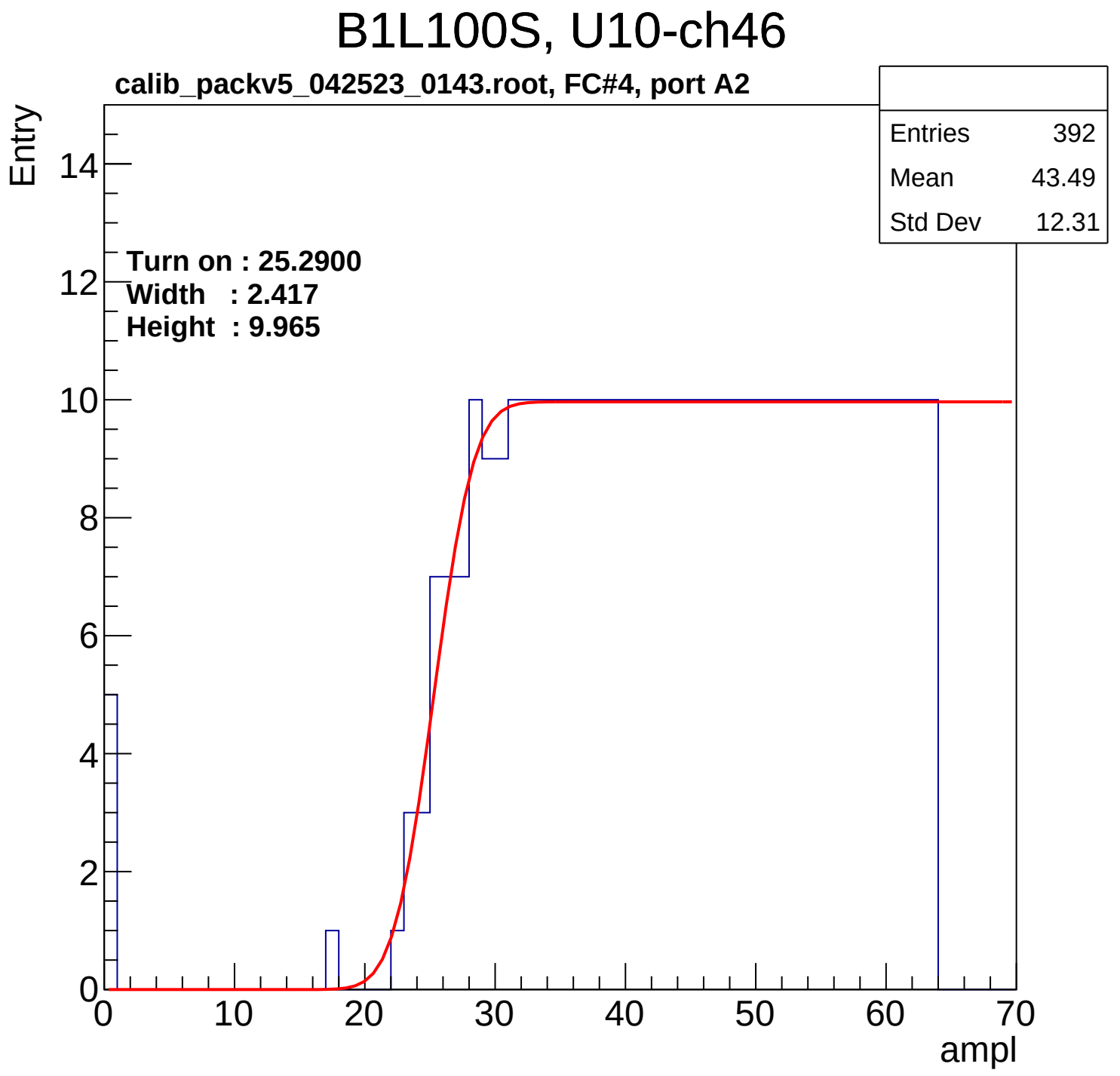
B1L100S, U10-ch46
calib_packv5_042523_0143.root, FC#4, port A2
Entries 392
Mean 43.49
Std Dev 12.31
Turn on : 25.2900
Width : 2.417
Height : 9.965
Entry
ampl
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6
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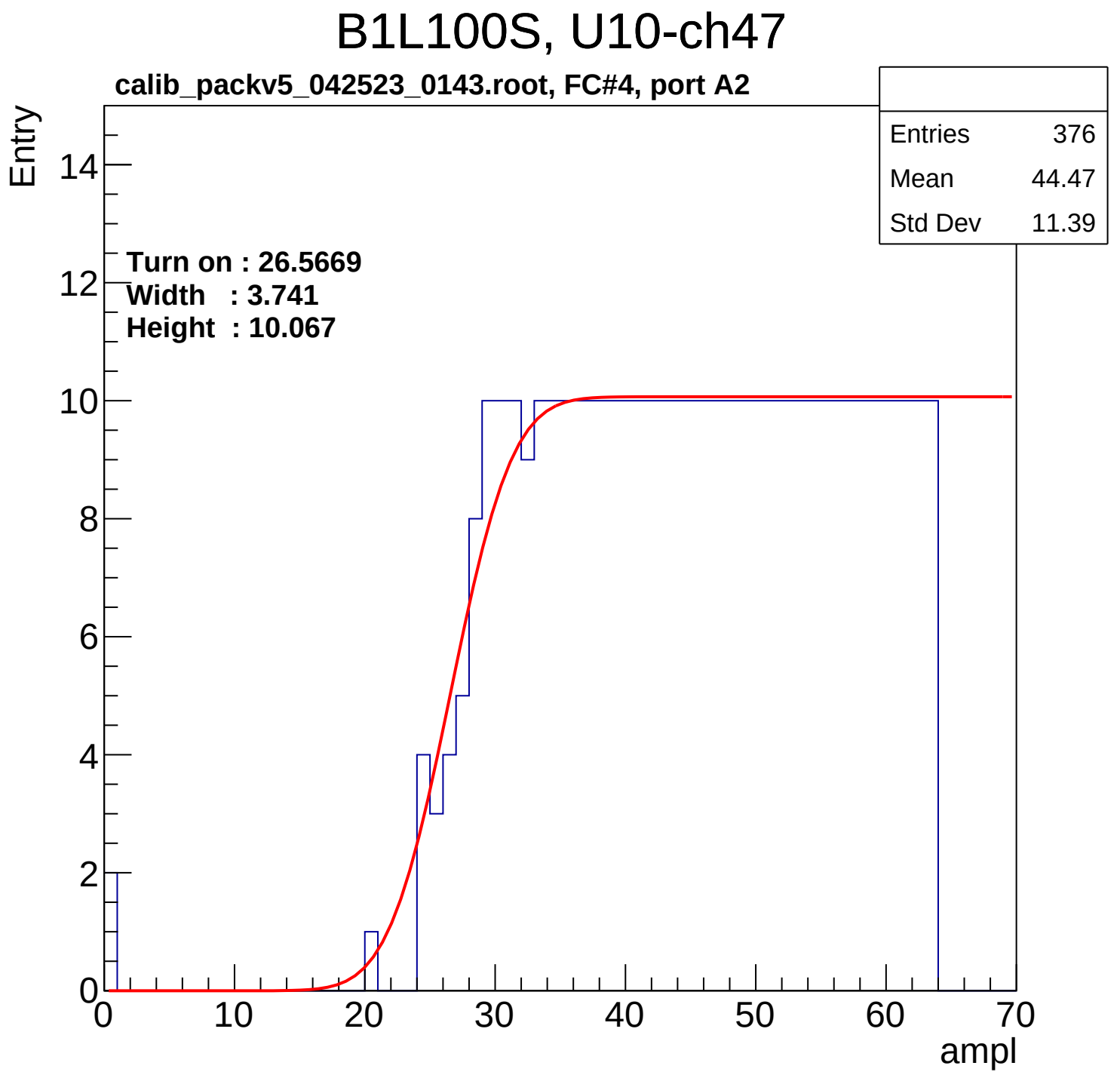
B1L100S, U10-ch47
calib_packv5_042523_0143.root, FC#4, port A2
Entries 376
Mean 44.47
Std Dev 11.39
Turn on : 26.5669
Width : 3.741
Height : 10.067
Entry
ampl
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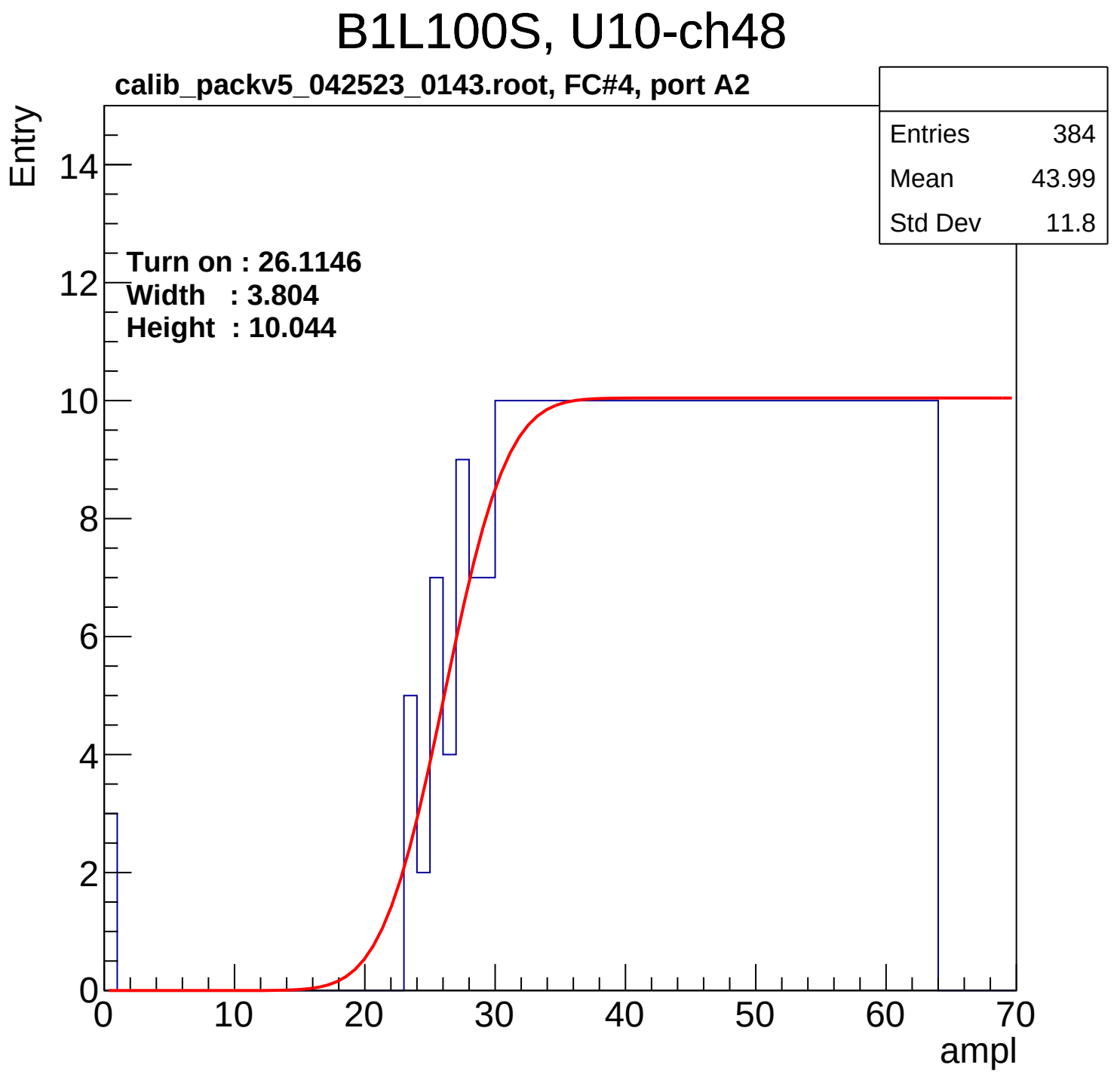
B1L100S, U10-ch48
calib_packv5_042523_0143.root, FC#4, port A2
Entries 384
Mean 43.99
Std Dev 11.8
Turn on : 26.1146
Width : 3.804
Height : 10.044
Entry
ampl
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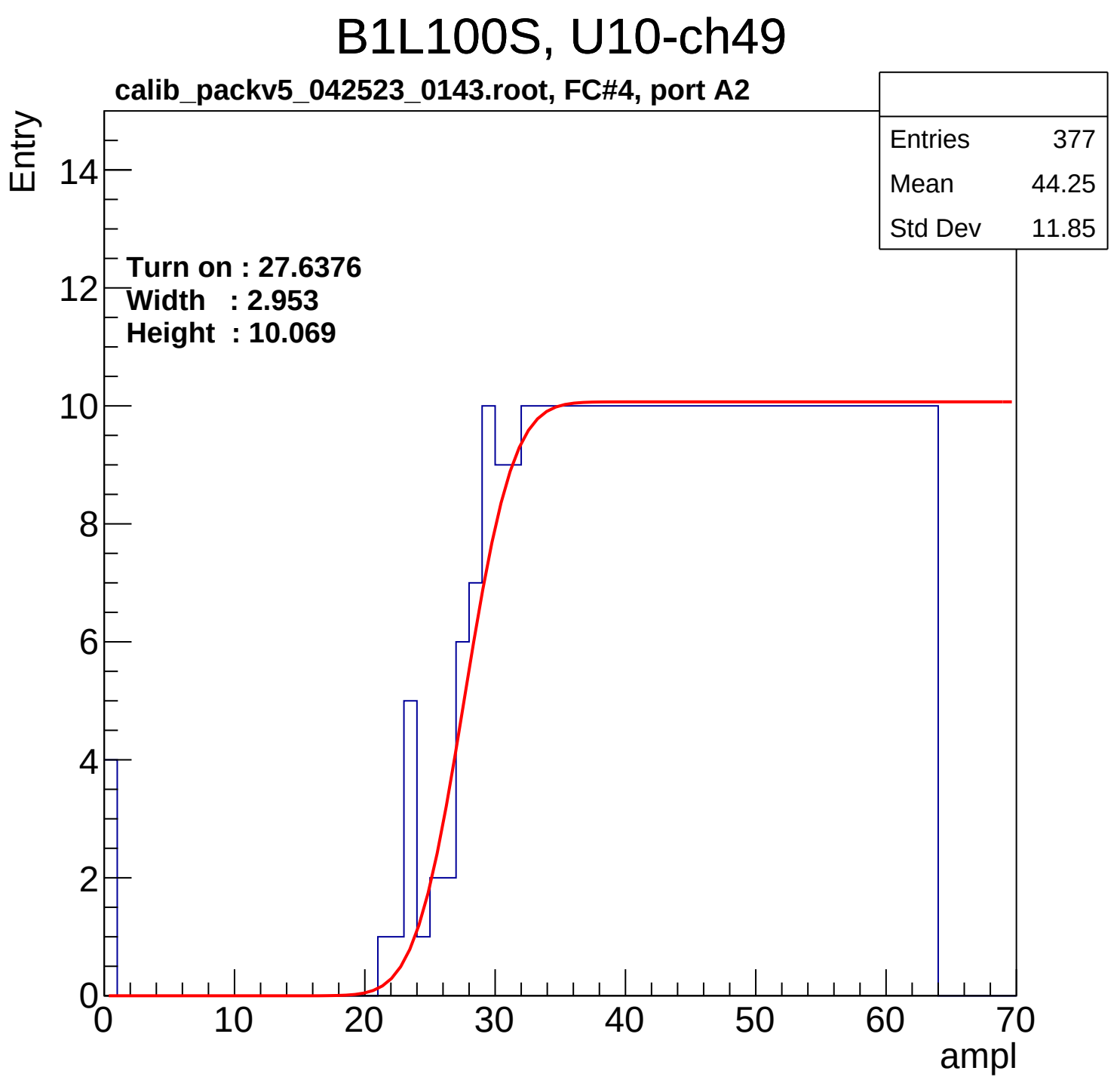
B1L100S, U10-ch49
calib_packv5_042523_0143.root, FC#4, port A2
Entries 377
Mean 44.25
Std Dev 11.85
Turn on : 27.6376
Width : 2.953
Height : 10.069
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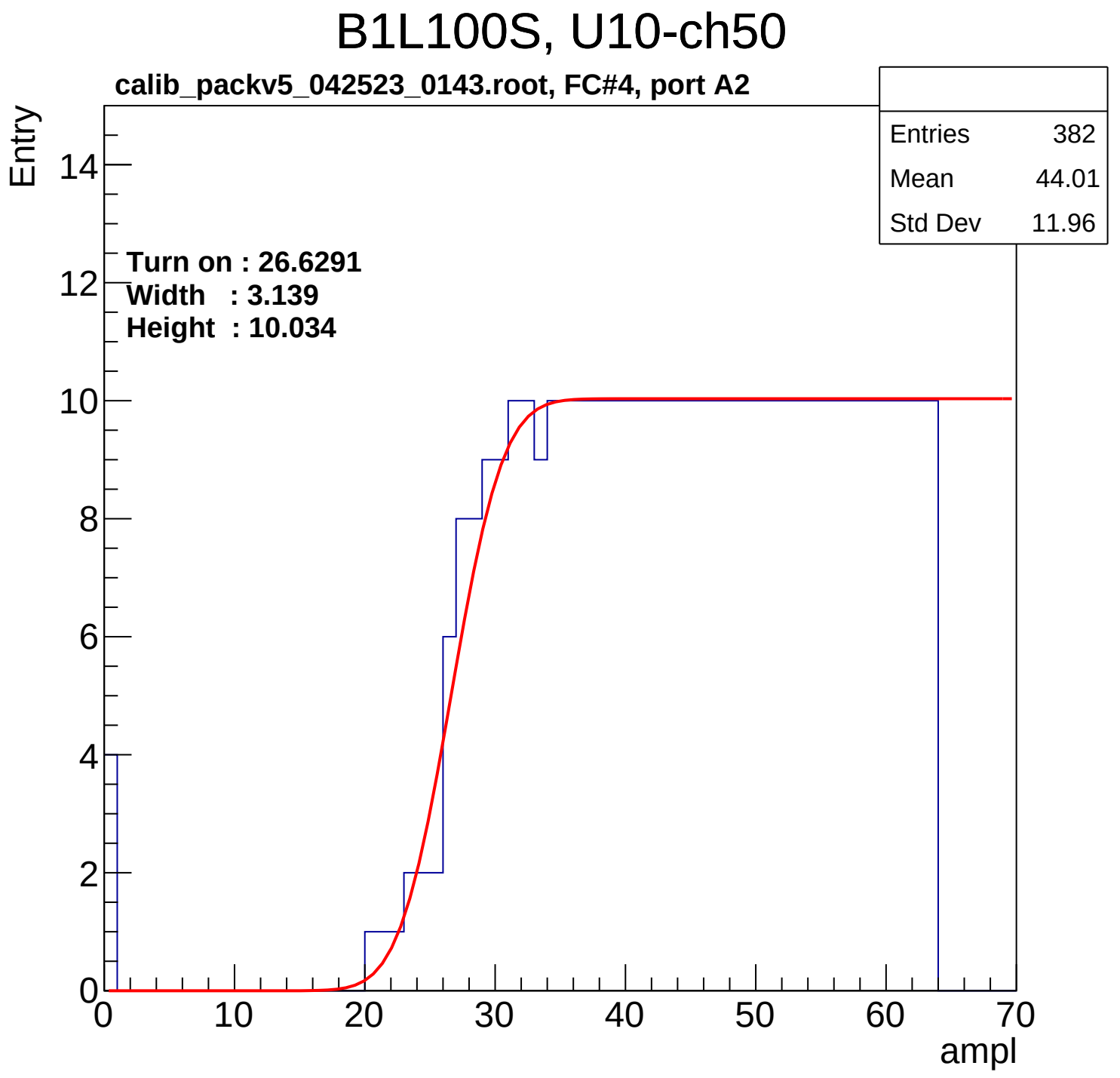
B1L100S, U10-ch50
calib_packv5_042523_0143.root, FC#4, port A2
Entries 382
Mean 44.01
Std Dev 11.96
Turn on : 26.6291
Width : 3.139
Height : 10.034
Entry
ampl
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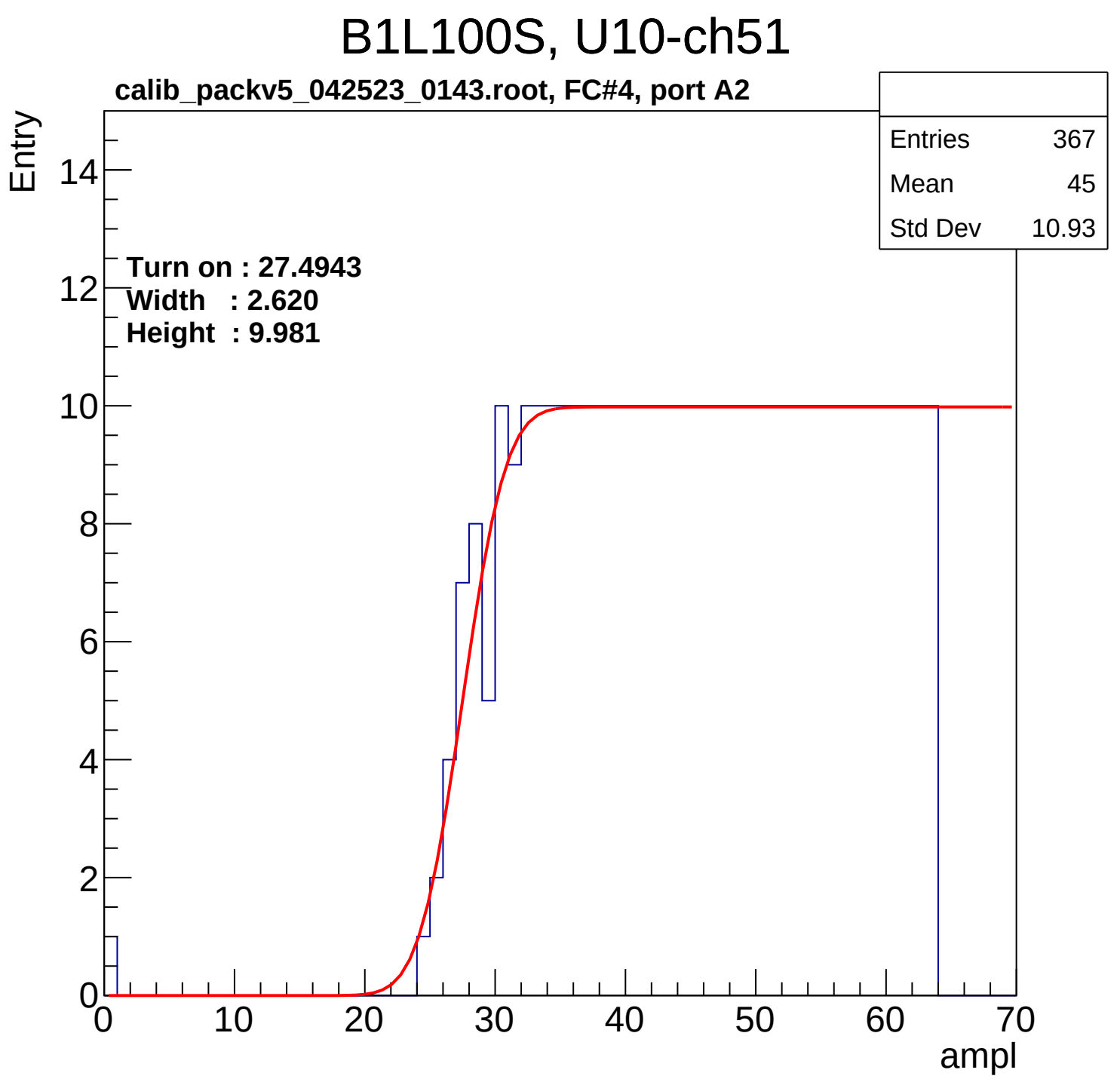
B1L100S, U10-ch51
calib_packv5_042523_0143.root, FC#4, port A2
Entries 367
Mean 45
Std Dev 10.93
Turn on : 27.4943
Width : 2.620
Height : 9.981
Entry
ampl
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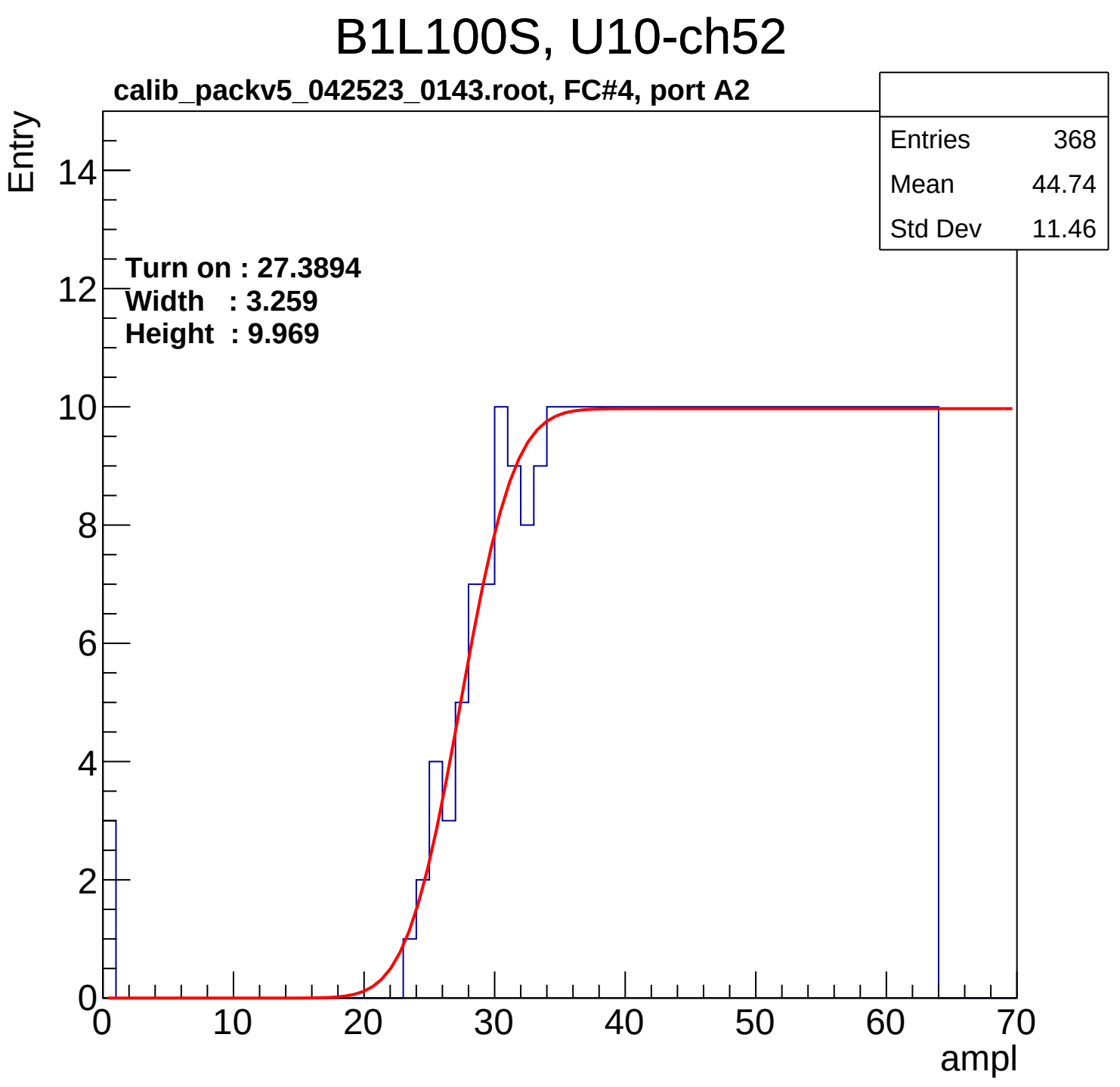
B1L100S, U10-ch52
calib_packv5_042523_0143.root, FC#4, port A2
Entries 368
Mean 44.74
Std Dev 11.46
Turn on : 27.3894
Width : 3.259
Height : 9.969
Entry
ampl
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6
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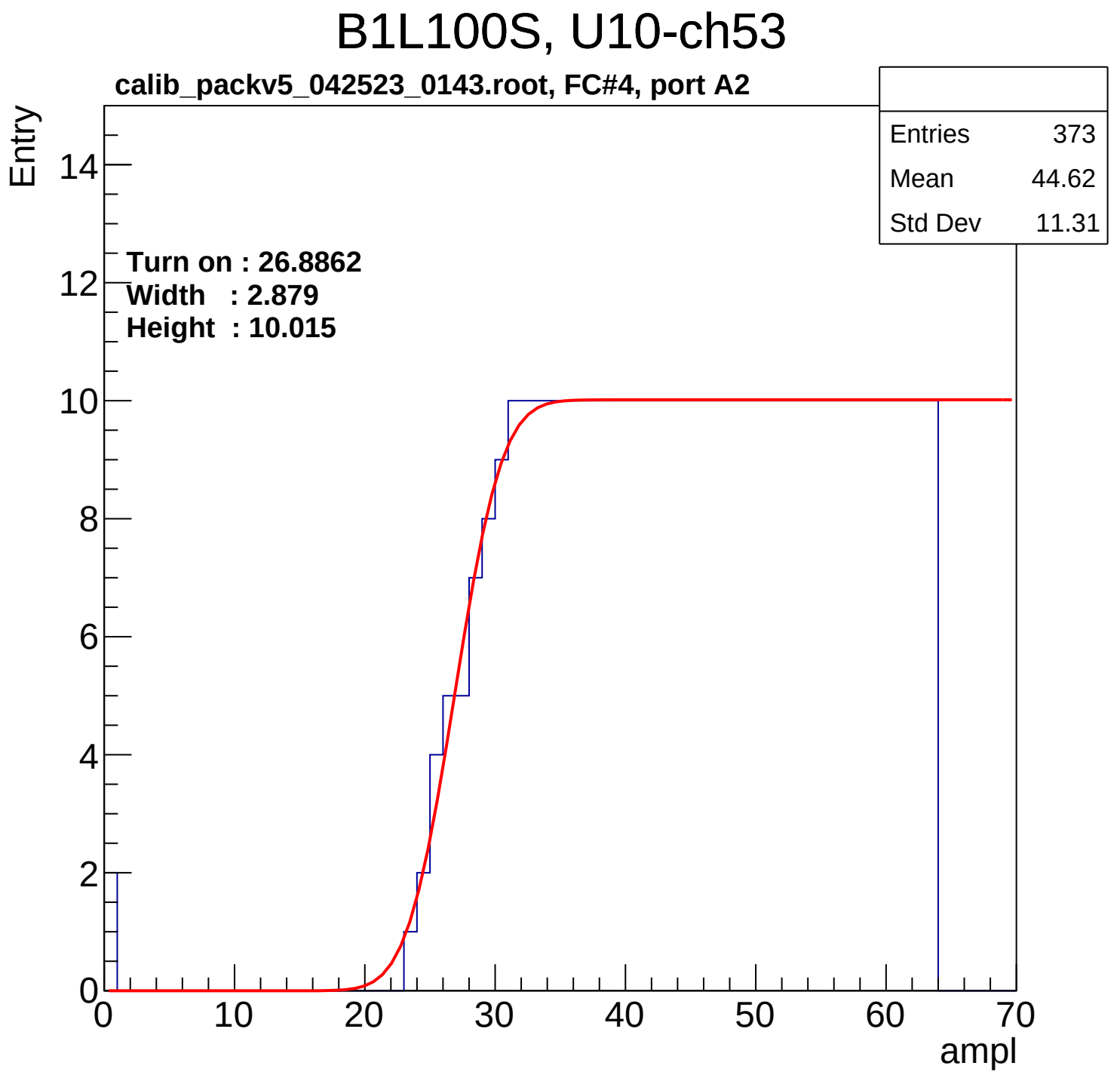
B1L100S, U10-ch53
calib_packv5_042523_0143.root, FC#4, port A2
Entries 373
Mean 44.62
Std Dev 11.31
Turn on : 26.8862
Width : 2.879
Height : 10.015
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ampl
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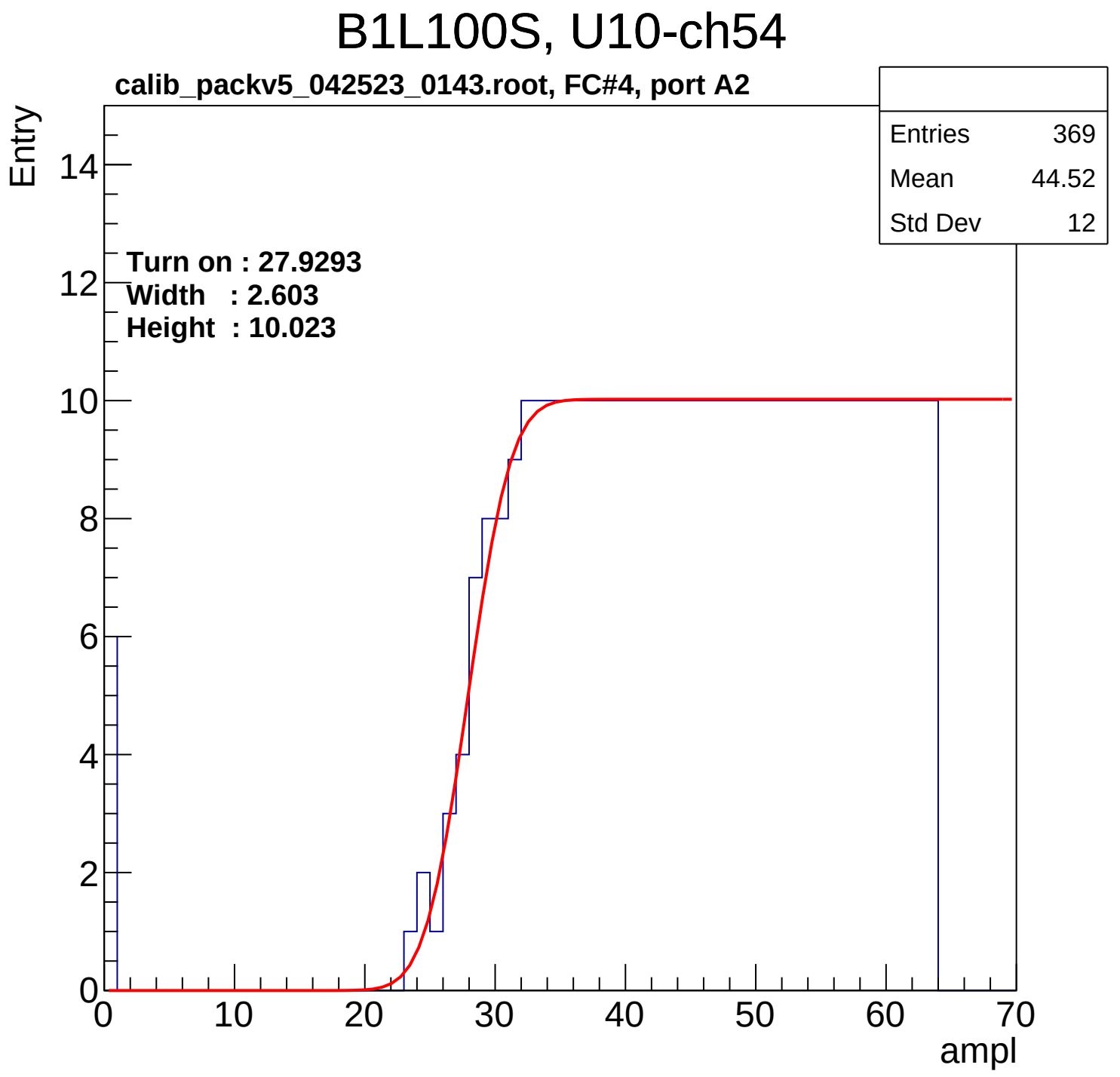
B1L100S, U10-ch54
calib_packv5_042523_0143.root, FC#4, port A2
Entries 369
Mean 44.52
Std Dev 12
Turn on : 27.9293
Width : 2.603
Height : 10.023
Entry
ampl
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4
6
8
10
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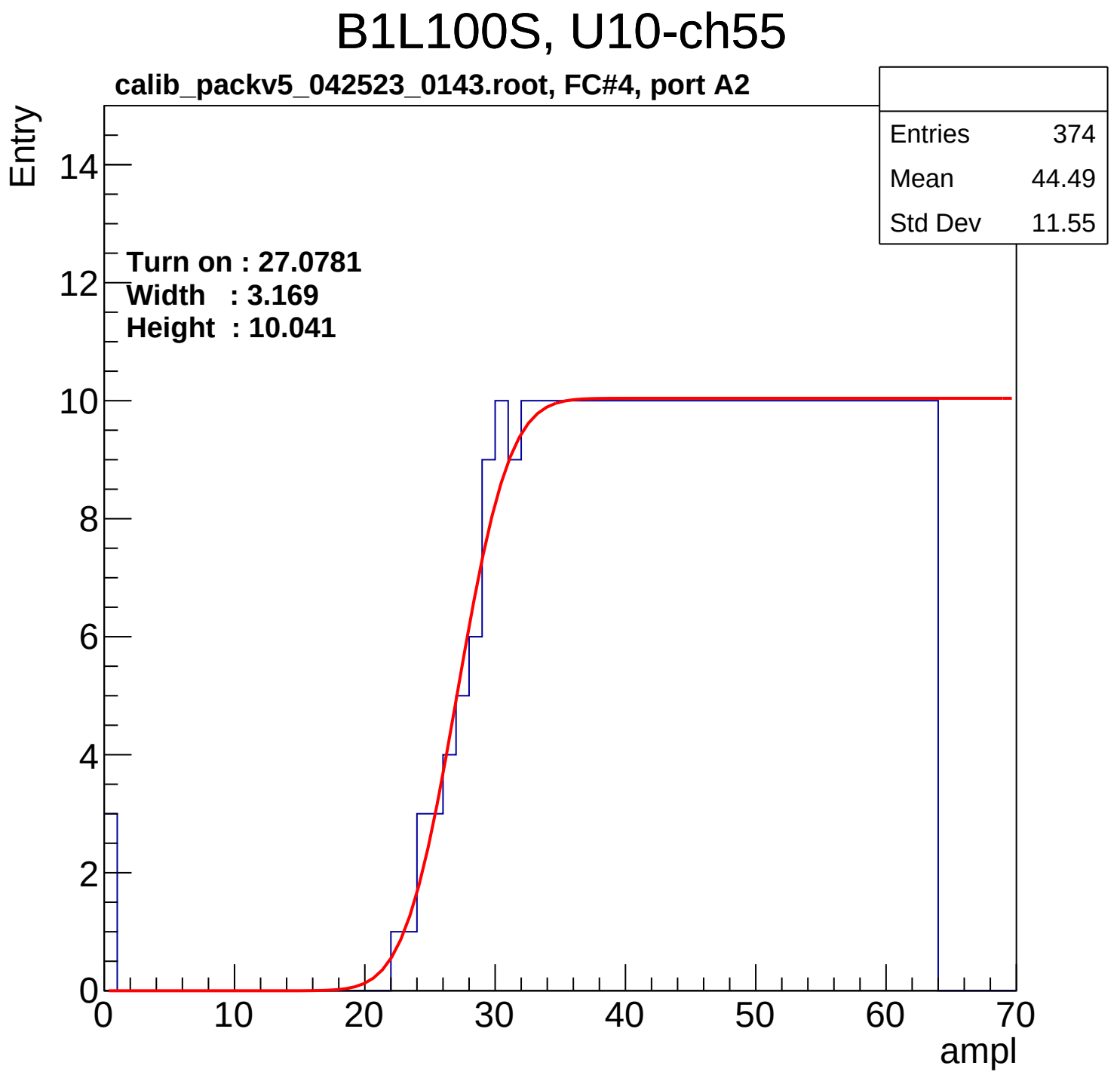
B1L100S, U10-ch55
calib_packv5_042523_0143.root, FC#4, port A2
Entries 374
Mean 44.49
Std Dev 11.55
Turn on : 27.0781
Width : 3.169
Height : 10.041
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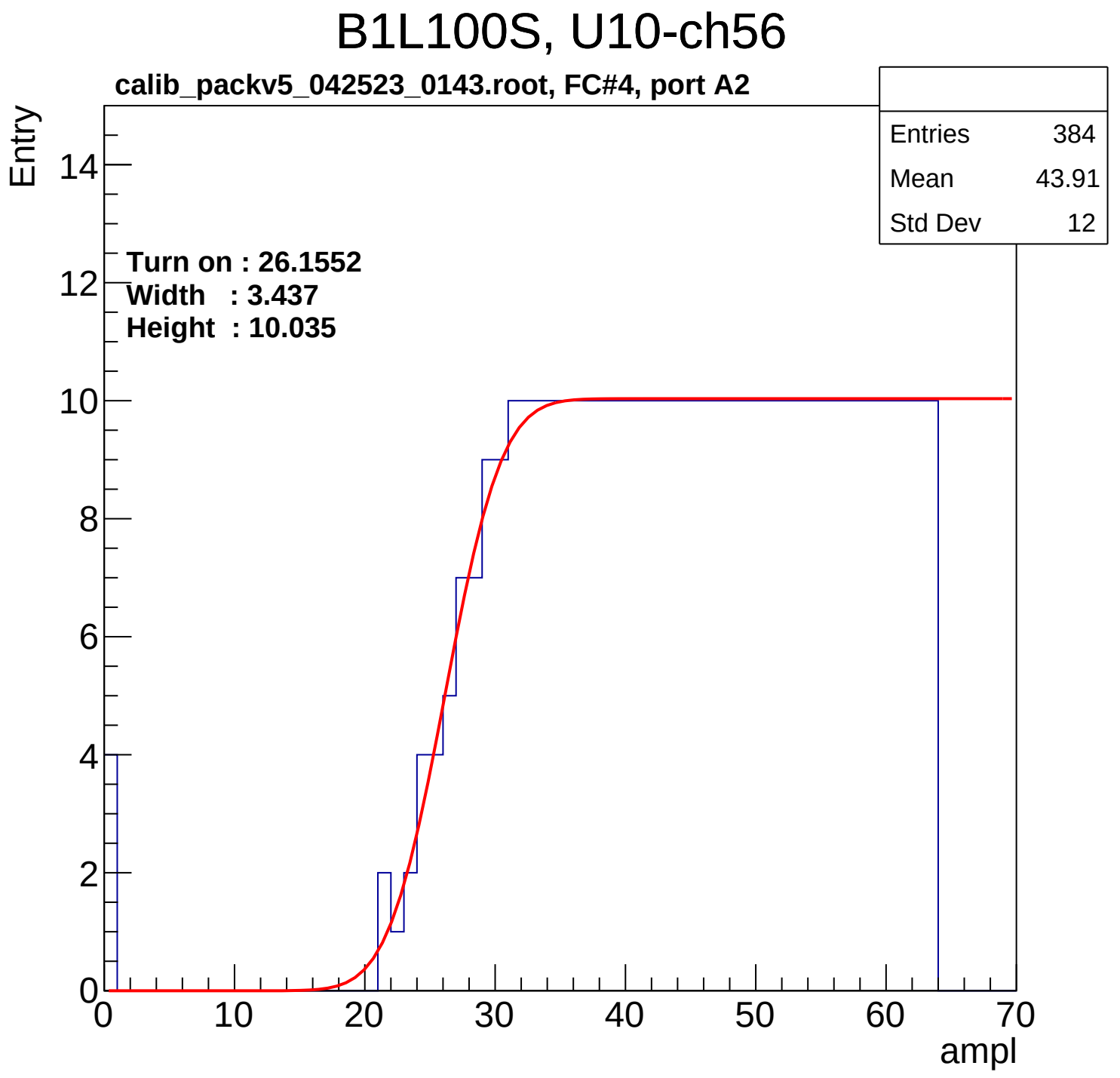
B1L100S, U10-ch56
calib_packv5_042523_0143.root, FC#4, port A2
Entries 384
Mean 43.91
Std Dev 12
Turn on : 26.1552
Width : 3.437
Height : 10.035
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ampl
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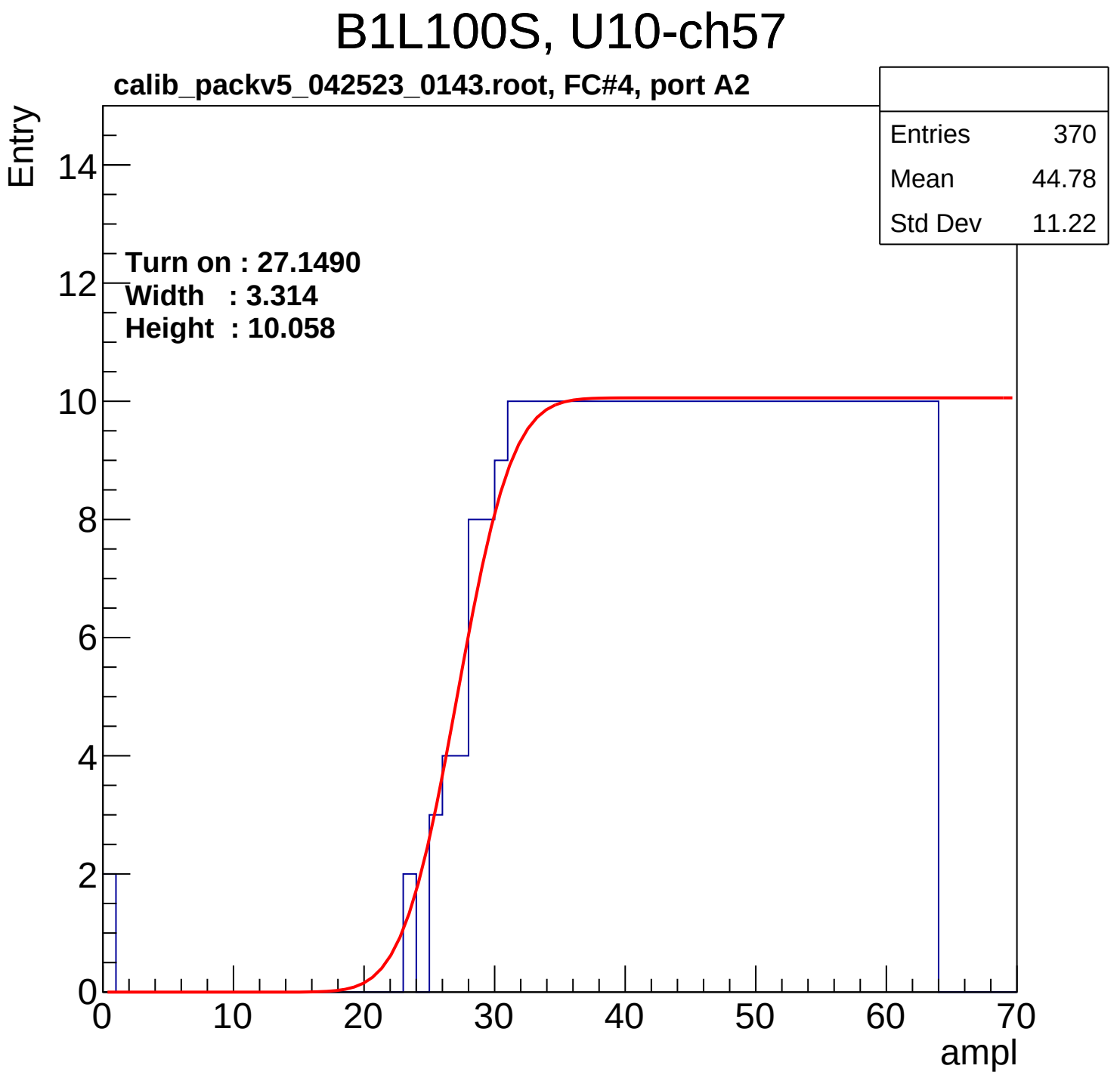
B1L100S, U10-ch57
calib_packv5_042523_0143.root, FC#4, port A2
Entries 370
Mean 44.78
Std Dev 11.22
Turn on : 27.1490
Width : 3.314
Height : 10.058
Entry
ampl
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6
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12
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10
20
30
40
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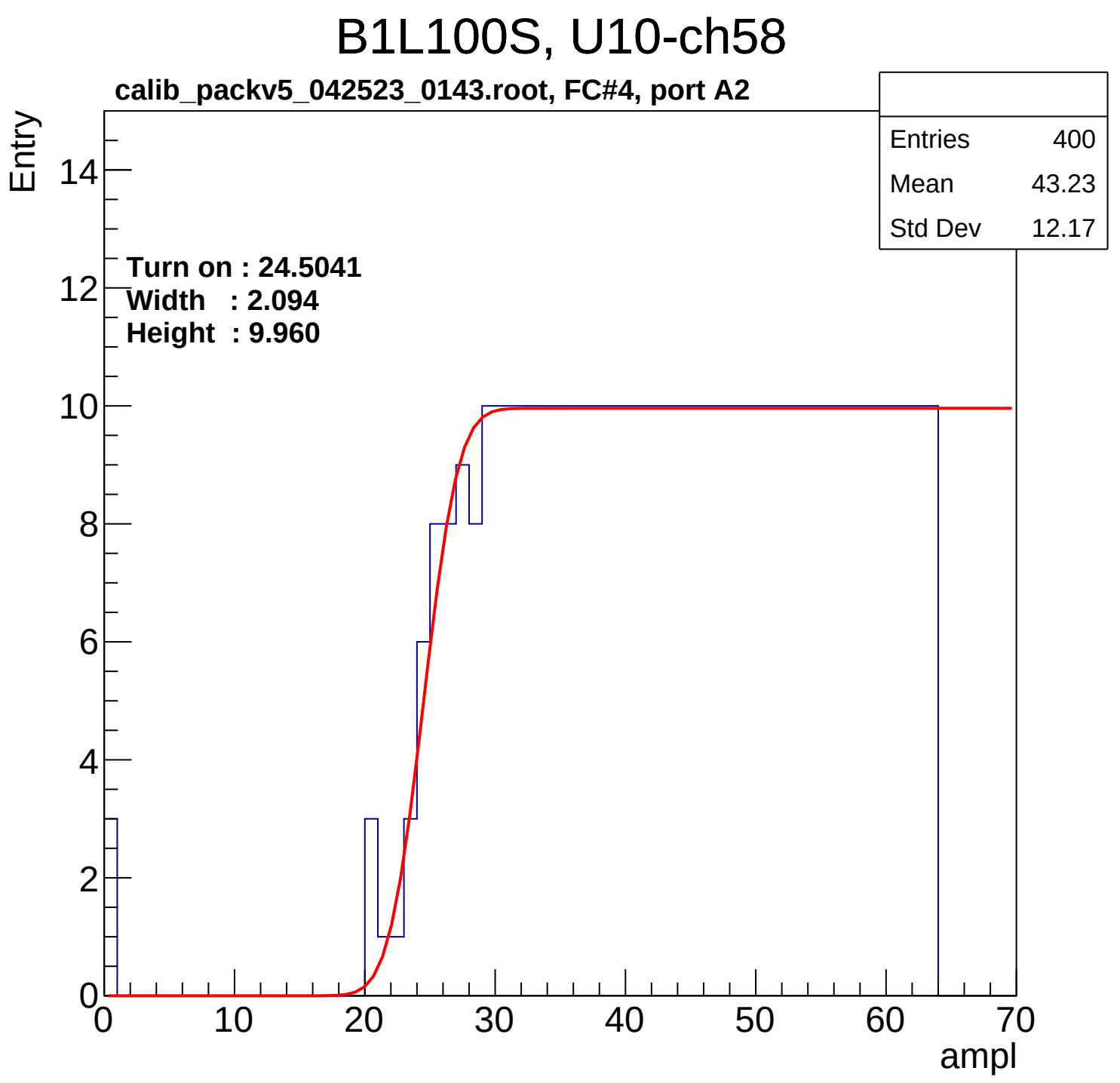
B1L100S, U10-ch58
calib_packv5_042523_0143.root, FC#4, port A2
Entries 400
Mean 43.23
Std Dev 12.17
Turn on : 24.5041
Width : 2.094
Height : 9.960
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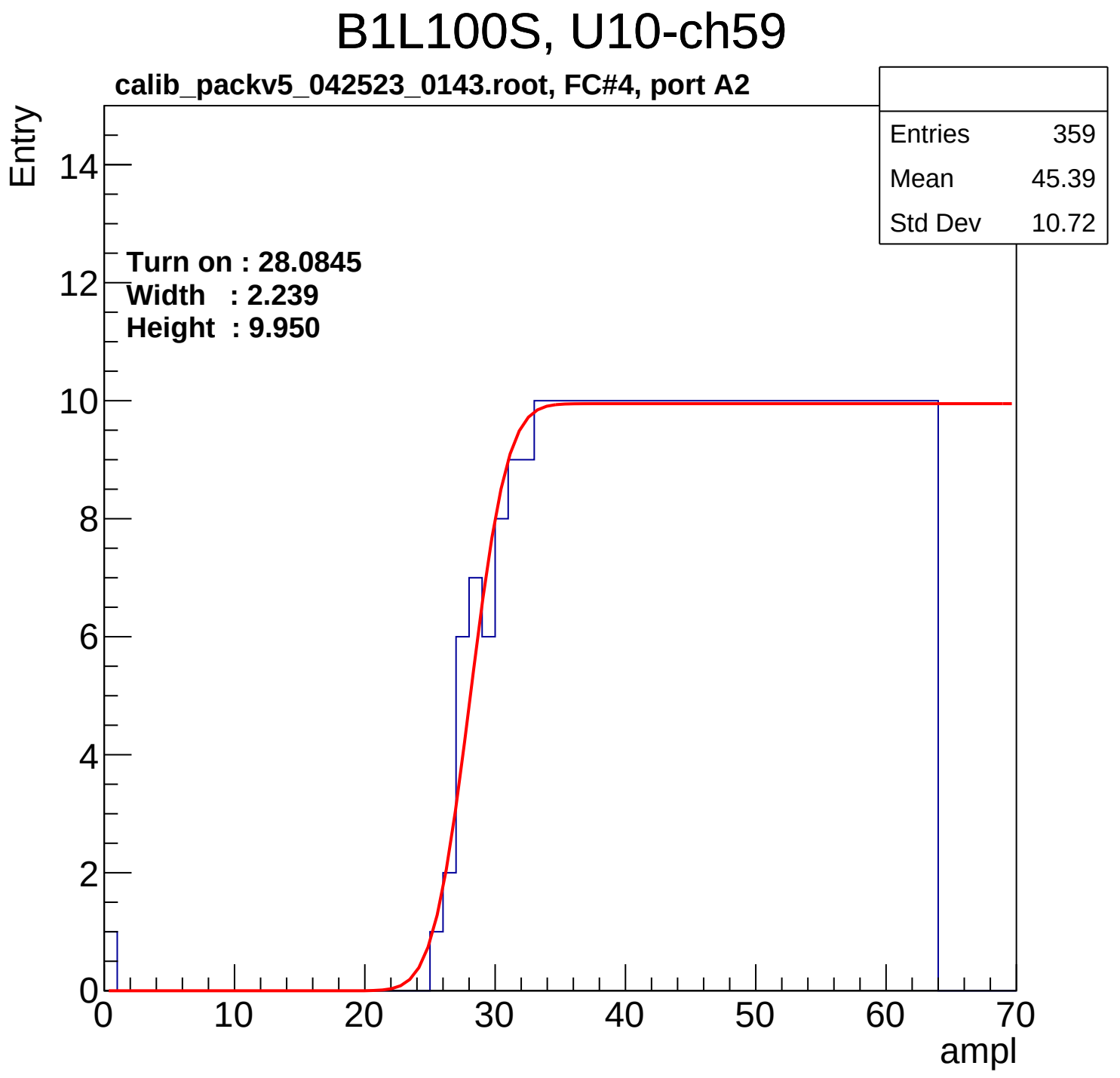
B1L100S, U10-ch59
calib_packv5_042523_0143.root, FC#4, port A2
Entries 359
Mean 45.39
Std Dev 10.72
Turn on : 28.0845
Width : 2.239
Height : 9.950
Entry
ampl
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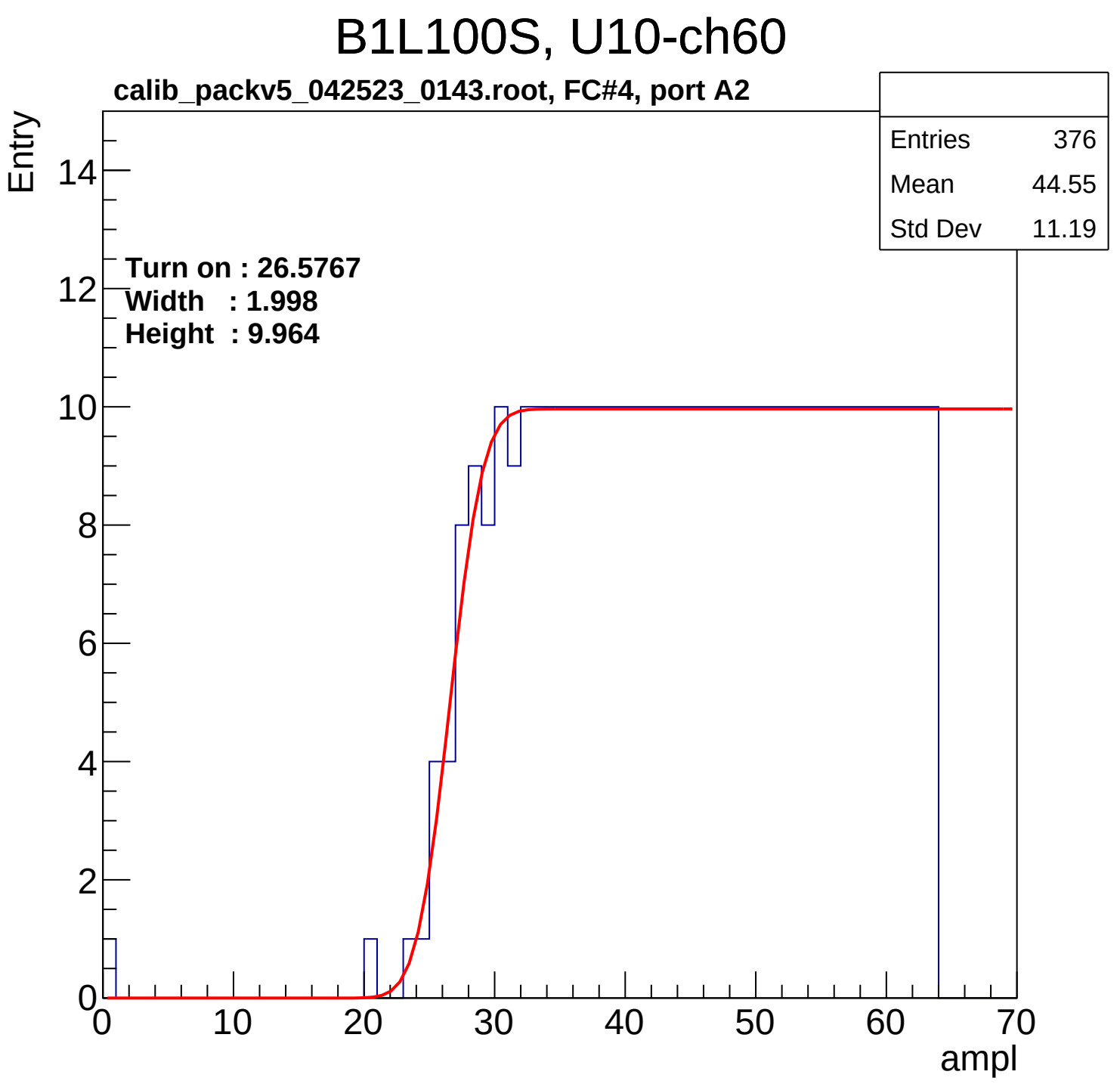
B1L100S, U10-ch60
calib_packv5_042523_0143.root, FC#4, port A2
Entries 376
Mean 44.55
Std Dev 11.19
Turn on : 26.5767
Width : 1.998
Height : 9.964
Entry
ampl
0
2
4
6
8
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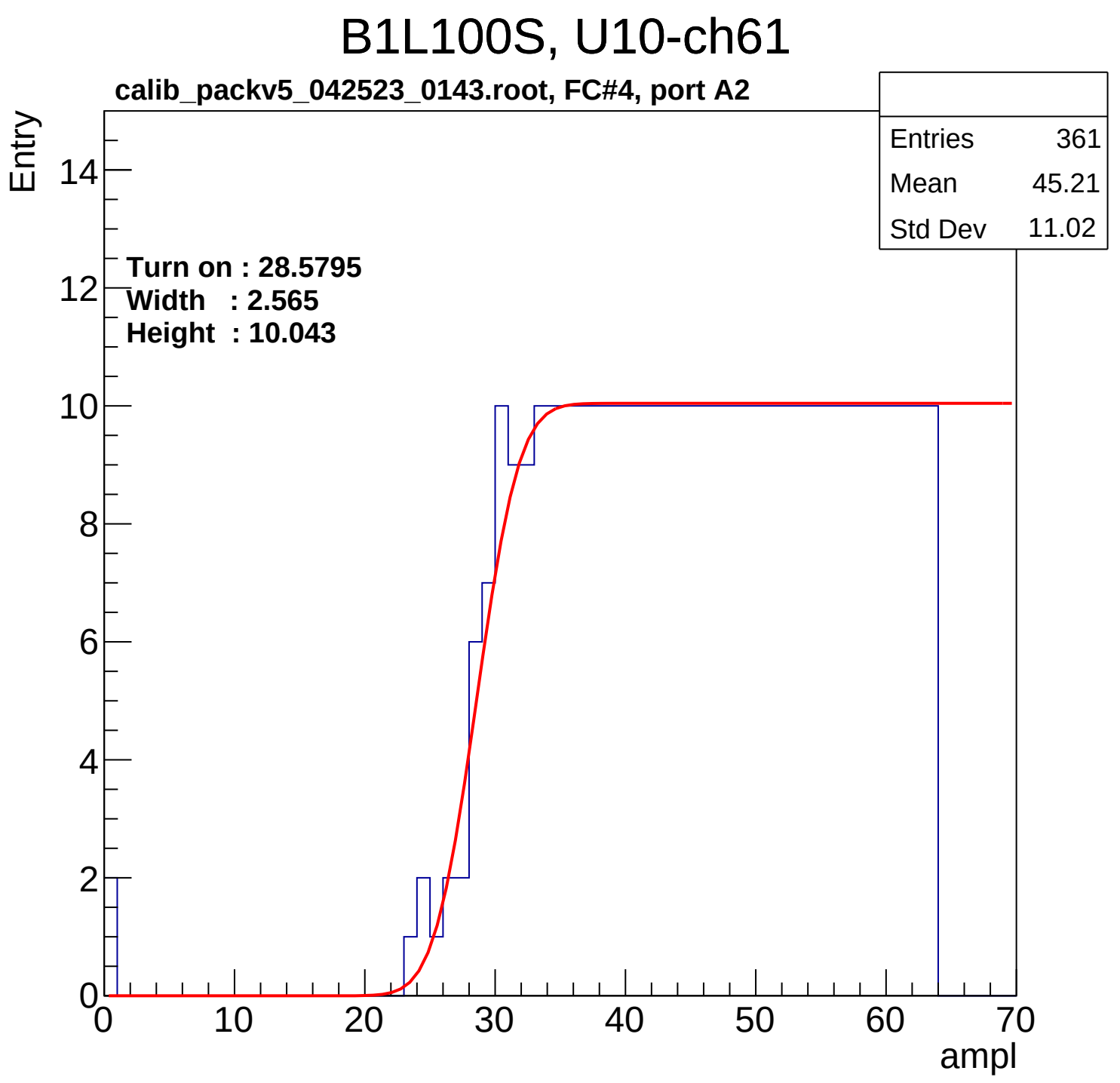
B1L100S, U10-ch61
calib_packv5_042523_0143.root, FC#4, port A2
Entries 361
Mean 45.21
Std Dev 11.02
Turn on : 28.5795
Width : 2.565
Height : 10.043
Entry
ampl
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2
4
6
8
10
12
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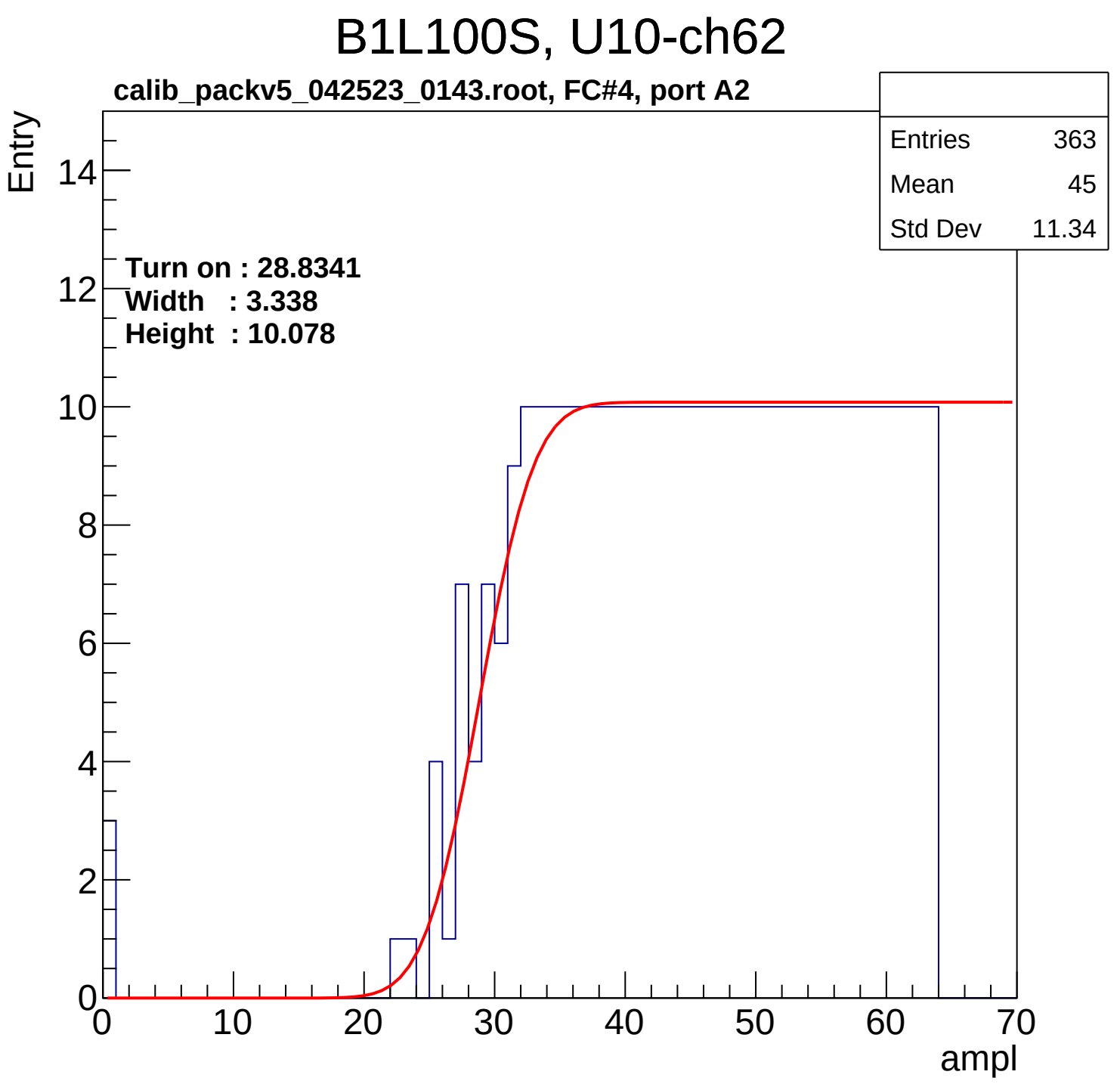
B1L100S, U10-ch62
calib_packv5_042523_0143.root, FC#4, port A2
Entries 363
Mean 45
Std Dev 11.34
Turn on : 28.8341
Width : 3.338
Height : 10.078
Entry
ampl
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2
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6
8
10
12
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0
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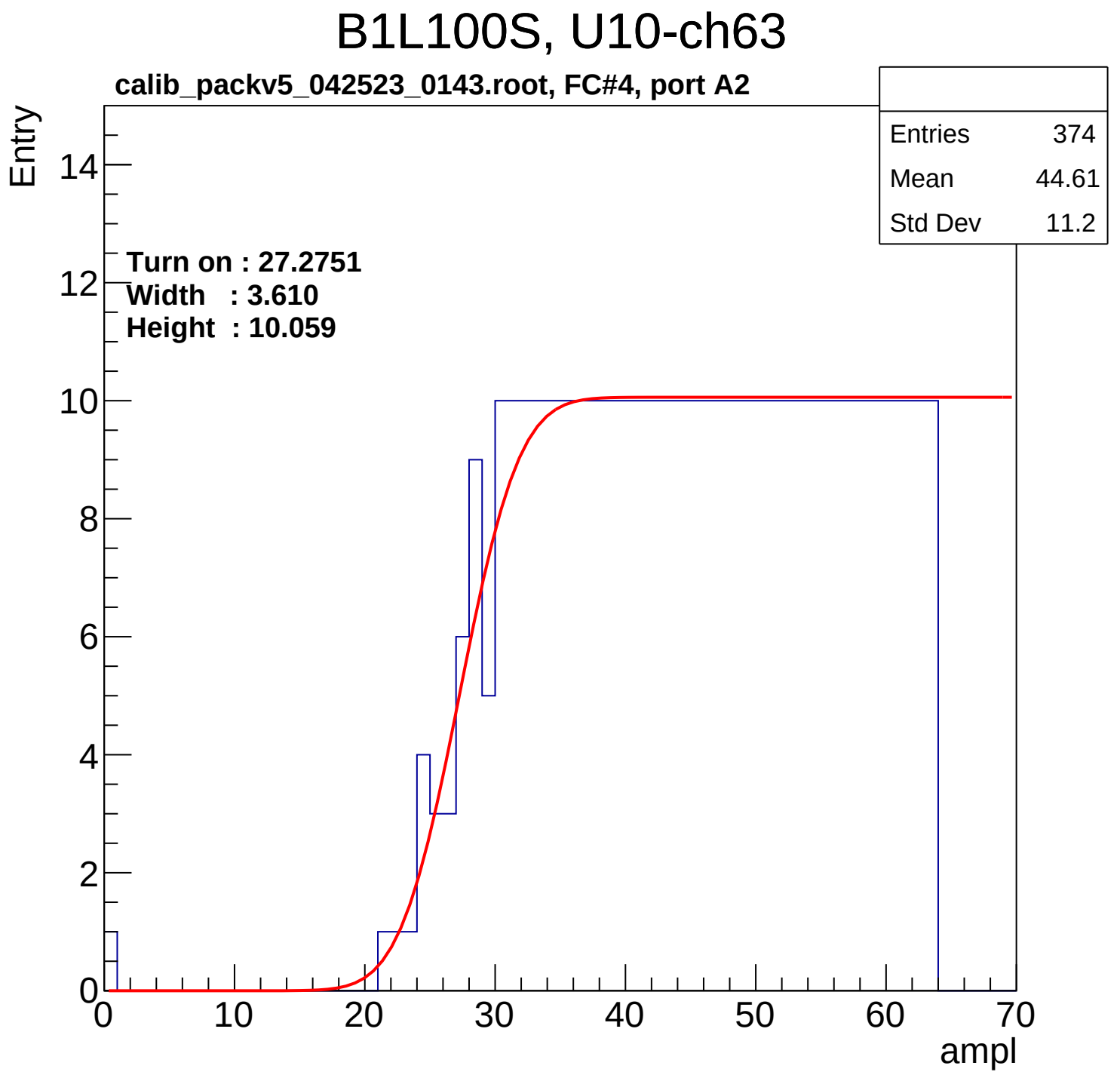
B1L100S, U10-ch63
calib_packv5_042523_0143.root, FC#4, port A2
Entries 374
Mean 44.61
Std Dev 11.2
Turn on : 27.2751
Width : 3.610
Height : 10.059
Entry
ampl
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2
4
6
8
10
12
14
0
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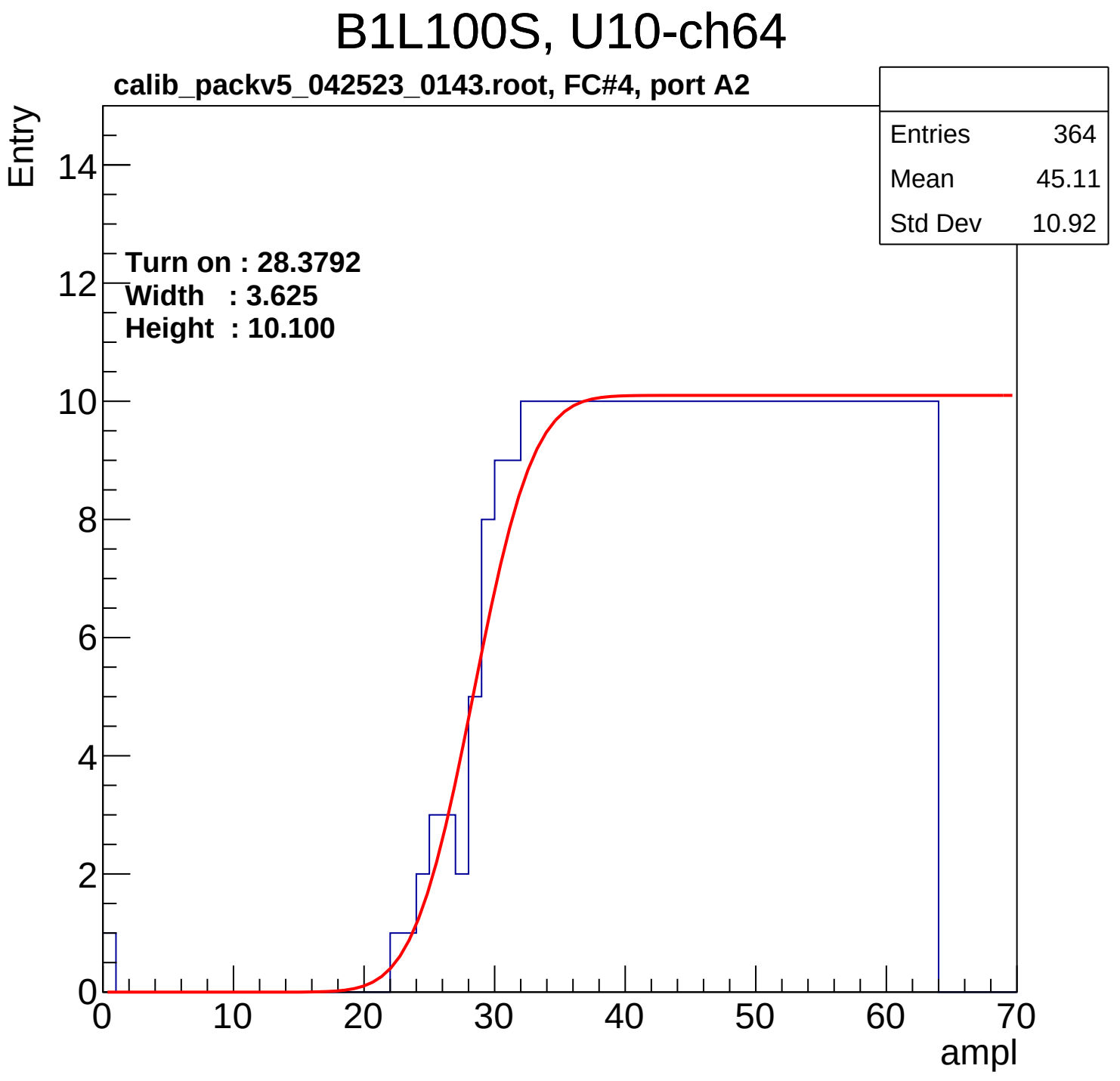
B1L100S, U10-ch64
calib_packv5_042523_0143.root, FC#4, port A2
Entries 364
Mean 45.11
Std Dev 10.92
Turn on : 28.3792
Width : 3.625
Height : 10.100
Entry
ampl
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2
4
6
8
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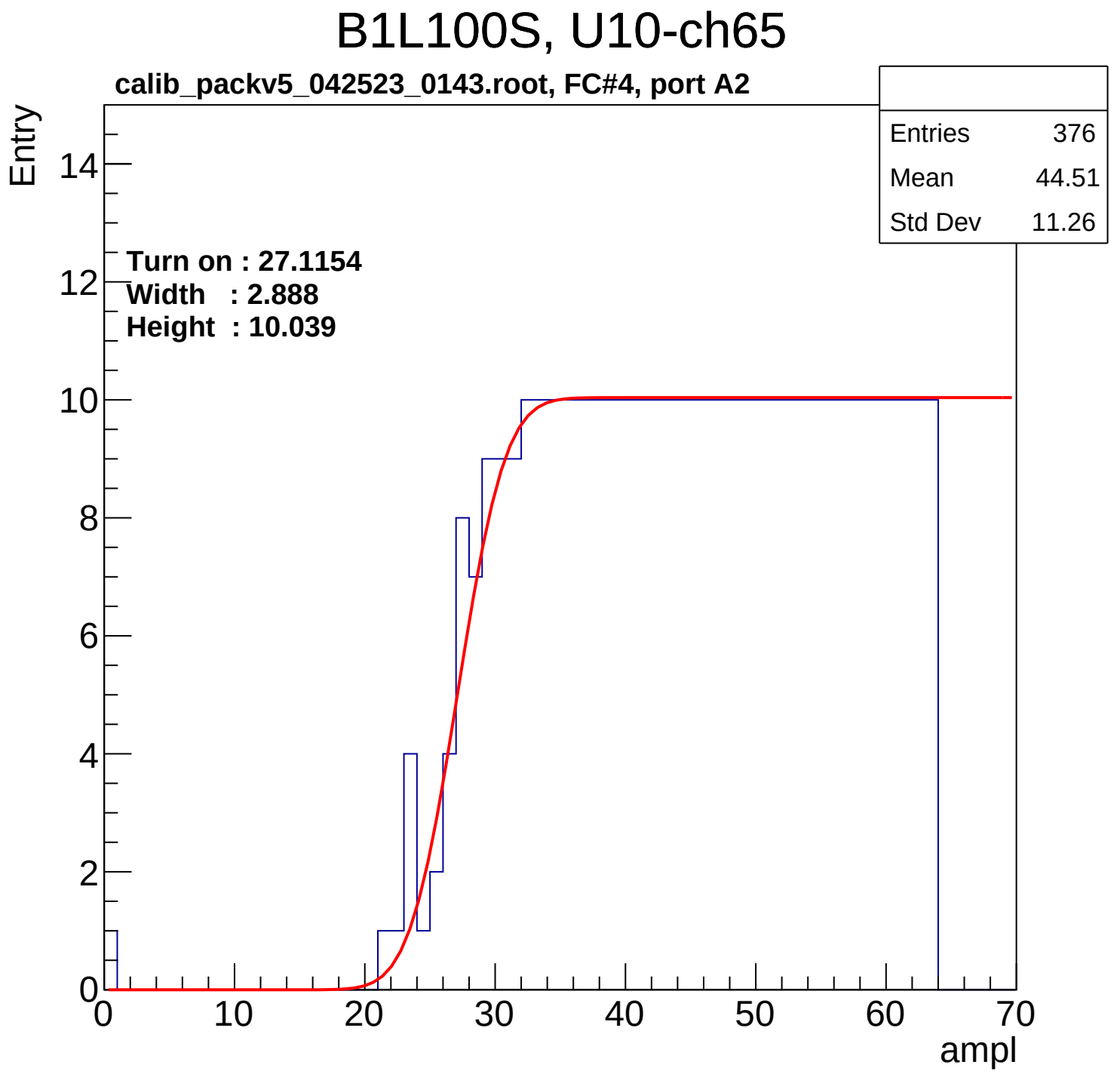
B1L100S, U10-ch65
calib_packv5_042523_0143.root, FC#4, port A2
Entries 376
Mean 44.51
Std Dev 11.26
Turn on : 27.1154
Width : 2.888
Height : 10.039
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
50
60
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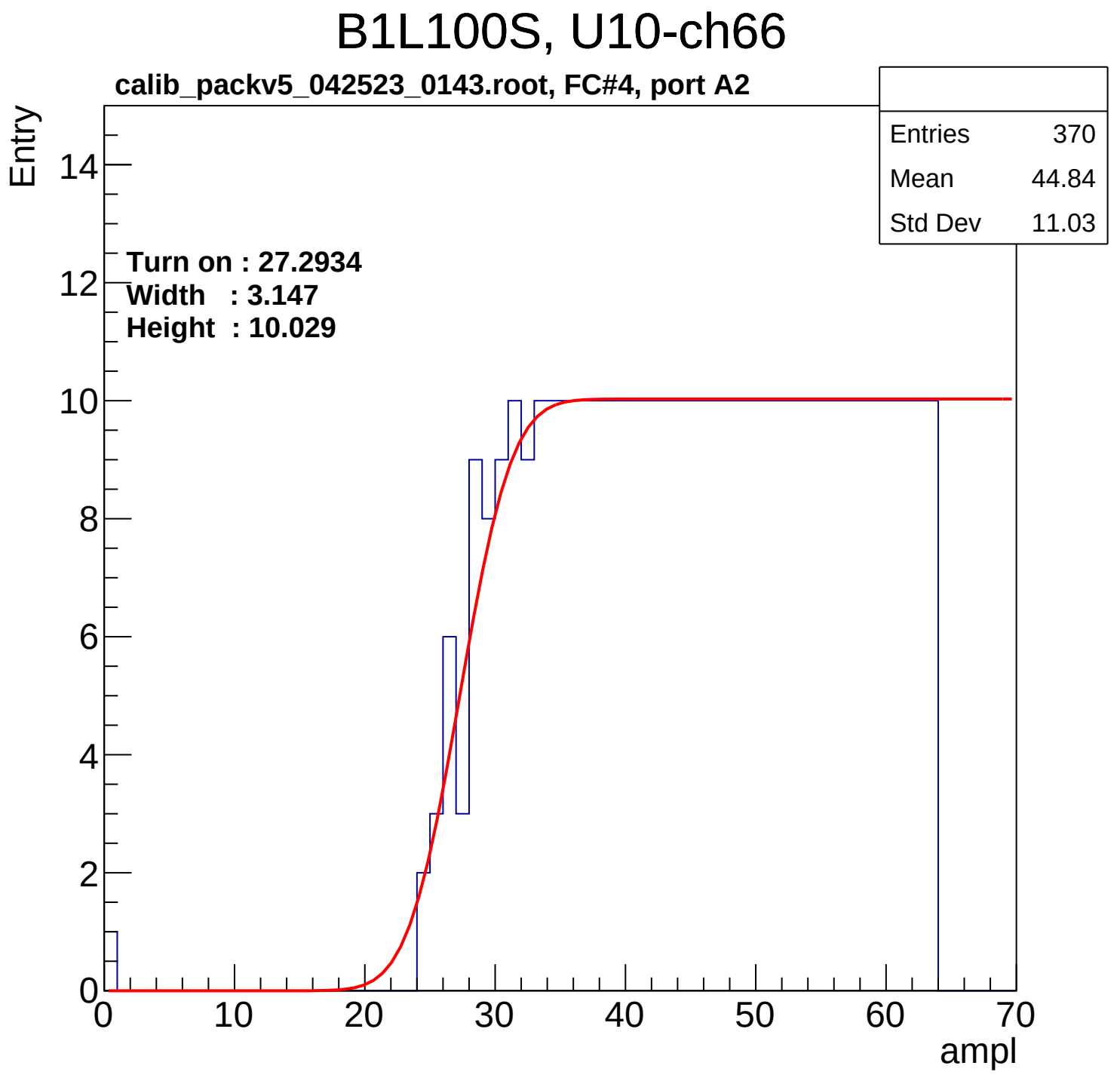
B1L100S, U10-ch66
calib_packv5_042523_0143.root, FC#4, port A2
Entries 370
Mean 44.84
Std Dev 11.03
Turn on : 27.2934
Width : 3.147
Height : 10.029
Entry
ampl
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2
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6
8
10
12
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60
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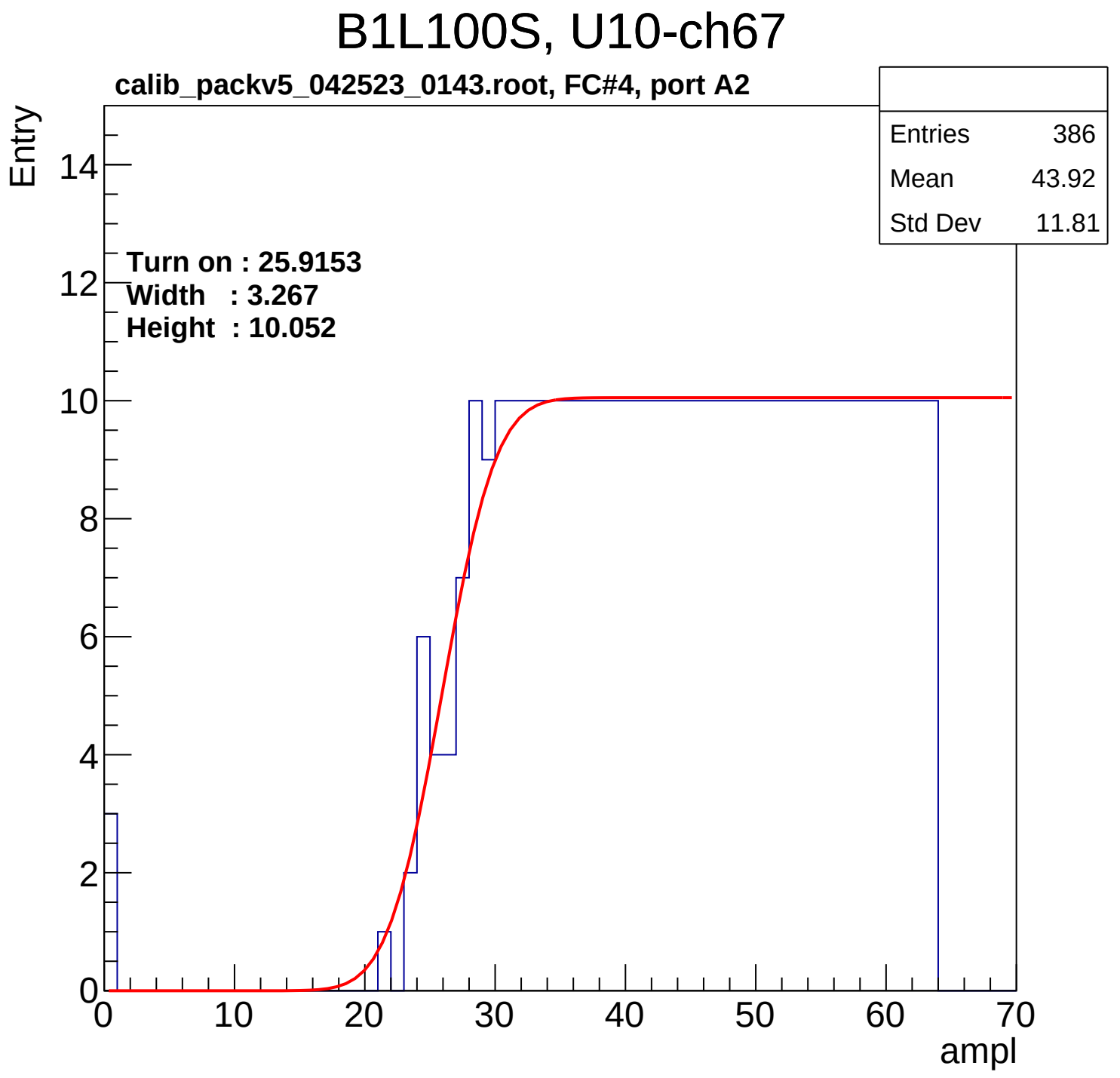
B1L100S, U10-ch67
calib_packv5_042523_0143.root, FC#4, port A2
Entries 386
Mean 43.92
Std Dev 11.81
Turn on : 25.9153
Width : 3.267
Height : 10.052
Entry
ampl
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6
8
10
12
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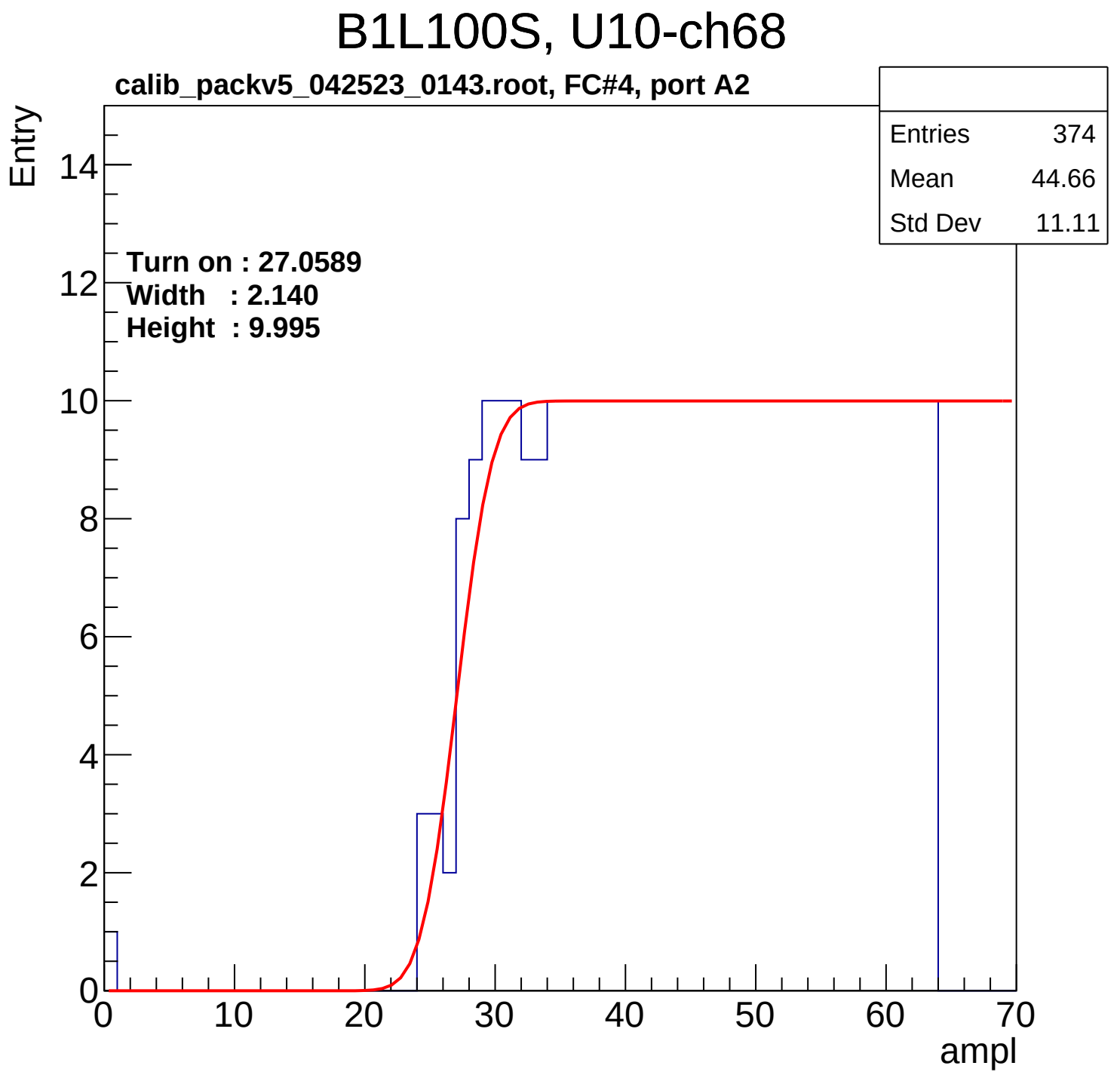
B1L100S, U10-ch68
calib_packv5_042523_0143.root, FC#4, port A2
Entries 374
Mean 44.66
Std Dev 11.11
Turn on : 27.0589
Width : 2.140
Height : 9.995
Entry
ampl
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6
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0
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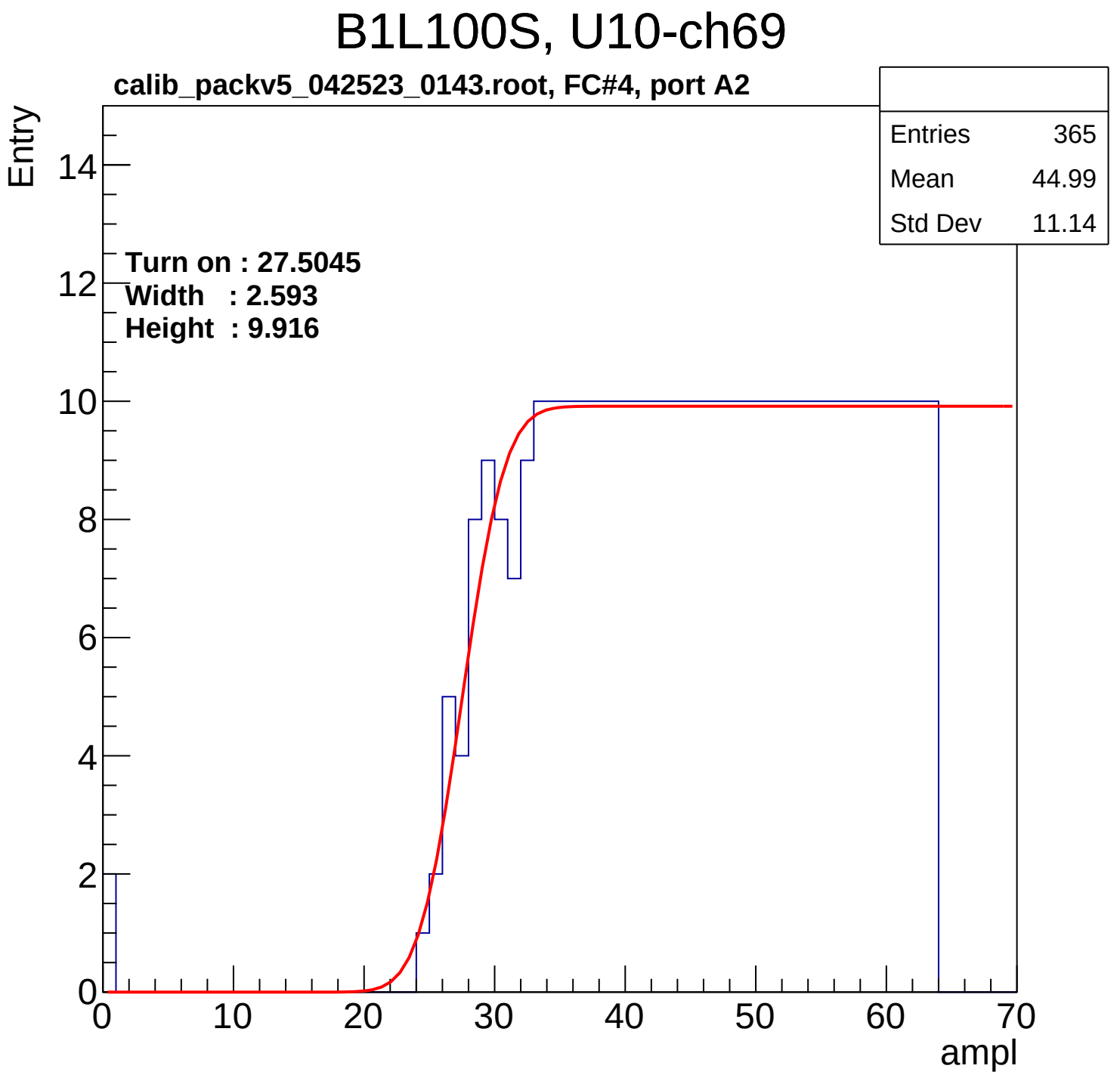
B1L100S, U10-ch69
calib_packv5_042523_0143.root, FC#4, port A2
Entries 365
Mean 44.99
Std Dev 11.14
Turn on : 27.5045
Width : 2.593
Height : 9.916
Entry
ampl
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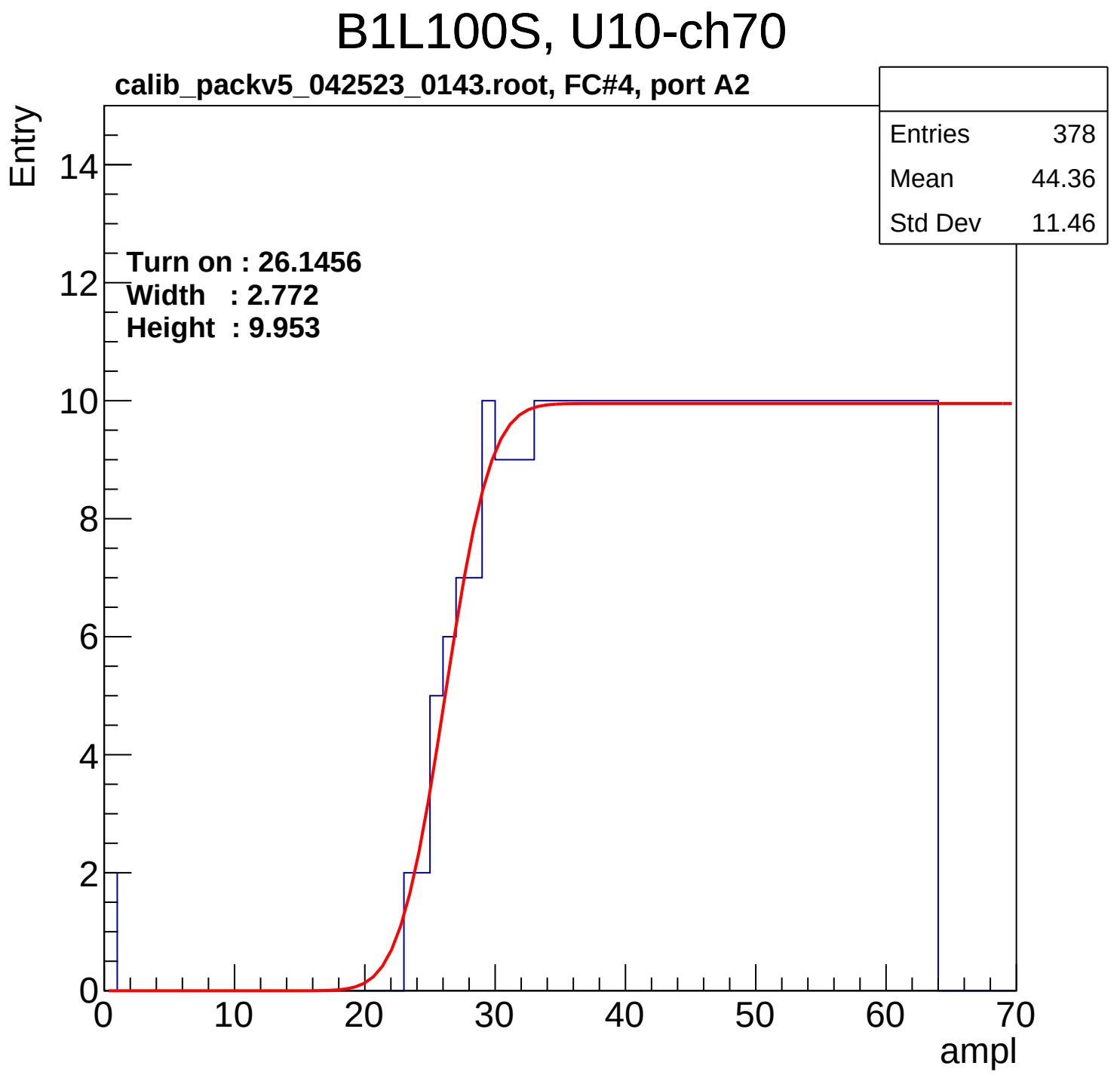
B1L100S, U10-ch70
calib_packv5_042523_0143.root, FC#4, port A2
Entries 378
Mean 44.36
Std Dev 11.46
Turn on : 26.1456
Width : 2.772
Height : 9.953
Entry
ampl
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6
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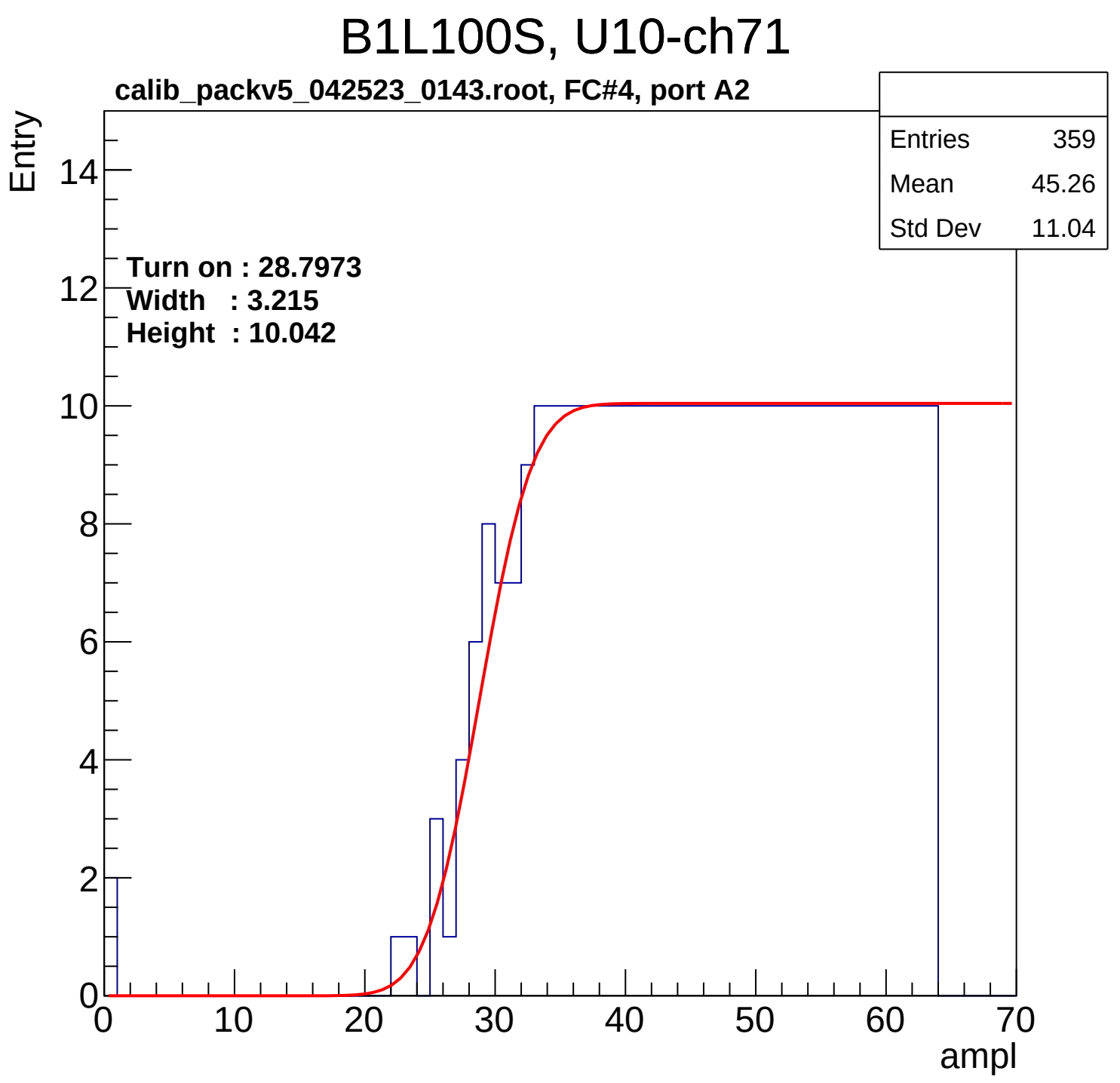
B1L100S, U10-ch71
calib_packv5_042523_0143.root, FC#4, port A2
Entries 359
Mean 45.26
Std Dev 11.04
Turn on : 28.7973
Width : 3.215
Height : 10.042
Entry
ampl
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6
8
10
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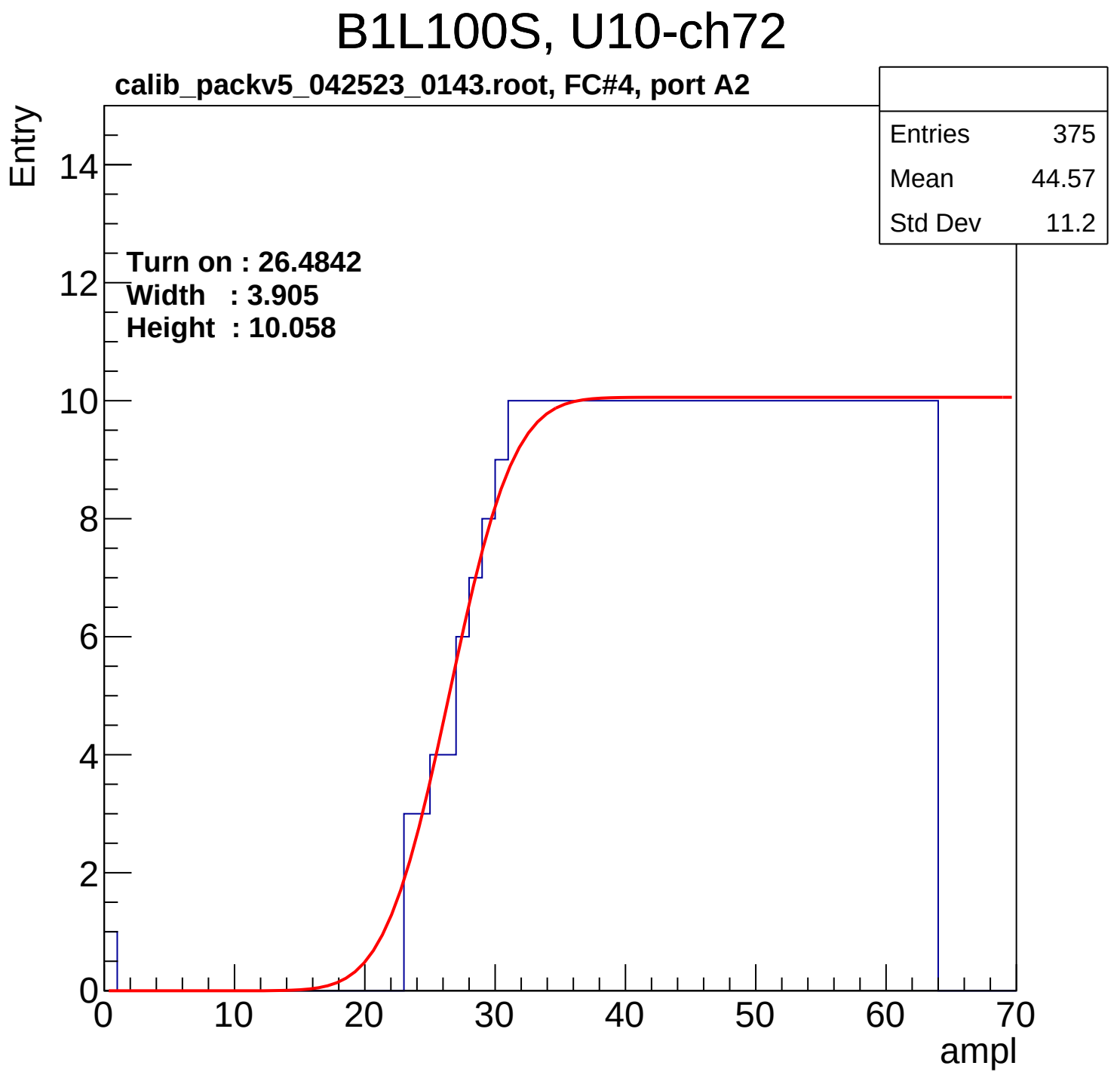
B1L100S, U10-ch72
calib_packv5_042523_0143.root, FC#4, port A2
Entries 375
Mean 44.57
Std Dev 11.2
Turn on : 26.4842
Width : 3.905
Height : 10.058
Entry
ampl
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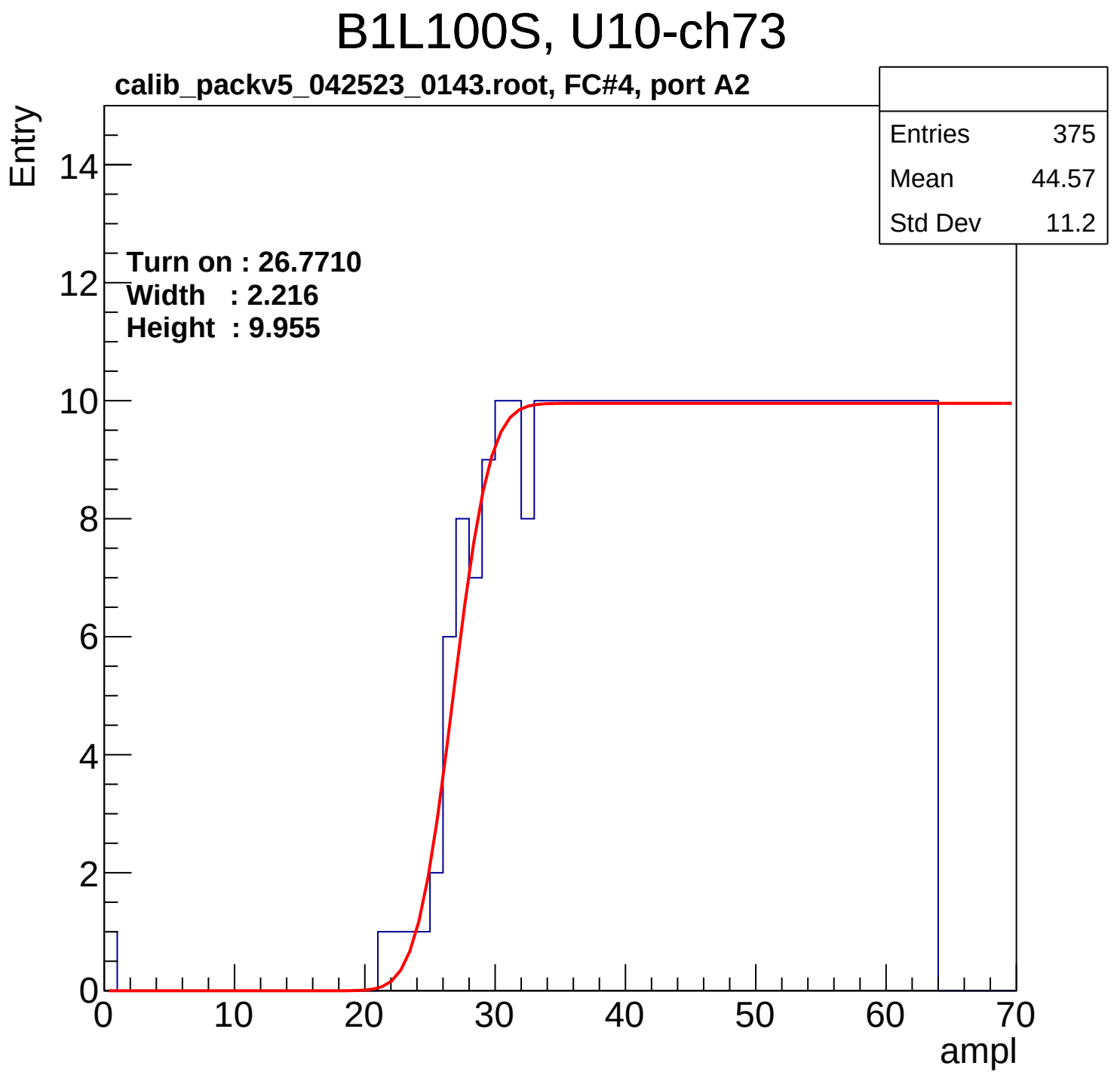
B1L100S, U10-ch73
calib_packv5_042523_0143.root, FC#4, port A2
Entries 375
Mean 44.57
Std Dev 11.2
Turn on : 26.7710
Width : 2.216
Height : 9.955
Entry
ampl
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8
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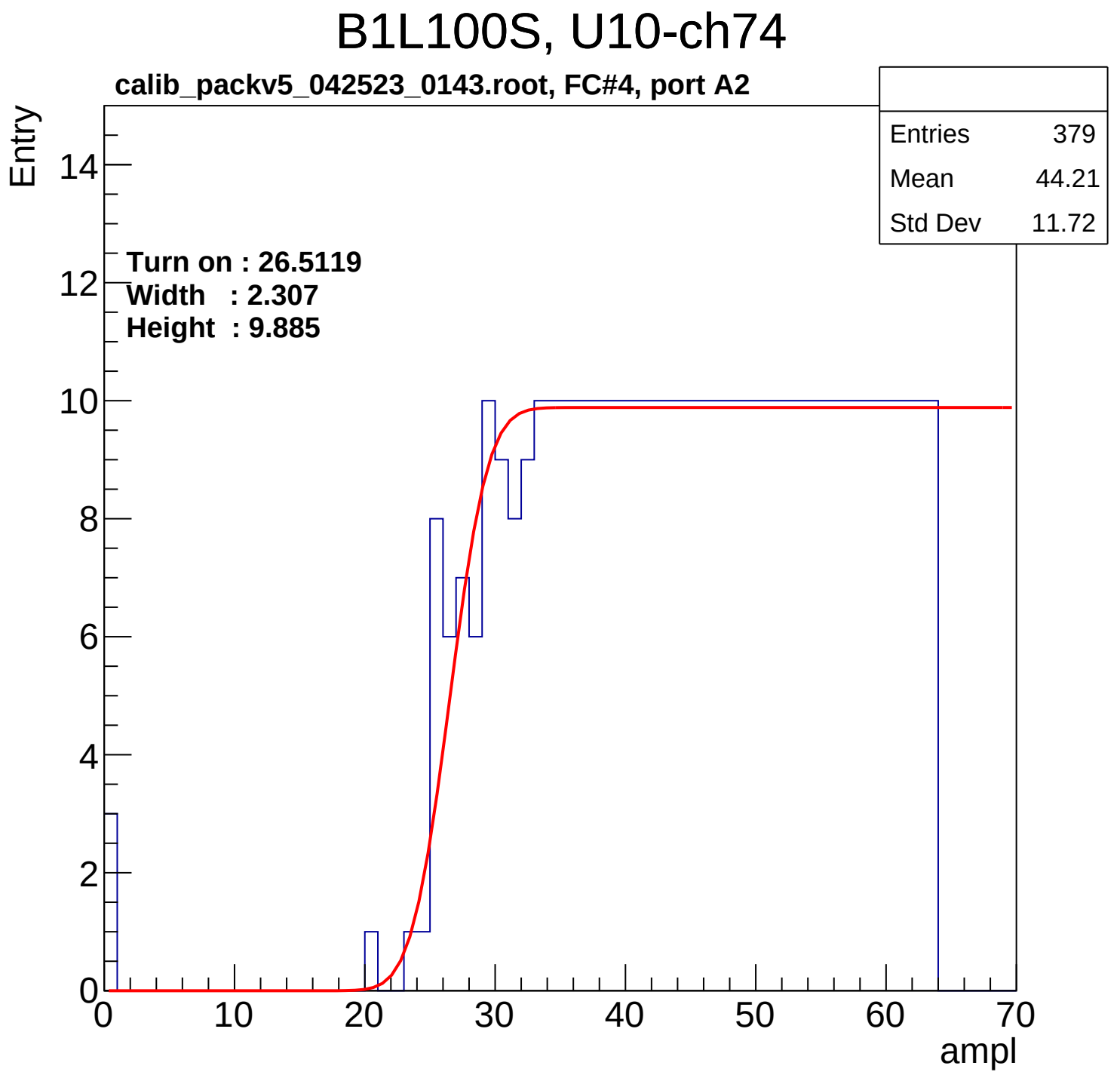
B1L100S, U10-ch74
calib_packv5_042523_0143.root, FC#4, port A2
Entries 379
Mean 44.21
Std Dev 11.72
Turn on : 26.5119
Width : 2.307
Height : 9.885
Entry
ampl
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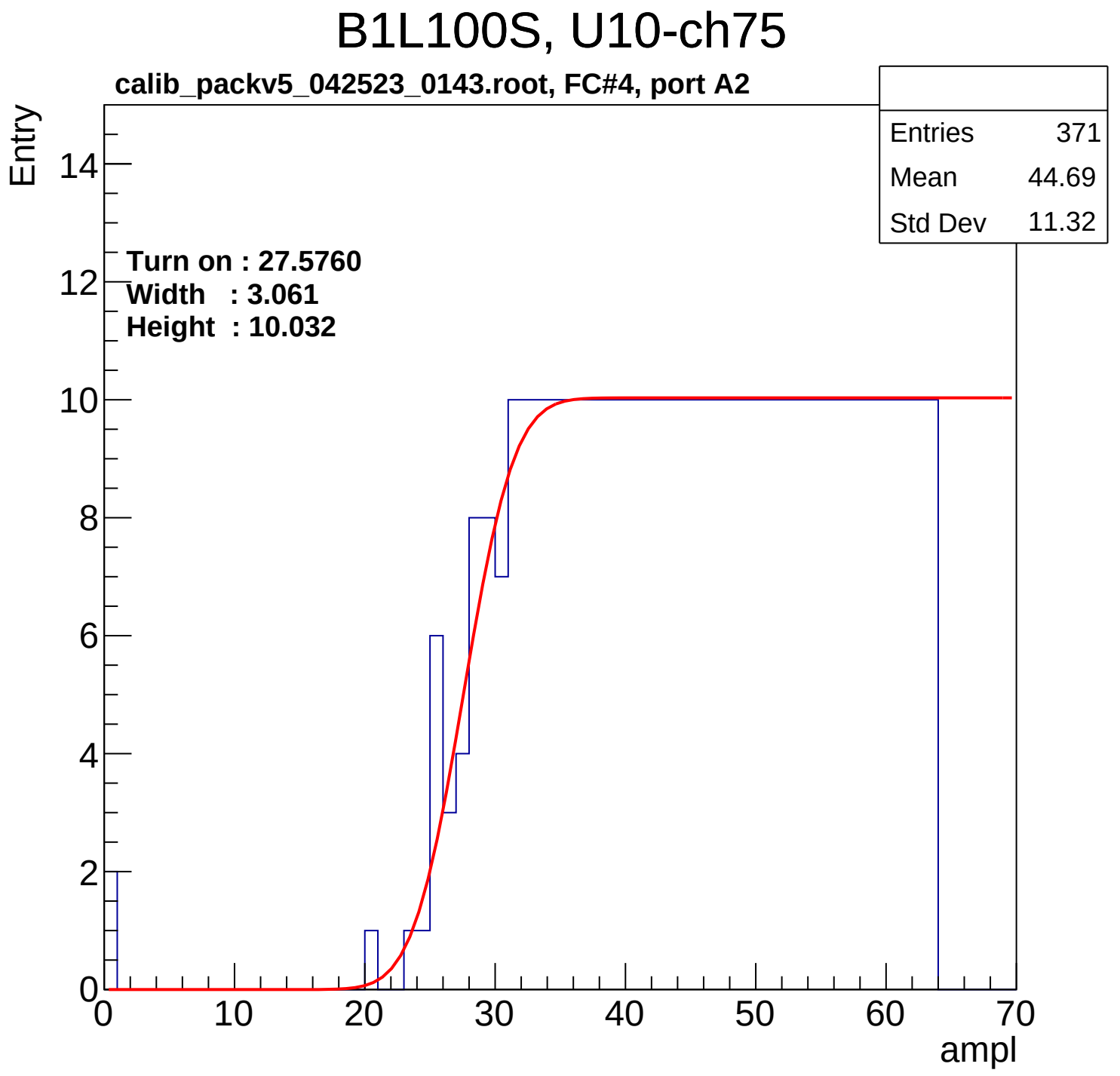
B1L100S, U10-ch75
calib_packv5_042523_0143.root, FC#4, port A2
Entries 371
Mean 44.69
Std Dev 11.32
Turn on : 27.5760
Width : 3.061
Height : 10.032
Entry
ampl
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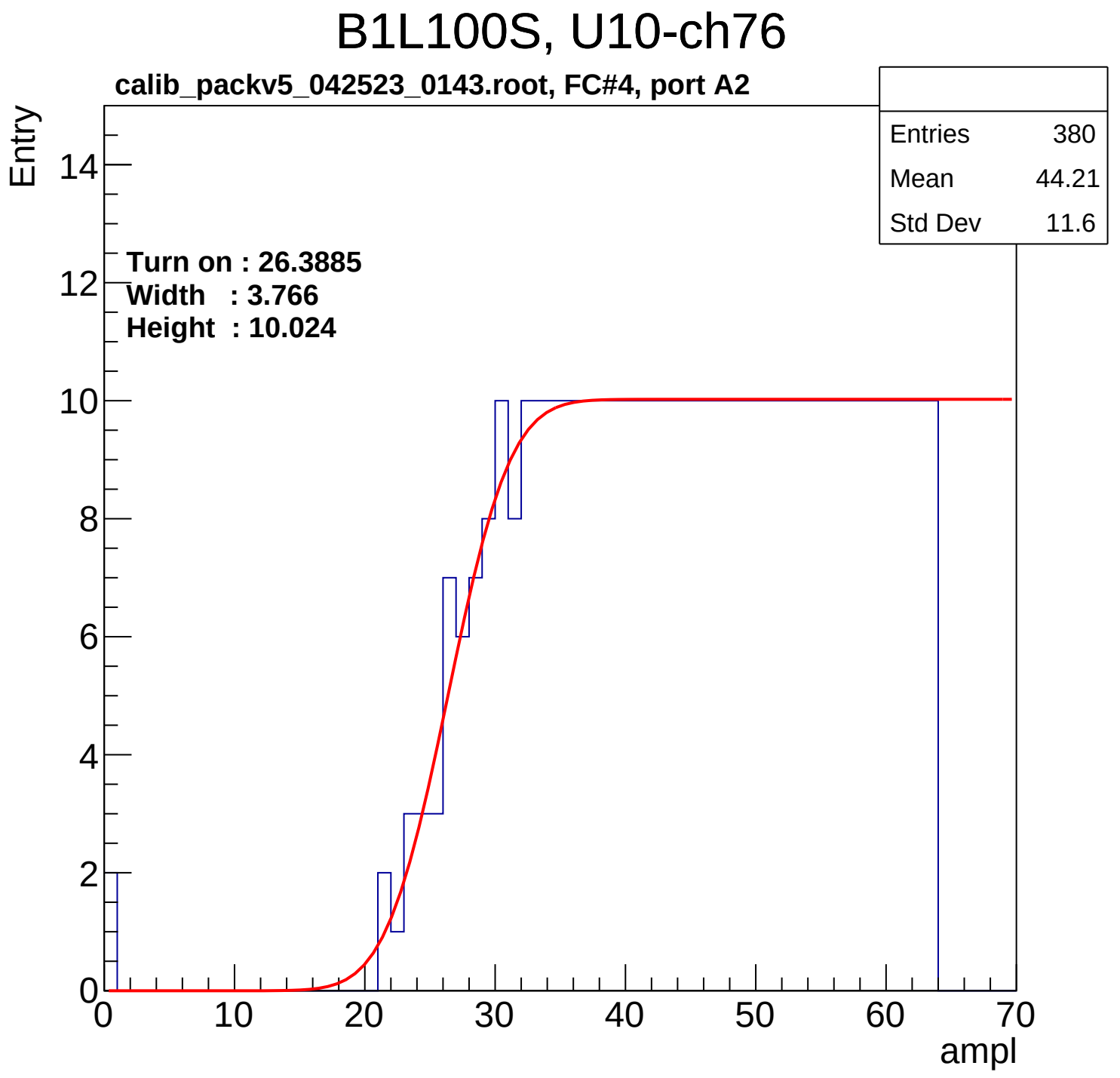
B1L100S, U10-ch76
calib_packv5_042523_0143.root, FC#4, port A2
Entries 380
Mean 44.21
Std Dev 11.6
Turn on : 26.3885
Width : 3.766
Height : 10.024
Entry
ampl
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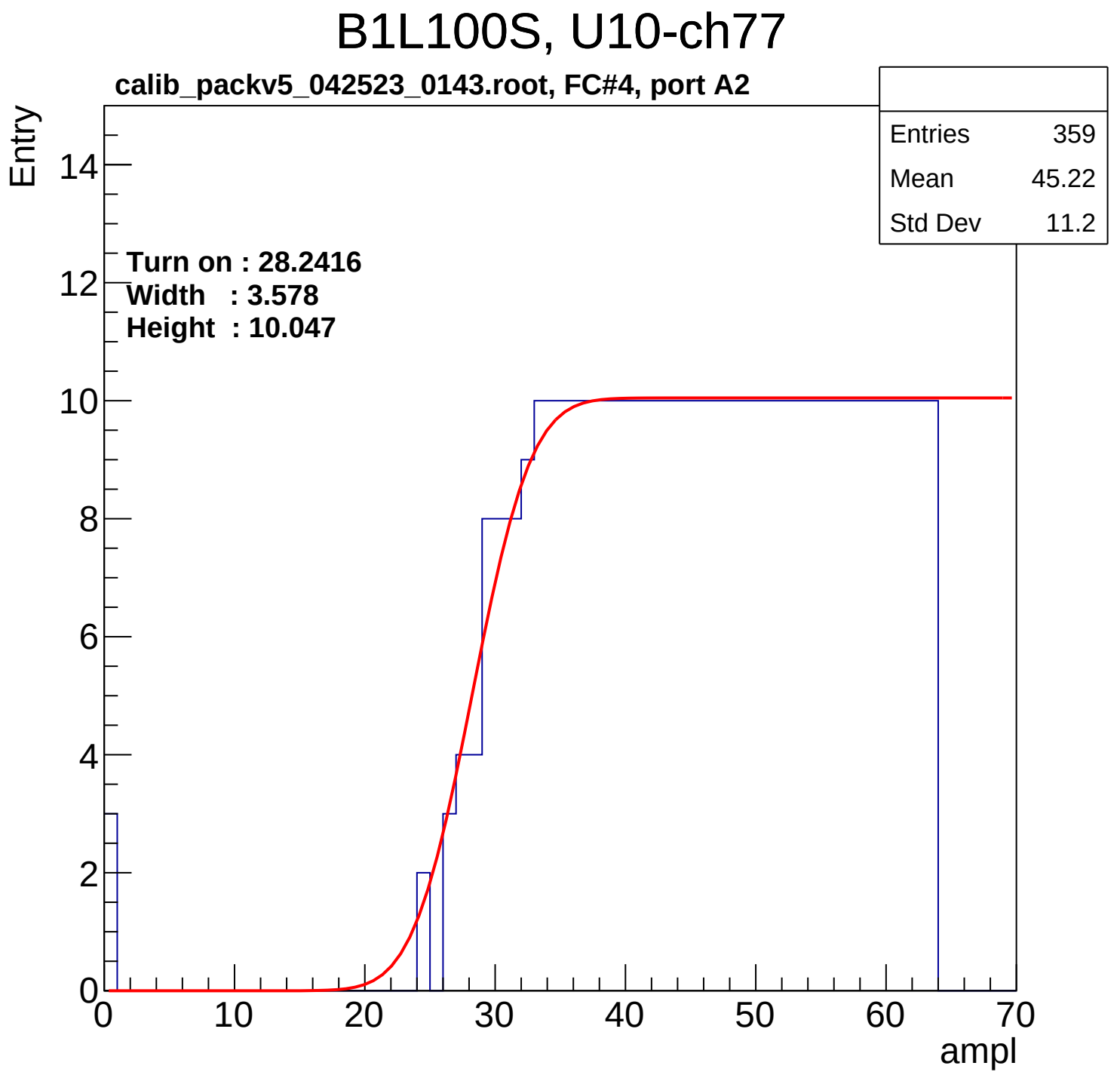
B1L100S, U10-ch77
calib_packv5_042523_0143.root, FC#4, port A2
Entries 359
Mean 45.22
Std Dev 11.2
Turn on : 28.2416
Width : 3.578
Height : 10.047
Entry
ampl
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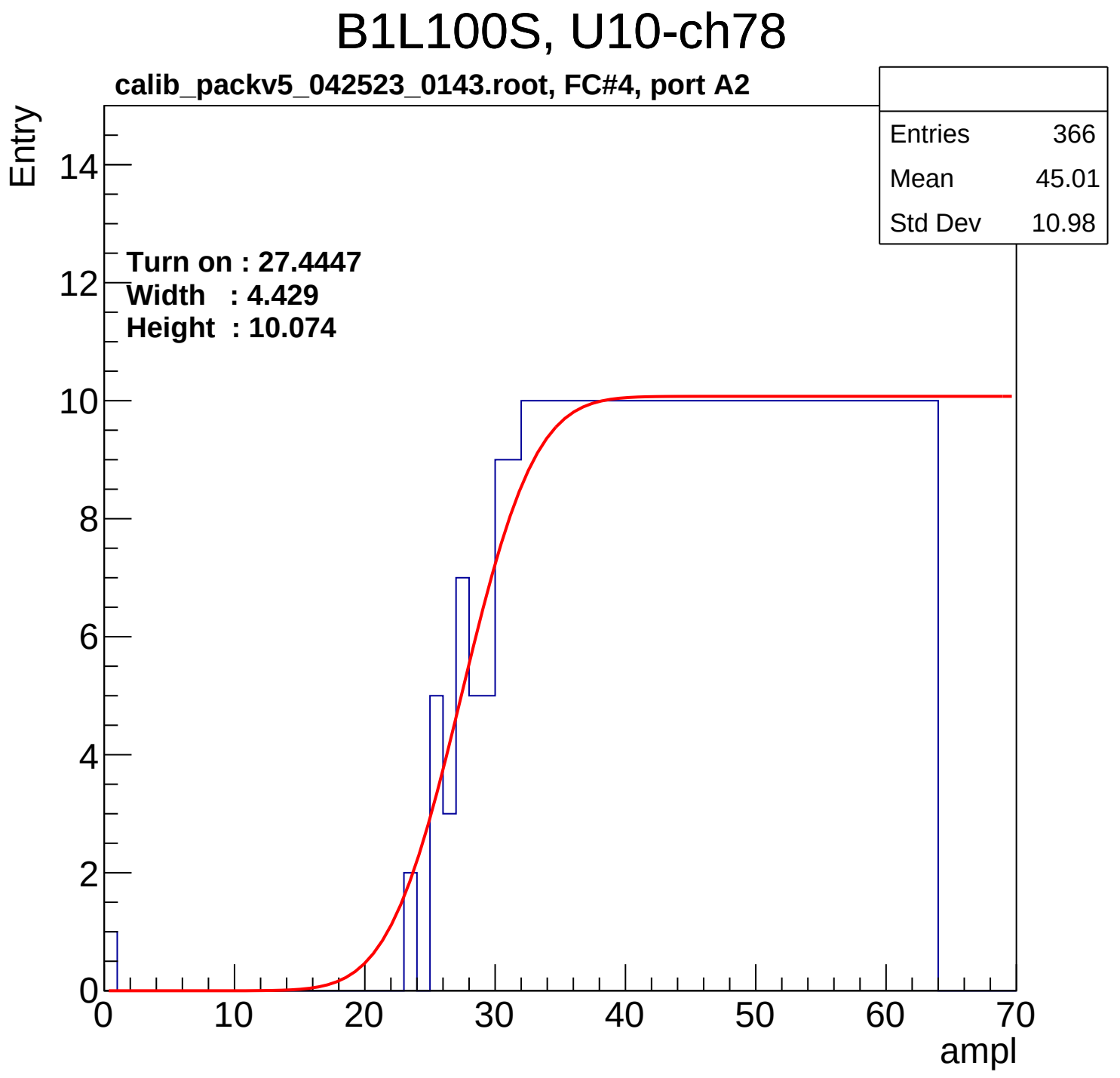
B1L100S, U10-ch78
calib_packv5_042523_0143.root, FC#4, port A2
Entries 366
Mean 45.01
Std Dev 10.98
Turn on : 27.4447
Width : 4.429
Height : 10.074
Entry
ampl
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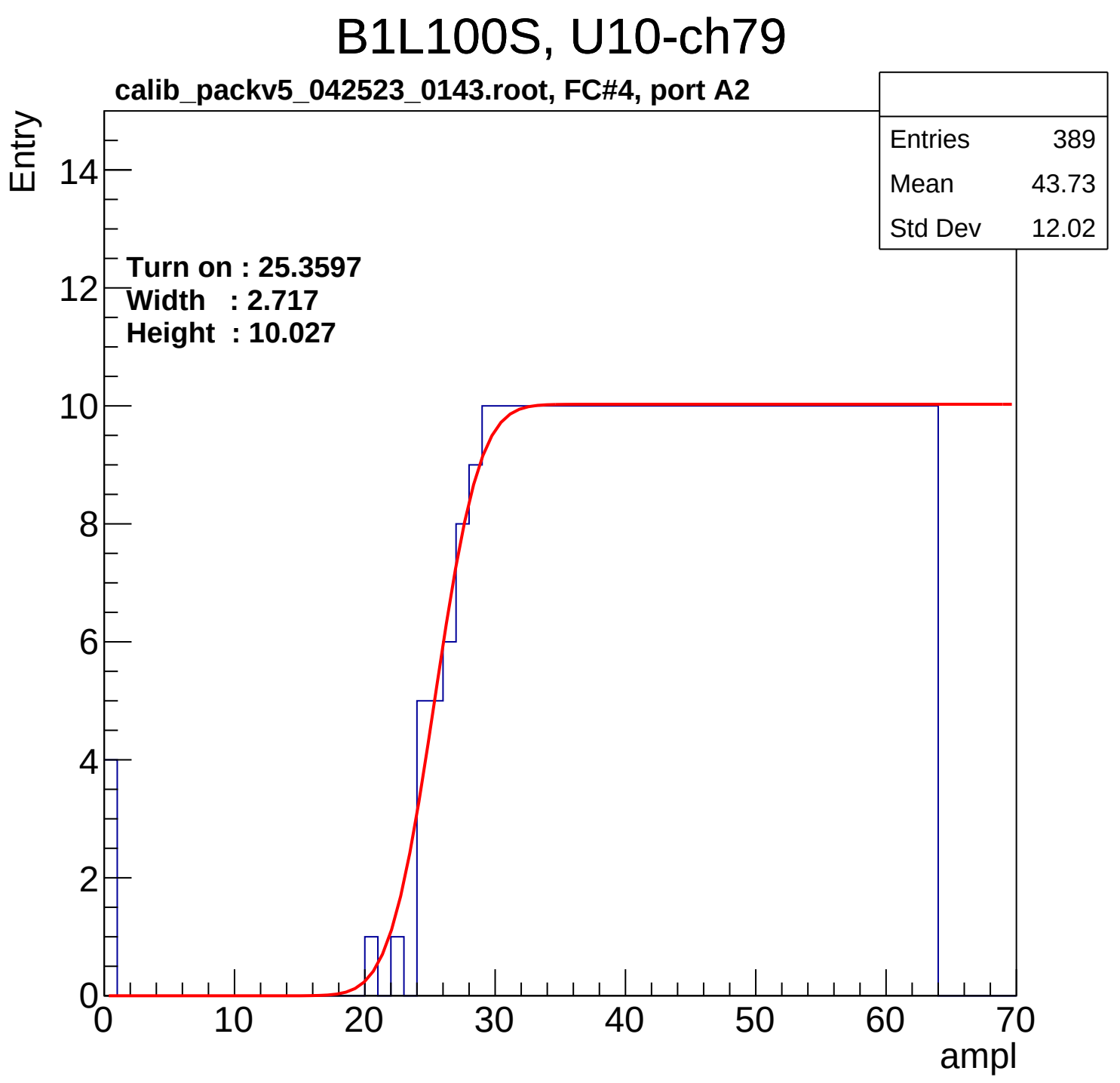
B1L100S, U10-ch79
calib_packv5_042523_0143.root, FC#4, port A2
Entries 389
Mean 43.73
Std Dev 12.02
Turn on : 25.3597
Width : 2.717
Height : 10.027
Entry
ampl
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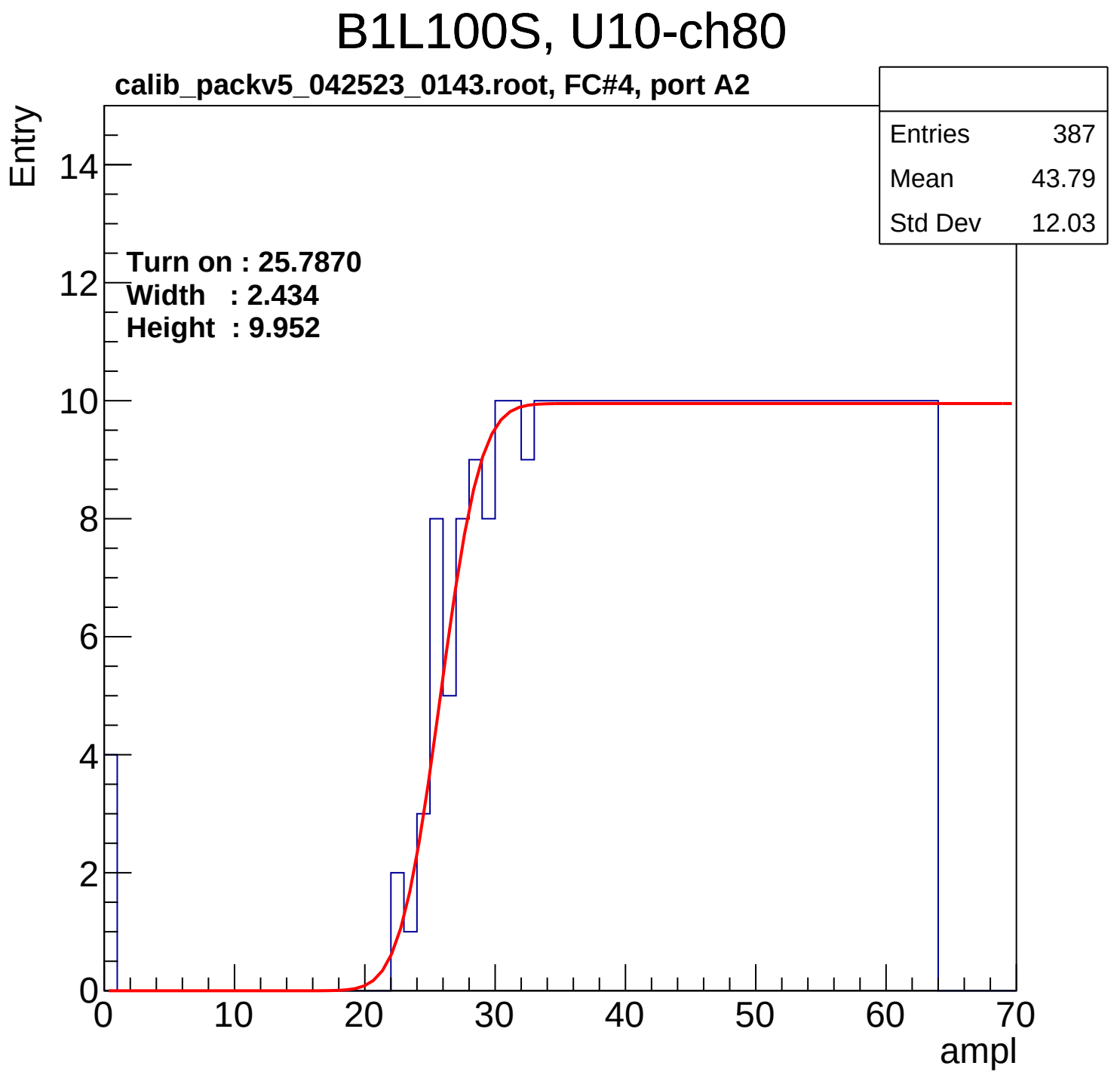
B1L100S, U10-ch80
calib_packv5_042523_0143.root, FC#4, port A2
Entries 387
Mean 43.79
Std Dev 12.03
Turn on : 25.7870
Width : 2.434
Height : 9.952
Entry
ampl
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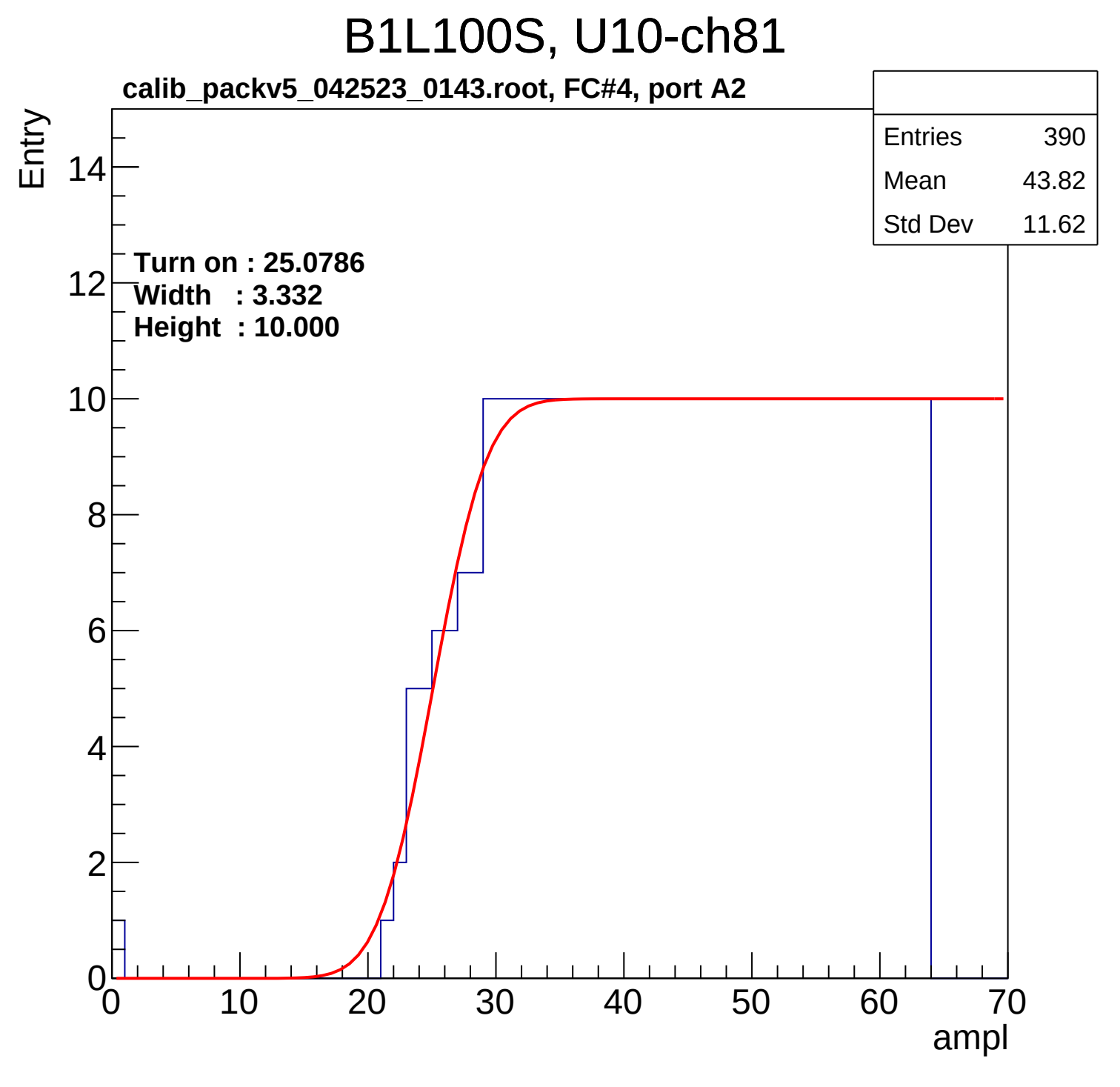
B1L100S, U10-ch81
calib_packv5_042523_0143.root, FC#4, port A2
Entries 390
Mean 43.82
Std Dev 11.62
Turn on : 25.0786
Width : 3.332
Height : 10.000
Entry
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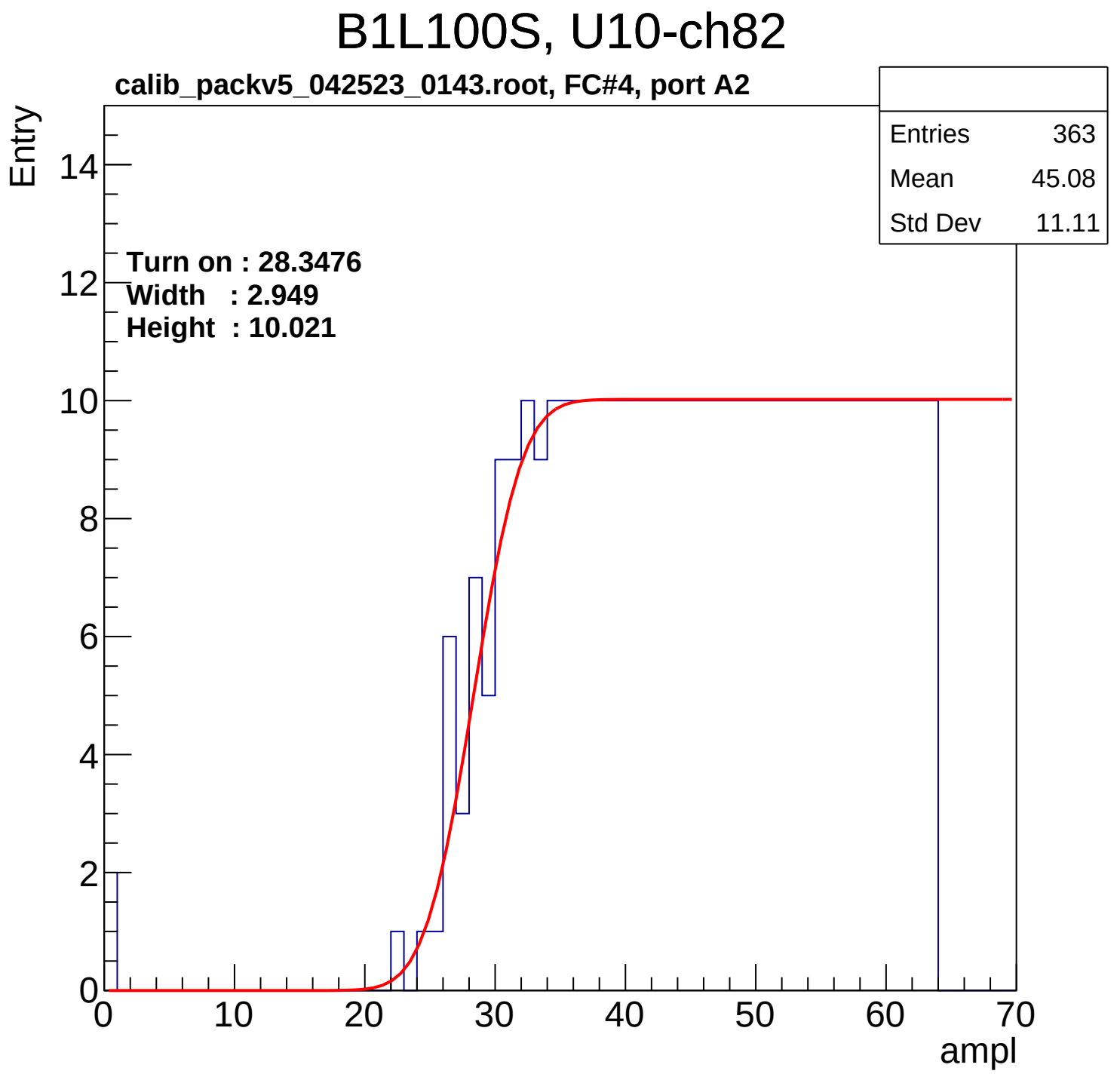
B1L100S, U10-ch82
calib_packv5_042523_0143.root, FC#4, port A2
Entries 363
Mean 45.08
Std Dev 11.11
Turn on : 28.3476
Width : 2.949
Height : 10.021
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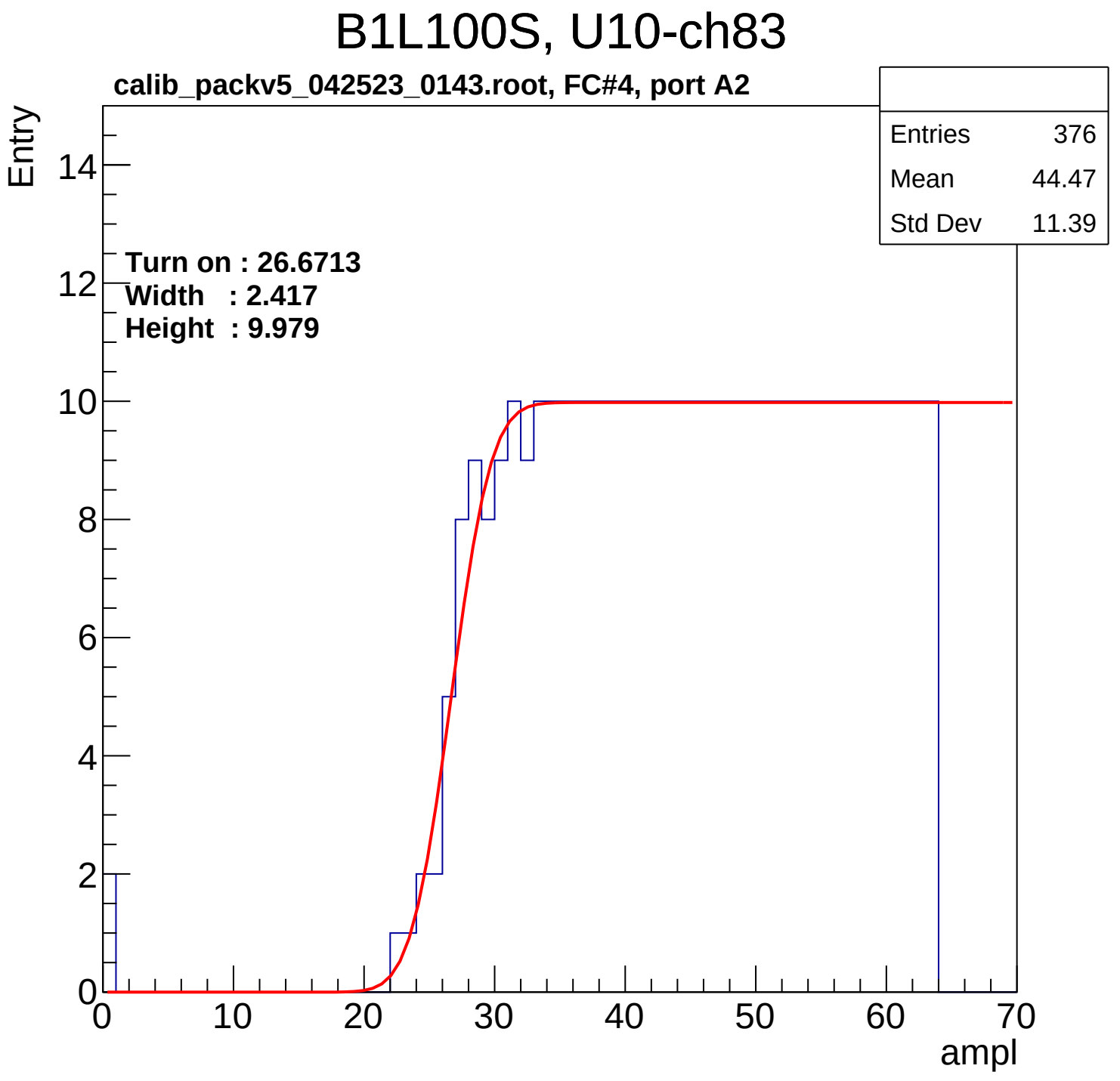
B1L100S, U10-ch83
calib_packv5_042523_0143.root, FC#4, port A2
Entries 376
Mean 44.47
Std Dev 11.39
Turn on : 26.6713
Width : 2.417
Height : 9.979
Entry
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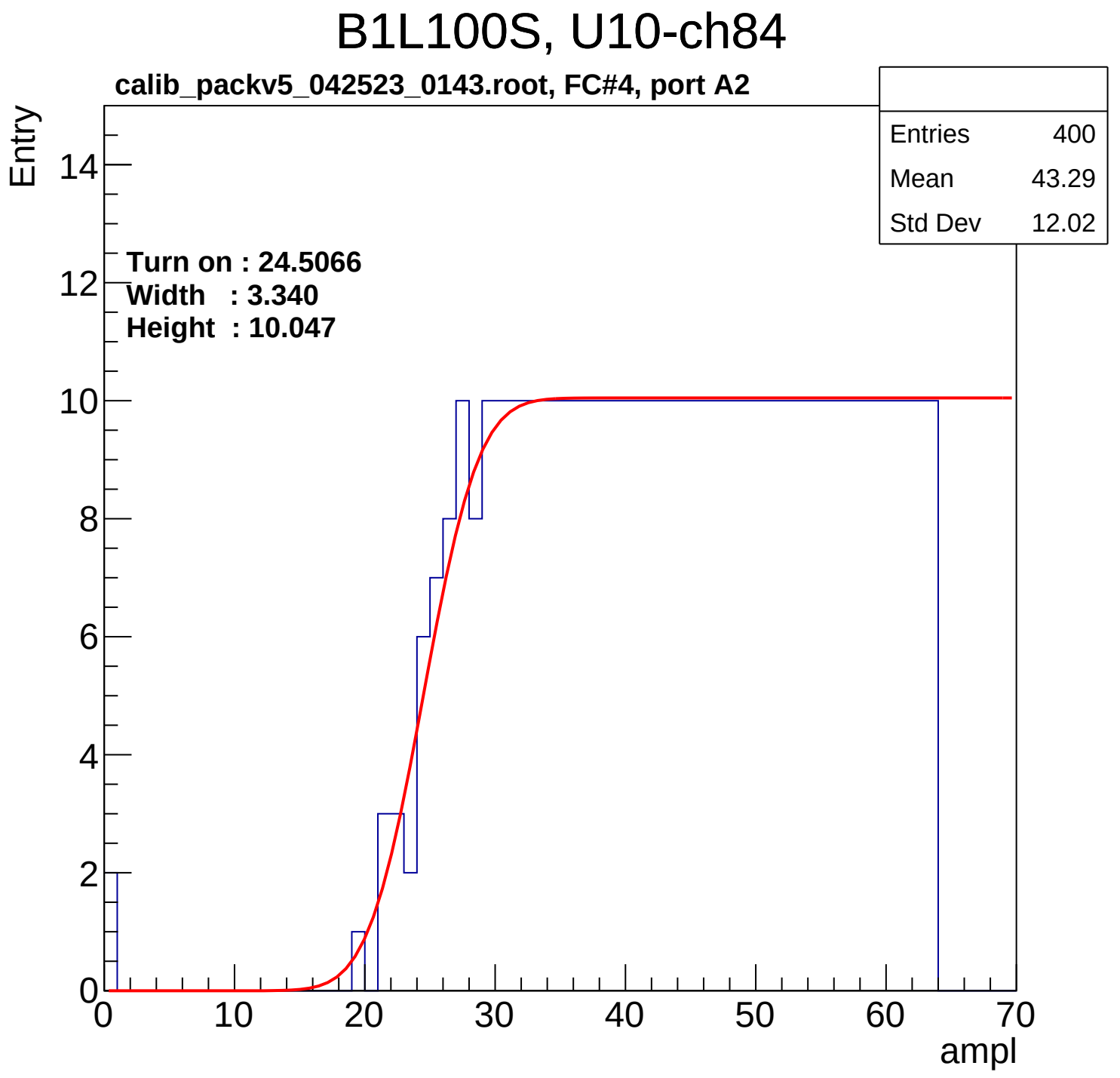
B1L100S, U10-ch84
calib_packv5_042523_0143.root, FC#4, port A2
Entries 400
Mean 43.29
Std Dev 12.02
Turn on : 24.5066
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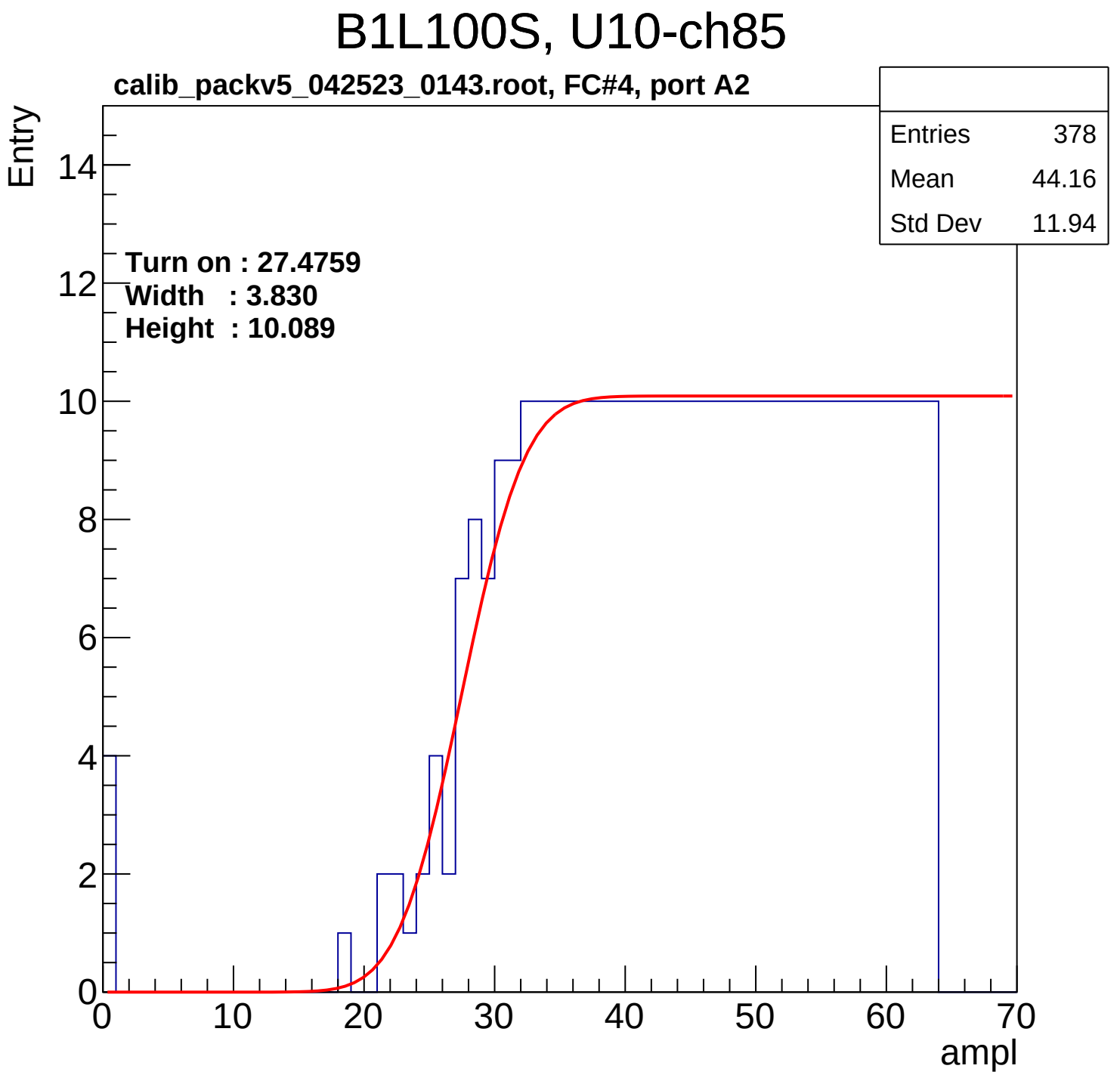
B1L100S, U10-ch85
calib_packv5_042523_0143.root, FC#4, port A2
Entries 378
Mean 44.16
Std Dev 11.94
Turn on : 27.4759
Width : 3.830
Height : 10.089
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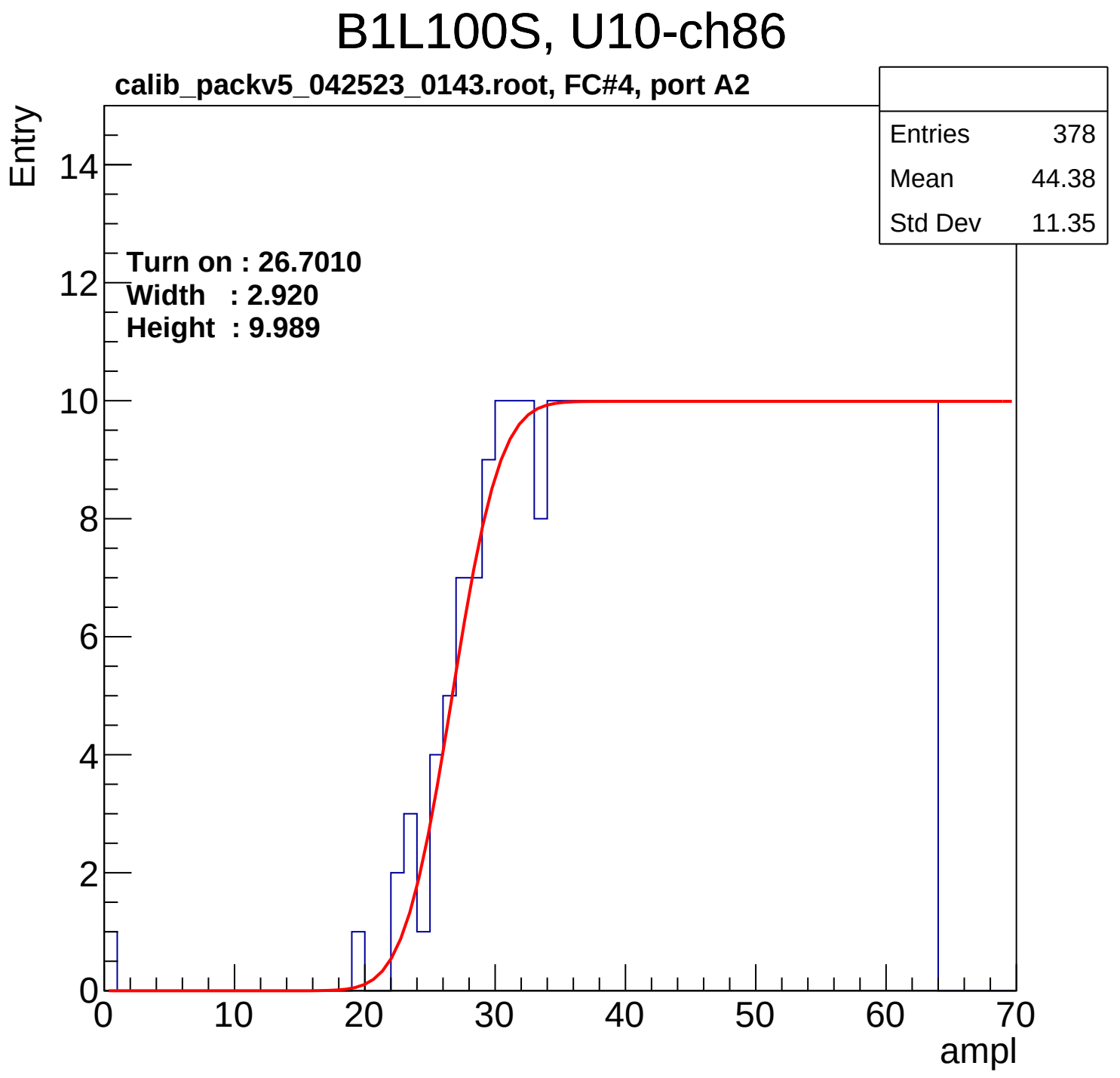
B1L100S, U10-ch86
calib_packv5_042523_0143.root, FC#4, port A2
Entries 378
Mean 44.38
Std Dev 11.35
Turn on : 26.7010
Width : 2.920
Height : 9.989
Entry
ampl
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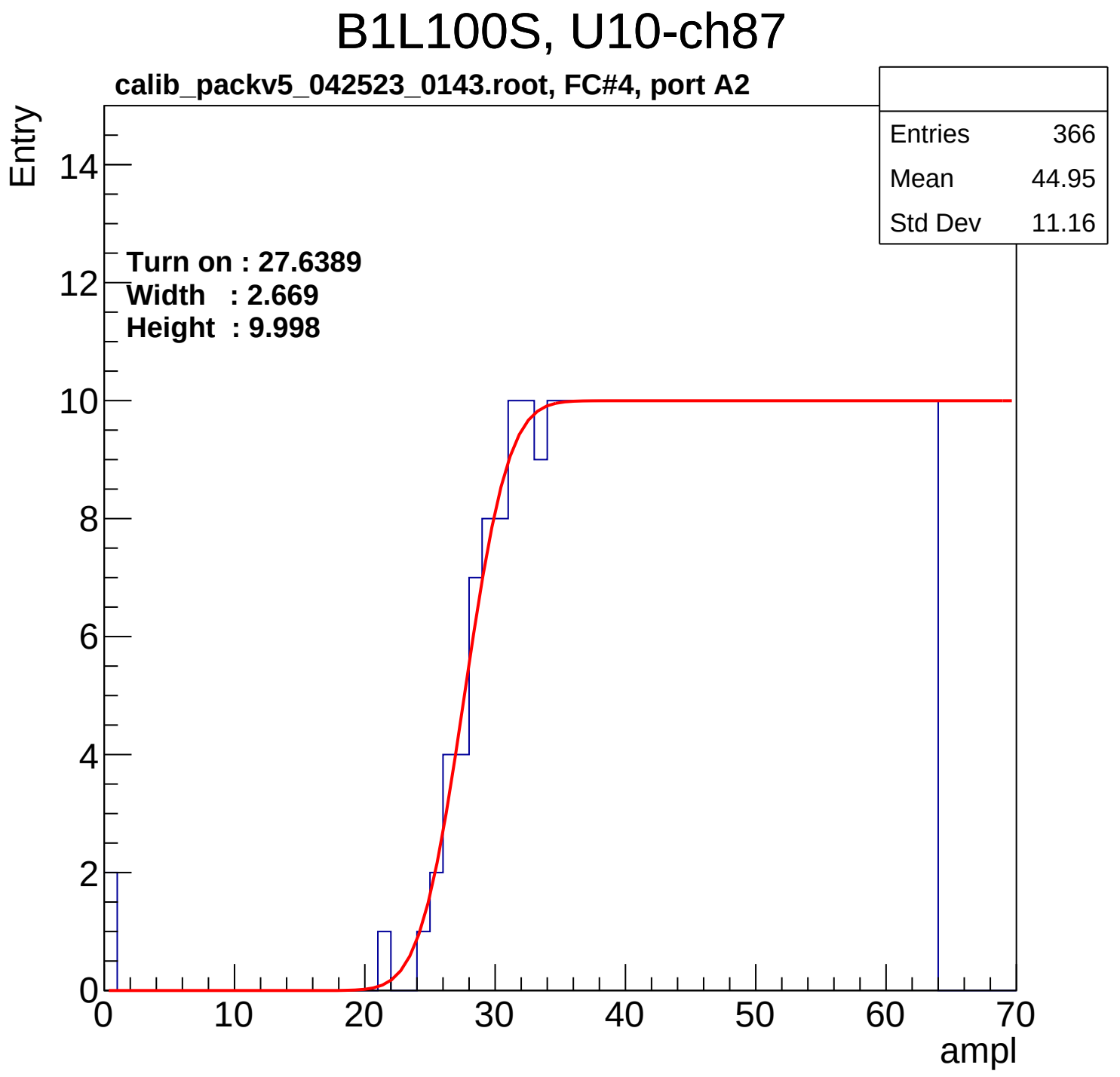
B1L100S, U10-ch87
calib_packv5_042523_0143.root, FC#4, port A2
Entries 366
Mean 44.95
Std Dev 11.16
Turn on : 27.6389
Width : 2.669
Height : 9.998
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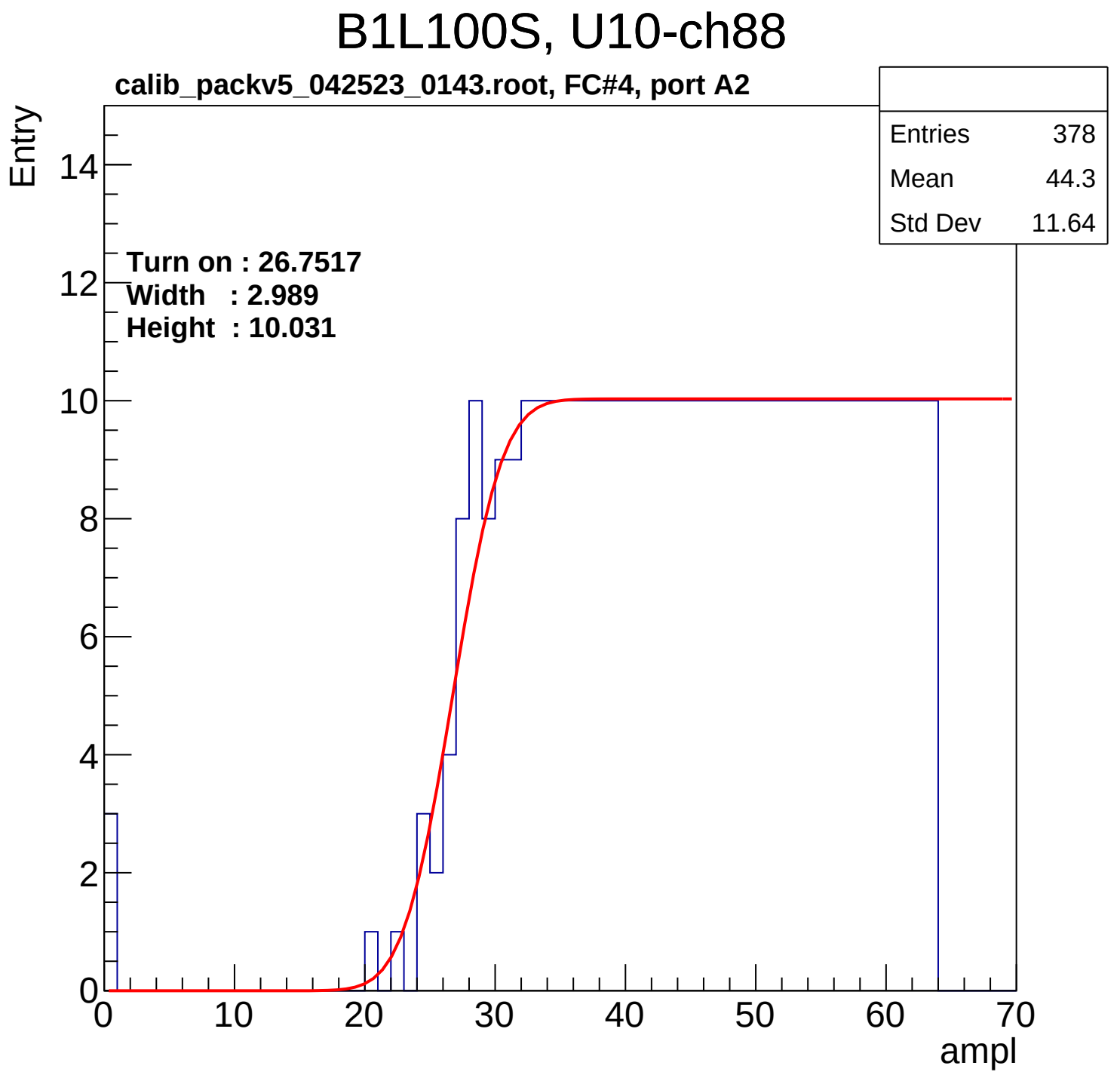
B1L100S, U10-ch88
calib_packv5_042523_0143.root, FC#4, port A2
Entries 378
Mean 44.3
Std Dev 11.64
Turn on : 26.7517
Width : 2.989
Height : 10.031
Entry
ampl
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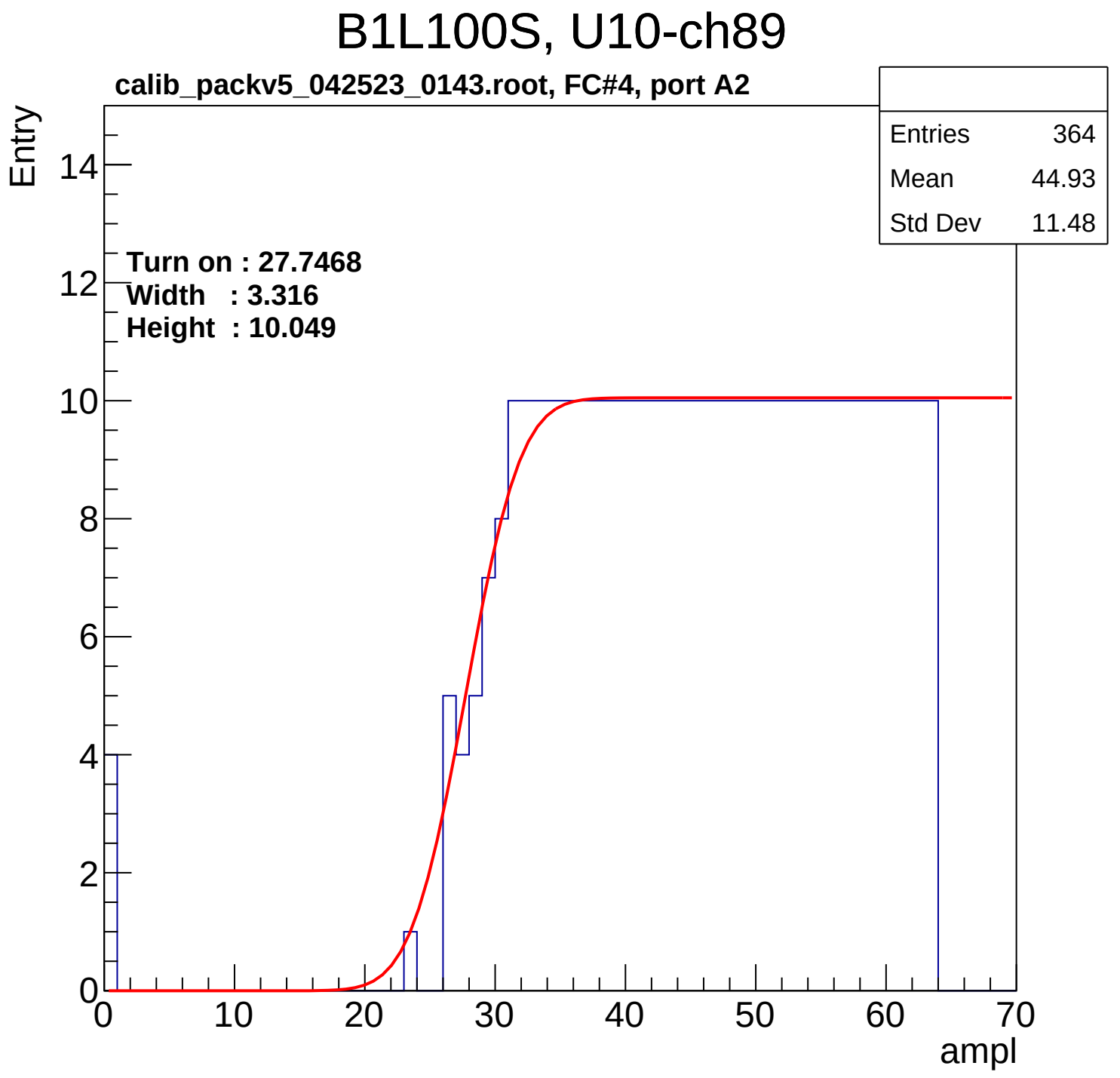
B1L100S, U10-ch89
calib_packv5_042523_0143.root, FC#4, port A2
Entries 364
Mean 44.93
Std Dev 11.48
Turn on : 27.7468
Width : 3.316
Height : 10.049
Entry
ampl
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2
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6
8
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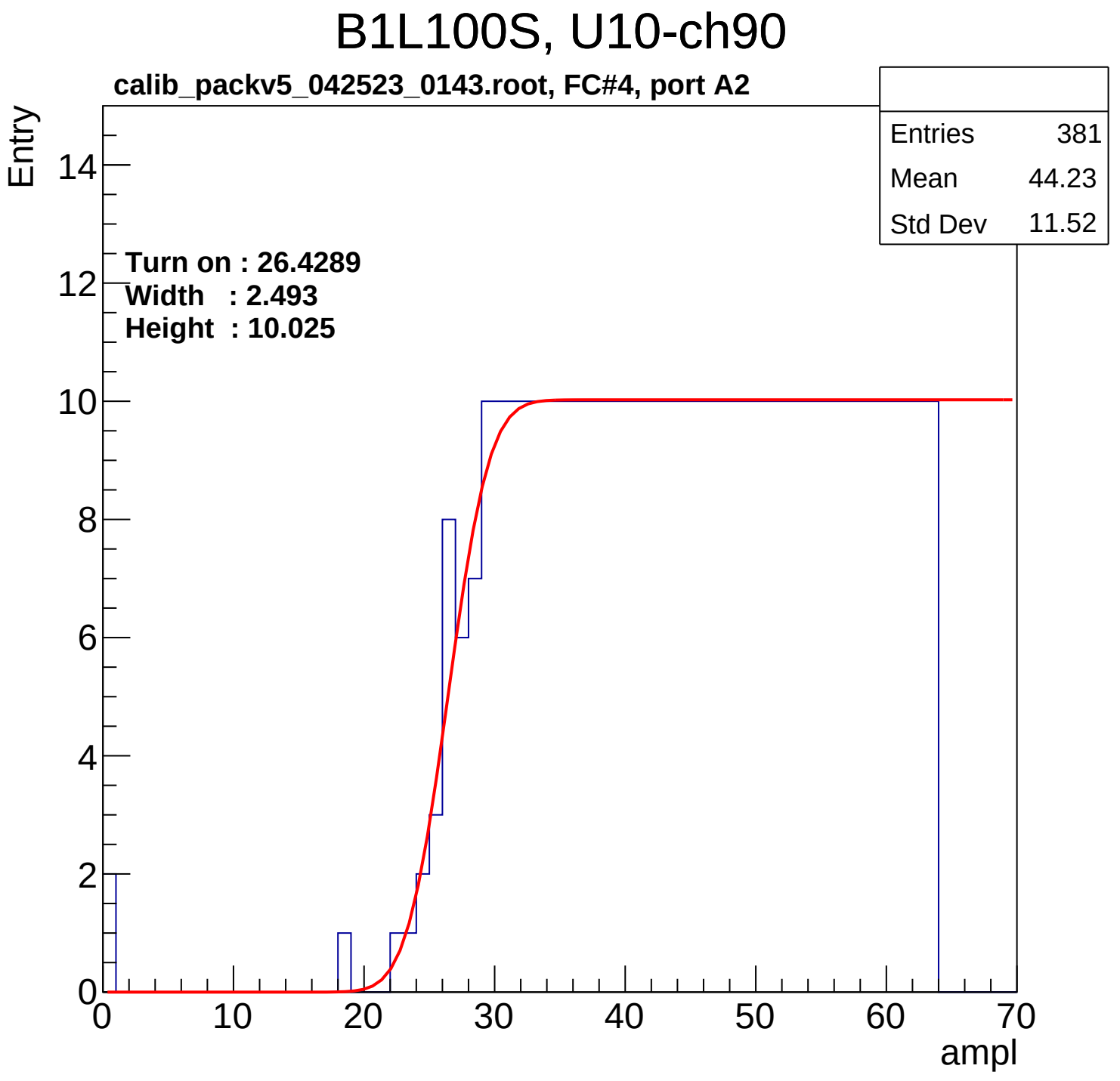
B1L100S, U10-ch90
calib_packv5_042523_0143.root, FC#4, port A2
Entries 381
Mean 44.23
Std Dev 11.52
Turn on : 26.4289
Width : 2.493
Height : 10.025
Entry
ampl
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2
4
6
8
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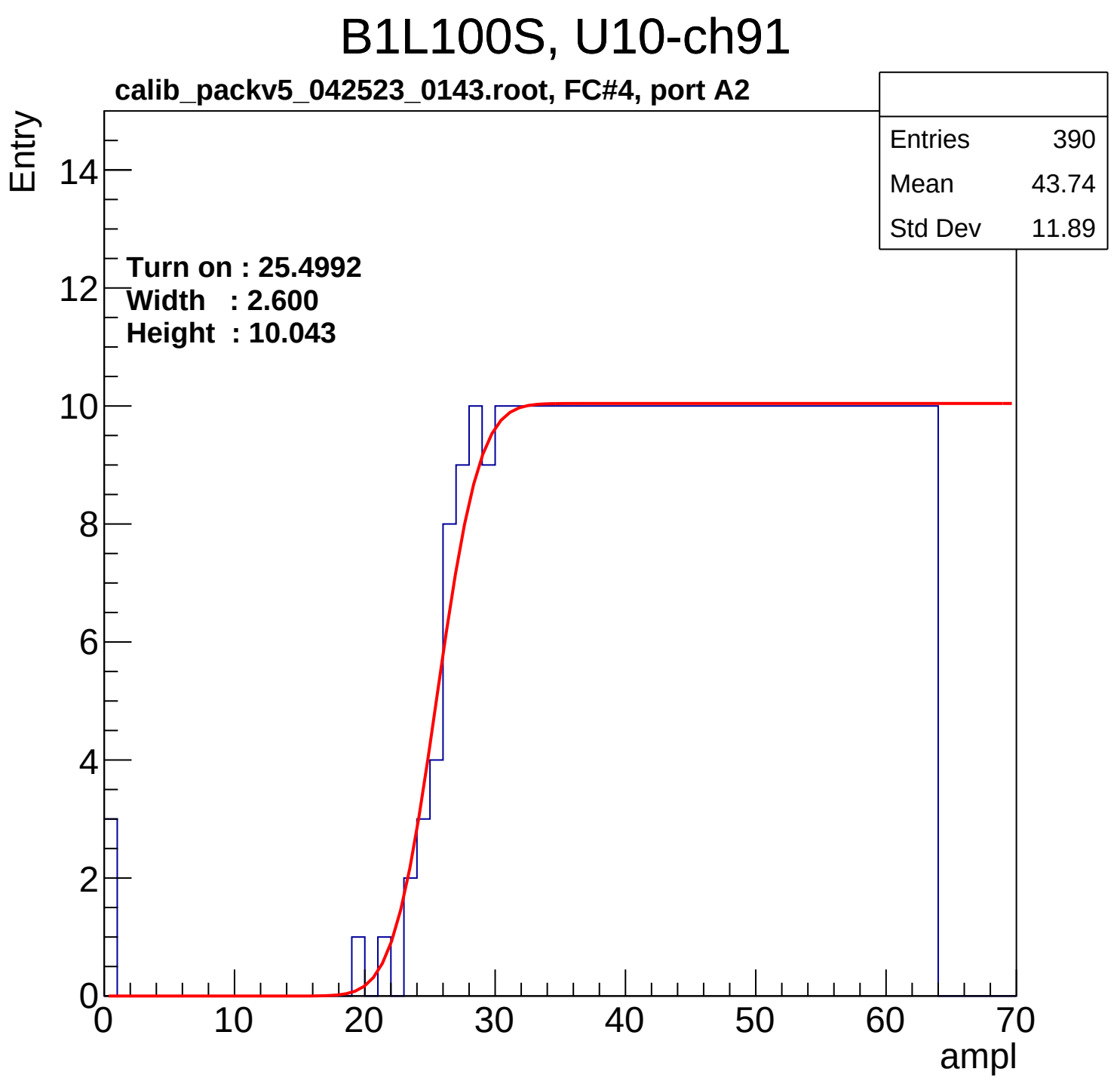
B1L100S, U10-ch91
calib_packv5_042523_0143.root, FC#4, port A2
Entries 390
Mean 43.74
Std Dev 11.89
Turn on : 25.4992
Width : 2.600
Height : 10.043
Entry
ampl
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2
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6
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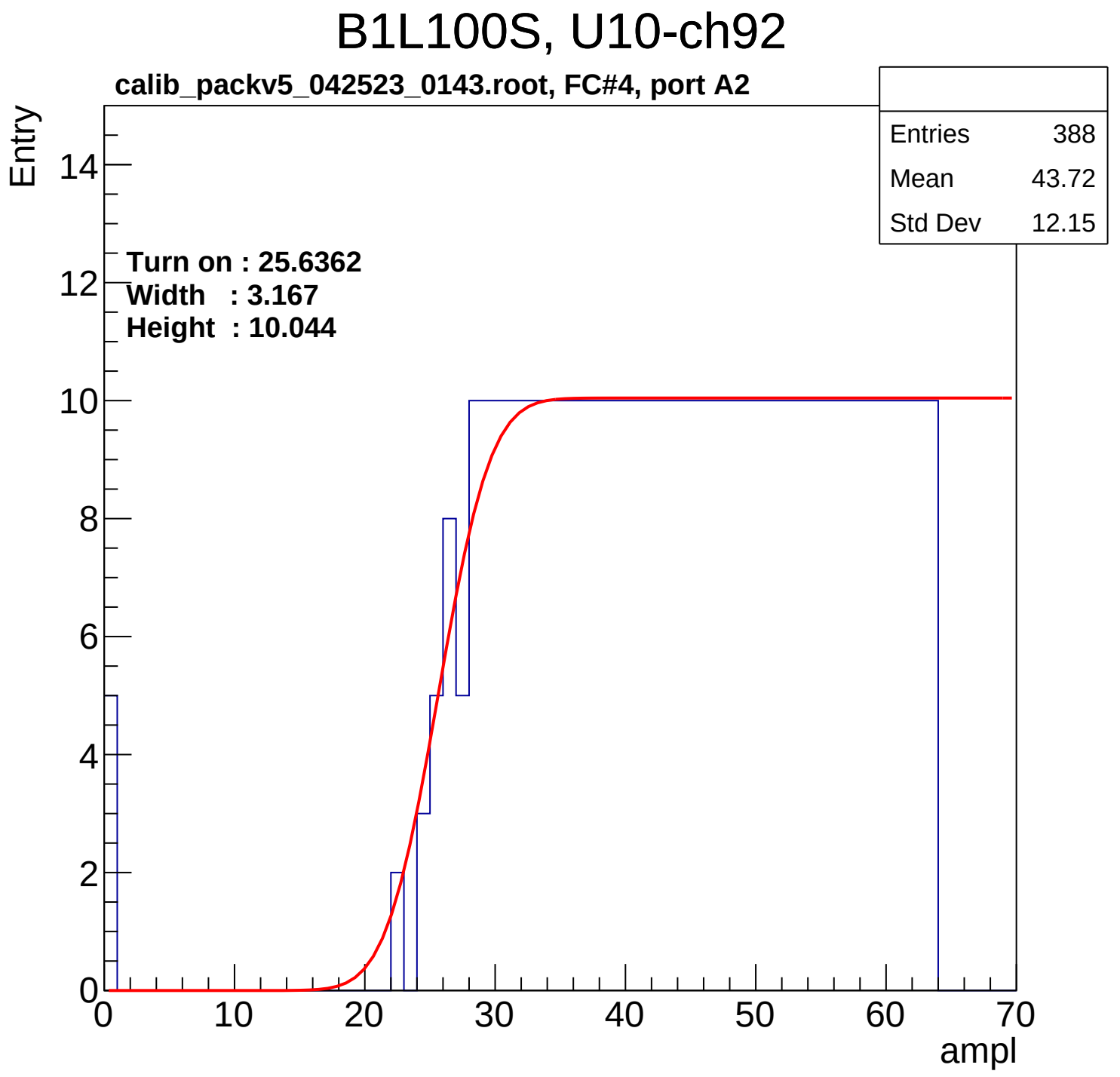
B1L100S, U10-ch92
calib_packv5_042523_0143.root, FC#4, port A2
Entries 388
Mean 43.72
Std Dev 12.15
Turn on : 25.6362
Width : 3.167
Height : 10.044
Entry
ampl
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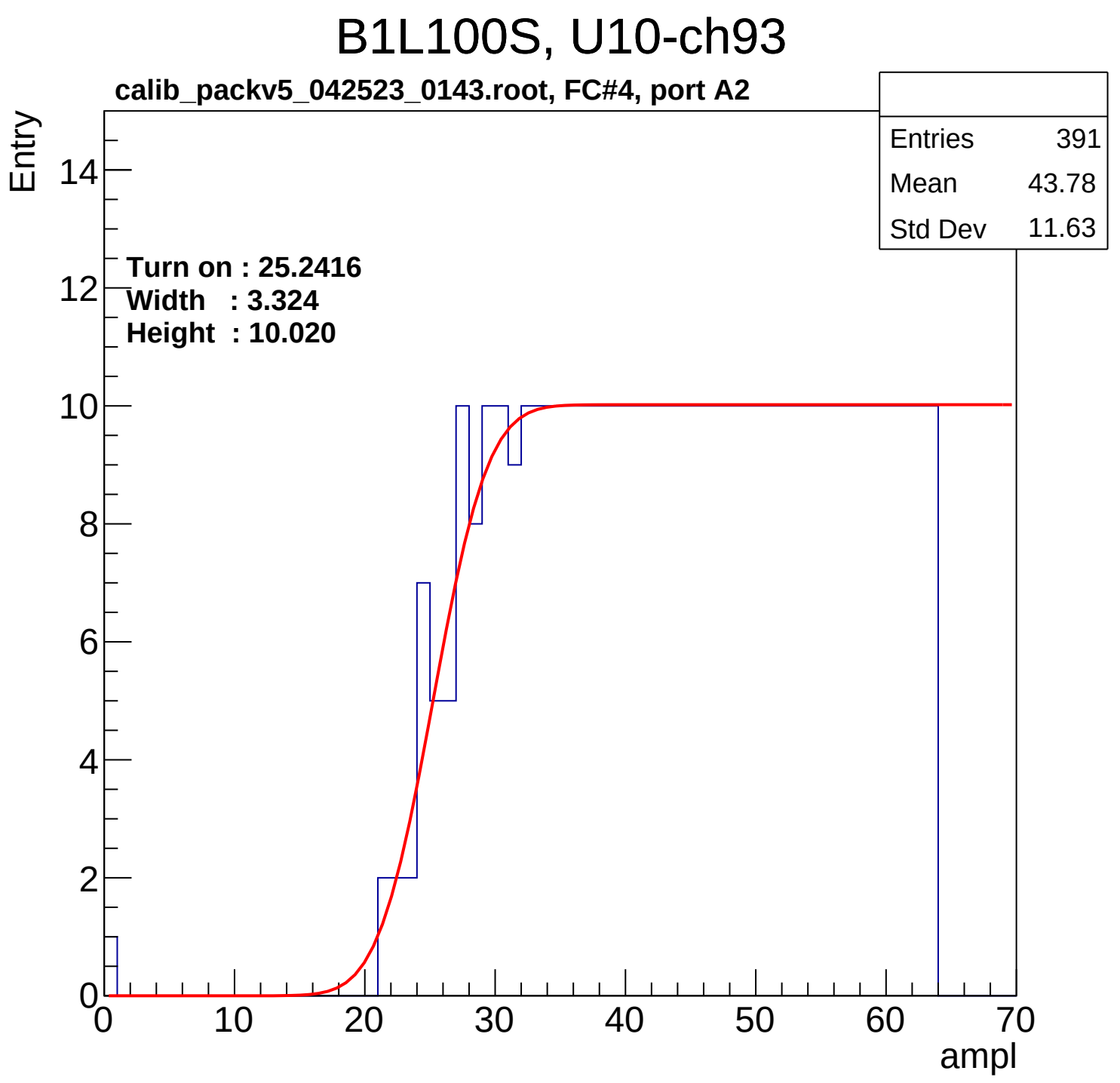
B1L100S, U10-ch93
calib_packv5_042523_0143.root, FC#4, port A2
Entries 391
Mean 43.78
Std Dev 11.63
Turn on : 25.2416
Width : 3.324
Height : 10.020
Entry
ampl
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6
8
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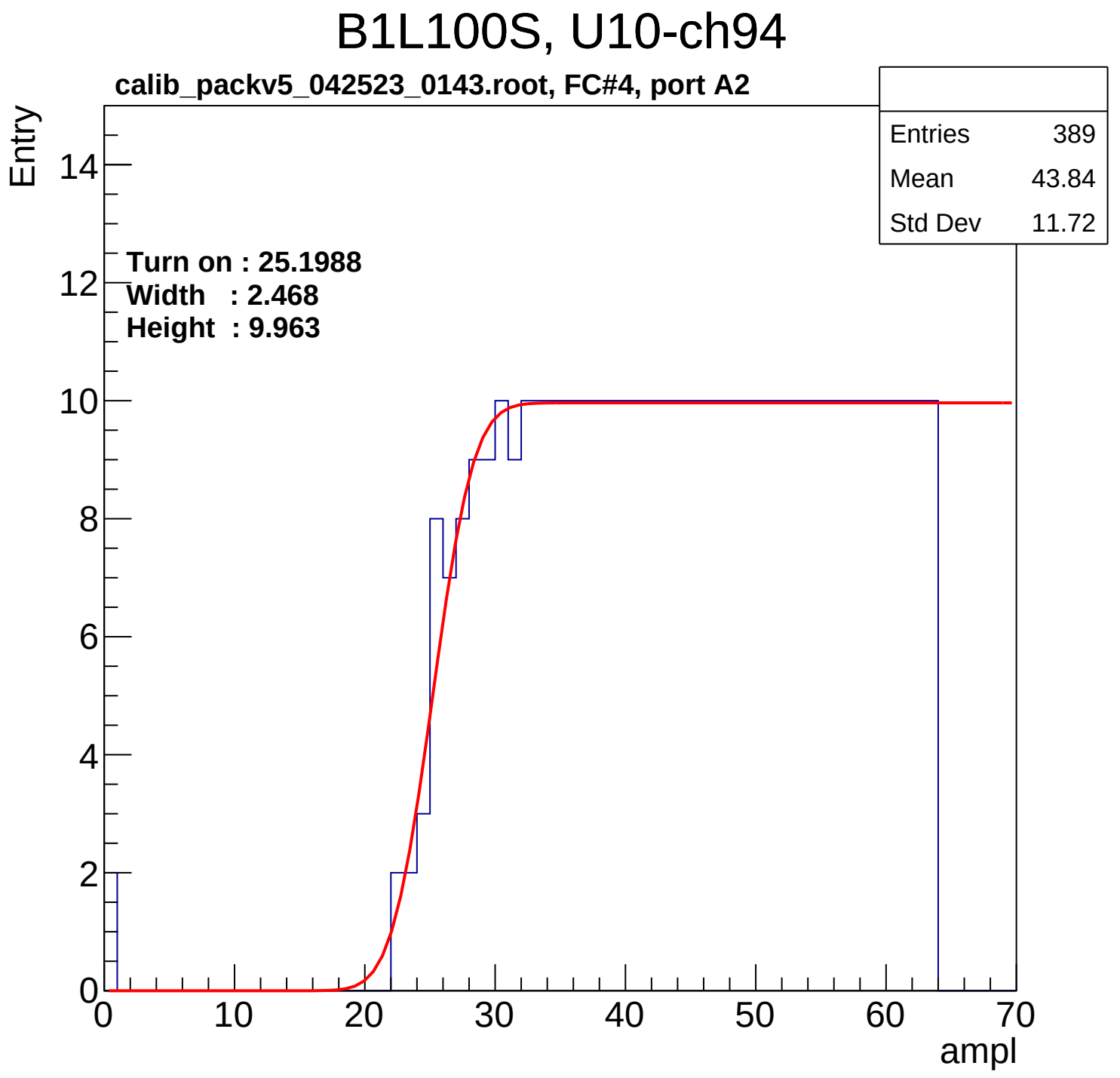
B1L100S, U10-ch94
calib_packv5_042523_0143.root, FC#4, port A2
Entries 389
Mean 43.84
Std Dev 11.72
Turn on : 25.1988
Width : 2.468
Height : 9.963
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
30
40
50
60
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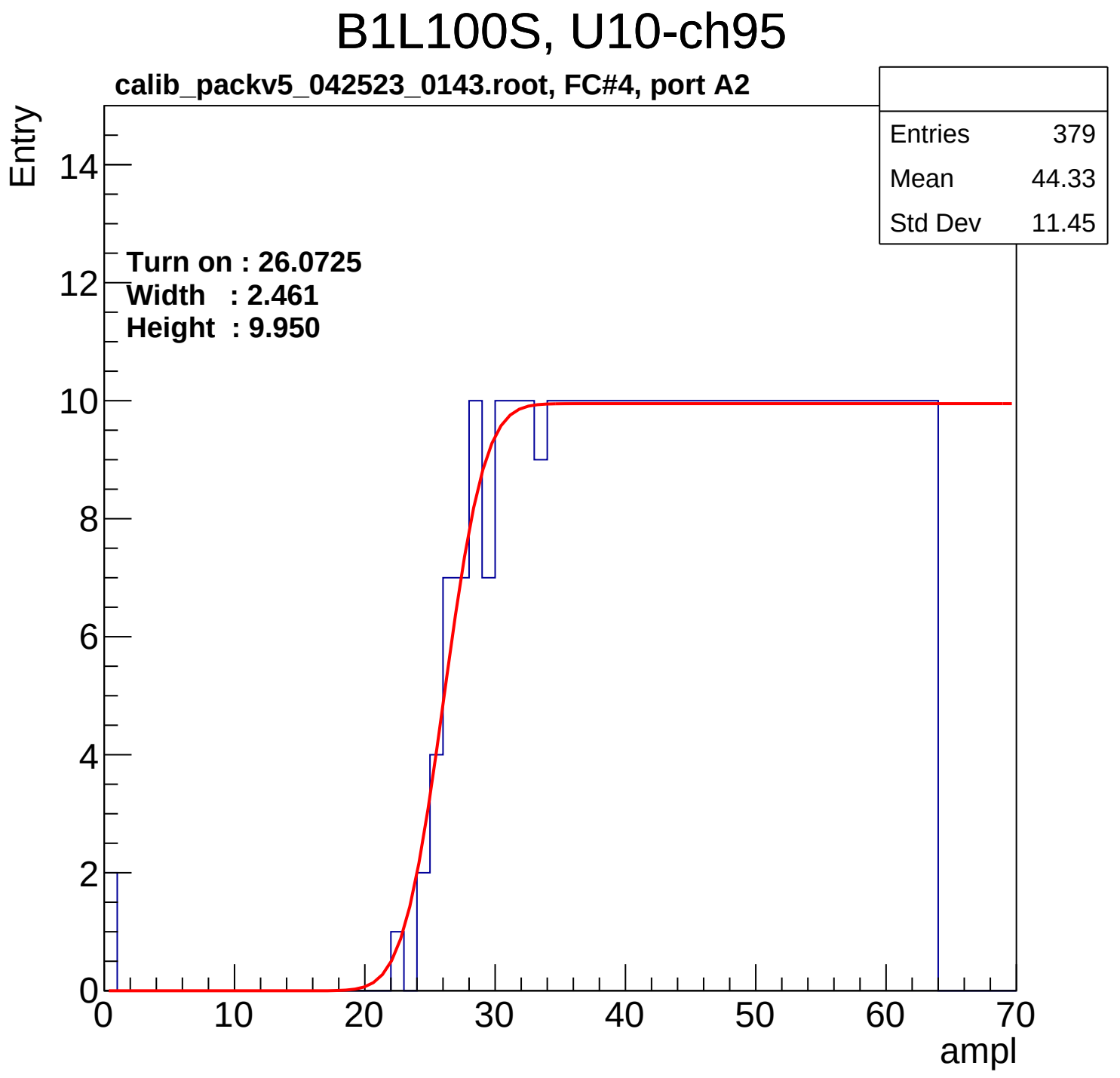
B1L100S, U10-ch95
calib_packv5_042523_0143.root, FC#4, port A2
Entries 379
Mean 44.33
Std Dev 11.45
Turn on : 26.0725
Width : 2.461
Height : 9.950
Entry
ampl
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6
8
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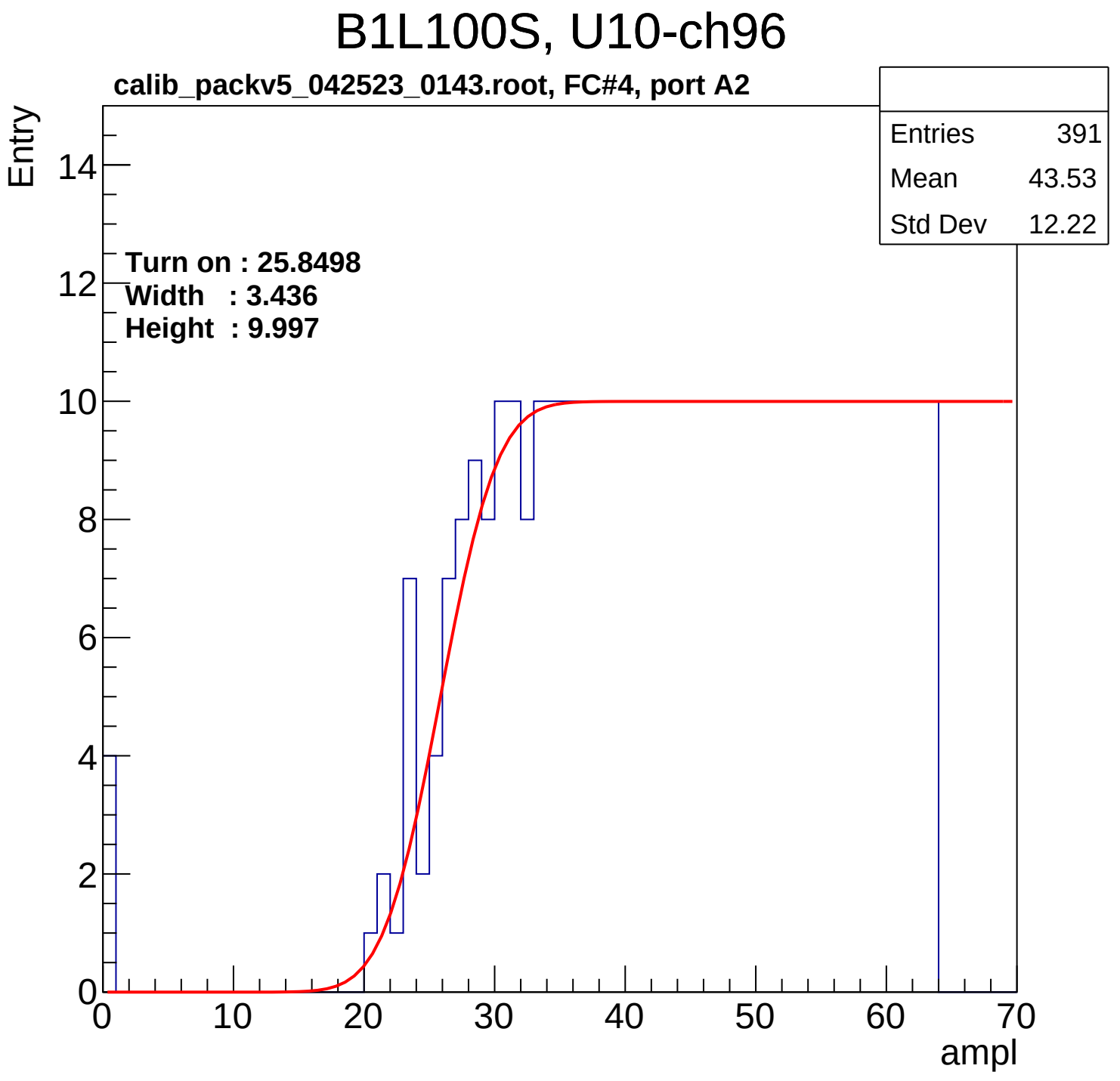
B1L100S, U10-ch96
calib_packv5_042523_0143.root, FC#4, port A2
Entries 391
Mean 43.53
Std Dev 12.22
Turn on : 25.8498
Width : 3.436
Height : 9.997
Entry
ampl
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2
4
6
8
10
12
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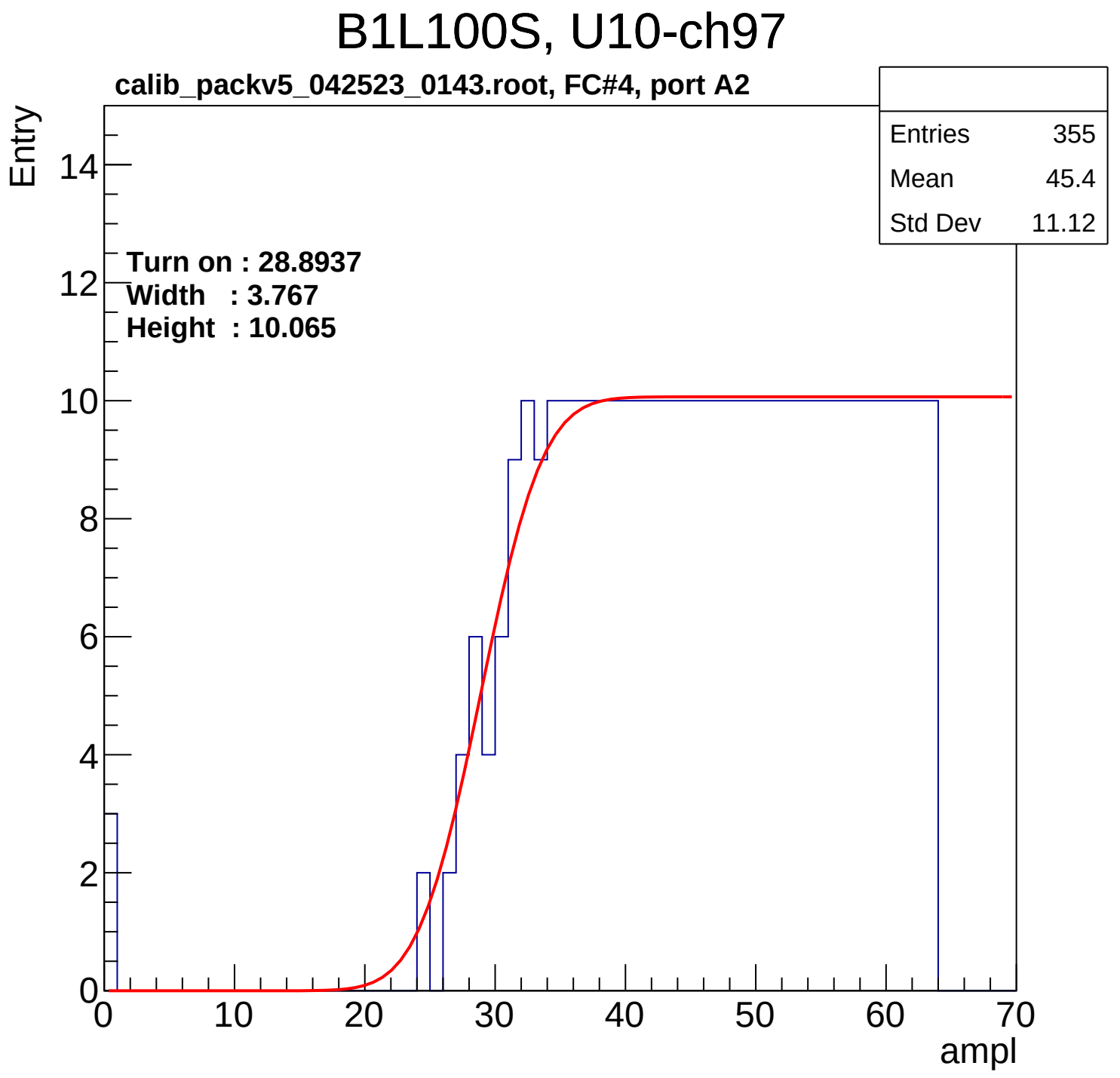
B1L100S, U10-ch97
calib_packv5_042523_0143.root, FC#4, port A2
Entries 355
Mean 45.4
Std Dev 11.12
Turn on : 28.8937
Width : 3.767
Height : 10.065
Entry
ampl
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4
6
8
10
12
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0
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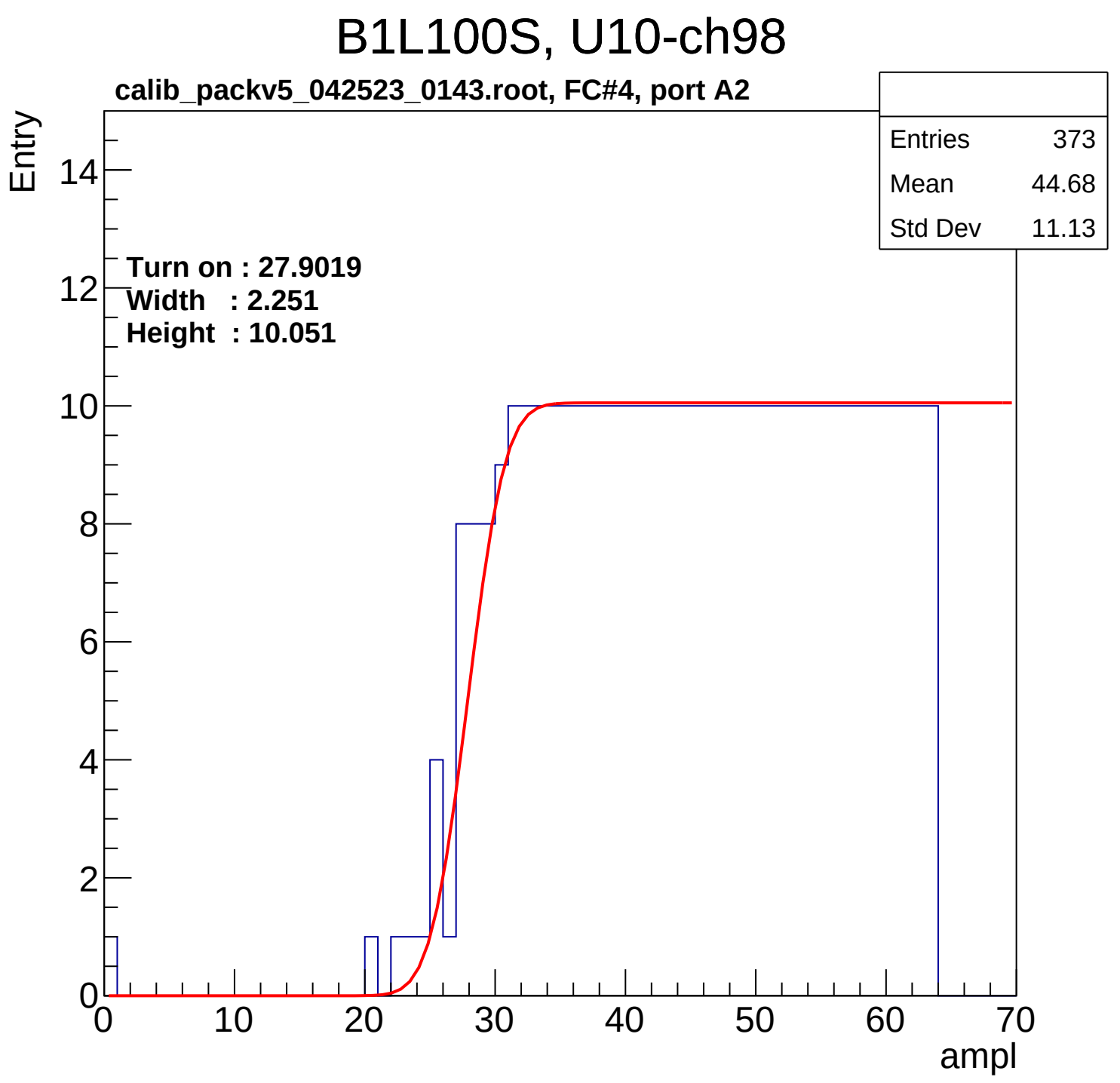
B1L100S, U10-ch98
calib_packv5_042523_0143.root, FC#4, port A2
Entries 373
Mean 44.68
Std Dev 11.13
Turn on : 27.9019
Width : 2.251
Height : 10.051
Entry
ampl
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2
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6
8
10
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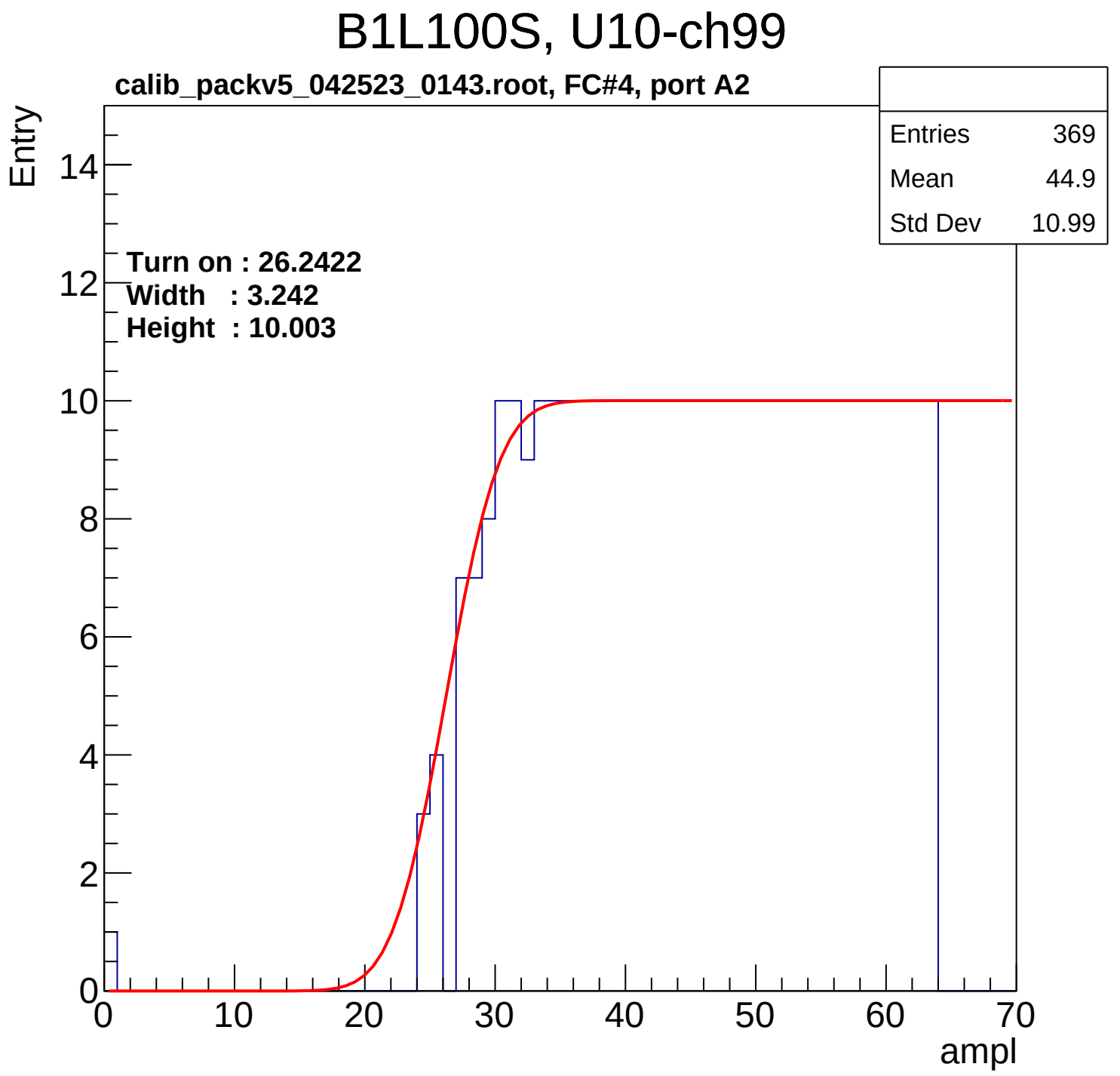
B1L100S, U10-ch99
calib_packv5_042523_0143.root, FC#4, port A2
Entries 369
Mean 44.9
Std Dev 10.99
Turn on : 26.2422
Width : 3.242
Height : 10.003
Entry
ampl
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6
8
10
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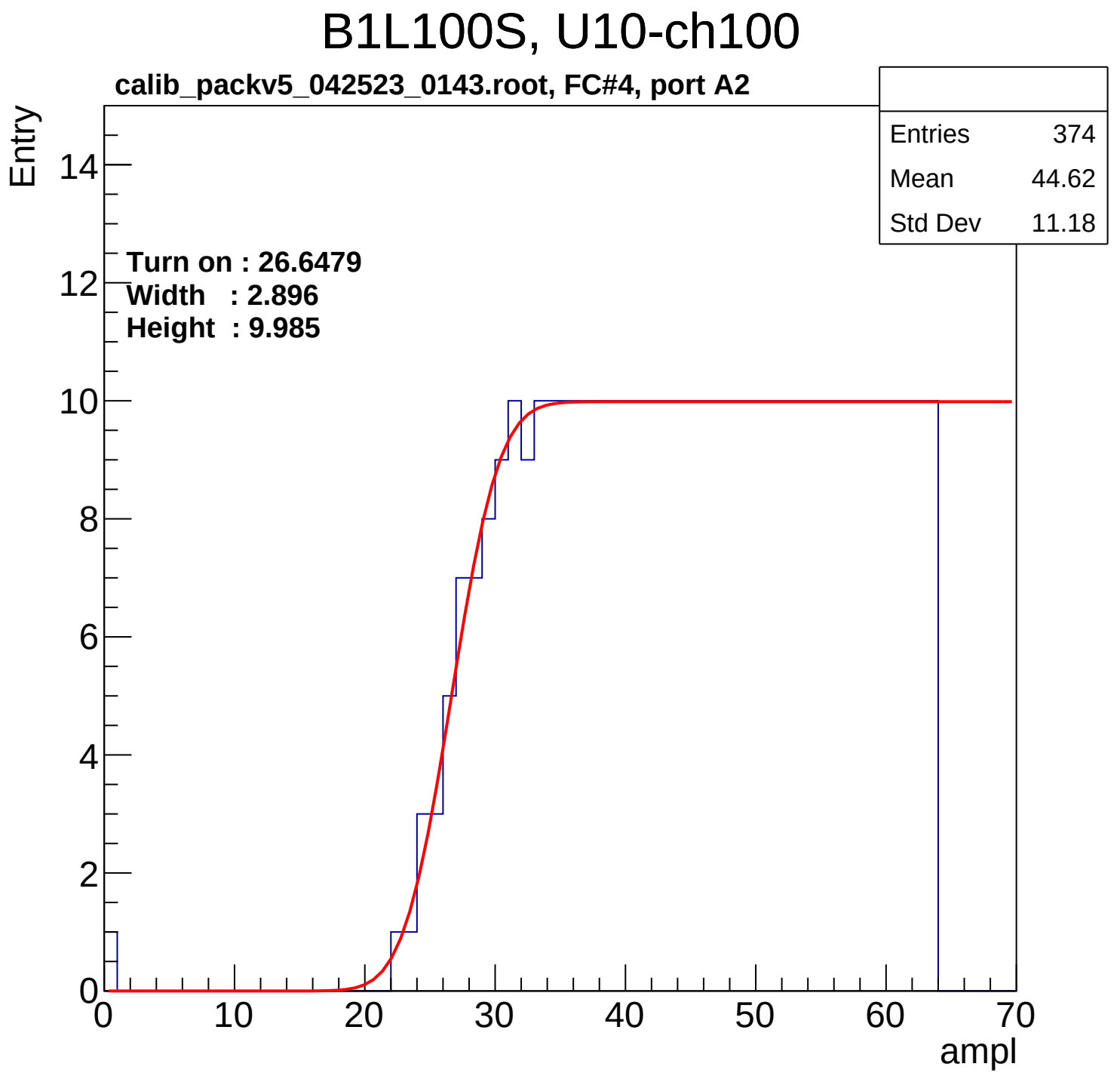
B1L100S, U10-ch100
calib_packv5_042523_0143.root, FC#4, port A2
Entries 374
Mean 44.62
Std Dev 11.18
Turn on : 26.6479
Width : 2.896
Height : 9.985
Entry
ampl
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6
8
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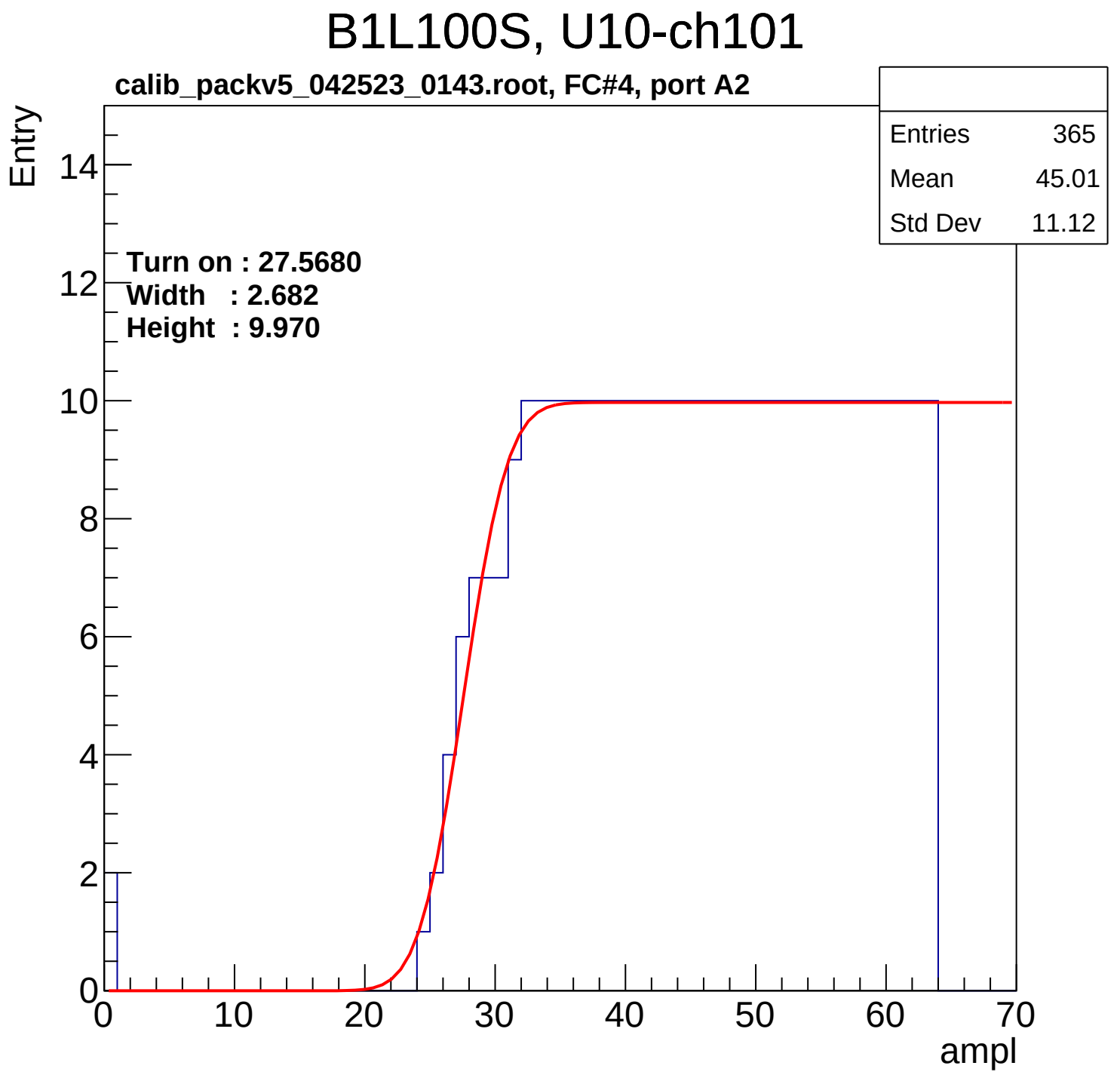
B1L100S, U10-ch101
calib_packv5_042523_0143.root, FC#4, port A2
Entries 365
Mean 45.01
Std Dev 11.12
Turn on : 27.5680
Width : 2.682
Height : 9.970
Entry
ampl
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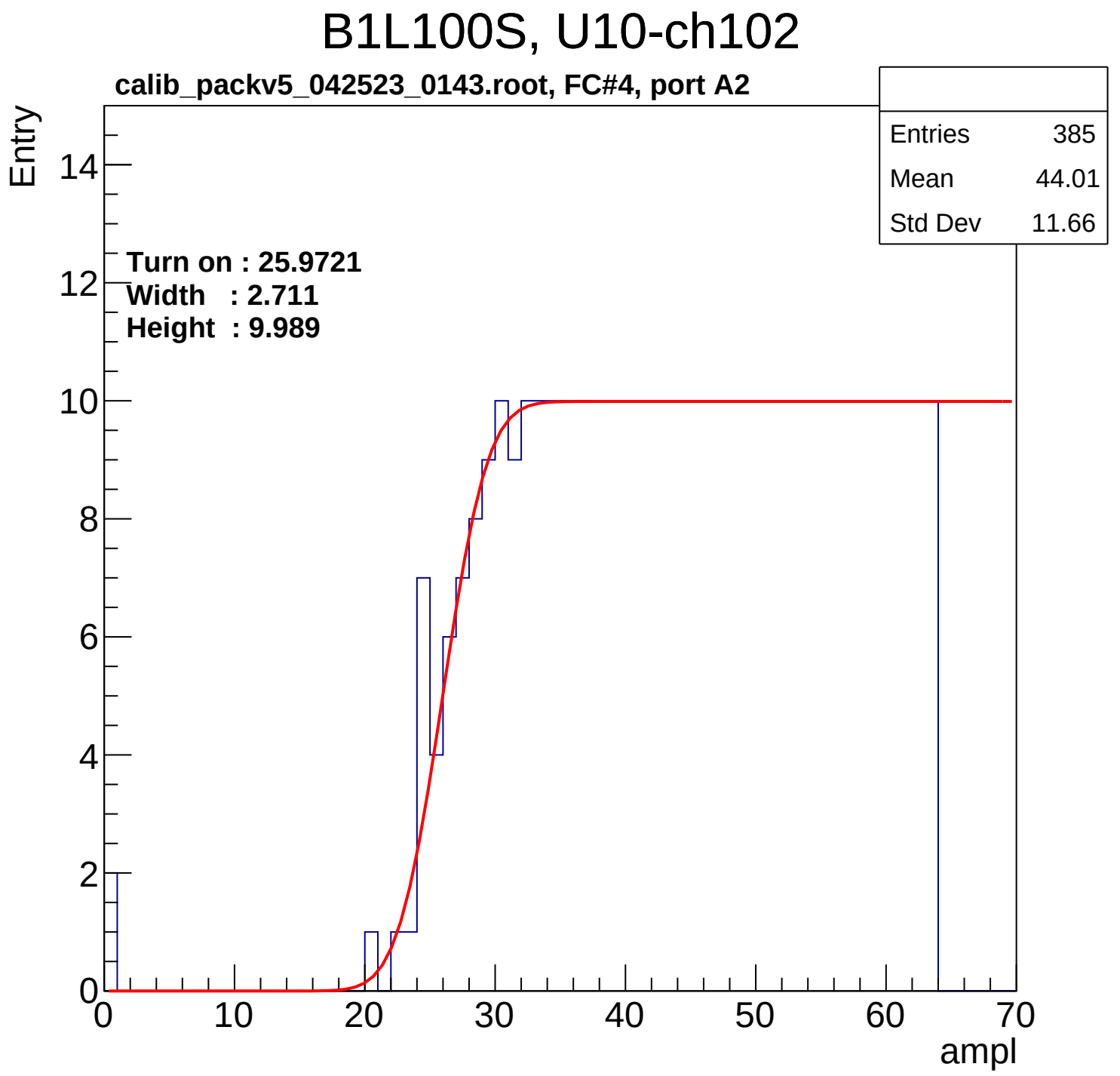
B1L100S, U10-ch102
calib_packv5_042523_0143.root, FC#4, port A2
Entries 385
Mean 44.01
Std Dev 11.66
Turn on : 25.9721
Width : 2.711
Height : 9.989
Entry
ampl
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6
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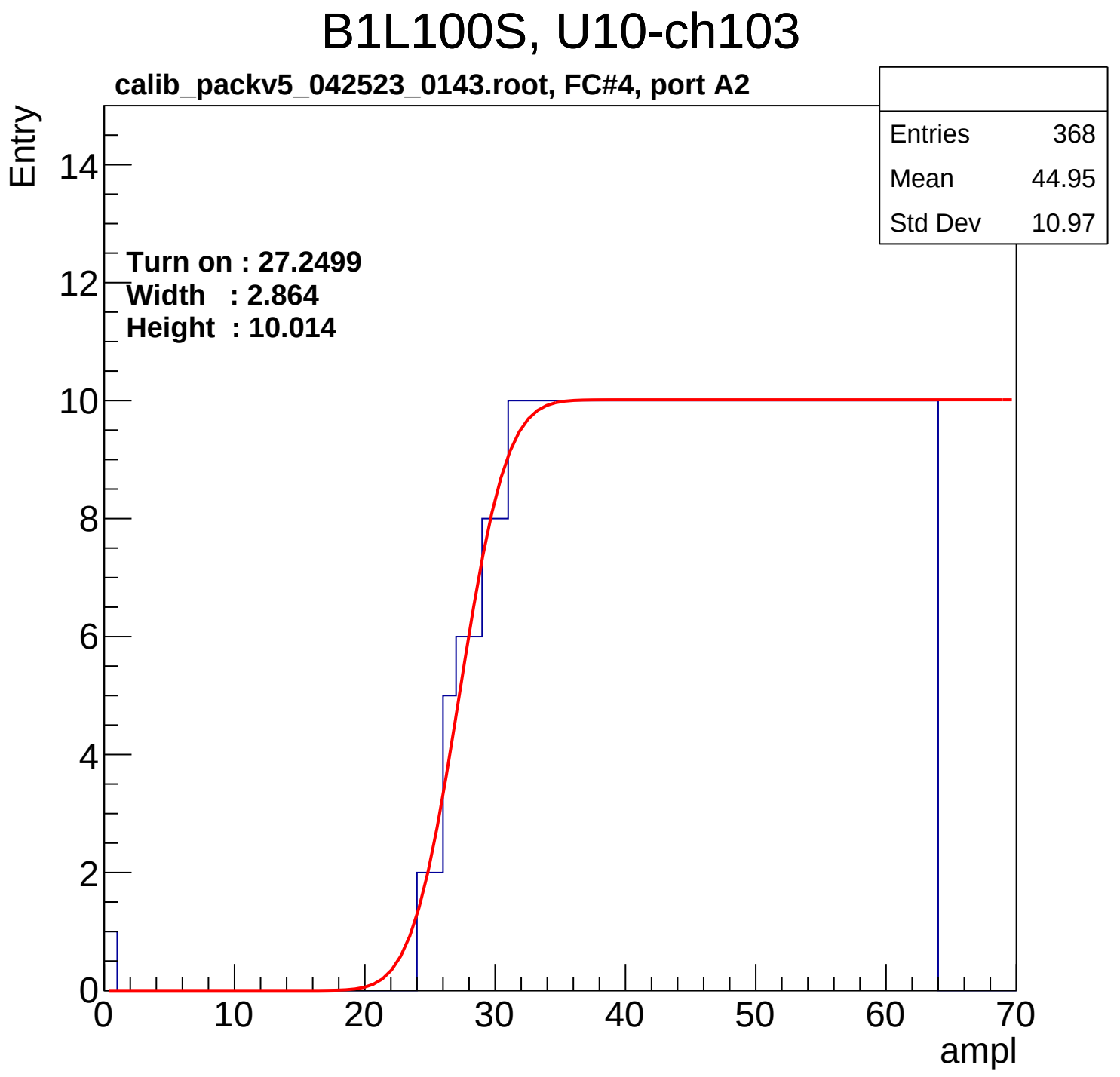
B1L100S, U10-ch103
calib_packv5_042523_0143.root, FC#4, port A2
Entries 368
Mean 44.95
Std Dev 10.97
Turn on : 27.2499
Width : 2.864
Height : 10.014
Entry
ampl
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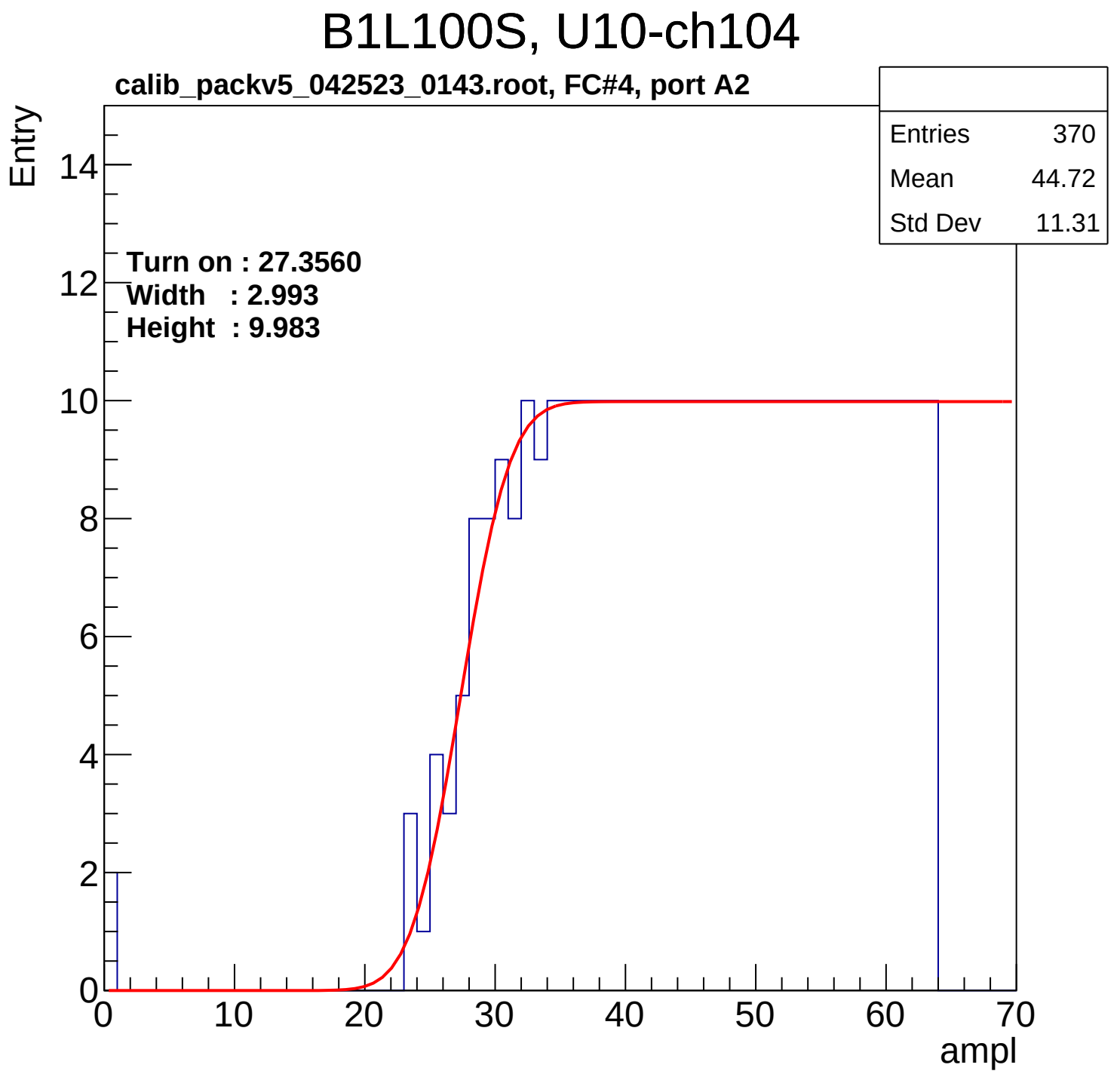
B1L100S, U10-ch104
calib_packv5_042523_0143.root, FC#4, port A2
Entries 370
Mean 44.72
Std Dev 11.31
Turn on : 27.3560
Width : 2.993
Height : 9.983
Entry
ampl
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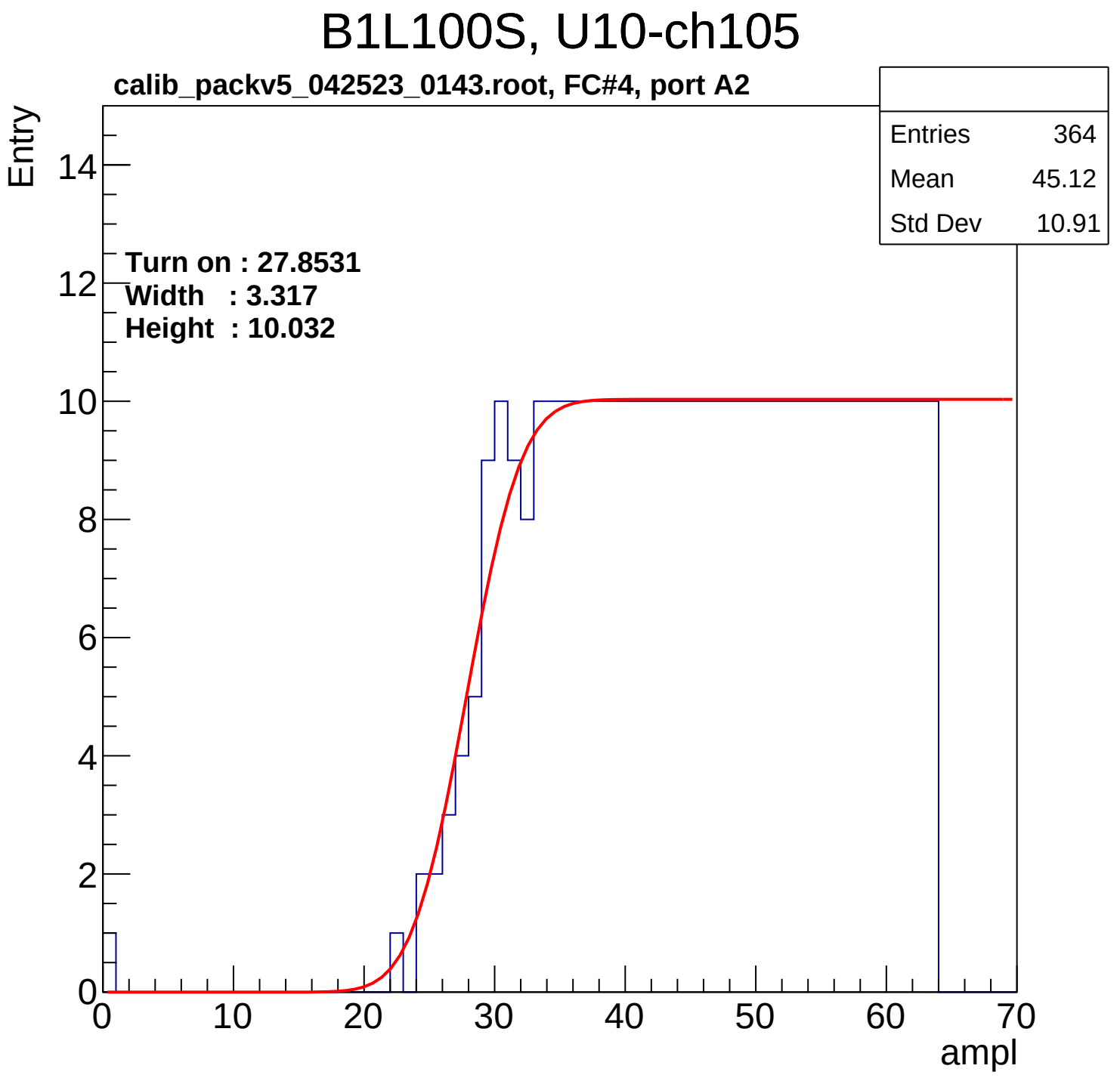
B1L100S, U10-ch105
calib_packv5_042523_0143.root, FC#4, port A2
Entries 364
Mean 45.12
Std Dev 10.91
Turn on : 27.8531
Width : 3.317
Height : 10.032
Entry
ampl
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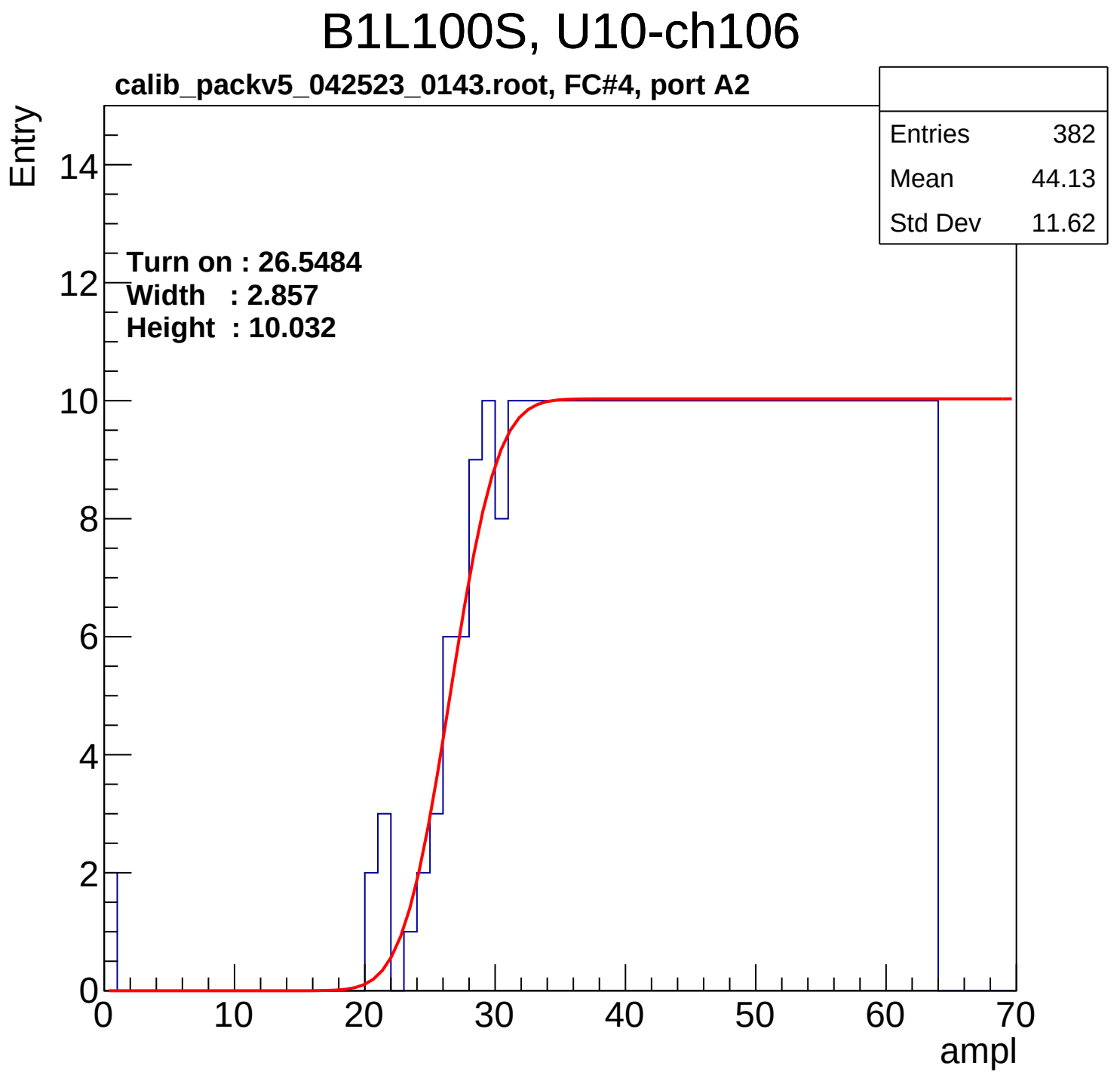
B1L100S, U10-ch106
calib_packv5_042523_0143.root, FC#4, port A2
Entries 382
Mean 44.13
Std Dev 11.62
Turn on : 26.5484
Width : 2.857
Height : 10.032
Entry
ampl
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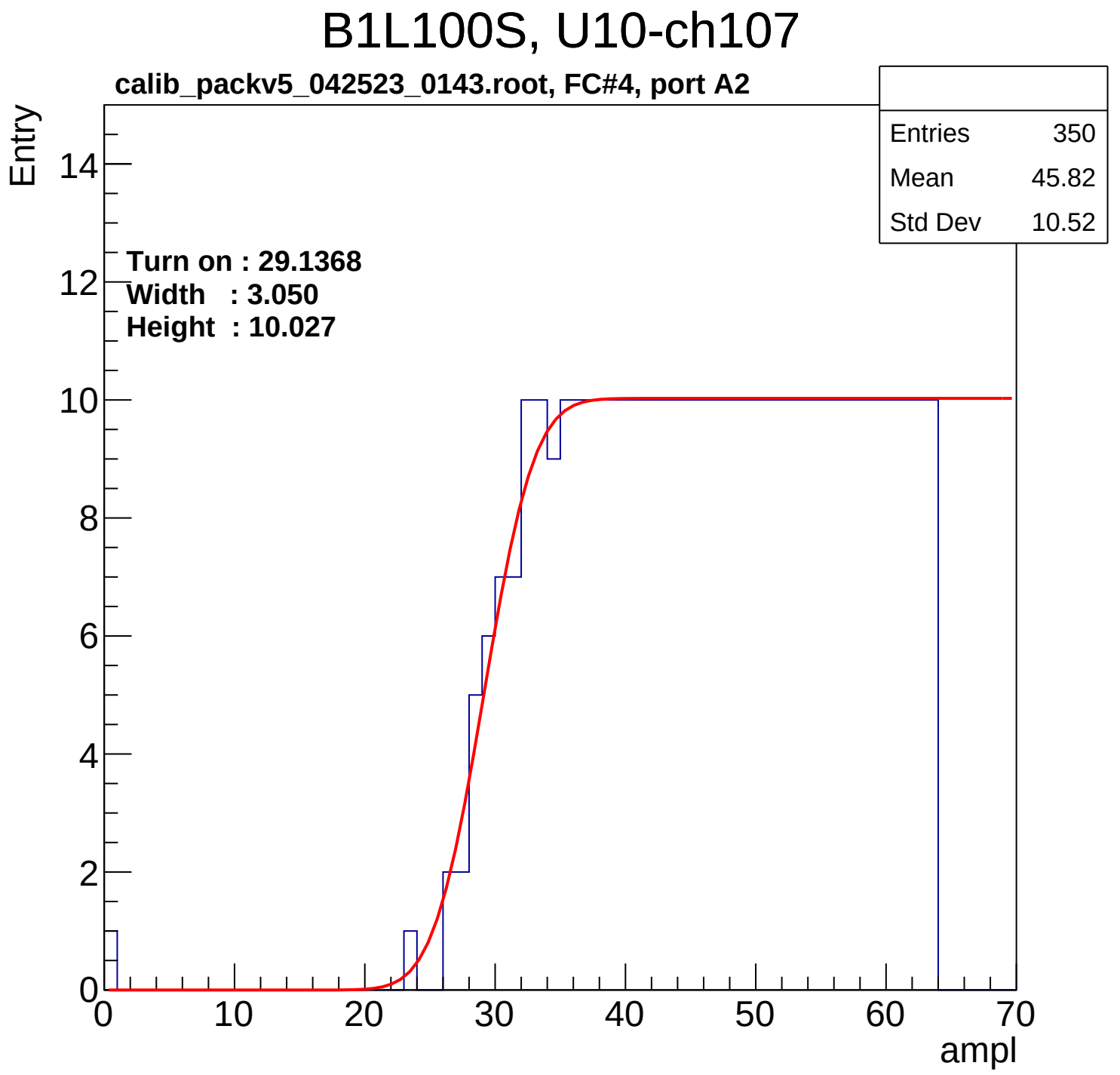
B1L100S, U10-ch107
calib_packv5_042523_0143.root, FC#4, port A2
Entries 350
Mean 45.82
Std Dev 10.52
Turn on : 29.1368
Width : 3.050
Height : 10.027
Entry
ampl
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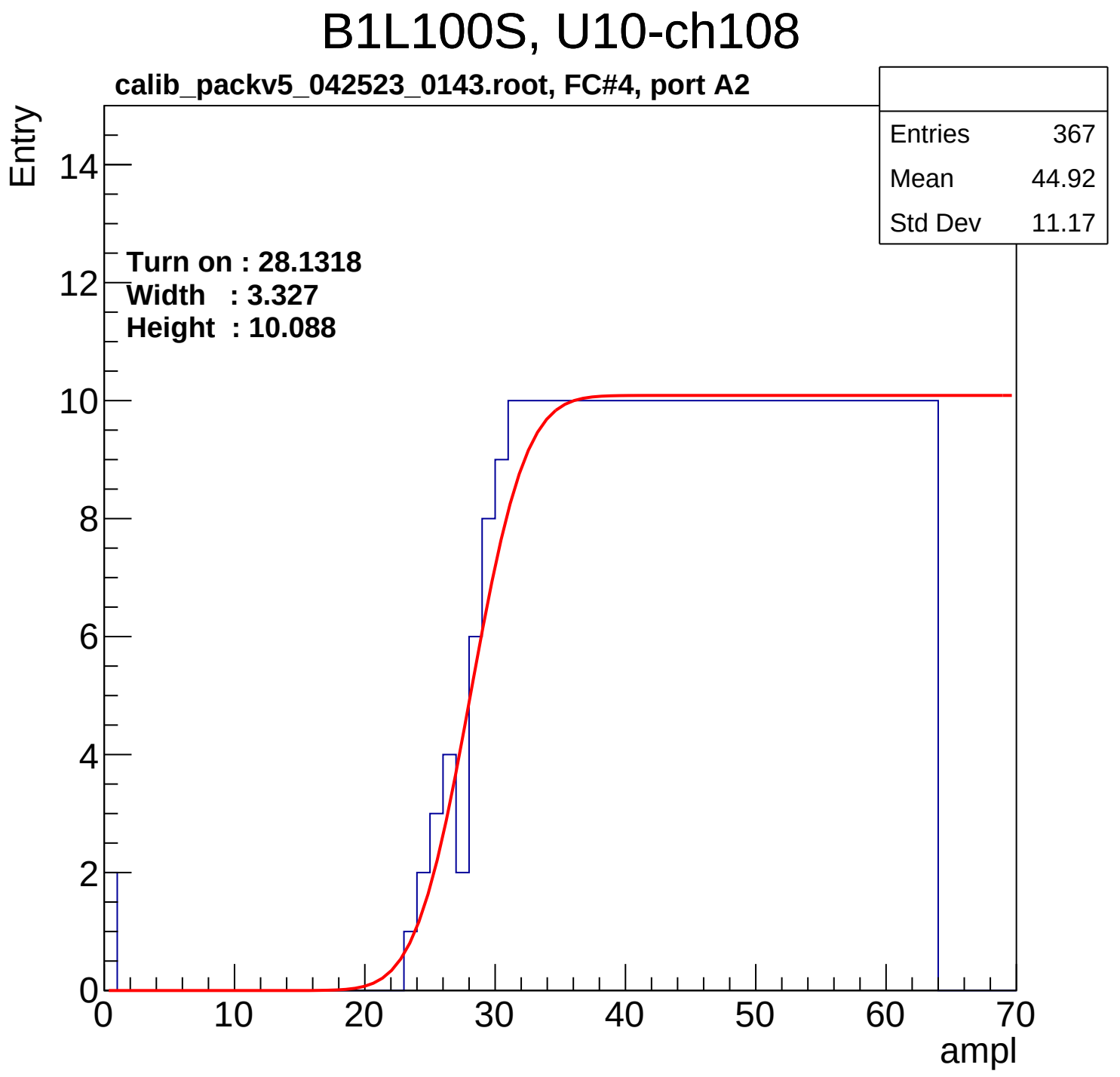
B1L100S, U10-ch108
calib_packv5_042523_0143.root, FC#4, port A2
Entries 367
Mean 44.92
Std Dev 11.17
Turn on : 28.1318
Width : 3.327
Height : 10.088
Entry
ampl
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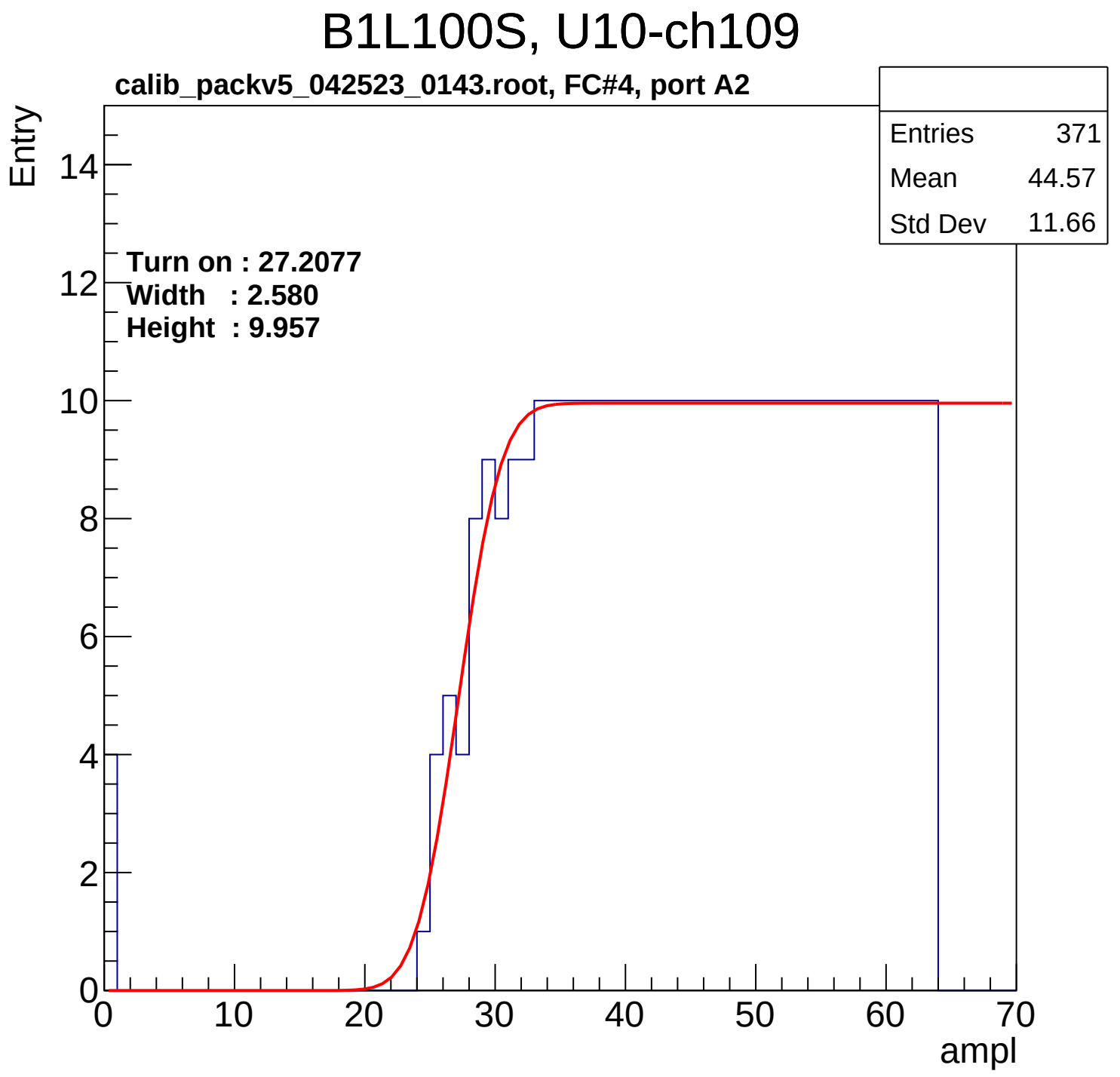
B1L100S, U10-ch109
calib_packv5_042523_0143.root, FC#4, port A2
Entries 371
Mean 44.57
Std Dev 11.66
Turn on : 27.2077
Width : 2.580
Height : 9.957
Entry
ampl
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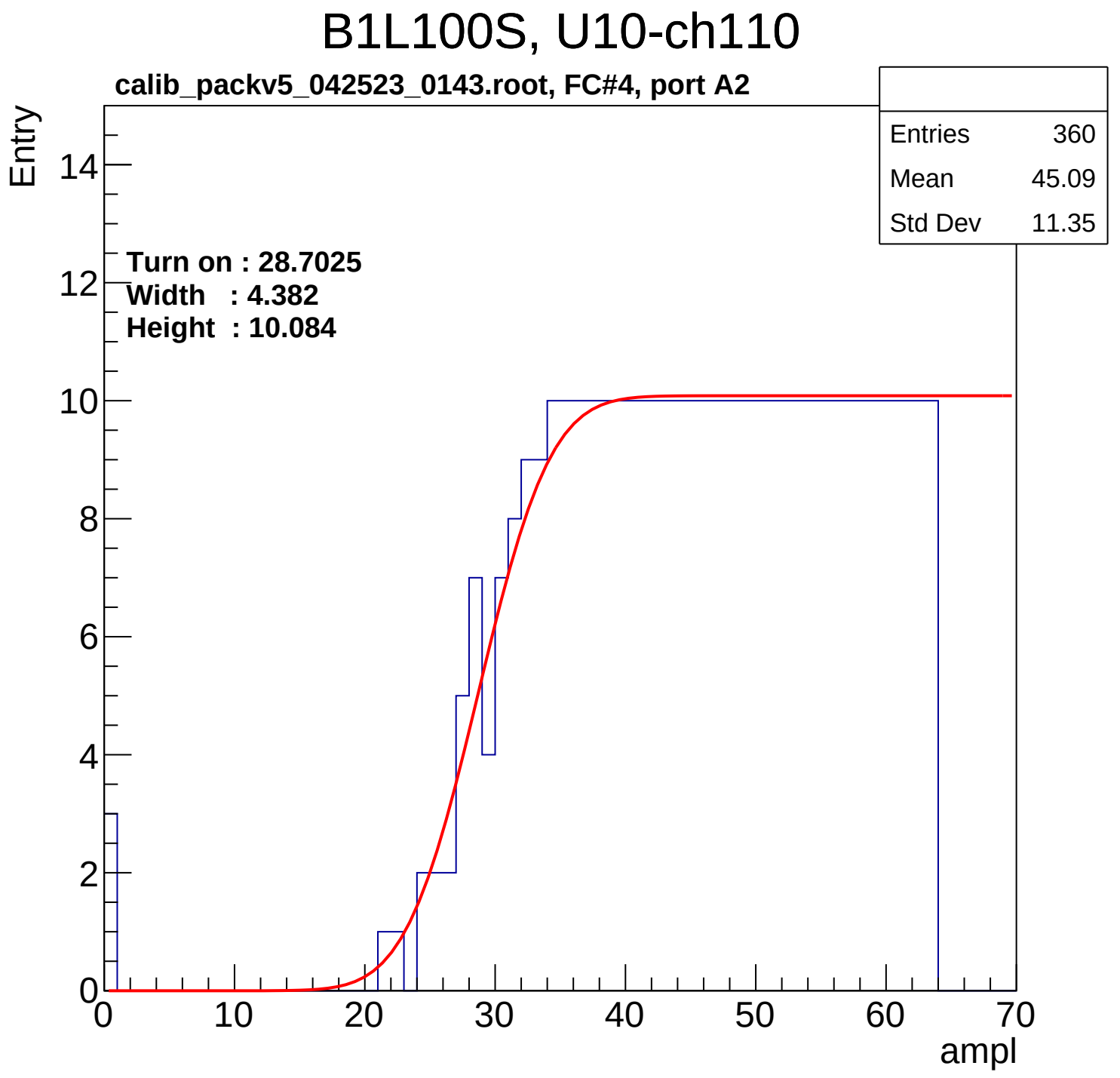
B1L100S, U10-ch110
calib_packv5_042523_0143.root, FC#4, port A2
Entries 360
Mean 45.09
Std Dev 11.35
Turn on : 28.7025
Width : 4.382
Height : 10.084
Entry
ampl
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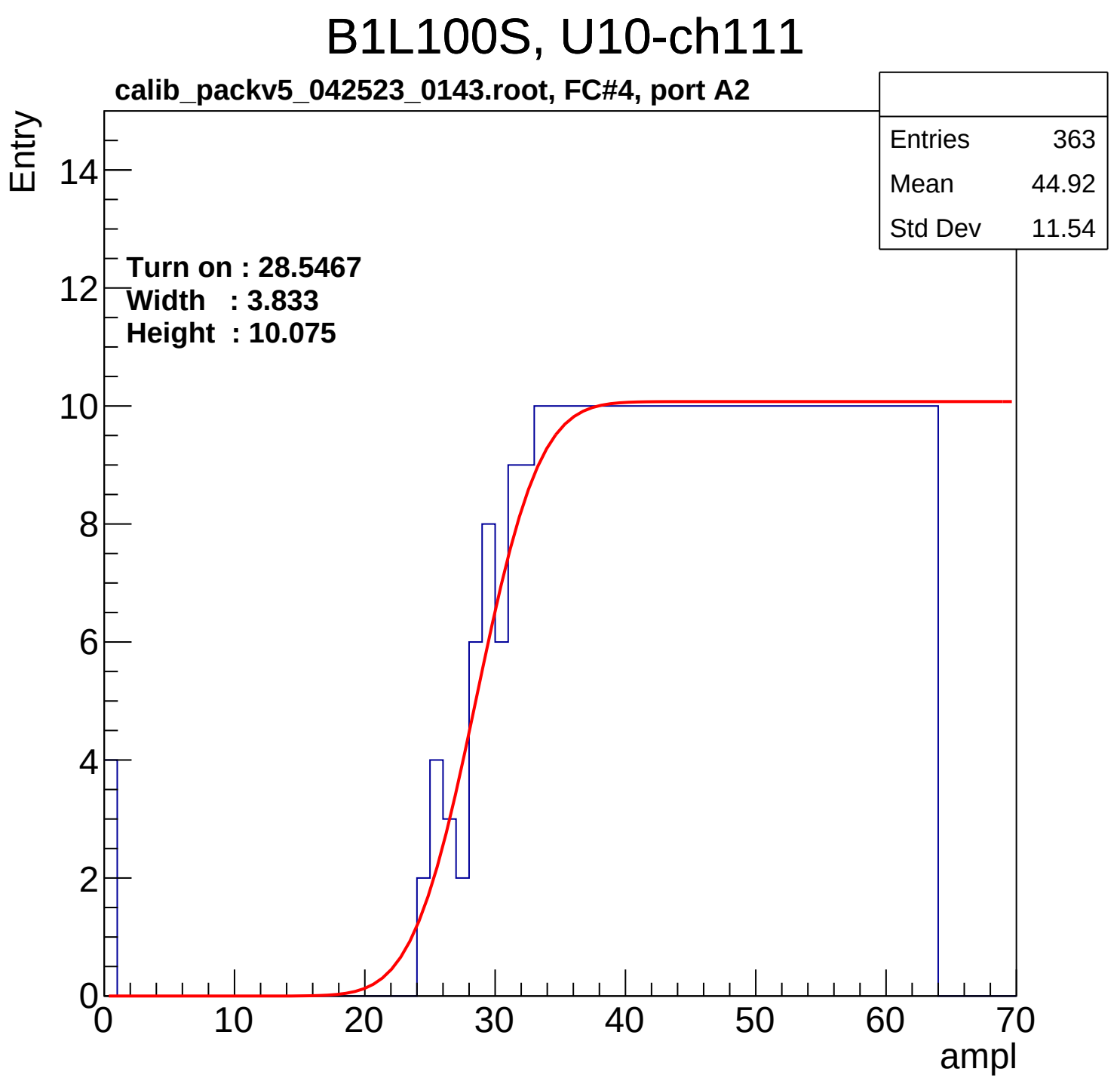
B1L100S, U10-ch111
calib_packv5_042523_0143.root, FC#4, port A2
Entries 363
Mean 44.92
Std Dev 11.54
Turn on : 28.5467
Width : 3.833
Height : 10.075
Entry
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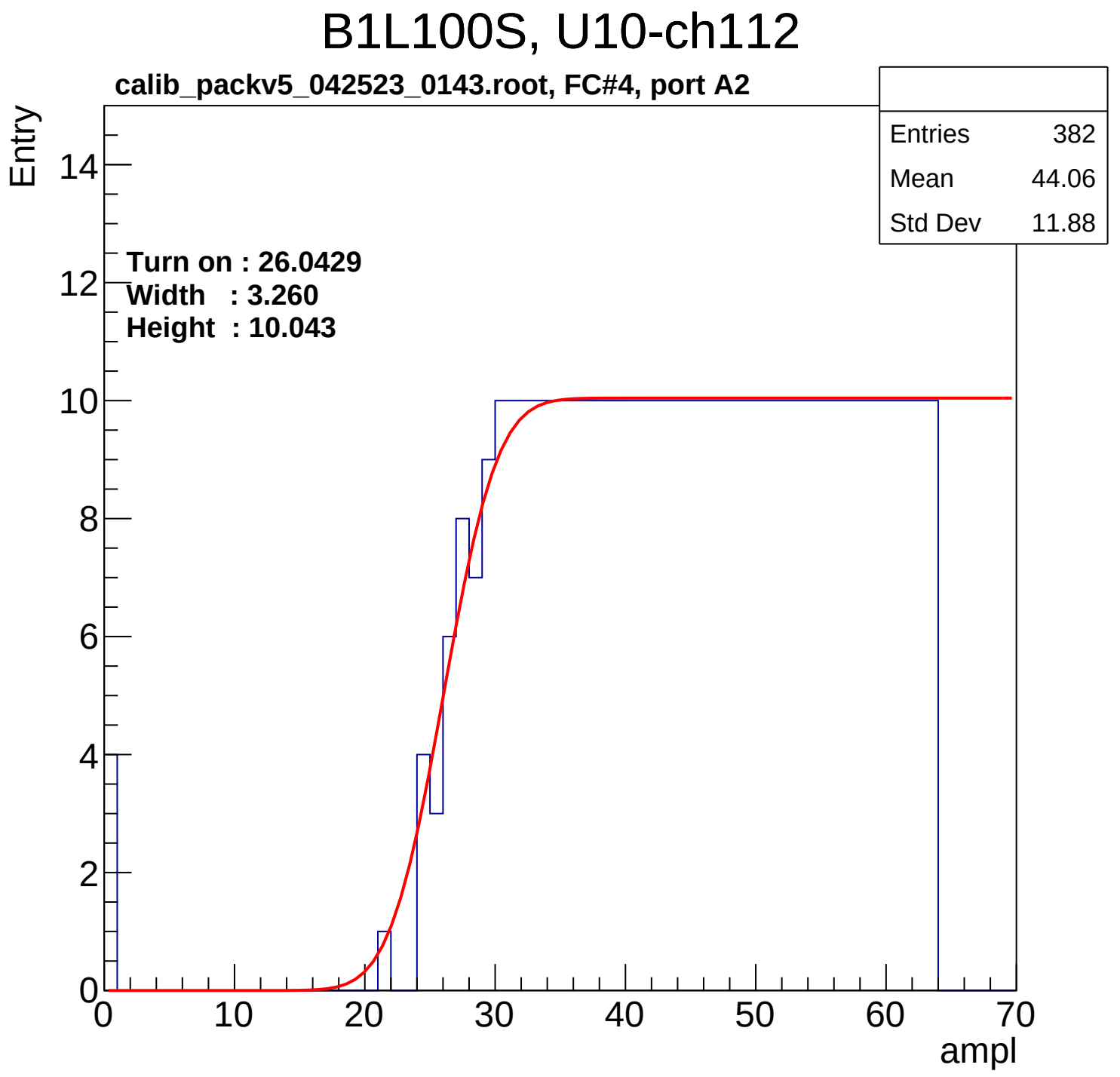
B1L100S, U10-ch112
calib_packv5_042523_0143.root, FC#4, port A2
Entries 382
Mean 44.06
Std Dev 11.88
Turn on : 26.0429
Width : 3.260
Height : 10.043
Entry
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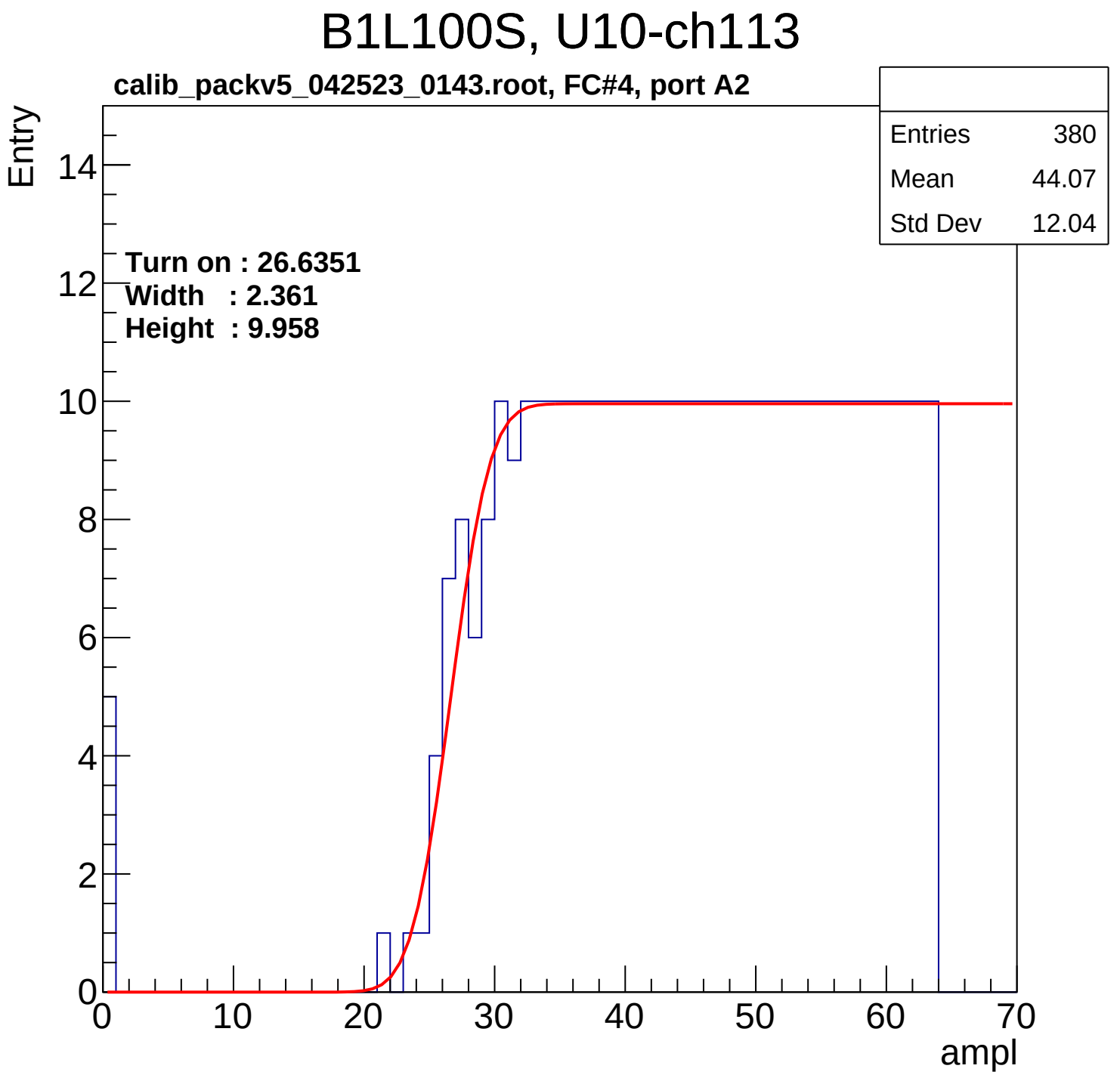
B1L100S, U10-ch113
calib_packv5_042523_0143.root, FC#4, port A2
Entries 380
Mean 44.07
Std Dev 12.04
Turn on : 26.6351
Width : 2.361
Height : 9.958
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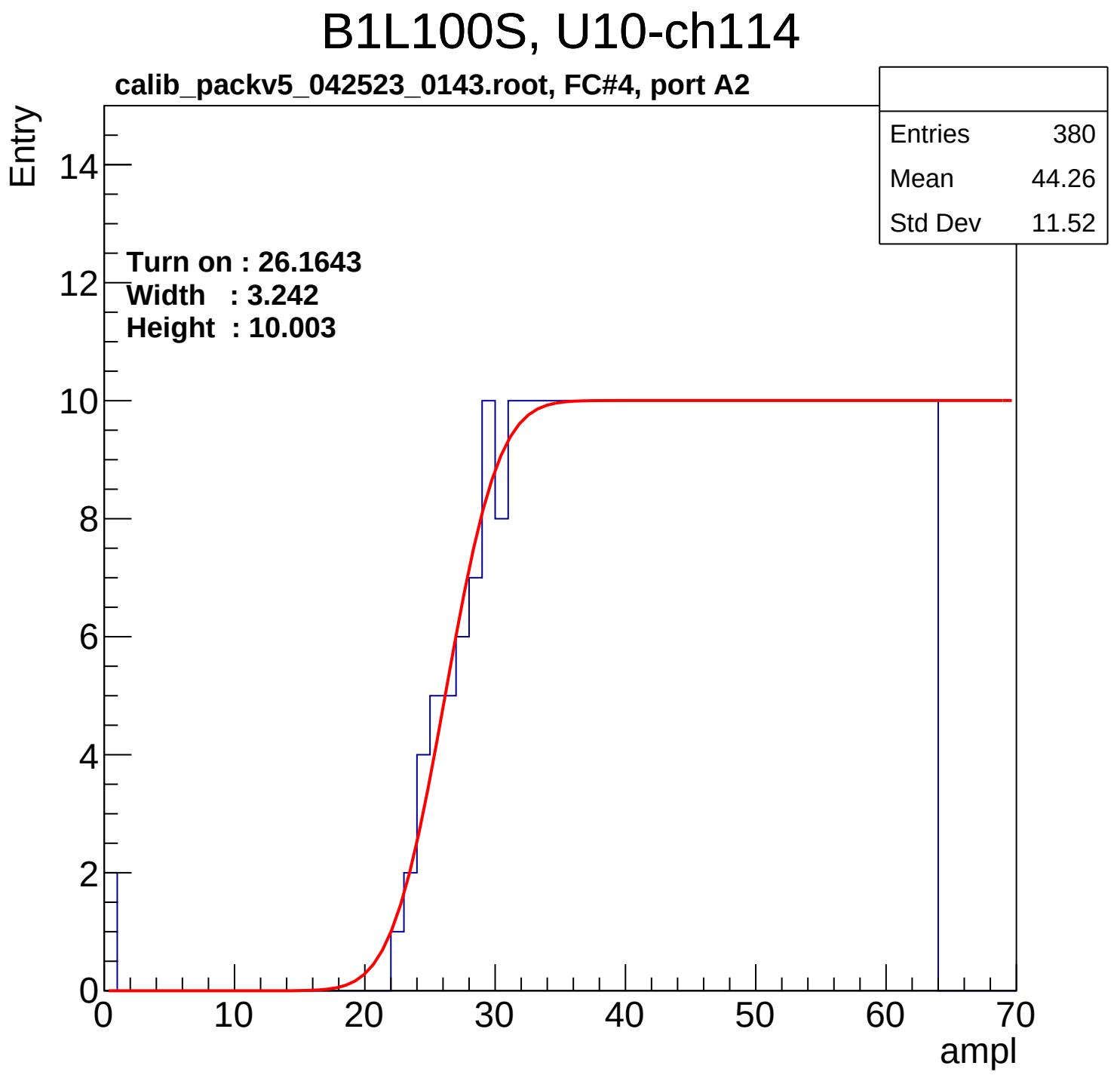
B1L100S, U10-ch114
calib_packv5_042523_0143.root, FC#4, port A2
Entries 380
Mean 44.26
Std Dev 11.52
Turn on : 26.1643
Width : 3.242
Height : 10.003
Entry
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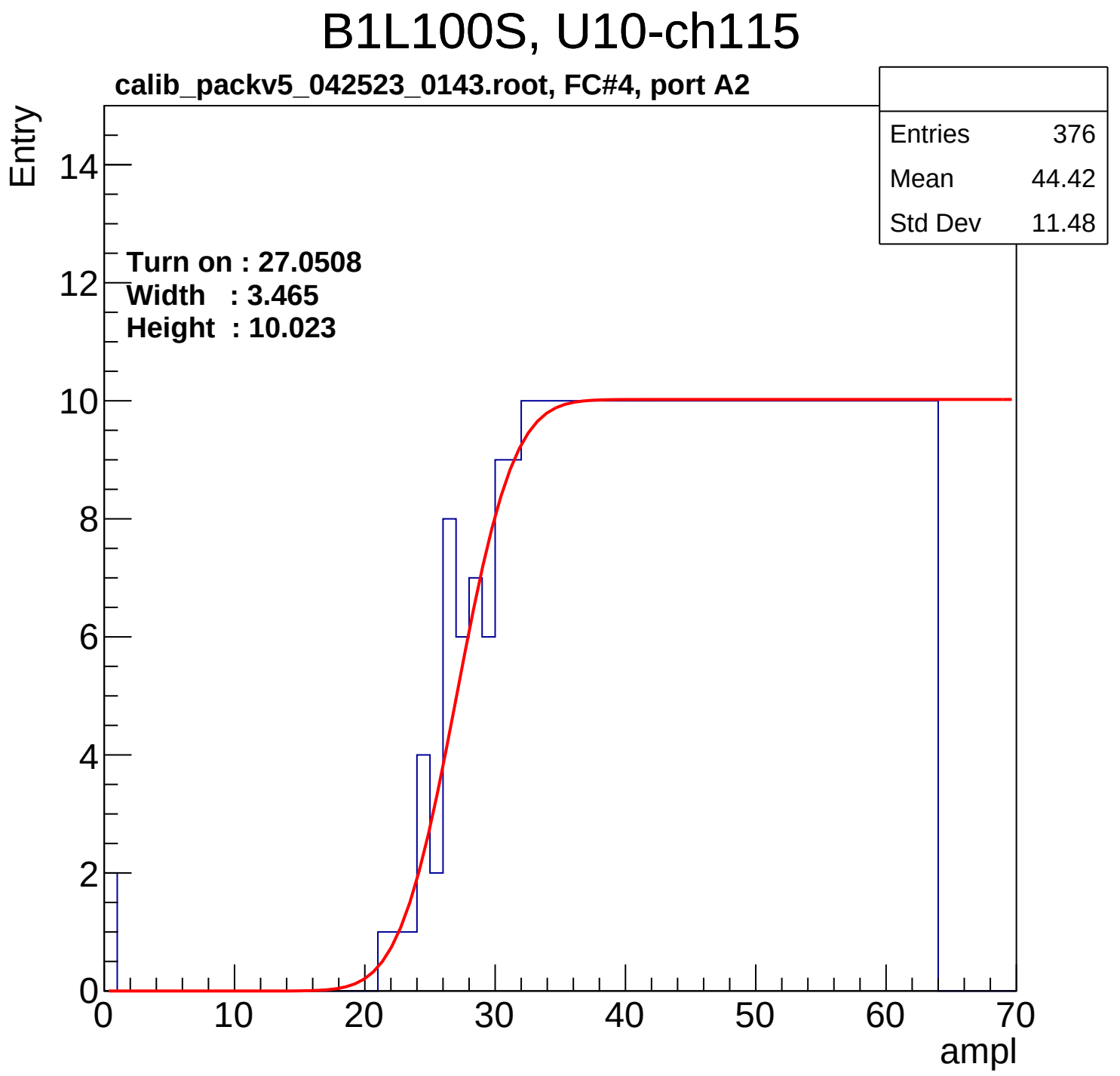
B1L100S, U10-ch115
calib_packv5_042523_0143.root, FC#4, port A2
Entries 376
Mean 44.42
Std Dev 11.48
Turn on : 27.0508
Width : 3.465
Height : 10.023
Entry
ampl
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4
6
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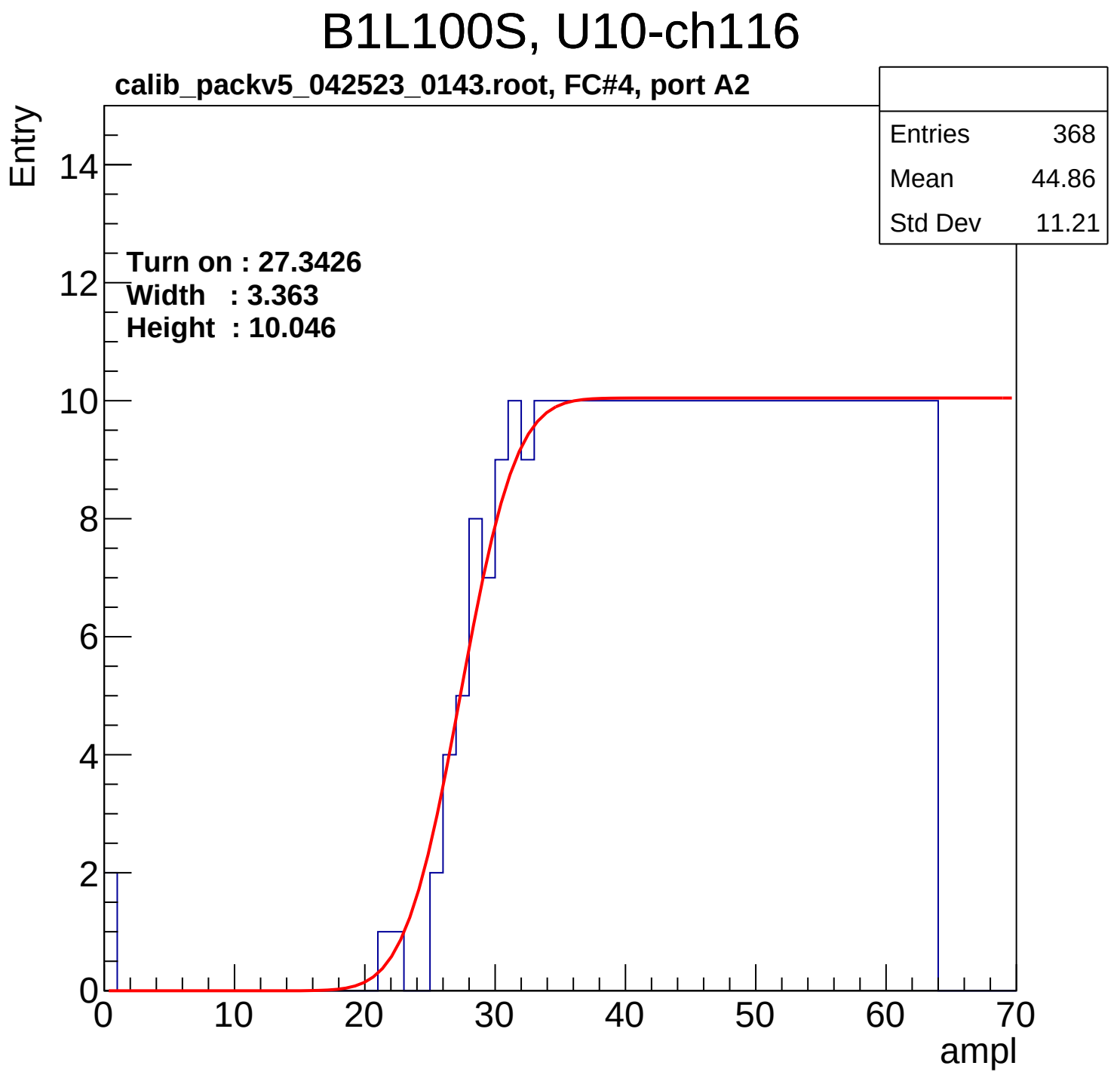
B1L100S, U10-ch116
calib_packv5_042523_0143.root, FC#4, port A2
Entries 368
Mean 44.86
Std Dev 11.21
Turn on : 27.3426
Width : 3.363
Height : 10.046
Entry
ampl
0
2
4
6
8
10
12
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0
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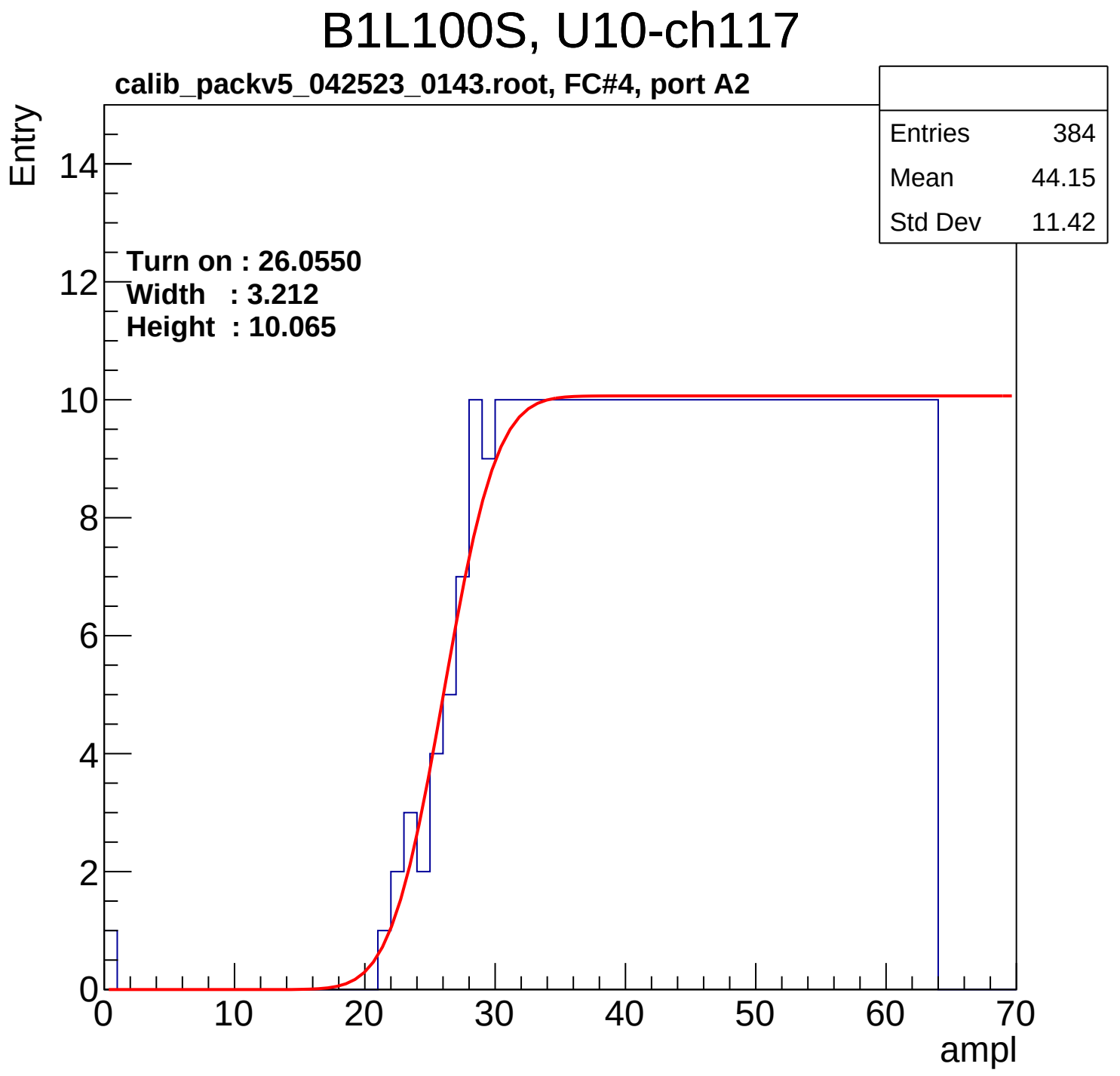
B1L100S, U10-ch117
calib_packv5_042523_0143.root, FC#4, port A2
Entries 384
Mean 44.15
Std Dev 11.42
Turn on : 26.0550
Width : 3.212
Height : 10.065
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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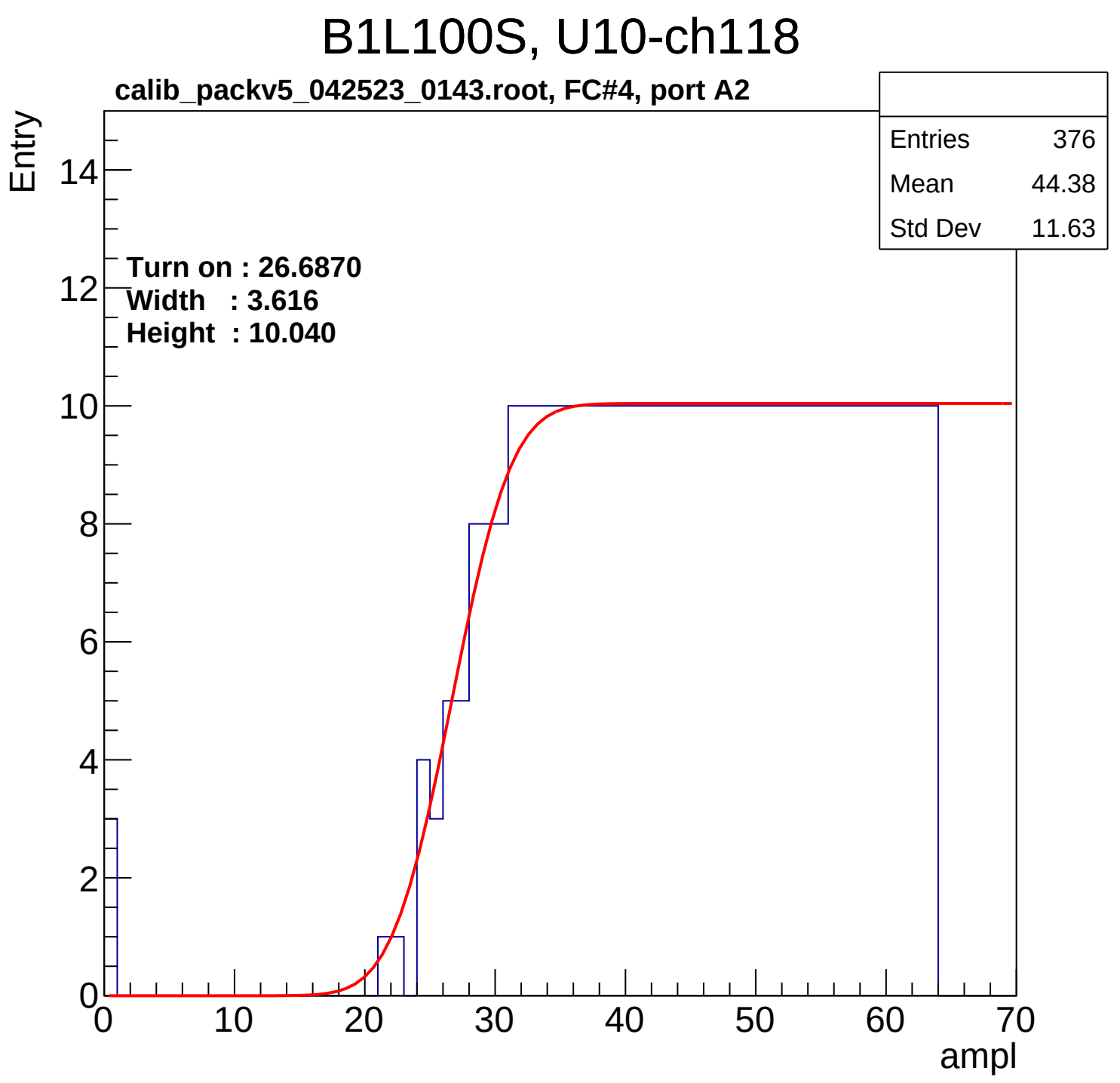
B1L100S, U10-ch118
calib_packv5_042523_0143.root, FC#4, port A2
Entries 376
Mean 44.38
Std Dev 11.63
Turn on : 26.6870
Width : 3.616
Height : 10.040
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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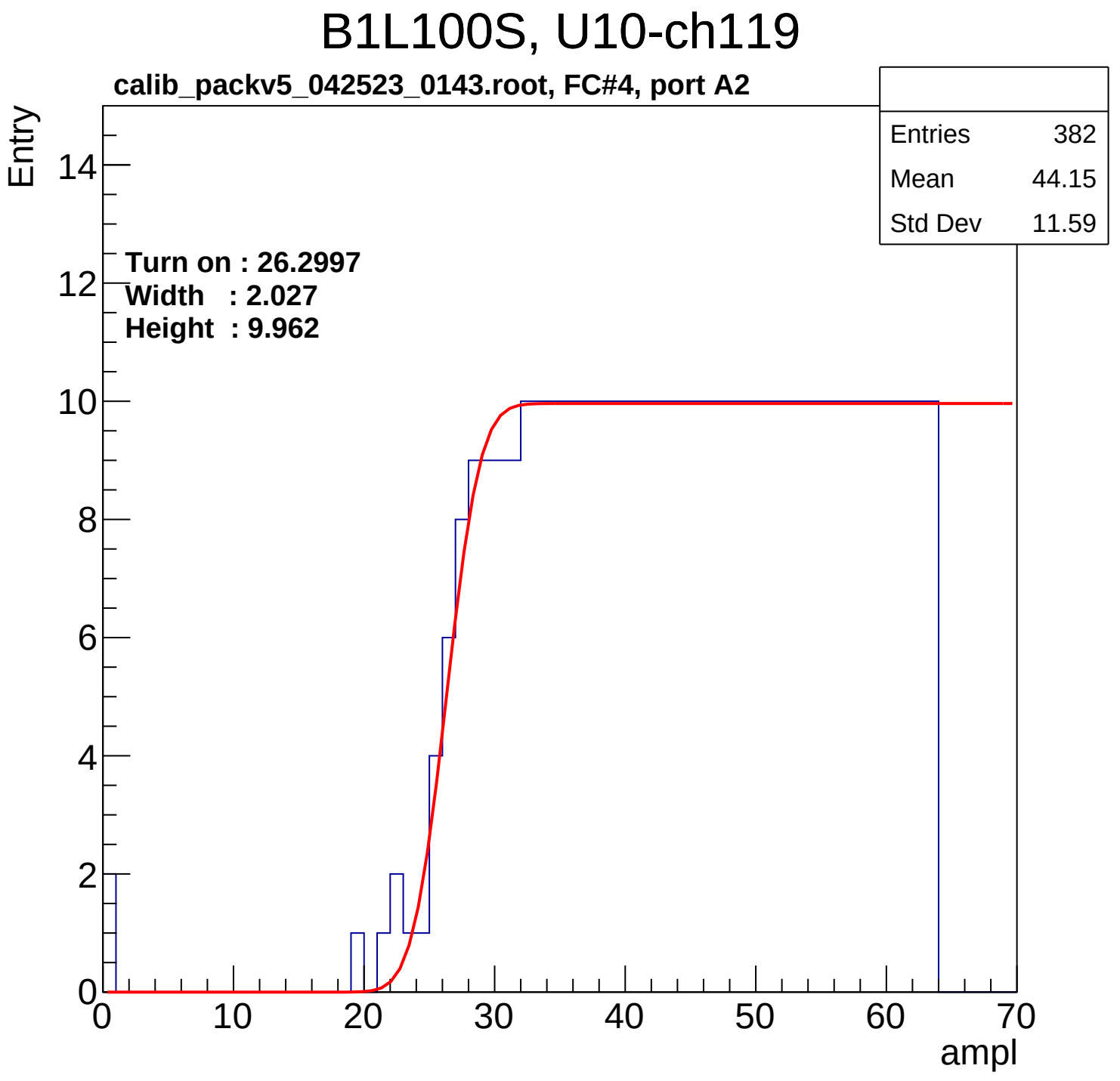
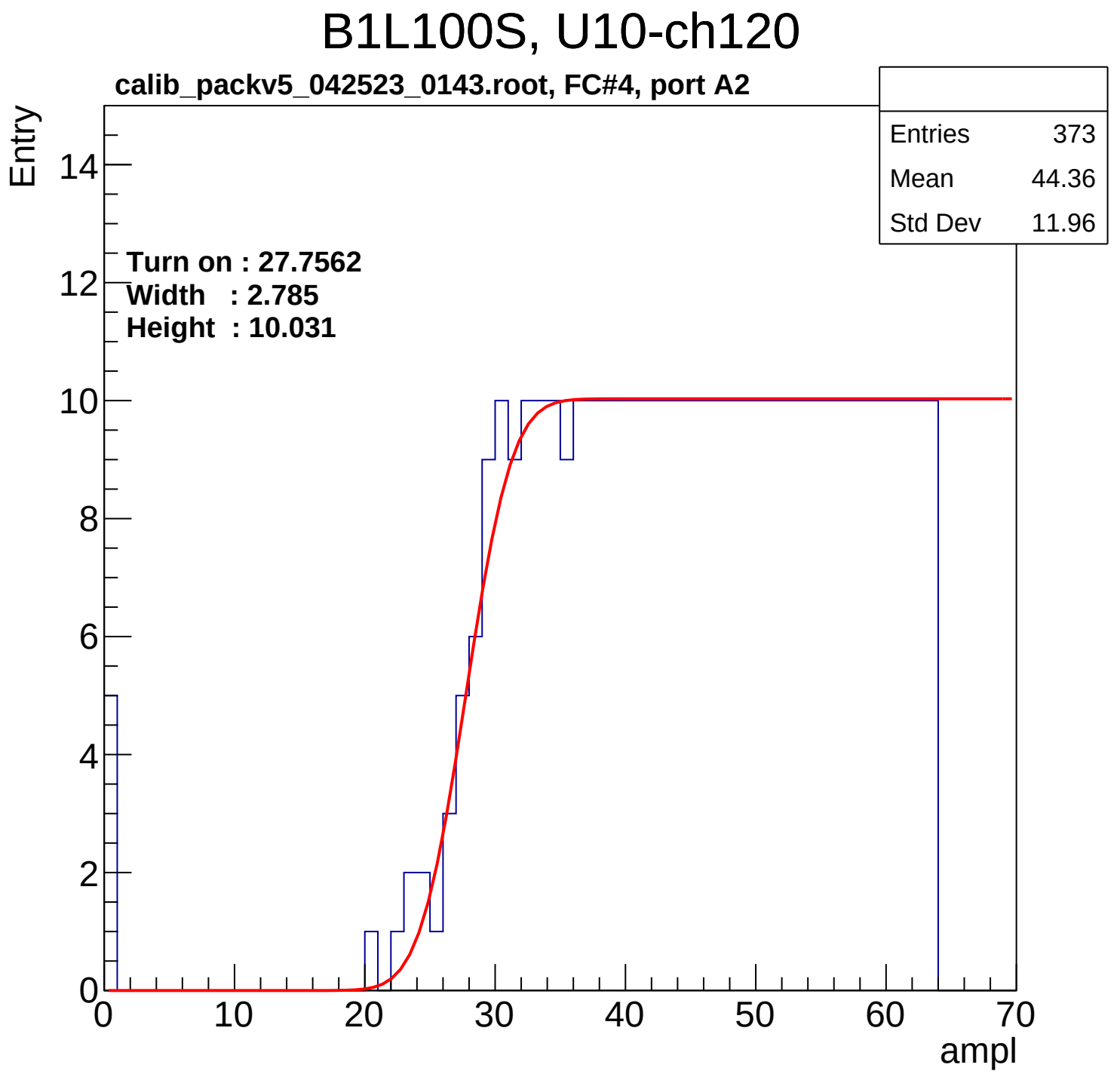

B1L100S, U10-ch119
calib_packv5_042523_0143.root, FC#4, port A2
Entries 382
Mean 44.15
Std Dev 11.59
Turn on : 26.2997
Width : 2.027
Height : 9.962
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L100S, U10-ch120
calib_packv5_042523_0143.root, FC#4, port A2
Entries 373
Mean 44.36
Std Dev 11.96
Turn on : 27.7562
Width : 2.785
Height : 10.031
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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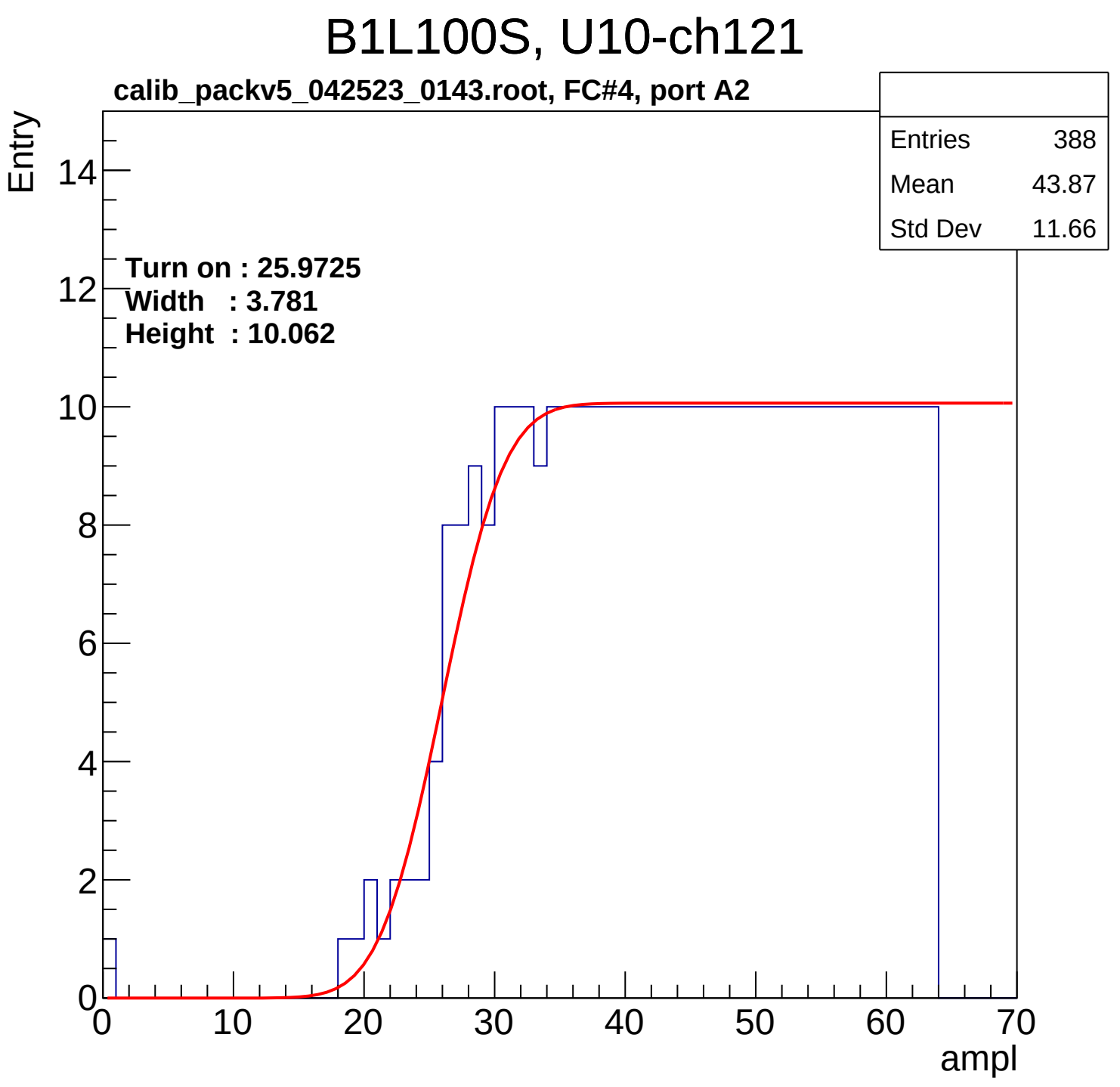
B1L100S, U10-ch121
calib_packv5_042523_0143.root, FC#4, port A2
Entries 388
Mean 43.87
Std Dev 11.66
Turn on : 25.9725
Width : 3.781
Height : 10.062
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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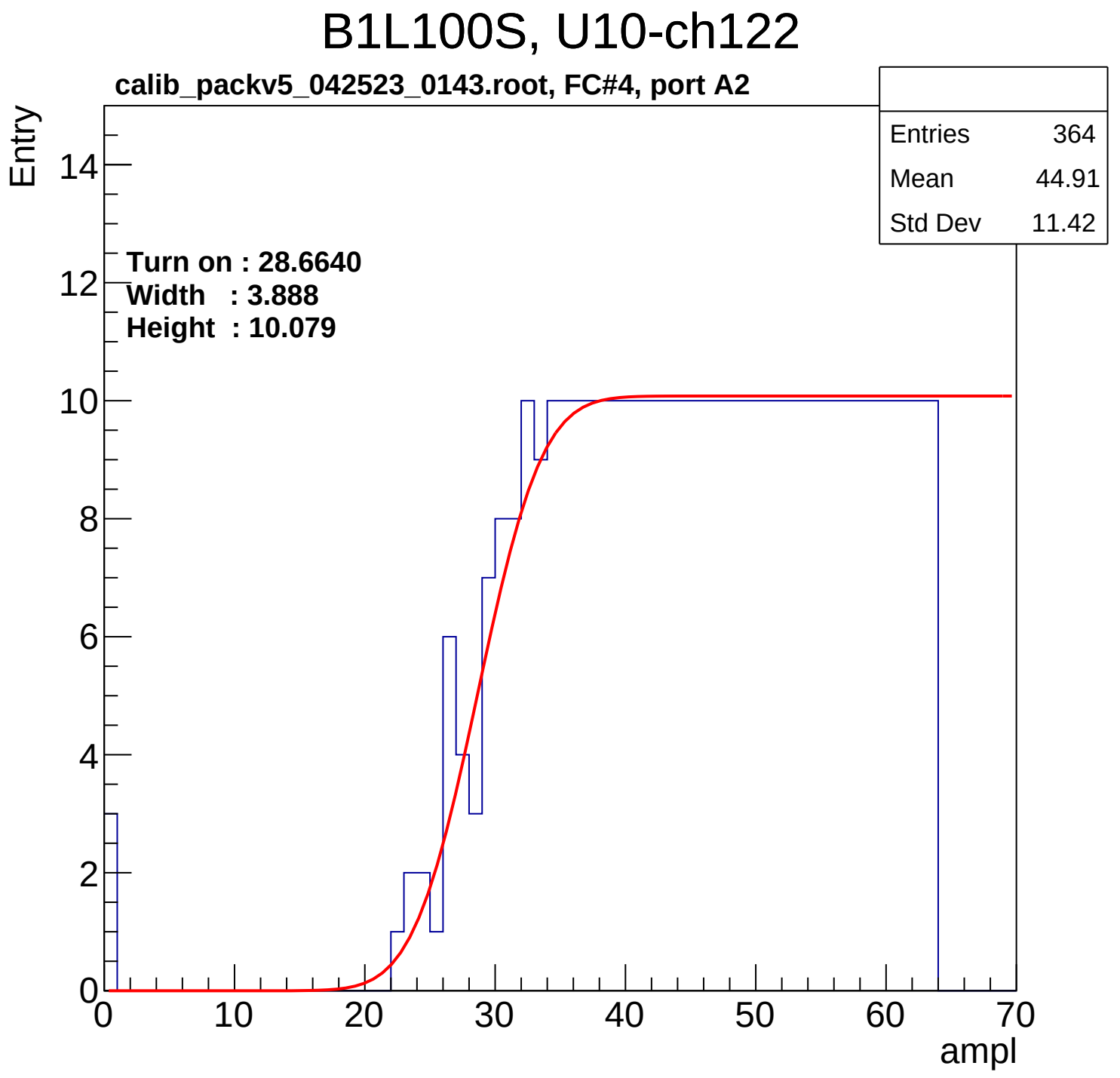
B1L100S, U10-ch122
calib_packv5_042523_0143.root, FC#4, port A2
Entries 364
Mean 44.91
Std Dev 11.42
Turn on : 28.6640
Width : 3.888
Height : 10.079
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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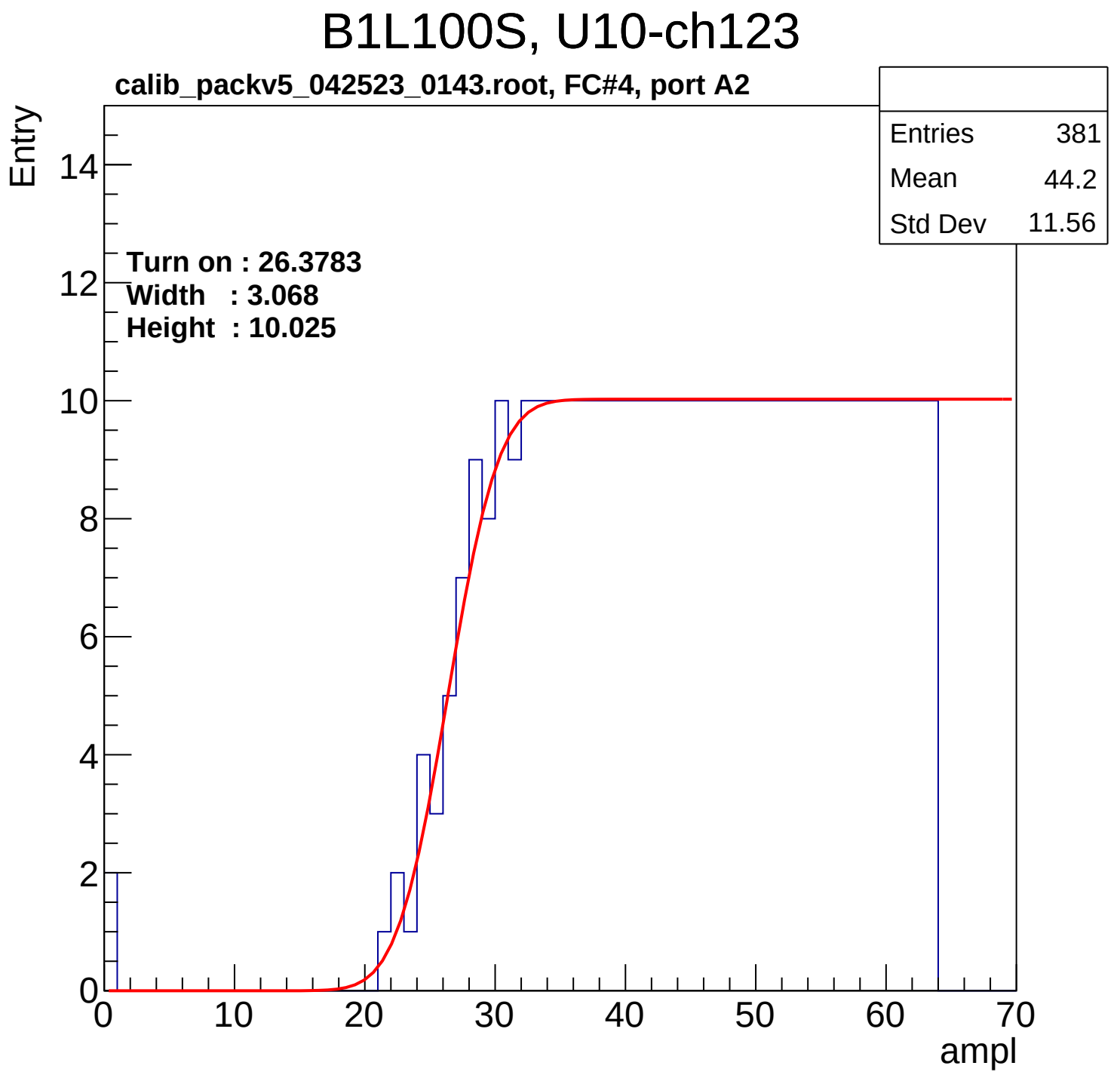
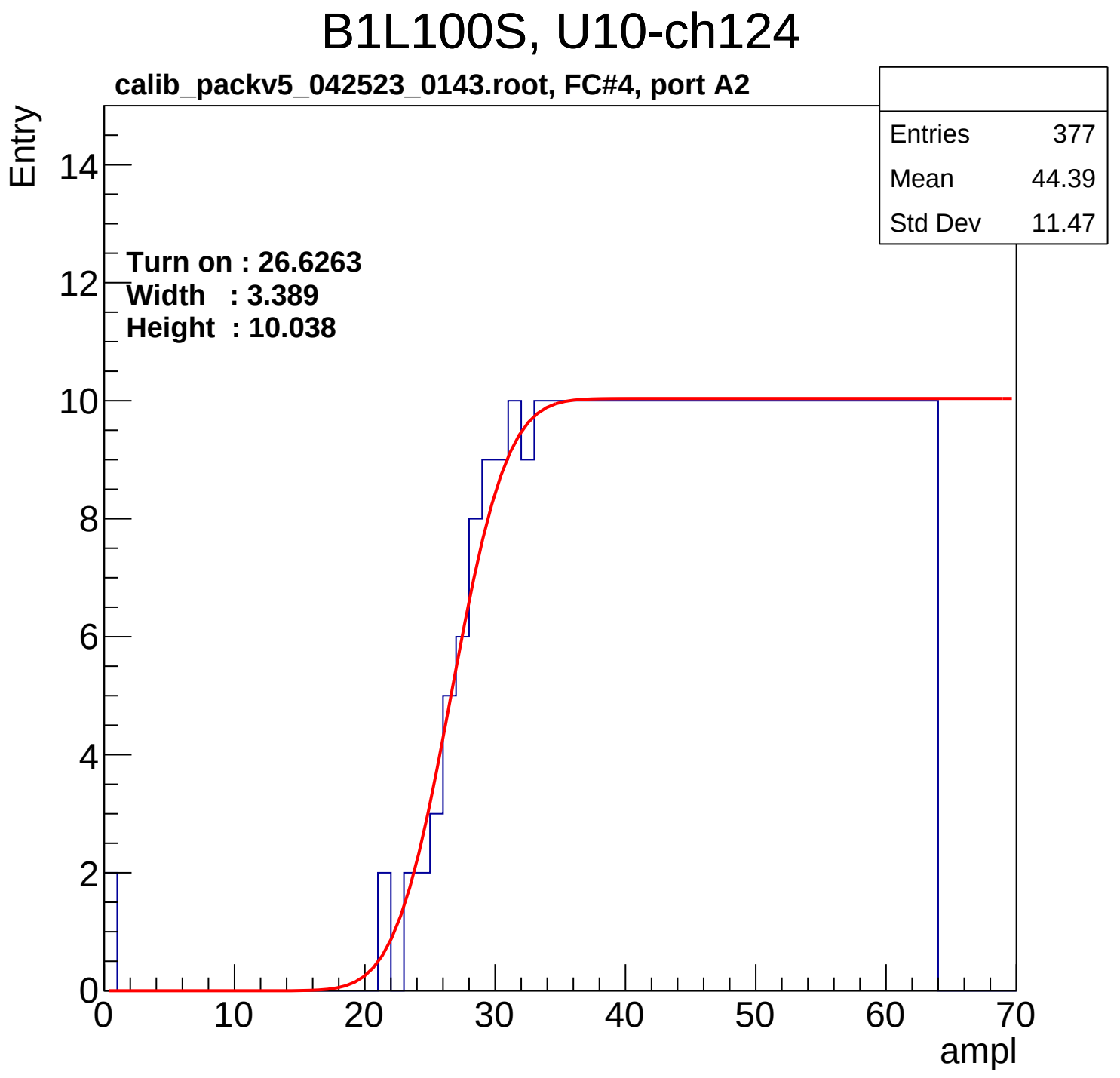

B1L100S, U10-ch123
calib_packv5_042523_0143.root, FC#4, port A2
Entries 381
Mean 44.2
Std Dev 11.56
Turn on : 26.3783
Width : 3.068
Height : 10.025
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L100S, U10-ch124
calib_packv5_042523_0143.root, FC#4, port A2
Entries 377
Mean 44.39
Std Dev 11.47
Turn on : 26.6263
Width : 3.389
Height : 10.038
Entry
ampl
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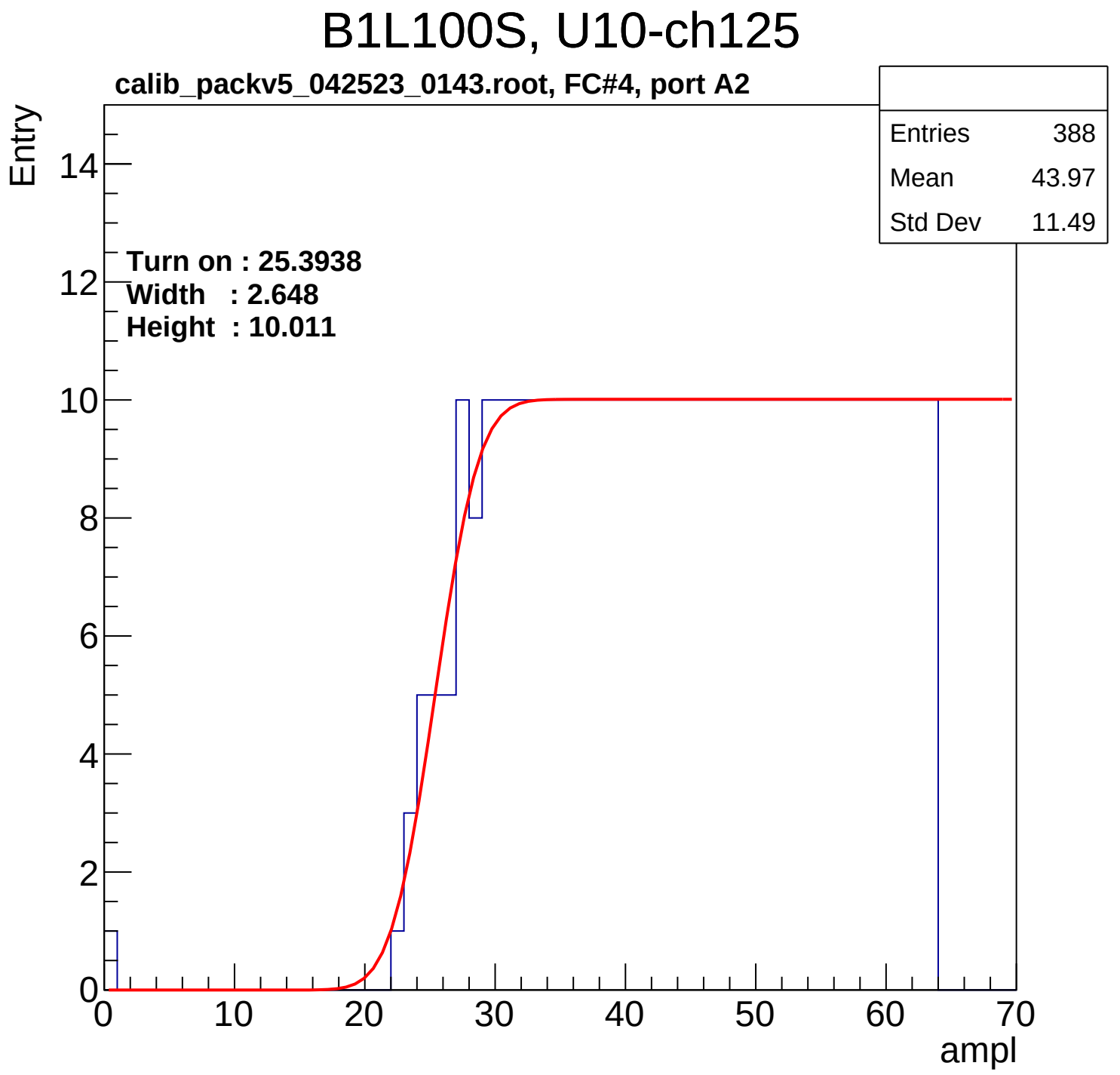
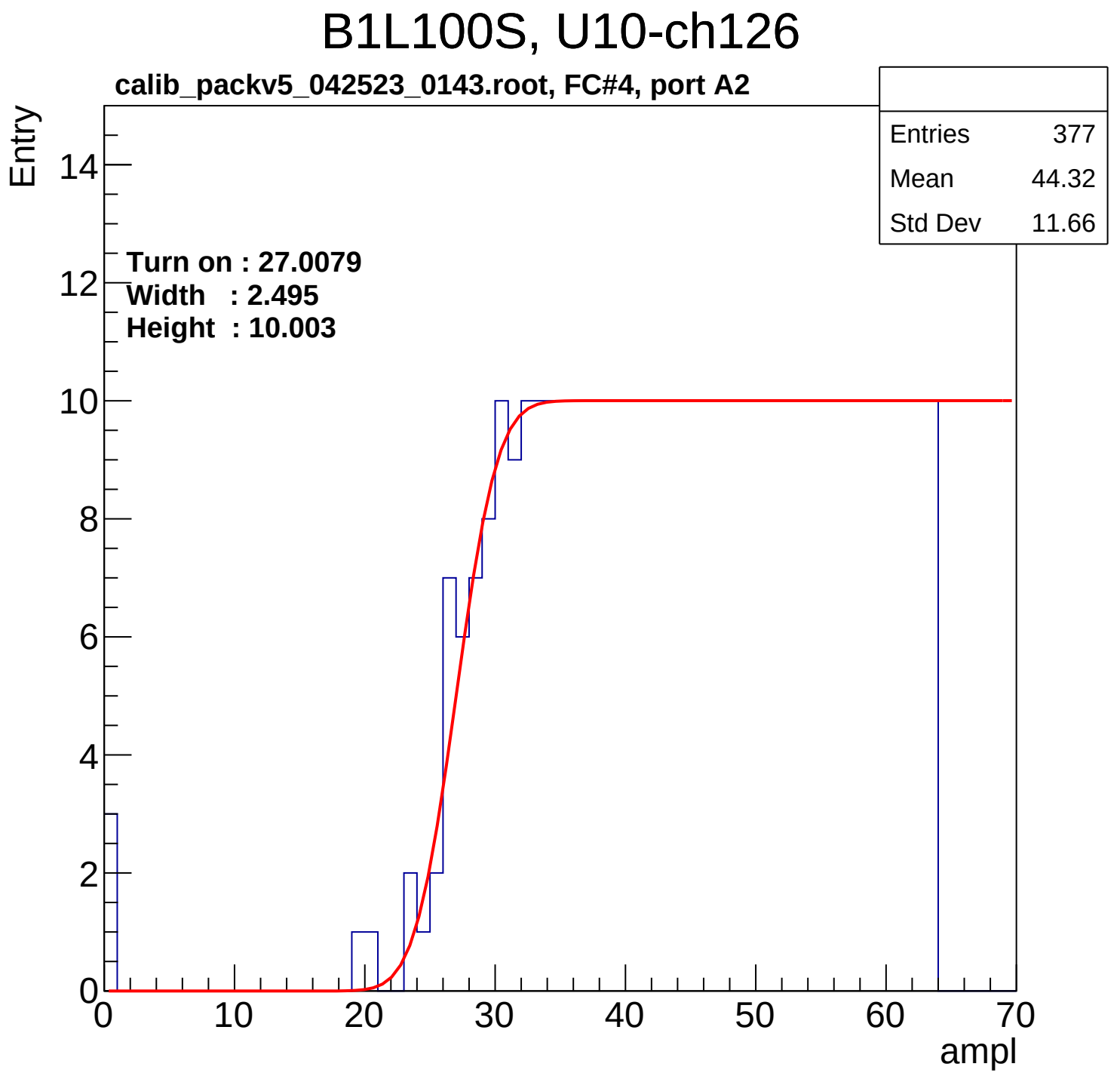
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L100S, U10-ch125
calib_packv5_042523_0143.root, FC#4, port A2
Entries 388
Mean 43.97
Std Dev 11.49
Turn on : 25.3938
Width : 2.648
Height : 10.011
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L100S, U10-ch126
calib_packv5_042523_0143.root, FC#4, port A2
Entries 377
Mean 44.32
Std Dev 11.66
Turn on : 27.0079
Width : 2.495
Height : 10.003
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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60
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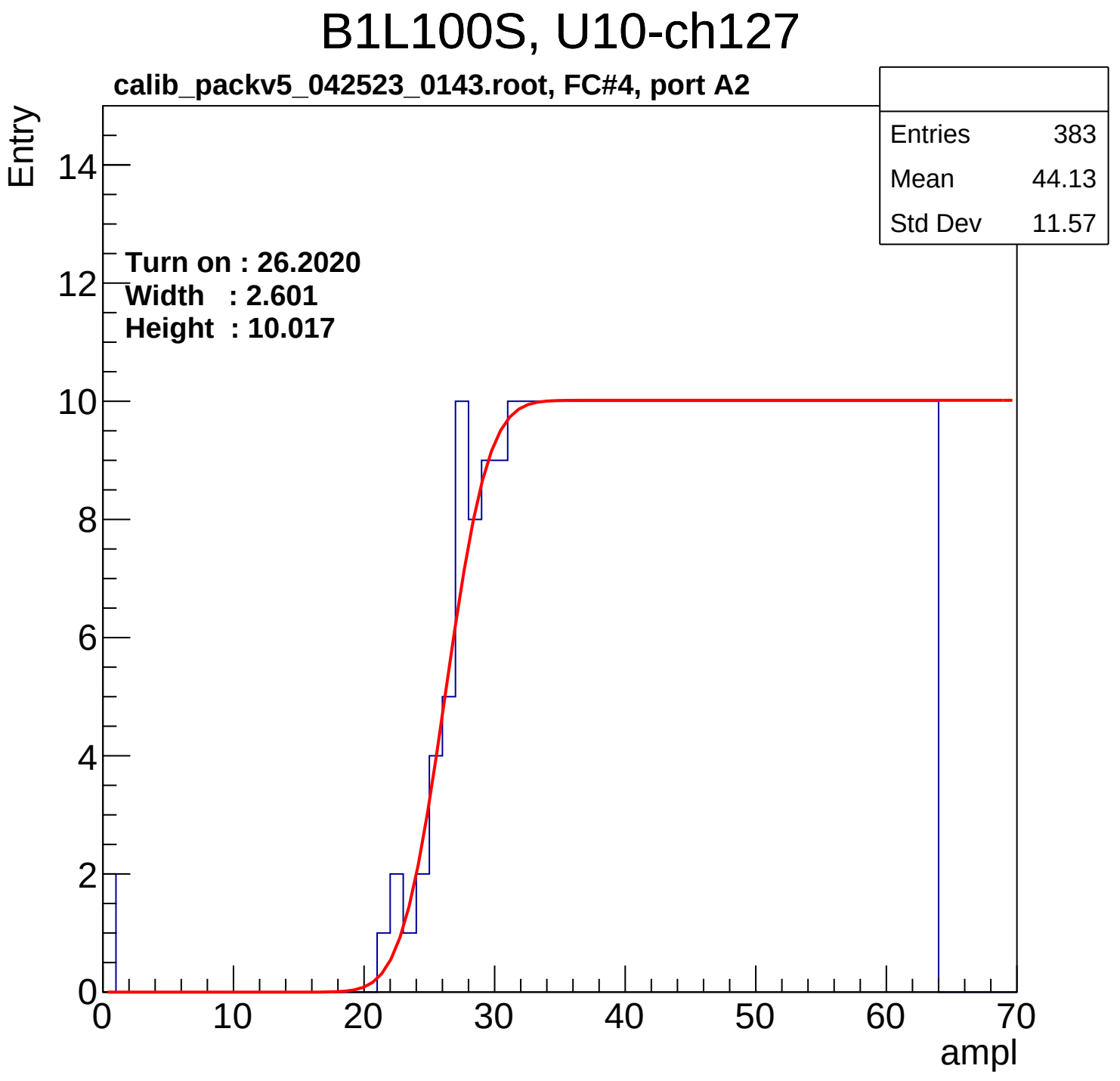
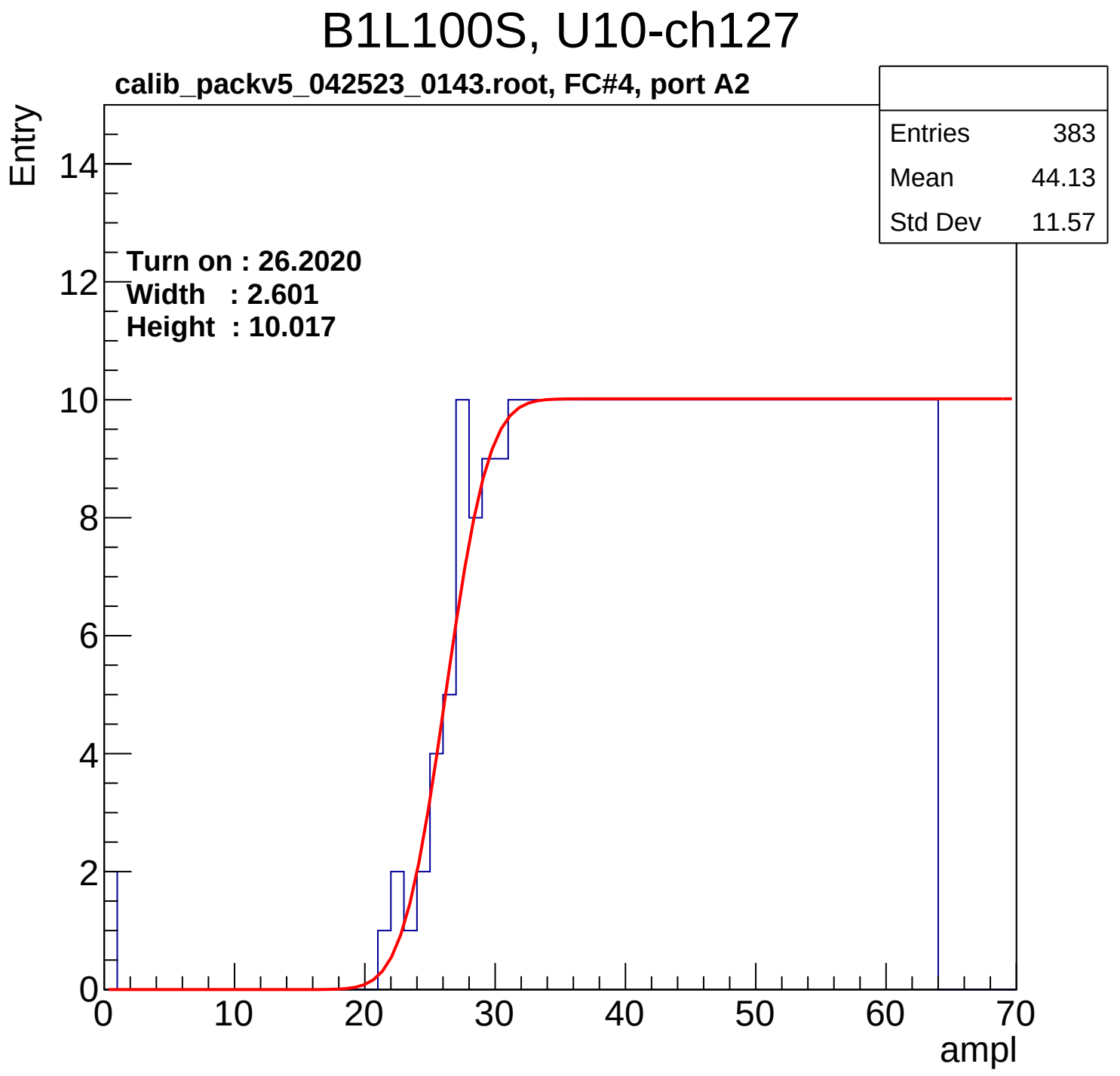

B1L100S, U10-ch127
calib_packv5_042523_0143.root, FC#4, port A2
Entries 383
Mean 44.13
Std Dev 11.57
Turn on : 26.2020
Width : 2.601
Height : 10.017
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L100S, U10-ch127
calib_packv5_042523_0143.root, FC#4, port A2
Entries 383
Mean 44.13
Std Dev 11.57
Turn on : 26.2020
Width : 2.601
Height : 10.017
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70