



# B1L102S, U5-ch0, adc0

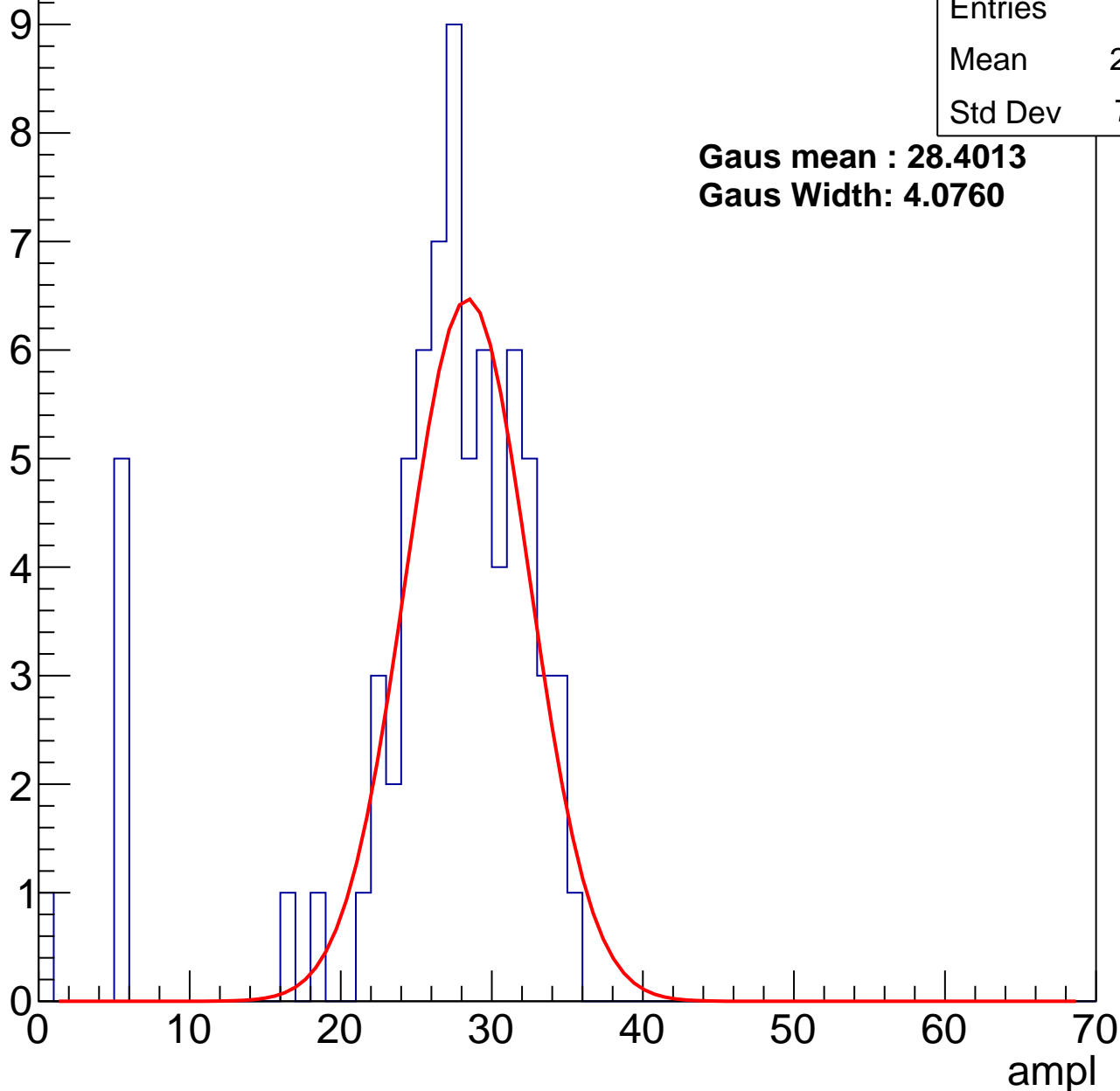
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	25.72
Std Dev	7.401

**Gaus mean : 28.4013**

**Gaus Width: 4.0760**



# B1L102S, U5-ch0, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	72
Mean	34.26
Std Dev	5.132

**Gaus mean : 34.3876**

**Gaus Width: 4.7129**

Entry

10  
8  
6  
4  
2  
0

ampl

0

10

20

30

40

50

60

70

# B1L102S, U5-ch0, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	76
Mean	41.05
Std Dev	6.852

**Gaus mean : 42.0588**

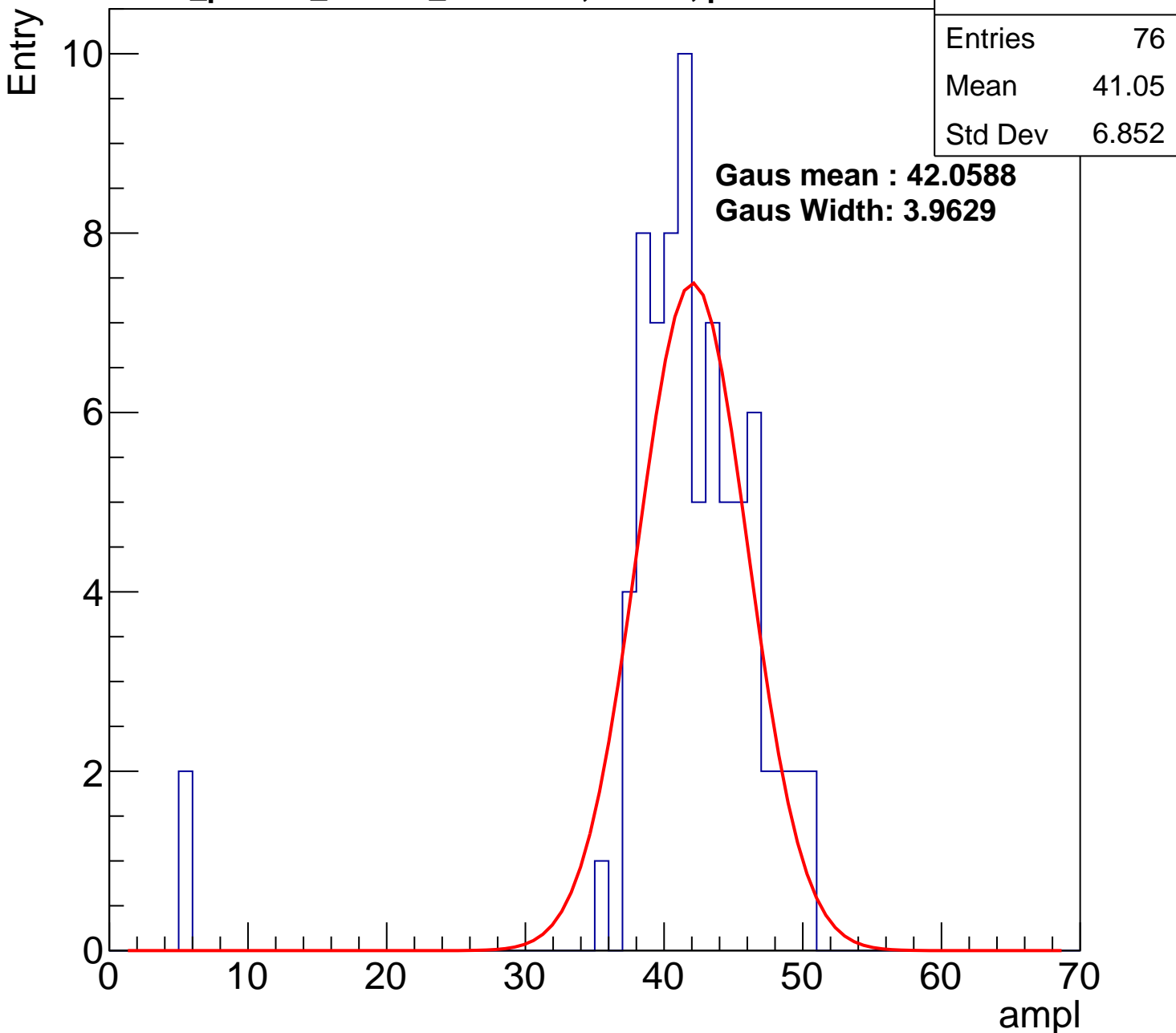
**Gaus Width: 3.9629**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

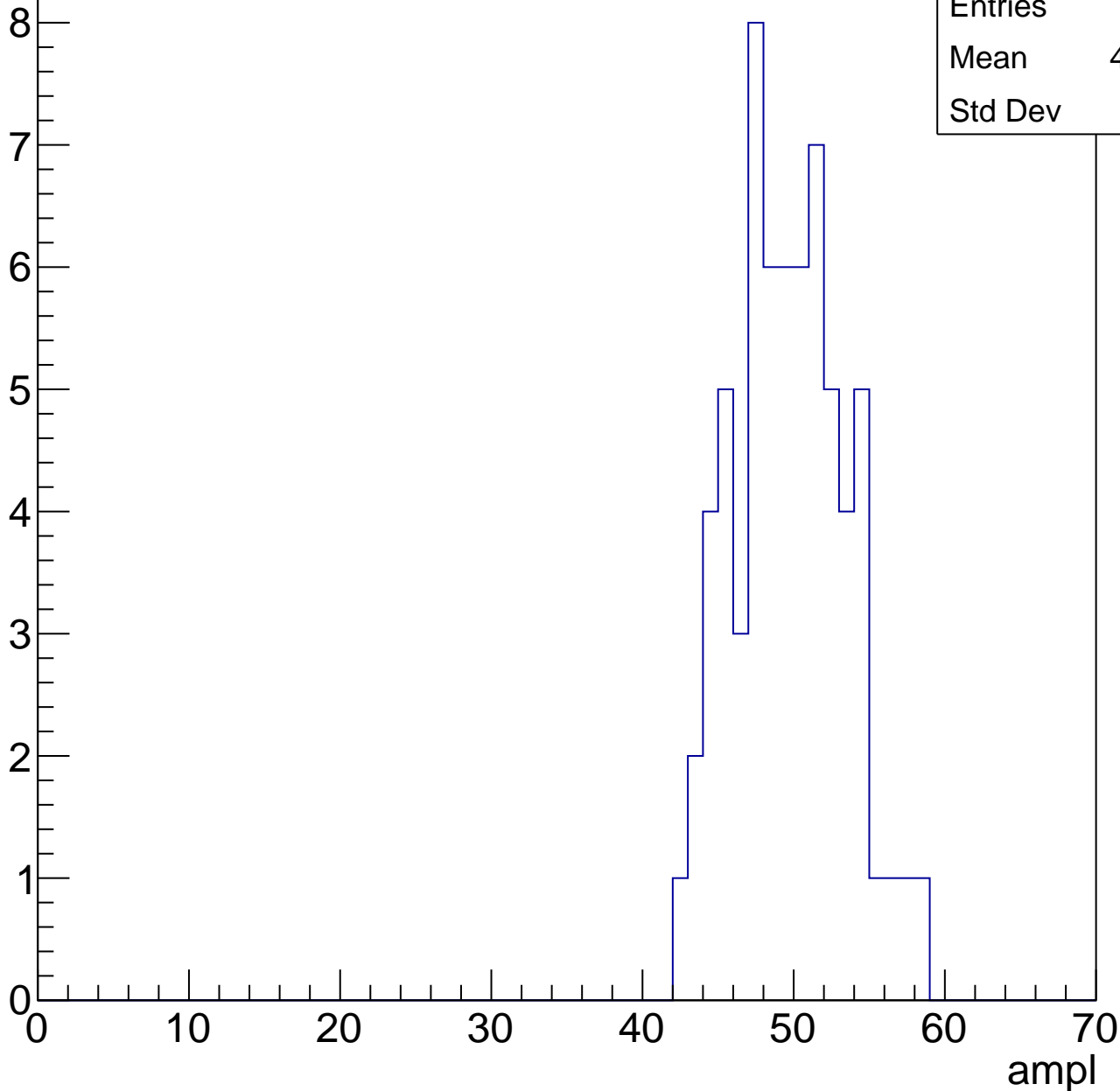


# B1L102S, U5-ch0, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	49.24
Std Dev	3.61

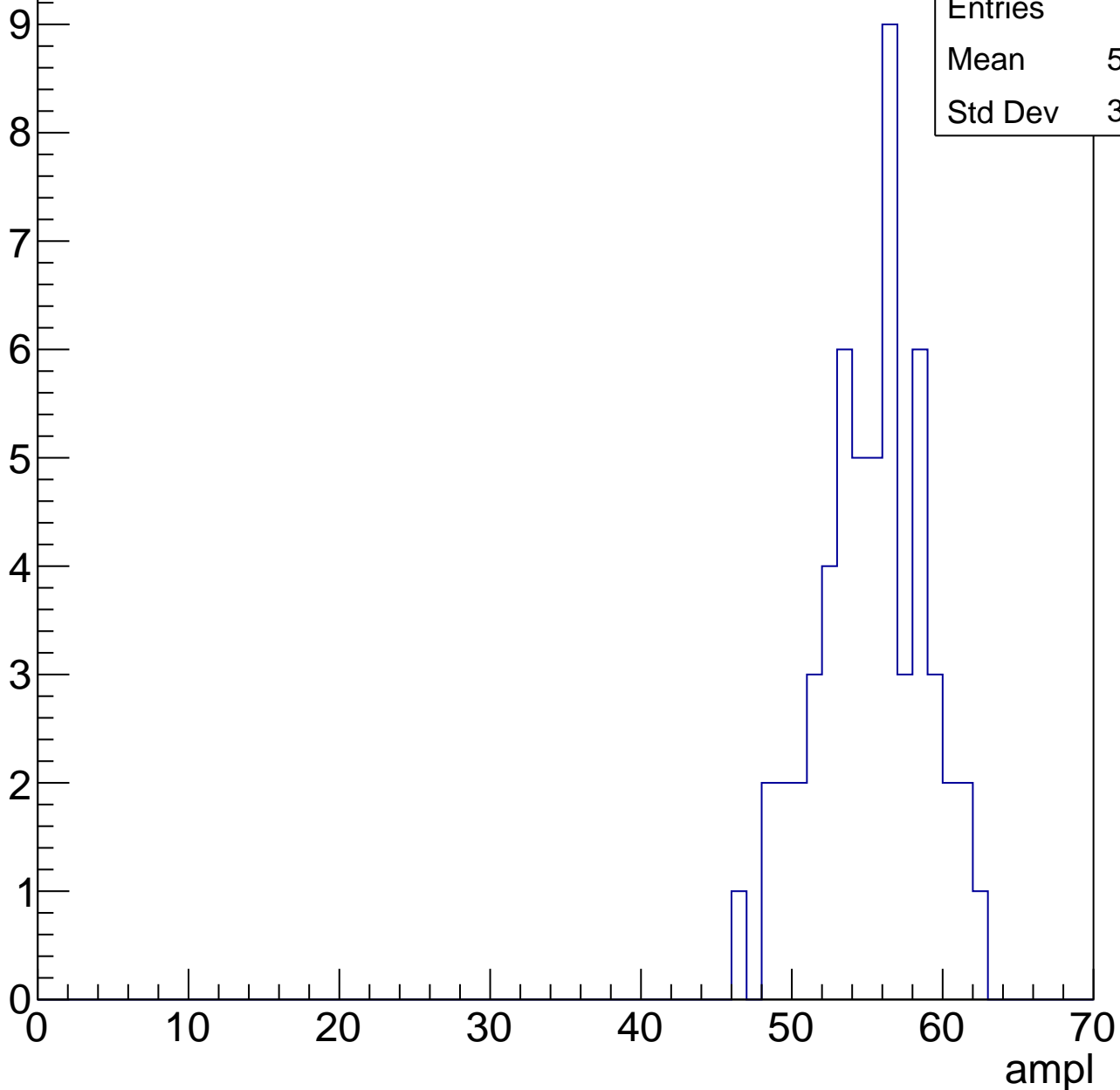


# B1L102S, U5-ch0, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	54.79
Std Dev	3.549

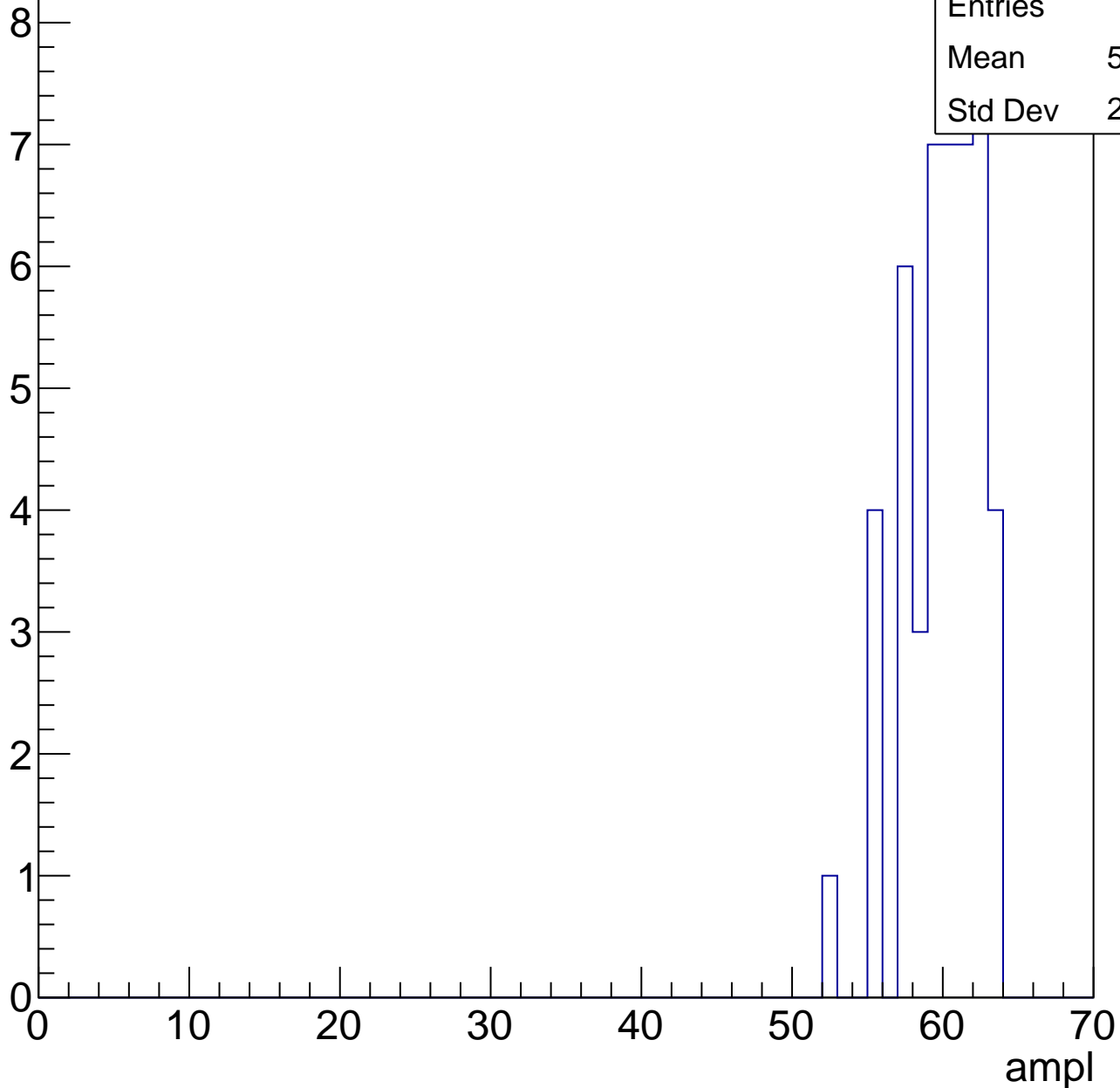


# B1L102S, U5-ch0, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	47
Mean	59.49
Std Dev	2.525

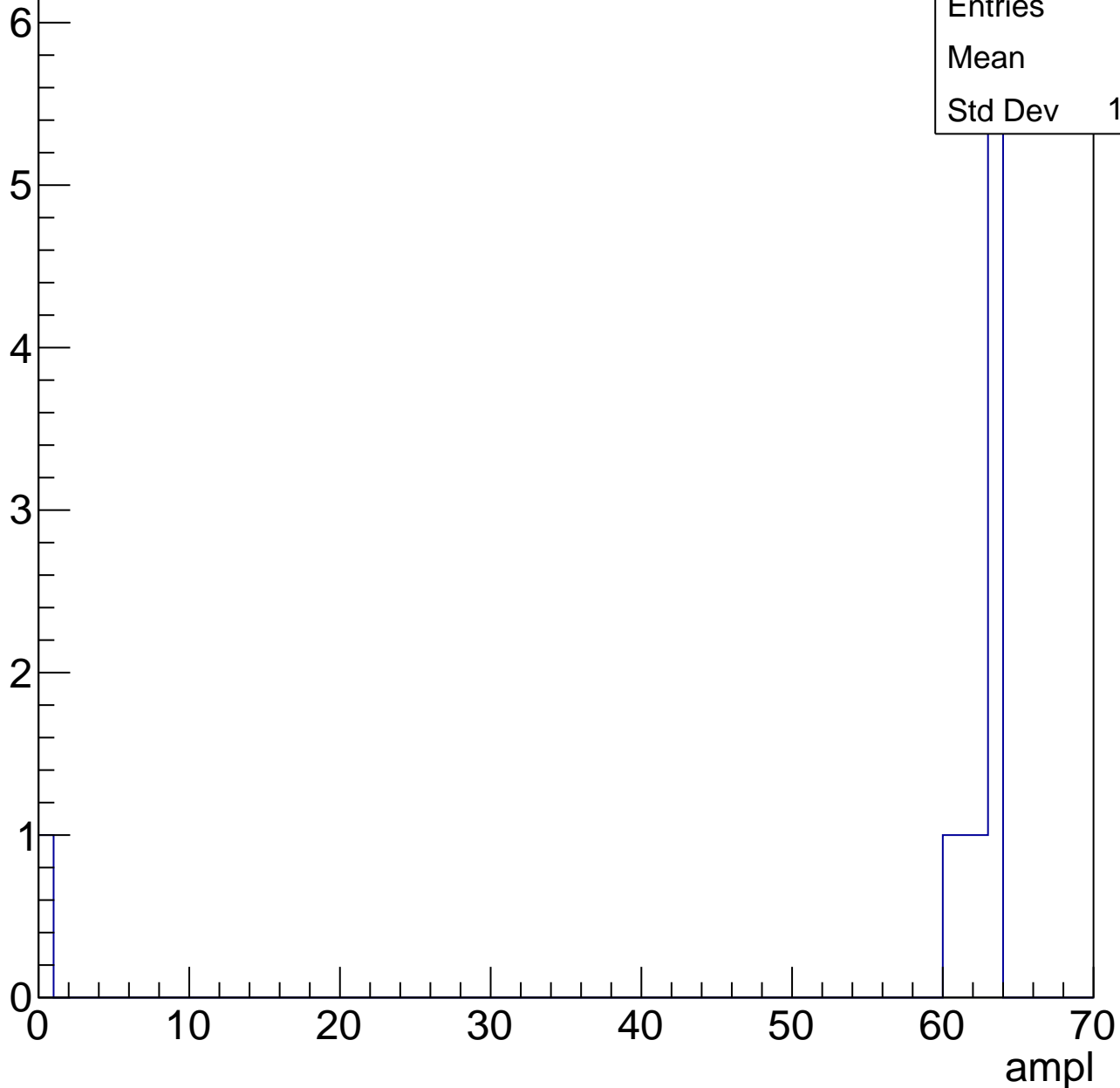


# B1L102S, U5-ch0, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	10
Mean	56.1
Std Dev	18.73





# B1L102S, U5-ch0, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U5-ch1, adc0

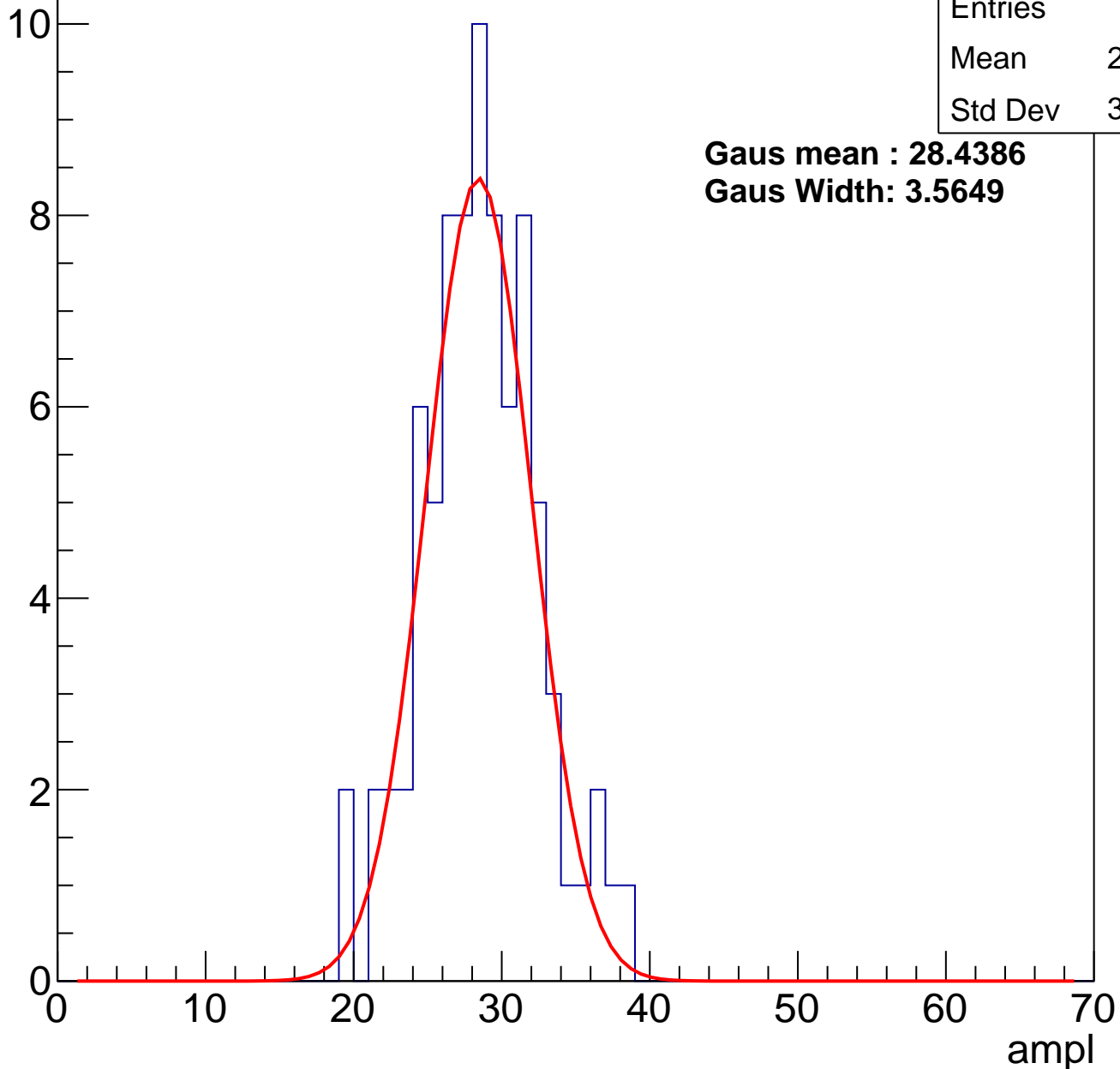
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	81
Mean	28.12
Std Dev	3.873

**Gaus mean : 28.4386**

**Gaus Width: 3.5649**

Entry



# B1L102S, U5-ch1, adc1

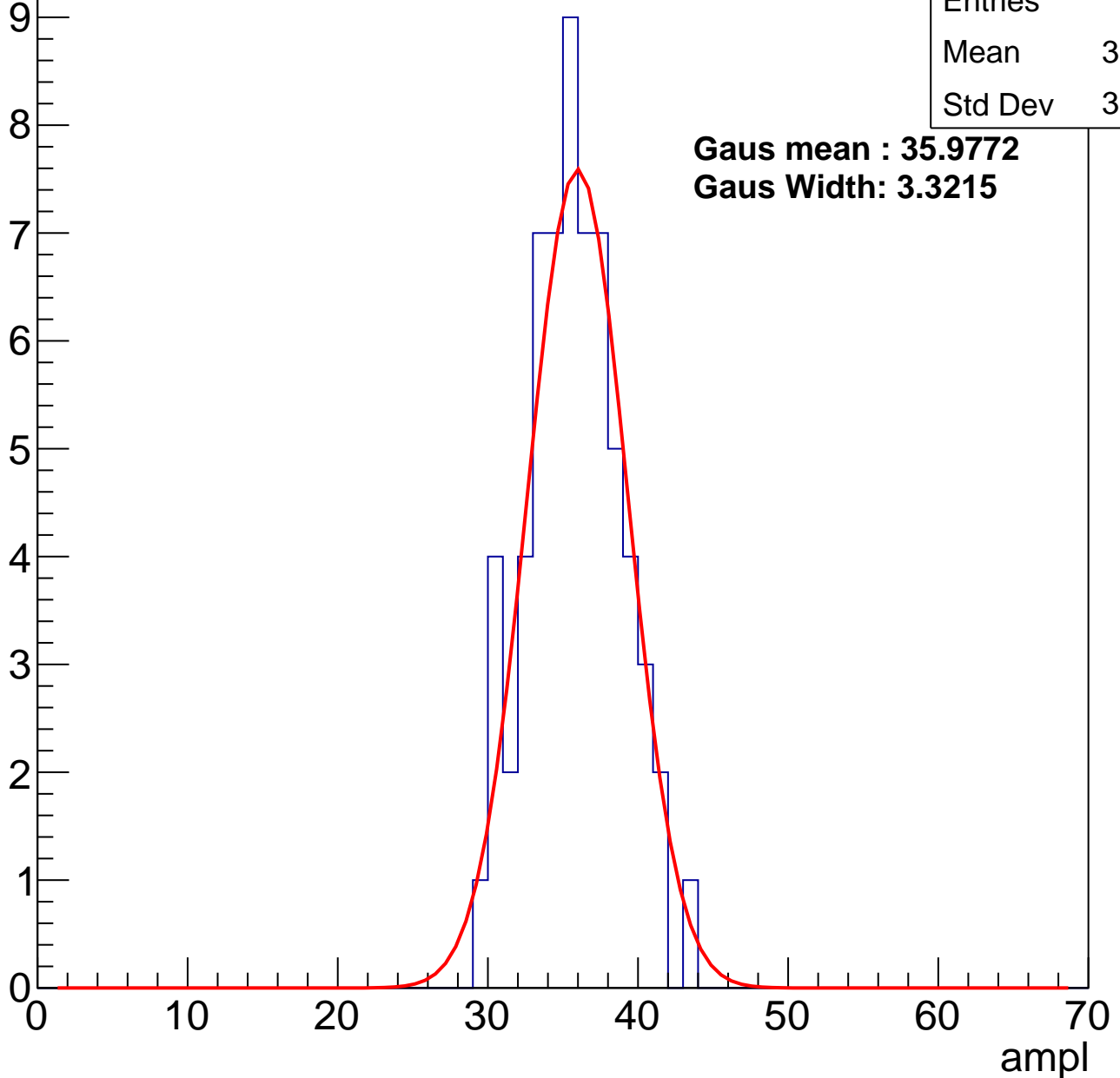
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	35.32
Std Dev	3.054

**Gaus mean : 35.9772**

**Gaus Width: 3.3215**



# B1L102S, U5-ch1, adc2

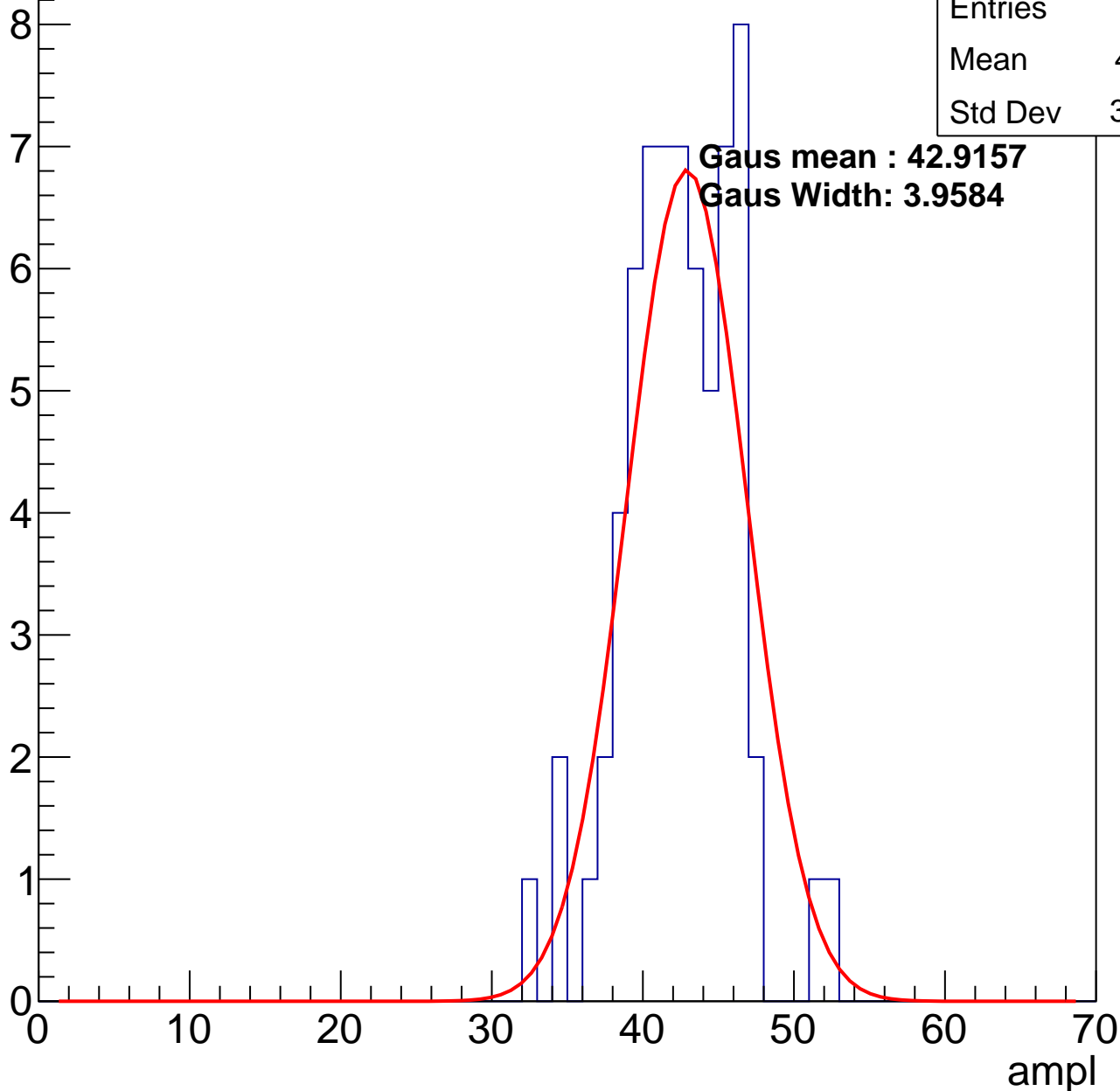
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	42.01
Std Dev	3.695

**Gaus mean : 42.9157**

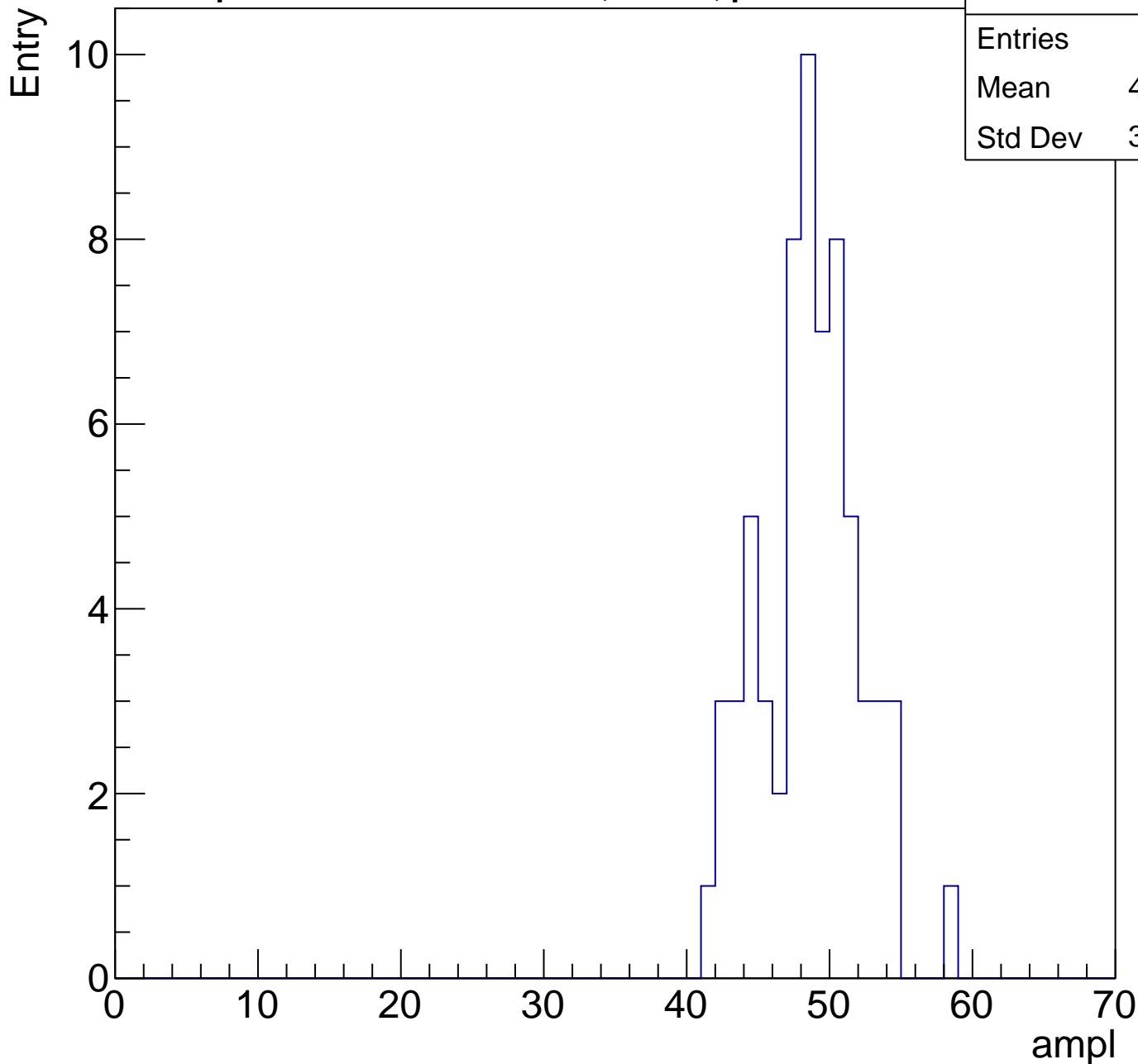
**Gaus Width: 3.9584**



# B1L102S, U5-ch1, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	65
Mean	48.18
Std Dev	3.437



# B1L102S, U5-ch1, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	69
Mean	55.13
Std Dev	3.153

Entry

10

8

6

4

2

0

0

10

20

30

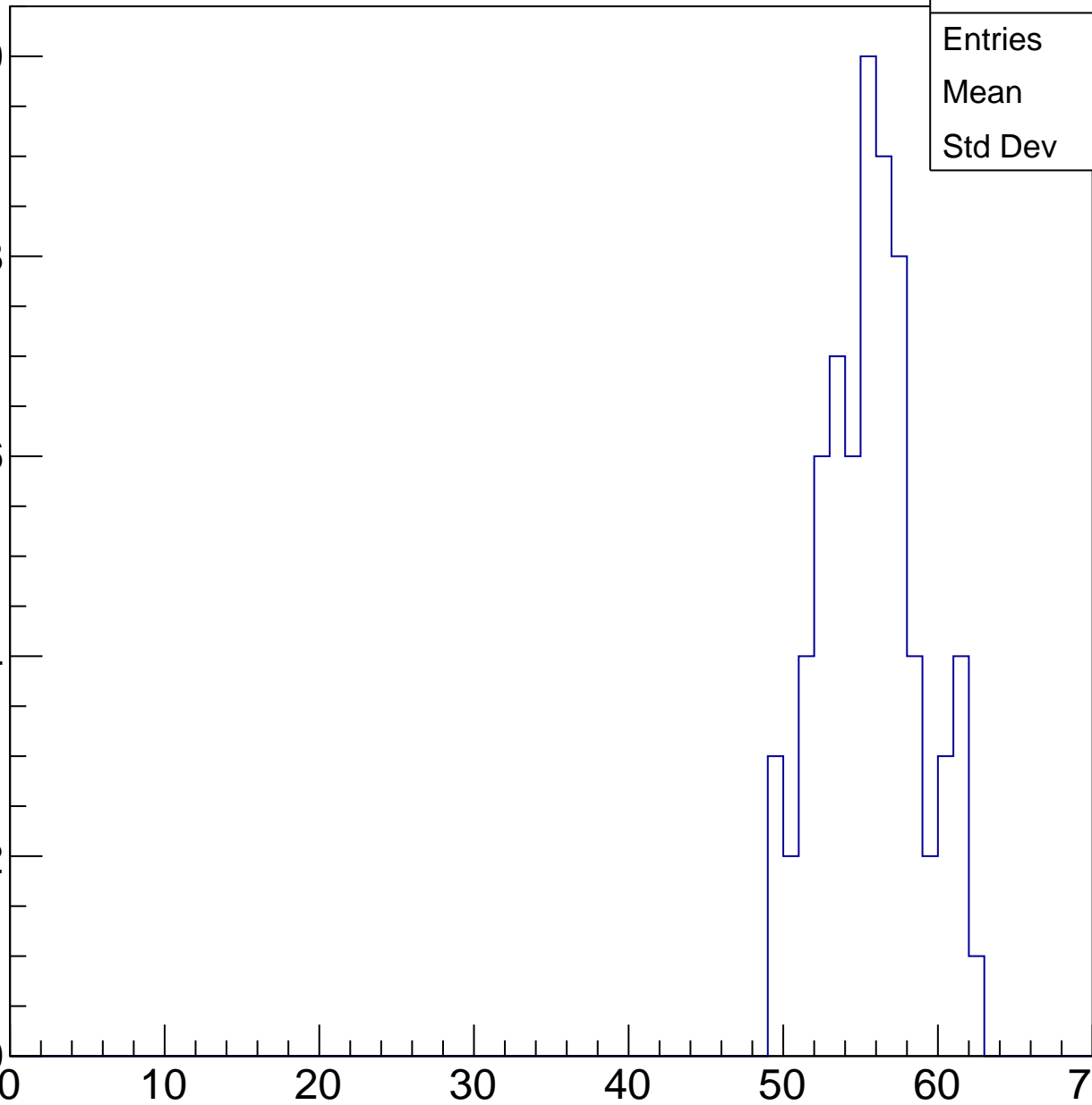
40

50

60

ampl

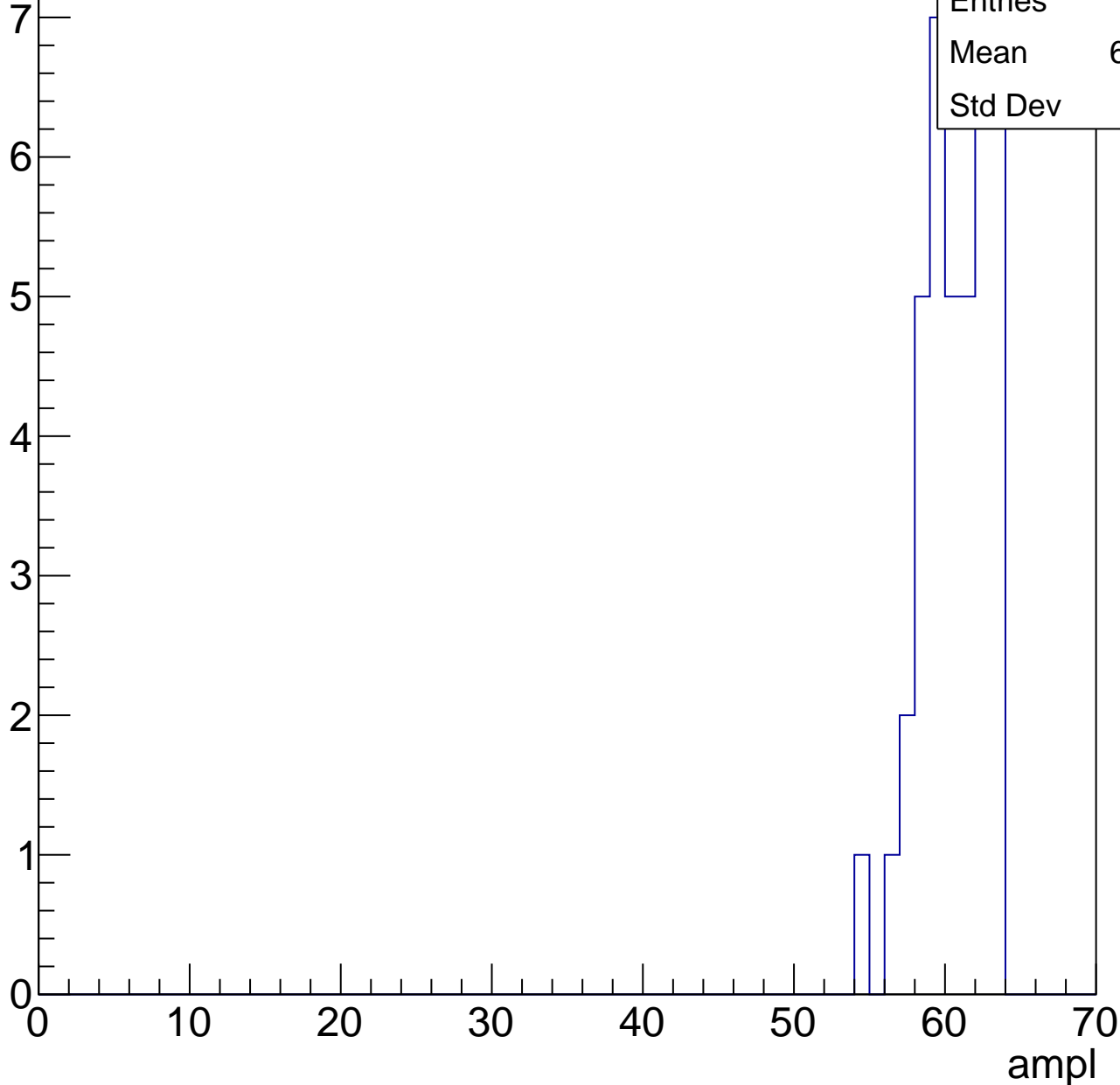
70



# B1L102S, U5-ch1, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

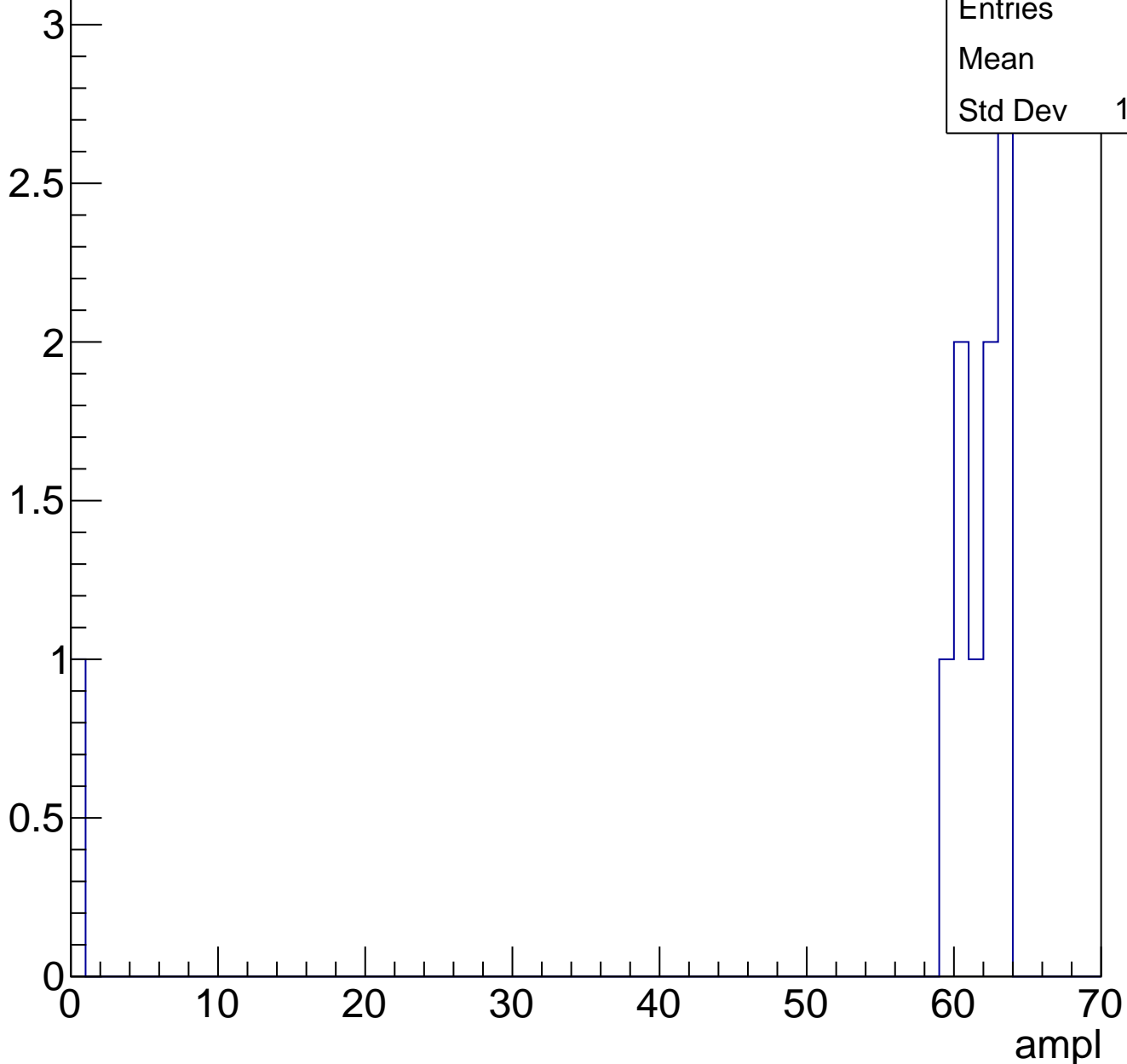
Entry



# B1L102S, U5-ch1, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U5-ch1, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U5-ch2, adc0

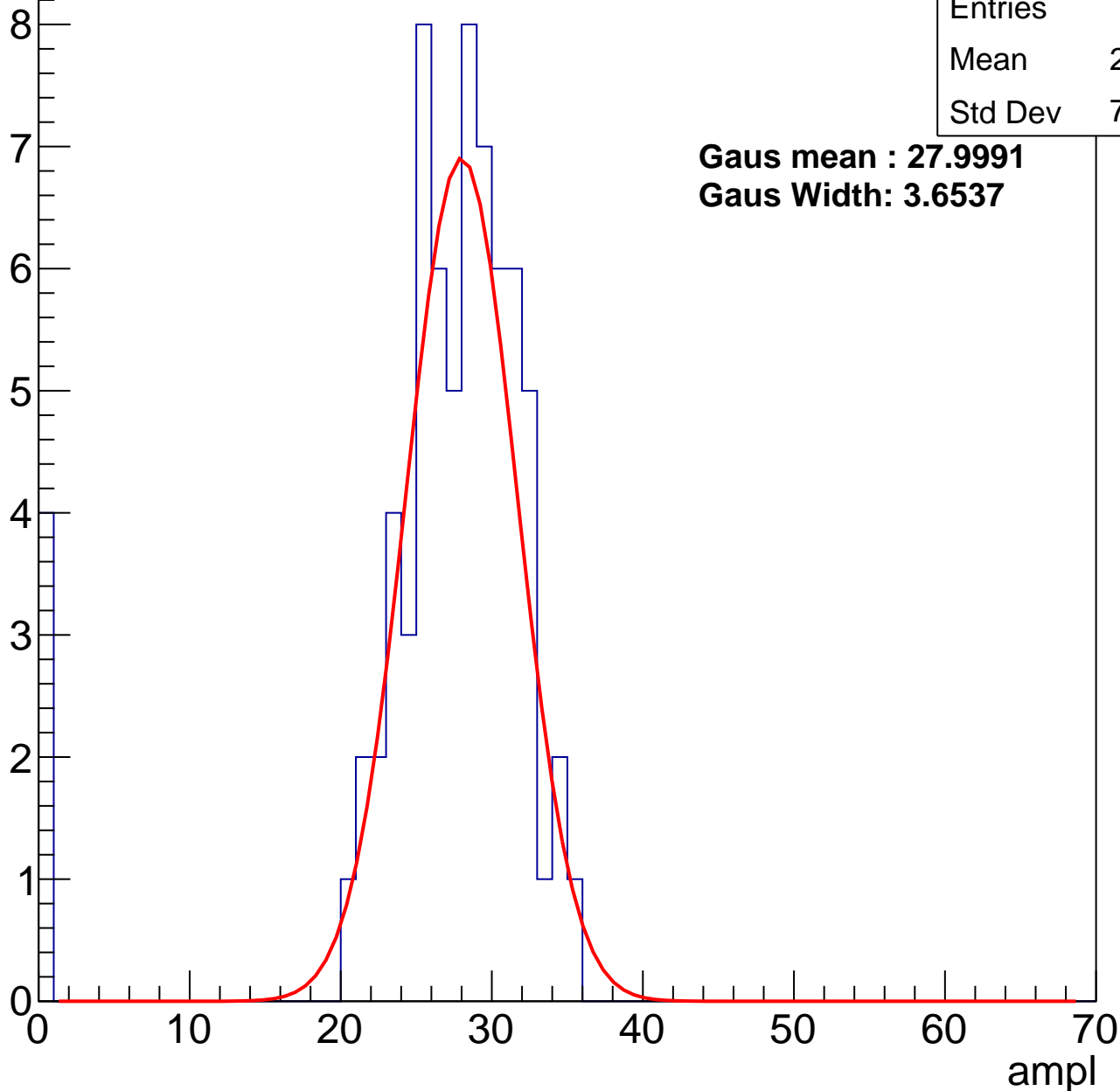
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	26.06
Std Dev	7.182

**Gaus mean : 27.9991**

**Gaus Width: 3.6537**



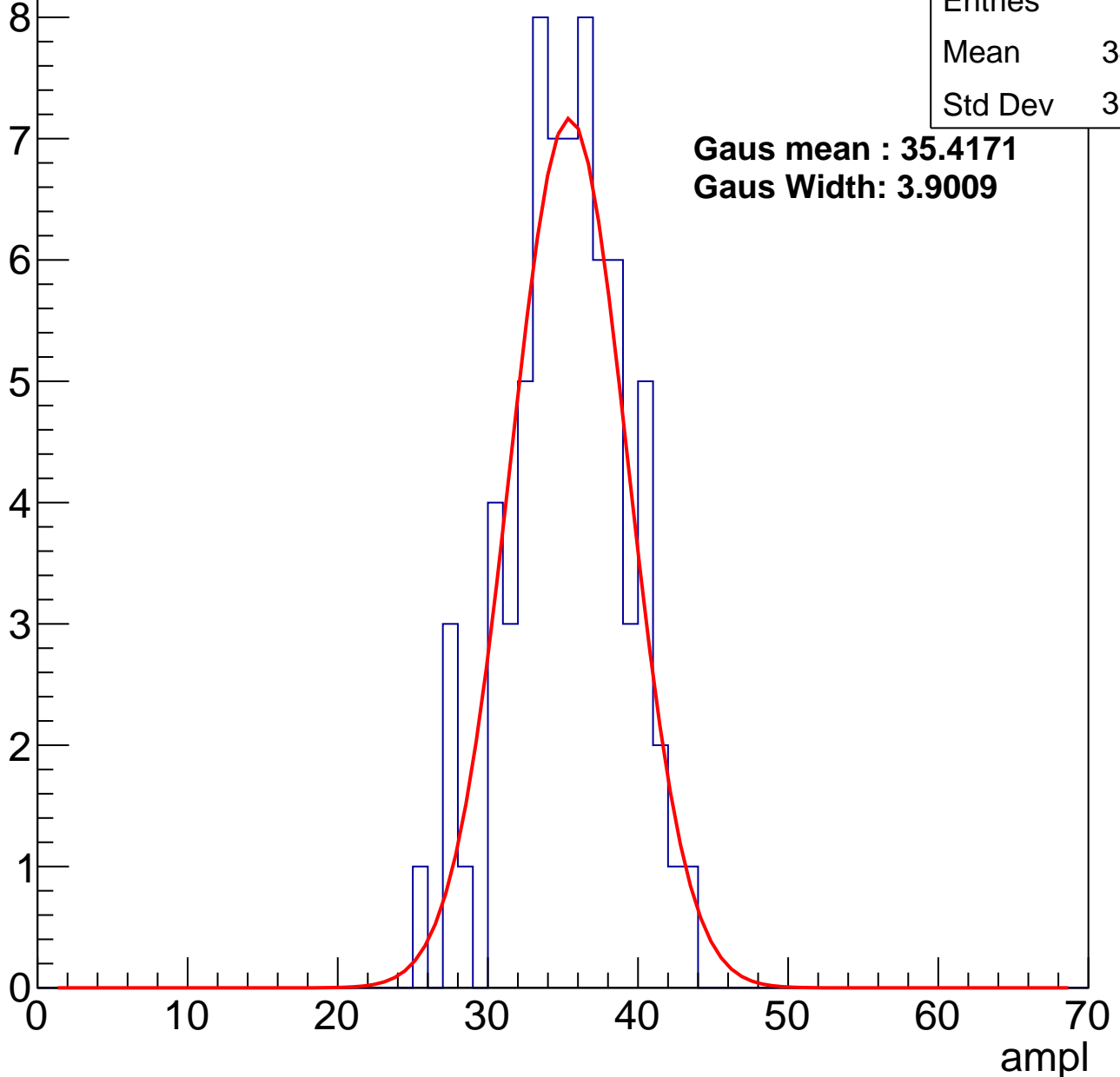
# B1L102S, U5-ch2, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	34.87
Std Dev	3.783

**Gaus mean : 35.4171**  
**Gaus Width: 3.9009**



# B1L102S, U5-ch2, adc2

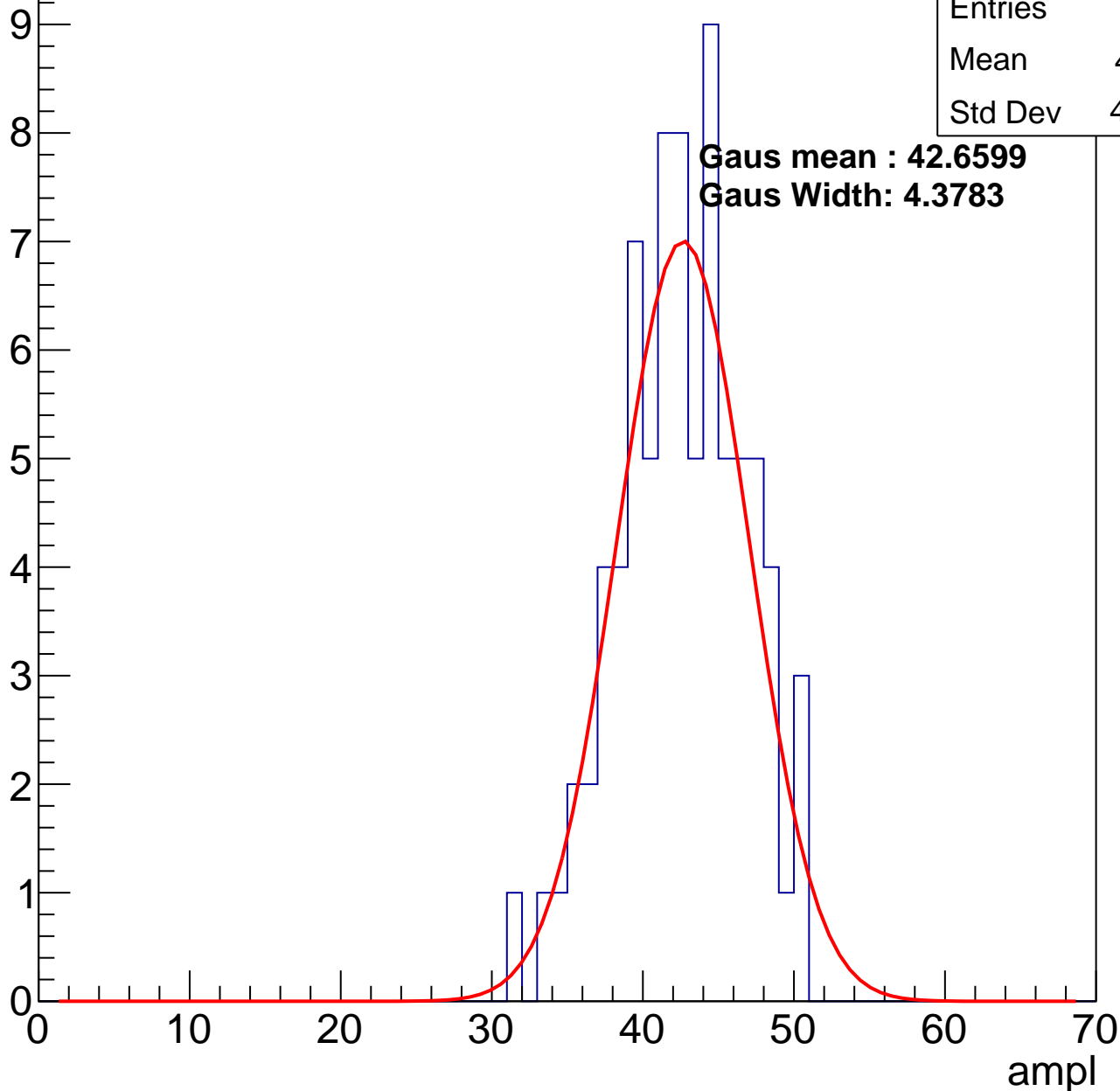
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	80
Mean	42.11
Std Dev	4.132

**Gaus mean : 42.6599**

**Gaus Width: 4.3783**

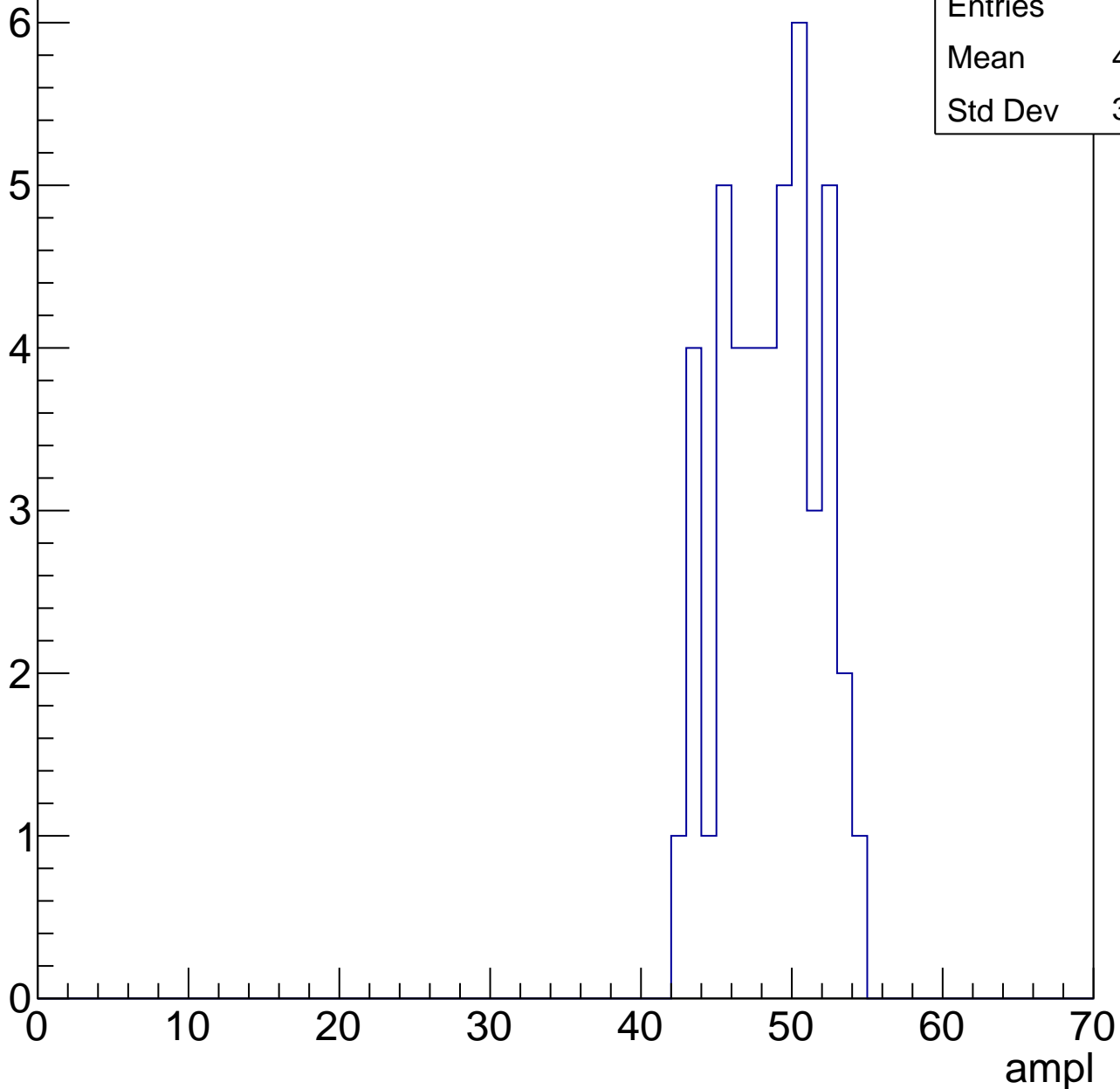


# B1L102S, U5-ch2, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	45
Mean	48.11
Std Dev	3.121

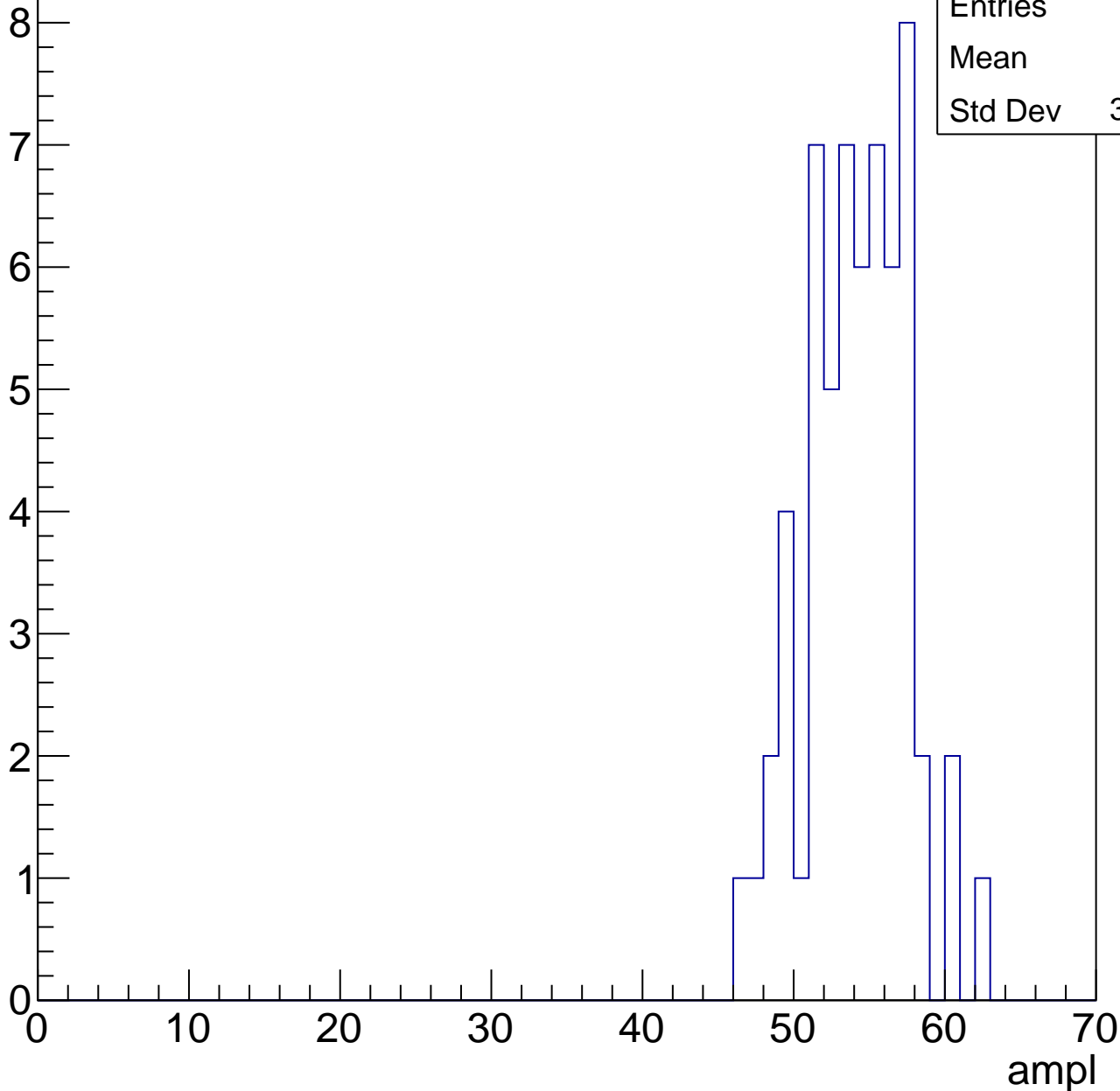


# B1L102S, U5-ch2, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

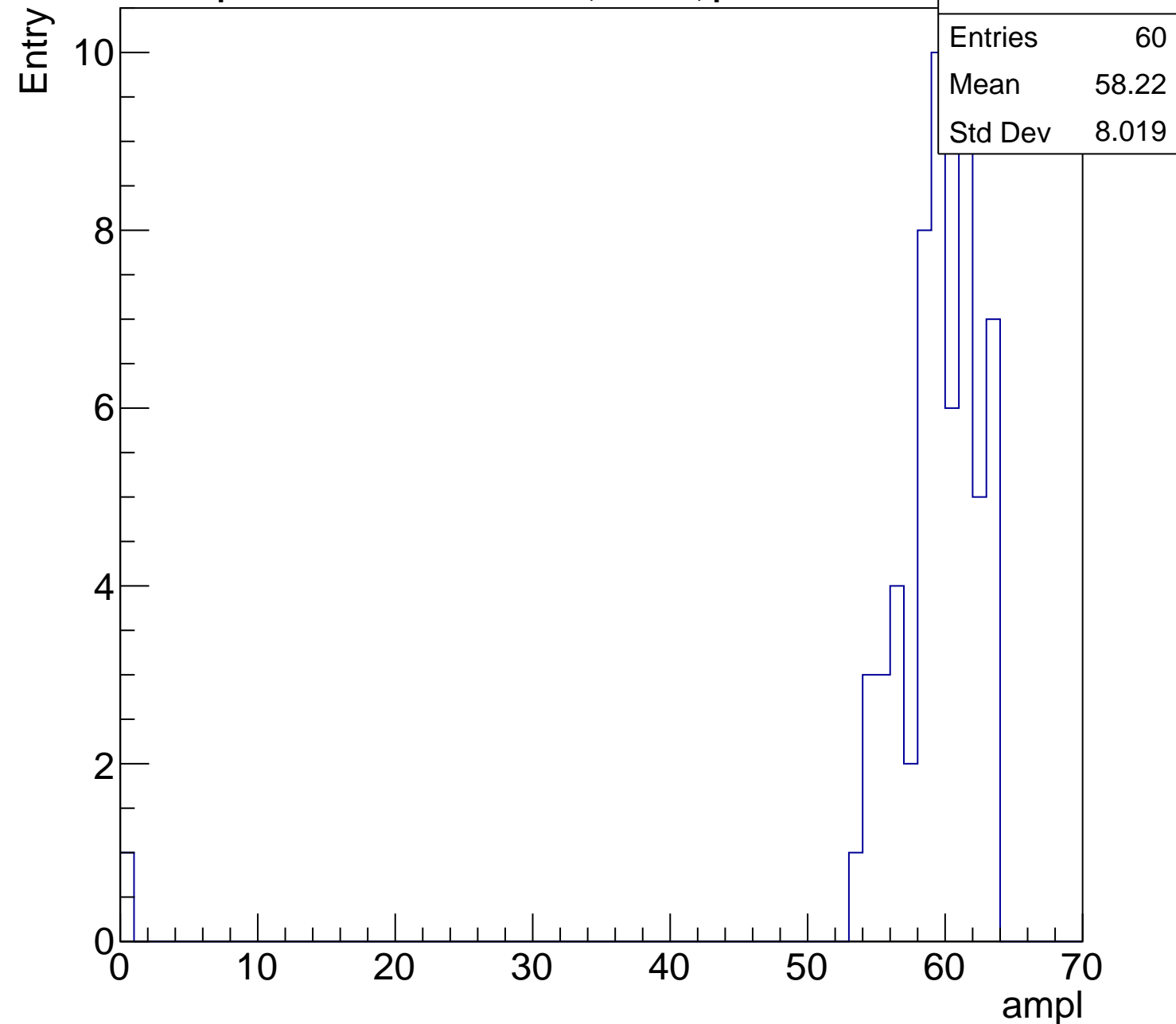
Entries	60
Mean	53.7
Std Dev	3.308



# B1L102S, U5-ch2, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

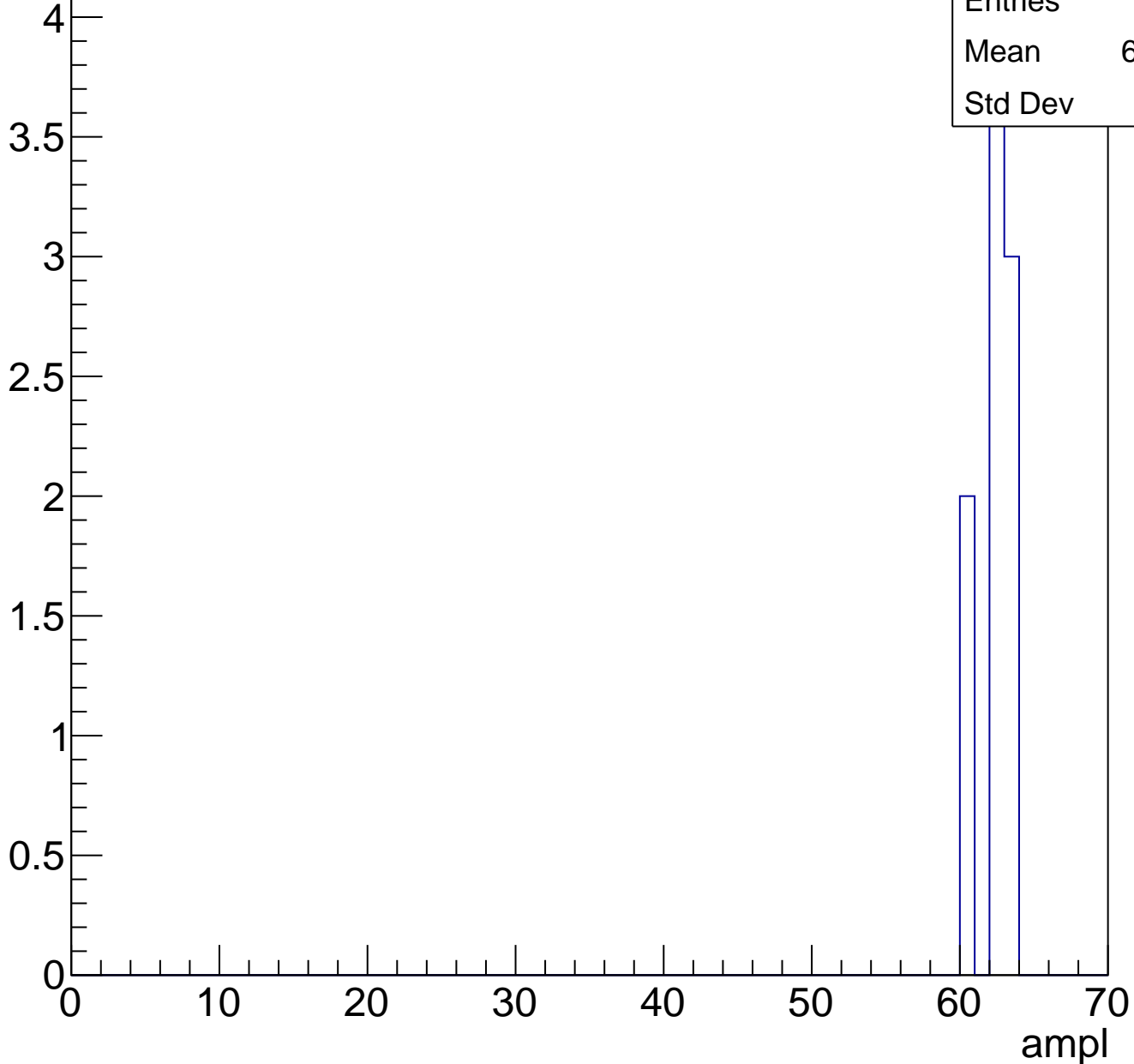
Entries	60
Mean	58.22
Std Dev	8.019



# B1L102S, U5-ch2, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U5-ch2, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U5-ch3, adc0

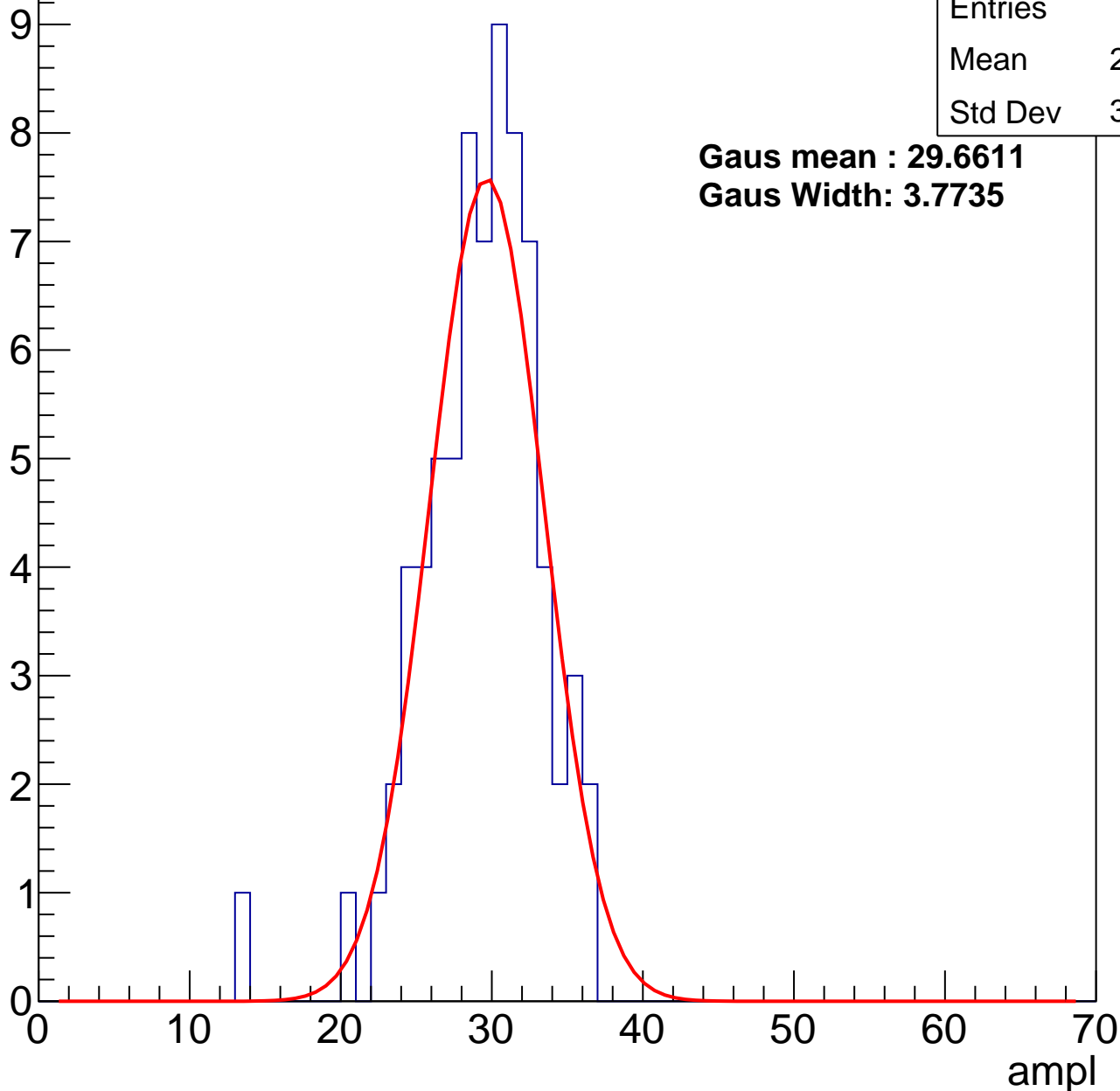
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	28.88
Std Dev	3.913

**Gaus mean : 29.6611**

**Gaus Width: 3.7735**



# B1L102S, U5-ch3, adc1

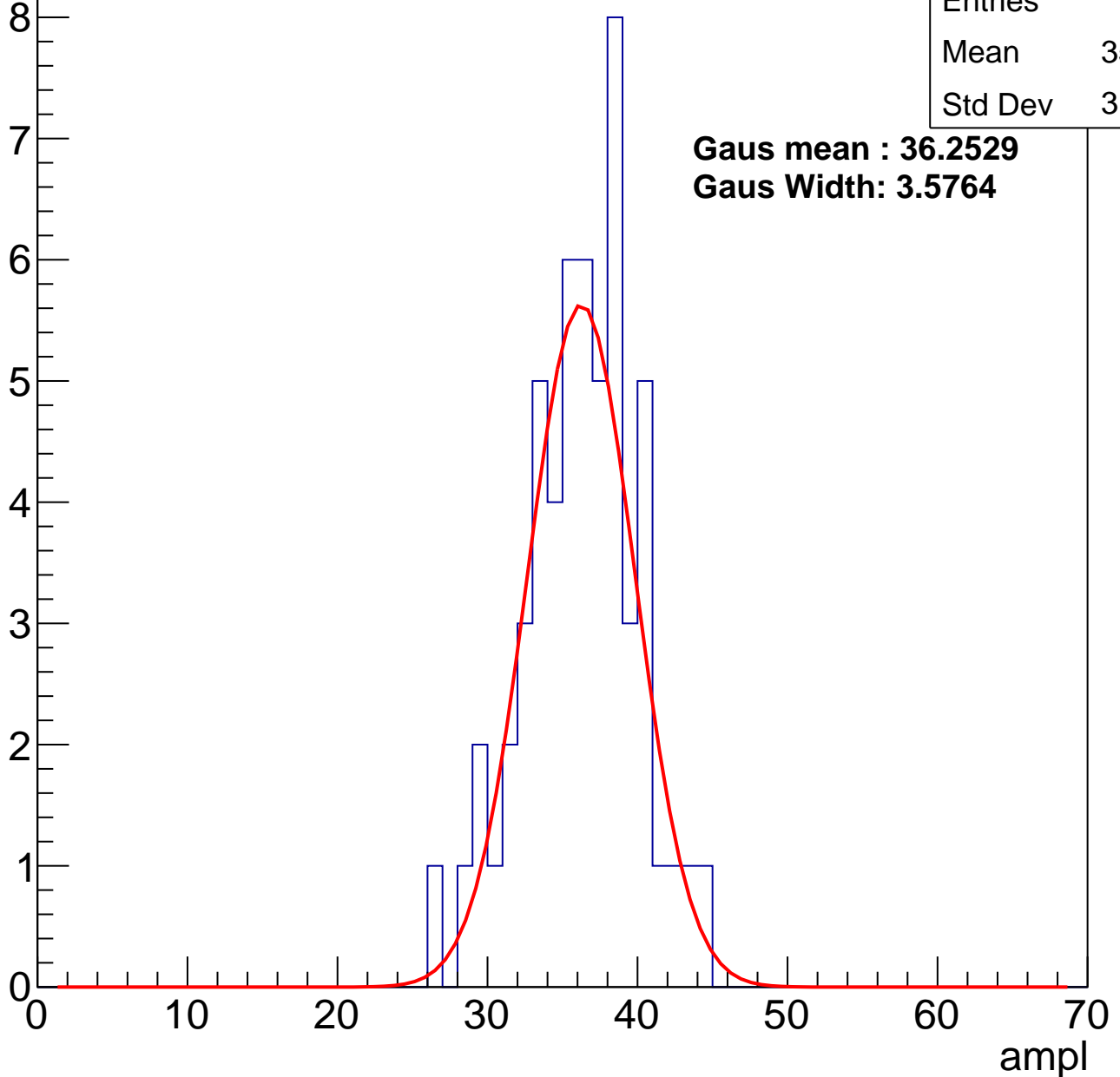
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	35.77
Std Dev	3.727

**Gaus mean : 36.2529**

**Gaus Width: 3.5764**



# B1L102S, U5-ch3, adc2

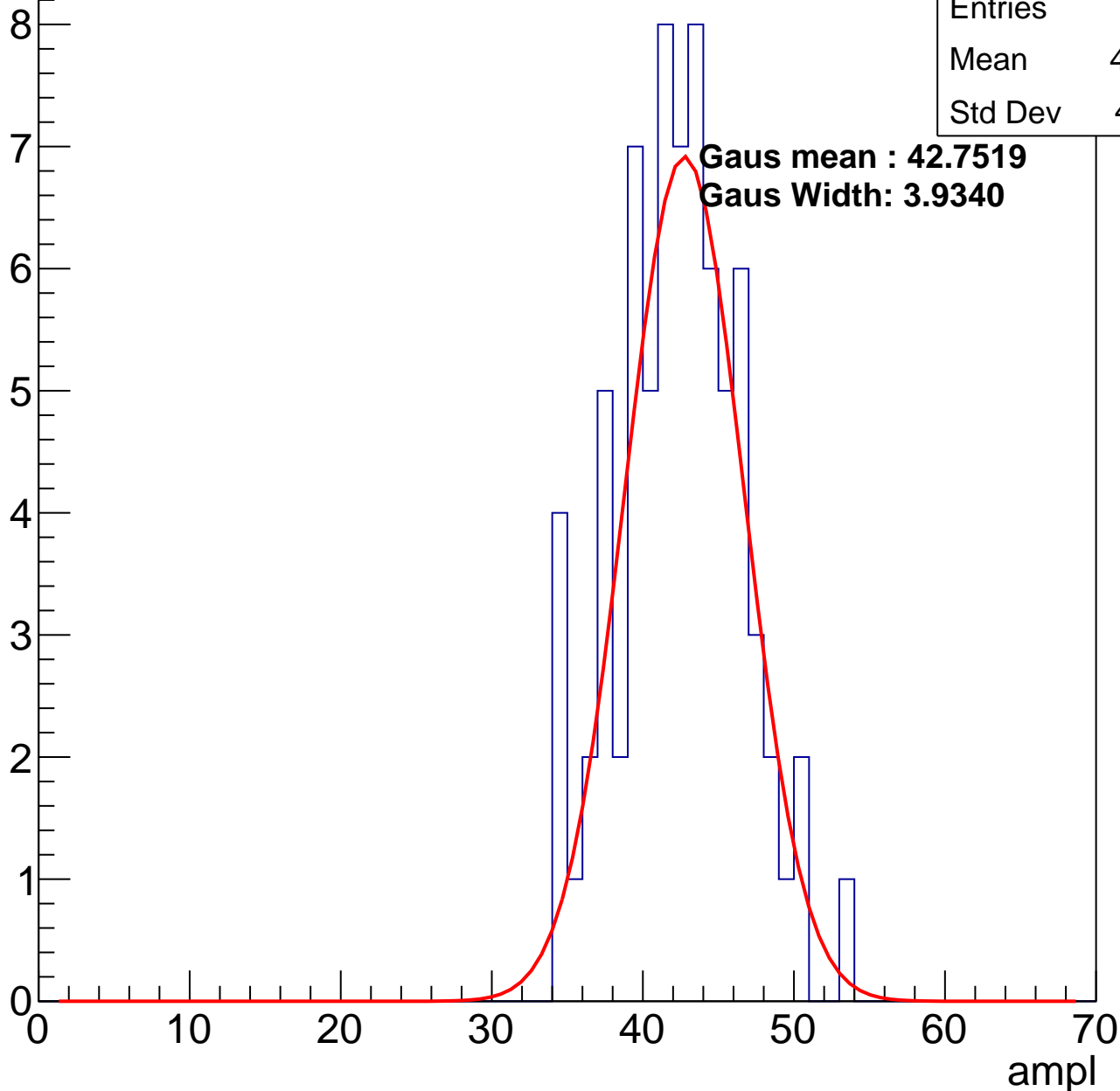
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	41.96
Std Dev	4.071

**Gaus mean : 42.7519**

**Gaus Width: 3.9340**

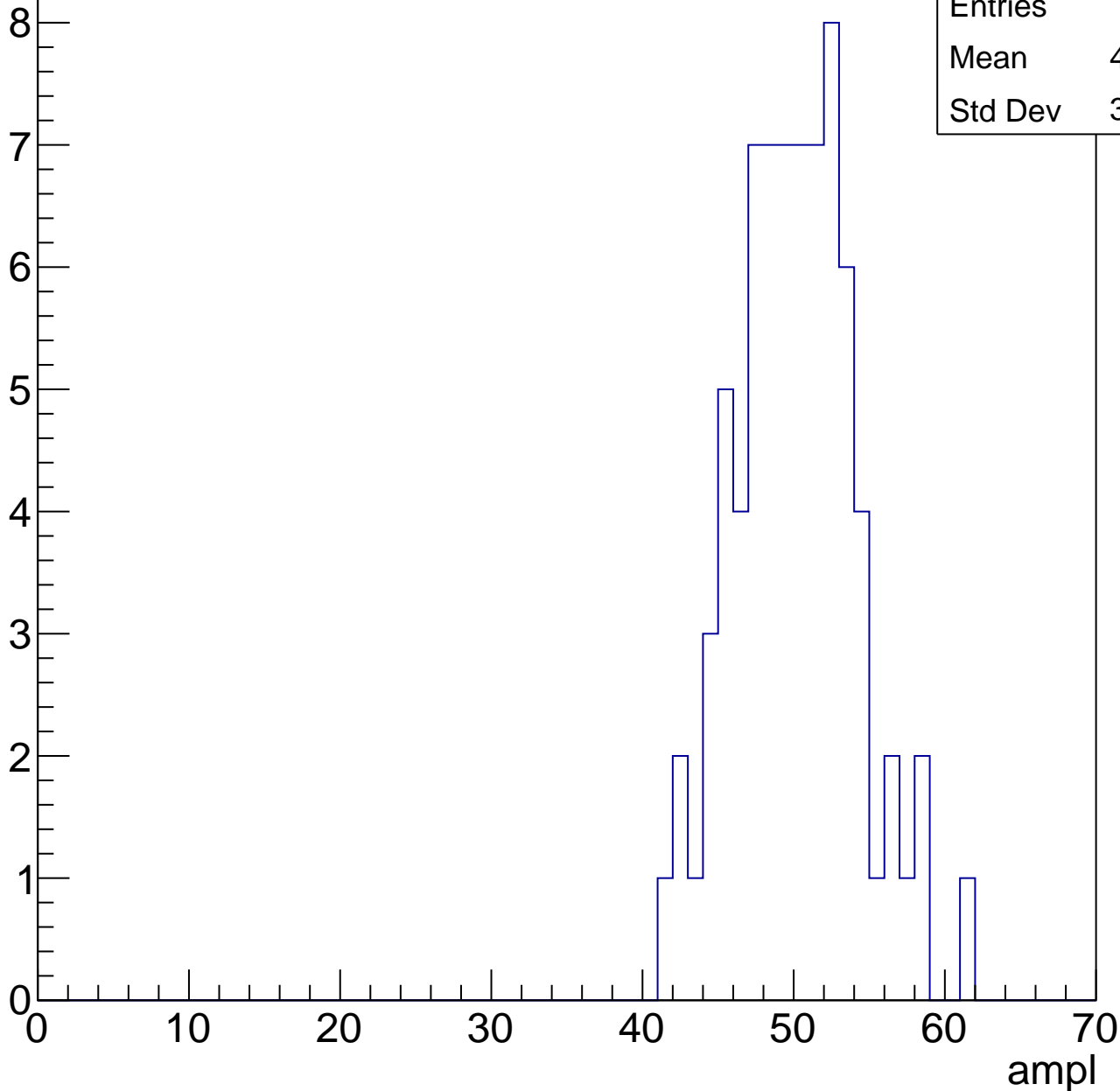


# B1L102S, U5-ch3, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	49.67
Std Dev	3.968

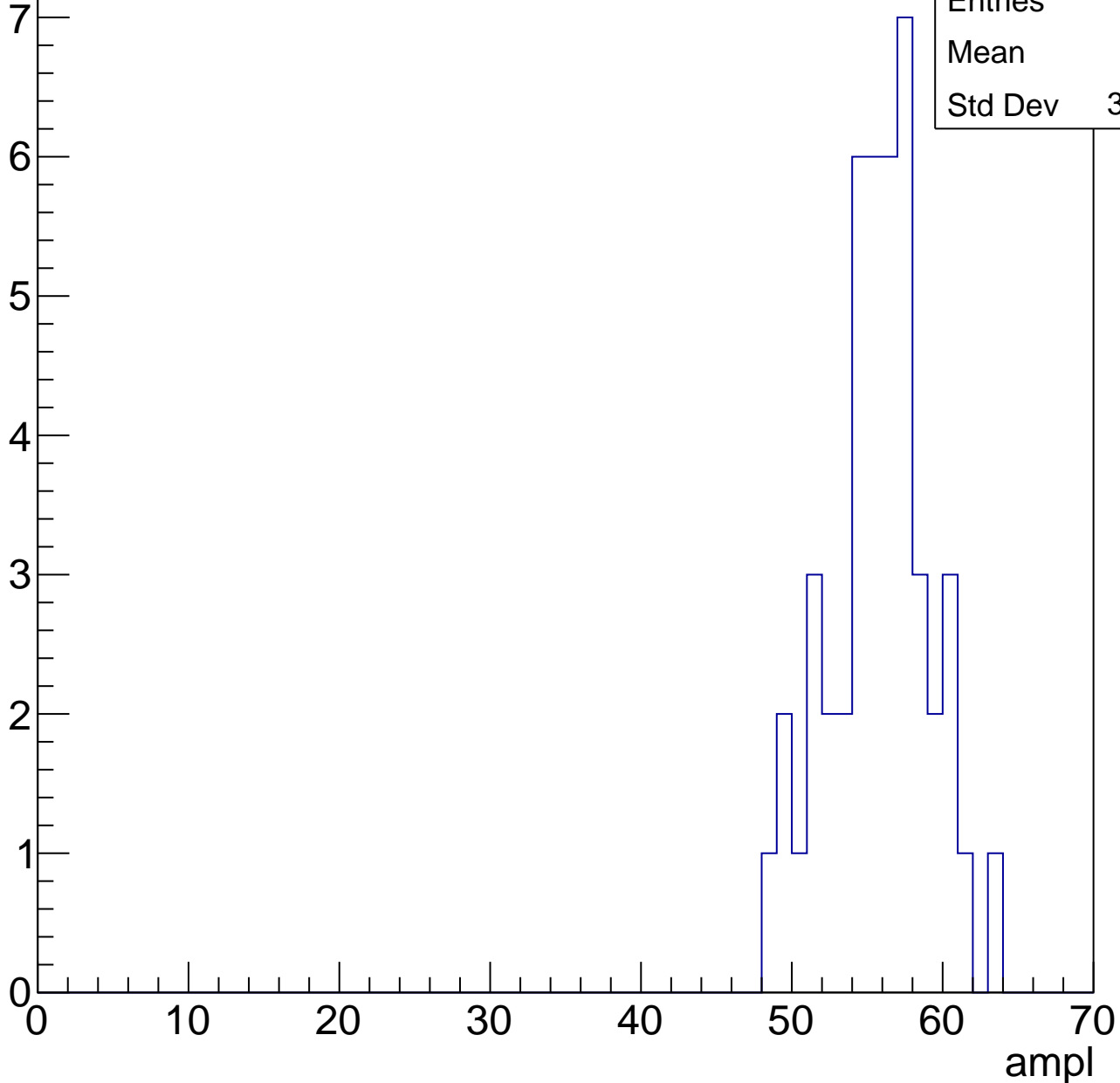


# B1L102S, U5-ch3, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	46
Mean	55.3
Std Dev	3.263

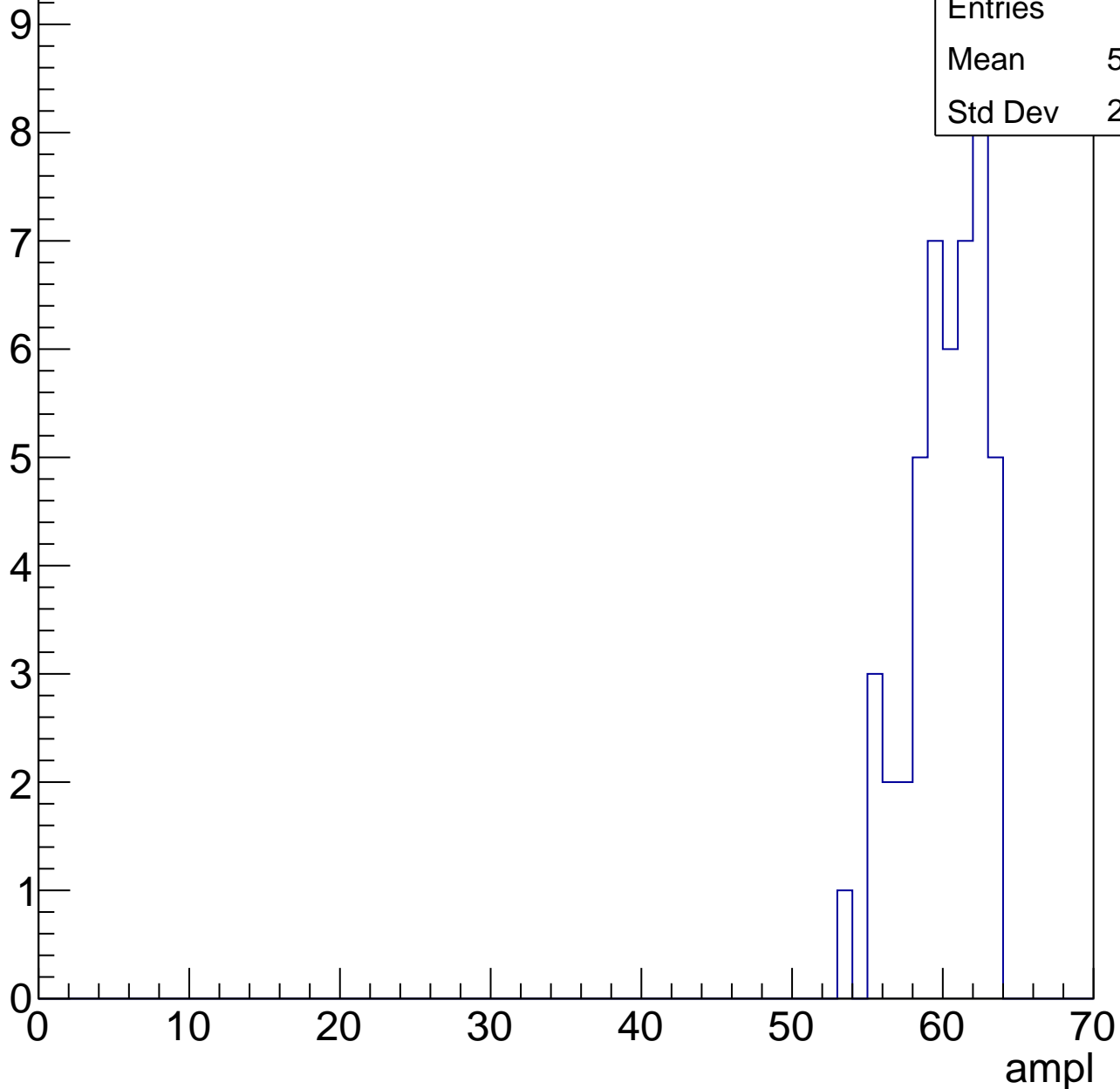


# B1L102S, U5-ch3, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	47
Mean	59.72
Std Dev	2.464



# B1L102S, U5-ch3, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

4  
3.5  
3  
2.5  
2  
1.5  
1  
0.5  
0

Entries	9
Mean	54.89
Std Dev	19.46

ampl



# B1L102S, U5-ch3, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L102S, U5-ch4, adc0

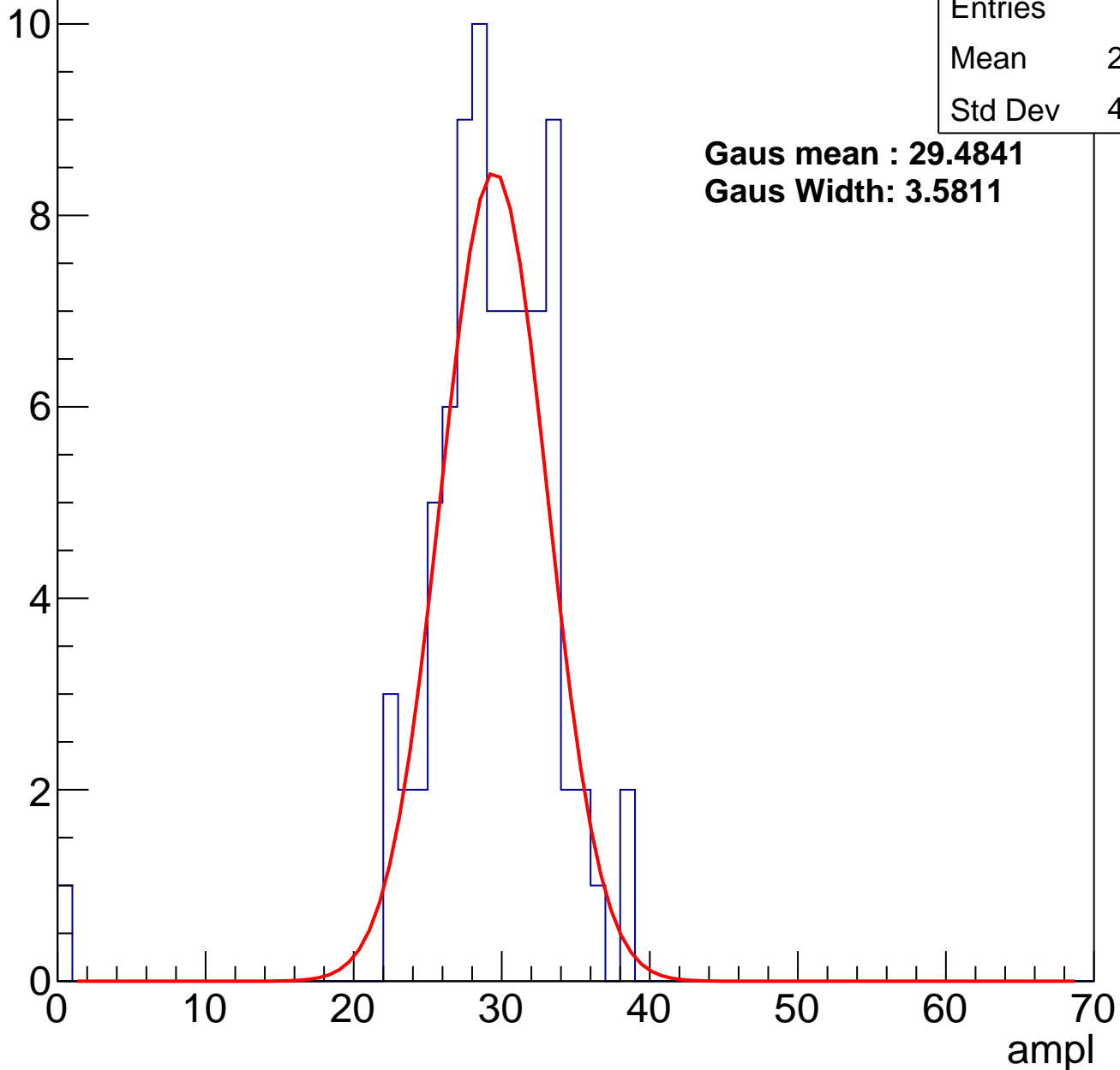
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	82
Mean	28.84
Std Dev	4.766

**Gaus mean : 29.4841**

**Gaus Width: 3.5811**

Entry



# B1L102S, U5-ch4, adc1

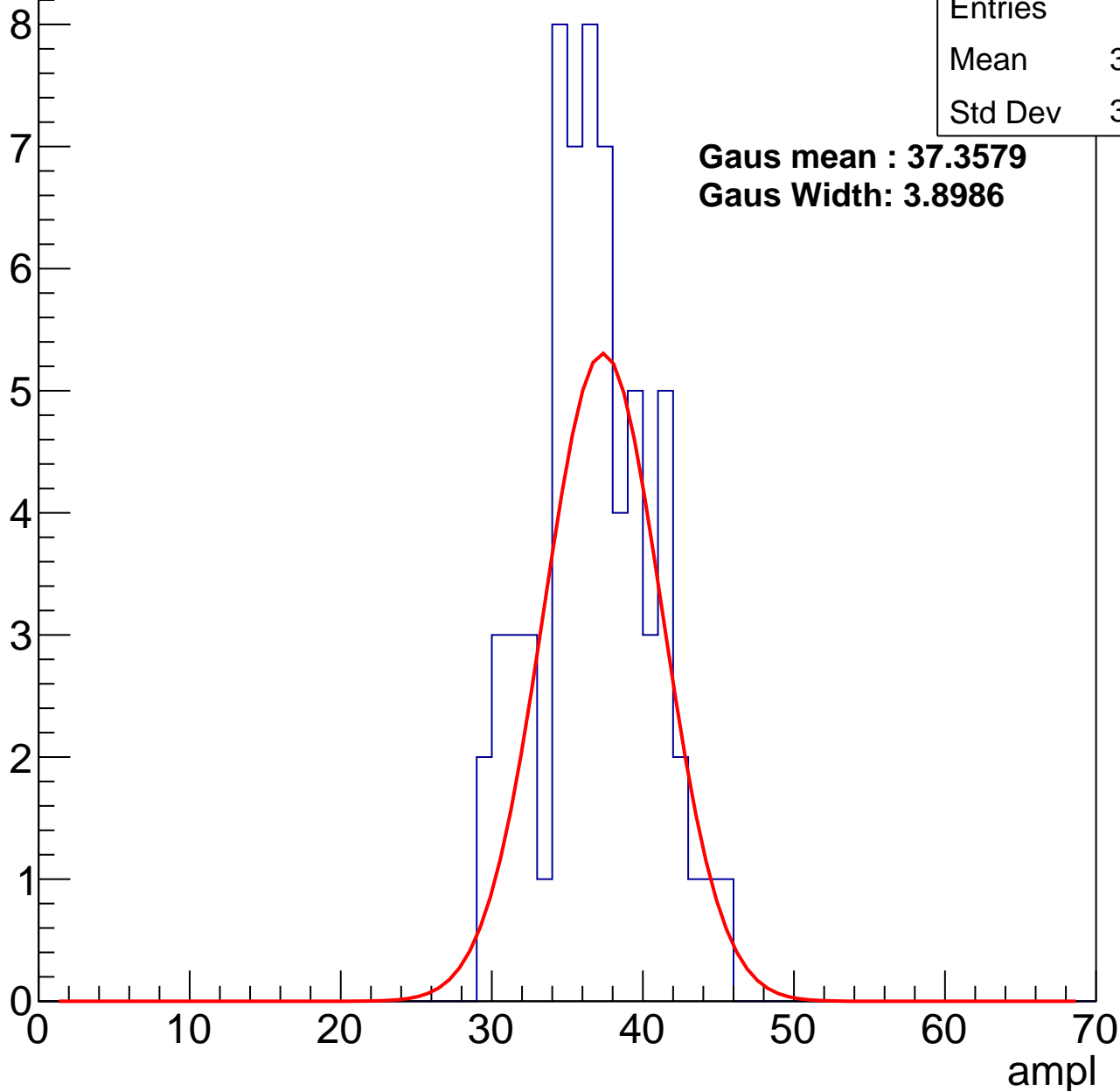
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	36.28
Std Dev	3.706

**Gaus mean : 37.3579**

**Gaus Width: 3.8986**



# B1L102S, U5-ch4, adc2

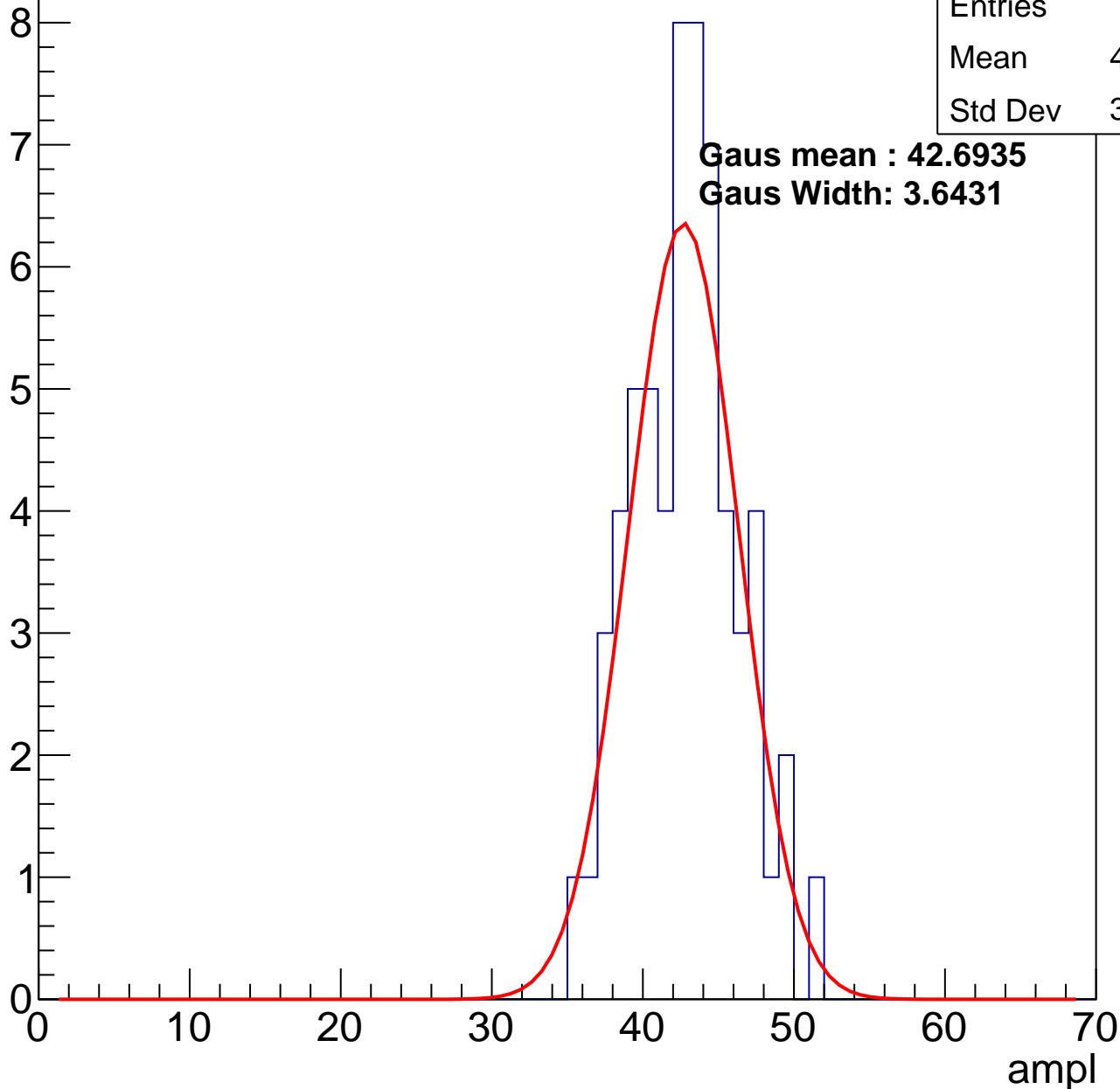
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	42.36
Std Dev	3.436

**Gaus mean : 42.6935**

**Gaus Width: 3.6431**



# B1L102S, U5-ch4, adc3

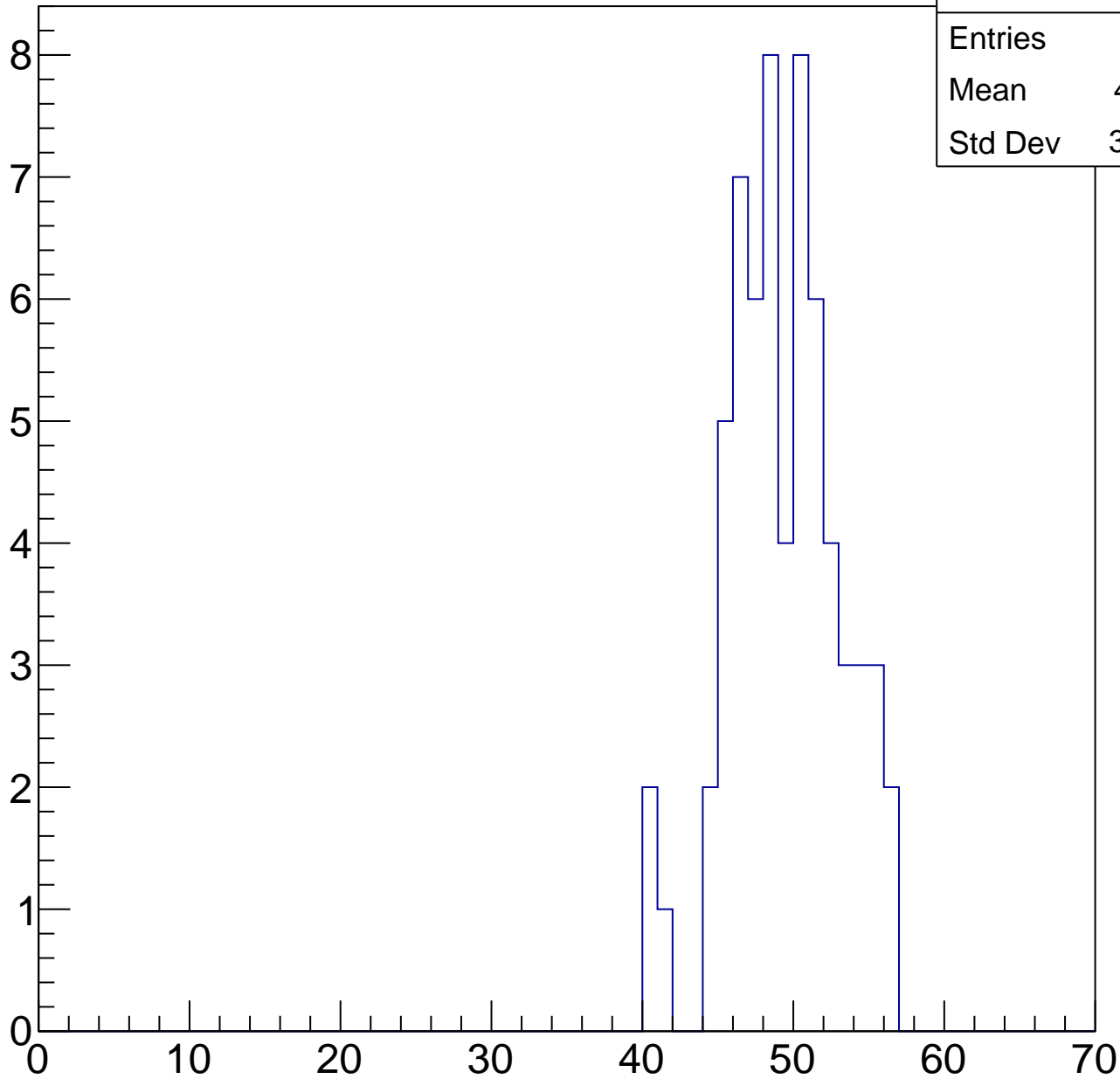
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	64
Mean	48.91
Std Dev	3.639

ampl

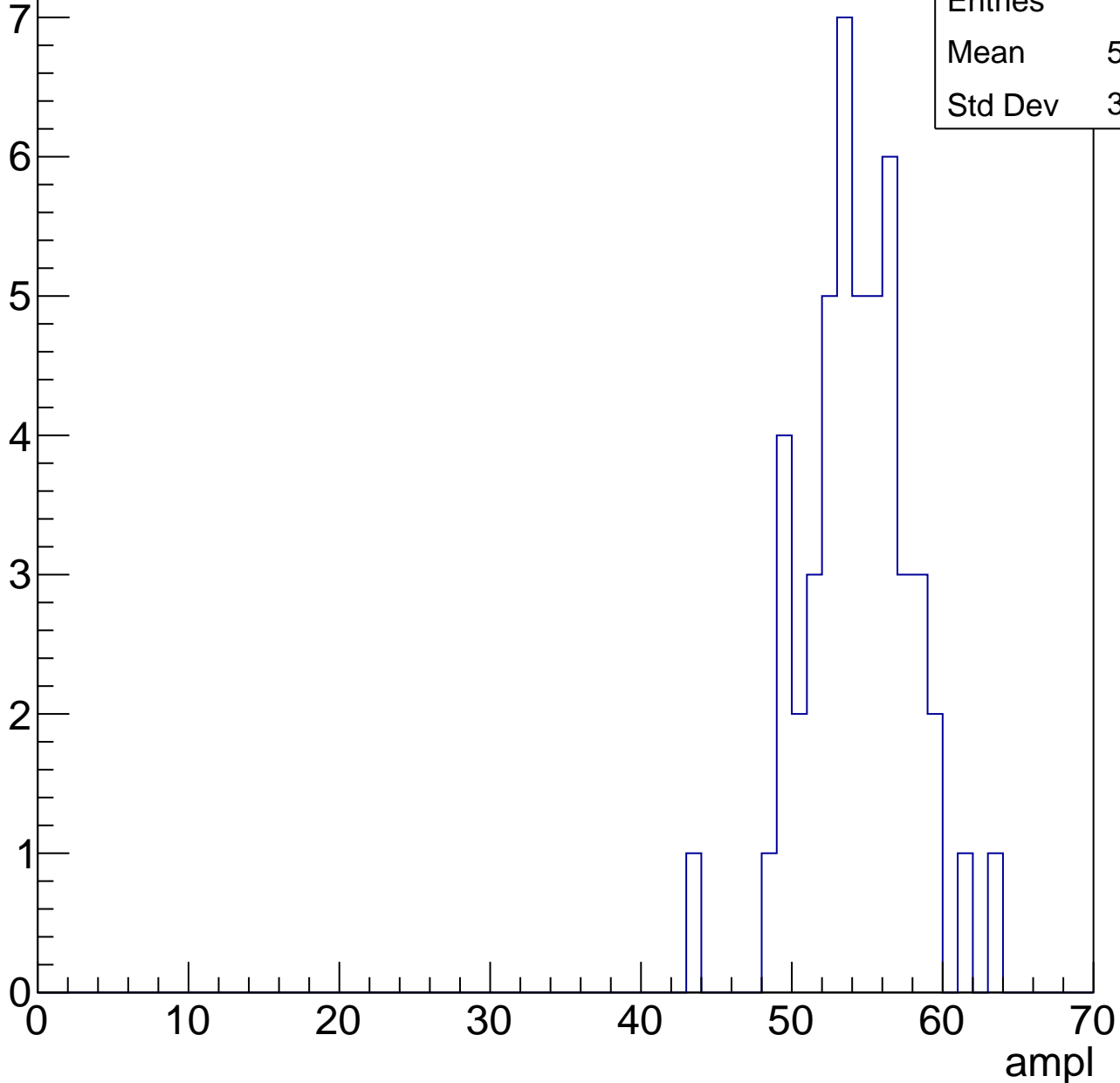


# B1L102S, U5-ch4, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

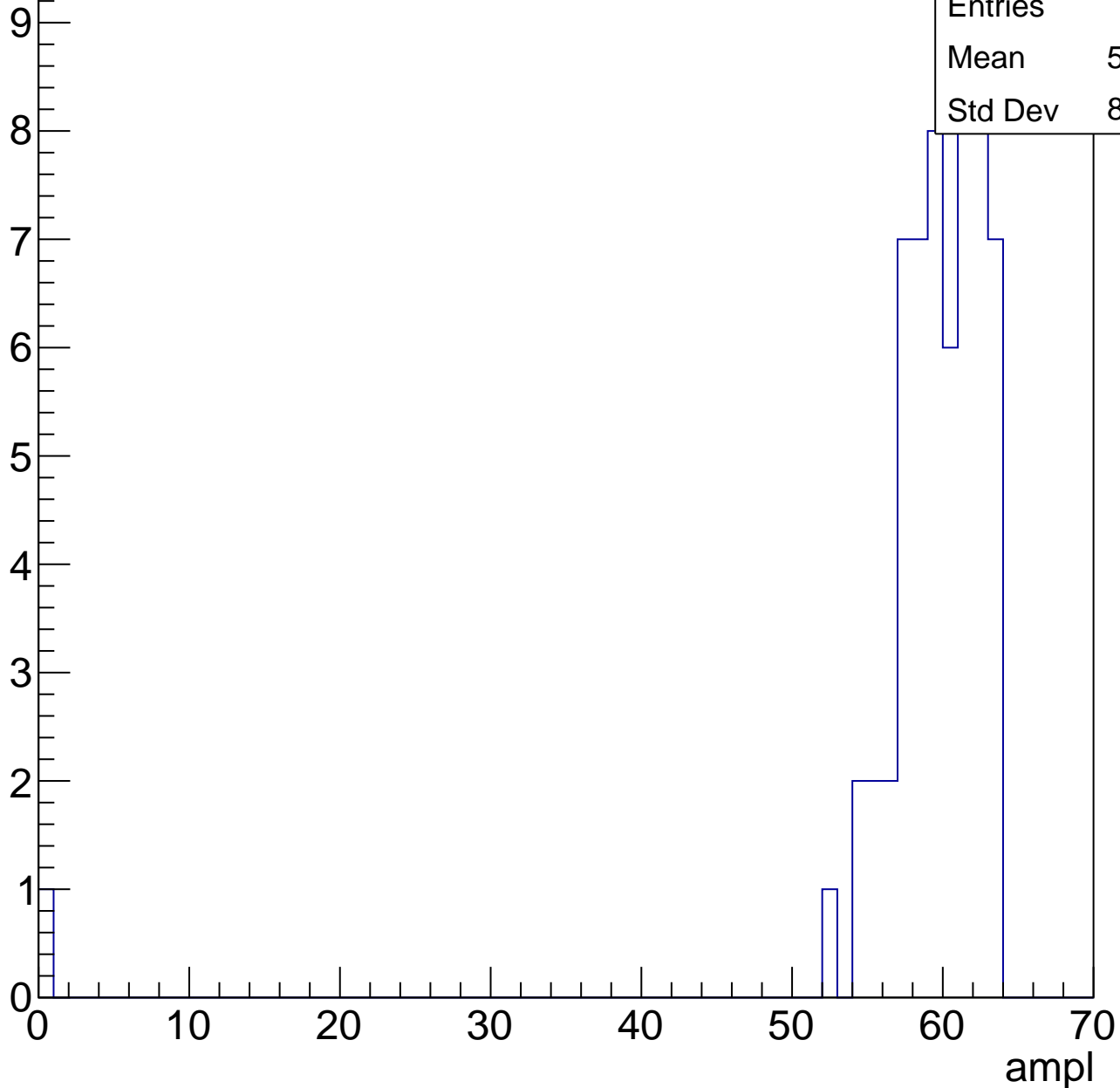
Entries	49
Mean	53.86
Std Dev	3.574



# B1L102S, U5-ch4, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

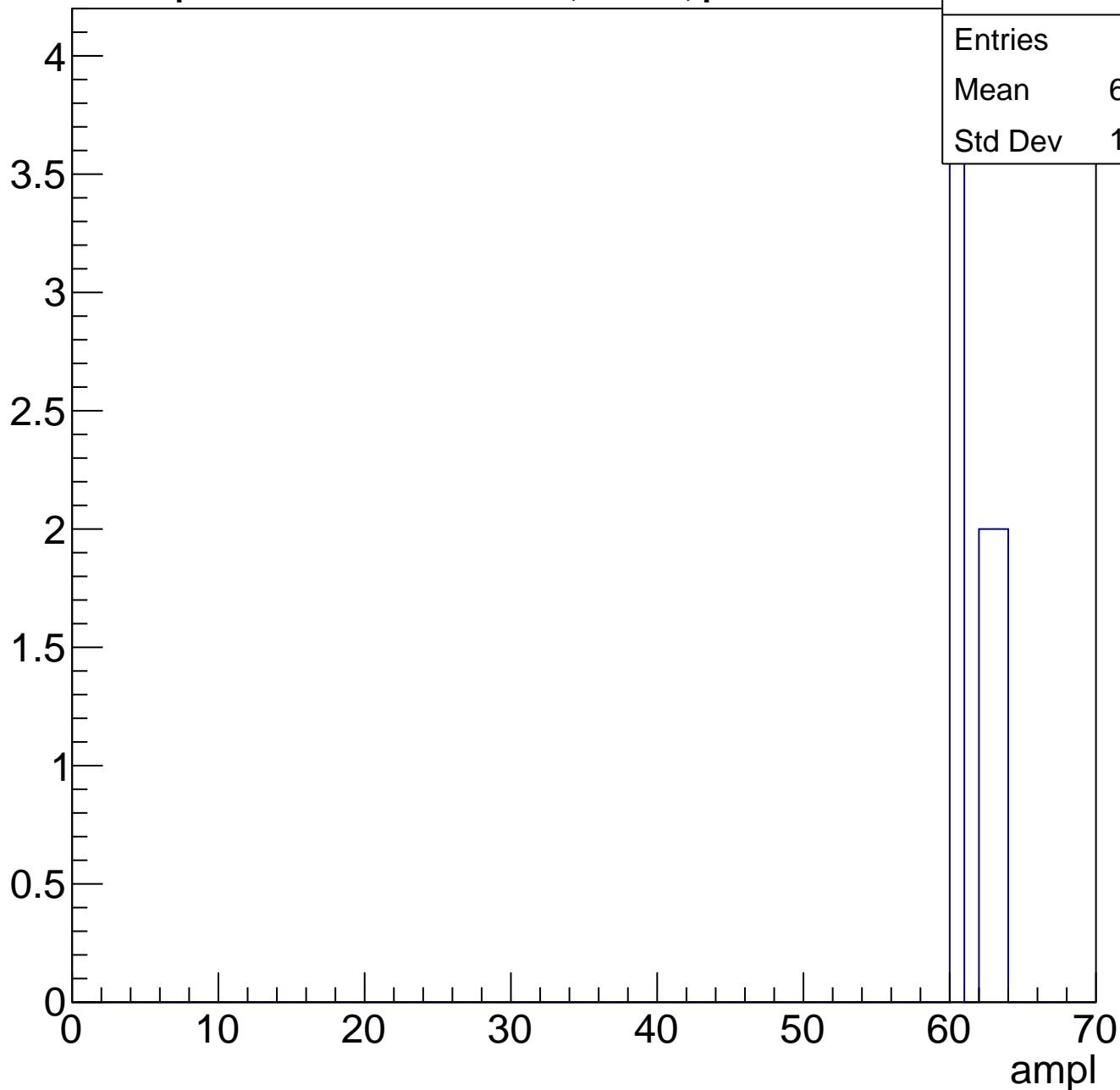
Entry



# B1L102S, U5-ch4, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

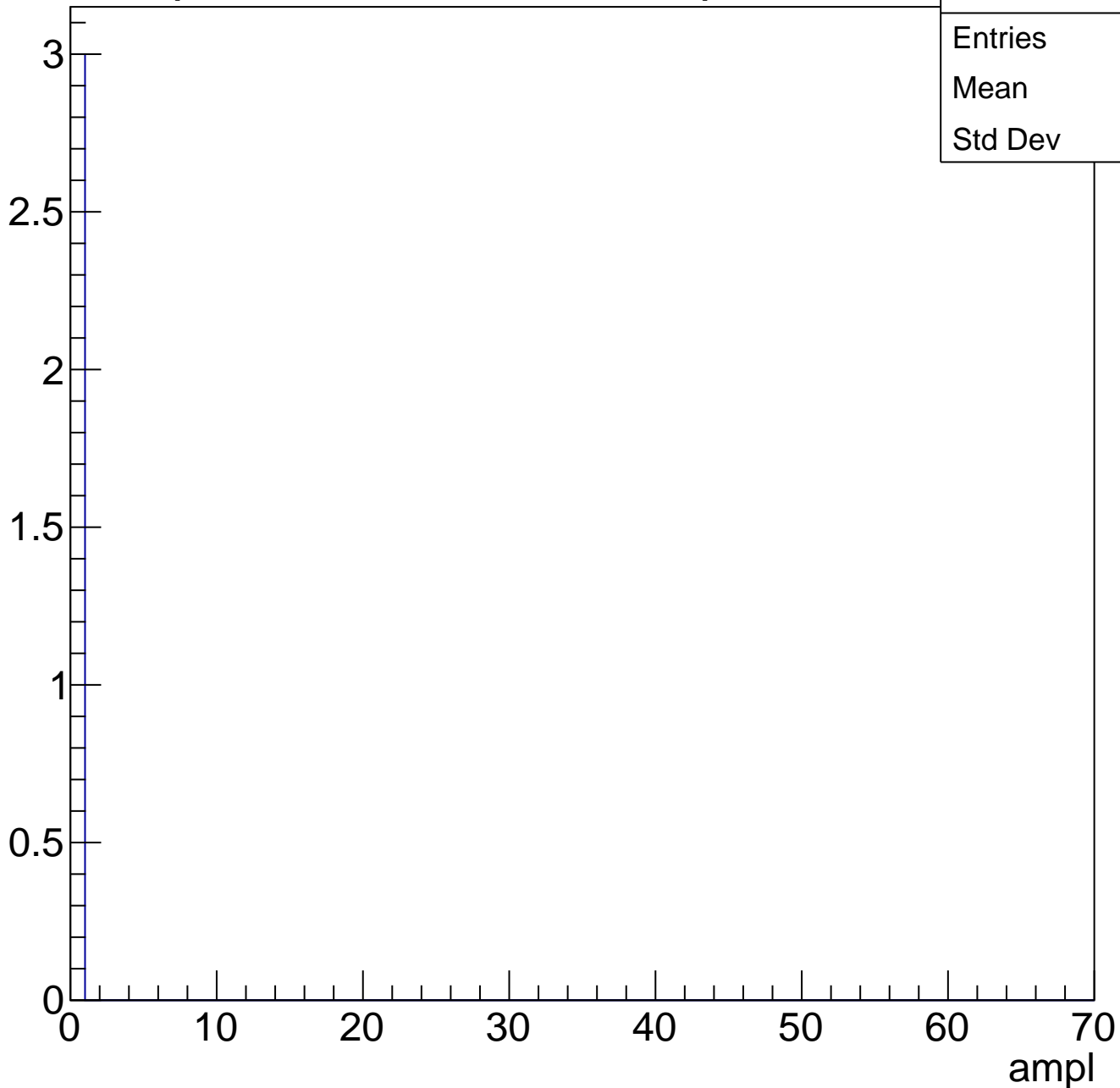




# B1L102S, U5-ch4, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L102S, U5-ch5, adc0

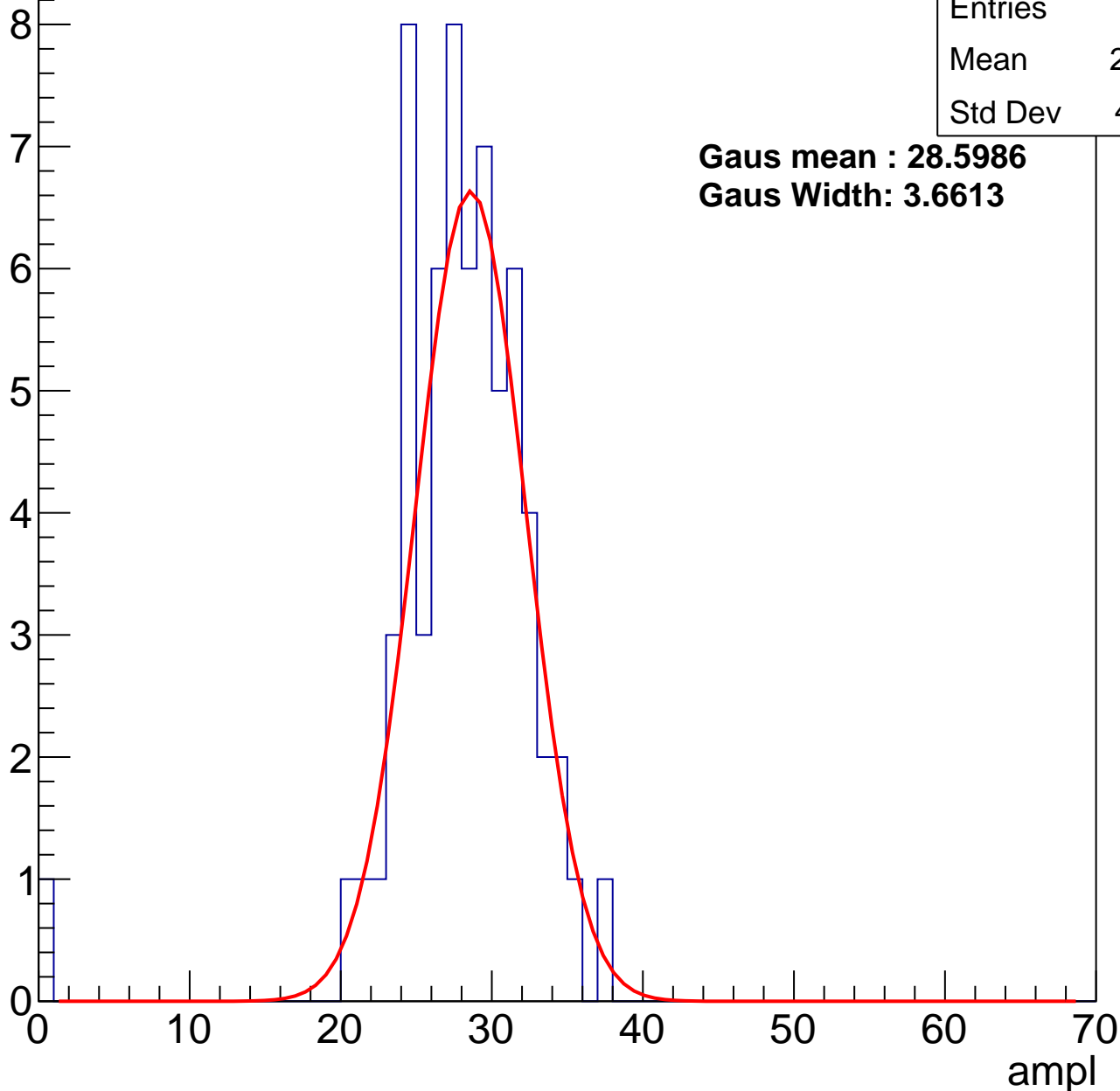
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	27.45
Std Dev	4.881

**Gaus mean : 28.5986**

**Gaus Width: 3.6613**



# B1L102S, U5-ch5, adc1

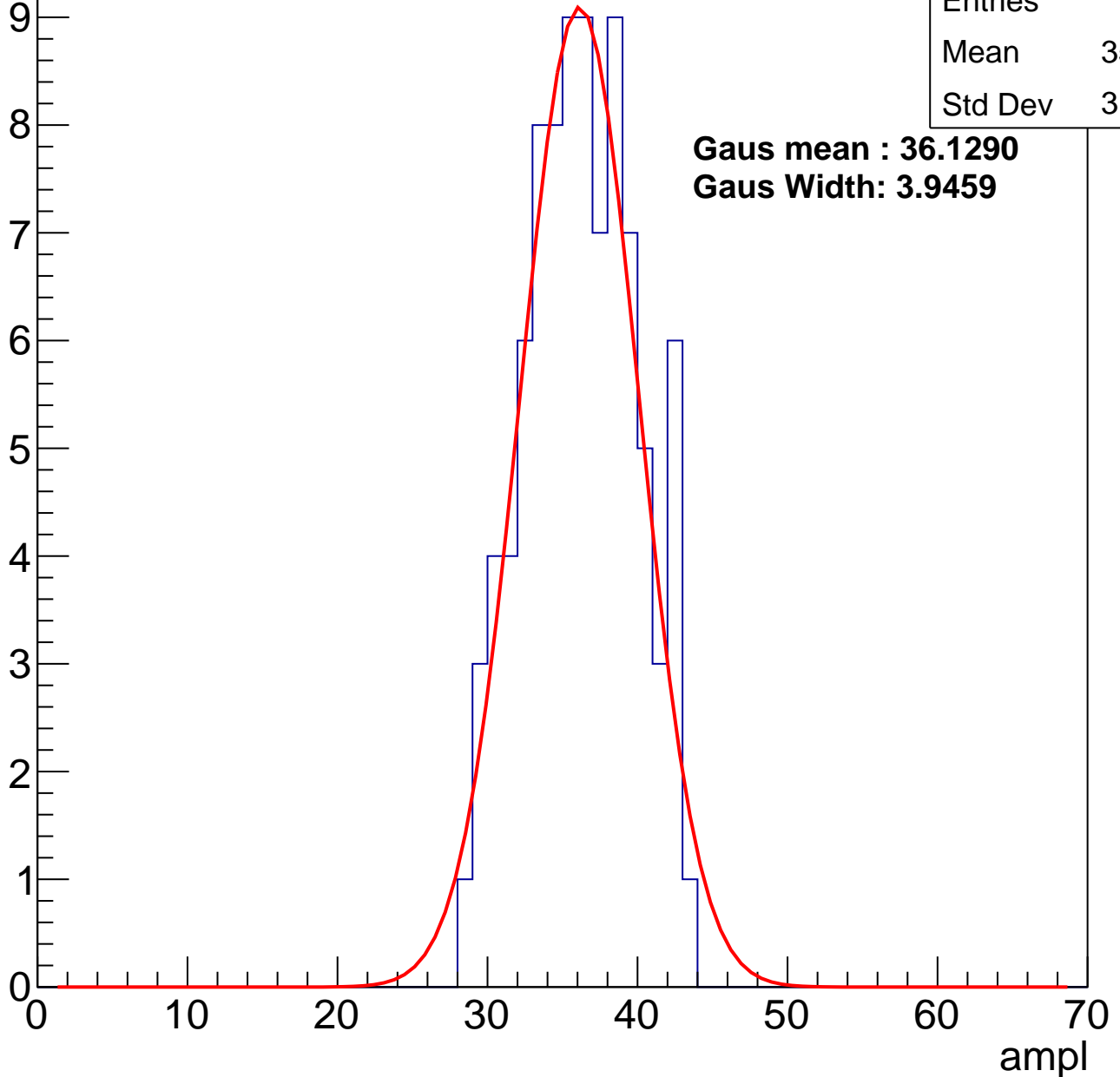
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	90
Mean	35.76
Std Dev	3.628

**Gaus mean : 36.1290**

**Gaus Width: 3.9459**



# B1L102S, U5-ch5, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

6  
5  
4  
3  
2  
1  
0

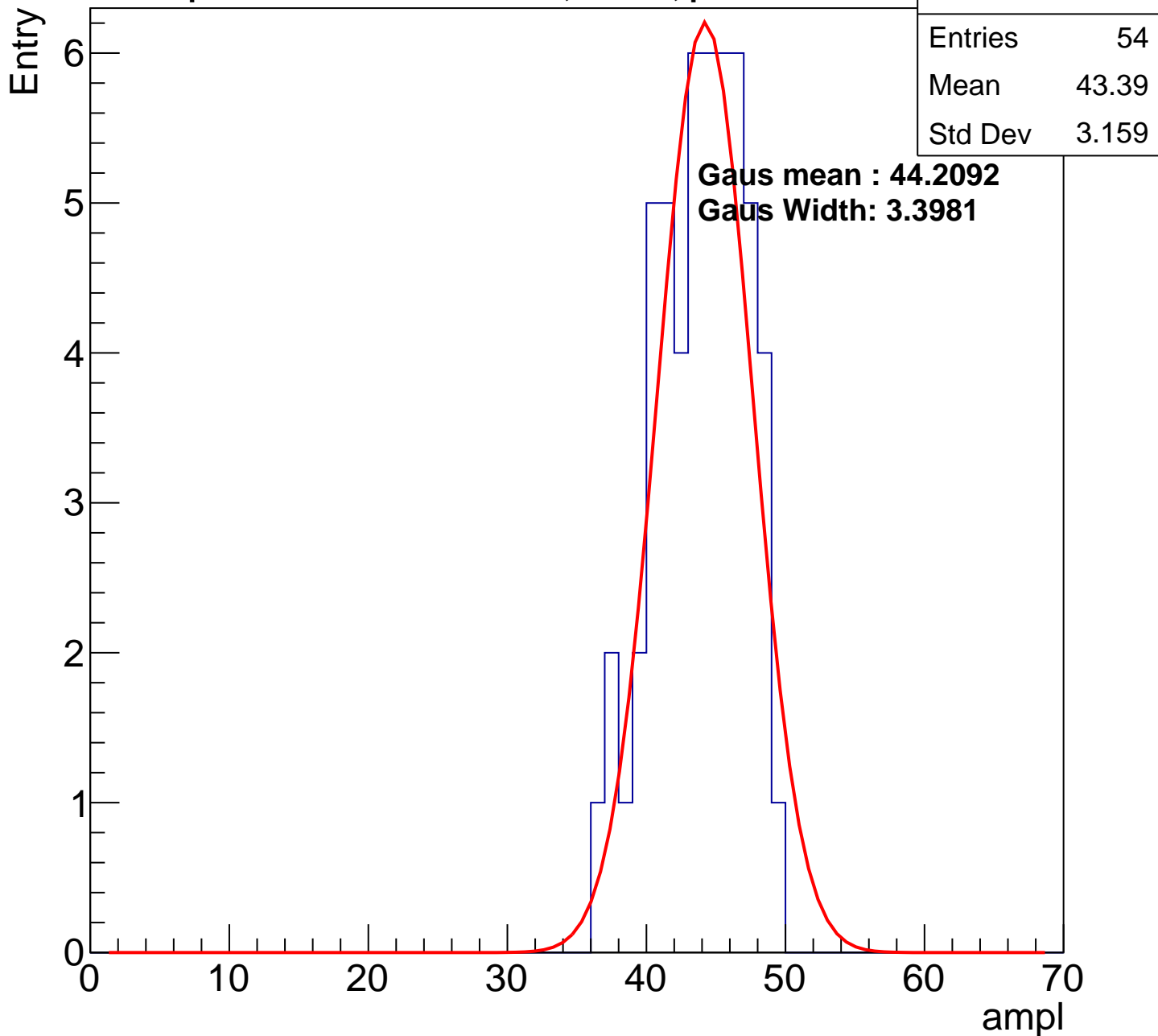
Entries	54
Mean	43.39
Std Dev	3.159

**Gaus mean : 44.2092**

**Gaus Width: 3.3981**

ampl

0 10 20 30 40 50 60 70

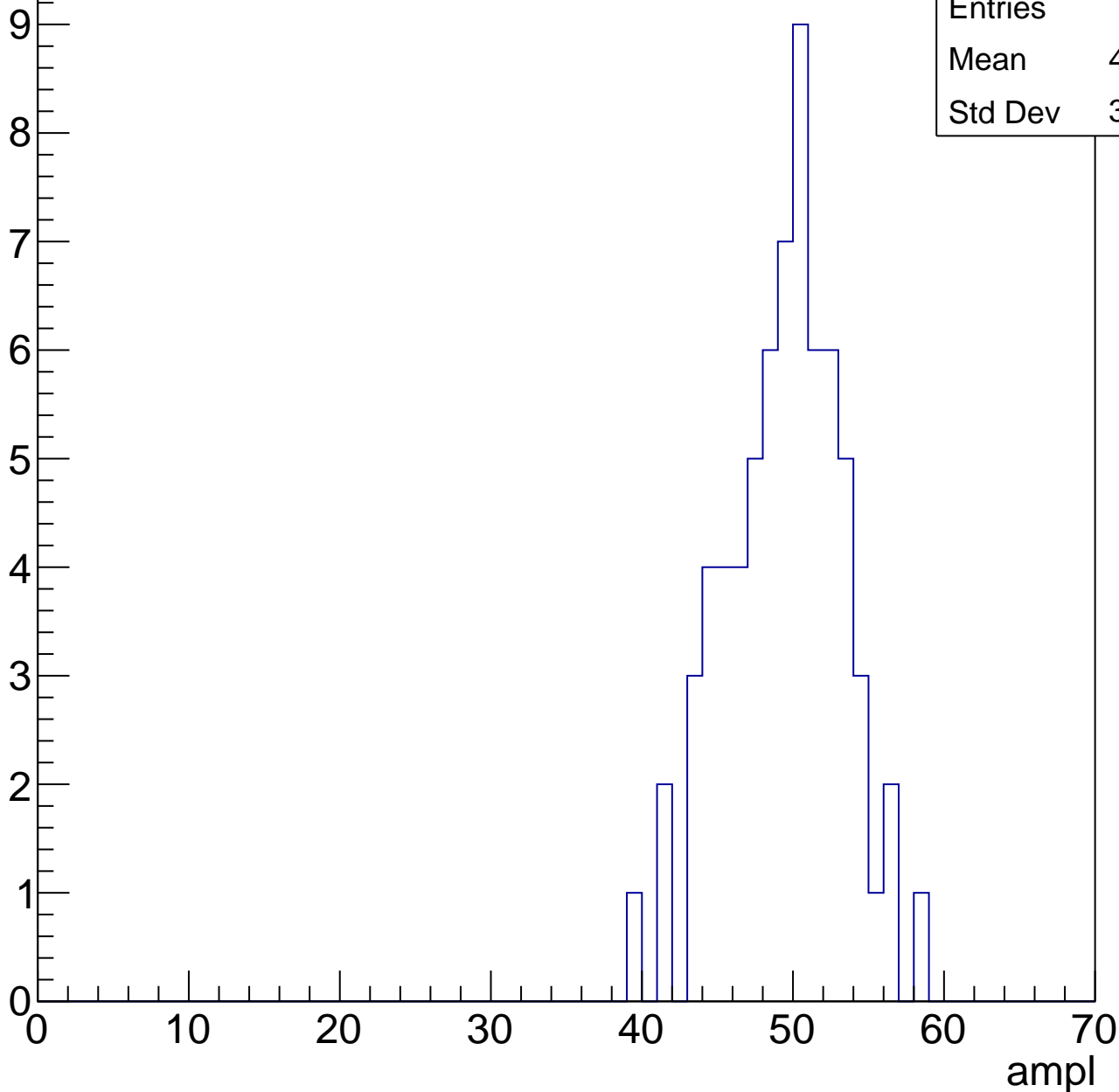


# B1L102S, U5-ch5, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	48.93
Std Dev	3.842

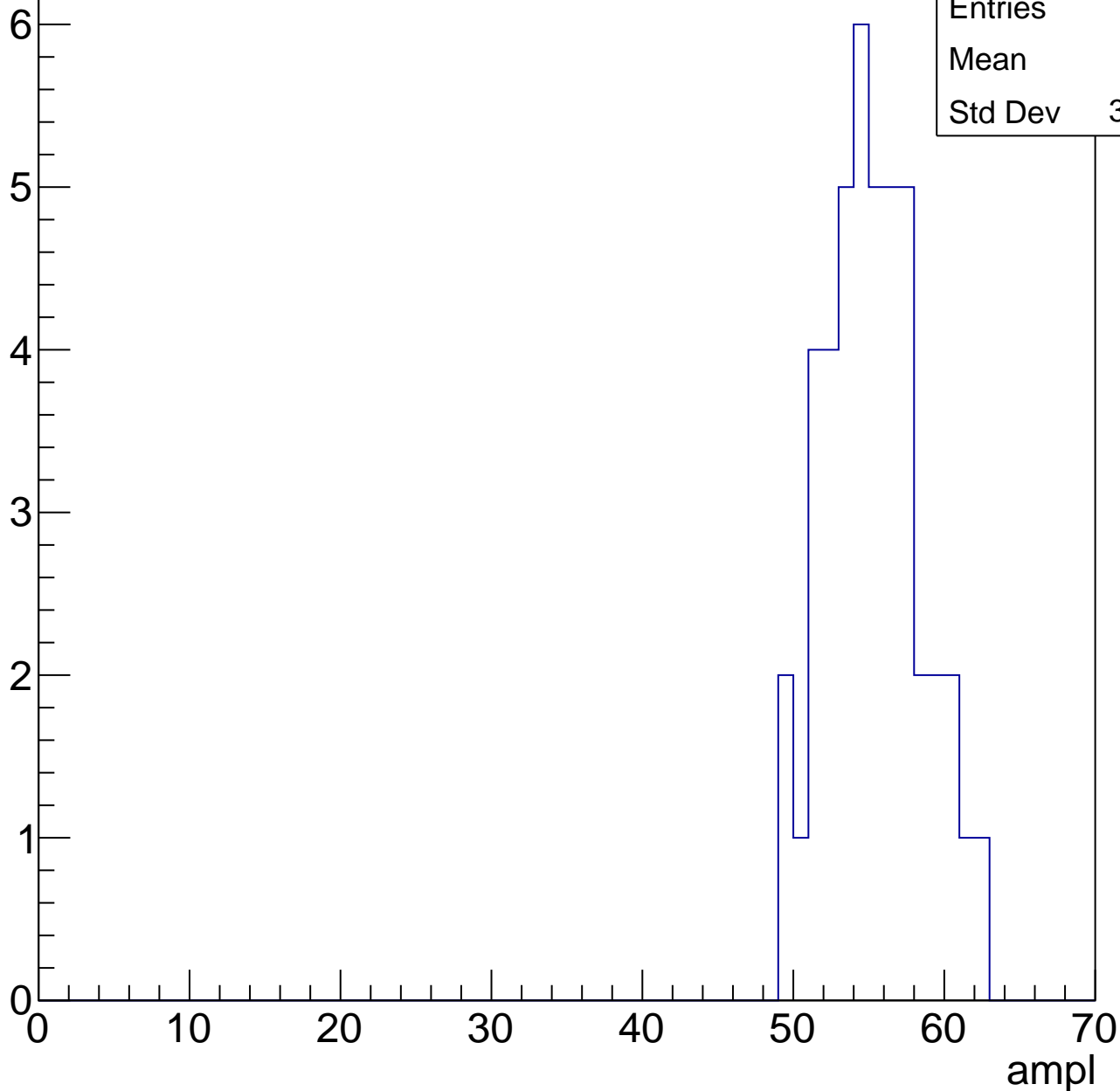


# B1L102S, U5-ch5, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	45
Mean	54.8
Std Dev	3.096



# B1L102S, U5-ch5, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

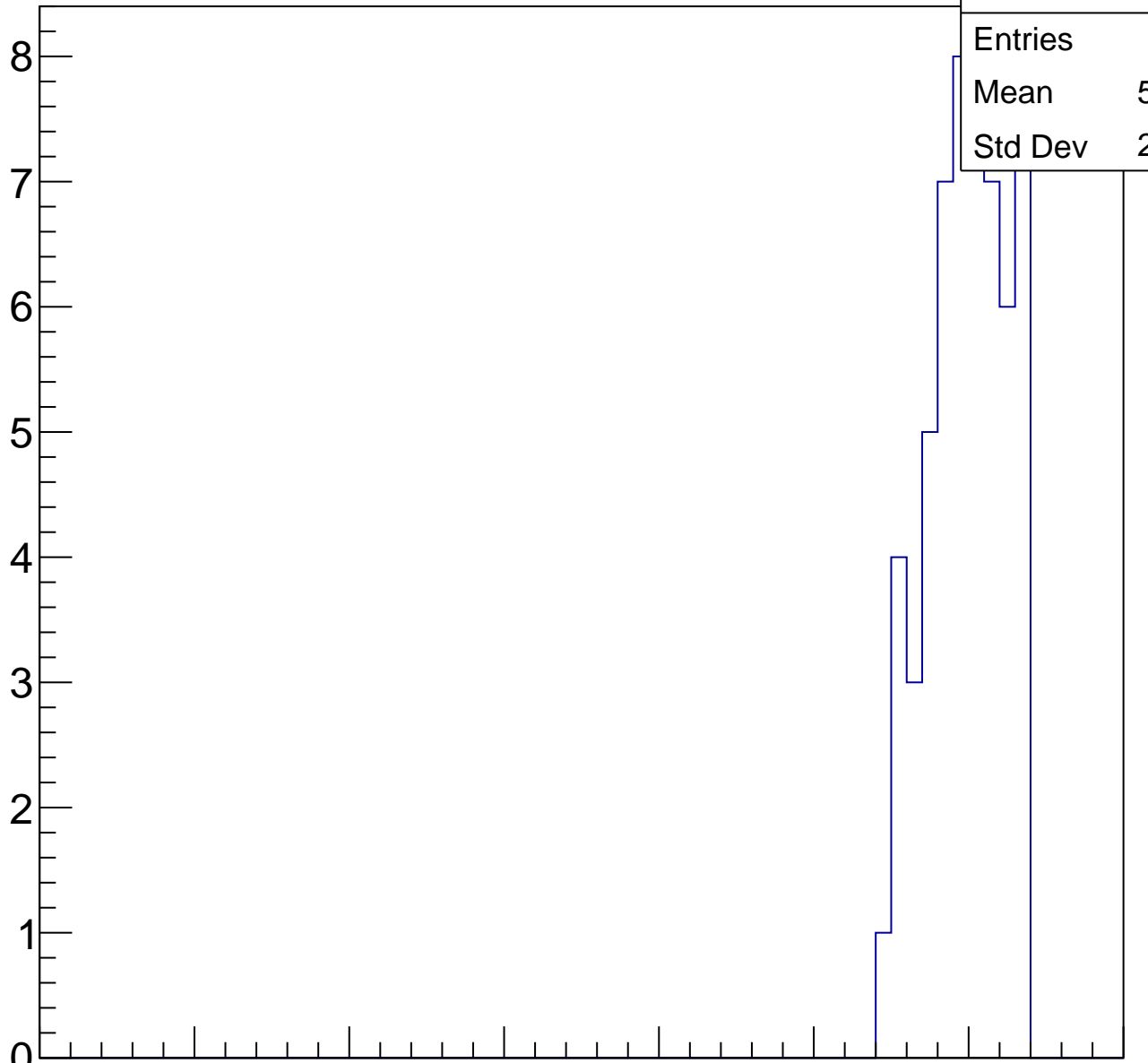
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	57
Mean	59.44
Std Dev	2.478

ampl

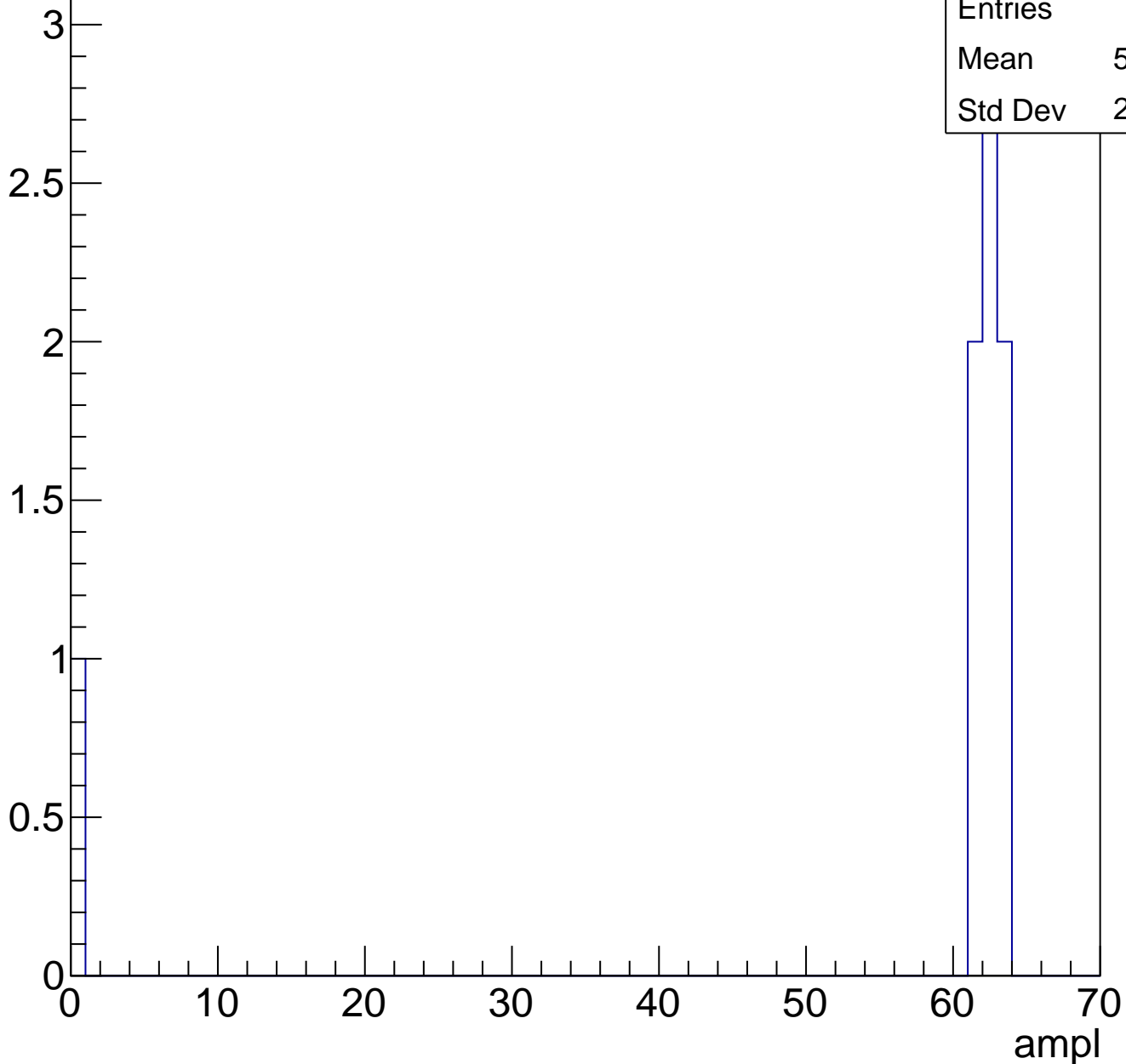
0 10 20 30 40 50 60 70



# B1L102S, U5-ch5, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U5-ch5, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U5-ch6, adc0

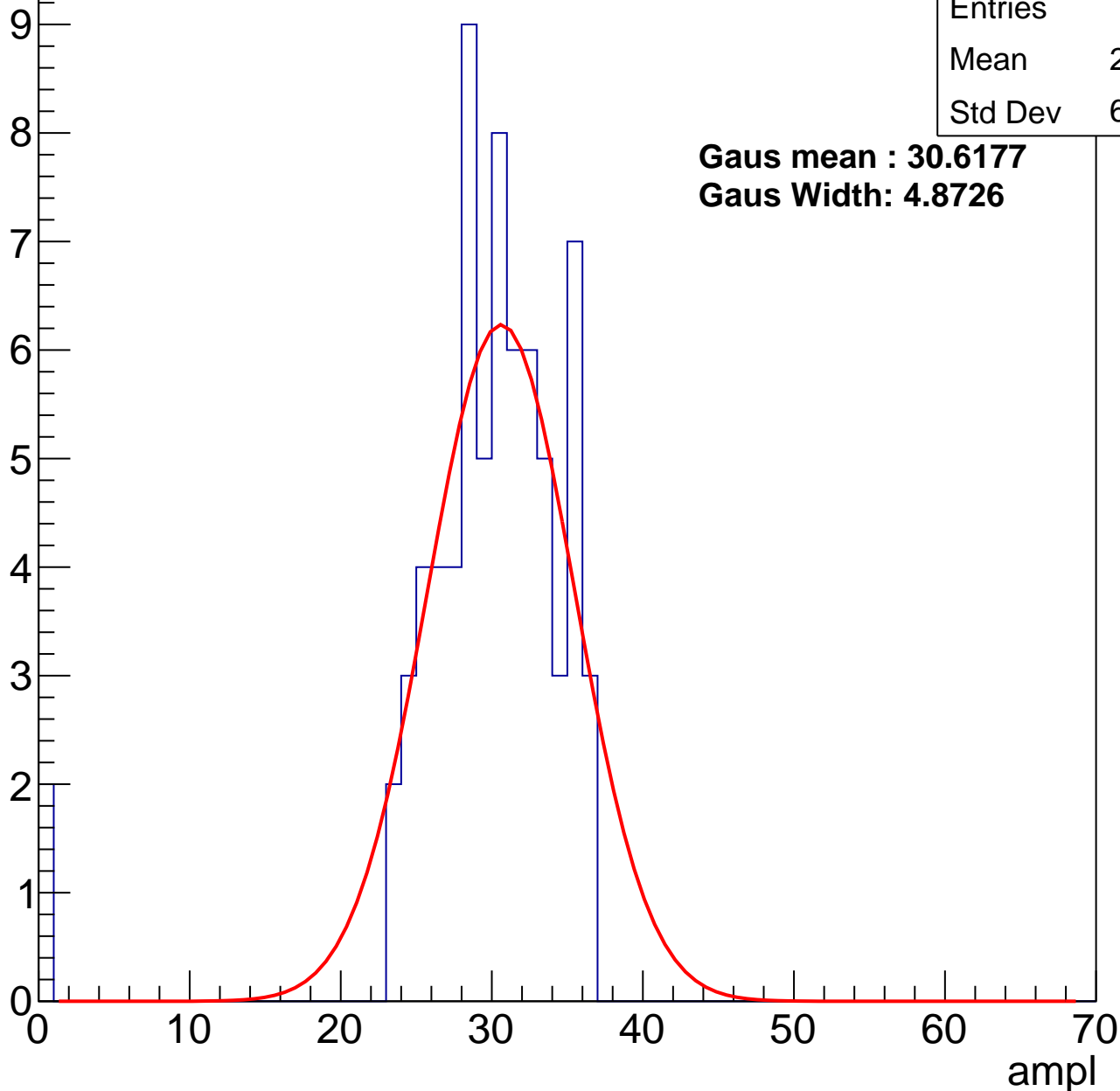
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	29.08
Std Dev	6.044

**Gaus mean : 30.6177**

**Gaus Width: 4.8726**



# B1L102S, U5-ch6, adc1

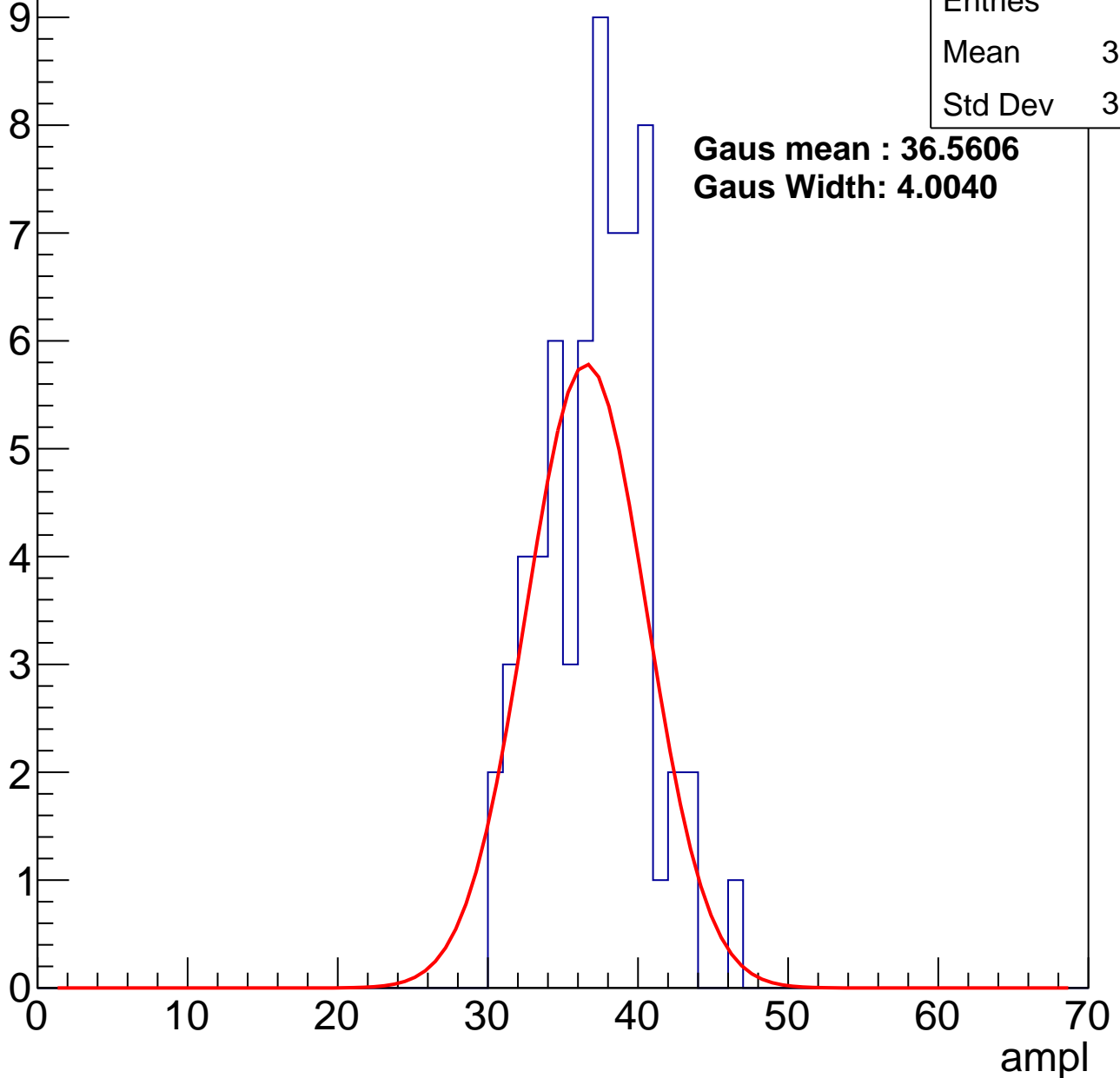
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	36.72
Std Dev	3.426

**Gaus mean : 36.5606**

**Gaus Width: 4.0040**



# B1L102S, U5-ch6, adc2

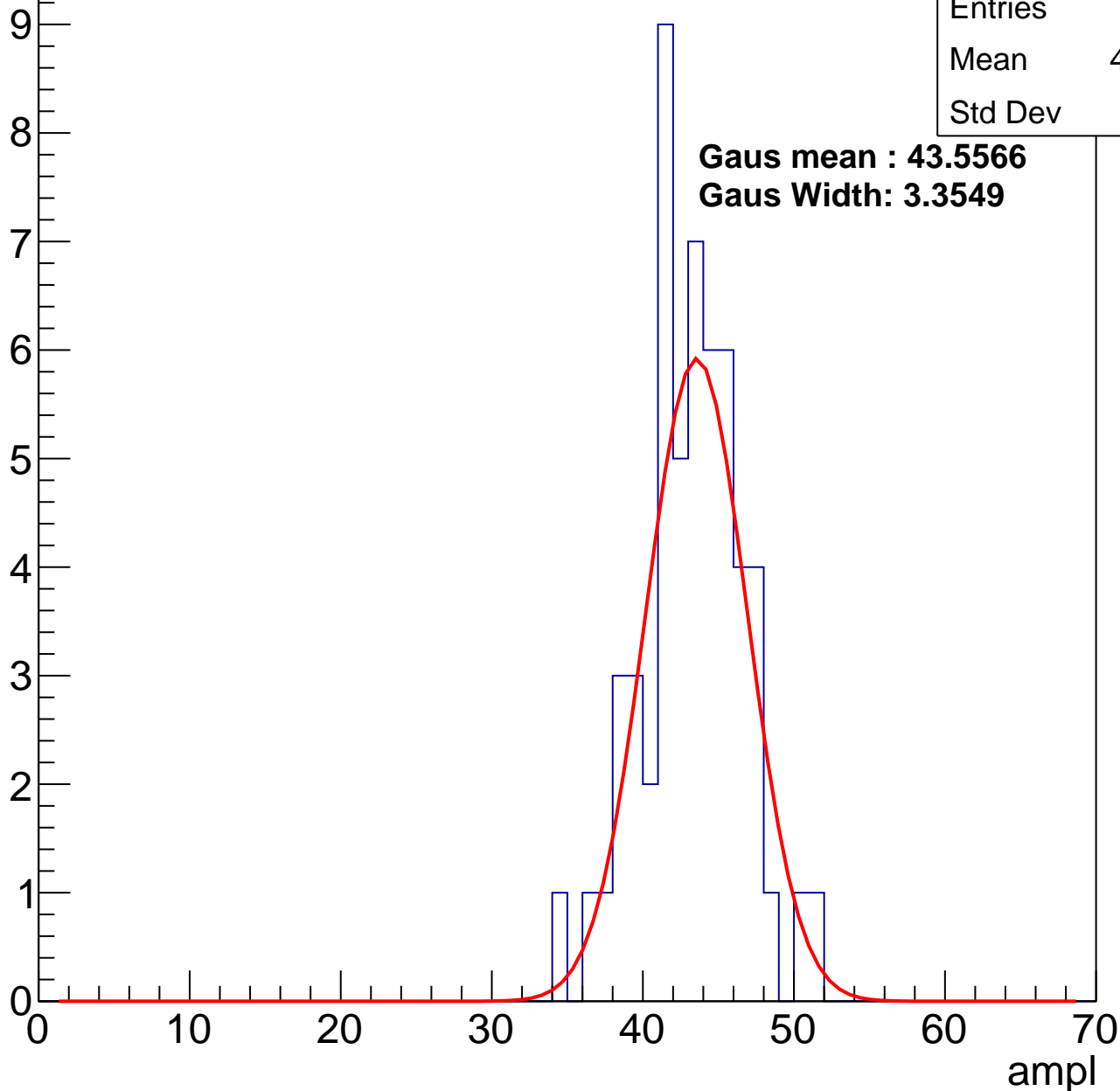
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	42.78
Std Dev	3.34

**Gaus mean : 43.5566**

**Gaus Width: 3.3549**

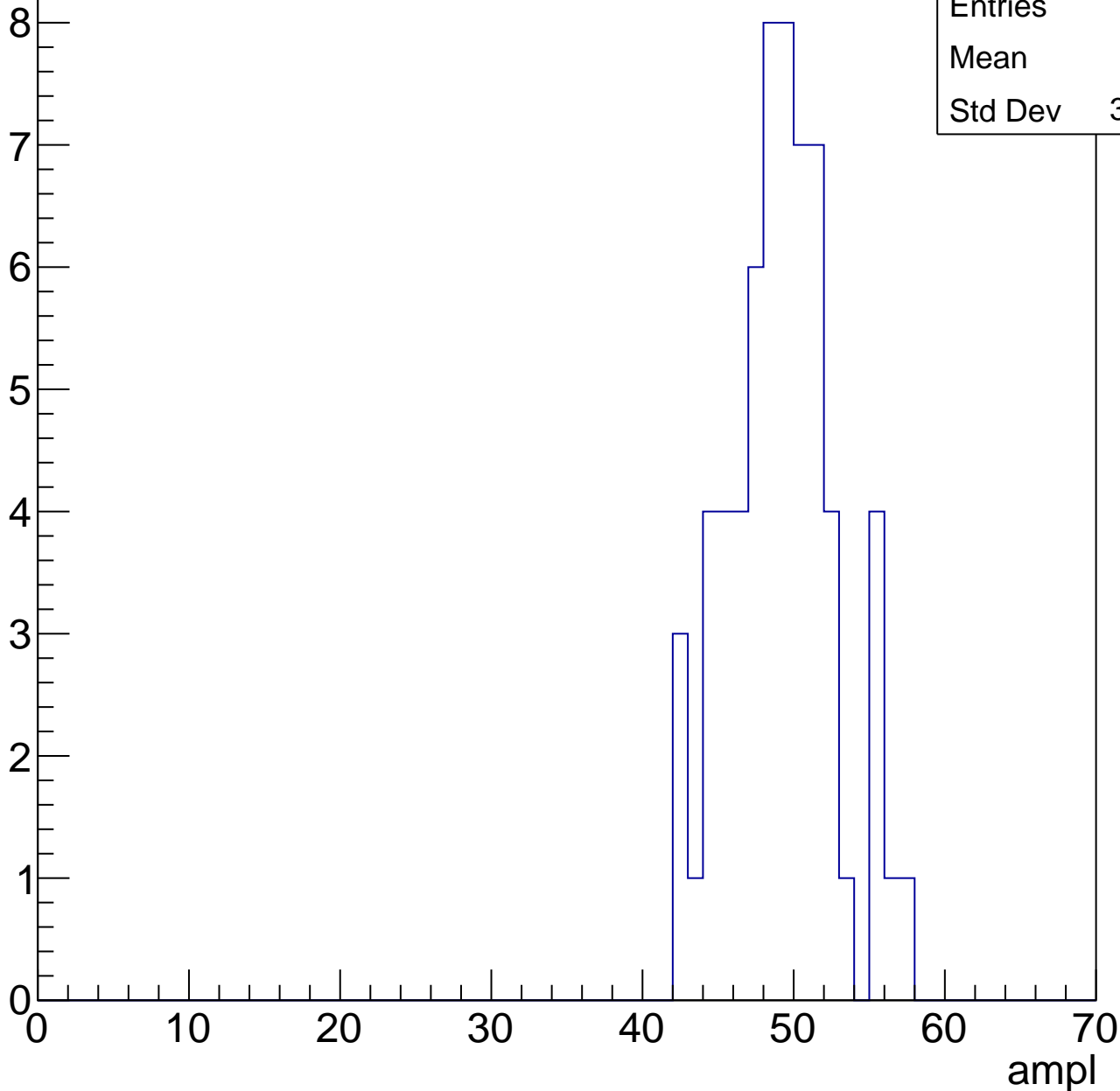


# B1L102S, U5-ch6, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	48.7
Std Dev	3.458

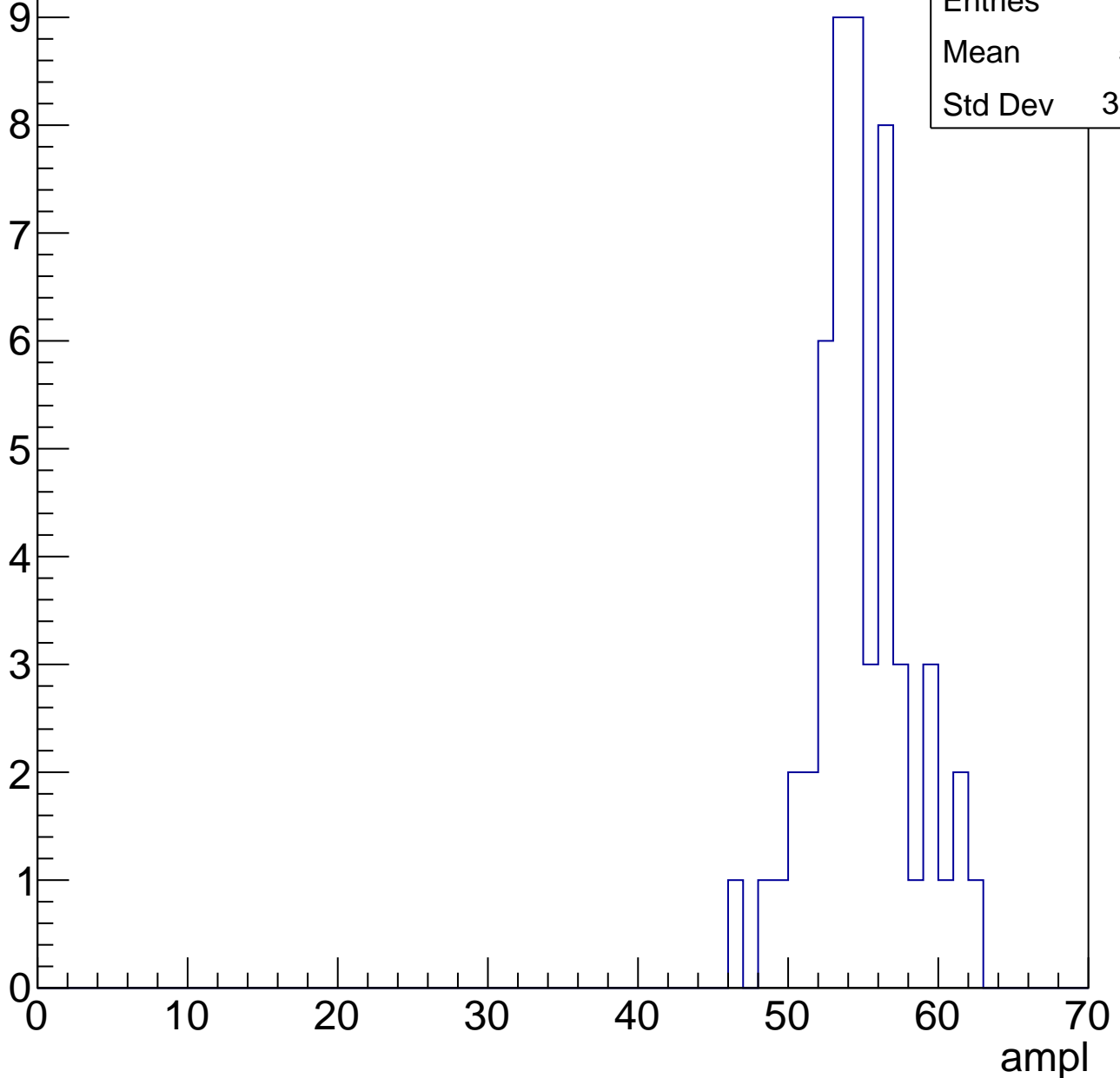


# B1L102S, U5-ch6, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

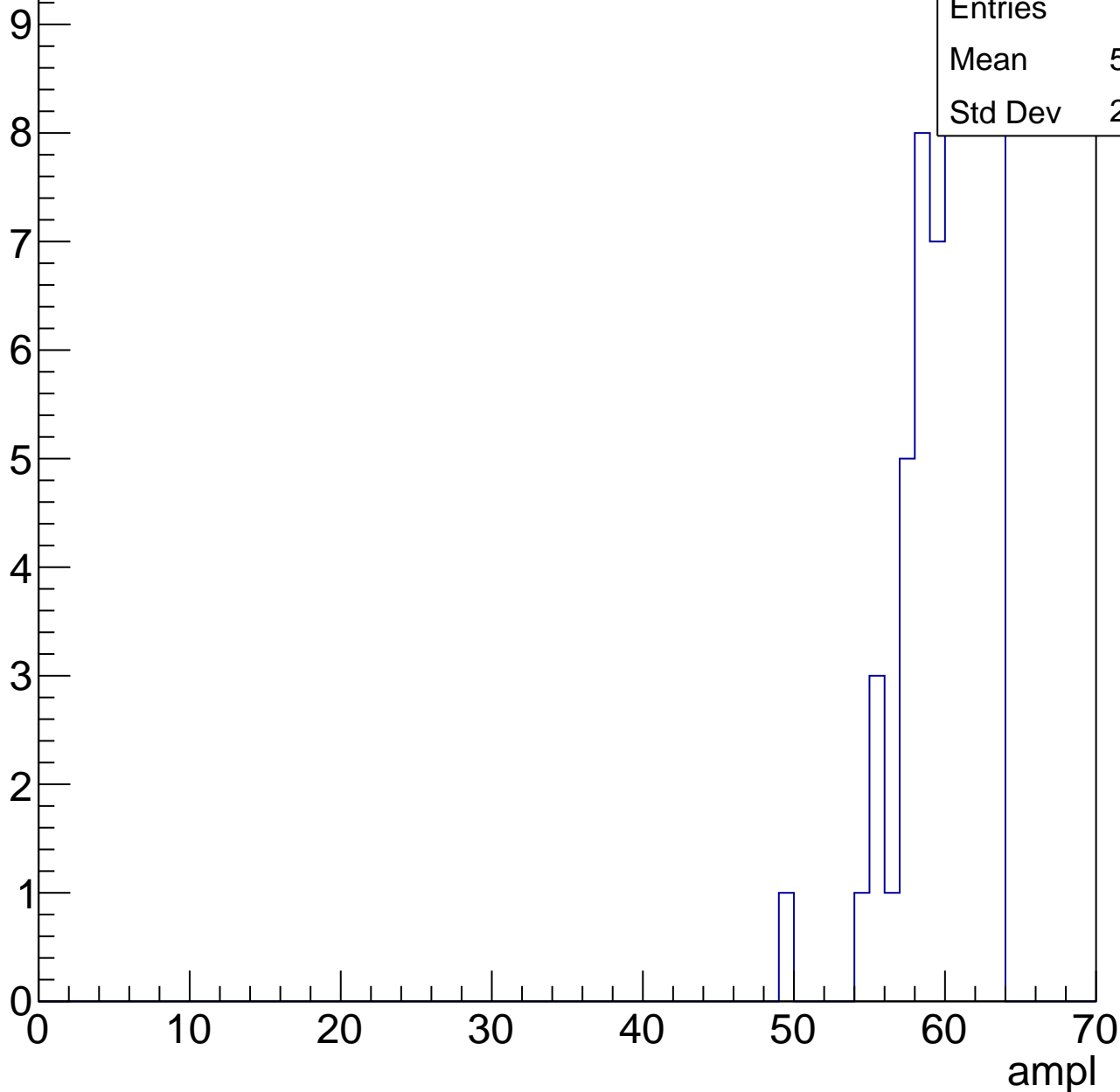
Entries	53
Mean	54.4
Std Dev	3.223



# B1L102S, U5-ch6, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	59
Mean	59.56
Std Dev	2.708

# B1L102S, U5-ch6, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

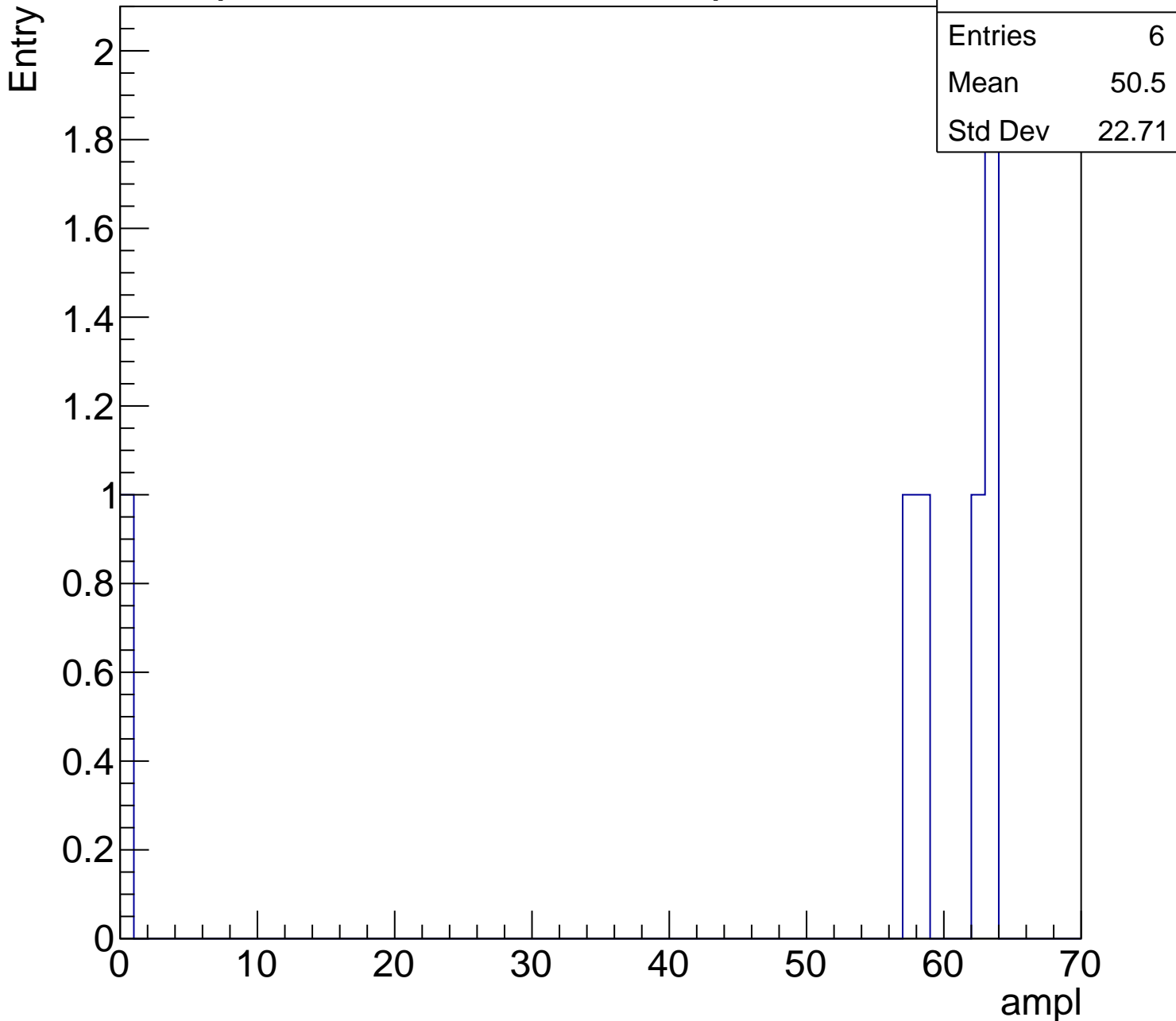
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	50.5
Std Dev	22.71

ampl

0 10 20 30 40 50 60 70





# B1L102S, U5-ch6, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	20
Std Dev	0

ampl

# B1L102S, U5-ch7, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	80
Mean	29.35
Std Dev	3.578

**Gaus mean : 30.3814**

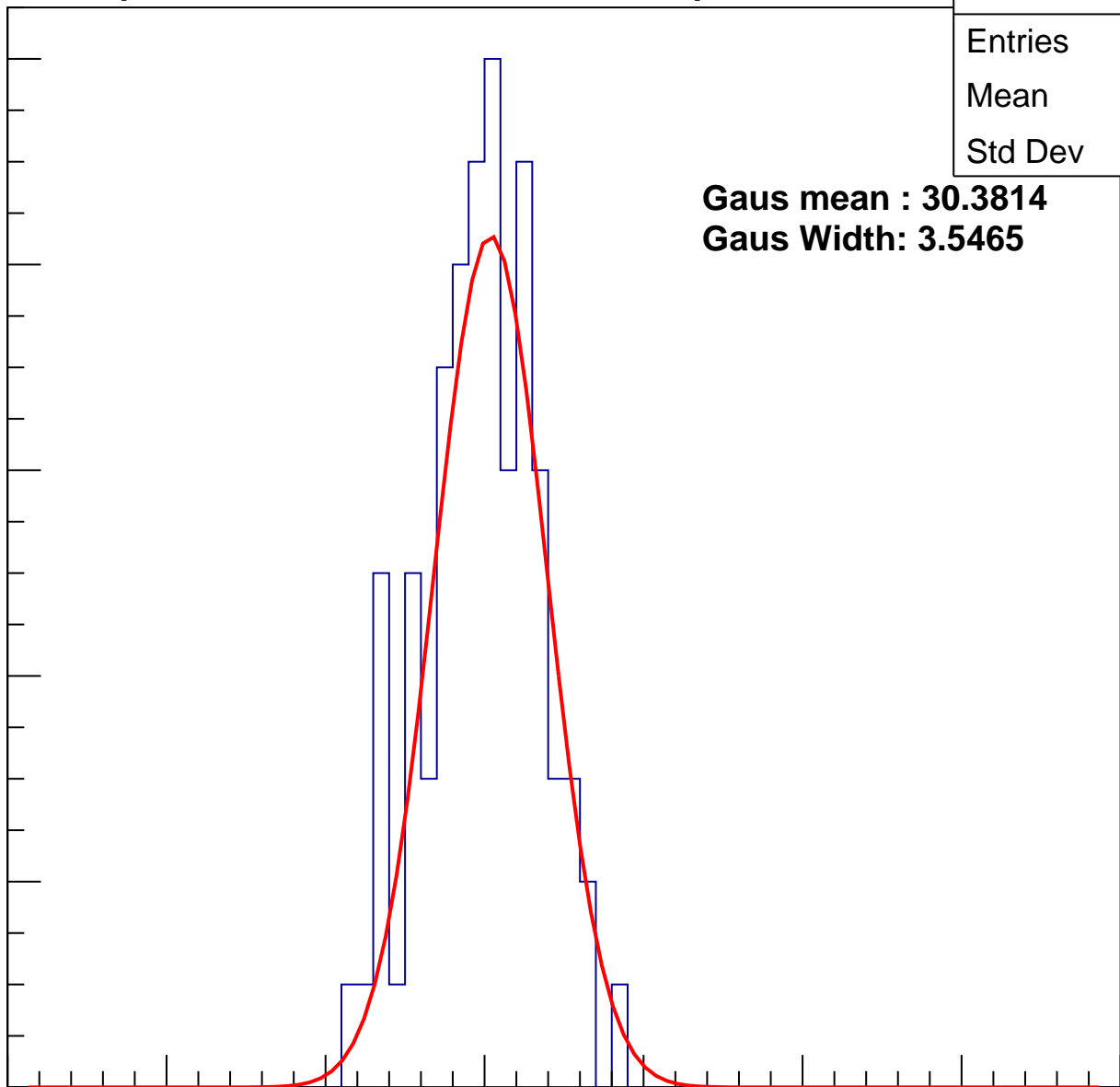
**Gaus Width: 3.5465**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U5-ch7, adc1

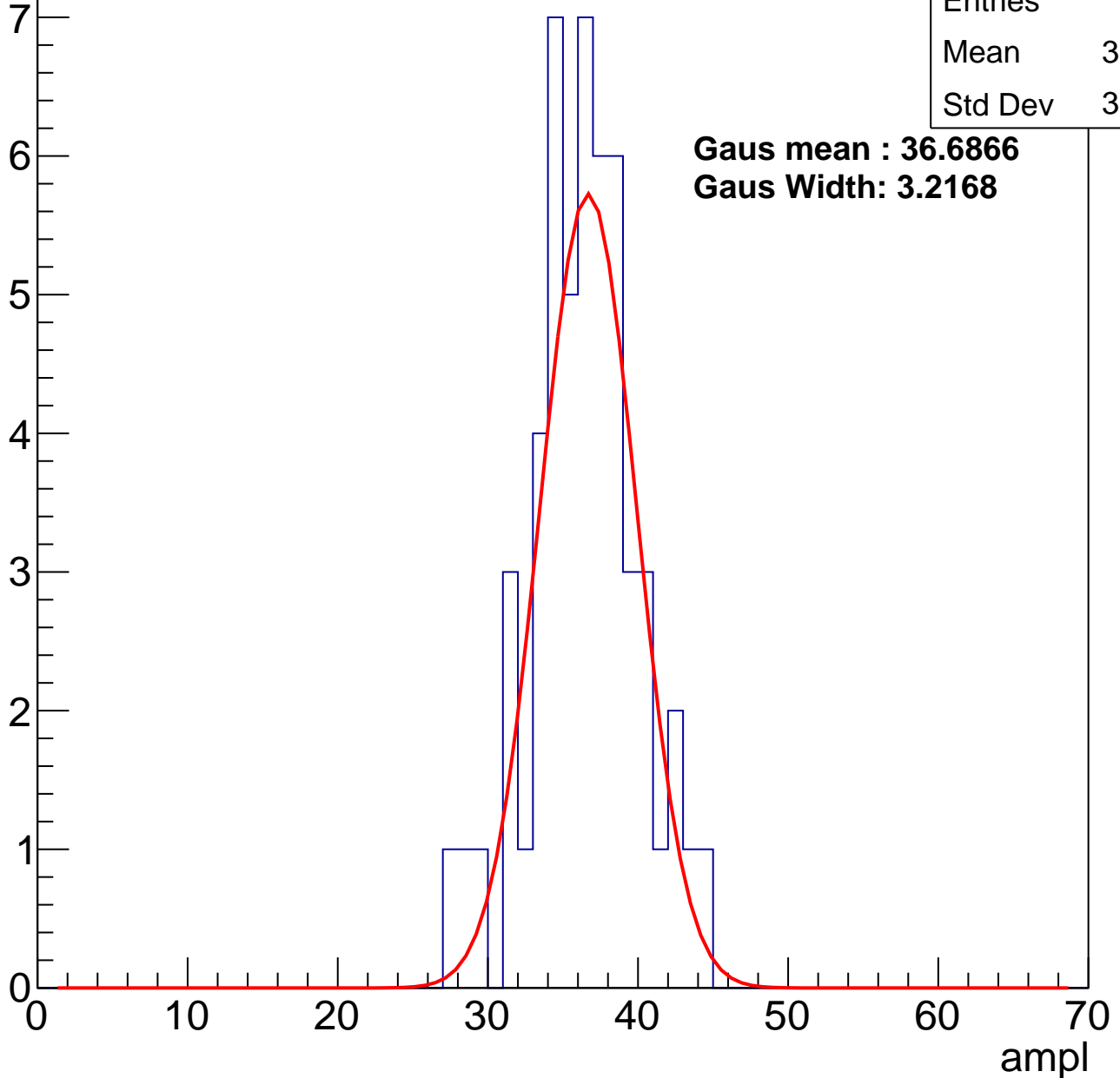
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	35.94
Std Dev	3.552

**Gaus mean : 36.6866**

**Gaus Width: 3.2168**



# B1L102S, U5-ch7, adc2

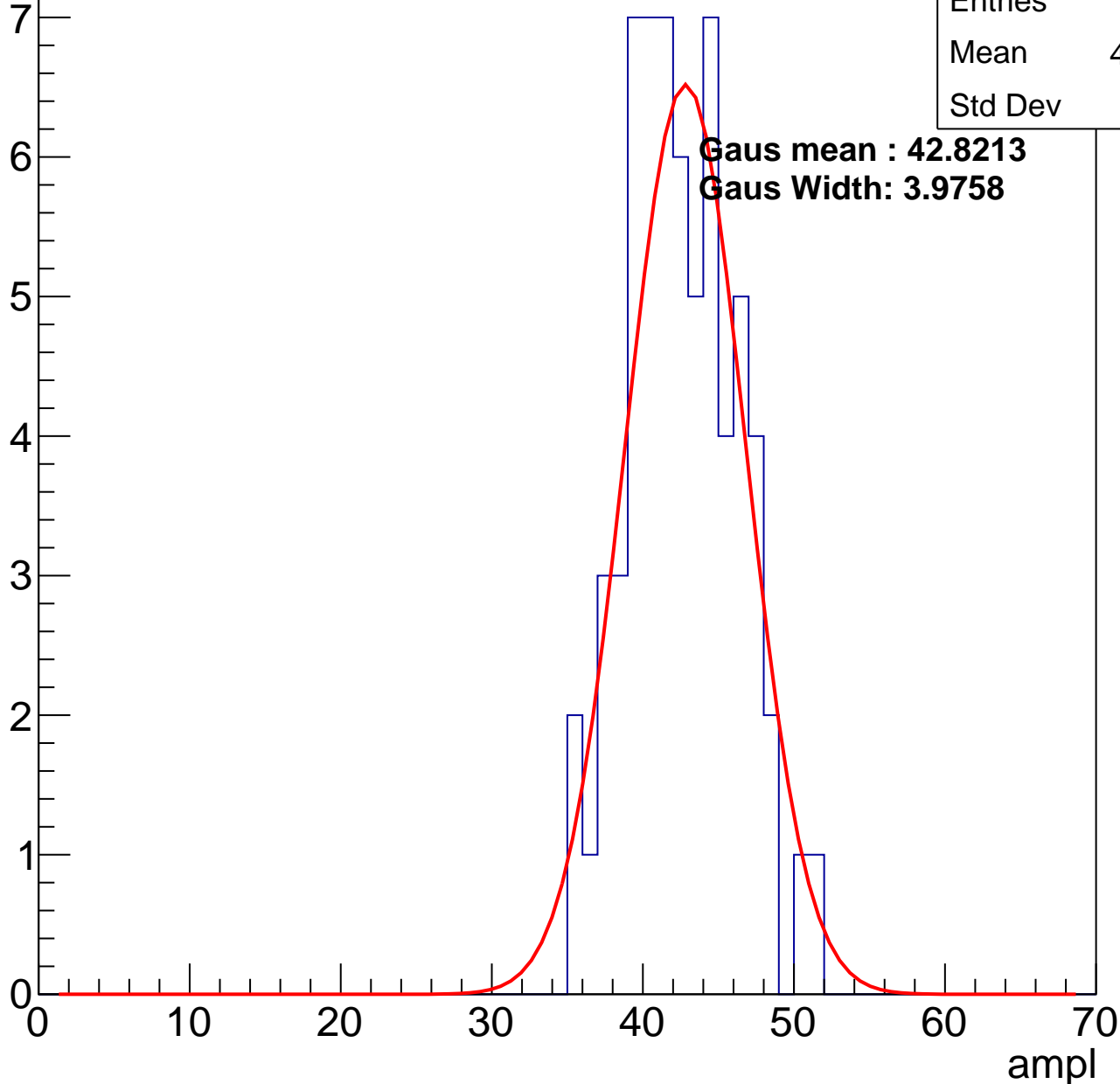
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	42.17
Std Dev	3.55

**Gaus mean : 42.8213**

**Gaus Width: 3.9758**

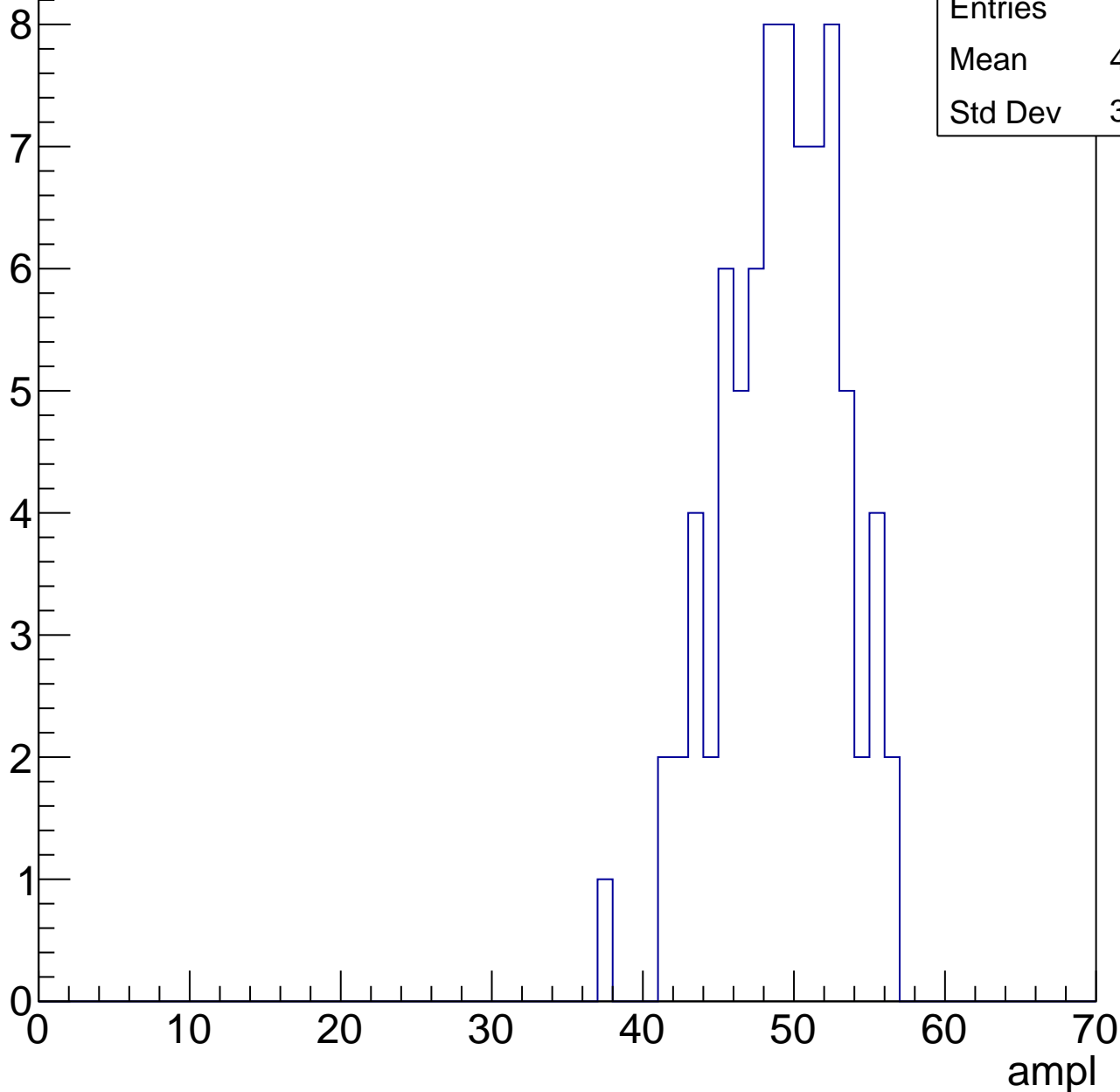


# B1L102S, U5-ch7, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	79
Mean	48.72
Std Dev	3.913

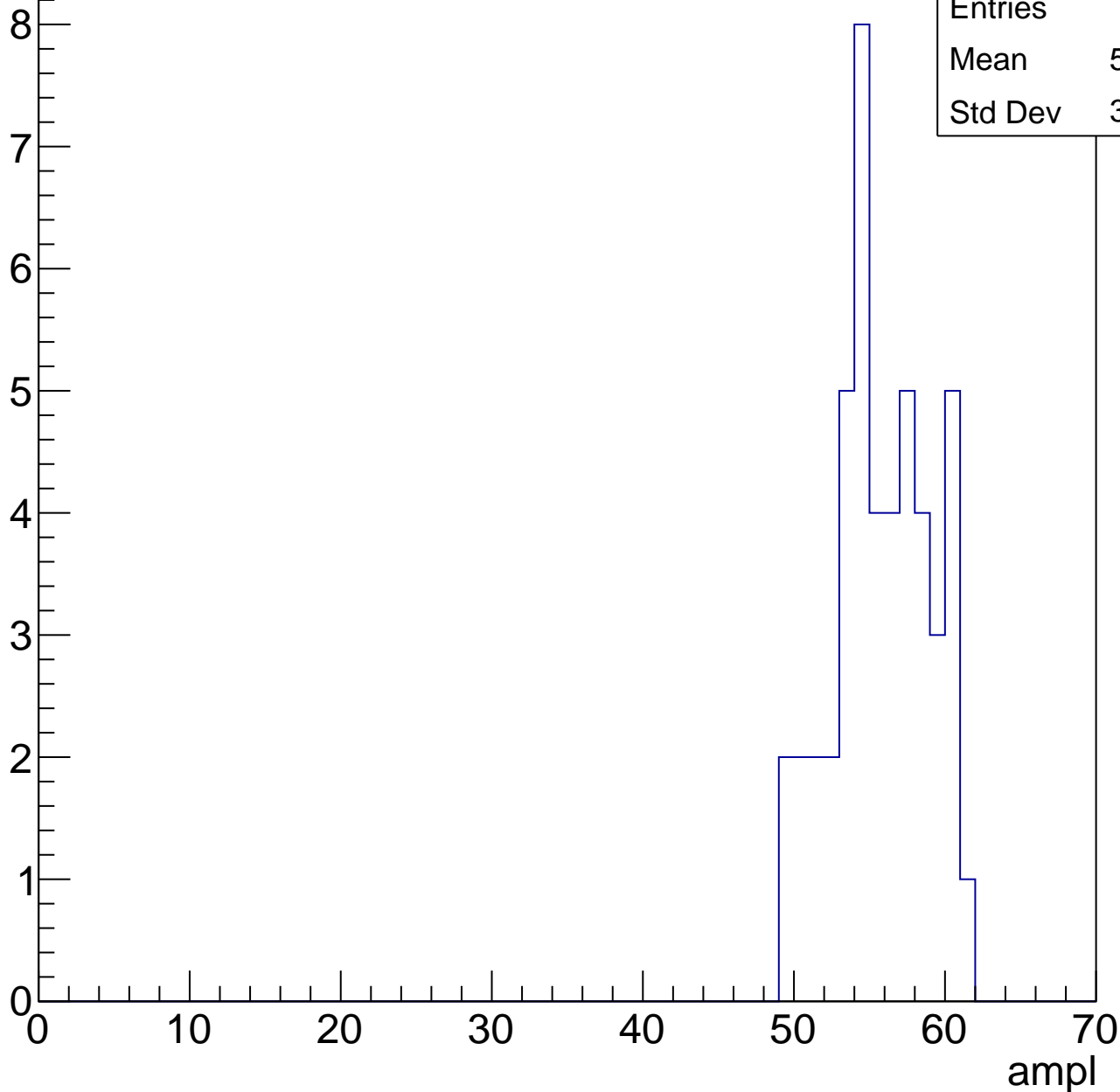


# B1L102S, U5-ch7, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

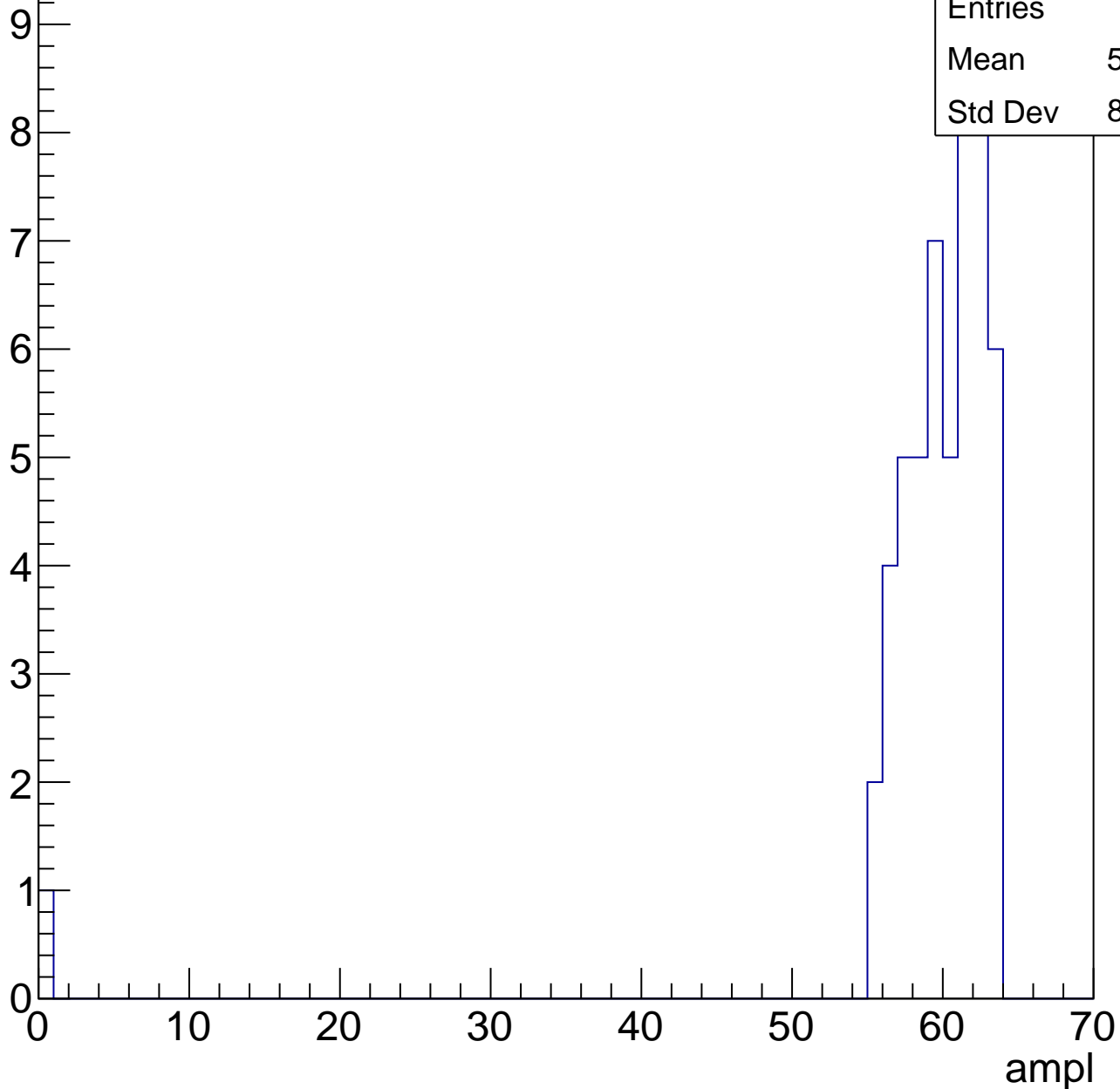
Entries	47
Mean	55.32
Std Dev	3.143



# B1L102S, U5-ch7, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

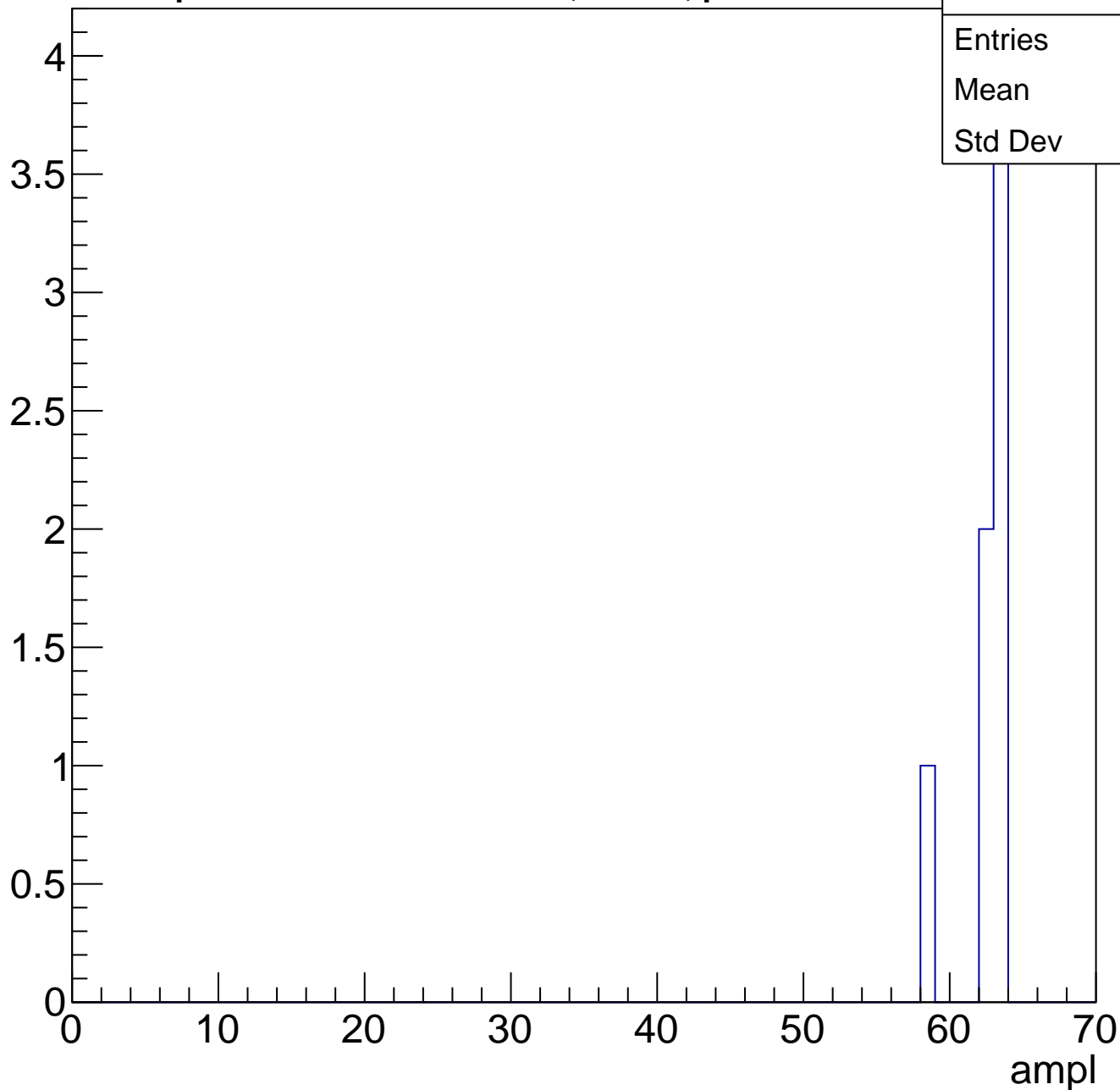
Entry



# B1L102S, U5-ch7, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U5-ch7, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	3
Mean	6.667
Std Dev	9.428

# B1L102S, U5-ch8, adc0

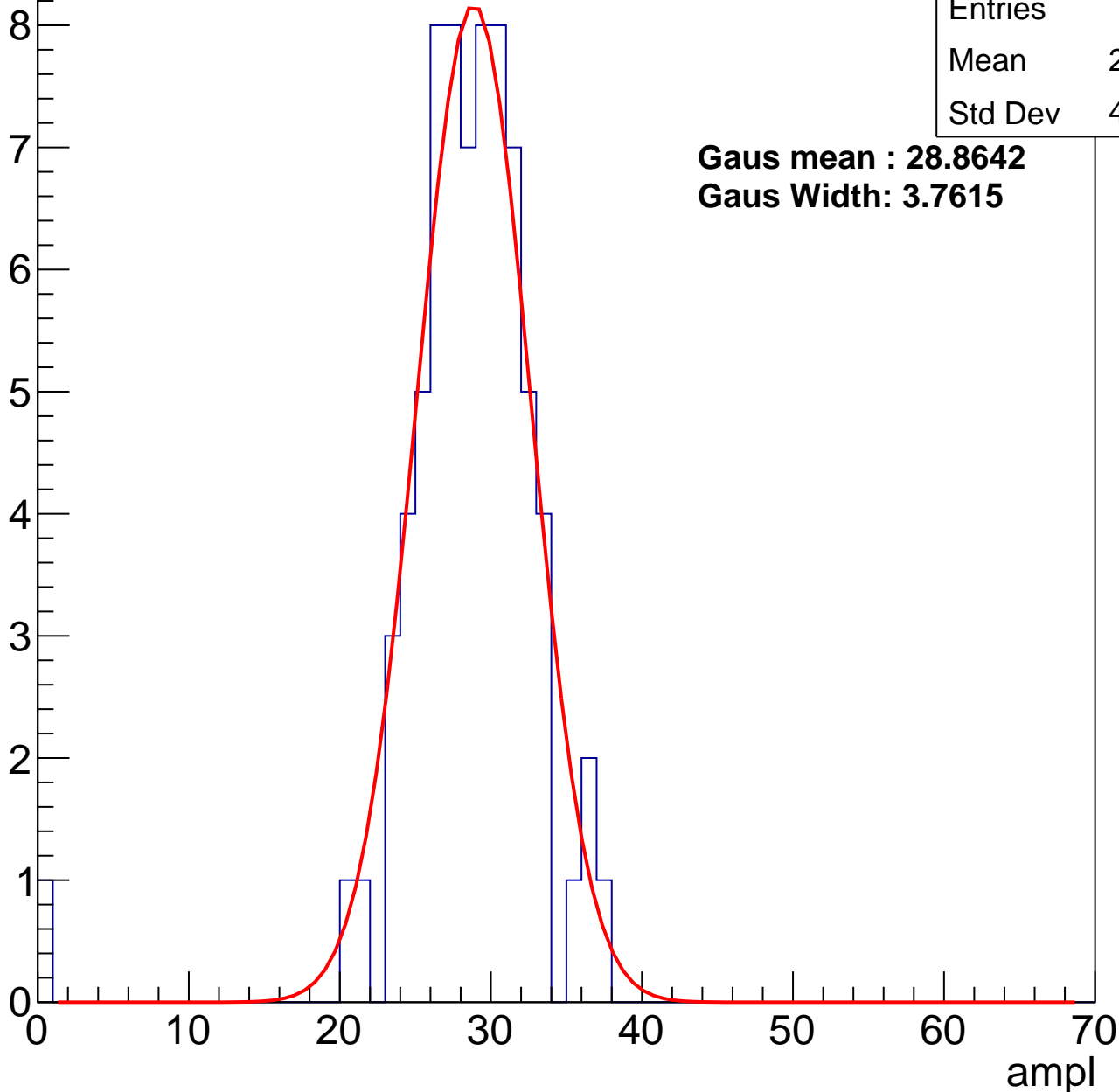
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	28.05
Std Dev	4.739

**Gaus mean : 28.8642**

**Gaus Width: 3.7615**



# B1L102S, U5-ch8, adc1

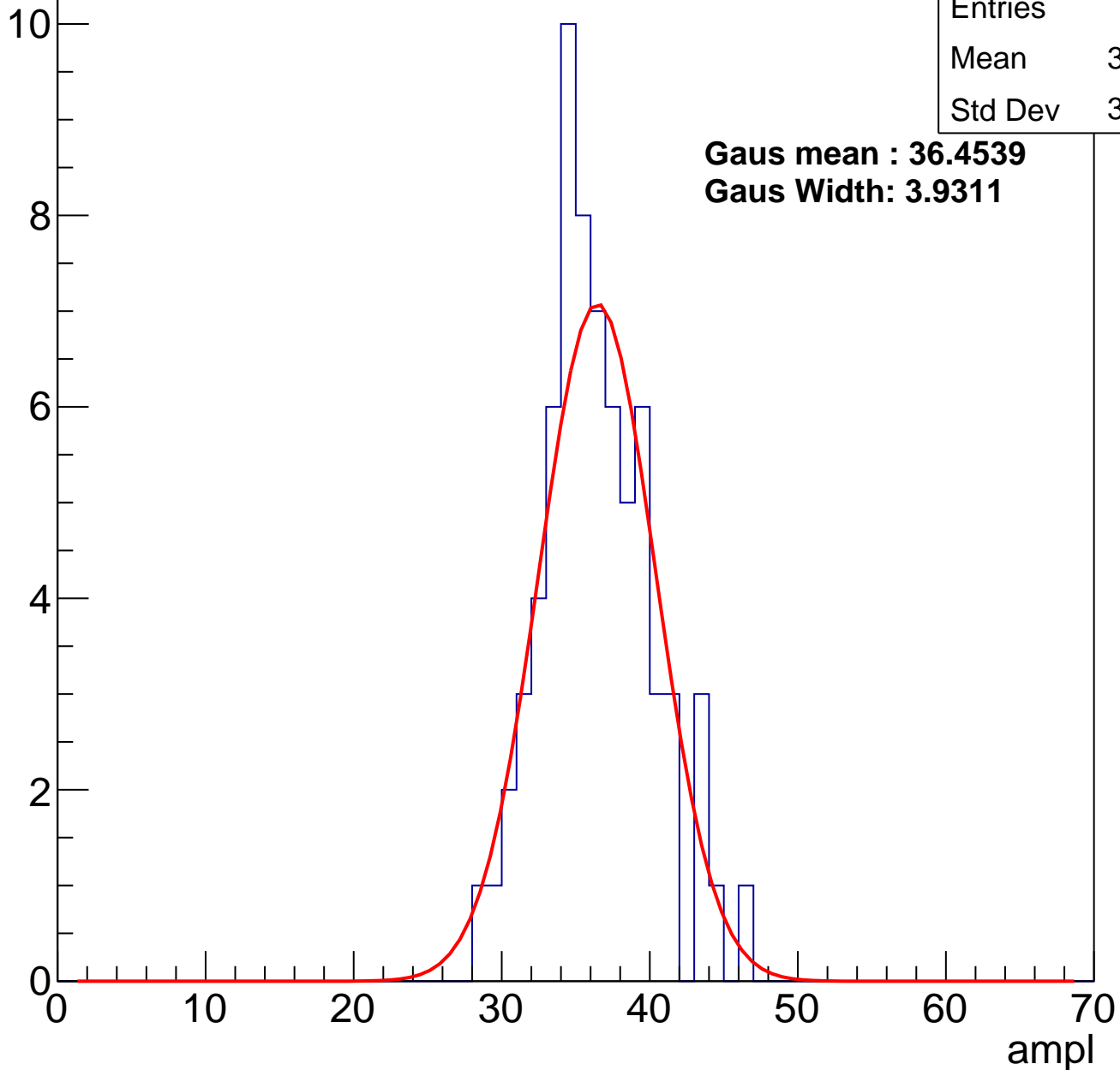
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	70
Mean	35.94
Std Dev	3.664

**Gaus mean : 36.4539**

**Gaus Width: 3.9311**

Entry



# B1L102S, U5-ch8, adc2

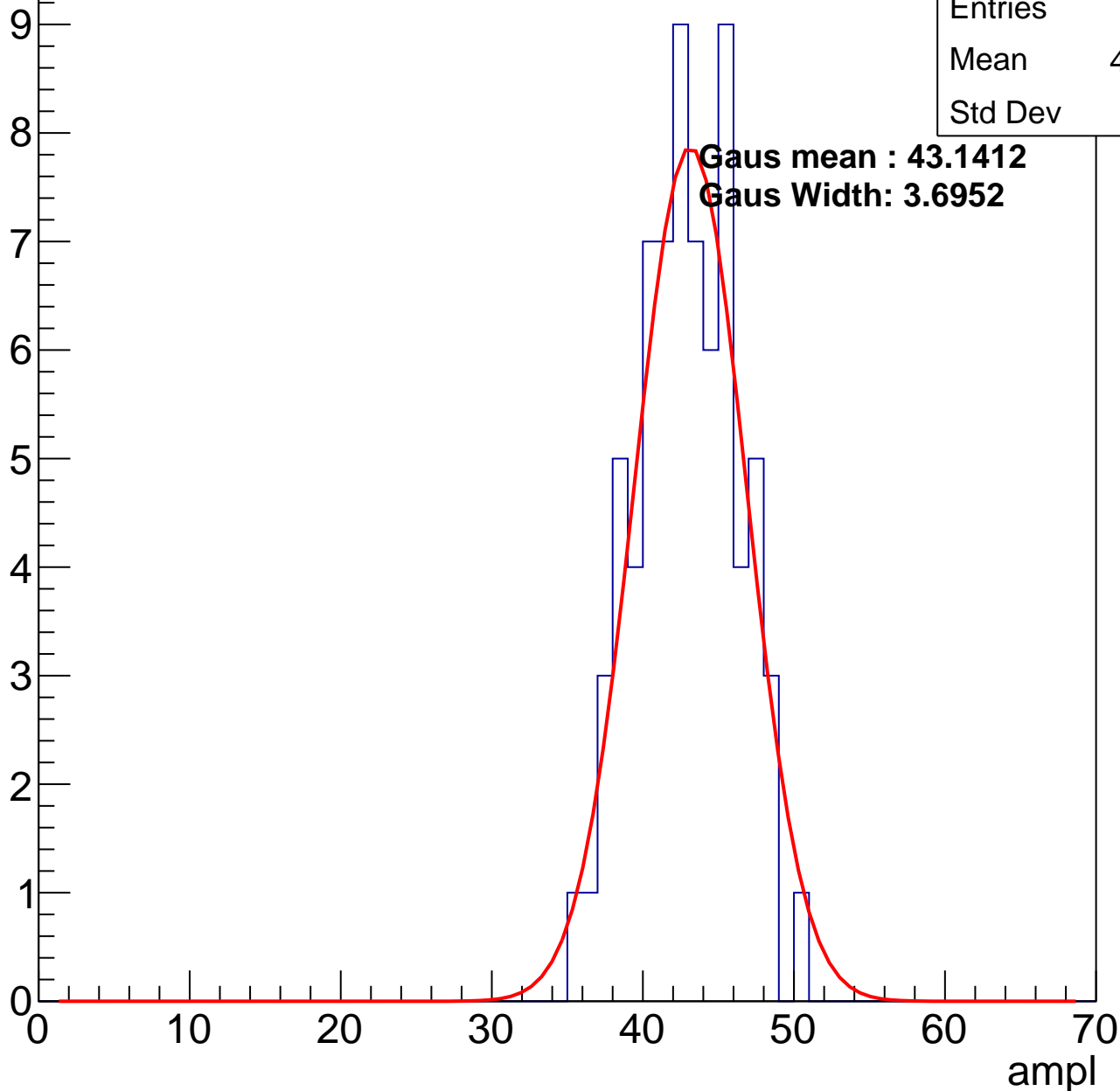
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	42.44
Std Dev	3.27

**Gaus mean : 43.1412**

**Gaus Width: 3.6952**

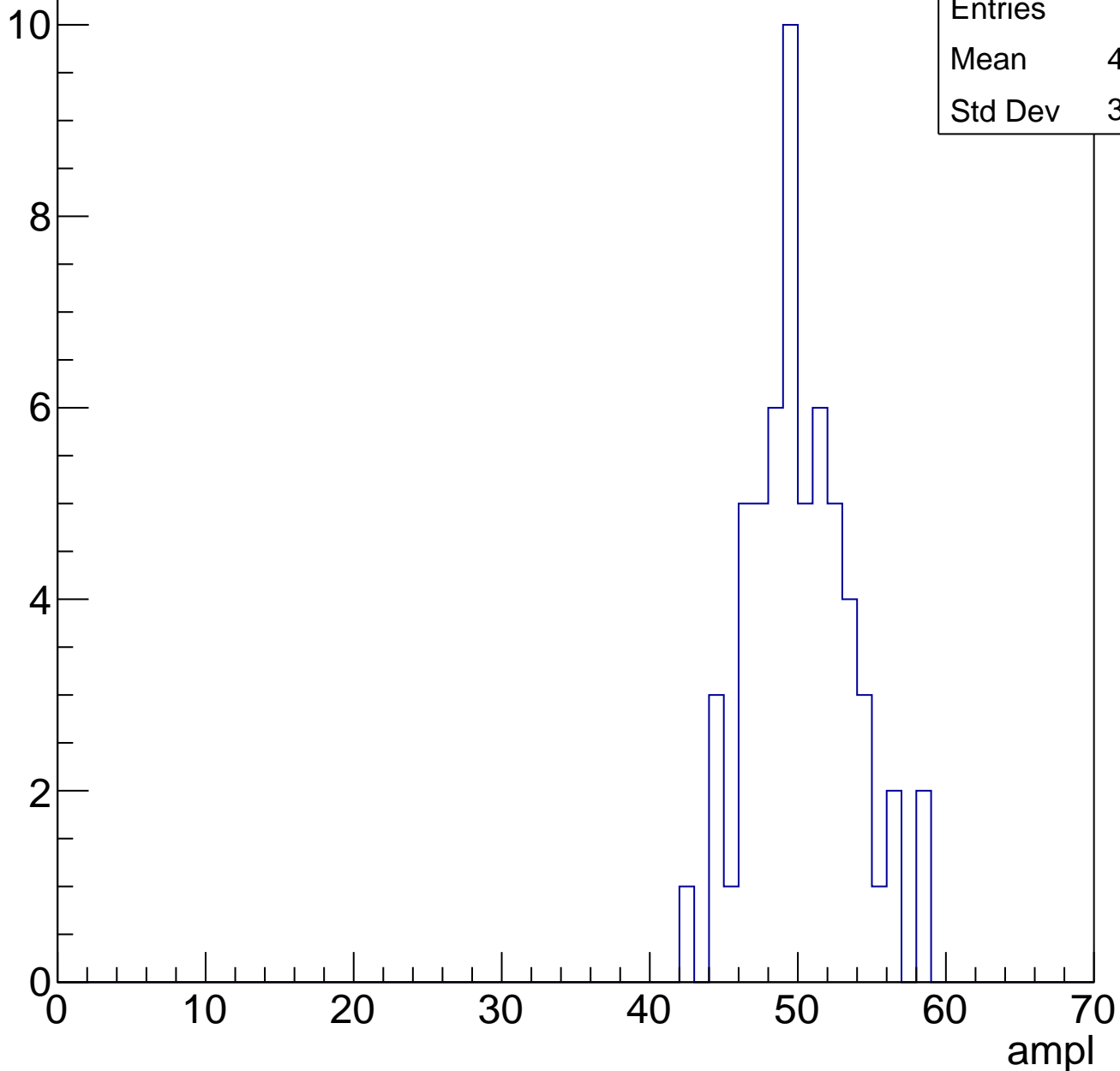


# B1L102S, U5-ch8, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	59
Mean	49.75
Std Dev	3.413

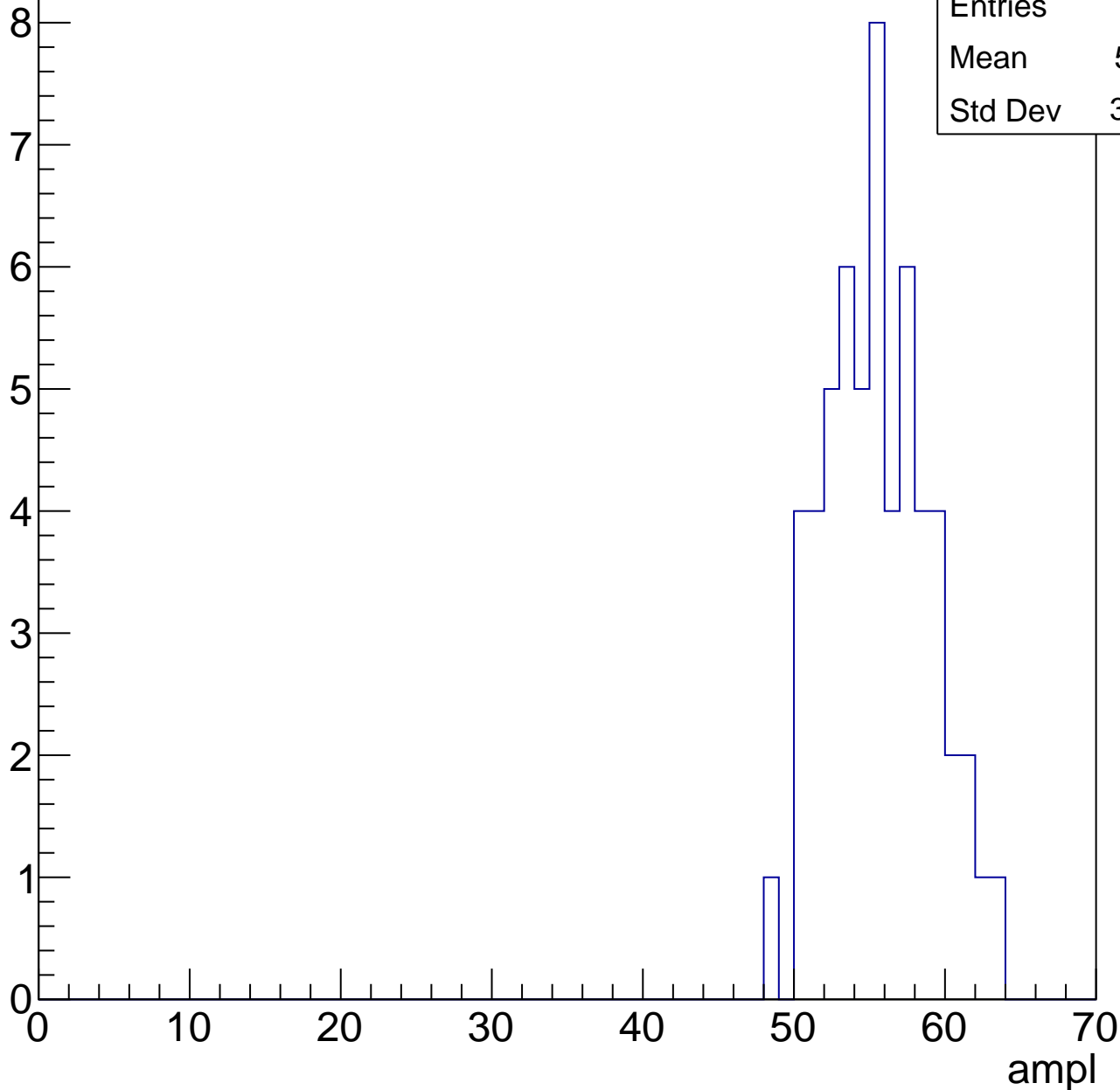
Entry



# B1L102S, U5-ch8, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	57
Mean	55.11
Std Dev	3.375

# B1L102S, U5-ch8, adc5

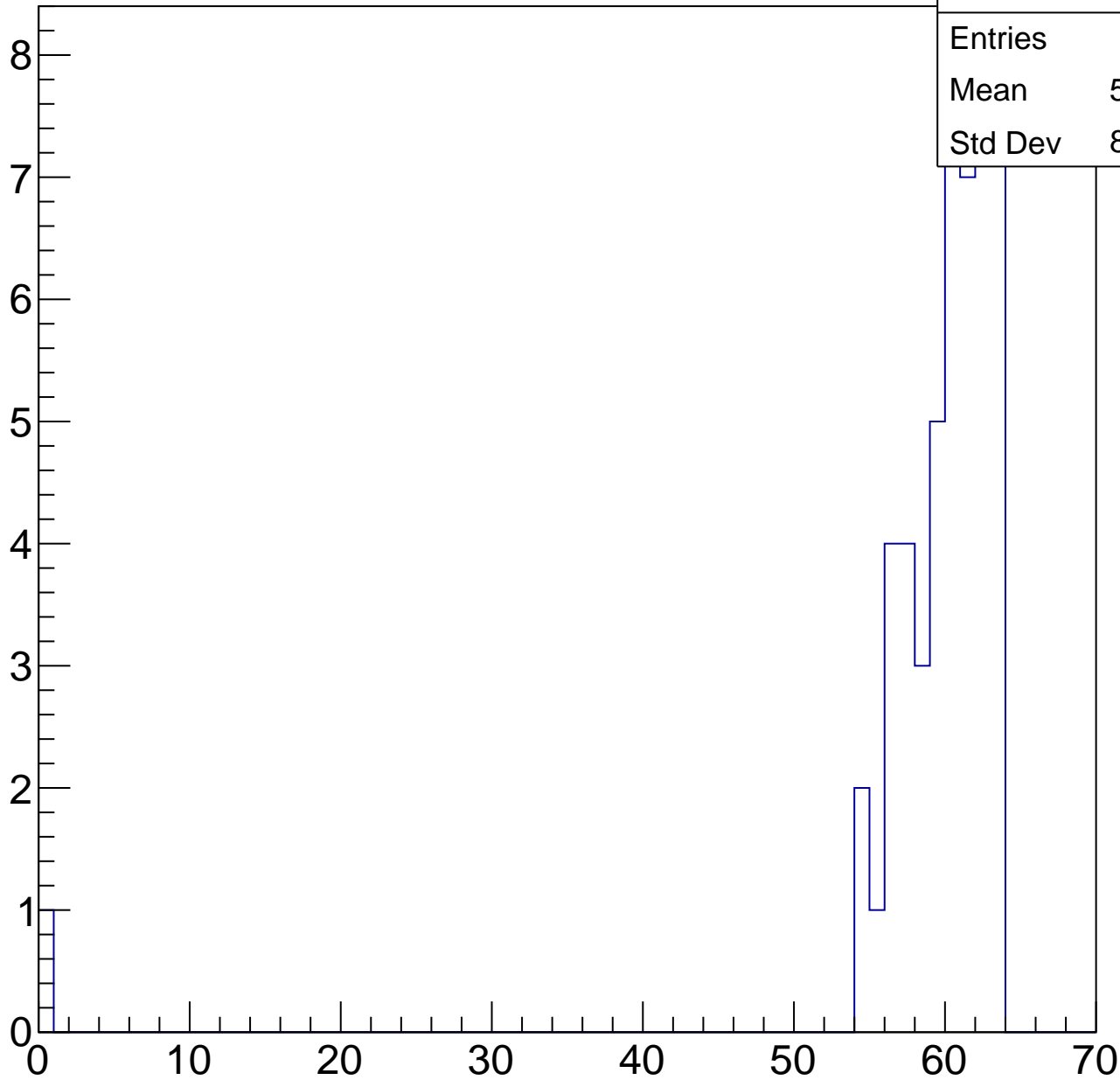
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	51
Mean	58.65
Std Dev	8.668

ampl



# B1L102S, U5-ch8, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	60.6
Std Dev	1.855

ampl

0 10 20 30 40 50 60 70



# B1L102S, U5-ch8, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U5-ch9, adc0

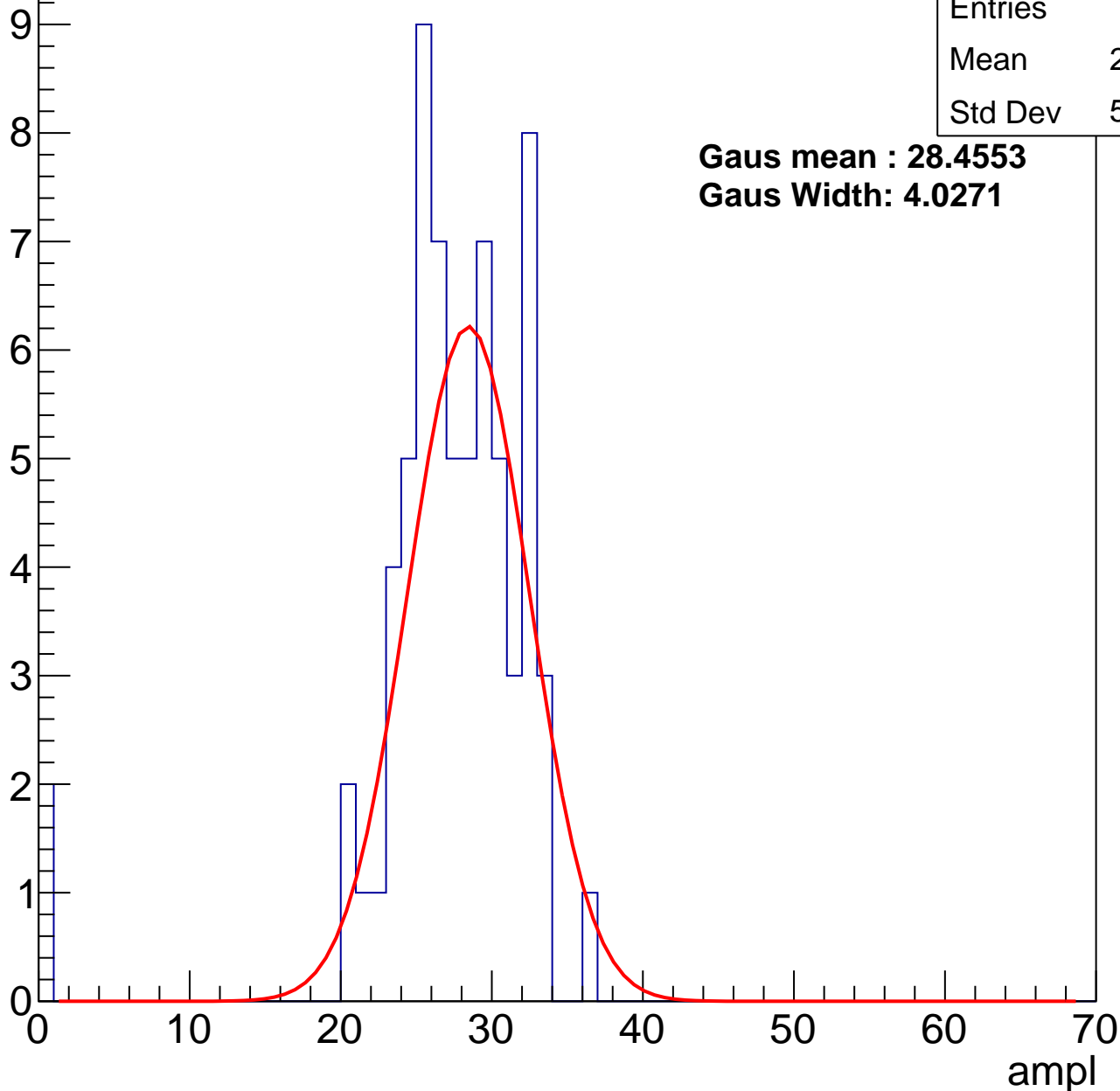
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	26.68
Std Dev	5.786

**Gaus mean : 28.4553**

**Gaus Width: 4.0271**



# B1L102S, U5-ch9, adc1

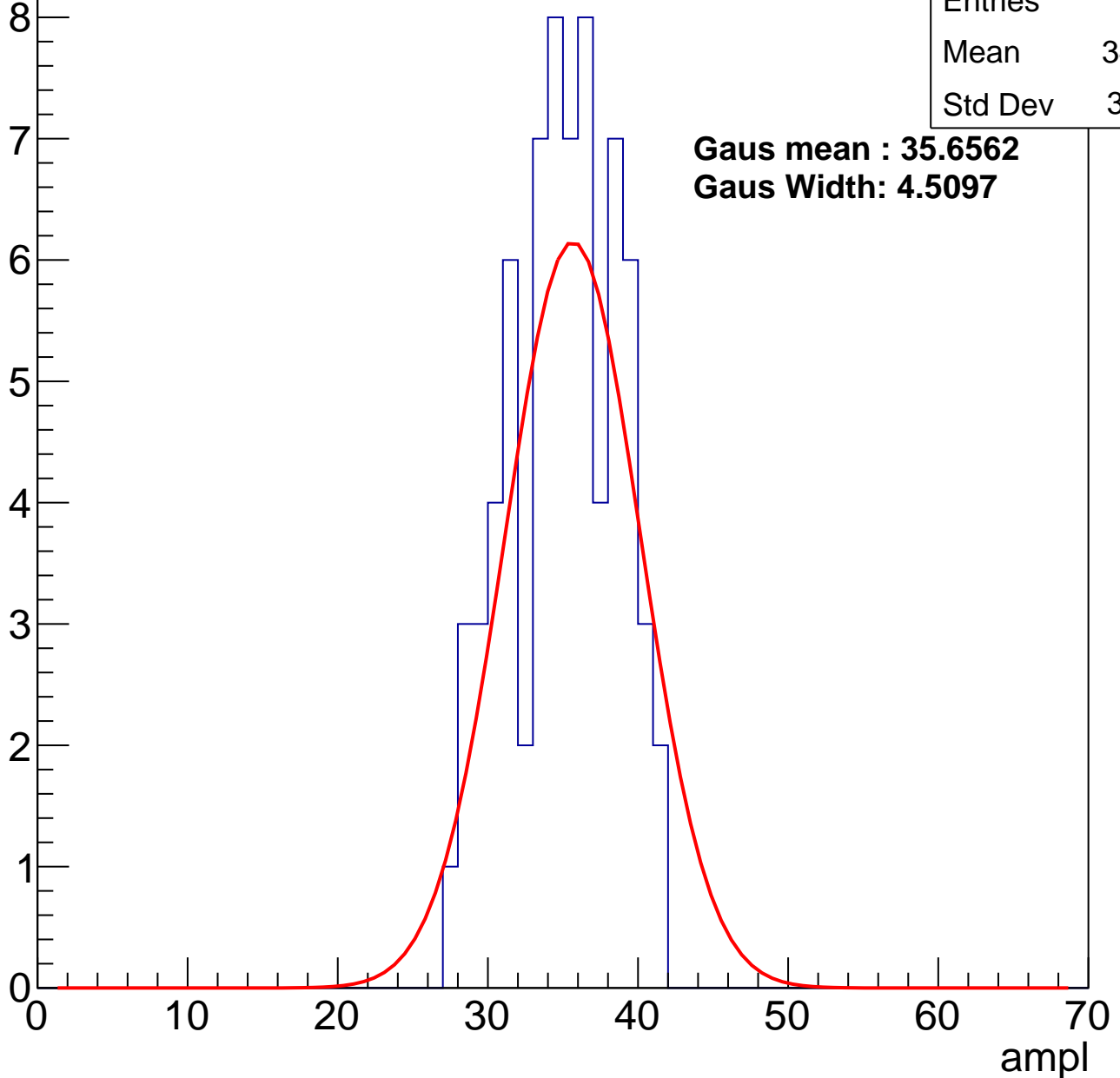
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	34.56
Std Dev	3.531

**Gaus mean : 35.6562**

**Gaus Width: 4.5097**



# B1L102S, U5-ch9, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	60
Mean	41.08
Std Dev	3.513

**Gaus mean : 41.9329**

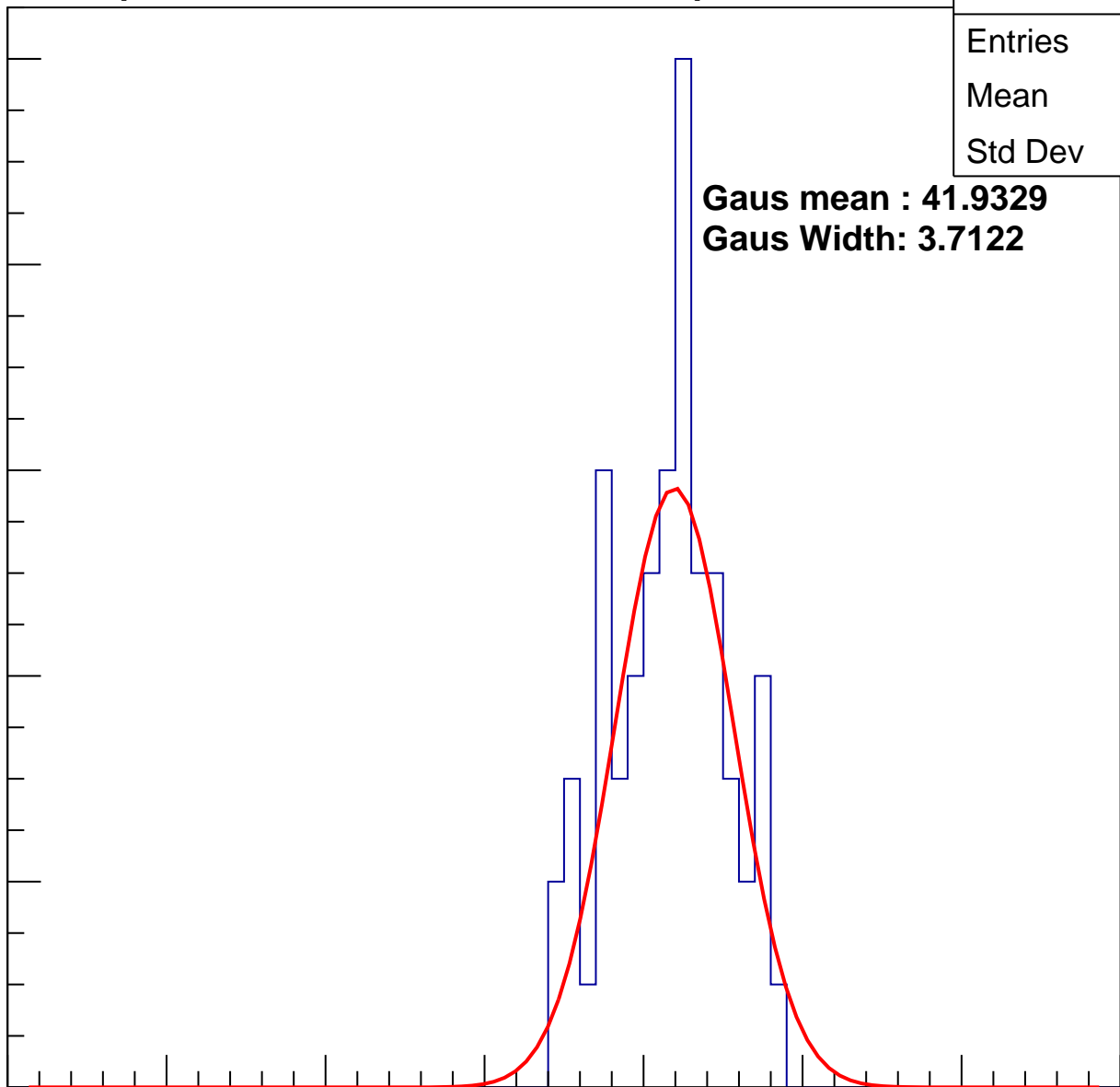
**Gaus Width: 3.7122**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

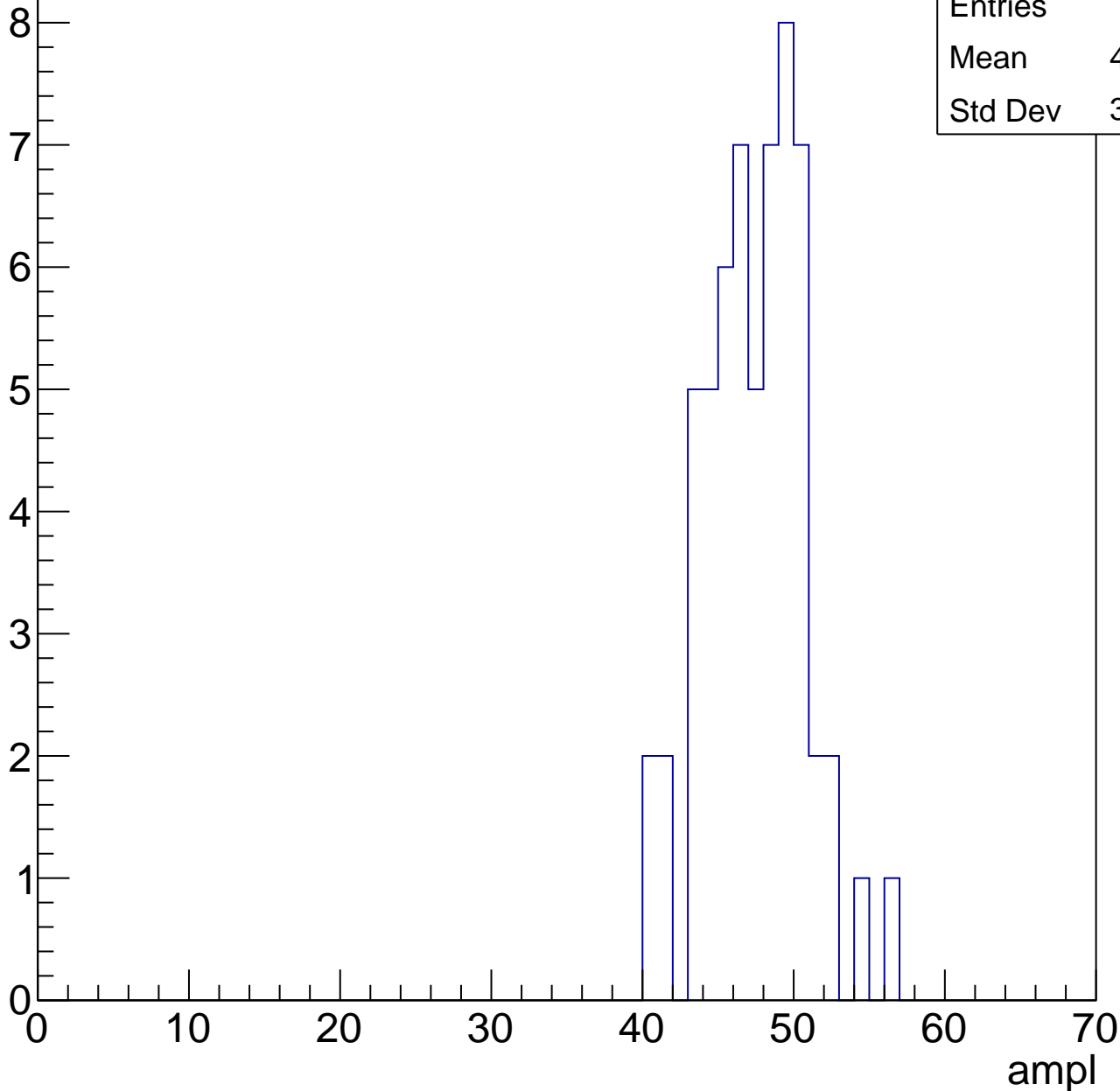


# B1L102S, U5-ch9, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

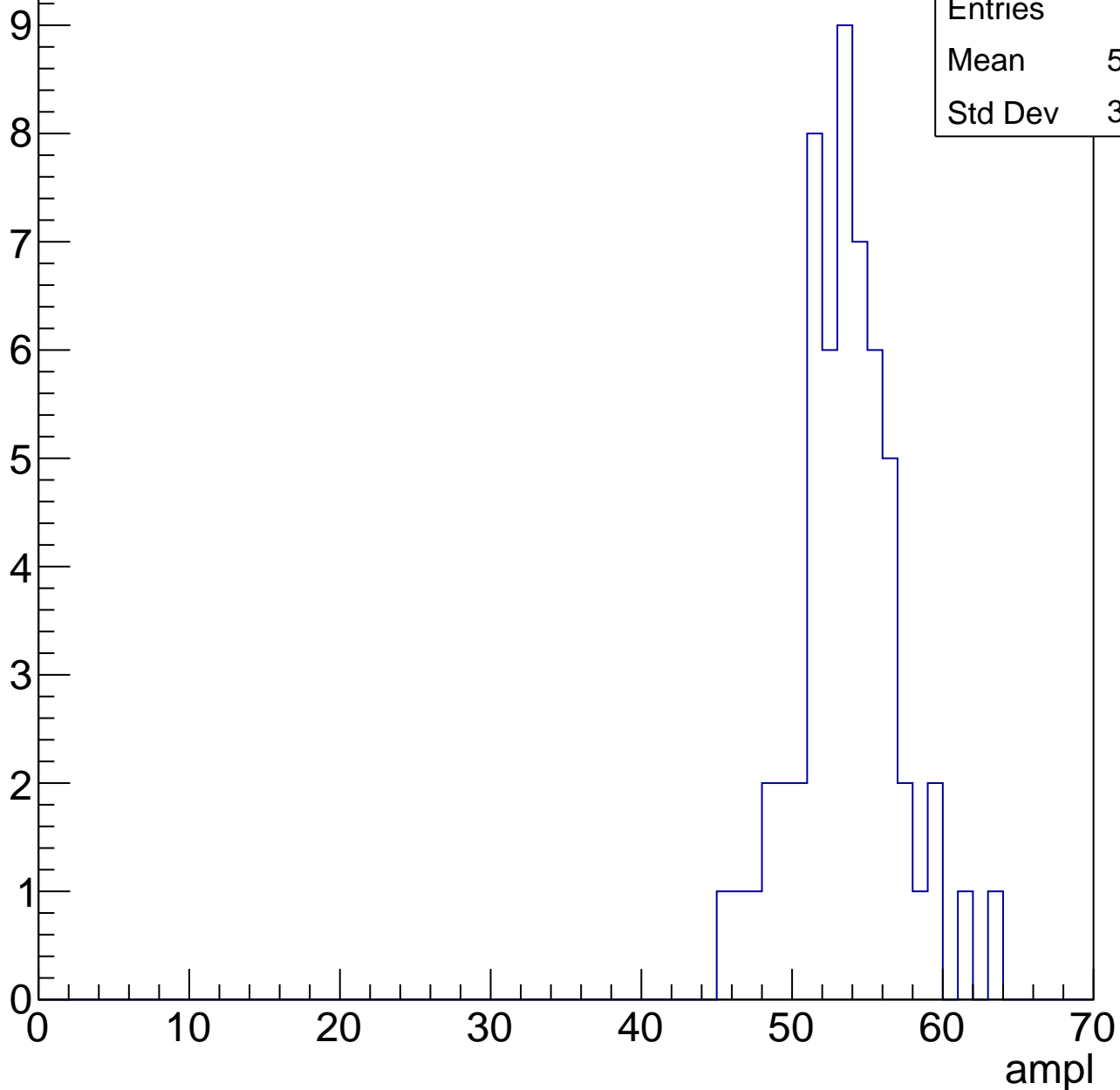
Entries	60
Mean	46.97
Std Dev	3.266



# B1L102S, U5-ch9, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	57
Mean	53.18
Std Dev	3.388

# B1L102S, U5-ch9, adc5

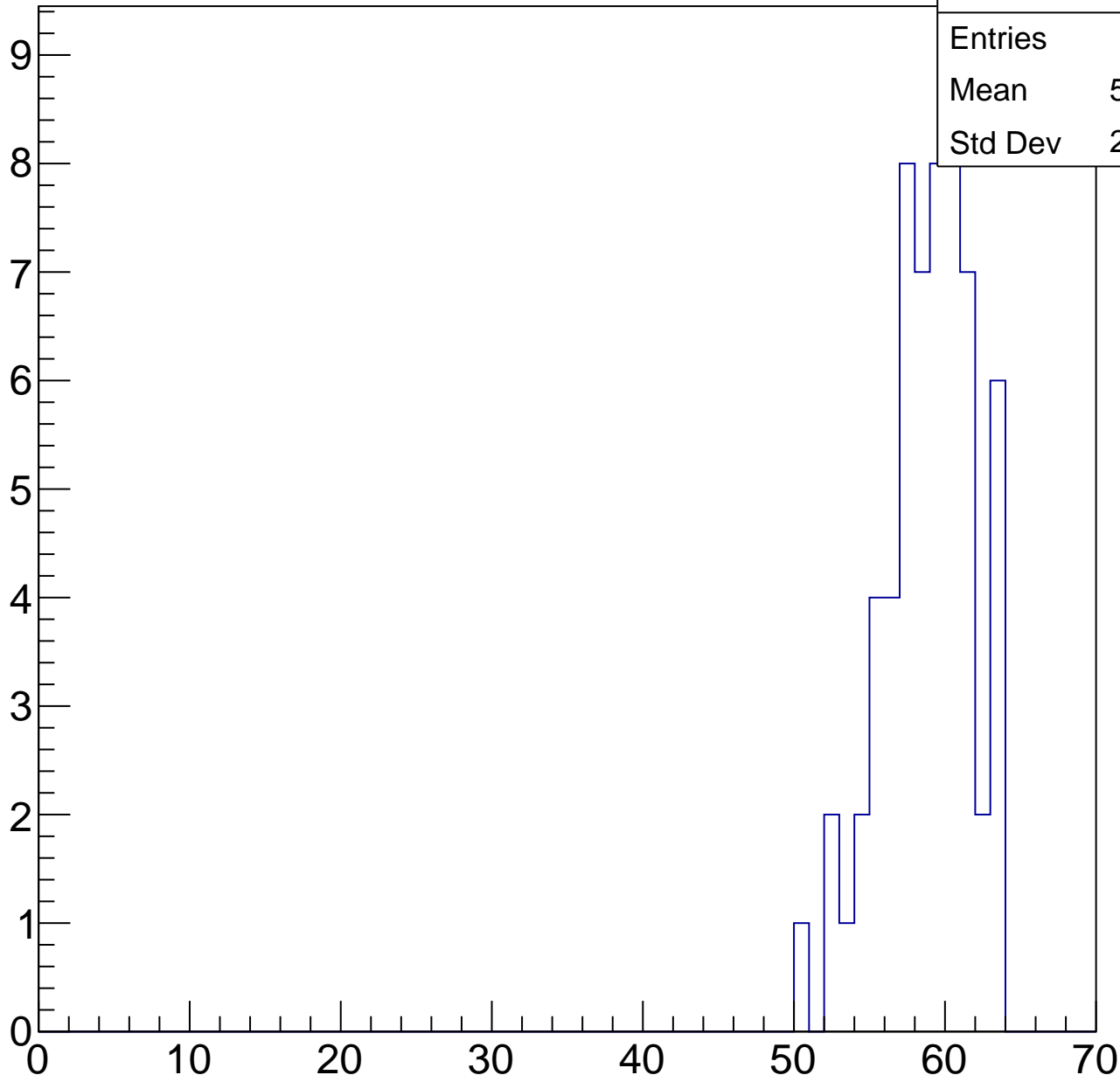
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	61
Mean	58.39
Std Dev	2.955

ampl

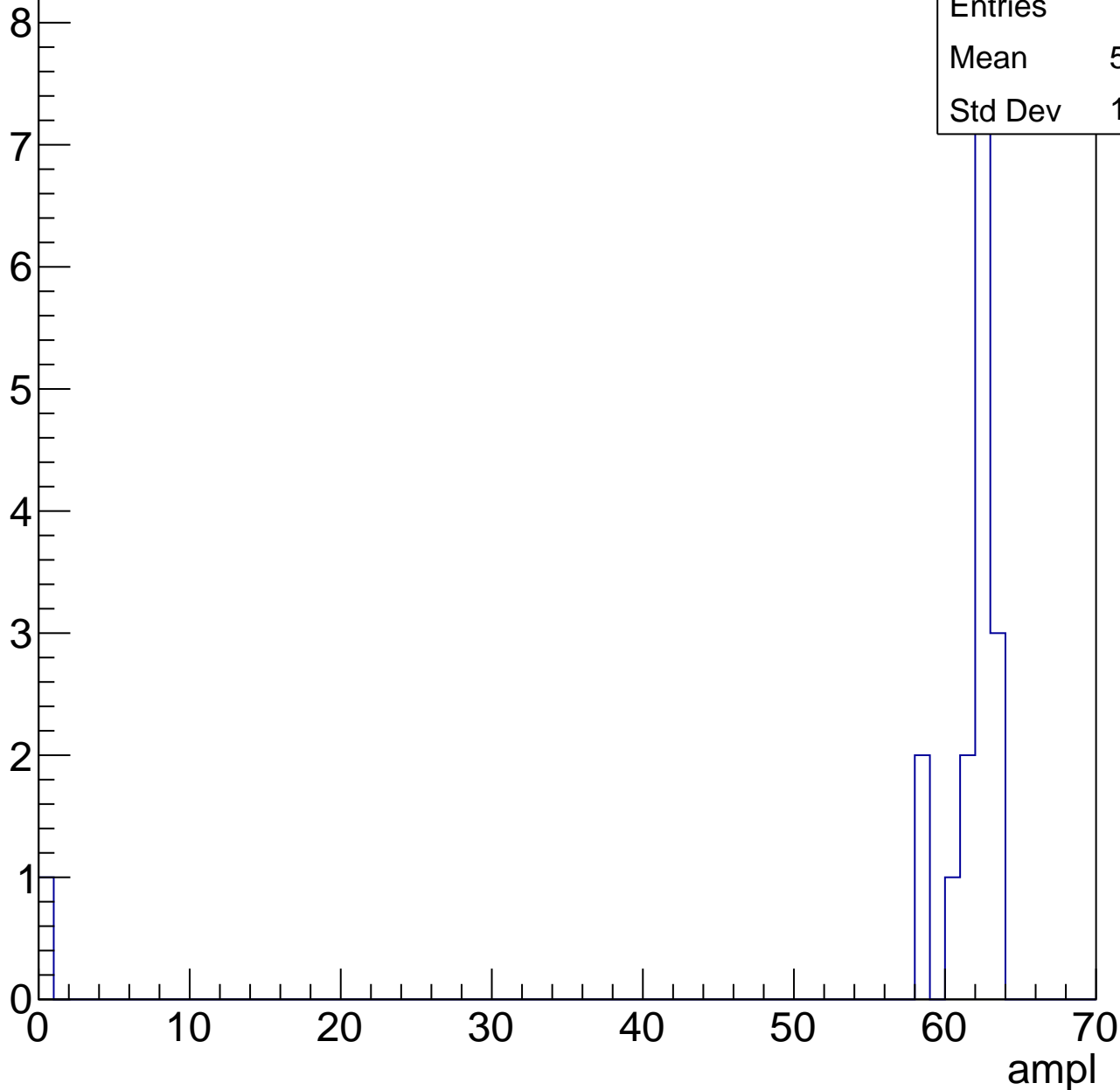


# B1L102S, U5-ch9, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	17
Mean	57.82
Std Dev	14.53





# B1L102S, U5-ch9, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U5-ch10, adc0

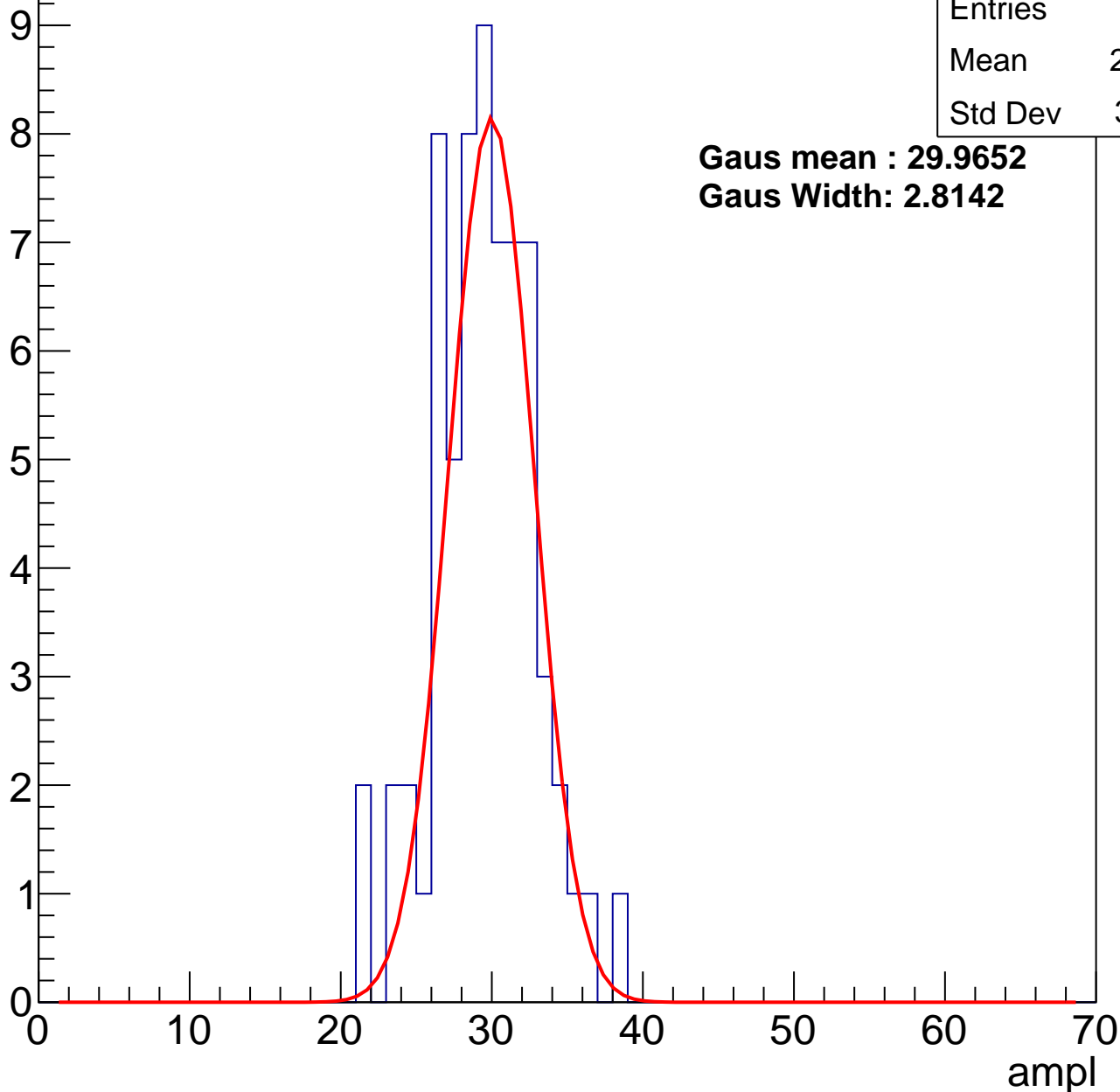
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	29.03
Std Dev	3.321

**Gaus mean : 29.9652**

**Gaus Width: 2.8142**



# B1L102S, U5-ch10, adc1

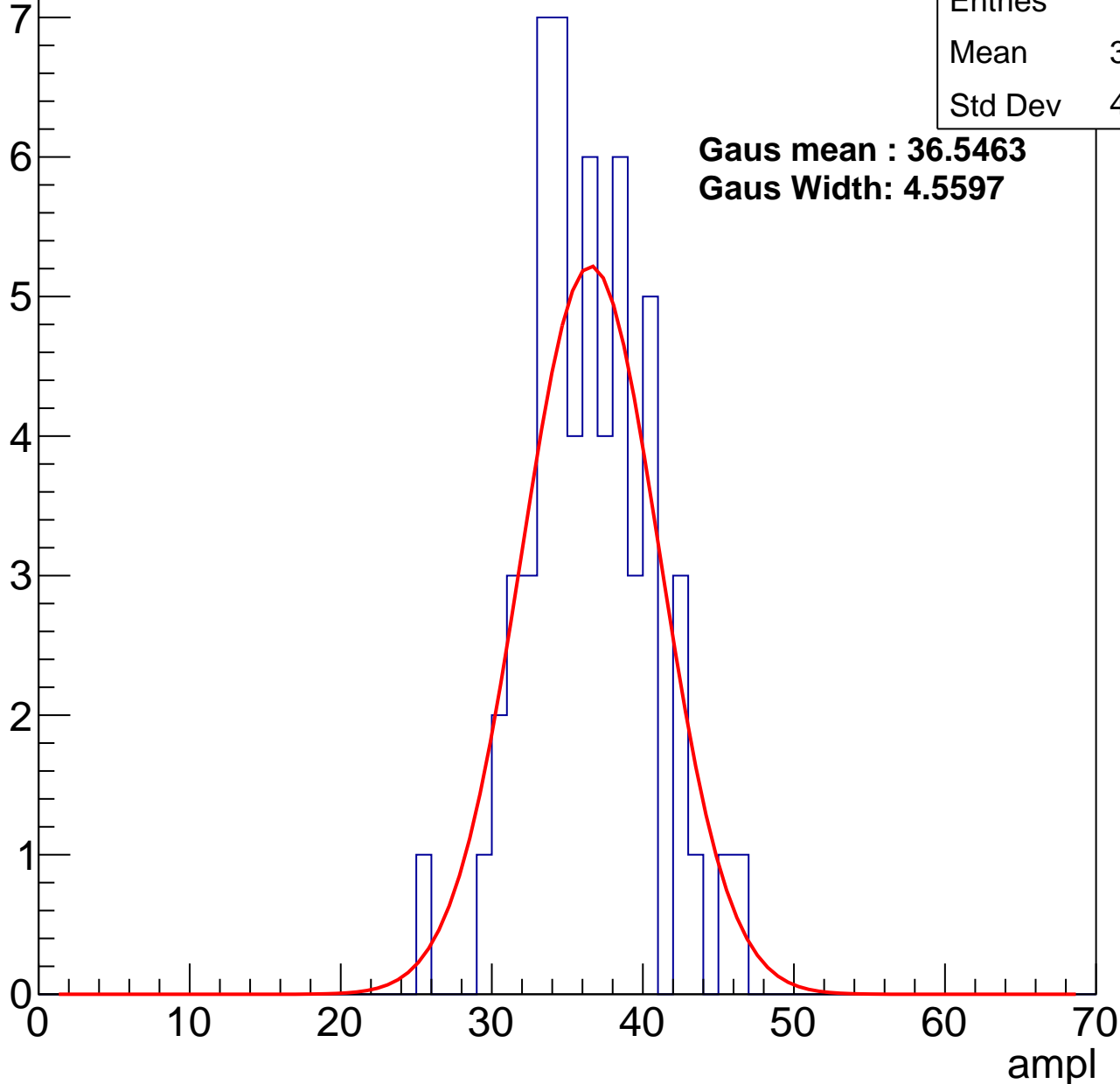
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	35.88
Std Dev	4.009

**Gaus mean : 36.5463**

**Gaus Width: 4.5597**



# B1L102S, U5-ch10, adc2

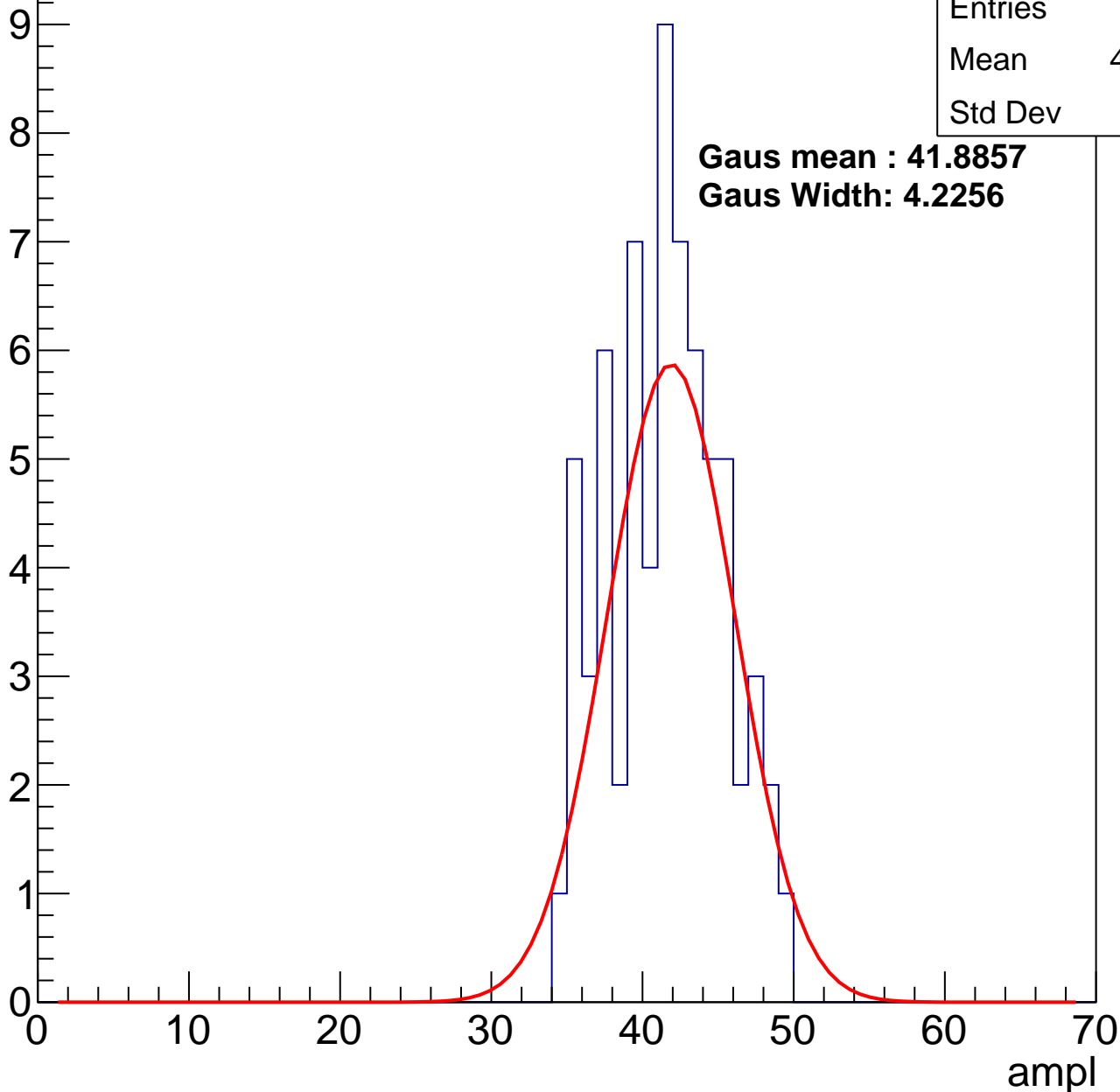
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	41.06
Std Dev	3.69

**Gaus mean : 41.8857**

**Gaus Width: 4.2256**

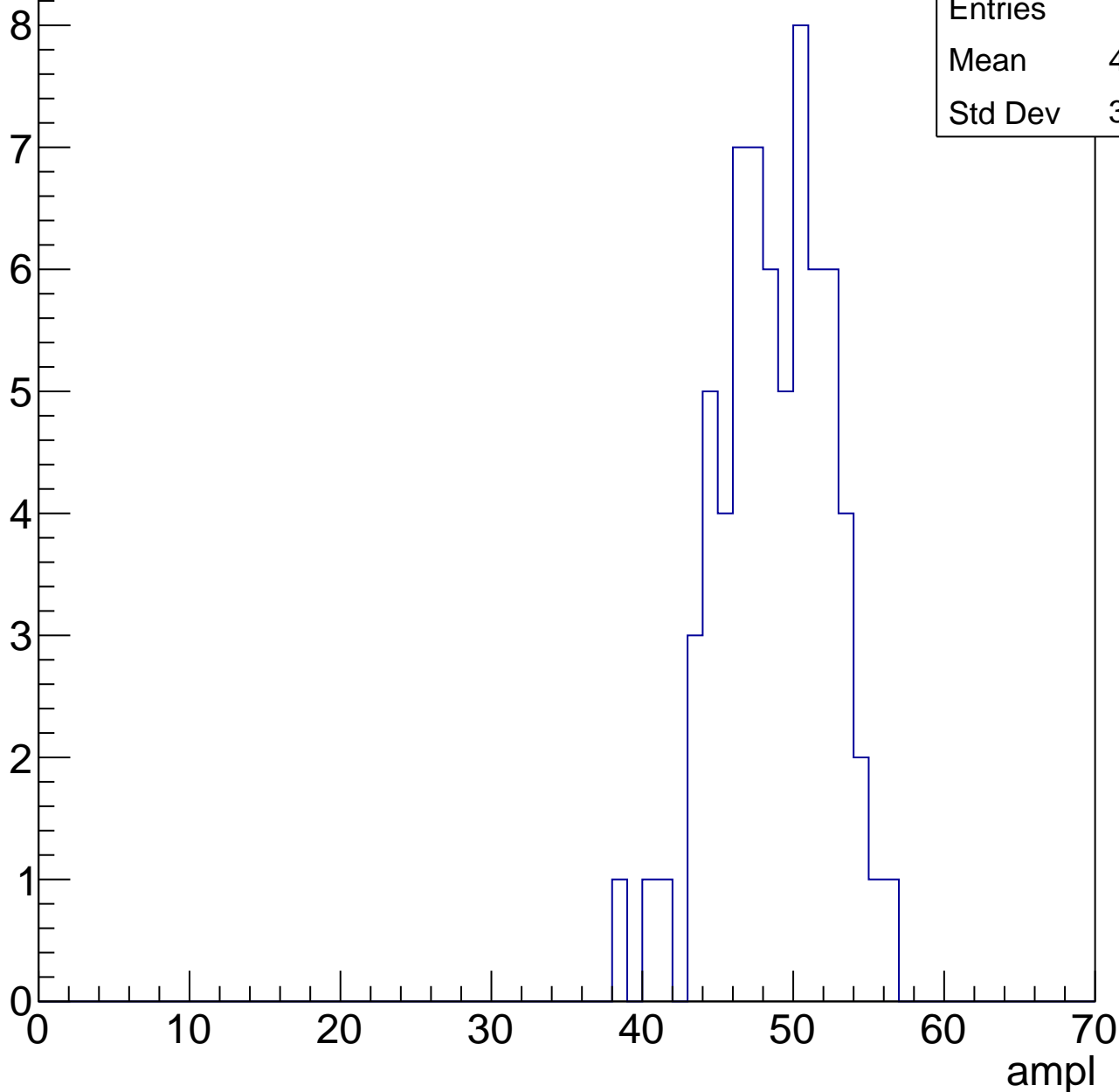


# B1L102S, U5-ch10, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	48.25
Std Dev	3.652

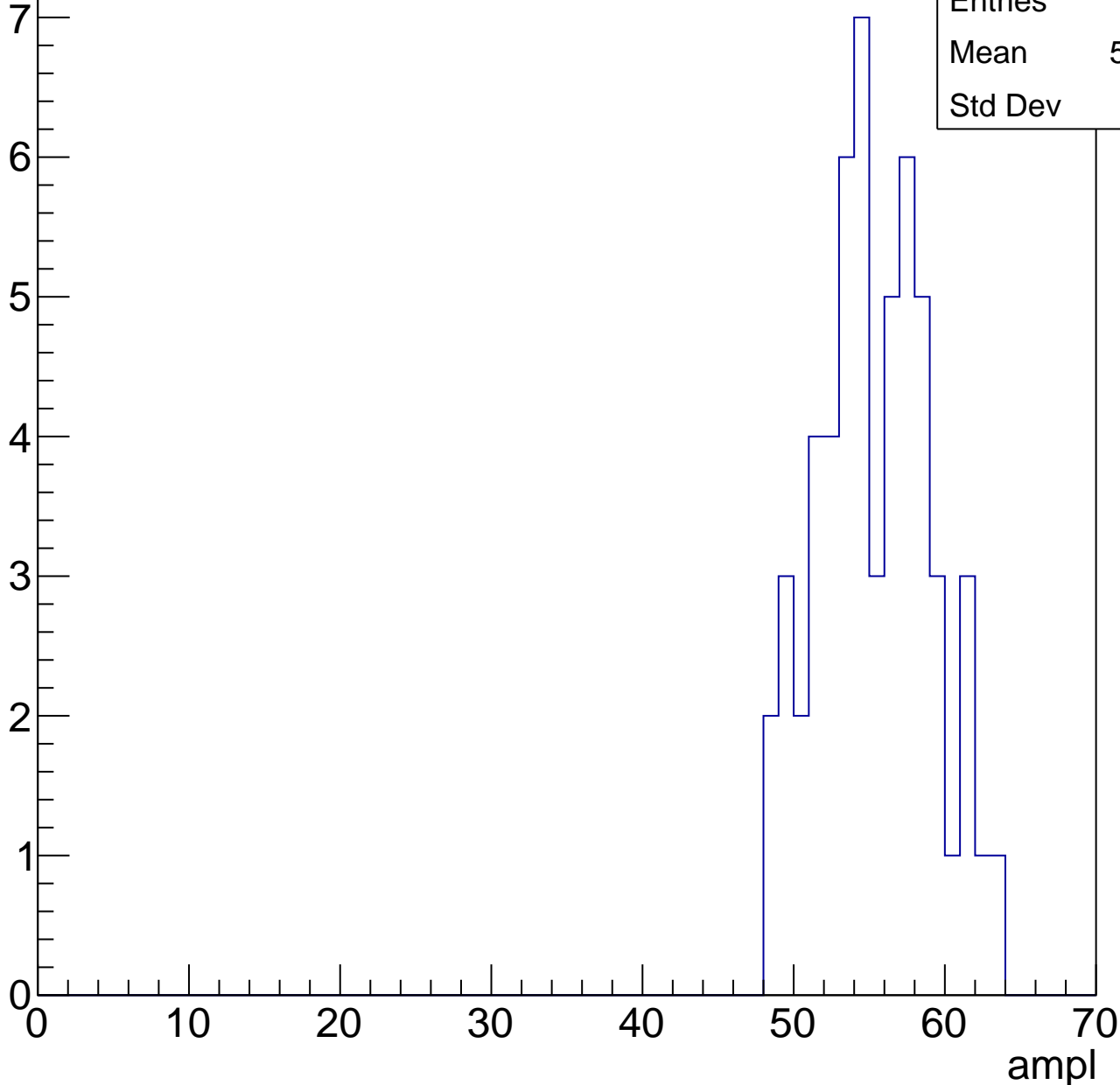


# B1L102S, U5-ch10, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	54.88
Std Dev	3.67

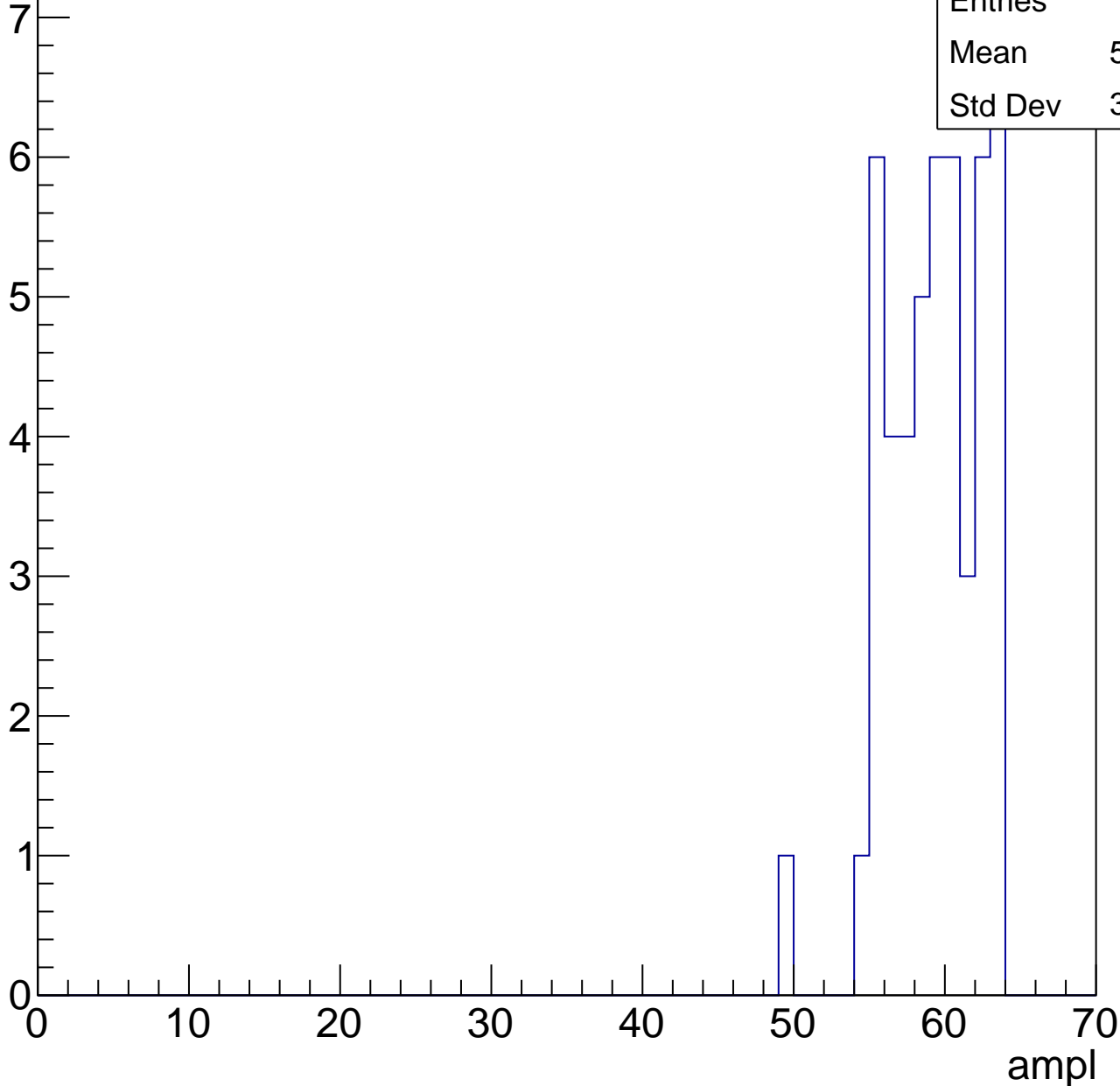


# B1L102S, U5-ch10, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

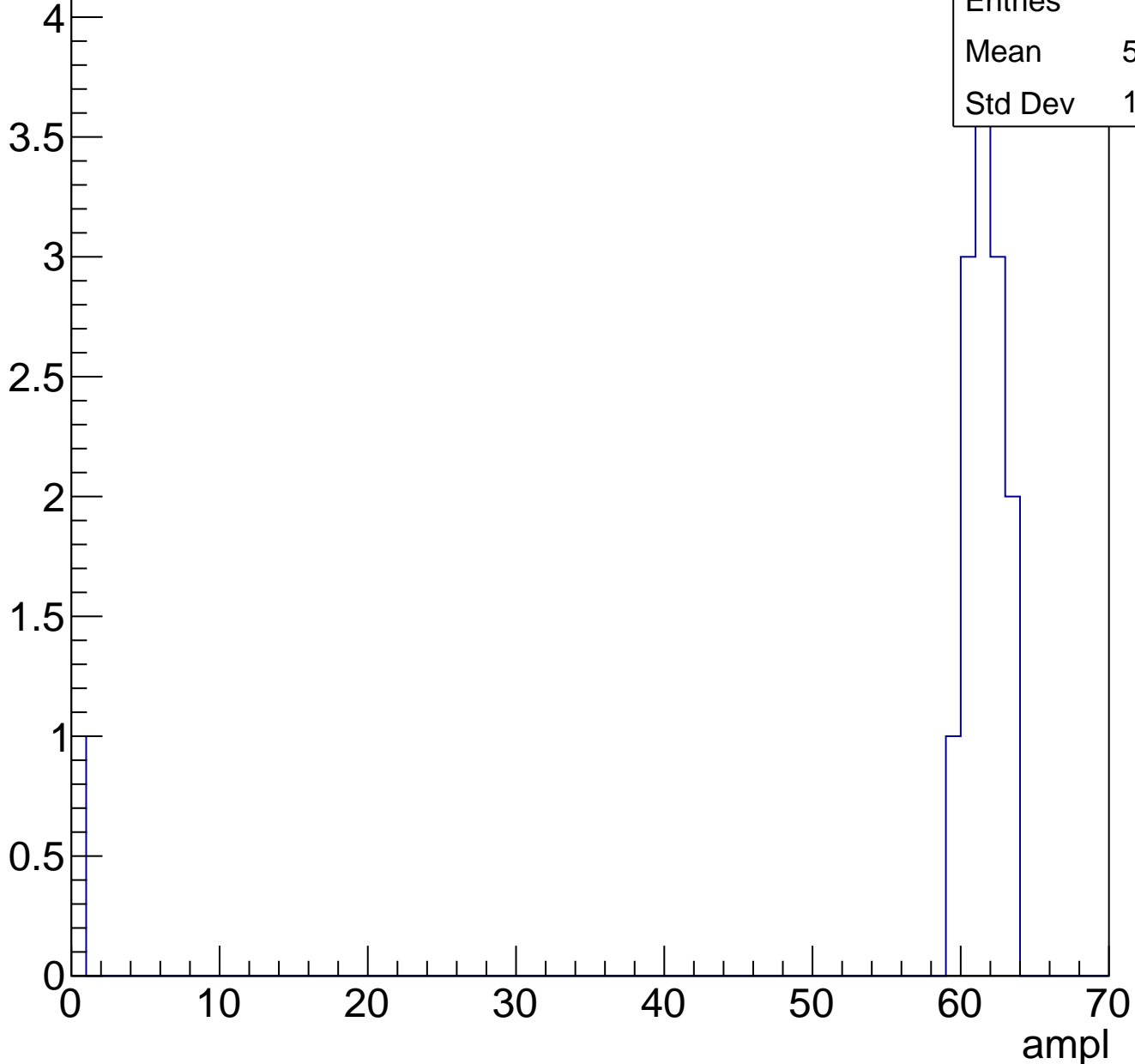
Entries	49
Mean	58.88
Std Dev	3.068



# B1L102S, U5-ch10, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U5-ch10, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U5-ch11, adc0

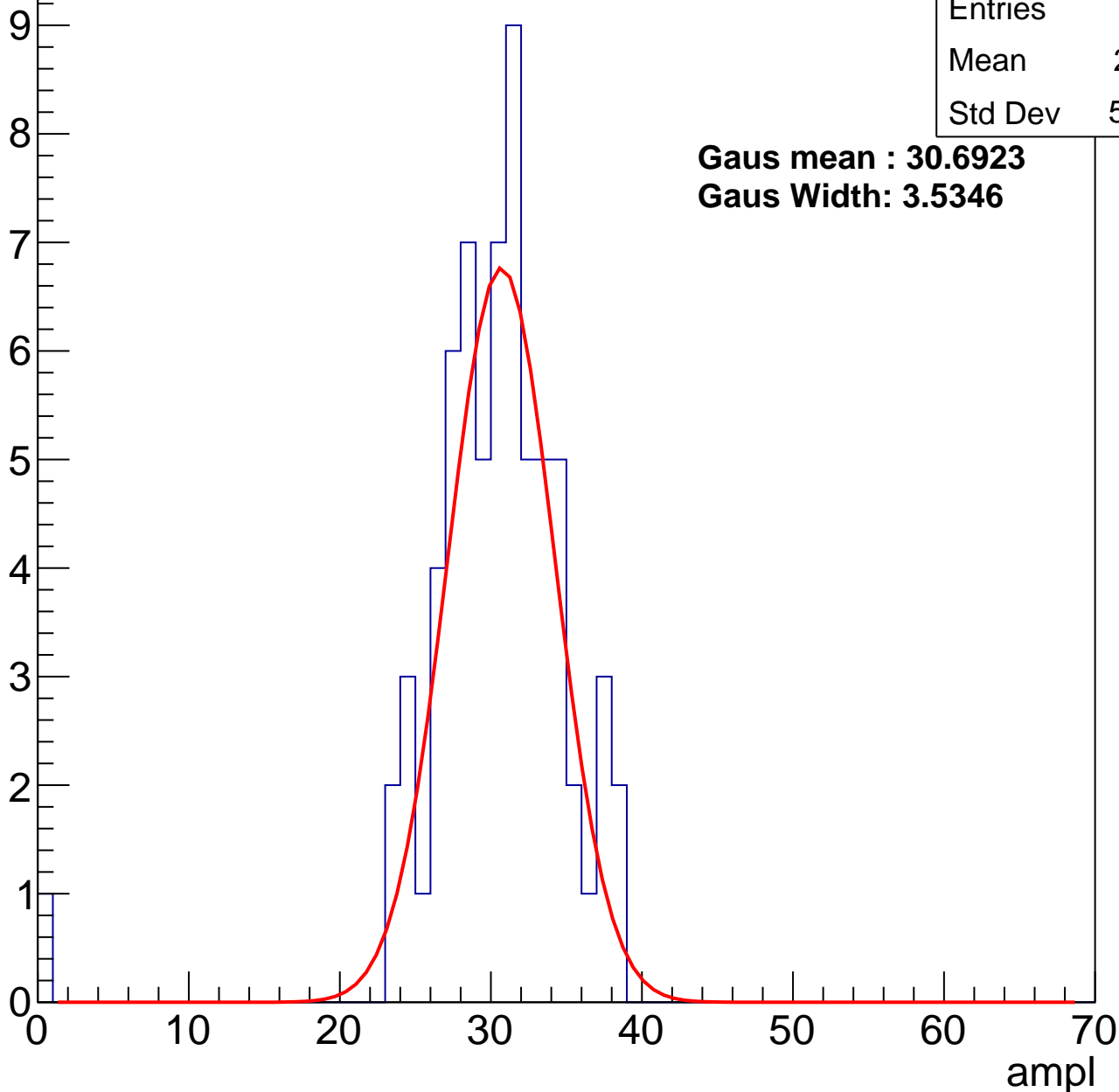
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	29.81
Std Dev	5.137

**Gaus mean : 30.6923**

**Gaus Width: 3.5346**



# B1L102S, U5-ch11, adc1

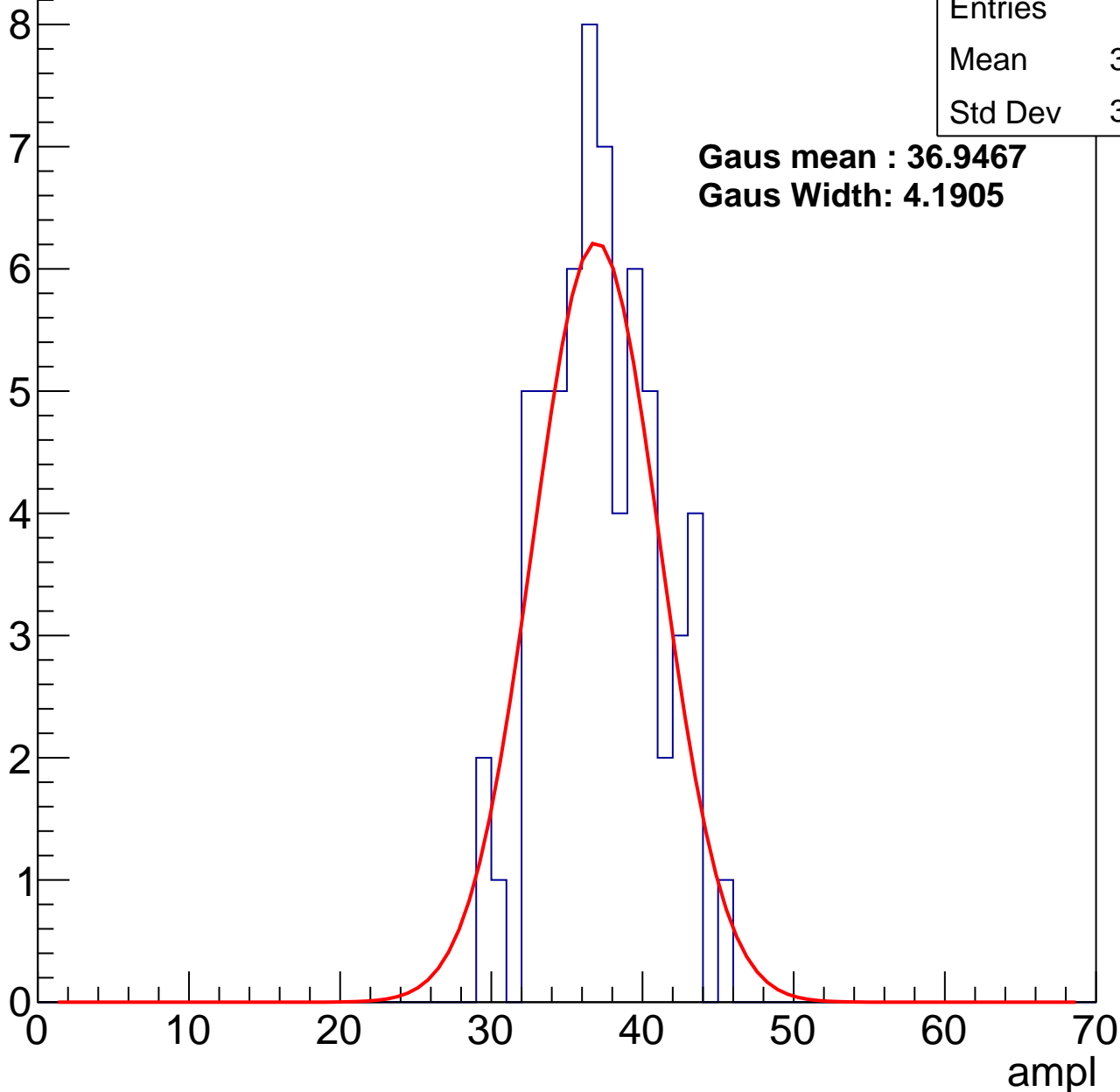
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	36.73
Std Dev	3.628

**Gaus mean : 36.9467**

**Gaus Width: 4.1905**



# B1L102S, U5-ch11, adc2

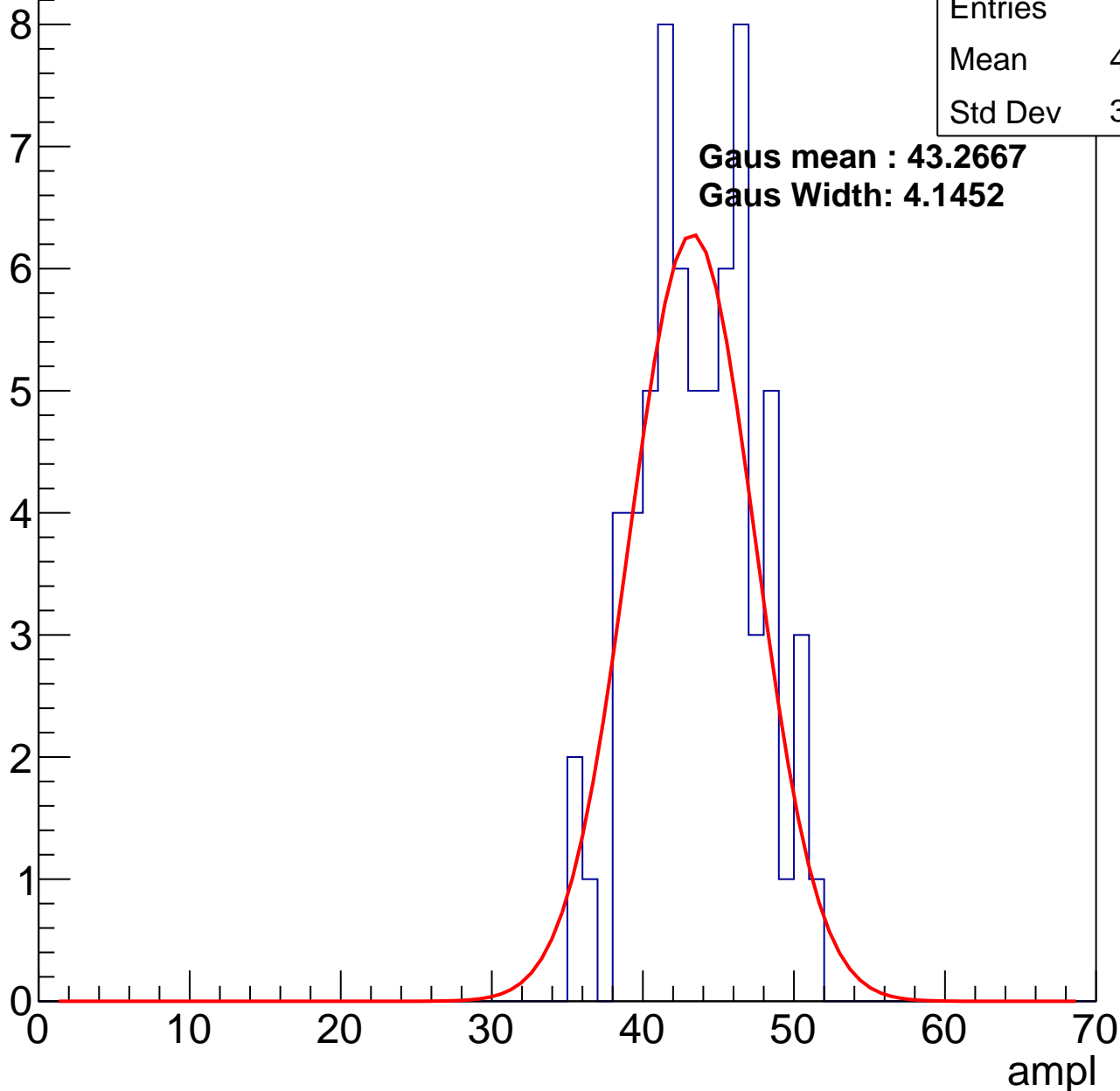
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	43.25
Std Dev	3.747

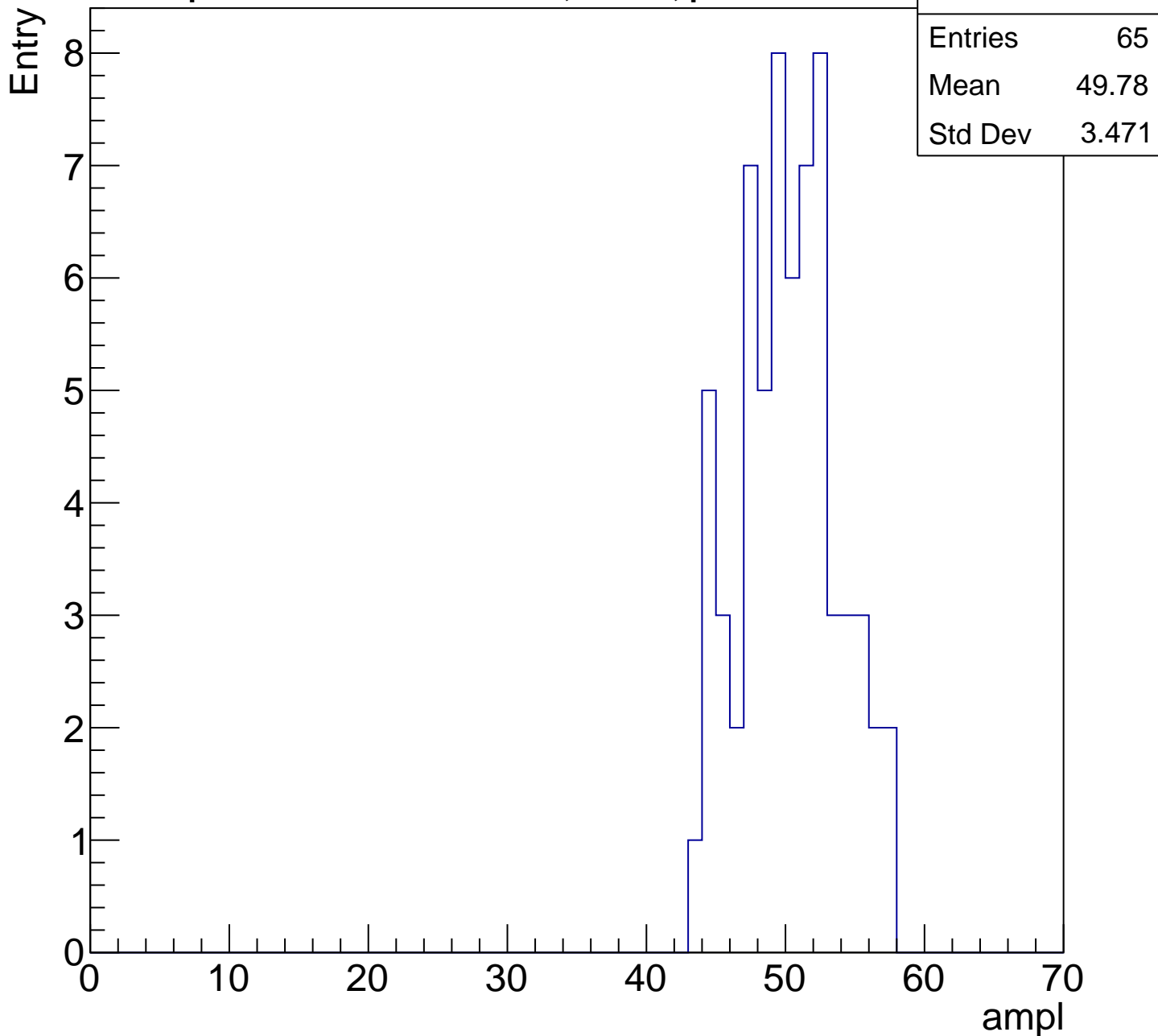
**Gaus mean : 43.2667**

**Gaus Width: 4.1452**



# B1L102S, U5-ch11, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

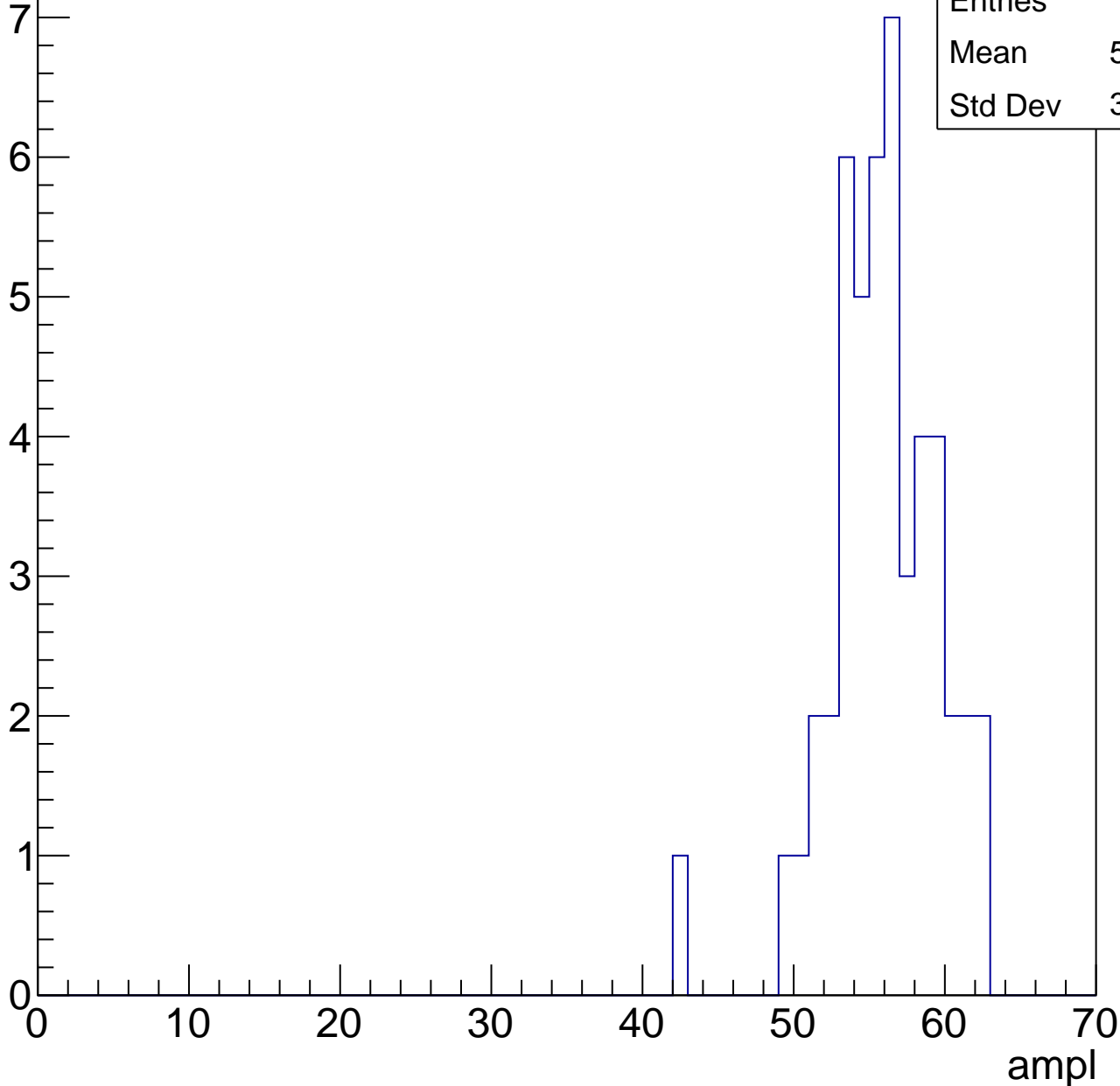


# B1L102S, U5-ch11, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	48
Mean	55.46
Std Dev	3.646

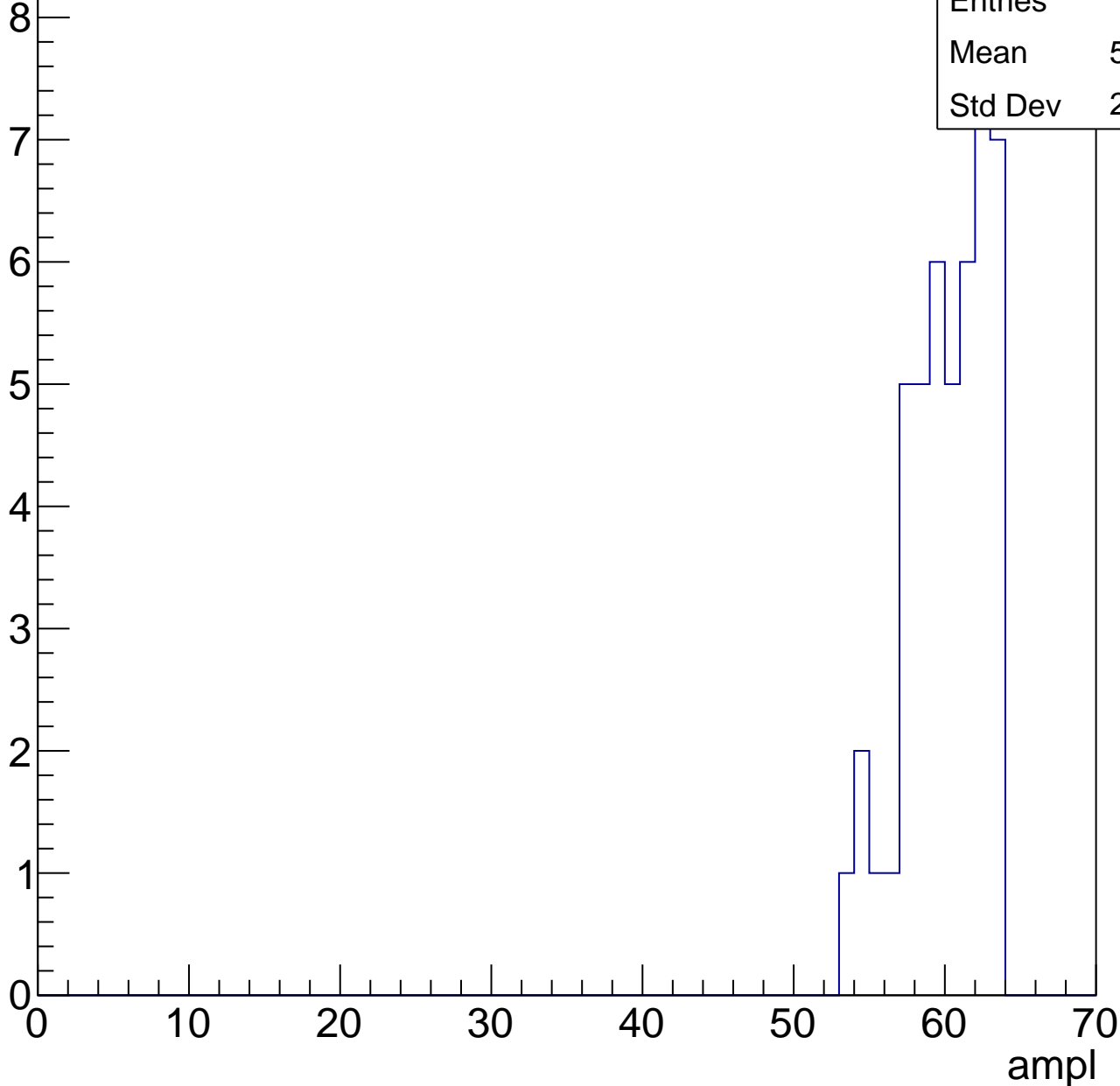


# B1L102S, U5-ch11, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	47
Mean	59.66
Std Dev	2.644



# B1L102S, U5-ch11, adc6

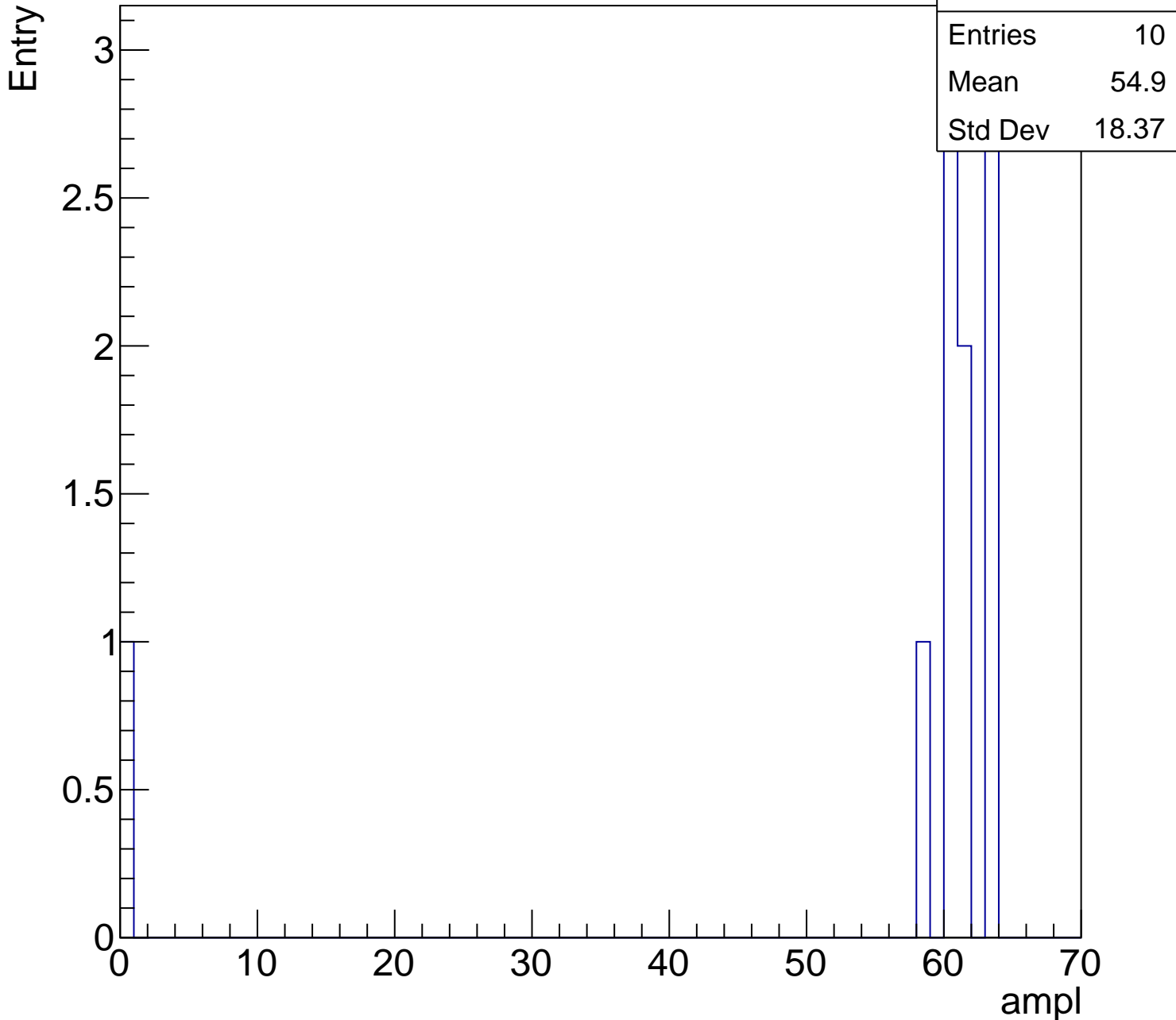
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

3  
2.5  
2  
1.5  
1  
0.5  
0

Entries	10
Mean	54.9
Std Dev	18.37

ampl





# B1L102S, U5-ch11, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	23
Std Dev	0

ampl

# B1L102S, U5-ch12, adc0

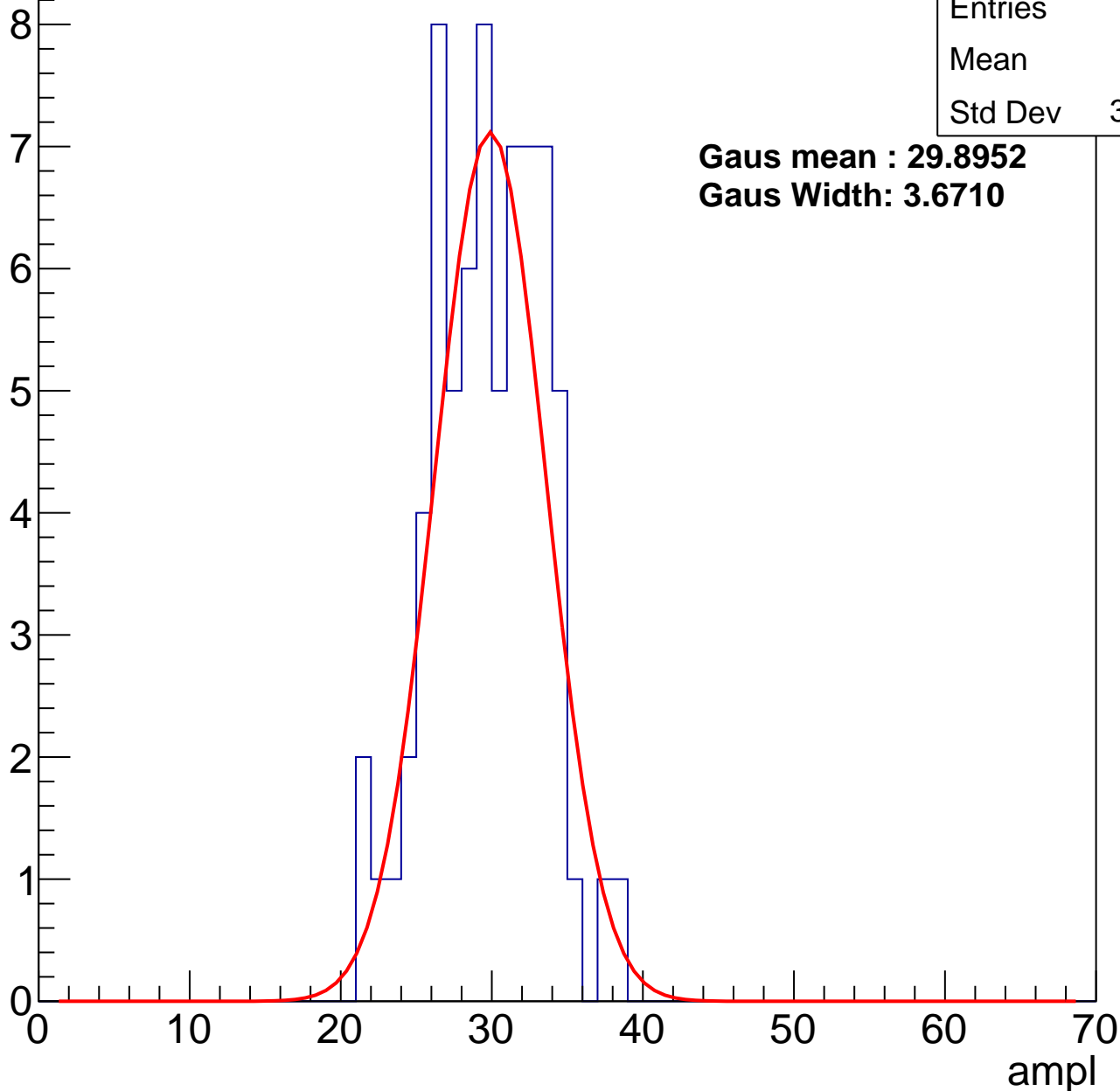
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	29.3
Std Dev	3.625

**Gaus mean : 29.8952**

**Gaus Width: 3.6710**



# B1L102S, U5-ch12, adc1

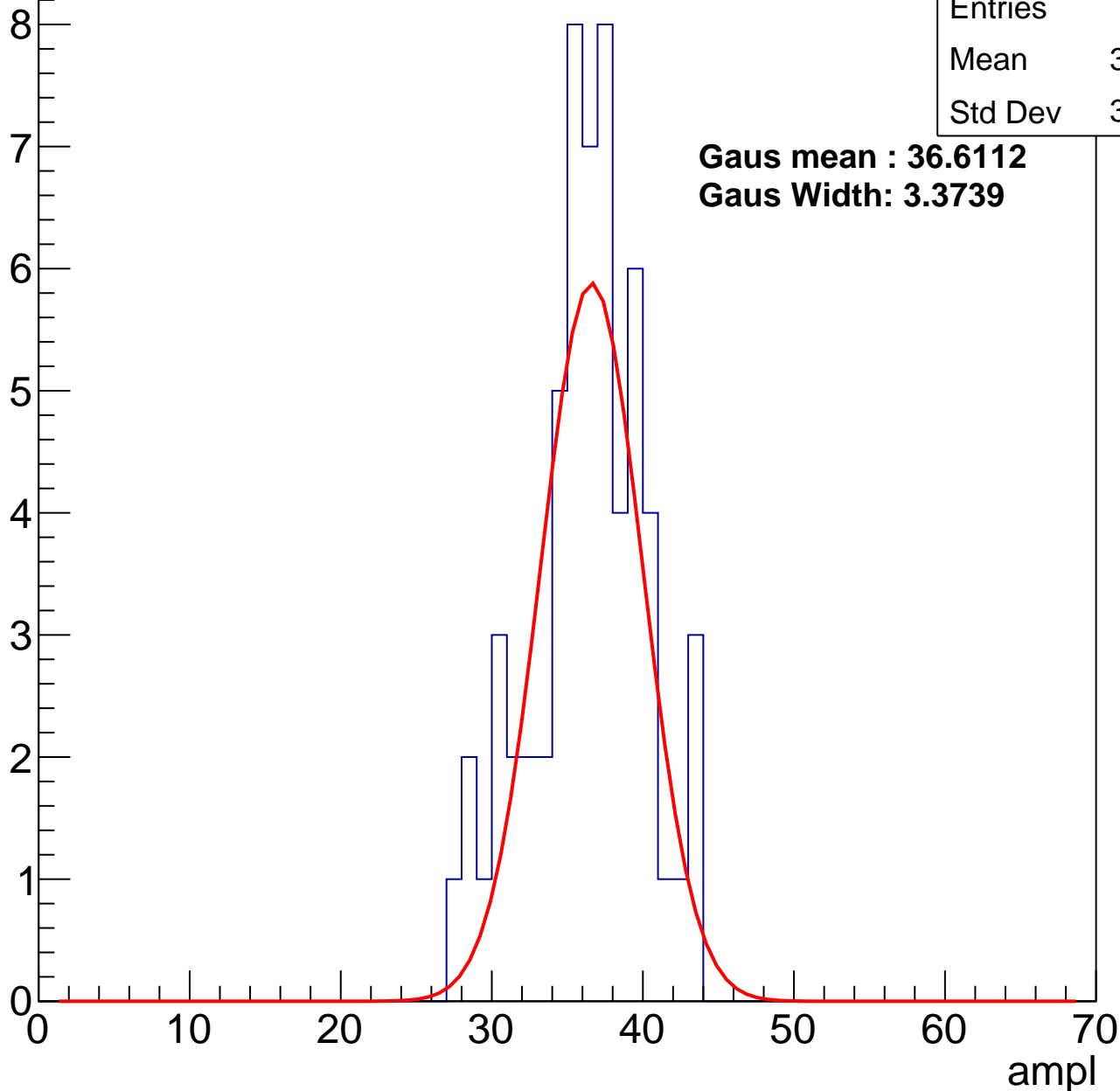
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	35.83
Std Dev	3.747

**Gaus mean : 36.6112**

**Gaus Width: 3.3739**



# B1L102S, U5-ch12, adc2

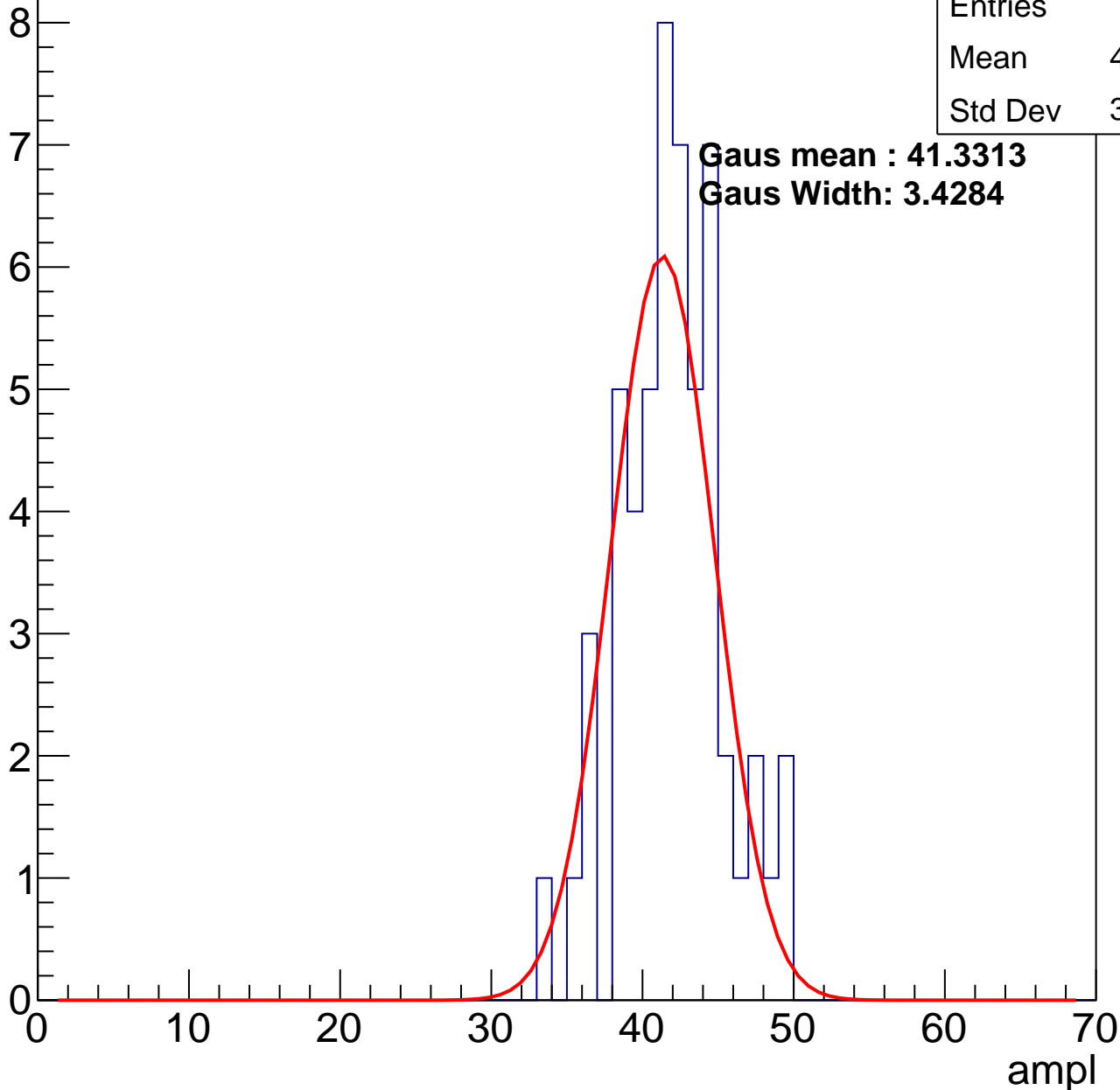
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	41.54
Std Dev	3.392

**Gaus mean : 41.3313**

**Gaus Width: 3.4284**

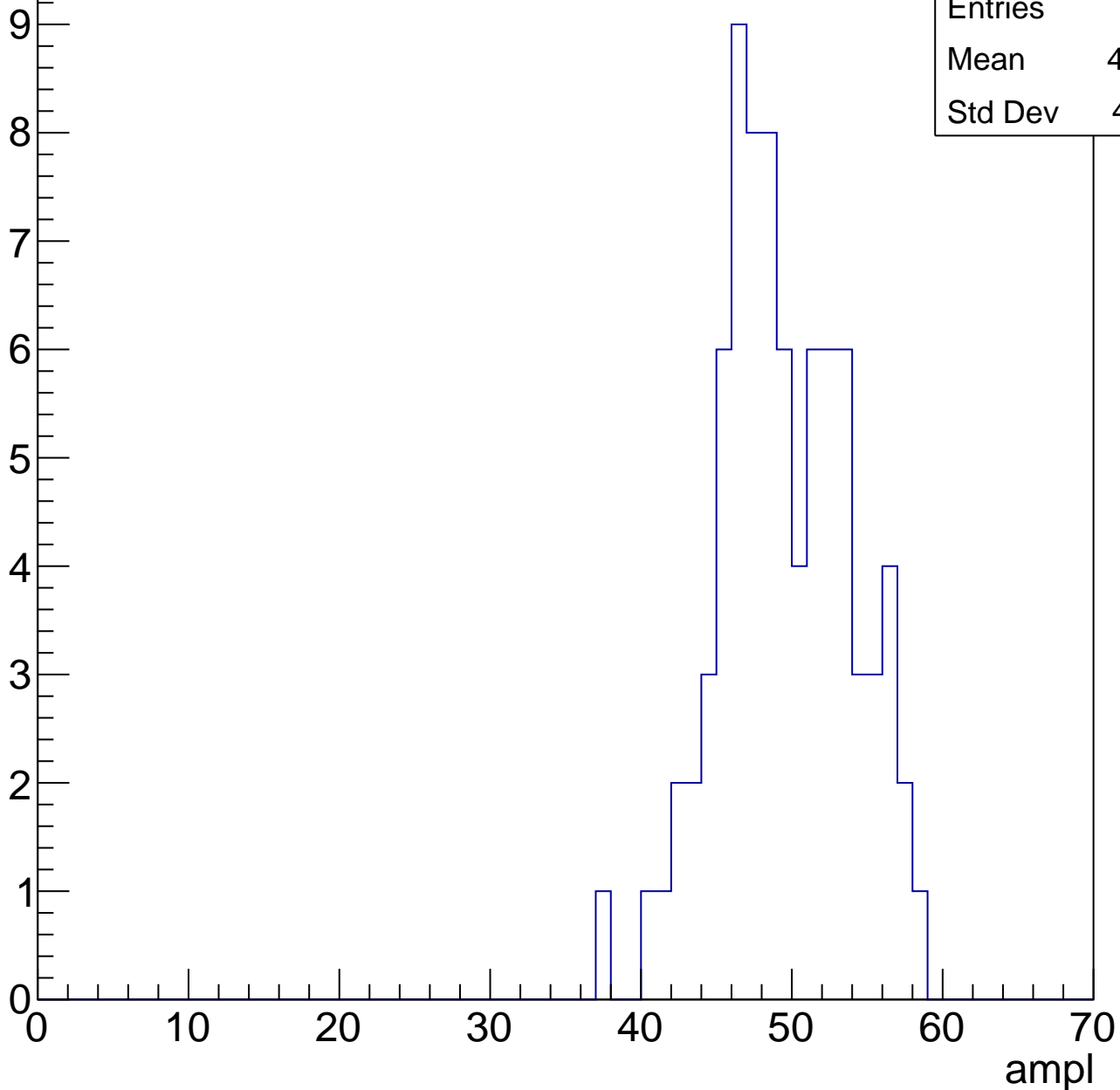


# B1L102S, U5-ch12, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	82
Mean	48.99
Std Dev	4.301

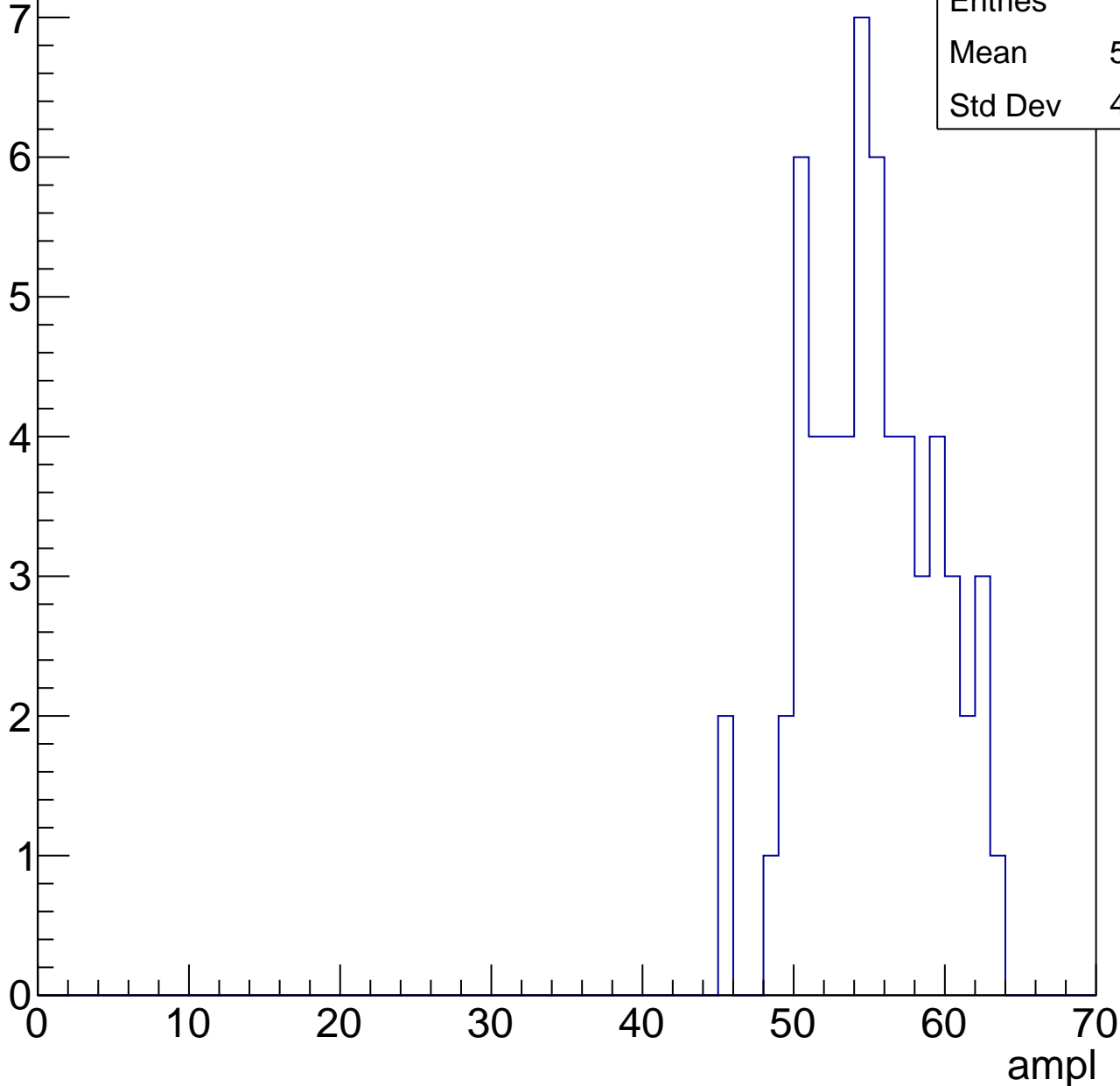


# B1L102S, U5-ch12, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	54.68
Std Dev	4.197

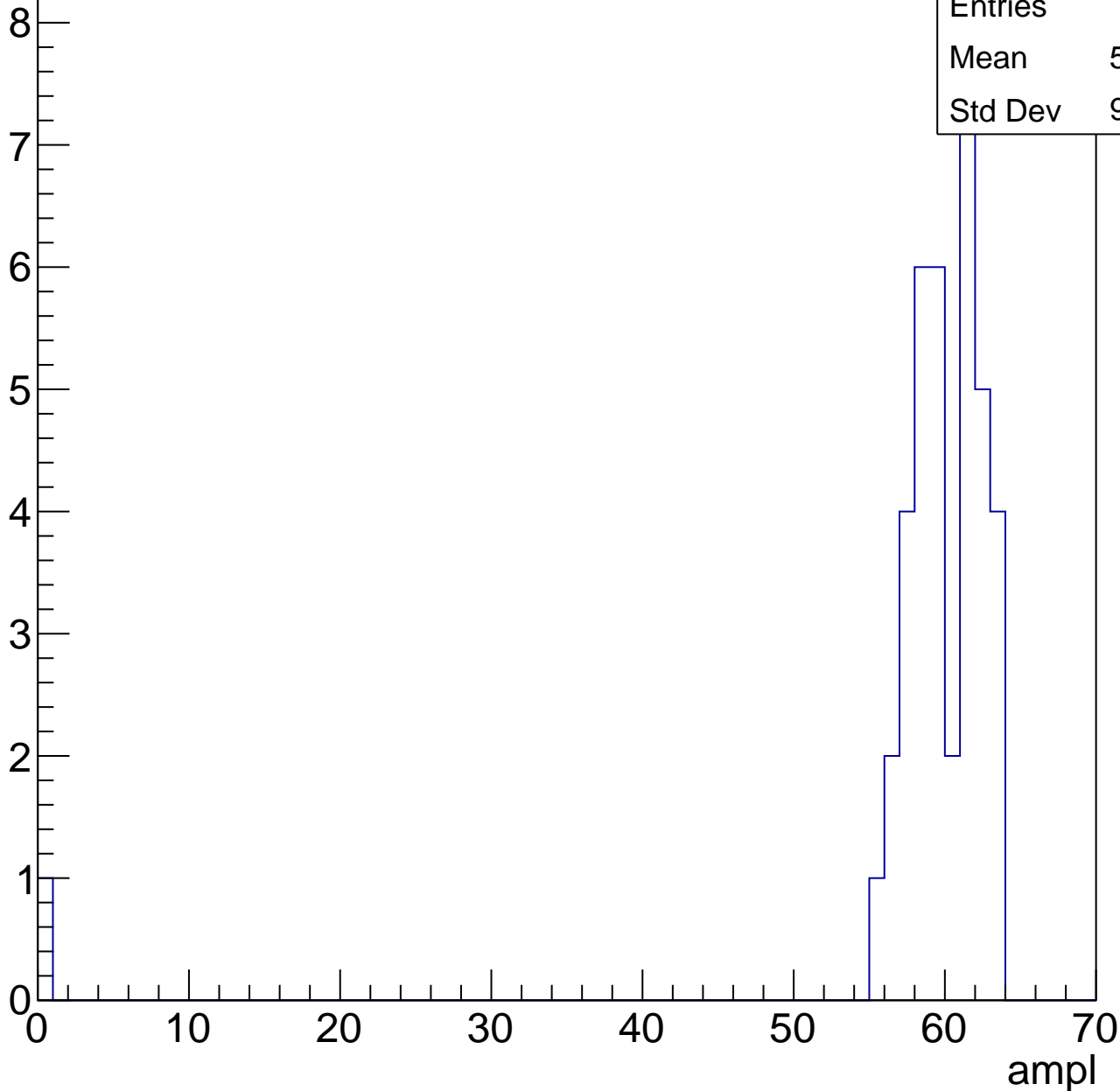


# B1L102S, U5-ch12, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	39
Mean	58.13
Std Dev	9.675

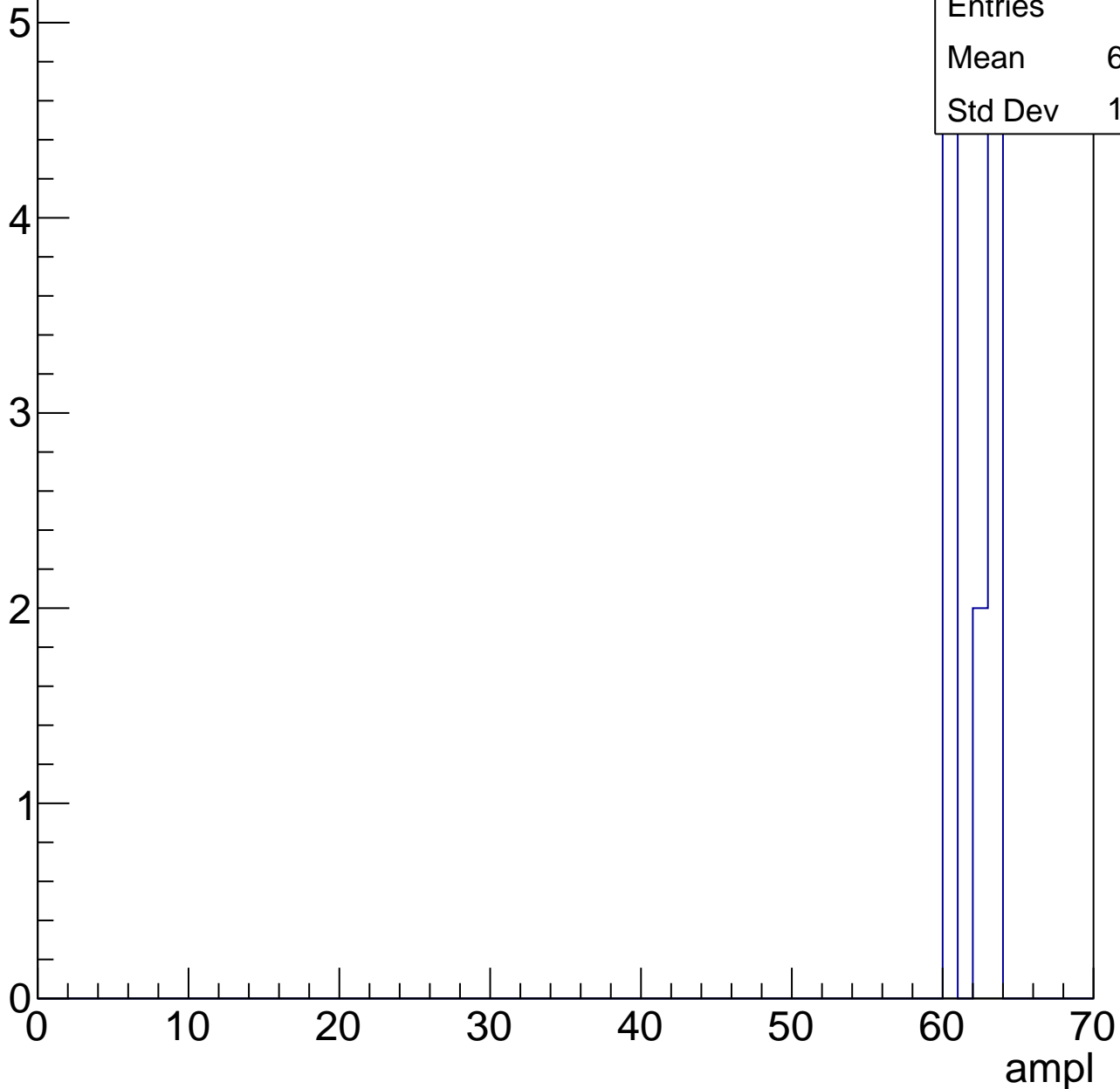


# B1L102S, U5-ch12, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	12
Mean	61.58
Std Dev	1.382





# B1L102S, U5-ch12, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U5-ch13, adc0

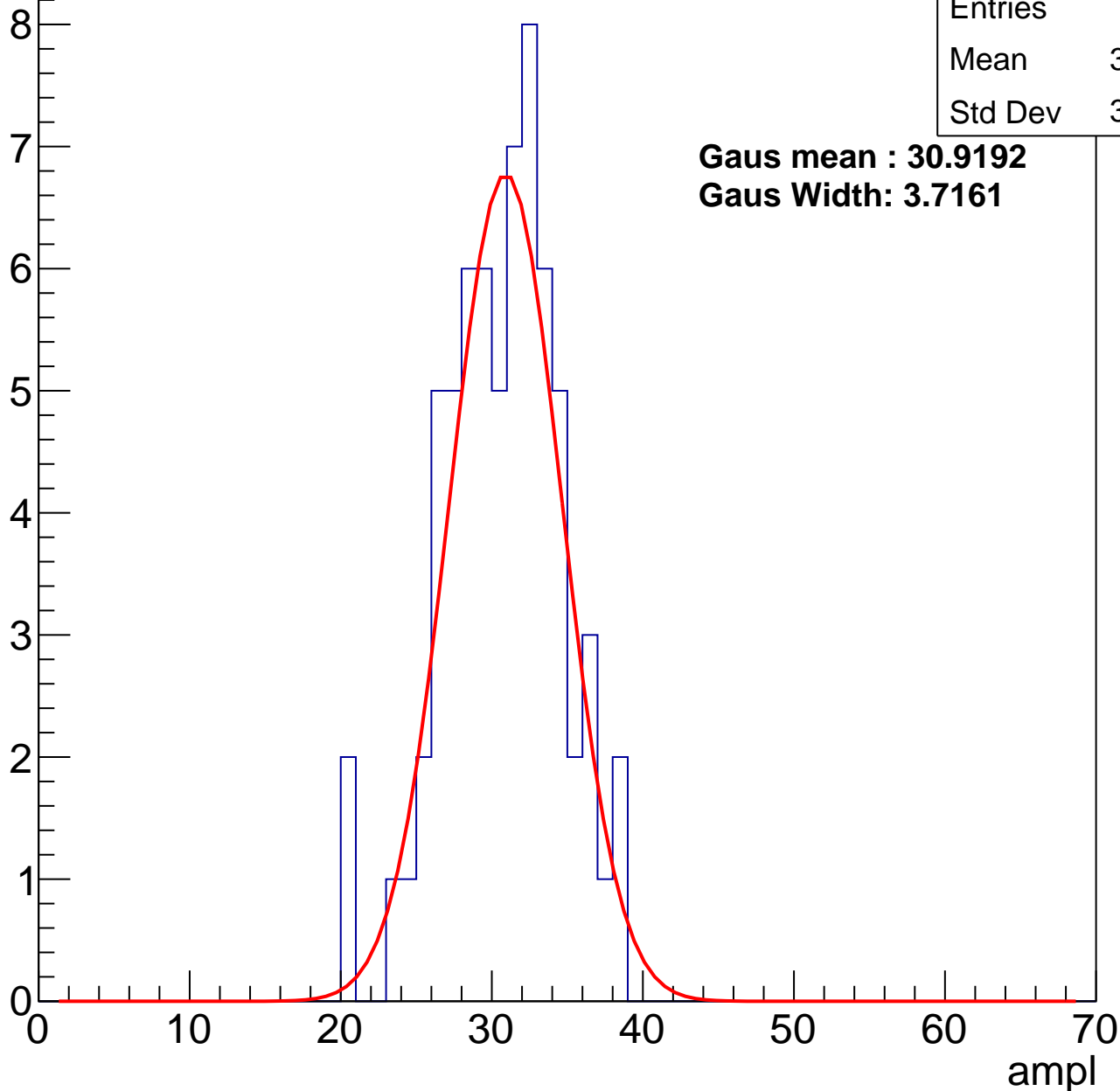
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	30.24
Std Dev	3.852

**Gaus mean : 30.9192**

**Gaus Width: 3.7161**



# B1L102S, U5-ch13, adc1

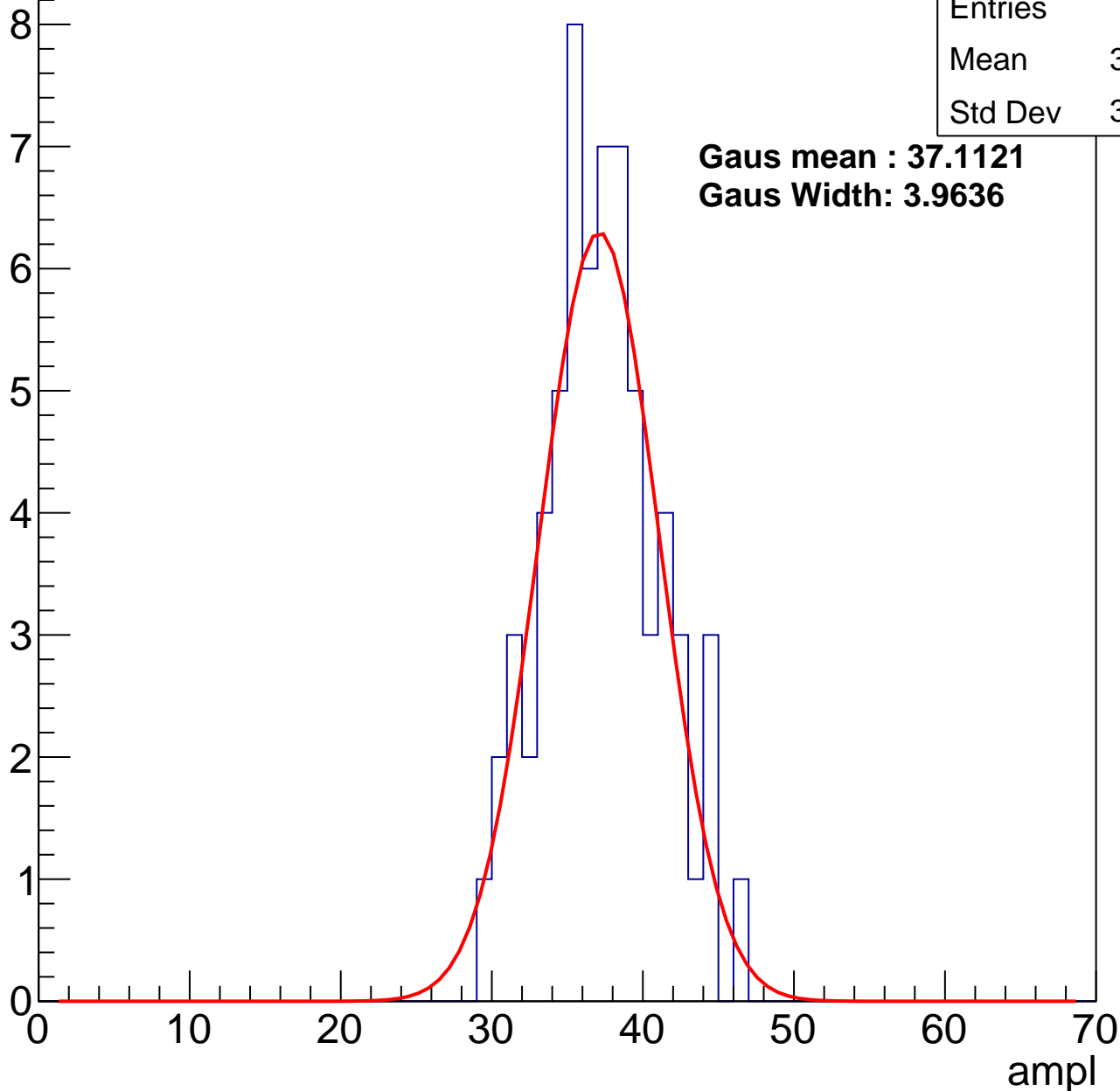
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	36.85
Std Dev	3.767

**Gaus mean : 37.1121**

**Gaus Width: 3.9636**



# B1L102S, U5-ch13, adc2

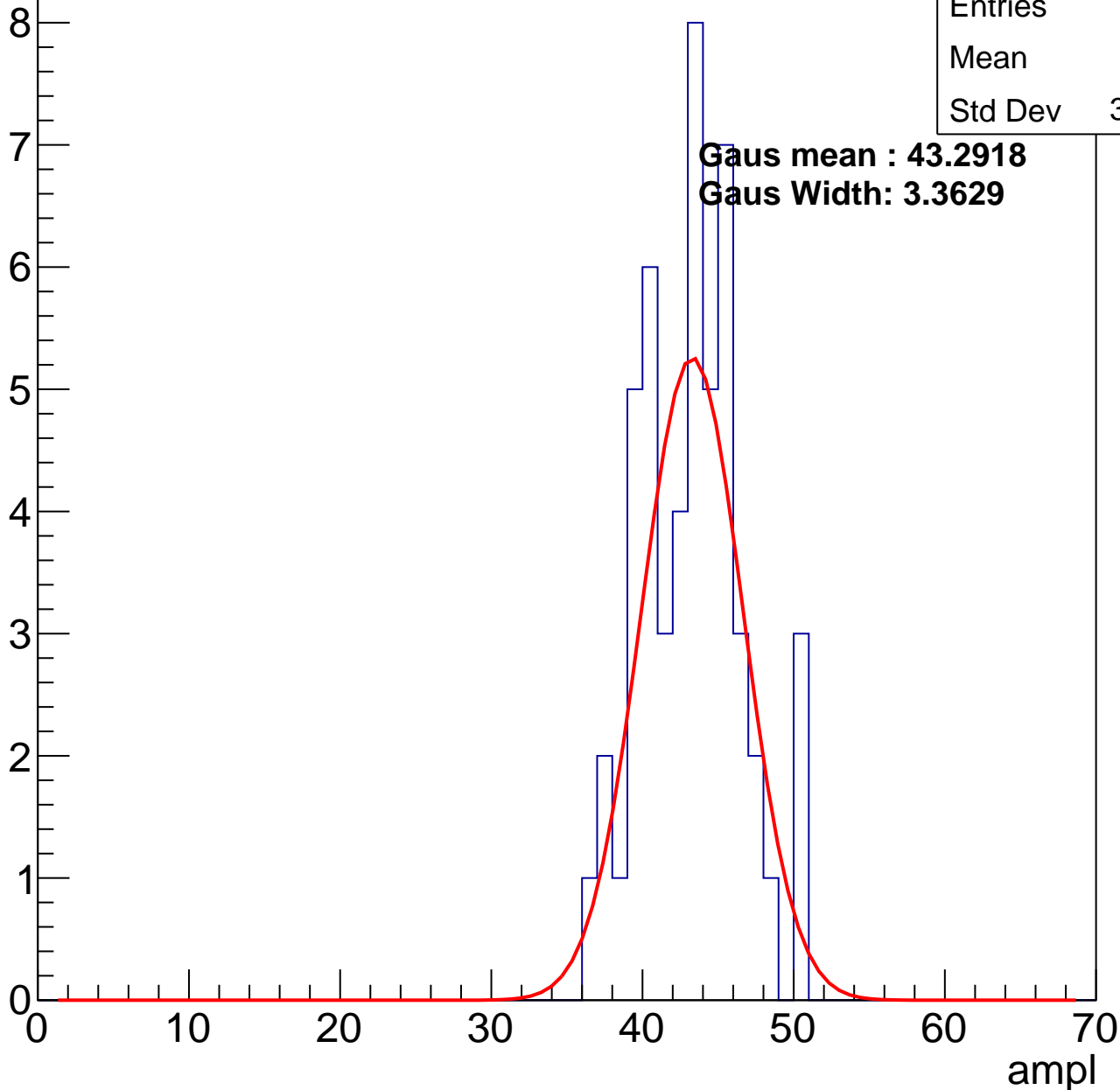
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	42.8
Std Dev	3.308

**Gaus mean : 43.2918**

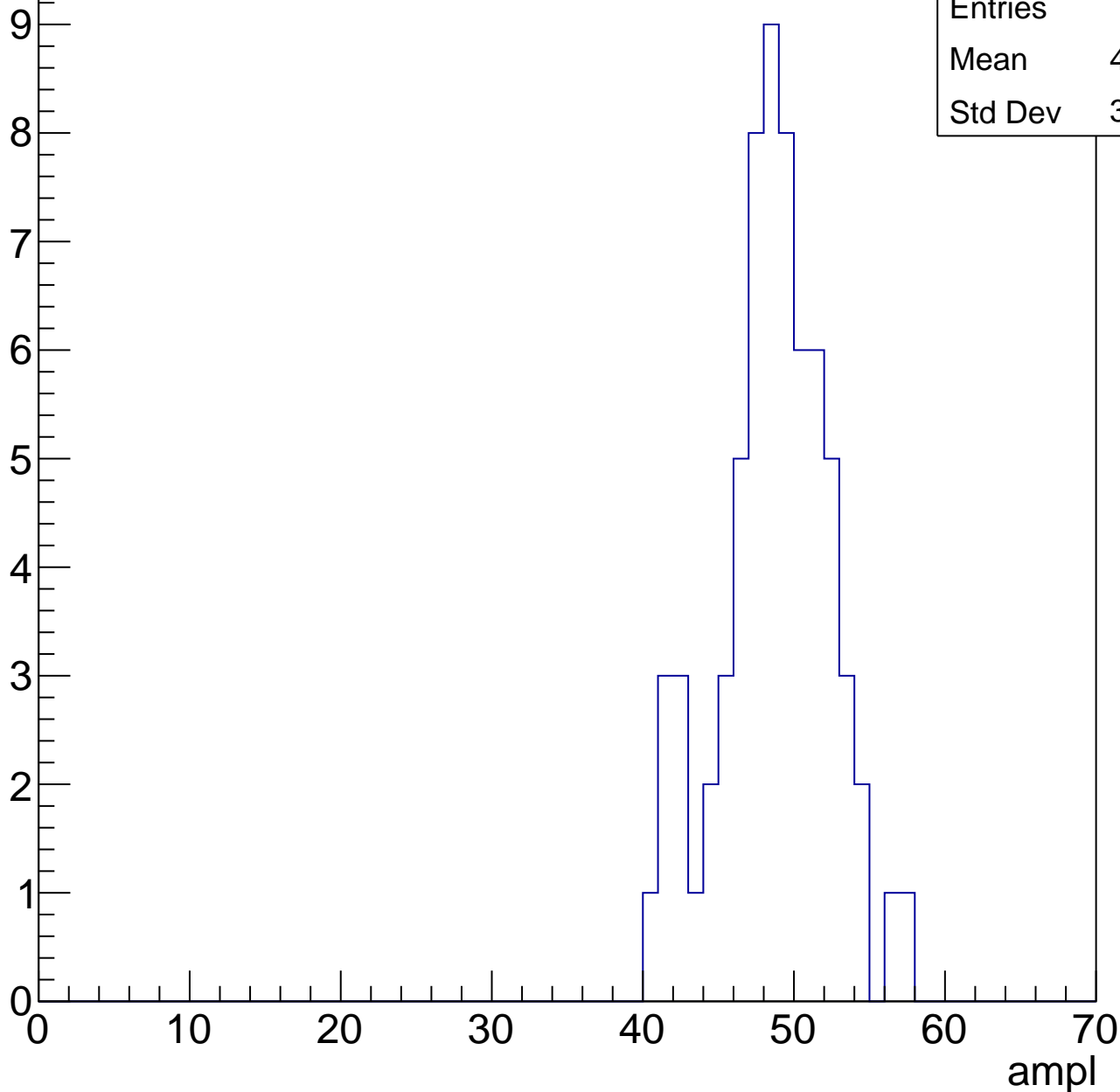
**Gaus Width: 3.3629**



# B1L102S, U5-ch13, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



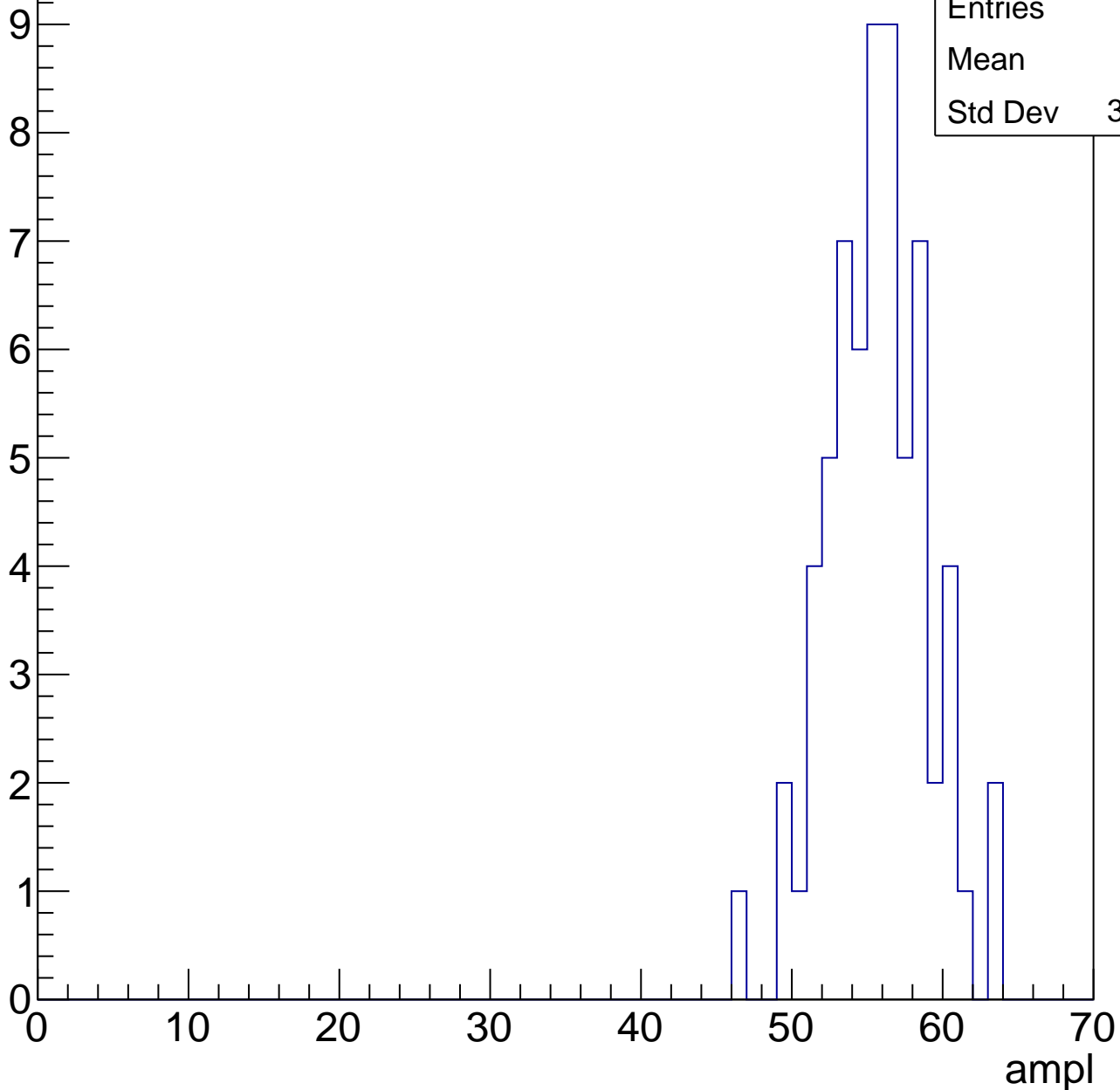
Entries	67
Mean	48.22
Std Dev	3.636

# B1L102S, U5-ch13, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	55.2
Std Dev	3.297

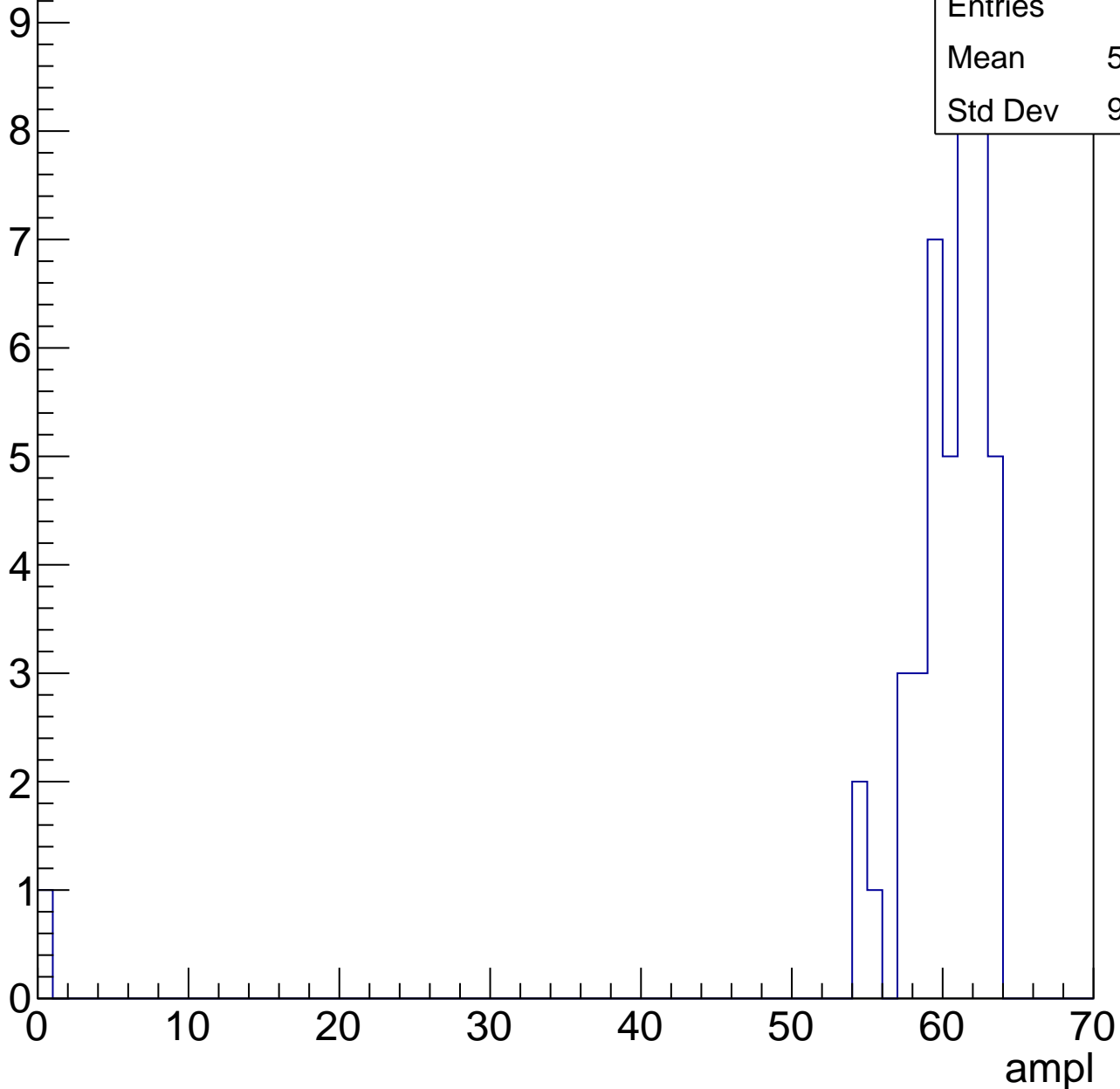


# B1L102S, U5-ch13, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	44
Mean	58.68
Std Dev	9.239



# B1L102S, U5-ch13, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

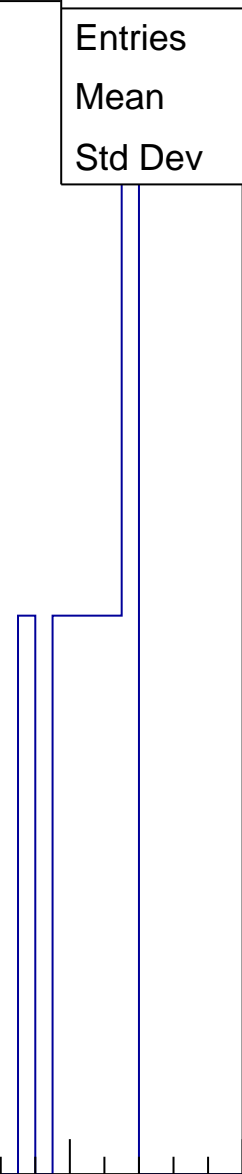
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	7
Mean	60.71
Std Dev	2.05

0 10 20 30 40 50 60 70

ampl





# B1L102S, U5-ch13, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U5-ch14, adc0

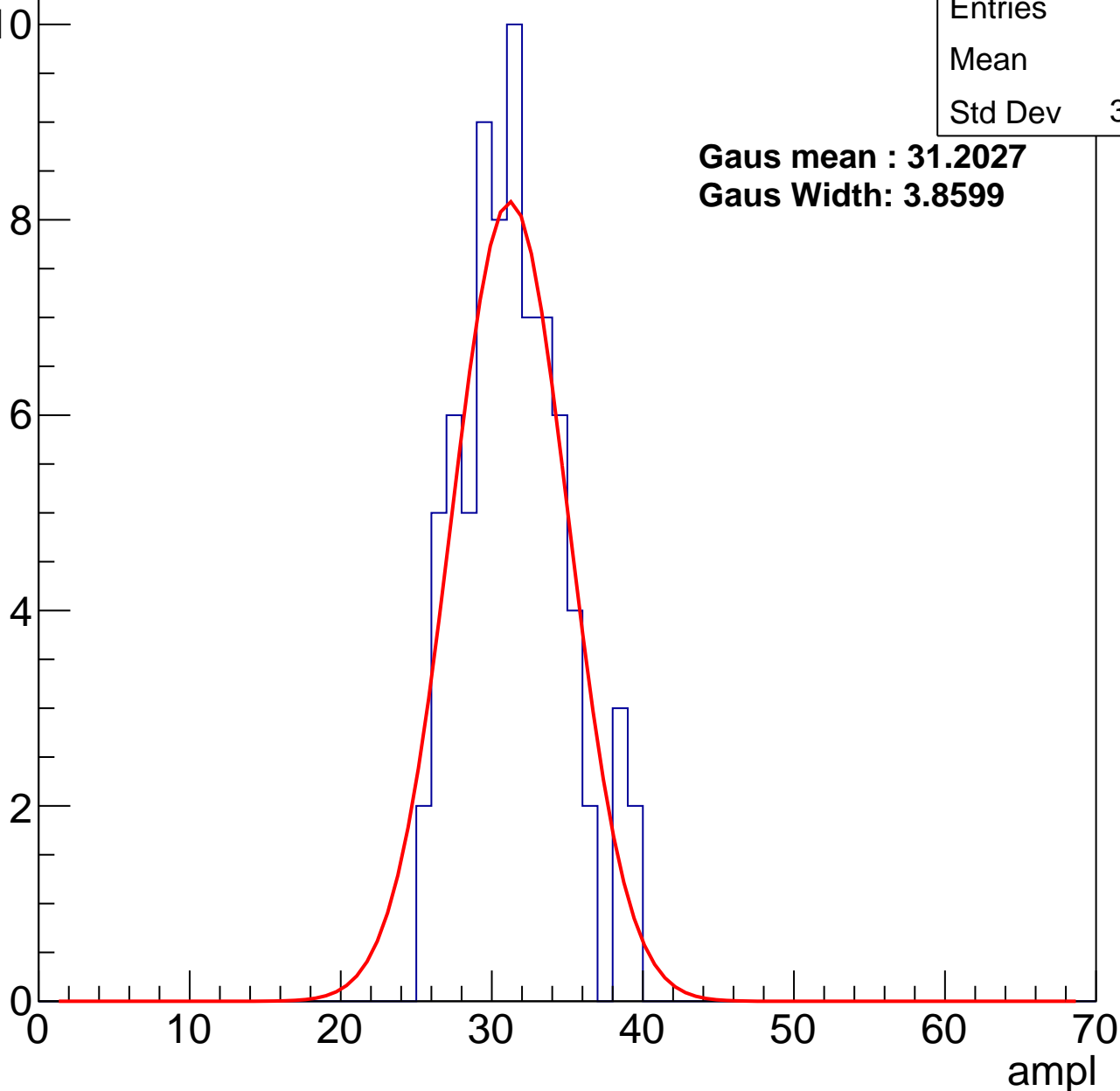
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	31
Std Dev	3.364

**Gaus mean : 31.2027**

**Gaus Width: 3.8599**



# B1L102S, U5-ch14, adc1

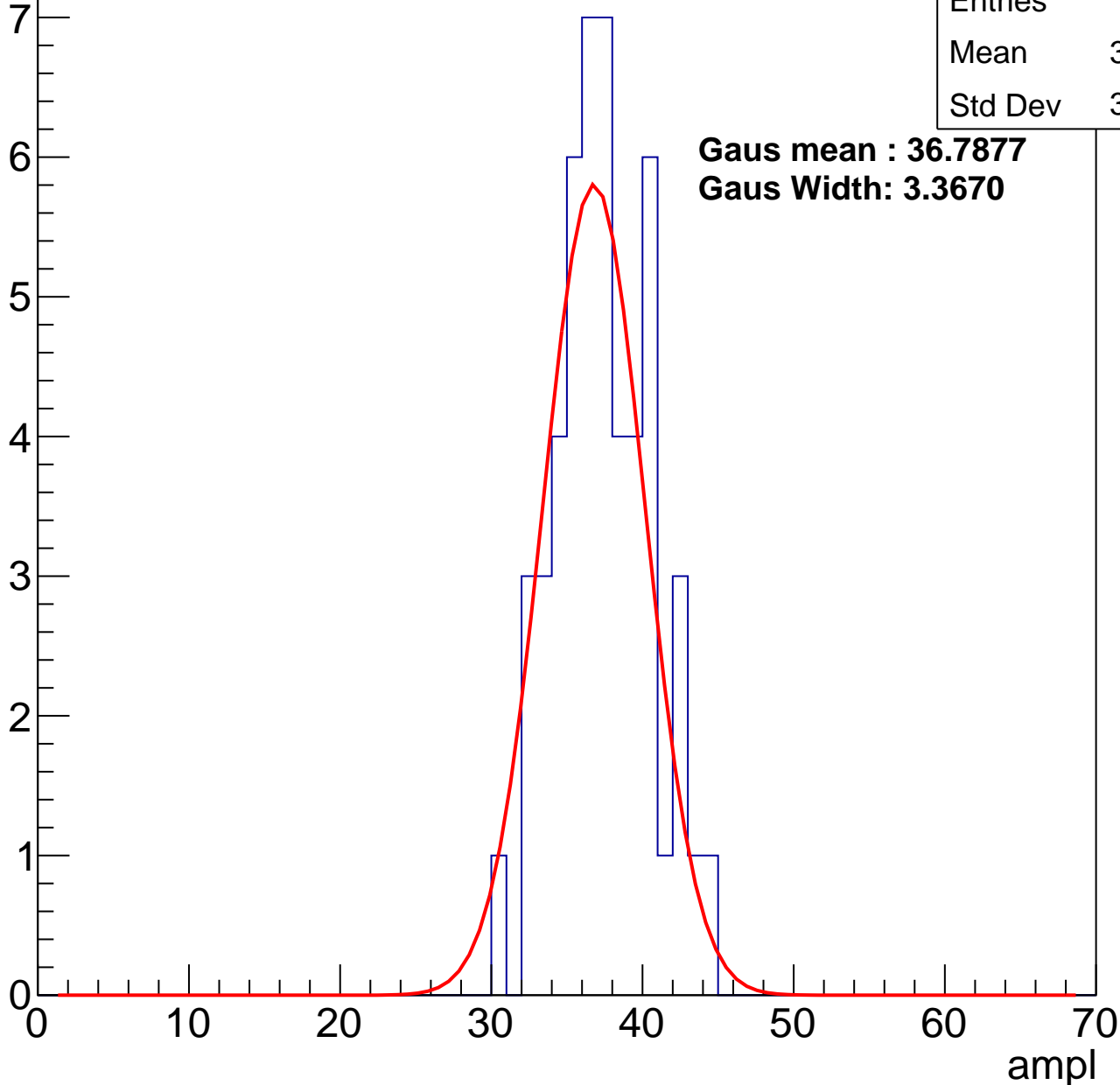
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	36.94
Std Dev	3.096

**Gaus mean : 36.7877**

**Gaus Width: 3.3670**



# B1L102S, U5-ch14, adc2

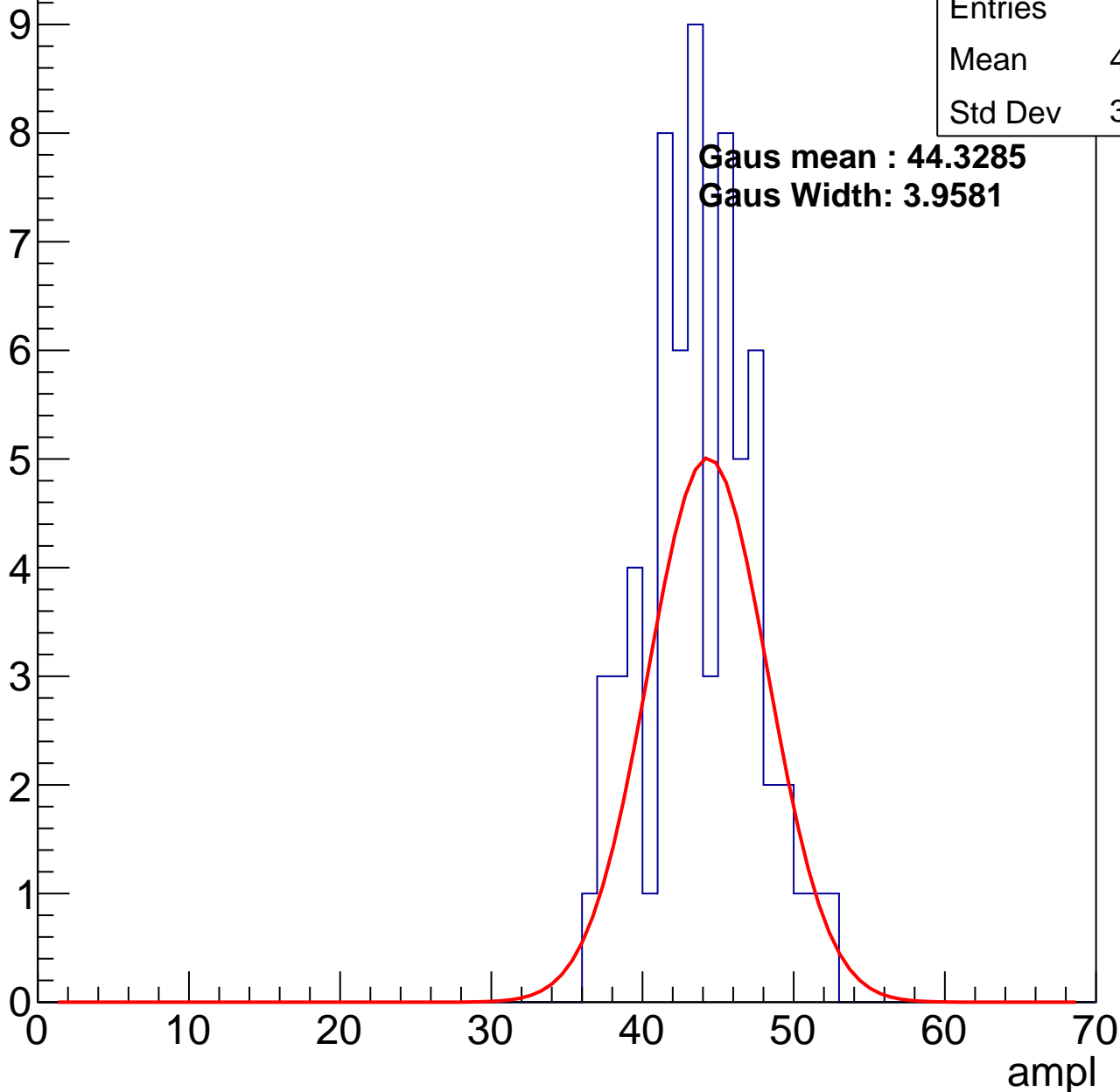
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	43.36
Std Dev	3.594

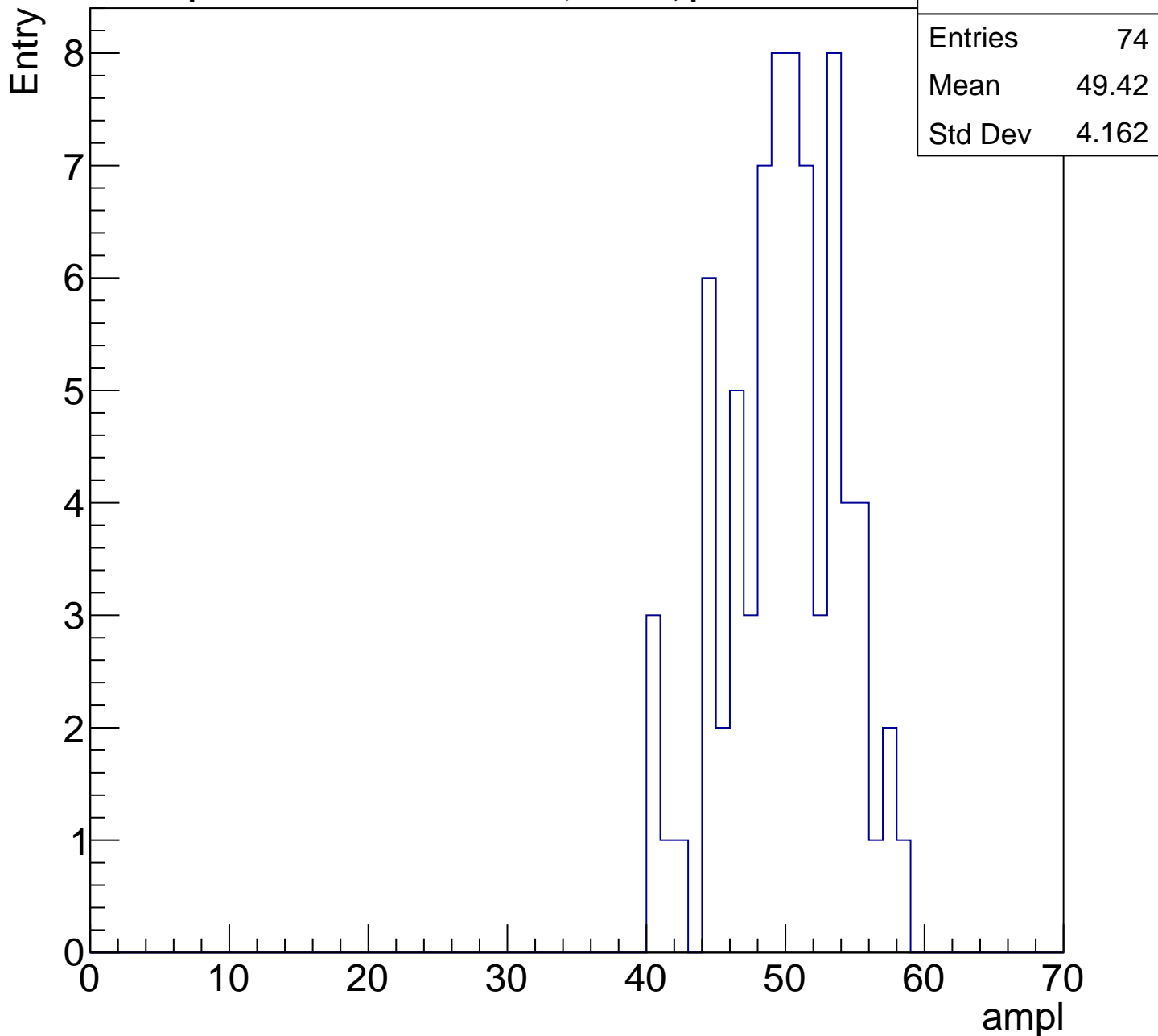
**Gaus mean : 44.3285**

**Gaus Width: 3.9581**



# B1L102S, U5-ch14, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

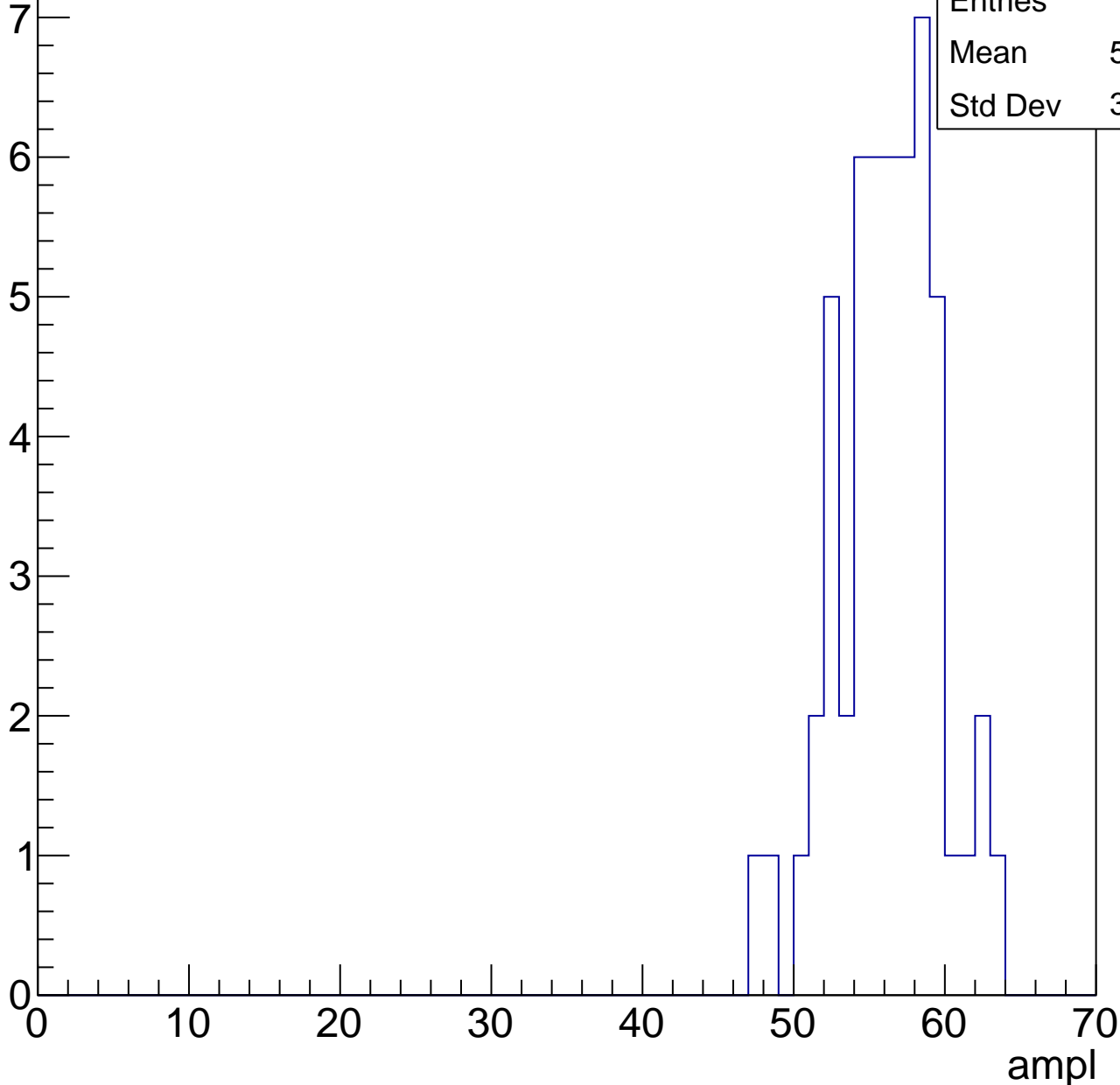


# B1L102S, U5-ch14, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	55.74
Std Dev	3.354

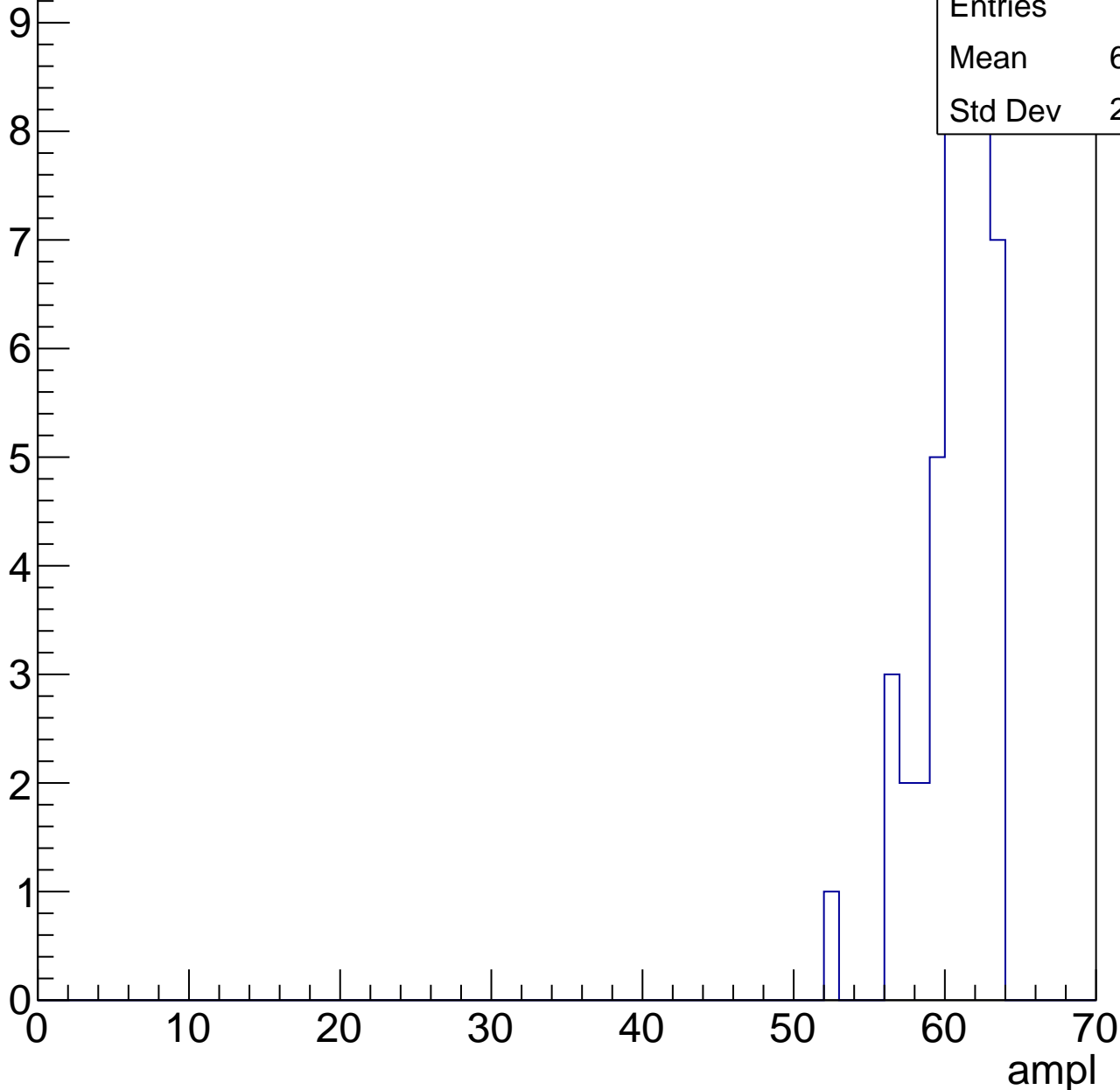


# B1L102S, U5-ch14, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

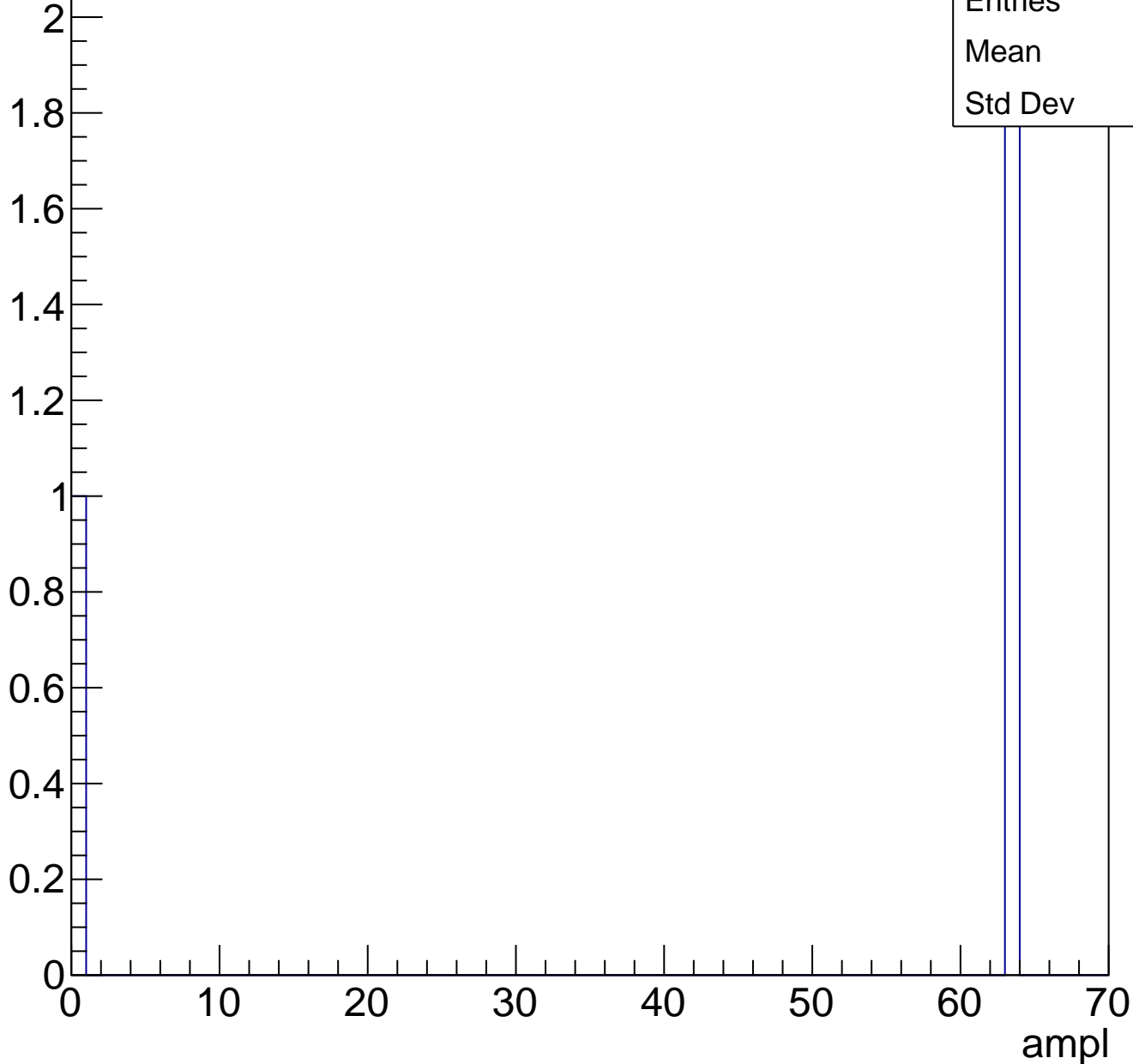
Entries	46
Mean	60.24
Std Dev	2.305



# B1L102S, U5-ch14, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U5-ch14, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U5-ch15, adc0

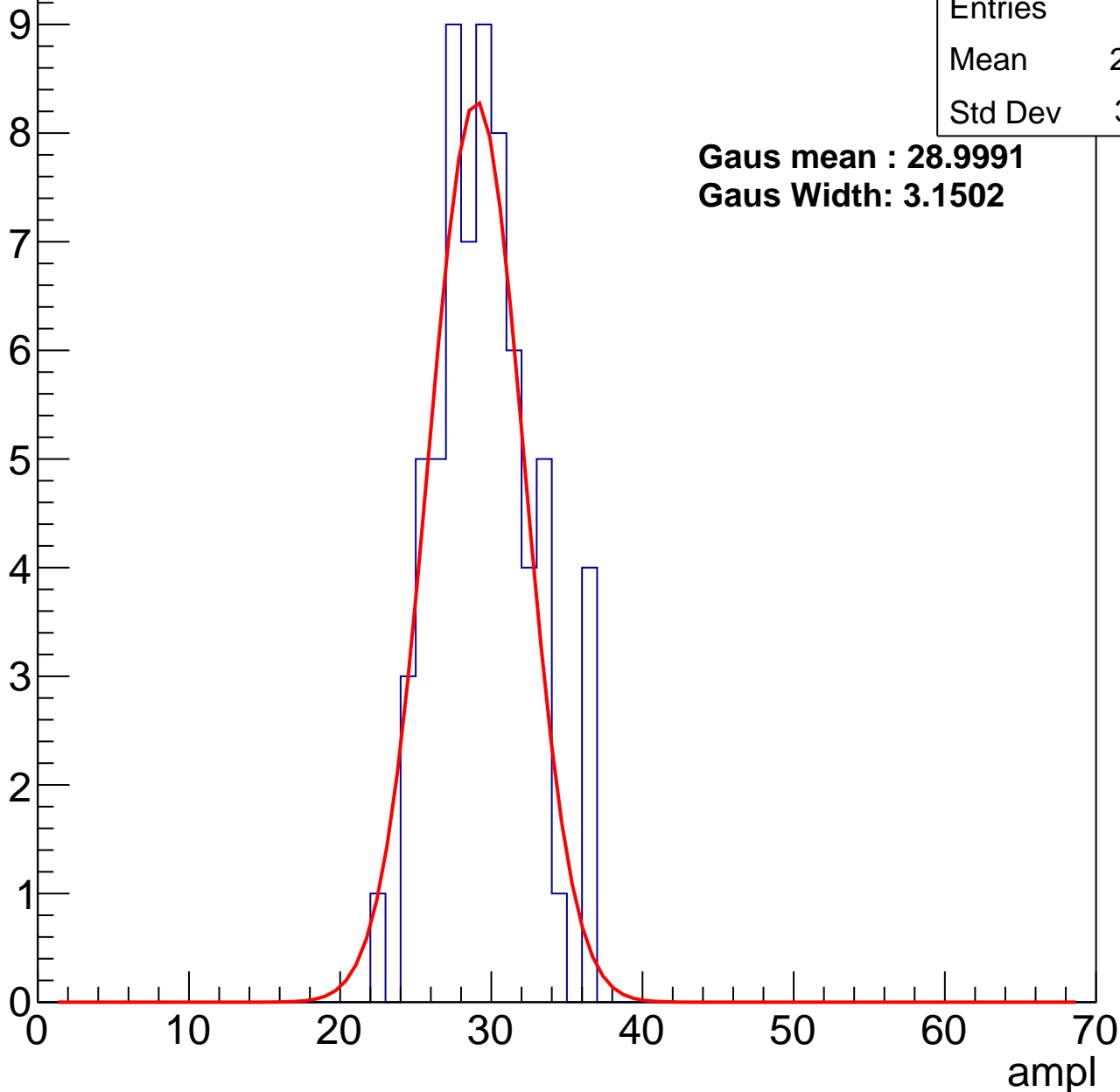
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	29.04
Std Dev	3.141

**Gaus mean : 28.9991**

**Gaus Width: 3.1502**



# B1L102S, U5-ch15, adc1

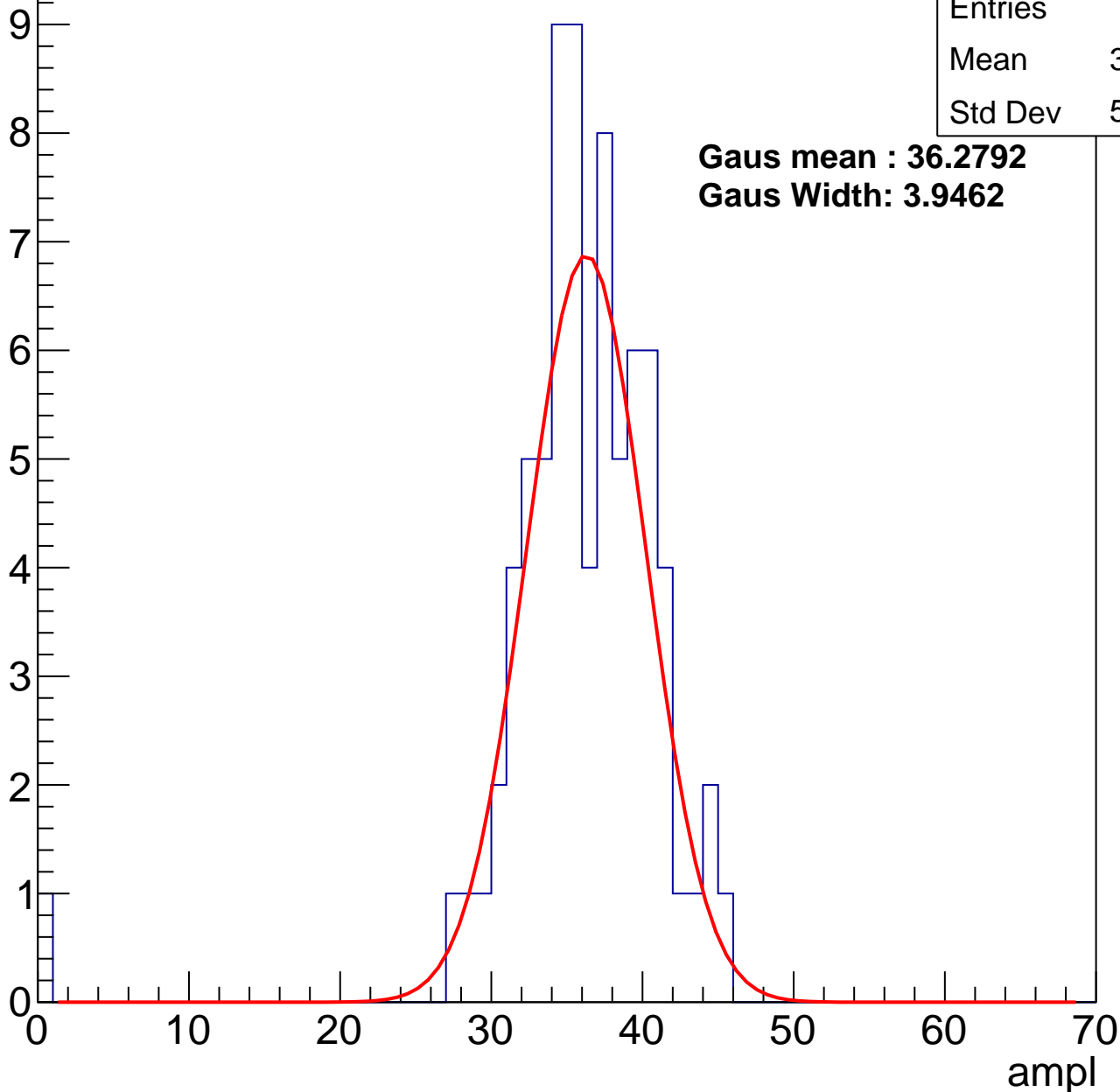
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	35.53
Std Dev	5.604

**Gaus mean : 36.2792**

**Gaus Width: 3.9462**



# B1L102S, U5-ch15, adc2

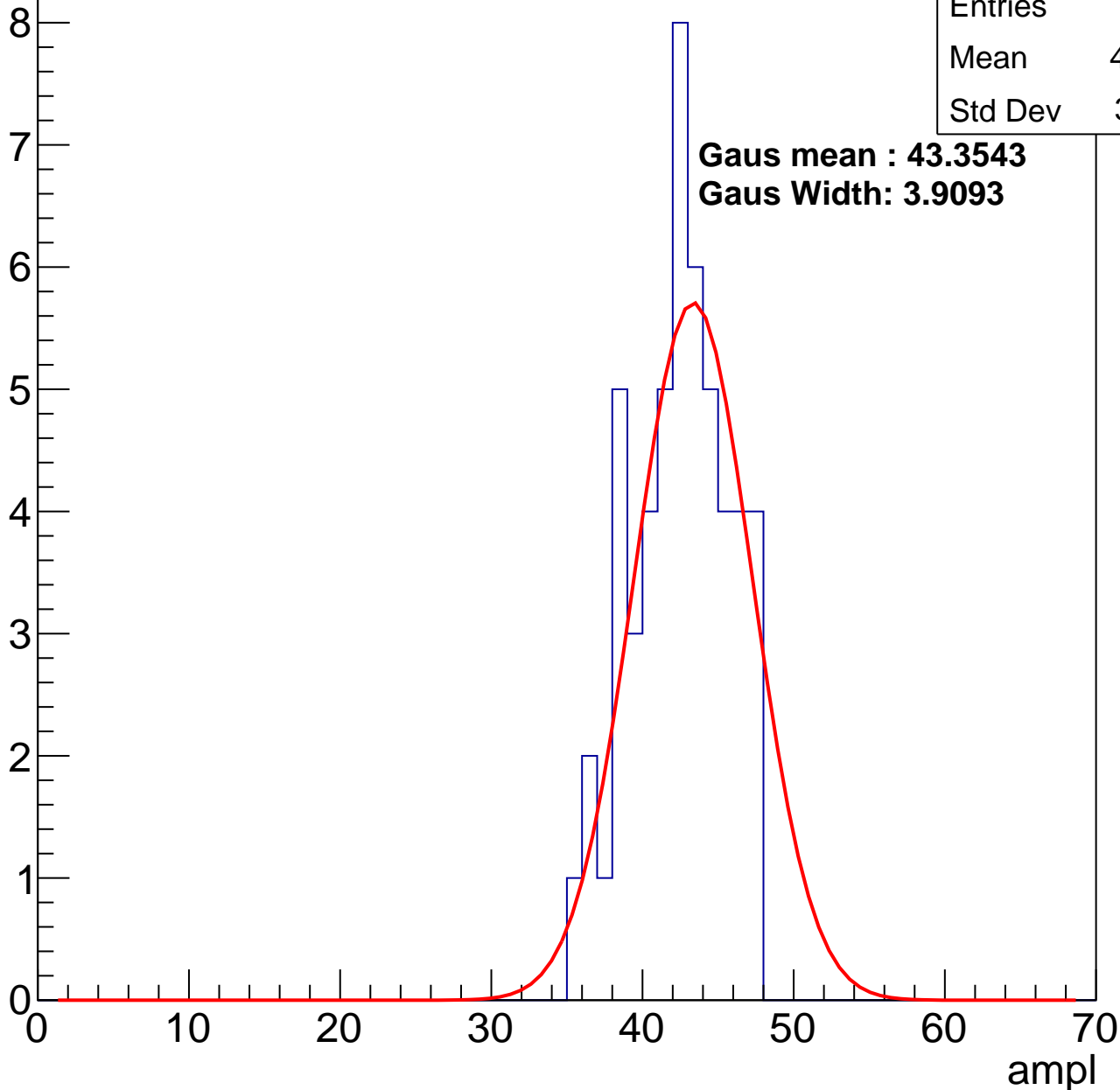
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	41.96
Std Dev	3.101

**Gaus mean : 43.3543**

**Gaus Width: 3.9093**

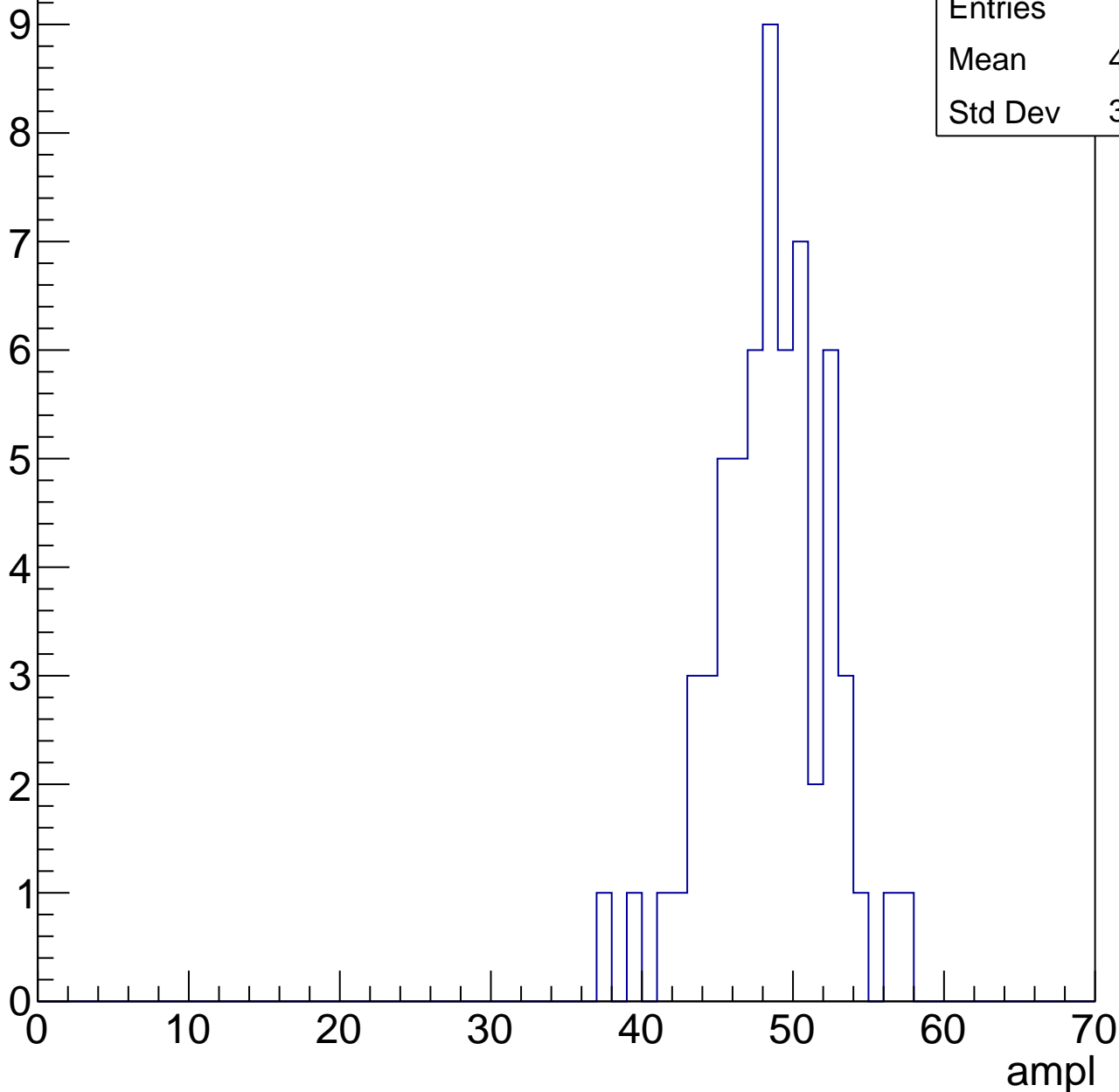


# B1L102S, U5-ch15, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

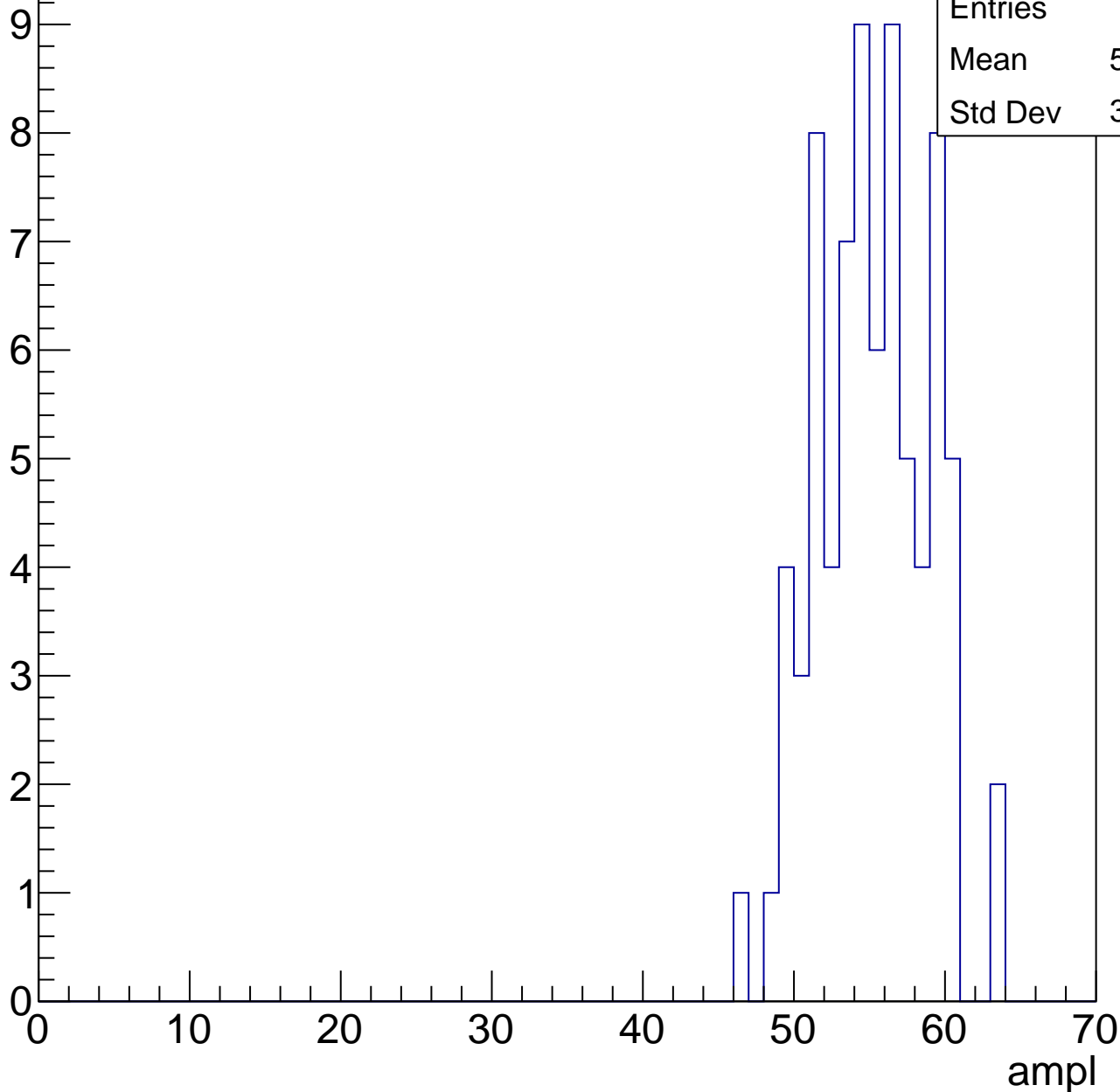
Entries	62
Mean	47.95
Std Dev	3.778



# B1L102S, U5-ch15, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

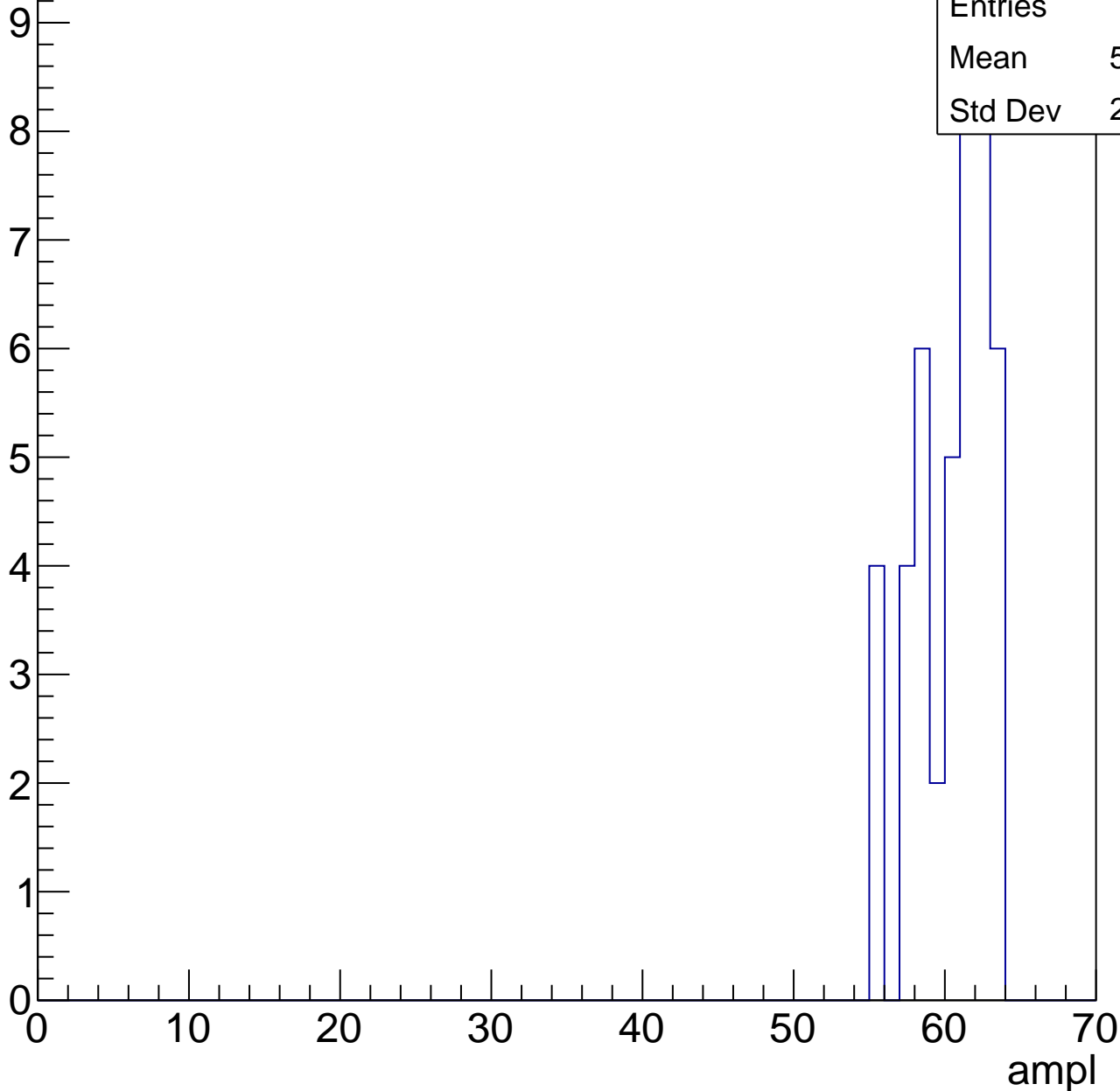


# B1L102S, U5-ch15, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

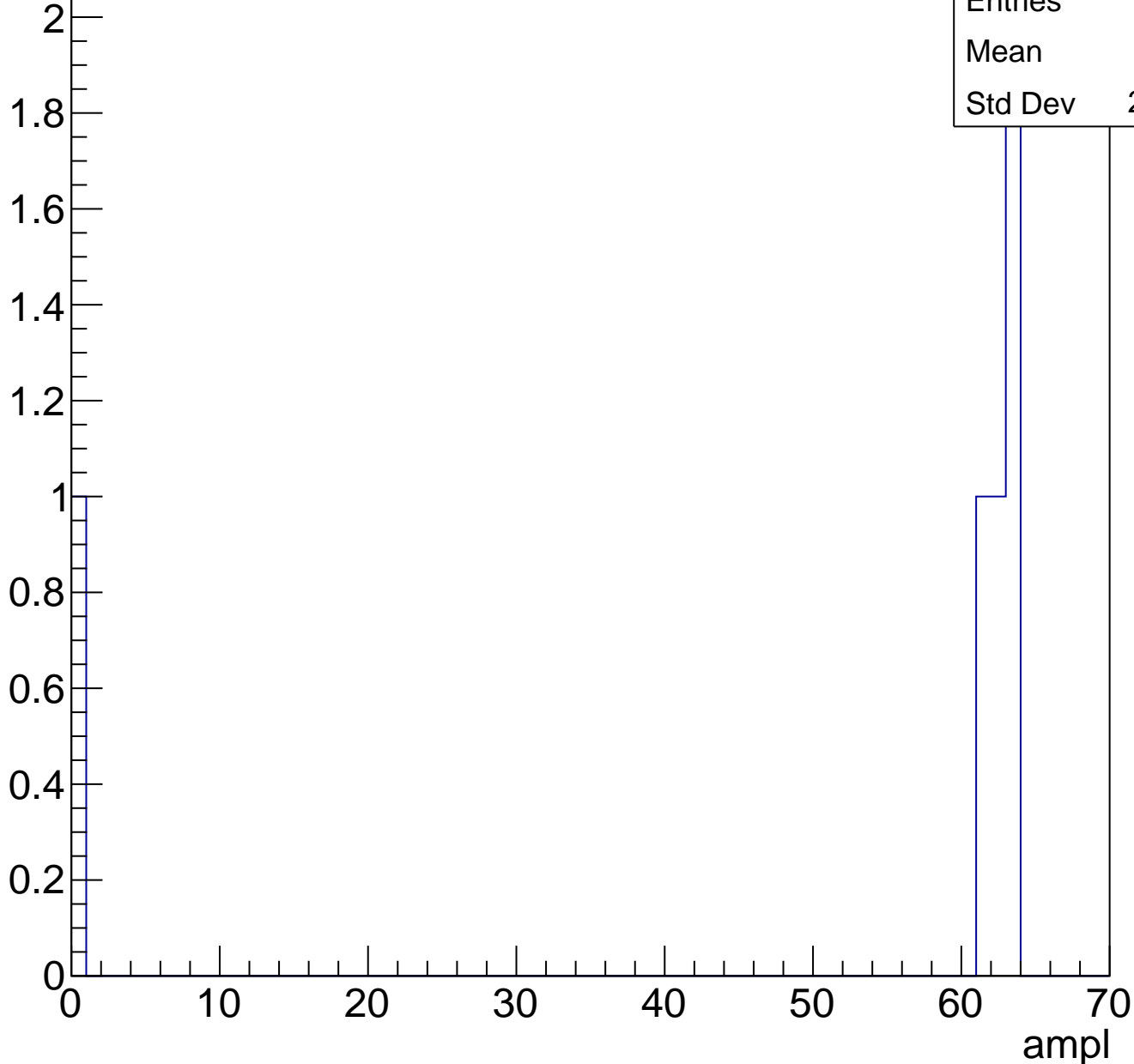
Entries	45
Mean	59.98
Std Dev	2.408



# B1L102S, U5-ch15, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U5-ch15, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U5-ch16, adc0

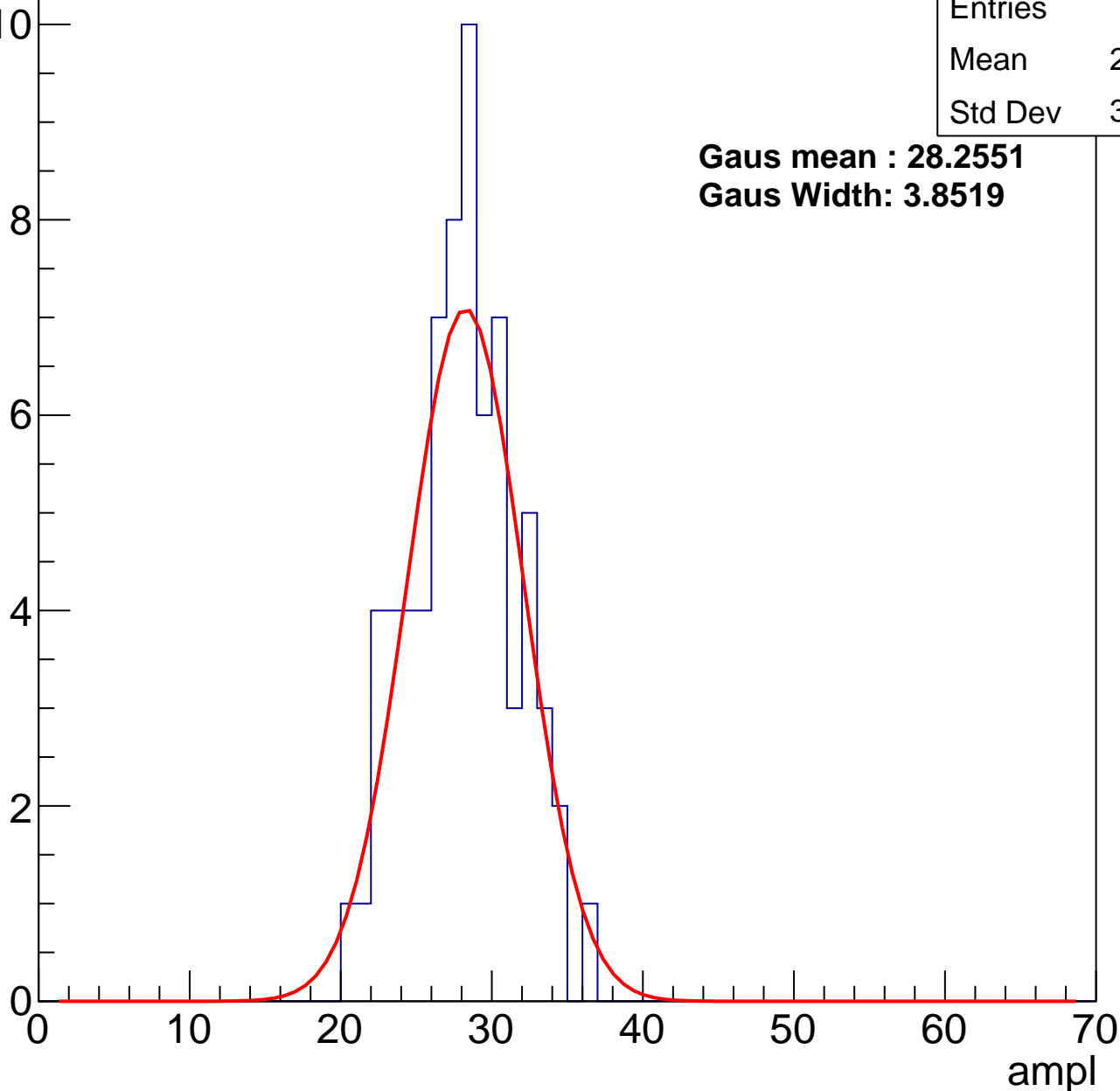
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	27.64
Std Dev	3.456

**Gaus mean : 28.2551**

**Gaus Width: 3.8519**



# B1L102S, U5-ch16, adc1

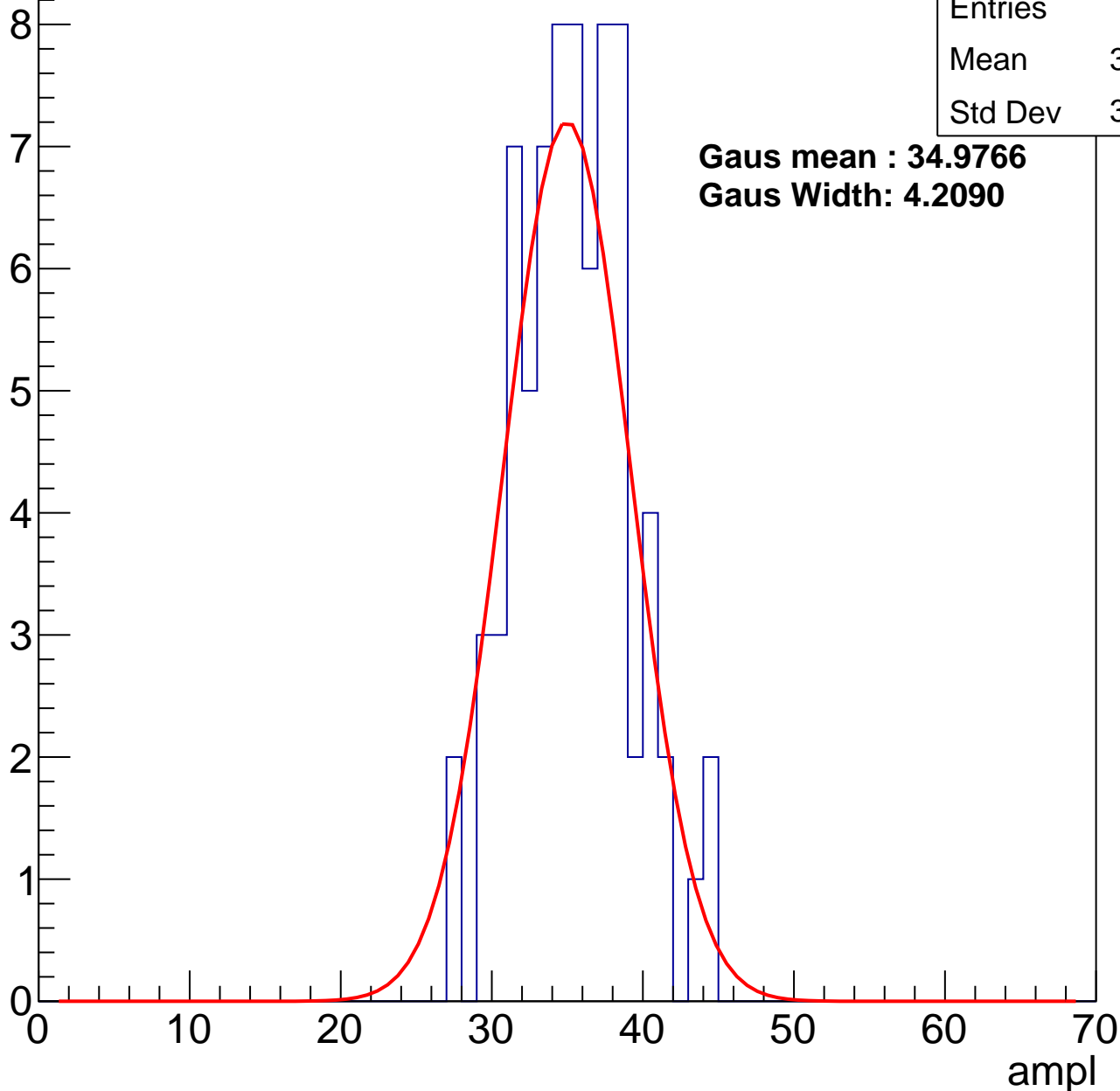
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	34.97
Std Dev	3.706

**Gaus mean : 34.9766**

**Gaus Width: 4.2090**



# B1L102S, U5-ch16, adc2

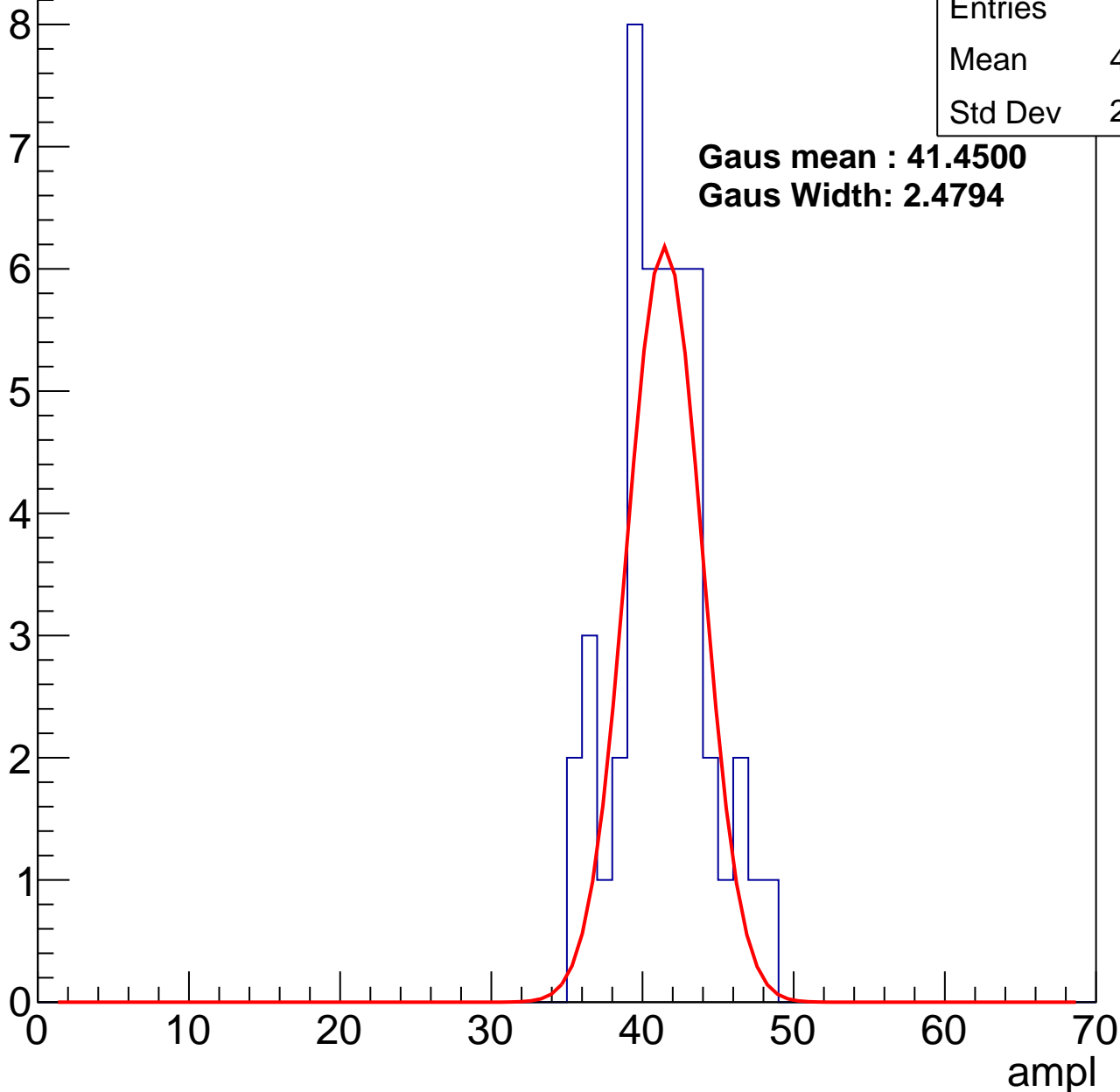
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	47
Mean	40.83
Std Dev	2.977

**Gaus mean : 41.4500**

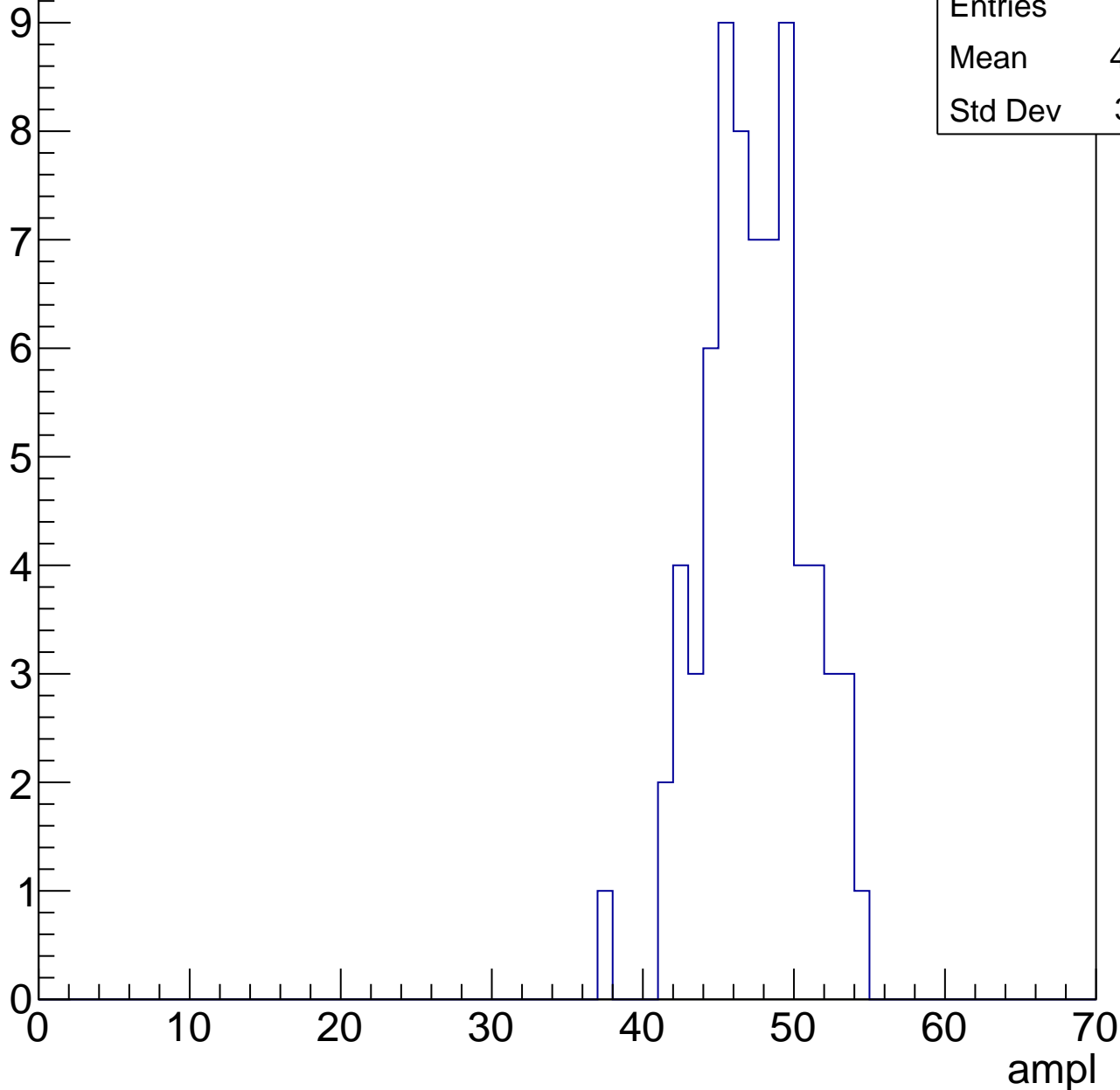
**Gaus Width: 2.4794**



# B1L102S, U5-ch16, adc3

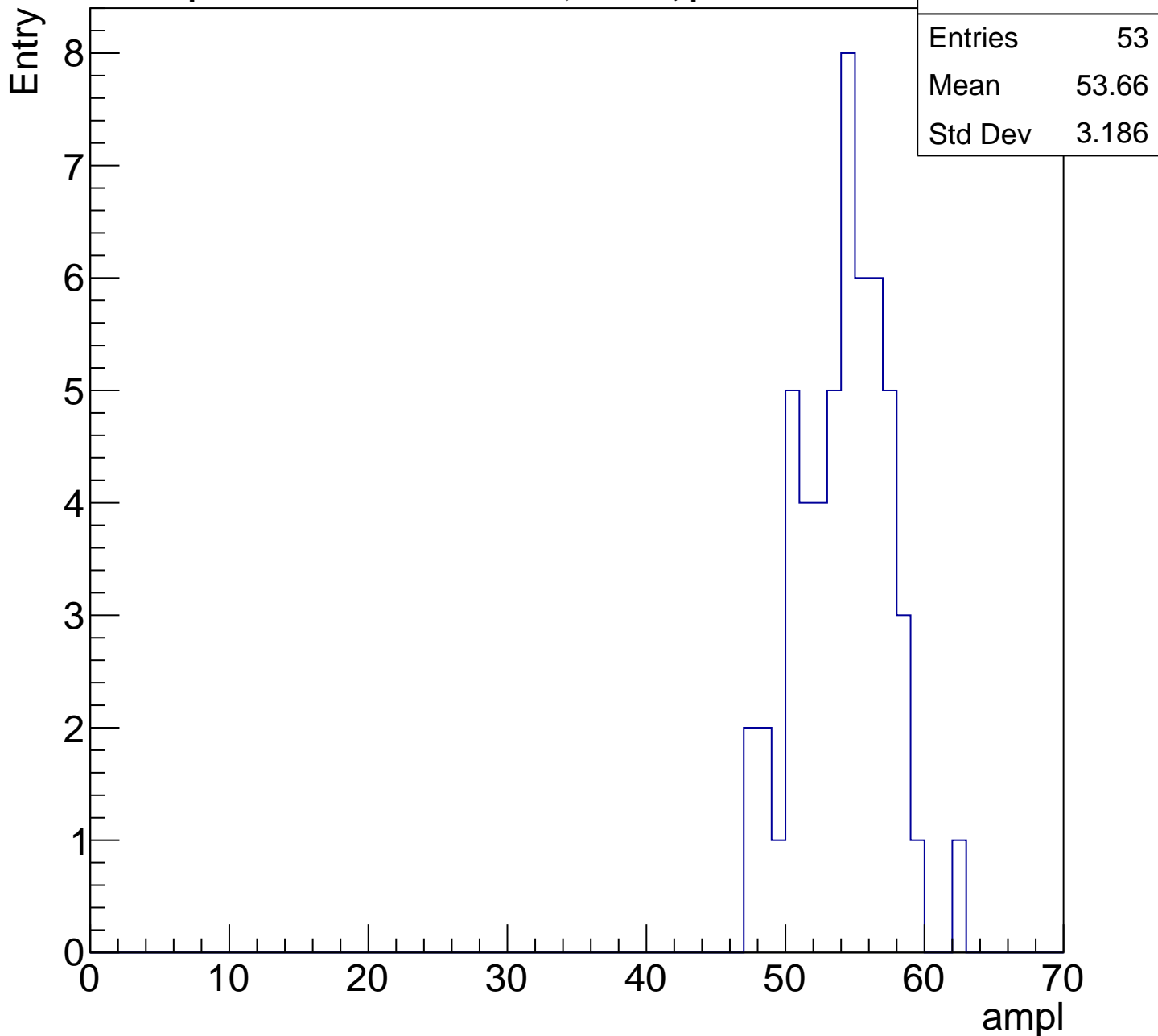
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U5-ch16, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

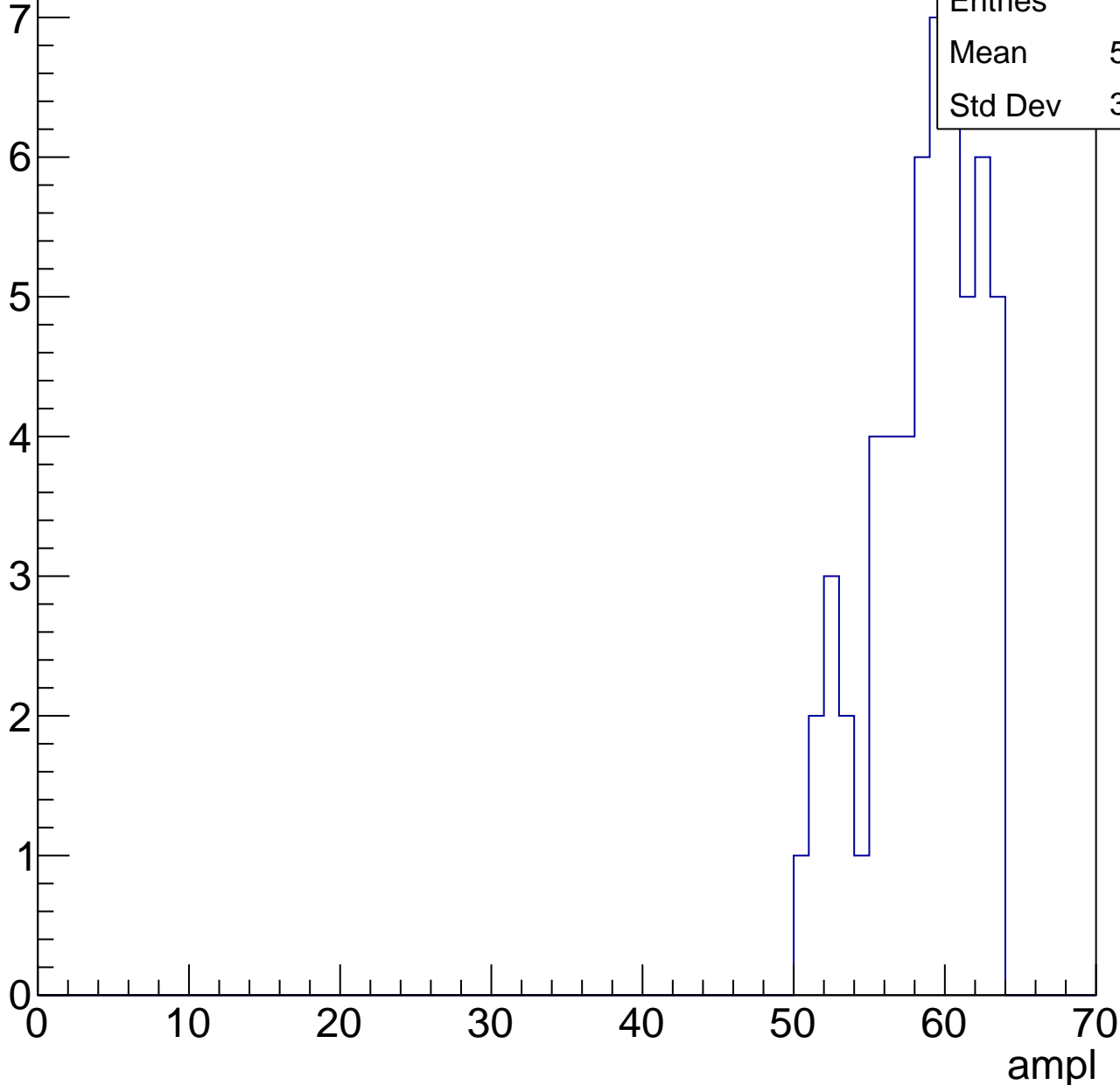


# B1L102S, U5-ch16, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	58.12
Std Dev	3.485

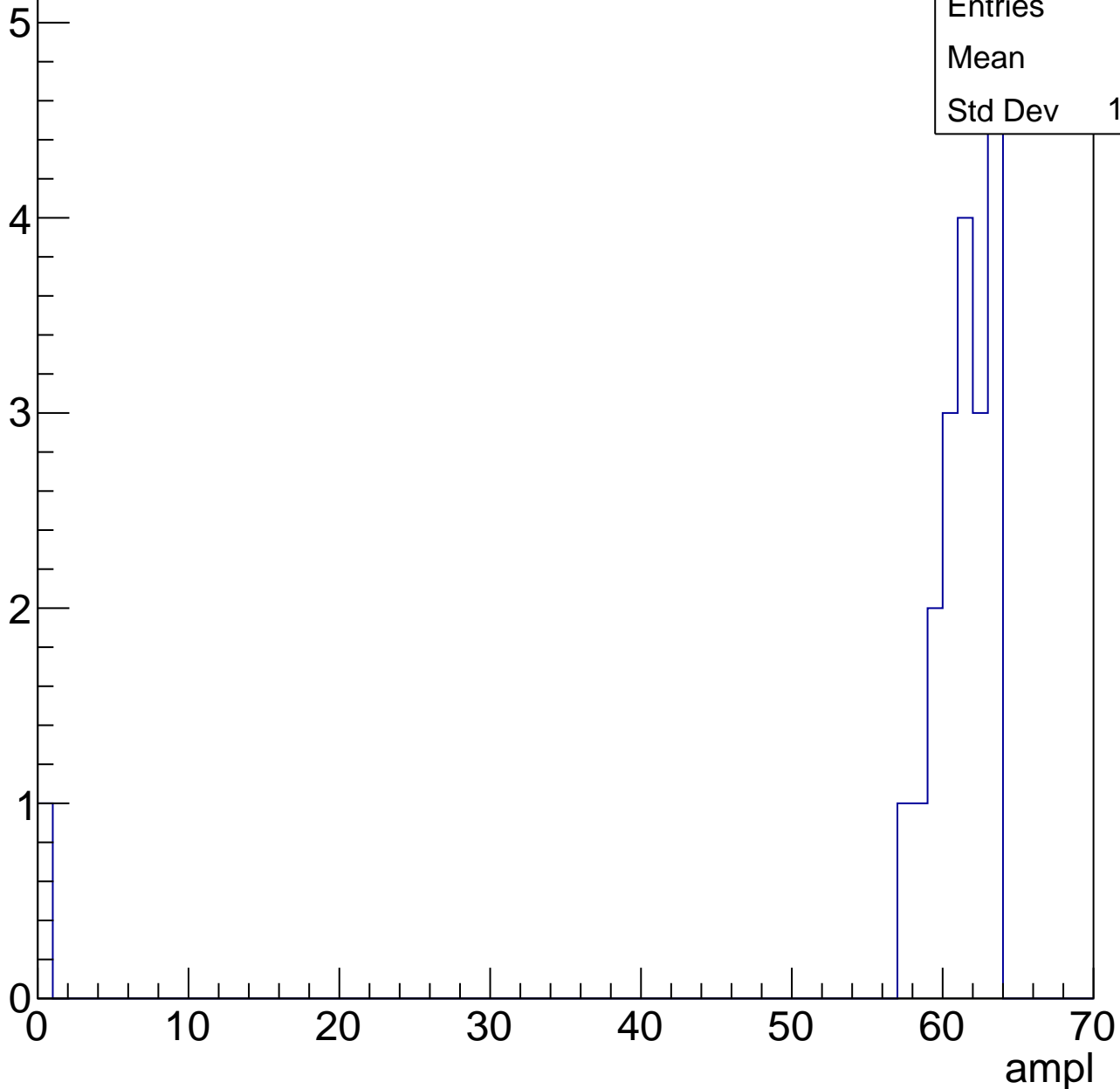


# B1L102S, U5-ch16, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	20
Mean	57.9
Std Dev	13.39

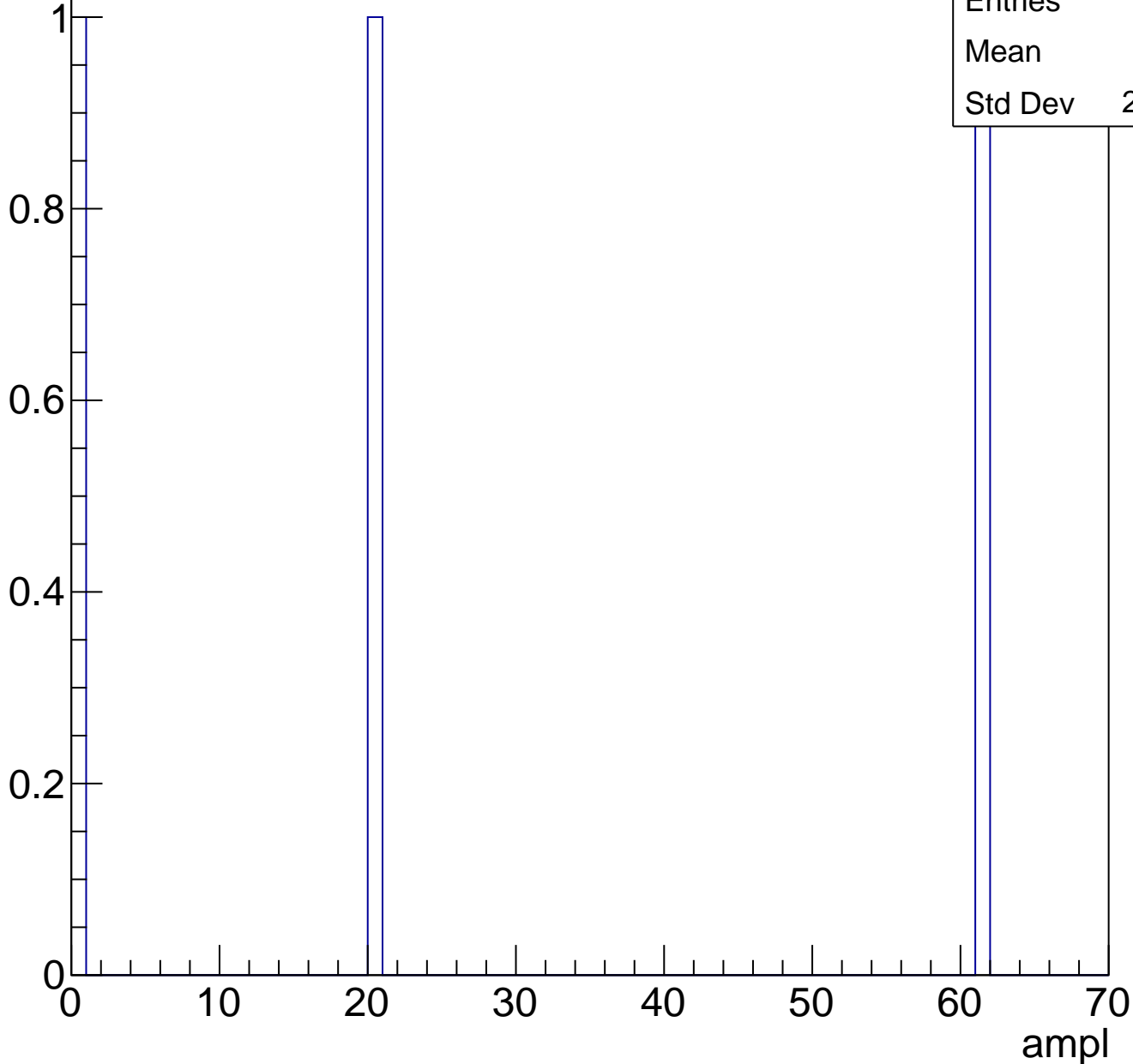




# B1L102S, U5-ch16, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U5-ch17, adc0

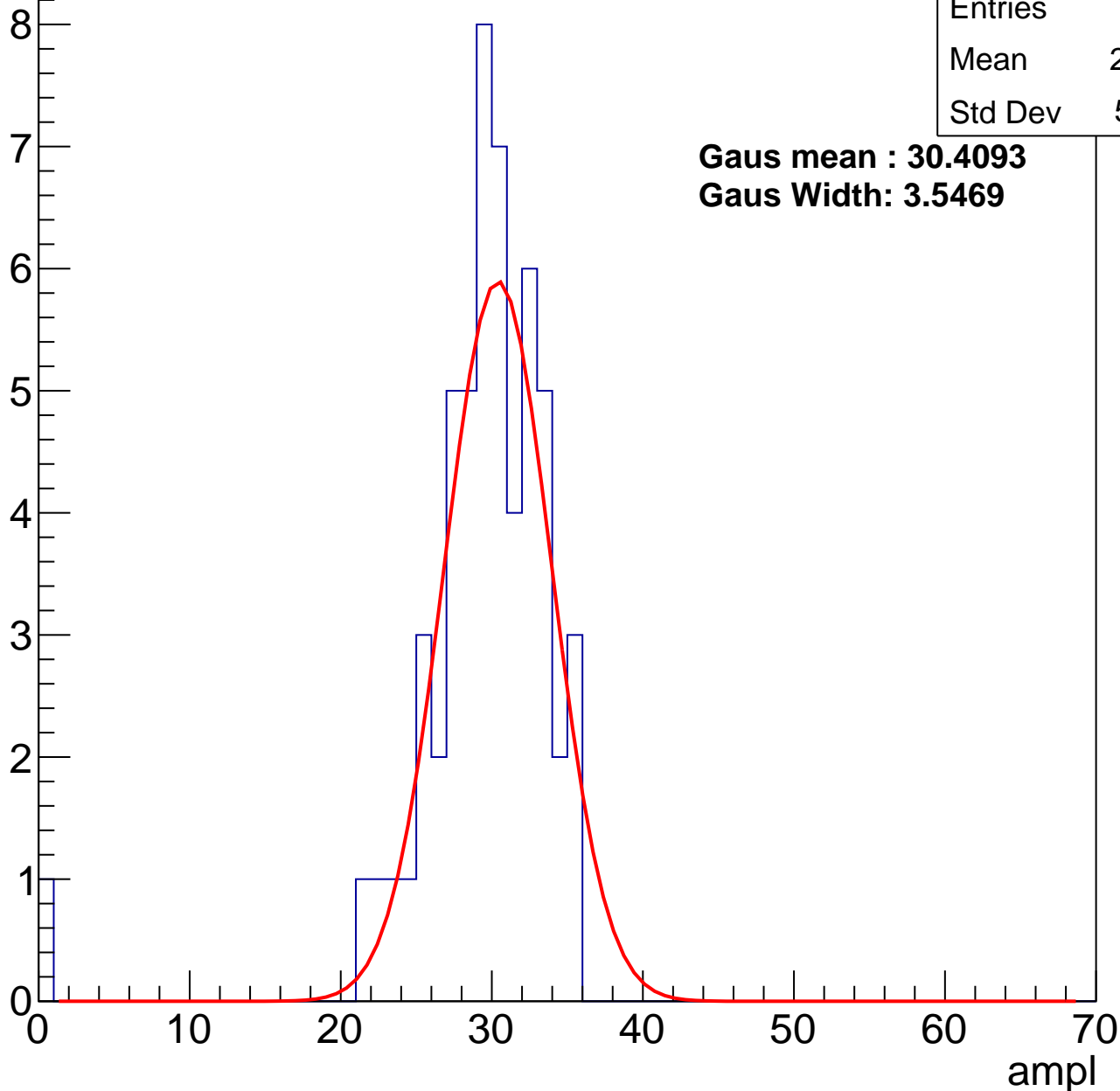
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	28.87
Std Dev	5.081

**Gaus mean : 30.4093**

**Gaus Width: 3.5469**



# B1L102S, U5-ch17, adc1

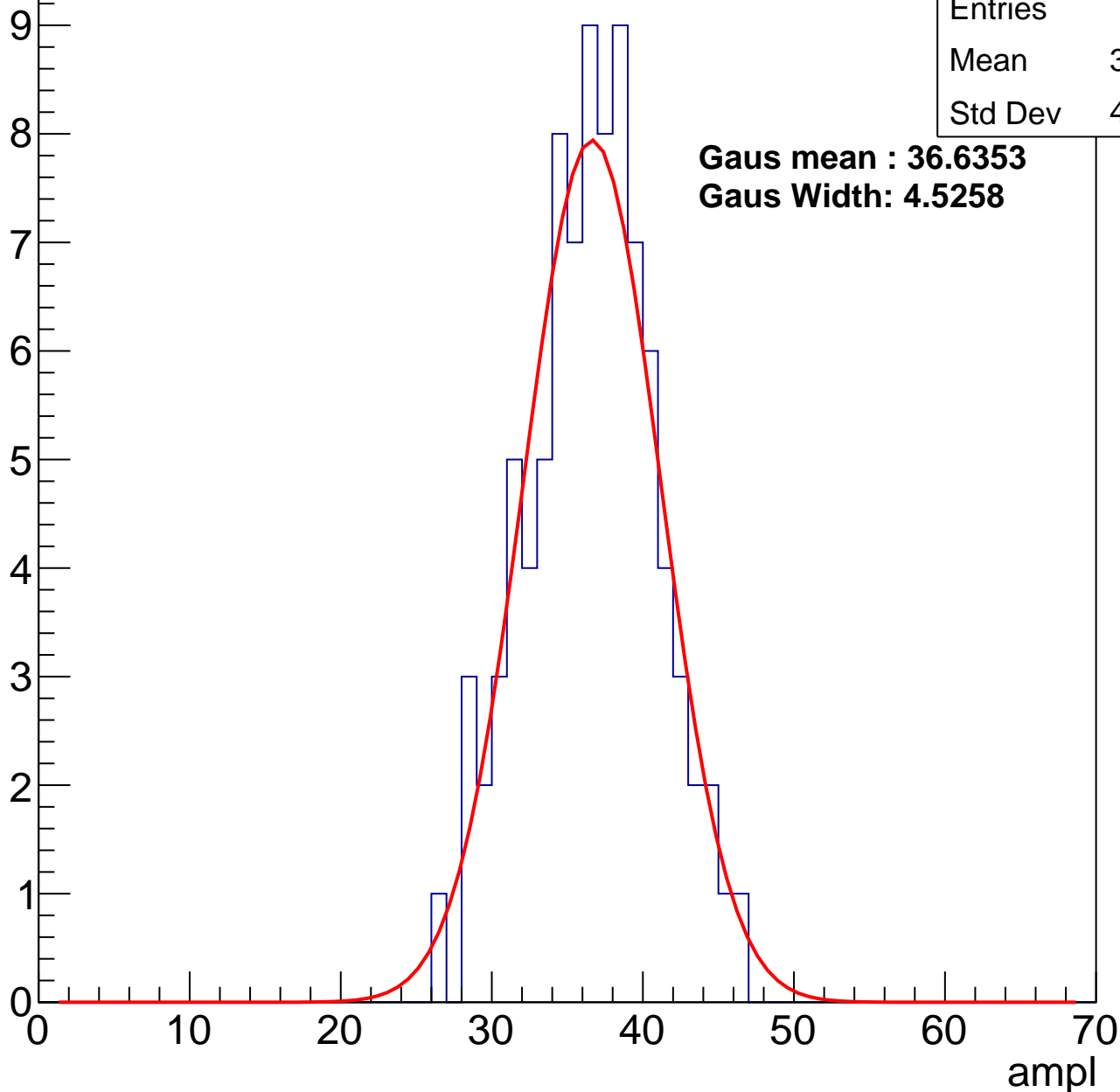
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	90
Mean	36.14
Std Dev	4.199

**Gaus mean : 36.6353**

**Gaus Width: 4.5258**

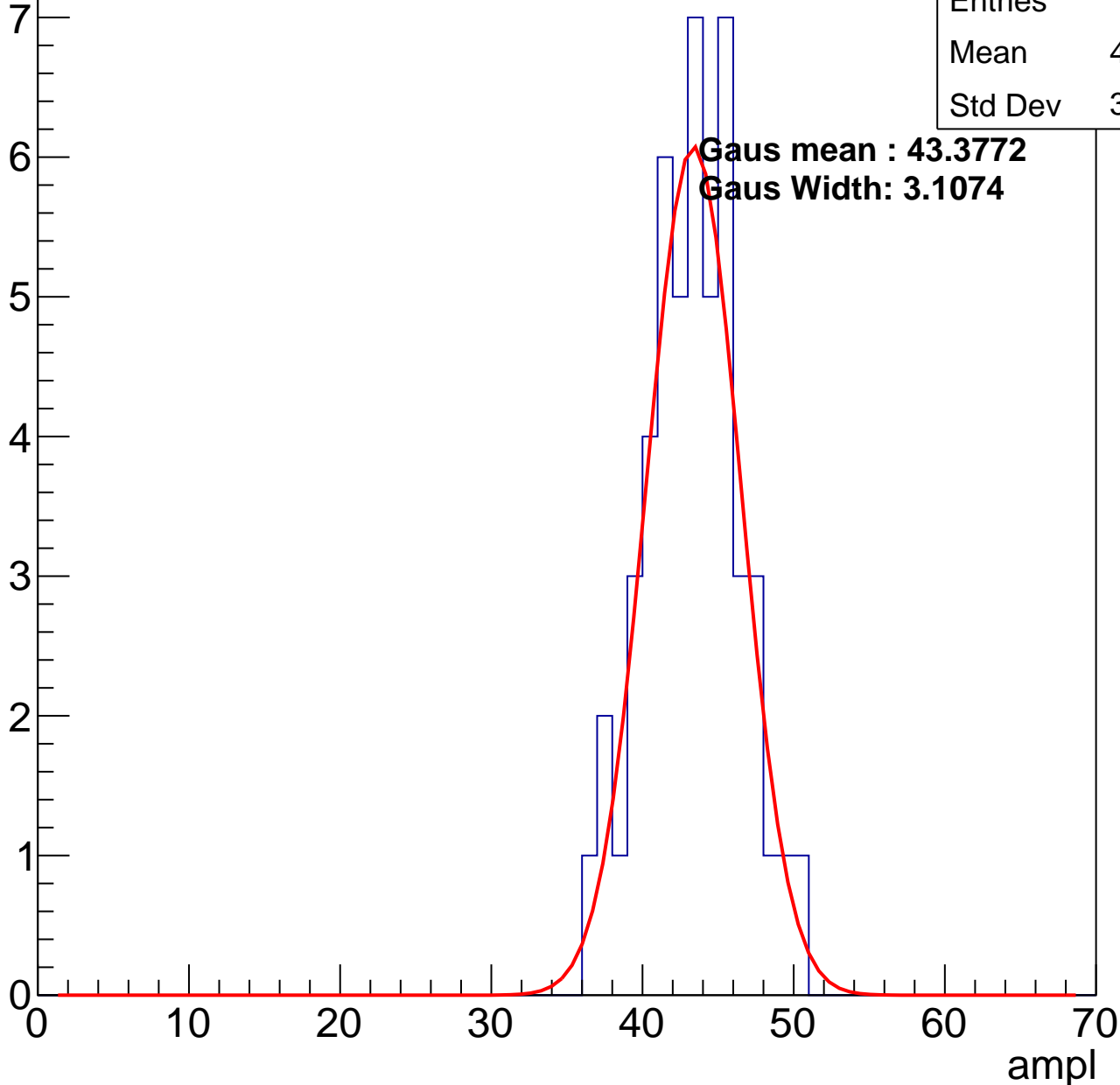


# B1L102S, U5-ch17, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	42.86
Std Dev	3.086

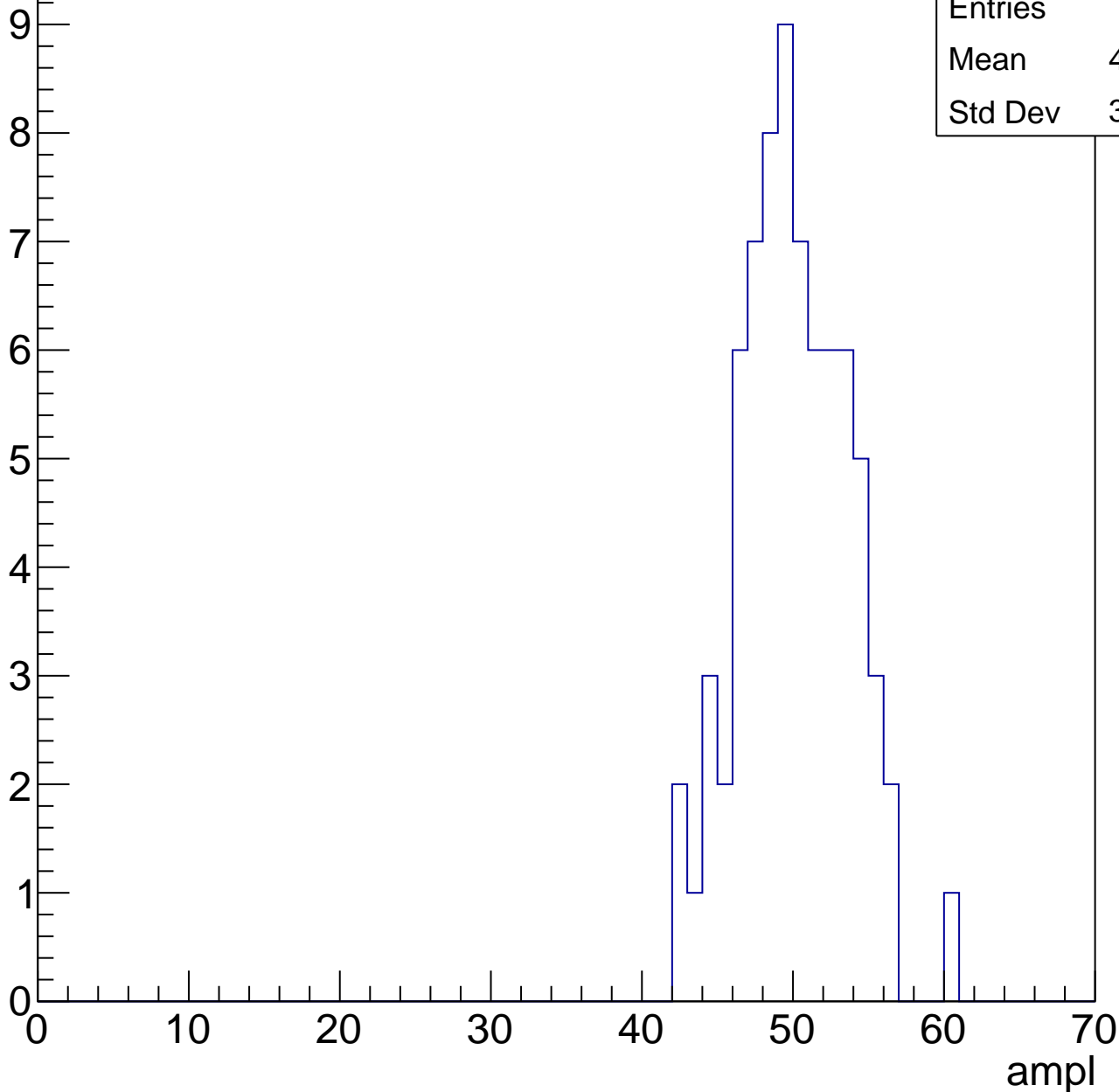


# B1L102S, U5-ch17, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

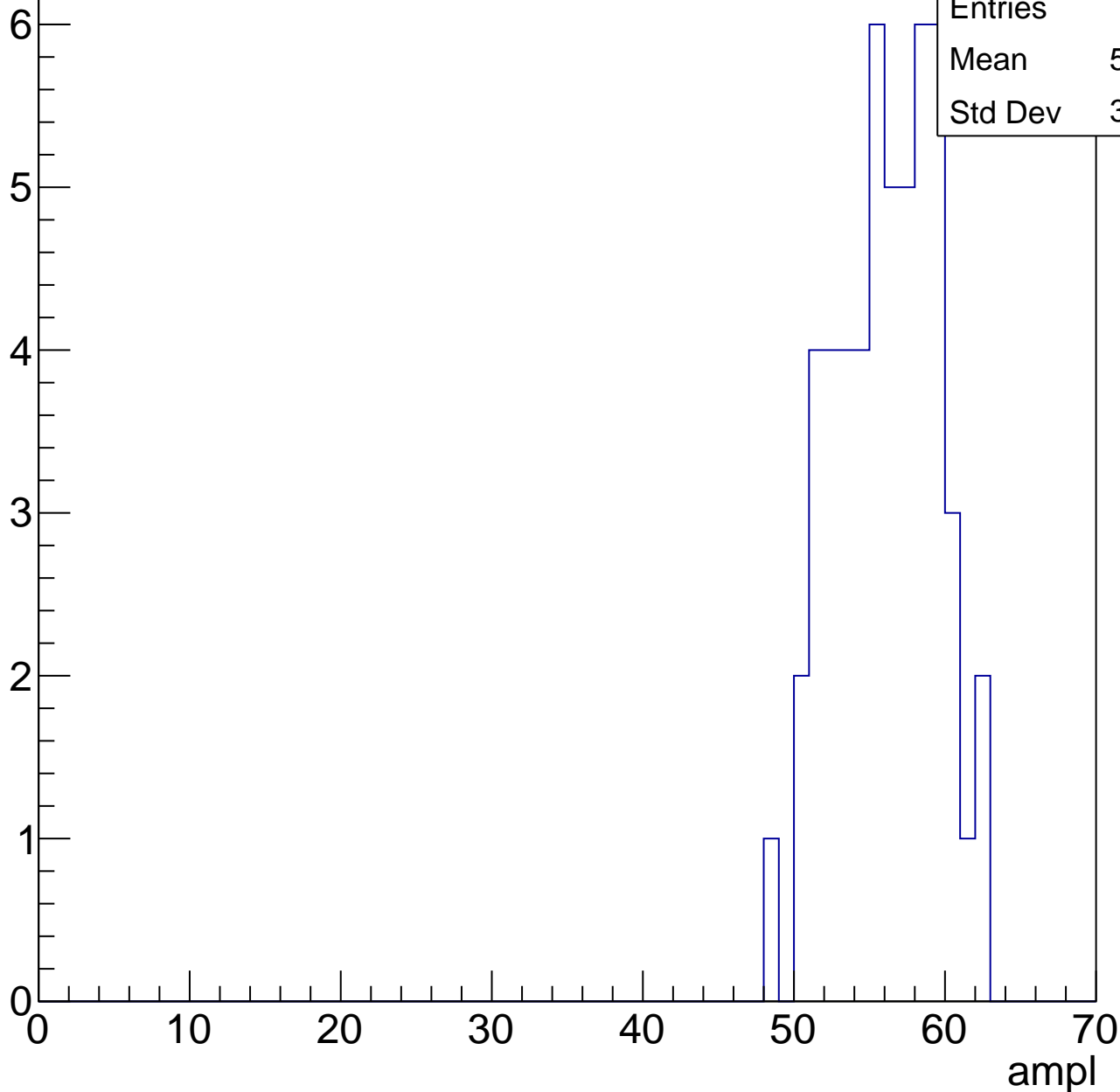
Entries	74
Mean	49.62
Std Dev	3.555



# B1L102S, U5-ch17, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



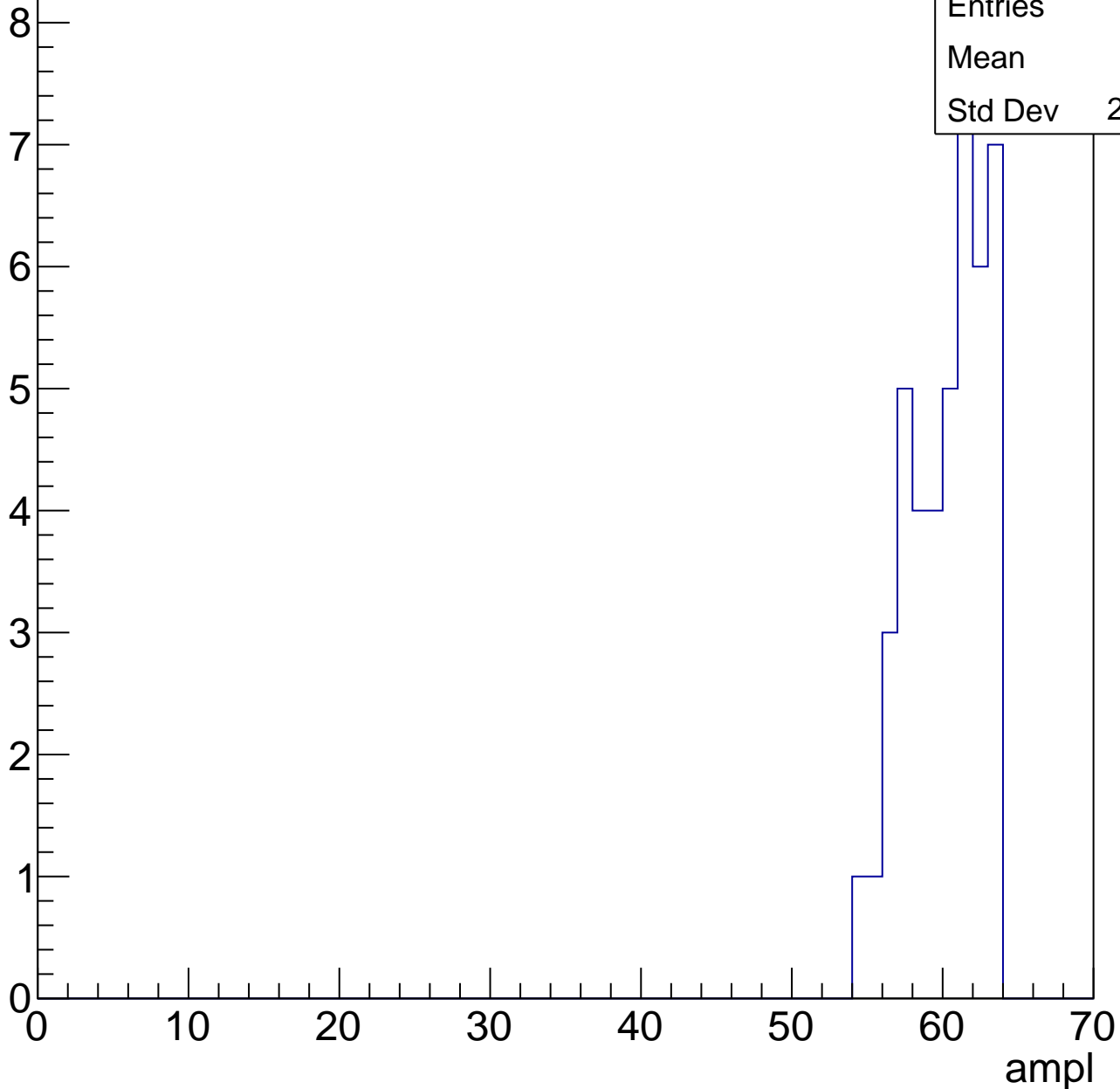
Entries	53
Mean	55.66
Std Dev	3.308

# B1L102S, U5-ch17, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

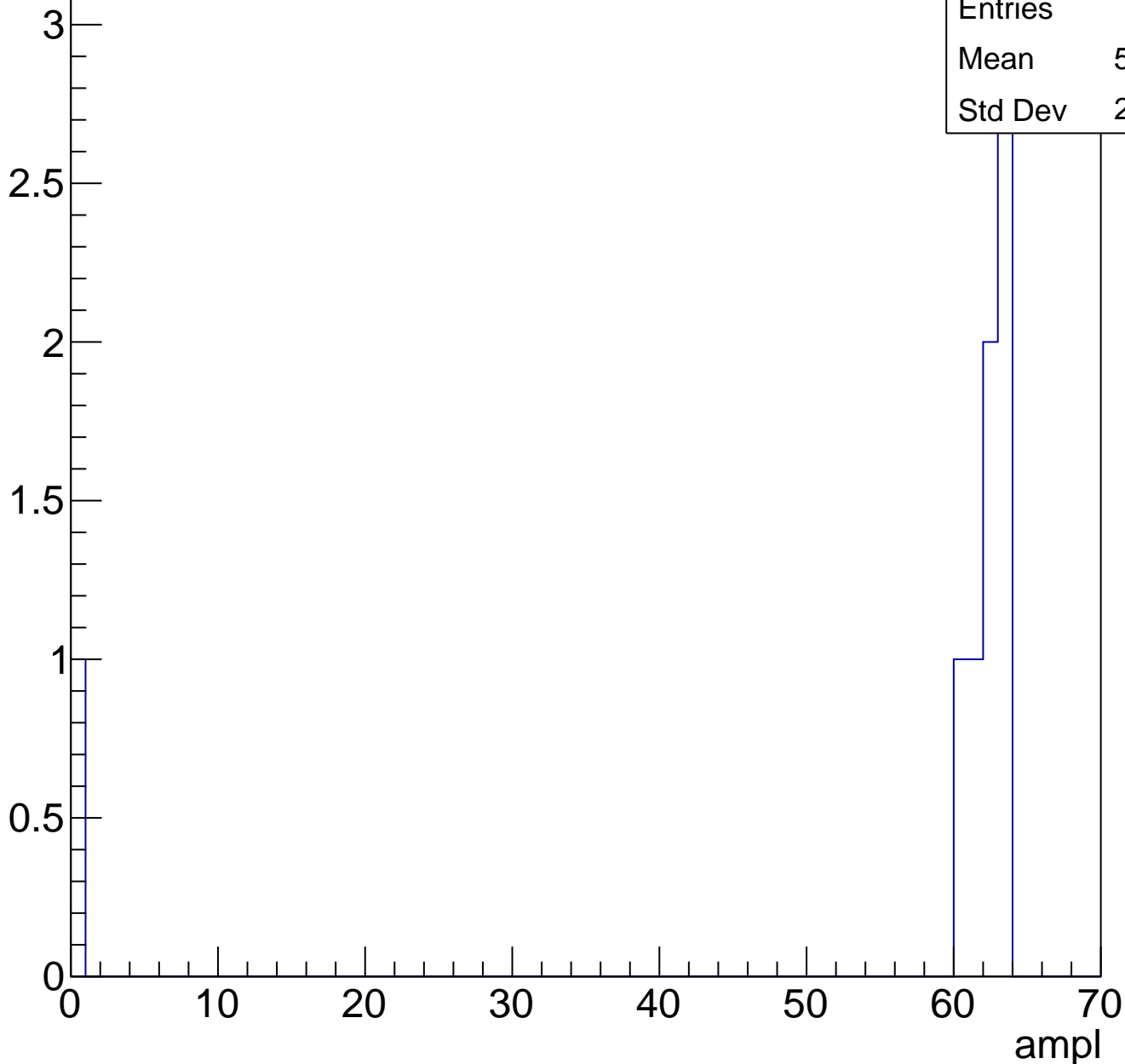
Entries	44
Mean	59.8
Std Dev	2.464



# B1L102S, U5-ch17, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U5-ch17, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L102S, U5-ch18, adc0

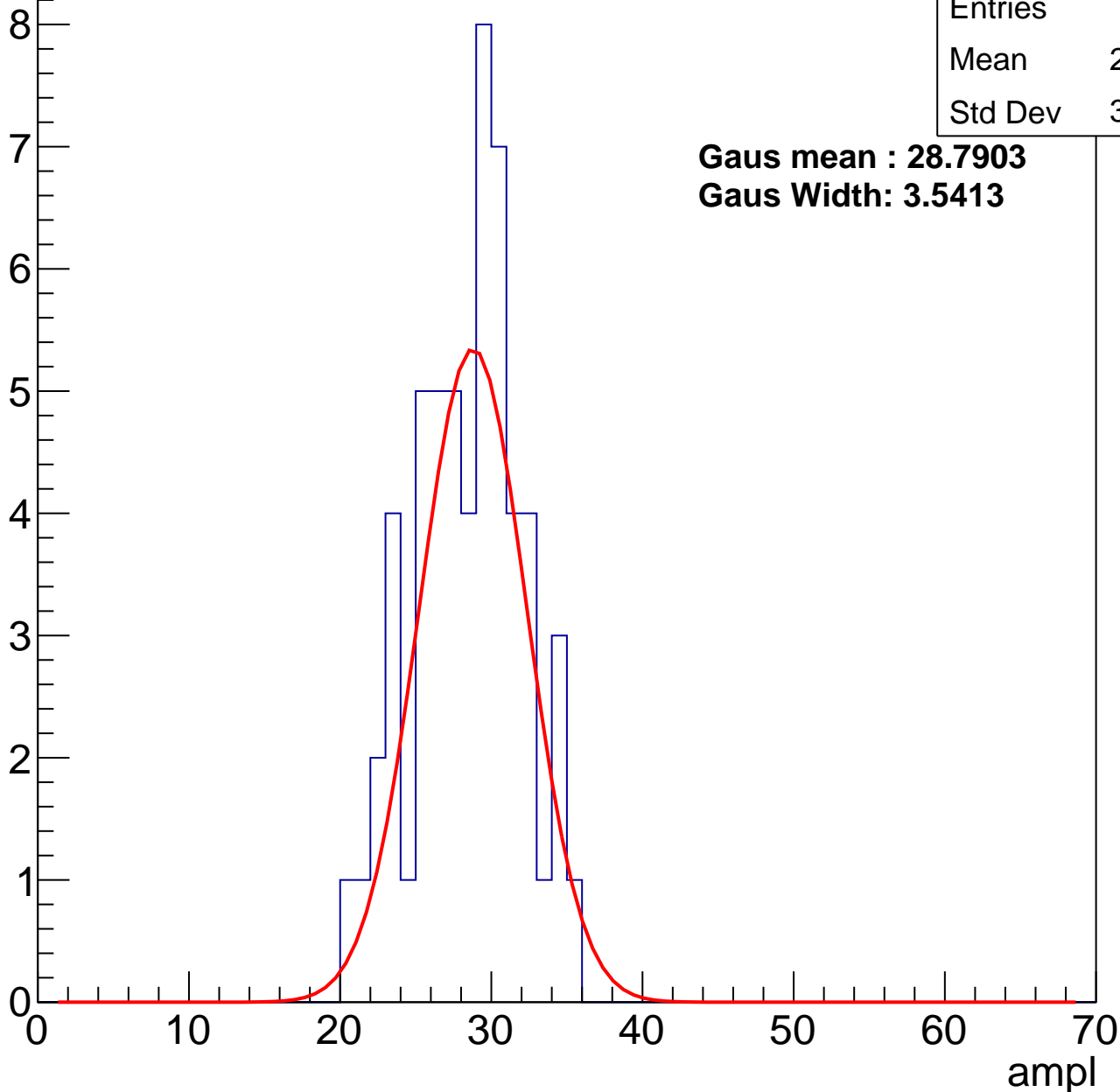
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	27.98
Std Dev	3.508

**Gaus mean : 28.7903**

**Gaus Width: 3.5413**



# B1L102S, U5-ch18, adc1

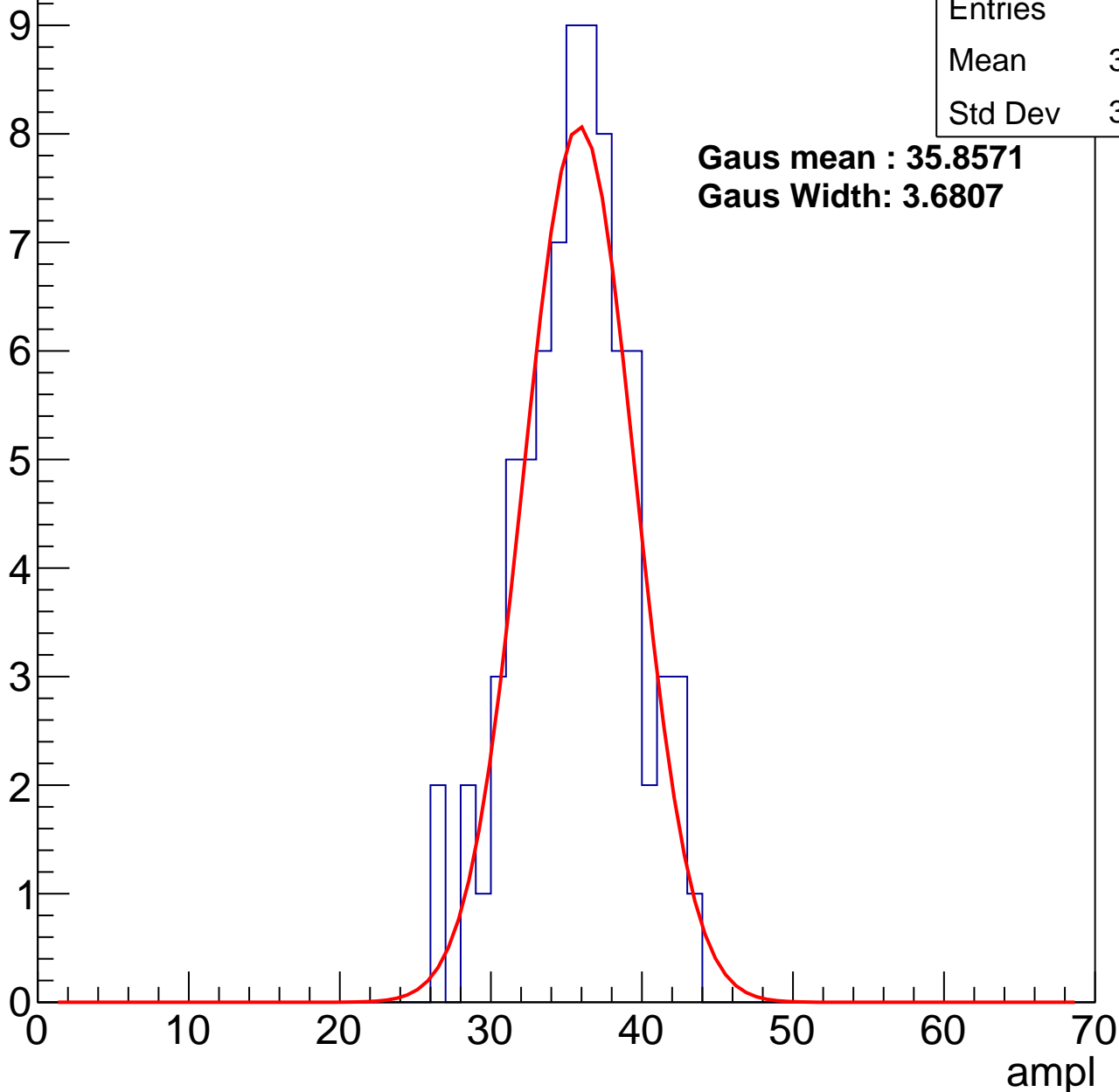
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	78
Mean	35.22
Std Dev	3.727

**Gaus mean : 35.8571**

**Gaus Width: 3.6807**



# B1L102S, U5-ch18, adc2

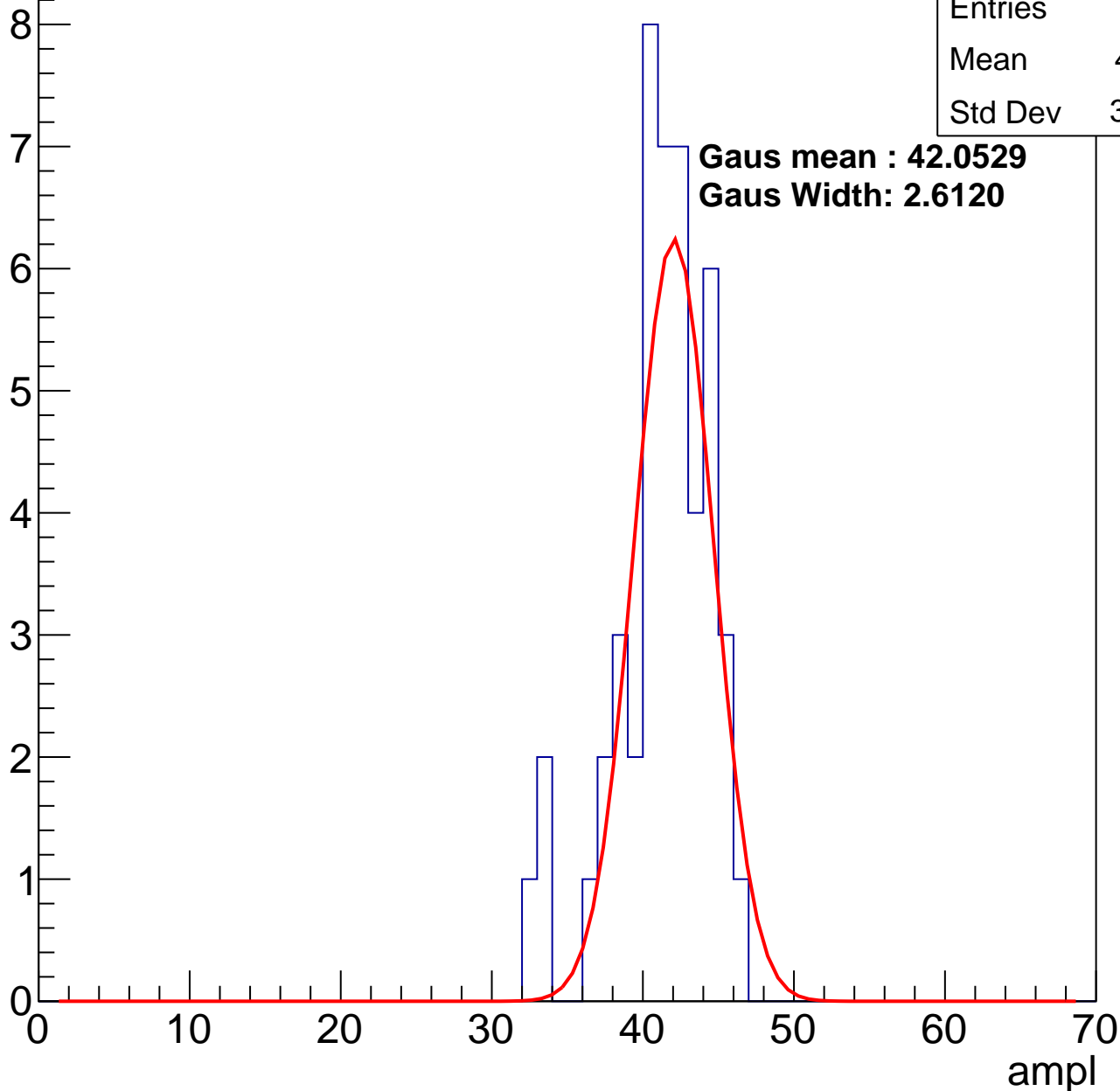
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	47
Mean	40.81
Std Dev	3.119

**Gaus mean : 42.0529**

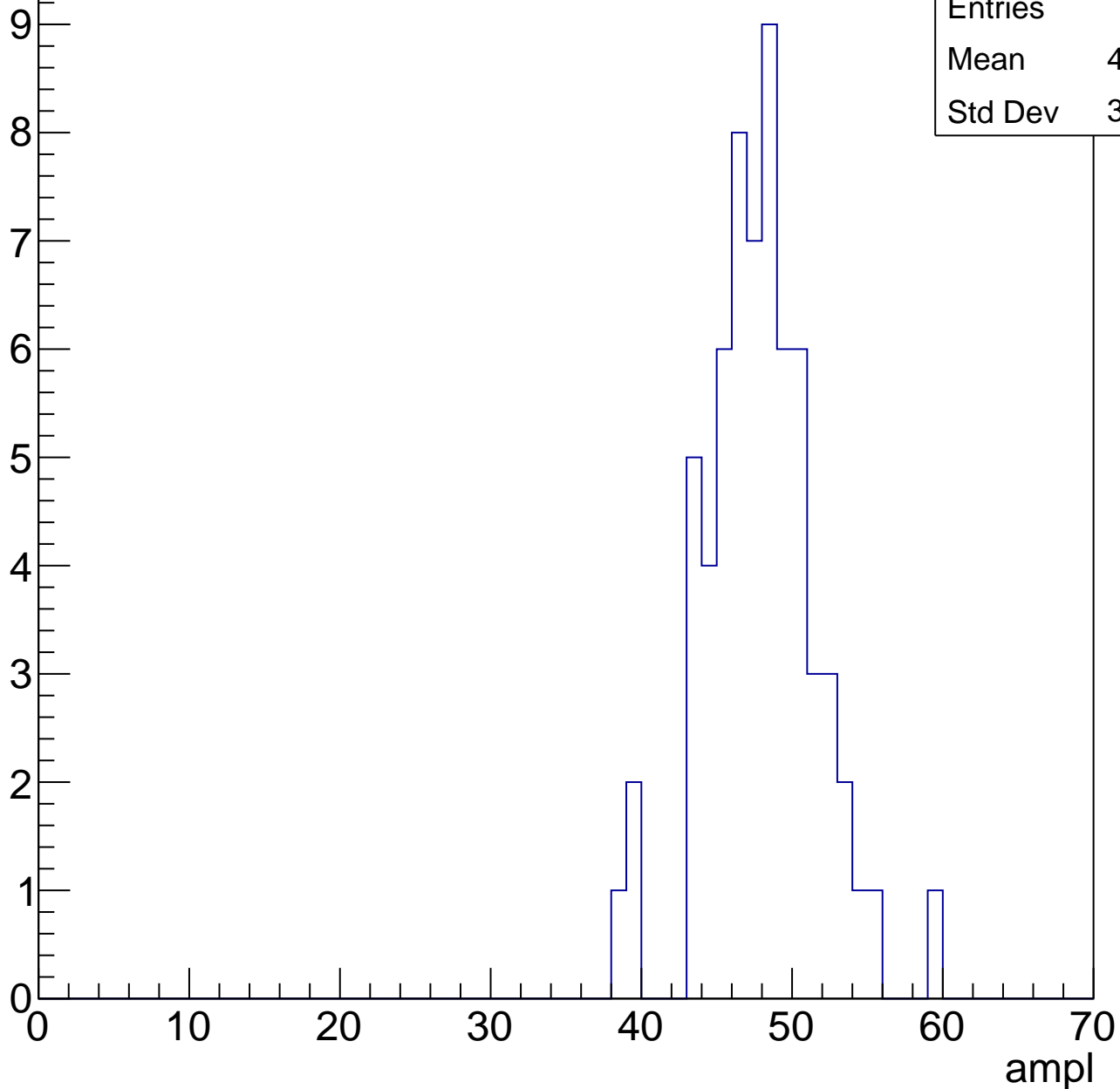
**Gaus Width: 2.6120**



# B1L102S, U5-ch18, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



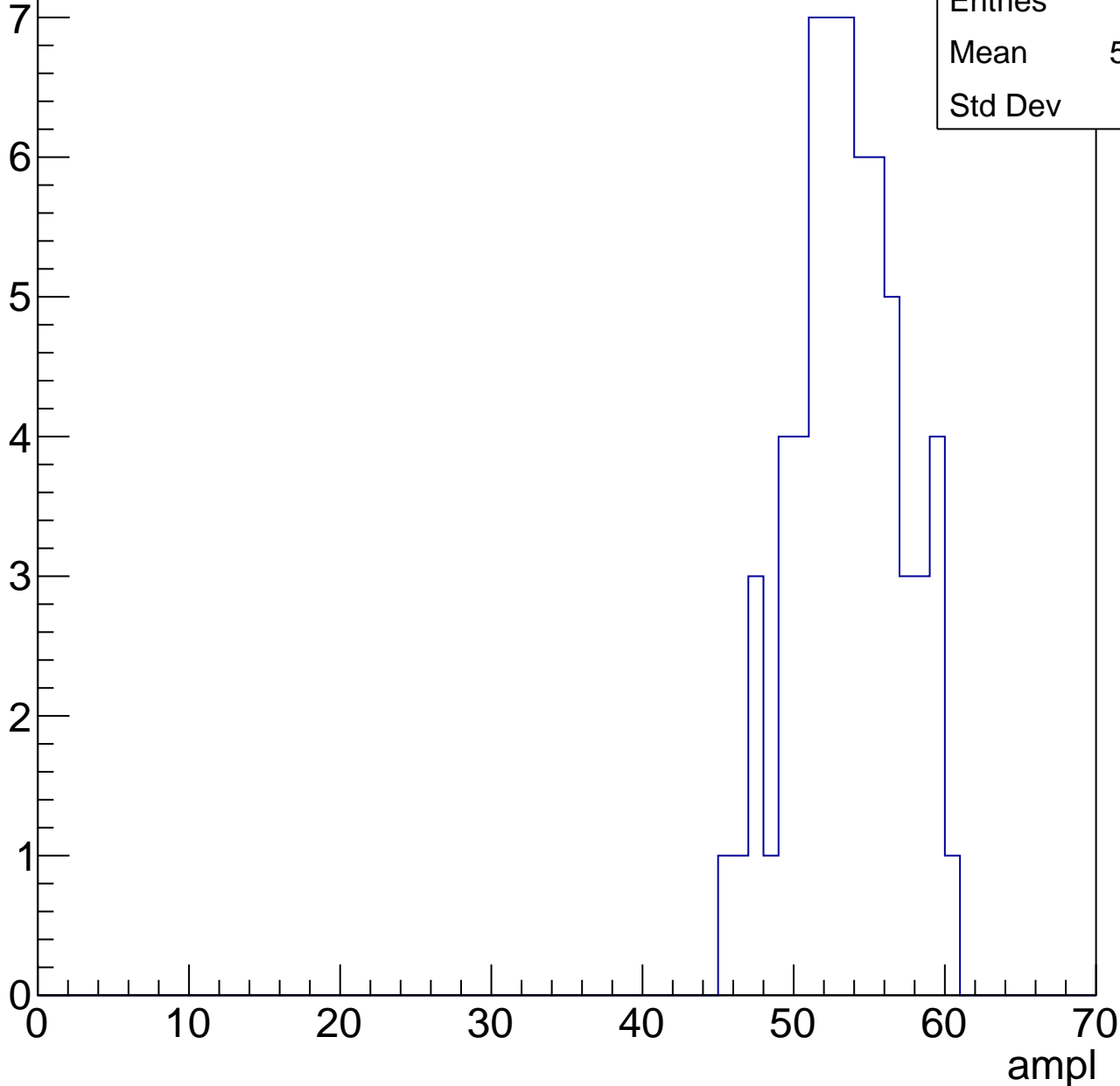
Entries	65
Mean	47.43
Std Dev	3.688

# B1L102S, U5-ch18, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	53.06
Std Dev	3.5

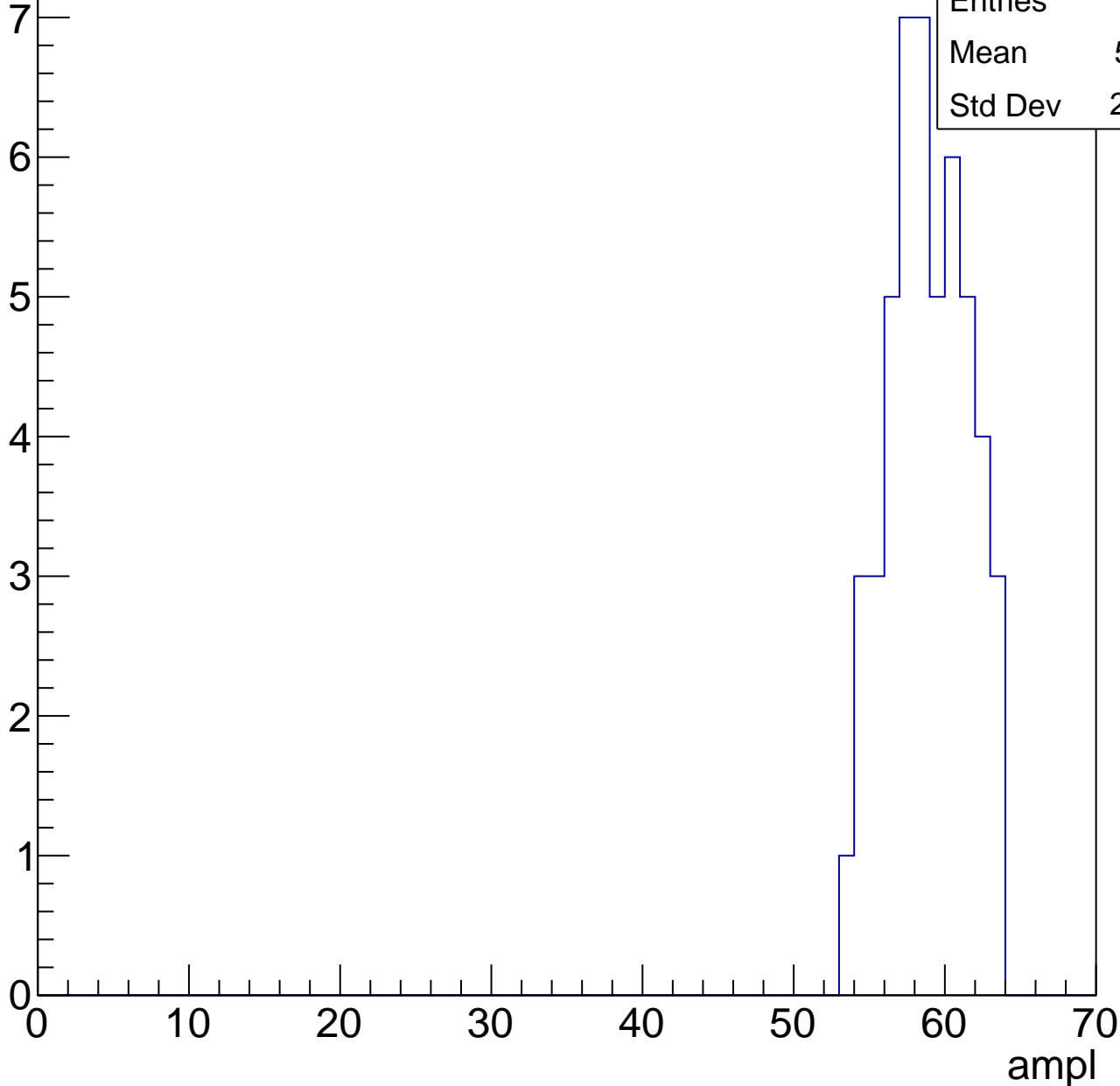


# B1L102S, U5-ch18, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	58.41
Std Dev	2.602

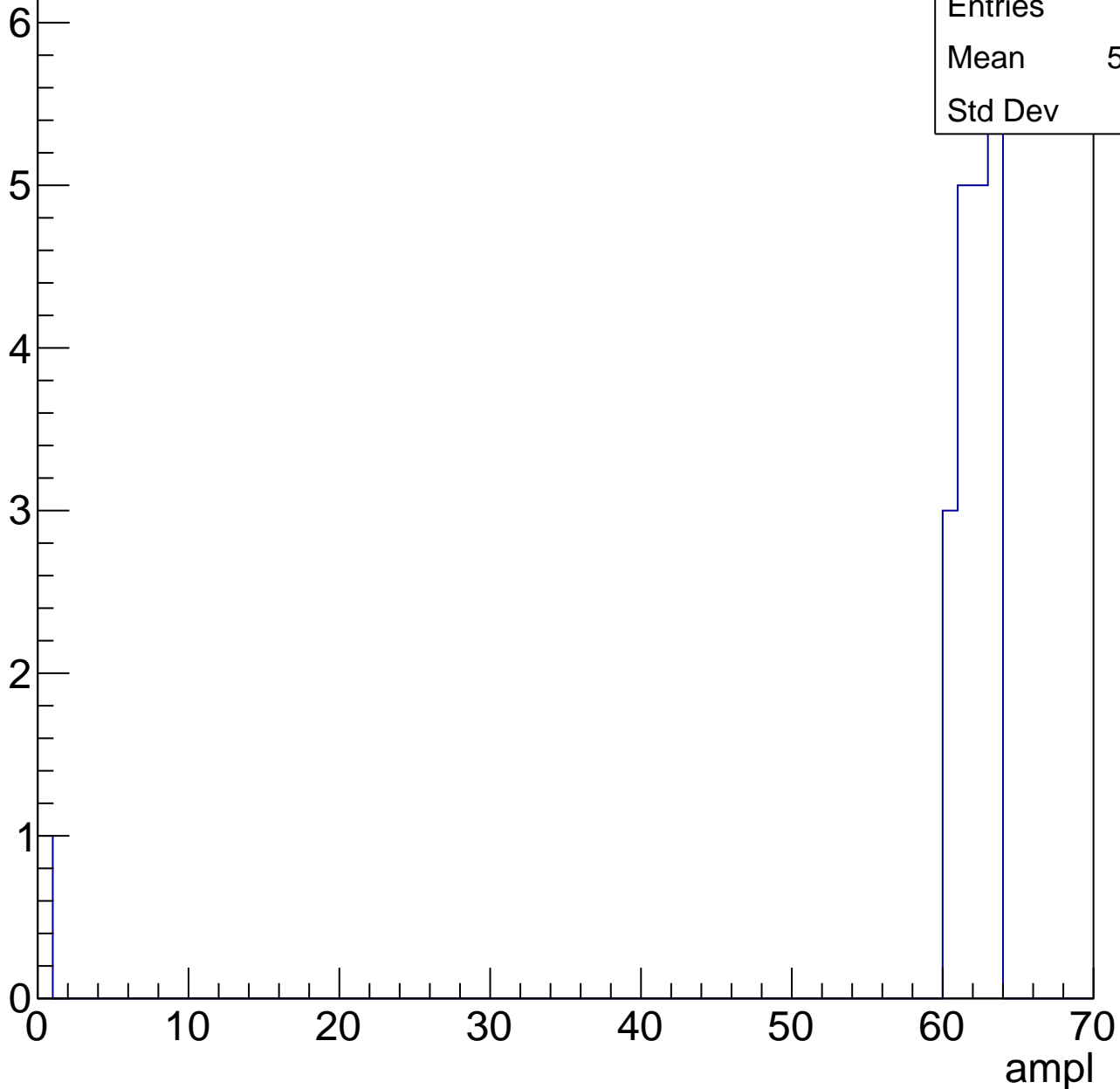


# B1L102S, U5-ch18, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	20
Mean	58.65
Std Dev	13.5





# B1L102S, U5-ch18, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U5-ch19, adc0

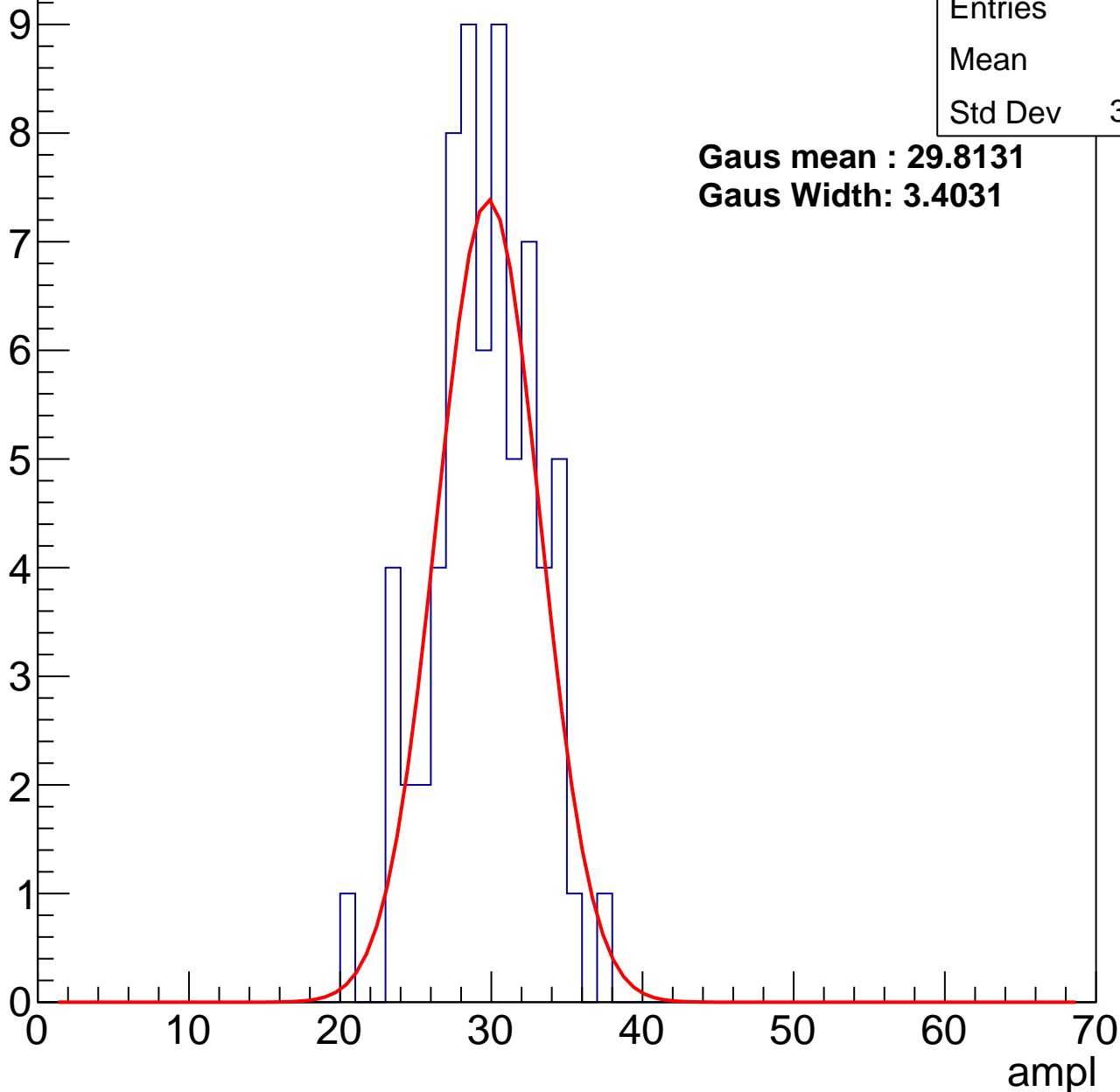
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	29.1
Std Dev	3.353

**Gaus mean : 29.8131**

**Gaus Width: 3.4031**



# B1L102S, U5-ch19, adc1

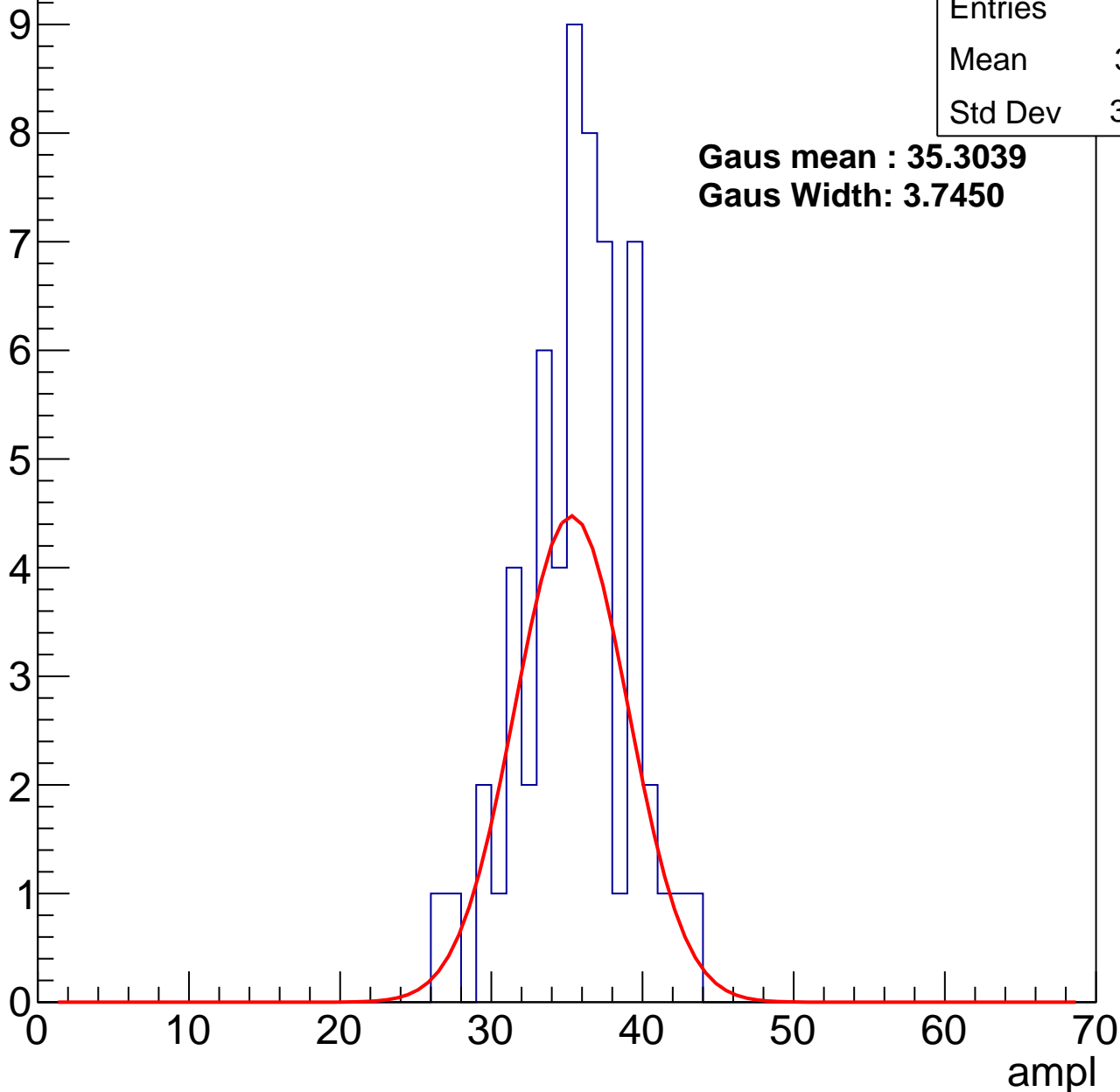
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	35.21
Std Dev	3.488

**Gaus mean : 35.3039**

**Gaus Width: 3.7450**



# B1L102S, U5-ch19, adc2

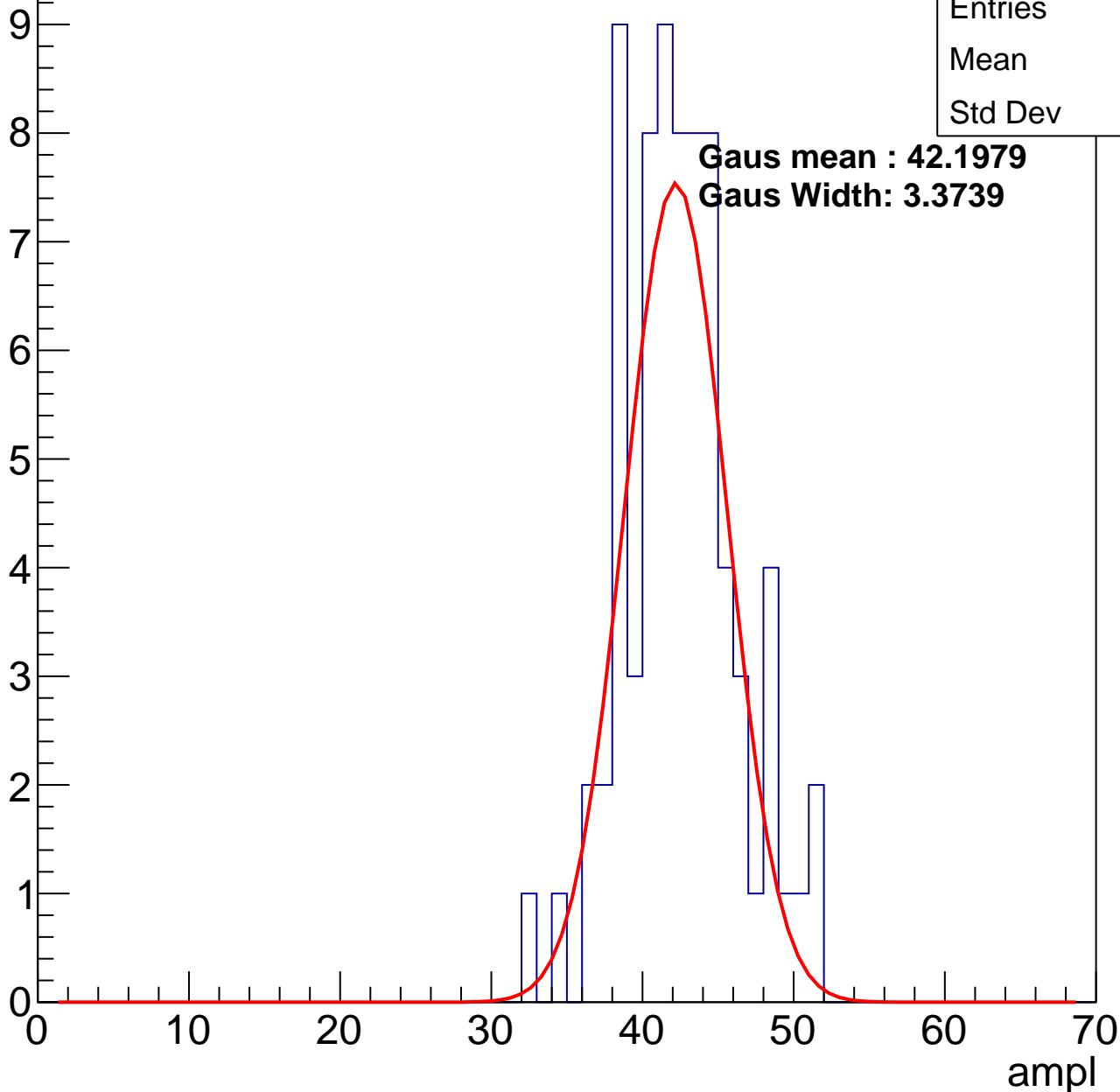
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	42
Std Dev	3.77

**Gaus mean : 42.1979**

**Gaus Width: 3.3739**

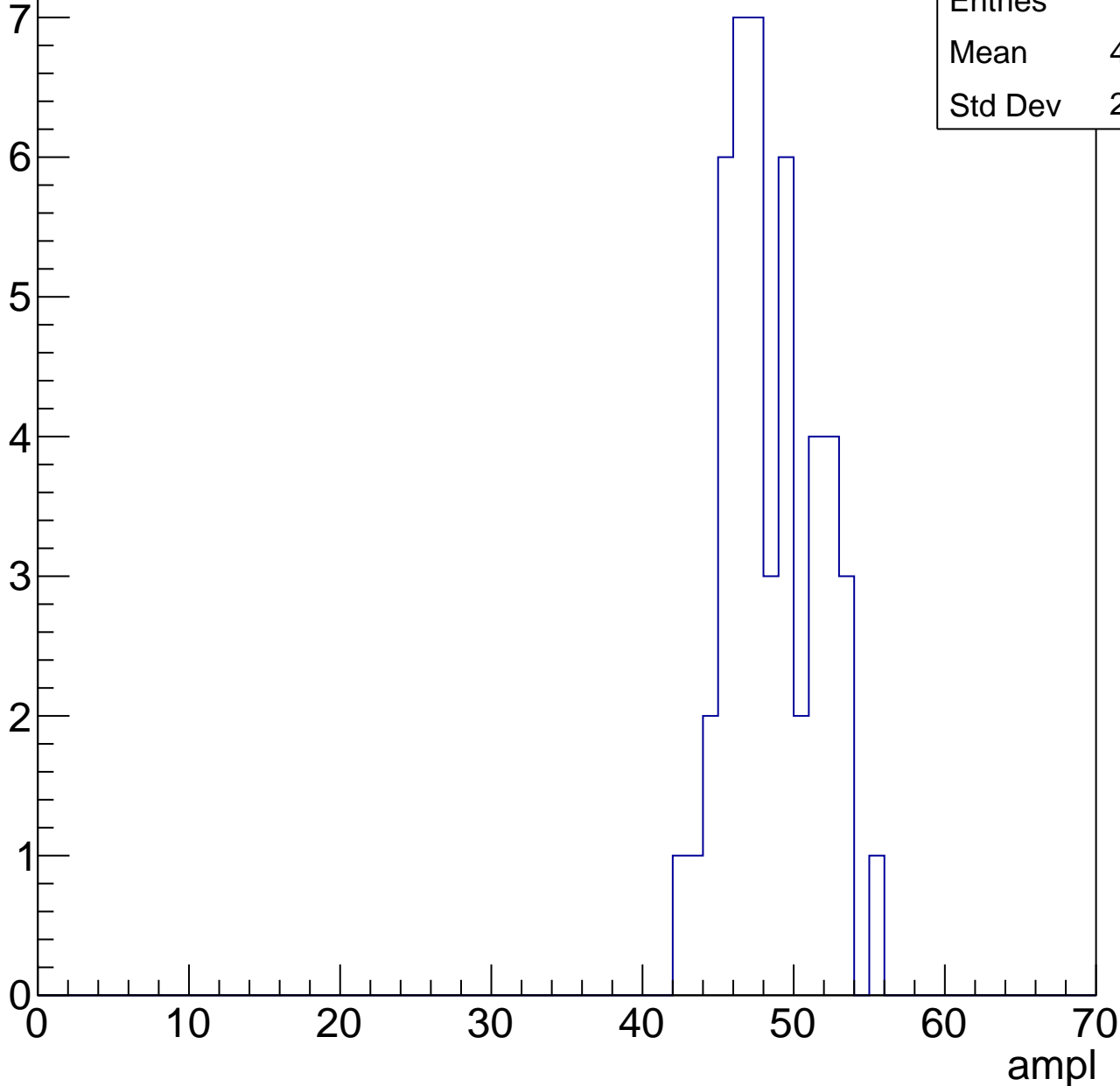


# B1L102S, U5-ch19, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

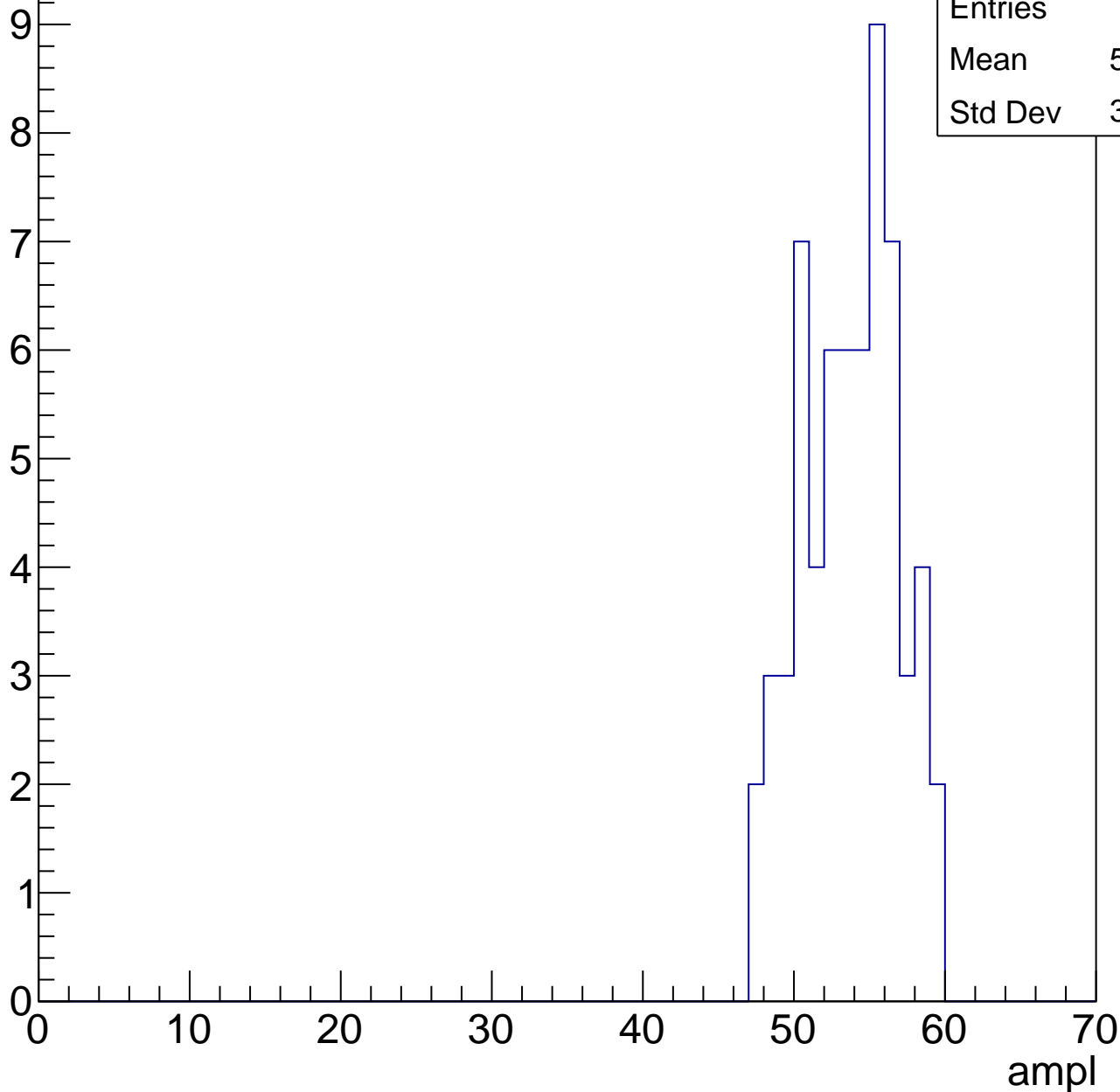
Entries	47
Mean	48.04
Std Dev	2.989



# B1L102S, U5-ch19, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

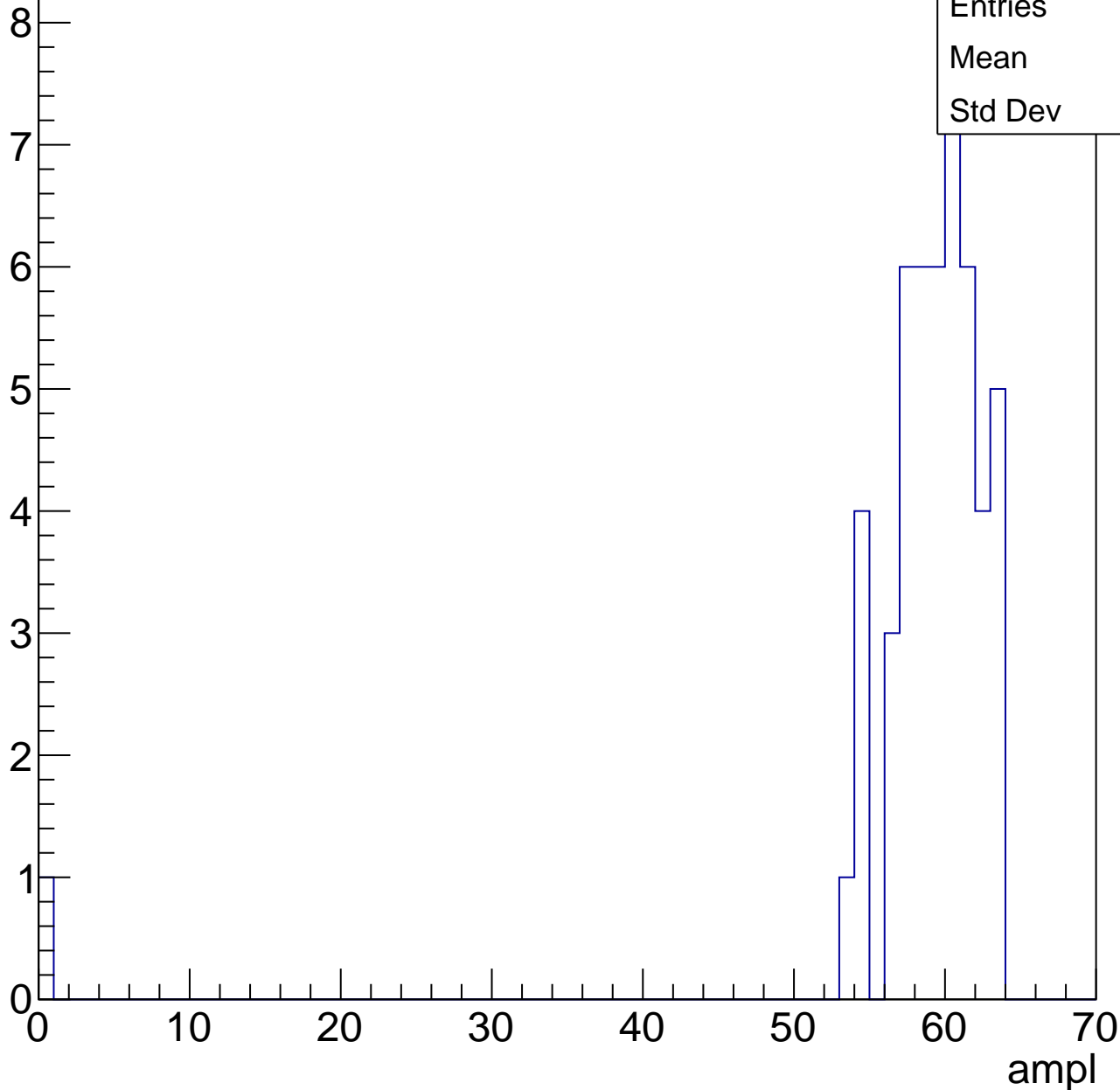


# B1L102S, U5-ch19, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	57.8
Std Dev	8.66

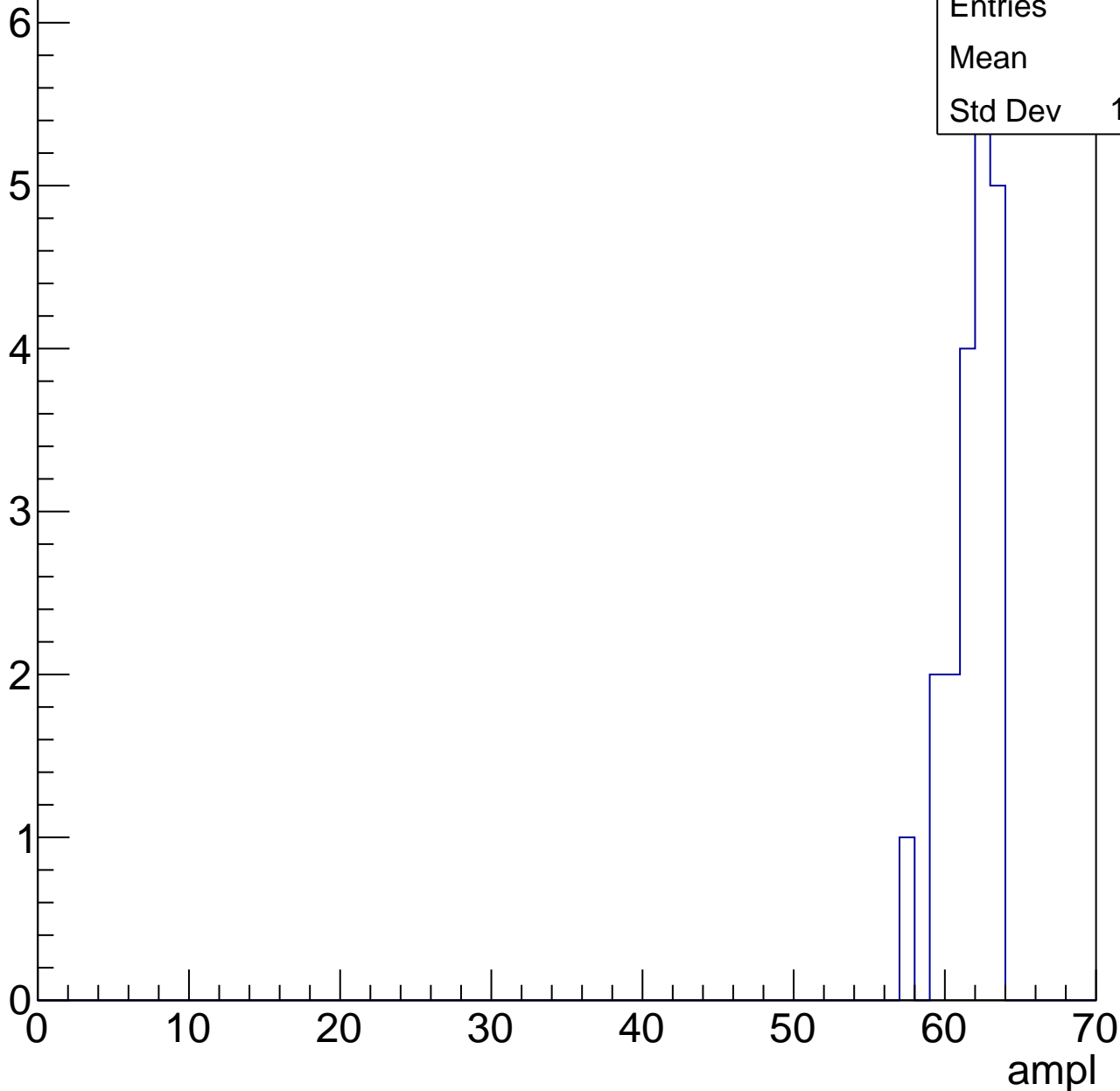


# B1L102S, U5-ch19, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	20
Mean	61.3
Std Dev	1.584





# B1L102S, U5-ch19, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	10
Std Dev	10

# B1L102S, U5-ch20, adc0

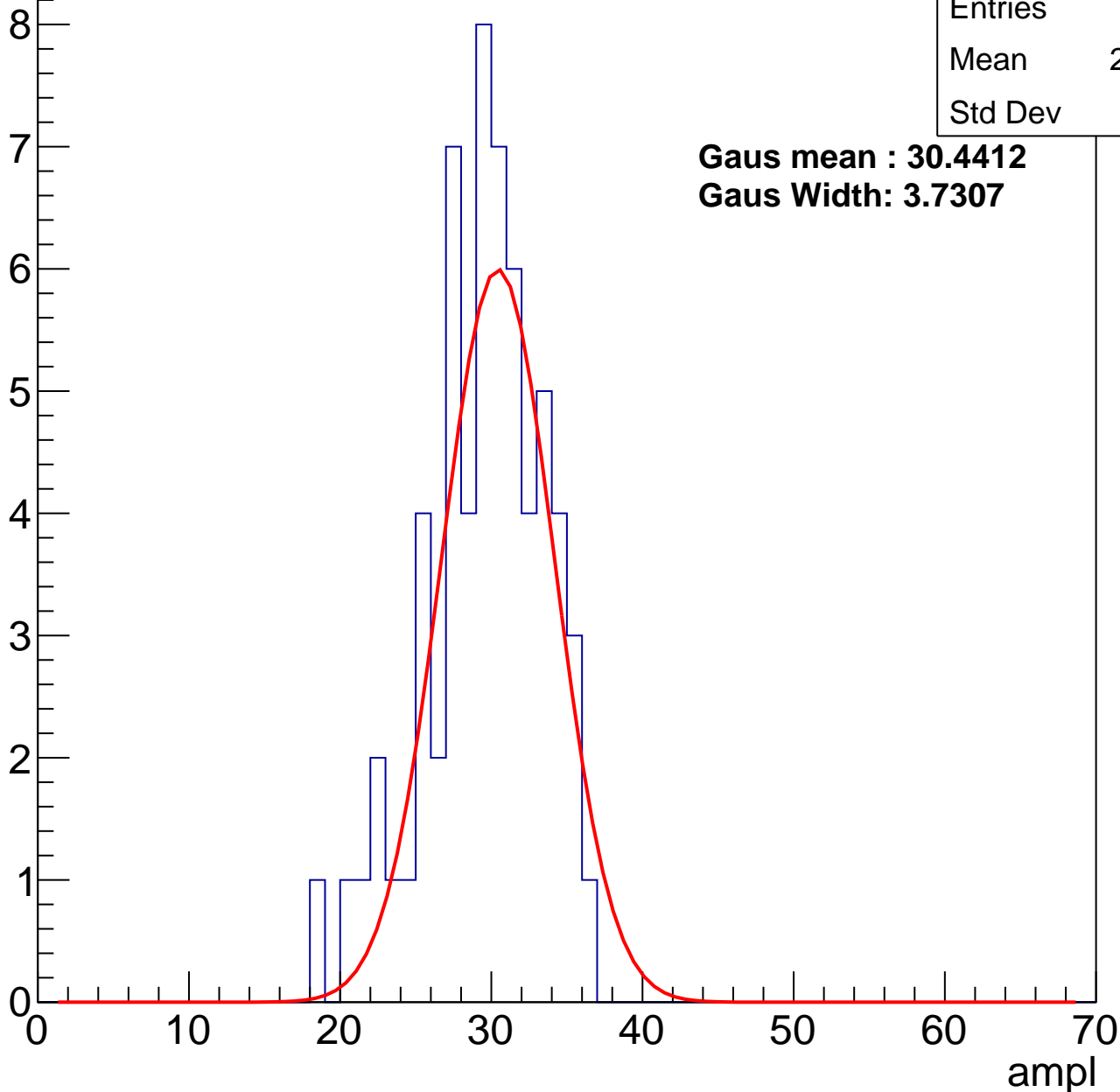
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	29.05
Std Dev	3.9

**Gaus mean : 30.4412**

**Gaus Width: 3.7307**



# B1L102S, U5-ch20, adc1

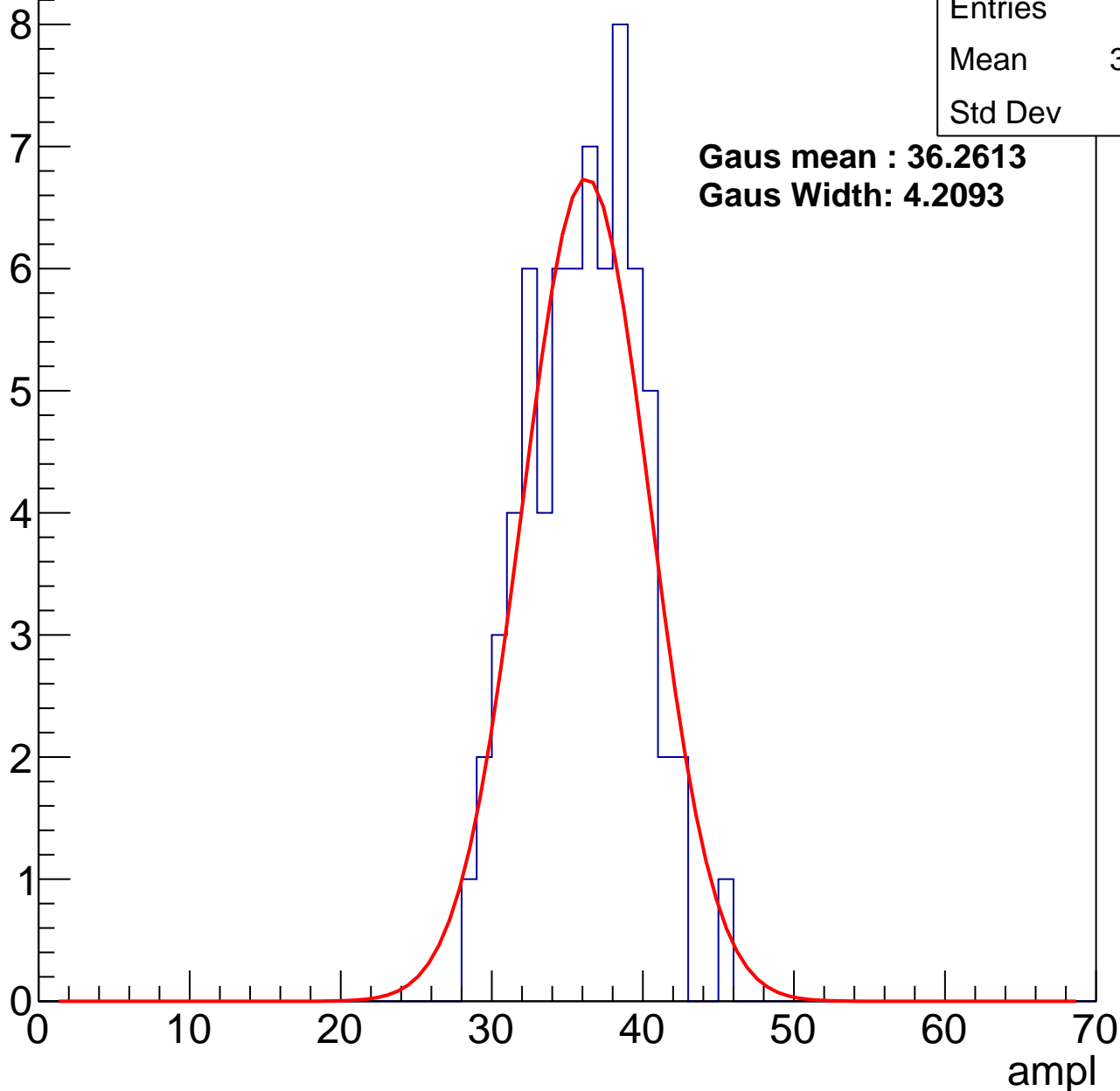
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	35.67
Std Dev	3.61

**Gaus mean : 36.2613**

**Gaus Width: 4.2093**



# B1L102S, U5-ch20, adc2

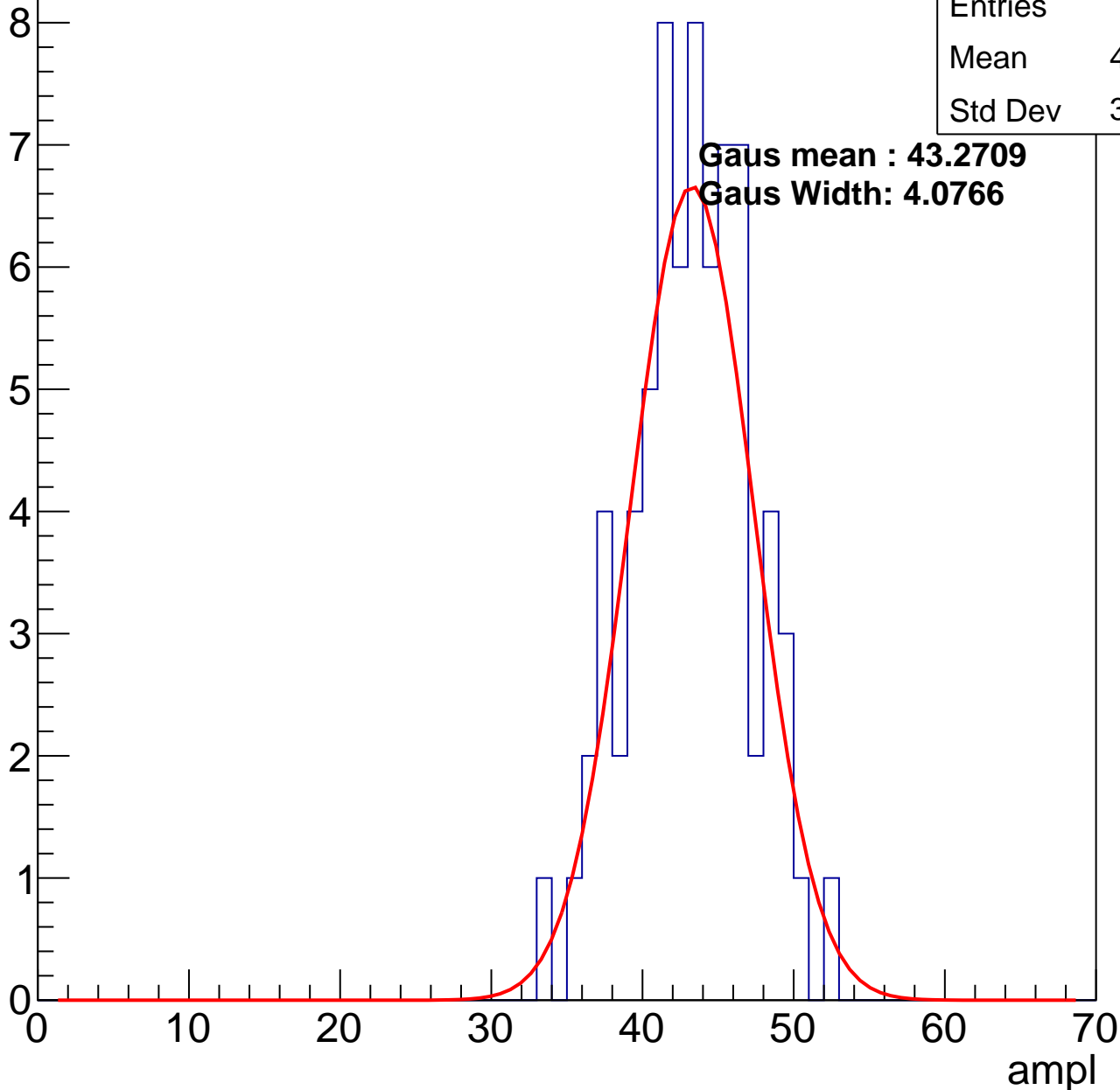
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	42.78
Std Dev	3.849

**Gaus mean : 43.2709**

**Gaus Width: 4.0766**

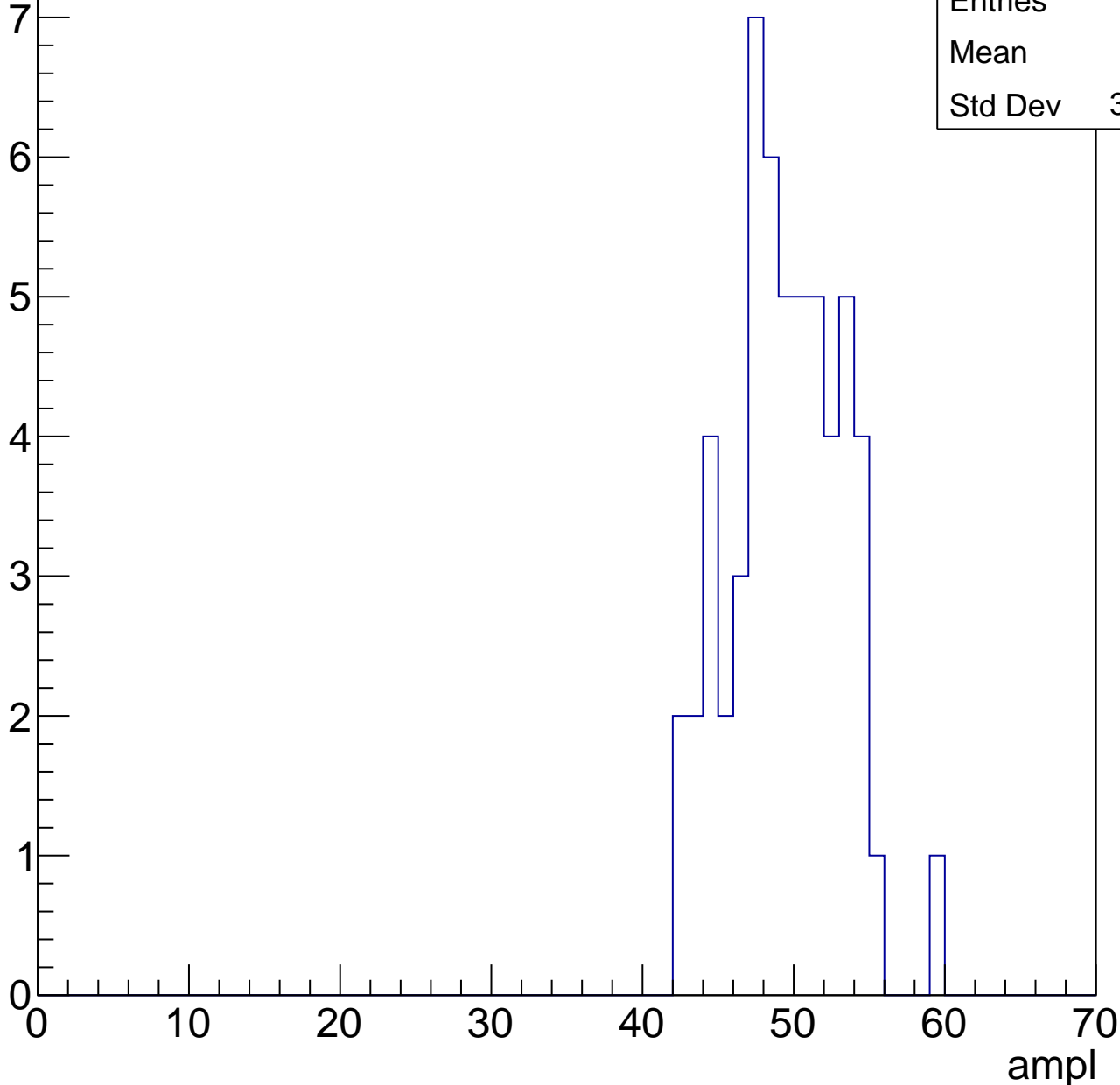


# B1L102S, U5-ch20, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	49
Std Dev	3.635



# B1L102S, U5-ch20, adc4

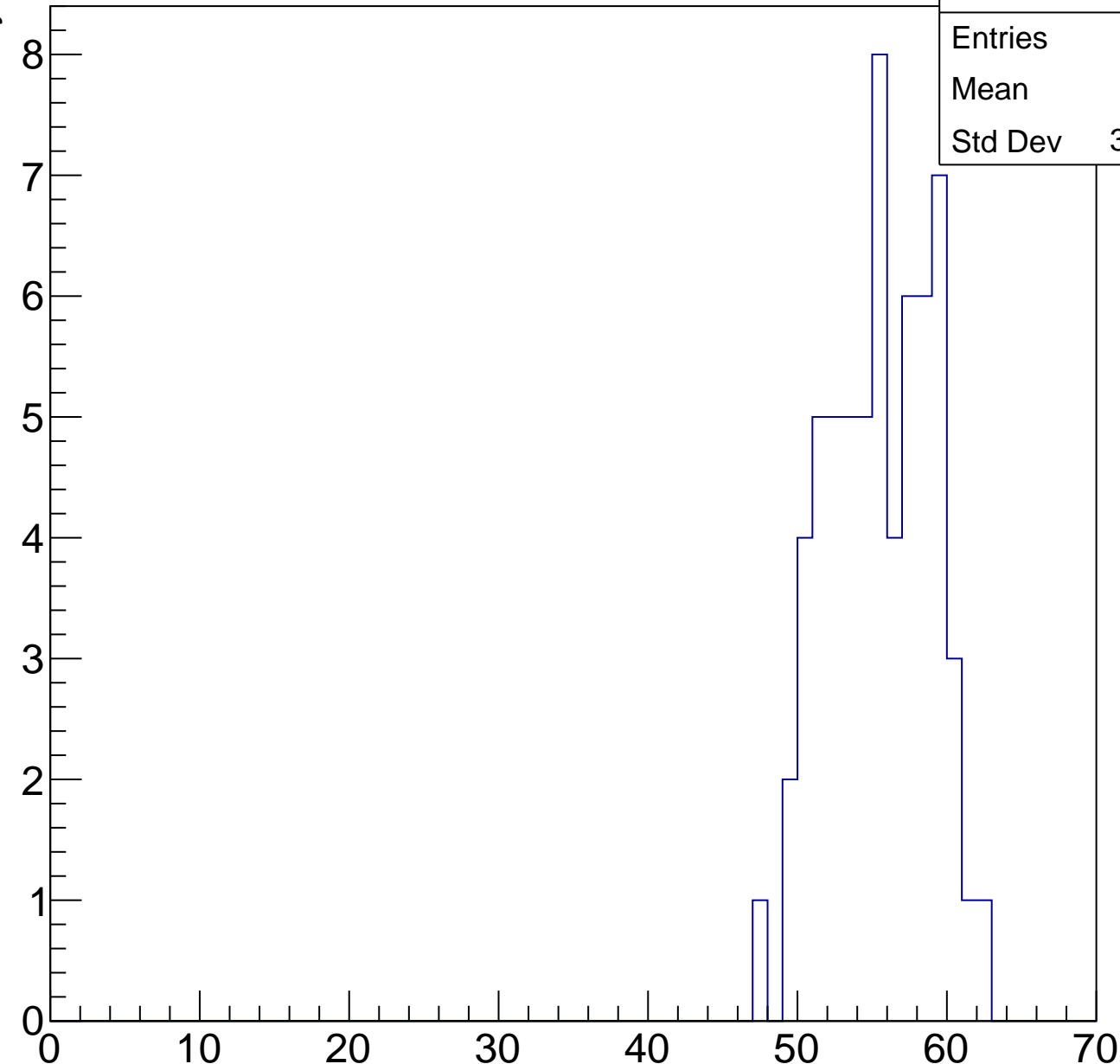
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	63
Mean	55
Std Dev	3.427

ampl

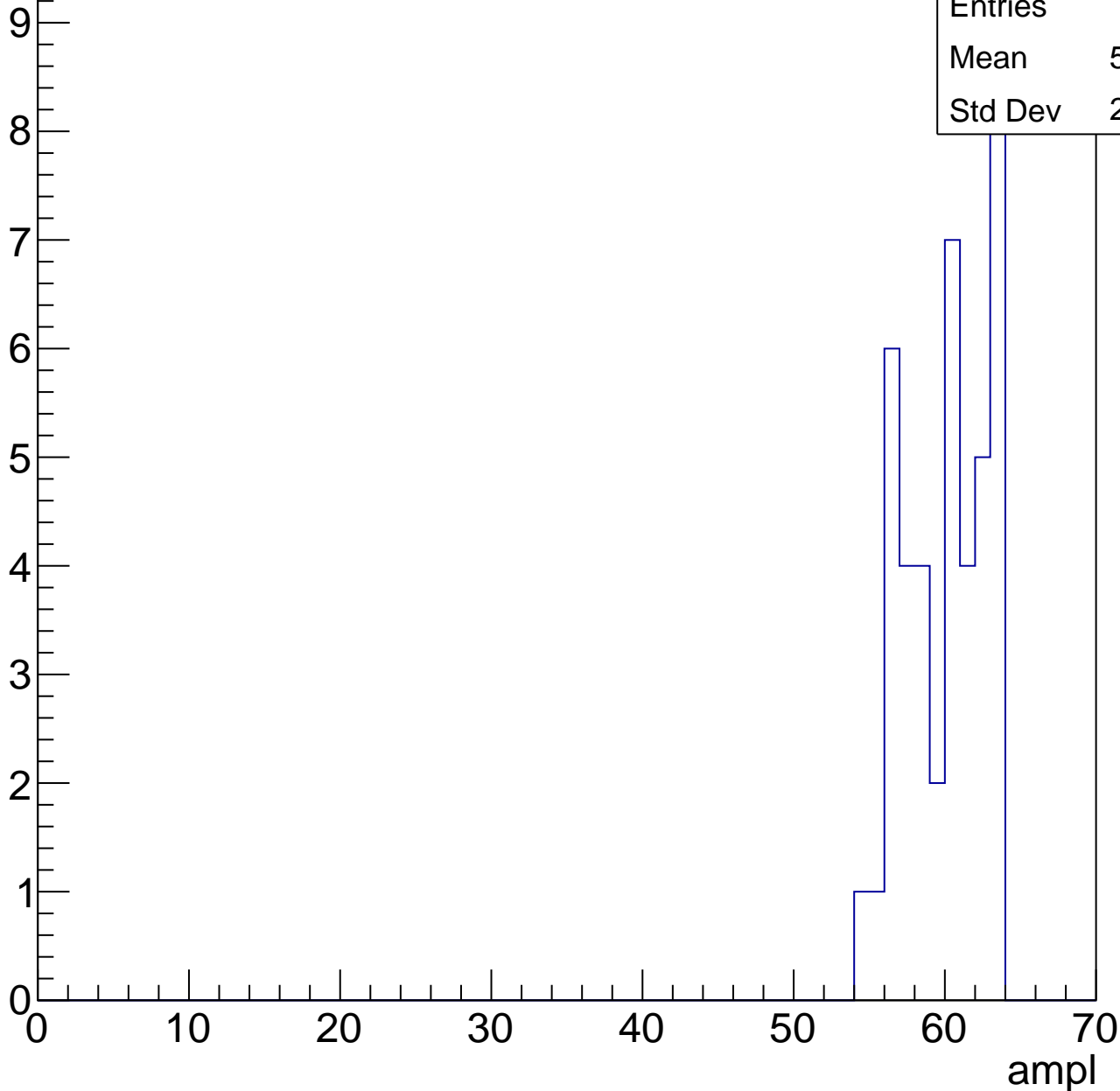


# B1L102S, U5-ch20, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	43
Mean	59.63
Std Dev	2.685

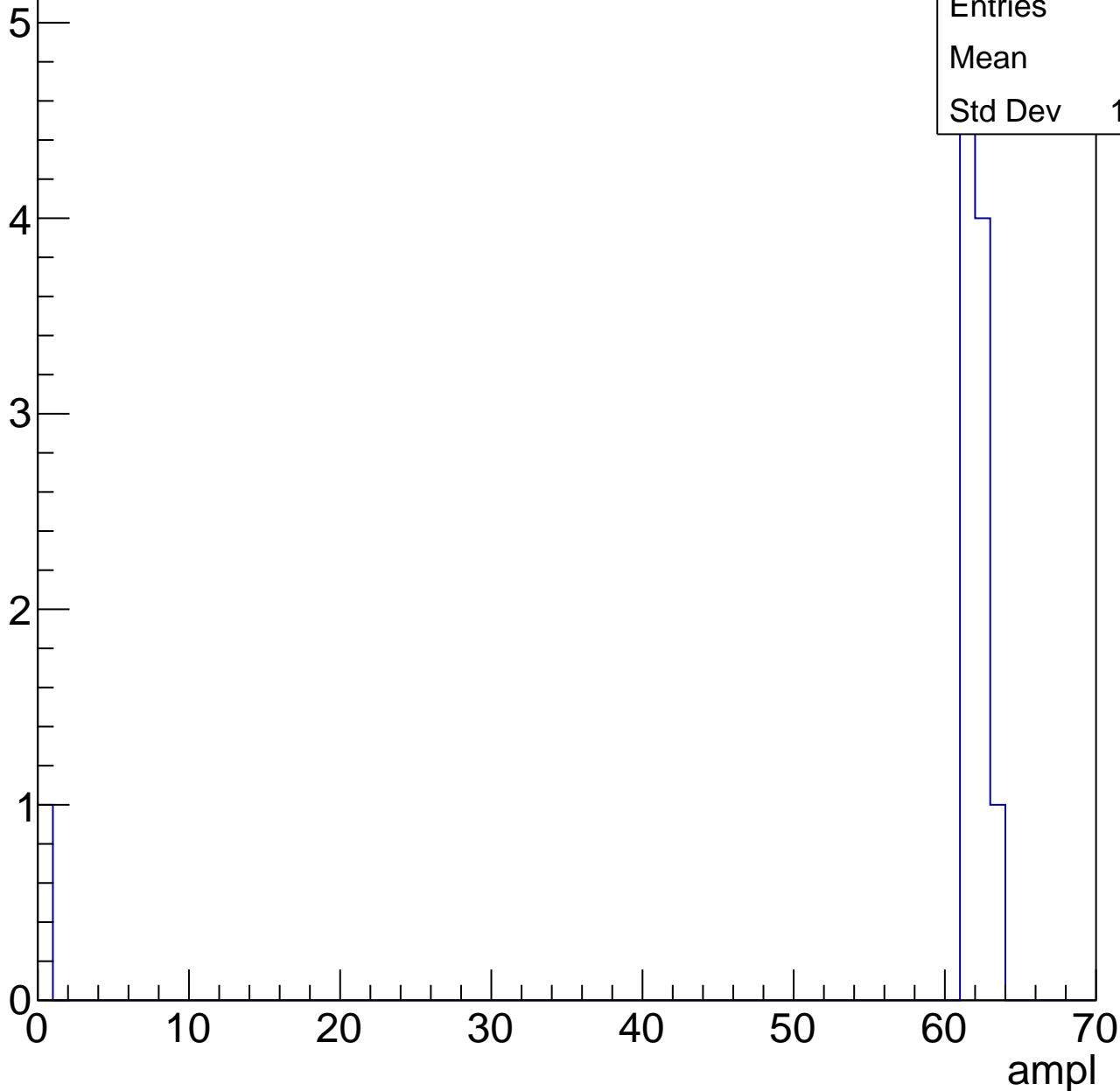


# B1L102S, U5-ch20, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	11
Mean	56
Std Dev	17.72





# B1L102S, U5-ch20, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U5-ch21, adc0

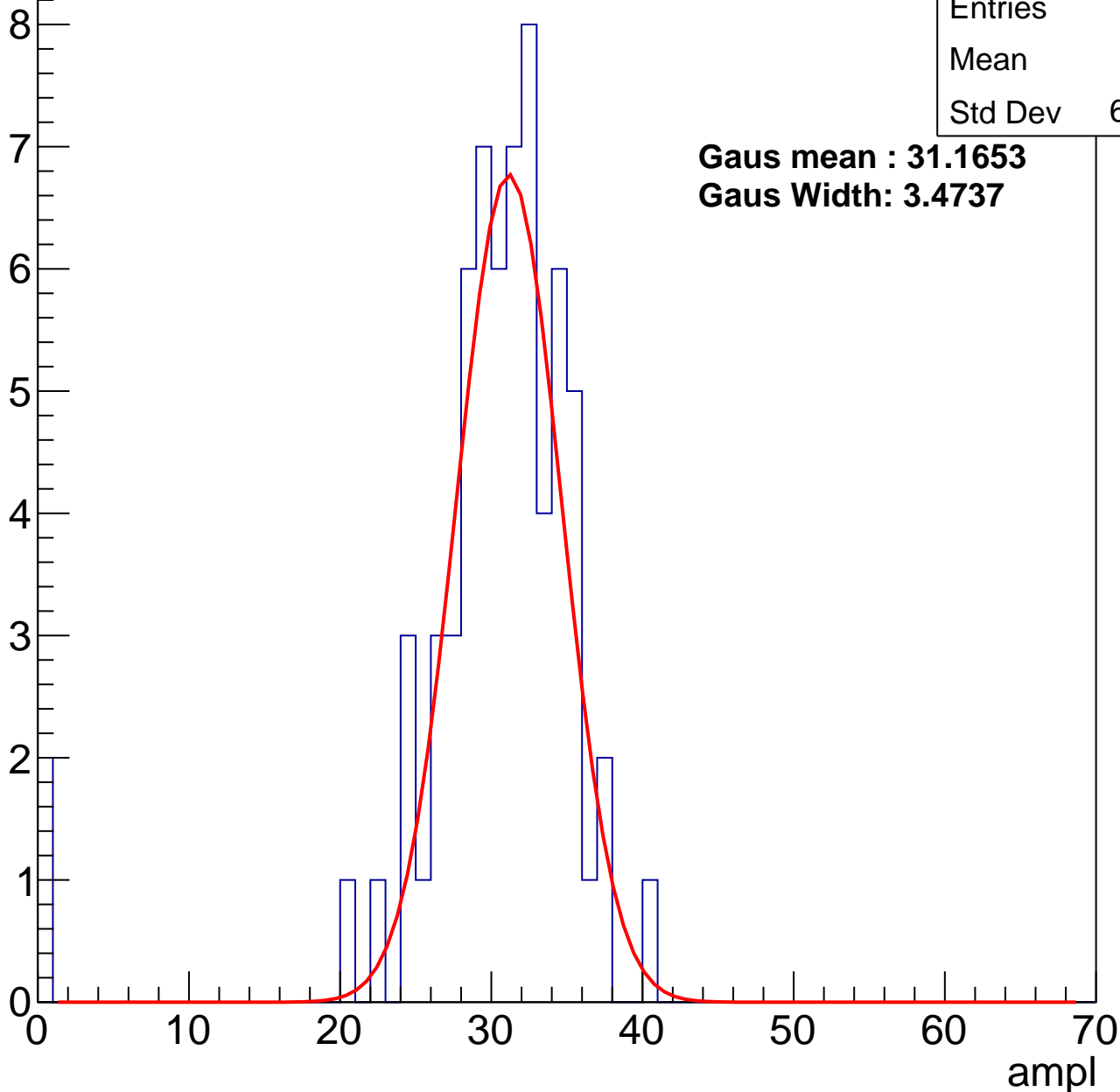
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	29.6
Std Dev	6.374

**Gaus mean : 31.1653**

**Gaus Width: 3.4737**



# B1L102S, U5-ch21, adc1

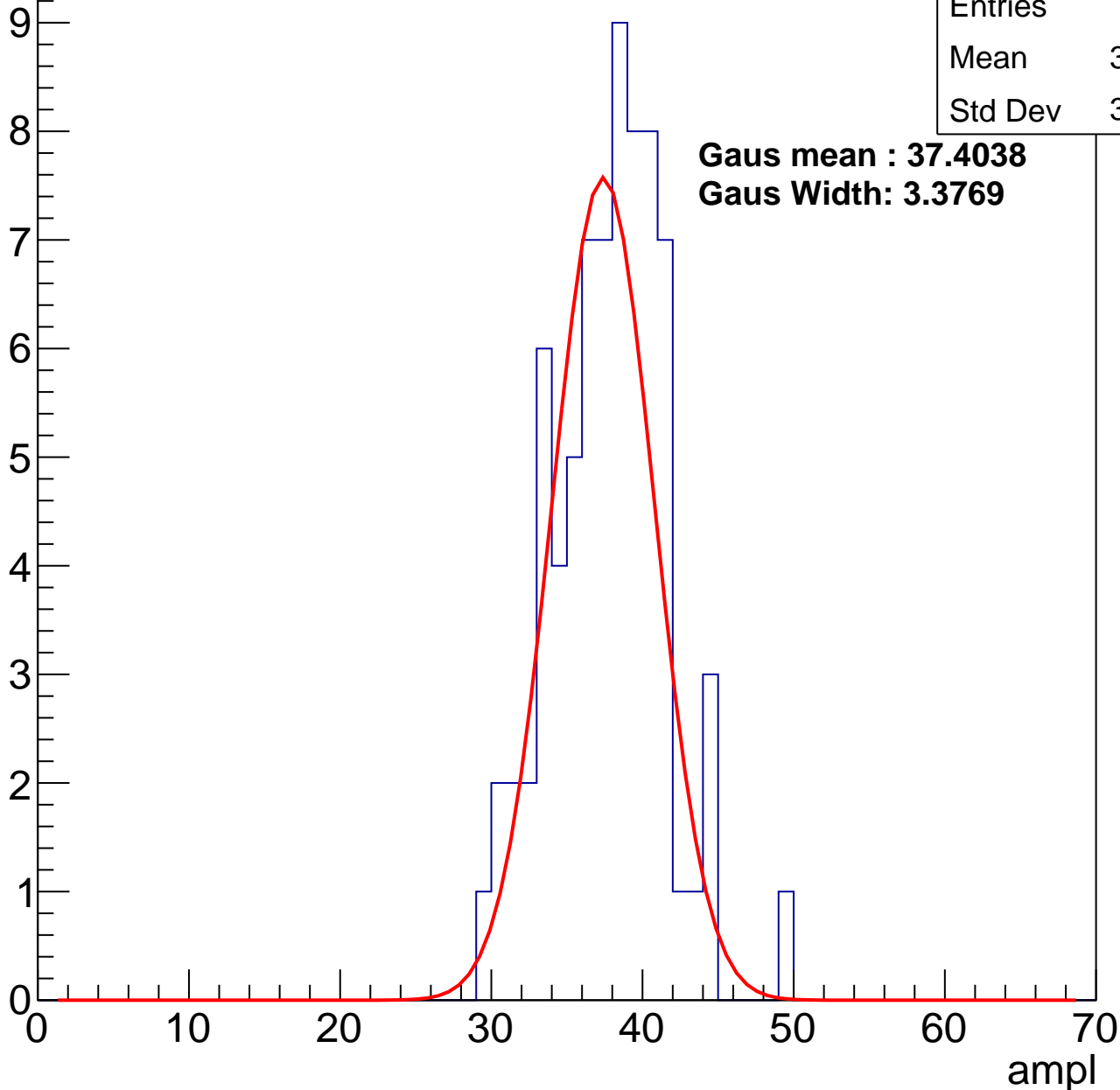
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	37.32
Std Dev	3.698

**Gaus mean : 37.4038**

**Gaus Width: 3.3769**



# B1L102S, U5-ch21, adc2

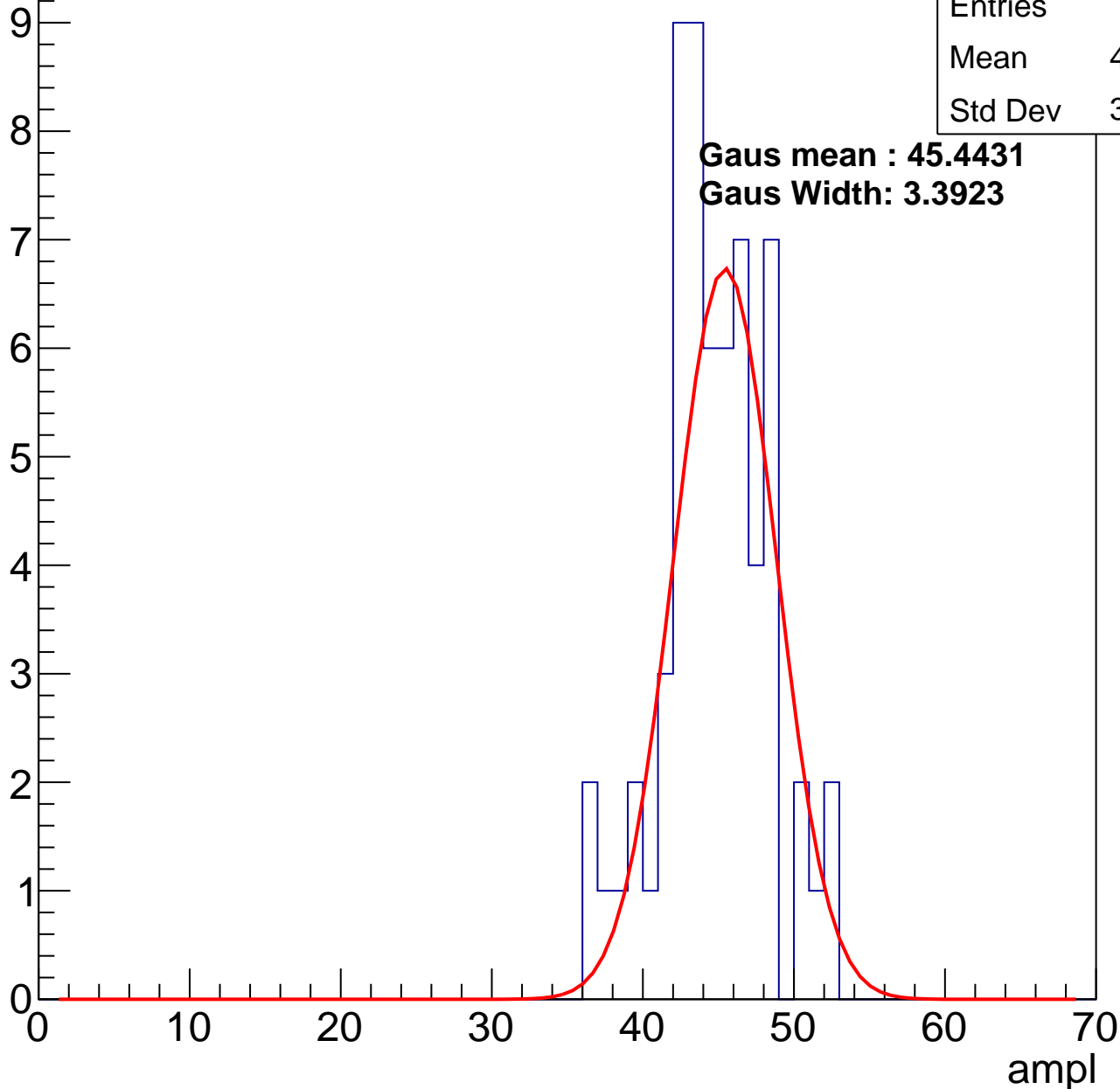
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	44.25
Std Dev	3.514

**Gaus mean : 45.4431**

**Gaus Width: 3.3923**

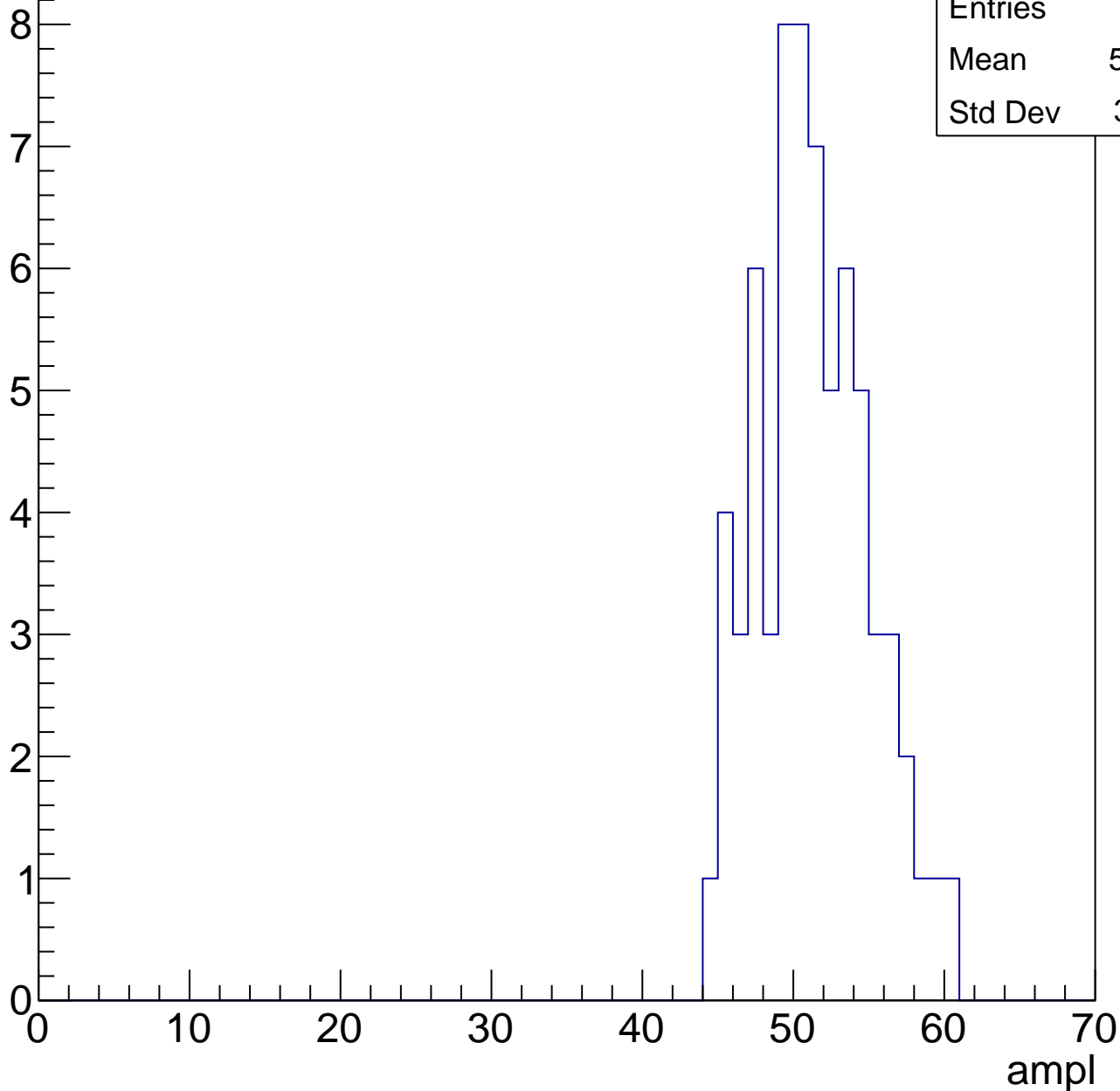


# B1L102S, U5-ch21, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	50.88
Std Dev	3.651

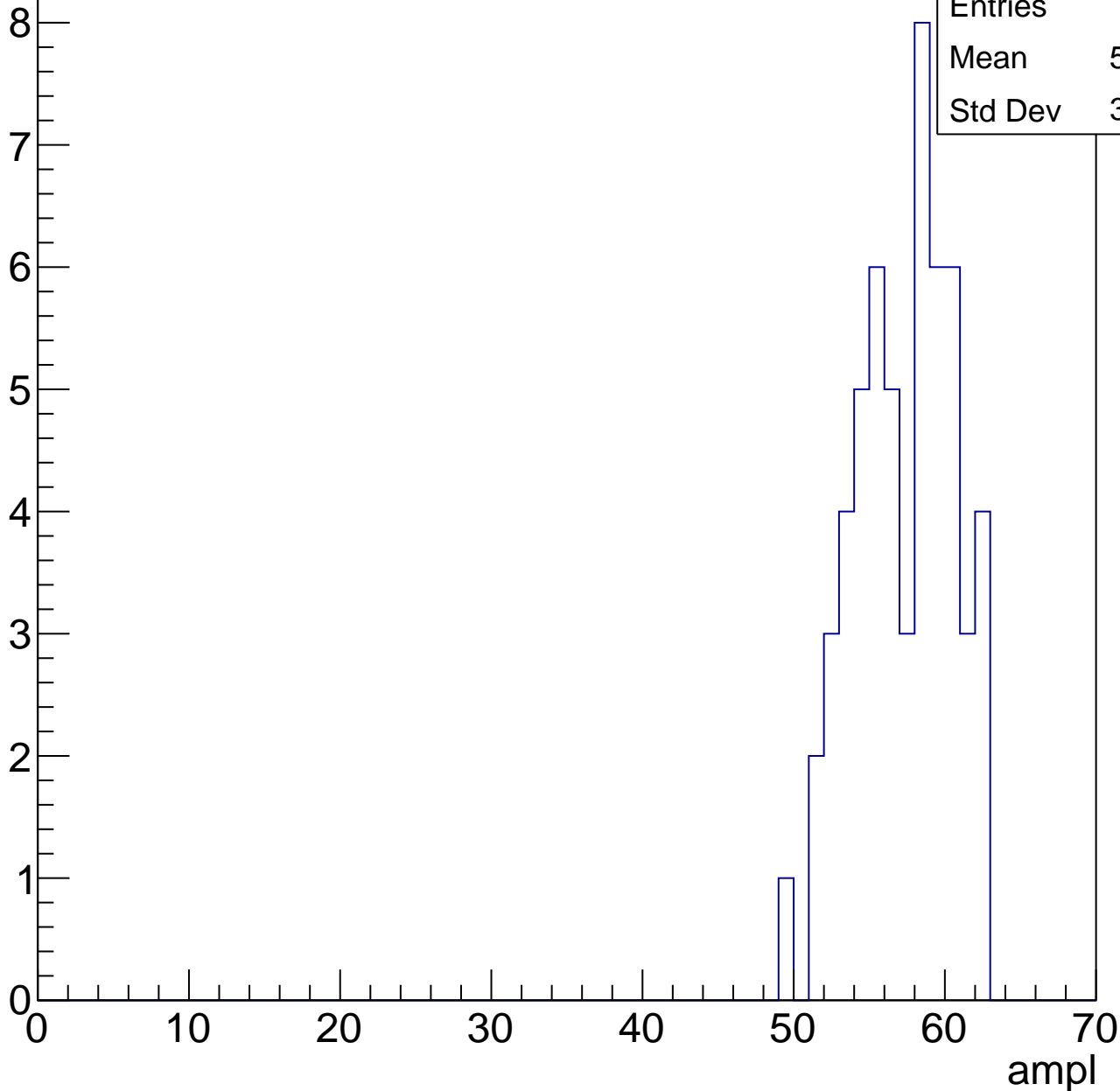


# B1L102S, U5-ch21, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	56.77
Std Dev	3.218

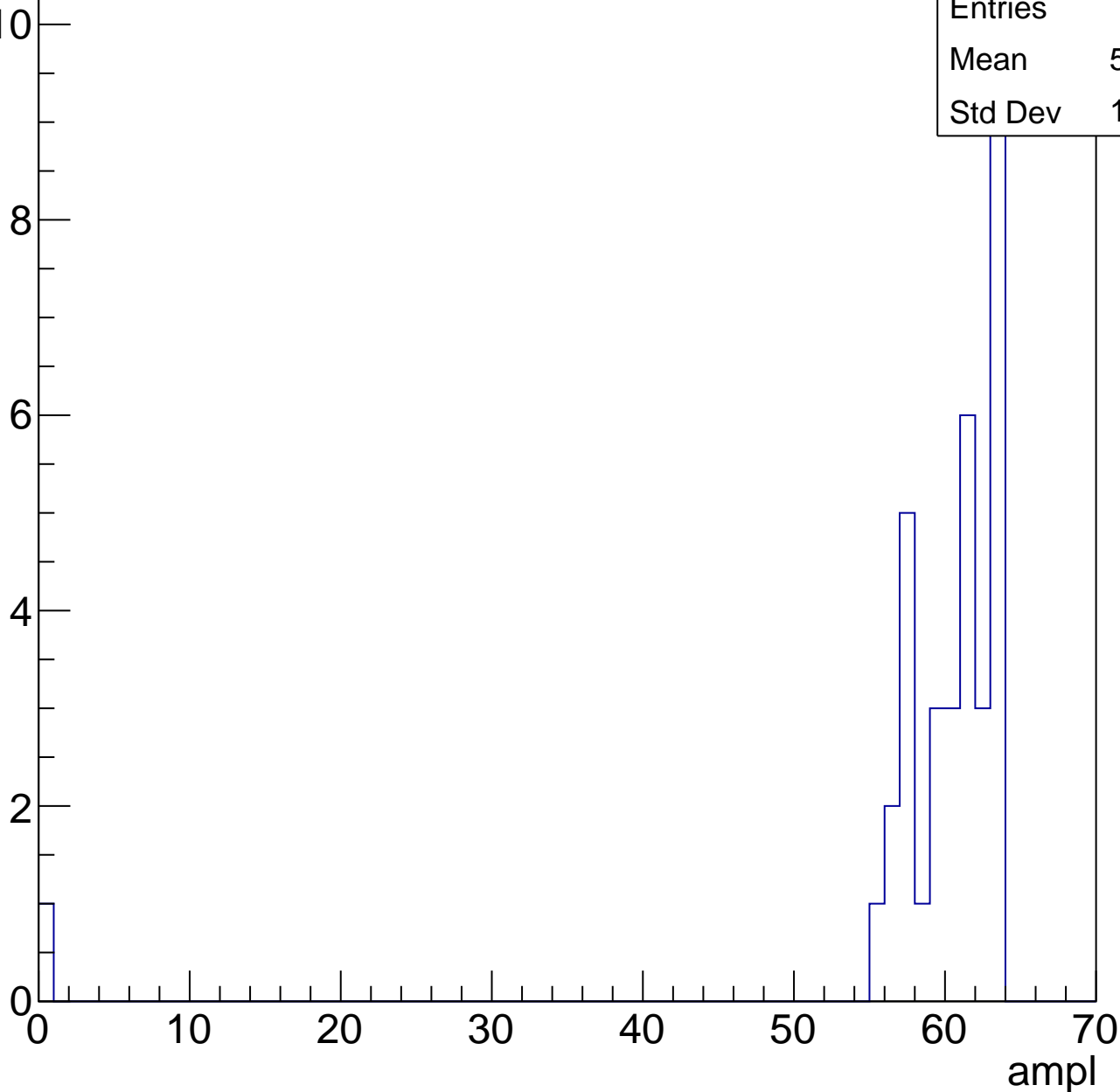


# B1L102S, U5-ch21, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	35
Mean	58.54
Std Dev	10.34



# B1L102S, U5-ch21, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U5-ch21, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U5-ch22, adc0

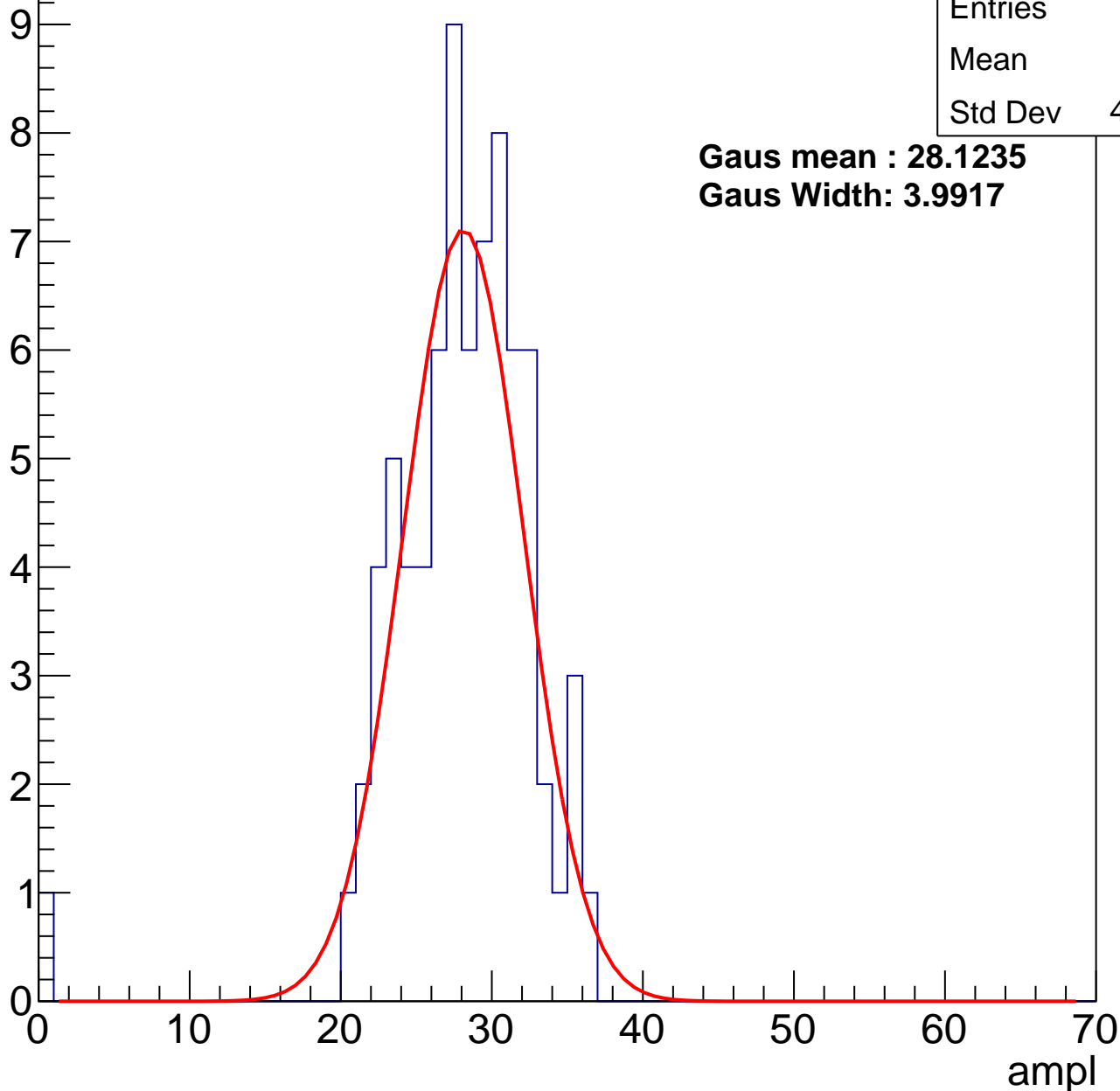
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	27.5
Std Dev	4.887

**Gaus mean : 28.1235**

**Gaus Width: 3.9917**



# B1L102S, U5-ch22, adc1

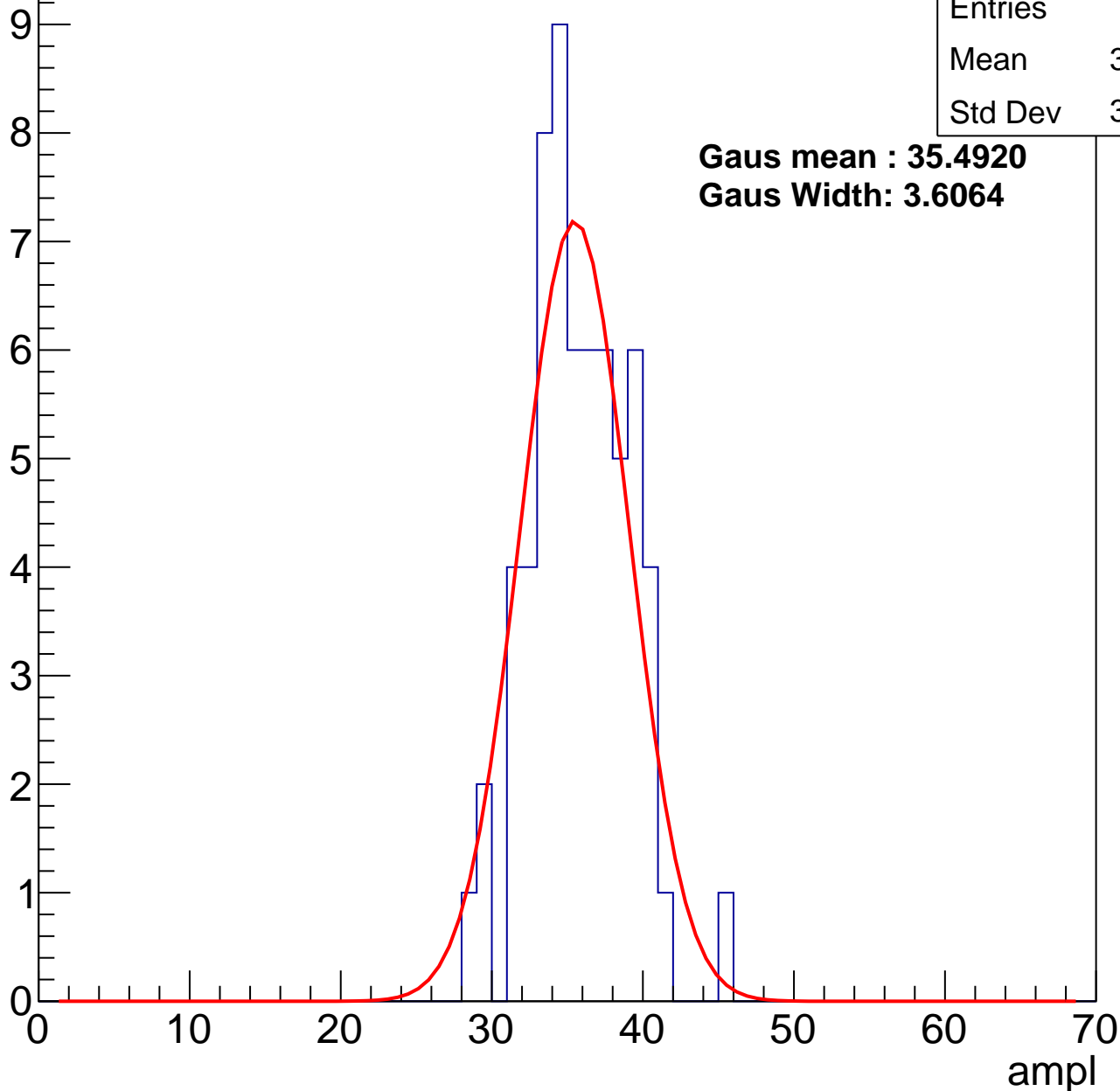
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	35.33
Std Dev	3.242

**Gaus mean : 35.4920**

**Gaus Width: 3.6064**



# B1L102S, U5-ch22, adc2

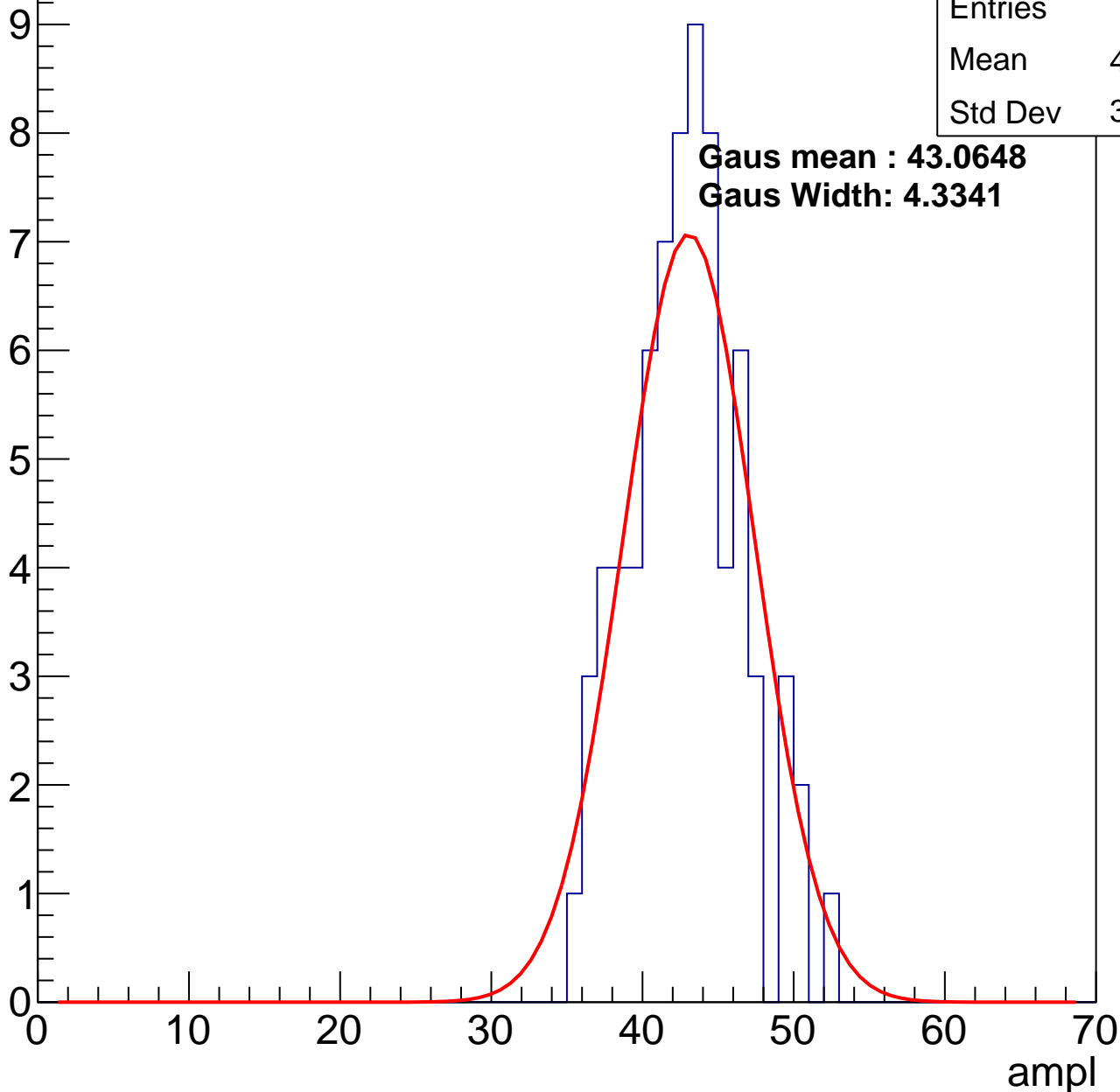
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	42.42
Std Dev	3.697

**Gaus mean : 43.0648**

**Gaus Width: 4.3341**



# B1L102S, U5-ch22, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

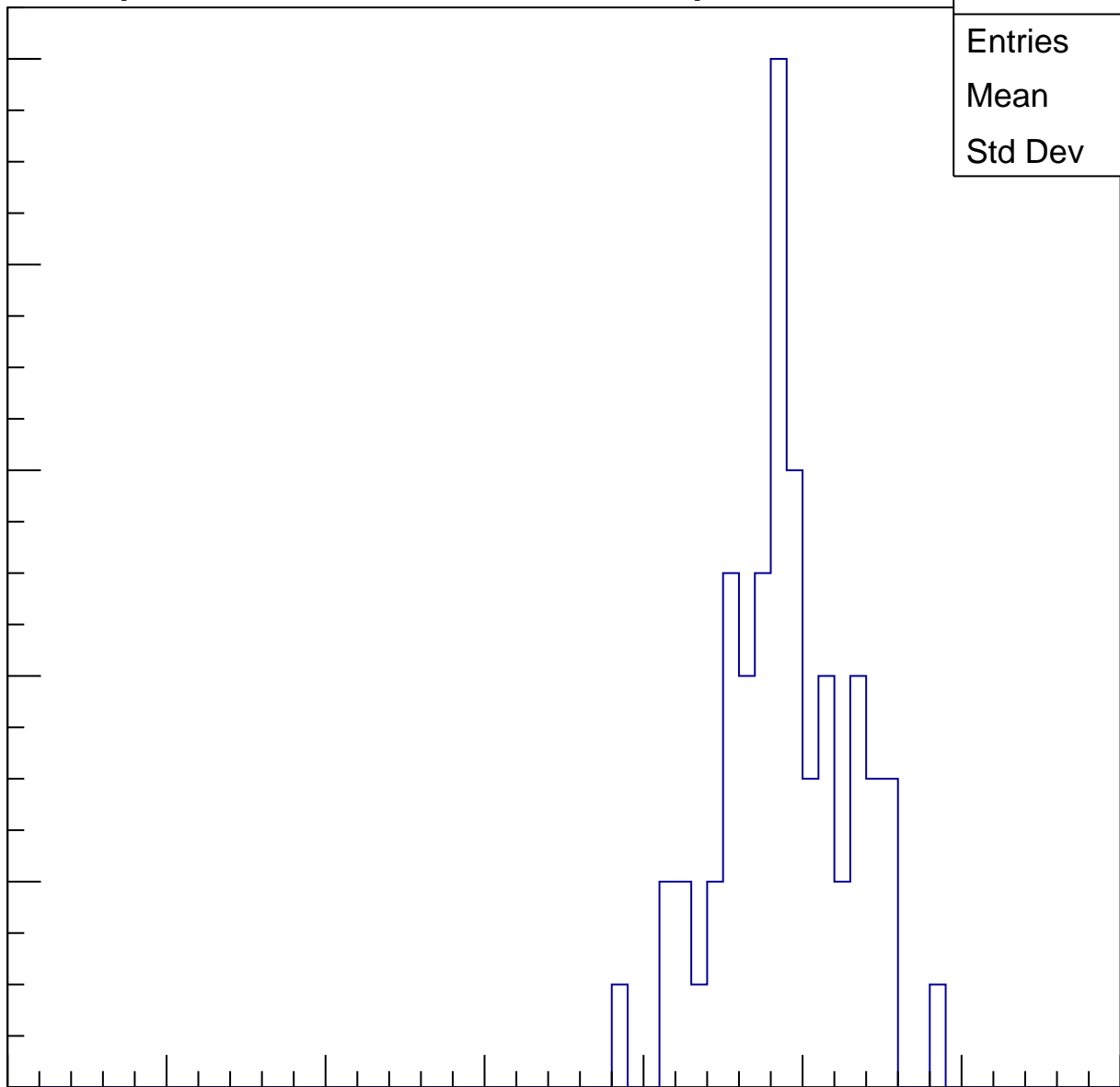
Entries	58
Mean	48.41
Std Dev	3.992

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

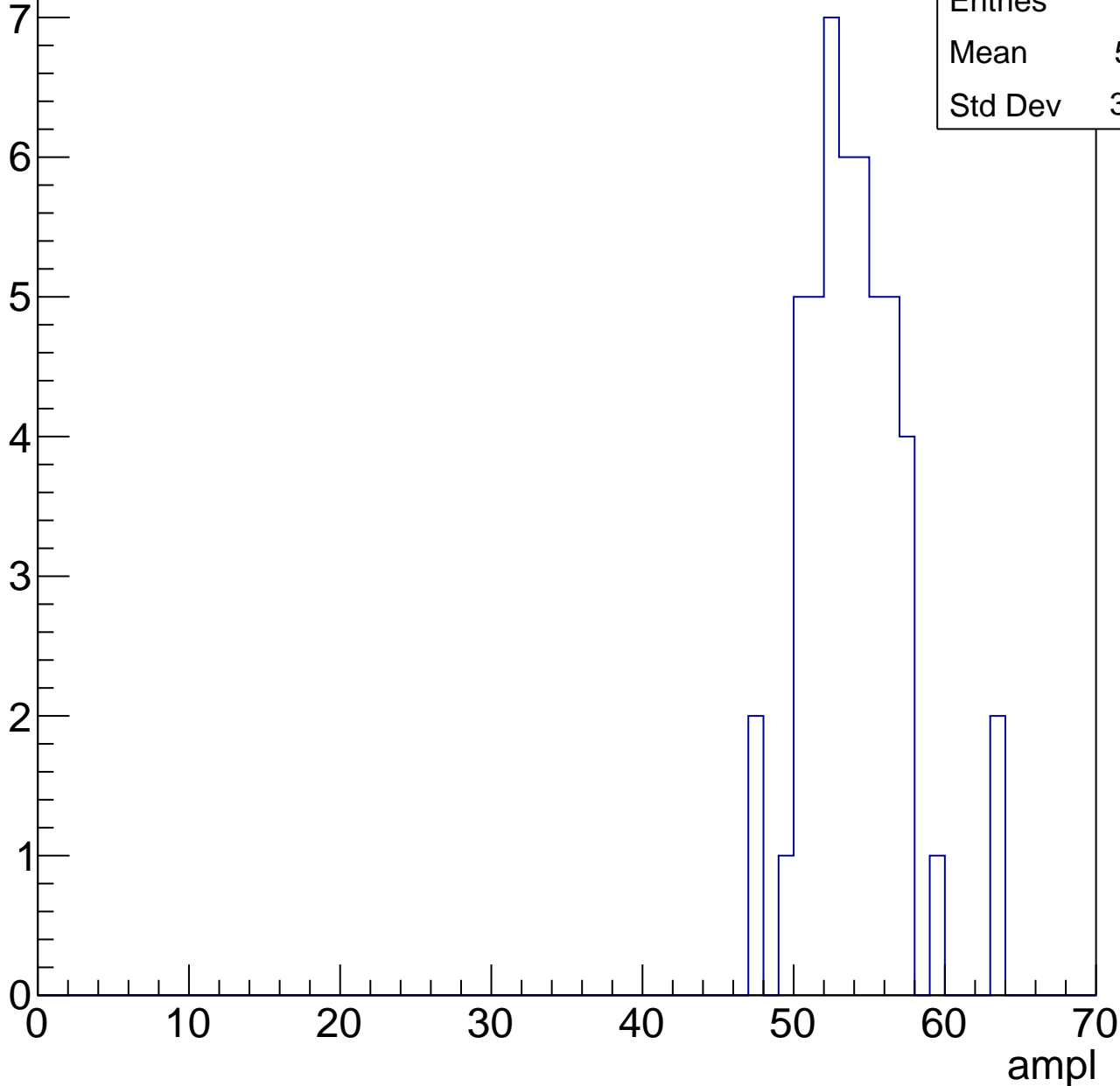


# B1L102S, U5-ch22, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	53.51
Std Dev	3.252



# B1L102S, U5-ch22, adc5

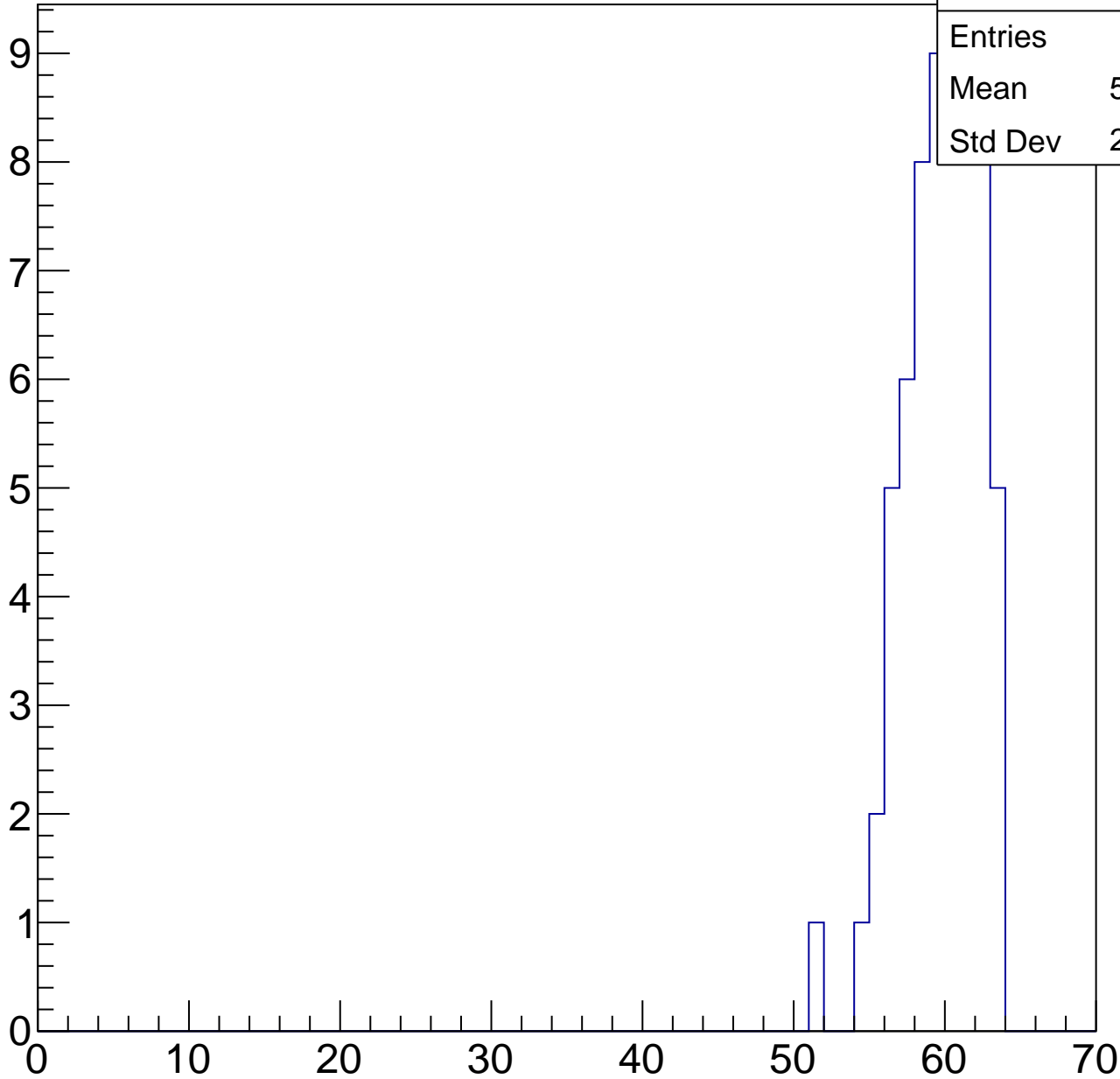
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	62
Mean	59.24
Std Dev	2.525

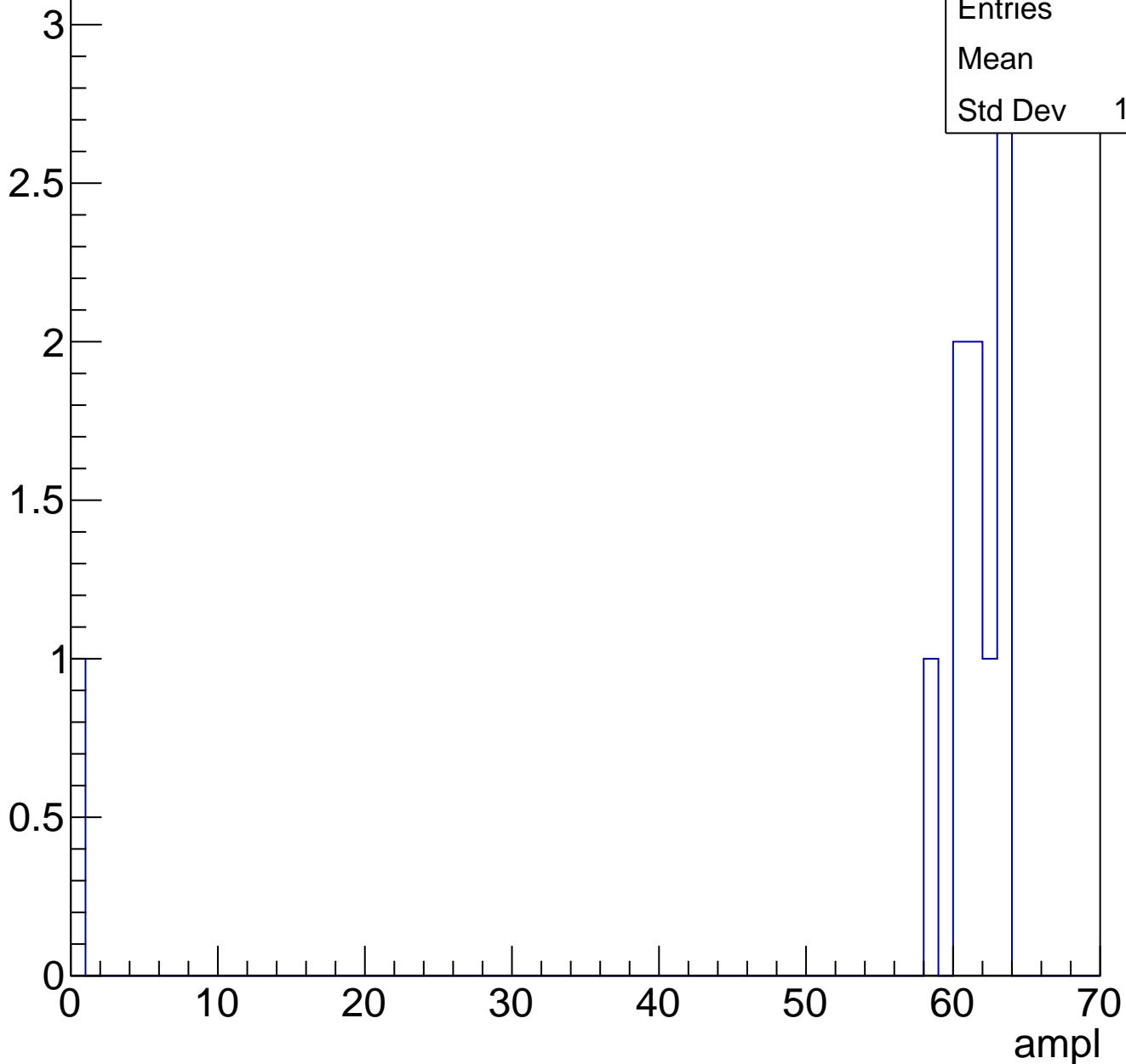
ampl



# B1L102S, U5-ch22, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U5-ch22, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U5-ch23, adc0

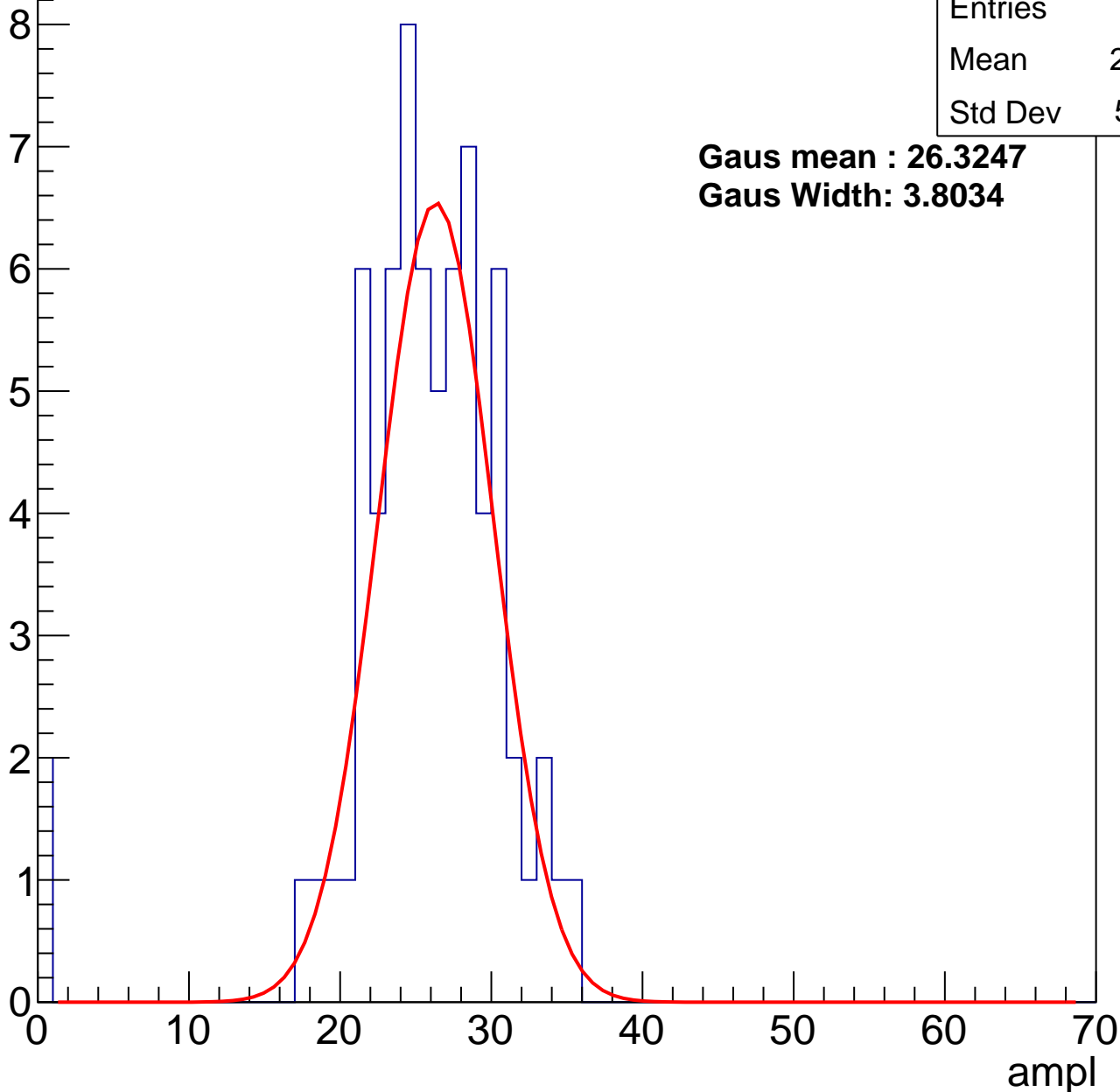
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	25.08
Std Dev	5.721

**Gaus mean : 26.3247**

**Gaus Width: 3.8034**



# B1L102S, U5-ch23, adc1

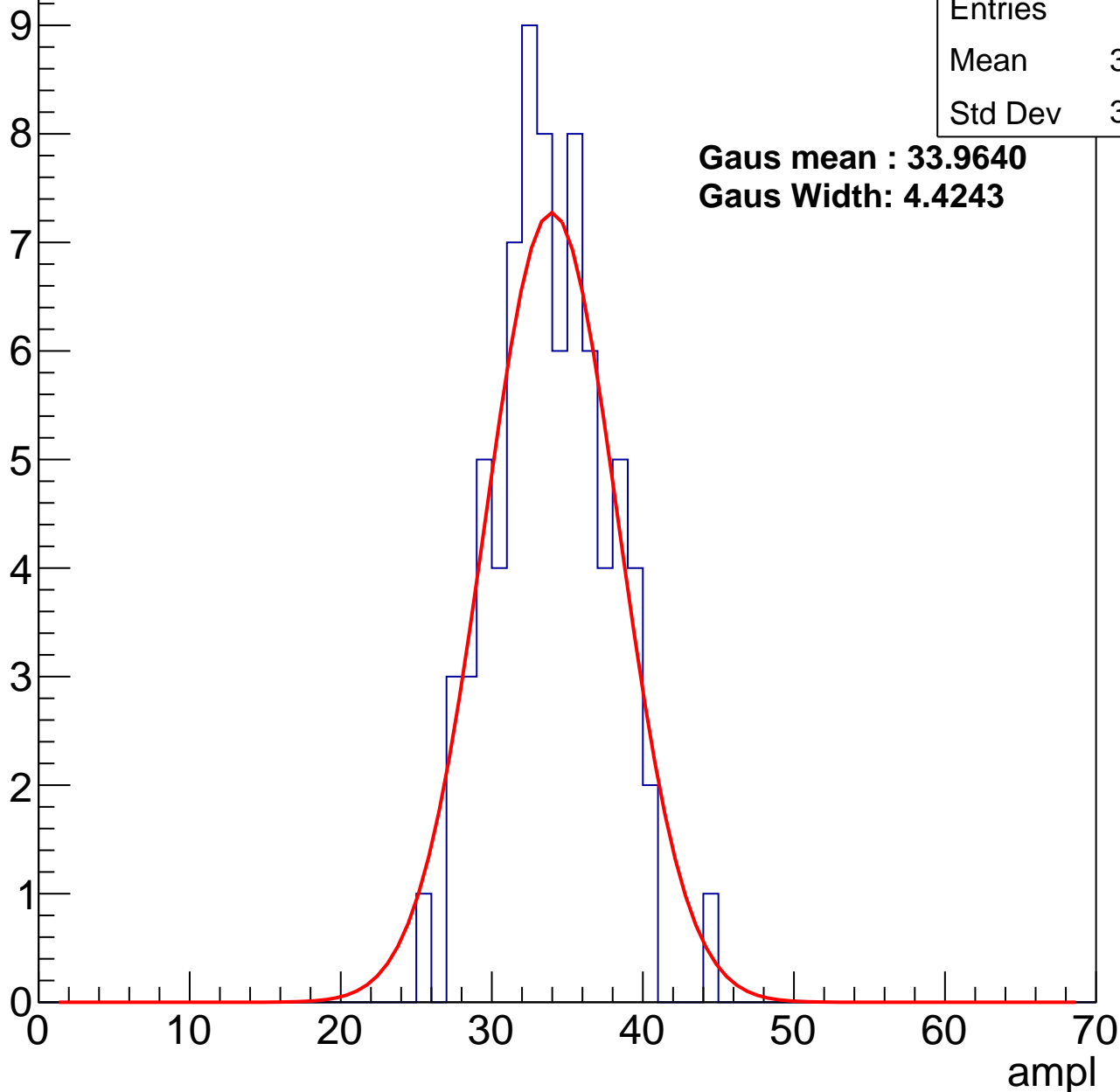
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	33.45
Std Dev	3.679

**Gaus mean : 33.9640**

**Gaus Width: 4.4243**



# B1L102S, U5-ch23, adc2

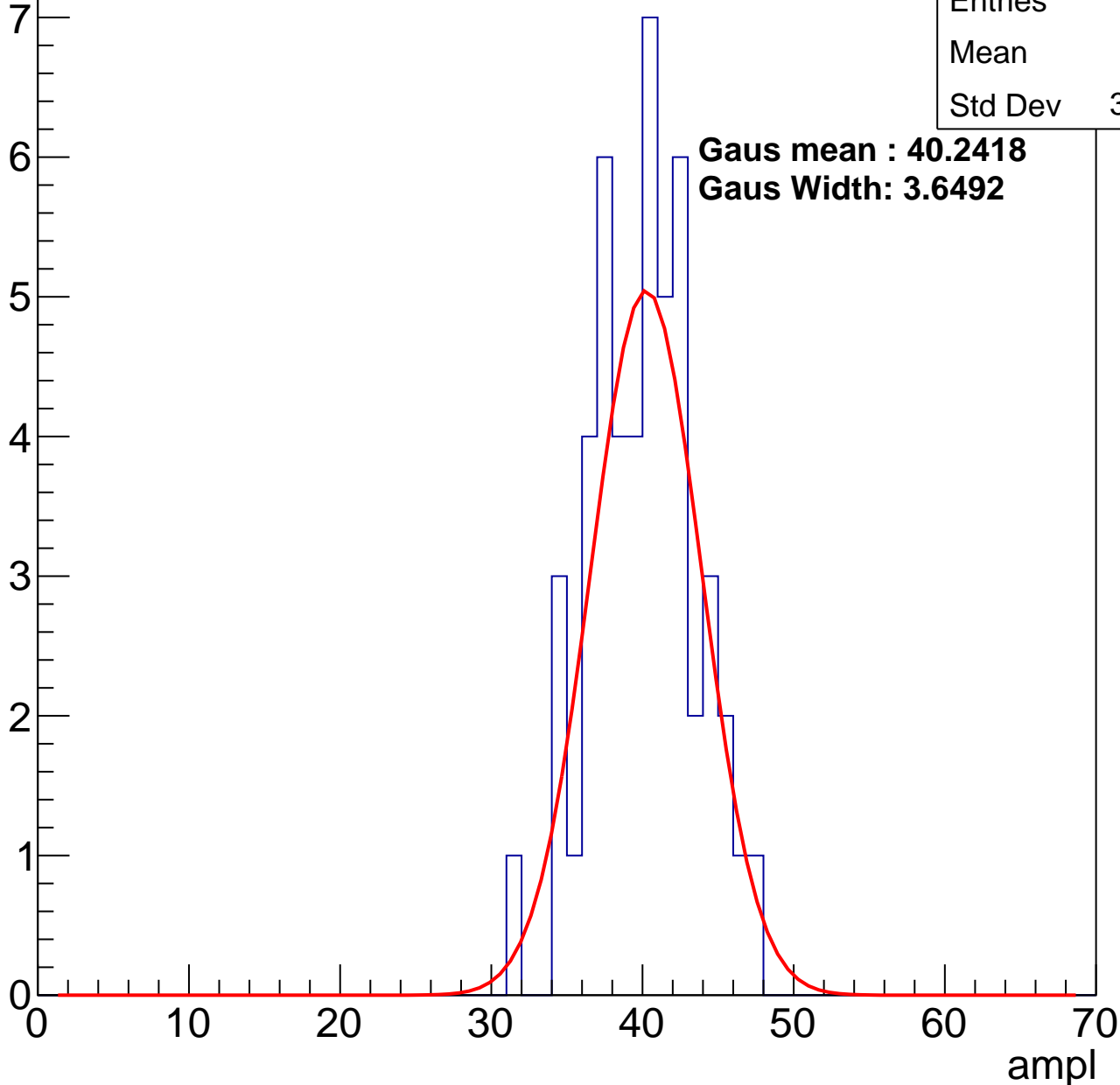
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	39.6
Std Dev	3.388

**Gaus mean : 40.2418**

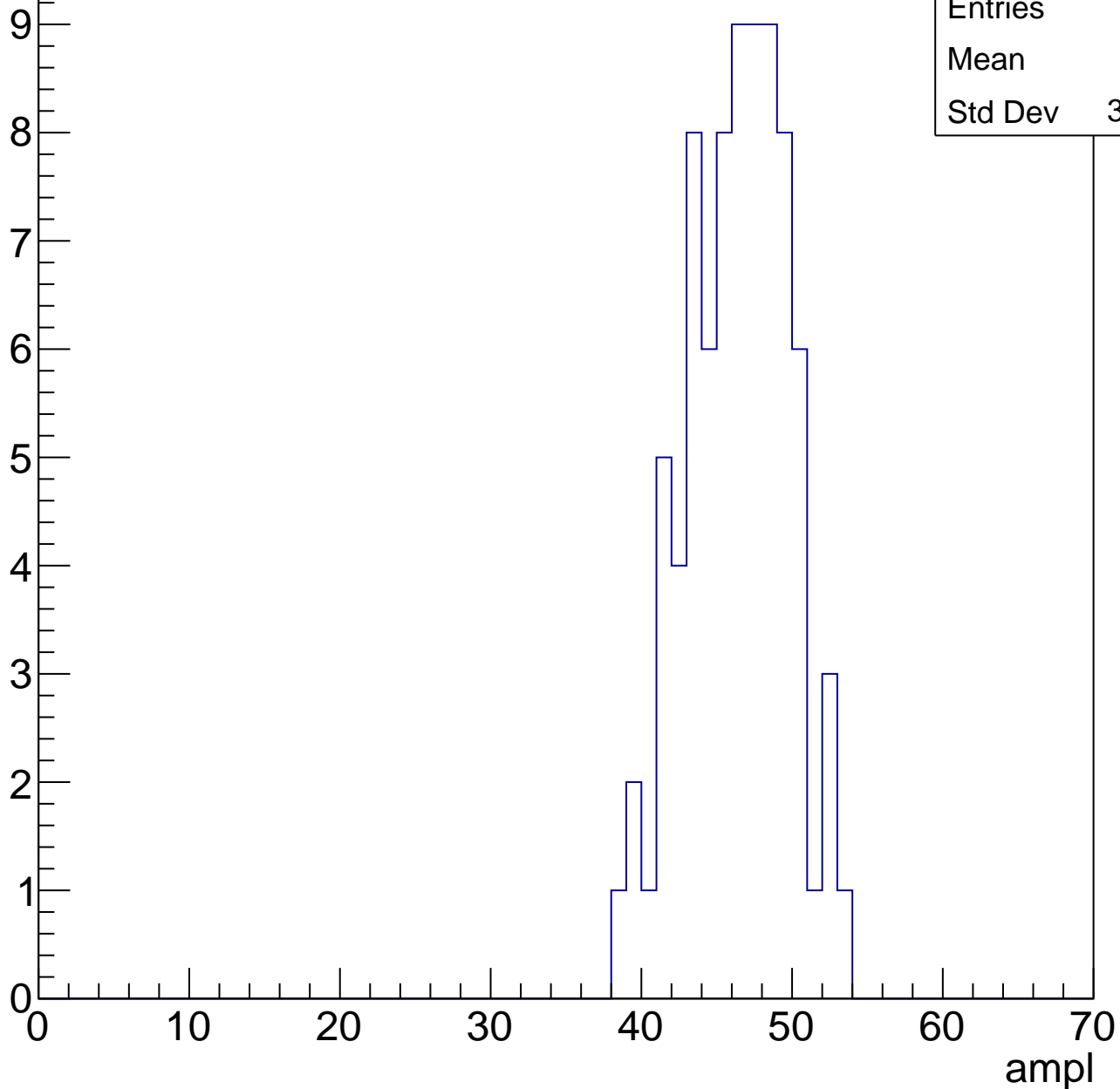
**Gaus Width: 3.6492**



# B1L102S, U5-ch23, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



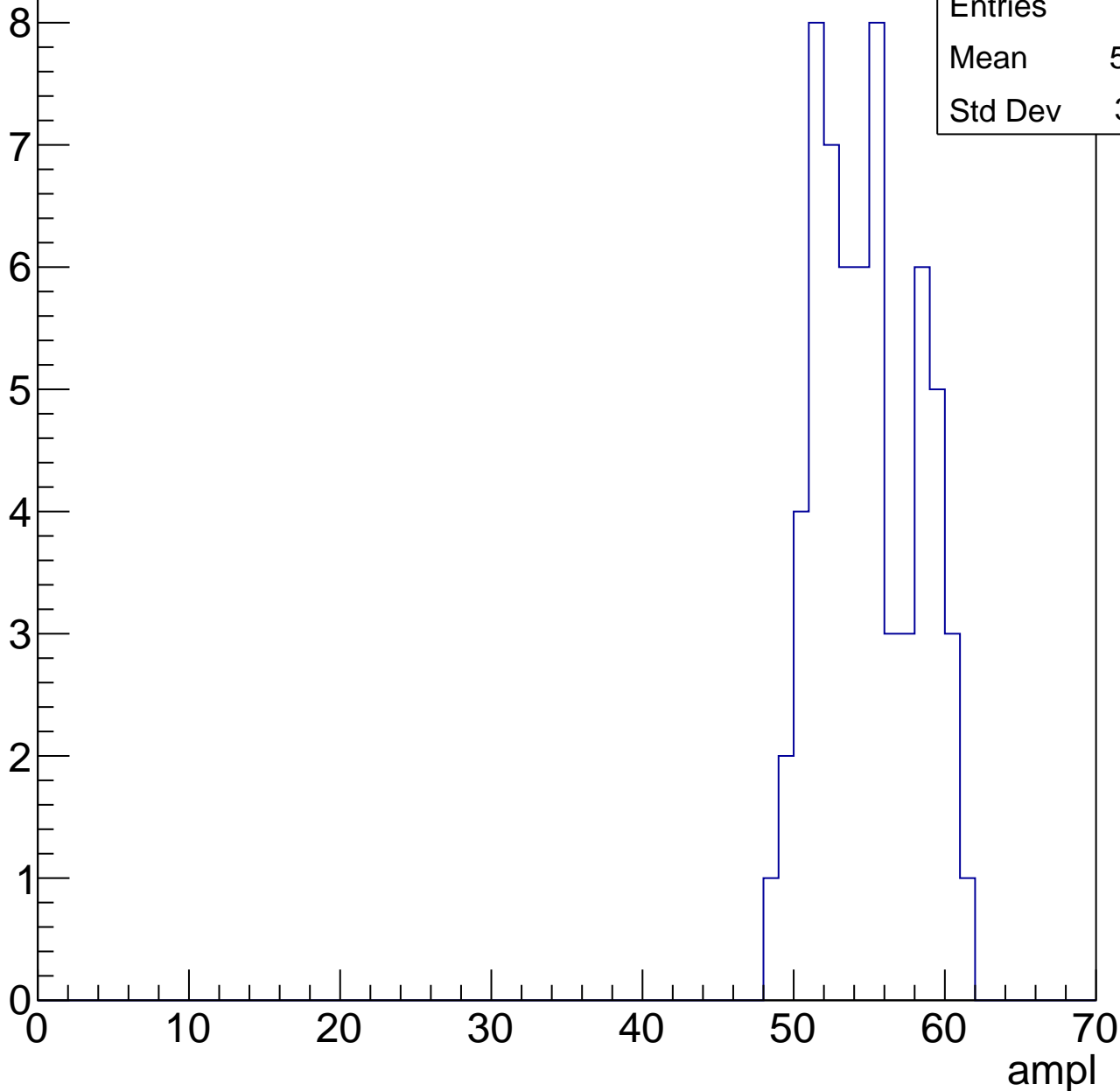
Entries	81
Mean	45.9
Std Dev	3.306

# B1L102S, U5-ch23, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	54.33
Std Dev	3.271

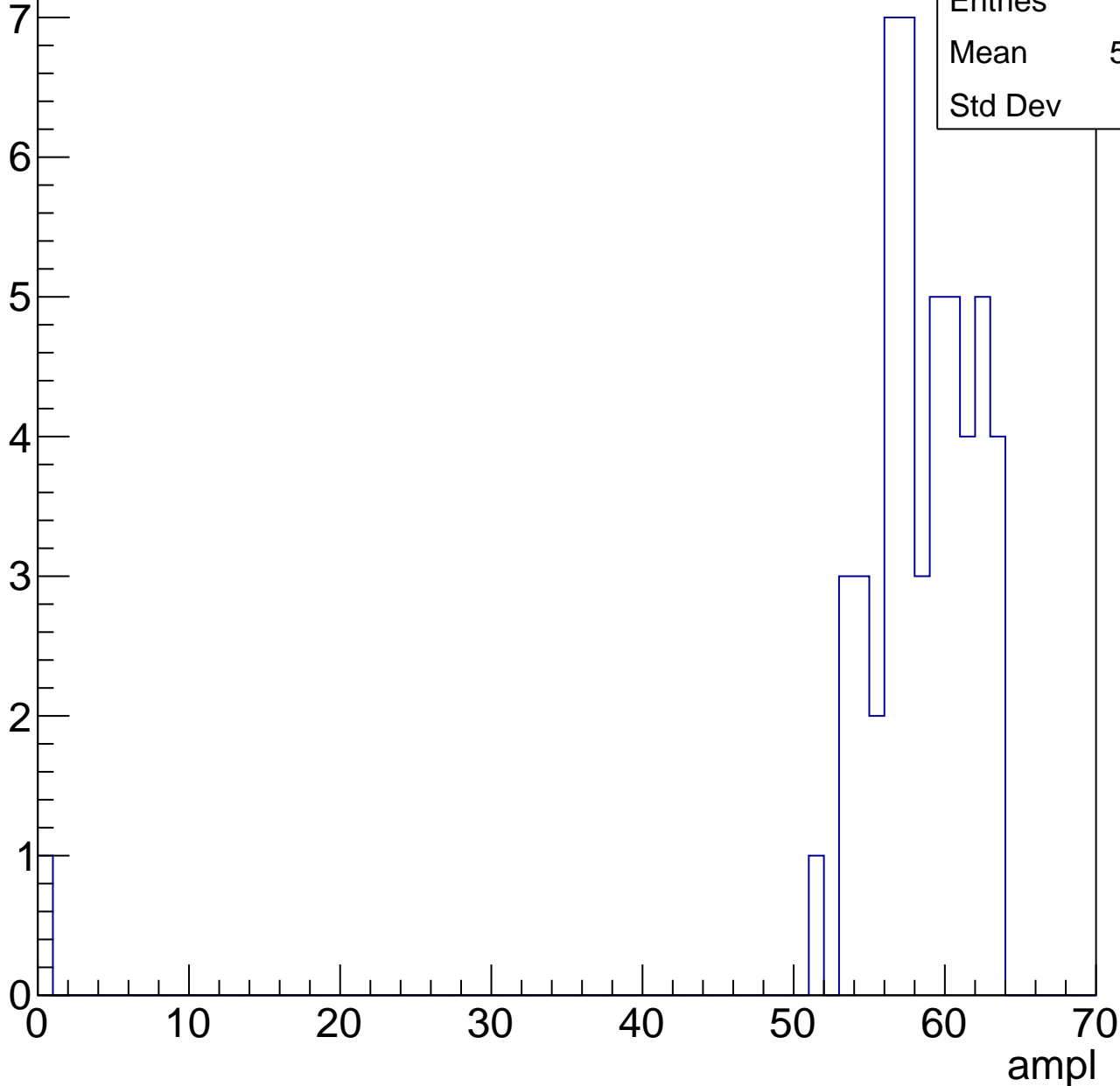


# B1L102S, U5-ch23, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	56.96
Std Dev	8.69

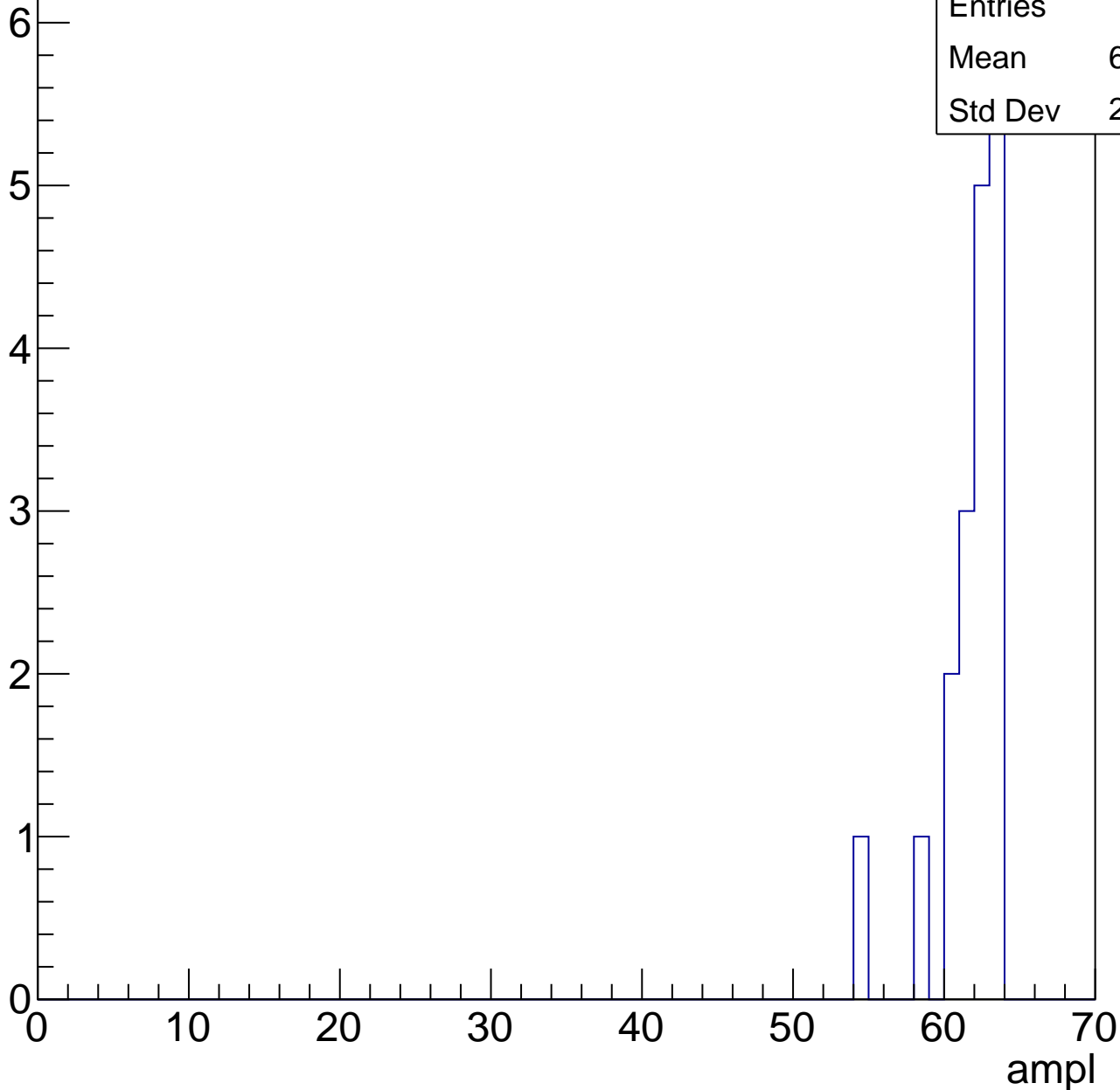


# B1L102S, U5-ch23, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	18
Mean	61.28
Std Dev	2.206

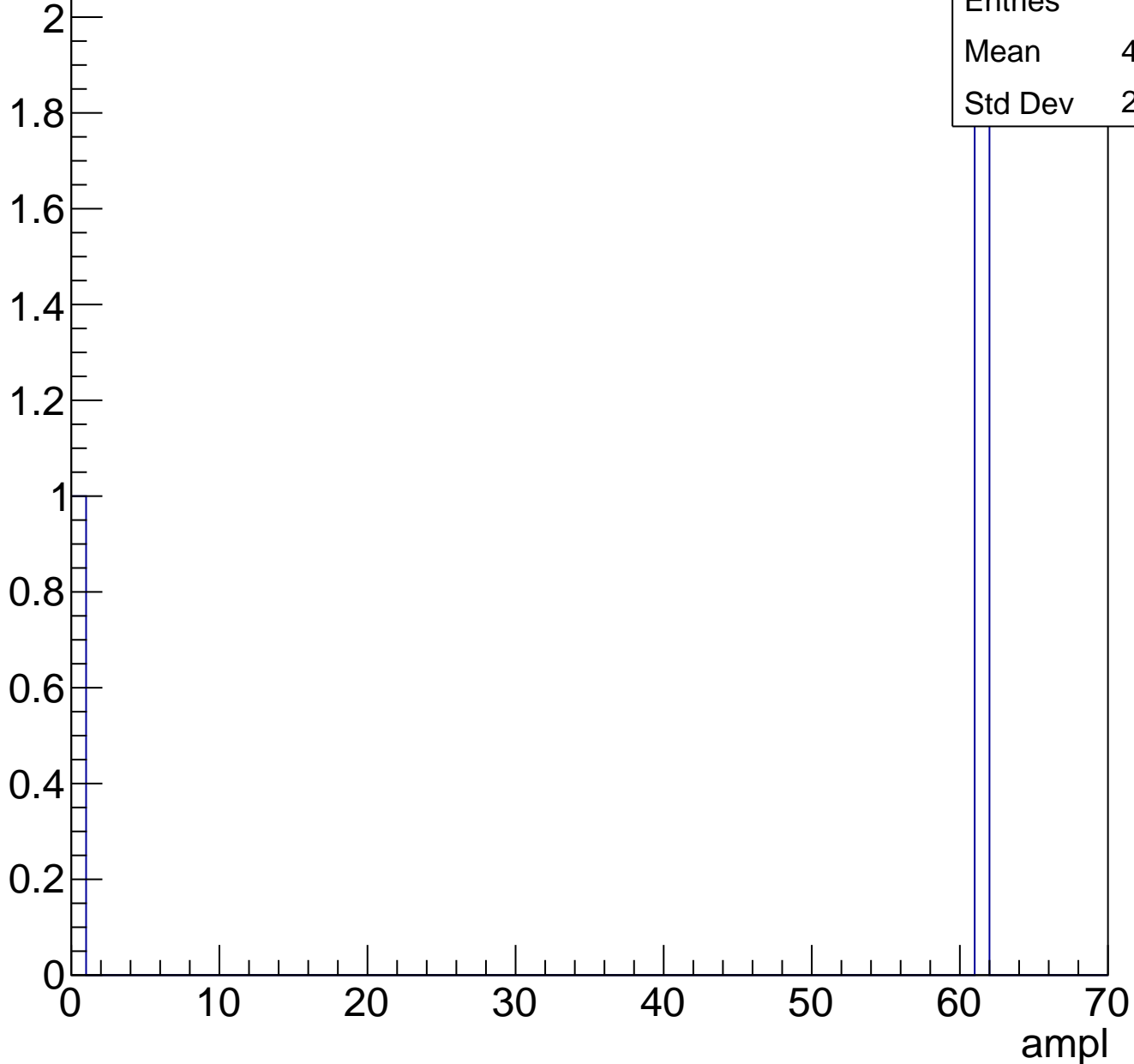




# B1L102S, U5-ch23, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U5-ch24, adc0

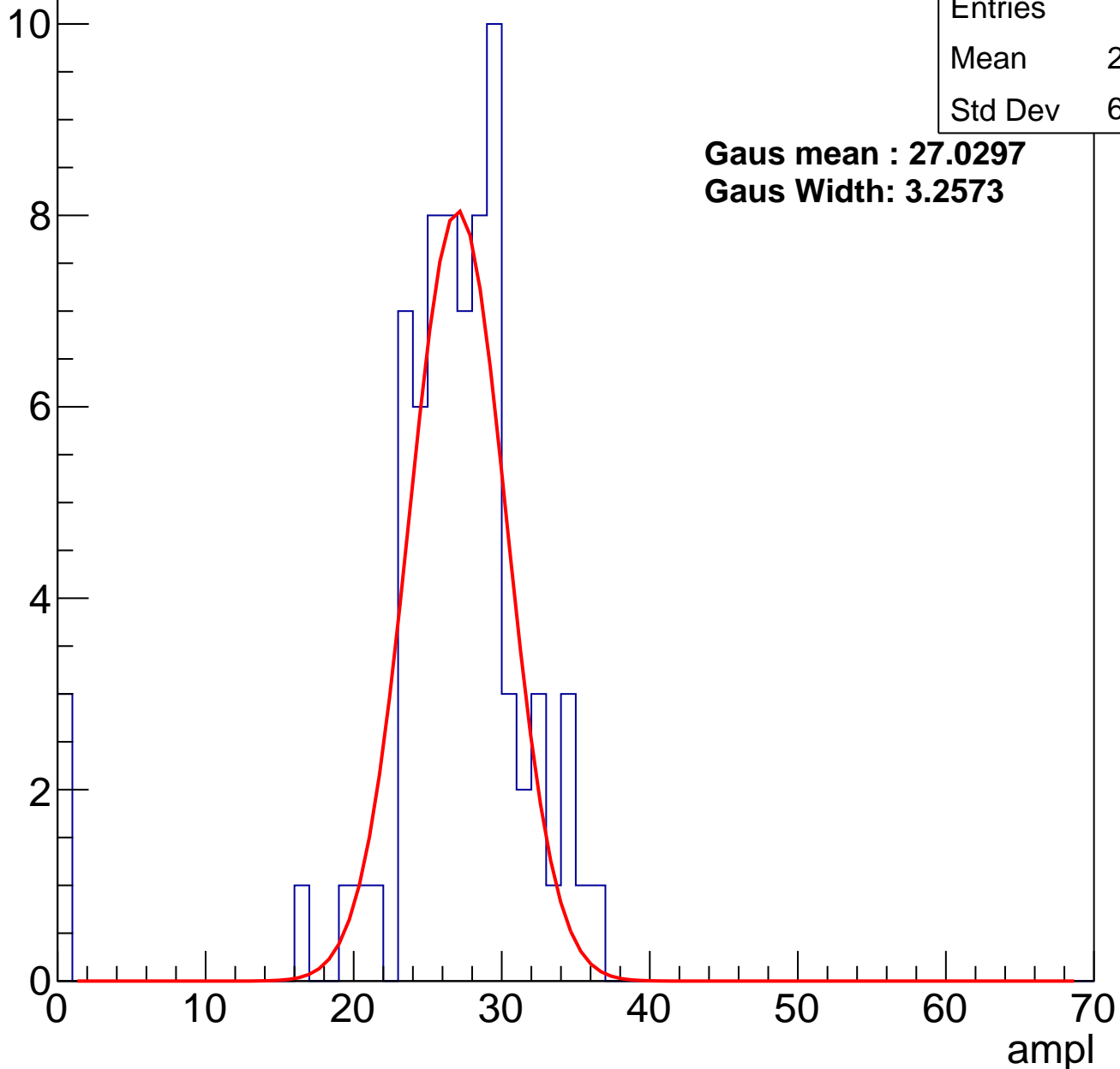
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	75
Mean	25.95
Std Dev	6.419

**Gaus mean : 27.0297**

**Gaus Width: 3.2573**

Entry



# B1L102S, U5-ch24, adc1

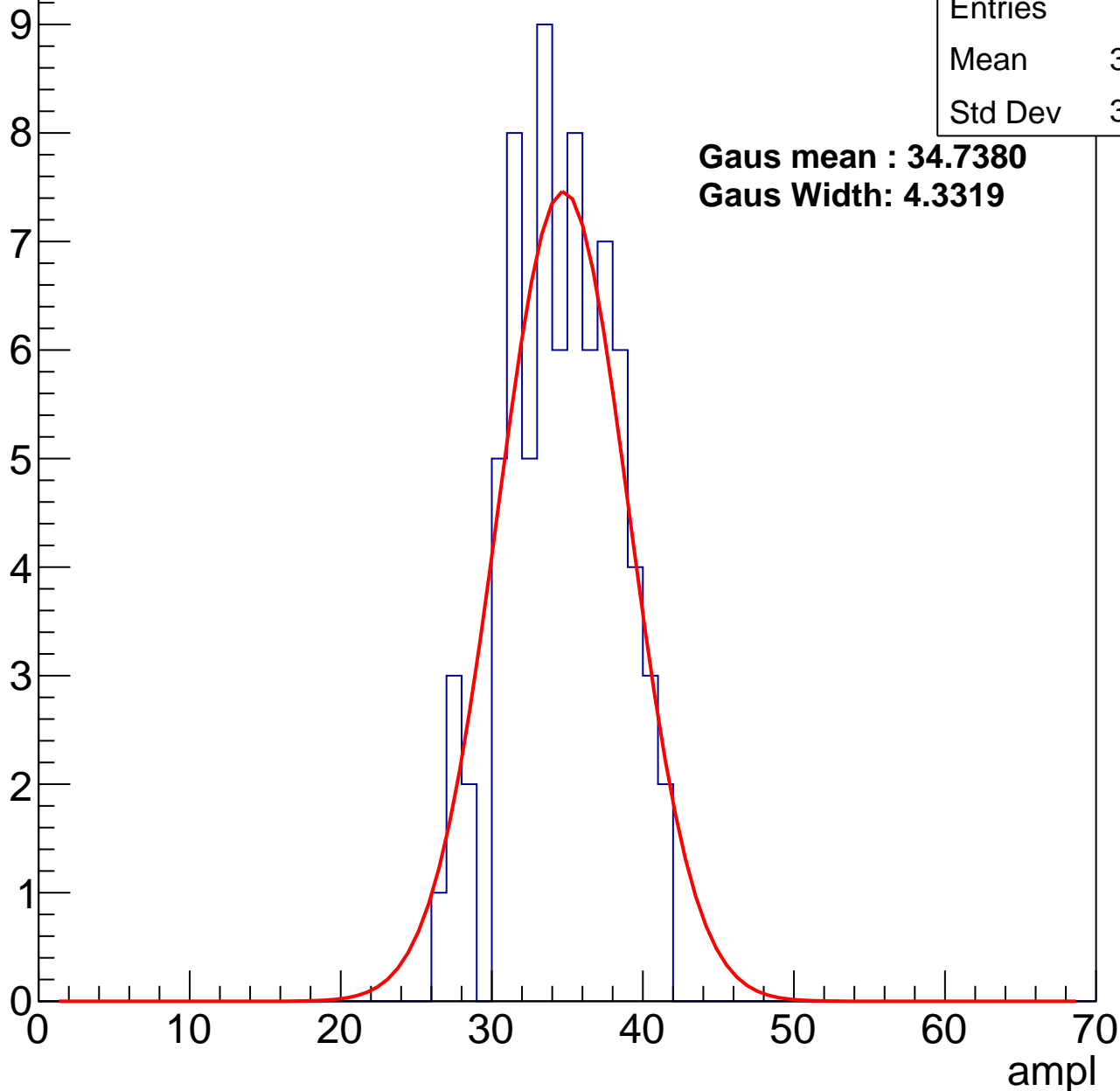
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	34.17
Std Dev	3.575

**Gaus mean : 34.7380**

**Gaus Width: 4.3319**



# B1L102S, U5-ch24, adc2

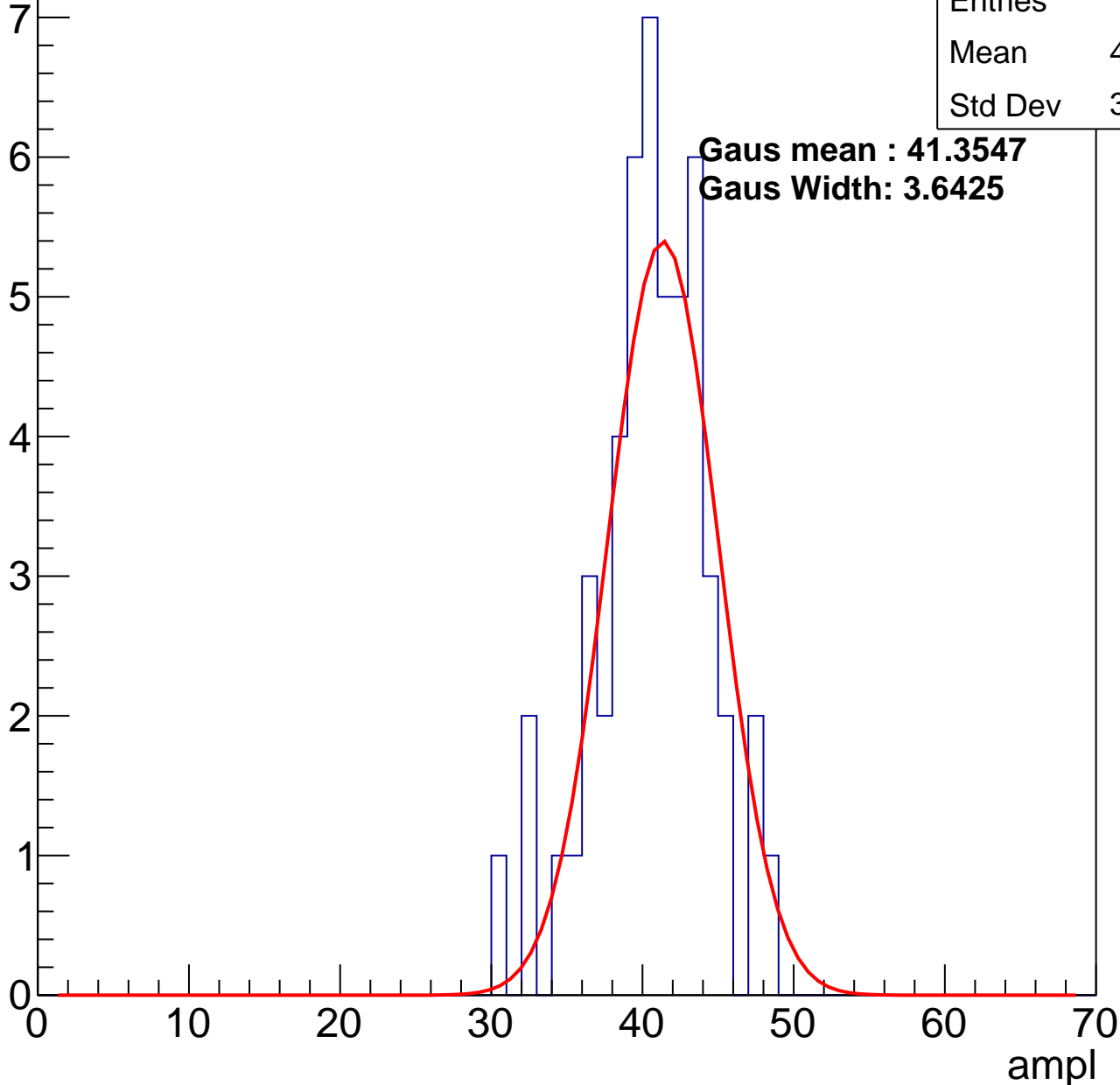
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	40.16
Std Dev	3.744

**Gaus mean : 41.3547**

**Gaus Width: 3.6425**

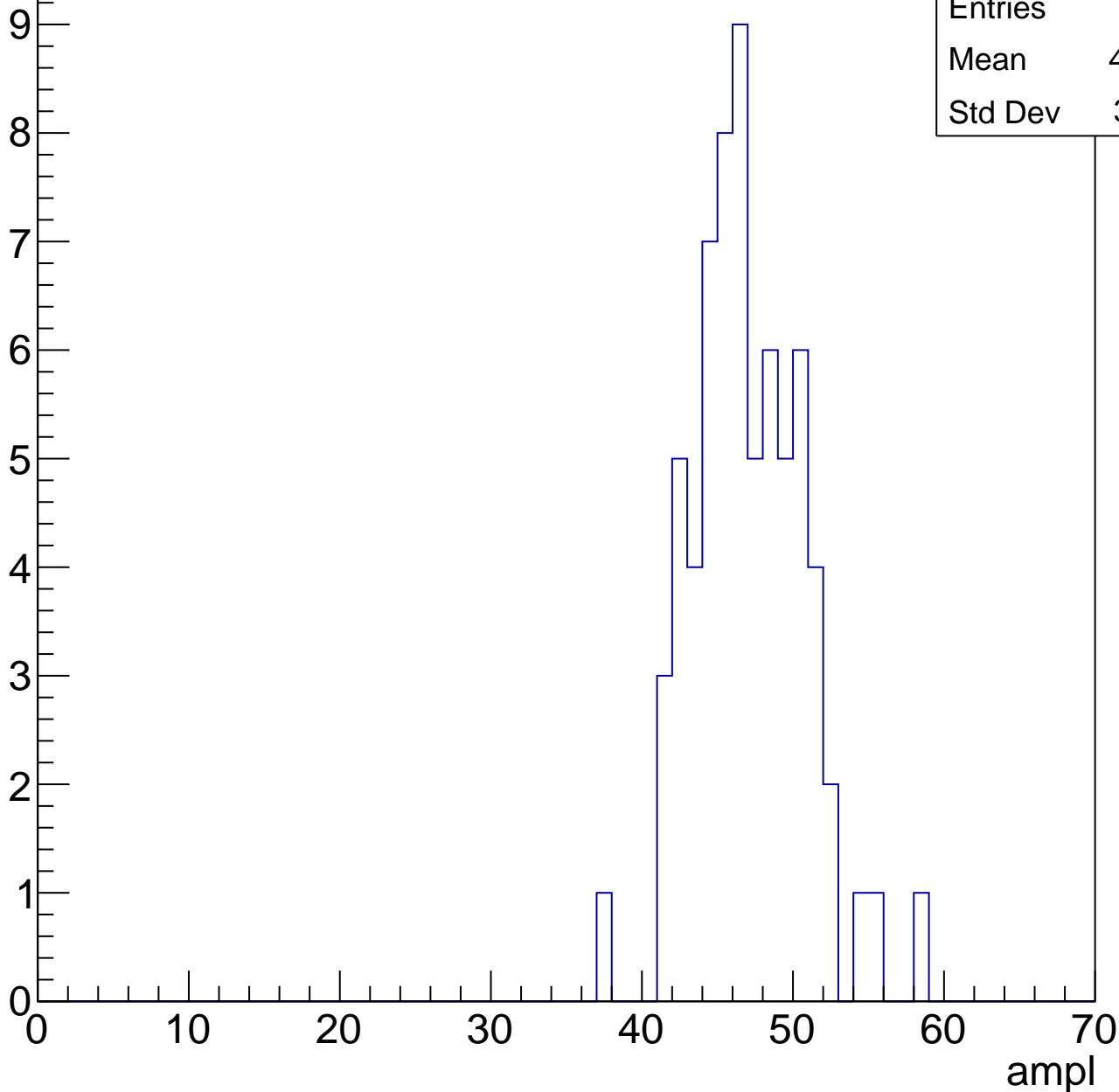


# B1L102S, U5-ch24, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	46.57
Std Dev	3.671

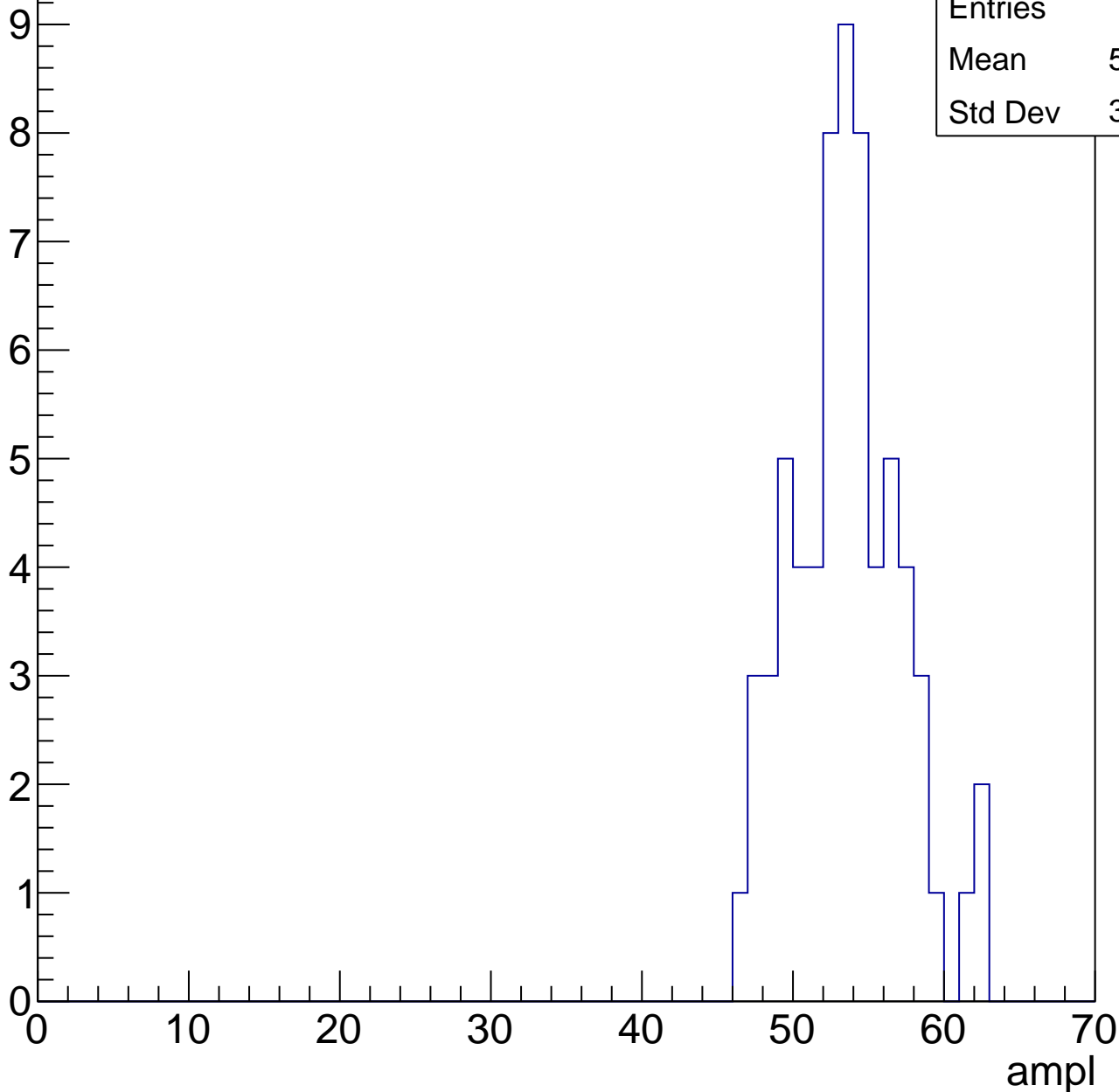


# B1L102S, U5-ch24, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	53.09
Std Dev	3.598

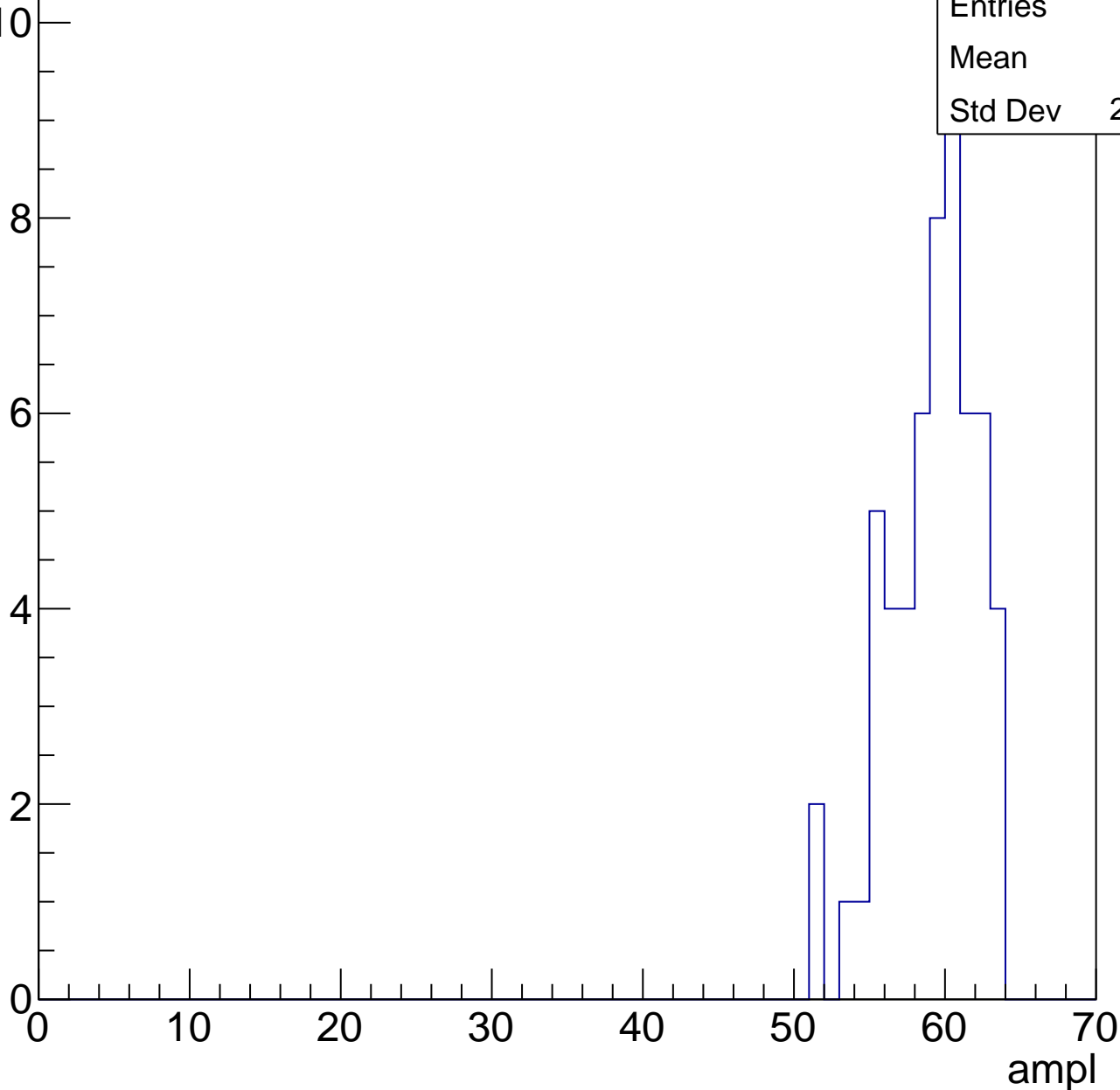


# B1L102S, U5-ch24, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	58.7
Std Dev	2.883

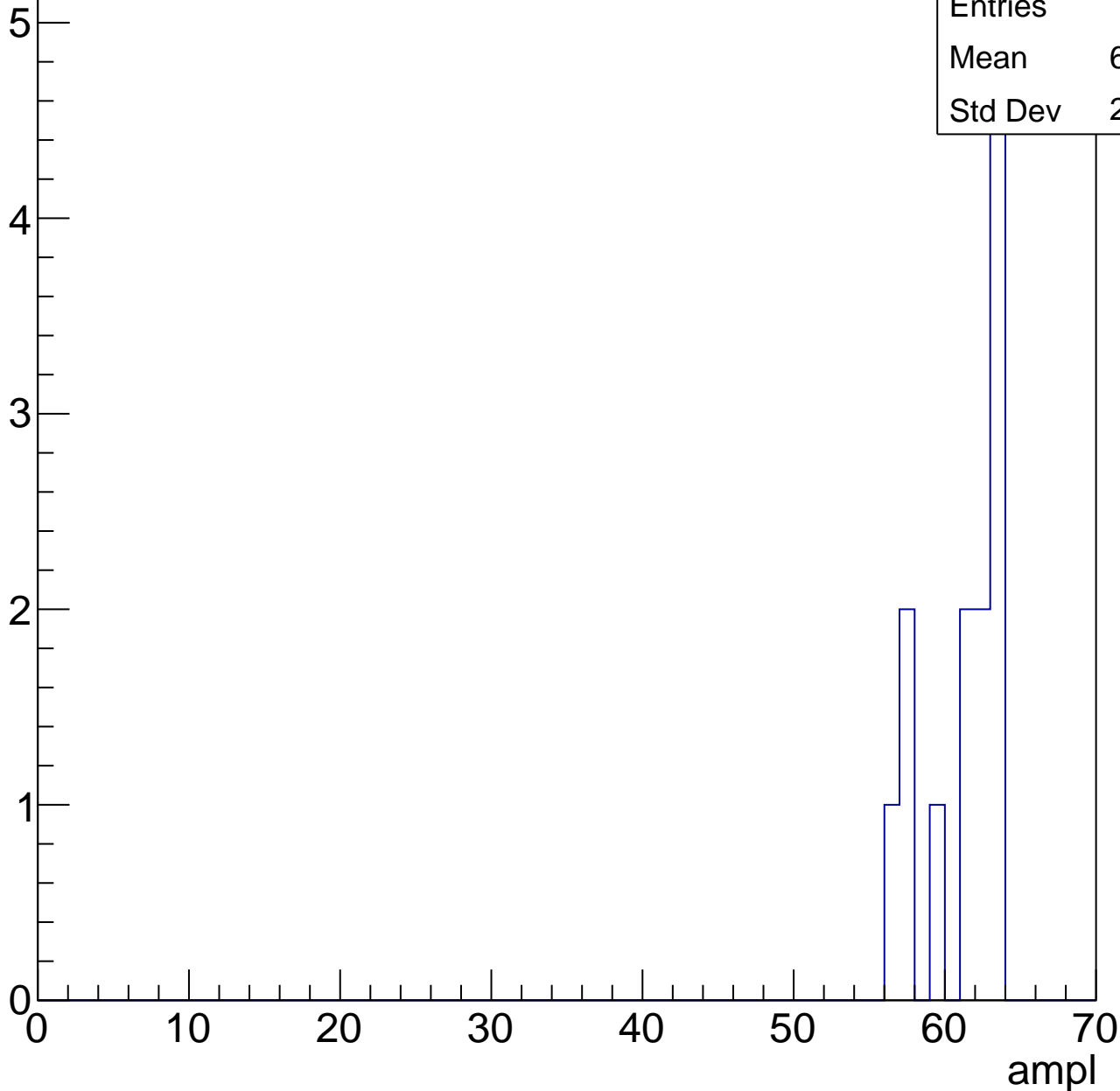


# B1L102S, U5-ch24, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	13
Mean	60.77
Std Dev	2.516

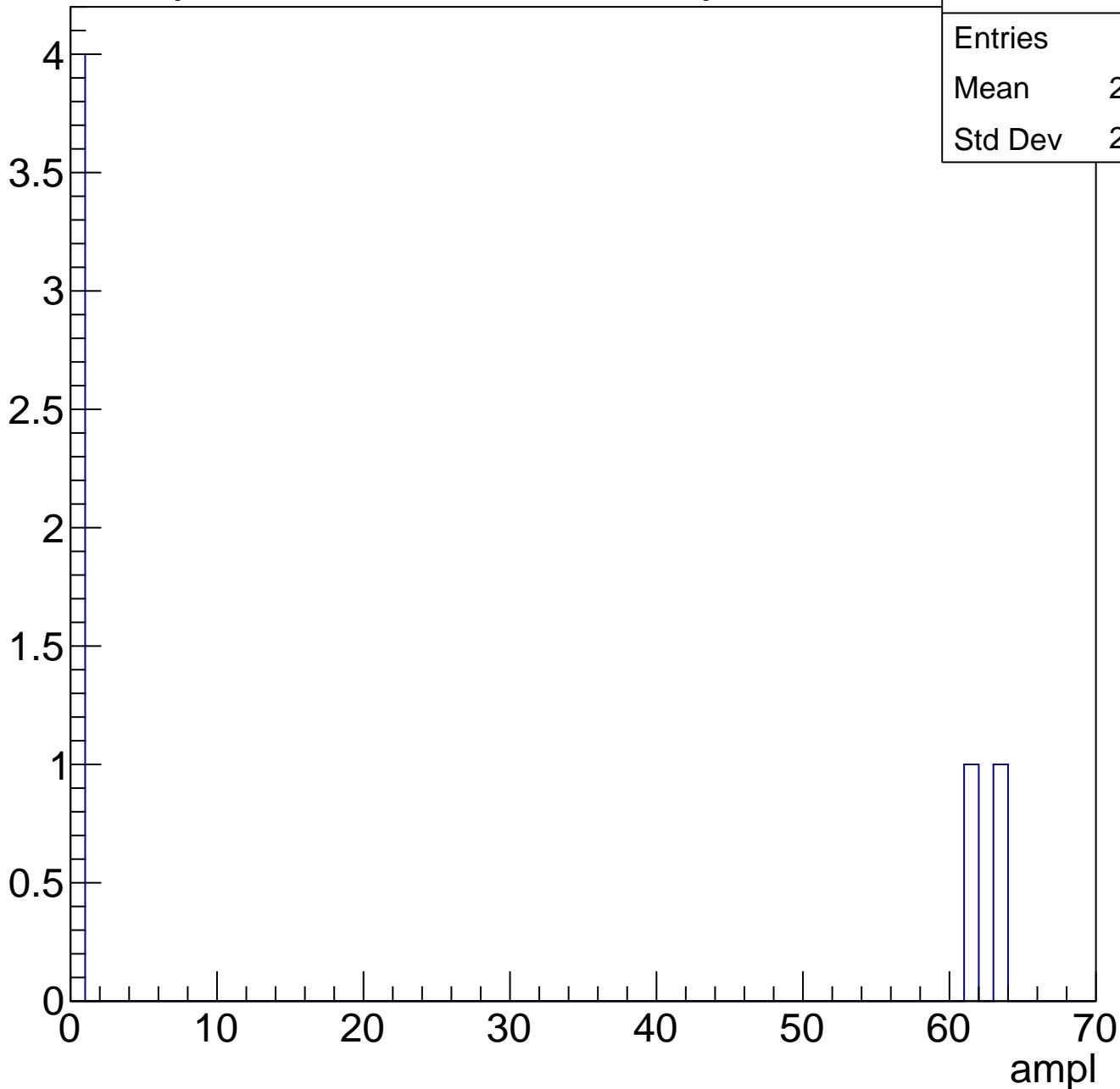




# B1L102S, U5-ch24, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	6
Mean	20.67
Std Dev	29.23

# B1L102S, U5-ch25, adc0

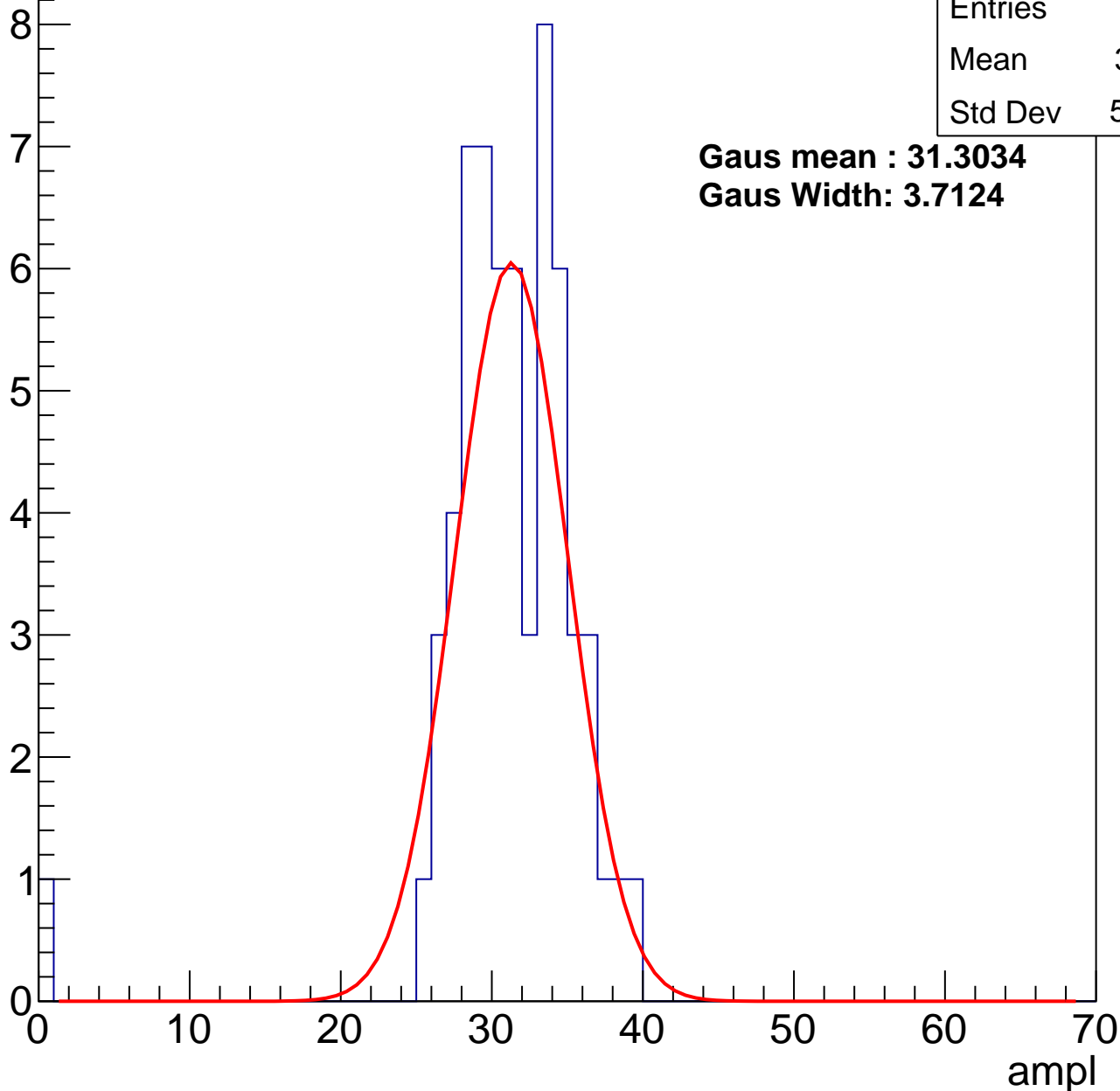
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	30.61
Std Dev	5.097

**Gaus mean : 31.3034**

**Gaus Width: 3.7124**



# B1L102S, U5-ch25, adc1

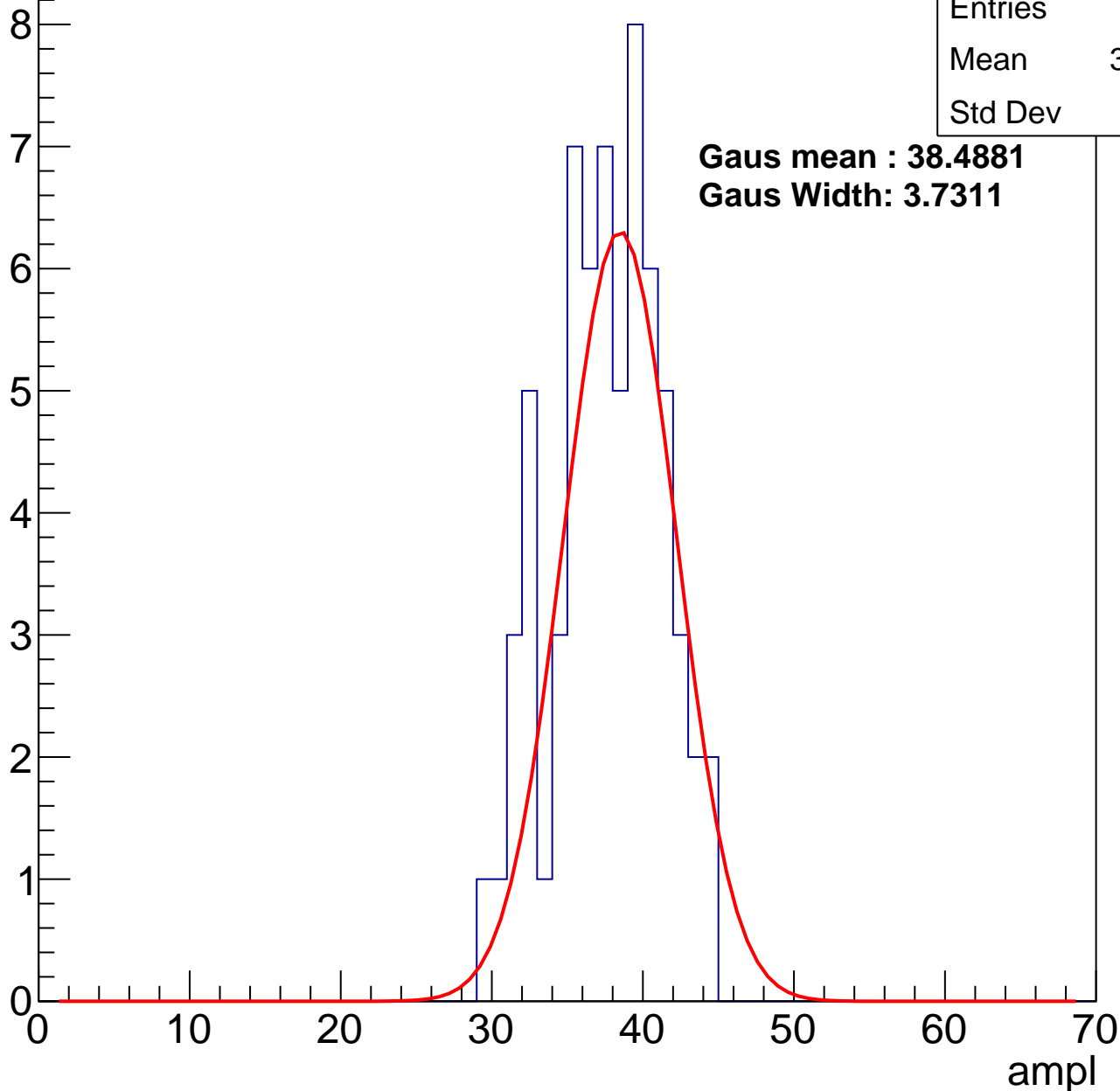
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	37.14
Std Dev	3.59

**Gaus mean : 38.4881**

**Gaus Width: 3.7311**



# B1L102S, U5-ch25, adc2

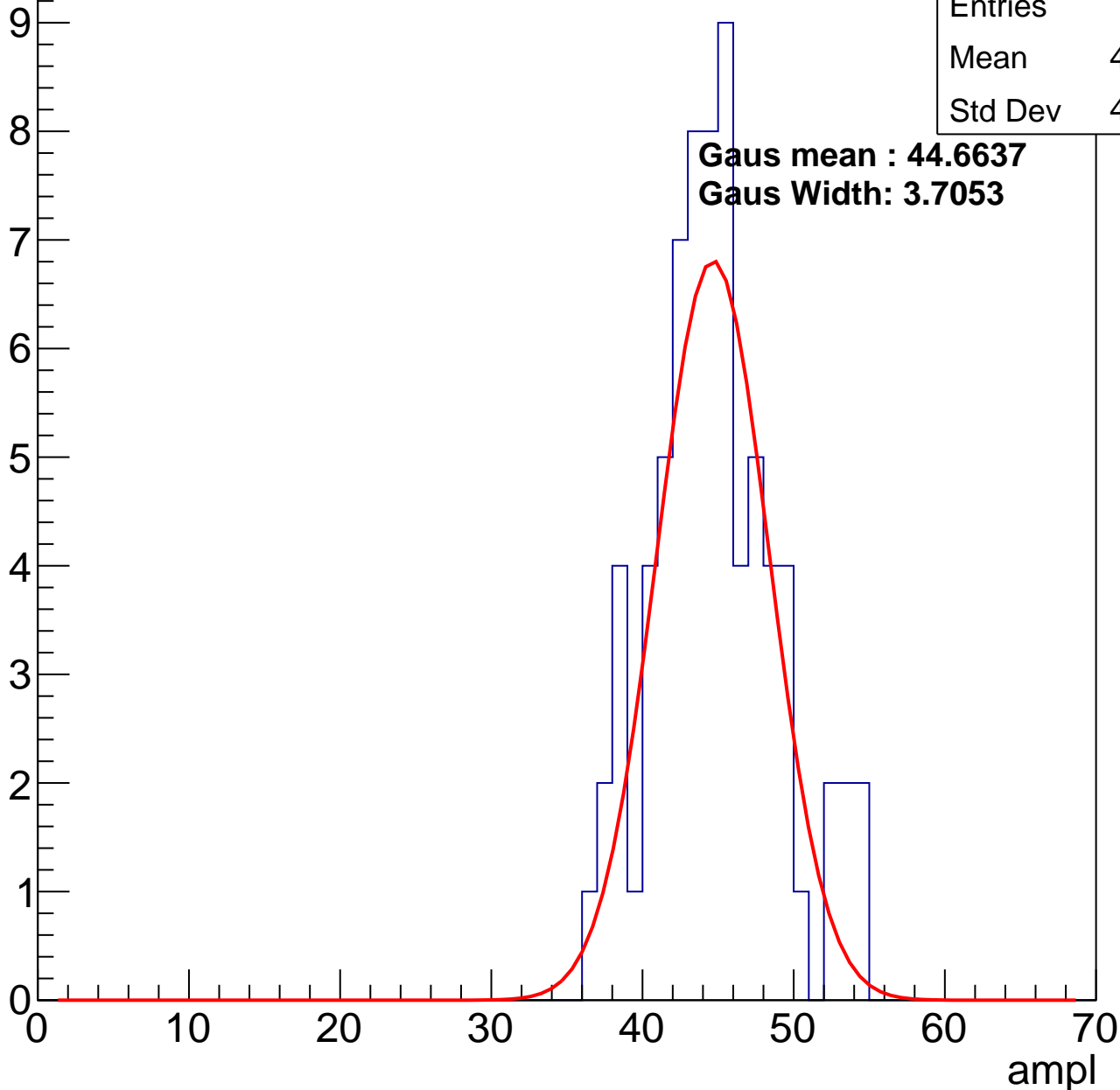
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	44.33
Std Dev	4.102

**Gaus mean : 44.6637**

**Gaus Width: 3.7053**

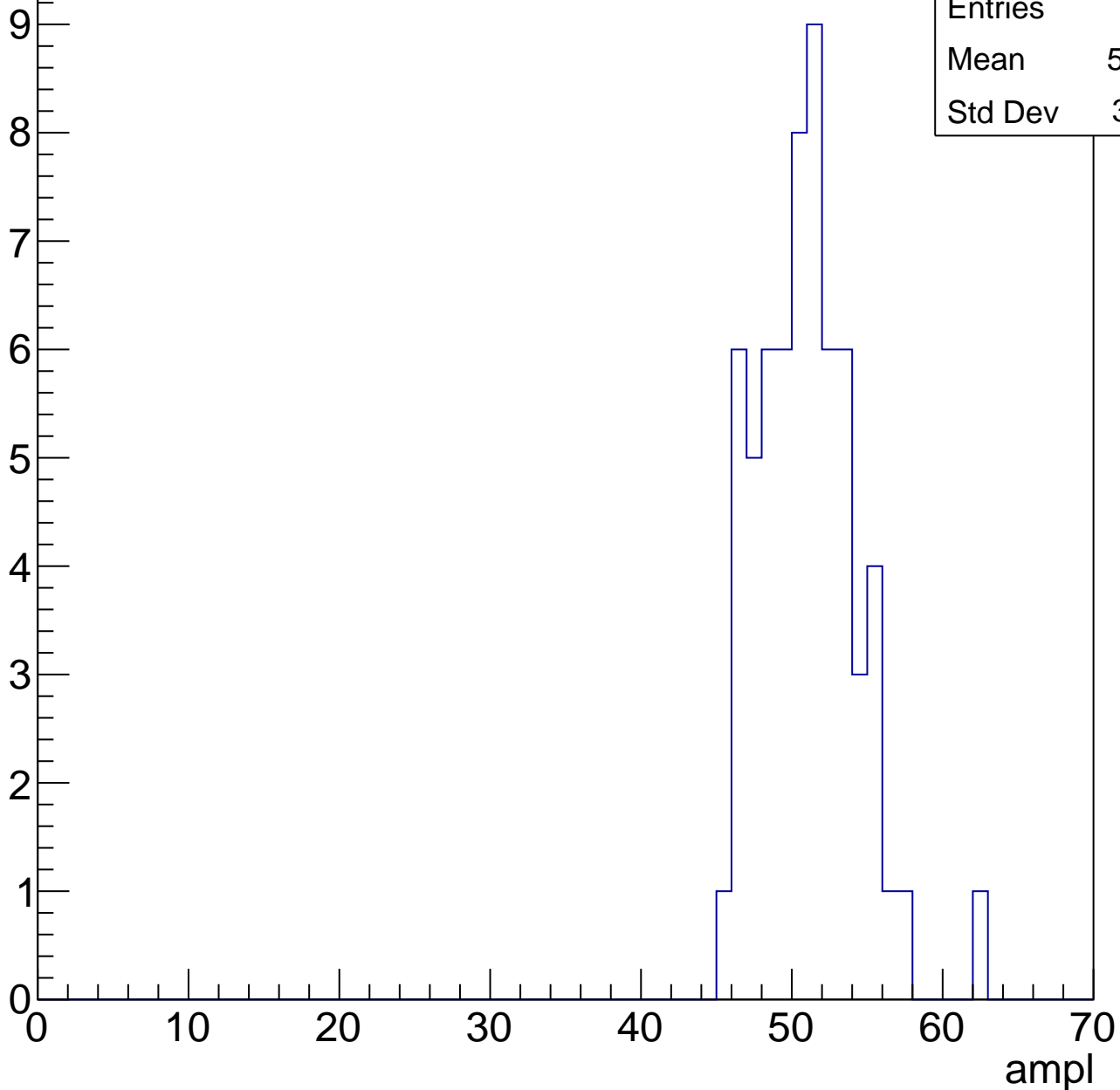


# B1L102S, U5-ch25, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

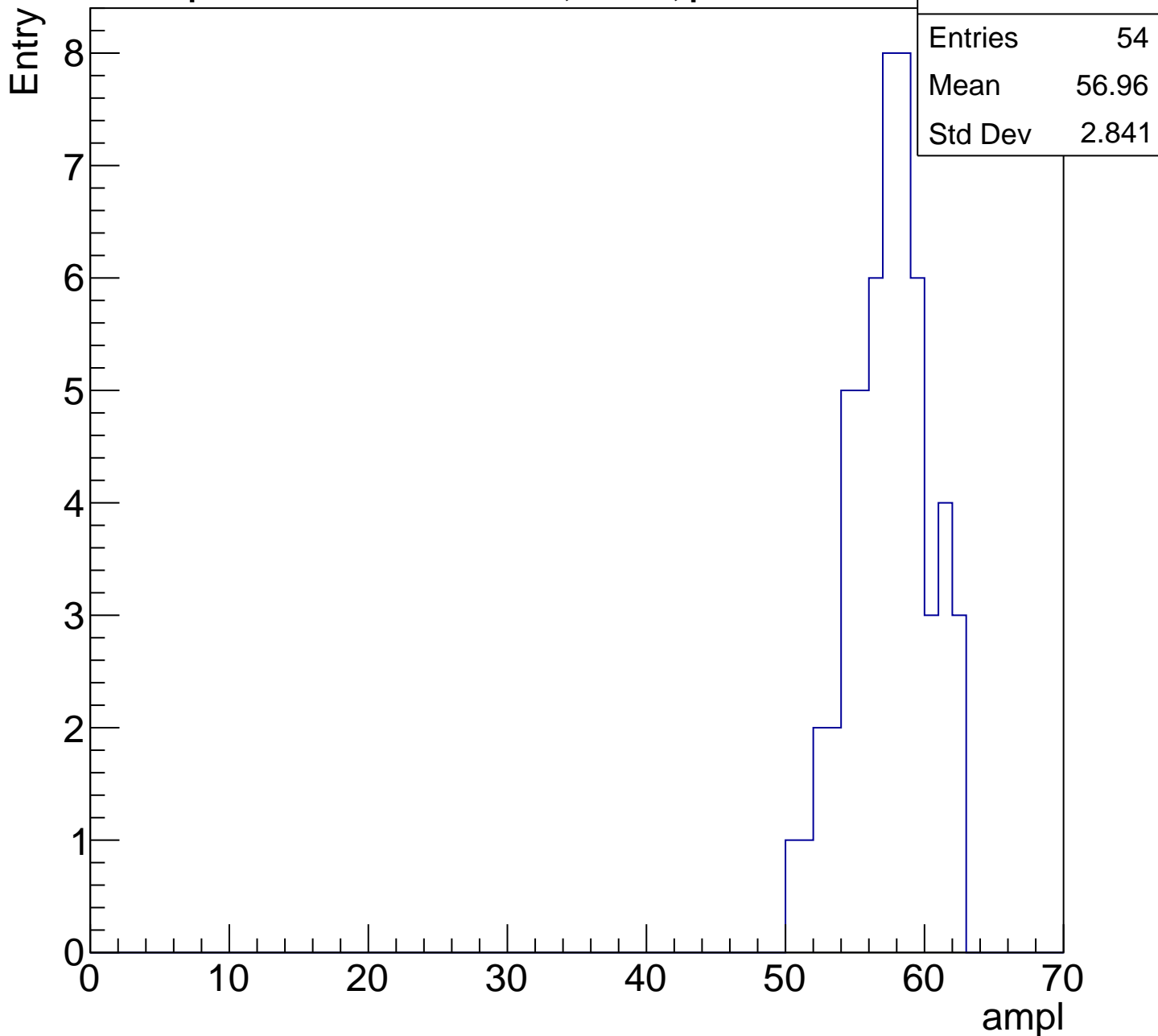
Entry

Entries	63
Mean	50.54
Std Dev	3.191



# B1L102S, U5-ch25, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

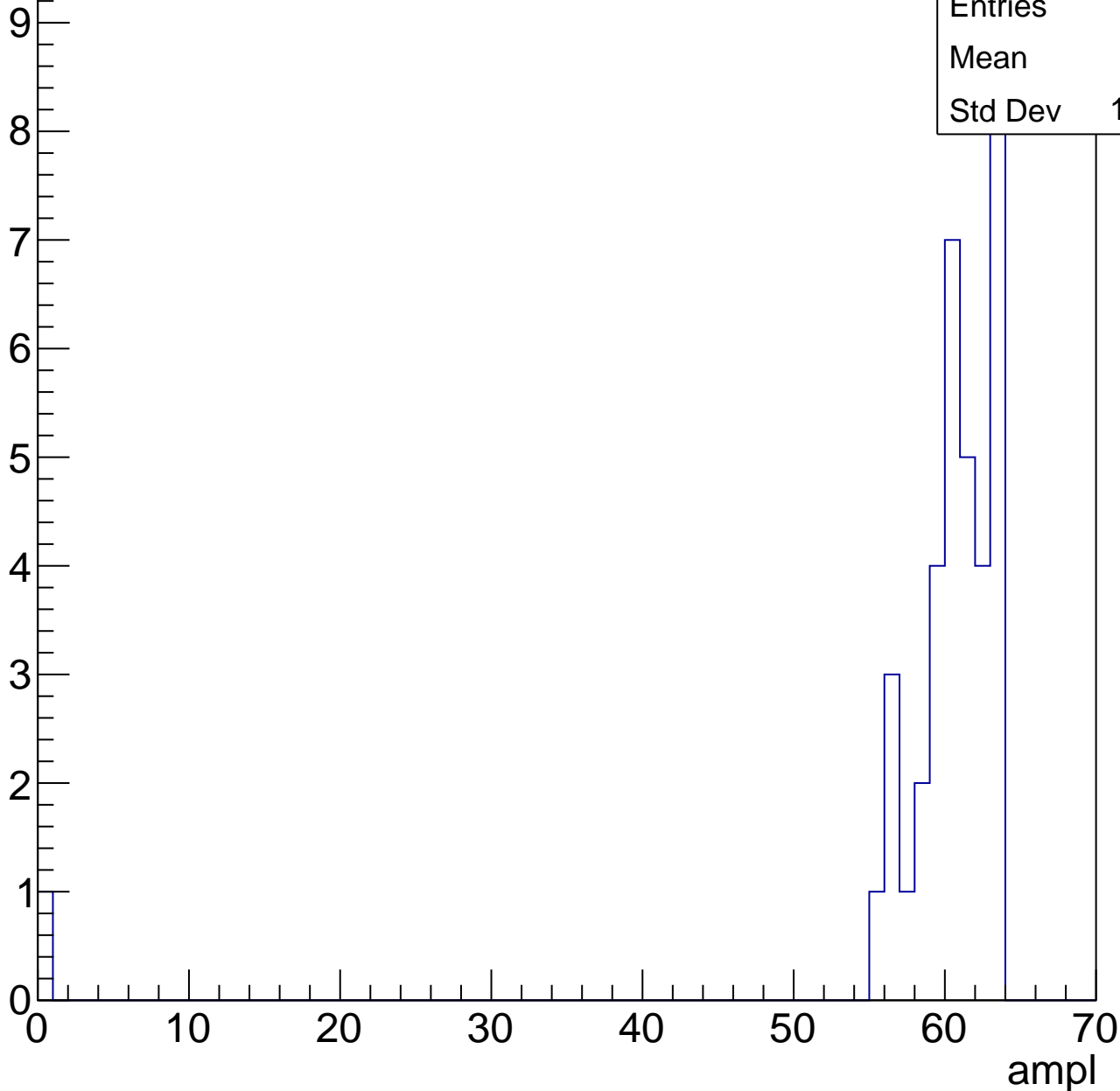


# B1L102S, U5-ch25, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	37
Mean	58.7
Std Dev	10.05



# B1L102S, U5-ch25, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

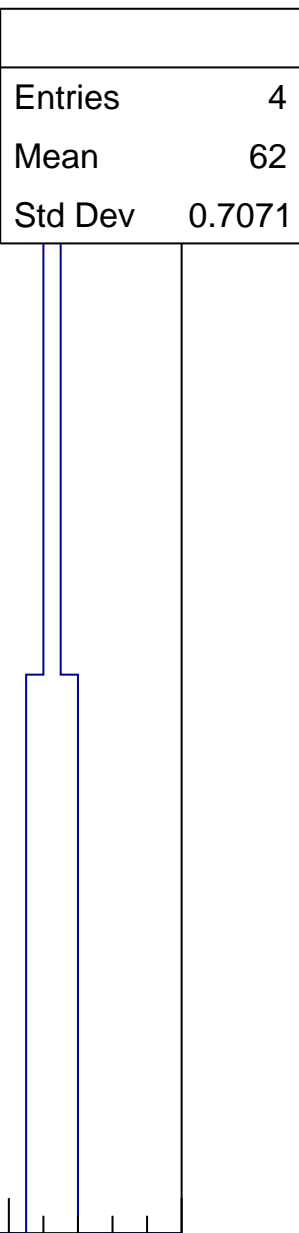
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	62
Std Dev	0.7071

0 10 20 30 40 50 60 70

ampl





# B1L102S, U5-ch25, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	25
Std Dev	0

ampl

# B1L102S, U5-ch26, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	70
Mean	27
Std Dev	3.641

**Gaus mean : 27.0337**

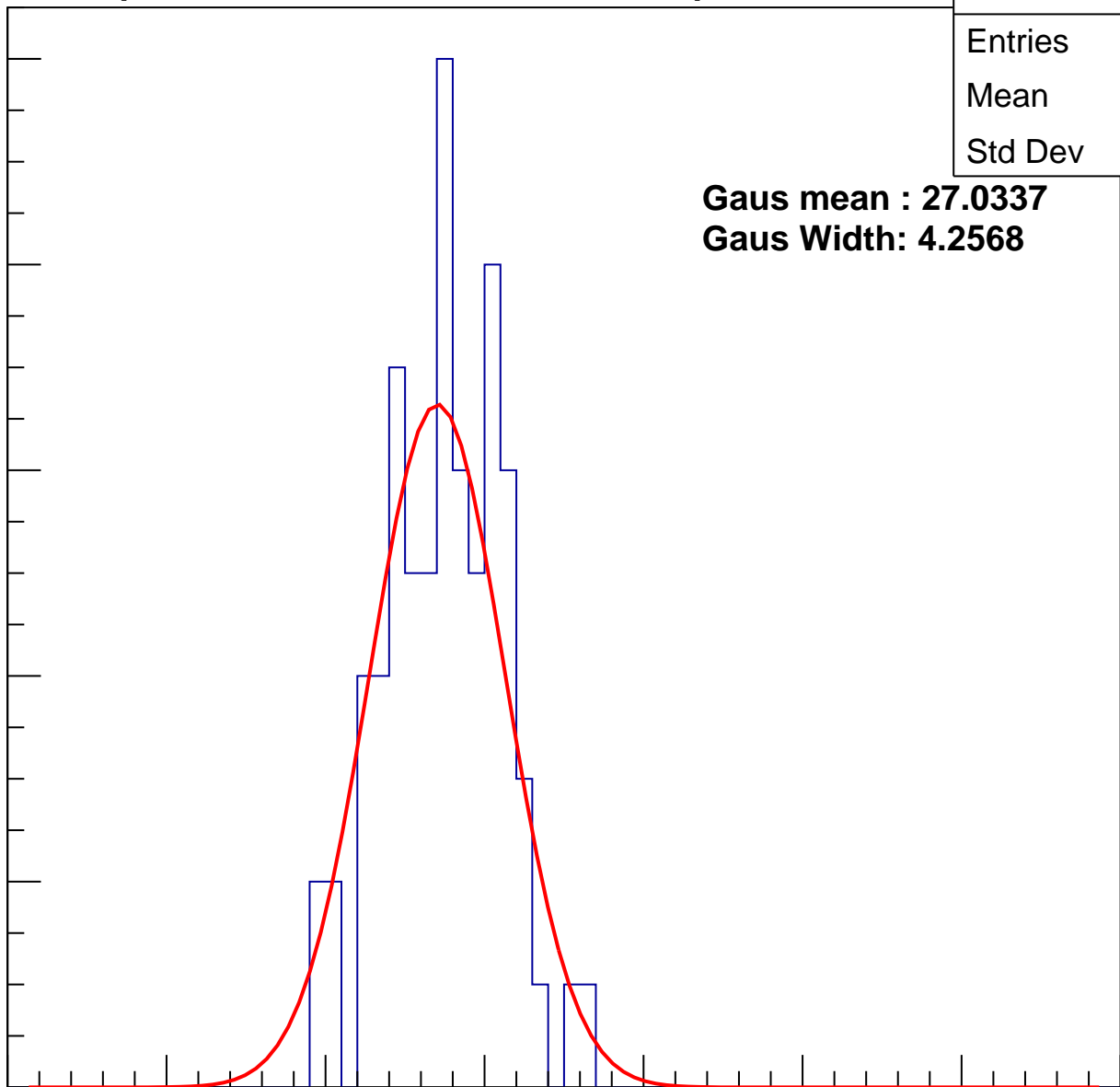
**Gaus Width: 4.2568**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U5-ch26, adc1

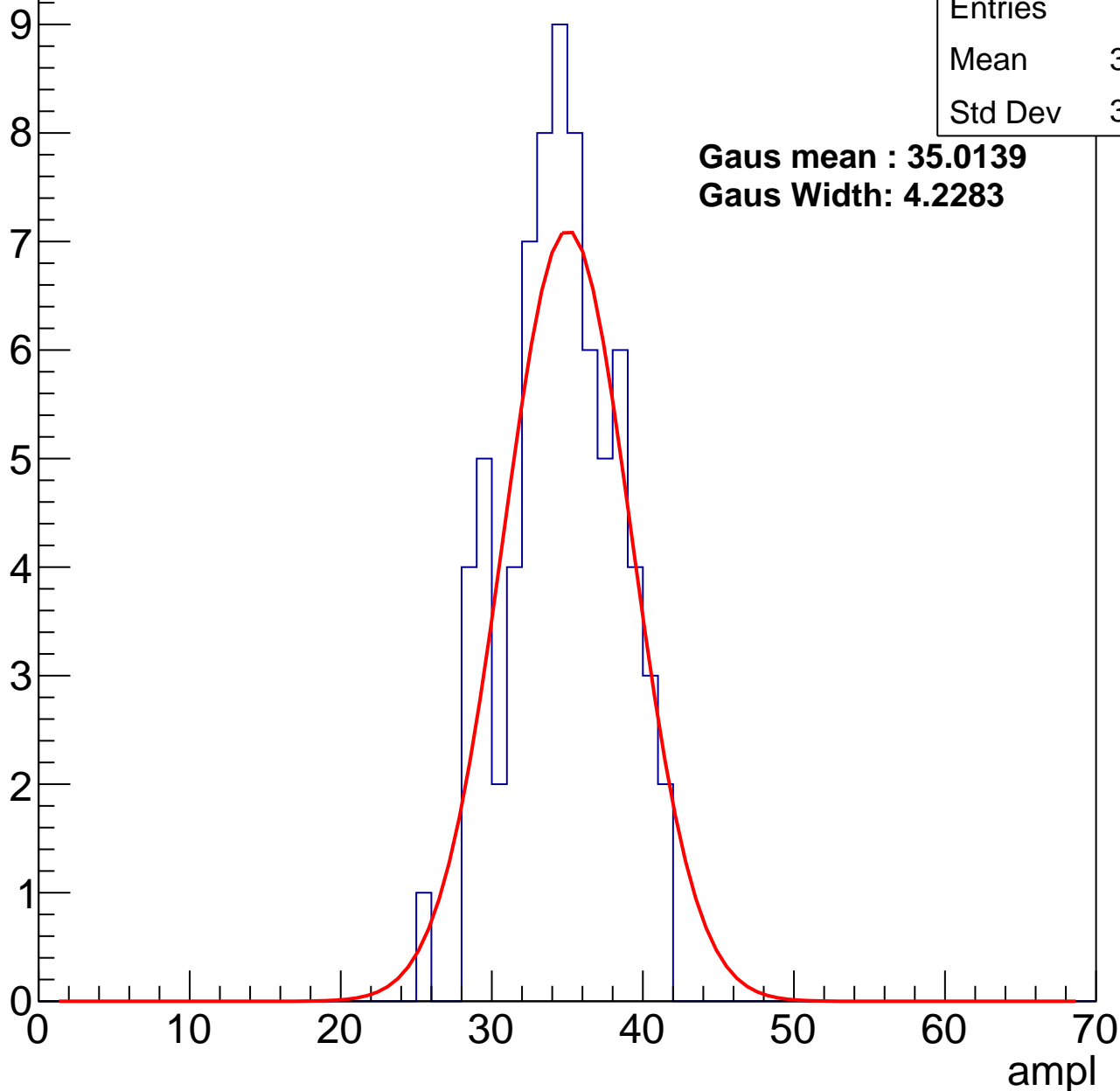
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	34.15
Std Dev	3.548

**Gaus mean : 35.0139**

**Gaus Width: 4.2283**

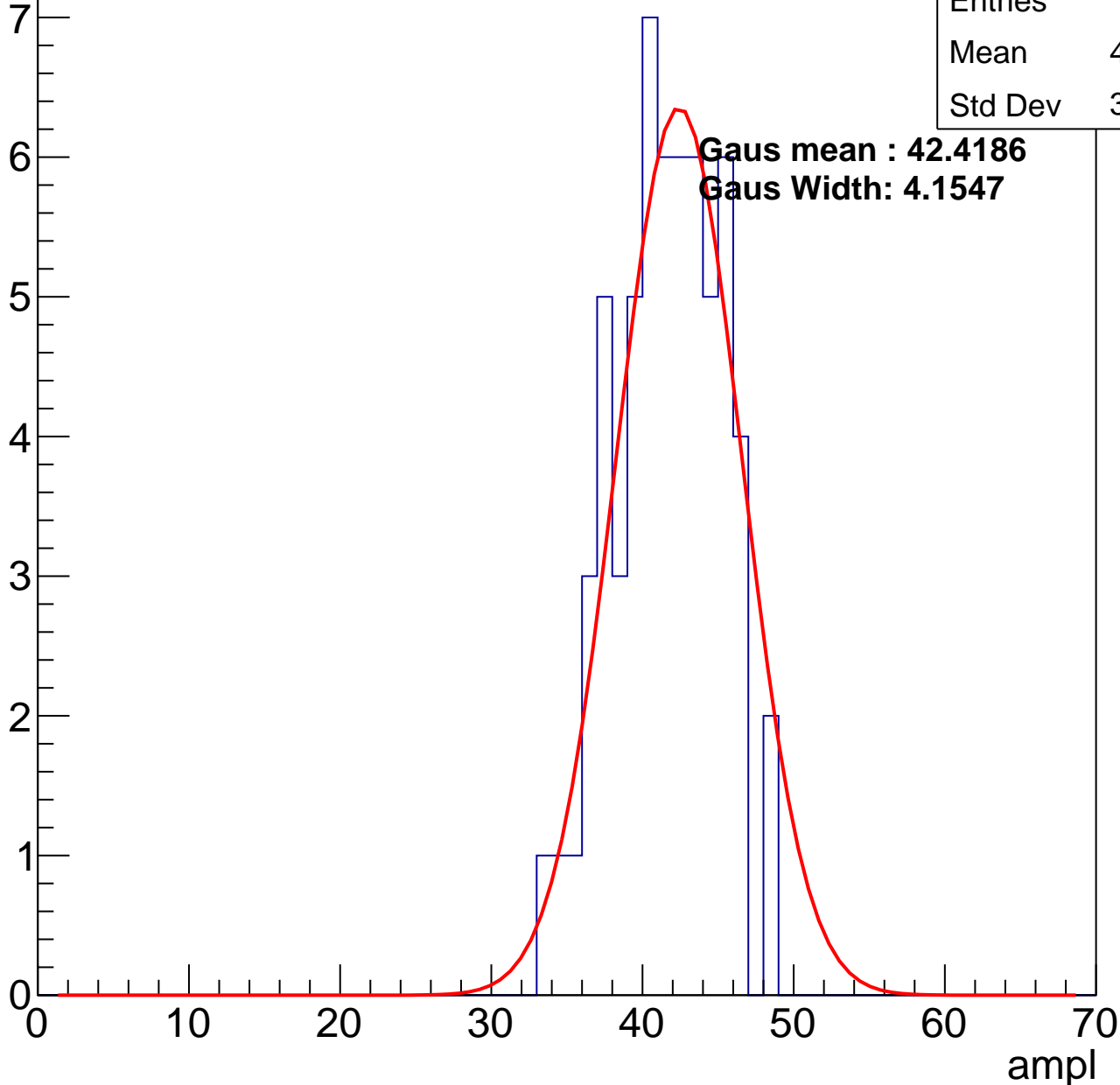


# B1L102S, U5-ch26, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	41.15
Std Dev	3.449



# B1L102S, U5-ch26, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	78
Mean	47.9
Std Dev	4.008

Entry

10

8

6

4

2

0

0

10

20

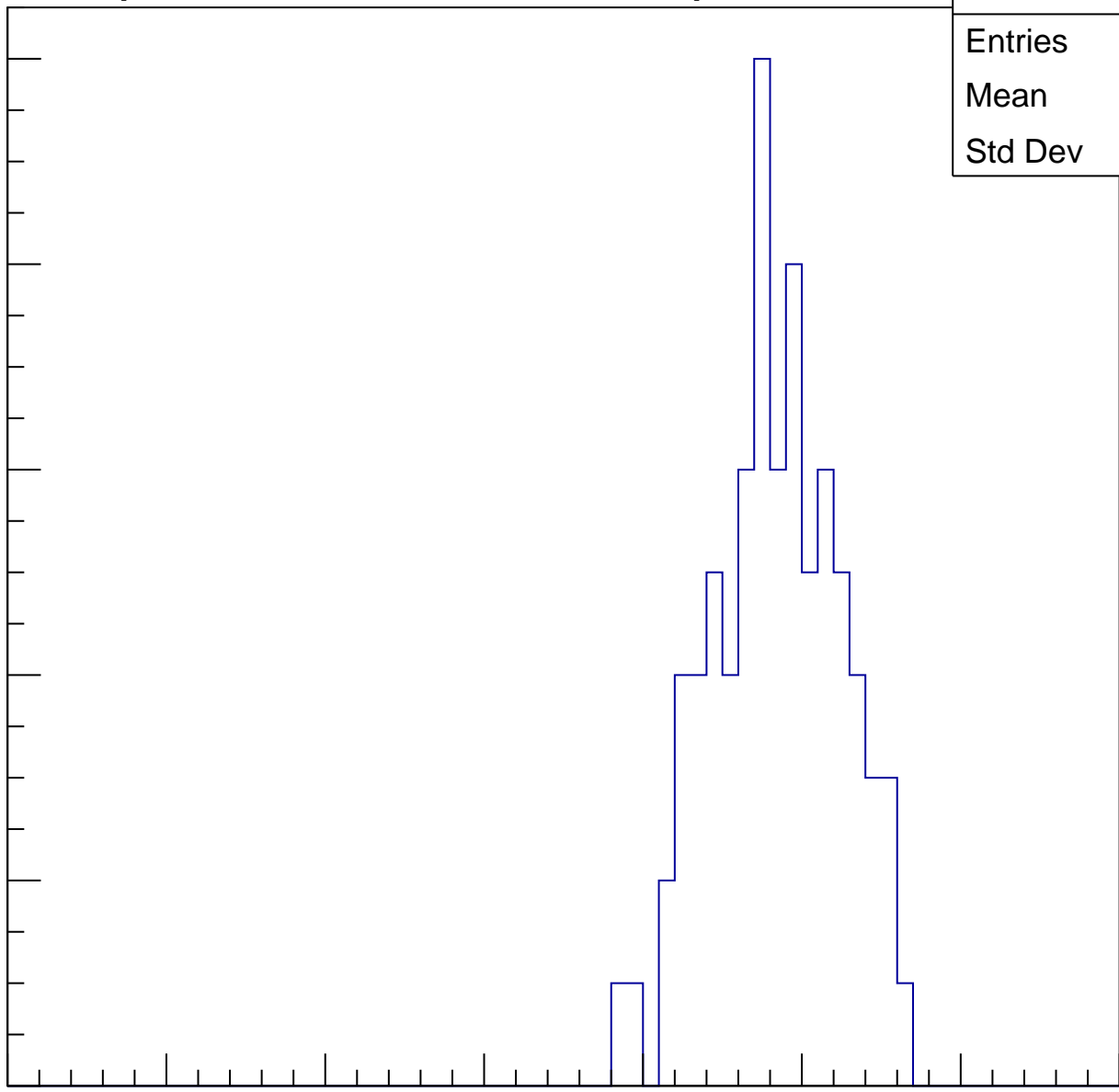
30

40

50

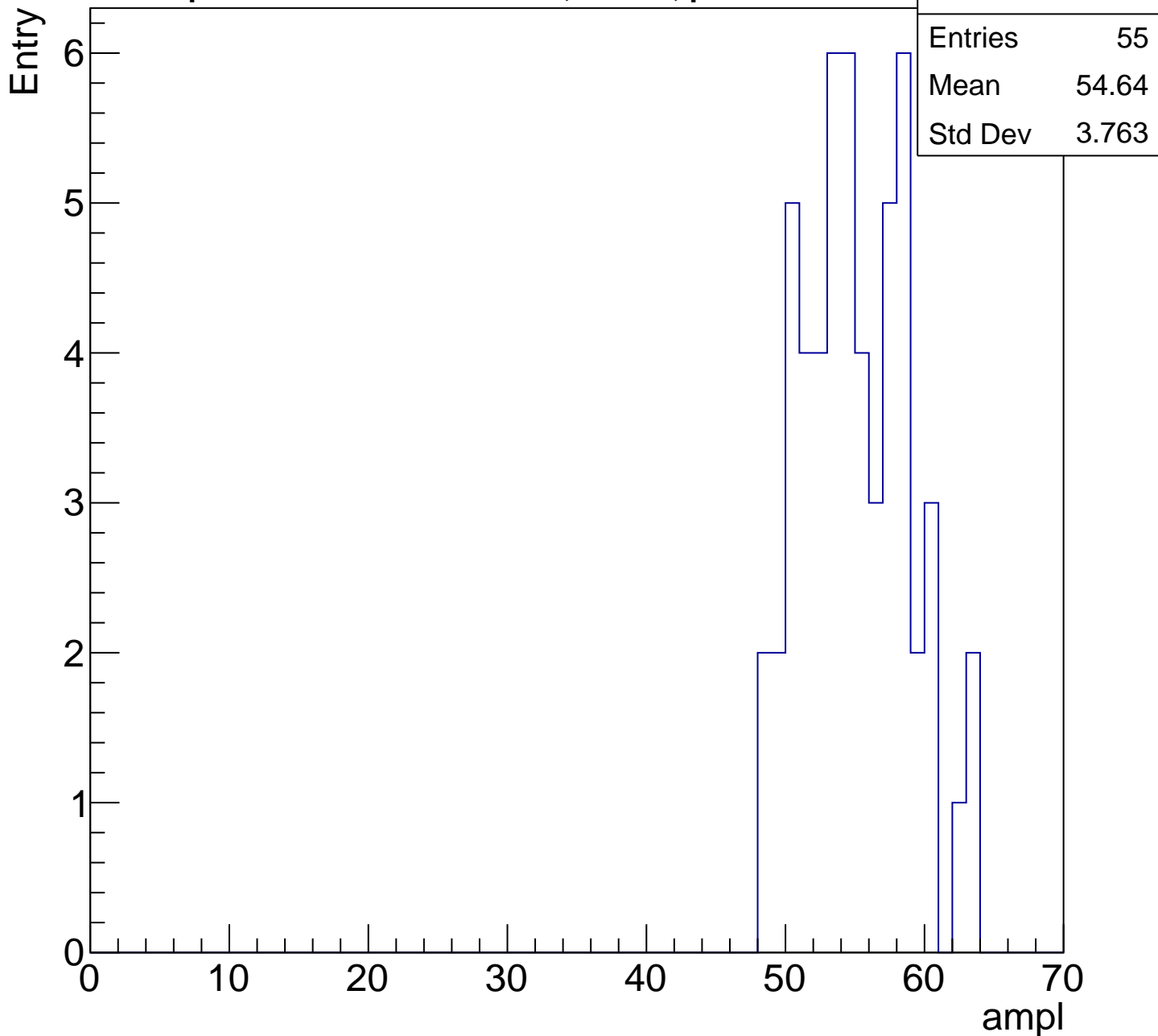
60

ampl



# B1L102S, U5-ch26, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

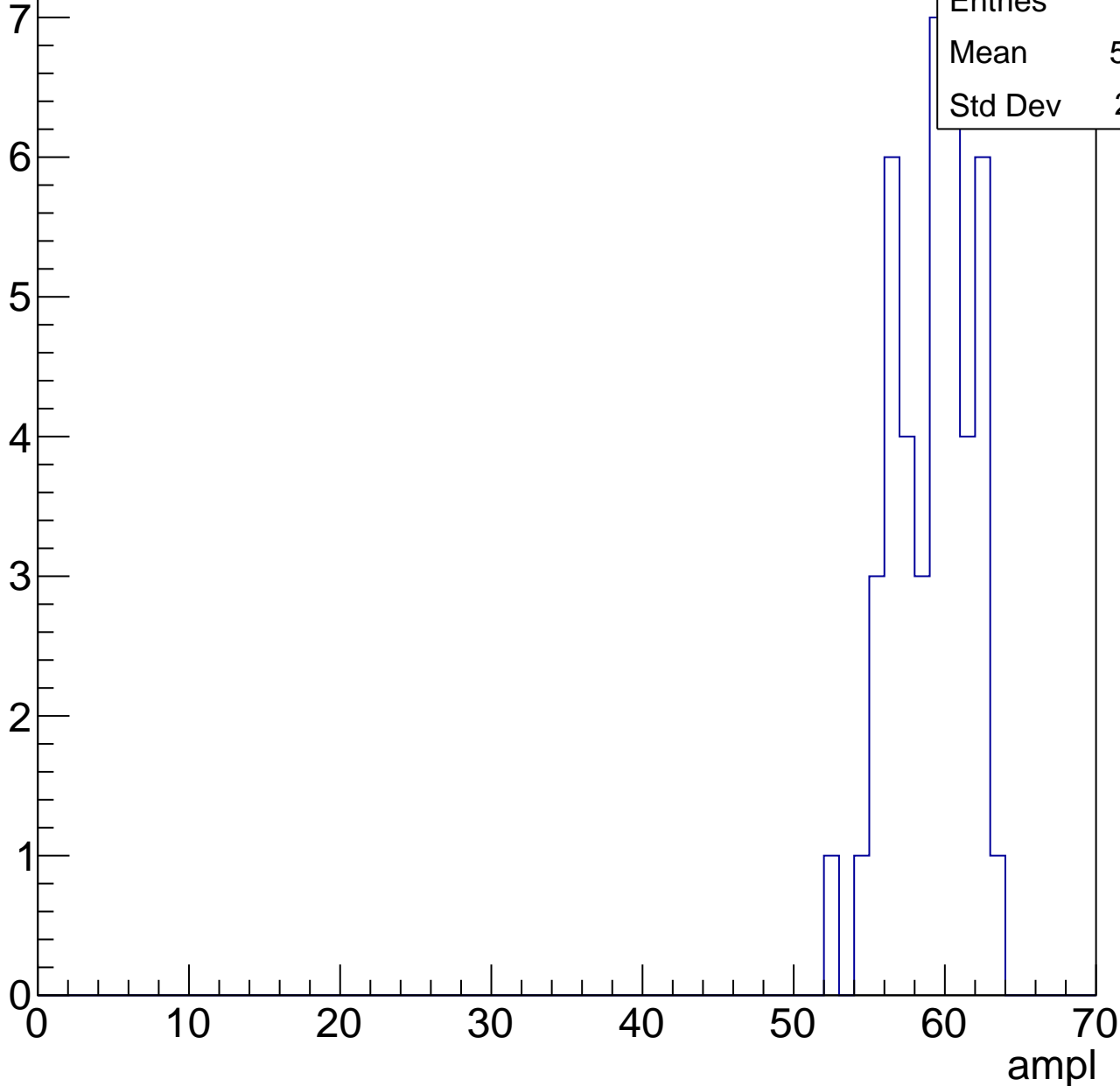


# B1L102S, U5-ch26, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	43
Mean	58.63
Std Dev	2.561

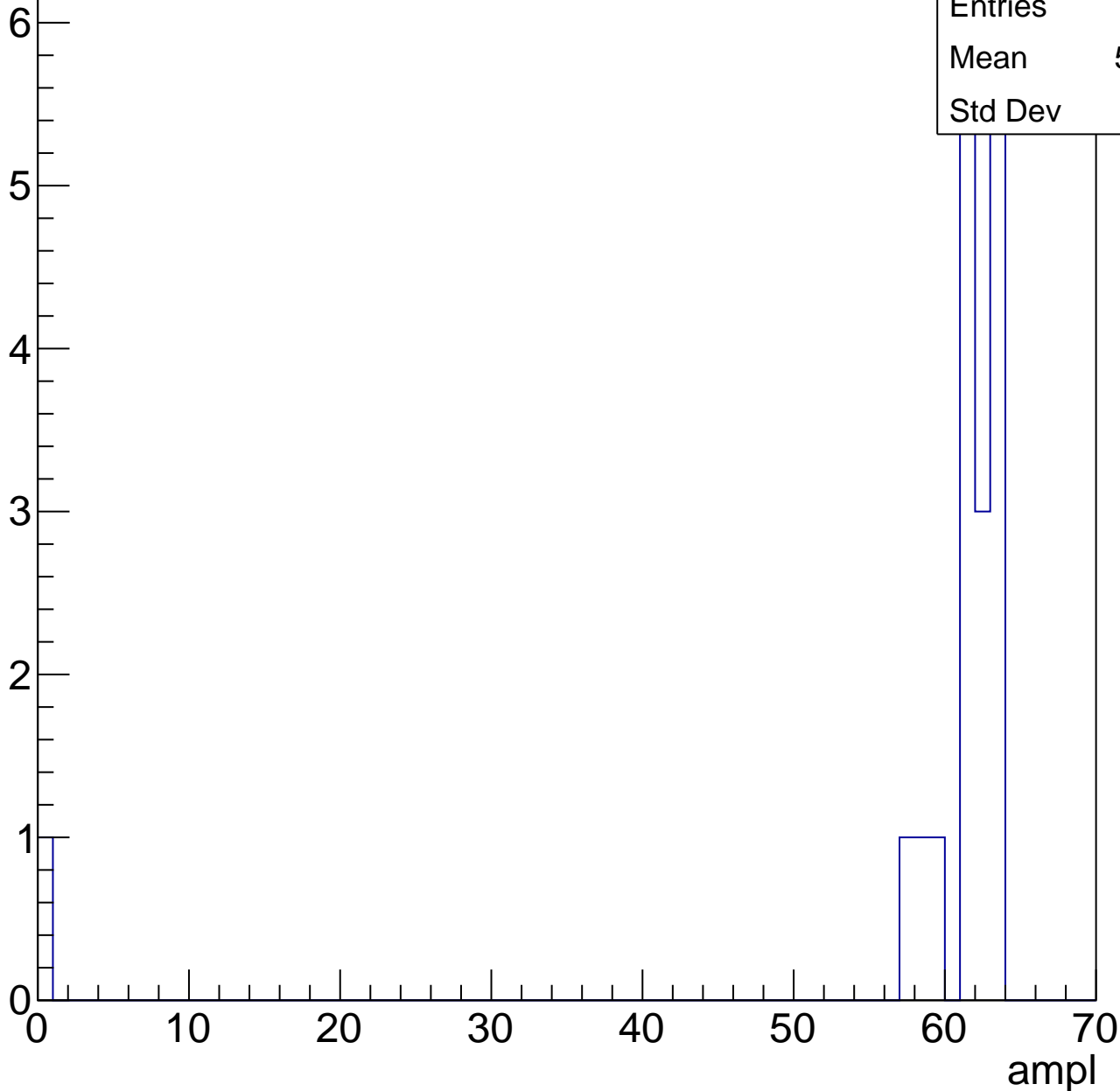


# B1L102S, U5-ch26, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	19
Mean	58.11
Std Dev	13.8





# B1L102S, U5-ch26, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U5-ch27, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	85
Mean	27.41
Std Dev	4.907

**Gaus mean : 28.0995**

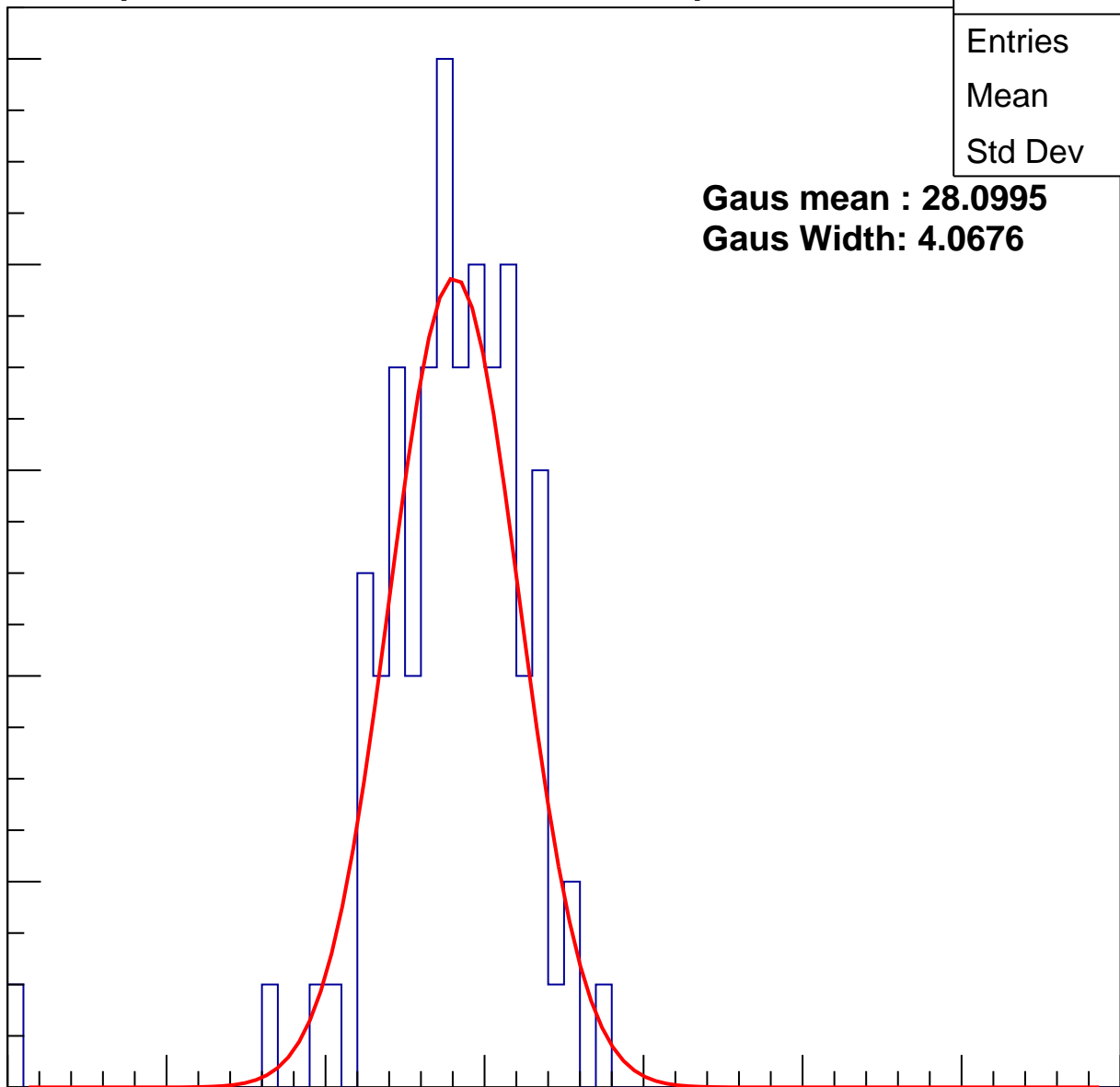
**Gaus Width: 4.0676**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U5-ch27, adc1

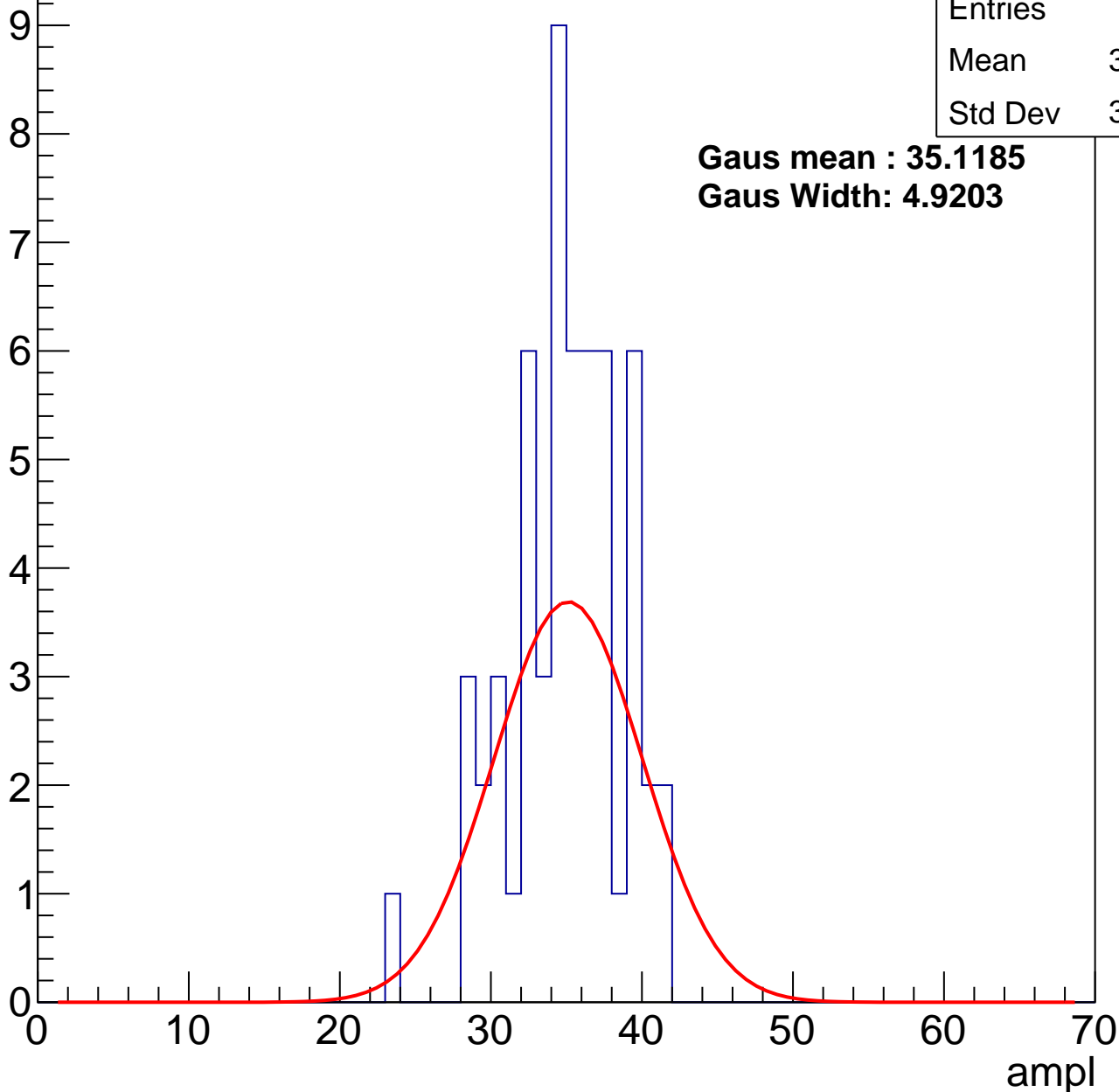
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	34.47
Std Dev	3.676

**Gaus mean : 35.1185**

**Gaus Width: 4.9203**



# B1L102S, U5-ch27, adc2

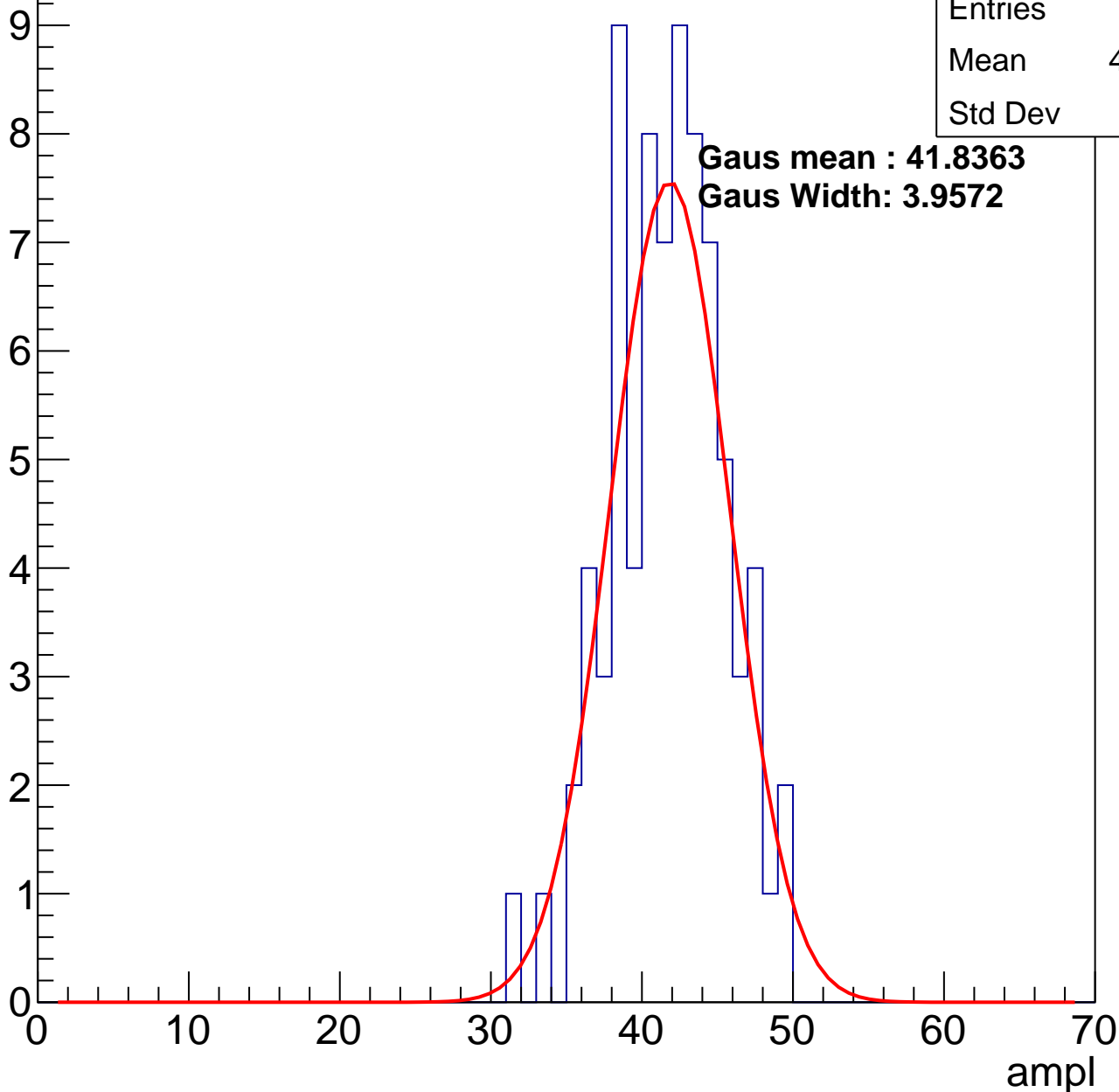
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	78
Mean	41.29
Std Dev	3.69

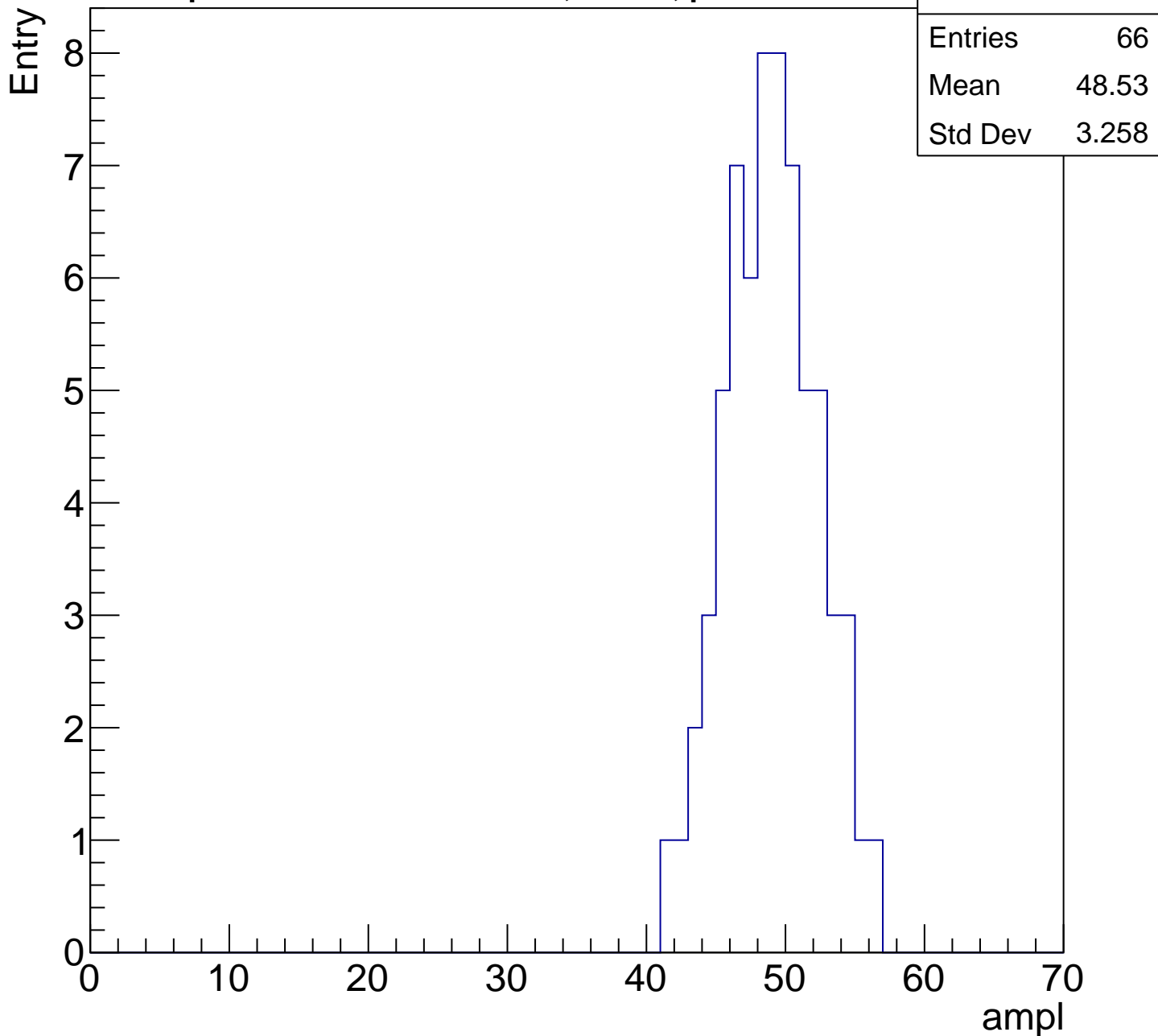
**Gaus mean : 41.8363**

**Gaus Width: 3.9572**



# B1L102S, U5-ch27, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2



# B1L102S, U5-ch27, adc4

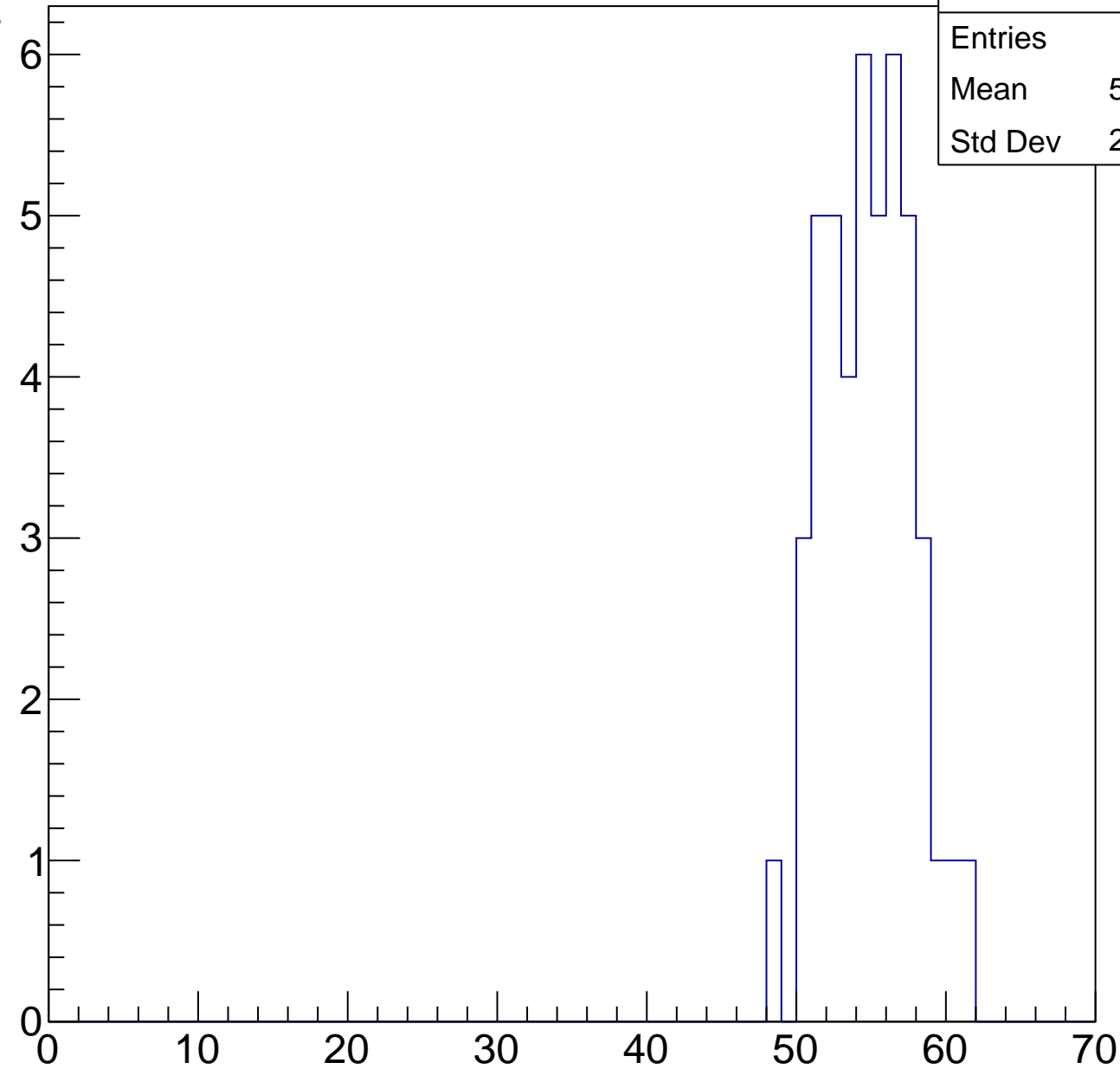
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

6  
5  
4  
3  
2  
1  
0

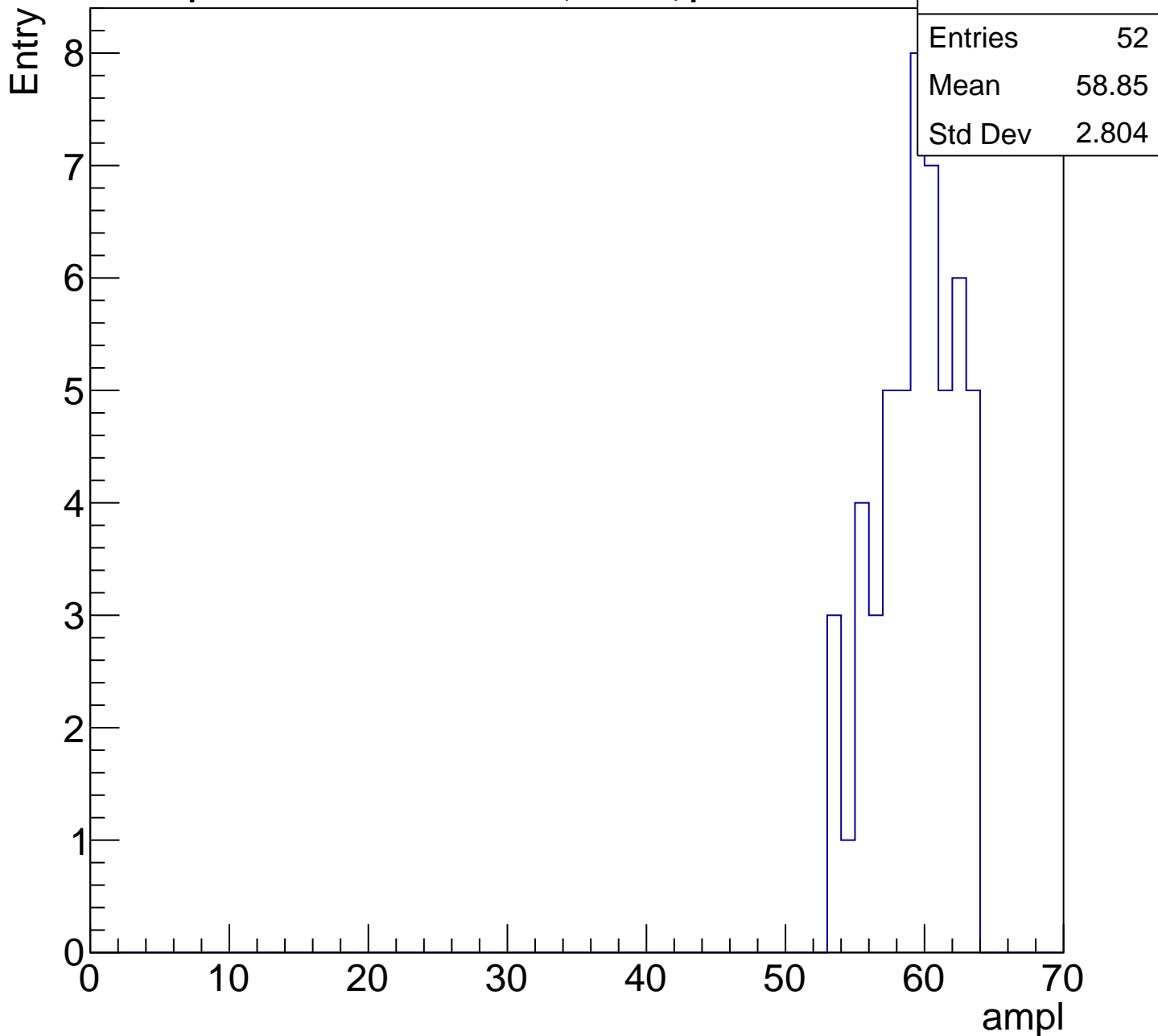
Entries	46
Mean	54.33
Std Dev	2.875

0 10 20 30 40 50 60 70  
ampl



# B1L102S, U5-ch27, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

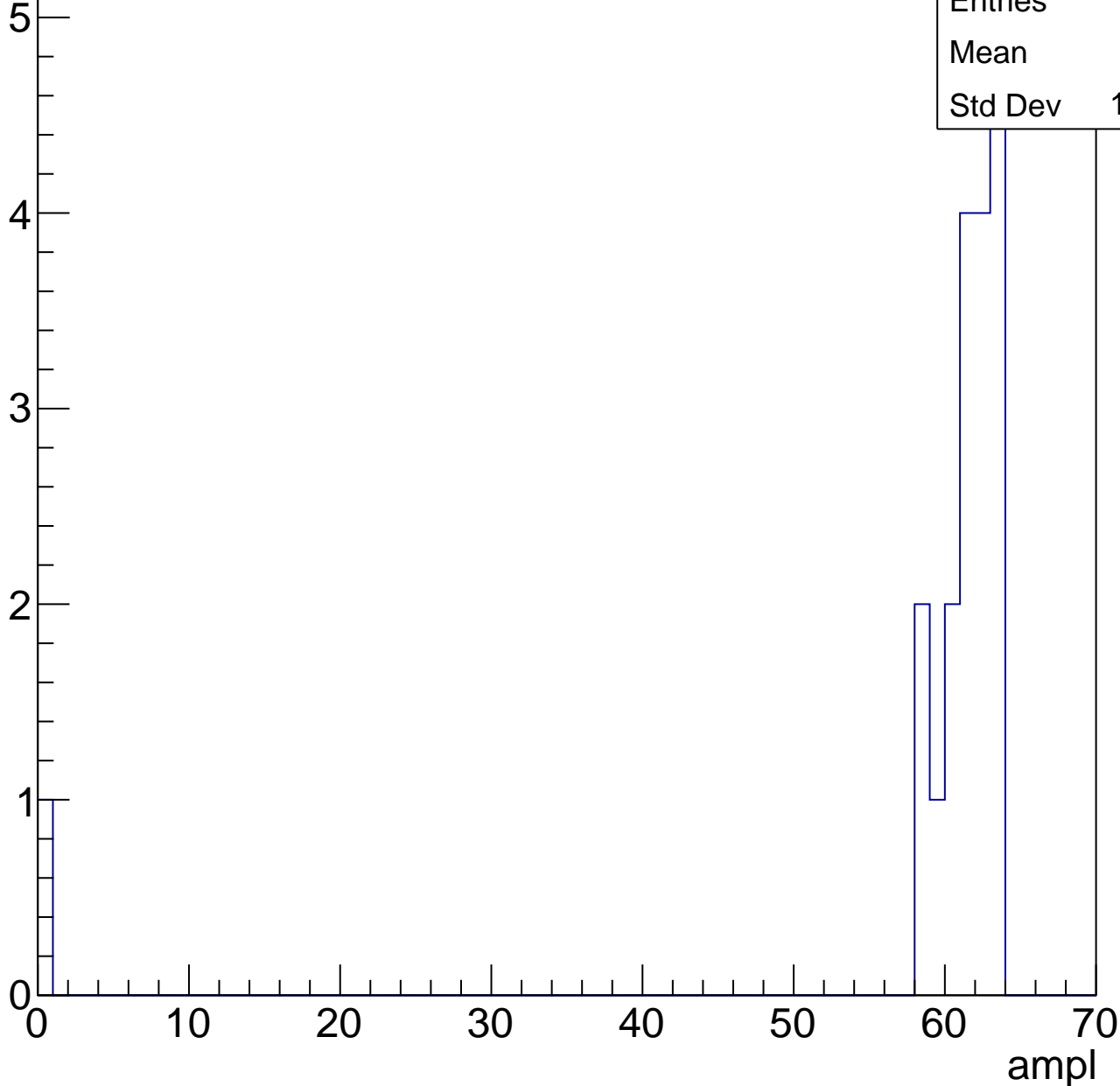


# B1L102S, U5-ch27, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	19
Mean	58
Std Dev	13.76





# B1L102S, U5-ch27, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U5-ch28, adc0

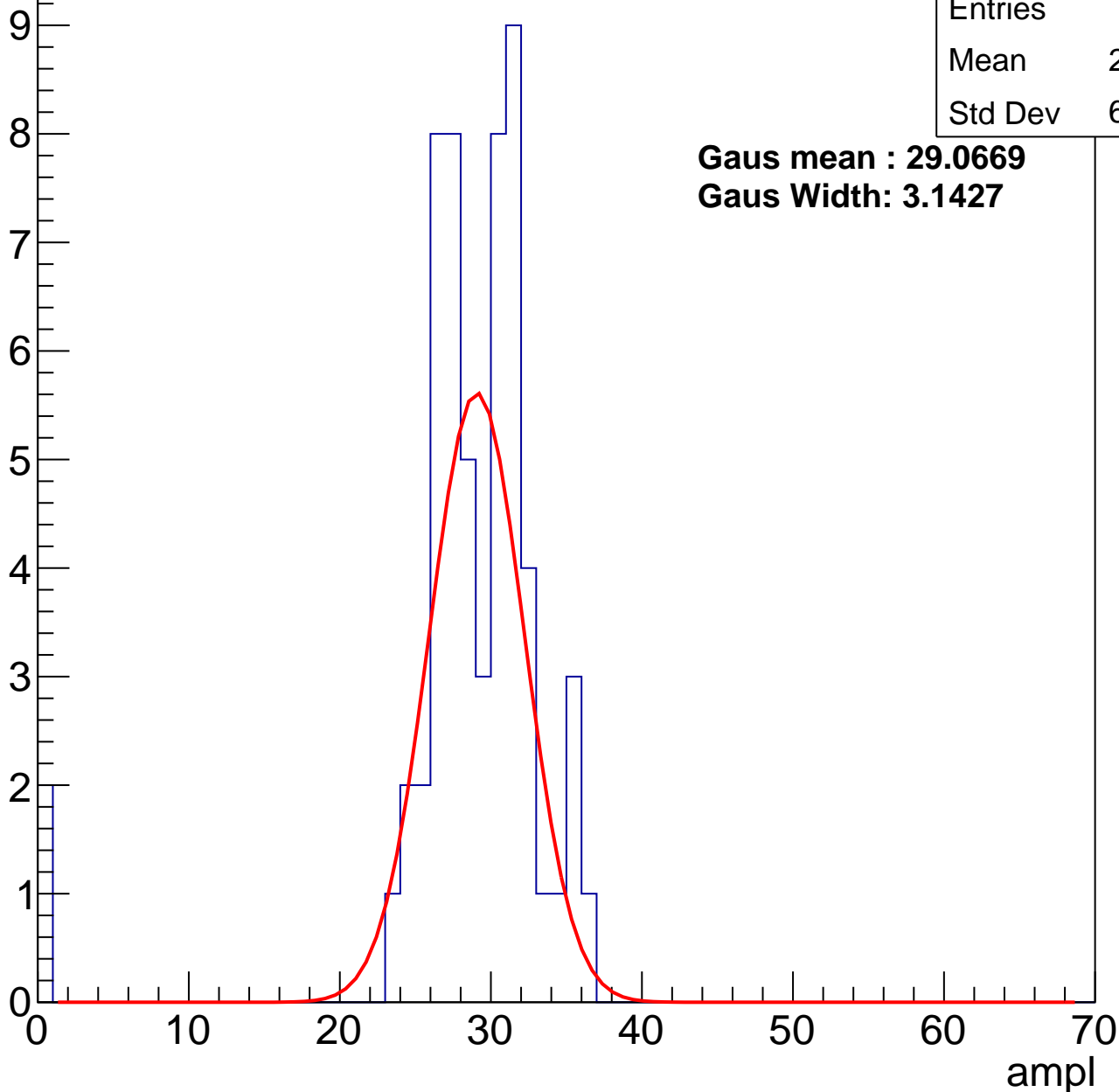
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	28.05
Std Dev	6.067

**Gaus mean : 29.0669**

**Gaus Width: 3.1427**



# B1L102S, U5-ch28, adc1

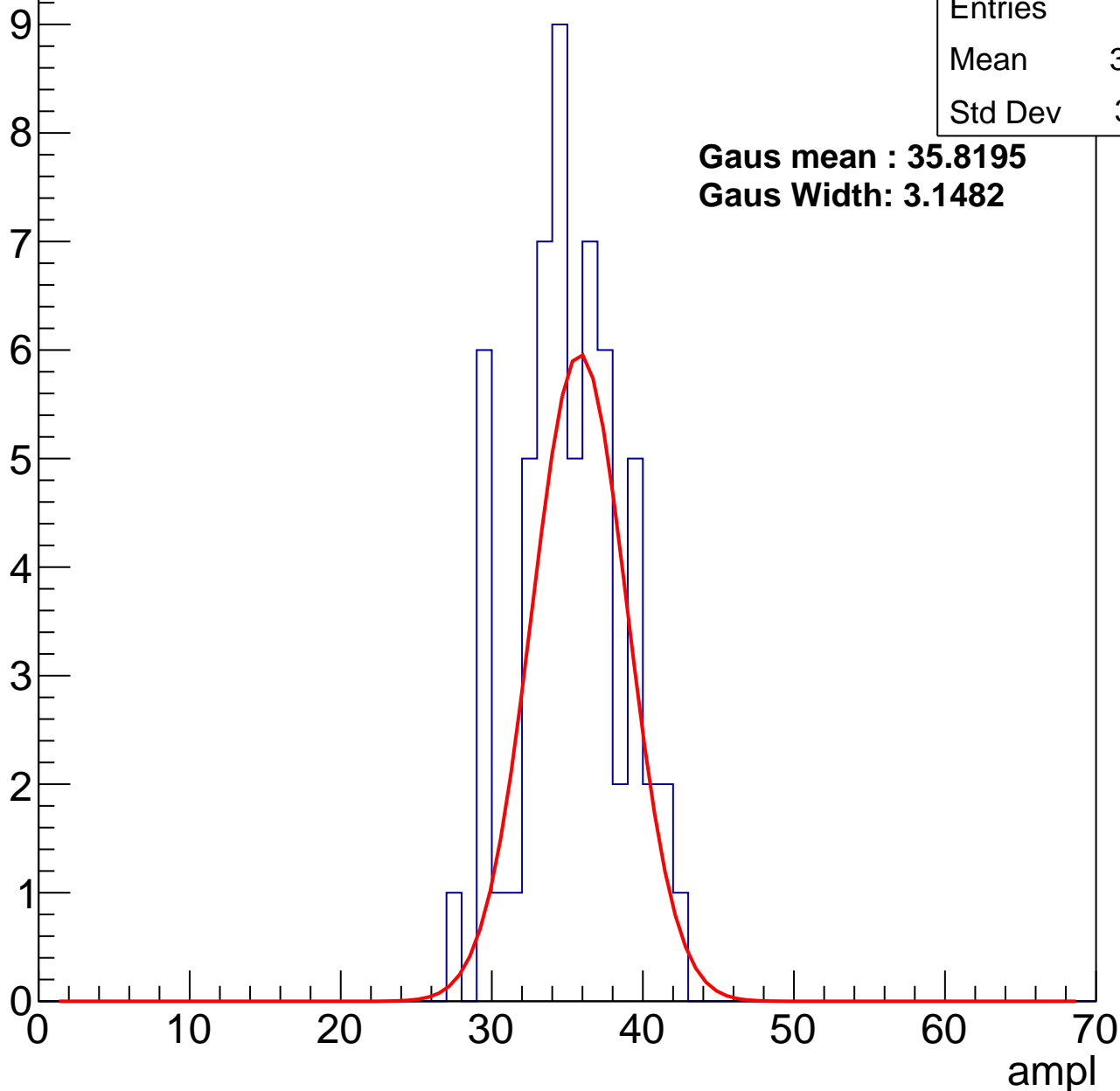
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	34.72
Std Dev	3.411

**Gaus mean : 35.8195**

**Gaus Width: 3.1482**



# B1L102S, U5-ch28, adc2

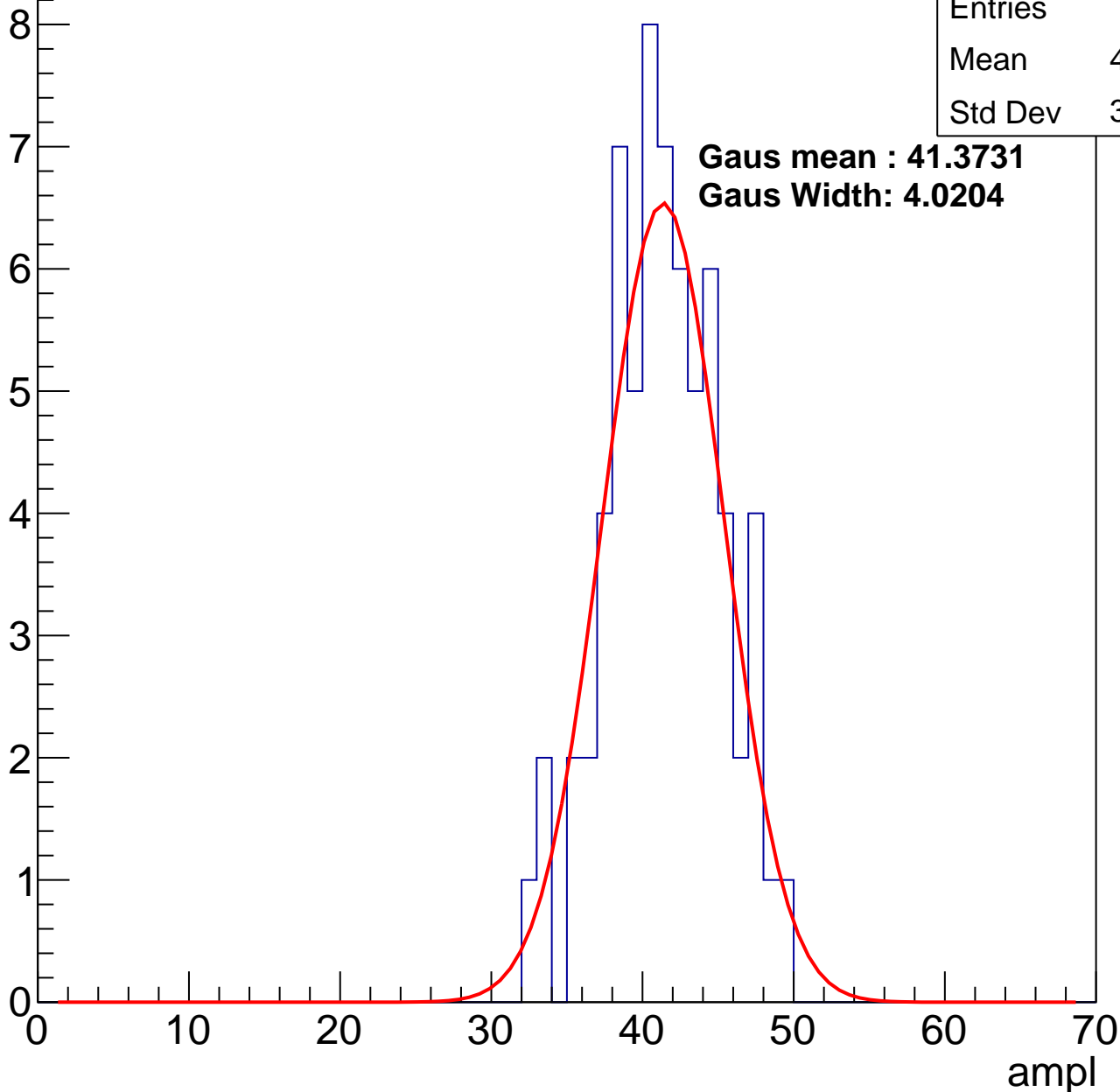
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	40.96
Std Dev	3.739

**Gaus mean : 41.3731**

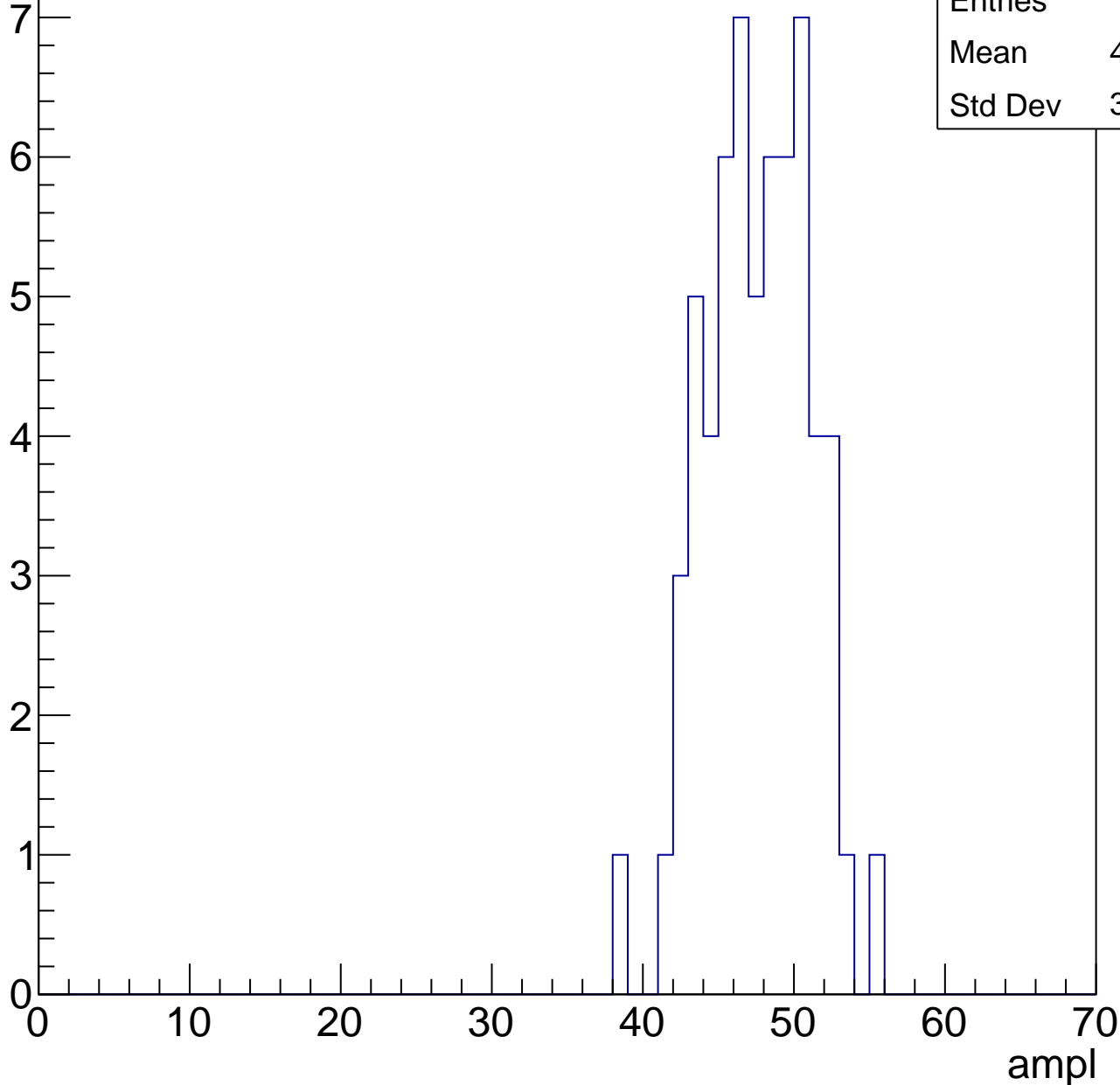
**Gaus Width: 4.0204**



# B1L102S, U5-ch28, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

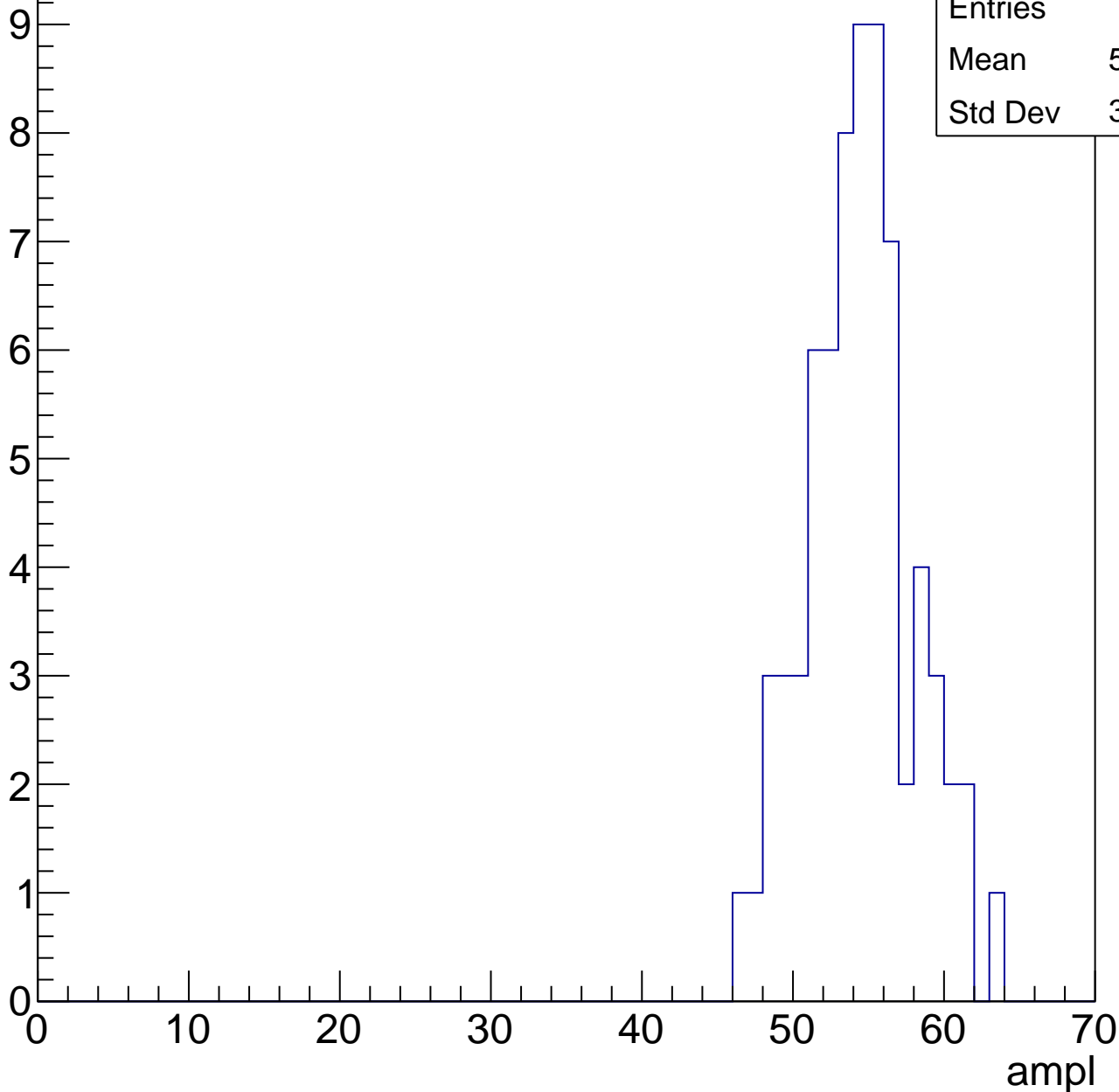


# B1L102S, U5-ch28, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	53.96
Std Dev	3.535

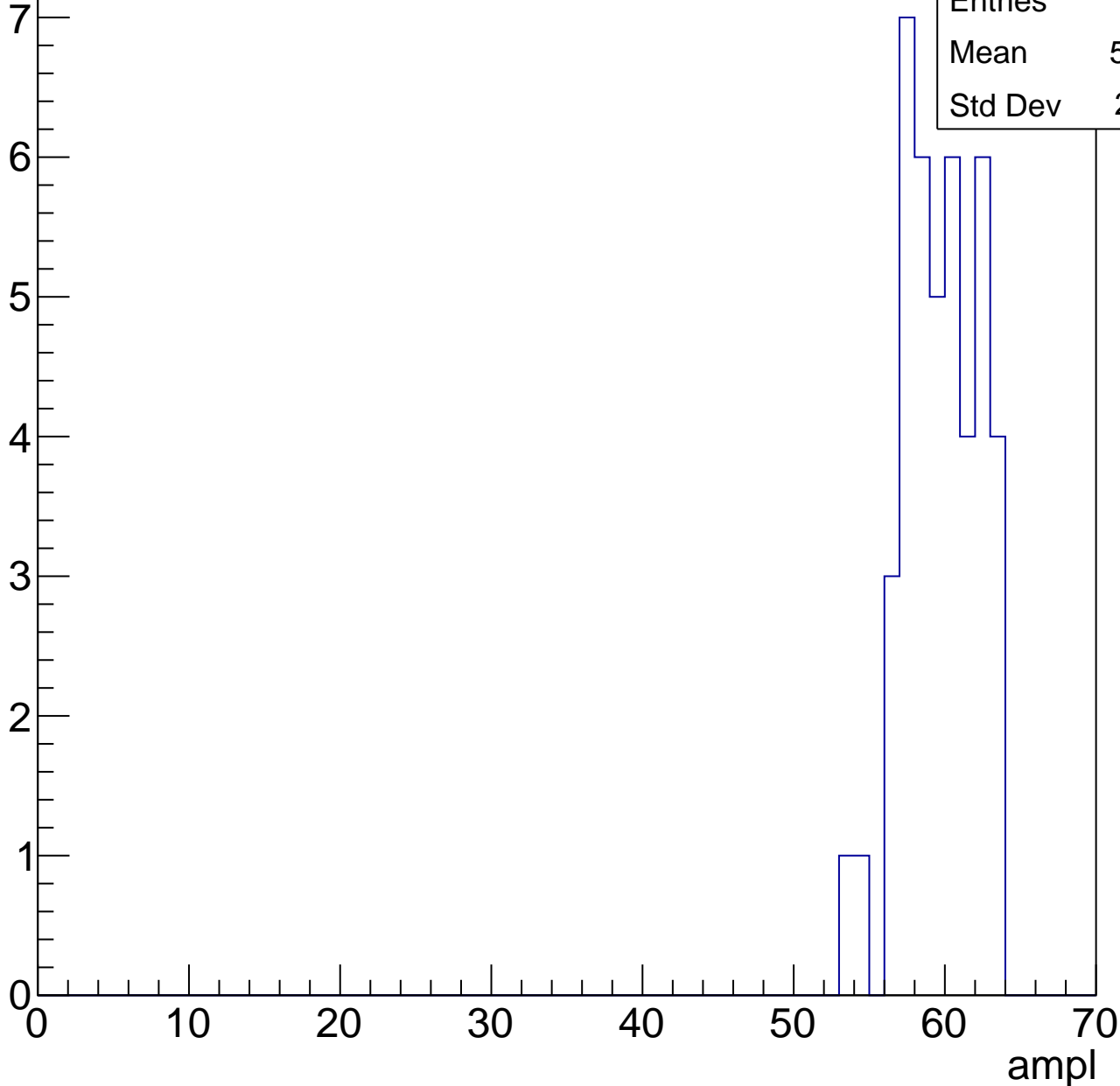


# B1L102S, U5-ch28, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	43
Mean	59.19
Std Dev	2.461

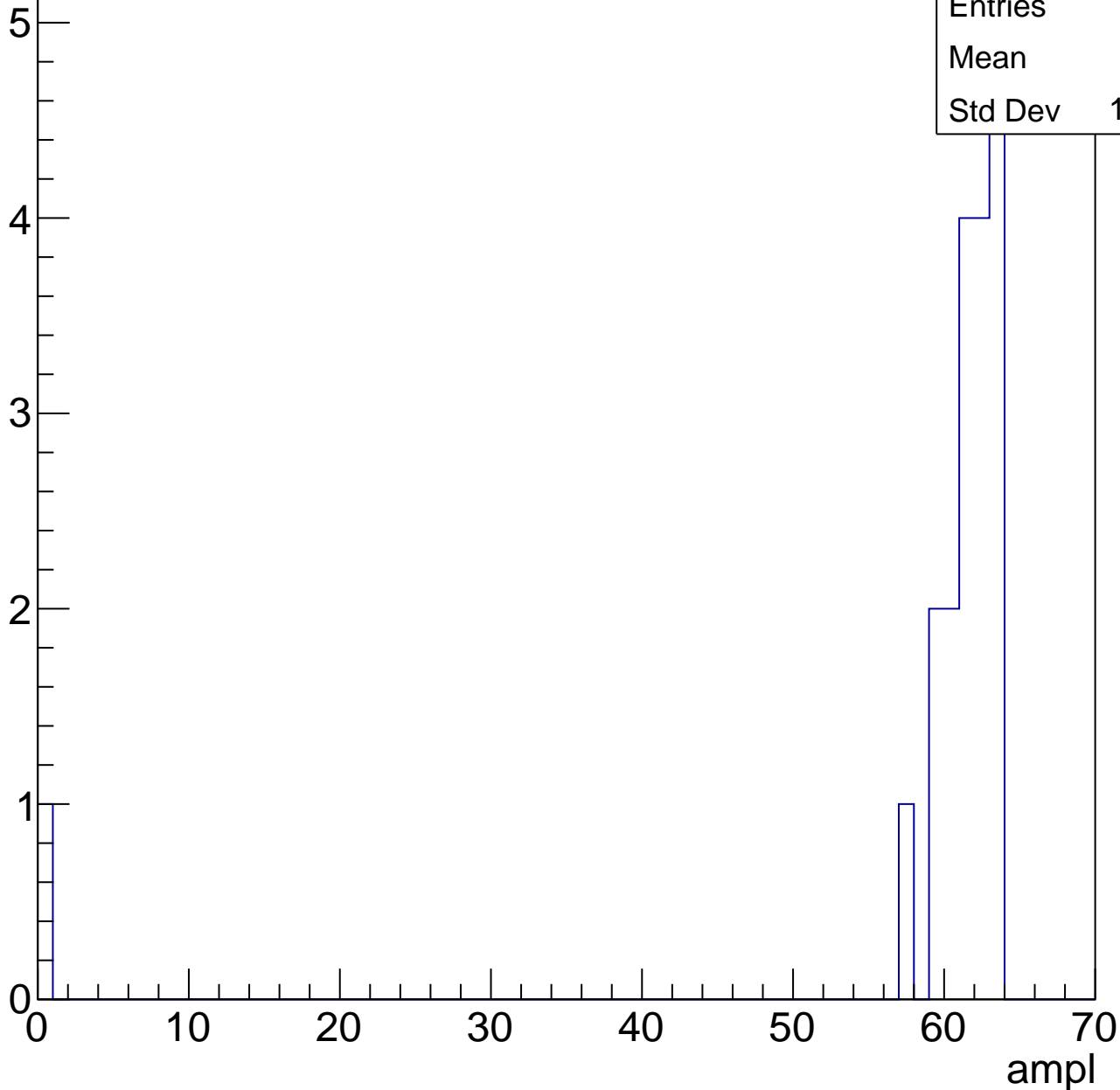


# B1L102S, U5-ch28, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	19
Mean	58
Std Dev	13.76





# B1L102S, U5-ch28, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U5-ch29, adc0

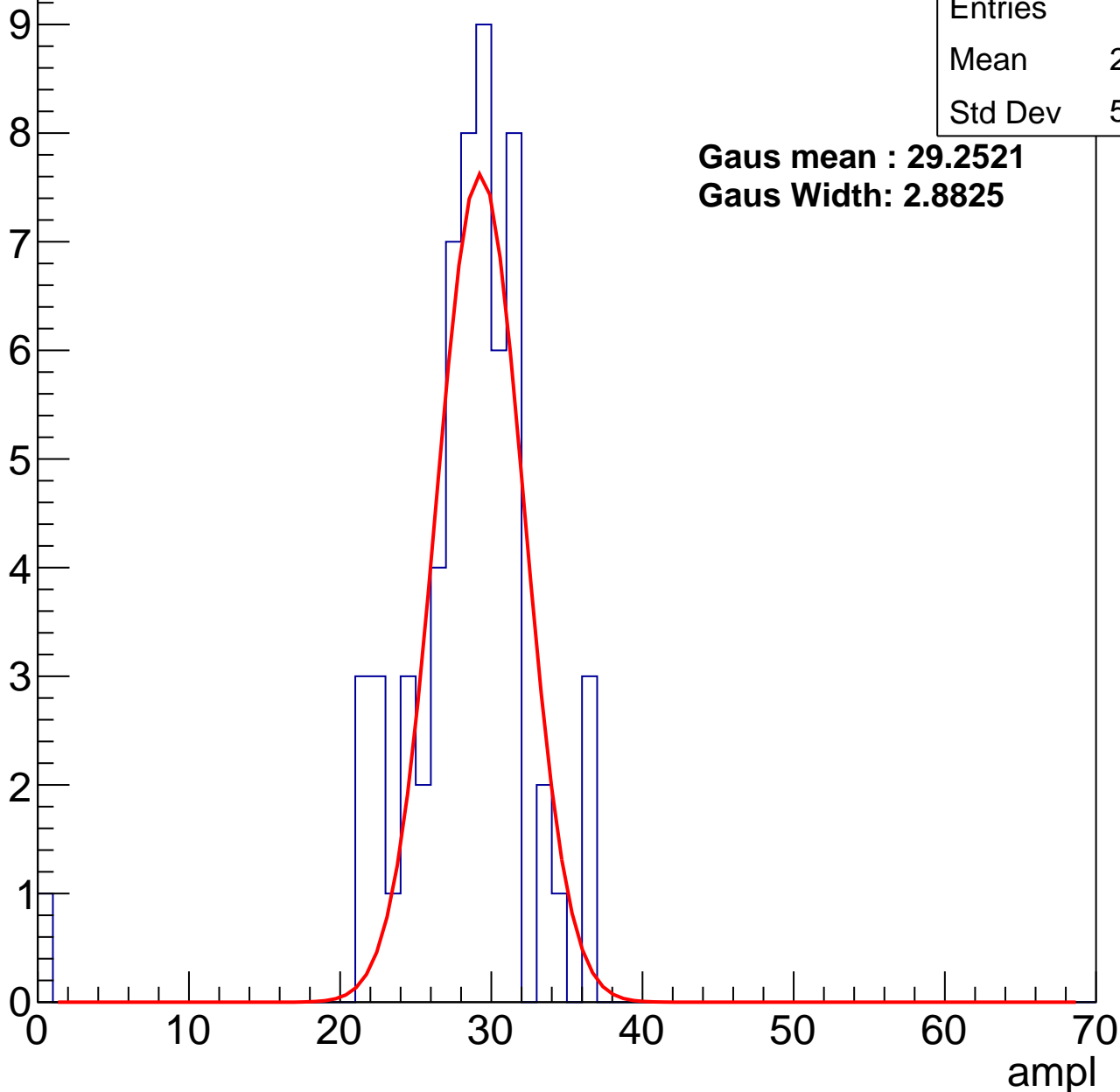
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	27.67
Std Dev	5.007

**Gaus mean : 29.2521**

**Gaus Width: 2.8825**



# B1L102S, U5-ch29, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	73
Mean	34.81
Std Dev	3.77

**Gaus mean : 35.6690**

**Gaus Width: 3.2484**

Entry

10  
8  
6  
4  
2  
0

ampl

0

10

20

30

40

50

60

70

# B1L102S, U5-ch29, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	75
Mean	42.31
Std Dev	3.29

**Gaus mean : 42.9202**

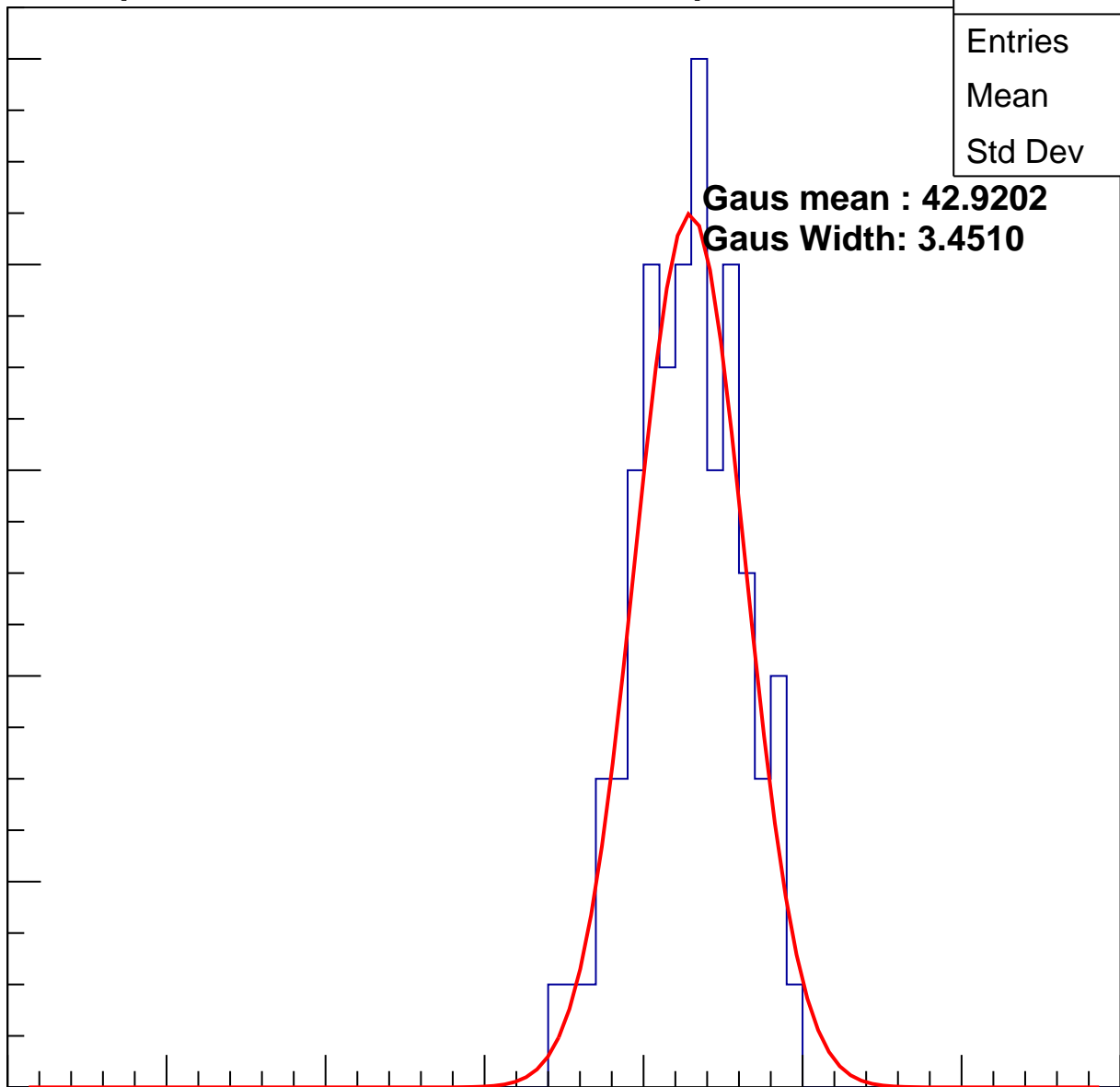
**Gaus Width: 3.4510**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

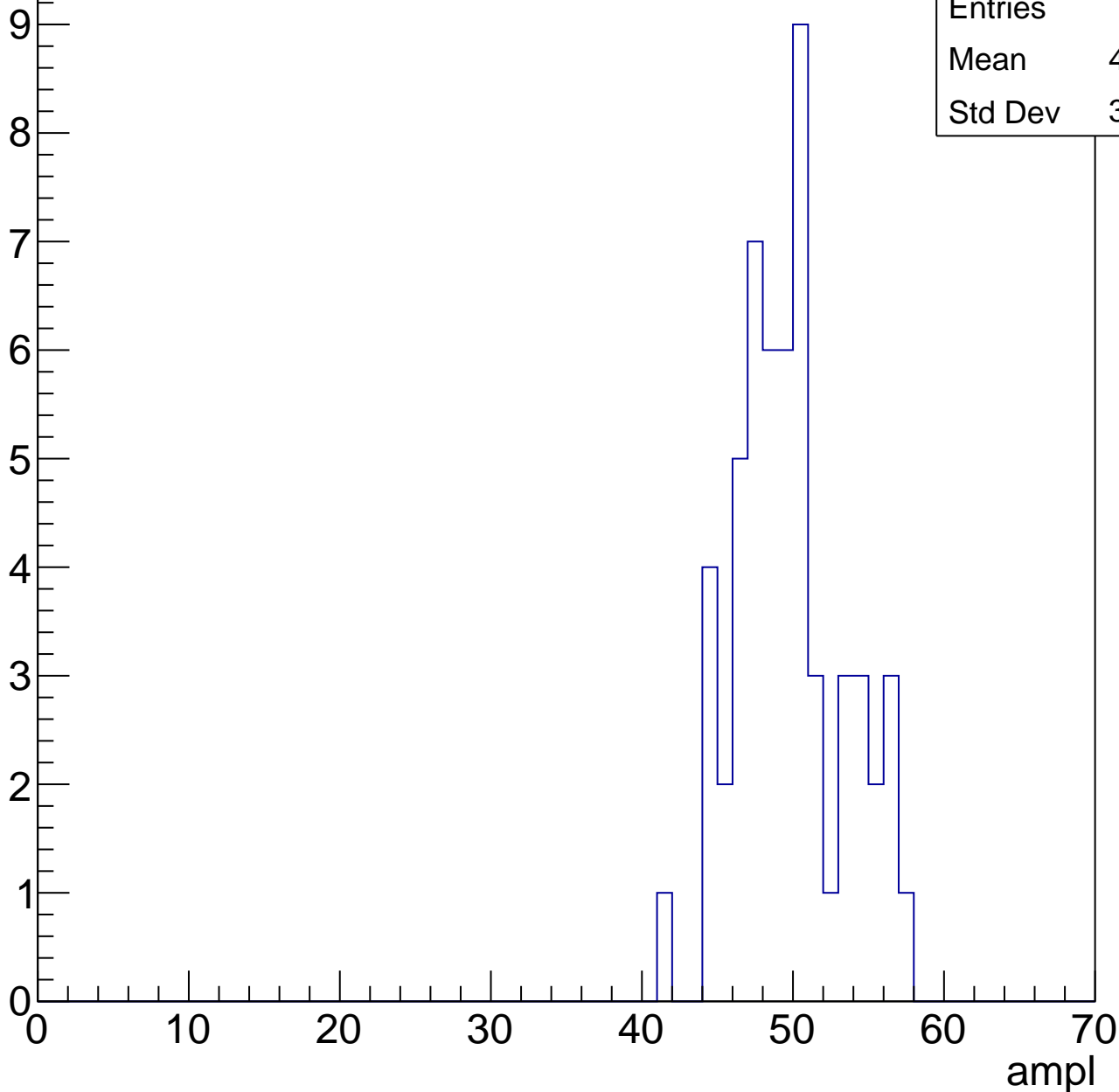


# B1L102S, U5-ch29, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	49.27
Std Dev	3.553

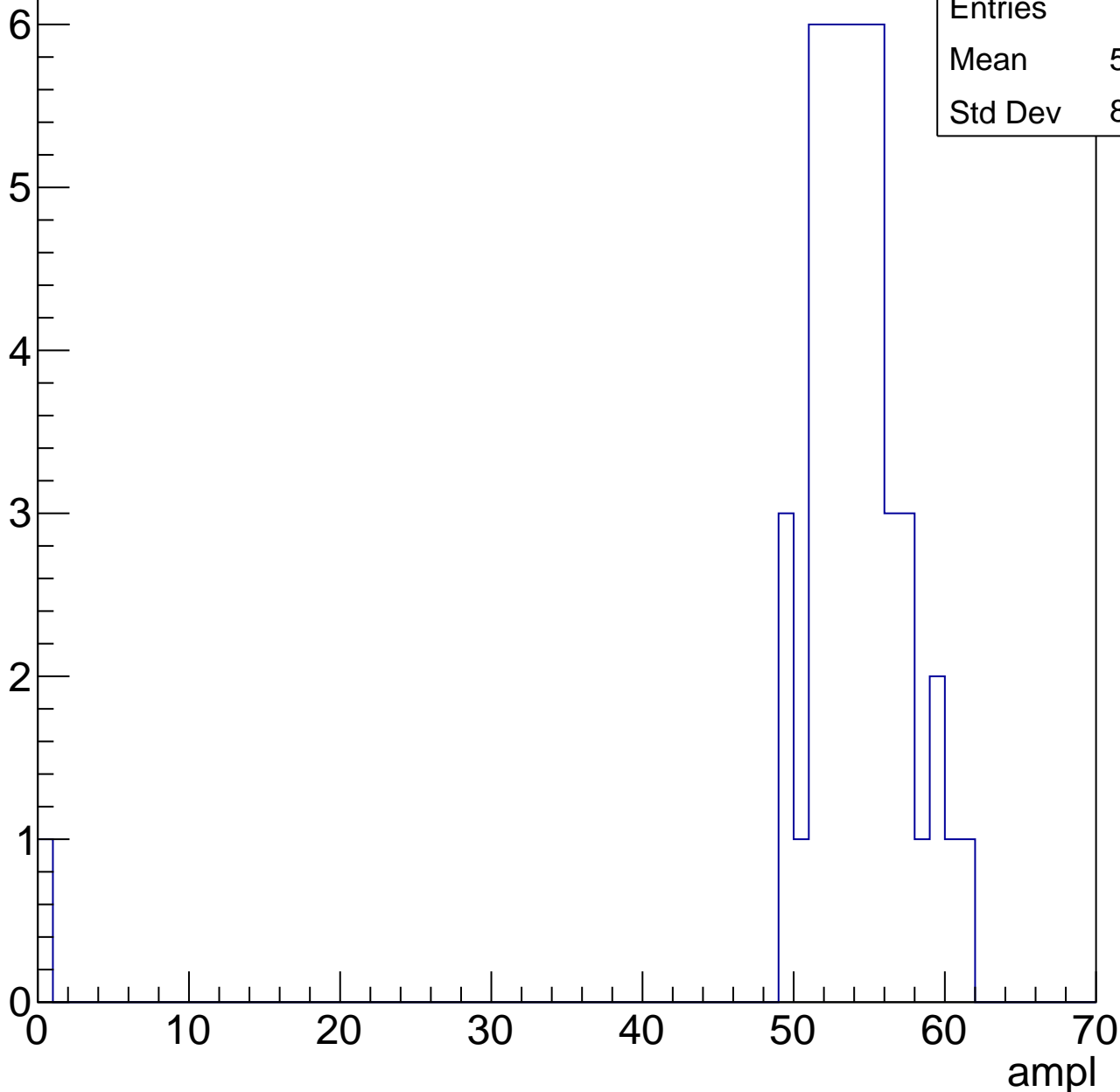


# B1L102S, U5-ch29, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

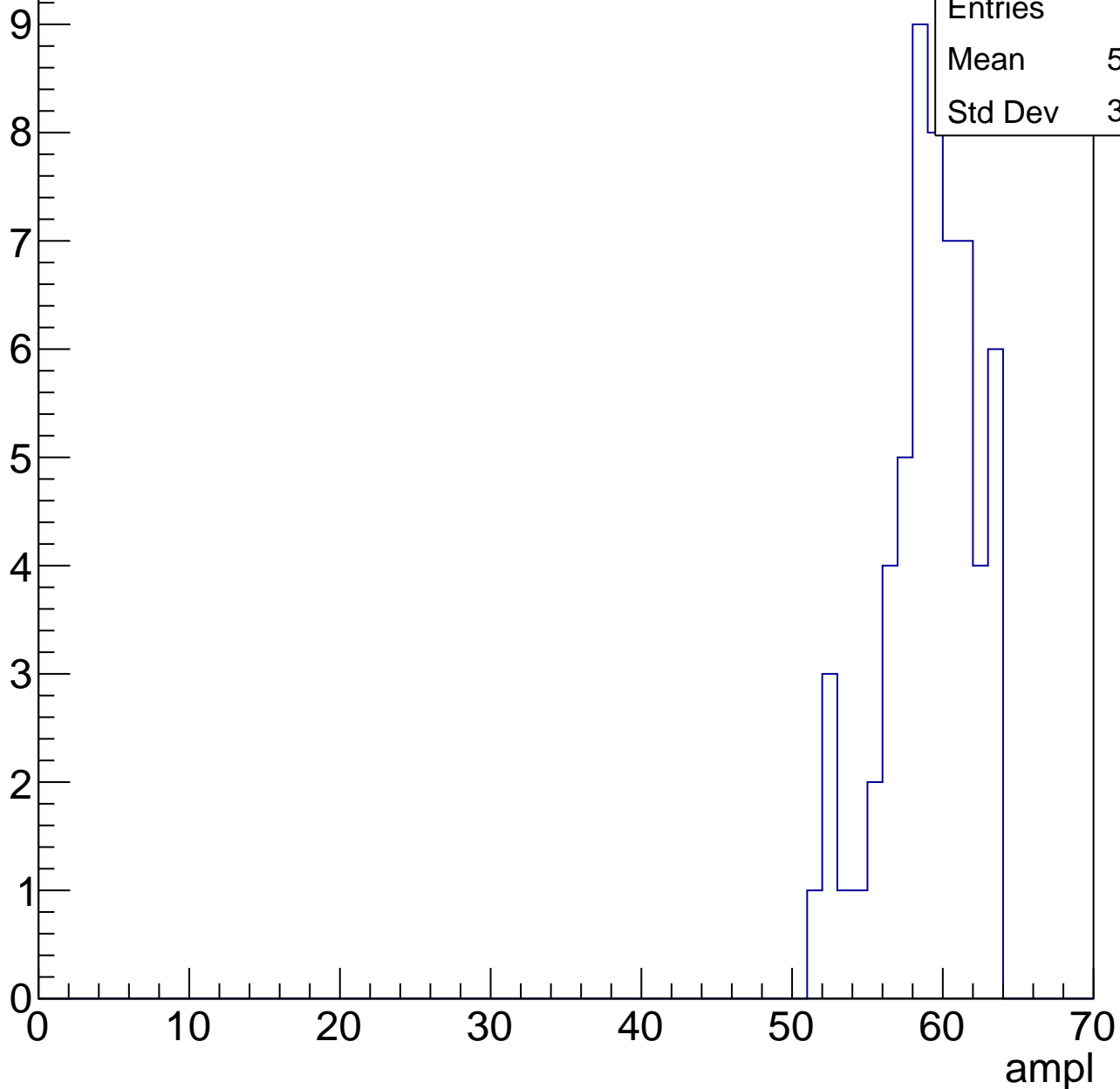
Entries	46
Mean	52.67
Std Dev	8.349



# B1L102S, U5-ch29, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



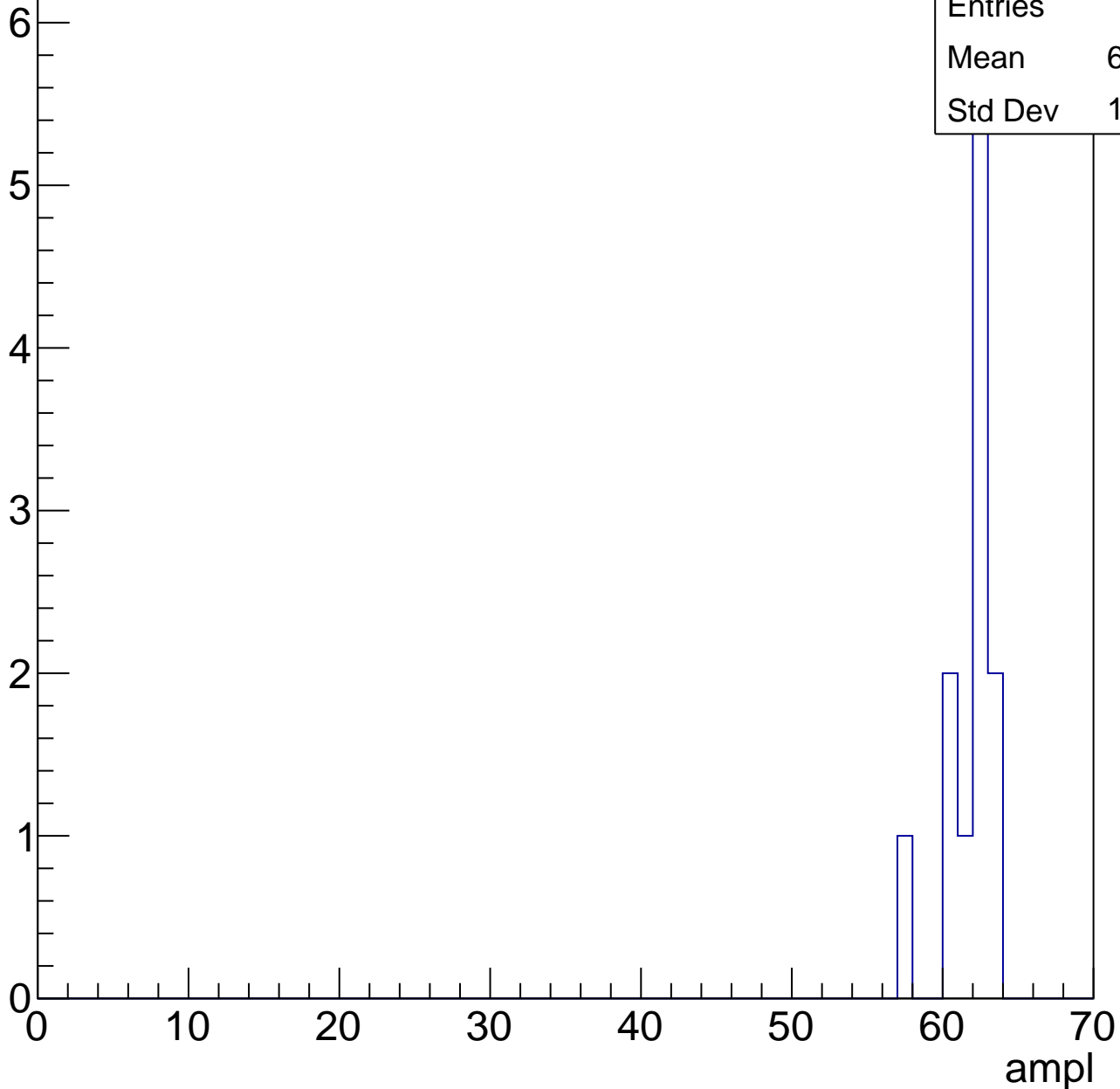
Entries	58
Mean	58.62
Std Dev	3.016

# B1L102S, U5-ch29, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	12
Mean	61.33
Std Dev	1.599





# B1L102S, U5-ch29, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U5-ch30, adc0

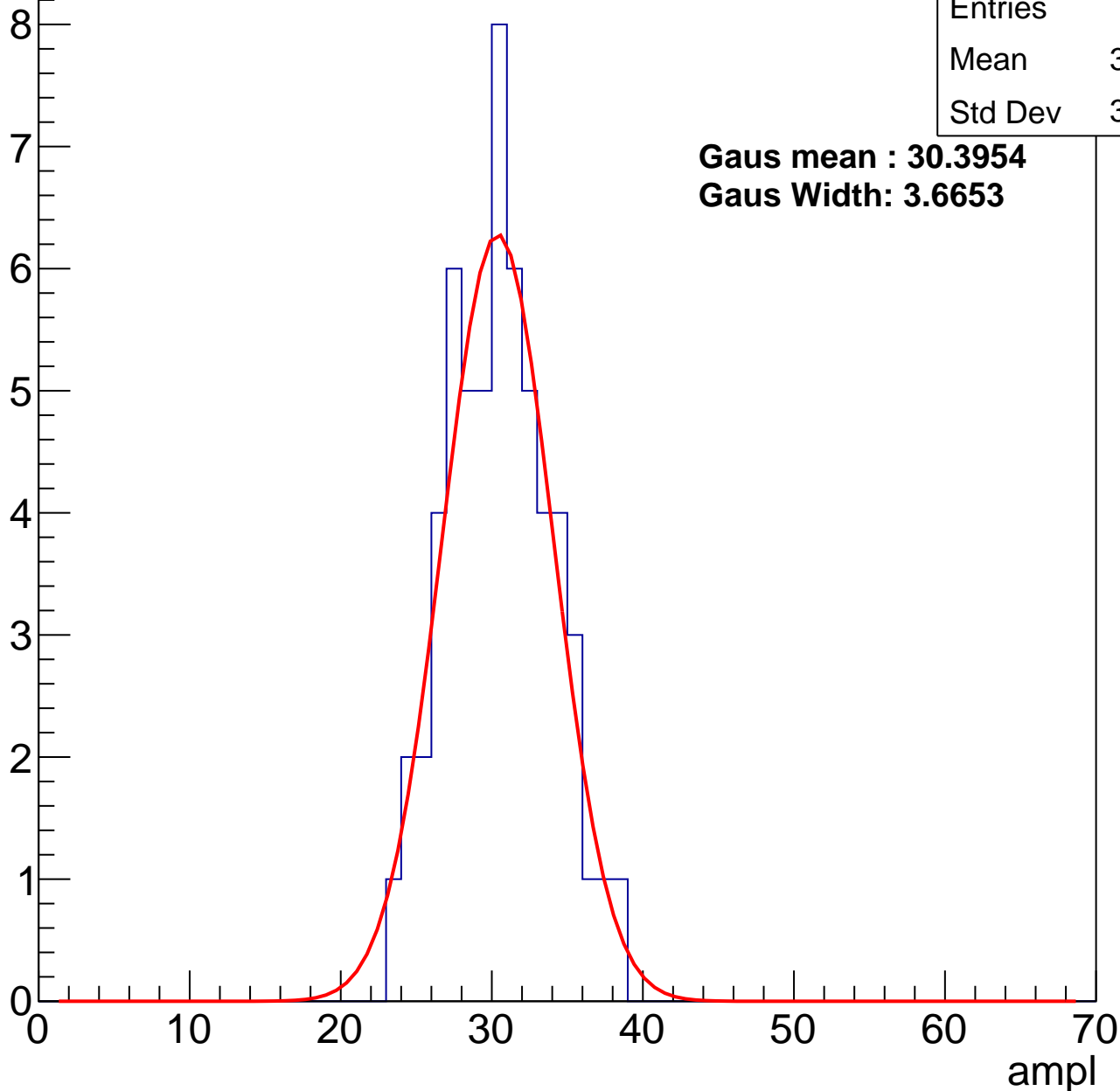
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	30.03
Std Dev	3.383

**Gaus mean : 30.3954**

**Gaus Width: 3.6653**



# B1L102S, U5-ch30, adc1

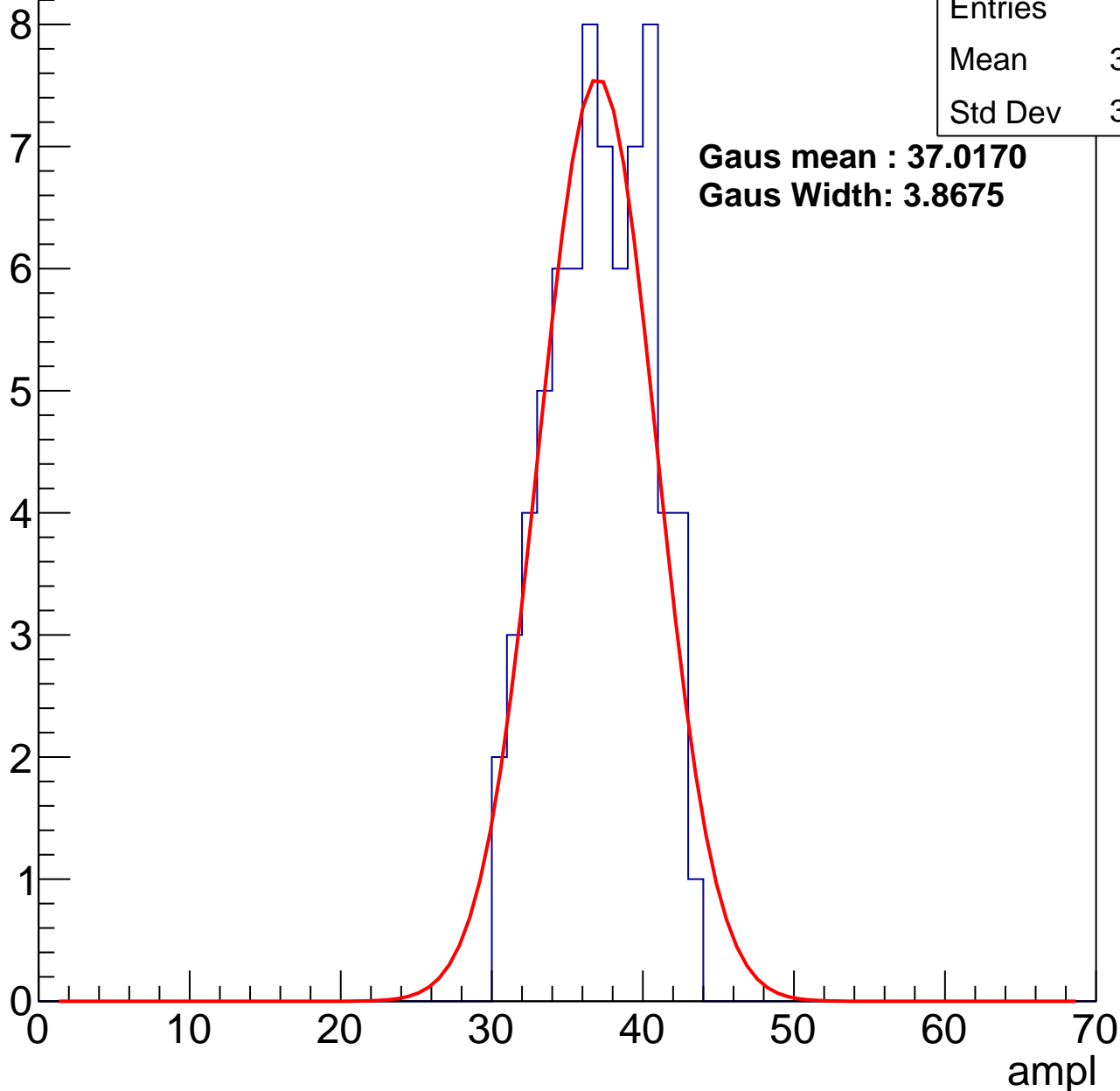
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	36.66
Std Dev	3.293

**Gaus mean : 37.0170**

**Gaus Width: 3.8675**



# B1L102S, U5-ch30, adc2

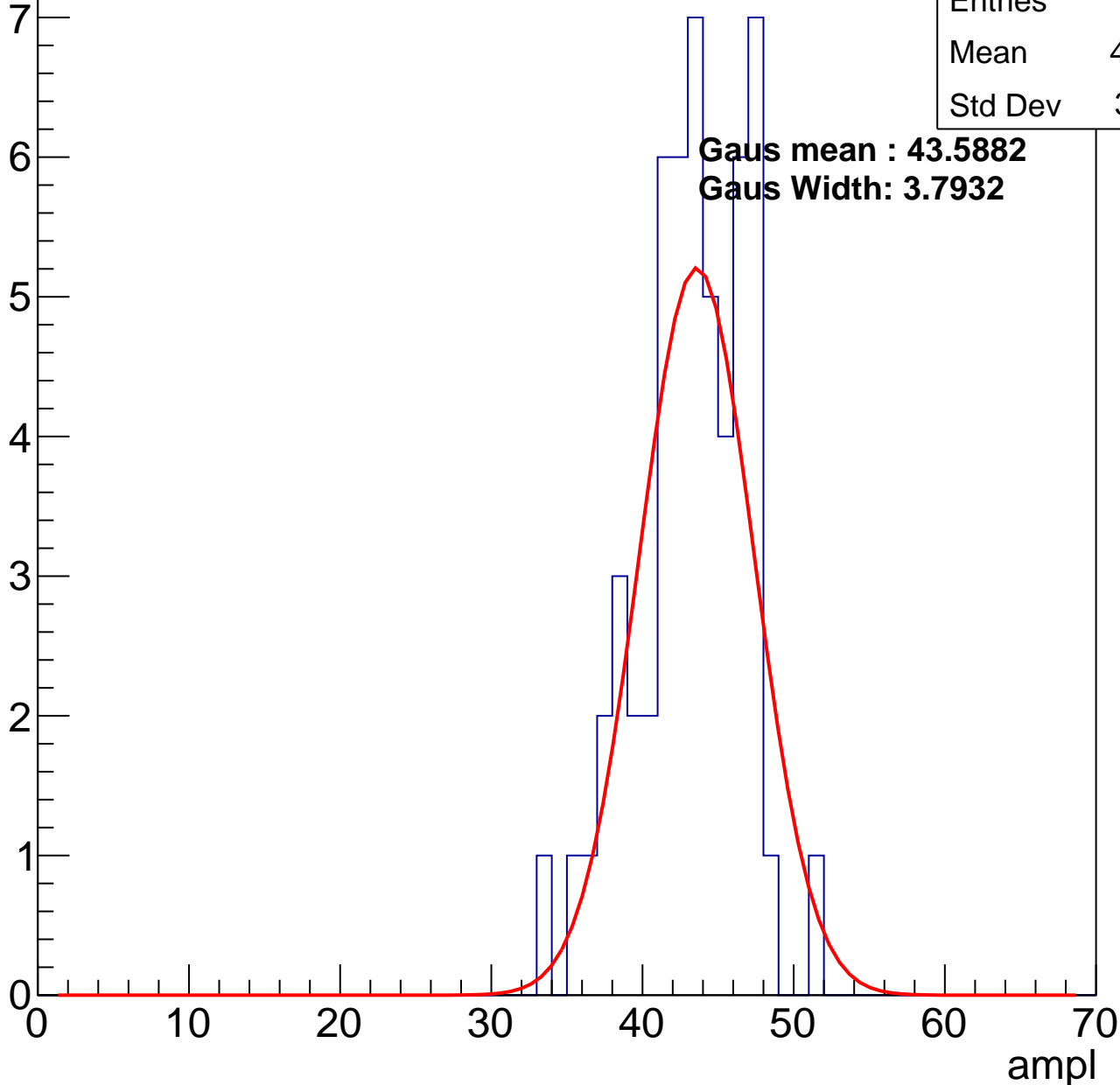
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	42.78
Std Dev	3.601

**Gaus mean : 43.5882**

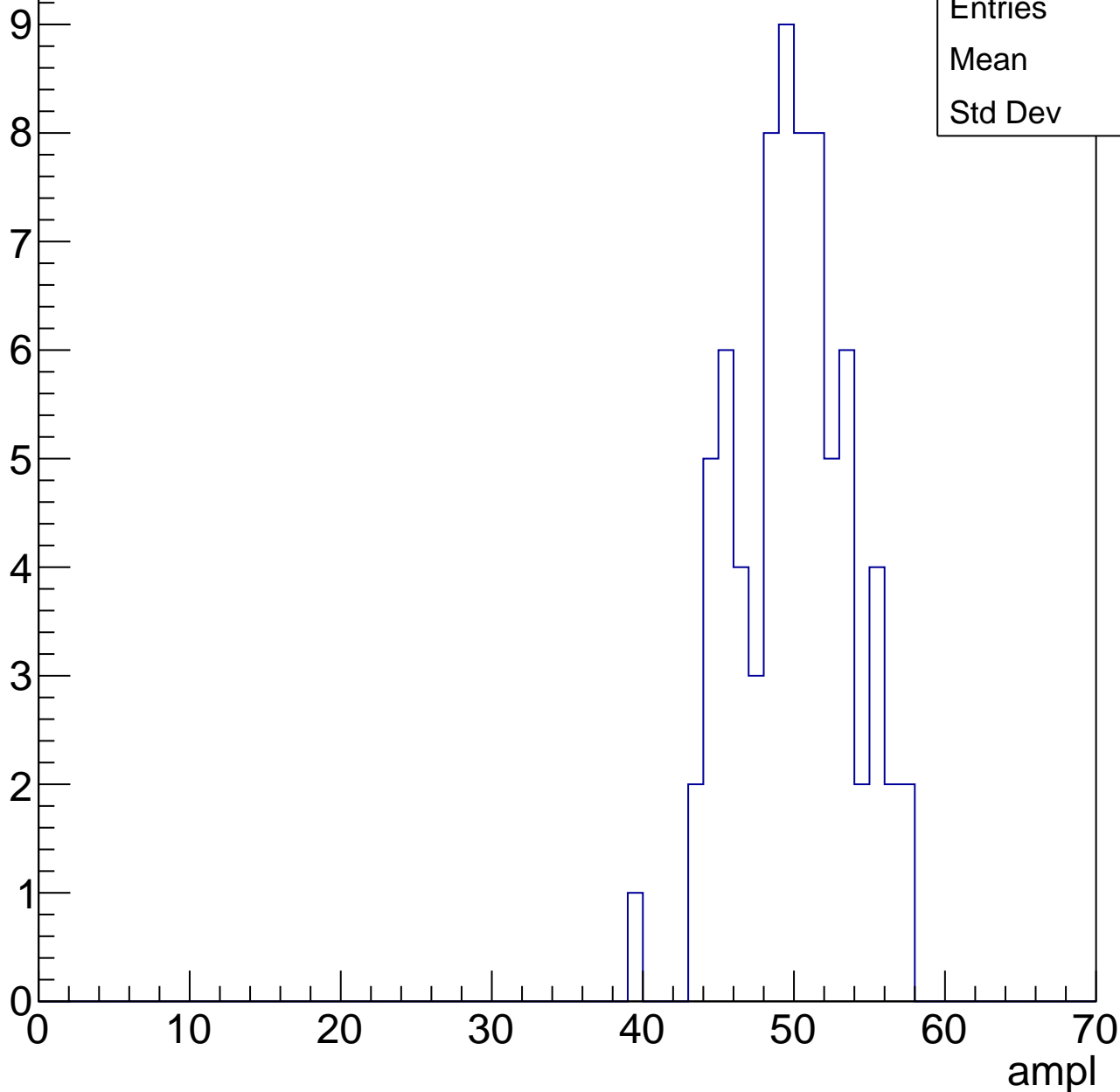
**Gaus Width: 3.7932**



# B1L102S, U5-ch30, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

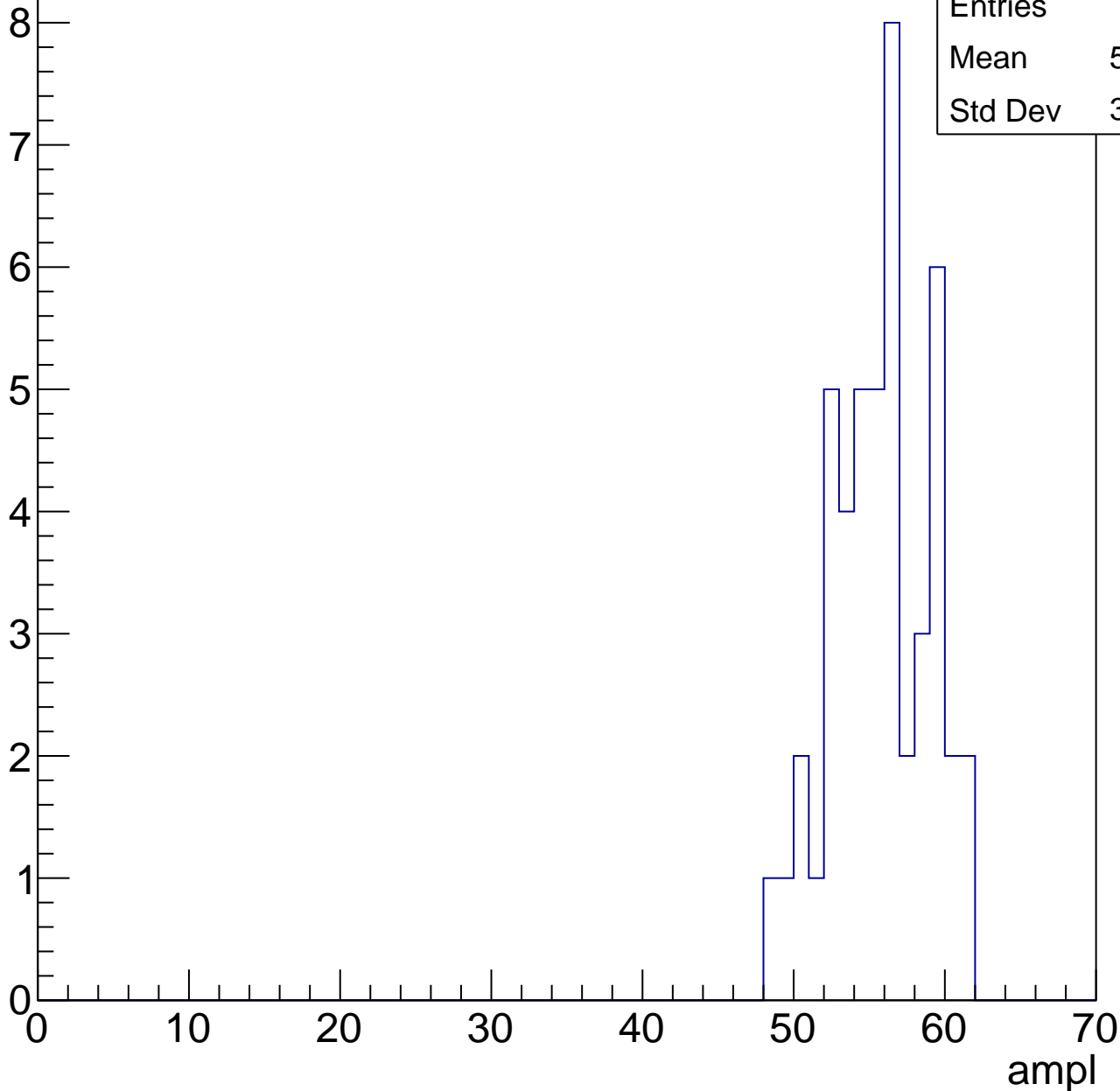


# B1L102S, U5-ch30, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	47
Mean	55.26
Std Dev	3.179

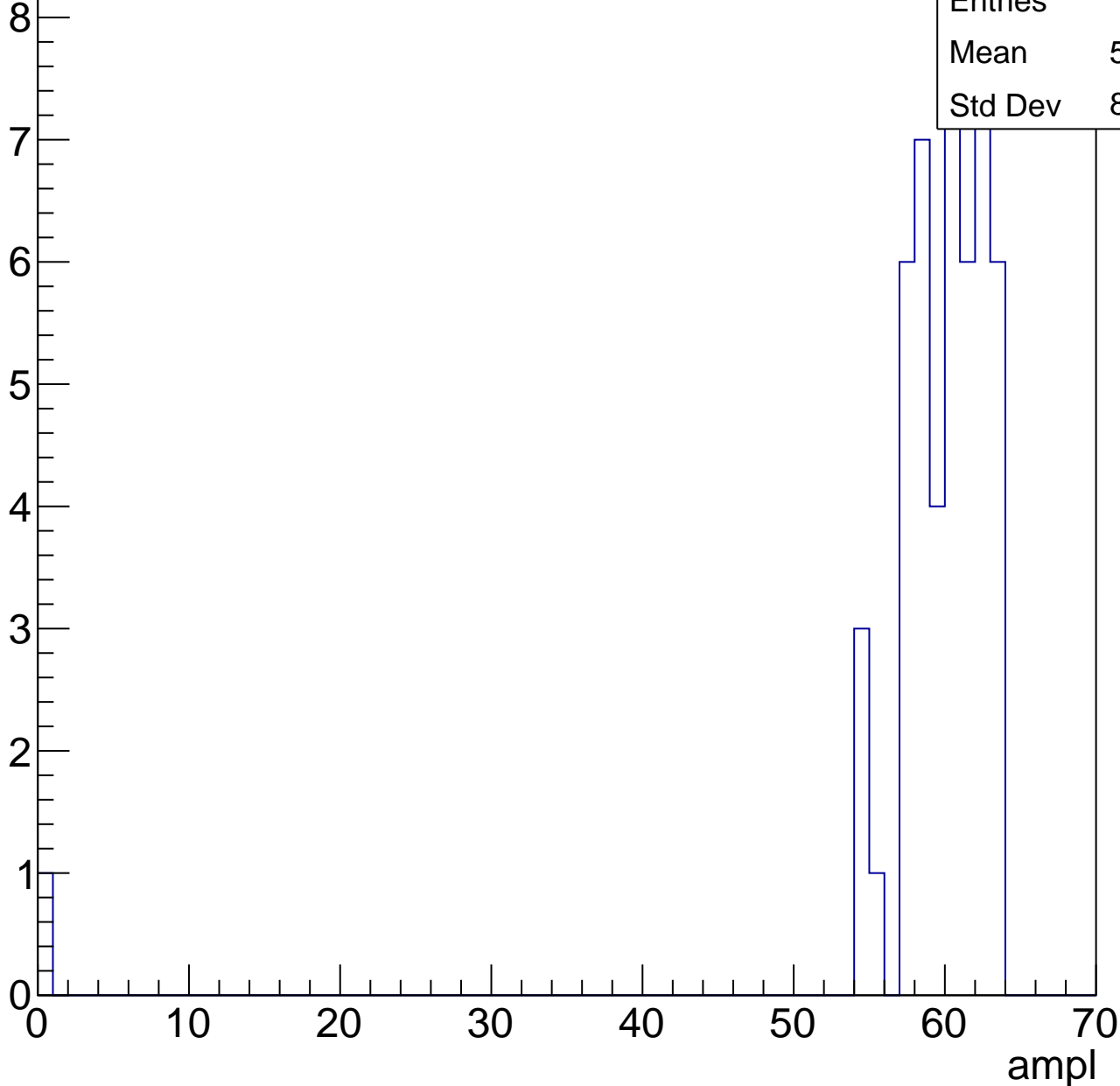


# B1L102S, U5-ch30, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

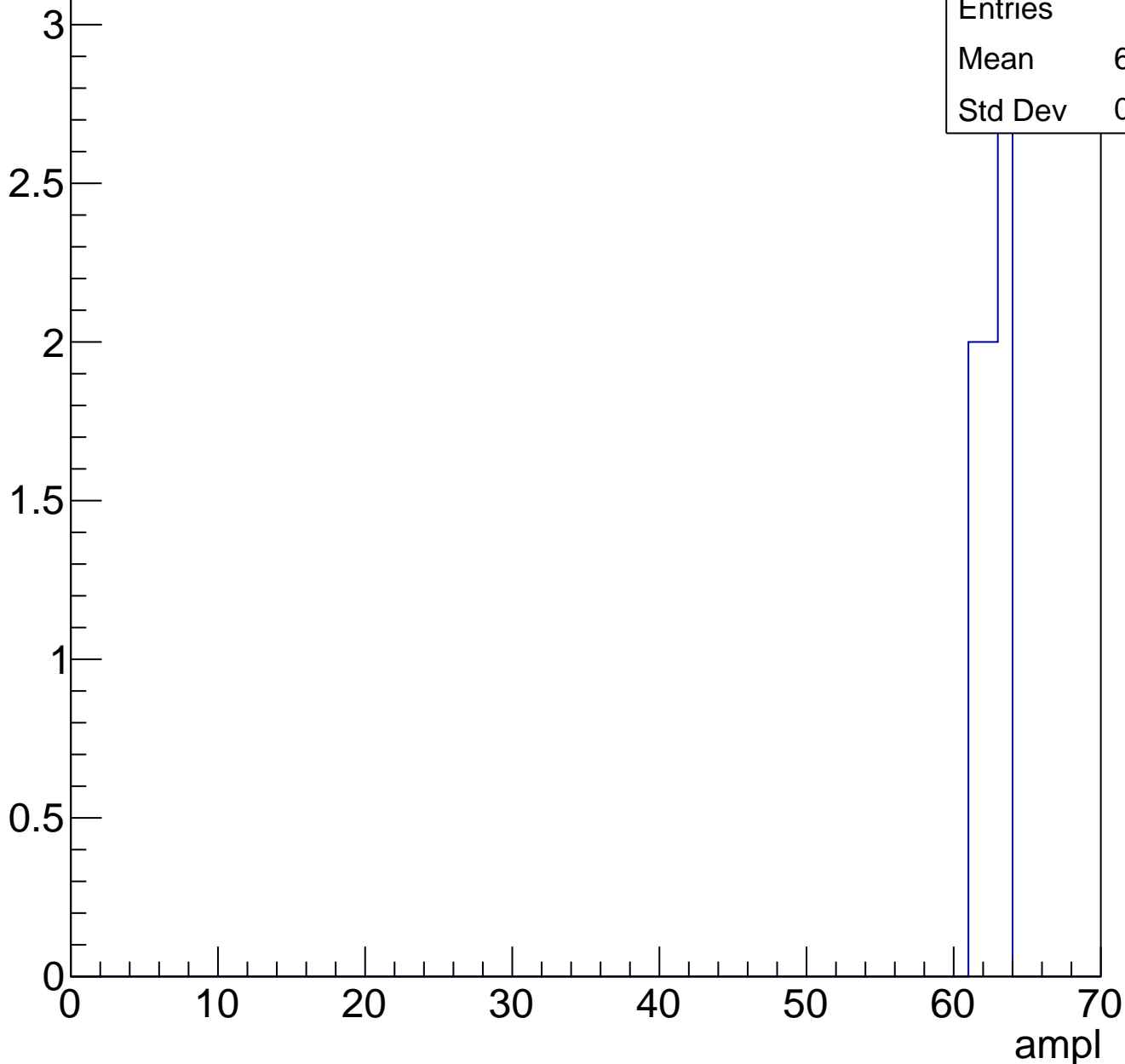
Entries	50
Mean	58.42
Std Dev	8.702



# B1L102S, U5-ch30, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

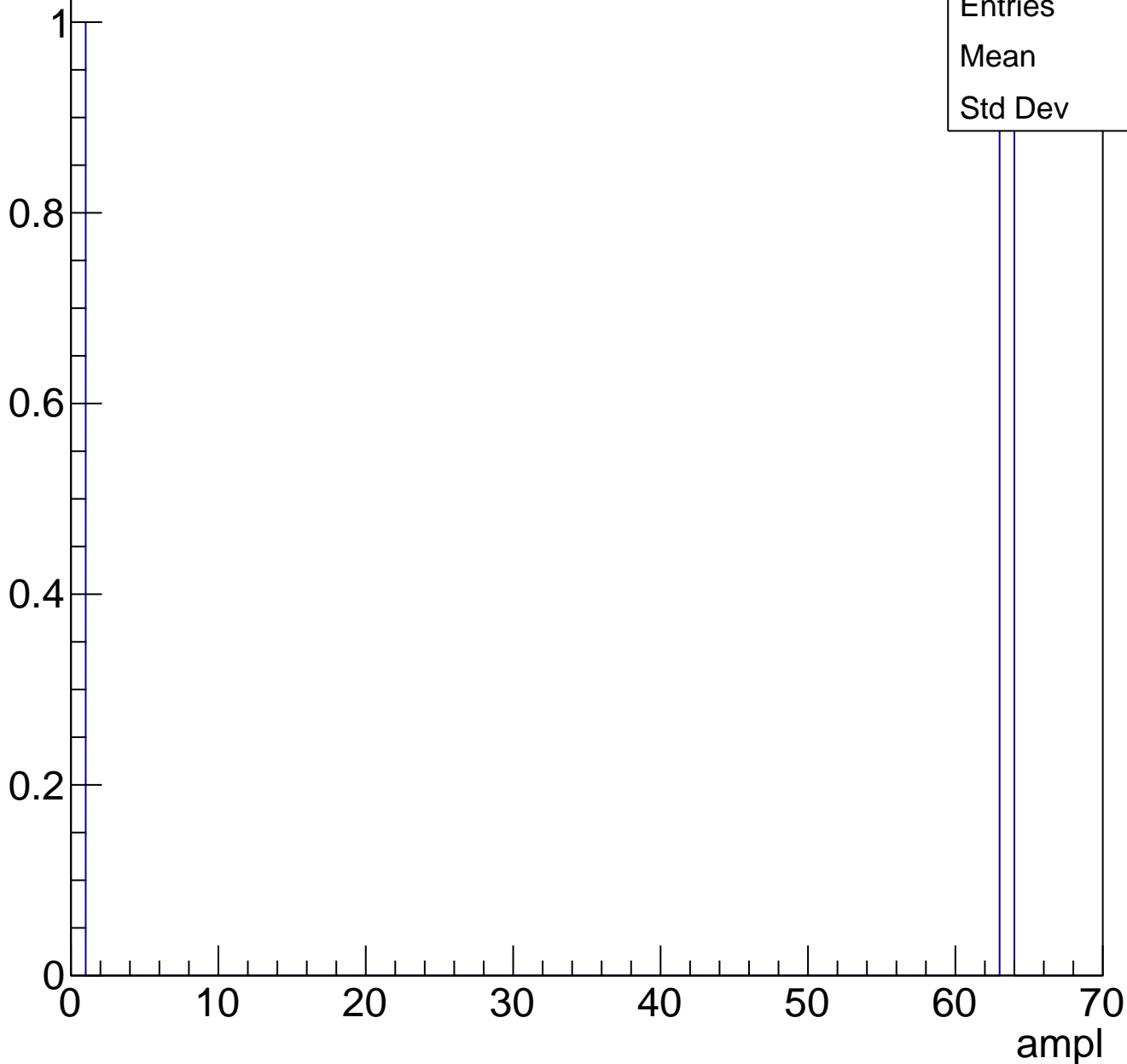




# B1L102S, U5-ch30, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U5-ch31, adc0

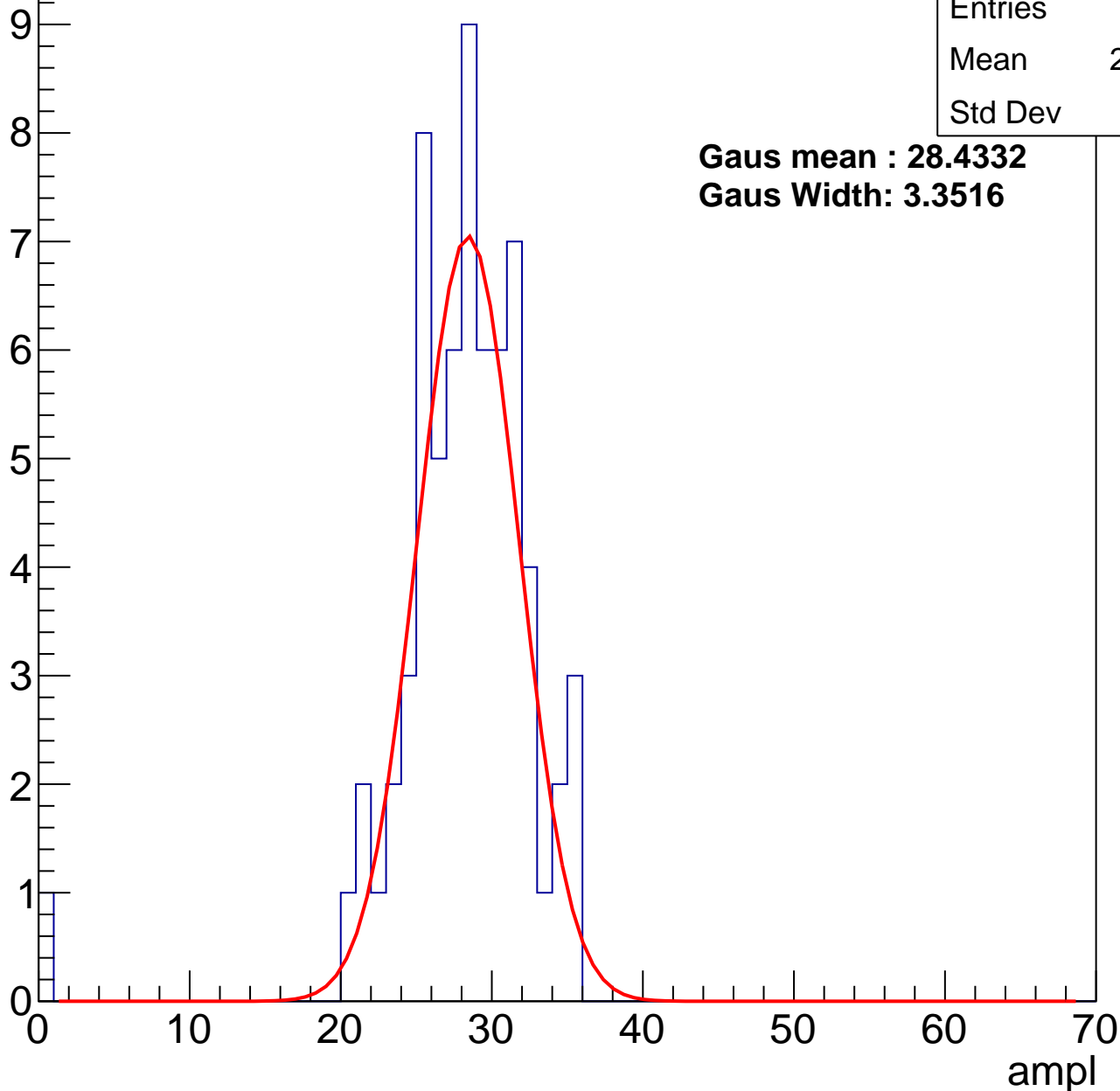
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	27.63
Std Dev	4.84

**Gaus mean : 28.4332**

**Gaus Width: 3.3516**



# B1L102S, U5-ch31, adc1

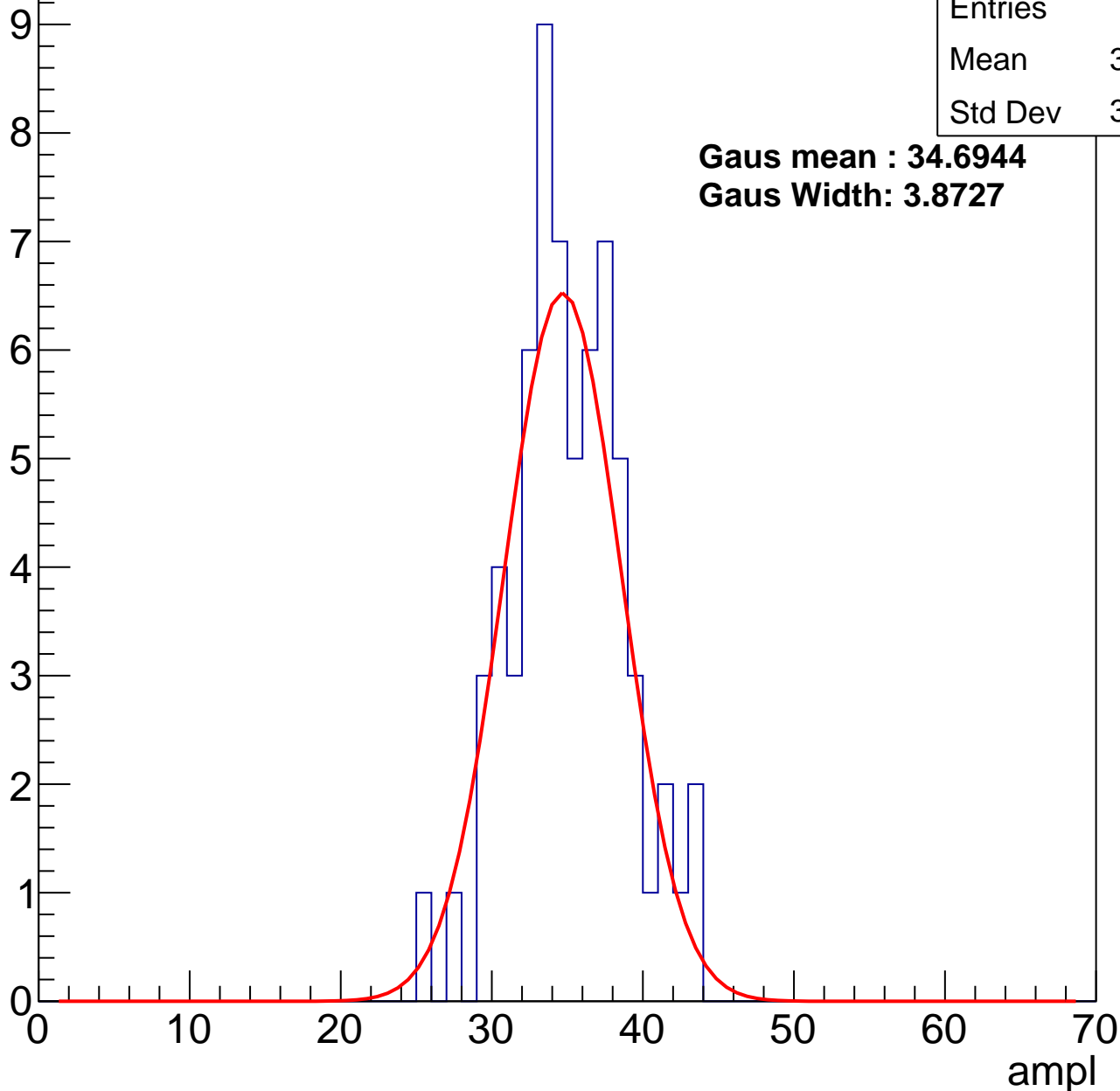
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	34.64
Std Dev	3.712

**Gaus mean : 34.6944**

**Gaus Width: 3.8727**



# B1L102S, U5-ch31, adc2

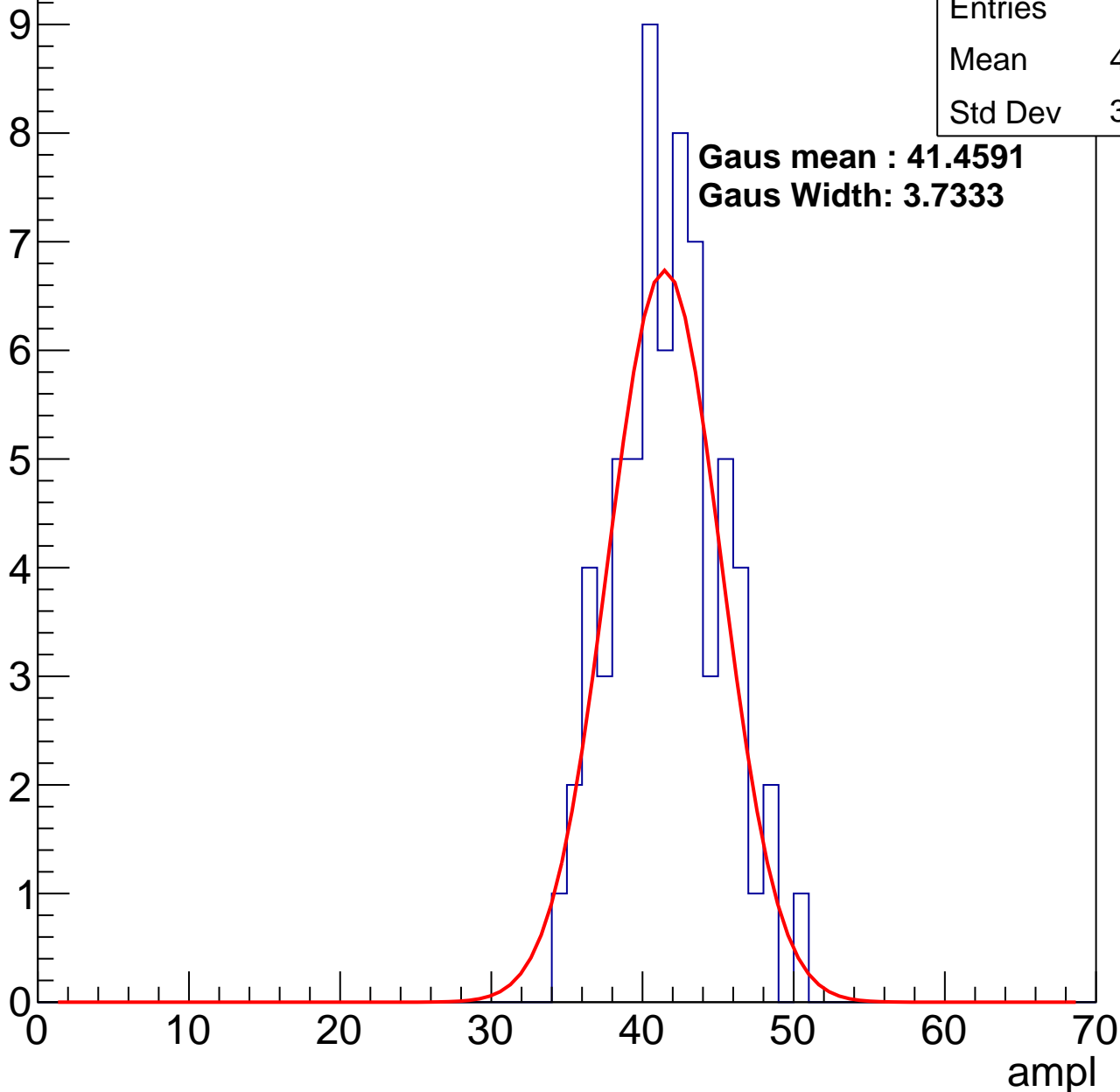
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	41.23
Std Dev	3.476

**Gaus mean : 41.4591**

**Gaus Width: 3.7333**

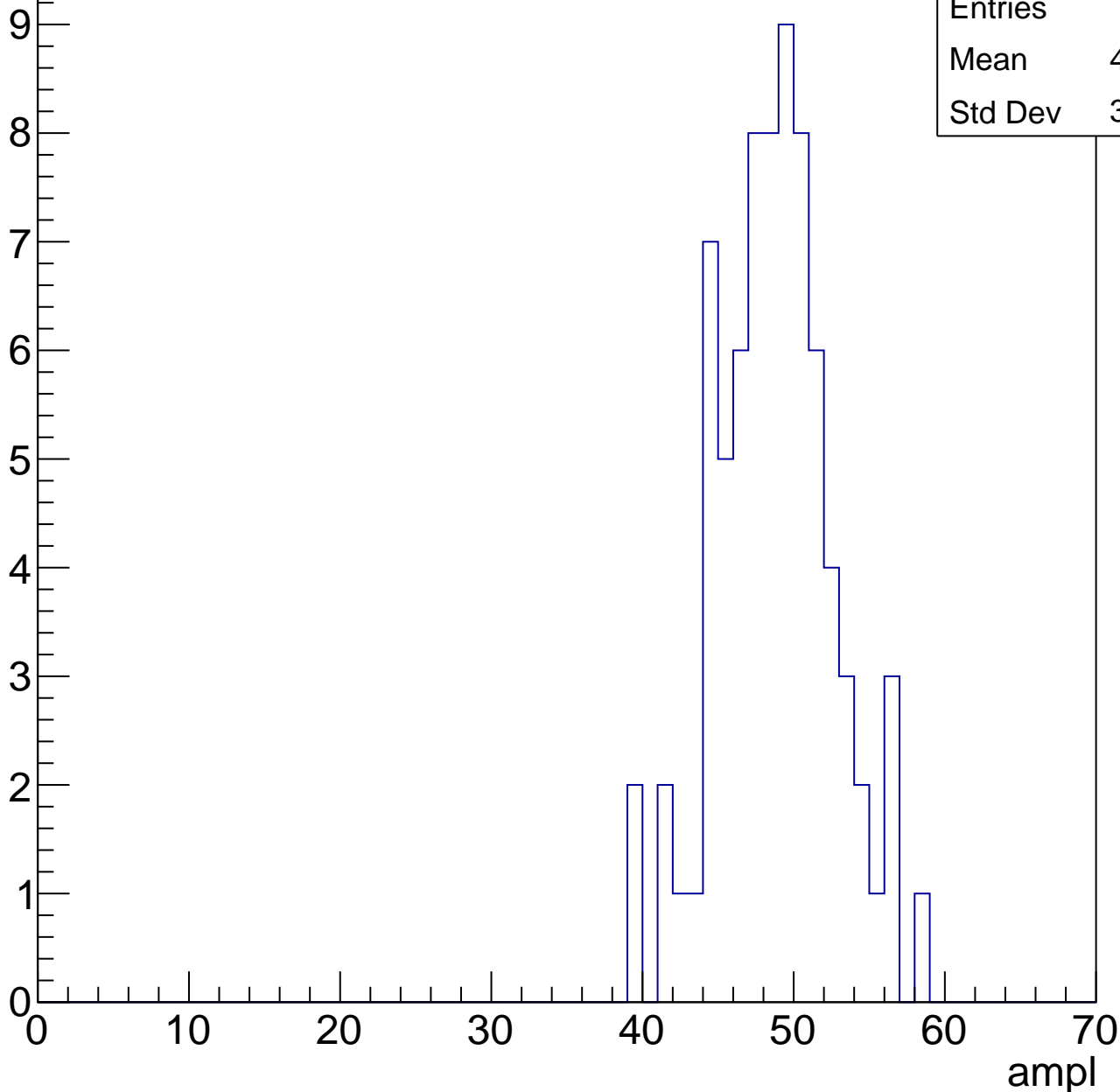


# B1L102S, U5-ch31, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	48.27
Std Dev	3.867

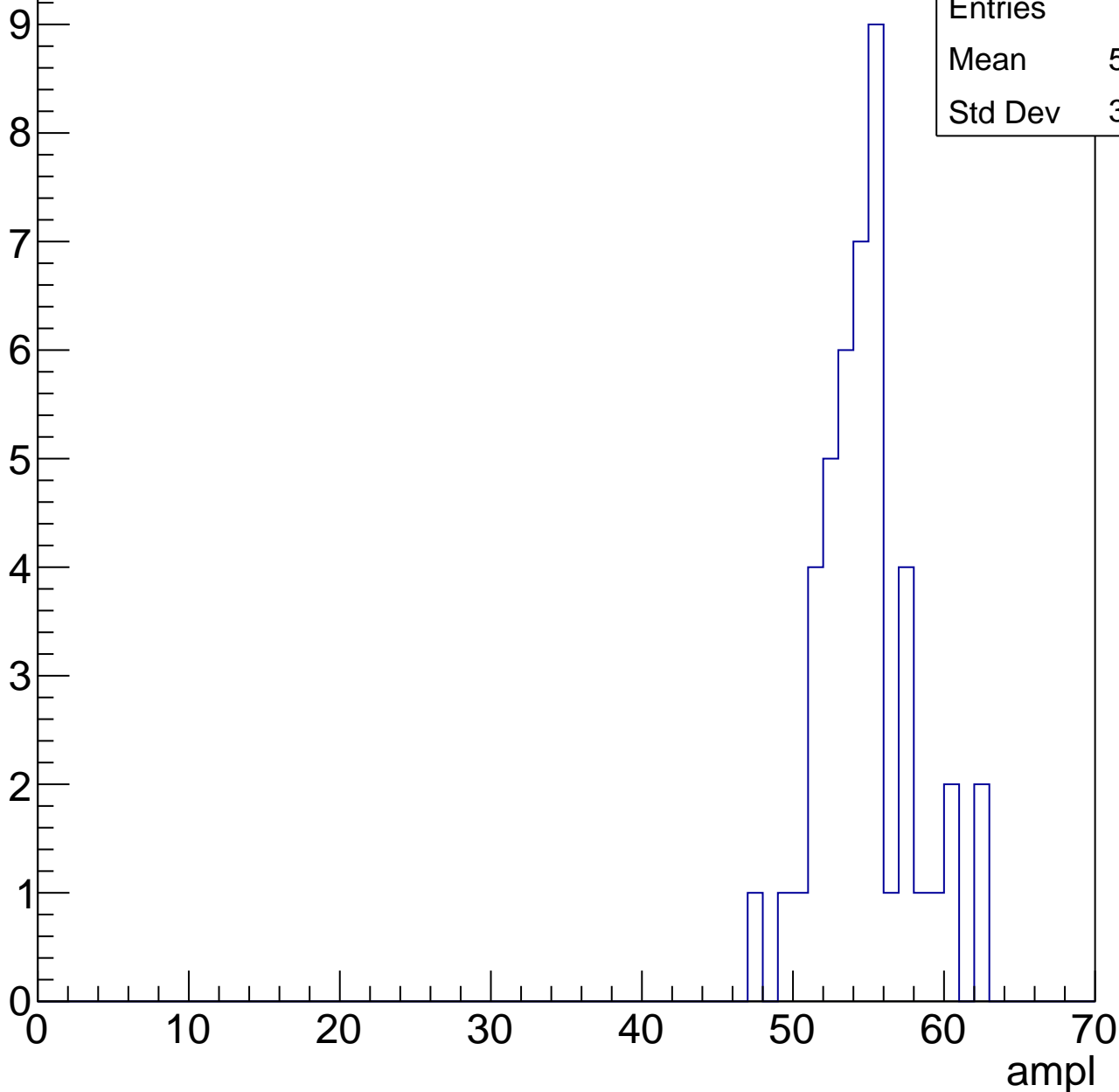


# B1L102S, U5-ch31, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	45
Mean	54.36
Std Dev	3.114

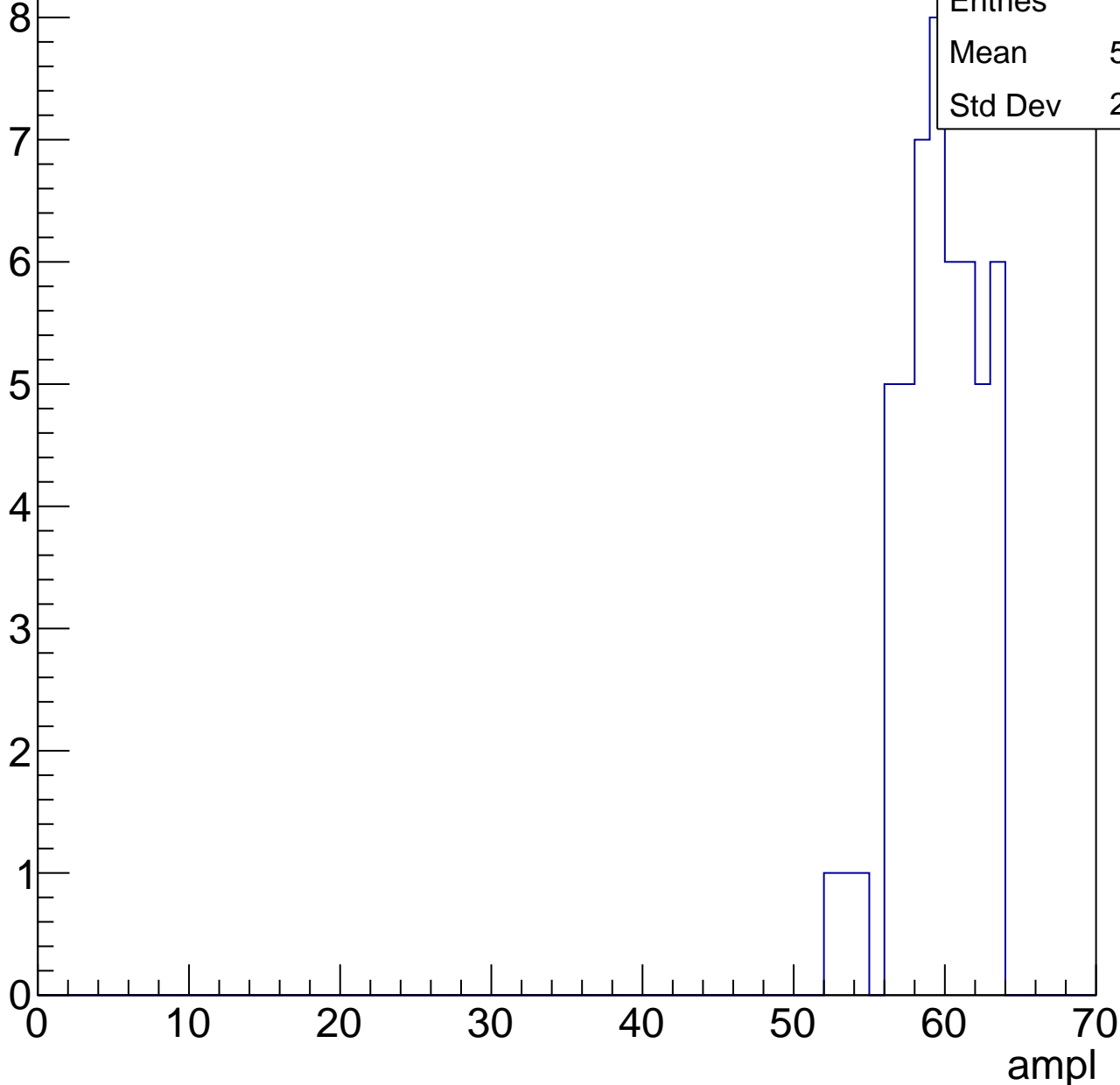


# B1L102S, U5-ch31, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

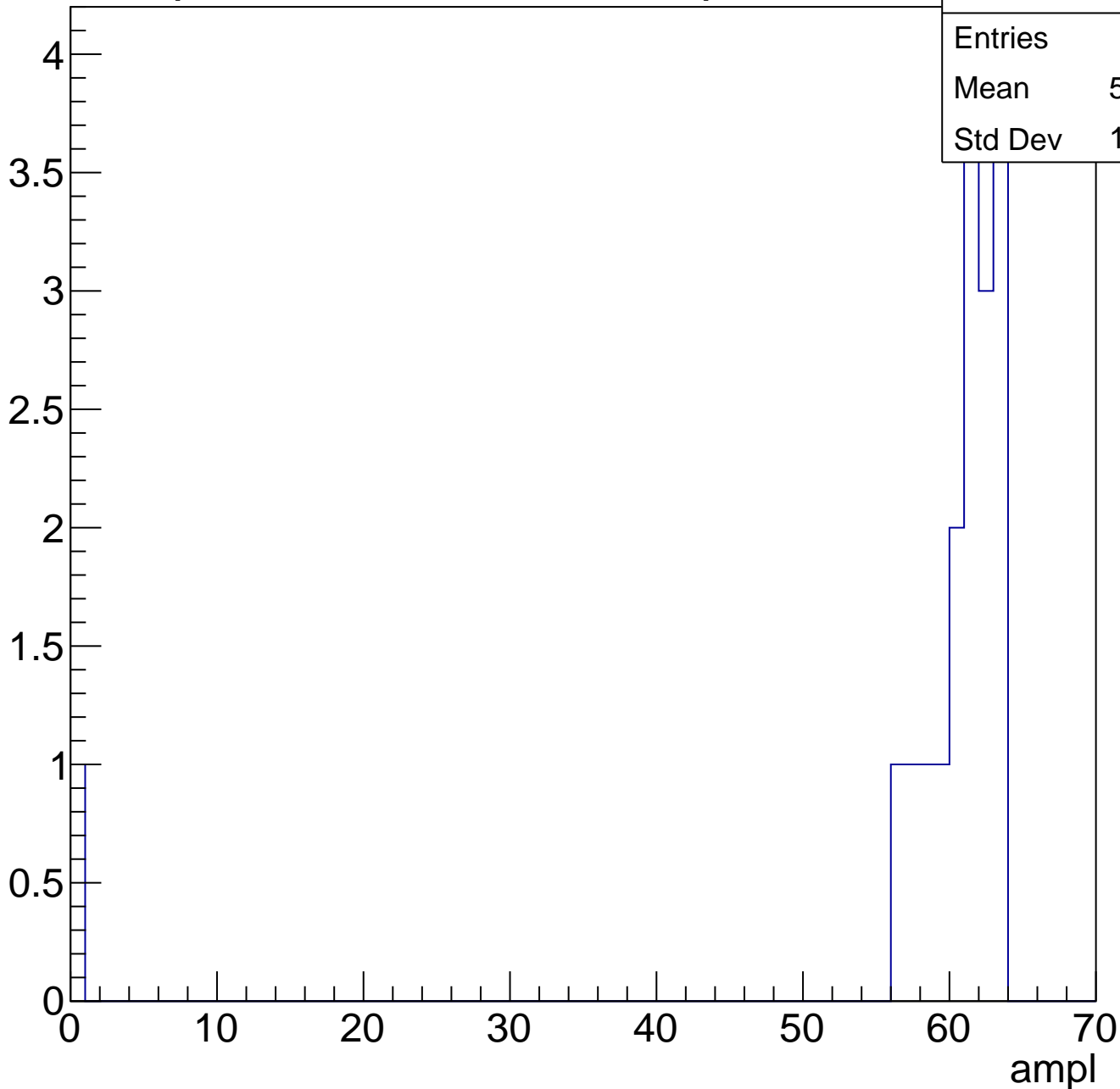
Entries	51
Mean	59.14
Std Dev	2.627



# B1L102S, U5-ch31, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	18
Mean	57.33
Std Dev	14.05



# B1L102S, U5-ch31, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U5-ch32, adc0

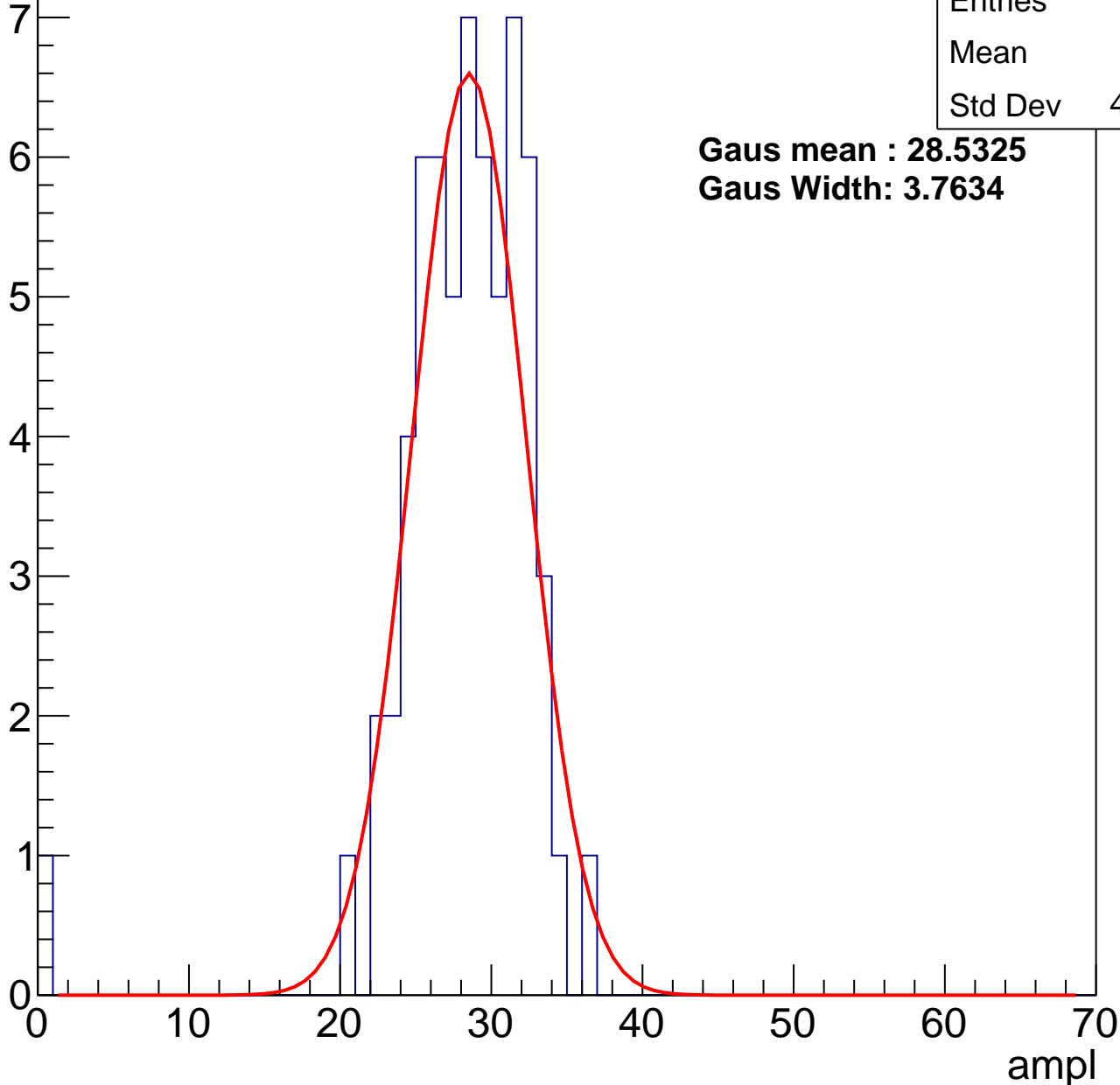
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	27.7
Std Dev	4.833

**Gaus mean : 28.5325**

**Gaus Width: 3.7634**



# B1L102S, U5-ch32, adc1

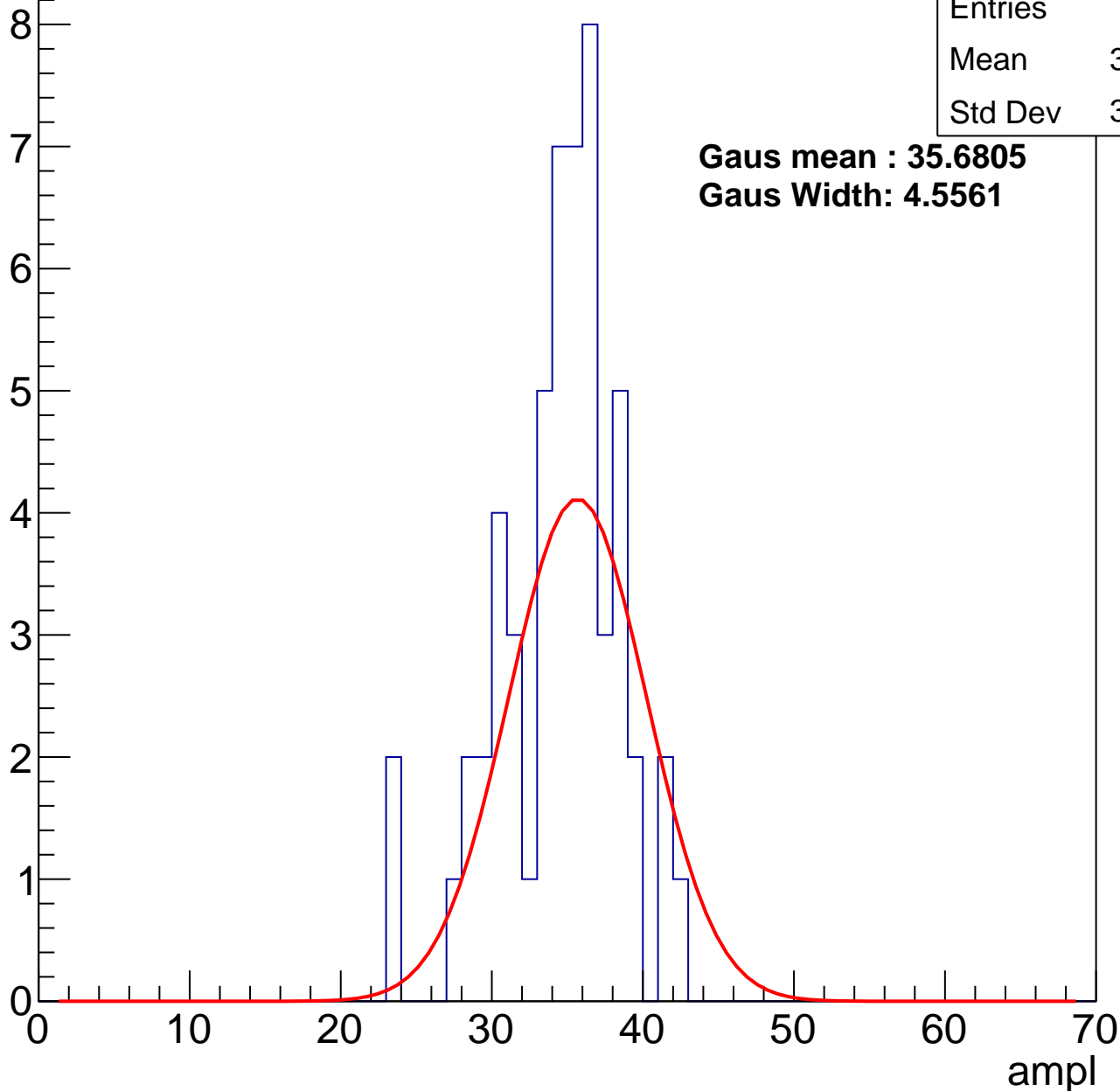
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	34.02
Std Dev	3.979

**Gaus mean : 35.6805**

**Gaus Width: 4.5561**



# B1L102S, U5-ch32, adc2

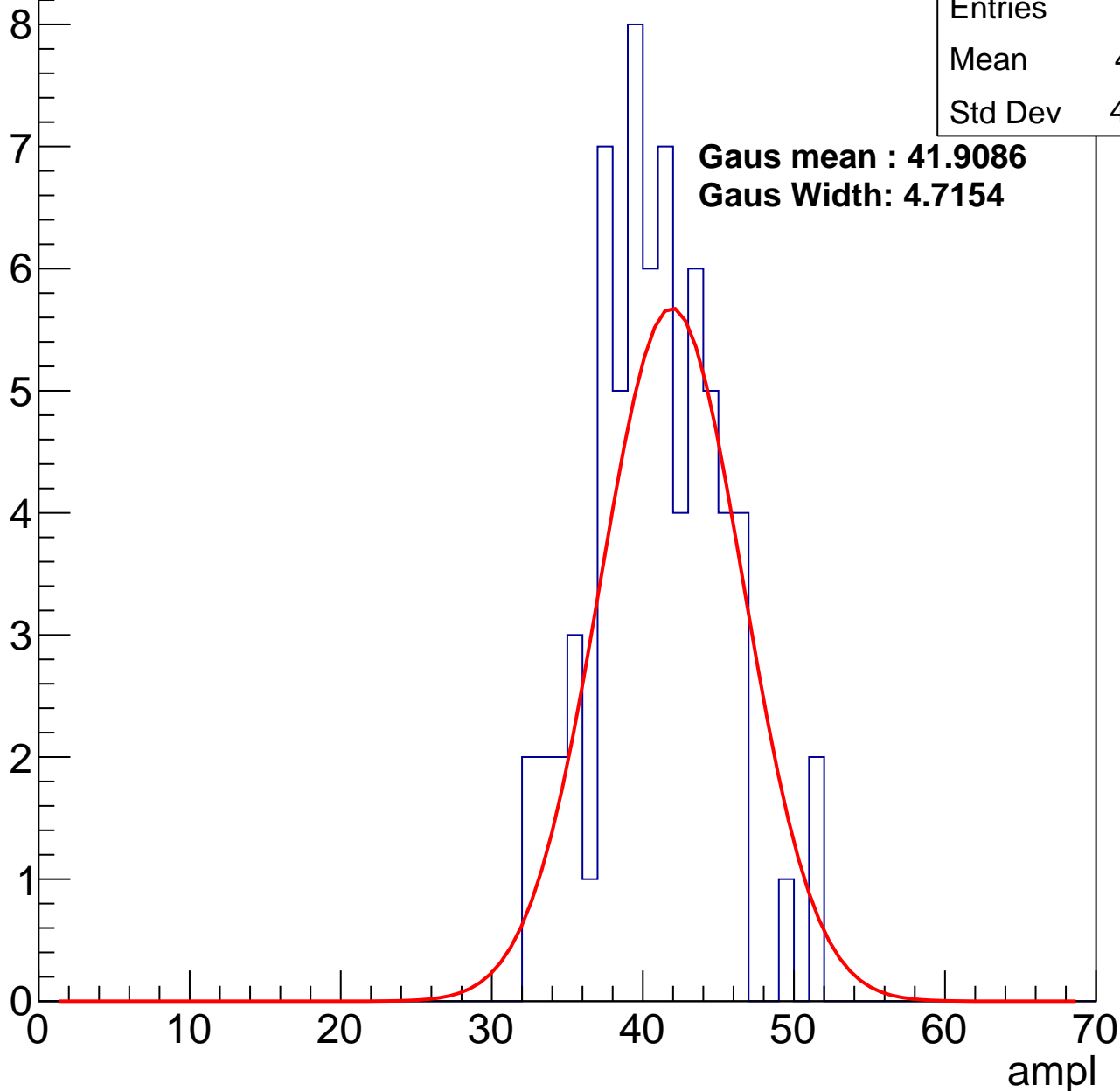
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	40.41
Std Dev	4.157

**Gaus mean : 41.9086**

**Gaus Width: 4.7154**

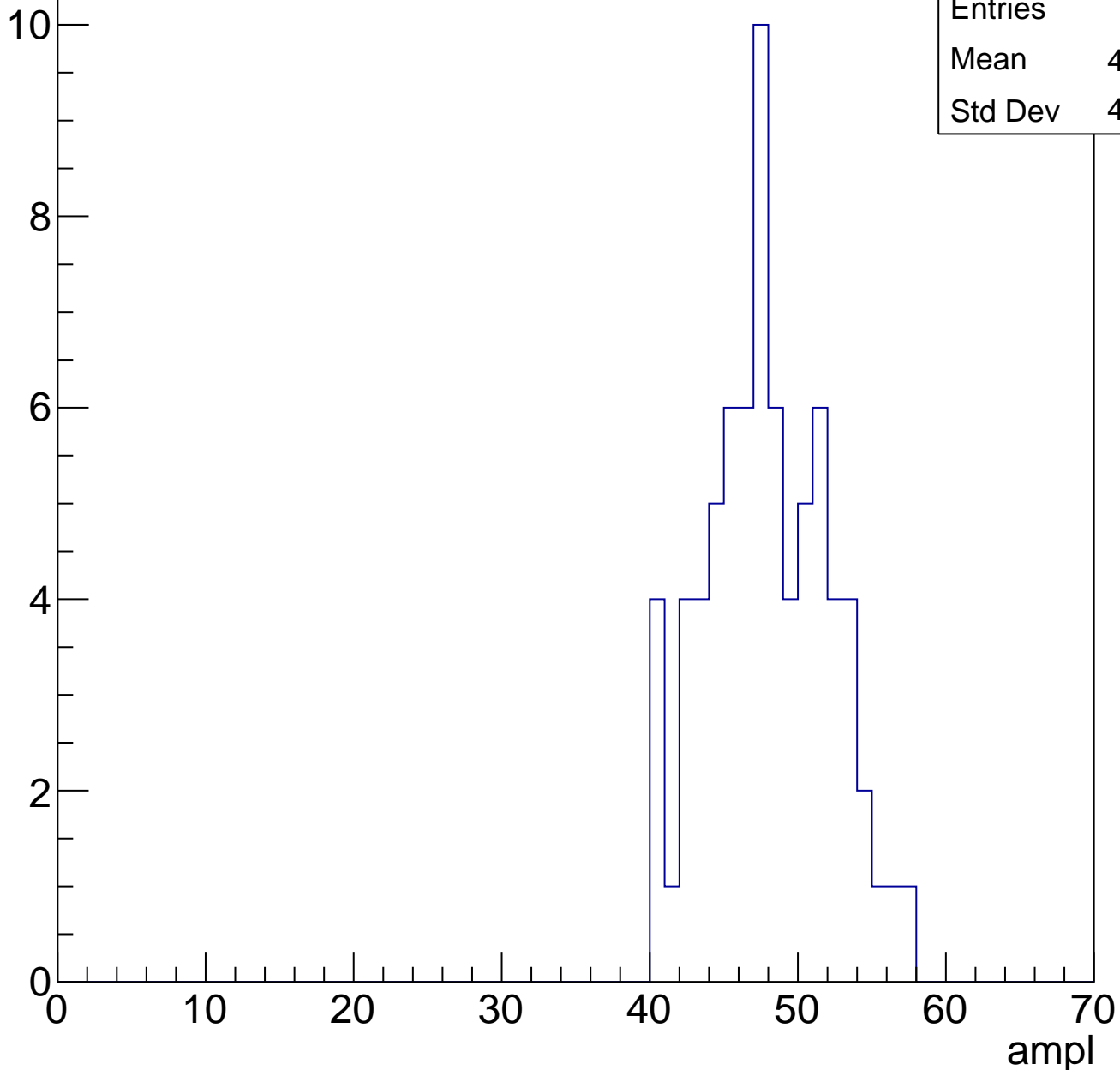


# B1L102S, U5-ch32, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	74
Mean	47.47
Std Dev	4.034

Entry

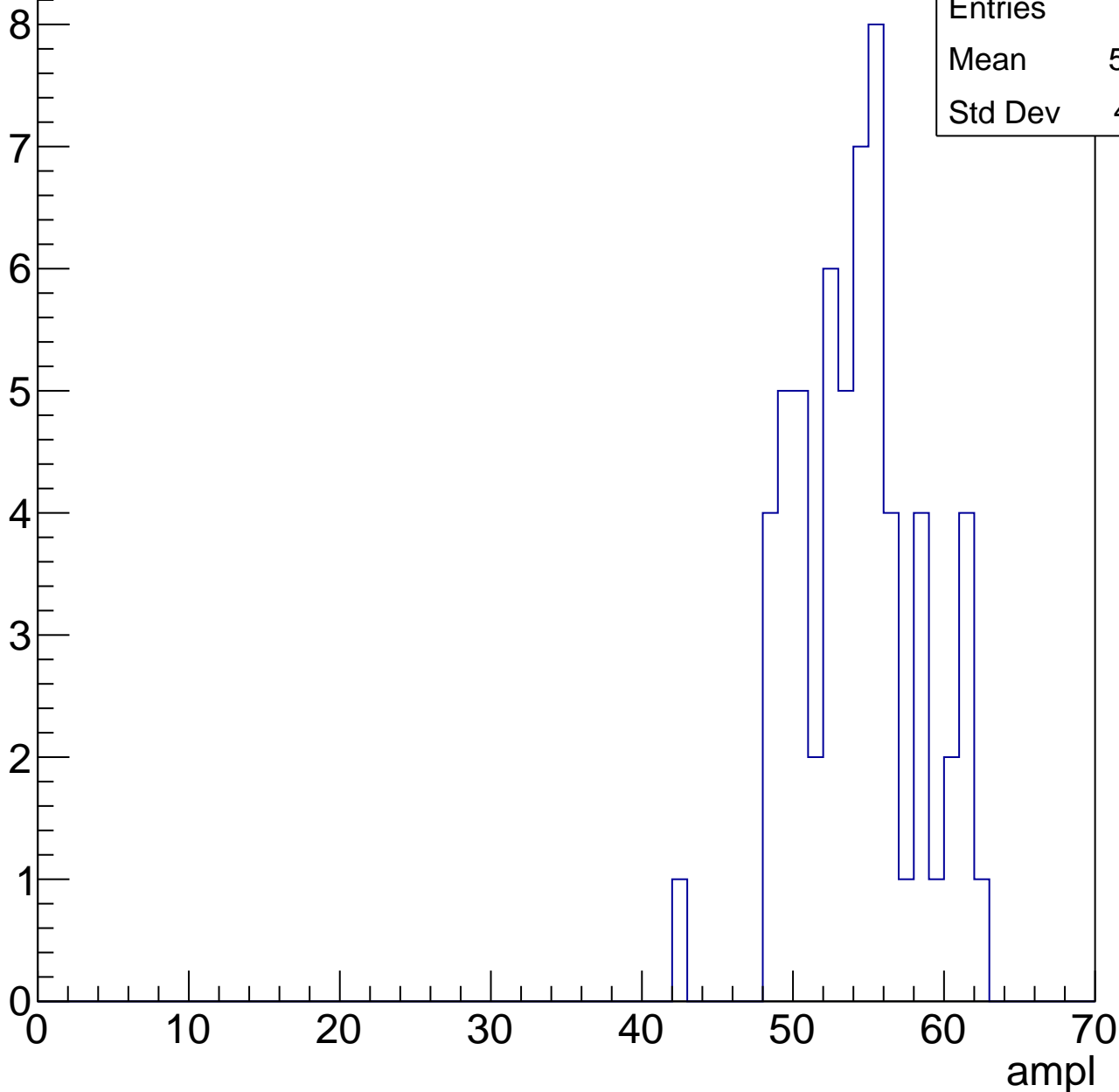


# B1L102S, U5-ch32, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	53.73
Std Dev	4.061

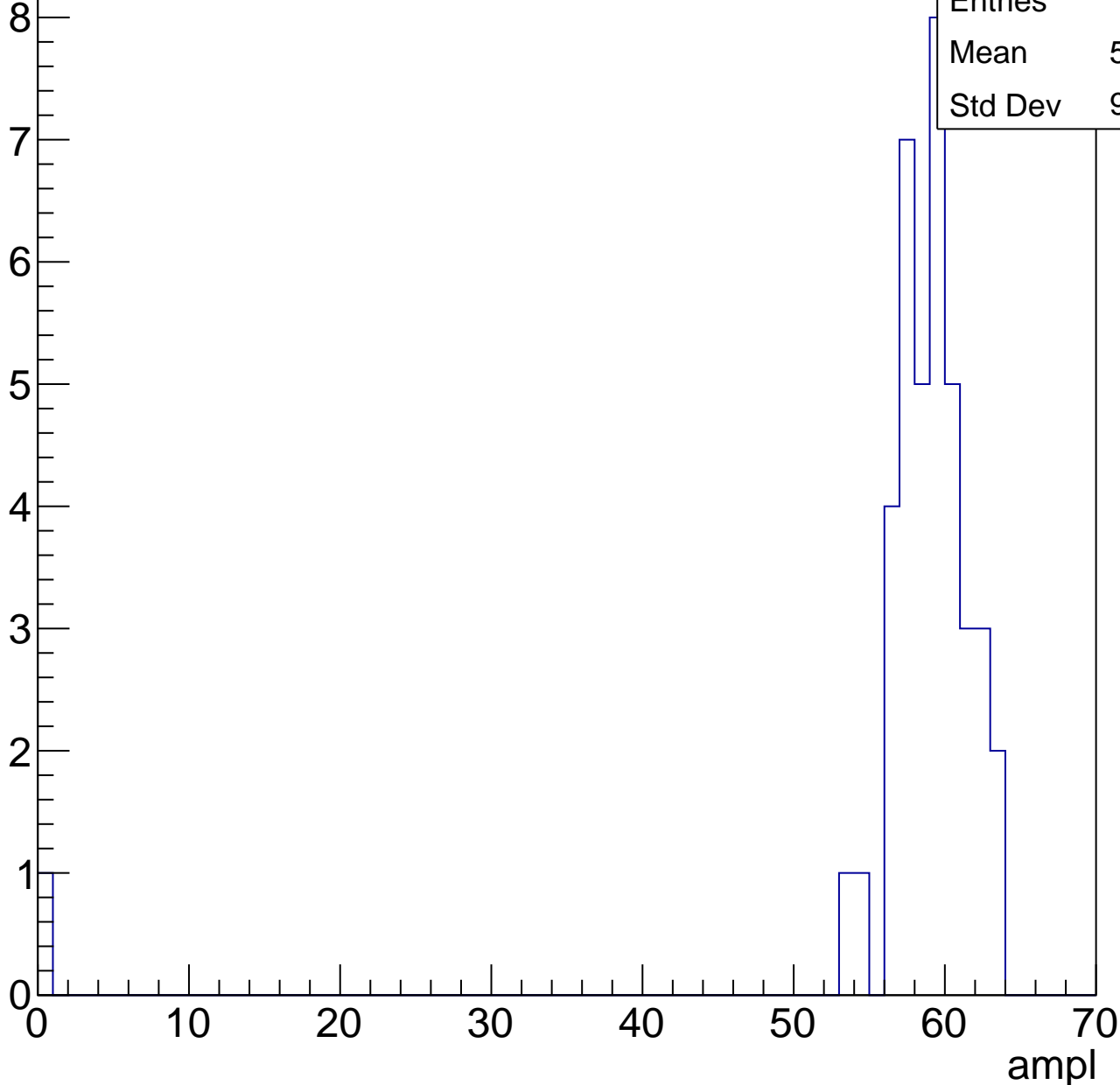


# B1L102S, U5-ch32, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	40
Mean	57.17
Std Dev	9.426

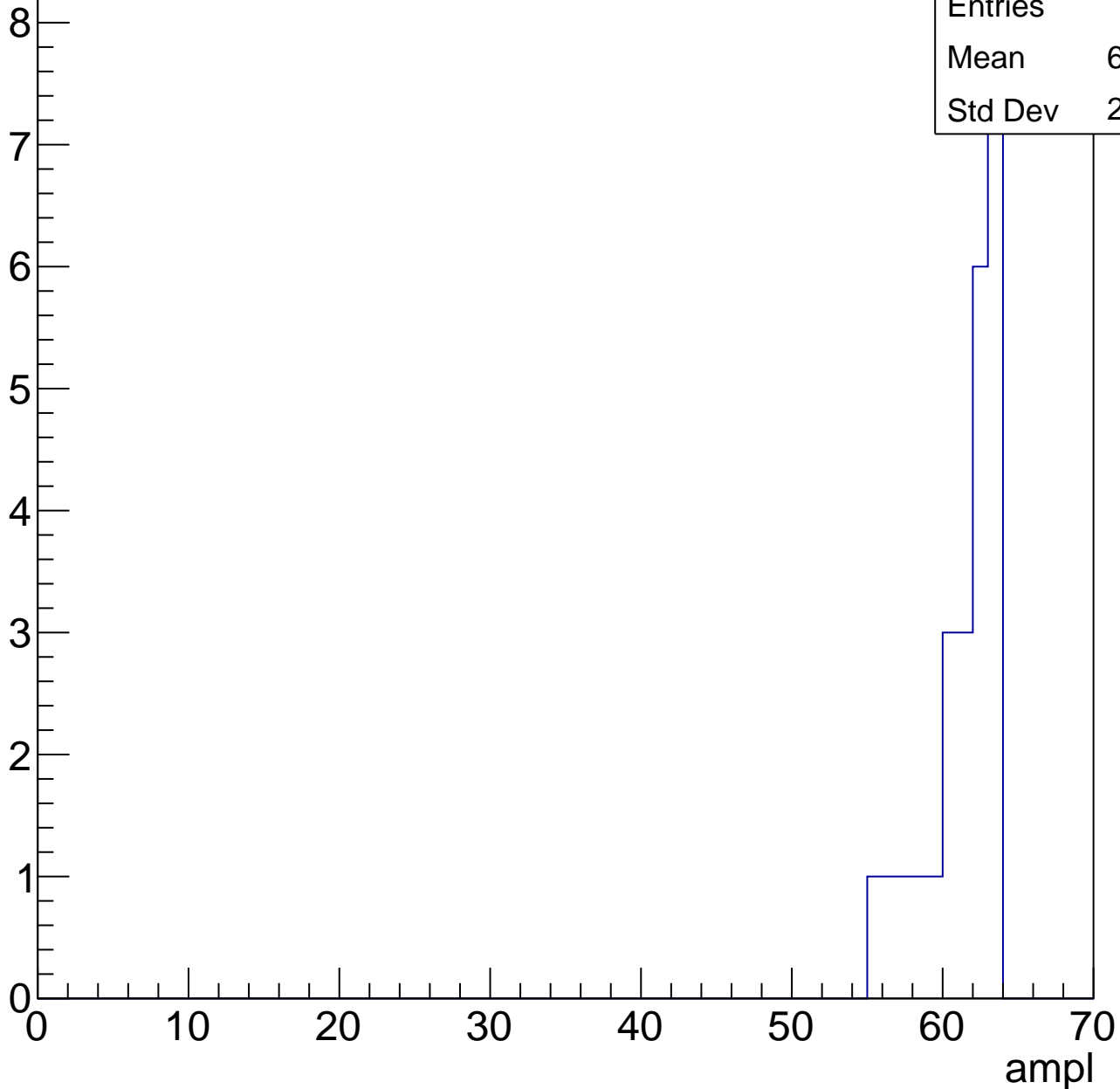


# B1L102S, U5-ch32, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	25
Mean	60.96
Std Dev	2.289





# B1L102S, U5-ch32, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U5-ch33, adc0

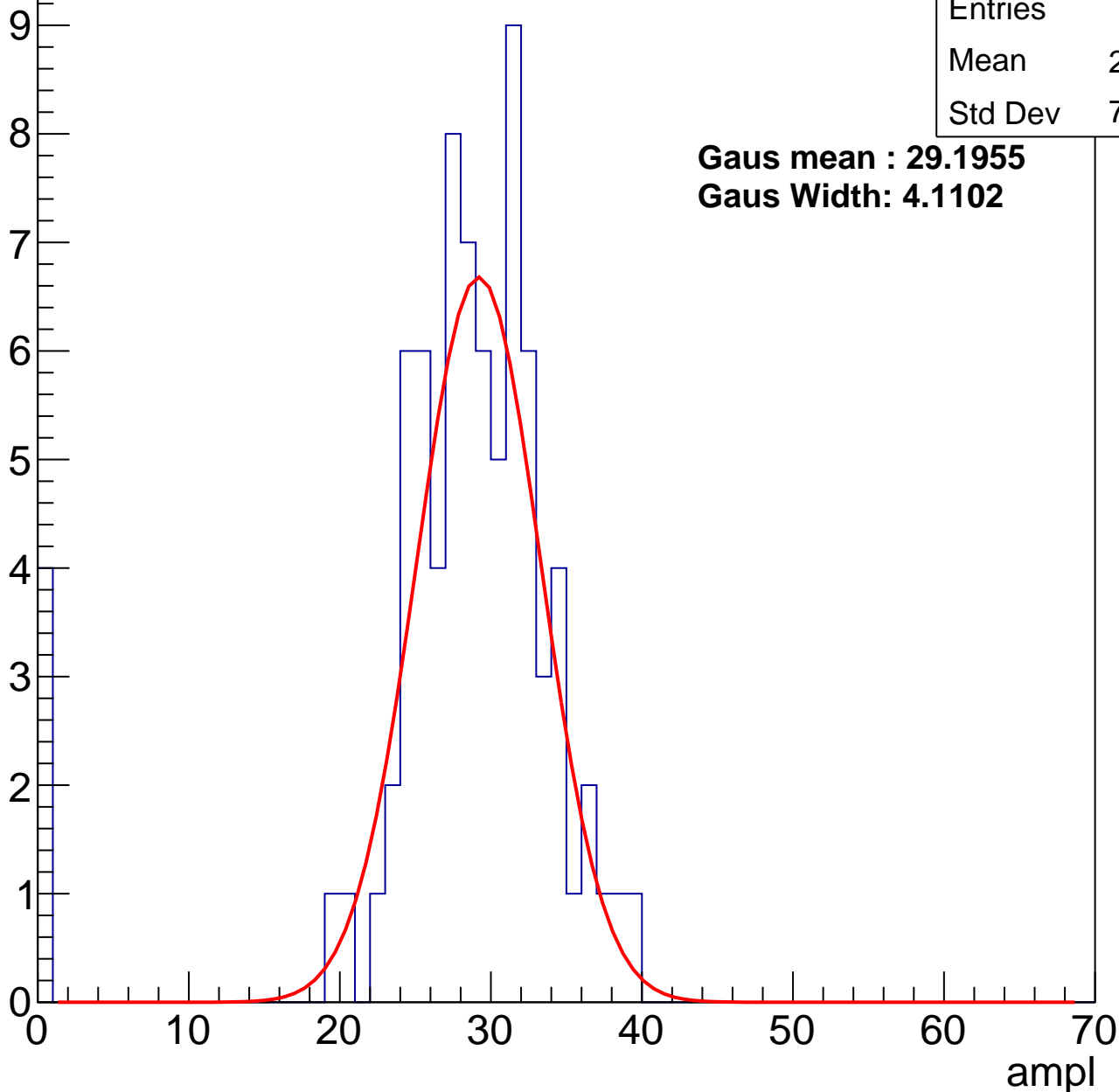
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	79
Mean	27.44
Std Dev	7.478

**Gaus mean : 29.1955**

**Gaus Width: 4.1102**



# B1L102S, U5-ch33, adc1

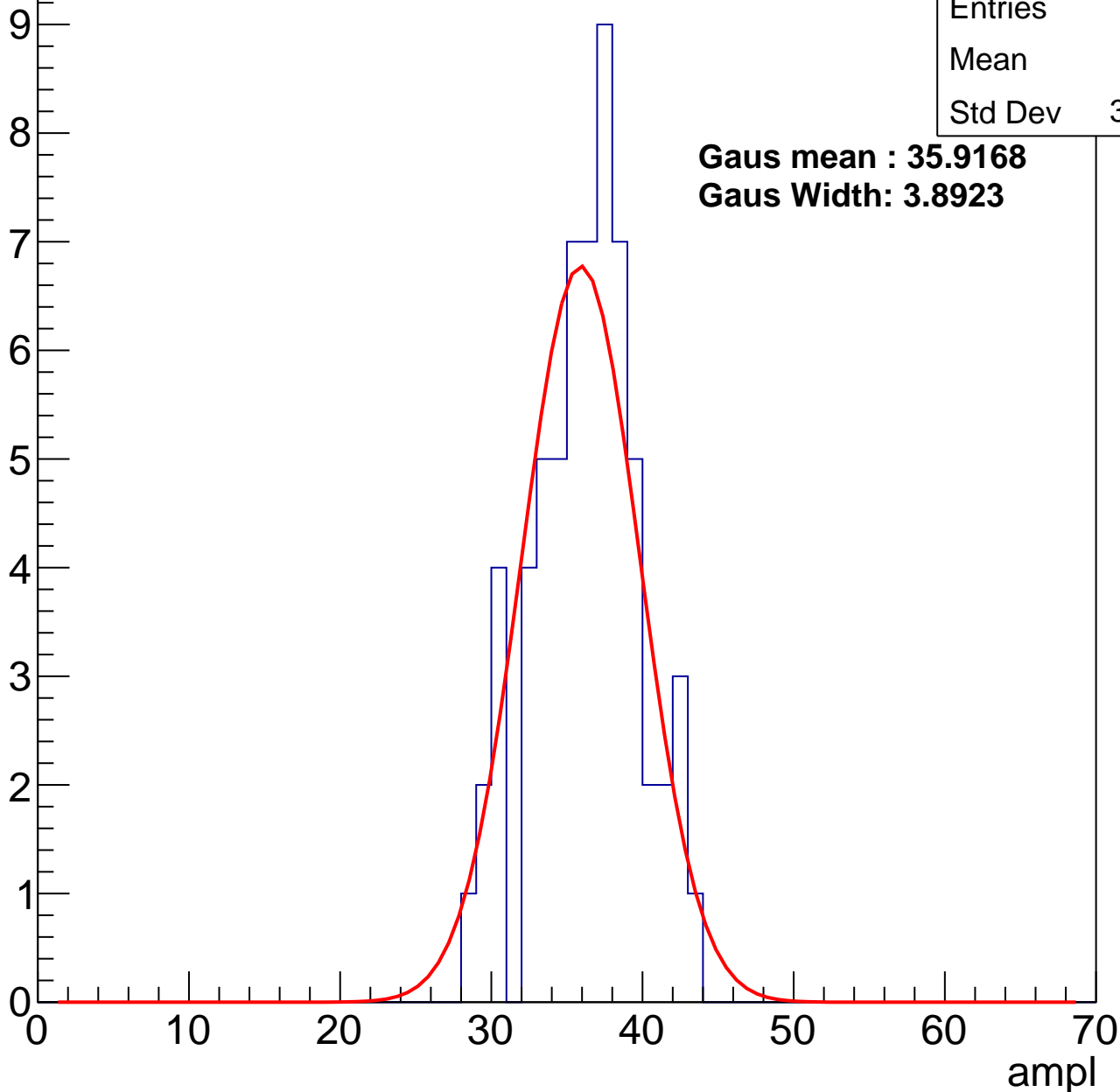
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	35.8
Std Dev	3.447

**Gaus mean : 35.9168**

**Gaus Width: 3.8923**



# B1L102S, U5-ch33, adc2

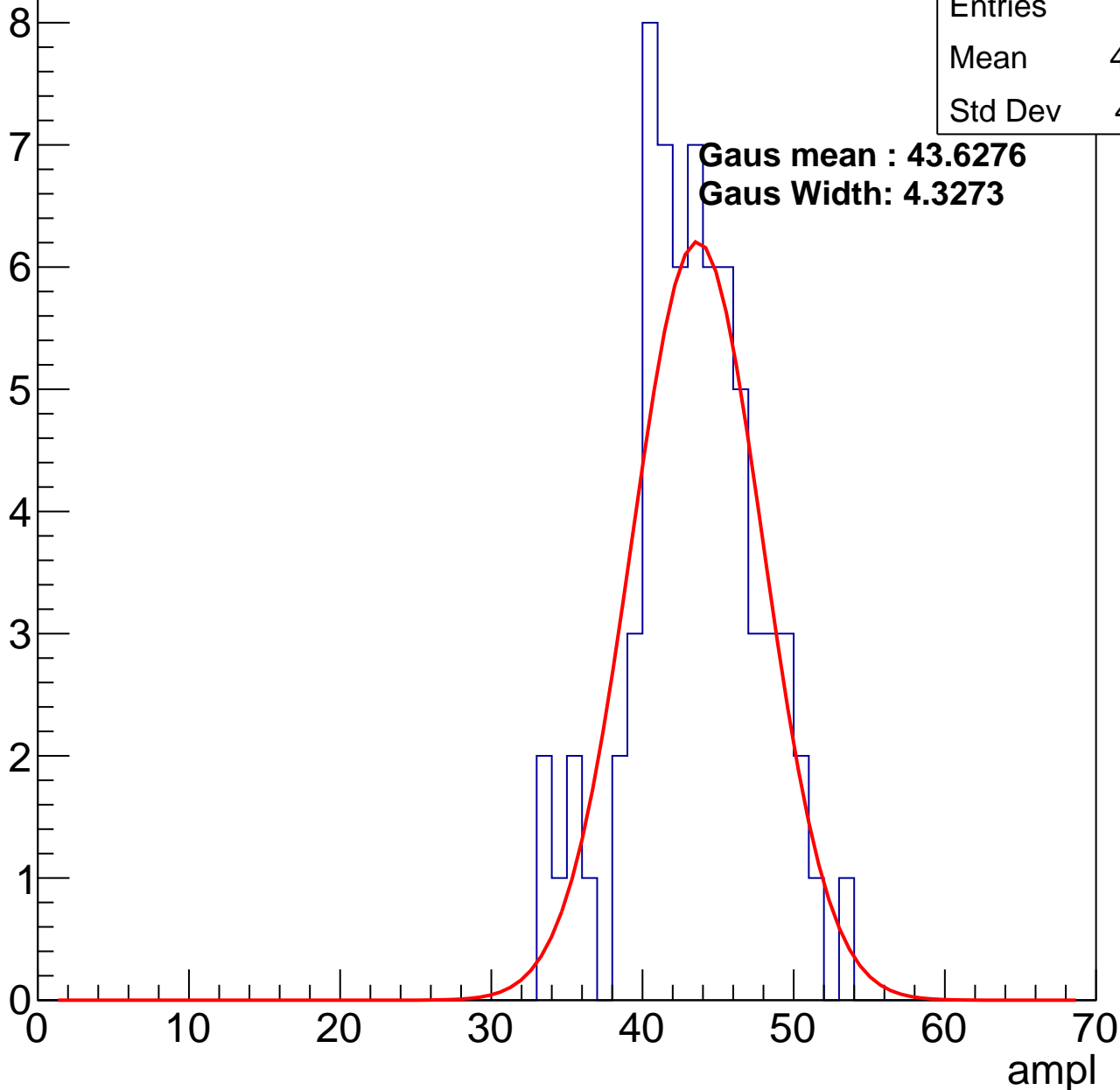
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	42.88
Std Dev	4.221

**Gaus mean : 43.6276**

**Gaus Width: 4.3273**

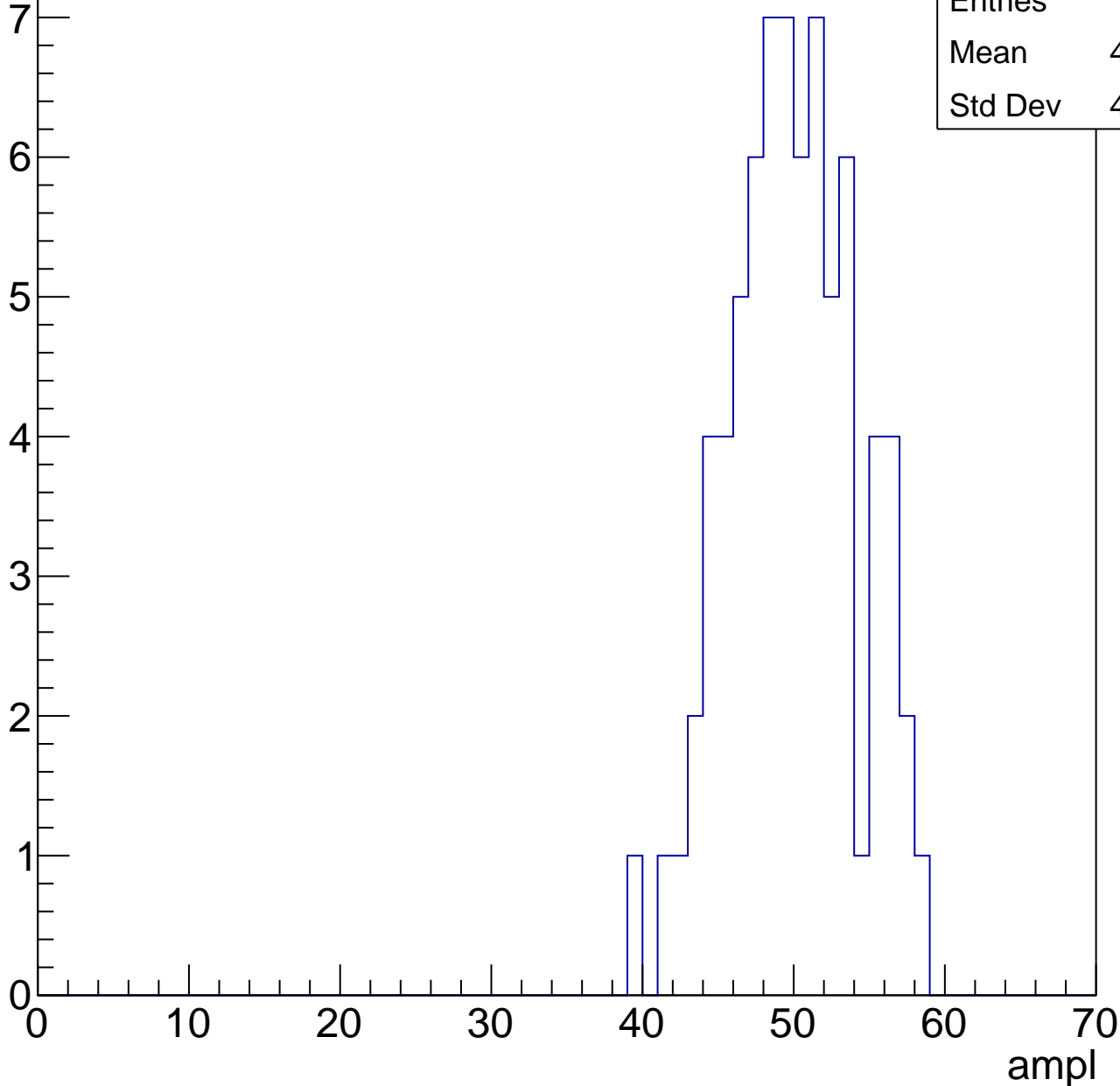


# B1L102S, U5-ch33, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

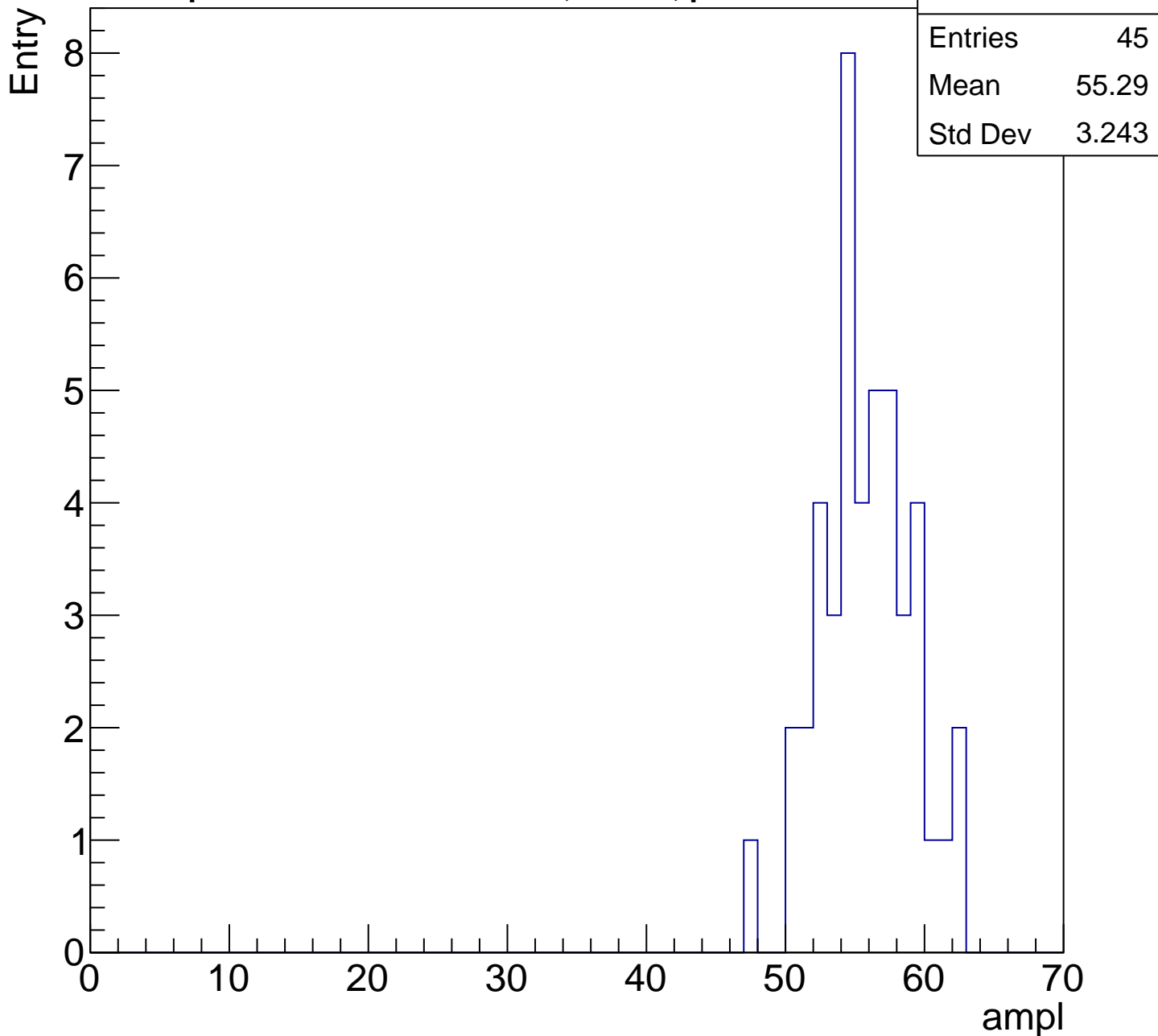
Entry

Entries	74
Mean	49.46
Std Dev	4.124



# B1L102S, U5-ch33, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

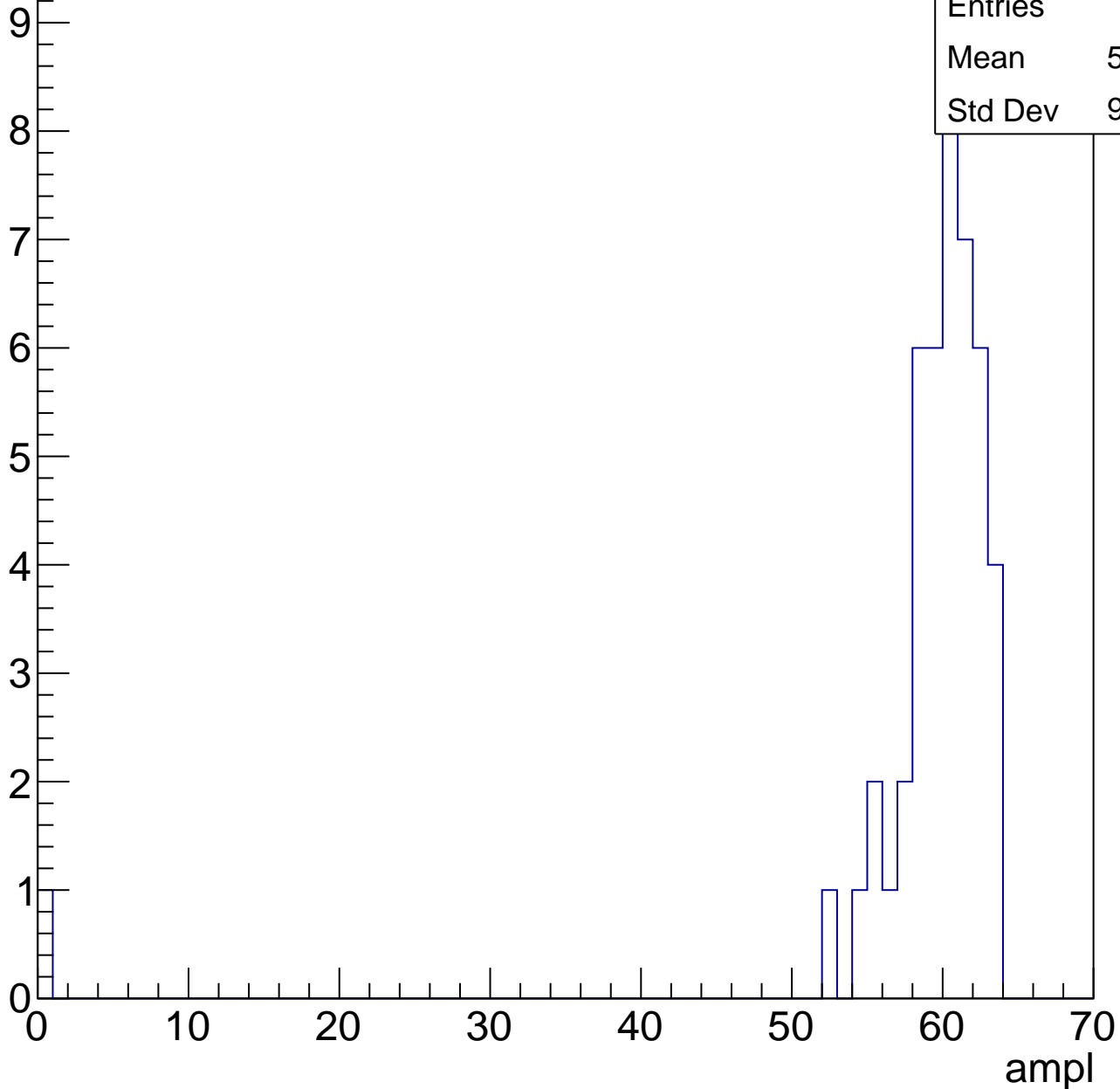


# B1L102S, U5-ch33, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	46
Mean	58.24
Std Dev	9.015

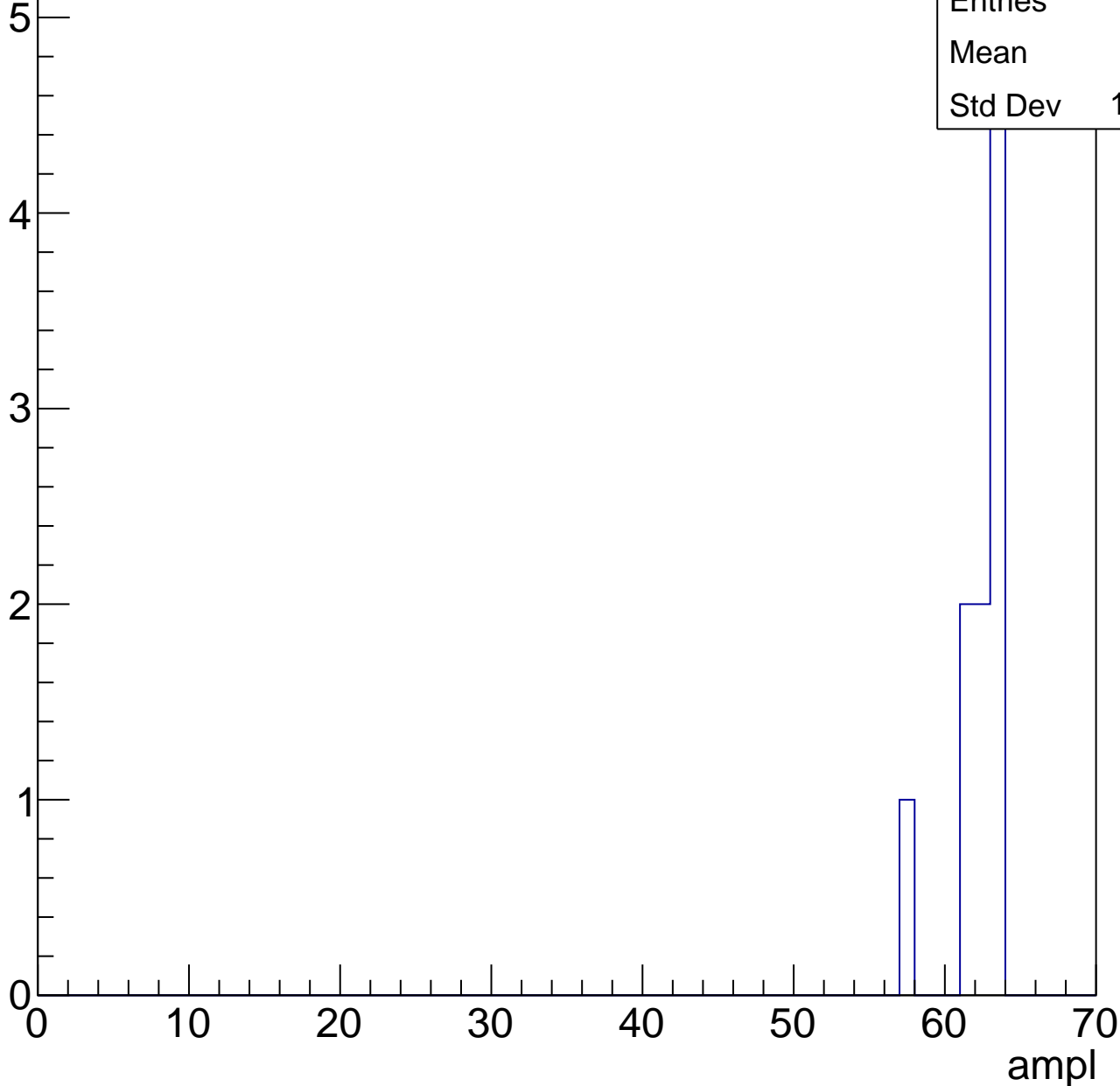


# B1L102S, U5-ch33, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	10
Mean	61.8
Std Dev	1.778





# B1L102S, U5-ch33, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U5-ch34, adc0

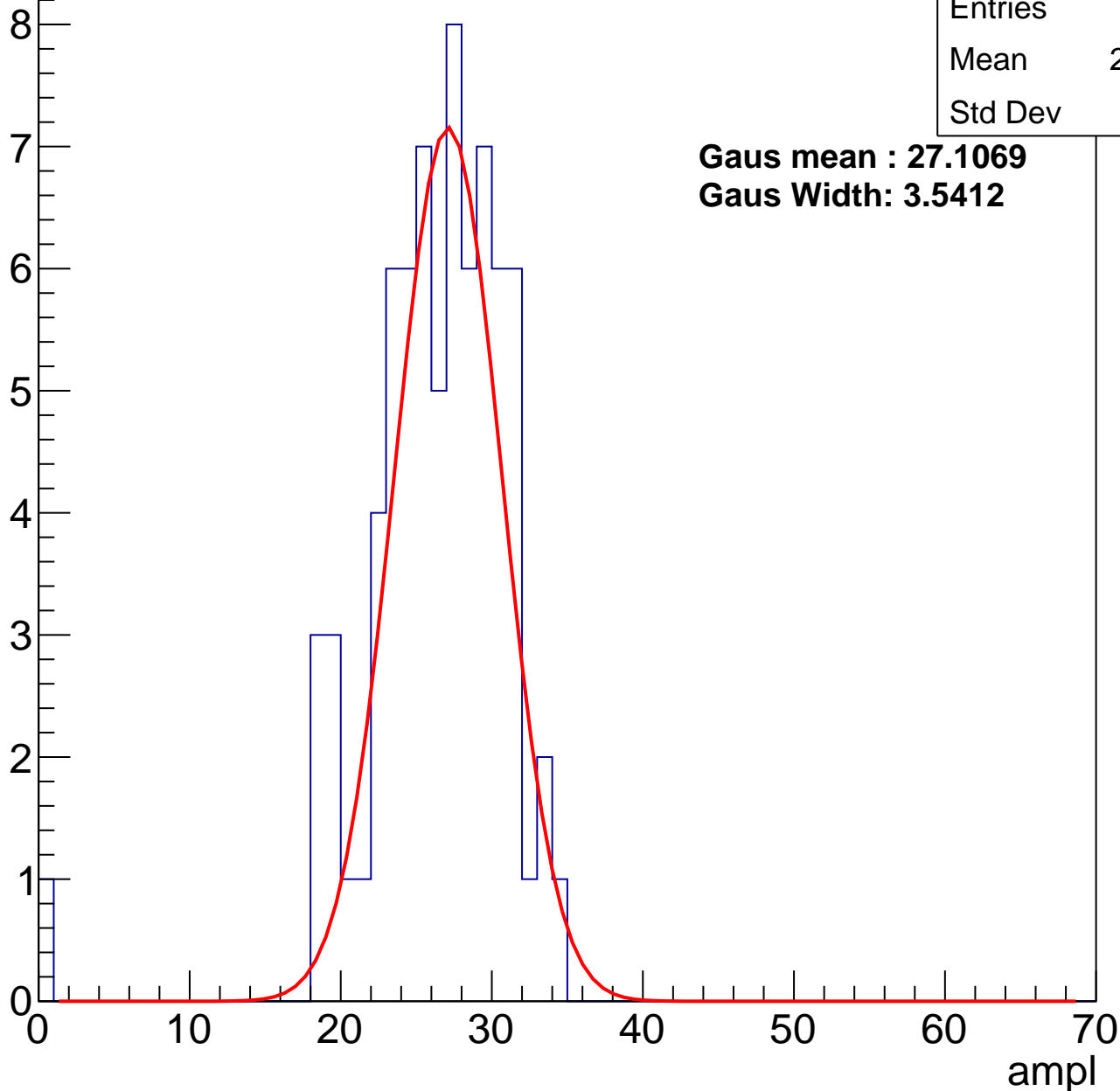
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	25.84
Std Dev	4.88

**Gaus mean : 27.1069**

**Gaus Width: 3.5412**



# B1L102S, U5-ch34, adc1

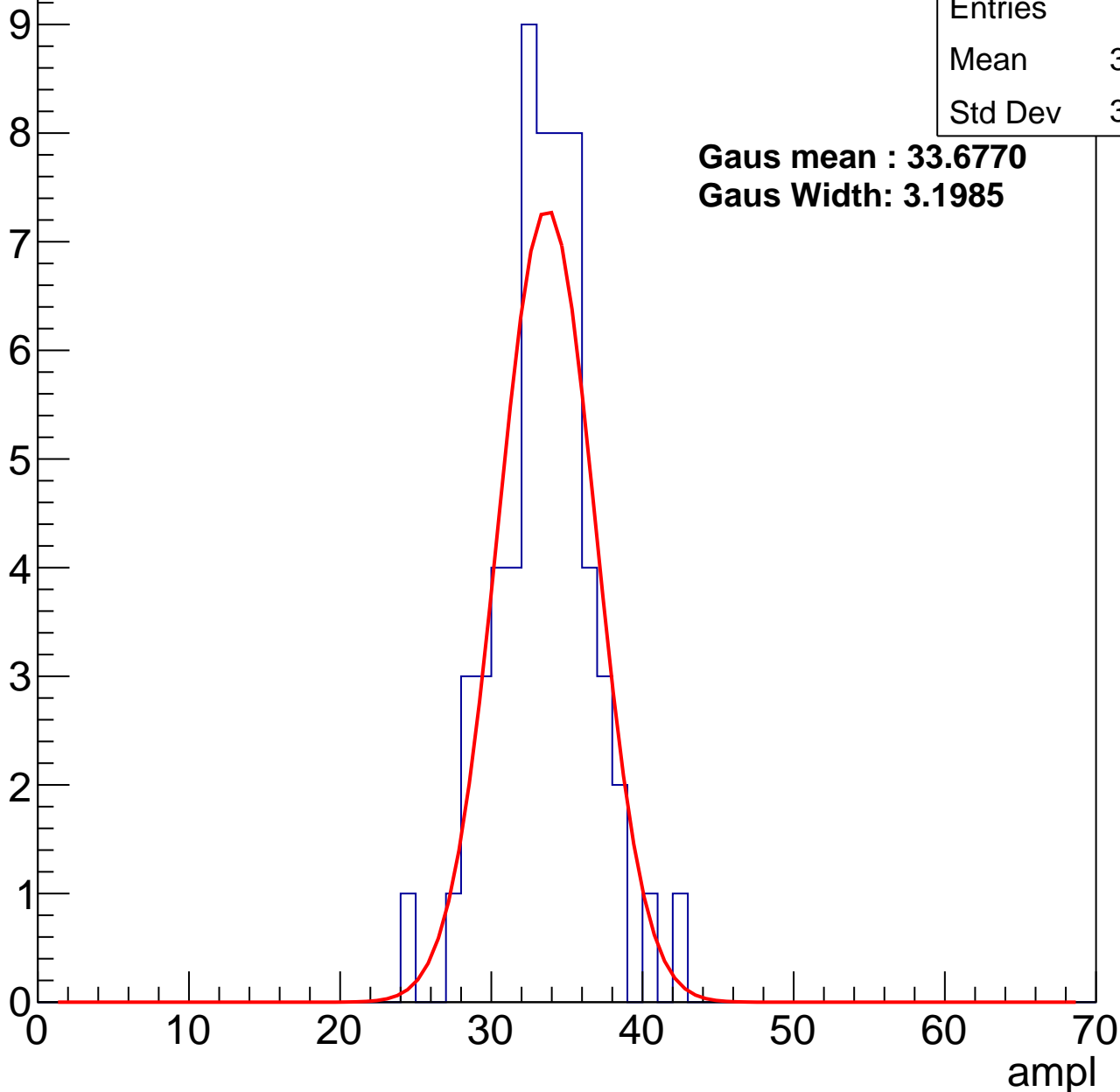
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	33.05
Std Dev	3.175

**Gaus mean : 33.6770**

**Gaus Width: 3.1985**



# B1L102S, U5-ch34, adc2

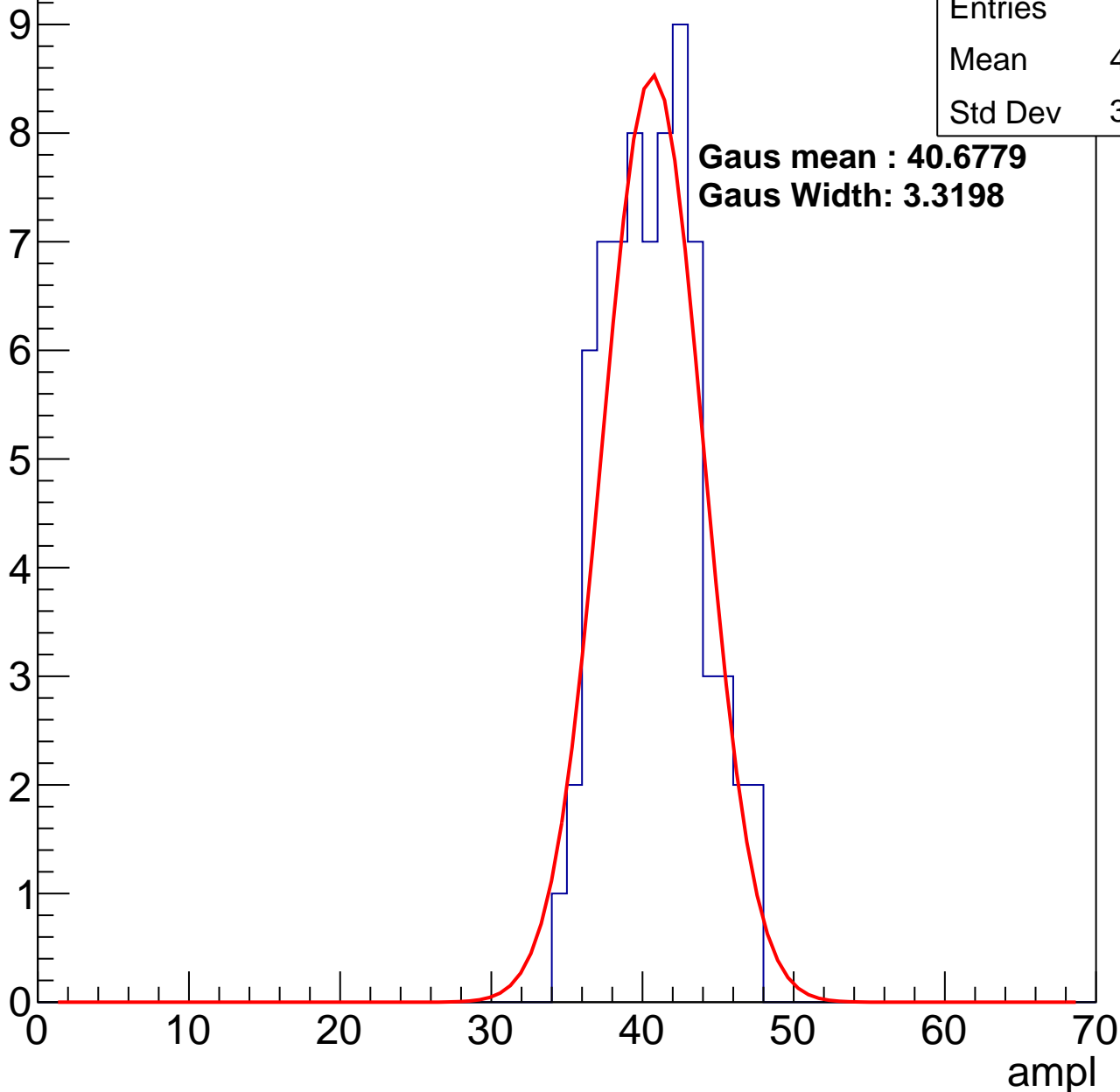
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	40.24
Std Dev	3.066

**Gaus mean : 40.6779**

**Gaus Width: 3.3198**

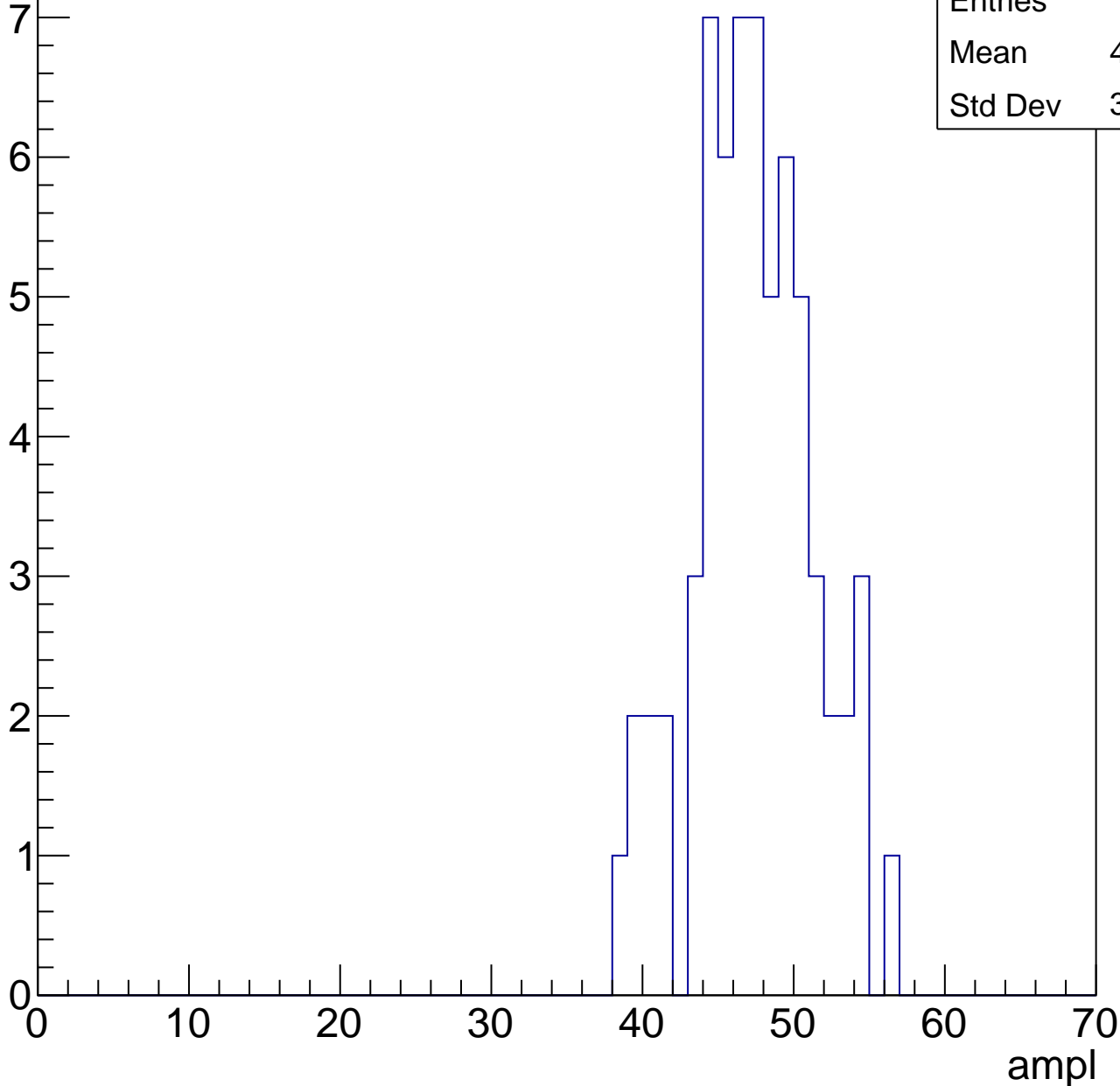


# B1L102S, U5-ch34, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	46.89
Std Dev	3.937

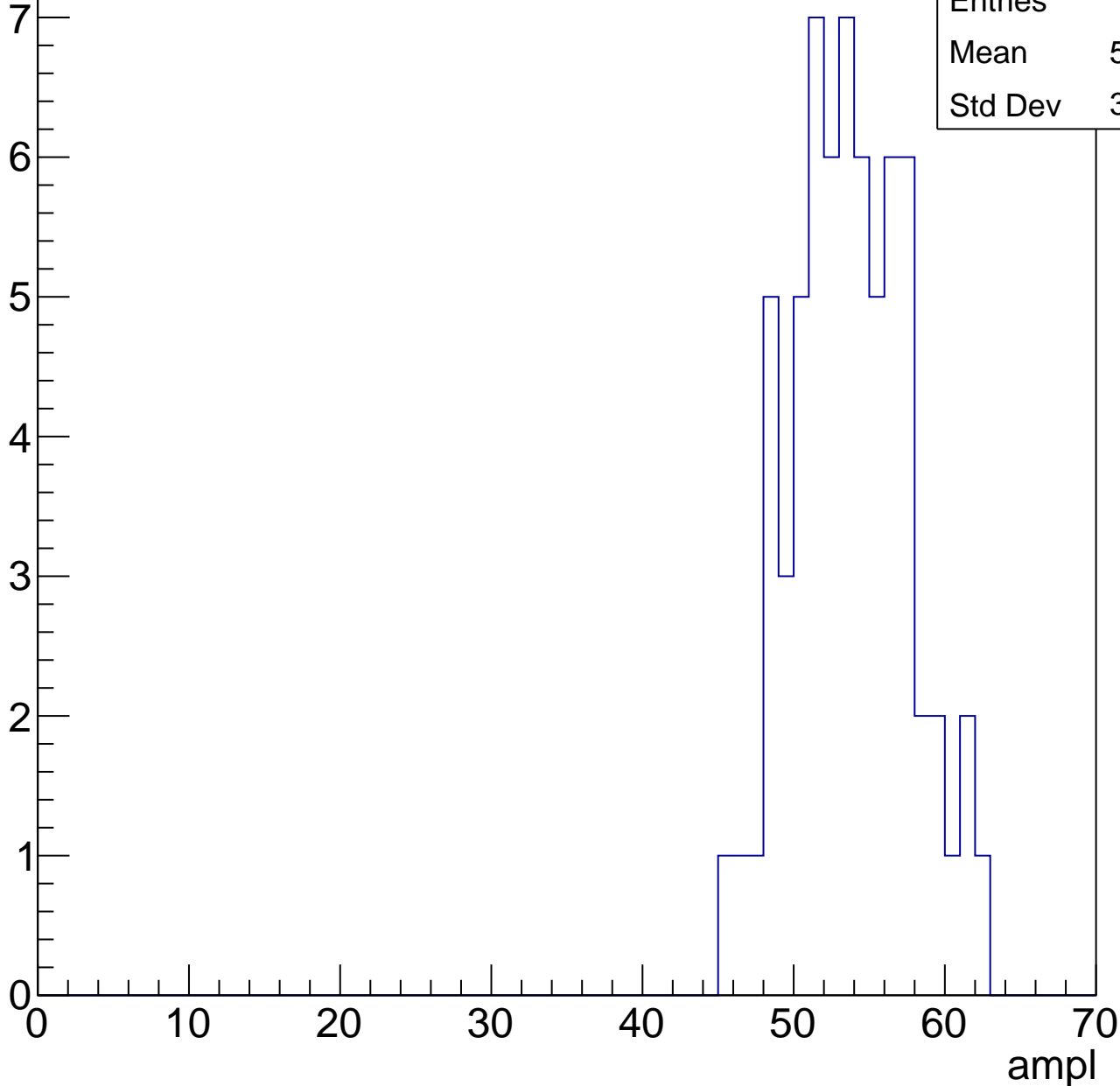


# B1L102S, U5-ch34, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	53.28
Std Dev	3.769

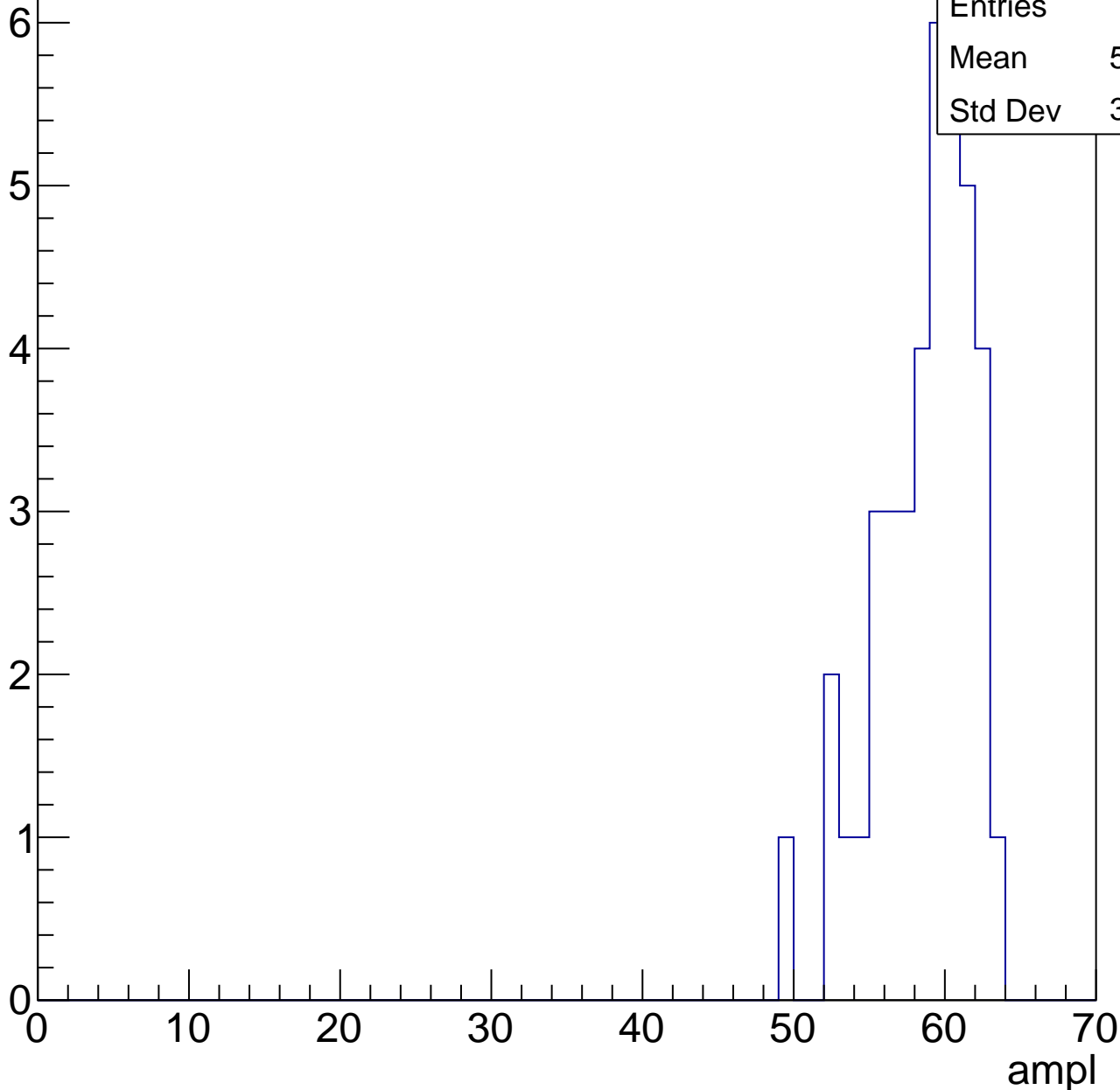


# B1L102S, U5-ch34, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	40
Mean	58.15
Std Dev	3.159

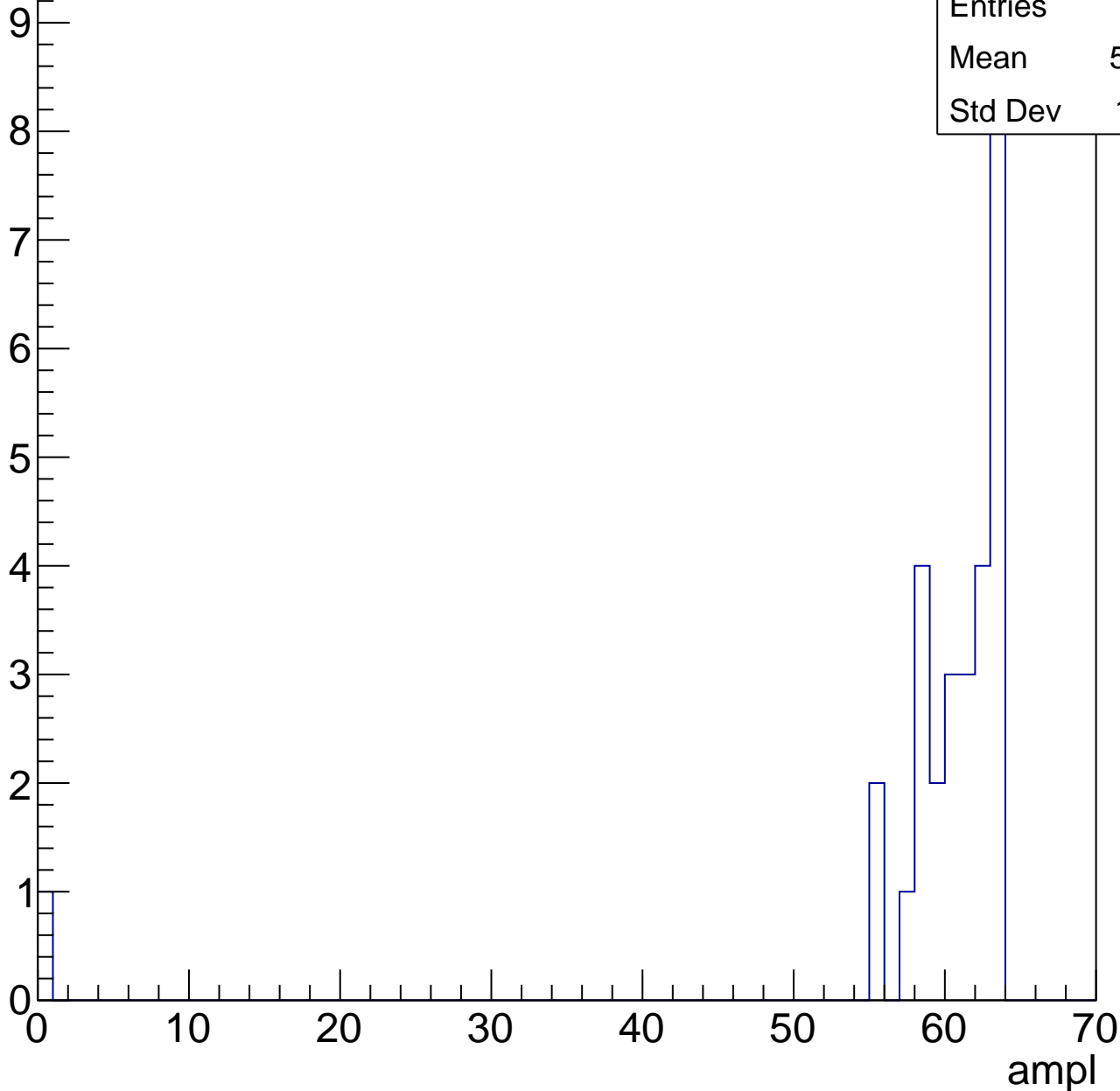


# B1L102S, U5-ch34, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	29
Mean	58.45
Std Dev	11.31





# B1L102S, U5-ch34, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U5-ch35, adc0

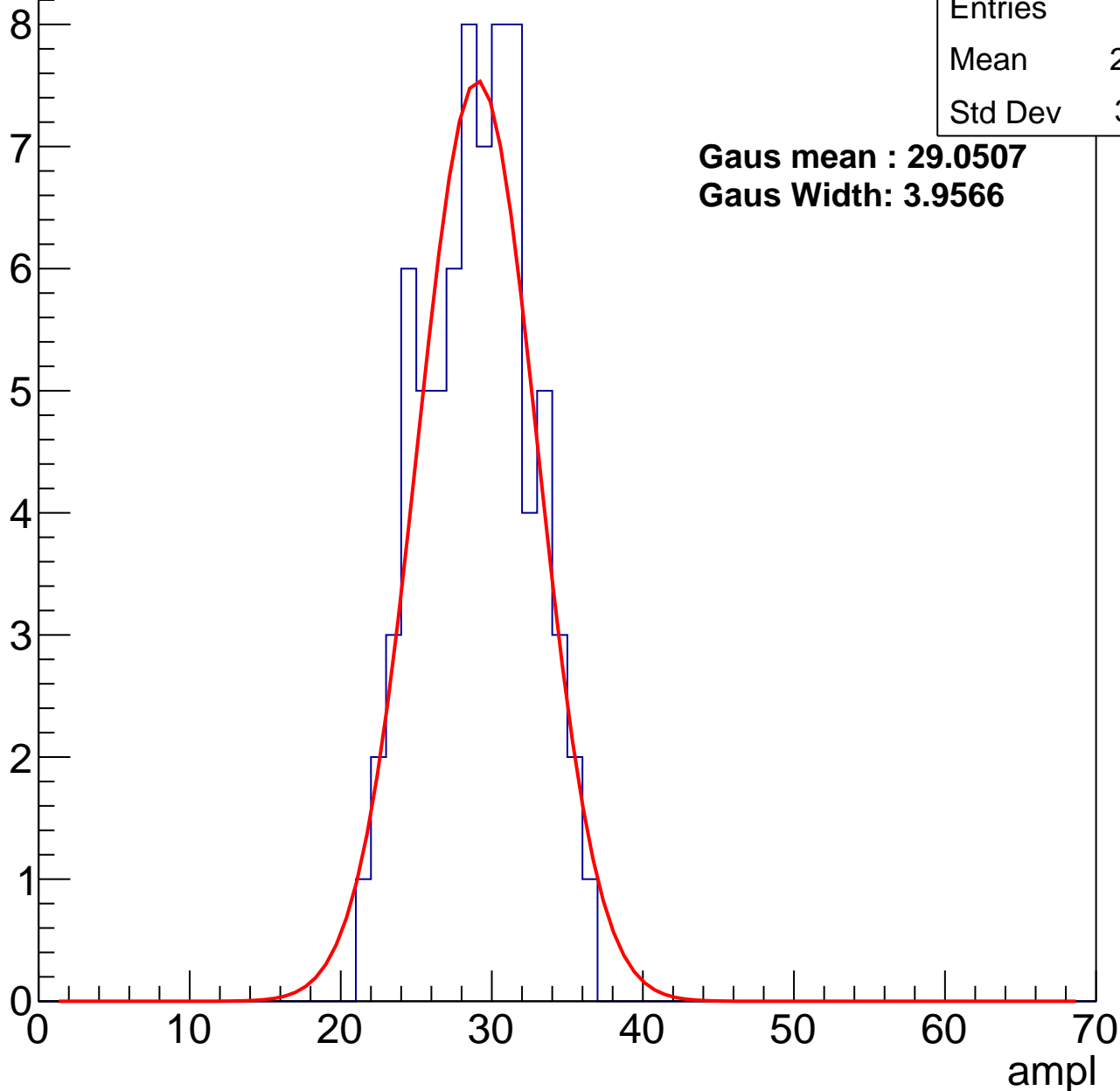
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	28.53
Std Dev	3.511

**Gaus mean : 29.0507**

**Gaus Width: 3.9566**



# B1L102S, U5-ch35, adc1

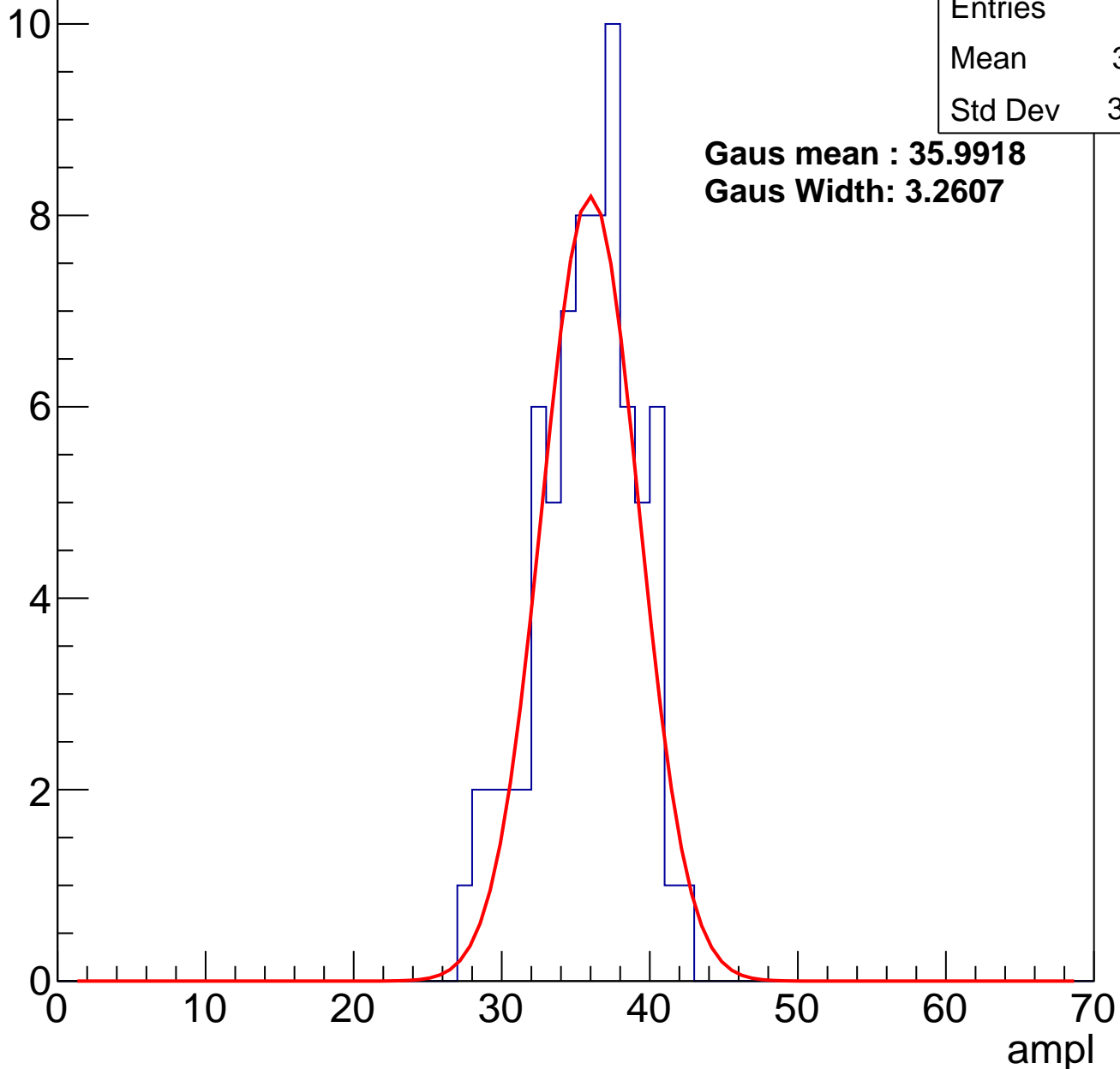
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	72
Mean	35.31
Std Dev	3.348

**Gaus mean : 35.9918**

**Gaus Width: 3.2607**

Entry



# B1L102S, U5-ch35, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	67
Mean	43.31
Std Dev	3.311

**Gaus mean : 43.7865**

**Gaus Width: 3.8902**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

0

2

4

6

8

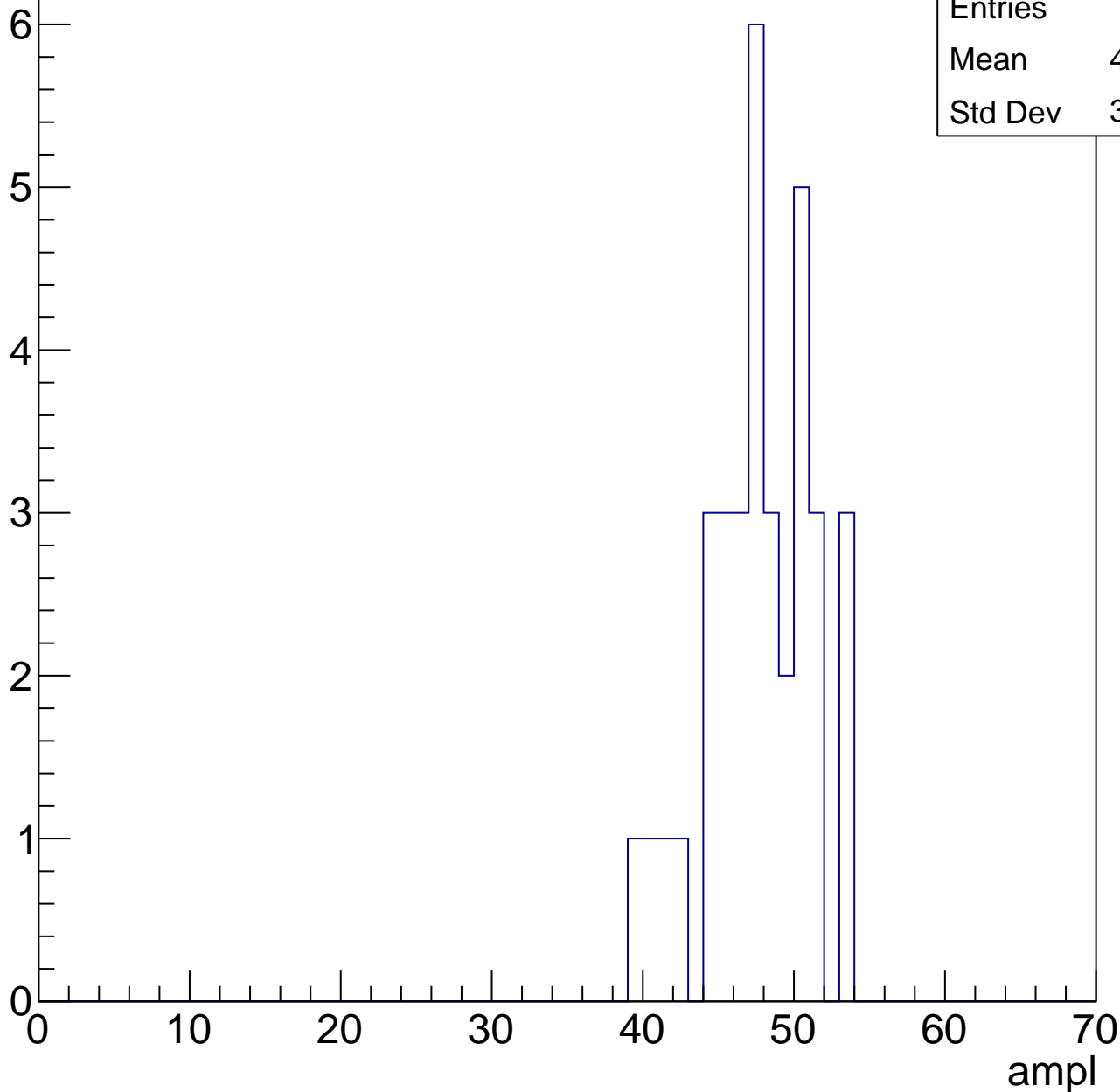
10

# B1L102S, U5-ch35, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	35
Mean	47.23
Std Dev	3.489

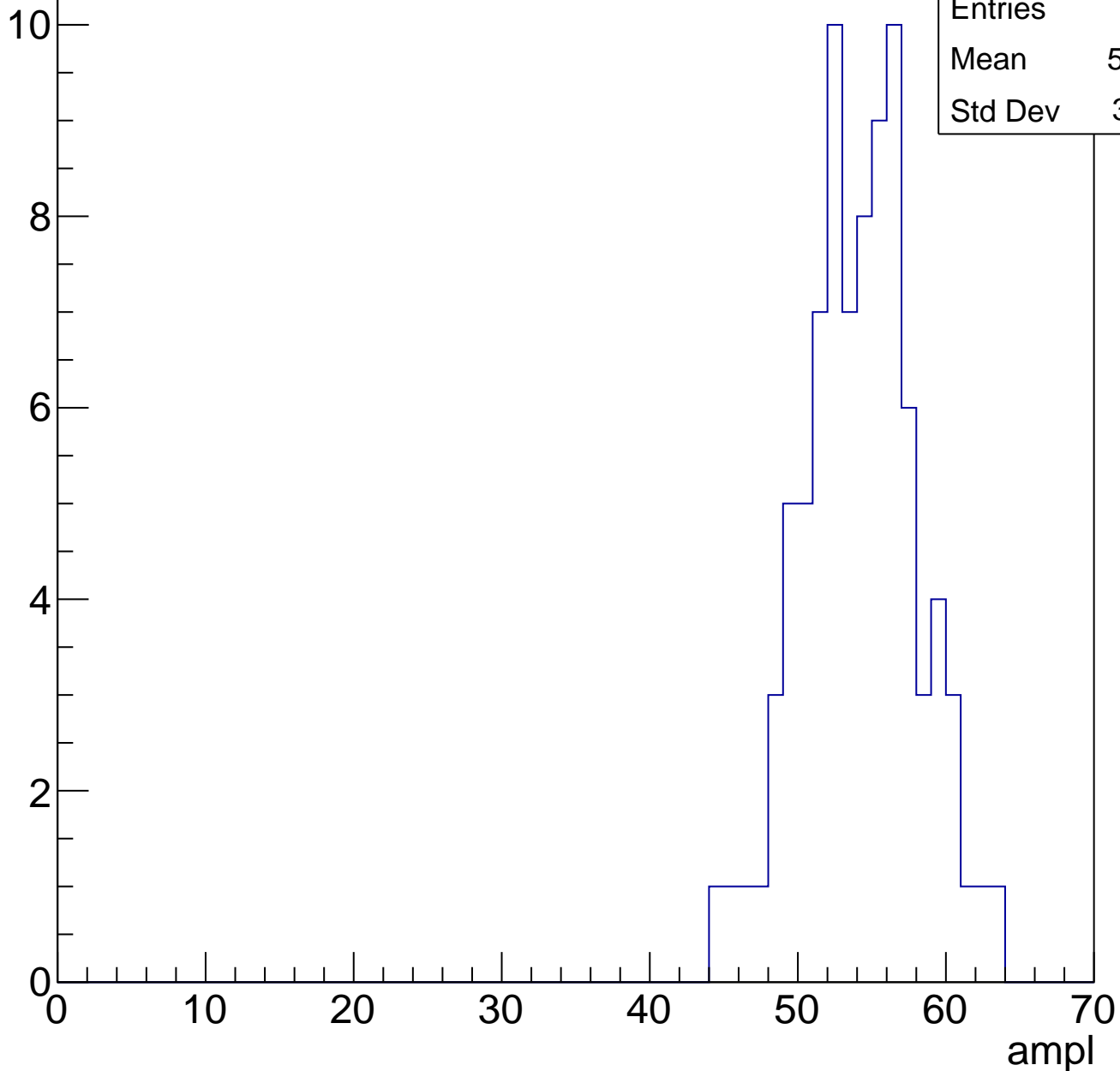


# B1L102S, U5-ch35, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	87
Mean	53.72
Std Dev	3.811

Entry

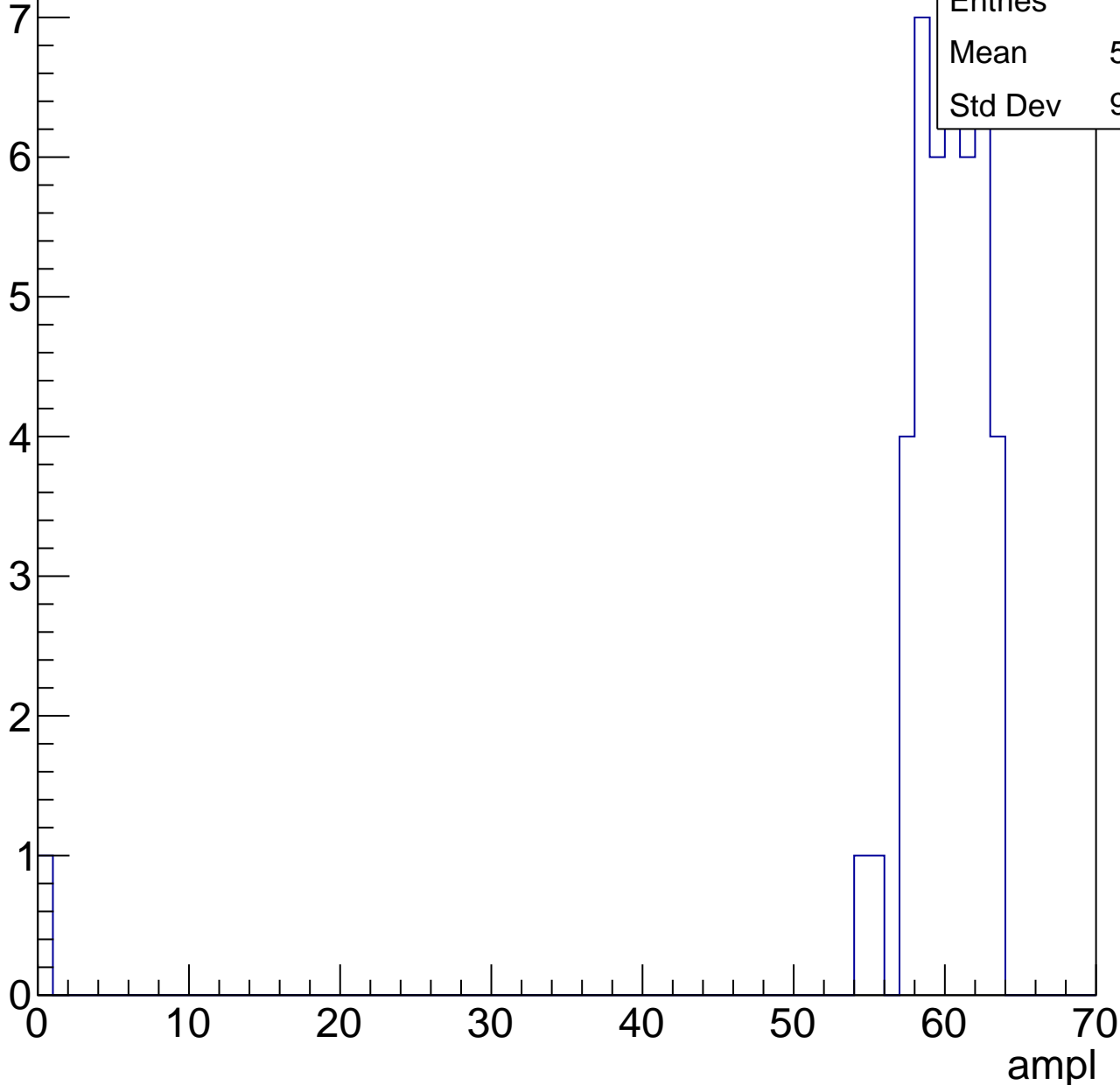


# B1L102S, U5-ch35, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	44
Mean	58.39
Std Dev	9.153

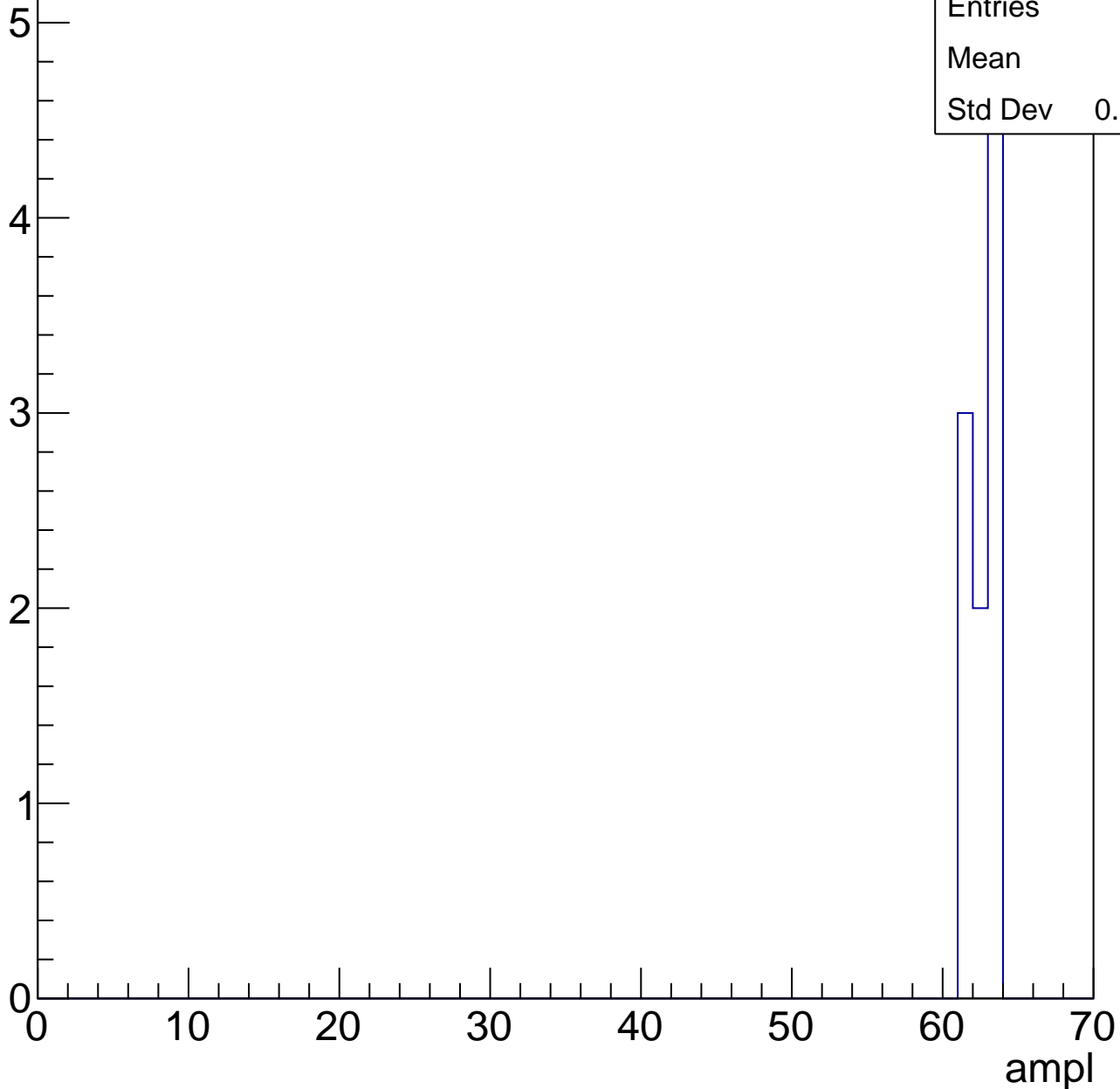


# B1L102S, U5-ch35, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	10
Mean	62.2
Std Dev	0.8718





# B1L102S, U5-ch35, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	20
Std Dev	0

ampl

# B1L102S, U5-ch36, adc0

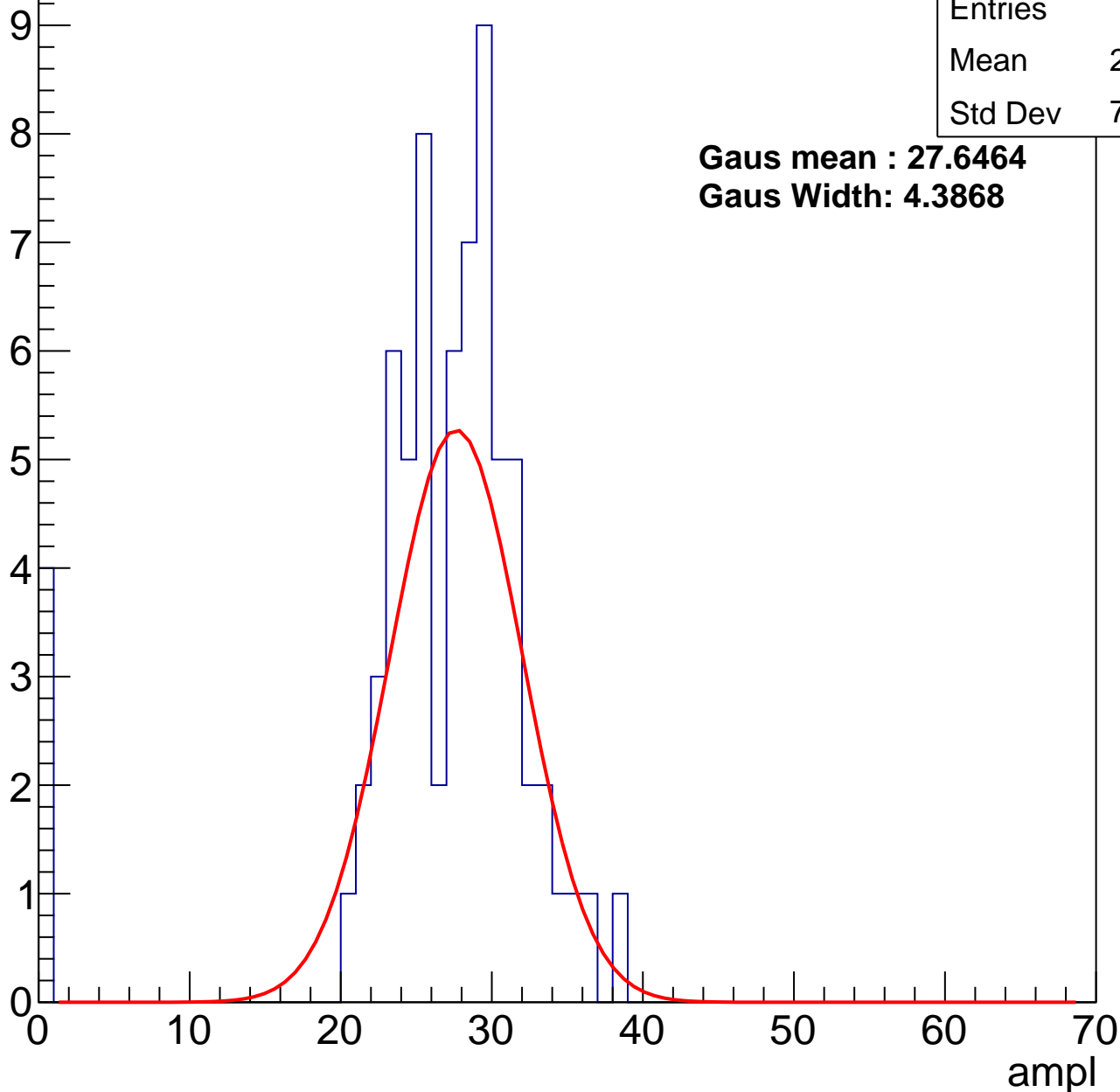
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	25.85
Std Dev	7.313

**Gaus mean : 27.6464**

**Gaus Width: 4.3868**



# B1L102S, U5-ch36, adc1

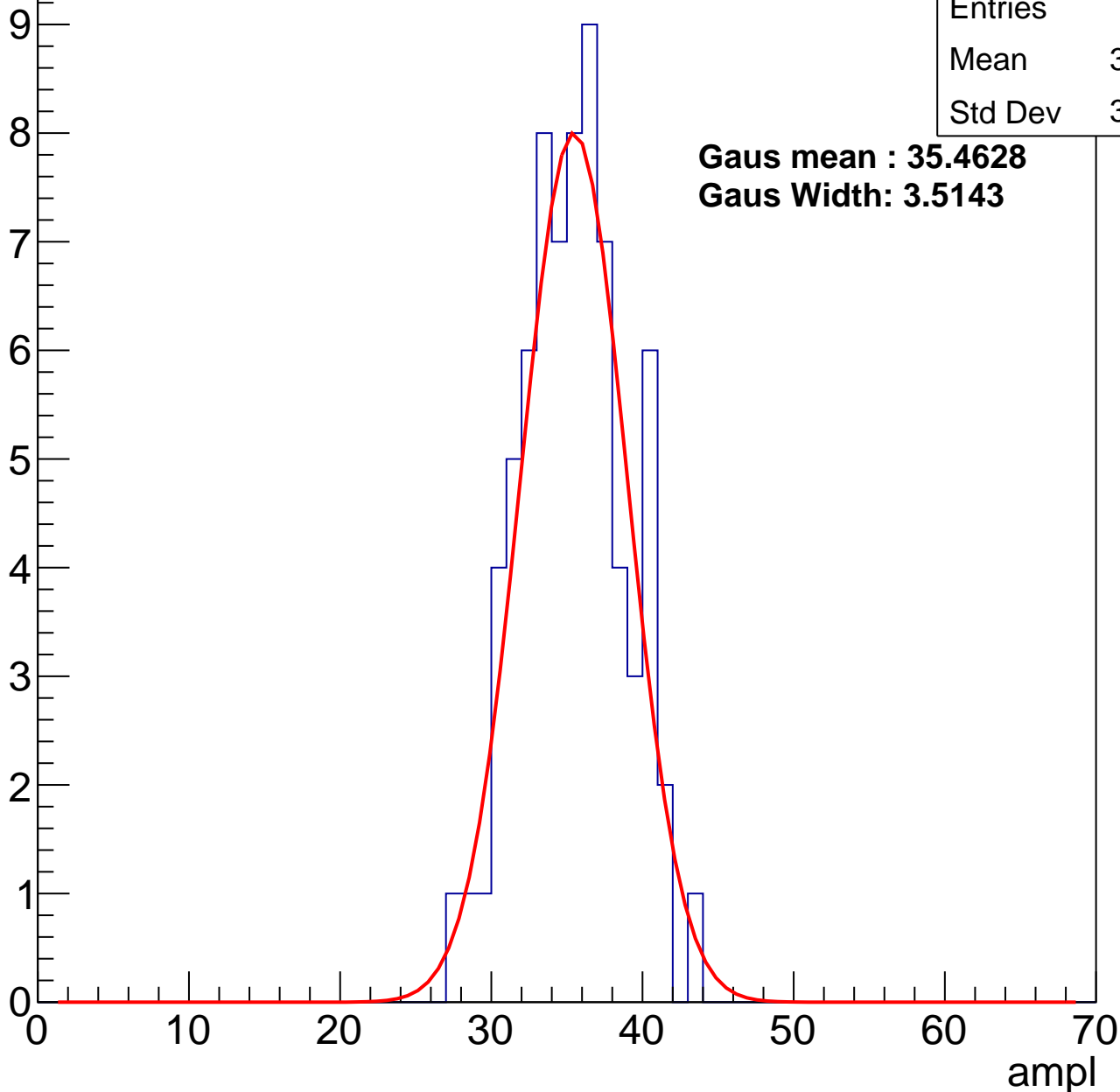
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	34.93
Std Dev	3.369

**Gaus mean : 35.4628**

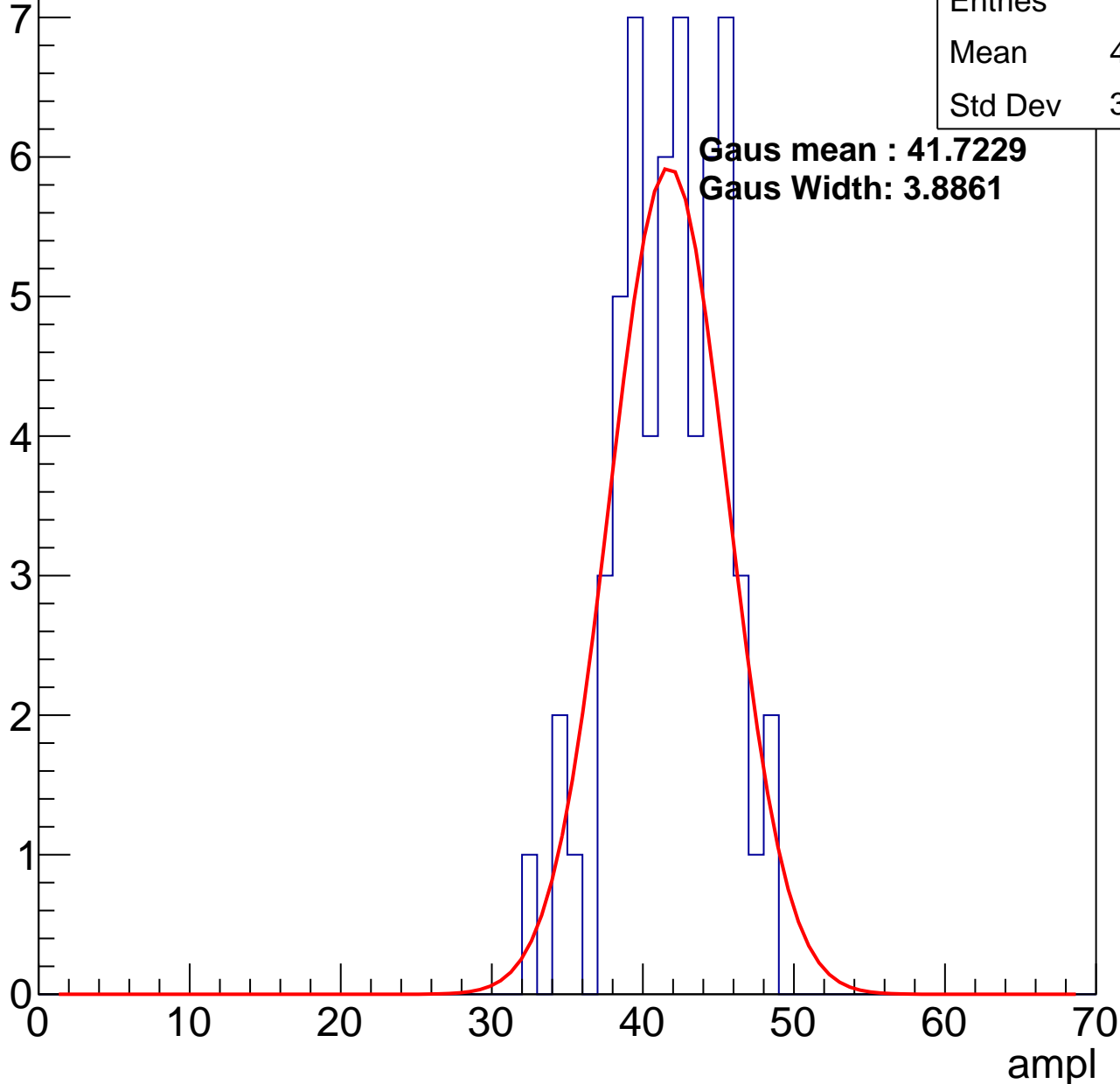
**Gaus Width: 3.5143**



# B1L102S, U5-ch36, adc2

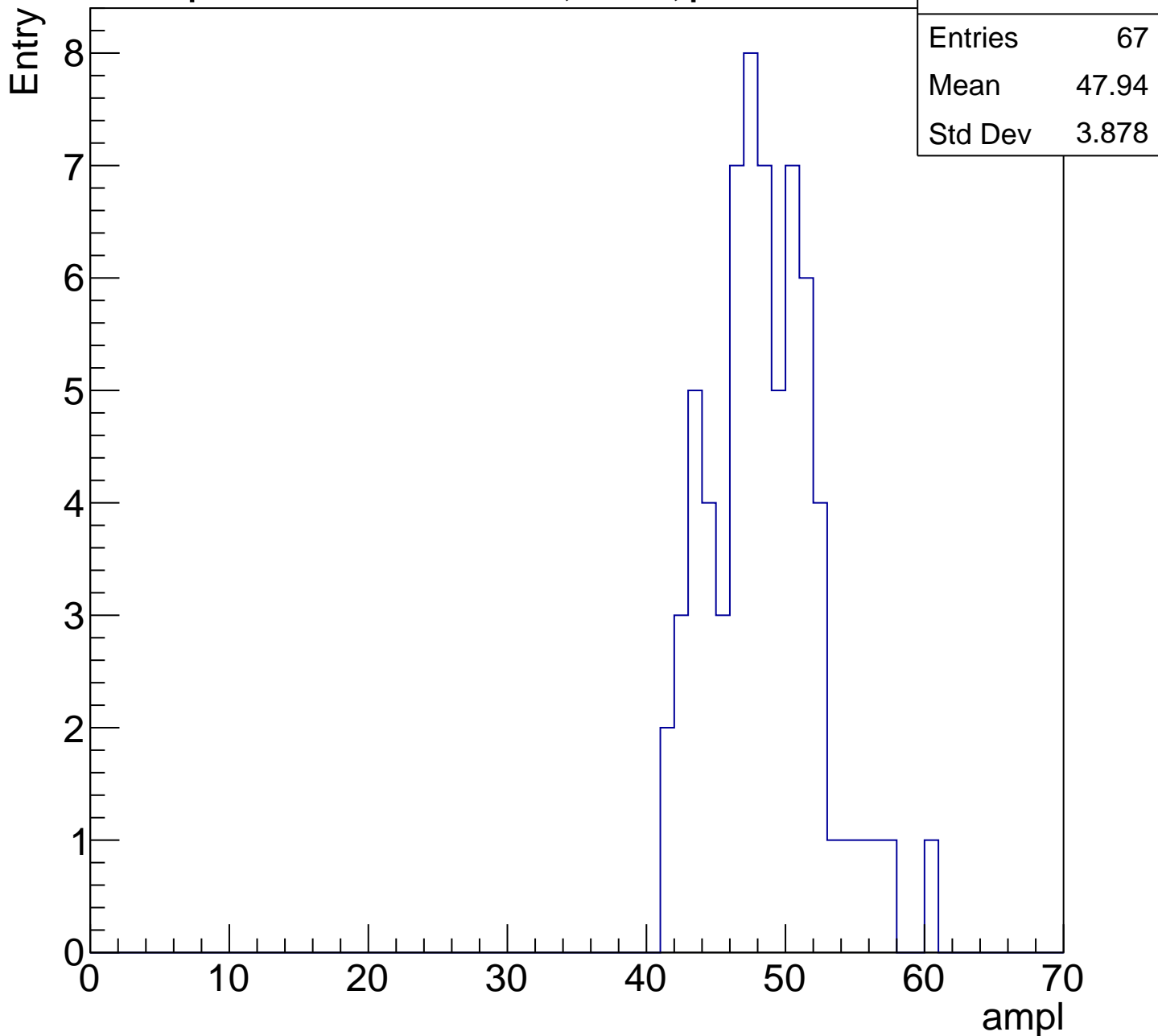
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



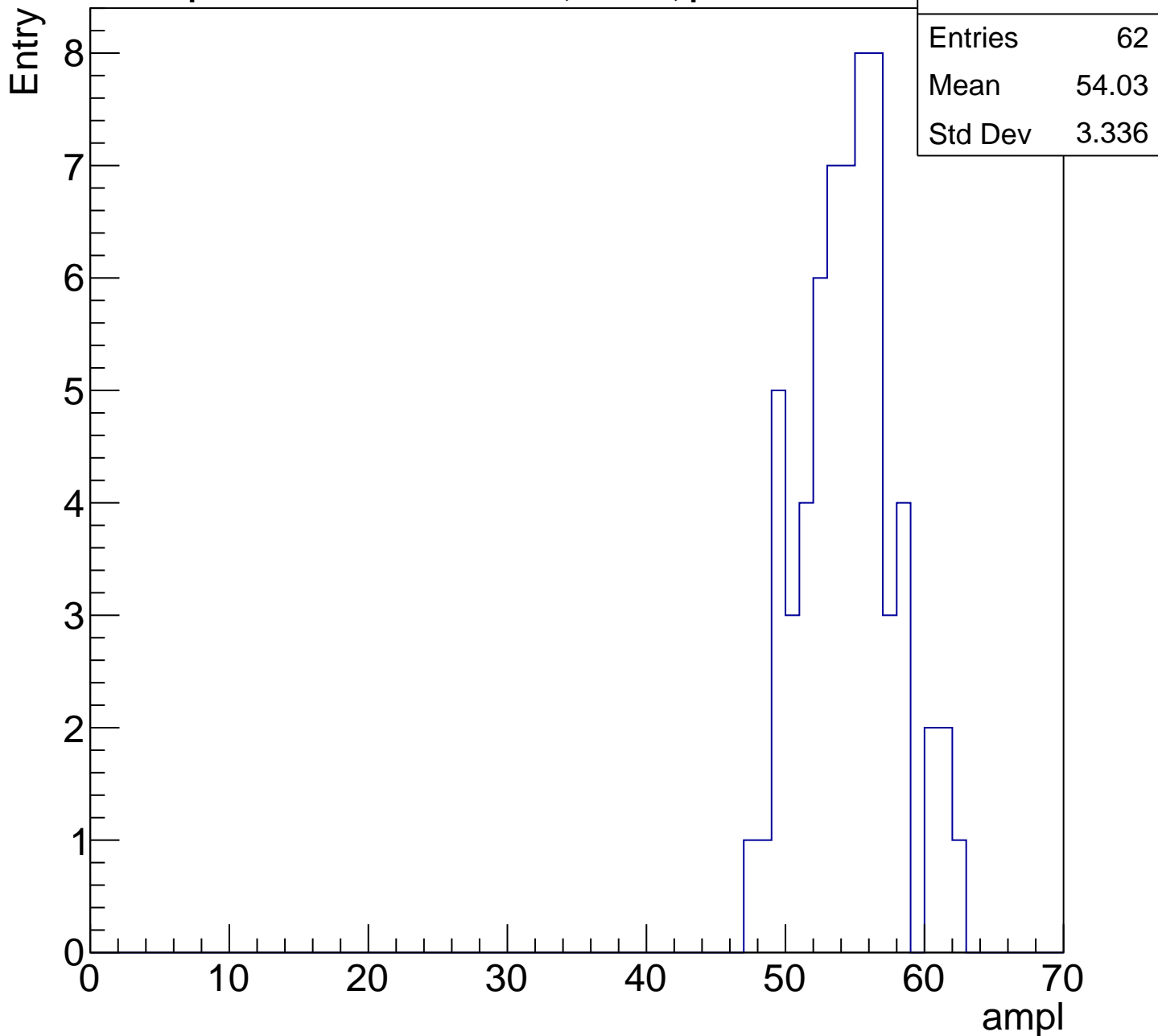
# B1L102S, U5-ch36, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2



# B1L102S, U5-ch36, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2



# B1L102S, U5-ch36, adc5

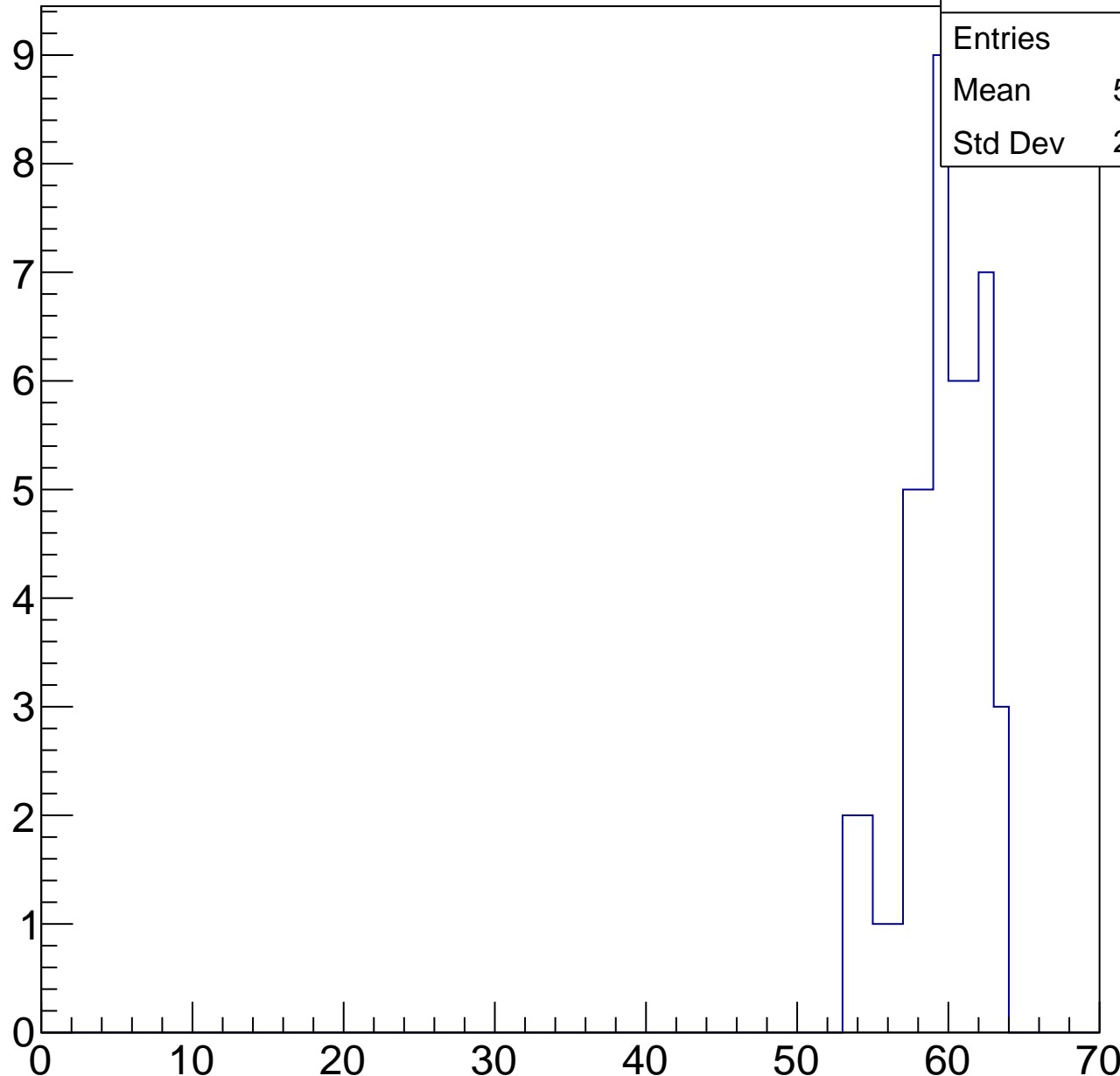
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	47
Mean	59.15
Std Dev	2.576

ampl

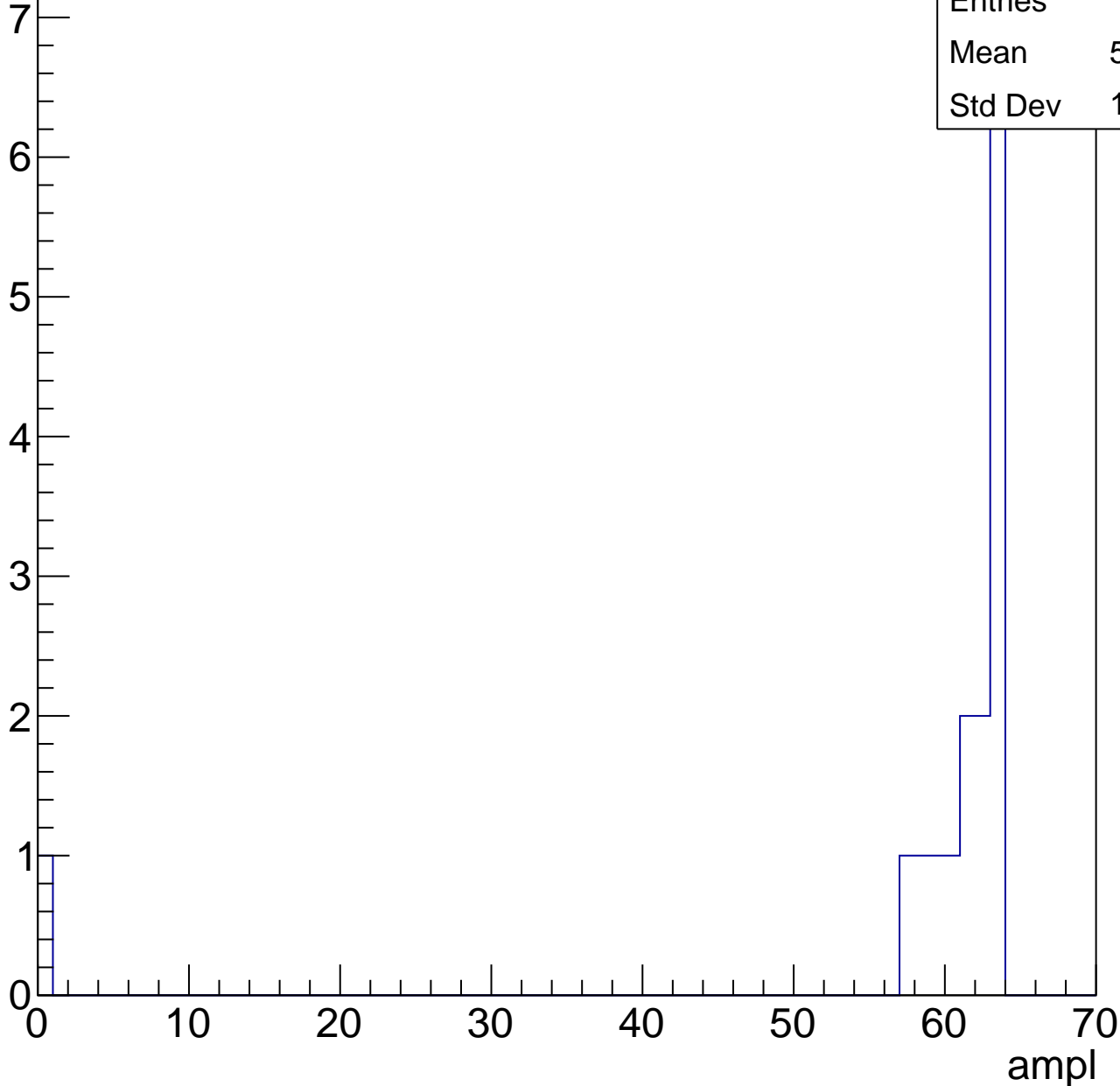


# B1L102S, U5-ch36, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	16
Mean	57.56
Std Dev	14.98





# B1L102S, U5-ch36, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L102S, U5-ch37, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	74
Mean	28.3
Std Dev	3.303

**Gaus mean : 28.4890**

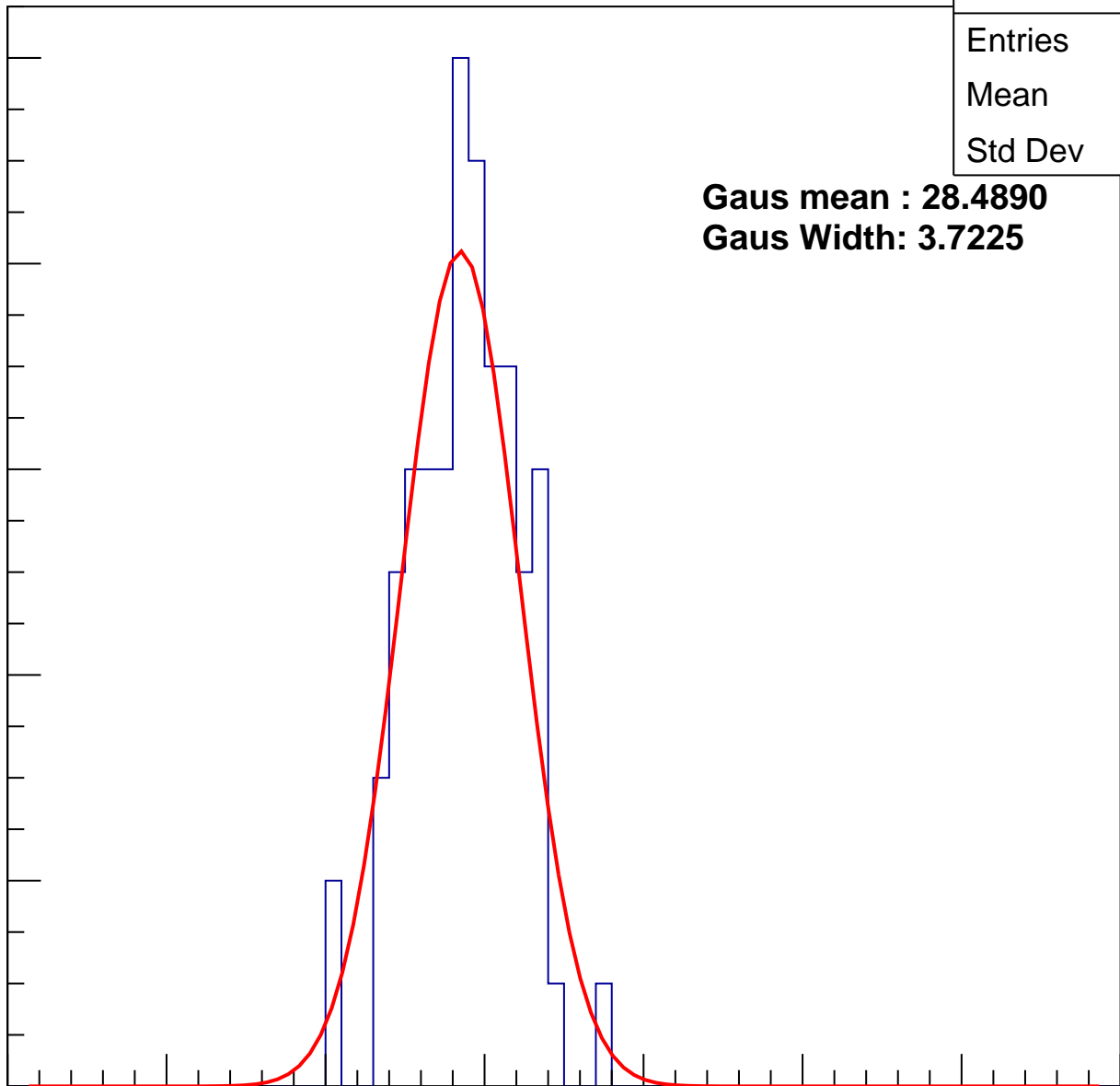
**Gaus Width: 3.7225**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U5-ch37, adc1

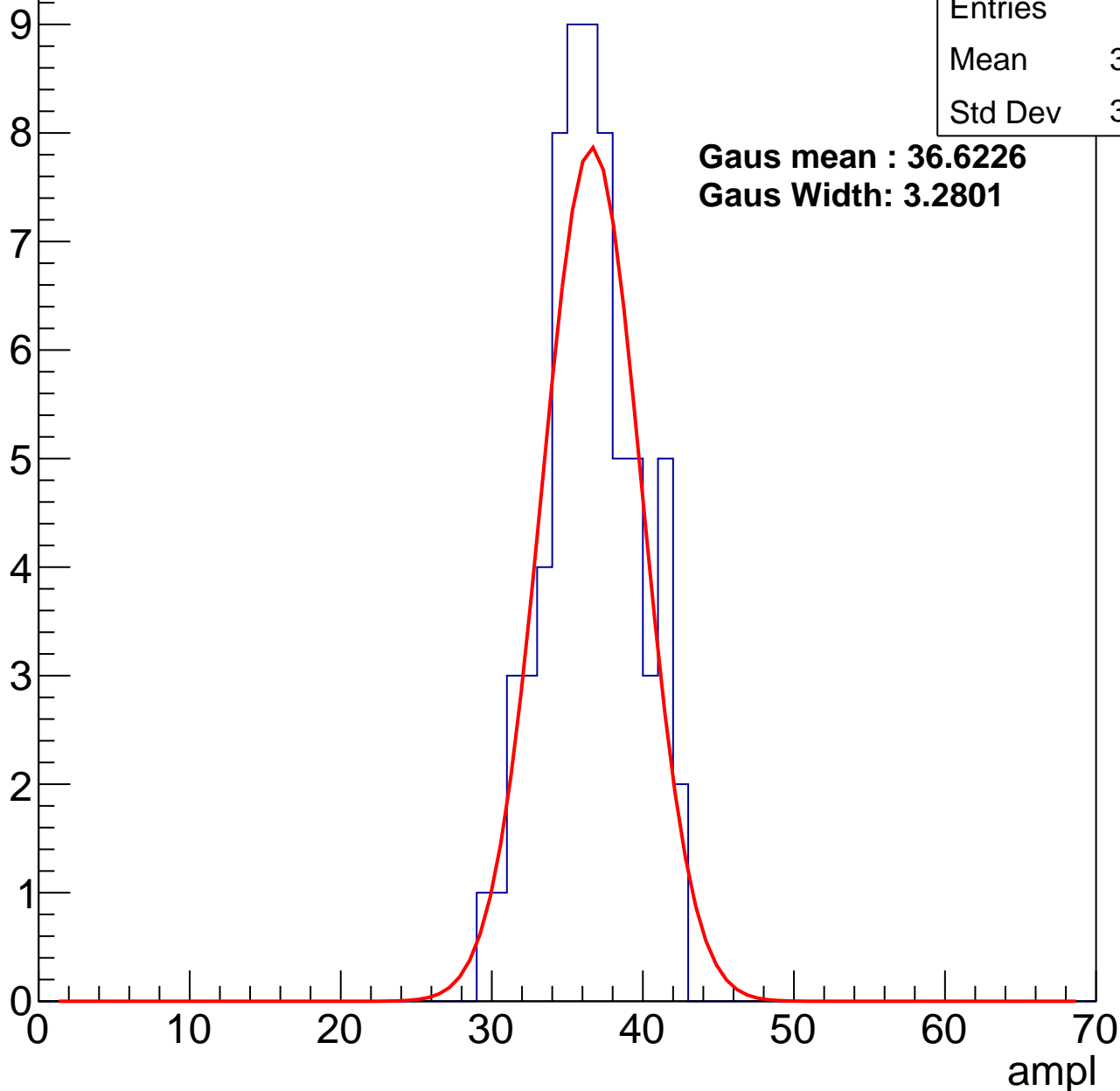
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	36.08
Std Dev	3.022

**Gaus mean : 36.6226**

**Gaus Width: 3.2801**



# B1L102S, U5-ch37, adc2

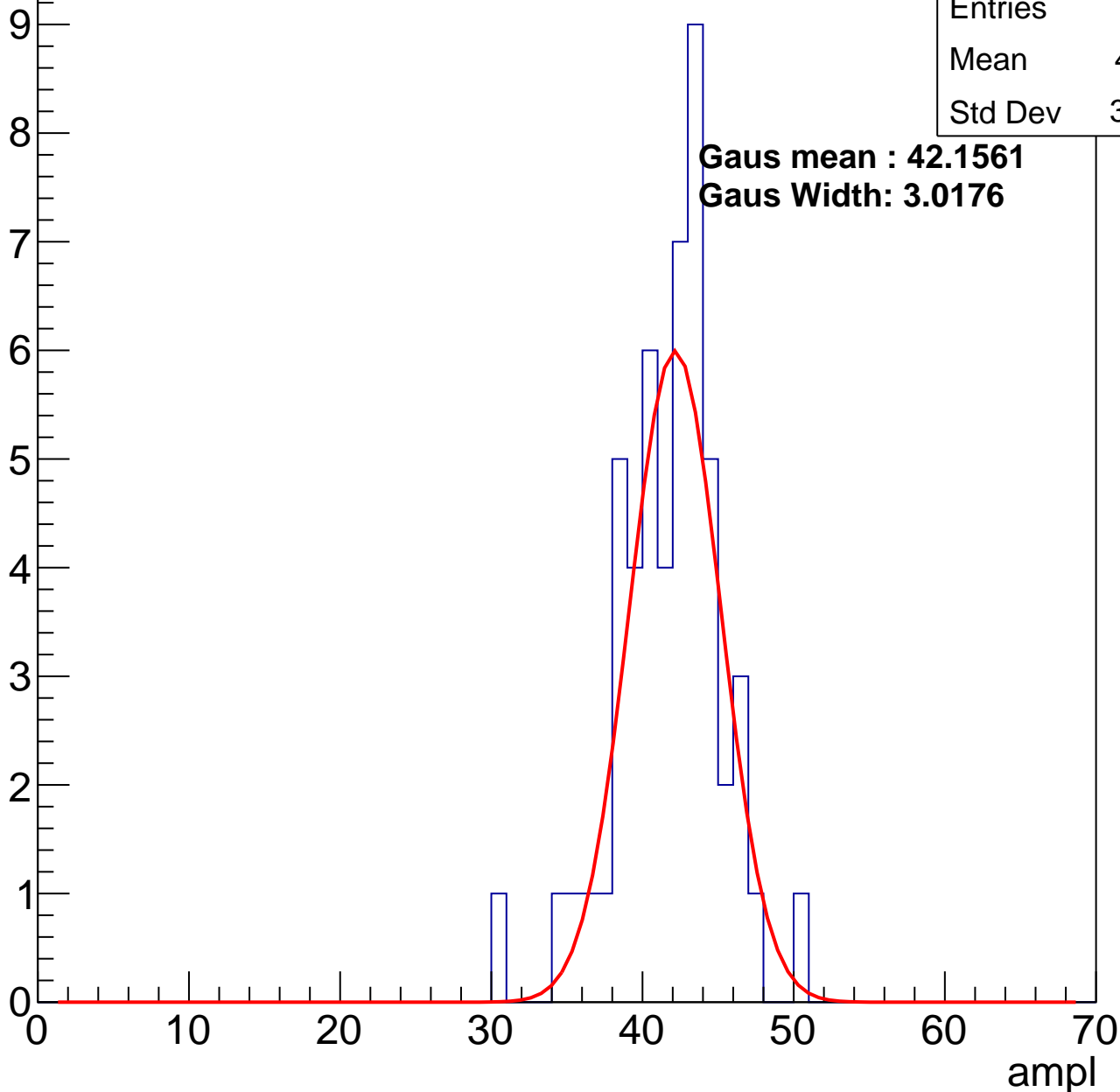
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	41.31
Std Dev	3.456

**Gaus mean : 42.1561**

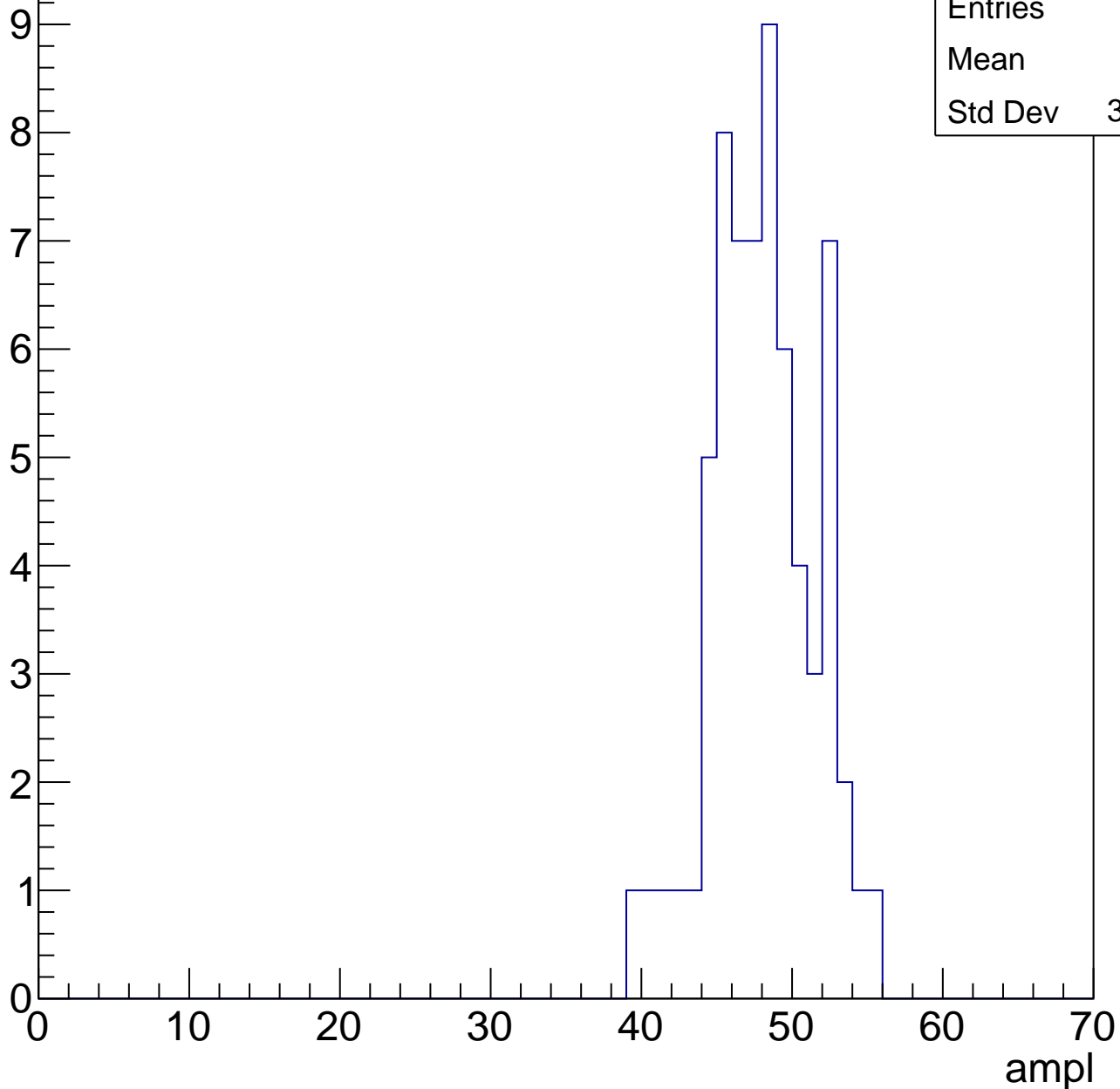
**Gaus Width: 3.0176**



# B1L102S, U5-ch37, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



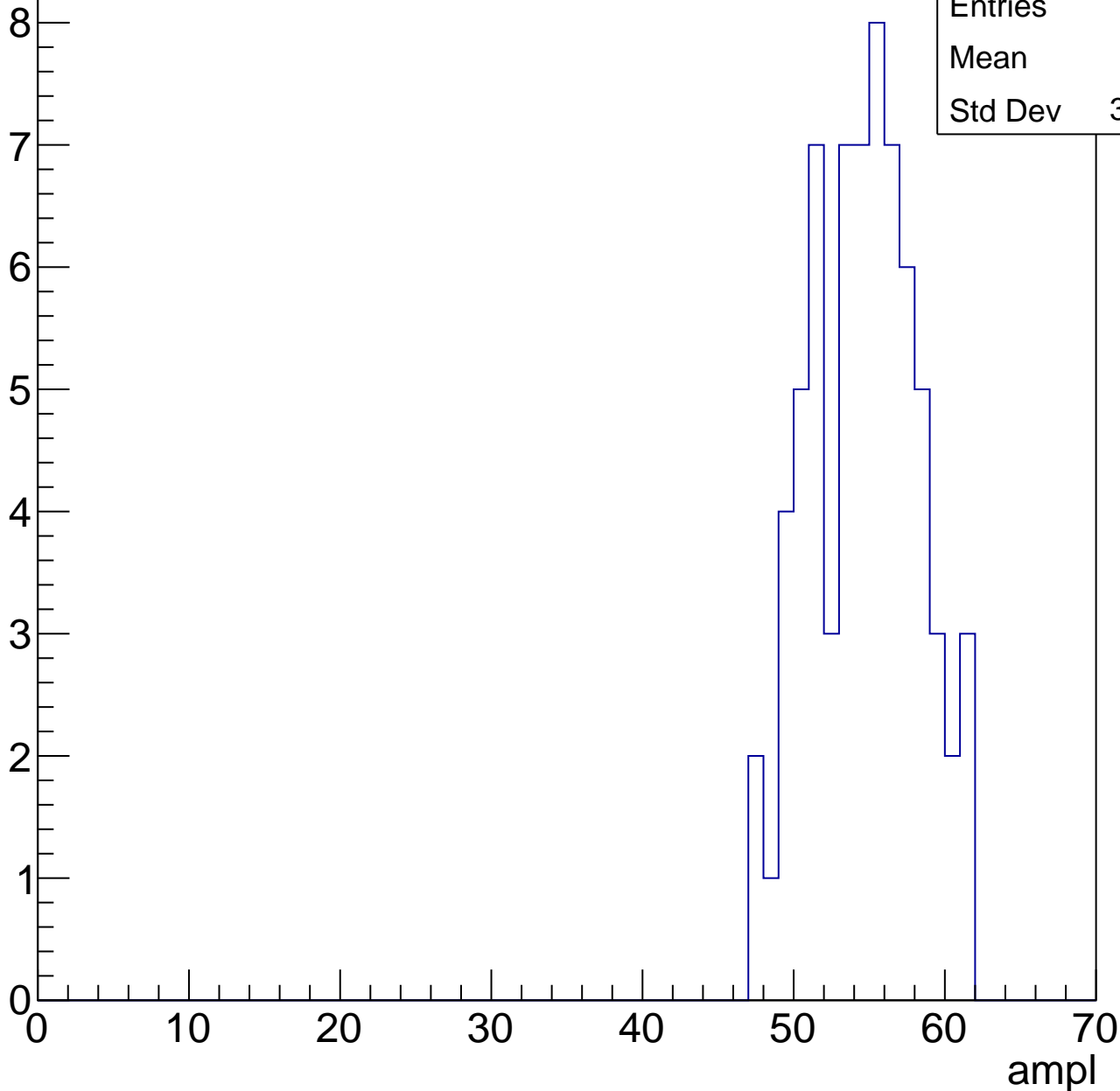
Entries	65
Mean	47.6
Std Dev	3.346

# B1L102S, U5-ch37, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	54.2
Std Dev	3.499



# B1L102S, U5-ch37, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	48
Mean	59.69
Std Dev	2.631

ampl

0 10 20 30 40 50 60 70

0

1

2

3

4

5

6

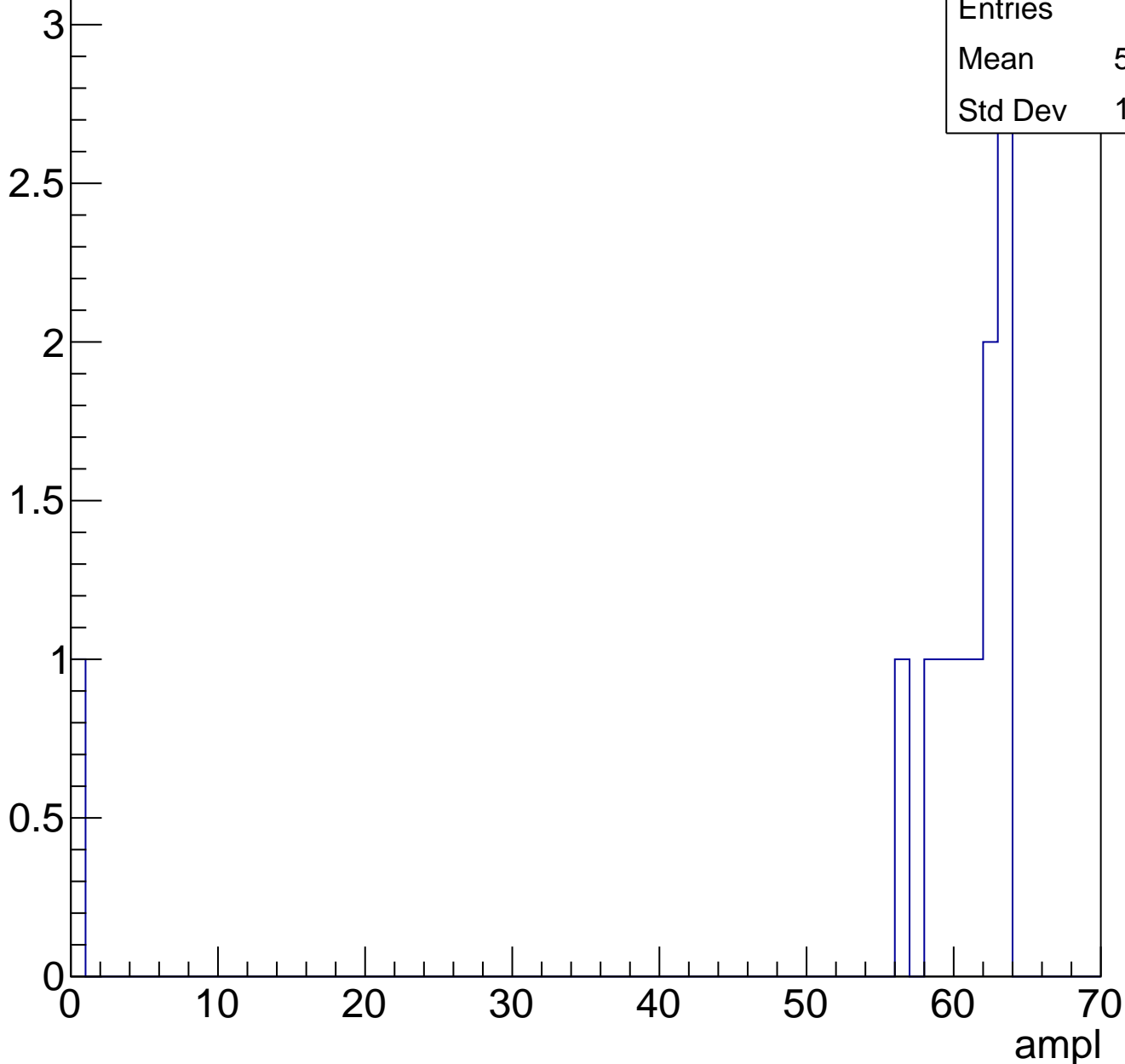
7

8

# B1L102S, U5-ch37, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U5-ch37, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U5-ch38, adc0

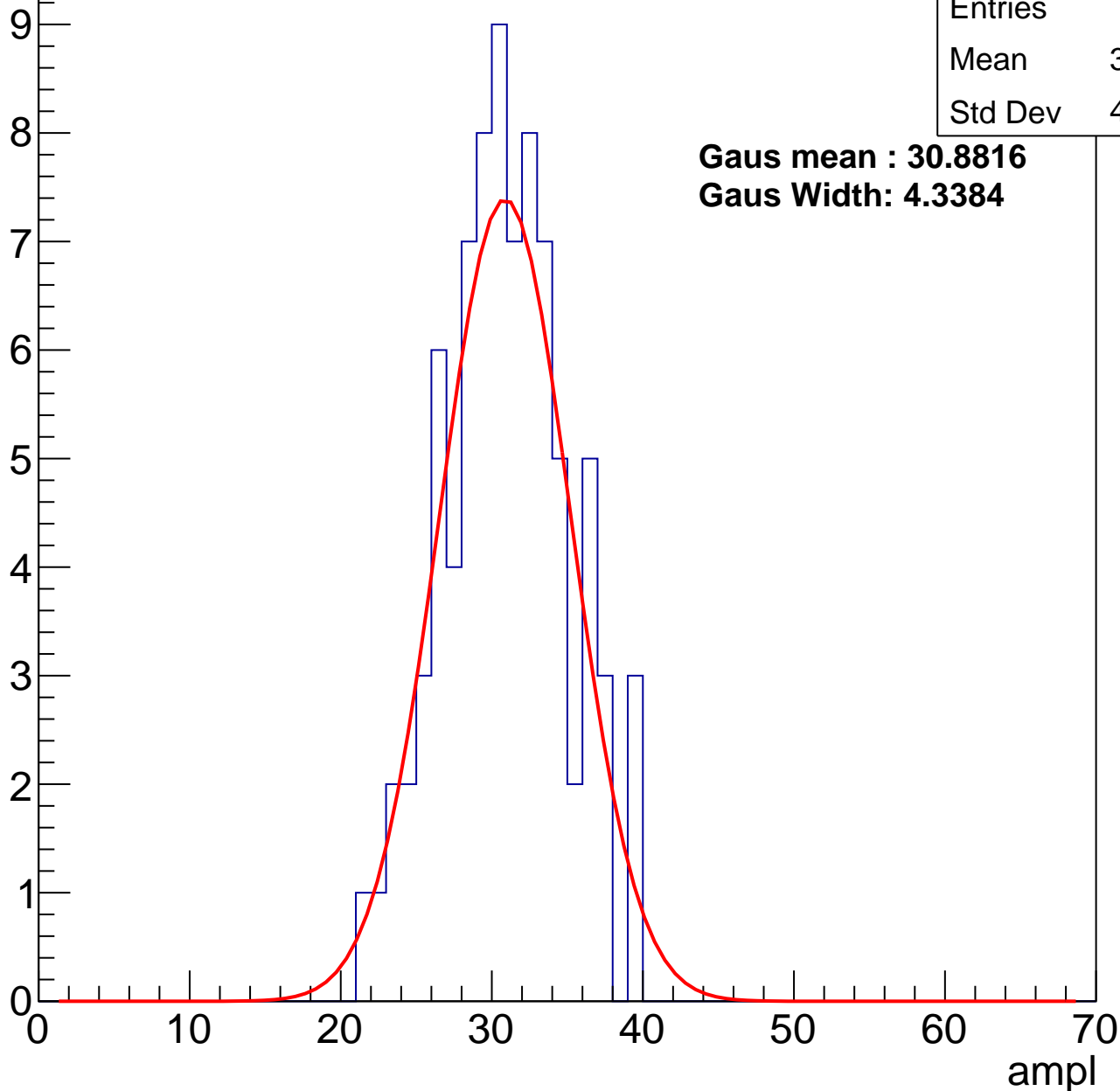
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	83
Mean	30.43
Std Dev	4.025

**Gaus mean : 30.8816**

**Gaus Width: 4.3384**



# B1L102S, U5-ch38, adc1

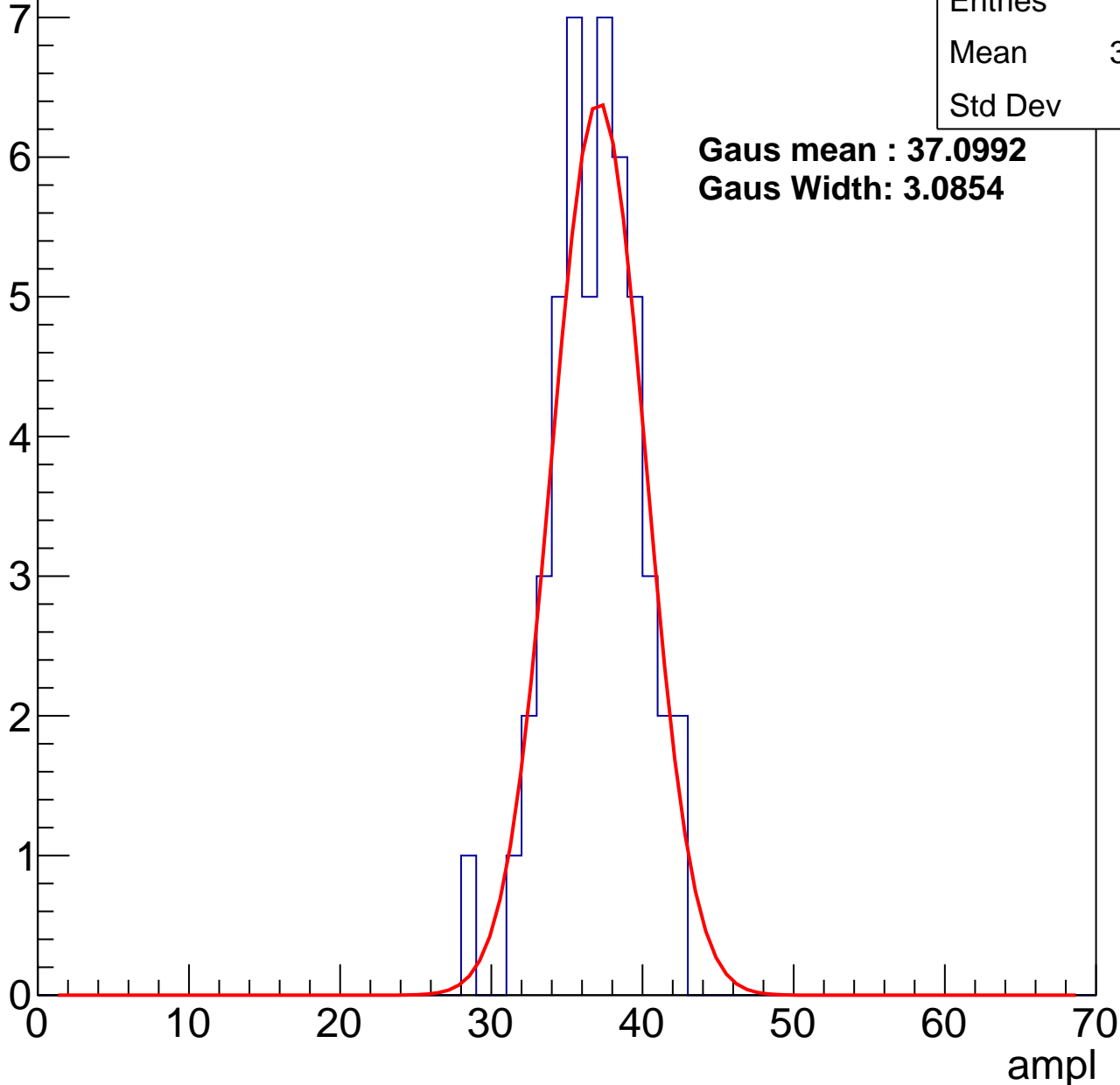
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	36.43
Std Dev	2.9

**Gaus mean : 37.0992**

**Gaus Width: 3.0854**



# B1L102S, U5-ch38, adc2

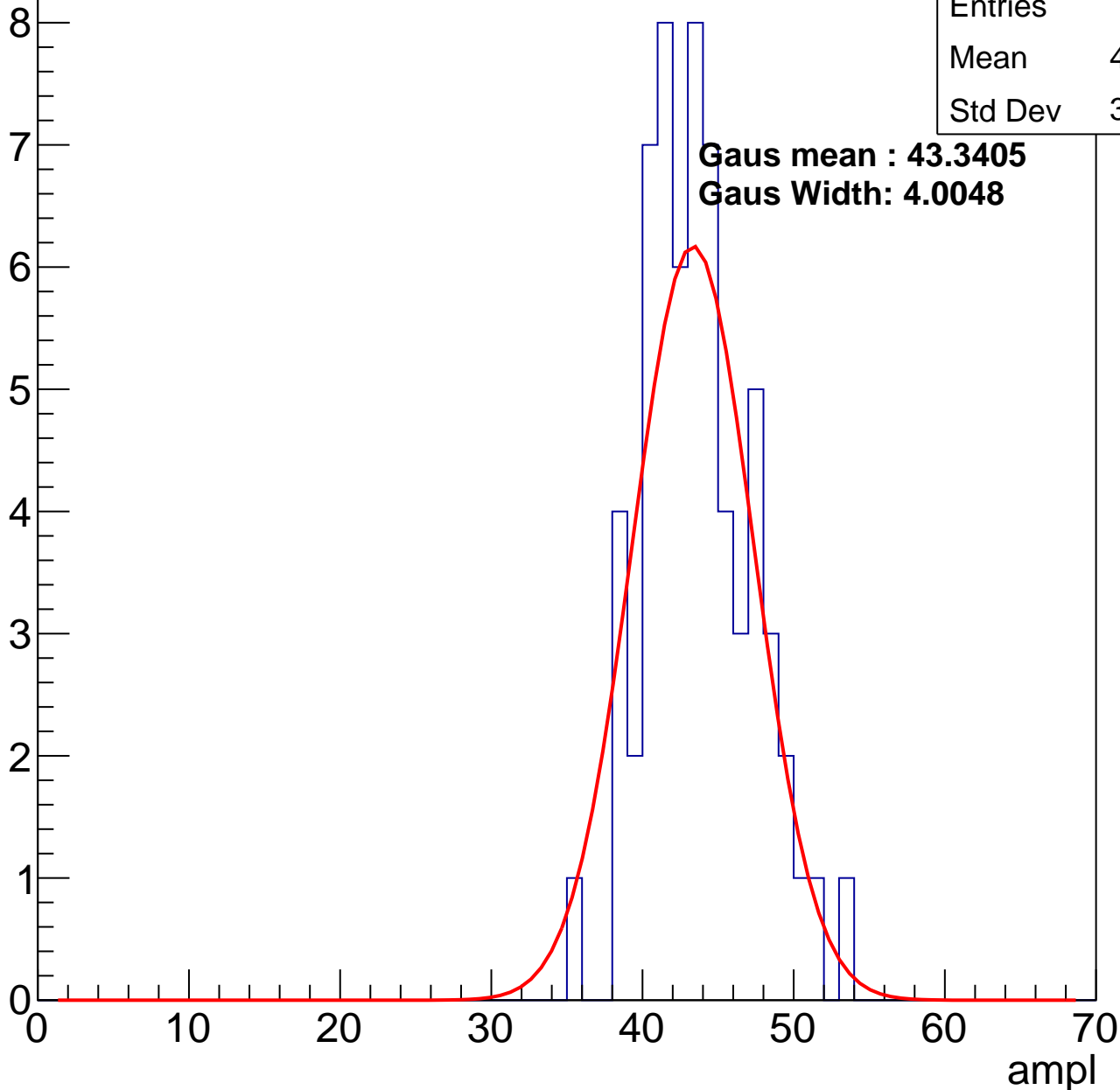
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	43.27
Std Dev	3.524

**Gaus mean : 43.3405**

**Gaus Width: 4.0048**

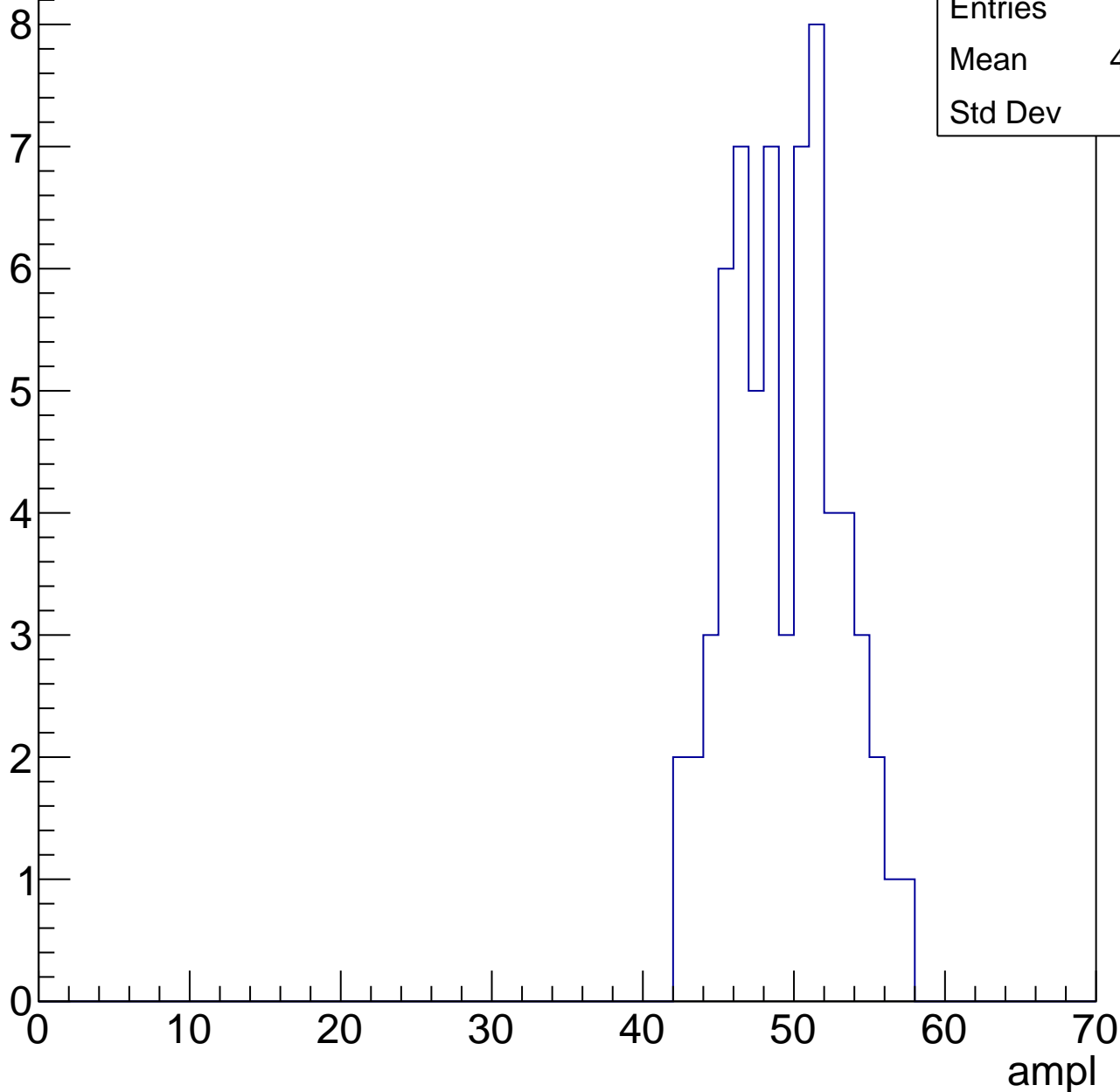


# B1L102S, U5-ch38, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	48.85
Std Dev	3.57

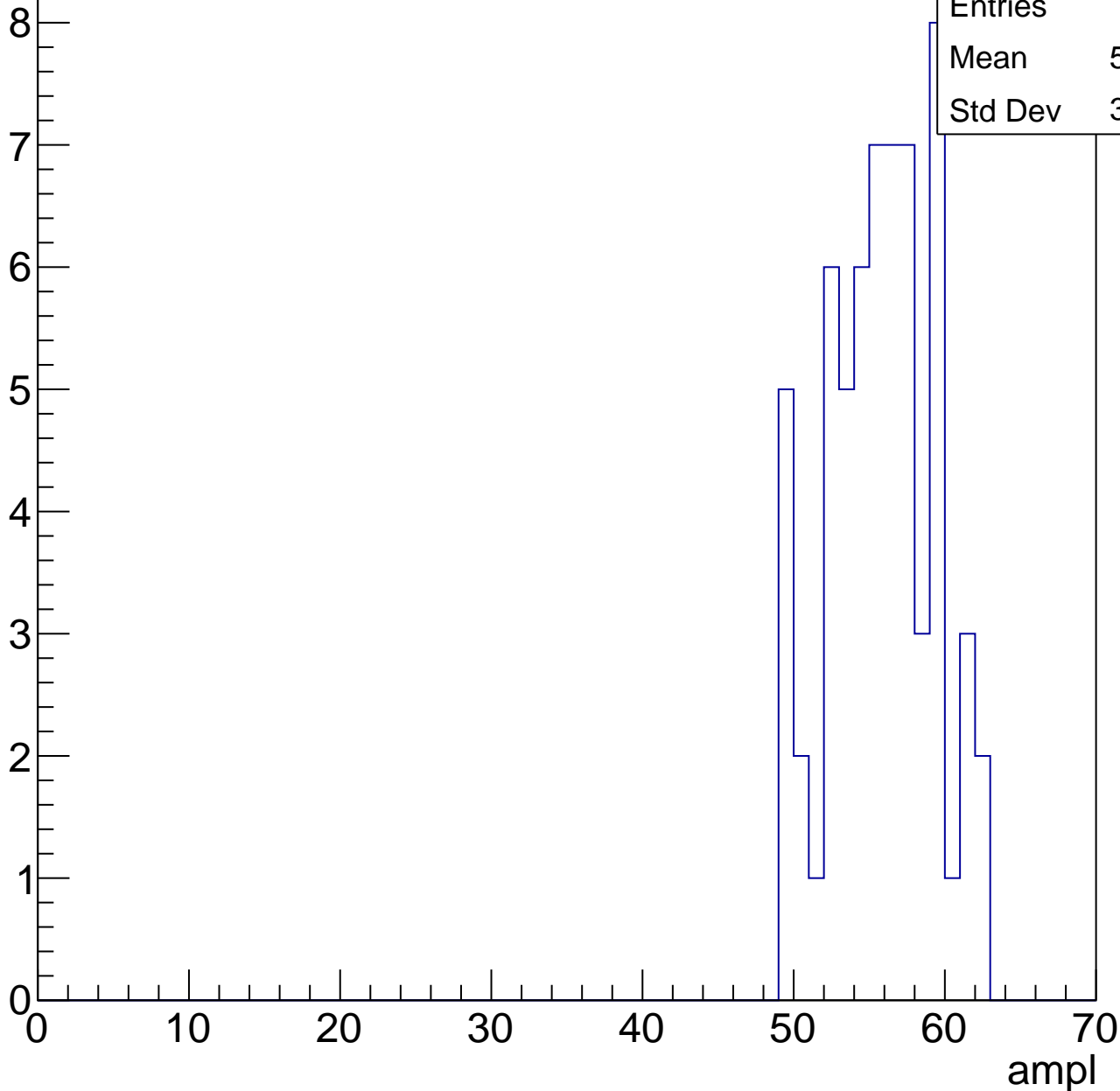


# B1L102S, U5-ch38, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	55.33
Std Dev	3.427

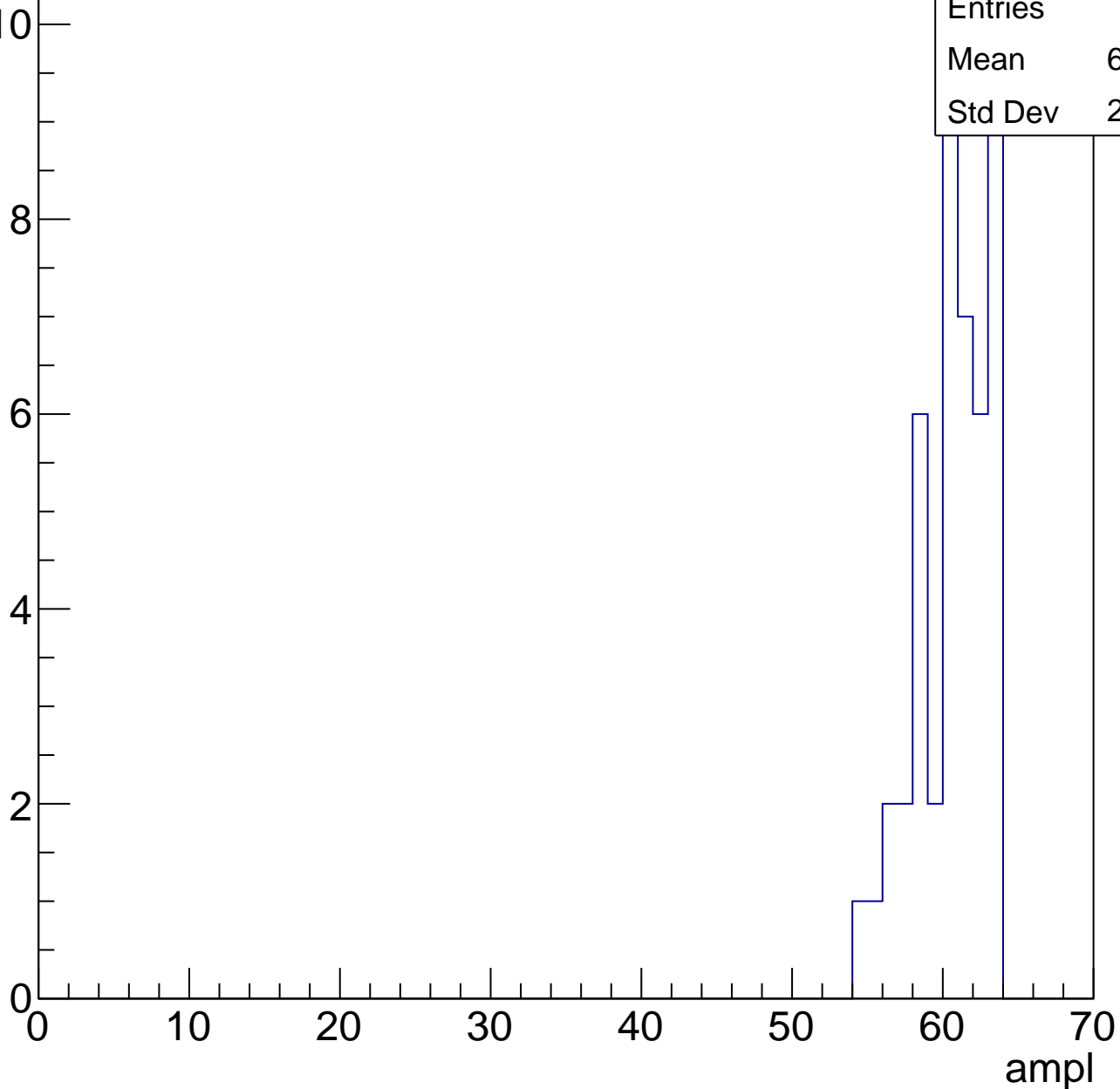


# B1L102S, U5-ch38, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

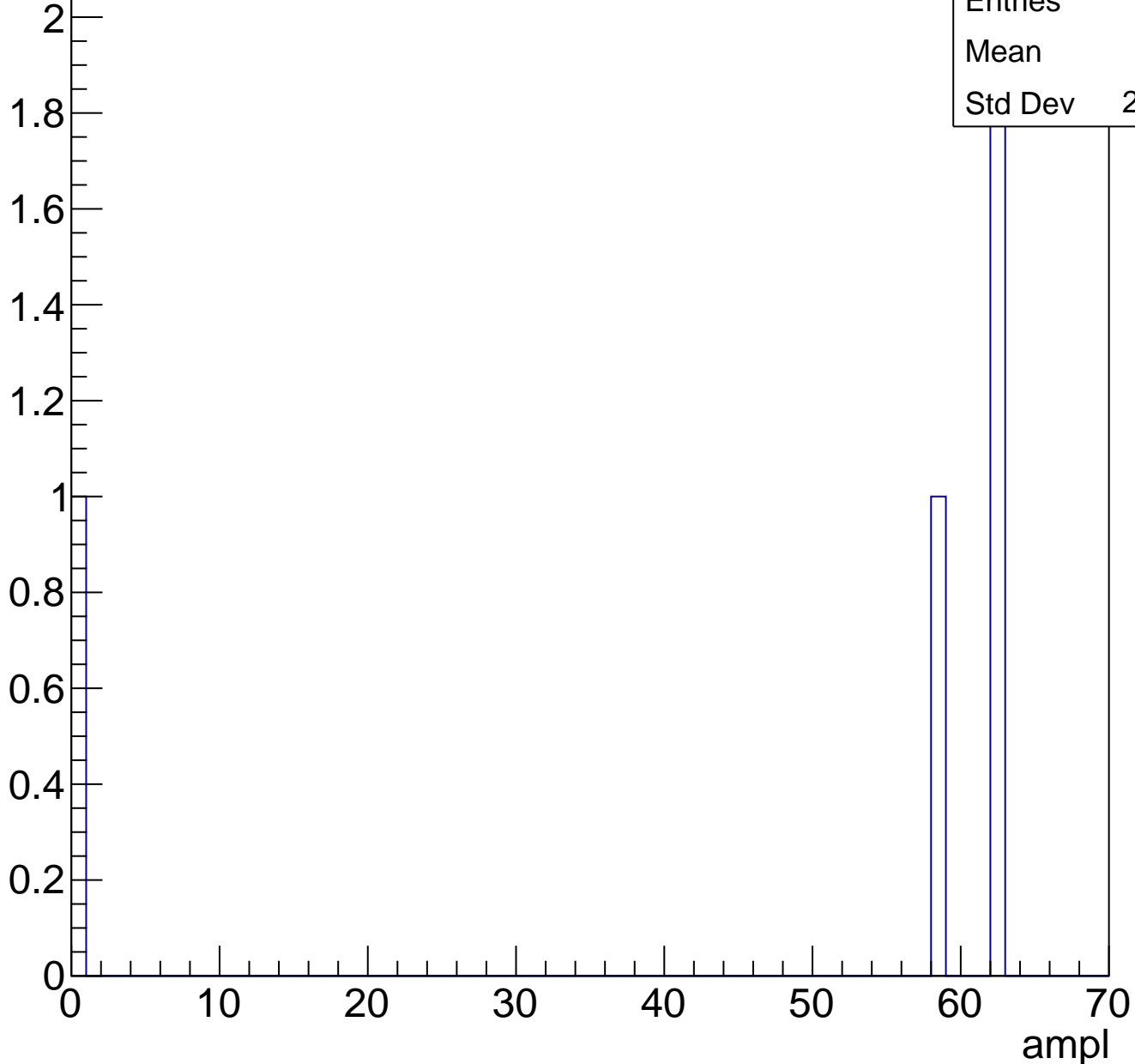
Entries	46
Mean	60.22
Std Dev	2.358



# B1L102S, U5-ch38, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	4
Mean	45.5
Std Dev	26.32



# B1L102S, U5-ch38, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U5-ch39, adc0

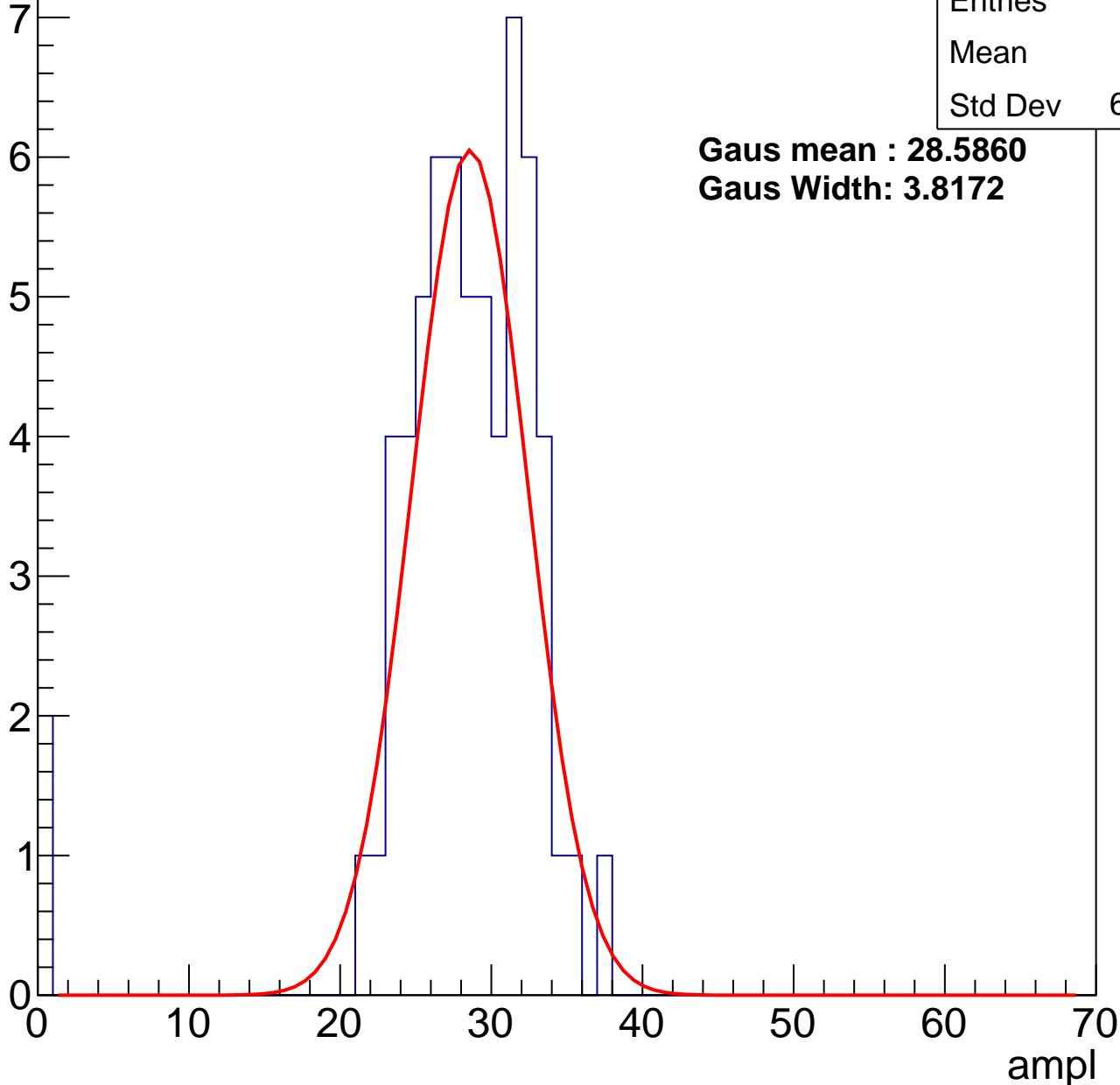
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	27.4
Std Dev	6.062

**Gaus mean : 28.5860**

**Gaus Width: 3.8172**



# B1L102S, U5-ch39, adc1

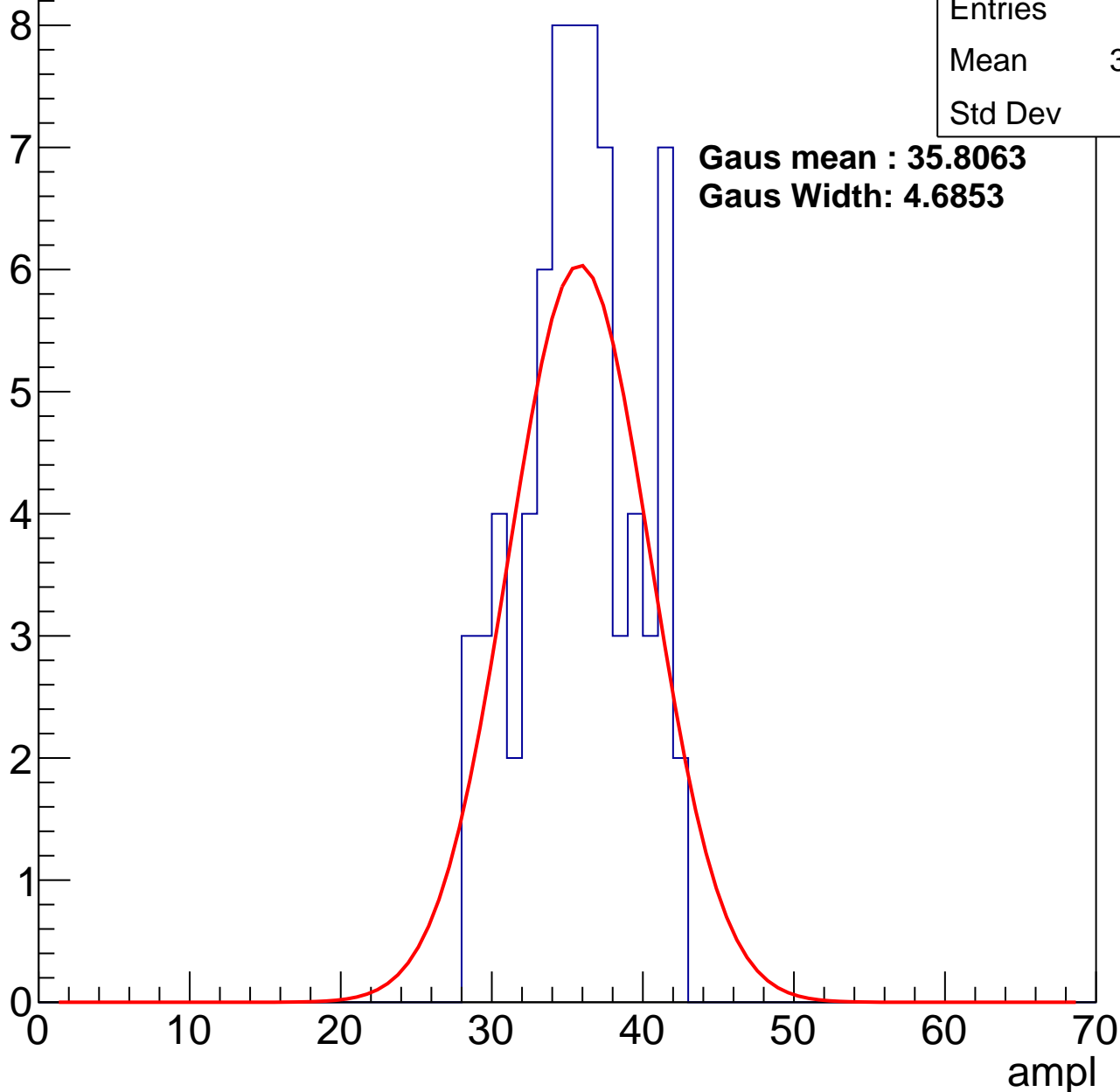
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	35.26
Std Dev	3.73

**Gaus mean : 35.8063**

**Gaus Width: 4.6853**



# B1L102S, U5-ch39, adc2

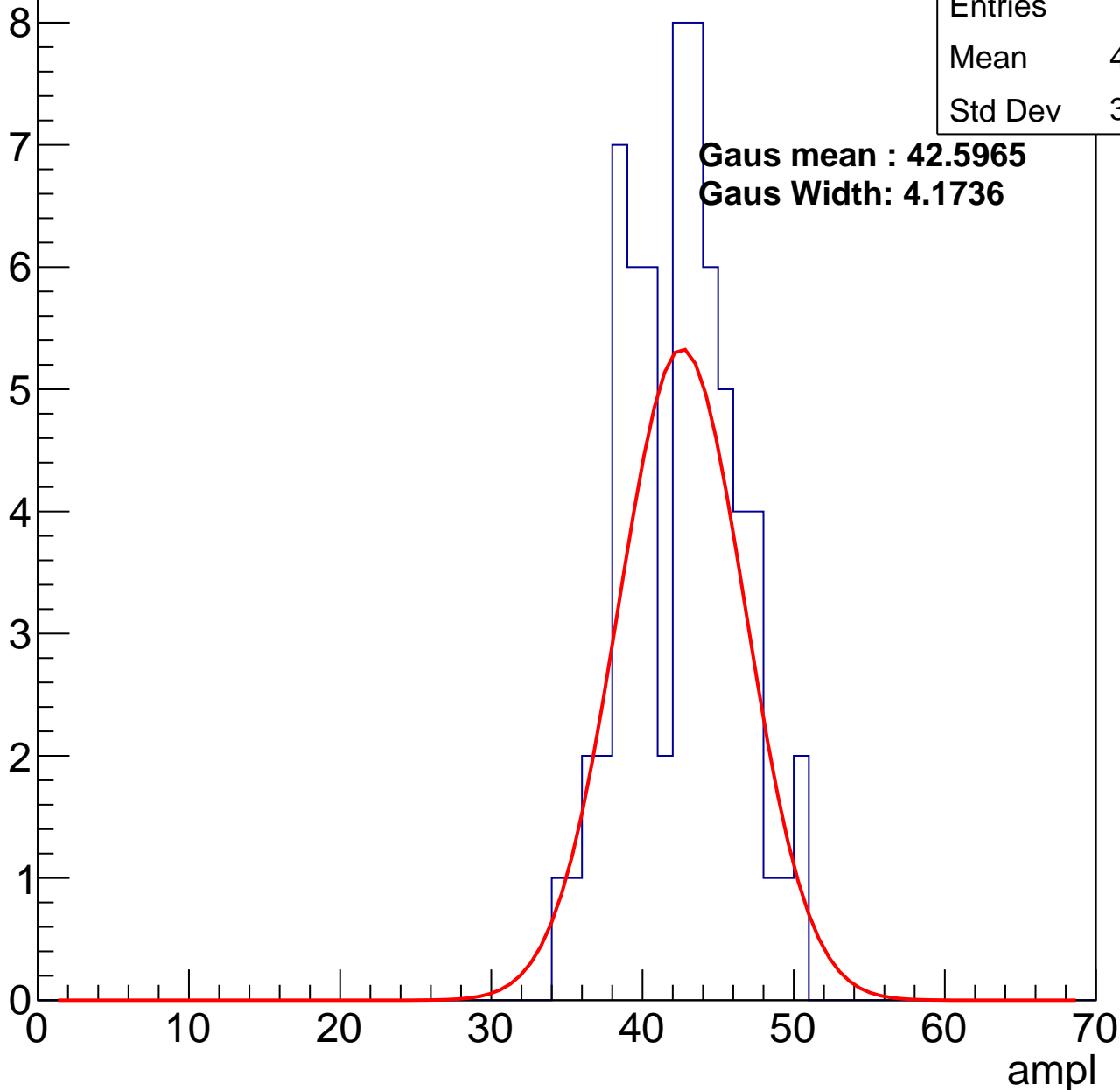
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	42.05
Std Dev	3.653

**Gaus mean : 42.5965**

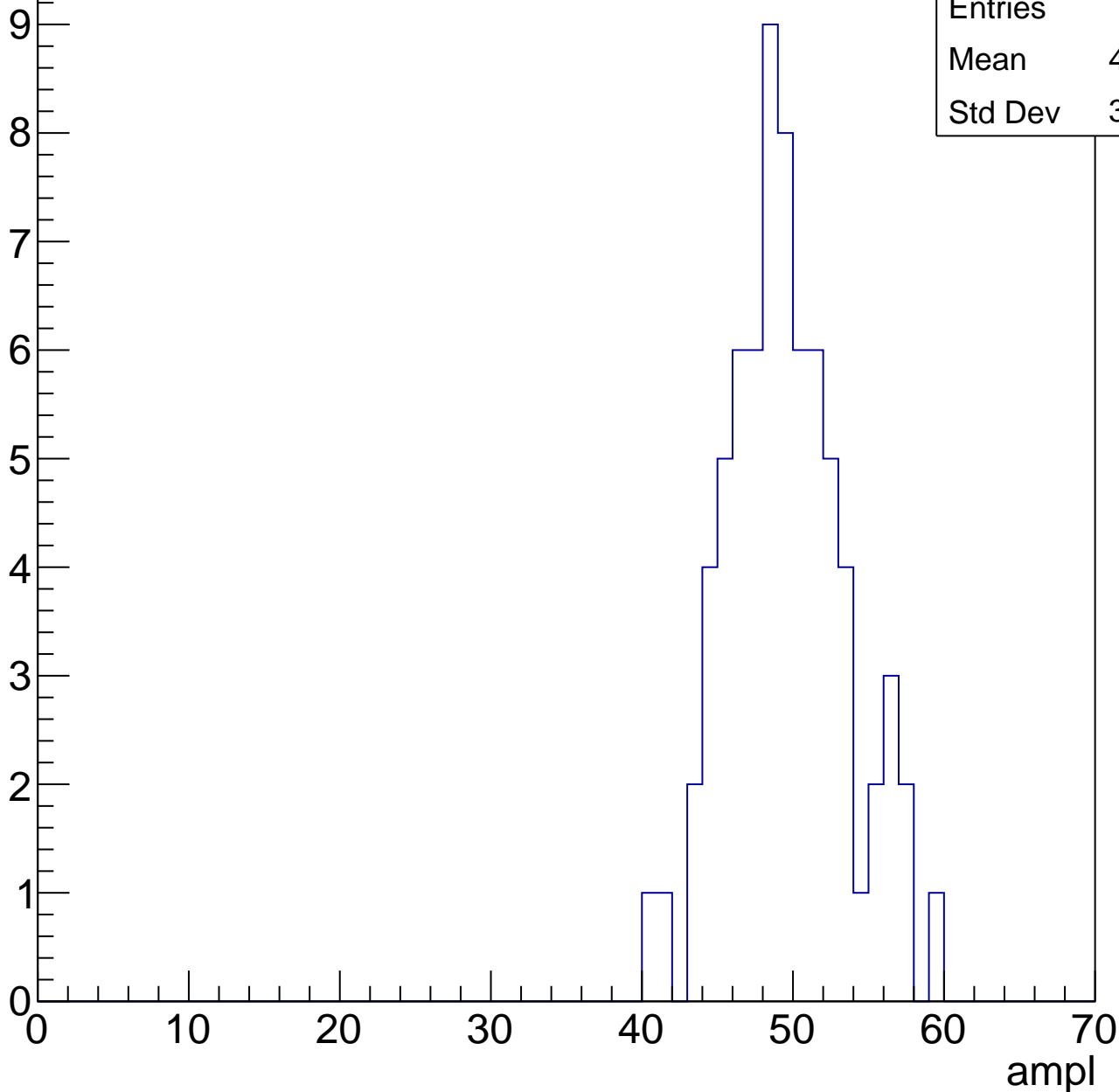
**Gaus Width: 4.1736**



# B1L102S, U5-ch39, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

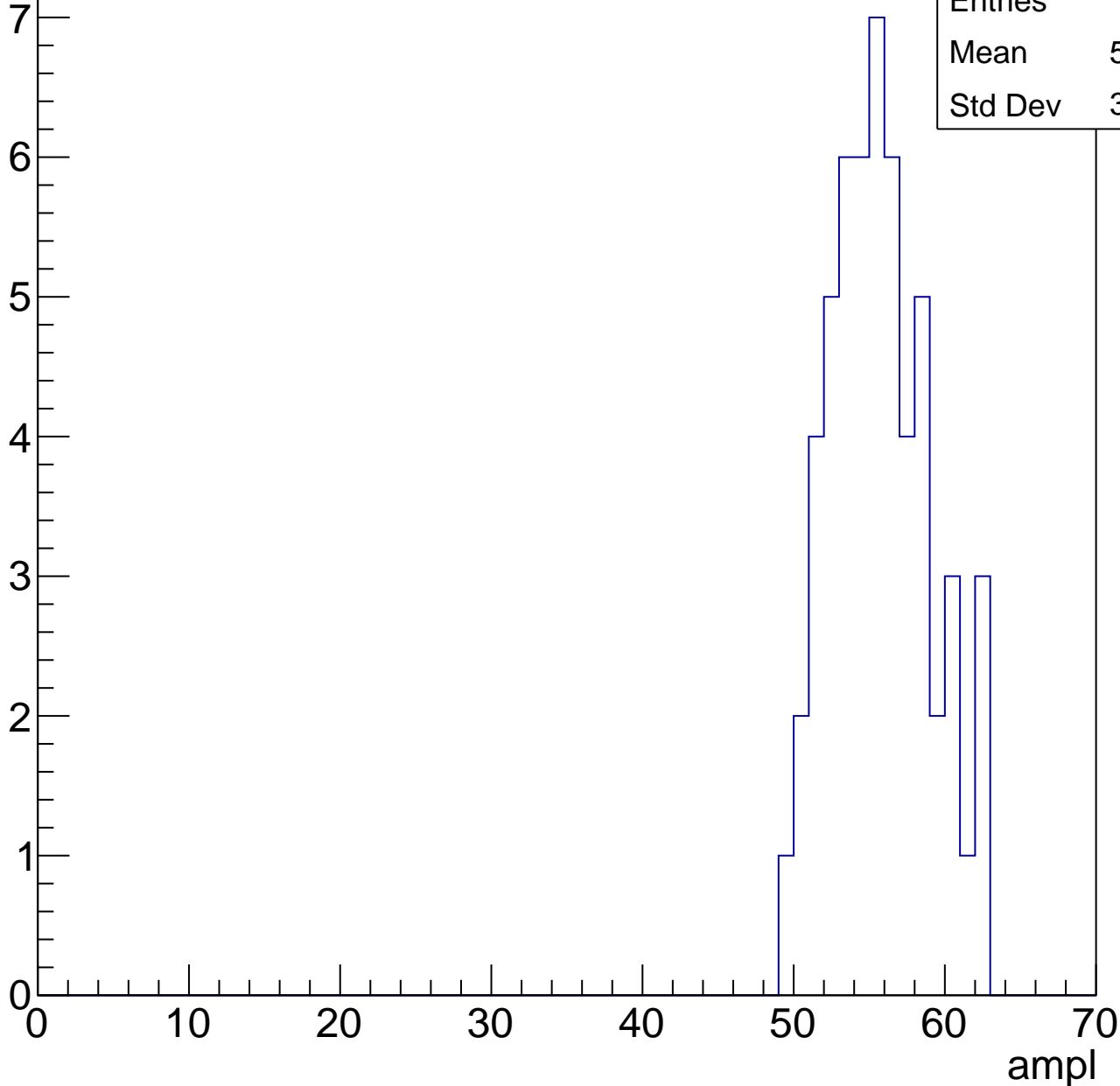


# B1L102S, U5-ch39, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	55.25
Std Dev	3.243

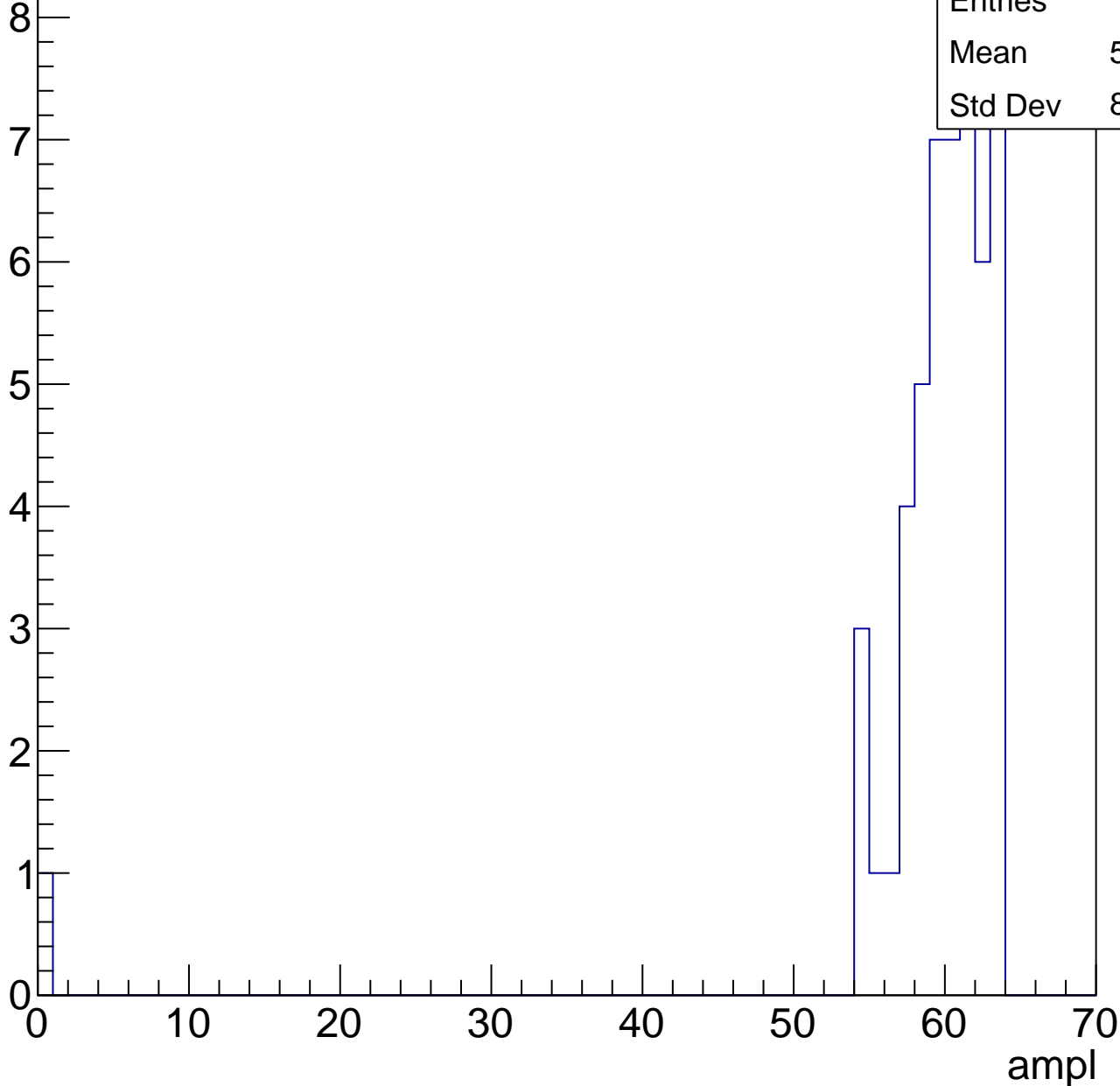


# B1L102S, U5-ch39, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	58.59
Std Dev	8.648



# B1L102S, U5-ch39, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U5-ch39, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U5-ch40, adc0

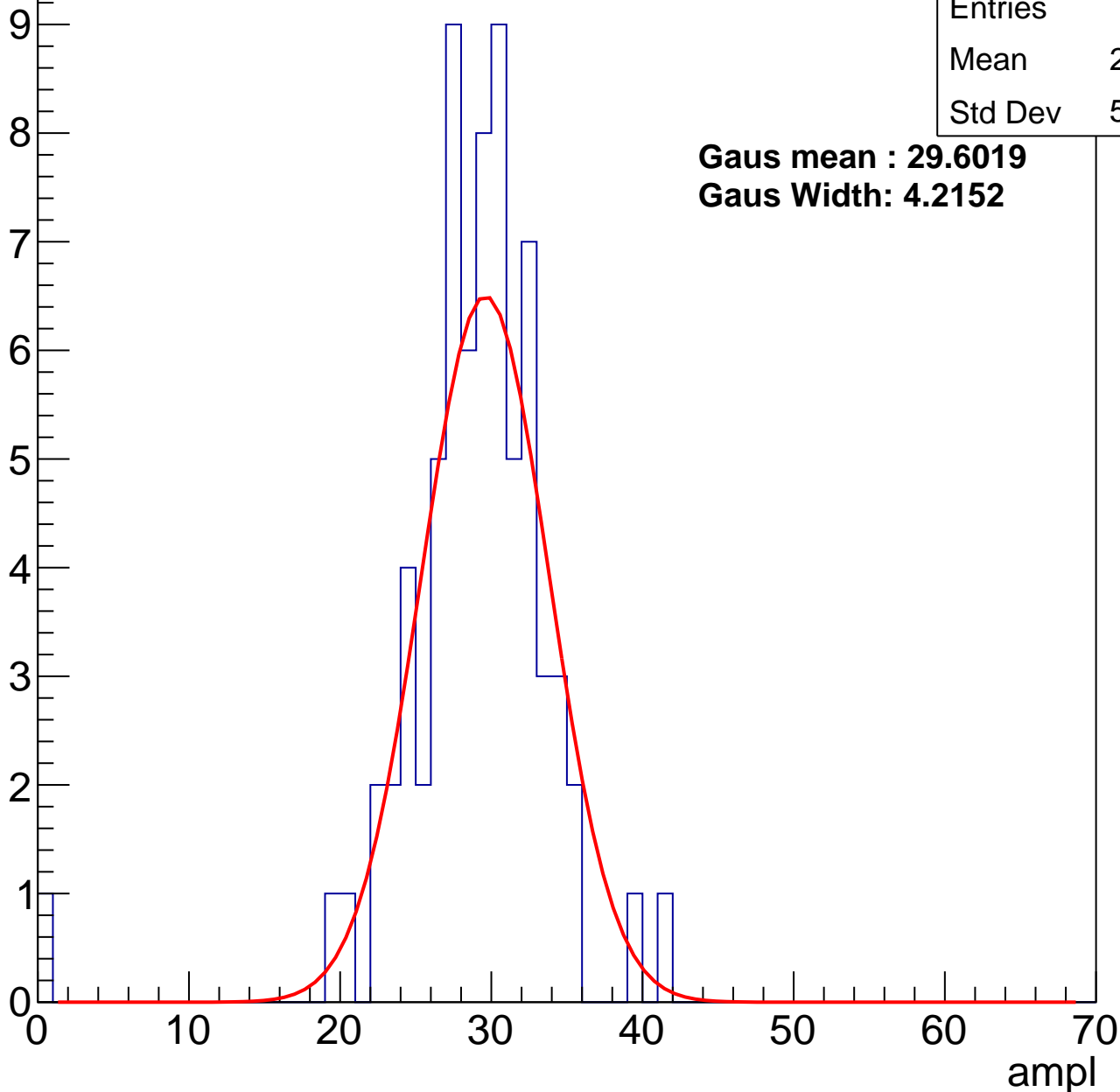
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	28.44
Std Dev	5.164

**Gaus mean : 29.6019**

**Gaus Width: 4.2152**



# B1L102S, U5-ch40, adc1

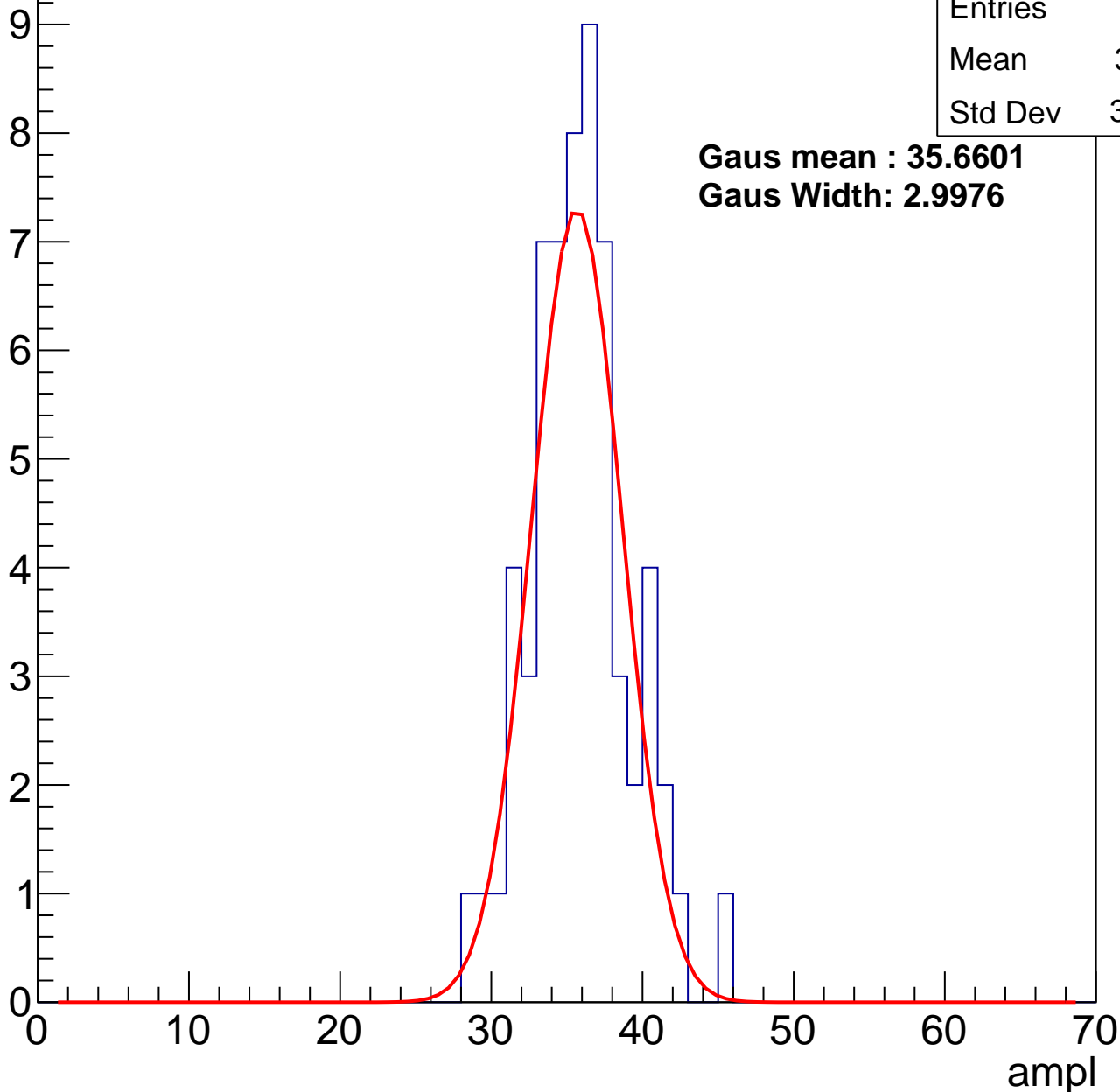
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	35.41
Std Dev	3.246

**Gaus mean : 35.6601**

**Gaus Width: 2.9976**



# B1L102S, U5-ch40, adc2

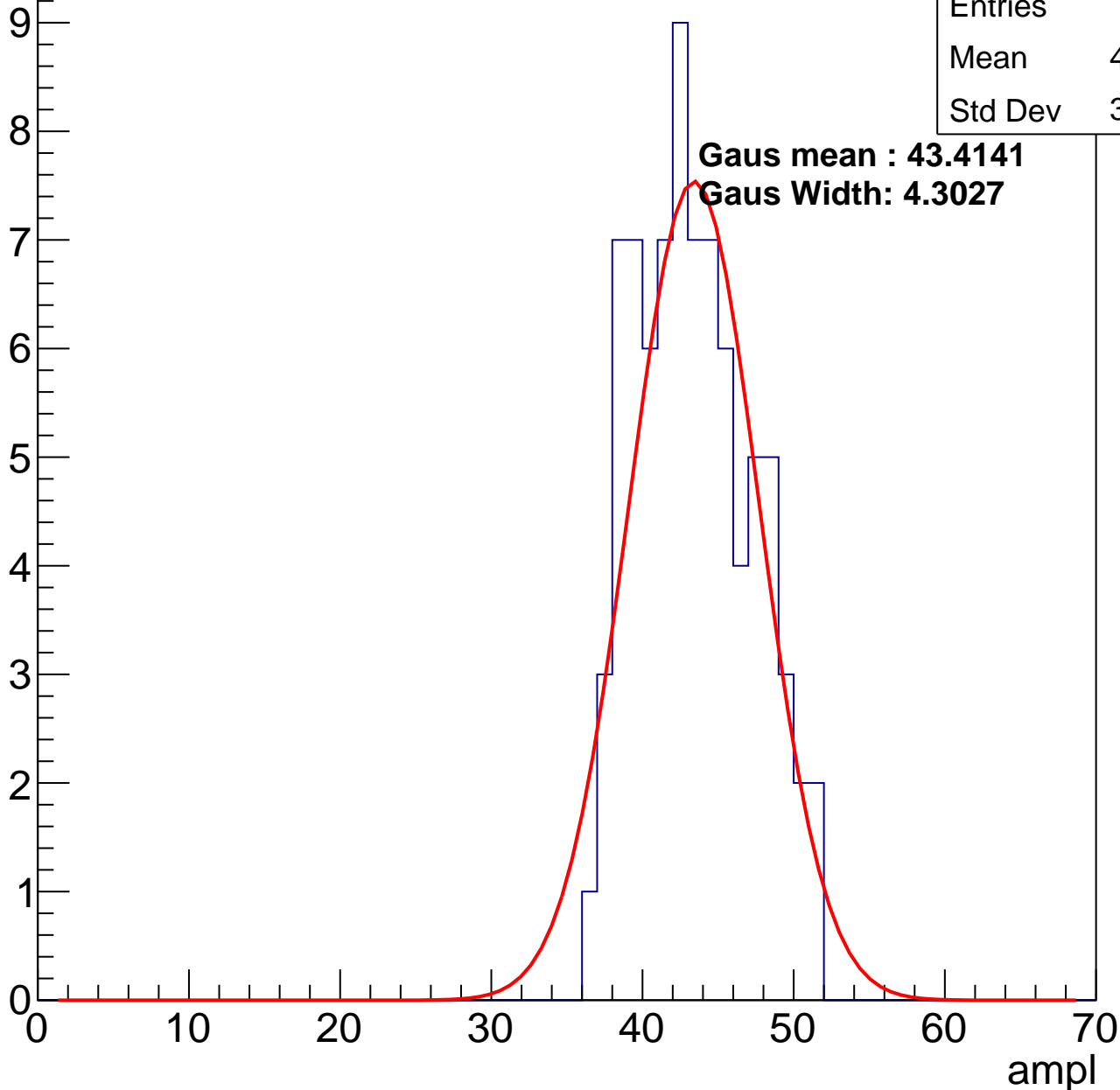
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	81
Mean	42.94
Std Dev	3.753

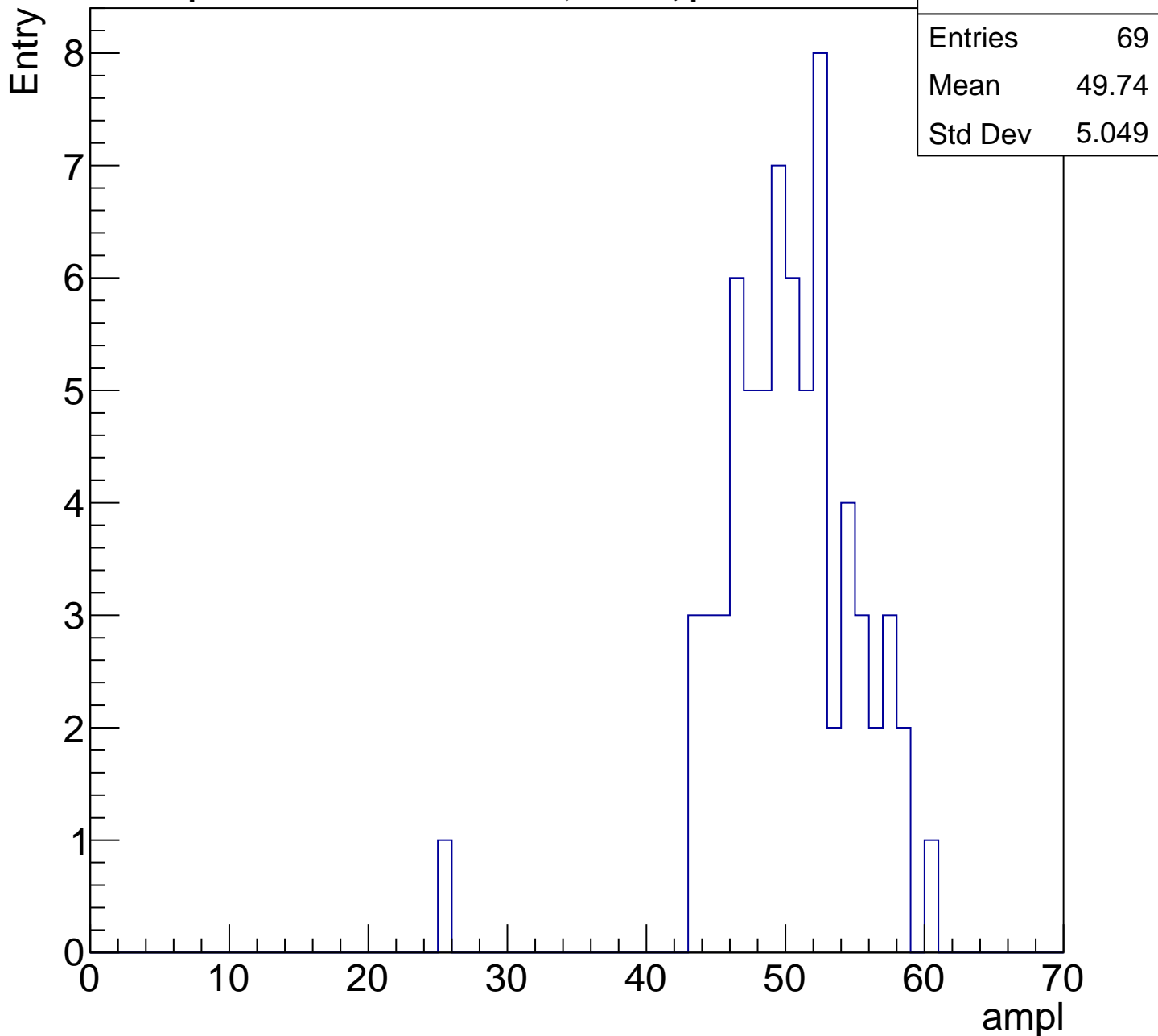
**Gaus mean : 43.4141**

**Gaus Width: 4.3027**



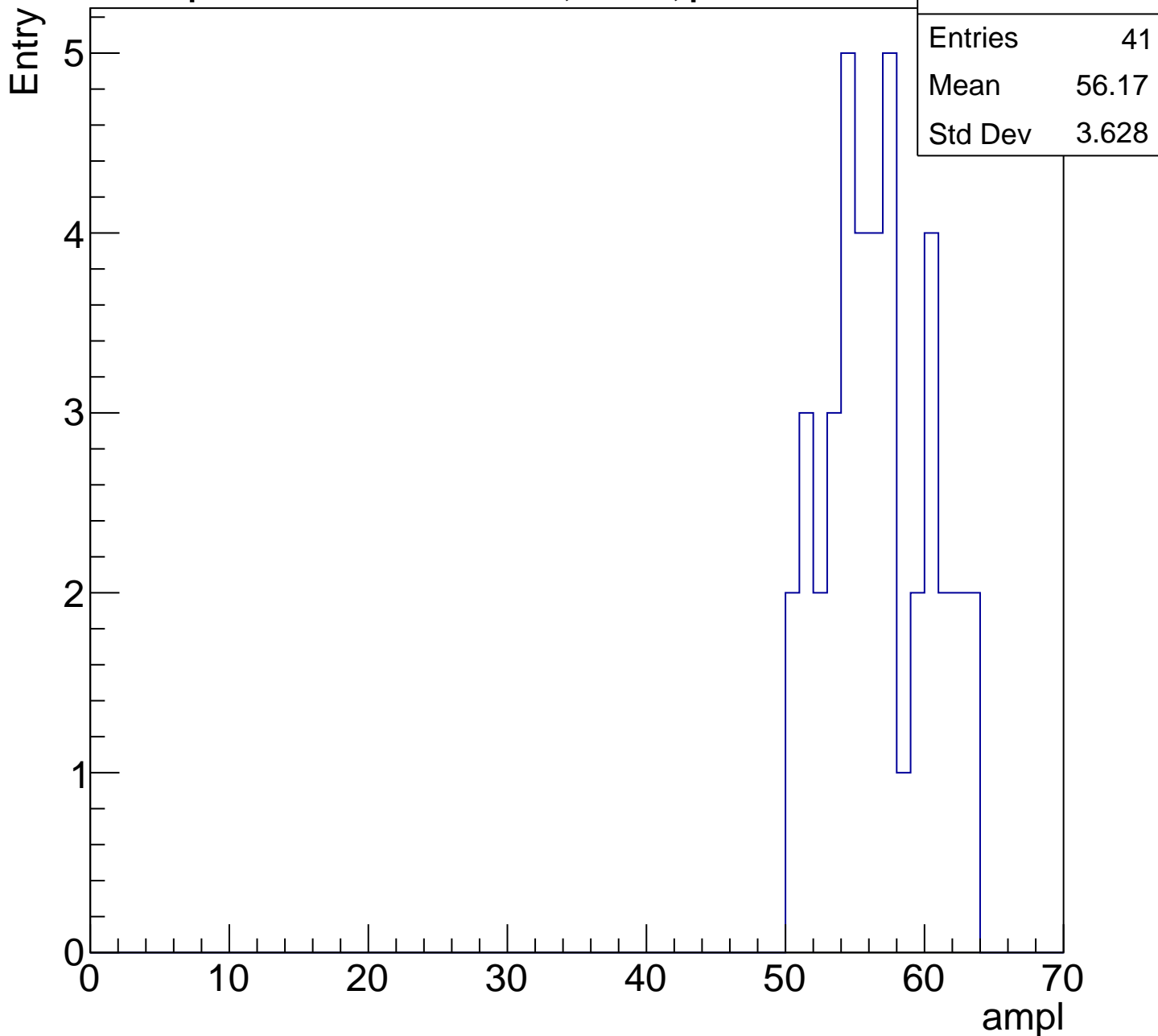
# B1L102S, U5-ch40, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2



# B1L102S, U5-ch40, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

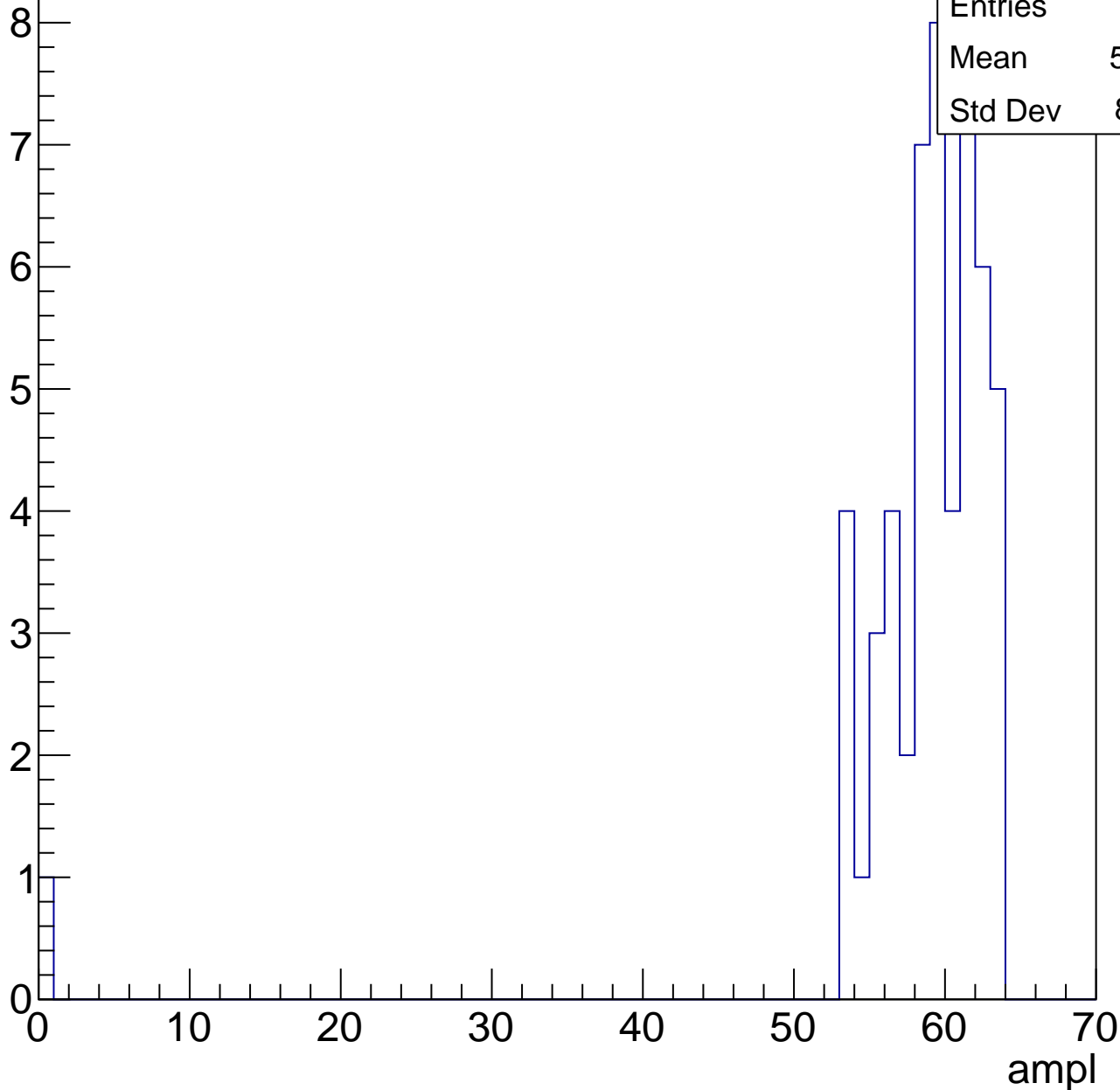


# B1L102S, U5-ch40, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	57.77
Std Dev	8.511



# B1L102S, U5-ch40, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

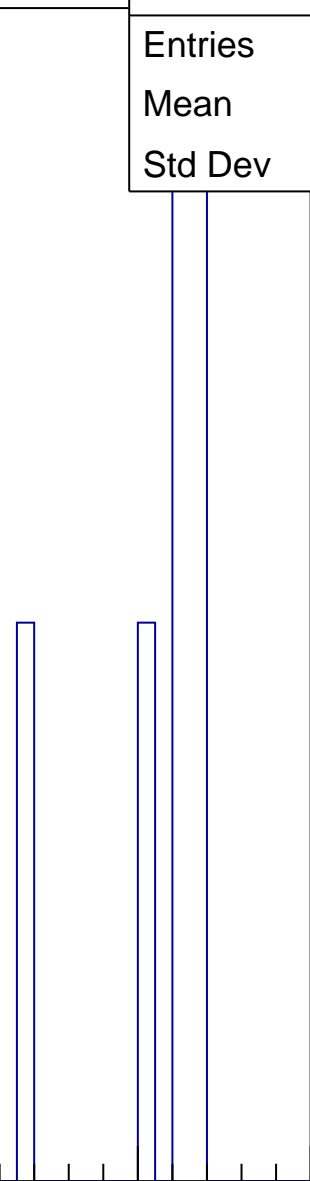
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	60.5
Std Dev	3.5

0 10 20 30 40 50 60 70

ampl





# B1L102S, U5-ch40, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	3
Mean	21
Std Dev	29.7

# B1L102S, U5-ch41, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	81
Mean	27.8
Std Dev	5.723

**Gaus mean : 29.1038**

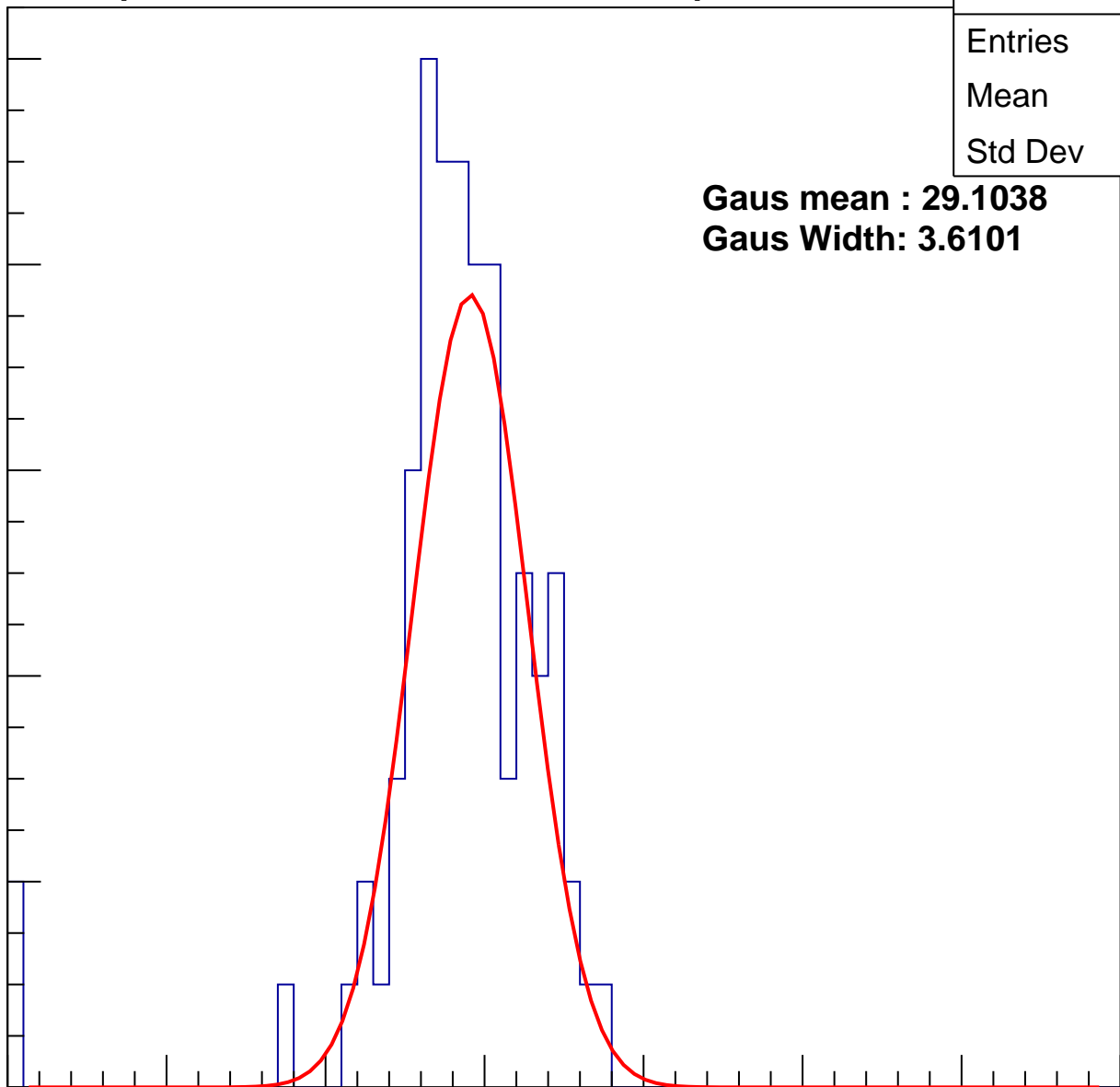
**Gaus Width: 3.6101**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U5-ch41, adc1

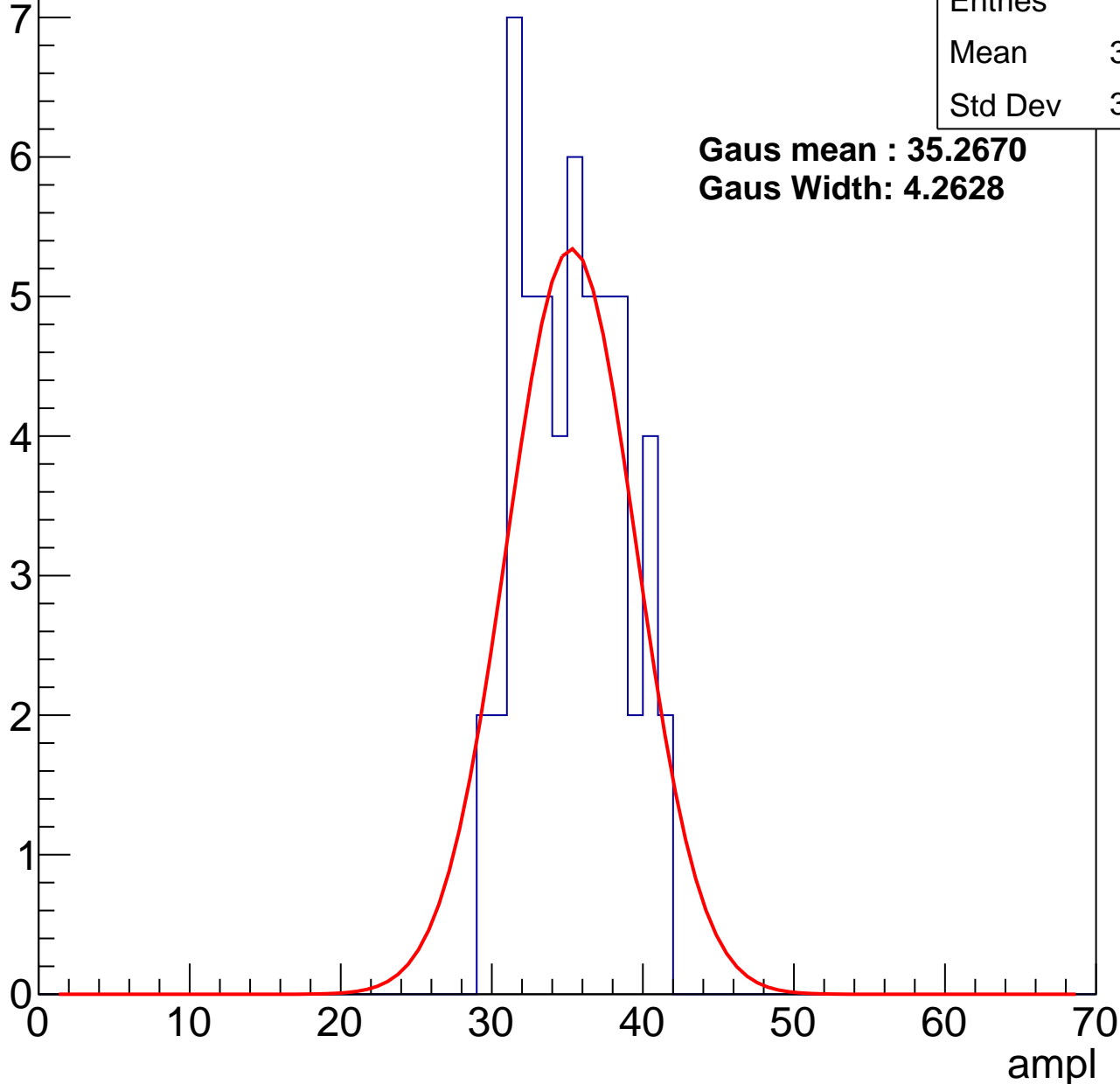
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	34.83
Std Dev	3.265

**Gaus mean : 35.2670**

**Gaus Width: 4.2628**



# B1L102S, U5-ch41, adc2

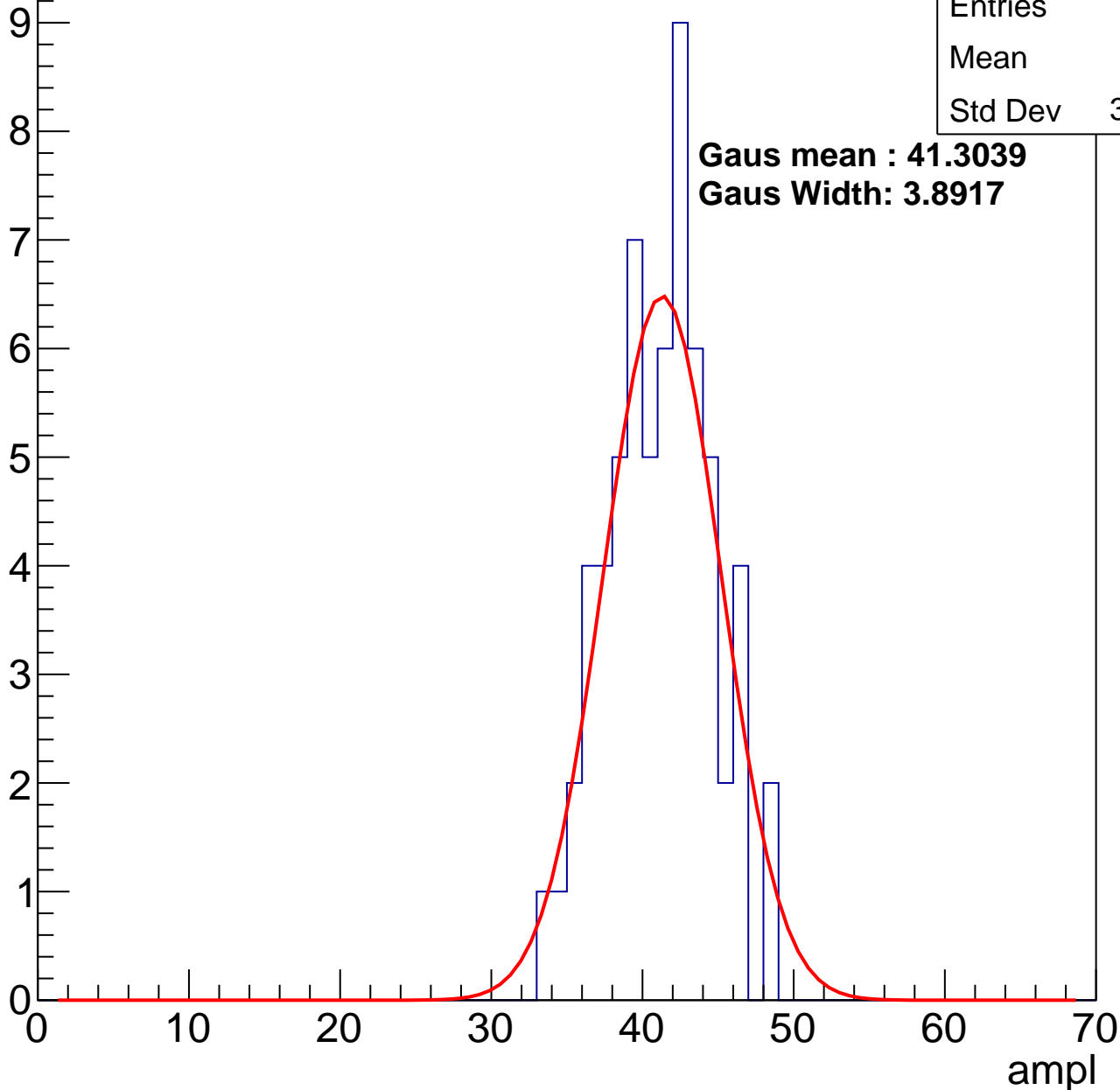
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	40.7
Std Dev	3.402

**Gaus mean : 41.3039**

**Gaus Width: 3.8917**

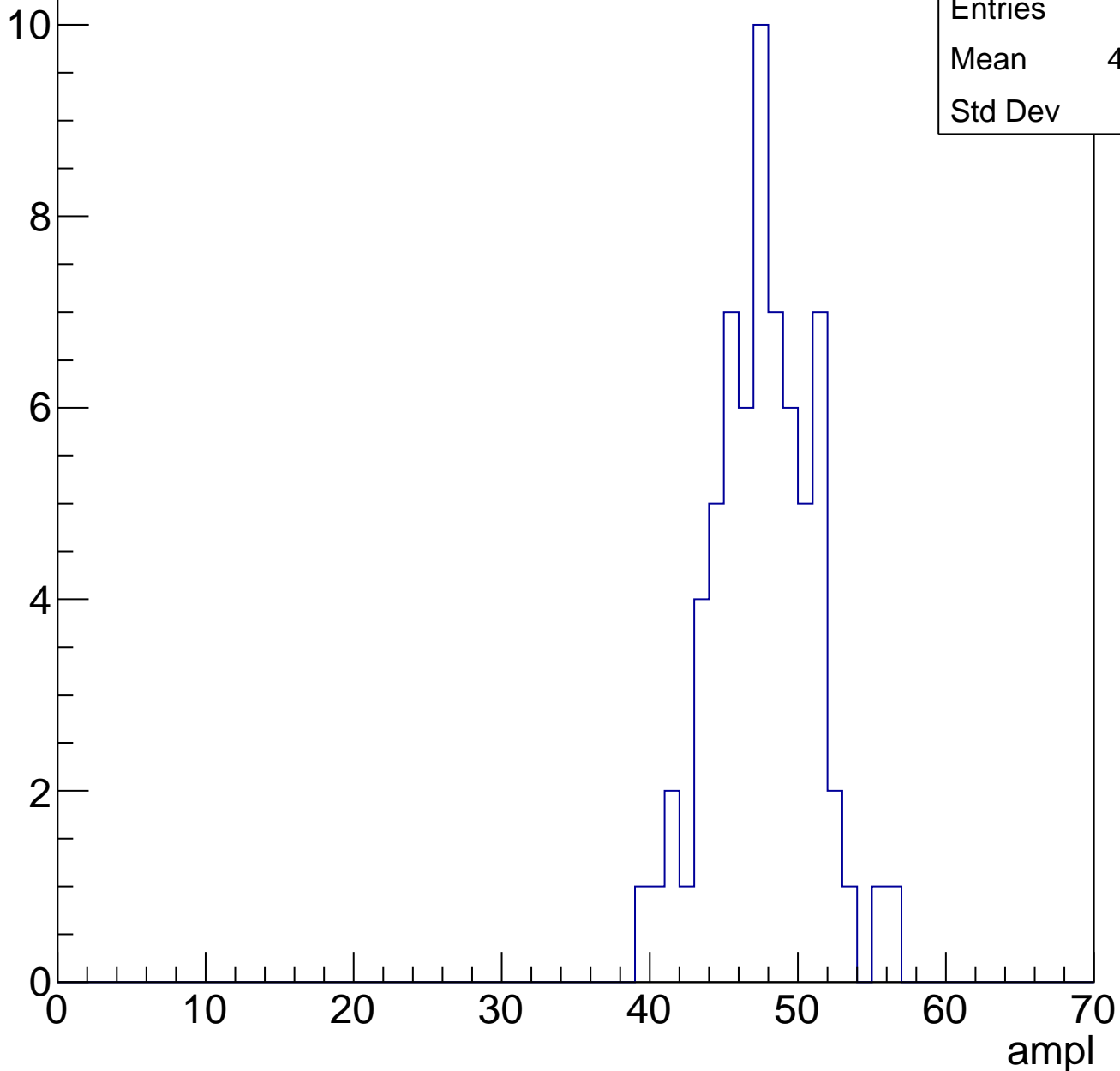


# B1L102S, U5-ch41, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

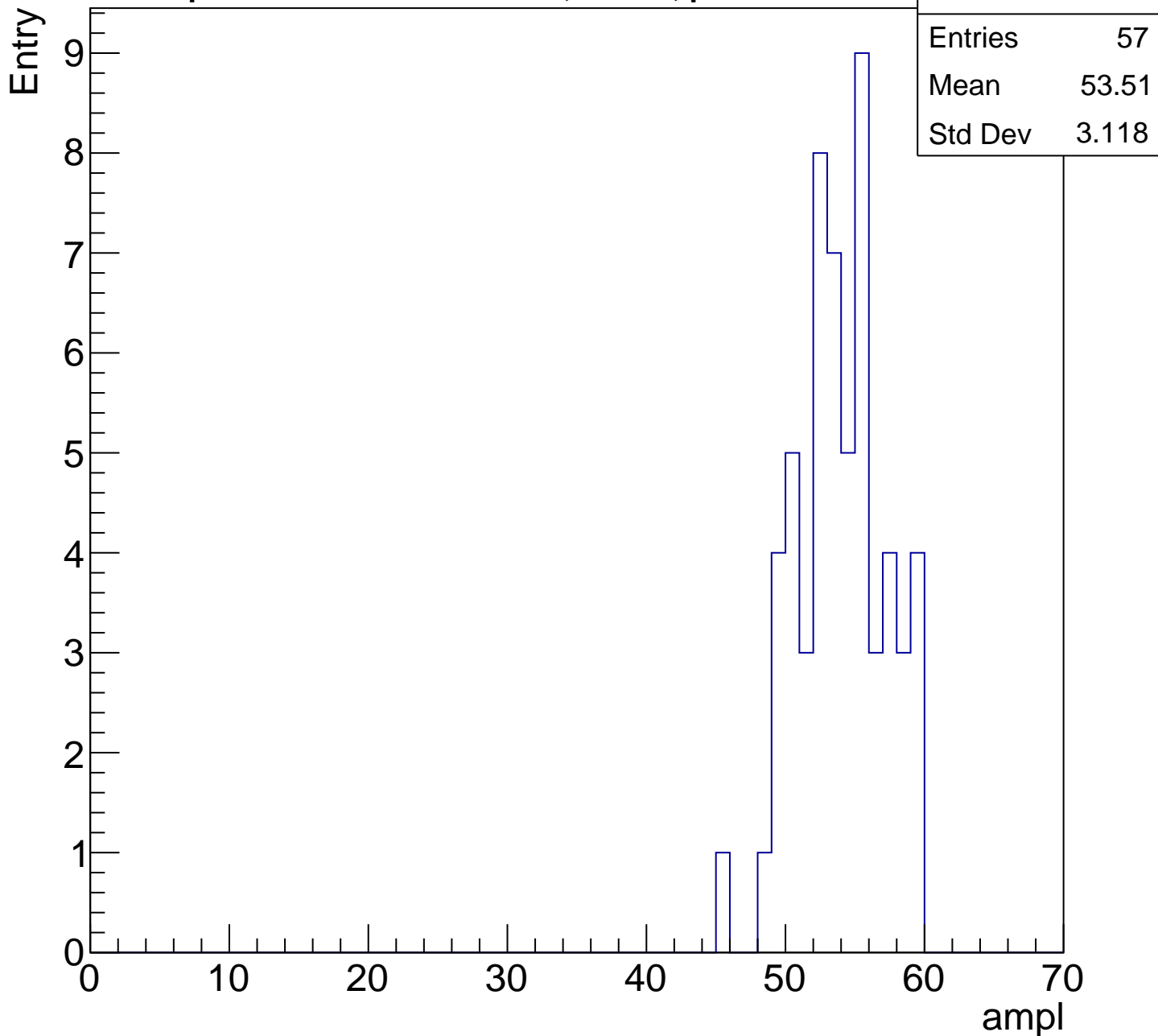
Entries	67
Mean	47.18
Std Dev	3.39

Entry



# B1L102S, U5-ch41, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

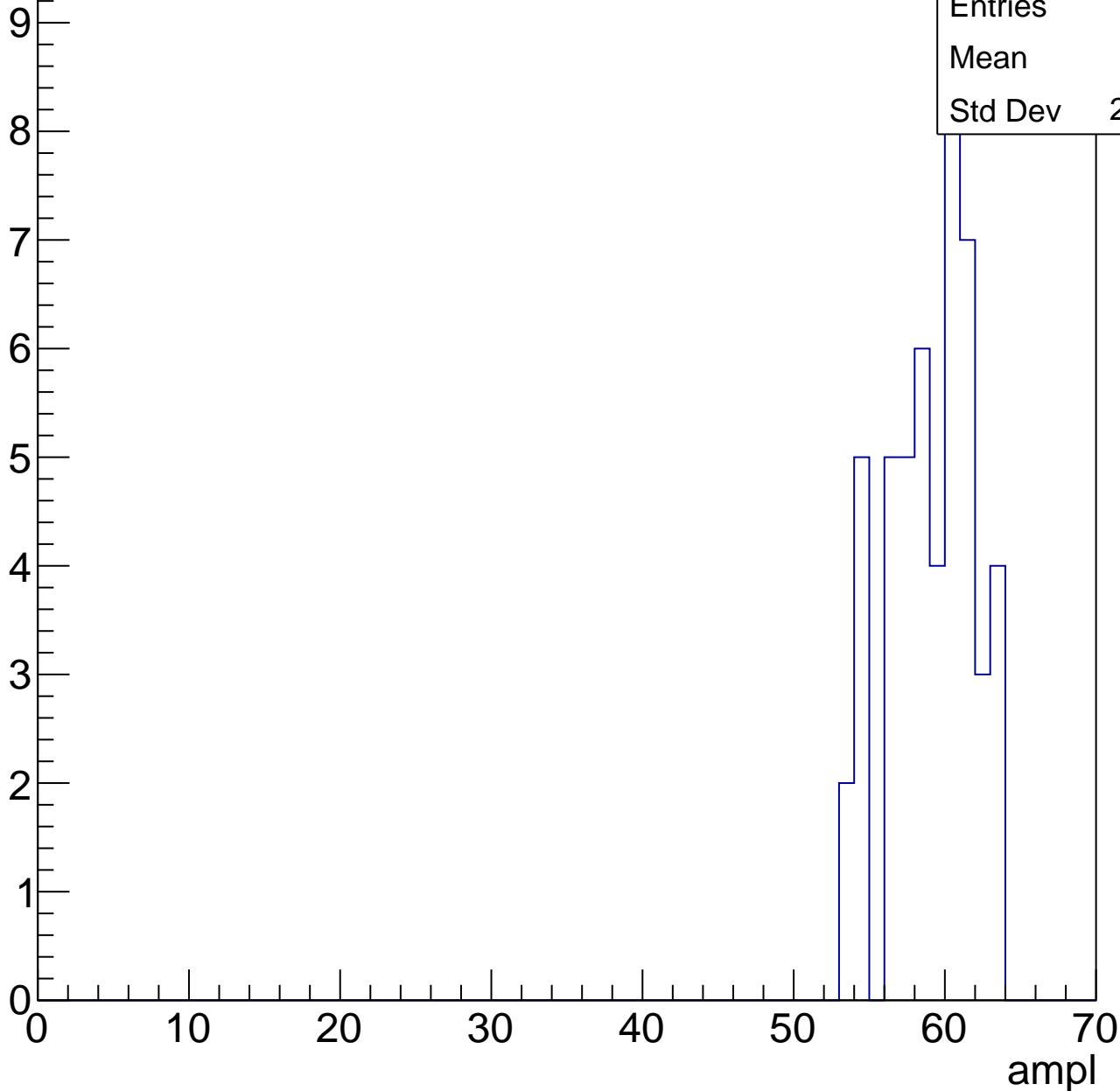


# B1L102S, U5-ch41, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	58.6
Std Dev	2.786

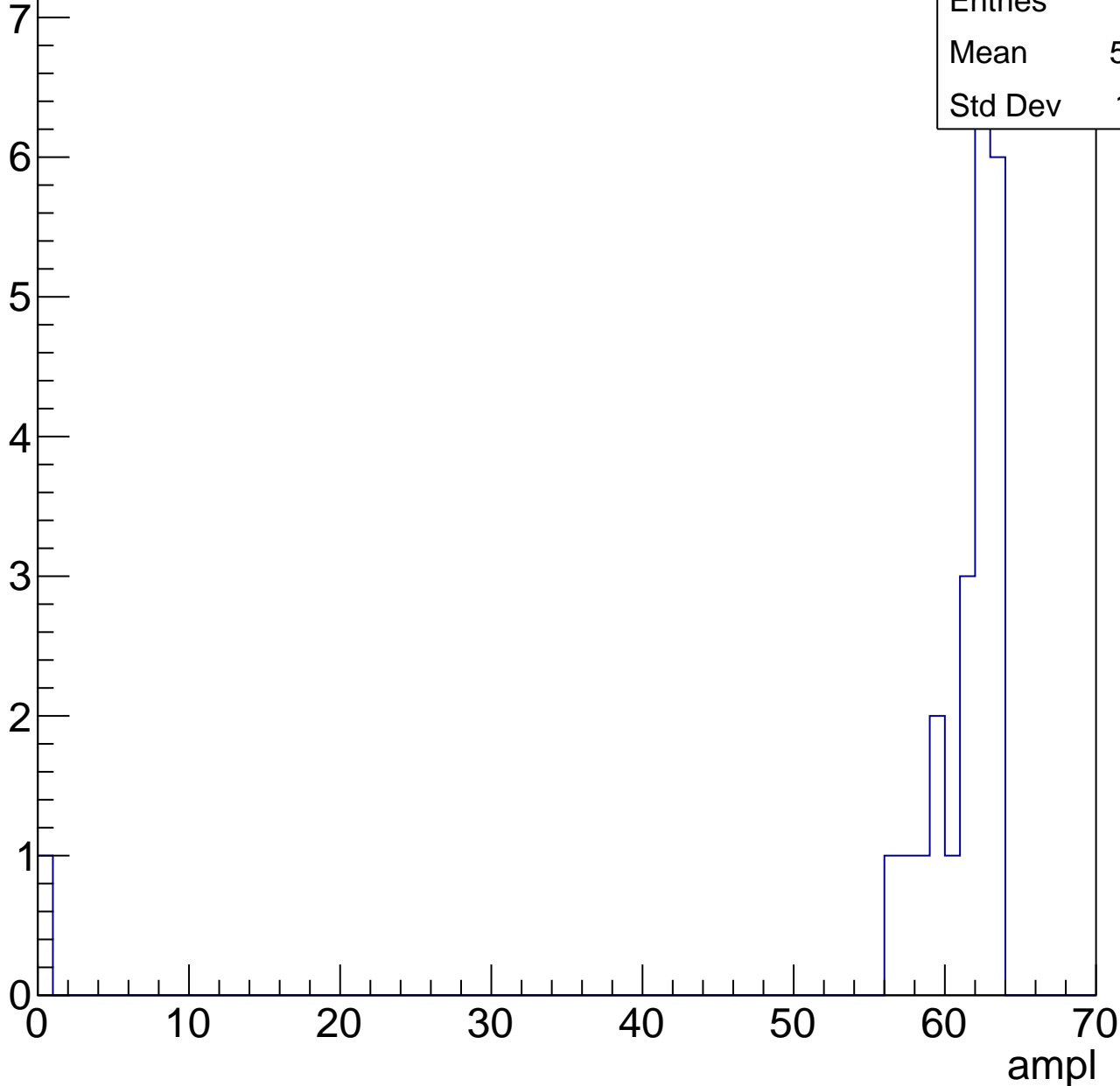


# B1L102S, U5-ch41, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	23
Mean	58.43
Std Dev	12.61

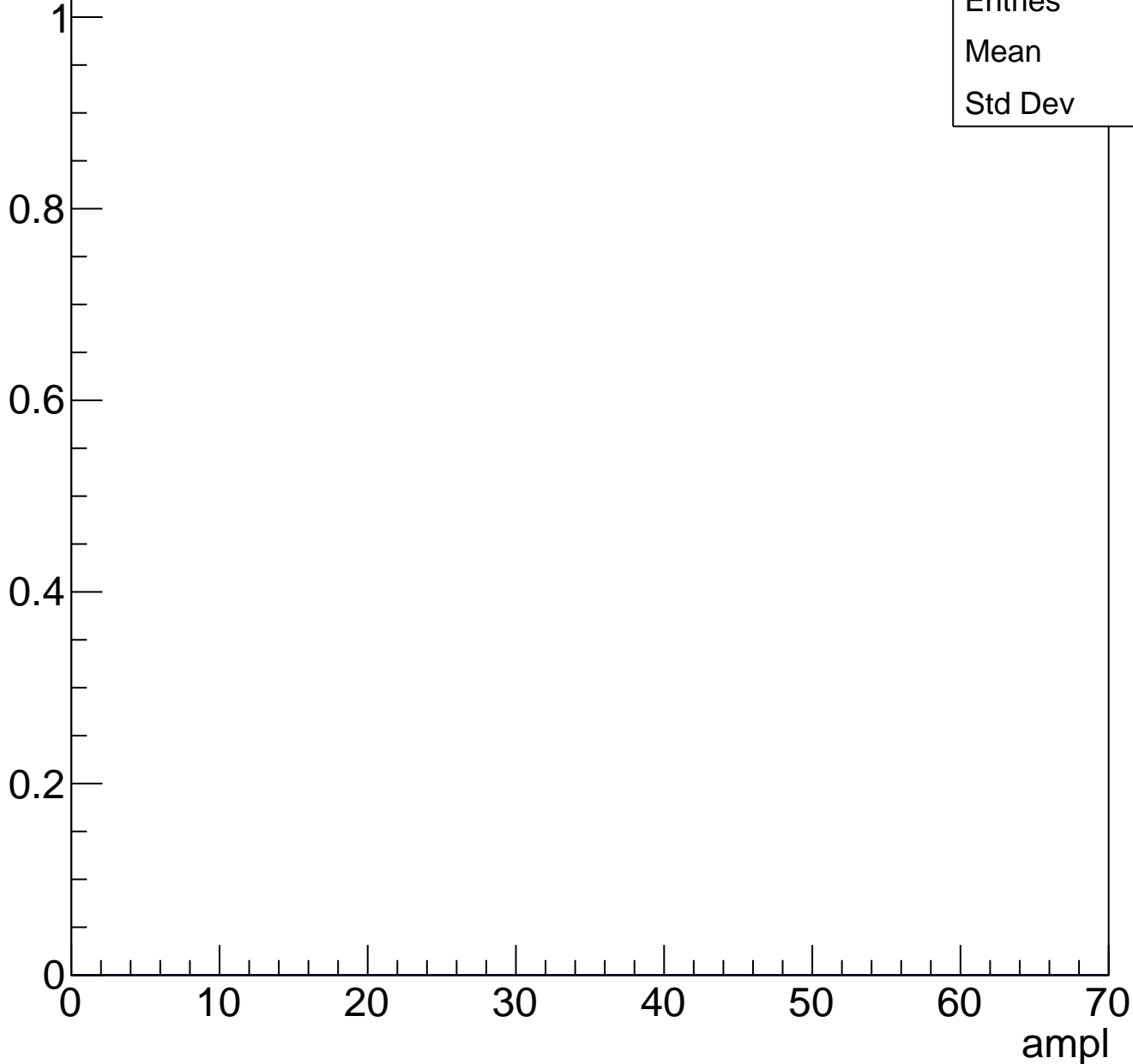




# B1L102S, U5-ch41, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U5-ch42, adc0

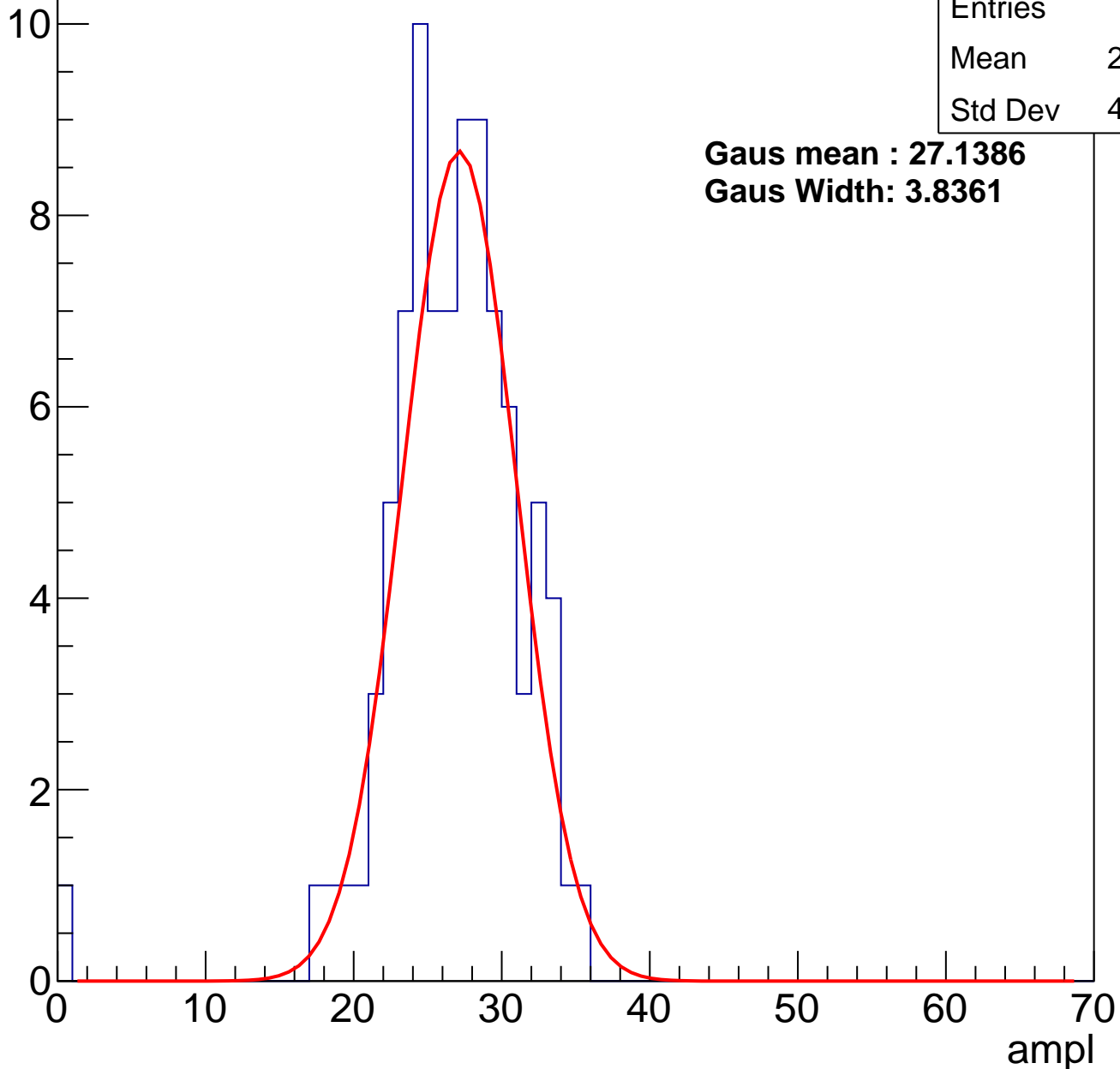
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	89
Mean	26.26
Std Dev	4.699

**Gaus mean : 27.1386**

**Gaus Width: 3.8361**

Entry



# B1L102S, U5-ch42, adc1

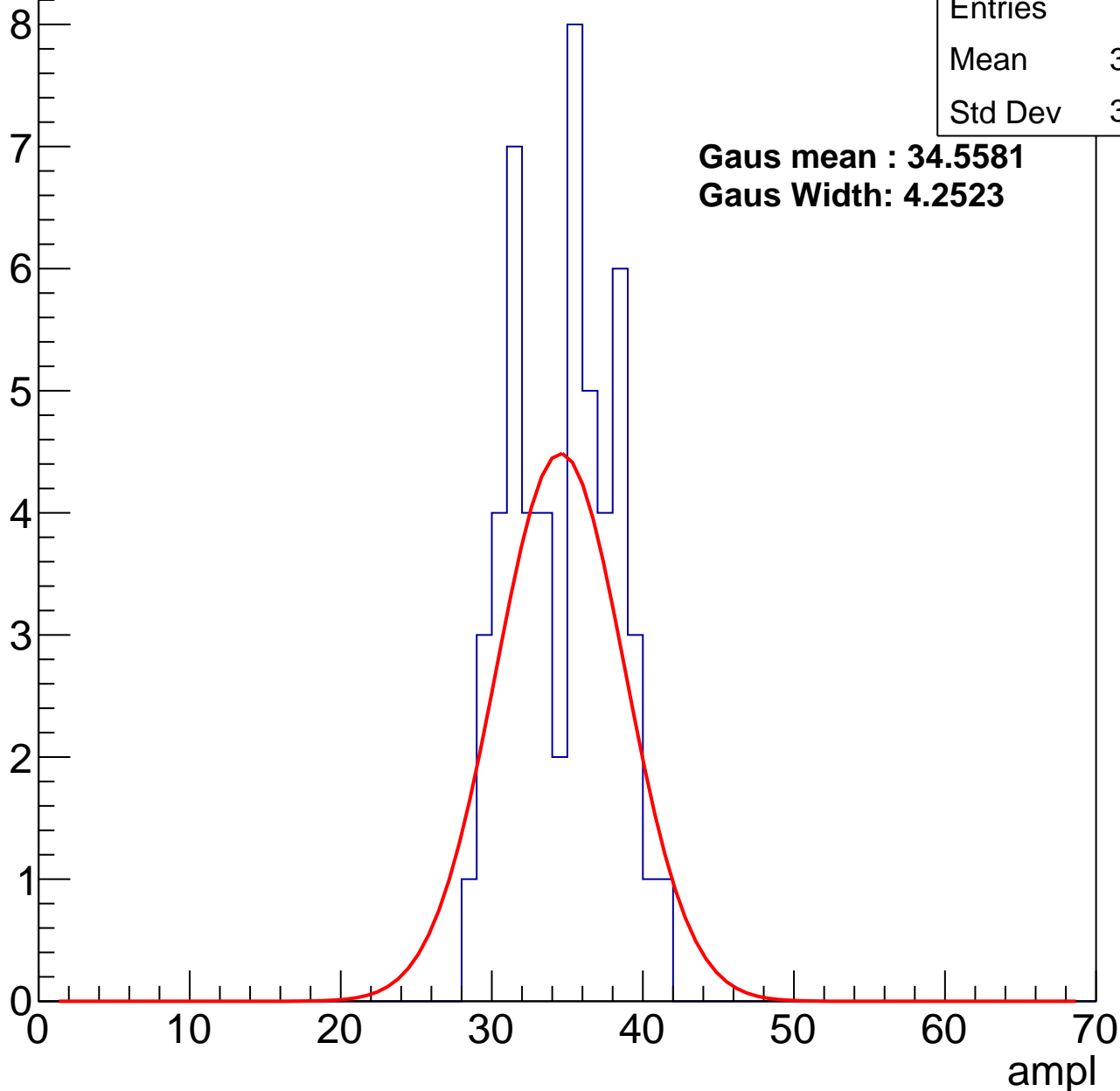
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	34.23
Std Dev	3.295

**Gaus mean : 34.5581**

**Gaus Width: 4.2523**



# B1L102S, U5-ch42, adc2

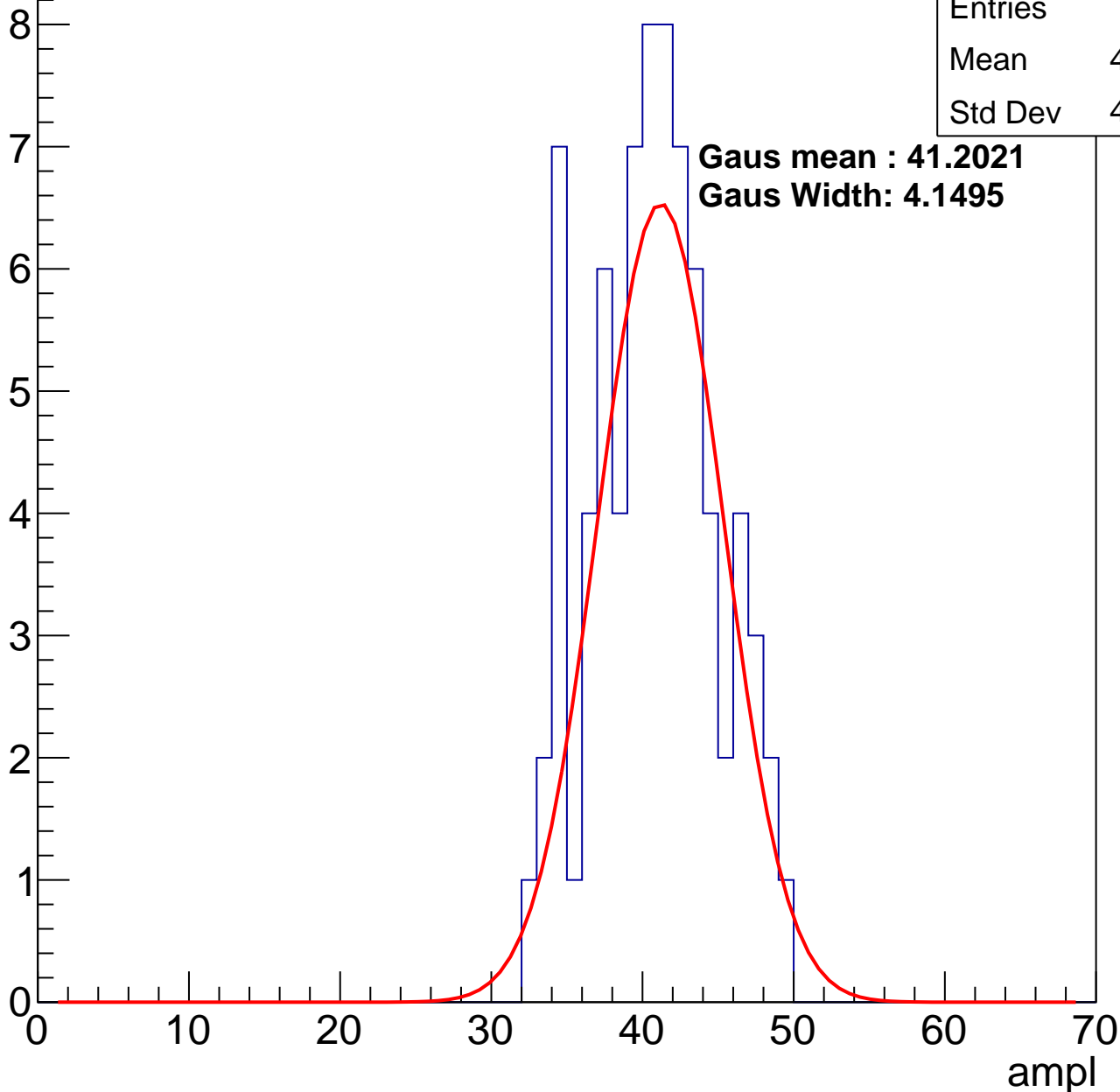
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	40.23
Std Dev	4.077

**Gaus mean : 41.2021**

**Gaus Width: 4.1495**

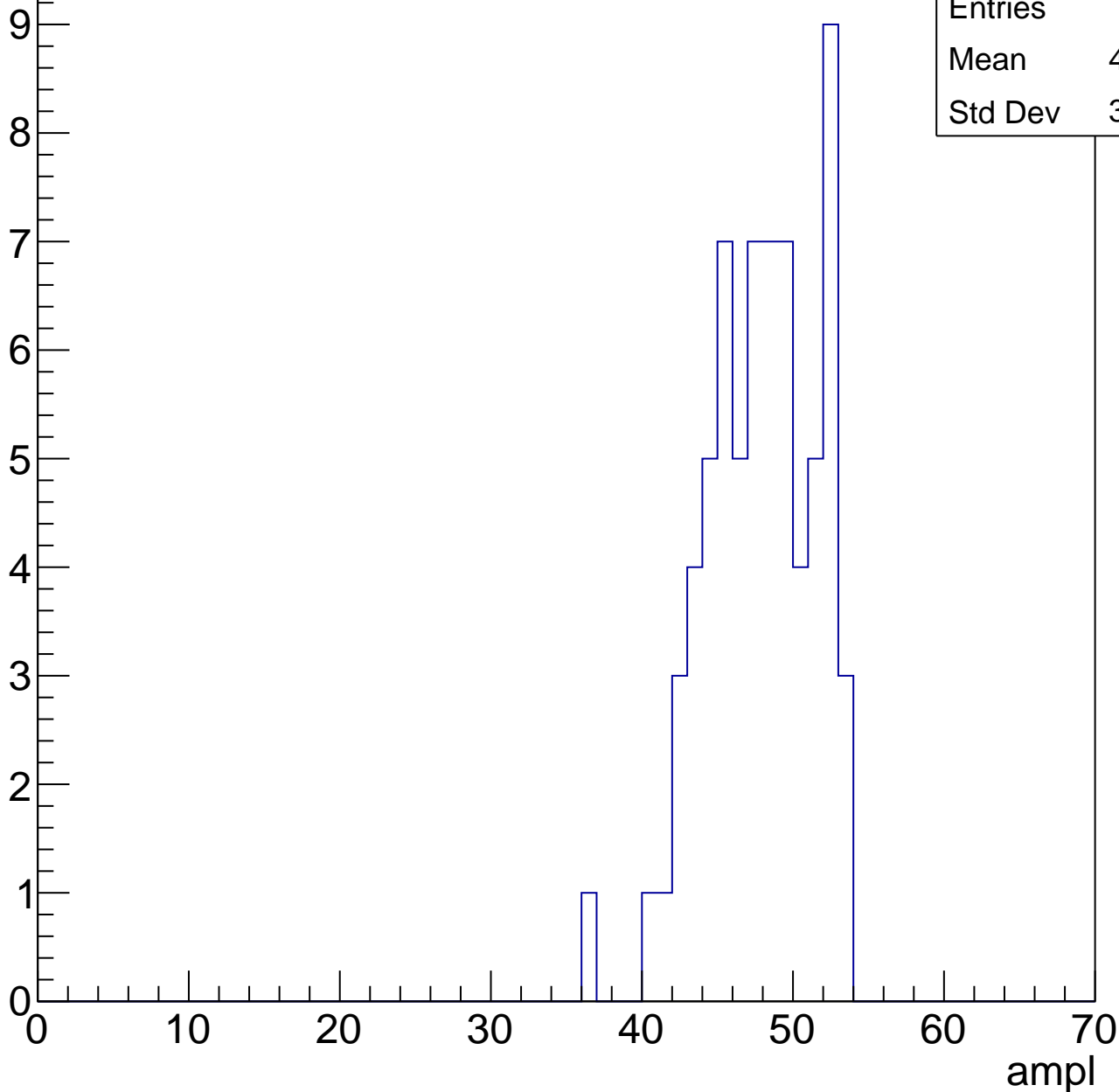


# B1L102S, U5-ch42, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	47.39
Std Dev	3.604

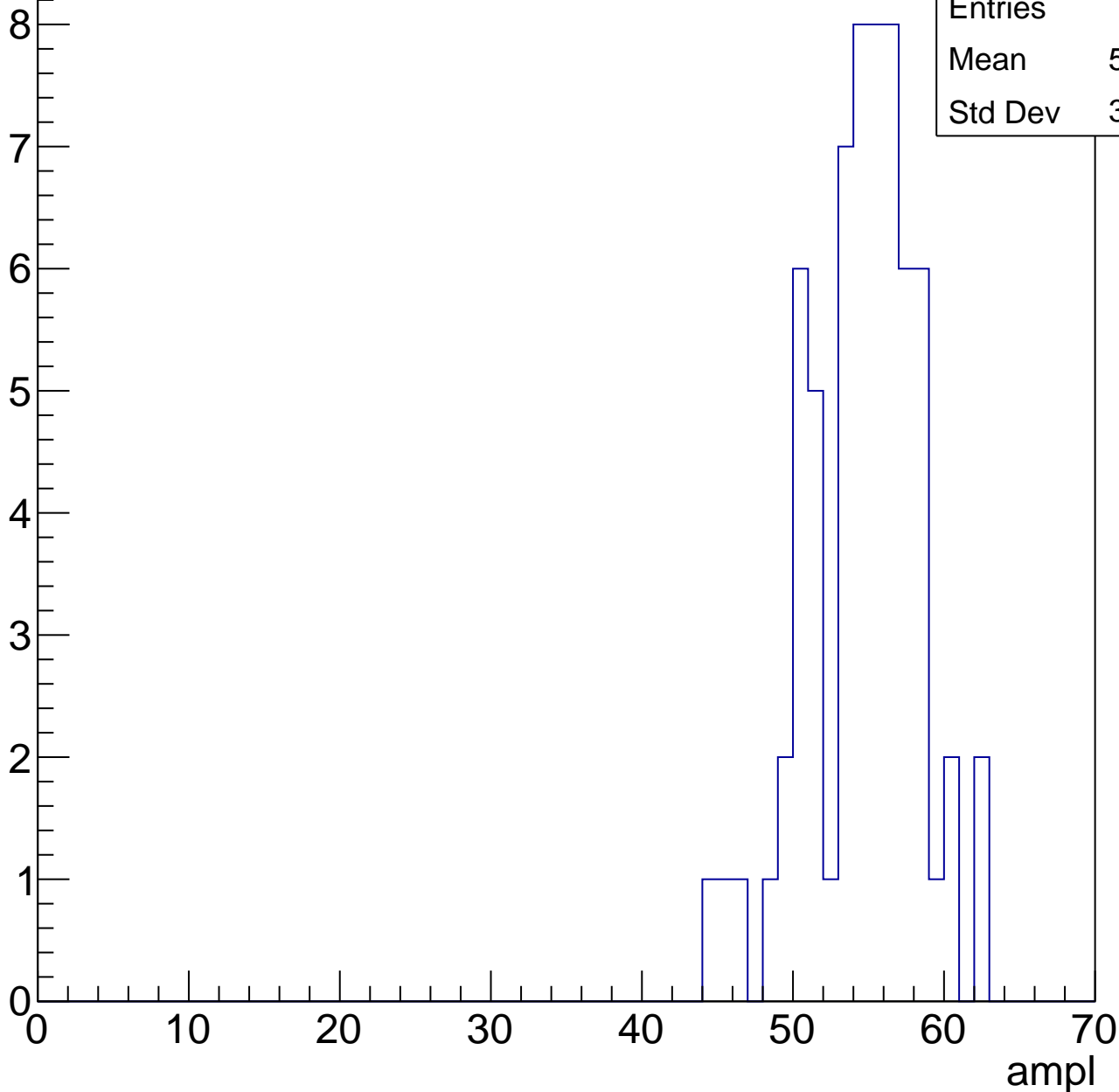


# B1L102S, U5-ch42, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	54.12
Std Dev	3.687



# B1L102S, U5-ch42, adc5

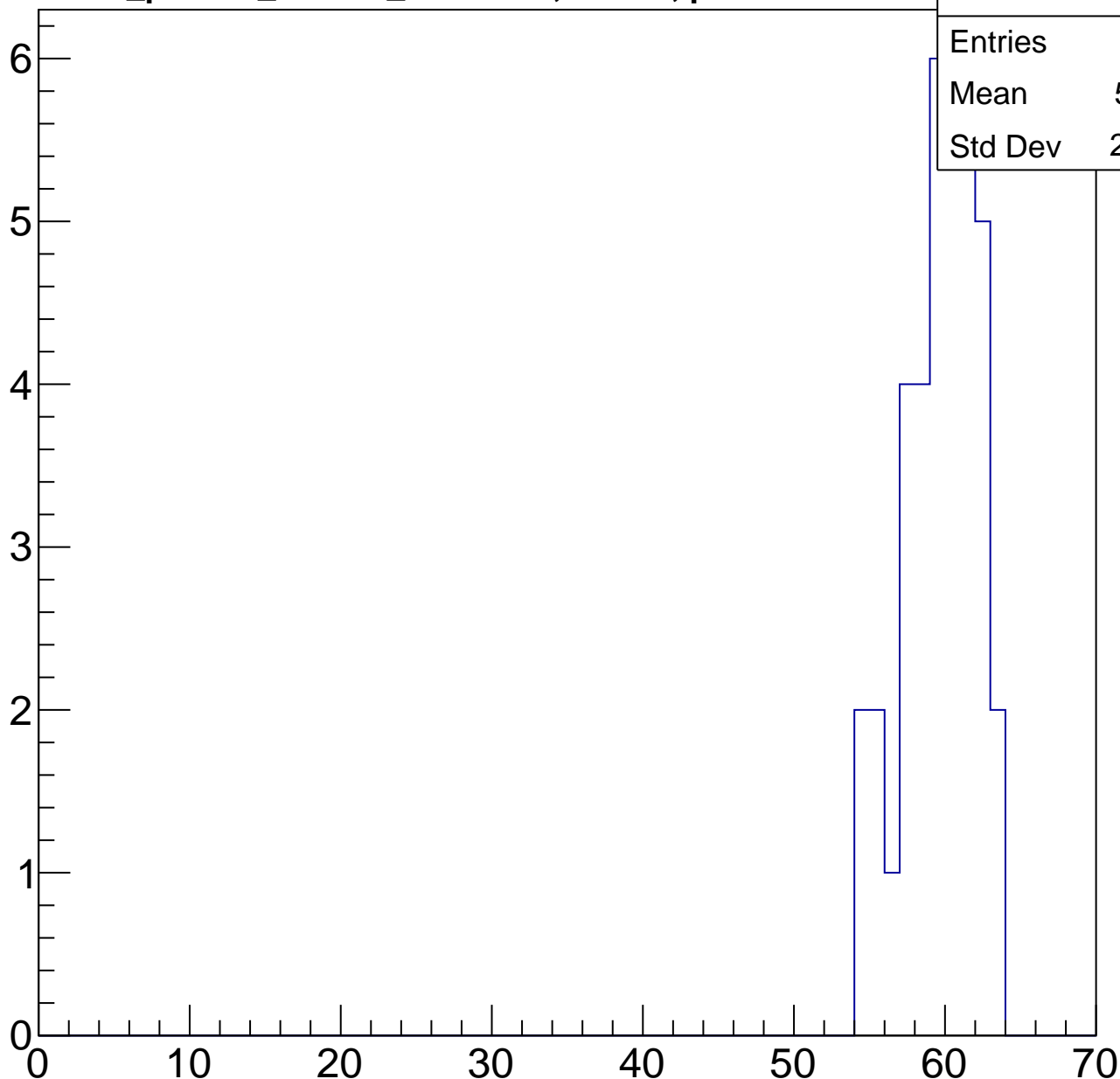
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

6  
5  
4  
3  
2  
1  
0

Entries	38
Mean	59.21
Std Dev	2.386

ampl

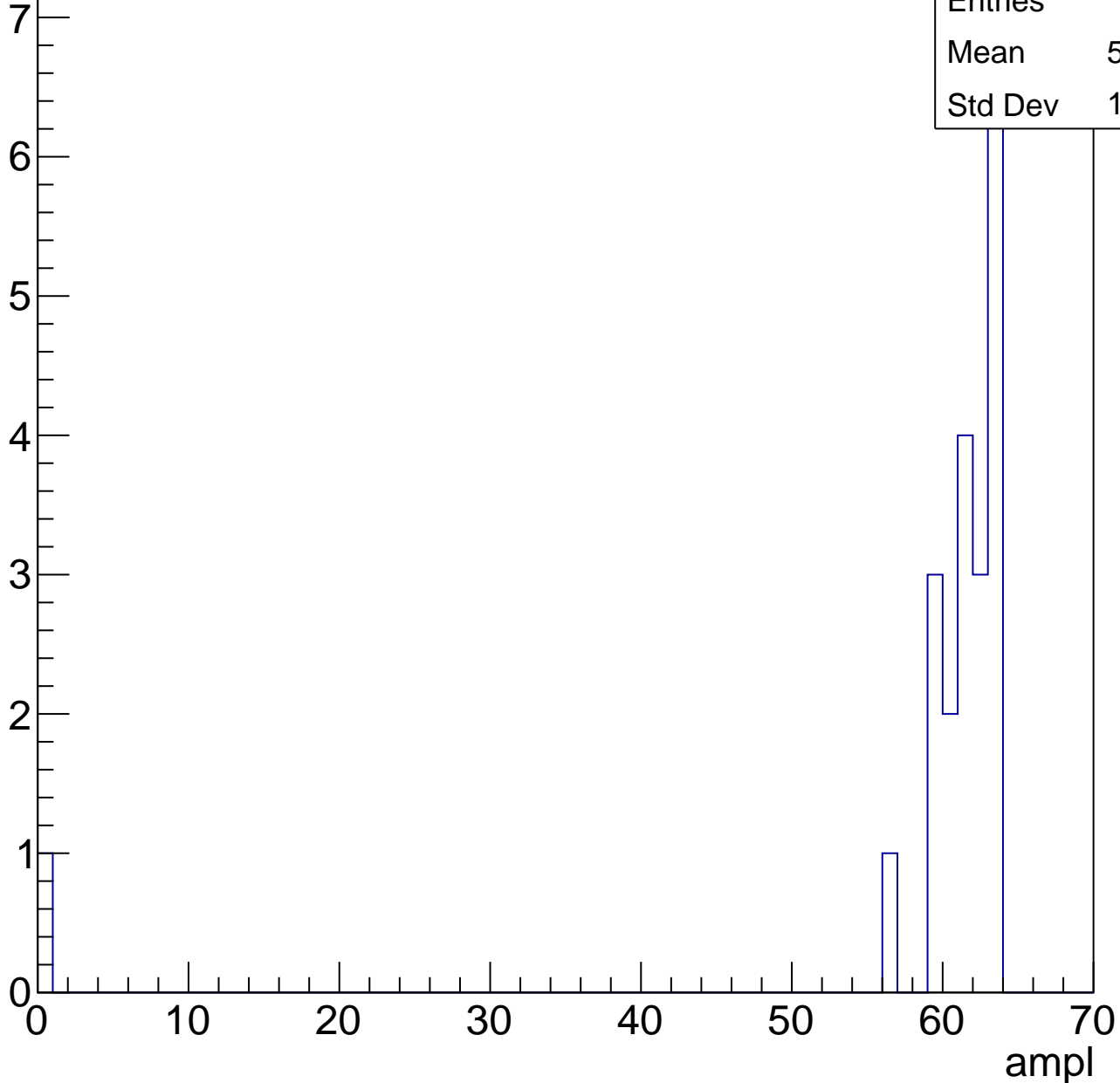


# B1L102S, U5-ch42, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	21
Mean	58.29
Std Dev	13.16





# B1L102S, U5-ch42, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U5-ch43, adc0

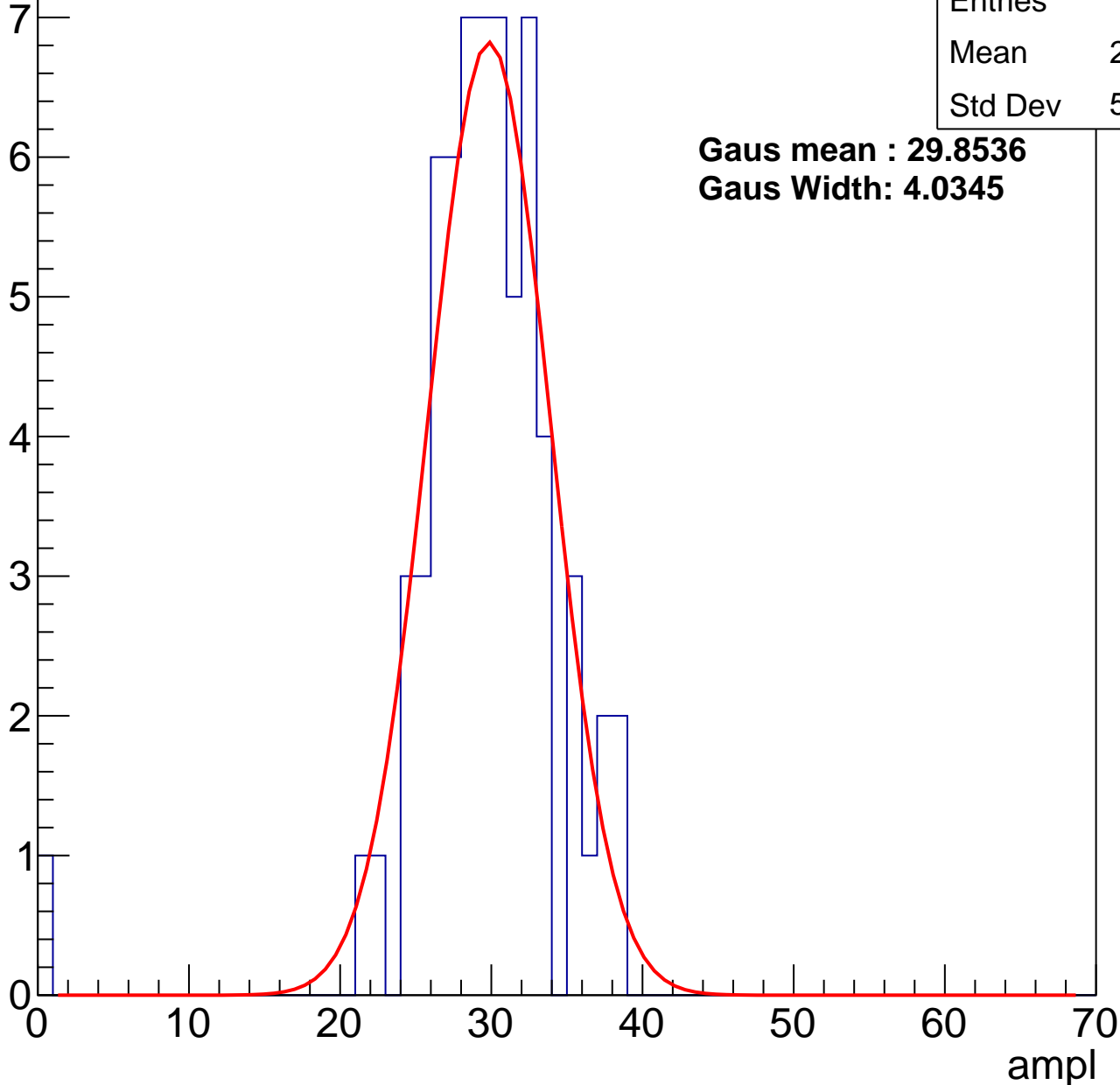
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	29.08
Std Dev	5.168

**Gaus mean : 29.8536**

**Gaus Width: 4.0345**



# B1L102S, U5-ch43, adc1

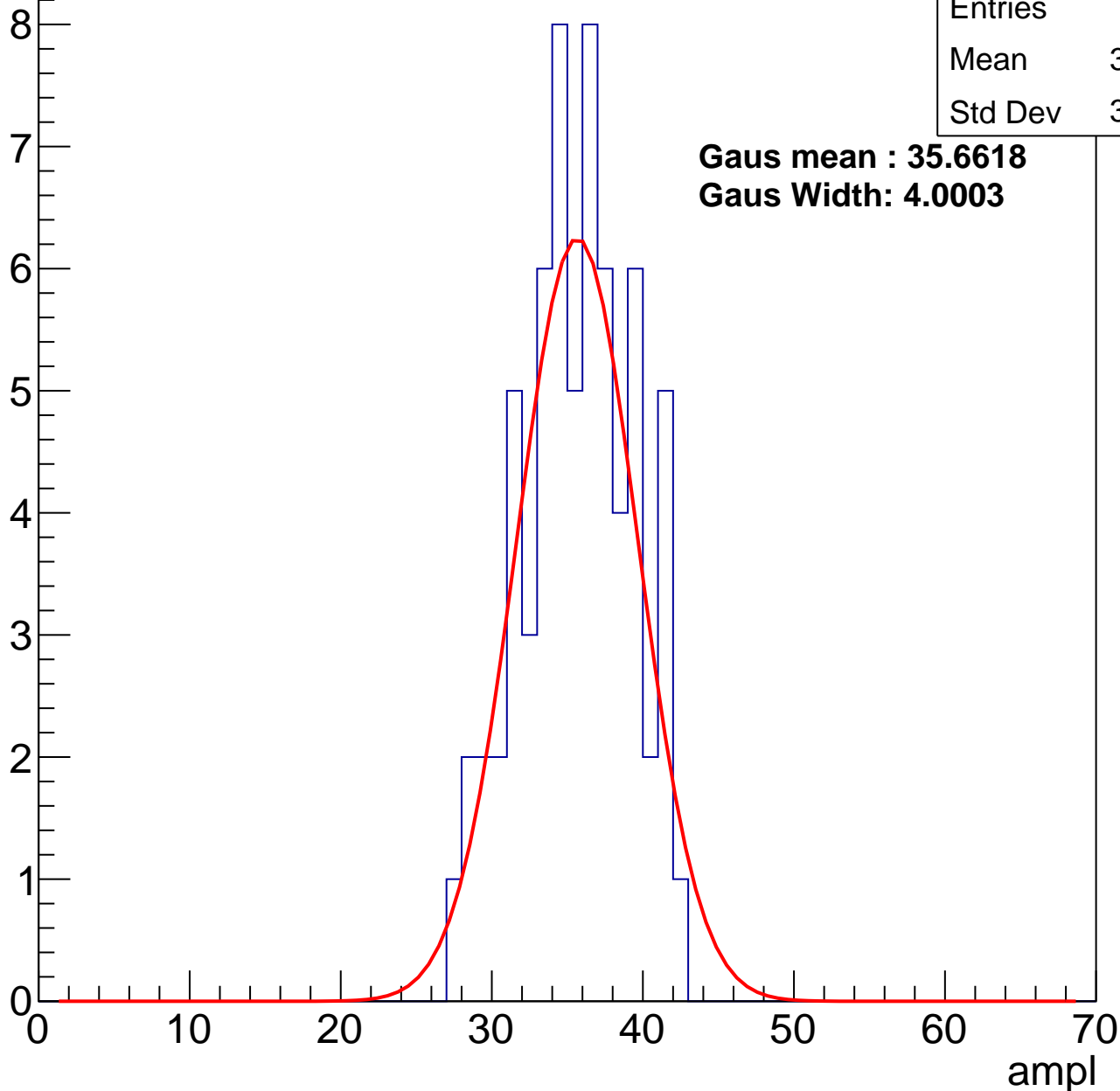
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	35.15
Std Dev	3.619

**Gaus mean : 35.6618**

**Gaus Width: 4.0003**



# B1L102S, U5-ch43, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	79
Mean	42.77
Std Dev	4.012

**Gaus mean : 43.3355**

**Gaus Width: 3.8993**

10

8

6

4

2

0

0

10

20

30

40

50

60

70

ampl

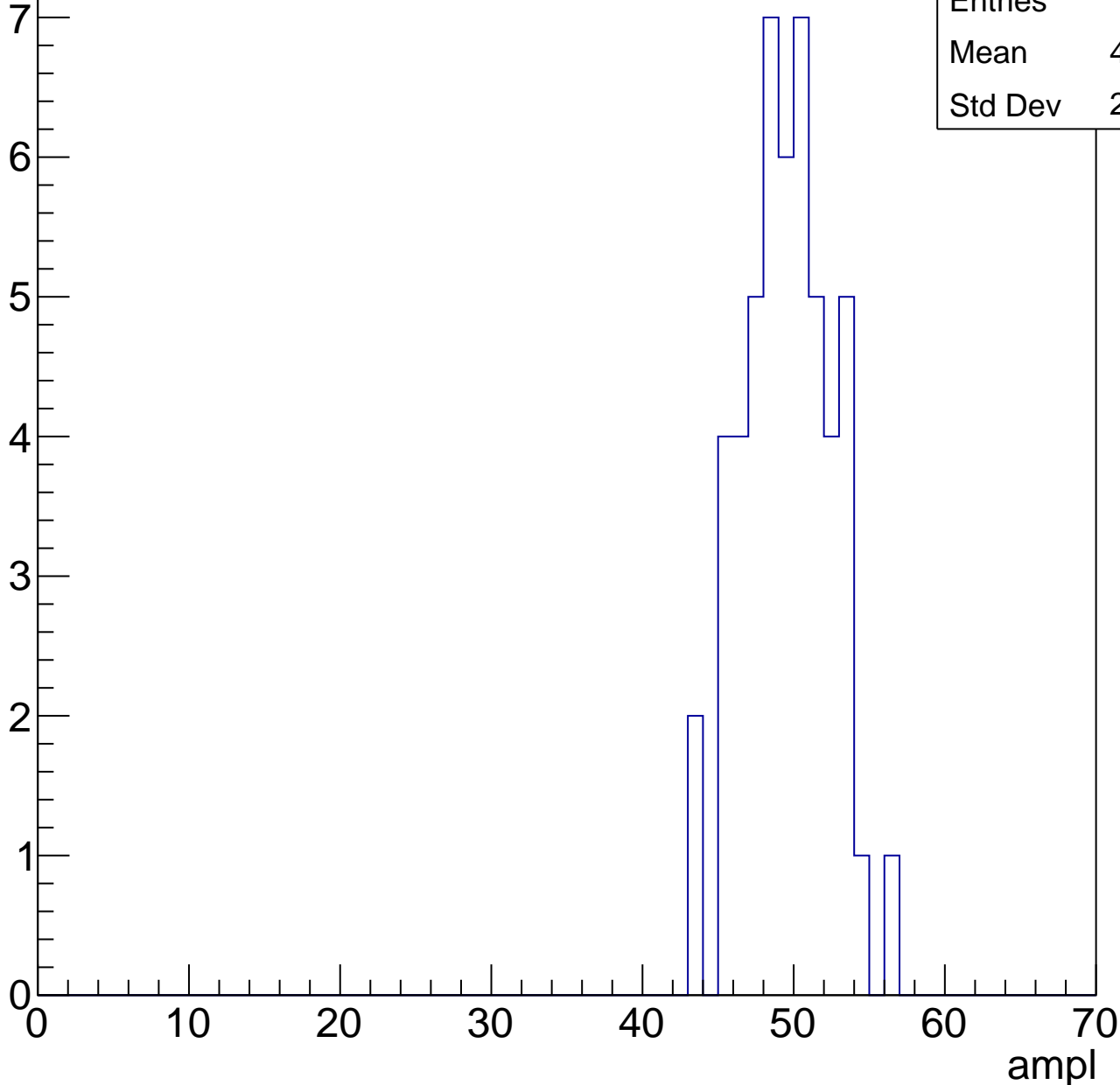


# B1L102S, U5-ch43, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

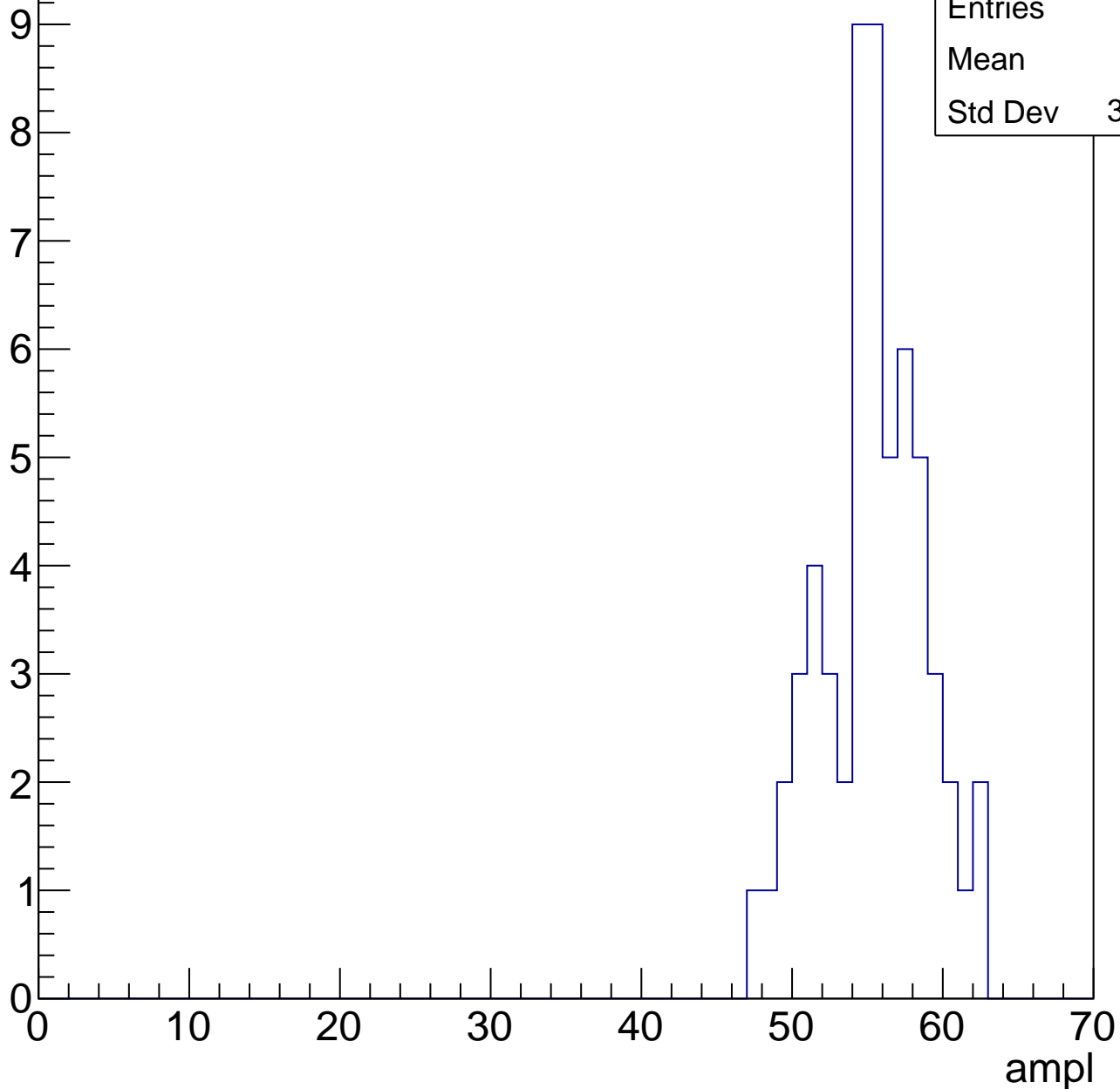
Entries	51
Mean	49.08
Std Dev	2.855



# B1L102S, U5-ch43, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



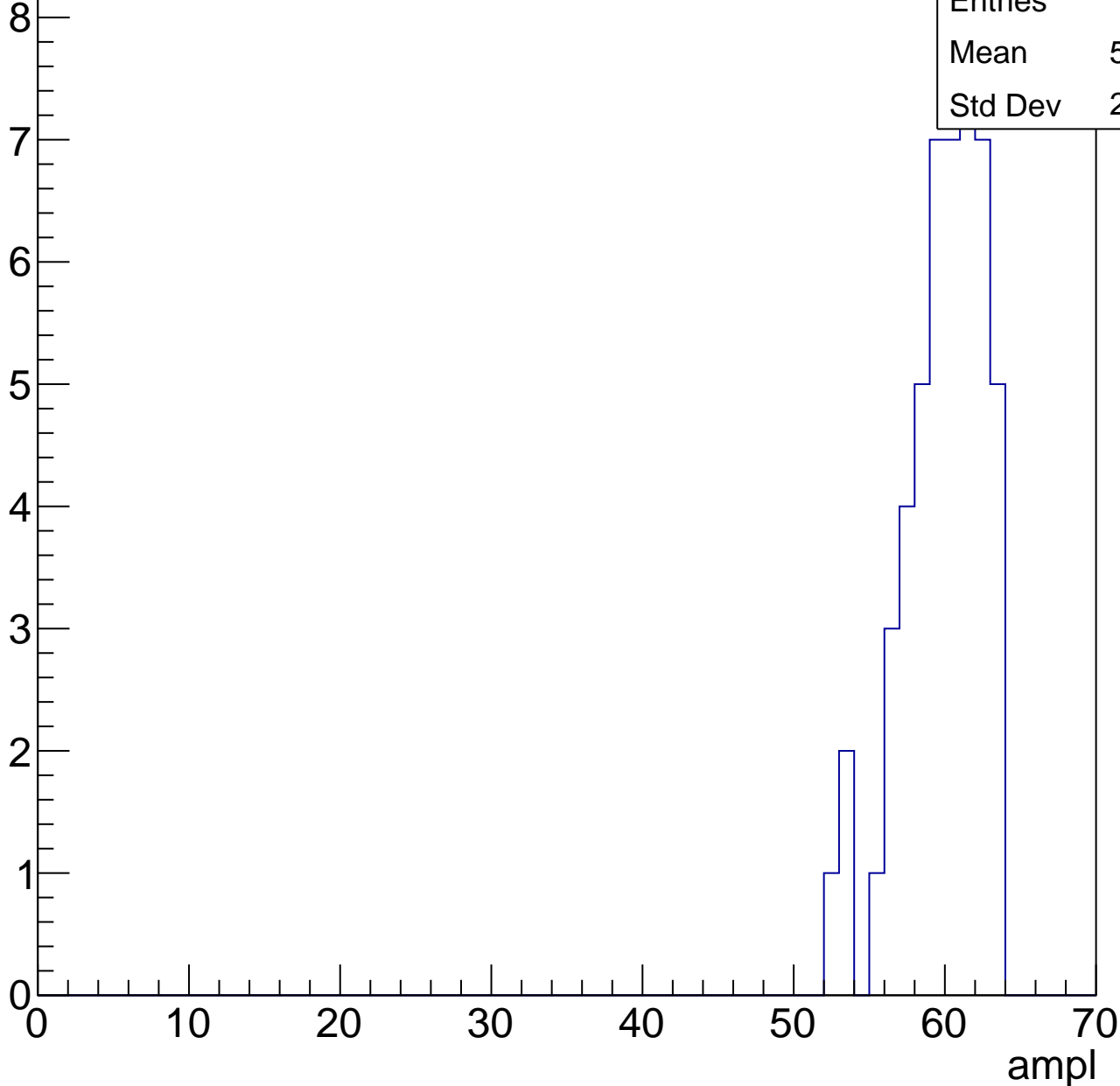
Entries	58
Mean	54.9
Std Dev	3.407

# B1L102S, U5-ch43, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	59.38
Std Dev	2.682

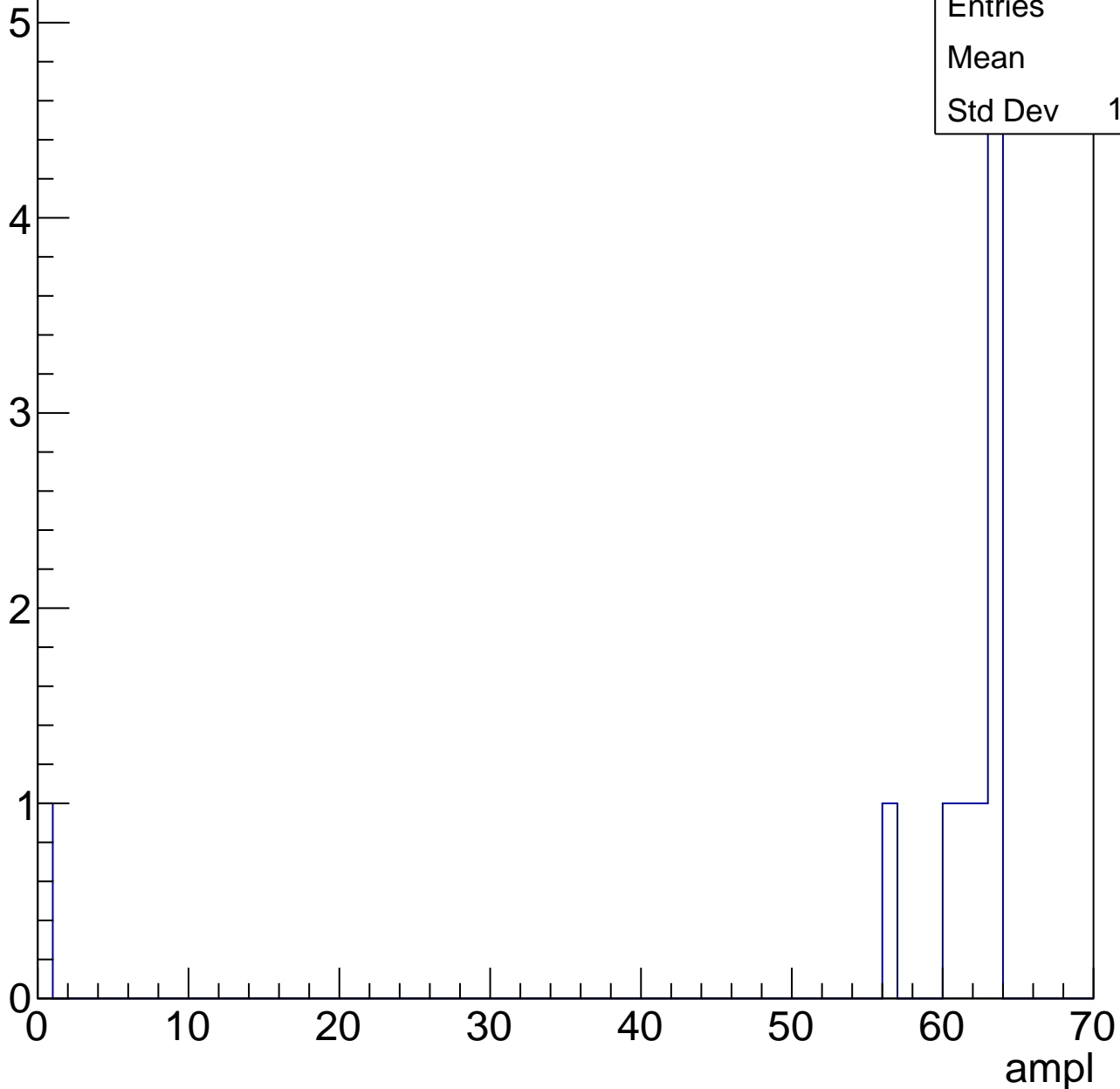


# B1L102S, U5-ch43, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	10
Mean	55.4
Std Dev	18.59





# B1L102S, U5-ch43, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L102S, U5-ch44, adc0

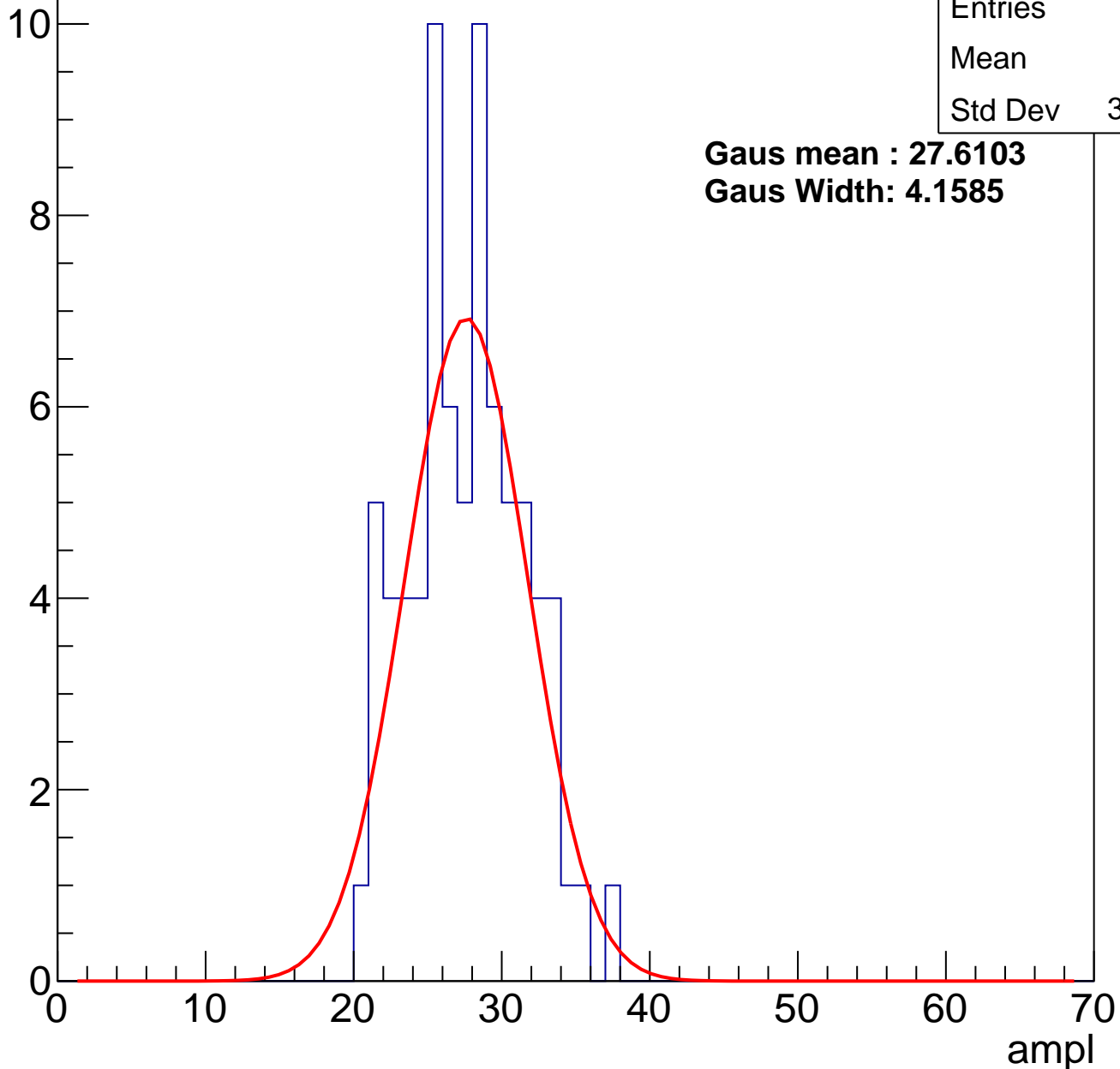
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	76
Mean	27.2
Std Dev	3.784

**Gaus mean : 27.6103**

**Gaus Width: 4.1585**

Entry



# B1L102S, U5-ch44, adc1

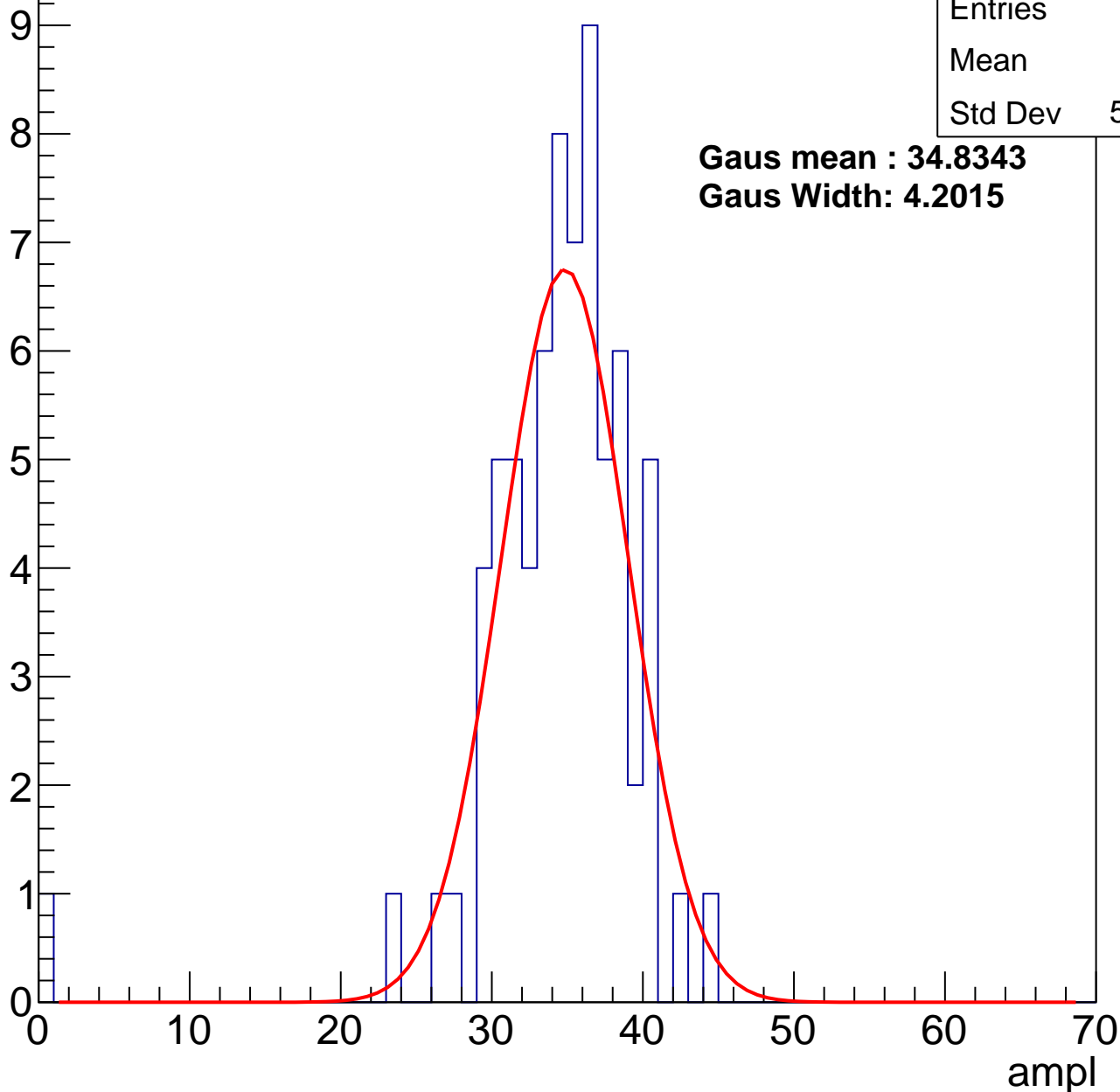
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	33.9
Std Dev	5.546

**Gaus mean : 34.8343**

**Gaus Width: 4.2015**



# B1L102S, U5-ch44, adc2

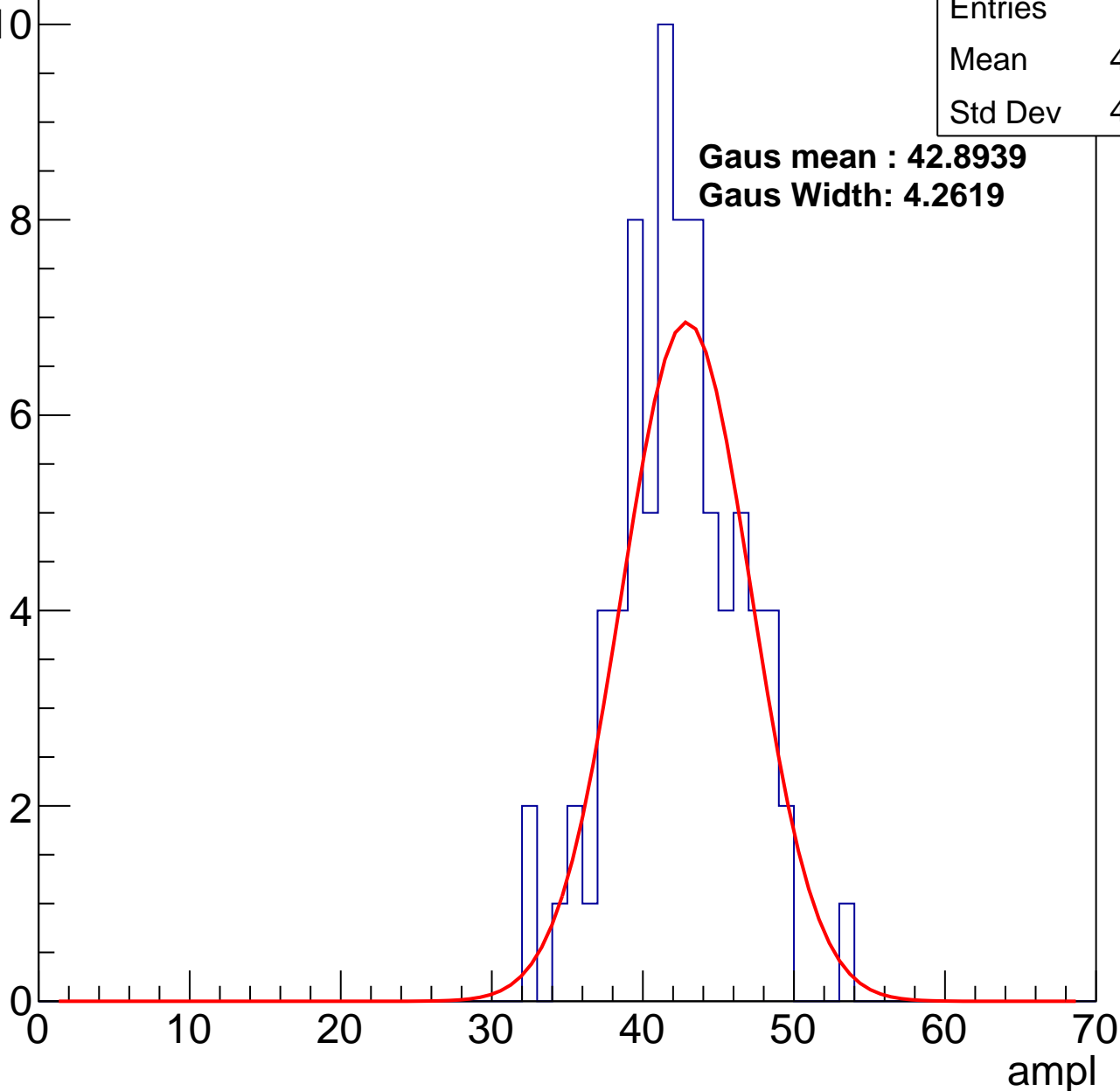
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	78
Mean	41.88
Std Dev	4.035

**Gaus mean : 42.8939**

**Gaus Width: 4.2619**

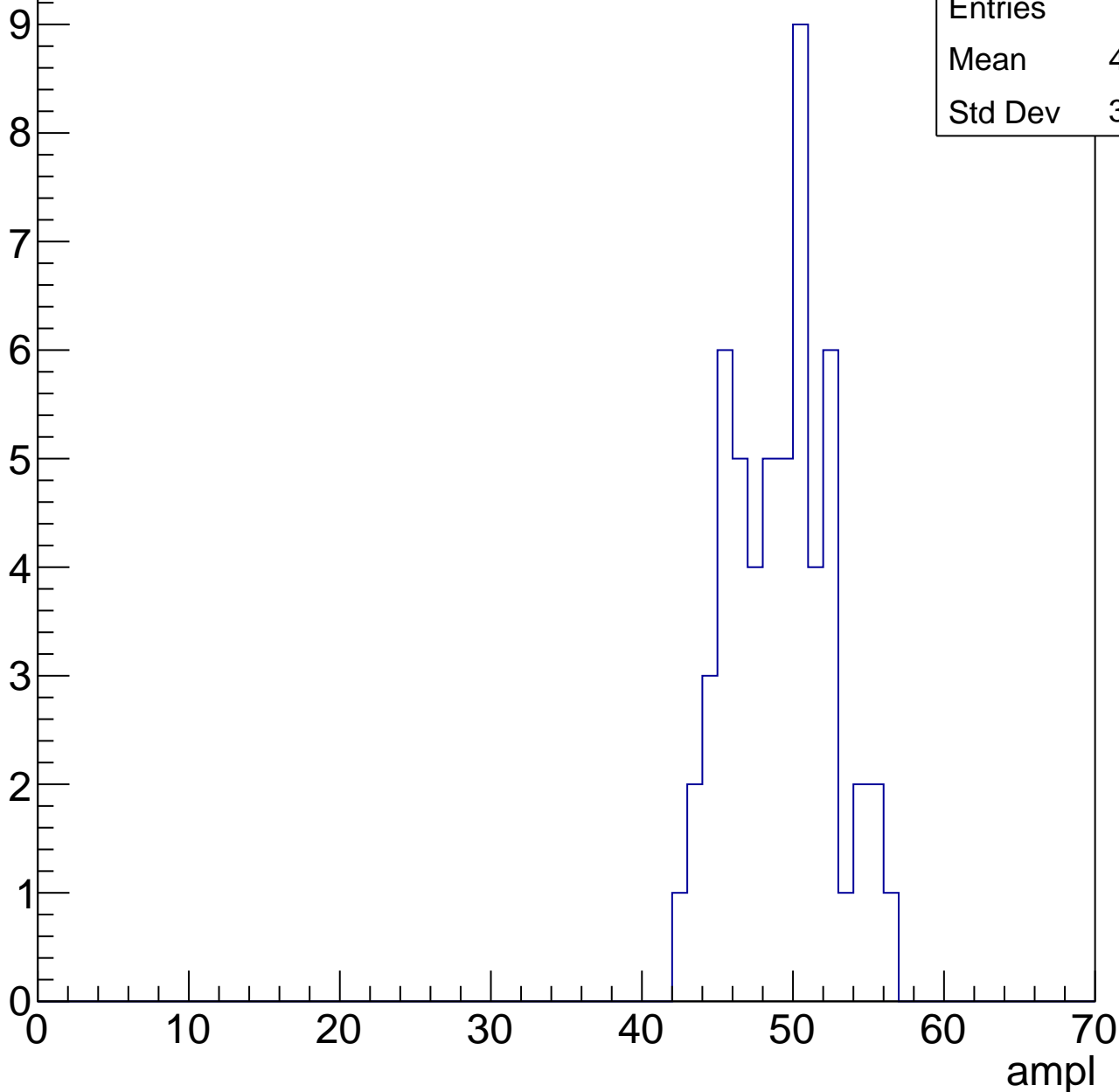


# B1L102S, U5-ch44, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

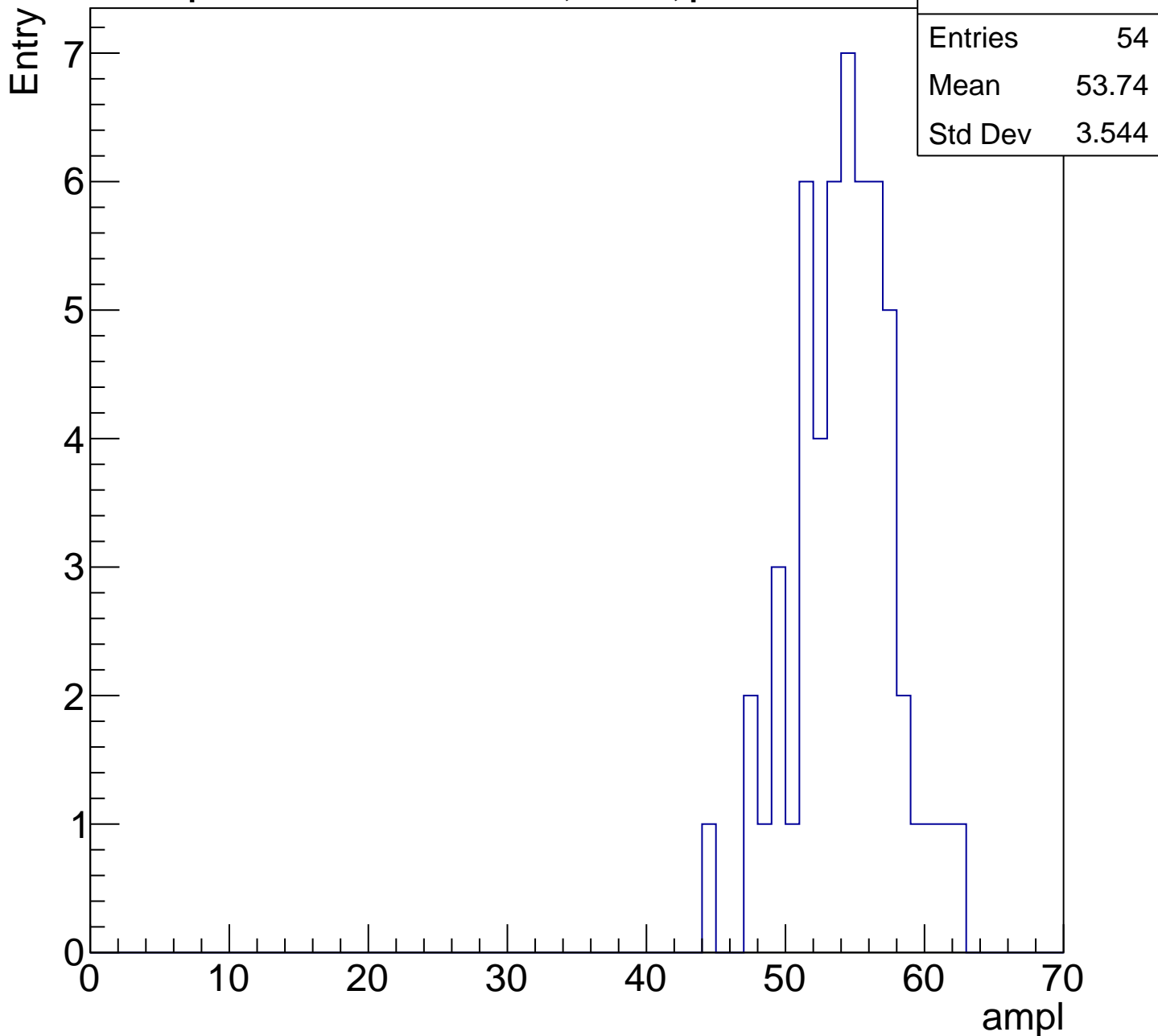
Entry

Entries	56
Mean	48.68
Std Dev	3.323



# B1L102S, U5-ch44, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2



# B1L102S, U5-ch44, adc5

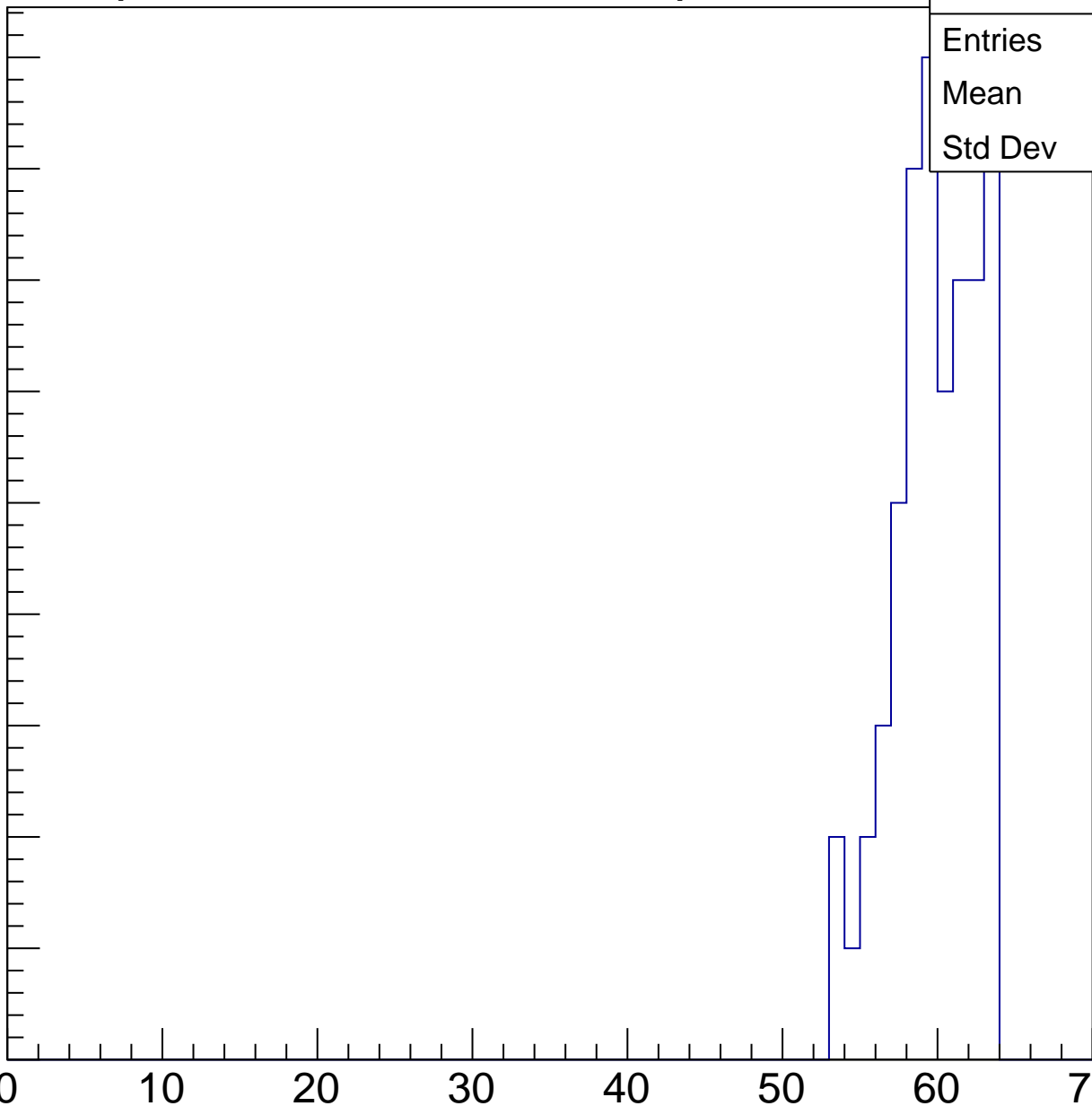
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	58
Mean	59.36
Std Dev	2.631

ampl



# B1L102S, U5-ch44, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries	10
Mean	55.2
Std Dev	18.43



# B1L102S, U5-ch44, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U5-ch45, adc0

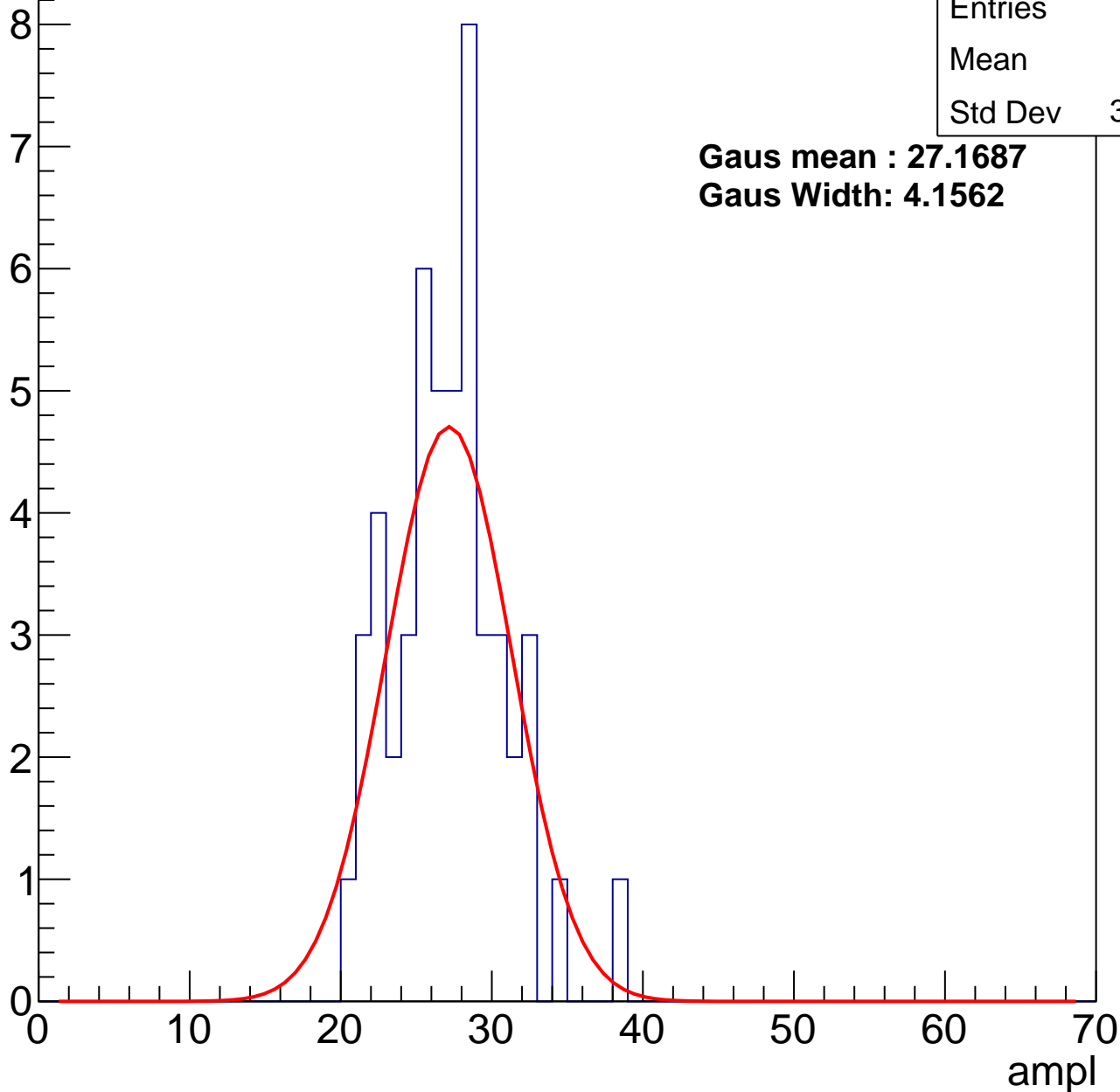
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	26.7
Std Dev	3.646

**Gaus mean : 27.1687**

**Gaus Width: 4.1562**



# B1L102S, U5-ch45, adc1

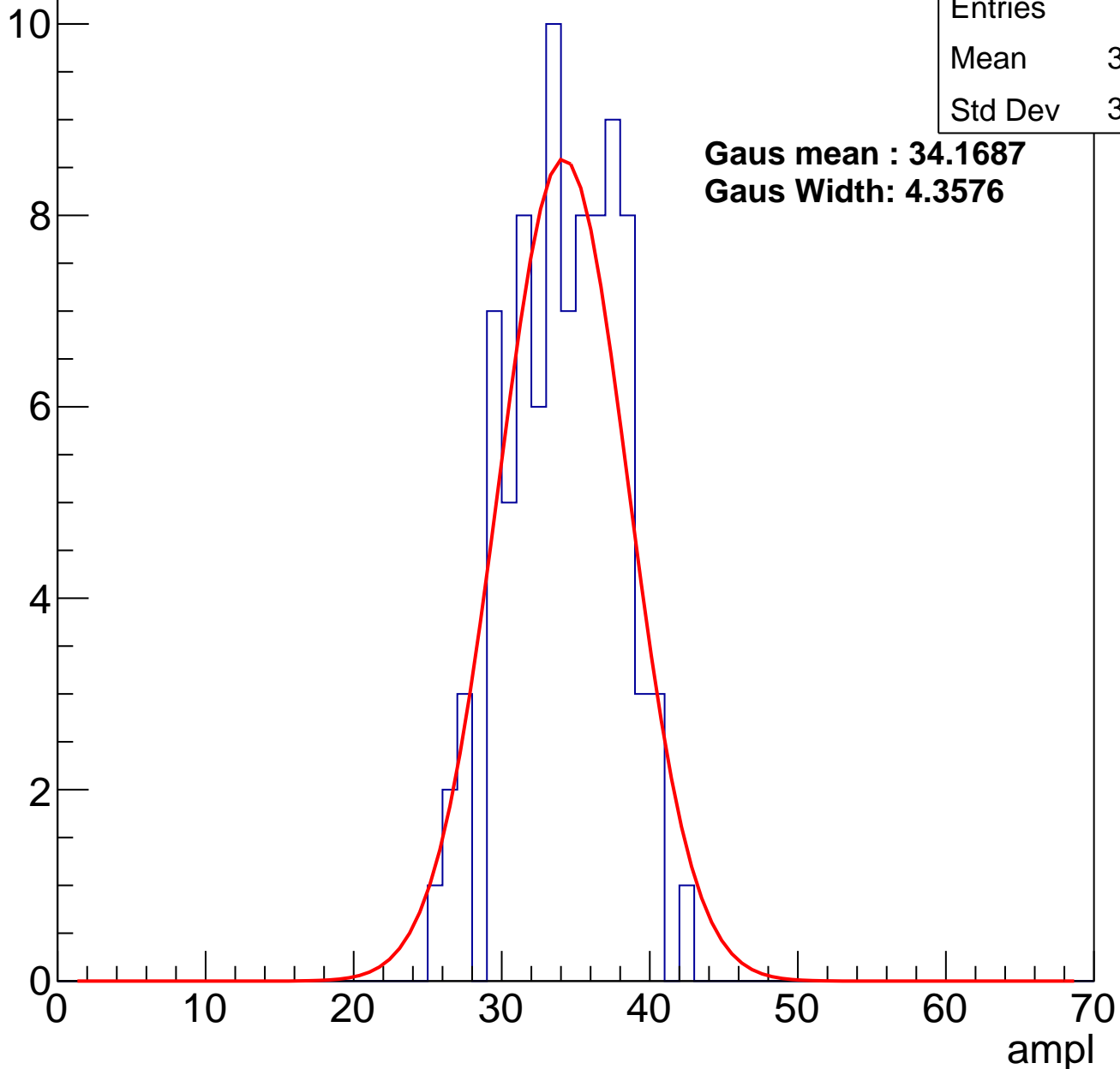
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	89
Mean	33.74
Std Dev	3.683

**Gaus mean : 34.1687**

**Gaus Width: 4.3576**

Entry



# B1L102S, U5-ch45, adc2

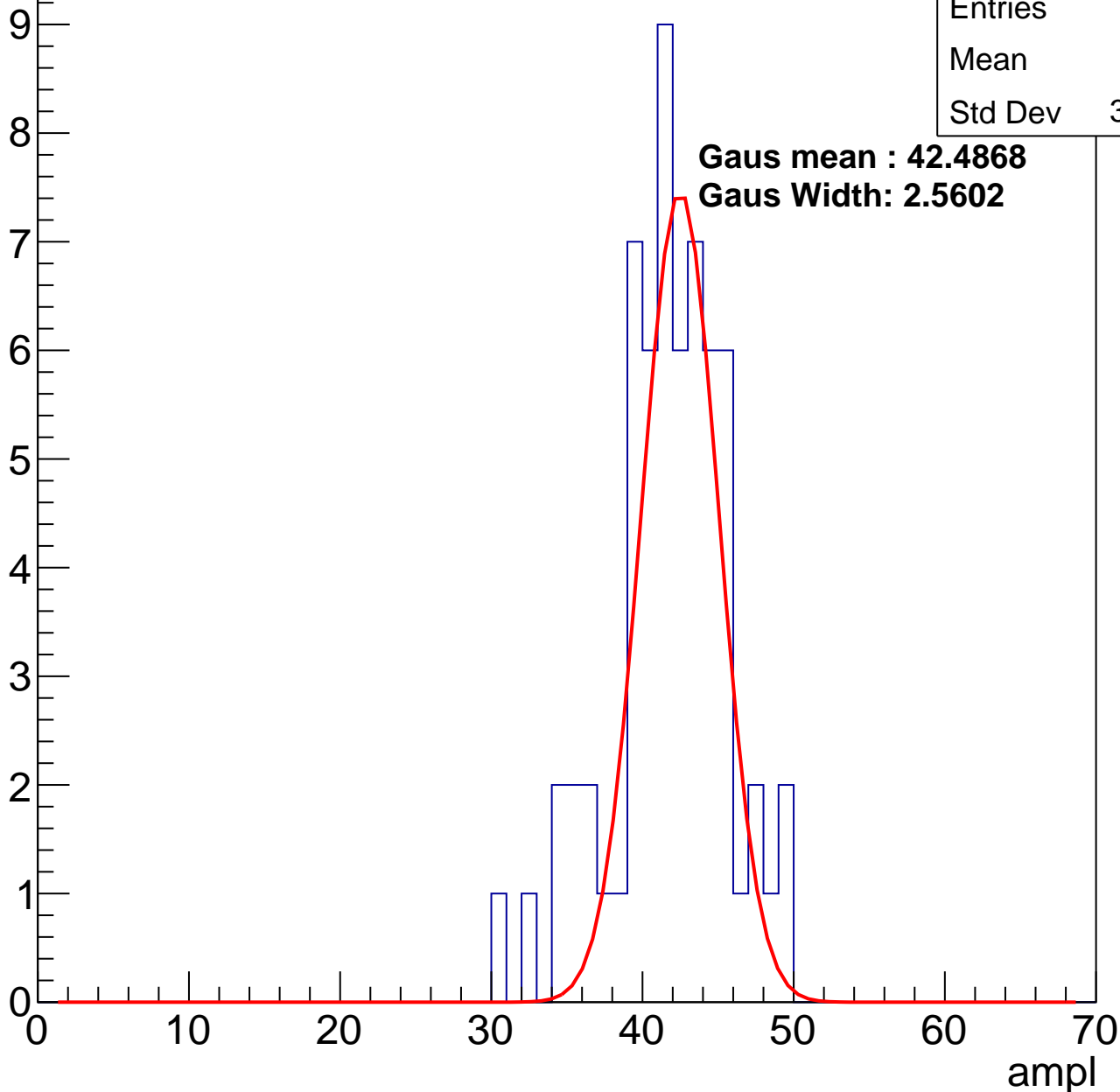
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	41.3
Std Dev	3.849

**Gaus mean : 42.4868**

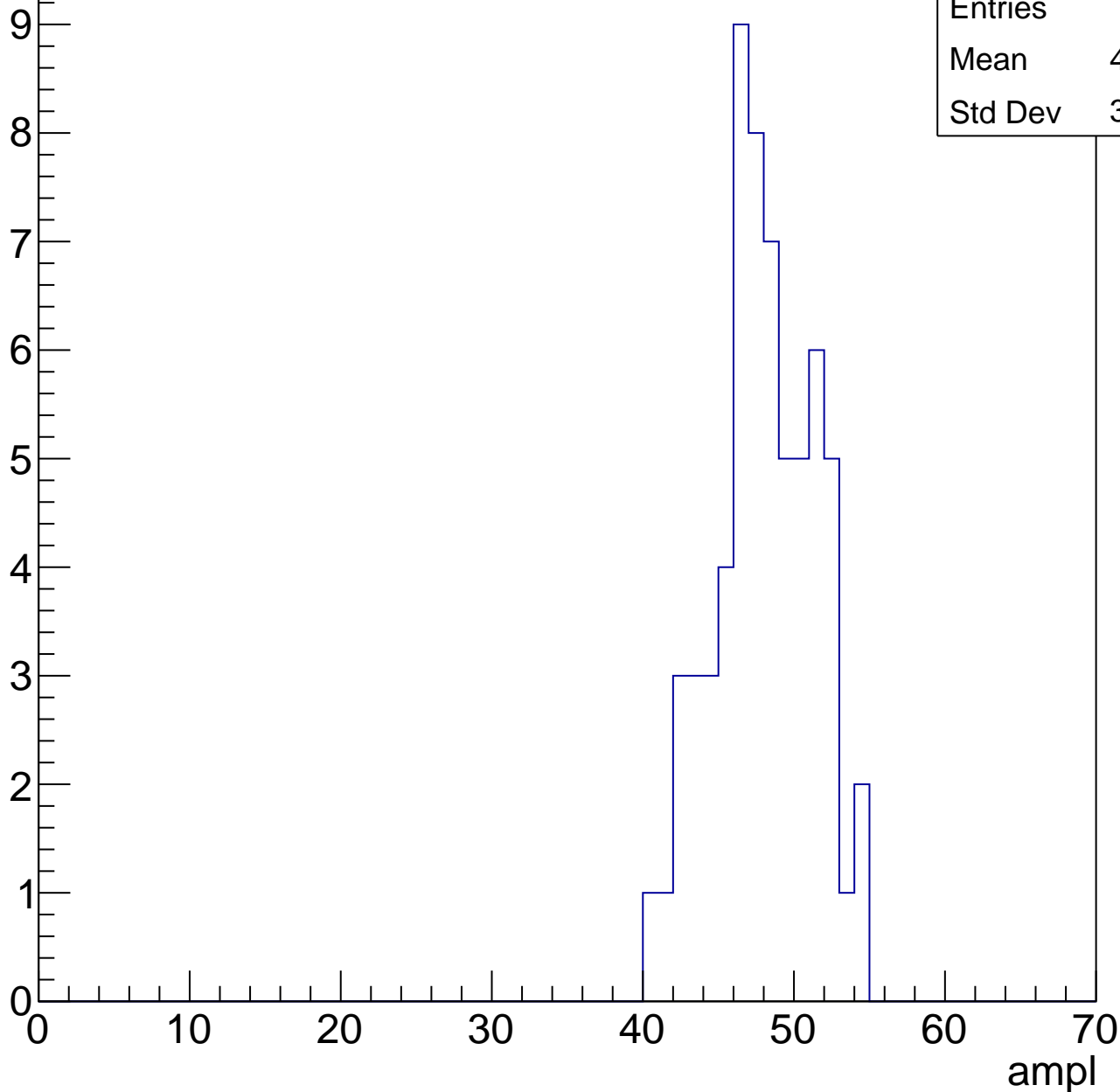
**Gaus Width: 2.5602**



# B1L102S, U5-ch45, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

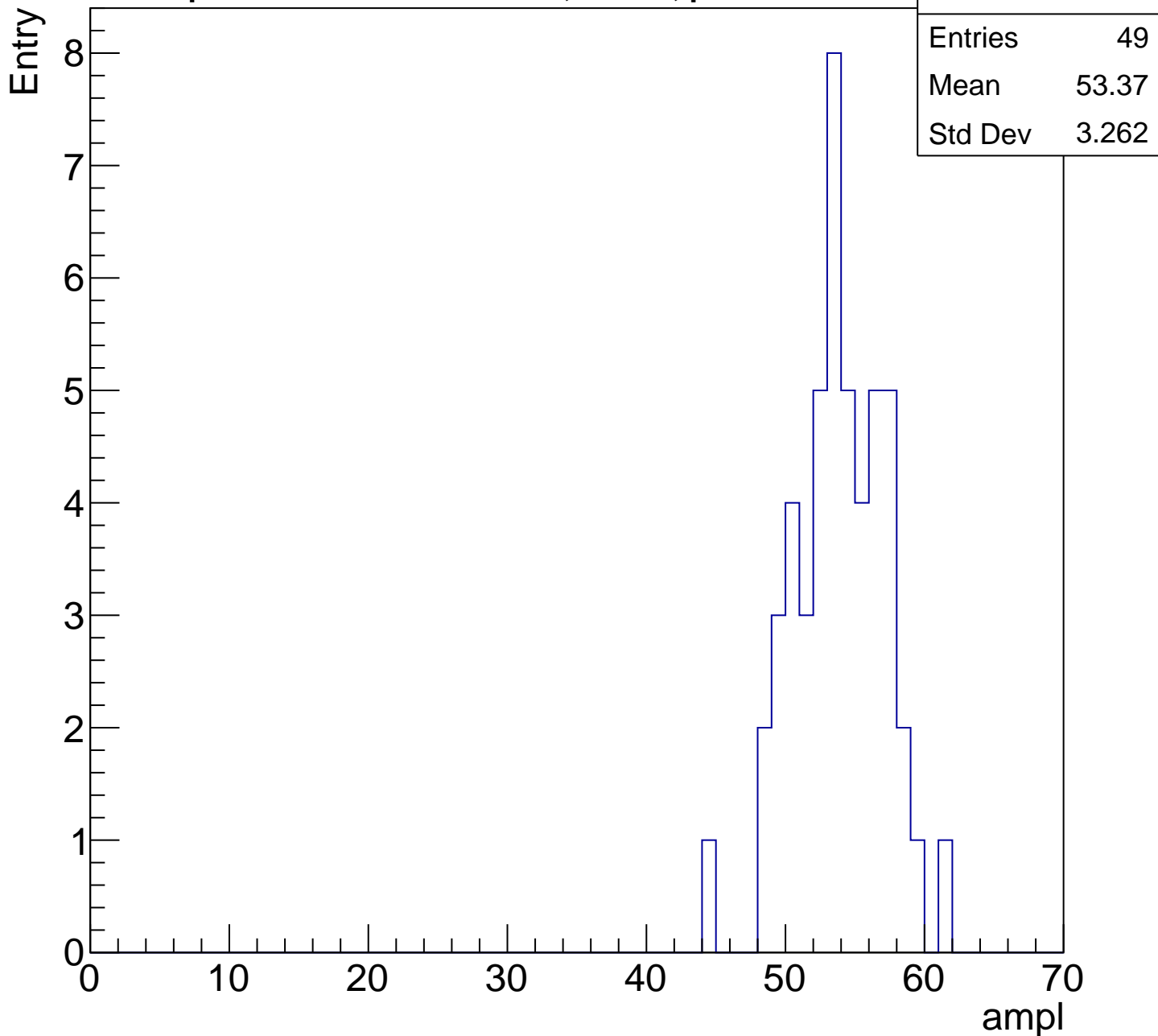
Entry



Entries	63
Mean	47.56
Std Dev	3.255

# B1L102S, U5-ch45, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

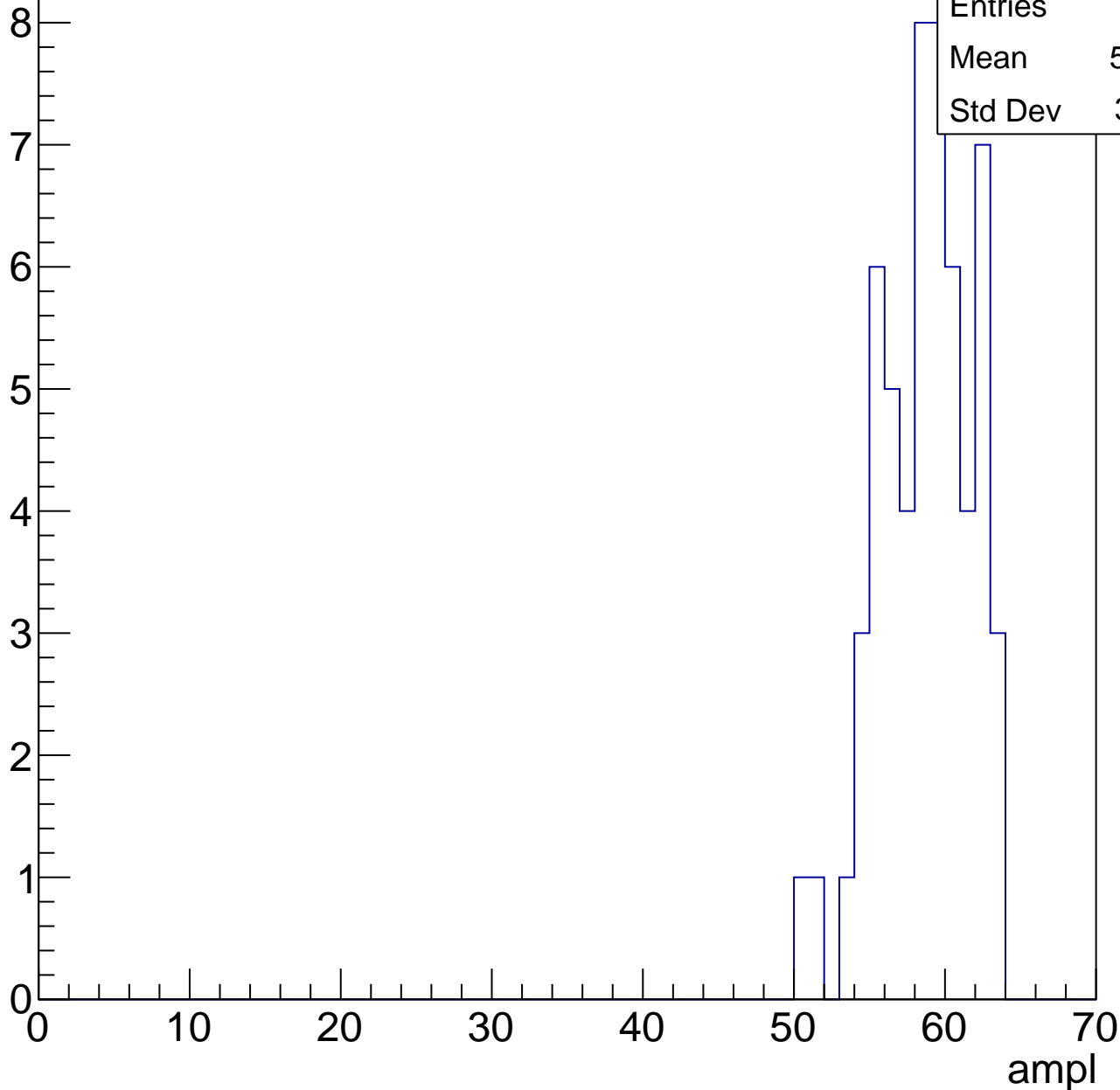


# B1L102S, U5-ch45, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	58.19
Std Dev	3.011

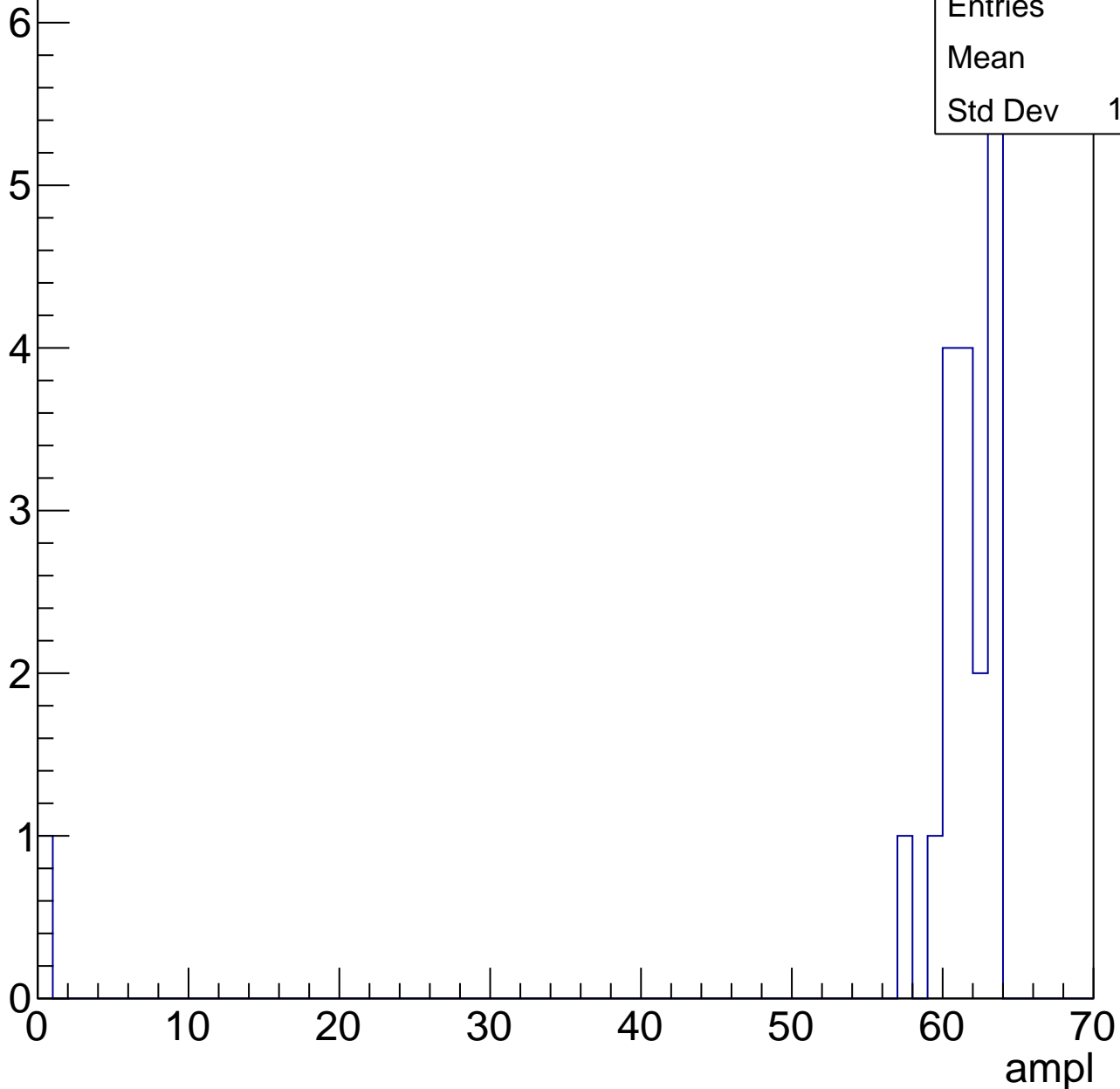


# B1L102S, U5-ch45, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	19
Mean	58
Std Dev	13.76

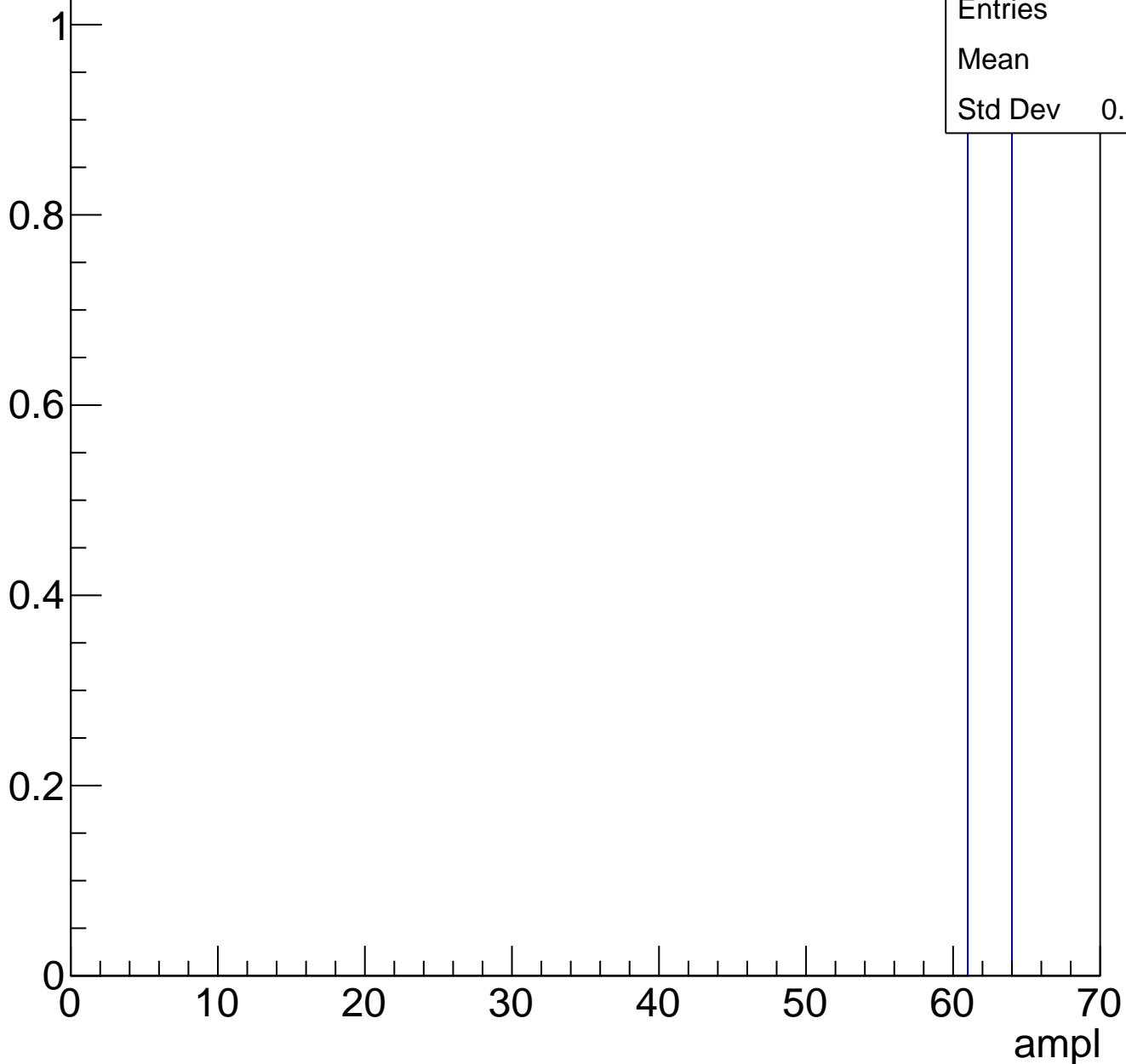




# B1L102S, U5-ch45, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U5-ch46, adc0

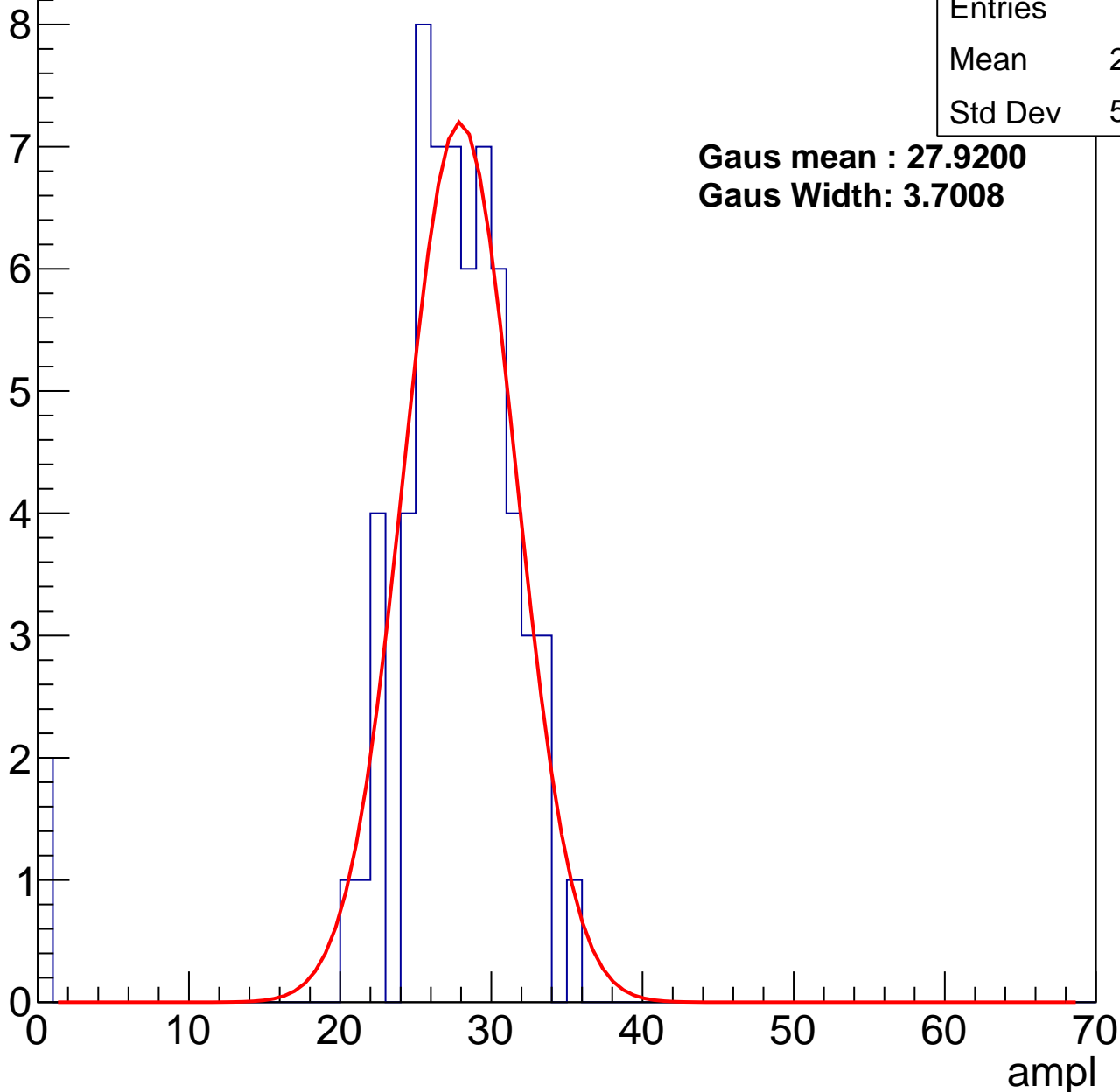
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	26.58
Std Dev	5.736

**Gaus mean : 27.9200**

**Gaus Width: 3.7008**



# B1L102S, U5-ch46, adc1

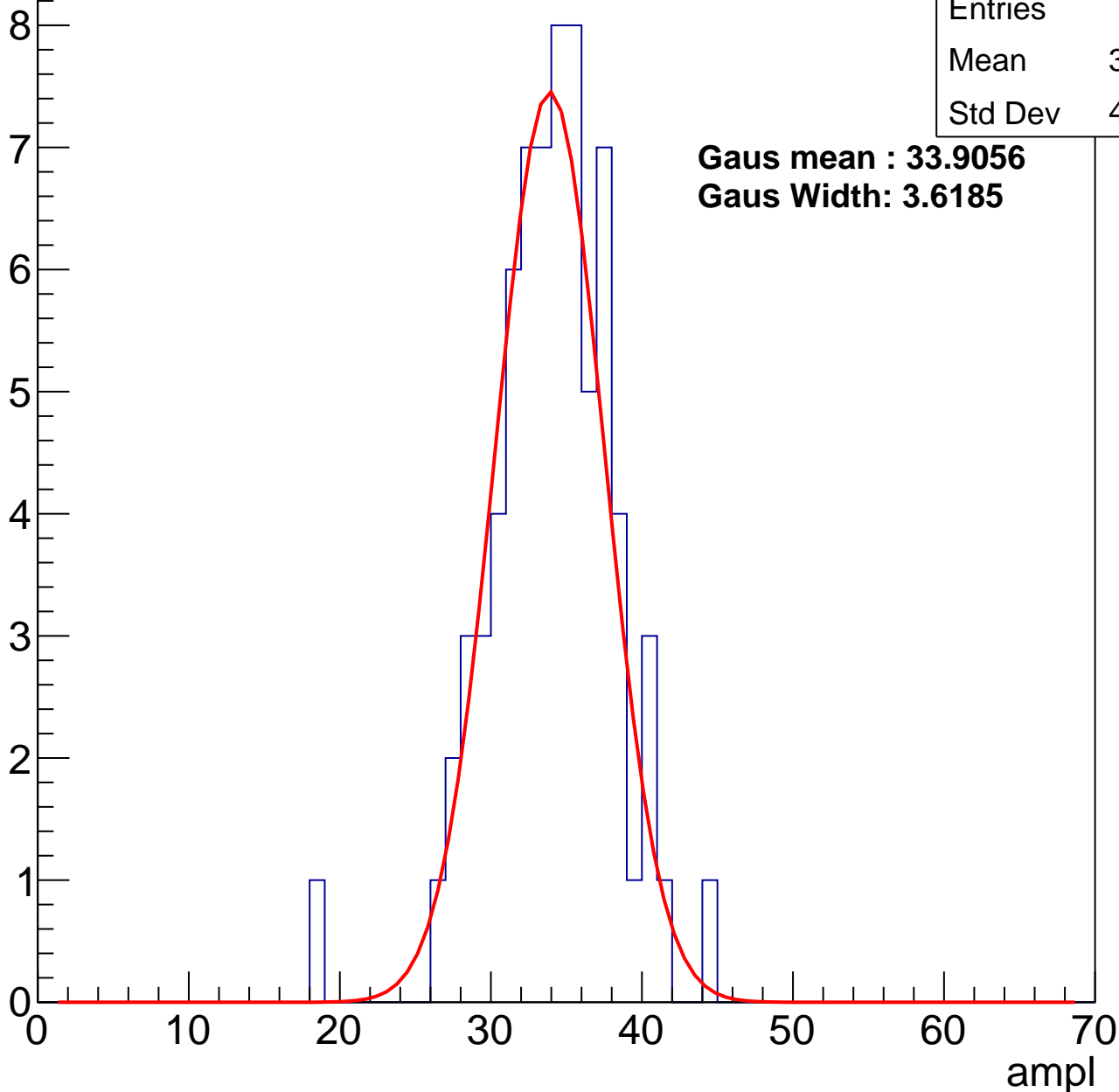
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	33.57
Std Dev	4.044

**Gaus mean : 33.9056**

**Gaus Width: 3.6185**



# B1L102S, U5-ch46, adc2

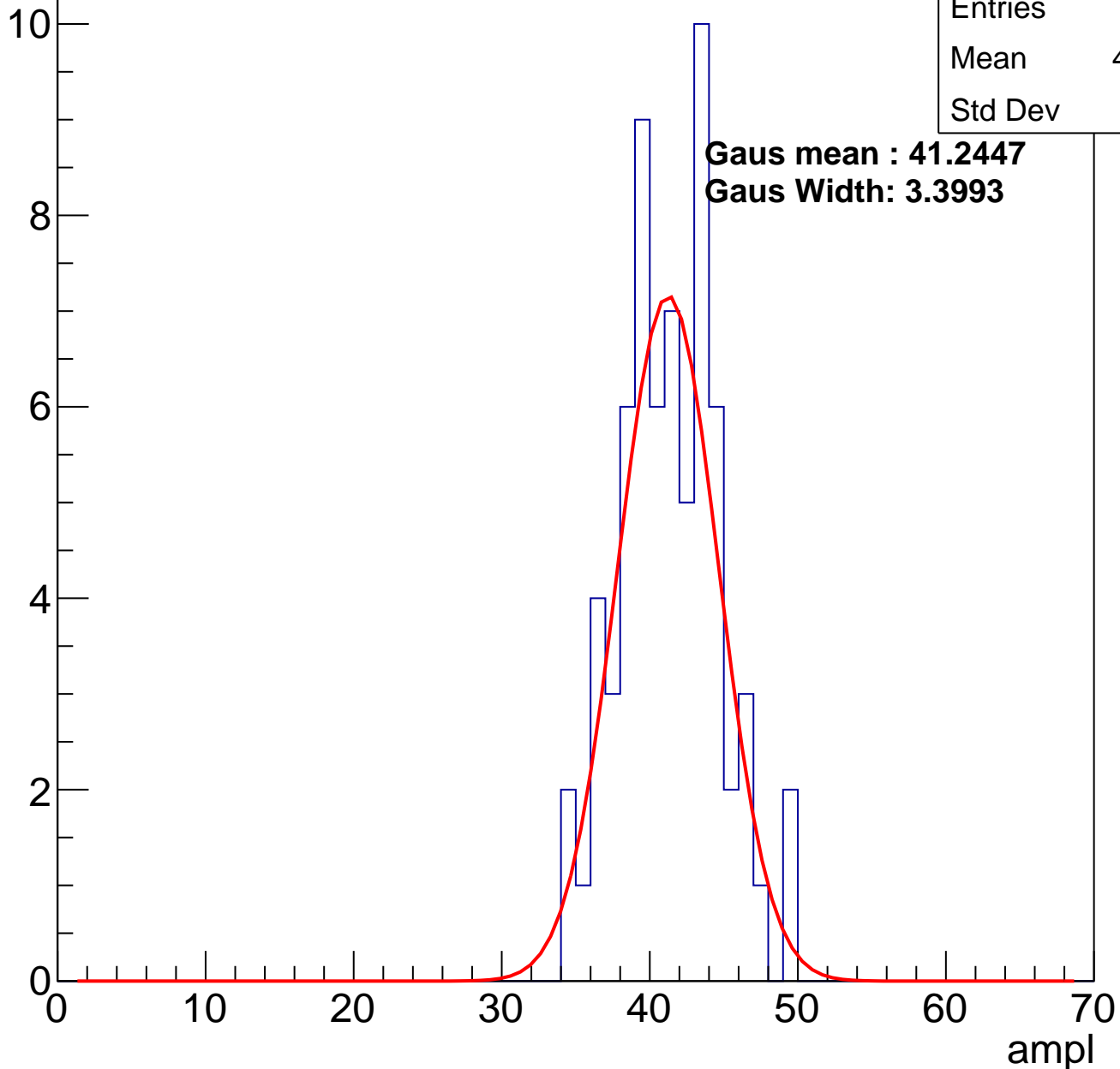
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	67
Mean	40.91
Std Dev	3.34

**Gaus mean : 41.2447**

**Gaus Width: 3.3993**

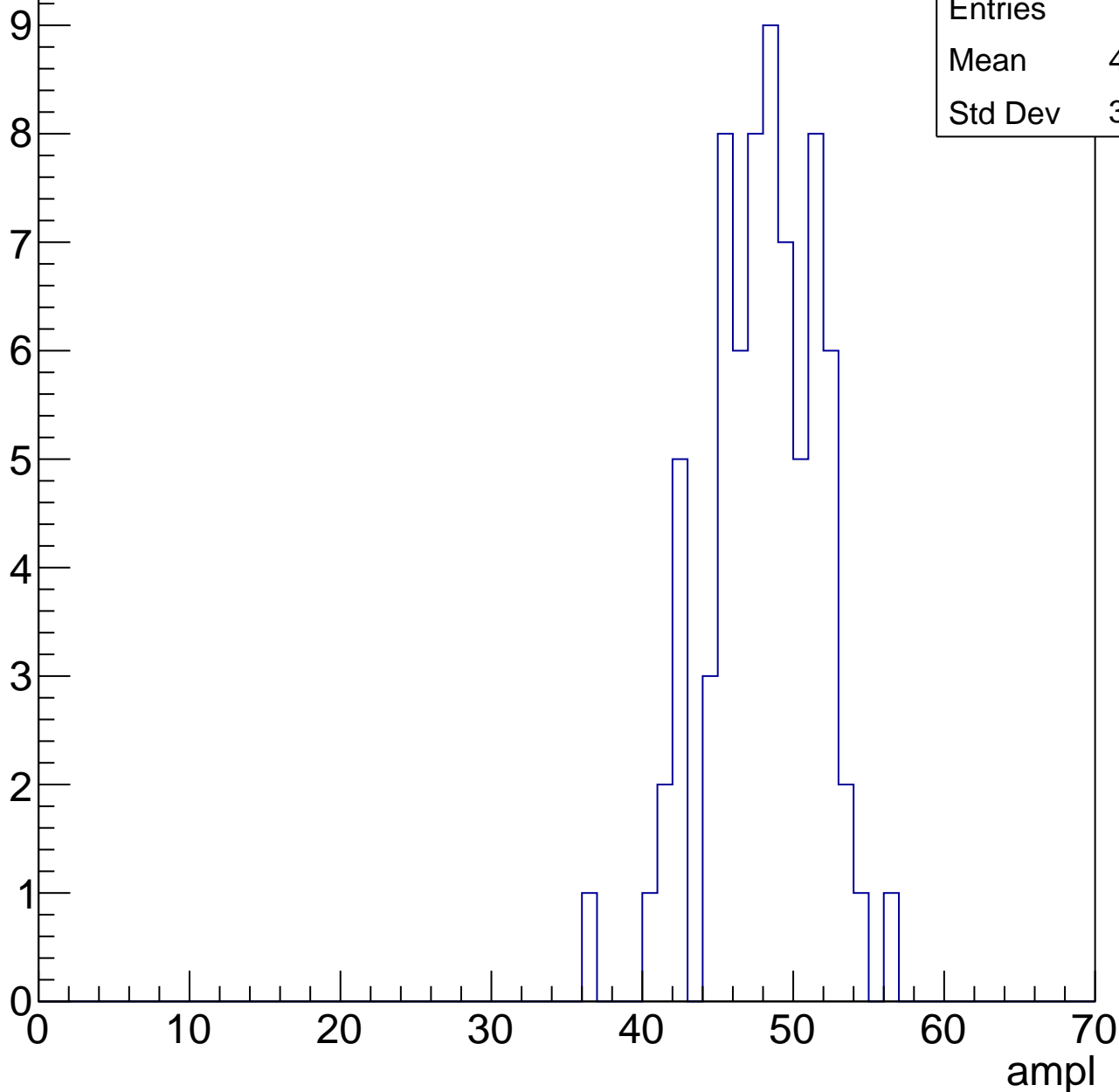
Entry



# B1L102S, U5-ch46, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

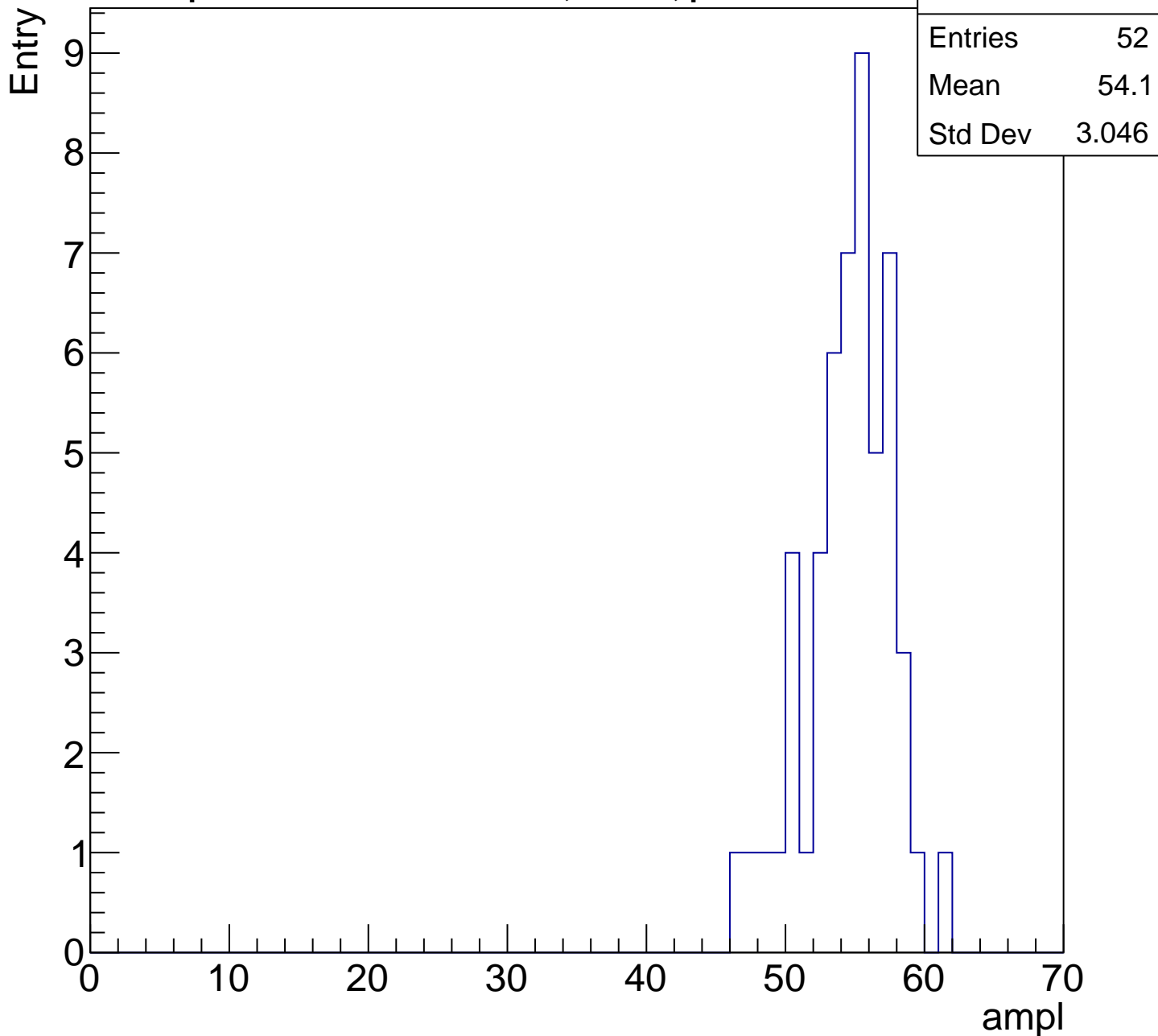
Entry



Entries	73
Mean	47.58
Std Dev	3.645

# B1L102S, U5-ch46, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2



# B1L102S, U5-ch46, adc5

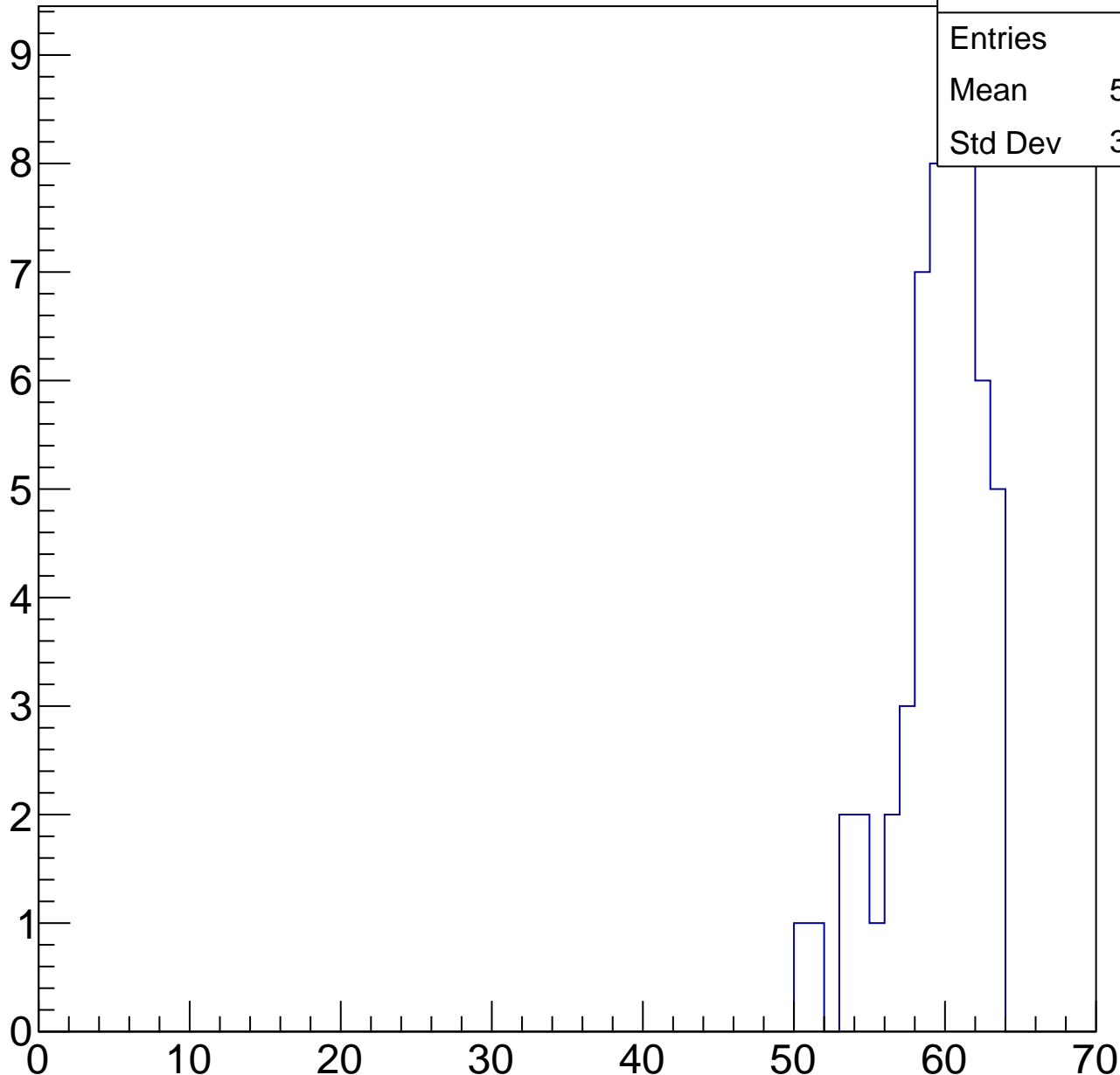
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	55
Mean	59.04
Std Dev	3.009

ampl

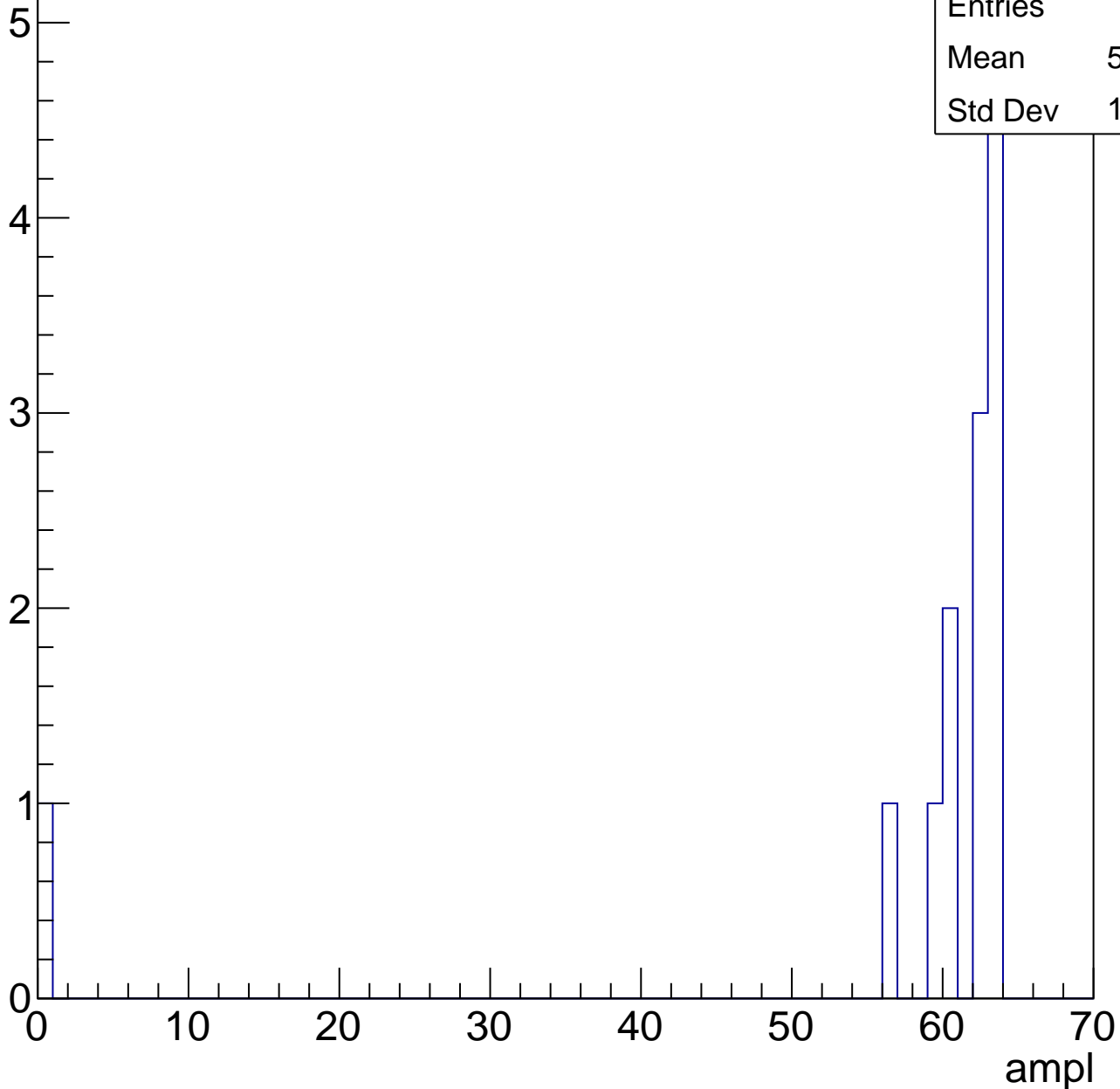


# B1L102S, U5-ch46, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	13
Mean	56.62
Std Dev	16.47

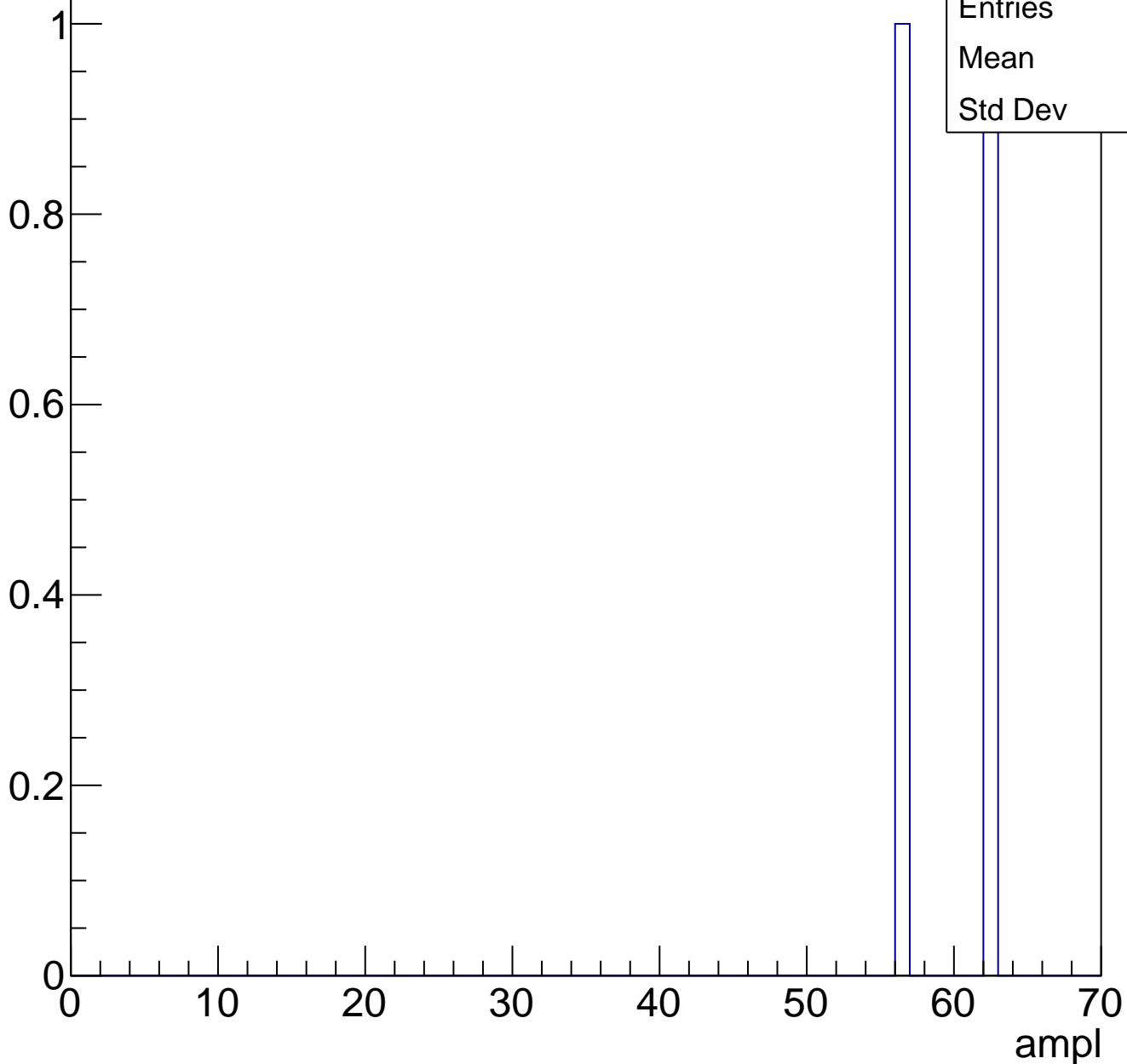




# B1L102S, U5-ch46, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U5-ch47, adc0

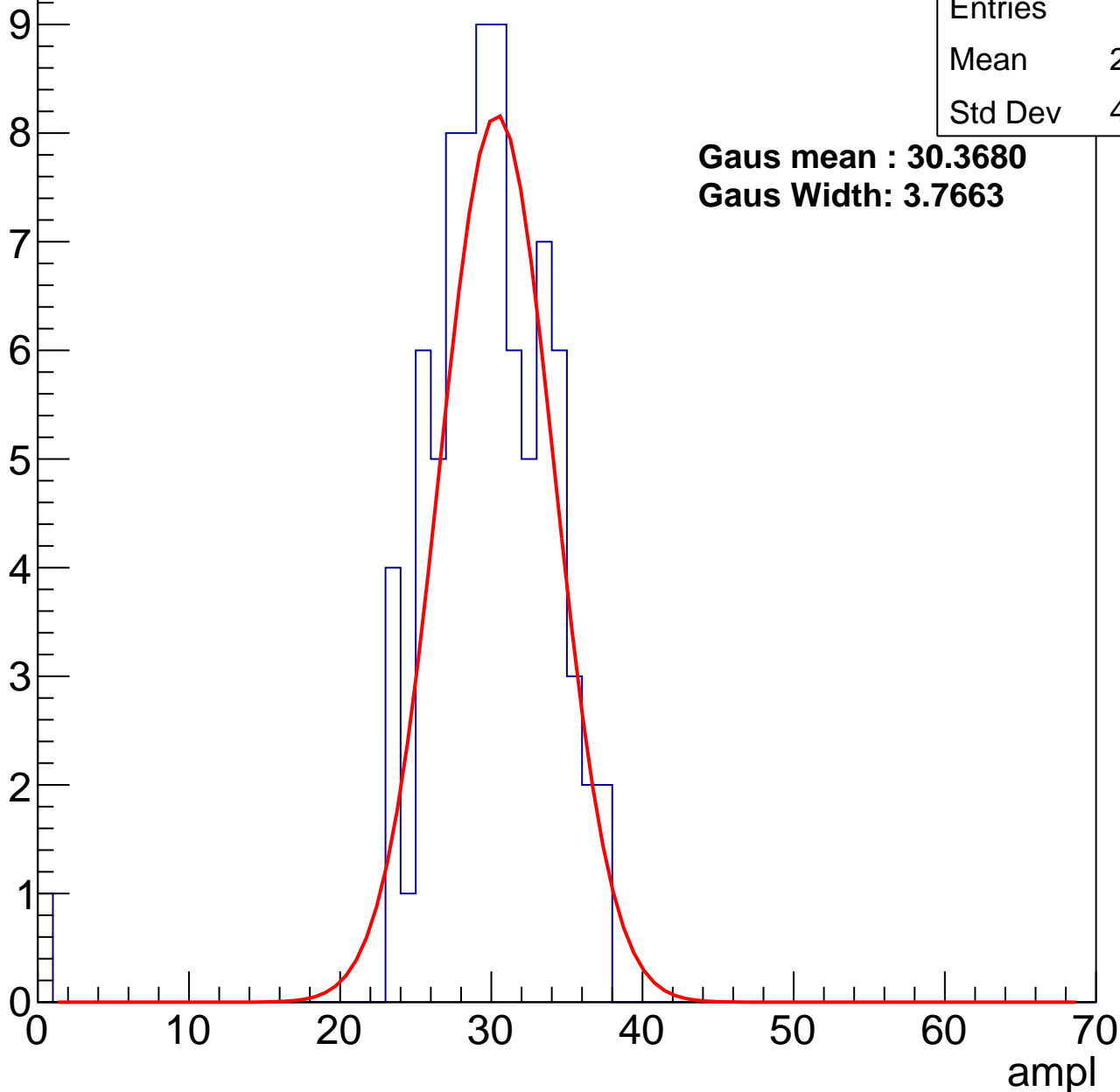
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	82
Mean	29.26
Std Dev	4.762

**Gaus mean : 30.3680**

**Gaus Width: 3.7663**



# B1L102S, U5-ch47, adc1

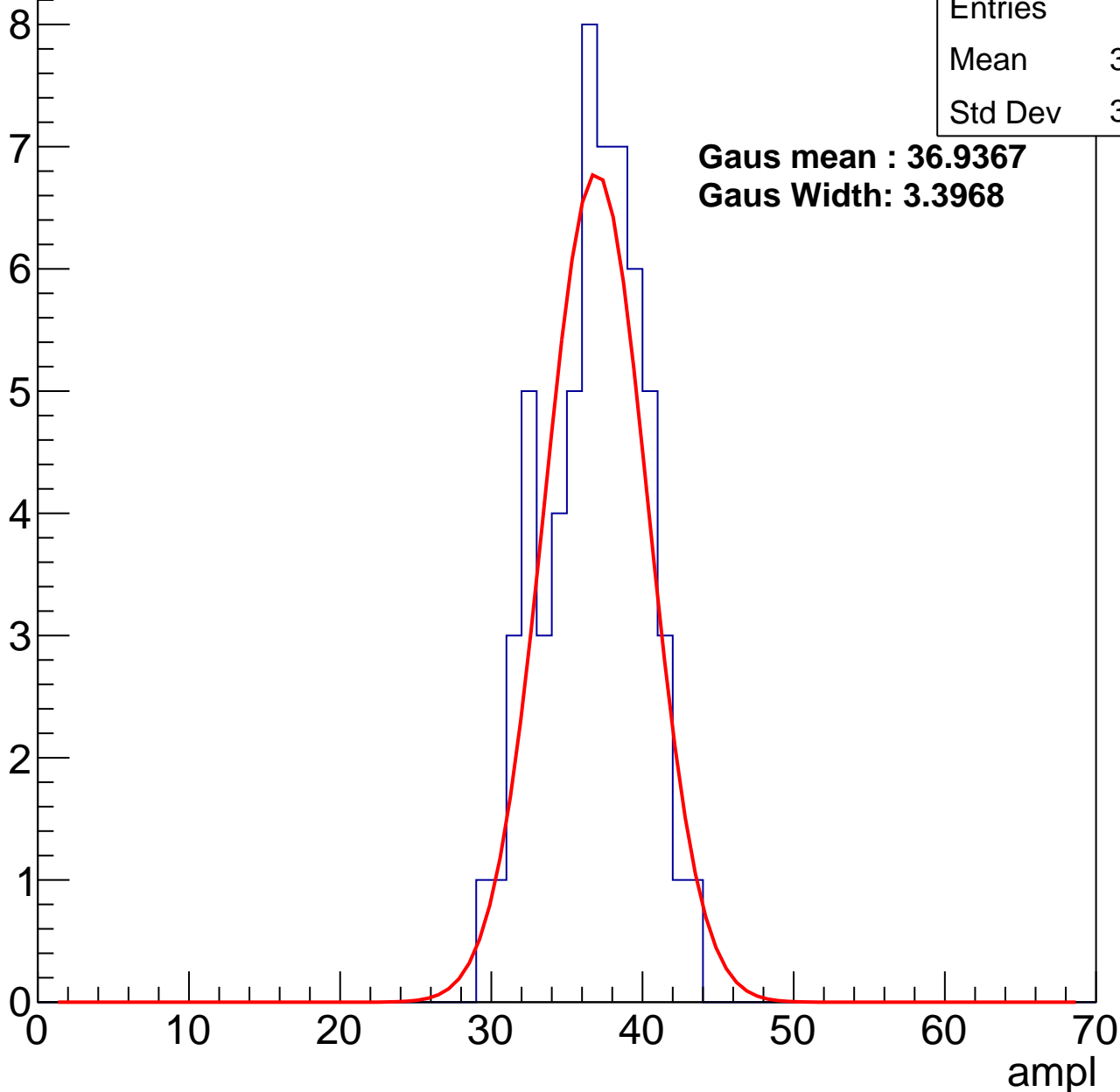
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	36.28
Std Dev	3.194

**Gaus mean : 36.9367**

**Gaus Width: 3.3968**



# B1L102S, U5-ch47, adc2

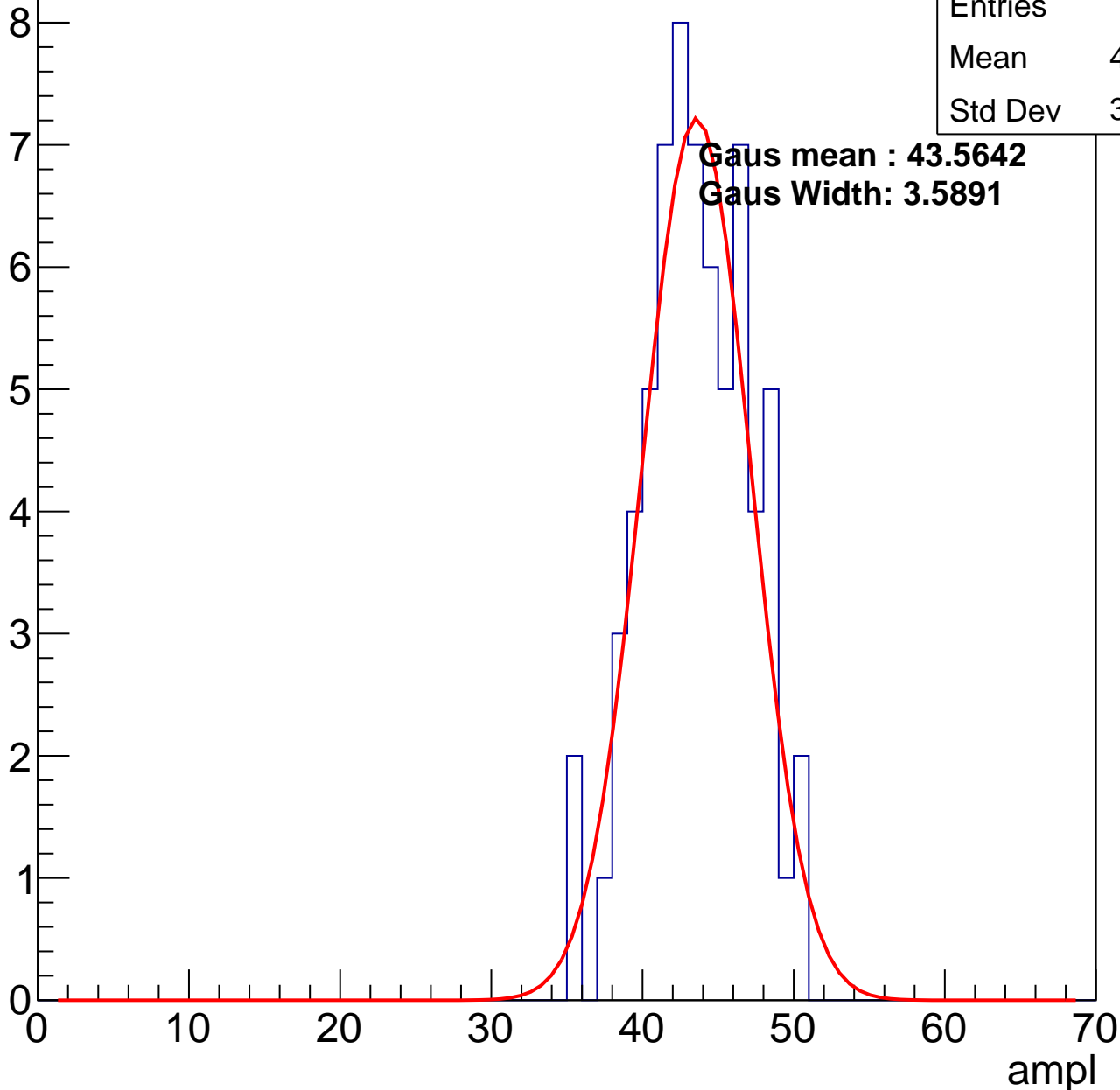
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	43.12
Std Dev	3.445

**Gaus mean : 43.5642**

**Gaus Width: 3.5891**

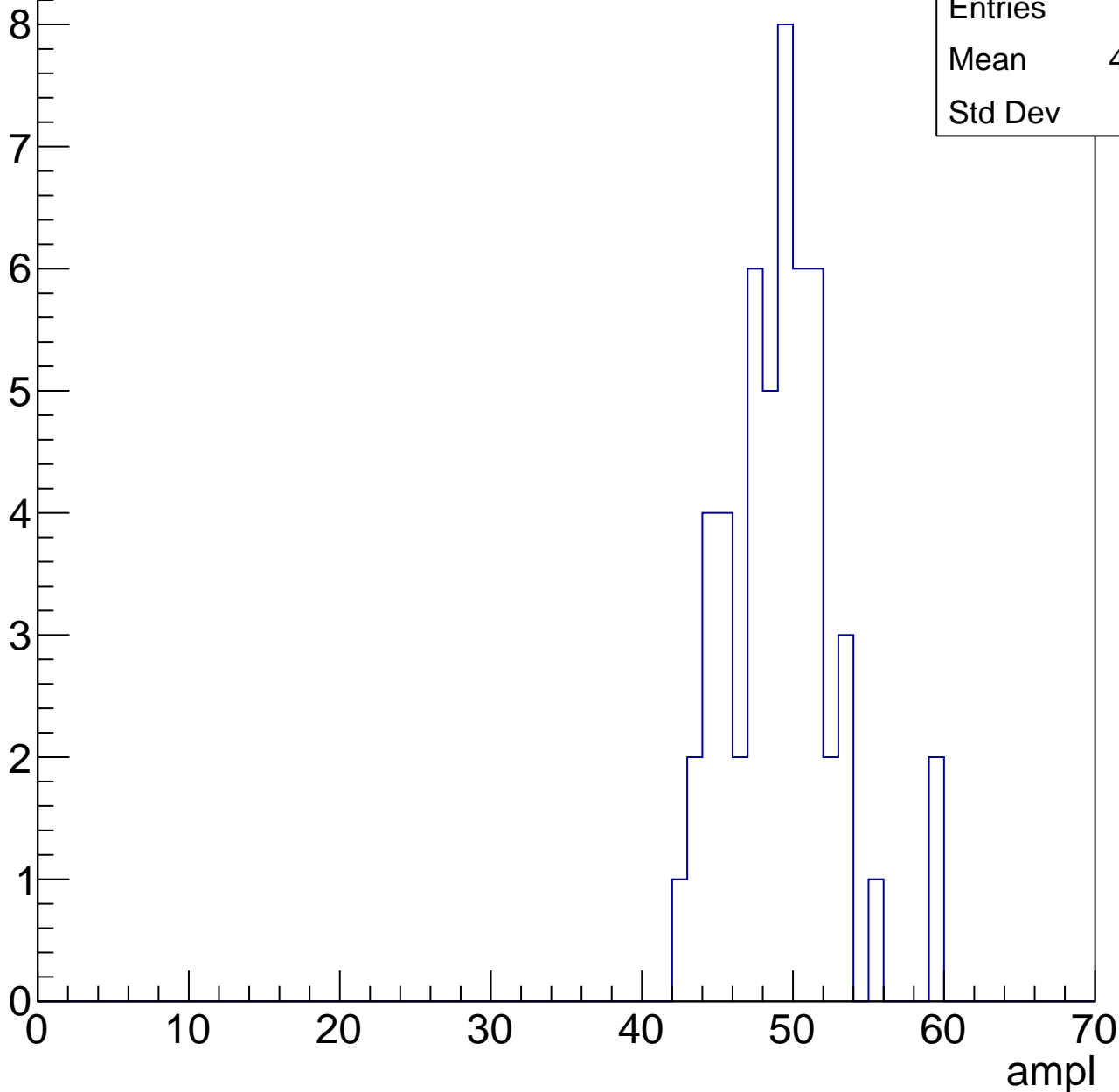


# B1L102S, U5-ch47, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	48.69
Std Dev	3.56

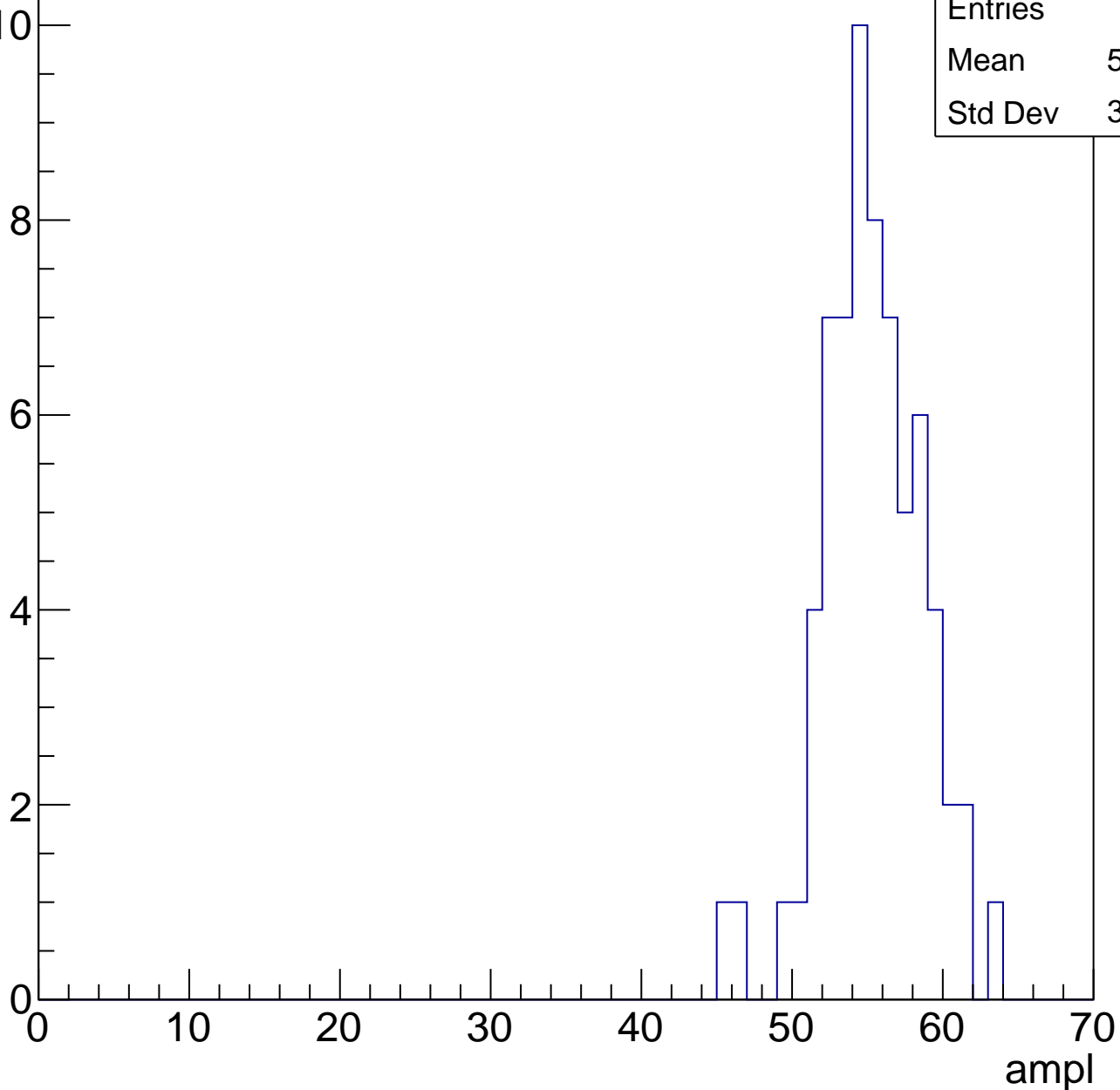


# B1L102S, U5-ch47, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	54.85
Std Dev	3.316

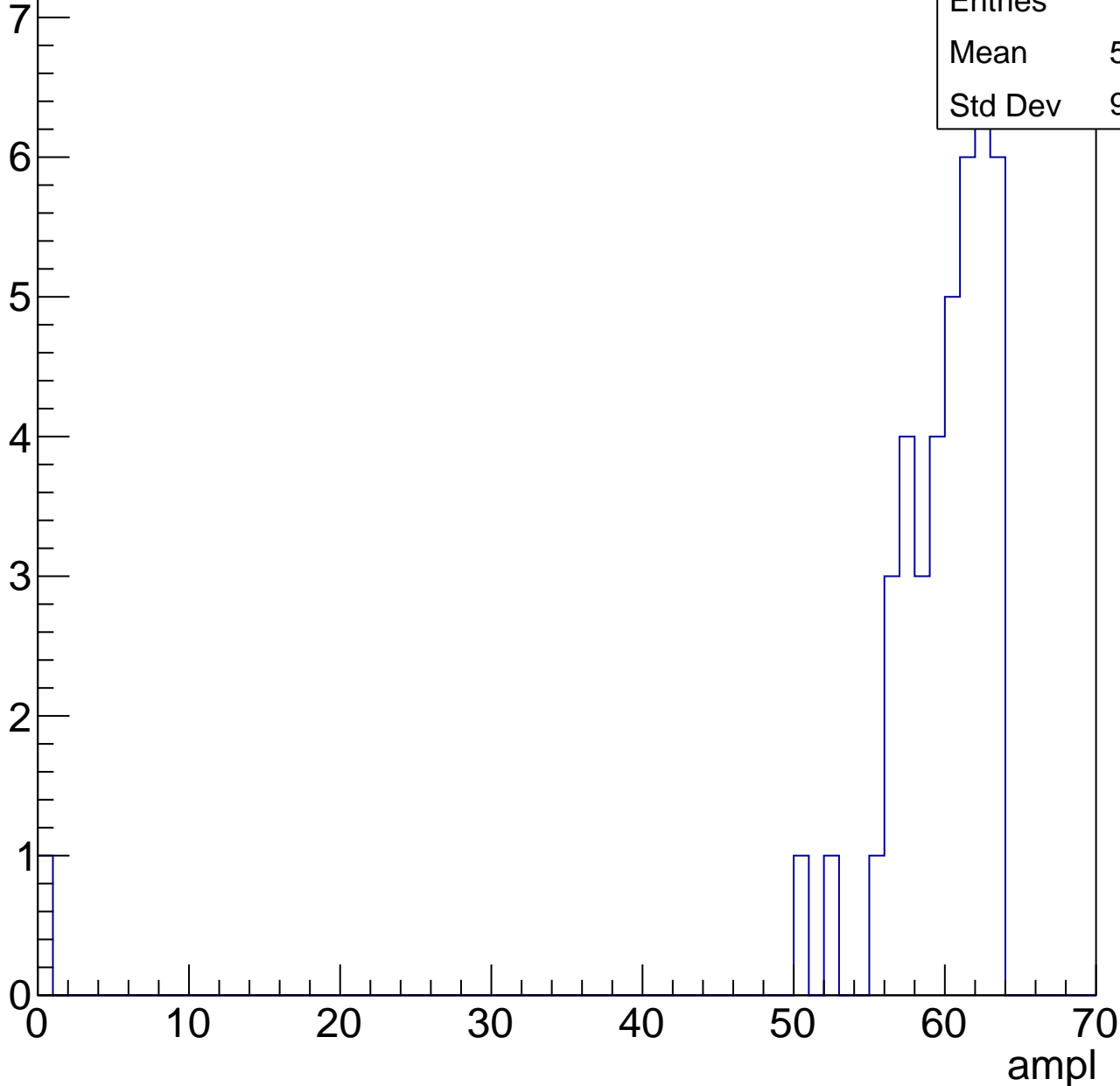


# B1L102S, U5-ch47, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	42
Mean	58.12
Std Dev	9.547



# B1L102S, U5-ch47, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries	13
Mean	60.92
Std Dev	1.817



# B1L102S, U5-ch47, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	11
Std Dev	11

# B1L102S, U5-ch48, adc0

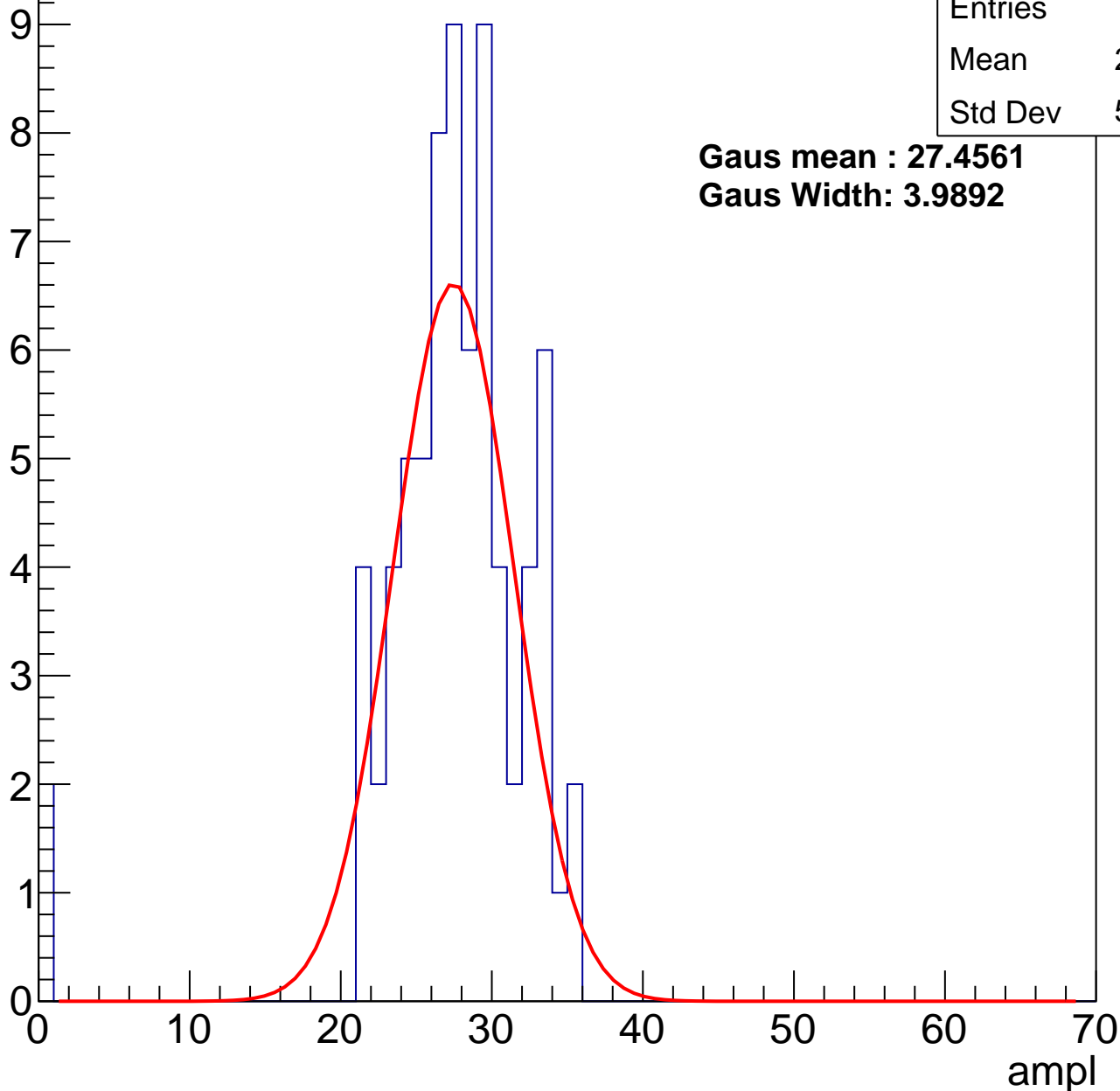
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	26.81
Std Dev	5.721

**Gaus mean : 27.4561**

**Gaus Width: 3.9892**



# B1L102S, U5-ch48, adc1

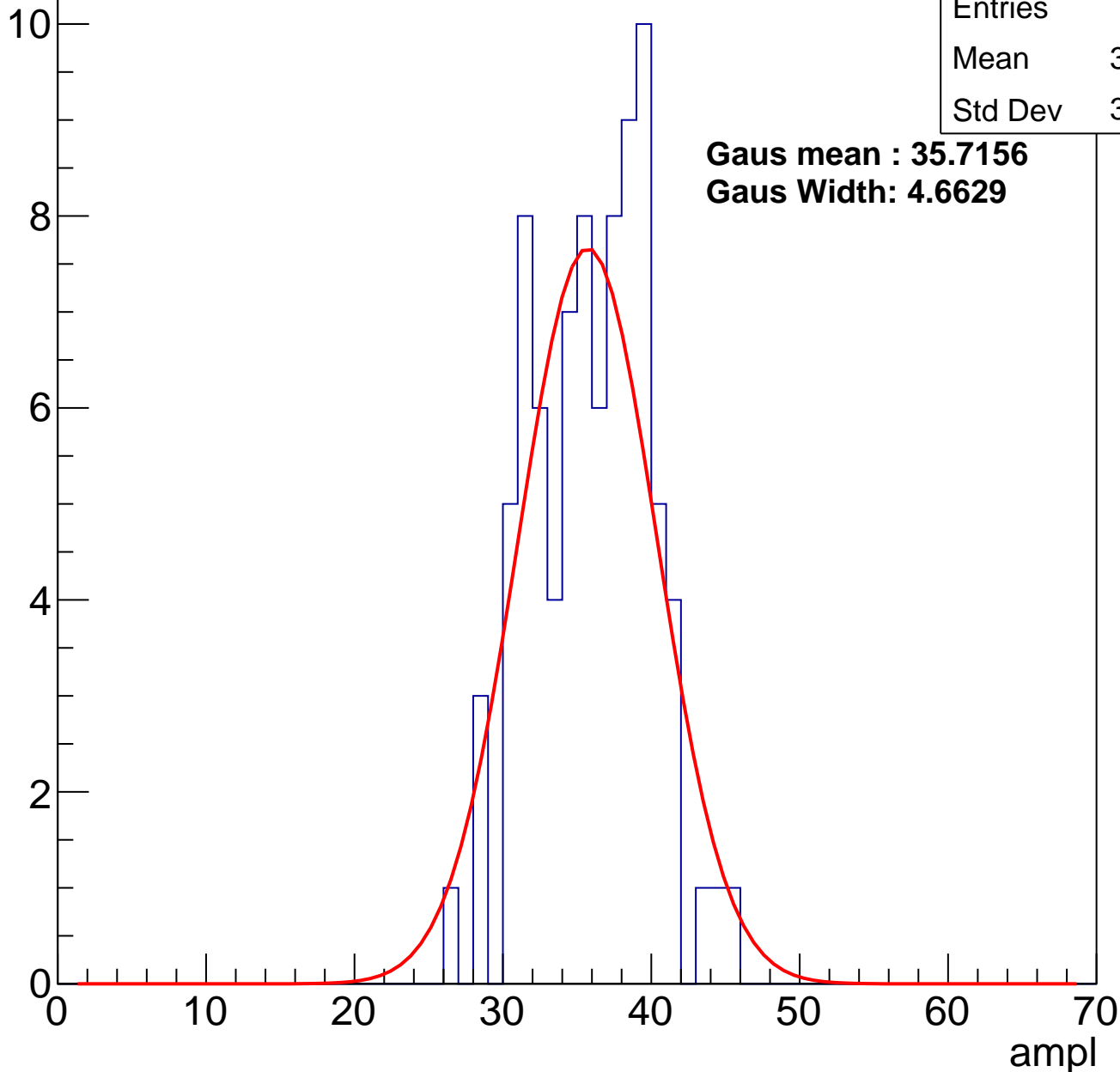
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	87
Mean	35.52
Std Dev	3.907

**Gaus mean : 35.7156**

**Gaus Width: 4.6629**

Entry



# B1L102S, U5-ch48, adc2

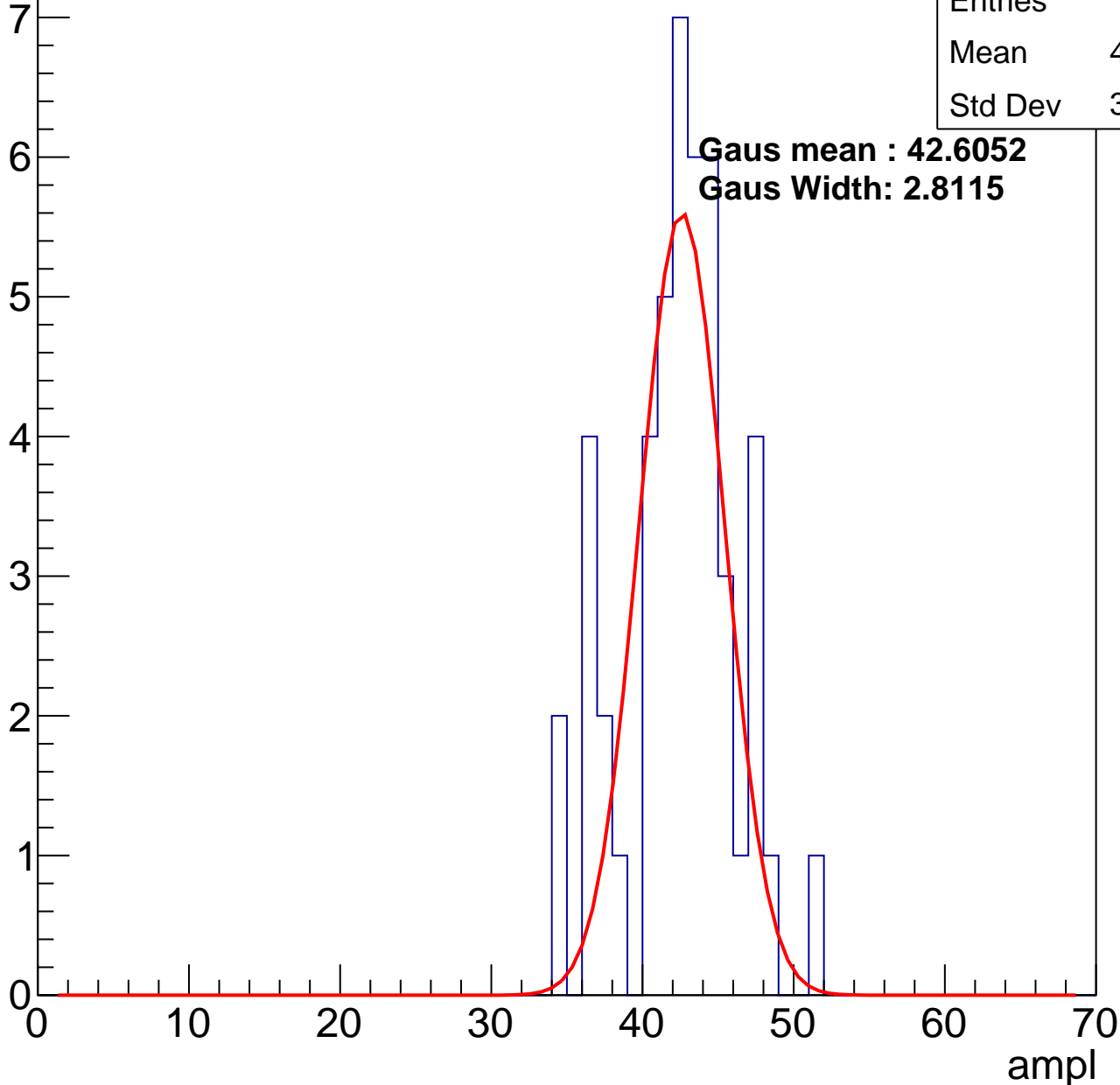
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	47
Mean	41.98
Std Dev	3.716

**Gaus mean : 42.6052**

**Gaus Width: 2.8115**

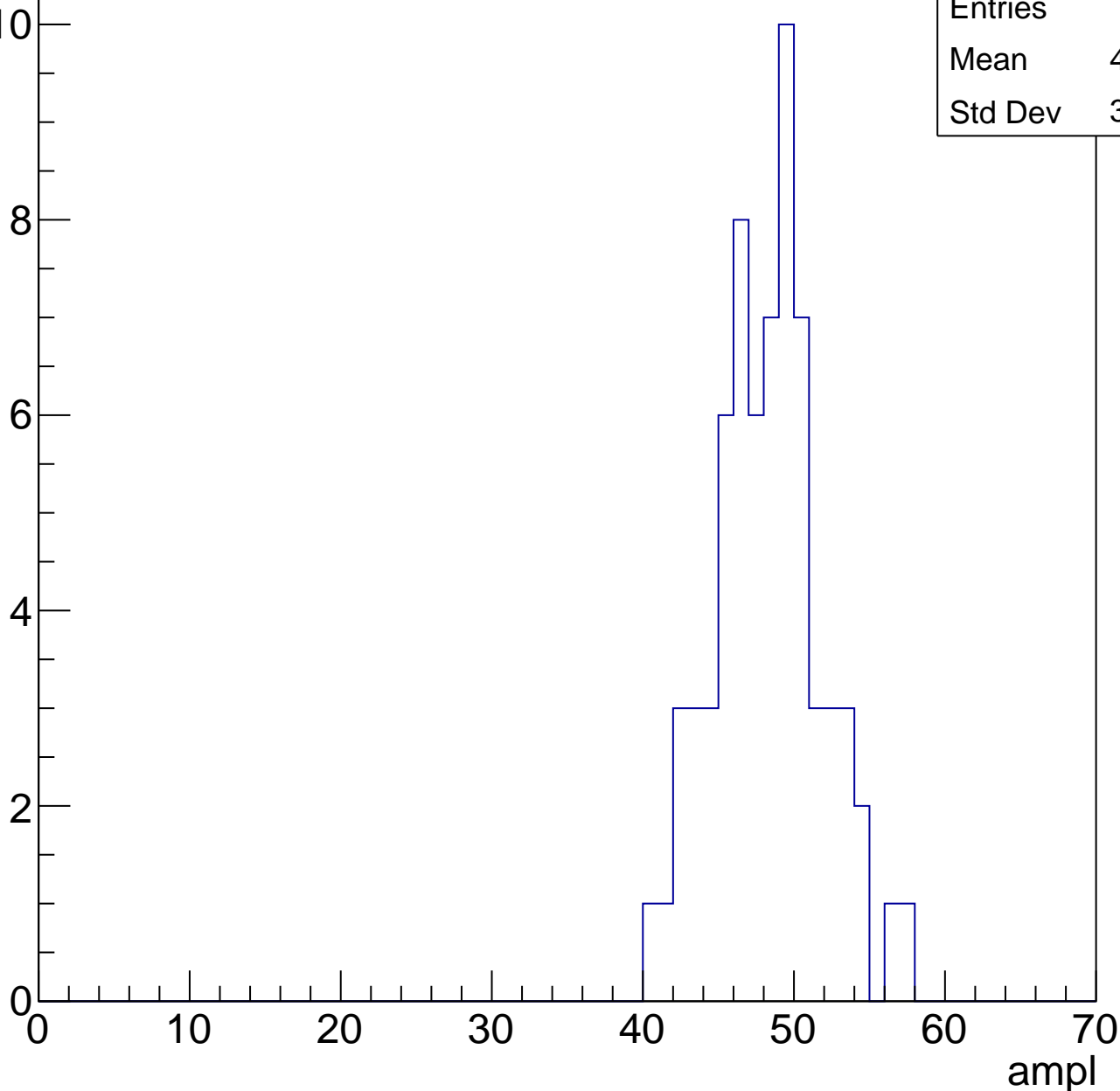


# B1L102S, U5-ch48, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	47.84
Std Dev	3.513

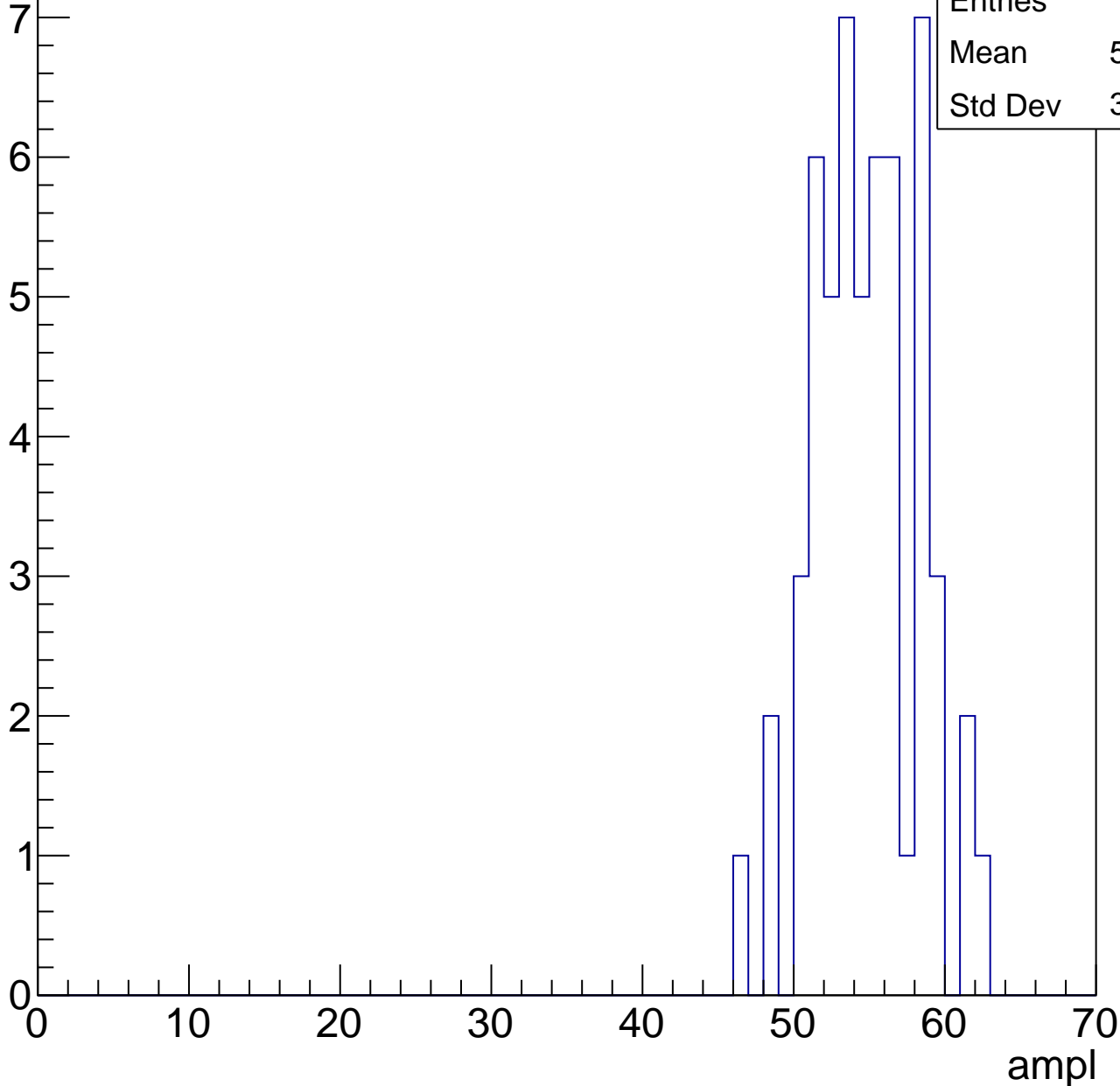


# B1L102S, U5-ch48, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

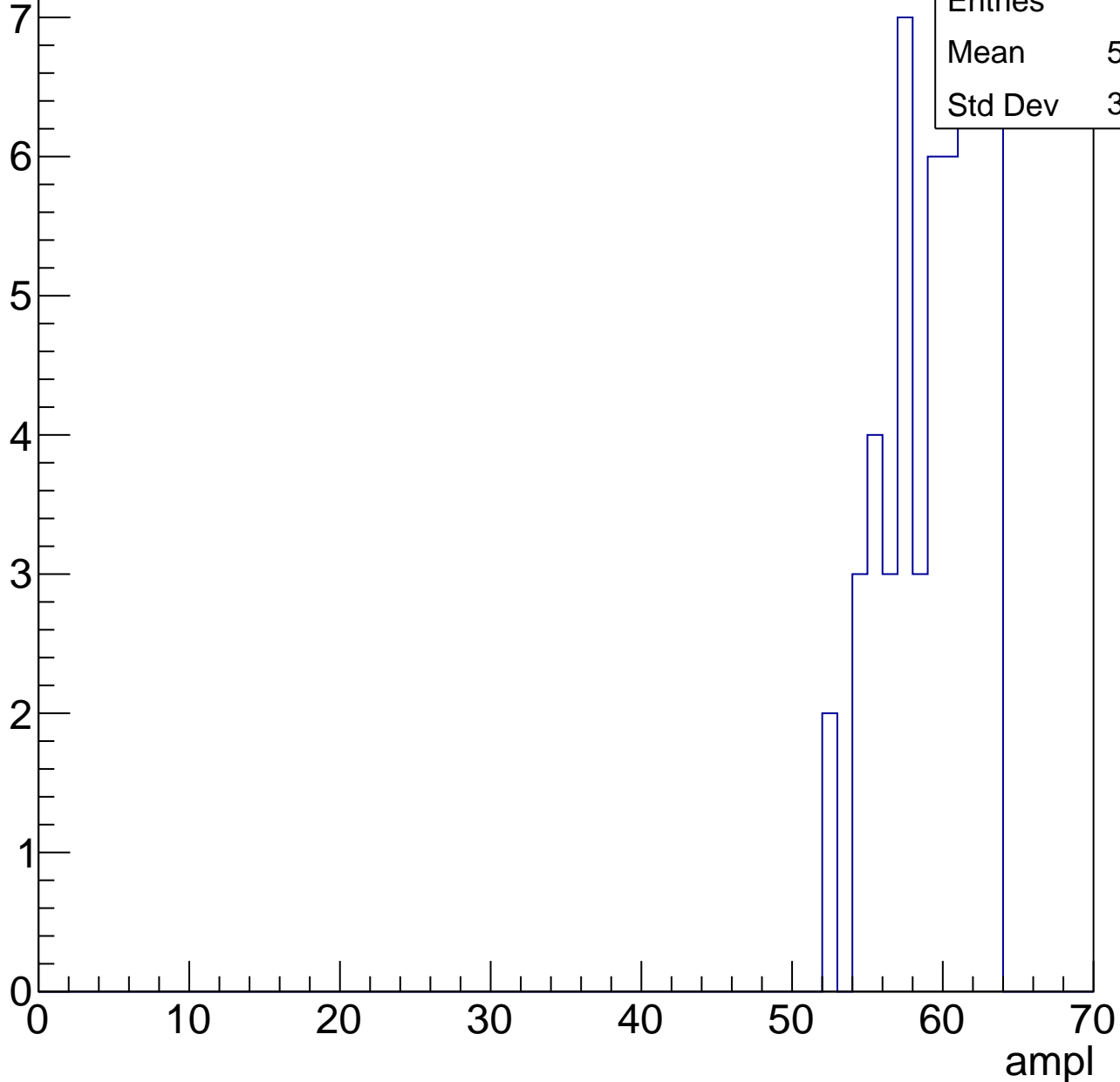
Entries	55
Mean	54.35
Std Dev	3.428



# B1L102S, U5-ch48, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

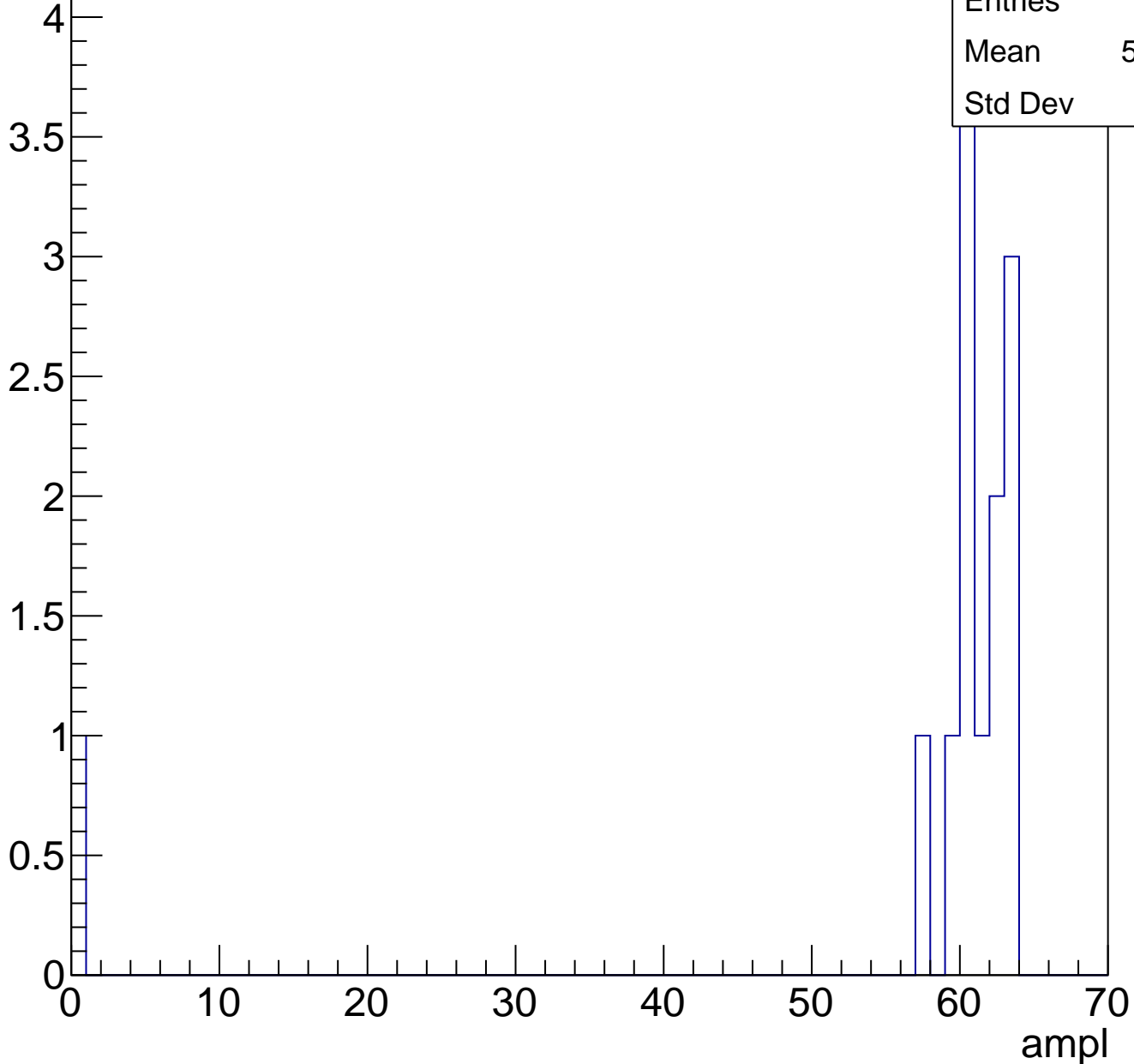
Entry



# B1L102S, U5-ch48, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U5-ch48, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U5-ch49, adc0

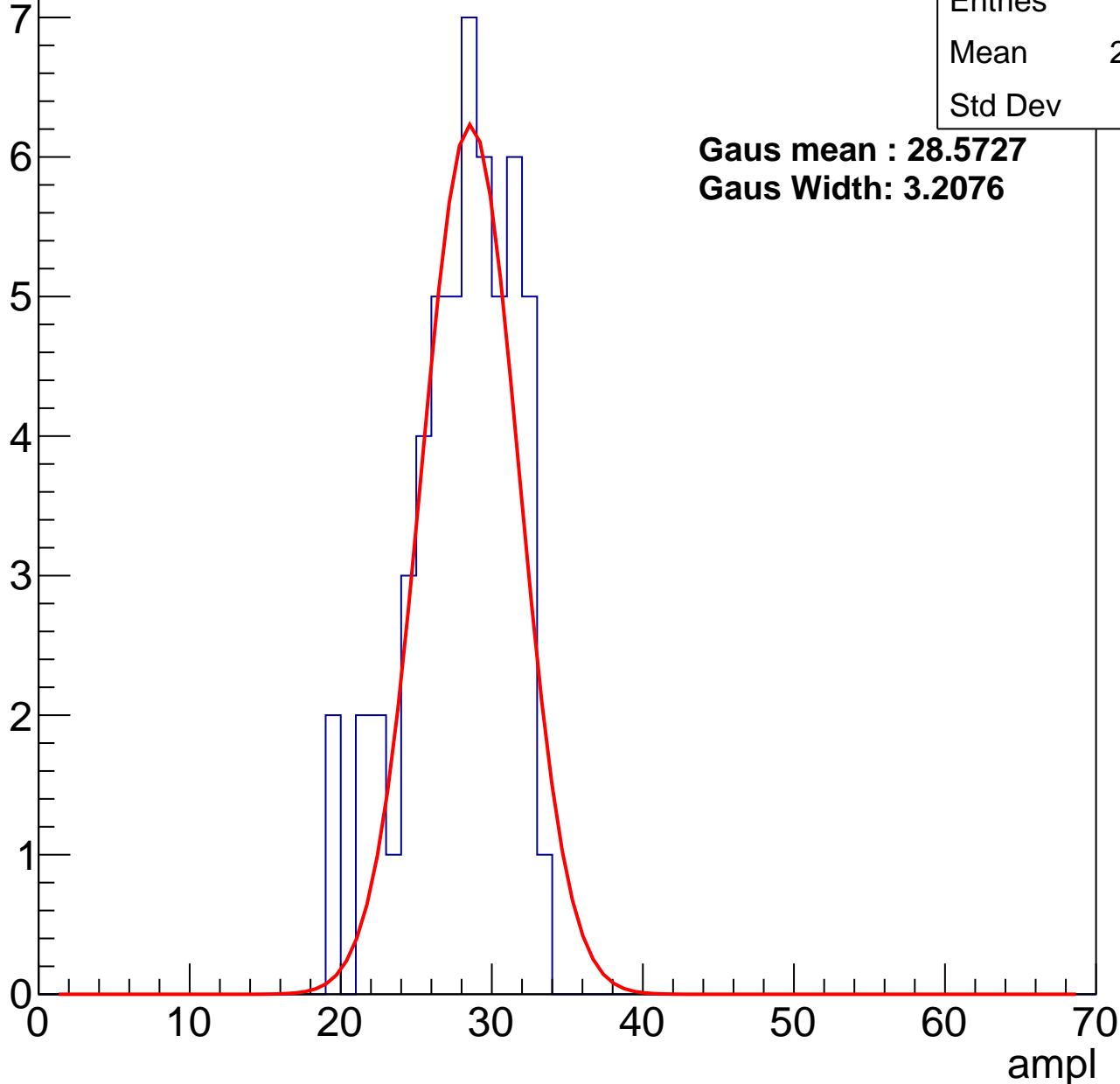
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	27.46
Std Dev	3.43

**Gaus mean : 28.5727**

**Gaus Width: 3.2076**



# B1L102S, U5-ch49, adc1

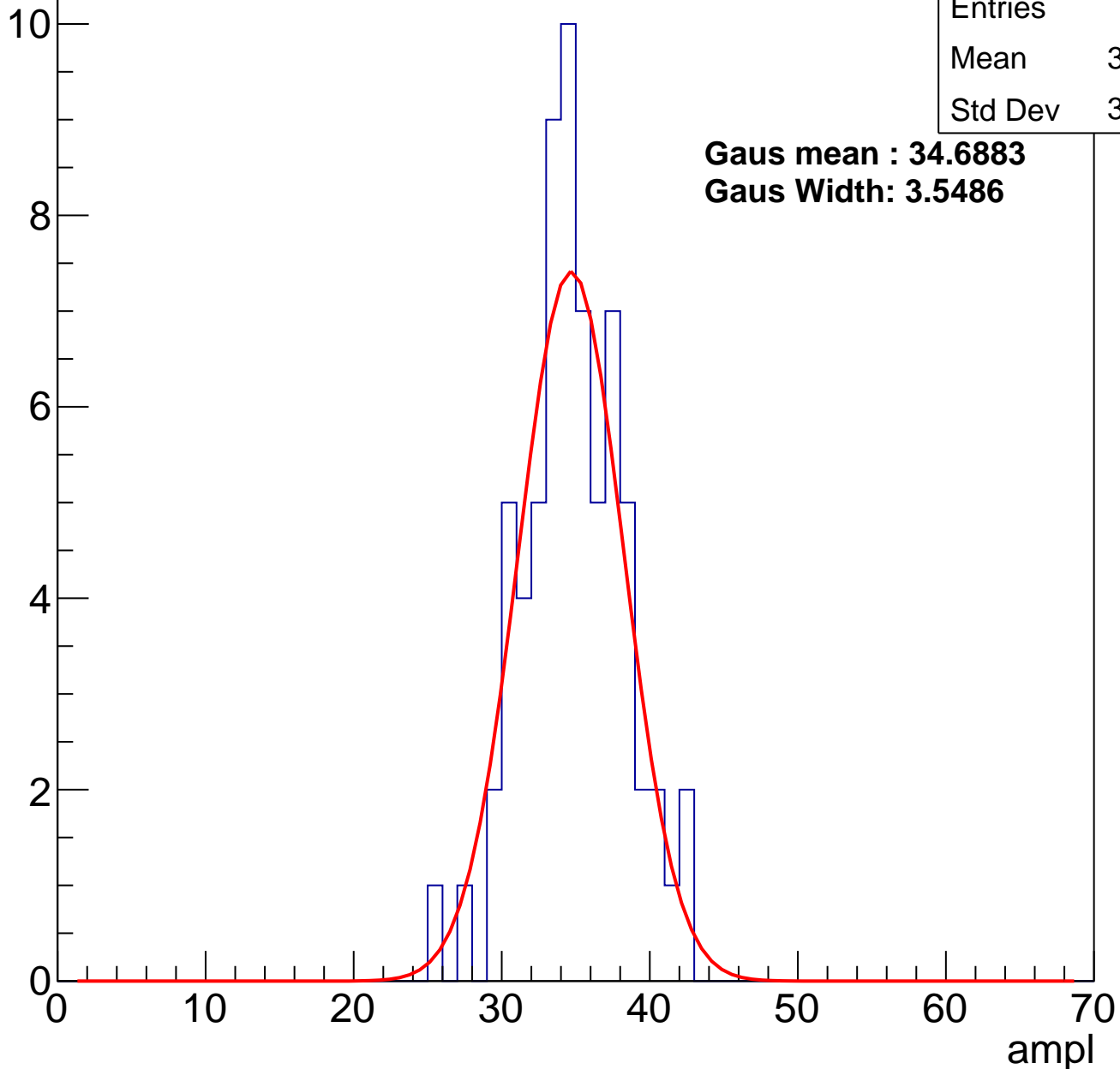
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	68
Mean	34.38
Std Dev	3.396

**Gaus mean : 34.6883**

**Gaus Width: 3.5486**

Entry



# B1L102S, U5-ch49, adc2

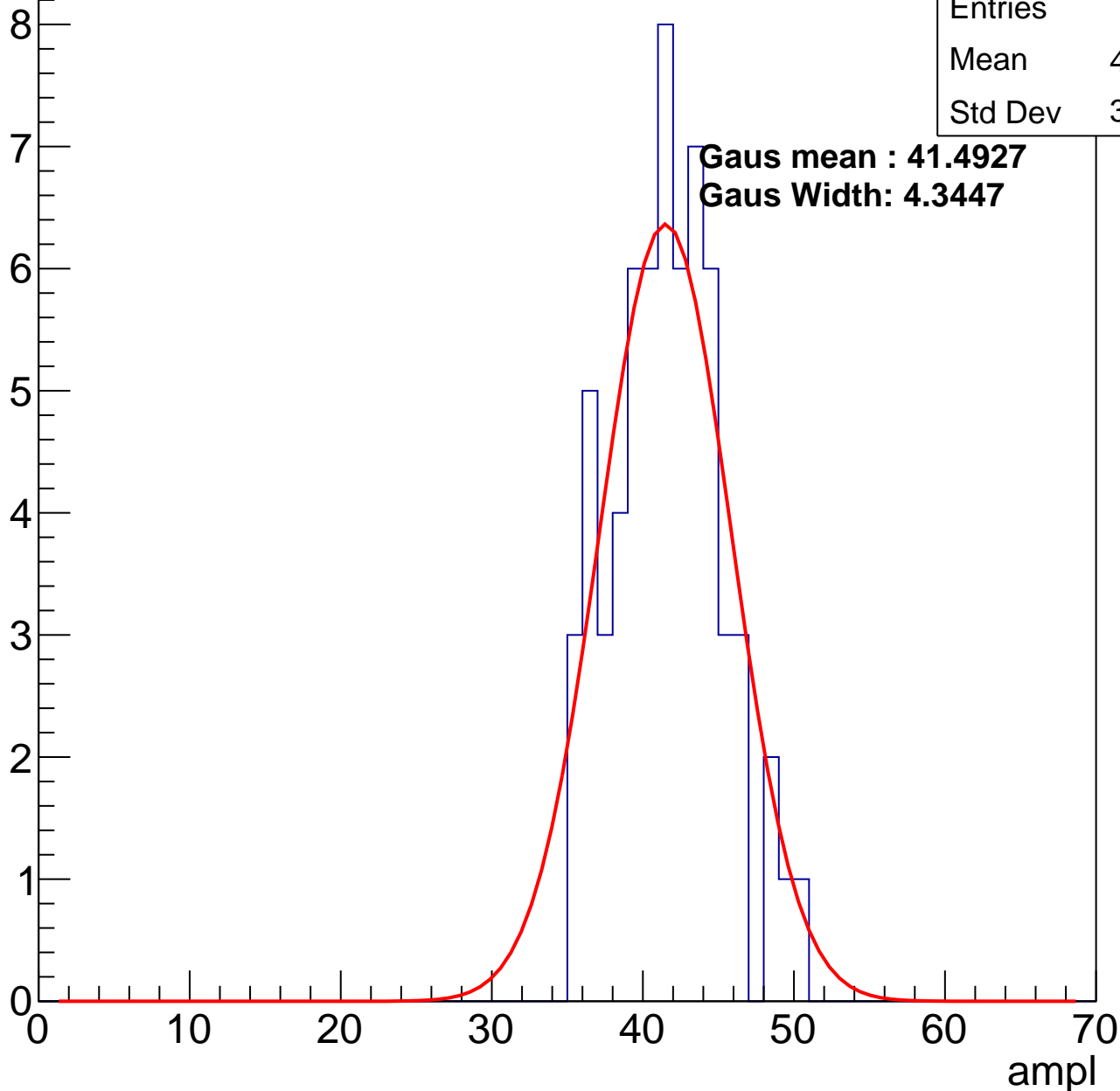
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	41.17
Std Dev	3.534

**Gaus mean : 41.4927**

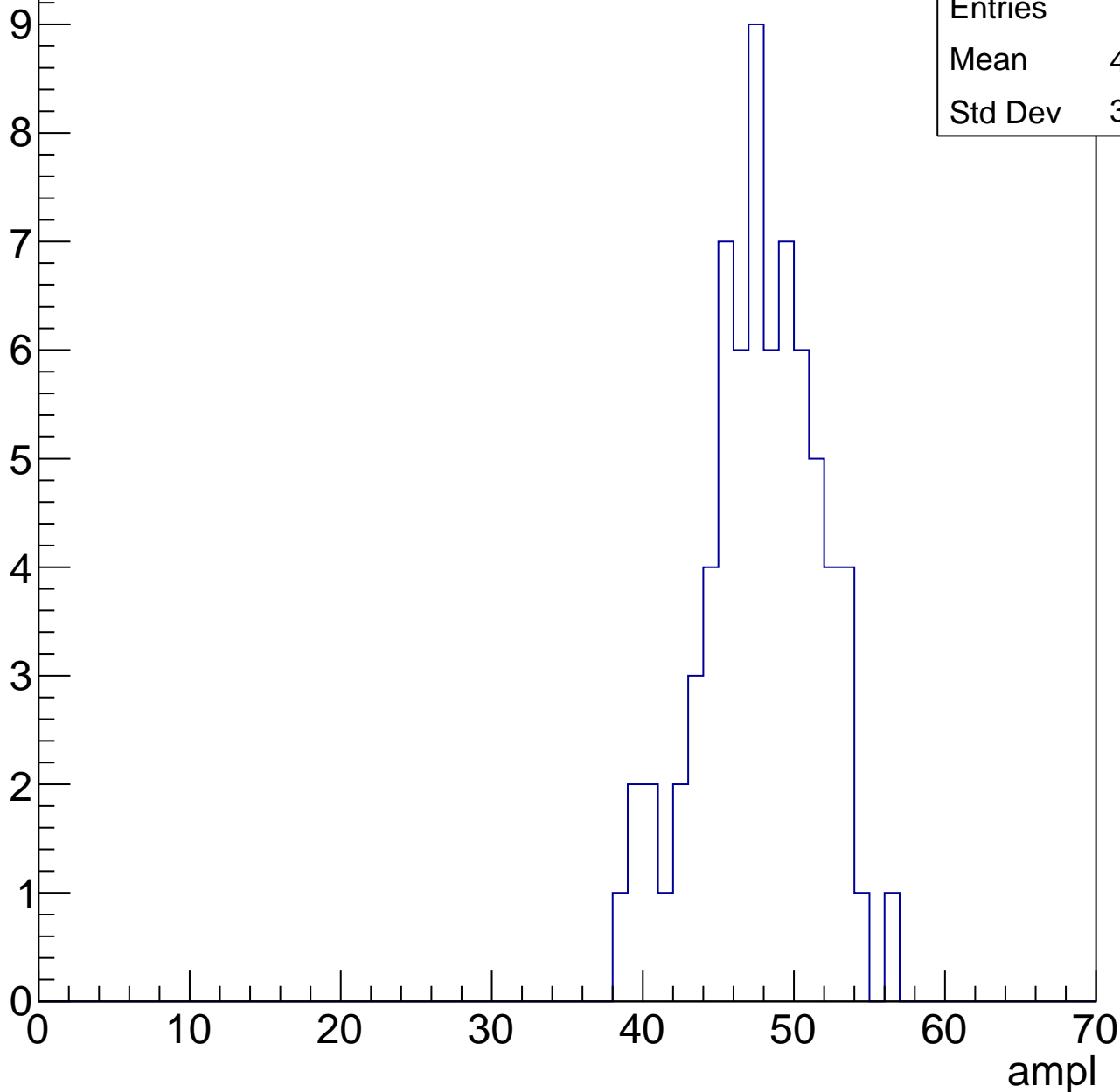
**Gaus Width: 4.3447**



# B1L102S, U5-ch49, adc3

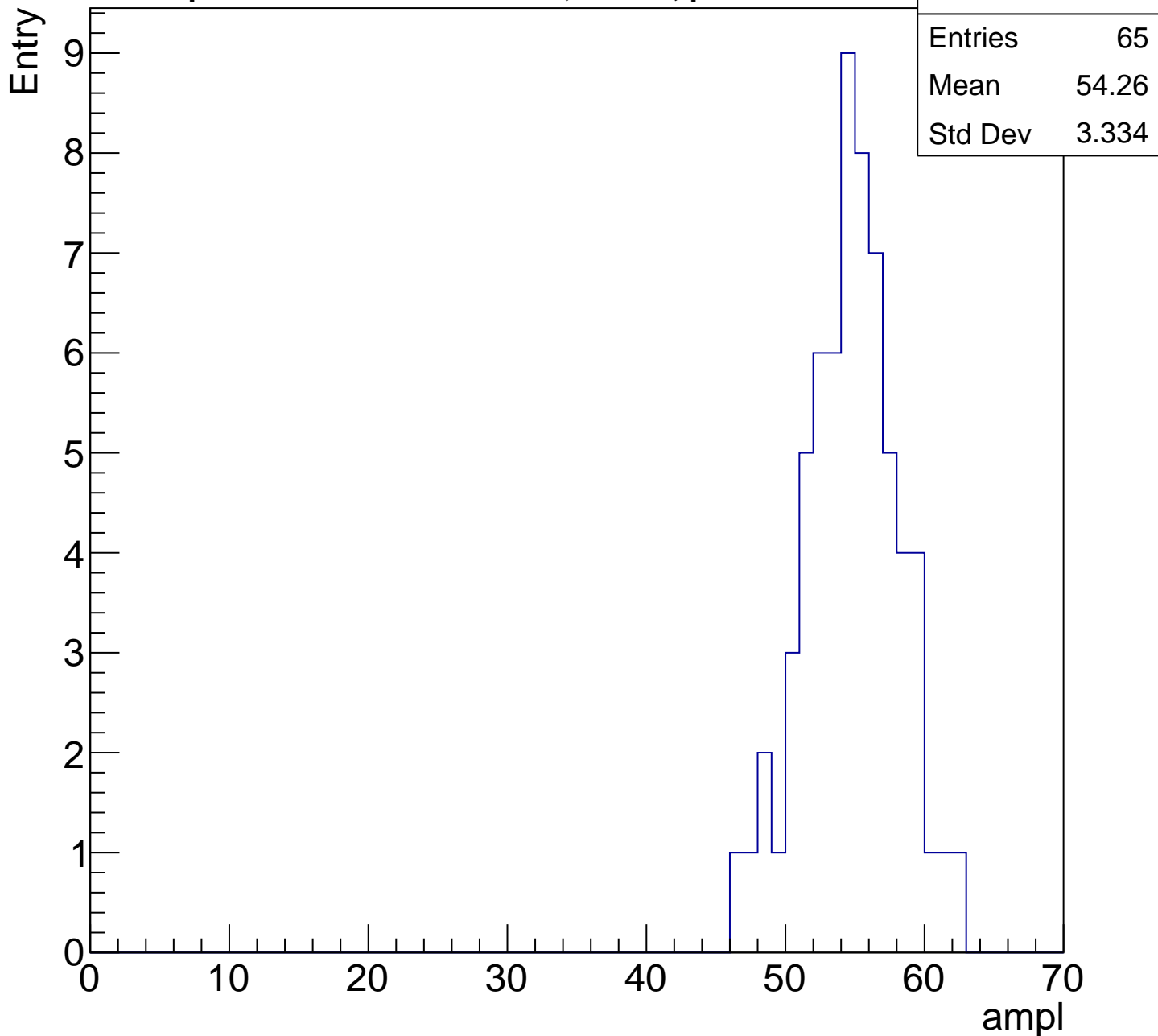
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U5-ch49, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2



# B1L102S, U5-ch49, adc5

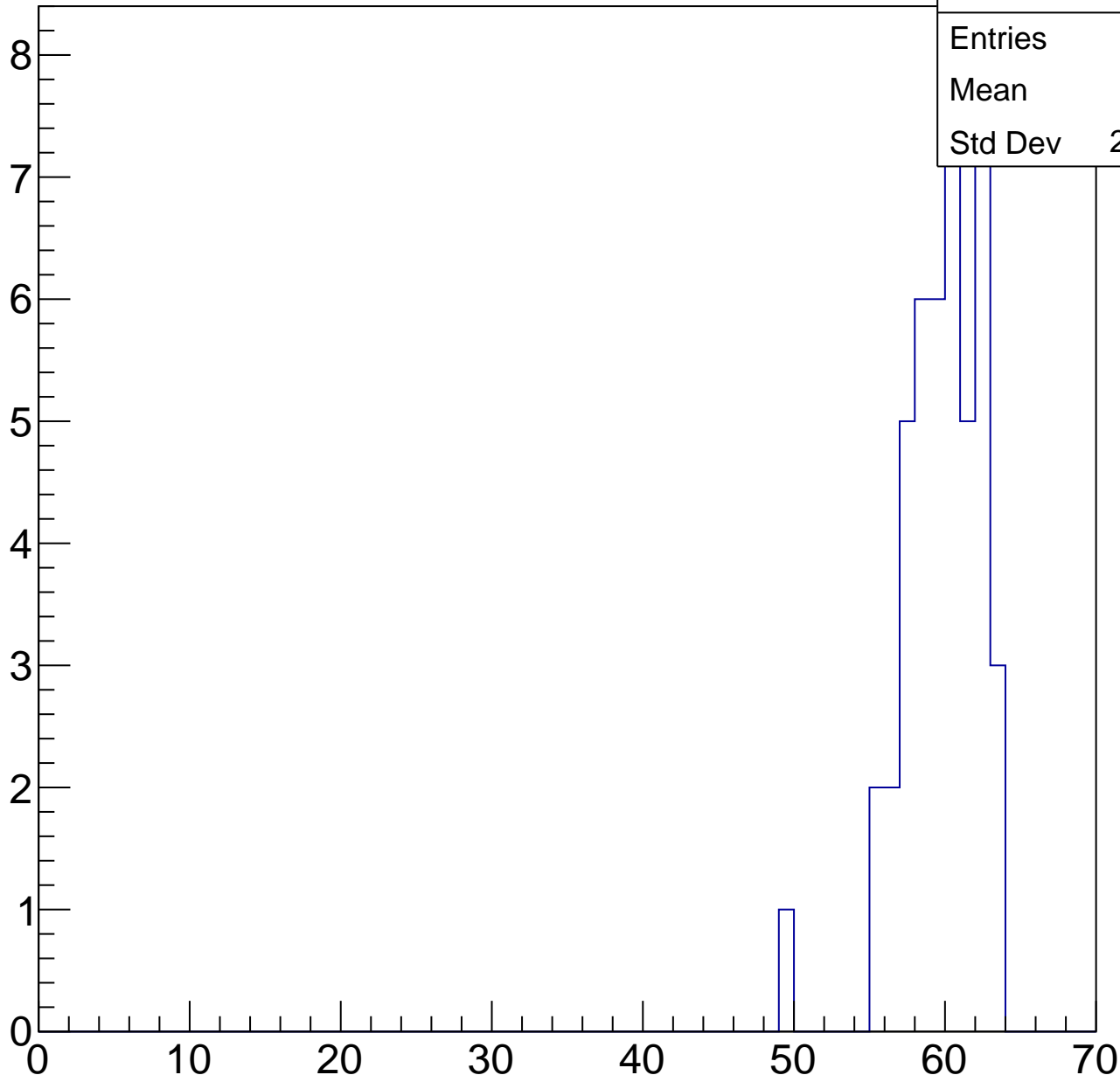
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	46
Mean	59.3
Std Dev	2.636

ampl

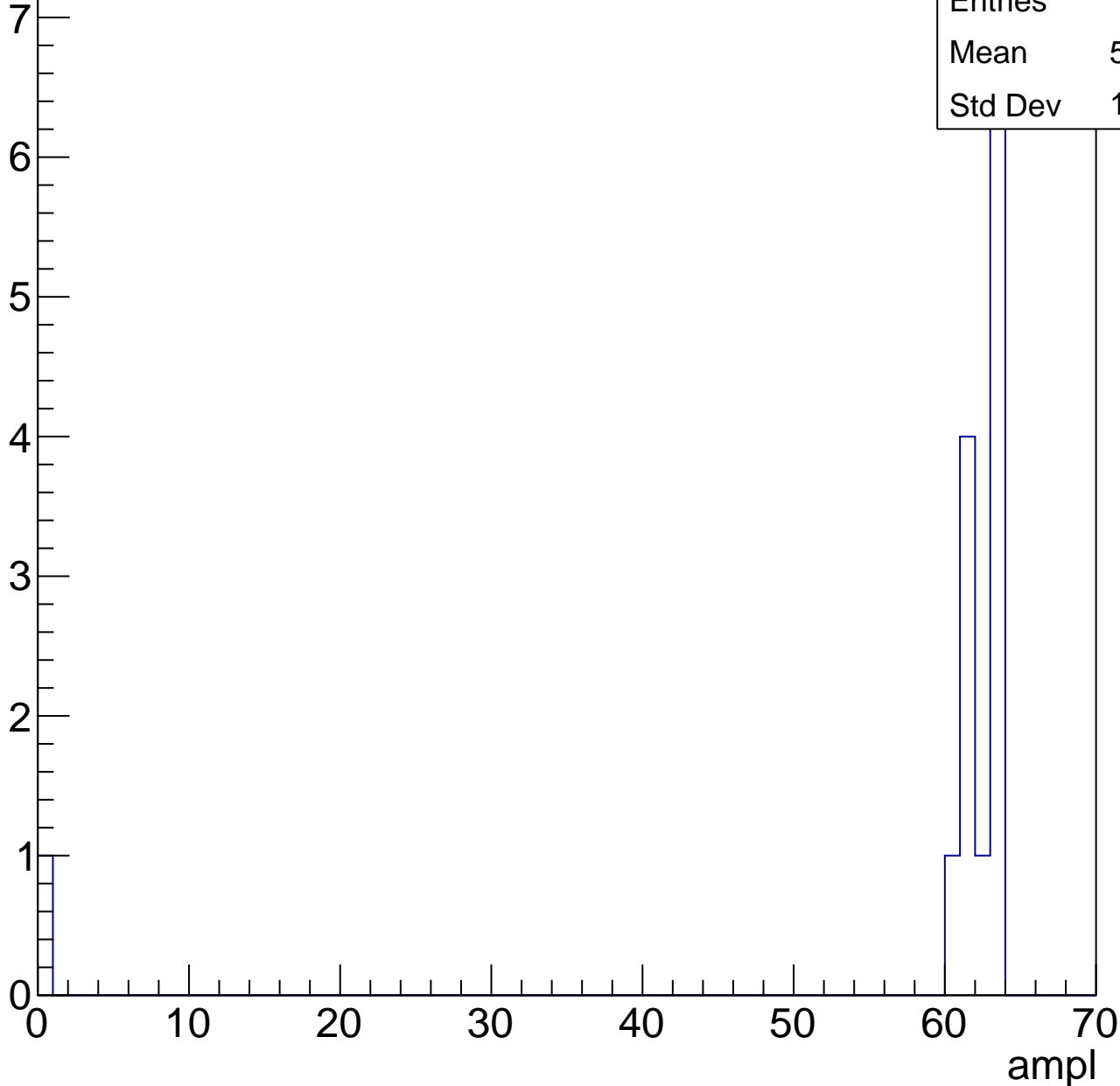


# B1L102S, U5-ch49, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	14
Mean	57.64
Std Dev	16.02





# B1L102S, U5-ch49, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U5-ch50, adc0

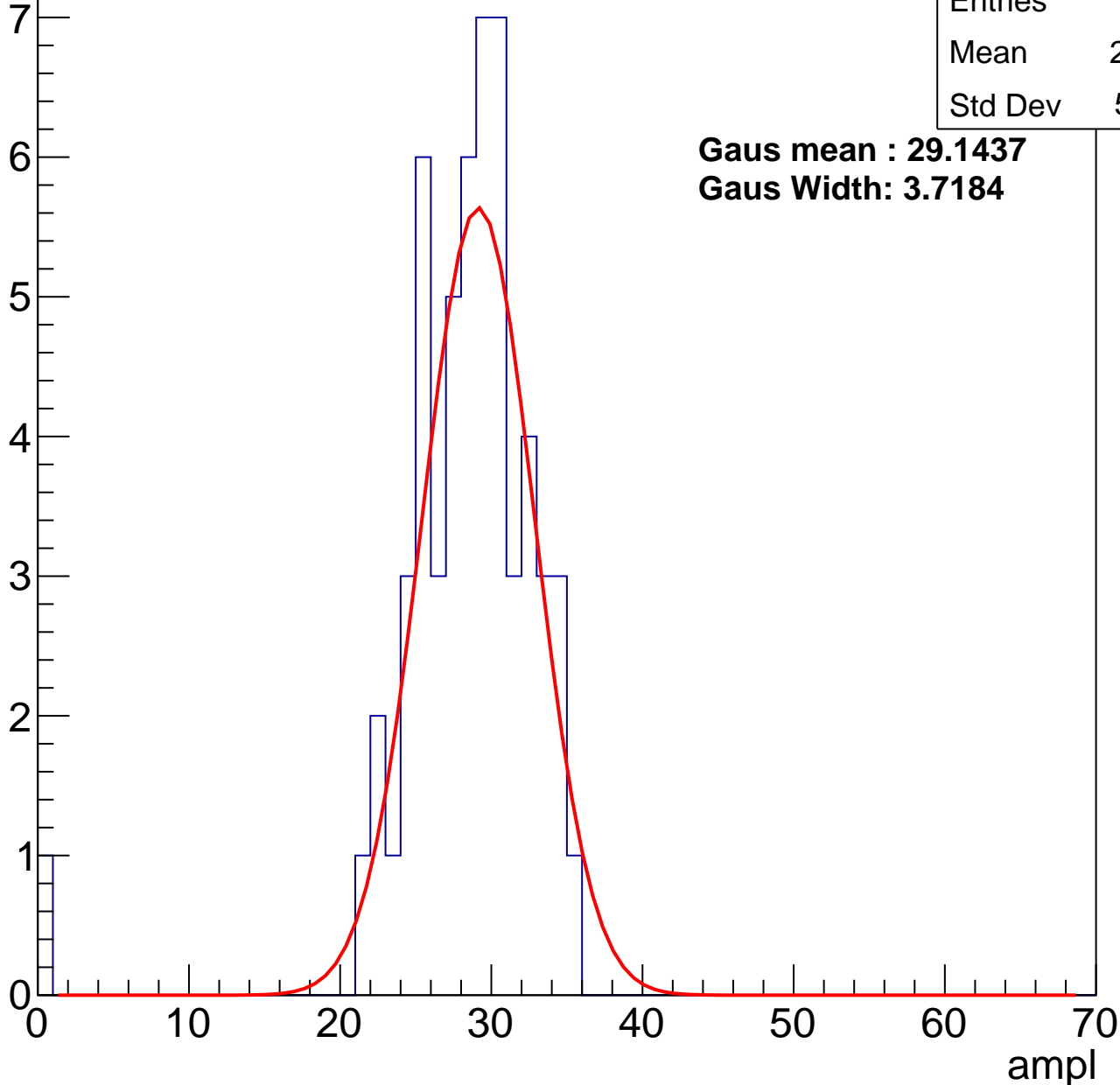
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	27.88
Std Dev	5.011

**Gaus mean : 29.1437**

**Gaus Width: 3.7184**



# B1L102S, U5-ch50, adc1

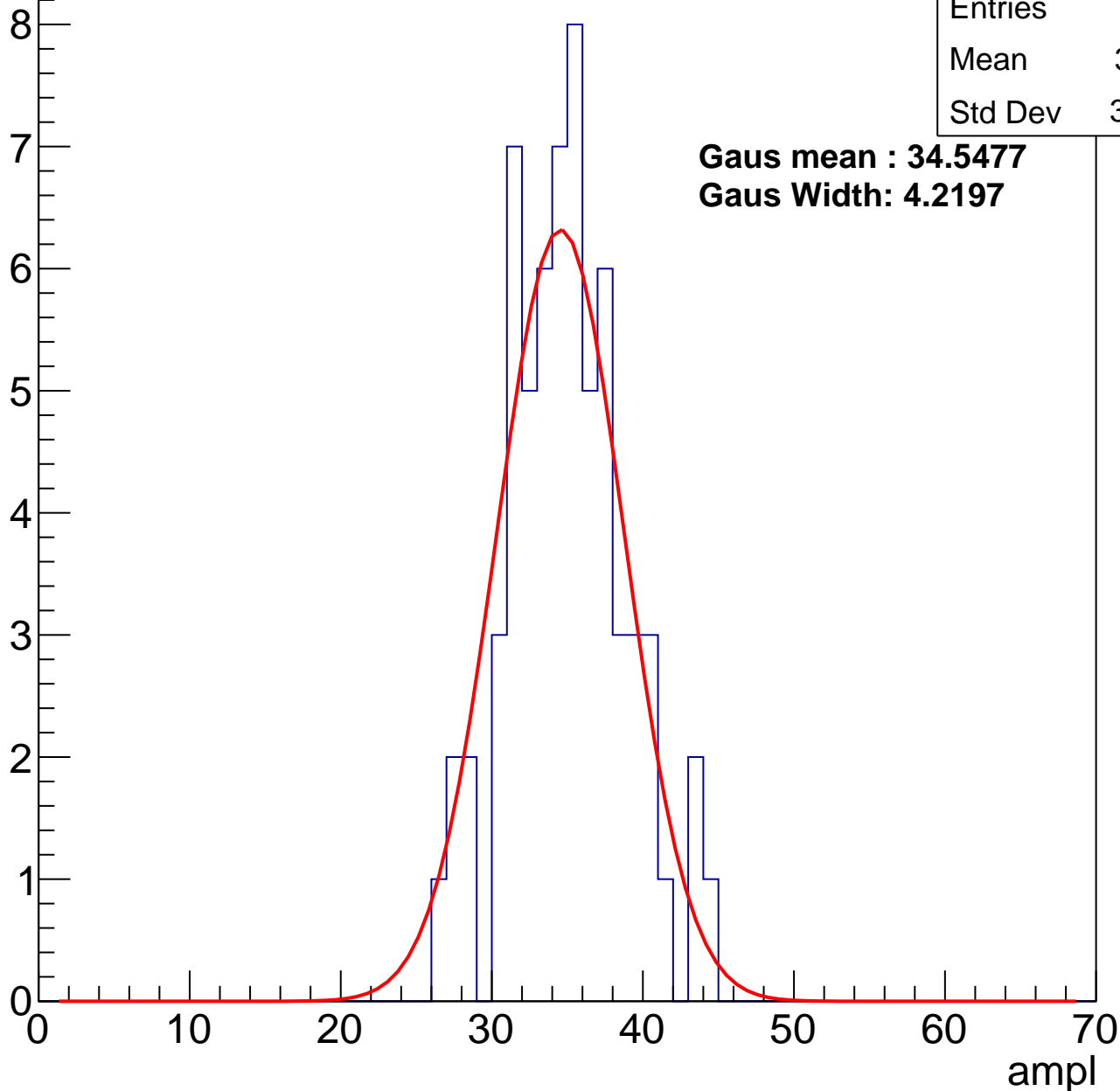
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	34.51
Std Dev	3.879

**Gaus mean : 34.5477**

**Gaus Width: 4.2197**



# B1L102S, U5-ch50, adc2

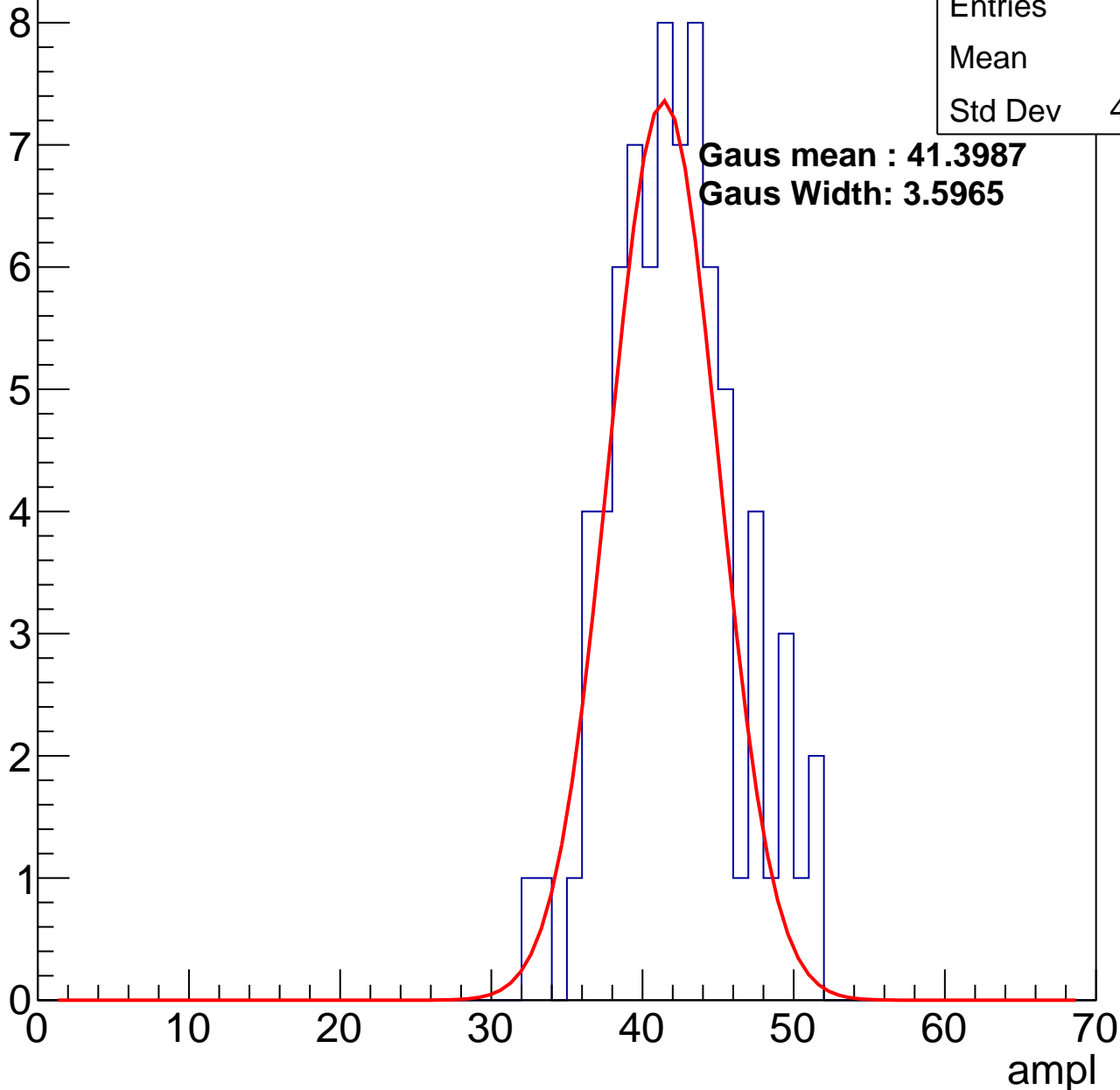
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	41.7
Std Dev	4.072

**Gaus mean : 41.3987**

**Gaus Width: 3.5965**

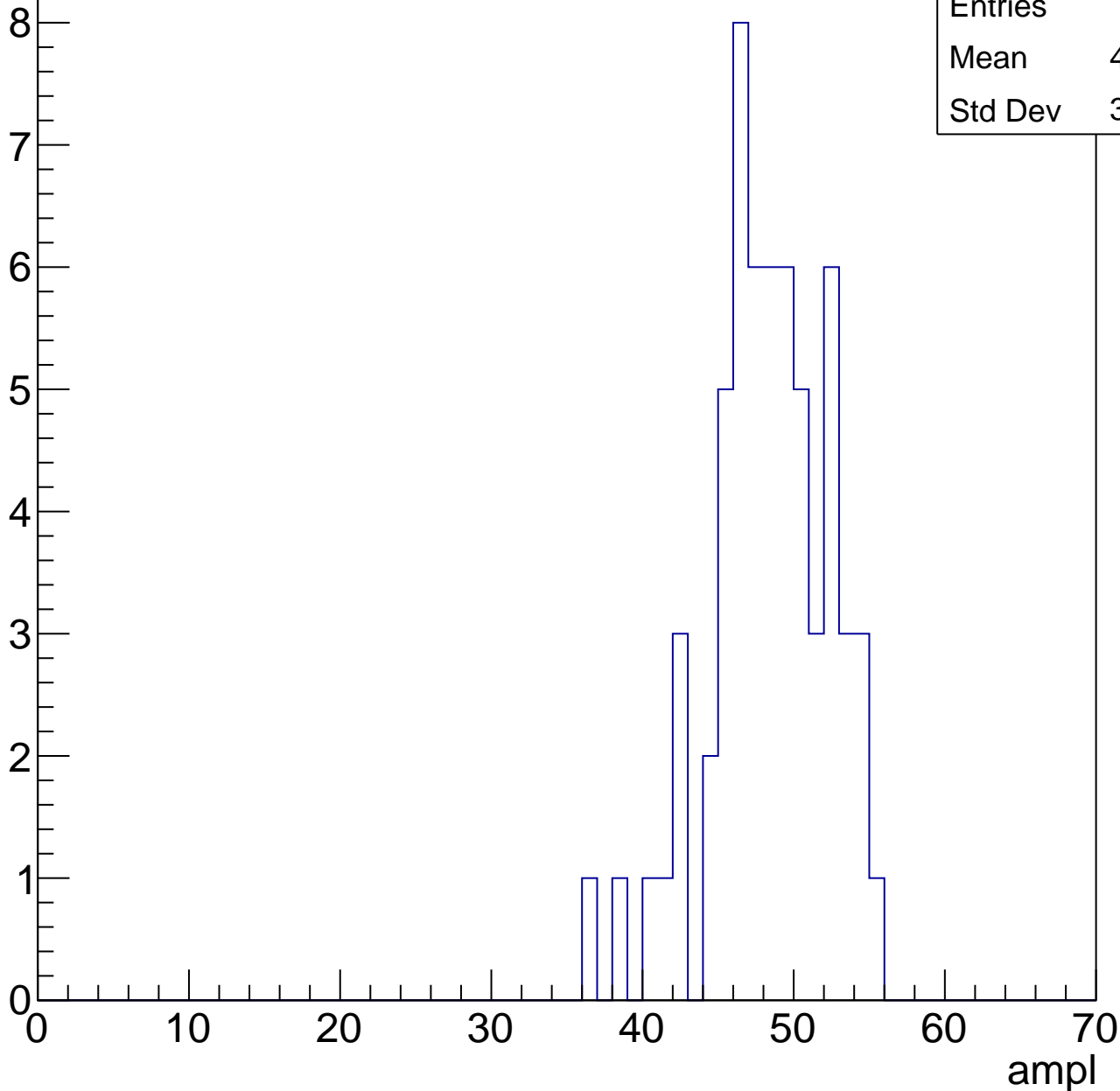


# B1L102S, U5-ch50, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

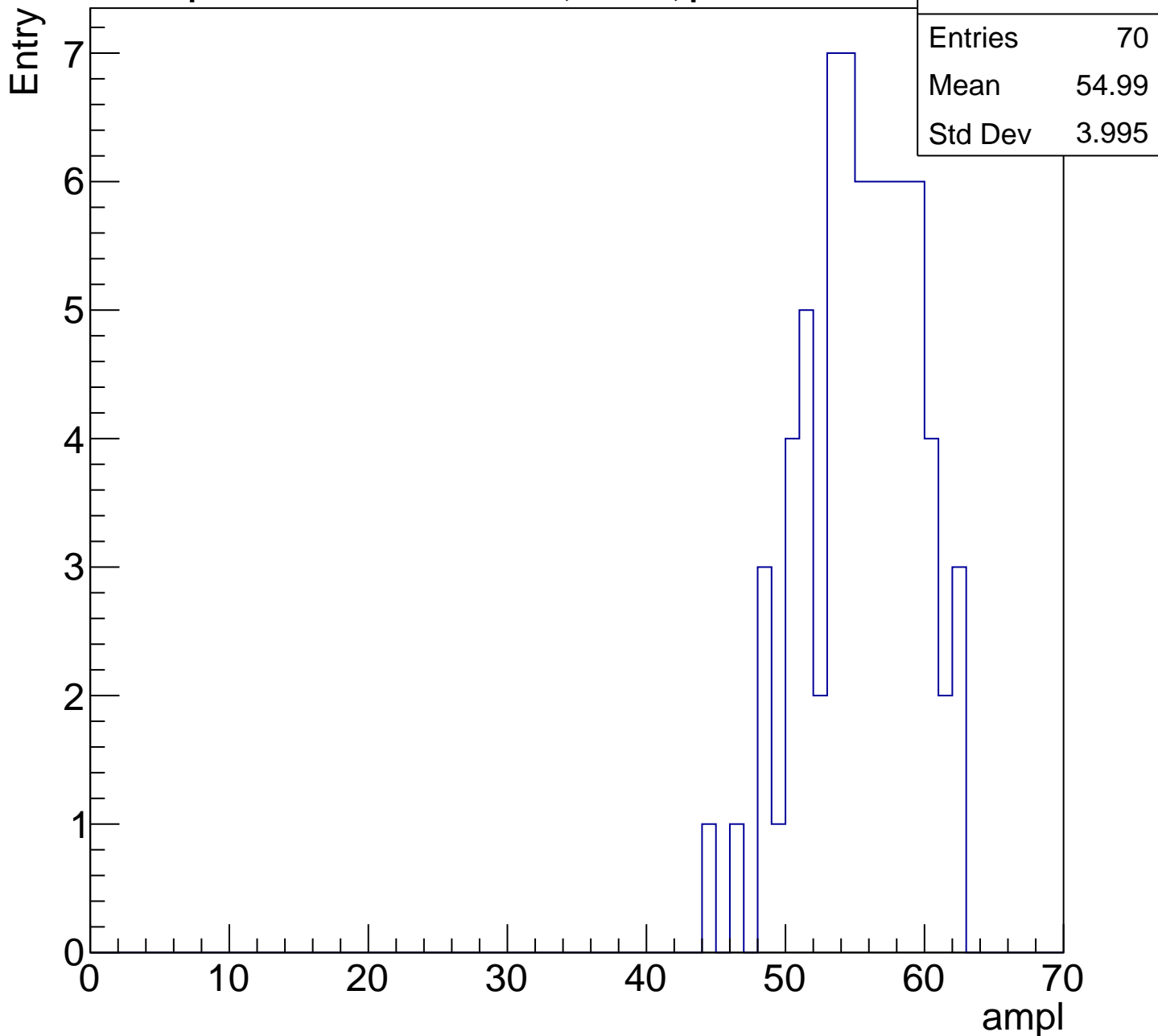
Entry

Entries	61
Mean	47.82
Std Dev	3.965



# B1L102S, U5-ch50, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

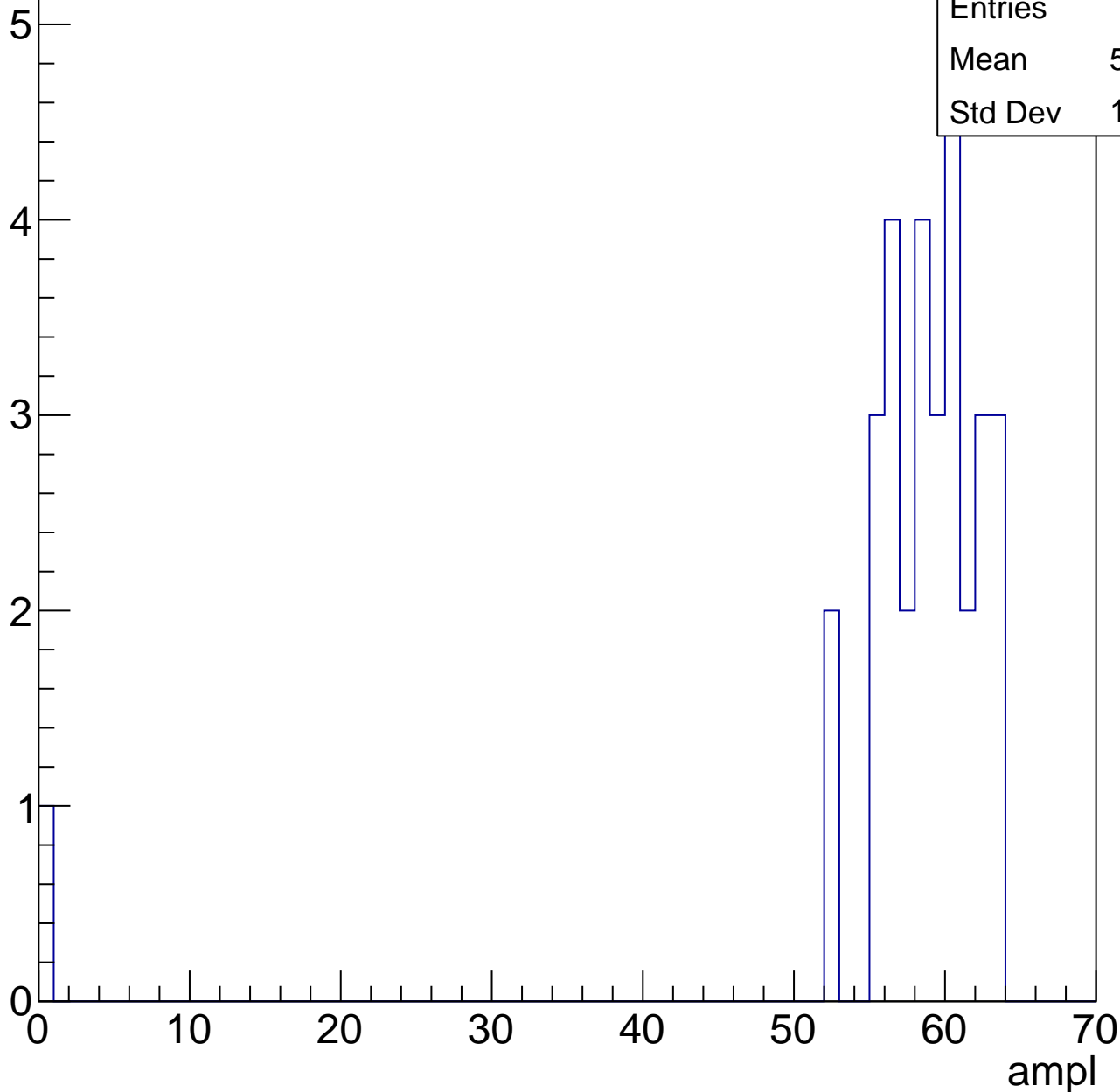


# B1L102S, U5-ch50, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	32
Mean	56.66
Std Dev	10.59

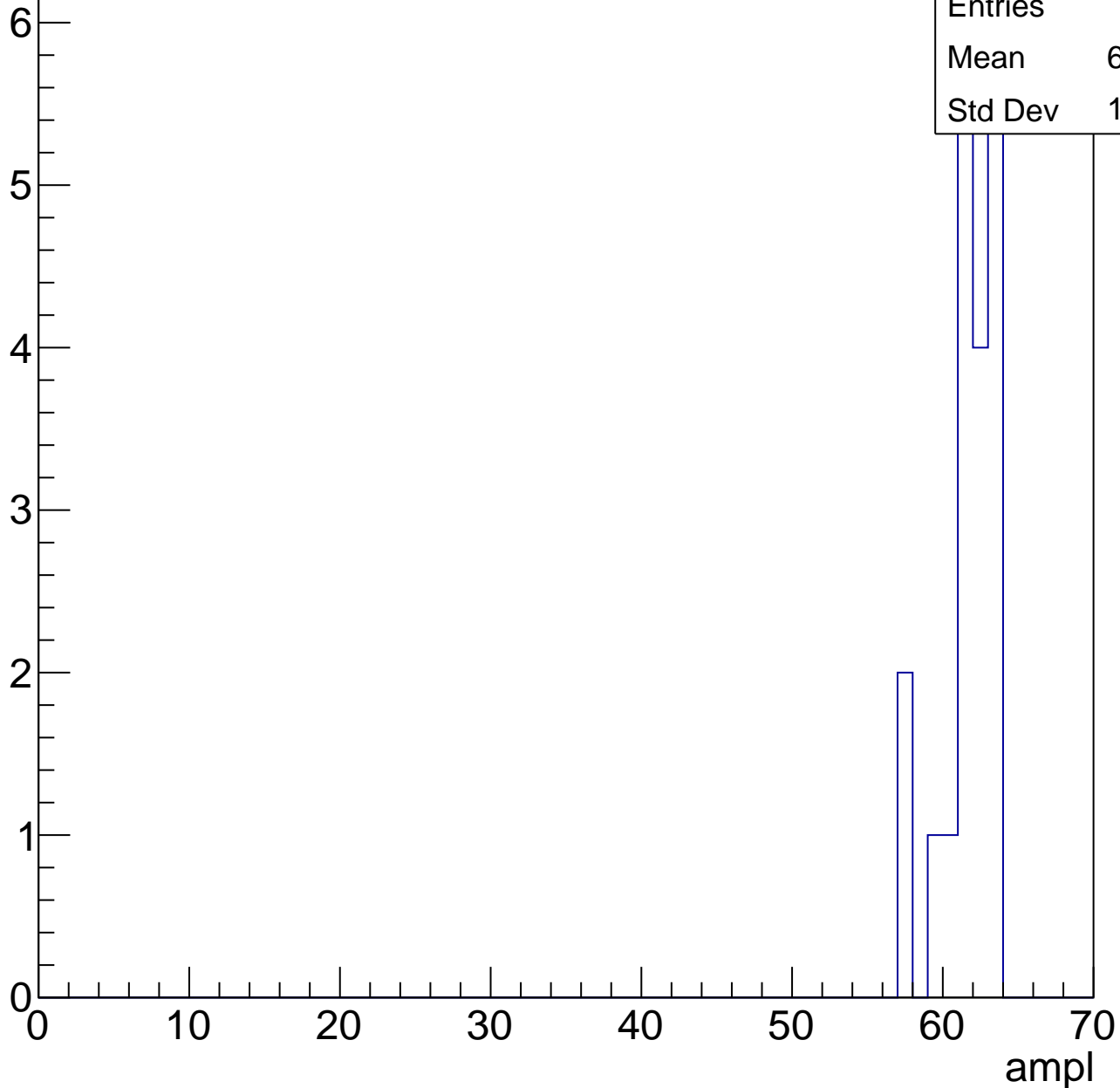


# B1L102S, U5-ch50, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	20
Mean	61.25
Std Dev	1.785





# B1L102S, U5-ch50, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U5-ch51, adc0

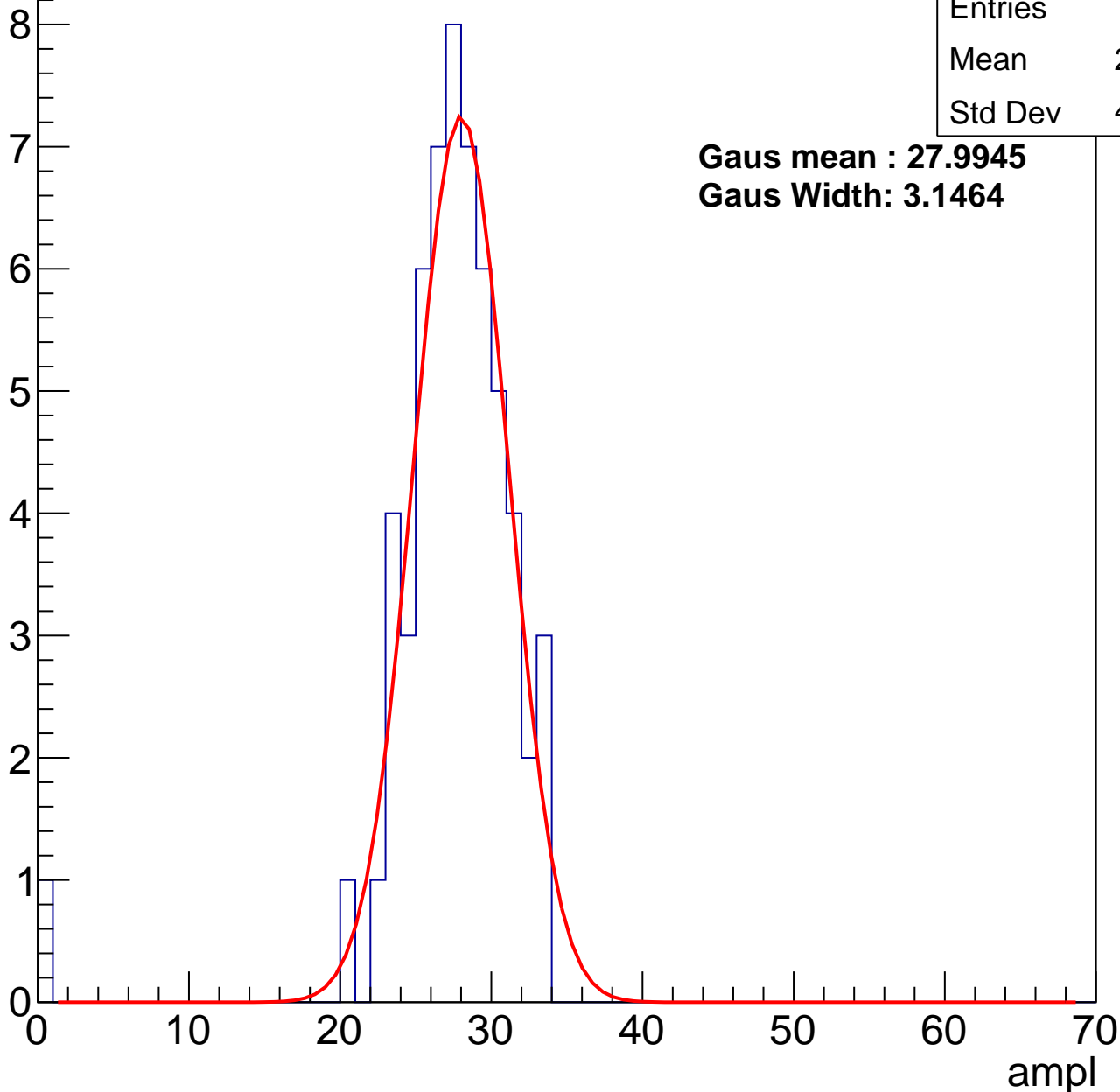
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	26.91
Std Dev	4.591

**Gaus mean : 27.9945**

**Gaus Width: 3.1464**



# B1L102S, U5-ch51, adc1

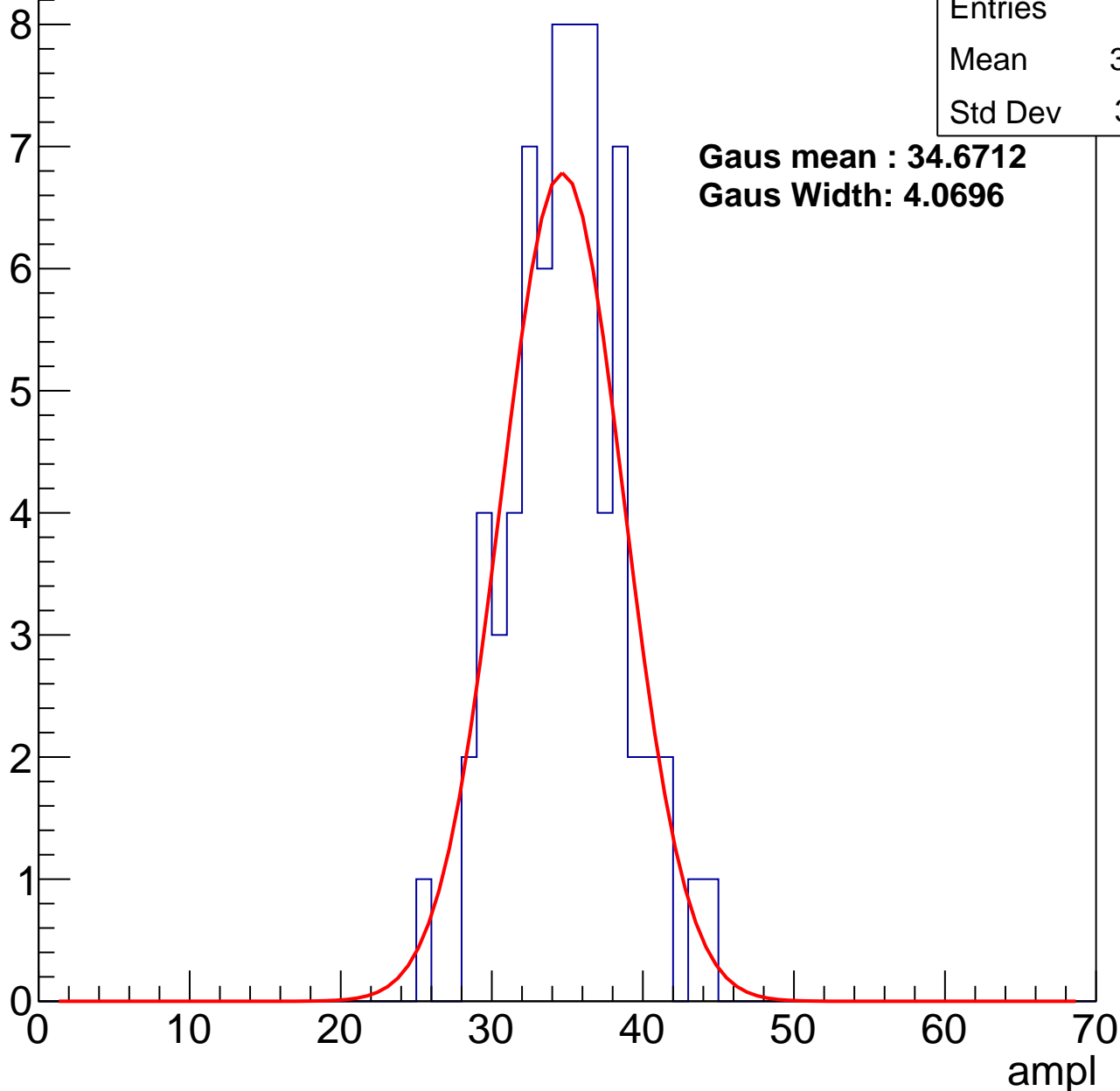
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	34.49
Std Dev	3.671

**Gaus mean : 34.6712**

**Gaus Width: 4.0696**



# B1L102S, U5-ch51, adc2

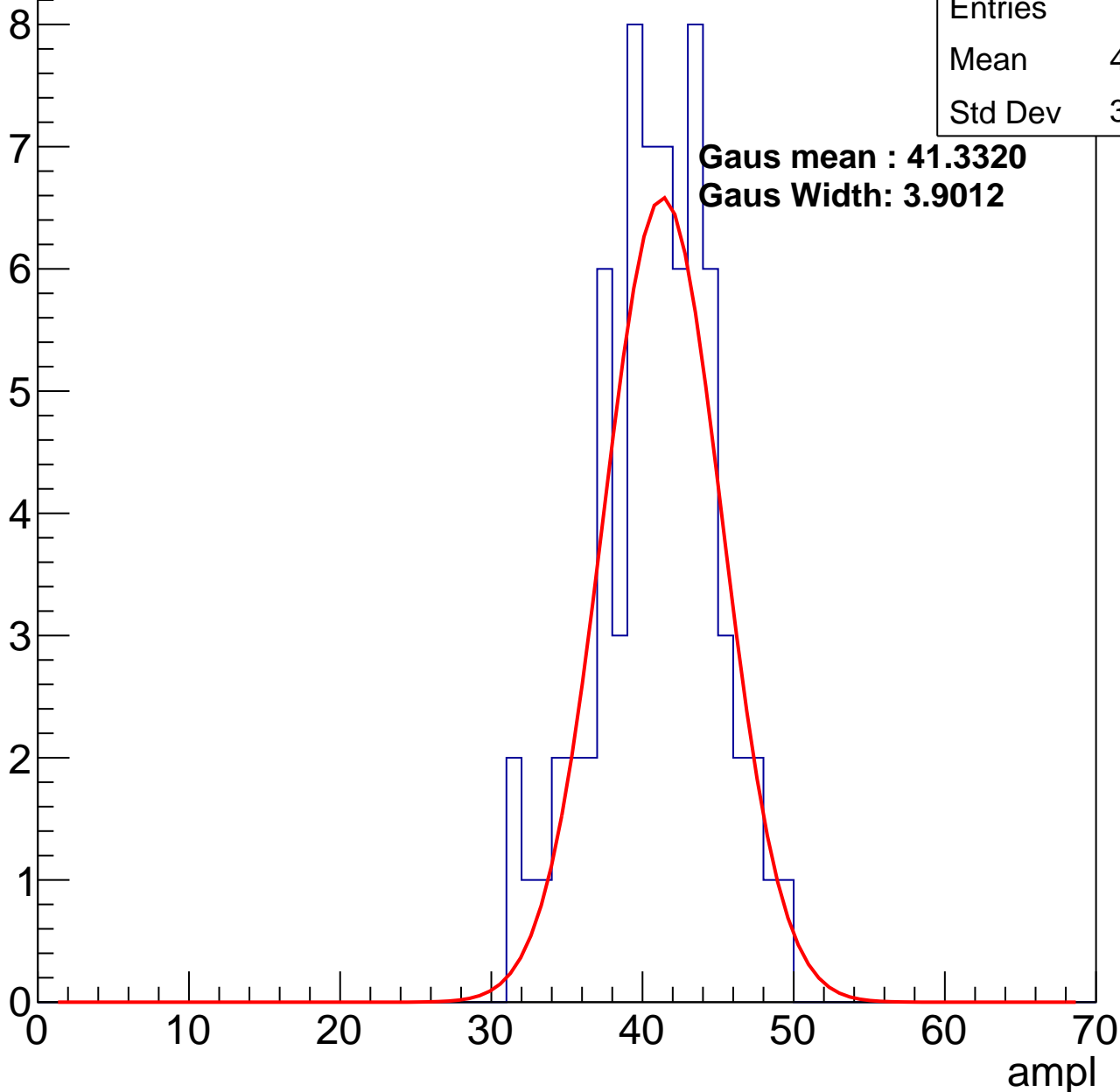
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	40.43
Std Dev	3.926

**Gaus mean : 41.3320**

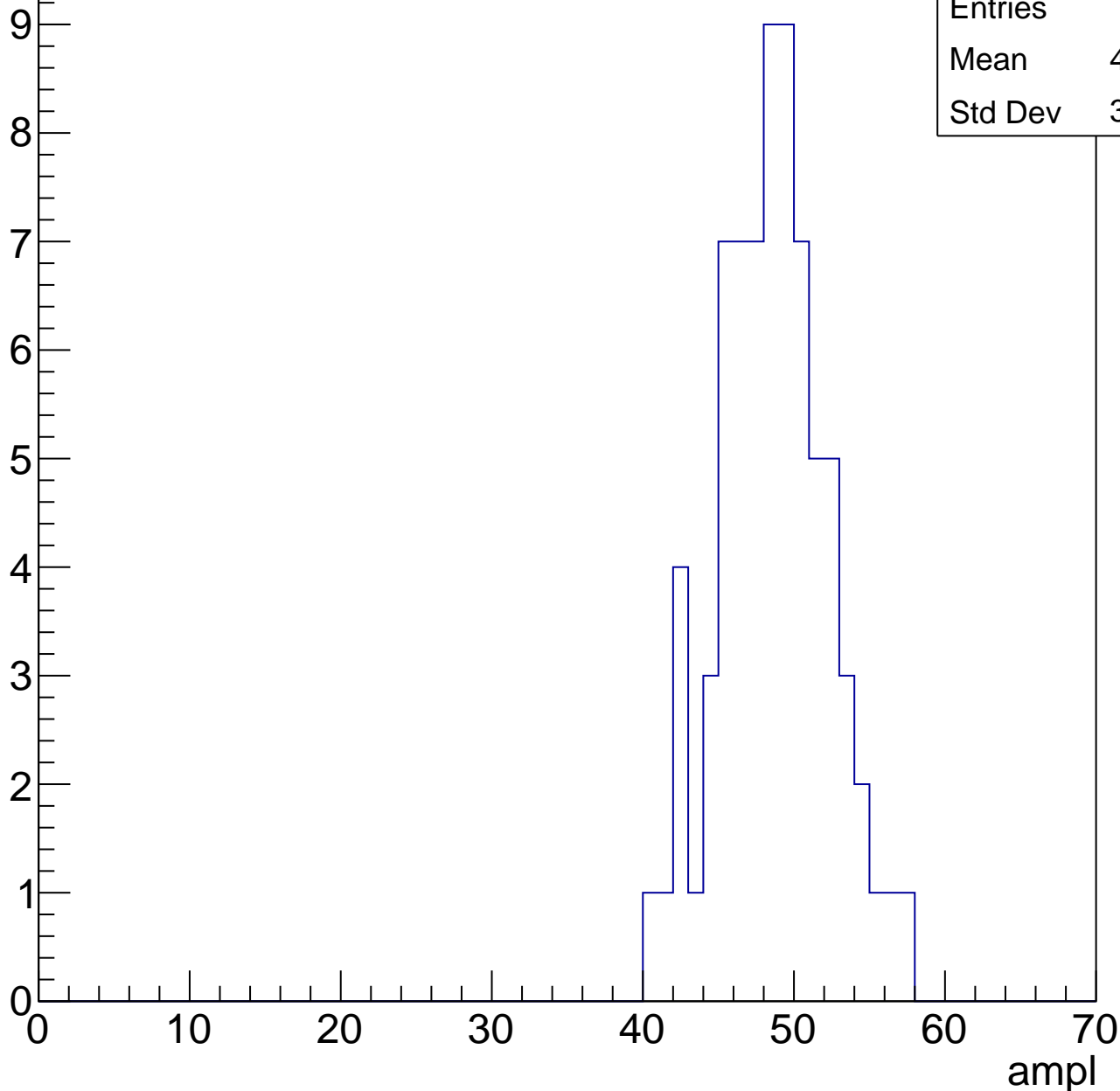
**Gaus Width: 3.9012**



# B1L102S, U5-ch51, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



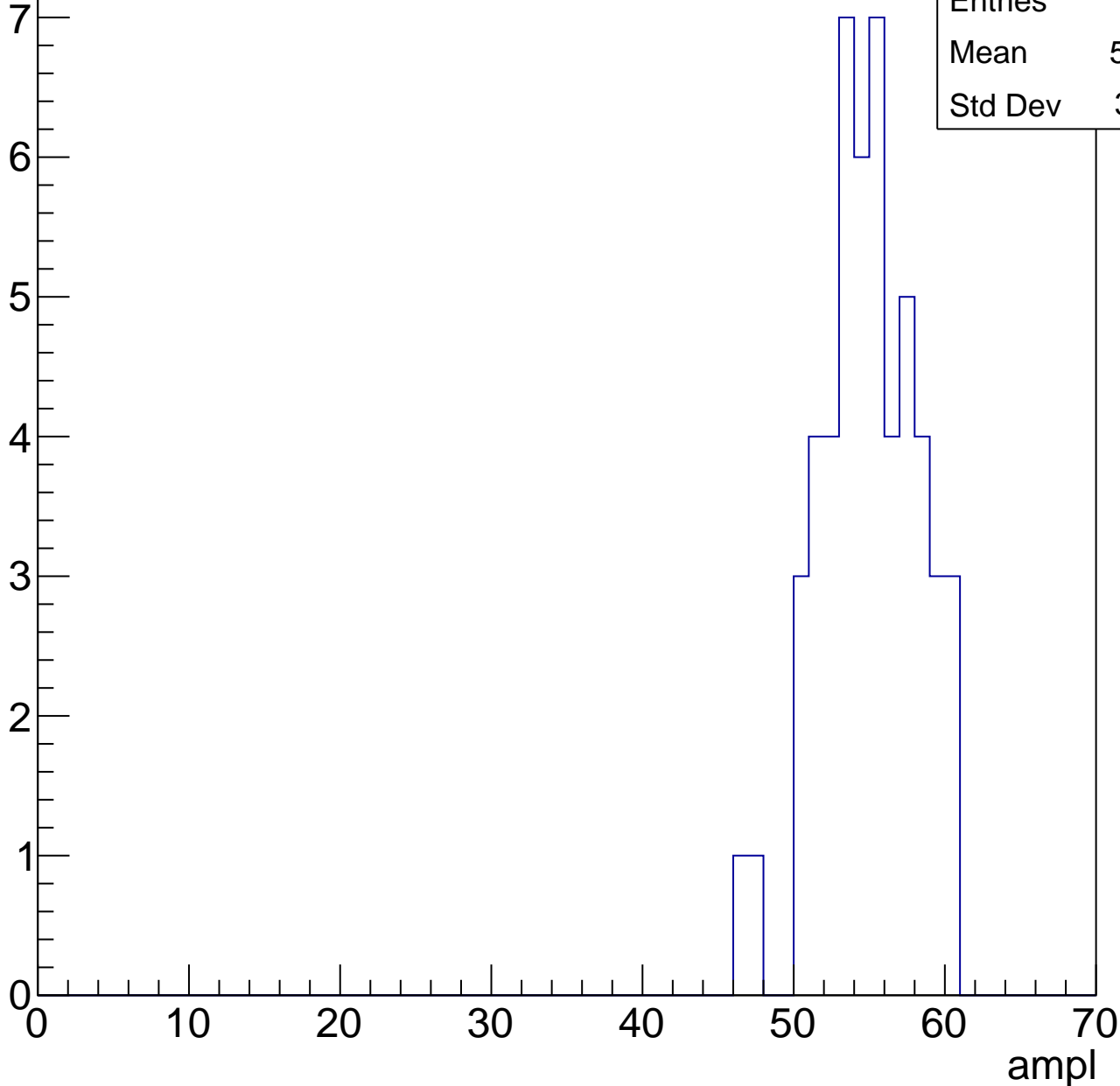
Entries	74
Mean	48.15
Std Dev	3.544

# B1L102S, U5-ch51, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

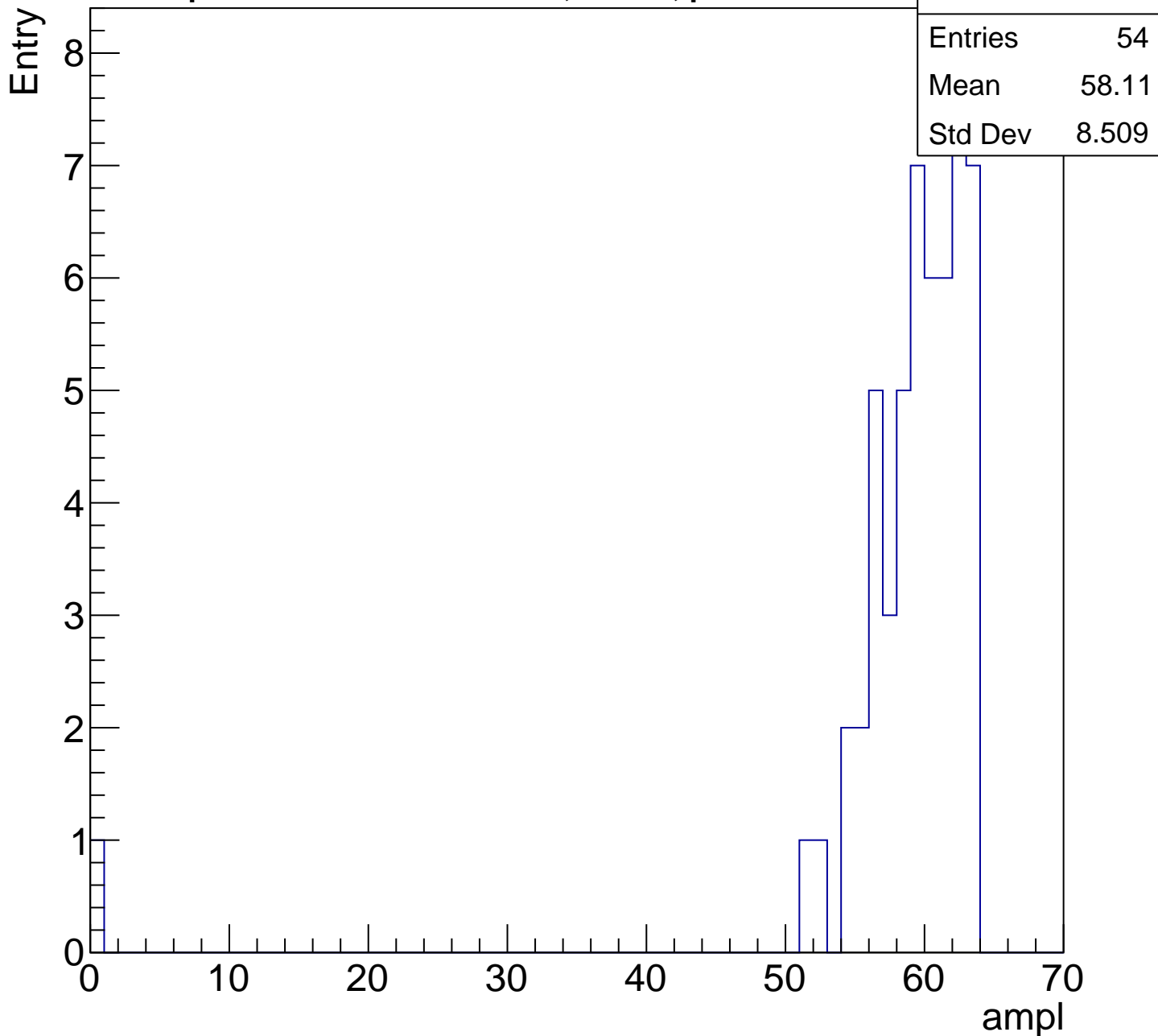
Entry

Entries	52
Mean	54.48
Std Dev	3.171



# B1L102S, U5-ch51, adc5

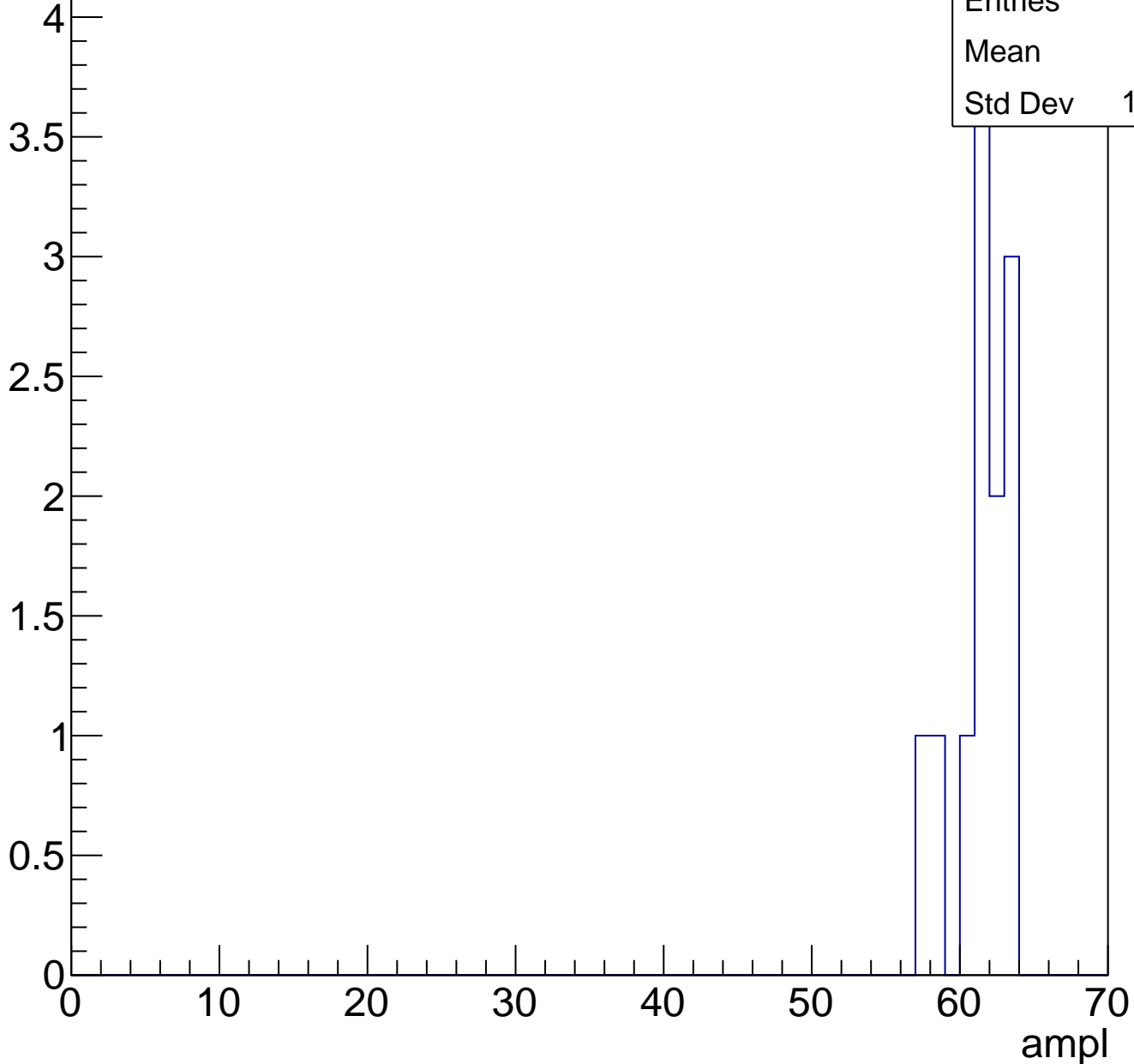
calib\_packv5\_042523\_0143.root, FC#11, port A2



# B1L102S, U5-ch51, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U5-ch51, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U5-ch52, adc0

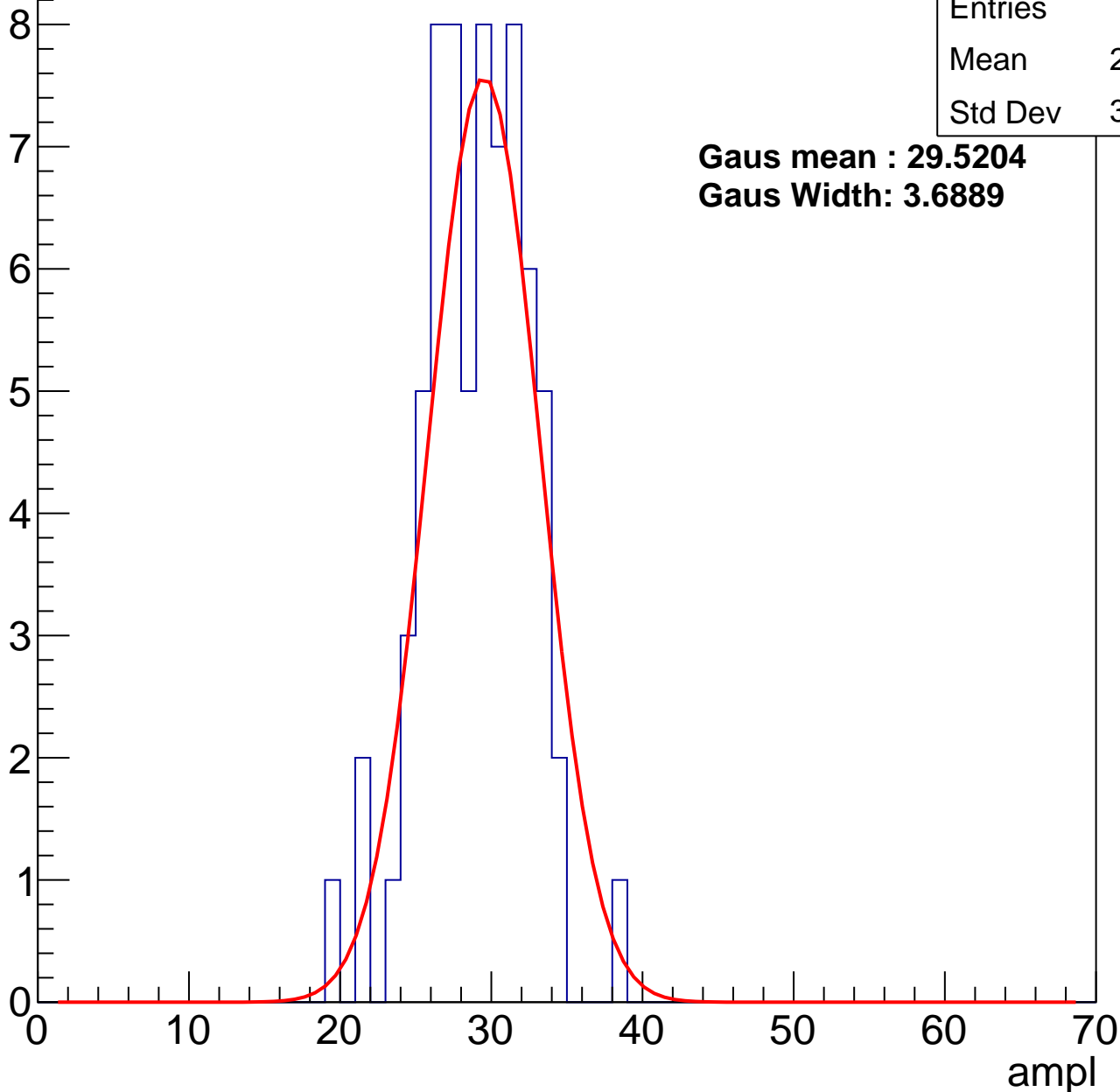
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	28.54
Std Dev	3.417

**Gaus mean : 29.5204**

**Gaus Width: 3.6889**



# B1L102S, U5-ch52, adc1

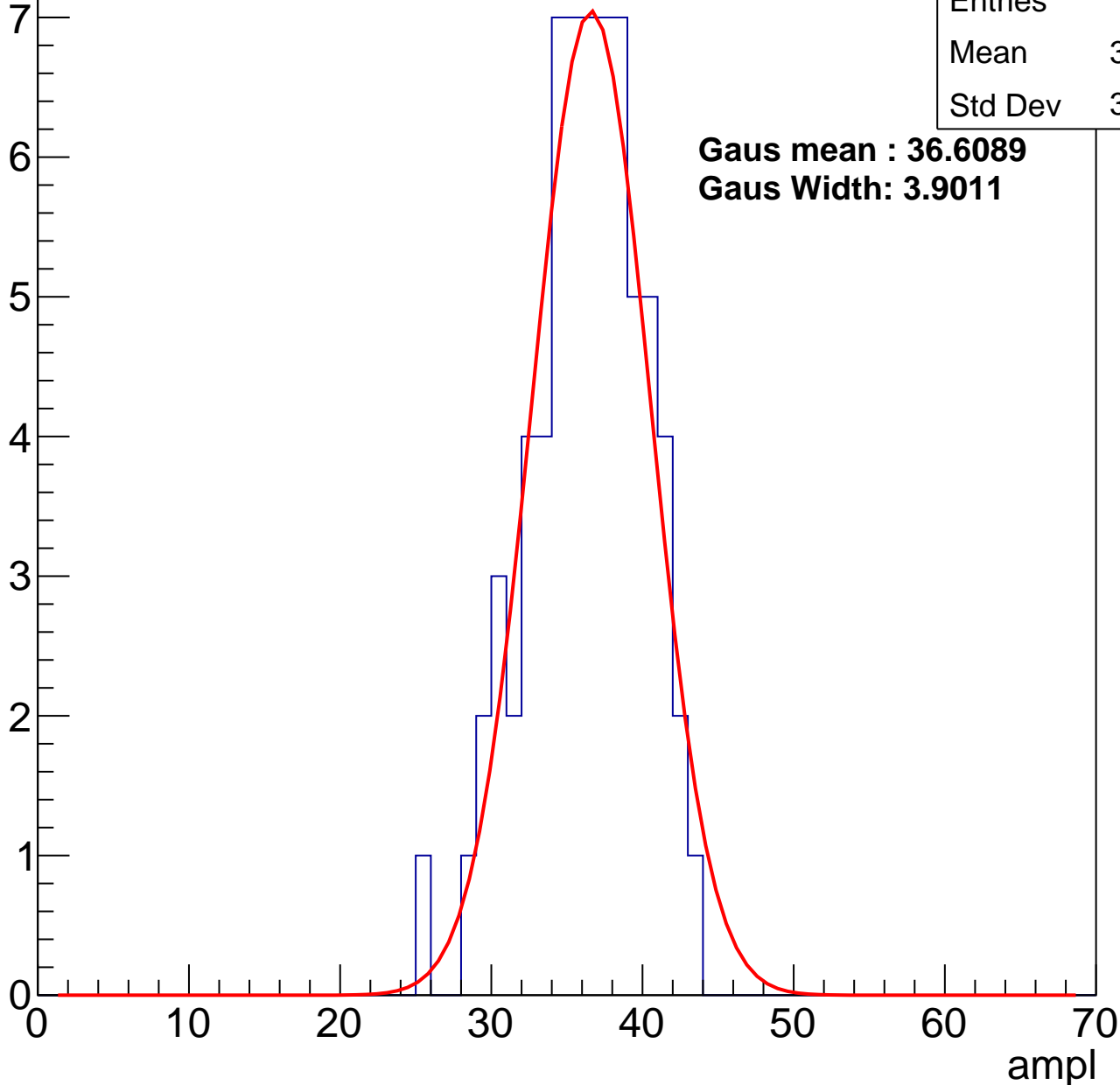
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	35.78
Std Dev	3.718

**Gaus mean : 36.6089**

**Gaus Width: 3.9011**



# B1L102S, U5-ch52, adc2

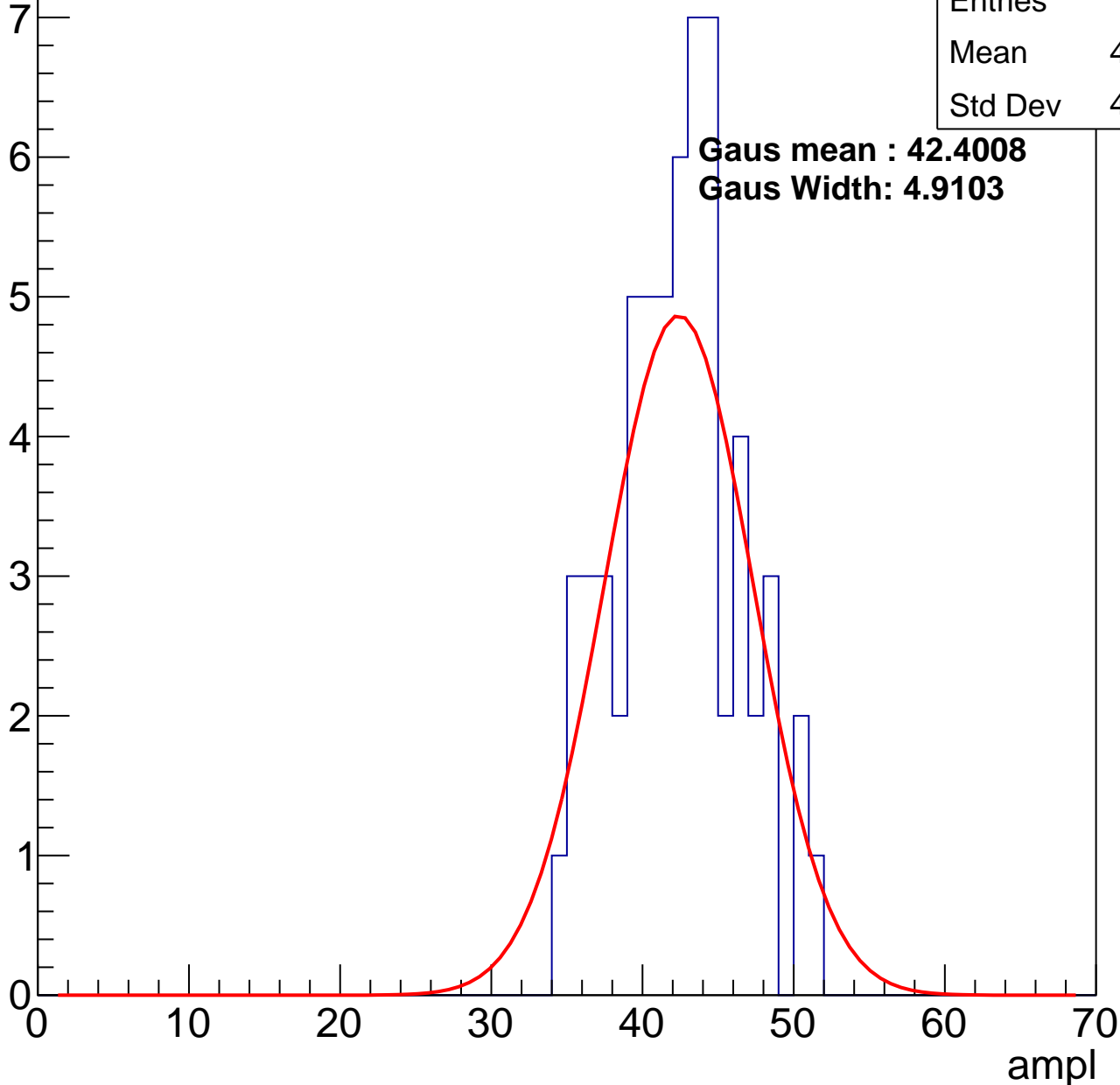
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	41.93
Std Dev	4.008

**Gaus mean : 42.4008**

**Gaus Width: 4.9103**

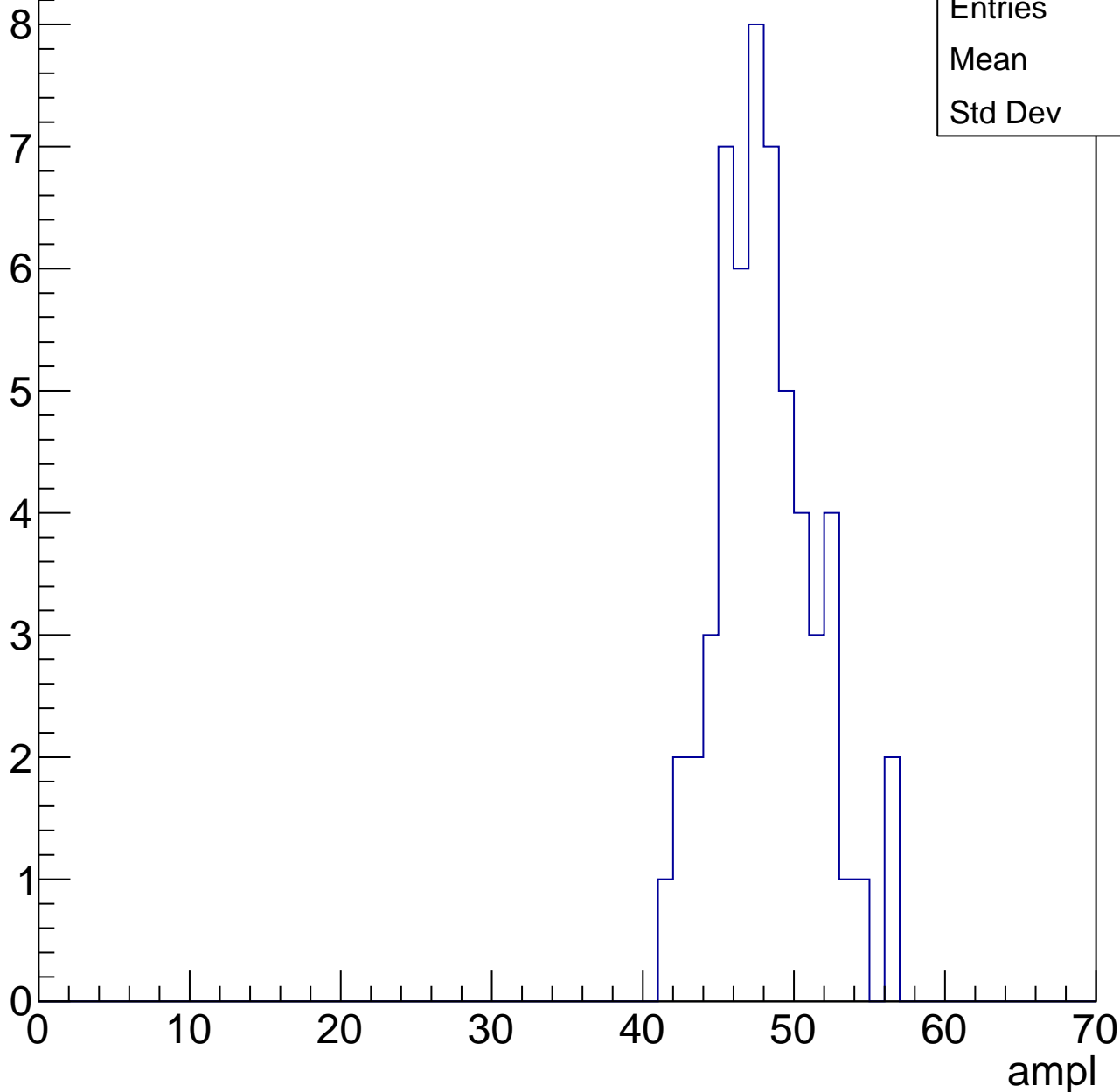


# B1L102S, U5-ch52, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	47.7
Std Dev	3.3

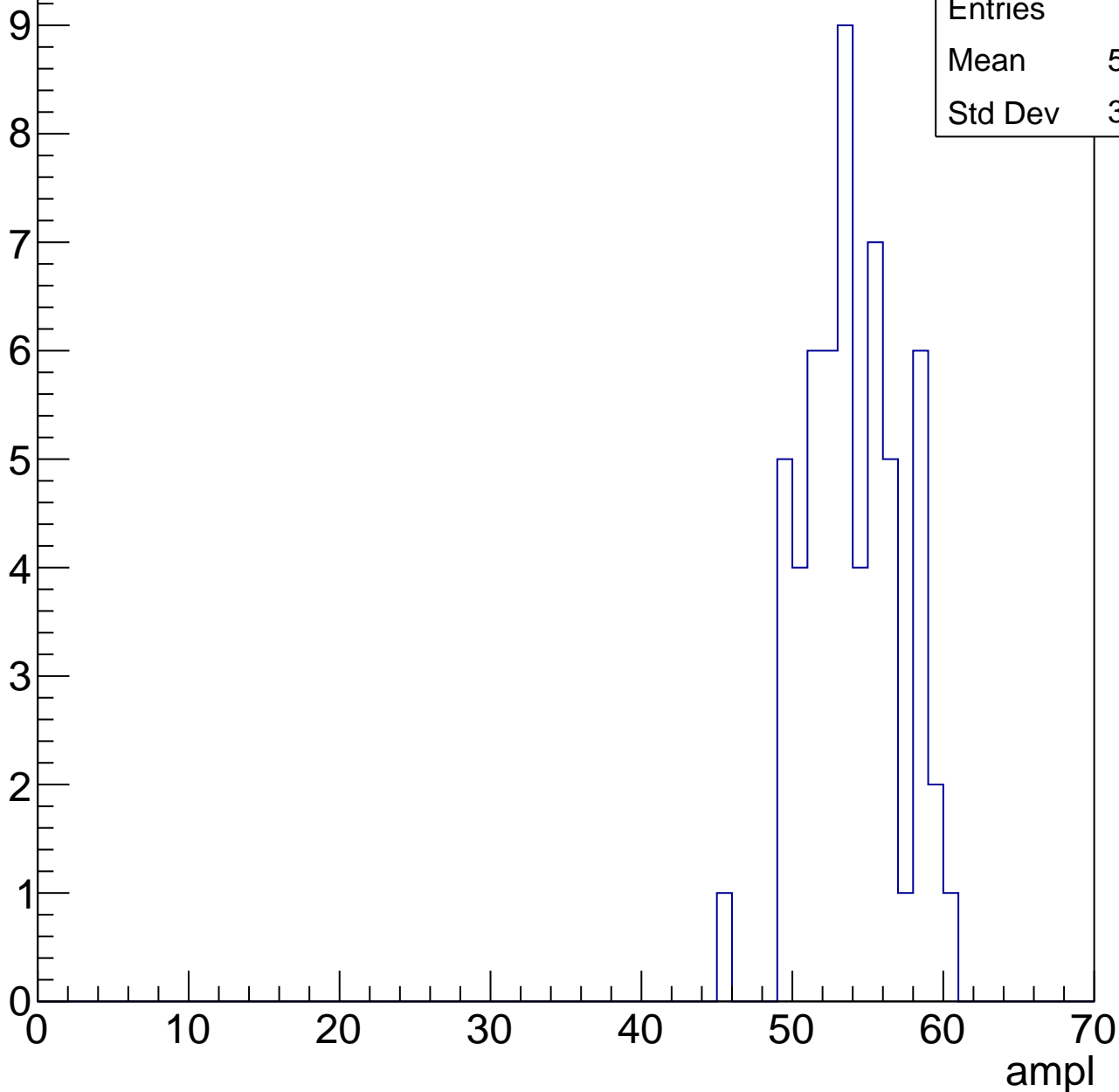


# B1L102S, U5-ch52, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

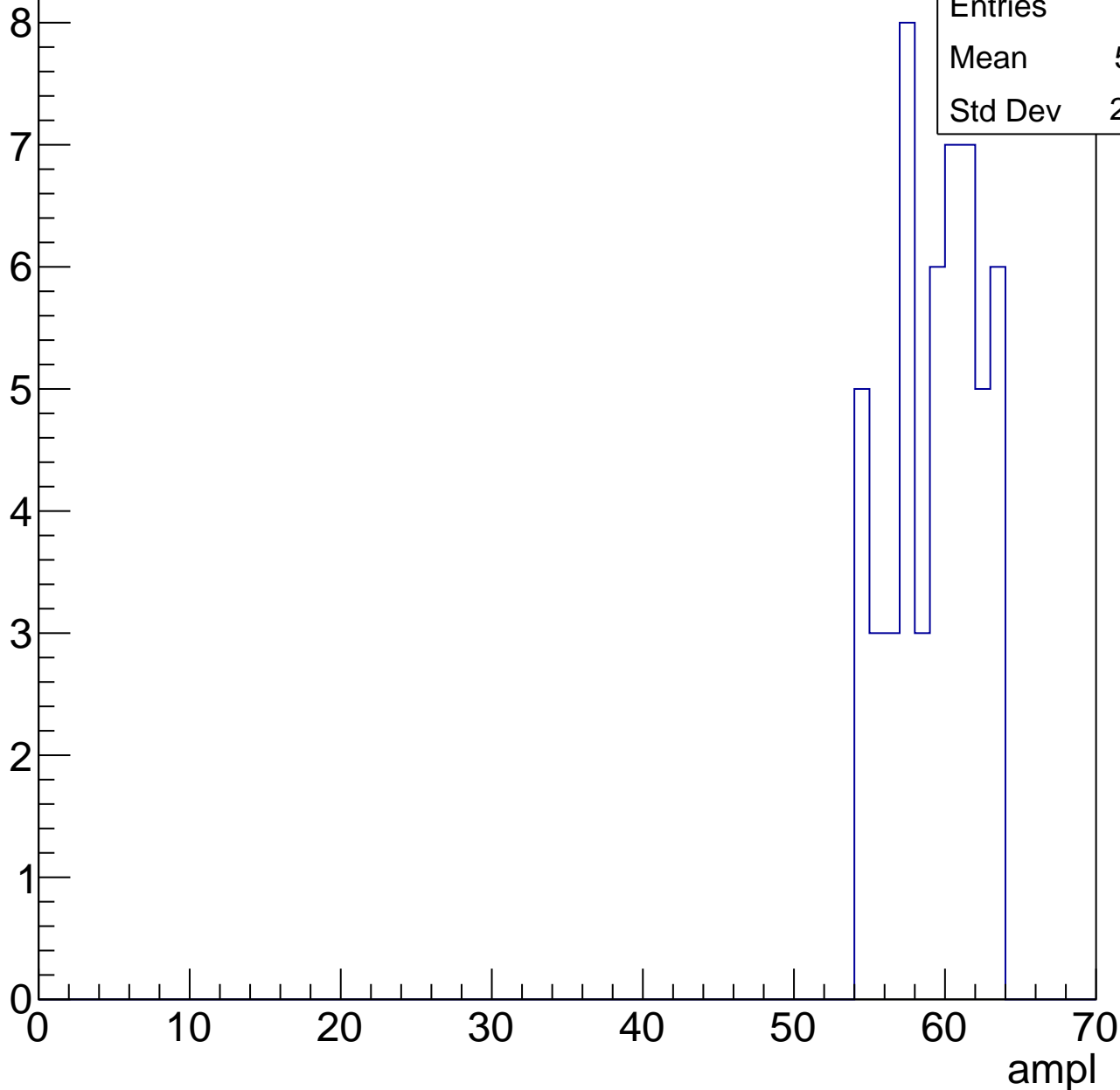
Entries	57
Mean	53.49
Std Dev	3.135



# B1L102S, U5-ch52, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



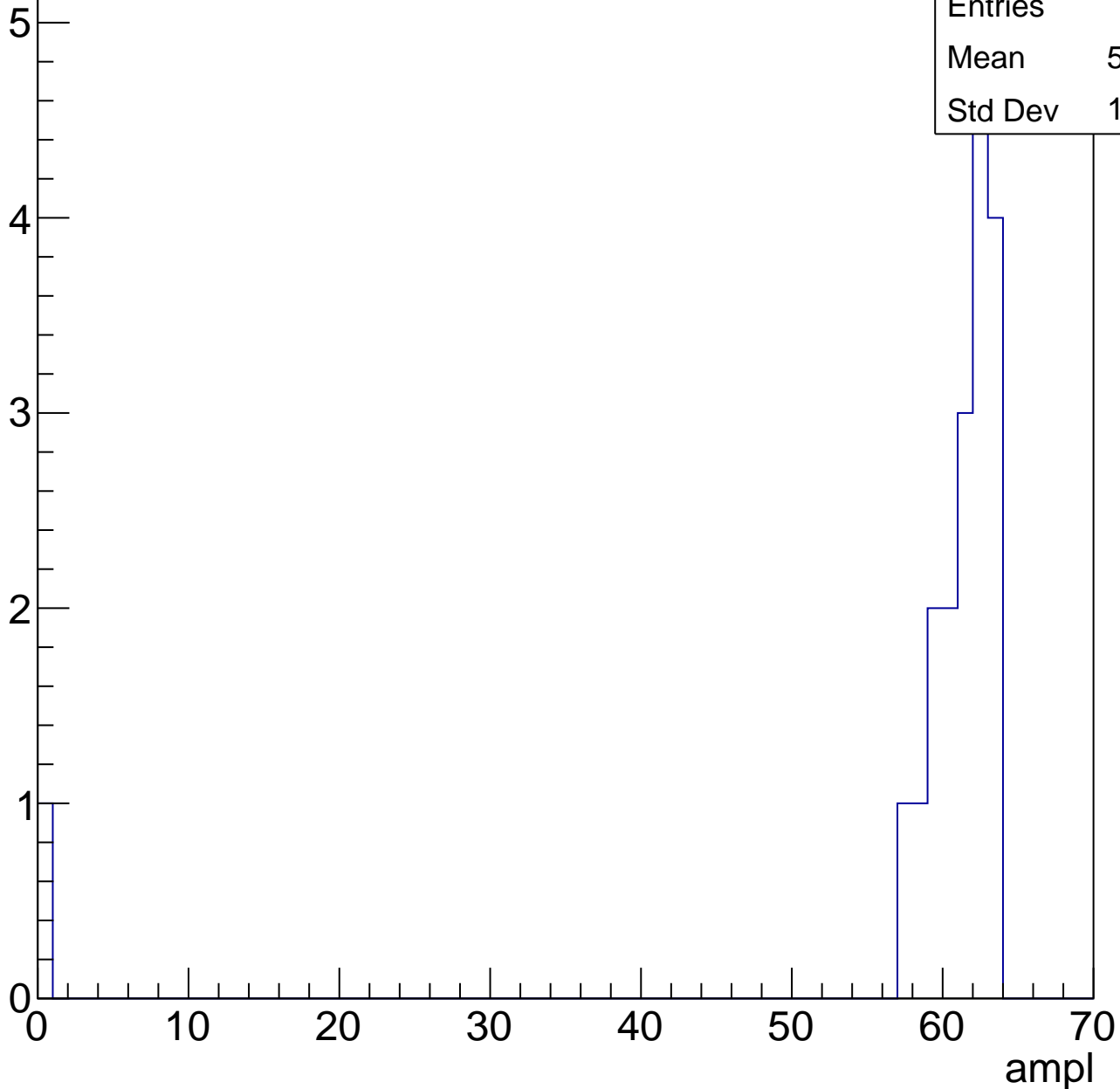
Entries	53
Mean	58.91
Std Dev	2.783

# B1L102S, U5-ch52, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	19
Mean	57.79
Std Dev	13.73





# B1L102S, U5-ch52, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U5-ch53, adc0

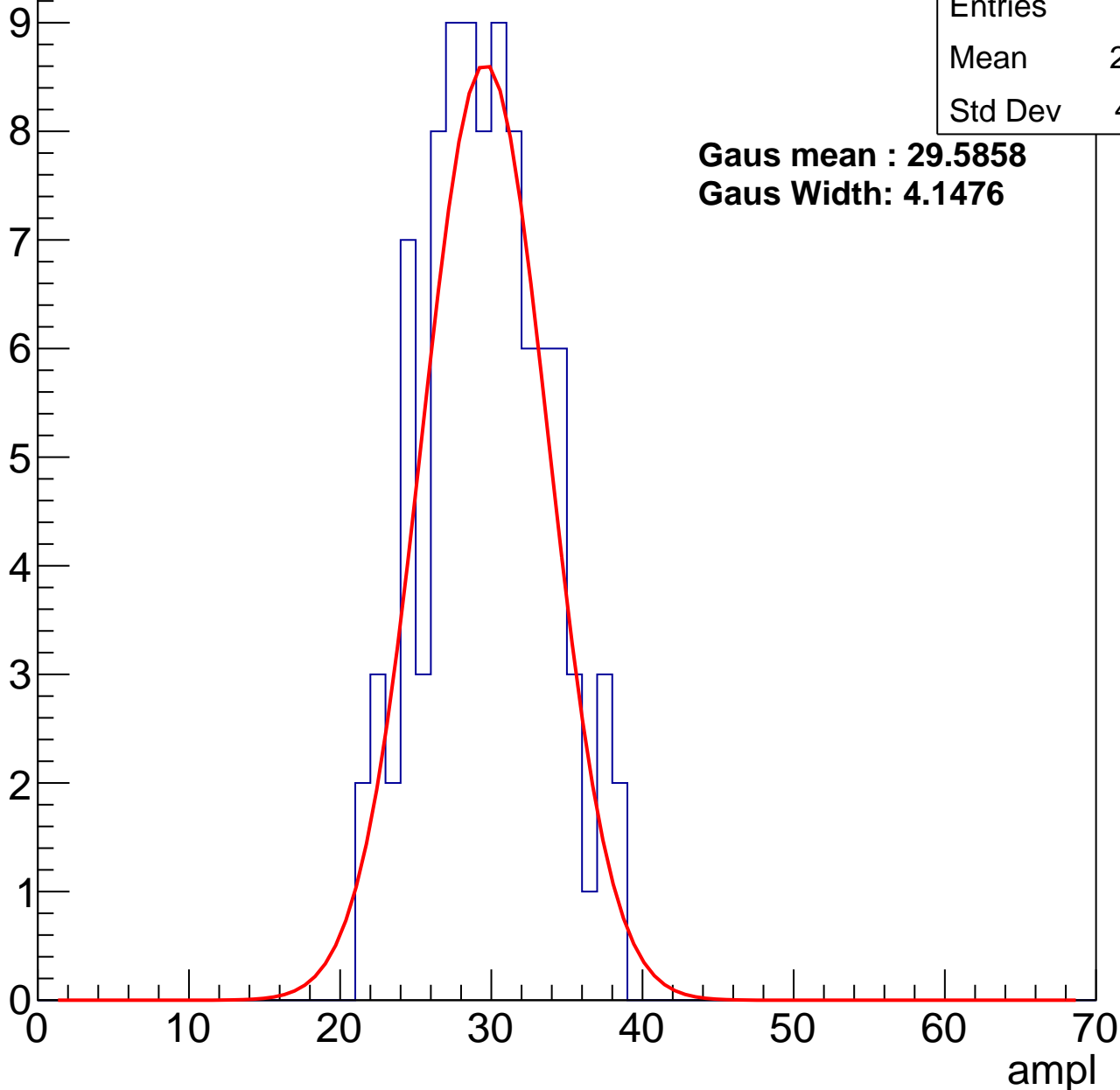
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	95
Mean	29.18
Std Dev	4.021

**Gaus mean : 29.5858**

**Gaus Width: 4.1476**



# B1L102S, U5-ch53, adc1

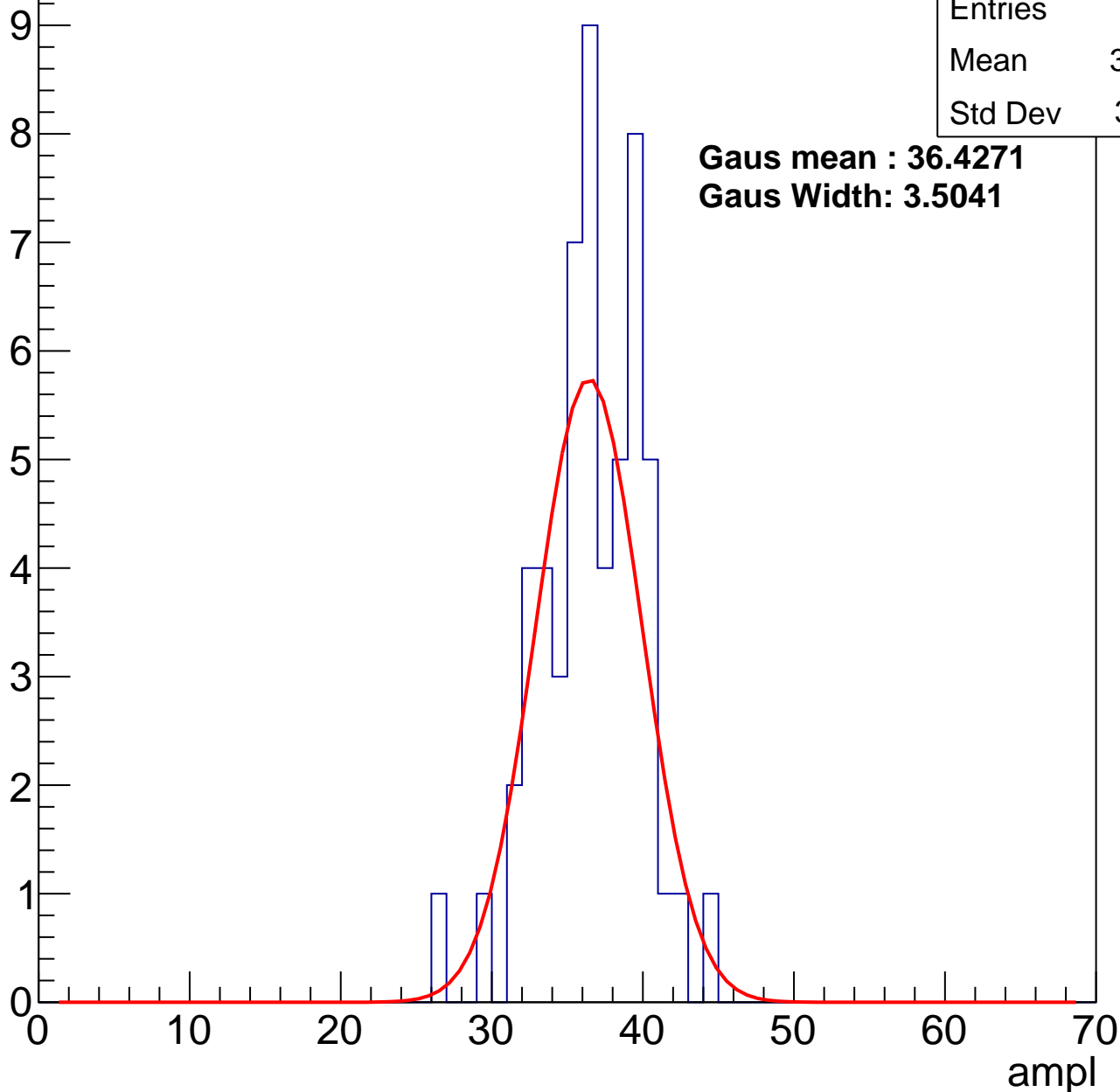
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	36.16
Std Dev	3.321

**Gaus mean : 36.4271**

**Gaus Width: 3.5041**



# B1L102S, U5-ch53, adc2

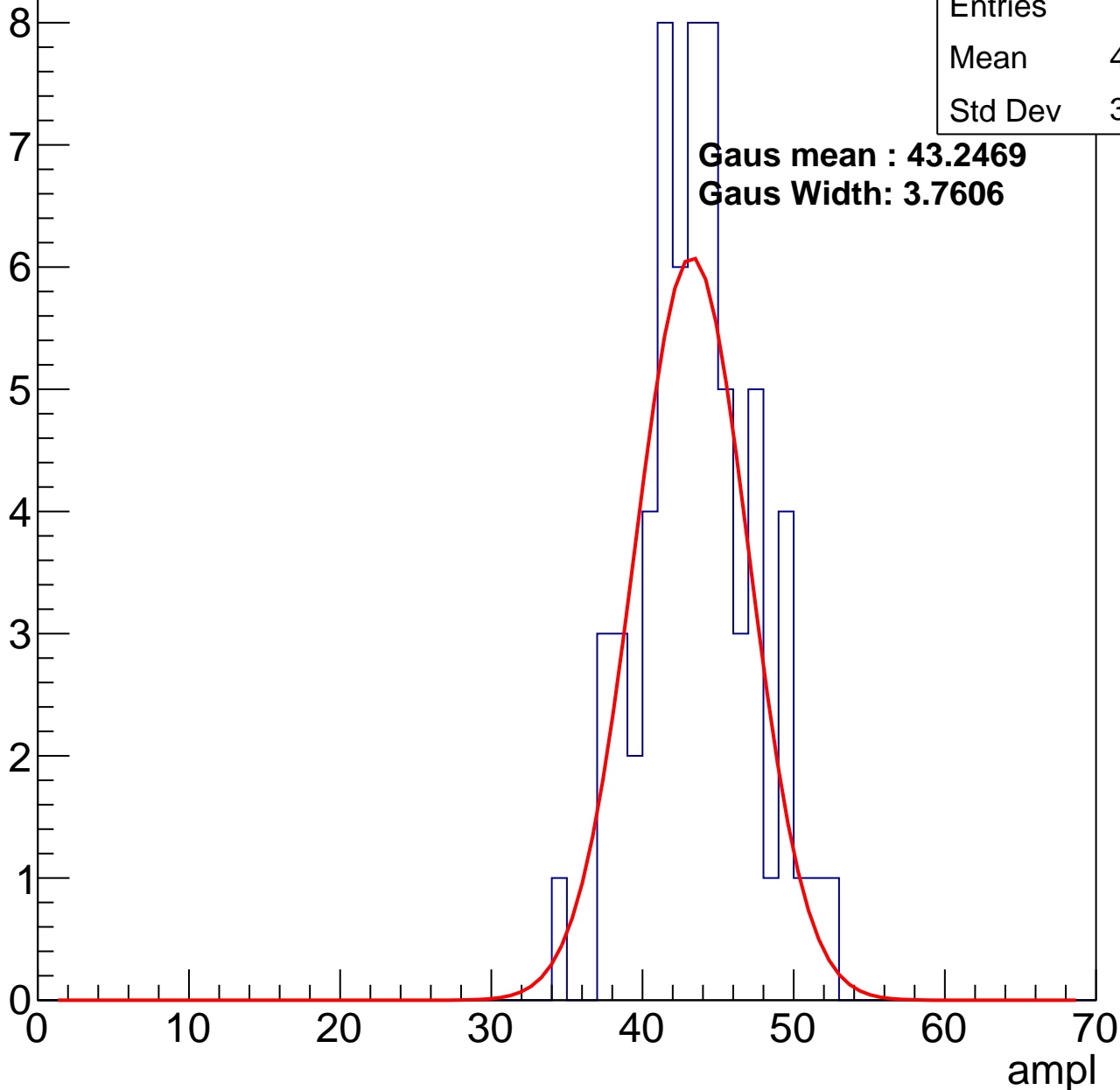
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	43.25
Std Dev	3.674

**Gaus mean : 43.2469**

**Gaus Width: 3.7606**

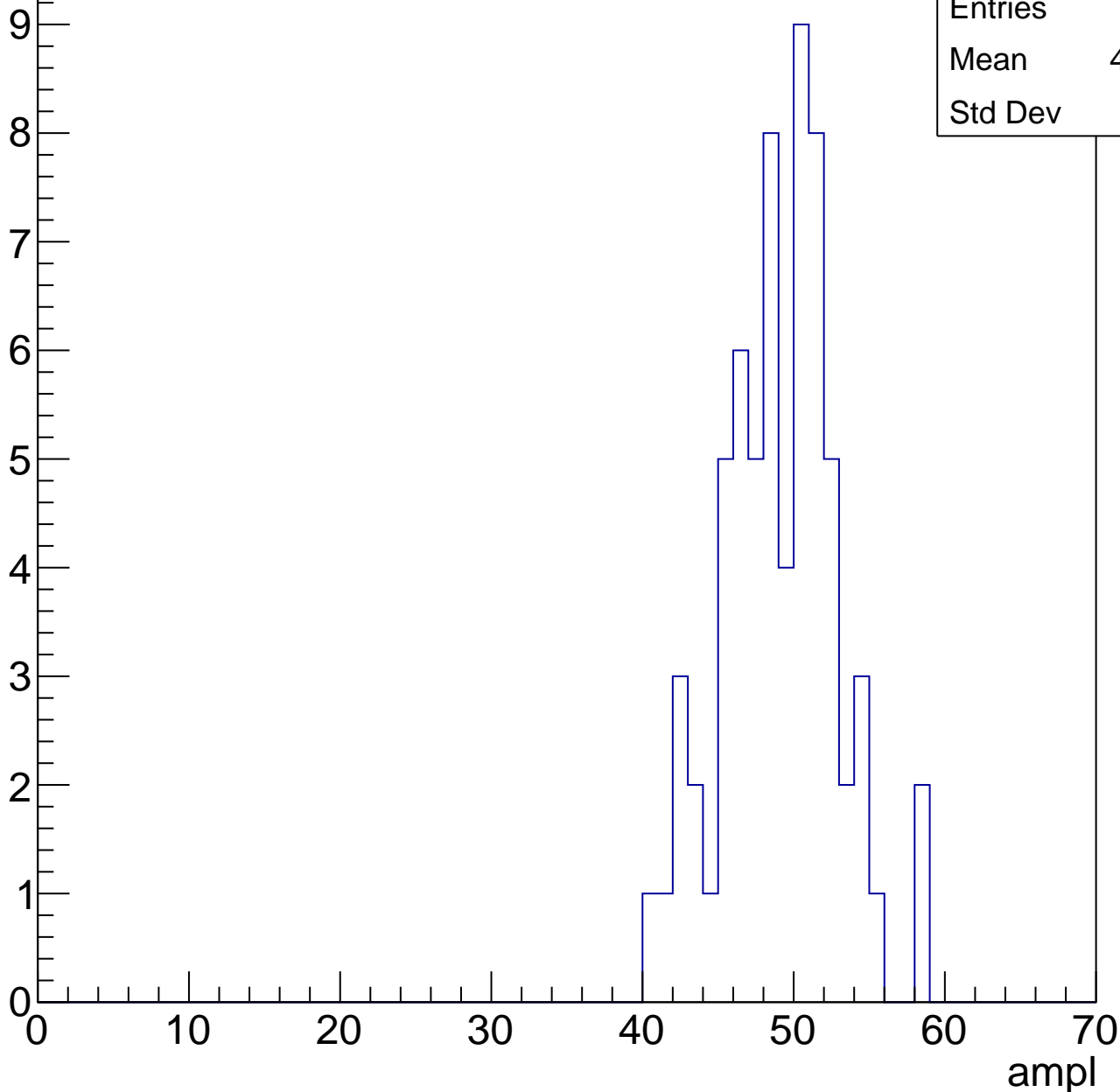


# B1L102S, U5-ch53, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	48.64
Std Dev	3.76

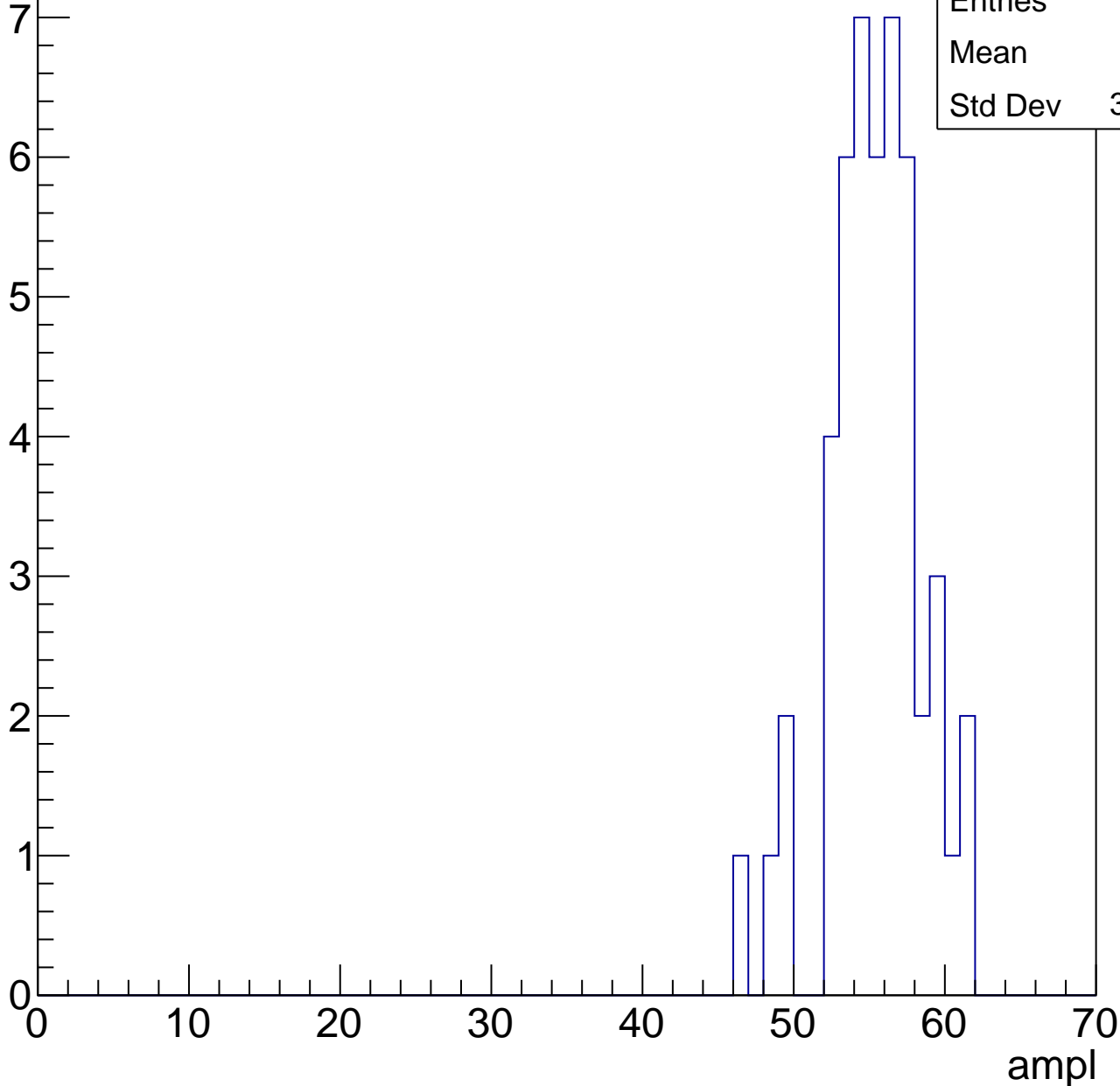


# B1L102S, U5-ch53, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	48
Mean	54.9
Std Dev	3.104



# B1L102S, U5-ch53, adc5

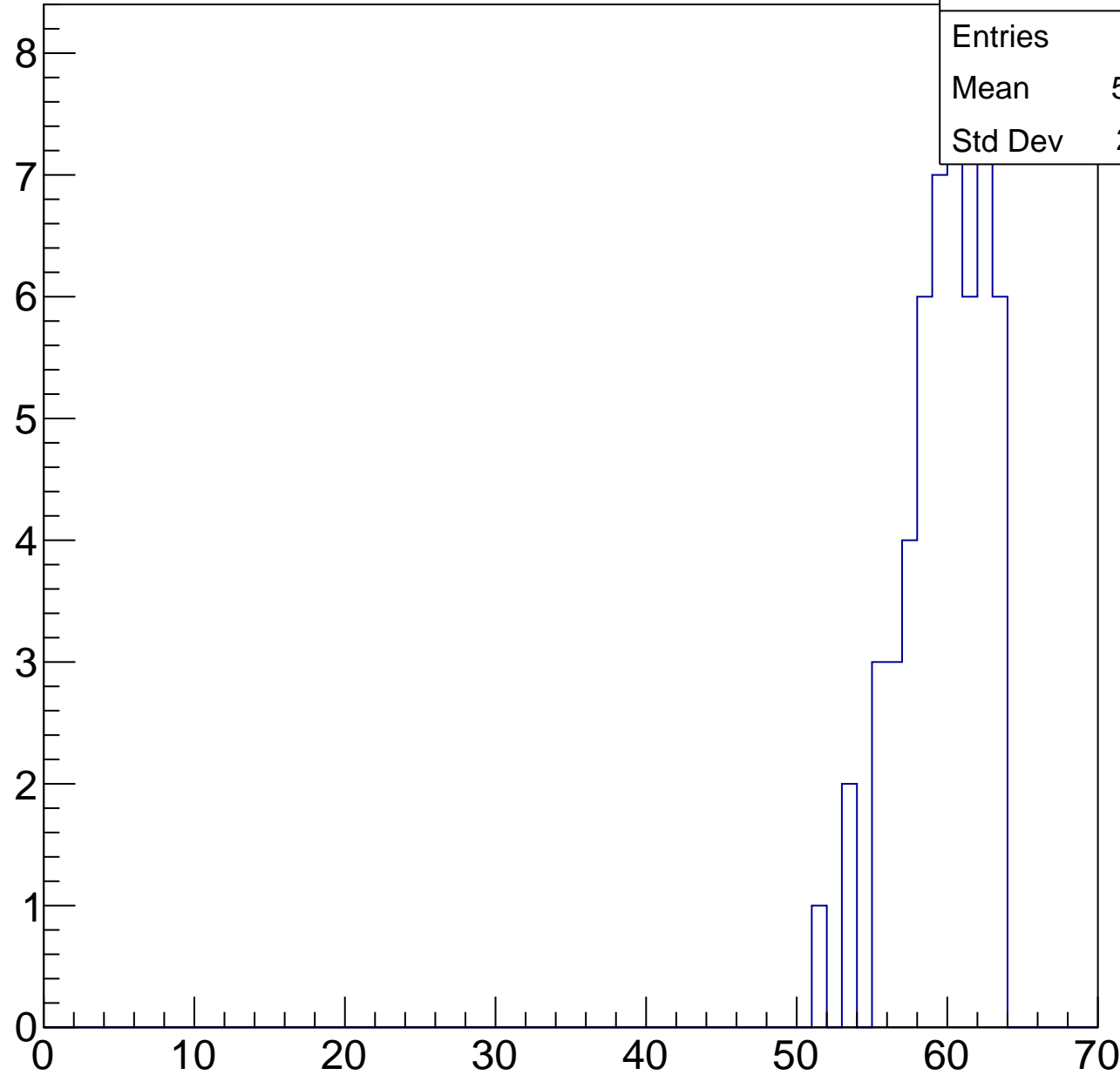
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	54
Mean	59.24
Std Dev	2.821

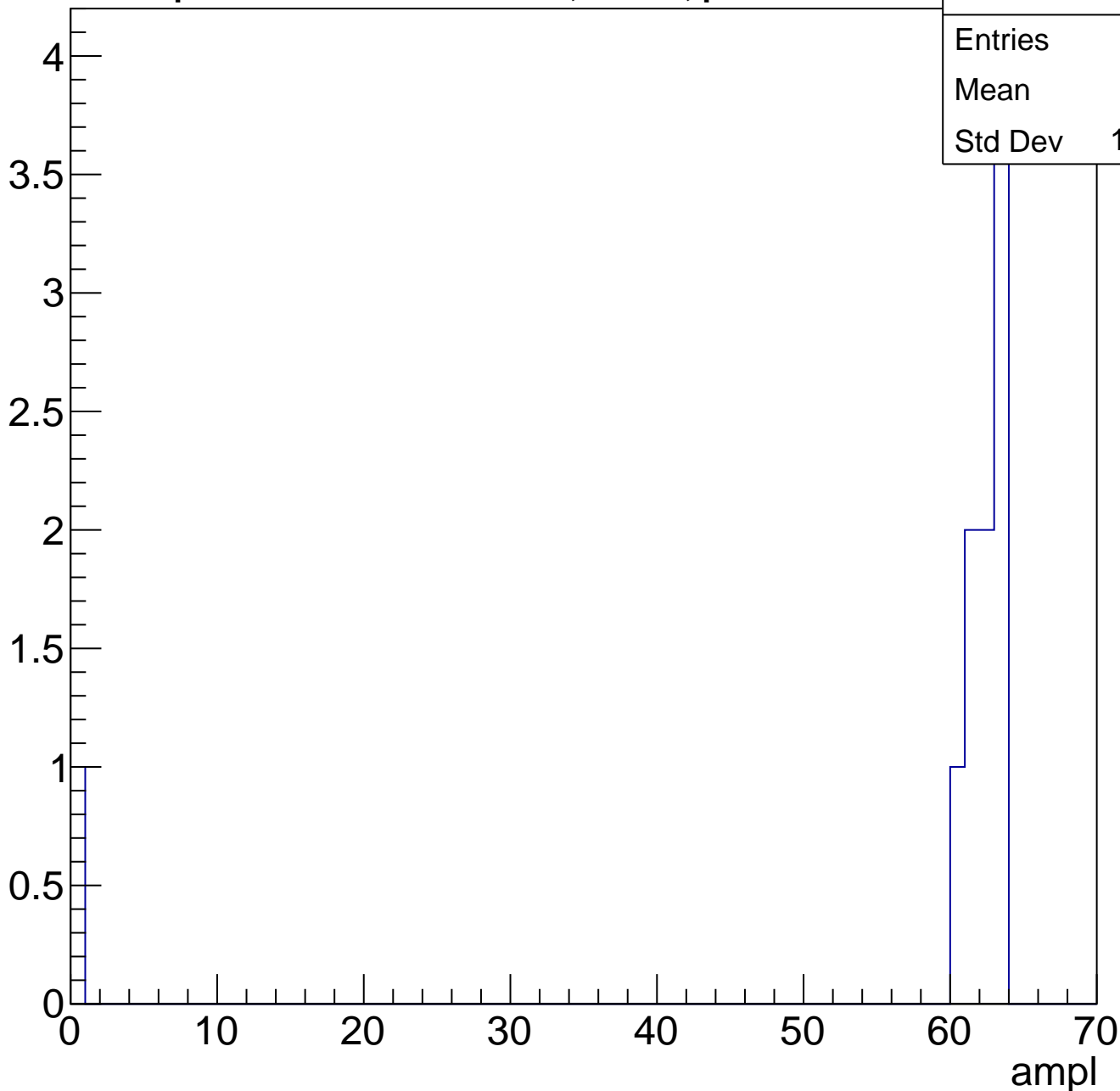
ampl



# B1L102S, U5-ch53, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U5-ch53, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U5-ch54, adc0

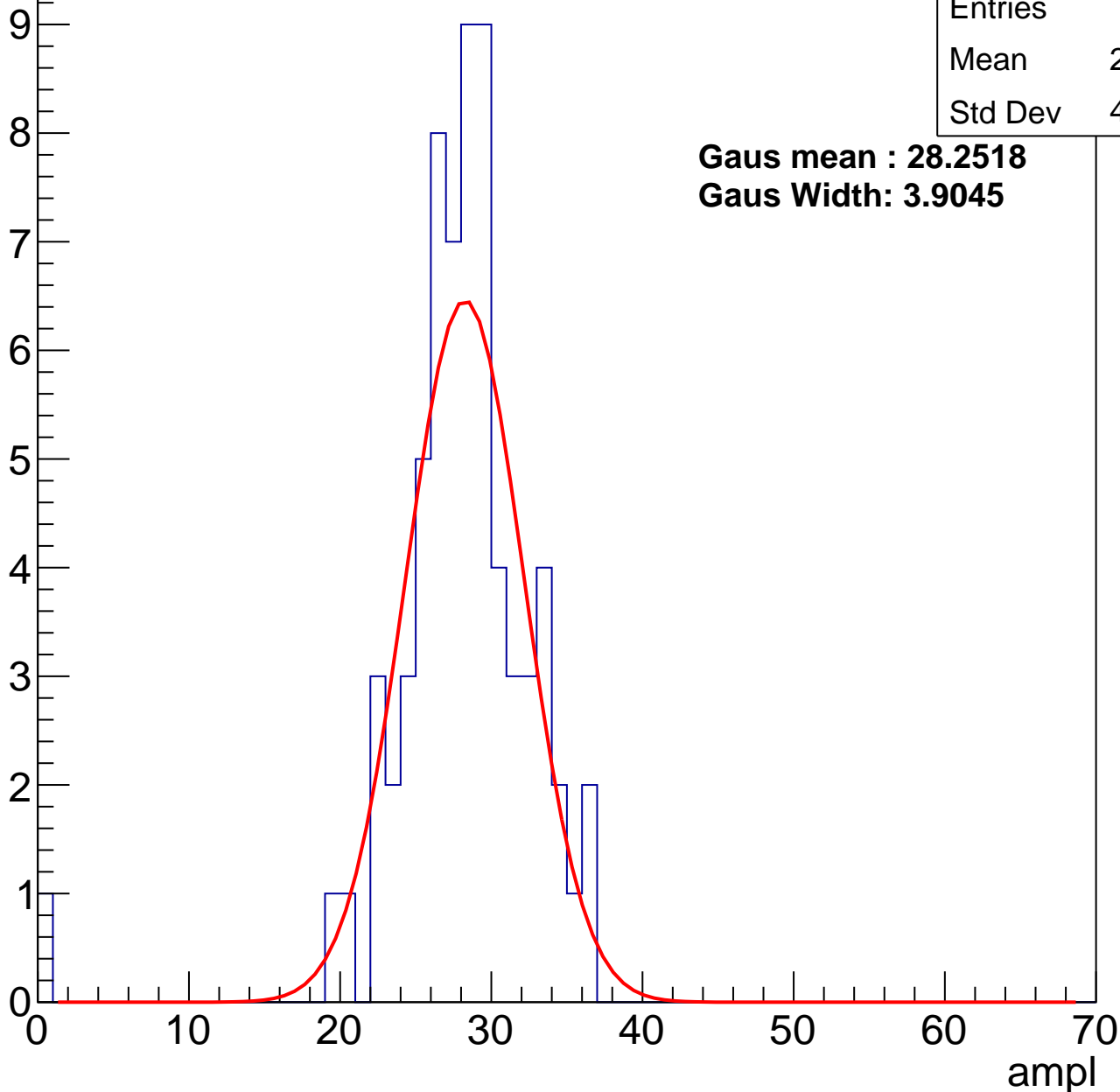
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	27.56
Std Dev	4.933

**Gaus mean : 28.2518**

**Gaus Width: 3.9045**



# B1L102S, U5-ch54, adc1

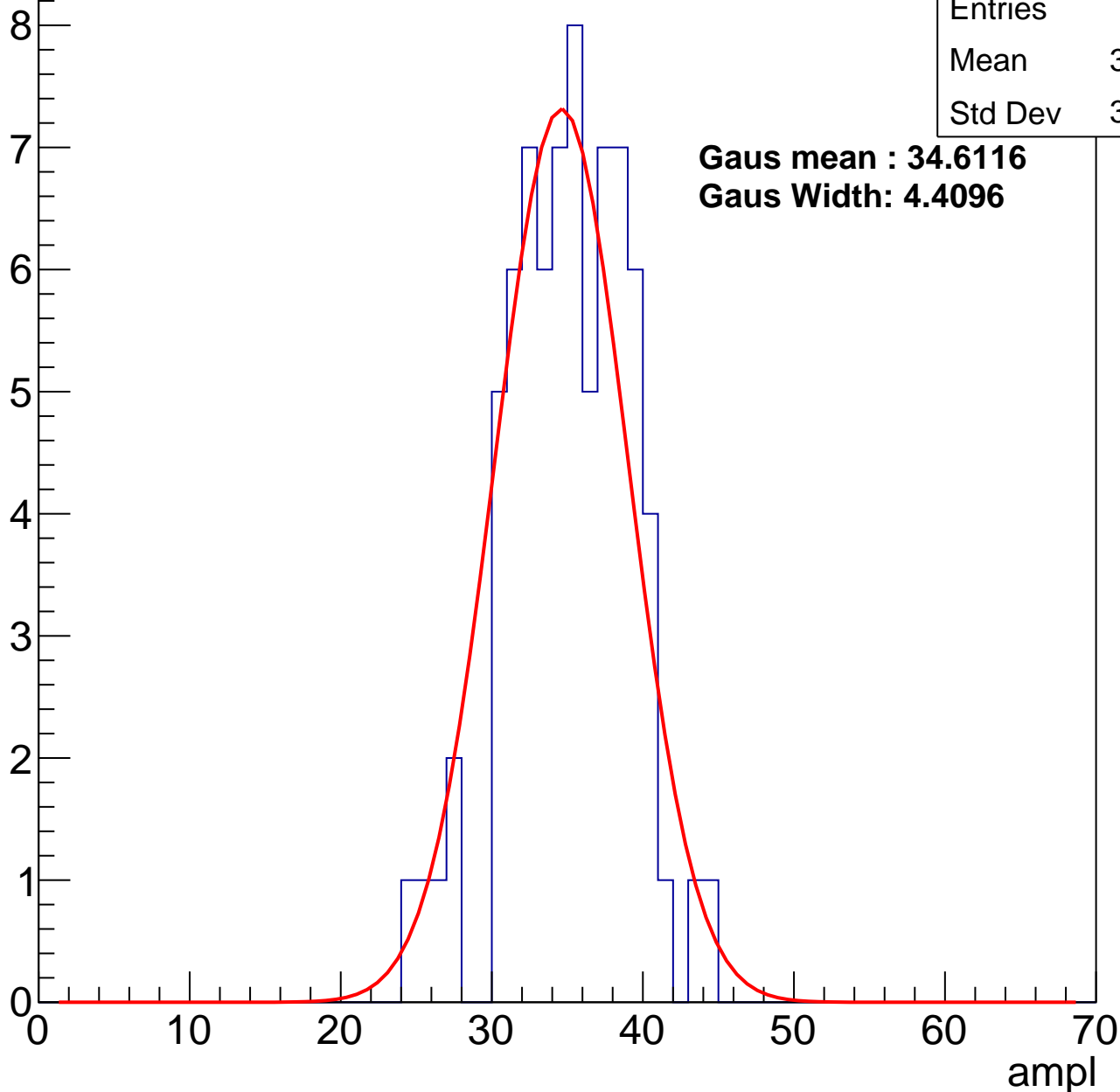
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	34.63
Std Dev	3.986

**Gaus mean : 34.6116**

**Gaus Width: 4.4096**



# B1L102S, U5-ch54, adc2

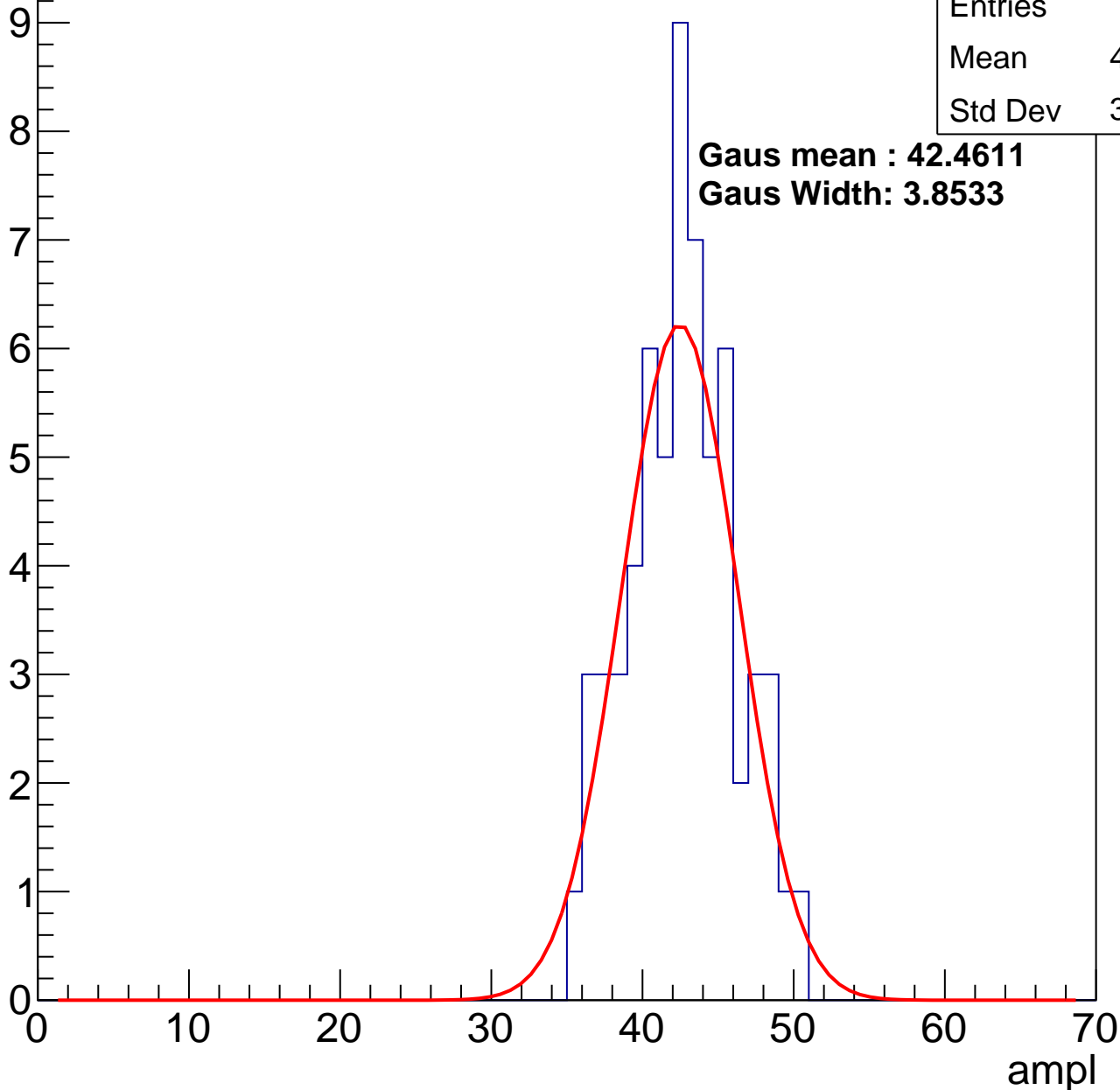
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	42.16
Std Dev	3.484

**Gaus mean : 42.4611**

**Gaus Width: 3.8533**

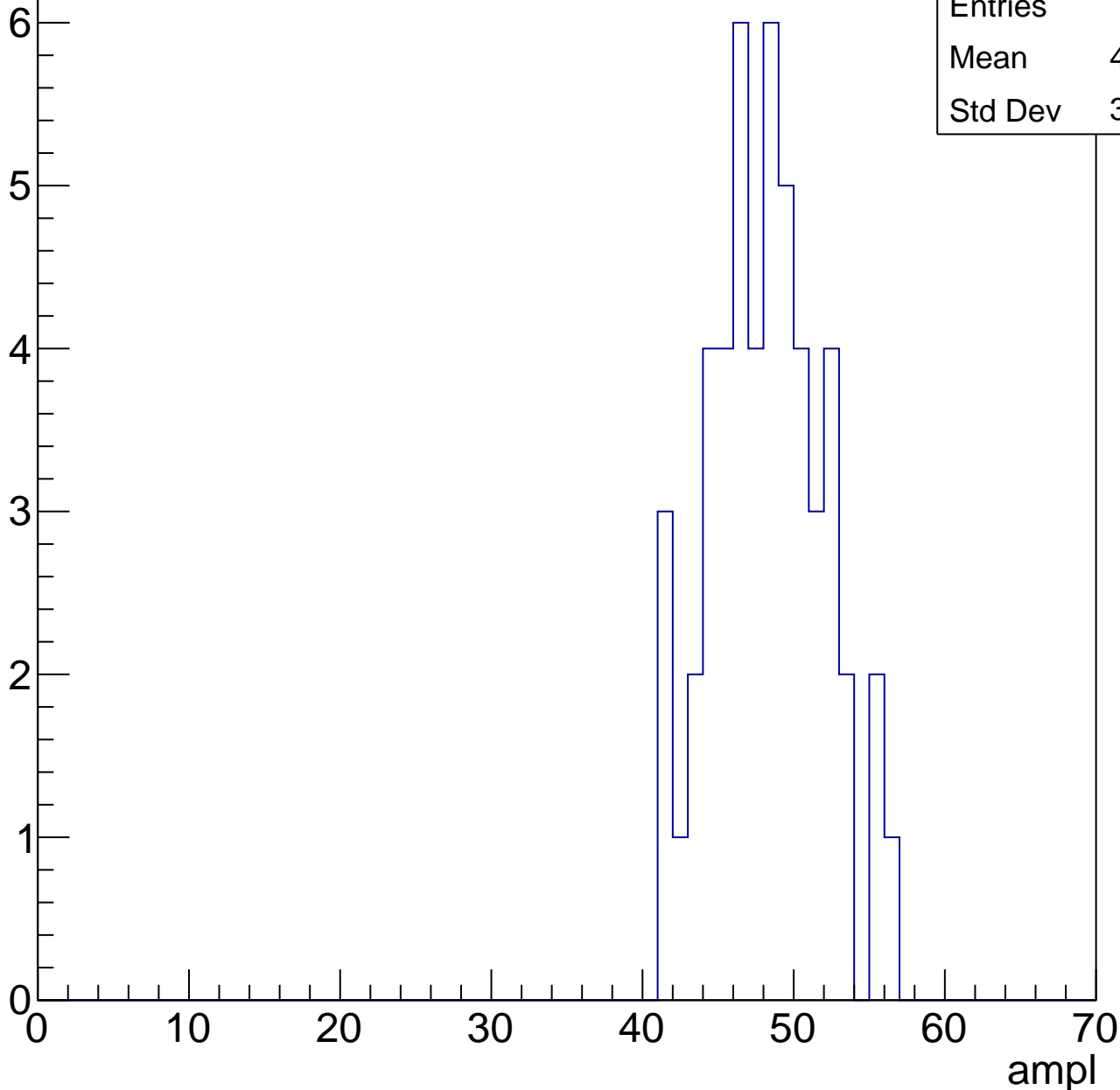


# B1L102S, U5-ch54, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

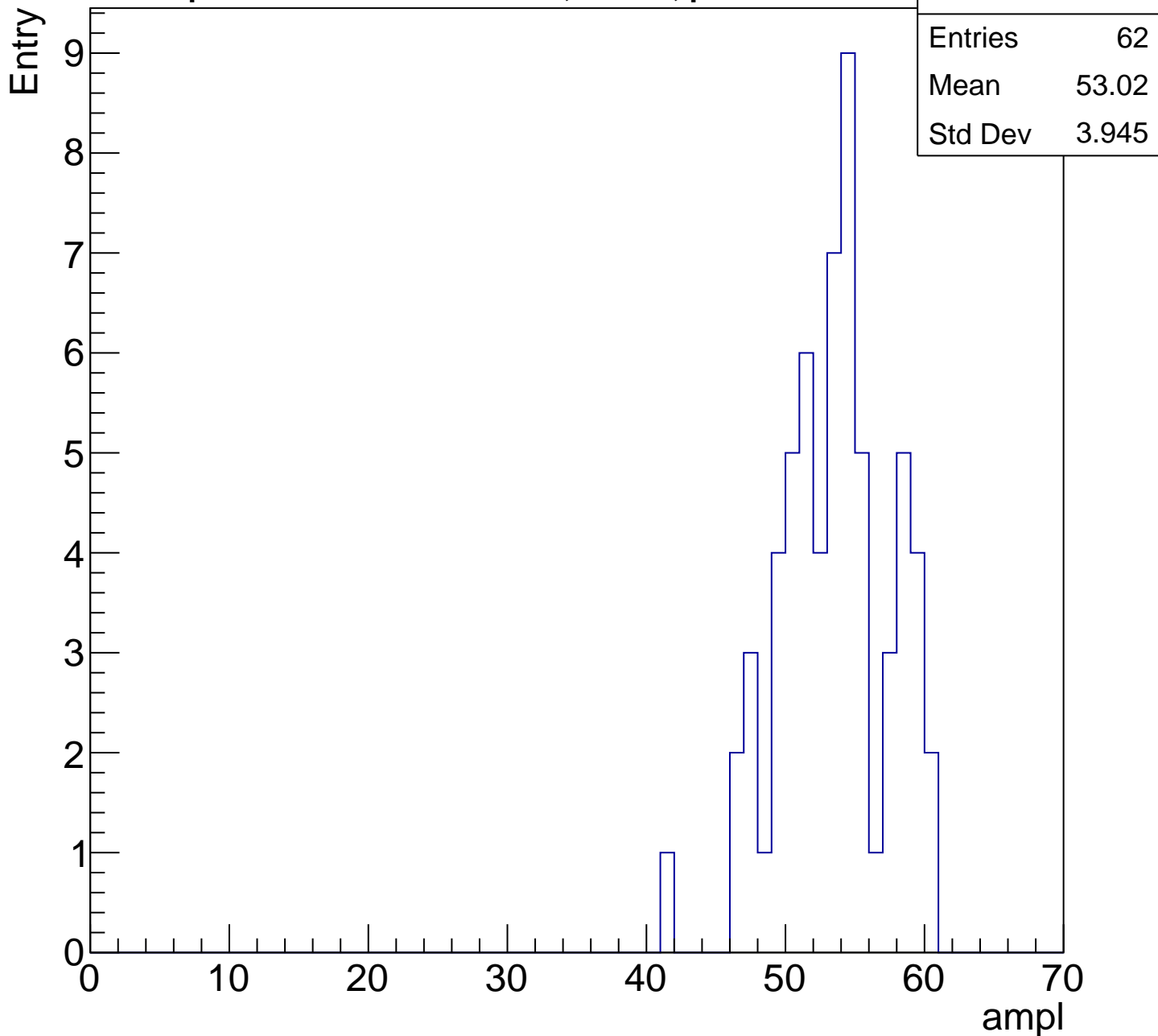
Entry

Entries	51
Mean	47.78
Std Dev	3.659



# B1L102S, U5-ch54, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

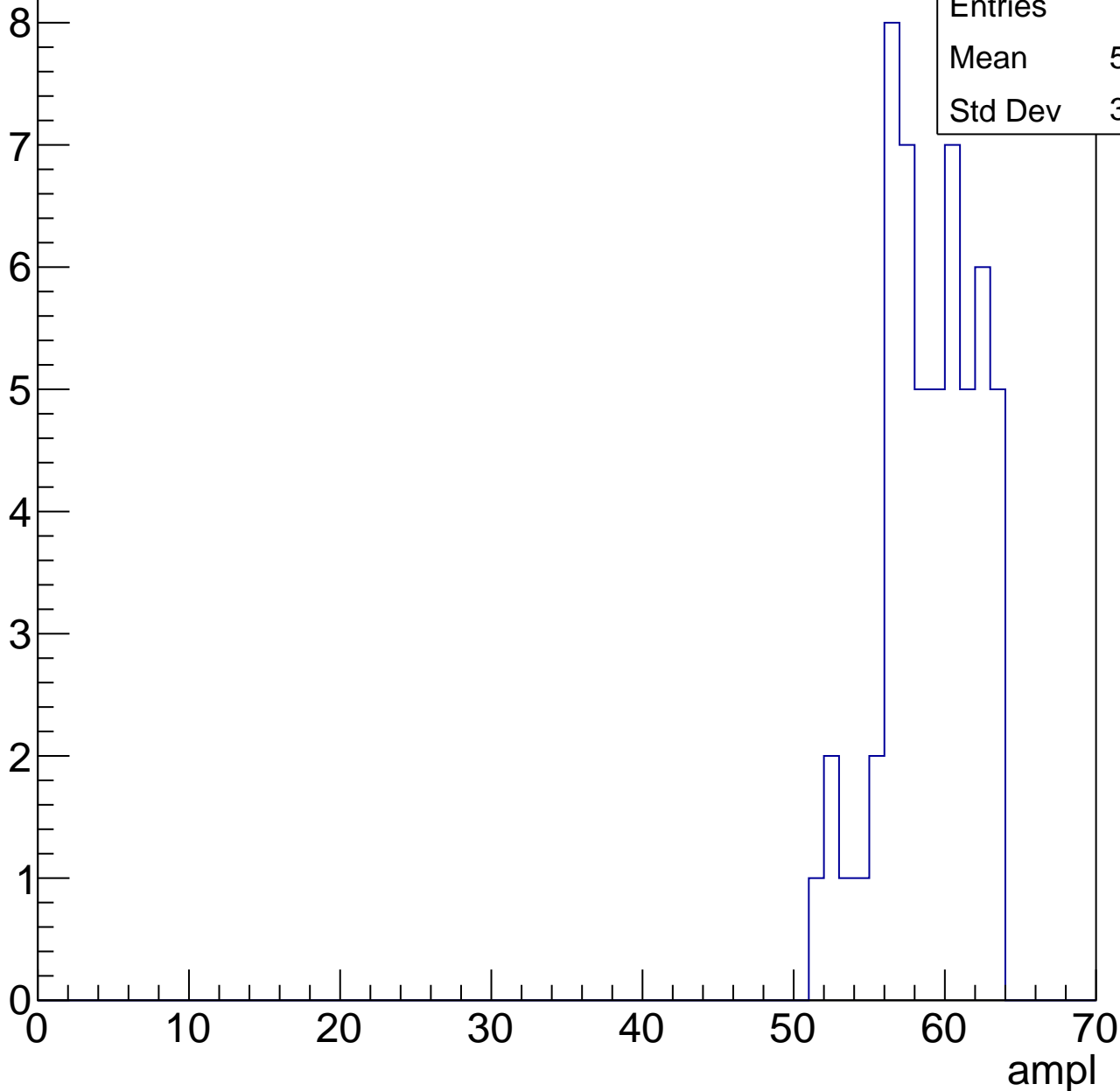


# B1L102S, U5-ch54, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	58.47
Std Dev	3.032

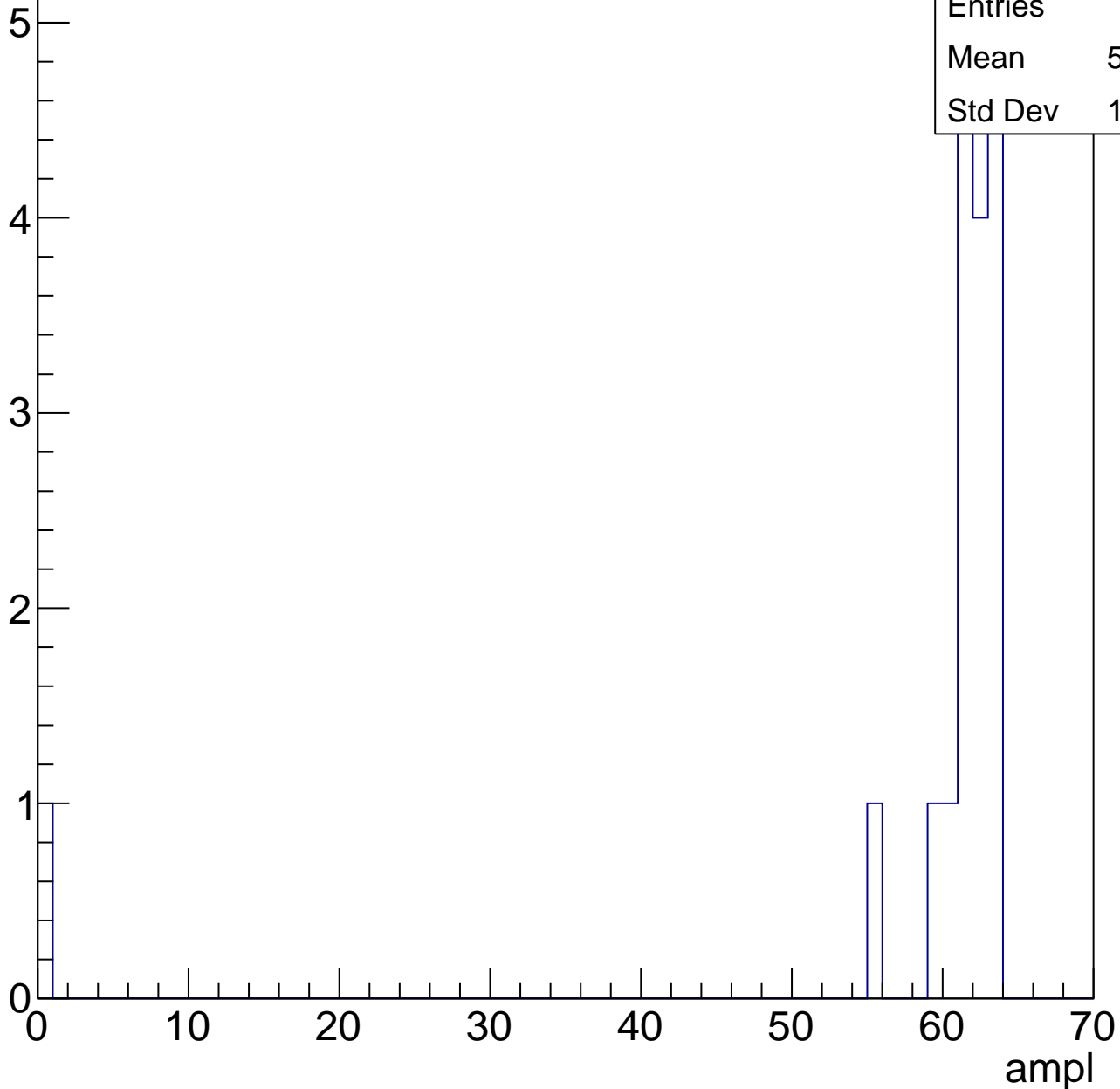


# B1L102S, U5-ch54, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	18
Mean	57.89
Std Dev	14.17





# B1L102S, U5-ch54, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U5-ch55, adc0

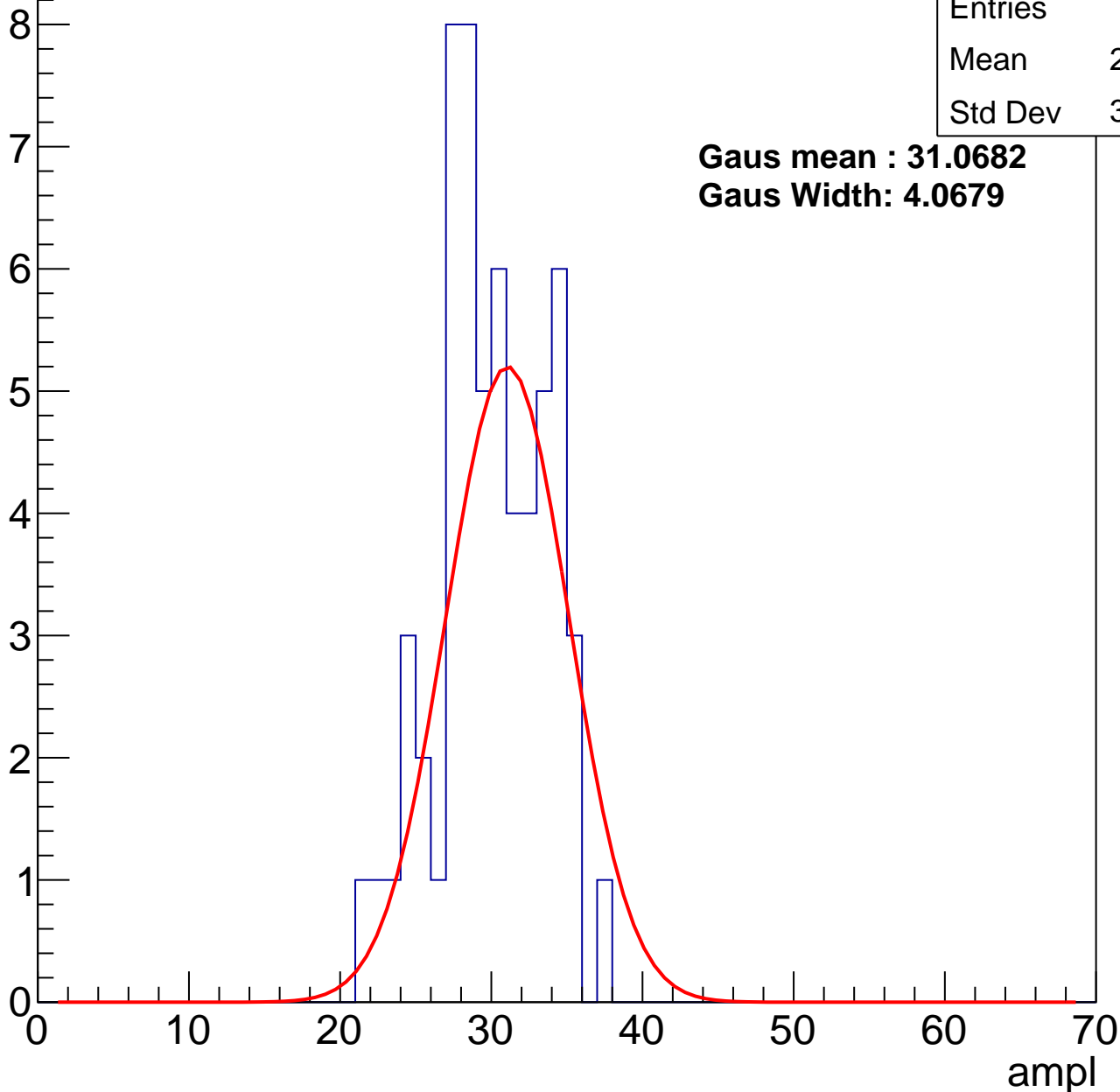
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	29.53
Std Dev	3.562

**Gaus mean : 31.0682**

**Gaus Width: 4.0679**



# B1L102S, U5-ch55, adc1

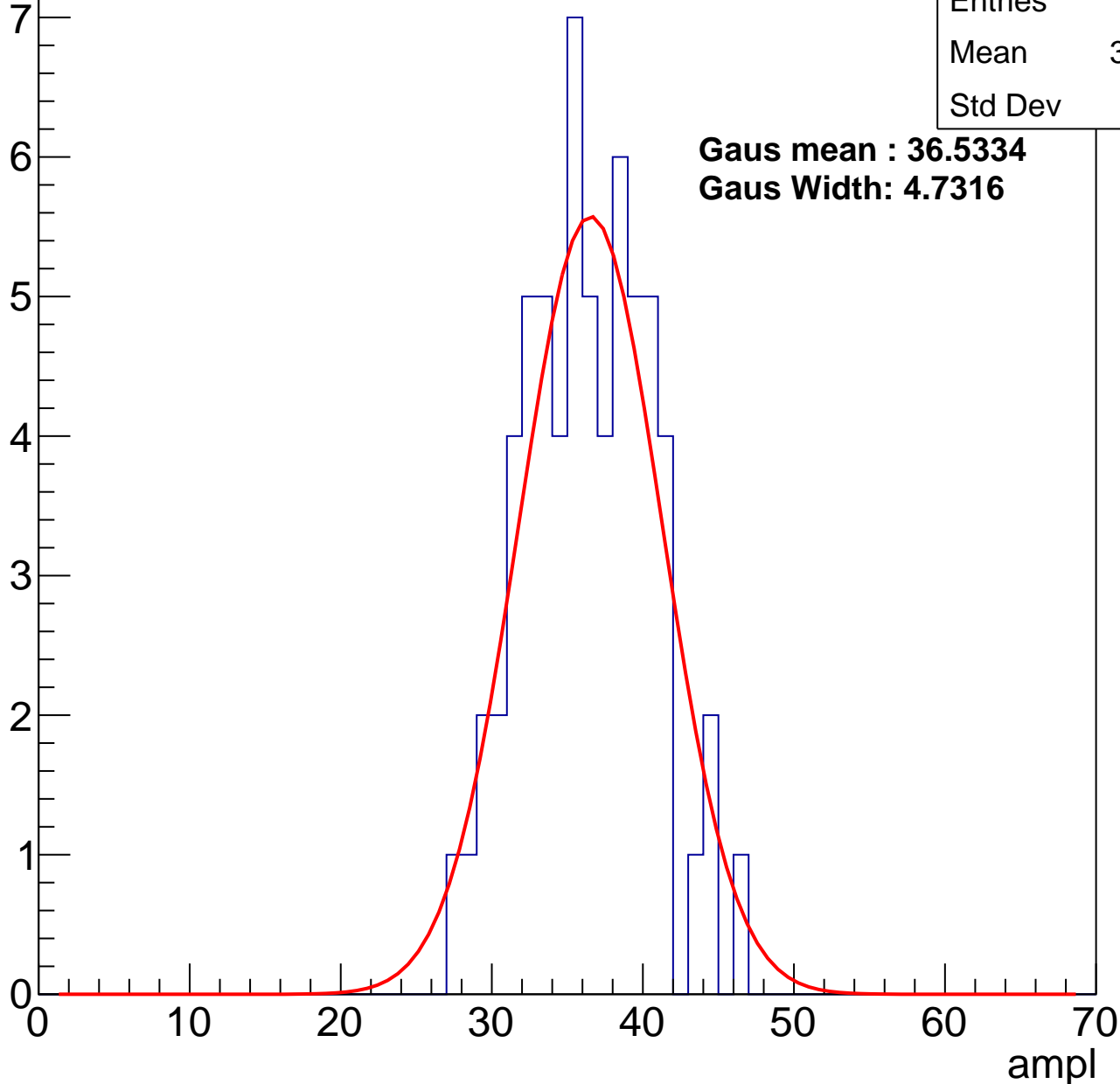
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	35.86
Std Dev	4.13

**Gaus mean : 36.5334**

**Gaus Width: 4.7316**



# B1L102S, U5-ch55, adc2

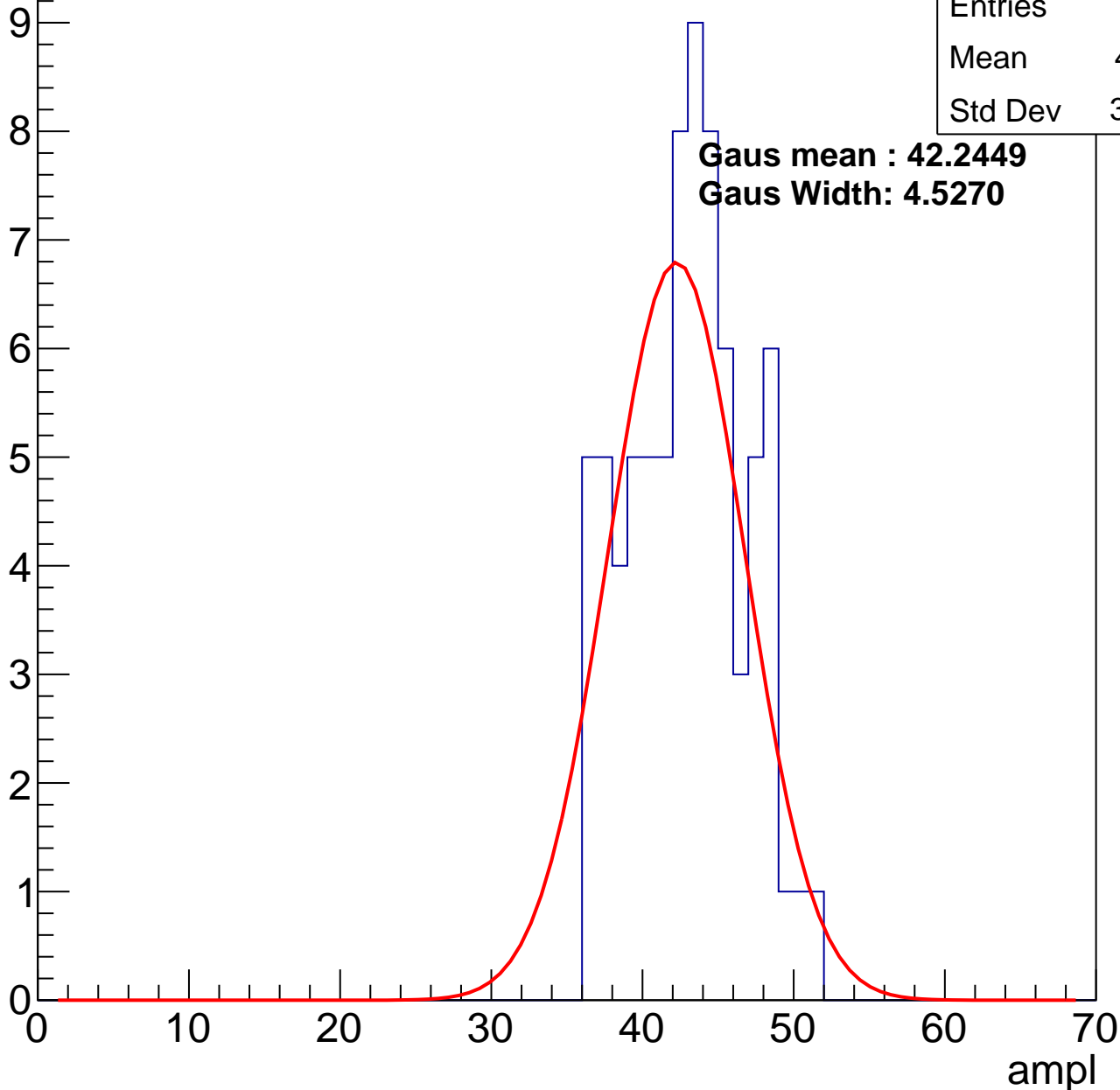
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	42.51
Std Dev	3.775

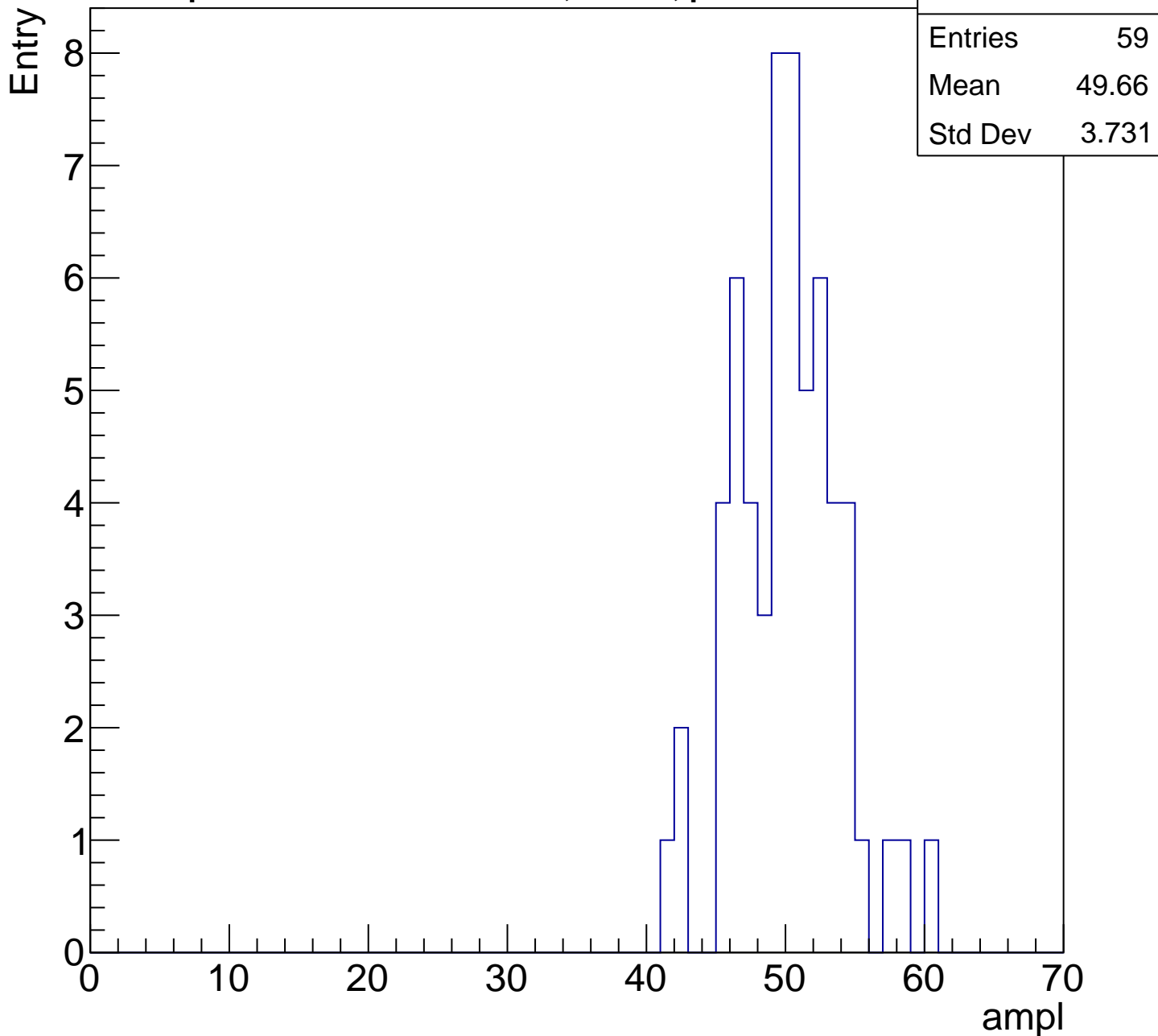
**Gaus mean : 42.2449**

**Gaus Width: 4.5270**



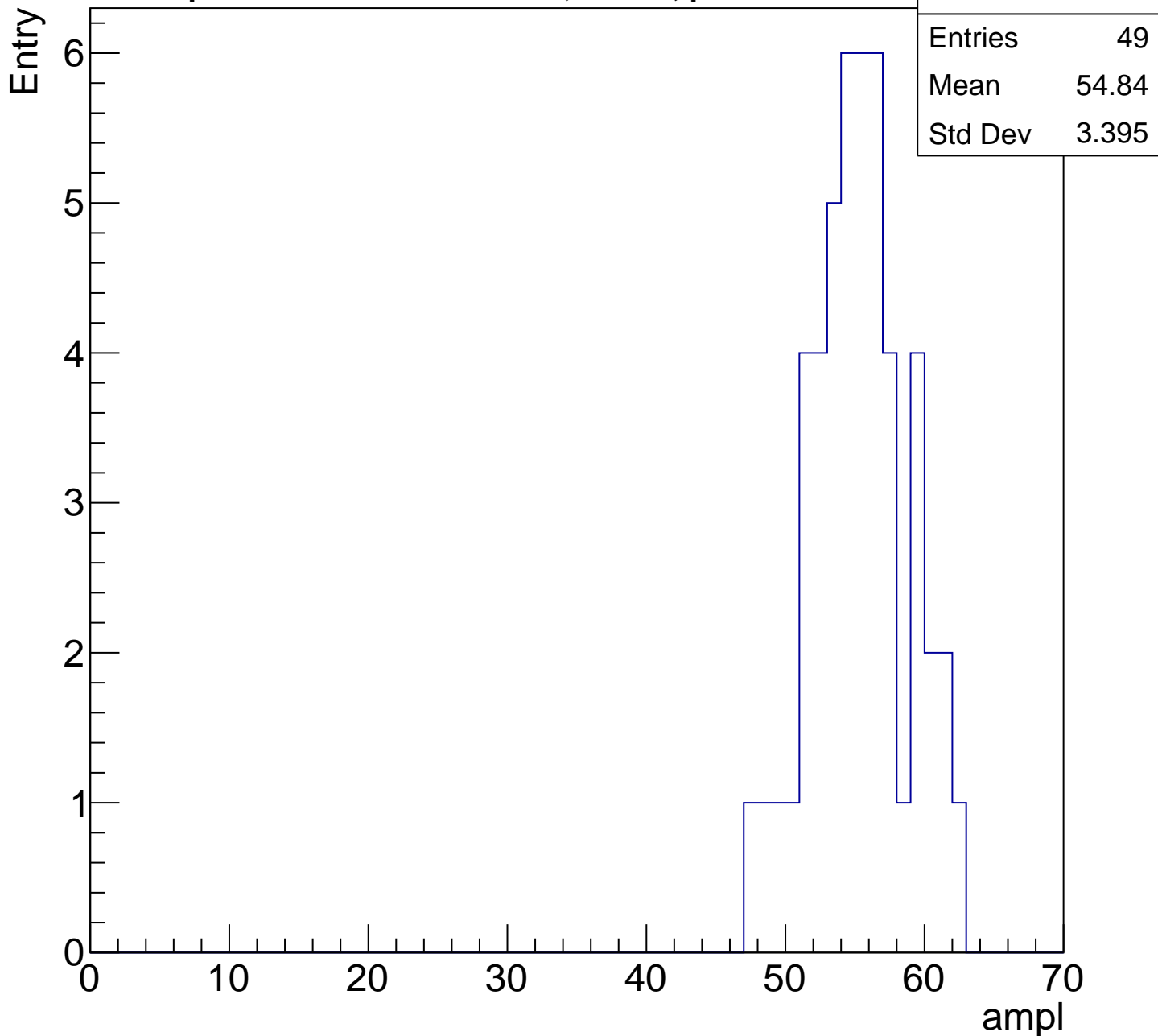
# B1L102S, U5-ch55, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2



# B1L102S, U5-ch55, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

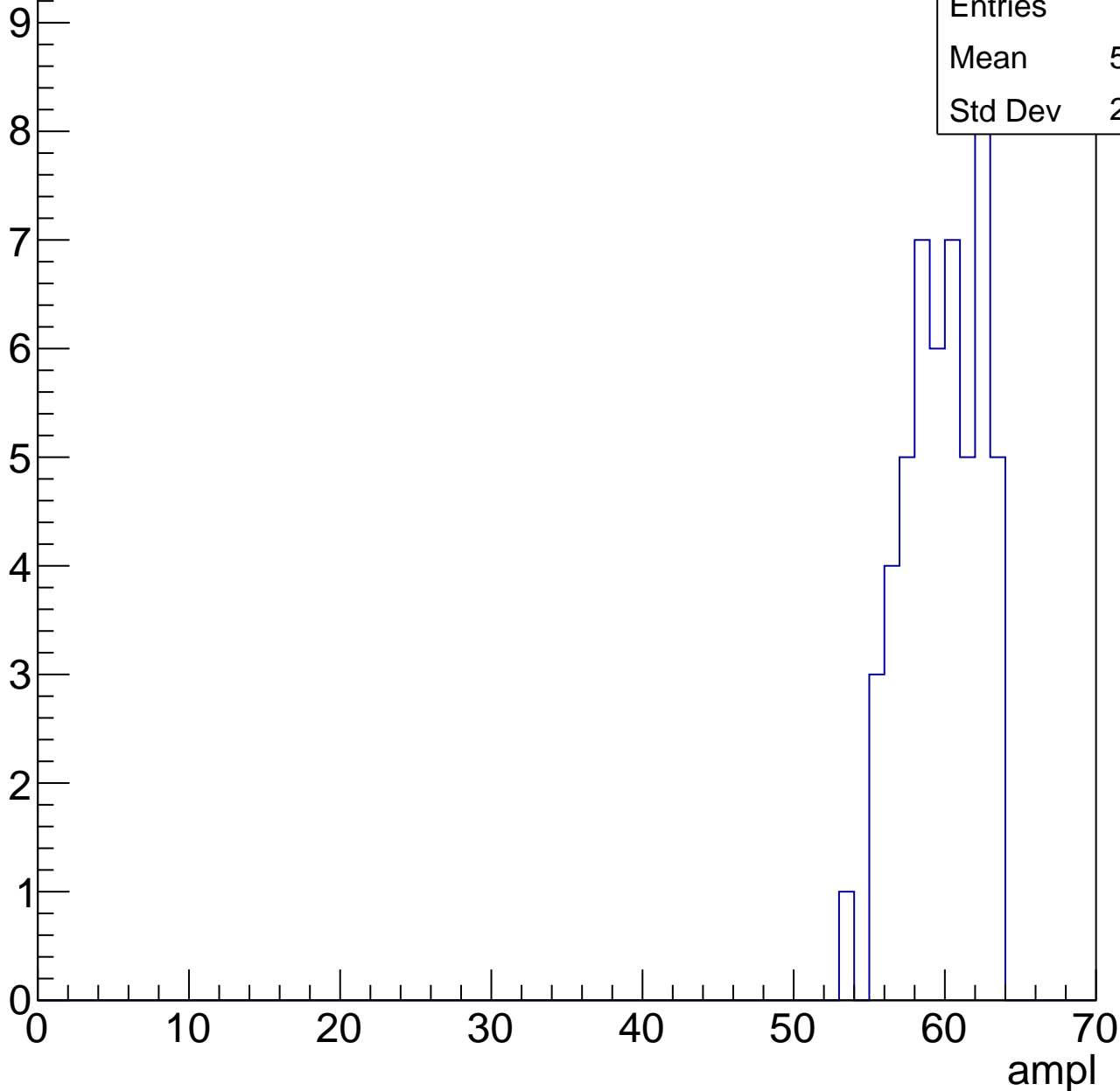


# B1L102S, U5-ch55, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	59.33
Std Dev	2.517

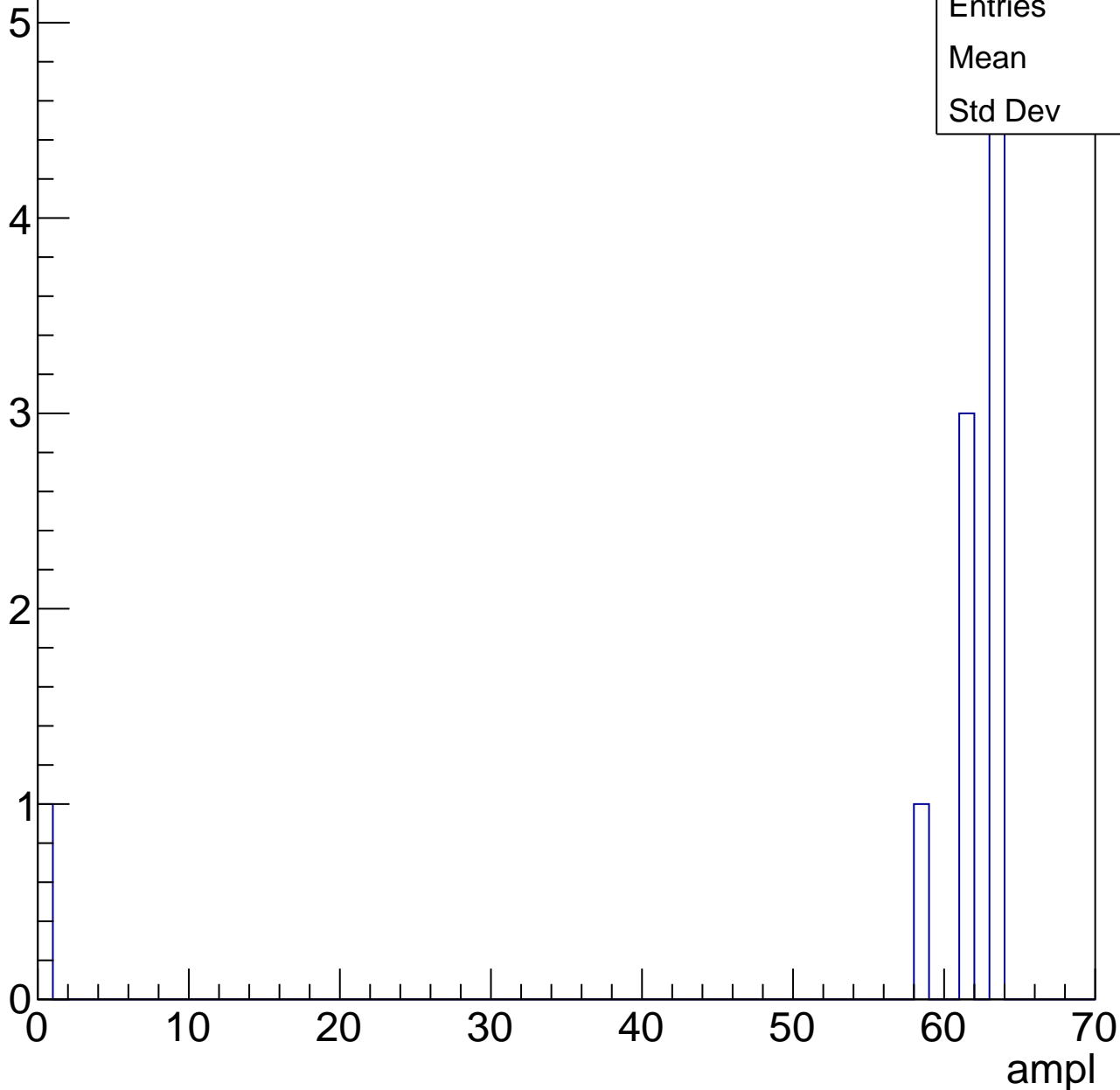


# B1L102S, U5-ch55, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	10
Mean	55.6
Std Dev	18.6





# B1L102S, U5-ch55, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U5-ch56, adc0

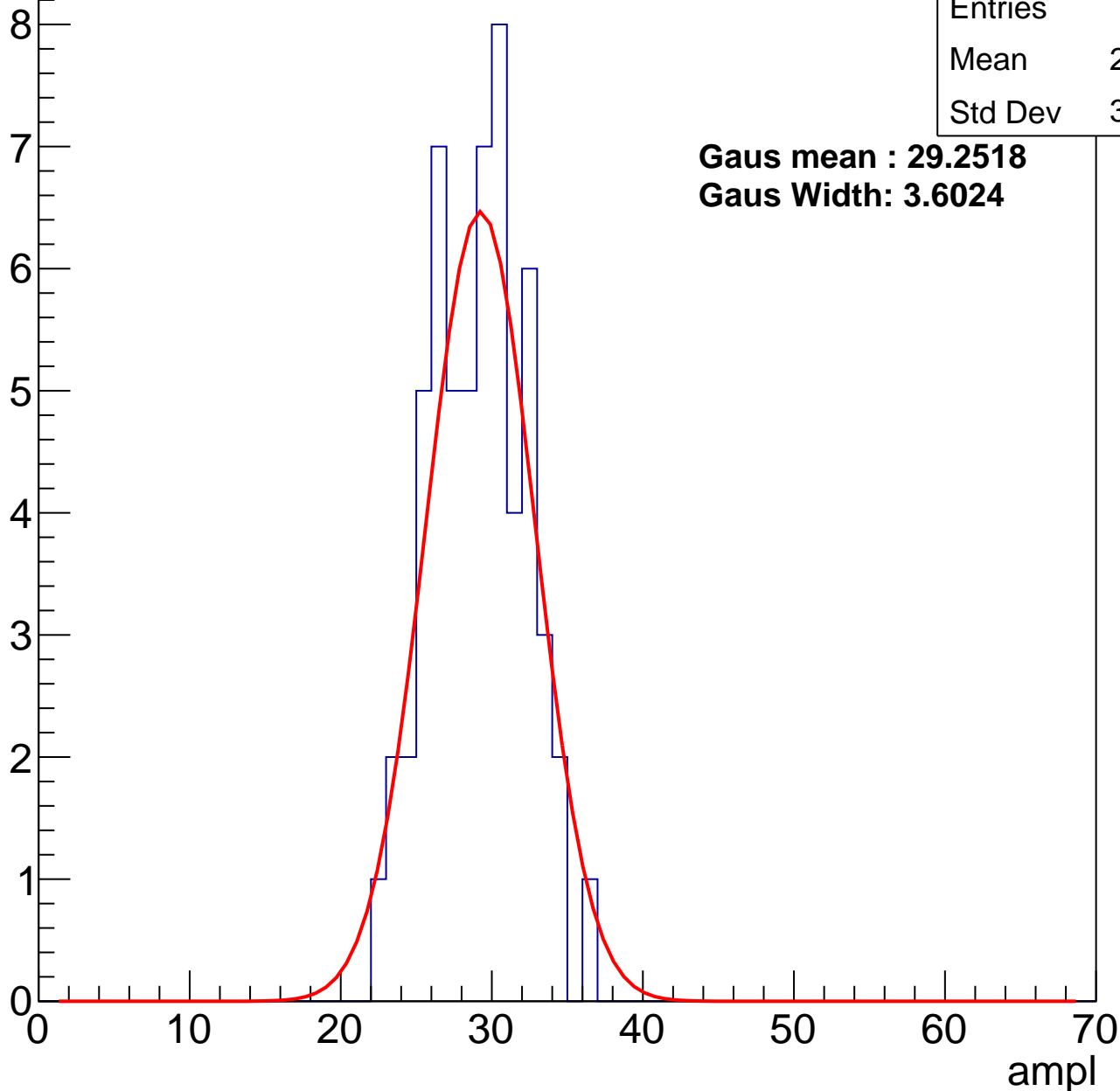
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	28.62
Std Dev	3.095

**Gaus mean : 29.2518**

**Gaus Width: 3.6024**



# B1L102S, U5-ch56, adc1

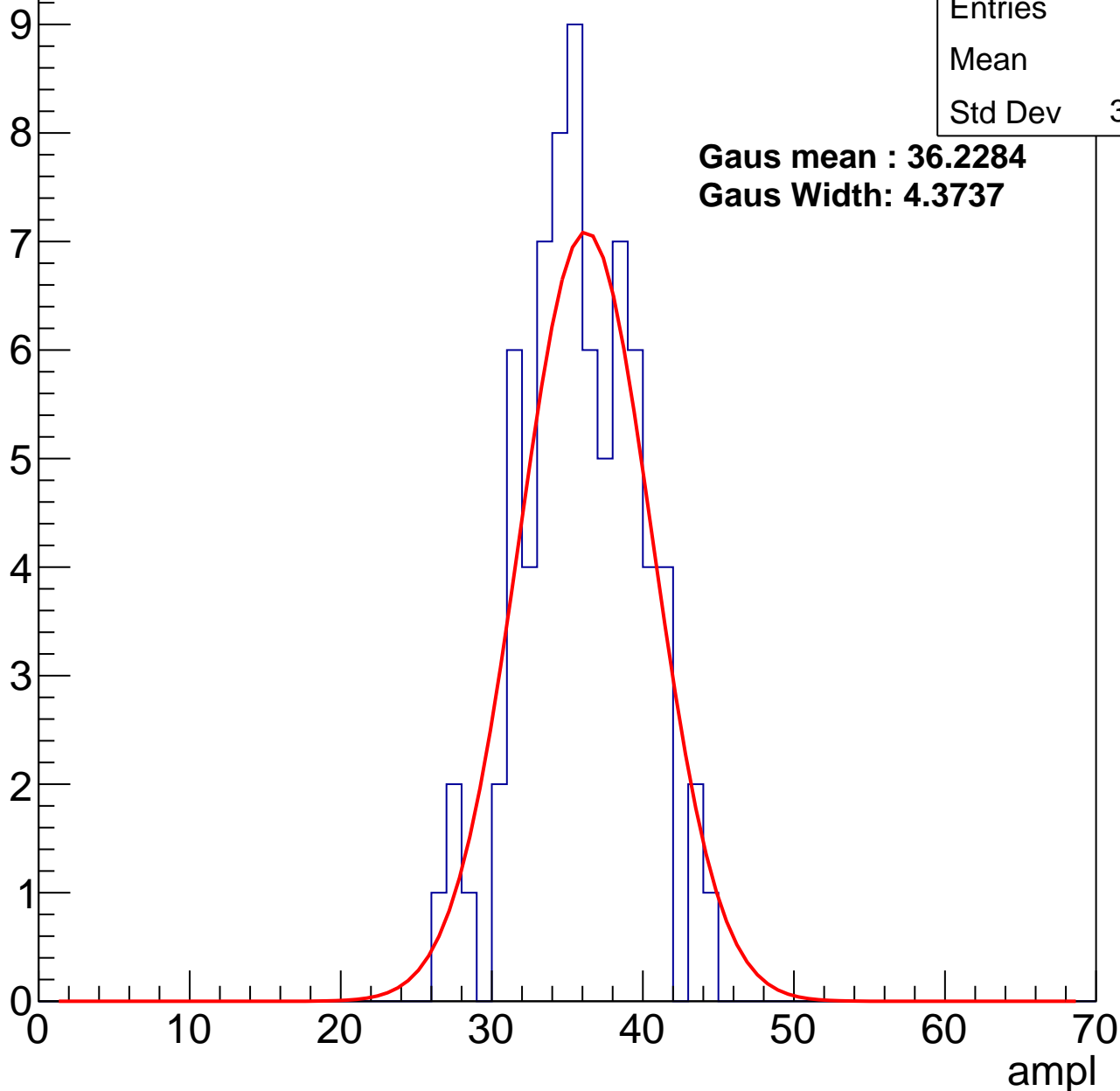
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	35.4
Std Dev	3.833

**Gaus mean : 36.2284**

**Gaus Width: 4.3737**



# B1L102S, U5-ch56, adc2

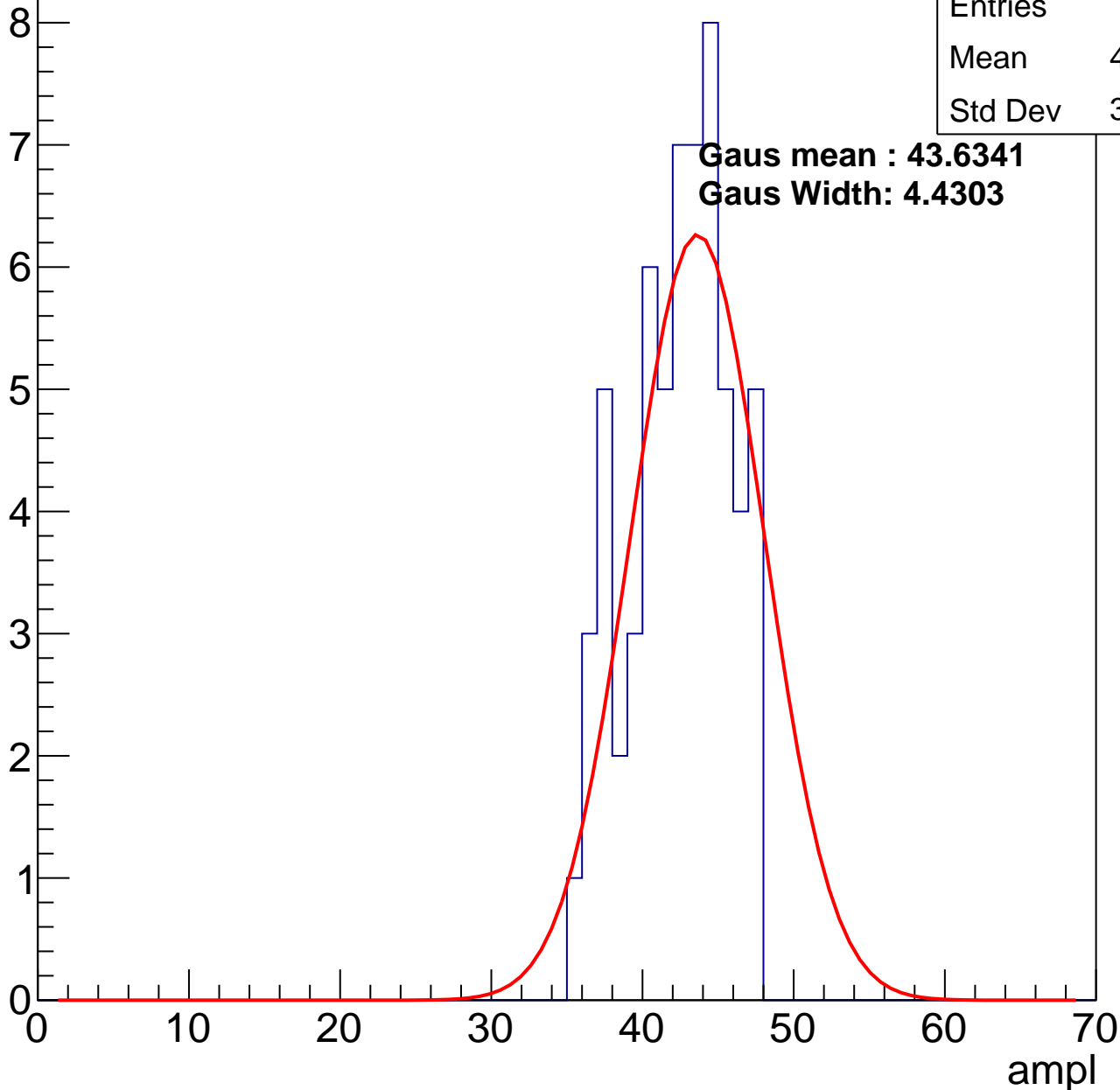
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	41.92
Std Dev	3.246

**Gaus mean : 43.6341**

**Gaus Width: 4.4303**

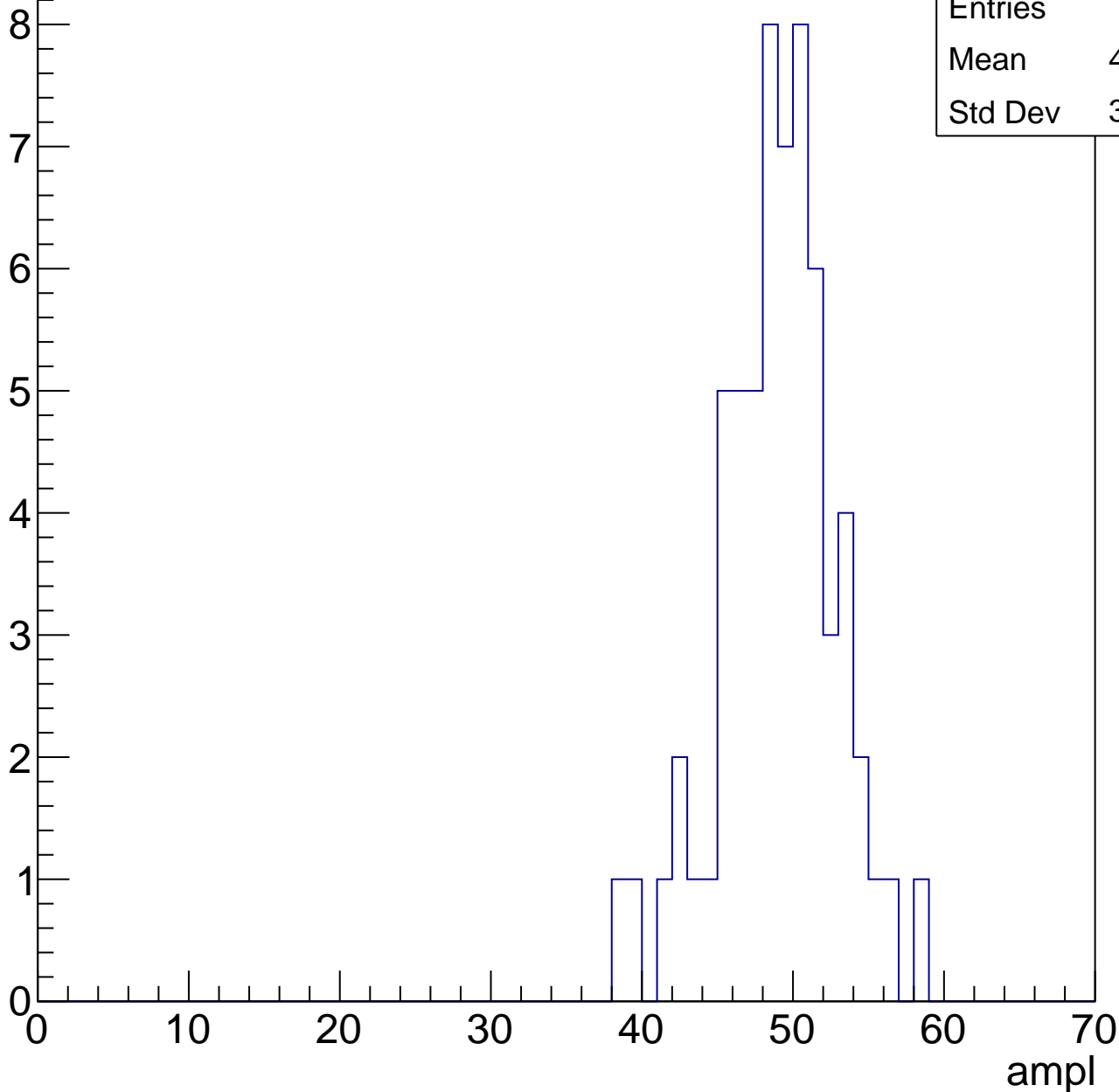


# B1L102S, U5-ch56, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	48.52
Std Dev	3.825

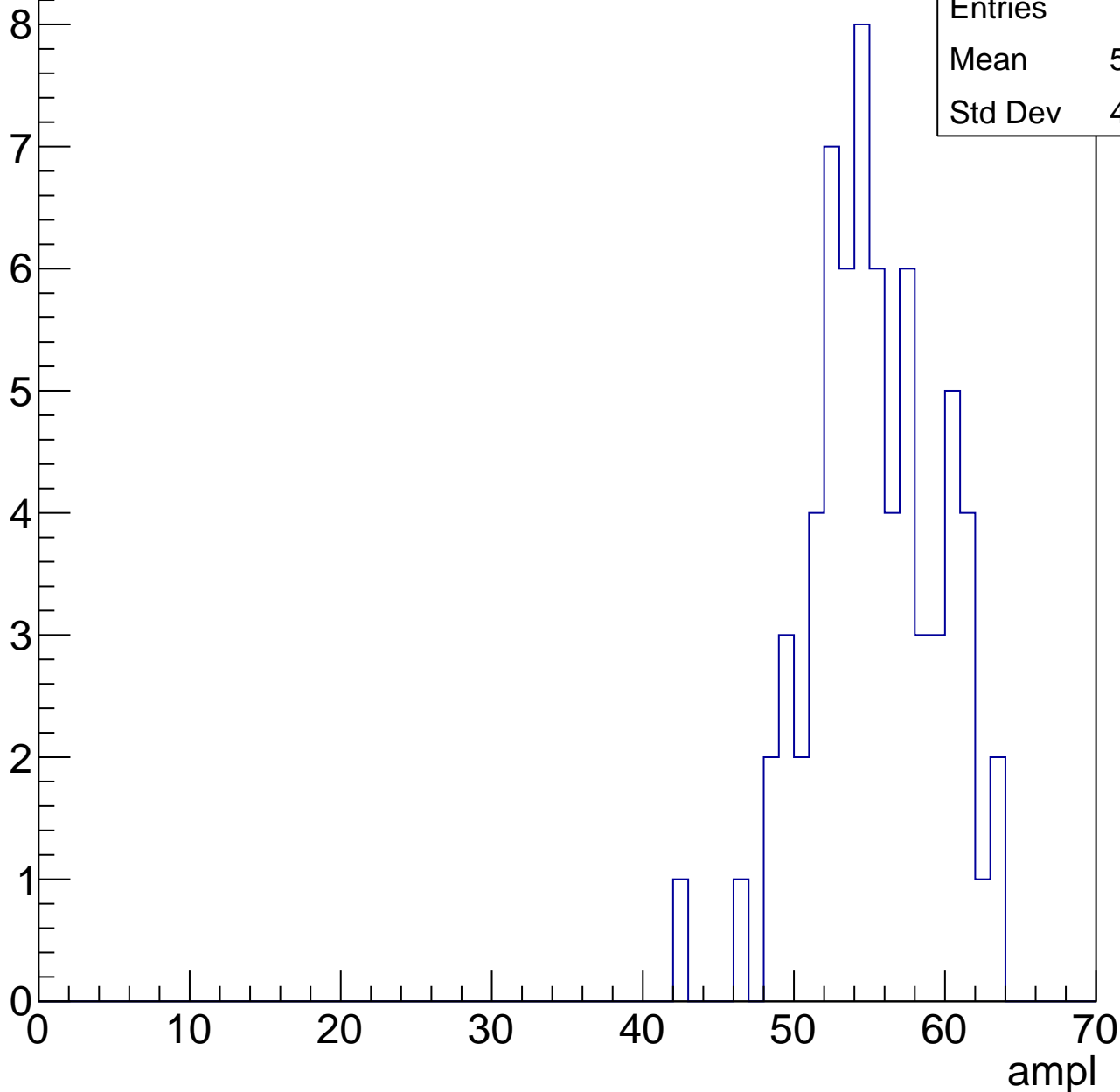


# B1L102S, U5-ch56, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	54.82
Std Dev	4.222



# B1L102S, U5-ch56, adc5

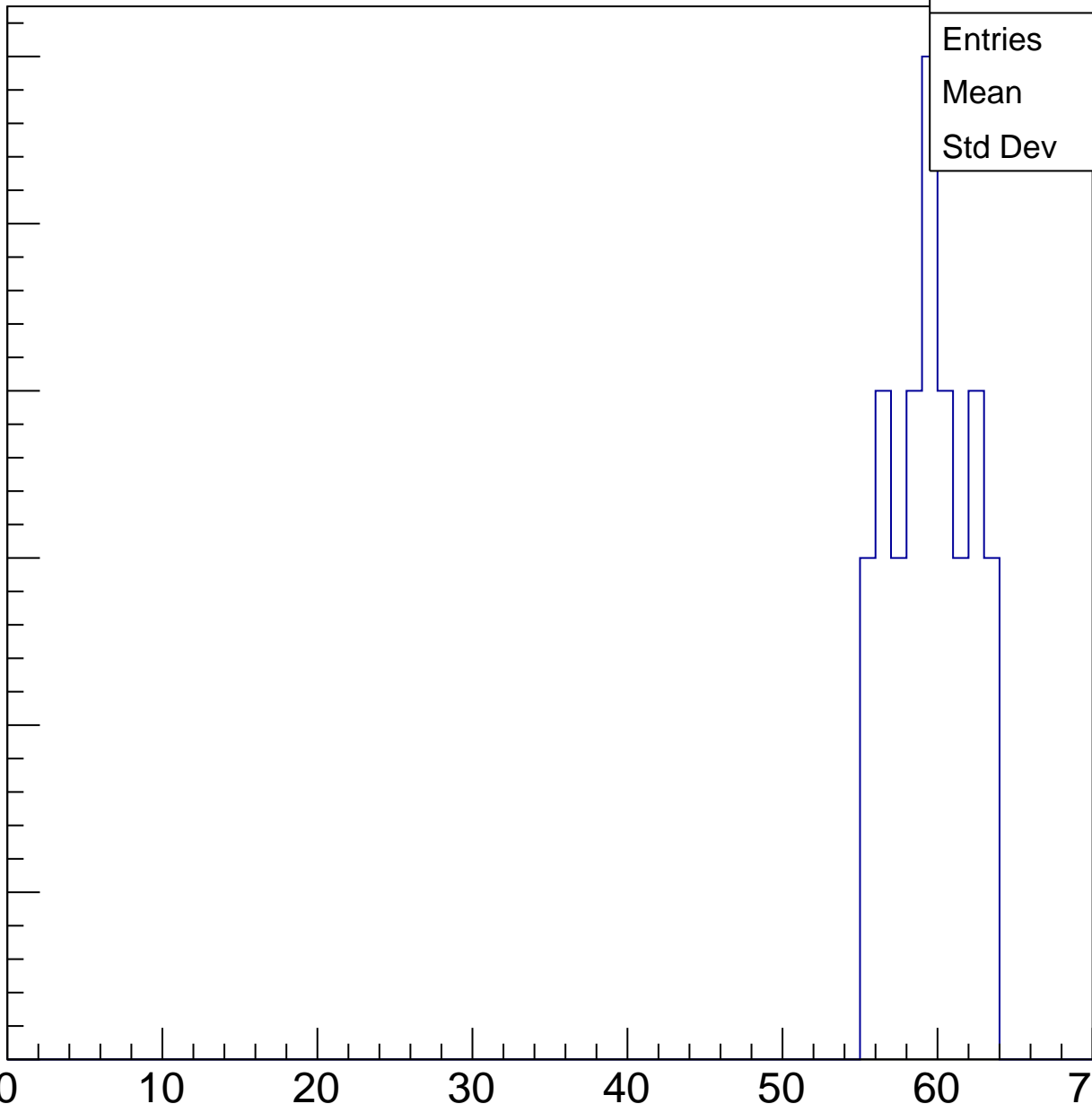
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

6  
5  
4  
3  
2  
1  
0

Entries	34
Mean	59
Std Dev	2.425

ampl

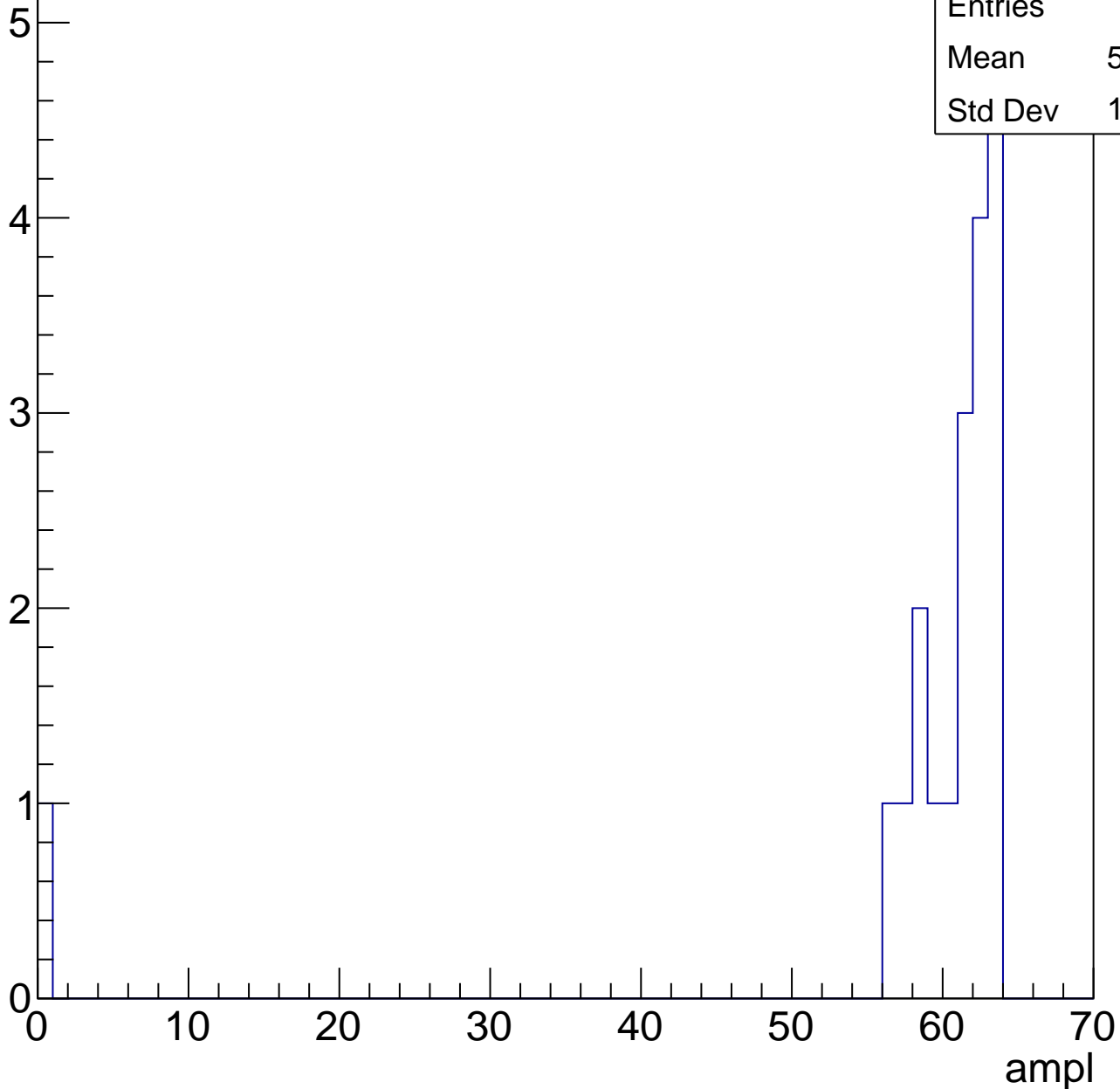


# B1L102S, U5-ch56, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	19
Mean	57.58
Std Dev	13.74

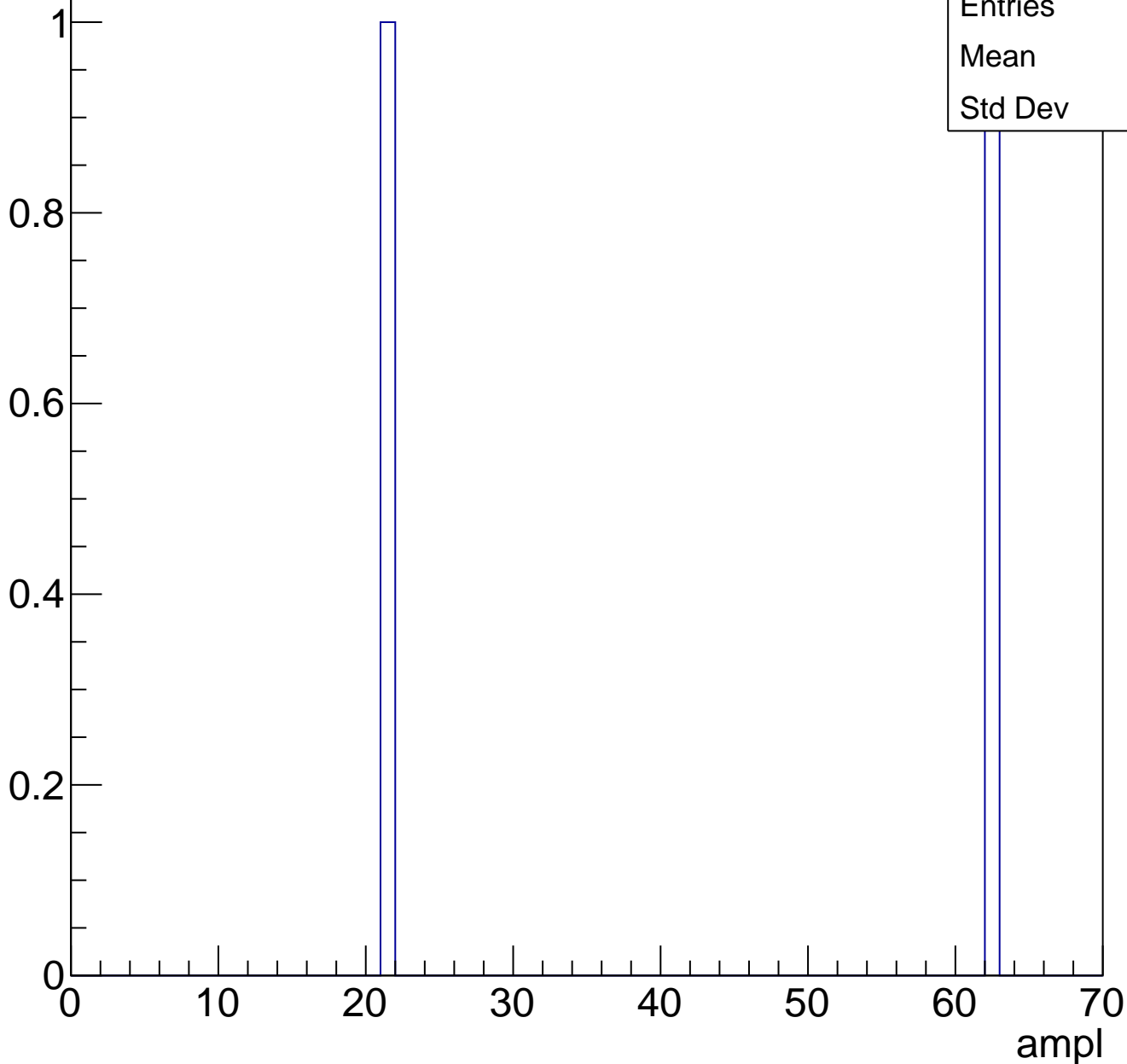




# B1L102S, U5-ch56, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U5-ch57, adc0

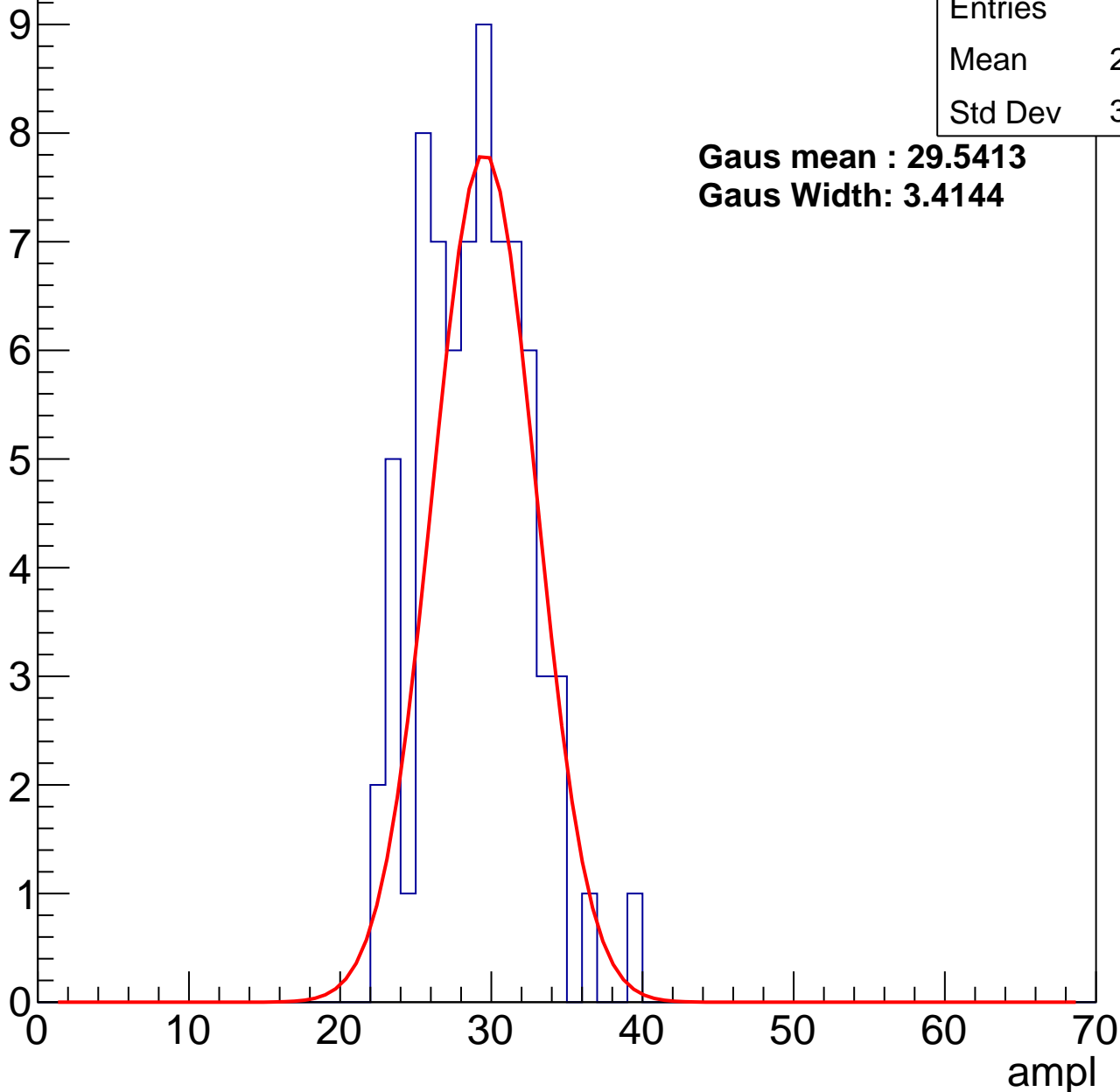
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	28.48
Std Dev	3.445

**Gaus mean : 29.5413**

**Gaus Width: 3.4144**



# B1L102S, U5-ch57, adc1

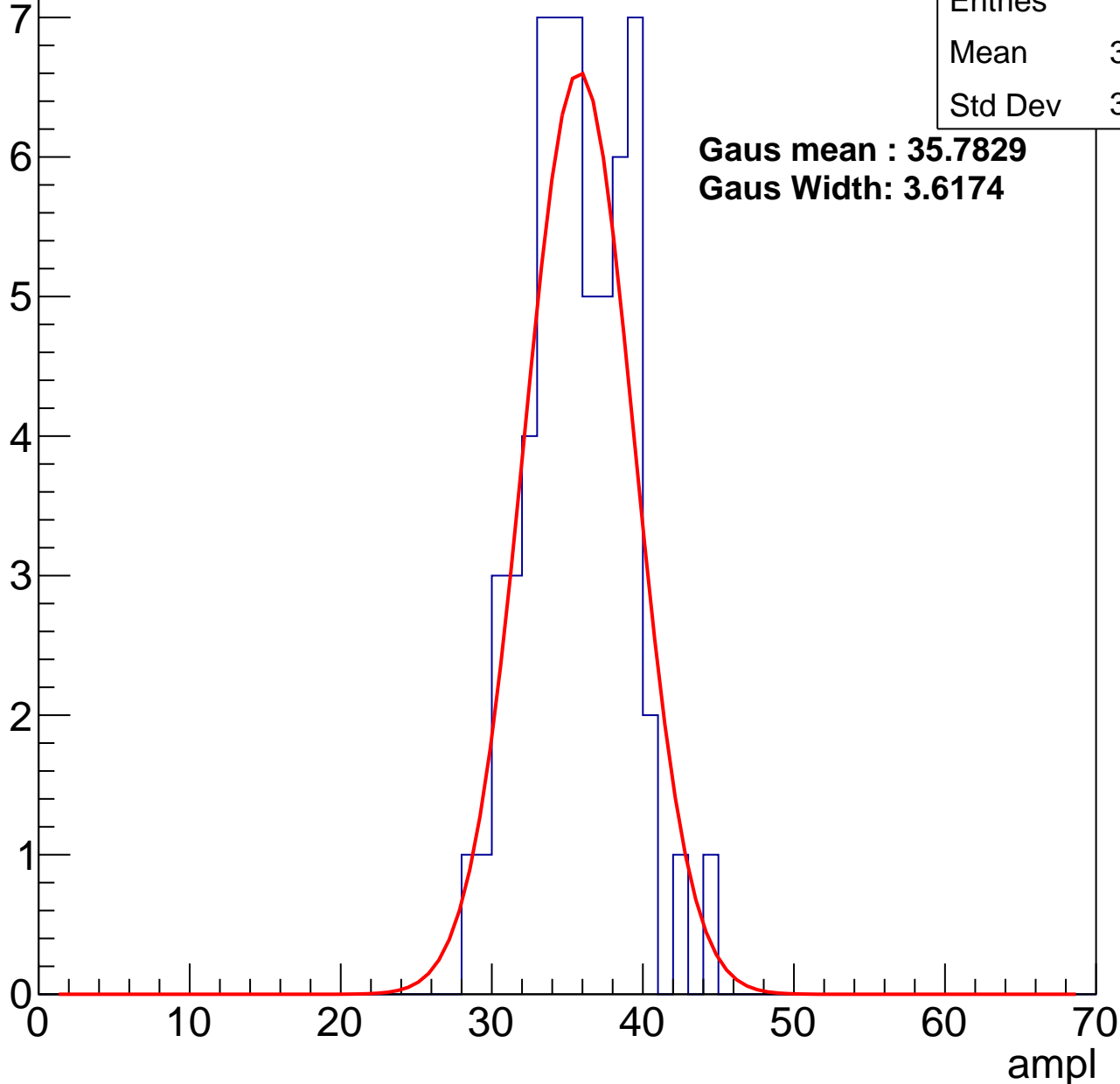
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	35.23
Std Dev	3.283

**Gaus mean : 35.7829**

**Gaus Width: 3.6174**



# B1L102S, U5-ch57, adc2

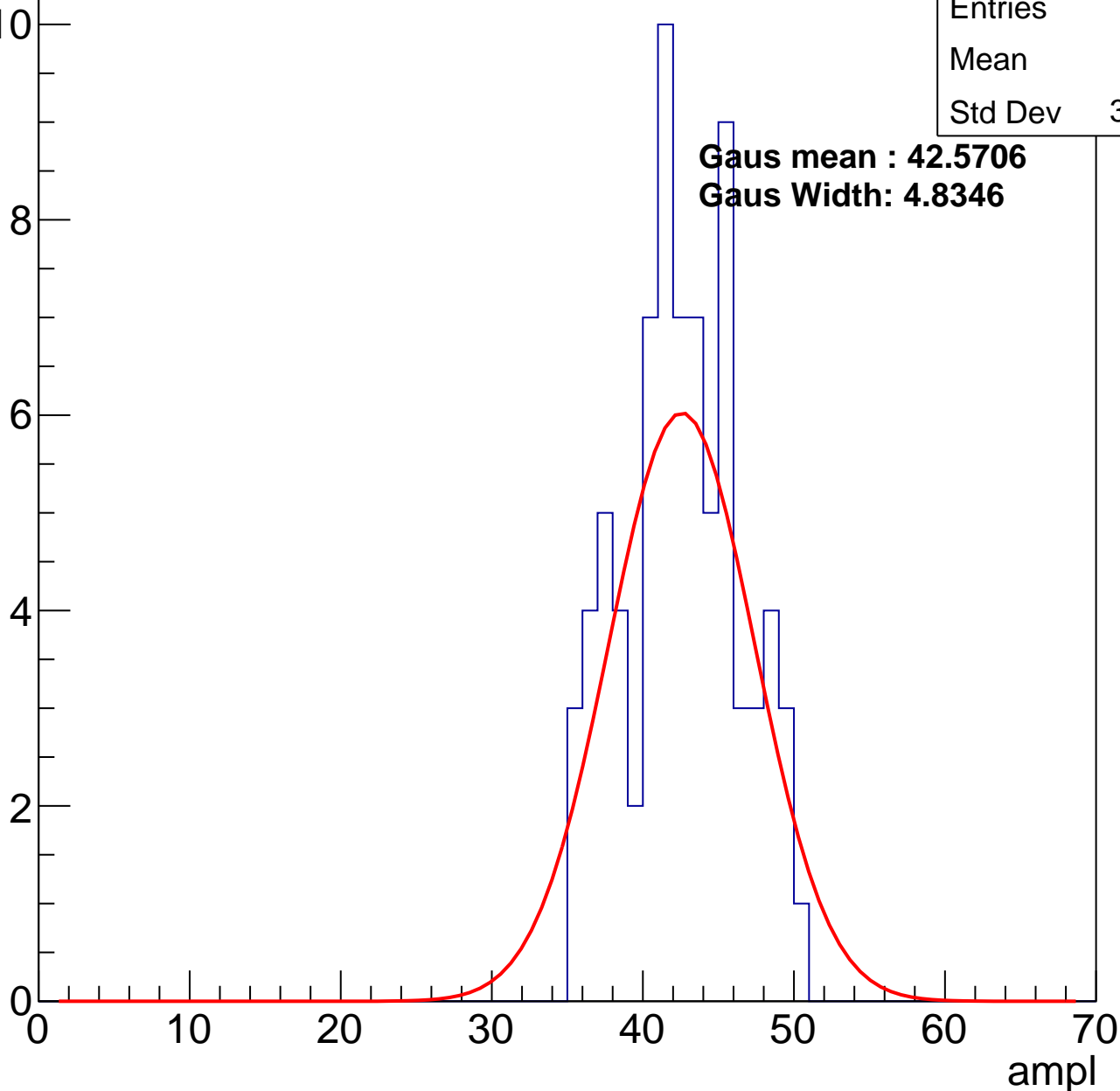
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	42.1
Std Dev	3.816

**Gaus mean : 42.5706**

**Gaus Width: 4.8346**

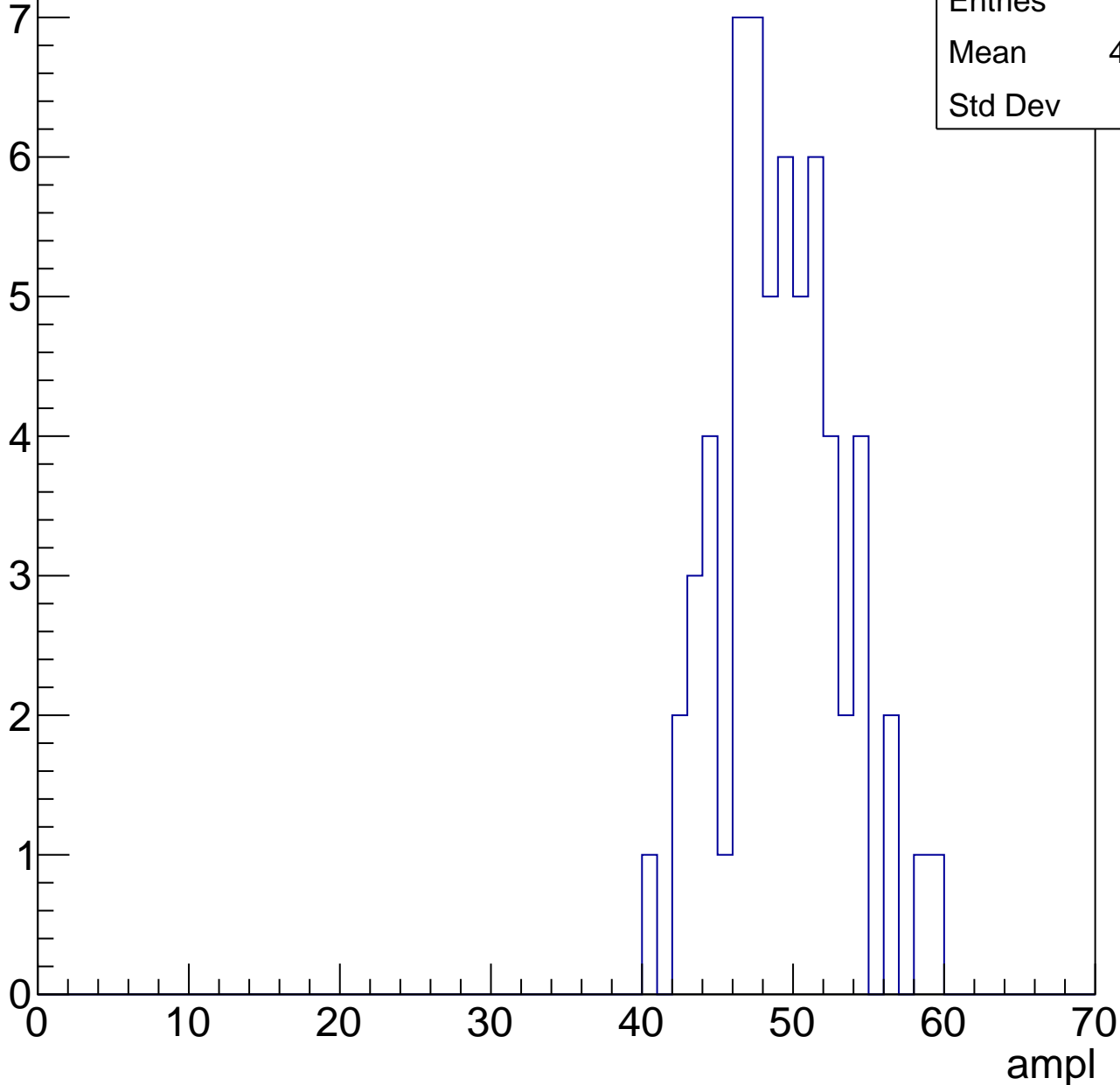


# B1L102S, U5-ch57, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	48.75
Std Dev	3.99

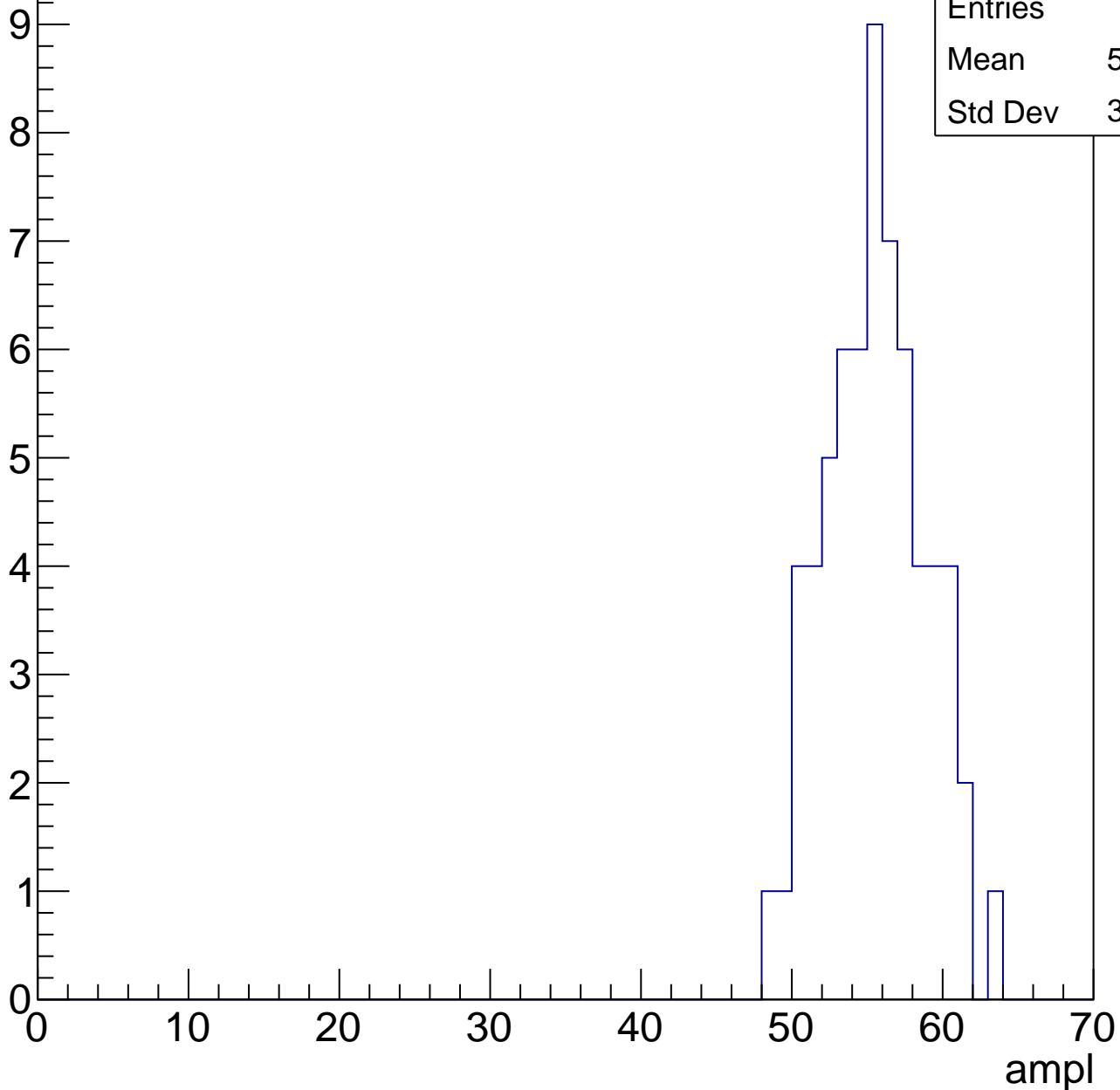


# B1L102S, U5-ch57, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	55.08
Std Dev	3.285

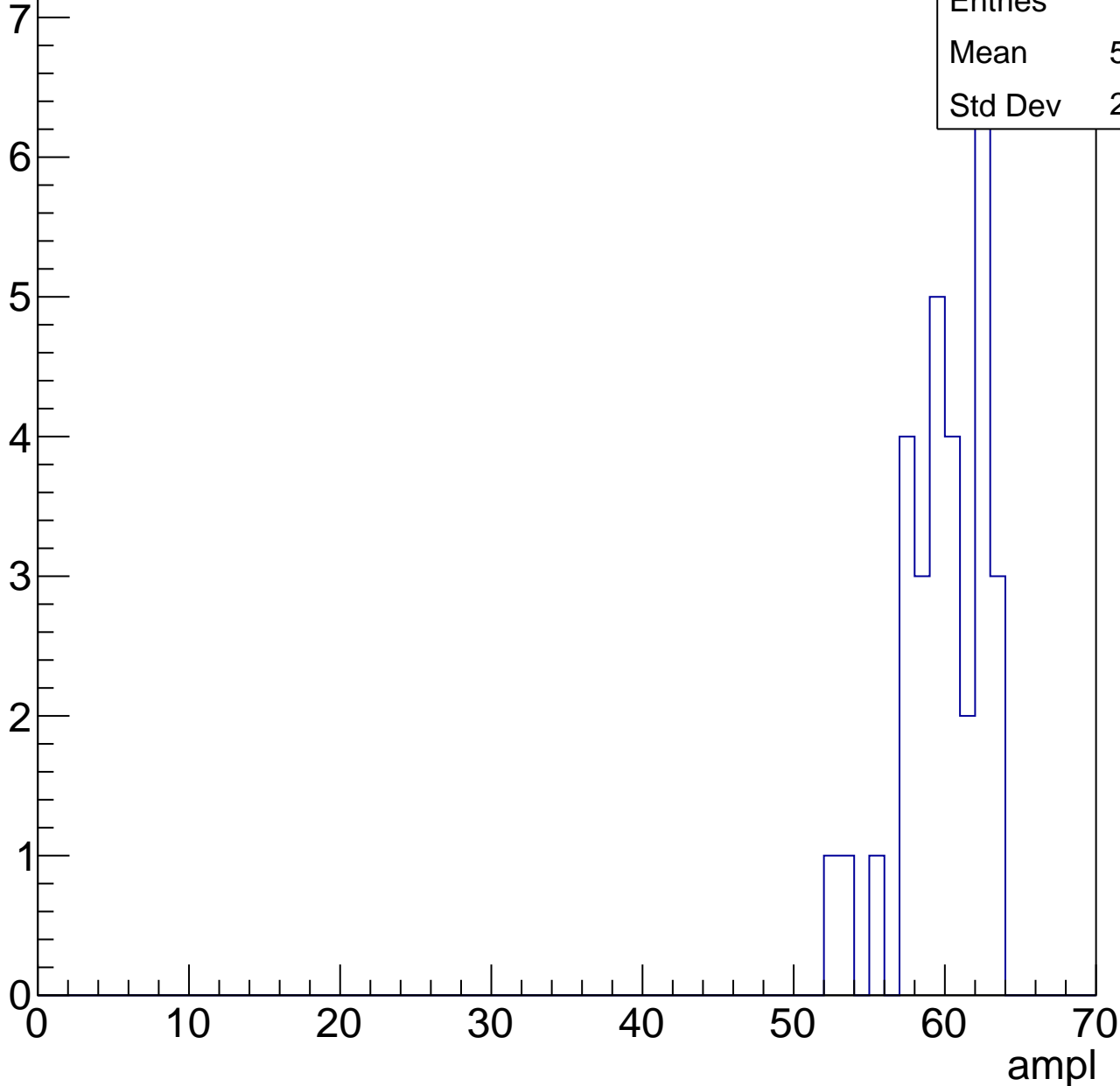


# B1L102S, U5-ch57, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	31
Mean	59.42
Std Dev	2.768

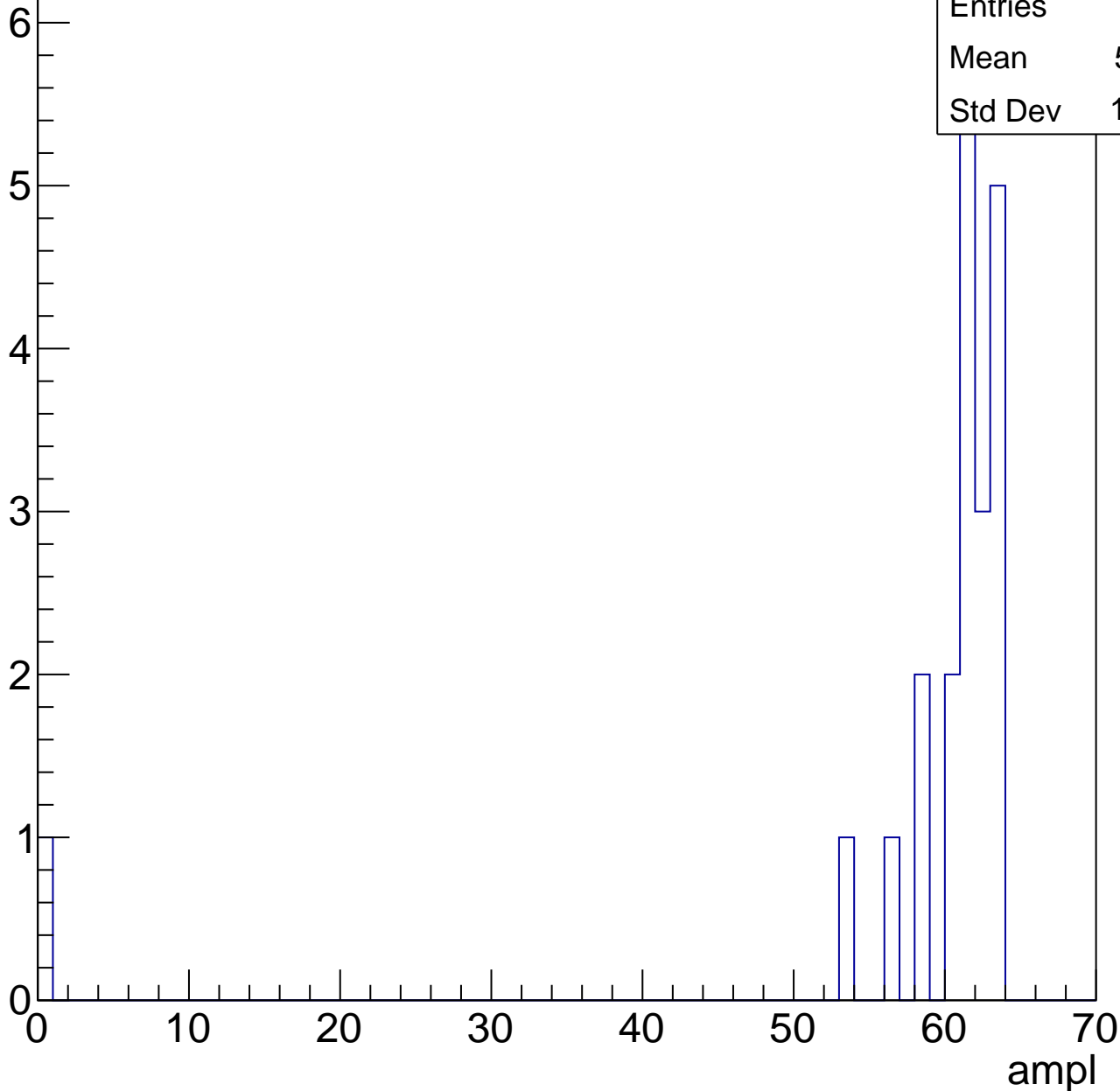


# B1L102S, U5-ch57, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	21
Mean	57.71
Std Dev	13.14

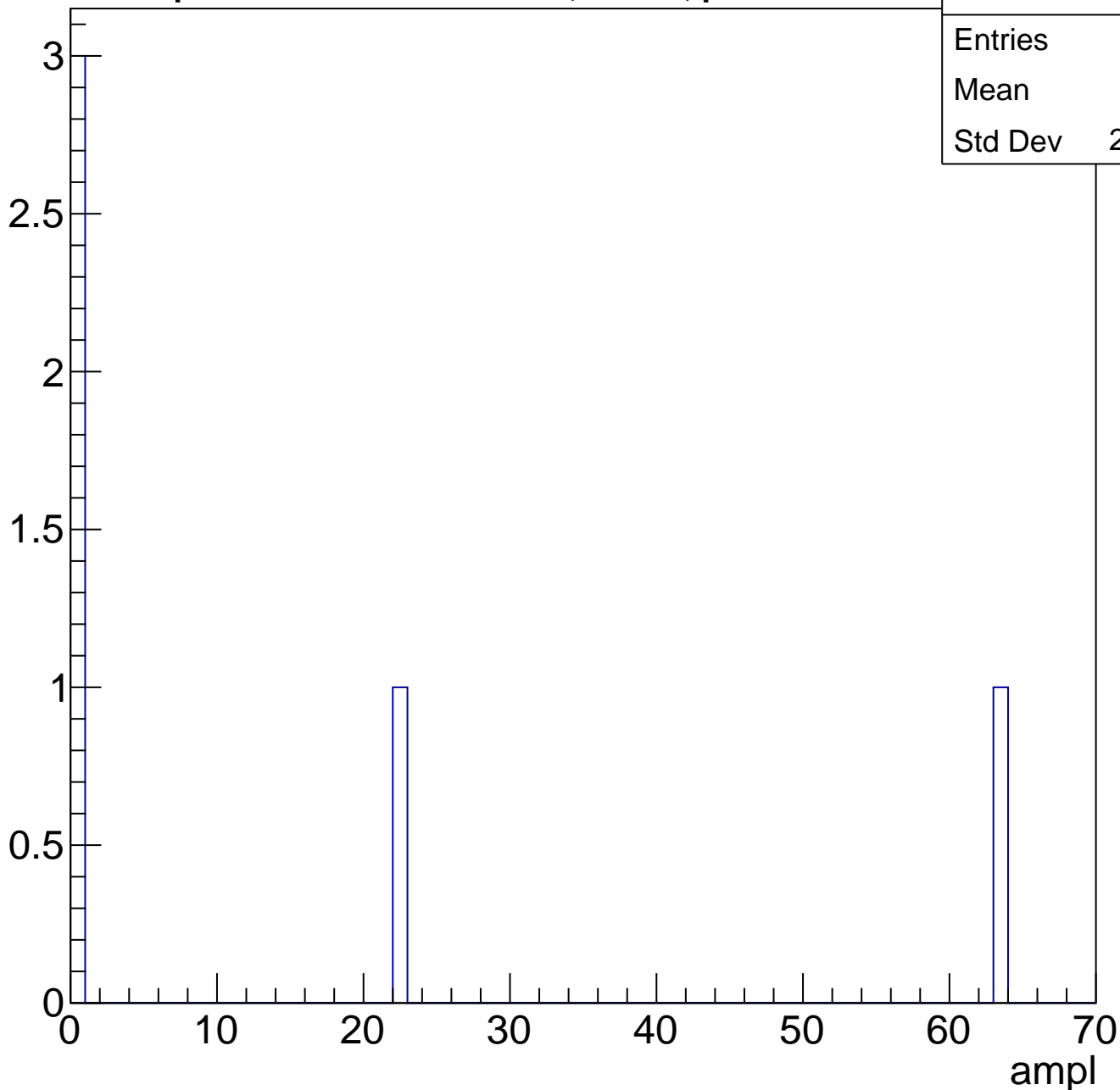




# B1L102S, U5-ch57, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	5
Mean	17
Std Dev	24.53

# B1L102S, U5-ch58, adc0

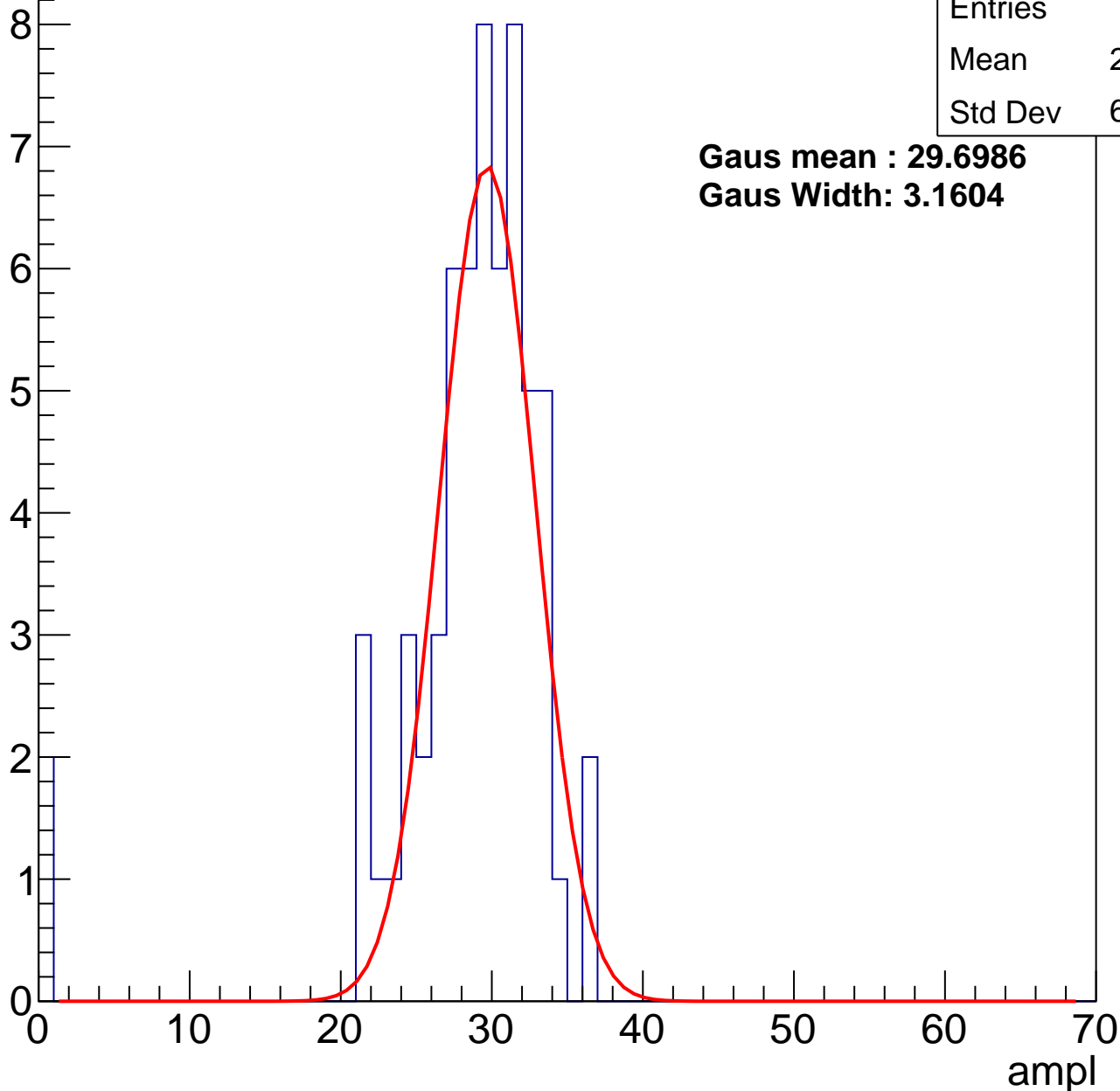
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	27.89
Std Dev	6.133

**Gaus mean : 29.6986**

**Gaus Width: 3.1604**



# B1L102S, U5-ch58, adc1

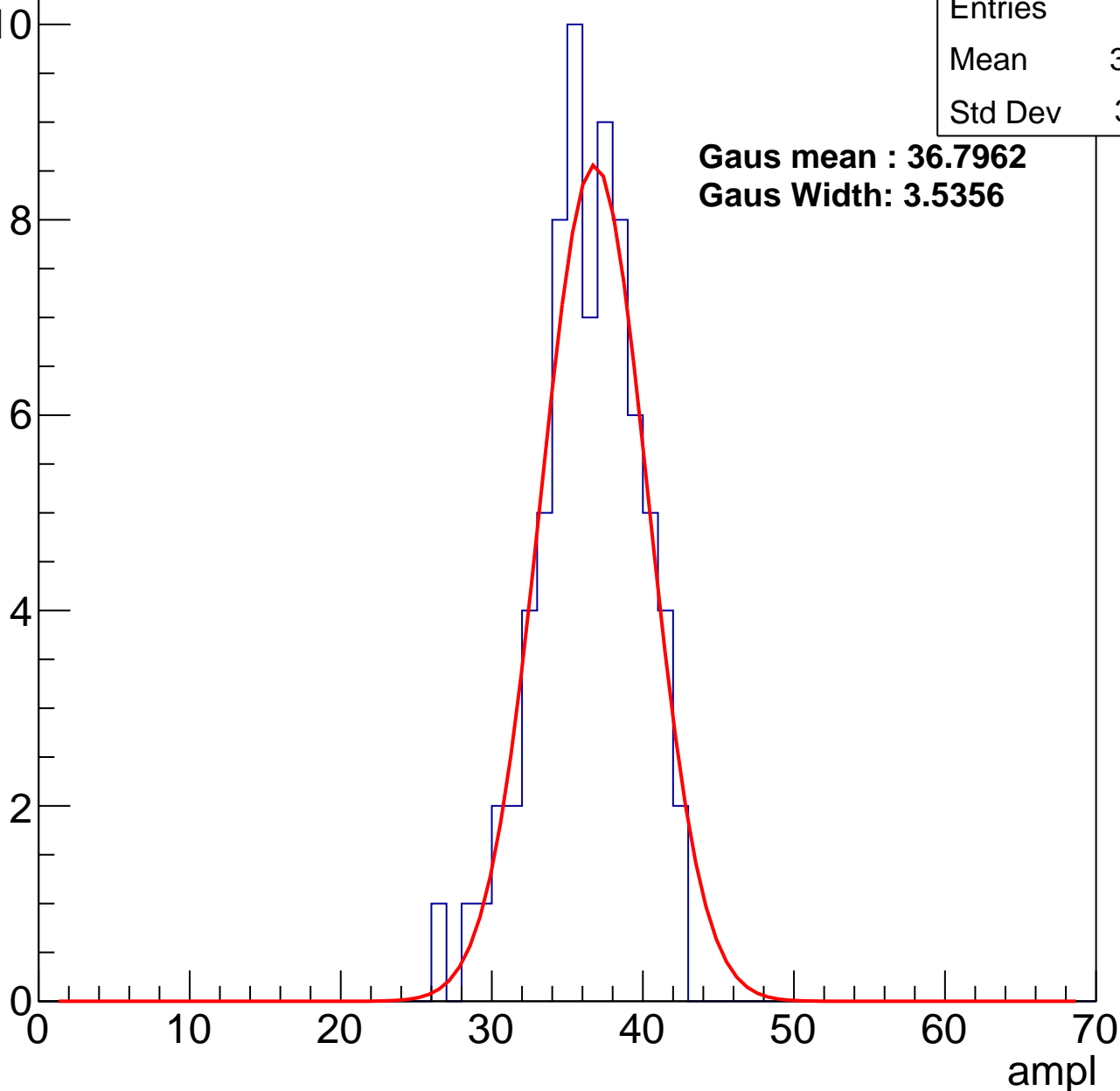
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	35.88
Std Dev	3.331

**Gaus mean : 36.7962**

**Gaus Width: 3.5356**



# B1L102S, U5-ch58, adc2

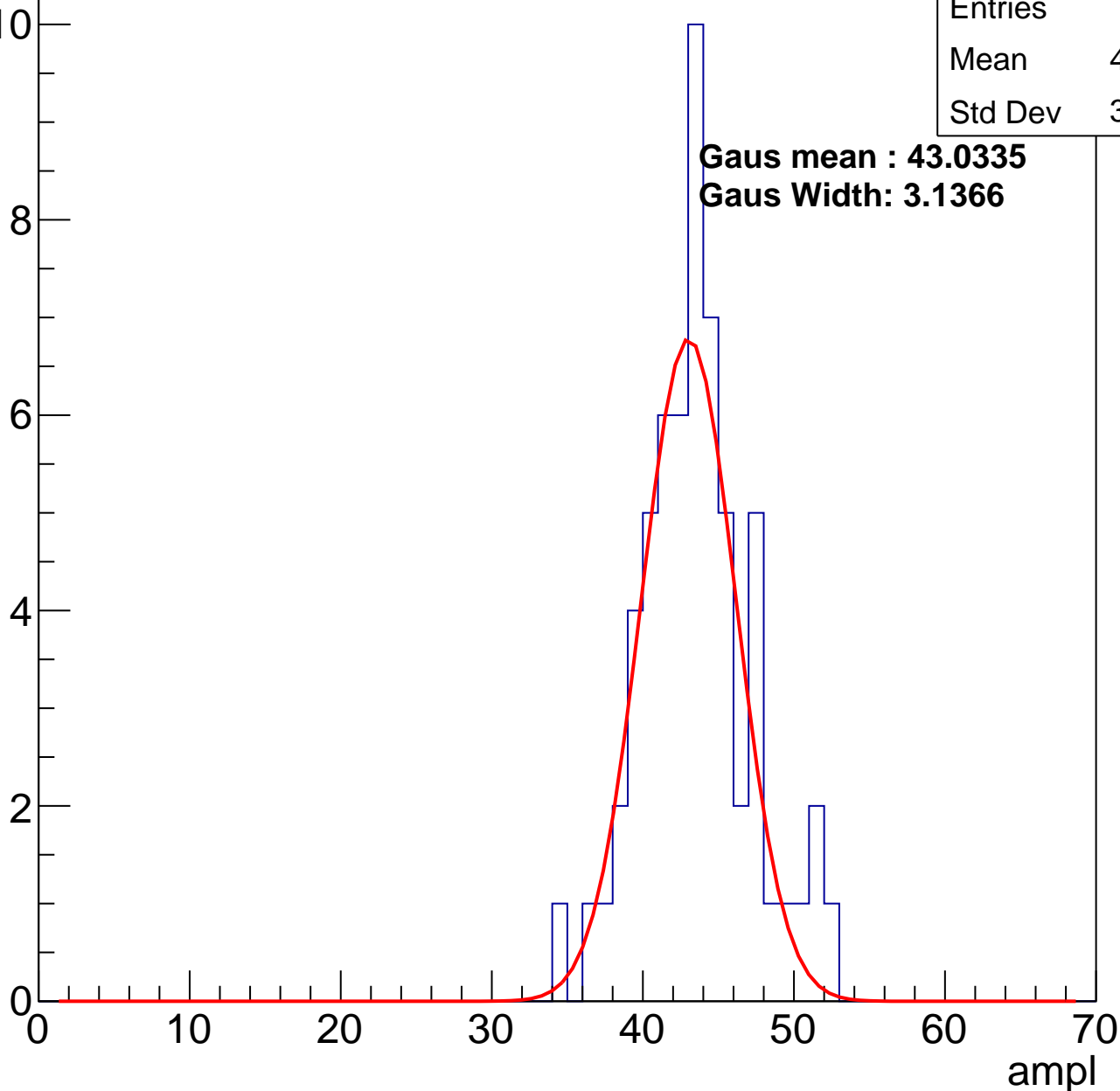
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	43.08
Std Dev	3.618

**Gaus mean : 43.0335**

**Gaus Width: 3.1366**

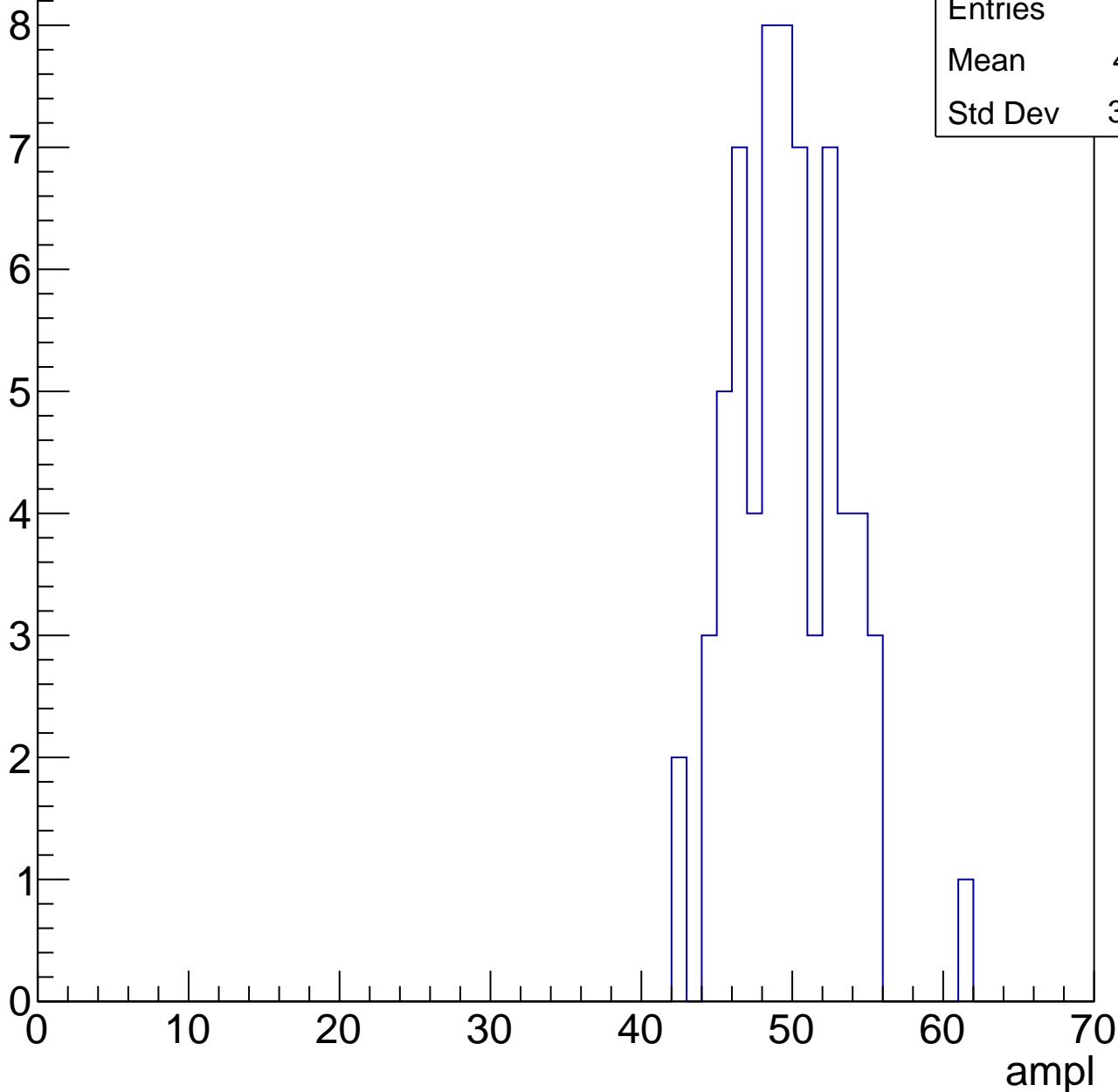


# B1L102S, U5-ch58, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

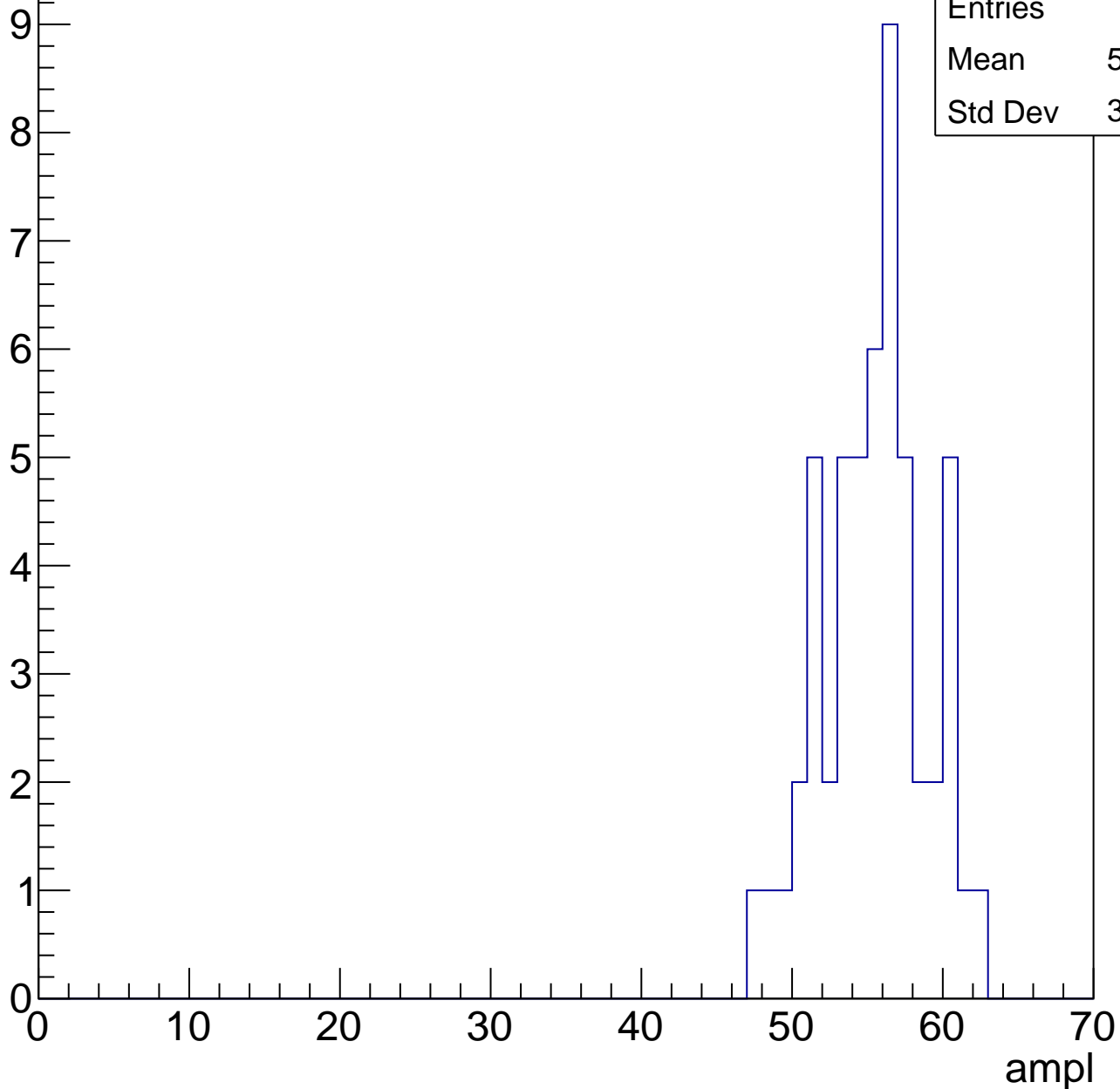
Entries	66
Mean	49.21
Std Dev	3.557



# B1L102S, U5-ch58, adc4

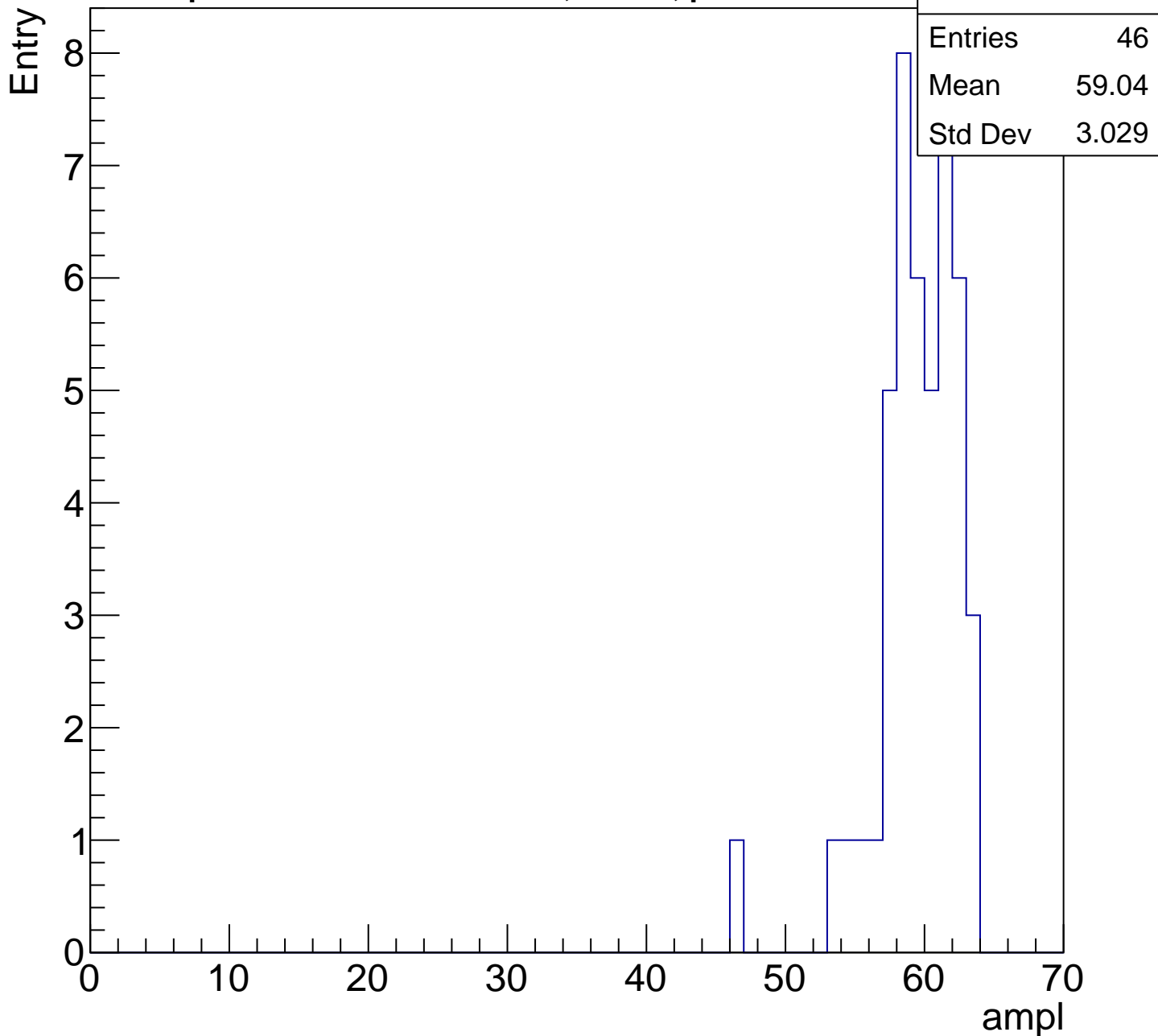
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U5-ch58, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

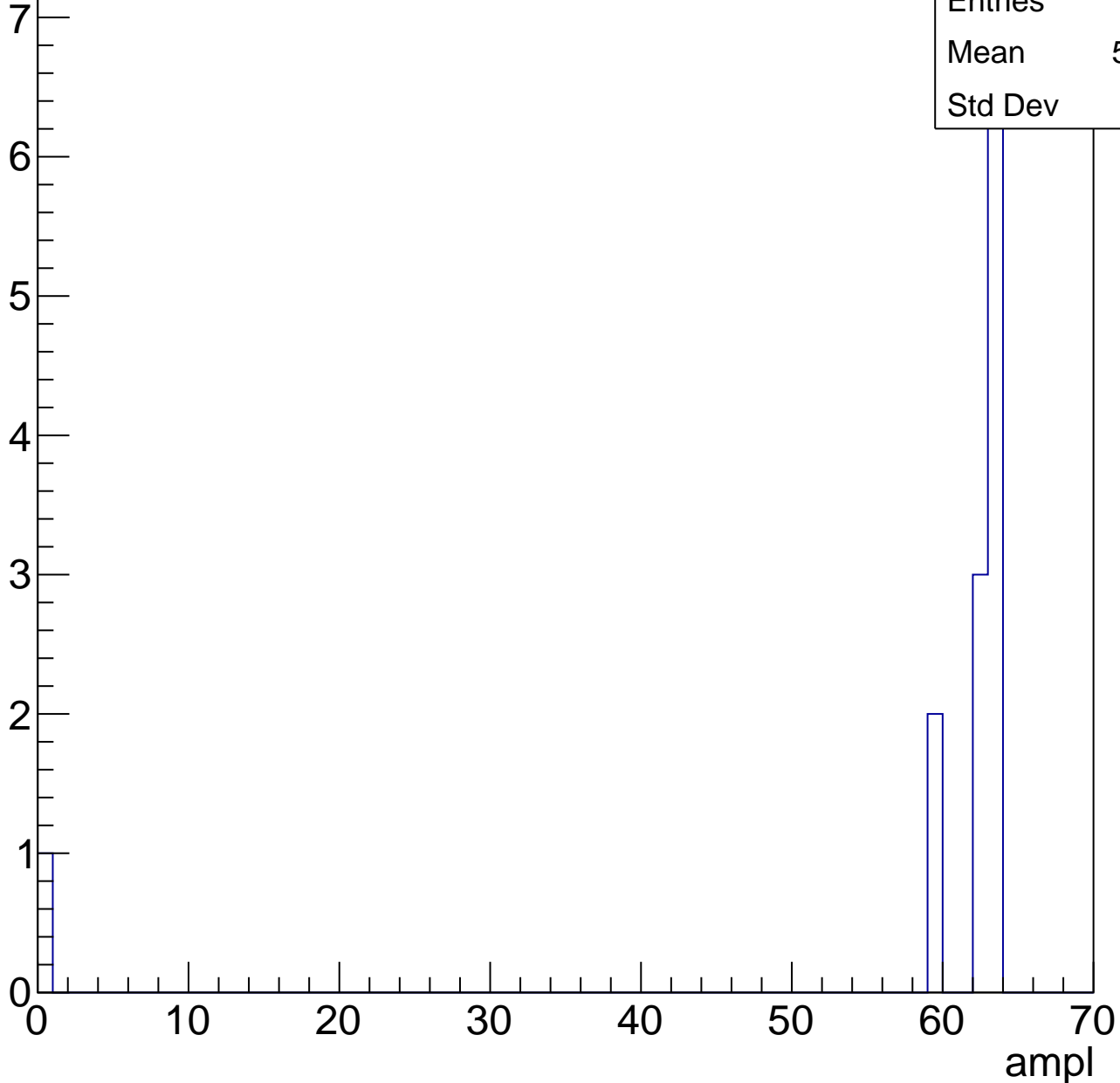


# B1L102S, U5-ch58, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	13
Mean	57.31
Std Dev	16.6





# B1L102S, U5-ch58, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U5-ch59, adc0

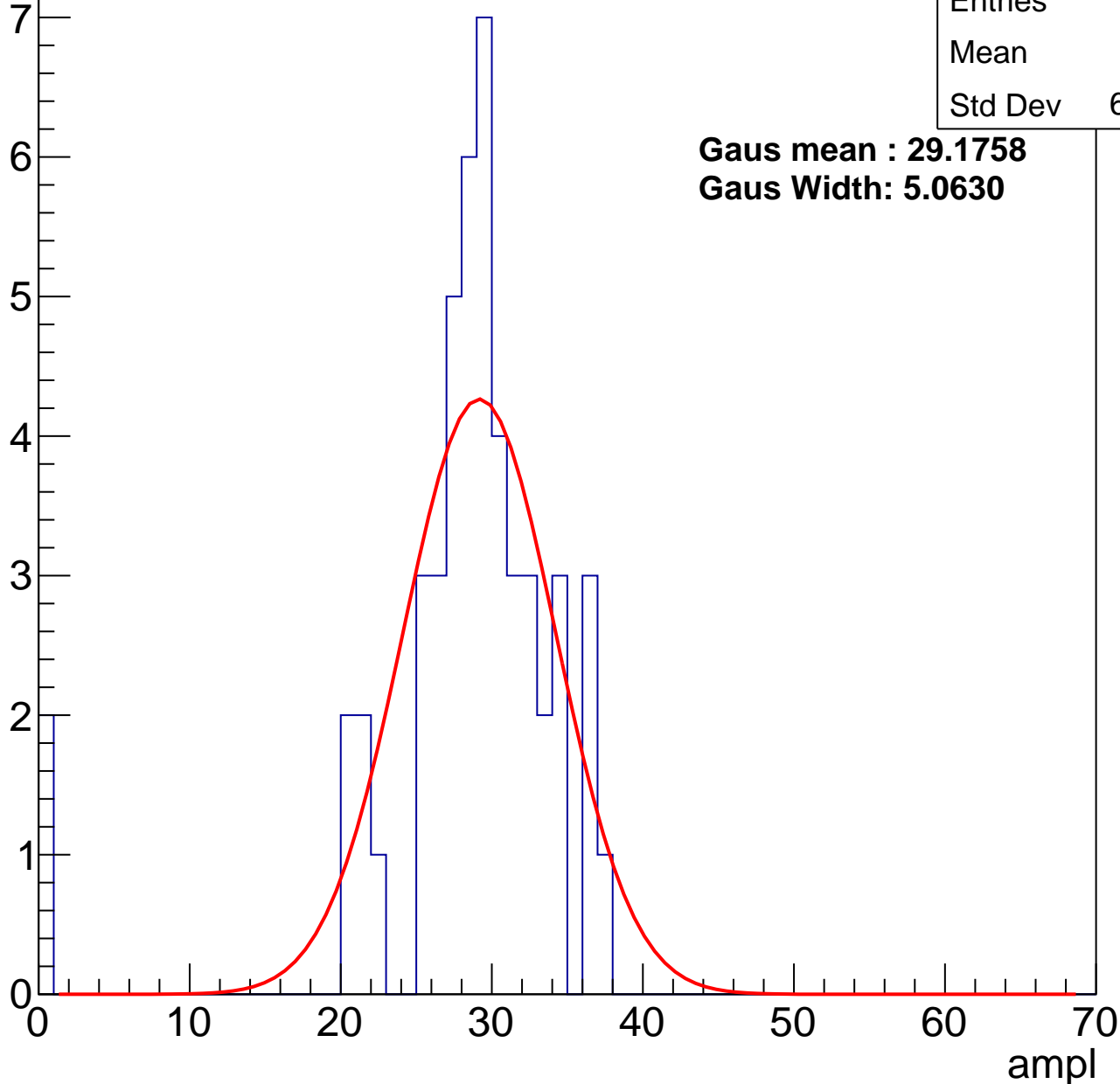
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	27.7
Std Dev	6.926

**Gaus mean : 29.1758**

**Gaus Width: 5.0630**



# B1L102S, U5-ch59, adc1

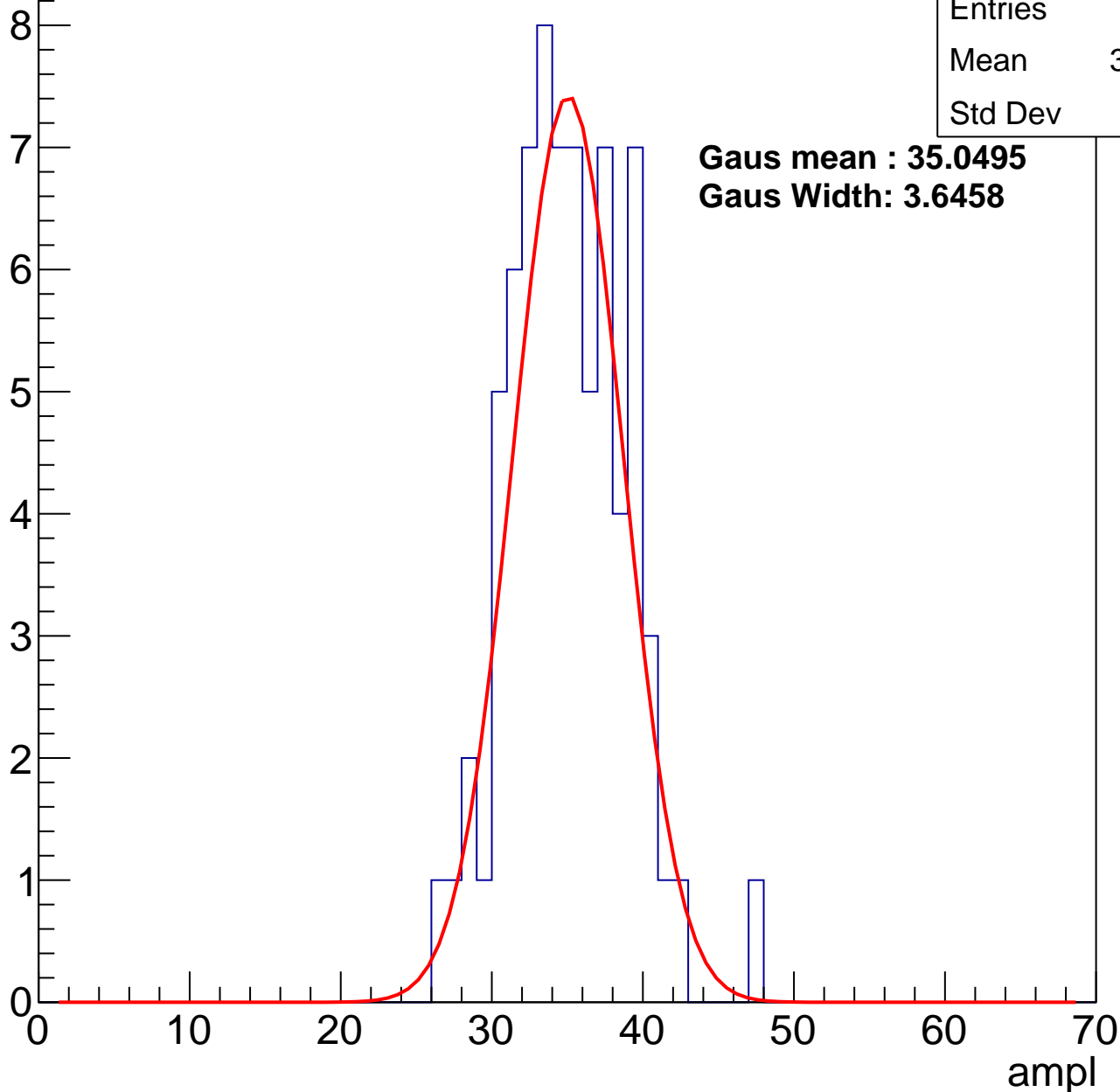
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	34.58
Std Dev	3.81

**Gaus mean : 35.0495**

**Gaus Width: 3.6458**



# B1L102S, U5-ch59, adc2

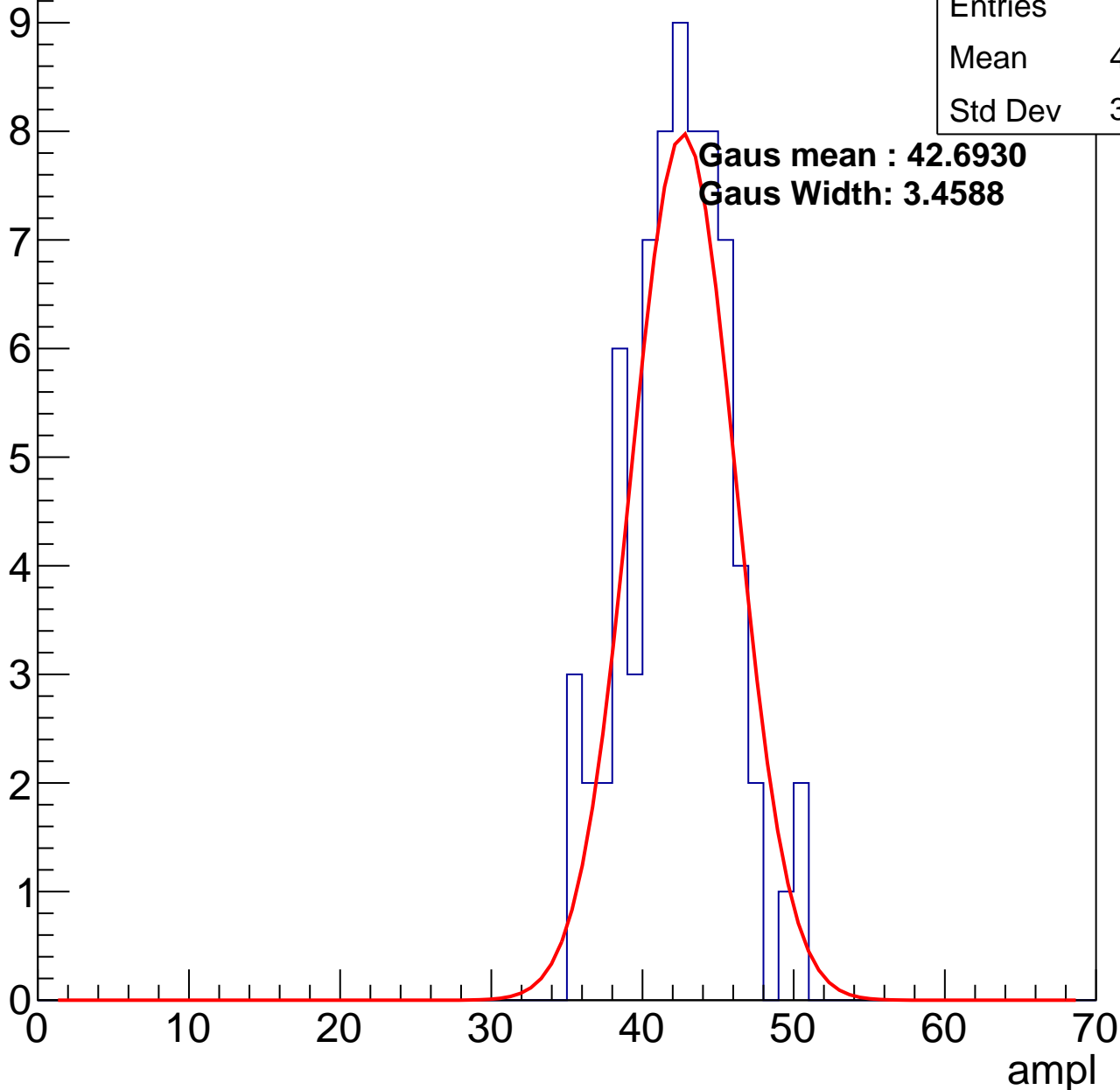
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	41.94
Std Dev	3.378

**Gaus mean : 42.6930**

**Gaus Width: 3.4588**

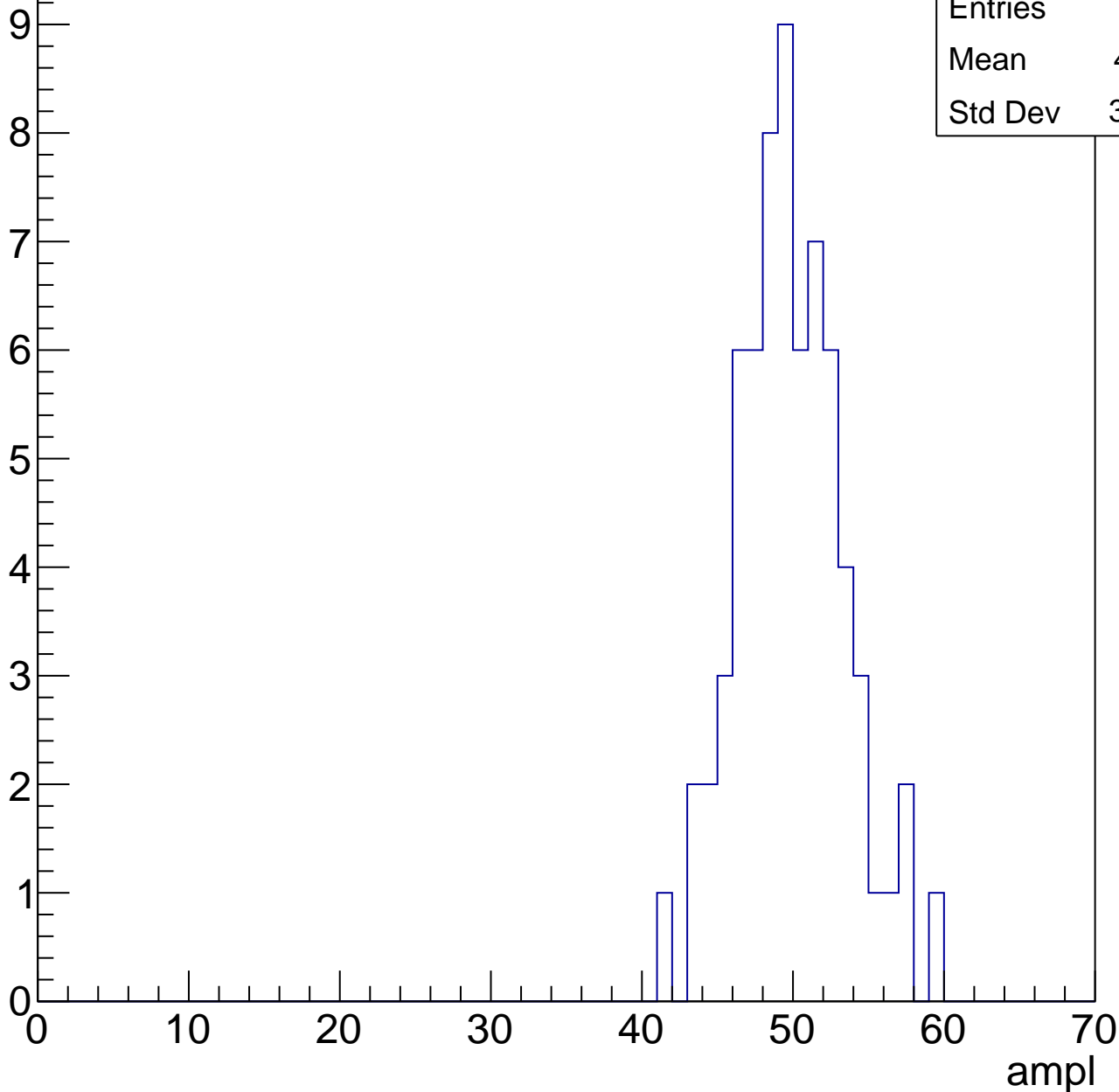


# B1L102S, U5-ch59, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	49.41
Std Dev	3.532

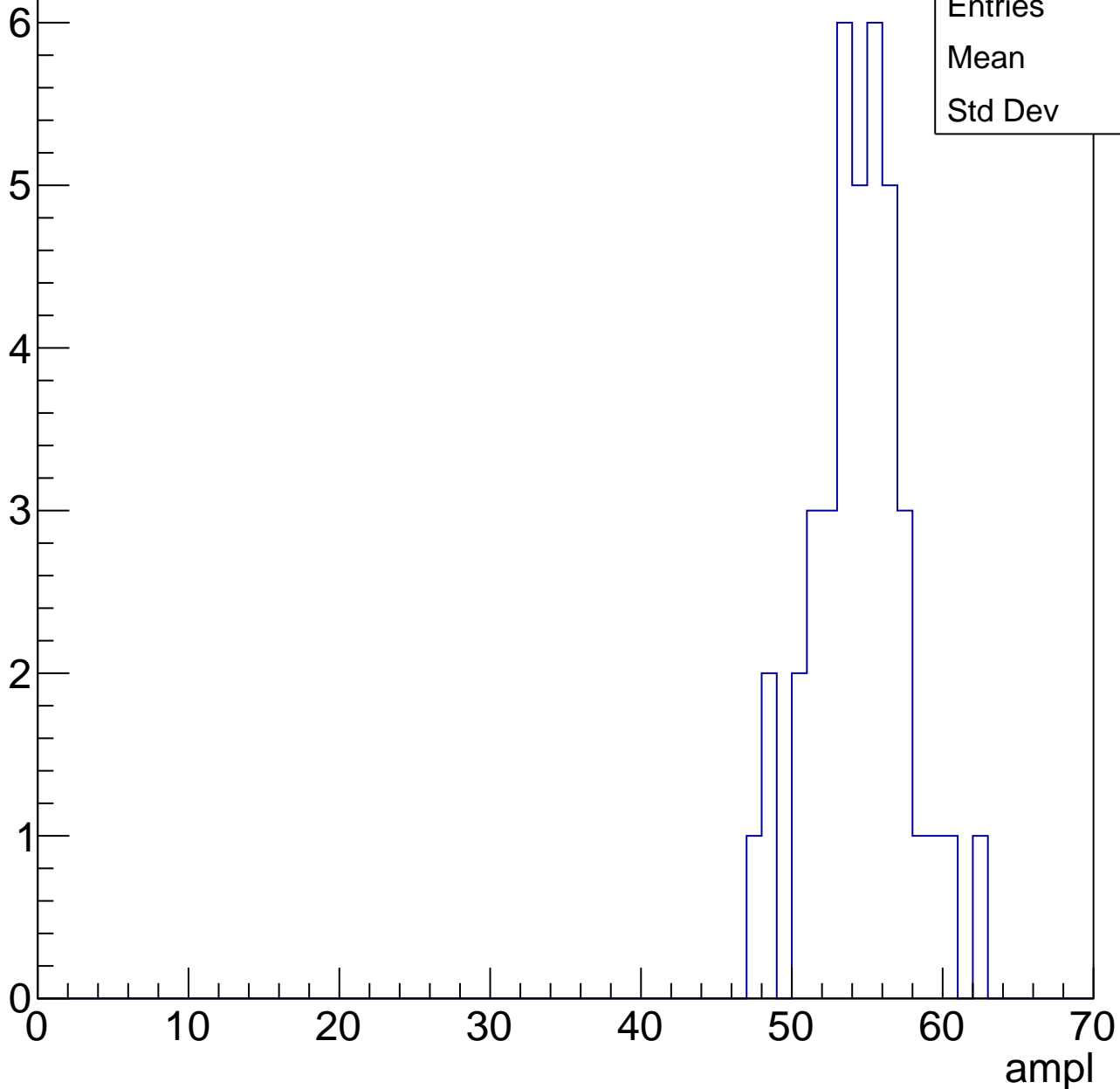


# B1L102S, U5-ch59, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	40
Mean	54
Std Dev	3.13



# B1L102S, U5-ch59, adc5

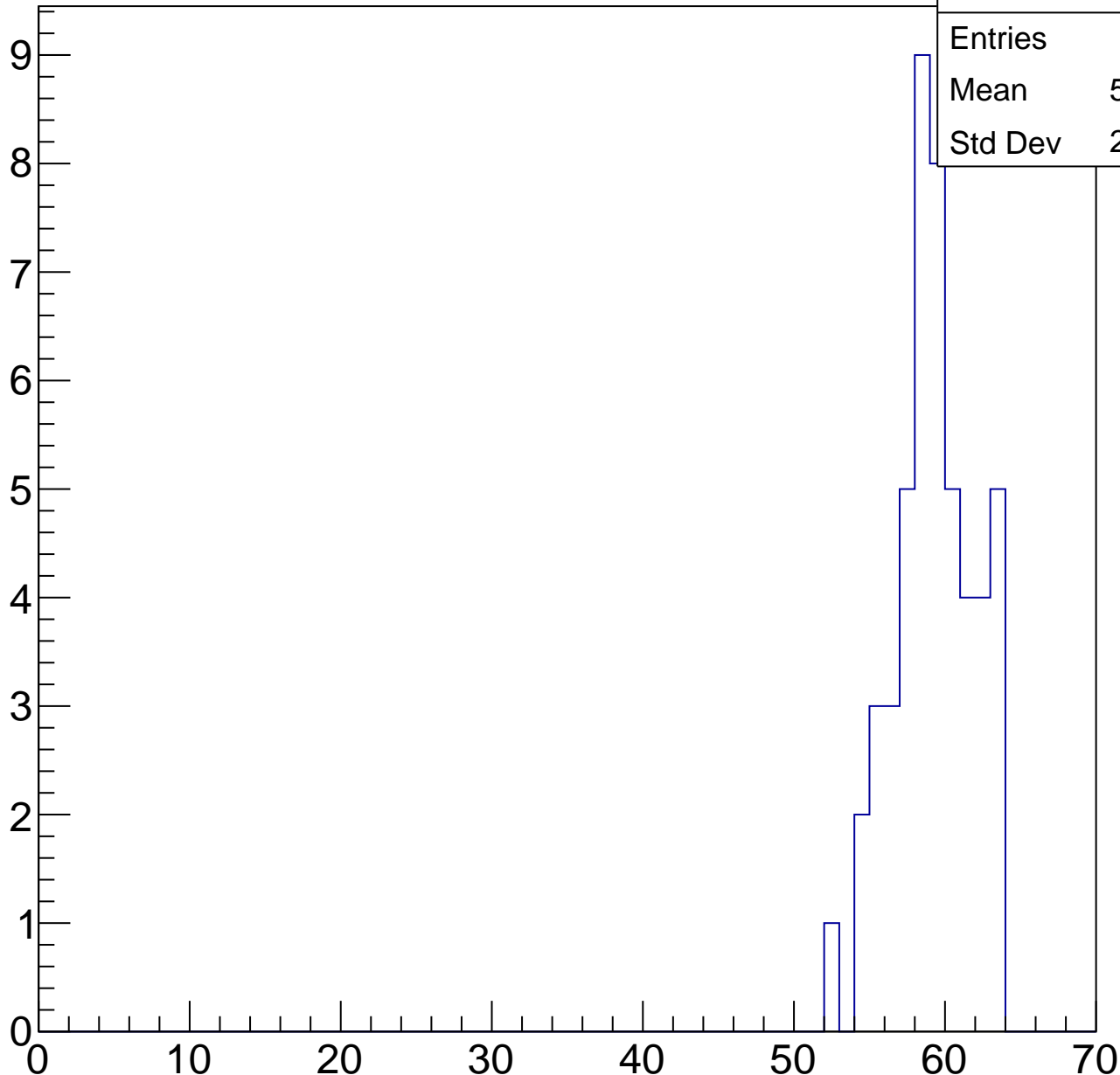
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	49
Mean	58.76
Std Dev	2.623

ampl

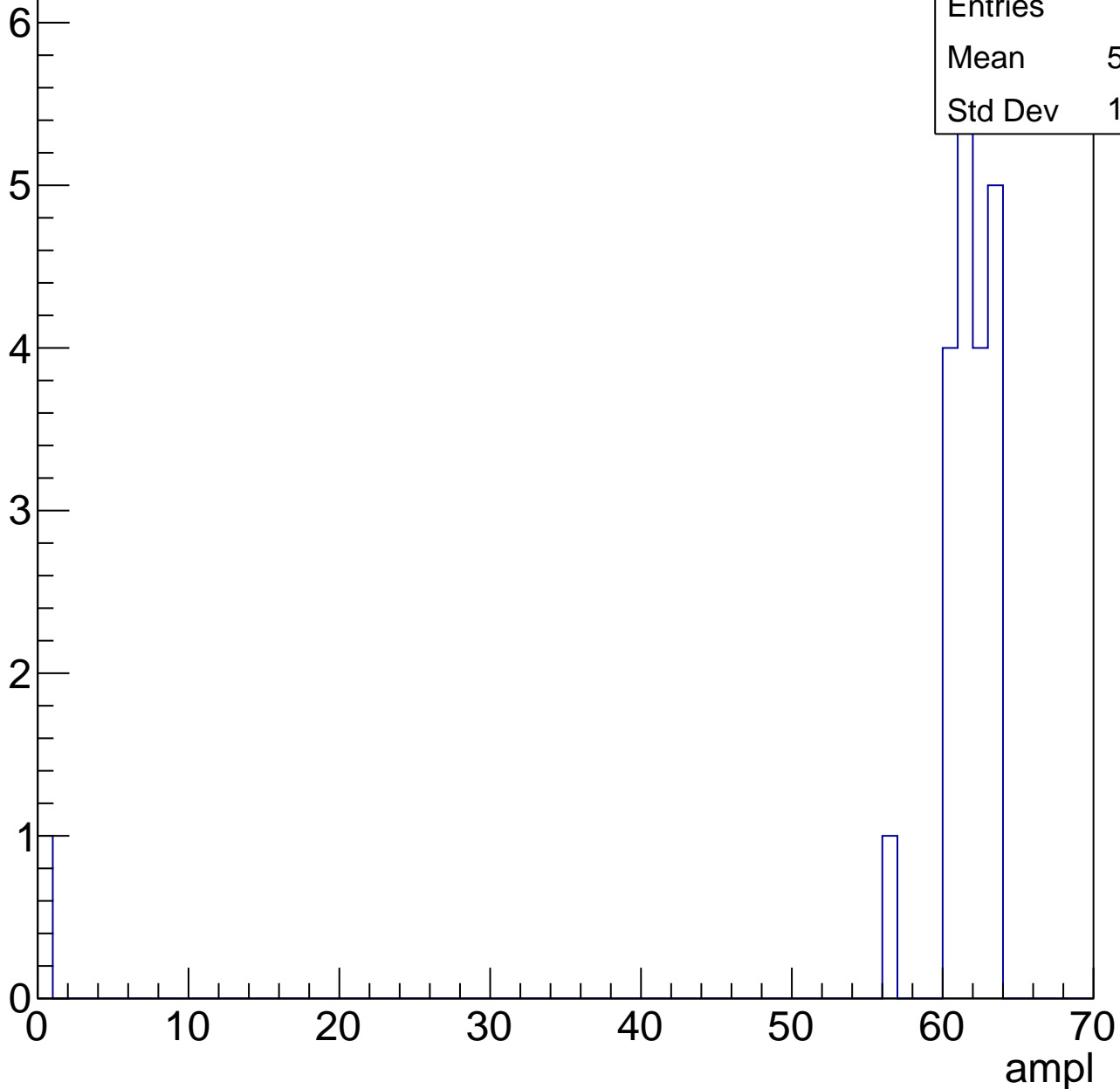


# B1L102S, U5-ch59, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	21
Mean	58.33
Std Dev	13.14





# B1L102S, U5-ch59, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U5-ch60, adc0

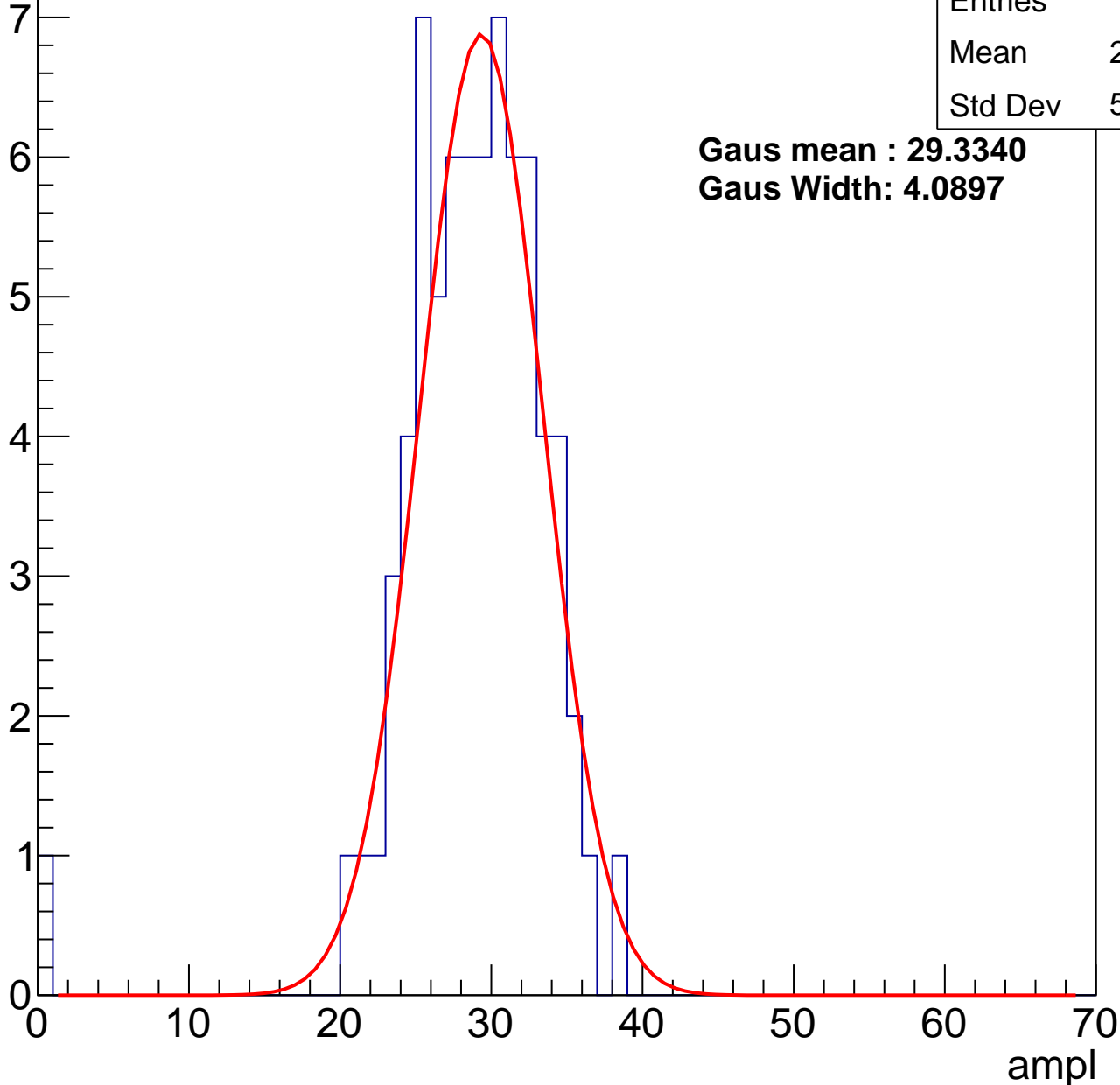
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	28.29
Std Dev	5.062

**Gaus mean : 29.3340**

**Gaus Width: 4.0897**



# B1L102S, U5-ch60, adc1

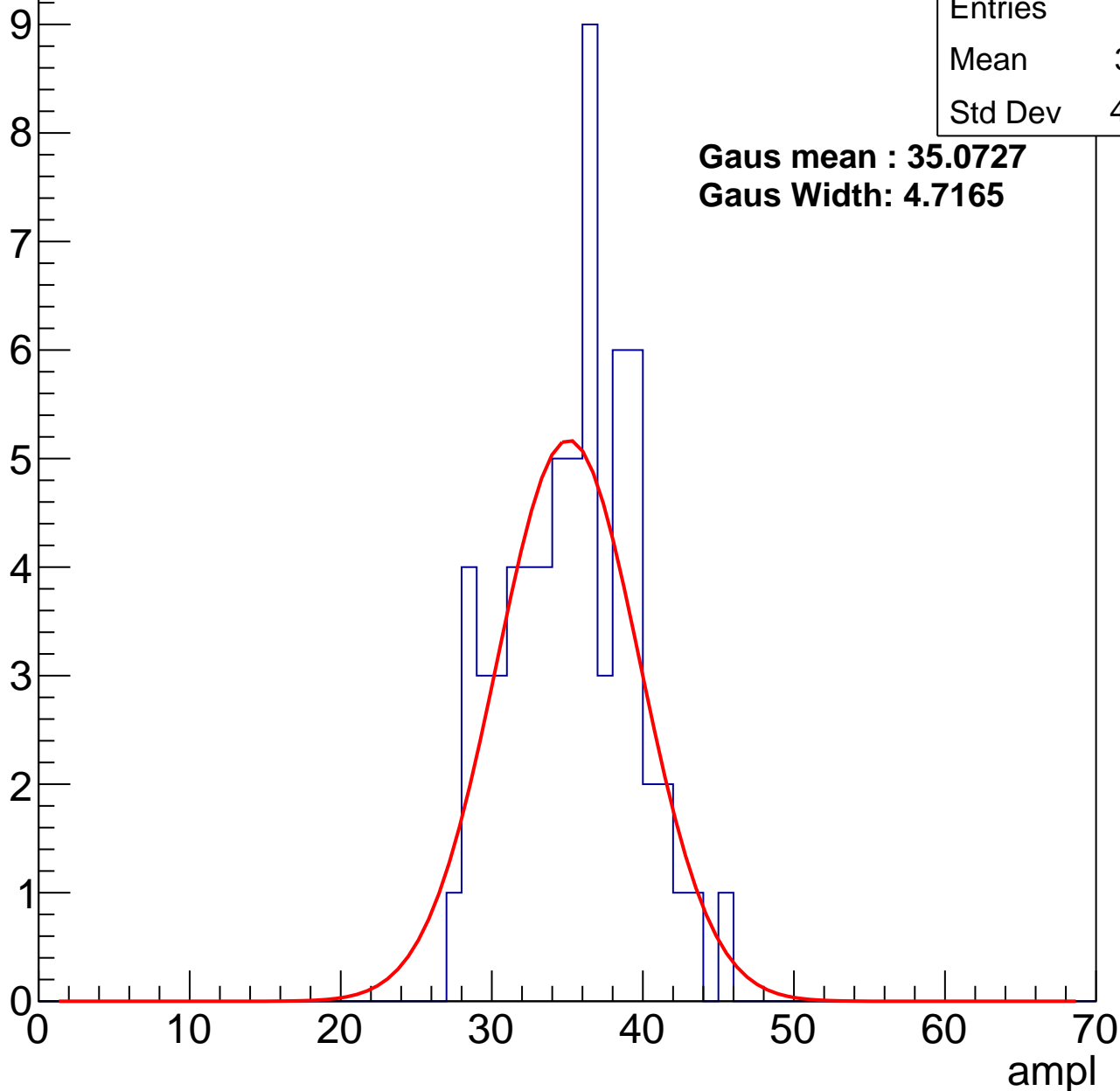
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	34.91
Std Dev	4.088

**Gaus mean : 35.0727**

**Gaus Width: 4.7165**



# B1L102S, U5-ch60, adc2

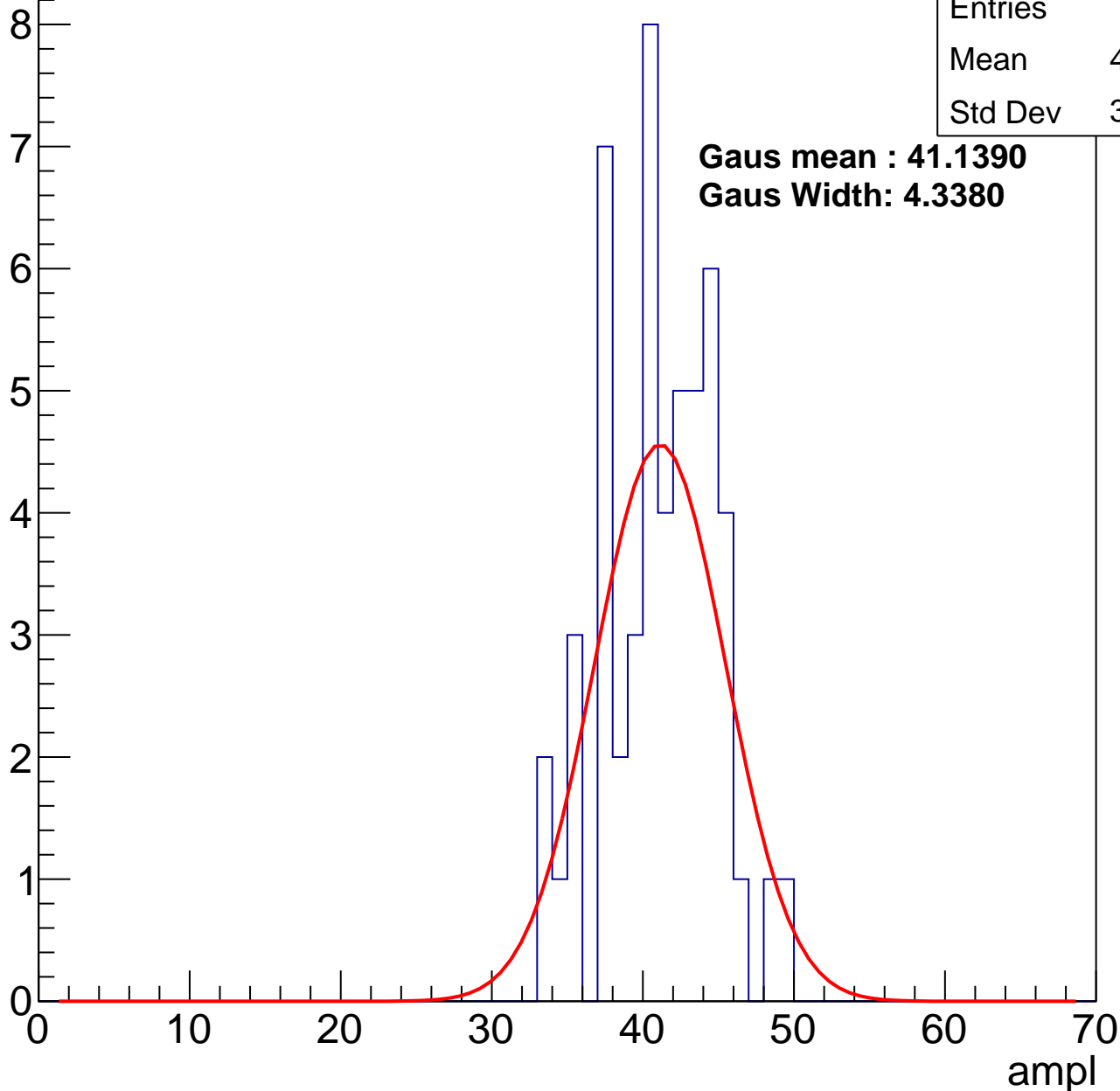
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	40.62
Std Dev	3.656

**Gaus mean : 41.1390**

**Gaus Width: 4.3380**

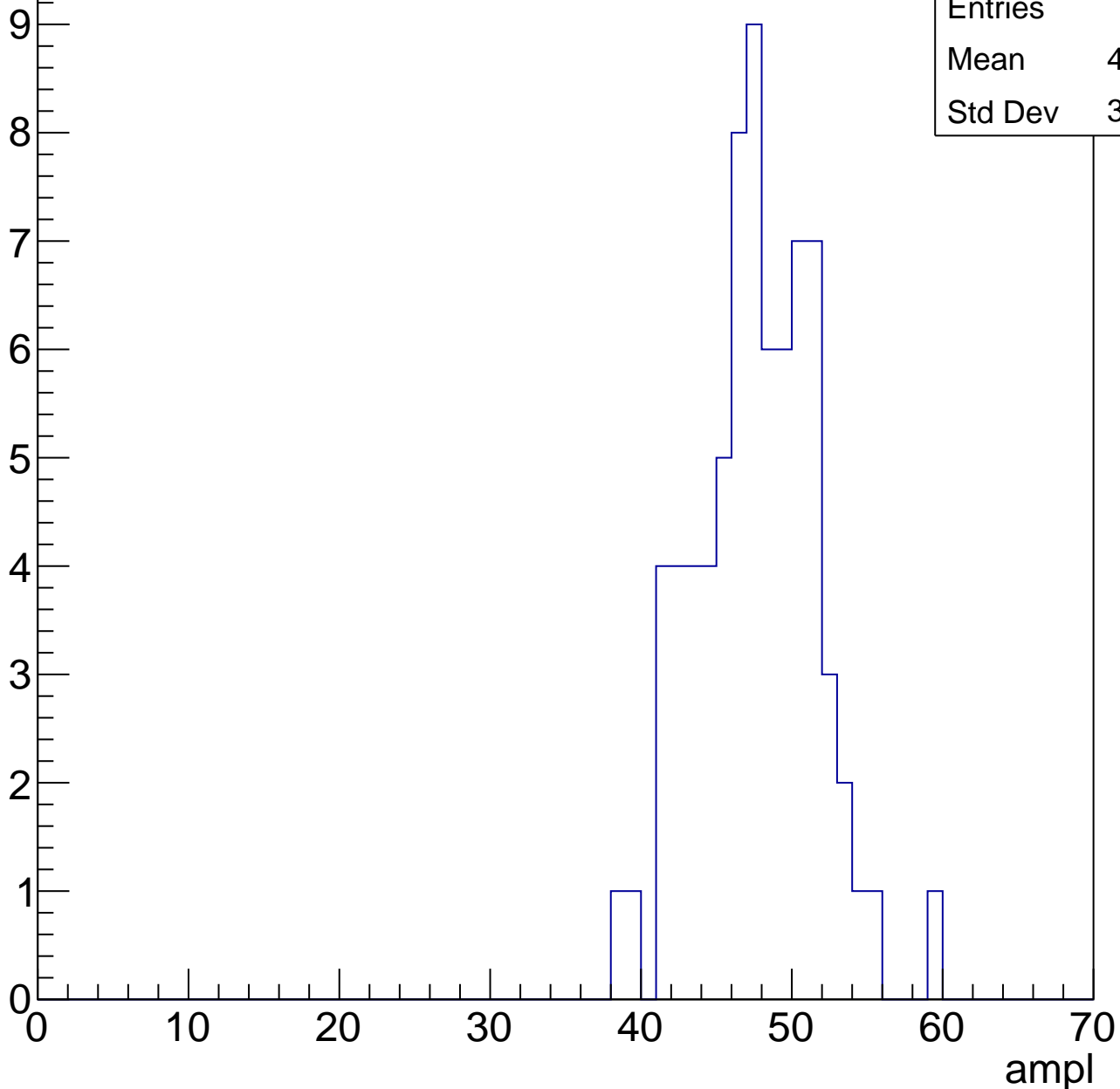


# B1L102S, U5-ch60, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

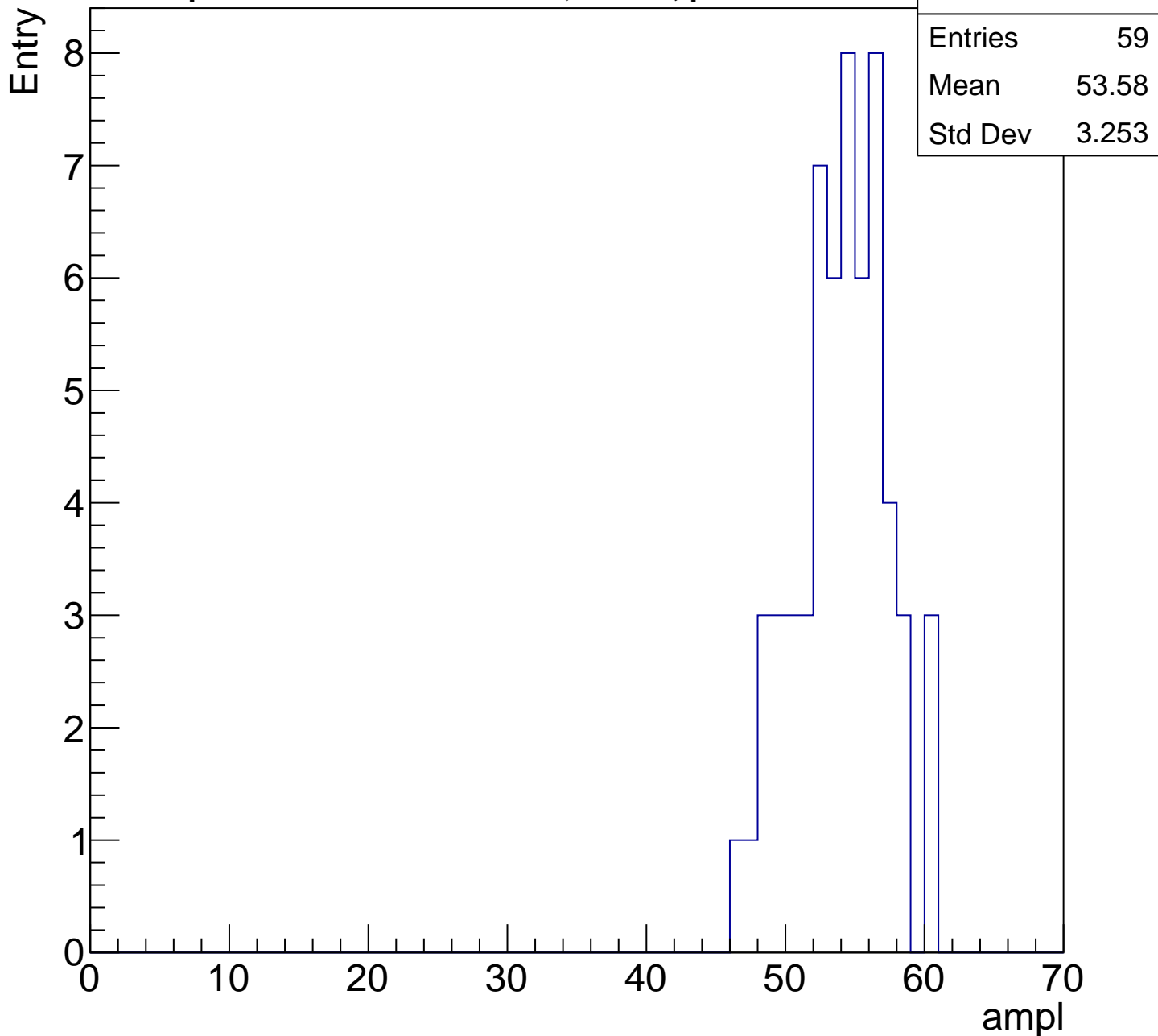
Entry

Entries	74
Mean	47.19
Std Dev	3.896



# B1L102S, U5-ch60, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

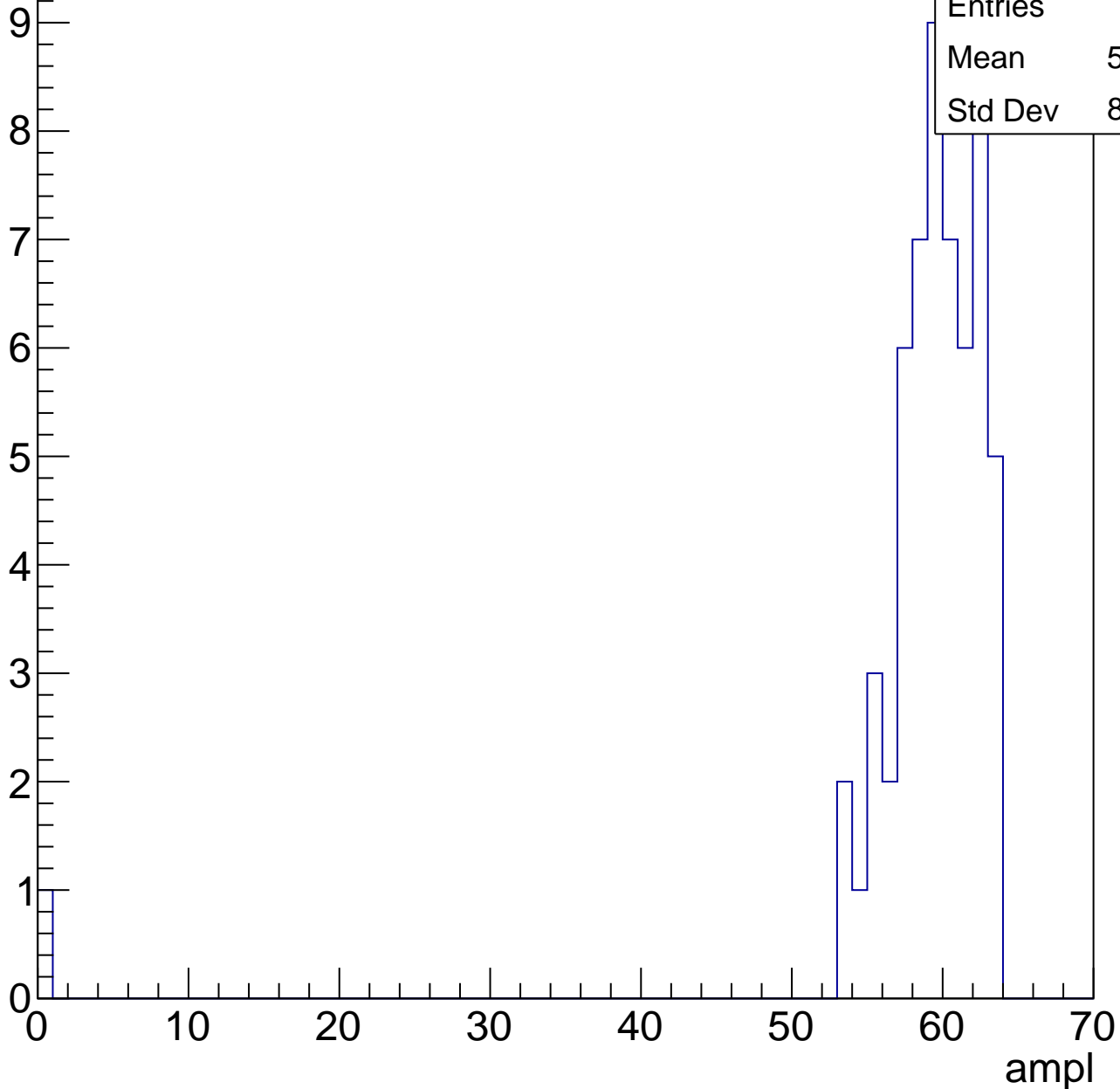


# B1L102S, U5-ch60, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

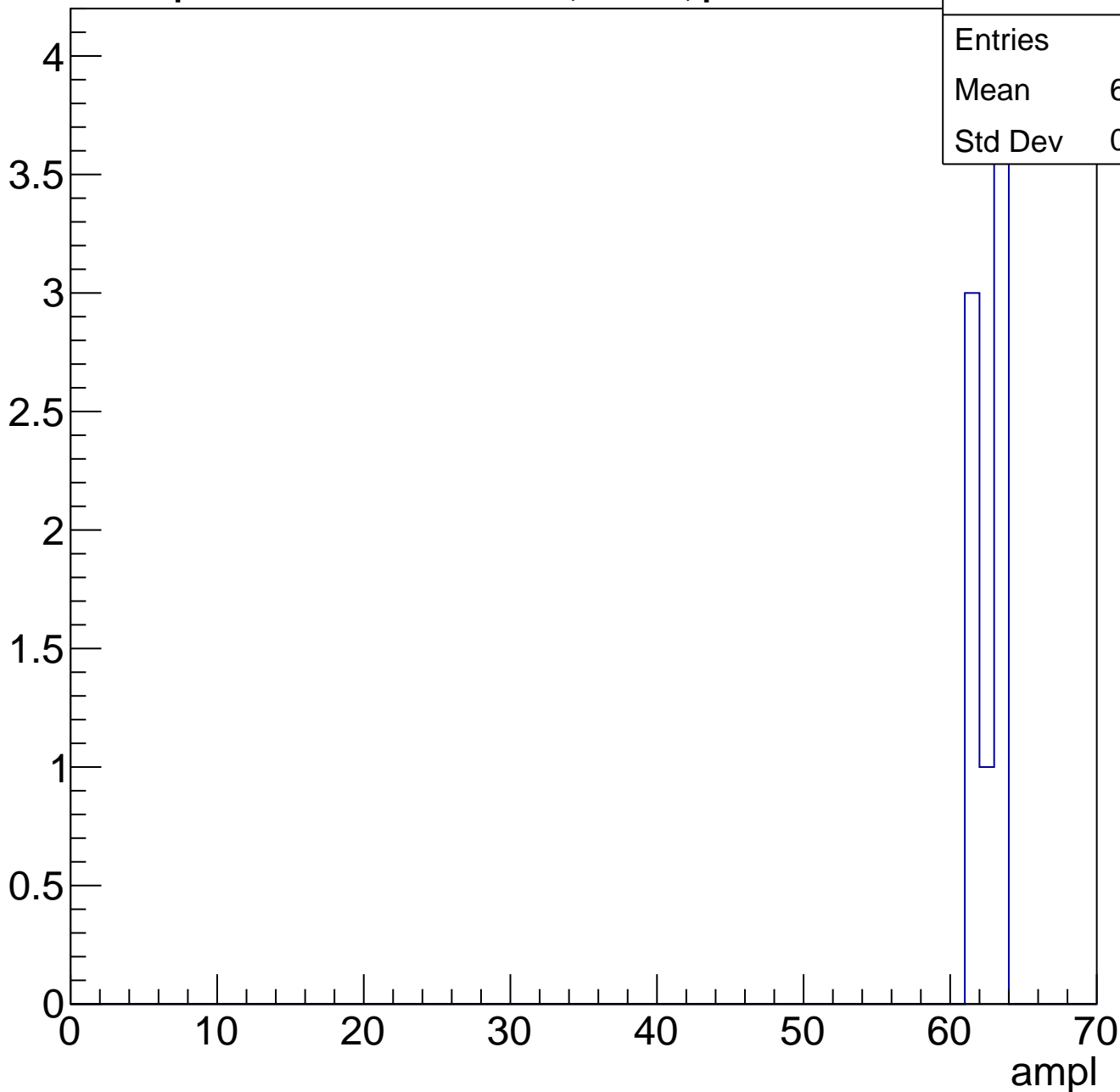
Entries	58
Mean	58.19
Std Dev	8.125



# B1L102S, U5-ch60, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

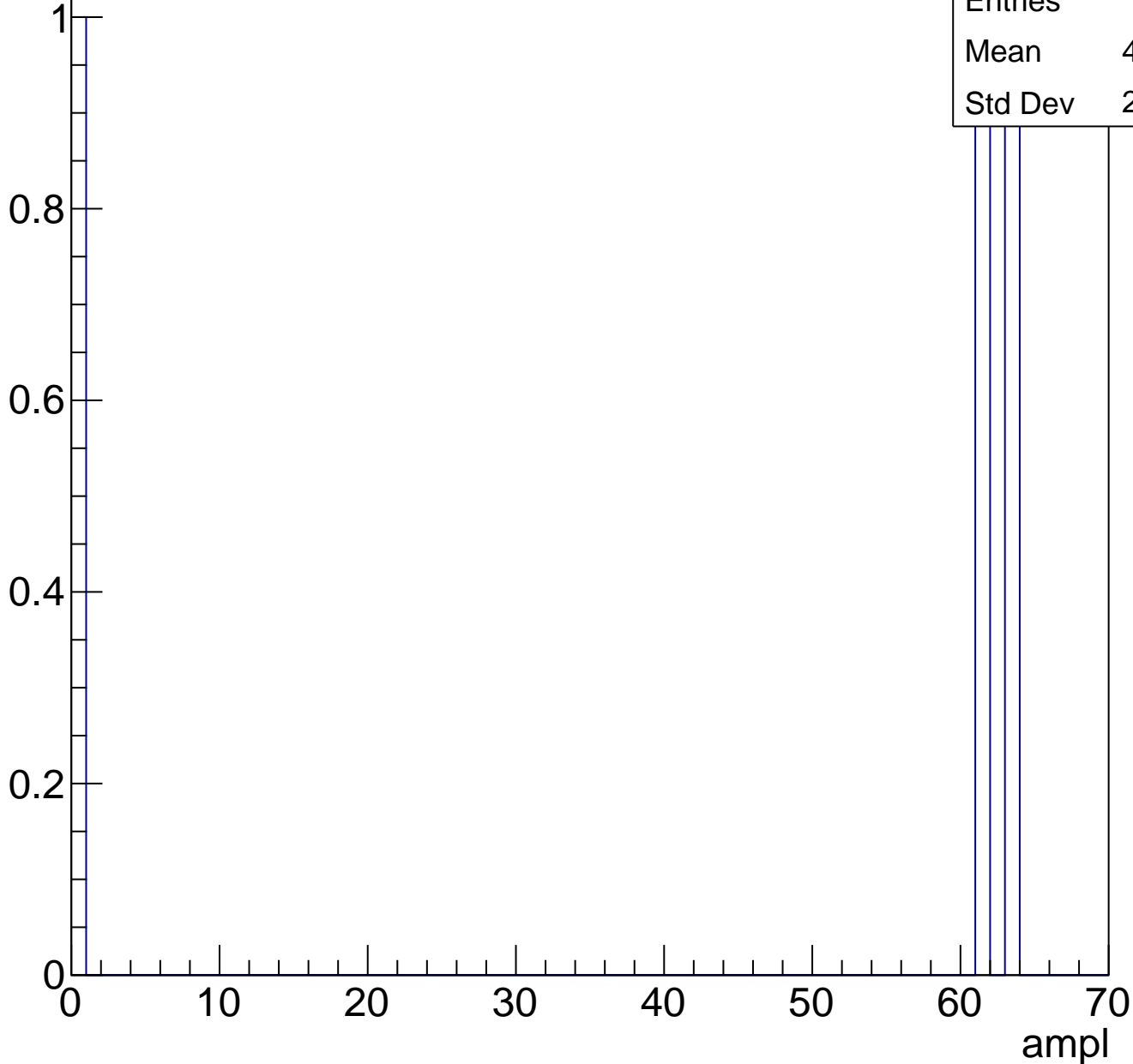




# B1L102S, U5-ch60, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U5-ch61, adc0

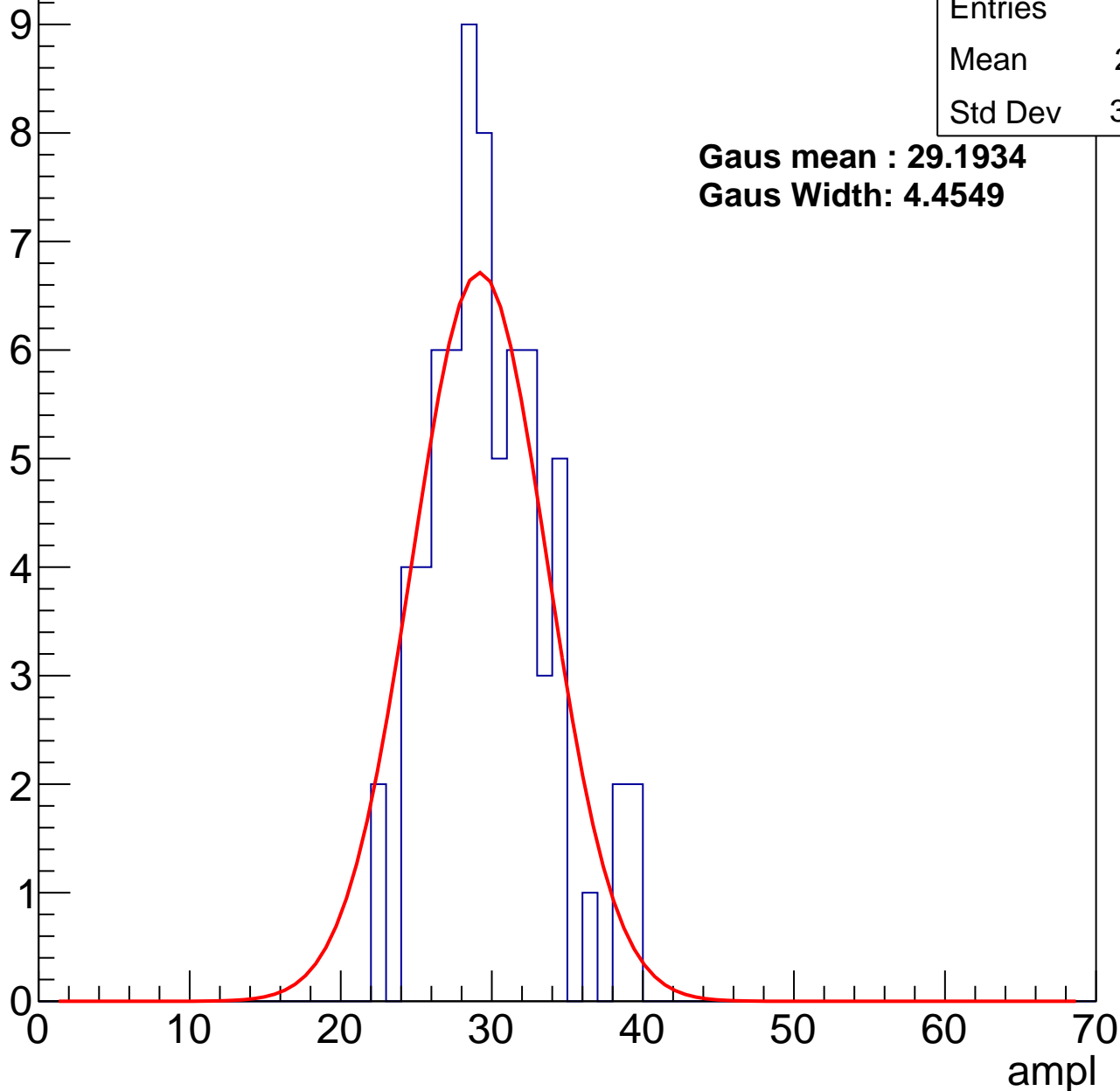
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	29.41
Std Dev	3.816

**Gaus mean : 29.1934**

**Gaus Width: 4.4549**



# B1L102S, U5-ch61, adc1

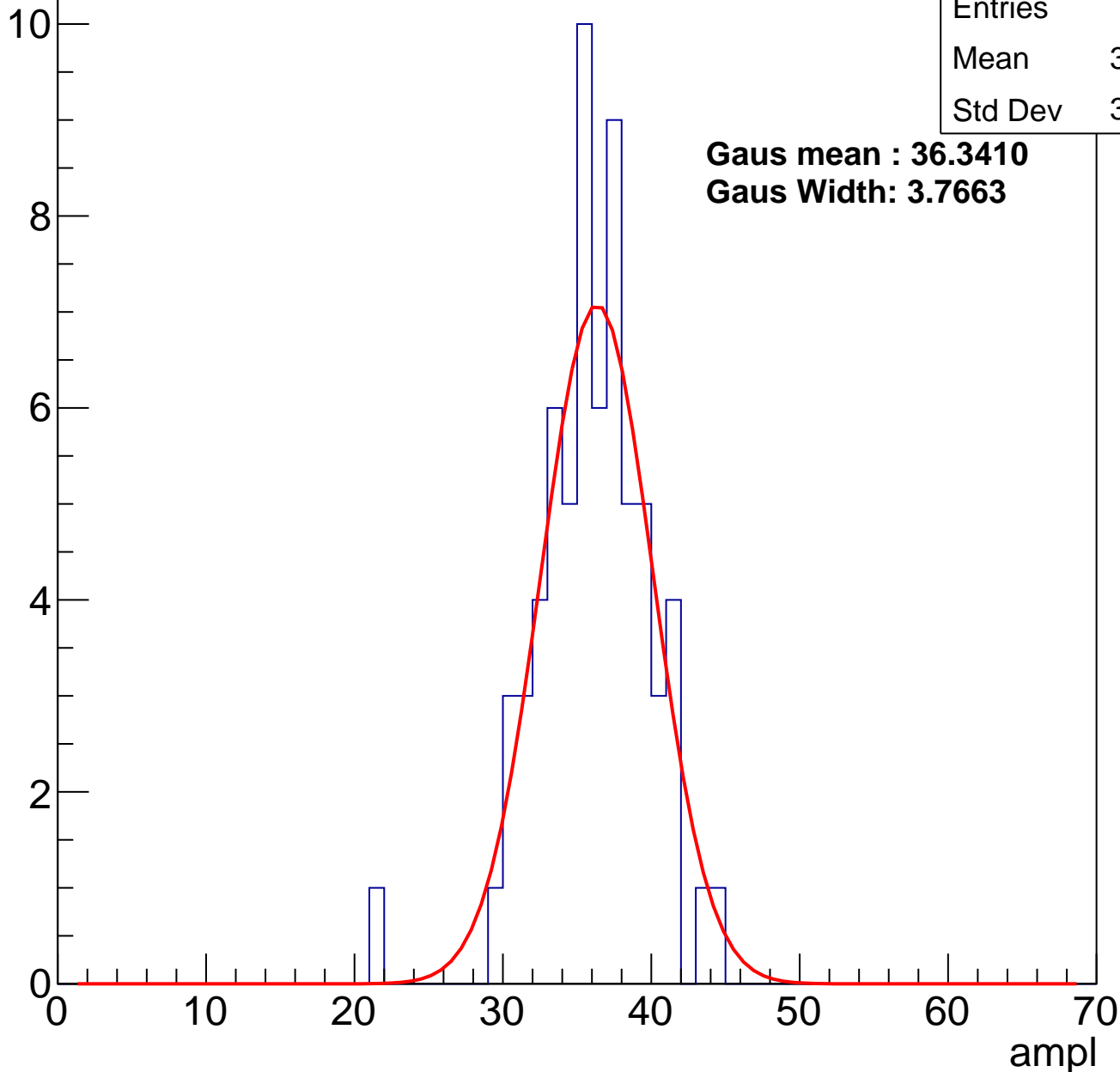
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	67
Mean	35.58
Std Dev	3.722

**Gaus mean : 36.3410**

**Gaus Width: 3.7663**

Entry

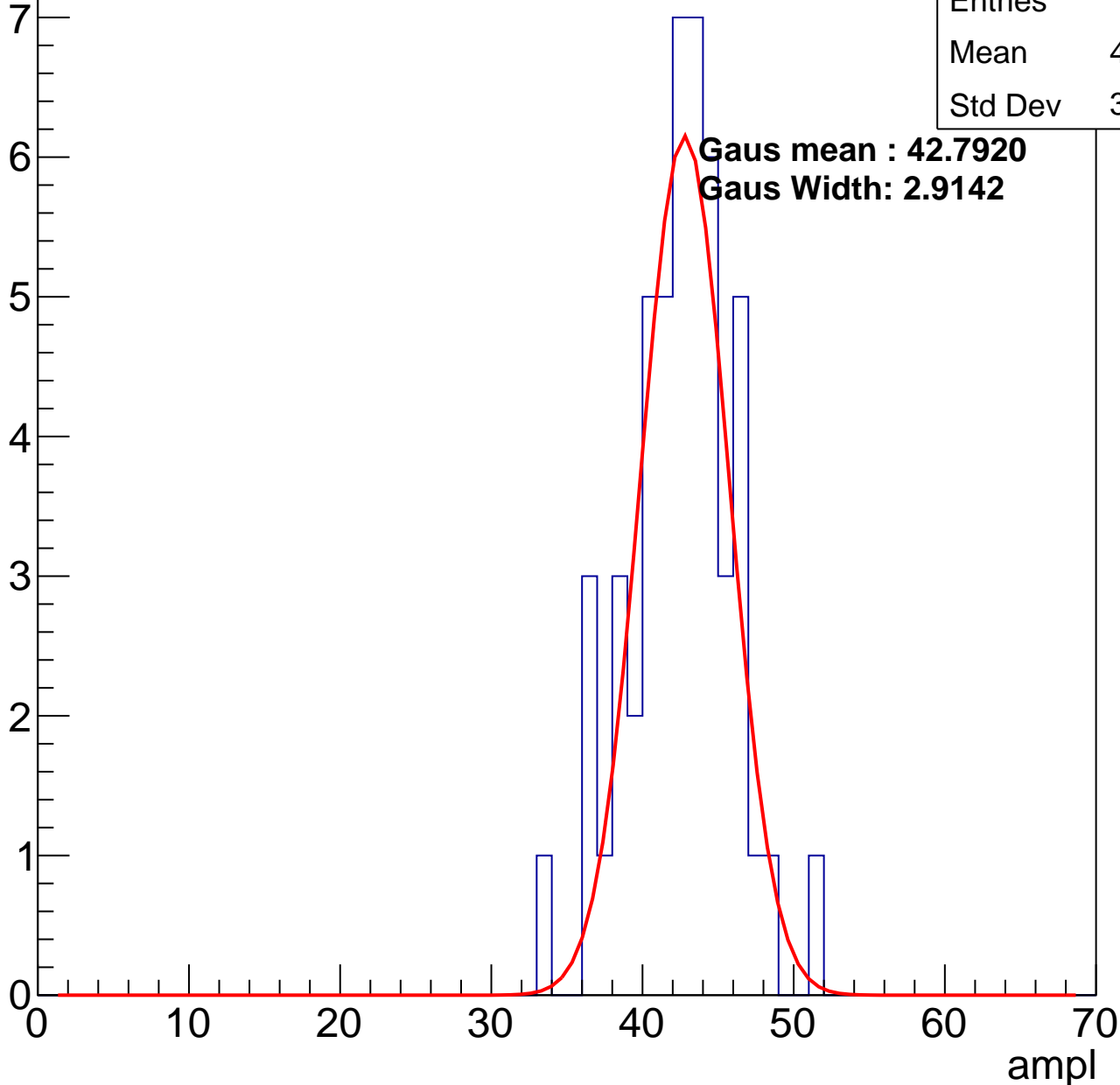


# B1L102S, U5-ch61, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	42.06
Std Dev	3.386

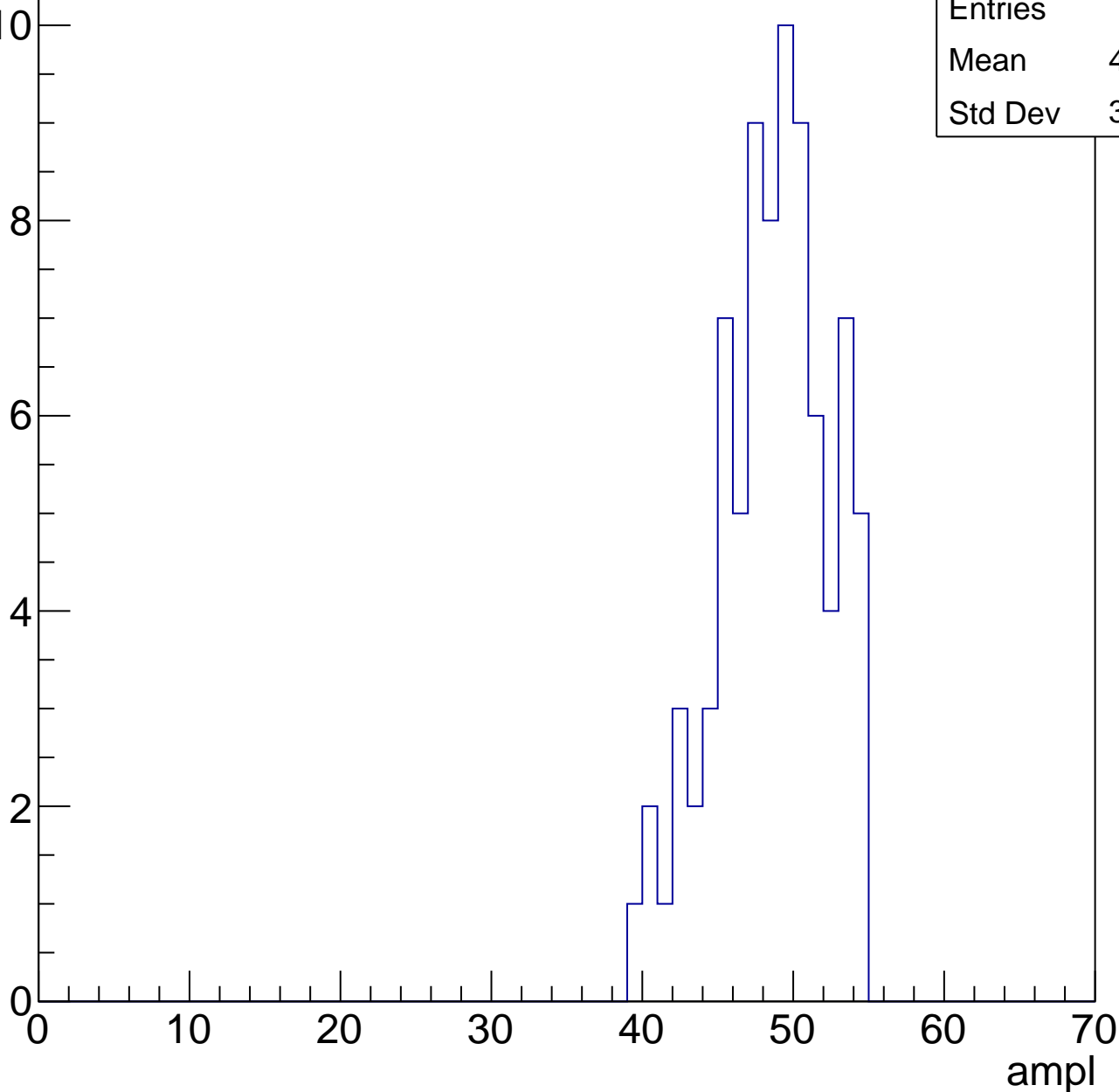


# B1L102S, U5-ch61, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	82
Mean	48.18
Std Dev	3.616

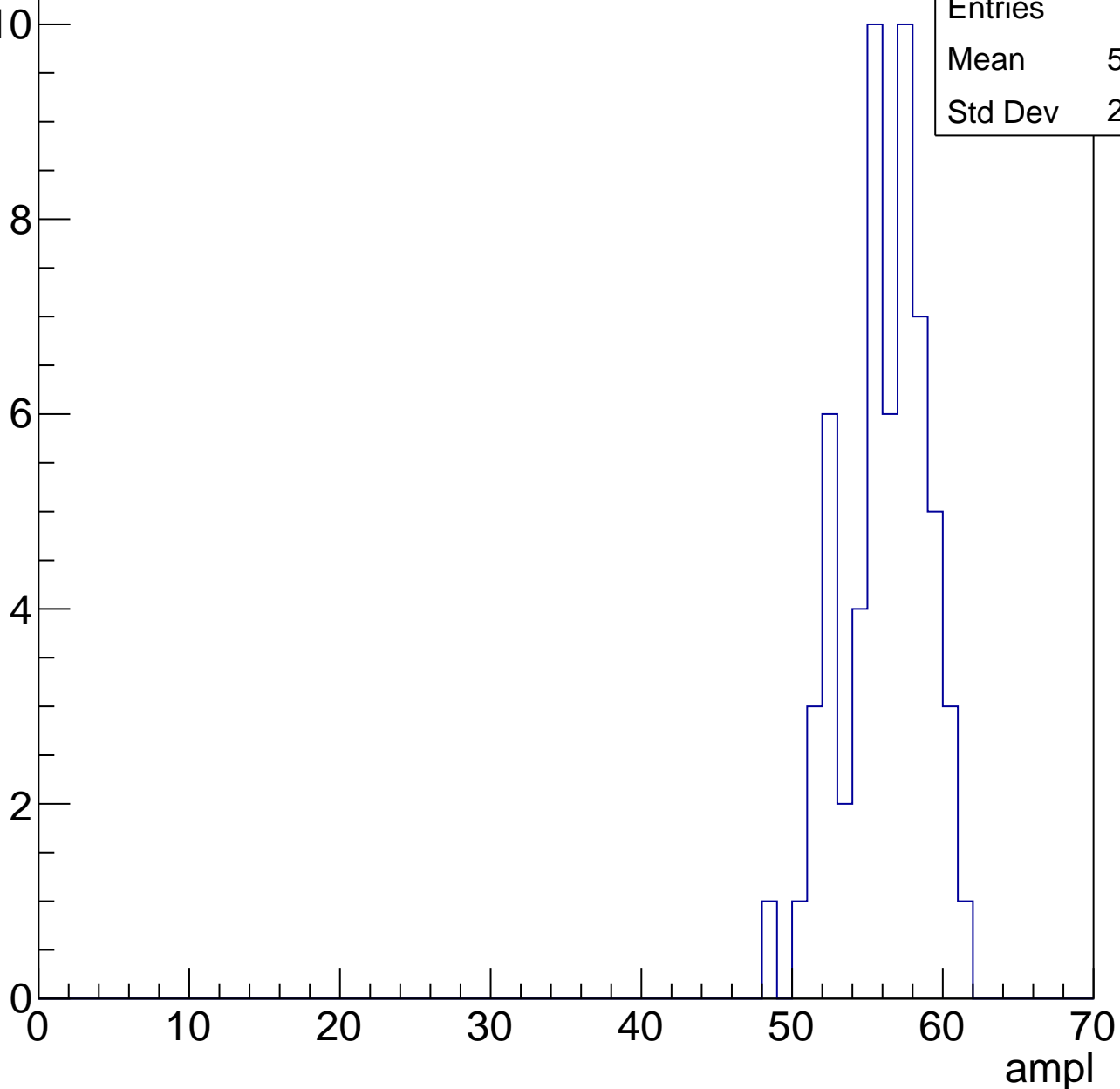


# B1L102S, U5-ch61, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	55.64
Std Dev	2.803

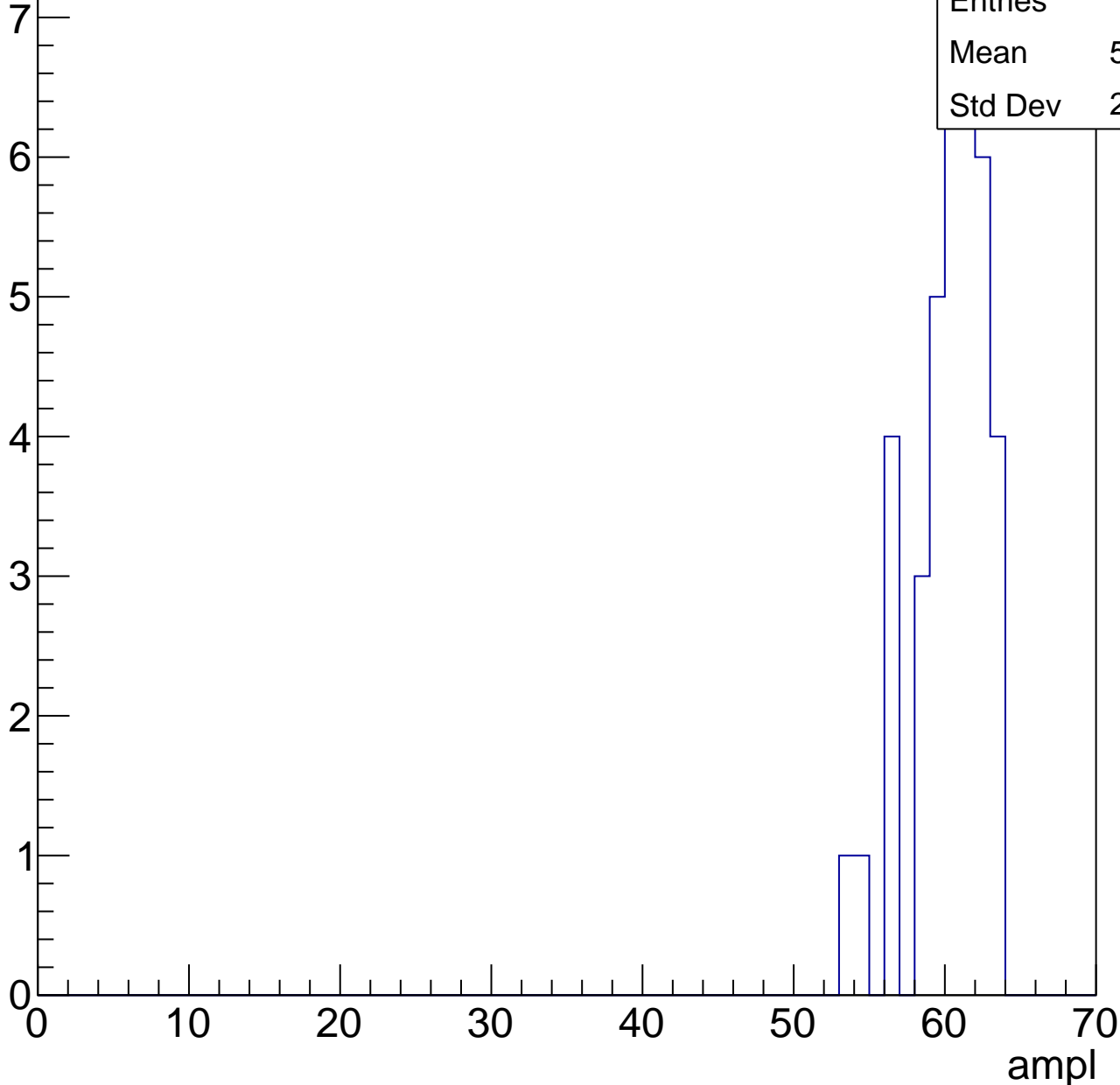


# B1L102S, U5-ch61, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	38
Mean	59.76
Std Dev	2.465

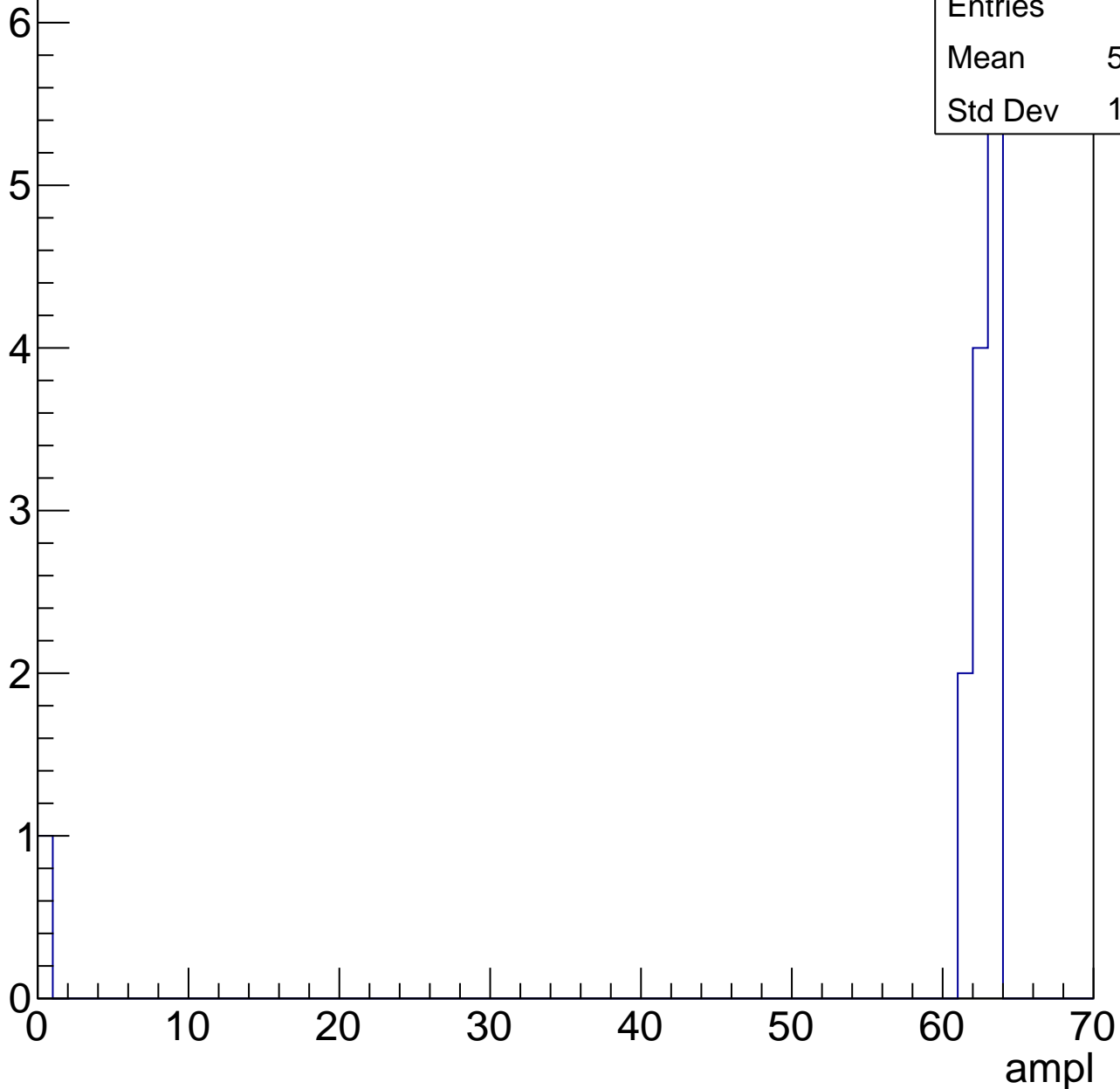


# B1L102S, U5-ch61, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	13
Mean	57.54
Std Dev	16.63

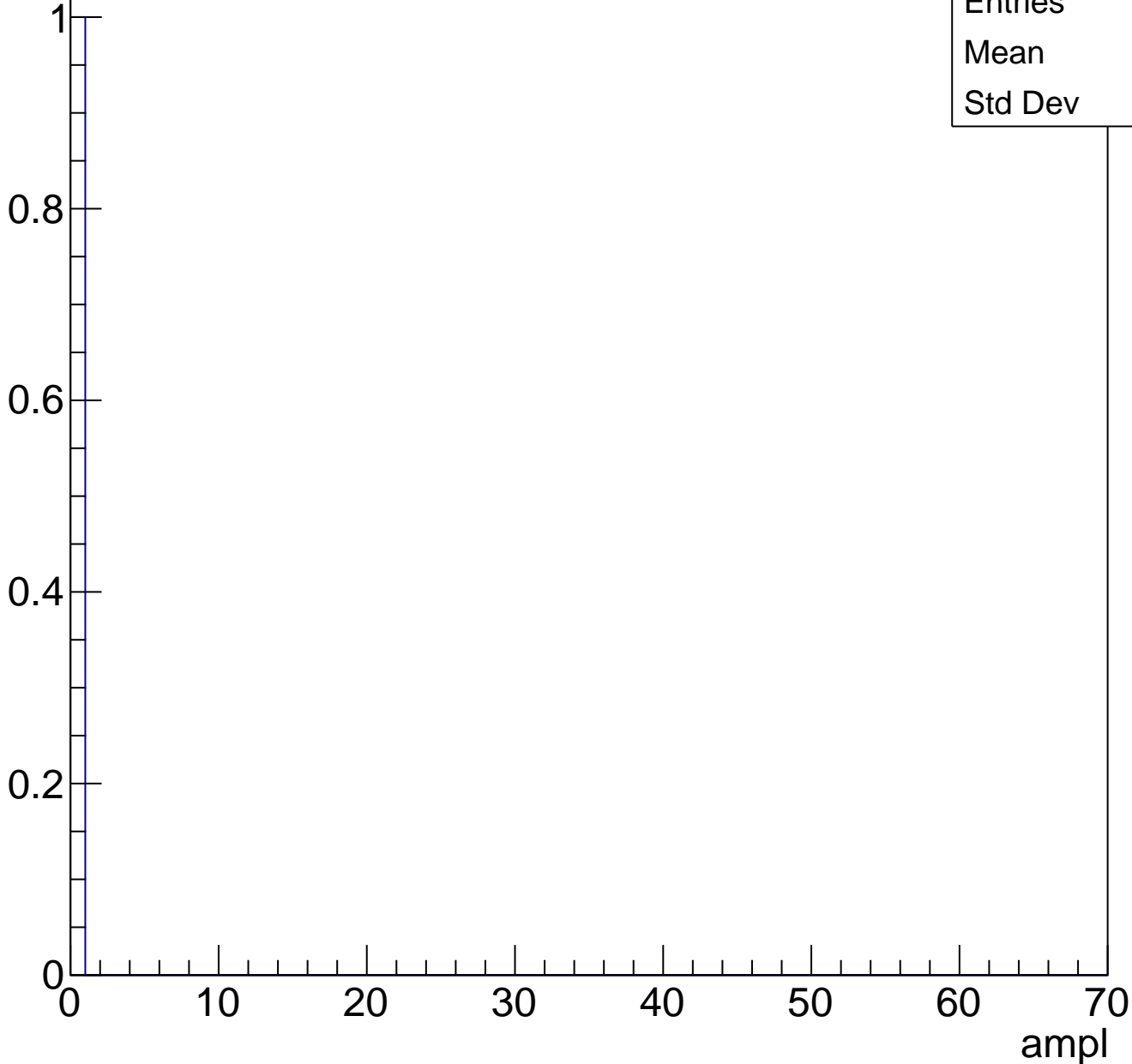




# B1L102S, U5-ch61, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U5-ch62, adc0

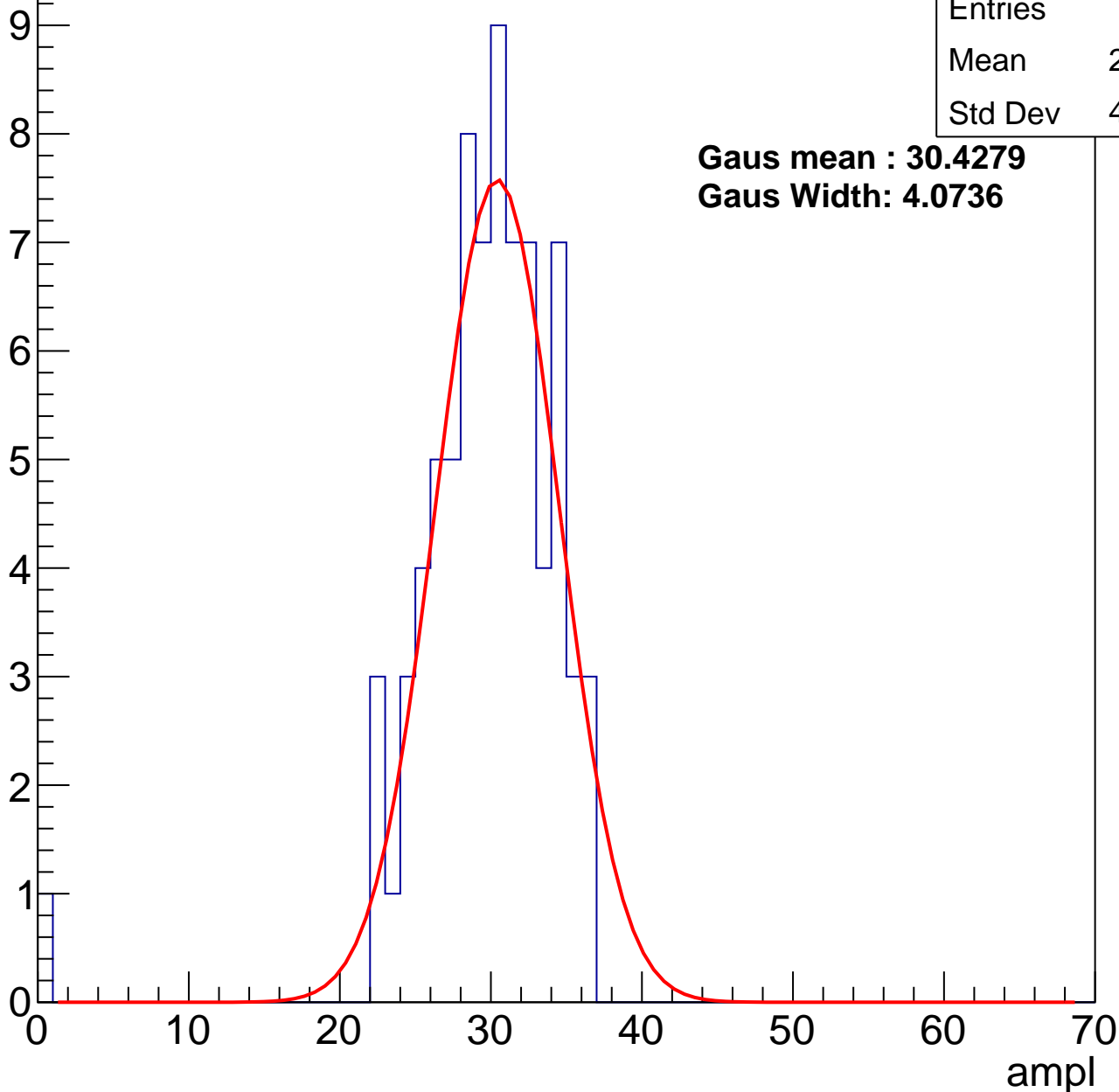
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	29.18
Std Dev	4.872

**Gaus mean : 30.4279**

**Gaus Width: 4.0736**



# B1L102S, U5-ch62, adc1

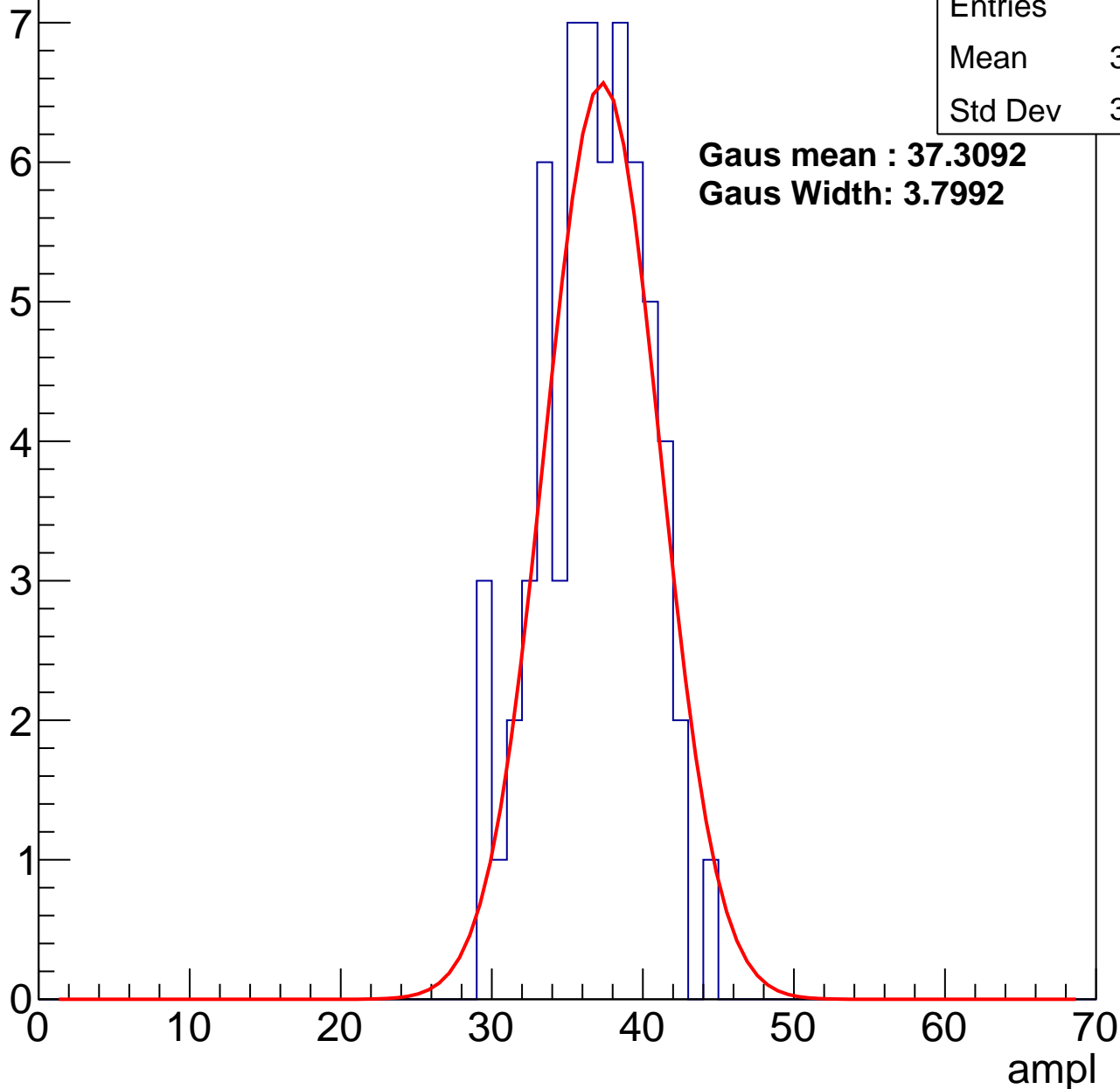
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	36.29
Std Dev	3.457

**Gaus mean : 37.3092**

**Gaus Width: 3.7992**



# B1L102S, U5-ch62, adc2

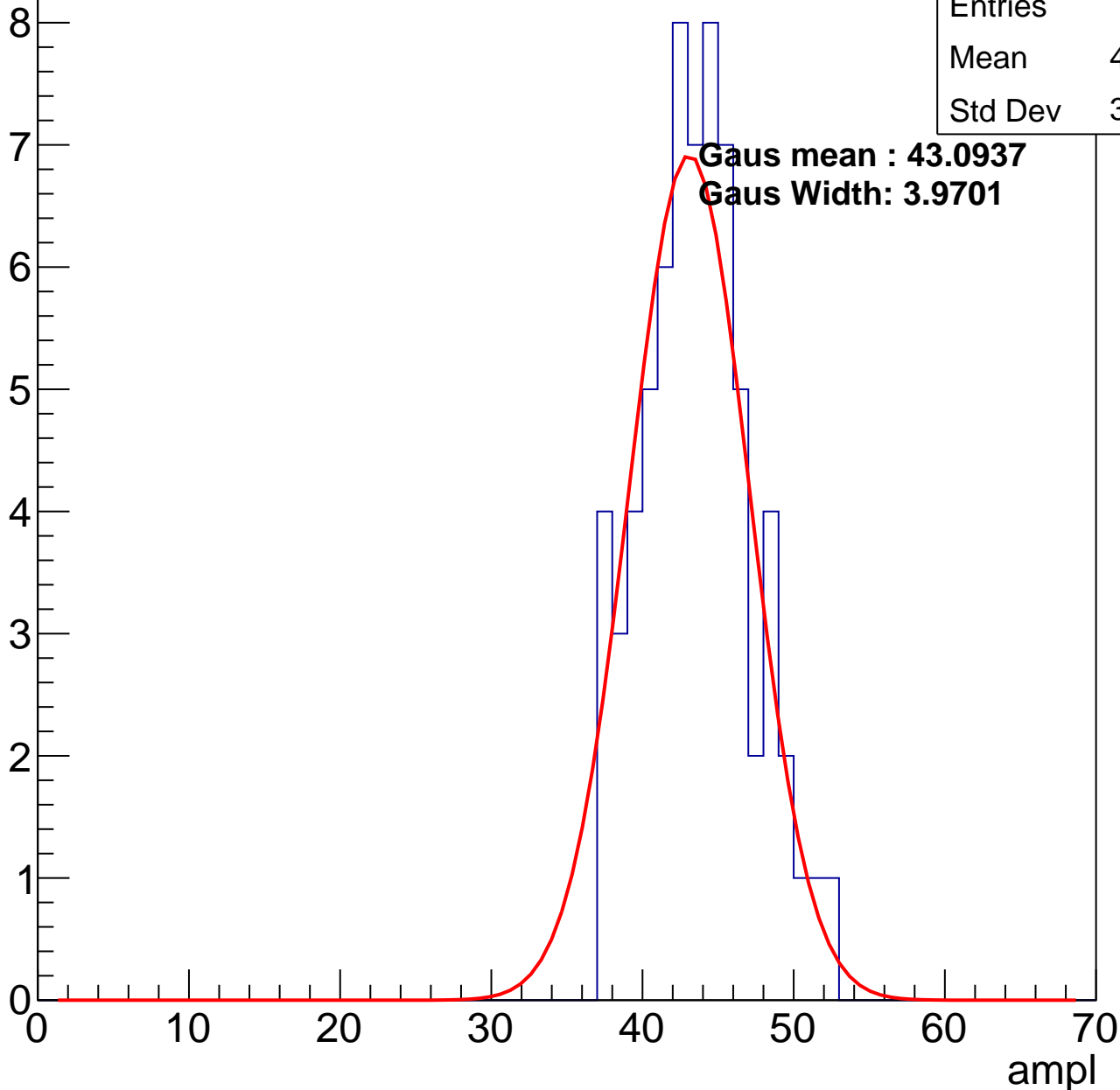
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	43.16
Std Dev	3.509

**Gaus mean : 43.0937**

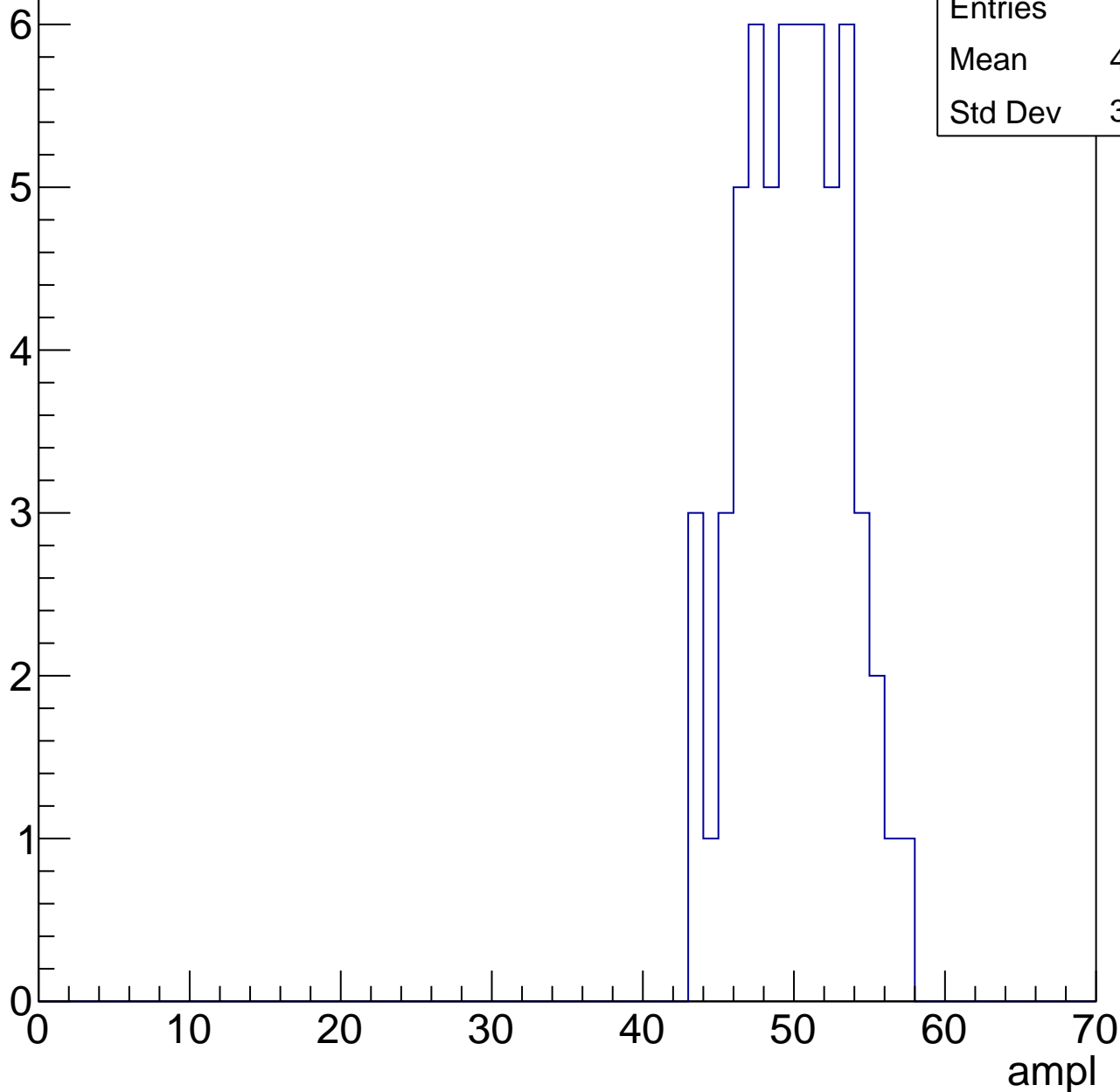
**Gaus Width: 3.9701**



# B1L102S, U5-ch62, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

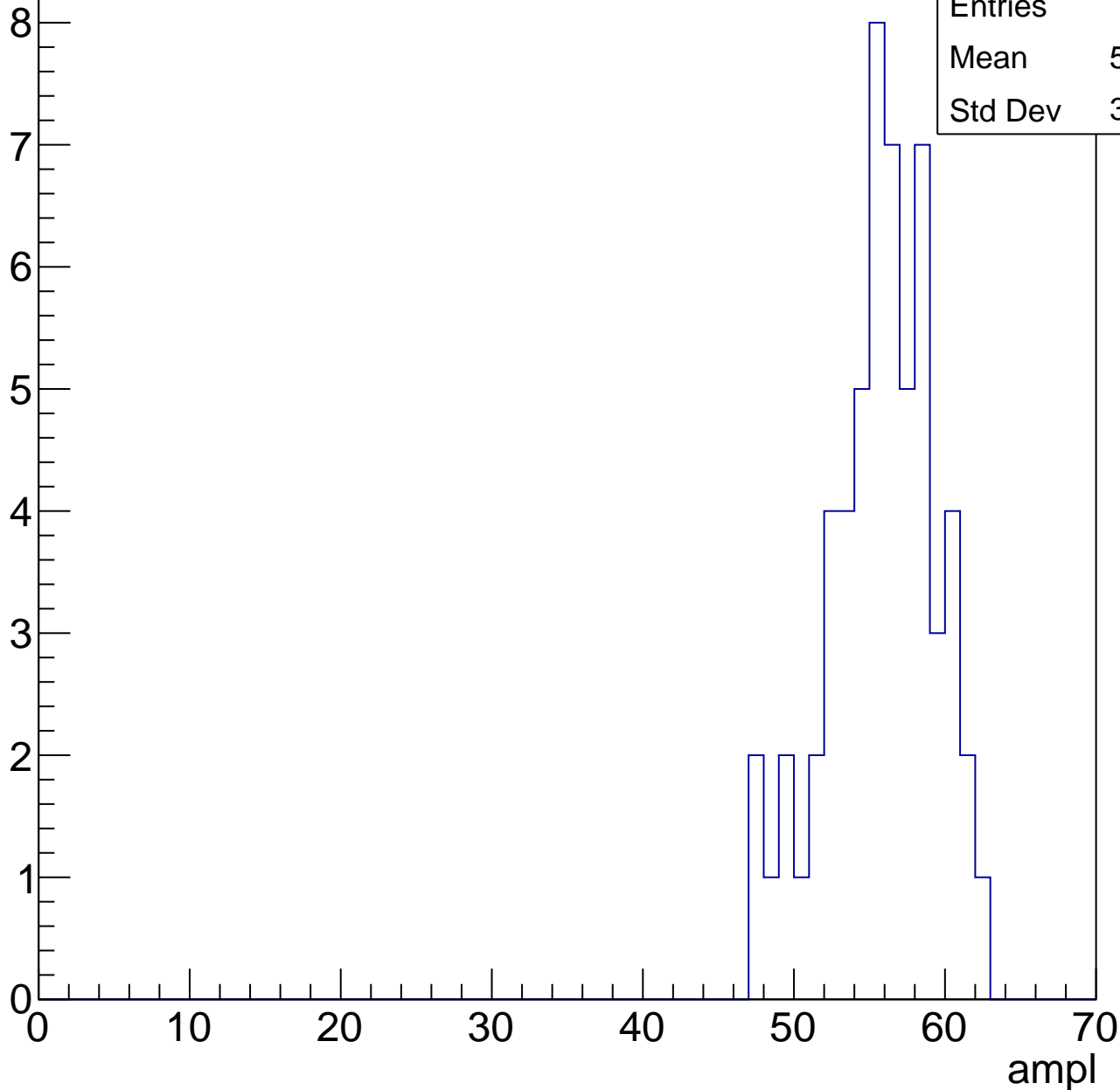


Entries	59
Mean	49.54
Std Dev	3.366

# B1L102S, U5-ch62, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

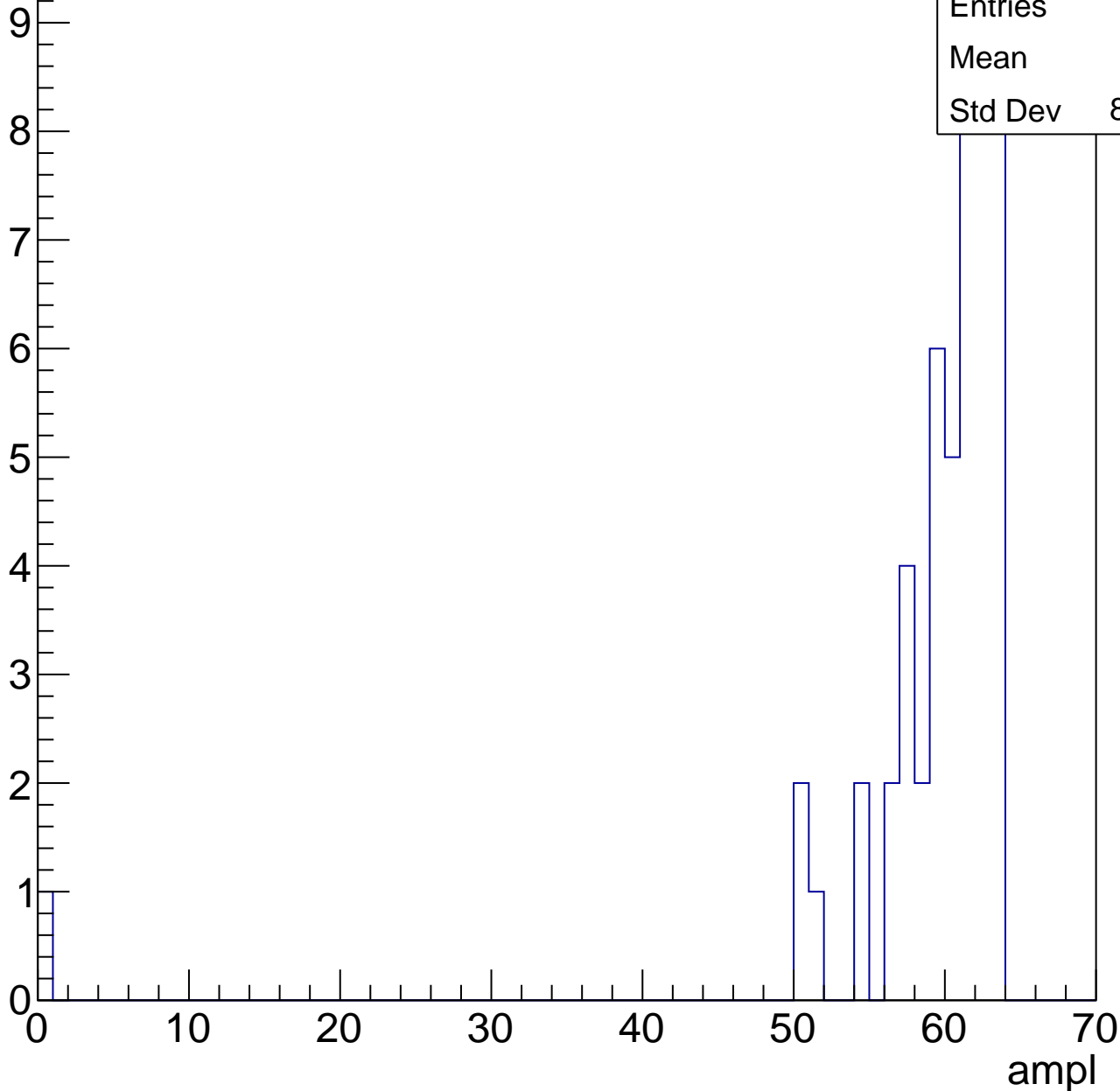


# B1L102S, U5-ch62, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	58.4
Std Dev	8.976



# B1L102S, U5-ch62, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries	5
Mean	60.4
Std Dev	1.855



# B1L102S, U5-ch62, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U5-ch63, adc0

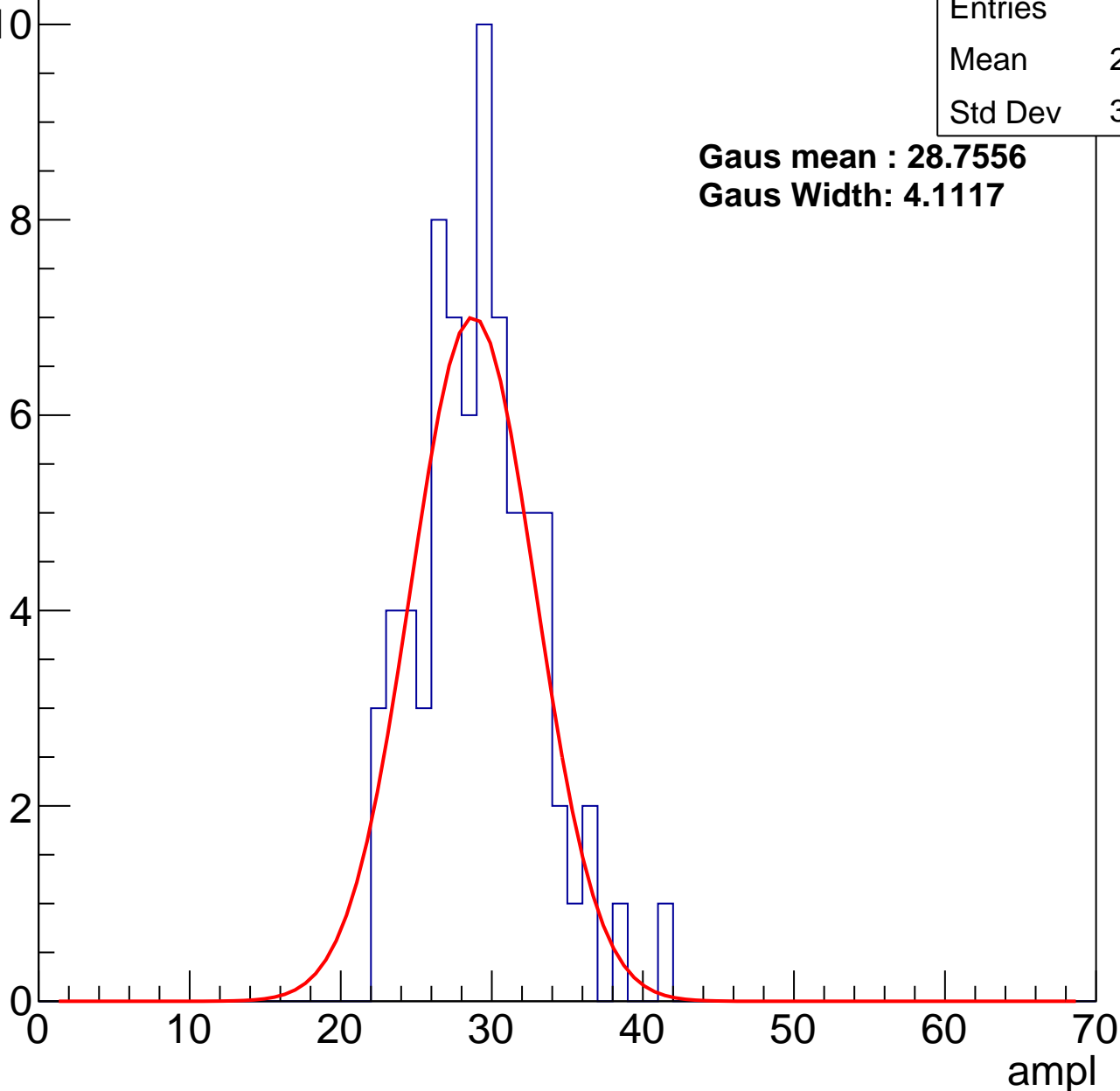
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	28.76
Std Dev	3.858

**Gaus mean : 28.7556**

**Gaus Width: 4.1117**



# B1L102S, U5-ch63, adc1

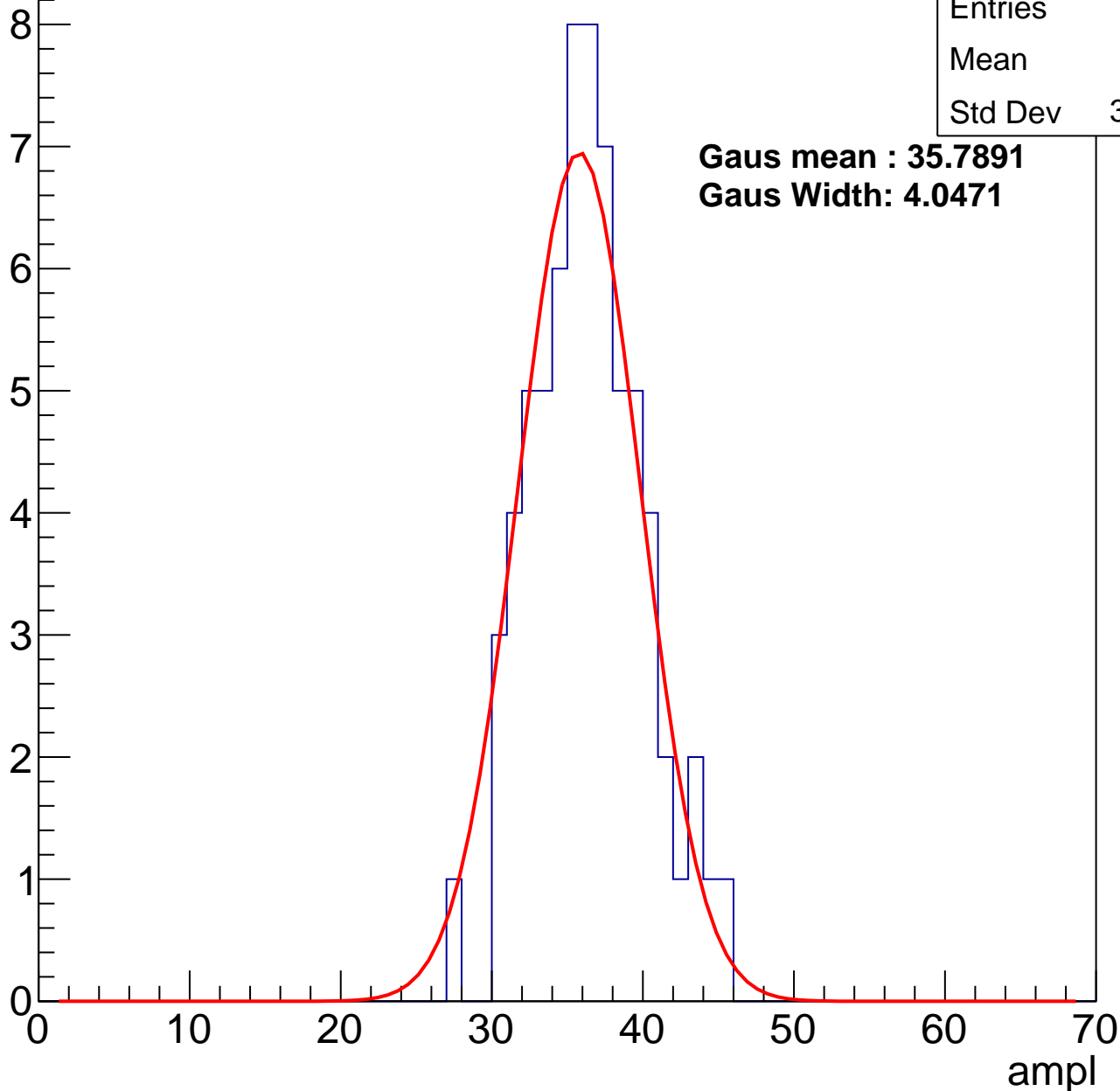
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	35.9
Std Dev	3.659

**Gaus mean : 35.7891**

**Gaus Width: 4.0471**



# B1L102S, U5-ch63, adc2

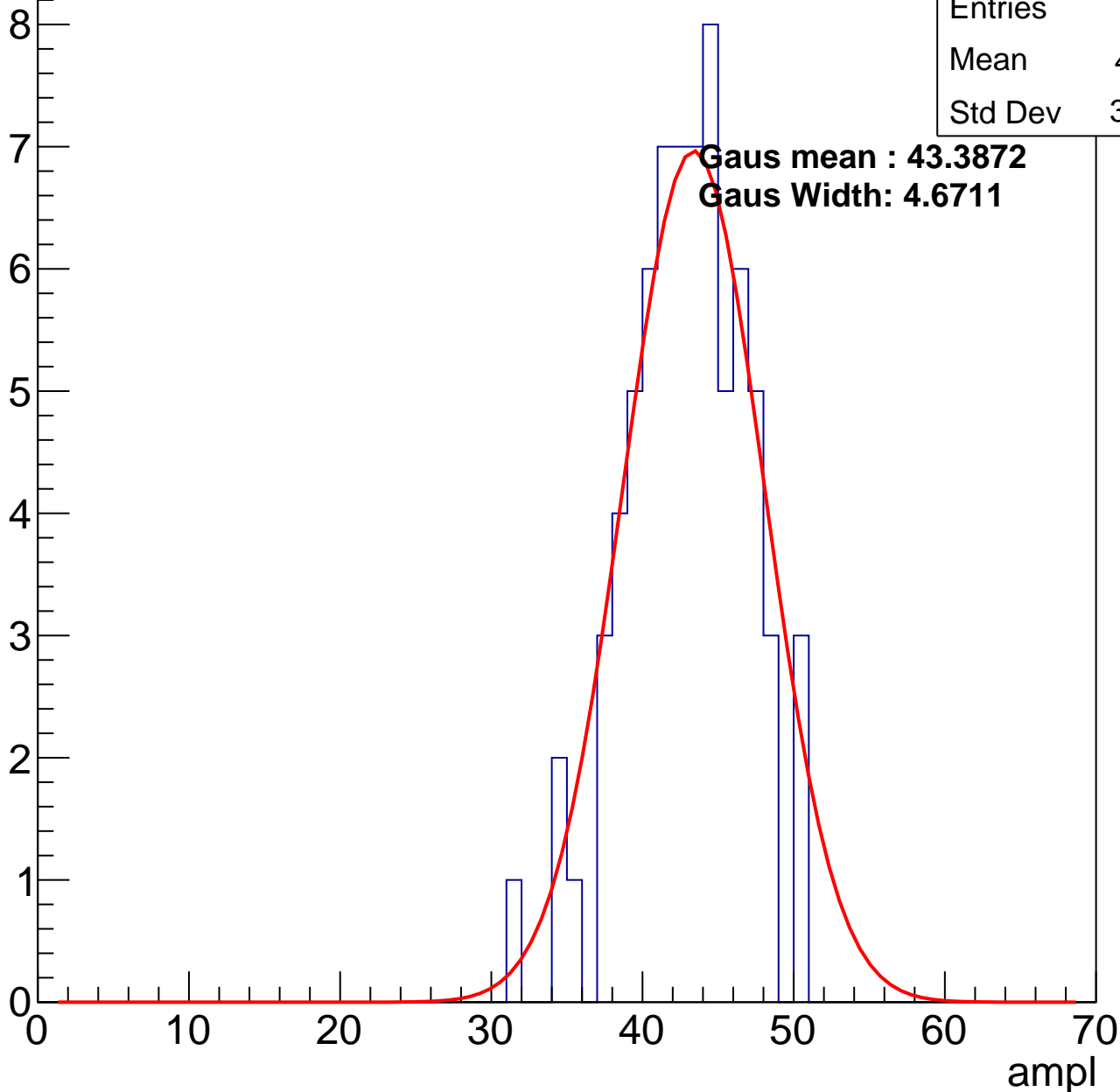
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	42.41
Std Dev	3.892

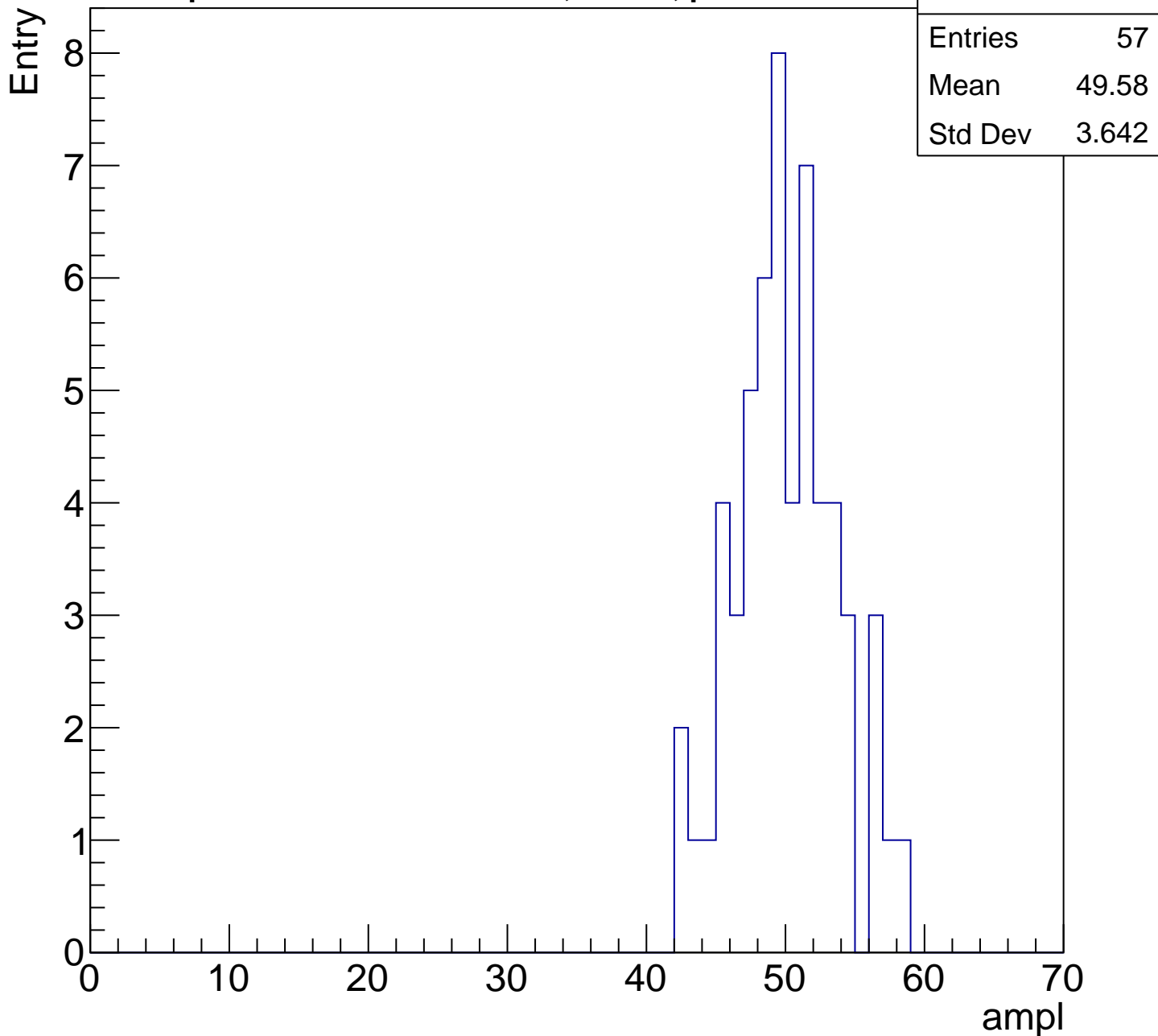
**Gaus mean : 43.3872**

**Gaus Width: 4.6711**



# B1L102S, U5-ch63, adc3

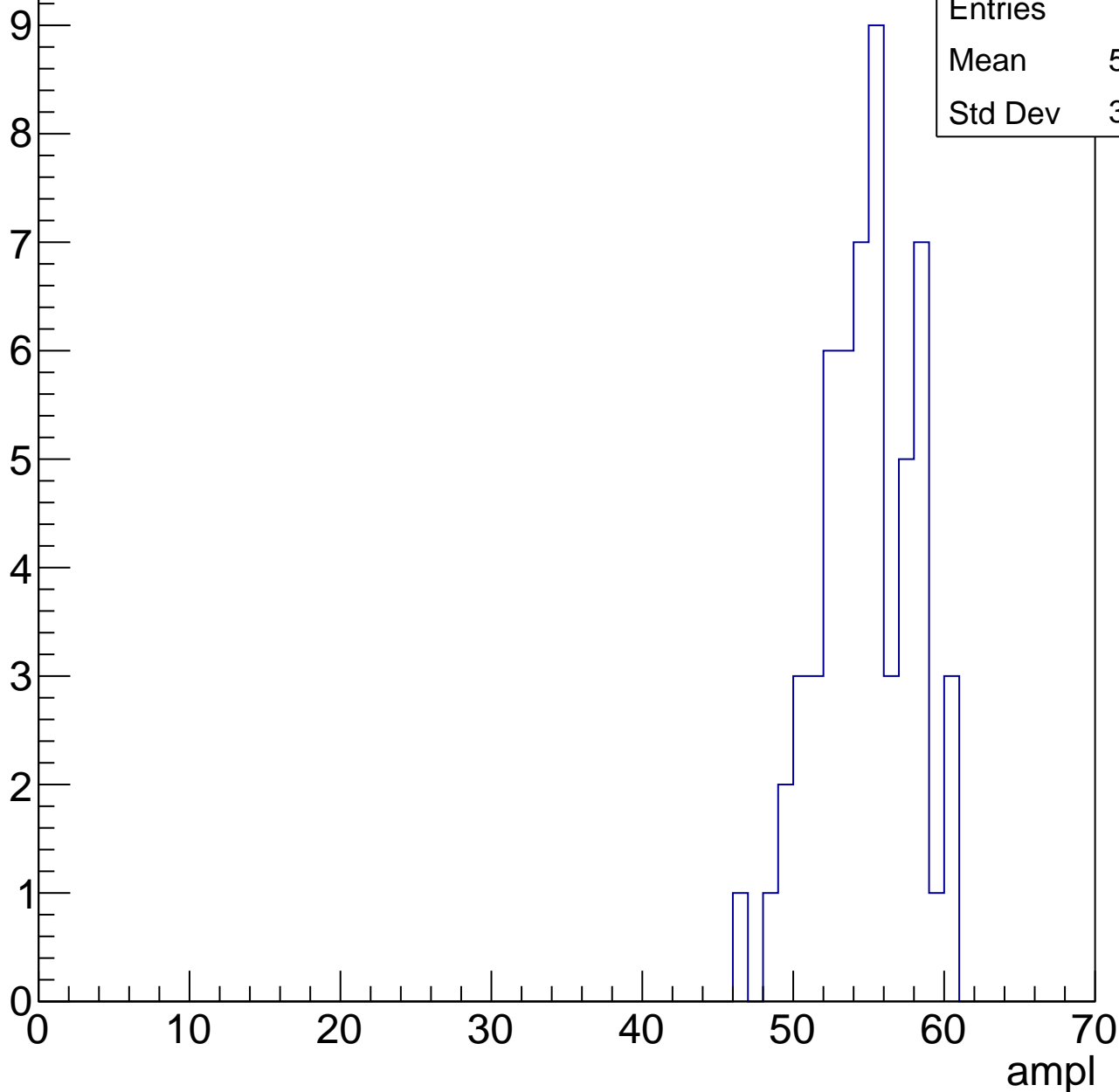
calib\_packv5\_042523\_0143.root, FC#11, port A2



# B1L102S, U5-ch63, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U5-ch63, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	48
Mean	59.85
Std Dev	2.15

ampl

0 10 20 30 40 50 60 70

0

1

2

3

4

5

6

7

8

9

# B1L102S, U5-ch63, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U5-ch63, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U5-ch64, adc0

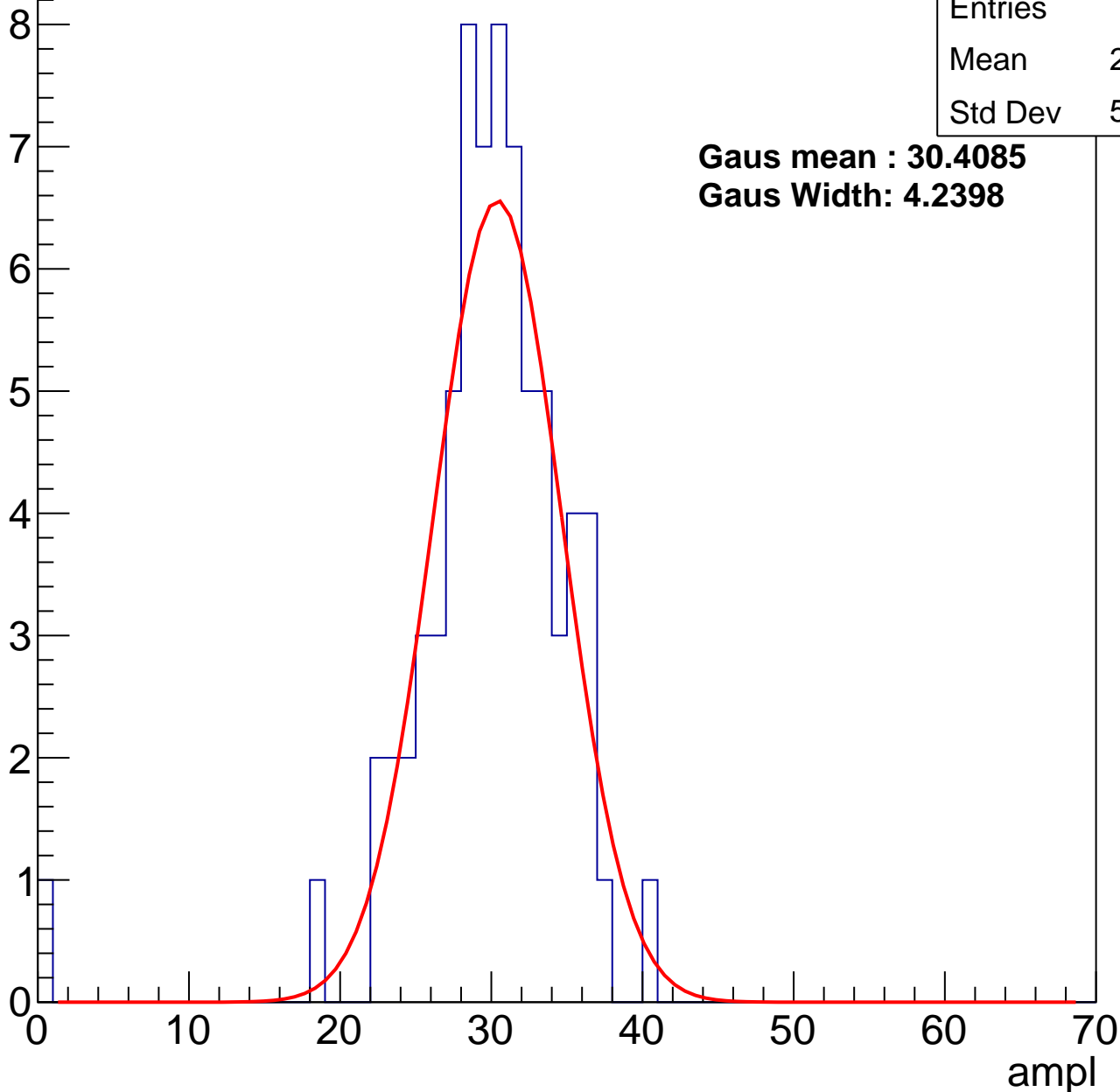
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	29.39
Std Dev	5.317

**Gaus mean : 30.4085**

**Gaus Width: 4.2398**



# B1L102S, U5-ch64, adc1

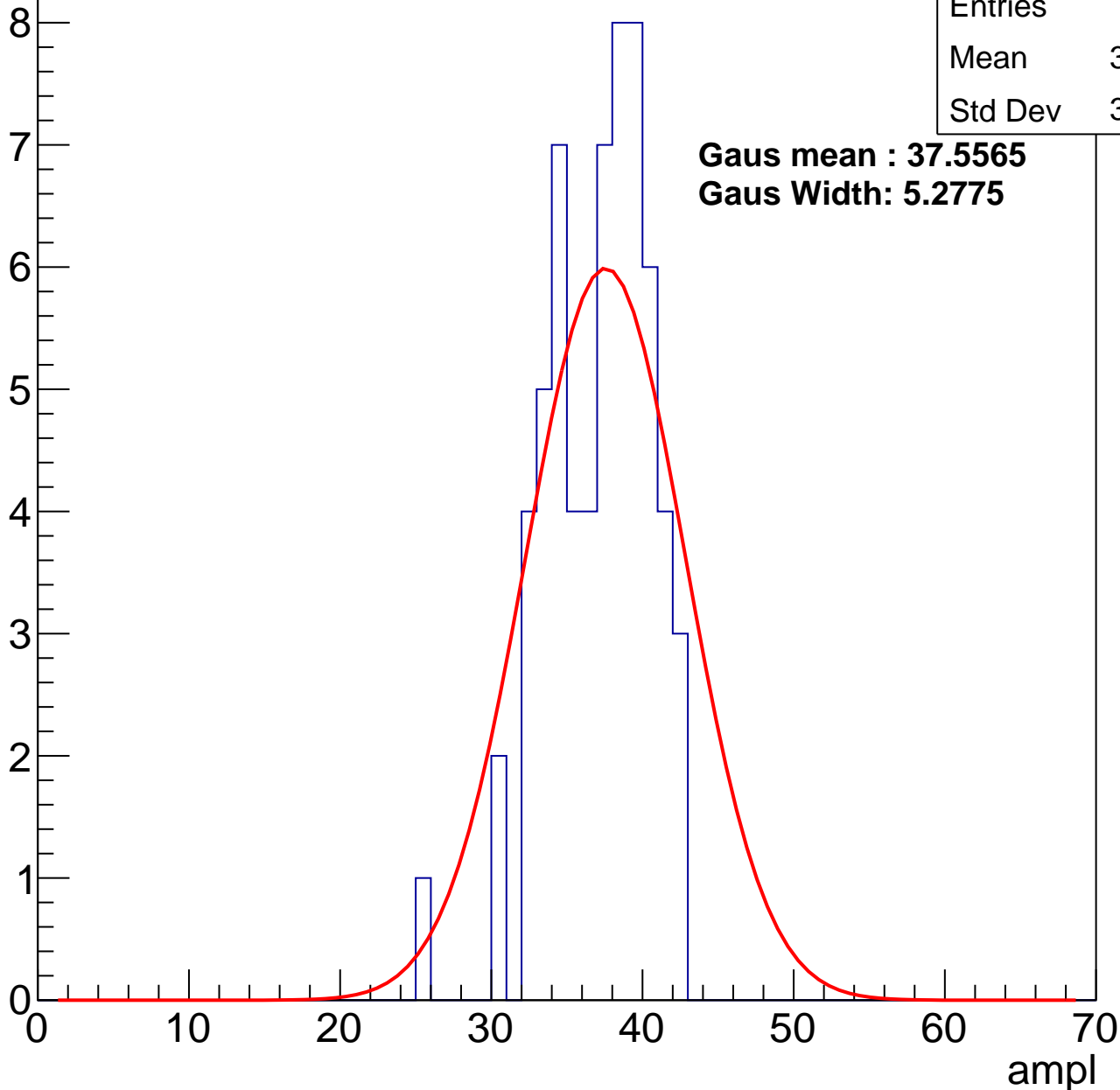
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	36.59
Std Dev	3.398

**Gaus mean : 37.5565**

**Gaus Width: 5.2775**

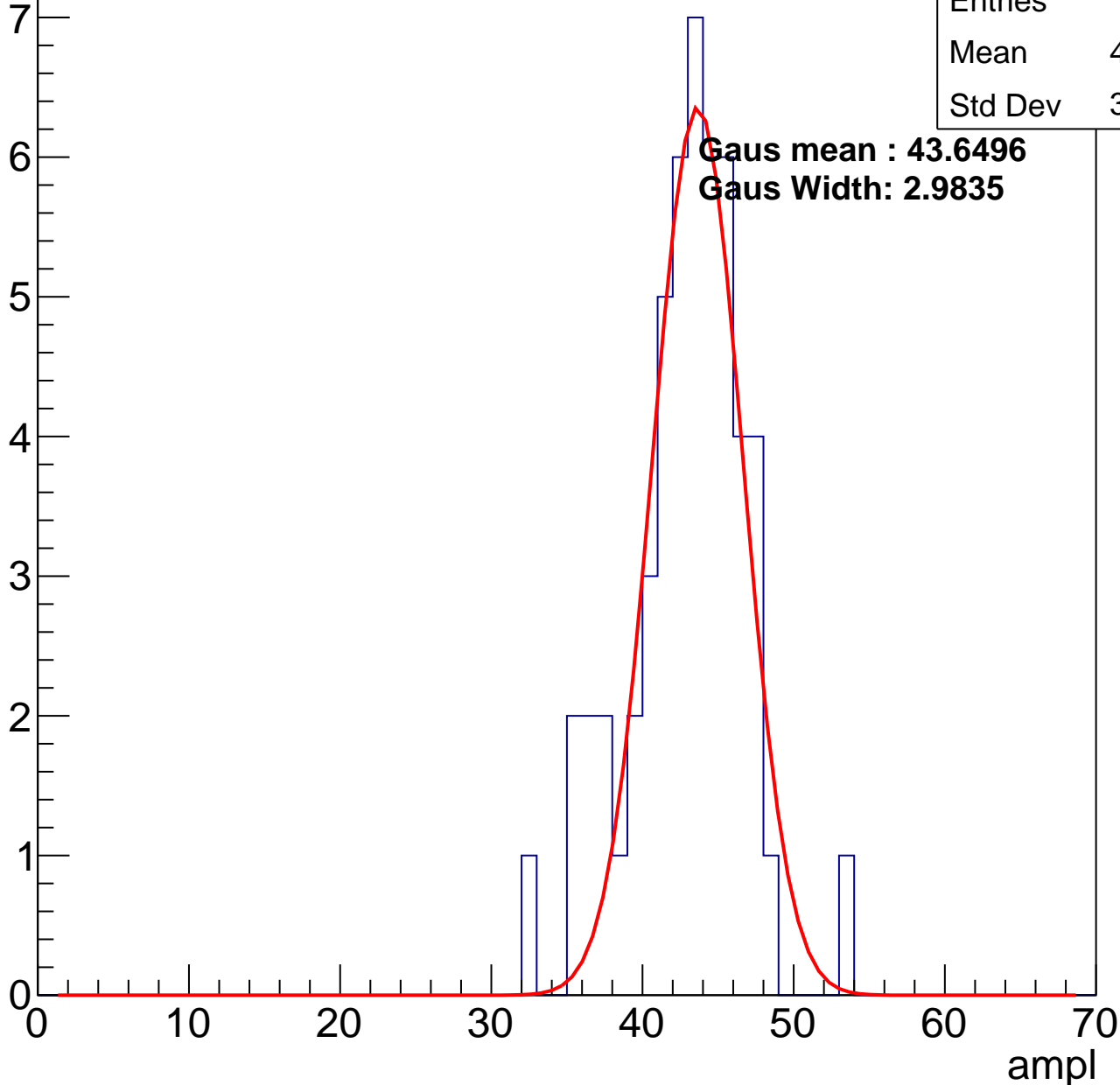


# B1L102S, U5-ch64, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

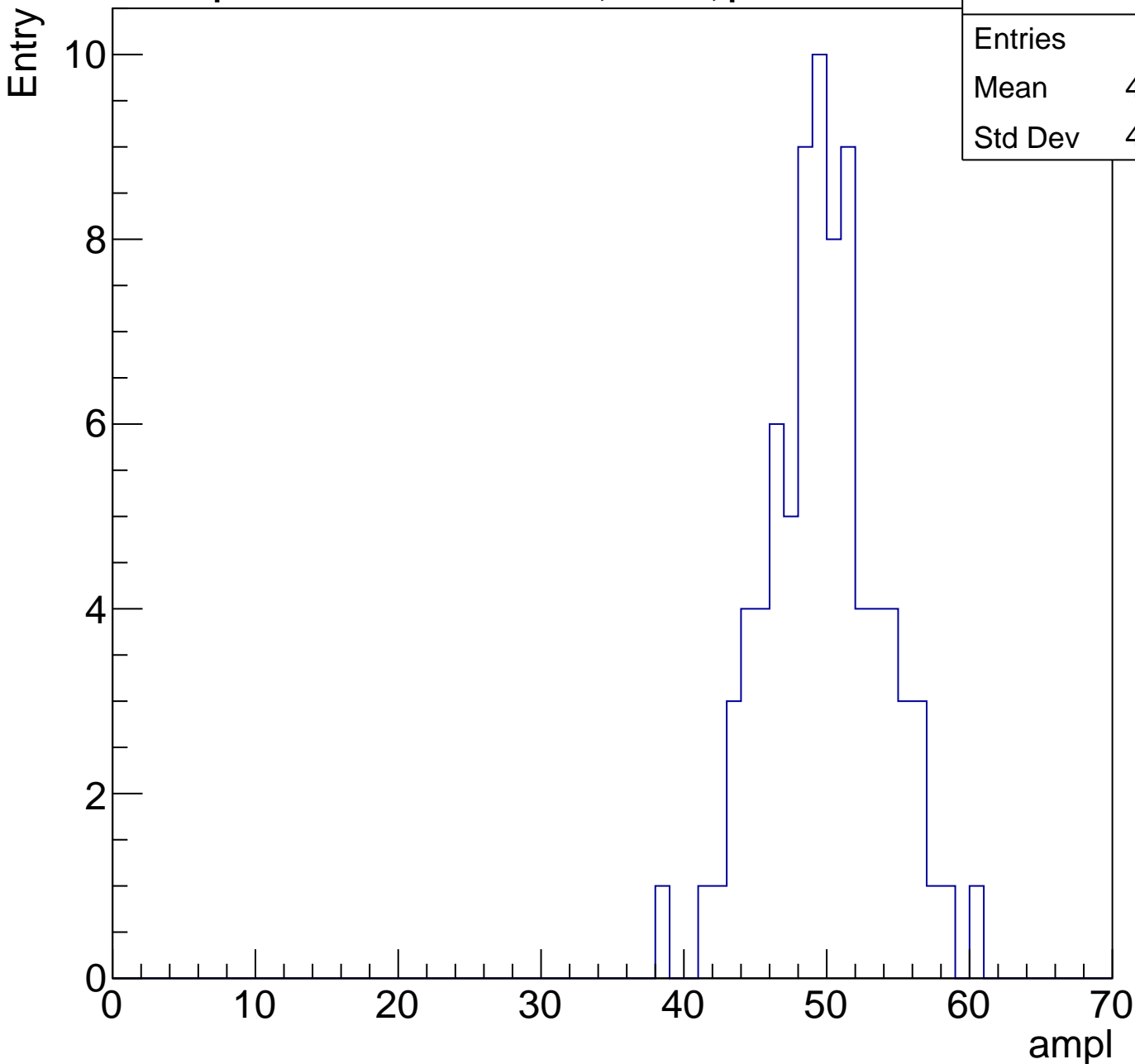
Entries	53
Mean	42.43
Std Dev	3.804



# B1L102S, U5-ch64, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	82
Mean	49.29
Std Dev	4.053

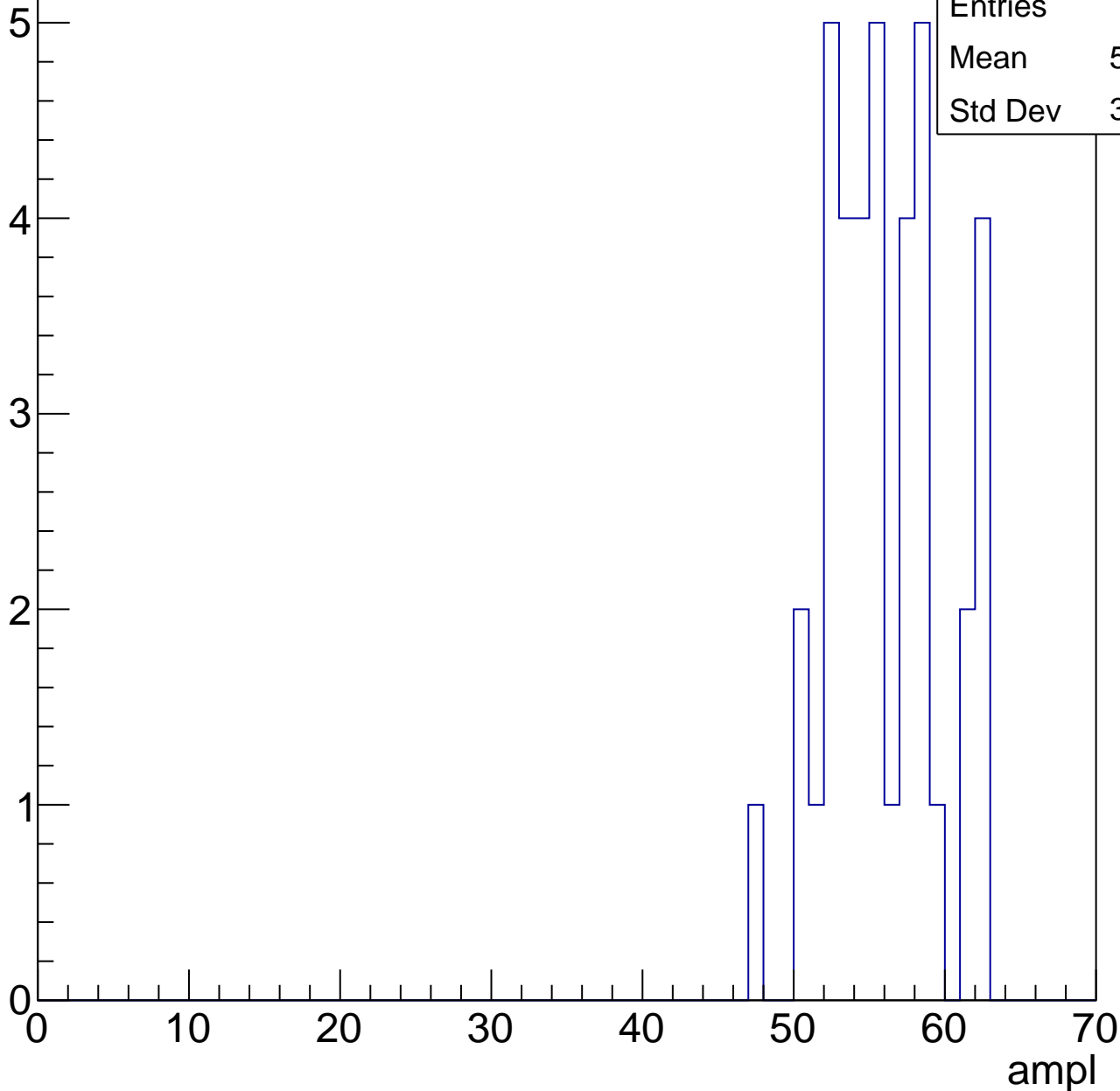


# B1L102S, U5-ch64, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	39
Mean	55.49
Std Dev	3.692

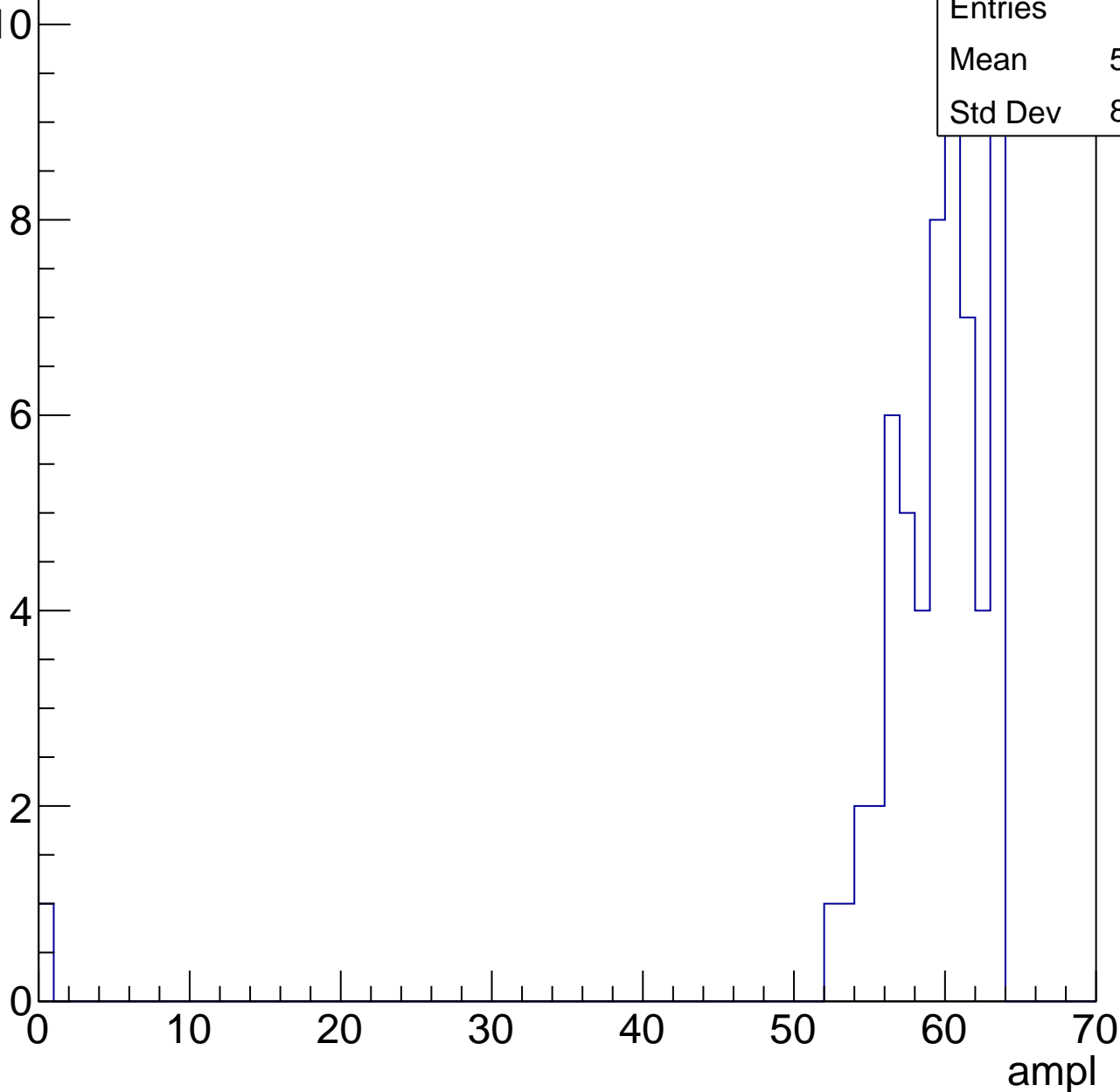


# B1L102S, U5-ch64, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

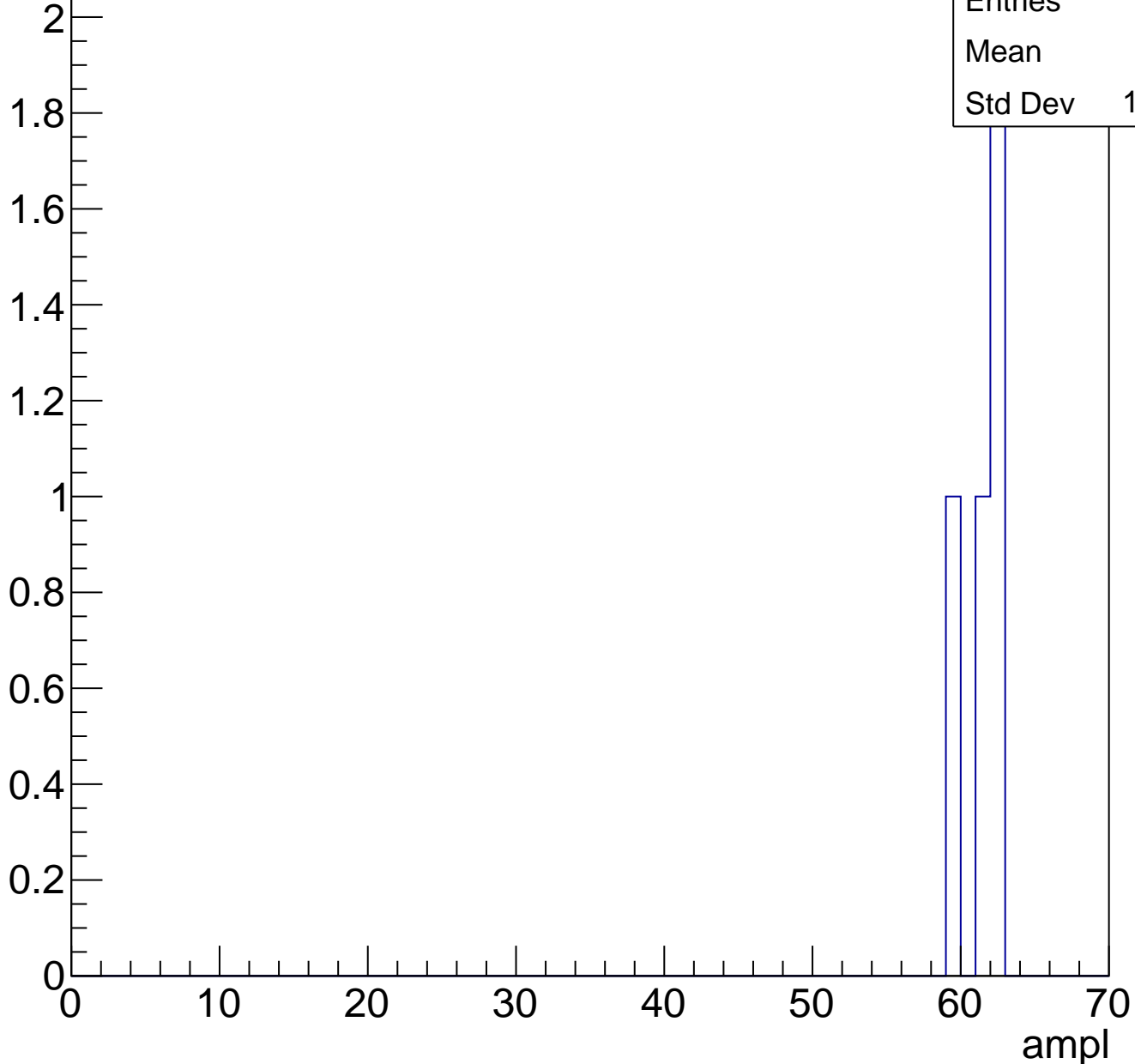
Entries	60
Mean	58.22
Std Dev	8.085



# B1L102S, U5-ch64, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U5-ch64, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L102S, U5-ch65, adc0

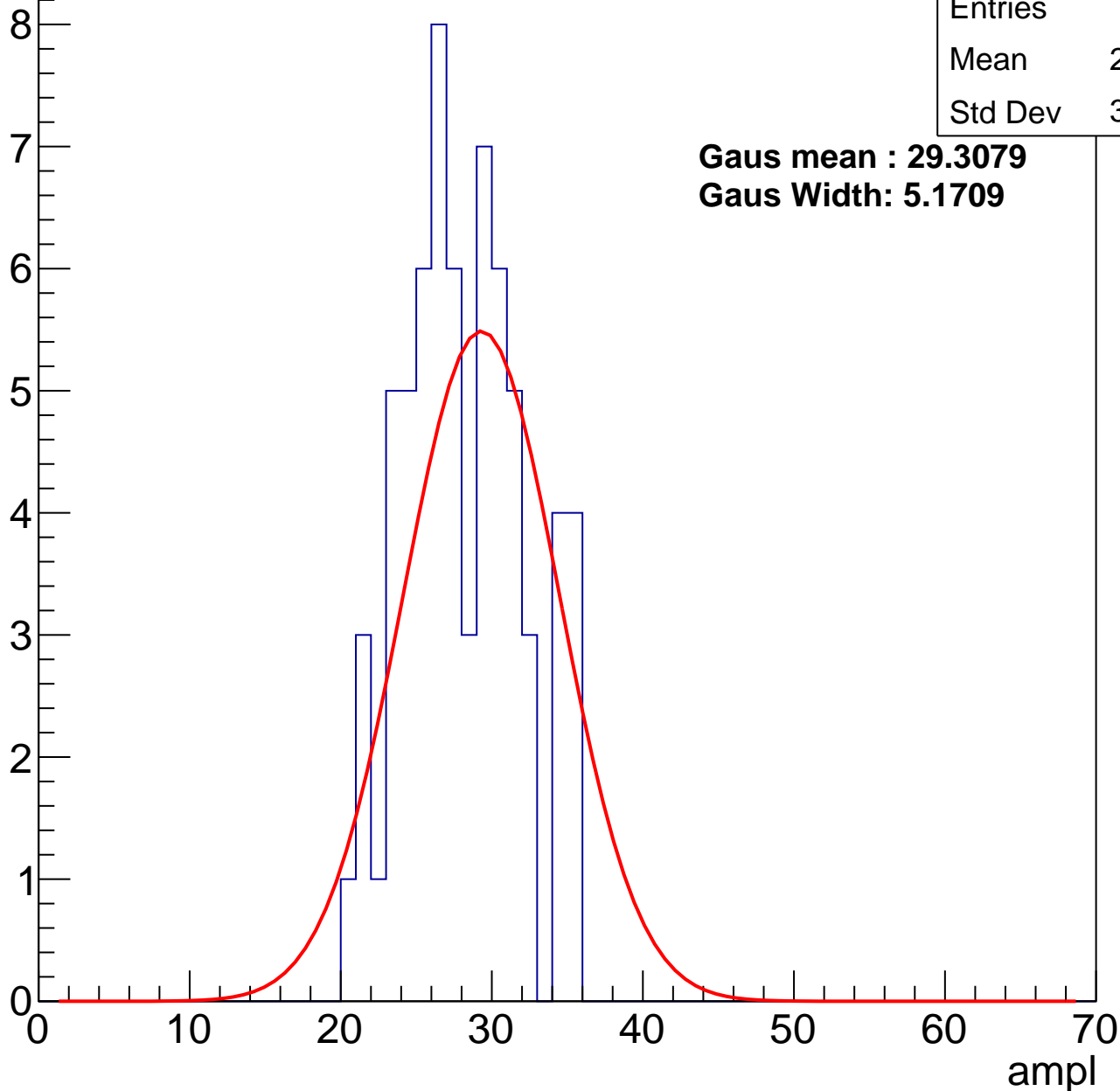
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	27.67
Std Dev	3.865

**Gaus mean : 29.3079**

**Gaus Width: 5.1709**



# B1L102S, U5-ch65, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	60
Mean	32.95
Std Dev	3.685

**Gaus mean : 30.6022**

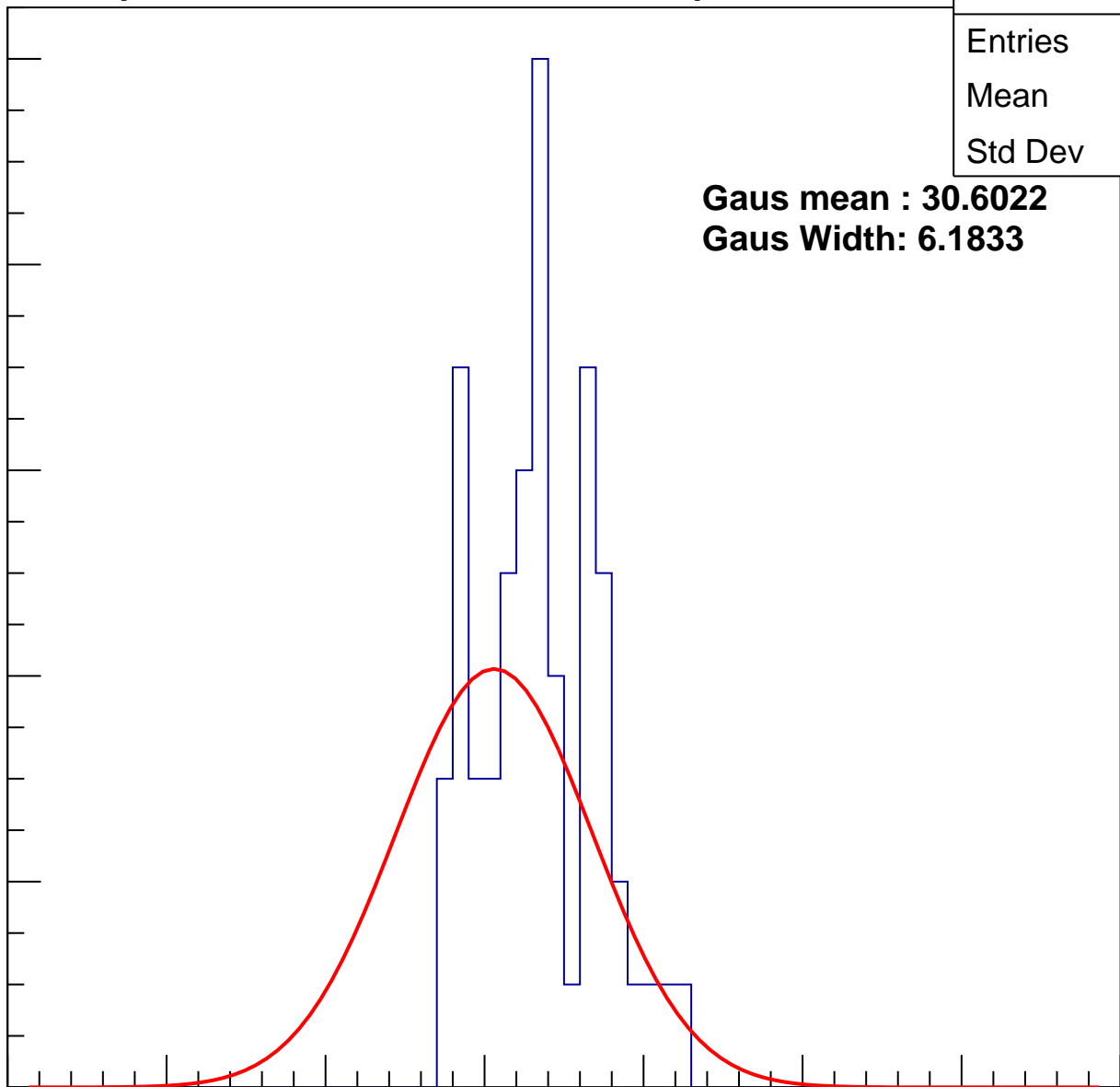
**Gaus Width: 6.1833**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U5-ch65, adc2

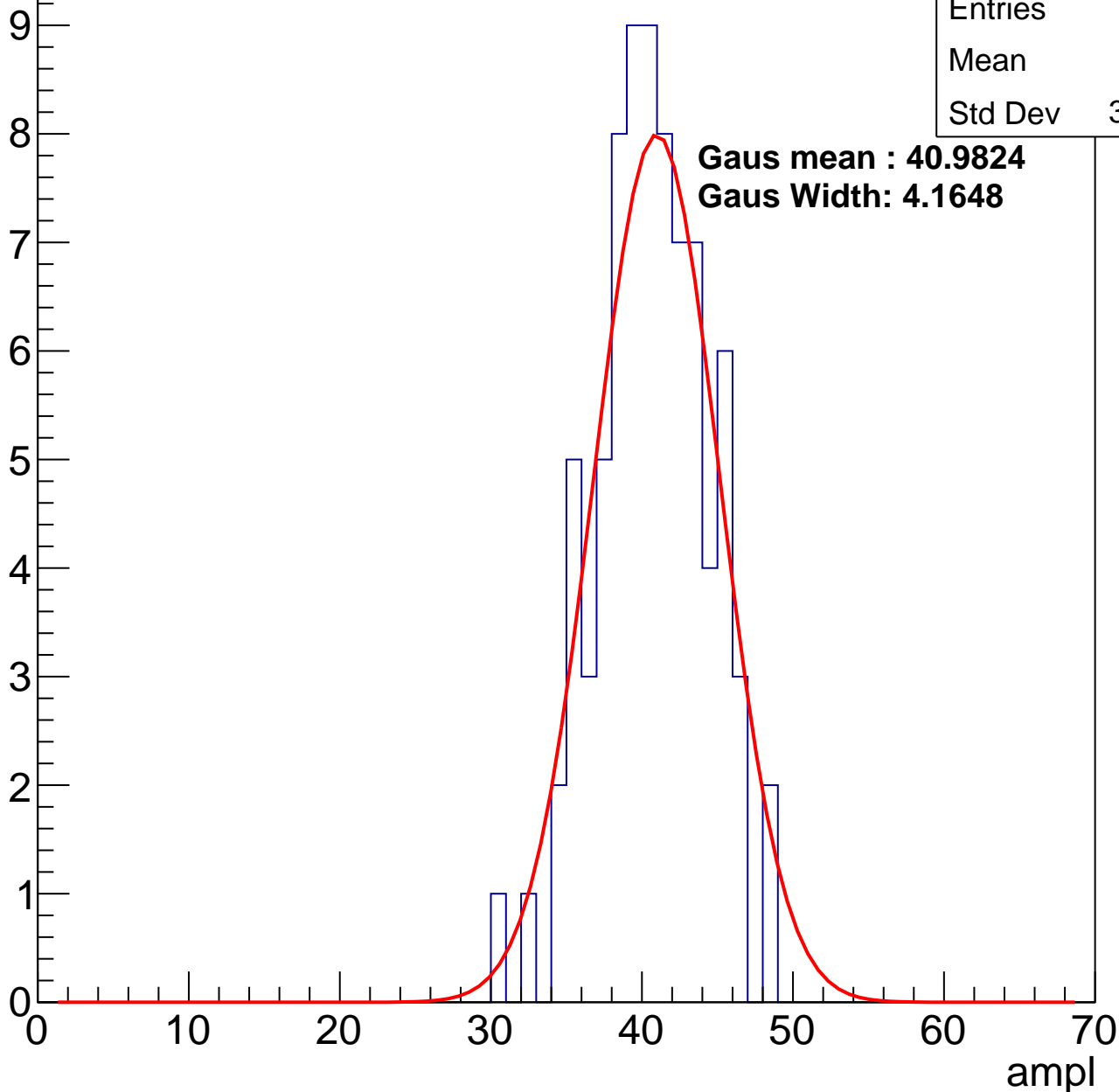
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	80
Mean	40.2
Std Dev	3.607

**Gaus mean : 40.9824**

**Gaus Width: 4.1648**

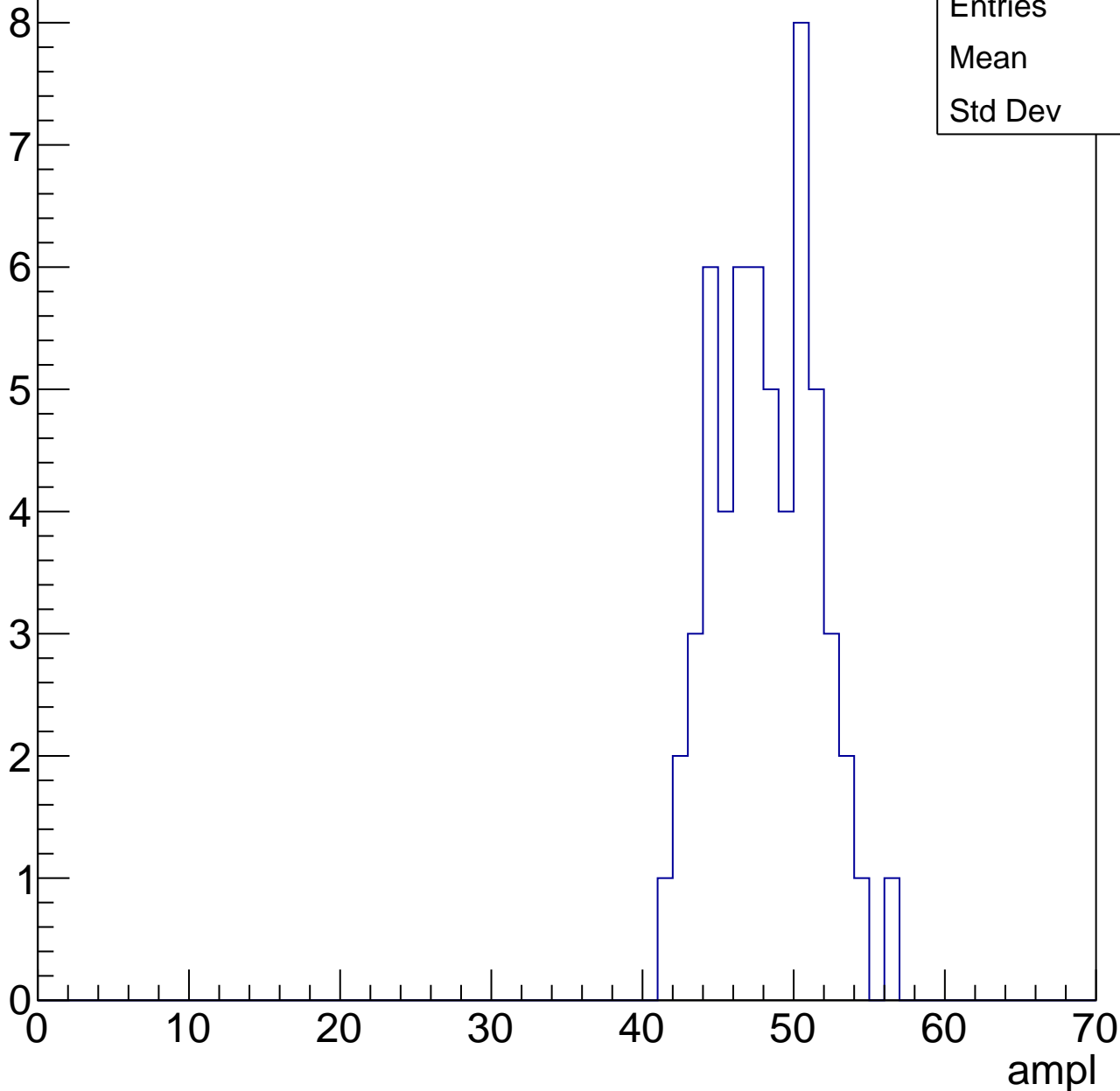


# B1L102S, U5-ch65, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	47.7
Std Dev	3.33

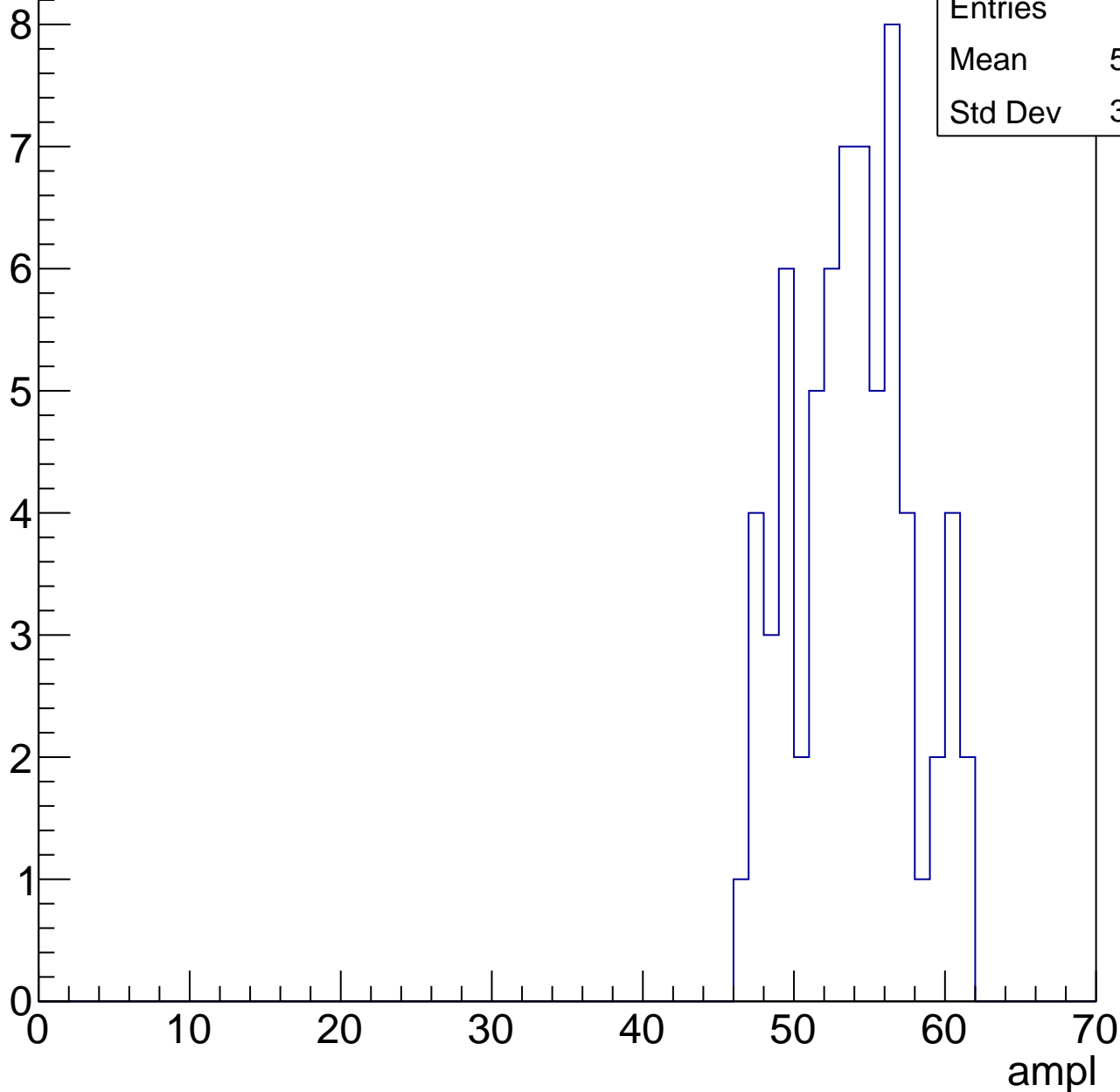


# B1L102S, U5-ch65, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

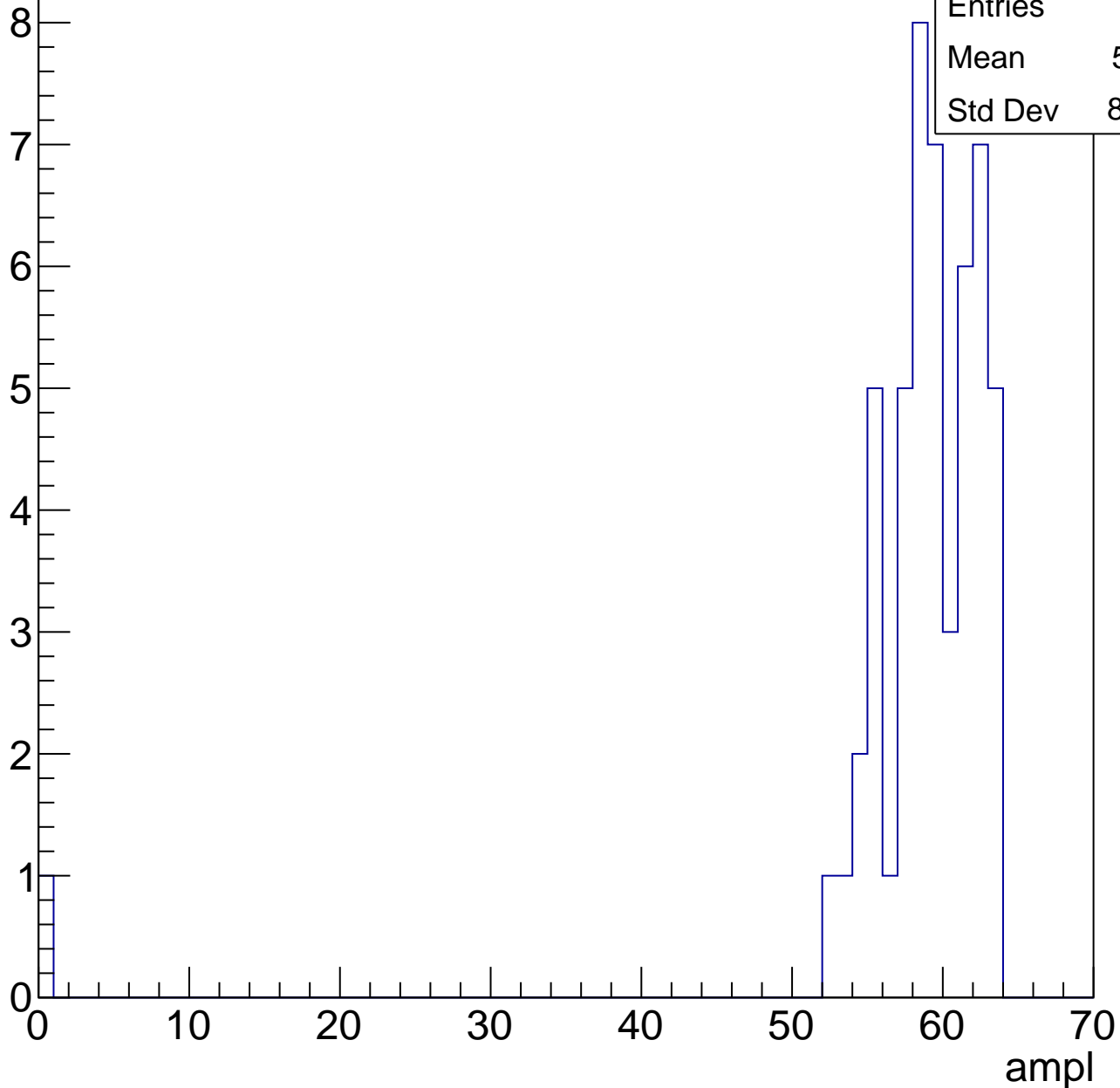
Entries	67
Mean	53.39
Std Dev	3.828



# B1L102S, U5-ch65, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

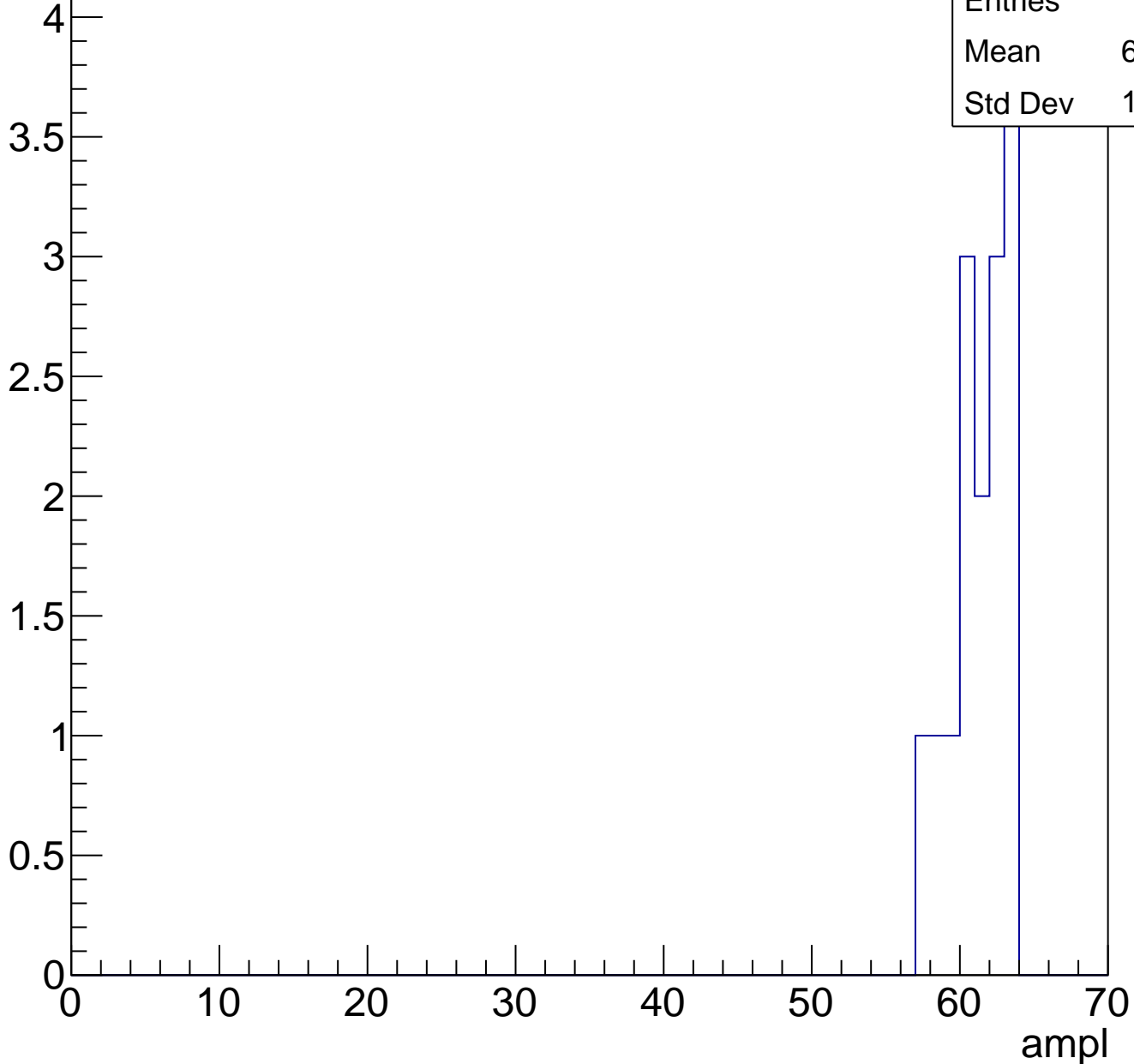
Entry



# B1L102S, U5-ch65, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

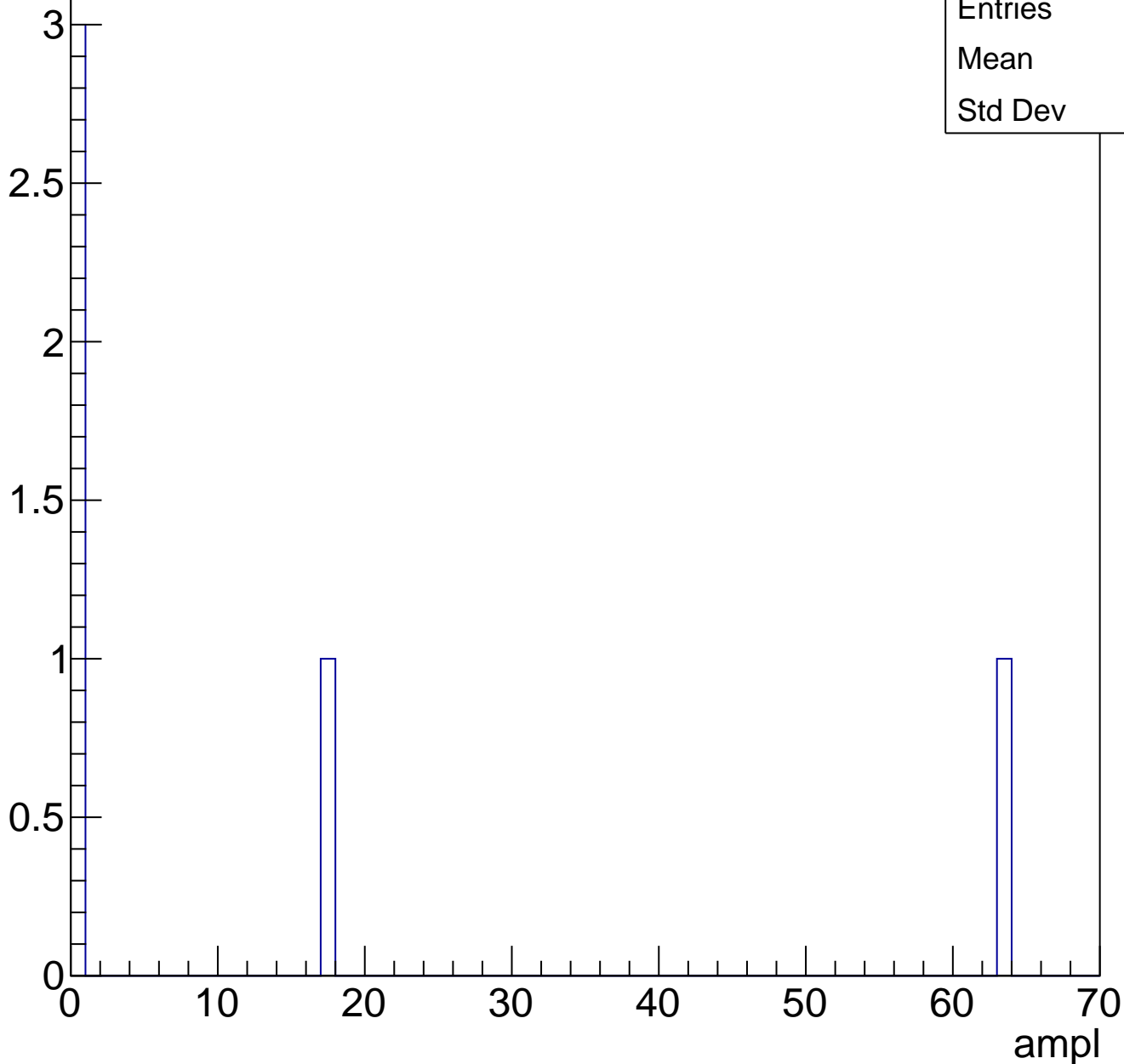




# B1L102S, U5-ch65, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	5
Mean	16
Std Dev	24.4

# B1L102S, U5-ch66, adc0

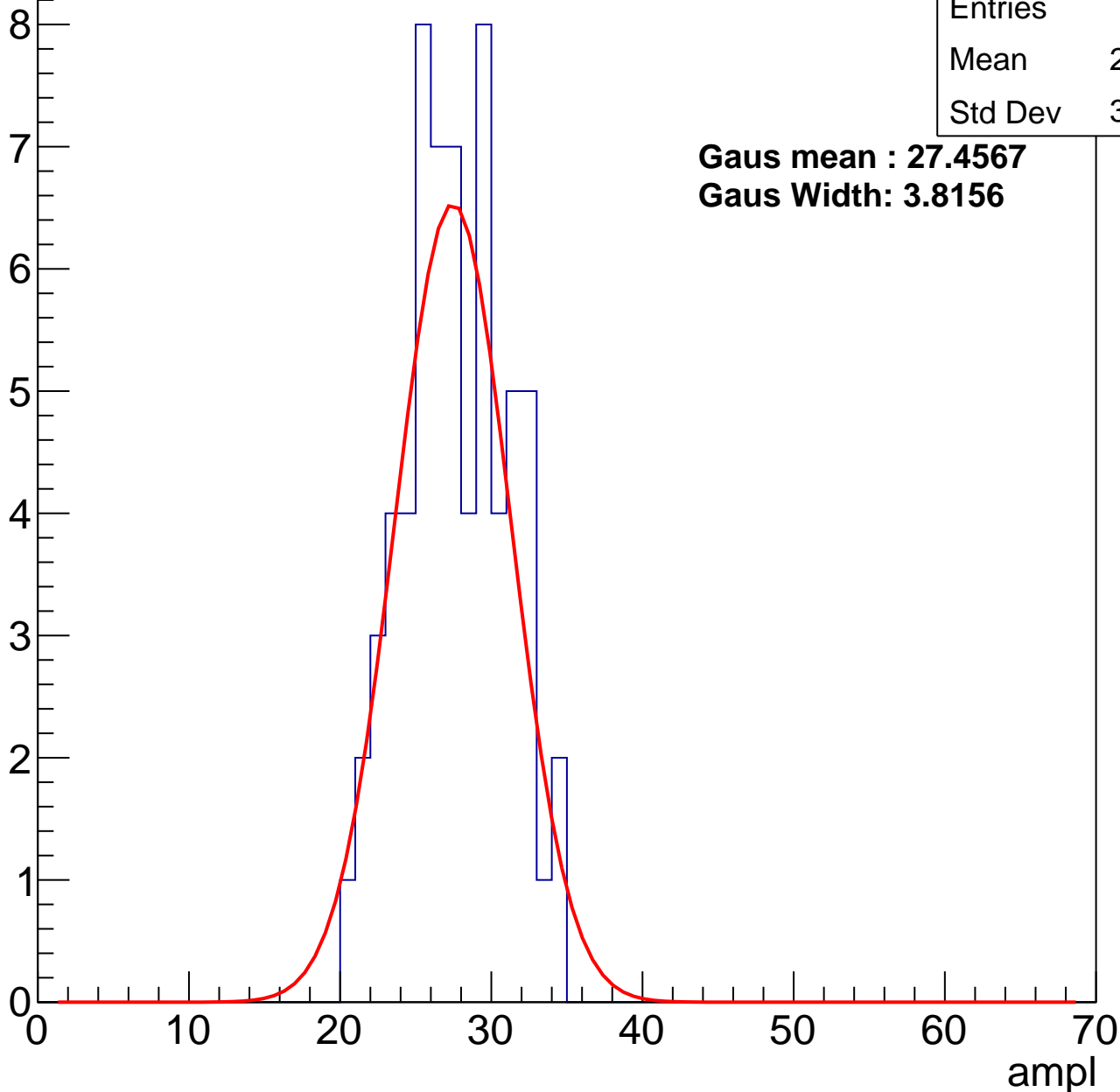
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	27.18
Std Dev	3.383

**Gaus mean : 27.4567**

**Gaus Width: 3.8156**



# B1L102S, U5-ch66, adc1

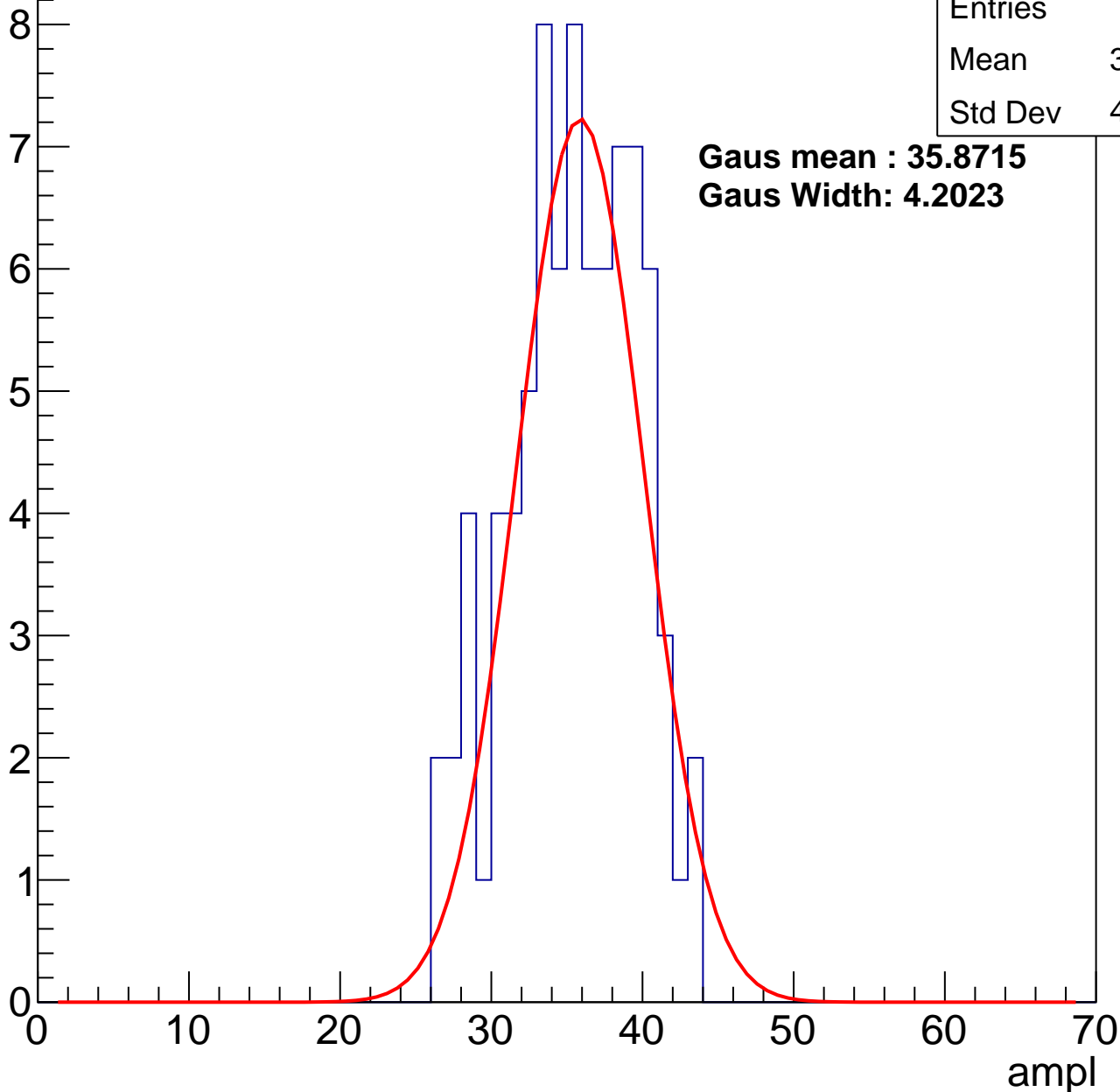
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	82
Mean	34.96
Std Dev	4.145

**Gaus mean : 35.8715**

**Gaus Width: 4.2023**



# B1L102S, U5-ch66, adc2

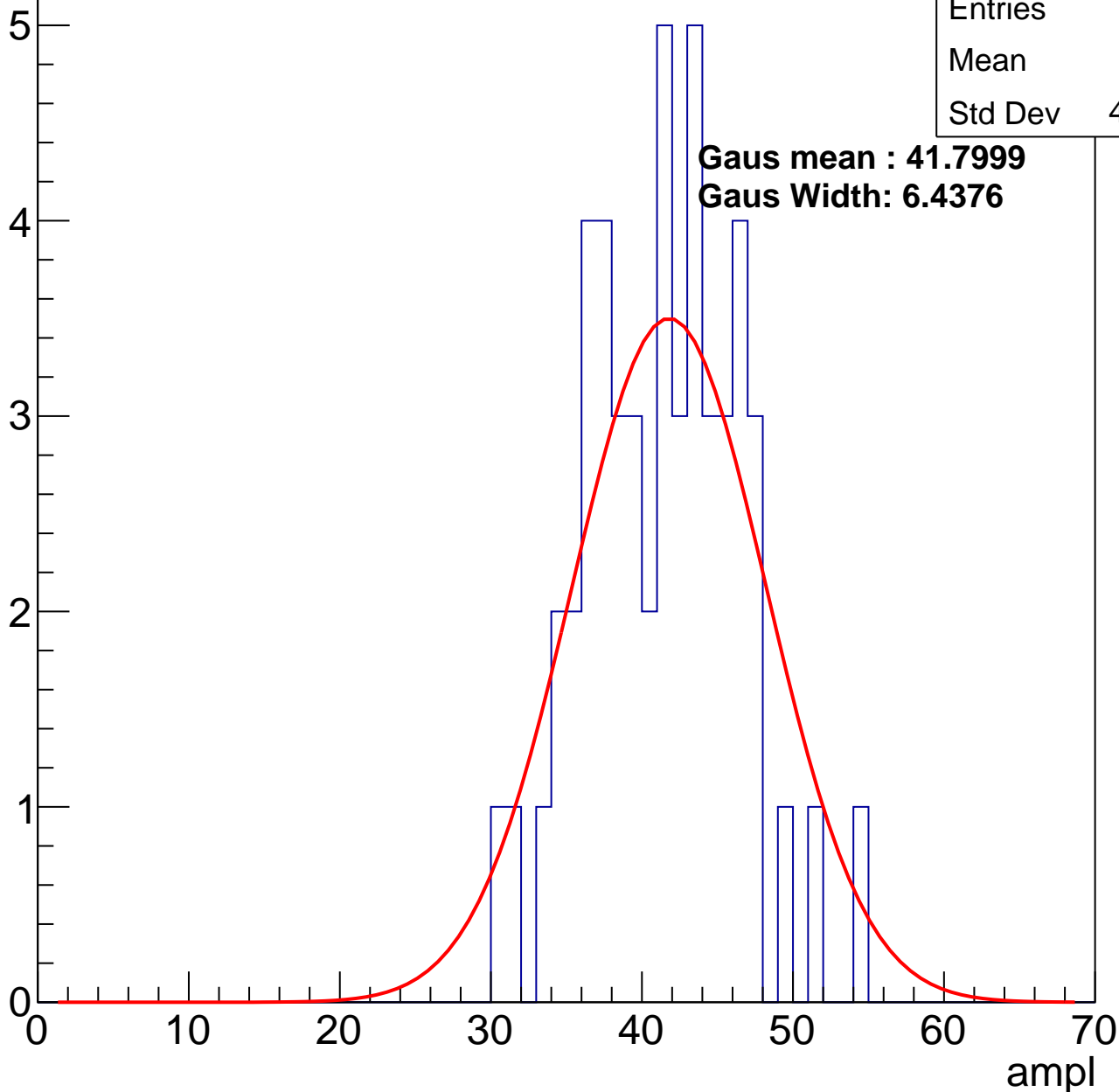
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	40.9
Std Dev	4.997

**Gaus mean : 41.7999**

**Gaus Width: 6.4376**

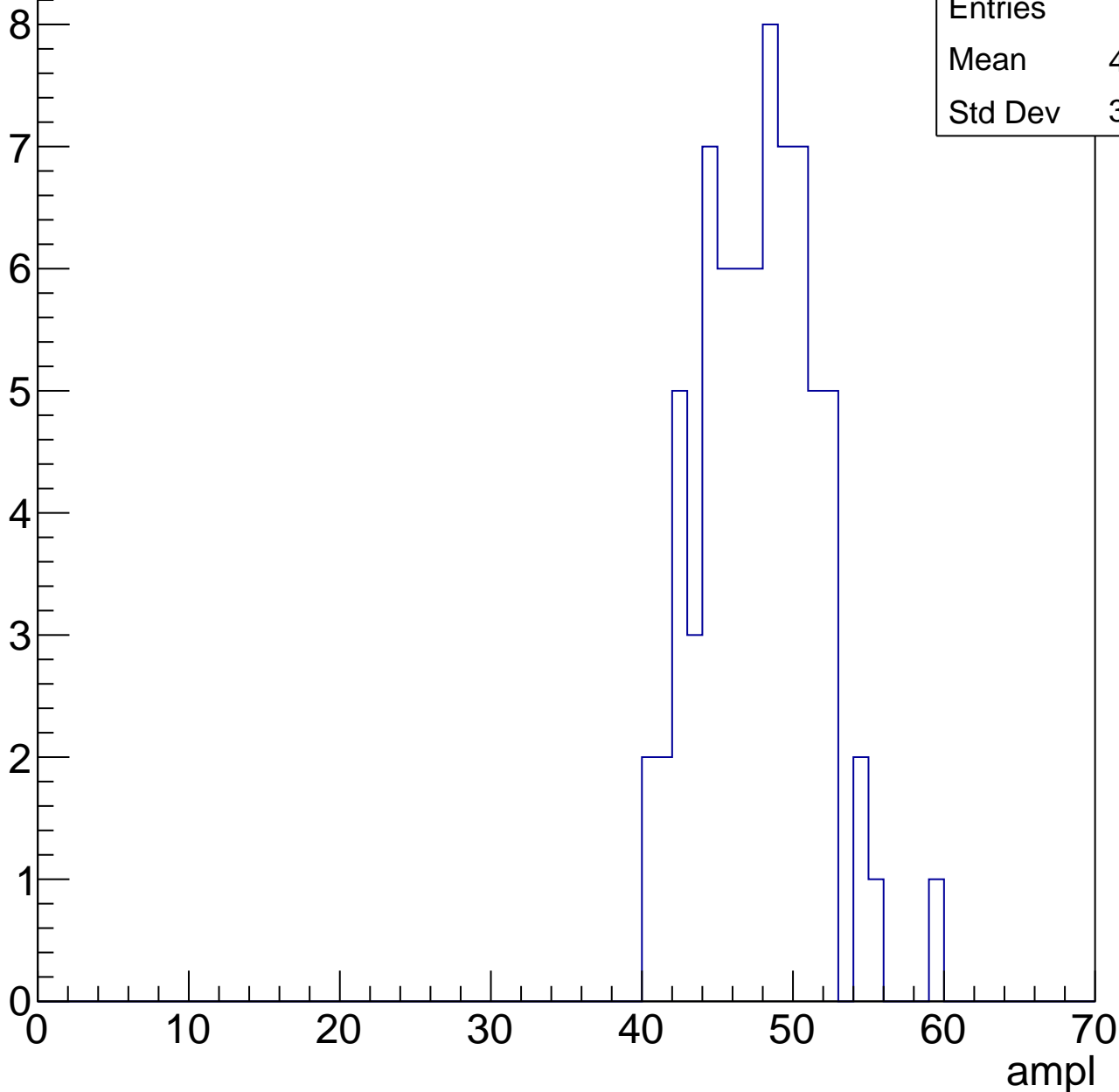


# B1L102S, U5-ch66, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

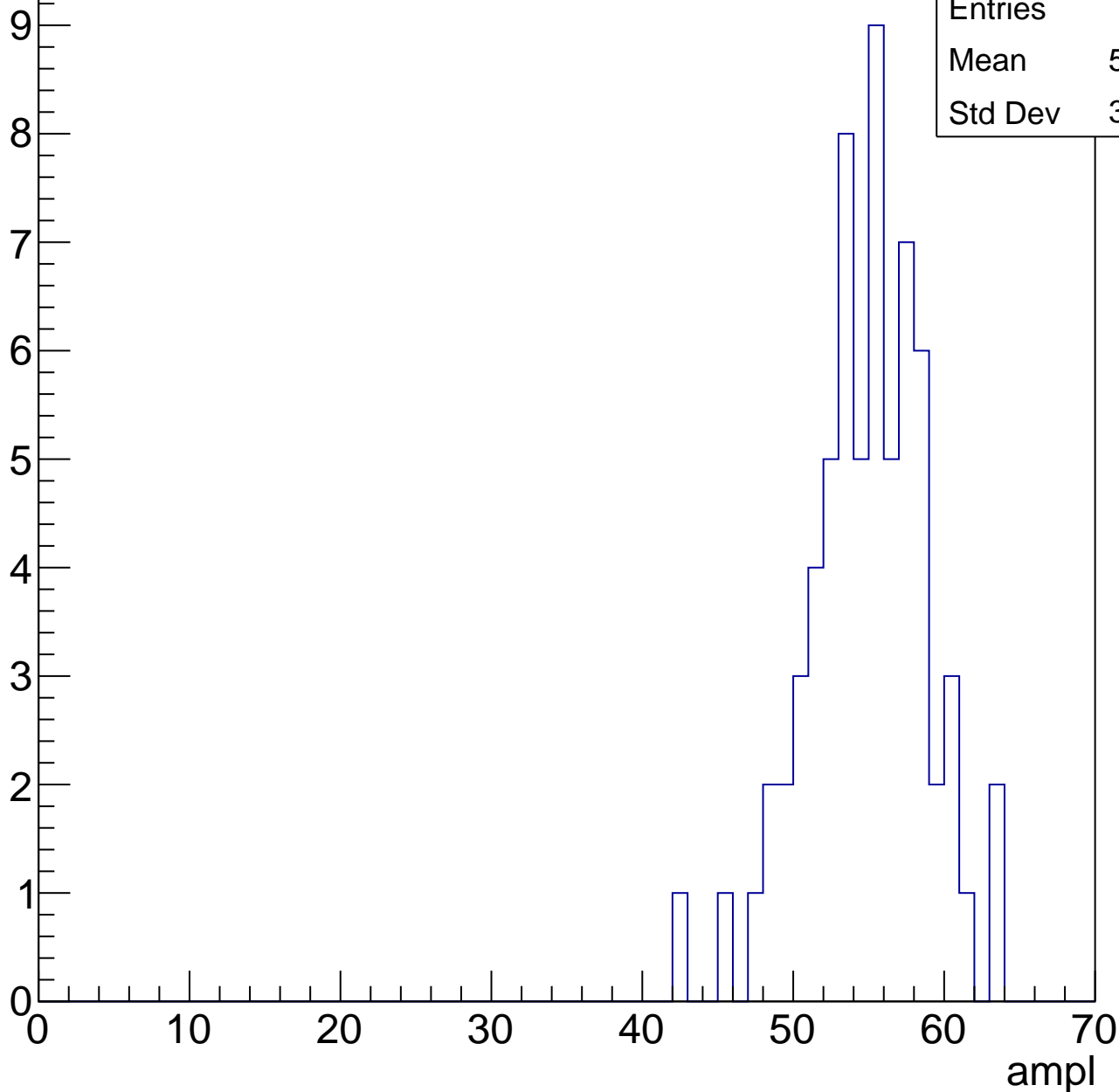
Entries	73
Mean	47.27
Std Dev	3.775



# B1L102S, U5-ch66, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

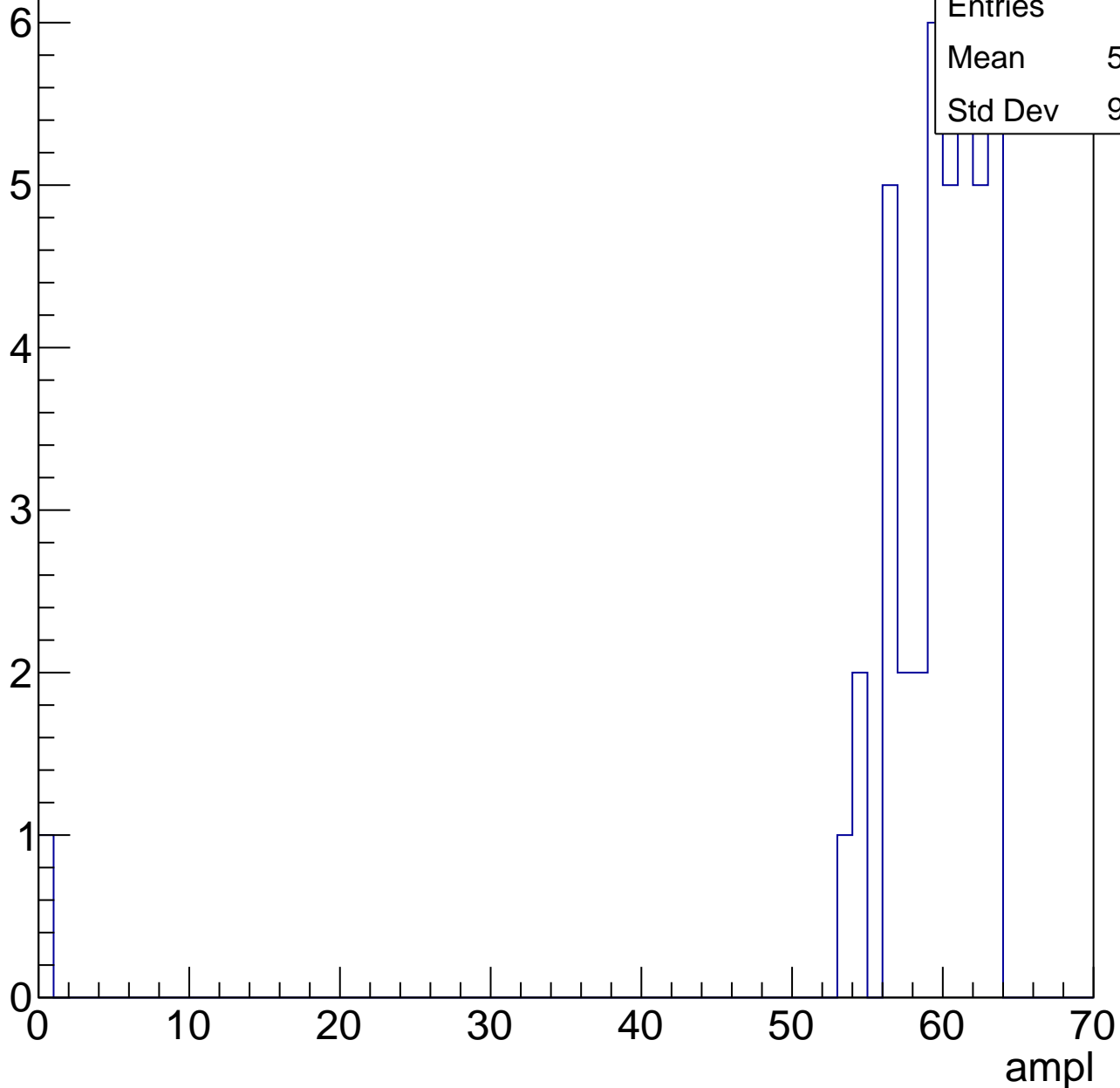
Entry



# B1L102S, U5-ch66, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

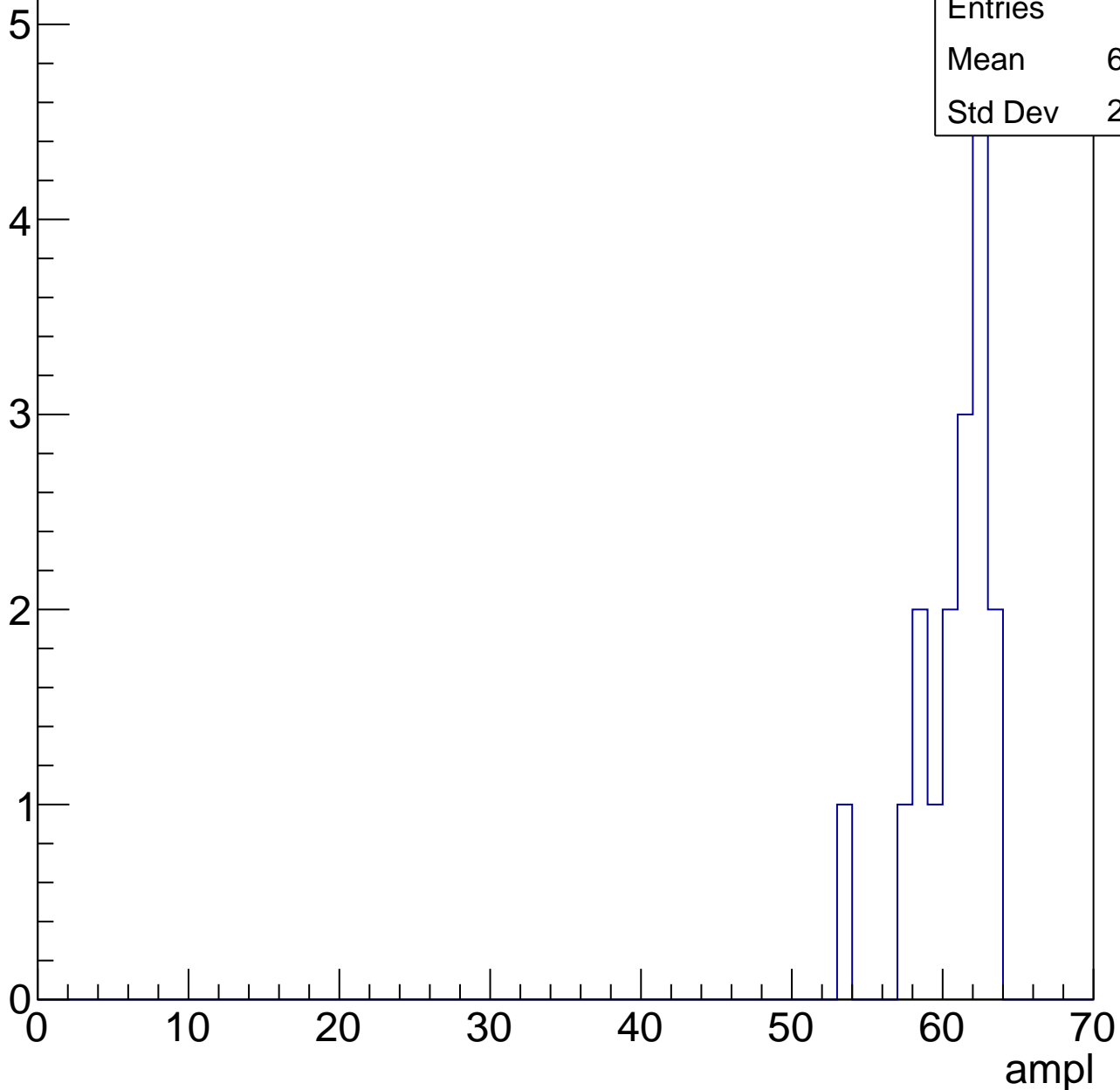


# B1L102S, U5-ch66, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	17
Mean	60.24
Std Dev	2.509





# B1L102S, U5-ch66, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U5-ch67, adc0

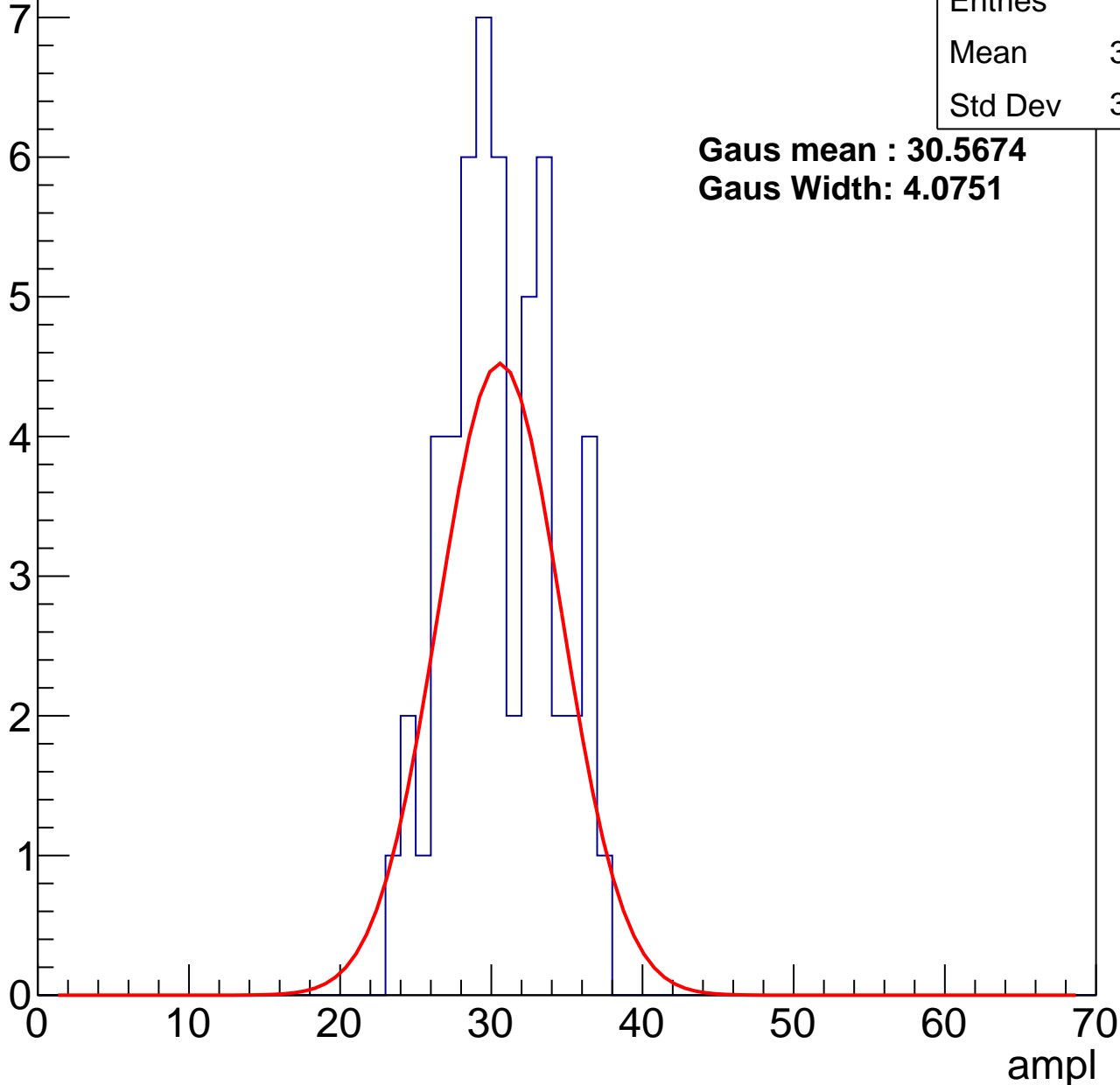
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	30.15
Std Dev	3.439

**Gaus mean : 30.5674**

**Gaus Width: 4.0751**



# B1L102S, U5-ch67, adc1

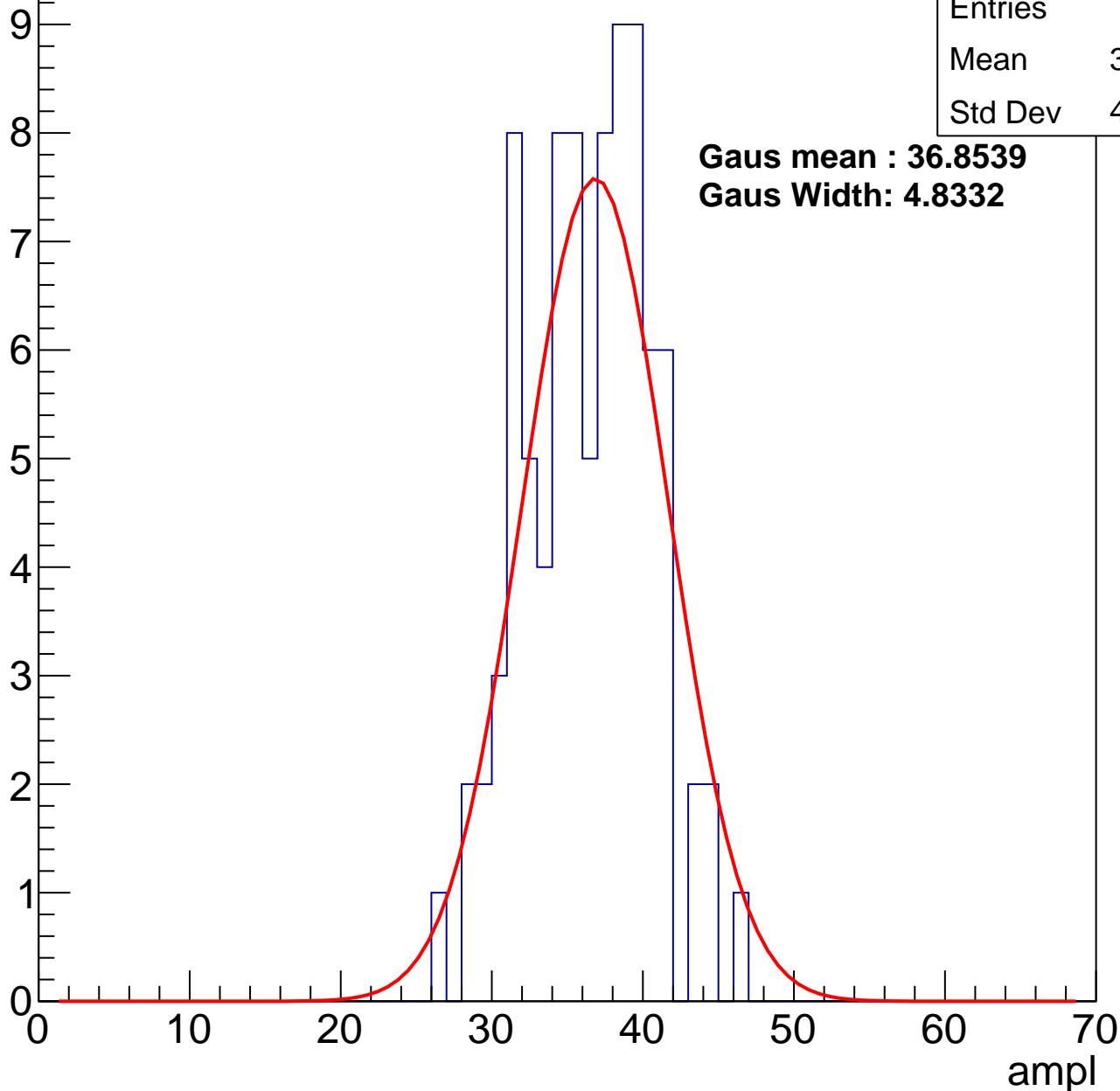
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	89
Mean	35.92
Std Dev	4.087

**Gaus mean : 36.8539**

**Gaus Width: 4.8332**



# B1L102S, U5-ch67, adc2

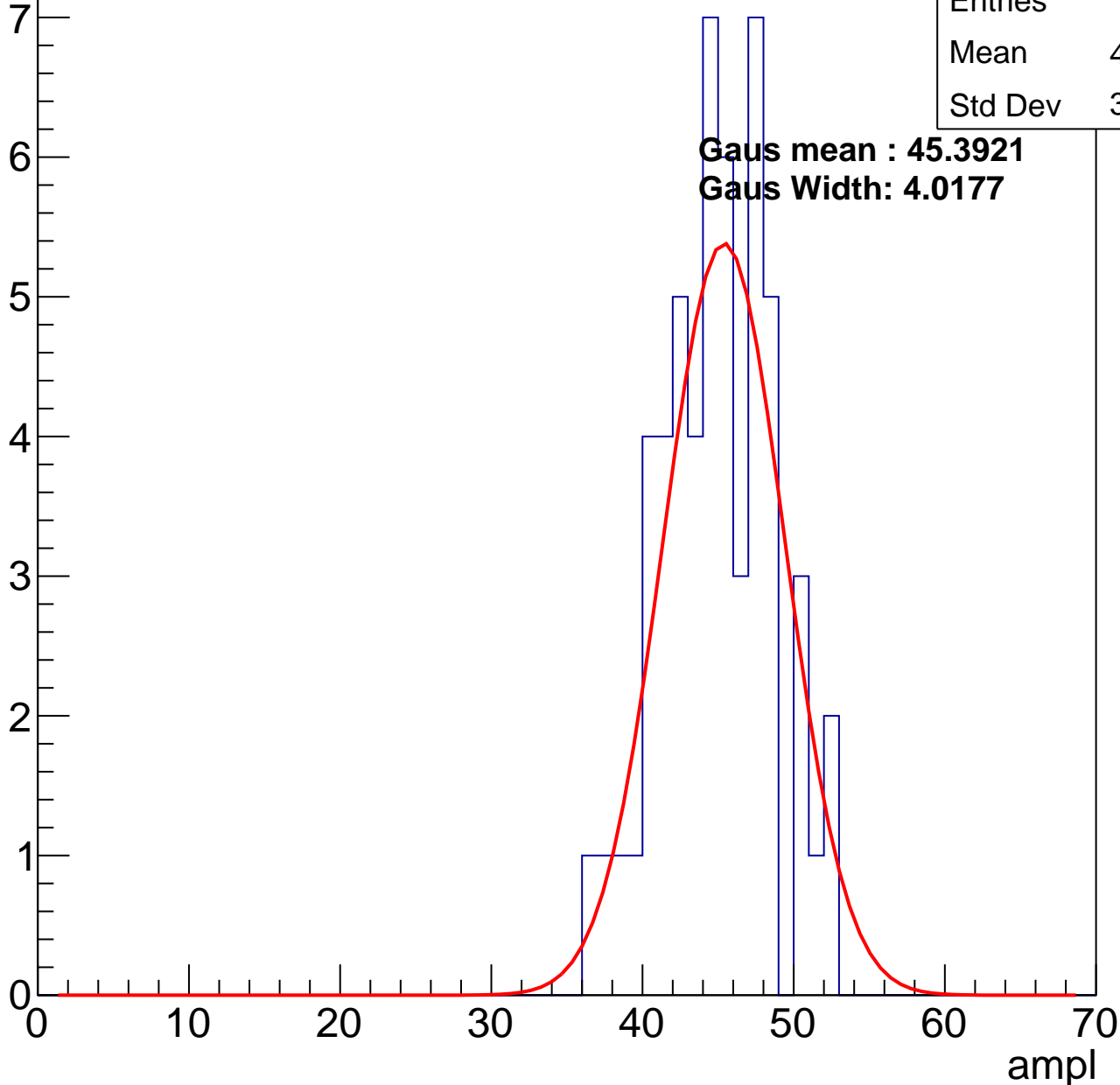
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	44.47
Std Dev	3.647

**Gaus mean : 45.3921**

**Gaus Width: 4.0177**

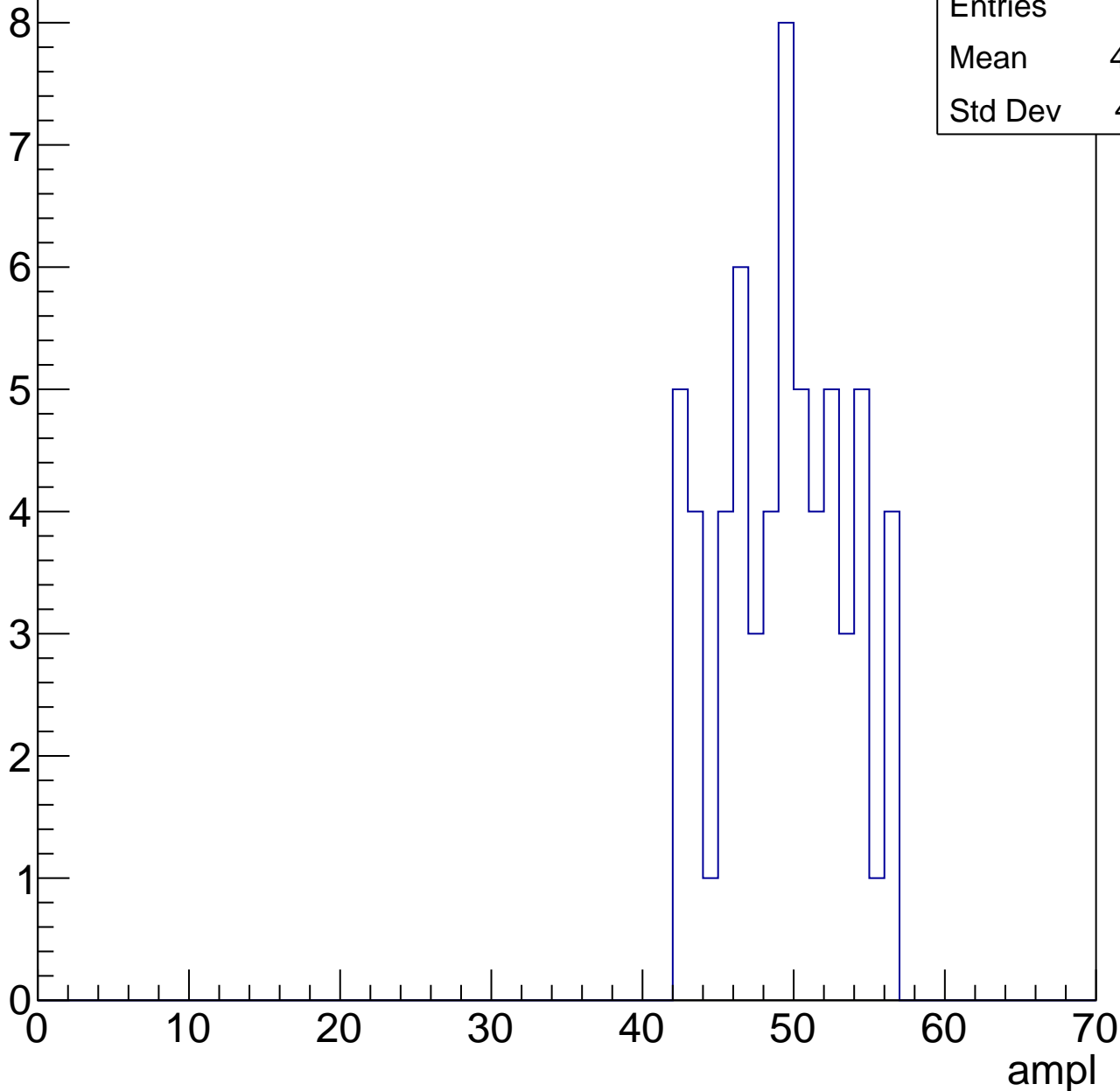


# B1L102S, U5-ch67, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

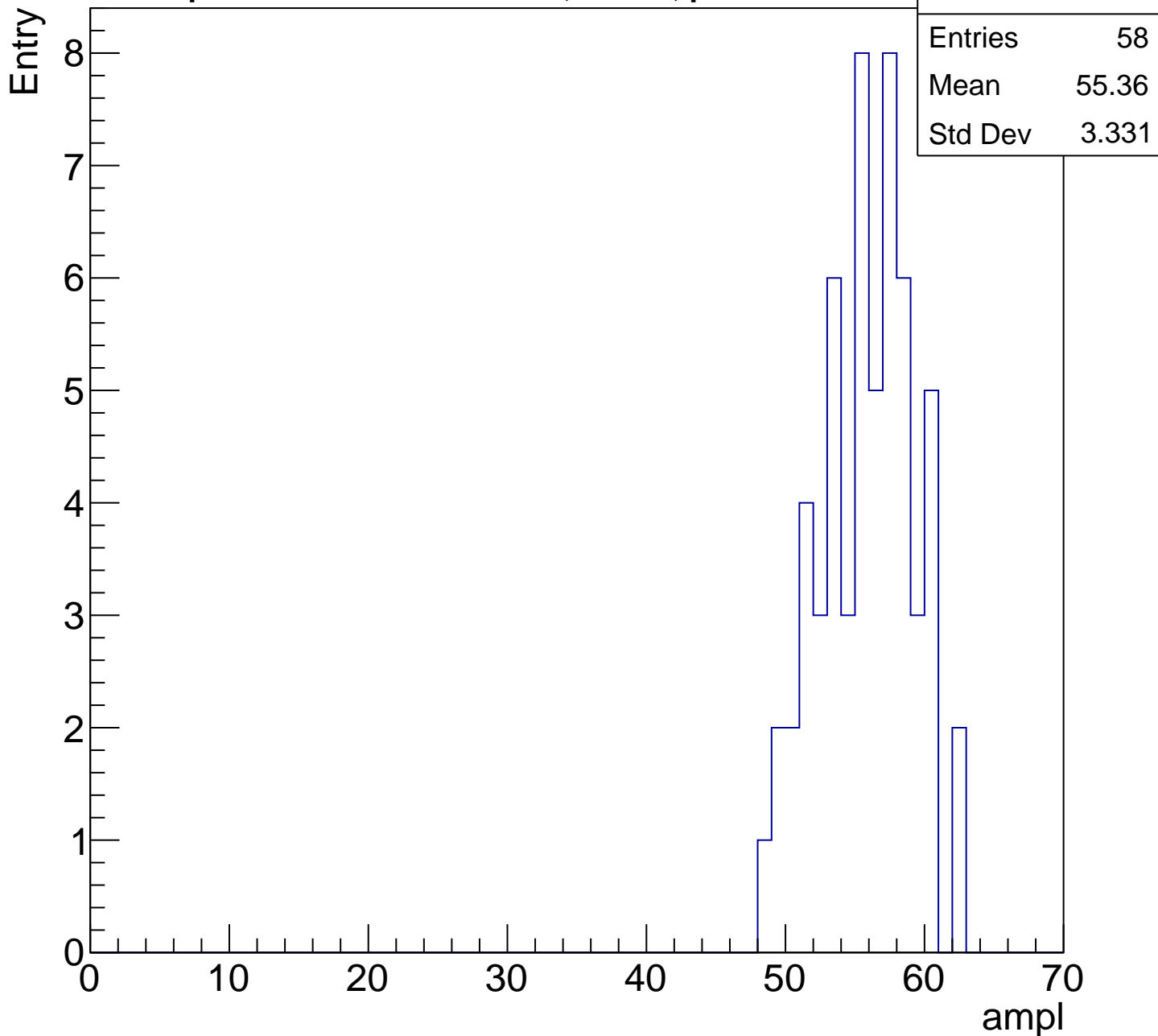
Entry

Entries	62
Mean	48.85
Std Dev	4.051



# B1L102S, U5-ch67, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

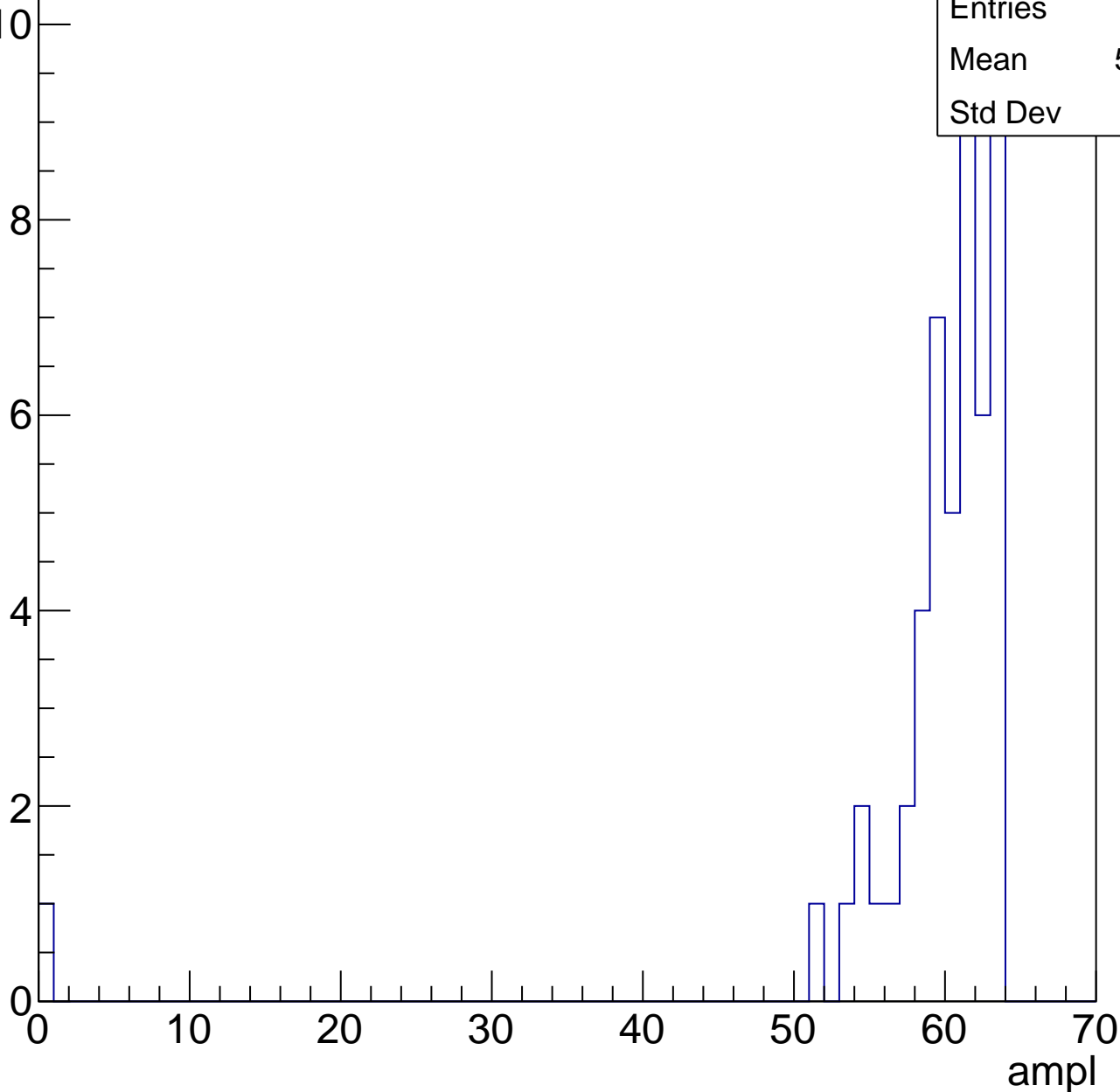


# B1L102S, U5-ch67, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	58.71
Std Dev	8.77



# B1L102S, U5-ch67, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	62
Std Dev	0

ampl



# B1L102S, U5-ch67, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U5-ch68, adc0

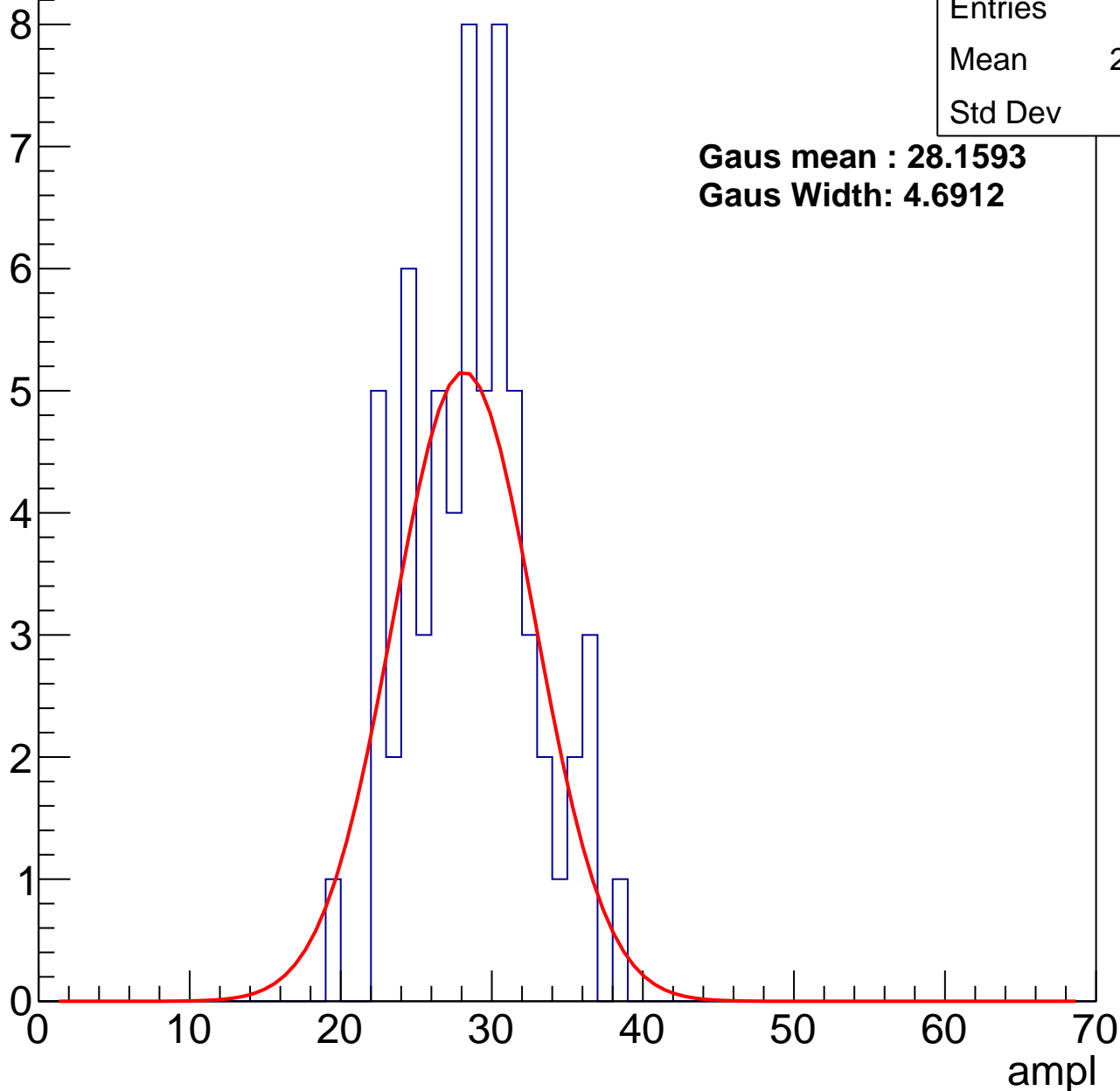
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	28.25
Std Dev	4.07

**Gaus mean : 28.1593**

**Gaus Width: 4.6912**



# B1L102S, U5-ch68, adc1

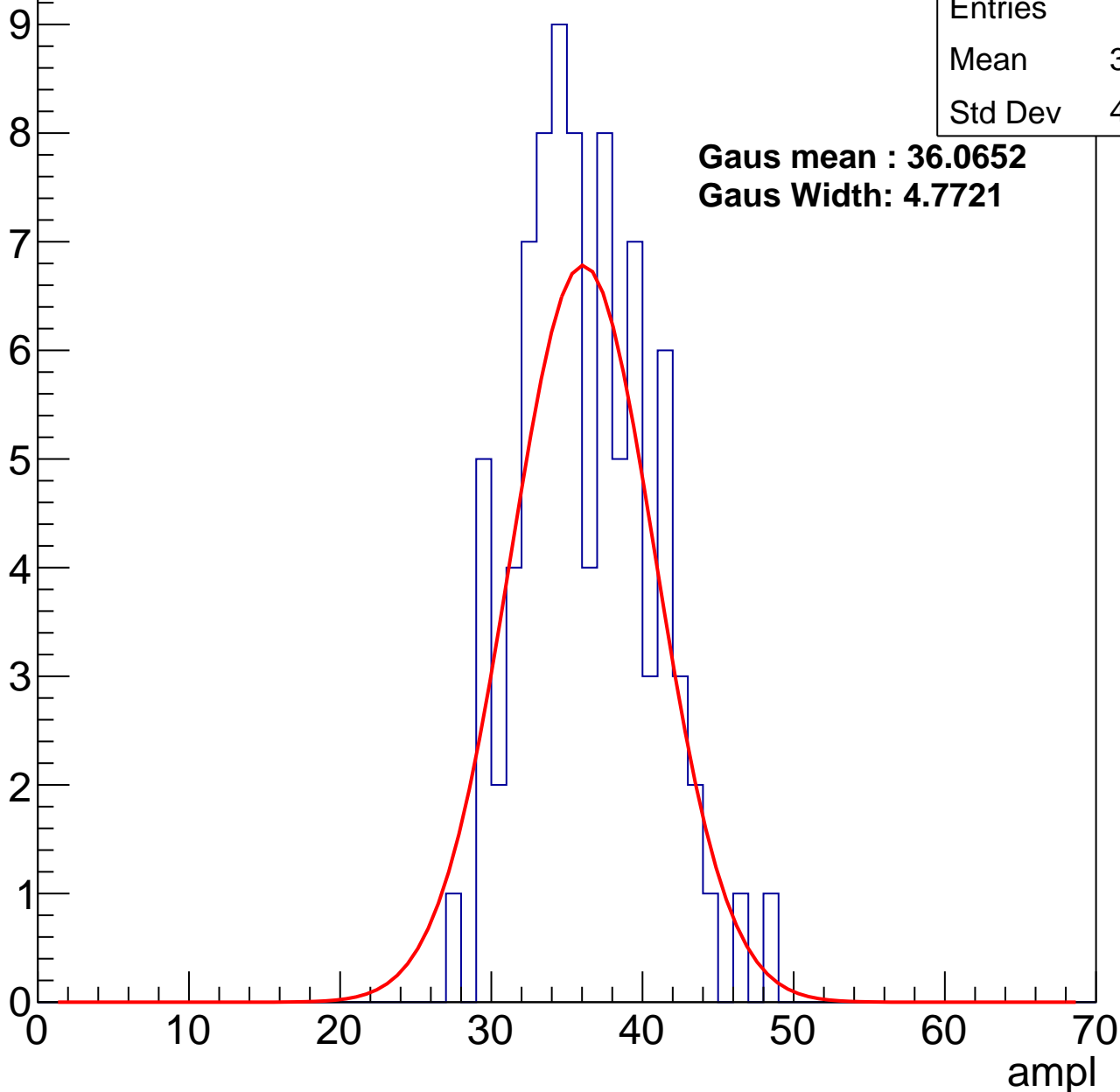
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	85
Mean	35.87
Std Dev	4.239

**Gaus mean : 36.0652**

**Gaus Width: 4.7721**



# B1L102S, U5-ch68, adc2

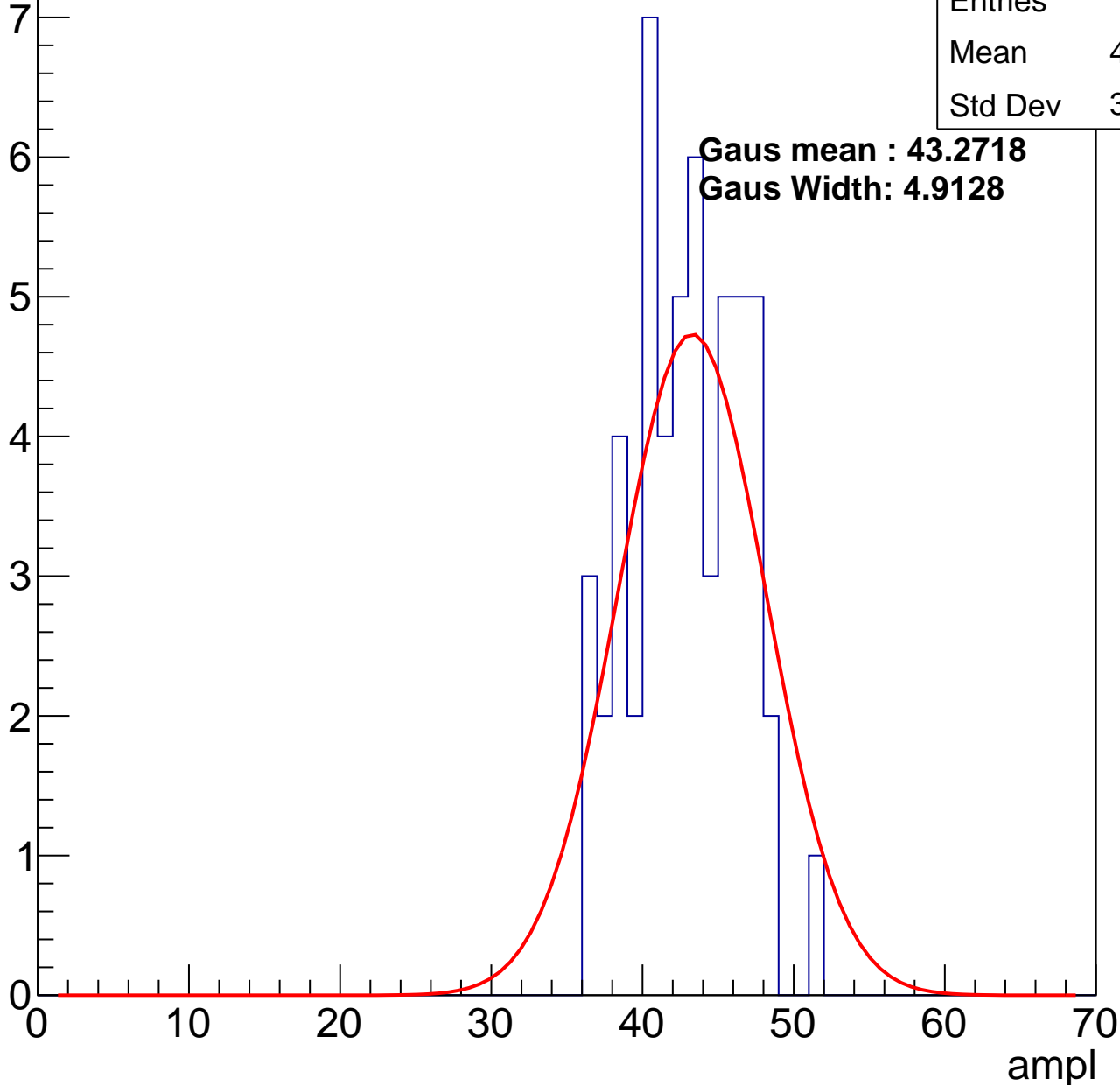
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	42.46
Std Dev	3.552

**Gaus mean : 43.2718**

**Gaus Width: 4.9128**

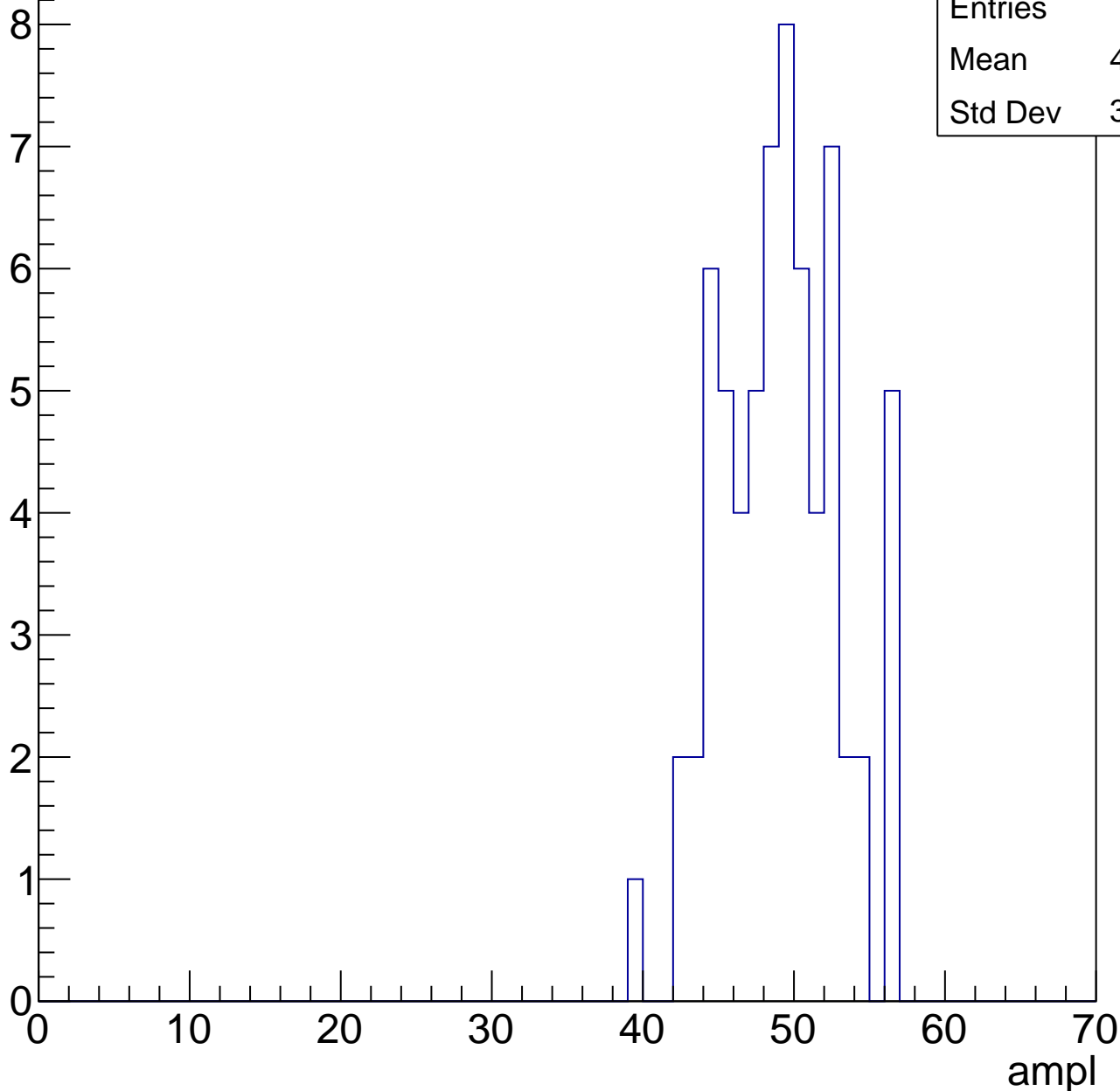


# B1L102S, U5-ch68, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	48.59
Std Dev	3.822

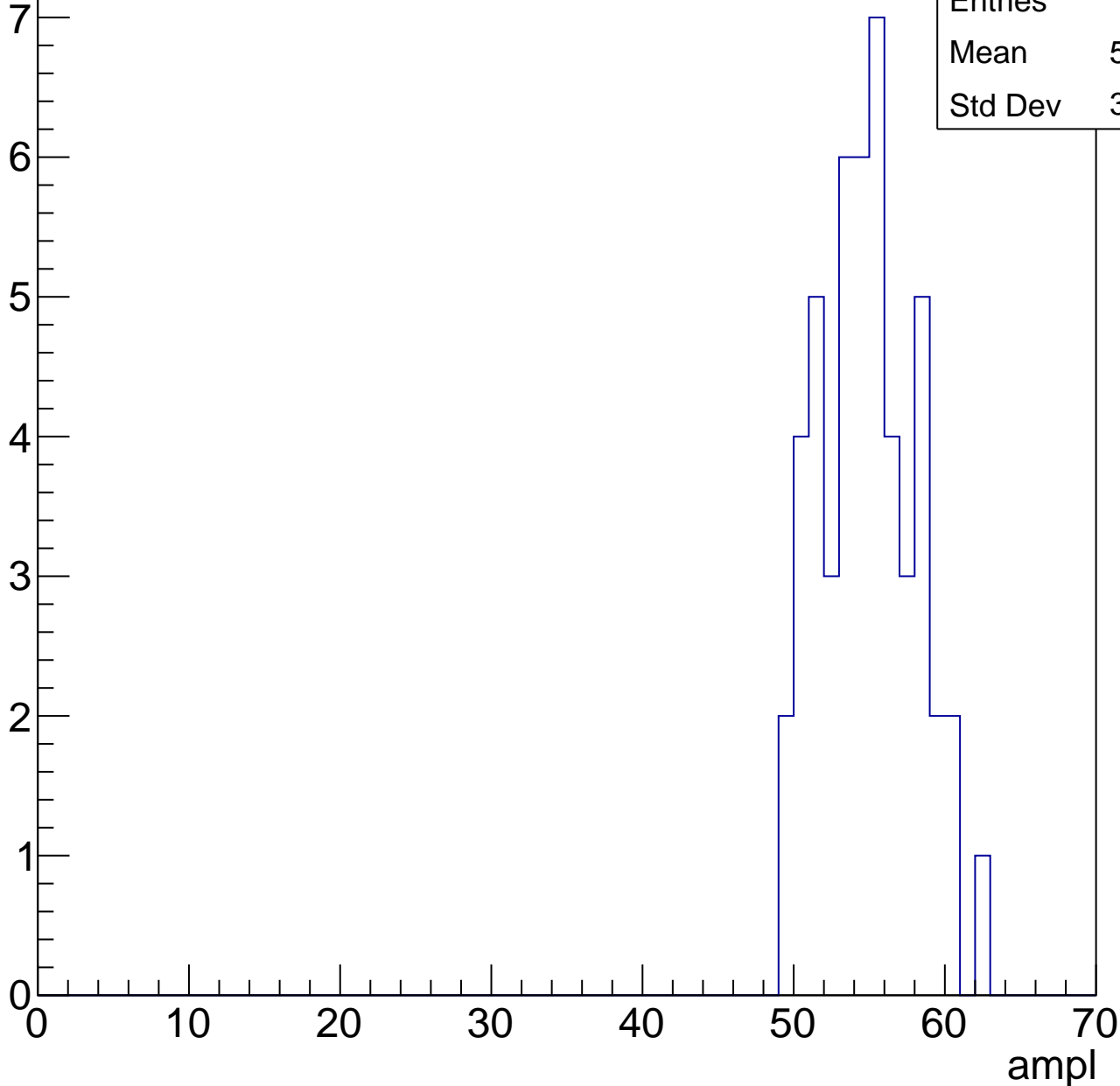


# B1L102S, U5-ch68, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	54.42
Std Dev	3.112

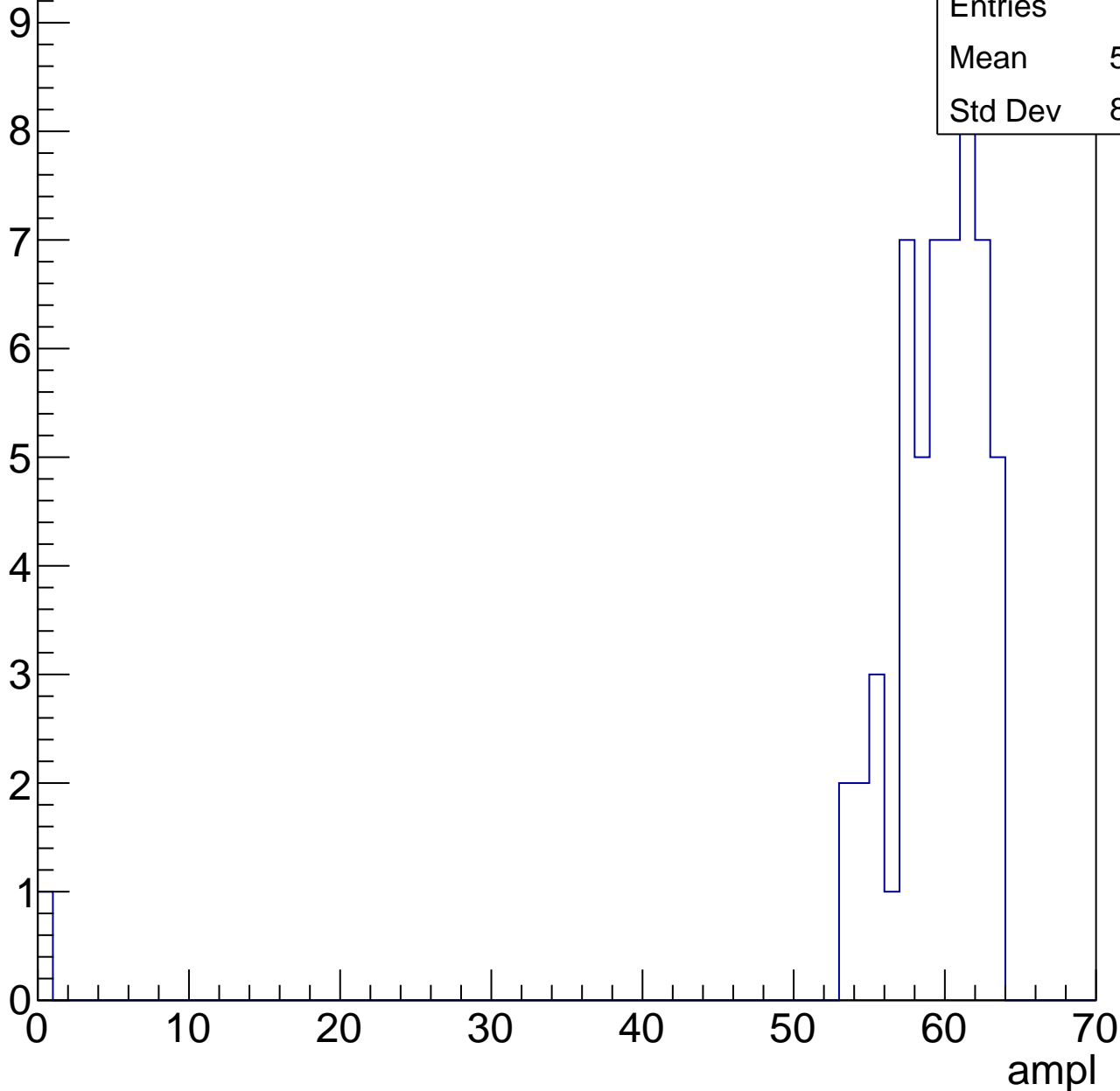


# B1L102S, U5-ch68, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	58.12
Std Dev	8.277

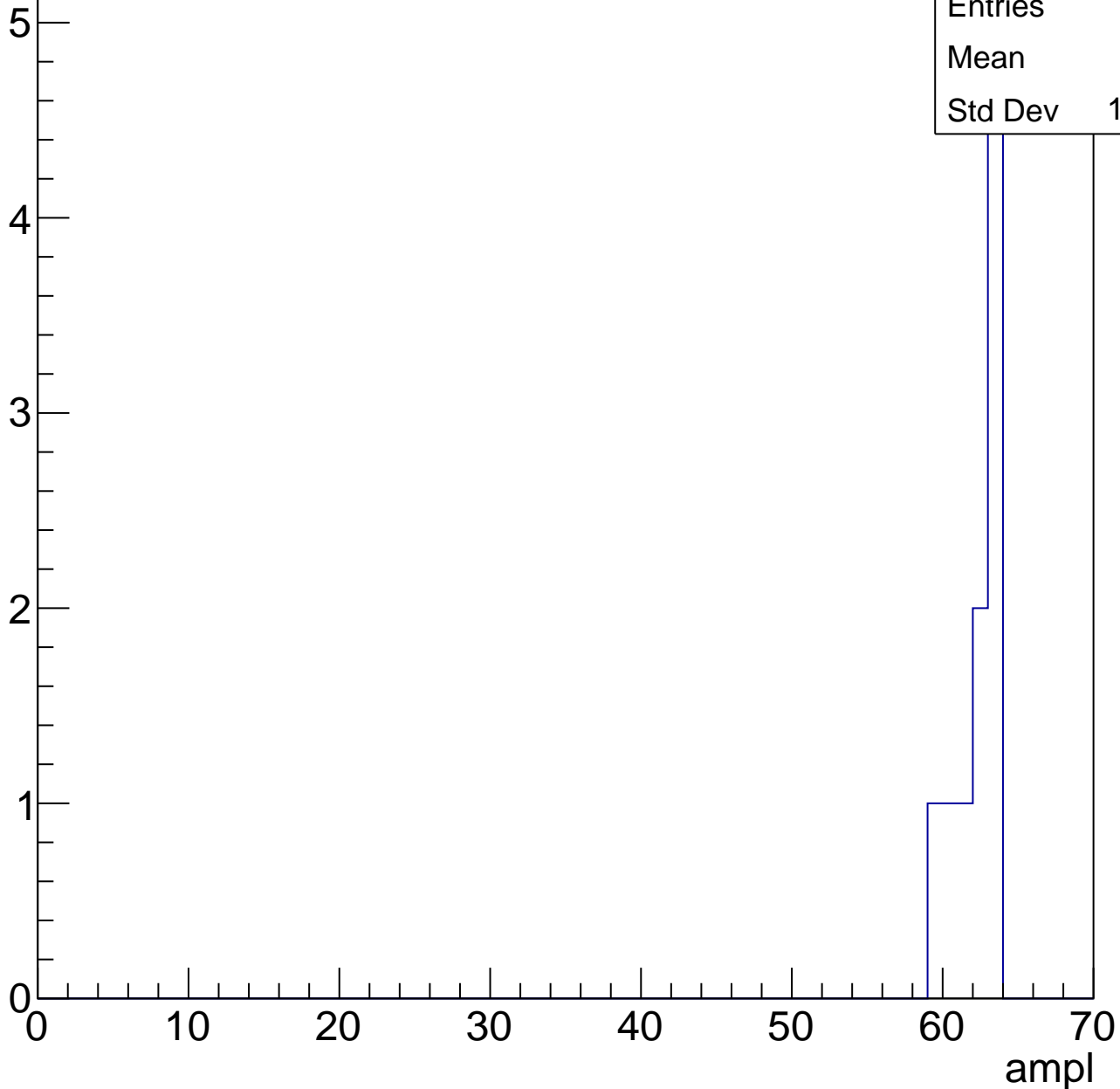


# B1L102S, U5-ch68, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	10
Mean	61.9
Std Dev	1.375





# B1L102S, U5-ch68, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U5-ch69, adc0

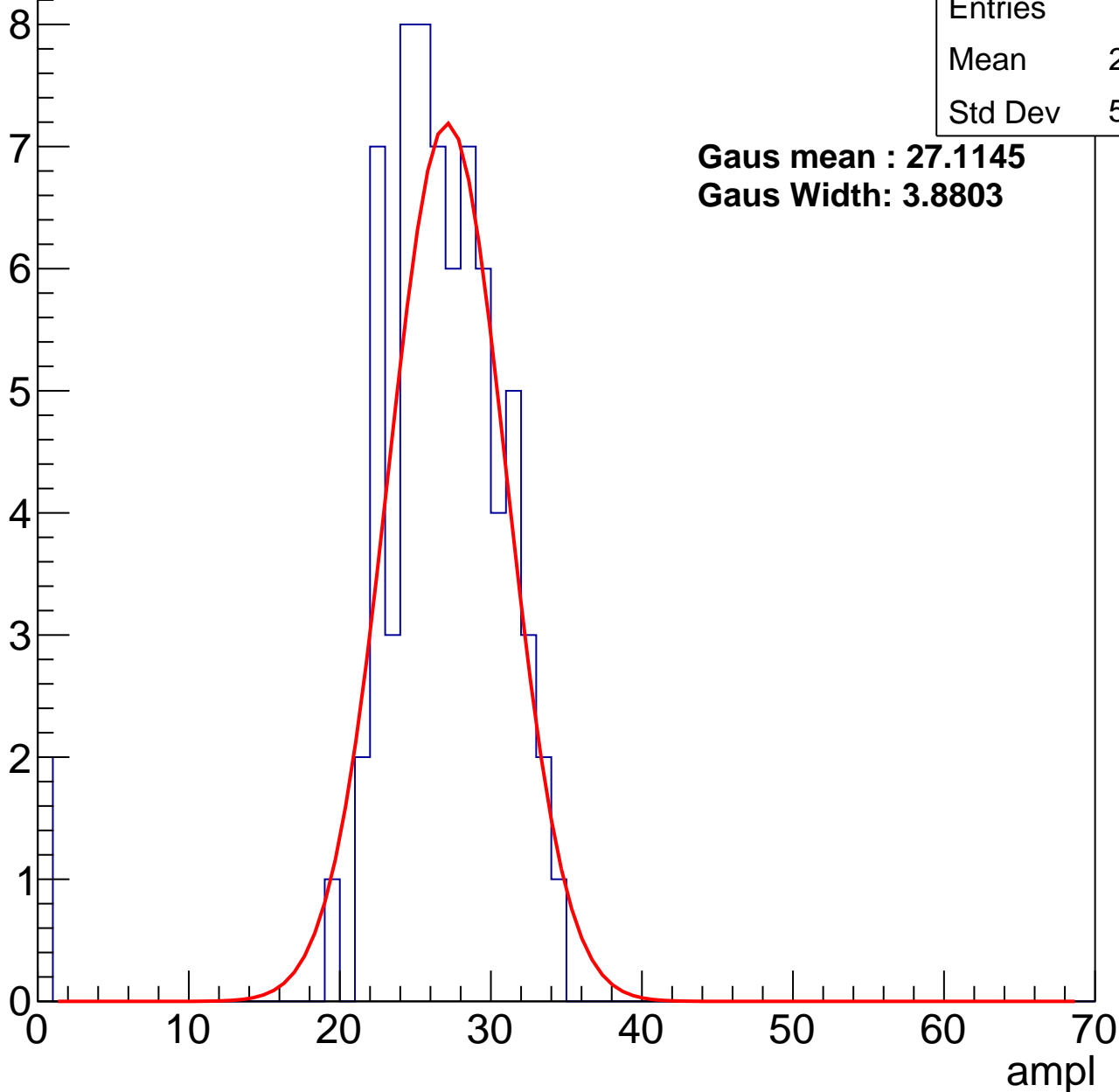
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	25.85
Std Dev	5.497

**Gaus mean : 27.1145**

**Gaus Width: 3.8803**



# B1L102S, U5-ch69, adc1

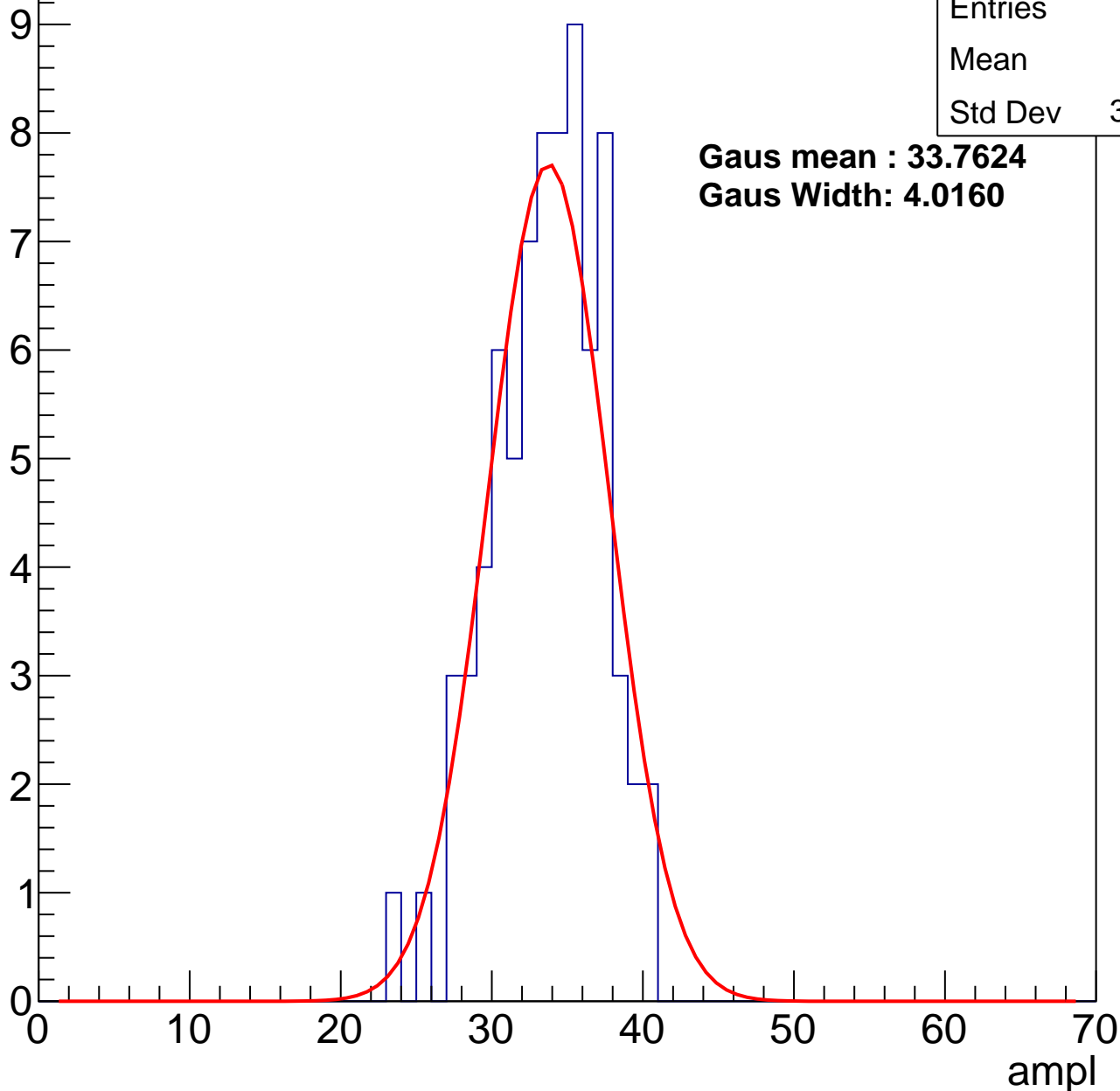
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	33.2
Std Dev	3.554

**Gaus mean : 33.7624**

**Gaus Width: 4.0160**



# B1L102S, U5-ch69, adc2

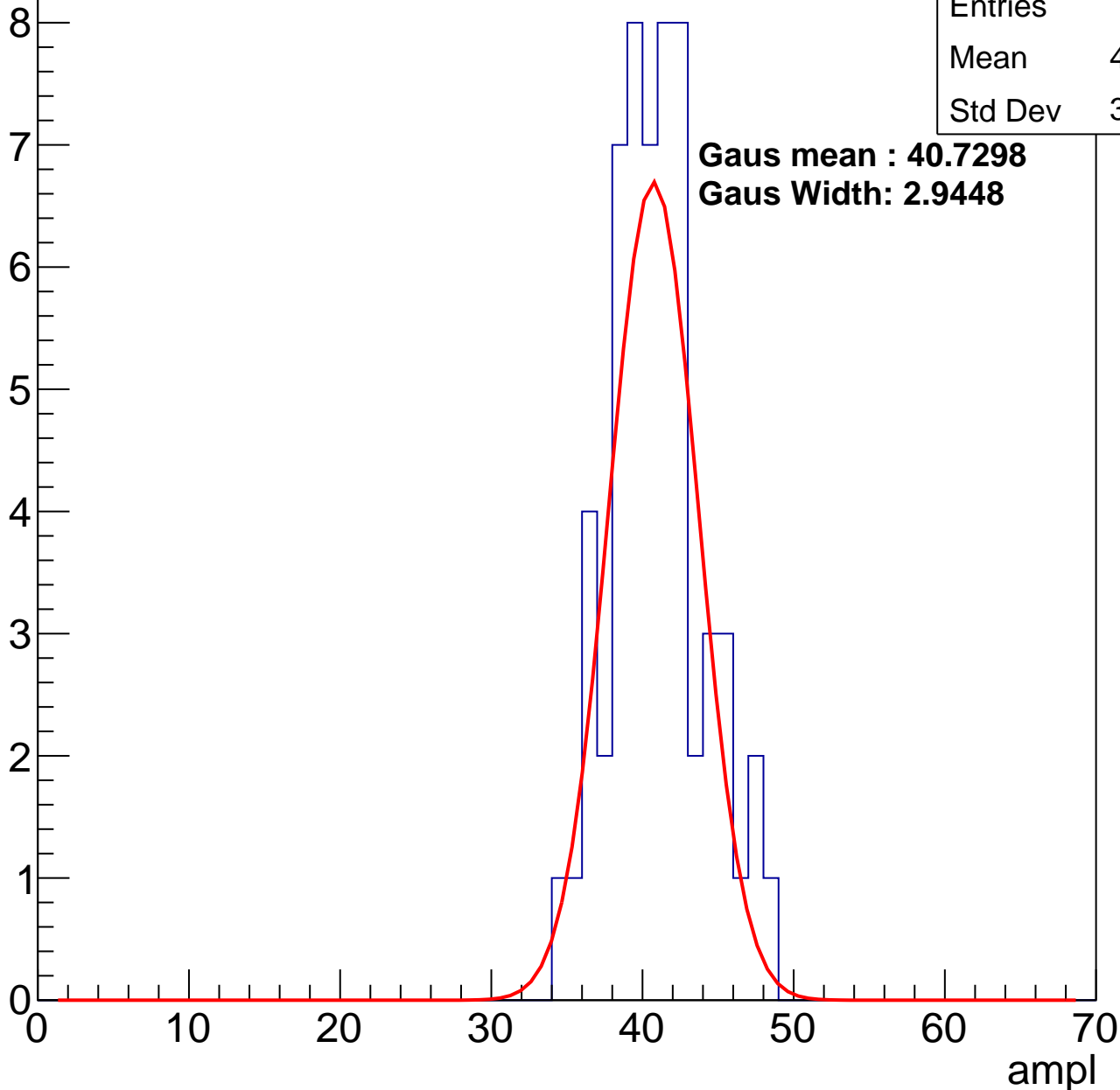
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	40.52
Std Dev	3.058

**Gaus mean : 40.7298**

**Gaus Width: 2.9448**

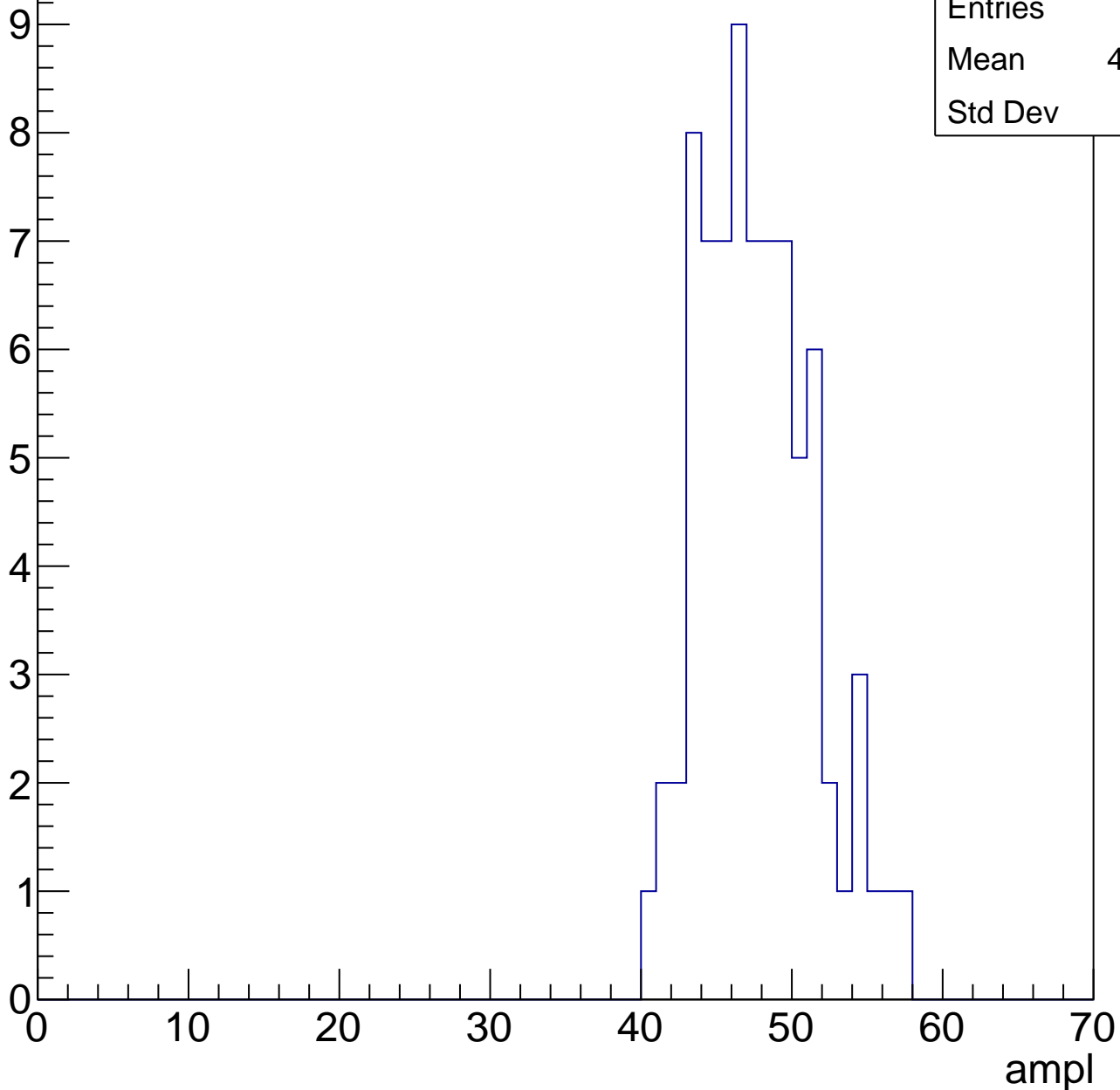


# B1L102S, U5-ch69, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

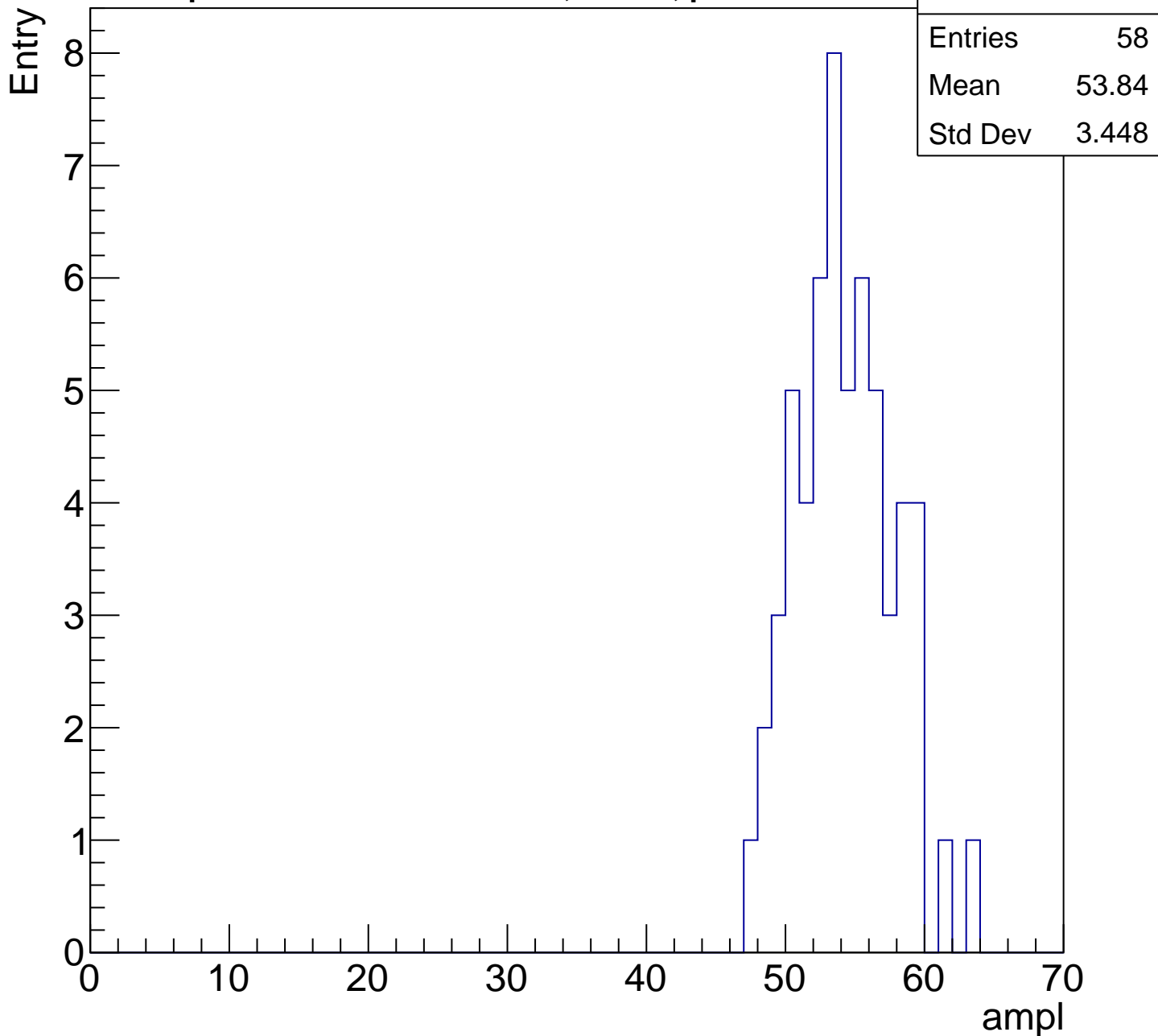
Entry

Entries	77
Mean	47.25
Std Dev	3.69



# B1L102S, U5-ch69, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2



# B1L102S, U5-ch69, adc5

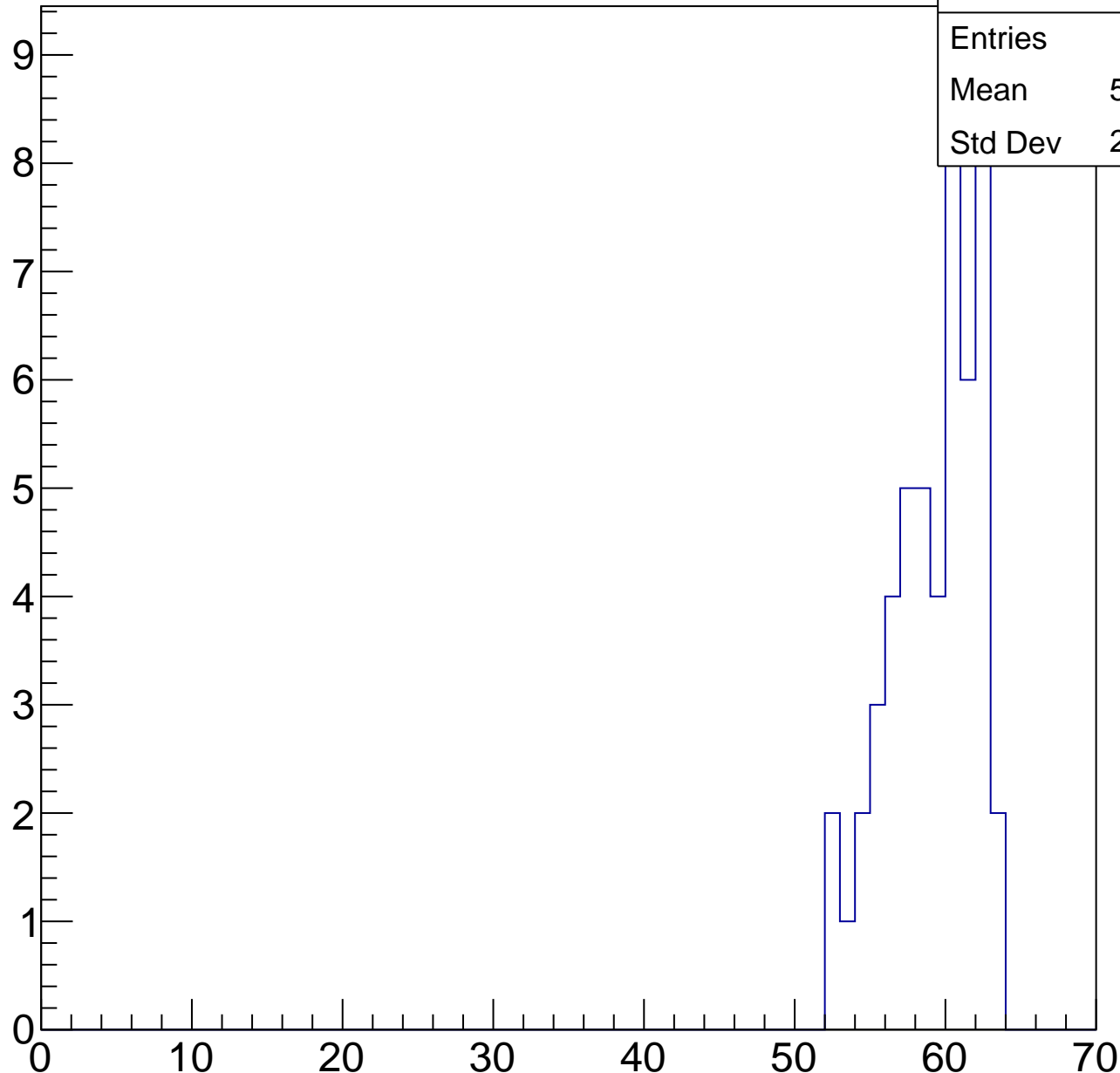
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	51
Mean	58.69
Std Dev	2.887

ampl

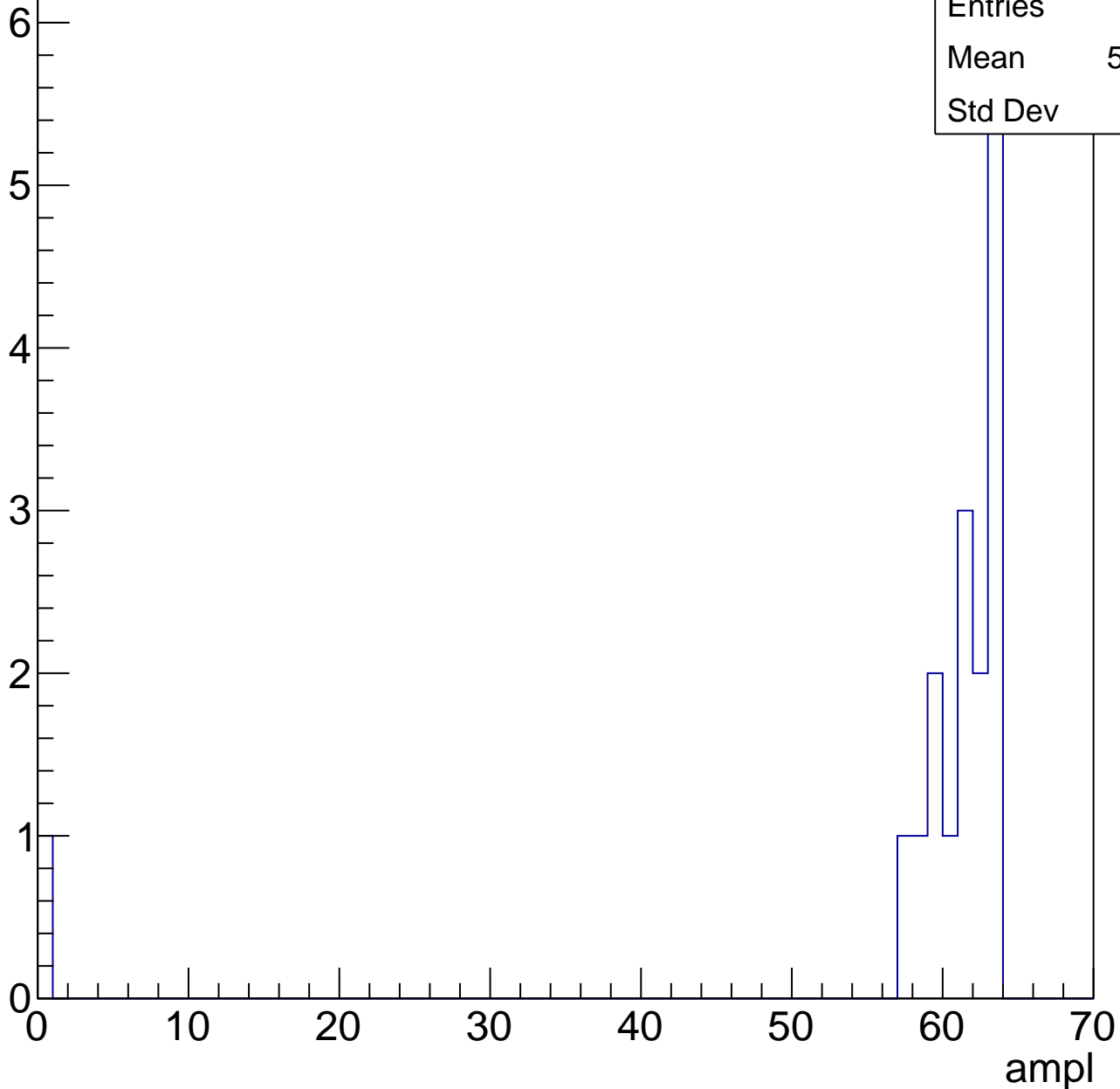


# B1L102S, U5-ch69, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	17
Mean	57.53
Std Dev	14.5





# B1L102S, U5-ch69, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	3
Mean	21
Std Dev	29.7

# B1L102S, U5-ch70, adc0

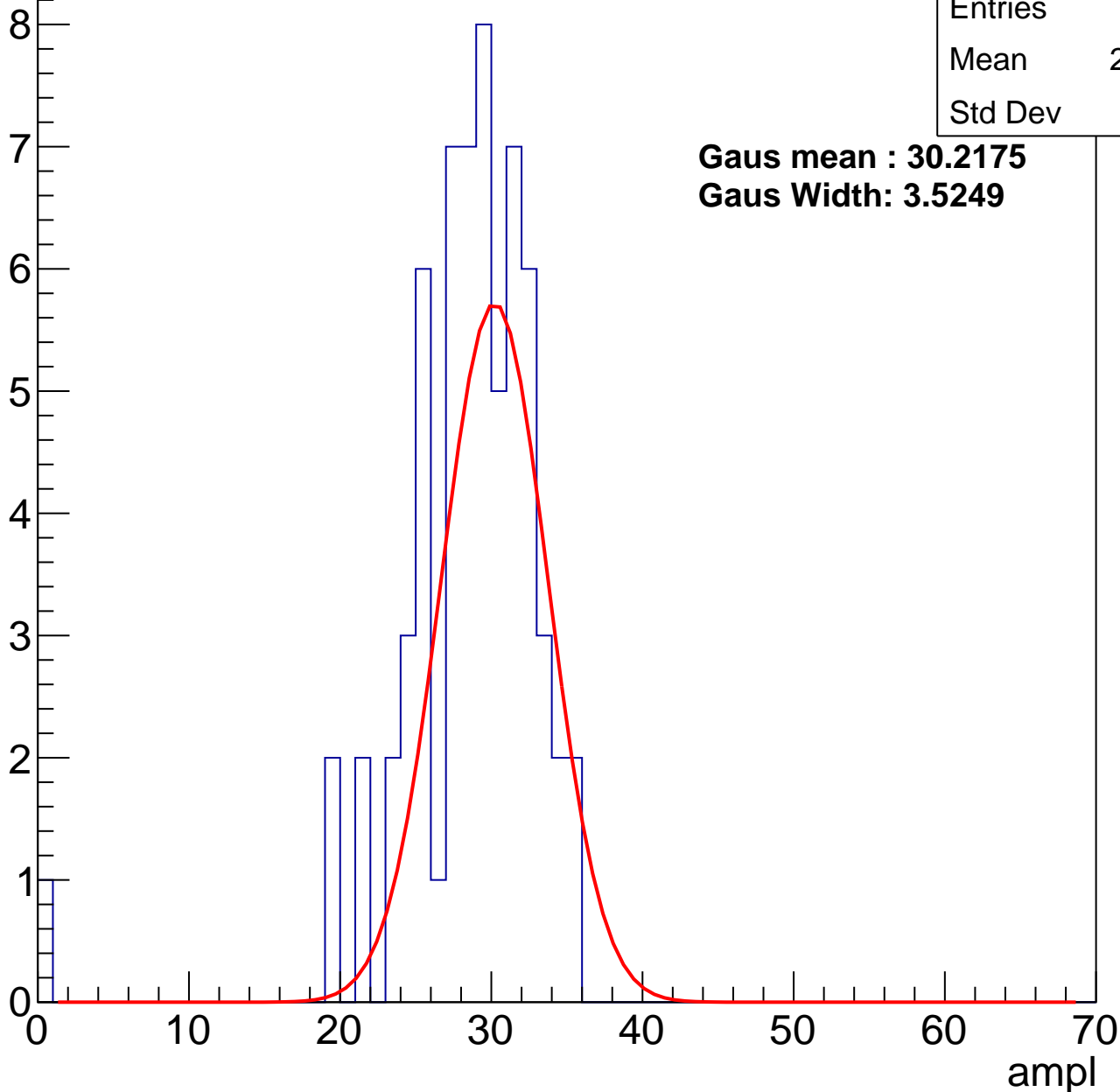
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	27.92
Std Dev	5.06

**Gaus mean : 30.2175**

**Gaus Width: 3.5249**



# B1L102S, U5-ch70, adc1

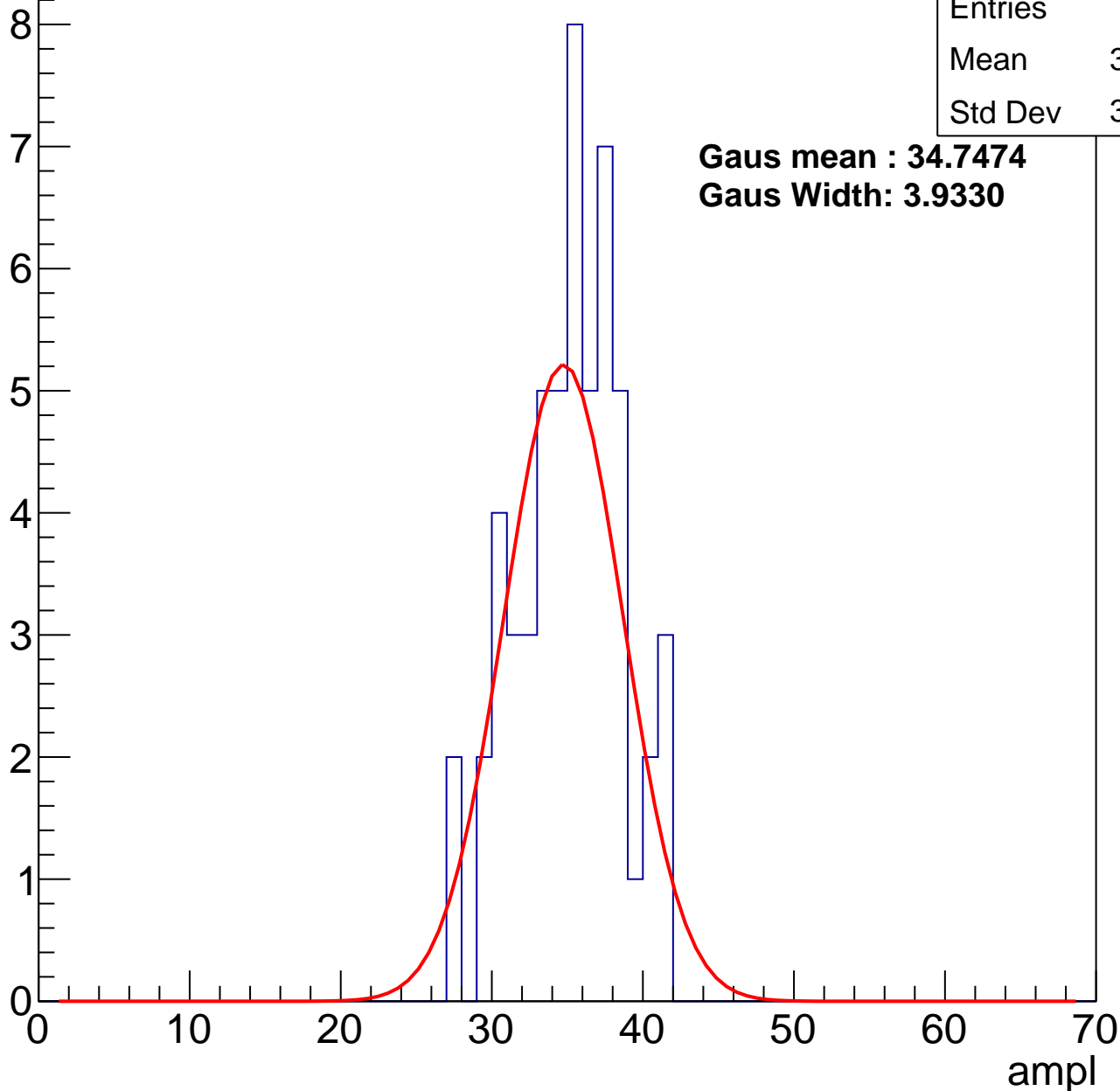
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	34.67
Std Dev	3.427

**Gaus mean : 34.7474**

**Gaus Width: 3.9330**



# B1L102S, U5-ch70, adc2

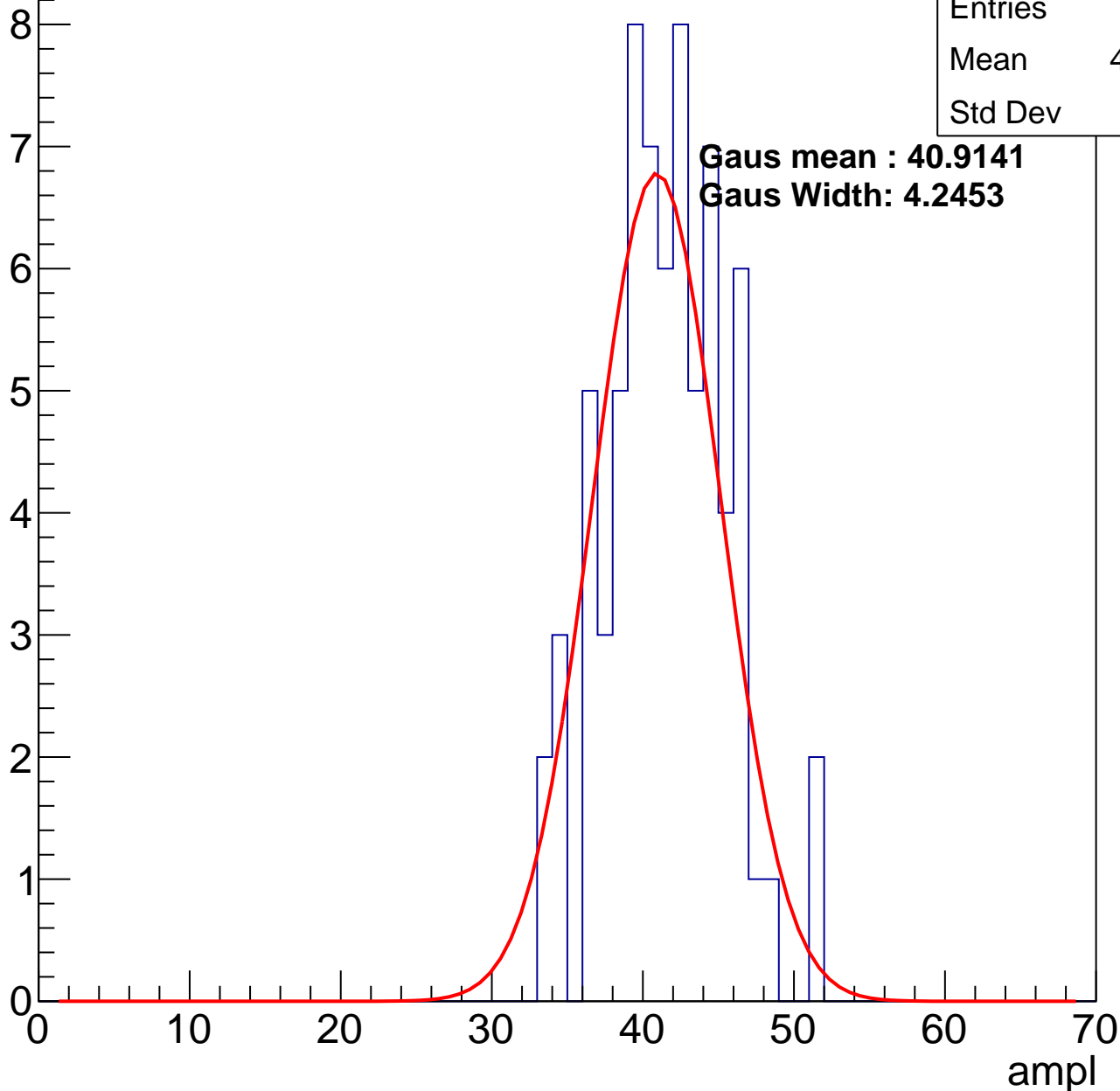
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	41.08
Std Dev	3.92

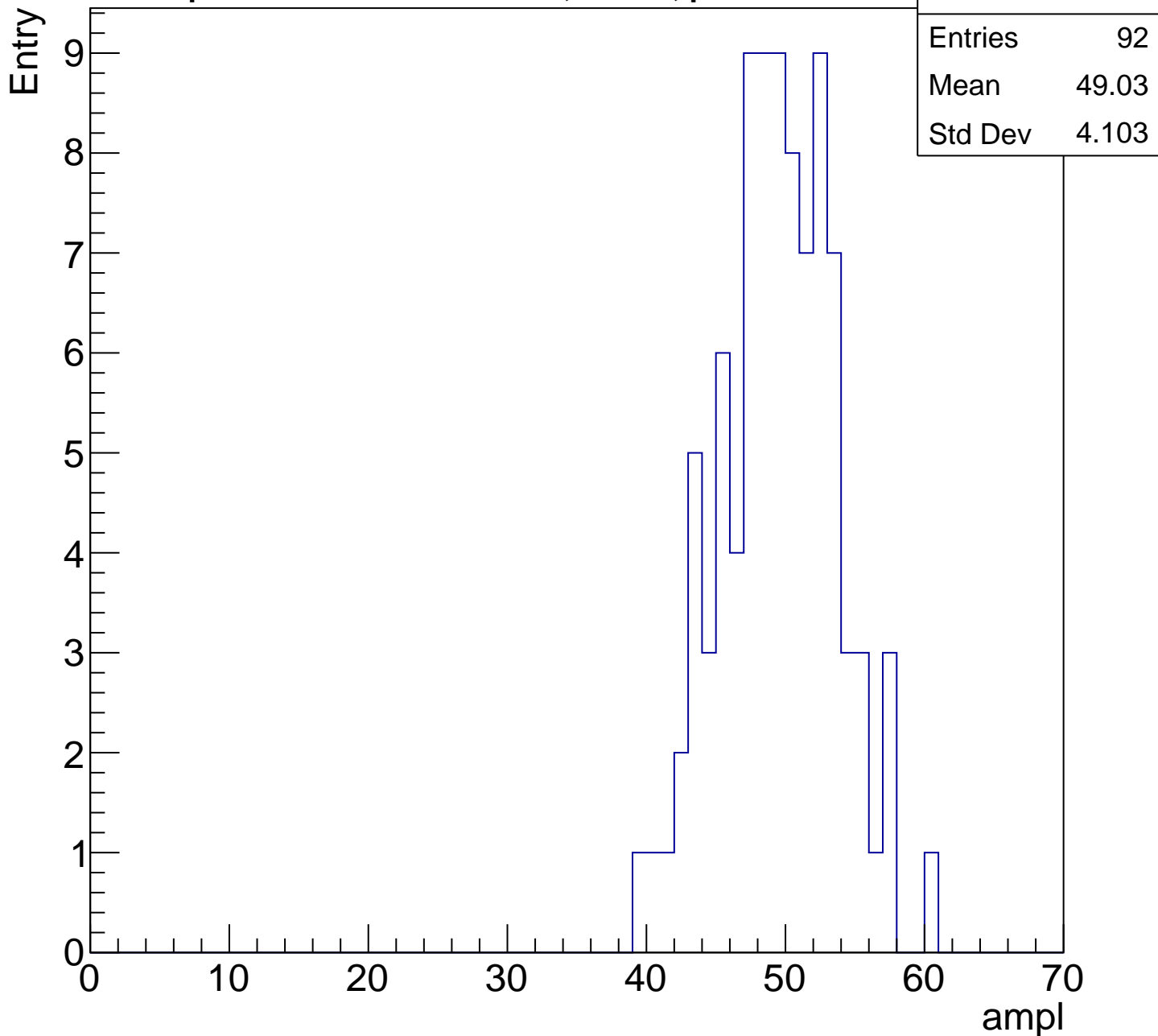
**Gaus mean : 40.9141**

**Gaus Width: 4.2453**



# B1L102S, U5-ch70, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

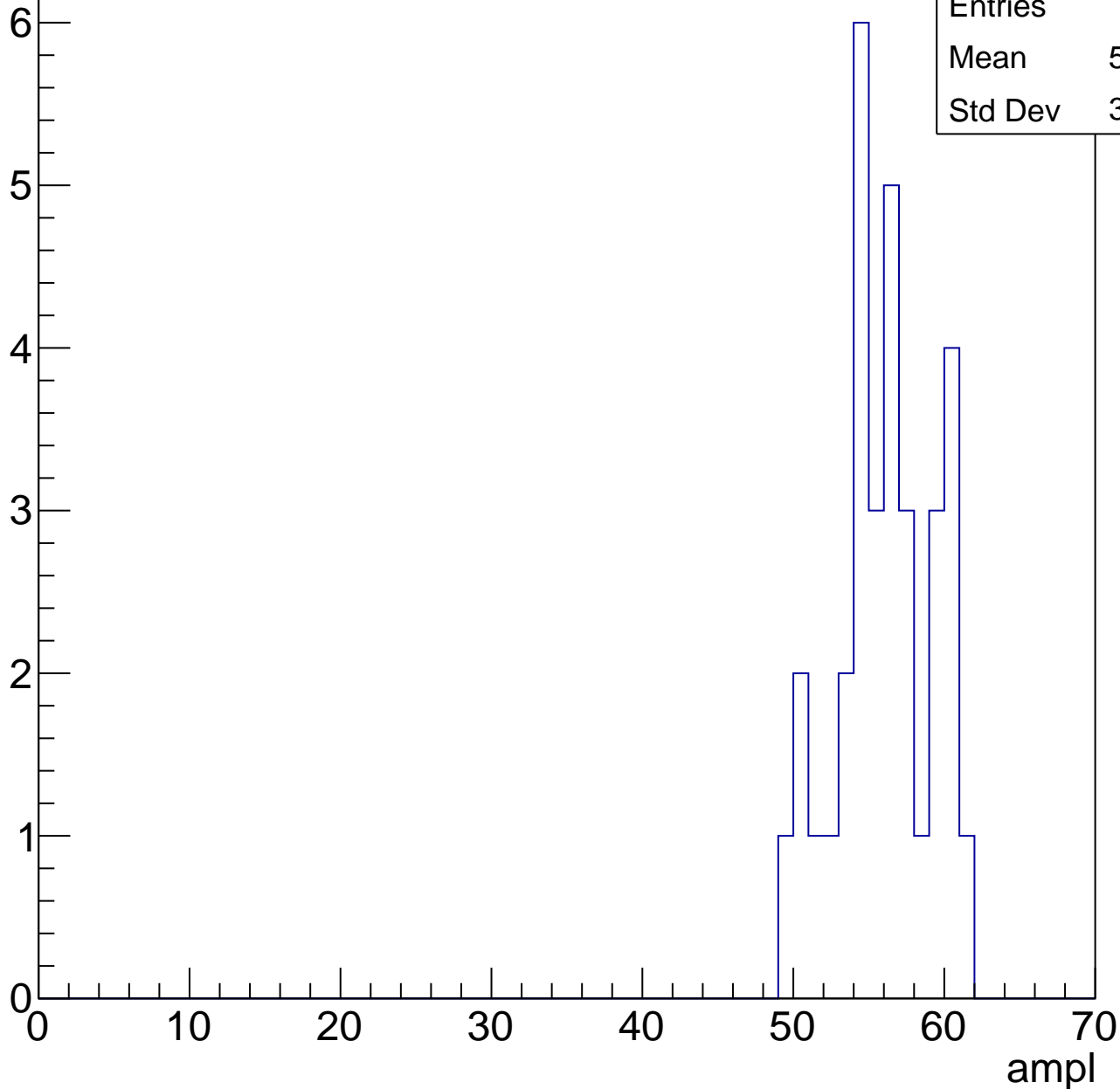


# B1L102S, U5-ch70, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	33
Mean	55.58
Std Dev	3.134



# B1L102S, U5-ch70, adc5

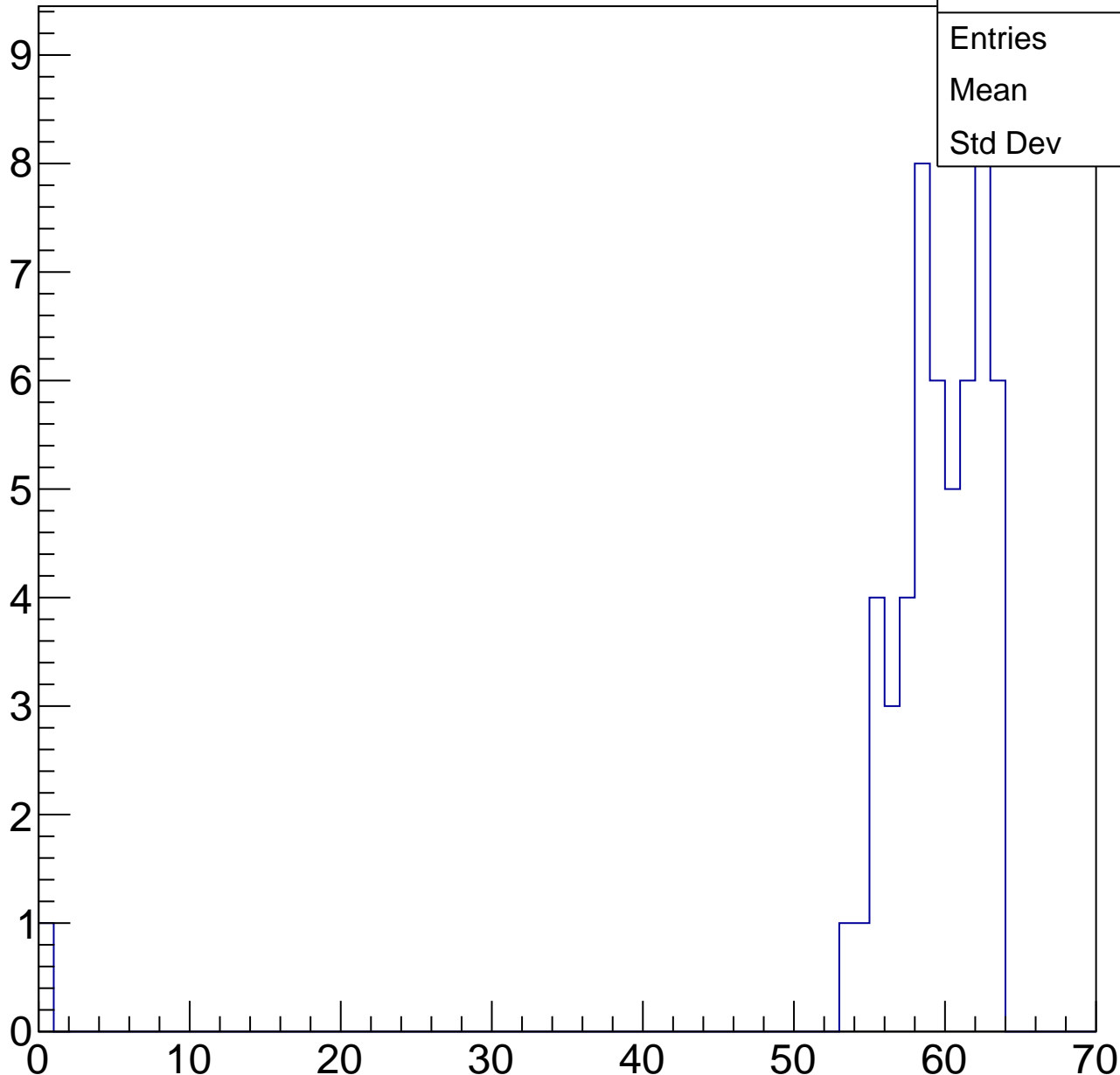
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	54
Mean	58.2
Std Dev	8.42

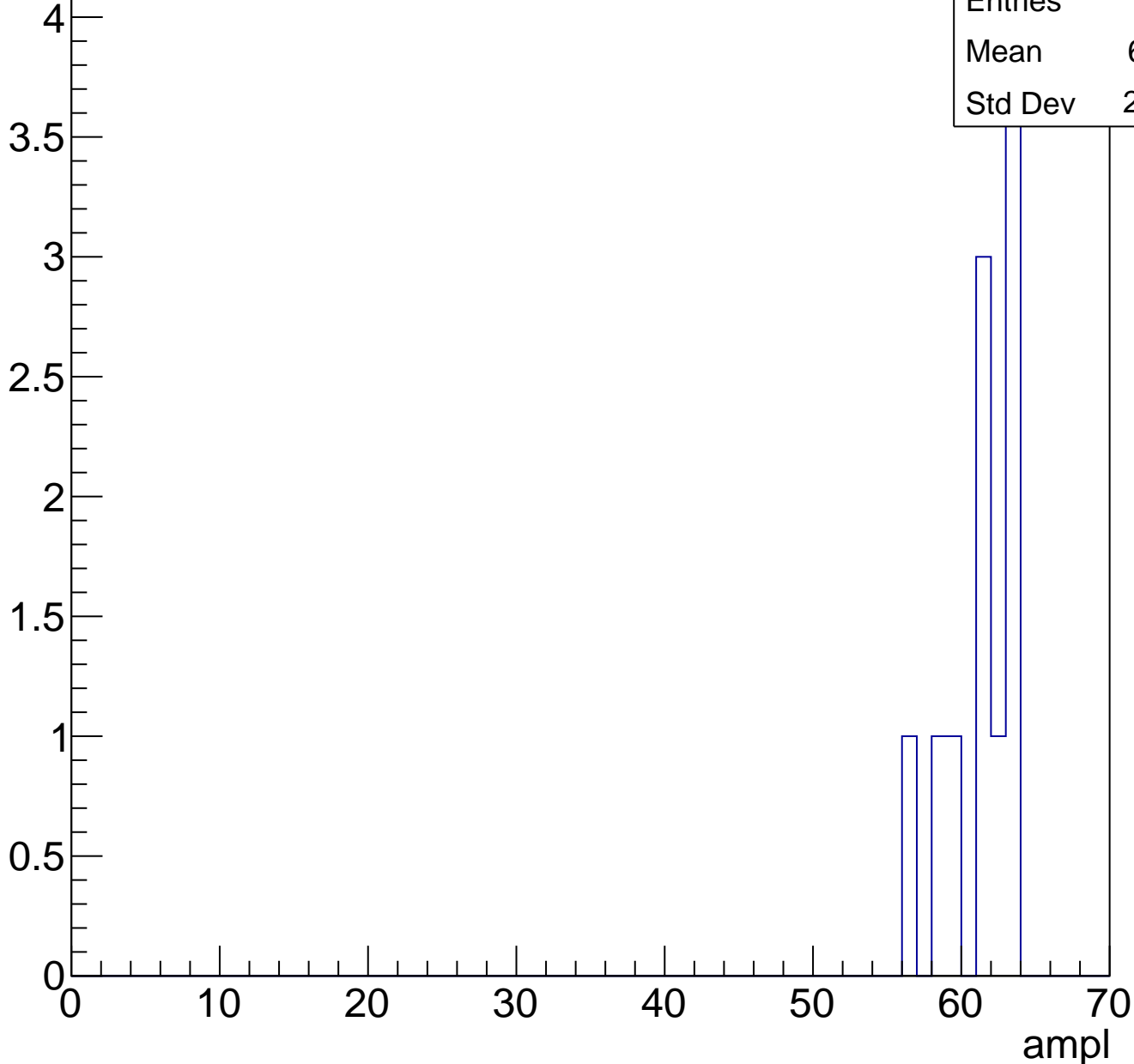
ampl



# B1L102S, U5-ch70, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U5-ch70, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U5-ch71, adc0

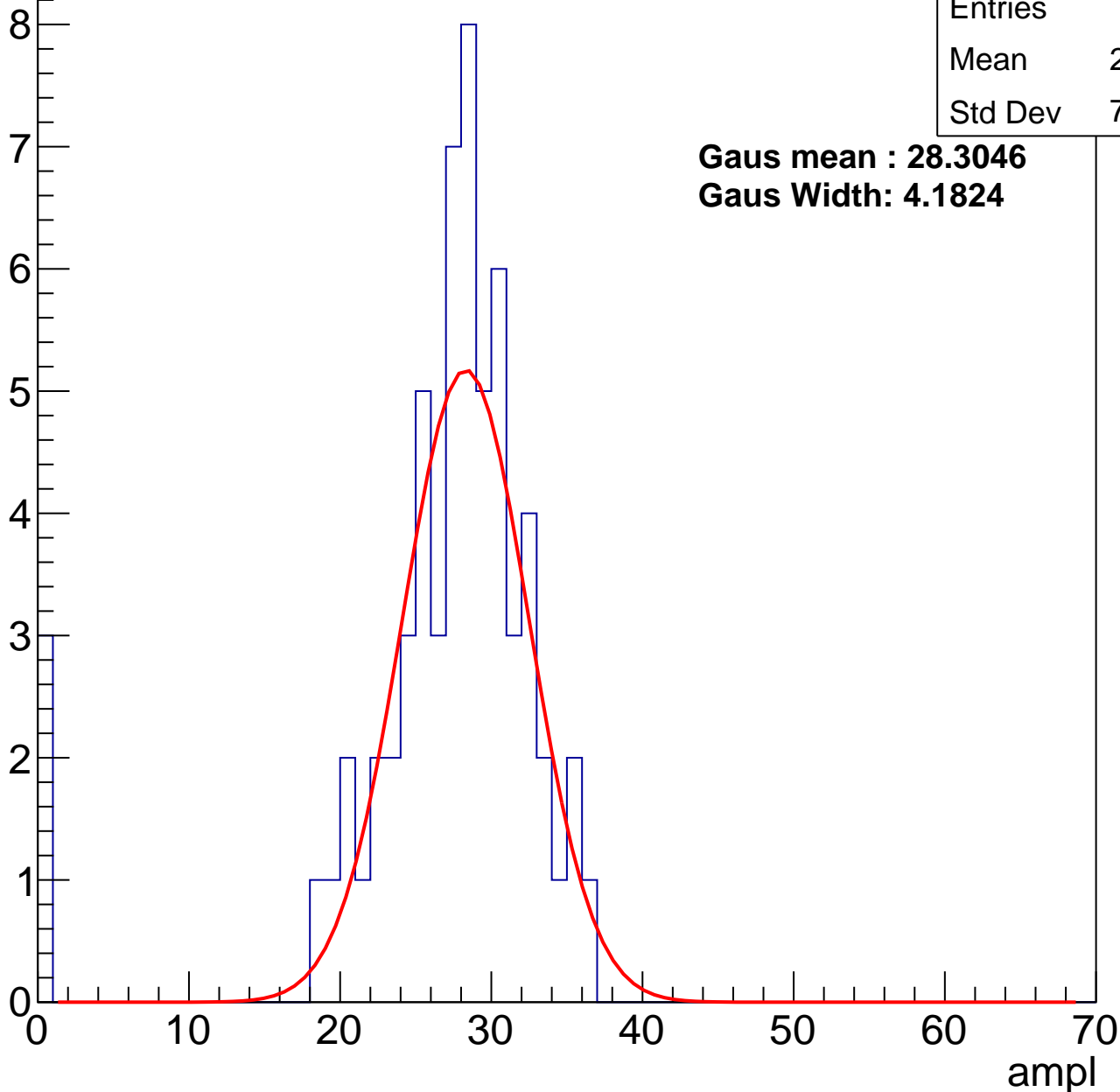
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	26.26
Std Dev	7.098

**Gaus mean : 28.3046**

**Gaus Width: 4.1824**



# B1L102S, U5-ch71, adc1

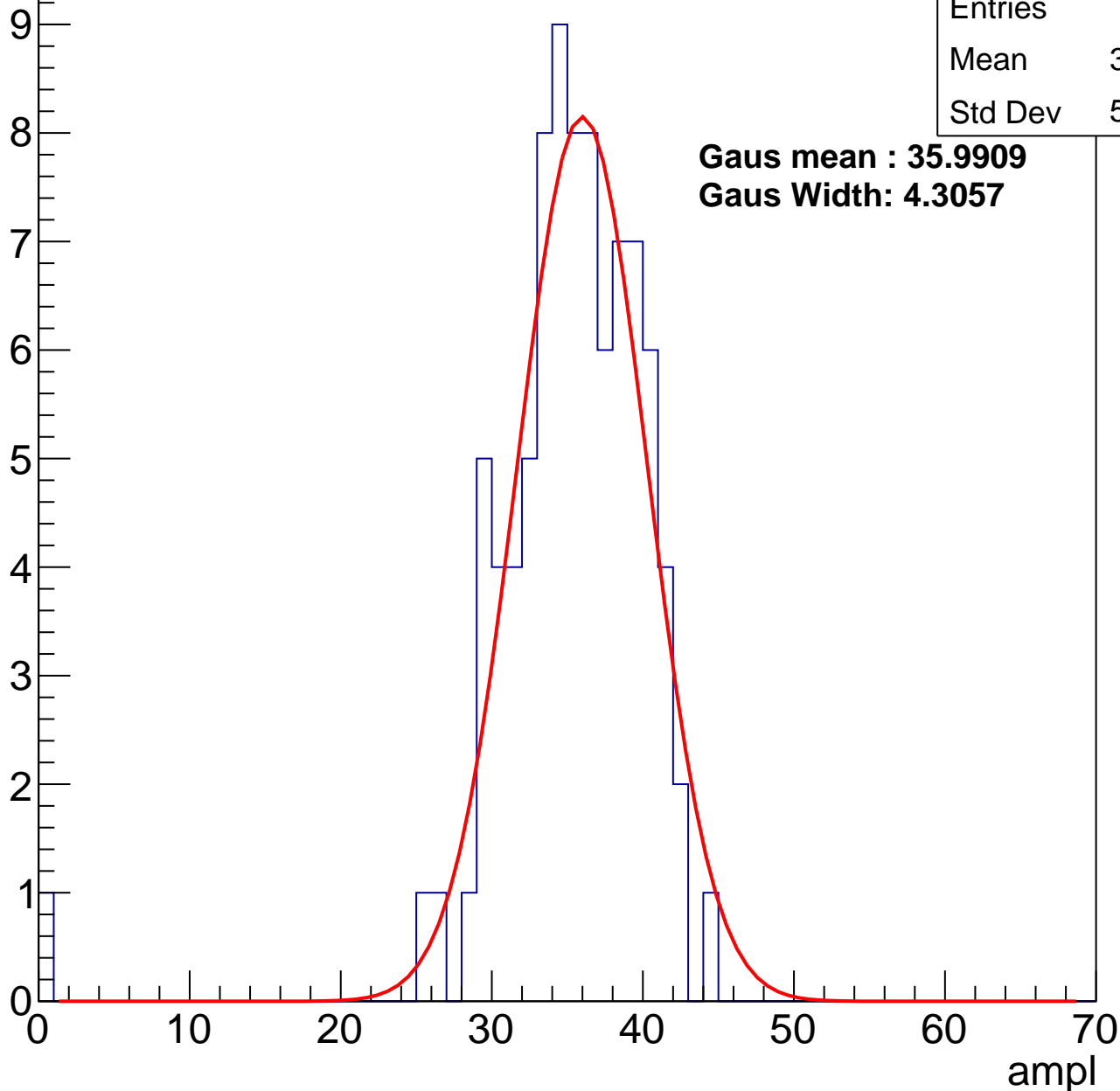
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	88
Mean	34.76
Std Dev	5.394

**Gaus mean : 35.9909**

**Gaus Width: 4.3057**

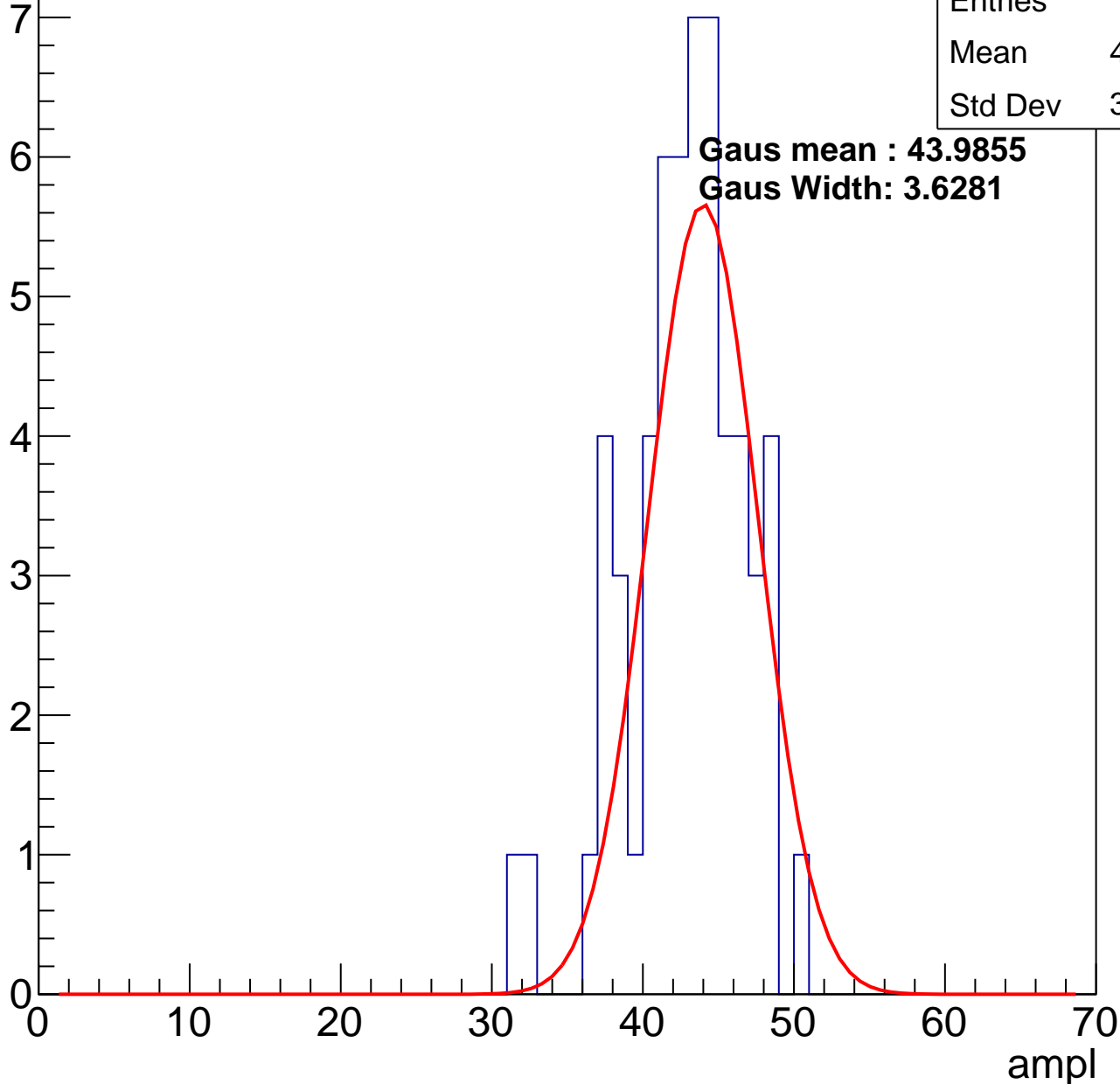


# B1L102S, U5-ch71, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	42.35
Std Dev	3.855

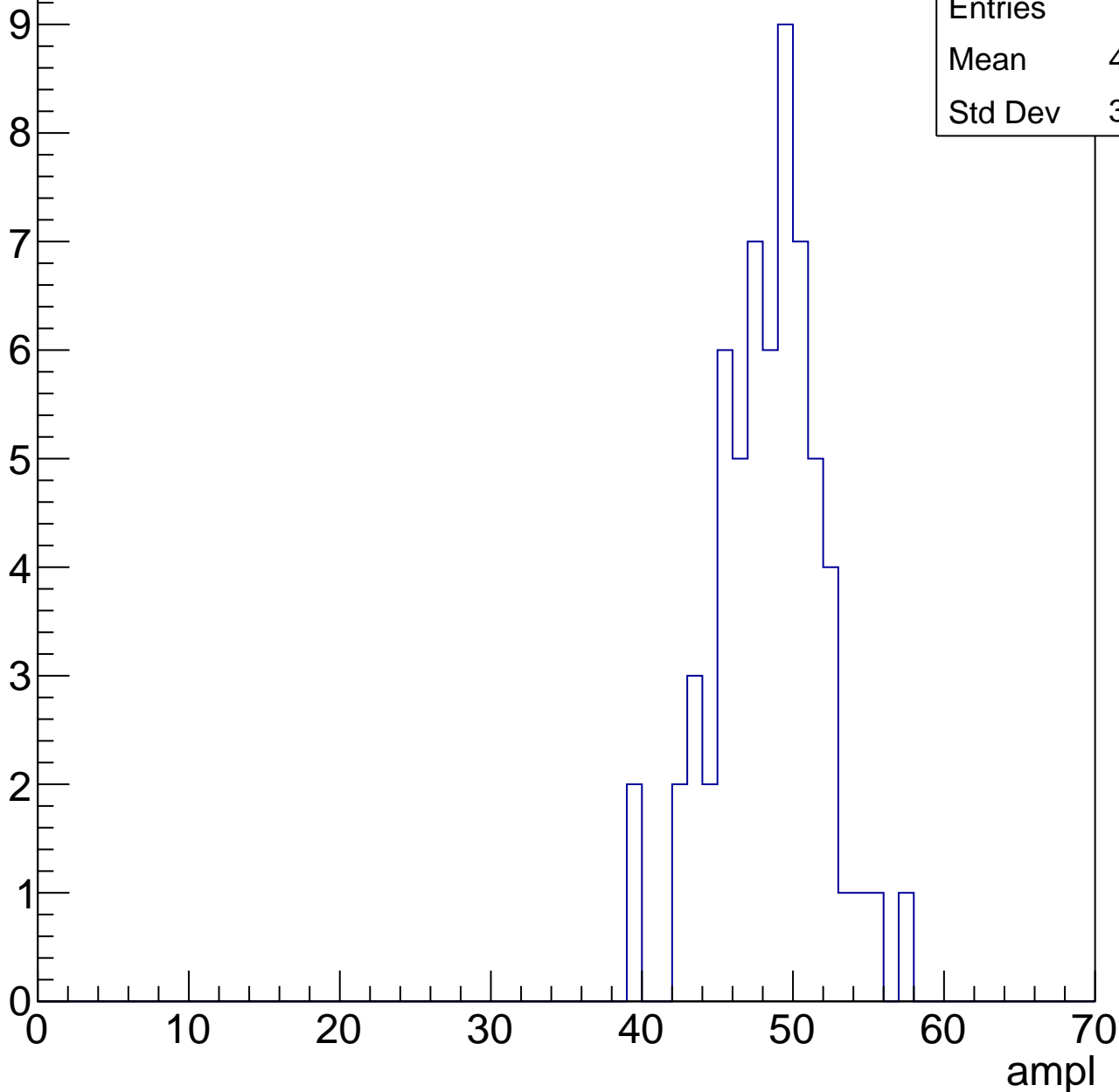


# B1L102S, U5-ch71, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

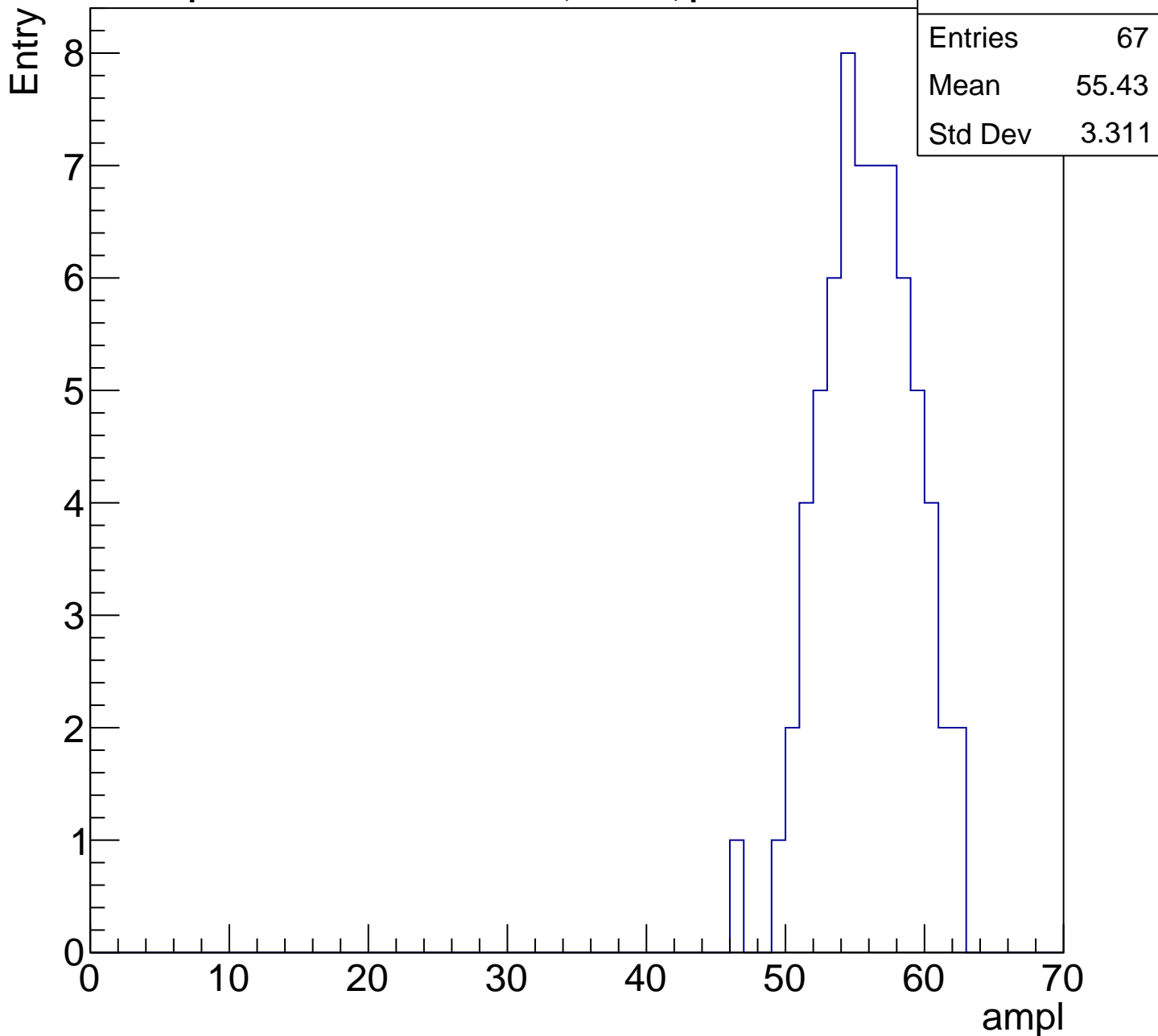
Entry

Entries	62
Mean	47.89
Std Dev	3.497



# B1L102S, U5-ch71, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

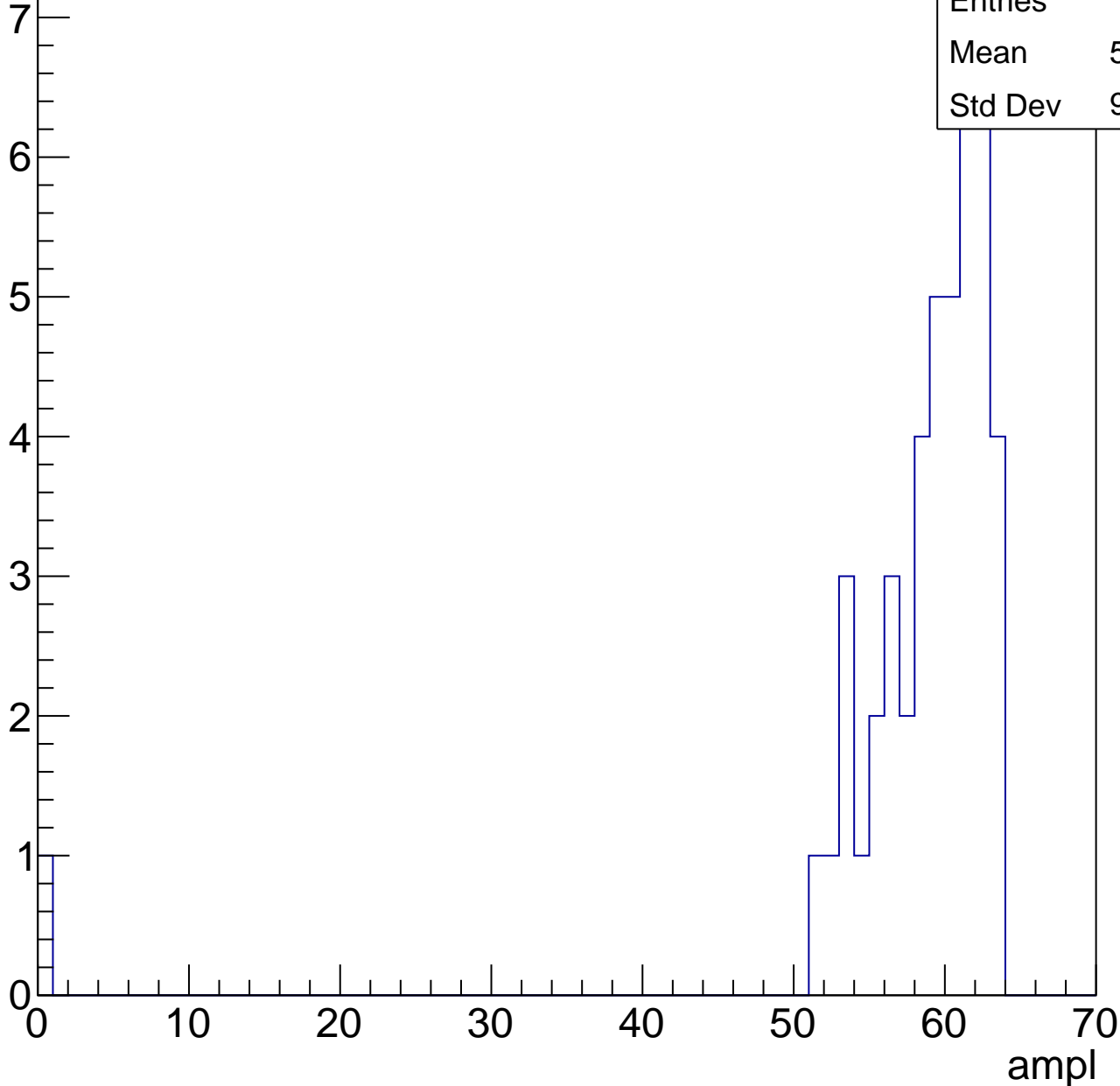


# B1L102S, U5-ch71, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	46
Mean	57.57
Std Dev	9.164

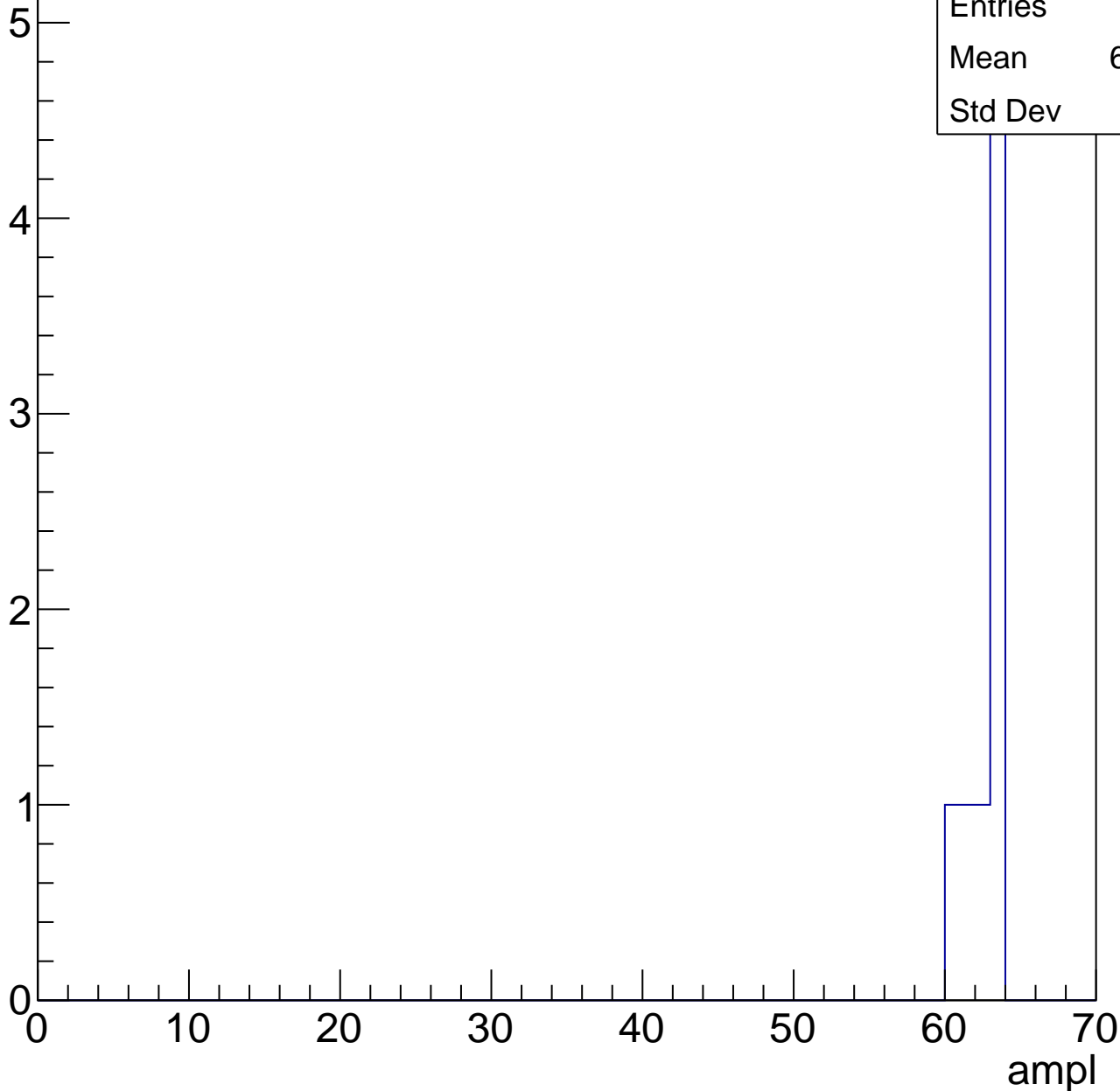


# B1L102S, U5-ch71, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	8
Mean	62.25
Std Dev	1.09





# B1L102S, U5-ch71, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U5-ch72, adc0

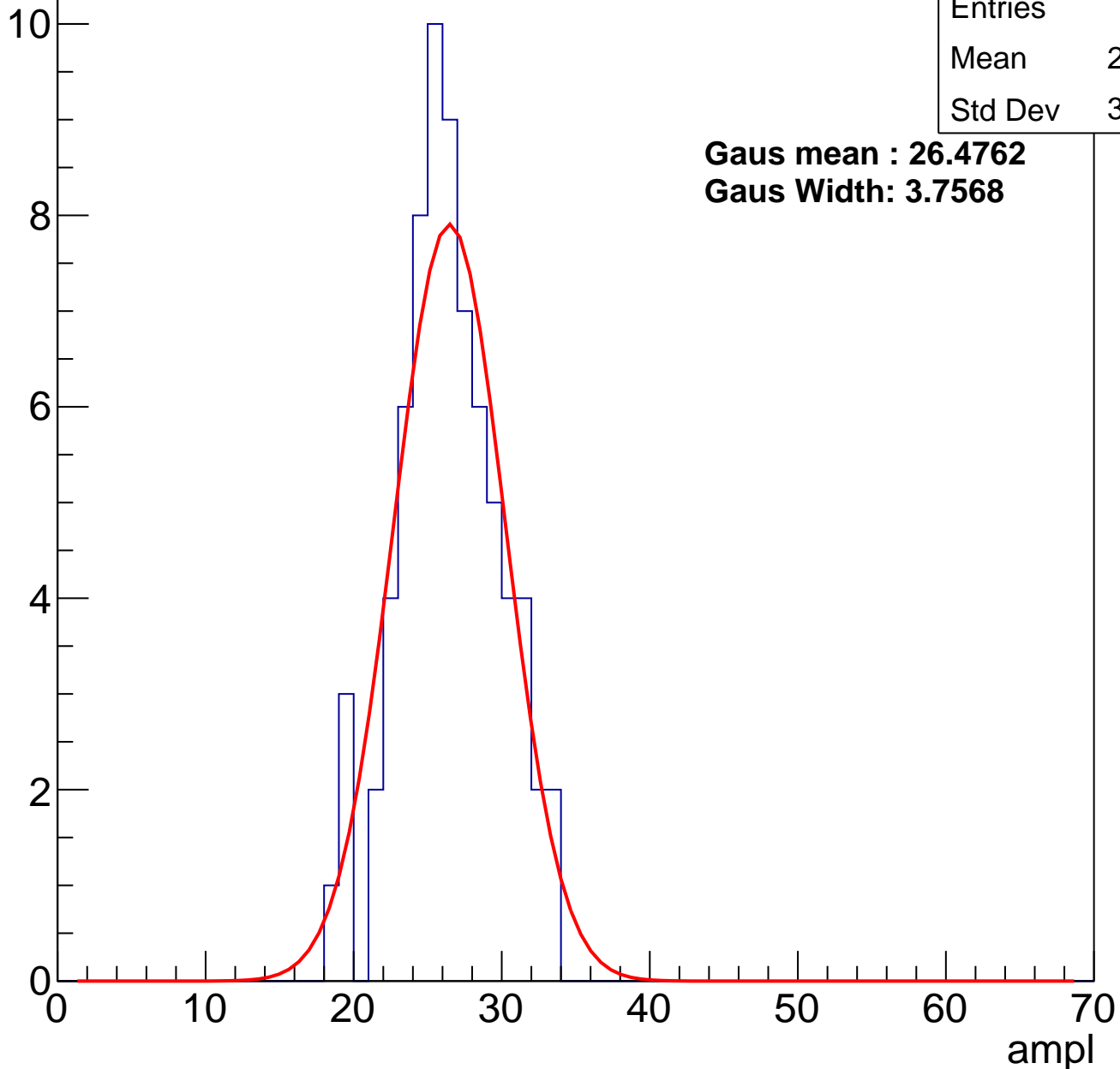
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	73
Mean	25.96
Std Dev	3.374

**Gaus mean : 26.4762**

**Gaus Width: 3.7568**

Entry



# B1L102S, U5-ch72, adc1

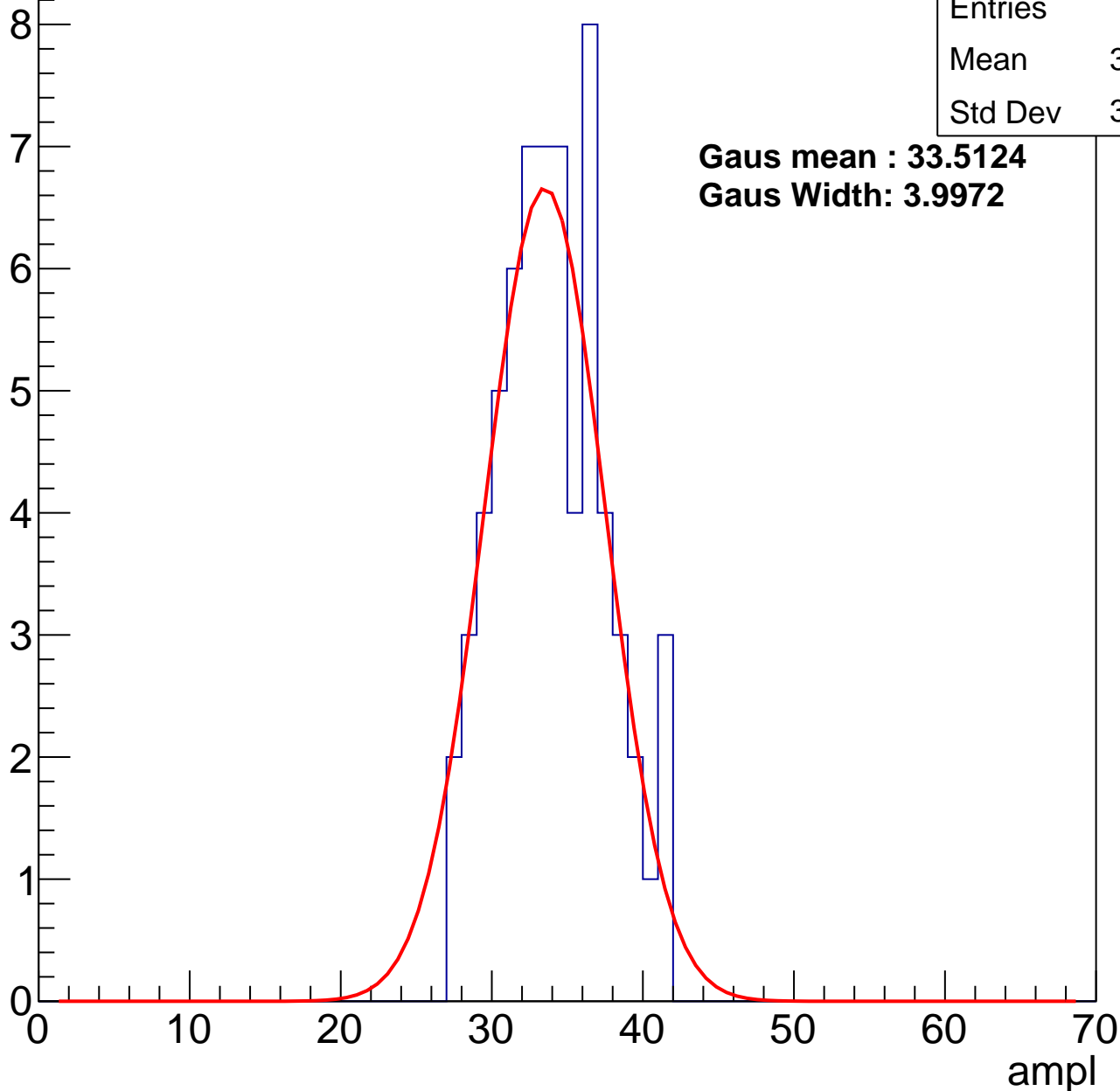
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	33.55
Std Dev	3.513

**Gaus mean : 33.5124**

**Gaus Width: 3.9972**



# B1L102S, U5-ch72, adc2

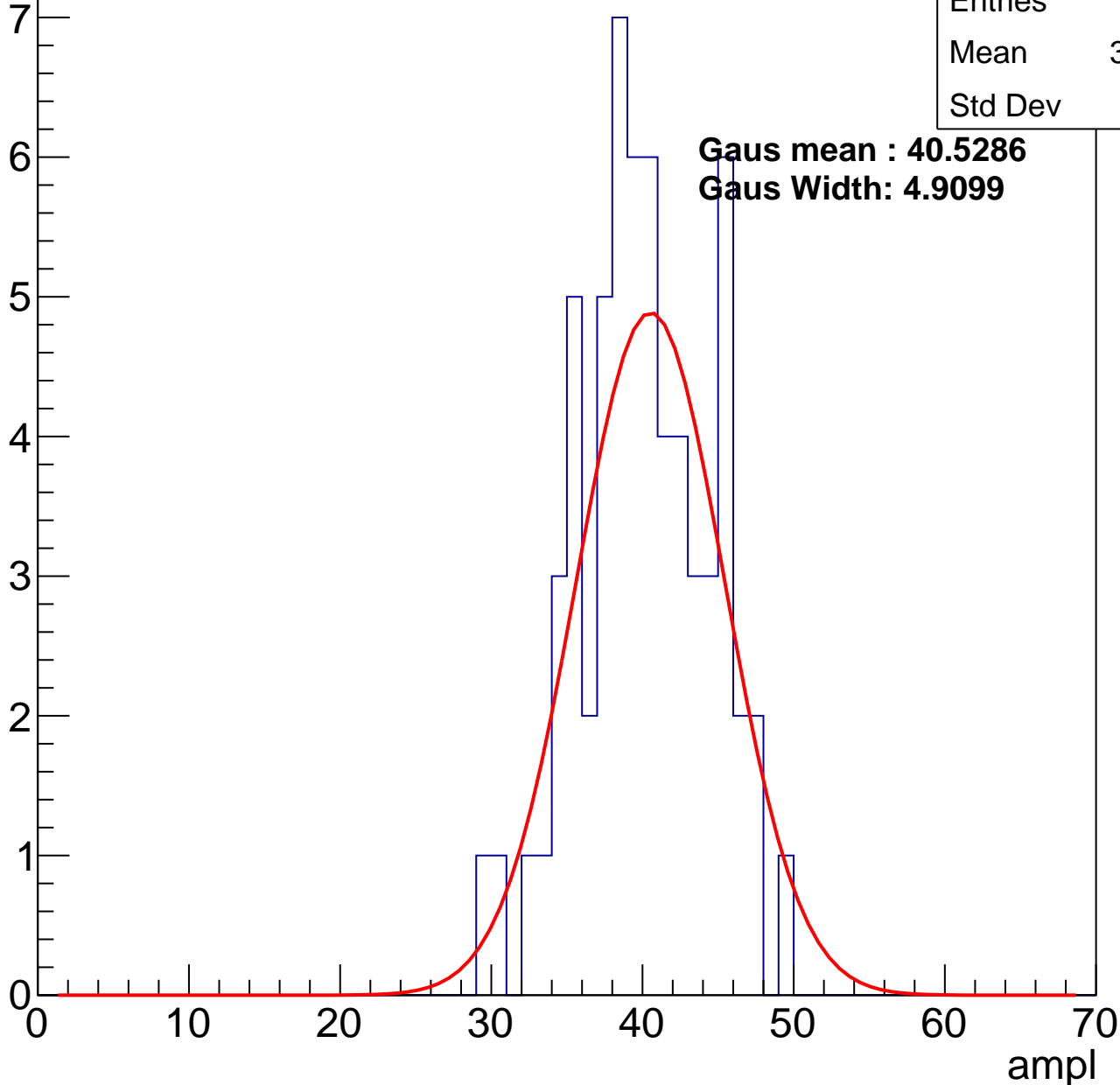
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	39.62
Std Dev	4.3

**Gaus mean : 40.5286**

**Gaus Width: 4.9099**

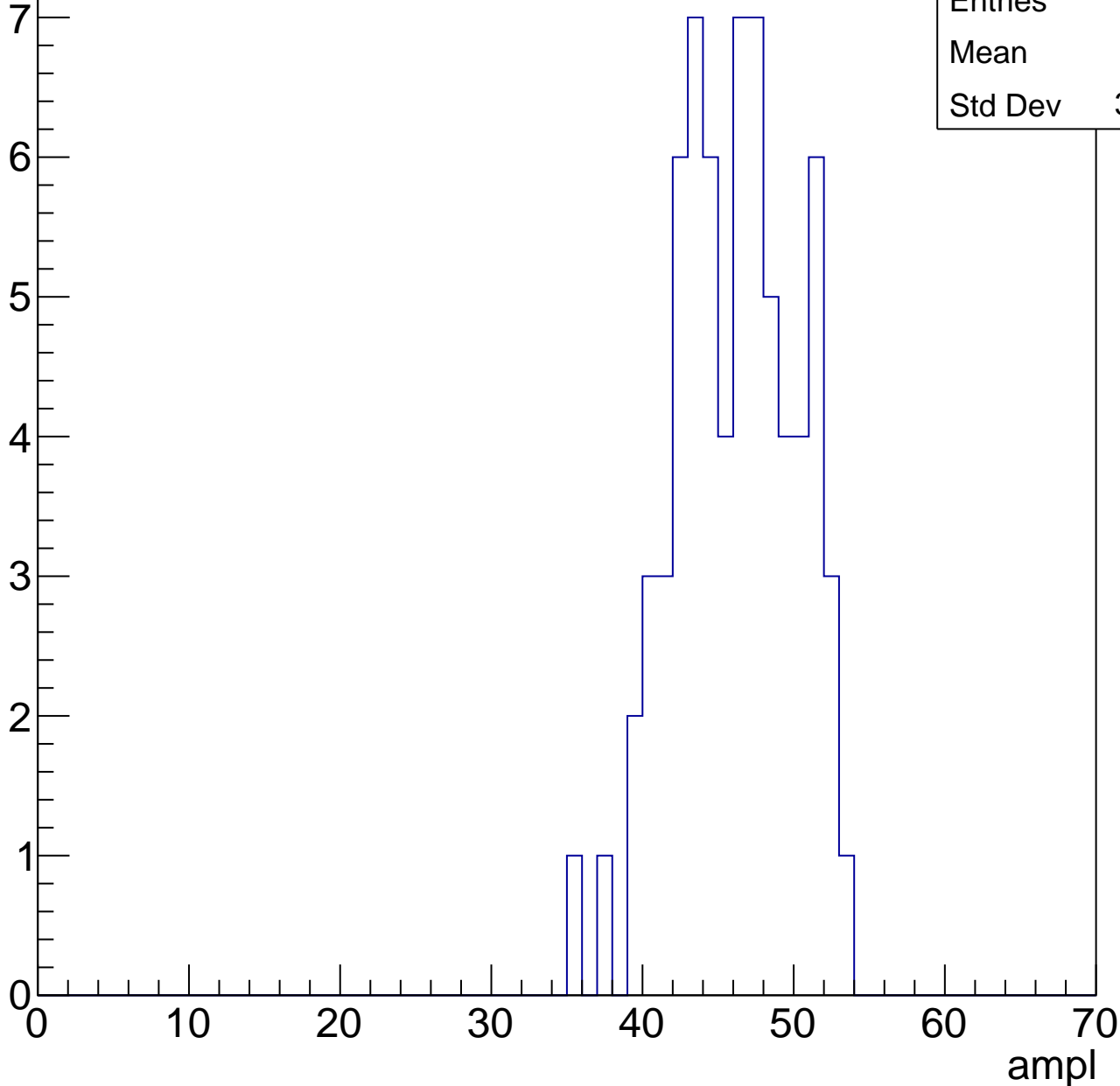


# B1L102S, U5-ch72, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	45.6
Std Dev	3.951

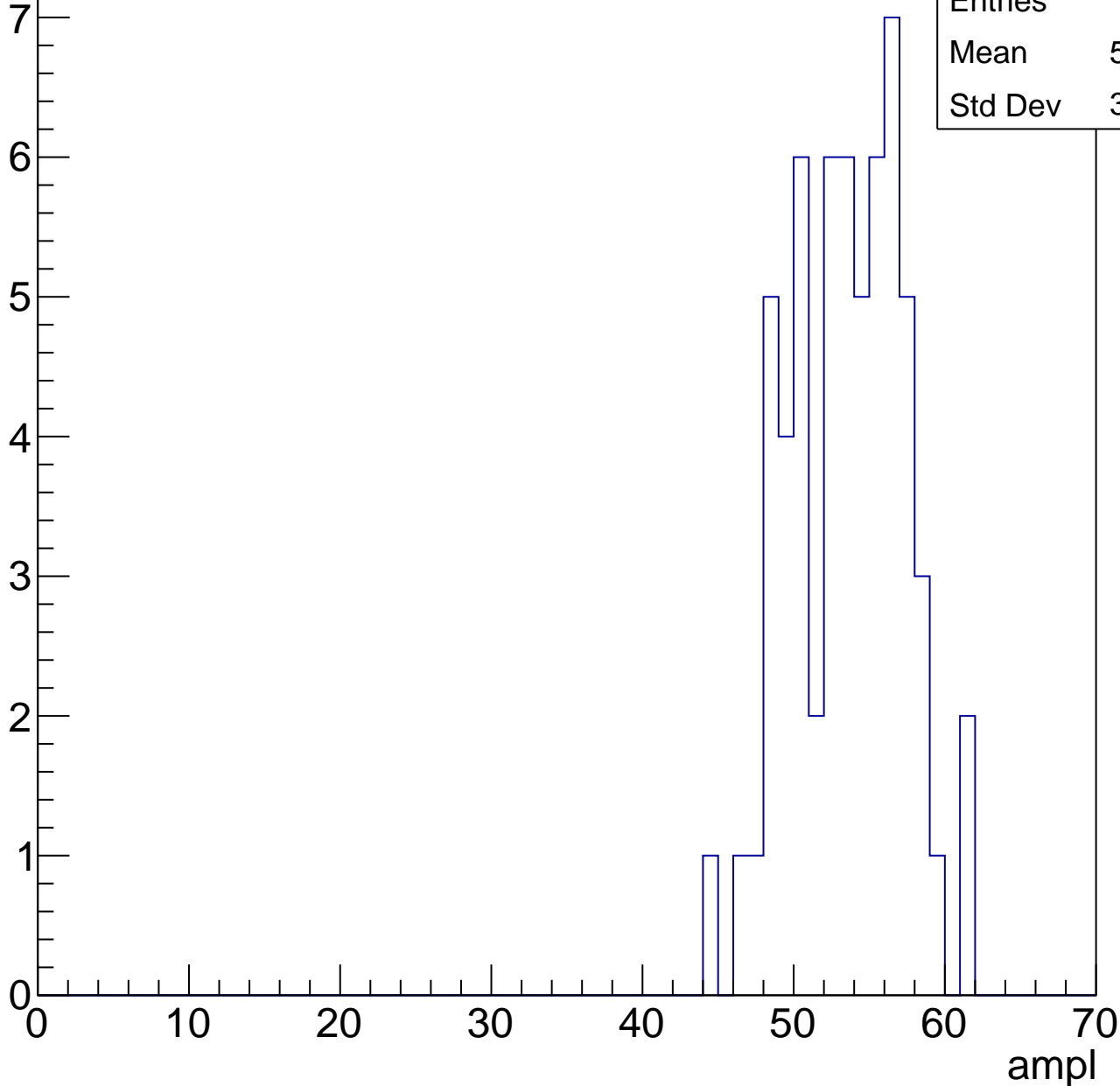


# B1L102S, U5-ch72, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	53.07
Std Dev	3.697

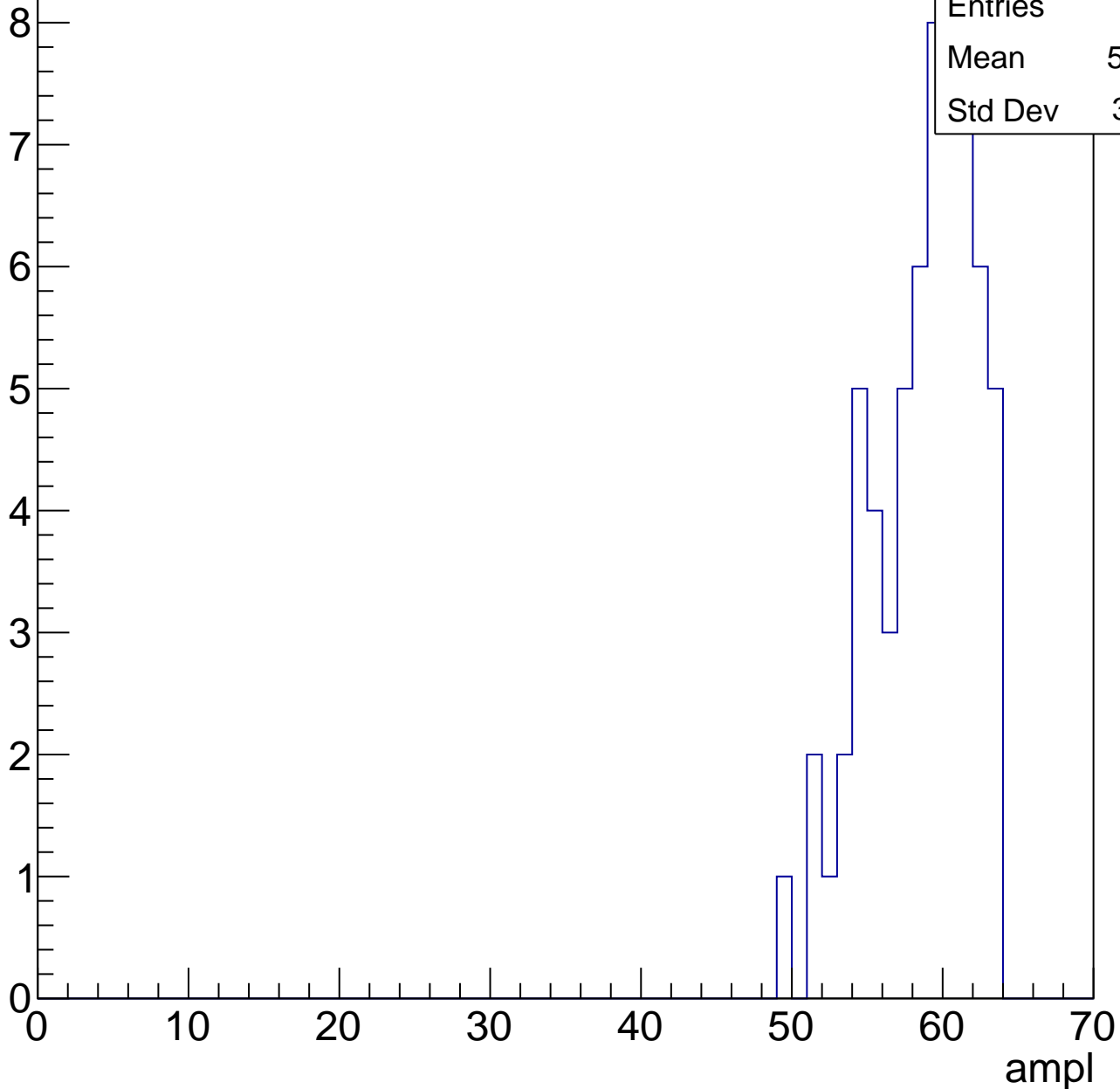


# B1L102S, U5-ch72, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

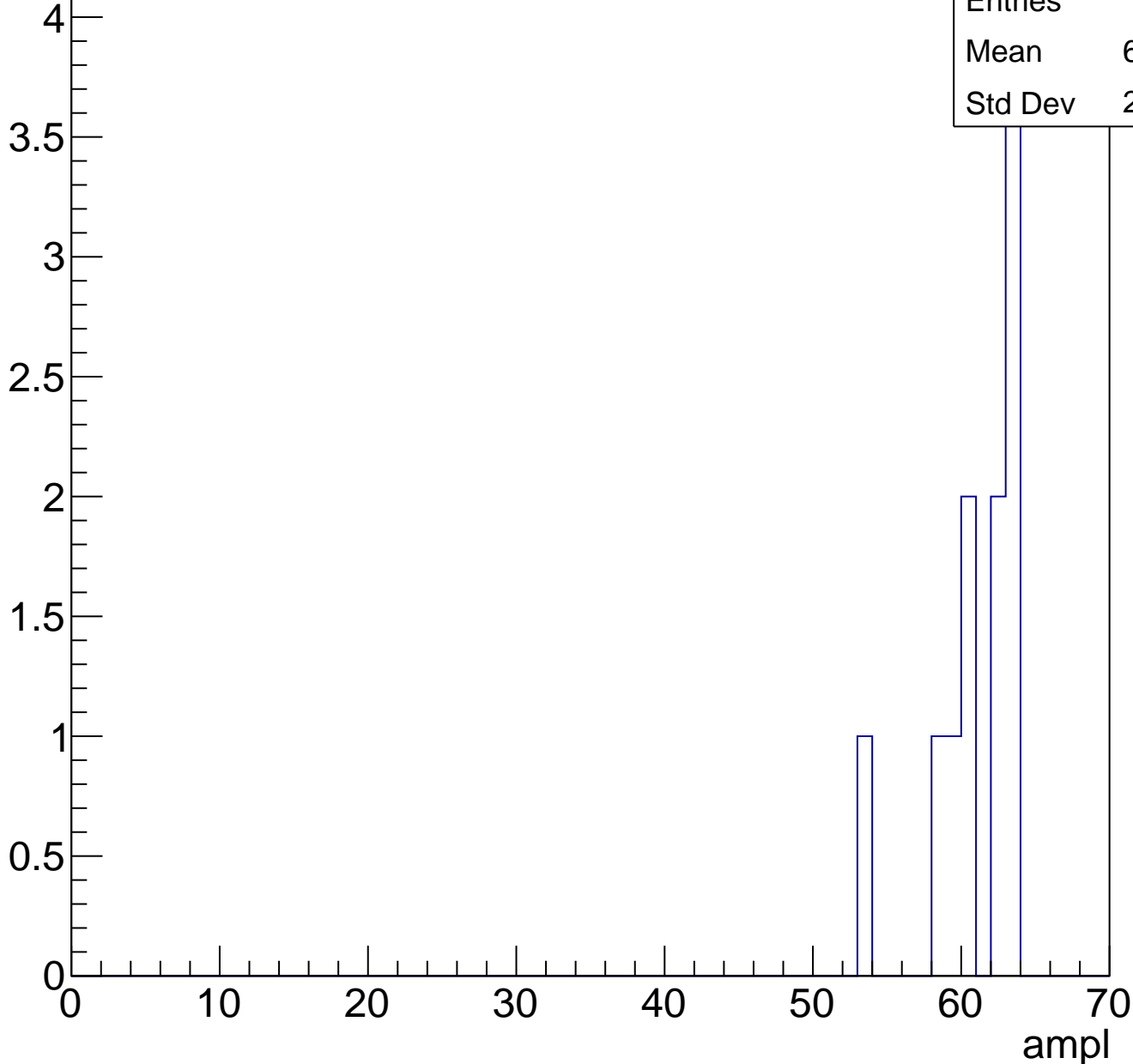
Entries	64
Mean	58.23
Std Dev	3.371



# B1L102S, U5-ch72, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

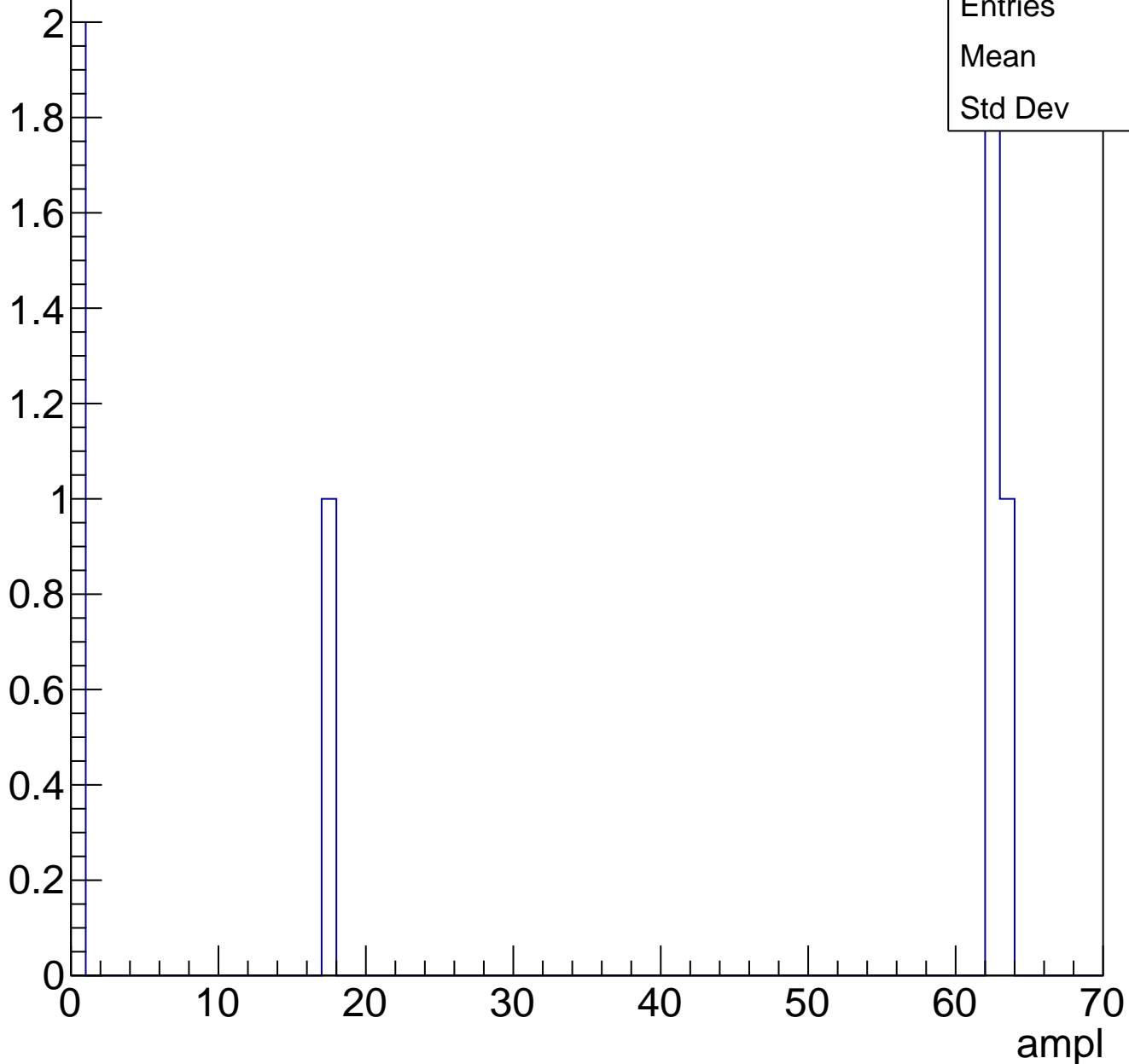




# B1L102S, U5-ch72, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U5-ch73, adc0

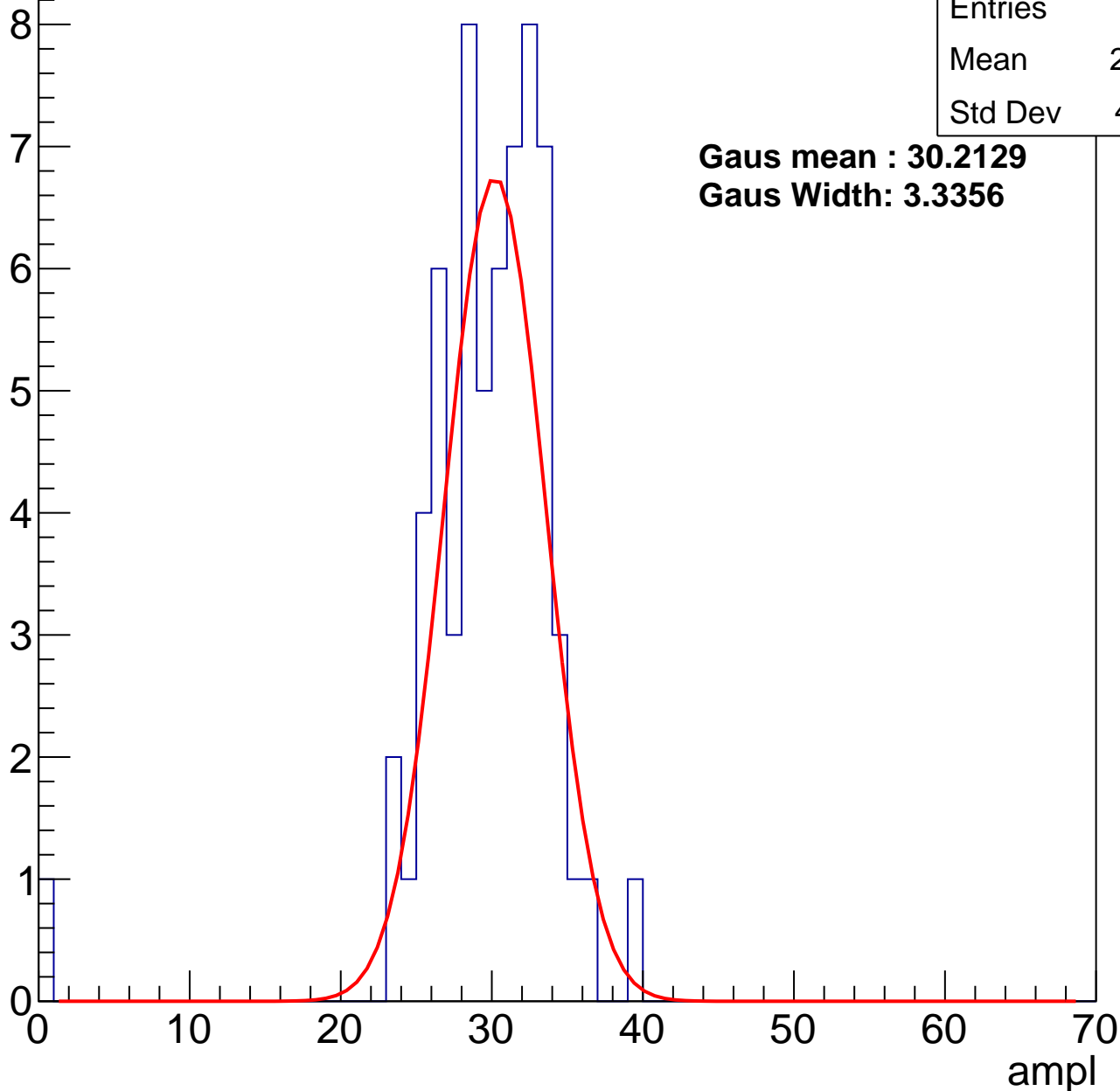
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	29.25
Std Dev	4.921

**Gaus mean : 30.2129**

**Gaus Width: 3.3356**



# B1L102S, U5-ch73, adc1

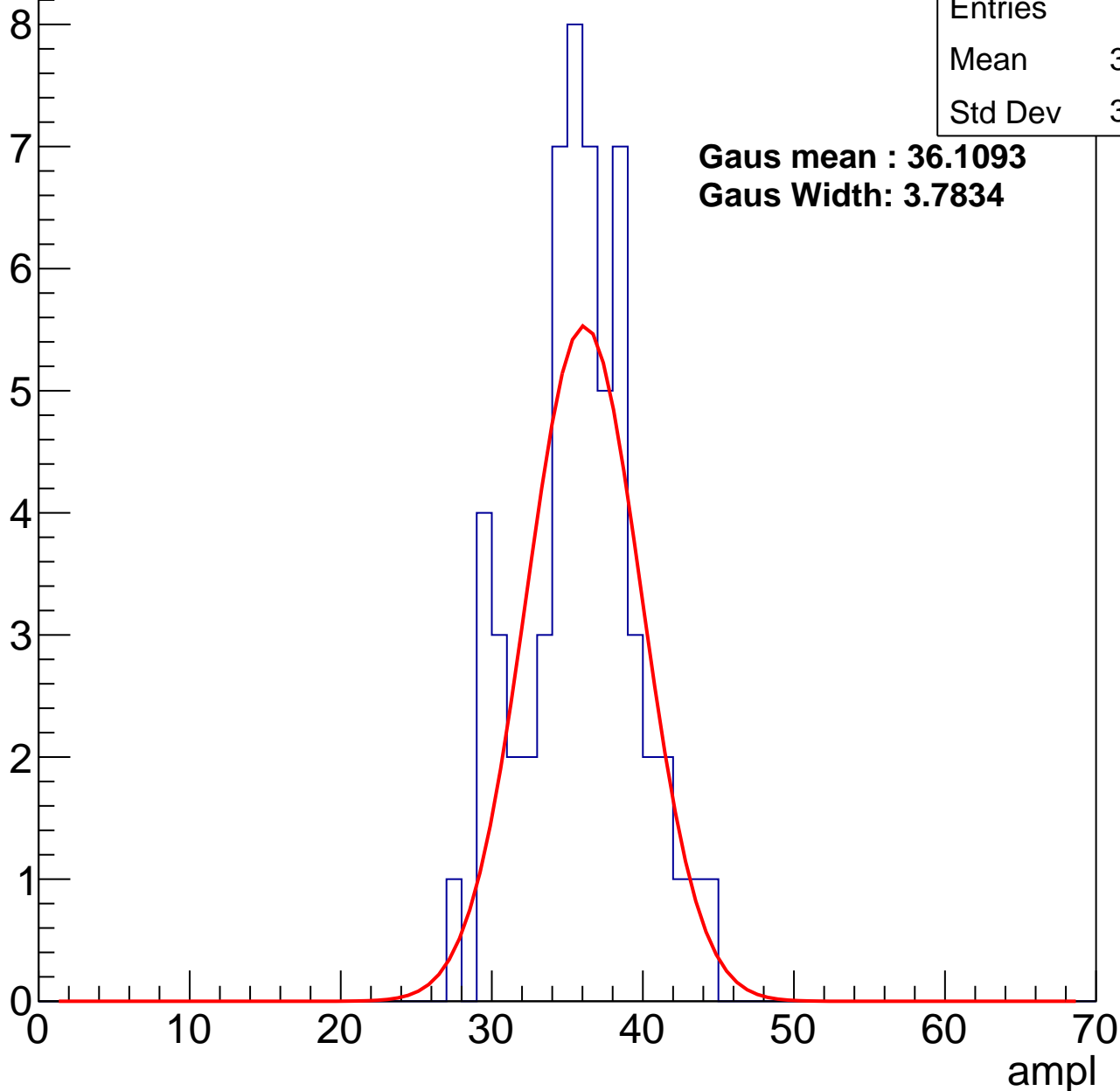
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	35.37
Std Dev	3.677

**Gaus mean : 36.1093**

**Gaus Width: 3.7834**



# B1L102S, U5-ch73, adc2

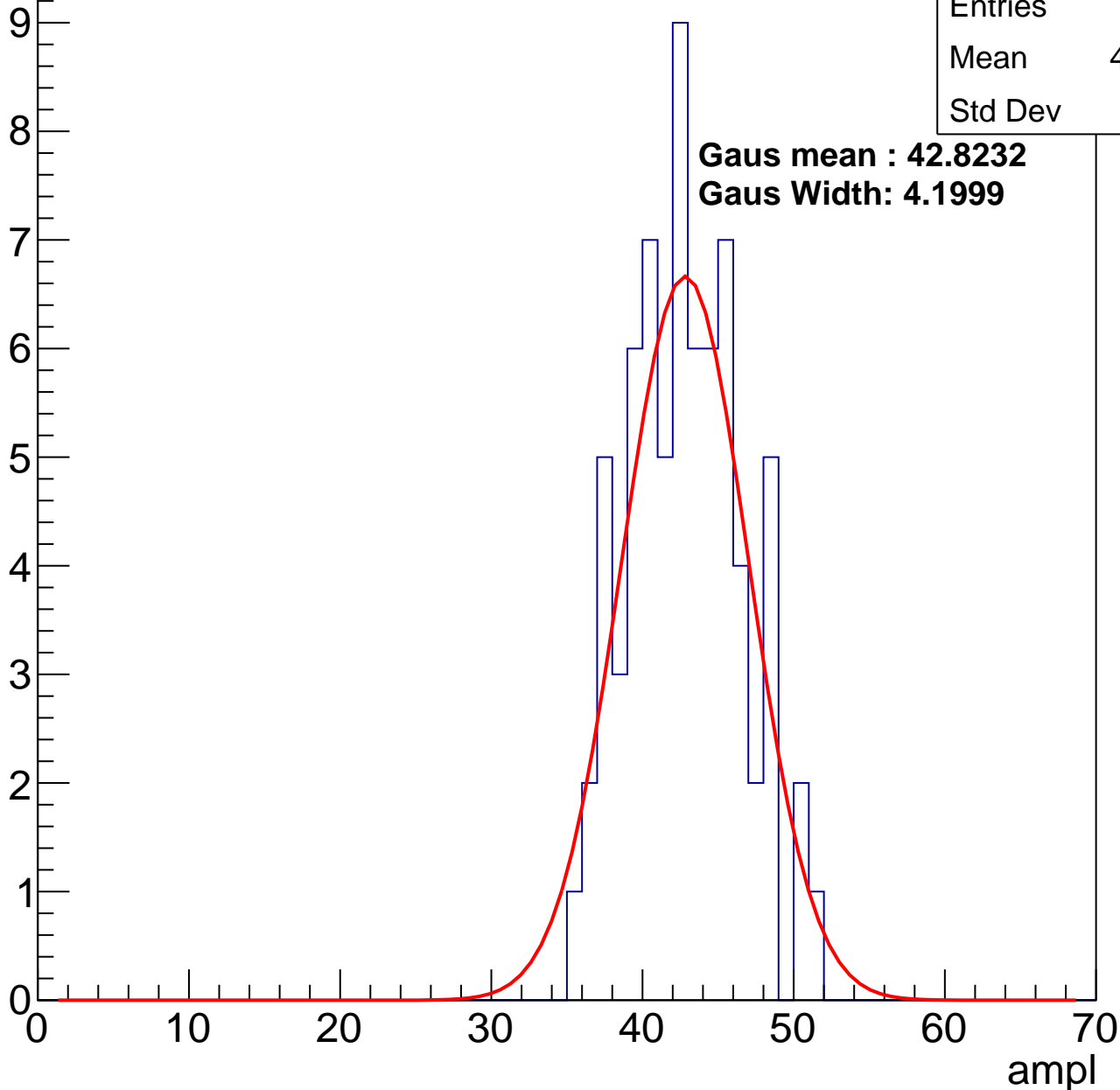
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	42.38
Std Dev	3.69

**Gaus mean : 42.8232**

**Gaus Width: 4.1999**

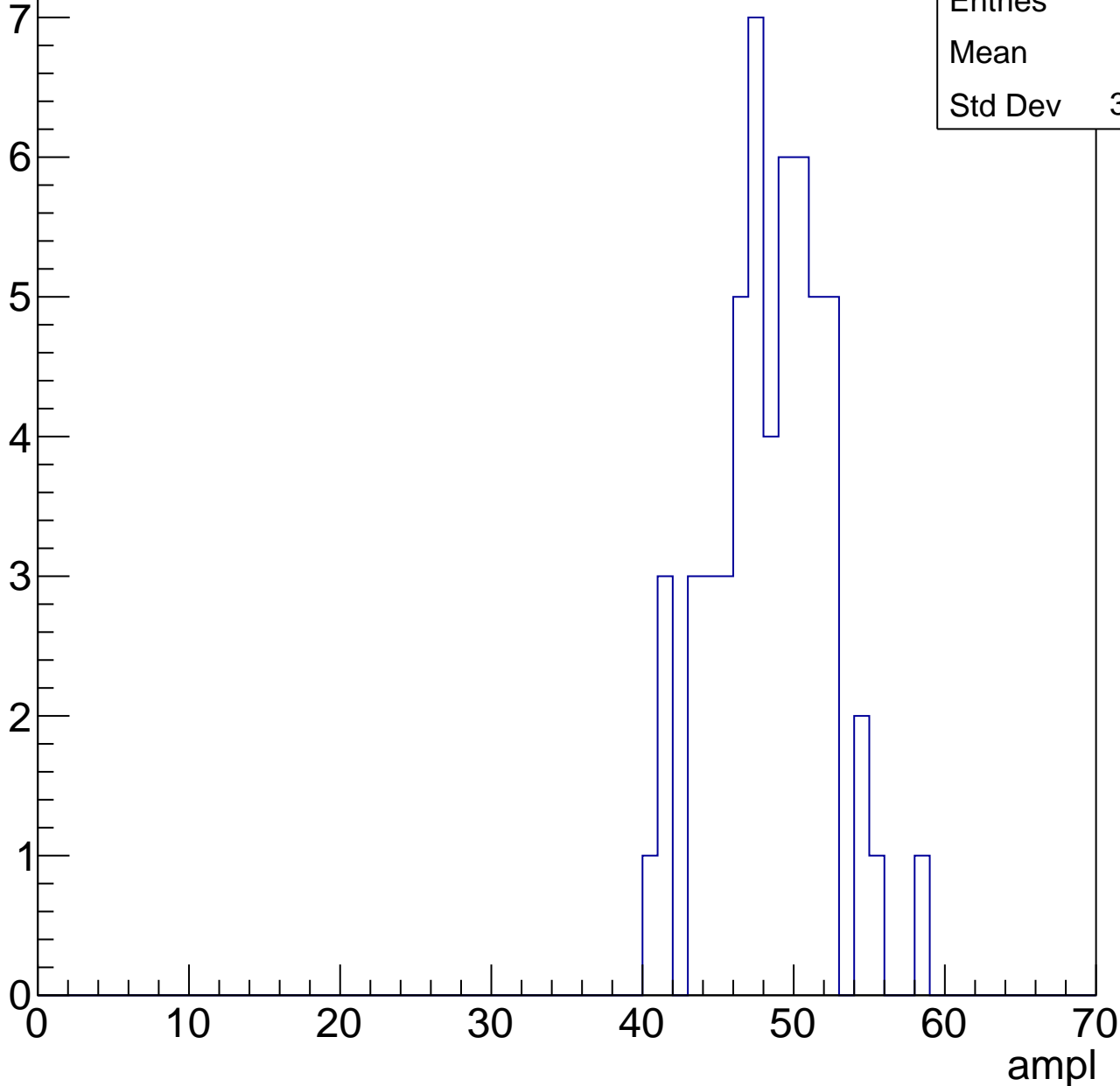


# B1L102S, U5-ch73, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

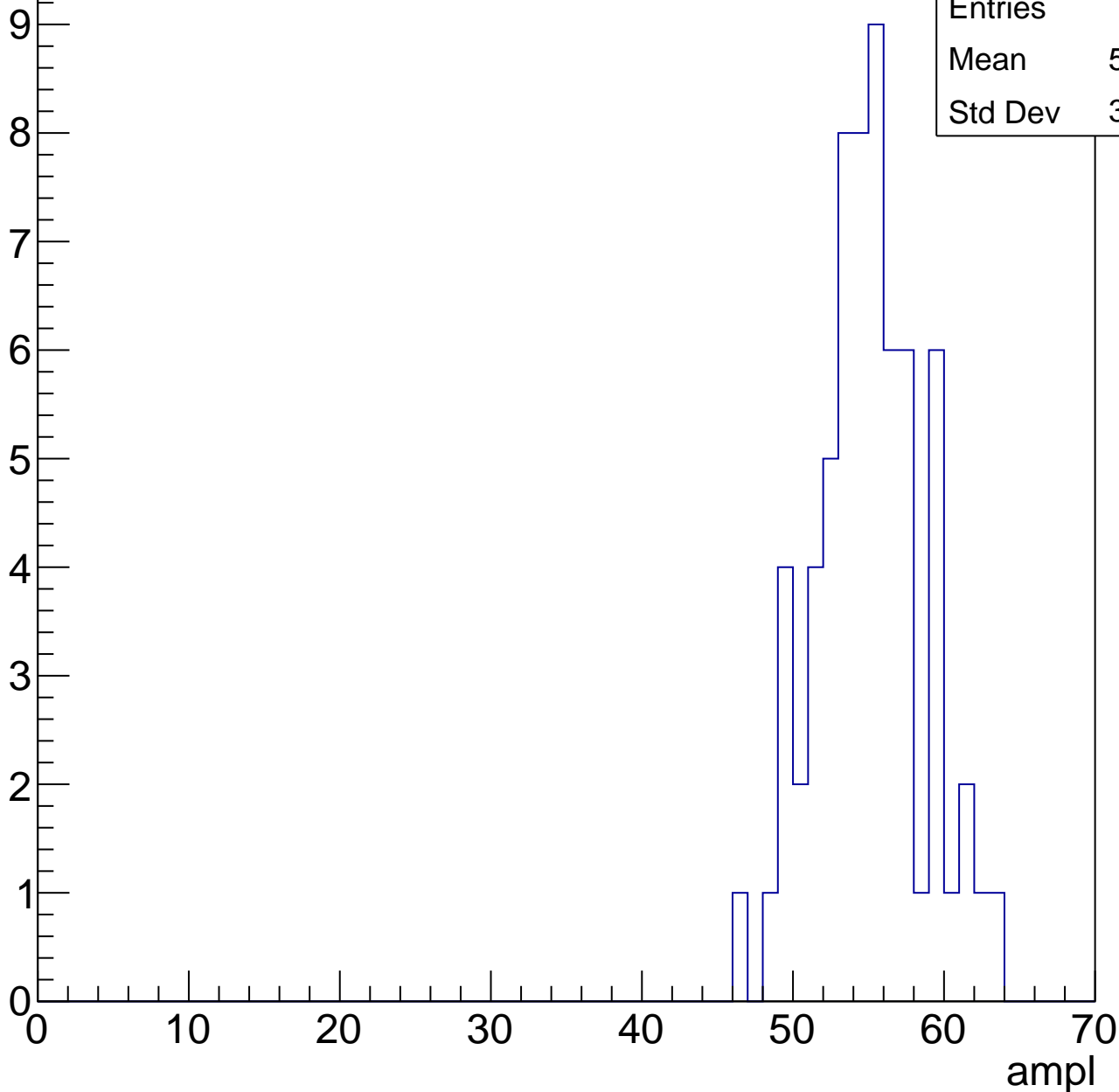
Entries	55
Mean	48
Std Dev	3.727



# B1L102S, U5-ch73, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

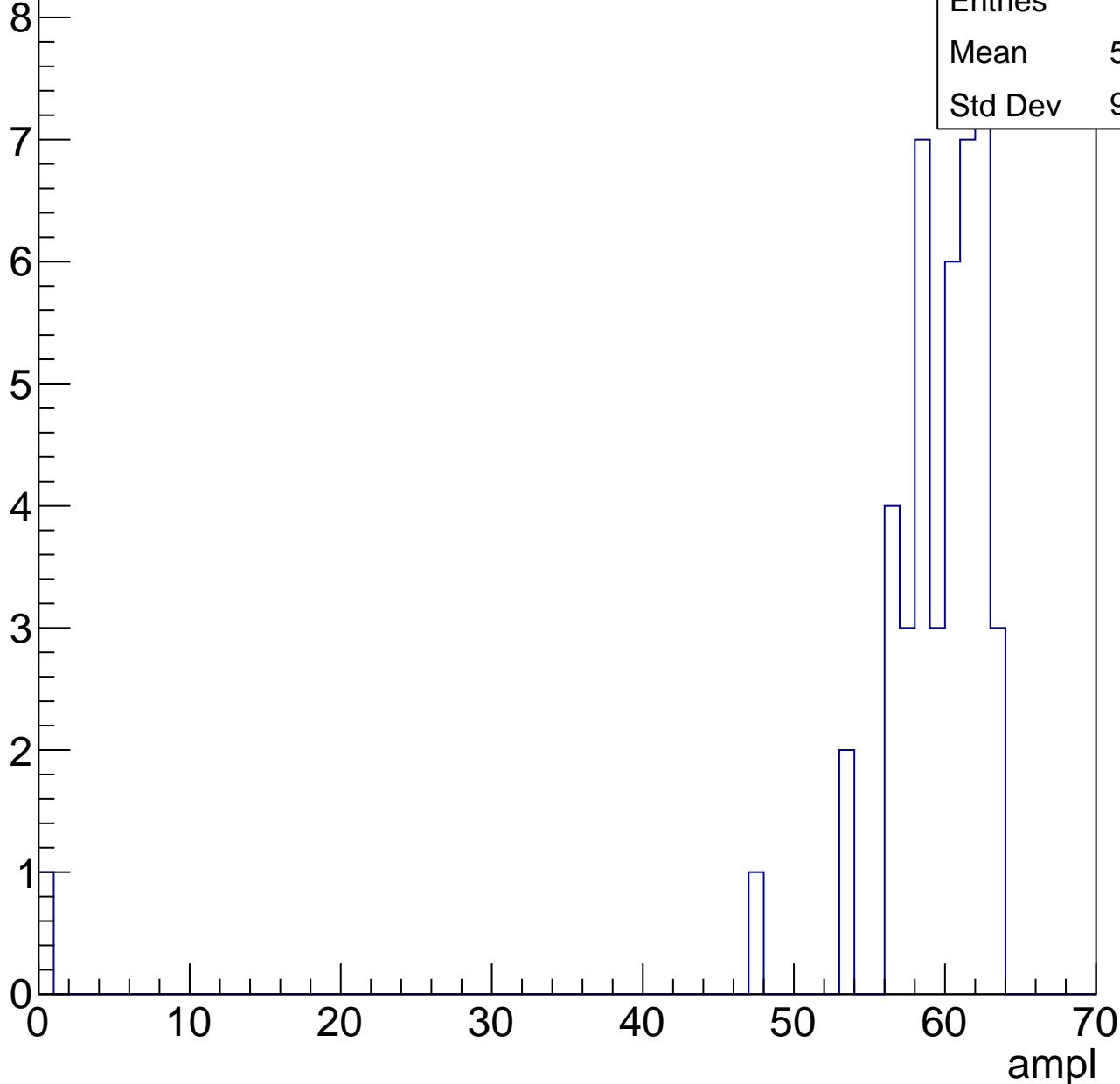


# B1L102S, U5-ch73, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	45
Mean	57.84
Std Dev	9.245



# B1L102S, U5-ch73, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries	11
Mean	60.55
Std Dev	1.971



# B1L102S, U5-ch73, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U5-ch74, adc0

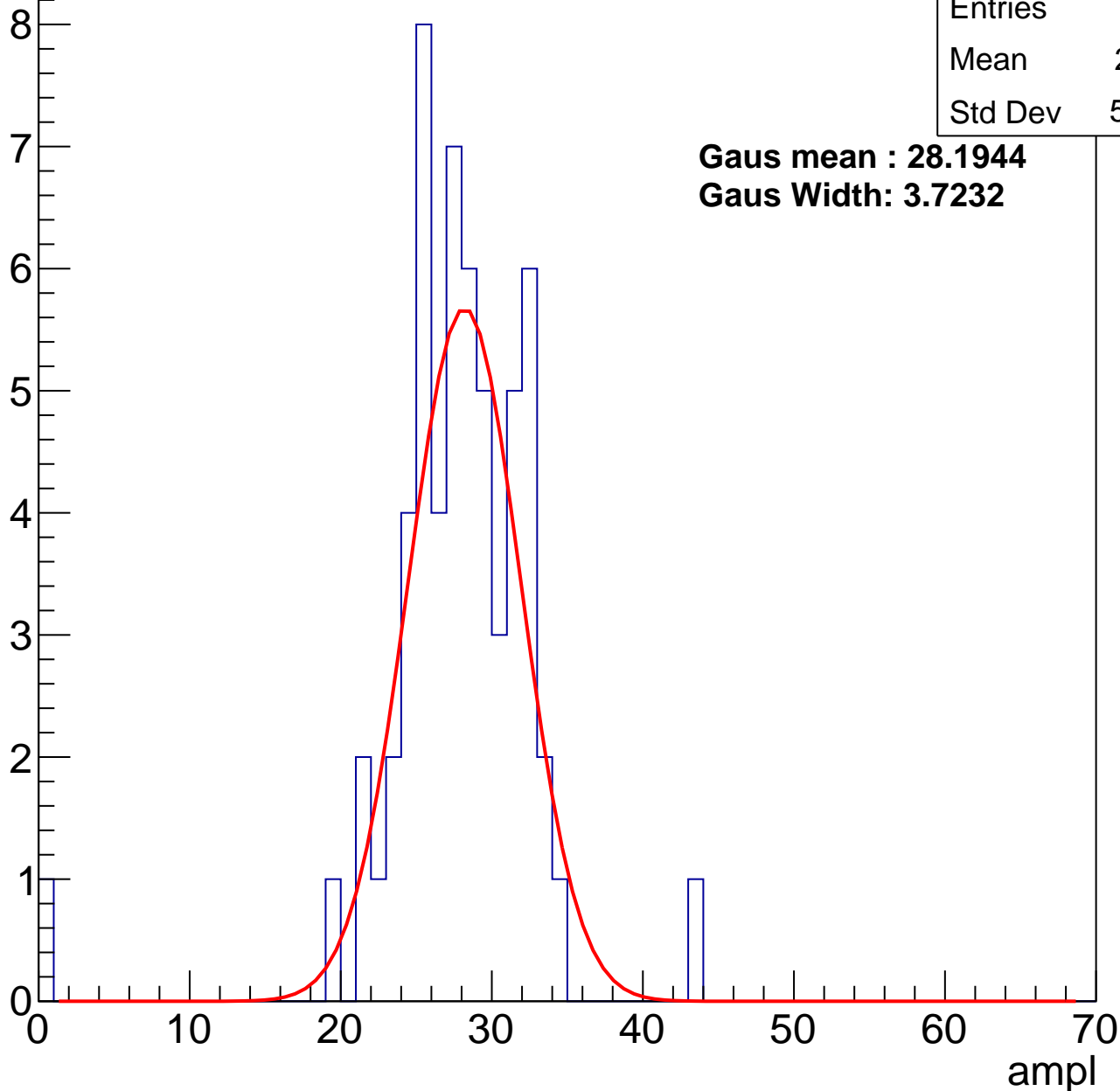
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	27.31
Std Dev	5.286

**Gaus mean : 28.1944**

**Gaus Width: 3.7232**



# B1L102S, U5-ch74, adc1

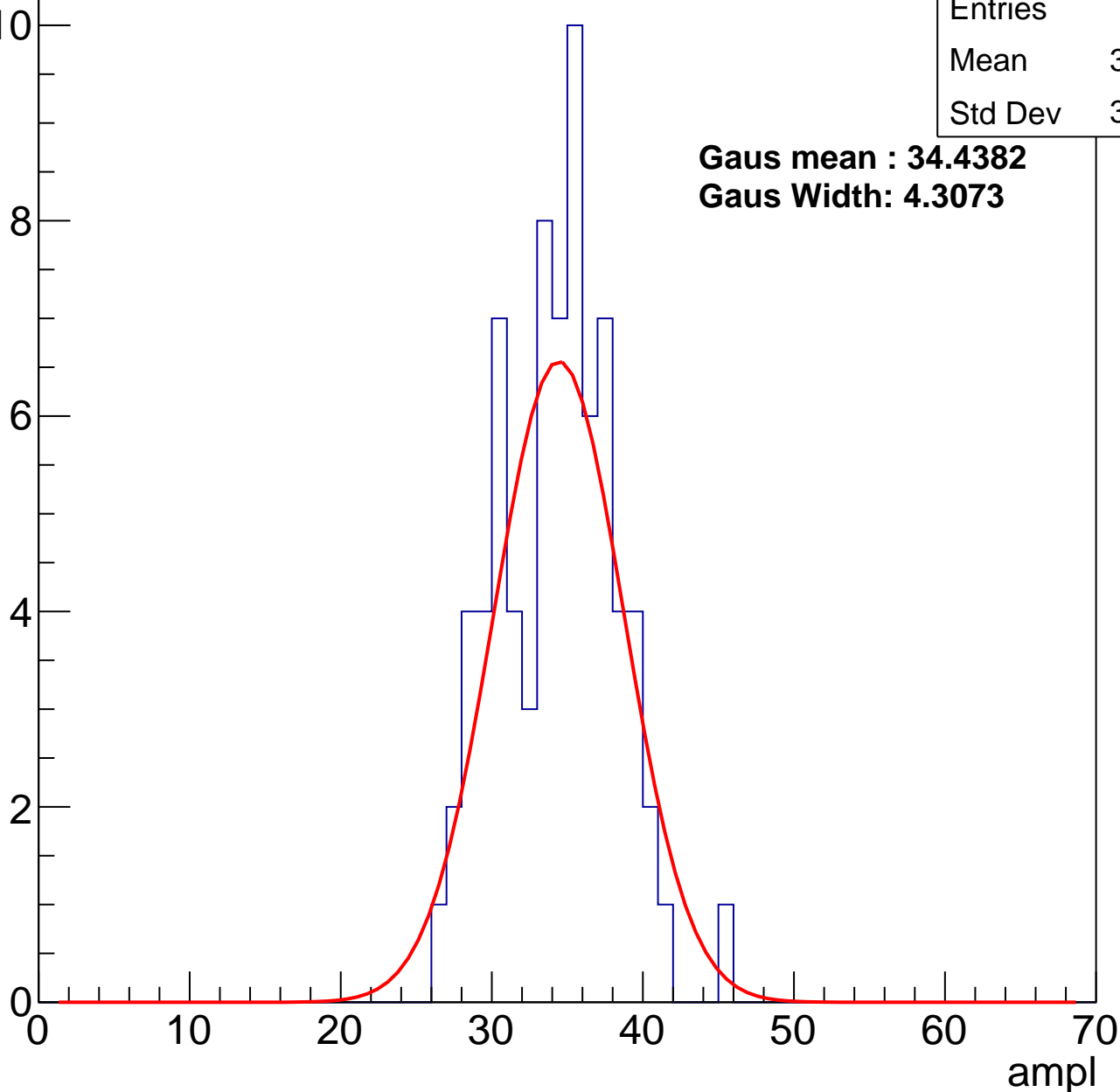
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	33.85
Std Dev	3.787

**Gaus mean : 34.4382**

**Gaus Width: 4.3073**



# B1L102S, U5-ch74, adc2

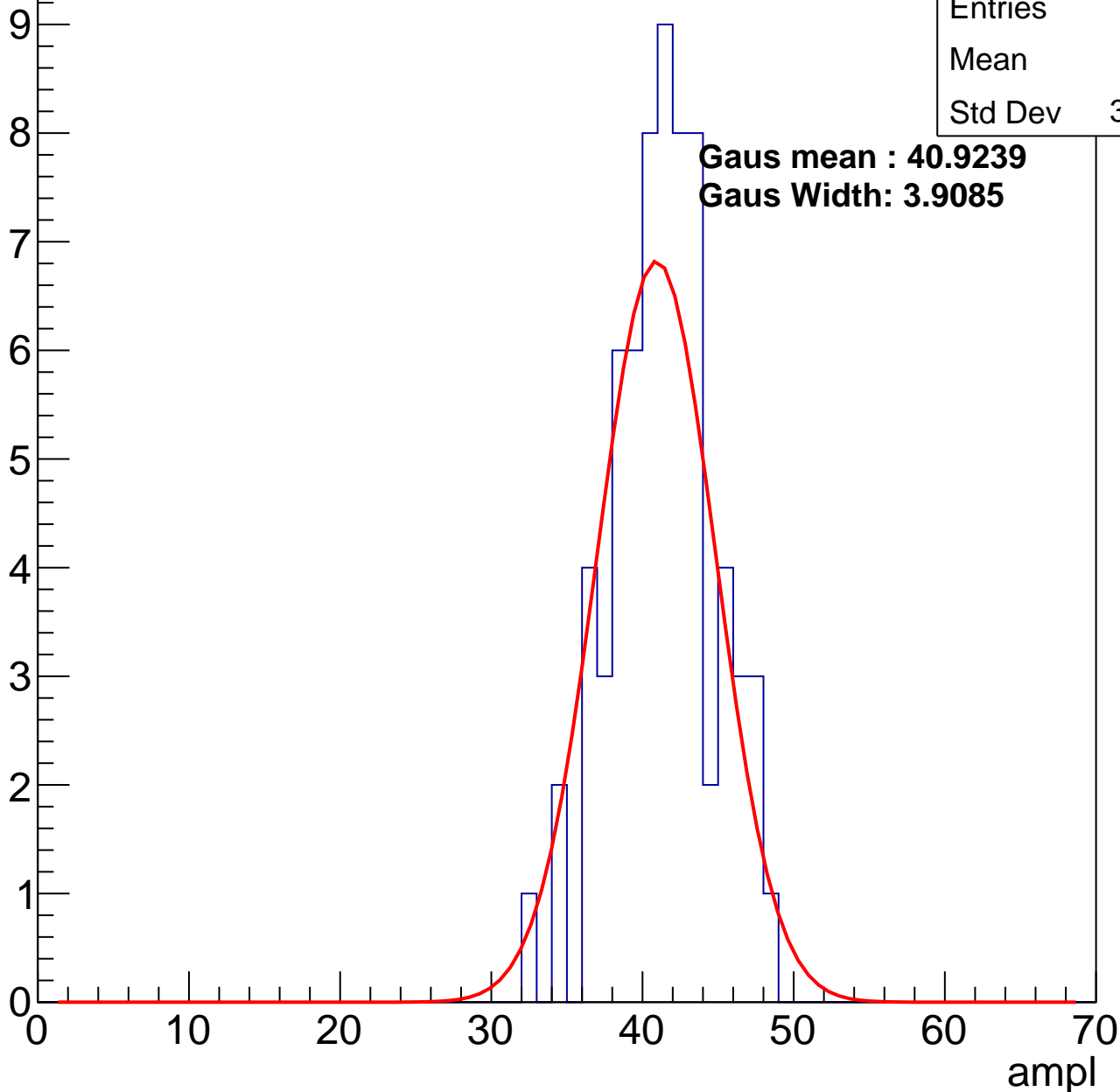
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	40.9
Std Dev	3.357

**Gaus mean : 40.9239**

**Gaus Width: 3.9085**

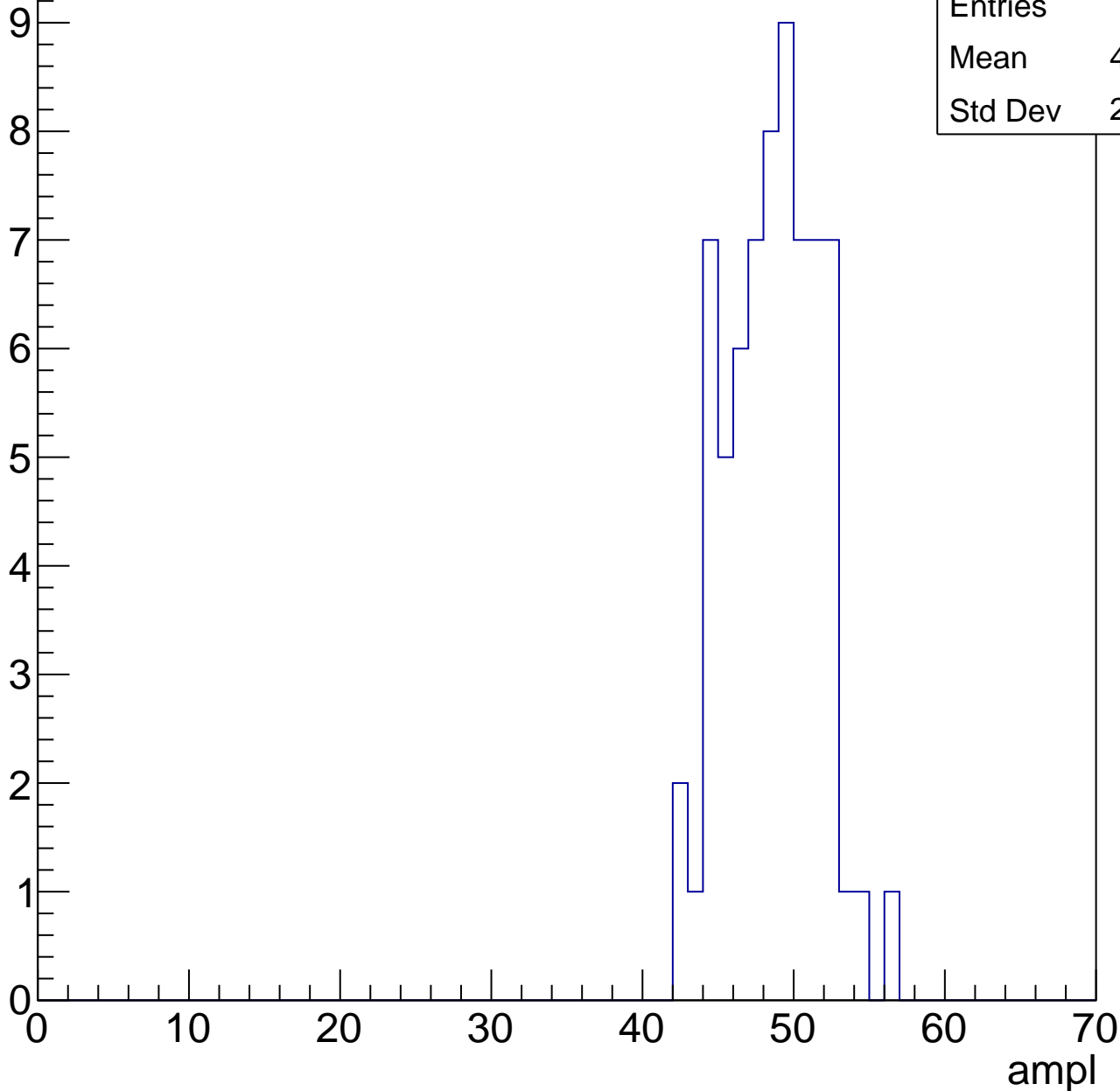


# B1L102S, U5-ch74, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

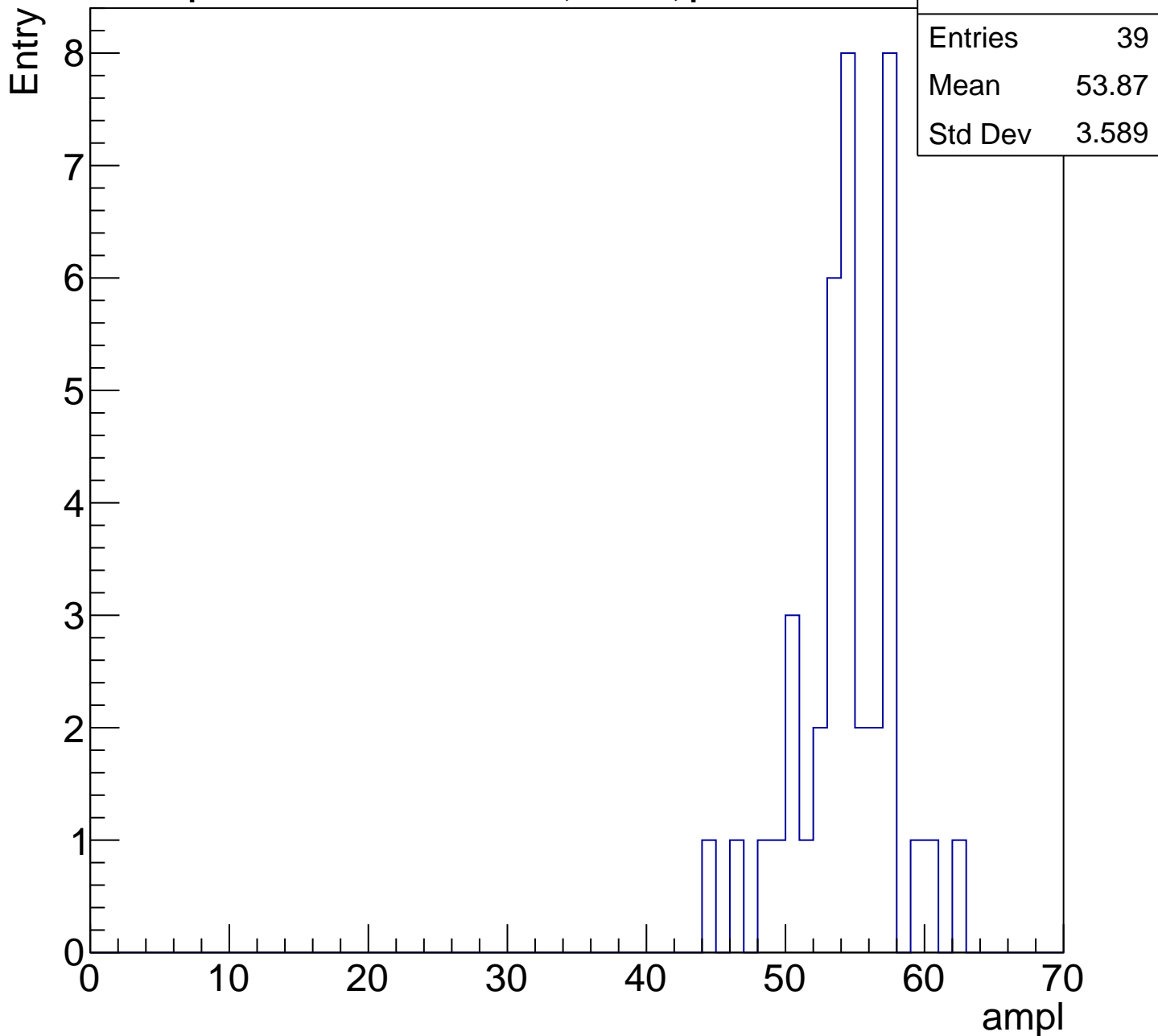
Entry

Entries	69
Mean	48.17
Std Dev	2.997



# B1L102S, U5-ch74, adc4

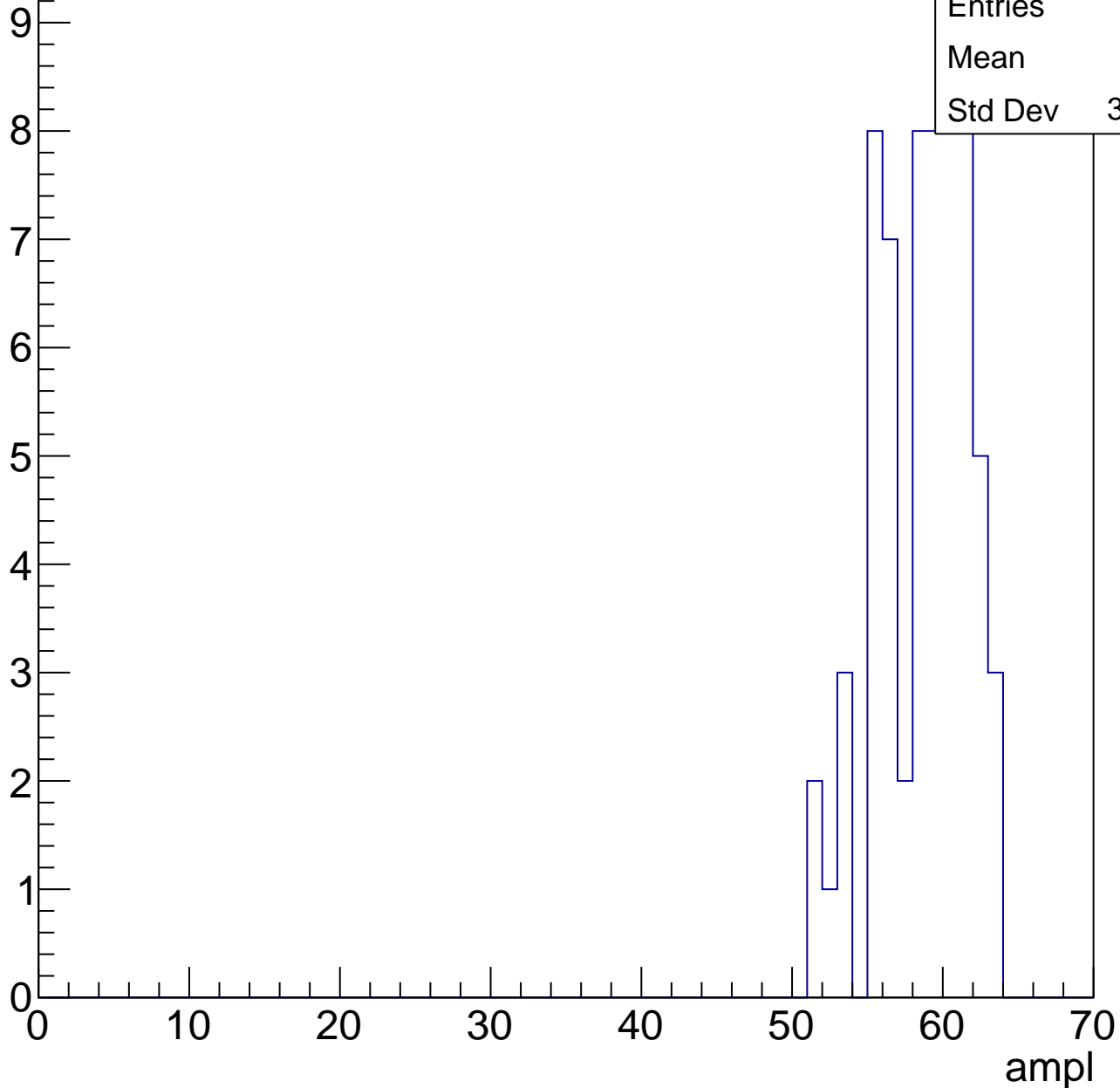
calib\_packv5\_042523\_0143.root, FC#11, port A2



# B1L102S, U5-ch74, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

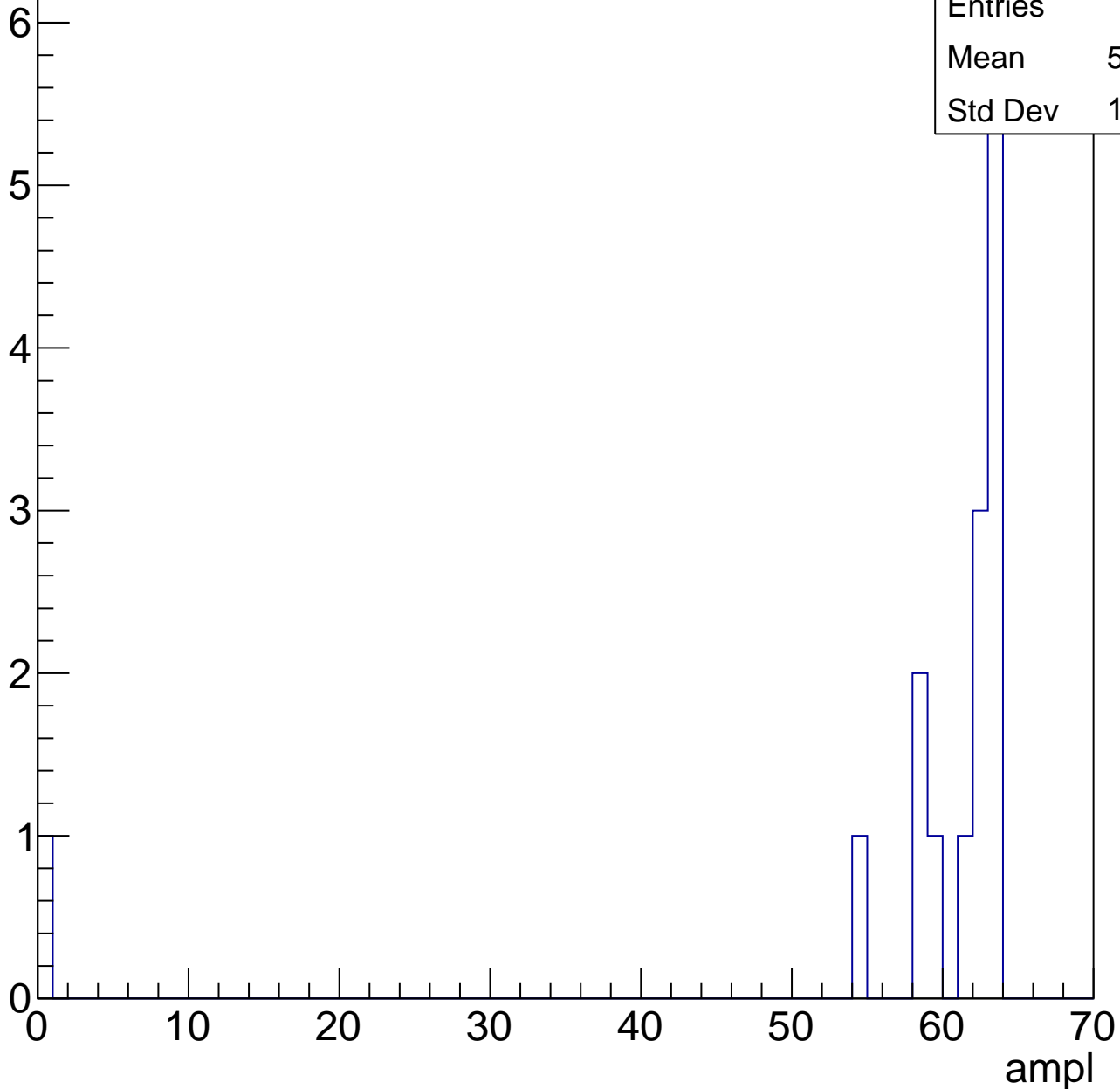


# B1L102S, U5-ch74, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	15
Mean	56.93
Std Dev	15.43





# B1L102S, U5-ch74, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U5-ch75, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	93
Mean	29
Std Dev	6.733

**Gaus mean : 30.1705**

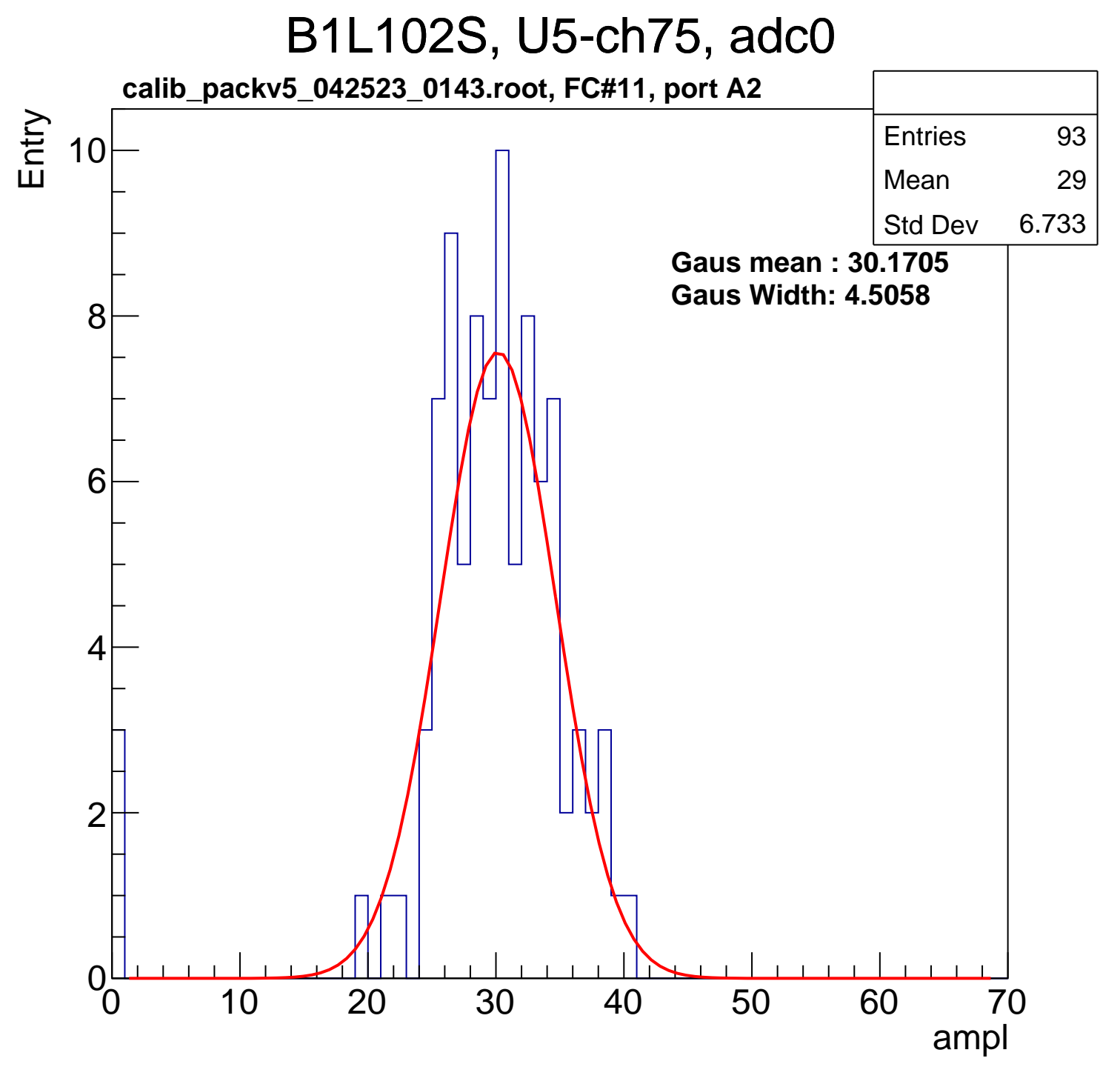
**Gaus Width: 4.5058**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U5-ch75, adc1

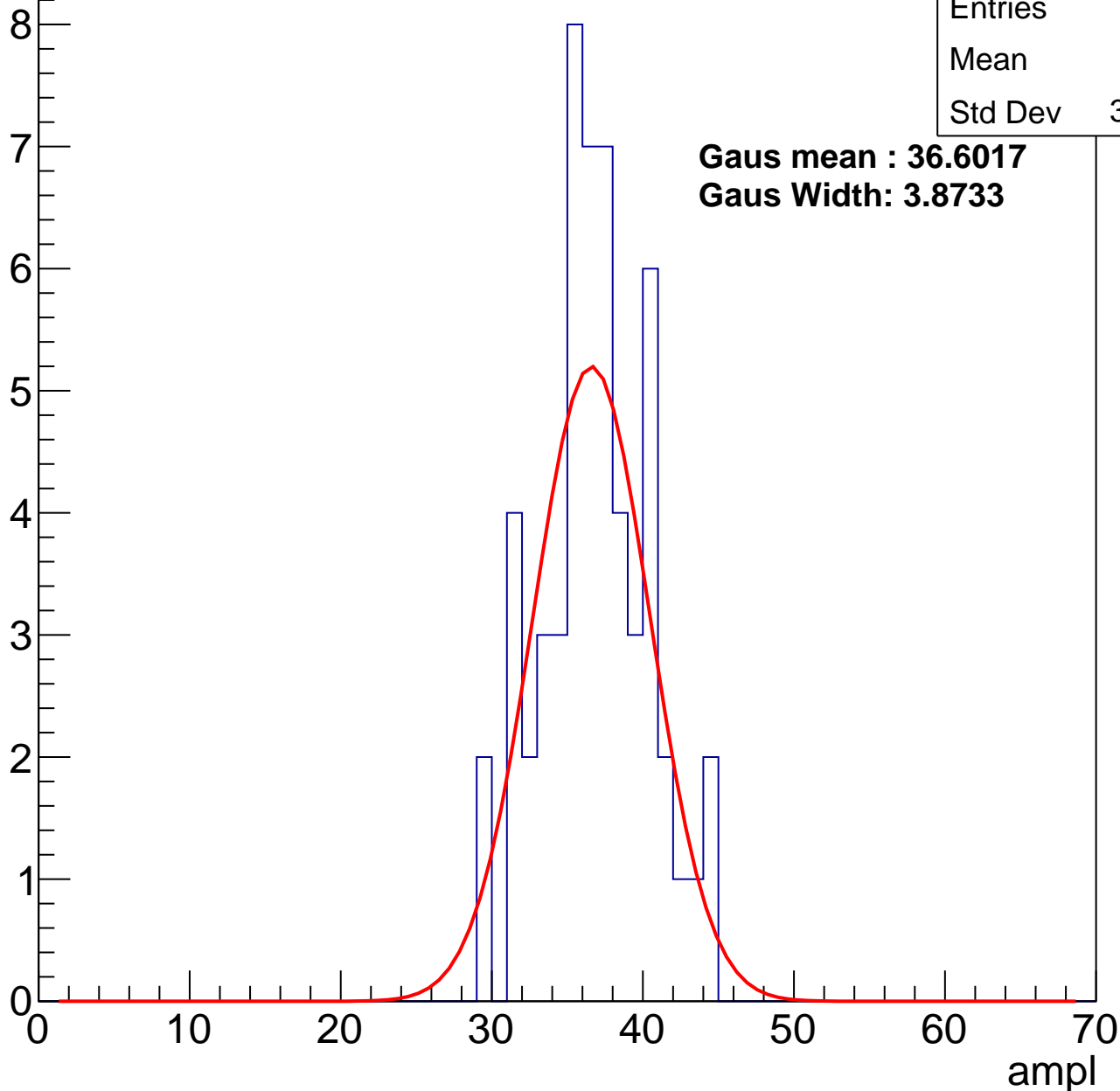
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	36.4
Std Dev	3.509

**Gaus mean : 36.6017**

**Gaus Width: 3.8733**



# B1L102S, U5-ch75, adc2

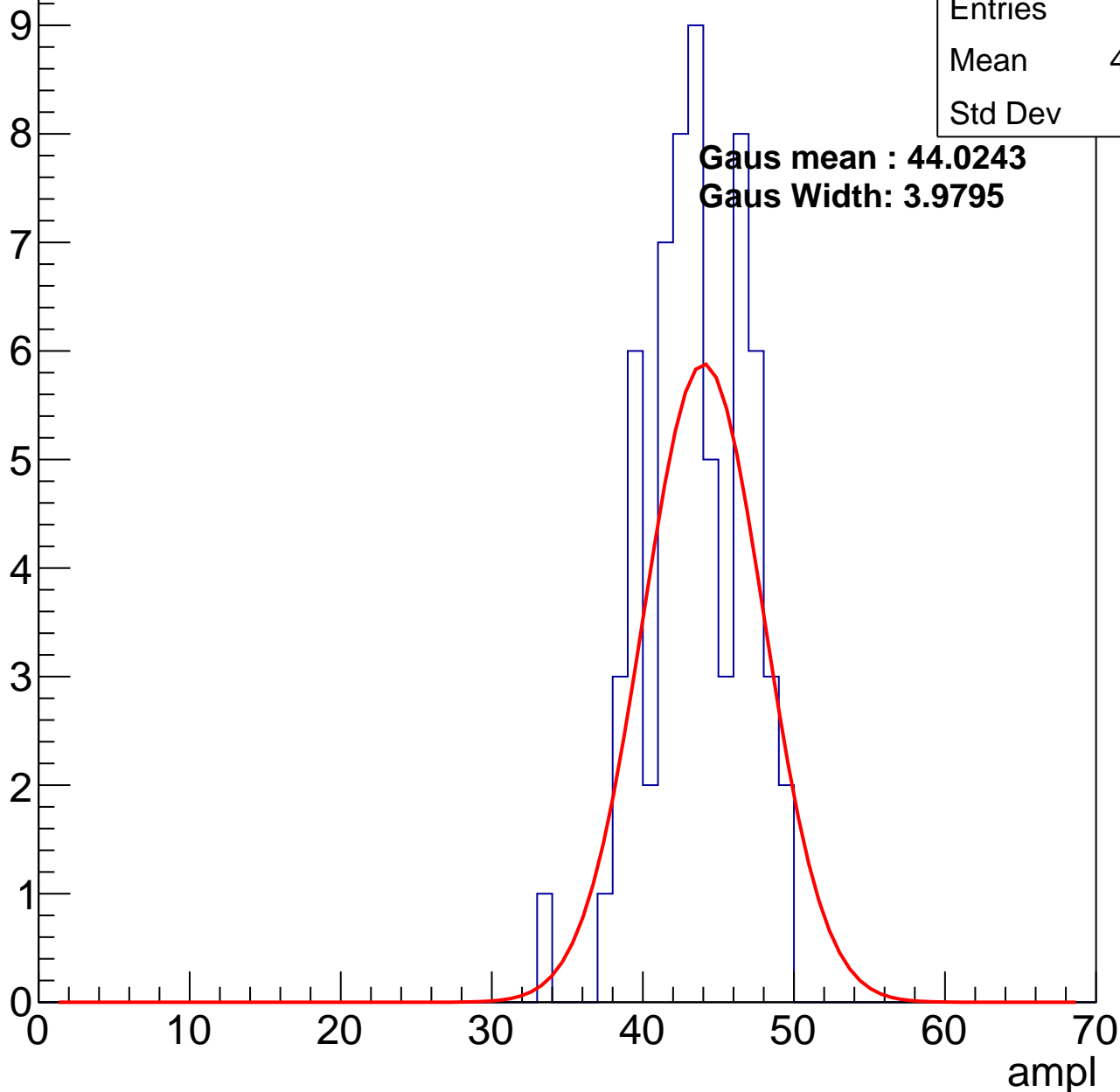
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	43.05
Std Dev	3.29

**Gaus mean : 44.0243**

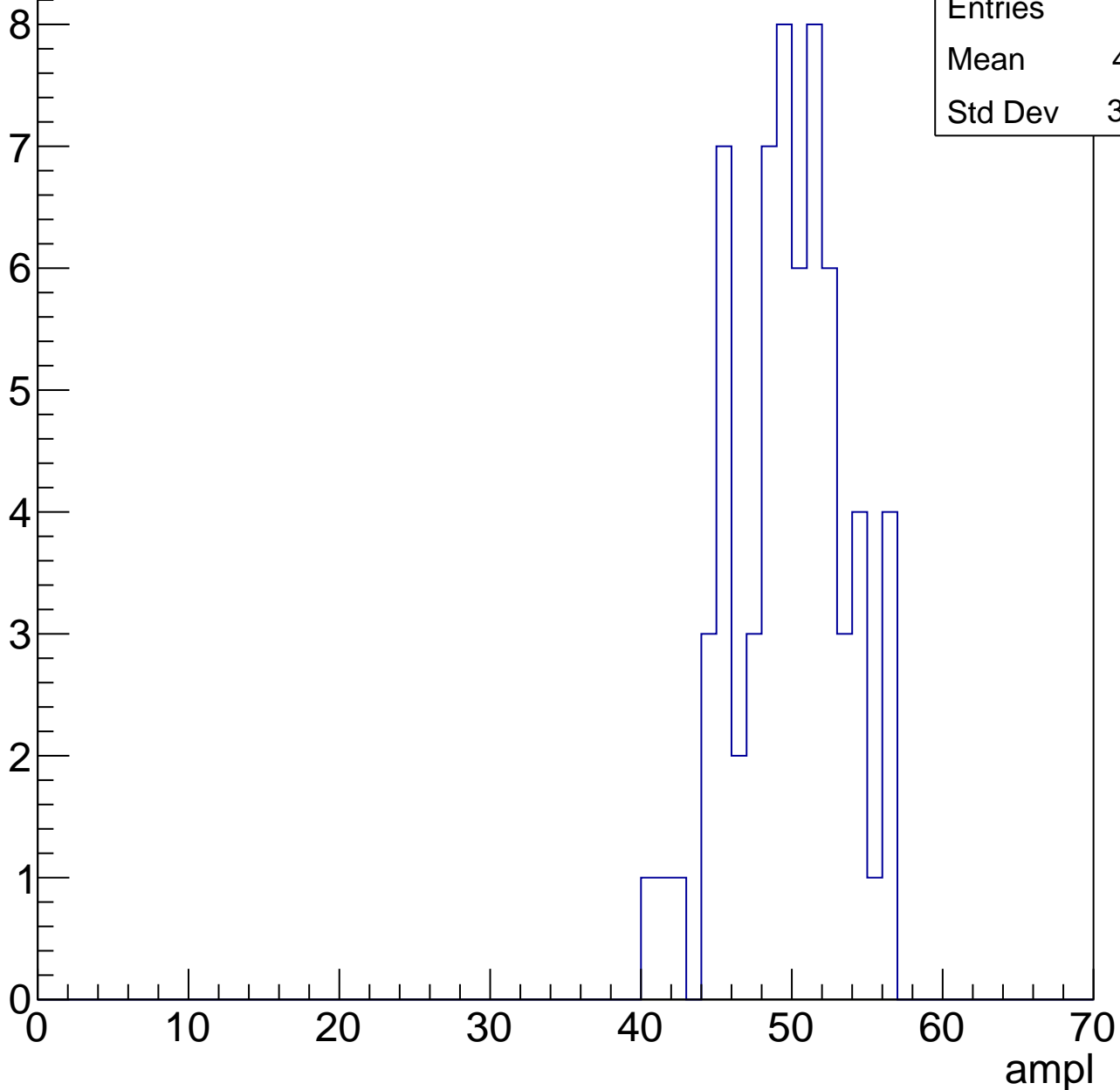
**Gaus Width: 3.9795**



# B1L102S, U5-ch75, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



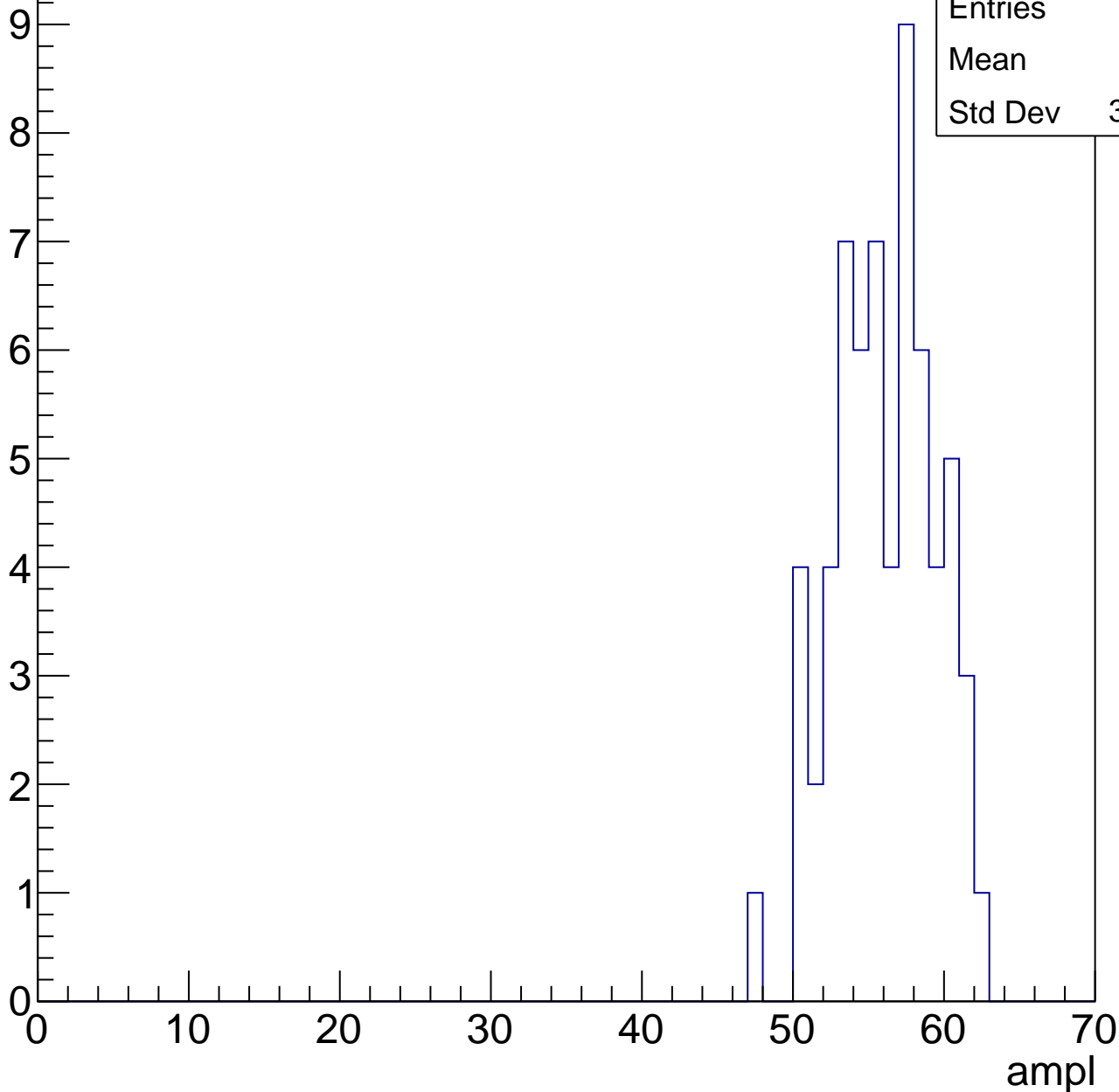
Entries	65
Mean	49.31
Std Dev	3.687

# B1L102S, U5-ch75, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	55.6
Std Dev	3.293

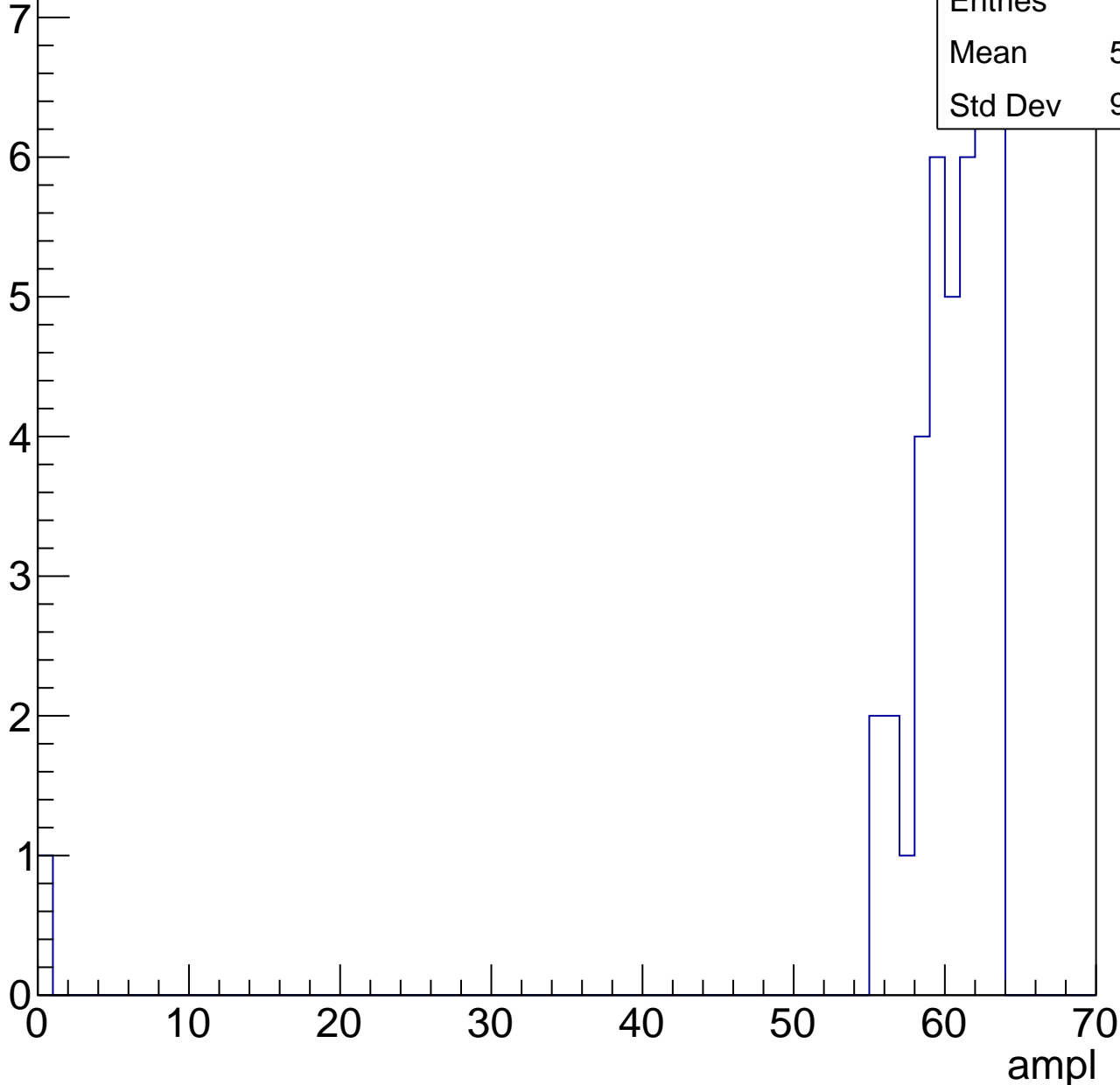


# B1L102S, U5-ch75, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

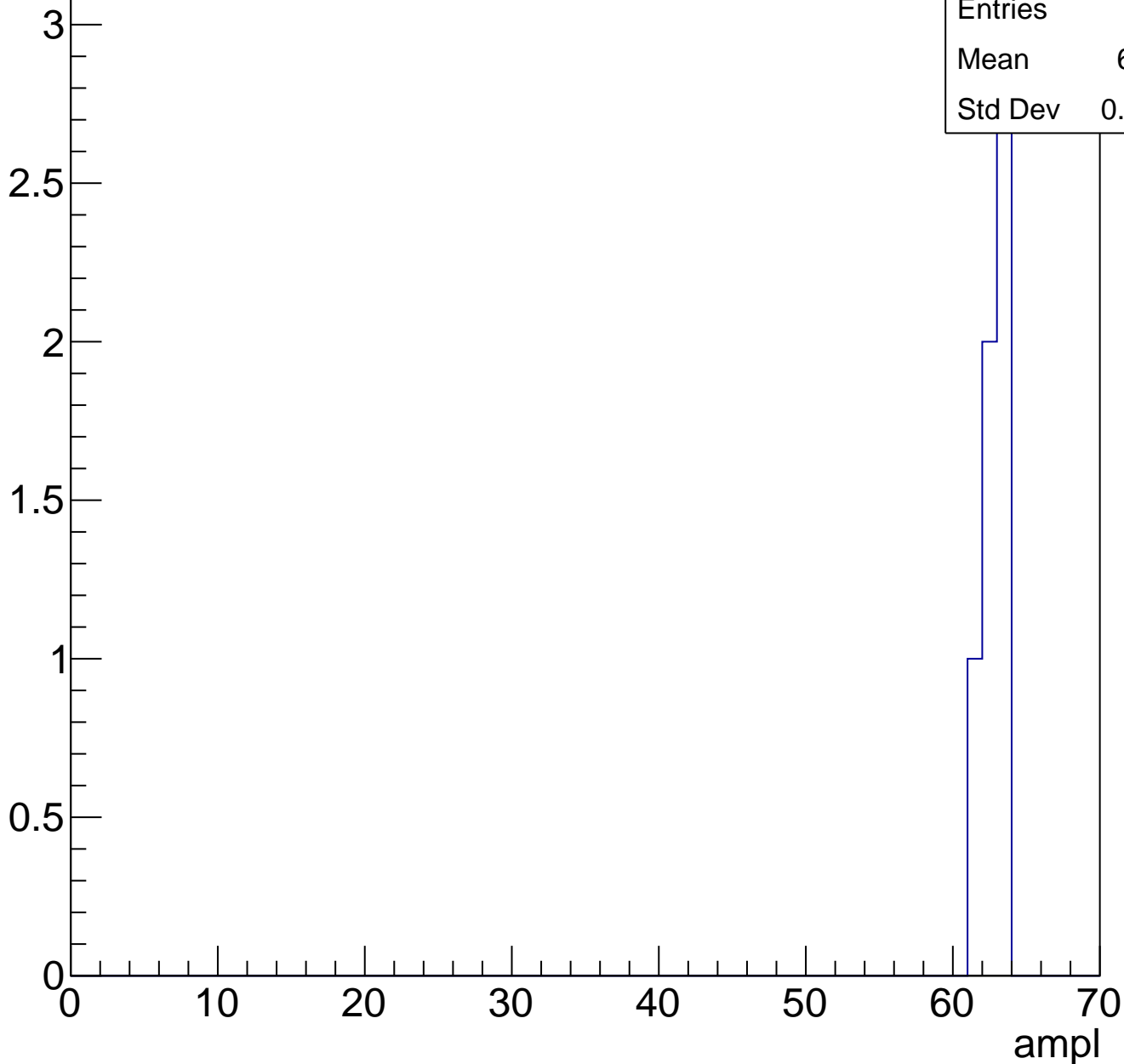
Entries	41
Mean	58.68
Std Dev	9.549



# B1L102S, U5-ch75, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U5-ch75, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U5-ch76, adc0

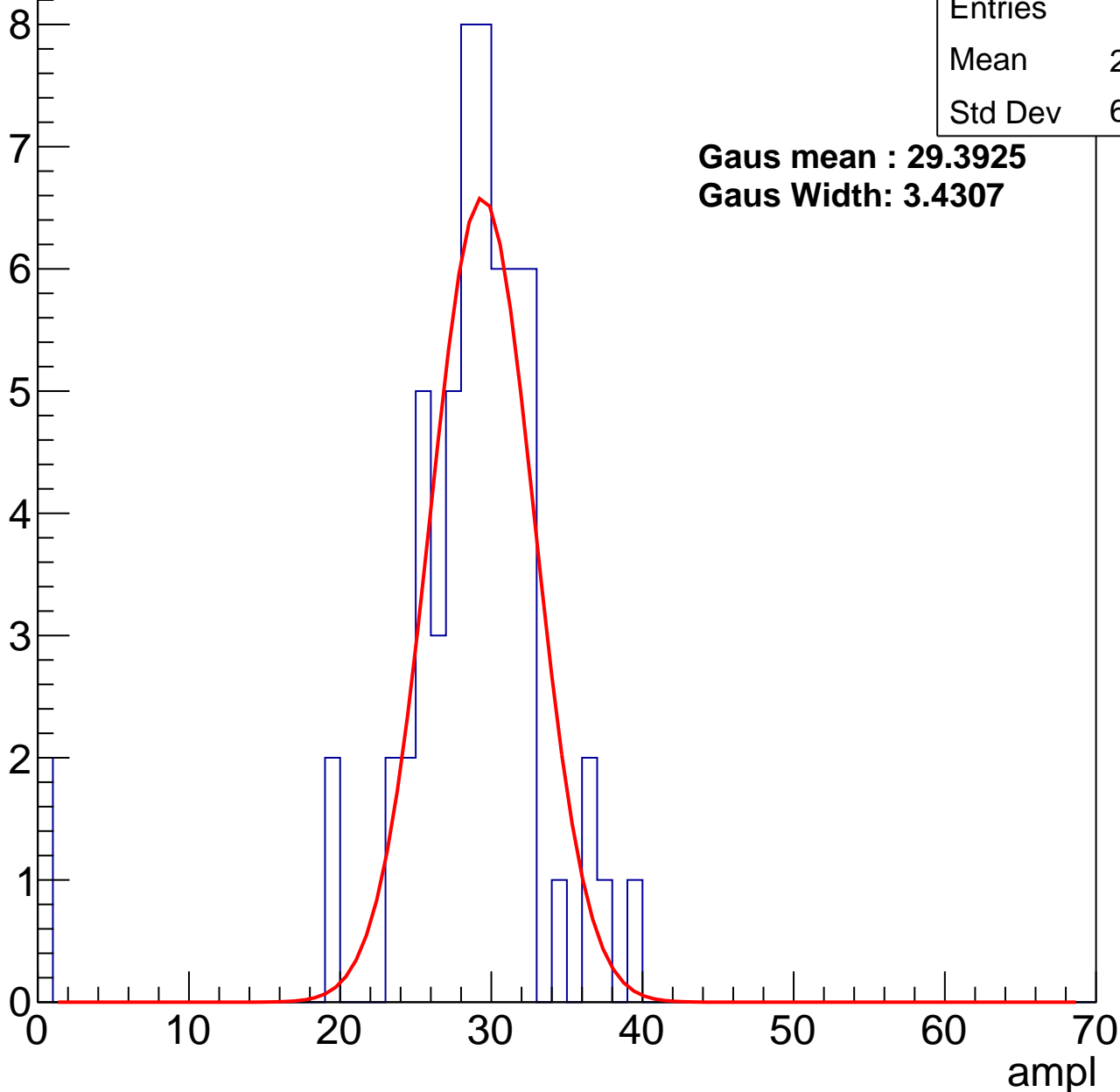
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	27.77
Std Dev	6.349

**Gaus mean : 29.3925**

**Gaus Width: 3.4307**



# B1L102S, U5-ch76, adc1

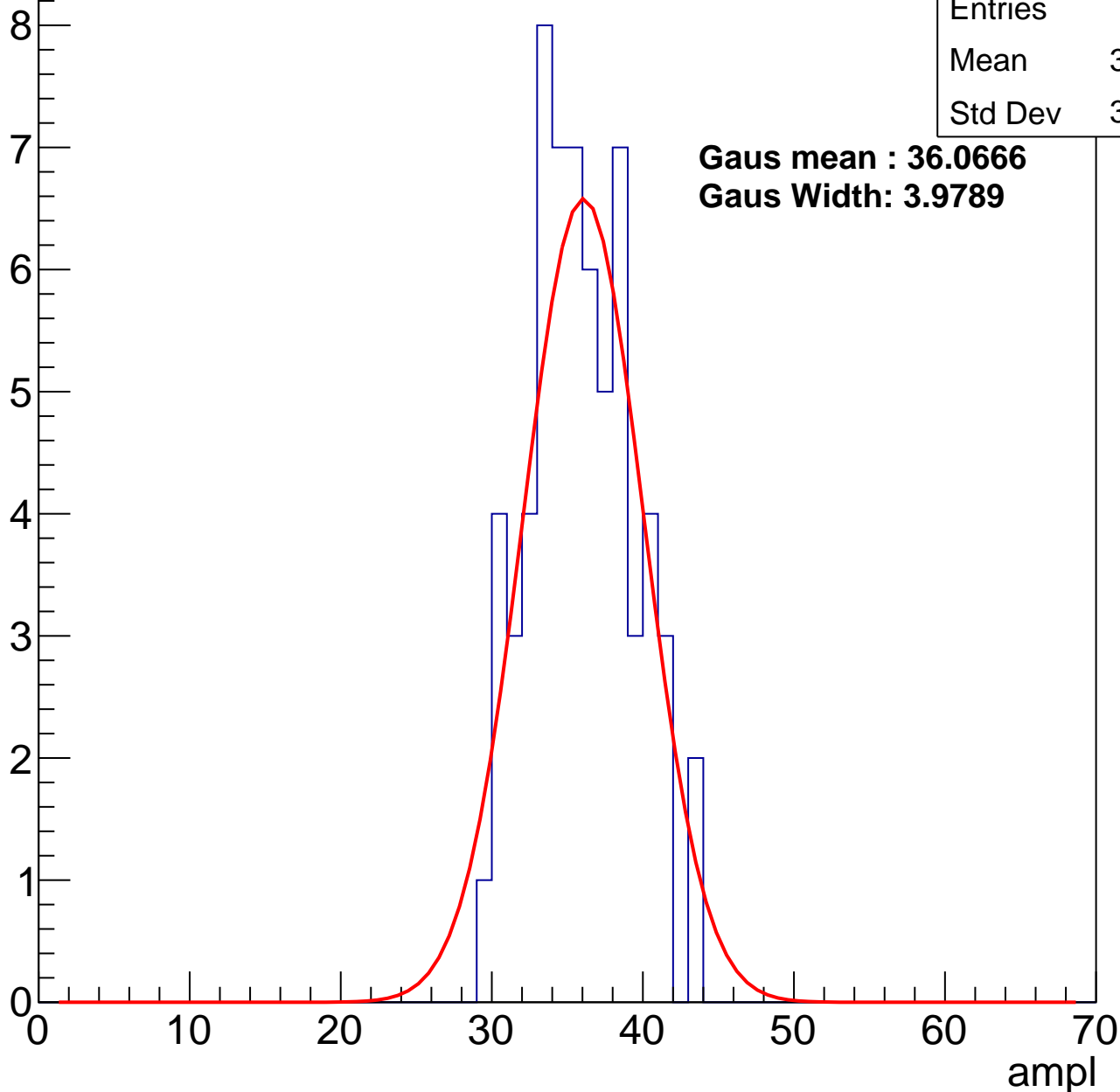
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	35.47
Std Dev	3.349

**Gaus mean : 36.0666**

**Gaus Width: 3.9789**



# B1L102S, U5-ch76, adc2

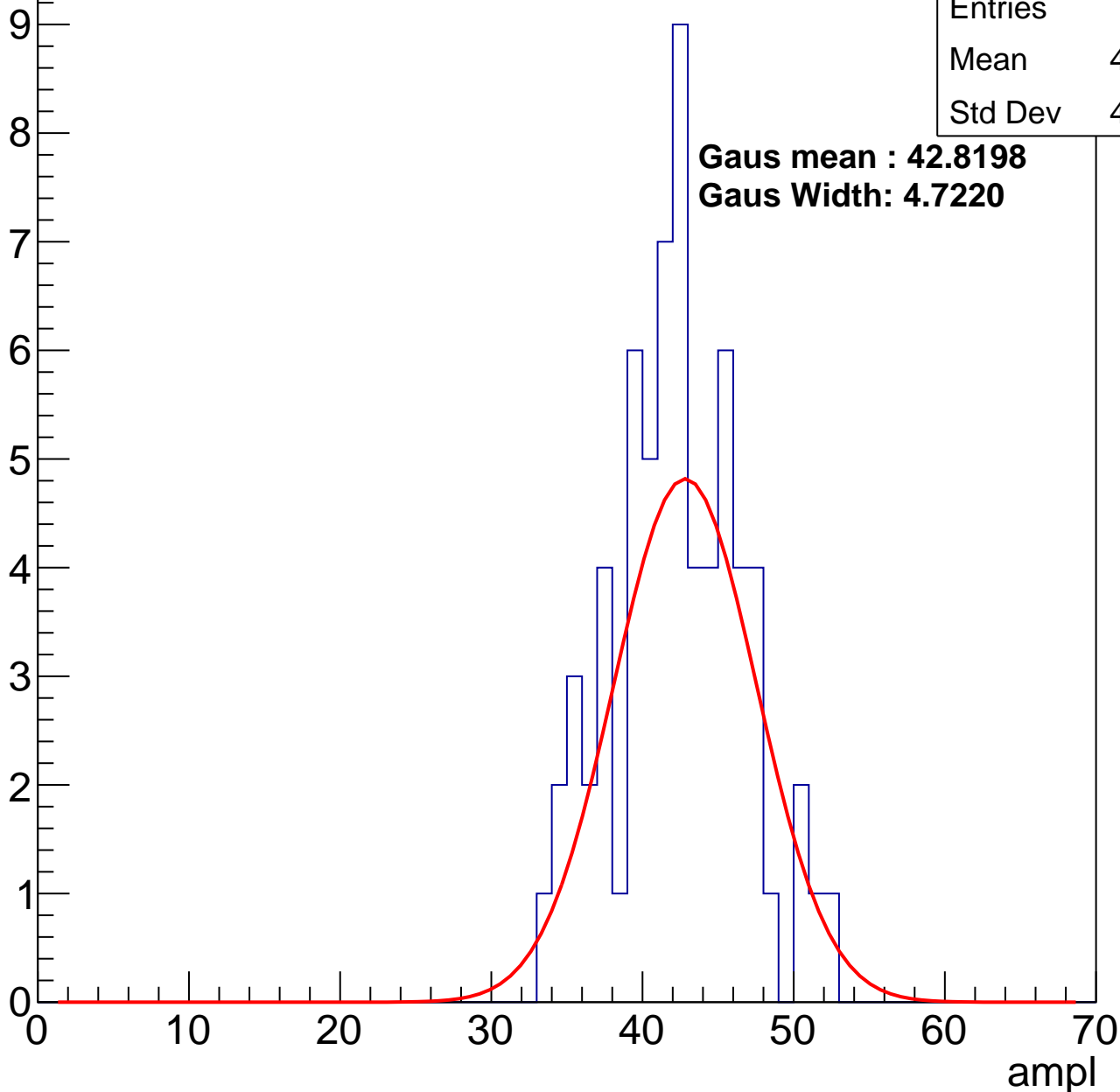
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	41.85
Std Dev	4.244

**Gaus mean : 42.8198**

**Gaus Width: 4.7220**

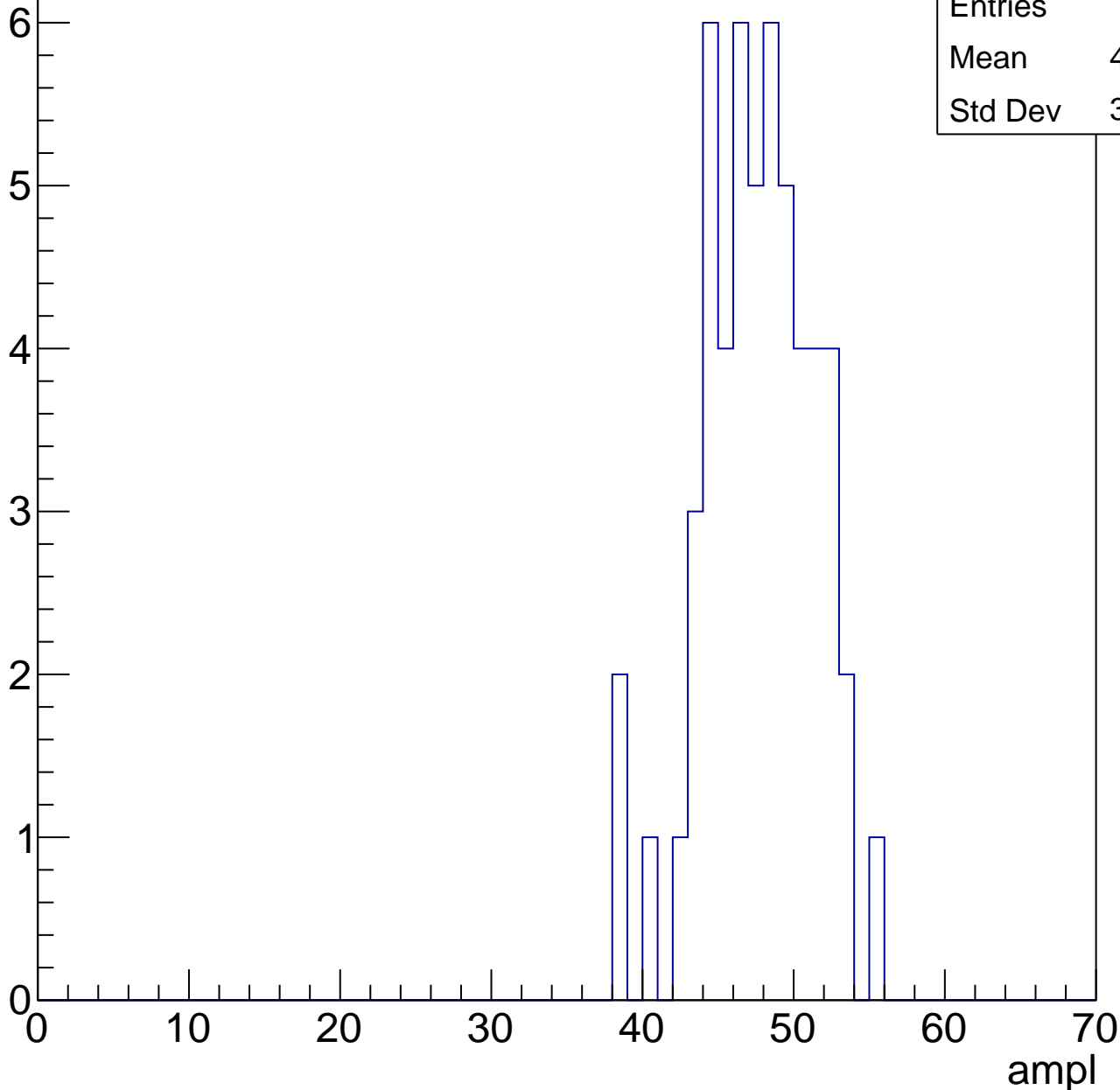


# B1L102S, U5-ch76, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	47.19
Std Dev	3.652

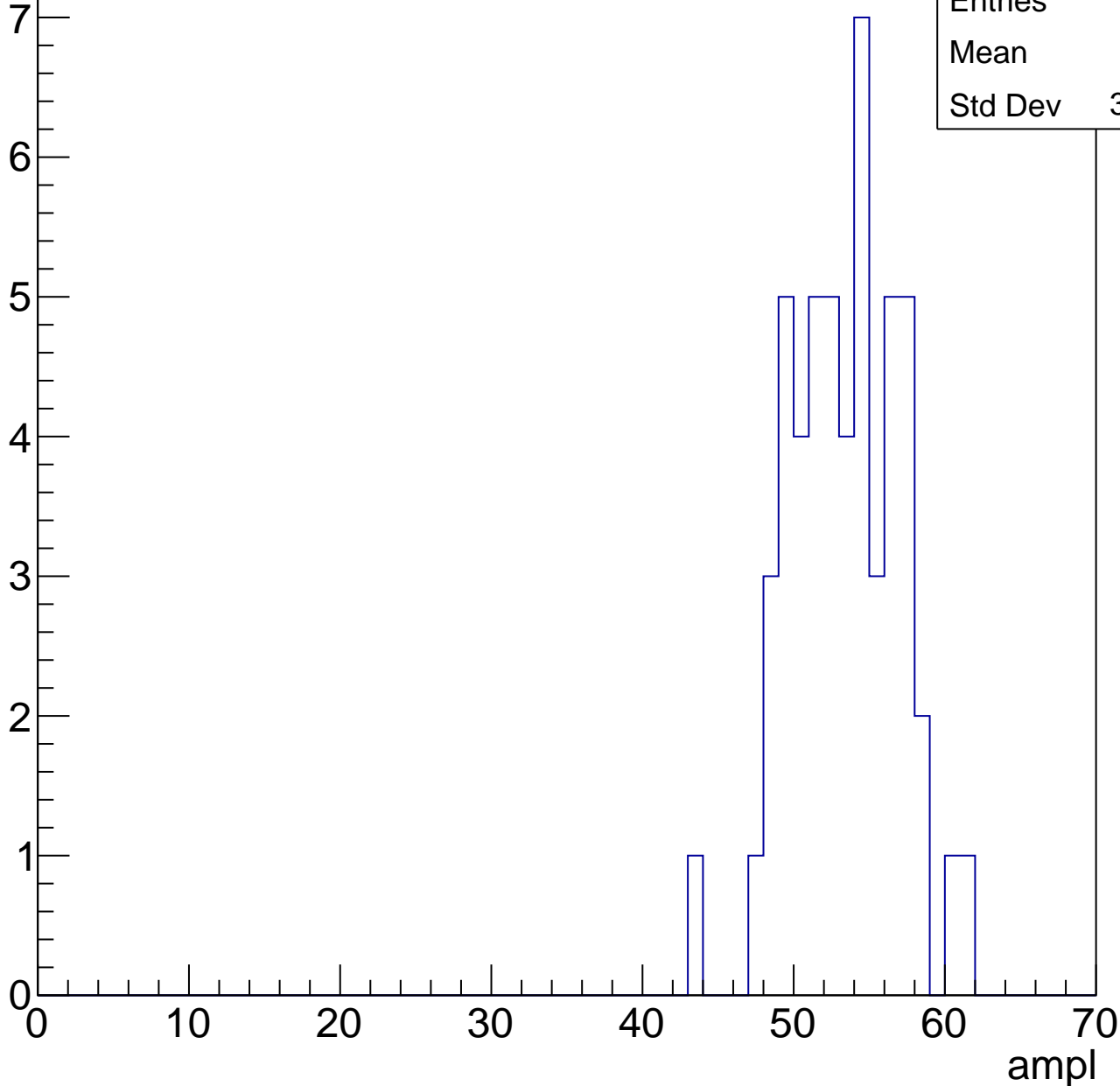


# B1L102S, U5-ch76, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	52.9
Std Dev	3.559



# B1L102S, U5-ch76, adc5

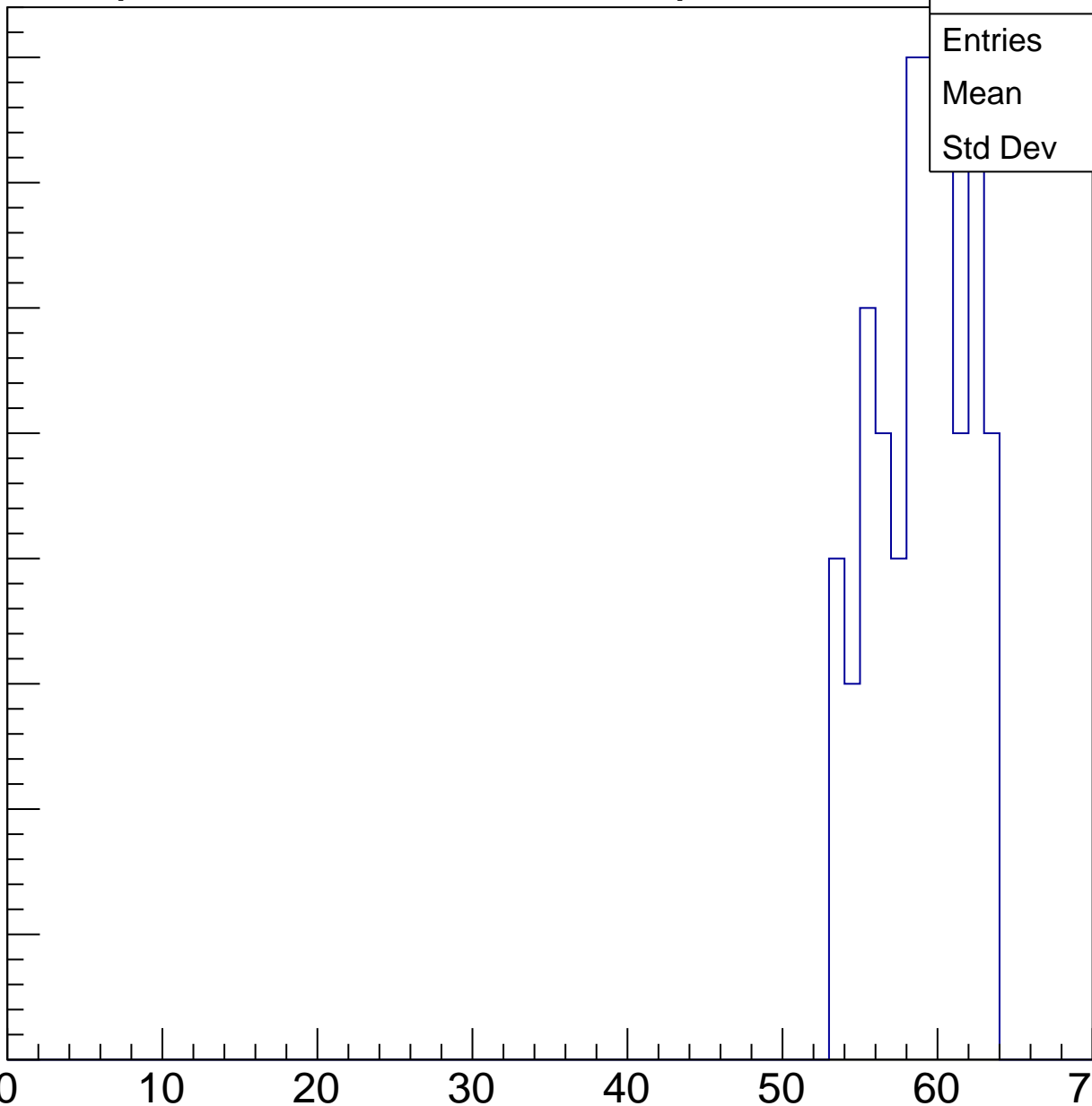
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	64
Mean	58.5
Std Dev	2.926

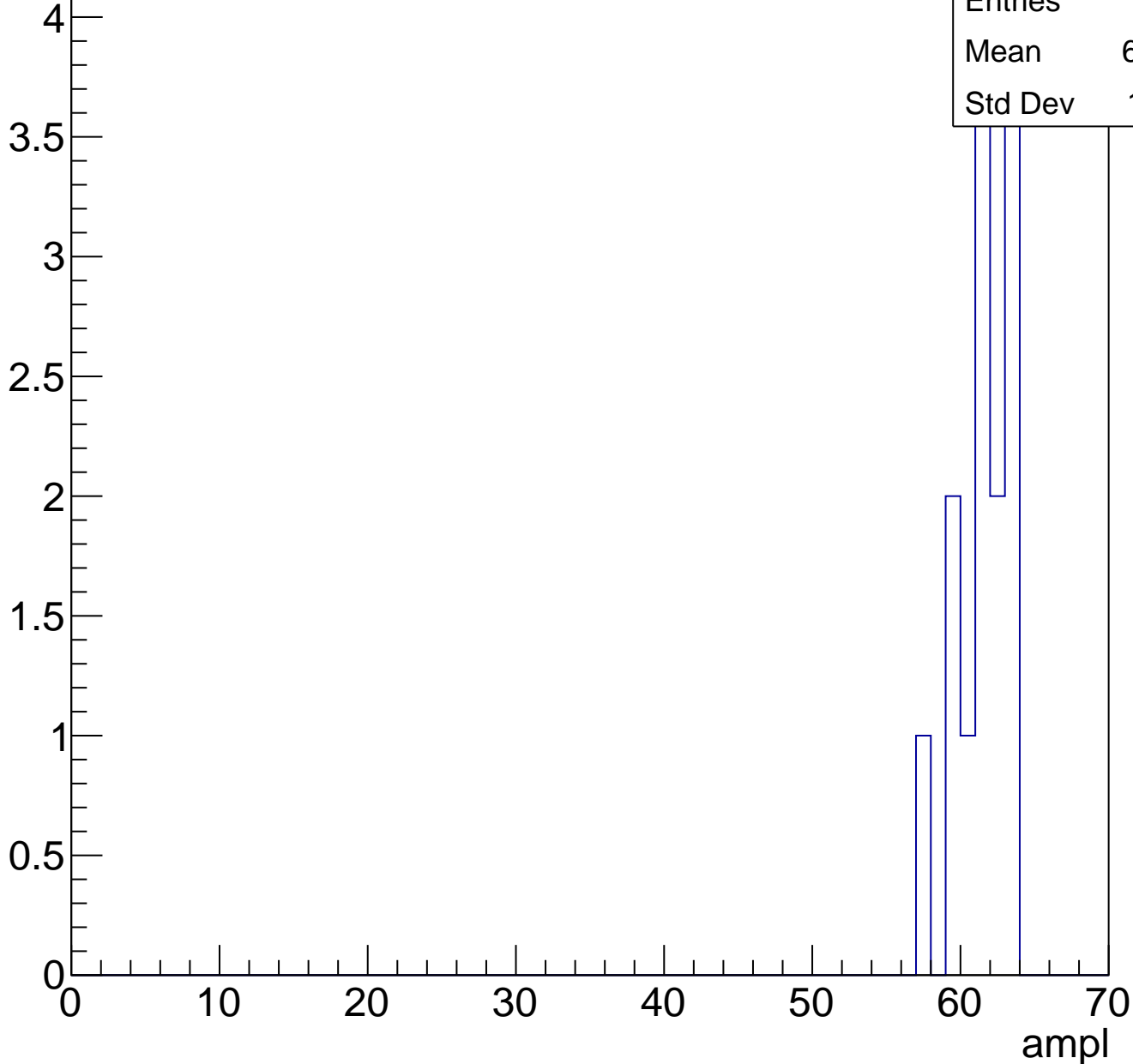
ampl



# B1L102S, U5-ch76, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

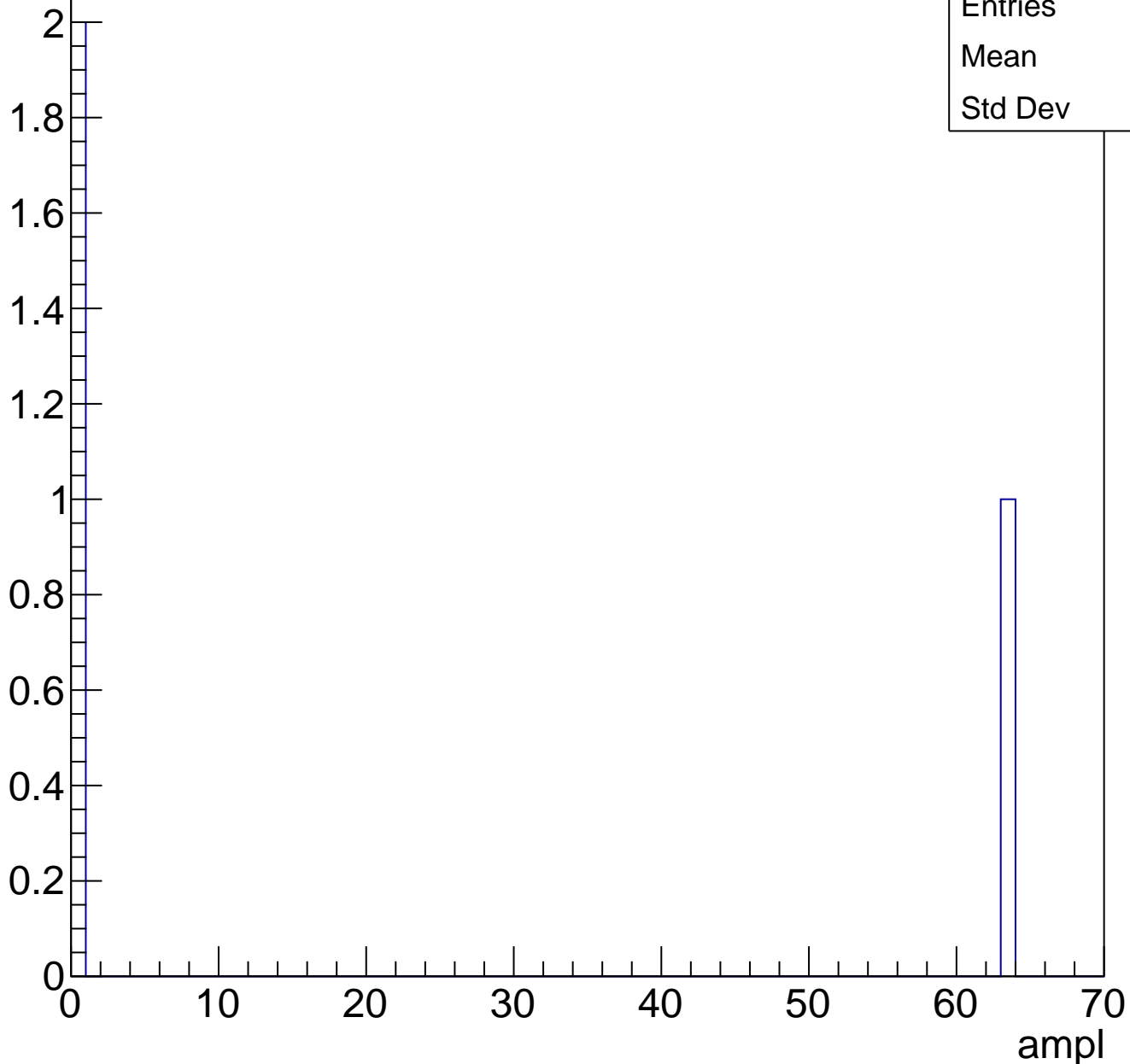




# B1L102S, U5-ch76, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	3
Mean	21
Std Dev	29.7

# B1L102S, U5-ch77, adc0

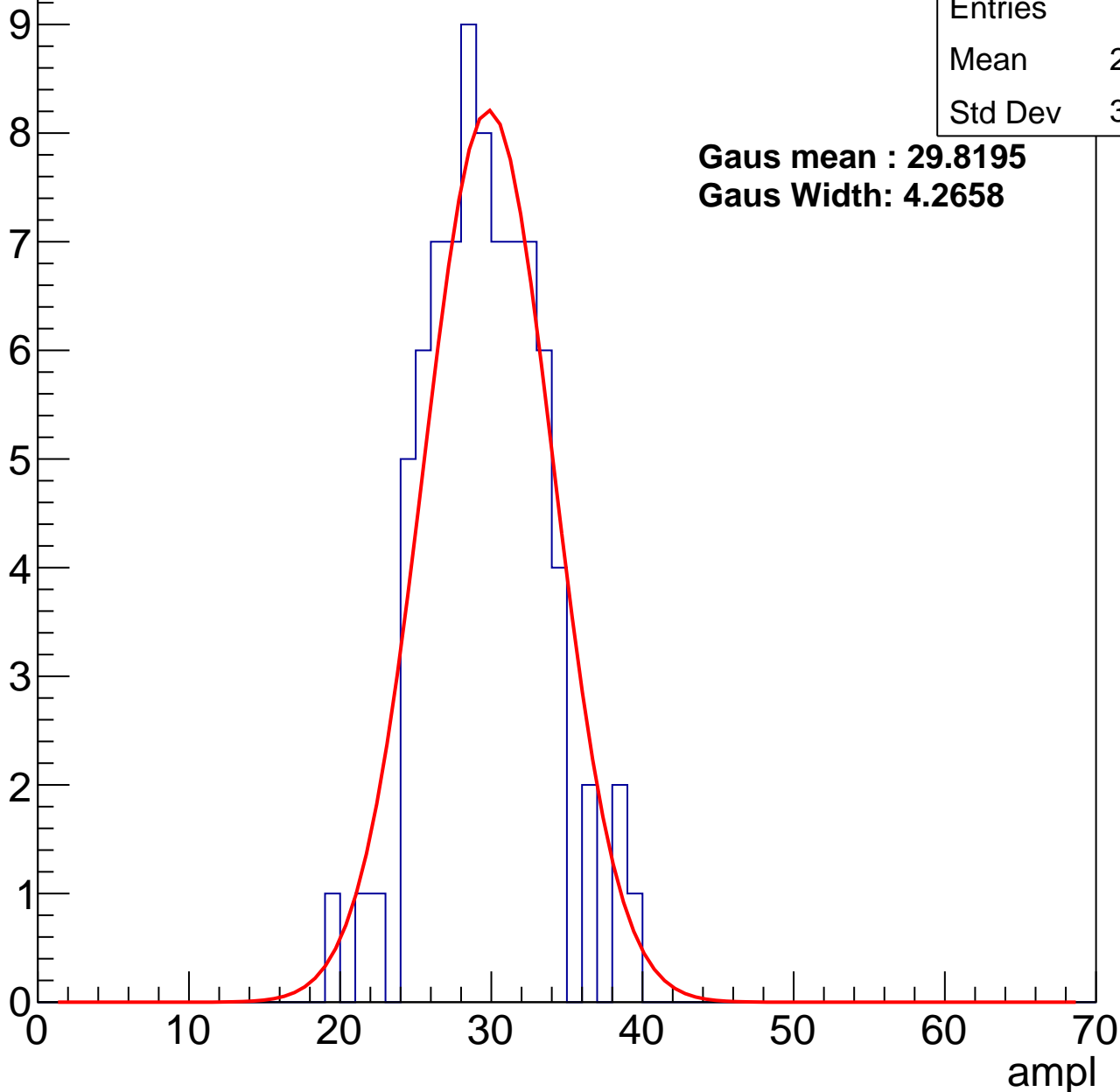
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	81
Mean	29.12
Std Dev	3.828

**Gaus mean : 29.8195**

**Gaus Width: 4.2658**



# B1L102S, U5-ch77, adc1

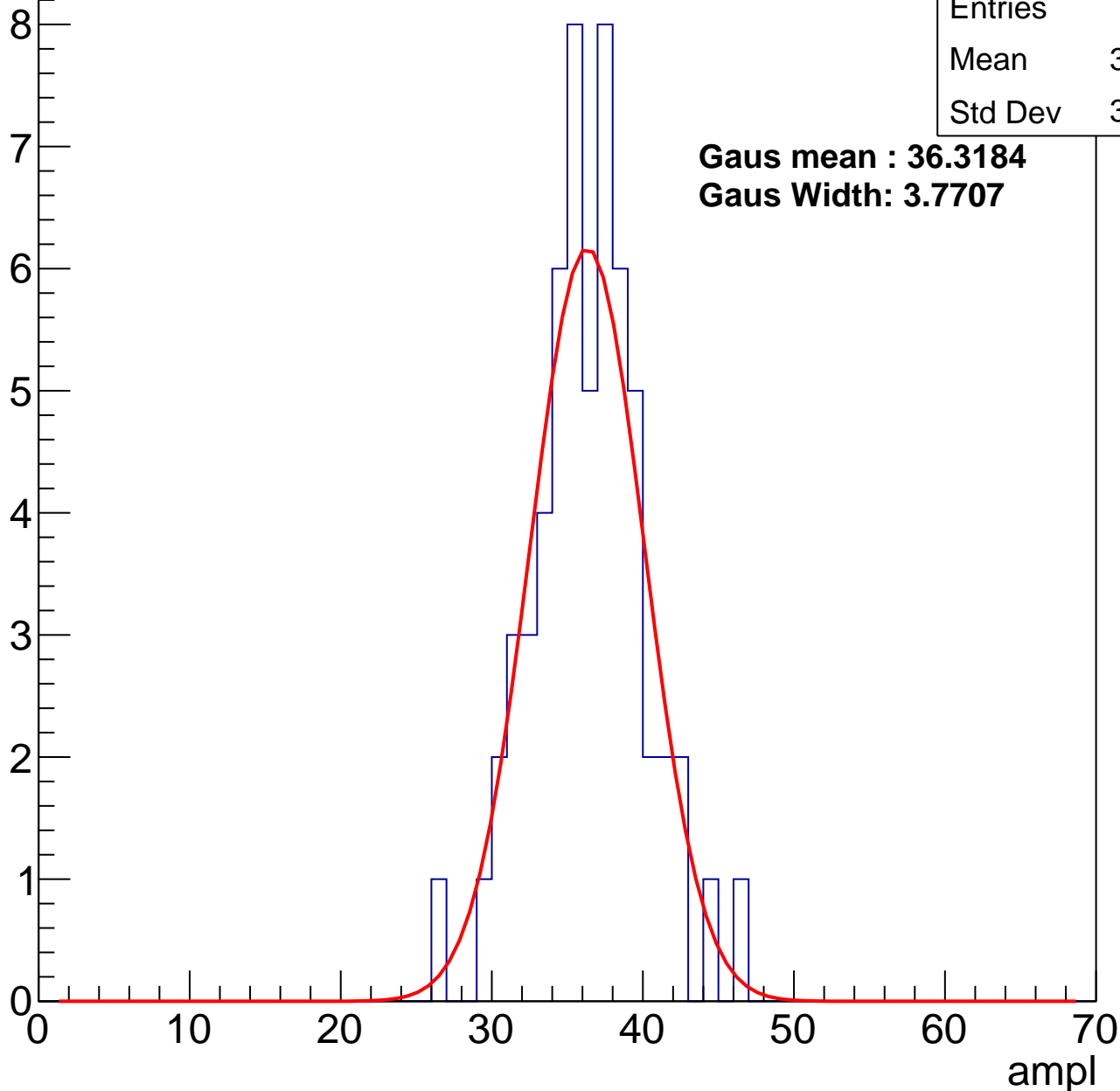
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	35.92
Std Dev	3.666

**Gaus mean : 36.3184**

**Gaus Width: 3.7707**



# B1L102S, U5-ch77, adc2

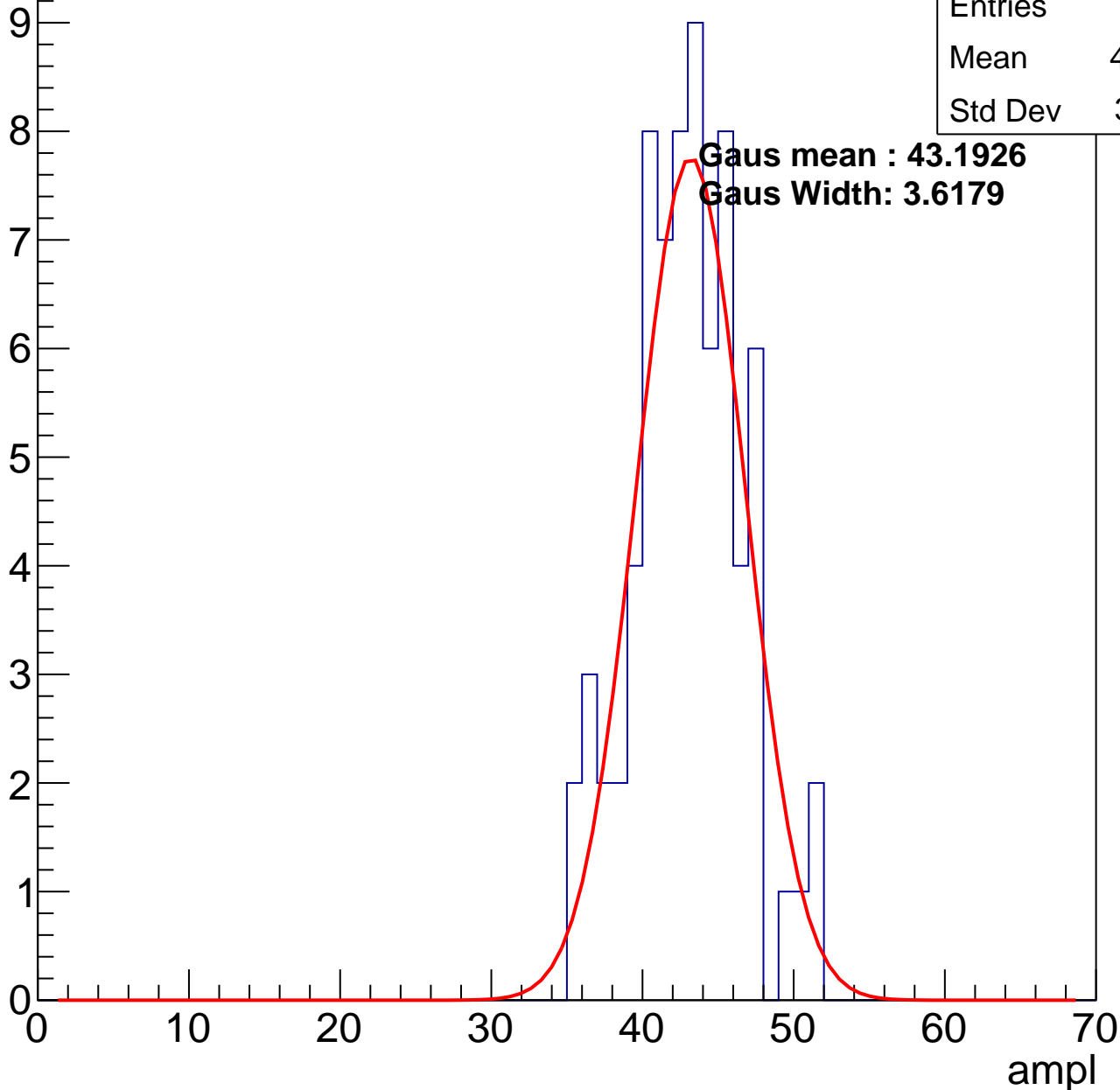
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	42.53
Std Dev	3.581

**Gaus mean : 43.1926**

**Gaus Width: 3.6179**

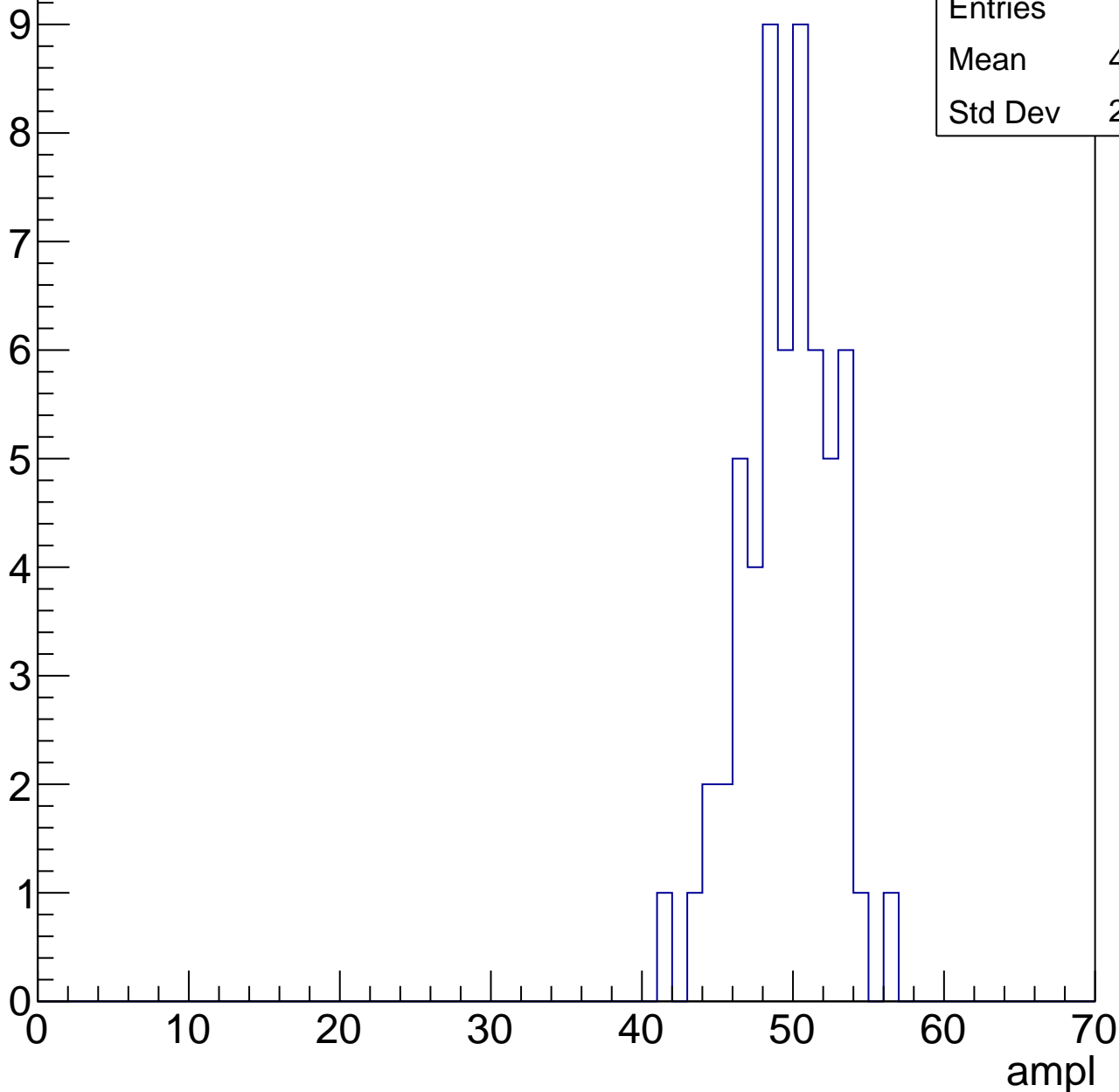


# B1L102S, U5-ch77, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

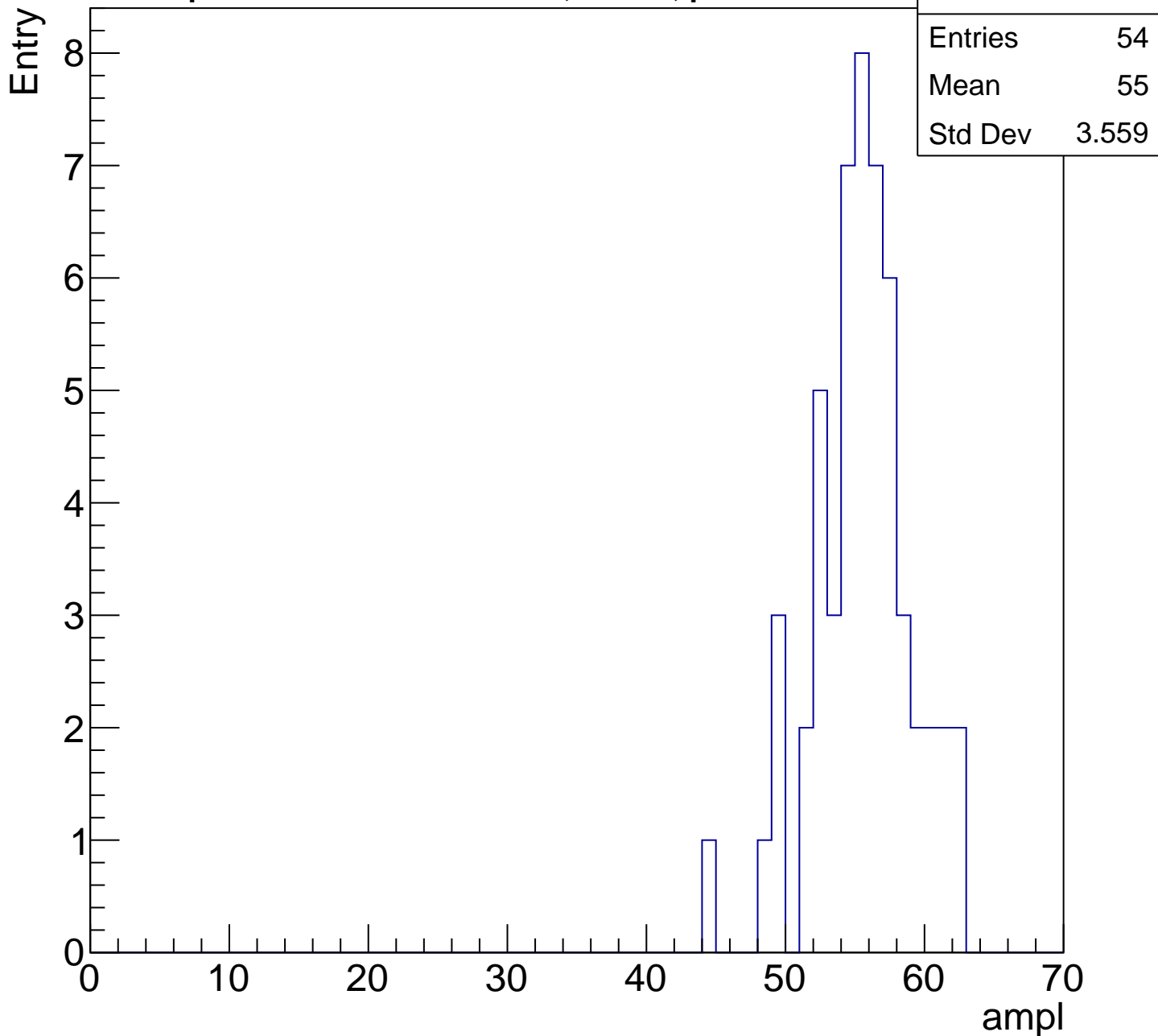
Entry

Entries	58
Mean	49.14
Std Dev	2.933



# B1L102S, U5-ch77, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2



# B1L102S, U5-ch77, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

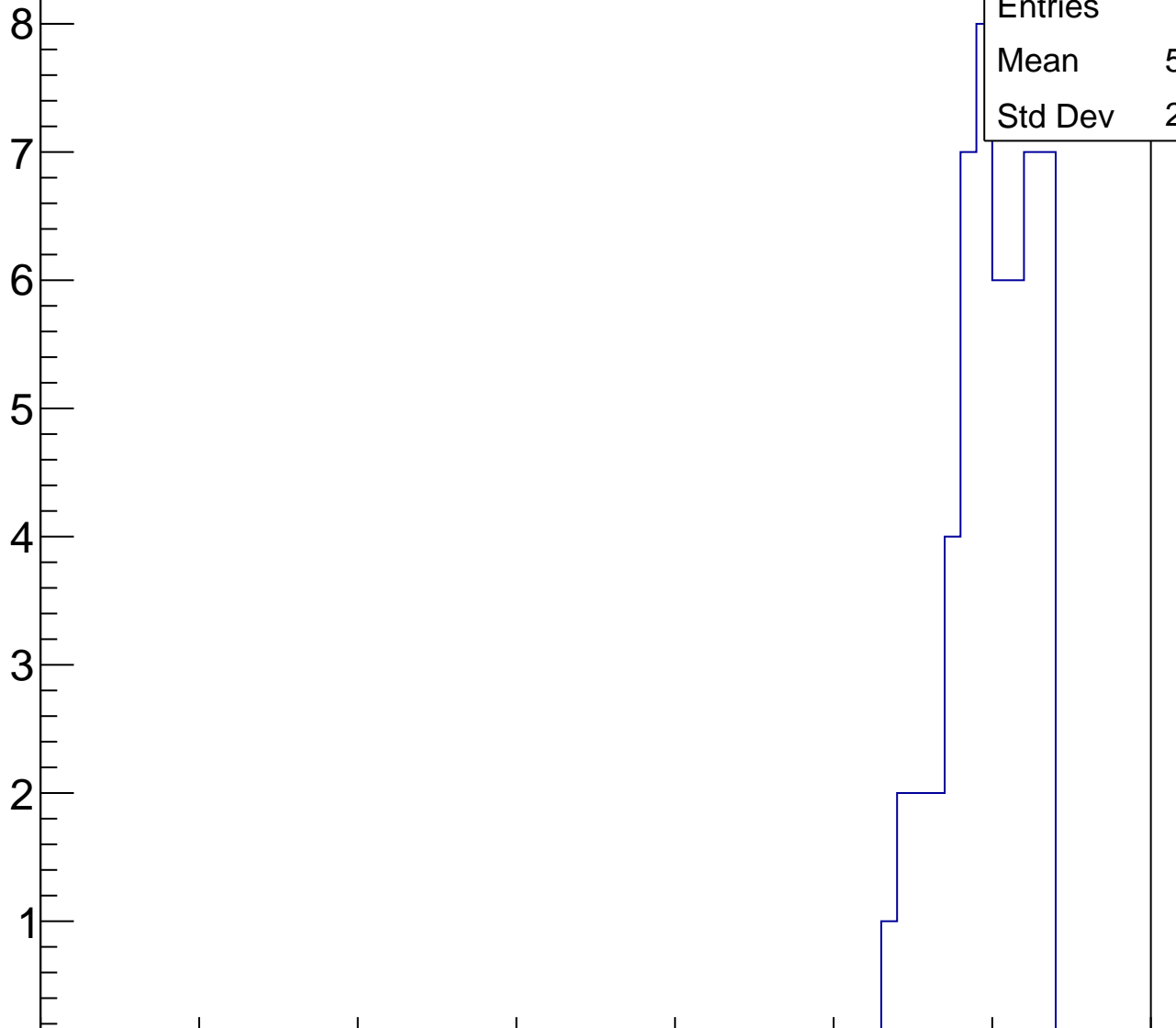
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	52
Mean	59.42
Std Dev	2.612

ampl

0 10 20 30 40 50 60 70



# B1L102S, U5-ch77, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

3

2.5

2

1.5

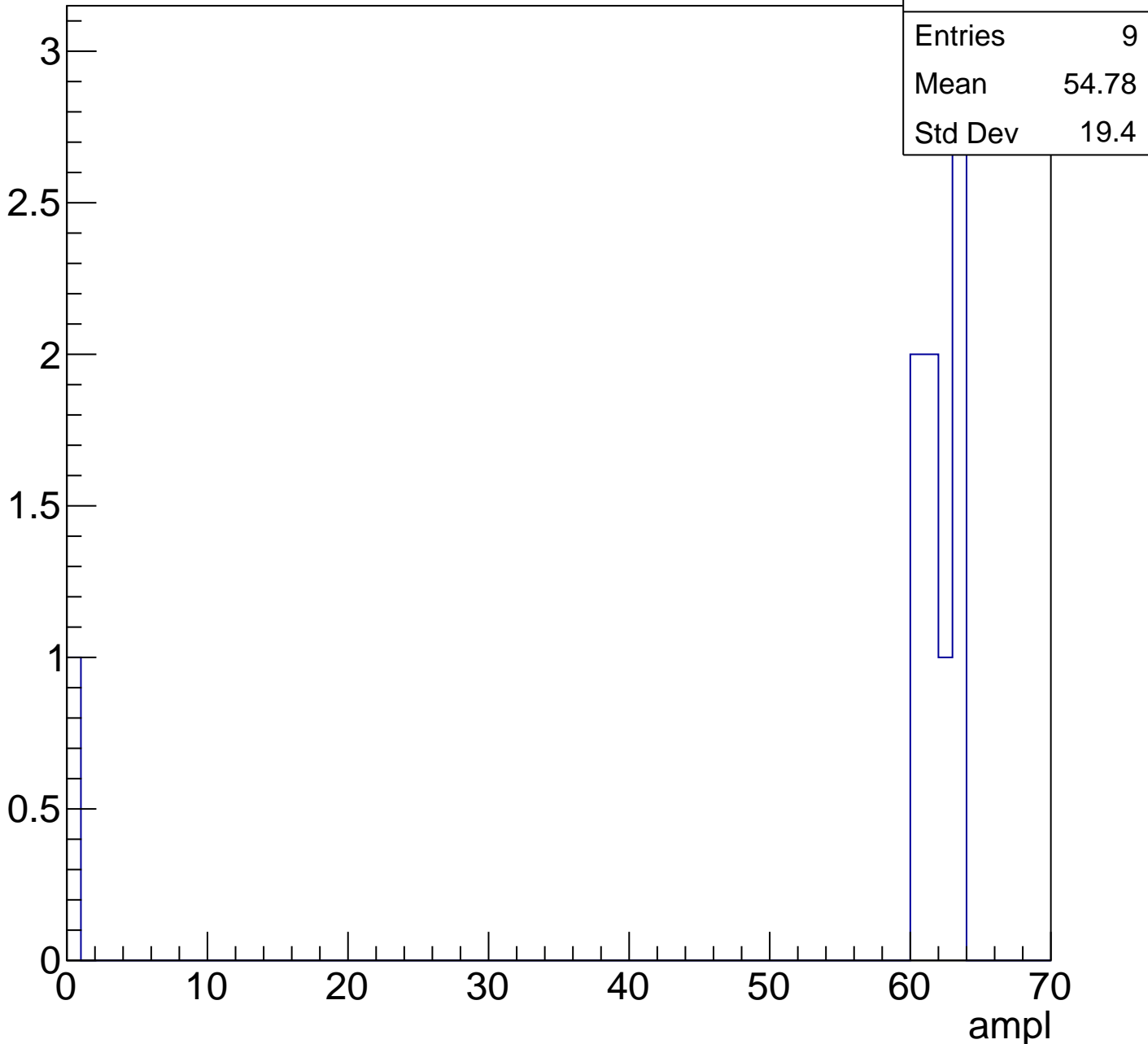
1

0.5

0

ampl

Entries	9
Mean	54.78
Std Dev	19.4





# B1L102S, U5-ch77, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U5-ch78, adc0

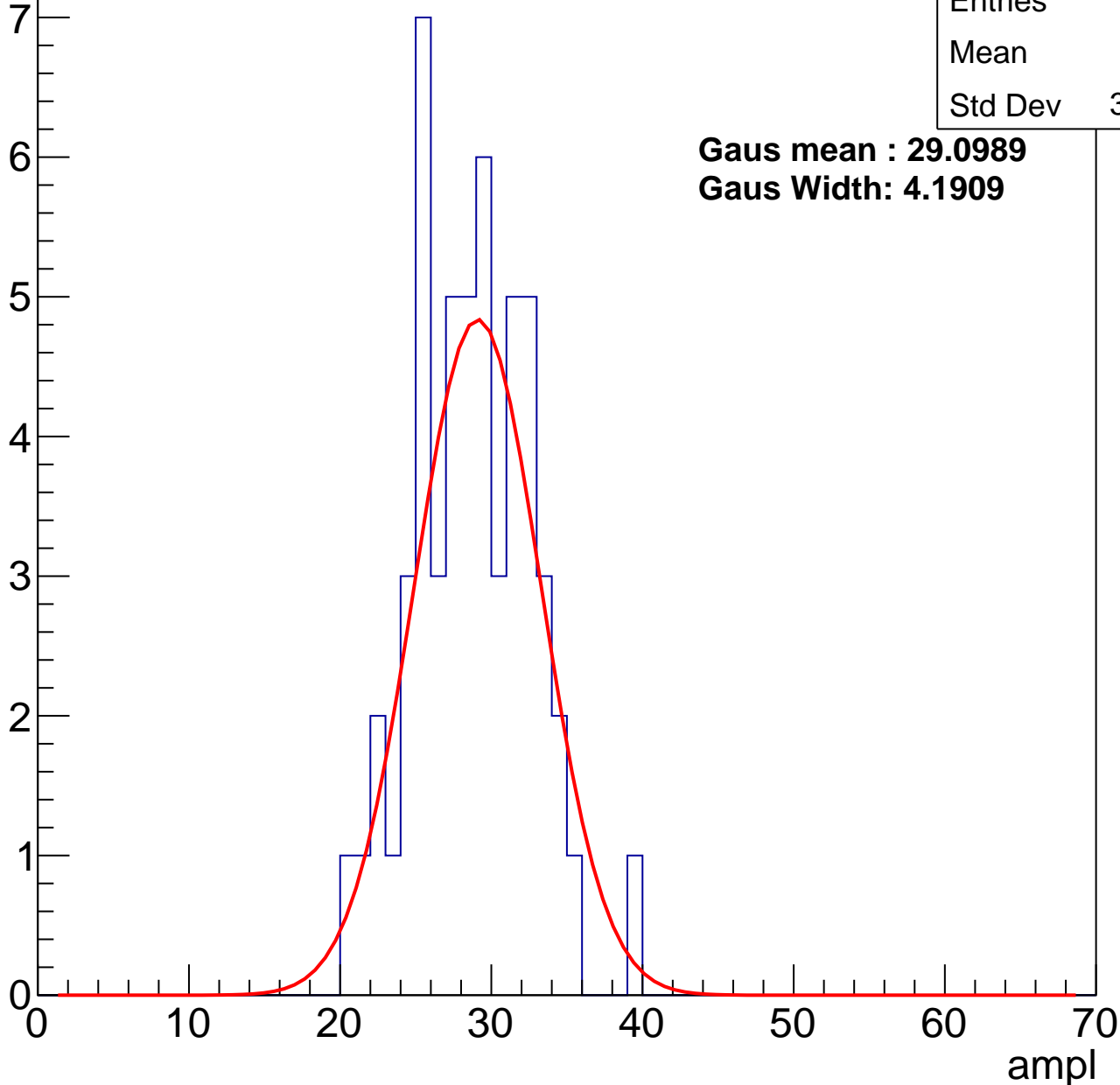
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	28.3
Std Dev	3.833

**Gaus mean : 29.0989**

**Gaus Width: 4.1909**



# B1L102S, U5-ch78, adc1

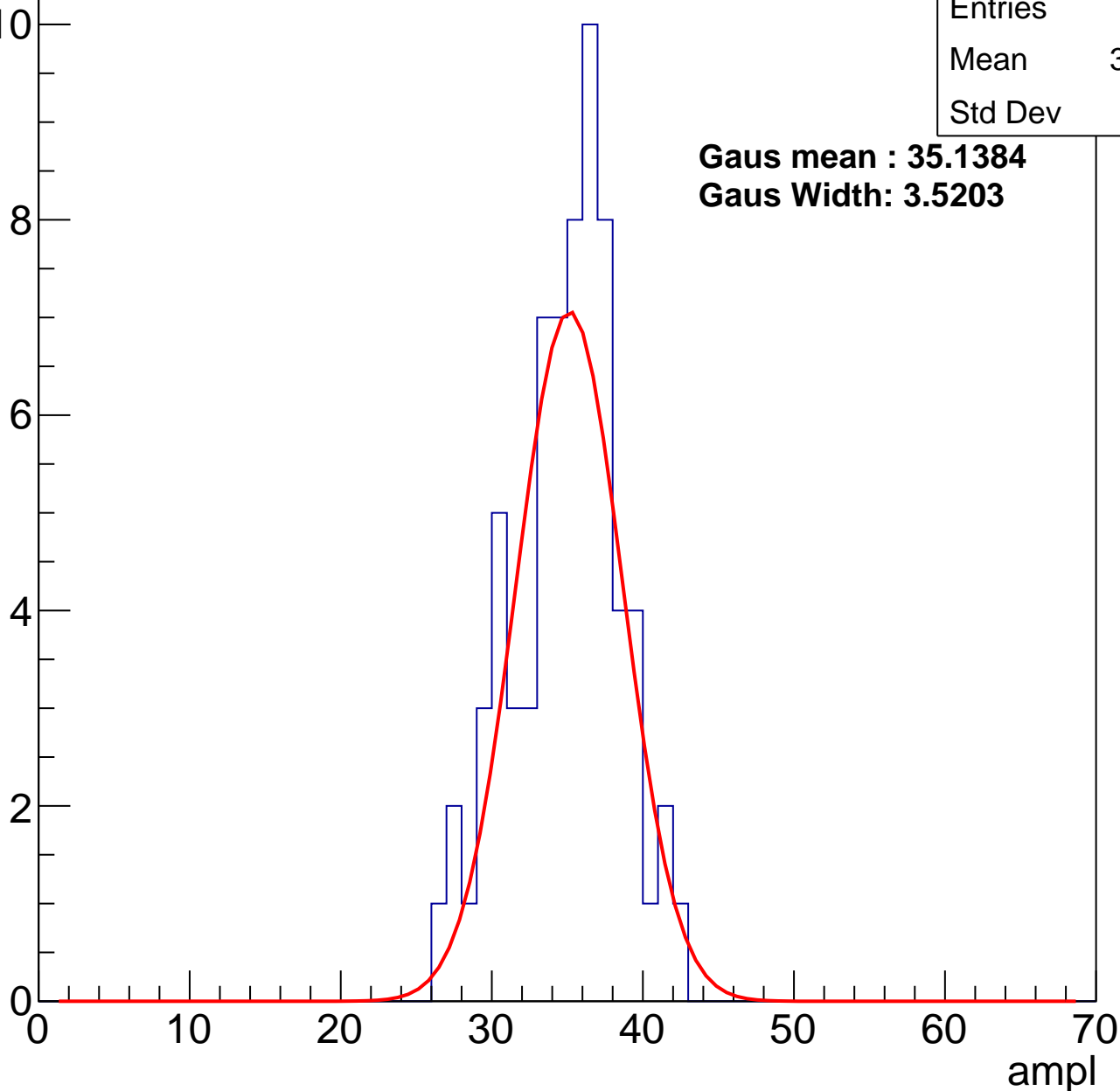
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	34.44
Std Dev	3.52

**Gaus mean : 35.1384**

**Gaus Width: 3.5203**



# B1L102S, U5-ch78, adc2

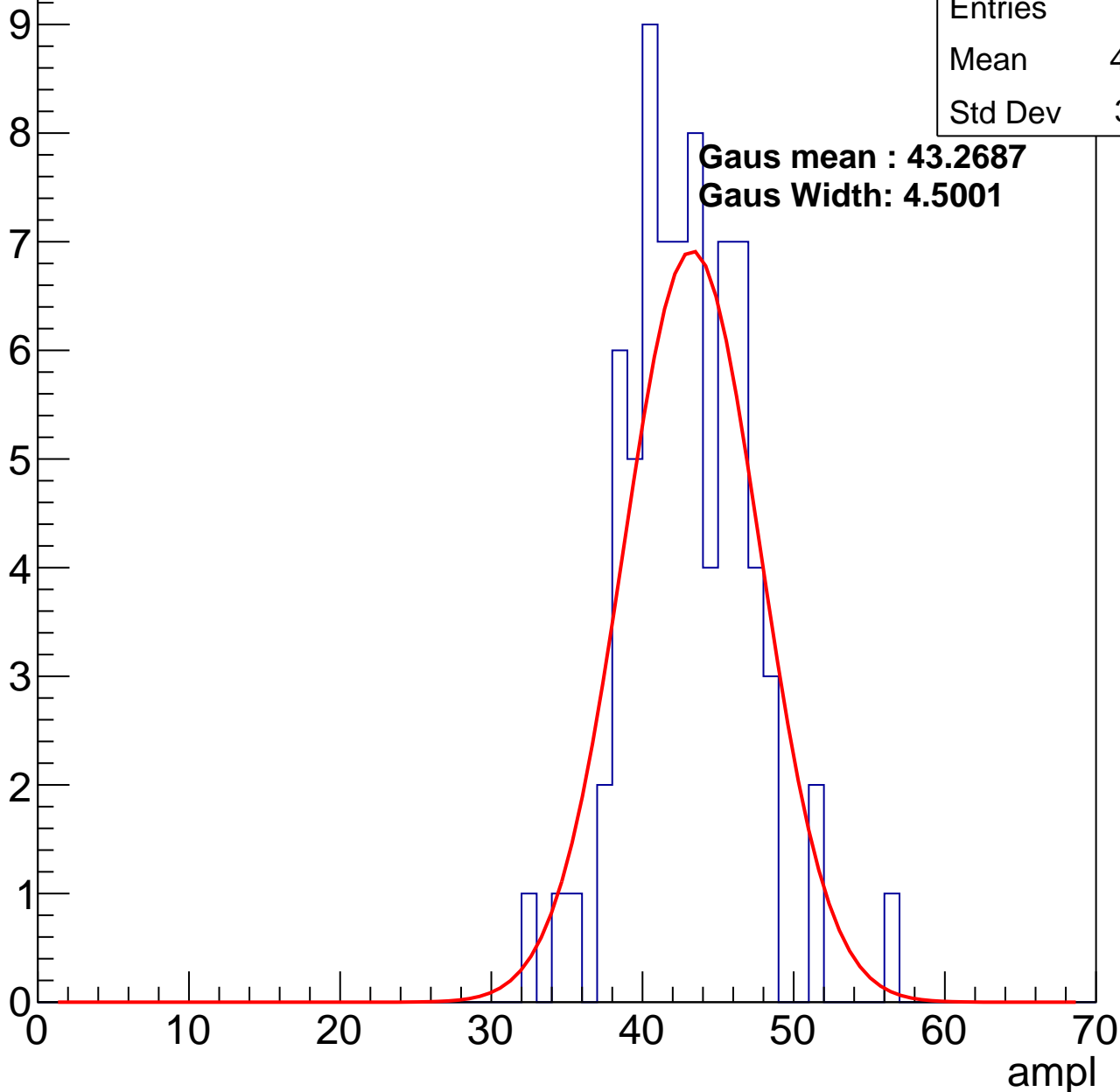
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	42.48
Std Dev	3.991

**Gaus mean : 43.2687**

**Gaus Width: 4.5001**

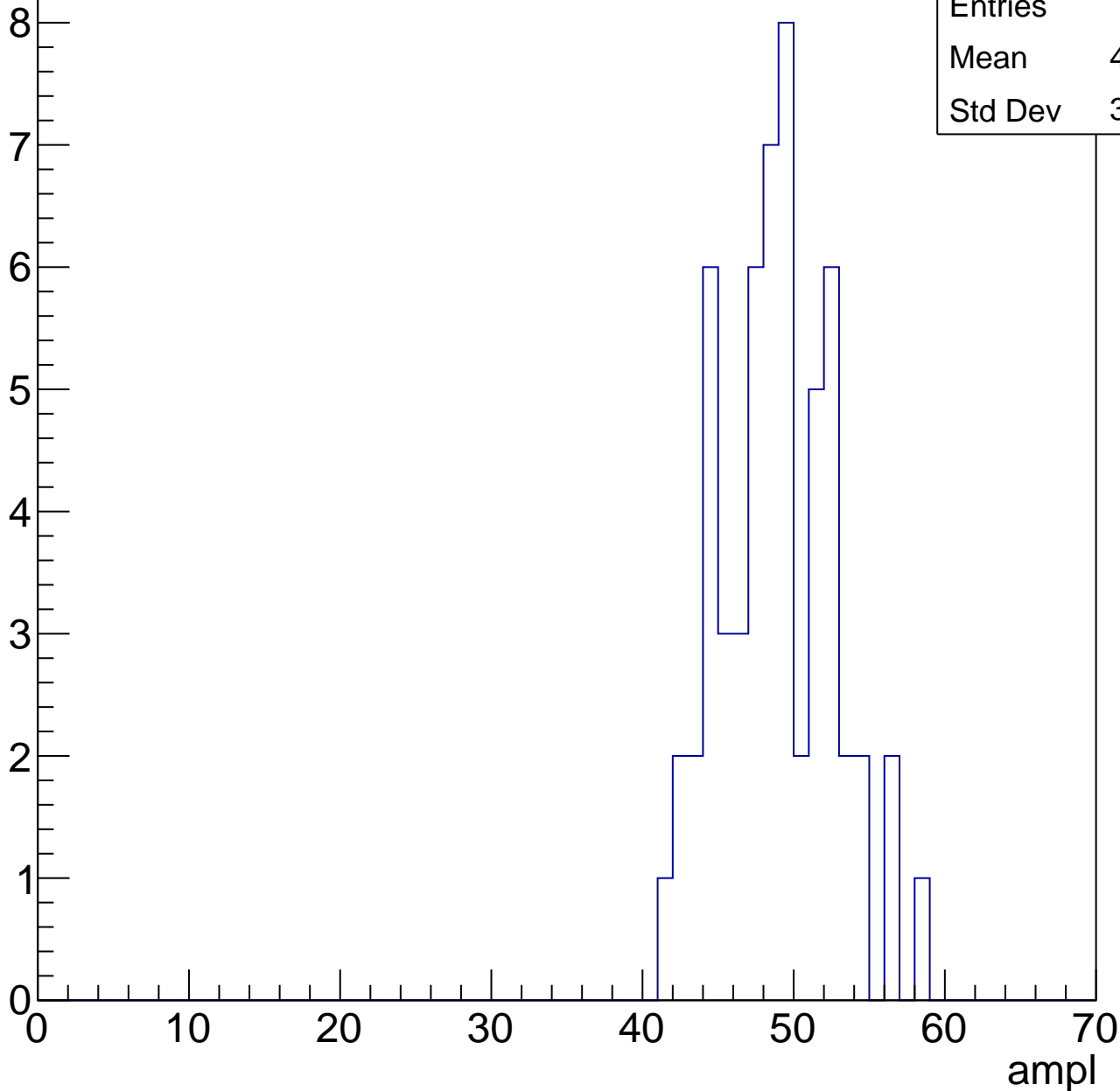


# B1L102S, U5-ch78, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	48.43
Std Dev	3.733

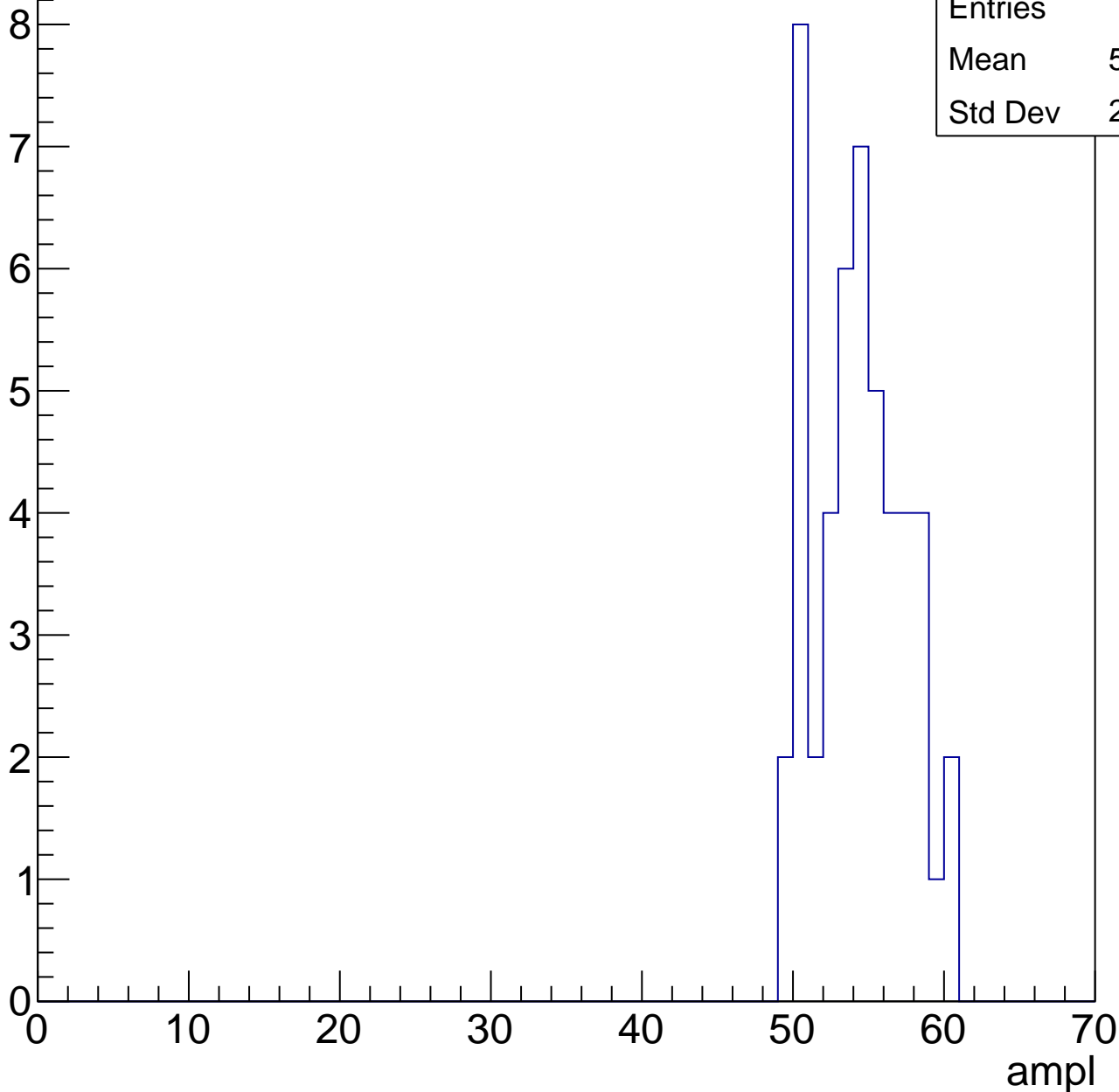


# B1L102S, U5-ch78, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	53.92
Std Dev	2.982



# B1L102S, U5-ch78, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

7

6

5

4

3

2

1

0

Entries 53

Mean 58.91

Std Dev 2.935

ampl

0

10

20

30

40

50

60

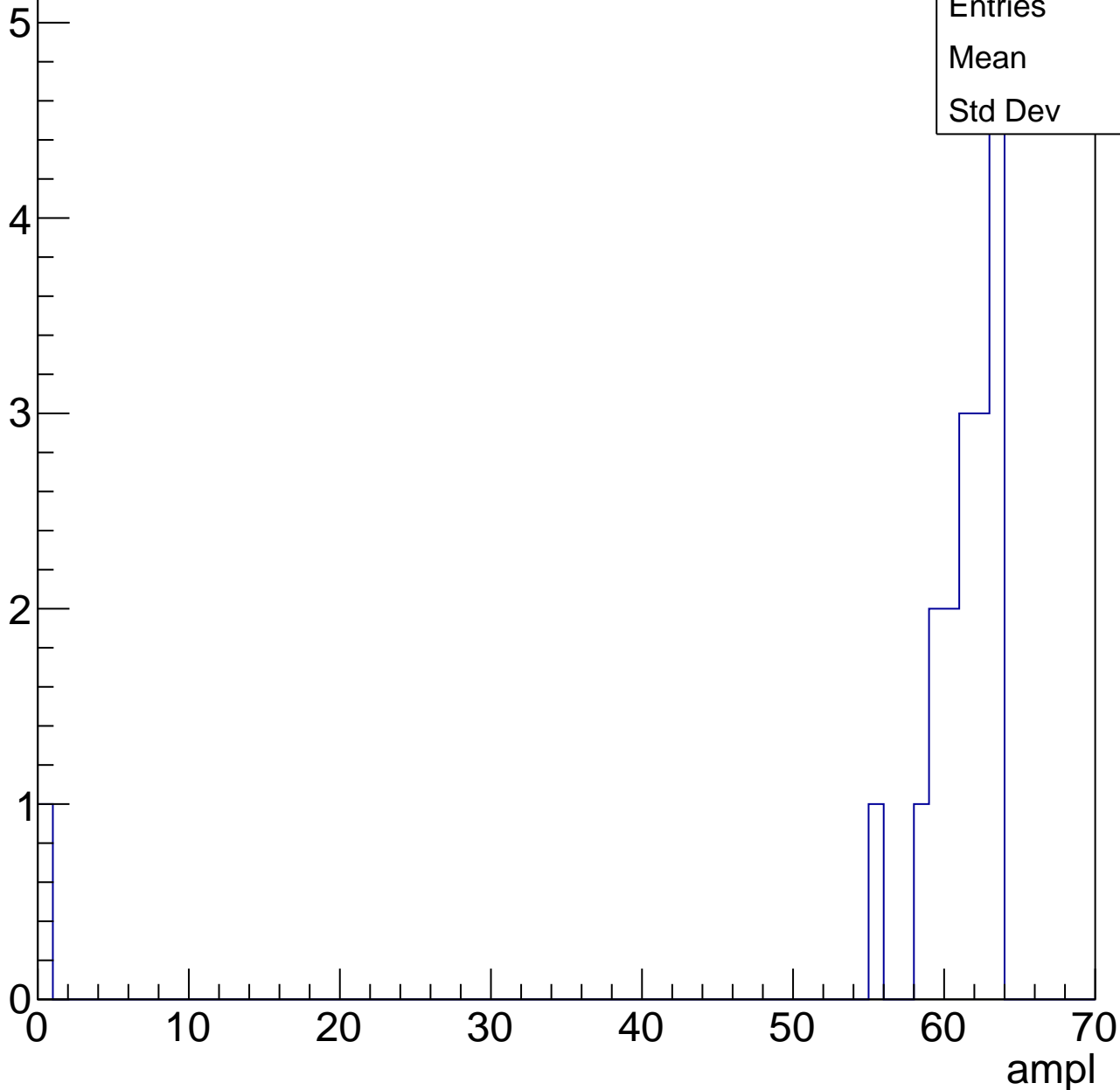
70

# B1L102S, U5-ch78, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	18
Mean	57.5
Std Dev	14.1





# B1L102S, U5-ch78, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U5-ch79, adc0

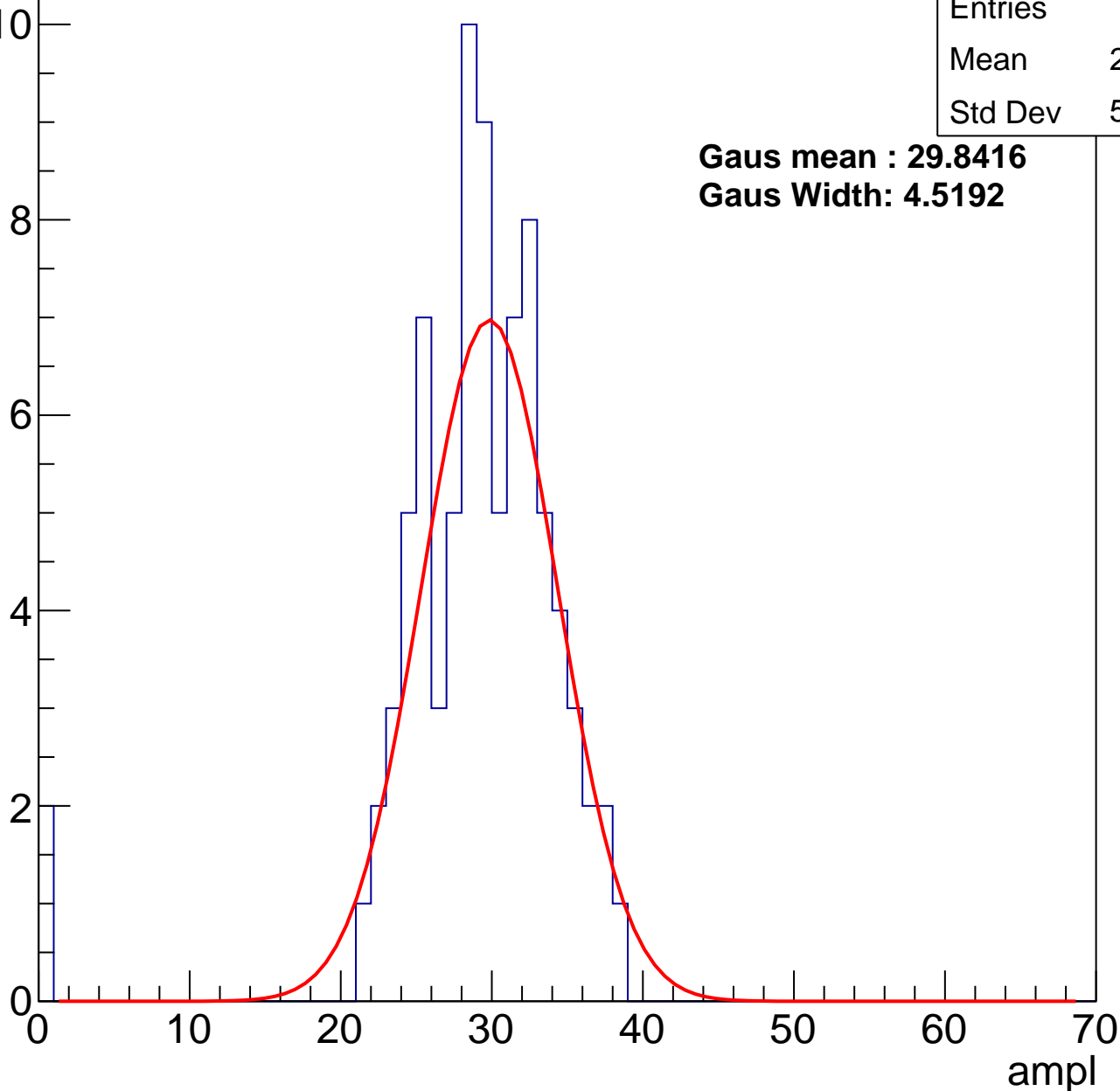
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	84
Mean	28.52
Std Dev	5.903

**Gaus mean : 29.8416**

**Gaus Width: 4.5192**



# B1L102S, U5-ch79, adc1

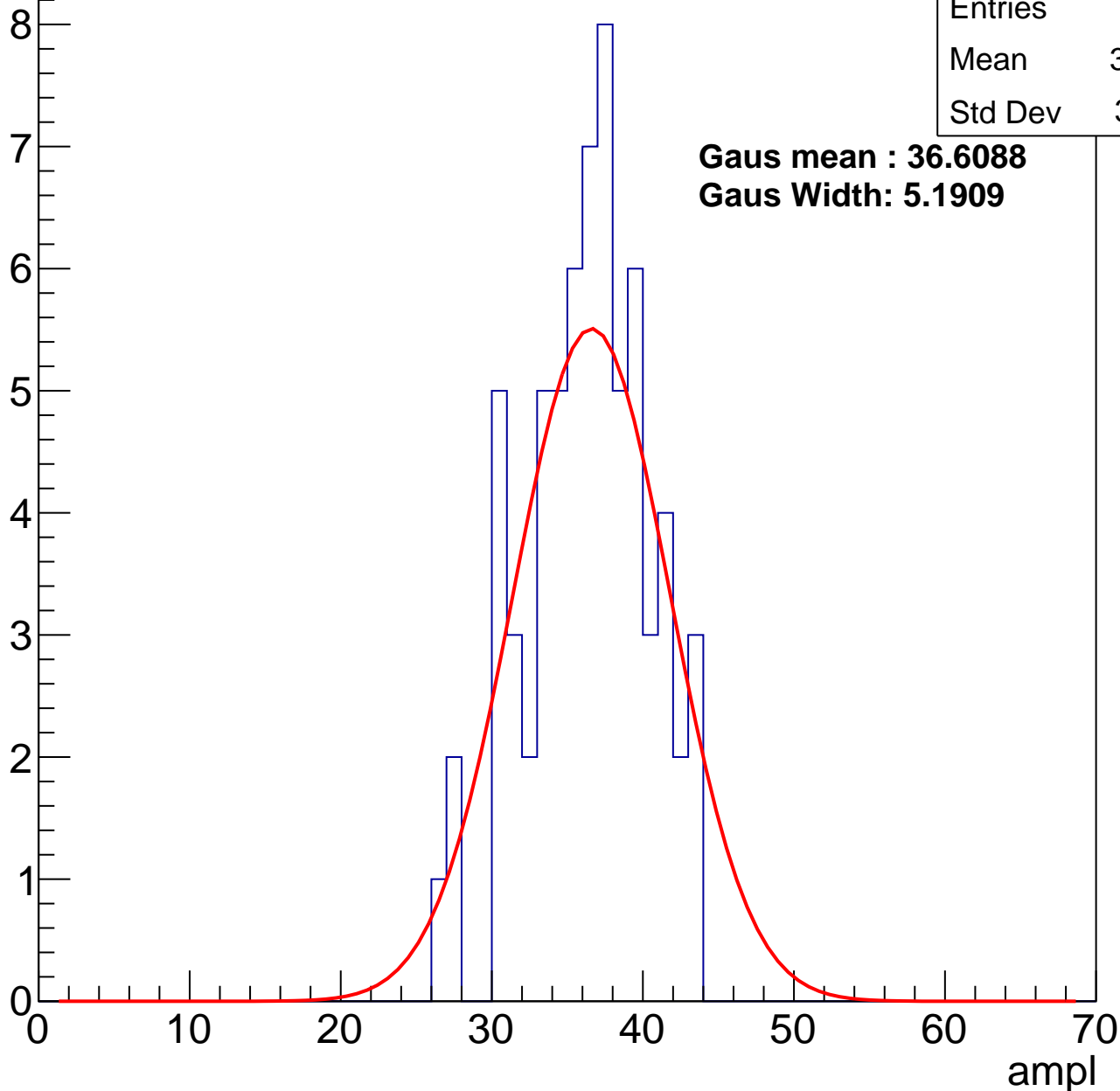
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	35.84
Std Dev	3.991

**Gaus mean : 36.6088**

**Gaus Width: 5.1909**



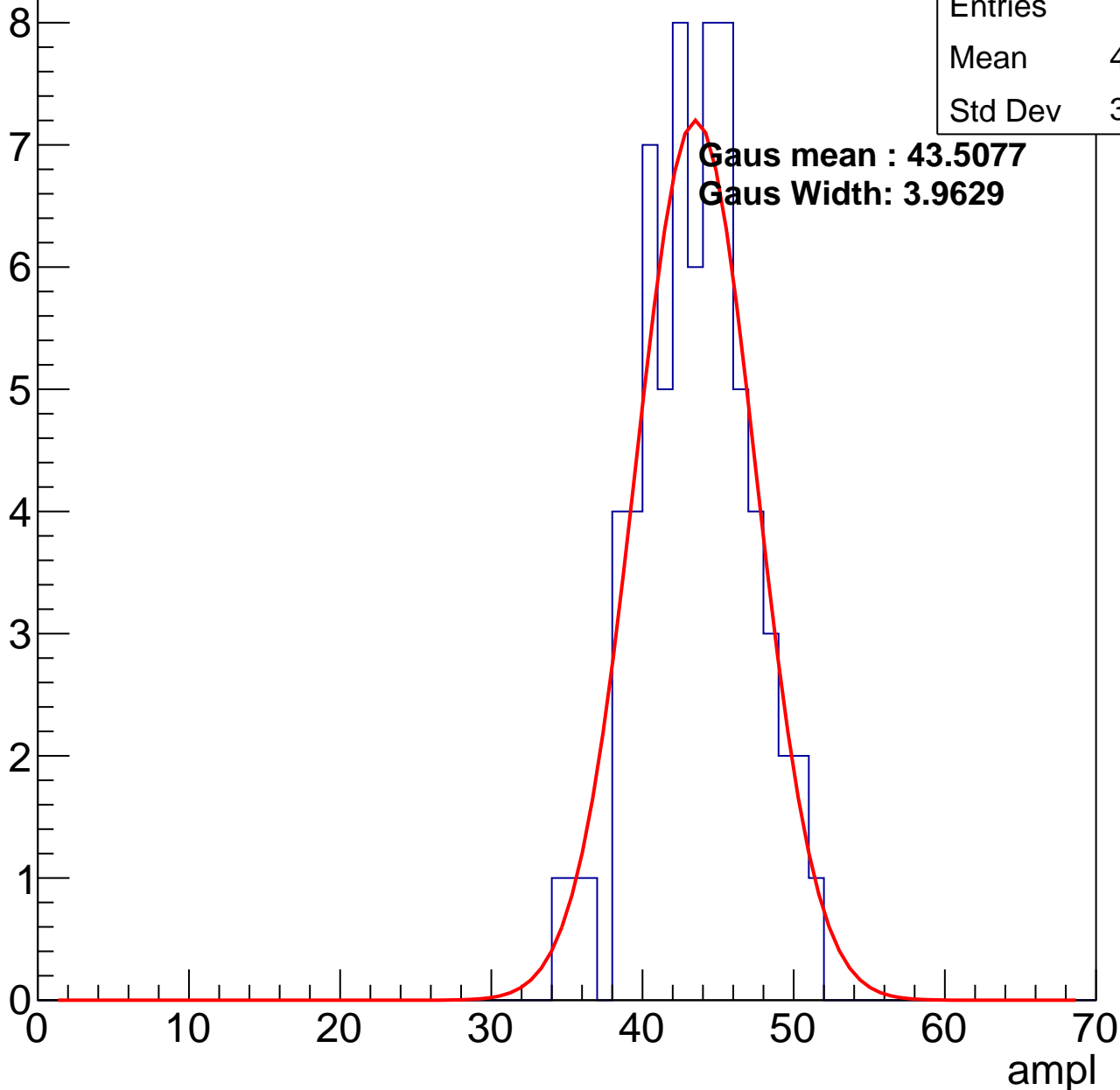
# B1L102S, U5-ch79, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	43.07
Std Dev	3.599

**Gaus mean : 43.5077**  
**Gaus Width: 3.9629**

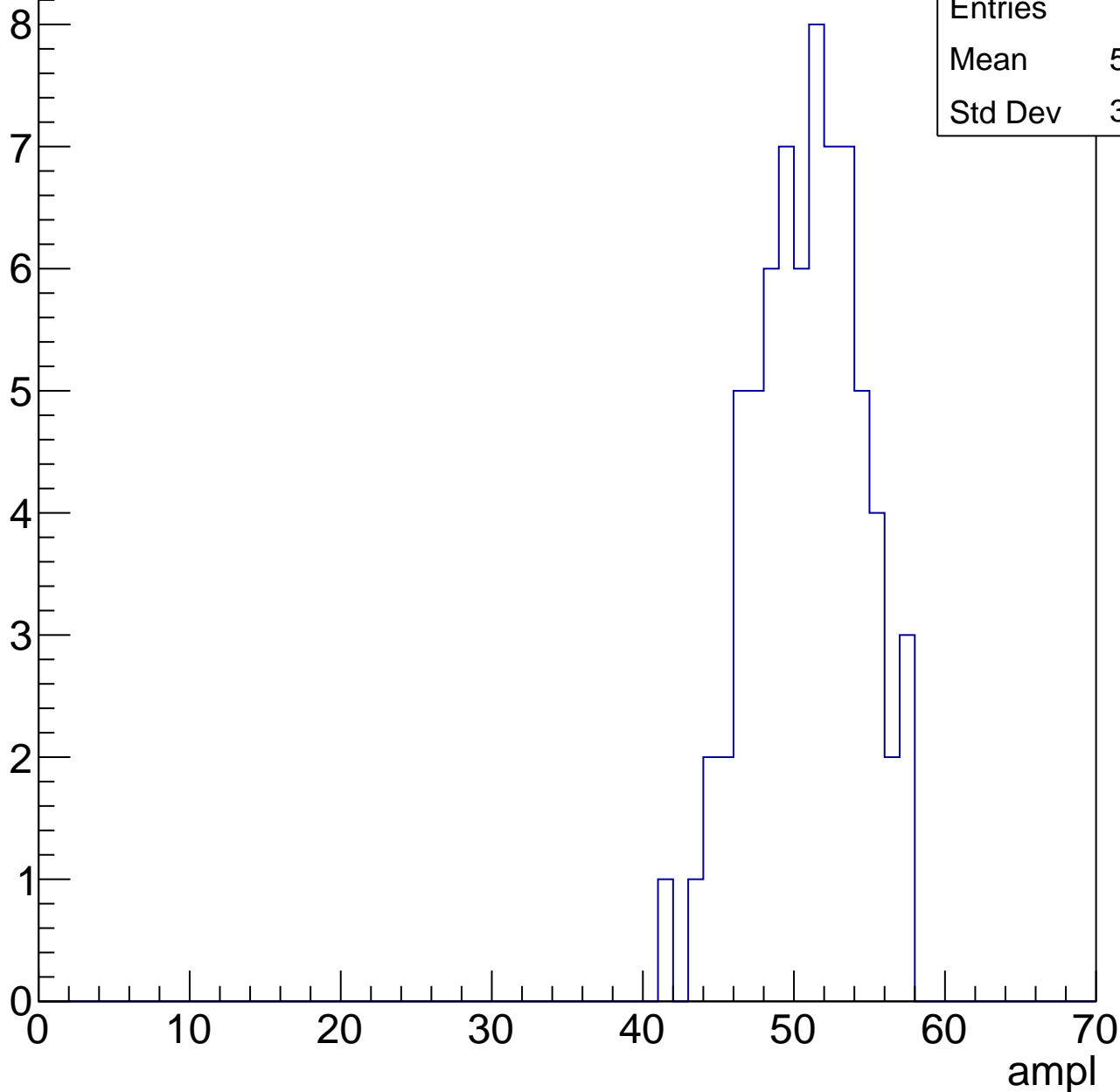


# B1L102S, U5-ch79, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	50.34
Std Dev	3.556

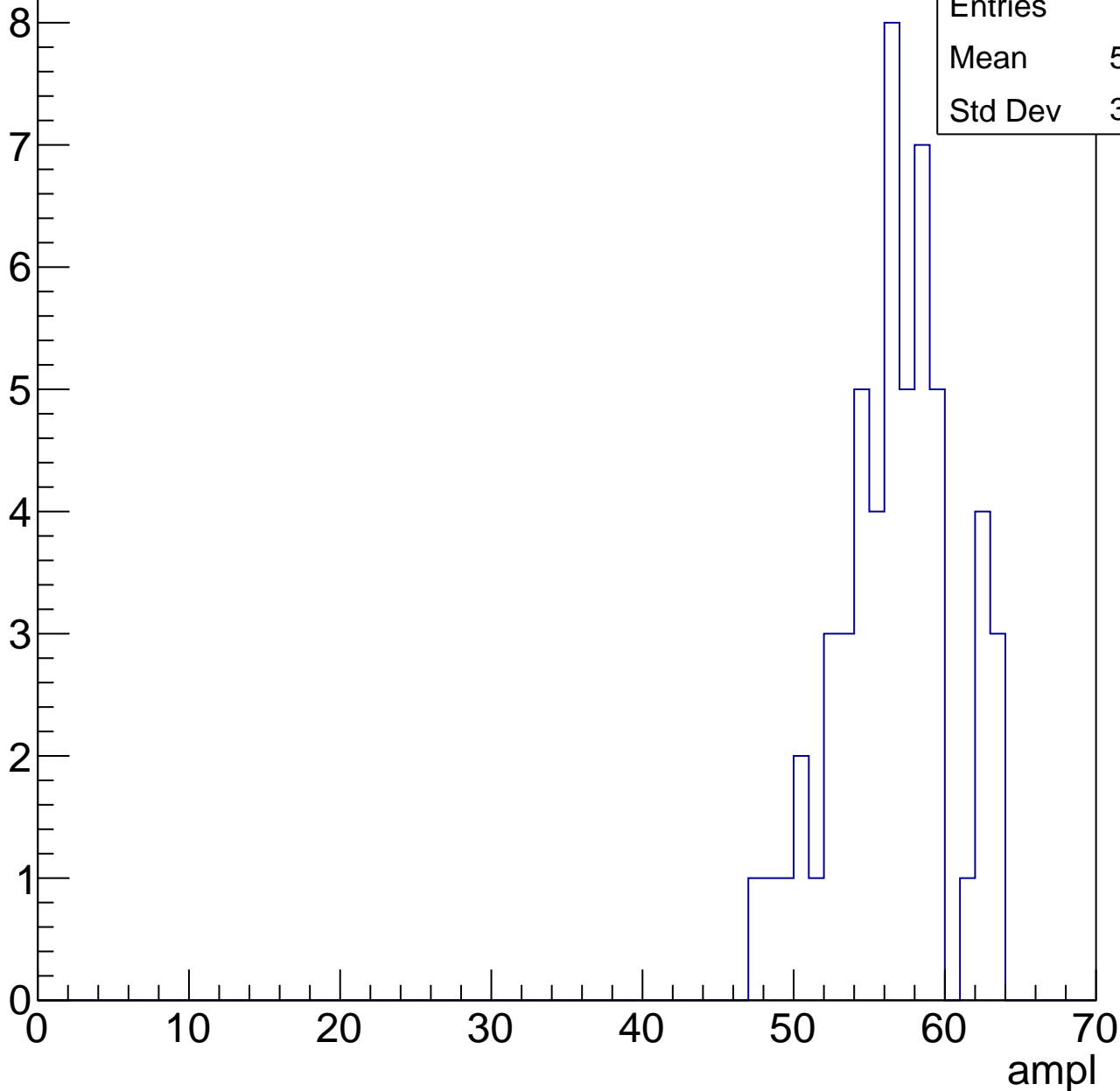


# B1L102S, U5-ch79, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	56.15
Std Dev	3.807



# B1L102S, U5-ch79, adc5

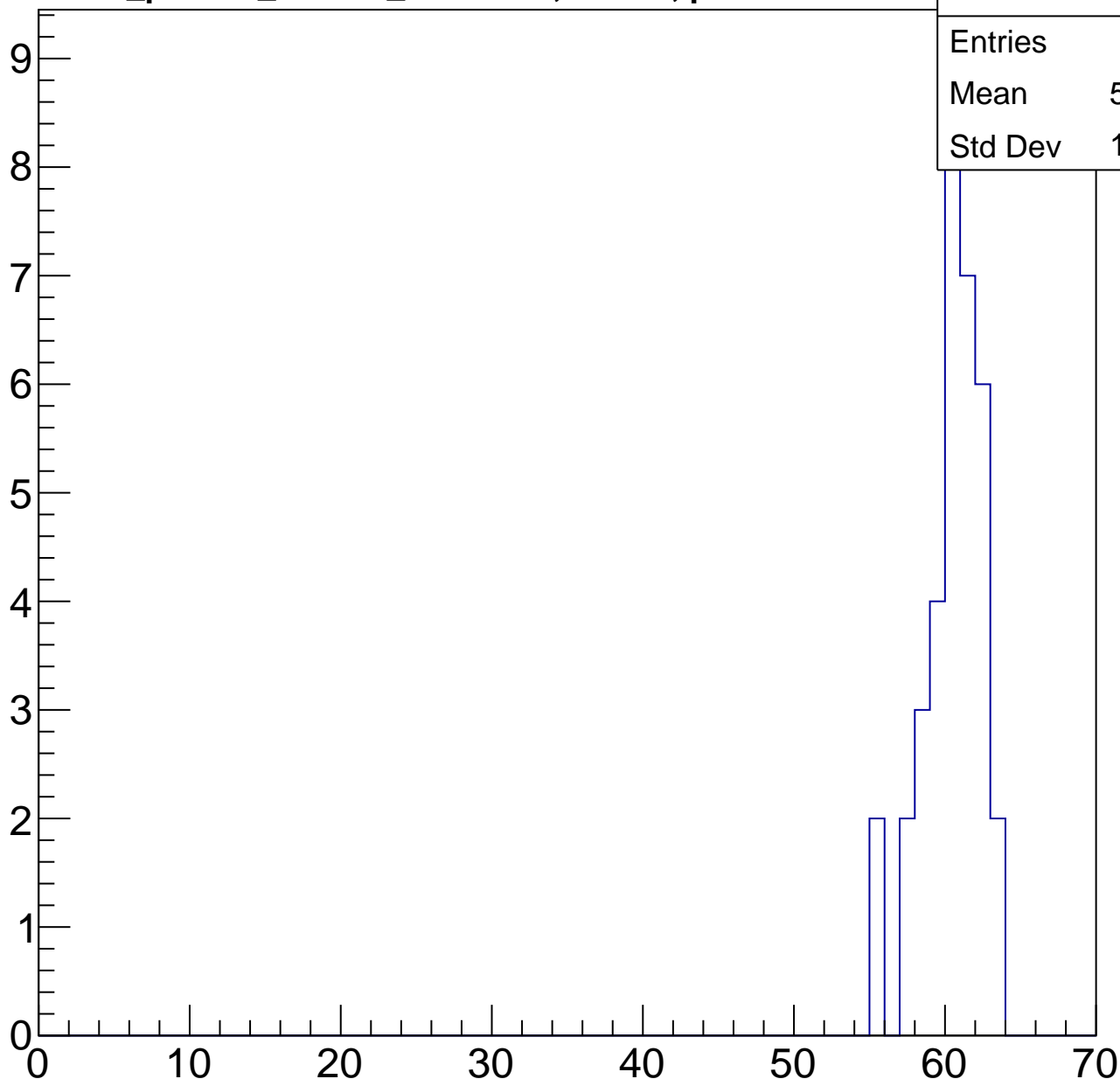
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	35
Mean	59.97
Std Dev	1.949

ampl

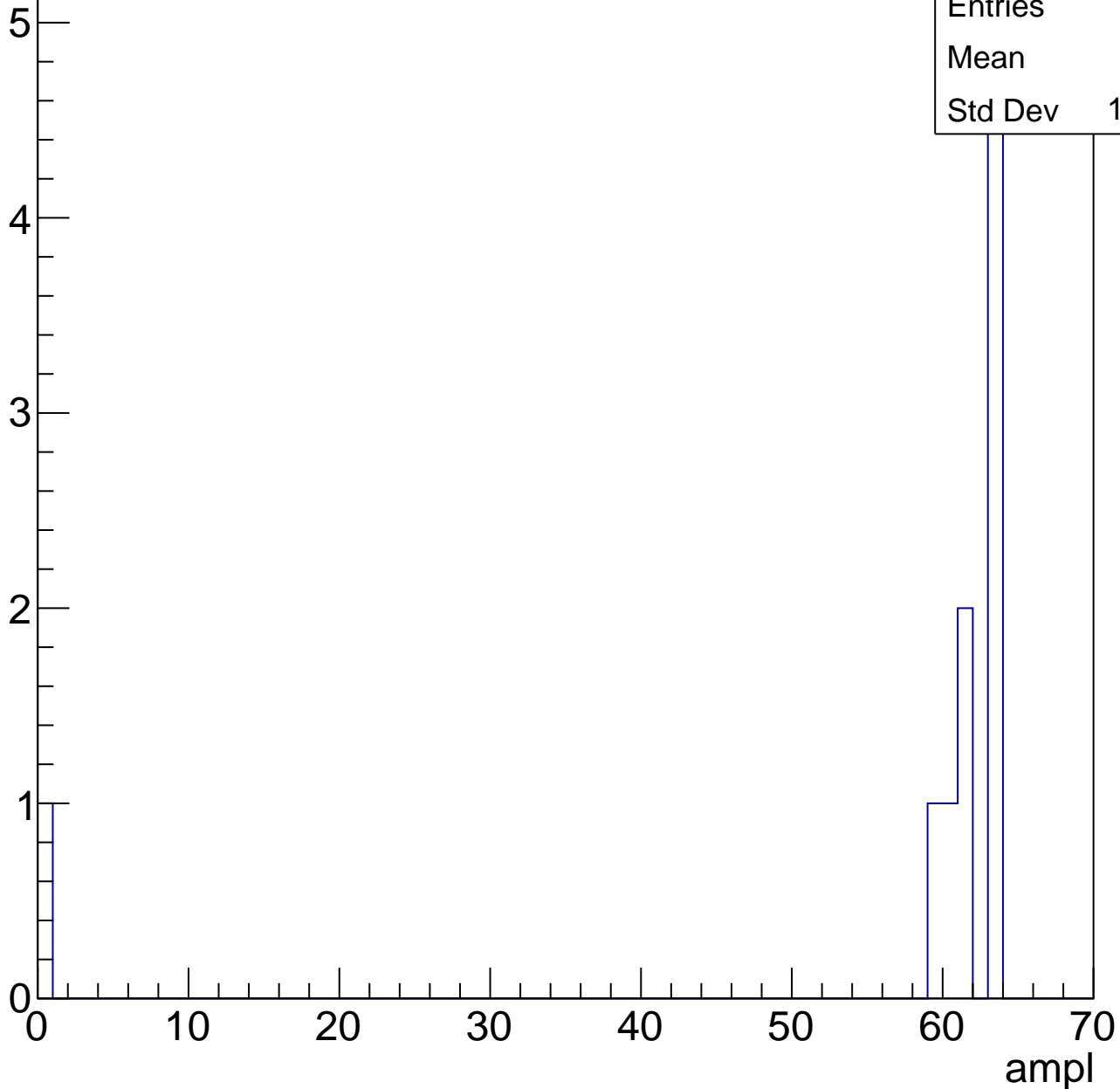


# B1L102S, U5-ch79, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	10
Mean	55.6
Std Dev	18.59





# B1L102S, U5-ch79, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U5-ch80, adc0

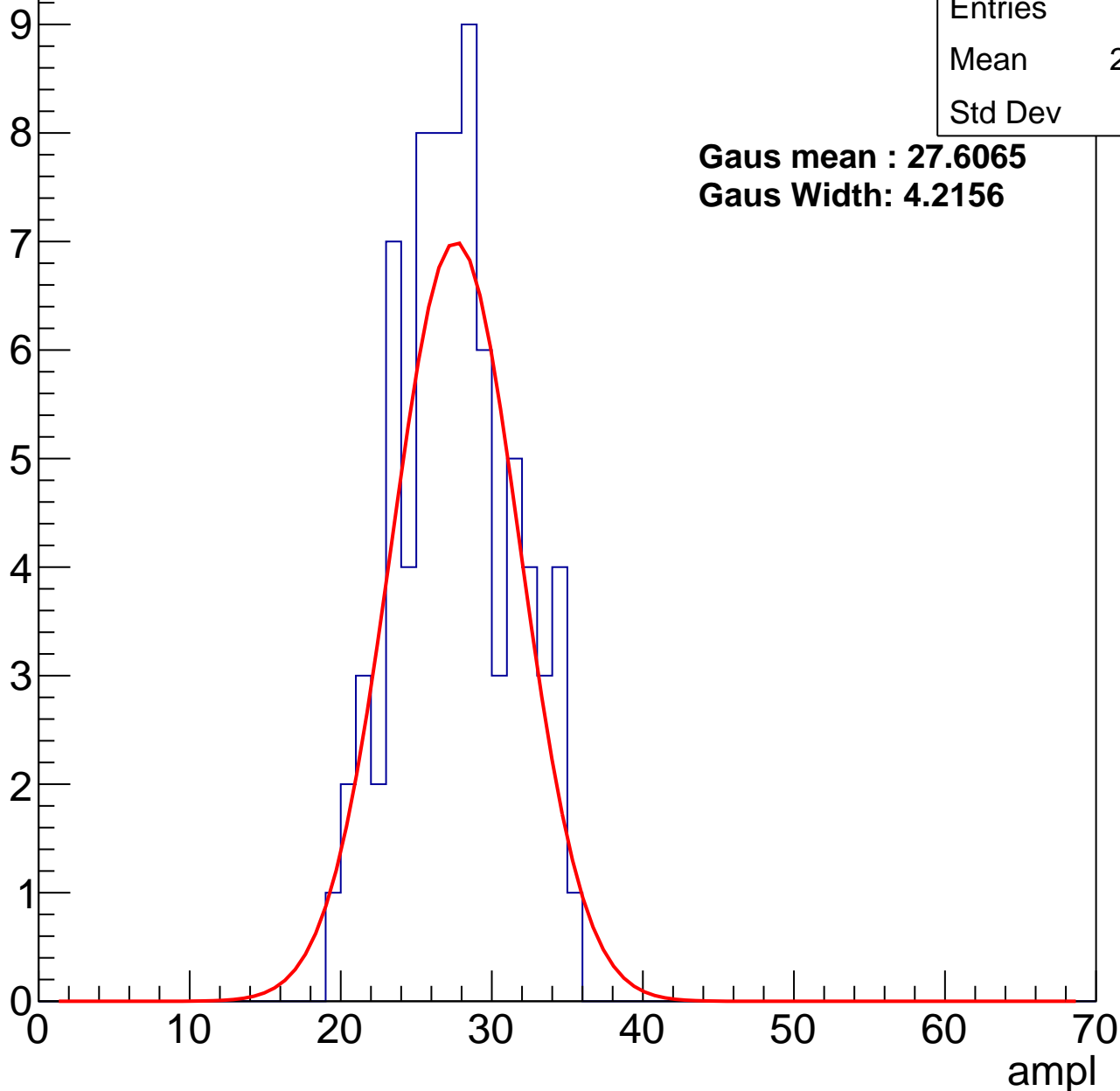
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	78
Mean	27.13
Std Dev	3.78

**Gaus mean : 27.6065**

**Gaus Width: 4.2156**



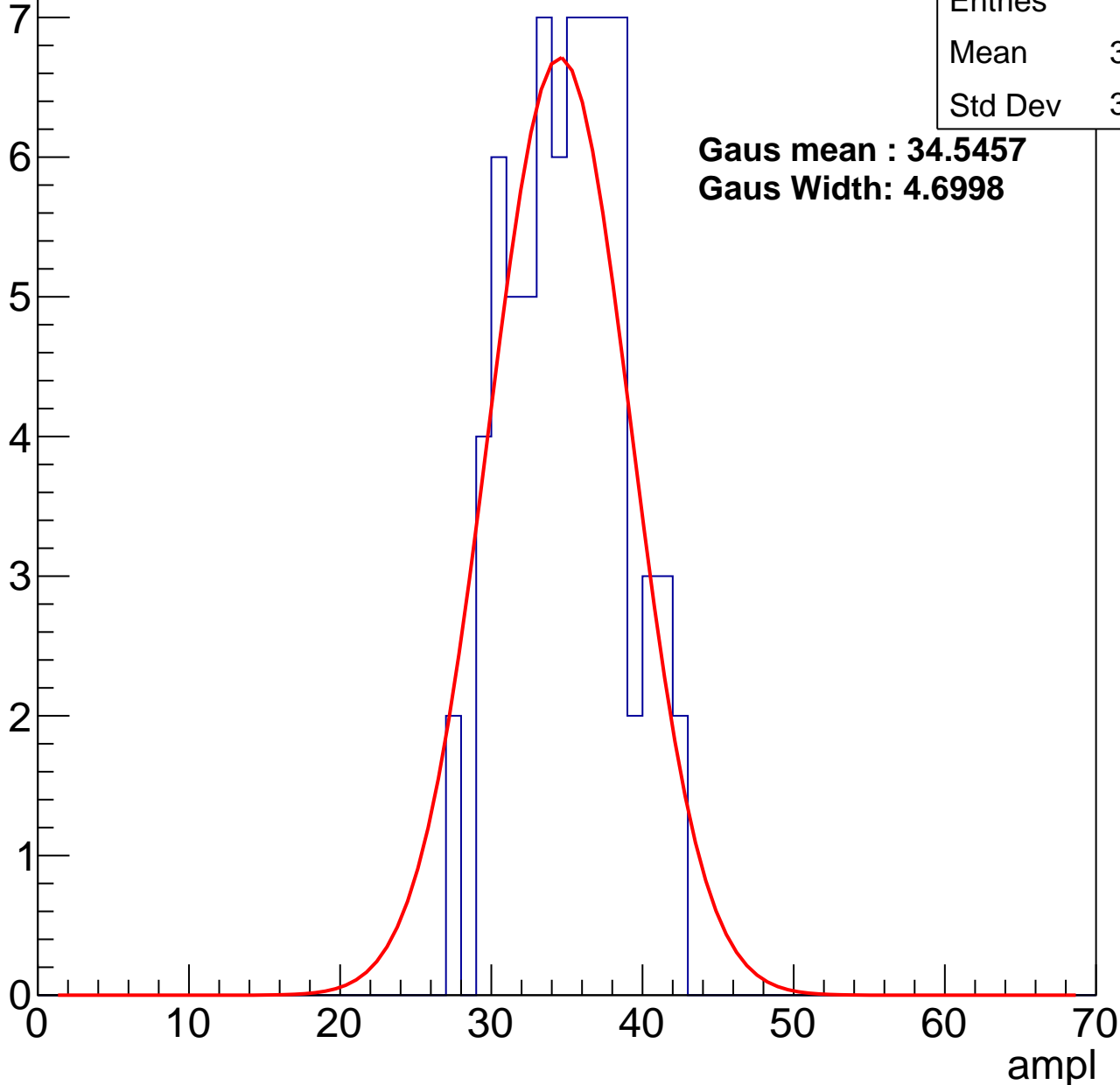
# B1L102S, U5-ch80, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	34.62
Std Dev	3.666

**Gaus mean : 34.5457**  
**Gaus Width: 4.6998**



# B1L102S, U5-ch80, adc2

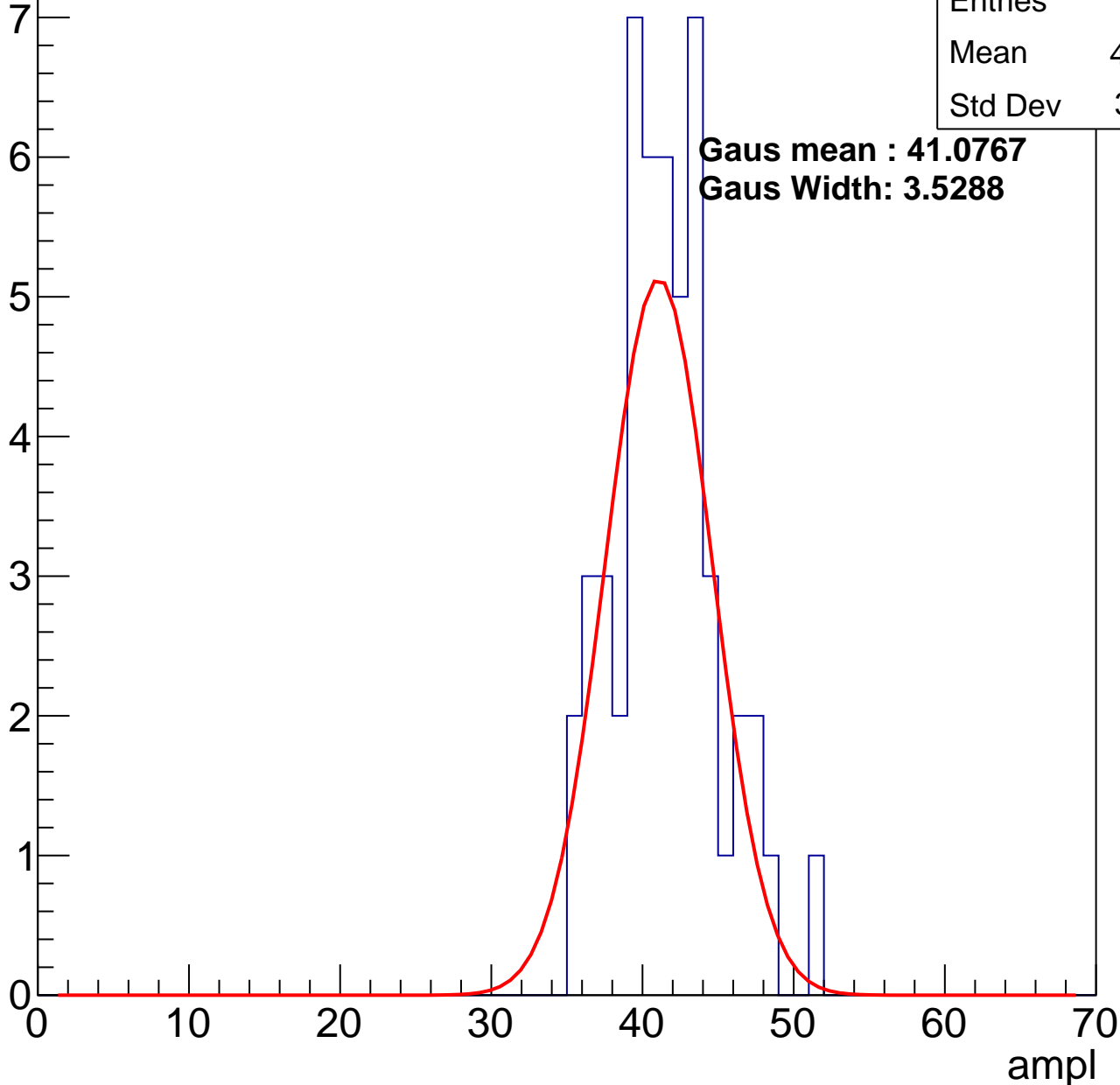
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	41.12
Std Dev	3.411

**Gaus mean : 41.0767**

**Gaus Width: 3.5288**



# B1L102S, U5-ch80, adc3

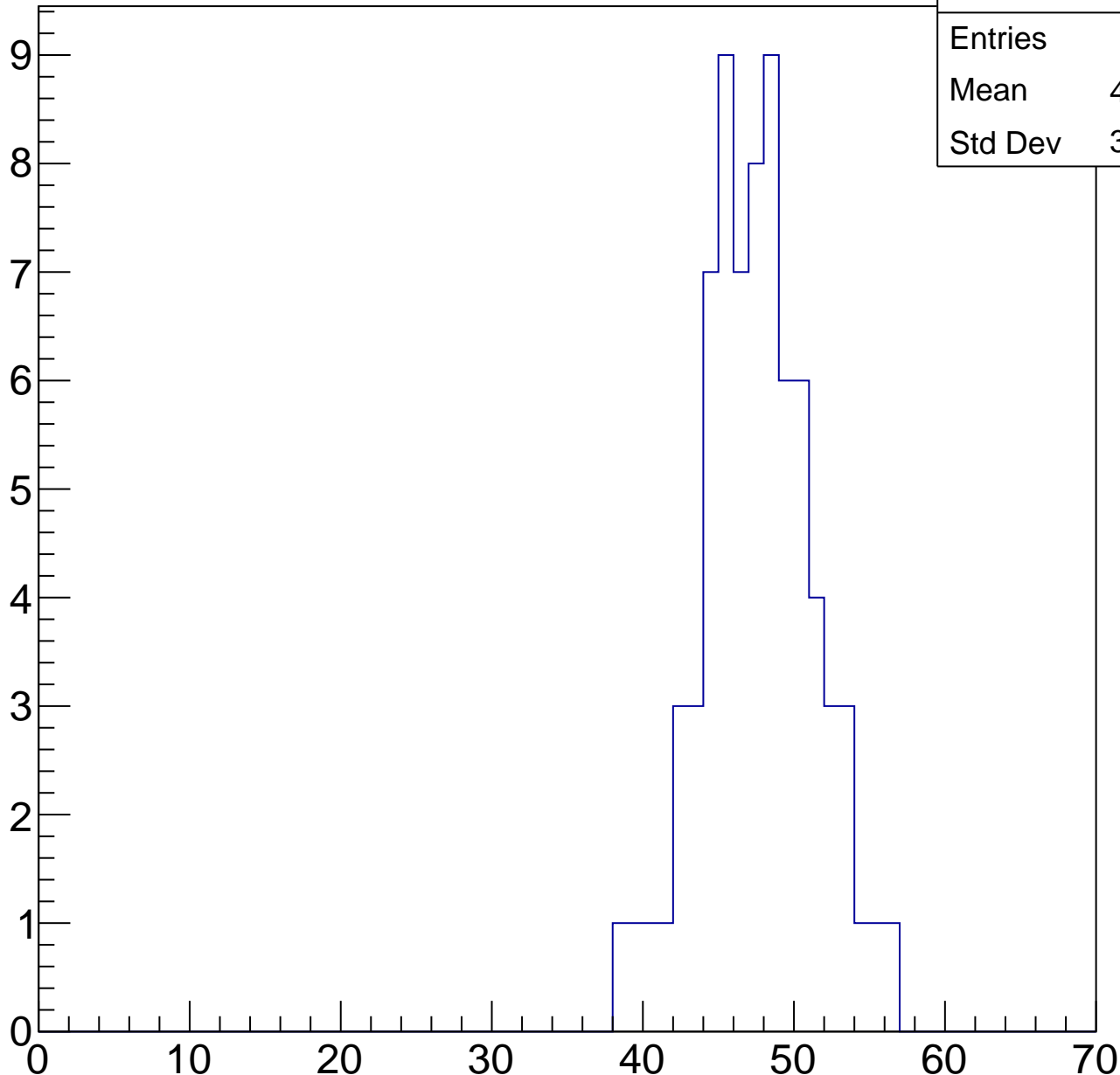
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

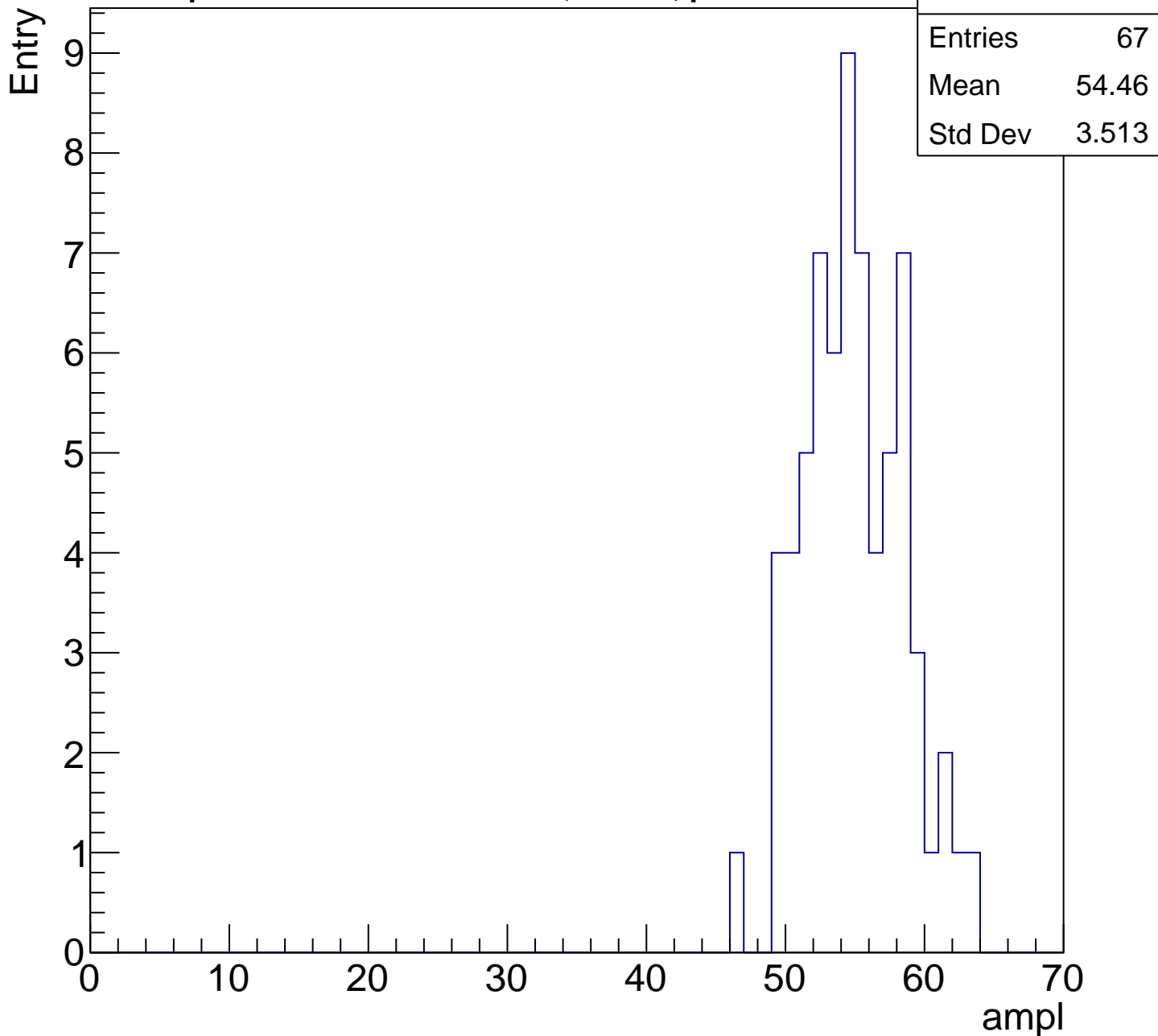
Entries	75
Mean	47.12
Std Dev	3.626

ampl



# B1L102S, U5-ch80, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

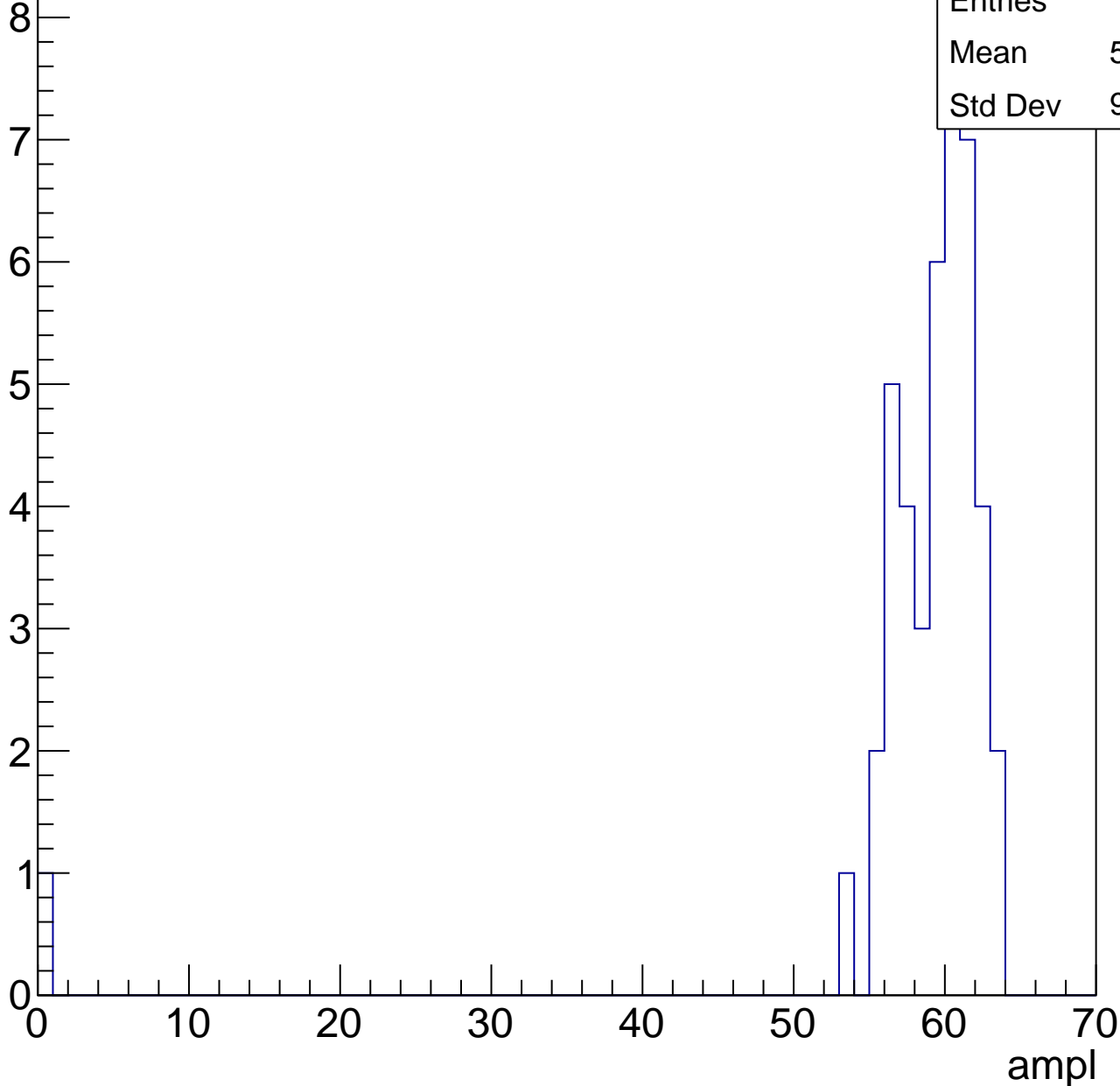


# B1L102S, U5-ch80, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	43
Mean	57.67
Std Dev	9.202

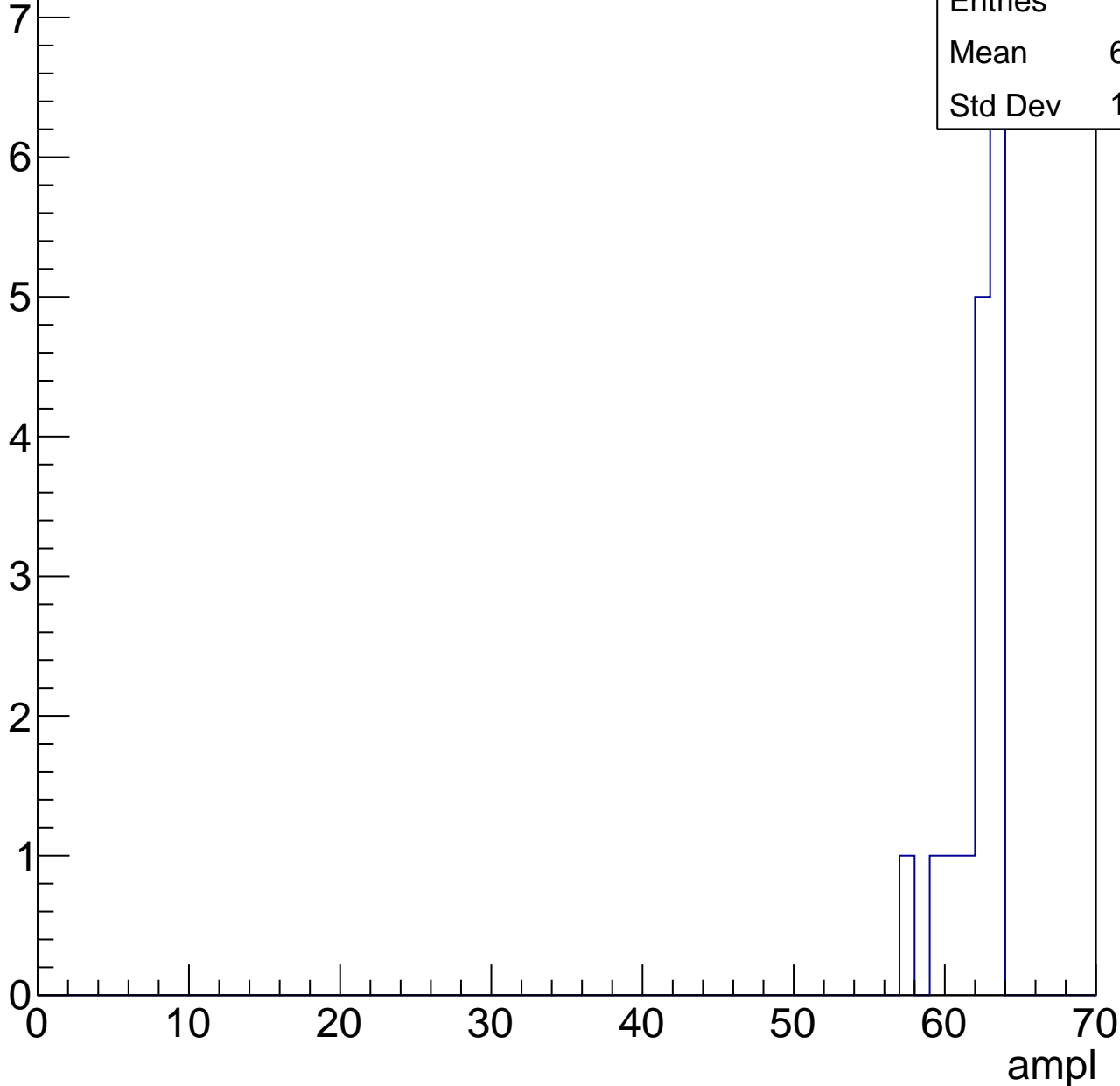


# B1L102S, U5-ch80, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	16
Mean	61.75
Std Dev	1.677





# B1L102S, U5-ch80, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U5-ch81, adc0

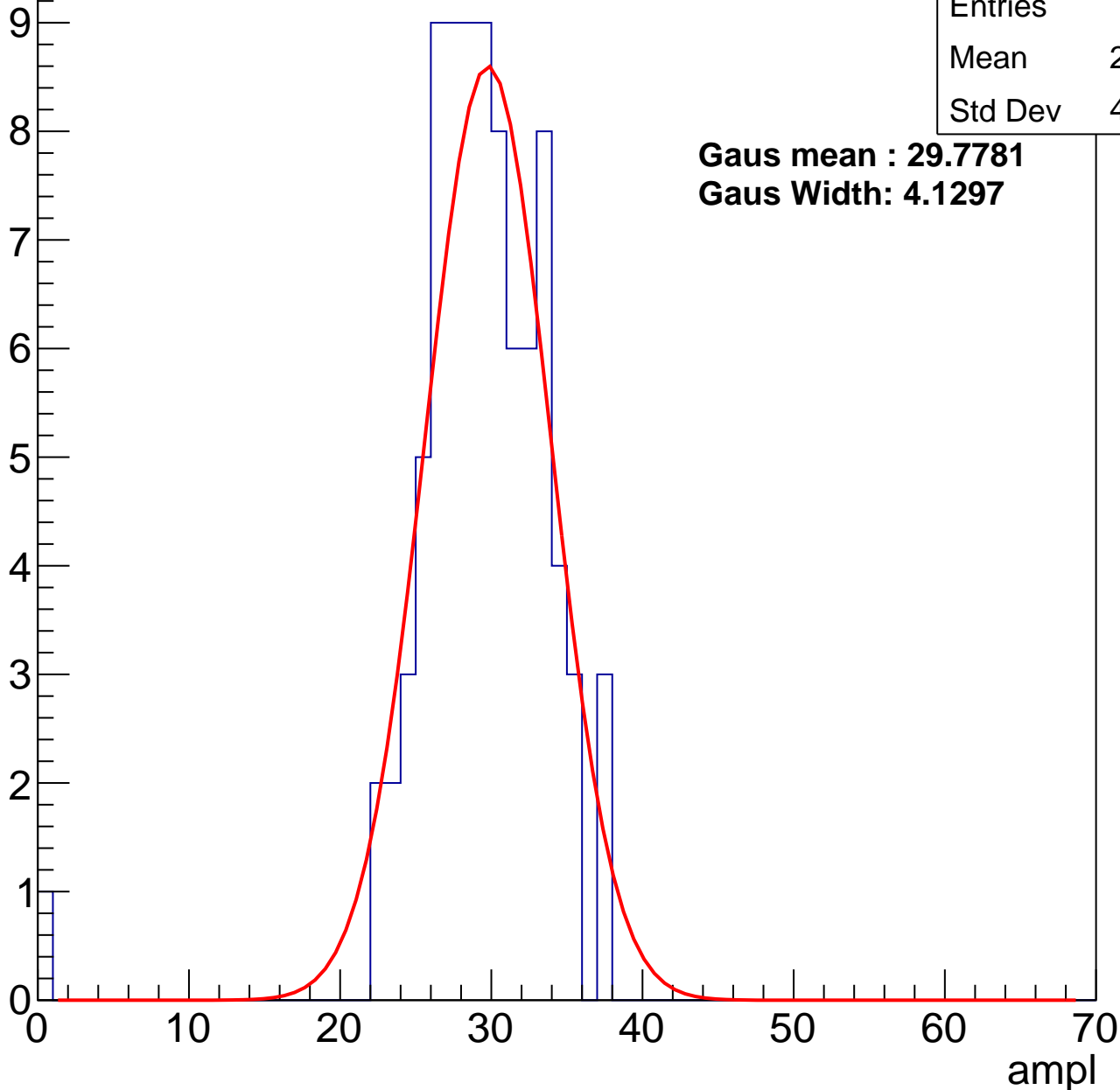
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	87
Mean	28.86
Std Dev	4.679

**Gaus mean : 29.7781**

**Gaus Width: 4.1297**



# B1L102S, U5-ch81, adc1

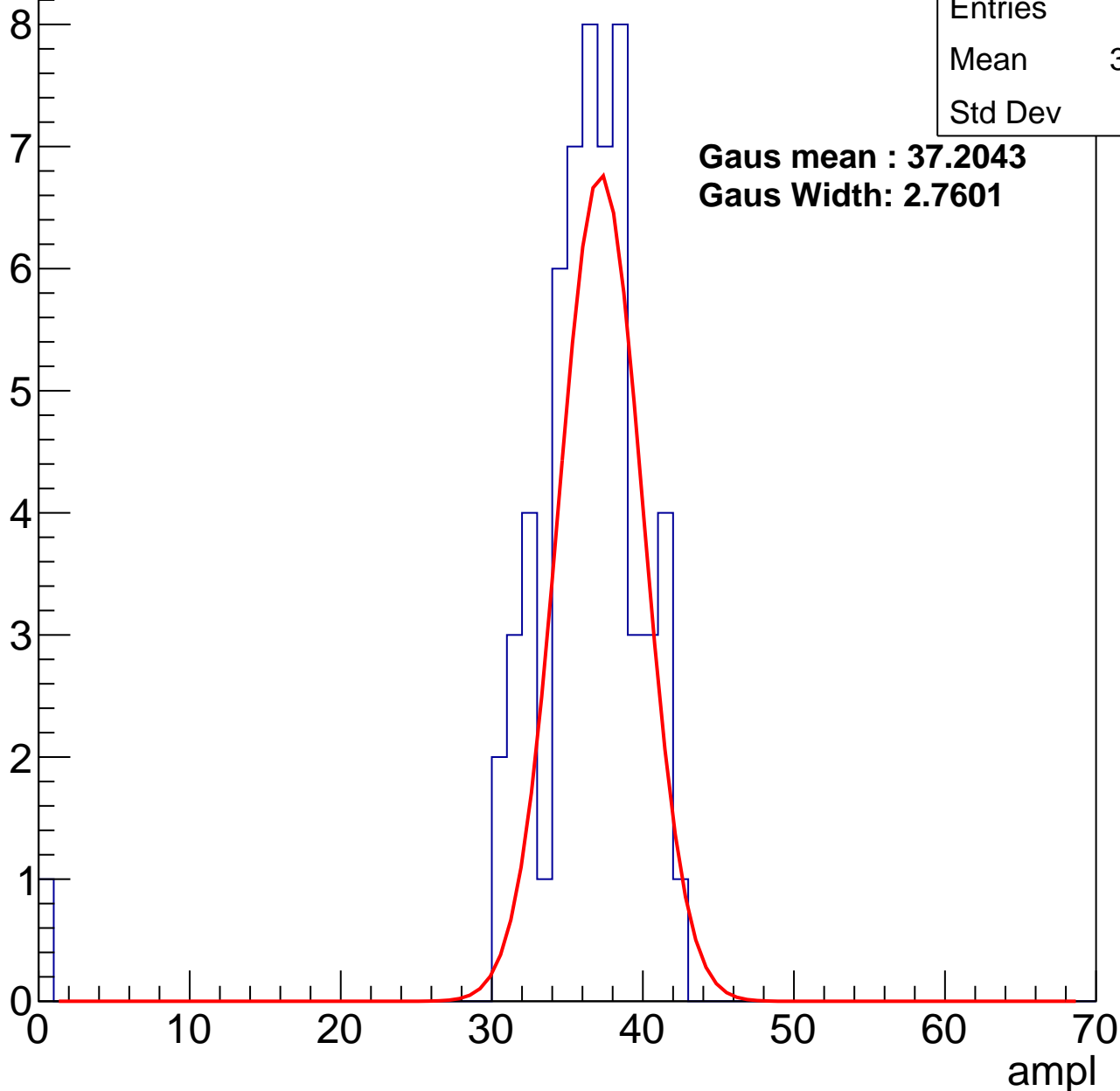
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	35.47
Std Dev	5.54

**Gaus mean : 37.2043**

**Gaus Width: 2.7601**



# B1L102S, U5-ch81, adc2

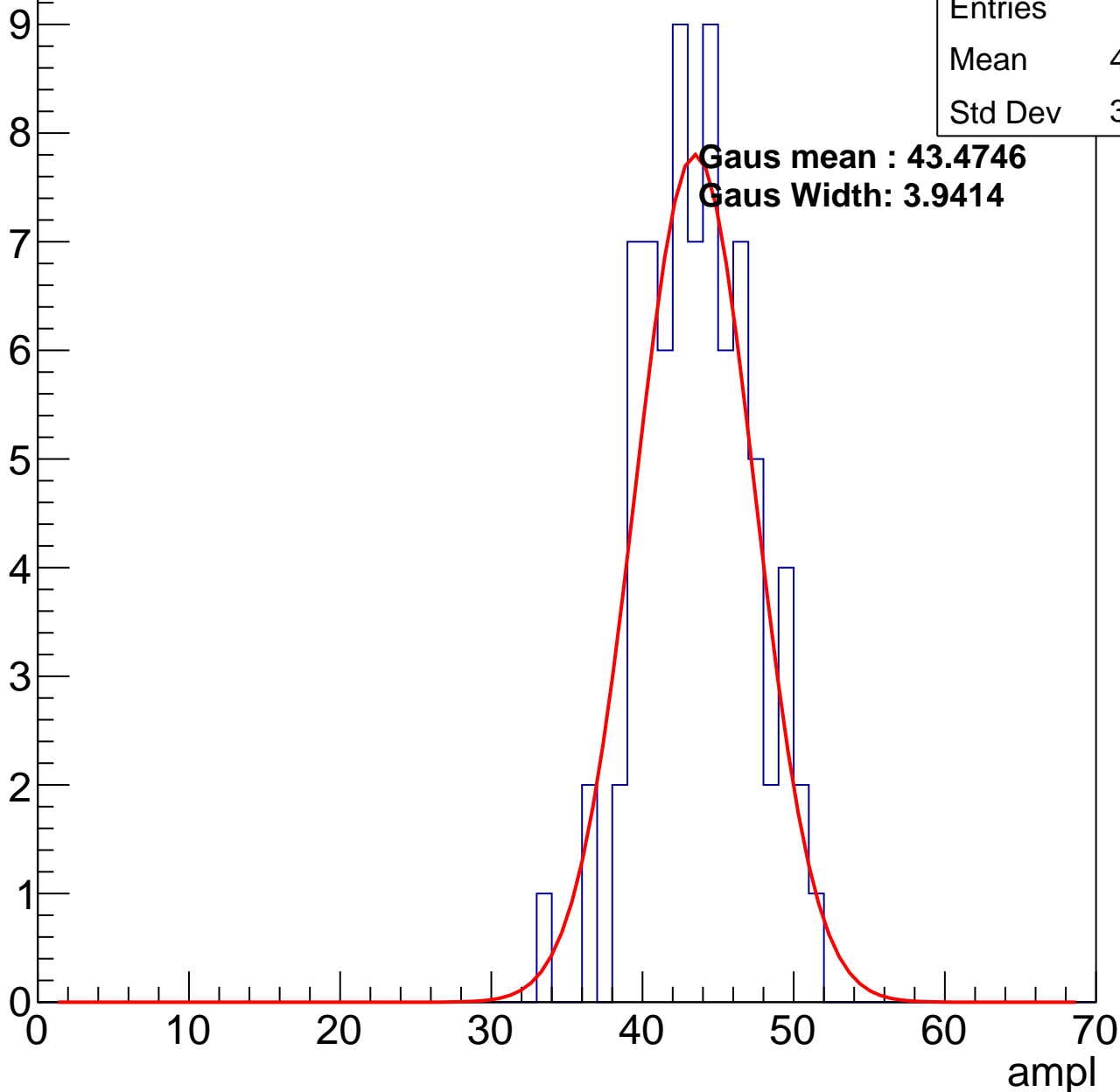
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	43.18
Std Dev	3.577

**Gaus mean : 43.4746**

**Gaus Width: 3.9414**

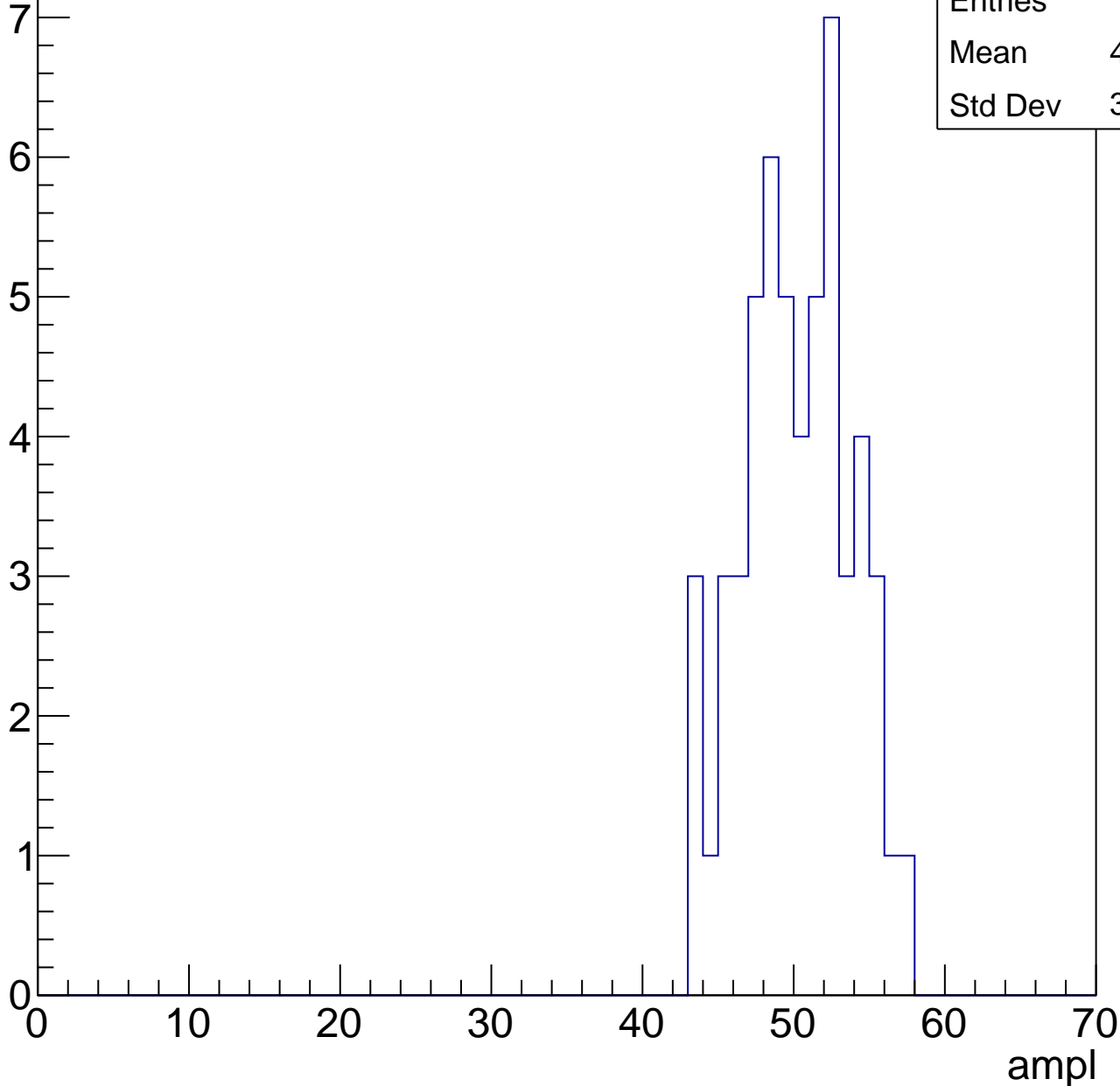


# B1L102S, U5-ch81, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	49.74
Std Dev	3.497

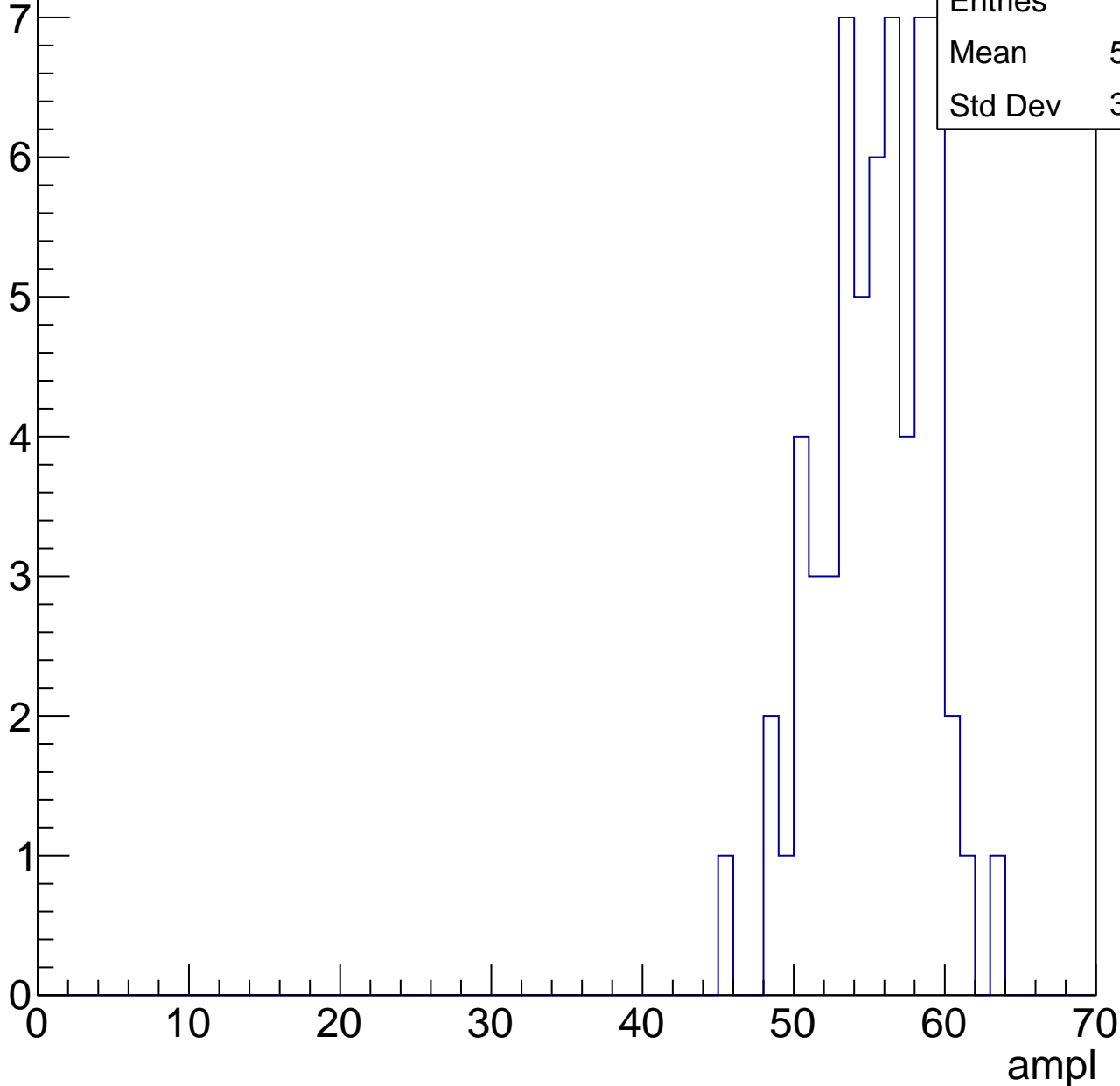


# B1L102S, U5-ch81, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	54.97
Std Dev	3.599

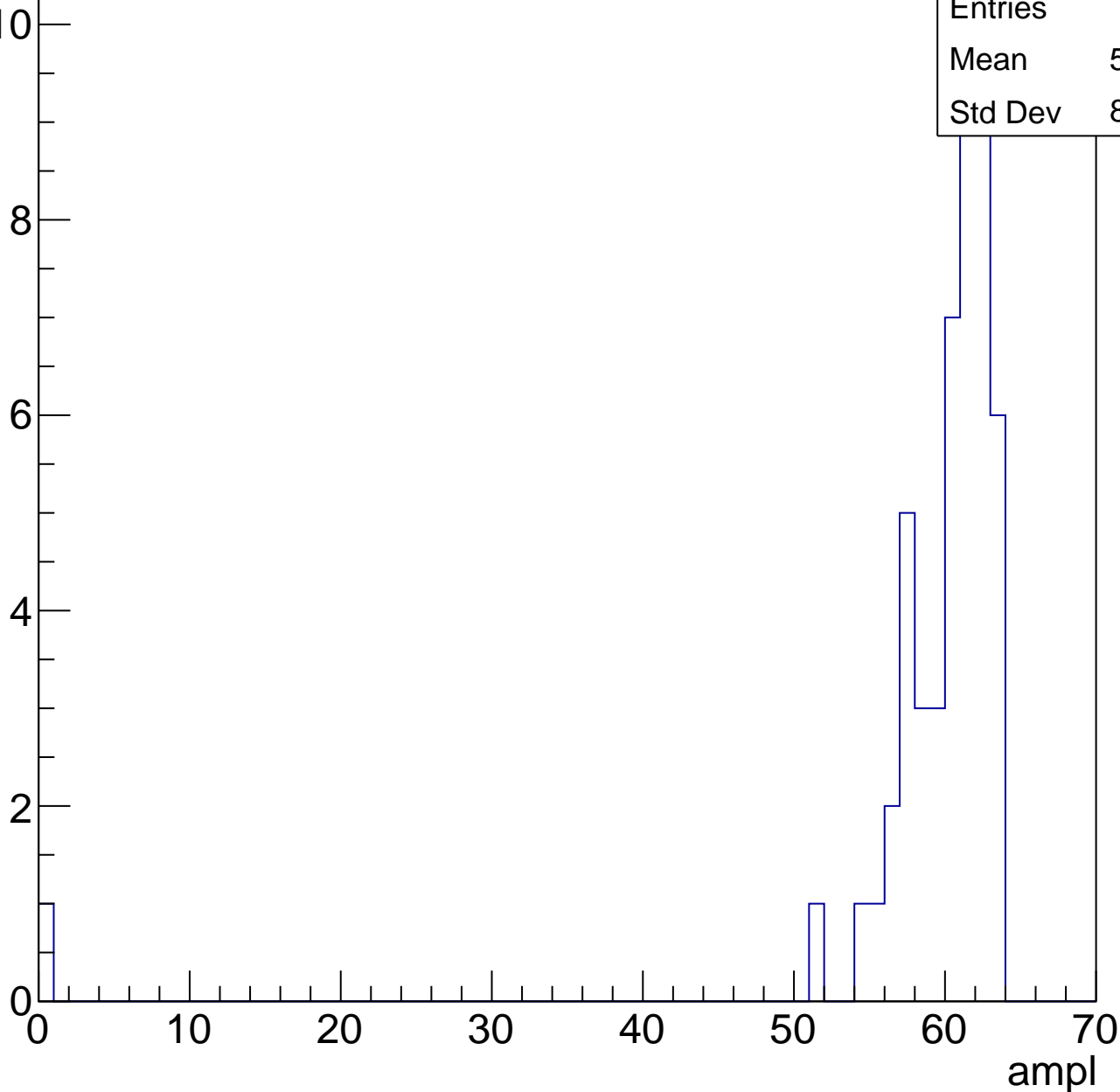


# B1L102S, U5-ch81, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

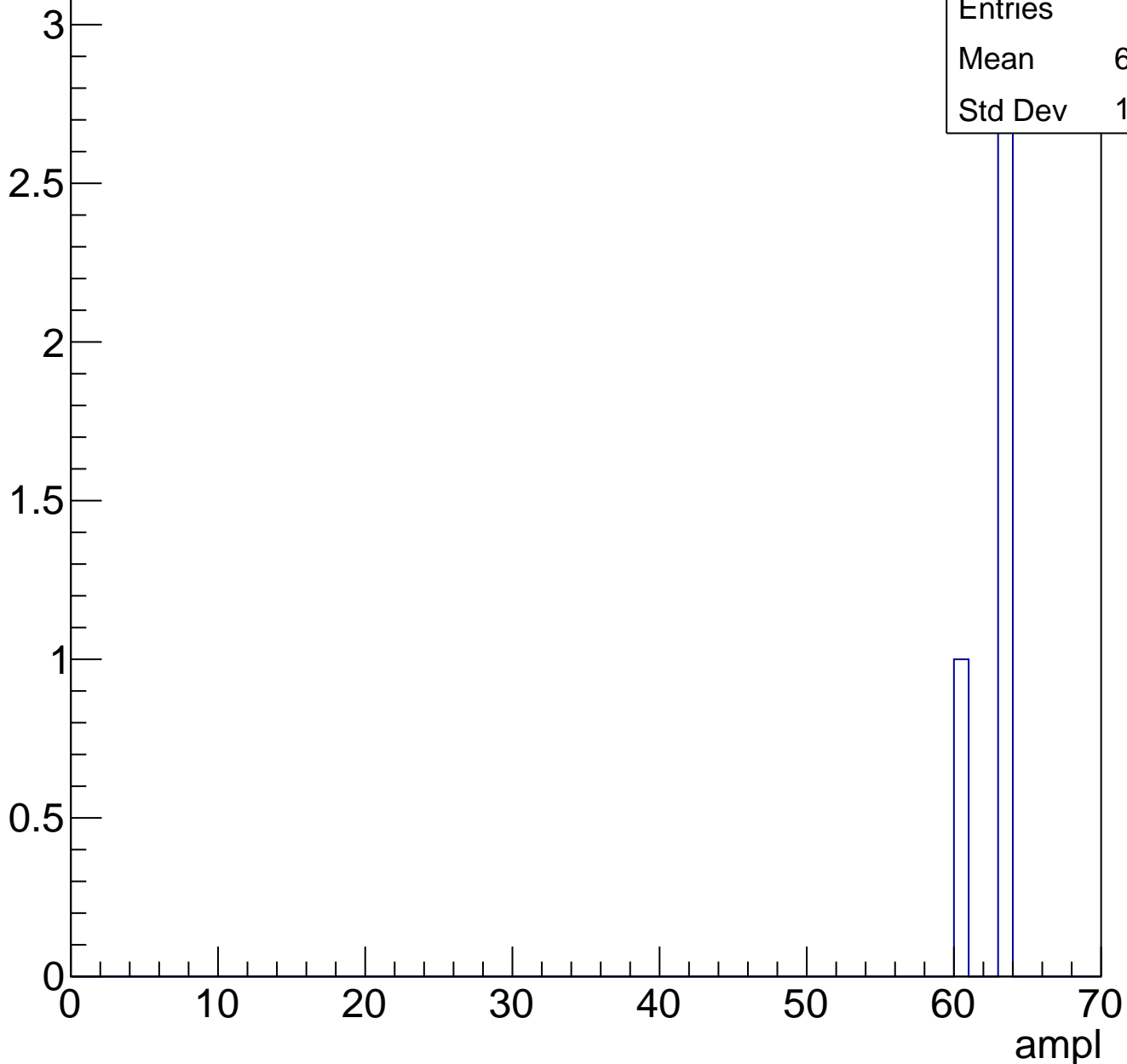
Entries	49
Mean	58.67
Std Dev	8.865



# B1L102S, U5-ch81, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U5-ch81, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U5-ch82, adc0

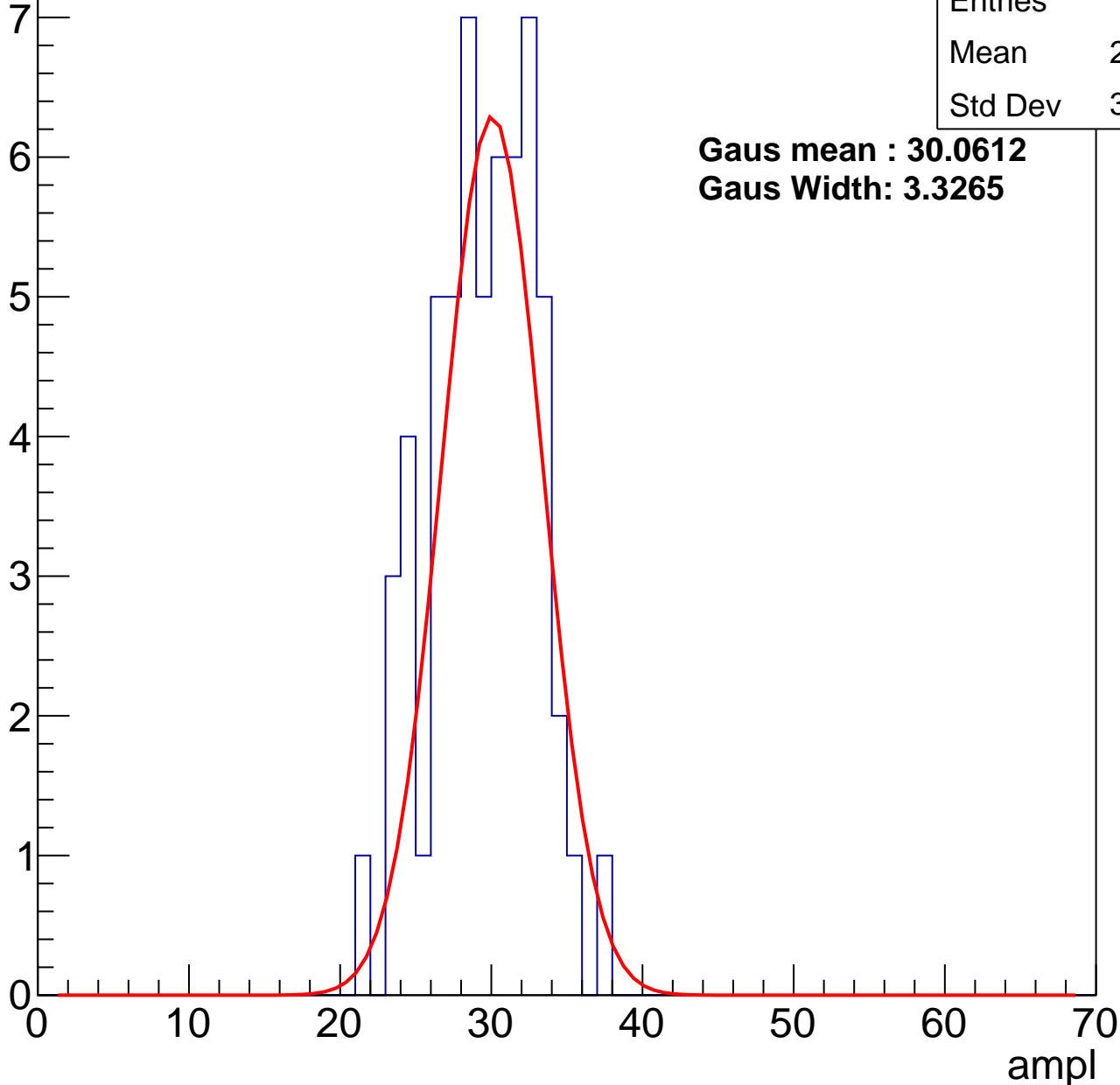
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	29.02
Std Dev	3.402

**Gaus mean : 30.0612**

**Gaus Width: 3.3265**



# B1L102S, U5-ch82, adc1

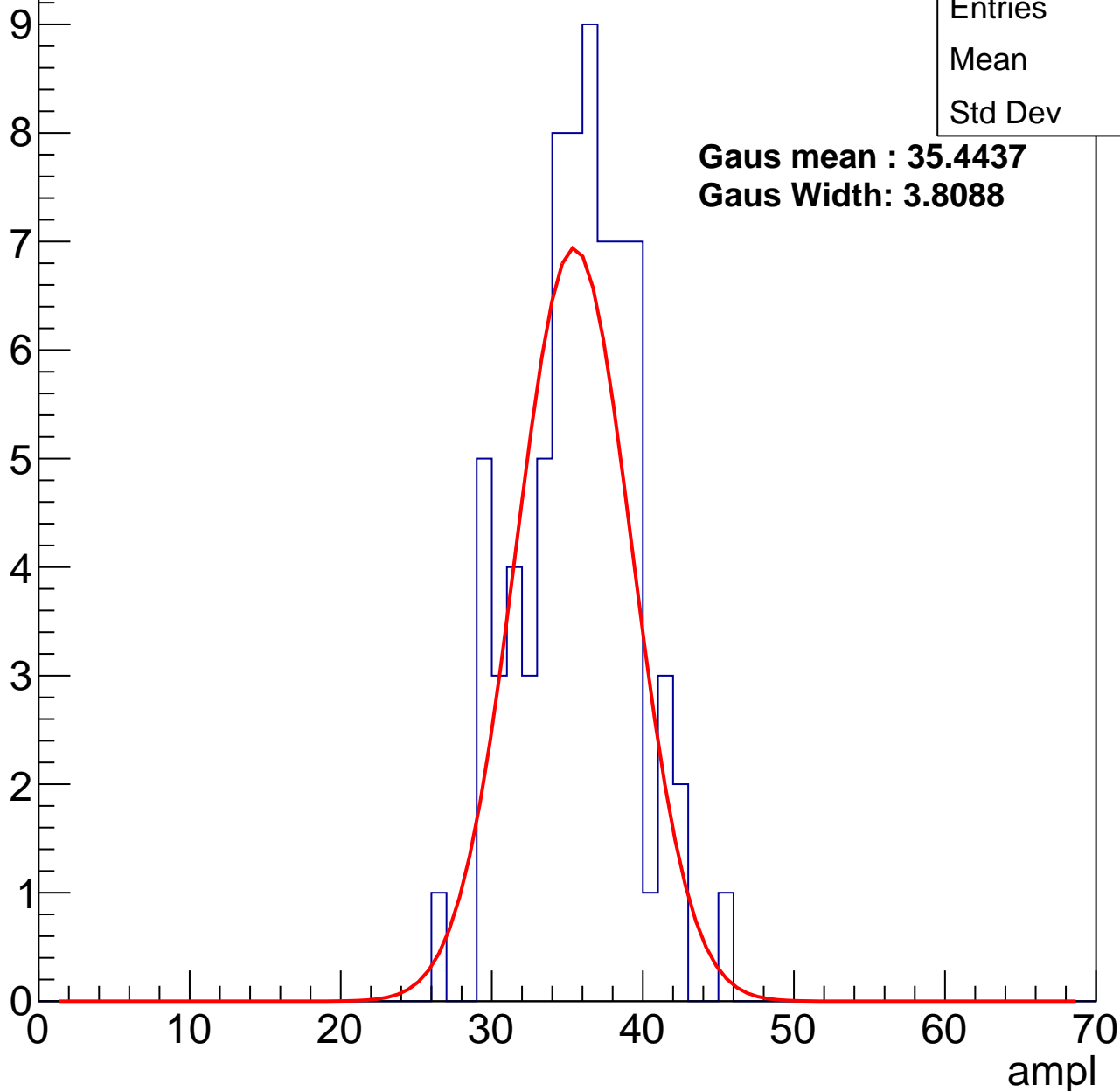
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	35.3
Std Dev	3.66

**Gaus mean : 35.4437**

**Gaus Width: 3.8088**



# B1L102S, U5-ch82, adc2

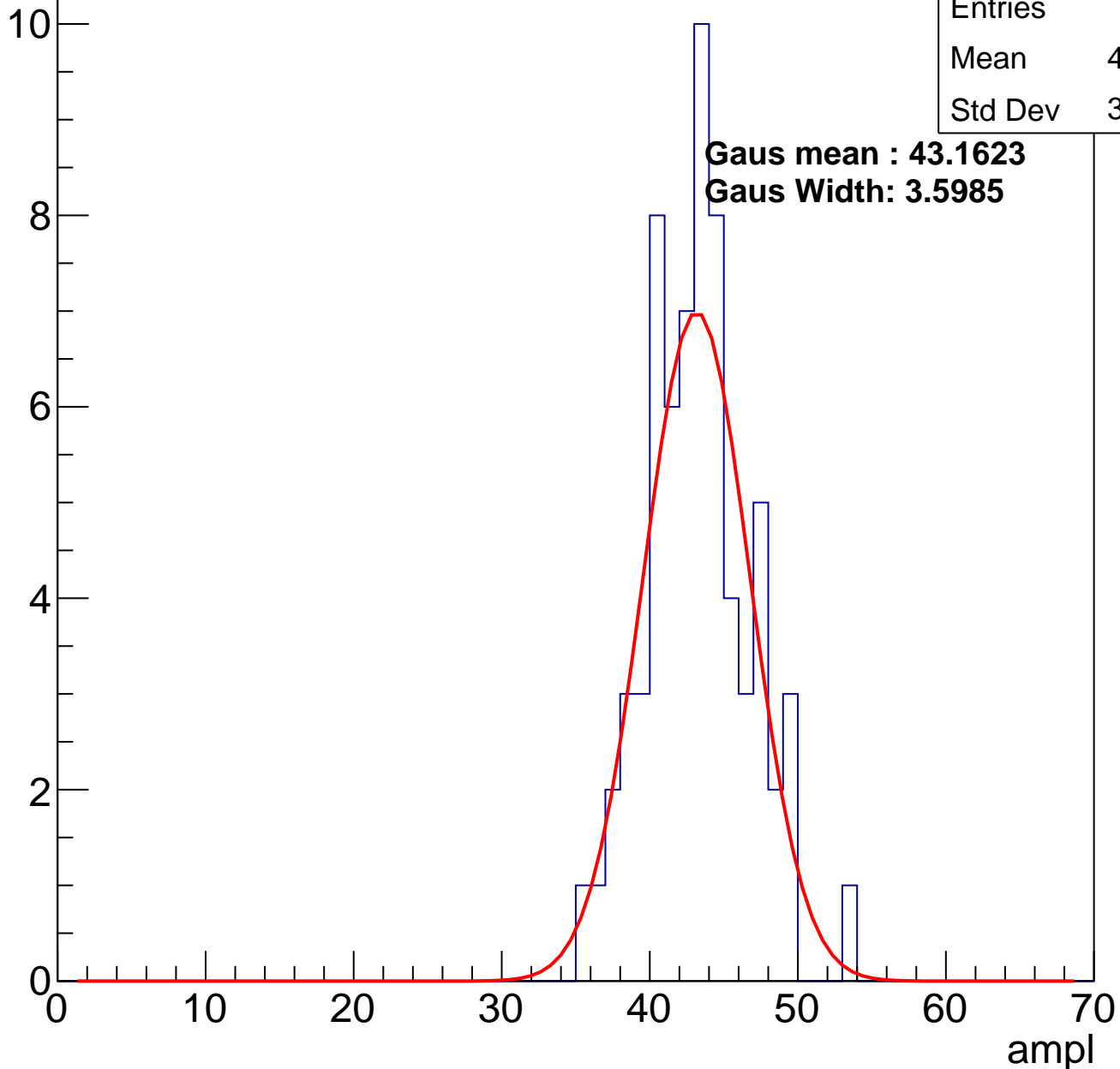
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	67
Mean	42.79
Std Dev	3.449

**Gaus mean : 43.1623**

**Gaus Width: 3.5985**

Entry

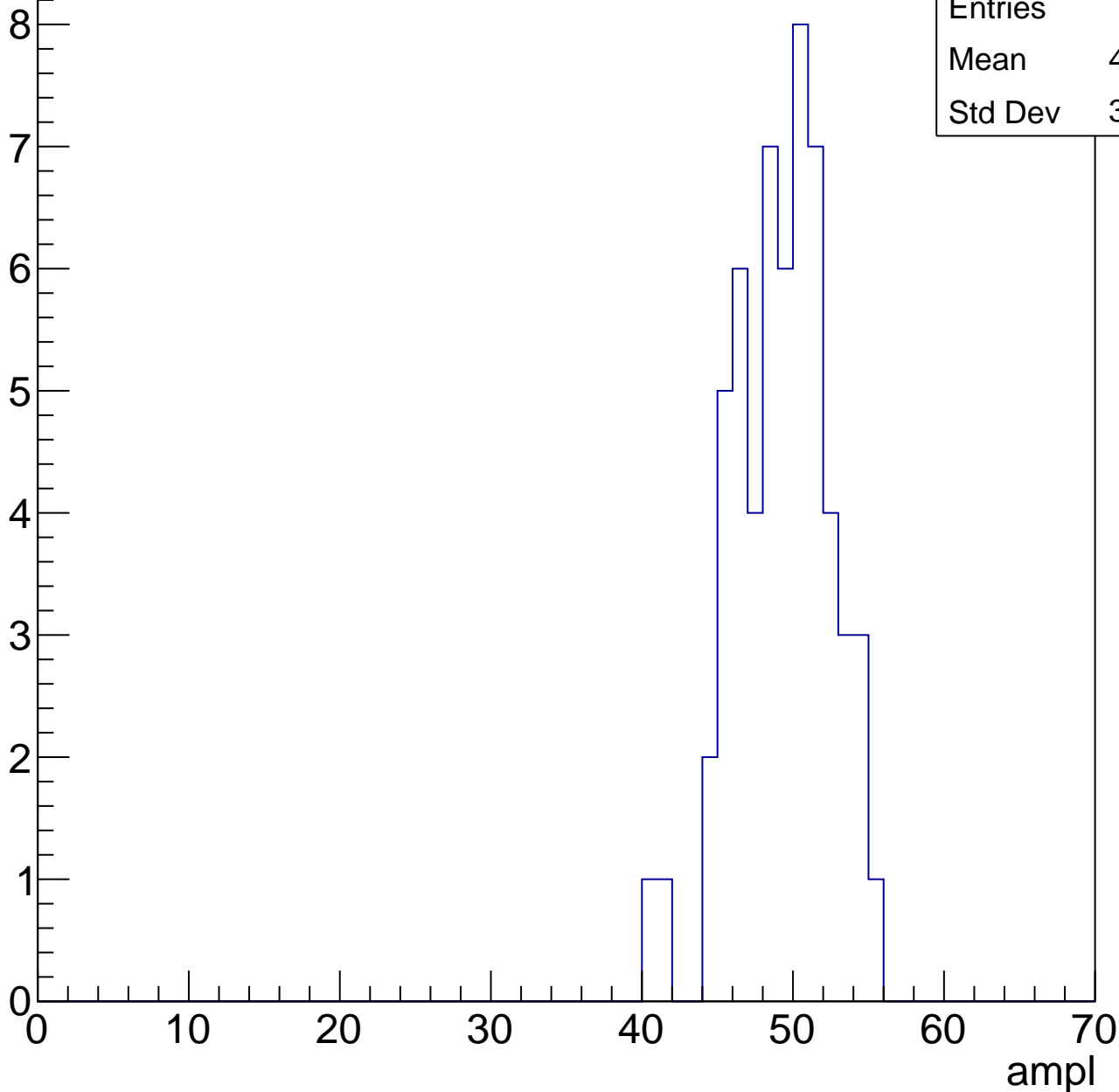


# B1L102S, U5-ch82, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

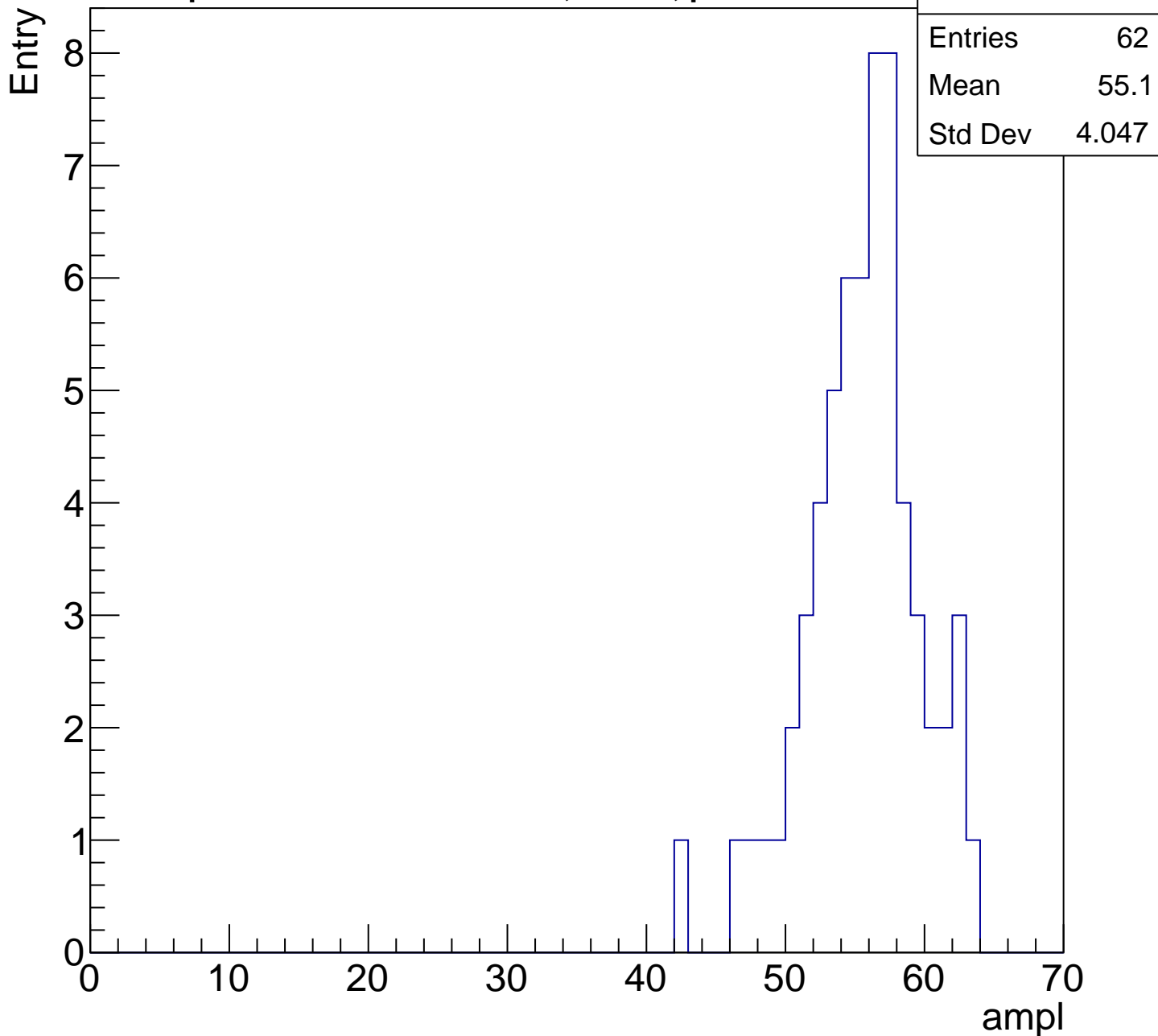
Entry

Entries	58
Mean	48.78
Std Dev	3.163



# B1L102S, U5-ch82, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

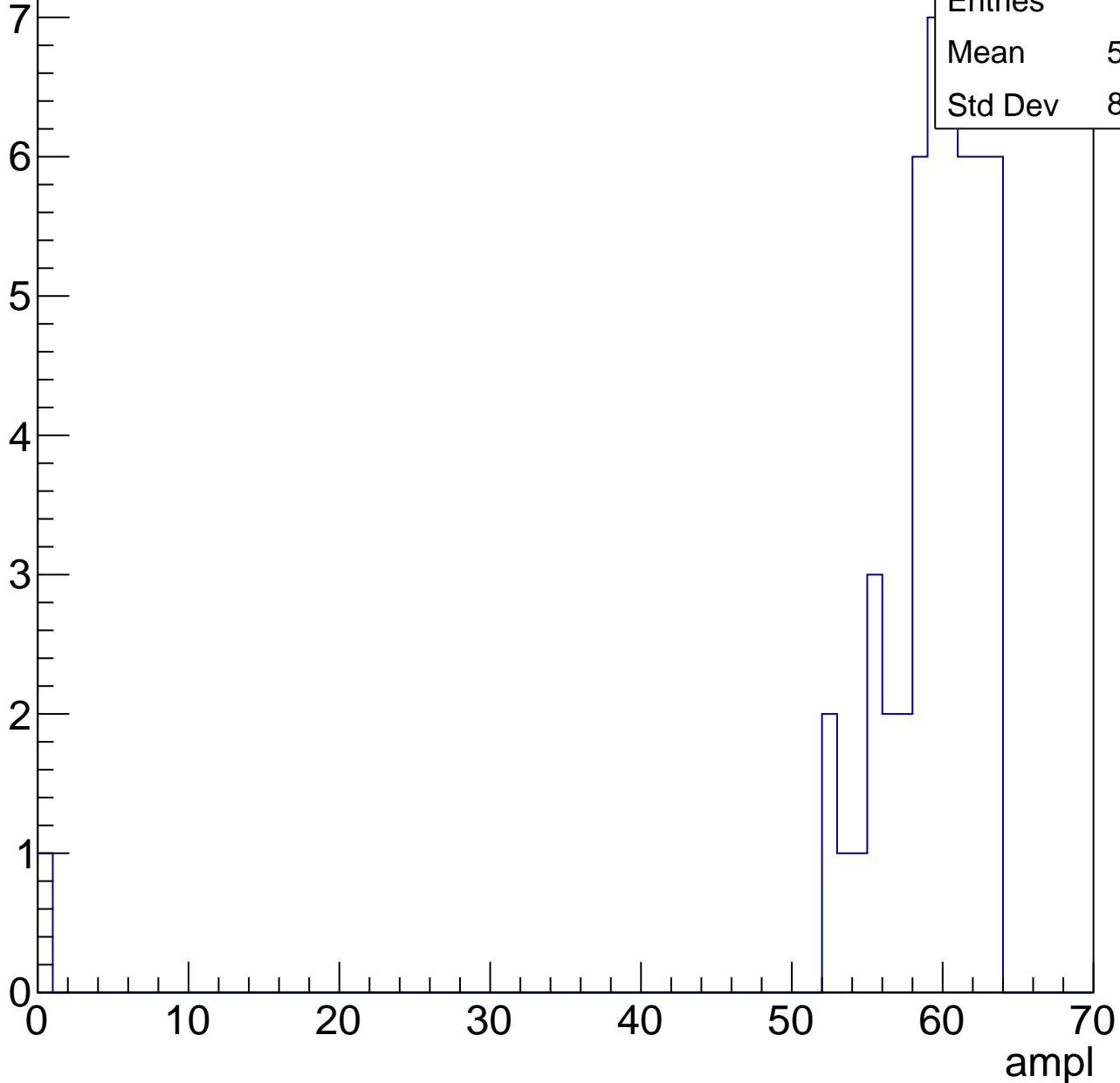


# B1L102S, U5-ch82, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	57.98
Std Dev	8.774



# B1L102S, U5-ch82, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	7
Mean	61.86
Std Dev	1.125



# B1L102S, U5-ch82, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L102S, U5-ch83, adc0

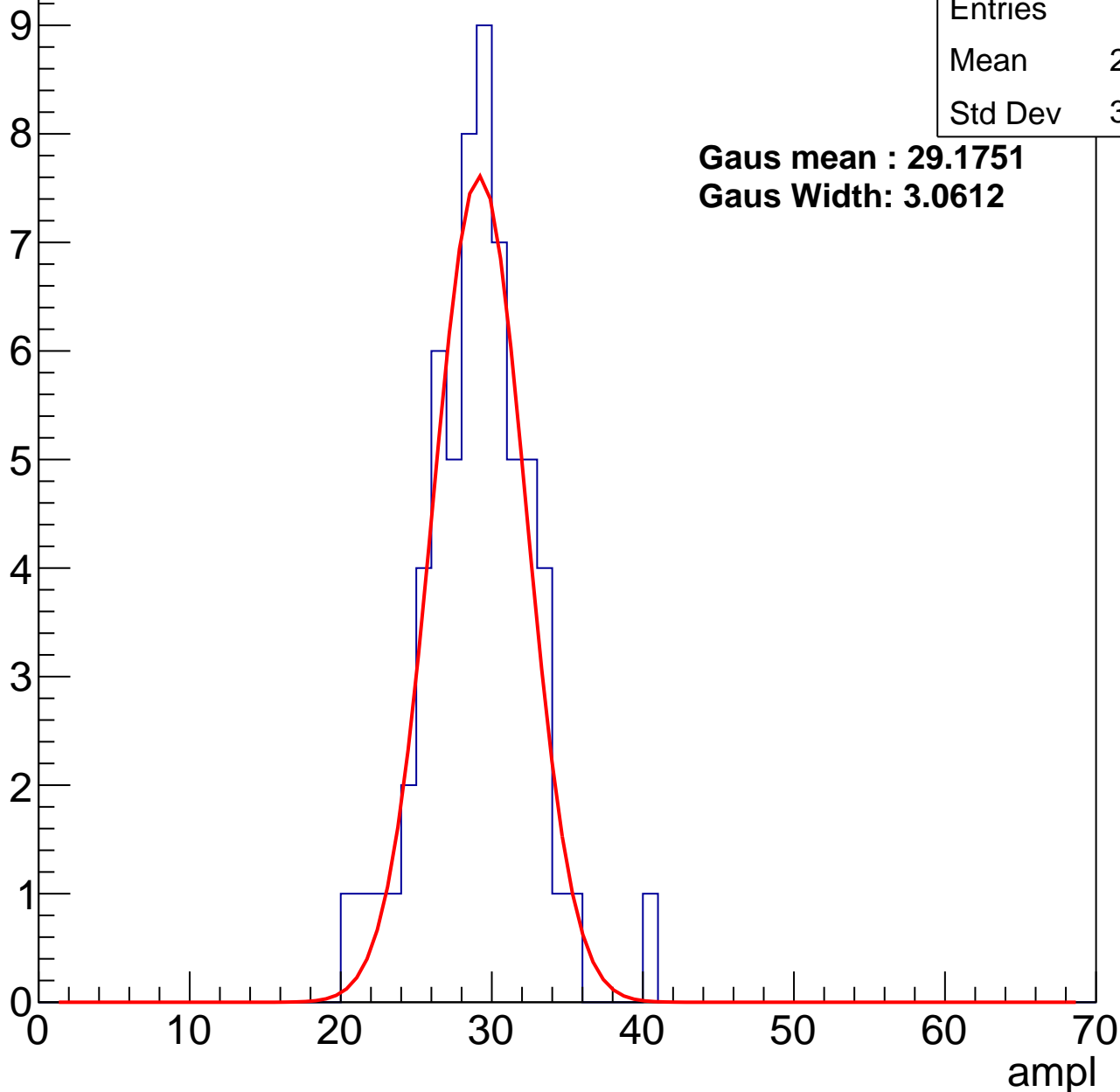
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	28.65
Std Dev	3.446

**Gaus mean : 29.1751**

**Gaus Width: 3.0612**



# B1L102S, U5-ch83, adc1

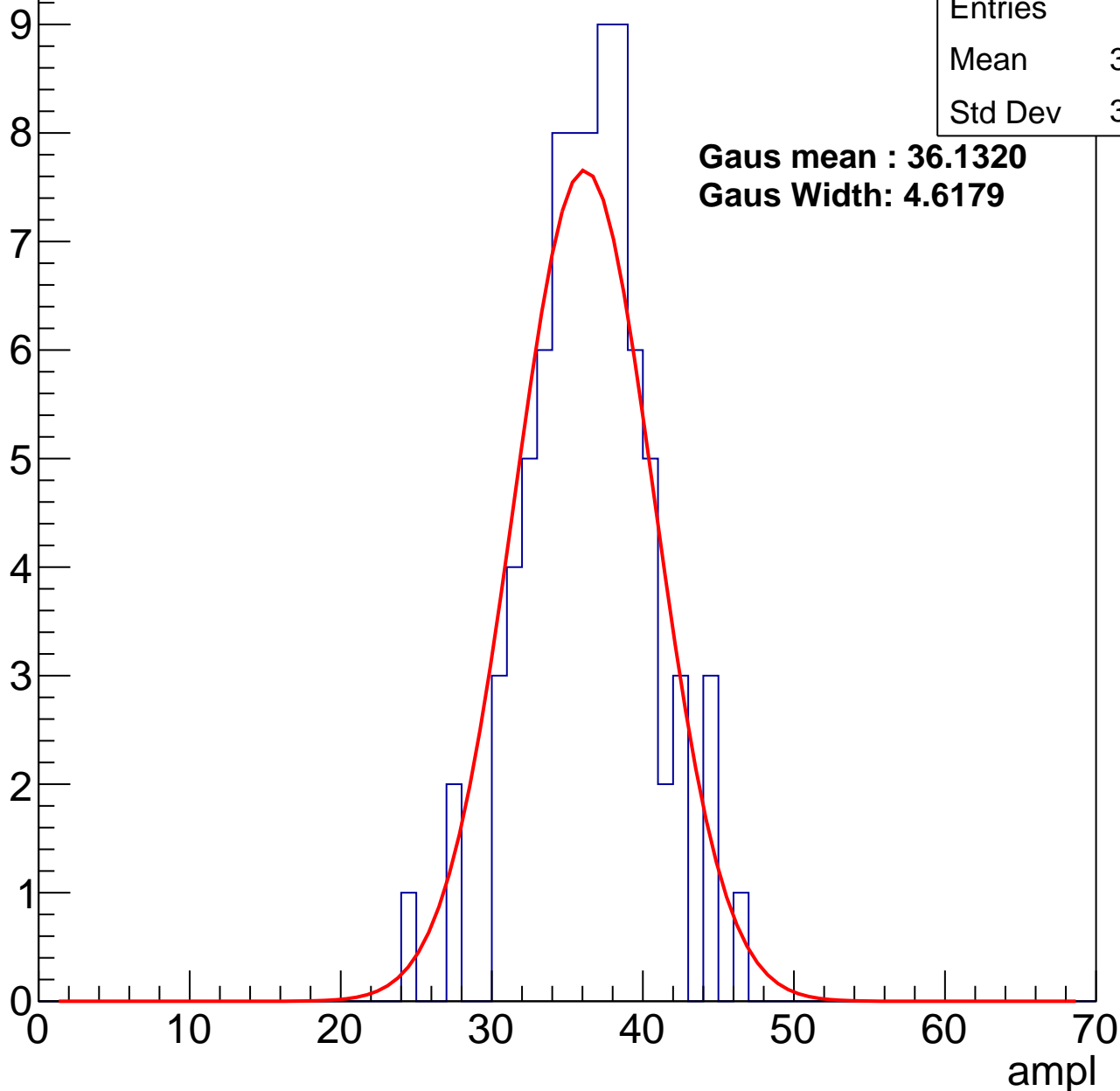
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	83
Mean	35.96
Std Dev	3.983

**Gaus mean : 36.1320**

**Gaus Width: 4.6179**



# B1L102S, U5-ch83, adc2

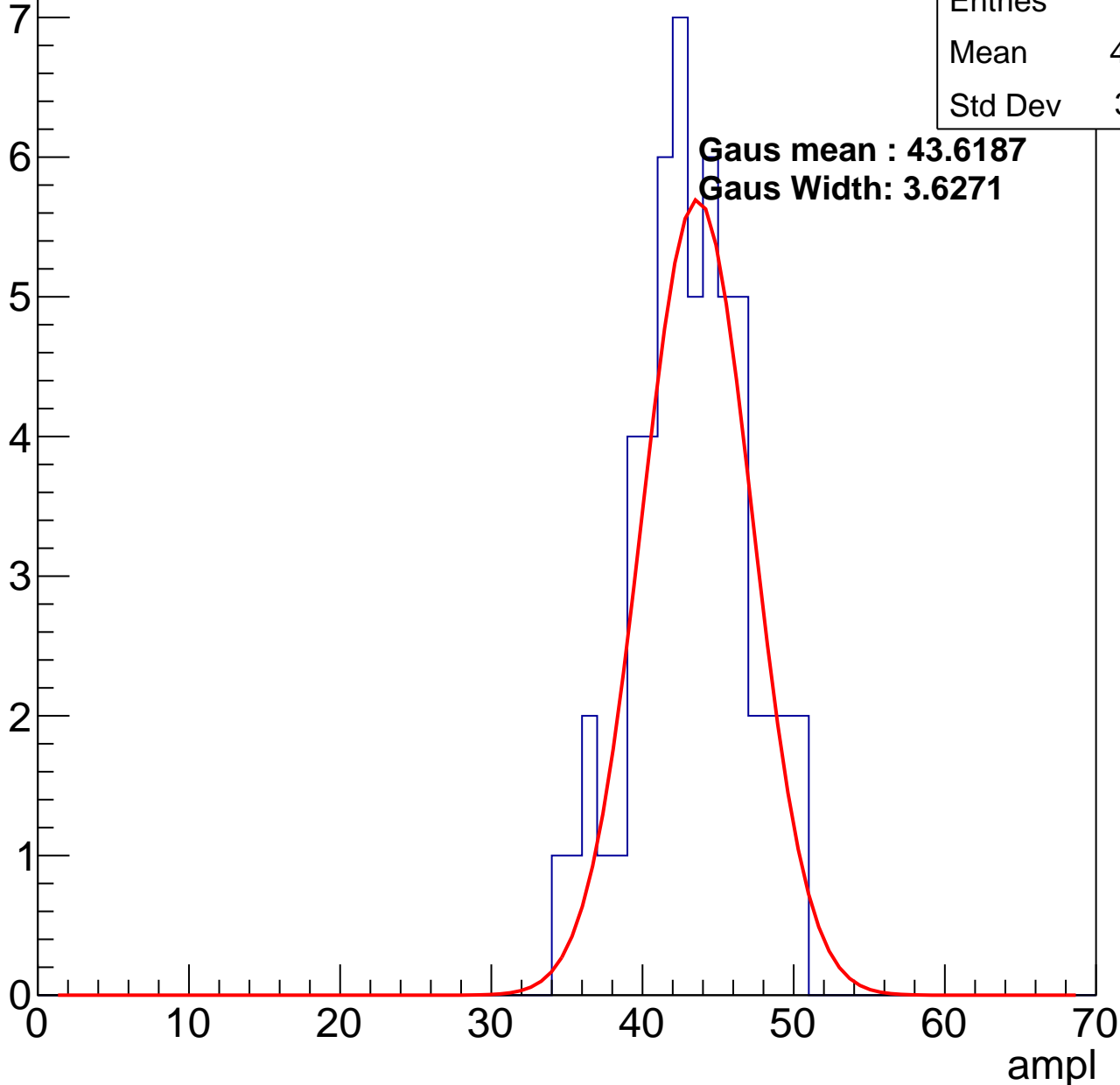
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	42.75
Std Dev	3.671

**Gaus mean : 43.6187**

**Gaus Width: 3.6271**

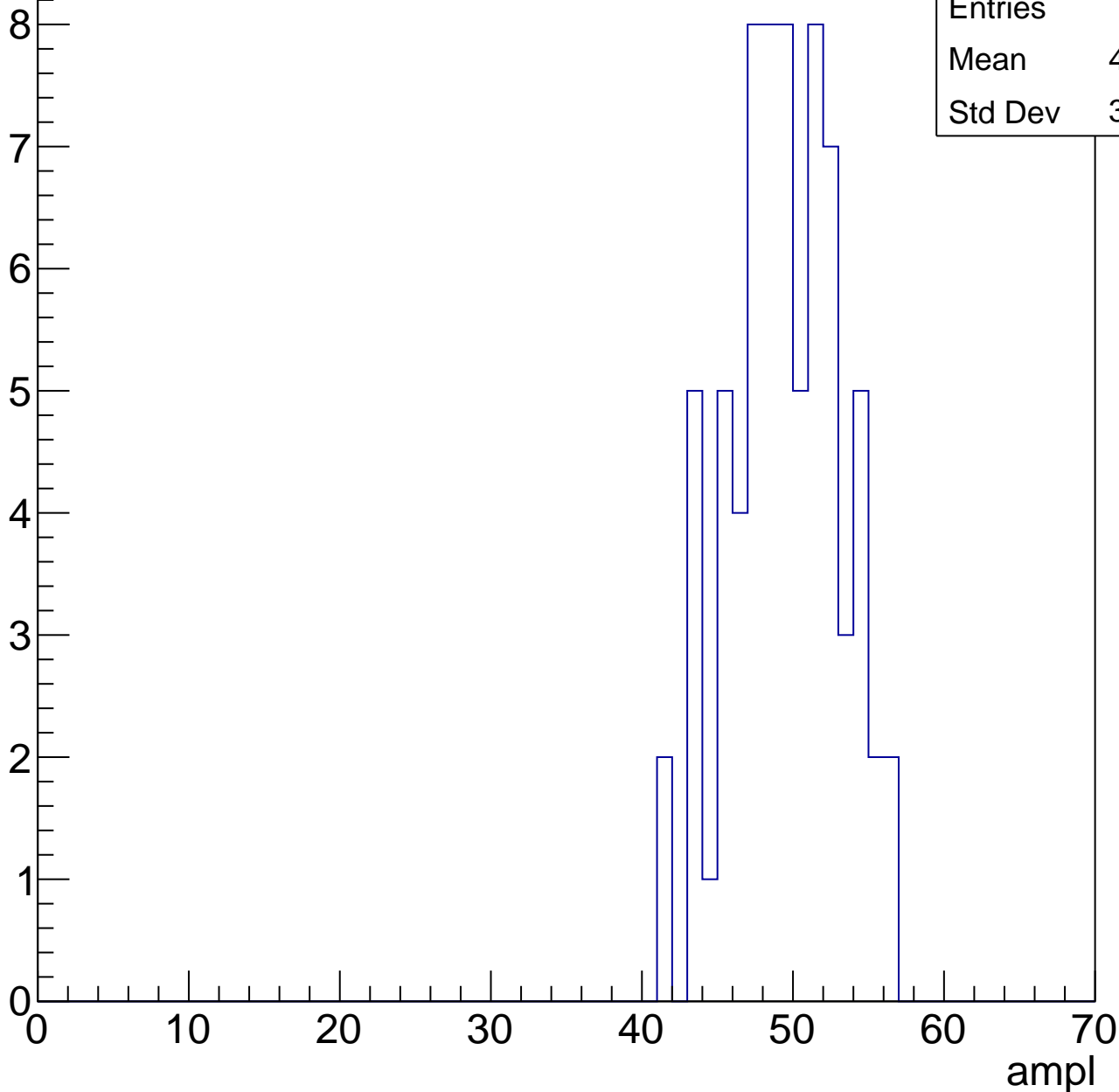


# B1L102S, U5-ch83, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	48.97
Std Dev	3.573



# B1L102S, U5-ch83, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

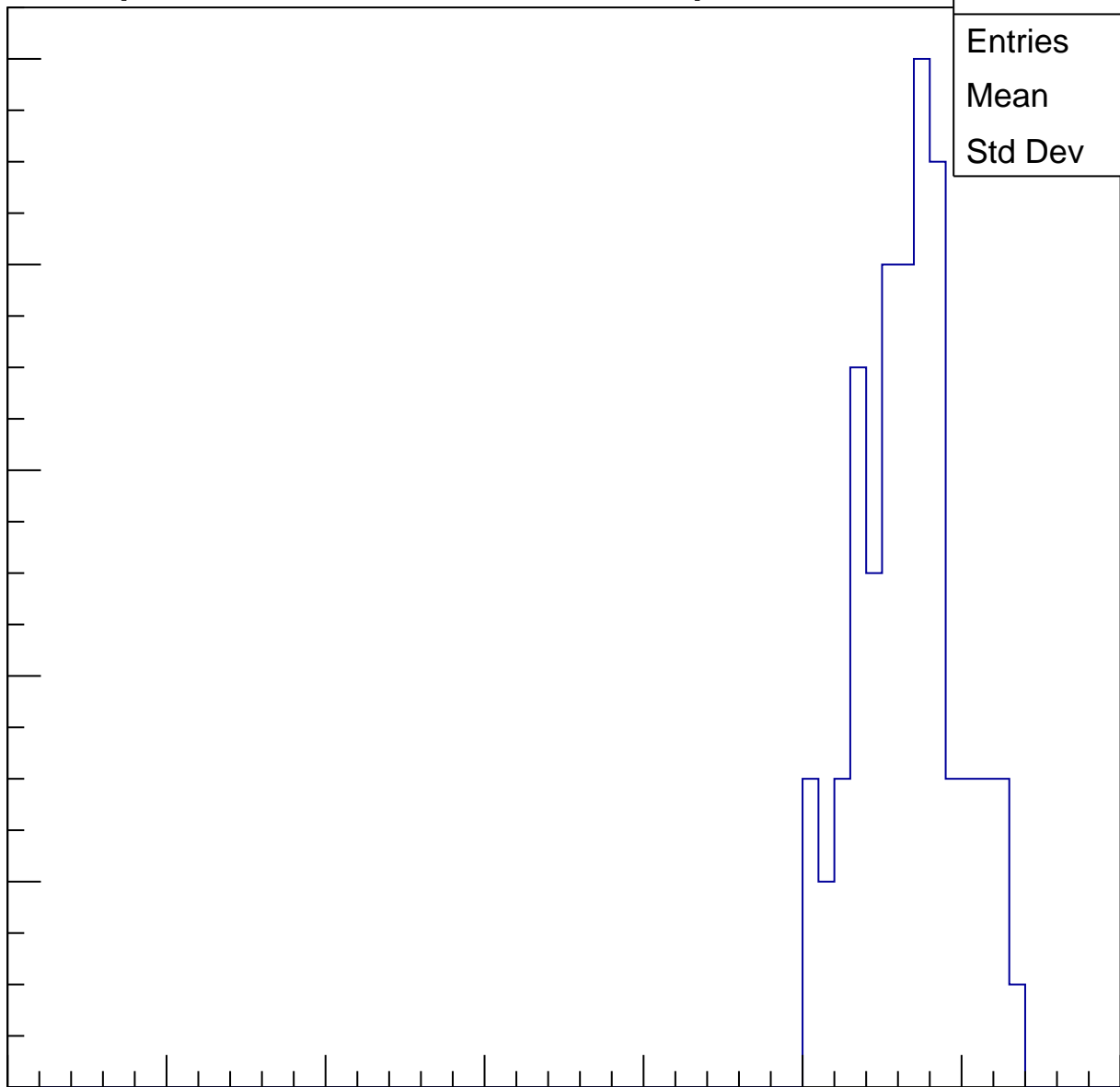
Entries	68
Mean	56.15
Std Dev	3.088

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

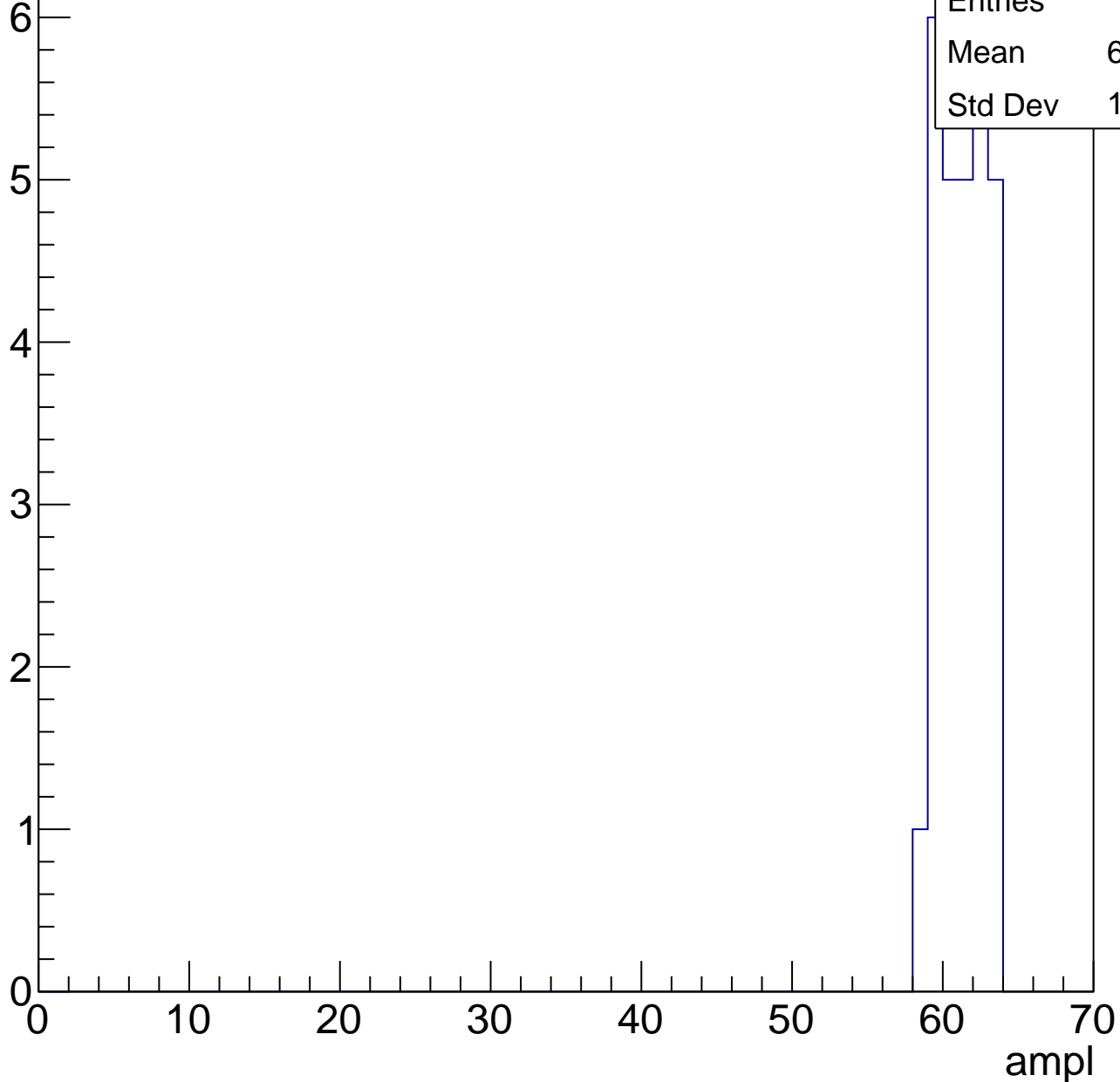
ampl



# B1L102S, U5-ch83, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

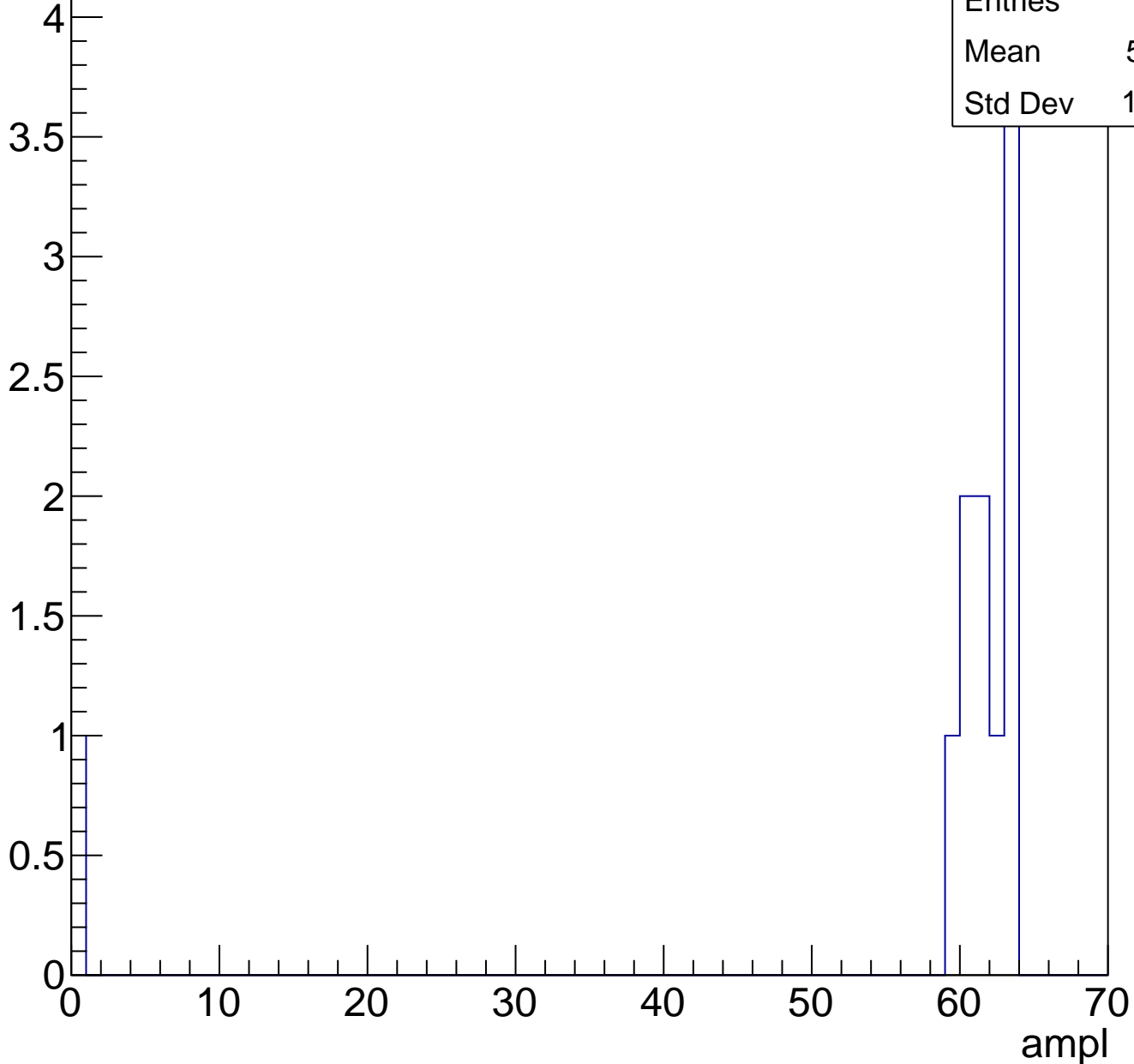
Entry



# B1L102S, U5-ch83, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	11
Mean	55.91
Std Dev	17.73



# B1L102S, U5-ch83, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U5-ch84, adc0

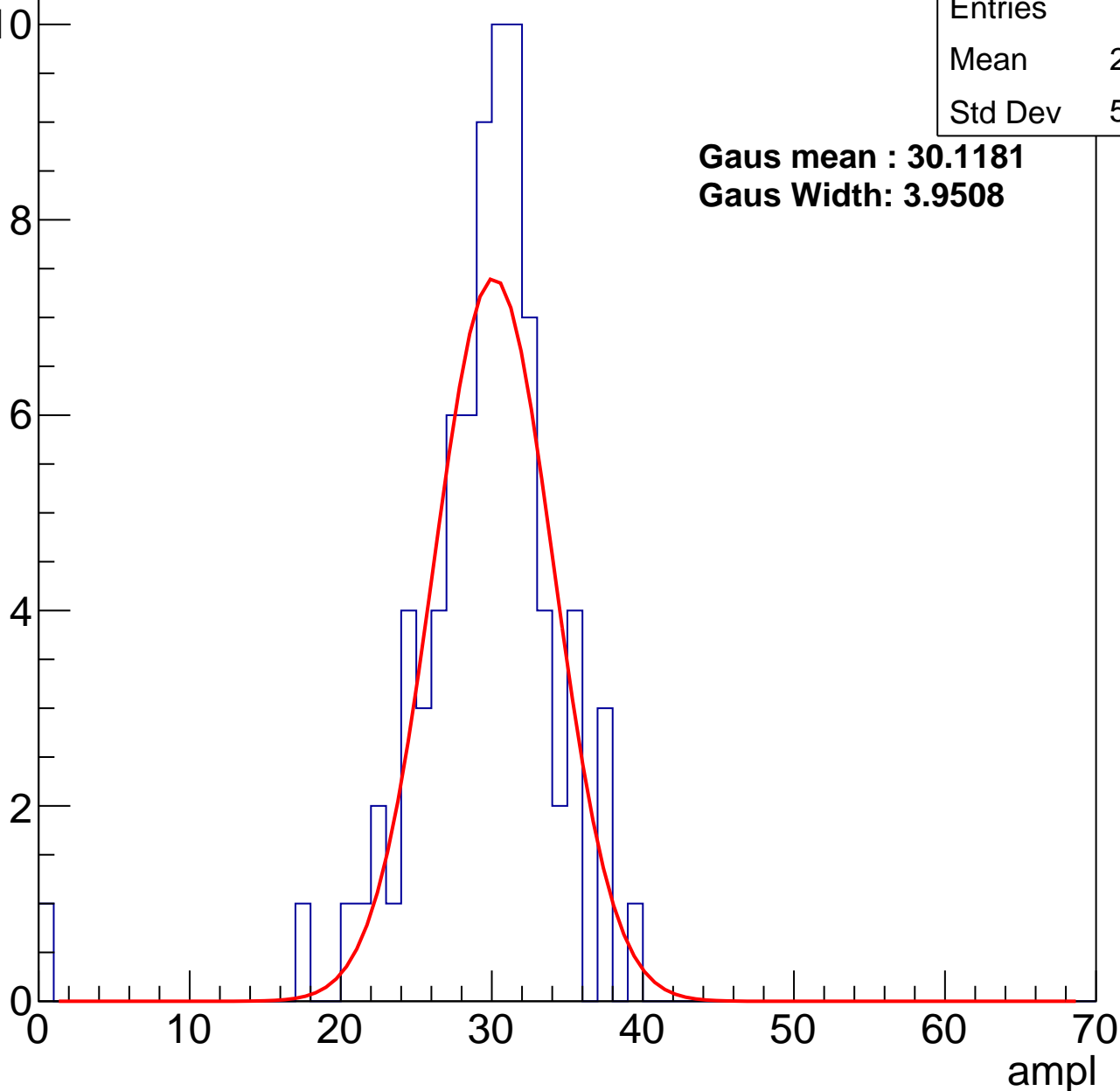
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	80
Mean	28.94
Std Dev	5.173

**Gaus mean : 30.1181**

**Gaus Width: 3.9508**



# B1L102S, U5-ch84, adc1

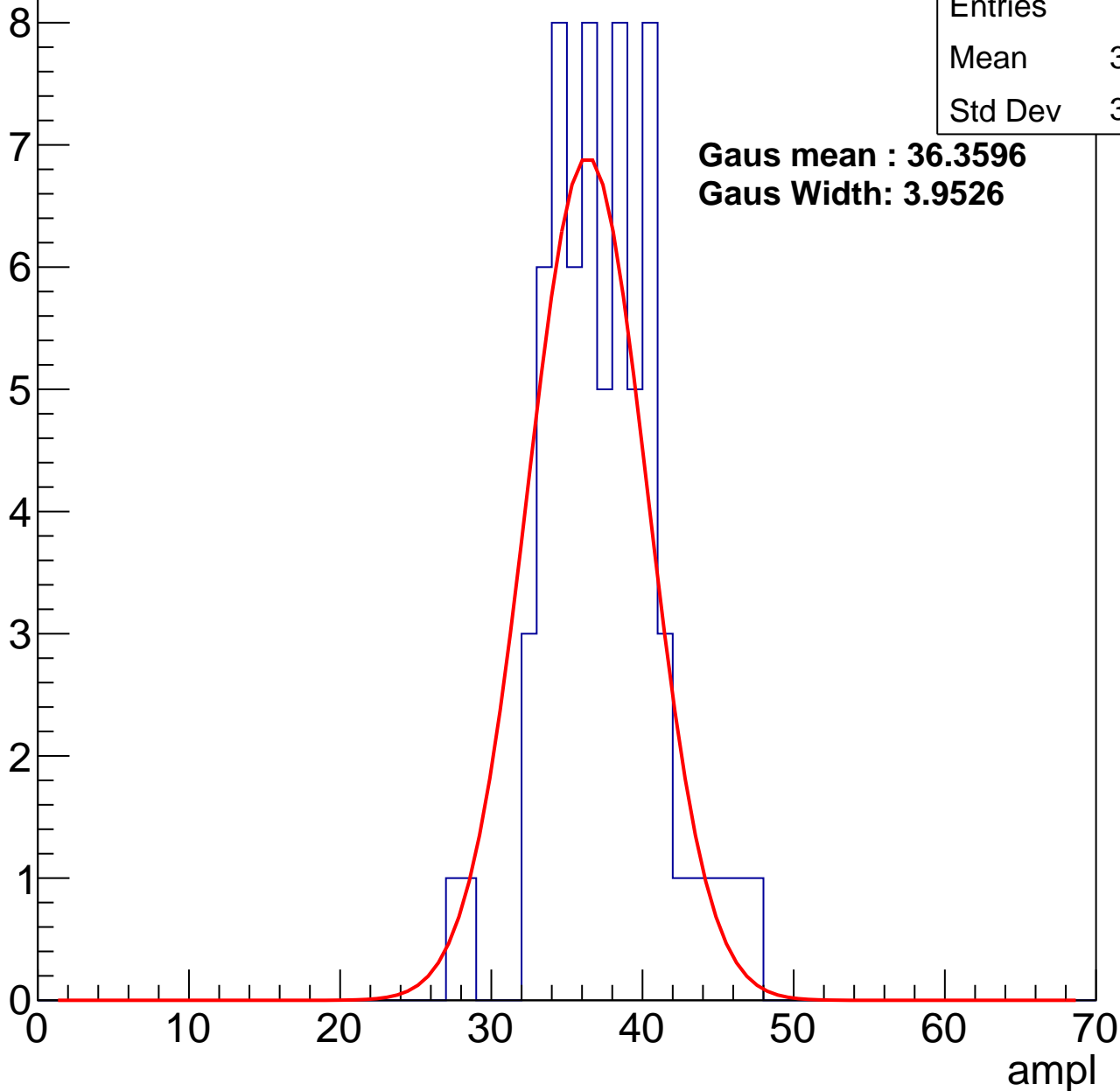
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	36.96
Std Dev	3.755

**Gaus mean : 36.3596**

**Gaus Width: 3.9526**



# B1L102S, U5-ch84, adc2

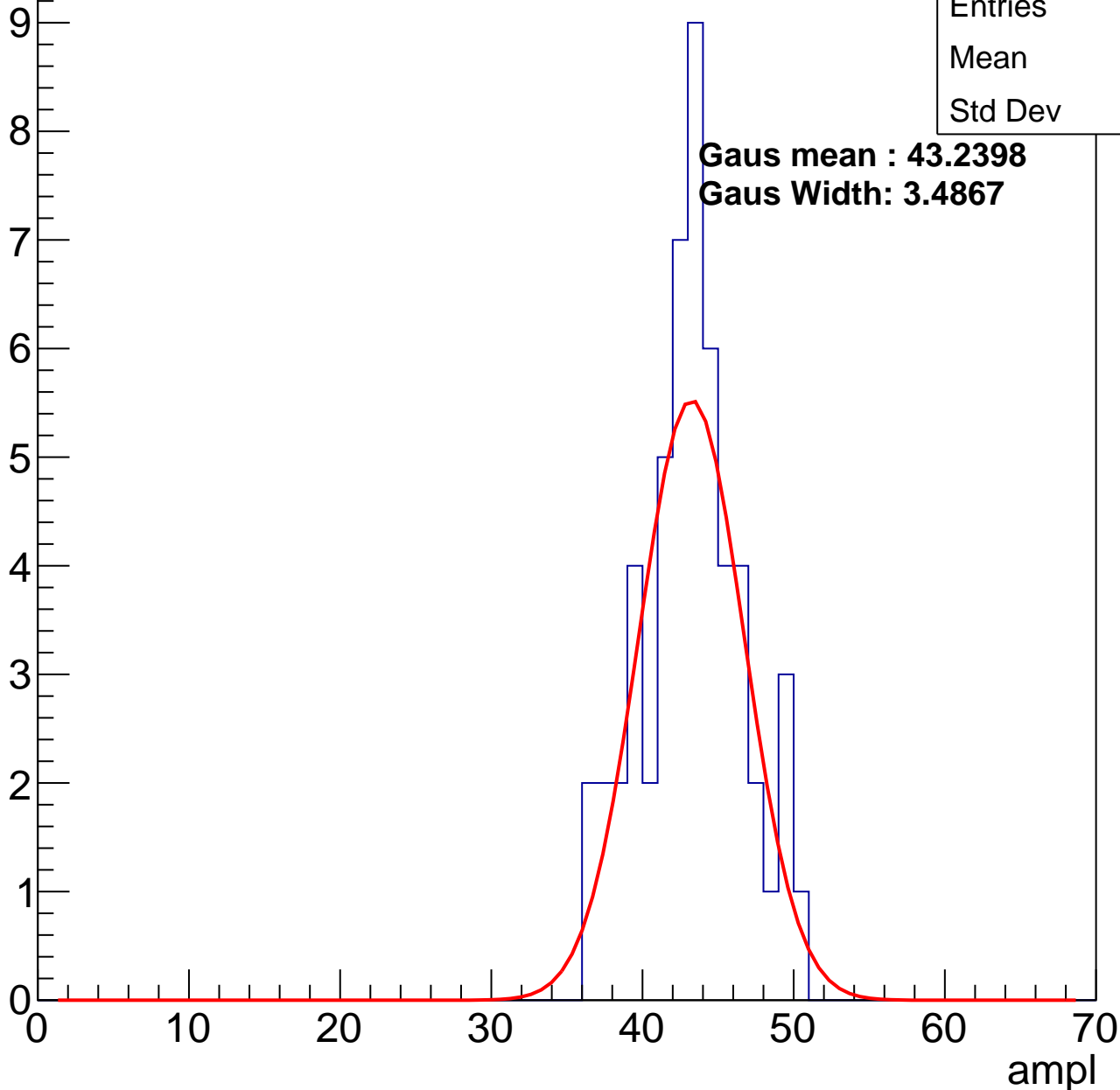
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	42.8
Std Dev	3.33

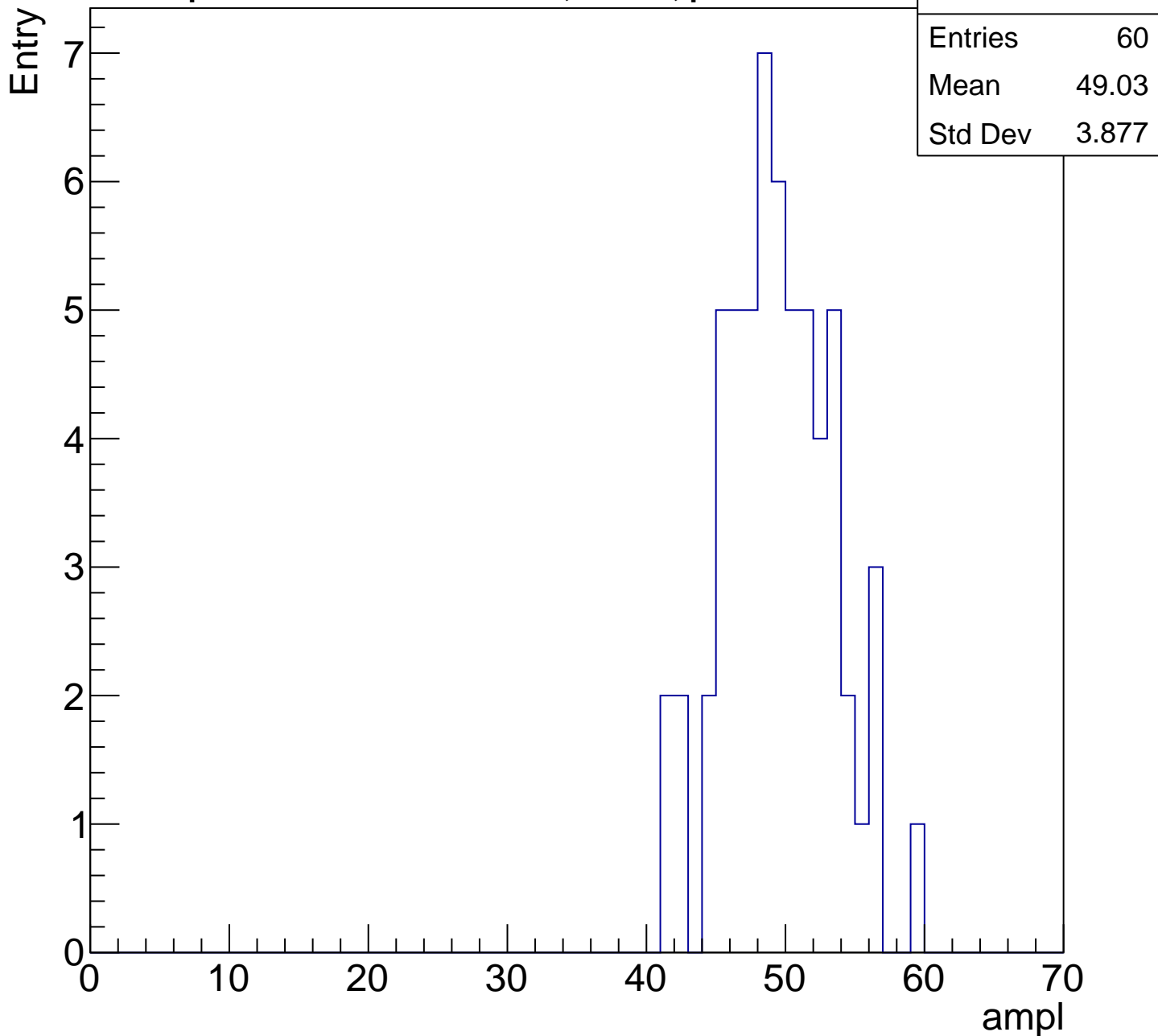
**Gaus mean : 43.2398**

**Gaus Width: 3.4867**



# B1L102S, U5-ch84, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

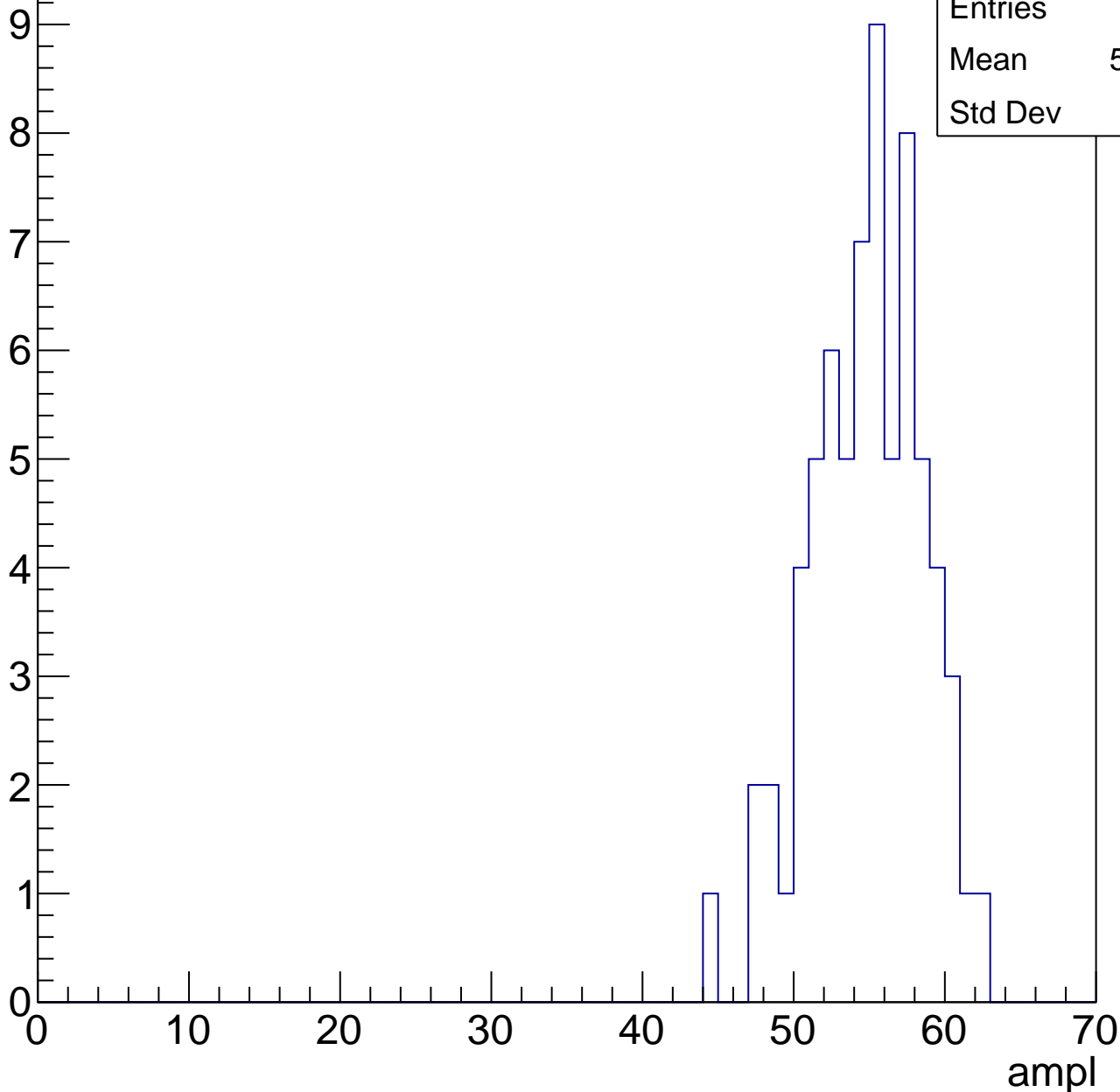


# B1L102S, U5-ch84, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	54.39
Std Dev	3.66

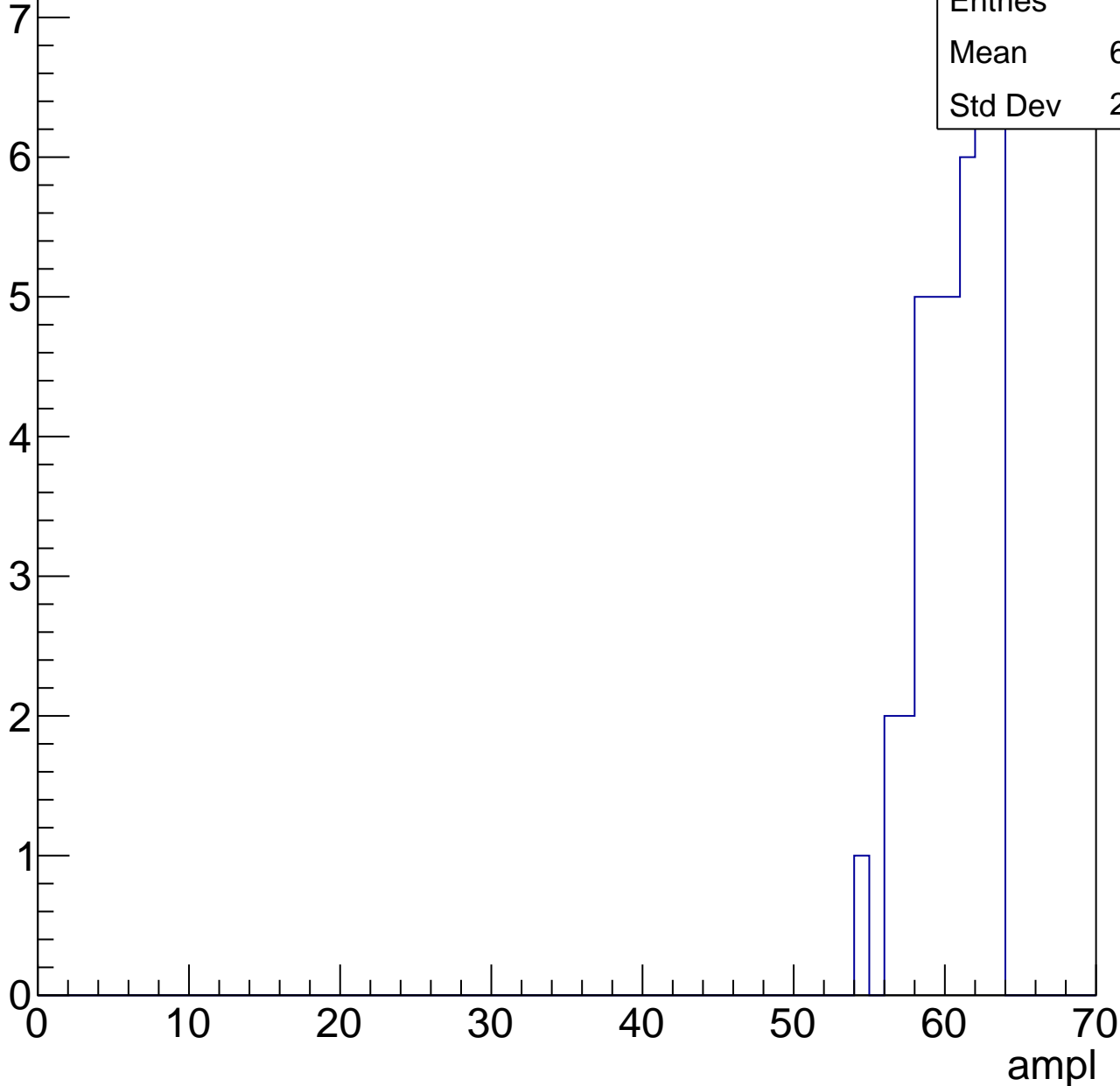


# B1L102S, U5-ch84, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

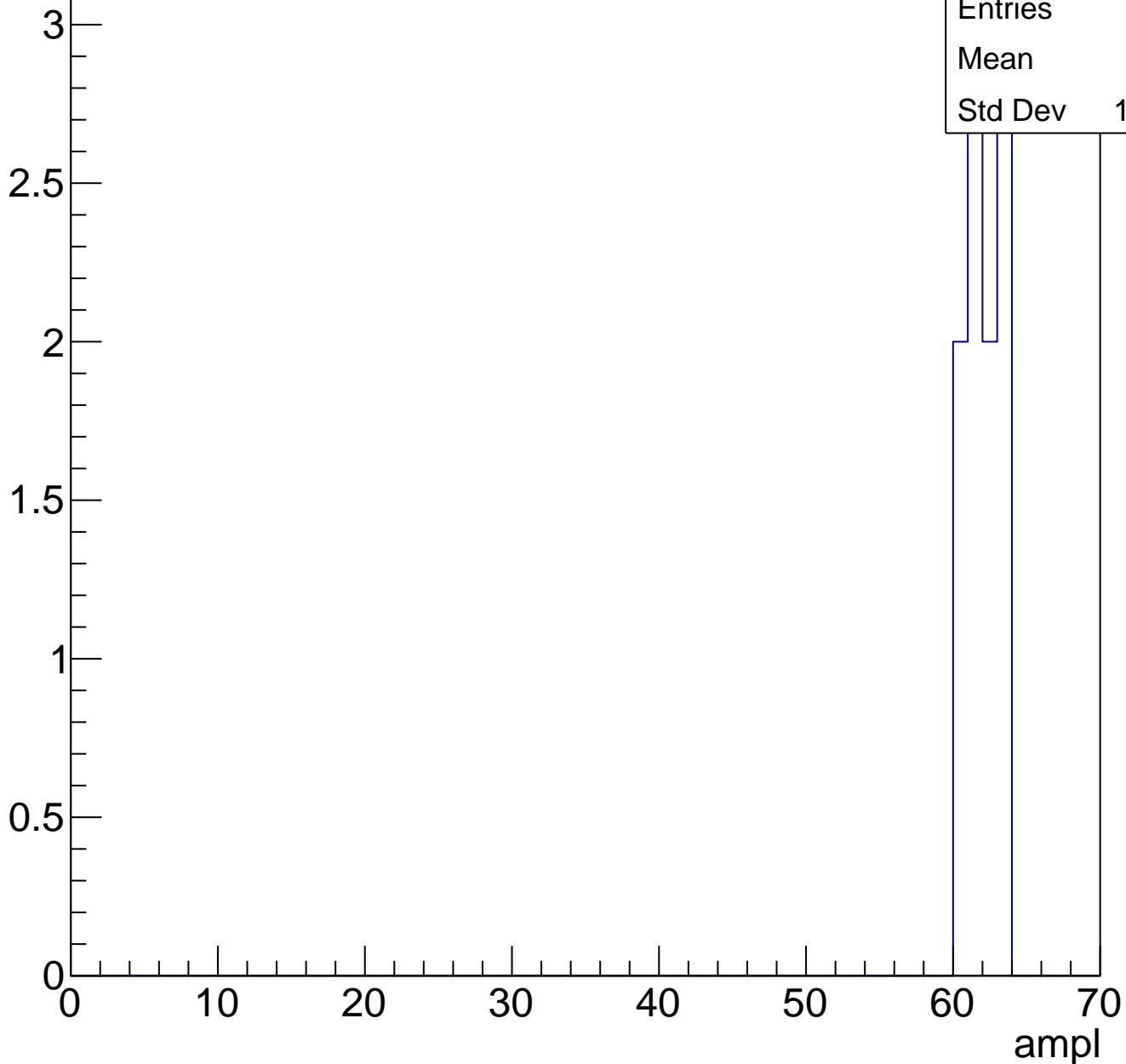
Entries	40
Mean	60.15
Std Dev	2.275



# B1L102S, U5-ch84, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U5-ch84, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U5-ch85, adc0

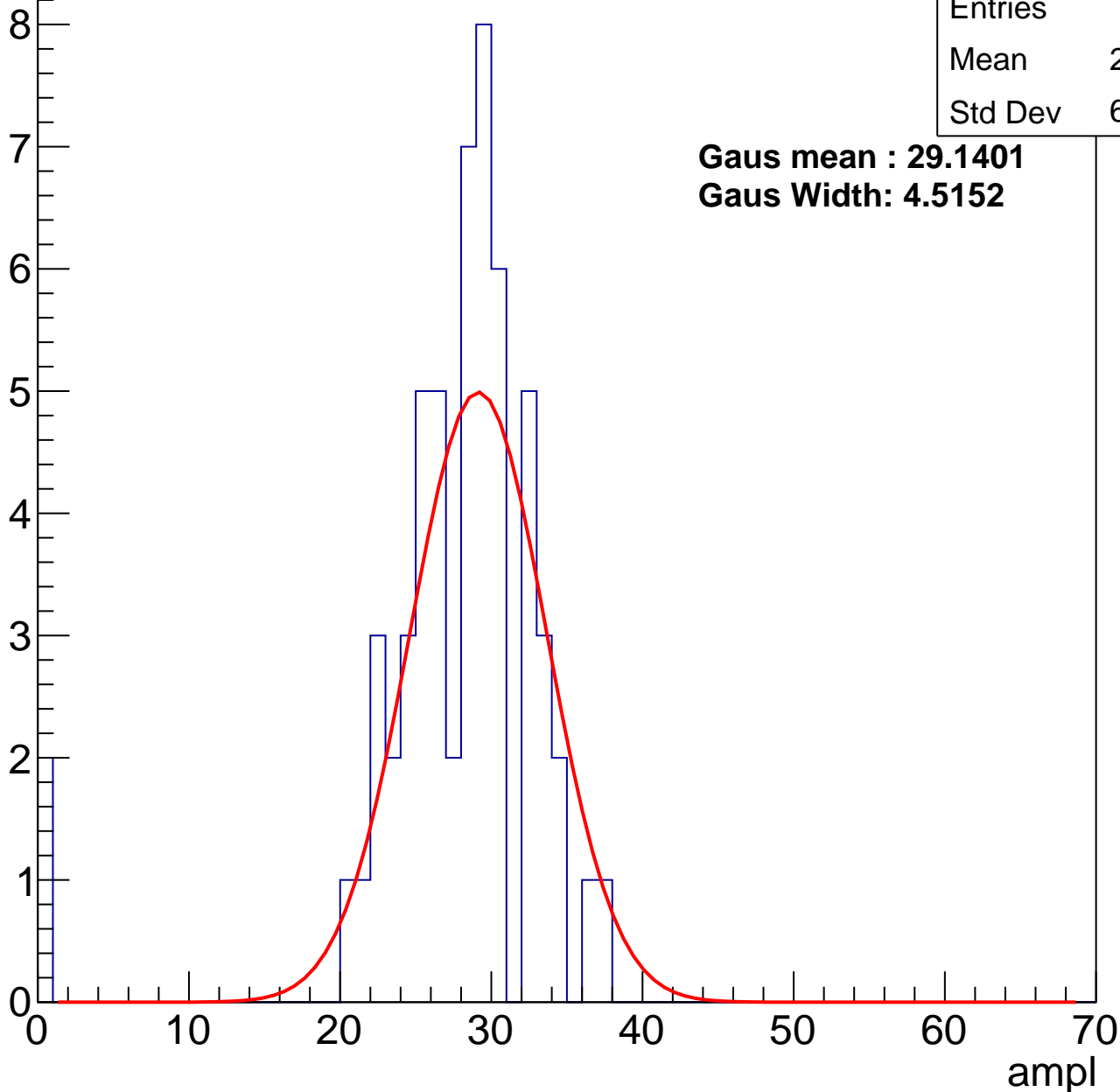
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	27.05
Std Dev	6.362

**Gaus mean : 29.1401**

**Gaus Width: 4.5152**



# B1L102S, U5-ch85, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	87
Mean	35.56
Std Dev	3.947

**Gaus mean : 35.8864**

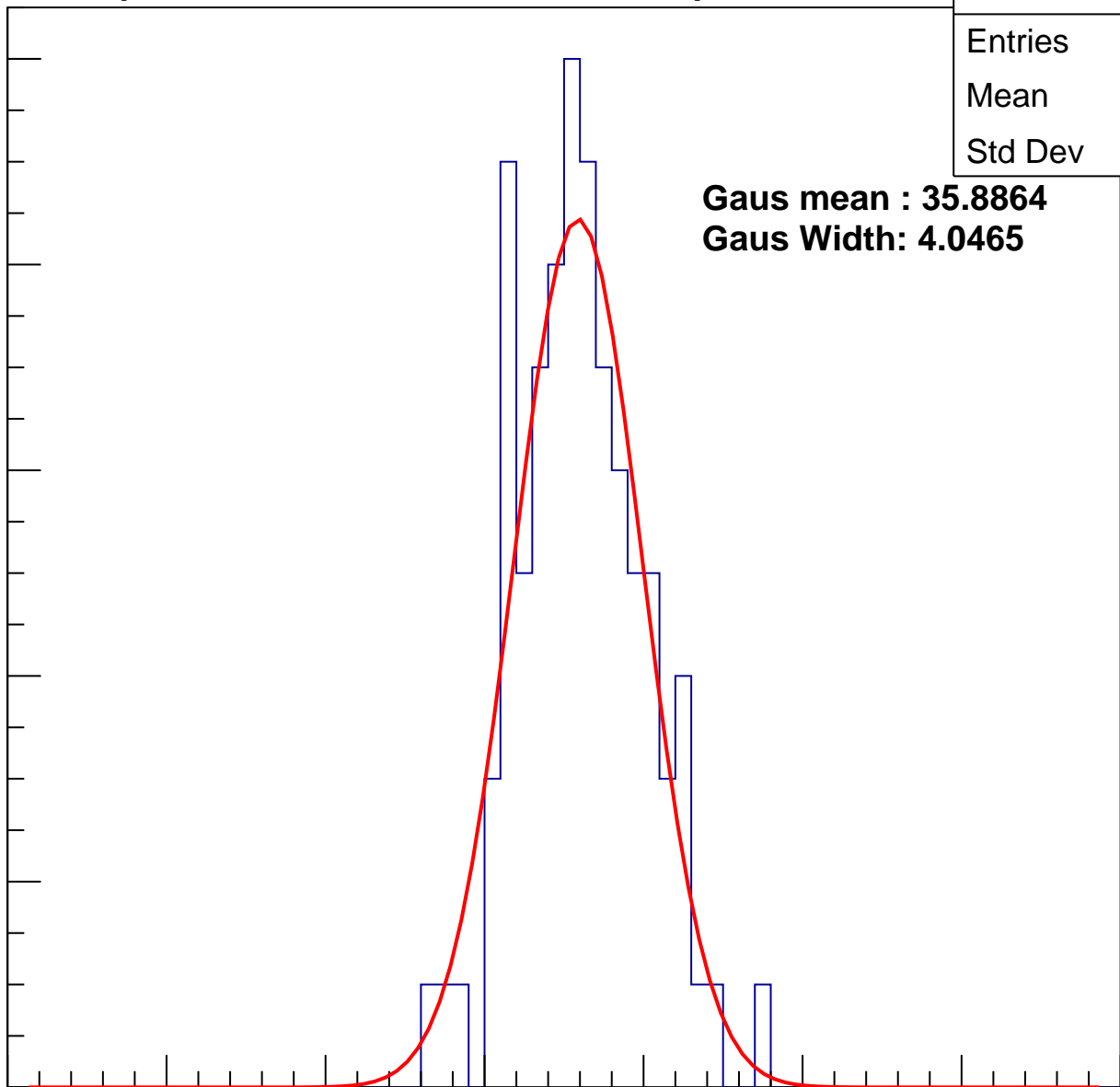
**Gaus Width: 4.0465**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U5-ch85, adc2

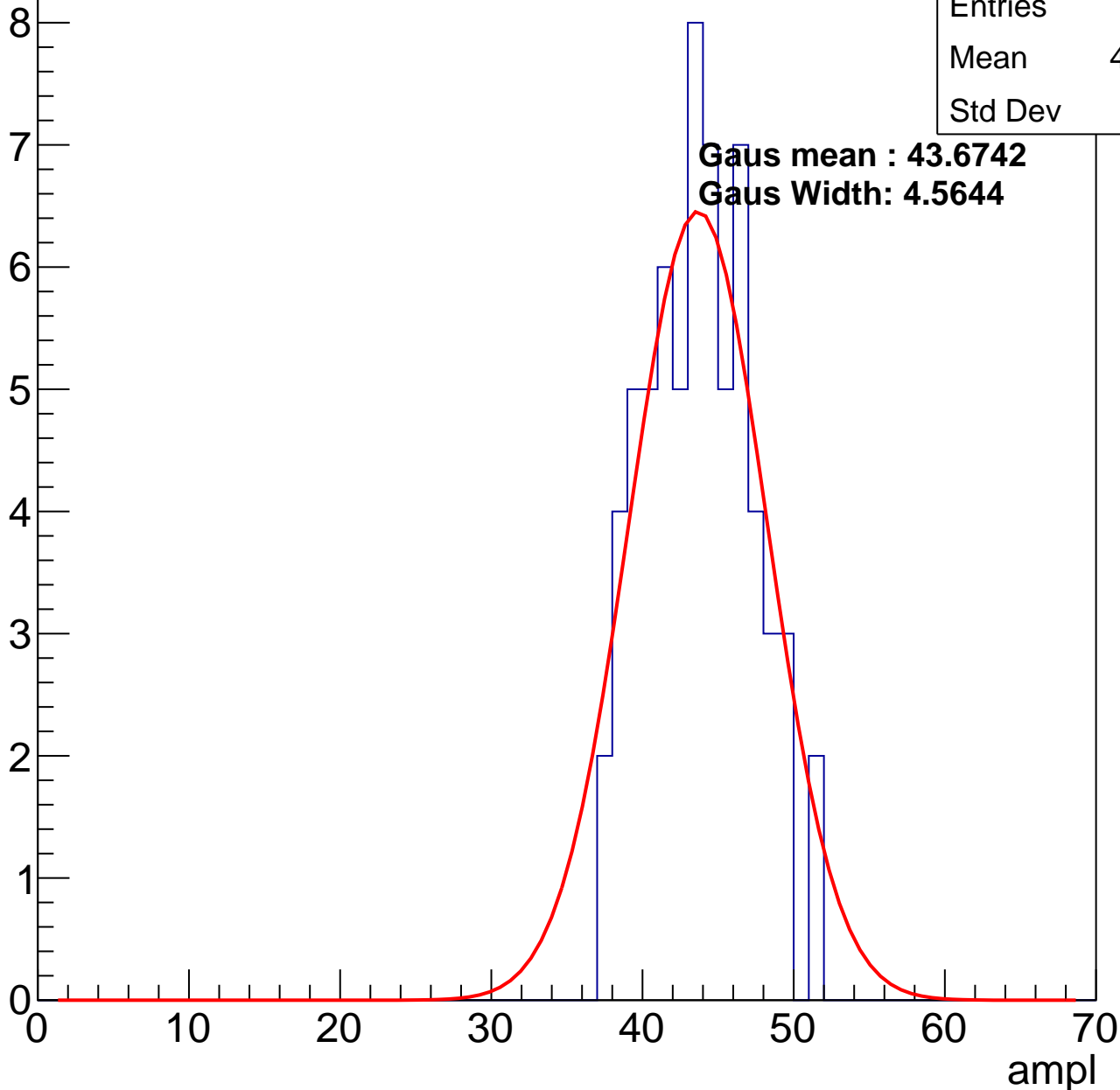
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	43.29
Std Dev	3.45

**Gaus mean : 43.6742**

**Gaus Width: 4.5644**

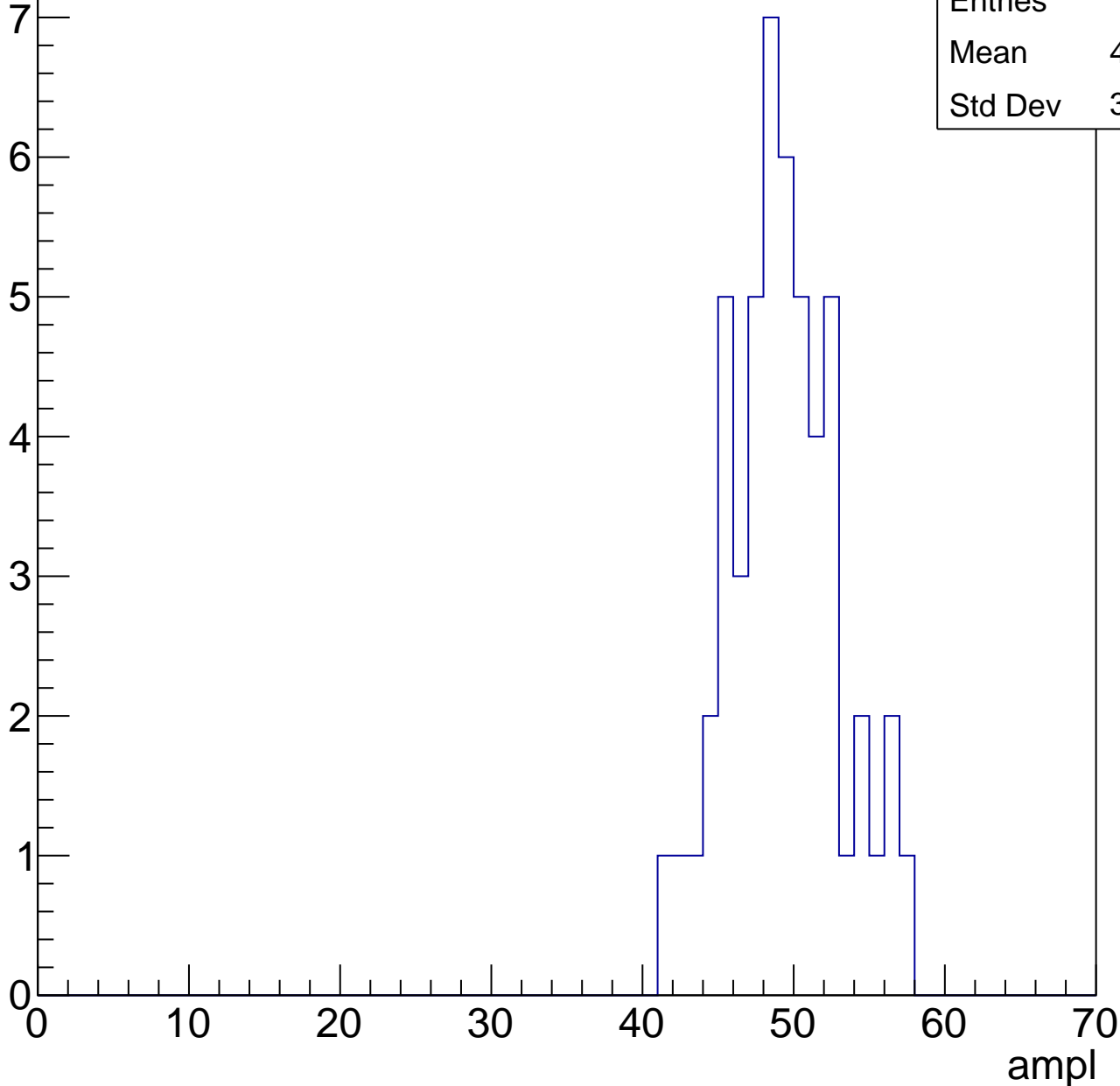


# B1L102S, U5-ch85, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

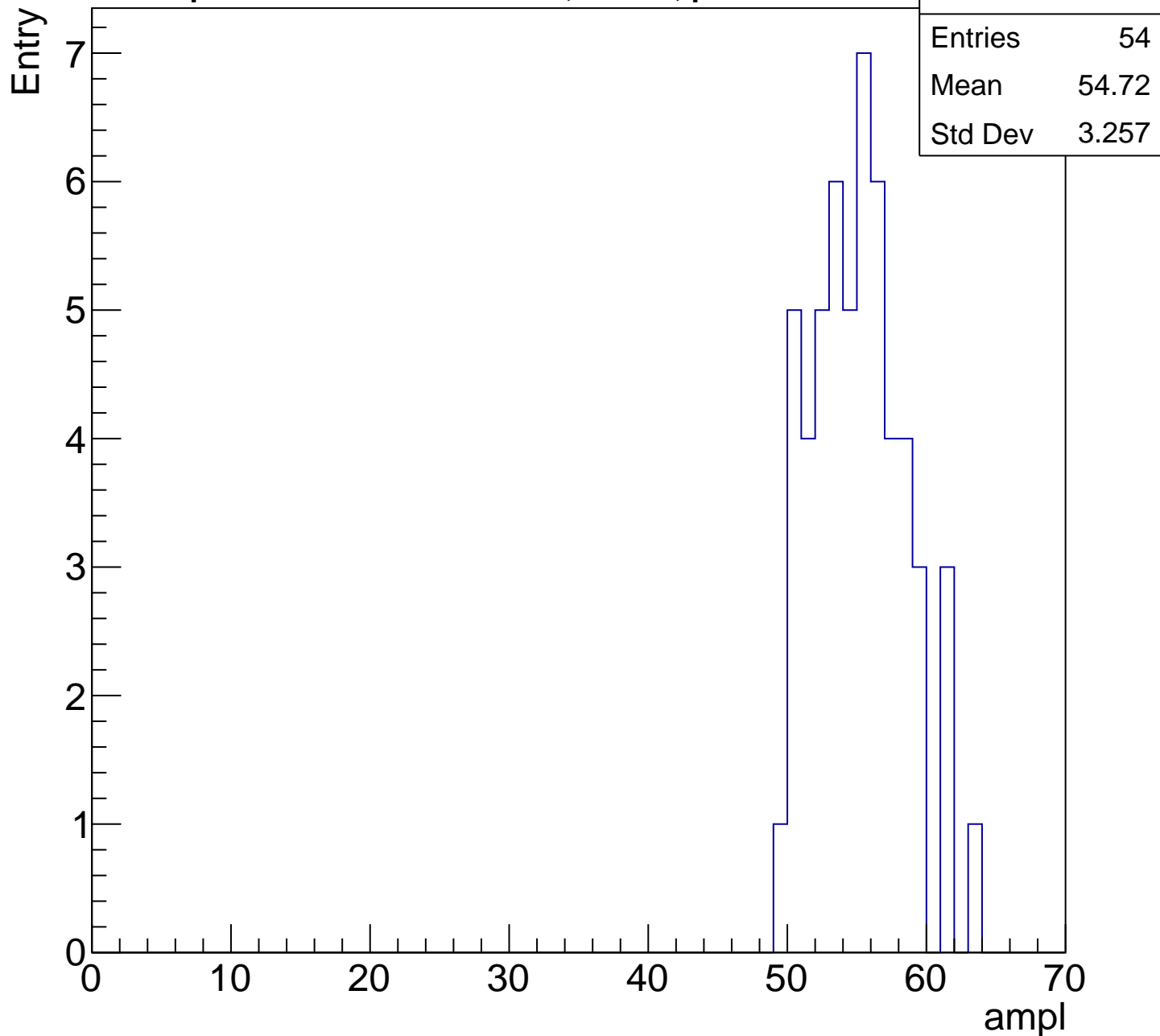
Entry

Entries	52
Mean	48.87
Std Dev	3.568



# B1L102S, U5-ch85, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

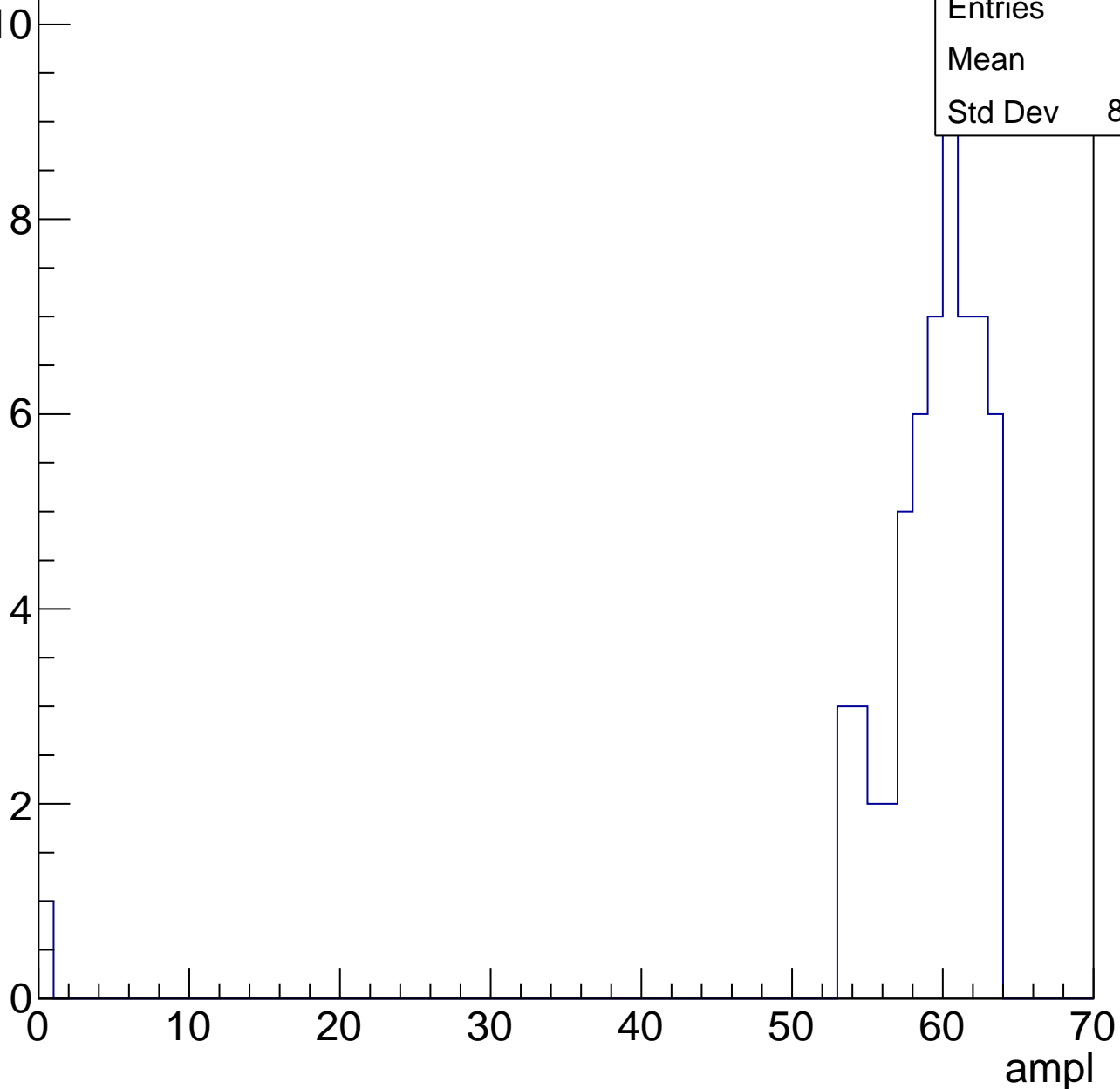


# B1L102S, U5-ch85, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	58.1
Std Dev	8.119



# B1L102S, U5-ch85, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U5-ch85, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U5-ch86, adc0

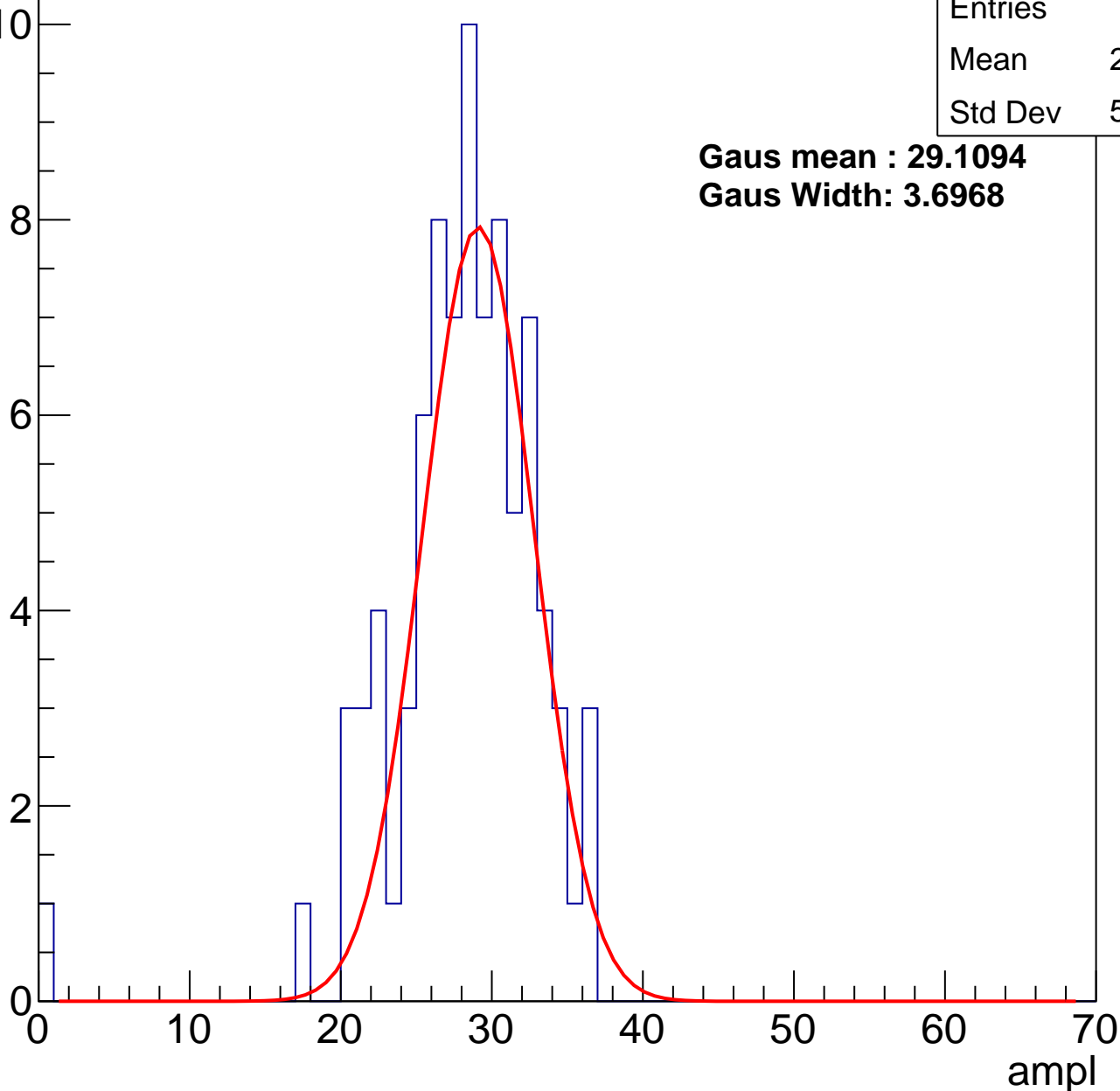
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	85
Mean	27.64
Std Dev	5.073

**Gaus mean : 29.1094**

**Gaus Width: 3.6968**



# B1L102S, U5-ch86, adc1

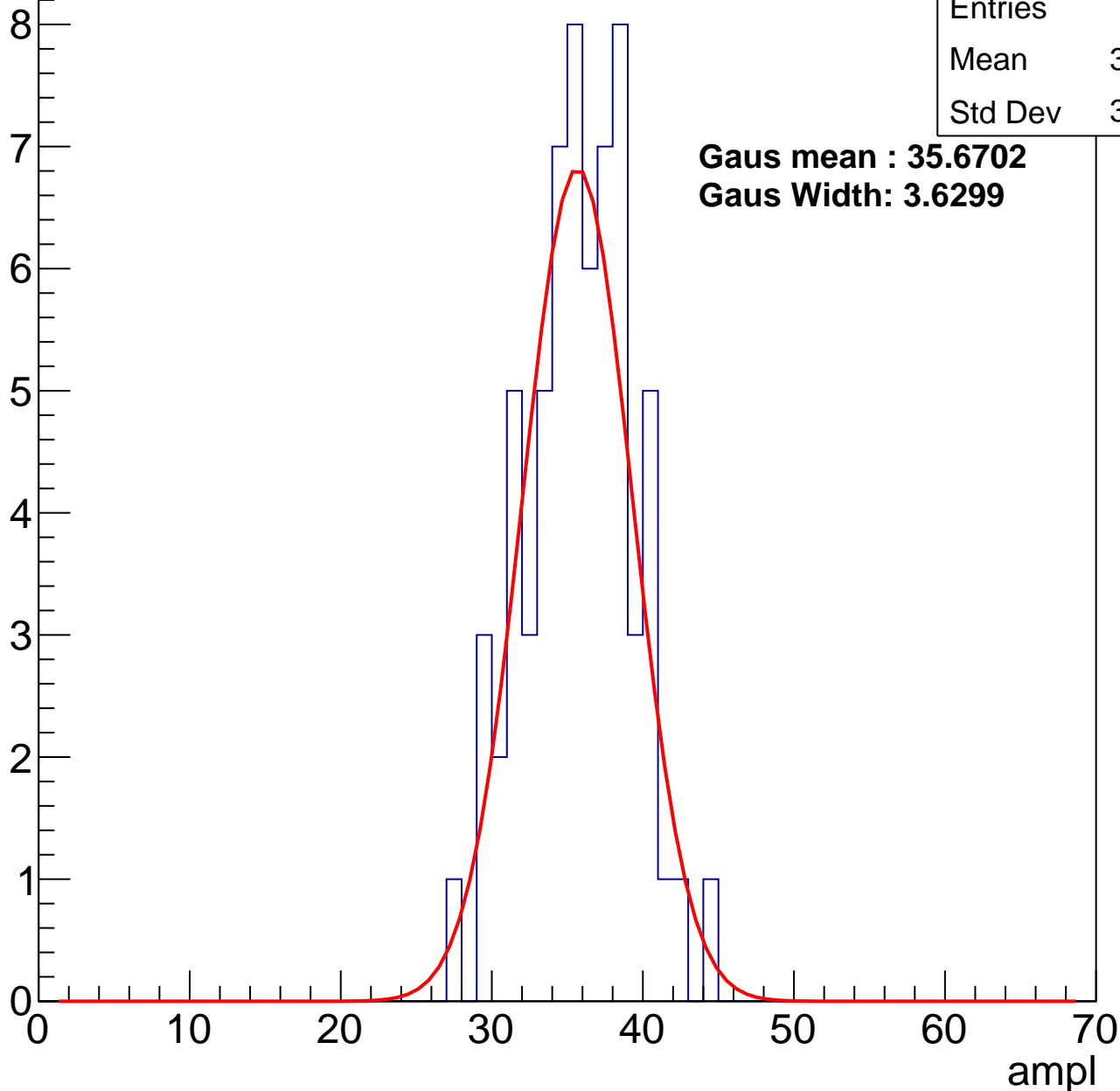
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	35.32
Std Dev	3.469

**Gaus mean : 35.6702**

**Gaus Width: 3.6299**



# B1L102S, U5-ch86, adc2

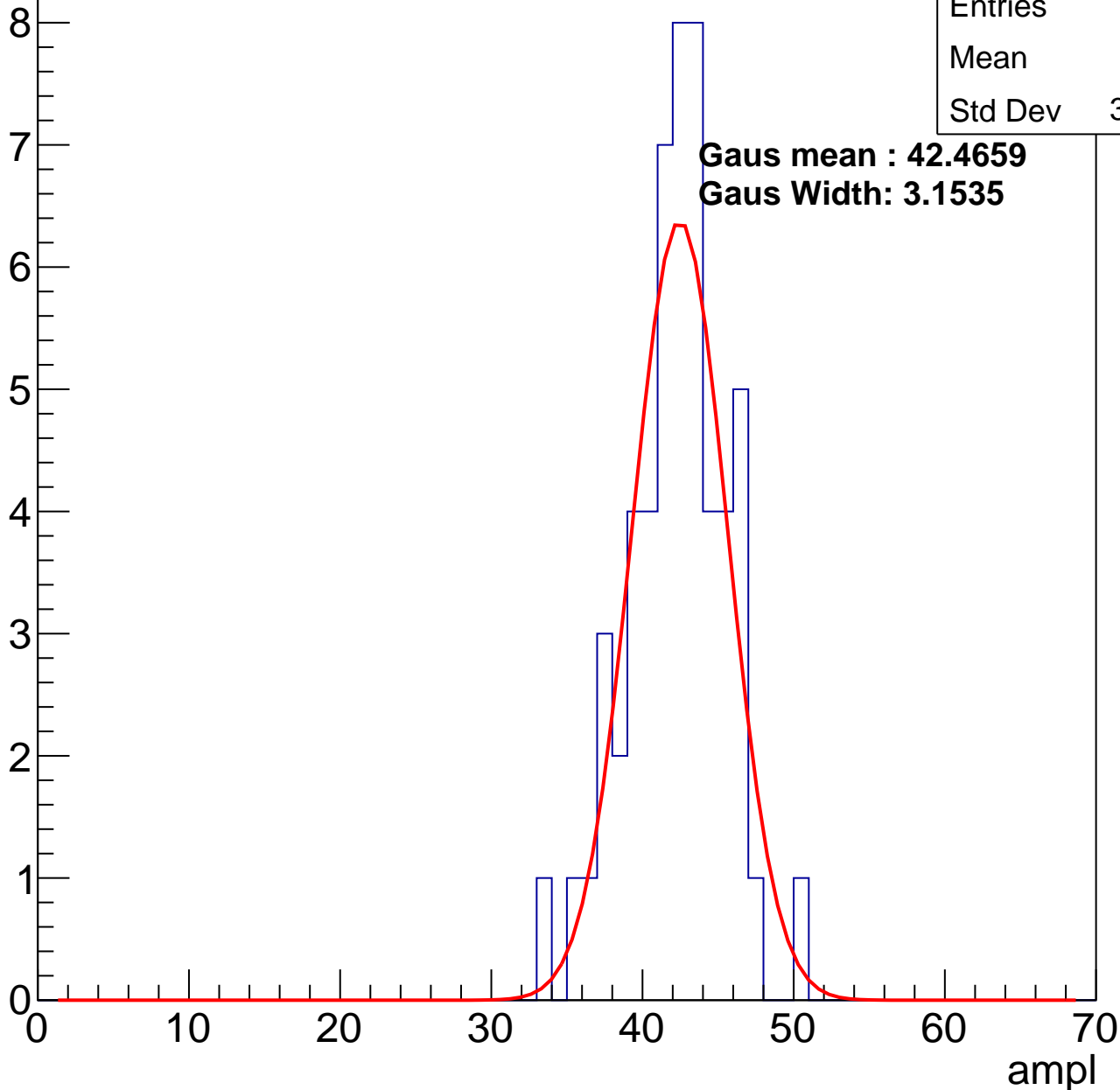
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	41.8
Std Dev	3.217

**Gaus mean : 42.4659**

**Gaus Width: 3.1535**



# B1L102S, U5-ch86, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	78
Mean	48
Std Dev	3.961

Entry

10

8

6

4

2

0

0

10

20

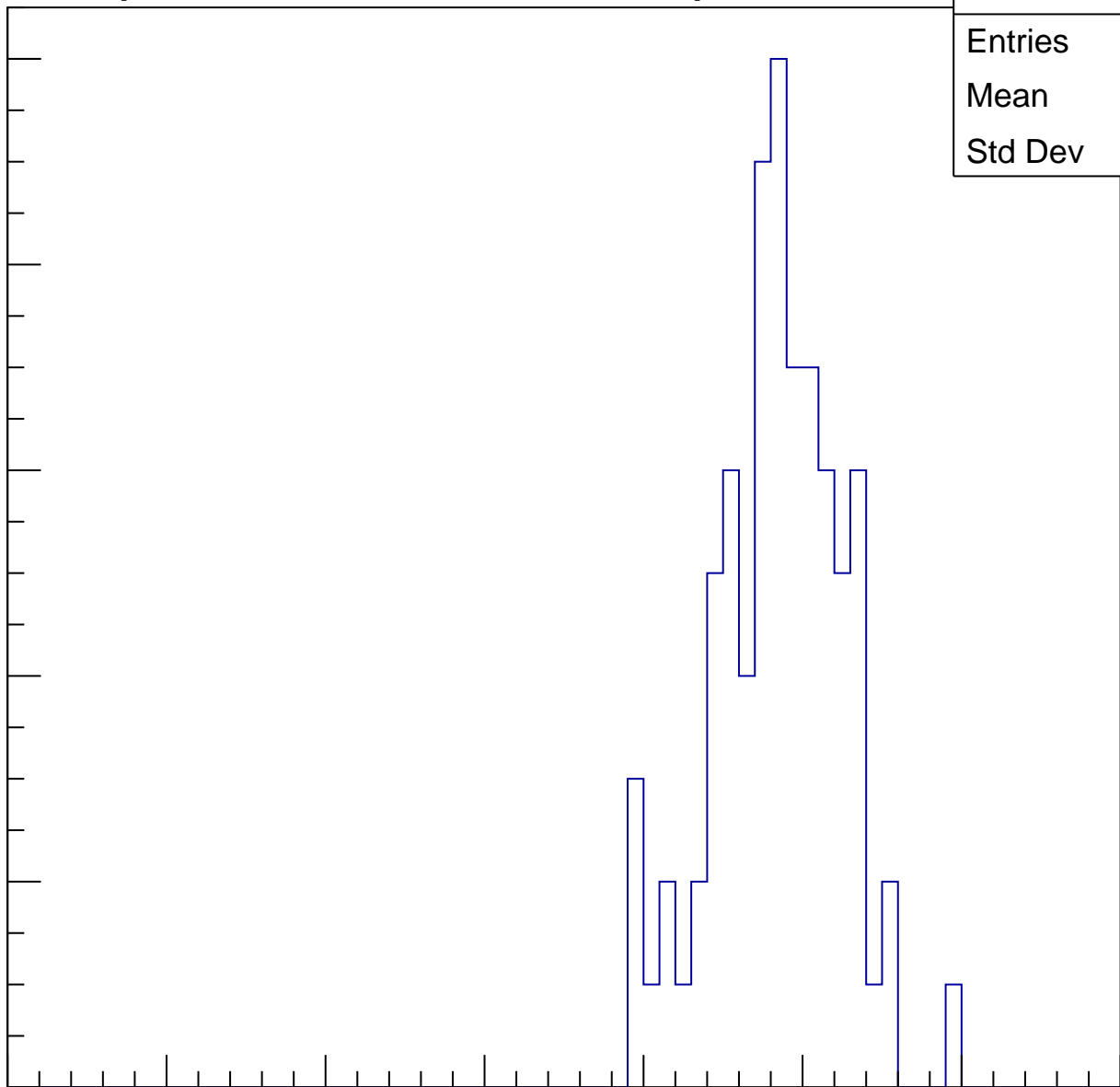
30

40

50

60

ampl

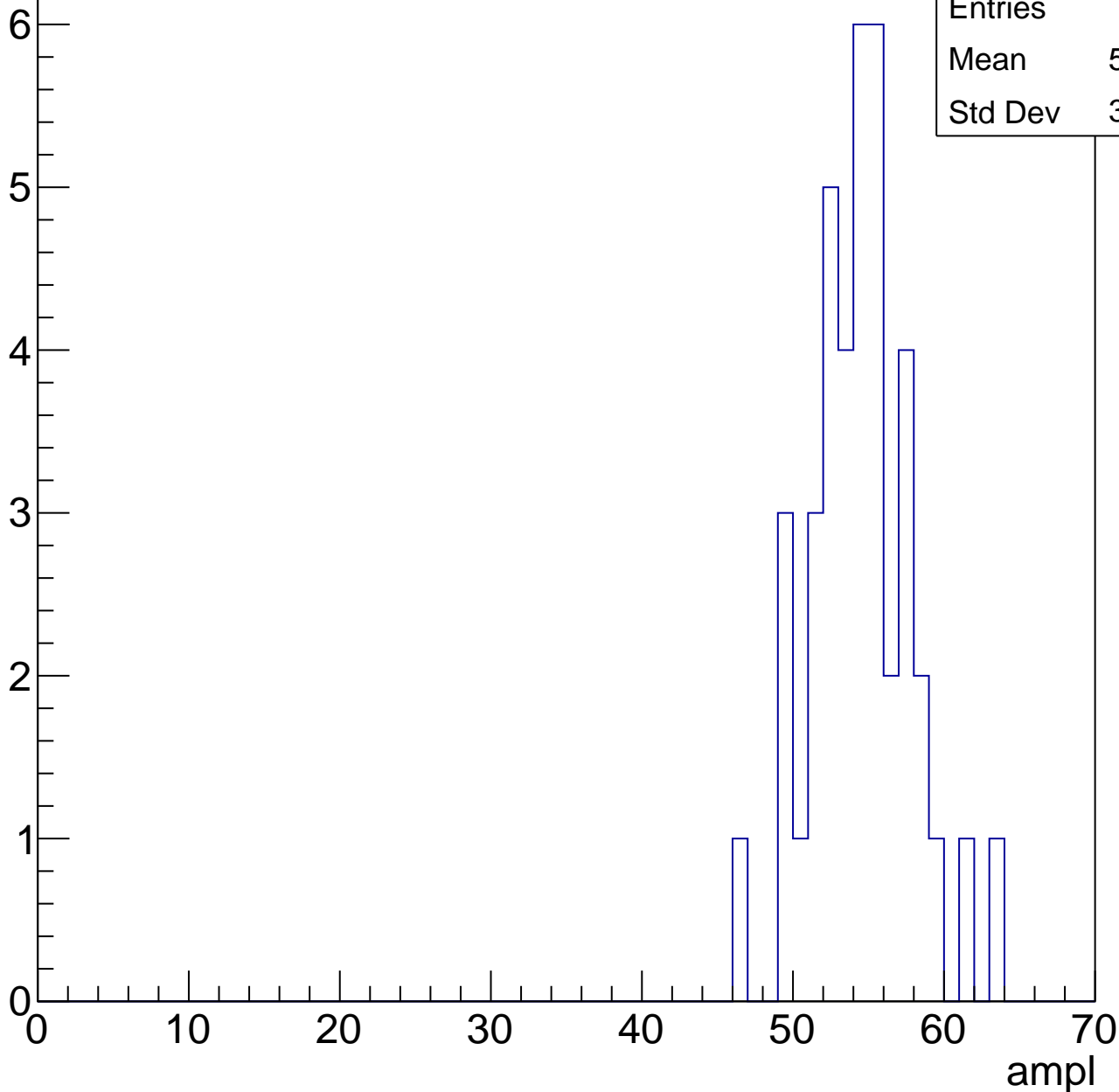


# B1L102S, U5-ch86, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	40
Mean	54.02
Std Dev	3.328

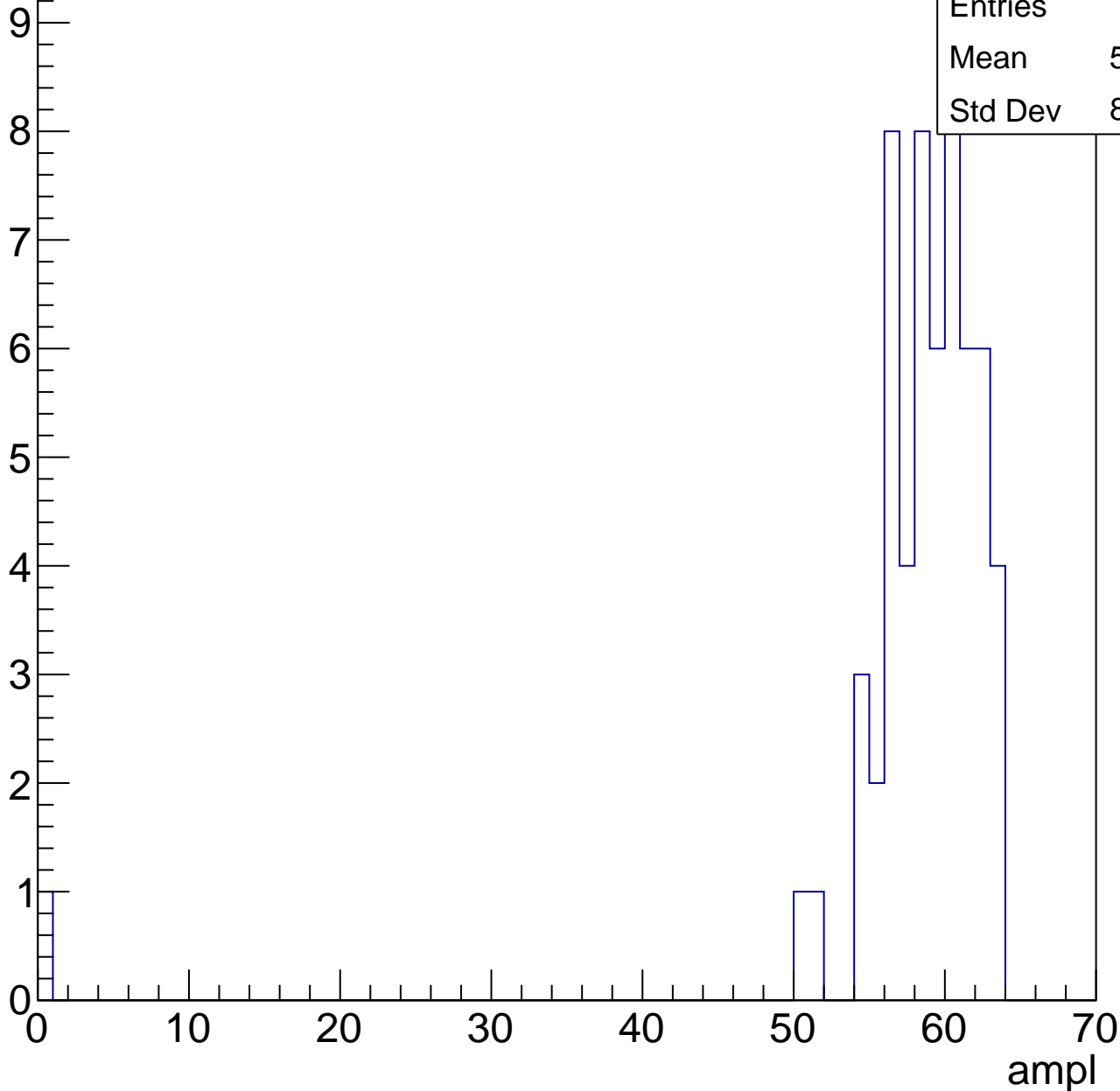


# B1L102S, U5-ch86, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	57.58
Std Dev	8.089

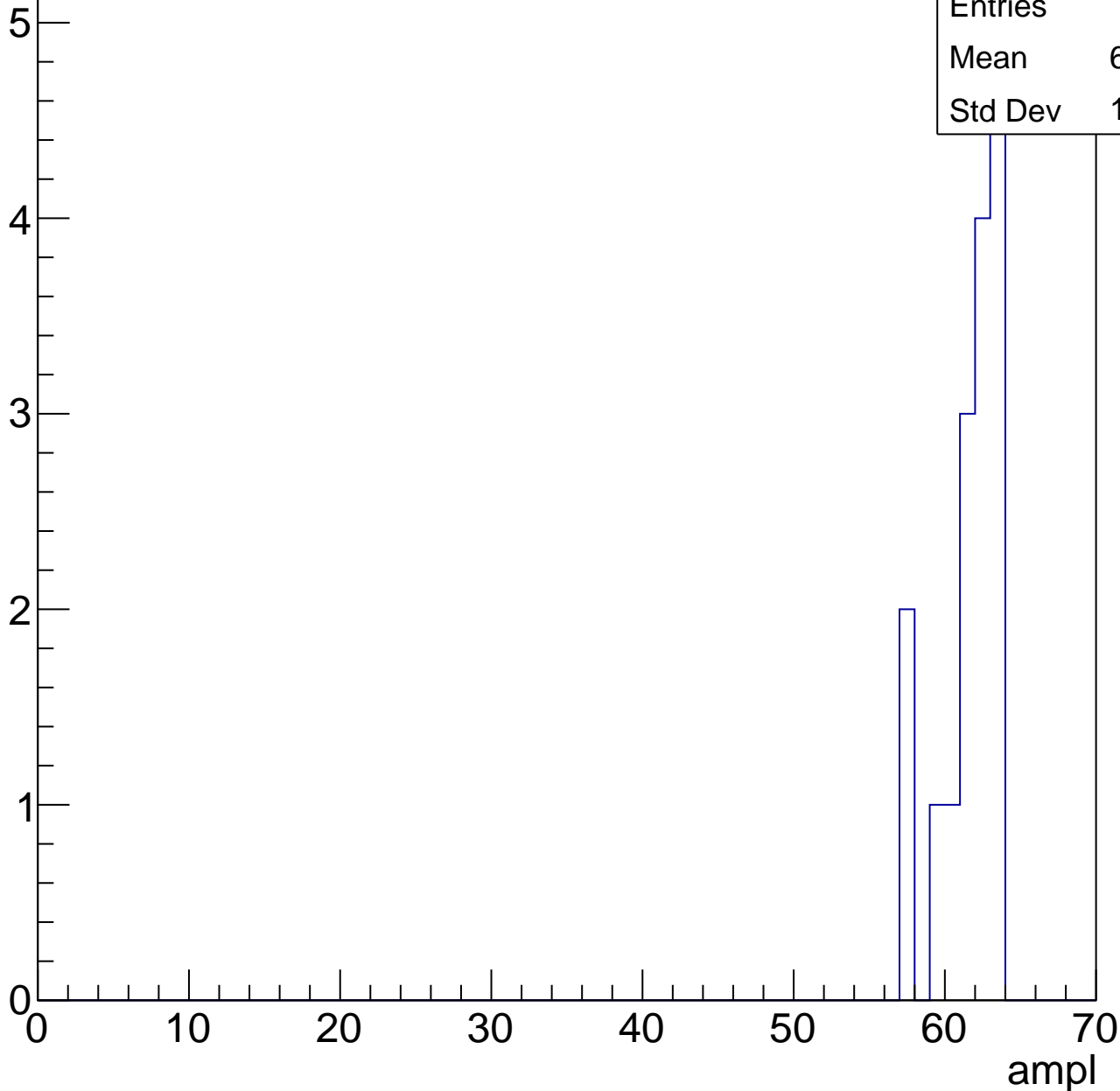


# B1L102S, U5-ch86, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	16
Mean	61.19
Std Dev	1.944

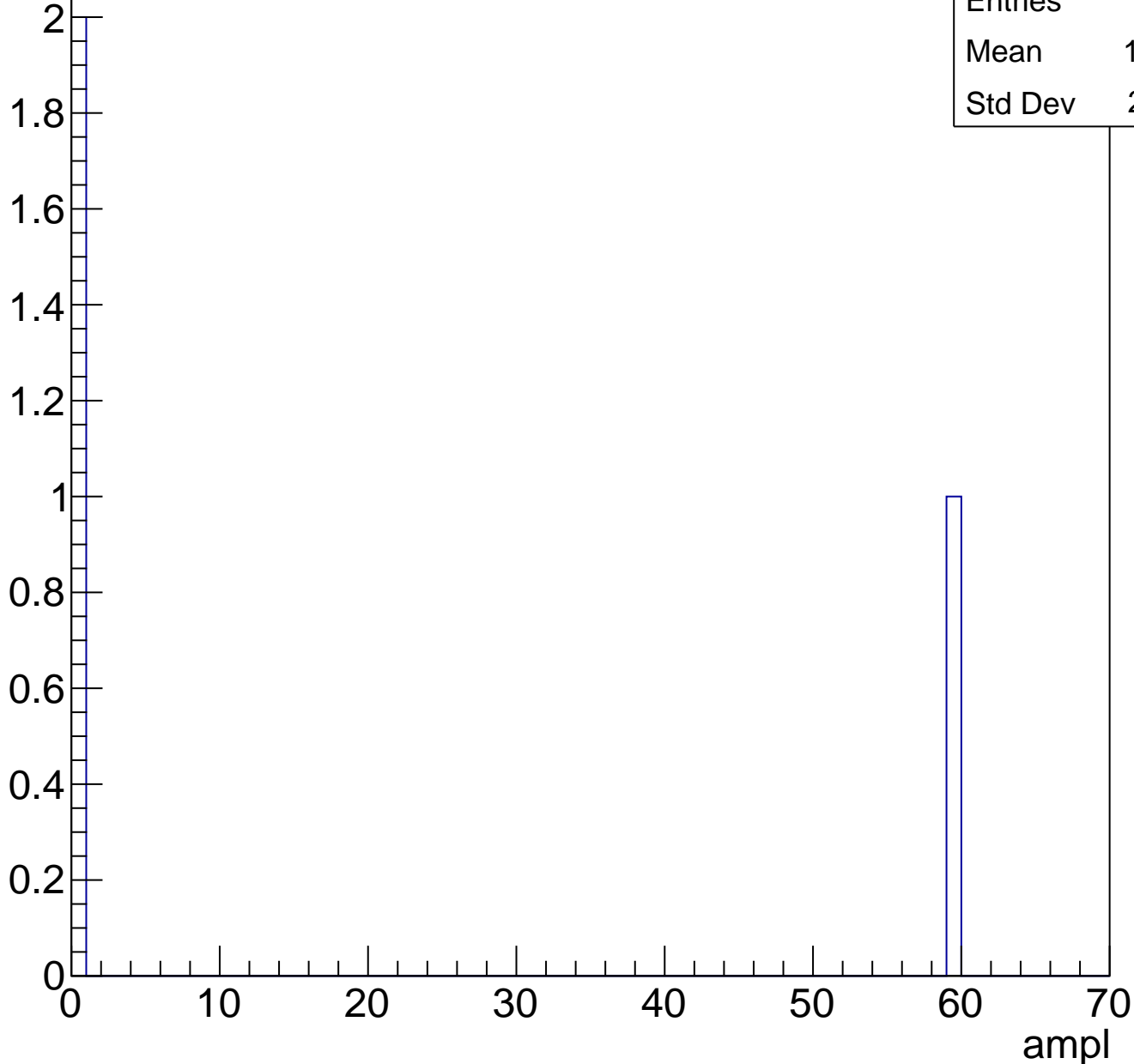




# B1L102S, U5-ch86, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U5-ch87, adc0

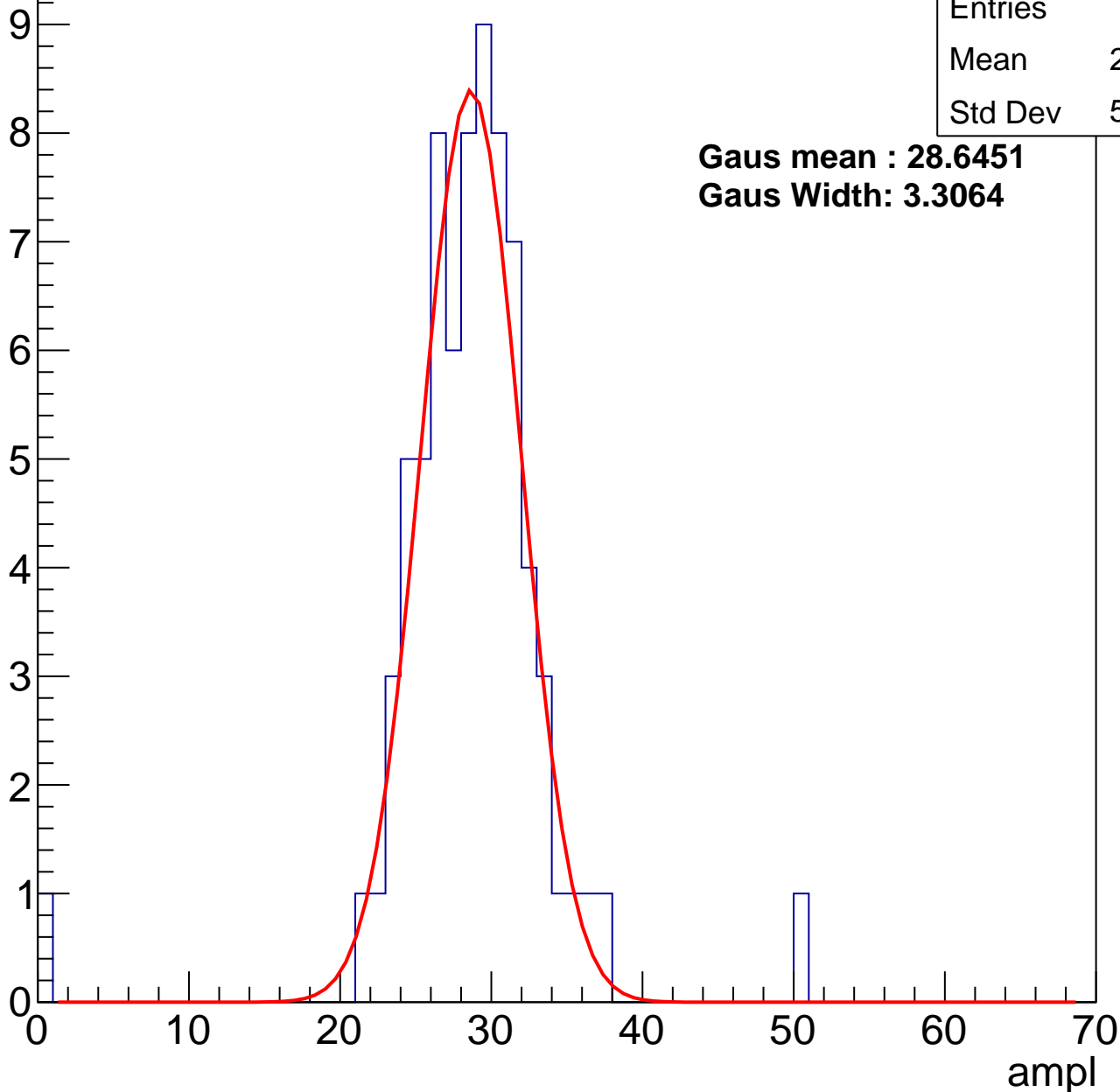
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	28.22
Std Dev	5.277

**Gaus mean : 28.6451**

**Gaus Width: 3.3064**



# B1L102S, U5-ch87, adc1

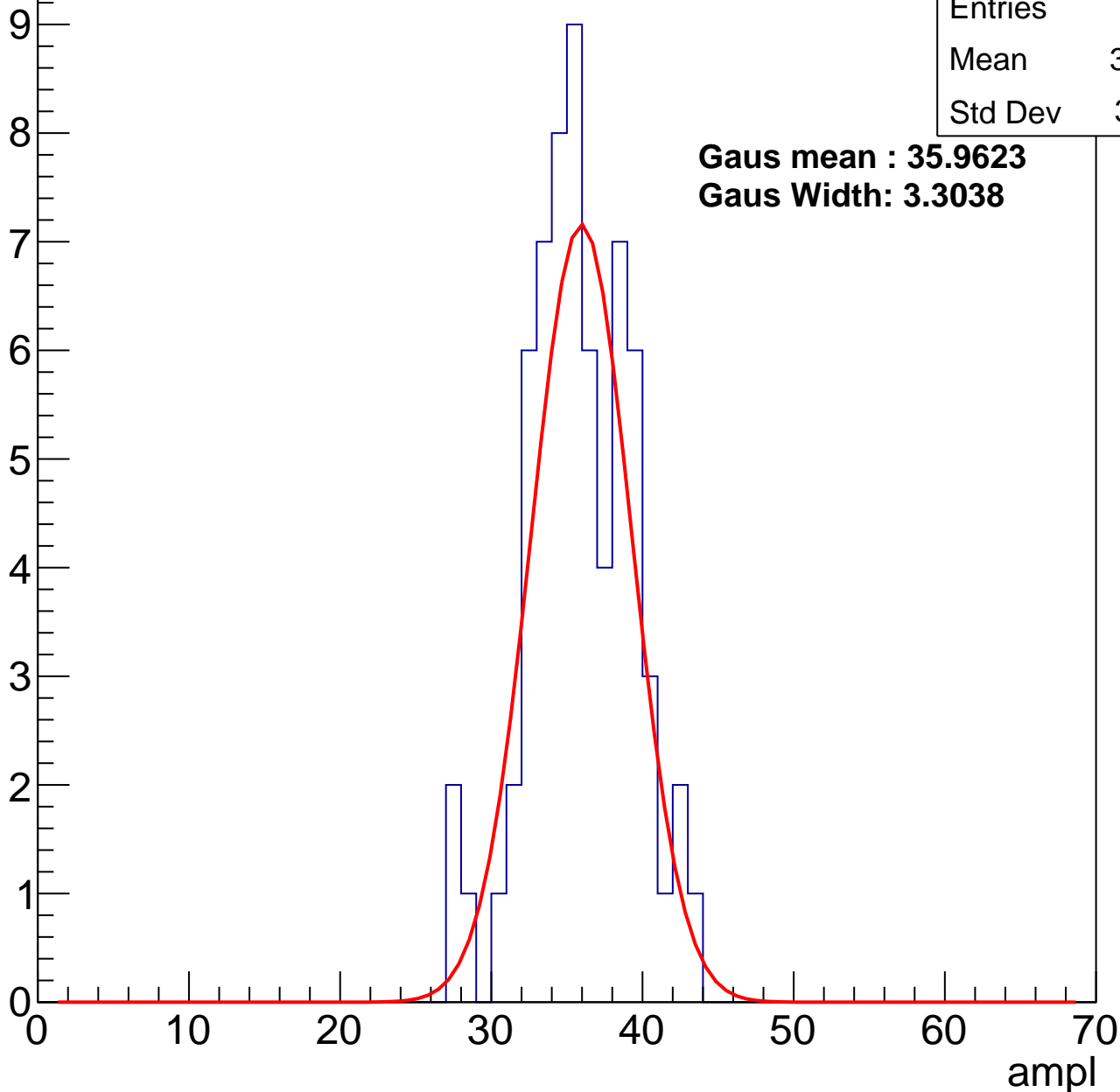
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	35.39
Std Dev	3.411

**Gaus mean : 35.9623**

**Gaus Width: 3.3038**

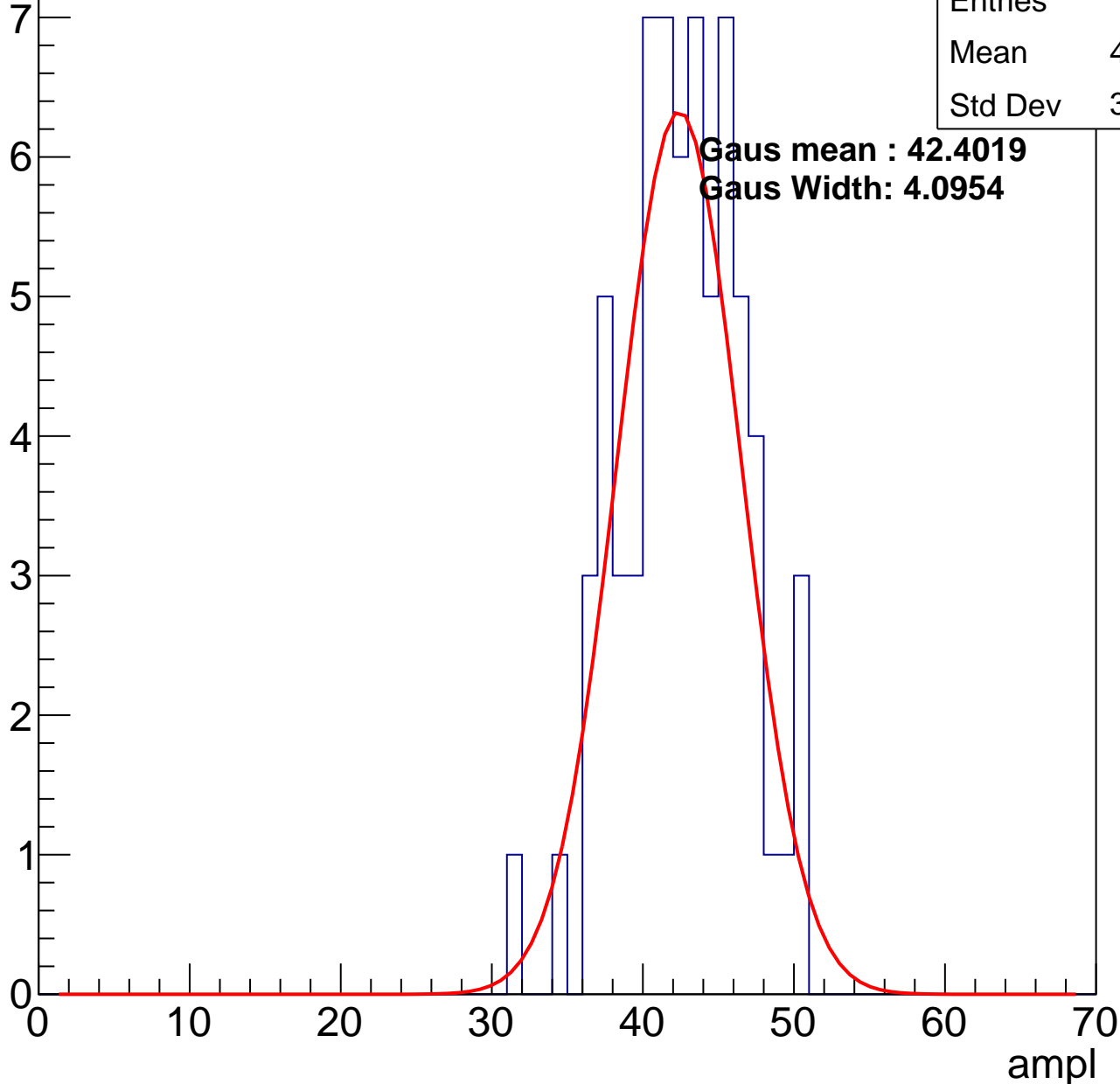


# B1L102S, U5-ch87, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	42.16
Std Dev	3.944

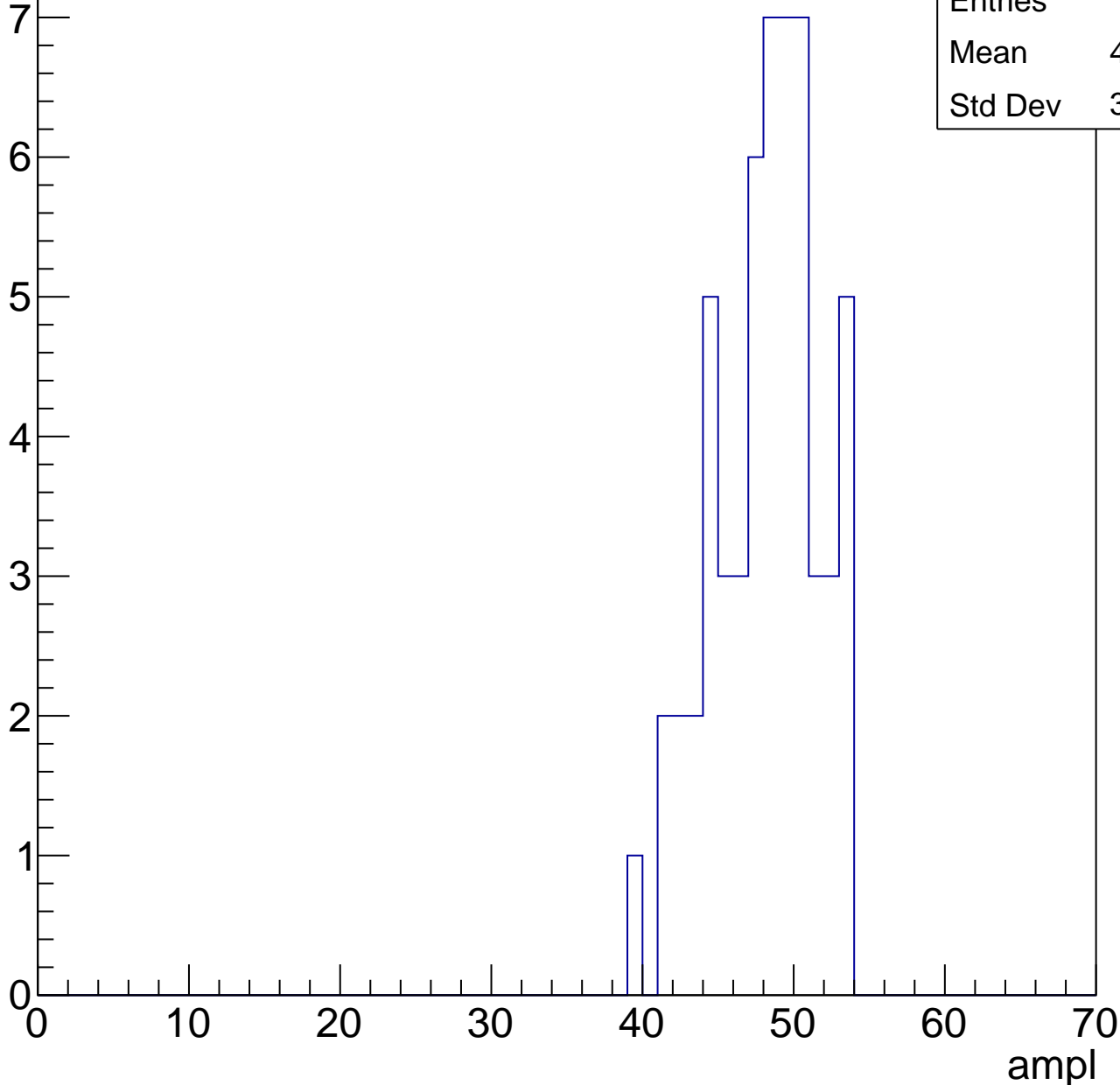


# B1L102S, U5-ch87, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	47.66
Std Dev	3.419

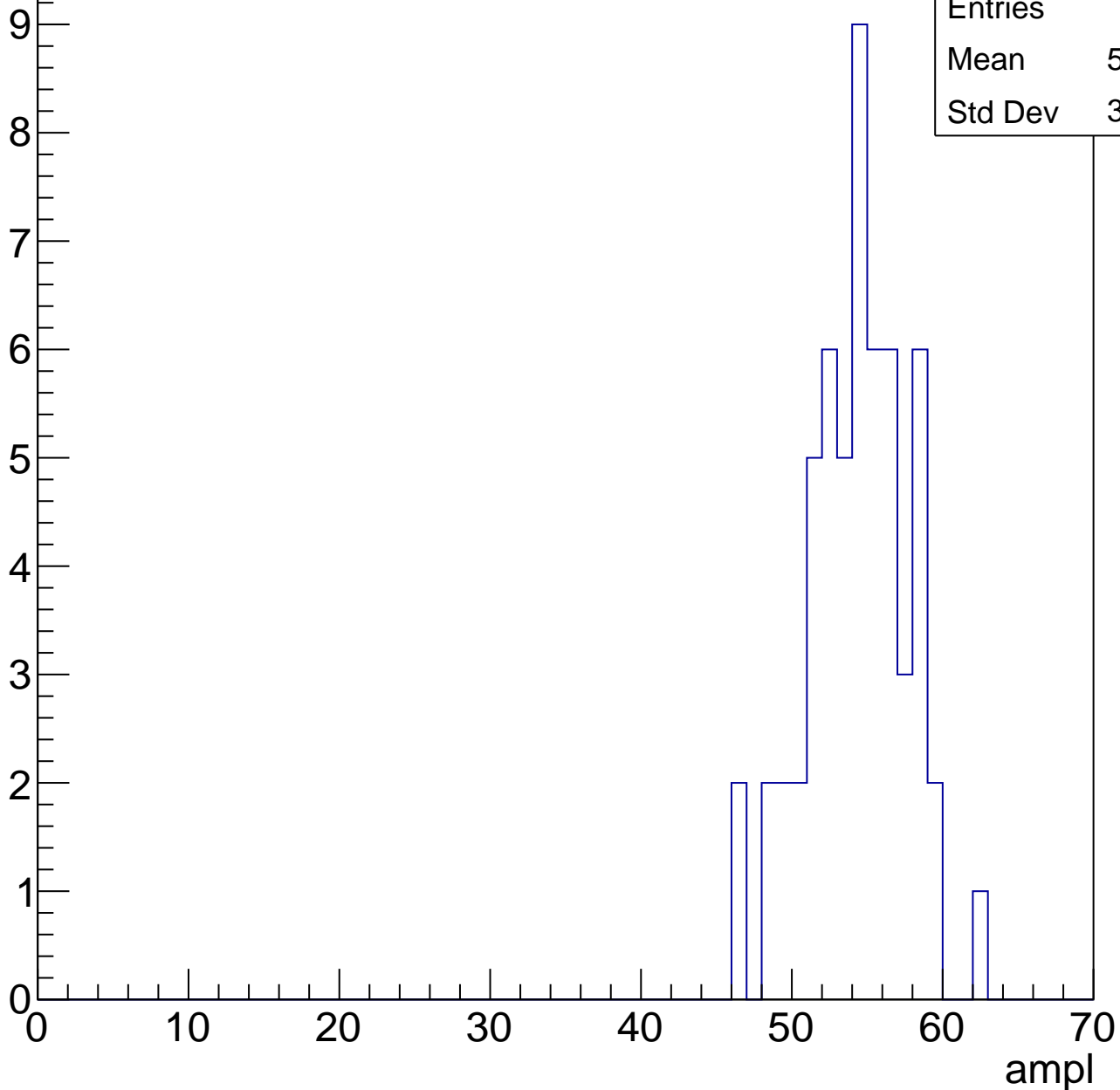


# B1L102S, U5-ch87, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	53.84
Std Dev	3.302

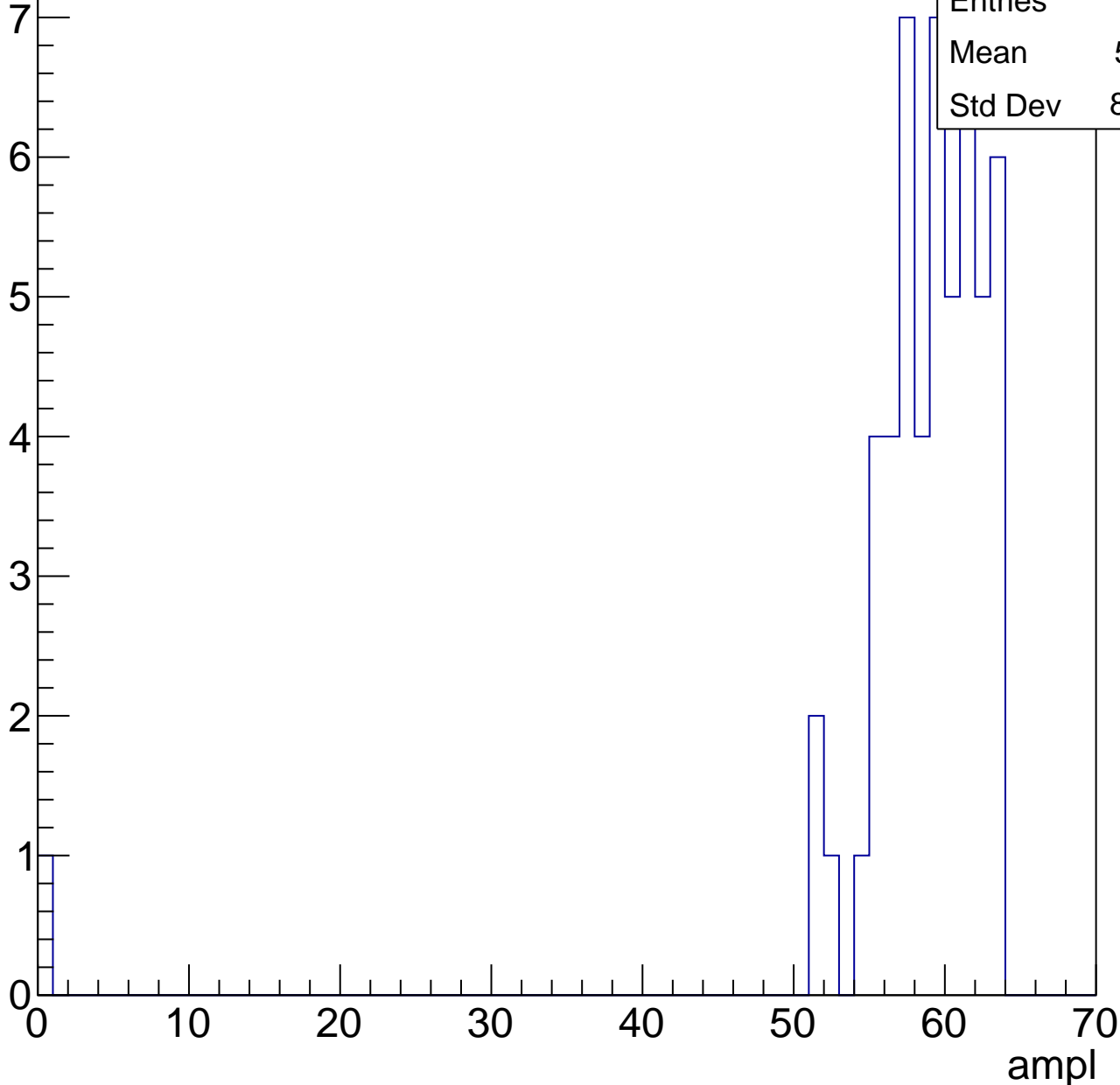


# B1L102S, U5-ch87, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	57.61
Std Dev	8.482

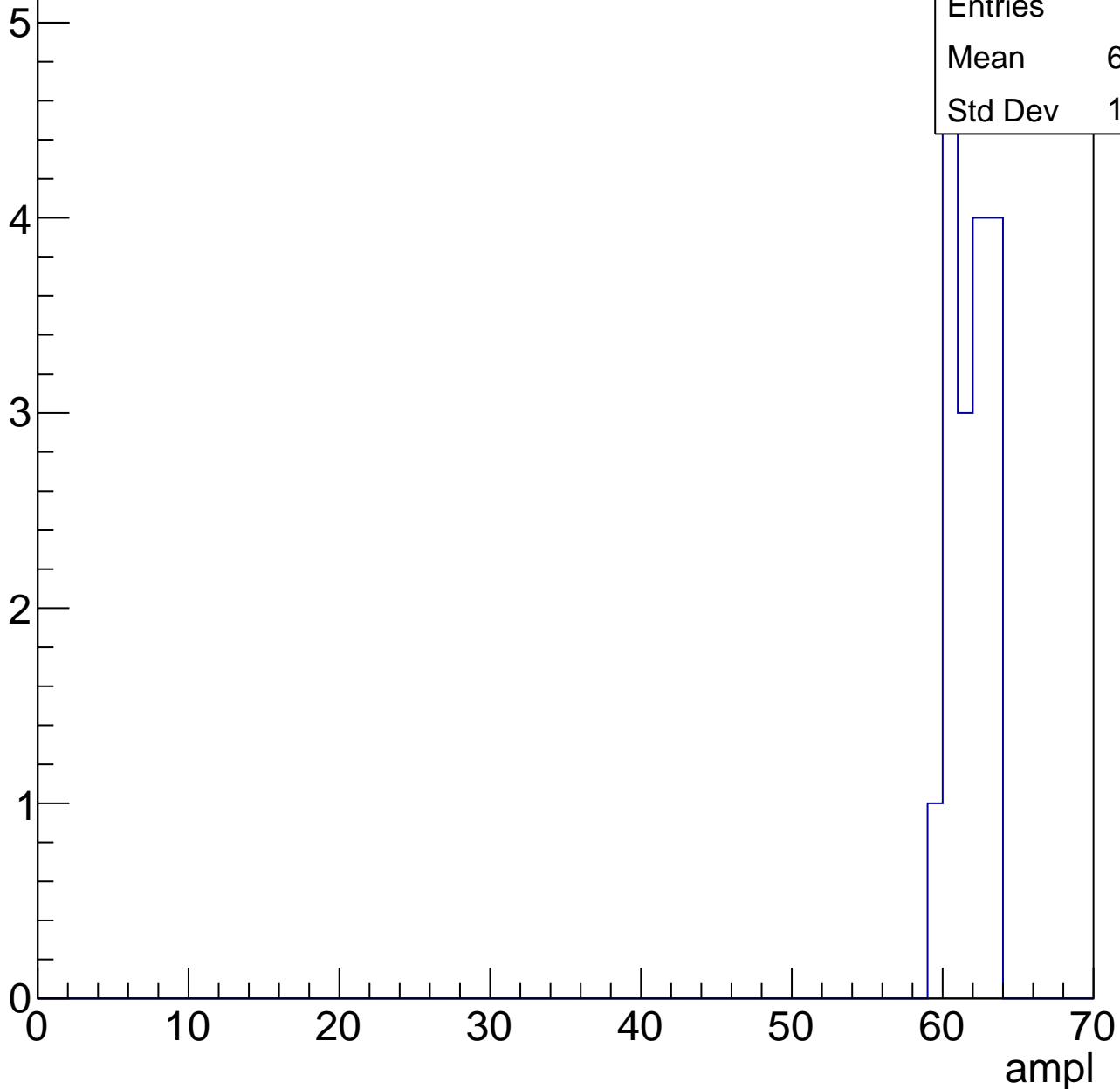


# B1L102S, U5-ch87, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	17
Mean	61.29
Std Dev	1.273





# B1L102S, U5-ch87, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U5-ch88, adc0

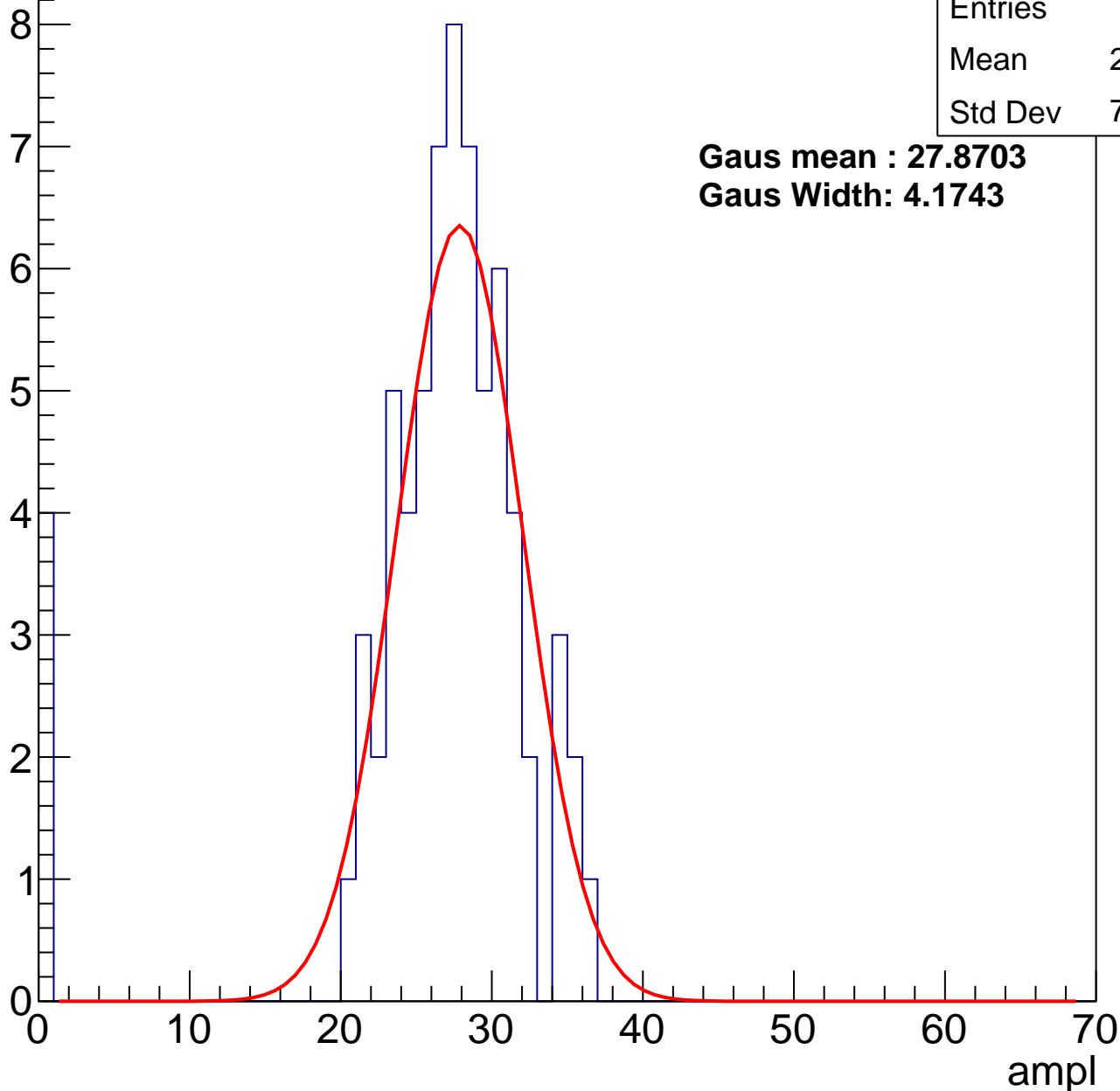
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	25.77
Std Dev	7.335

**Gaus mean : 27.8703**

**Gaus Width: 4.1743**



# B1L102S, U5-ch88, adc1

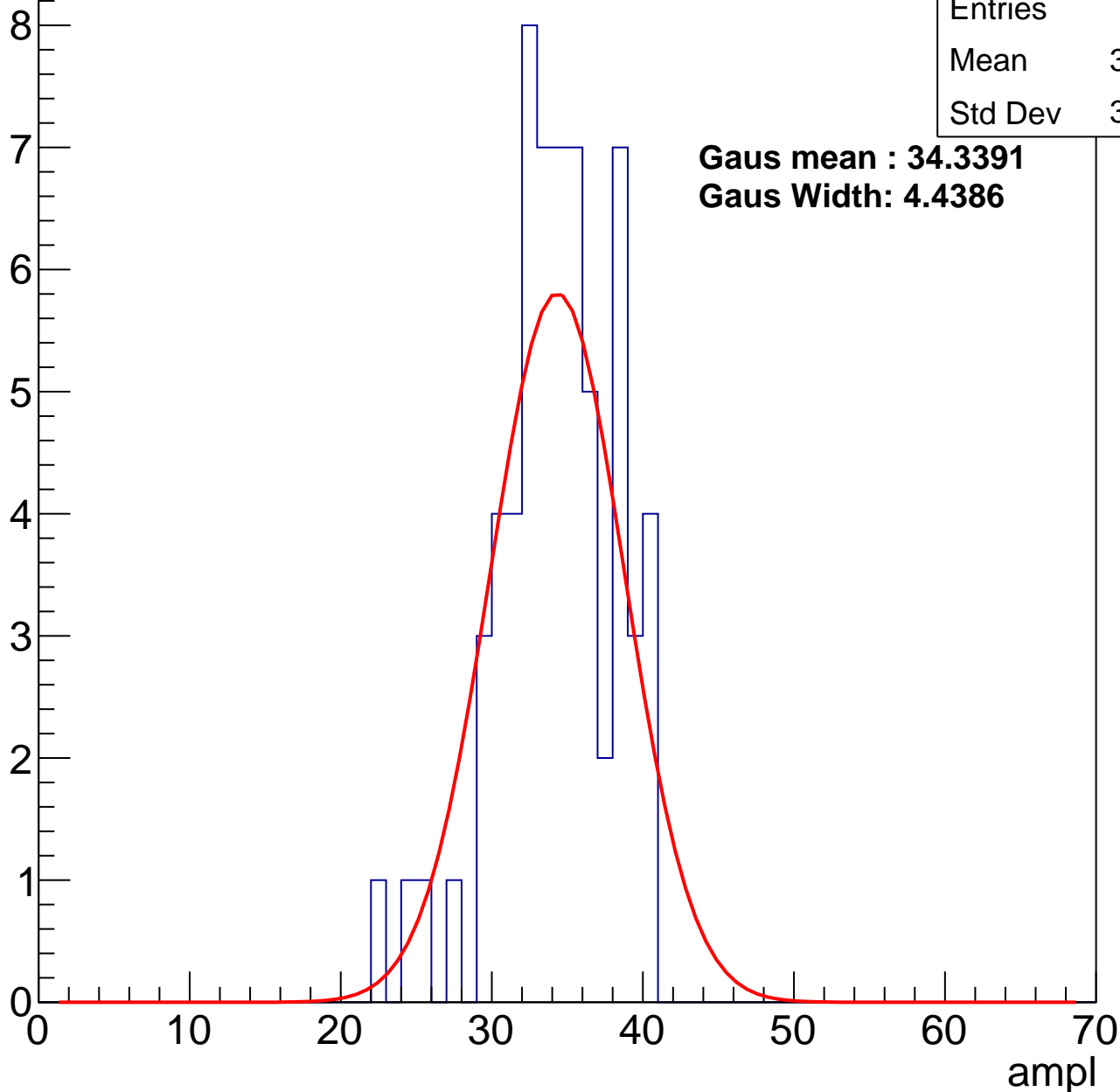
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	33.78
Std Dev	3.845

**Gaus mean : 34.3391**

**Gaus Width: 4.4386**



# B1L102S, U5-ch88, adc2

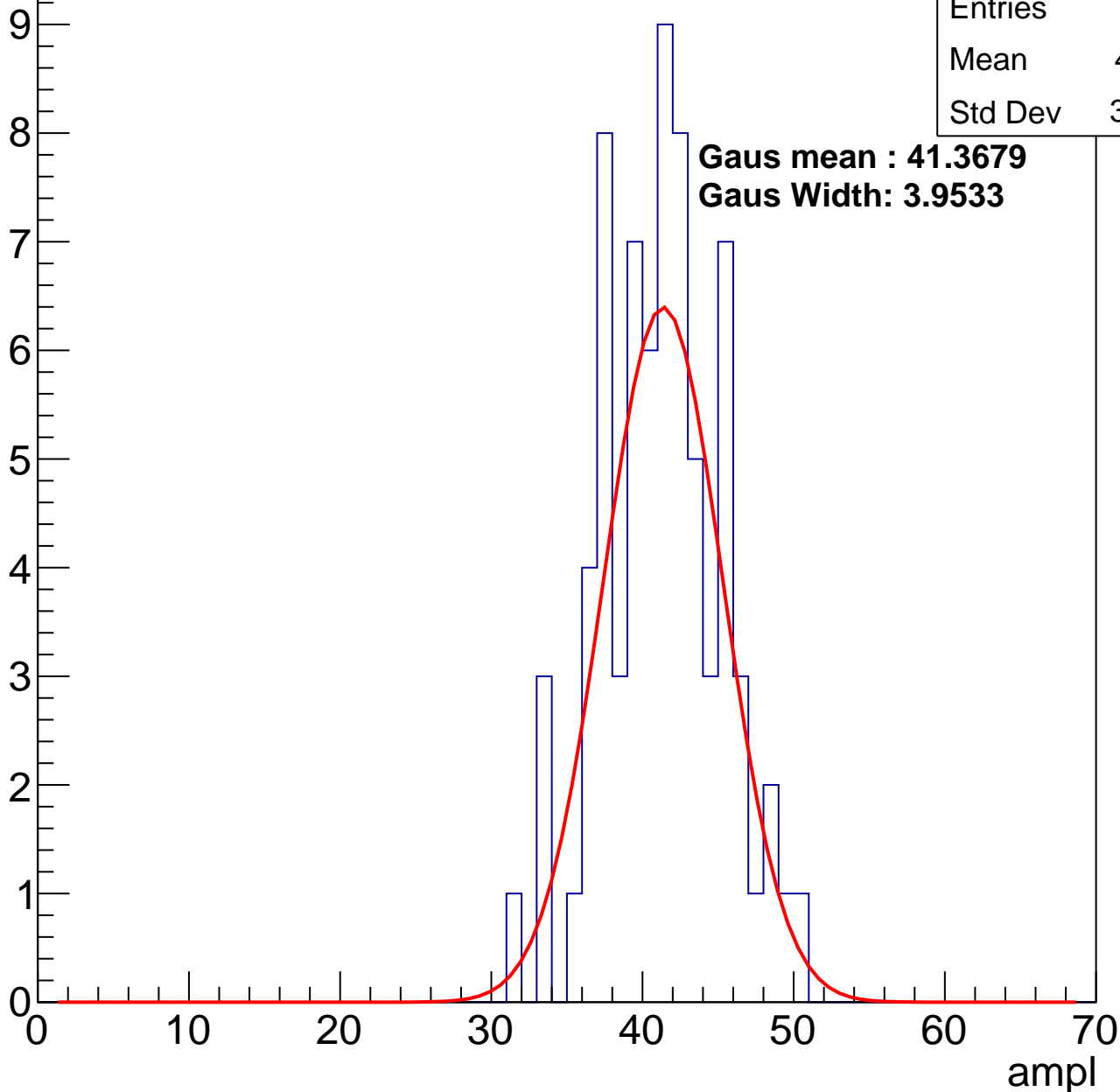
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	40.81
Std Dev	3.944

**Gaus mean : 41.3679**

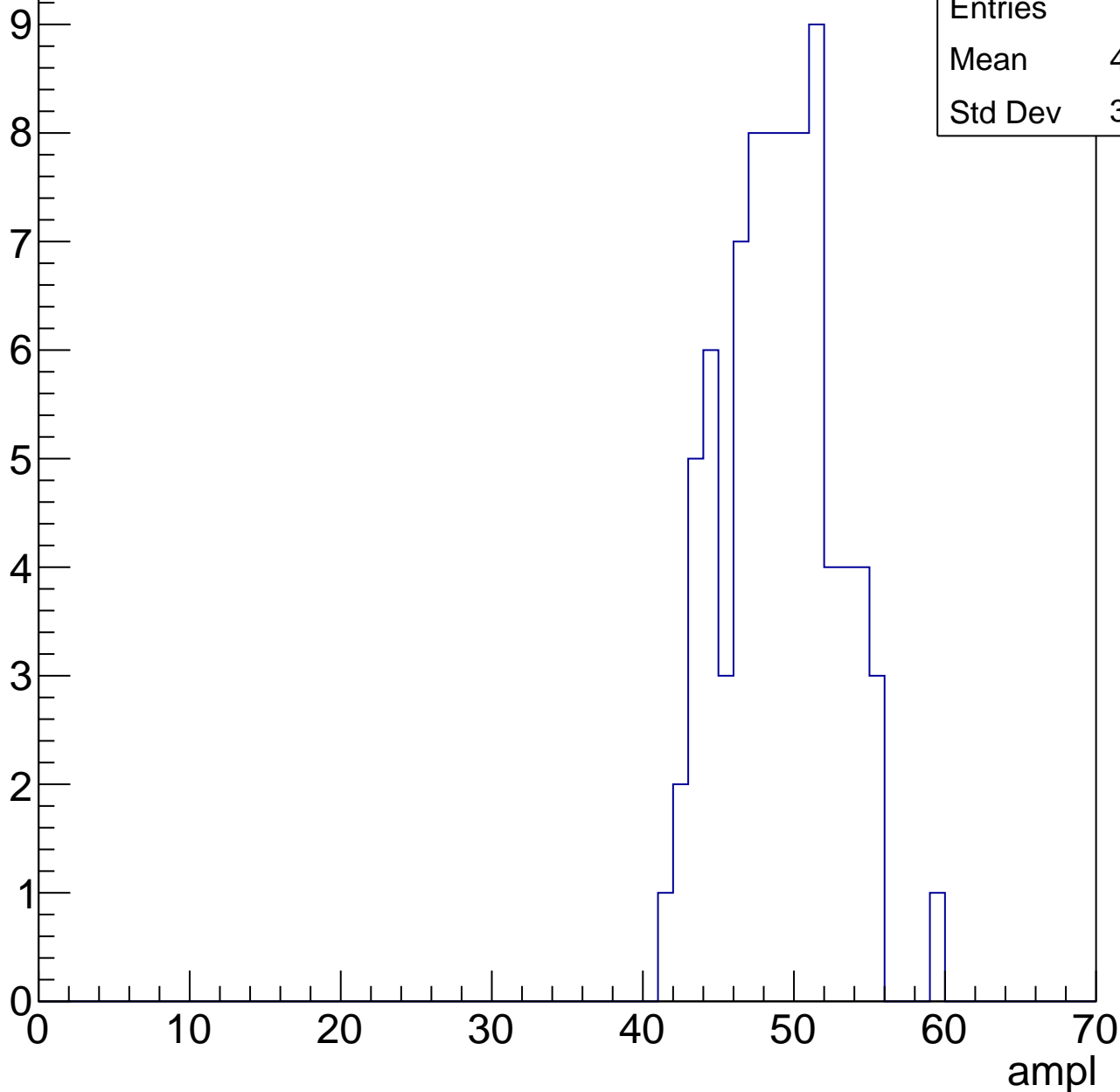
**Gaus Width: 3.9533**



# B1L102S, U5-ch88, adc3

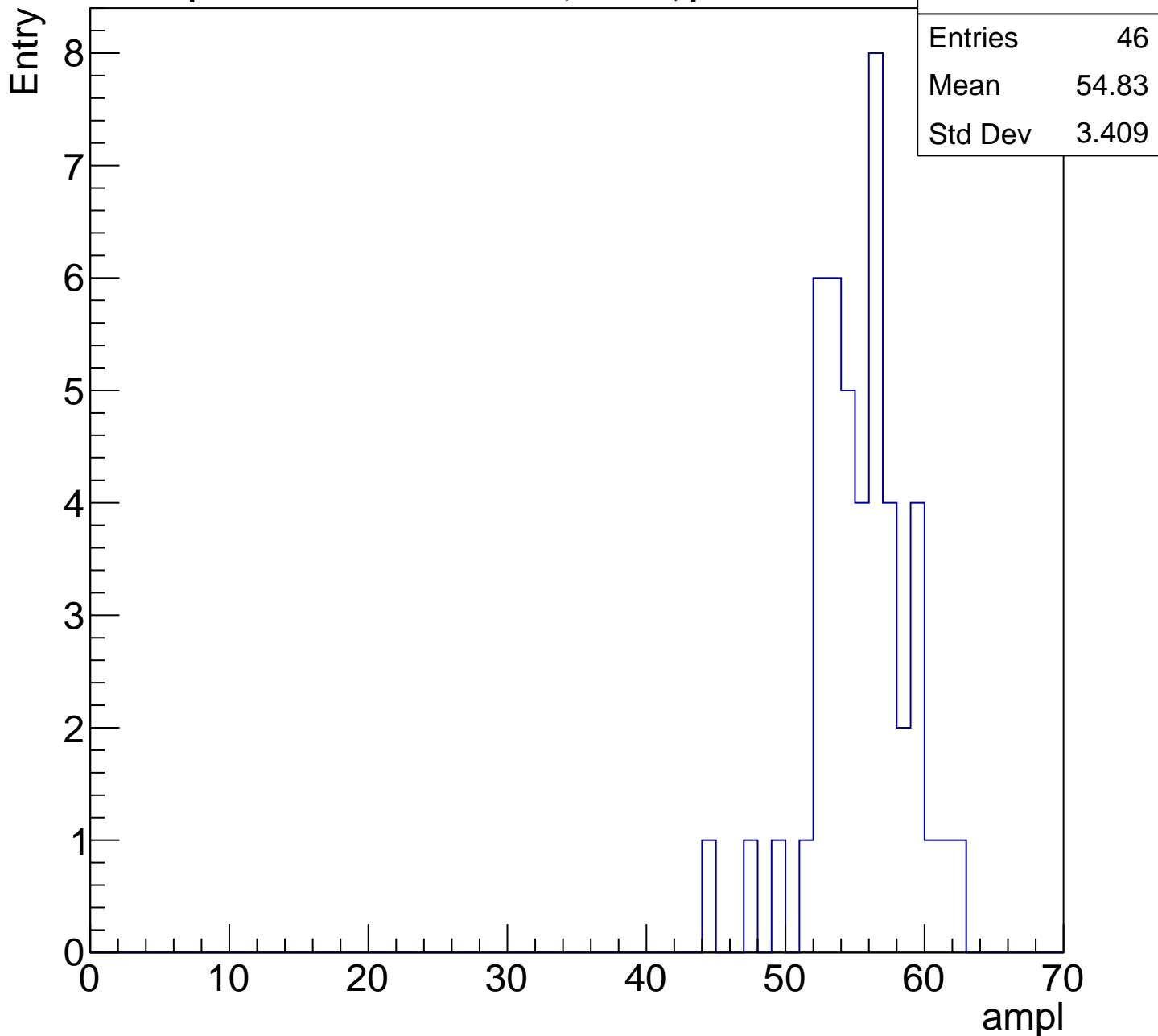
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U5-ch88, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

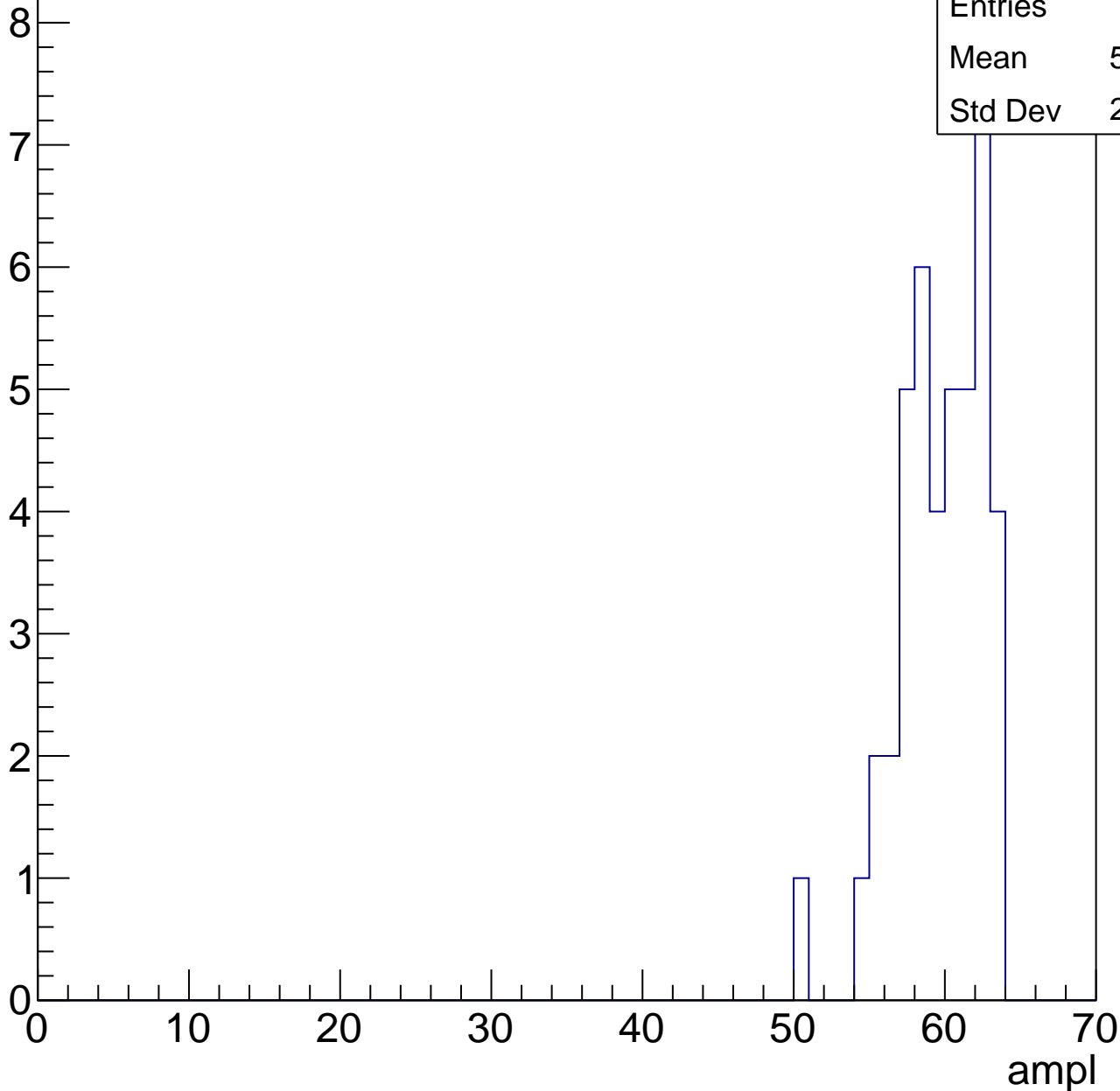


# B1L102S, U5-ch88, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	43
Mean	59.26
Std Dev	2.813

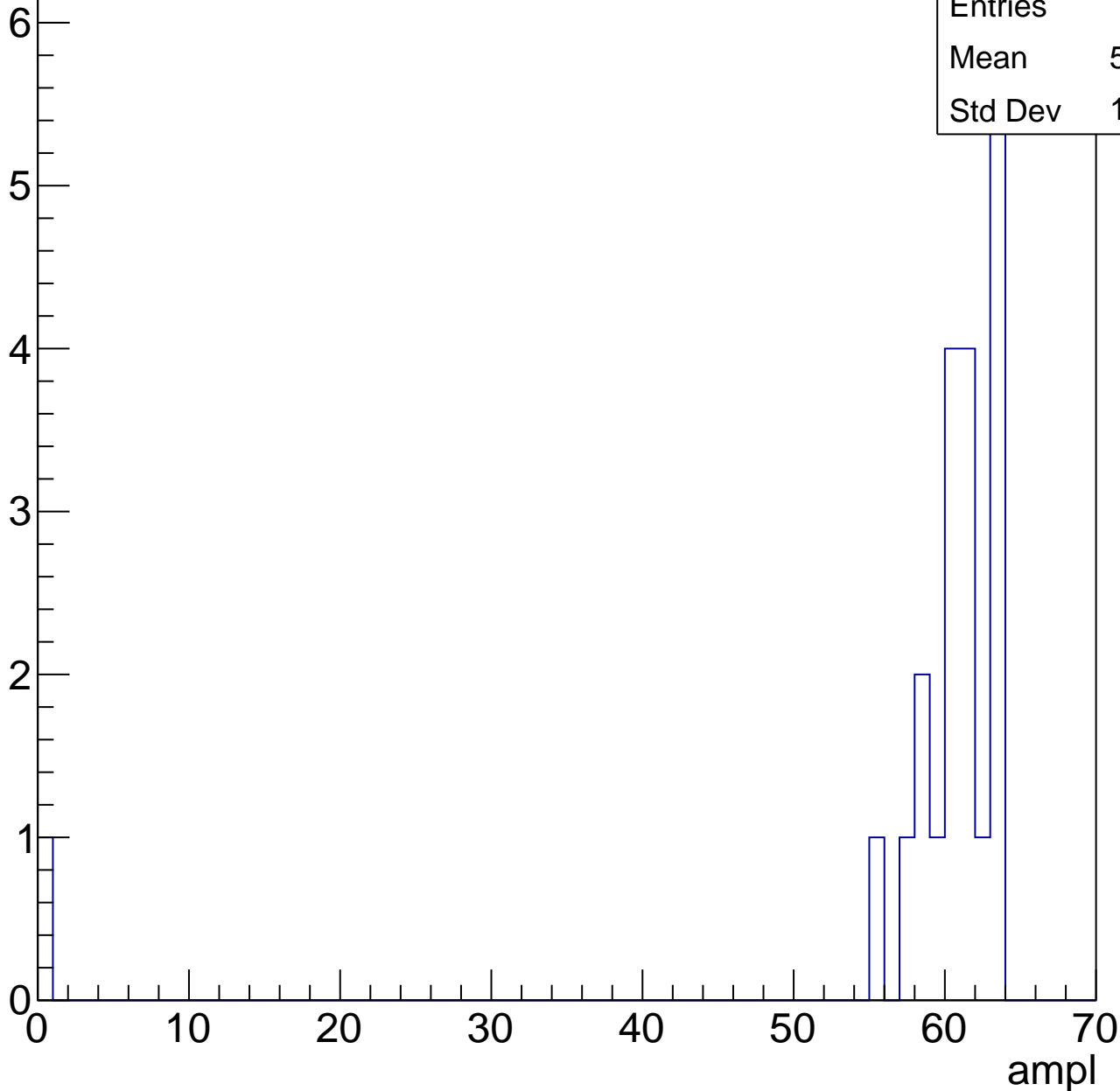


# B1L102S, U5-ch88, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	21
Mean	57.67
Std Dev	13.08





# B1L102S, U5-ch88, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U5-ch89, adc0

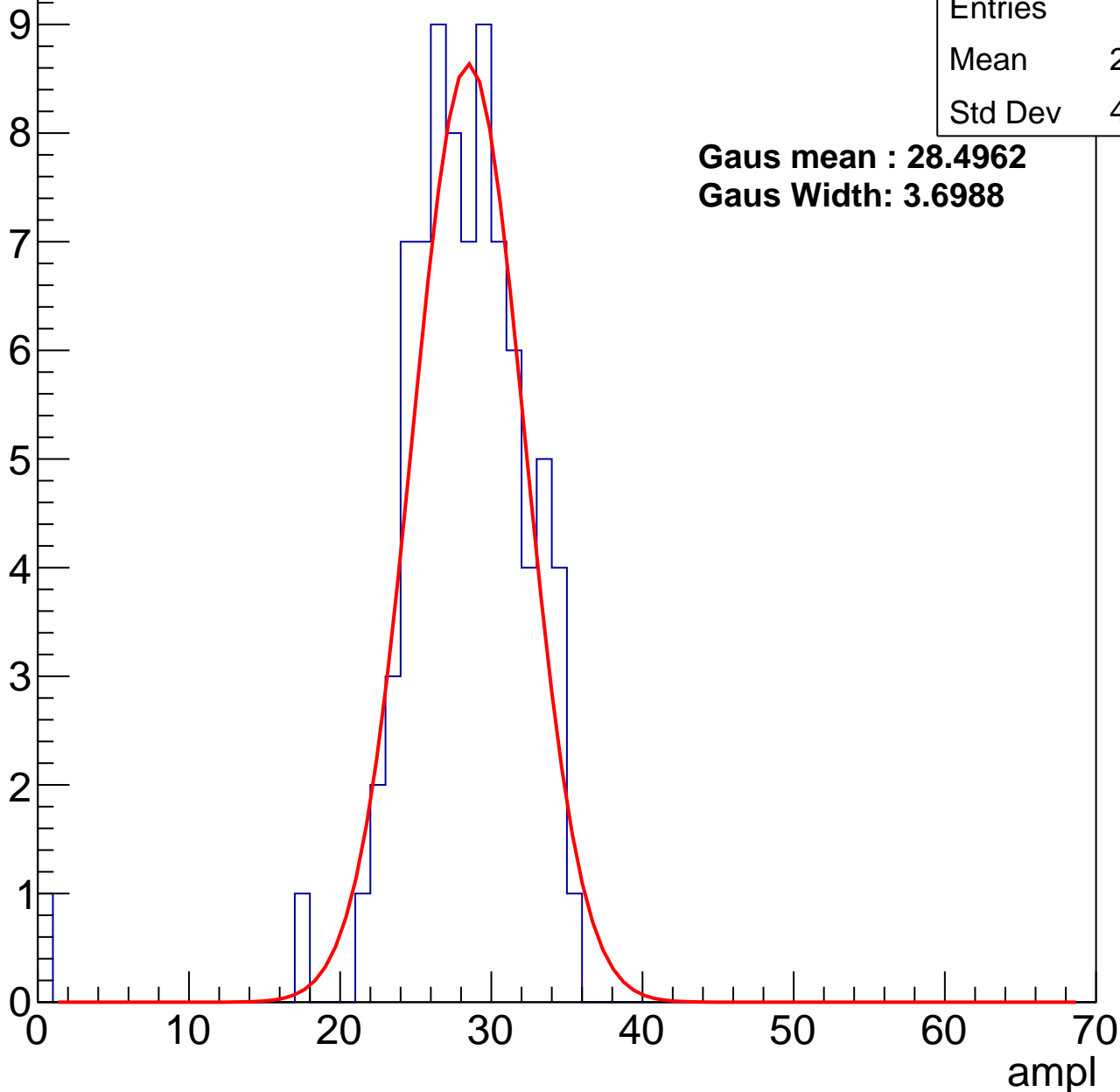
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	82
Mean	27.57
Std Dev	4.657

**Gaus mean : 28.4962**

**Gaus Width: 3.6988**



# B1L102S, U5-ch89, adc1

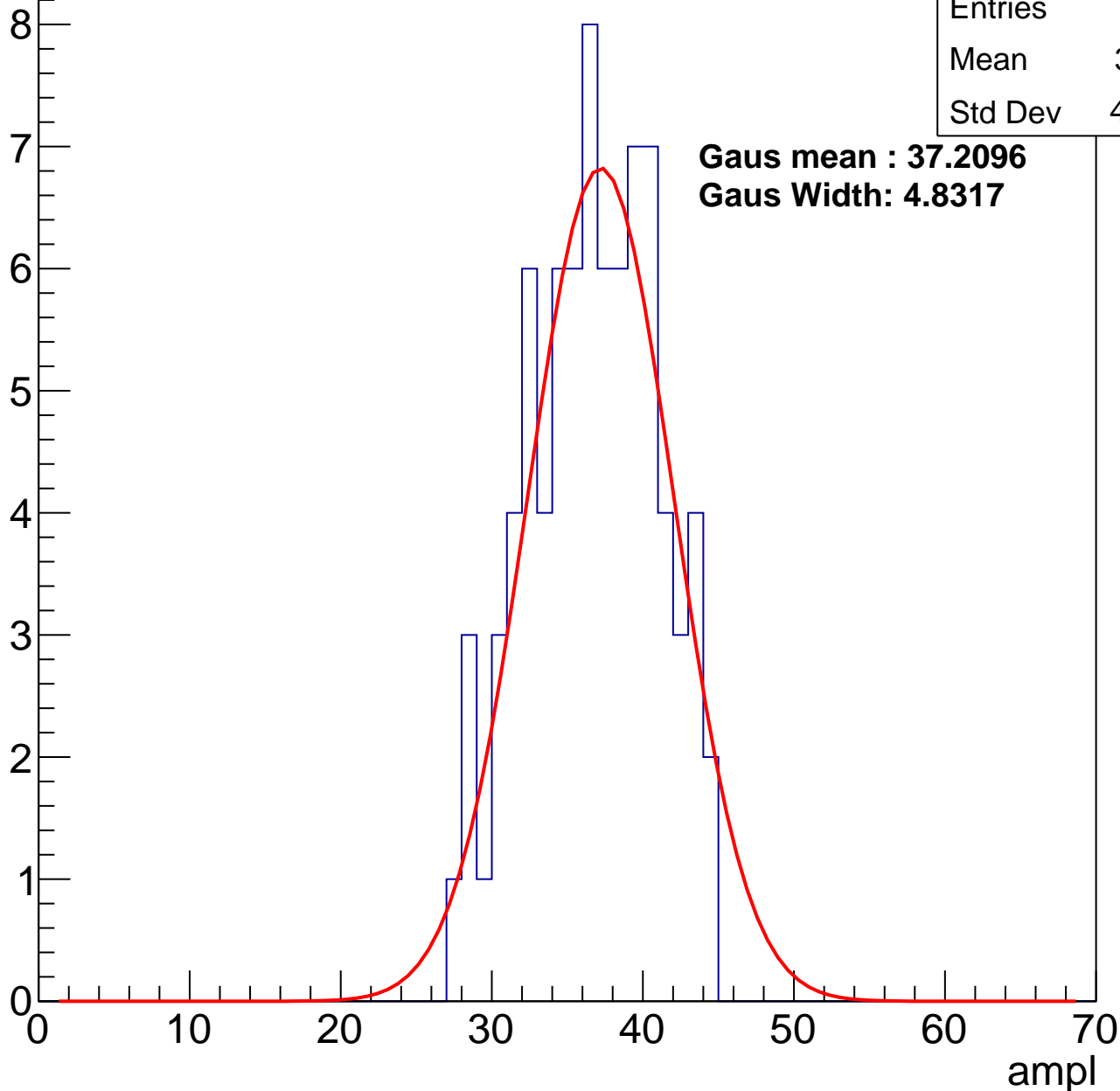
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	81
Mean	36.21
Std Dev	4.195

**Gaus mean : 37.2096**

**Gaus Width: 4.8317**



# B1L102S, U5-ch89, adc2

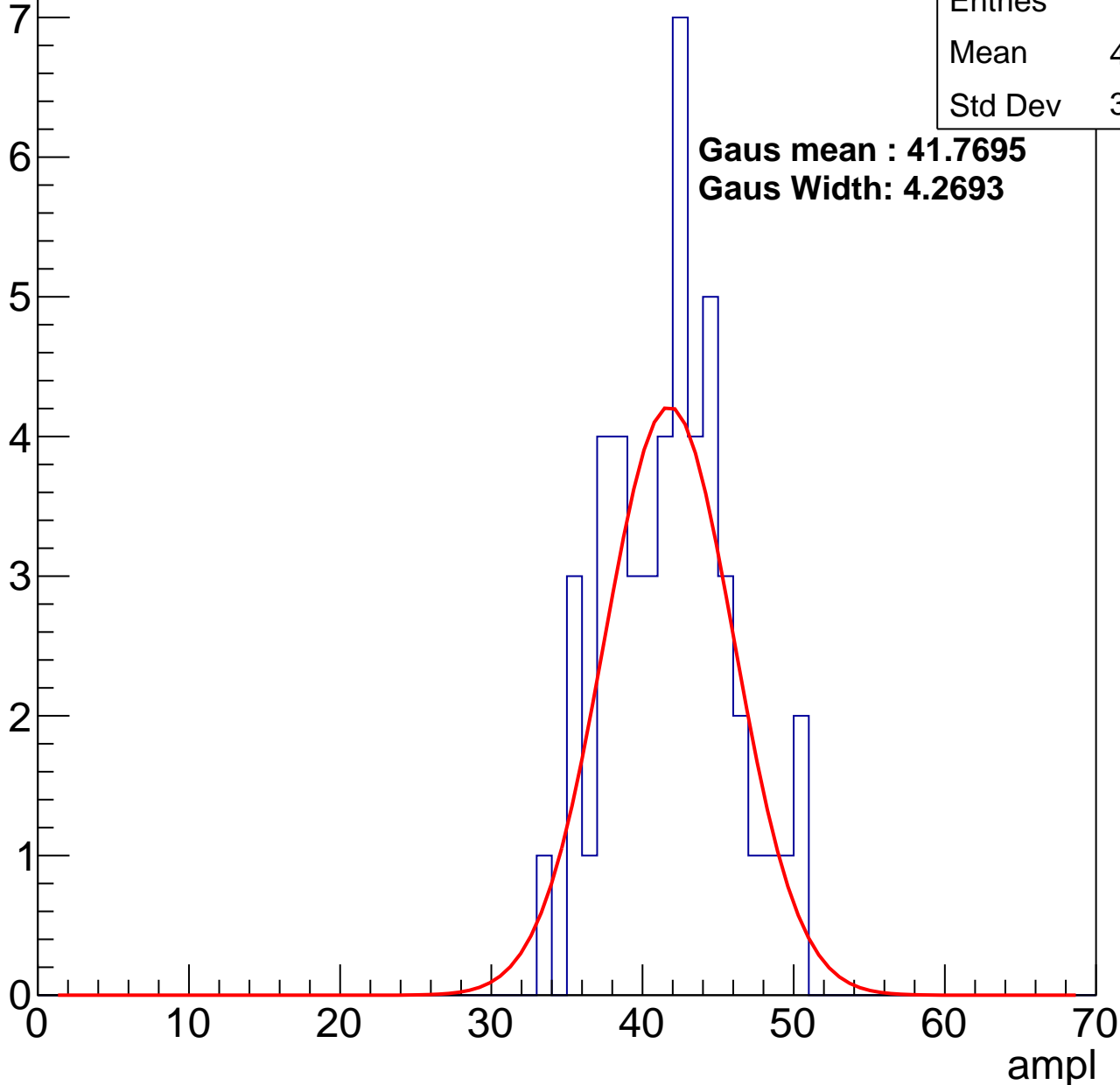
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	41.47
Std Dev	3.985

**Gaus mean : 41.7695**

**Gaus Width: 4.2693**

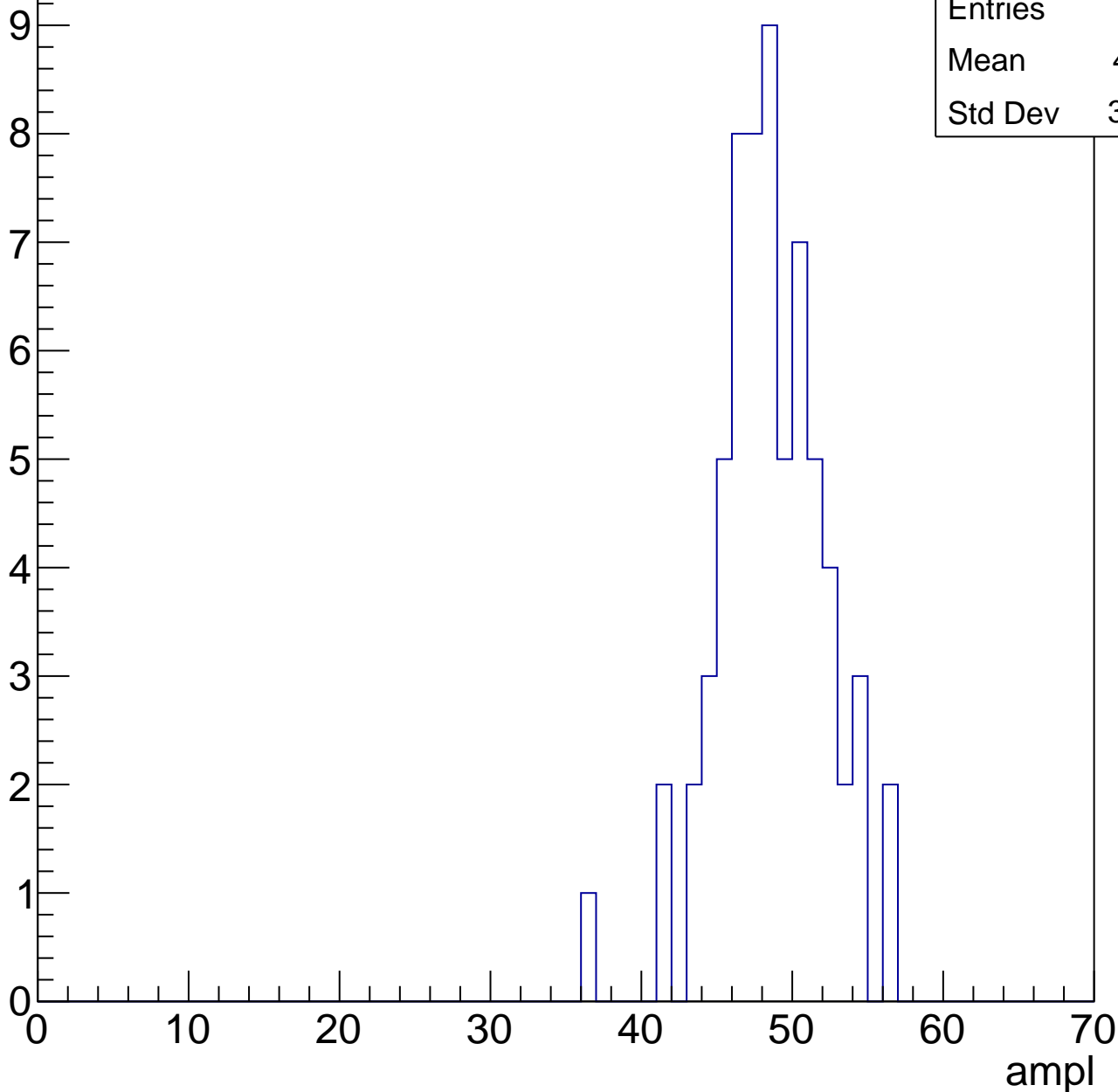


# B1L102S, U5-ch89, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	48.11
Std Dev	3.593

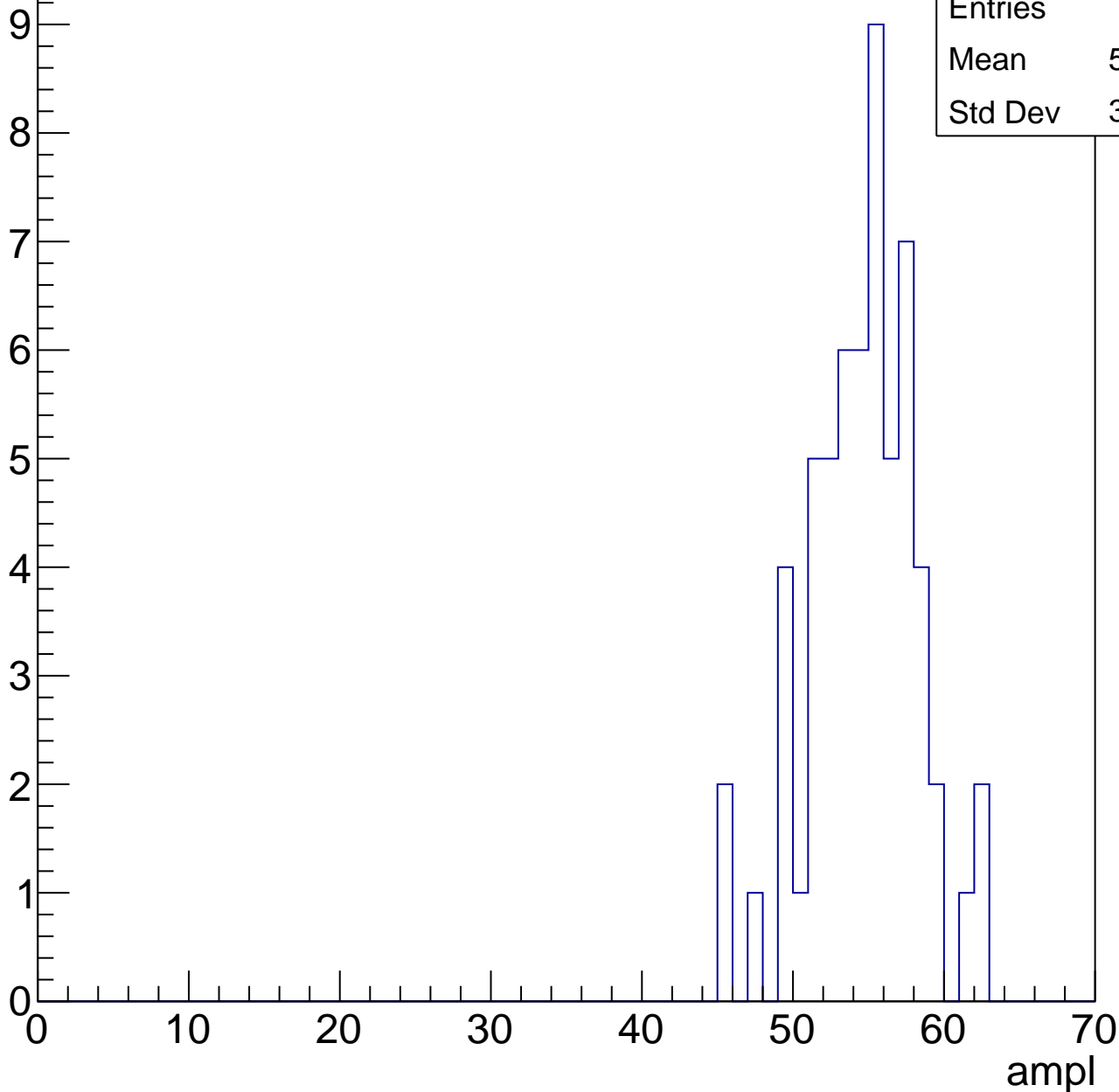


# B1L102S, U5-ch89, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	54.15
Std Dev	3.605

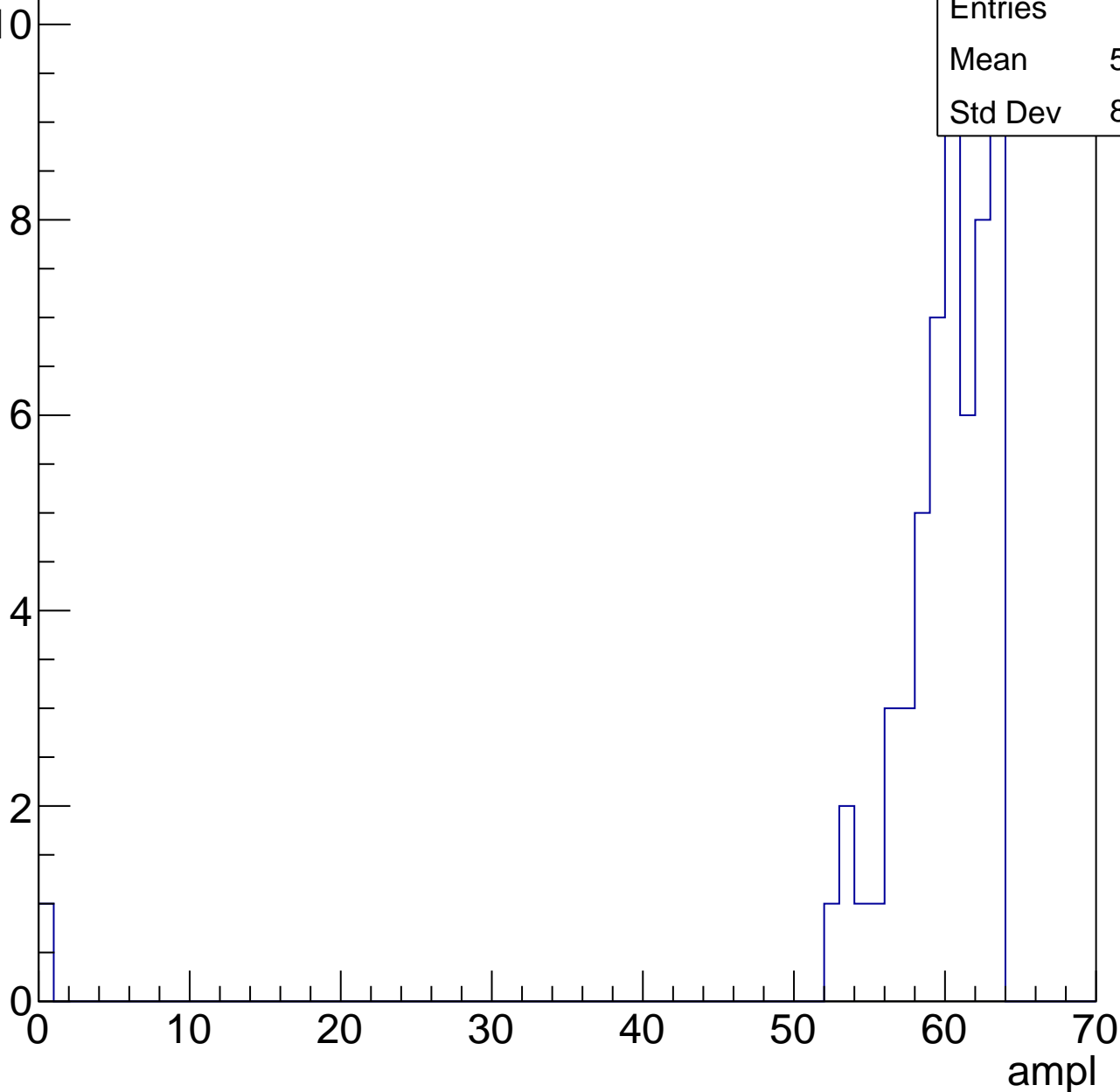


# B1L102S, U5-ch89, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

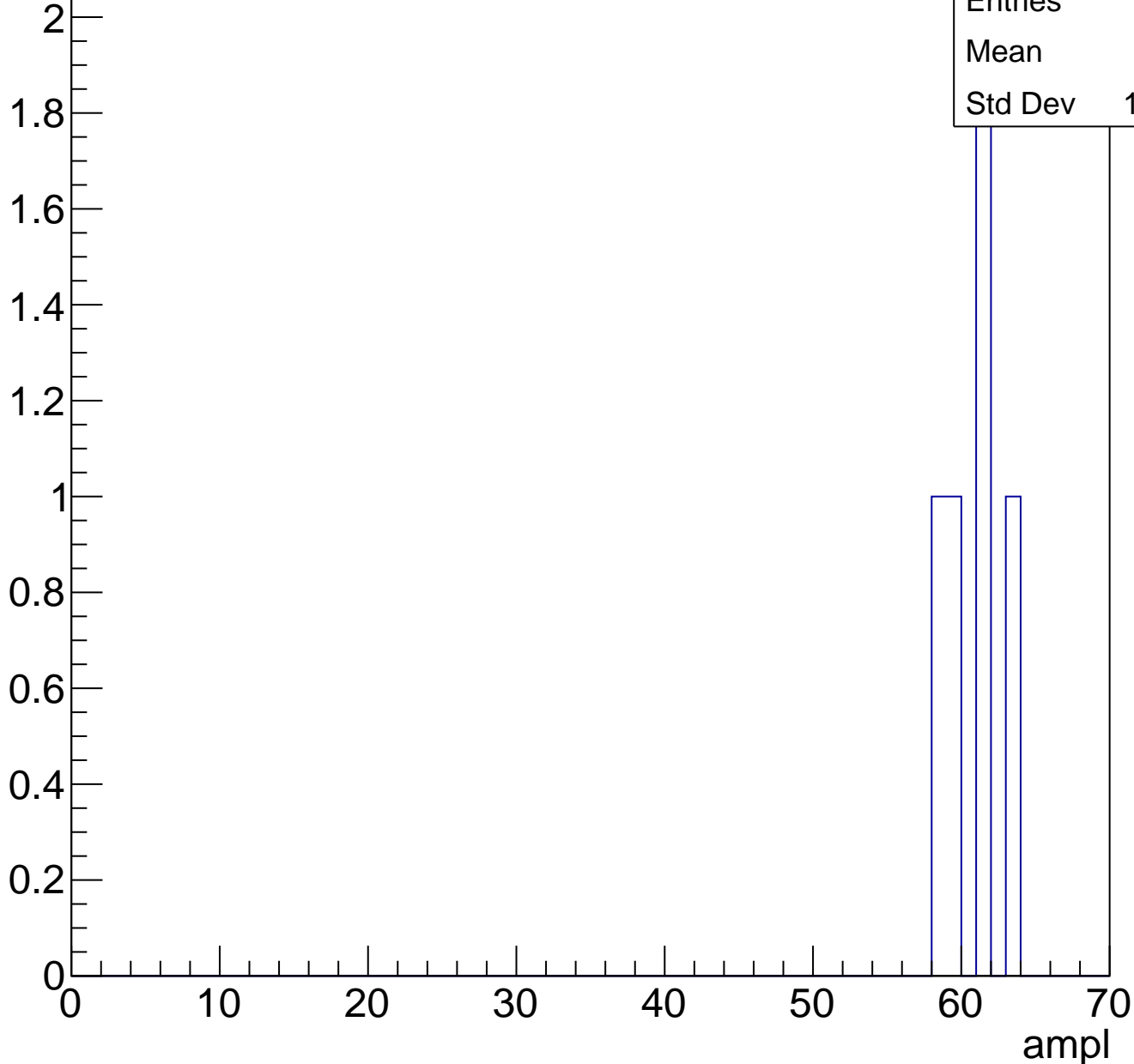
Entries	57
Mean	58.56
Std Dev	8.299



# B1L102S, U5-ch89, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U5-ch89, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	37.5
Std Dev	23.5

ampl

# B1L102S, U5-ch90, adc0

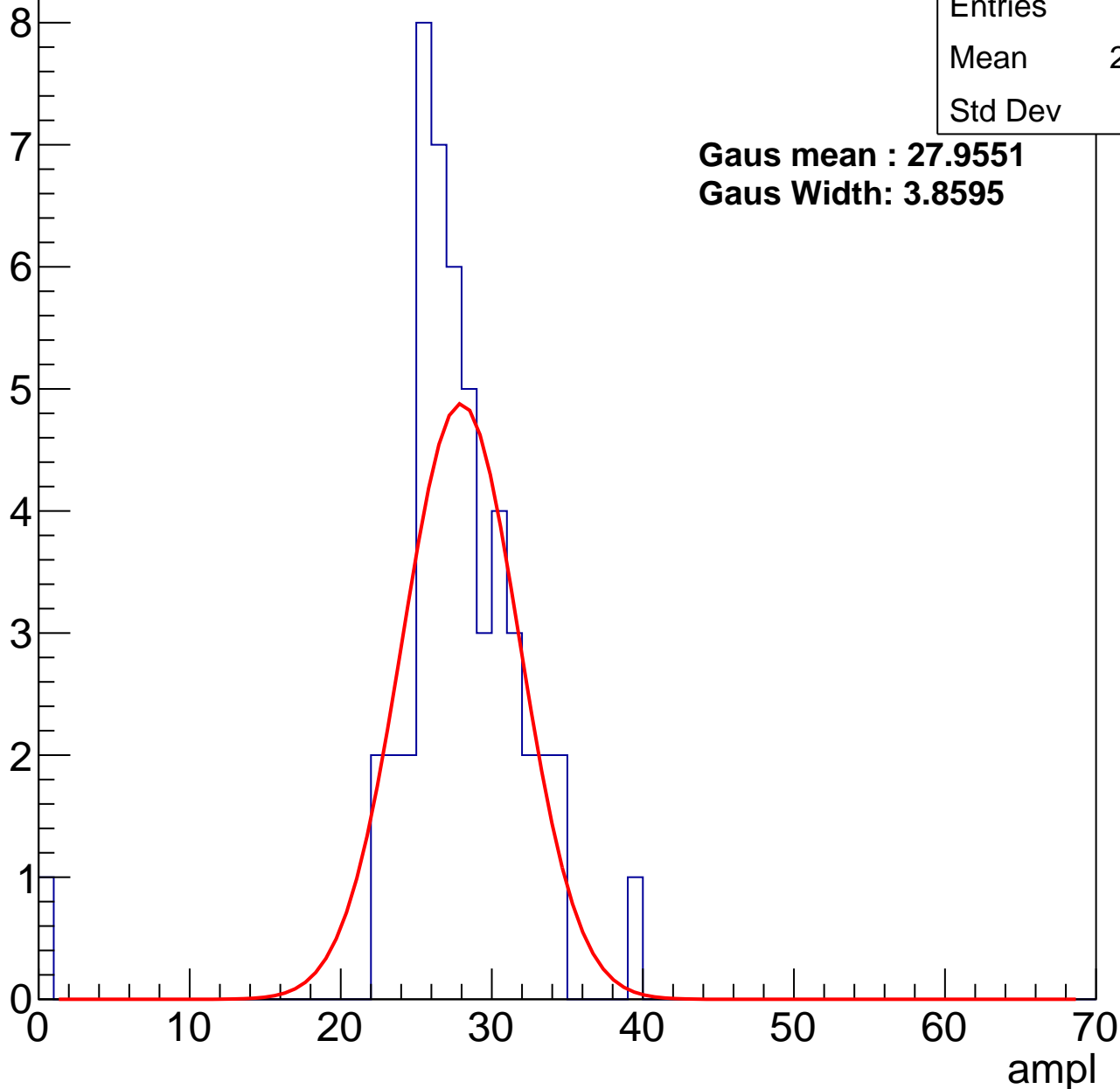
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	27.18
Std Dev	5.16

**Gaus mean : 27.9551**

**Gaus Width: 3.8595**



# B1L102S, U5-ch90, adc1

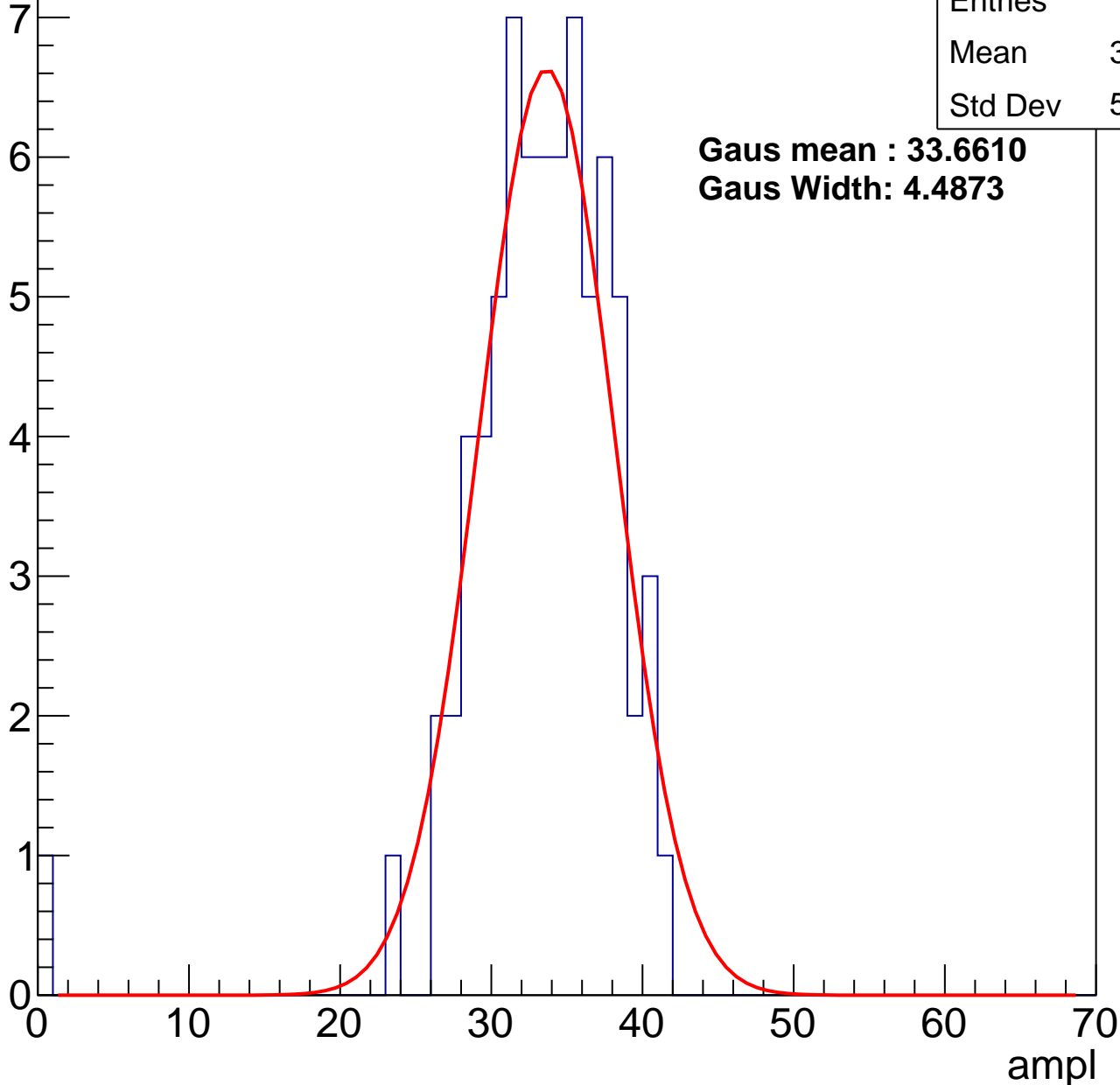
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	32.79
Std Dev	5.467

**Gaus mean : 33.6610**

**Gaus Width: 4.4873**



# B1L102S, U5-ch90, adc2

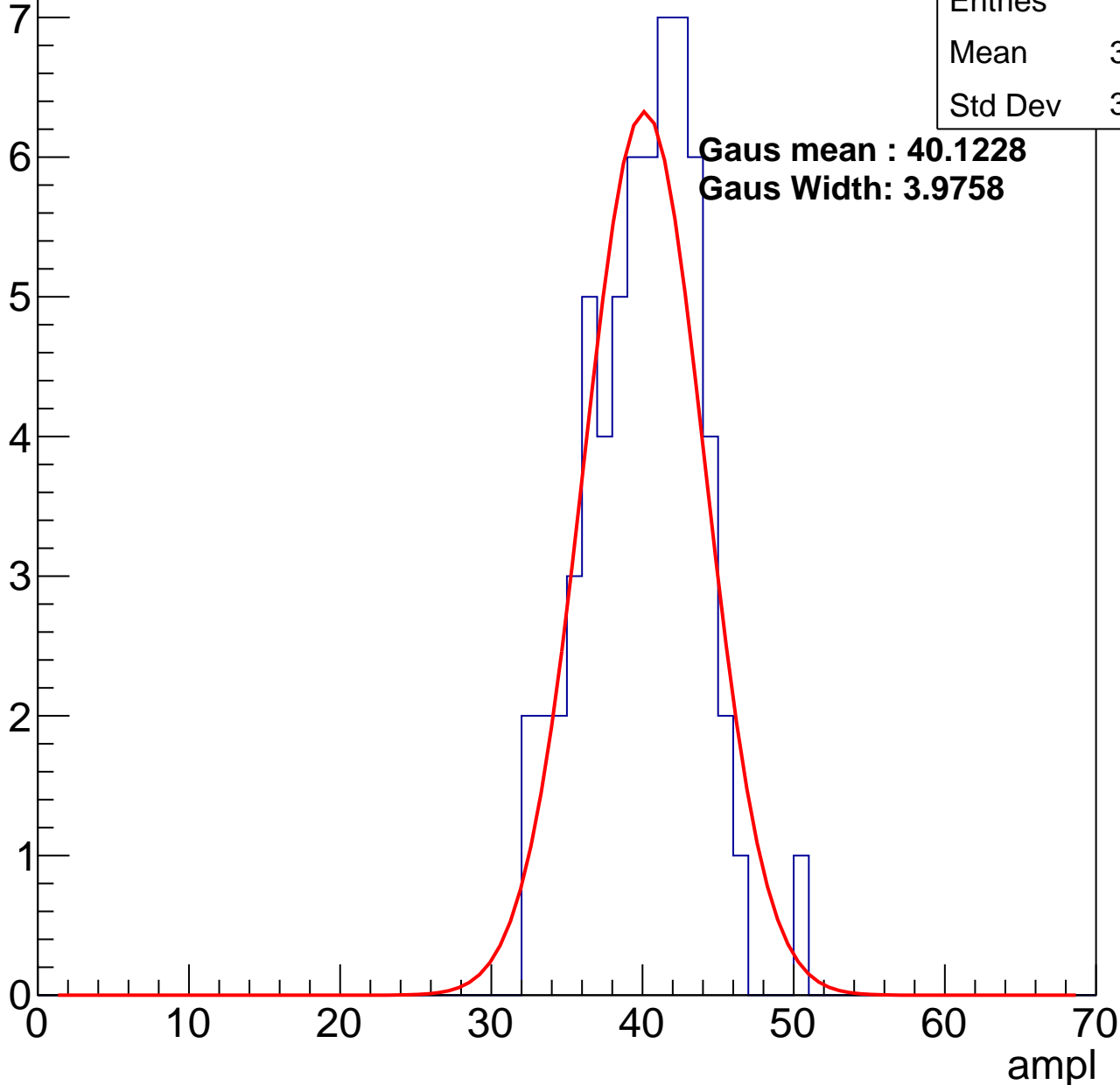
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	39.62
Std Dev	3.662

**Gaus mean : 40.1228**

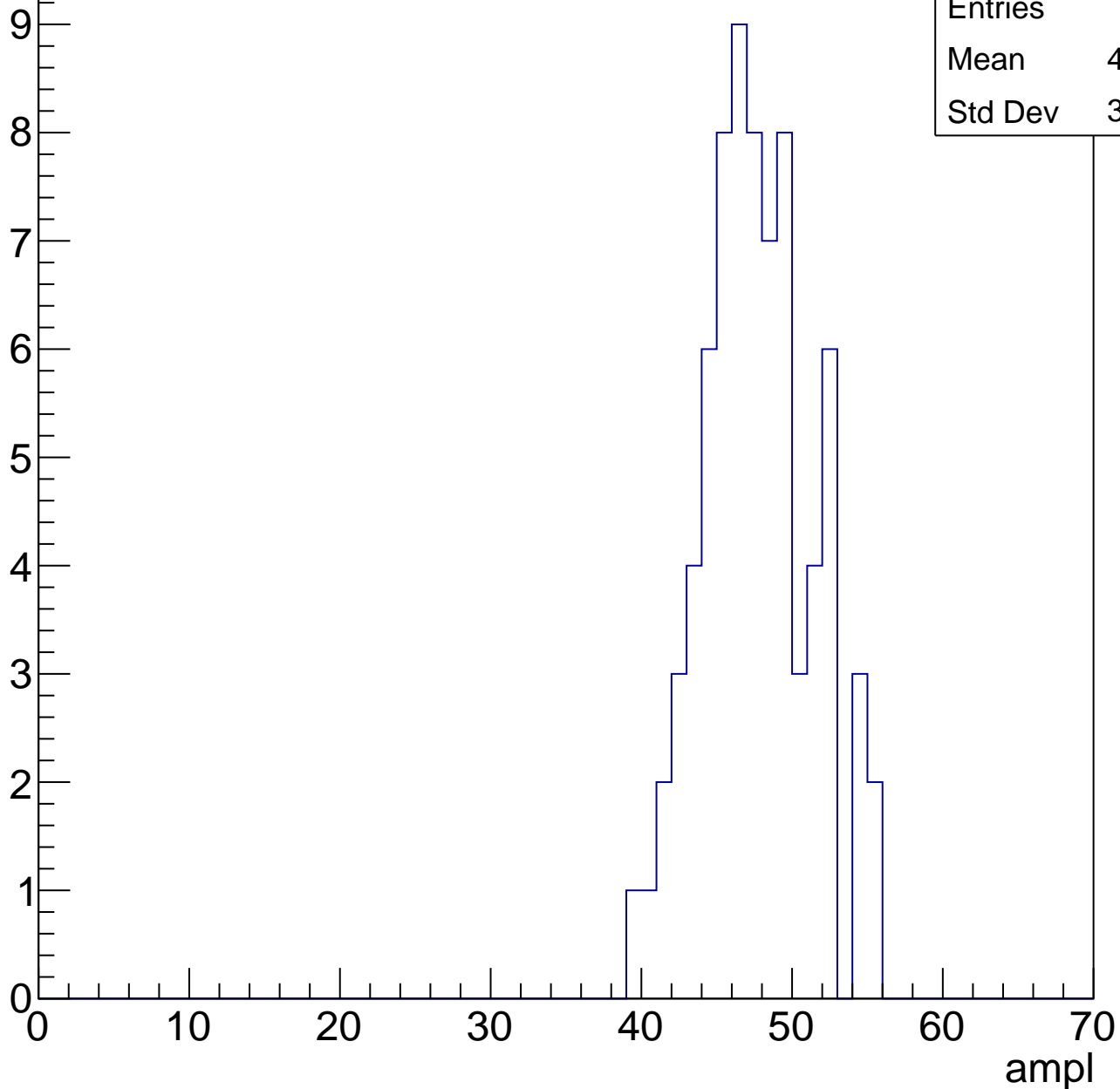
**Gaus Width: 3.9758**



# B1L102S, U5-ch90, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



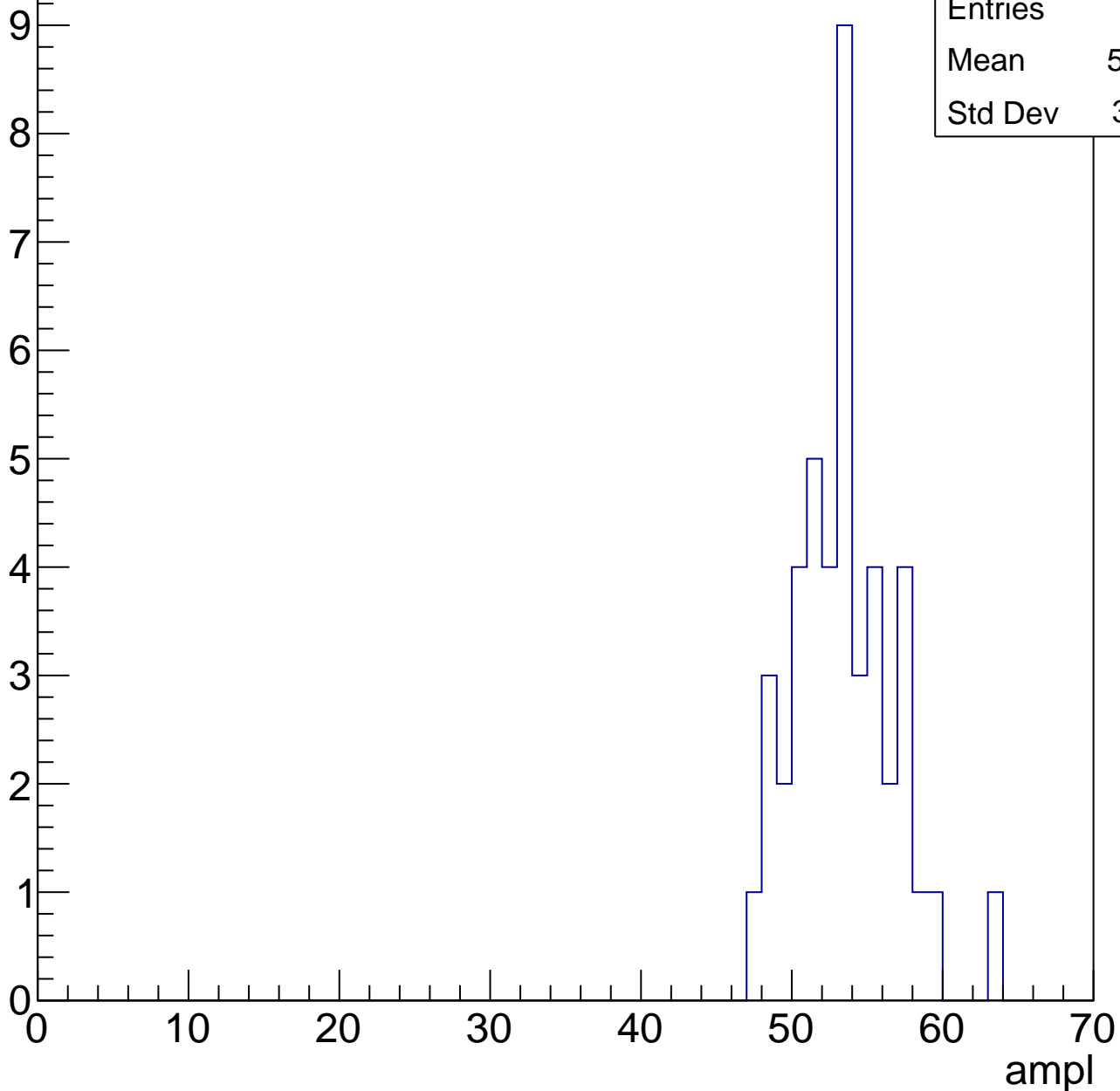
Entries	75
Mean	47.19
Std Dev	3.599

# B1L102S, U5-ch90, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	44
Mean	52.98
Std Dev	3.251

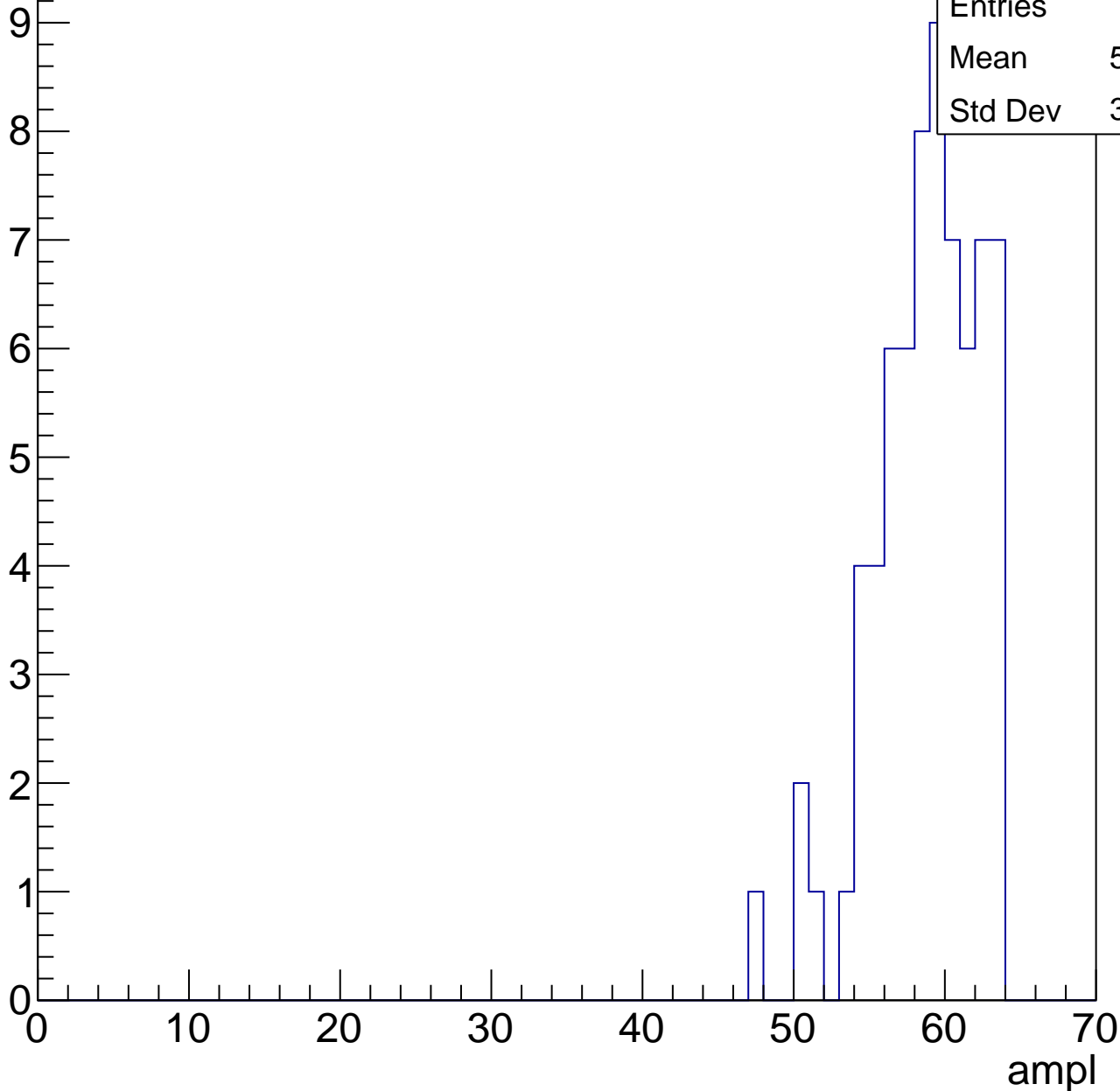


# B1L102S, U5-ch90, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

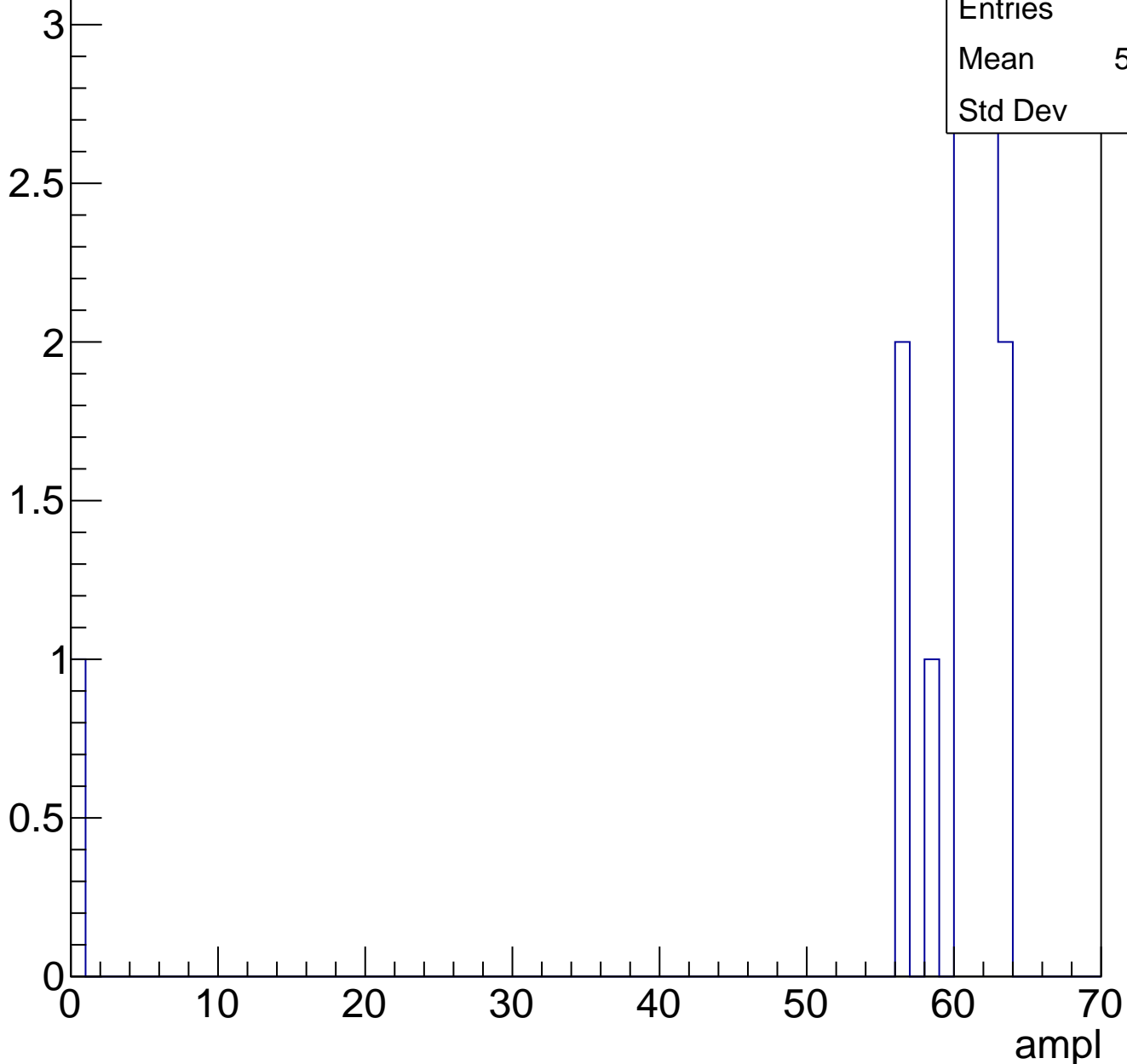
Entries	69
Mean	58.28
Std Dev	3.459



# B1L102S, U5-ch90, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

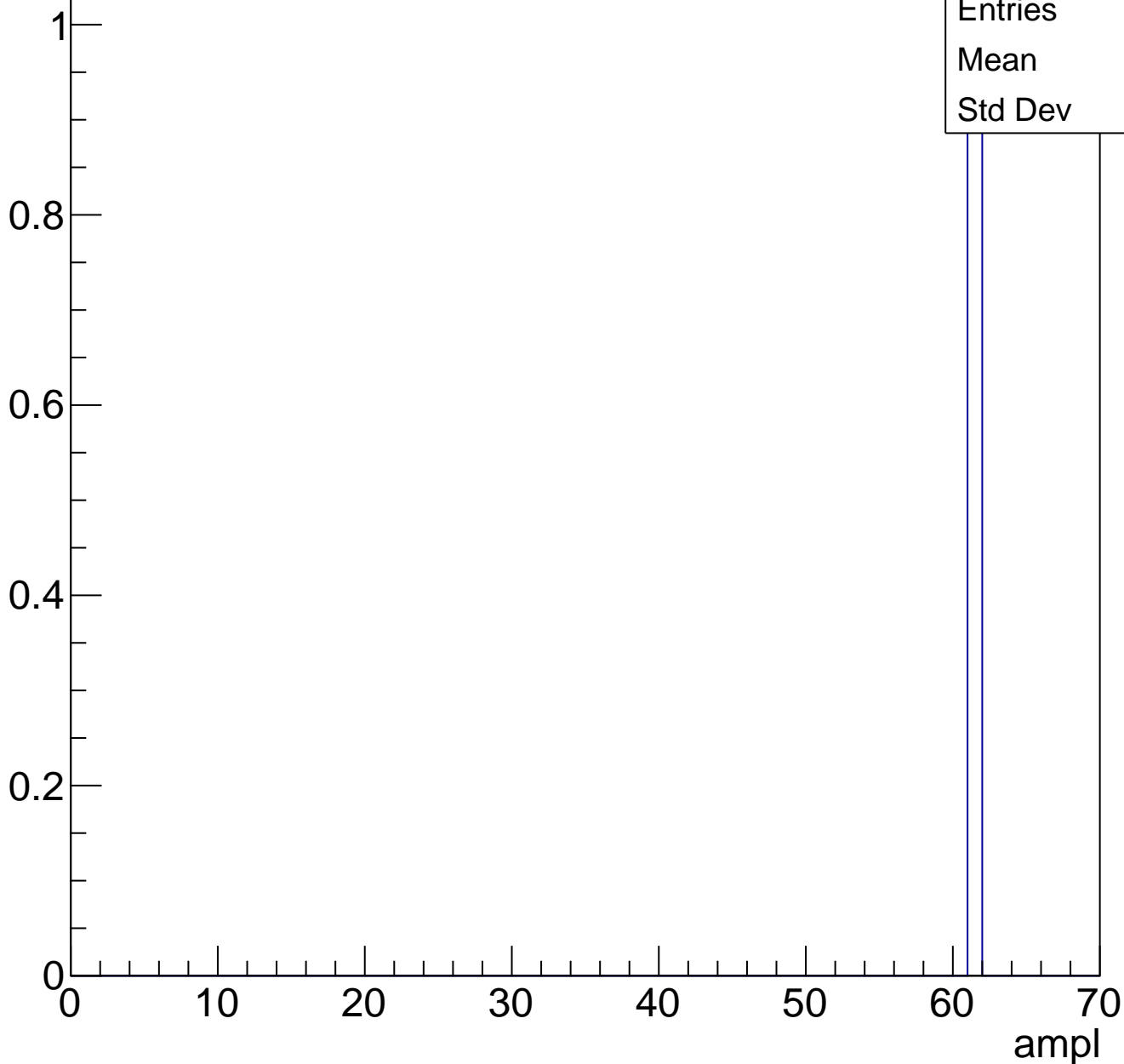




# B1L102S, U5-ch90, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U5-ch91, adc0

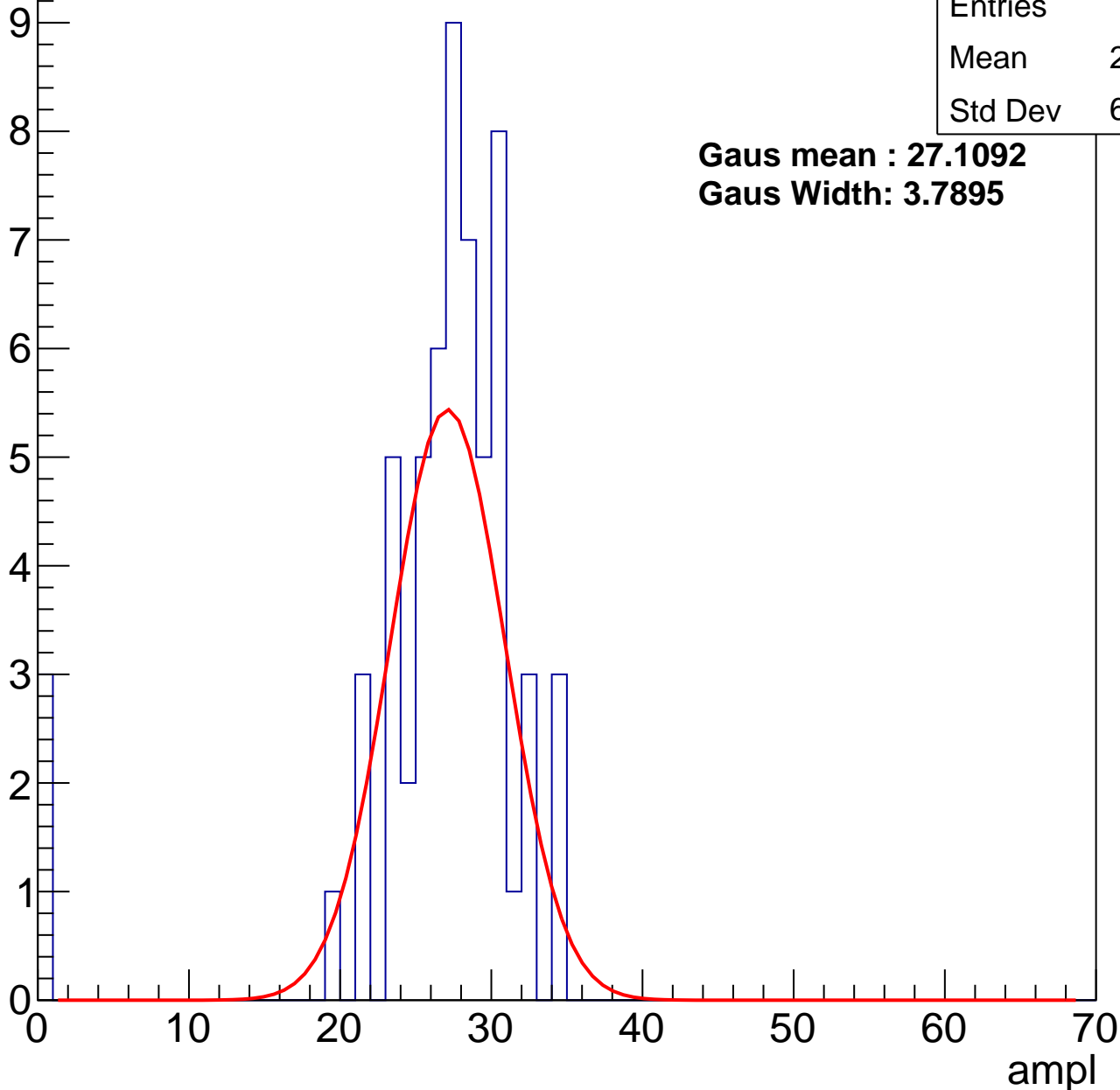
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	25.89
Std Dev	6.707

**Gaus mean : 27.1092**

**Gaus Width: 3.7895**



# B1L102S, U5-ch91, adc1

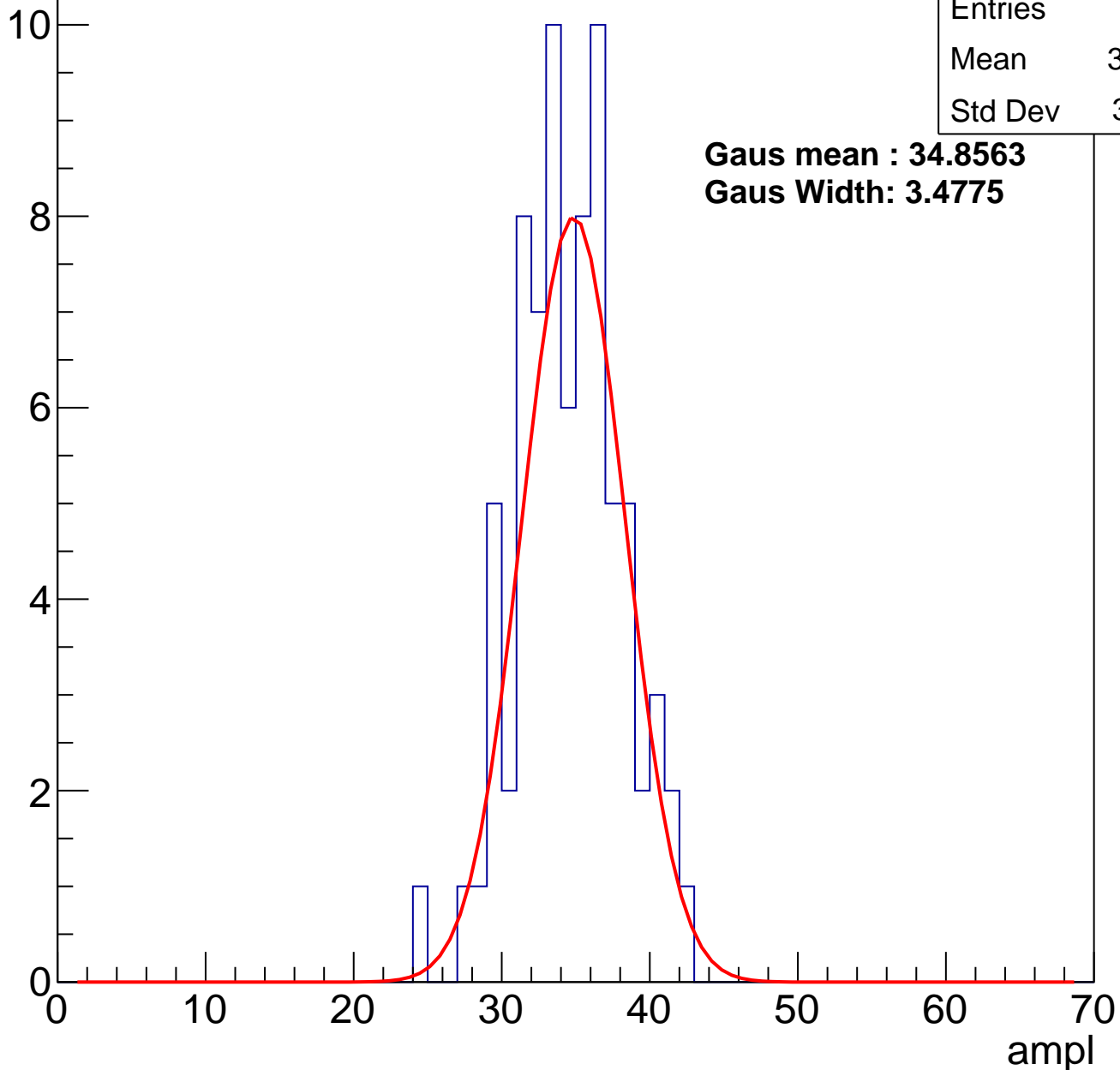
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	77
Mean	34.12
Std Dev	3.501

**Gaus mean : 34.8563**

**Gaus Width: 3.4775**

Entry



# B1L102S, U5-ch91, adc2

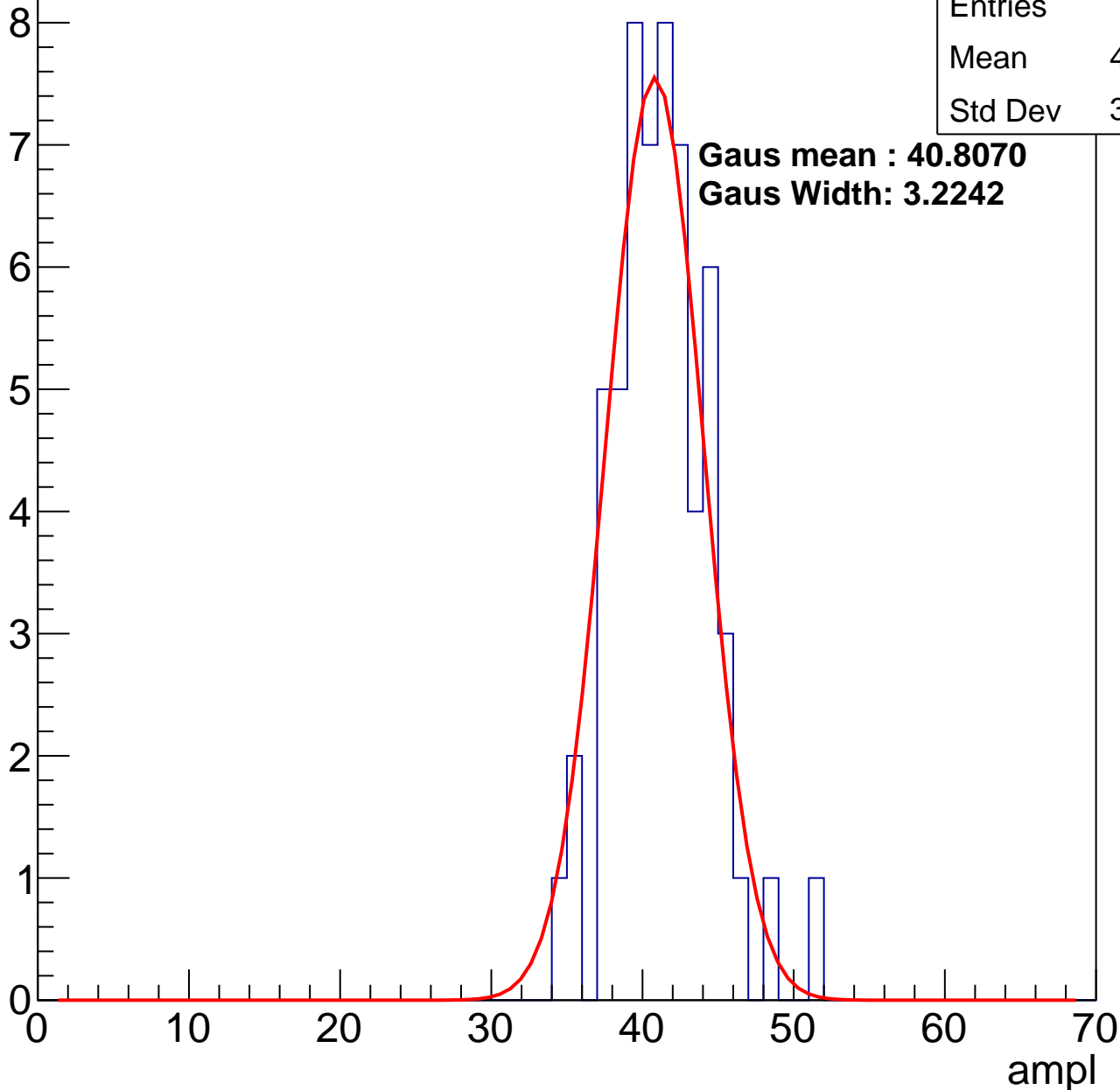
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	40.83
Std Dev	3.142

**Gaus mean : 40.8070**

**Gaus Width: 3.2242**

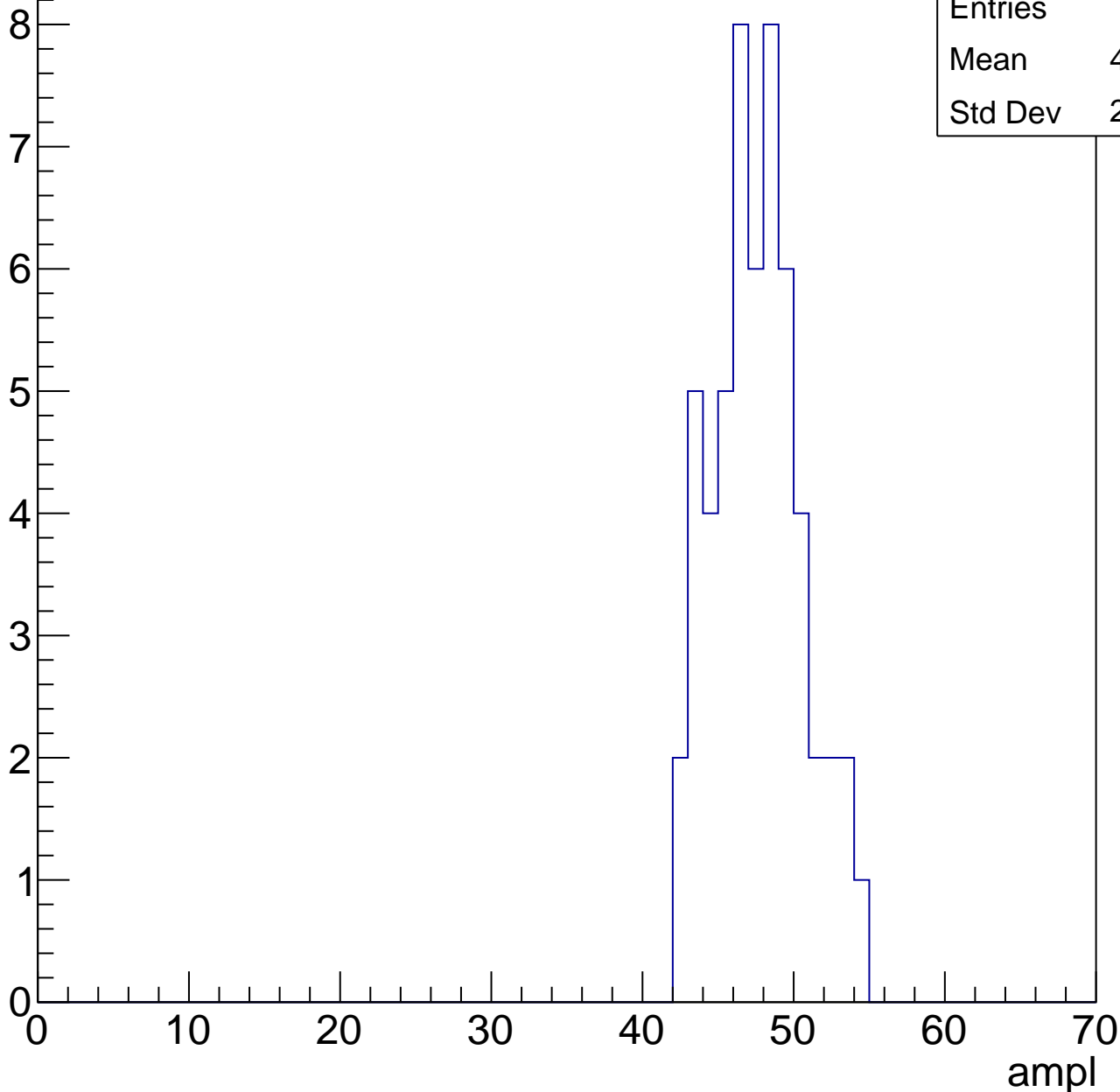


# B1L102S, U5-ch91, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

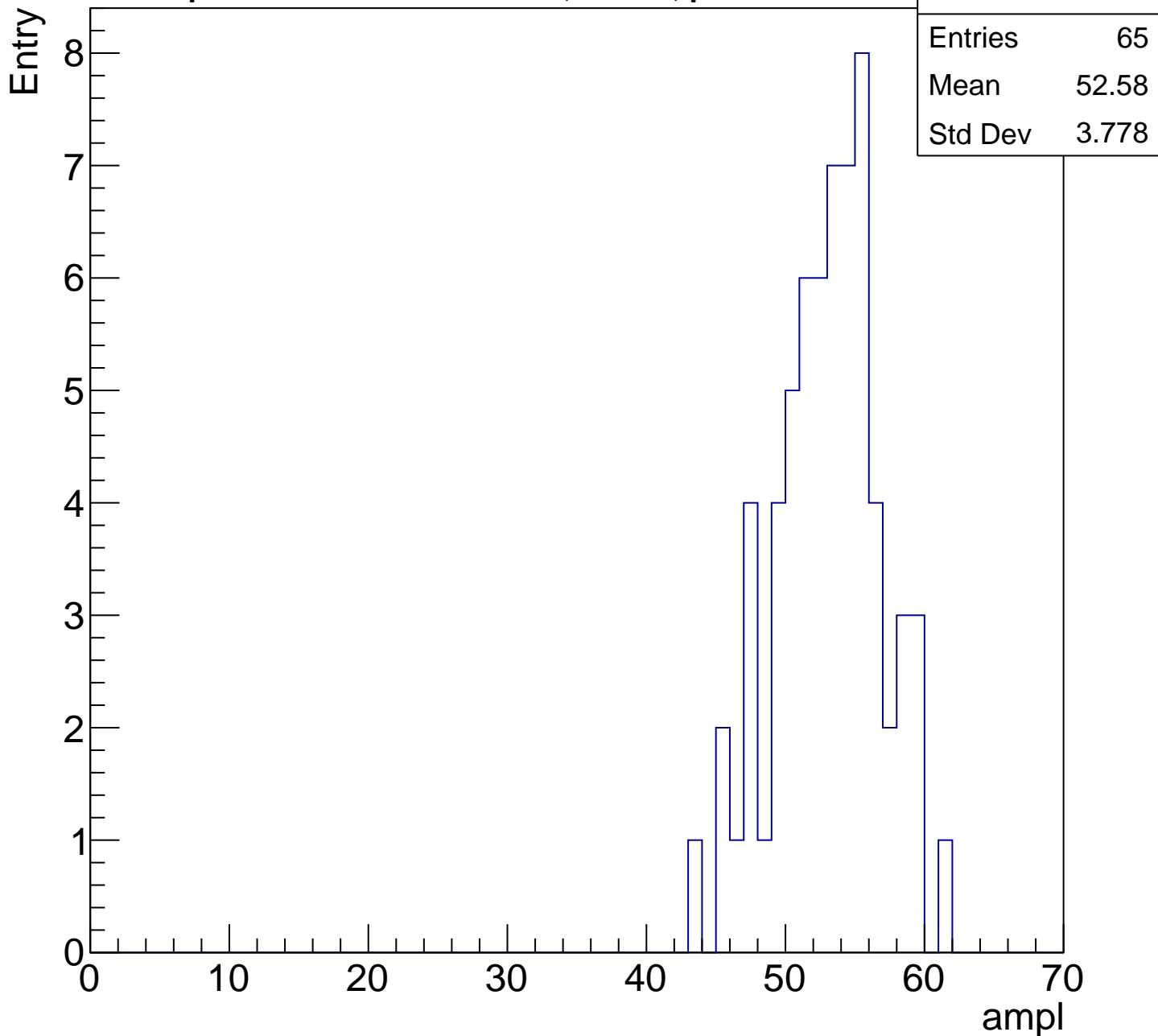
Entry

Entries	55
Mean	47.16
Std Dev	2.903



# B1L102S, U5-ch91, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

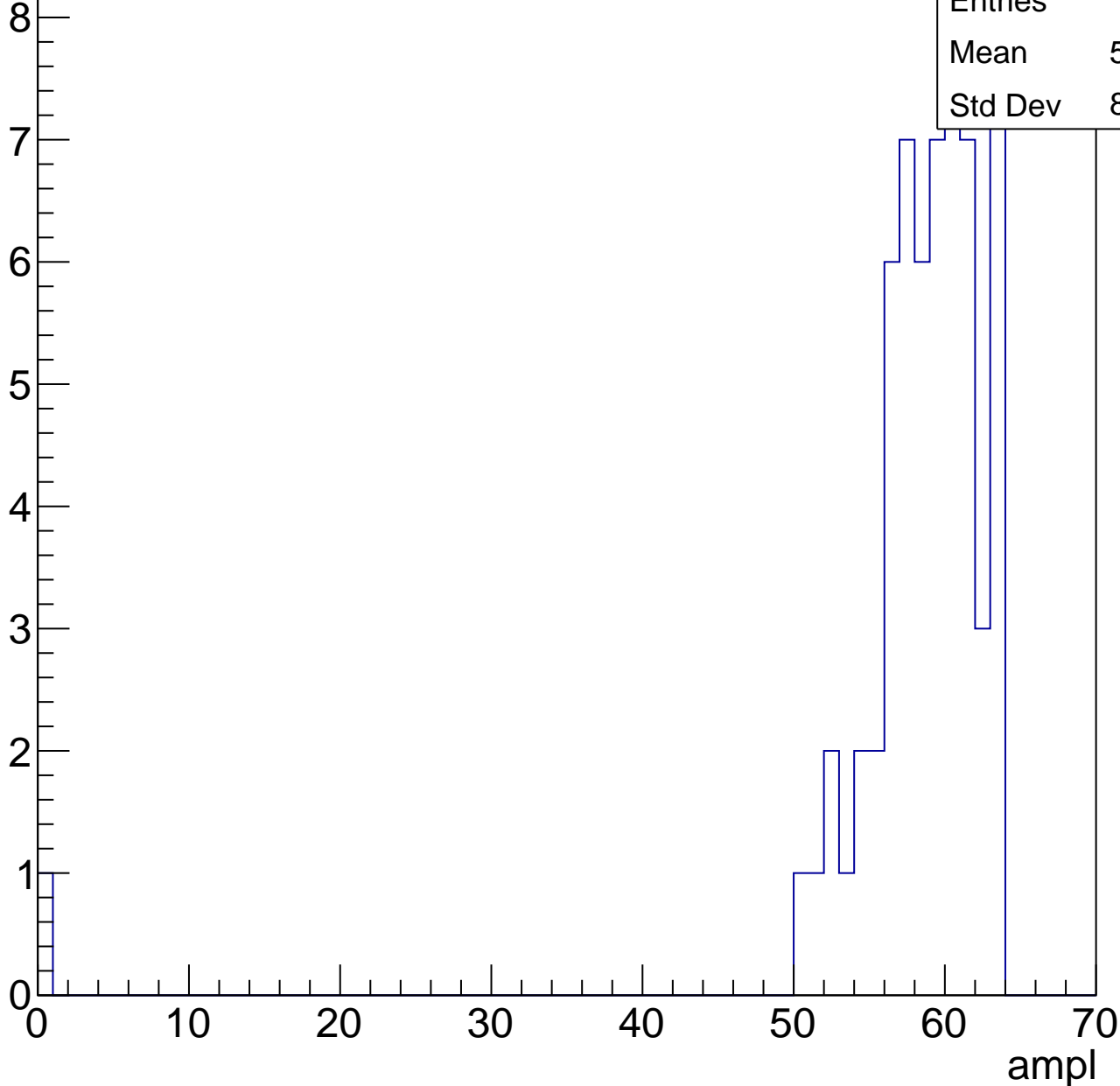


# B1L102S, U5-ch91, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	57.56
Std Dev	8.025

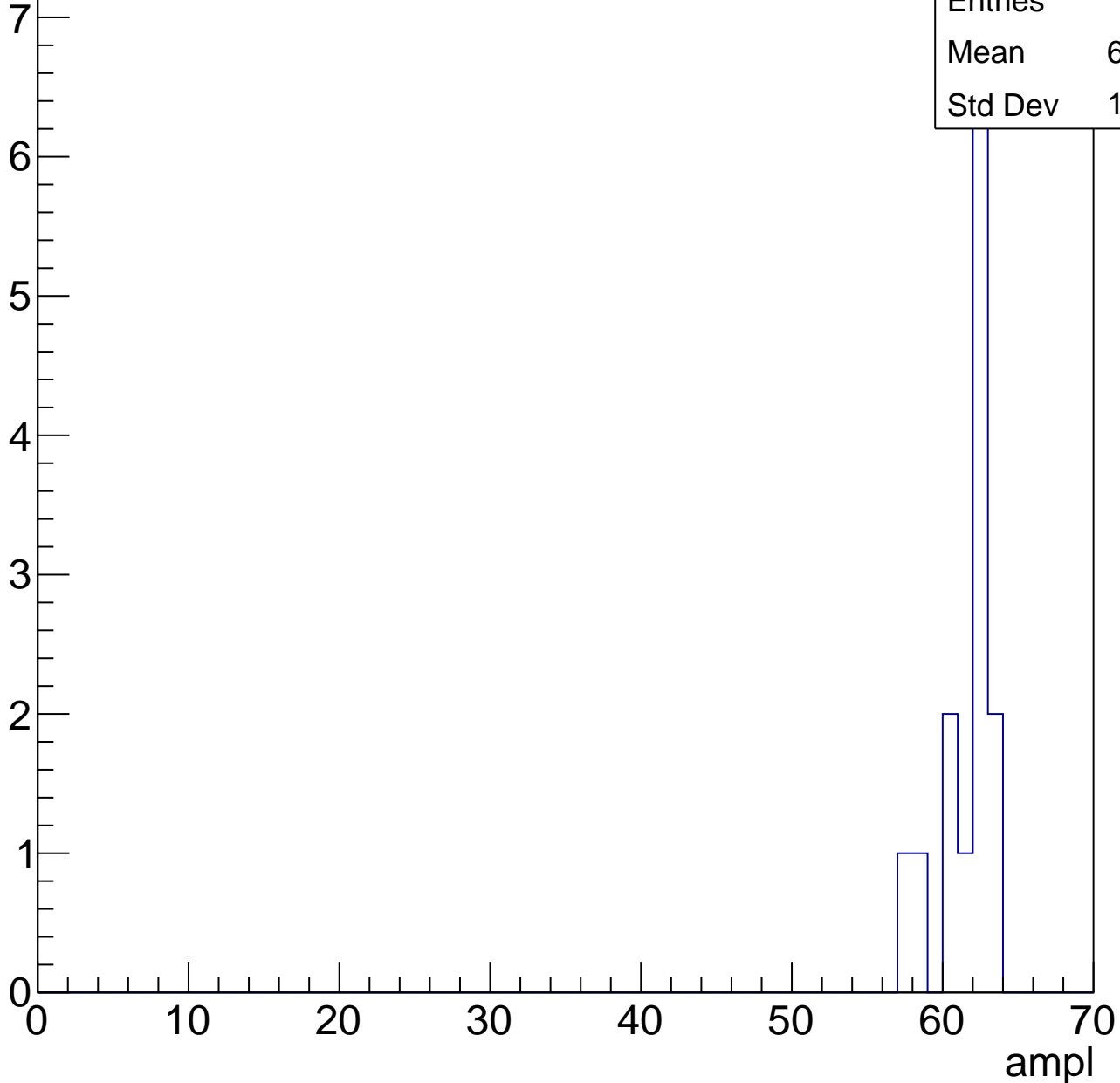


# B1L102S, U5-ch91, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	14
Mean	61.14
Std Dev	1.726





# B1L102S, U5-ch91, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U5-ch92, adc0

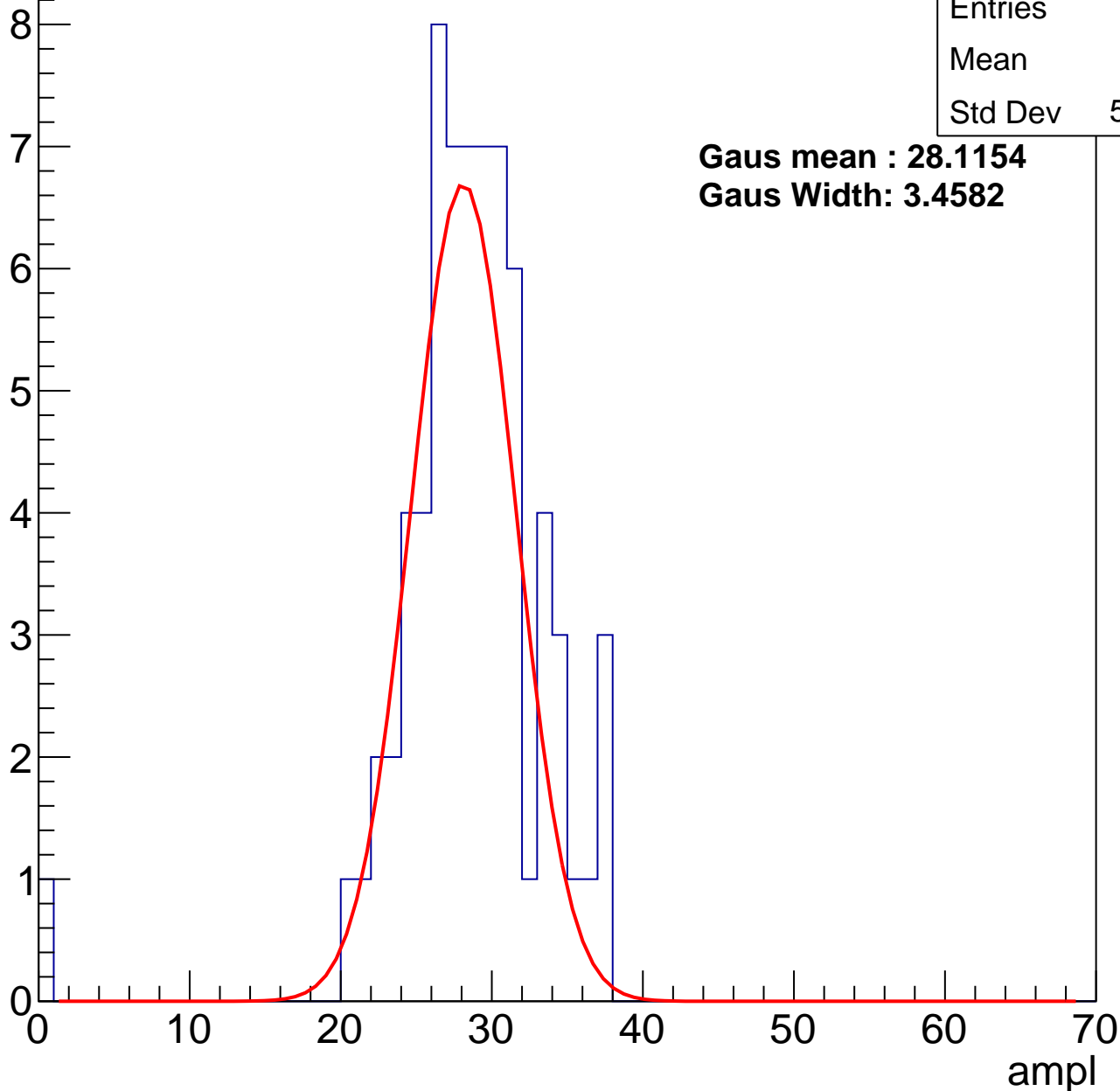
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	28.1
Std Dev	5.108

**Gaus mean : 28.1154**

**Gaus Width: 3.4582**



# B1L102S, U5-ch92, adc1

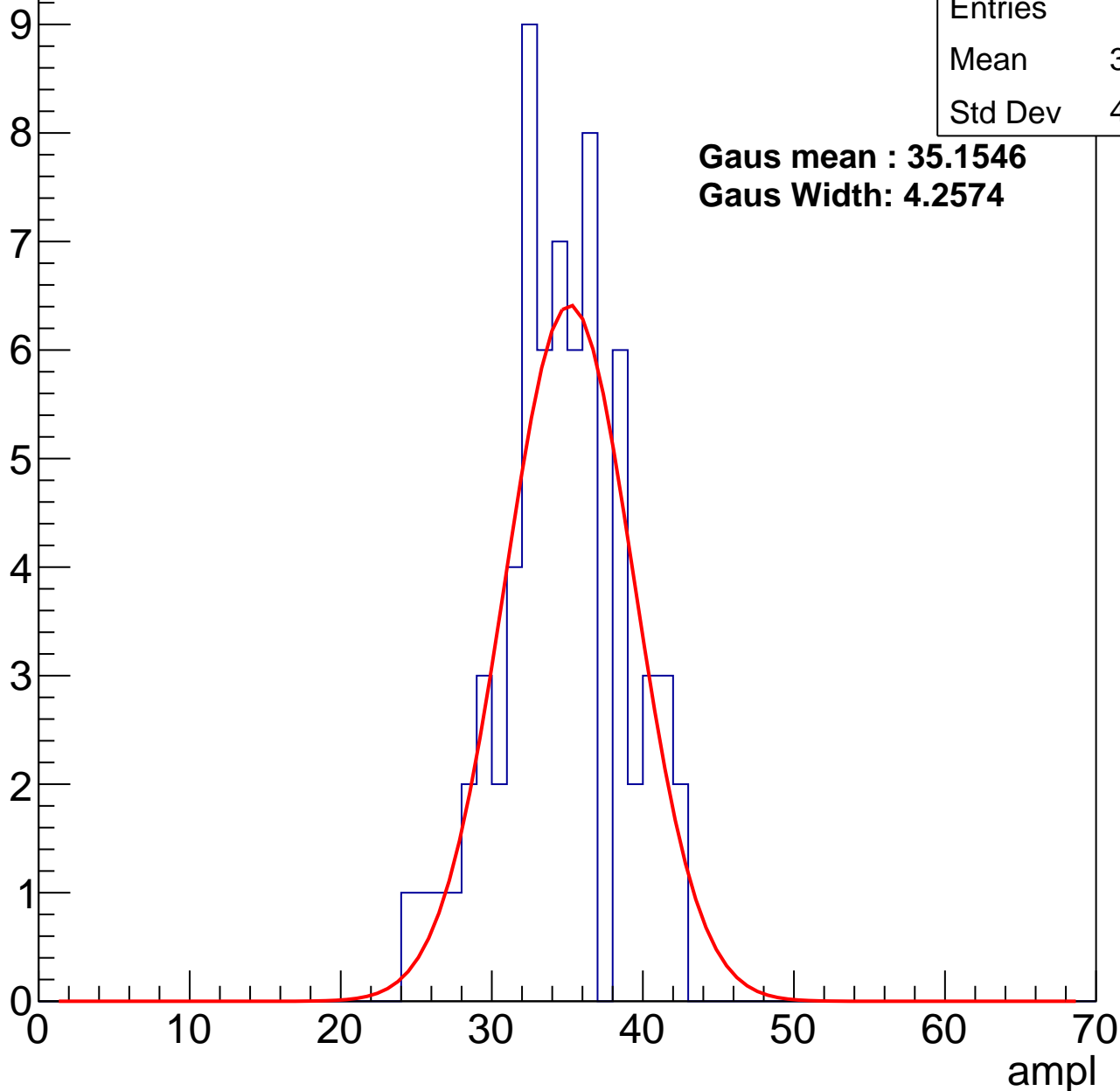
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	34.09
Std Dev	4.084

**Gaus mean : 35.1546**

**Gaus Width: 4.2574**



# B1L102S, U5-ch92, adc2

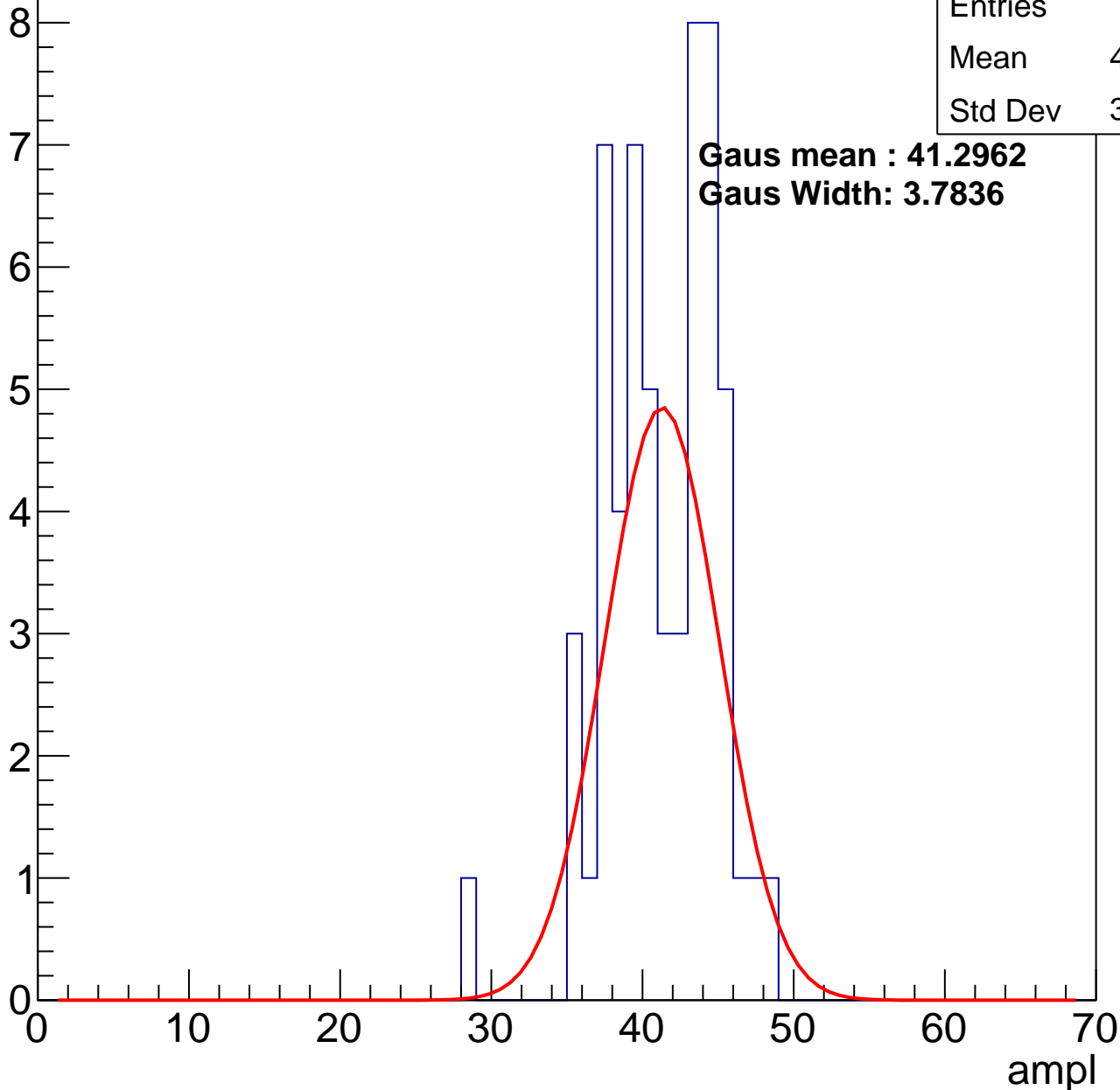
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	40.76
Std Dev	3.659

**Gaus mean : 41.2962**

**Gaus Width: 3.7836**

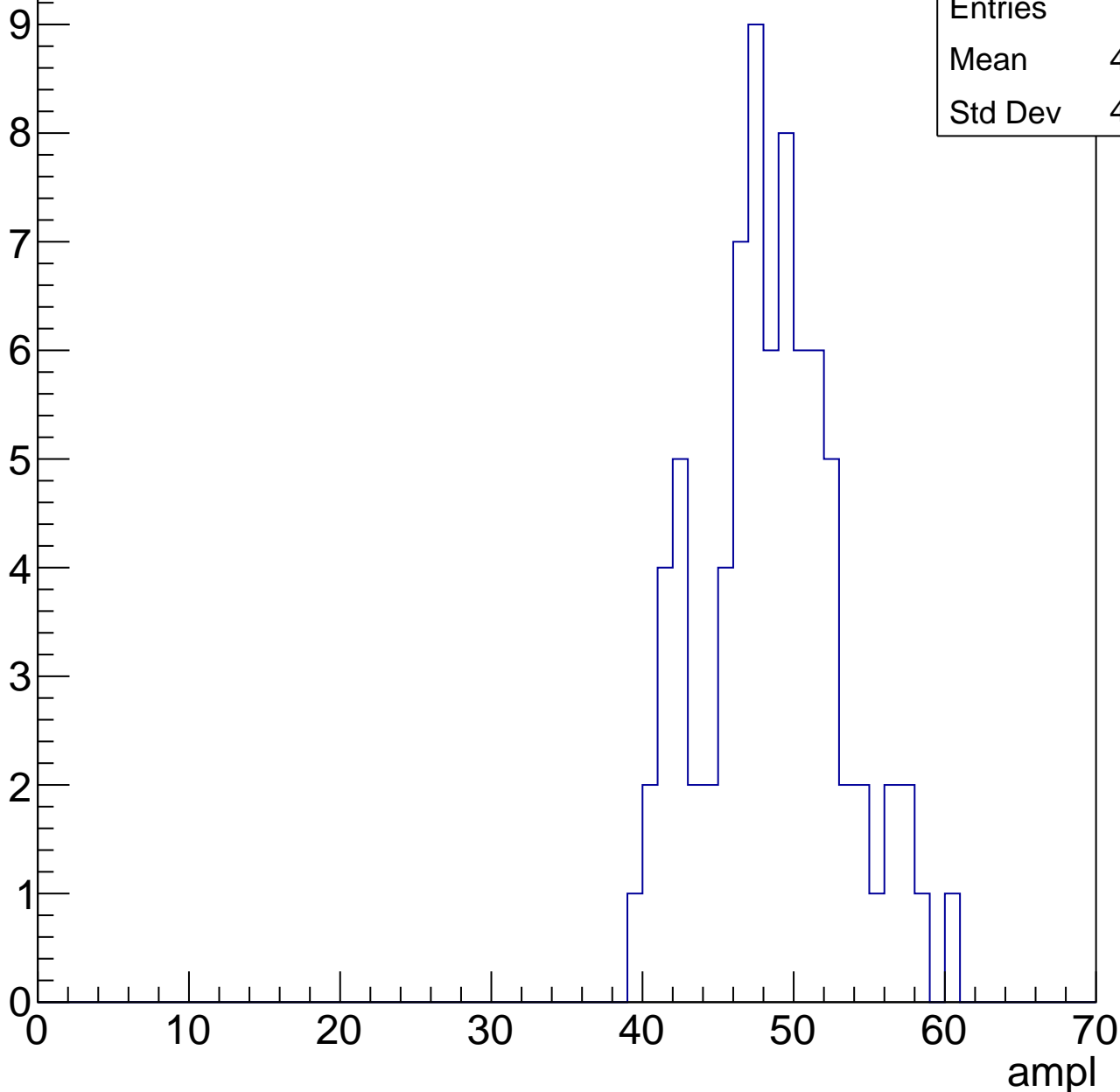


# B1L102S, U5-ch92, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	78
Mean	48.09
Std Dev	4.544

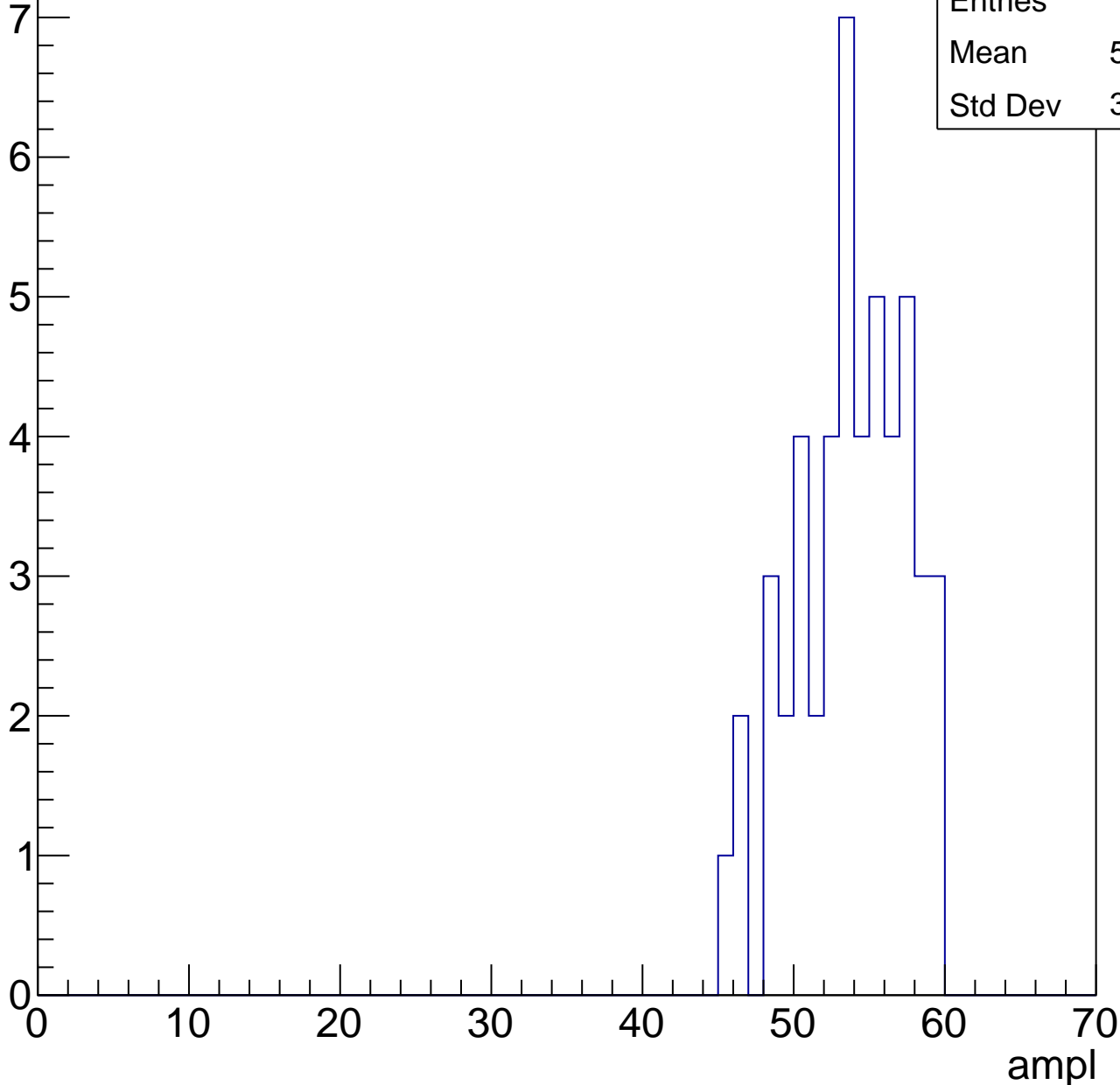


# B1L102S, U5-ch92, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	53.29
Std Dev	3.603

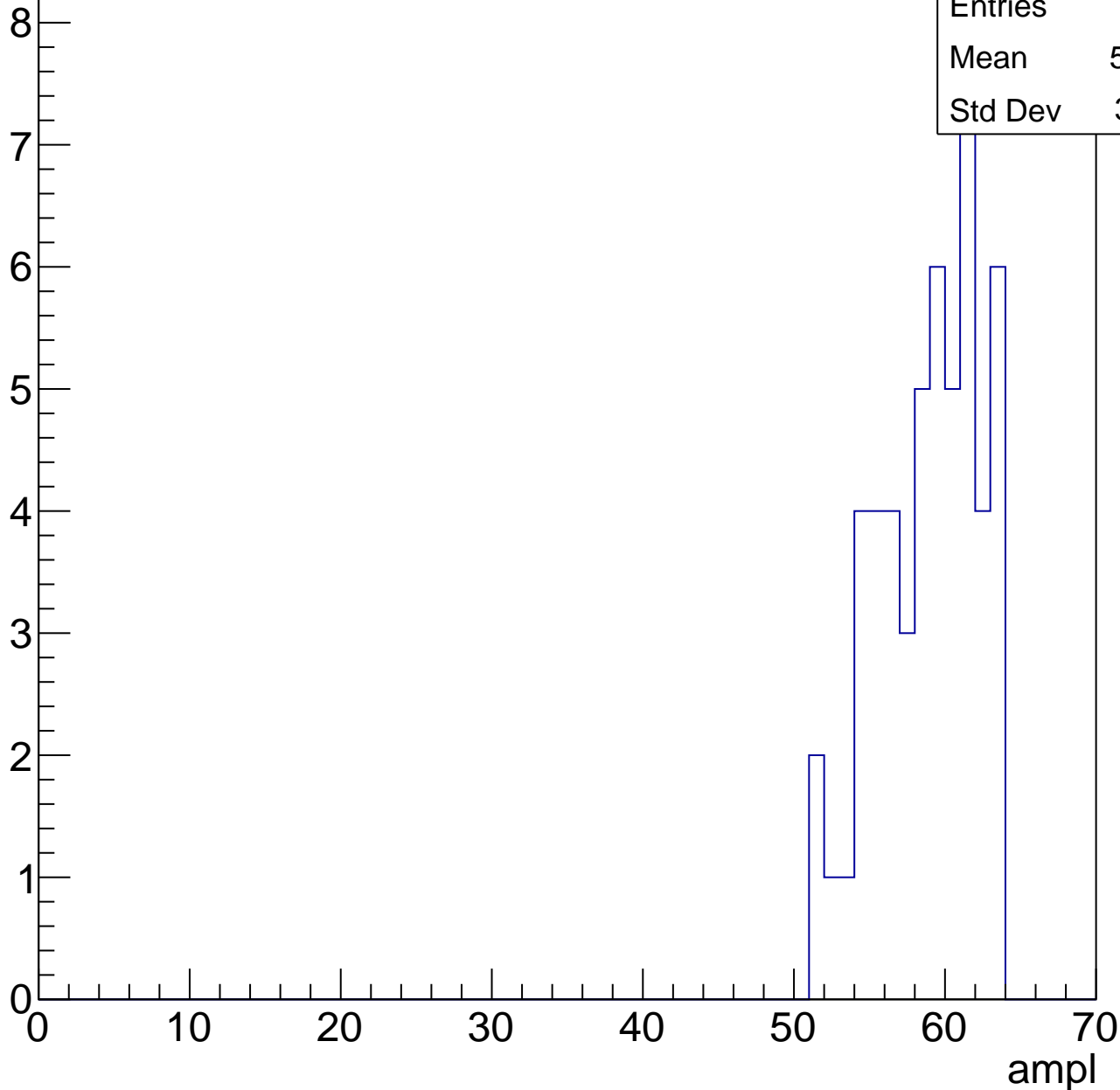


# B1L102S, U5-ch92, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	58.42
Std Dev	3.311

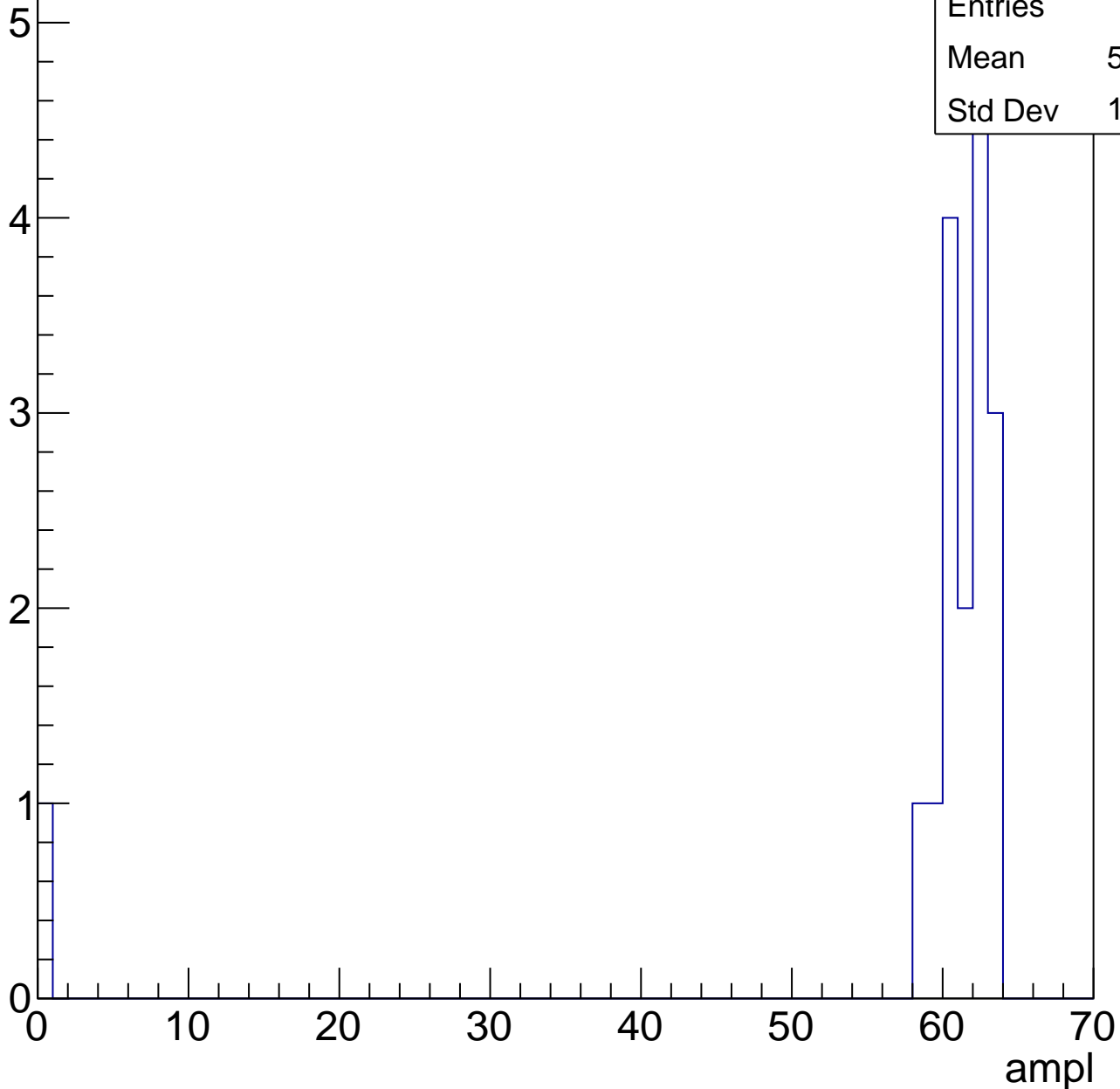


# B1L102S, U5-ch92, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	17
Mean	57.53
Std Dev	14.45





# B1L102S, U5-ch92, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U5-ch93, adc0

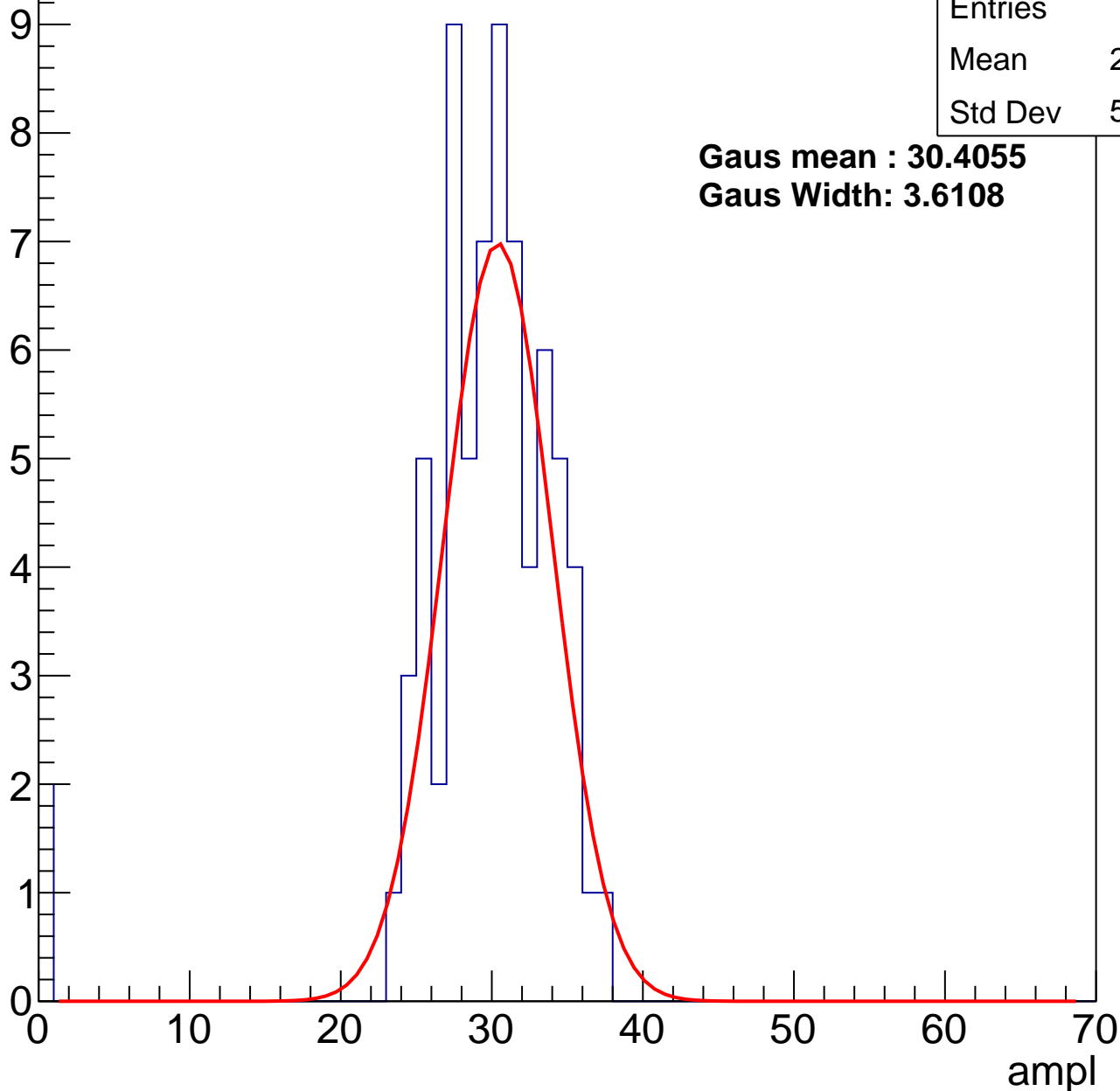
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	28.93
Std Dev	5.913

**Gaus mean : 30.4055**

**Gaus Width: 3.6108**



# B1L102S, U5-ch93, adc1

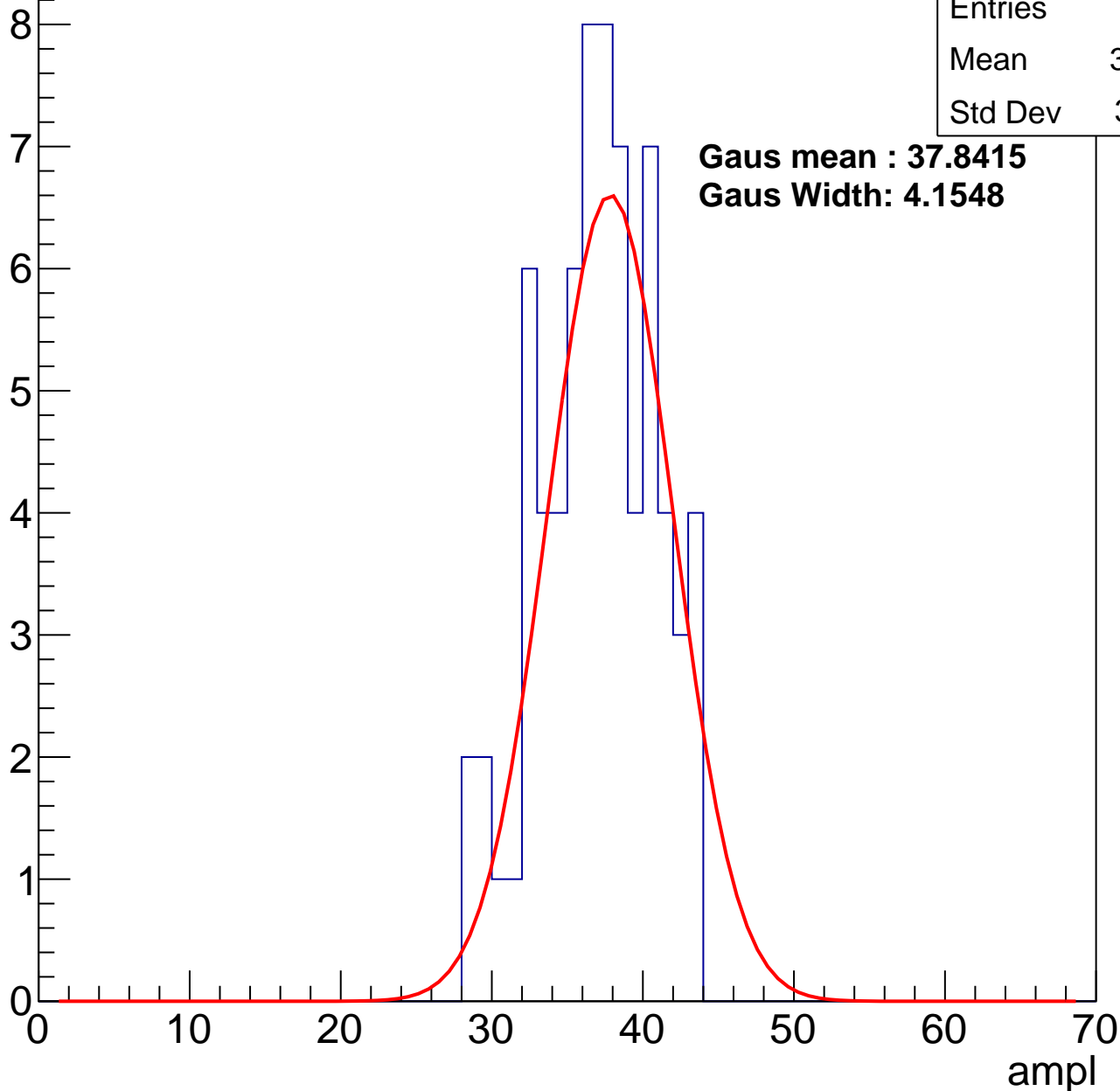
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	36.52
Std Dev	3.771

**Gaus mean : 37.8415**

**Gaus Width: 4.1548**



# B1L102S, U5-ch93, adc2

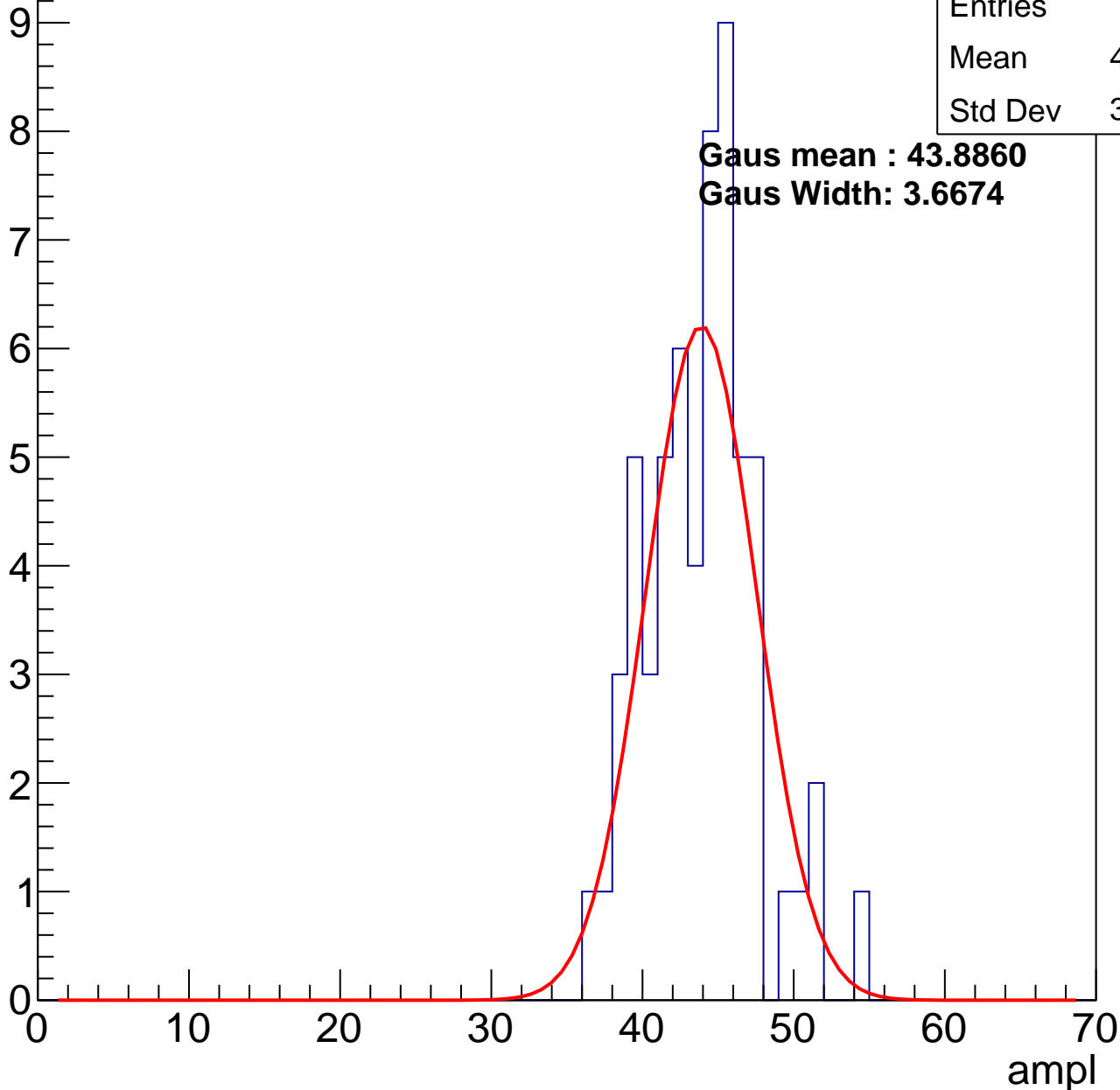
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	43.47
Std Dev	3.612

**Gaus mean : 43.8860**

**Gaus Width: 3.6674**

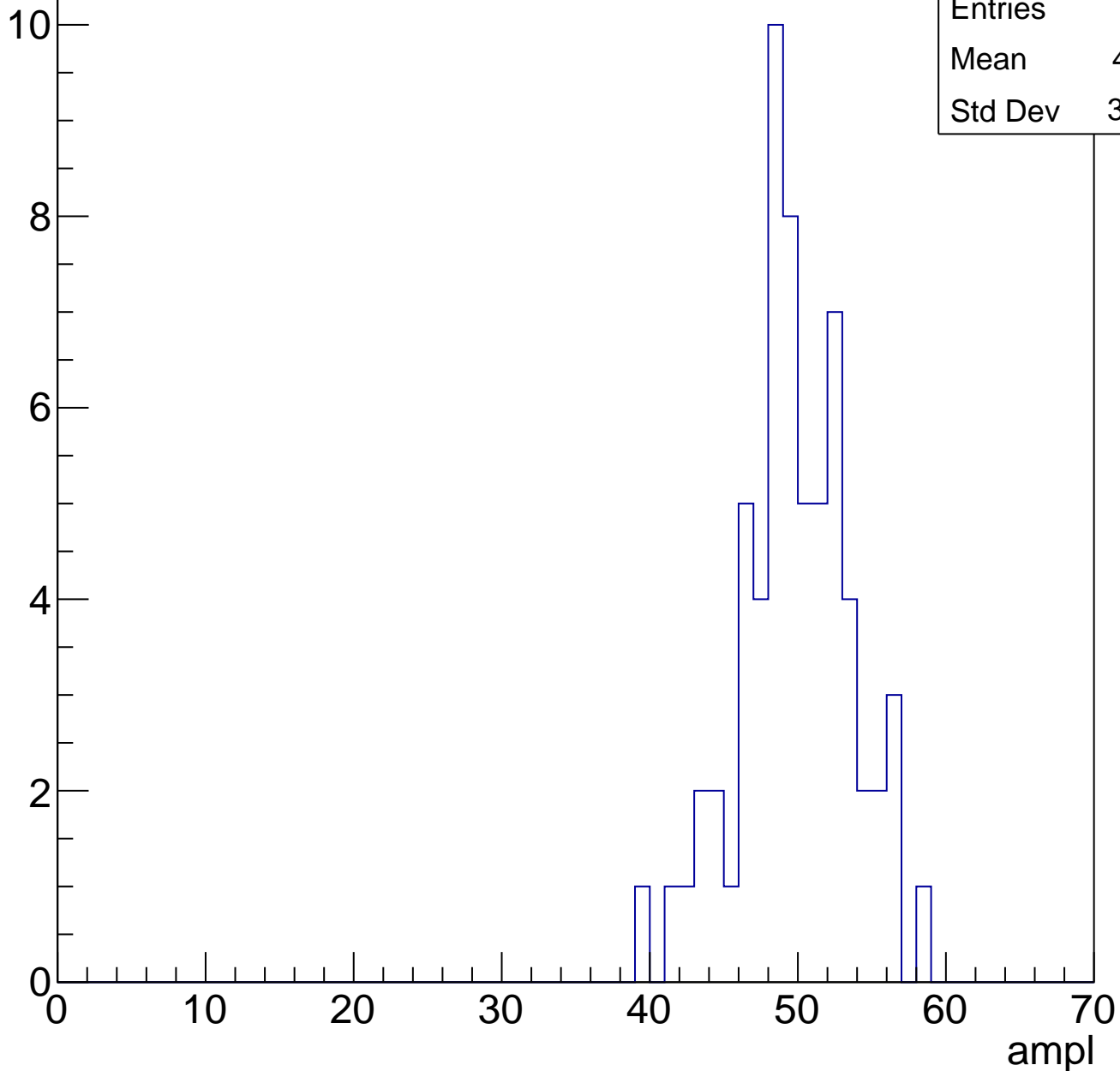


# B1L102S, U5-ch93, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	64
Mean	49.31
Std Dev	3.787

Entry

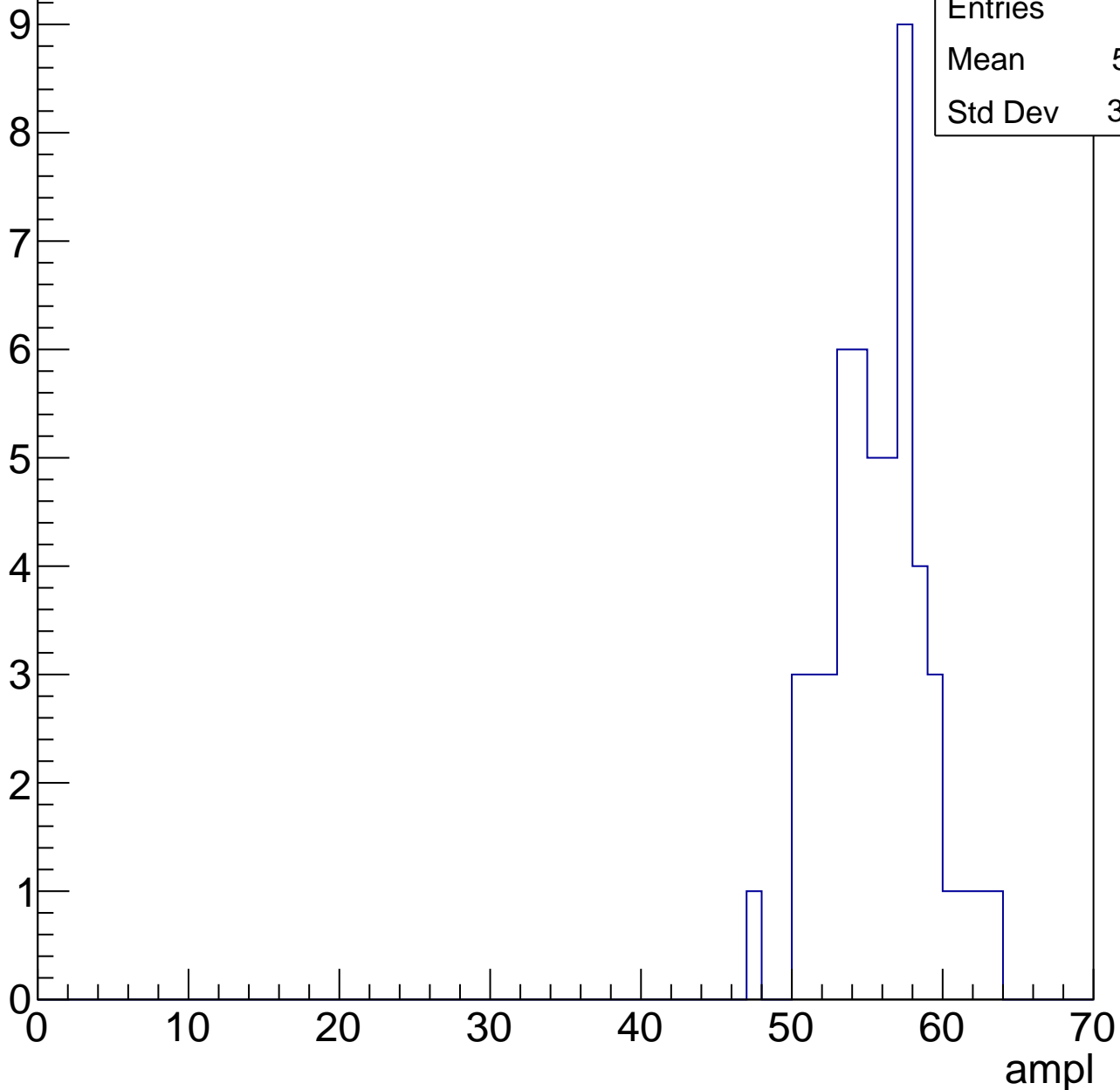


# B1L102S, U5-ch93, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

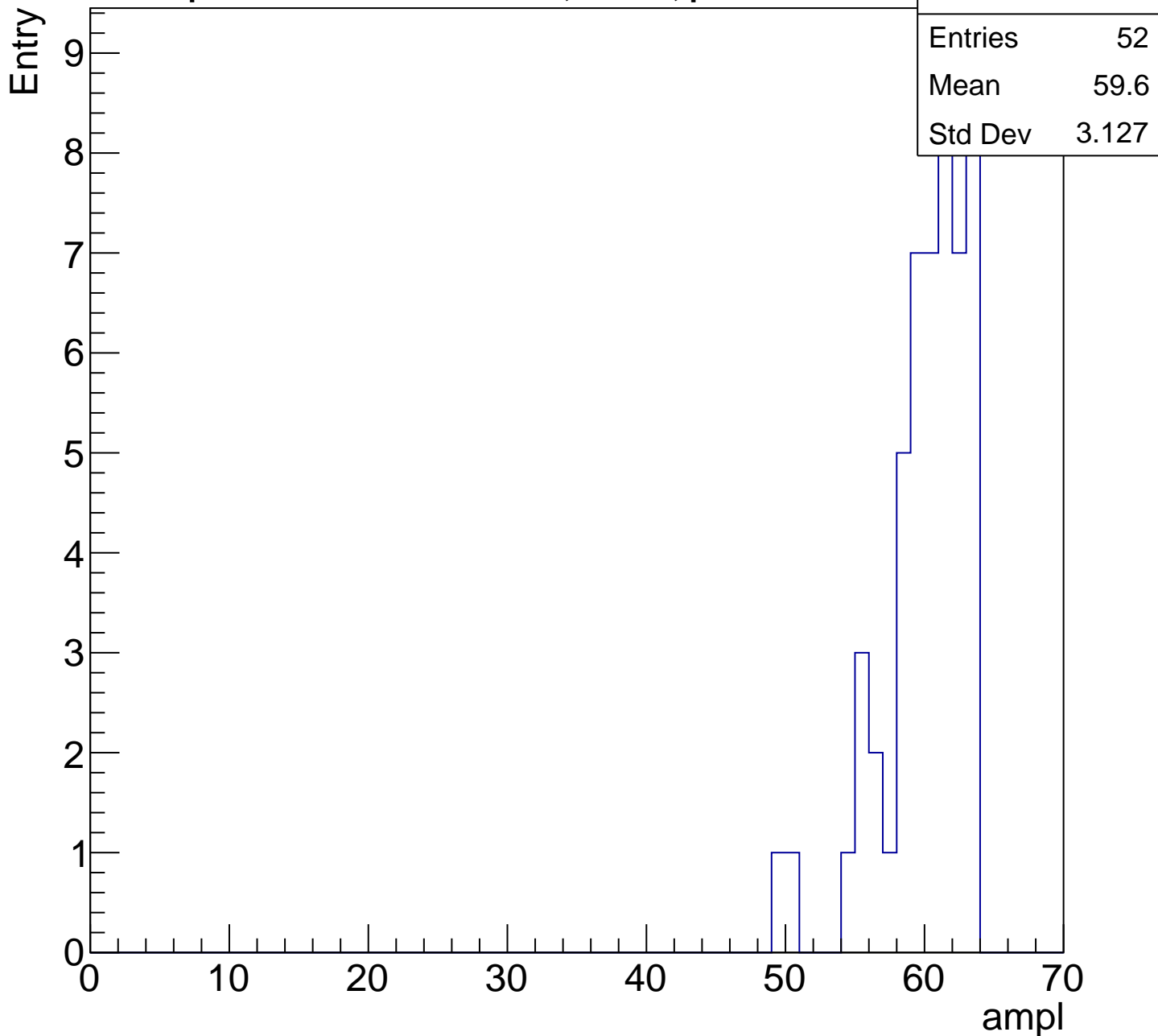
Entry

Entries	52
Mean	55.21
Std Dev	3.225



# B1L102S, U5-ch93, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2



# B1L102S, U5-ch93, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

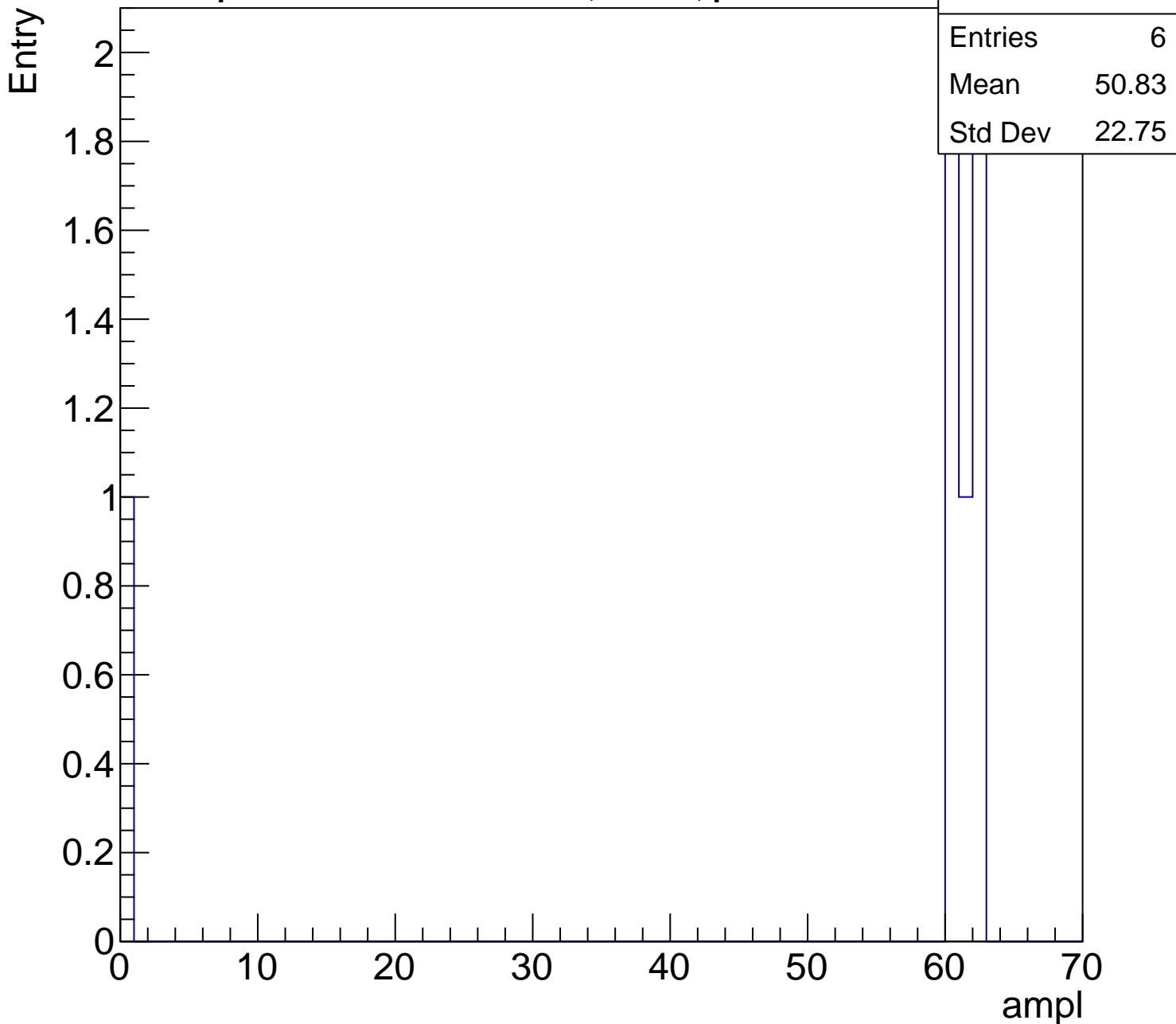
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	50.83
Std Dev	22.75

0 10 20 30 40 50 60 70

ampl





# B1L102S, U5-ch93, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	11
Std Dev	11

# B1L102S, U5-ch94, adc0

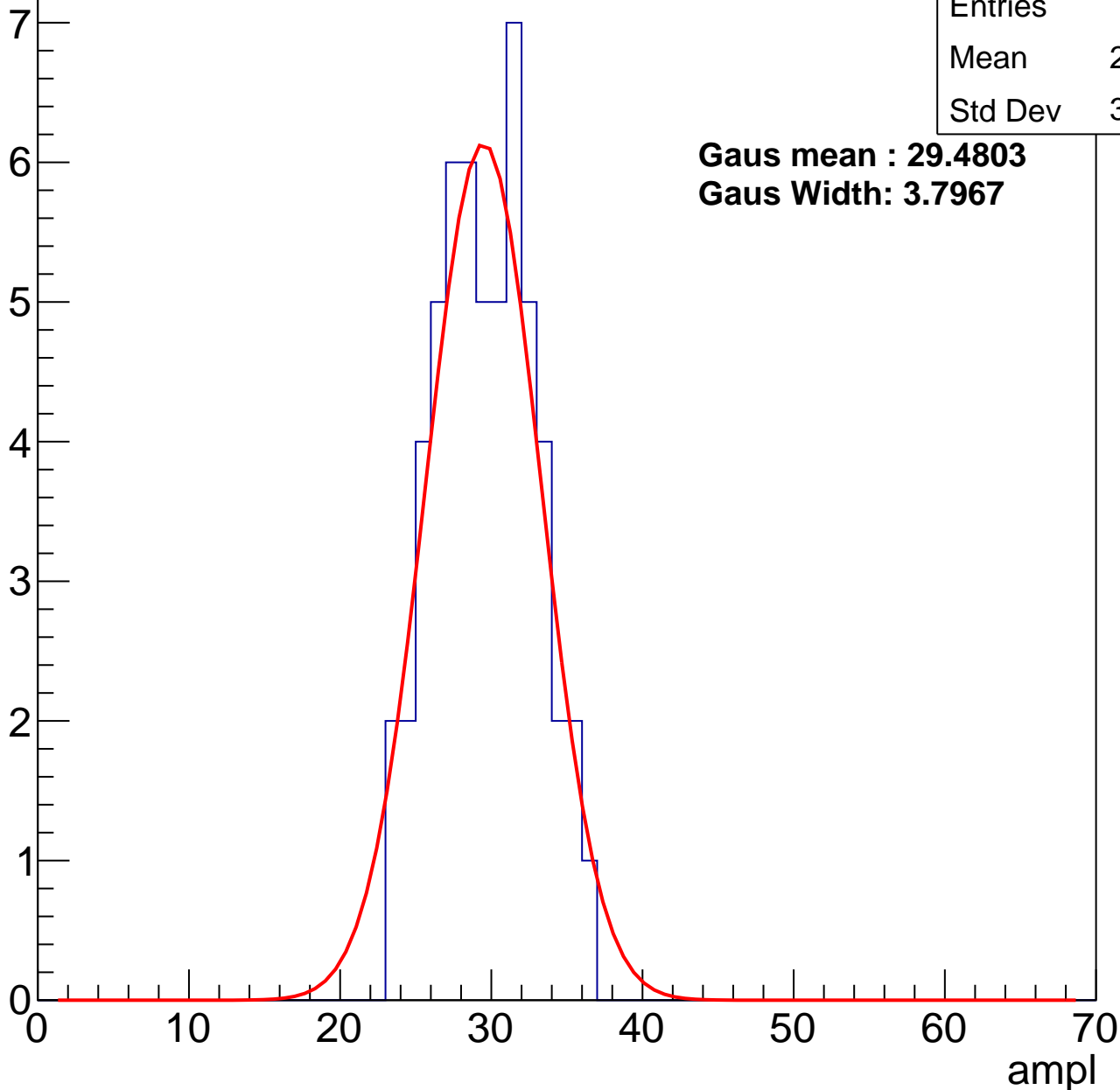
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	29.14
Std Dev	3.198

**Gaus mean : 29.4803**

**Gaus Width: 3.7967**



# B1L102S, U5-ch94, adc1

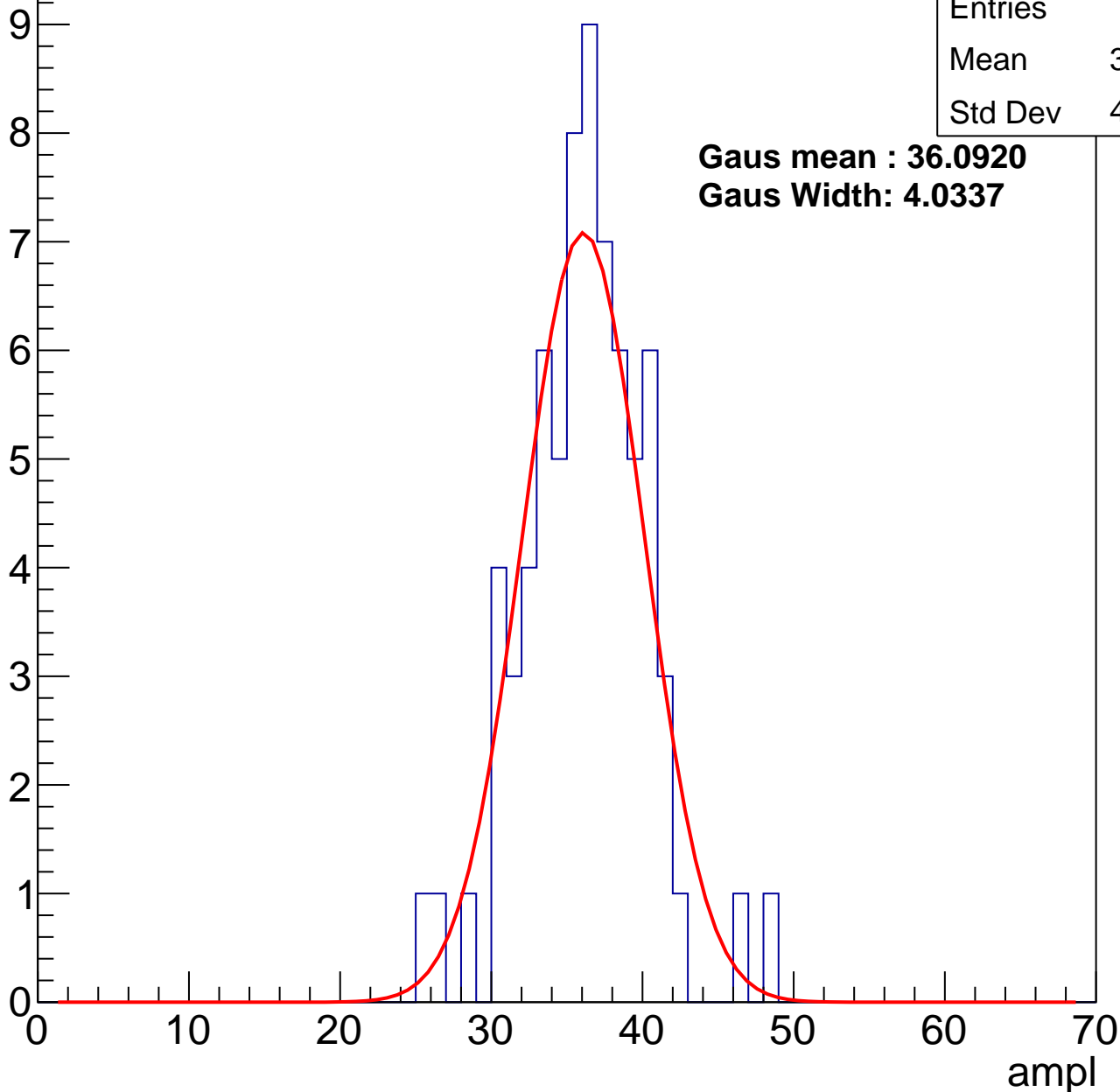
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	35.74
Std Dev	4.035

**Gaus mean : 36.0920**

**Gaus Width: 4.0337**



# B1L102S, U5-ch94, adc2

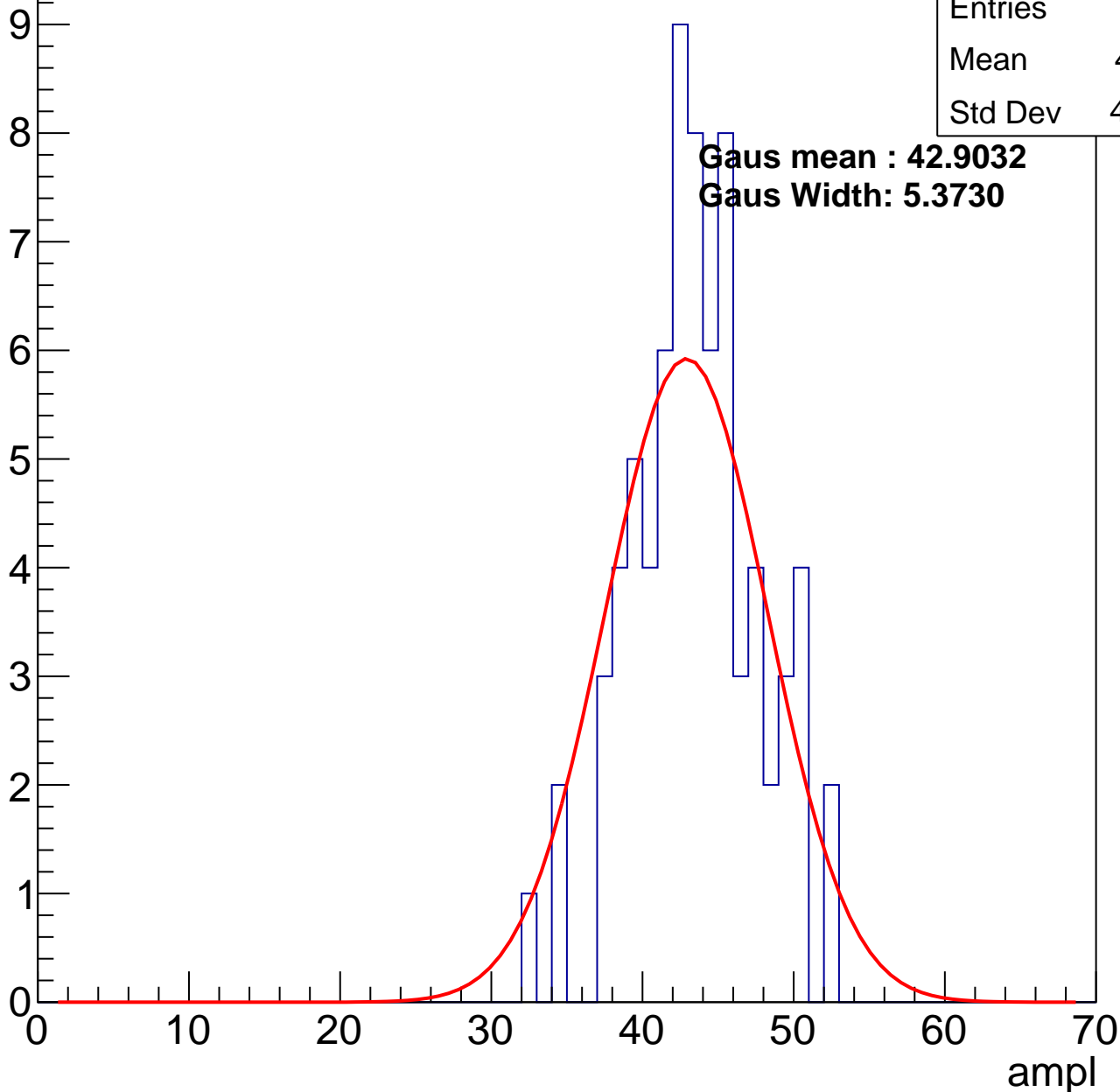
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	43.01
Std Dev	4.167

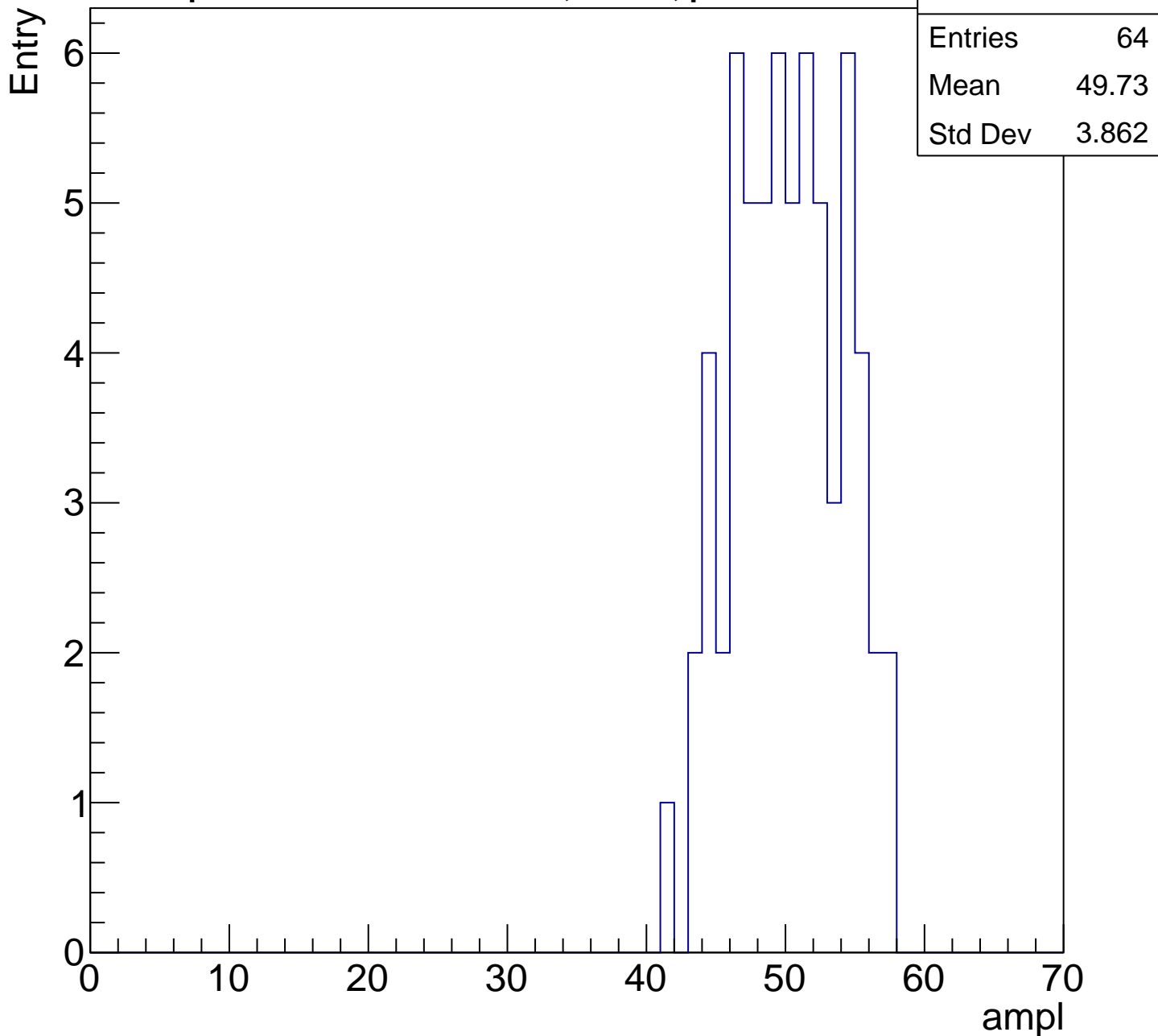
**Gaus mean : 42.9032**

**Gaus Width: 5.3730**



# B1L102S, U5-ch94, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2



# B1L102S, U5-ch94, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

7

6

5

4

3

2

1

0

Entries 65

Mean 55.68

Std Dev 3.57

ampl

0

10

20

30

40

50

60

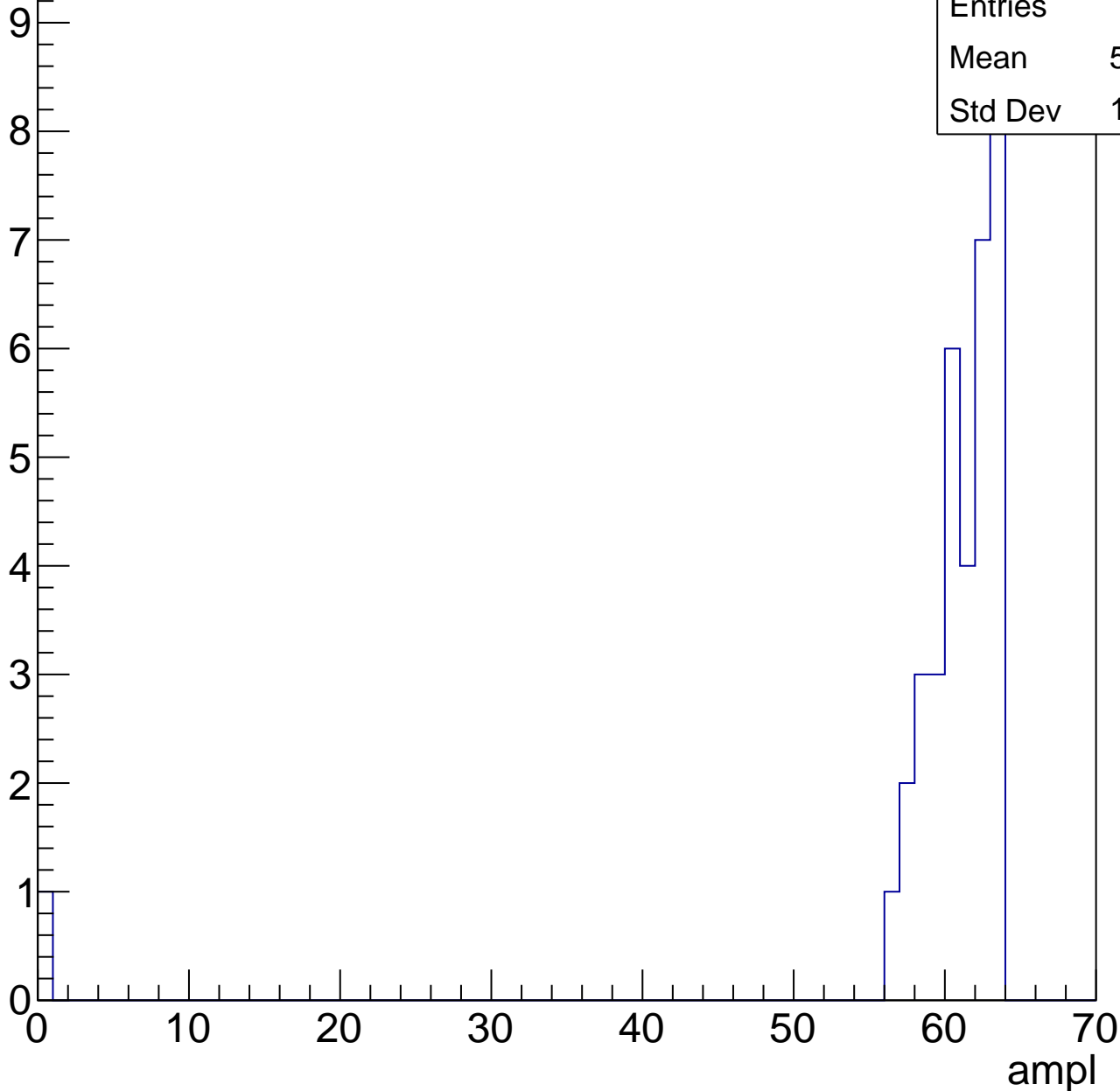
70

# B1L102S, U5-ch94, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	36
Mean	59.06
Std Dev	10.18



# B1L102S, U5-ch94, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U5-ch94, adc7

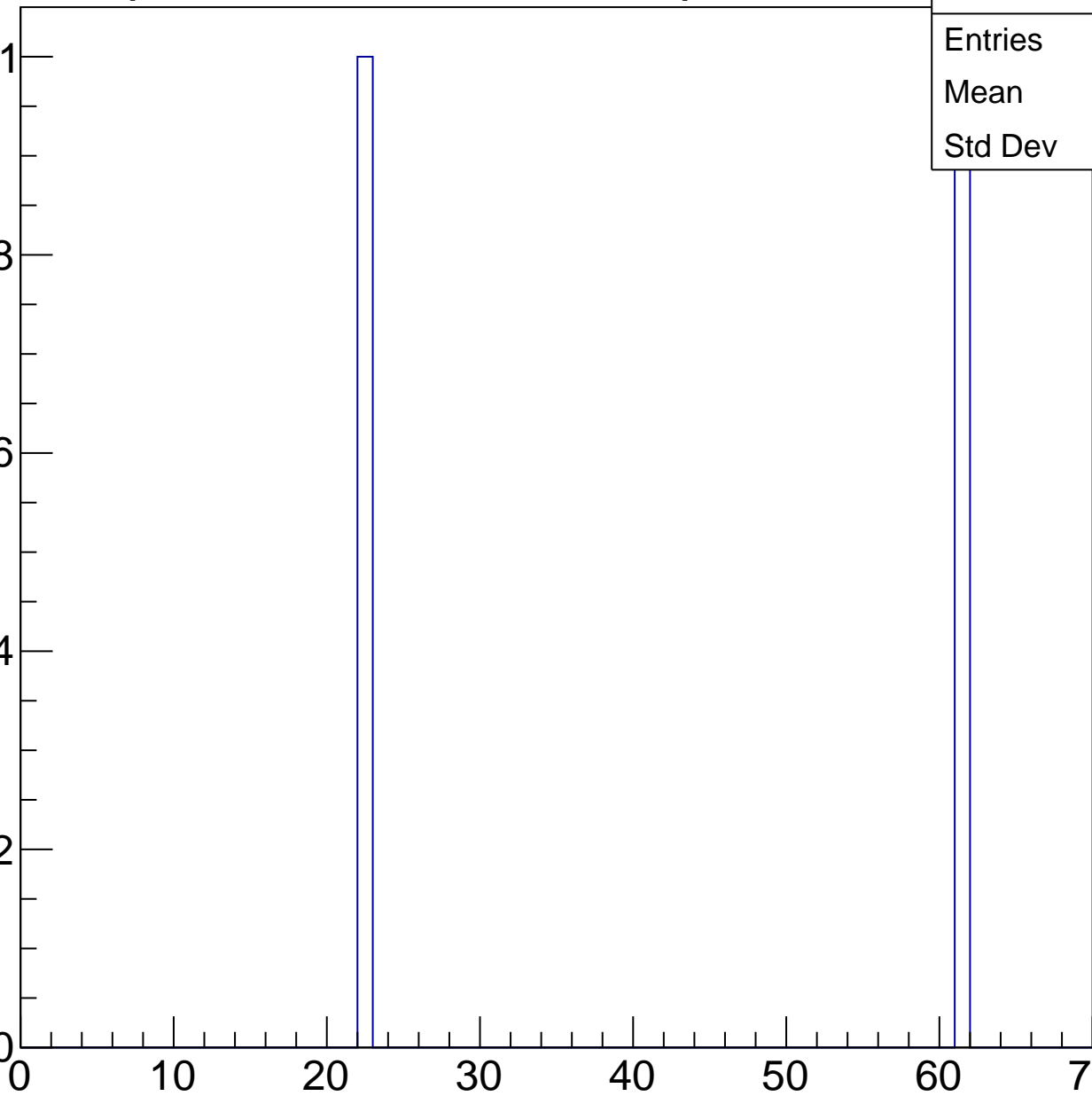
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	41.5
Std Dev	19.5

ampl



# B1L102S, U5-ch95, adc0

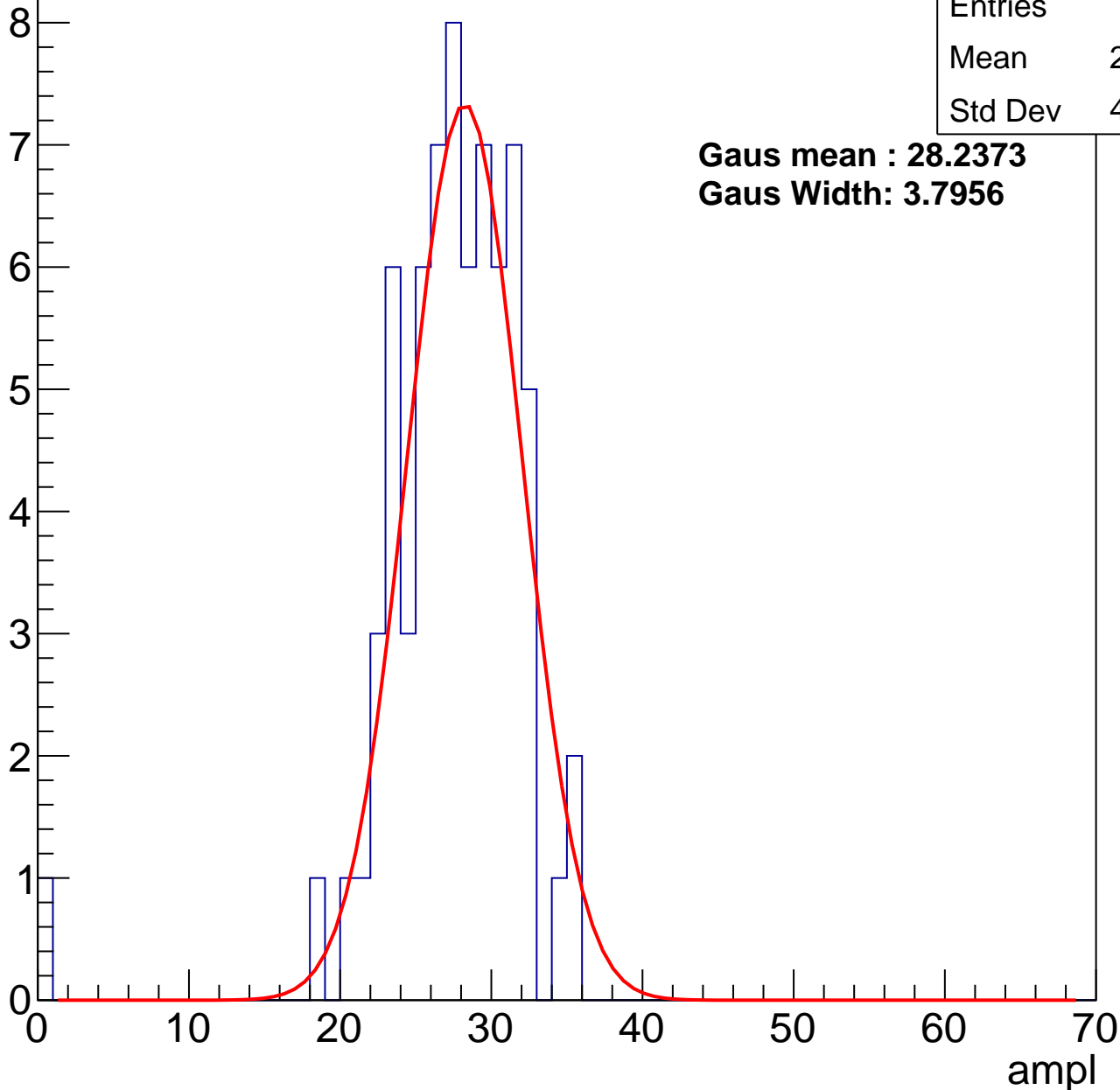
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	26.97
Std Dev	4.785

**Gaus mean : 28.2373**

**Gaus Width: 3.7956**



# B1L102S, U5-ch95, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	62
Mean	34.35
Std Dev	3.699

**Gaus mean : 34.6285**

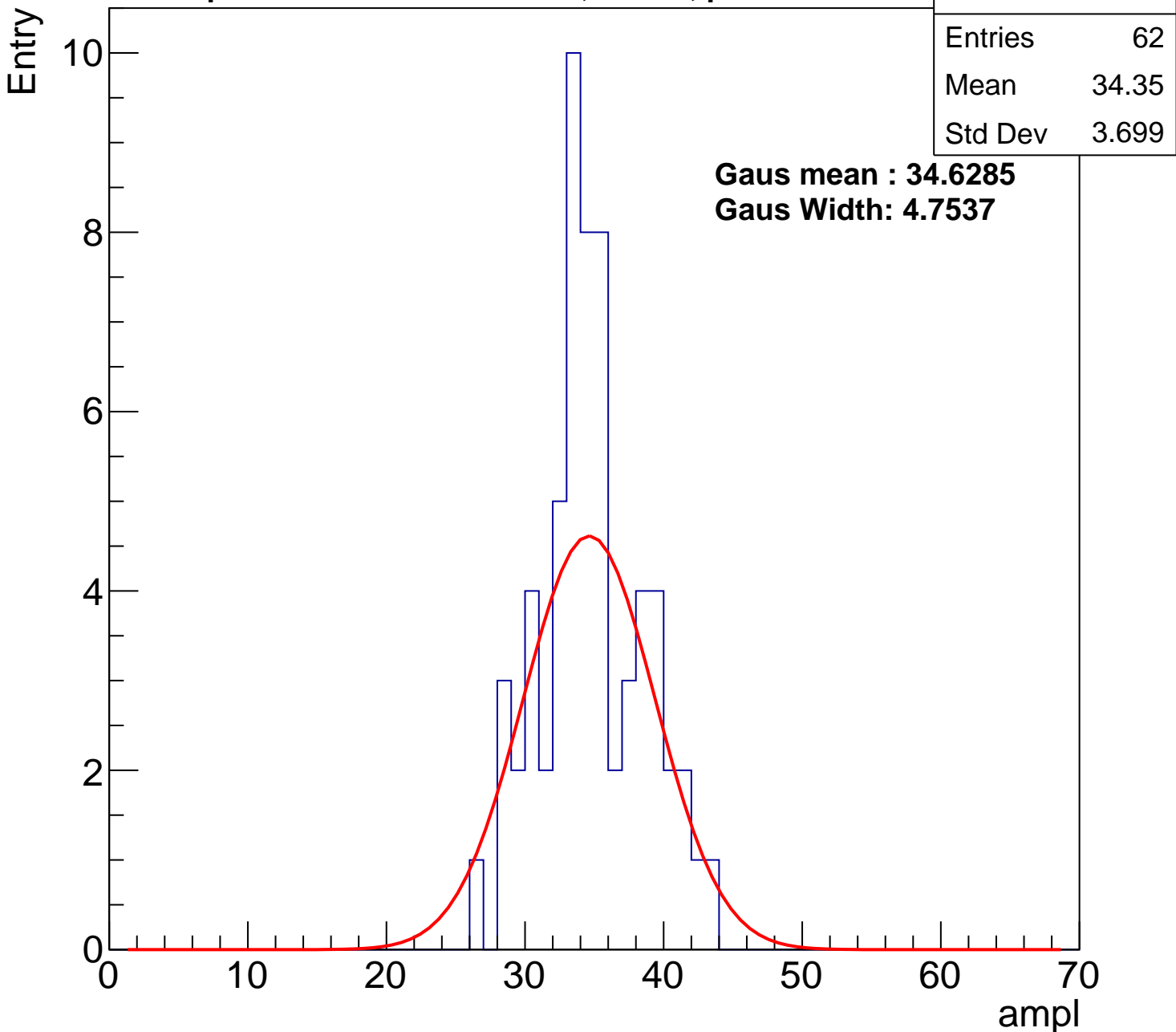
**Gaus Width: 4.7537**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U5-ch95, adc2

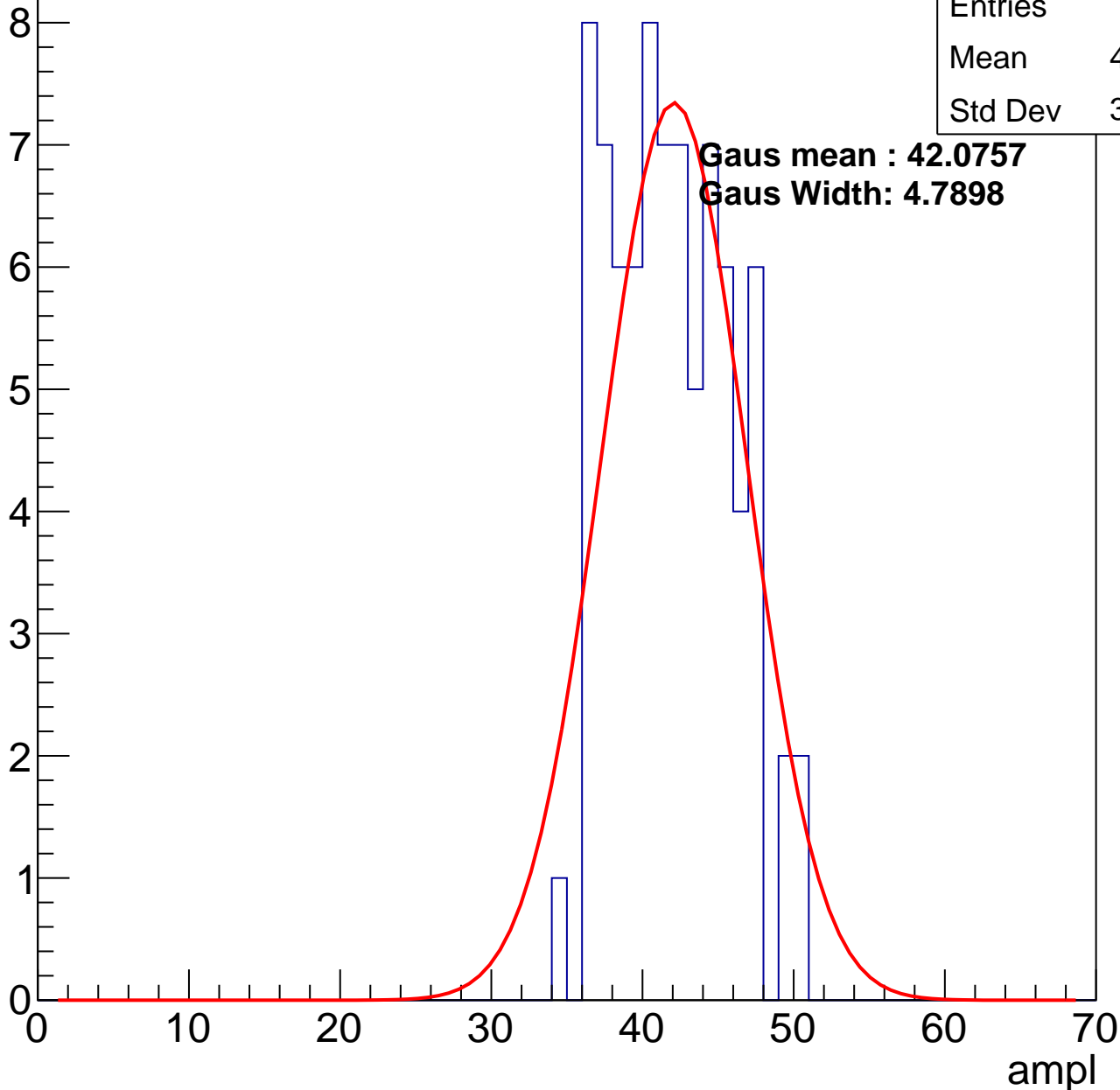
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	82
Mean	41.48
Std Dev	3.858

**Gaus mean : 42.0757**

**Gaus Width: 4.7898**

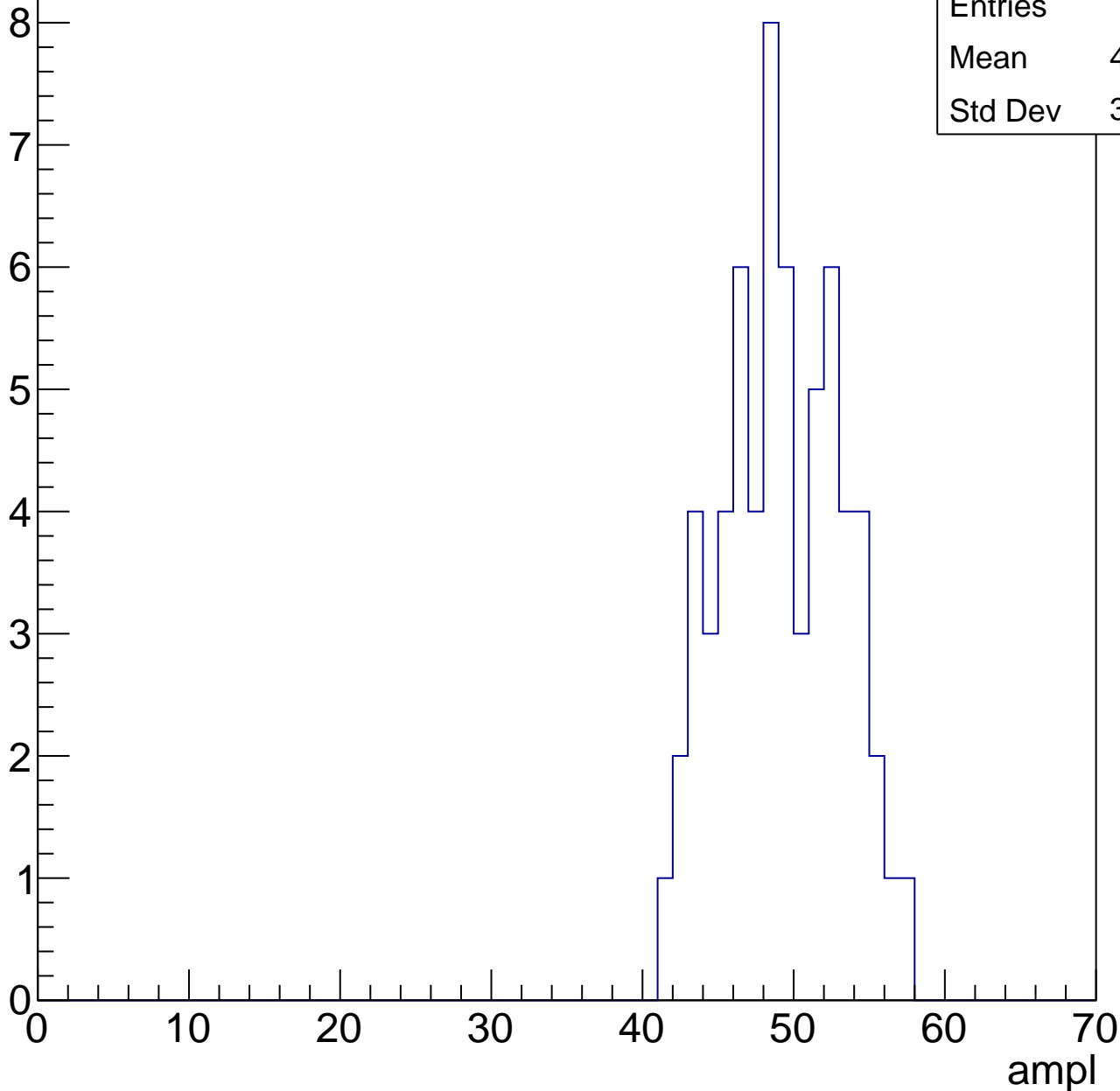


# B1L102S, U5-ch95, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	48.73
Std Dev	3.842



# B1L102S, U5-ch95, adc4

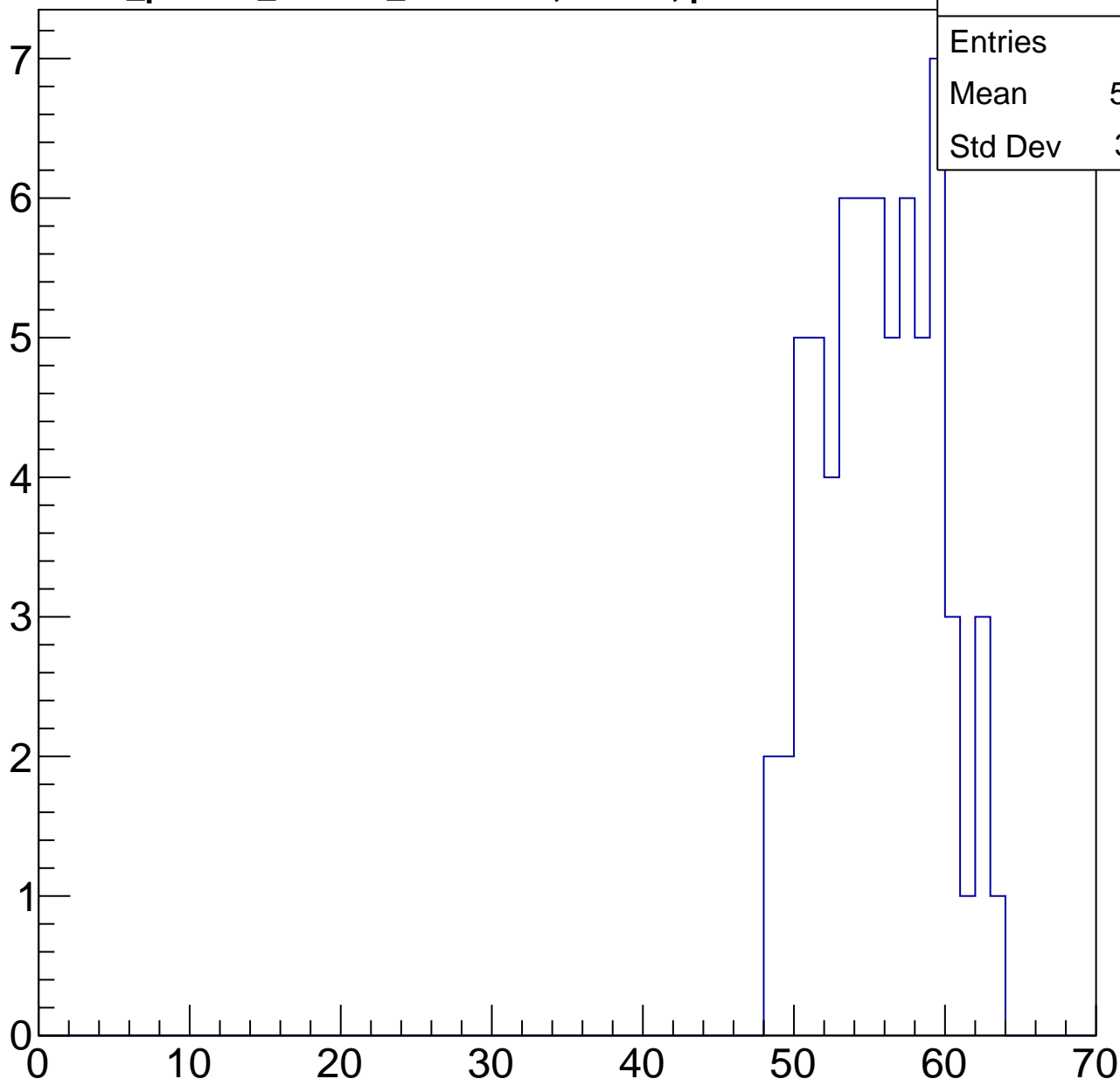
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

7  
6  
5  
4  
3  
2  
1  
0

Entries	67
Mean	55.13
Std Dev	3.761

ampl



# B1L102S, U5-ch95, adc5

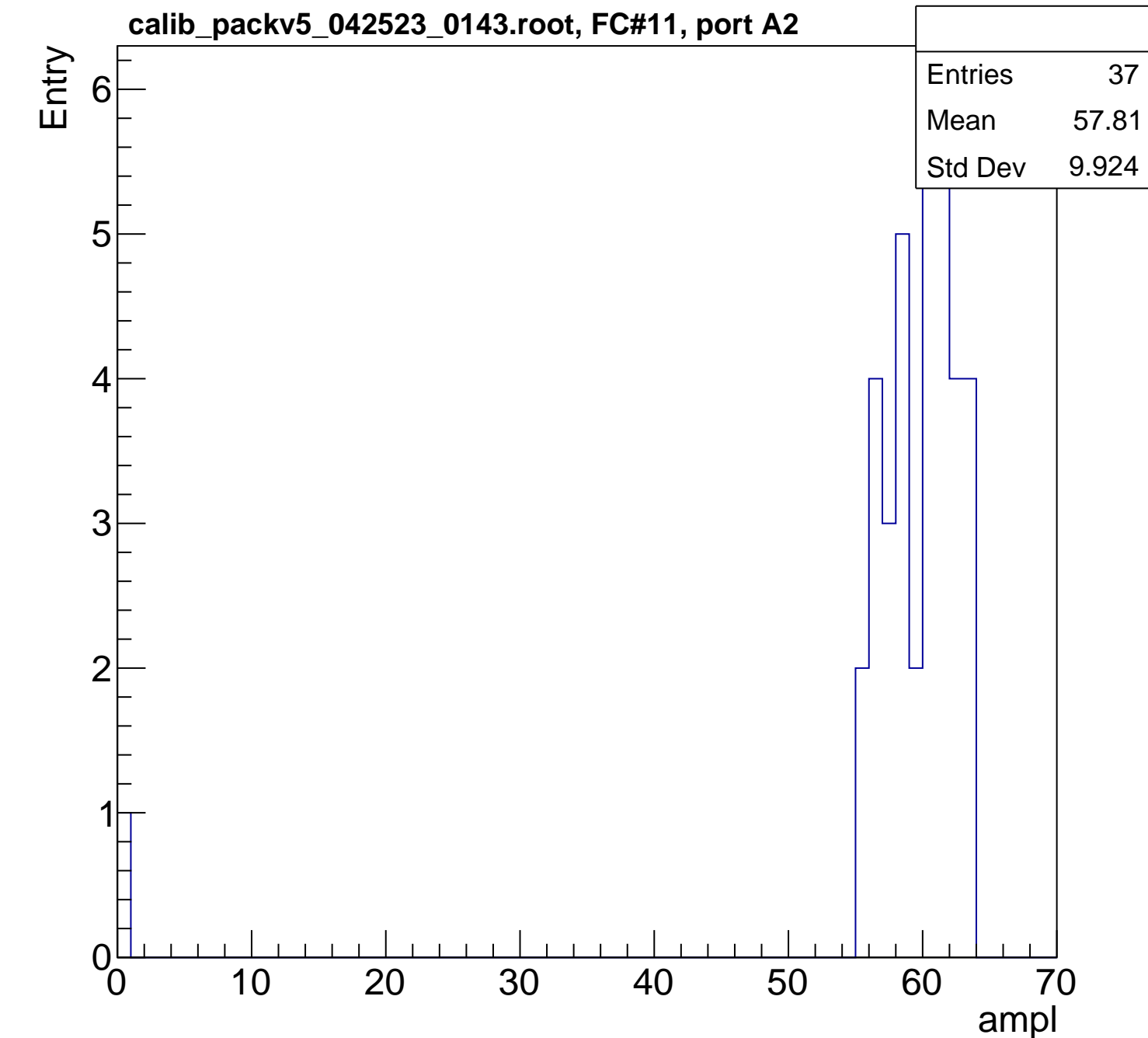
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

6  
5  
4  
3  
2  
1  
0

Entries	37
Mean	57.81
Std Dev	9.924

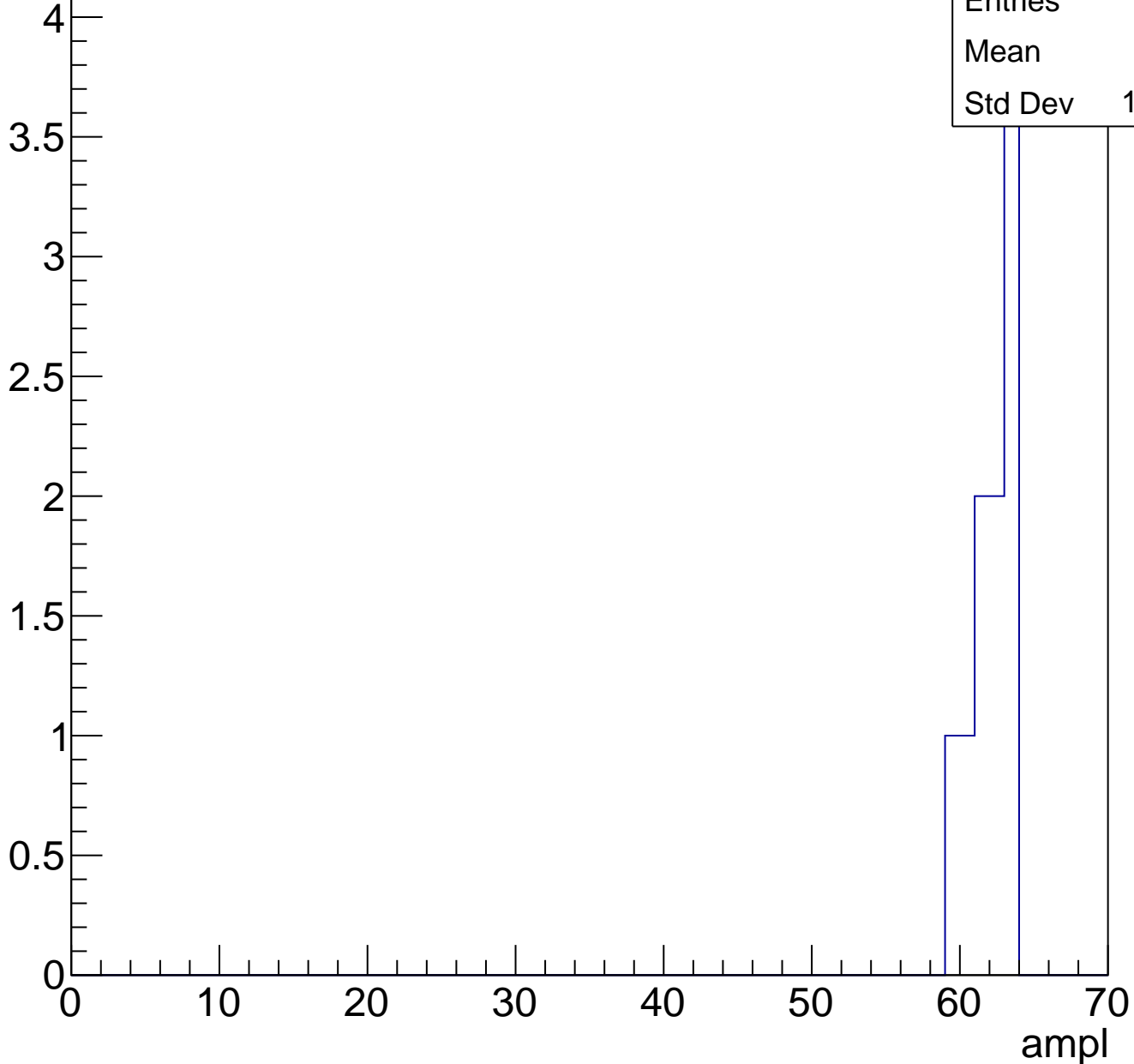
ampl



# B1L102S, U5-ch95, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



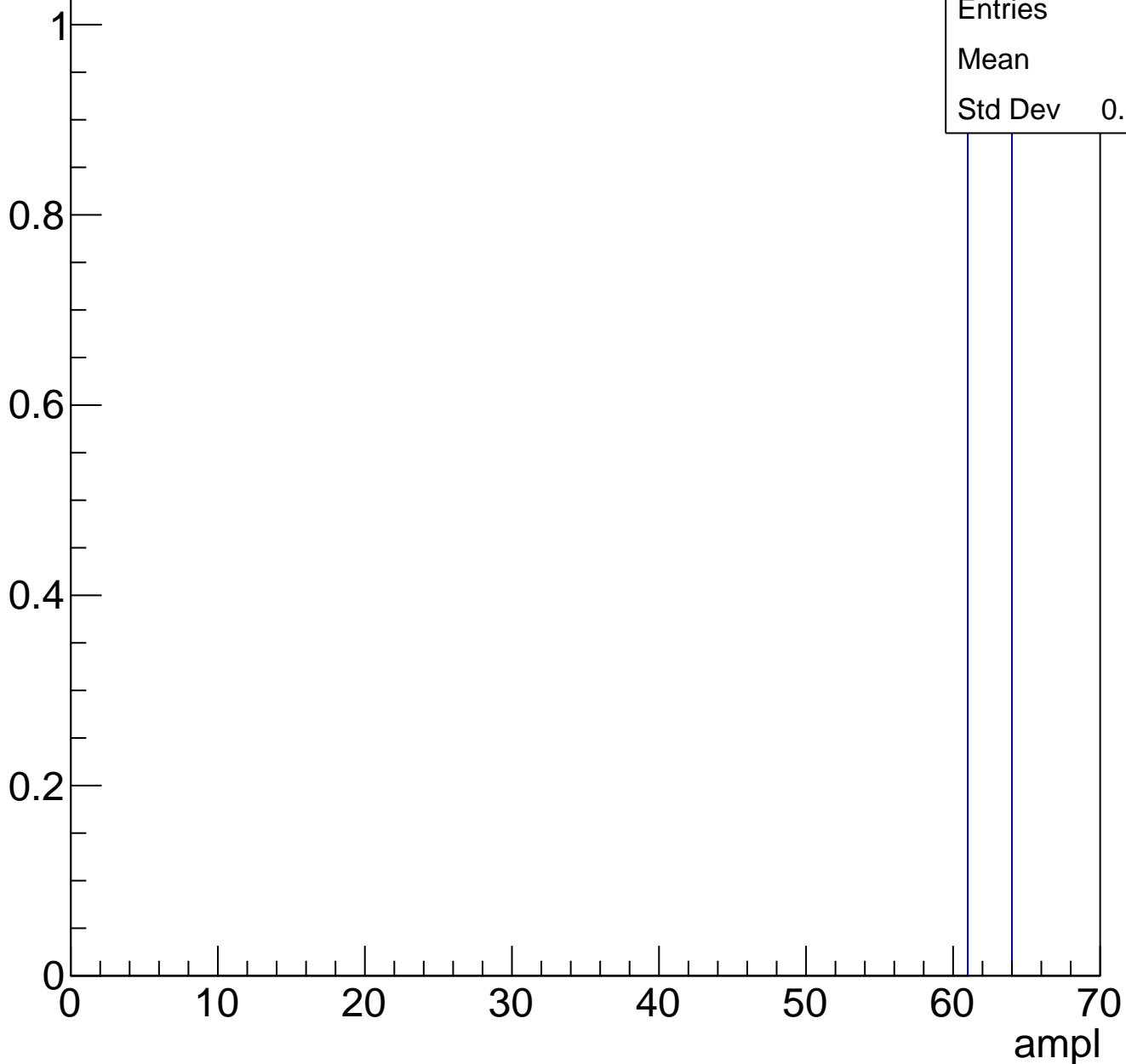
Entries	10
Mean	61.7
Std Dev	1.345



# B1L102S, U5-ch95, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U5-ch96, adc0

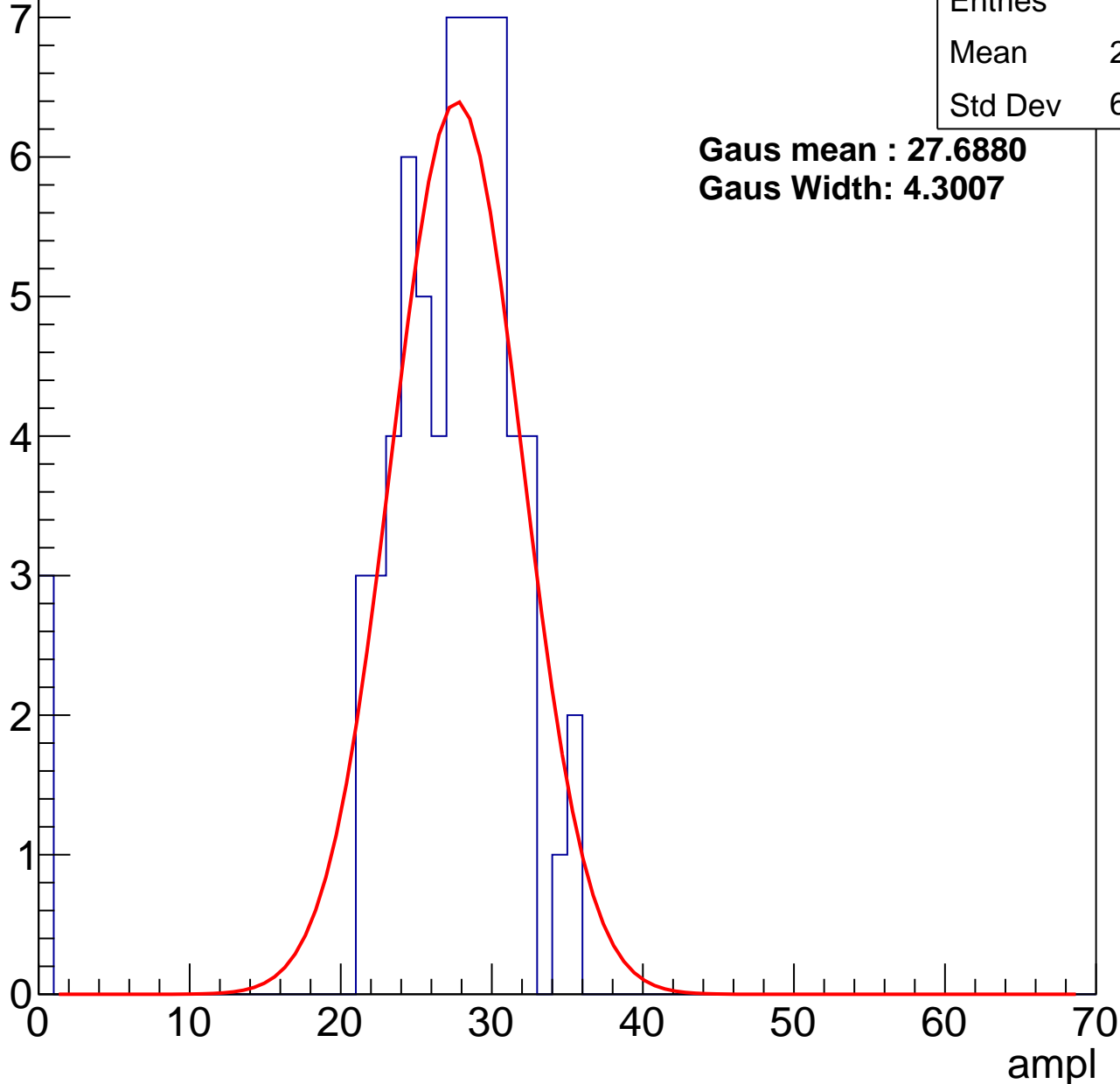
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	26.09
Std Dev	6.574

**Gaus mean : 27.6880**

**Gaus Width: 4.3007**



# B1L102S, U5-ch96, adc1

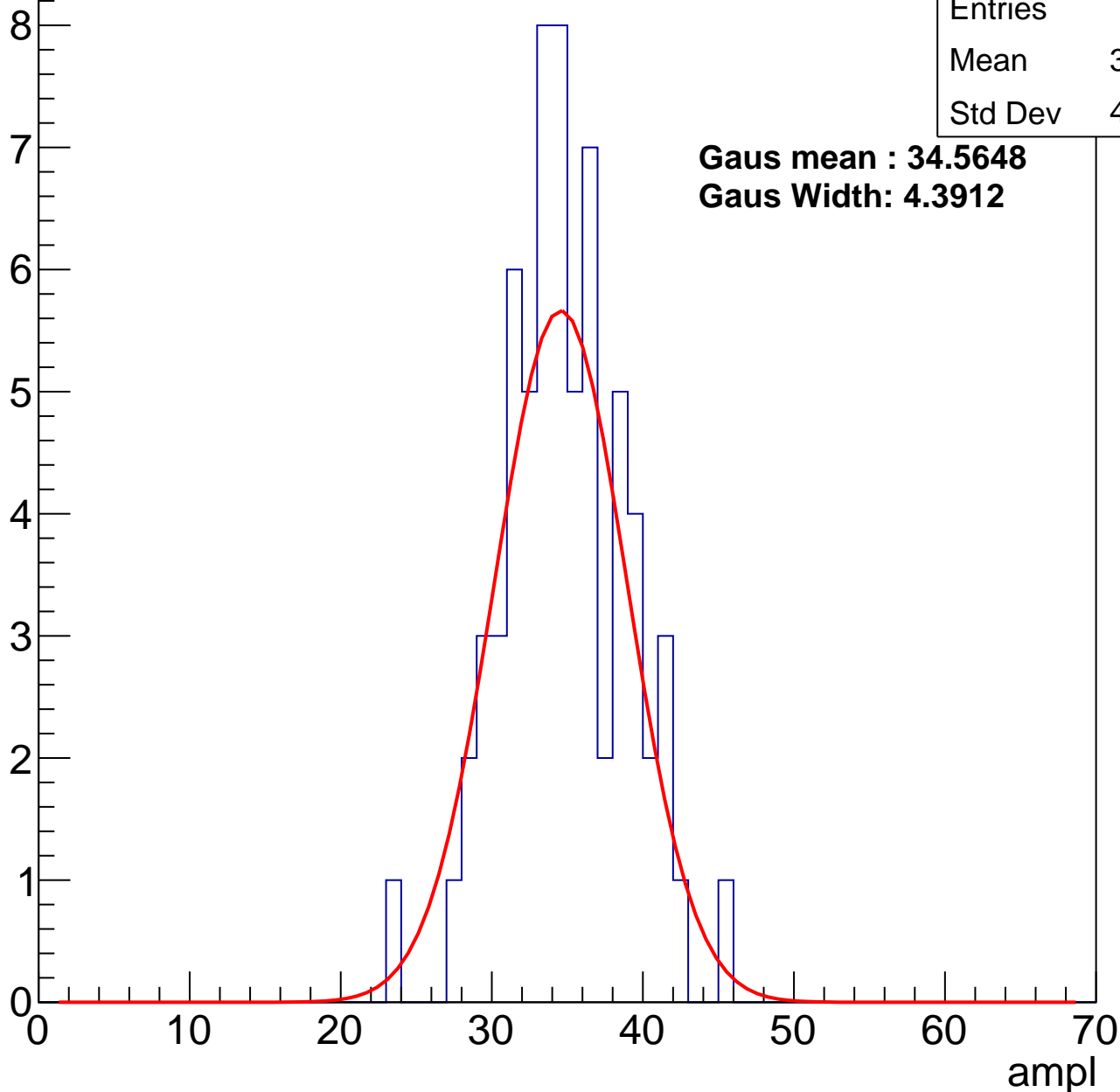
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	34.36
Std Dev	4.003

**Gaus mean : 34.5648**

**Gaus Width: 4.3912**



# B1L102S, U5-ch96, adc2

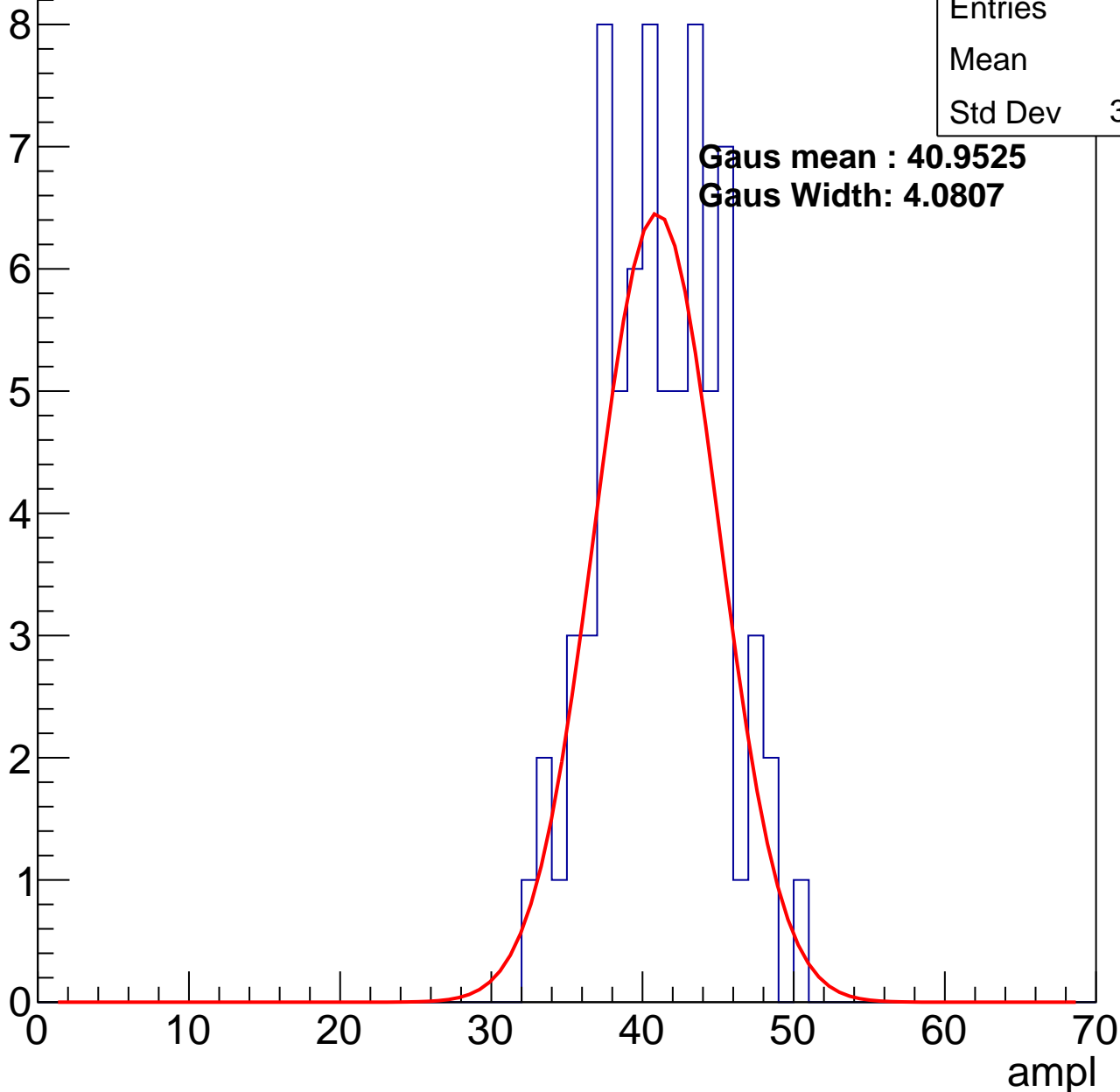
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	40.7
Std Dev	3.934

**Gaus mean : 40.9525**

**Gaus Width: 4.0807**

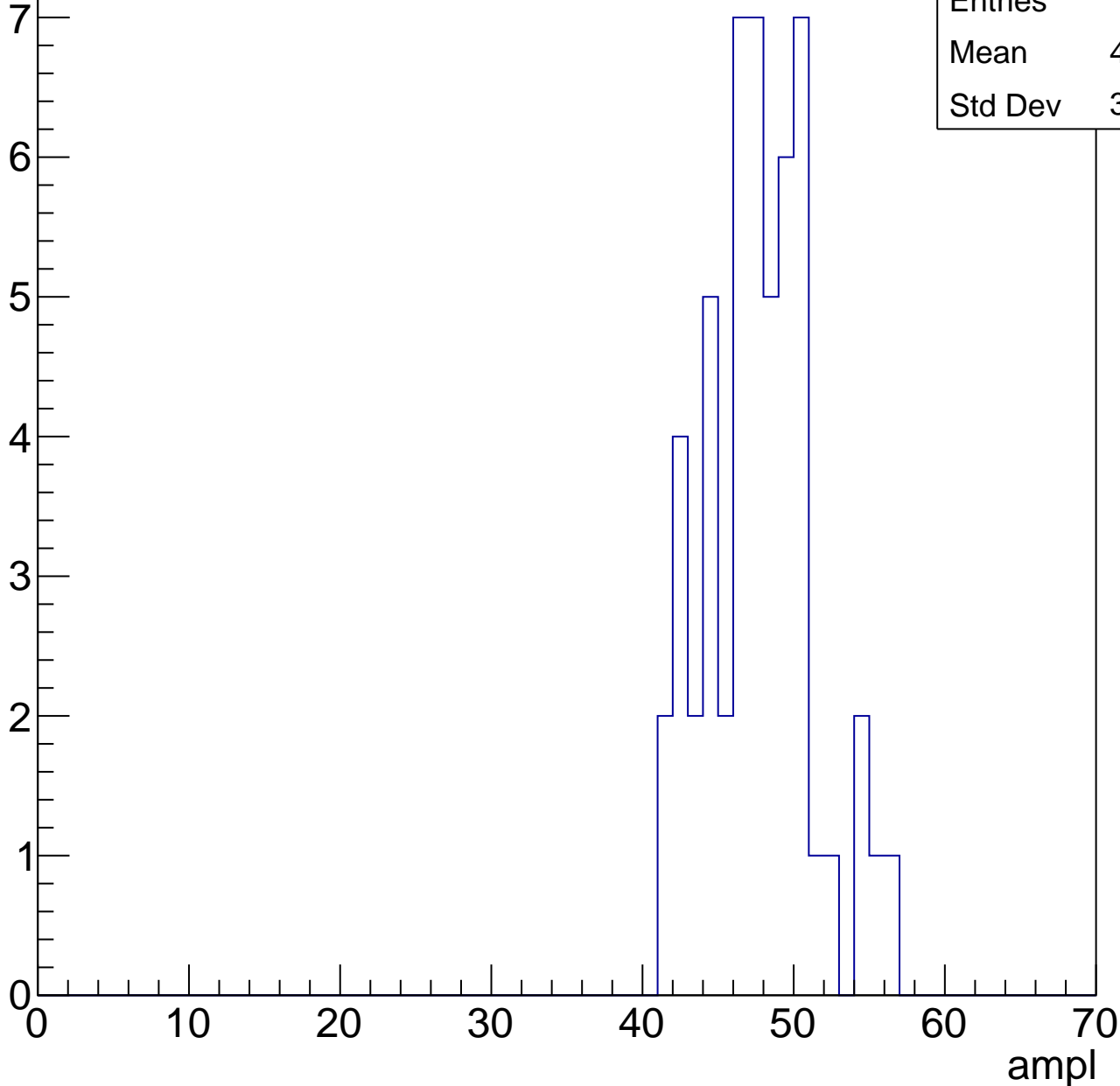


# B1L102S, U5-ch96, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	47.23
Std Dev	3.468

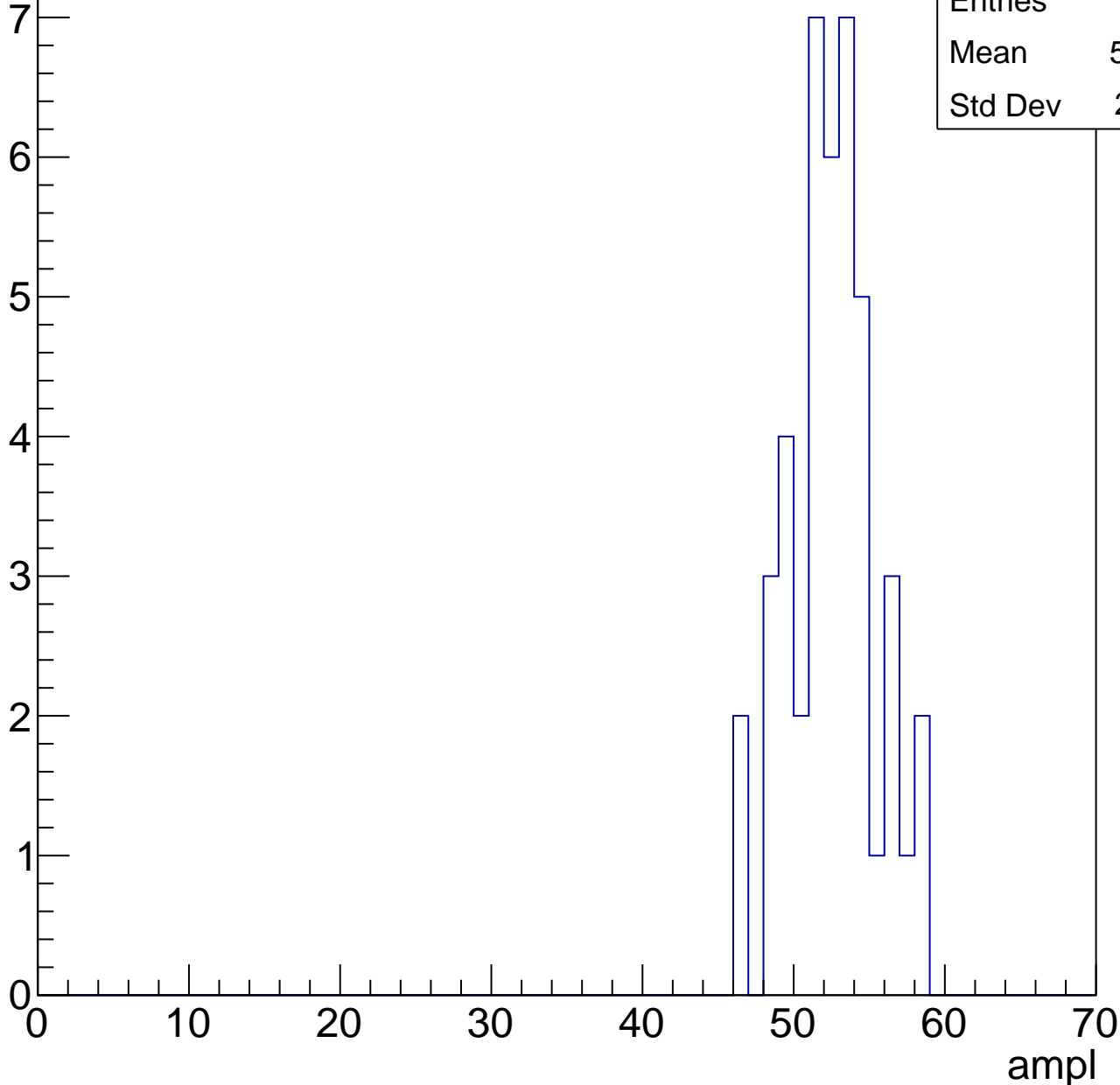


# B1L102S, U5-ch96, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

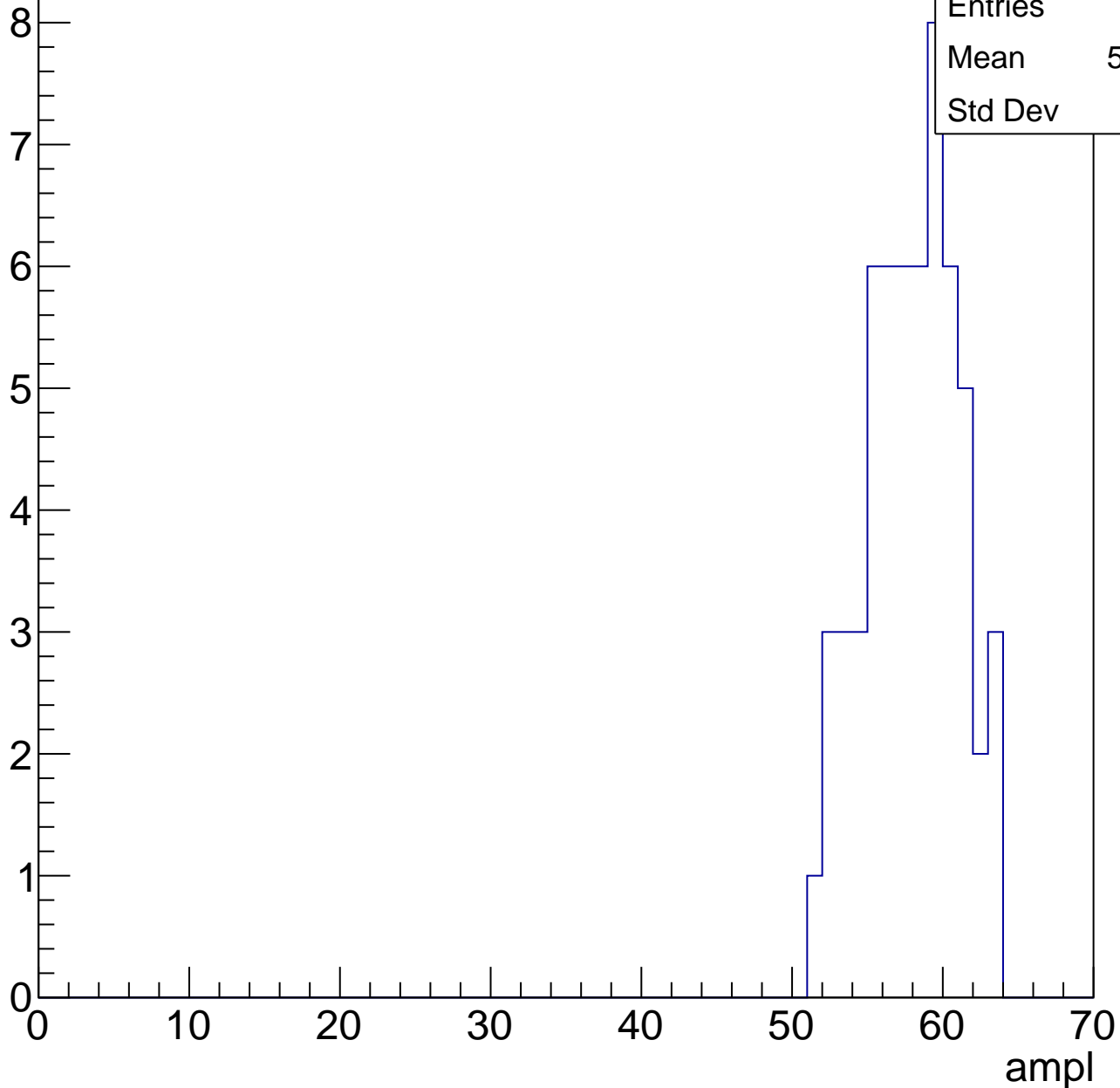
Entries	43
Mean	52.05
Std Dev	2.861



# B1L102S, U5-ch96, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

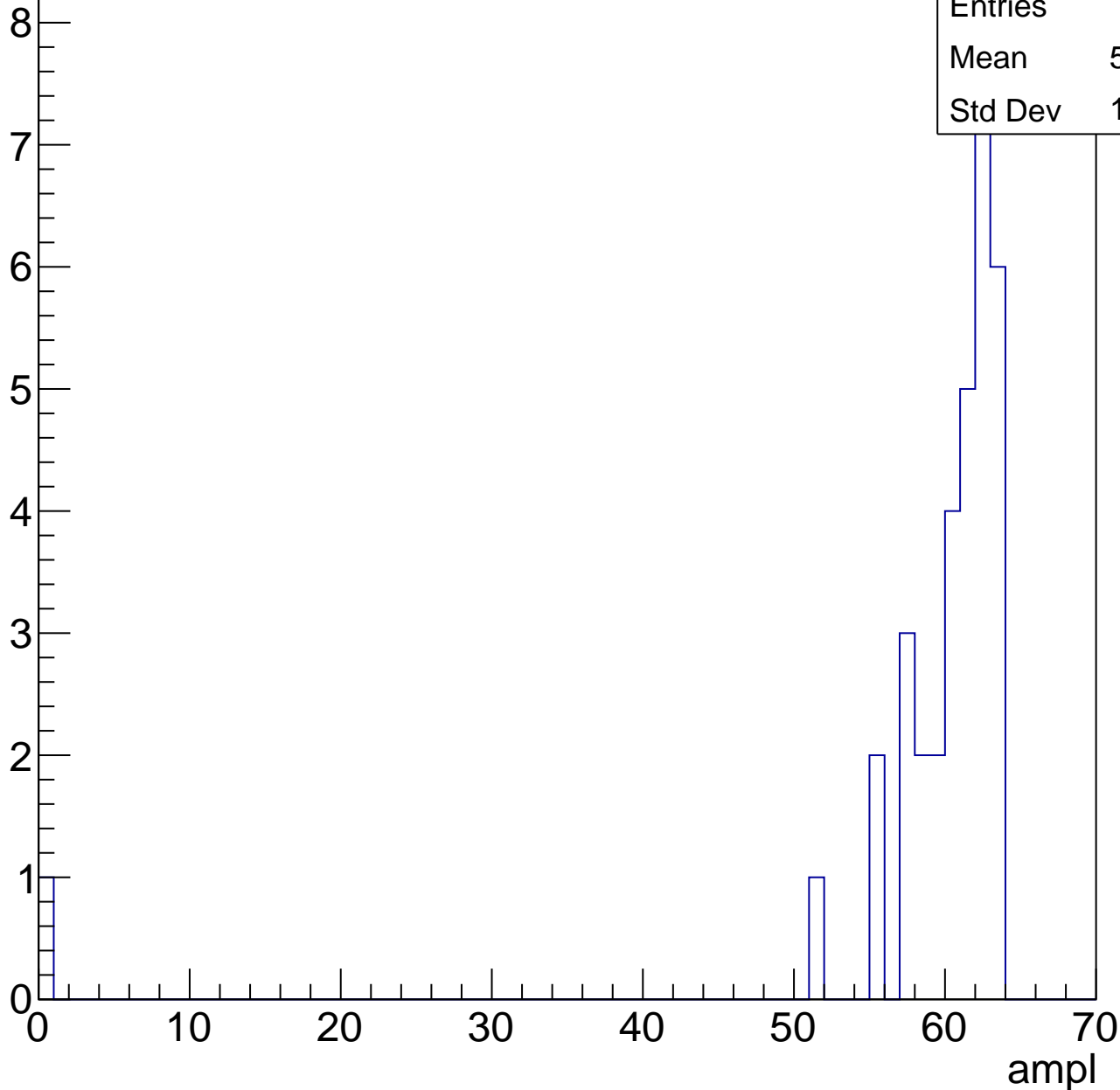


# B1L102S, U5-ch96, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	34
Mean	58.38
Std Dev	10.53





# B1L102S, U5-ch96, adc7

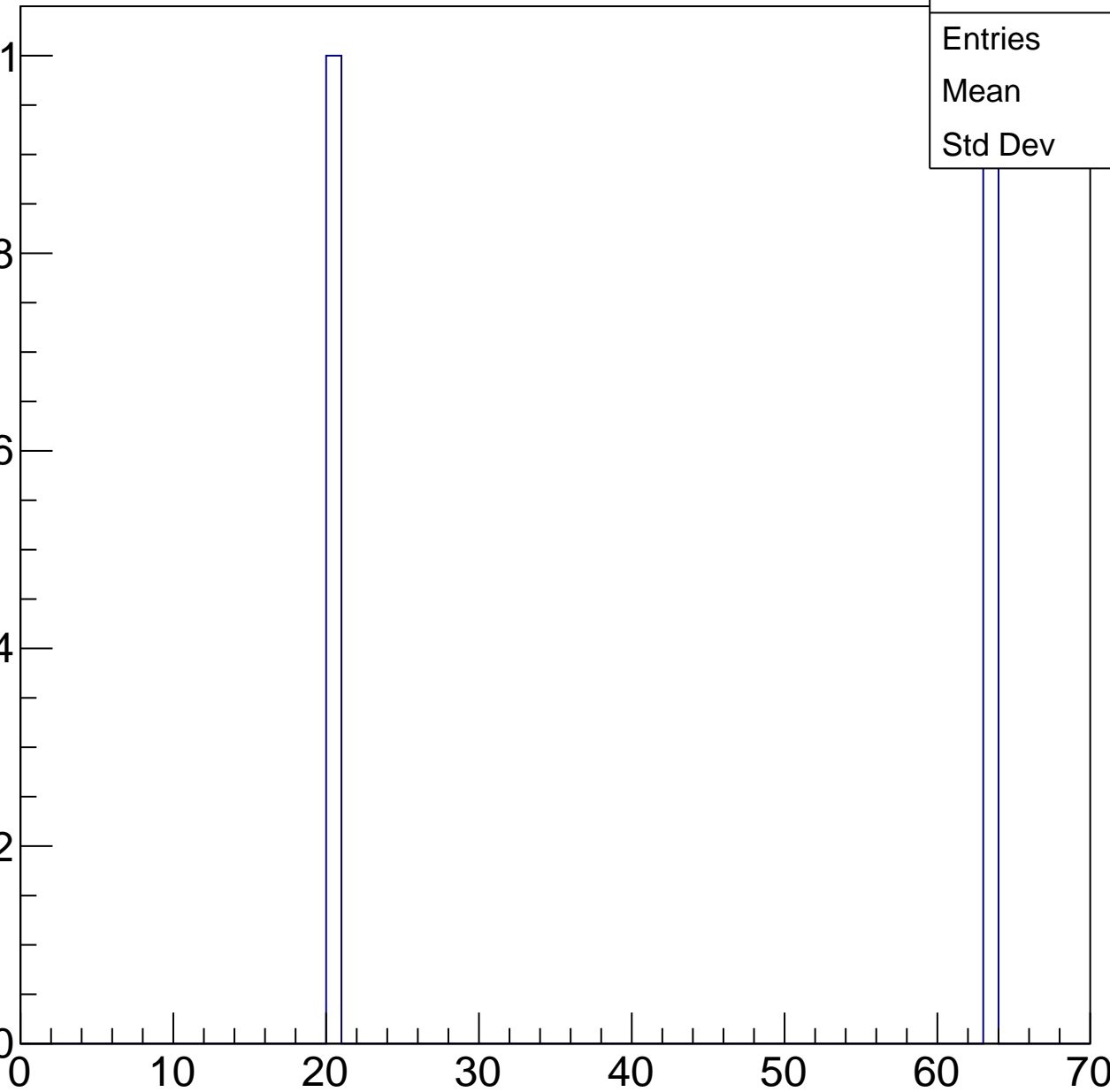
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	41.5
Std Dev	21.5

ampl



# B1L102S, U5-ch97, adc0

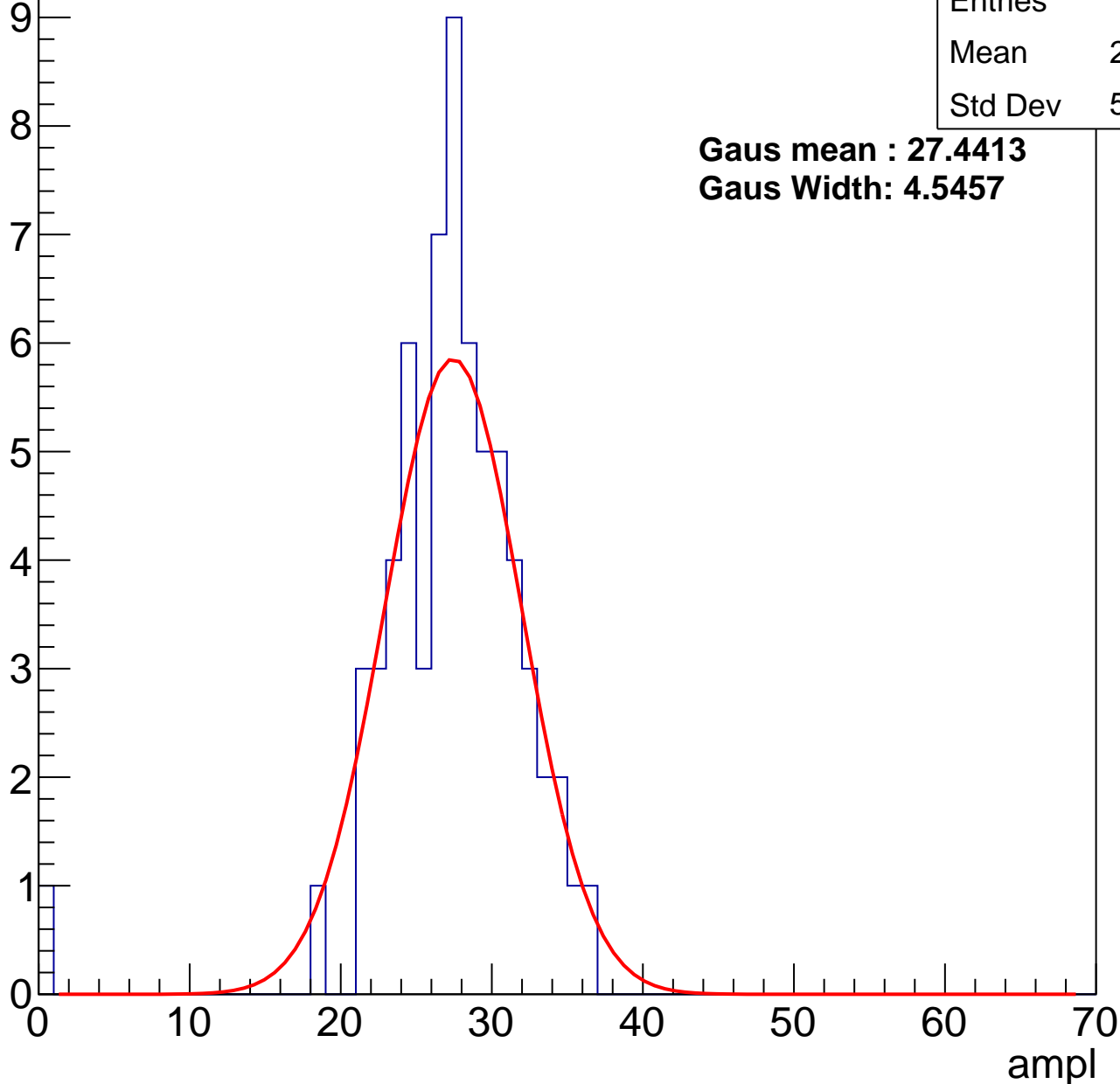
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	26.83
Std Dev	5.005

**Gaus mean : 27.4413**

**Gaus Width: 4.5457**



# B1L102S, U5-ch97, adc1

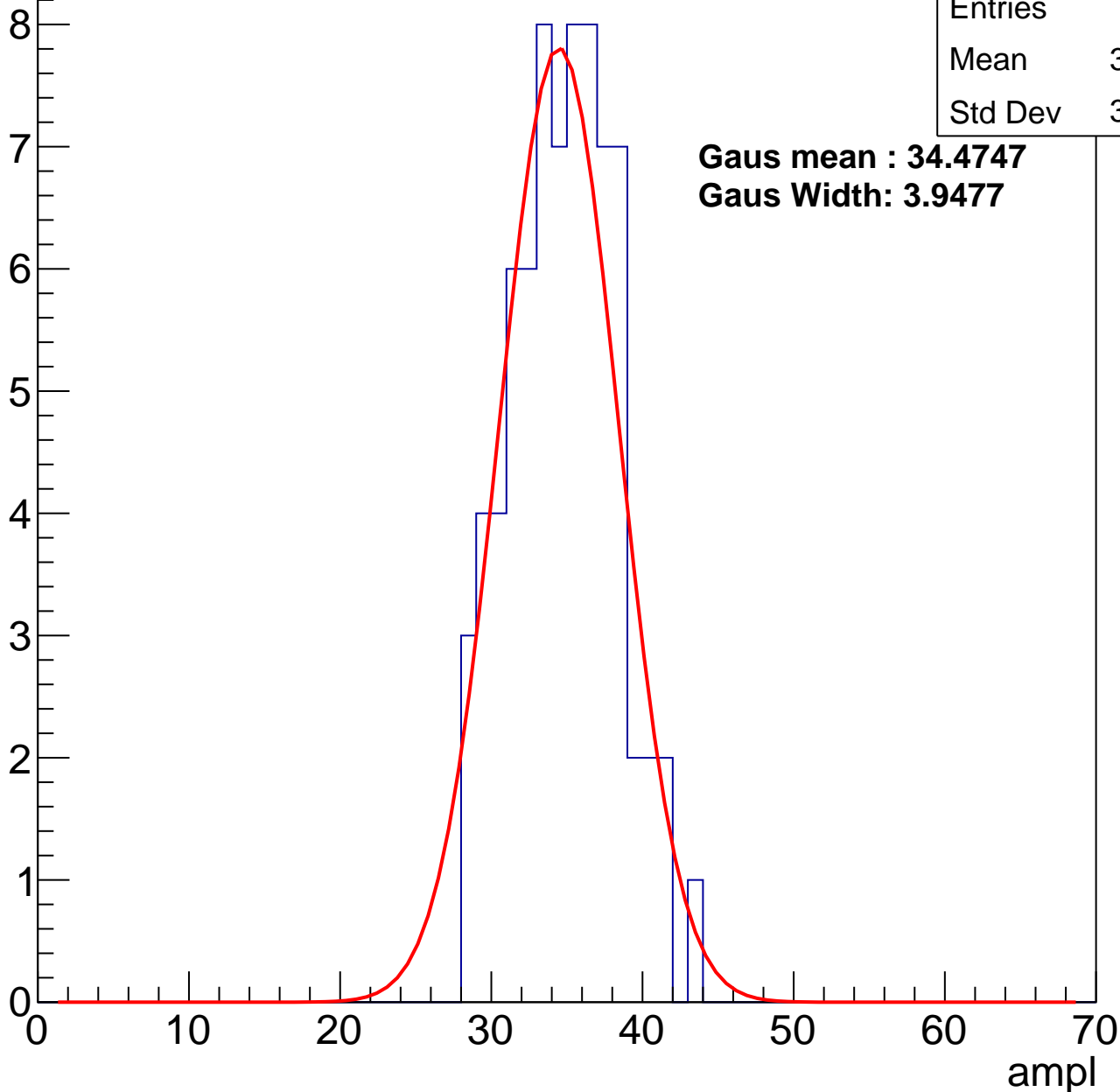
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	34.35
Std Dev	3.396

**Gaus mean : 34.4747**

**Gaus Width: 3.9477**



# B1L102S, U5-ch97, adc2

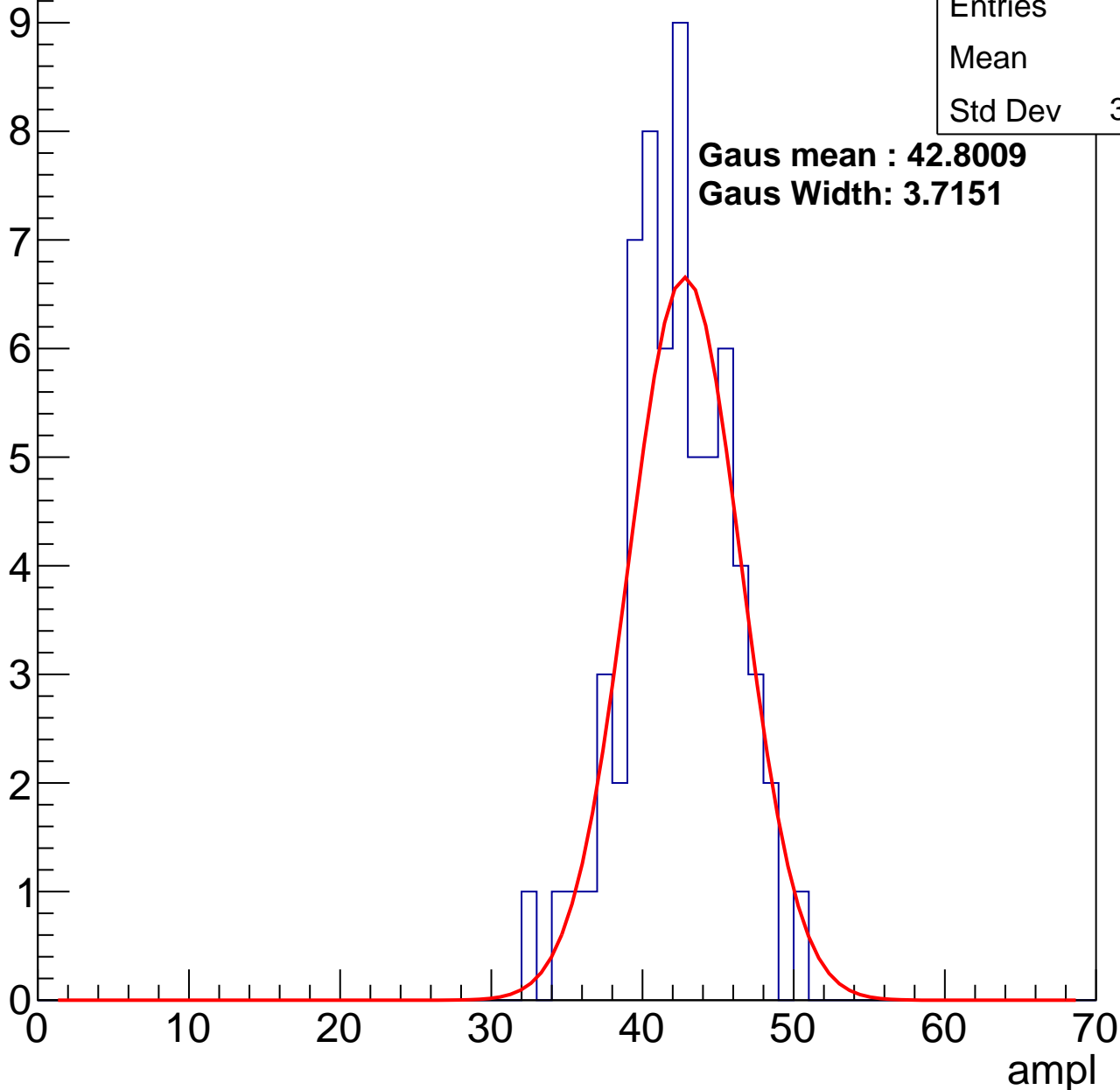
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	41.8
Std Dev	3.527

**Gaus mean : 42.8009**

**Gaus Width: 3.7151**

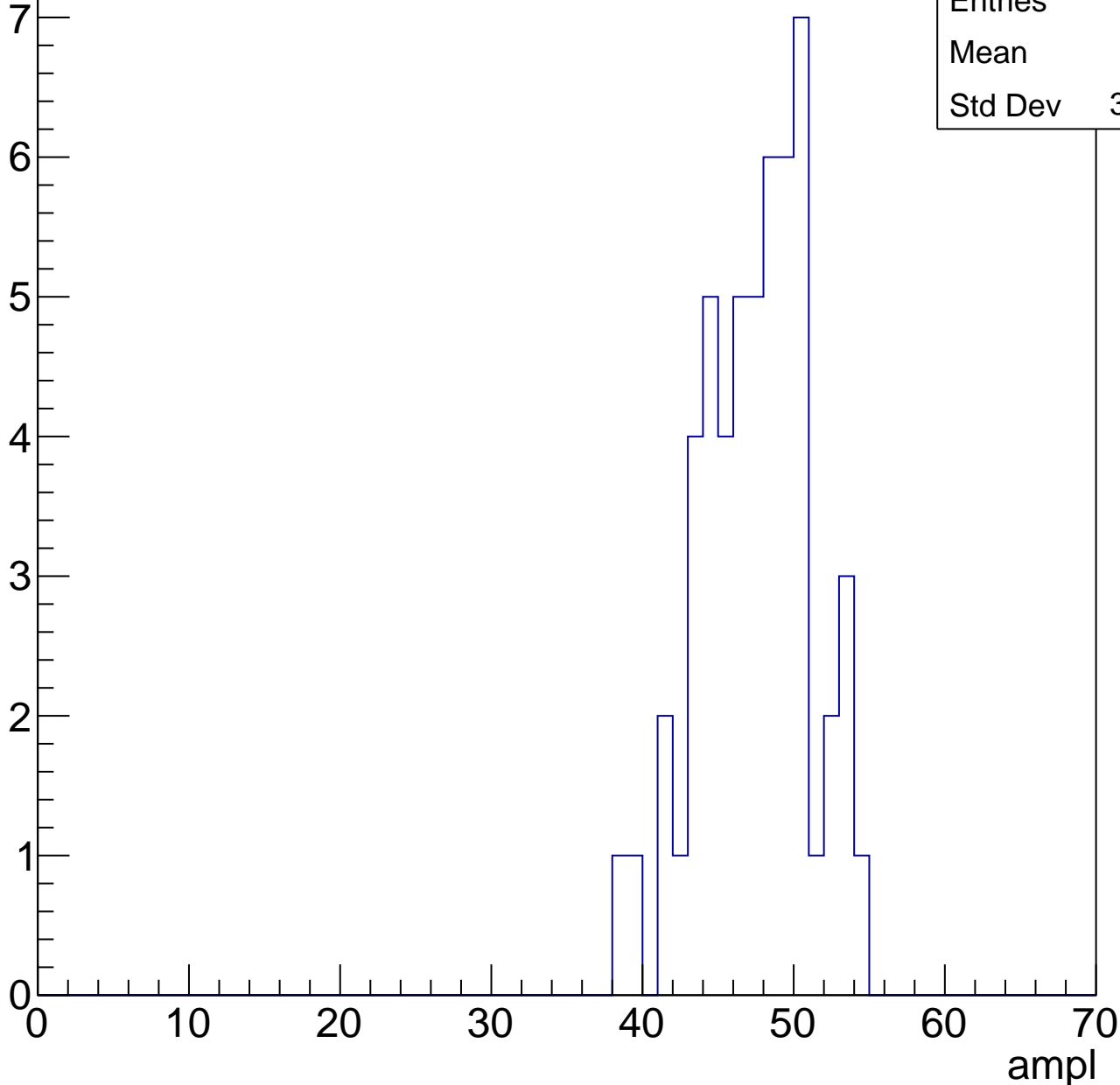


# B1L102S, U5-ch97, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	47
Std Dev	3.569

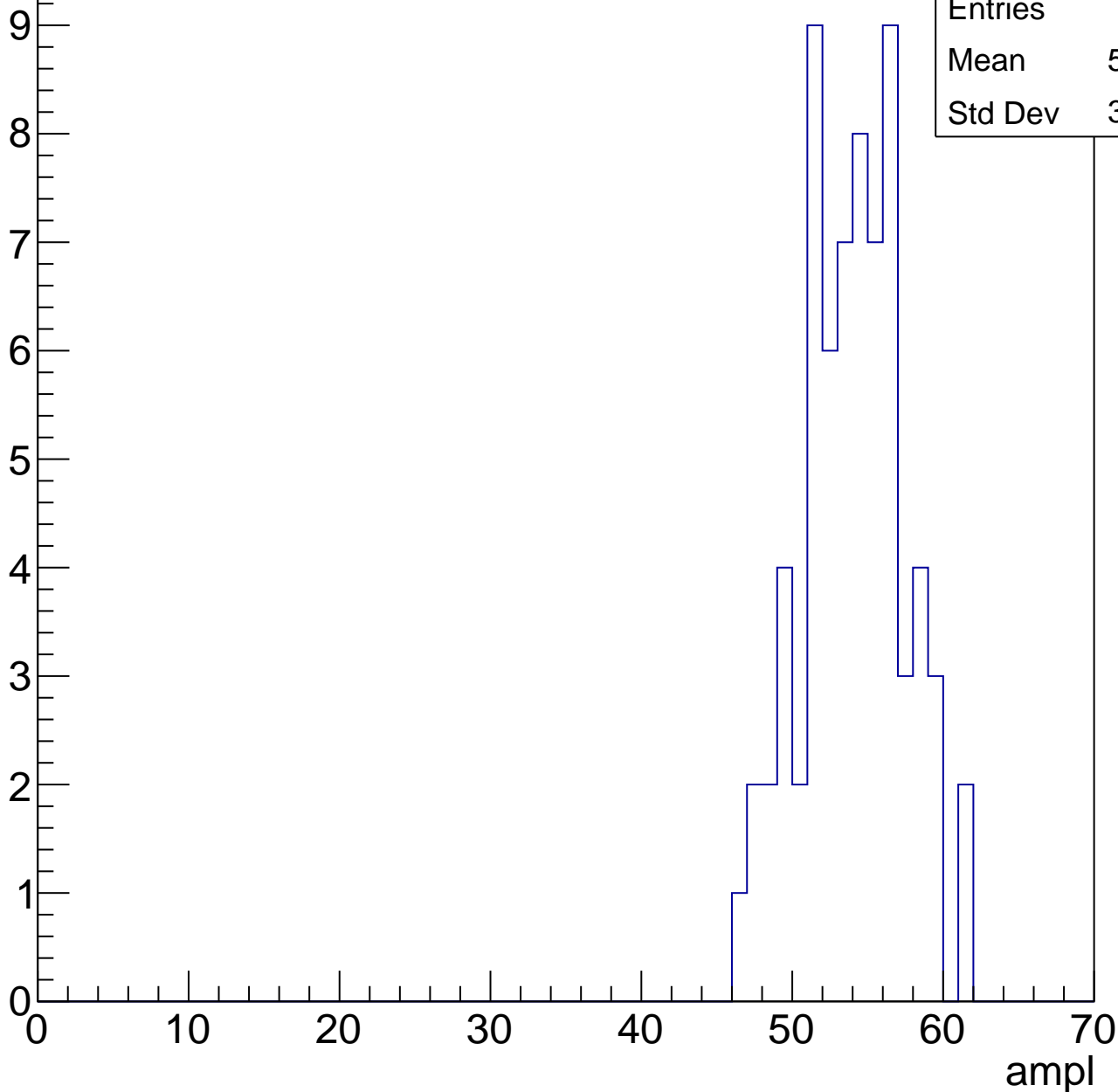


# B1L102S, U5-ch97, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	53.58
Std Dev	3.347

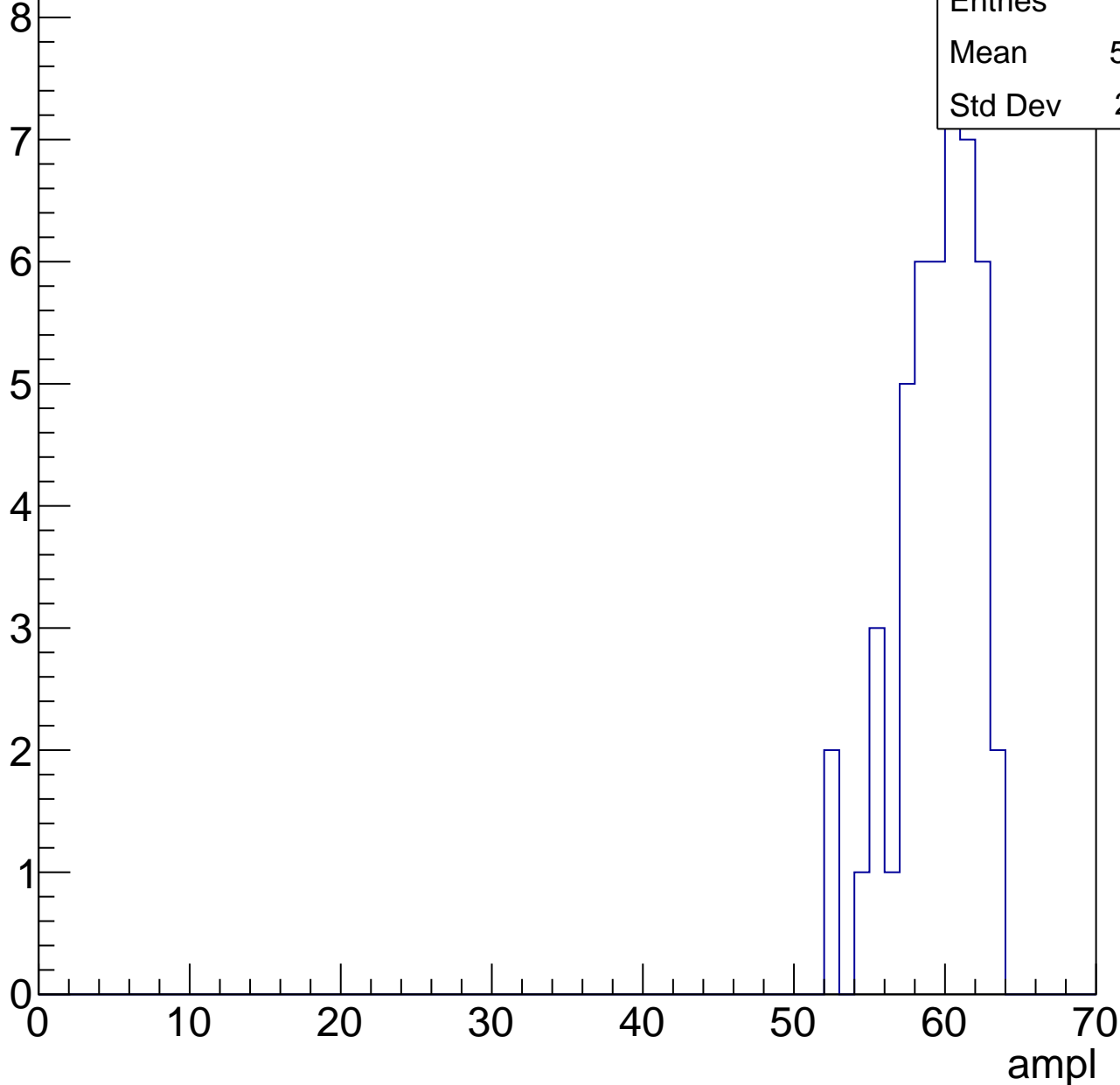


# B1L102S, U5-ch97, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	47
Mean	58.96
Std Dev	2.641

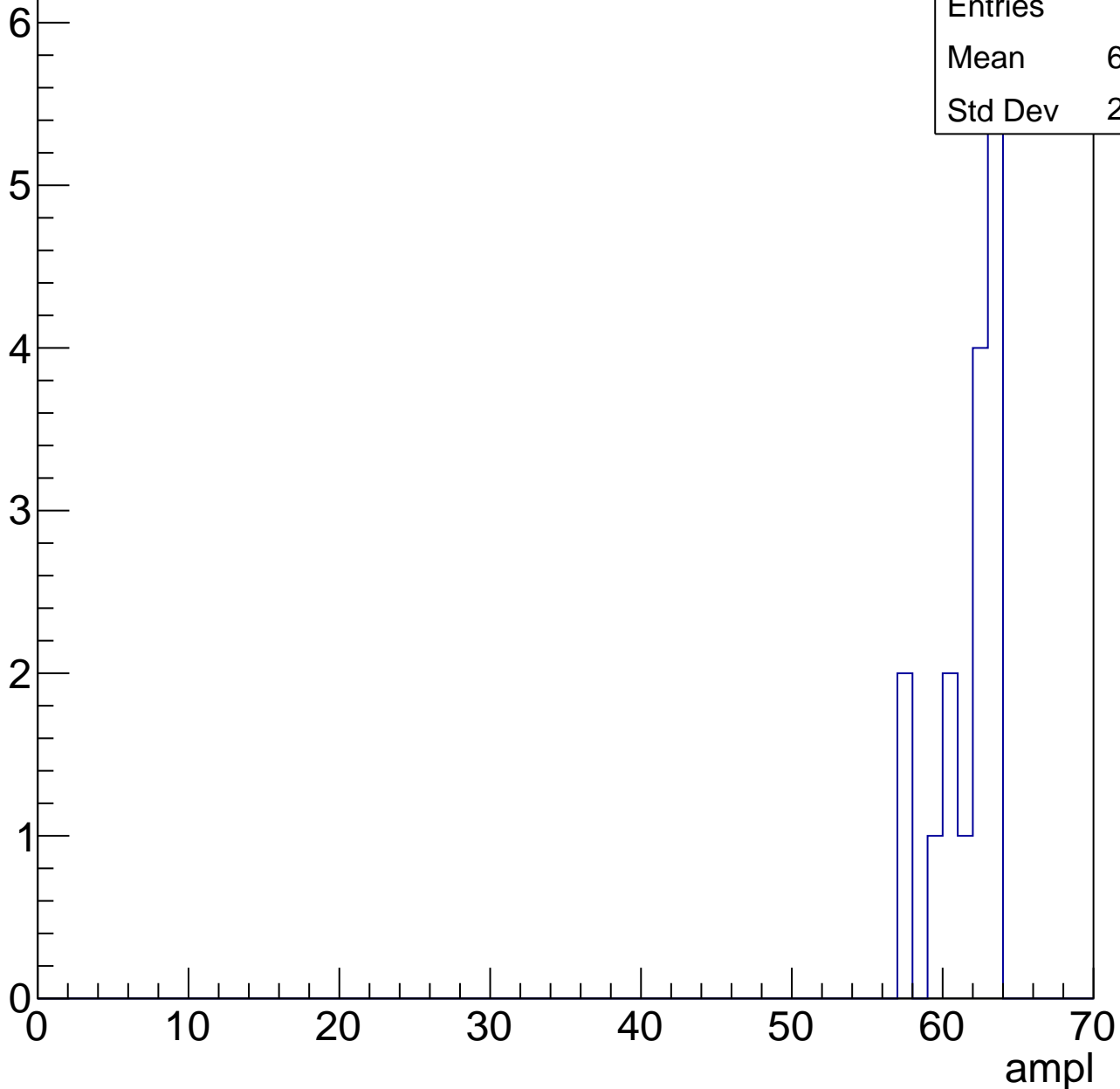


# B1L102S, U5-ch97, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	16
Mean	61.25
Std Dev	2.016





# B1L102S, U5-ch97, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U5-ch98, adc0

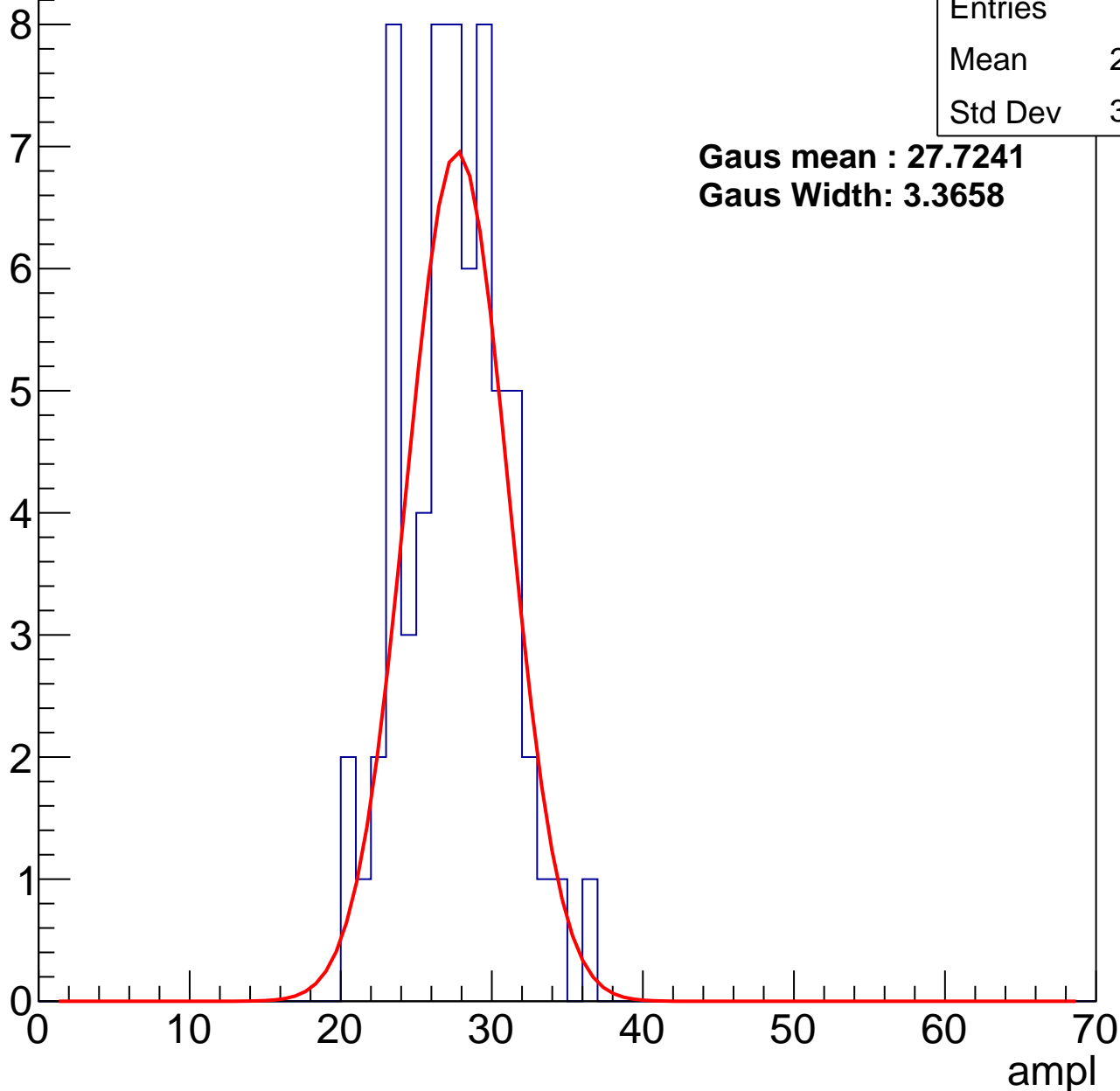
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	27.03
Std Dev	3.379

**Gaus mean : 27.7241**

**Gaus Width: 3.3658**



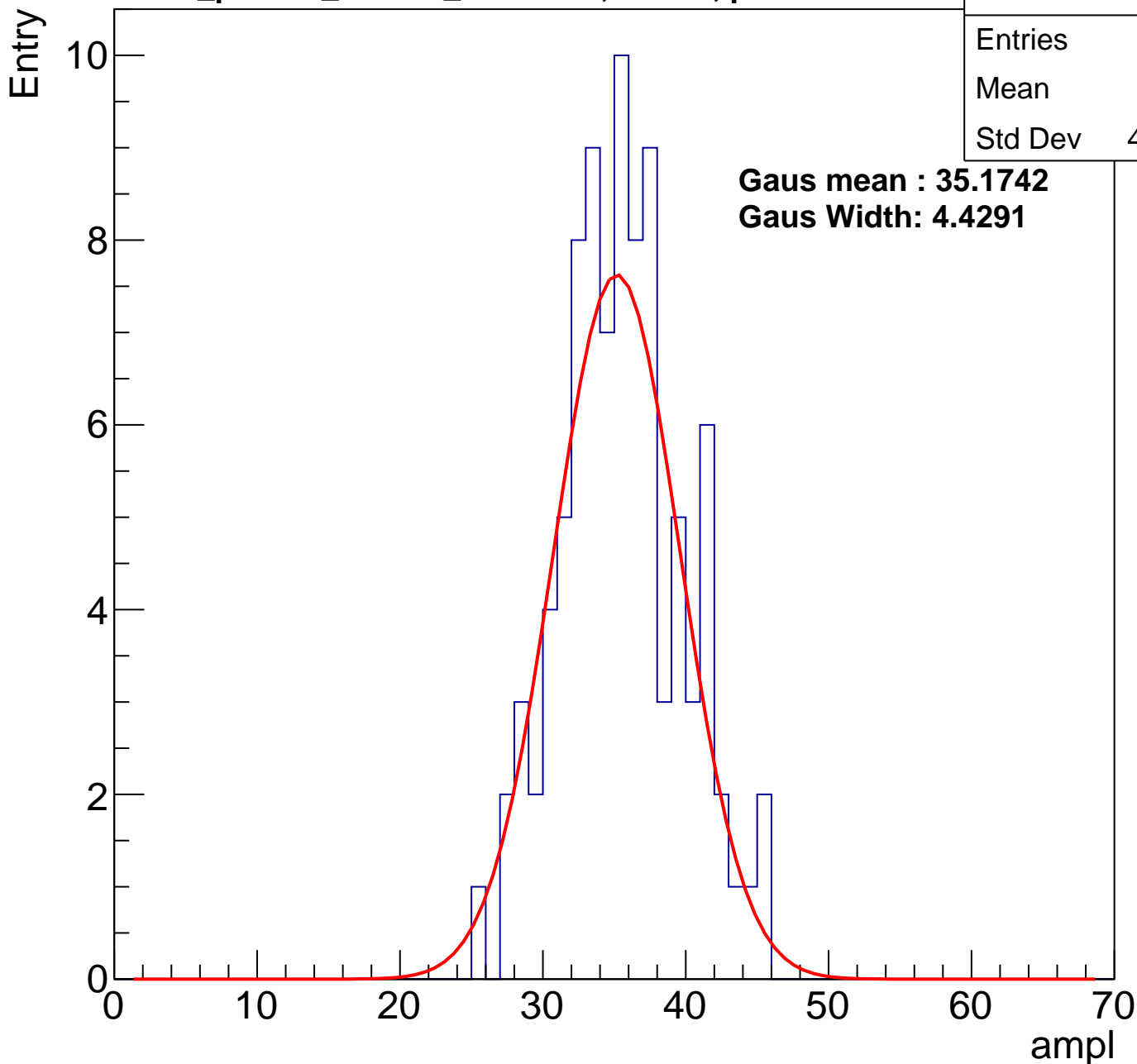
# B1L102S, U5-ch98, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	91
Mean	35.1
Std Dev	4.227

**Gaus mean : 35.1742**

**Gaus Width: 4.4291**



# B1L102S, U5-ch98, adc2

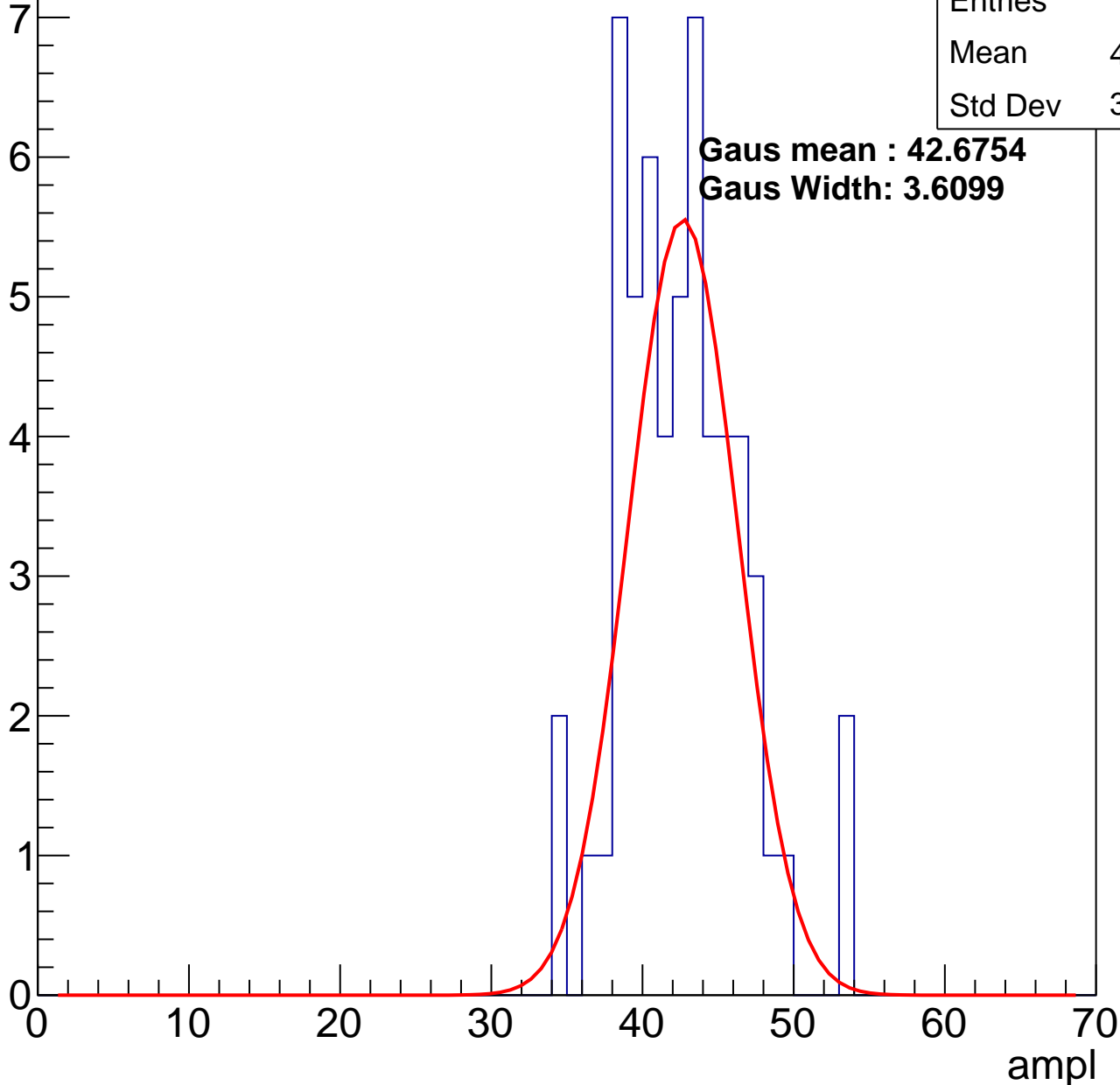
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	42.12
Std Dev	3.969

**Gaus mean : 42.6754**

**Gaus Width: 3.6099**

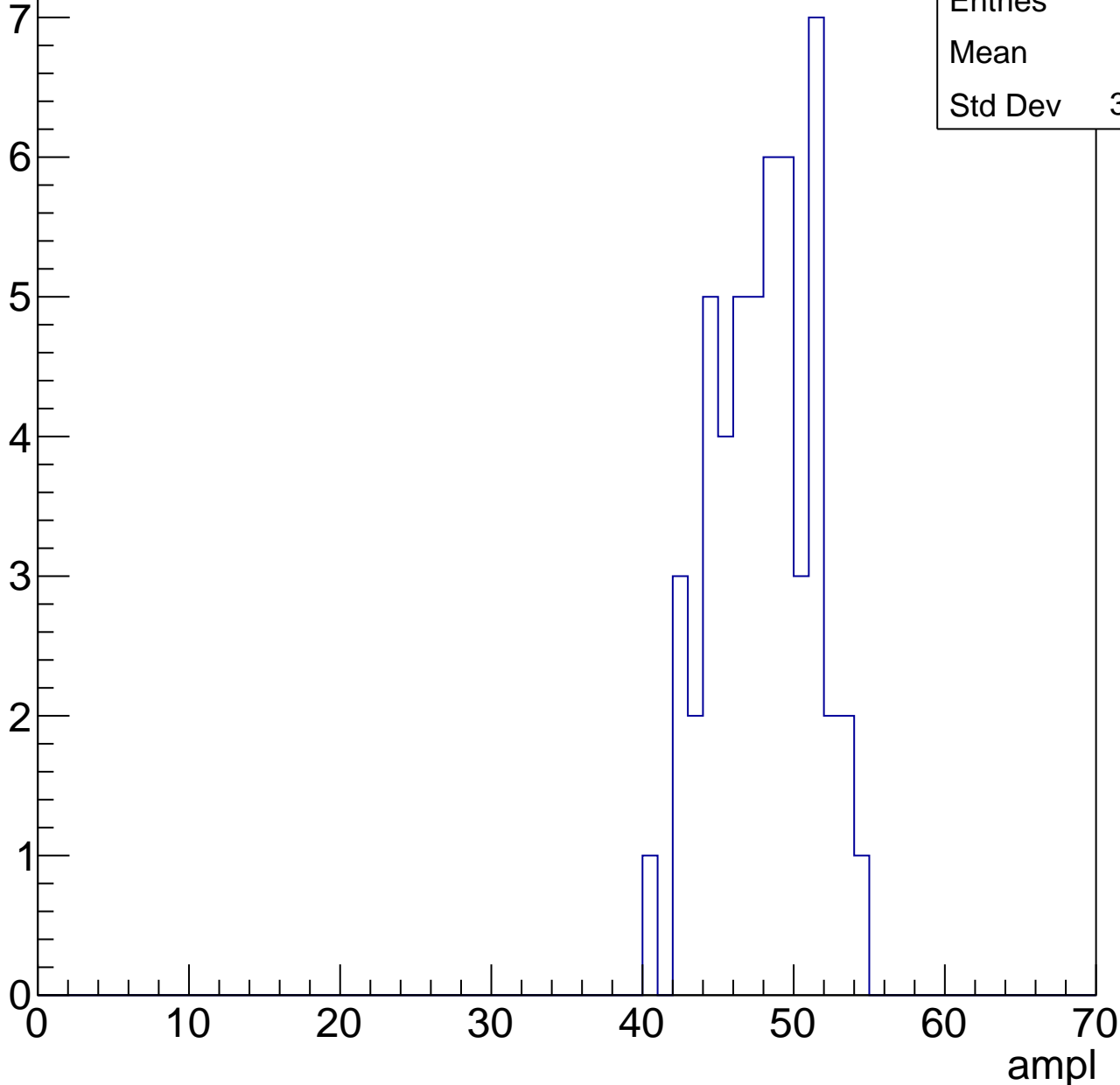


# B1L102S, U5-ch98, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

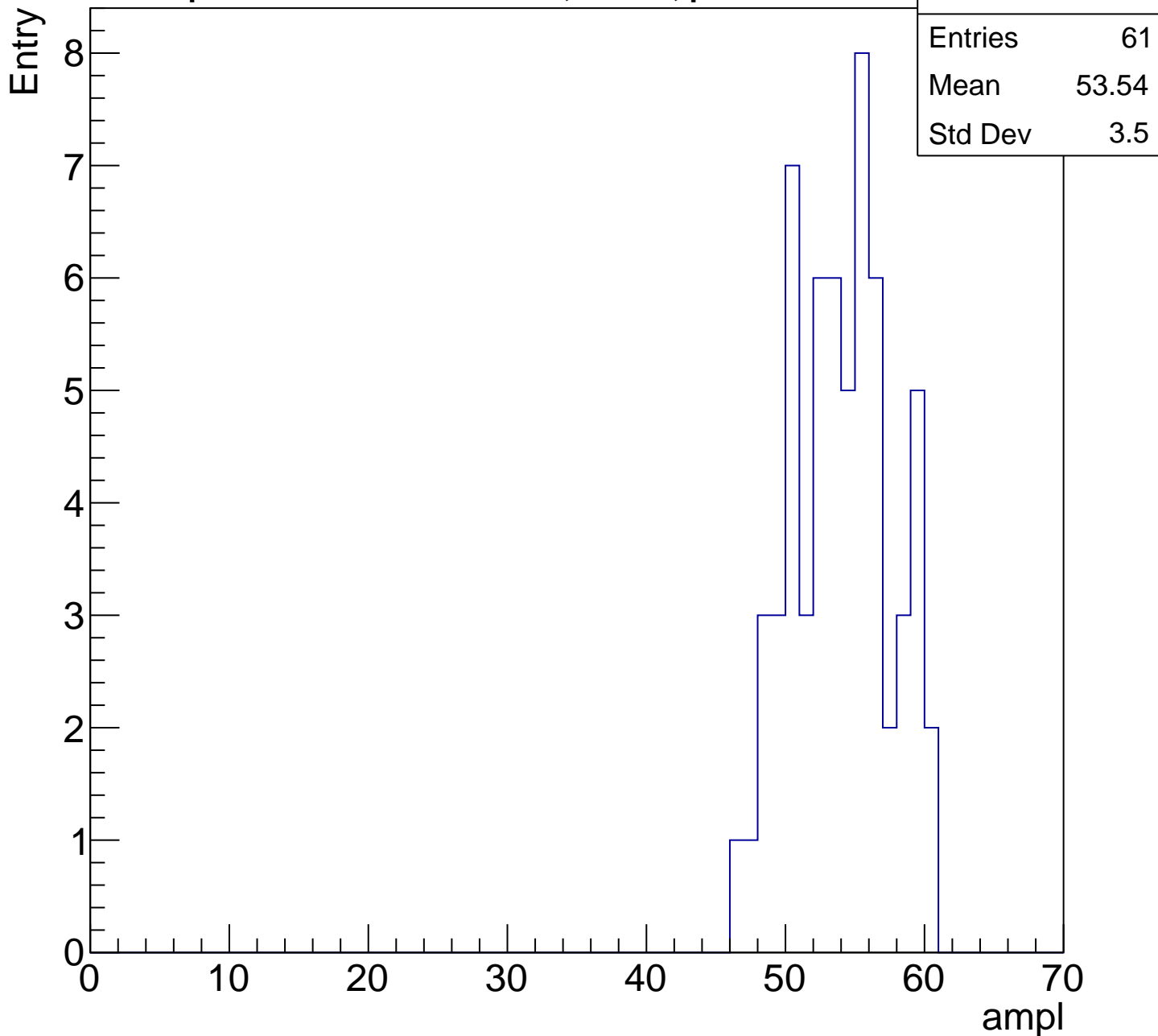
Entry

Entries	52
Mean	47.5
Std Dev	3.249



# B1L102S, U5-ch98, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

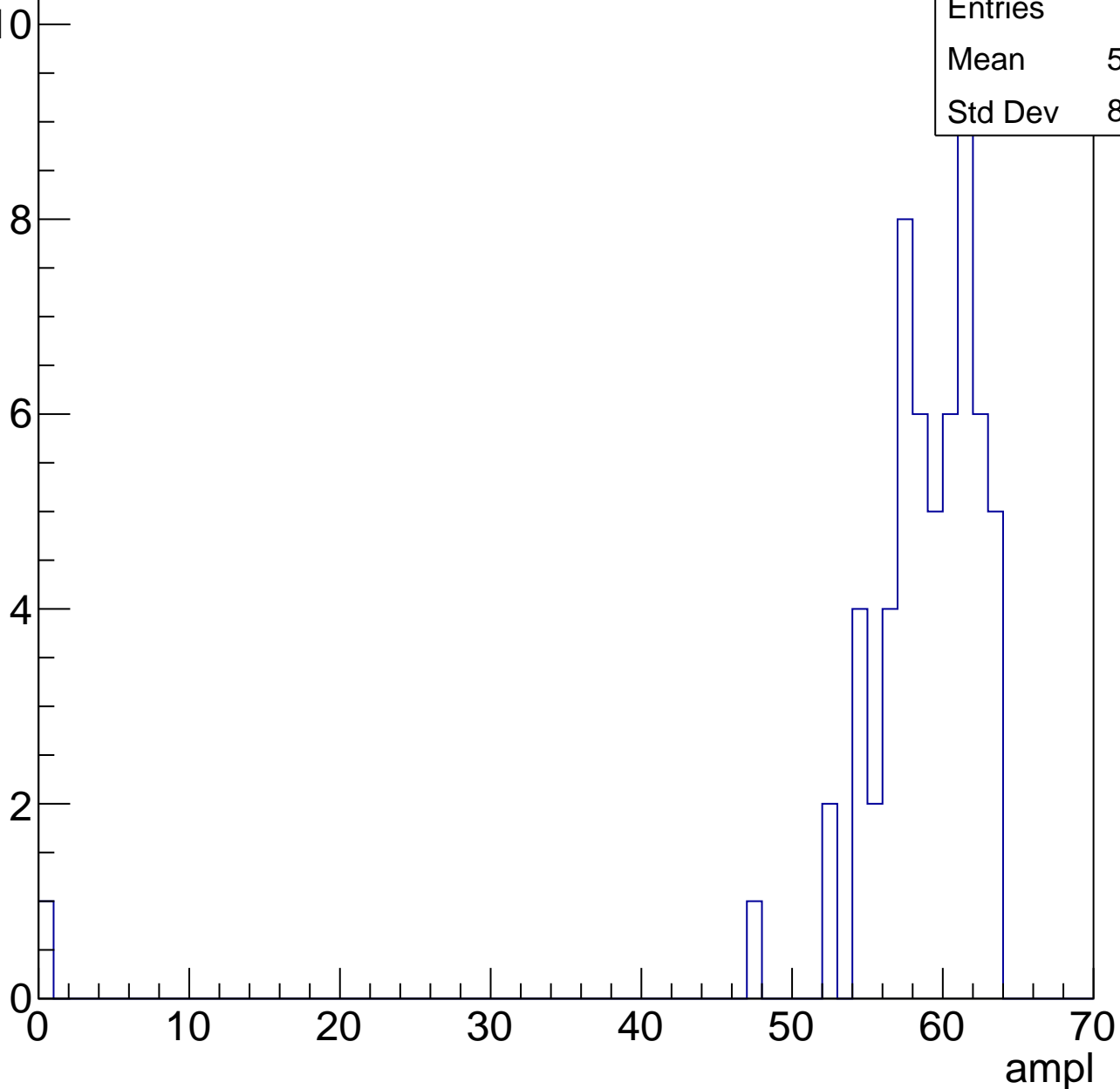


# B1L102S, U5-ch98, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	57.62
Std Dev	8.159

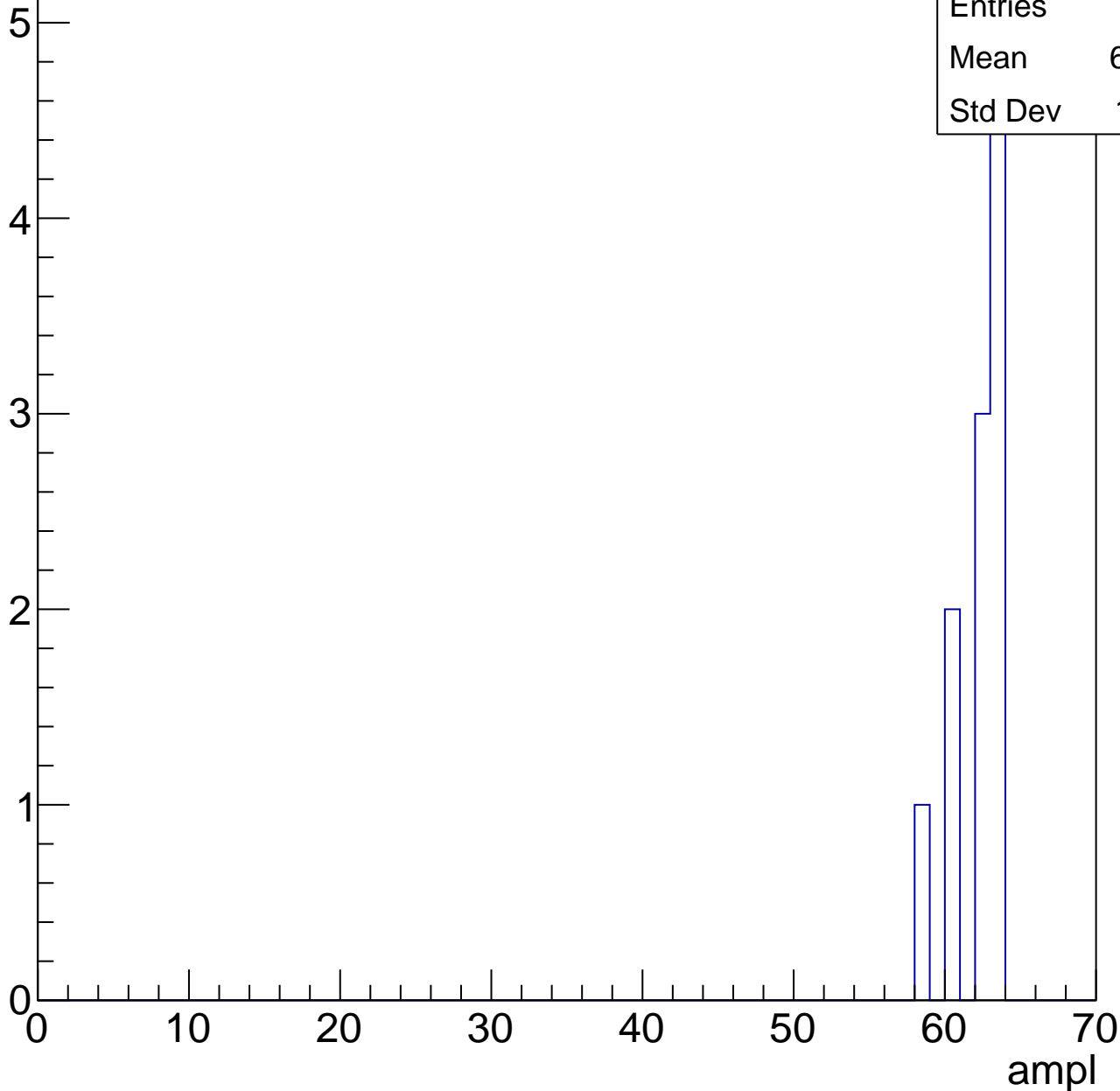


# B1L102S, U5-ch98, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	11
Mean	61.73
Std Dev	1.601

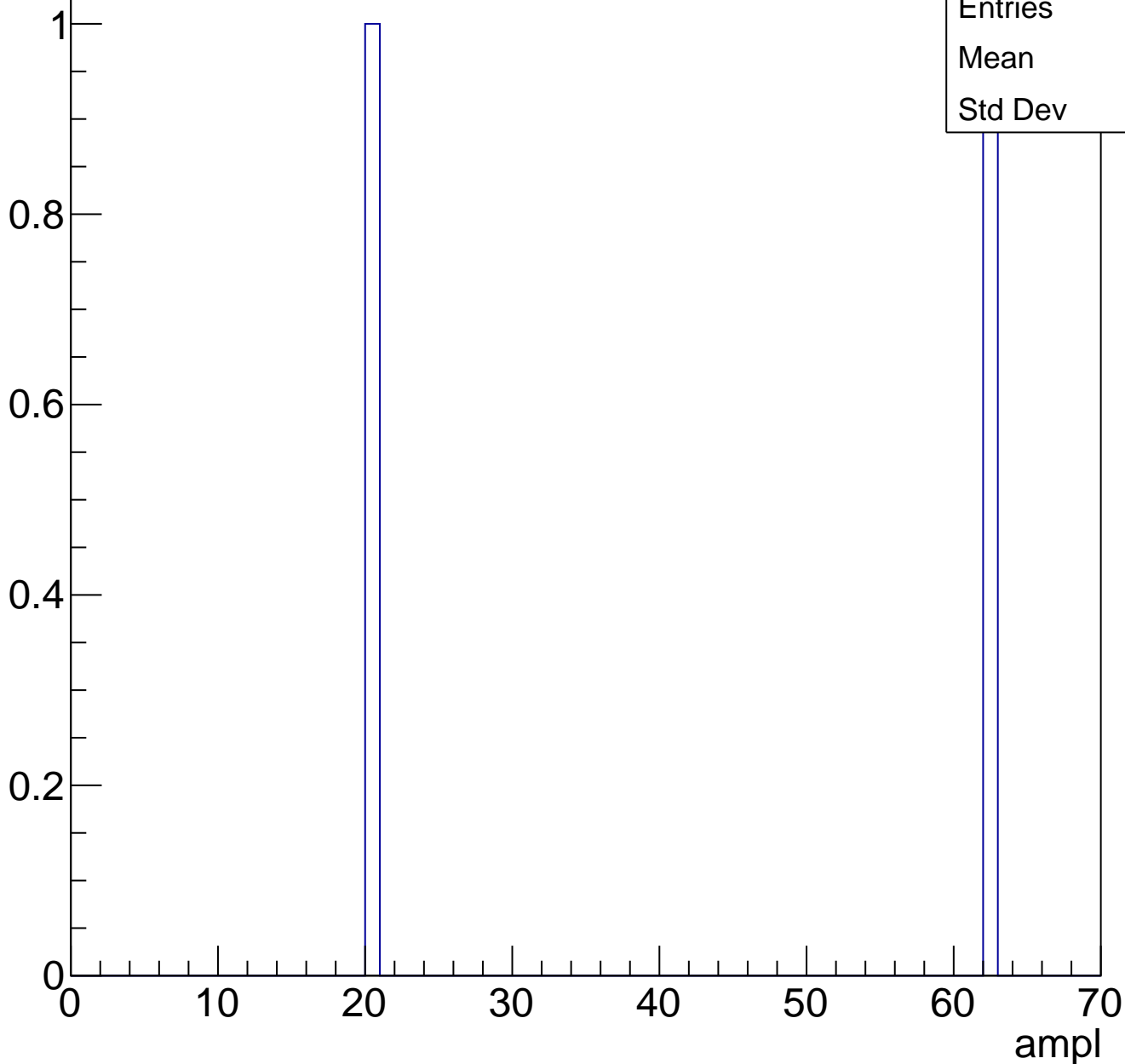




# B1L102S, U5-ch98, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U5-ch99, adc0

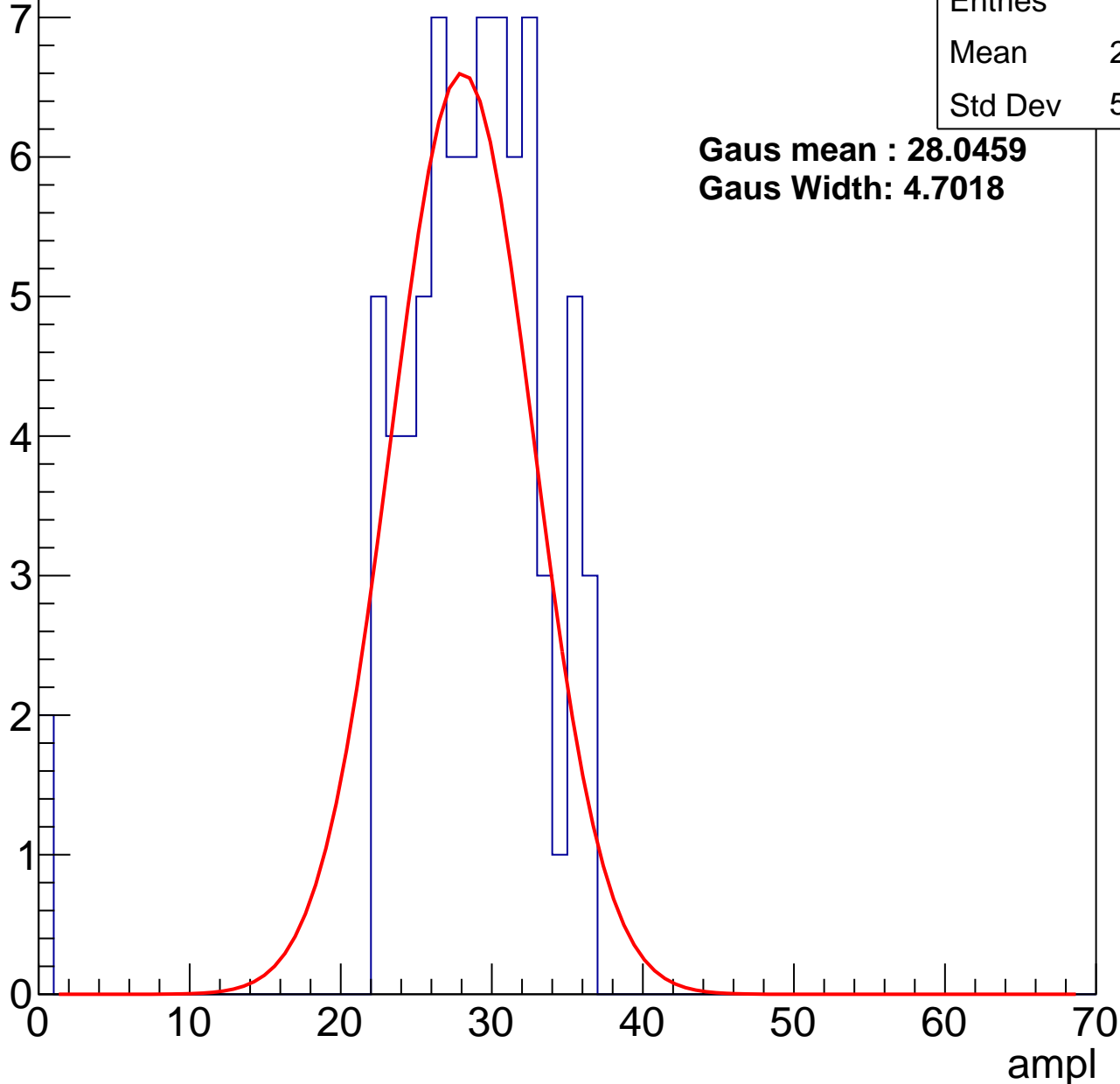
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	78
Mean	27.87
Std Dev	5.926

**Gaus mean : 28.0459**

**Gaus Width: 4.7018**



# B1L102S, U5-ch99, adc1

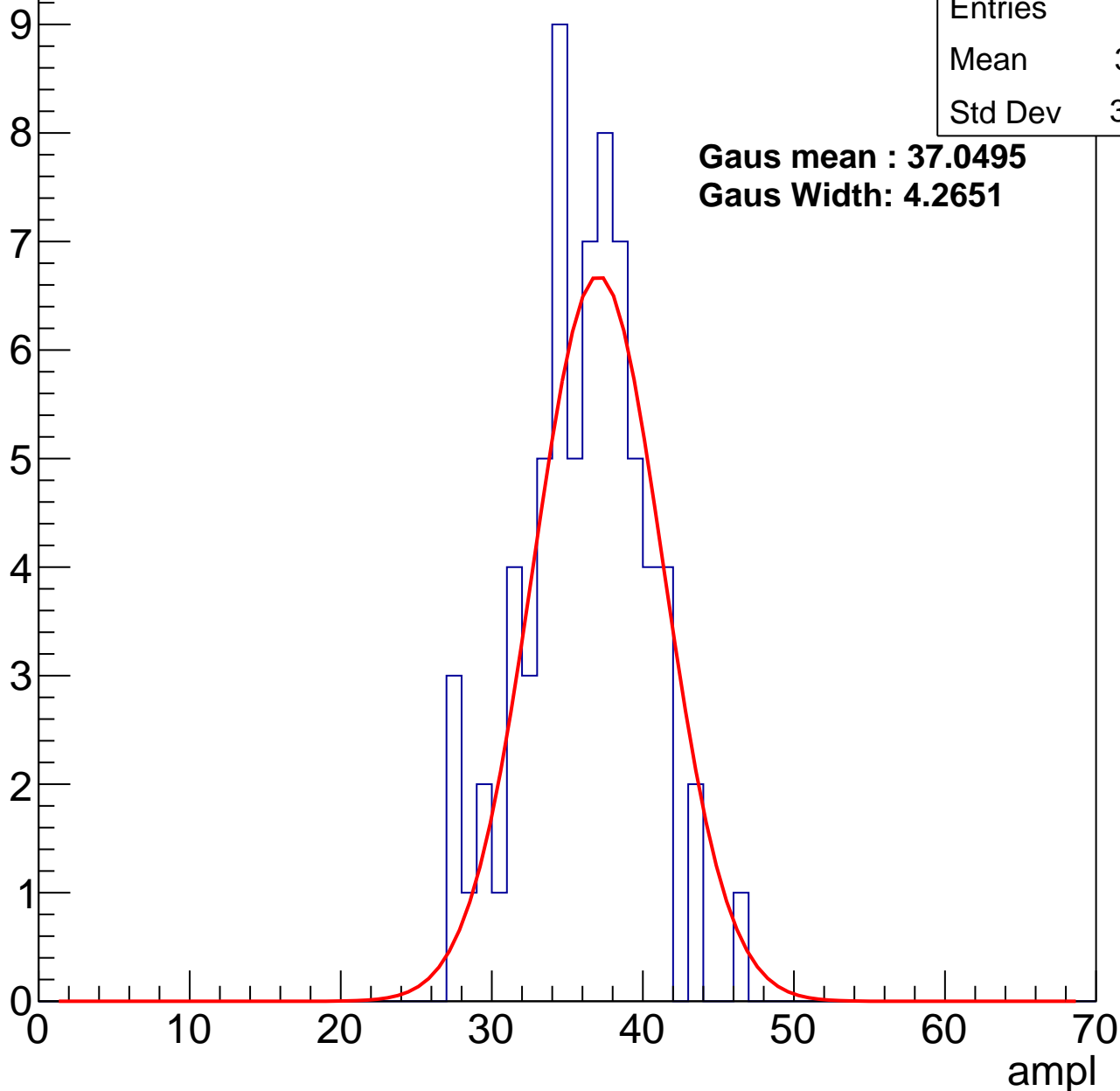
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	35.61
Std Dev	3.949

**Gaus mean : 37.0495**

**Gaus Width: 4.2651**



# B1L102S, U5-ch99, adc2

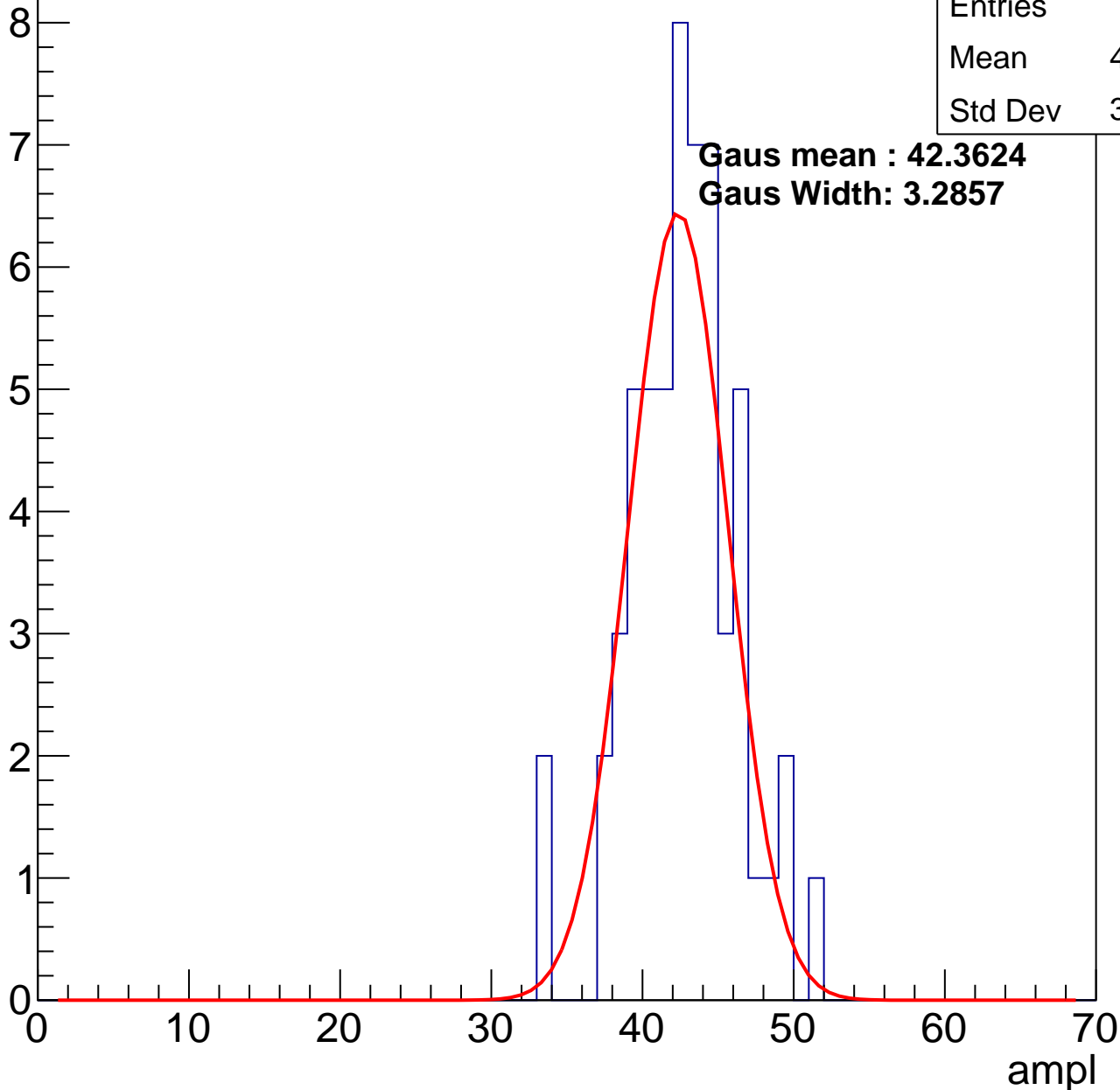
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	42.25
Std Dev	3.526

**Gaus mean : 42.3624**

**Gaus Width: 3.2857**

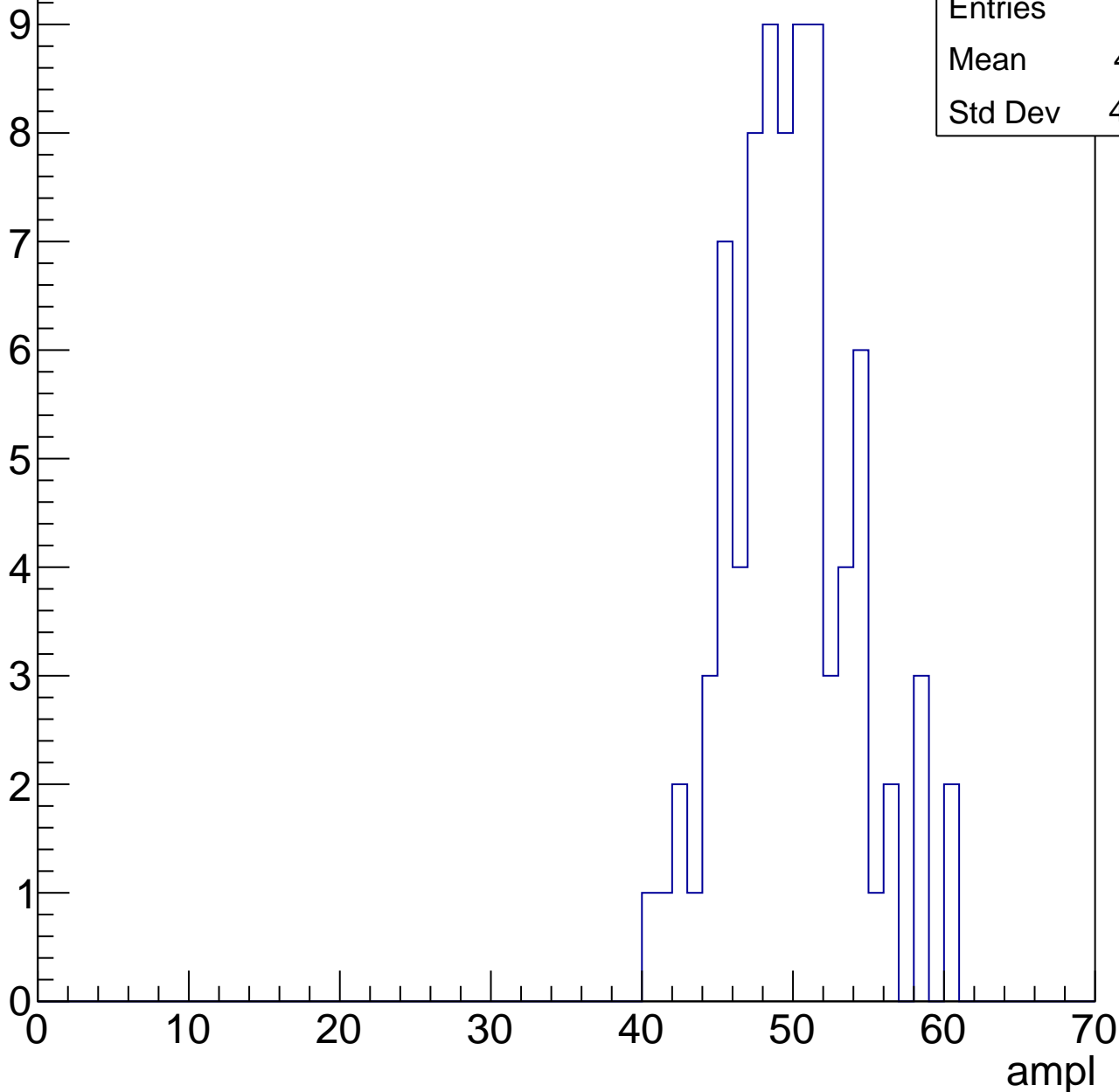


# B1L102S, U5-ch99, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	83
Mean	49.41
Std Dev	4.157

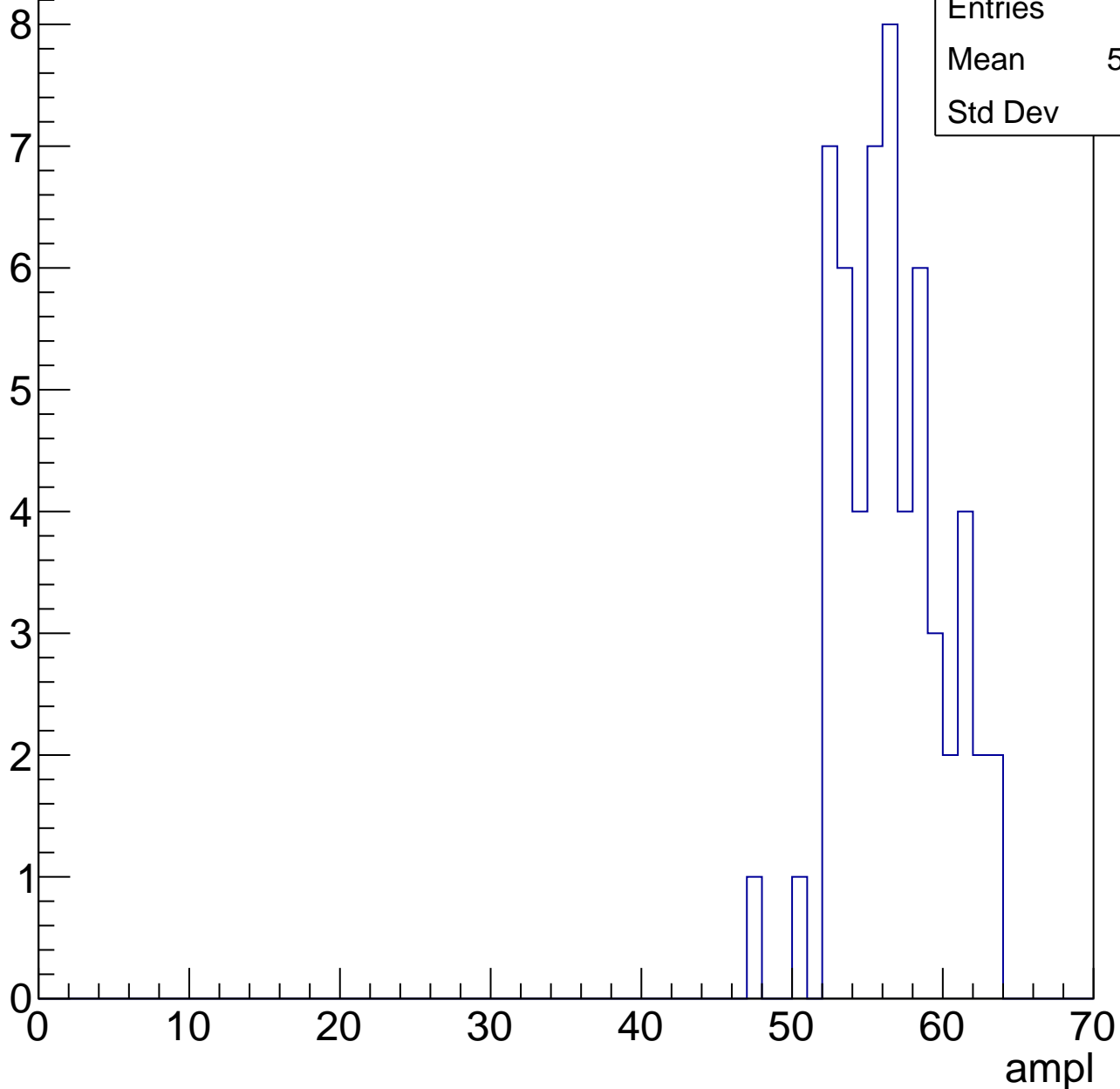


# B1L102S, U5-ch99, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	56.05
Std Dev	3.41



# B1L102S, U5-ch99, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

6

5

4

3

2

1

0

0

10

20

30

40

50

60

70

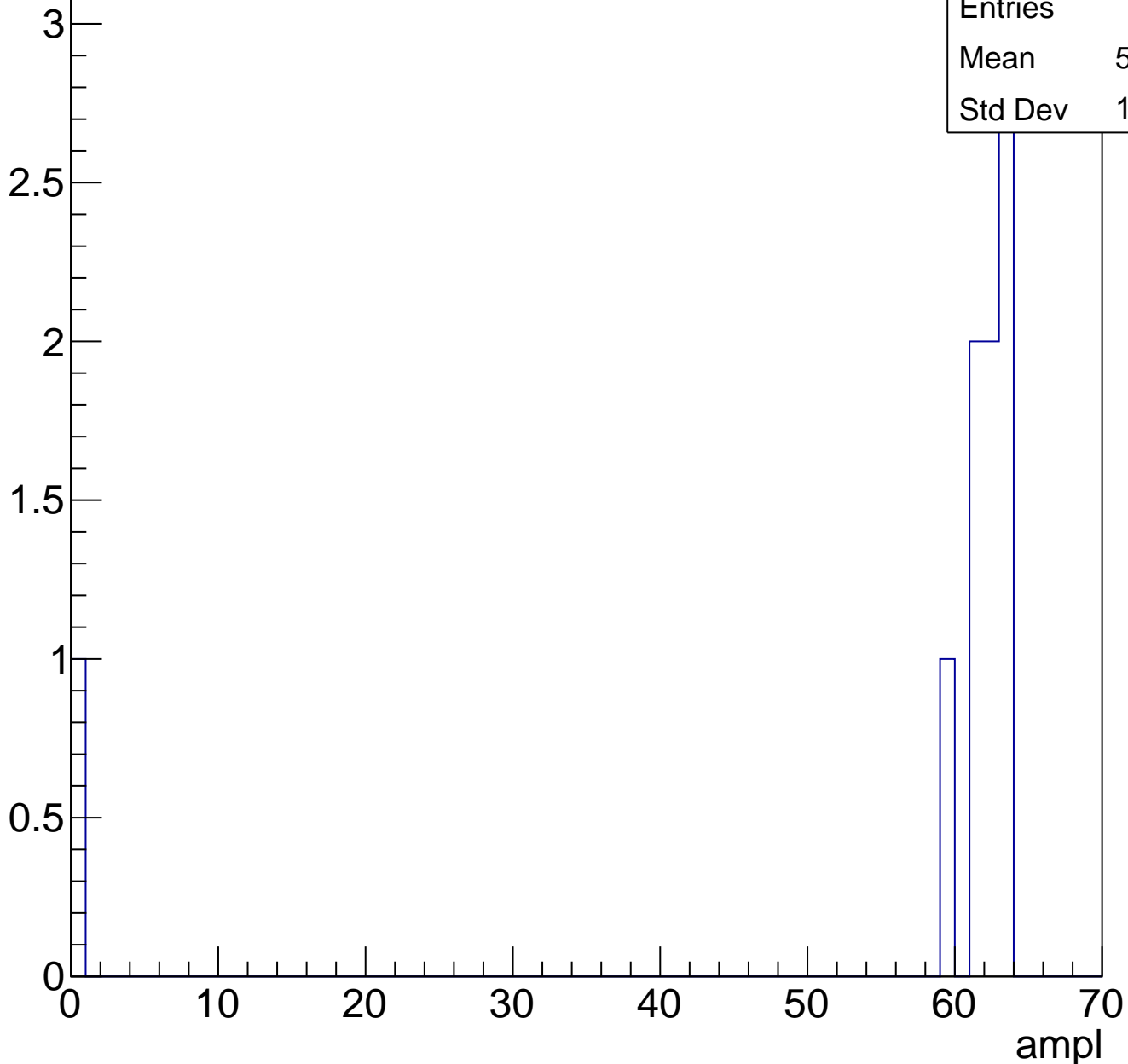
ampl

Entries	36
Mean	59.86
Std Dev	2.275

# B1L102S, U5-ch99, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	9
Mean	54.89
Std Dev	19.44



# B1L102S, U5-ch99, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L102S, U5-ch100, adc0

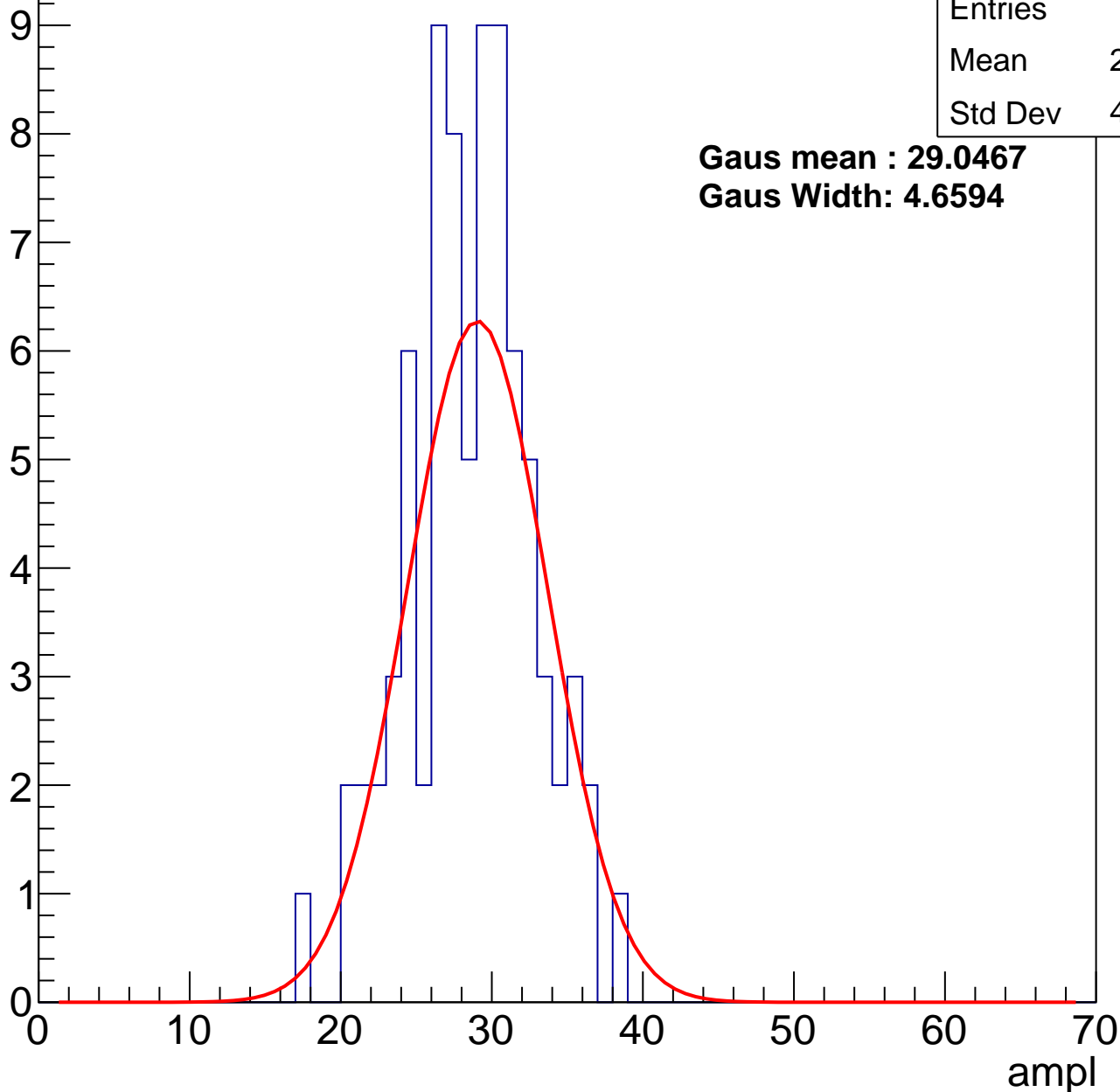
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	80
Mean	28.19
Std Dev	4.108

**Gaus mean : 29.0467**

**Gaus Width: 4.6594**



# B1L102S, U5-ch100, adc1

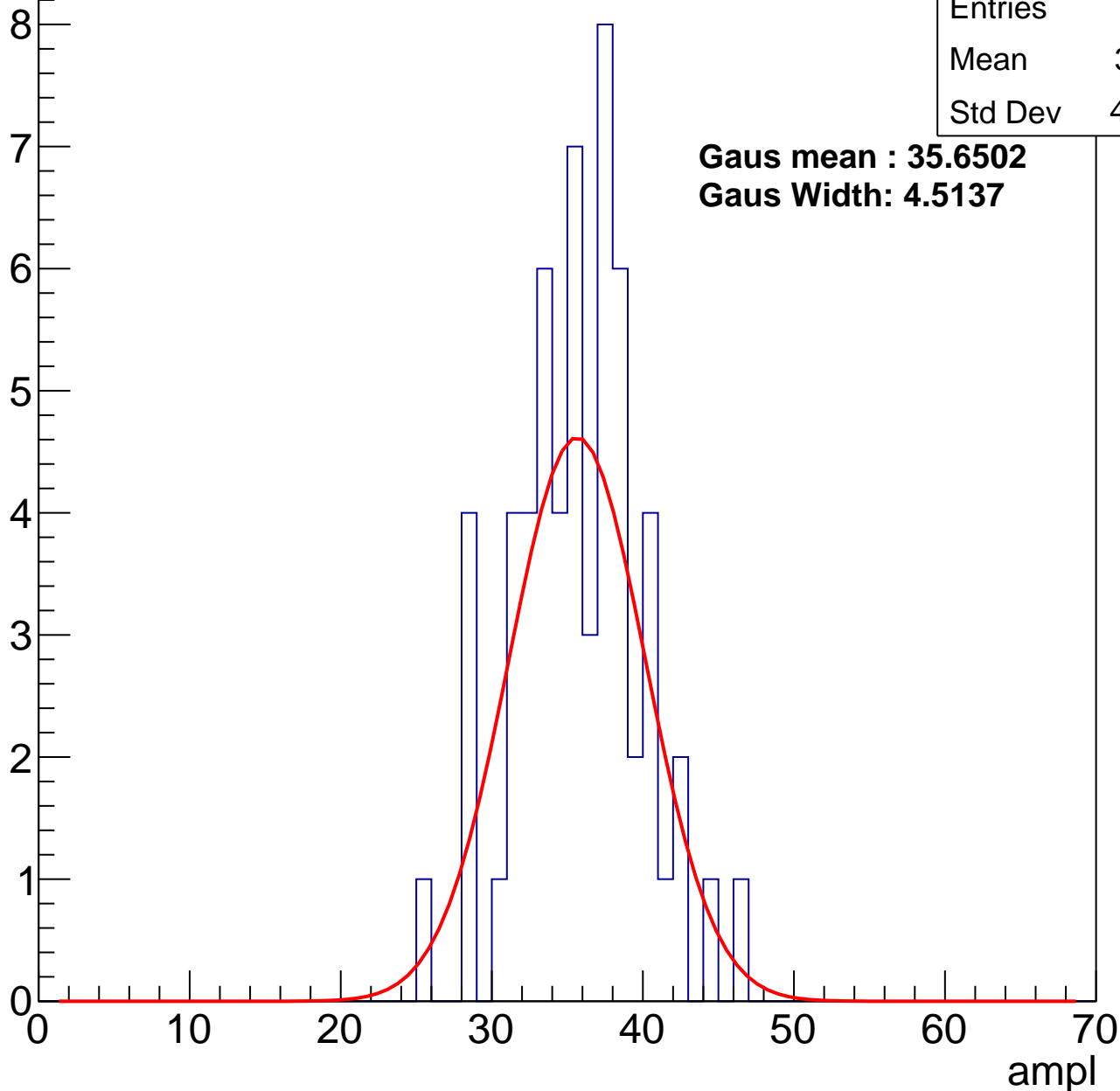
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	35.31
Std Dev	4.118

**Gaus mean : 35.6502**

**Gaus Width: 4.5137**



# B1L102S, U5-ch100, adc2

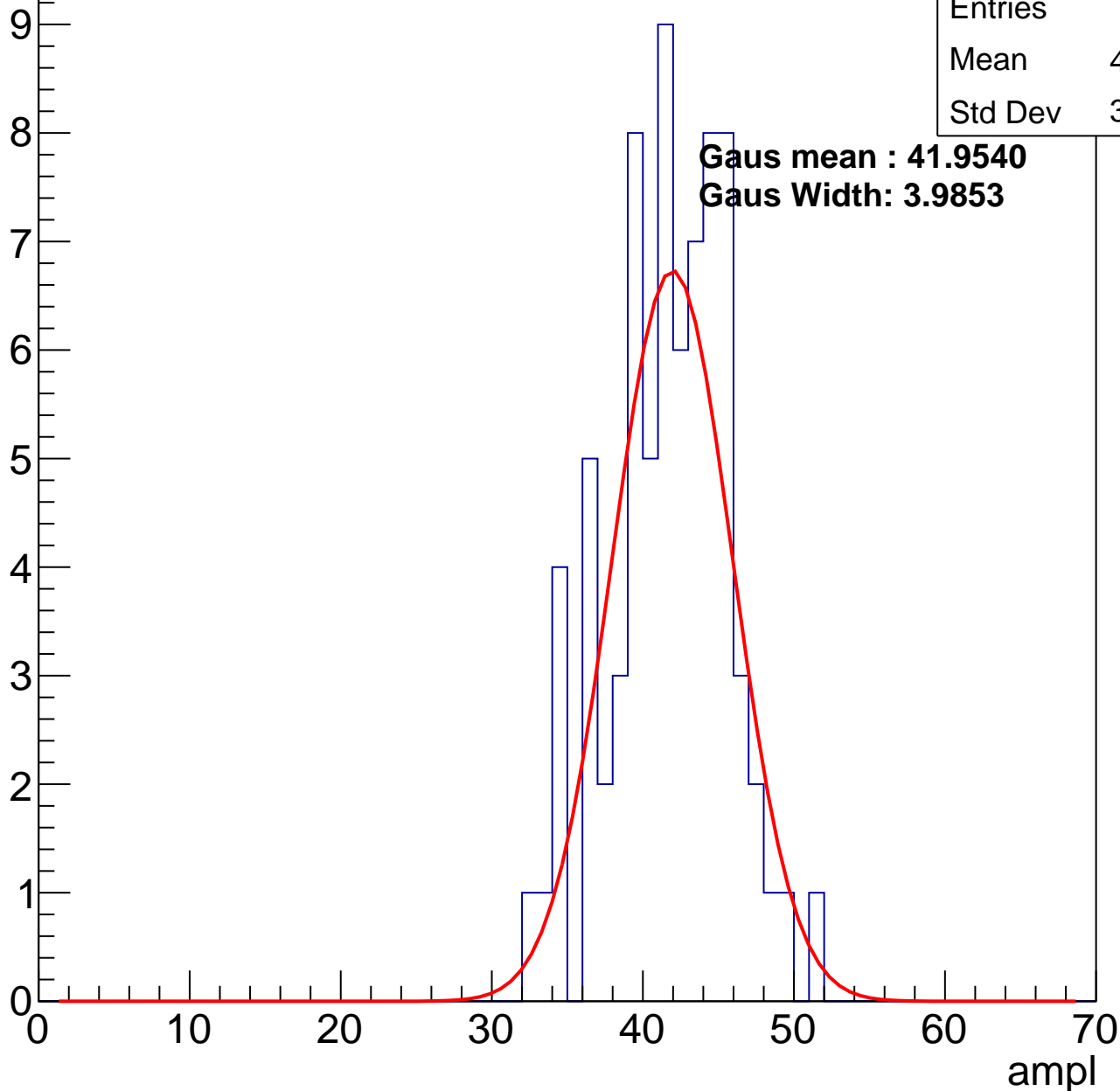
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	41.27
Std Dev	3.917

**Gaus mean : 41.9540**

**Gaus Width: 3.9853**

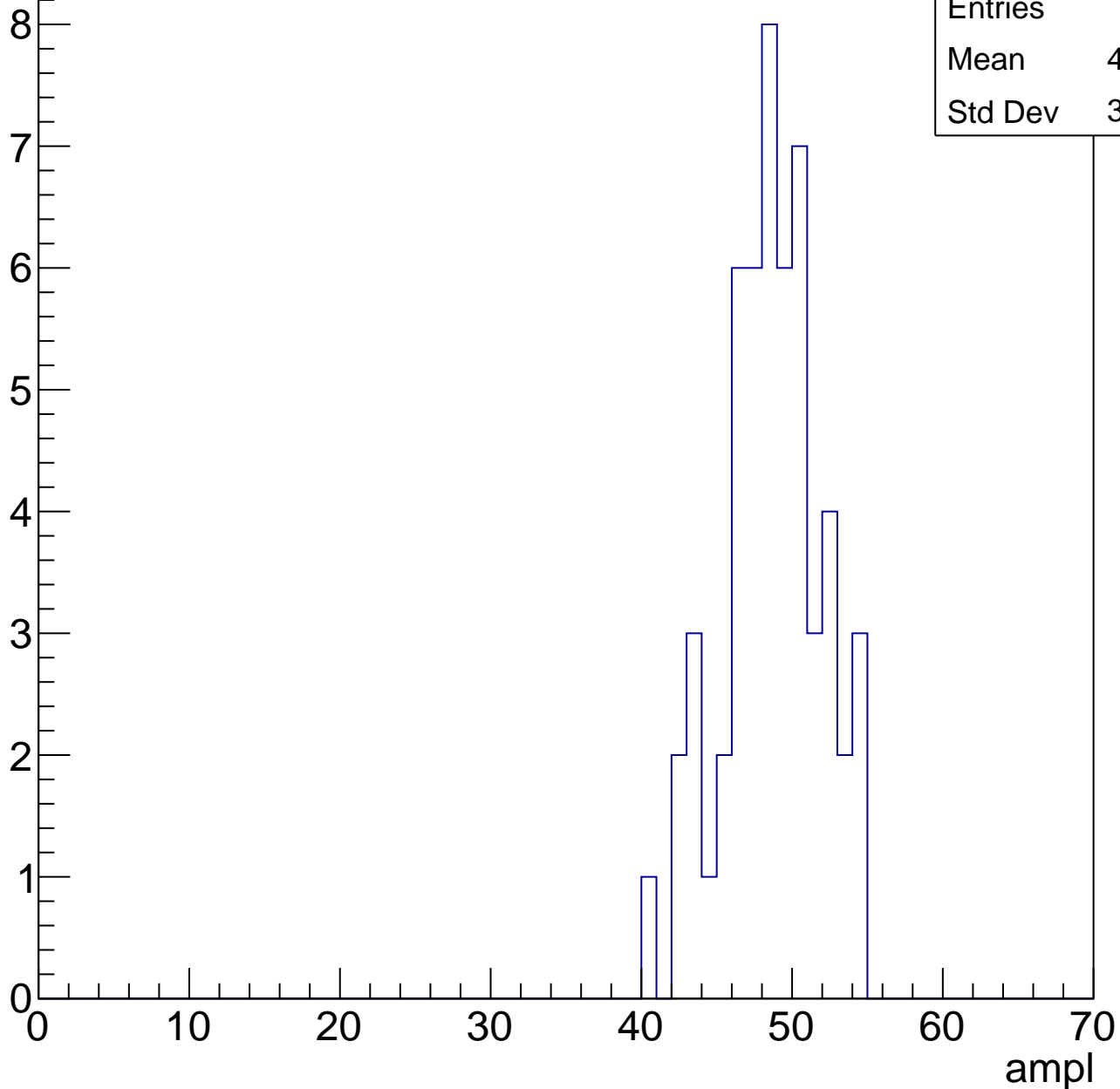


# B1L102S, U5-ch100, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

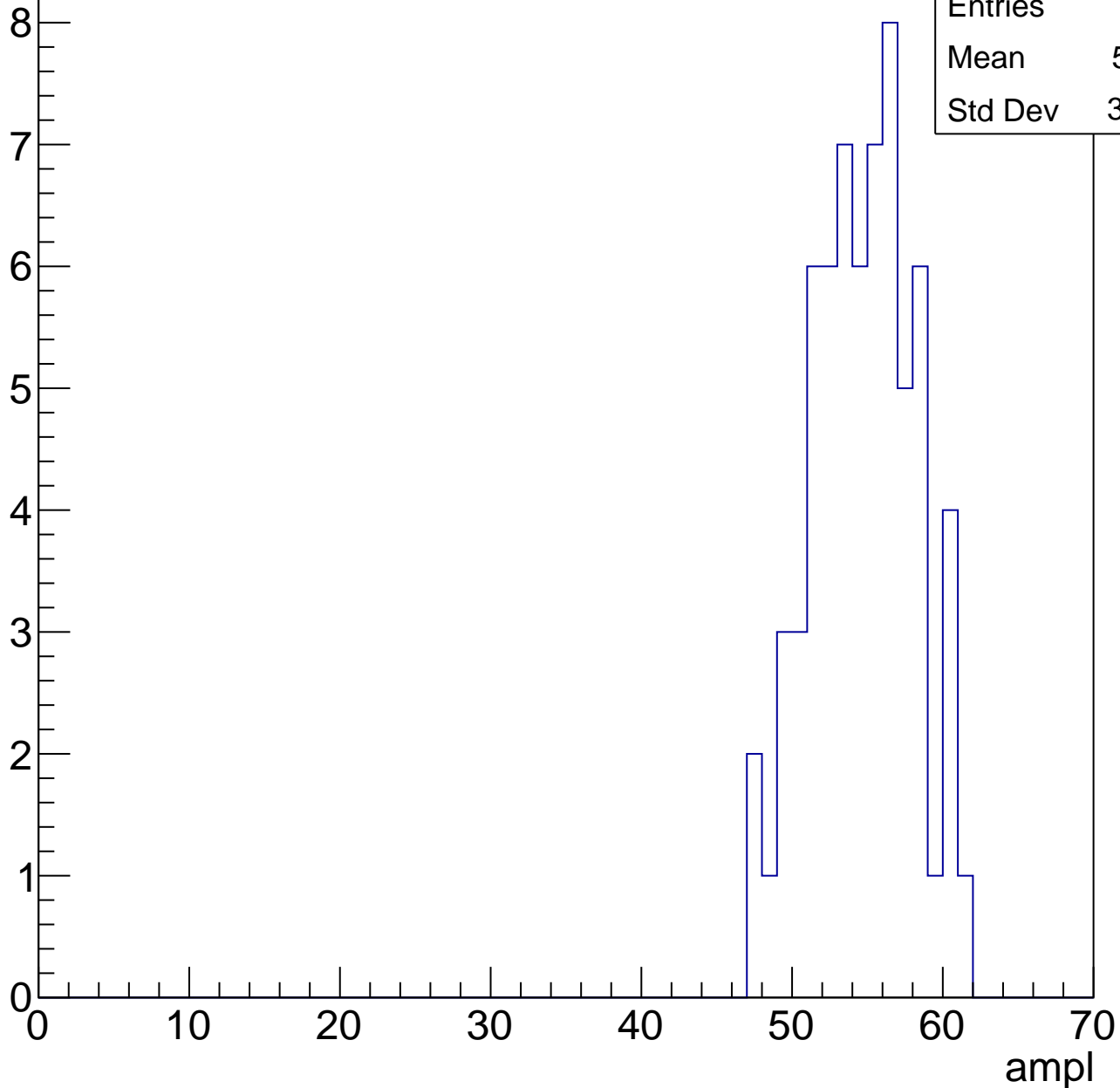
Entries	54
Mean	48.19
Std Dev	3.209



# B1L102S, U5-ch100, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	66
Mean	54.21
Std Dev	3.342

# B1L102S, U5-ch100, adc5

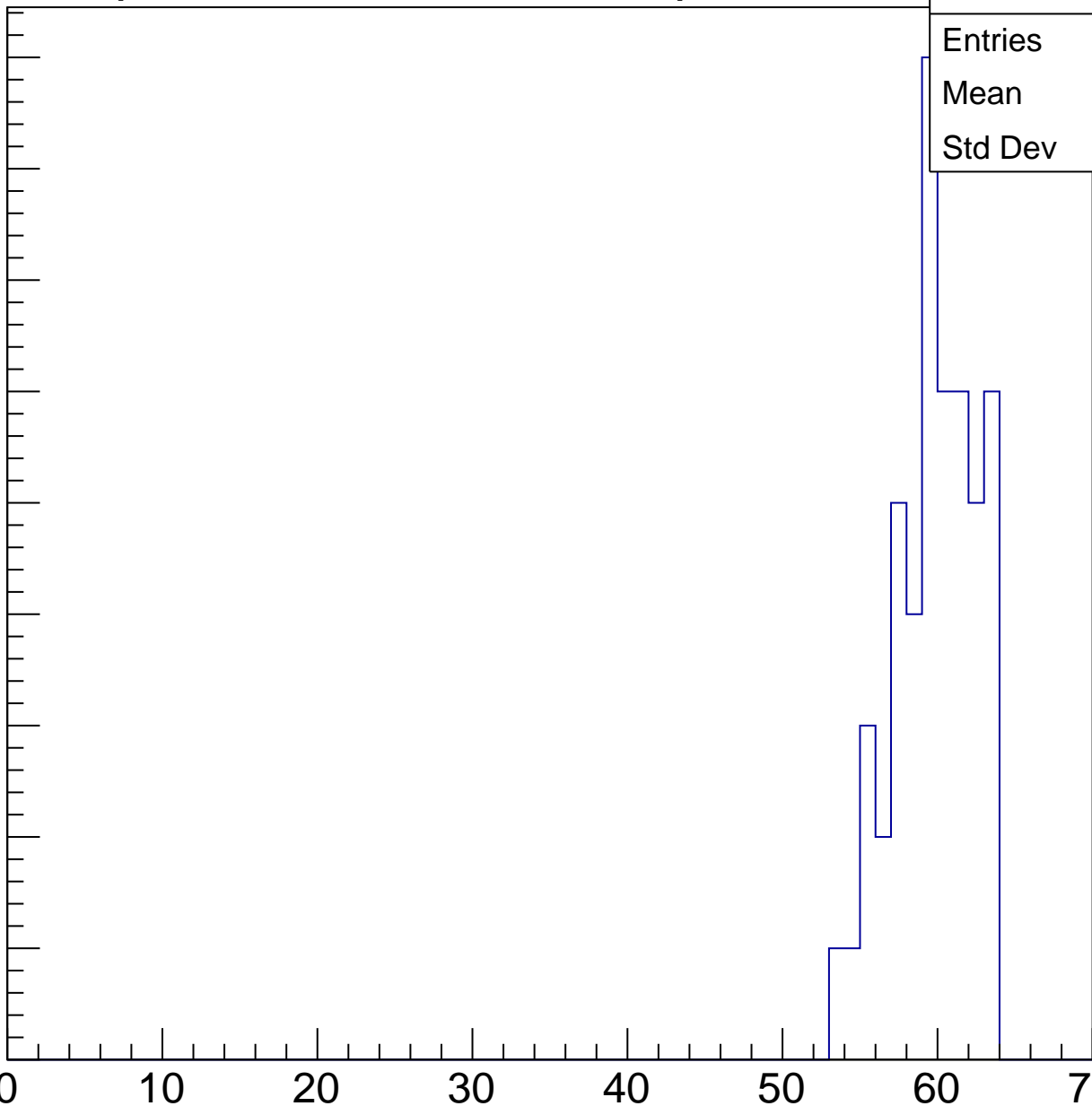
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	48
Mean	59.29
Std Dev	2.574

ampl

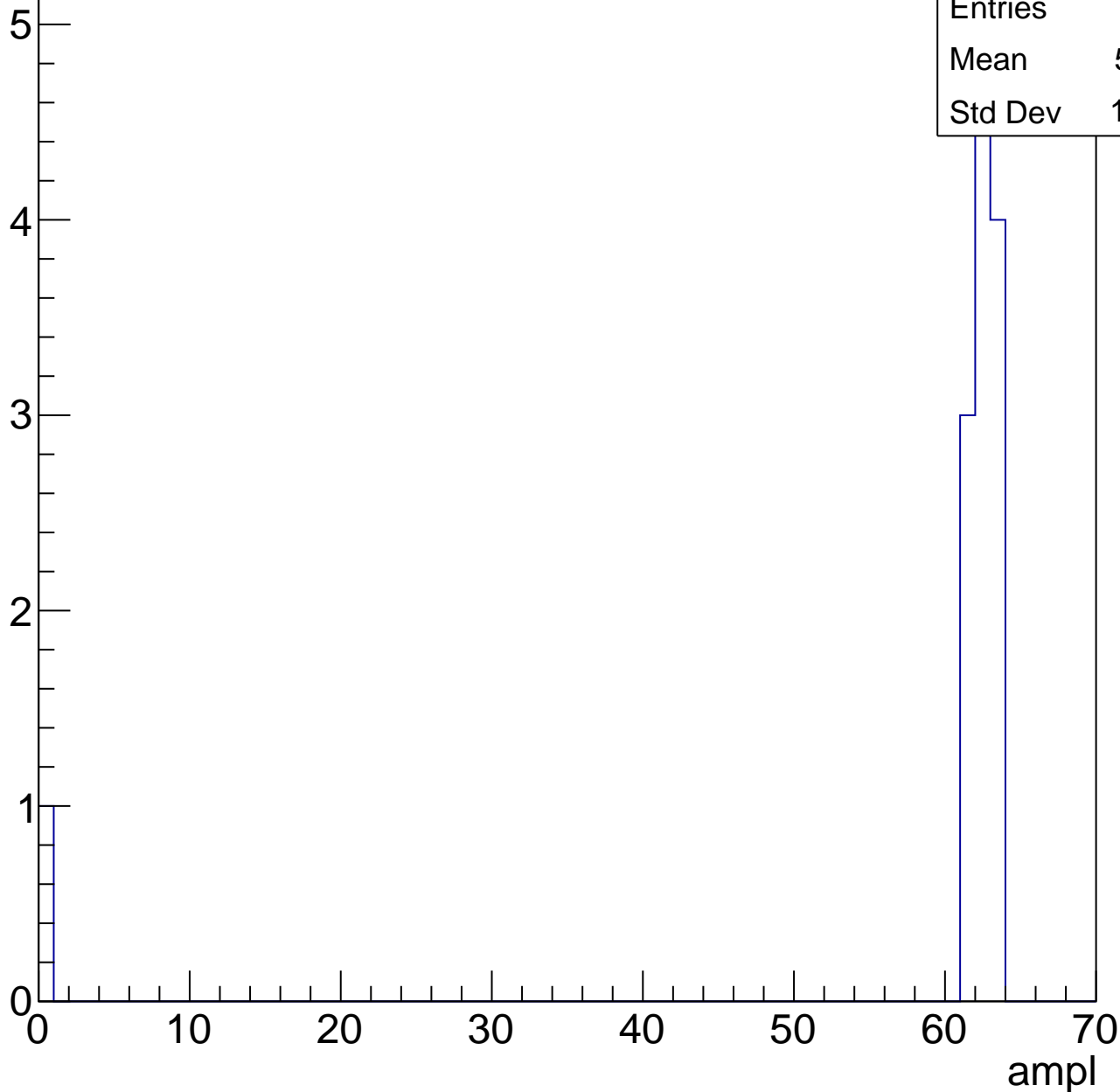


# B1L102S, U5-ch100, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	13
Mean	57.31
Std Dev	16.56





# B1L102S, U5-ch100, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U5-ch101, adc0

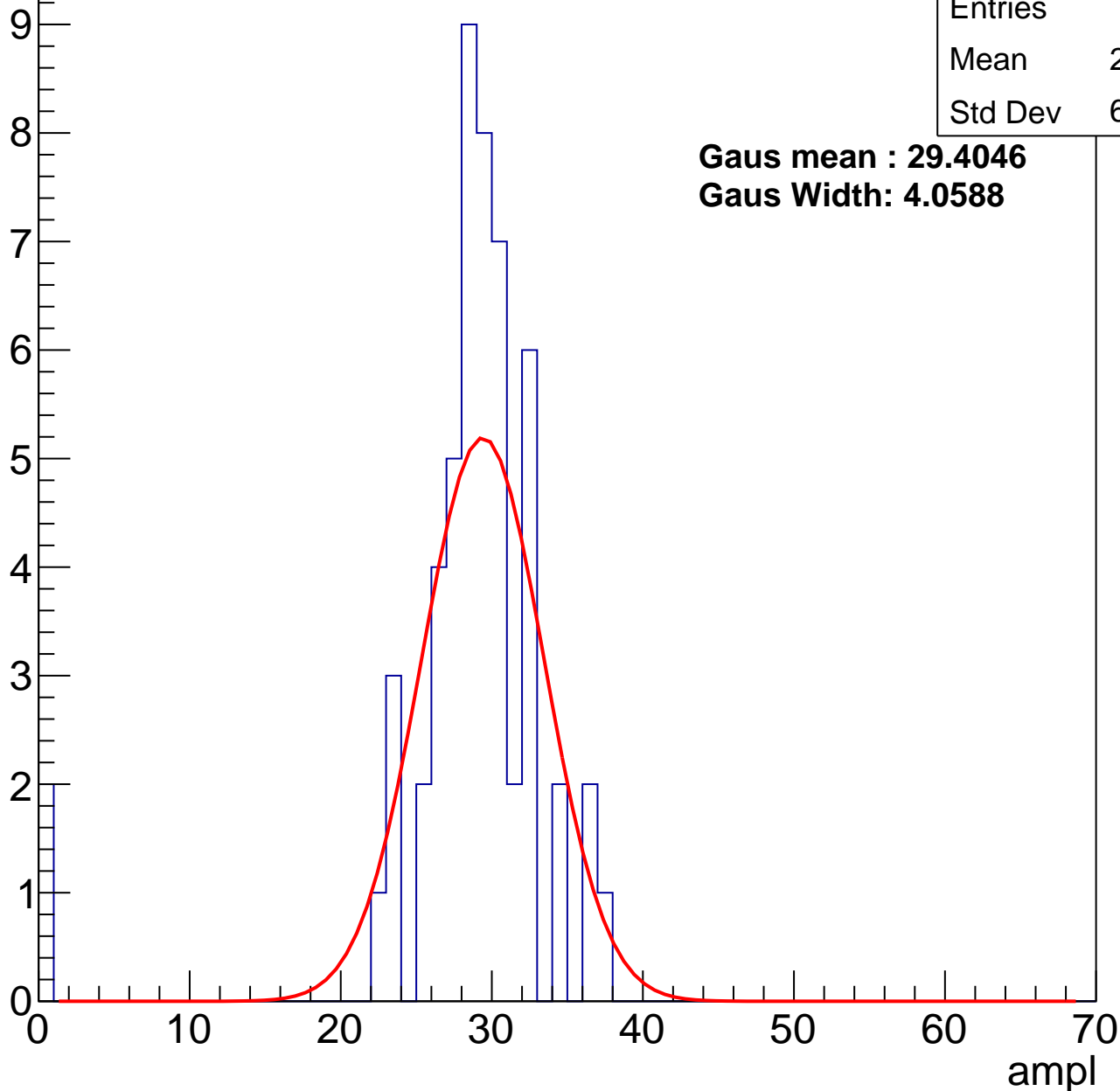
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	27.87
Std Dev	6.307

**Gaus mean : 29.4046**

**Gaus Width: 4.0588**



# B1L102S, U5-ch101, adc1

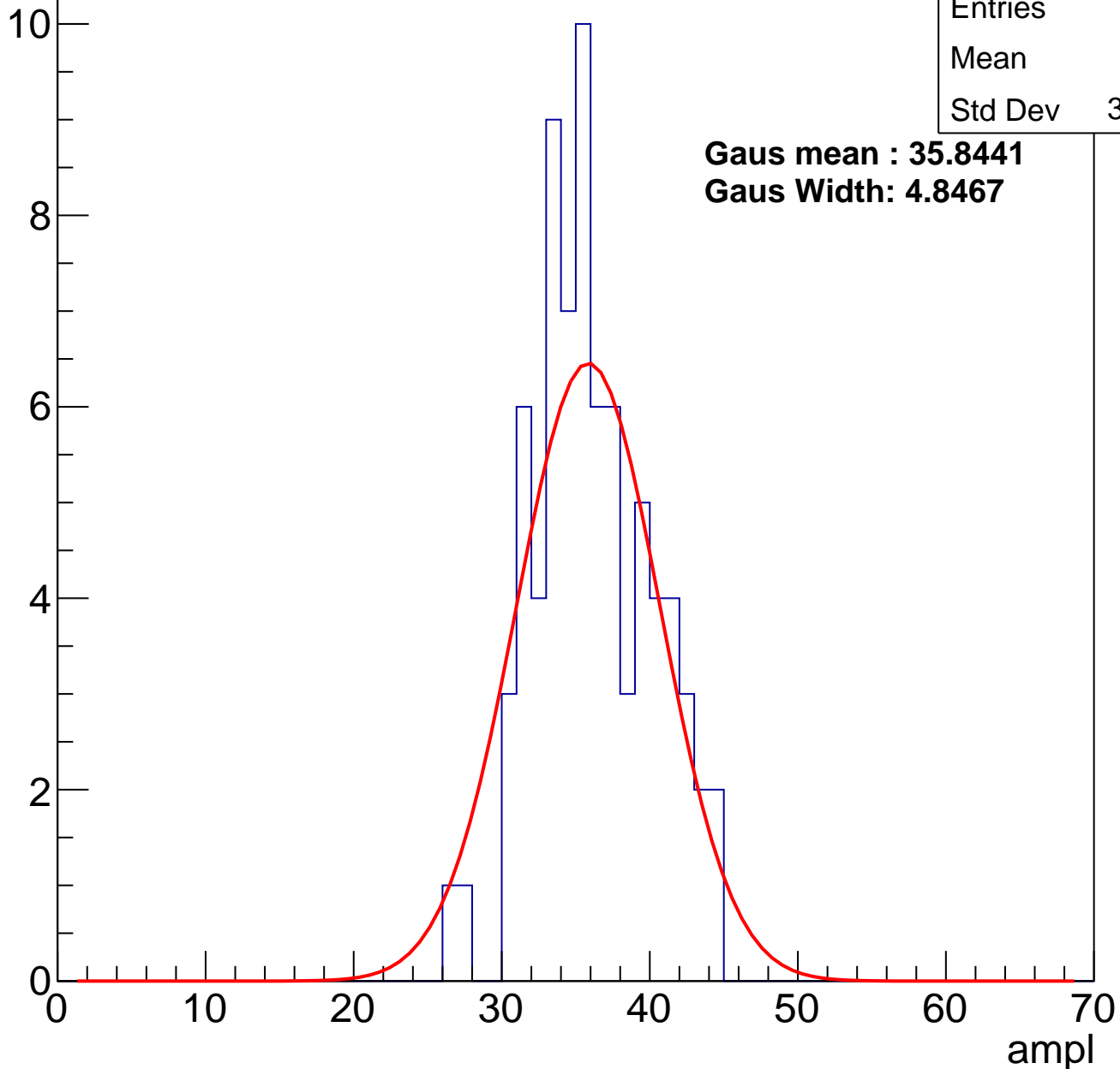
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	76
Mean	35.7
Std Dev	3.934

**Gaus mean : 35.8441**

**Gaus Width: 4.8467**

Entry



# B1L102S, U5-ch101, adc2

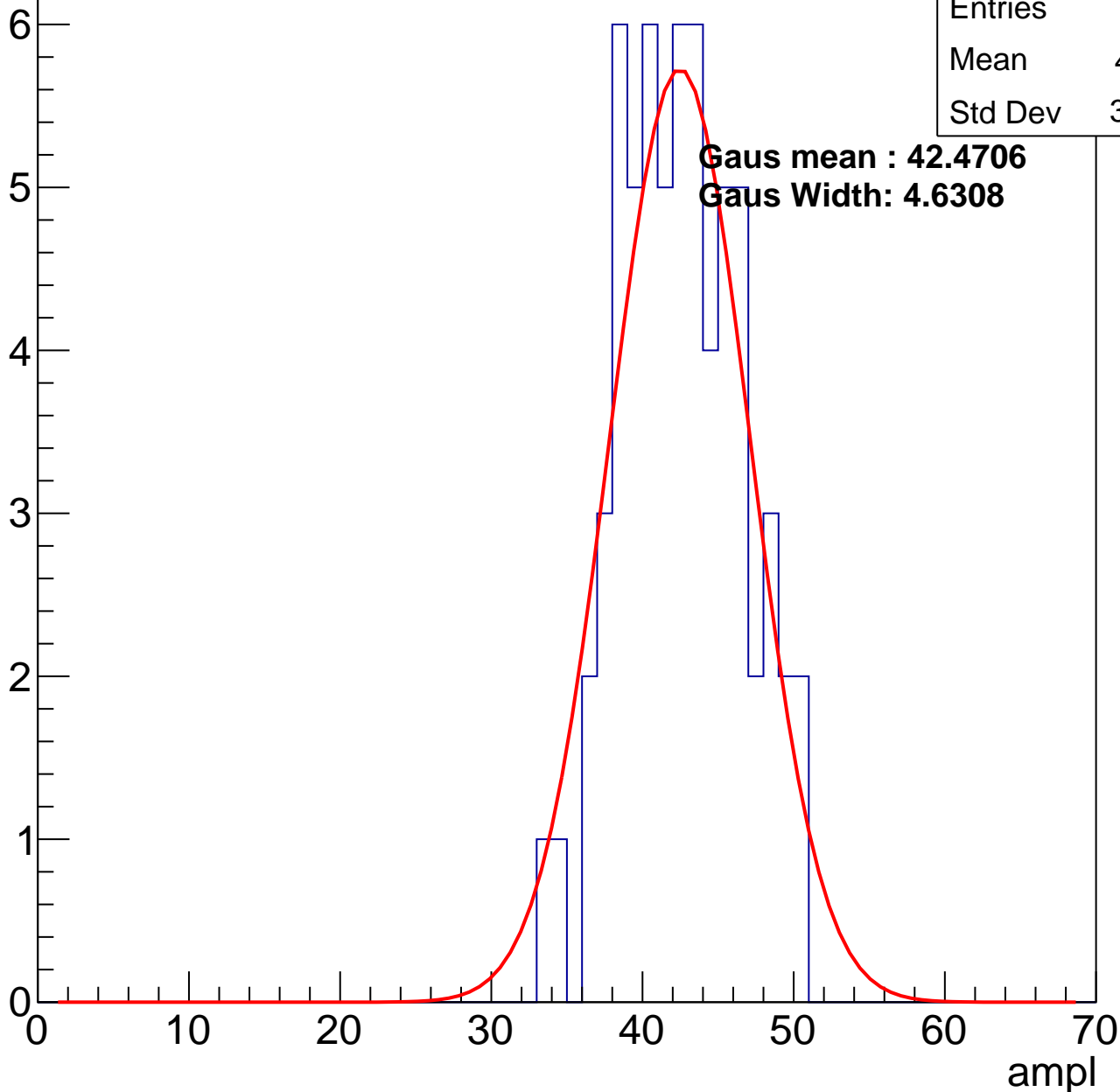
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	42.11
Std Dev	3.937

**Gaus mean : 42.4706**

**Gaus Width: 4.6308**

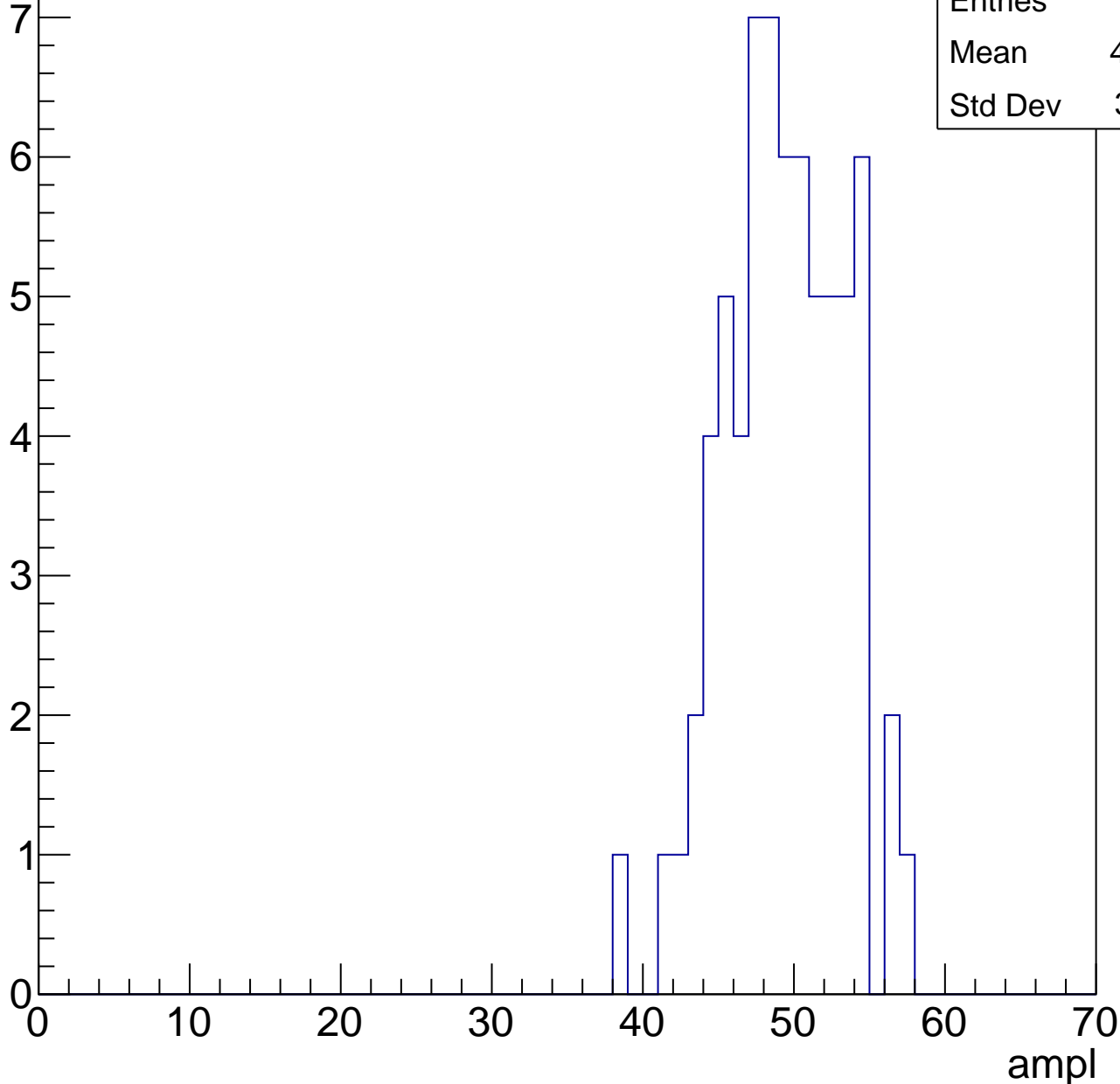


# B1L102S, U5-ch101, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	48.88
Std Dev	3.871

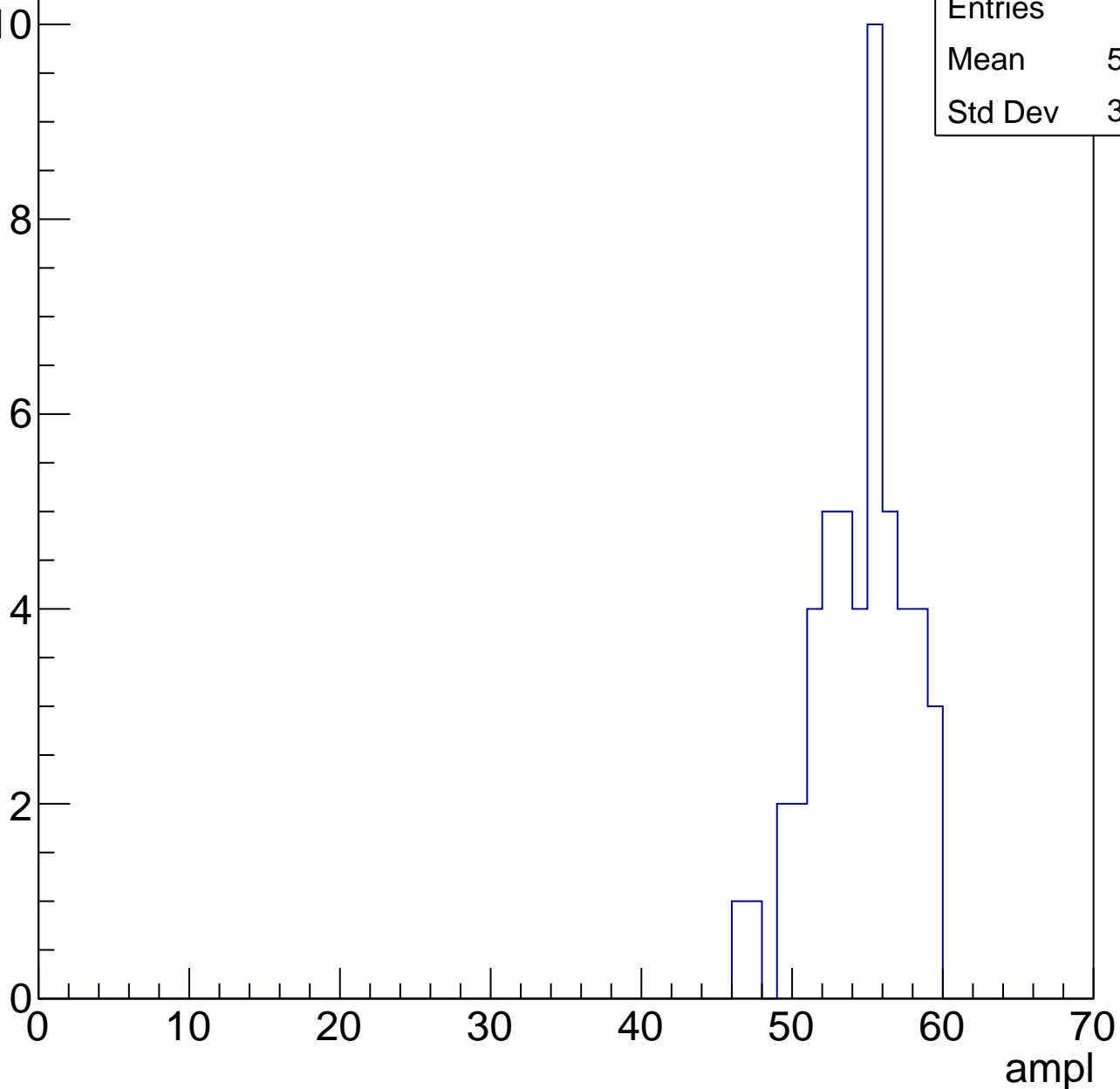


# B1L102S, U5-ch101, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	54.06
Std Dev	3.036

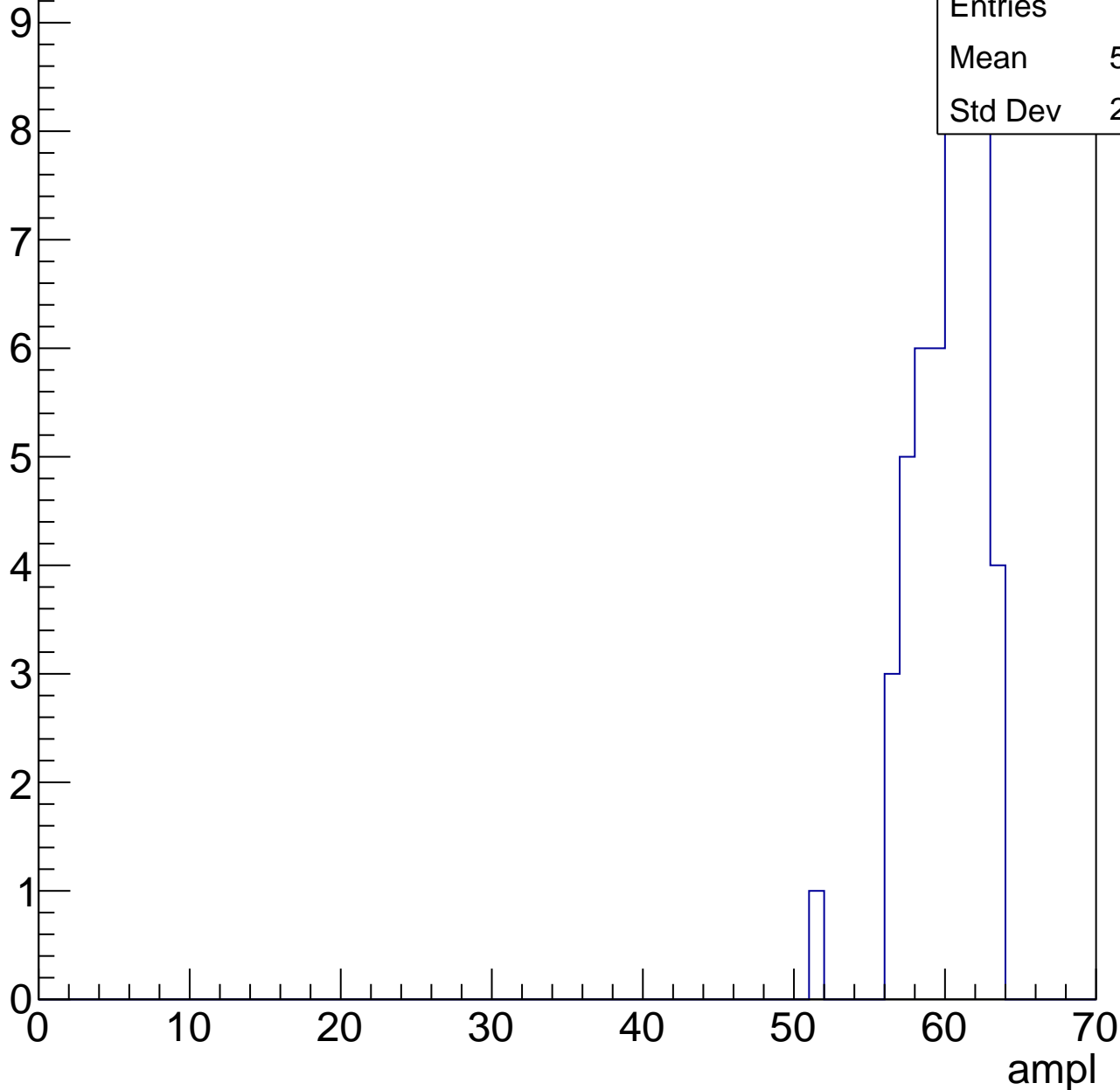


# B1L102S, U5-ch101, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	59.68
Std Dev	2.362

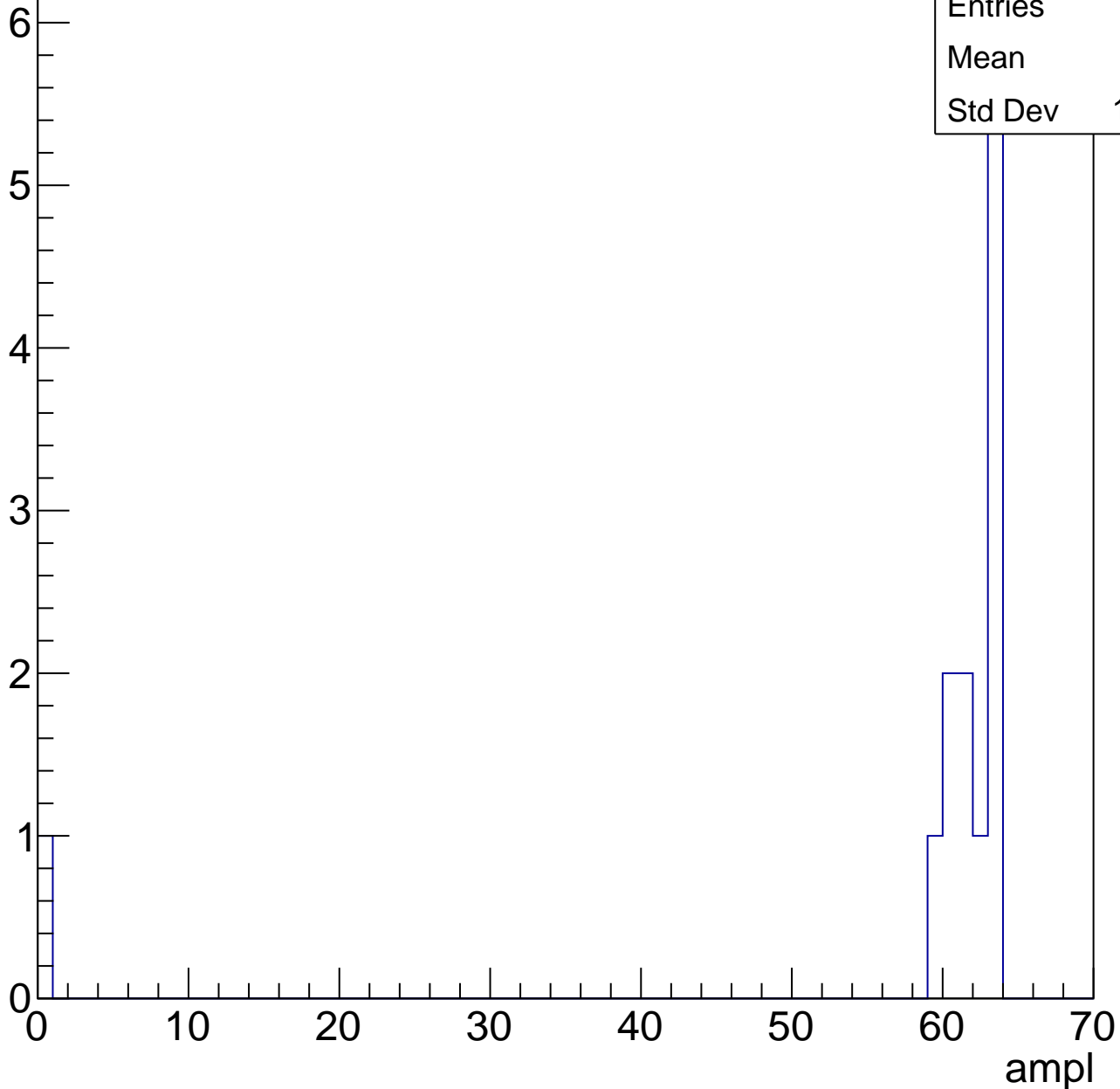


# B1L102S, U5-ch101, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	13
Mean	57
Std Dev	16.51





# B1L102S, U5-ch101, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L102S, U5-ch102, adc0

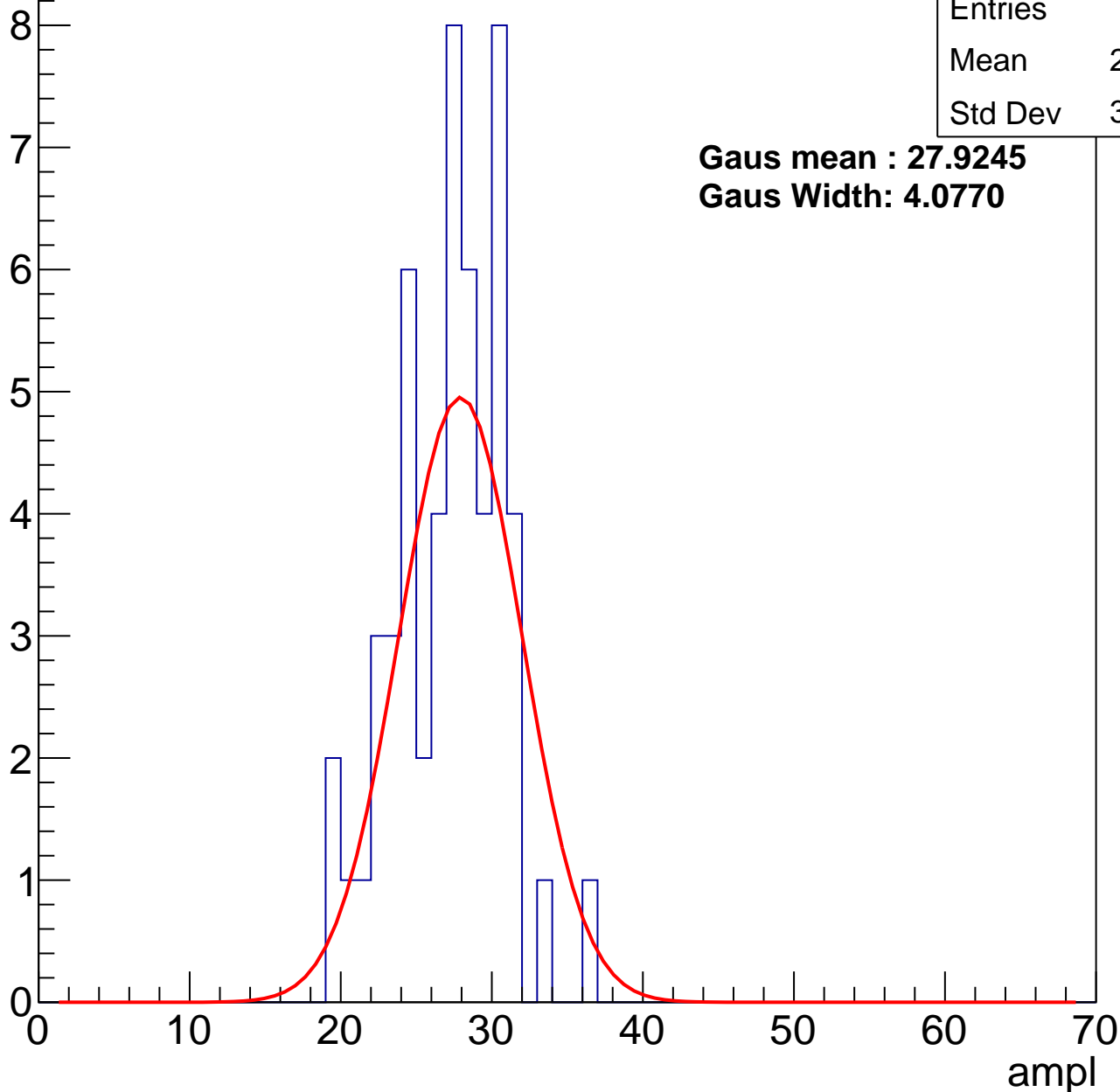
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	26.76
Std Dev	3.533

**Gaus mean : 27.9245**

**Gaus Width: 4.0770**



# B1L102S, U5-ch102, adc1

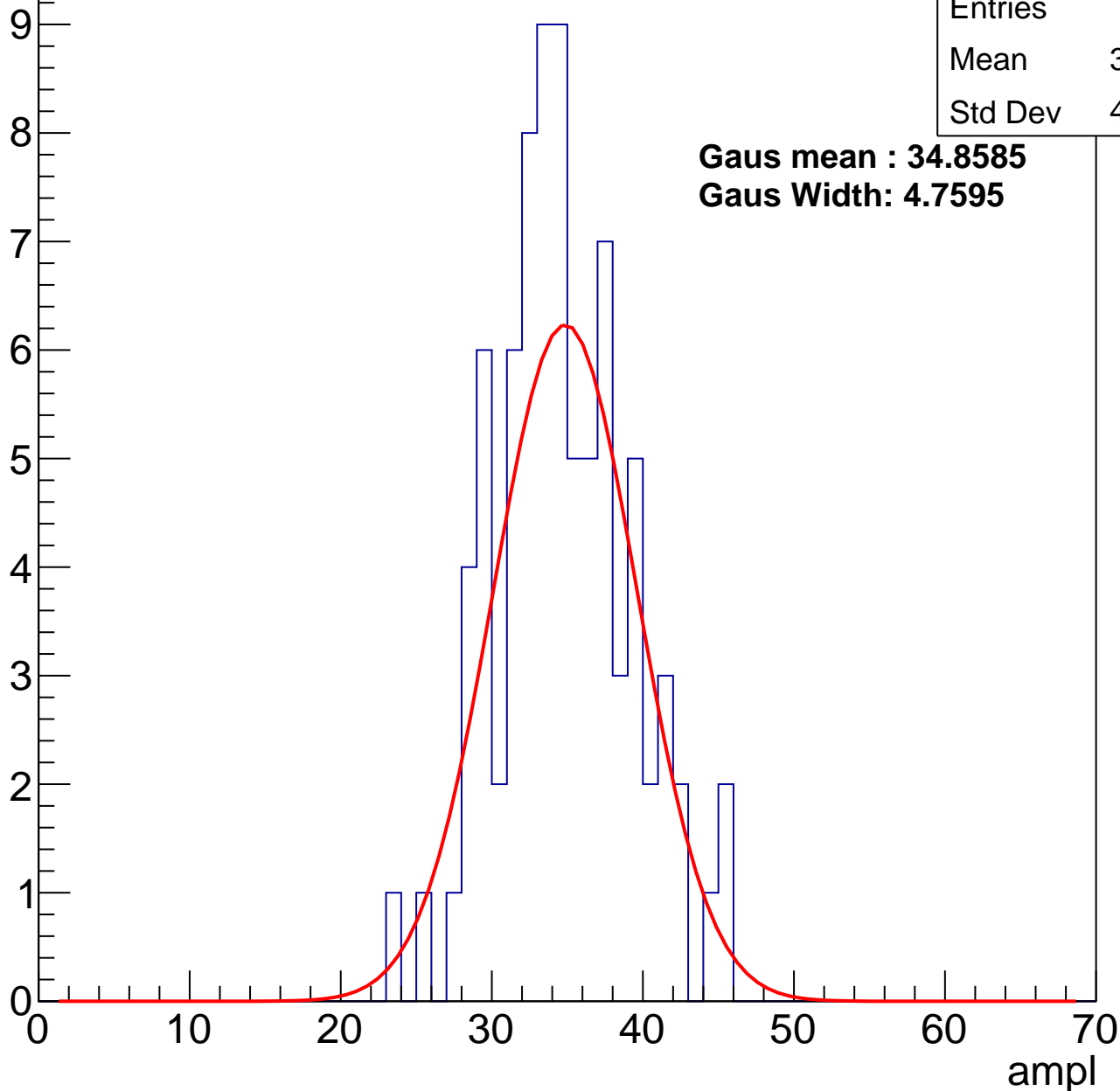
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	82
Mean	34.27
Std Dev	4.439

**Gaus mean : 34.8585**

**Gaus Width: 4.7595**

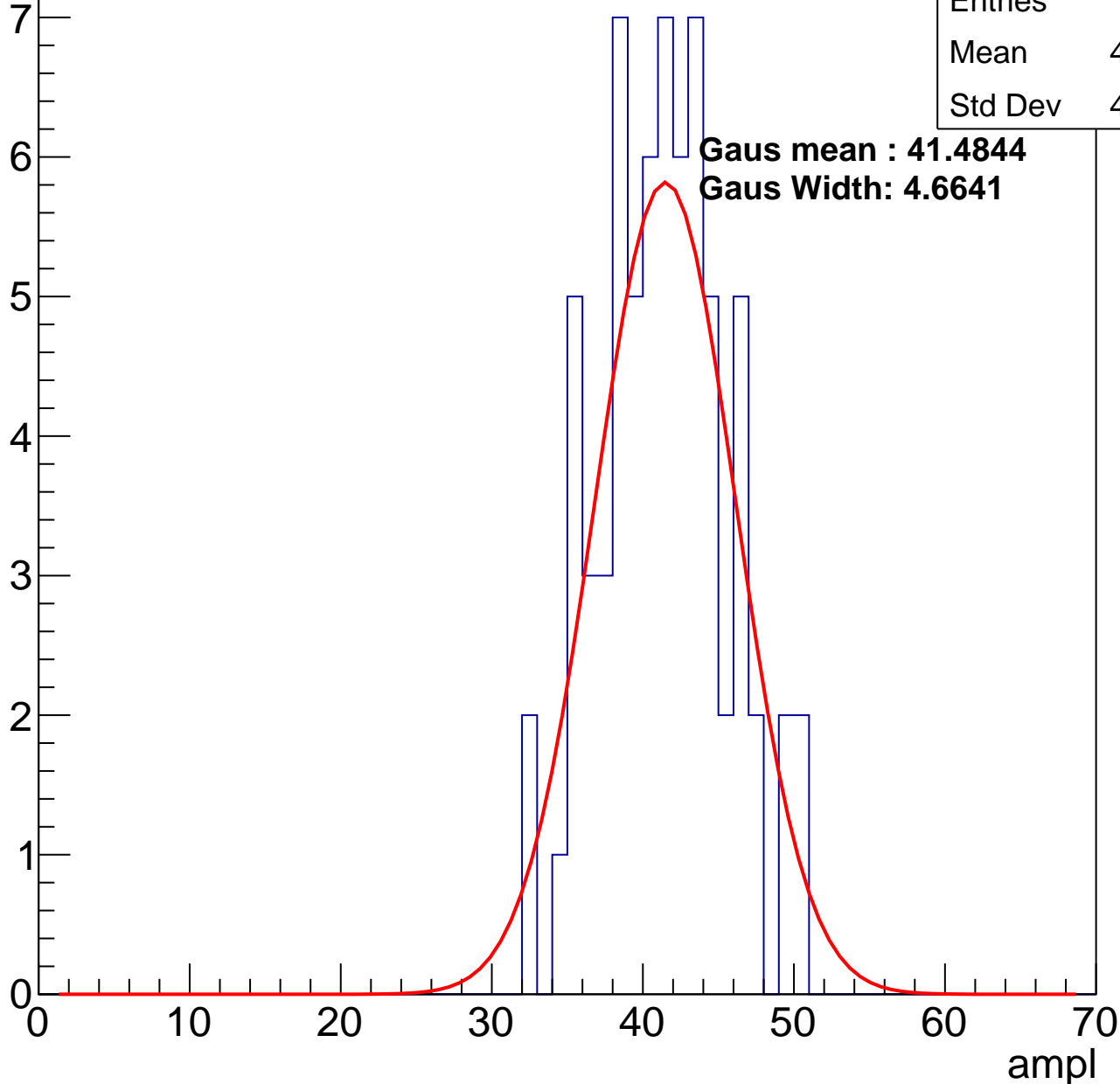


# B1L102S, U5-ch102, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	40.93
Std Dev	4.142



# B1L102S, U5-ch102, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

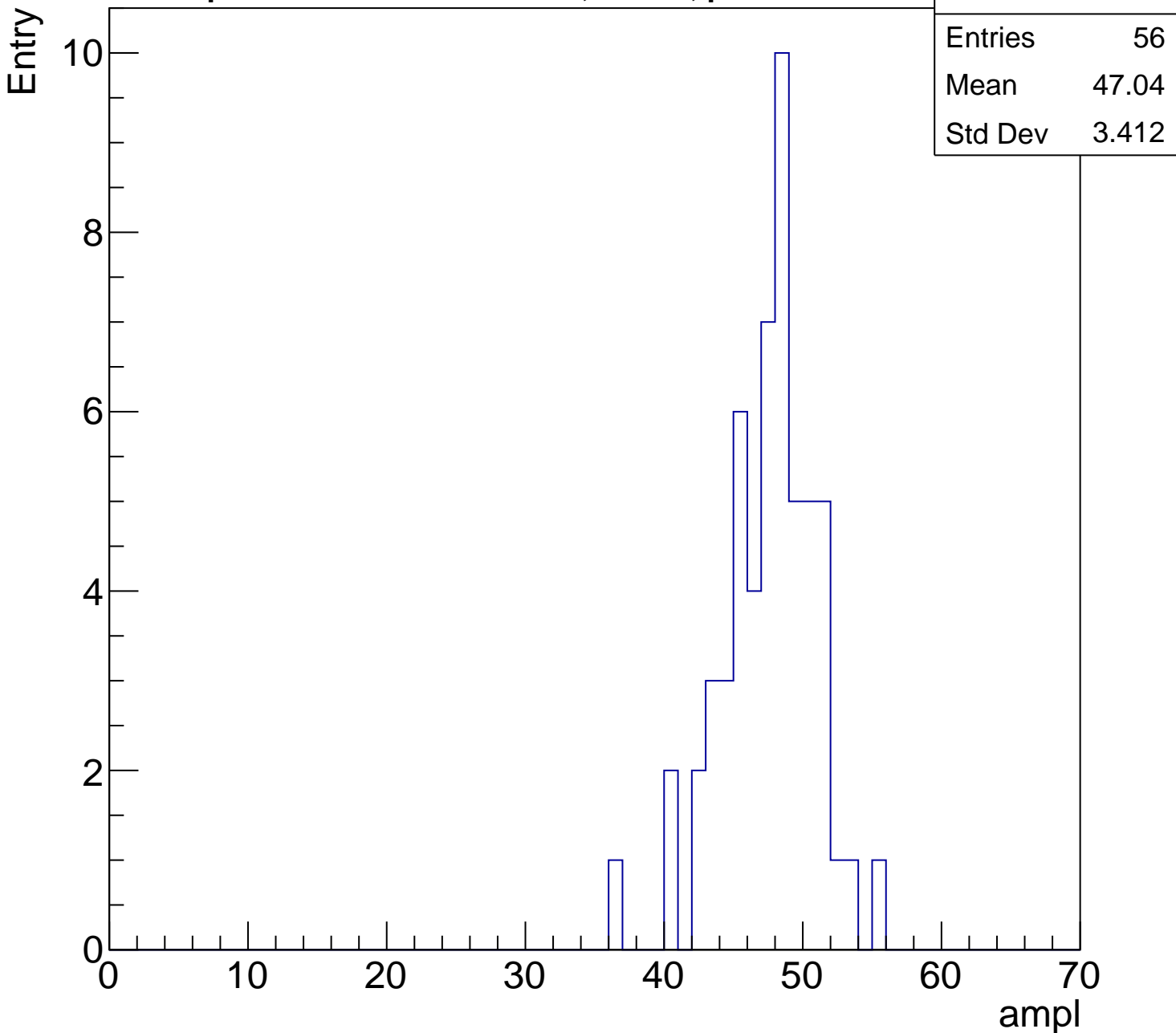
Entries	56
Mean	47.04
Std Dev	3.412

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

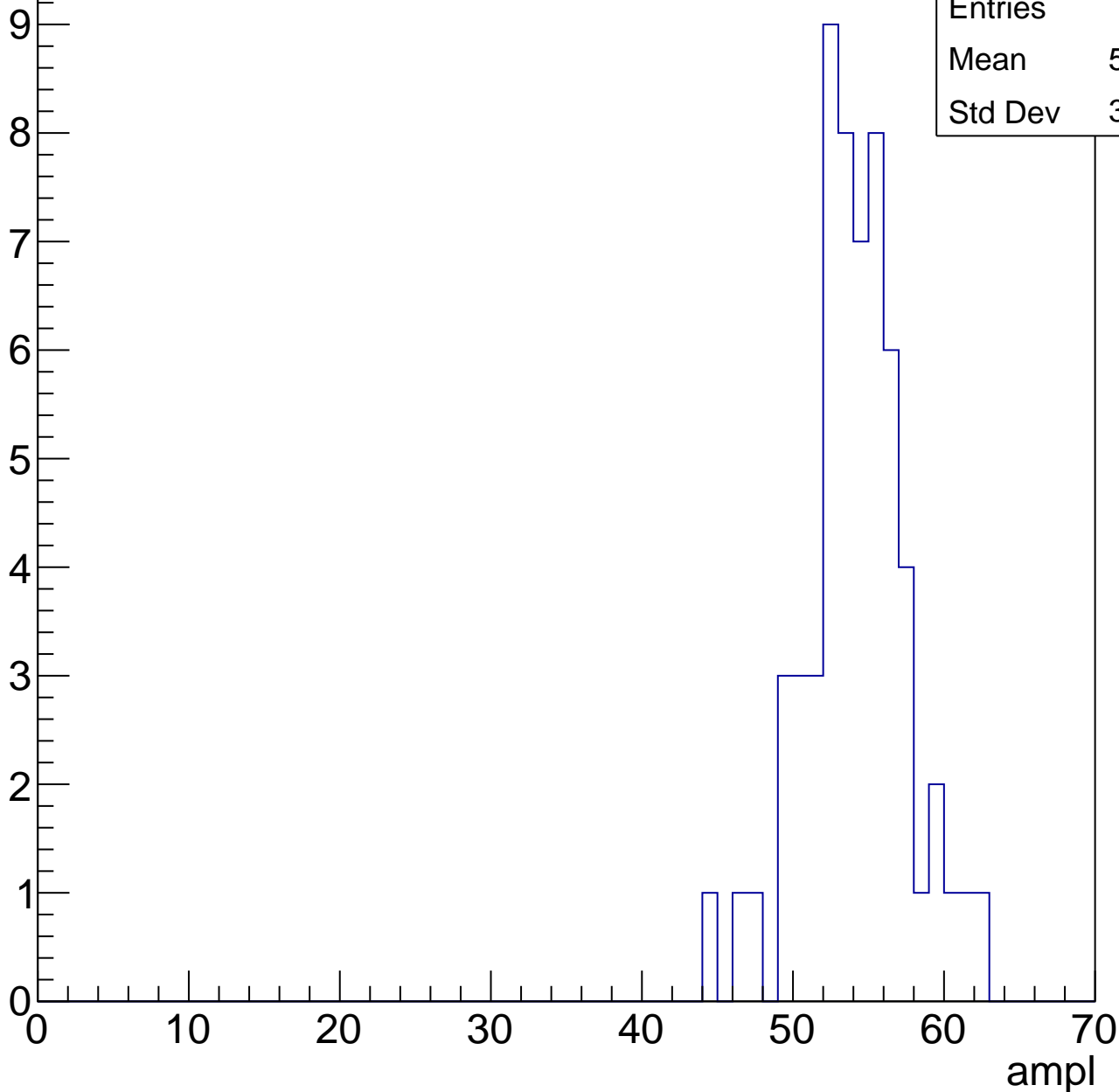


# B1L102S, U5-ch102, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

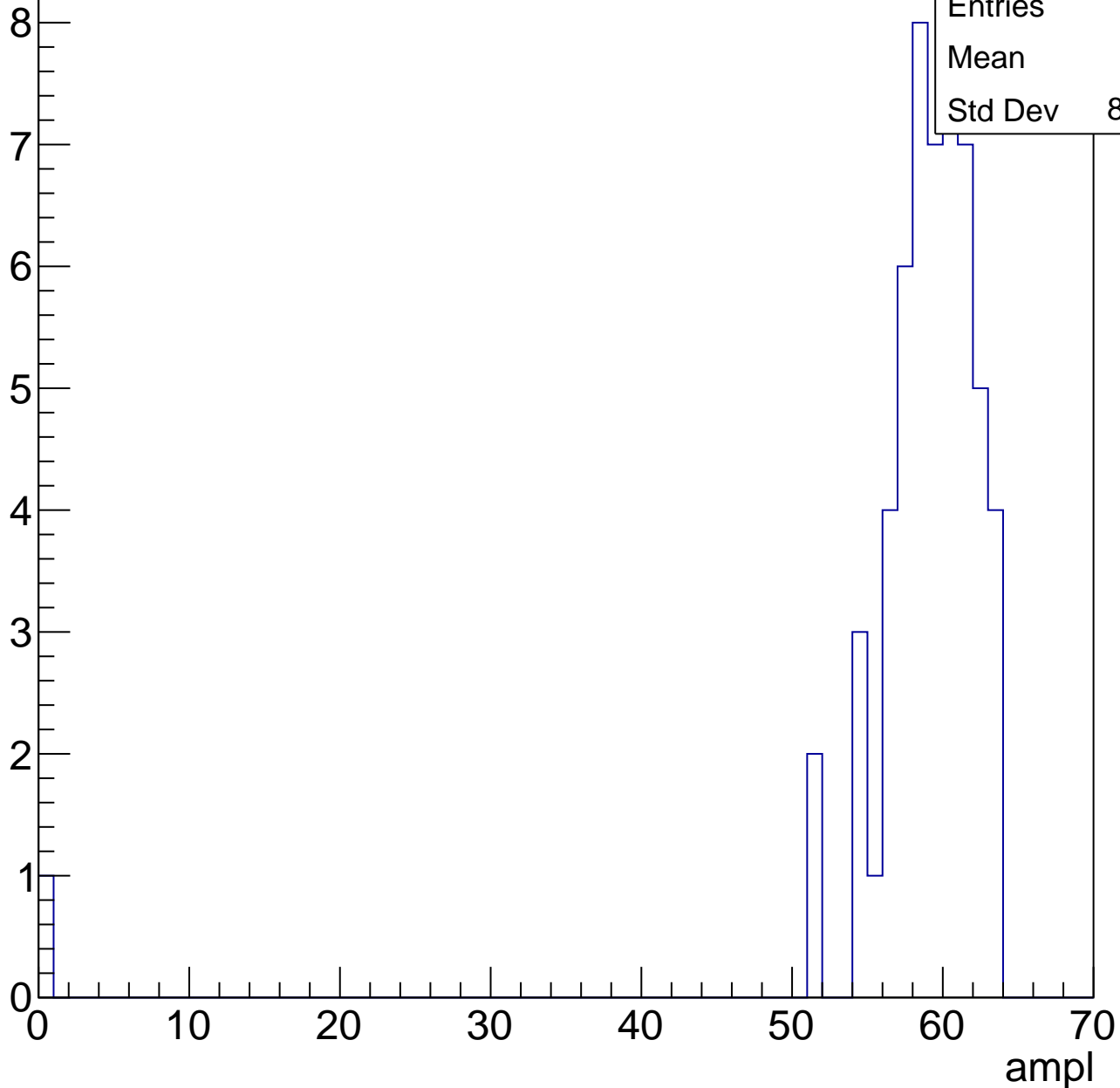
Entries	60
Mean	53.67
Std Dev	3.375



# B1L102S, U5-ch102, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

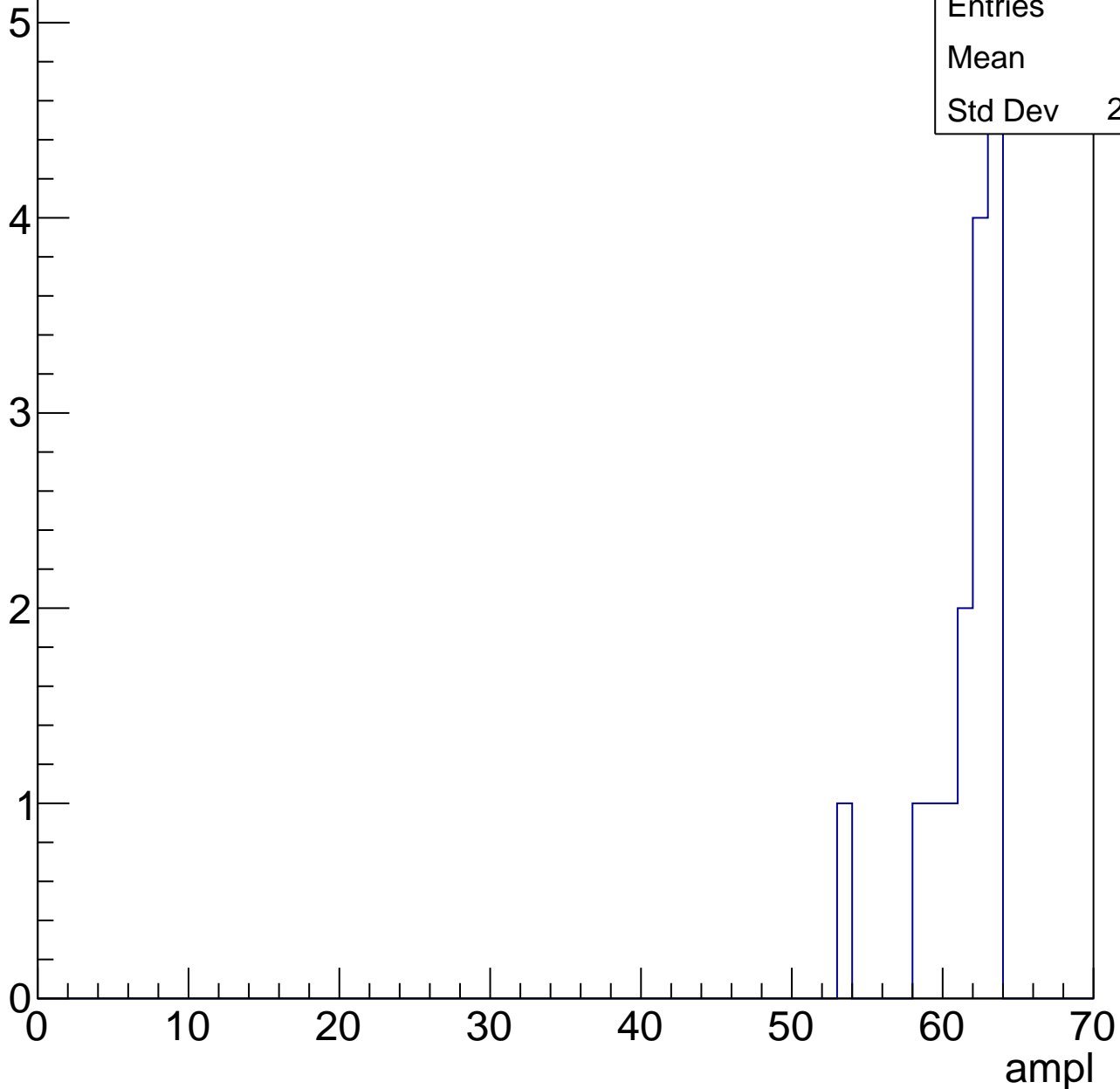


# B1L102S, U5-ch102, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	15
Mean	61
Std Dev	2.608





# B1L102S, U5-ch102, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U5-ch103, adc0

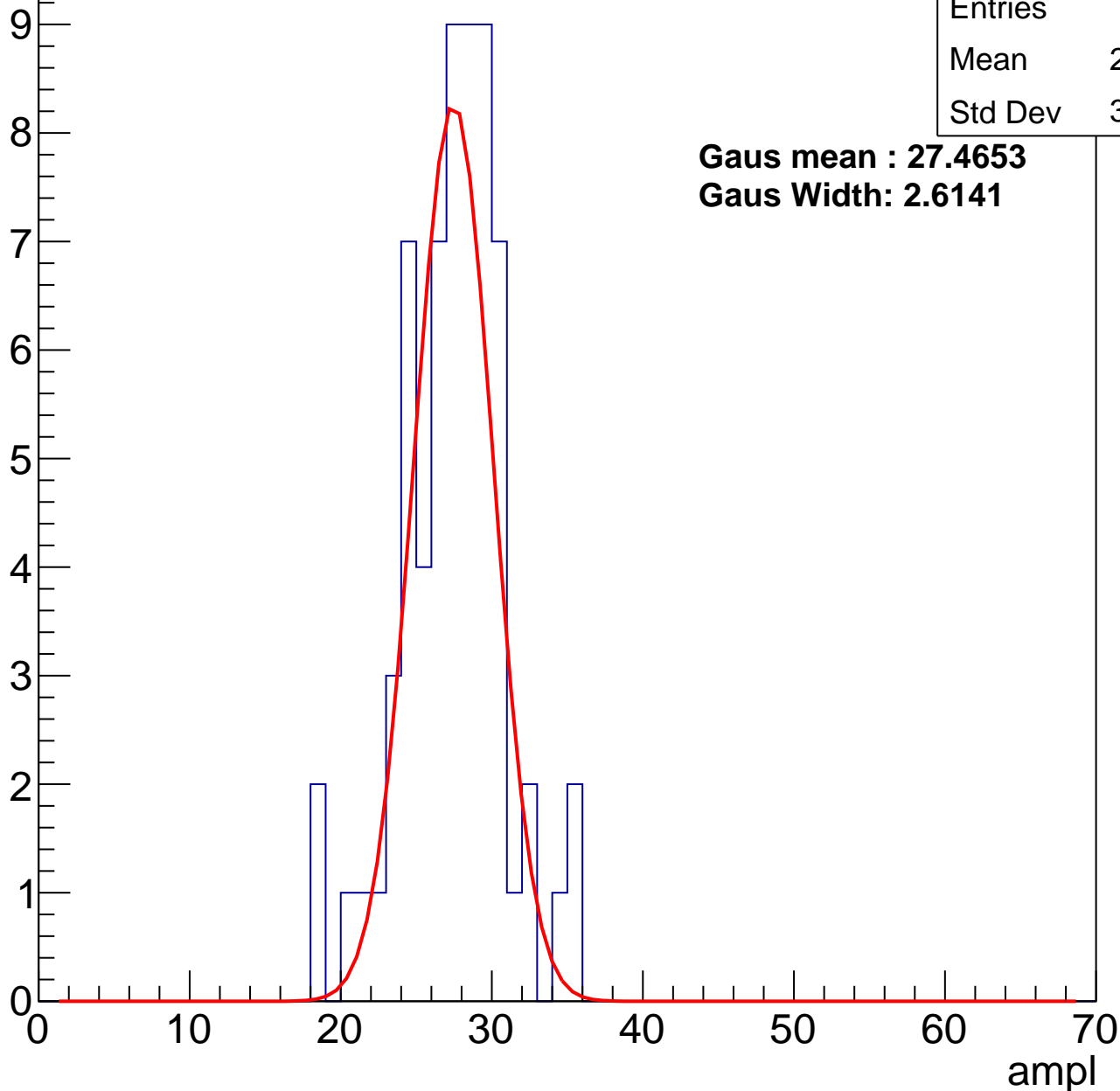
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	27.02
Std Dev	3.387

**Gaus mean : 27.4653**

**Gaus Width: 2.6141**



# B1L102S, U5-ch103, adc1

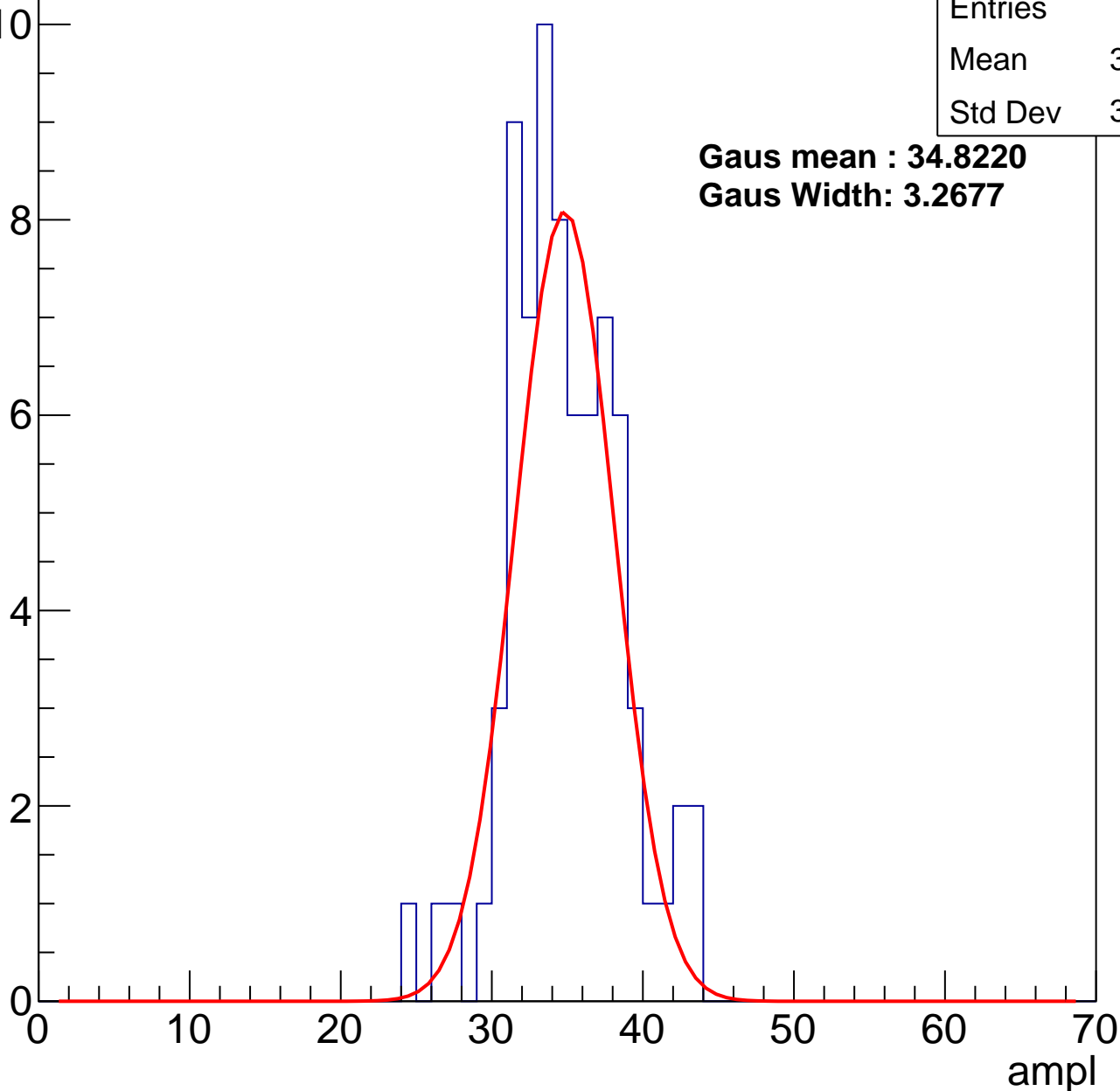
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	34.43
Std Dev	3.706

**Gaus mean : 34.8220**

**Gaus Width: 3.2677**



# B1L102S, U5-ch103, adc2

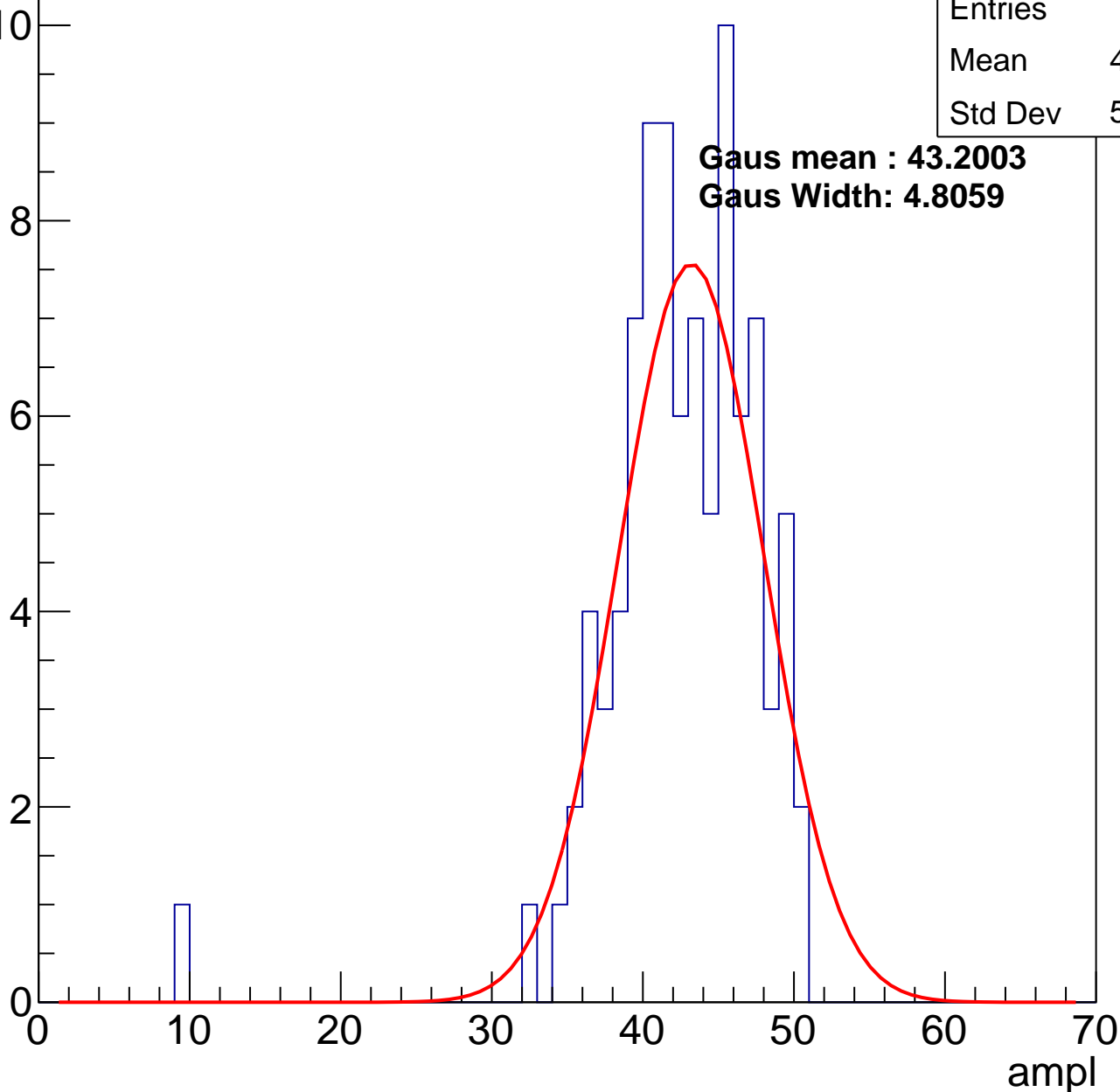
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	92
Mean	42.08
Std Dev	5.327

**Gaus mean : 43.2003**

**Gaus Width: 4.8059**

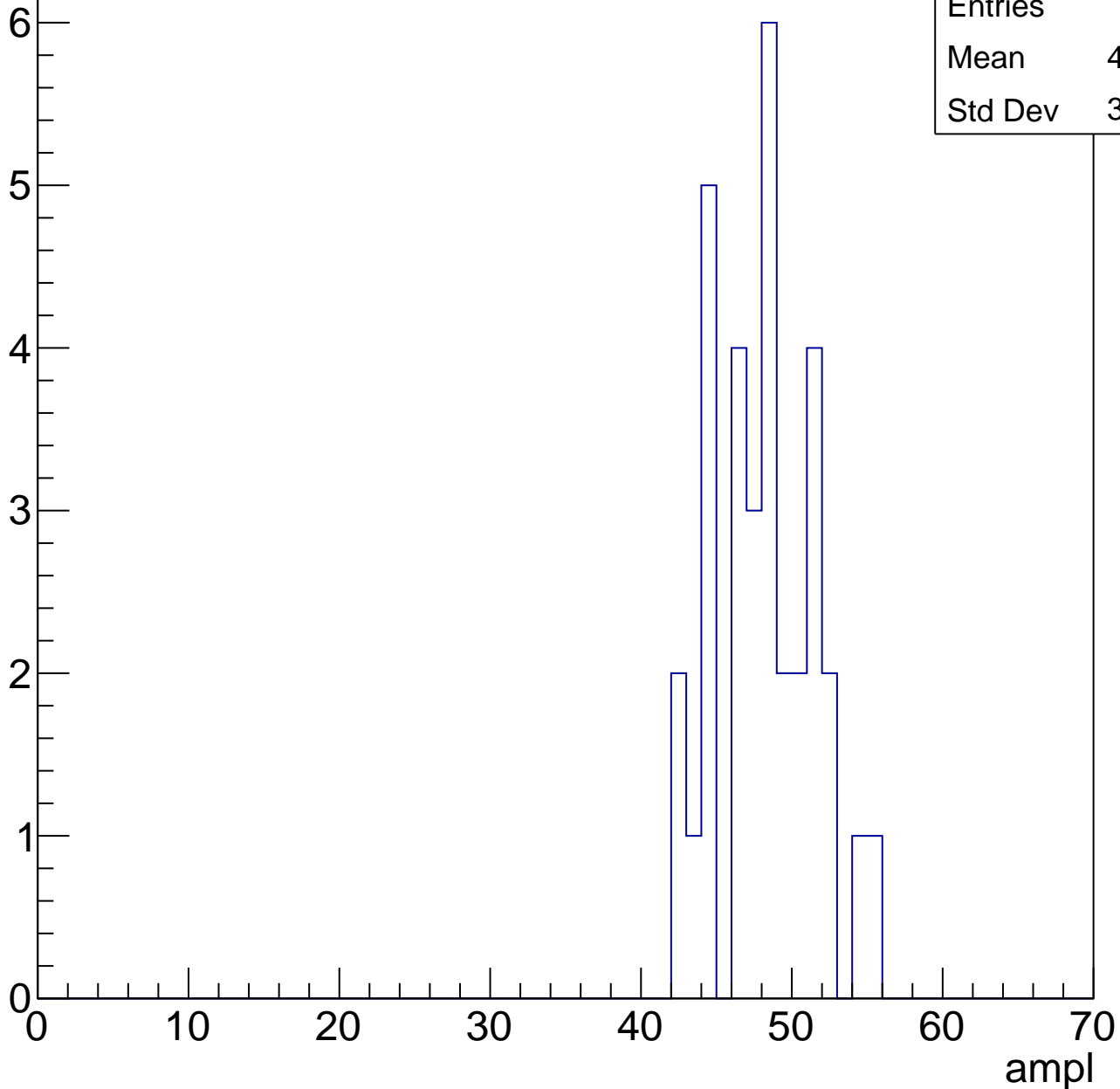


# B1L102S, U5-ch103, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	33
Mean	47.73
Std Dev	3.287

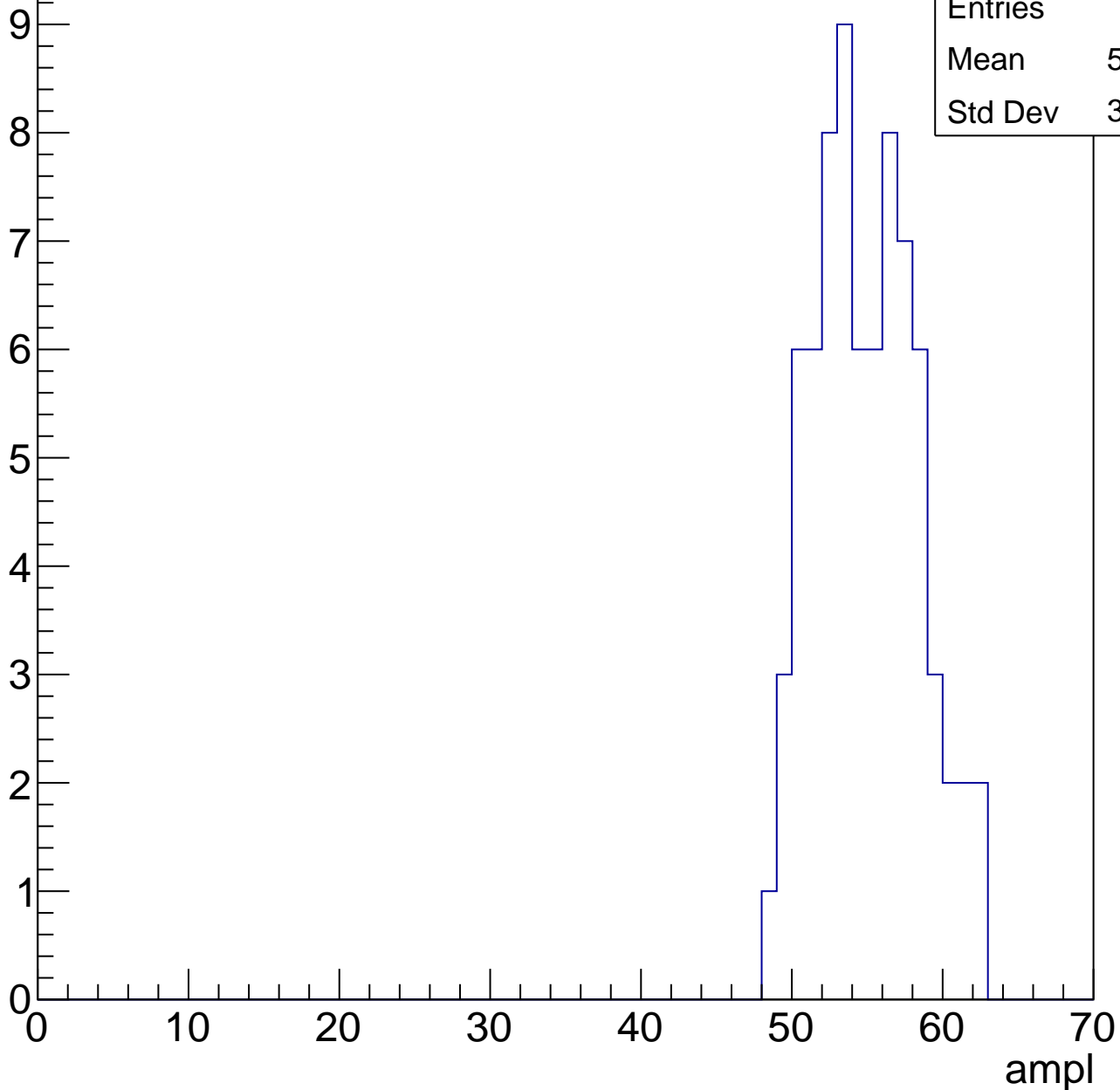


# B1L102S, U5-ch103, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	54.48
Std Dev	3.376



# B1L102S, U5-ch103, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

7

6

5

4

3

2

1

0

Entries

46

Mean

59.17

Std Dev

2.8

0

ampl

0

10

20

30

40

50

60

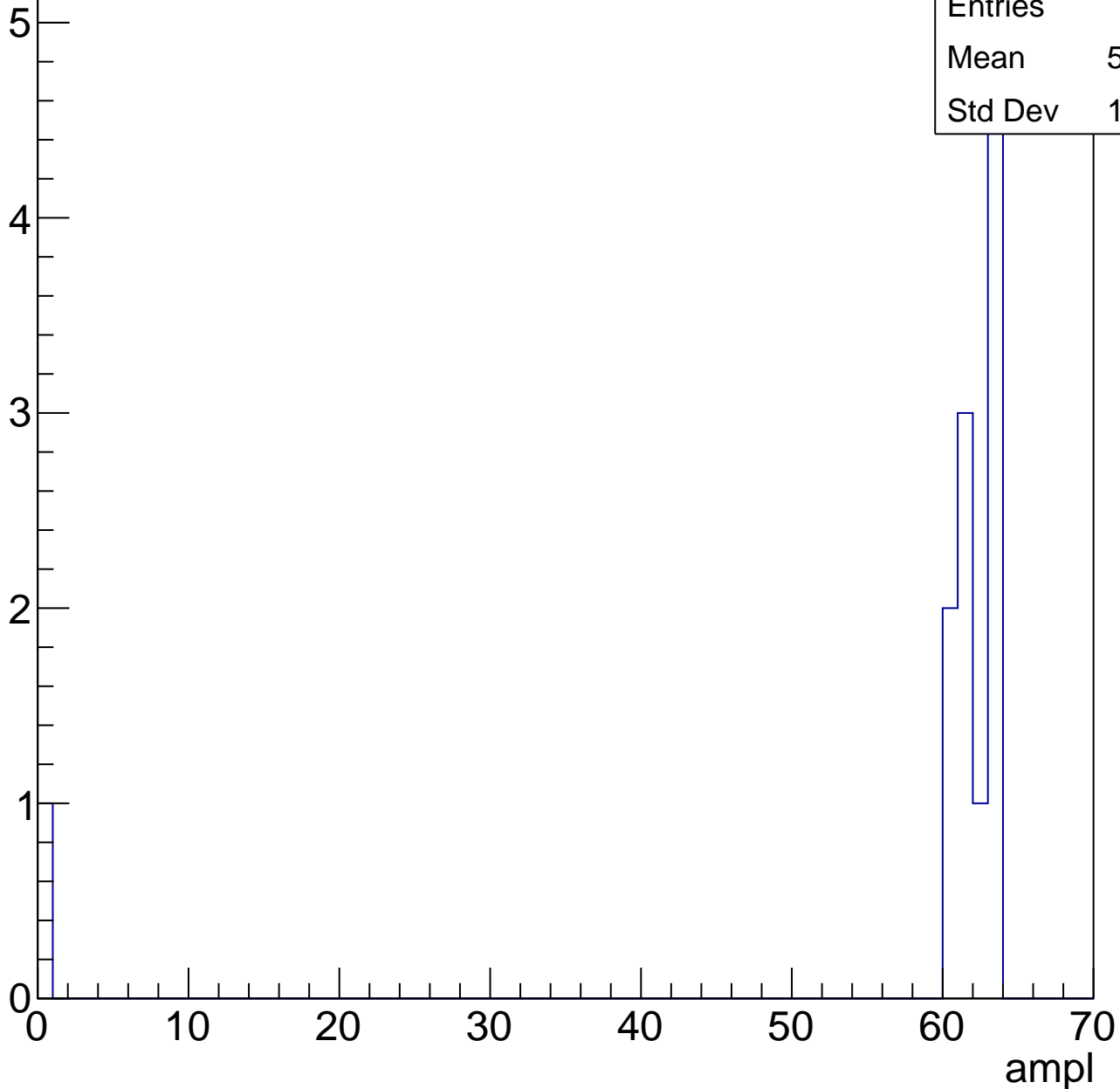
70

# B1L102S, U5-ch103, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	12
Mean	56.67
Std Dev	17.12

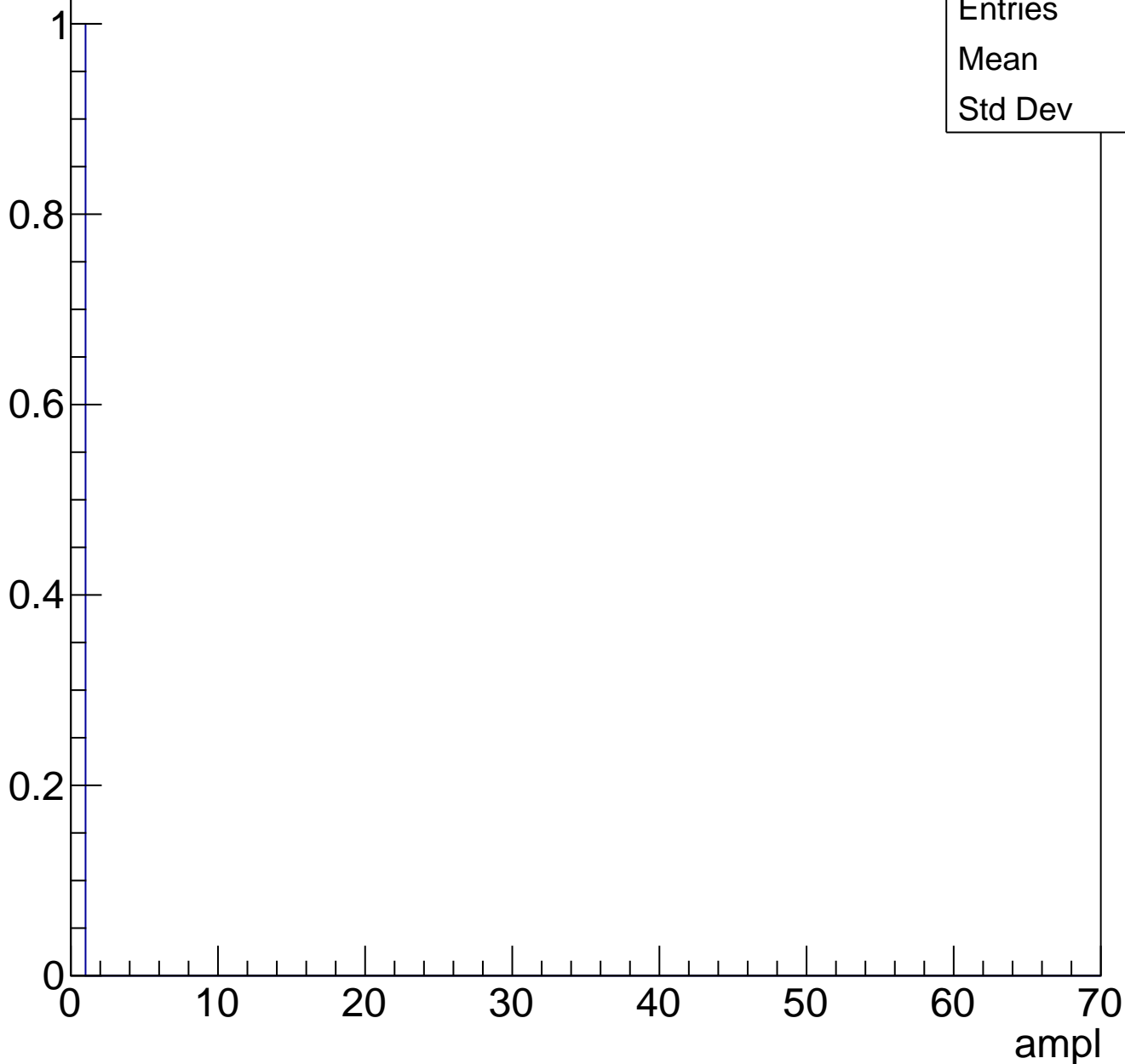




# B1L102S, U5-ch103, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L102S, U5-ch104, adc0

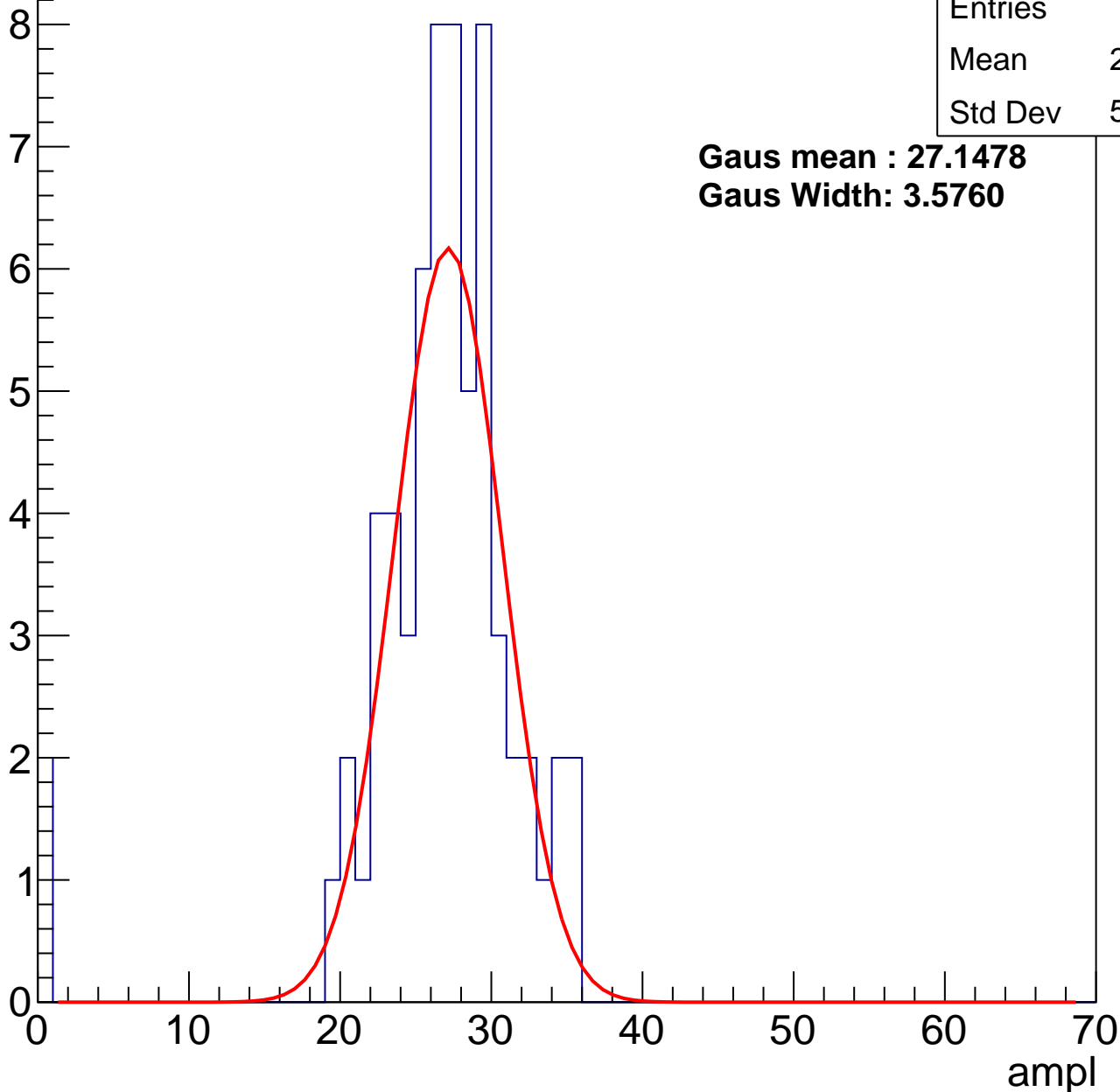
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	26.02
Std Dev	5.896

**Gaus mean : 27.1478**

**Gaus Width: 3.5760**



# B1L102S, U5-ch104, adc1

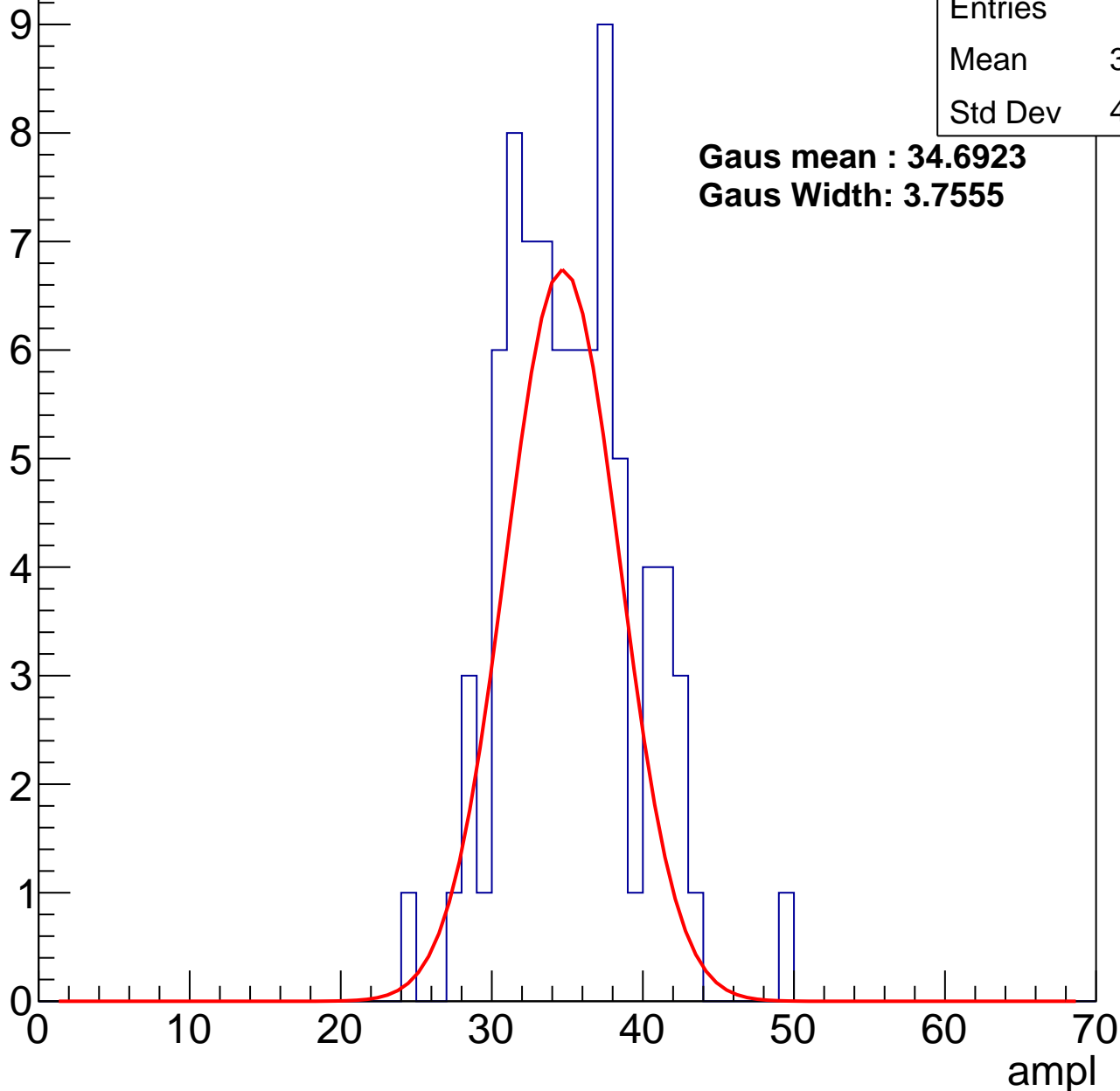
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	80
Mean	34.76
Std Dev	4.319

**Gaus mean : 34.6923**

**Gaus Width: 3.7555**



# B1L102S, U5-ch104, adc2

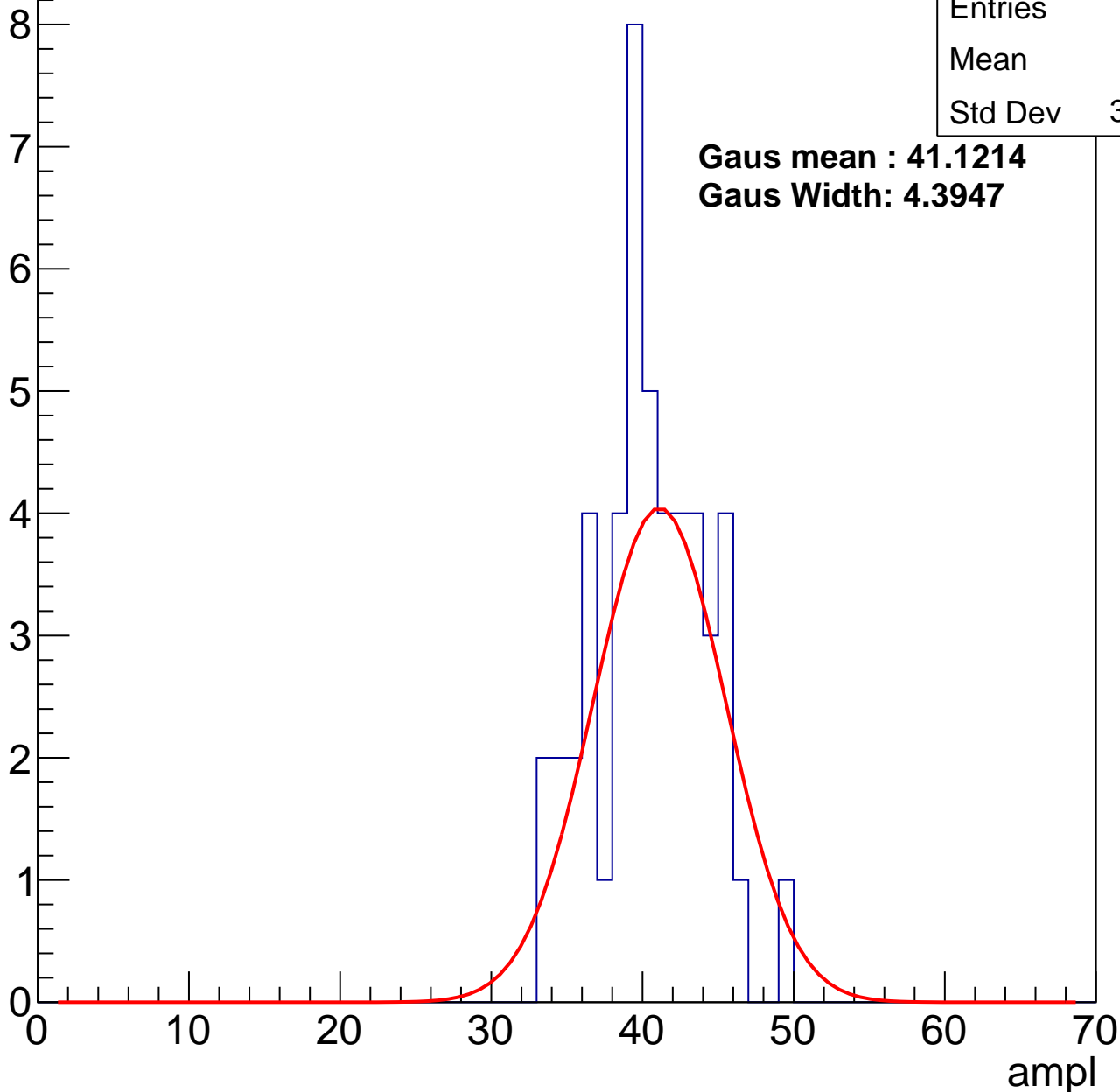
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	40
Std Dev	3.608

**Gaus mean : 41.1214**

**Gaus Width: 4.3947**

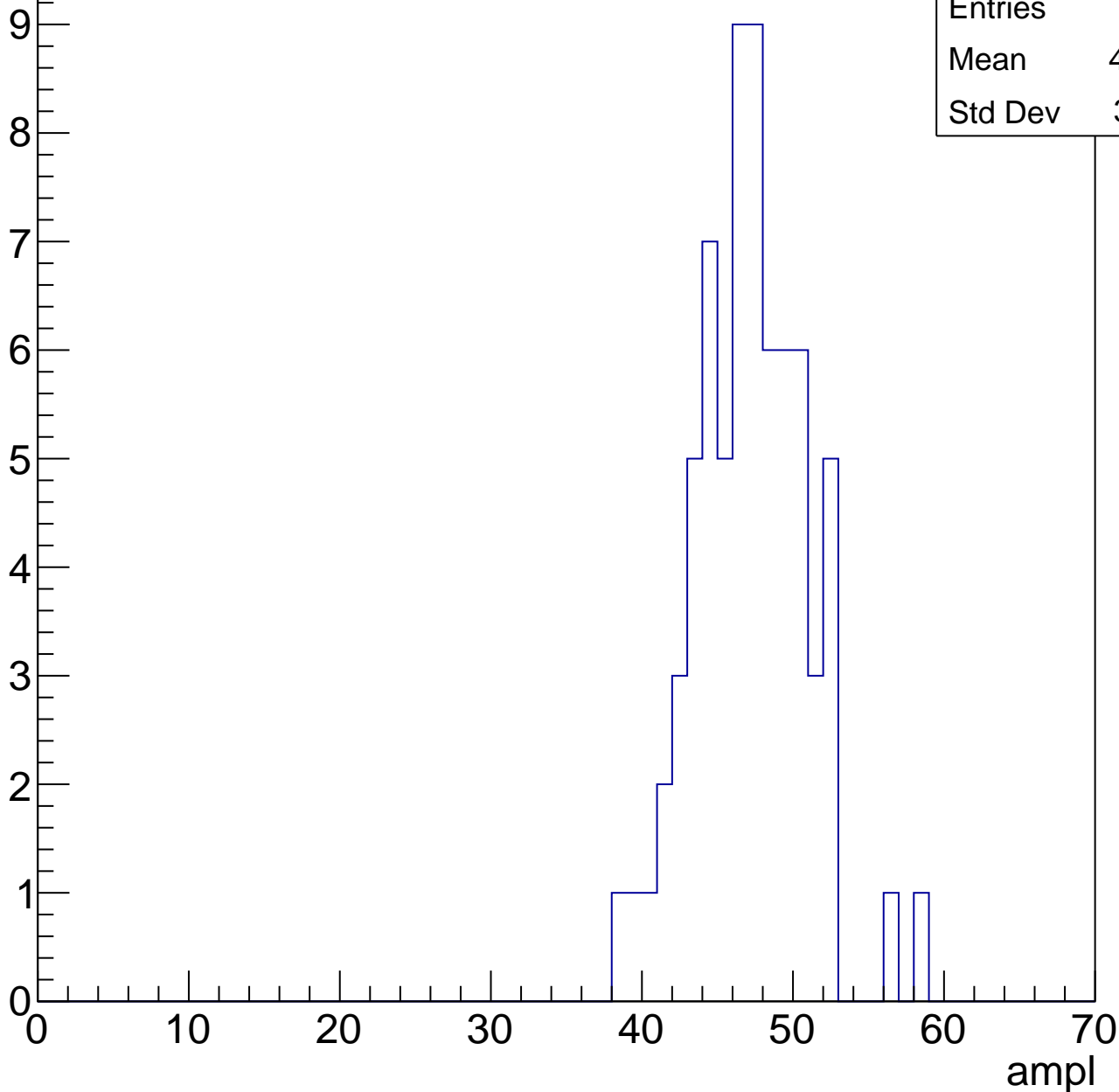


# B1L102S, U5-ch104, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	46.75
Std Dev	3.691

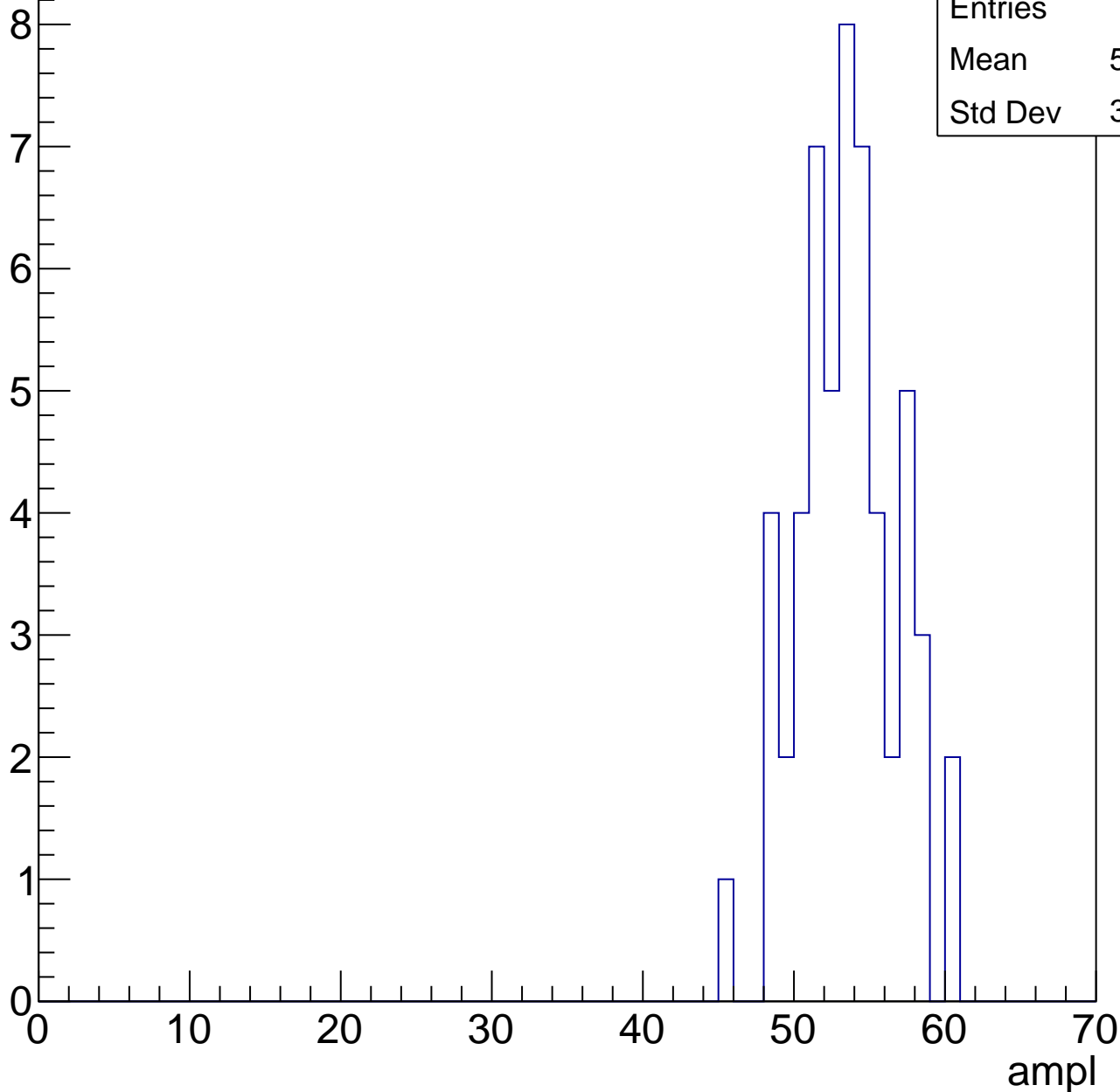


# B1L102S, U5-ch104, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	53.06
Std Dev	3.217



# B1L102S, U5-ch104, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

7

6

5

4

3

2

1

0

Entries 56

Mean 58.14

Std Dev 3.176

0

10

20

30

40

50

60

70

ampl

0

1

2

3

4

5

6

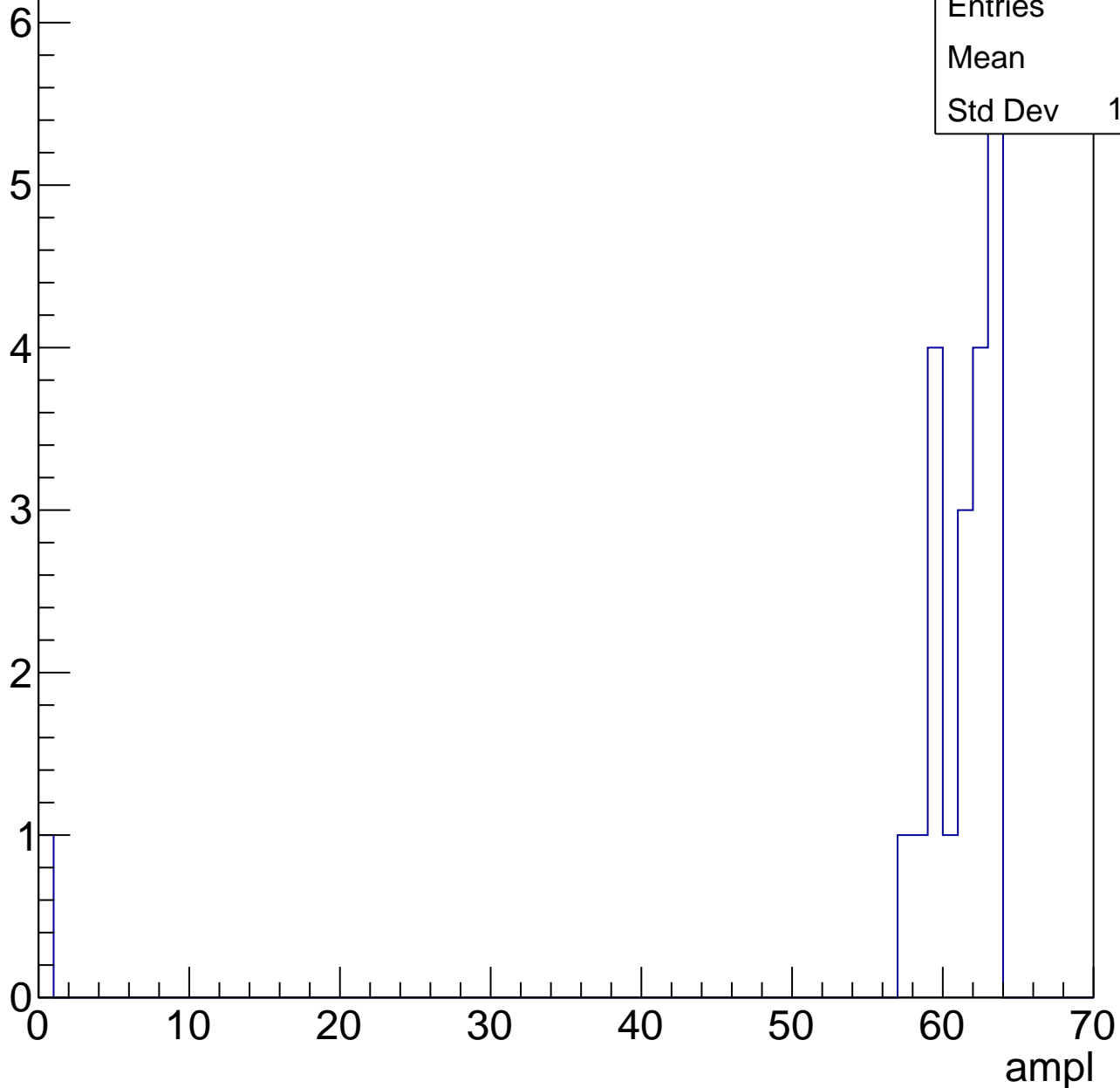
7

# B1L102S, U5-ch104, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	21
Mean	58.1
Std Dev	13.12

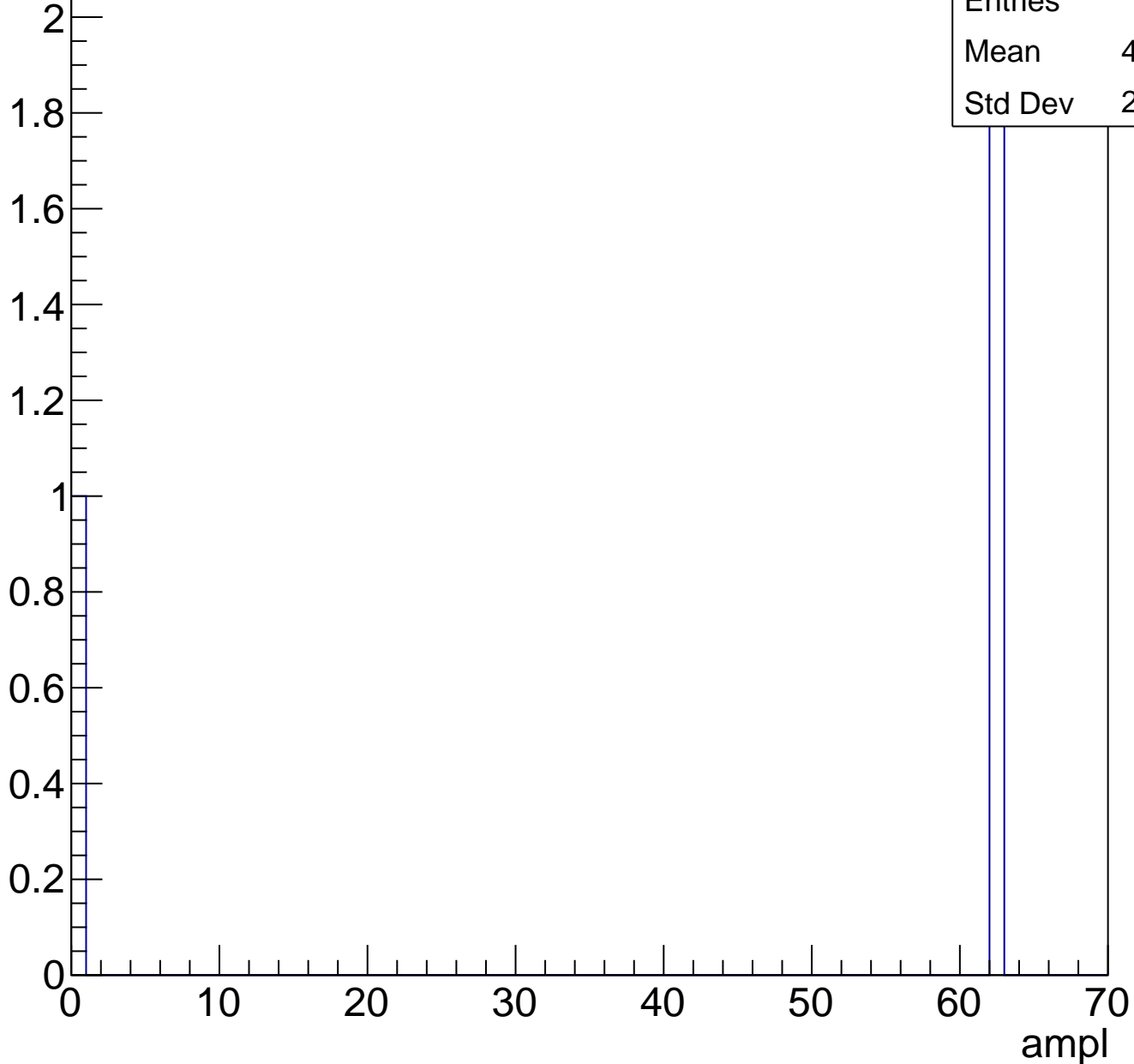




# B1L102S, U5-ch104, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U5-ch105, adc0

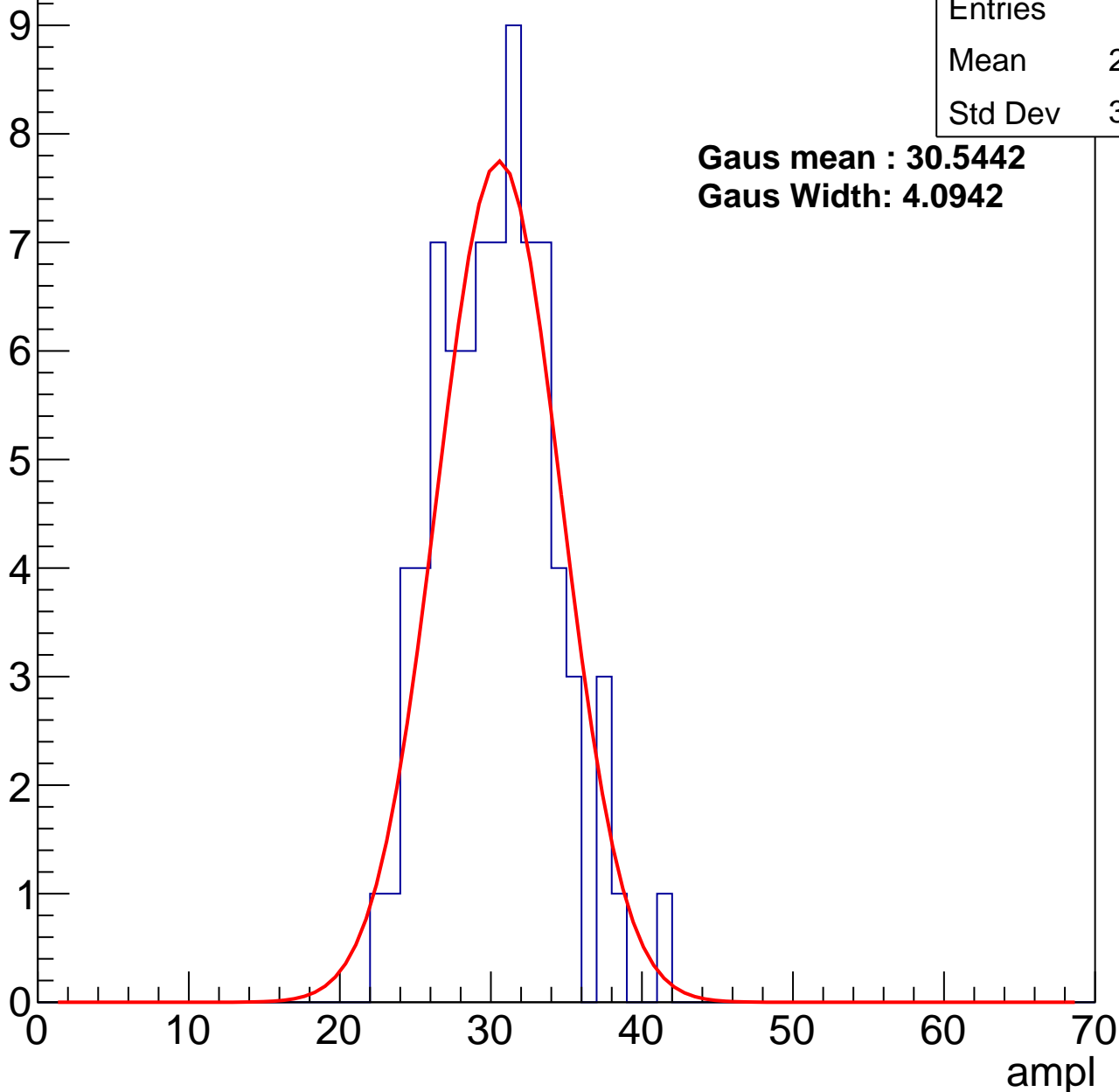
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	78
Mean	29.88
Std Dev	3.796

**Gaus mean : 30.5442**

**Gaus Width: 4.0942**



# B1L102S, U5-ch105, adc1

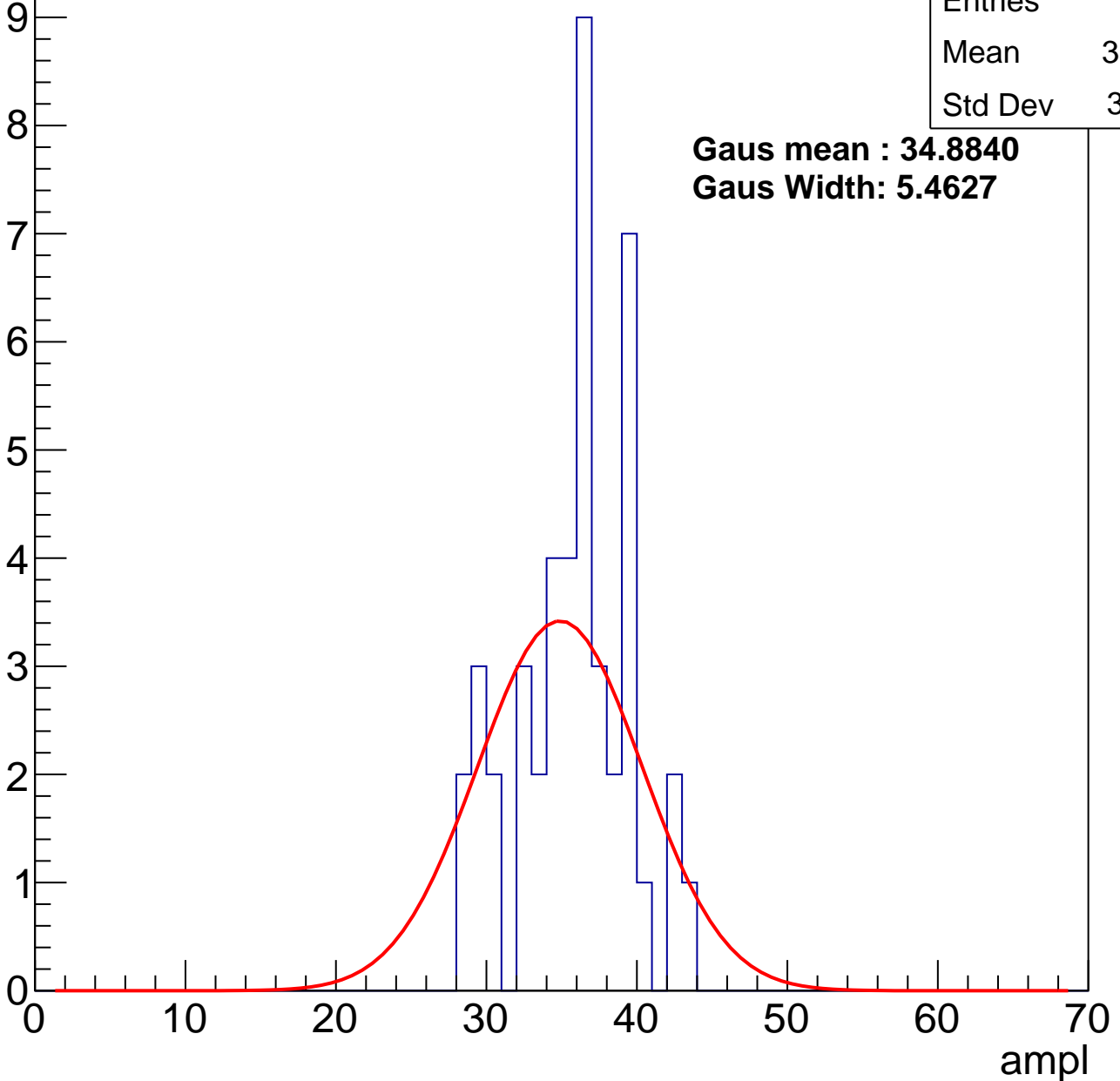
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	45
Mean	35.38
Std Dev	3.731

**Gaus mean : 34.8840**

**Gaus Width: 5.4627**



# B1L102S, U5-ch105, adc2

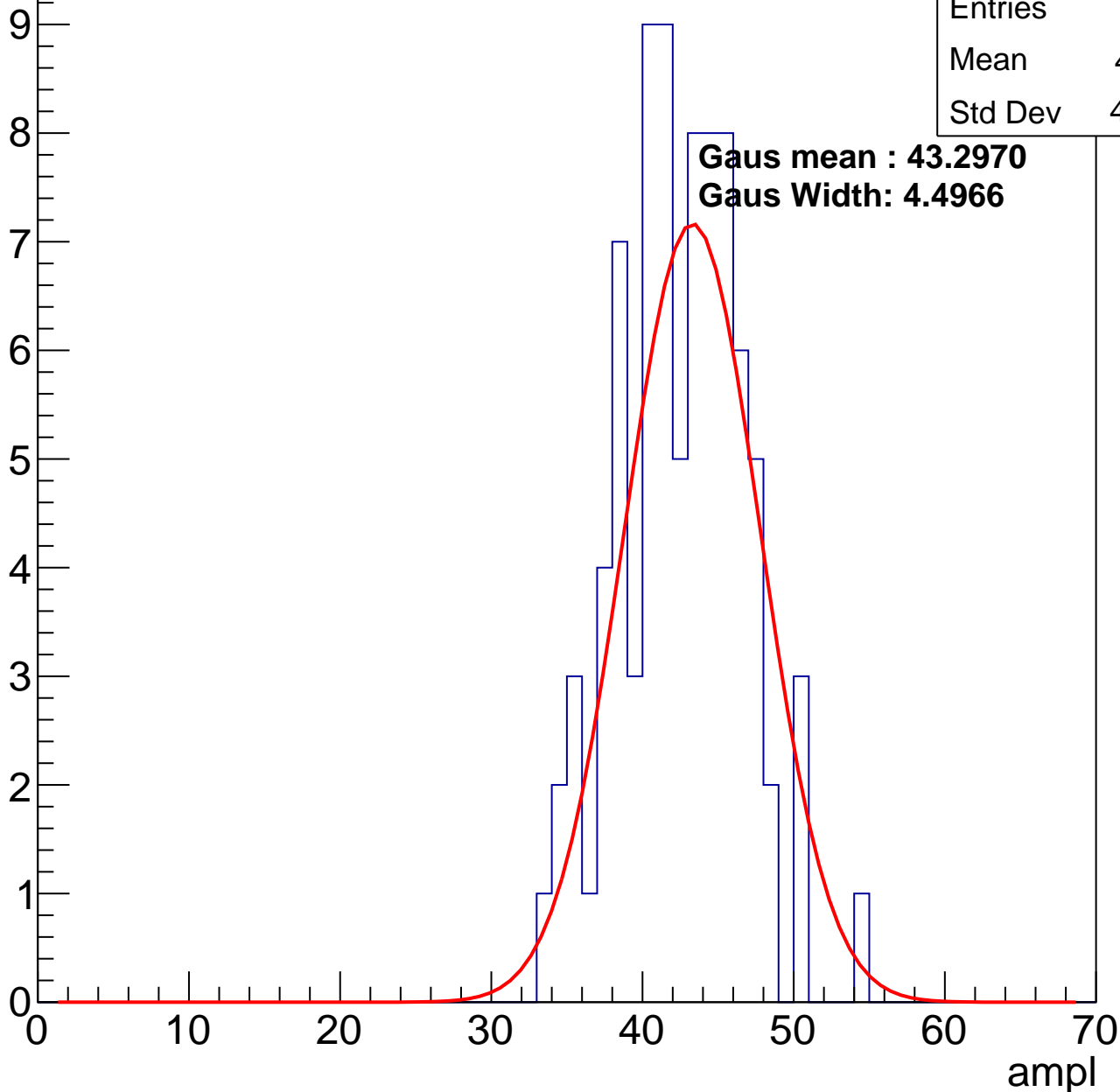
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	85
Mean	42.11
Std Dev	4.082

**Gaus mean : 43.2970**

**Gaus Width: 4.4966**

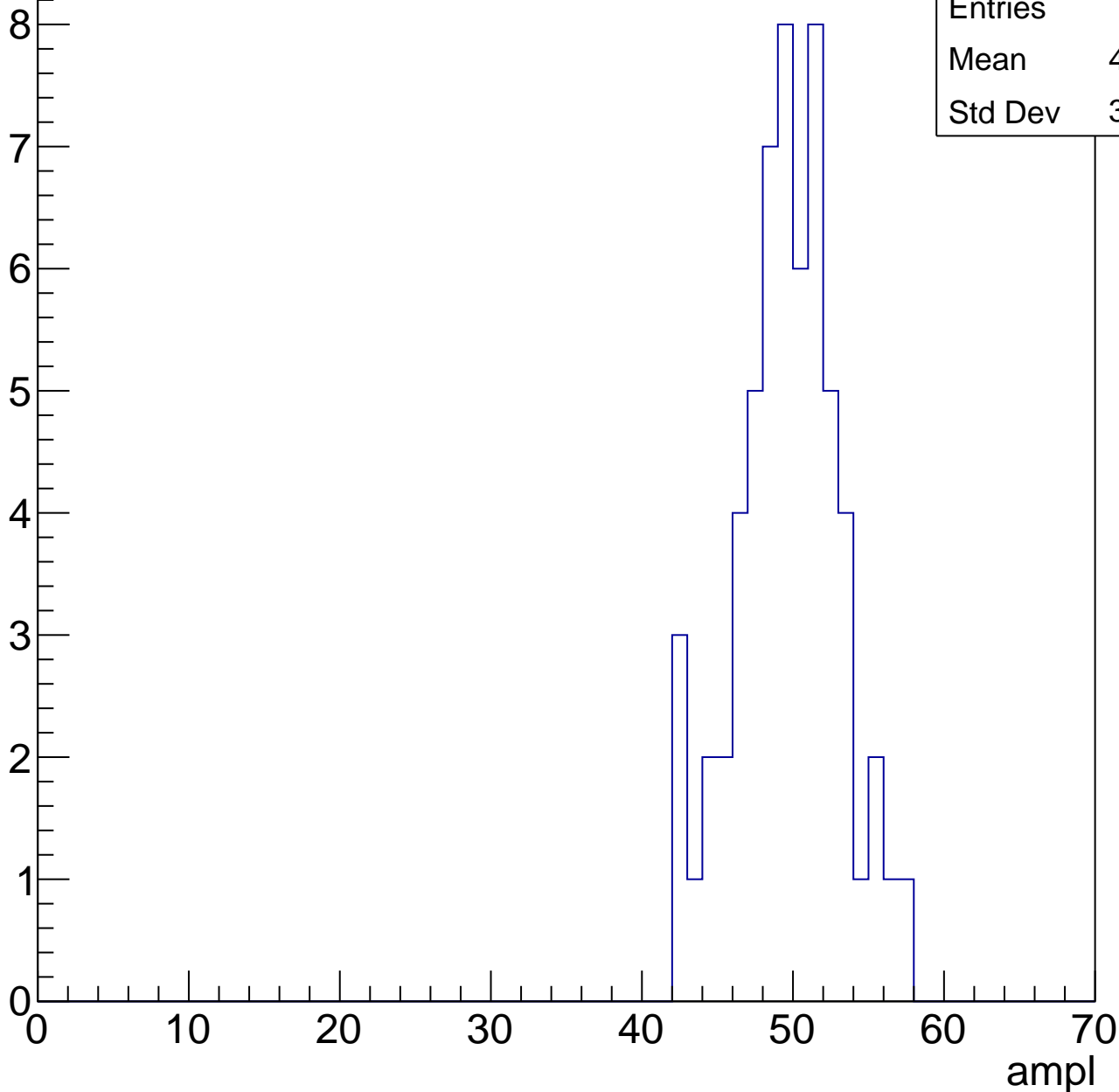


# B1L102S, U5-ch105, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

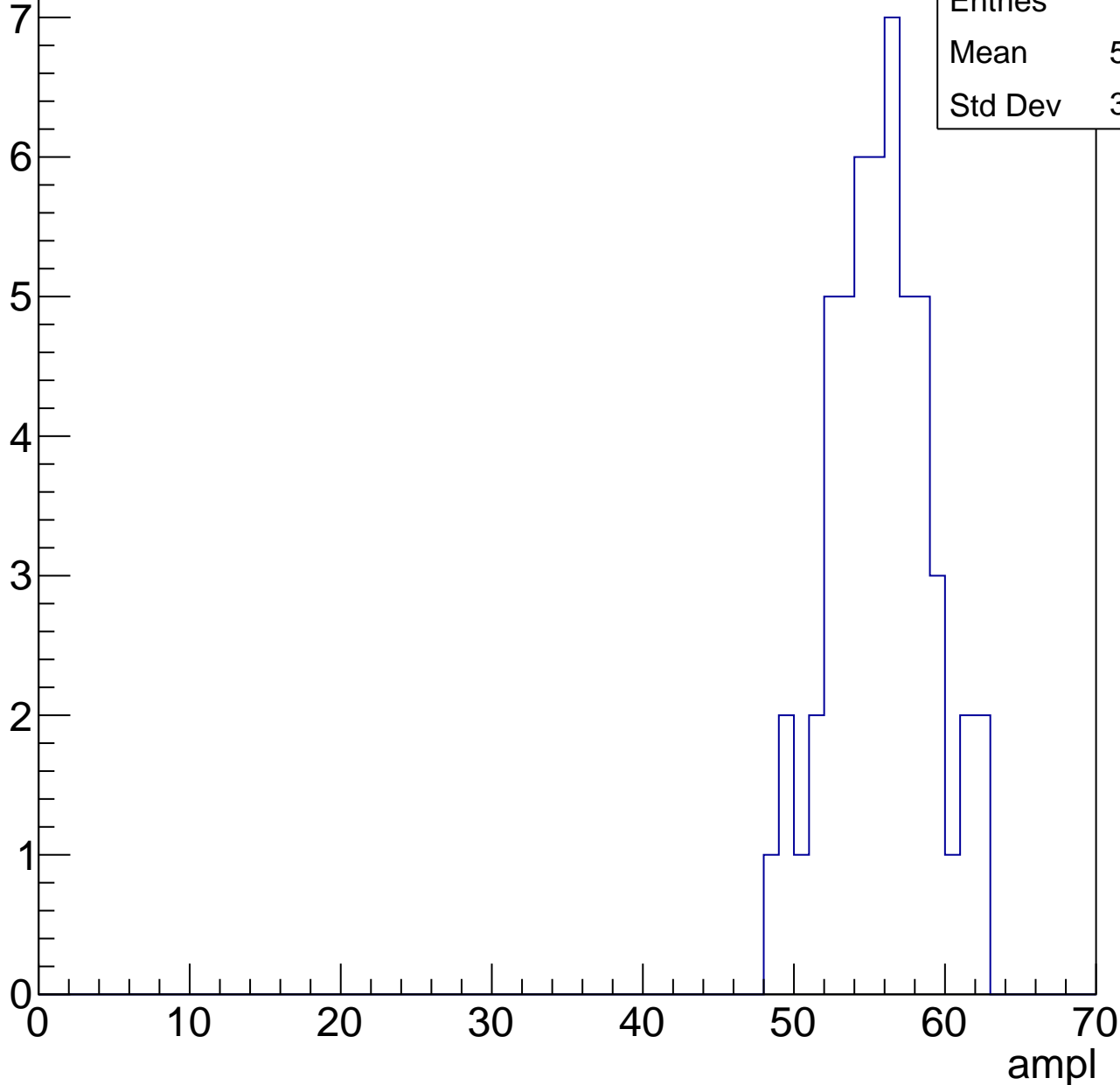
Entries	60
Mean	49.18
Std Dev	3.374



# B1L102S, U5-ch105, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



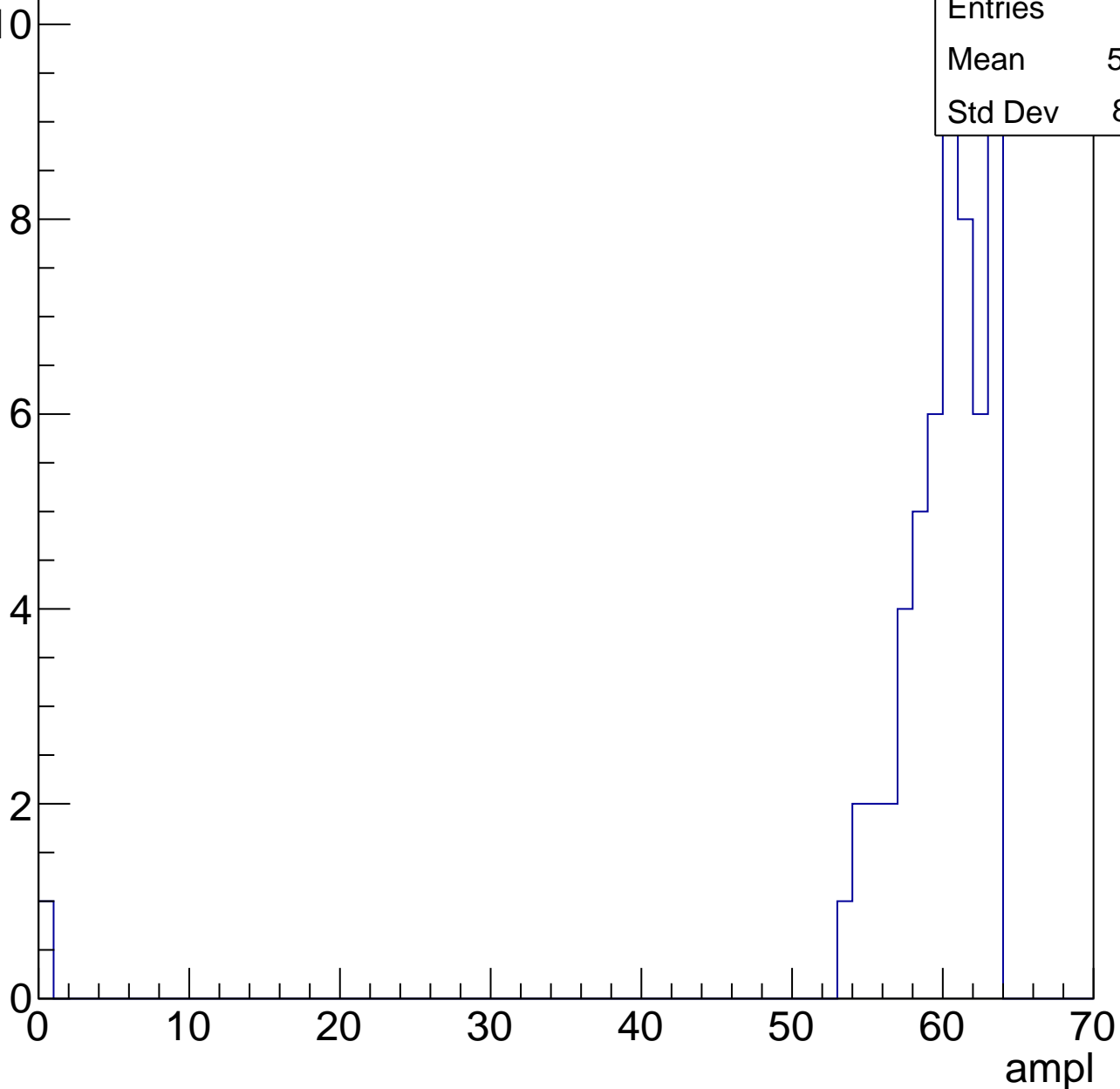
Entries	53
Mean	55.23
Std Dev	3.254

# B1L102S, U5-ch105, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

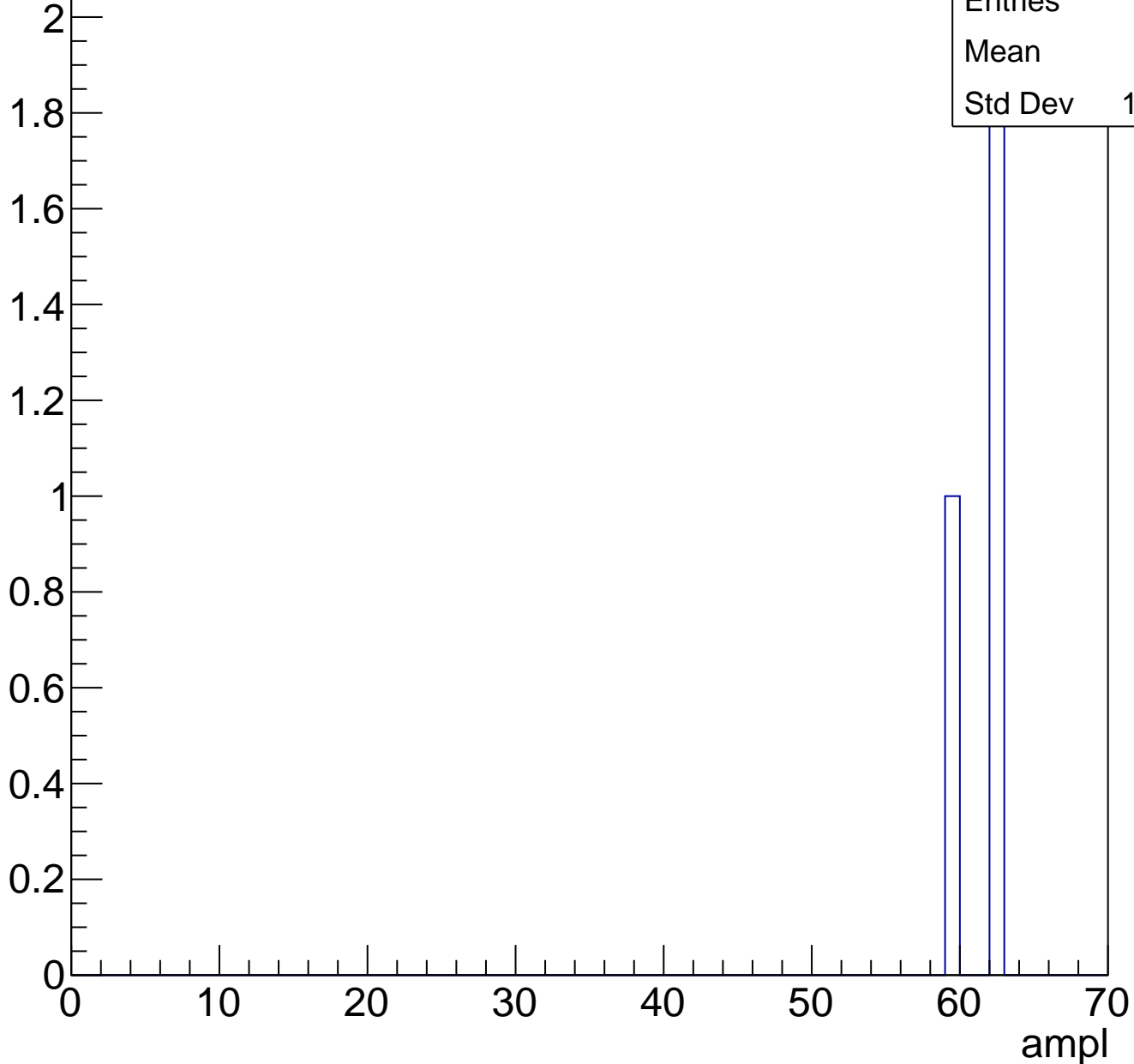
Entries	56
Mean	58.66
Std Dev	8.331



# B1L102S, U5-ch105, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U5-ch105, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U5-ch106, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	81
Mean	24.49
Std Dev	5.953

**Gaus mean : 26.6518**

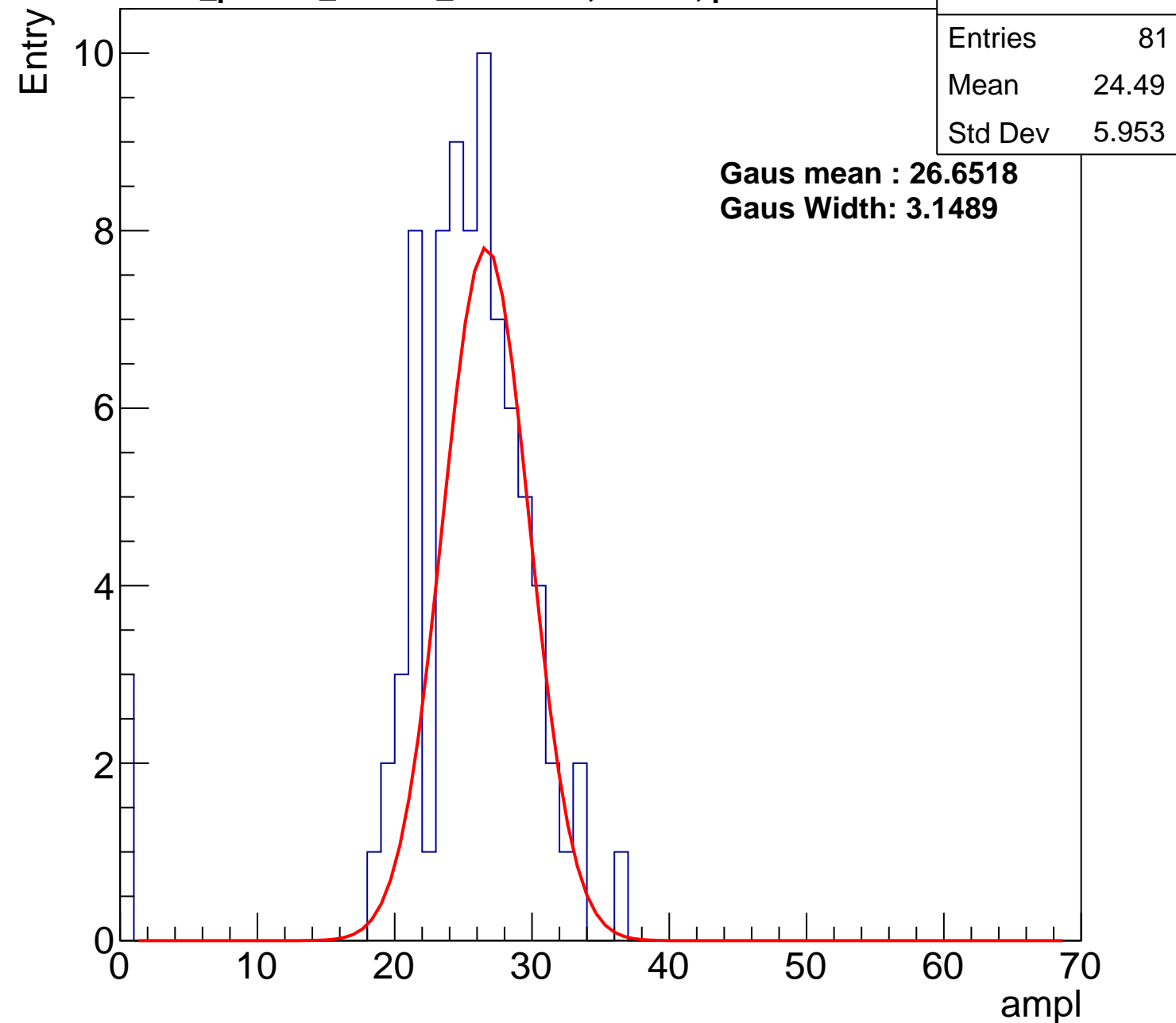
**Gaus Width: 3.1489**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U5-ch106, adc1

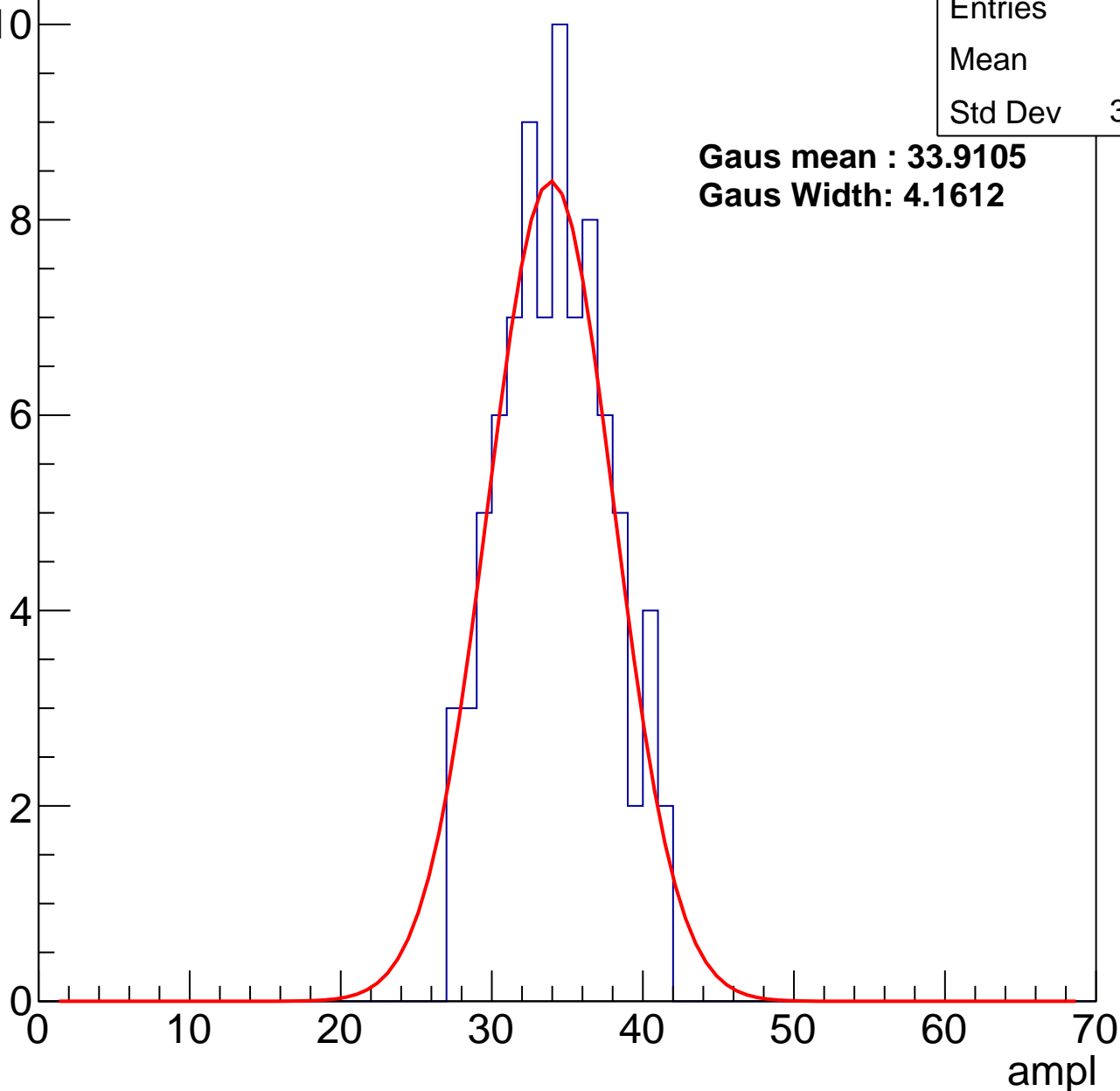
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	84
Mean	33.7
Std Dev	3.518

**Gaus mean : 33.9105**

**Gaus Width: 4.1612**



# B1L102S, U5-ch106, adc2

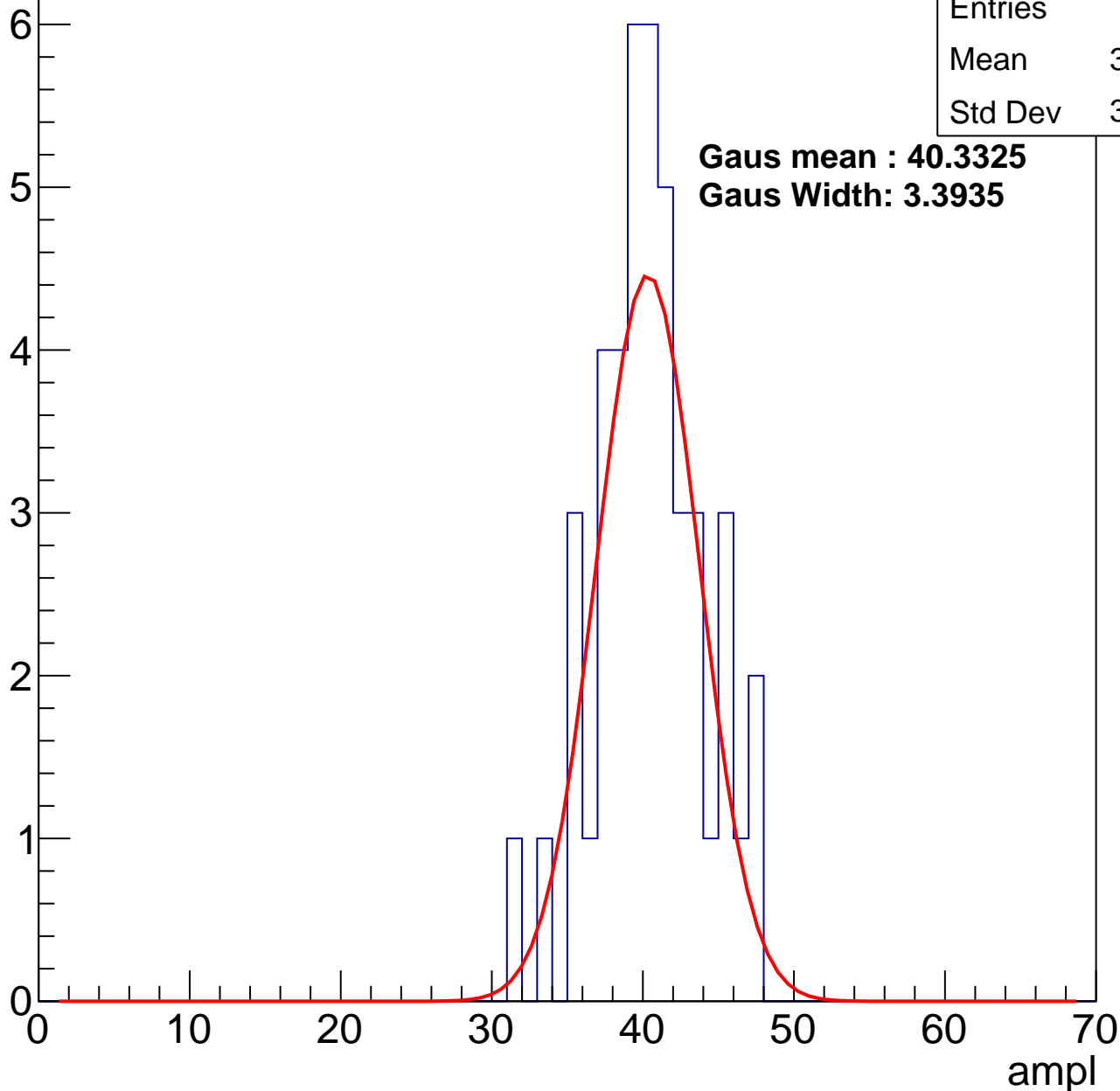
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	44
Mean	39.95
Std Dev	3.529

**Gaus mean : 40.3325**

**Gaus Width: 3.3935**

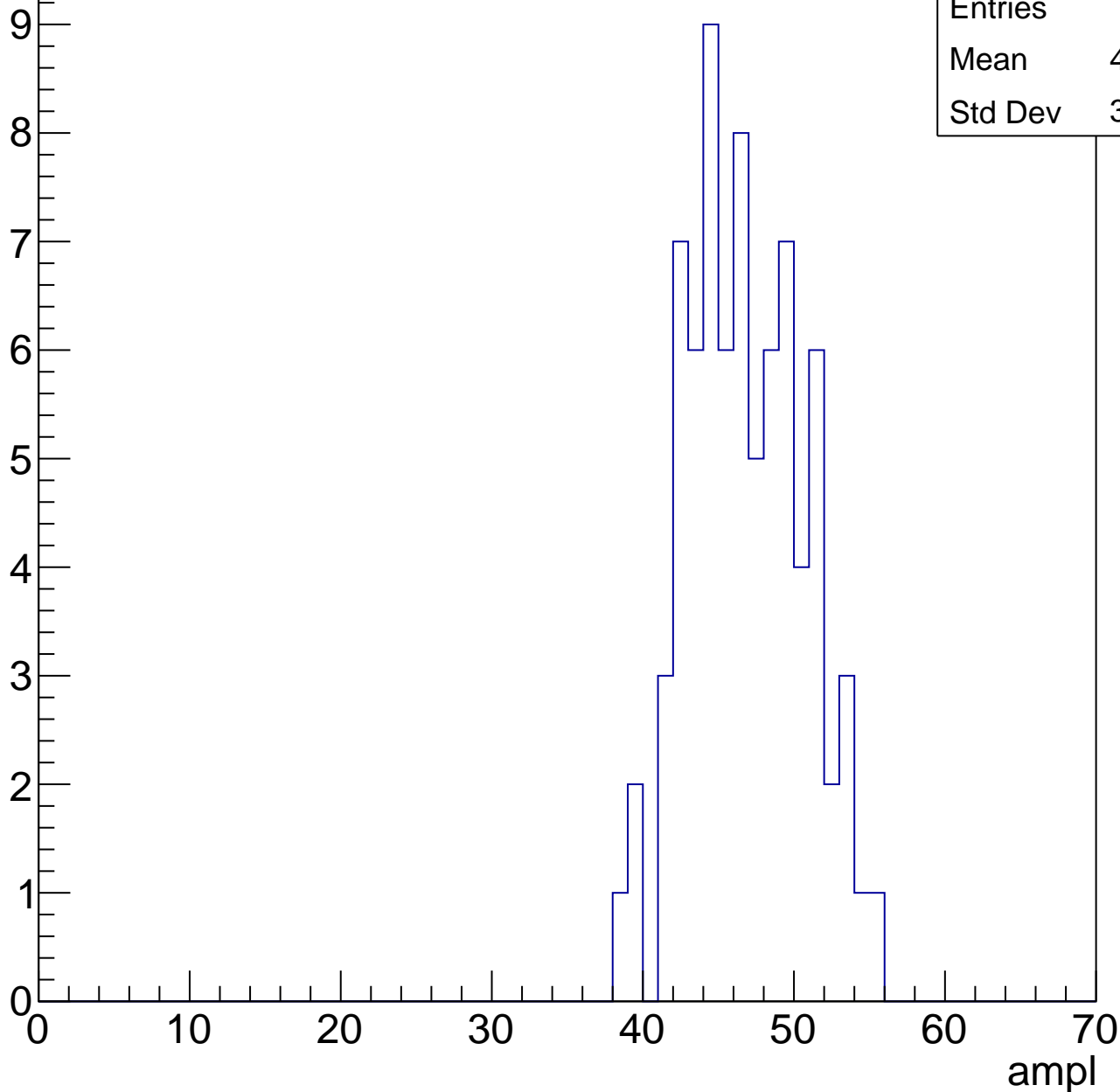


# B1L102S, U5-ch106, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	46.35
Std Dev	3.789

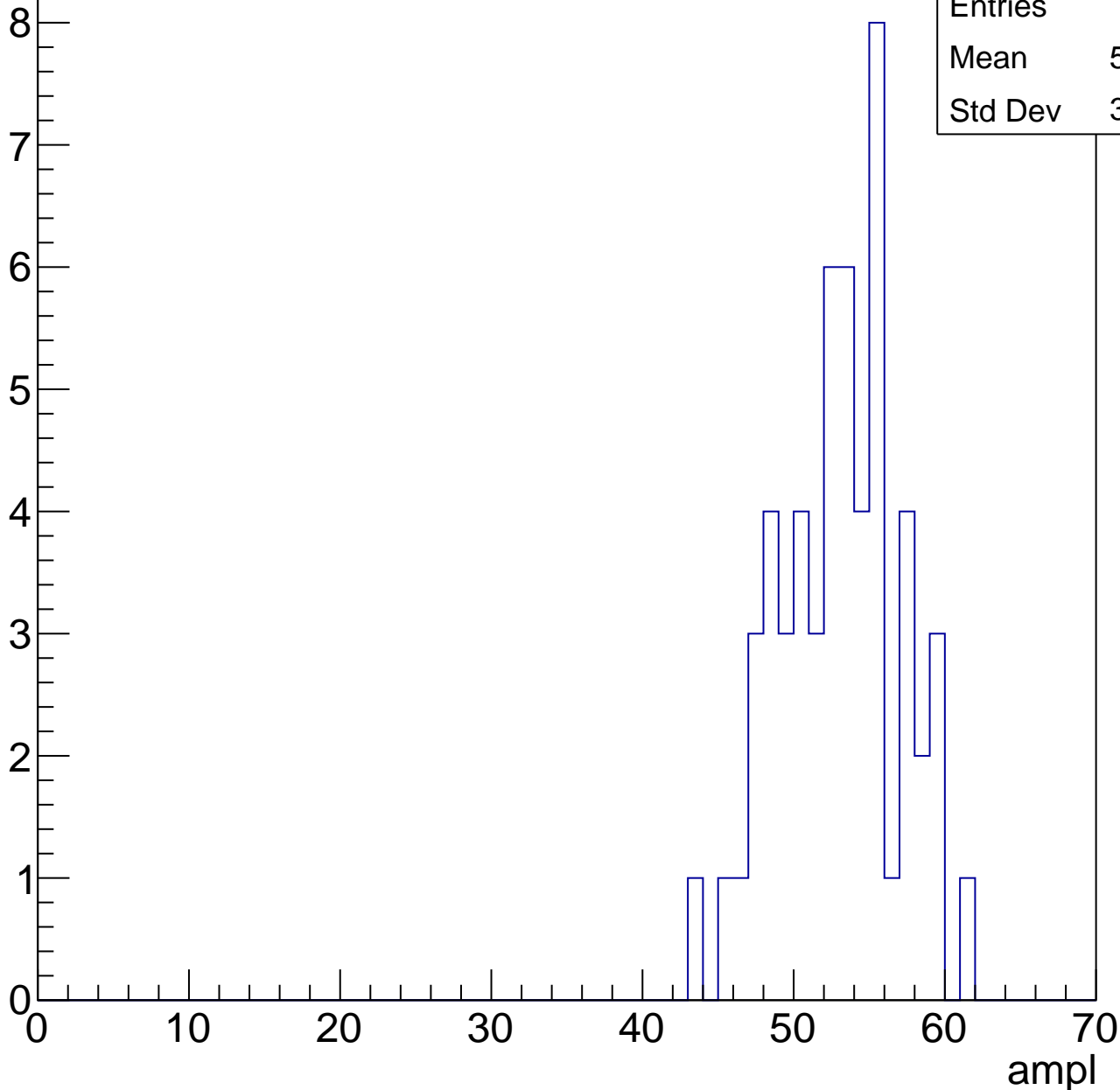


# B1L102S, U5-ch106, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	52.56
Std Dev	3.916

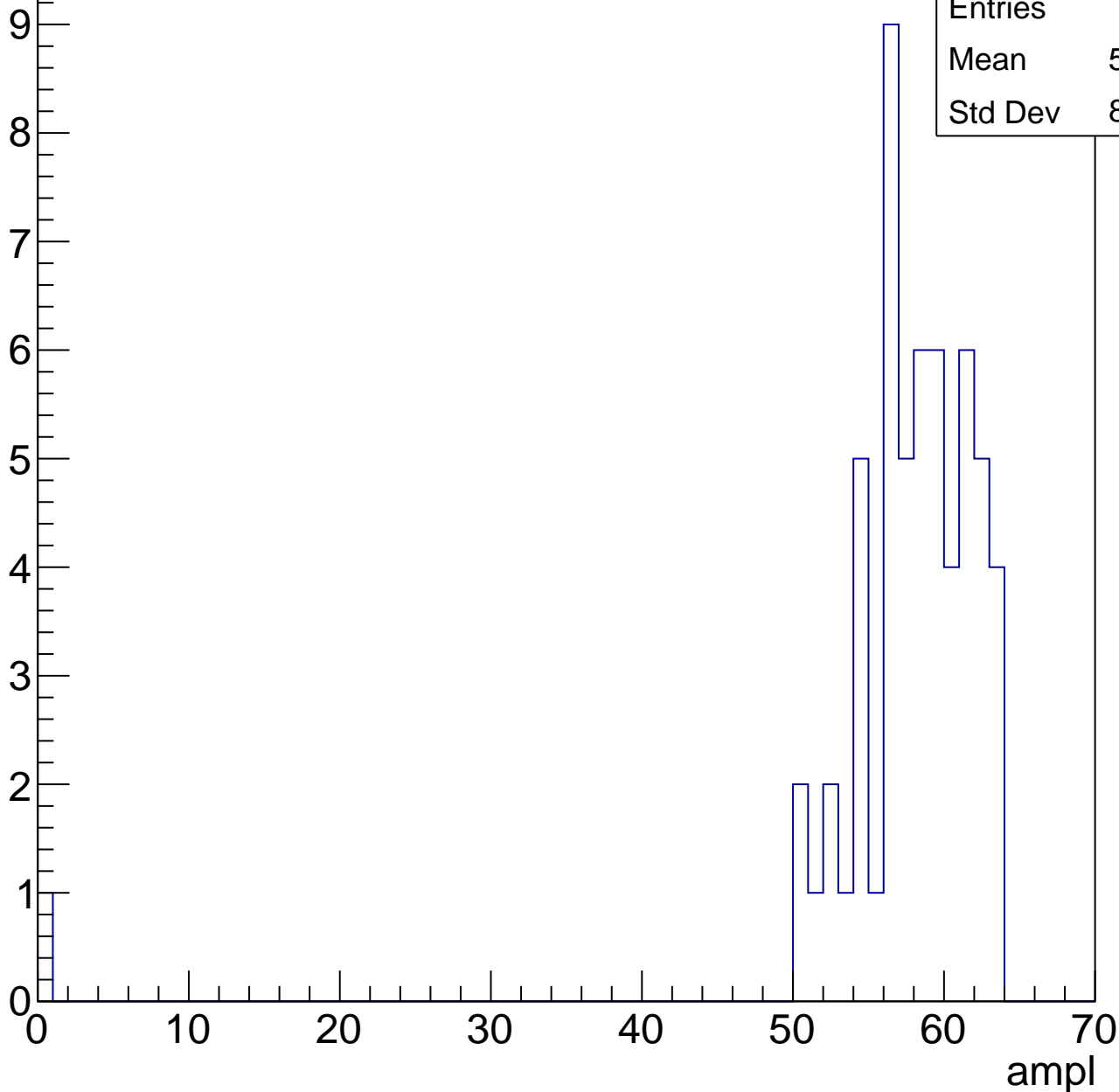


# B1L102S, U5-ch106, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	56.76
Std Dev	8.236

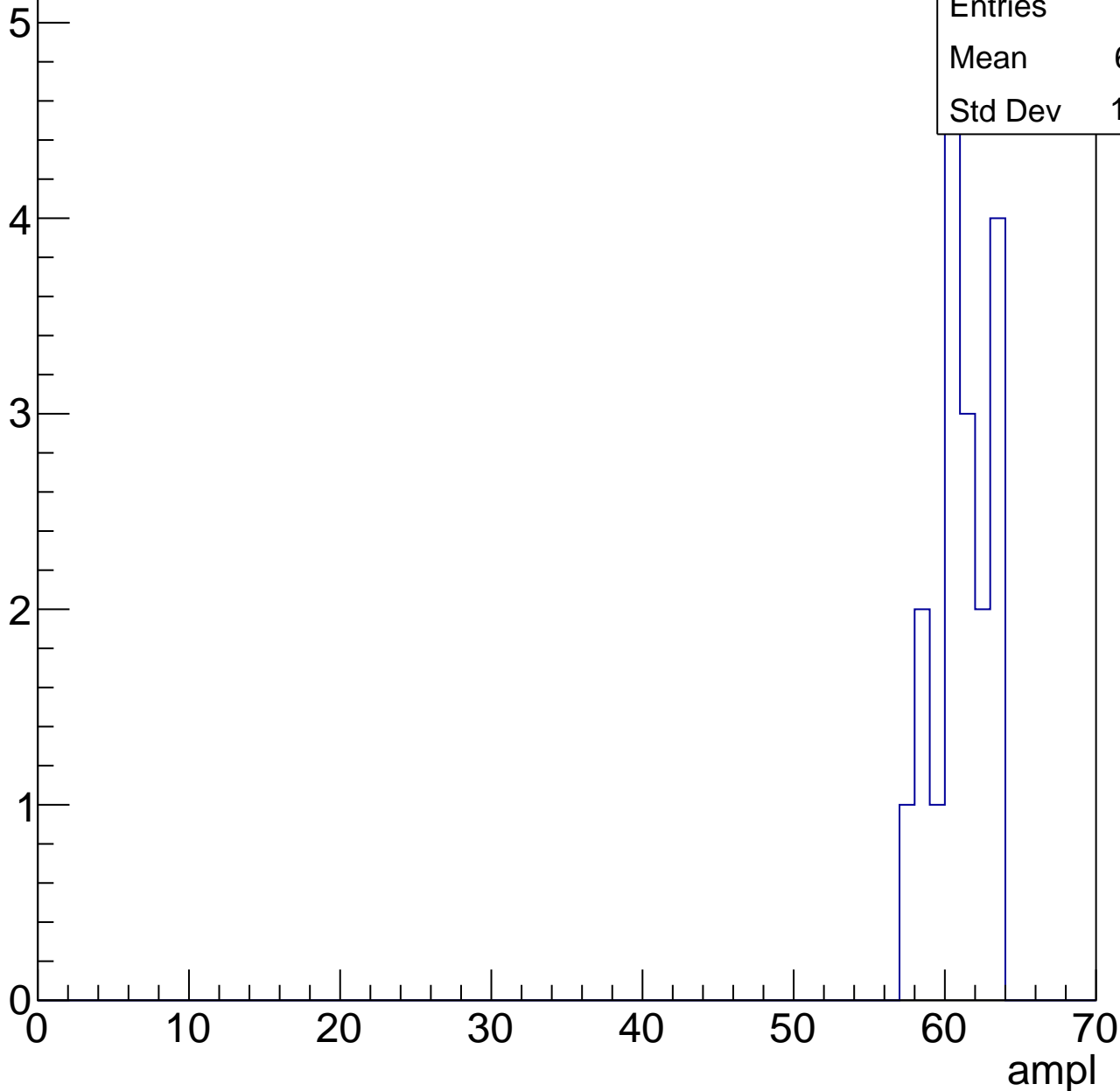


# B1L102S, U5-ch106, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	18
Mean	60.61
Std Dev	1.799

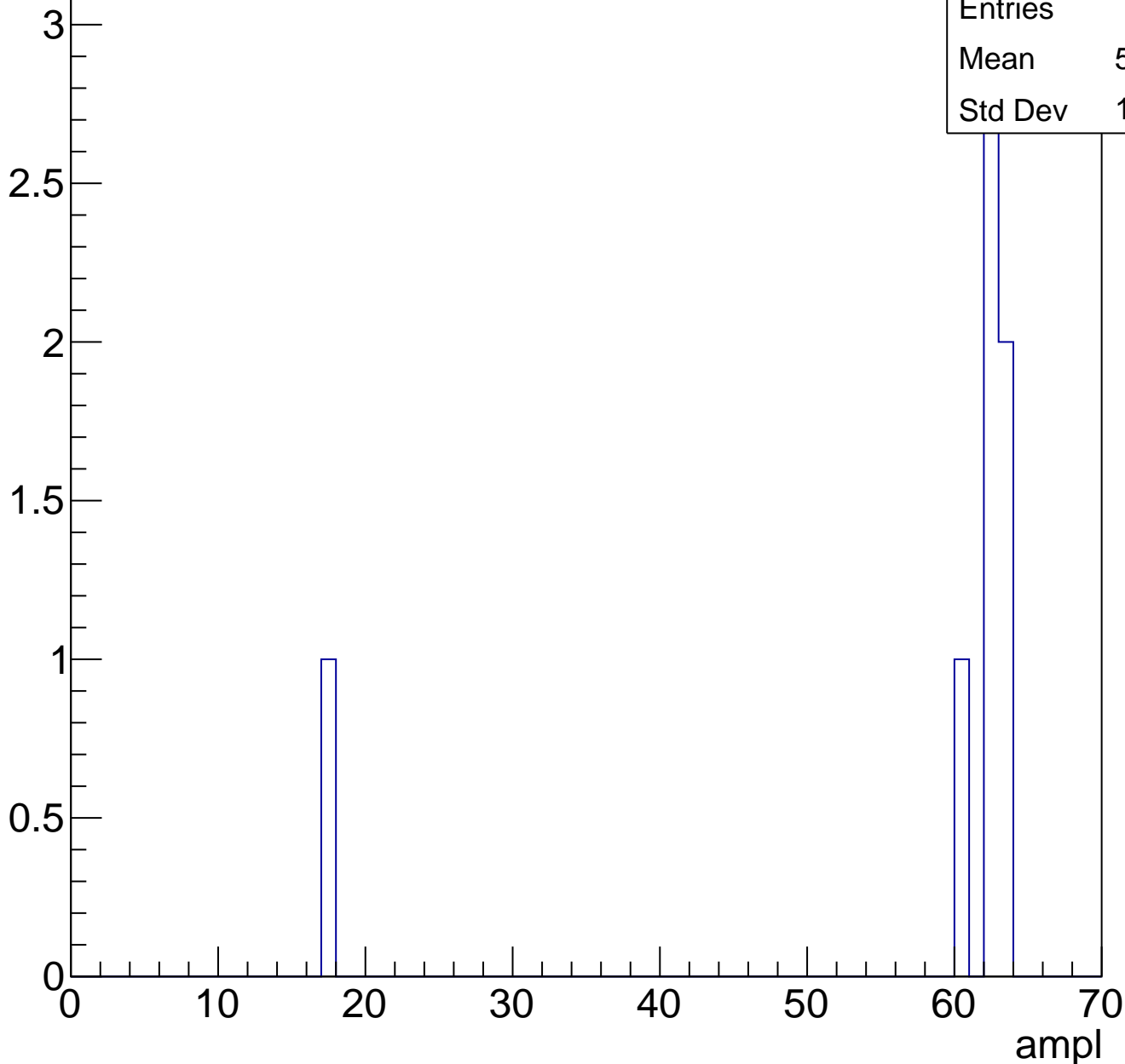




# B1L102S, U5-ch106, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U5-ch107, adc0

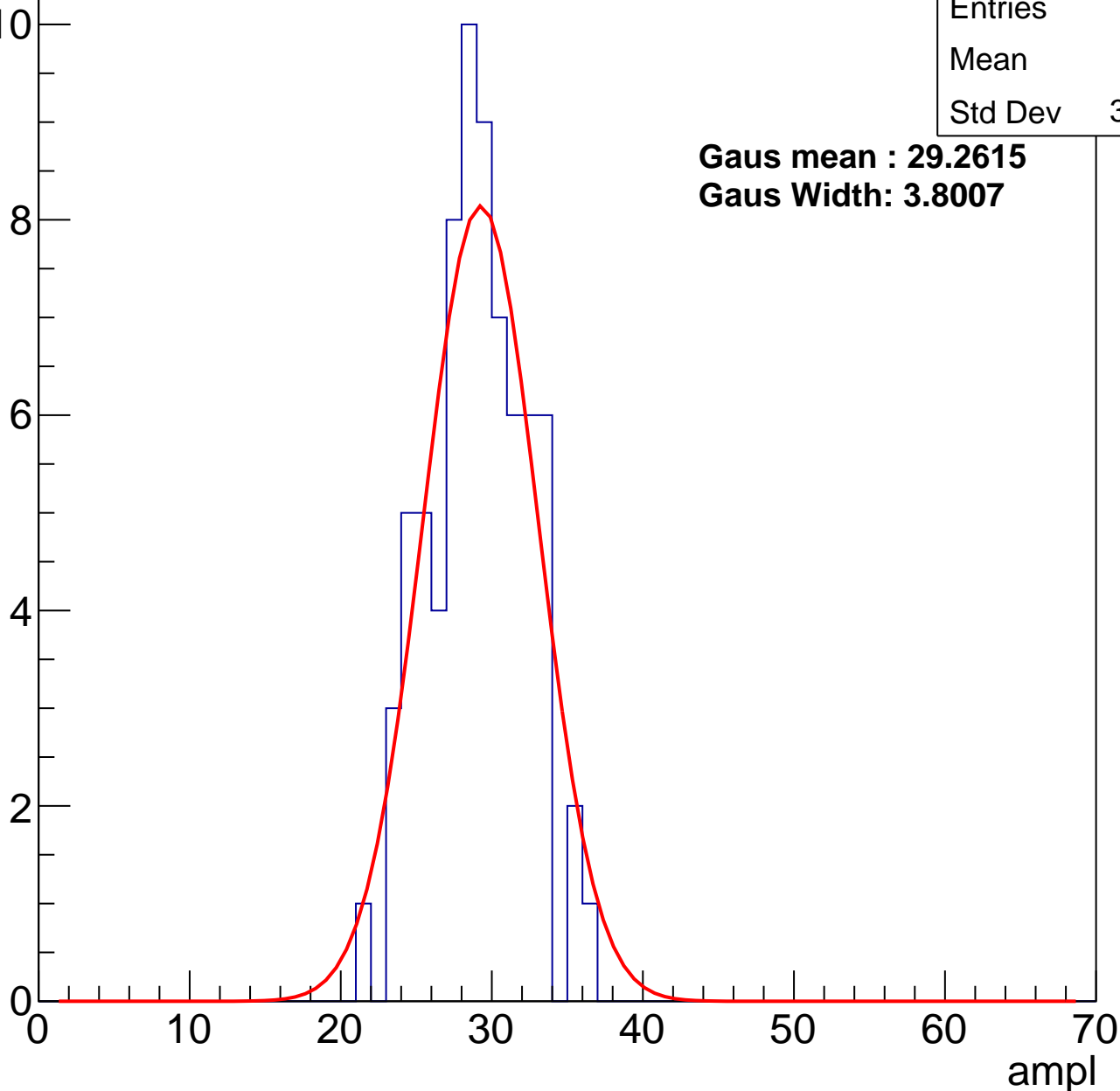
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	28.6
Std Dev	3.196

**Gaus mean : 29.2615**

**Gaus Width: 3.8007**



# B1L102S, U5-ch107, adc1

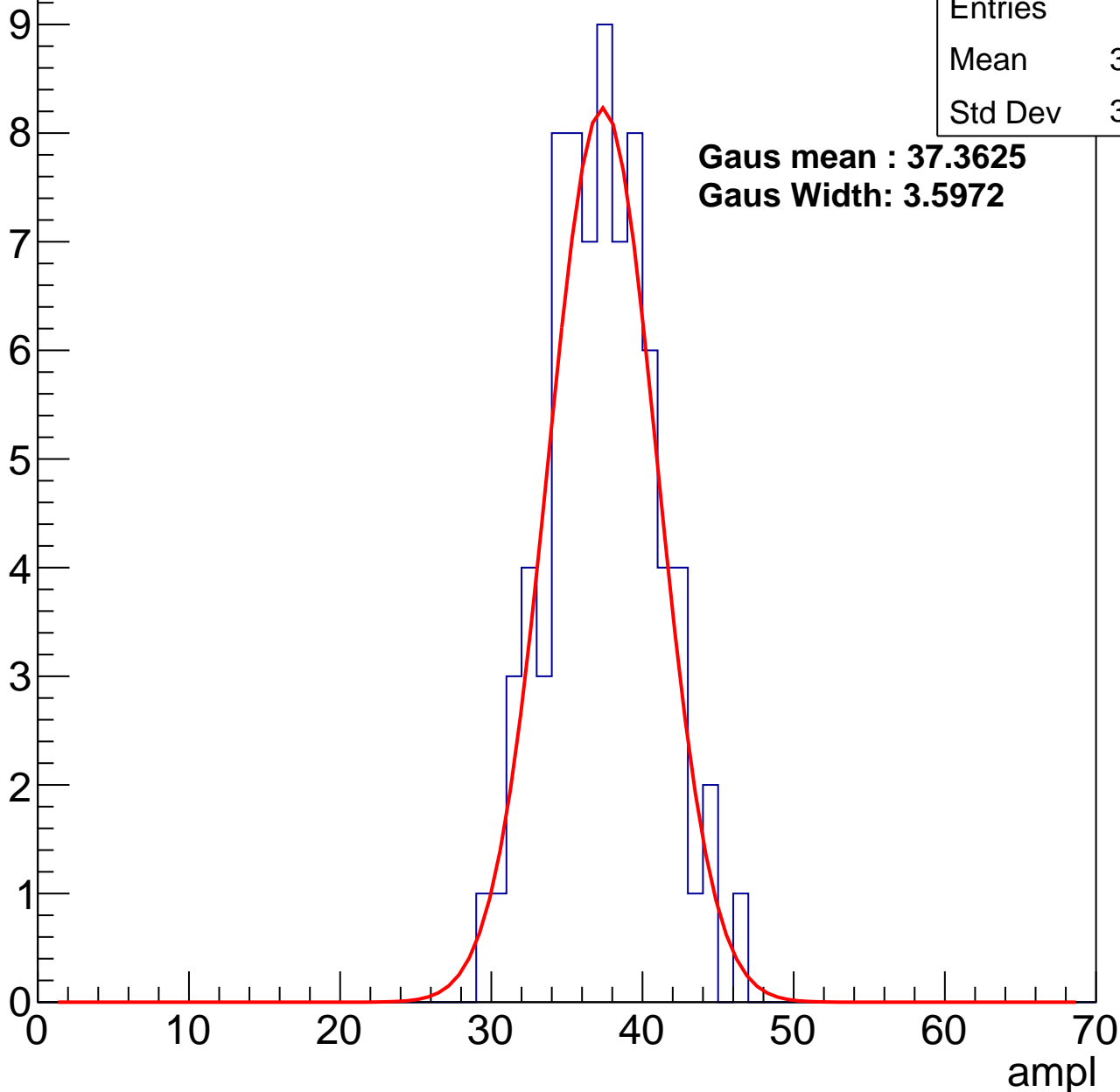
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	36.92
Std Dev	3.515

**Gaus mean : 37.3625**

**Gaus Width: 3.5972**



# B1L102S, U5-ch107, adc2

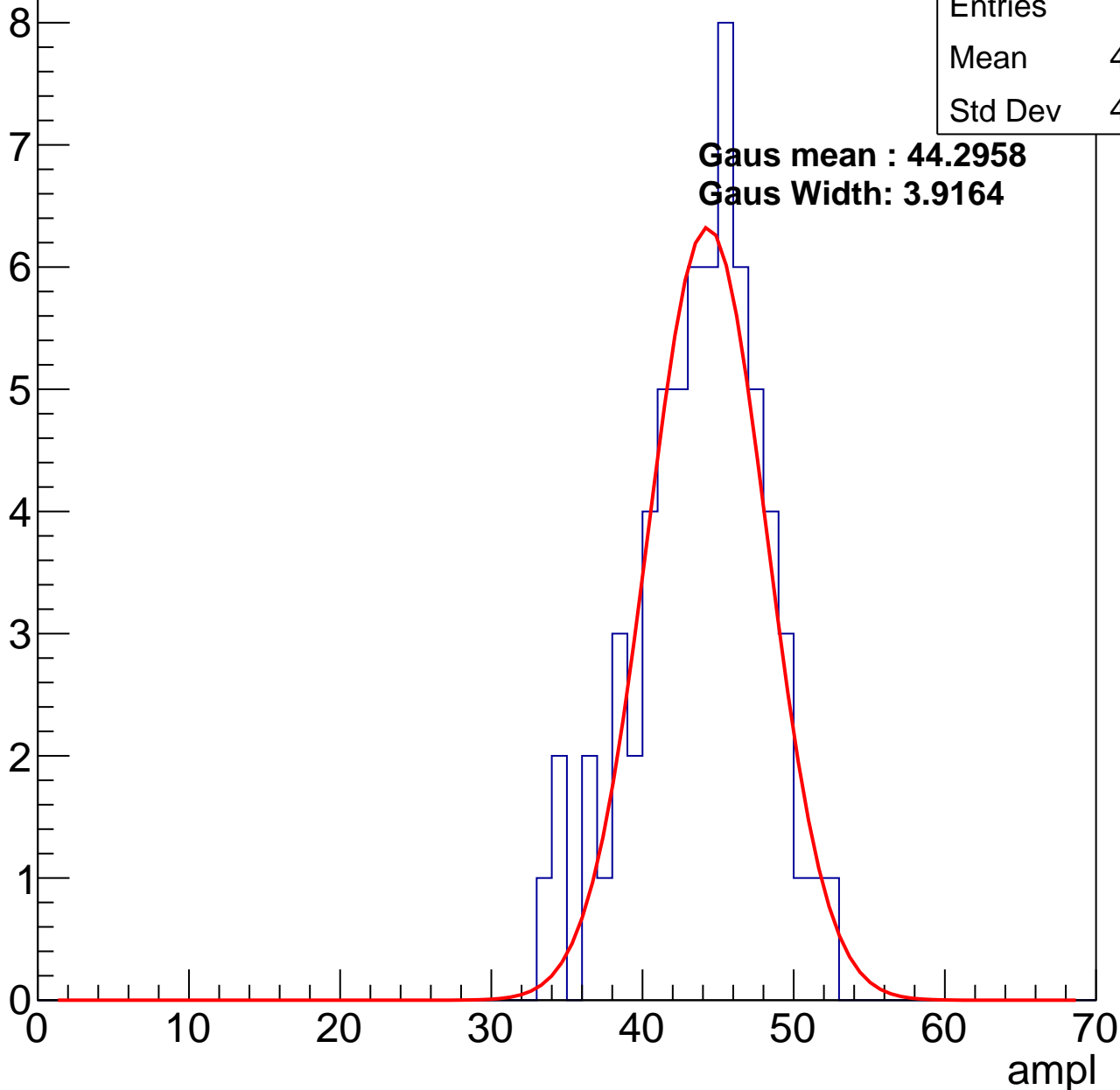
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	43.36
Std Dev	4.136

**Gaus mean : 44.2958**

**Gaus Width: 3.9164**

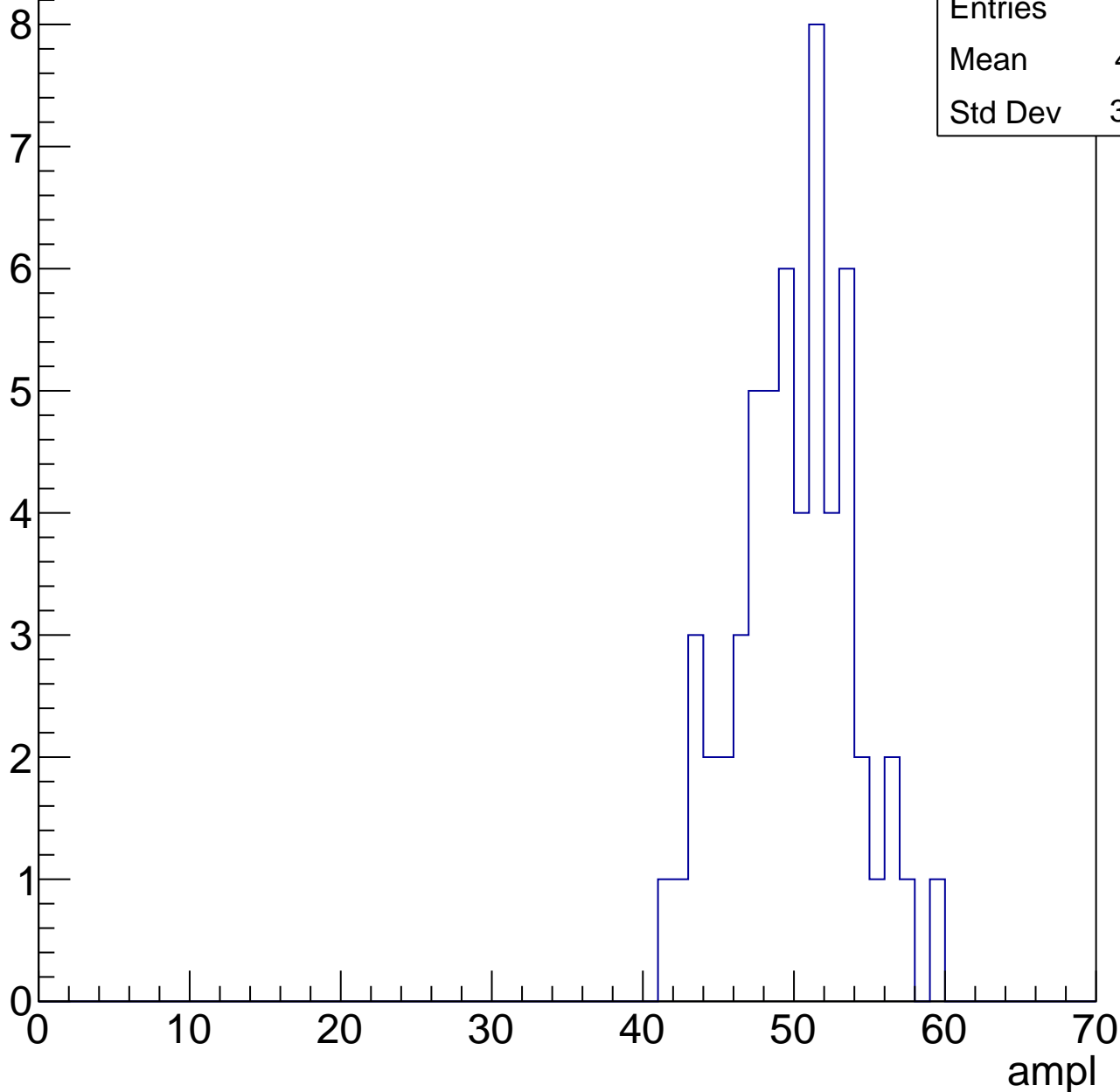


# B1L102S, U5-ch107, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	49.51
Std Dev	3.876

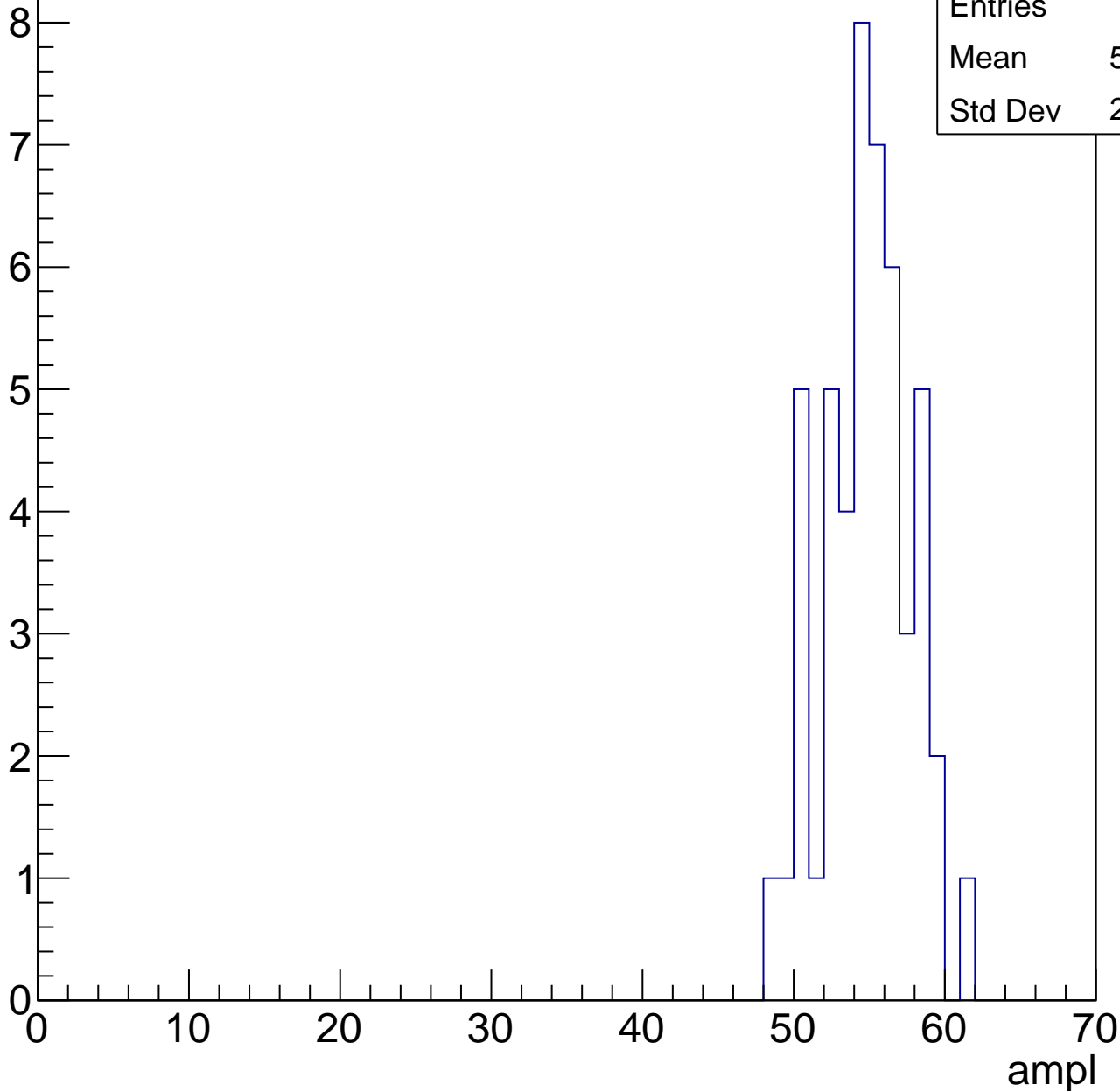


# B1L102S, U5-ch107, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

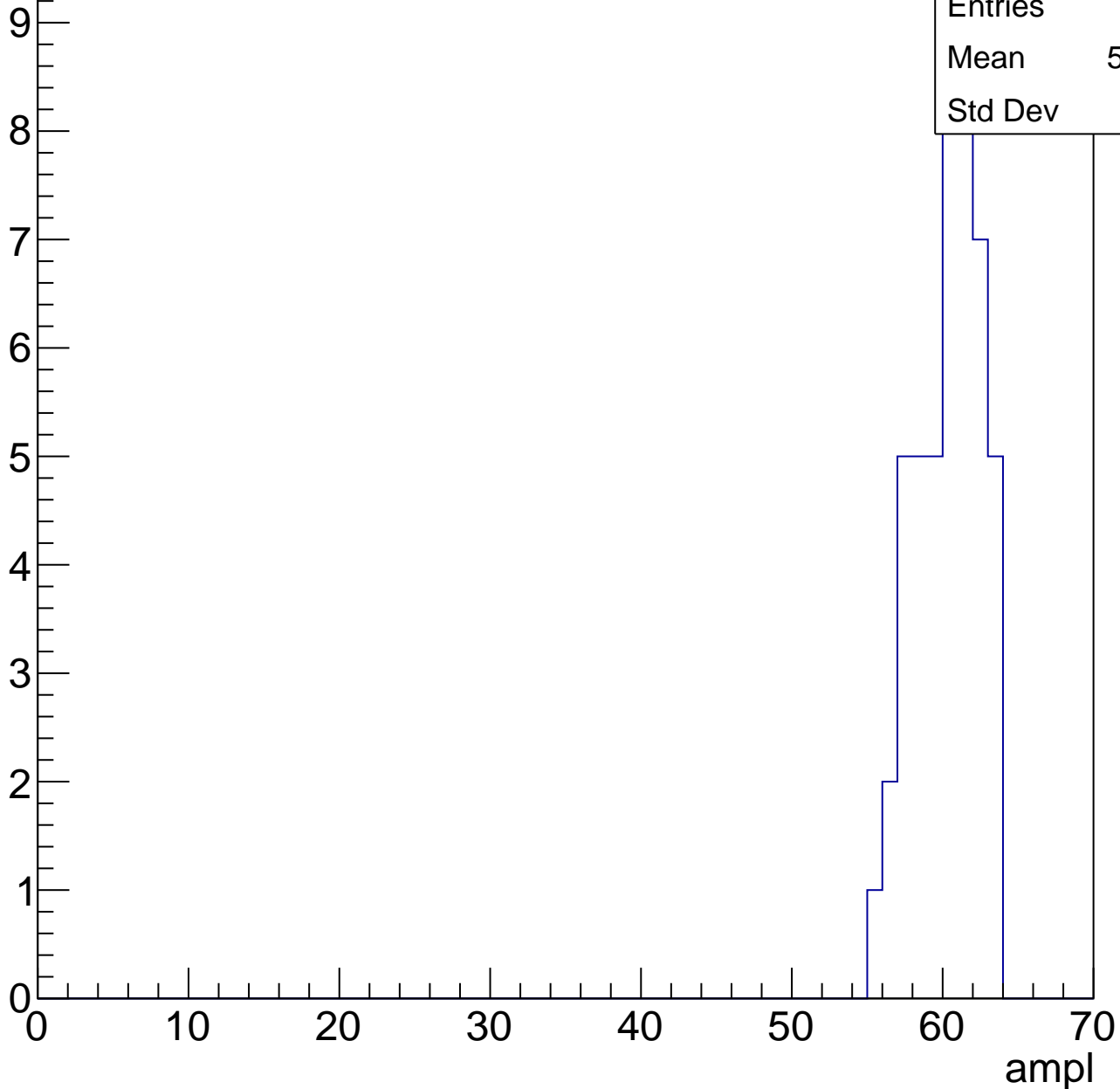
Entries	49
Mean	54.35
Std Dev	2.875



# B1L102S, U5-ch107, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



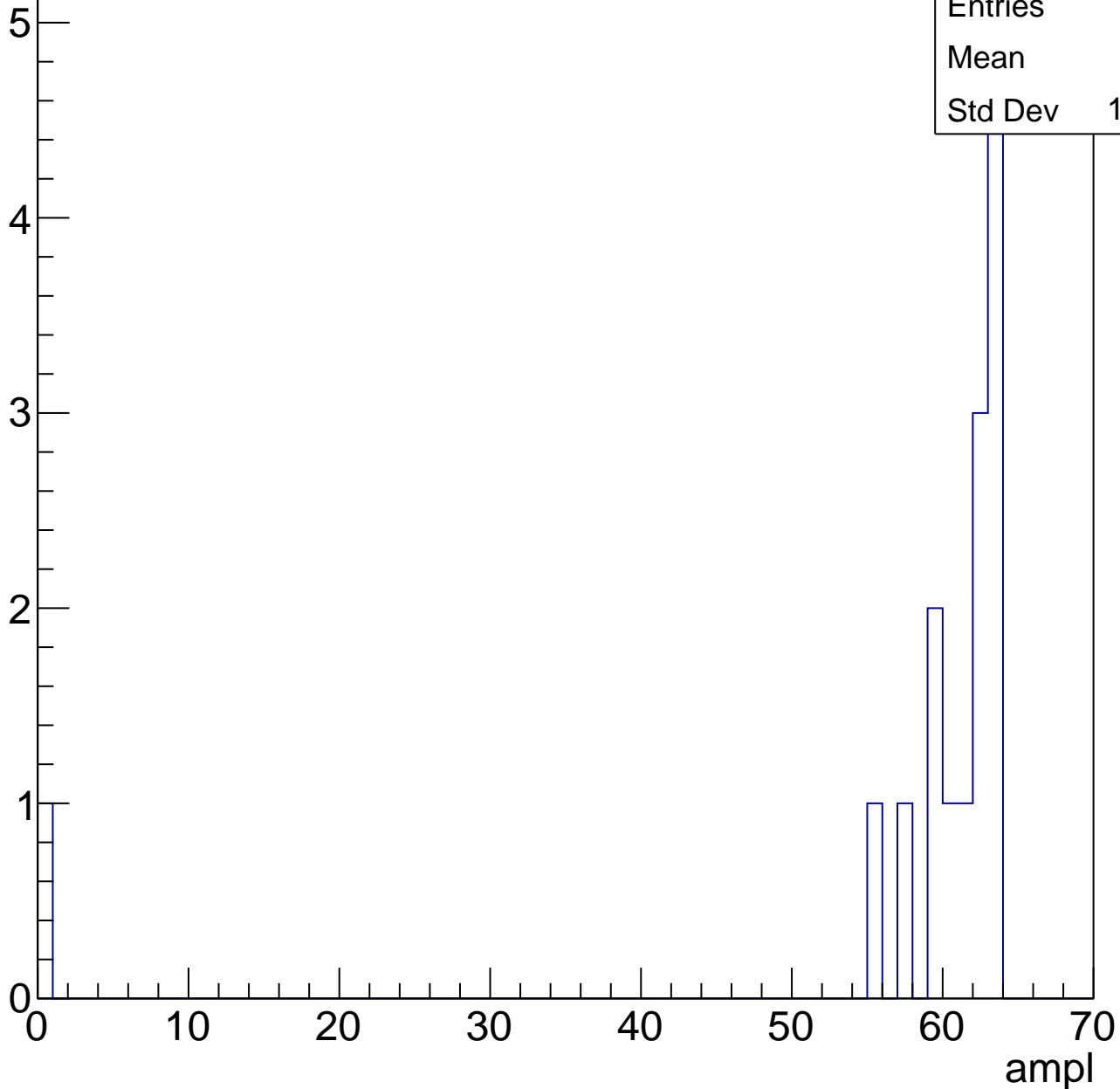
Entries	47
Mean	59.87
Std Dev	2.1

# B1L102S, U5-ch107, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	15
Mean	56.8
Std Dev	15.36





# B1L102S, U5-ch107, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L102S, U5-ch108, adc0

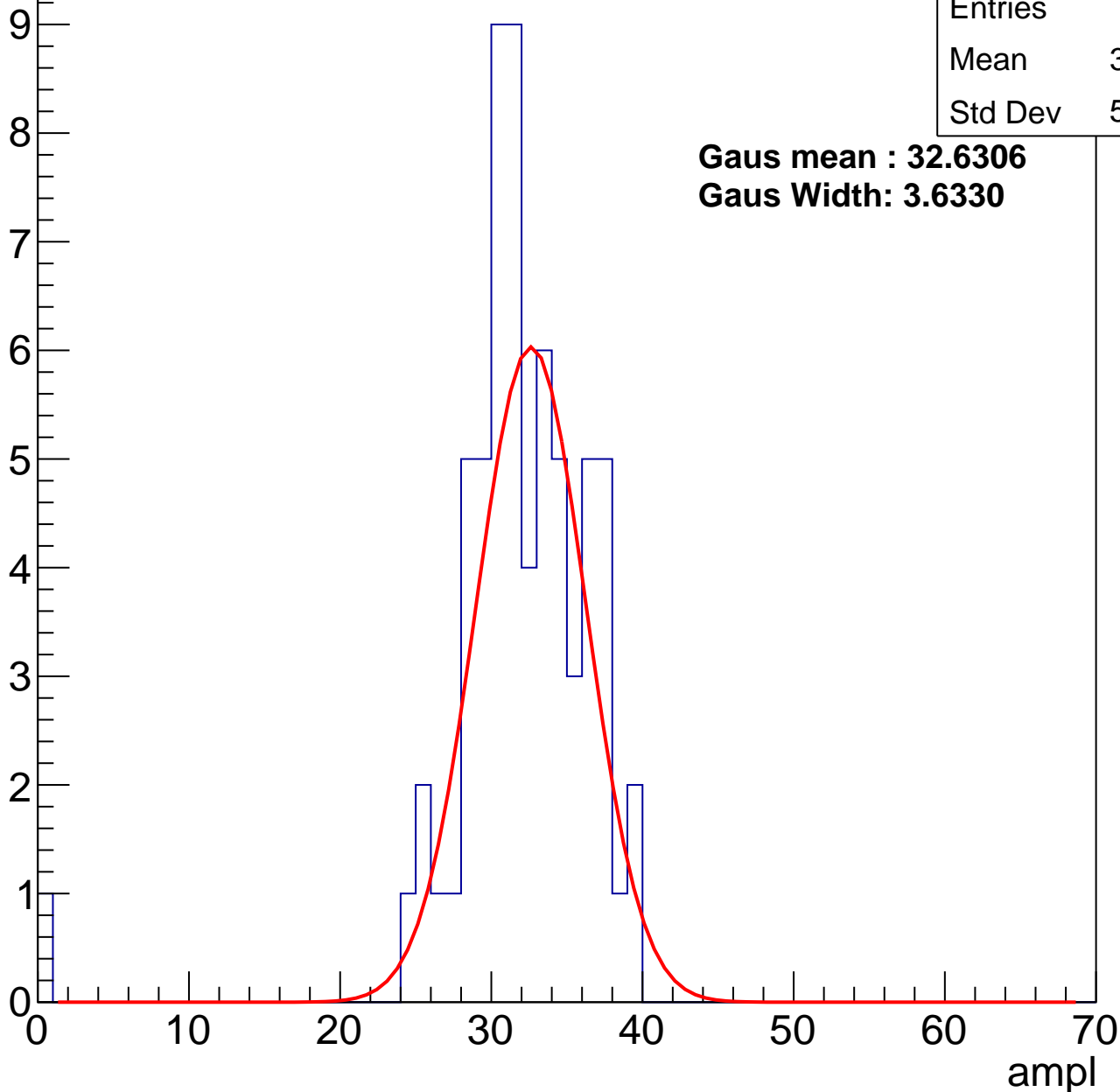
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	31.43
Std Dev	5.245

**Gaus mean : 32.6306**

**Gaus Width: 3.6330**



# B1L102S, U5-ch108, adc1

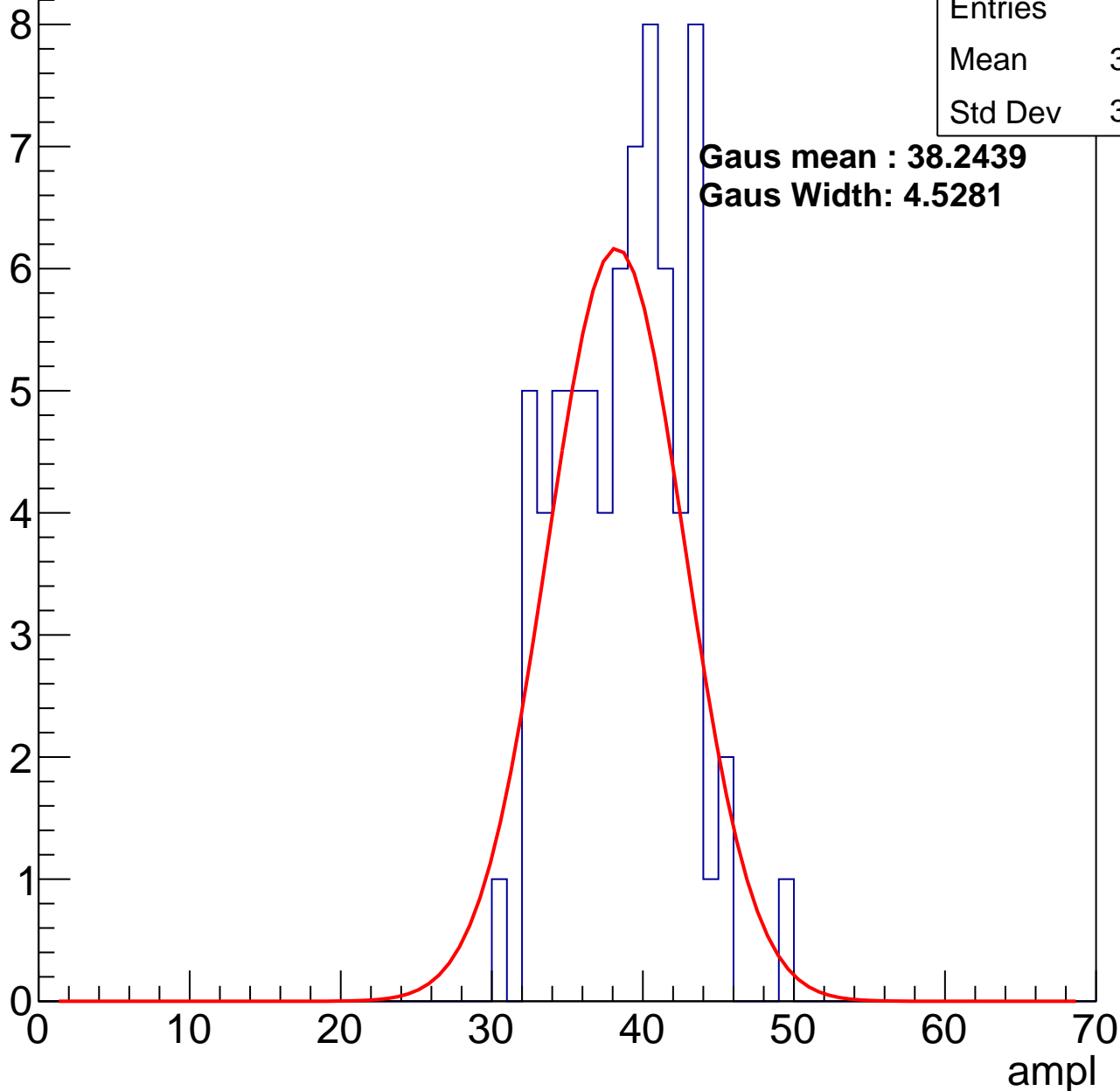
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	38.29
Std Dev	3.907

**Gaus mean : 38.2439**

**Gaus Width: 4.5281**



# B1L102S, U5-ch108, adc2

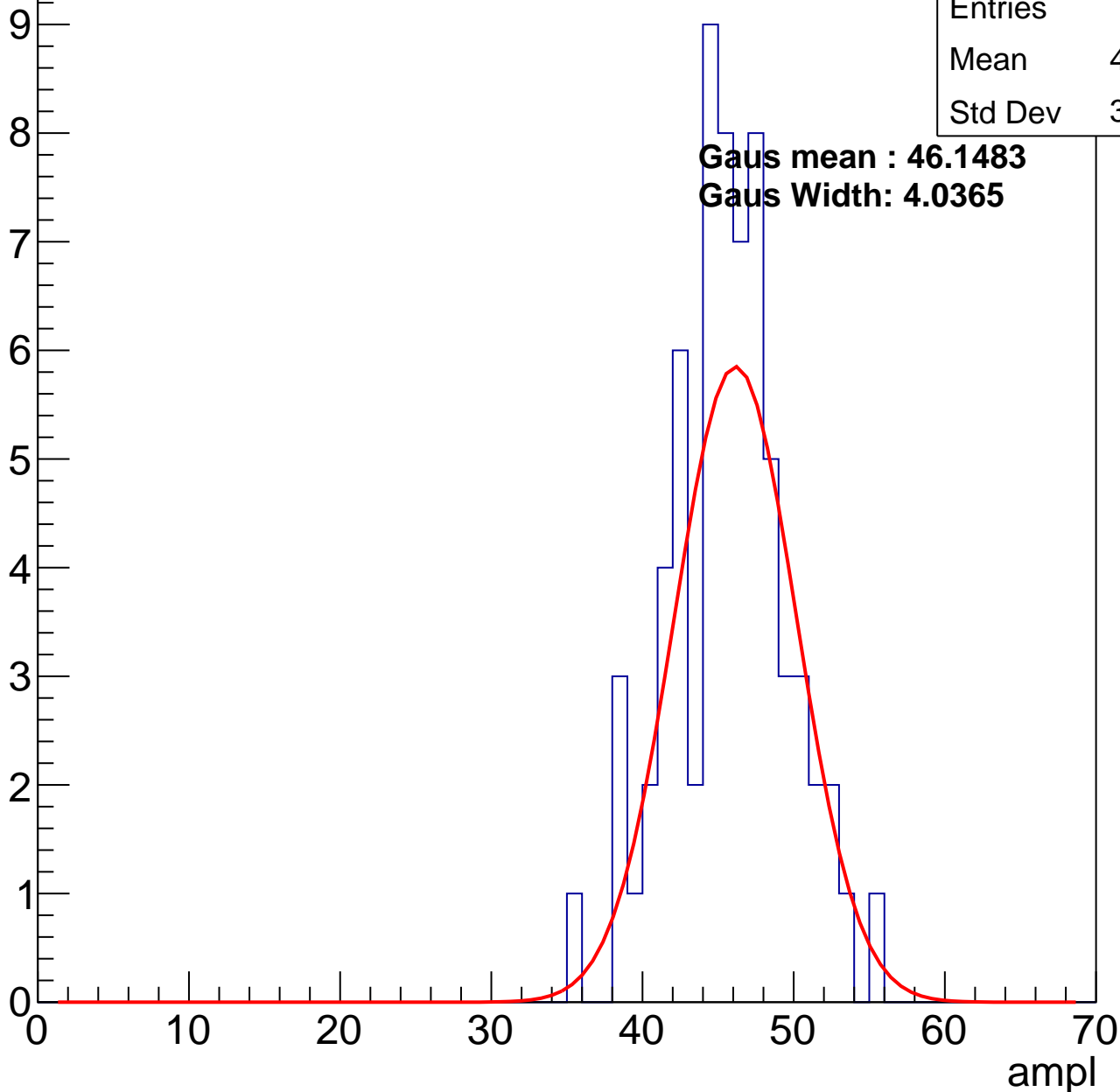
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	45.22
Std Dev	3.846

**Gaus mean : 46.1483**

**Gaus Width: 4.0365**

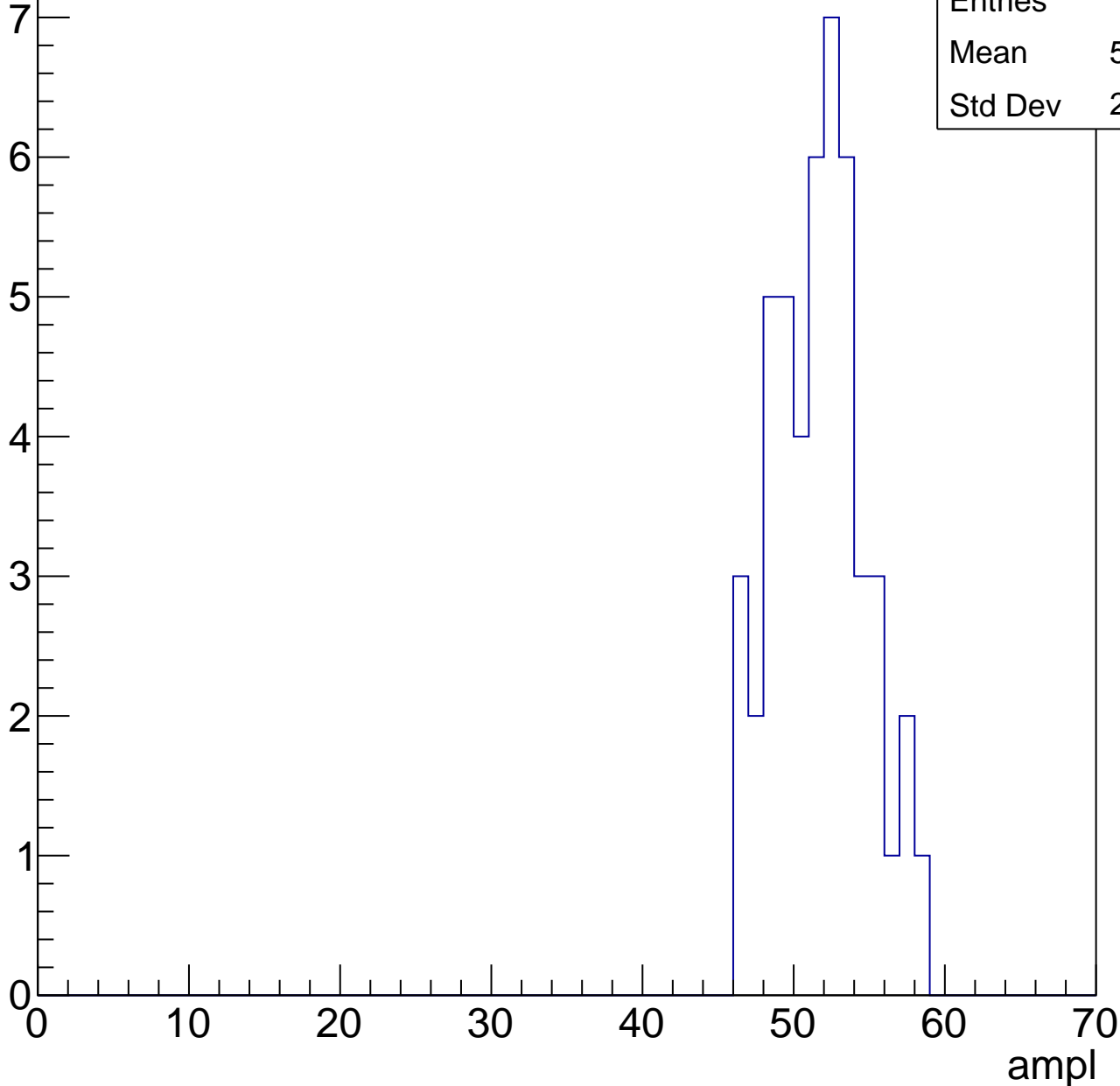


# B1L102S, U5-ch108, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	48
Mean	51.25
Std Dev	2.976

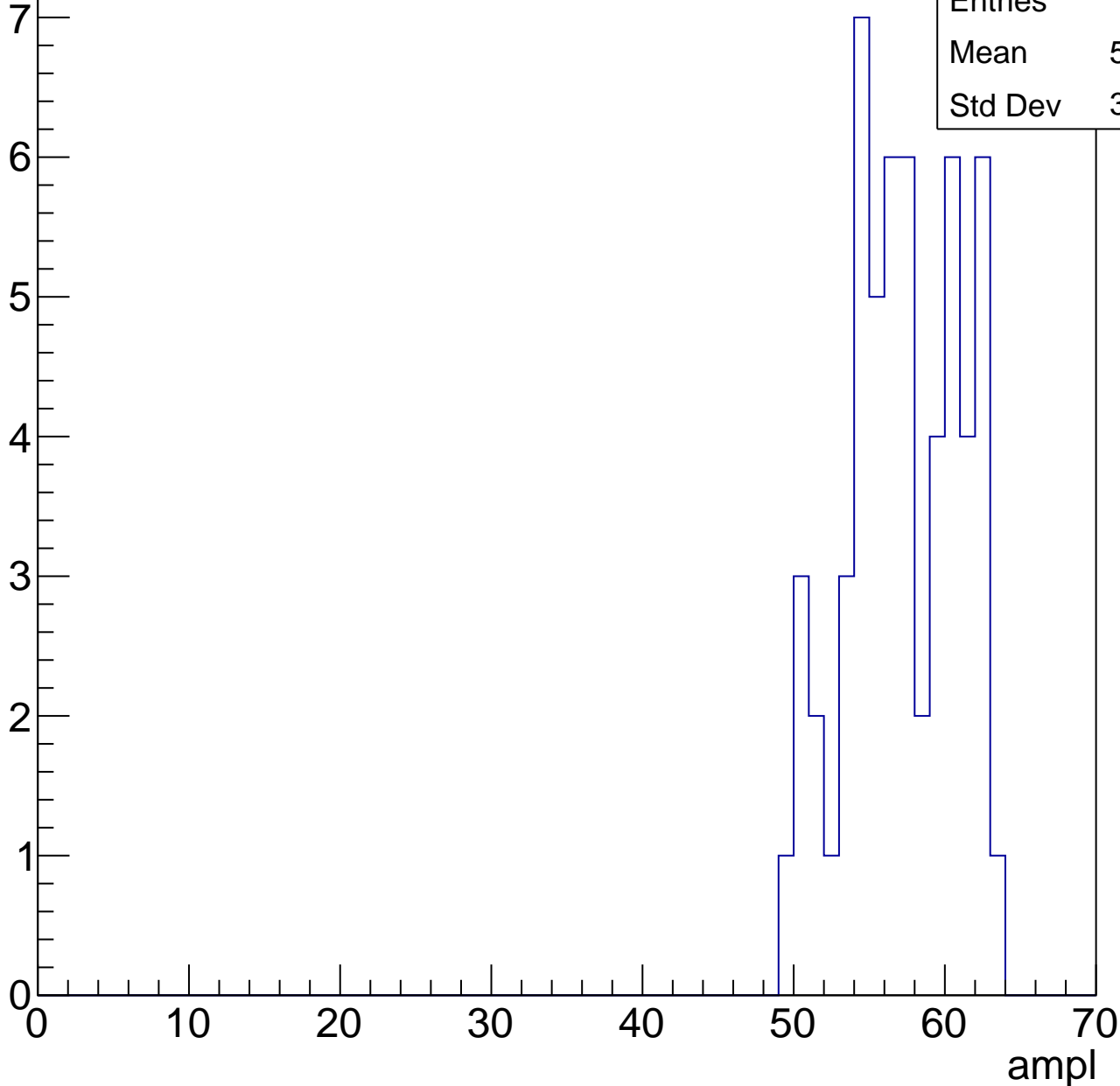


# B1L102S, U5-ch108, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	56.74
Std Dev	3.659

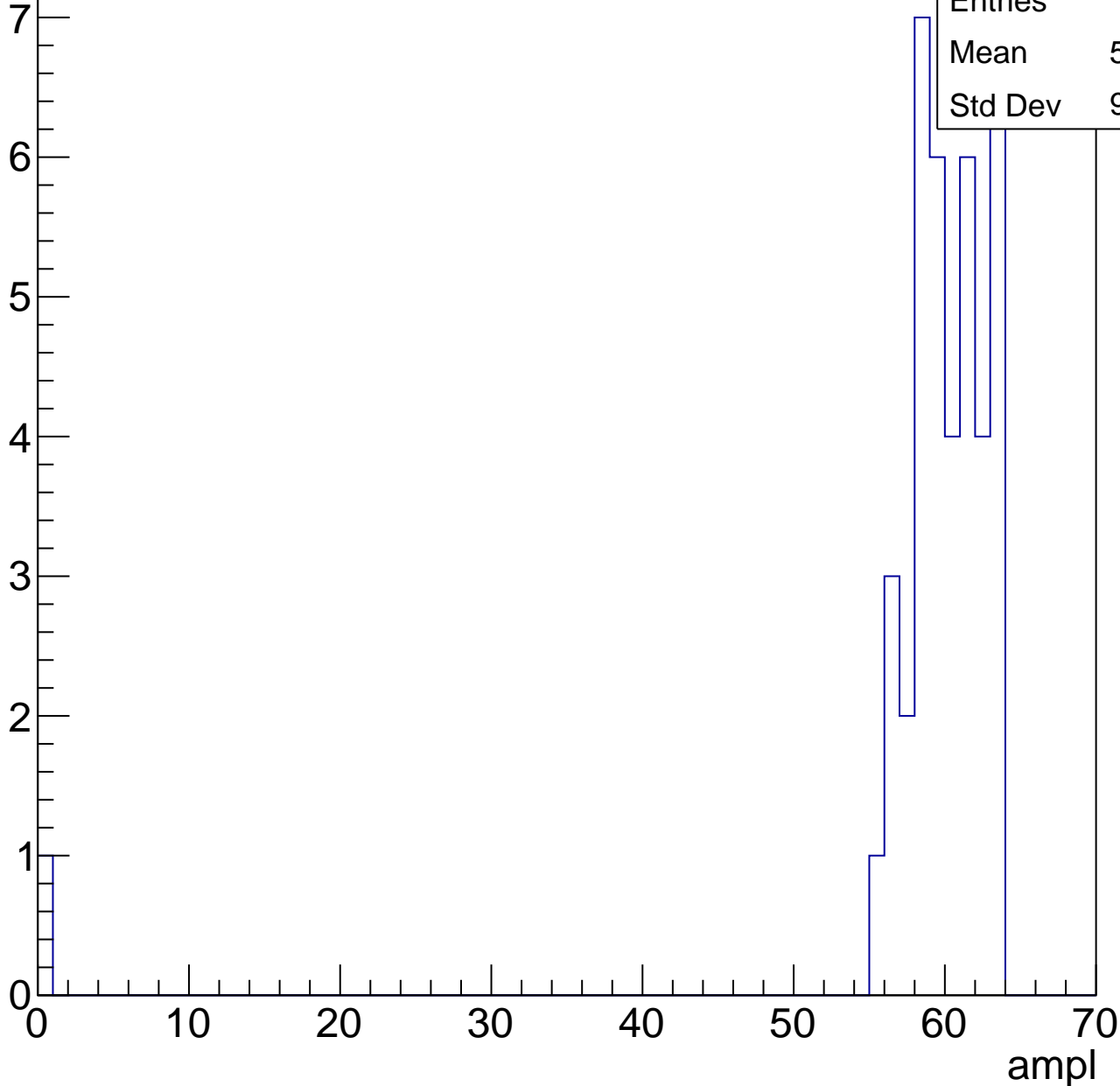


# B1L102S, U5-ch108, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	41
Mean	58.34
Std Dev	9.496



# B1L102S, U5-ch108, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U5-ch108, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U5-ch109, adc0

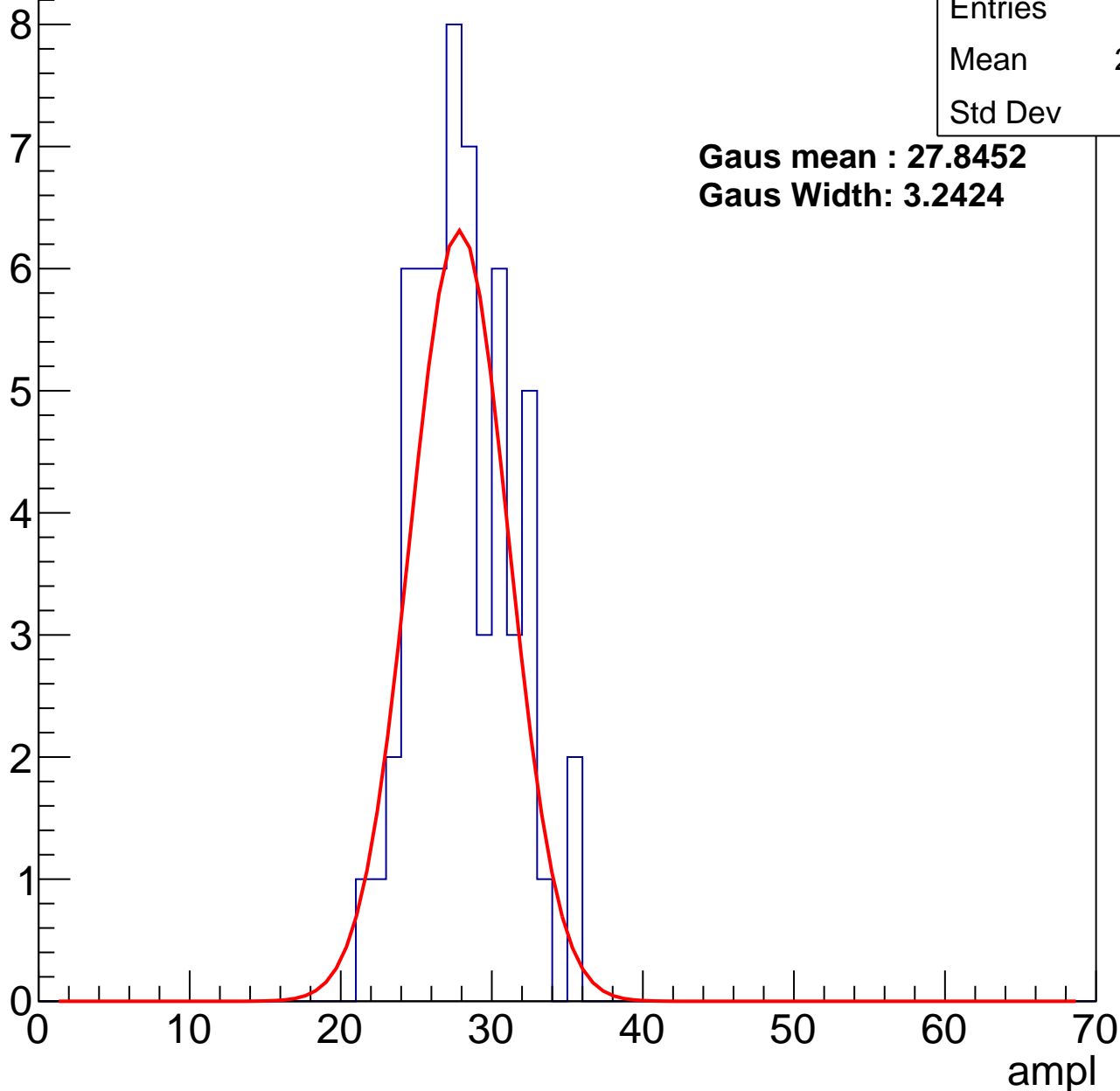
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	27.61
Std Dev	3.15

**Gaus mean : 27.8452**

**Gaus Width: 3.2424**



# B1L102S, U5-ch109, adc1

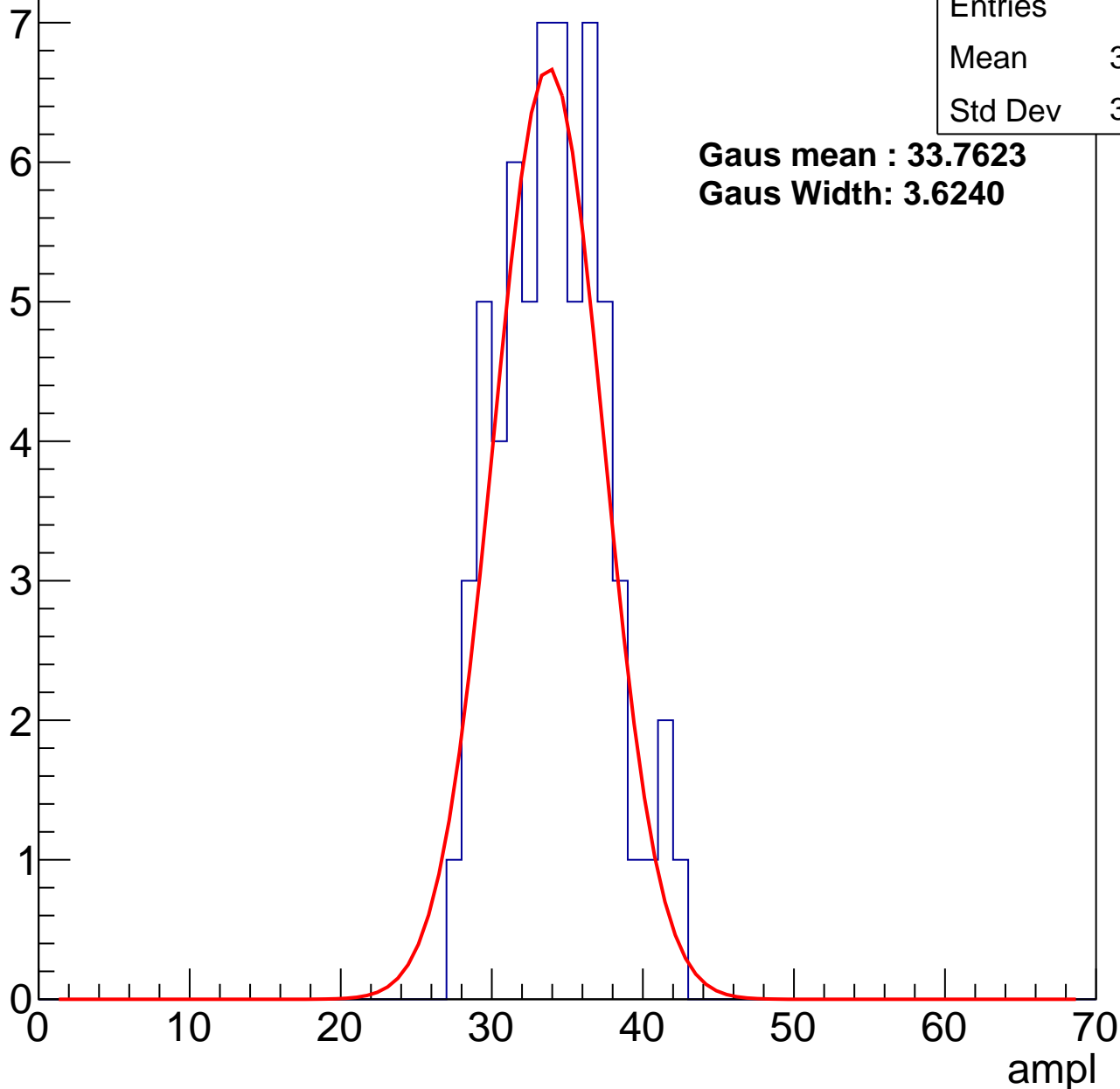
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	33.65
Std Dev	3.492

**Gaus mean : 33.7623**

**Gaus Width: 3.6240**



# B1L102S, U5-ch109, adc2

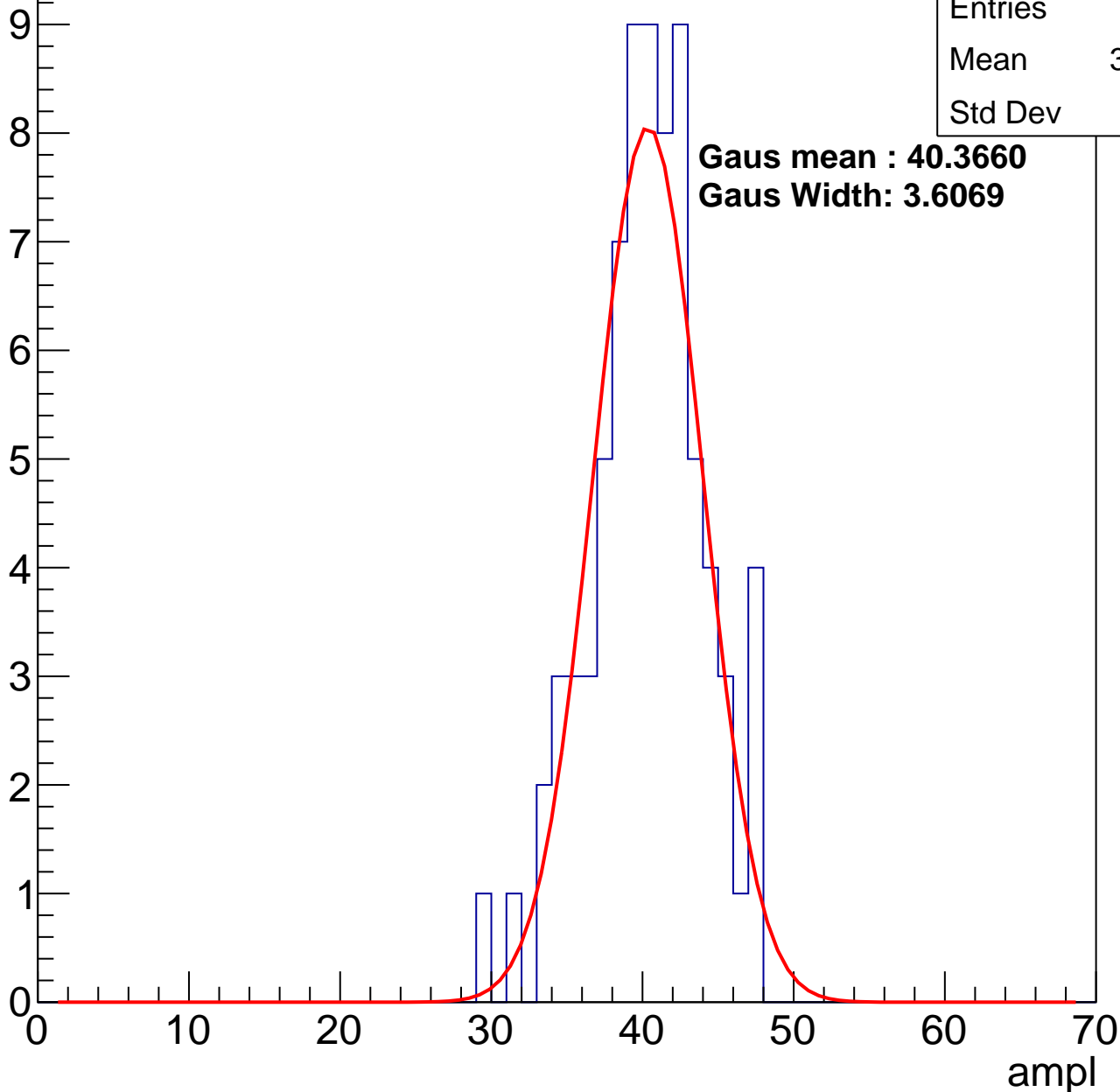
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	39.86
Std Dev	3.73

**Gaus mean : 40.3660**

**Gaus Width: 3.6069**

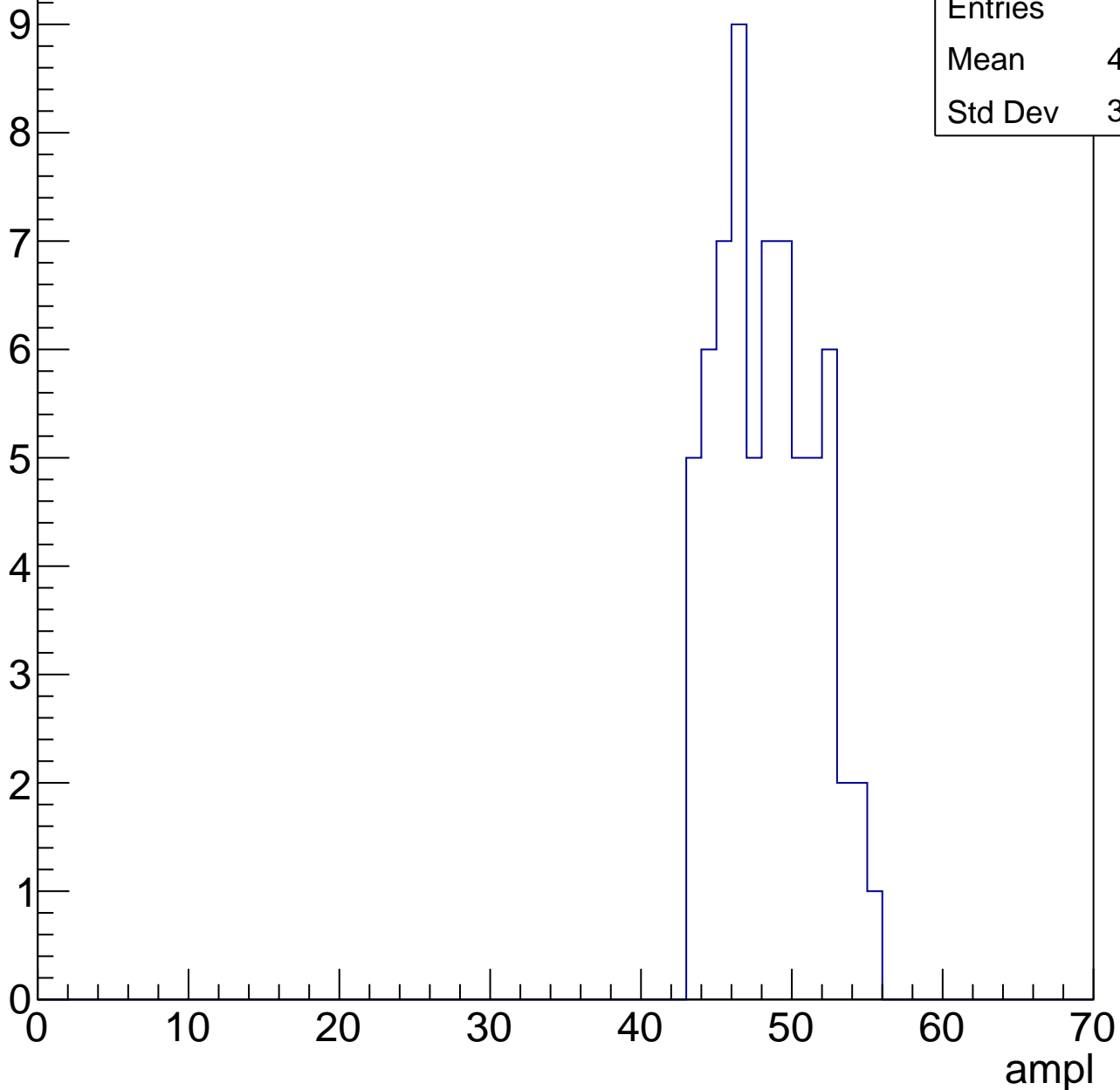


# B1L102S, U5-ch109, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	47.88
Std Dev	3.146

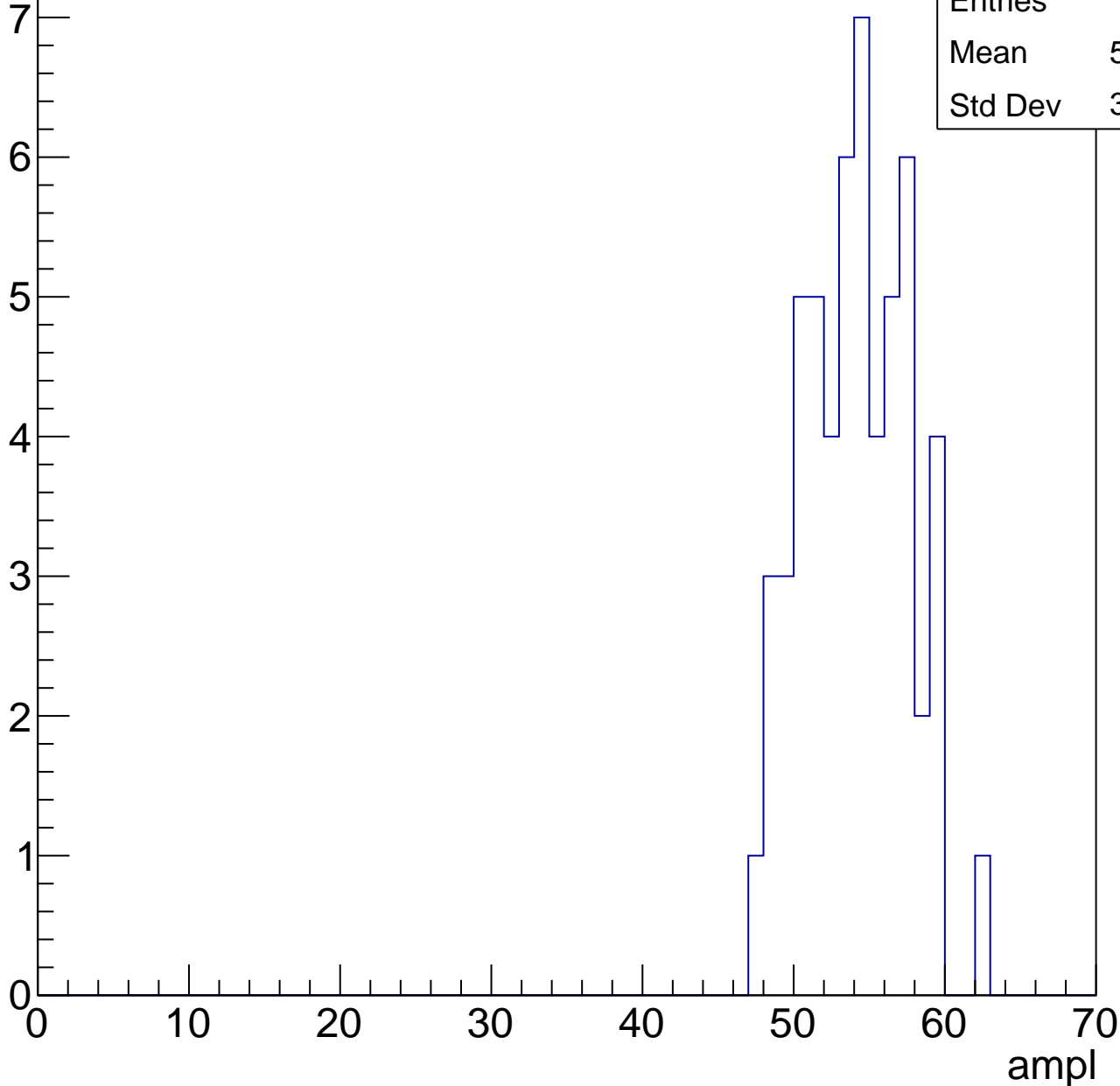


# B1L102S, U5-ch109, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	53.62
Std Dev	3.394

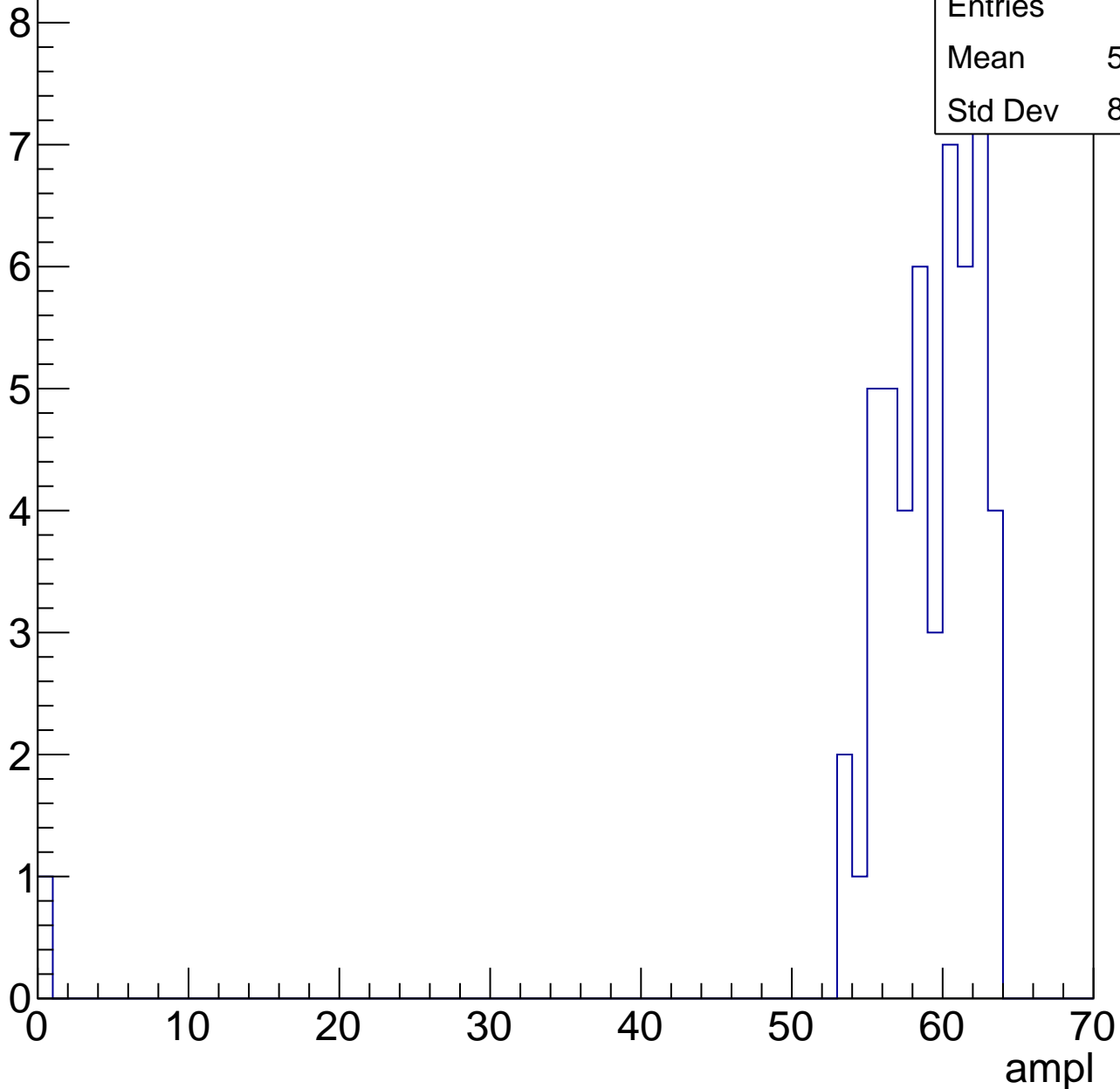


# B1L102S, U5-ch109, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	57.73
Std Dev	8.558

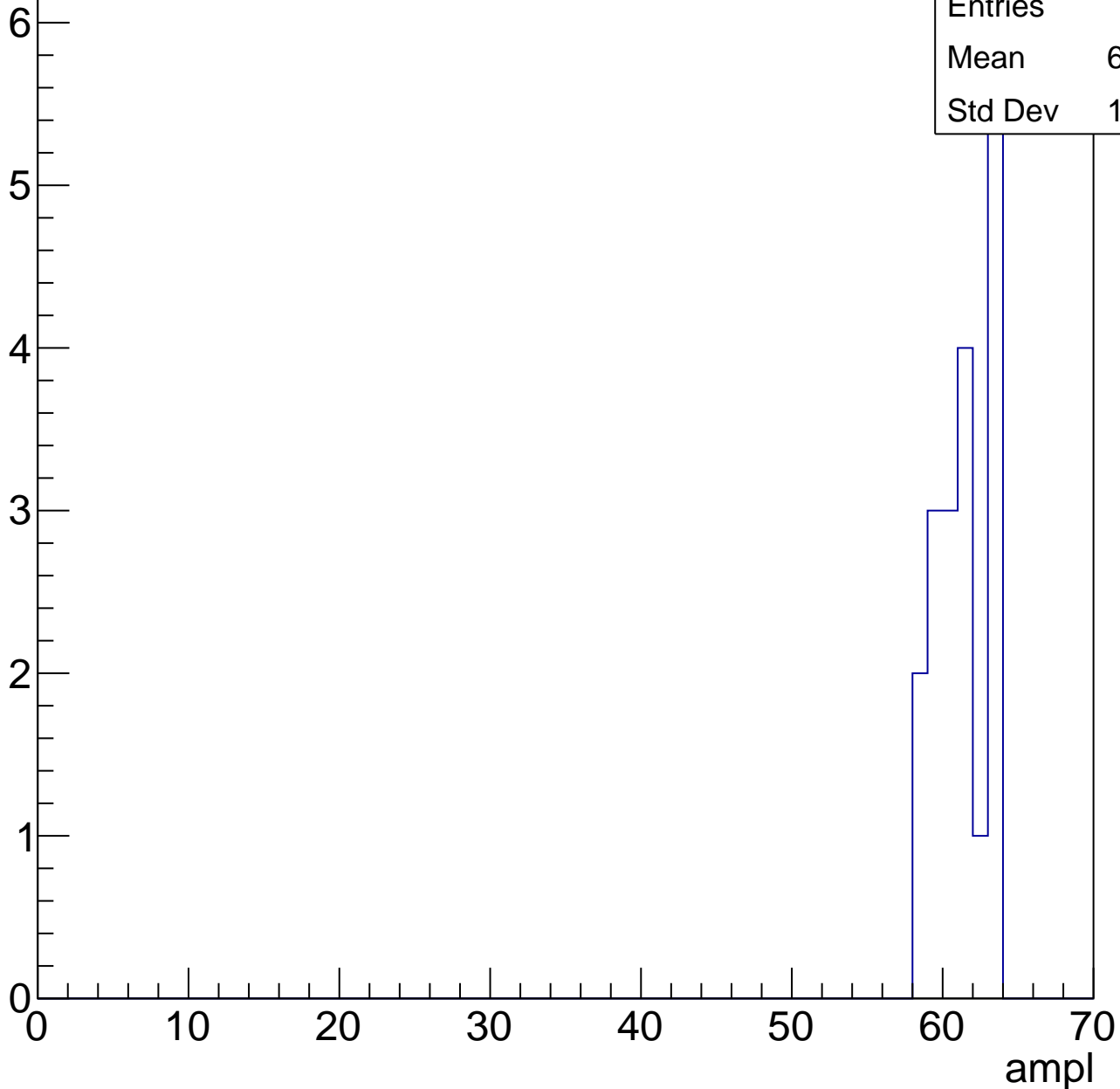


# B1L102S, U5-ch109, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	19
Mean	60.89
Std Dev	1.744





# B1L102S, U5-ch109, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U5-ch110, adc0

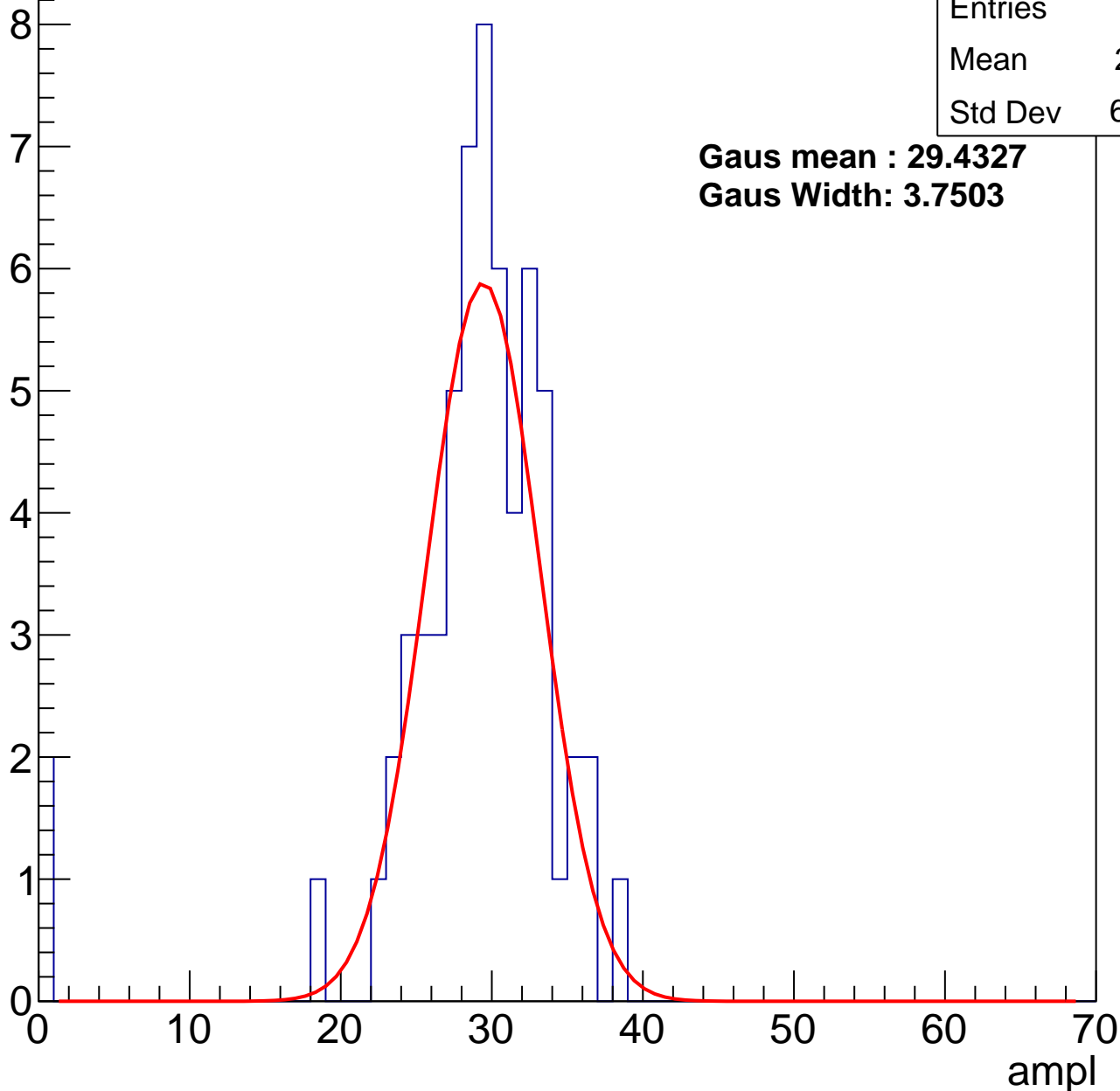
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	28.21
Std Dev	6.343

**Gaus mean : 29.4327**

**Gaus Width: 3.7503**



# B1L102S, U5-ch110, adc1

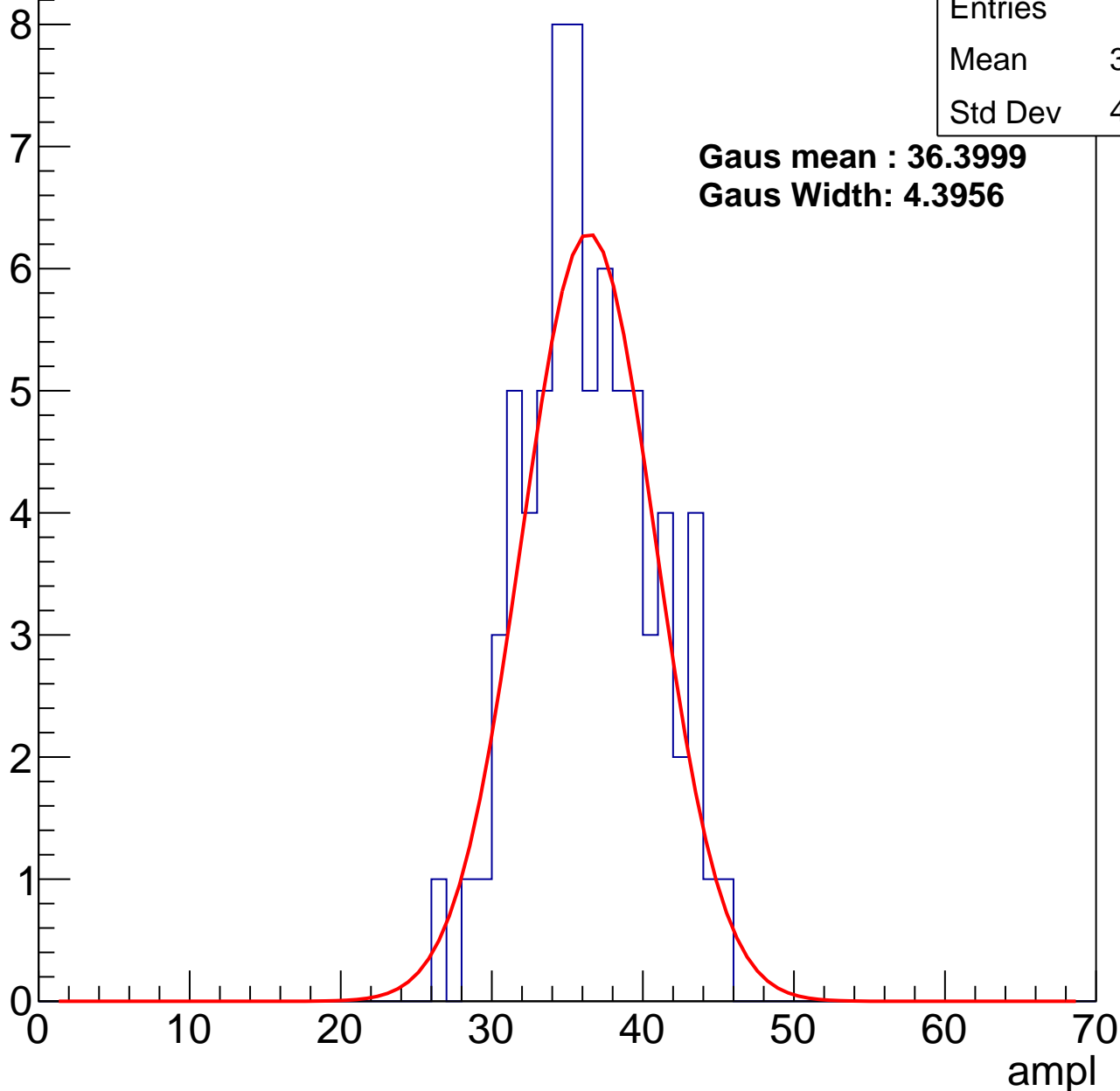
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	35.96
Std Dev	4.128

**Gaus mean : 36.3999**

**Gaus Width: 4.3956**



# B1L102S, U5-ch110, adc2

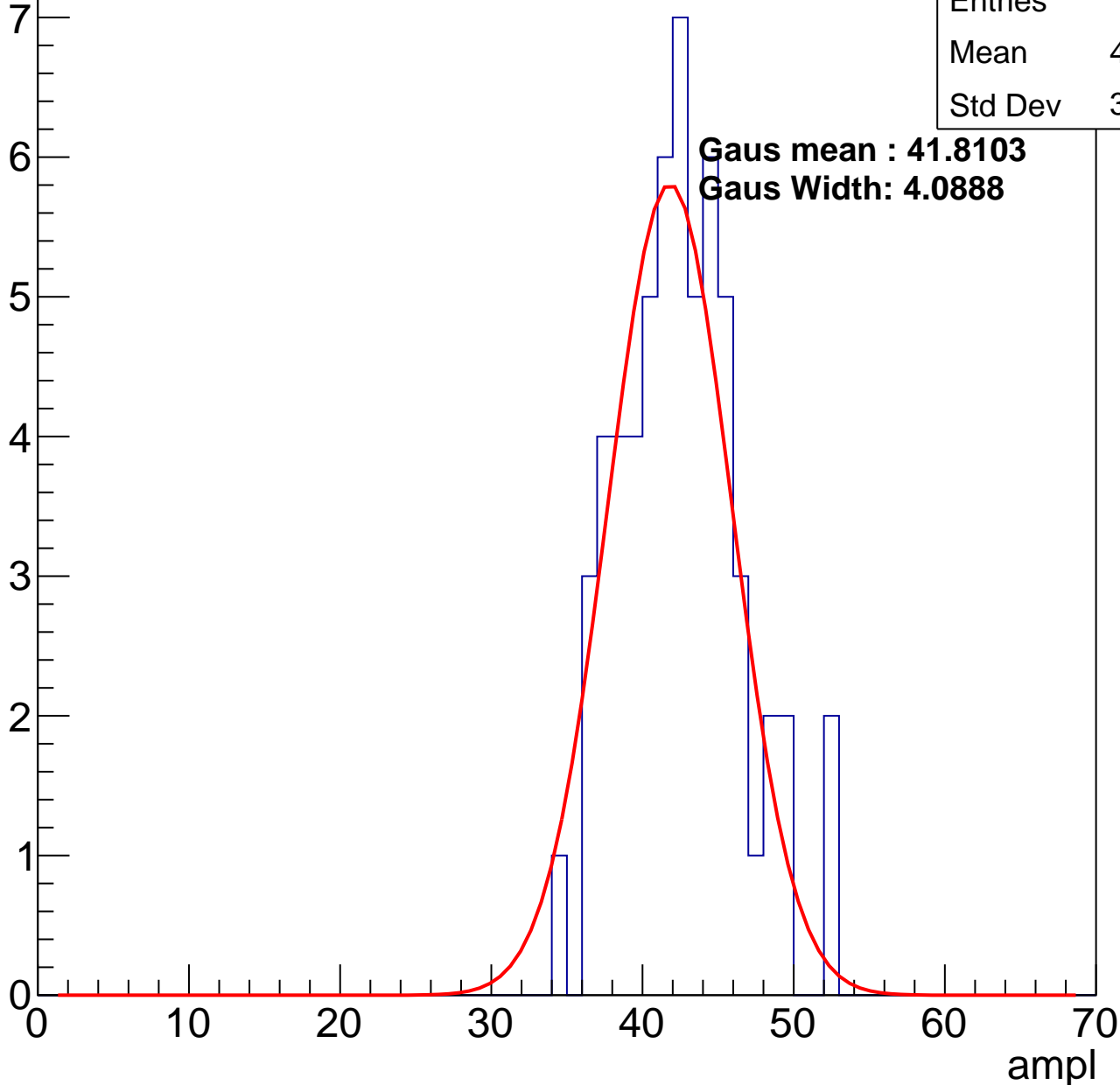
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	42.08
Std Dev	3.904

**Gaus mean : 41.8103**

**Gaus Width: 4.0888**

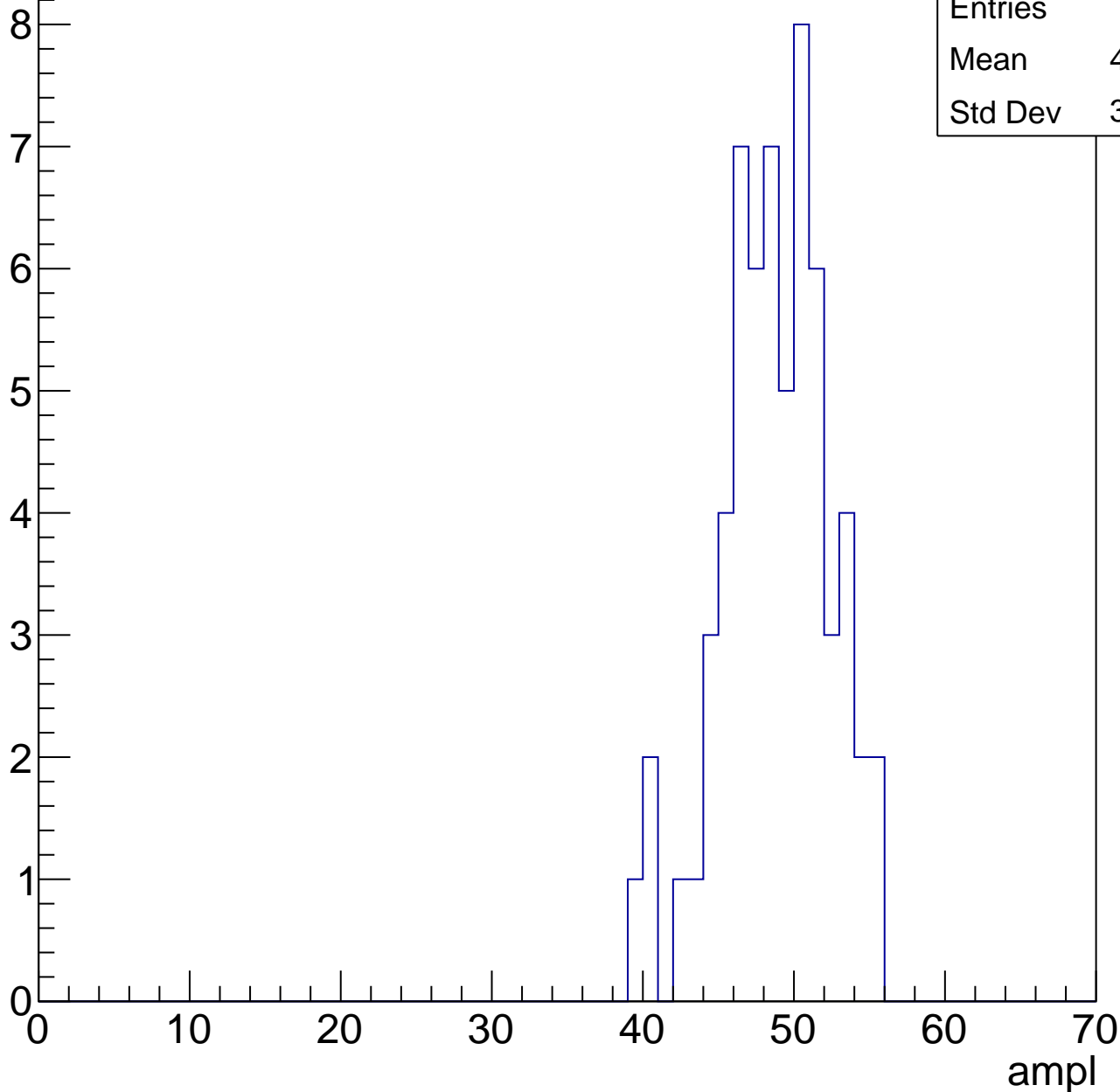


# B1L102S, U5-ch110, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	48.27
Std Dev	3.575

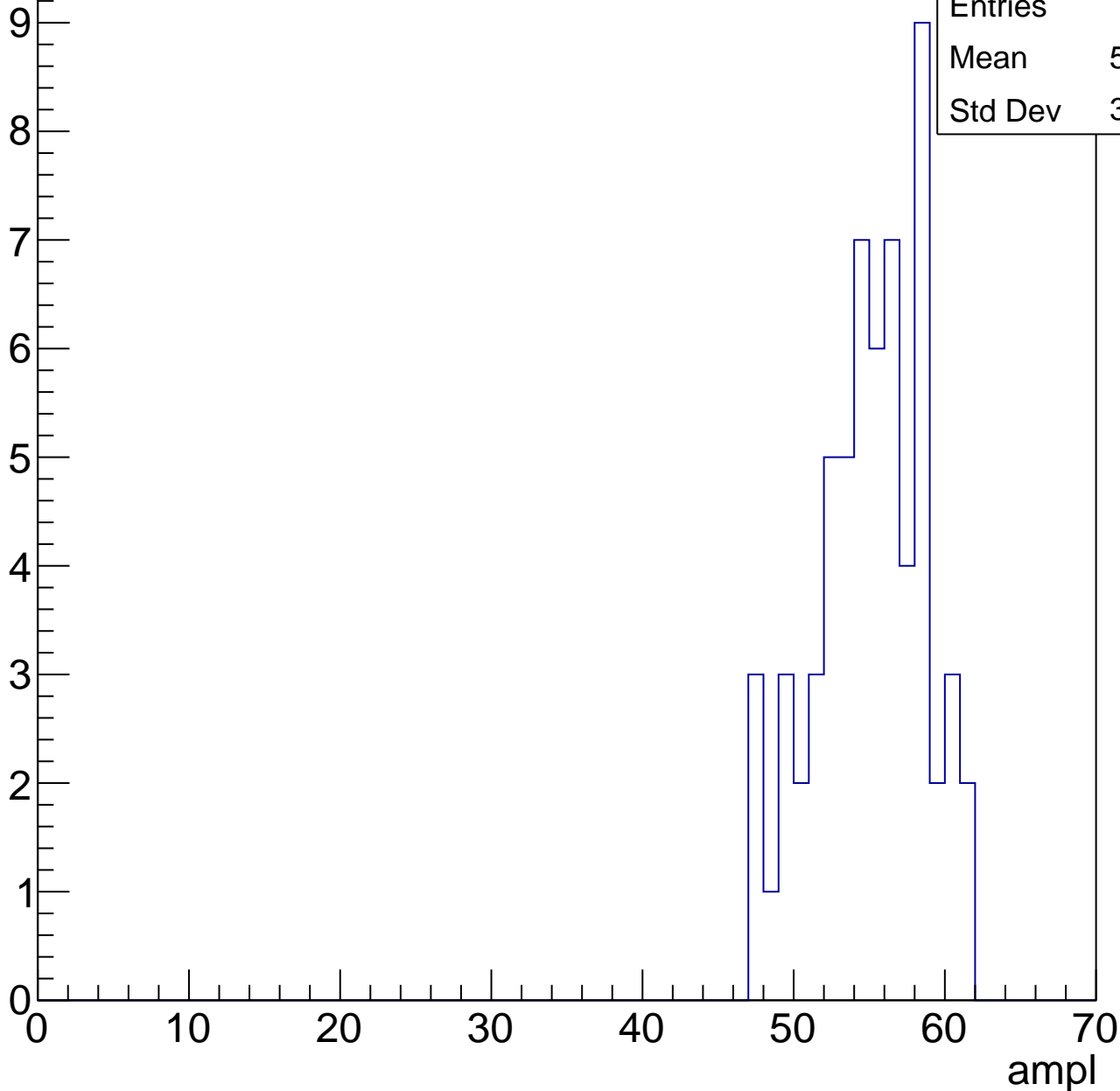


# B1L102S, U5-ch110, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	54.58
Std Dev	3.572

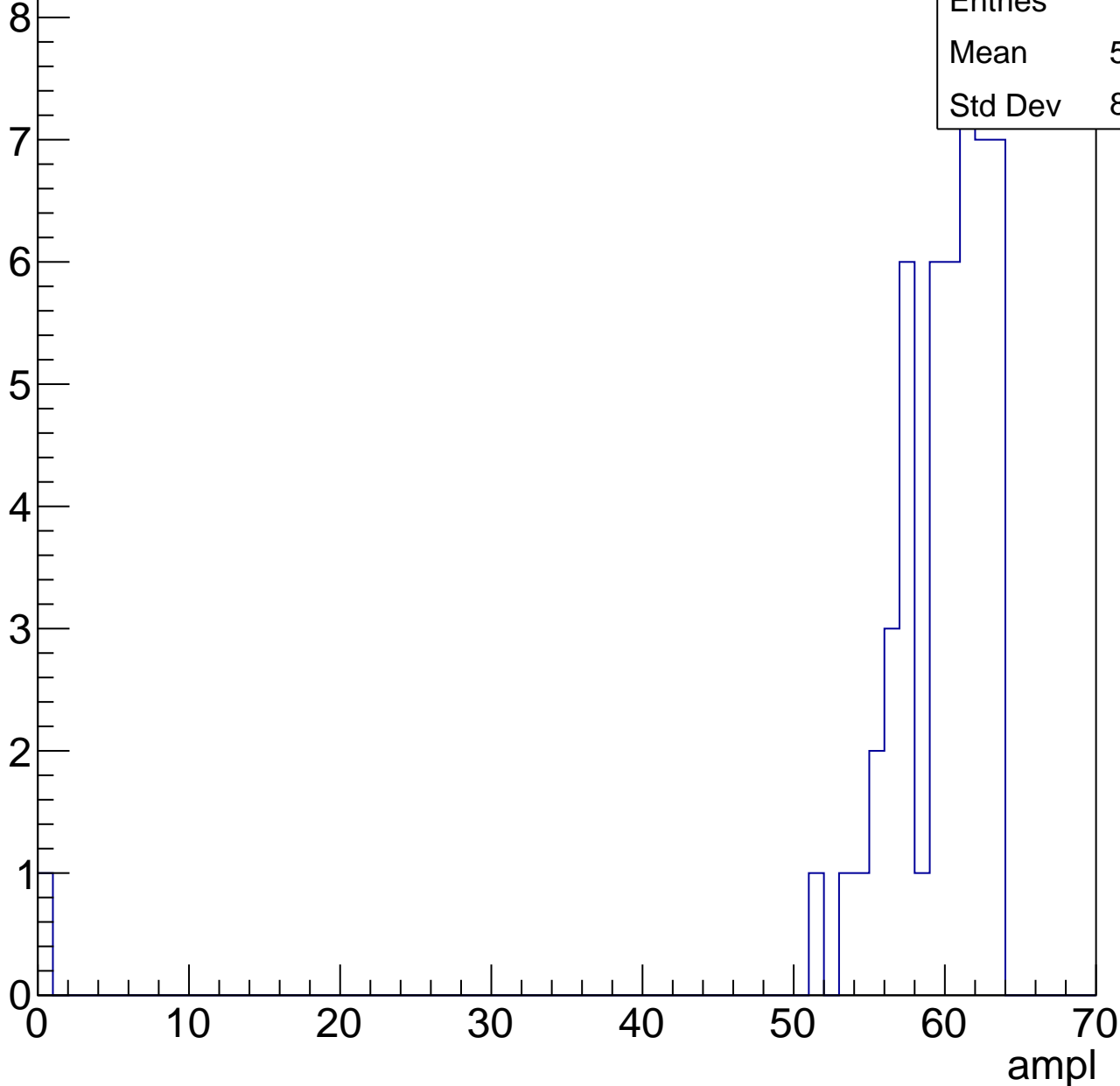


# B1L102S, U5-ch110, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	58.26
Std Dev	8.804



# B1L102S, U5-ch110, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries	9
Mean	61.44
Std Dev	1.571



# B1L102S, U5-ch110, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U5-ch111, adc0

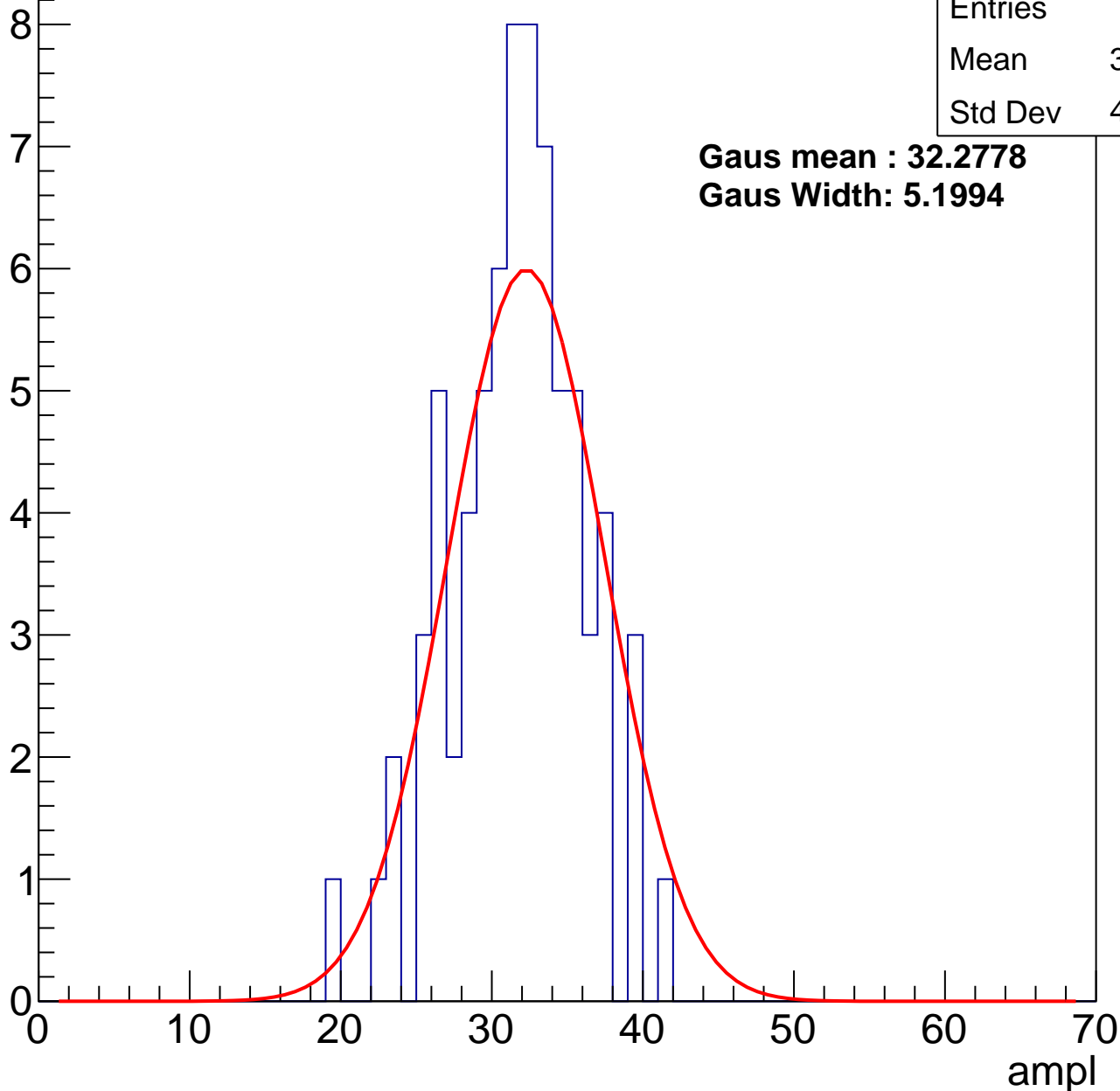
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	31.19
Std Dev	4.299

**Gaus mean : 32.2778**

**Gaus Width: 5.1994**



# B1L102S, U5-ch111, adc1

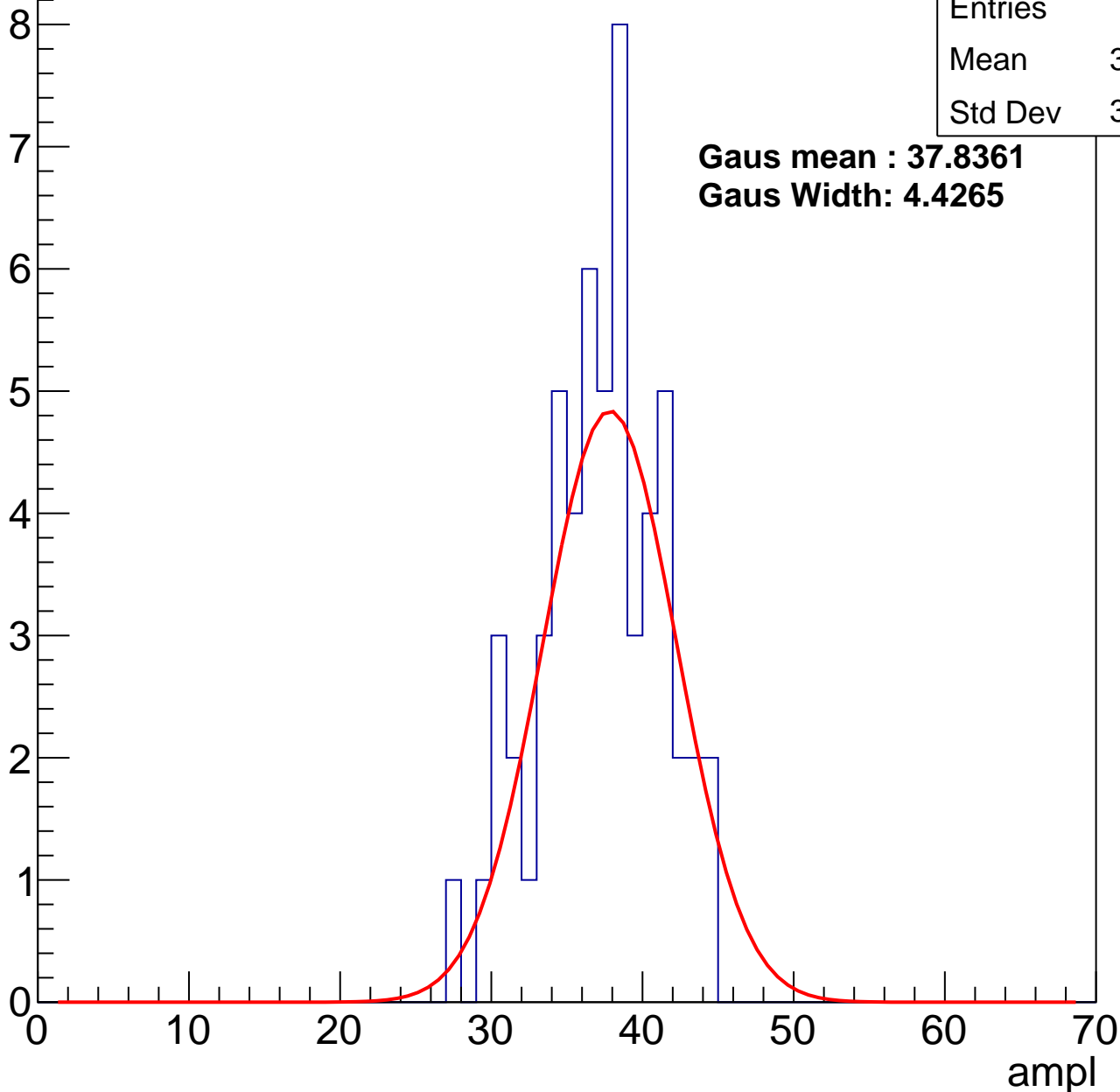
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	36.74
Std Dev	3.918

**Gaus mean : 37.8361**

**Gaus Width: 4.4265**



# B1L102S, U5-ch111, adc2

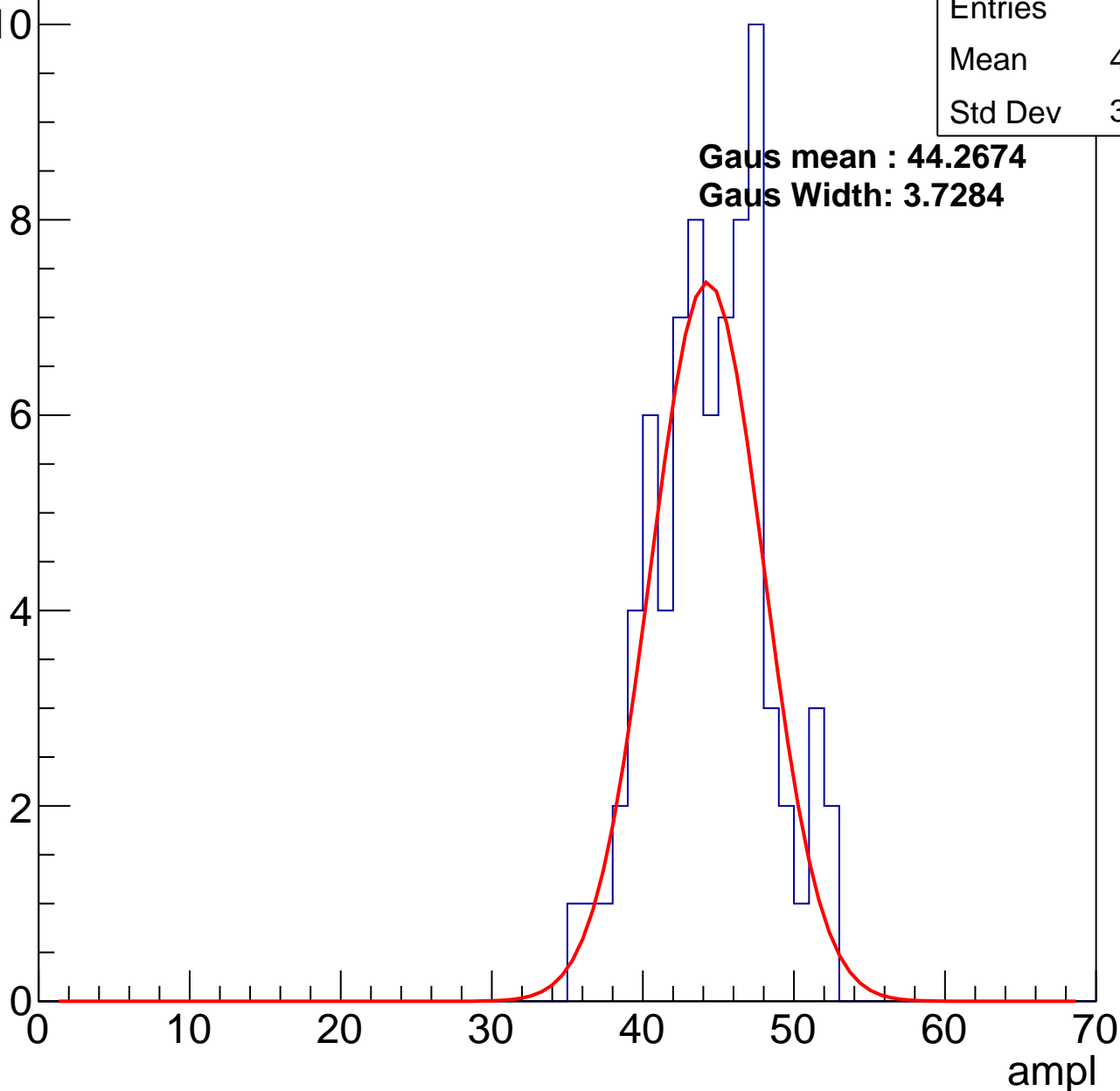
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	44.05
Std Dev	3.755

**Gaus mean : 44.2674**

**Gaus Width: 3.7284**

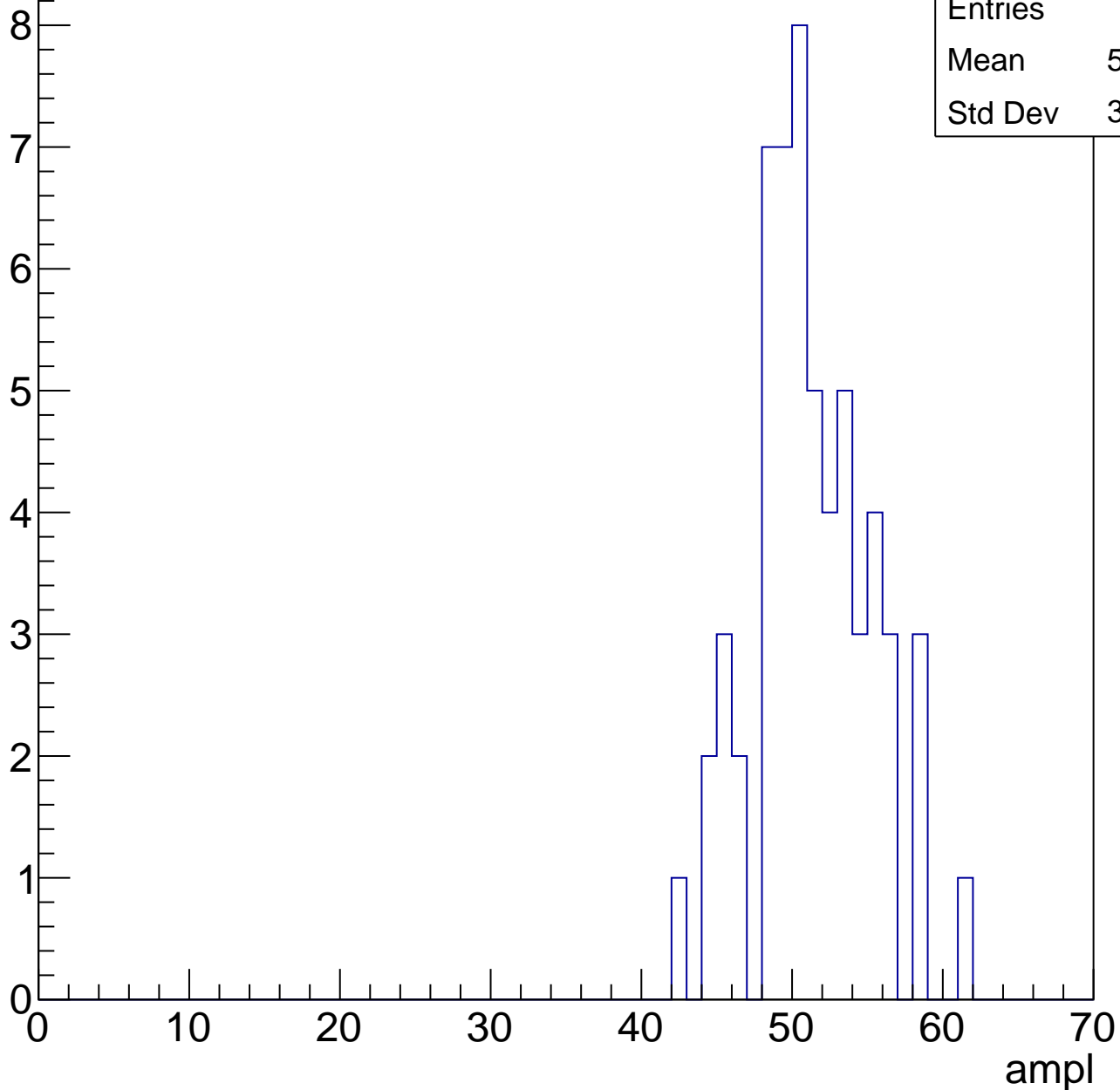


# B1L102S, U5-ch111, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

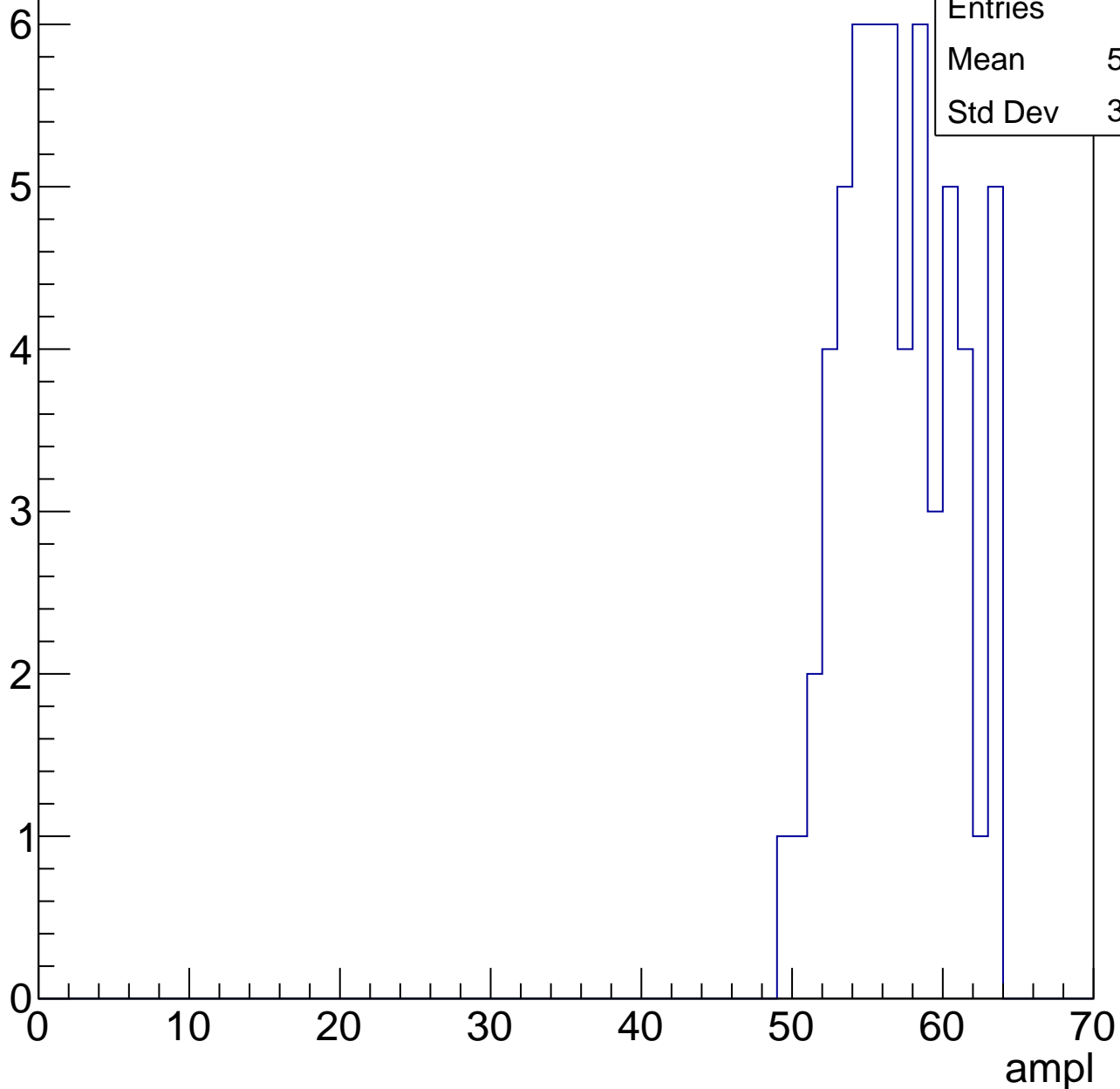
Entries	58
Mean	50.84
Std Dev	3.877



# B1L102S, U5-ch111, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



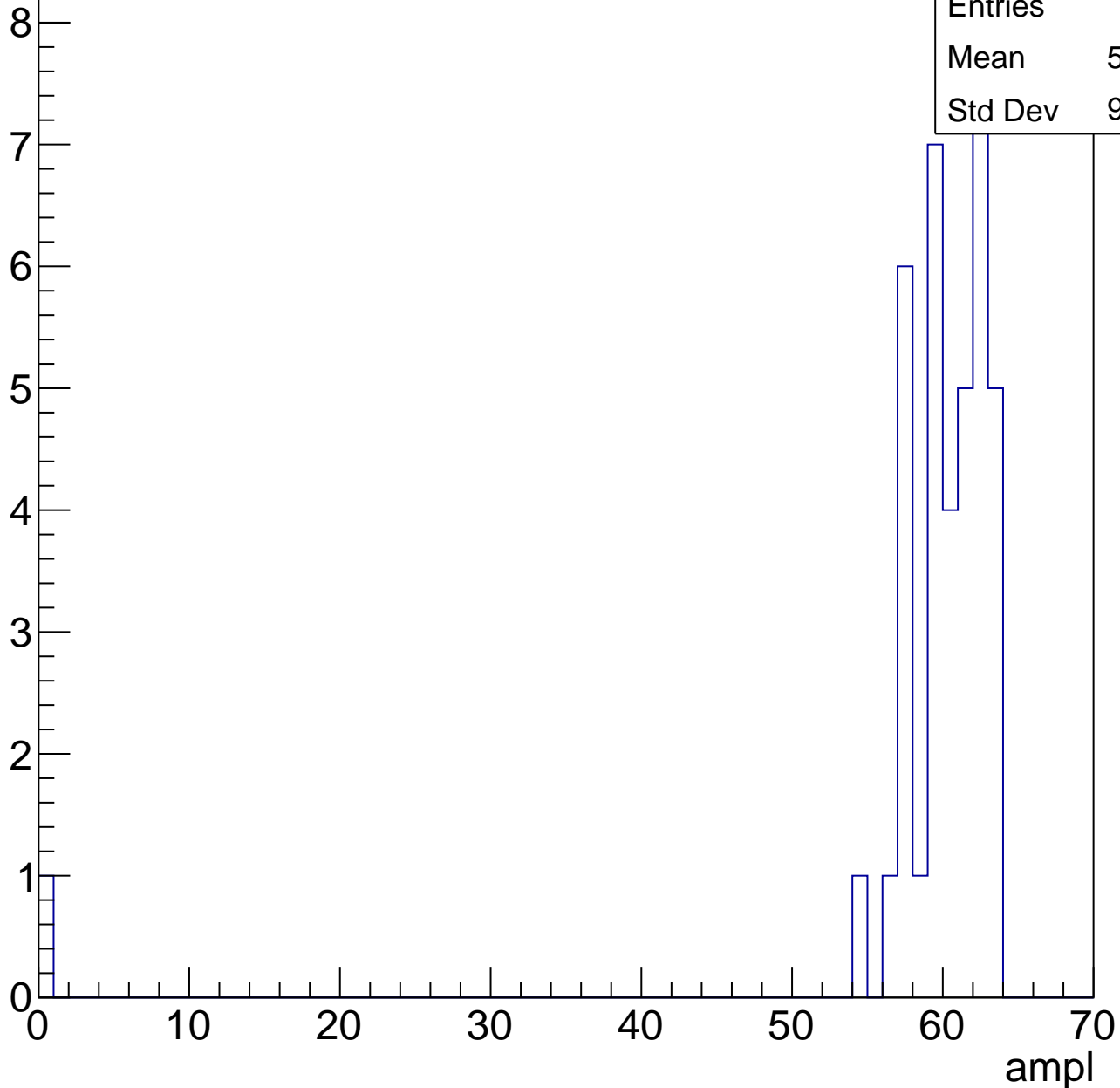
Entries	59
Mean	56.58
Std Dev	3.614

# B1L102S, U5-ch111, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	39
Mean	58.44
Std Dev	9.745



# B1L102S, U5-ch111, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U5-ch111, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U5-ch112, adc0

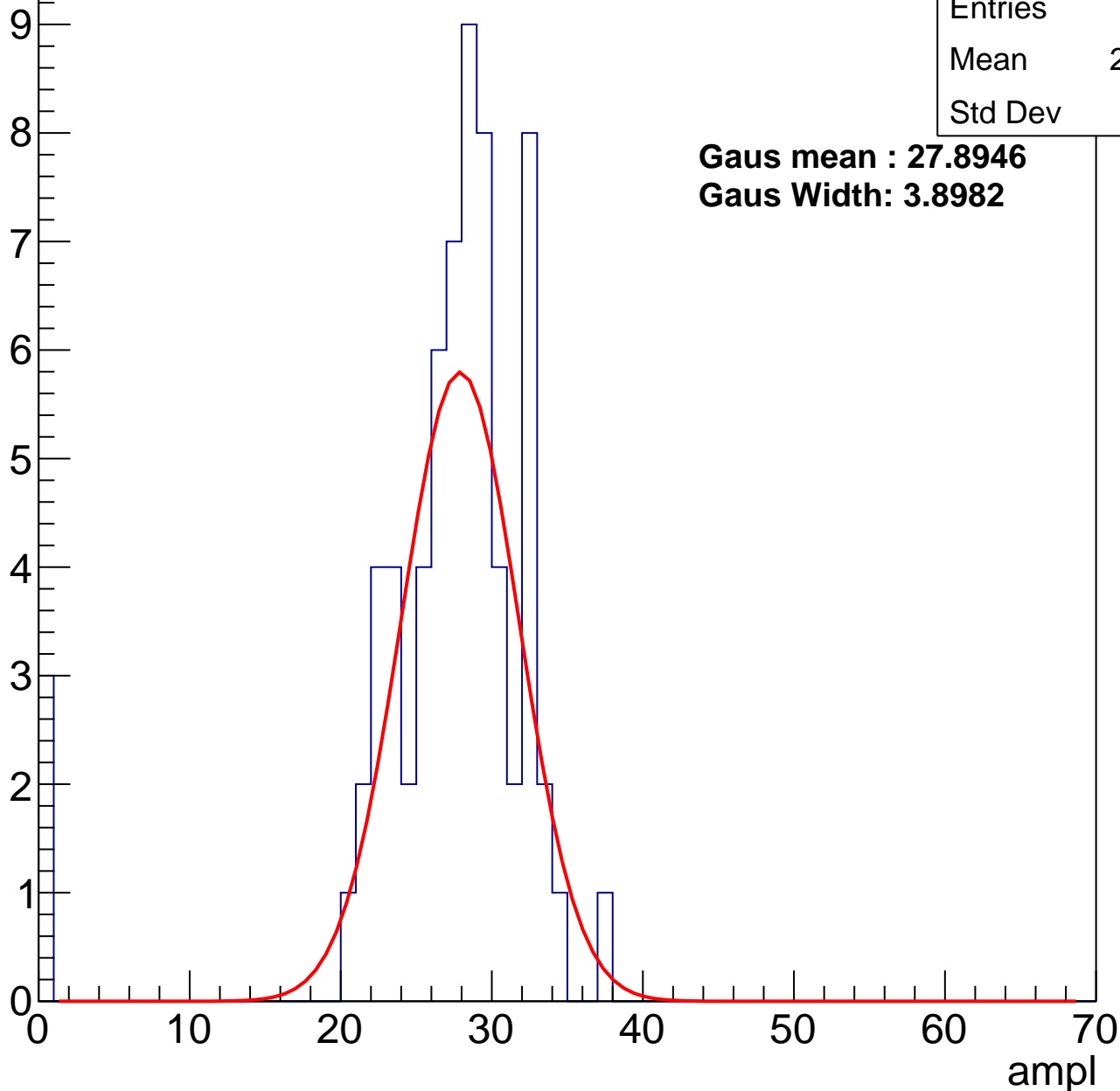
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	26.38
Std Dev	6.66

**Gaus mean : 27.8946**

**Gaus Width: 3.8982**



# B1L102S, U5-ch112, adc1

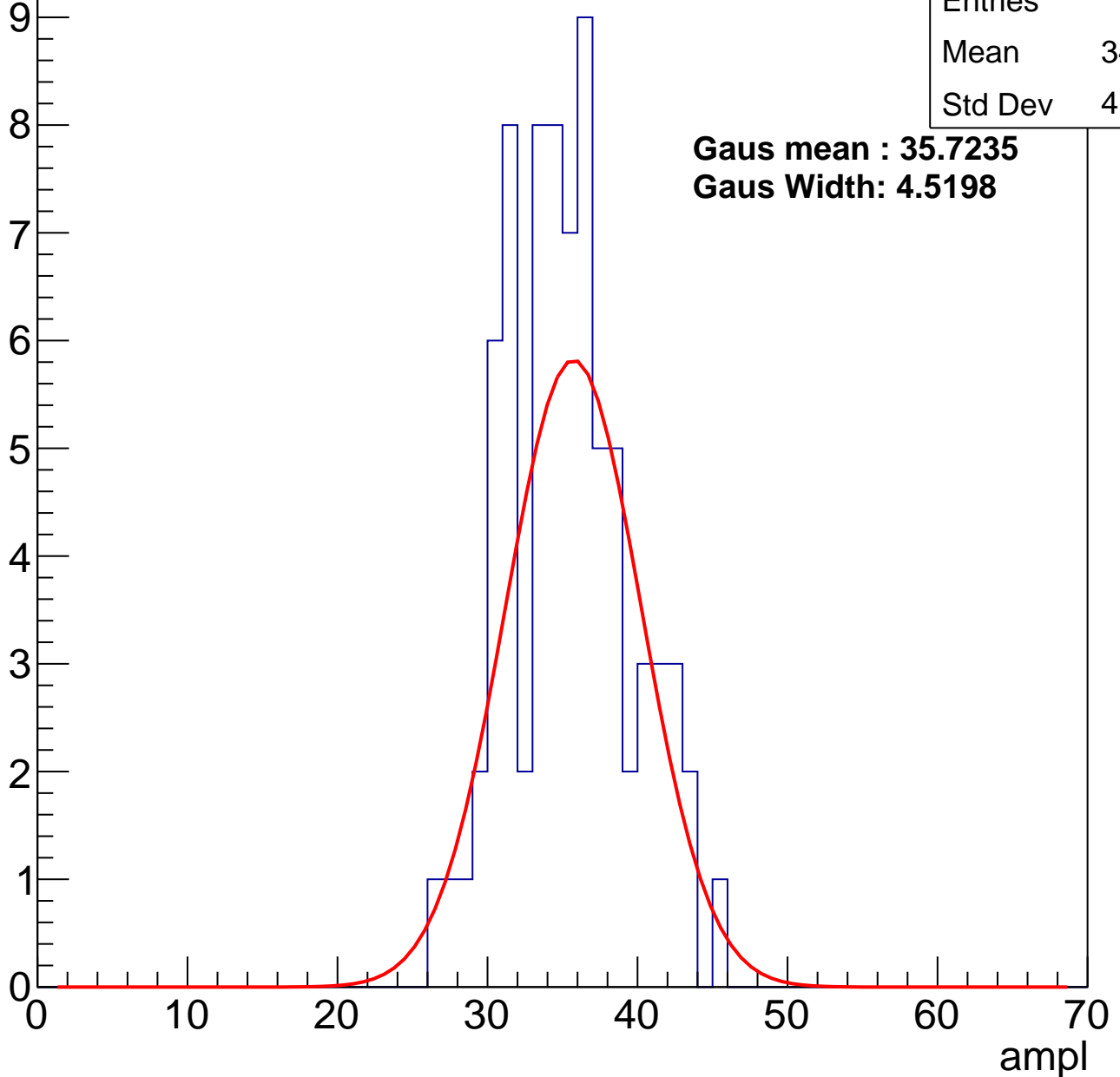
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	34.92
Std Dev	4.054

**Gaus mean : 35.7235**

**Gaus Width: 4.5198**



# B1L102S, U5-ch112, adc2

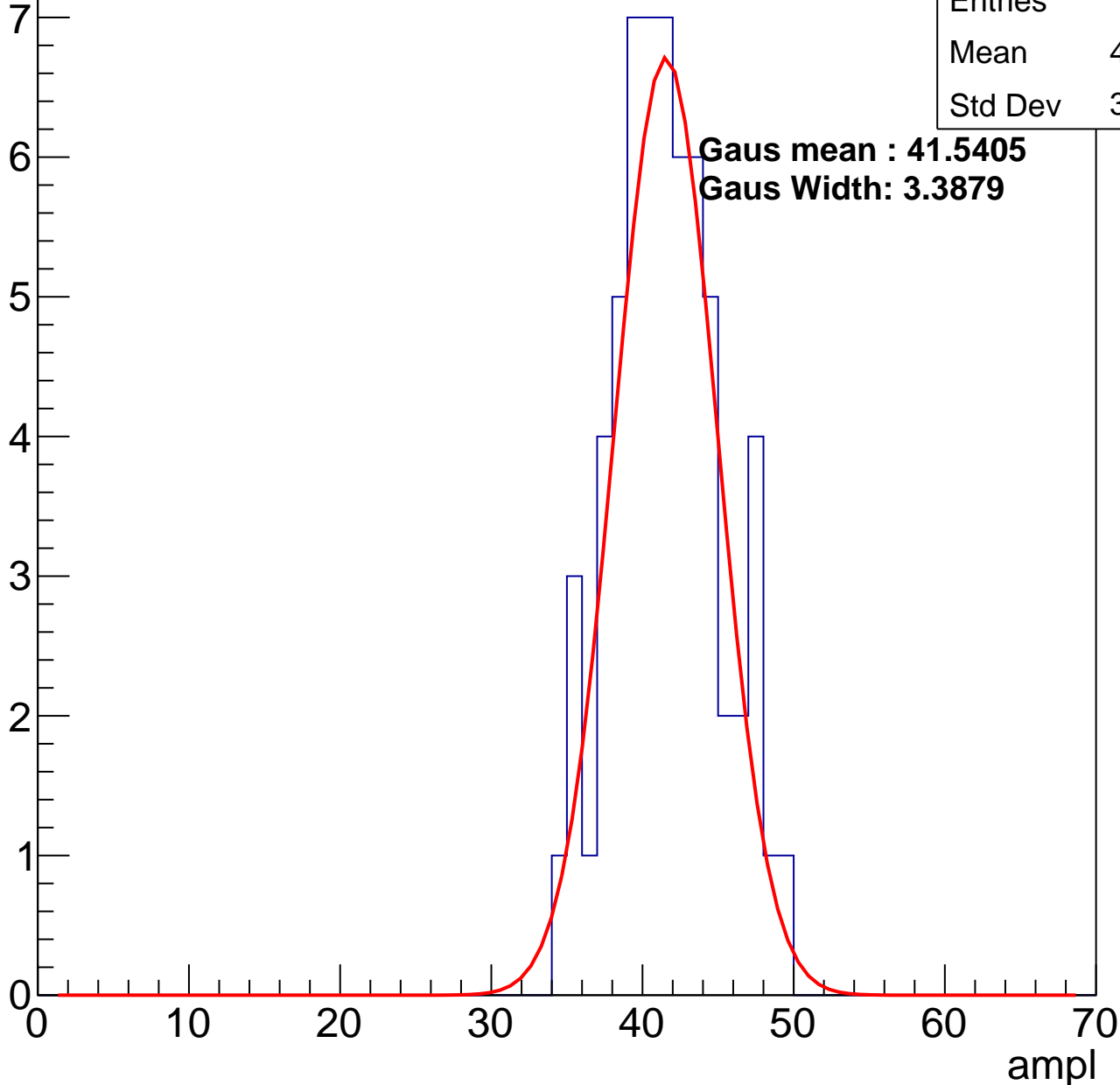
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	41.13
Std Dev	3.452

**Gaus mean : 41.5405**

**Gaus Width: 3.3879**

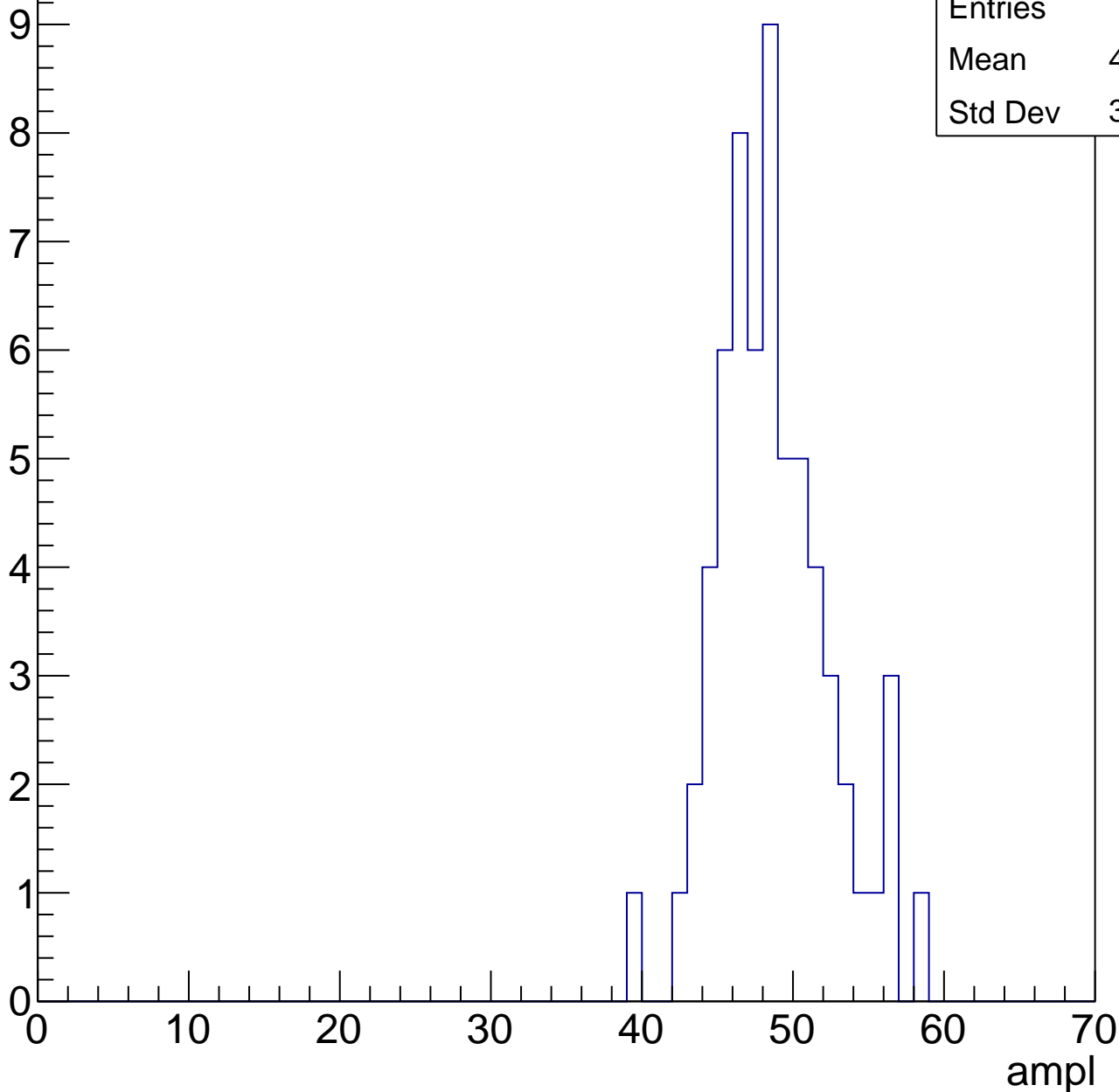


# B1L102S, U5-ch112, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	48.24
Std Dev	3.714

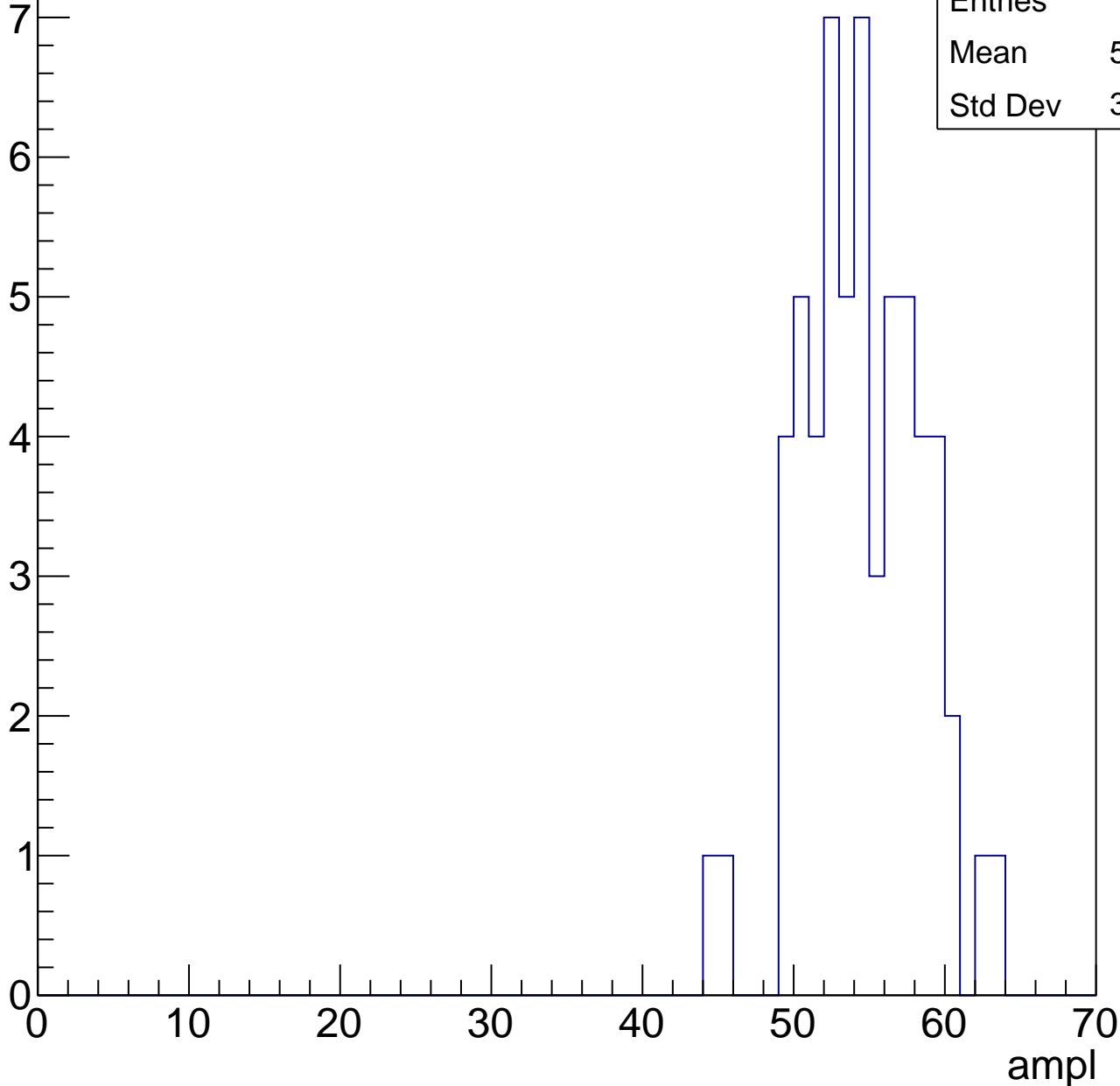


# B1L102S, U5-ch112, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	54.05
Std Dev	3.859

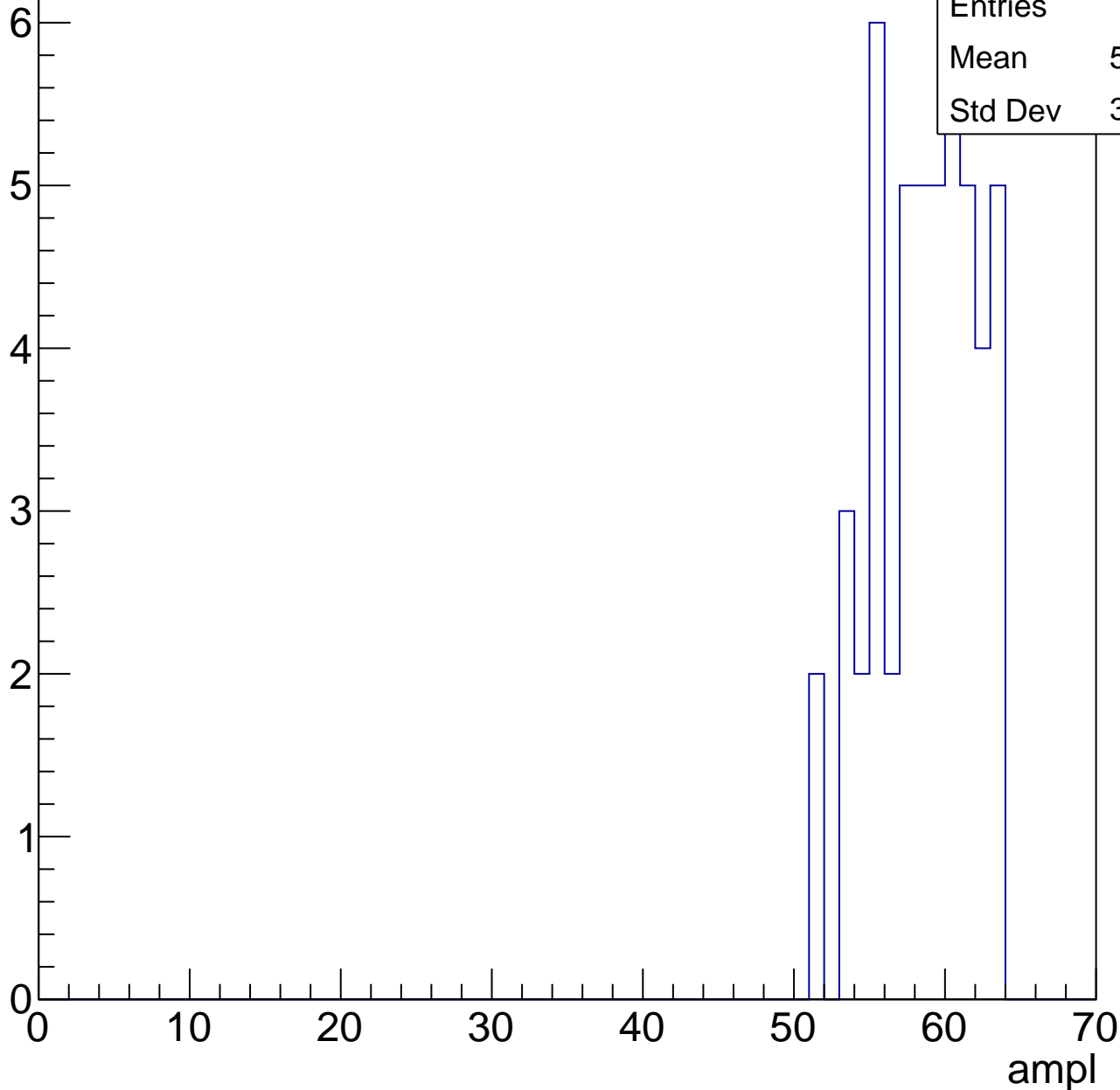


# B1L102S, U5-ch112, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	58.18
Std Dev	3.266

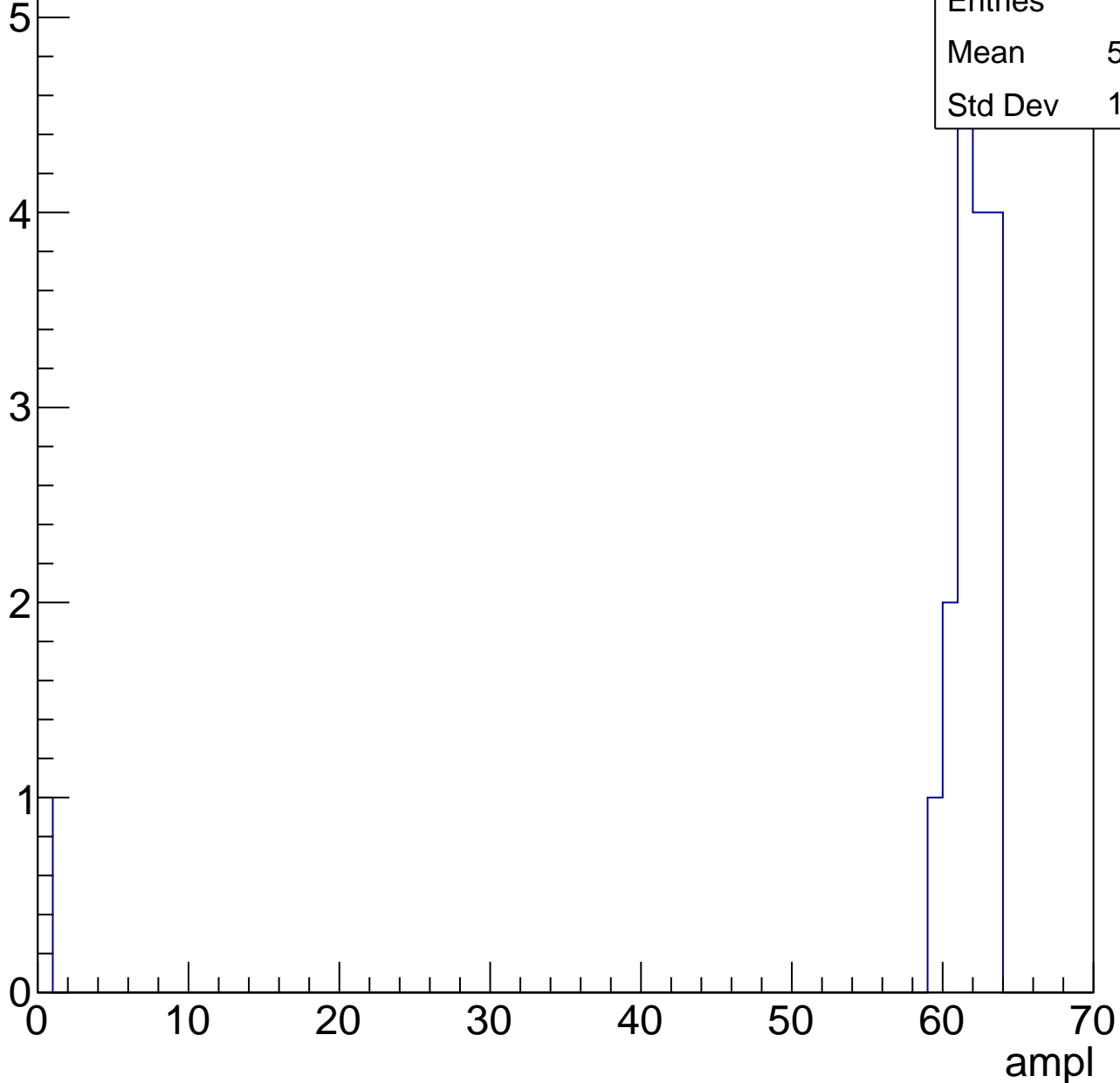


# B1L102S, U5-ch112, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	17
Mean	57.88
Std Dev	14.52

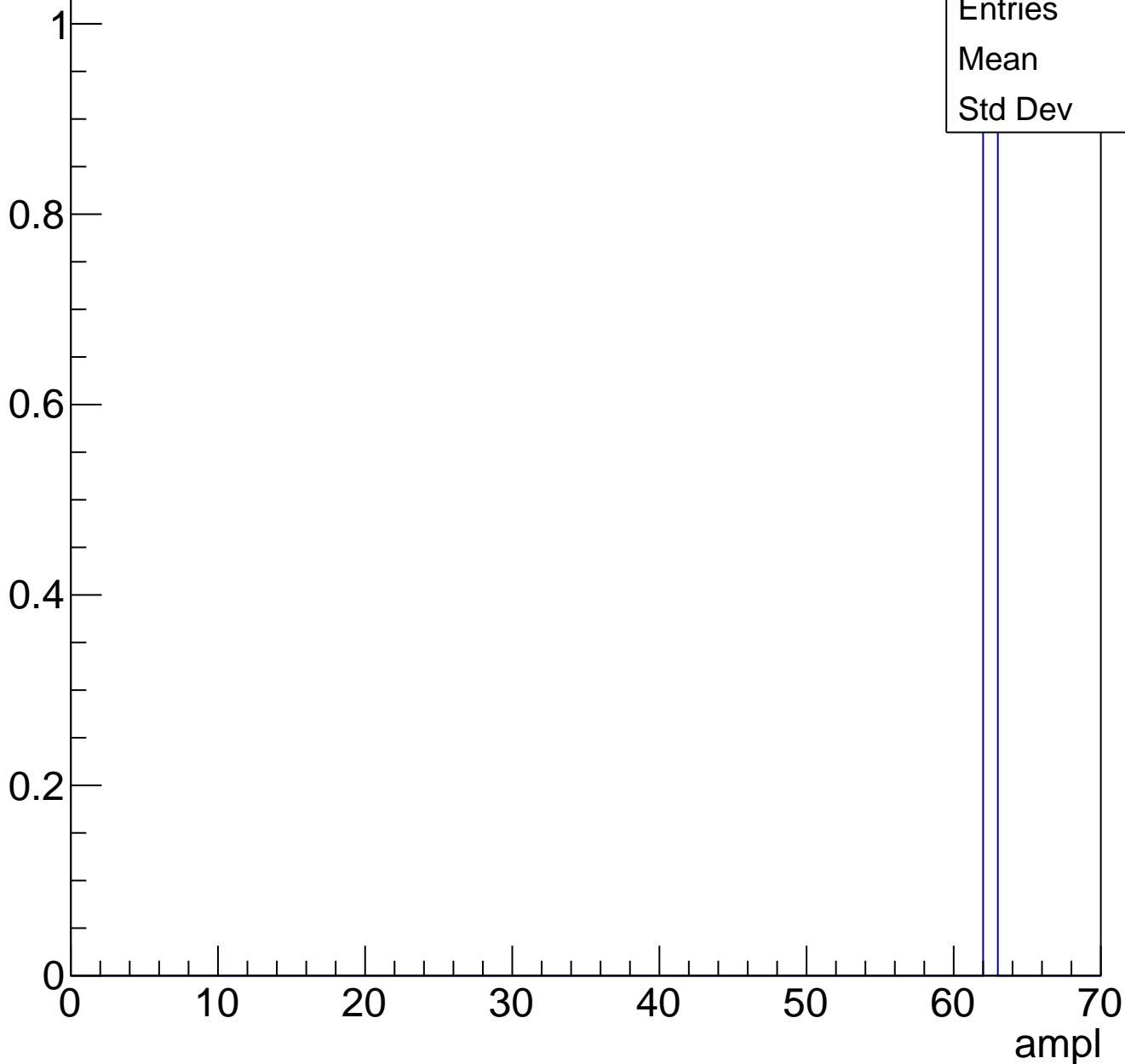




# B1L102S, U5-ch112, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U5-ch113, adc0

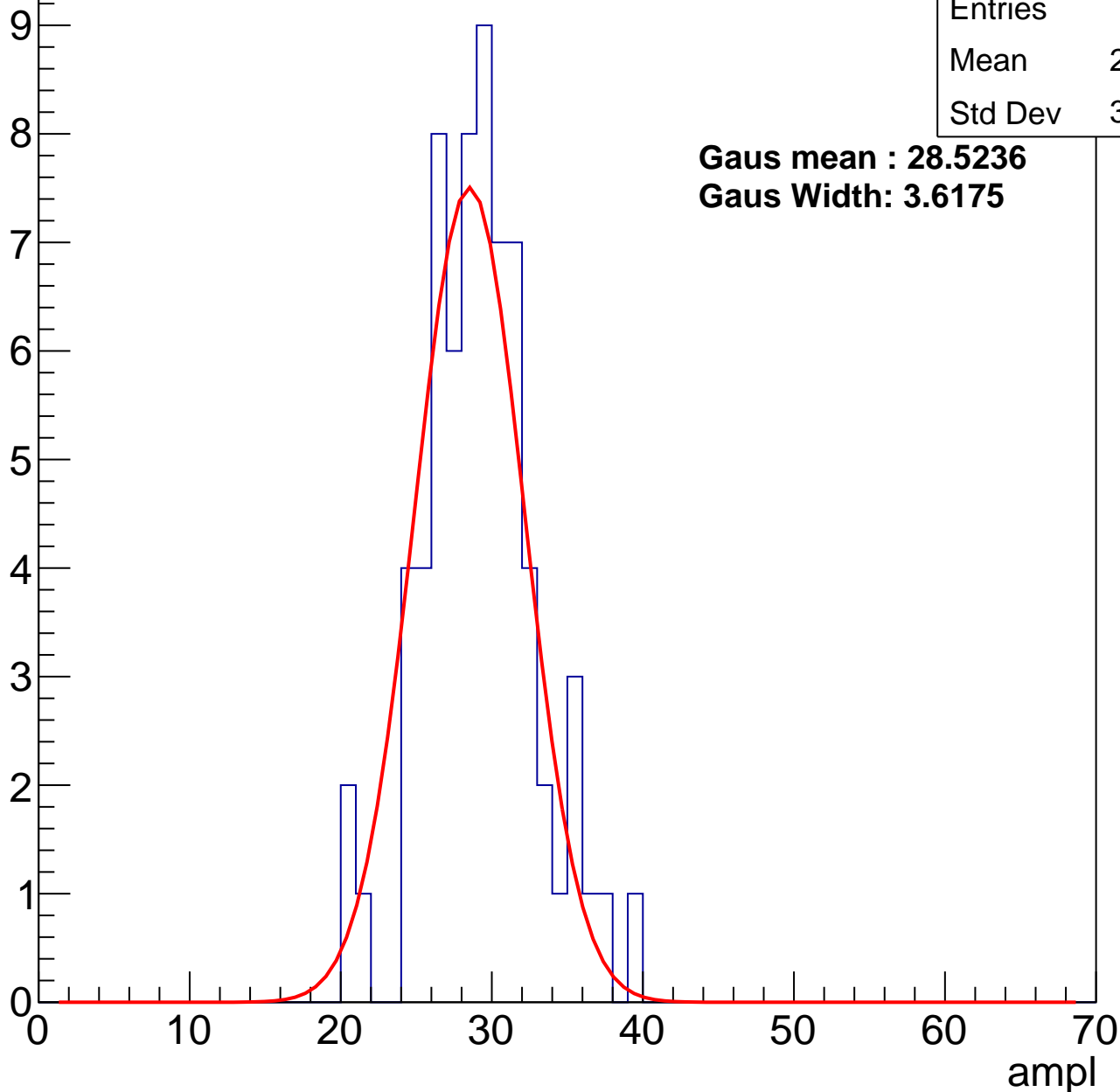
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	28.75
Std Dev	3.689

**Gaus mean : 28.5236**

**Gaus Width: 3.6175**



# B1L102S, U5-ch113, adc1

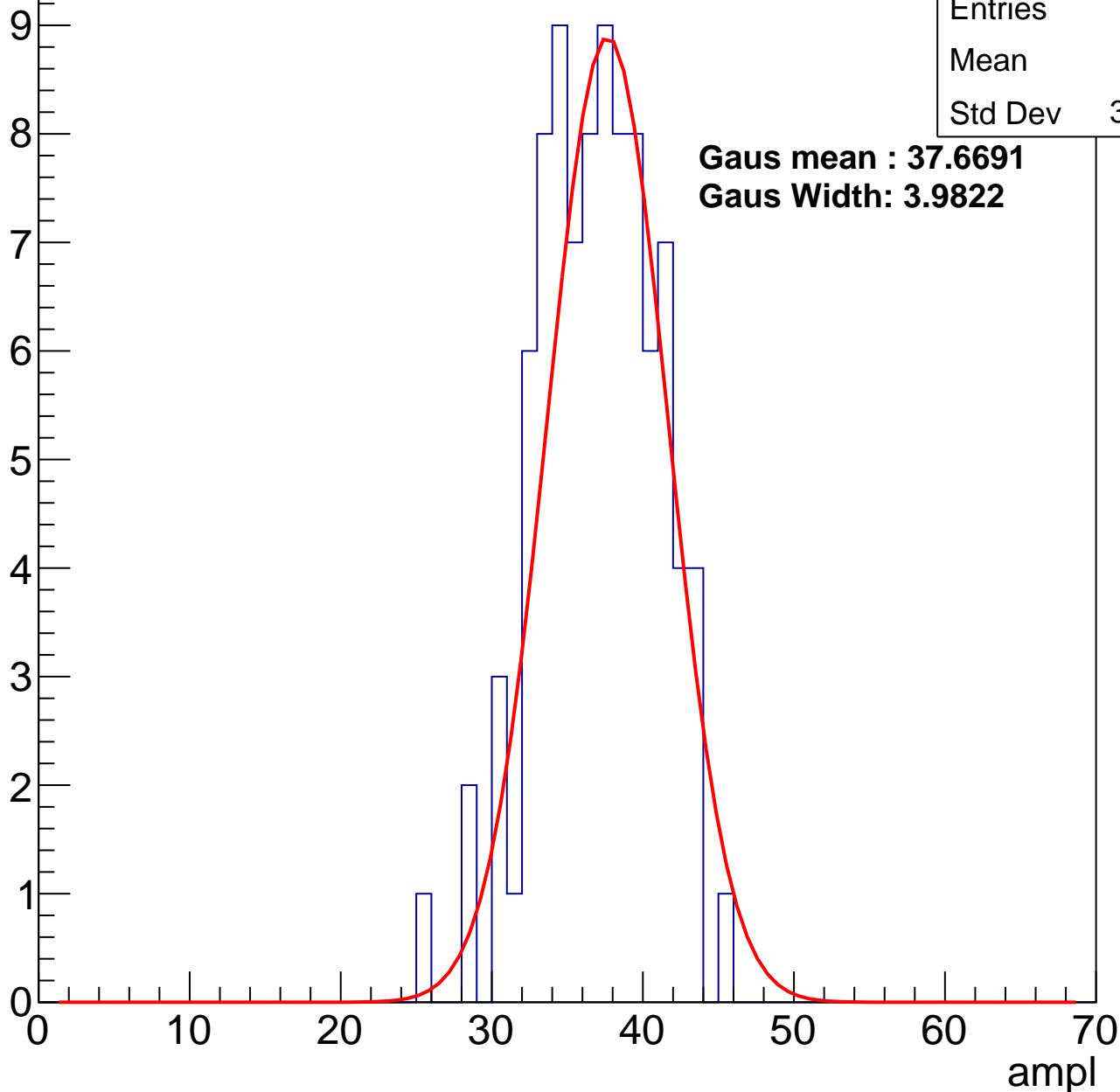
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	92
Mean	36.5
Std Dev	3.866

**Gaus mean : 37.6691**

**Gaus Width: 3.9822**



# B1L102S, U5-ch113, adc2

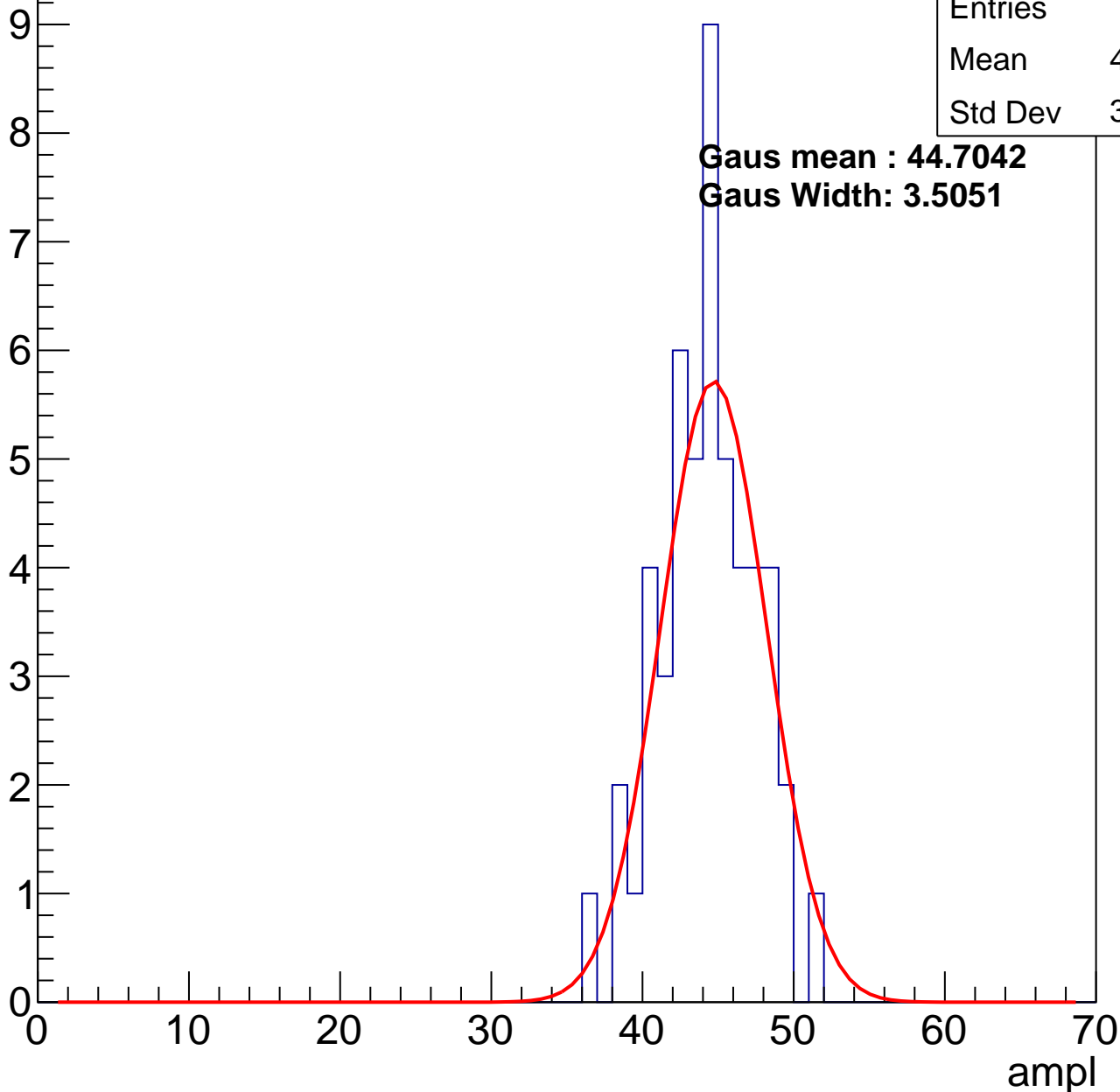
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	43.82
Std Dev	3.129

**Gaus mean : 44.7042**

**Gaus Width: 3.5051**

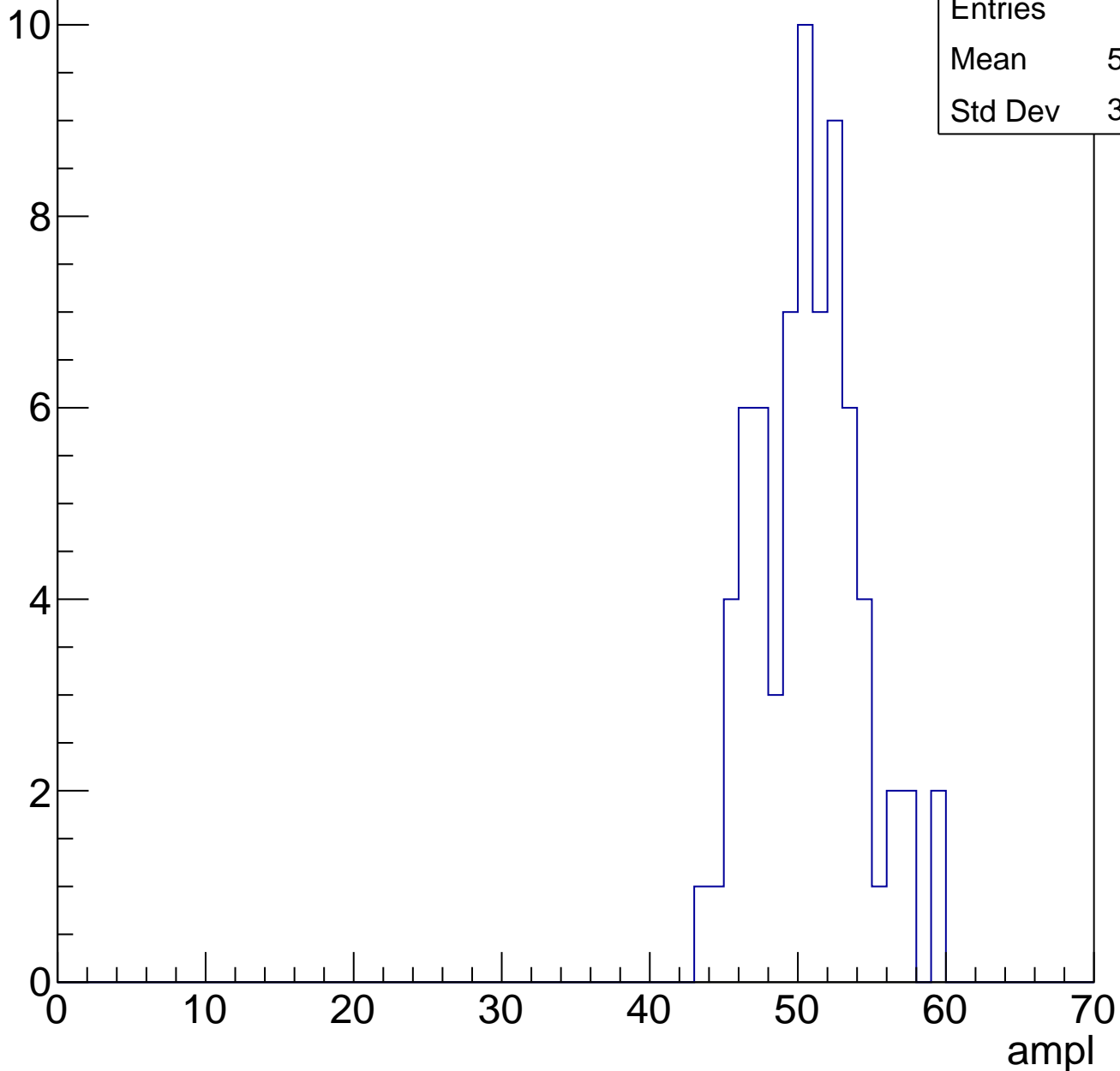


# B1L102S, U5-ch113, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	71
Mean	50.28
Std Dev	3.493

Entry

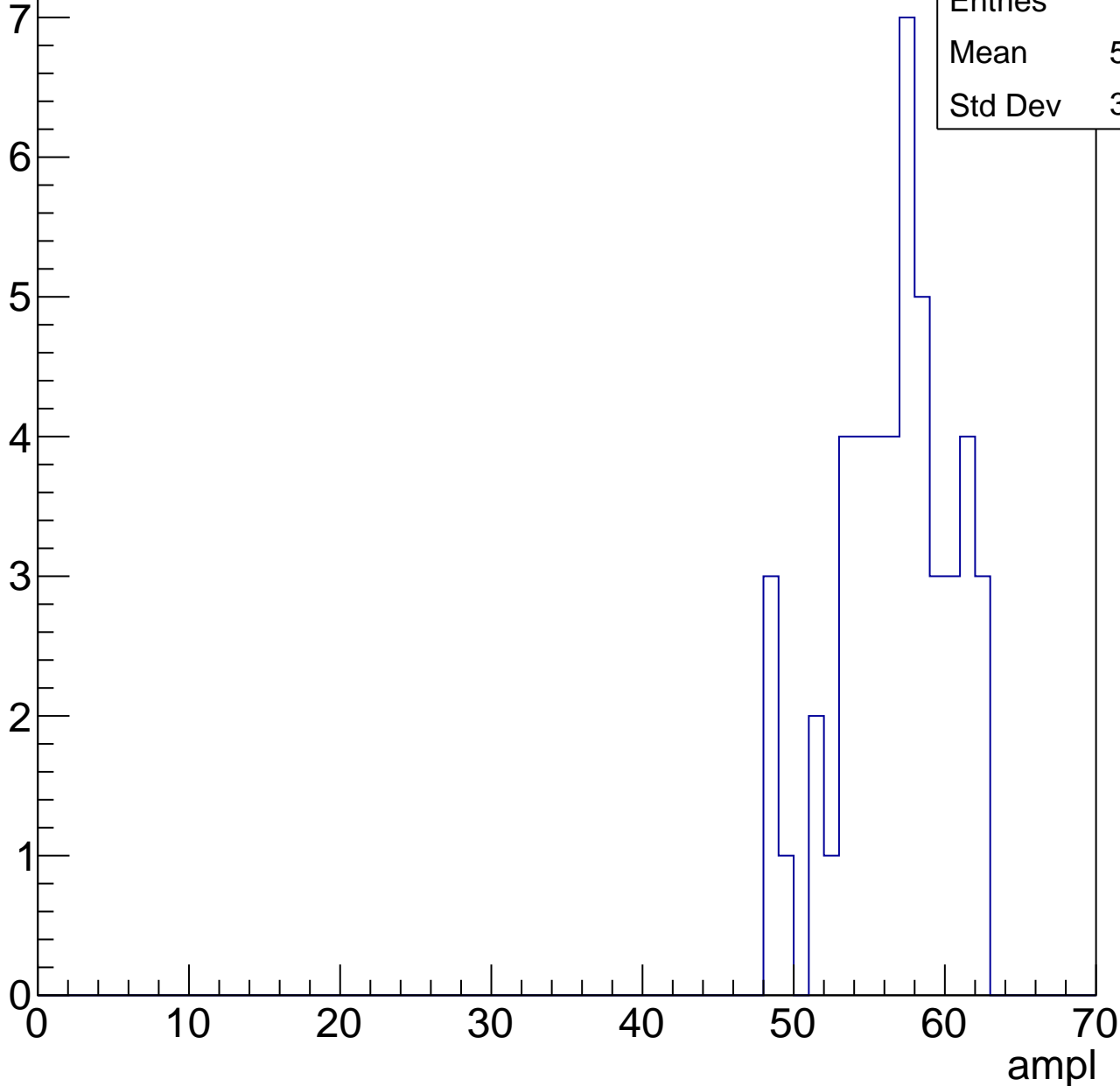


# B1L102S, U5-ch113, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

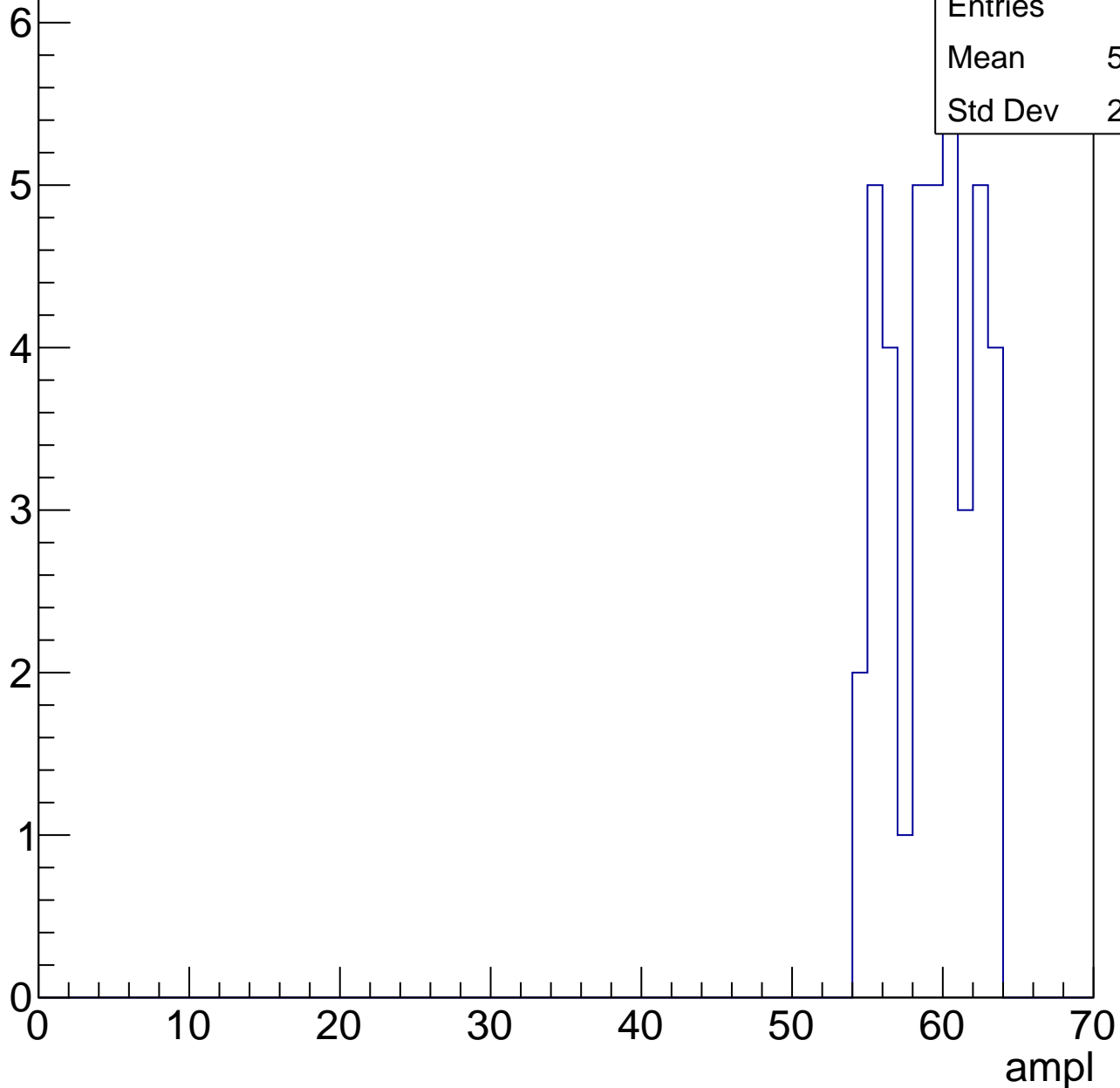
Entries	48
Mean	56.15
Std Dev	3.742



# B1L102S, U5-ch113, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

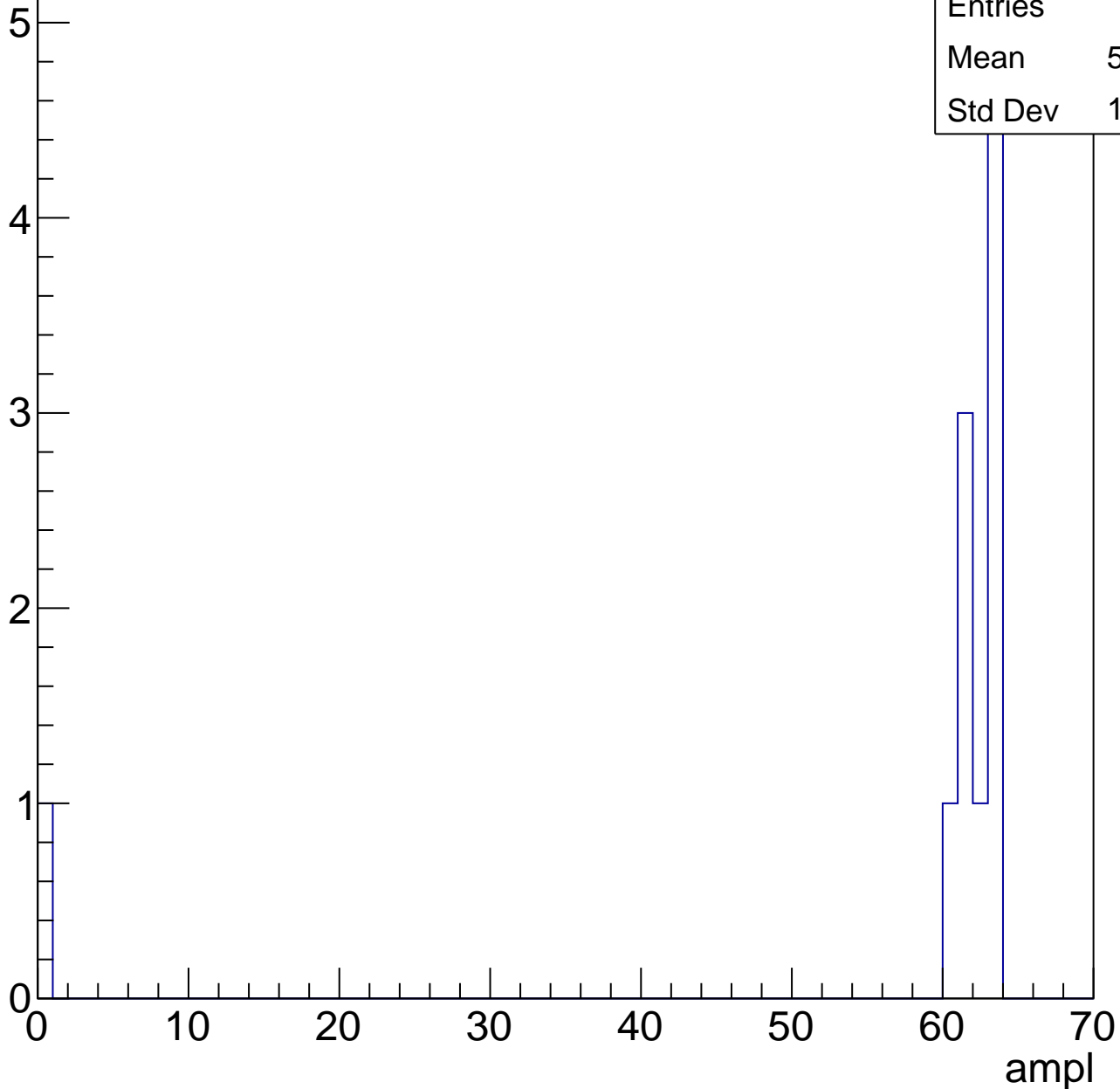


# B1L102S, U5-ch113, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	11
Mean	56.36
Std Dev	17.85





# B1L102S, U5-ch113, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U5-ch114, adc0

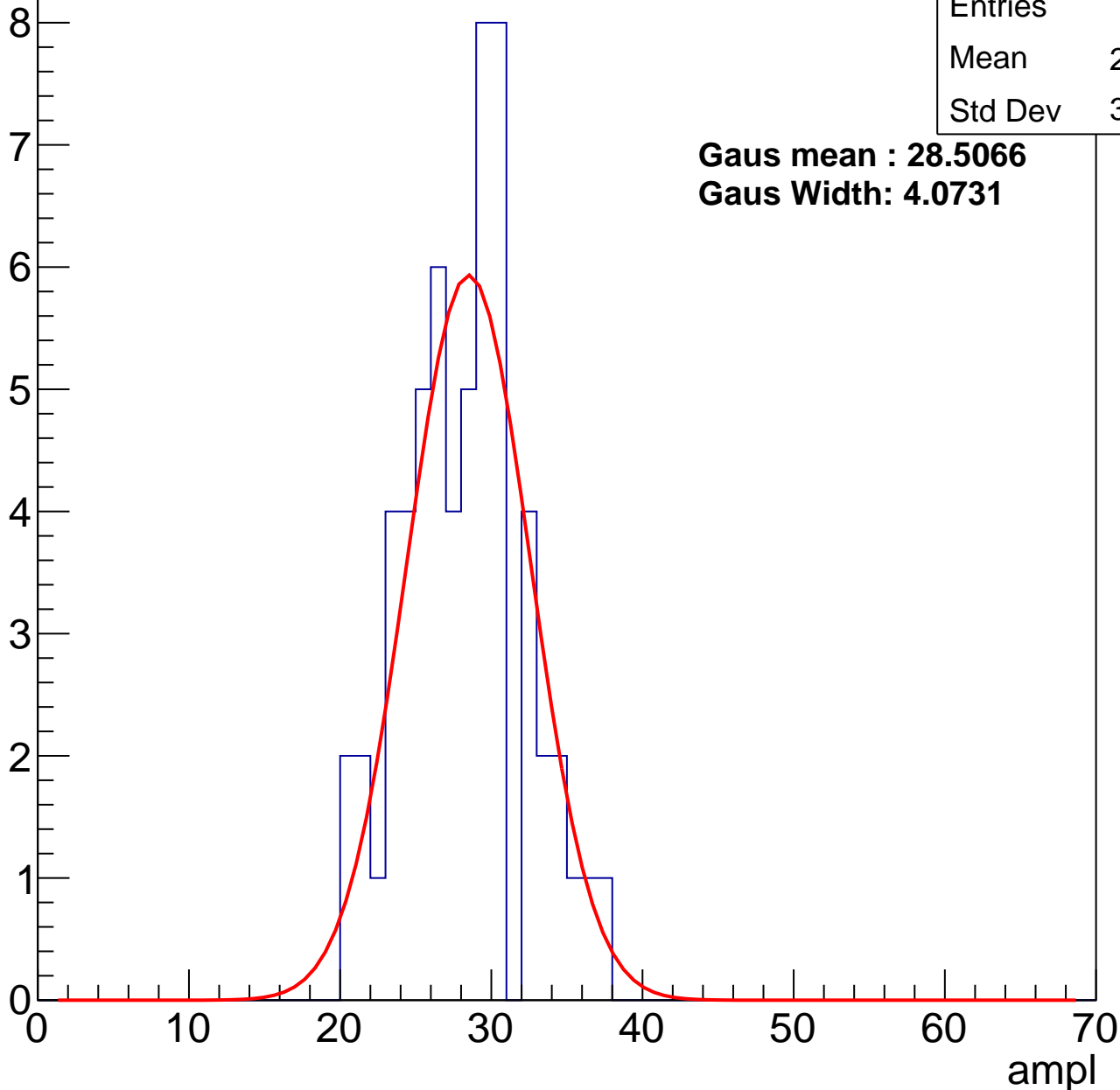
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	27.72
Std Dev	3.903

**Gaus mean : 28.5066**

**Gaus Width: 4.0731**



# B1L102S, U5-ch114, adc1

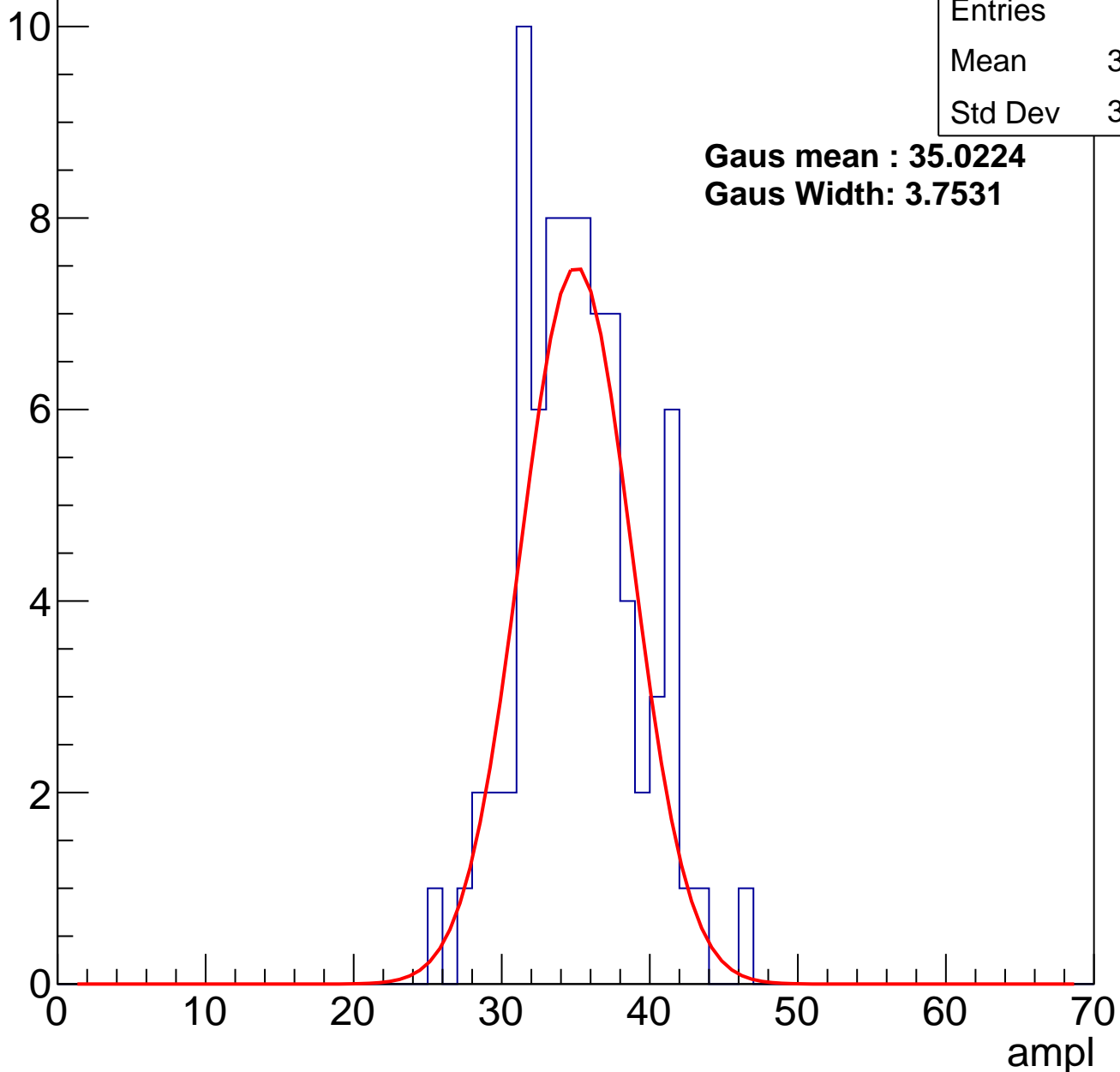
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	80
Mean	34.77
Std Dev	3.972

**Gaus mean : 35.0224**

**Gaus Width: 3.7531**

Entry



# B1L102S, U5-ch114, adc2

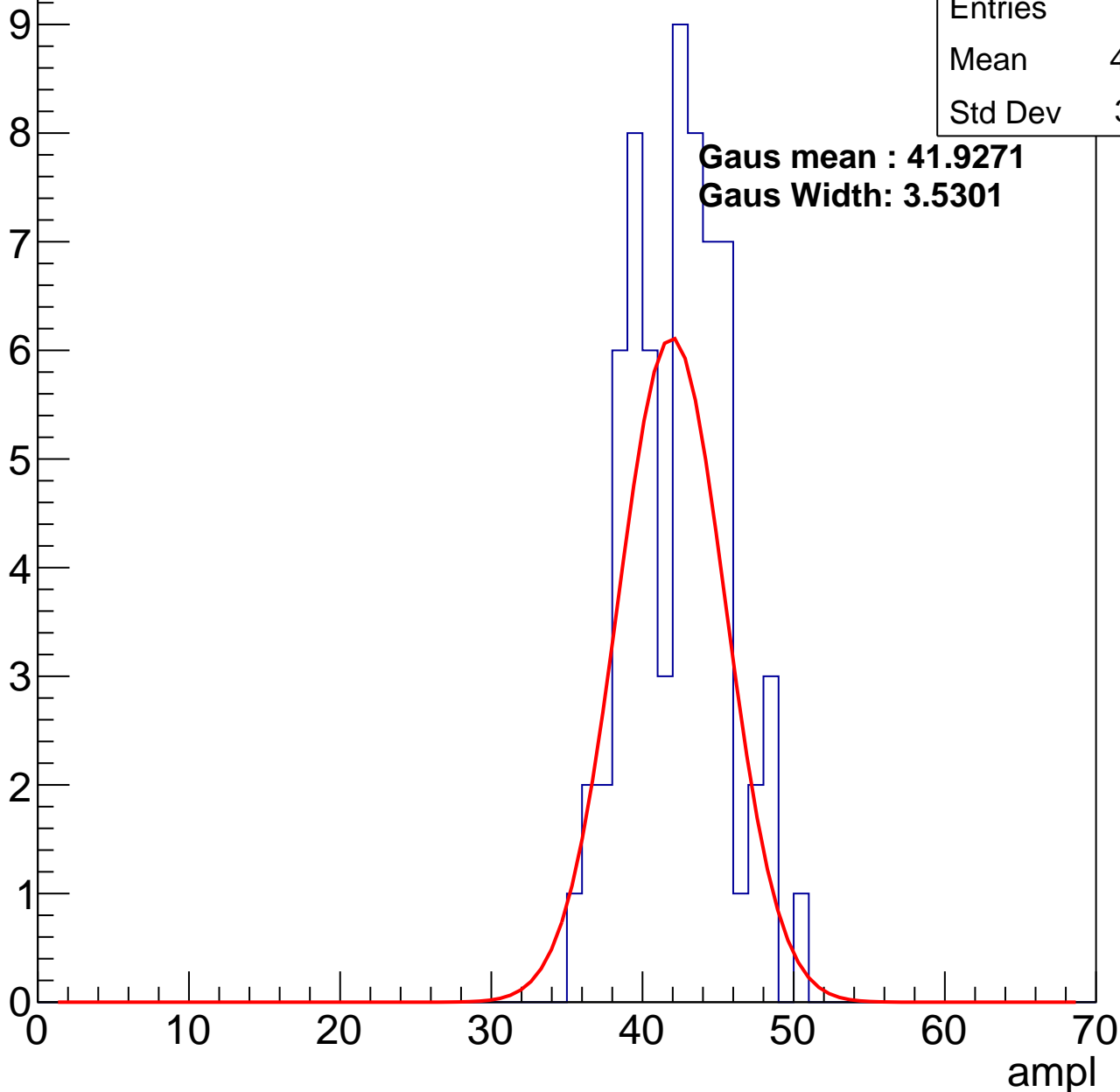
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	41.86
Std Dev	3.261

**Gaus mean : 41.9271**

**Gaus Width: 3.5301**

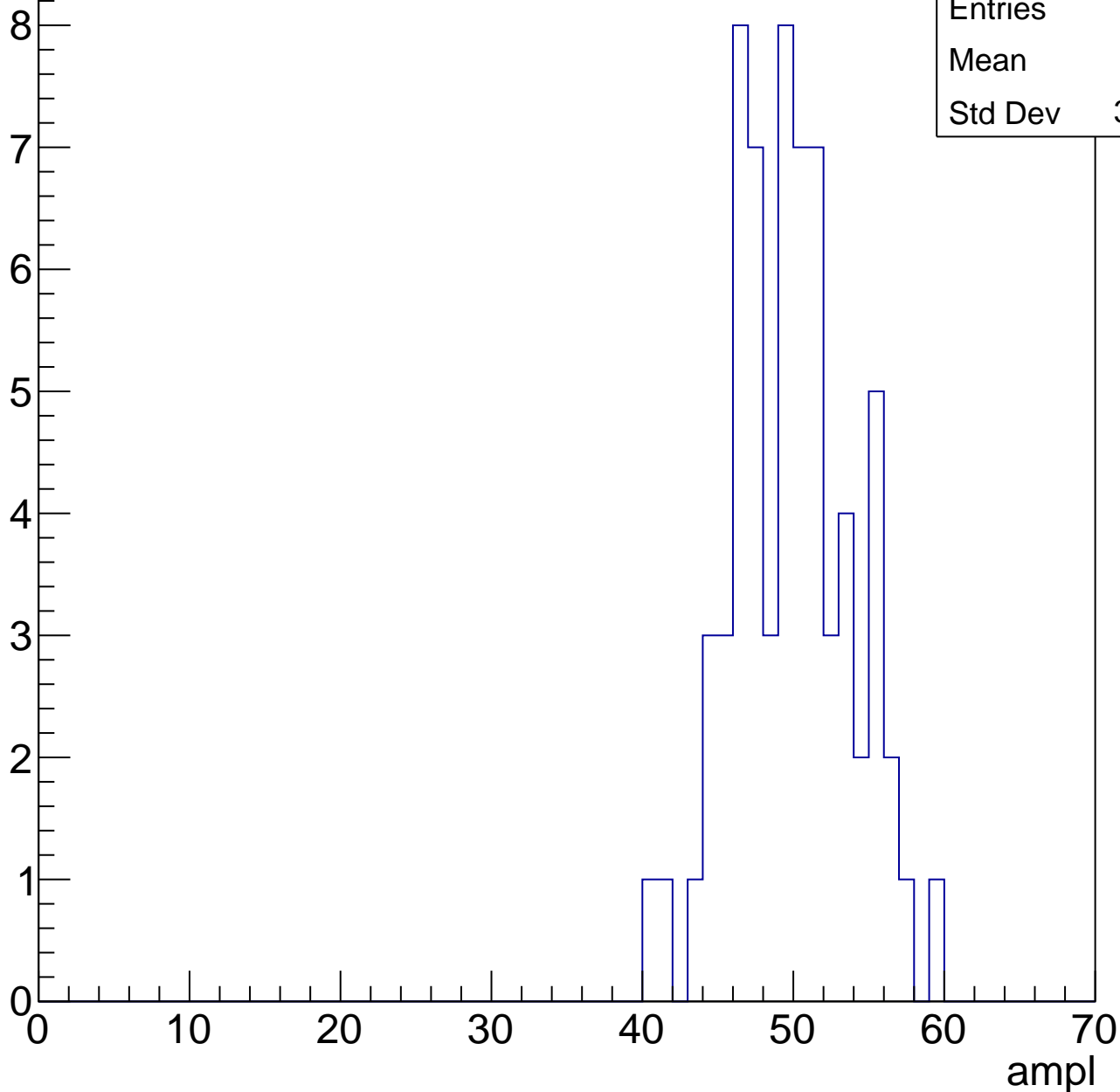


# B1L102S, U5-ch114, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	49.4
Std Dev	3.891

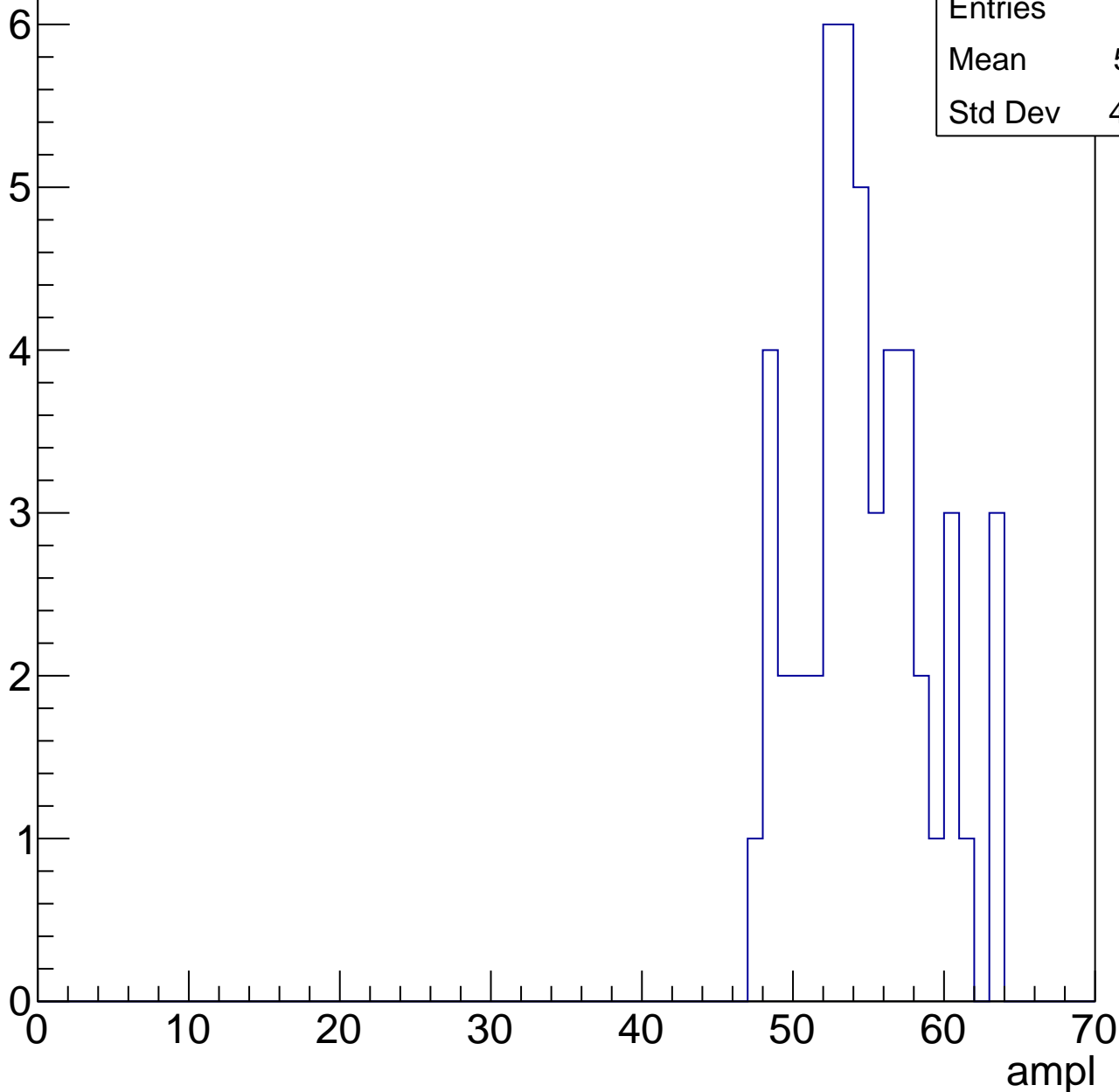


# B1L102S, U5-ch114, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	54.31
Std Dev	4.117

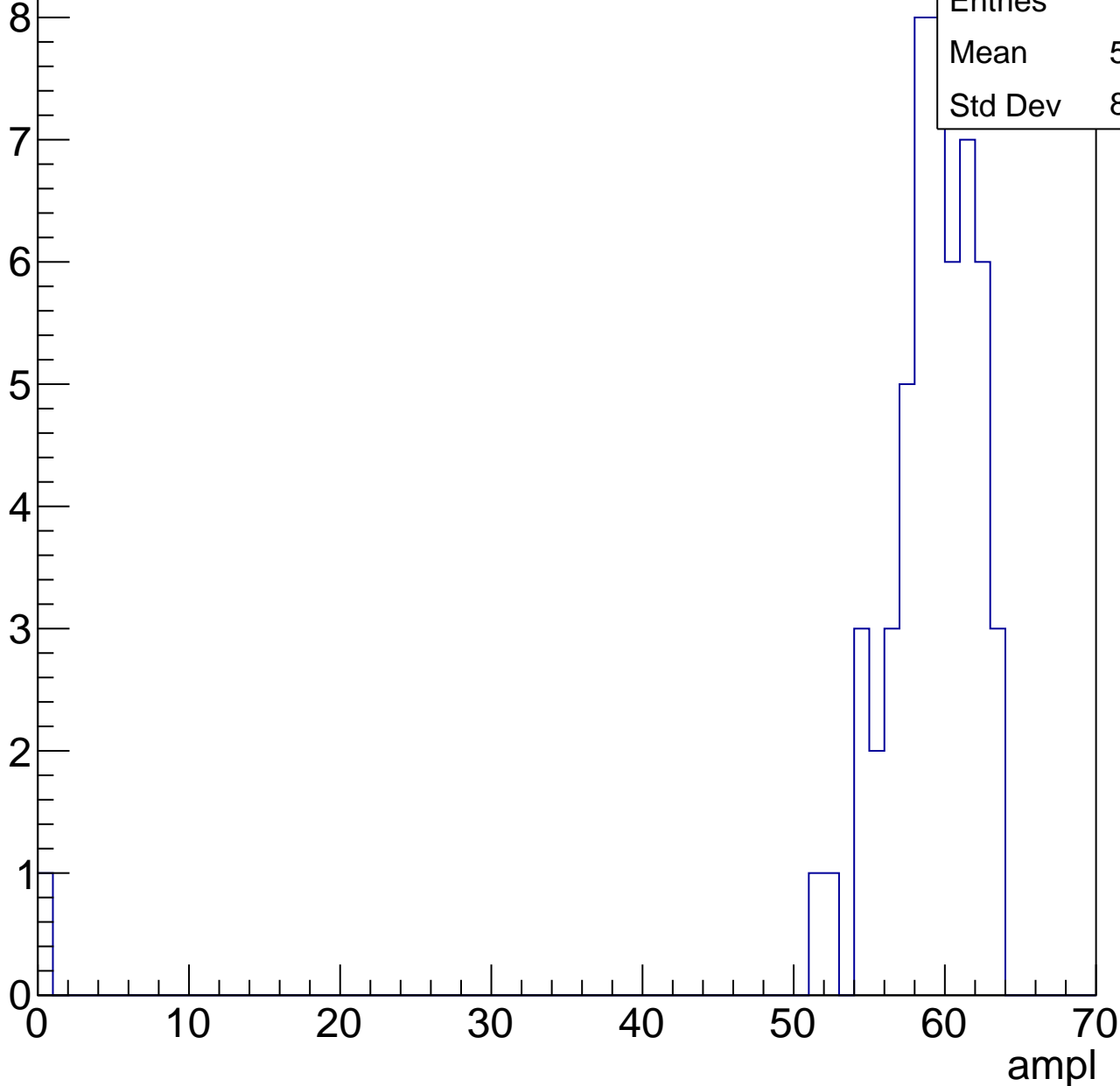


# B1L102S, U5-ch114, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

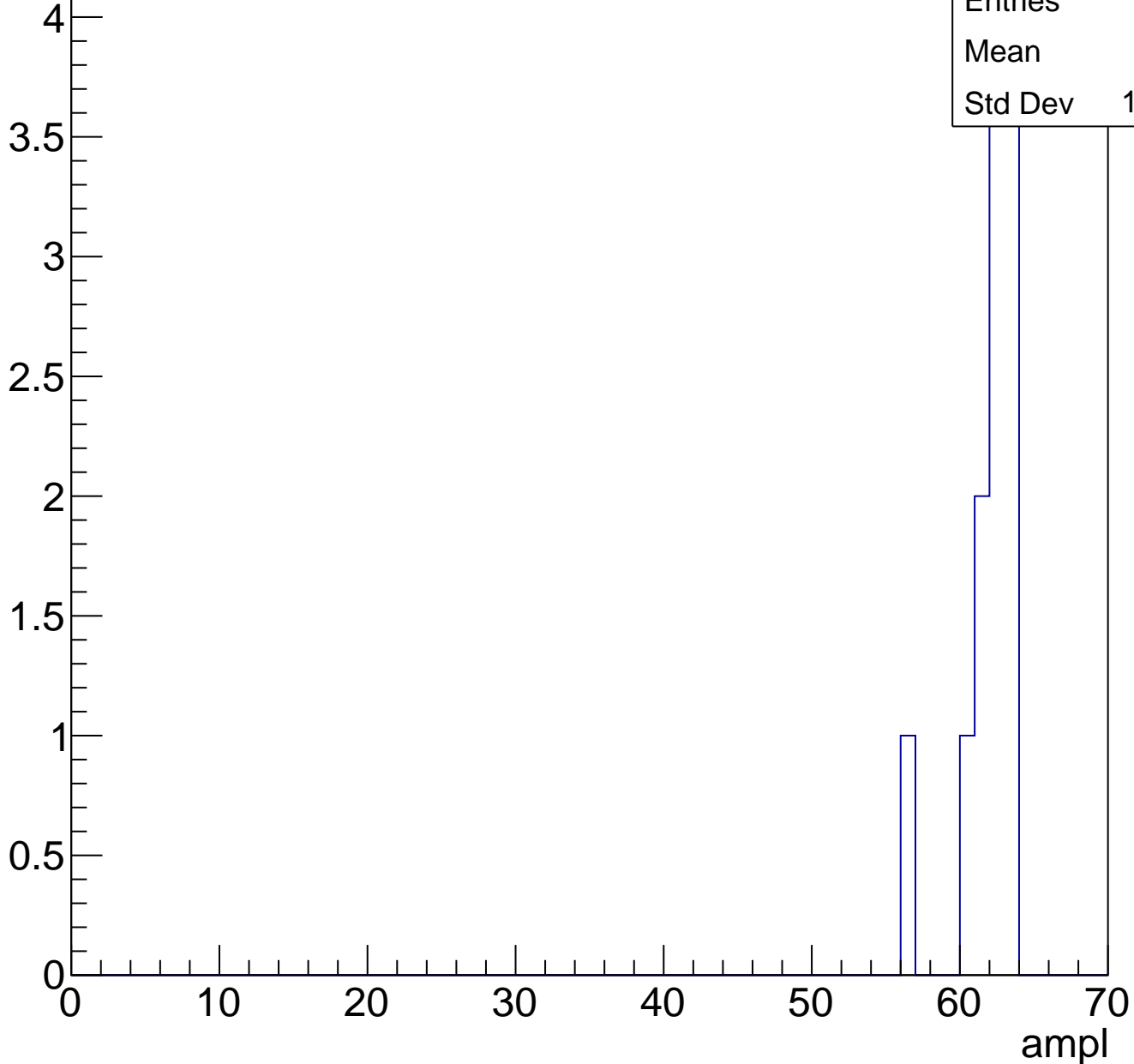
Entries	54
Mean	57.63
Std Dev	8.378



# B1L102S, U5-ch114, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U5-ch114, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U5-ch115, adc0

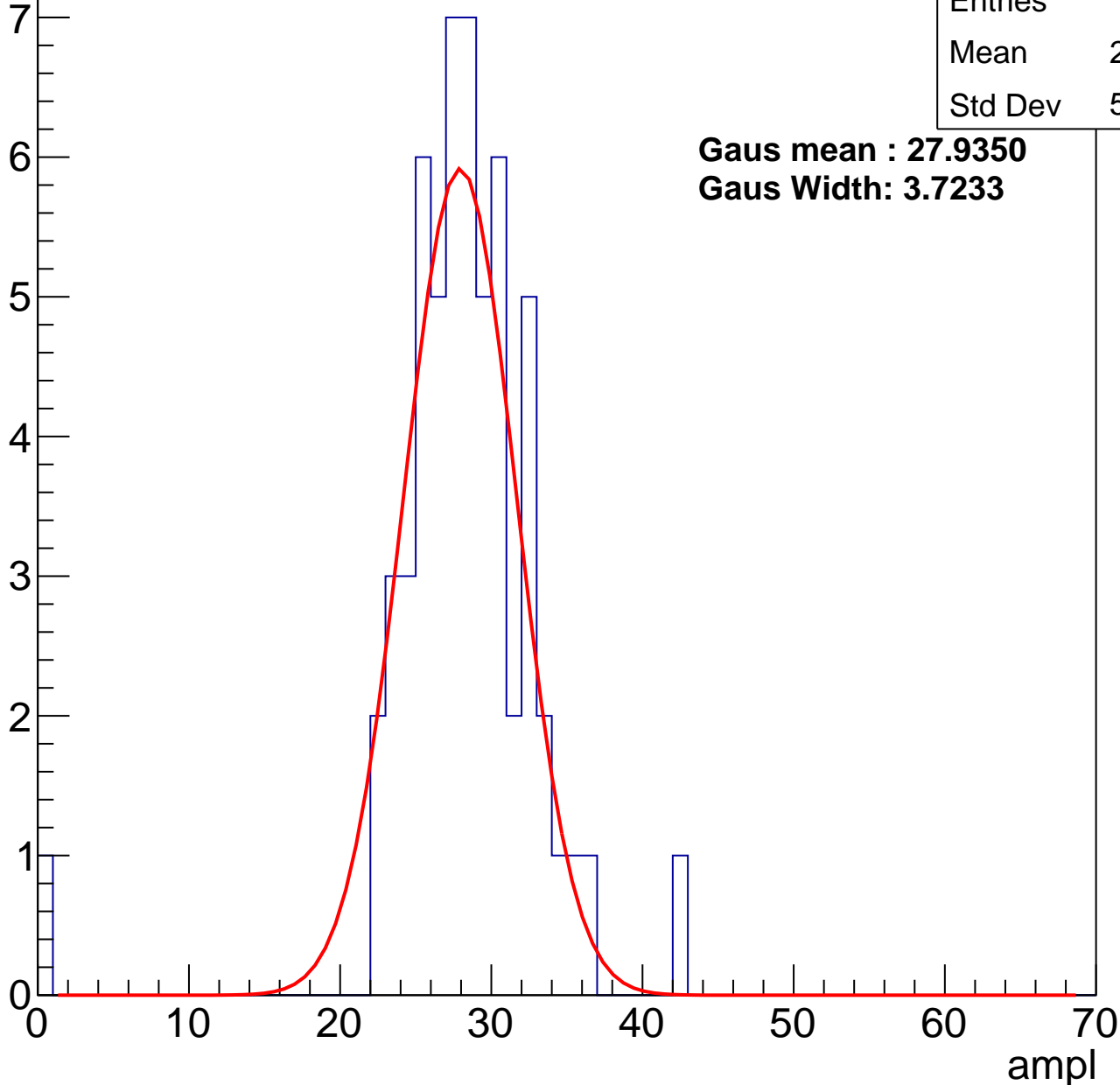
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	27.76
Std Dev	5.217

**Gaus mean : 27.9350**

**Gaus Width: 3.7233**



# B1L102S, U5-ch115, adc1

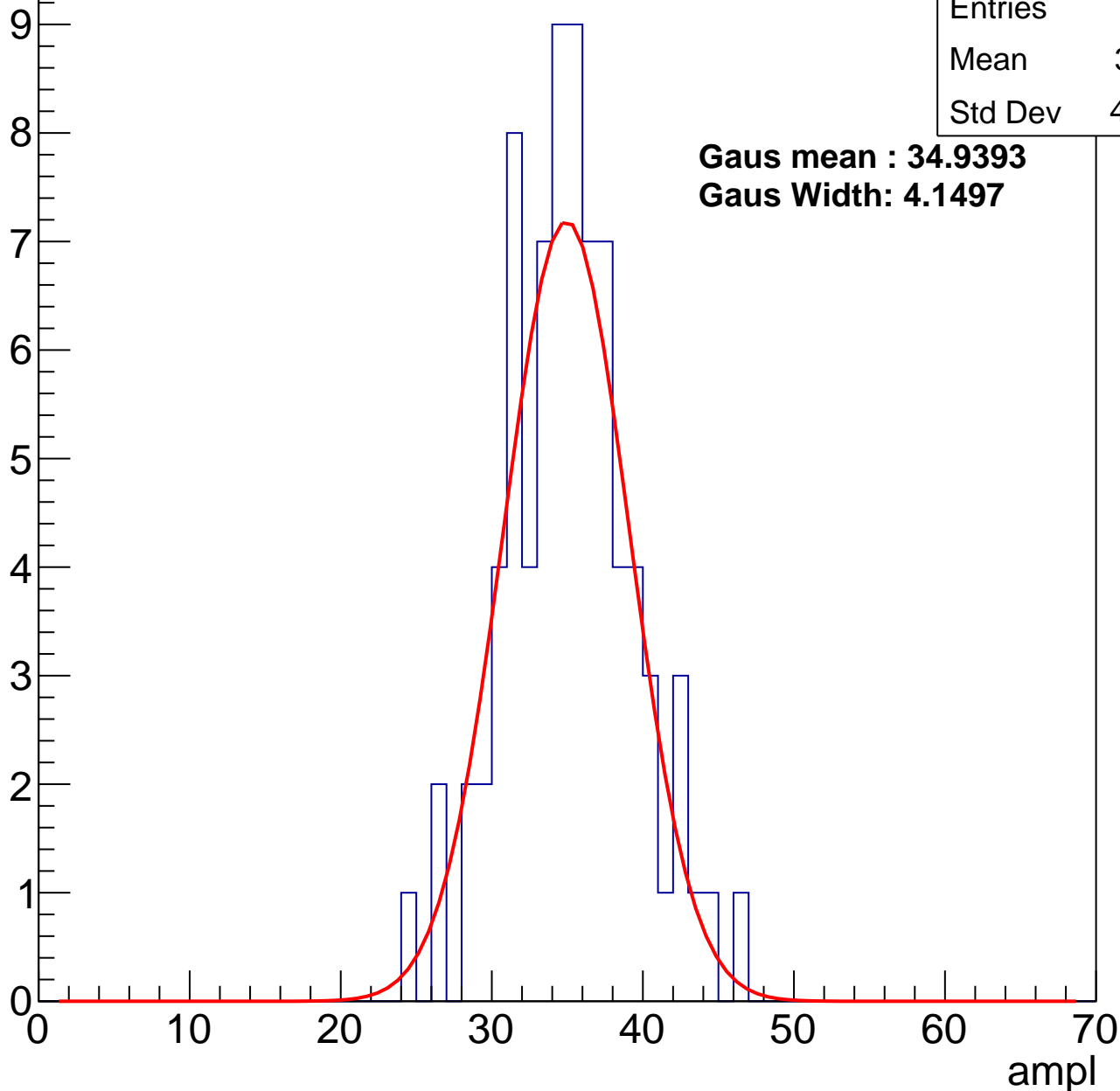
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	80
Mean	34.71
Std Dev	4.193

**Gaus mean : 34.9393**

**Gaus Width: 4.1497**



# B1L102S, U5-ch115, adc2

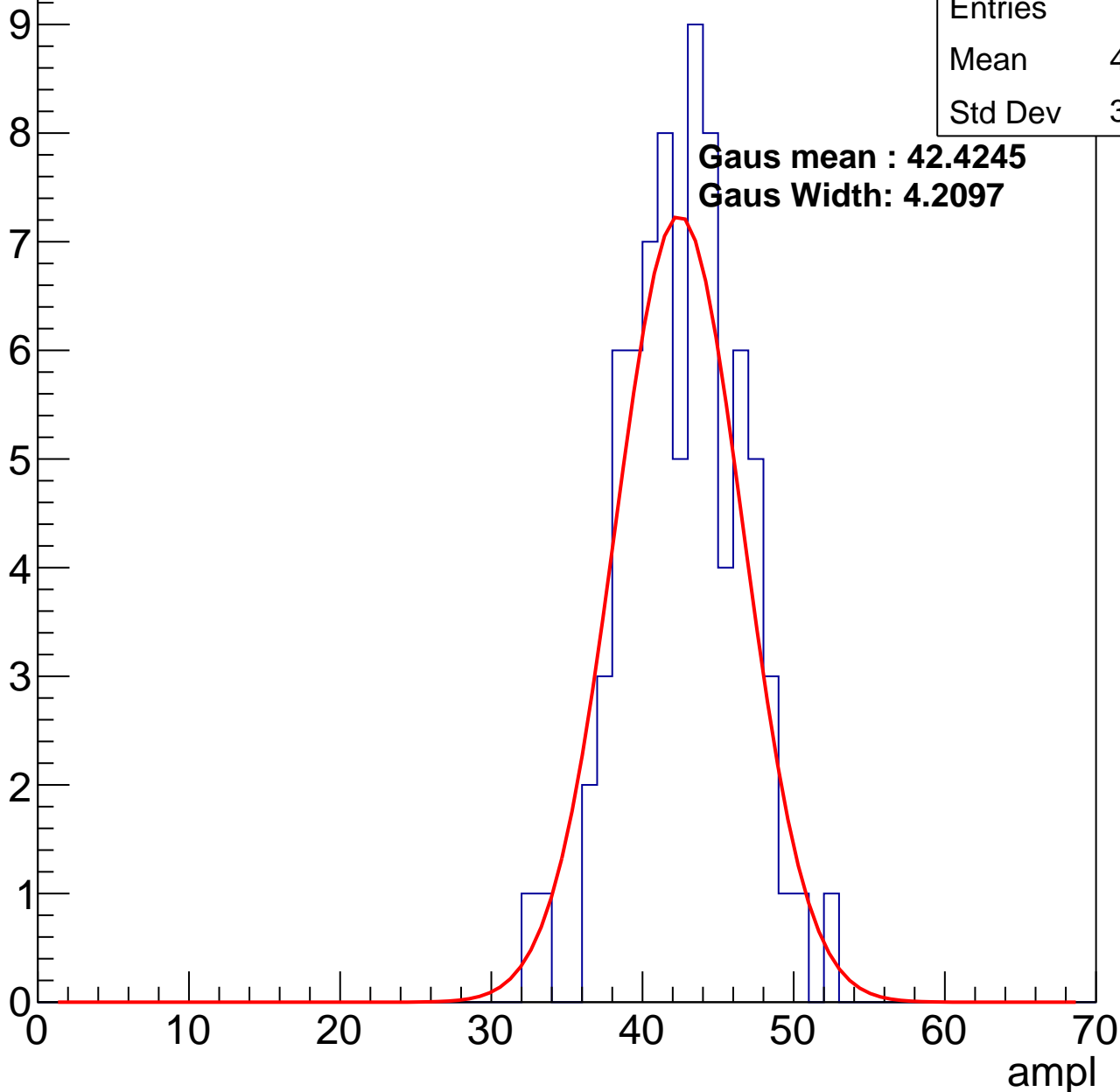
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	42.25
Std Dev	3.828

**Gaus mean : 42.4245**

**Gaus Width: 4.2097**

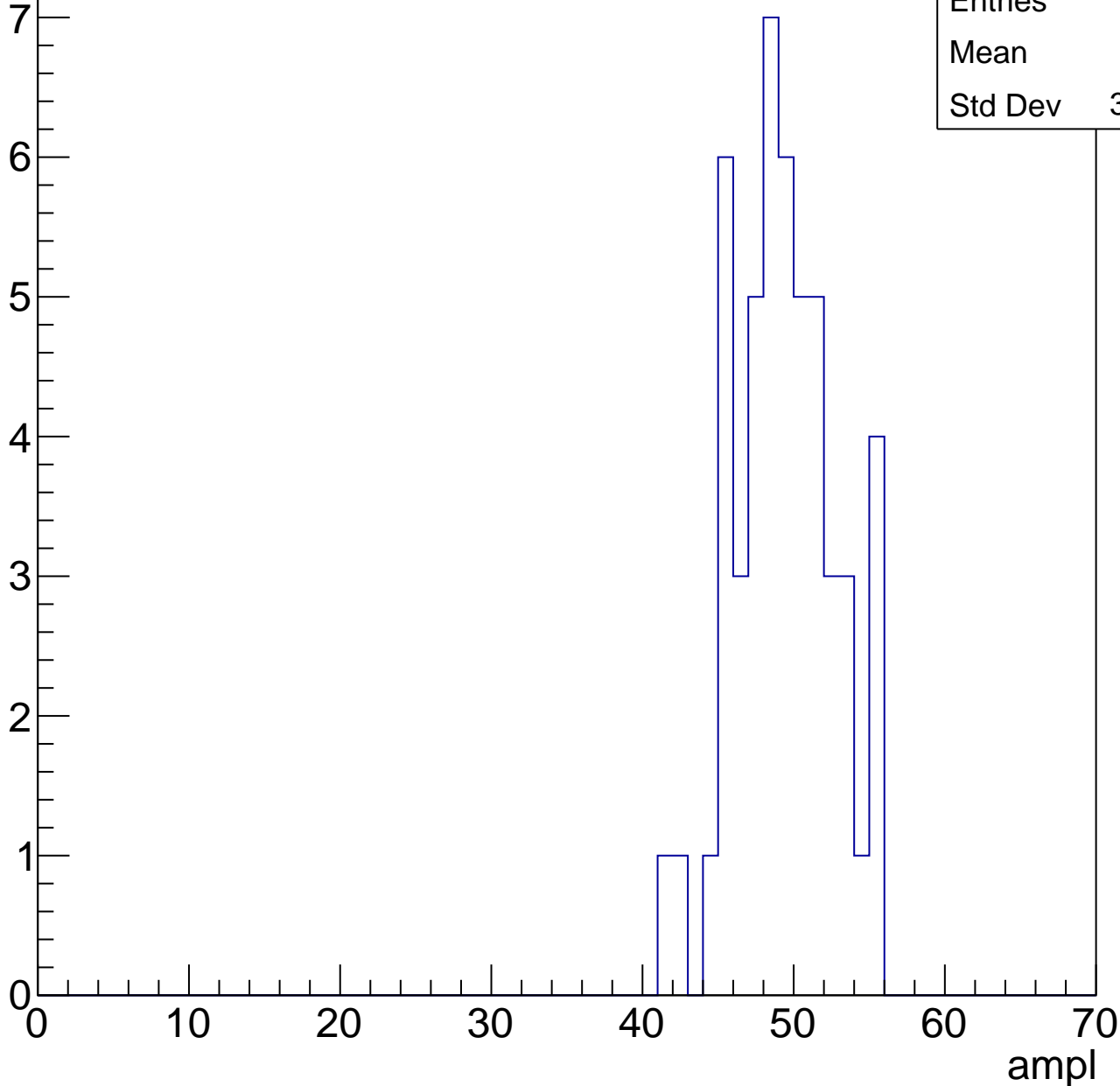


# B1L102S, U5-ch115, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	48.9
Std Dev	3.303

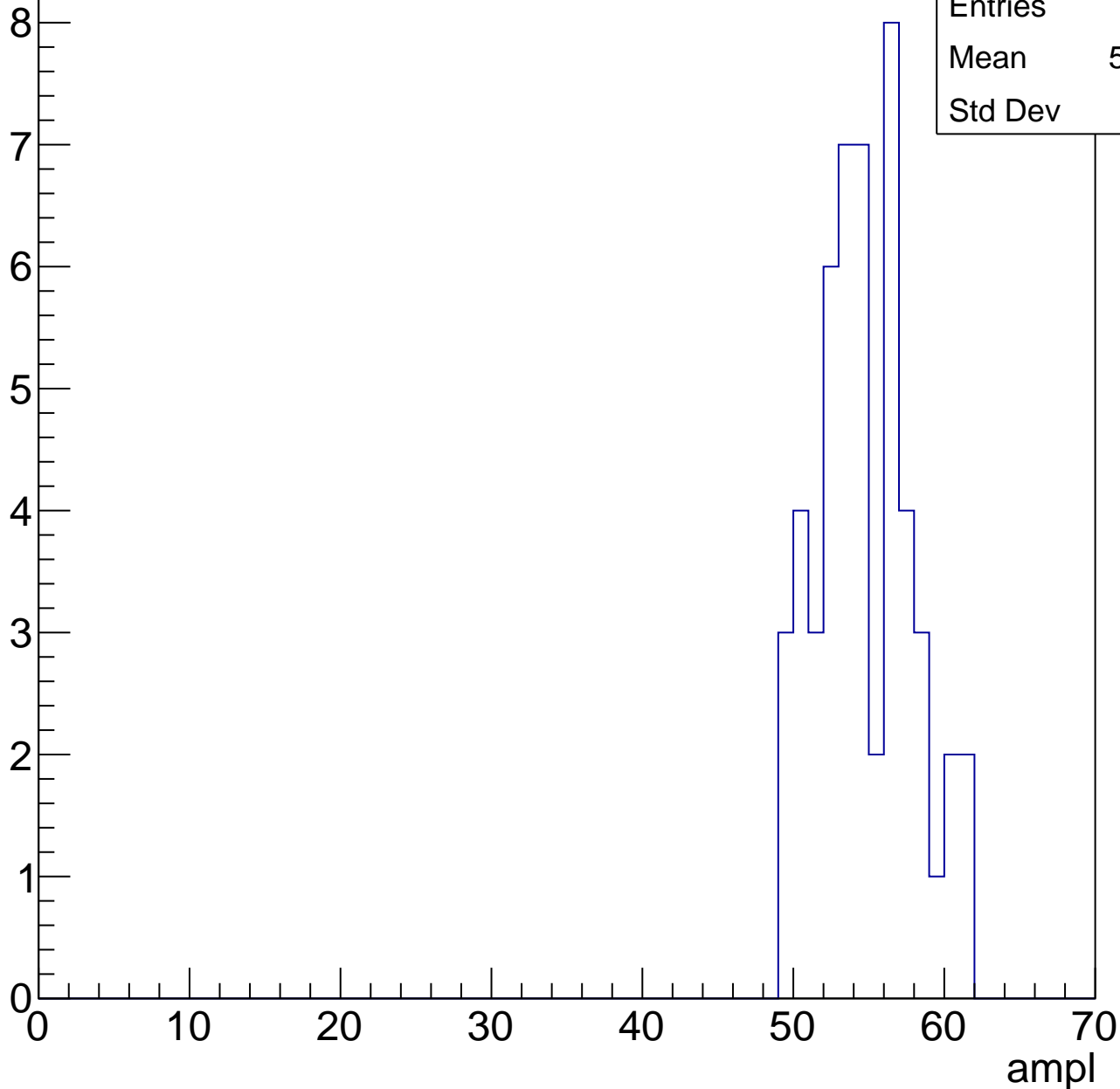


# B1L102S, U5-ch115, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	54.27
Std Dev	3.12

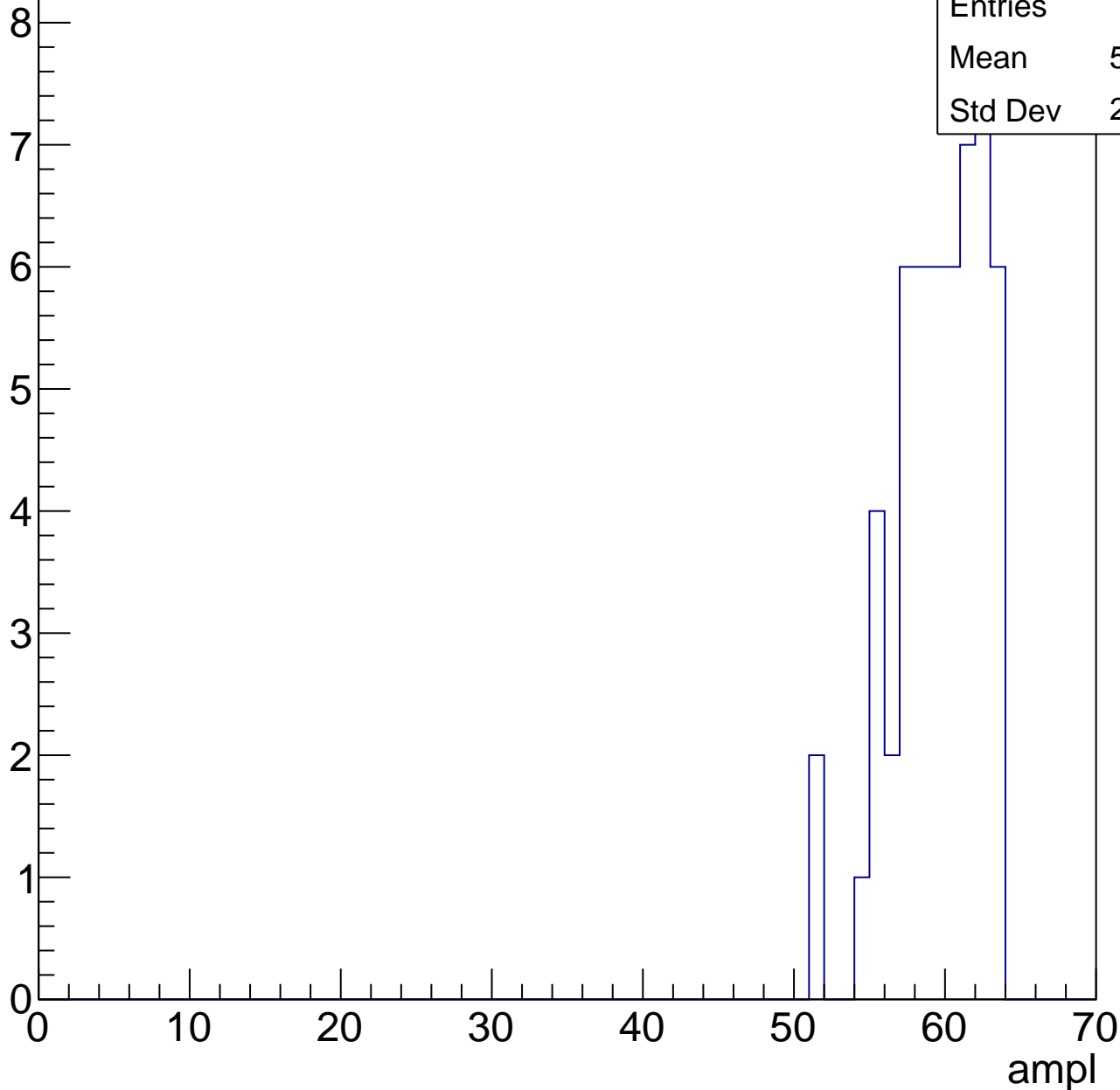


# B1L102S, U5-ch115, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

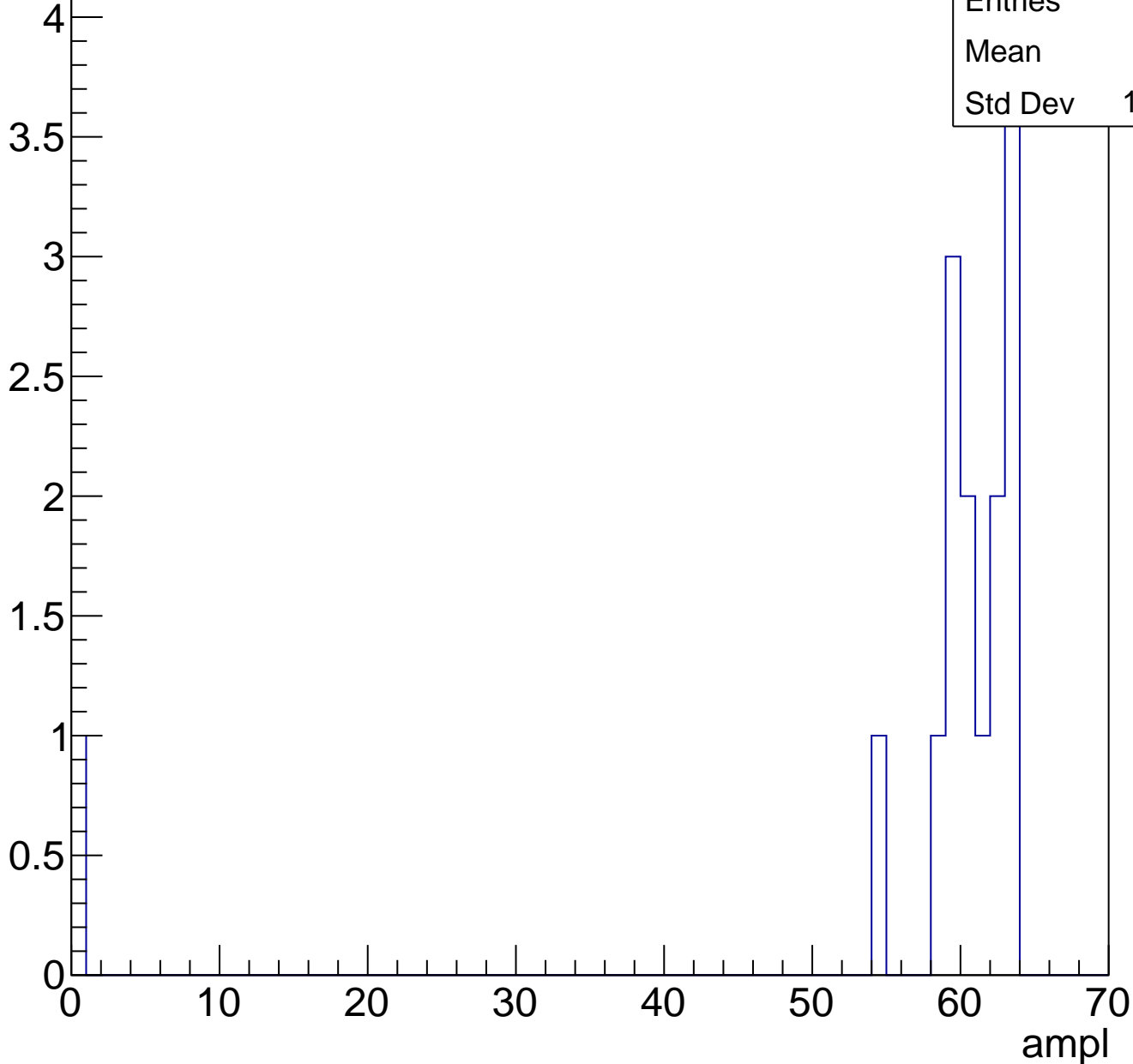
Entries	54
Mean	59.13
Std Dev	2.938



# B1L102S, U5-ch115, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U5-ch115, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U5-ch116, adc0

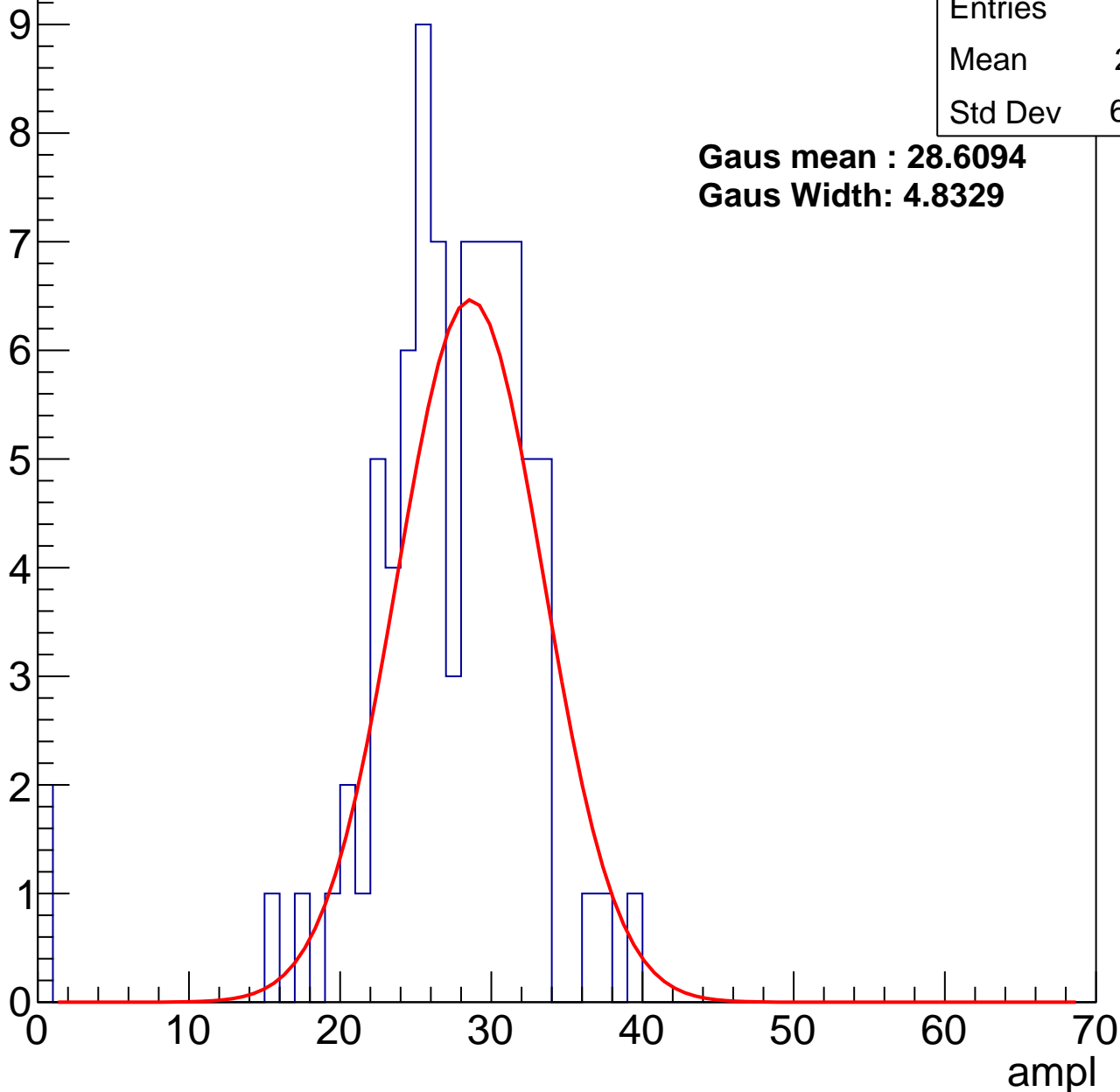
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	83
Mean	26.61
Std Dev	6.026

**Gaus mean : 28.6094**

**Gaus Width: 4.8329**



# B1L102S, U5-ch116, adc1

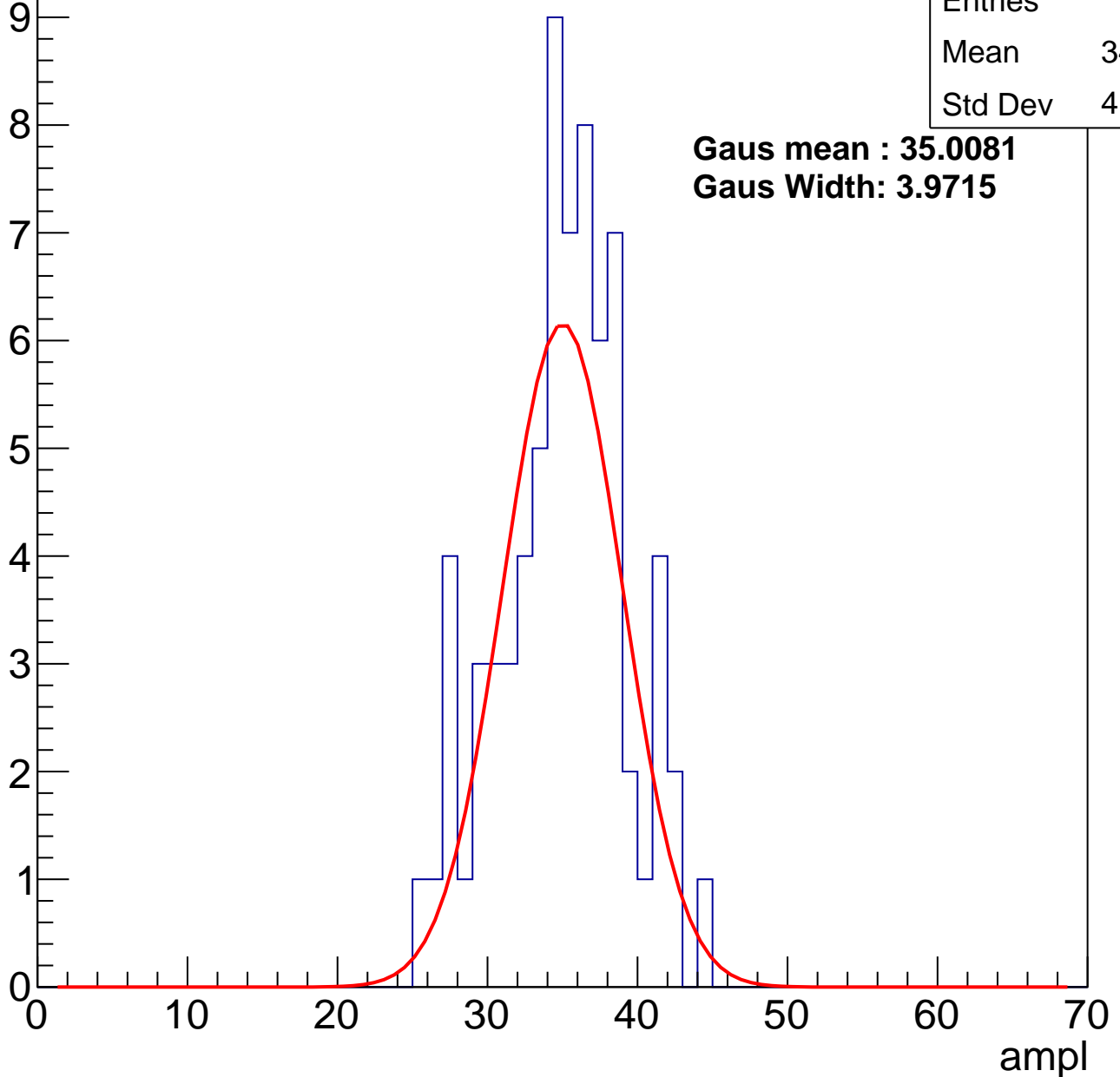
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	34.54
Std Dev	4.153

**Gaus mean : 35.0081**

**Gaus Width: 3.9715**



# B1L102S, U5-ch116, adc2

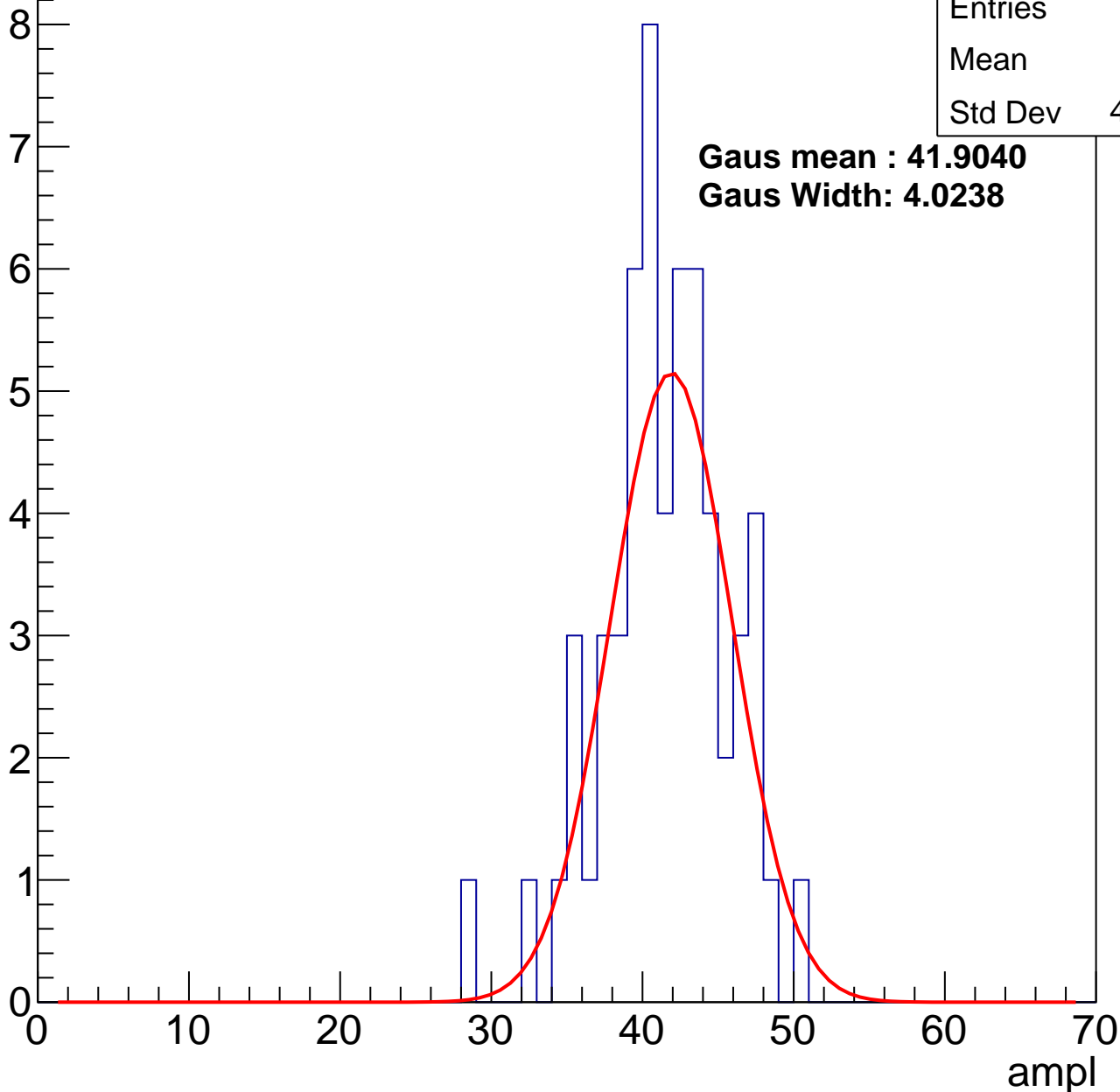
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	41
Std Dev	4.123

**Gaus mean : 41.9040**

**Gaus Width: 4.0238**

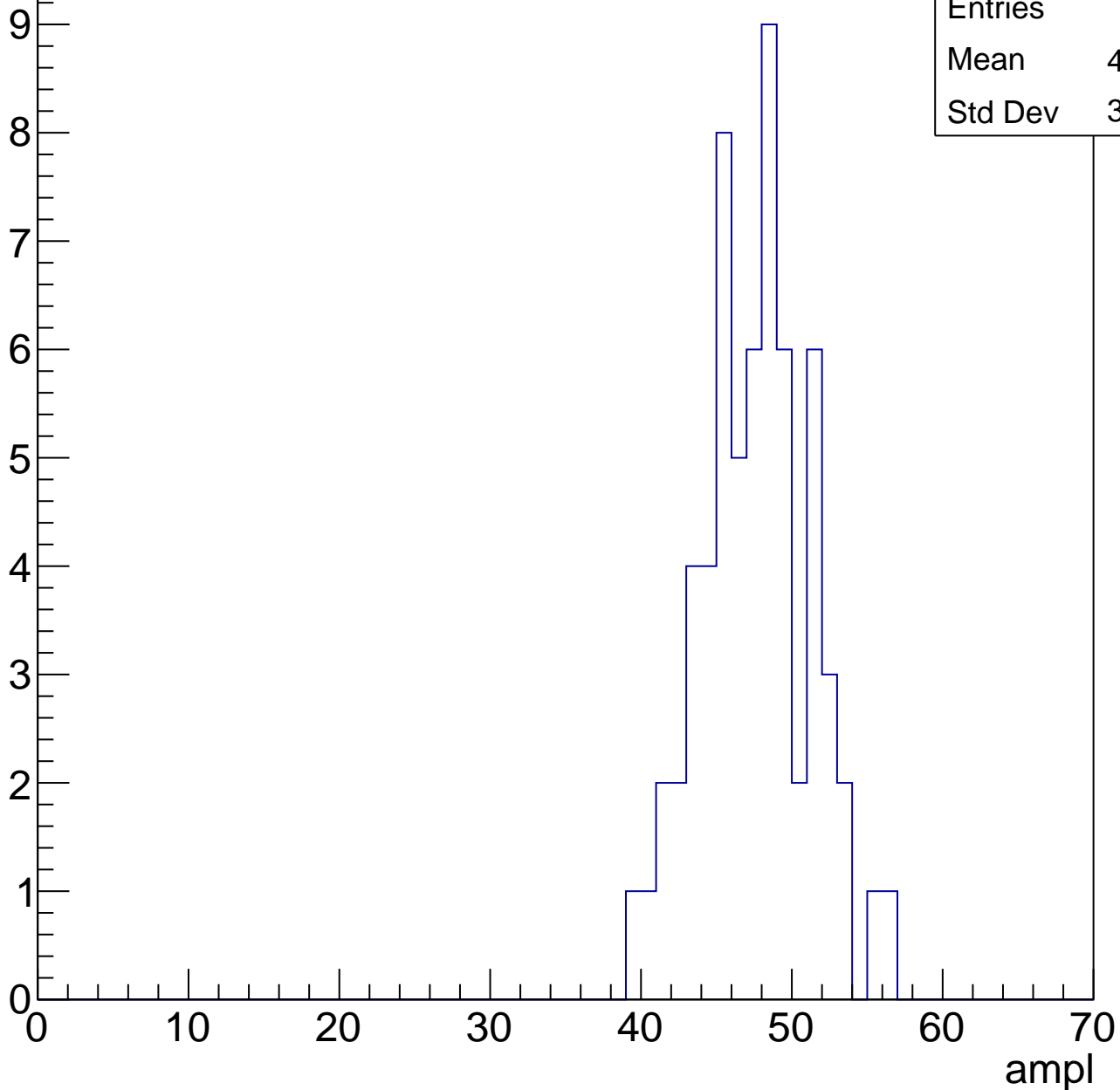


# B1L102S, U5-ch116, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	47.14
Std Dev	3.585

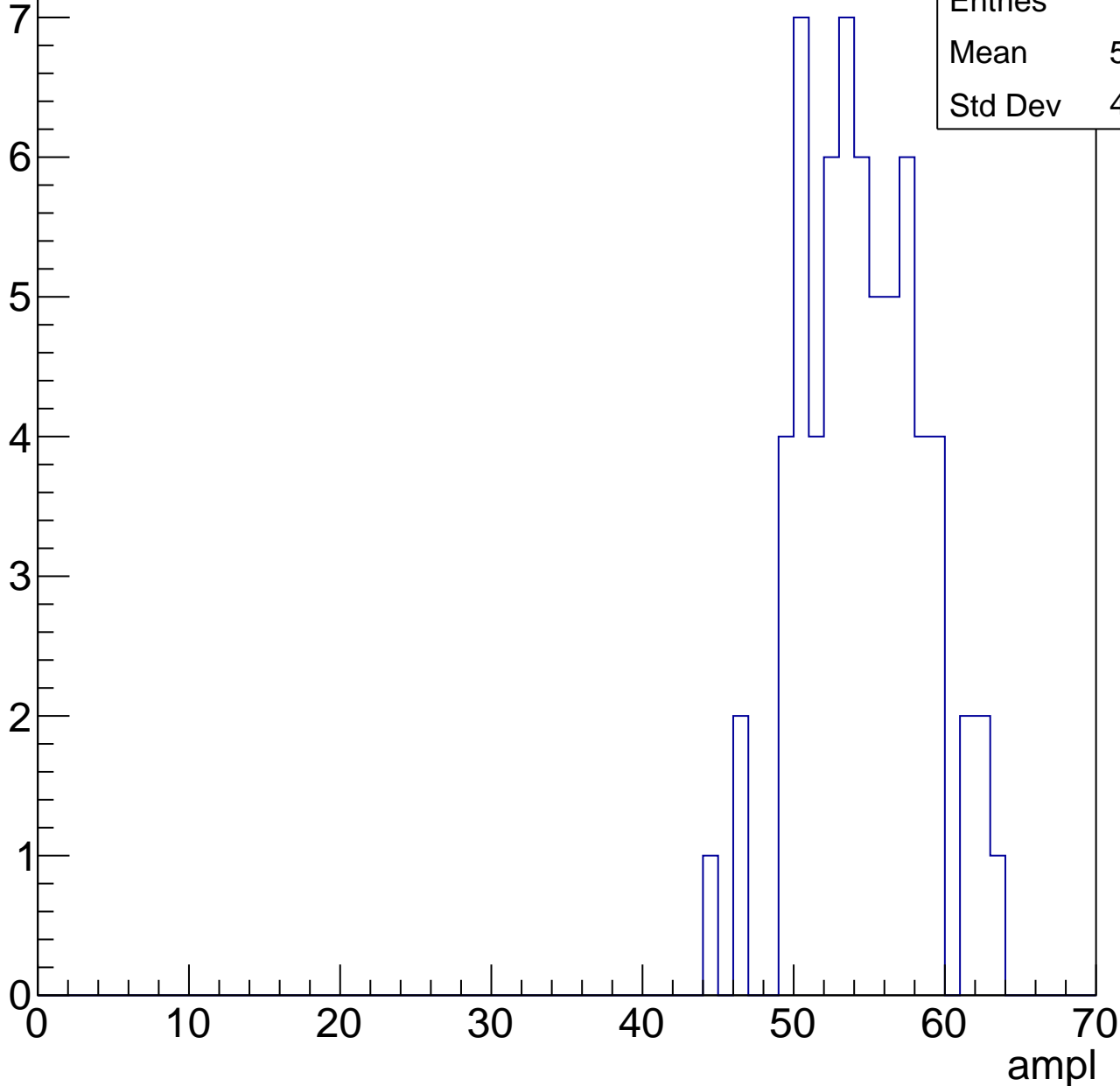


# B1L102S, U5-ch116, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	54.05
Std Dev	4.002



# B1L102S, U5-ch116, adc5

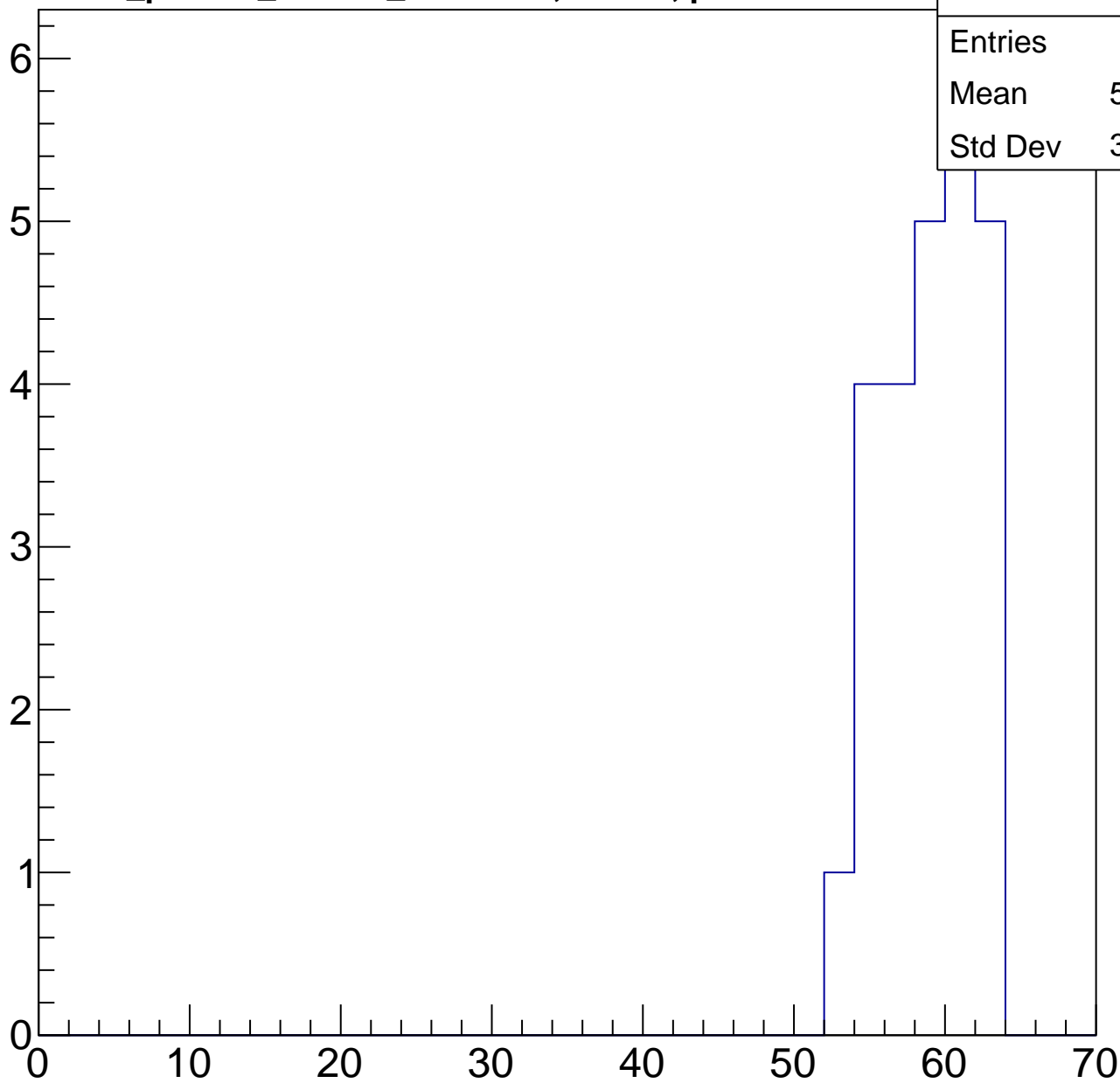
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

6  
5  
4  
3  
2  
1  
0

Entries	50
Mean	58.58
Std Dev	3.007

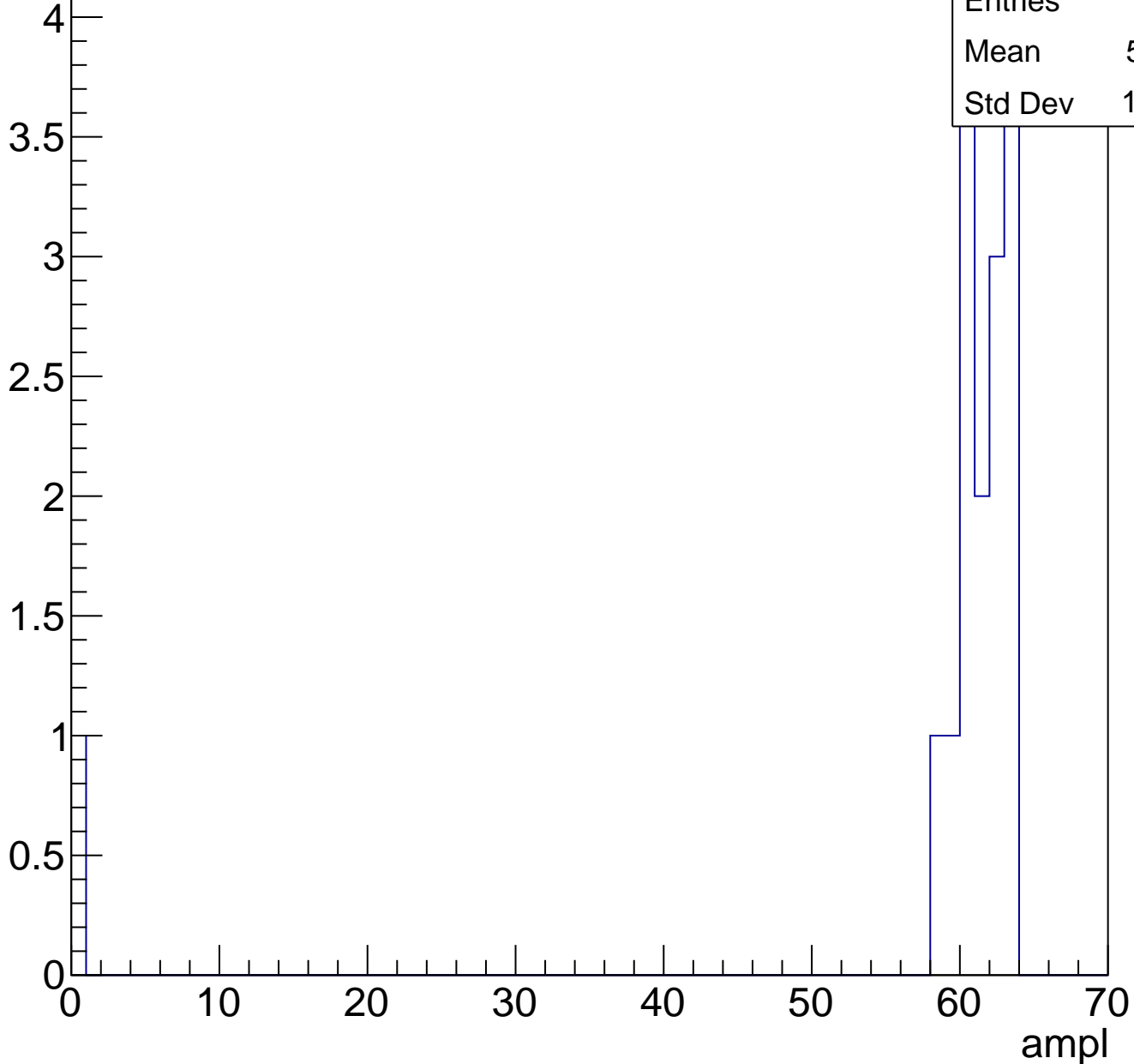
ampl



# B1L102S, U5-ch116, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U5-ch116, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U5-ch117, adc0

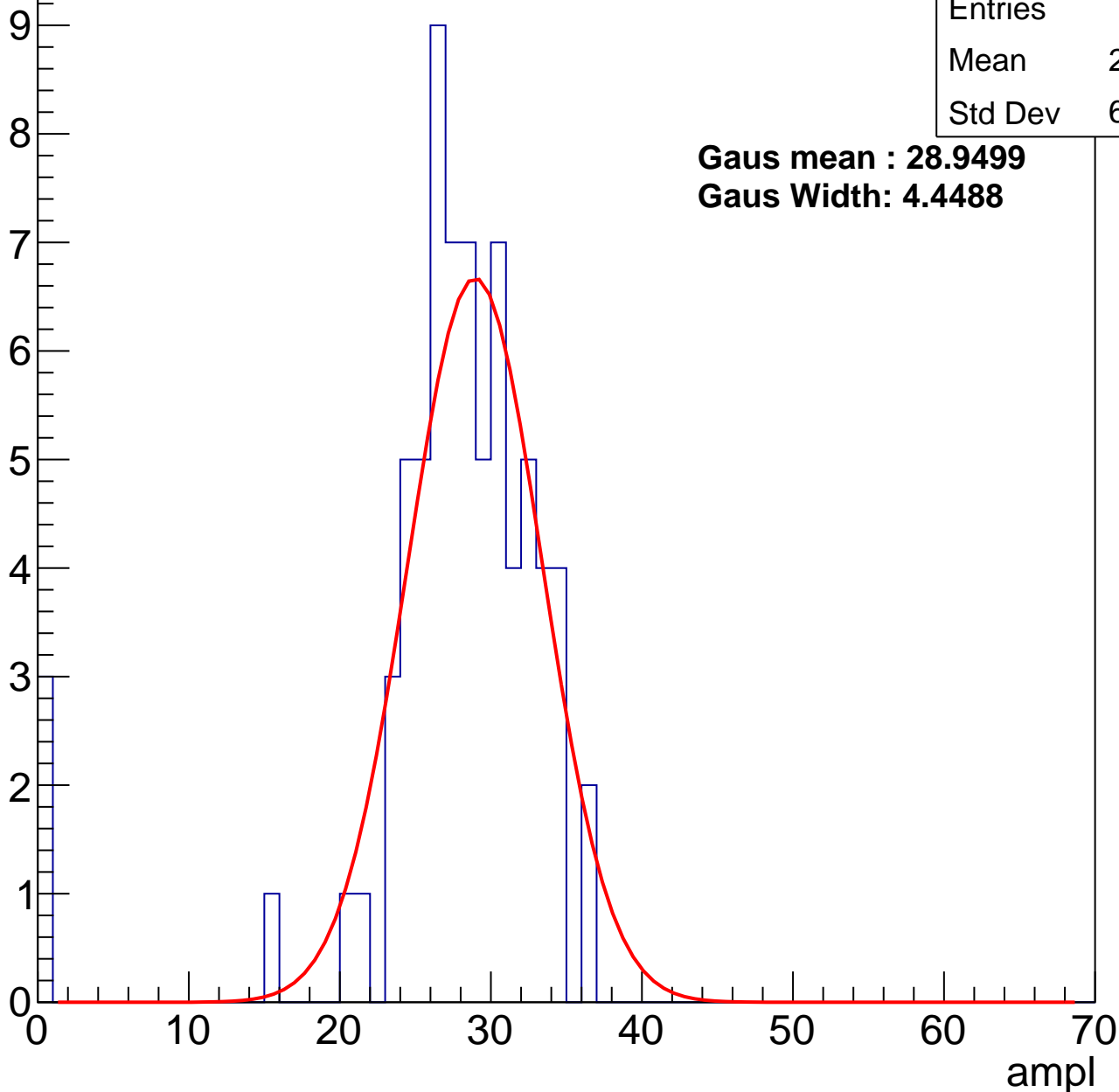
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	26.96
Std Dev	6.743

**Gaus mean : 28.9499**

**Gaus Width: 4.4488**



# B1L102S, U5-ch117, adc1

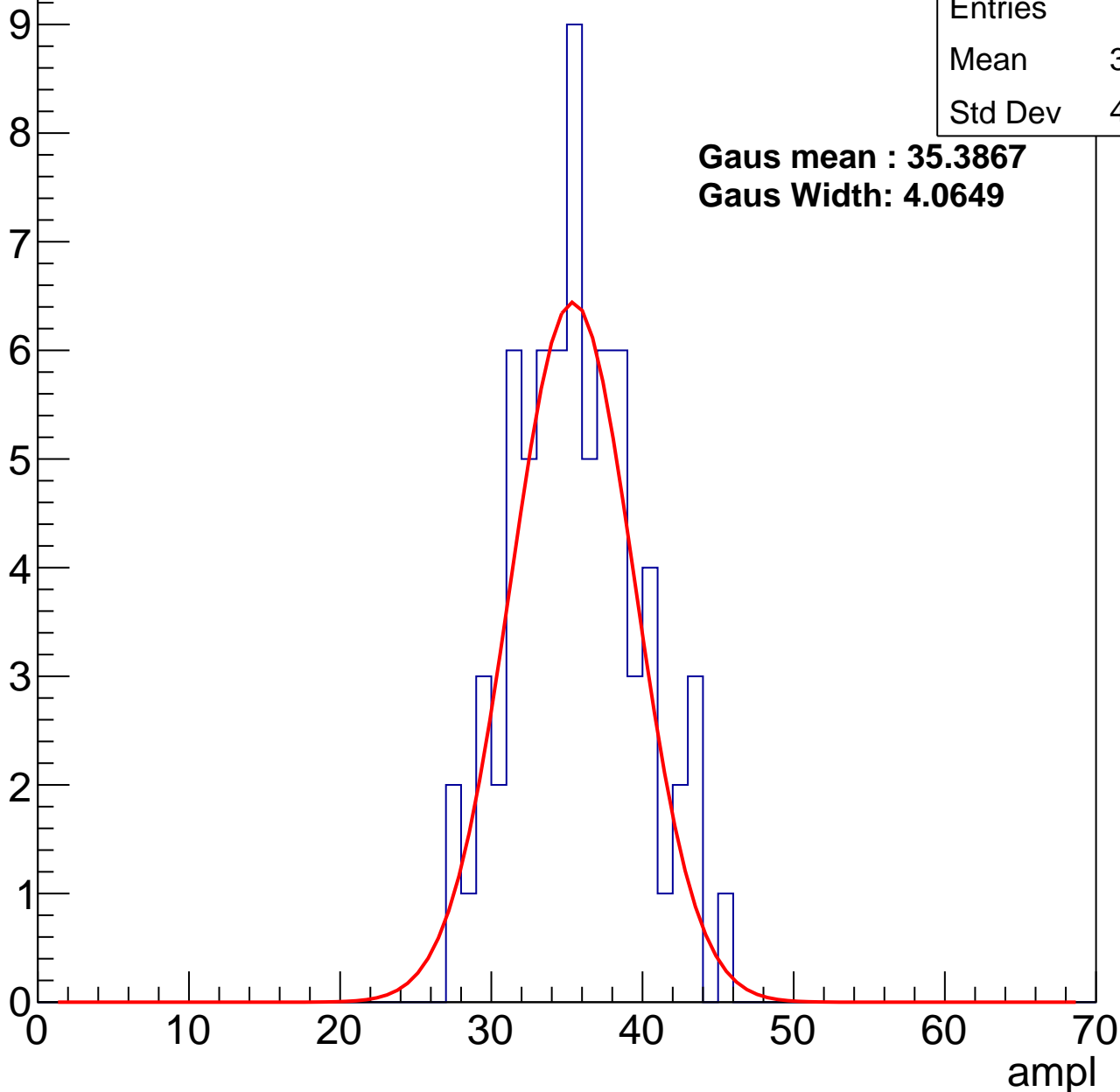
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	35.18
Std Dev	4.043

**Gaus mean : 35.3867**

**Gaus Width: 4.0649**



# B1L102S, U5-ch117, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	41.99
Std Dev	3.583

7

6

5

4

3

2

1

0

**Gaus mean : 42.4033**

**Gaus Width: 4.0383**

0

1

2

3

4

5

6

7

8

9

10

11

12

13

14

15

16

17

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20

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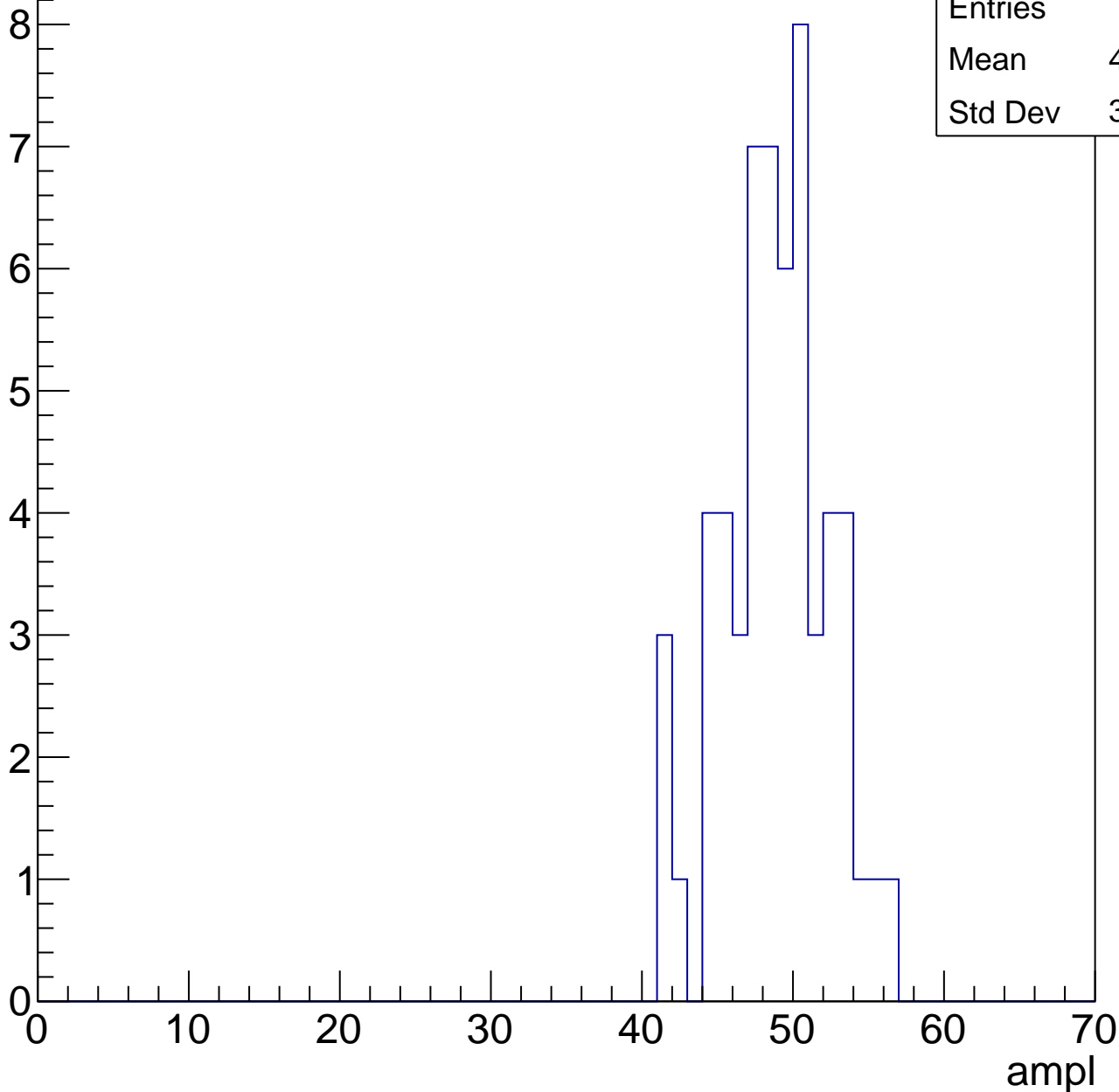
321

# B1L102S, U5-ch117, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	48.35
Std Dev	3.436

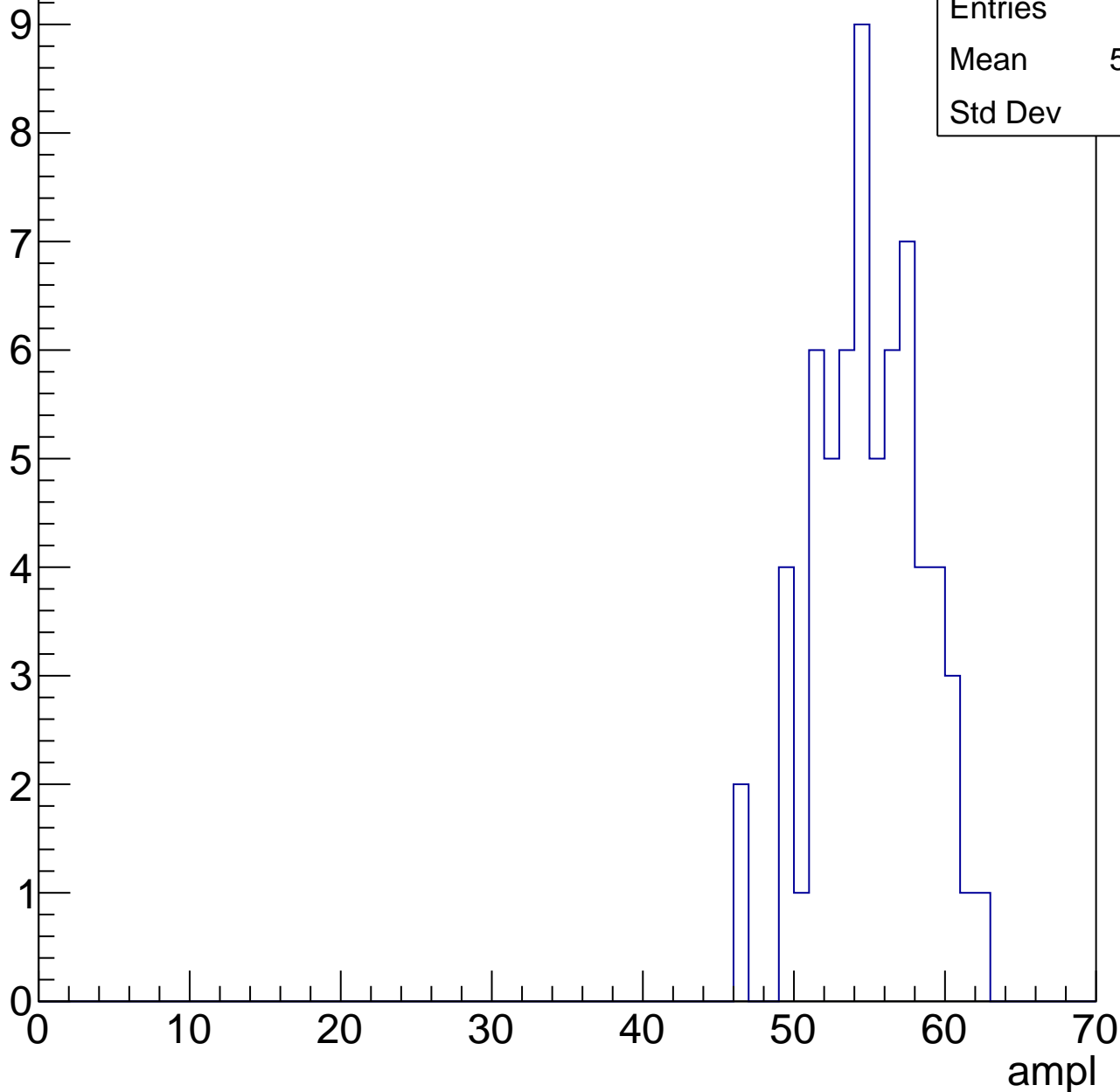


# B1L102S, U5-ch117, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	54.52
Std Dev	3.5

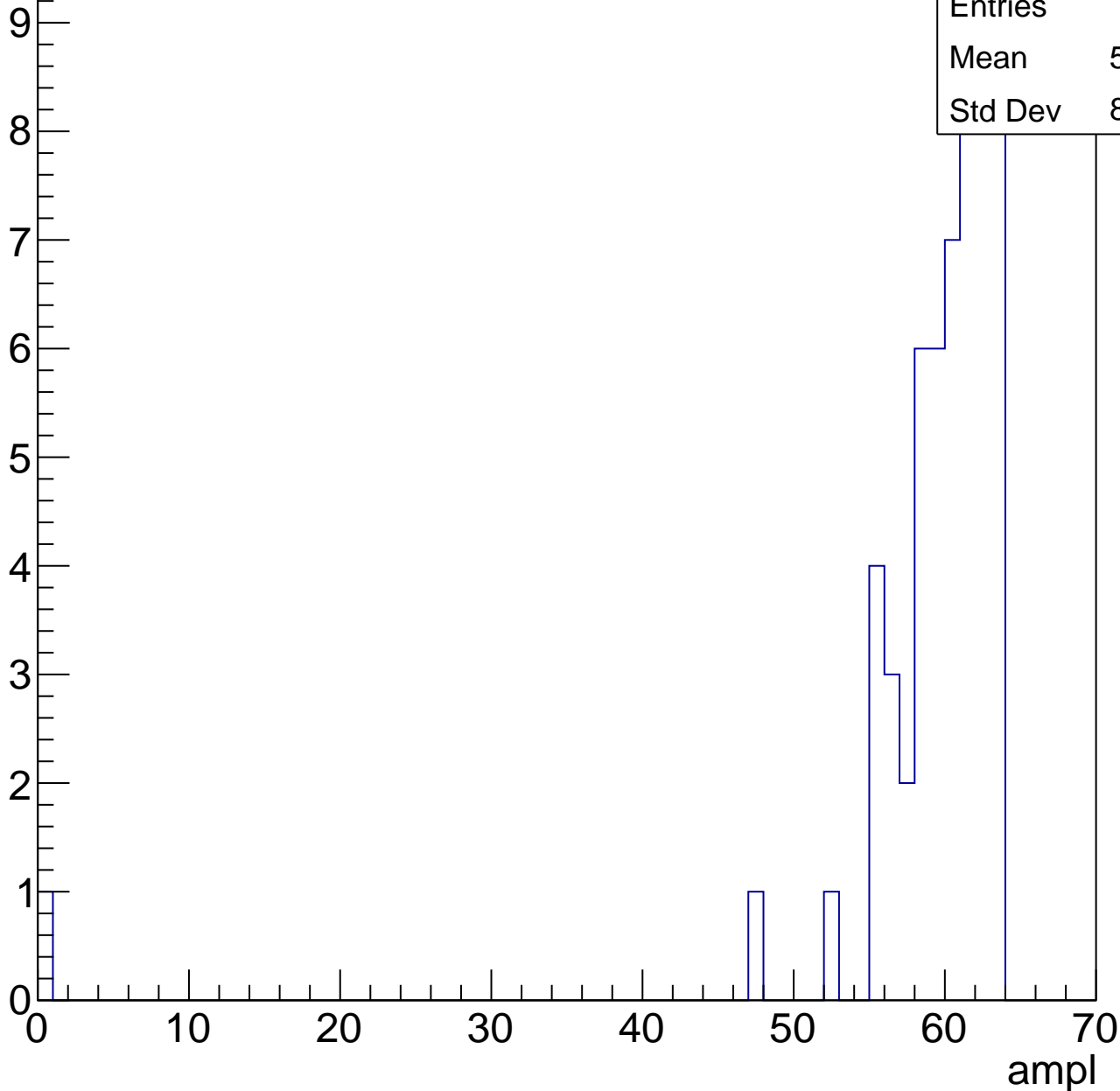


# B1L102S, U5-ch117, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	58.49
Std Dev	8.394



# B1L102S, U5-ch117, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

2

Mean

60

Std Dev

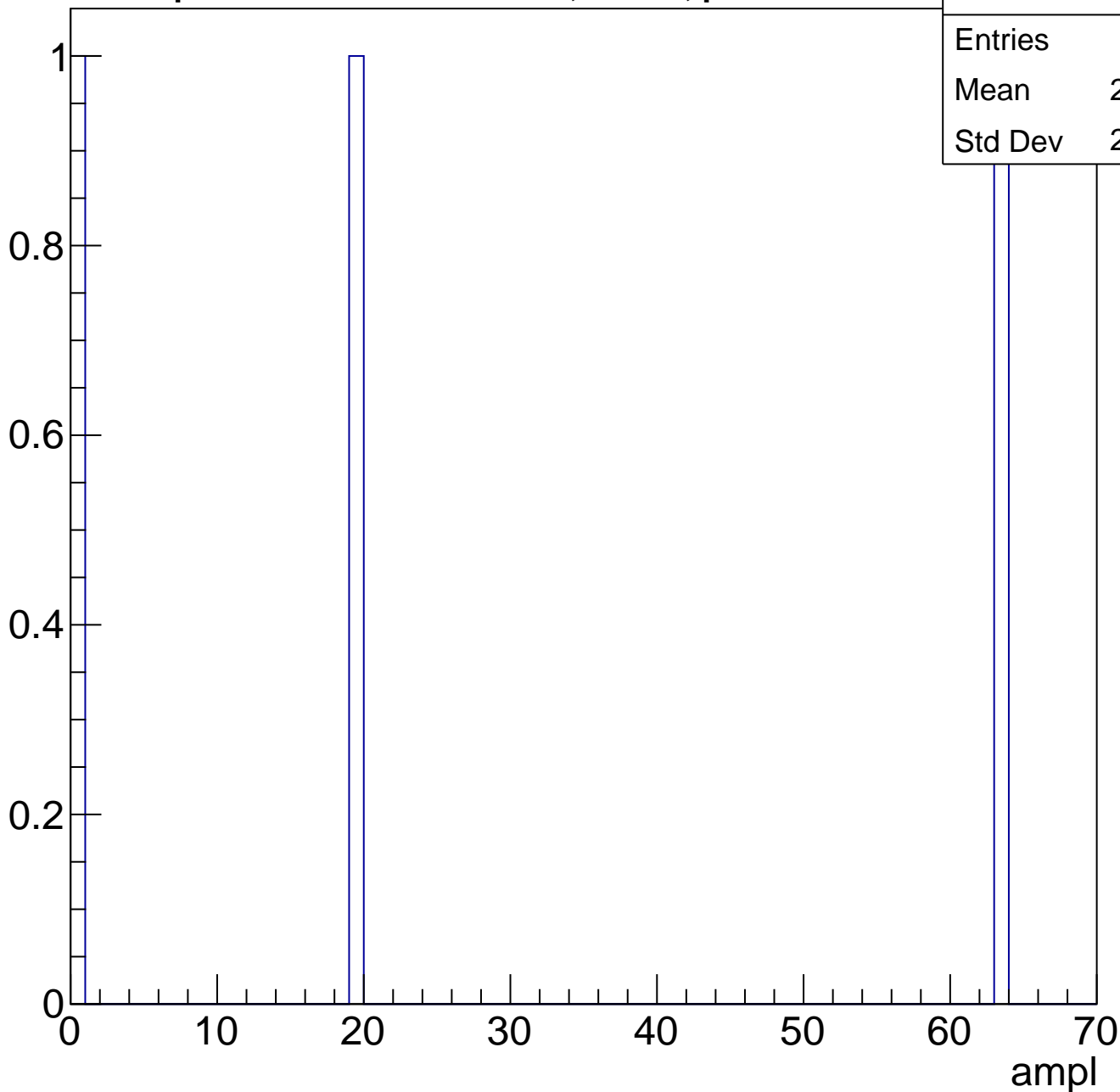
3



# B1L102S, U5-ch117, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	3
Mean	27.33
Std Dev	26.39

# B1L102S, U5-ch118, adc0

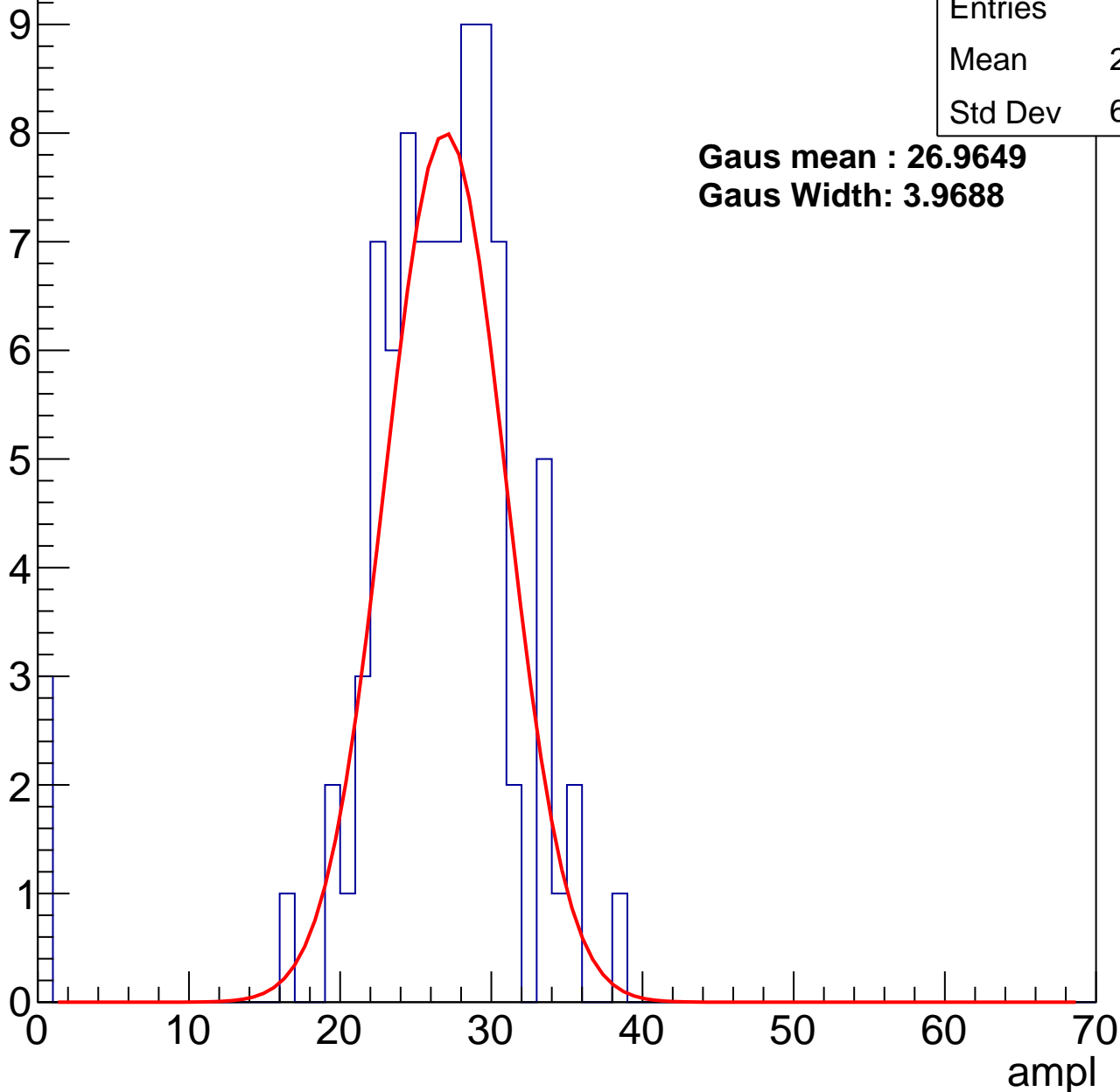
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	88
Mean	25.67
Std Dev	6.246

**Gaus mean : 26.9649**

**Gaus Width: 3.9688**



# B1L102S, U5-ch118, adc1

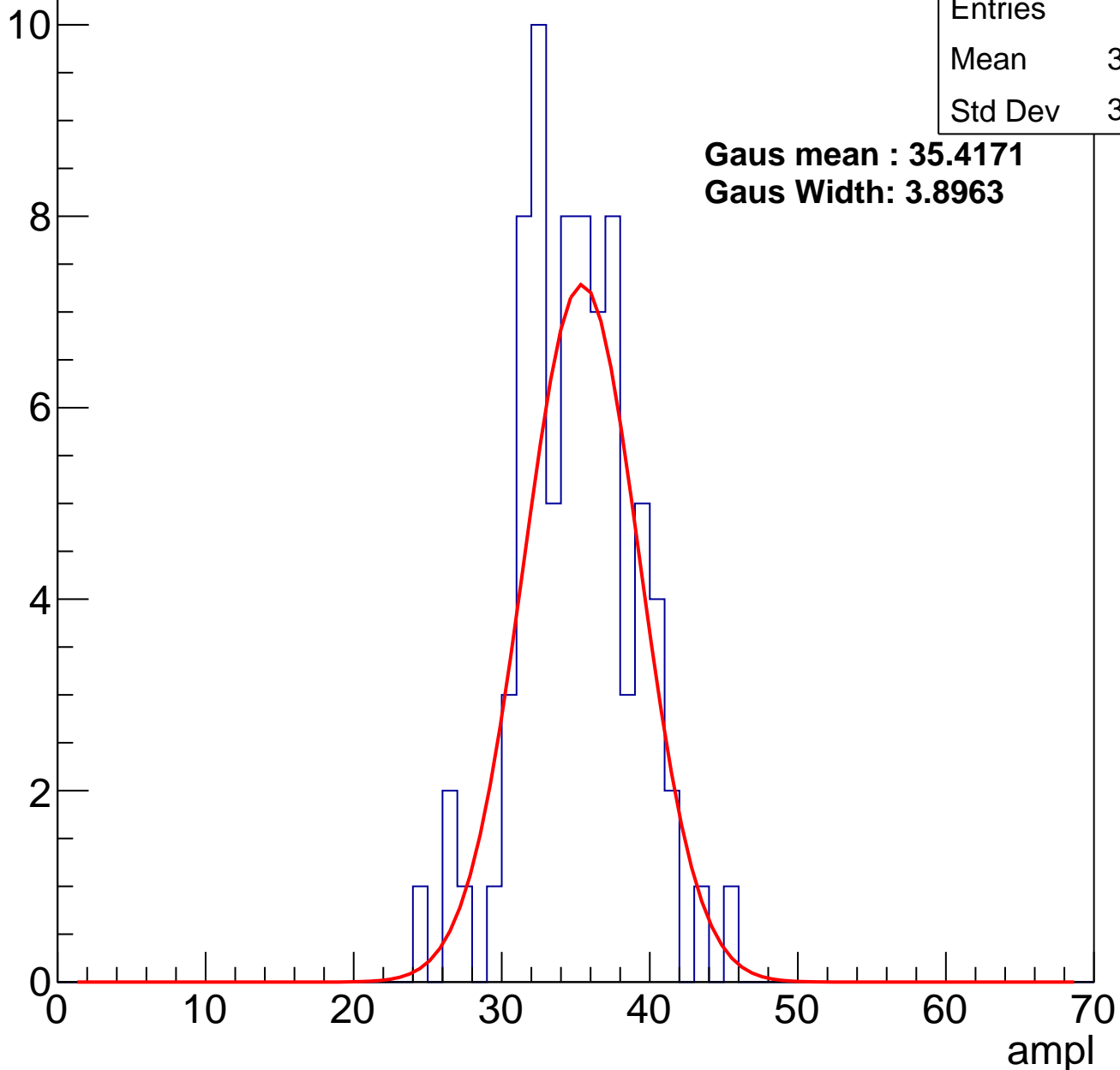
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	78
Mean	34.54
Std Dev	3.872

**Gaus mean : 35.4171**

**Gaus Width: 3.8963**

Entry



# B1L102S, U5-ch118, adc2

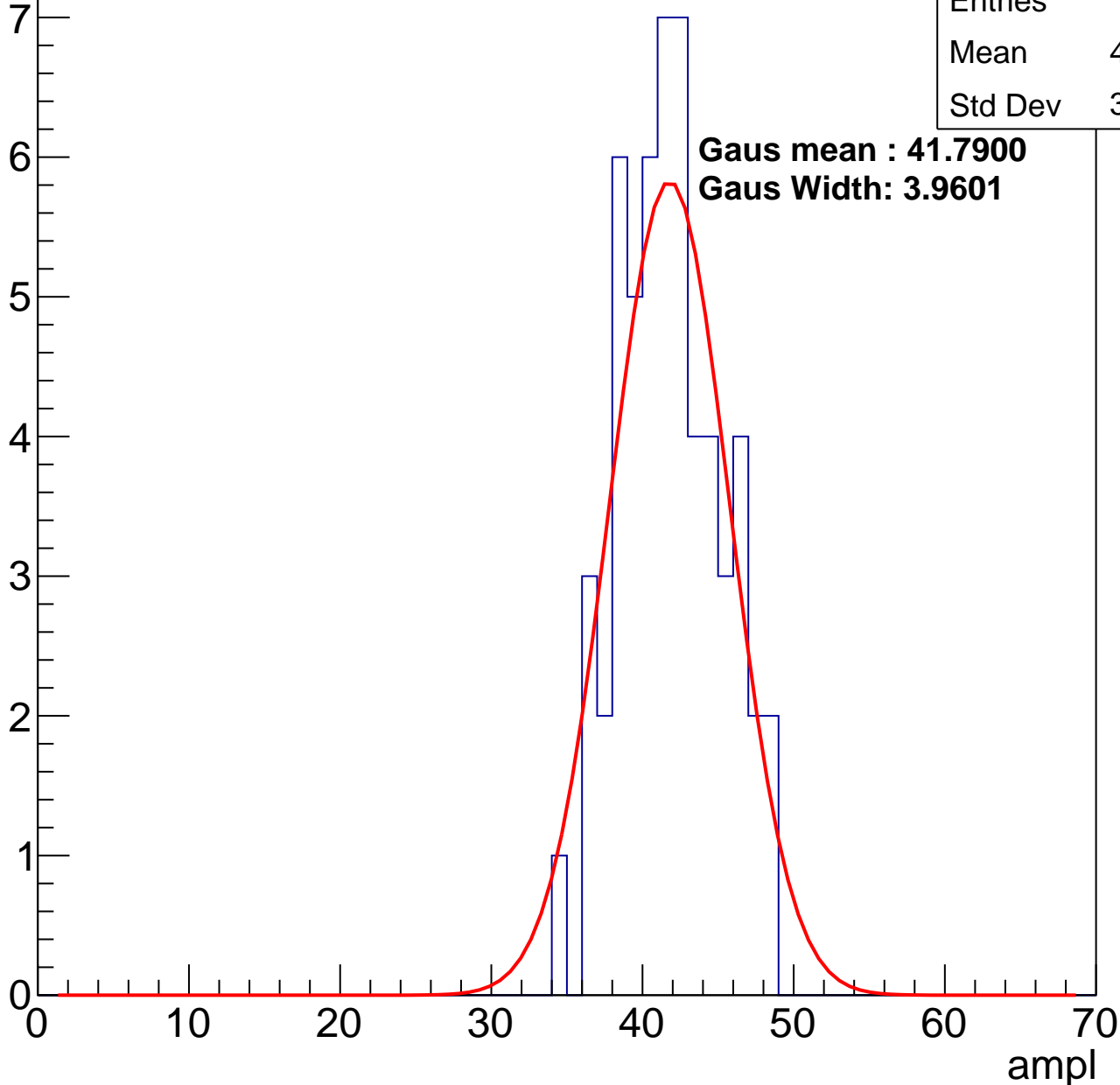
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	41.38
Std Dev	3.287

**Gaus mean : 41.7900**

**Gaus Width: 3.9601**

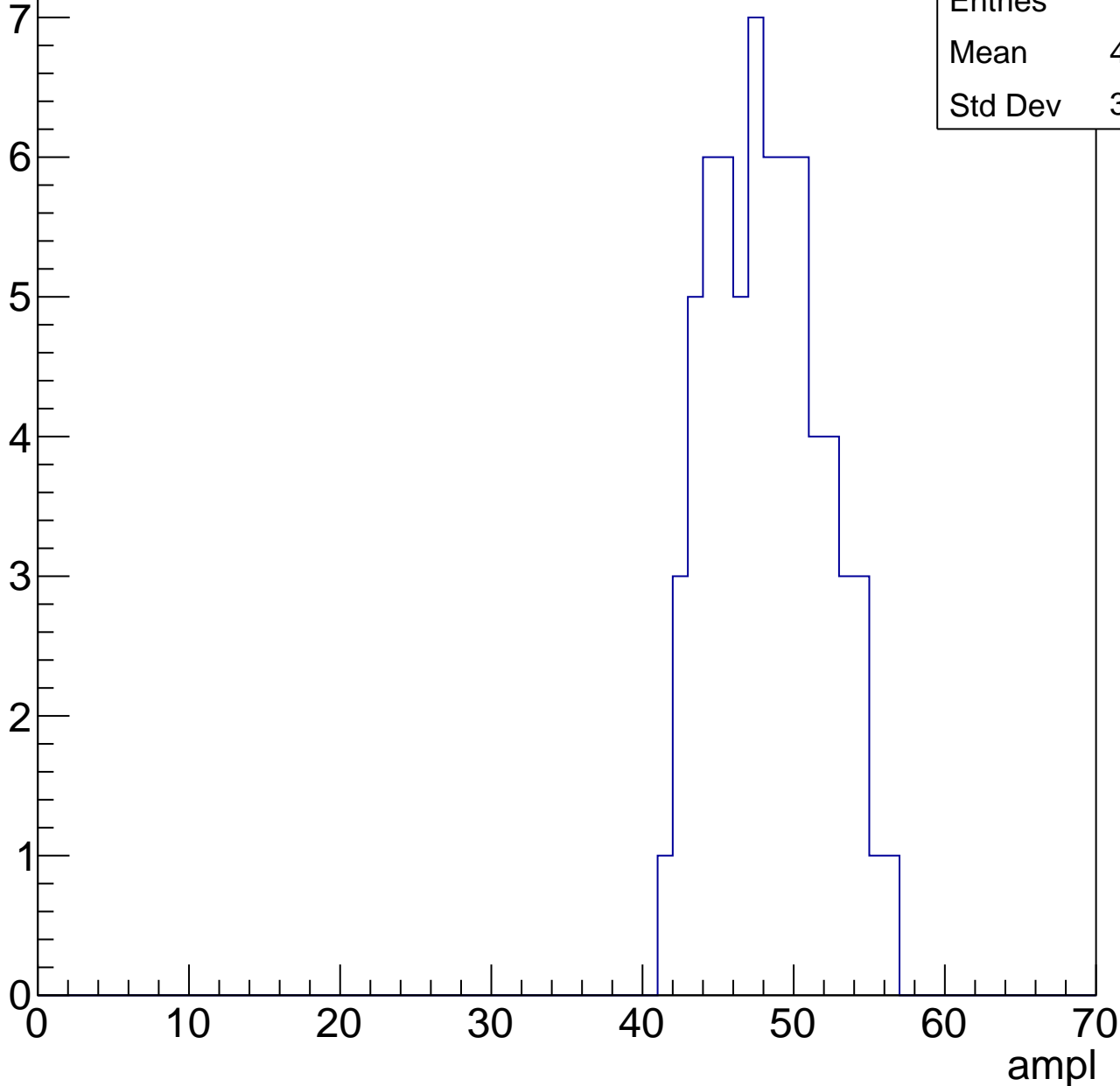


# B1L102S, U5-ch118, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	47.78
Std Dev	3.628

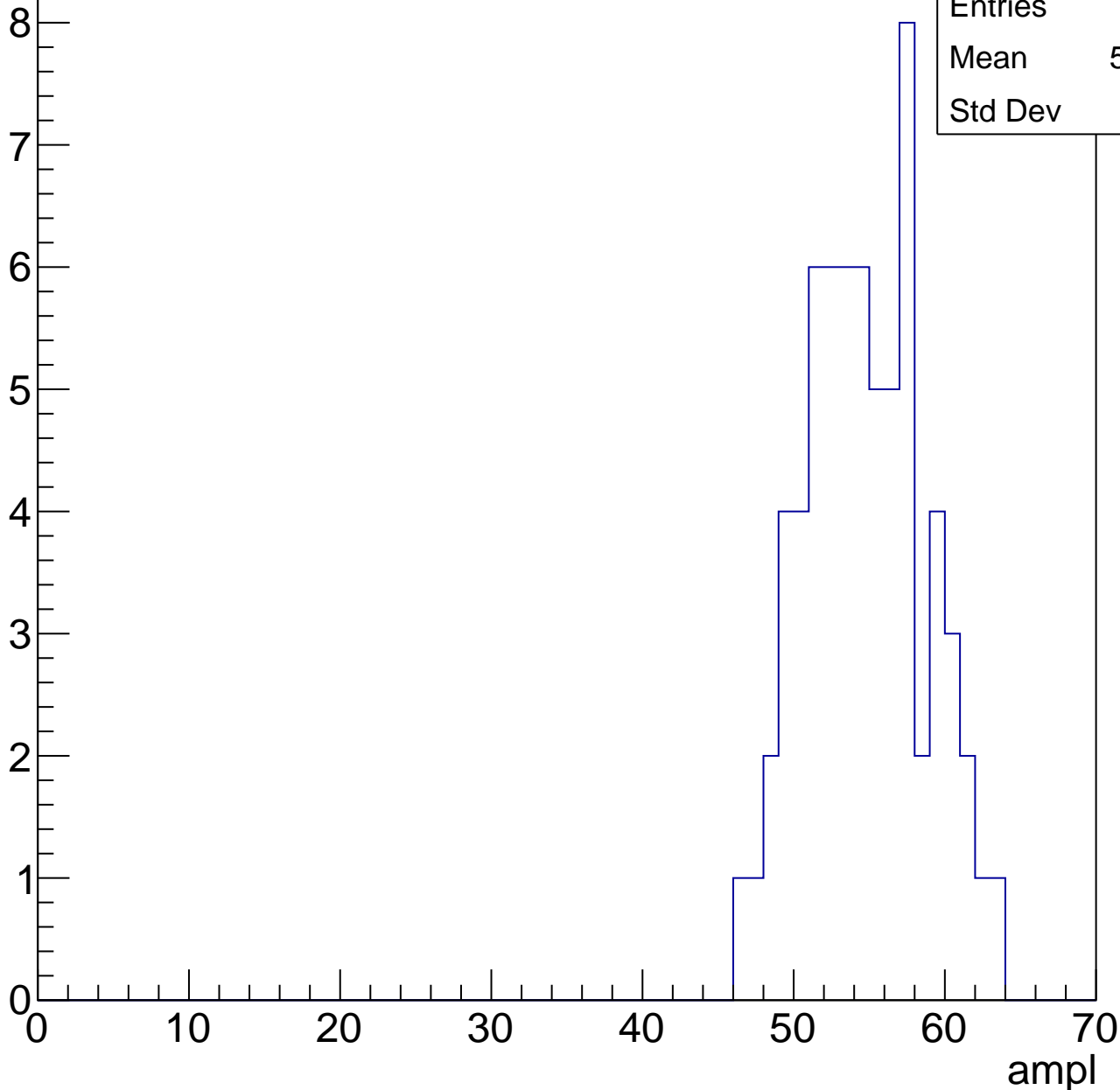


# B1L102S, U5-ch118, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

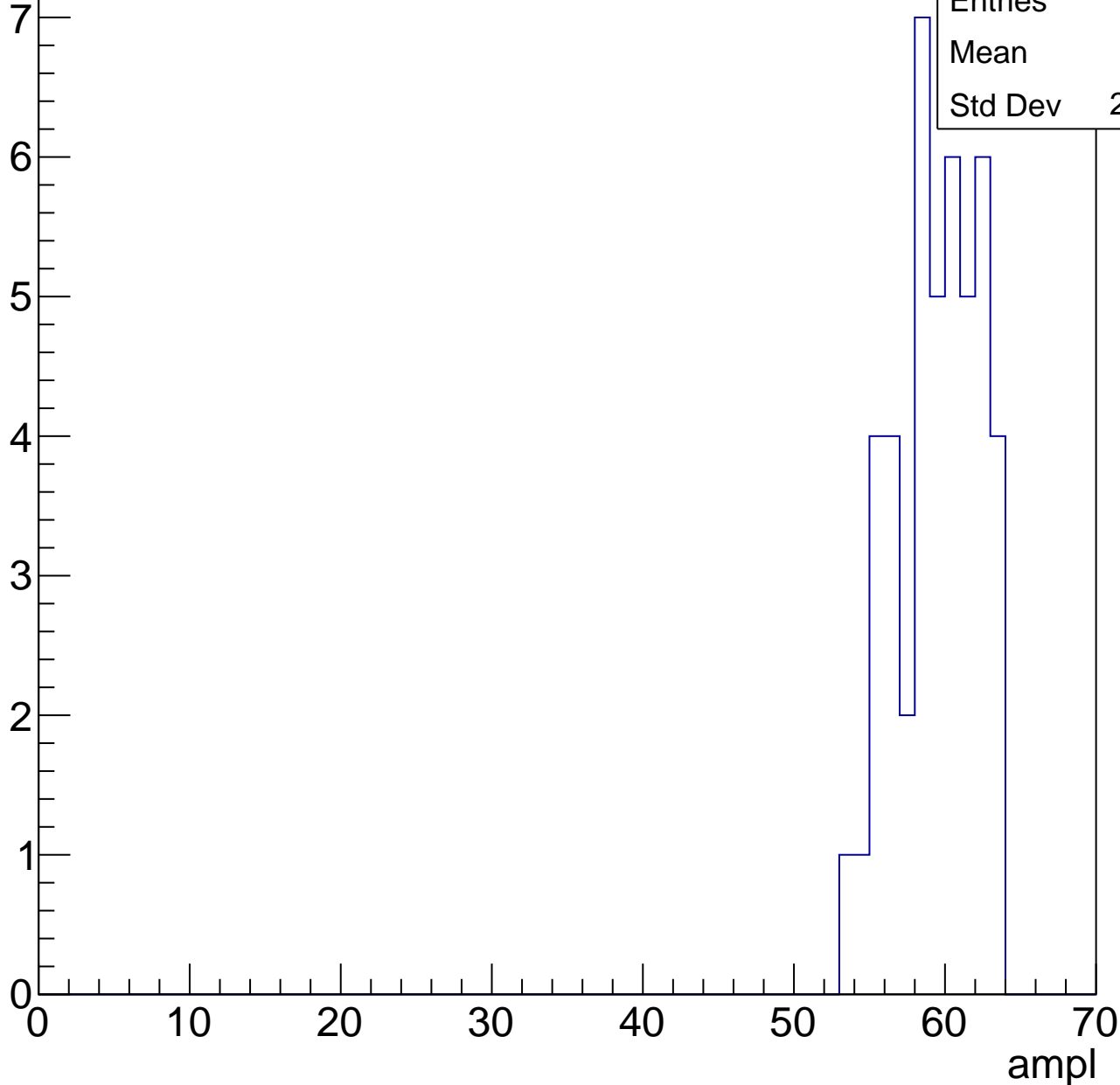
Entries	67
Mean	54.25
Std Dev	3.88



# B1L102S, U5-ch118, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

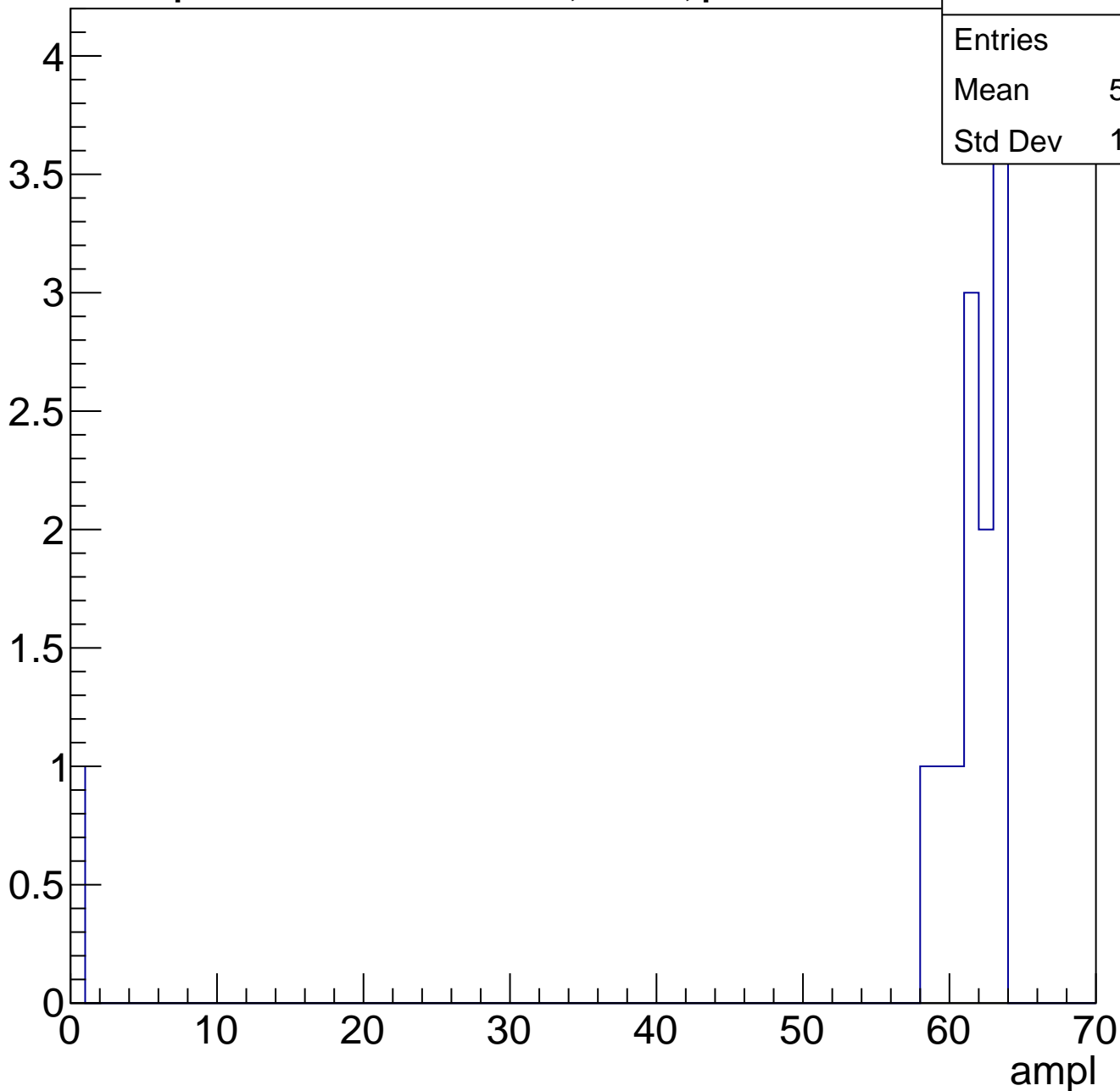
Entry



# B1L102S, U5-ch118, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

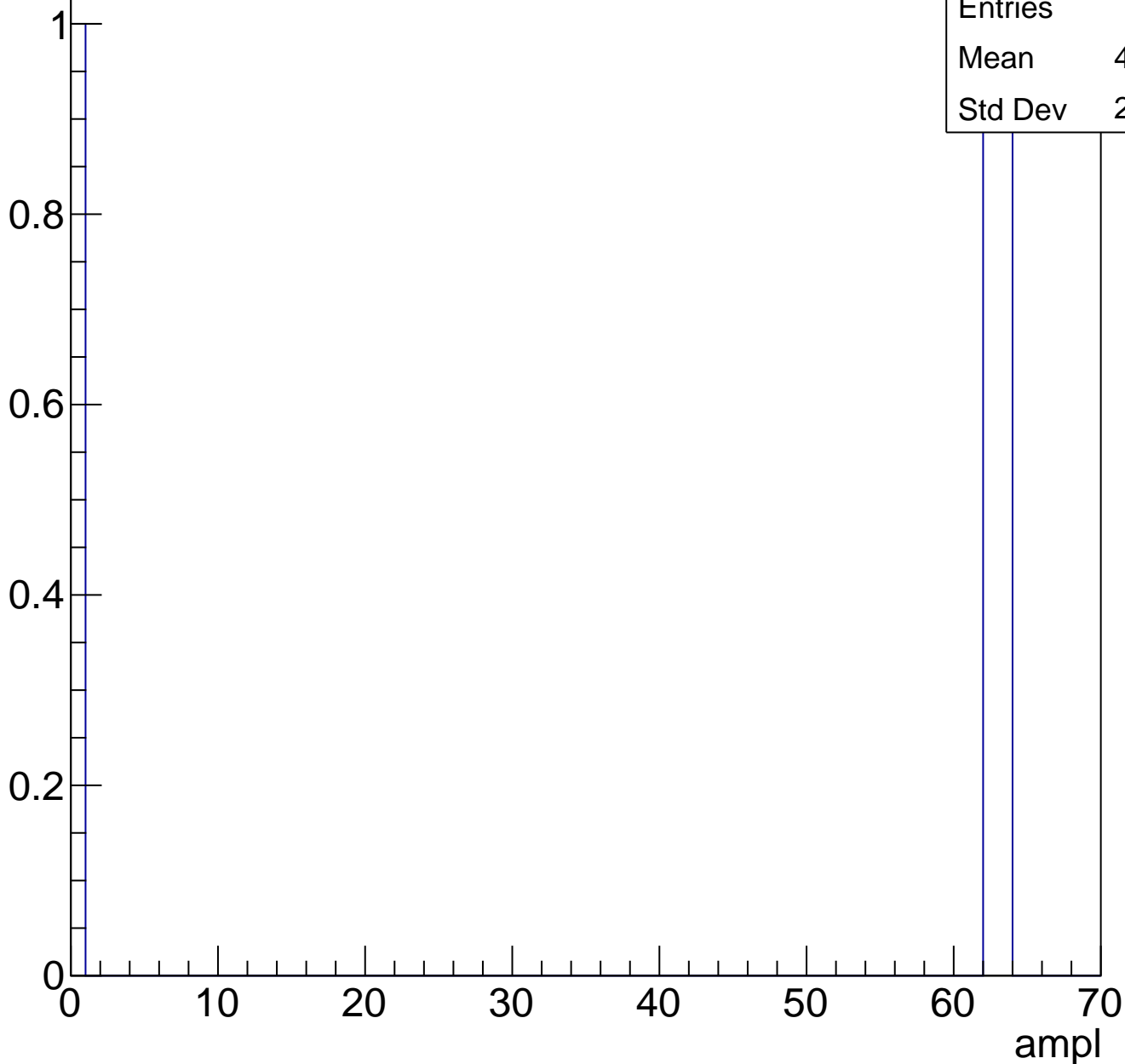




# B1L102S, U5-ch118, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U5-ch119, adc0

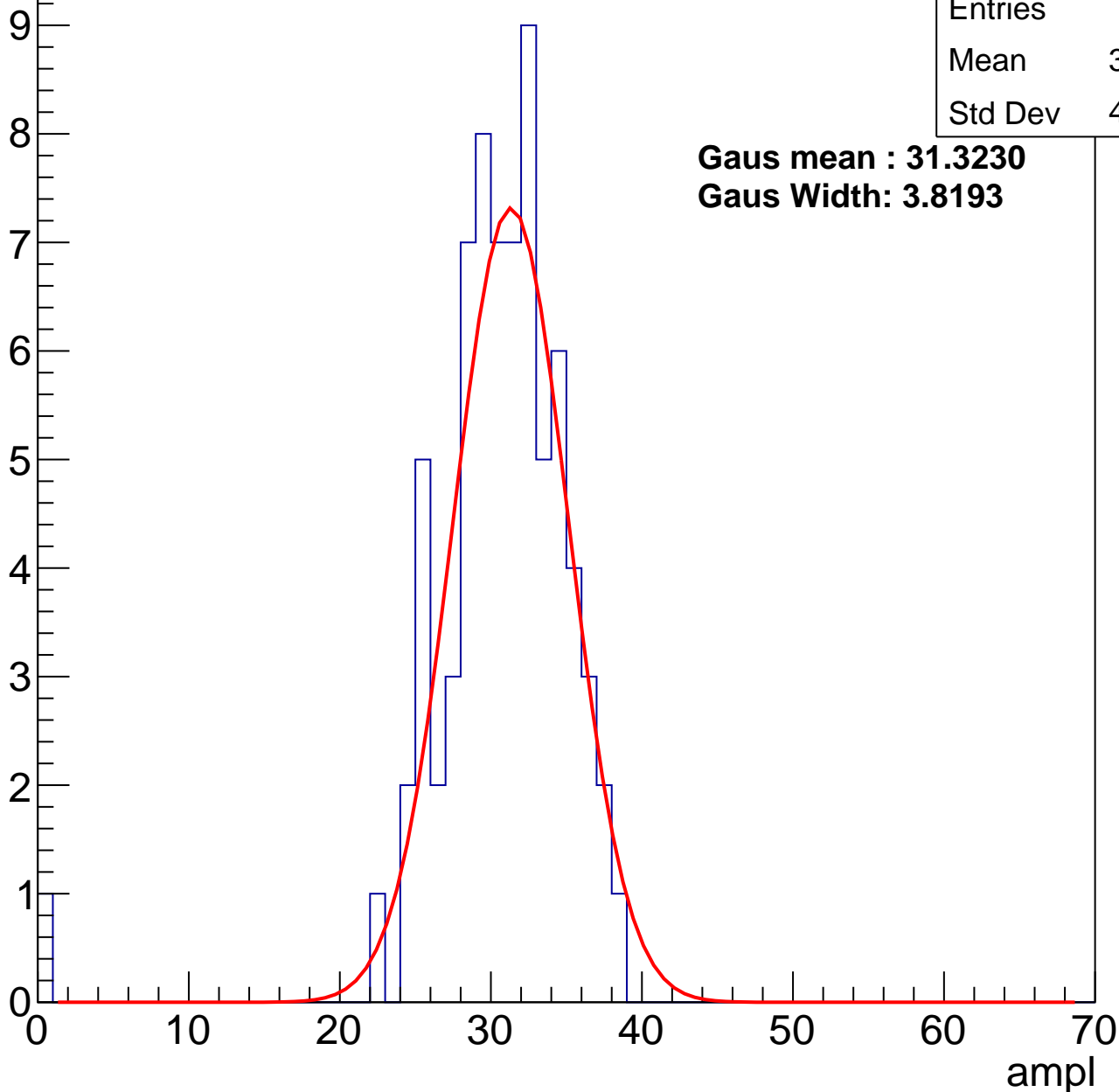
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	30.14
Std Dev	4.978

**Gaus mean : 31.3230**

**Gaus Width: 3.8193**



# B1L102S, U5-ch119, adc1

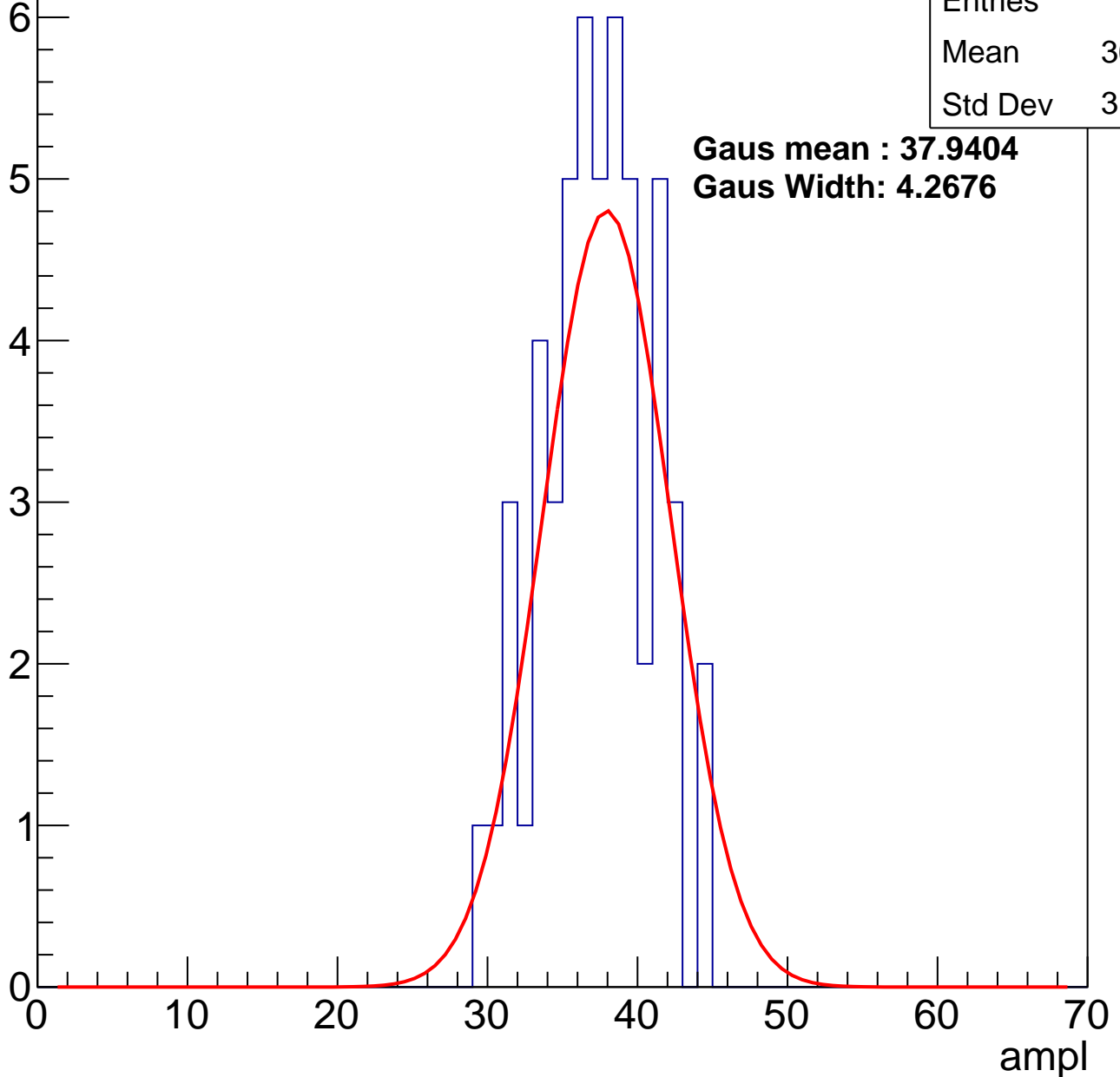
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	36.85
Std Dev	3.559

**Gaus mean : 37.9404**

**Gaus Width: 4.2676**



# B1L102S, U5-ch119, adc2

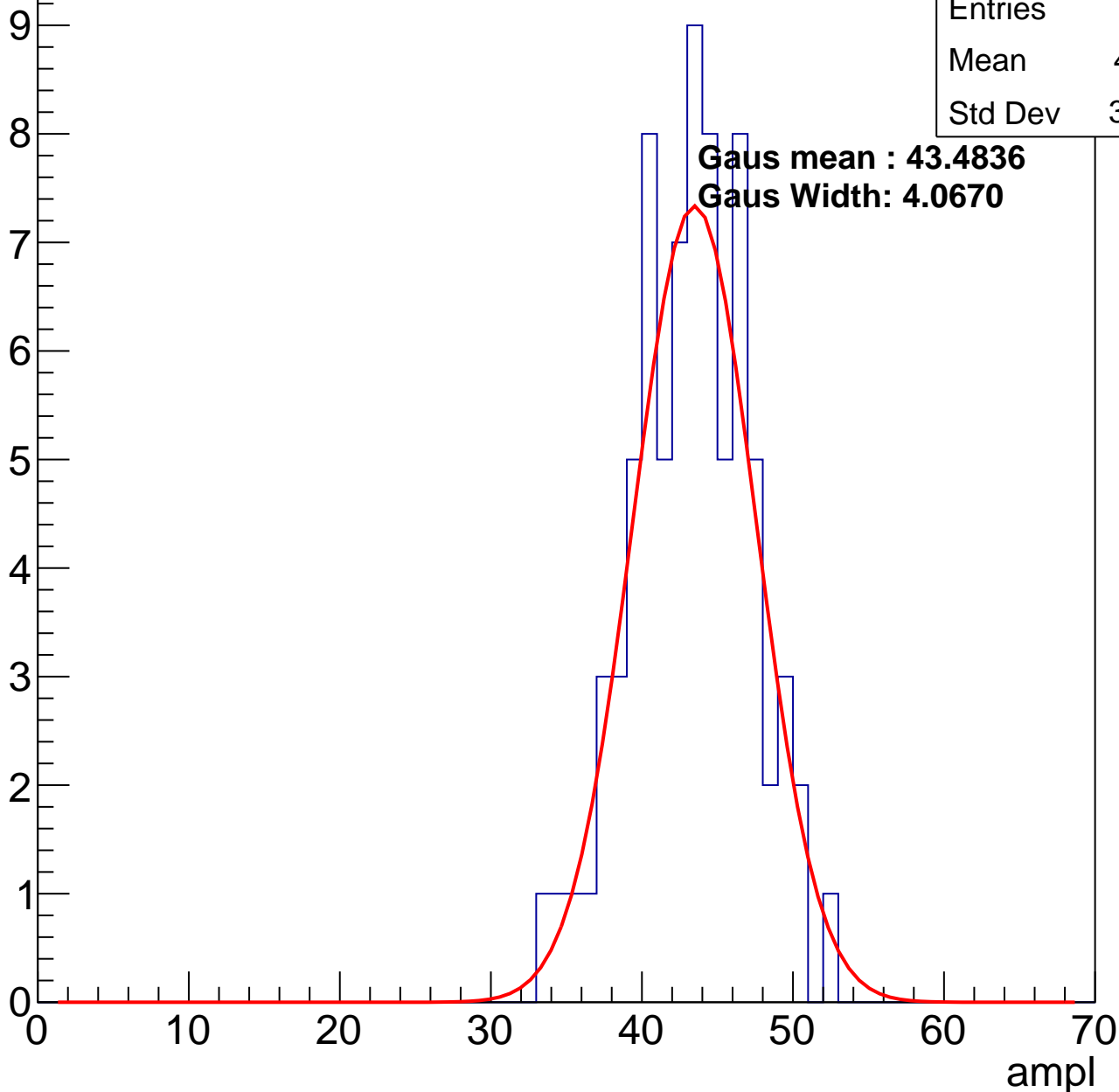
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	78
Mean	42.81
Std Dev	3.873

**Gaus mean : 43.4836**

**Gaus Width: 4.0670**

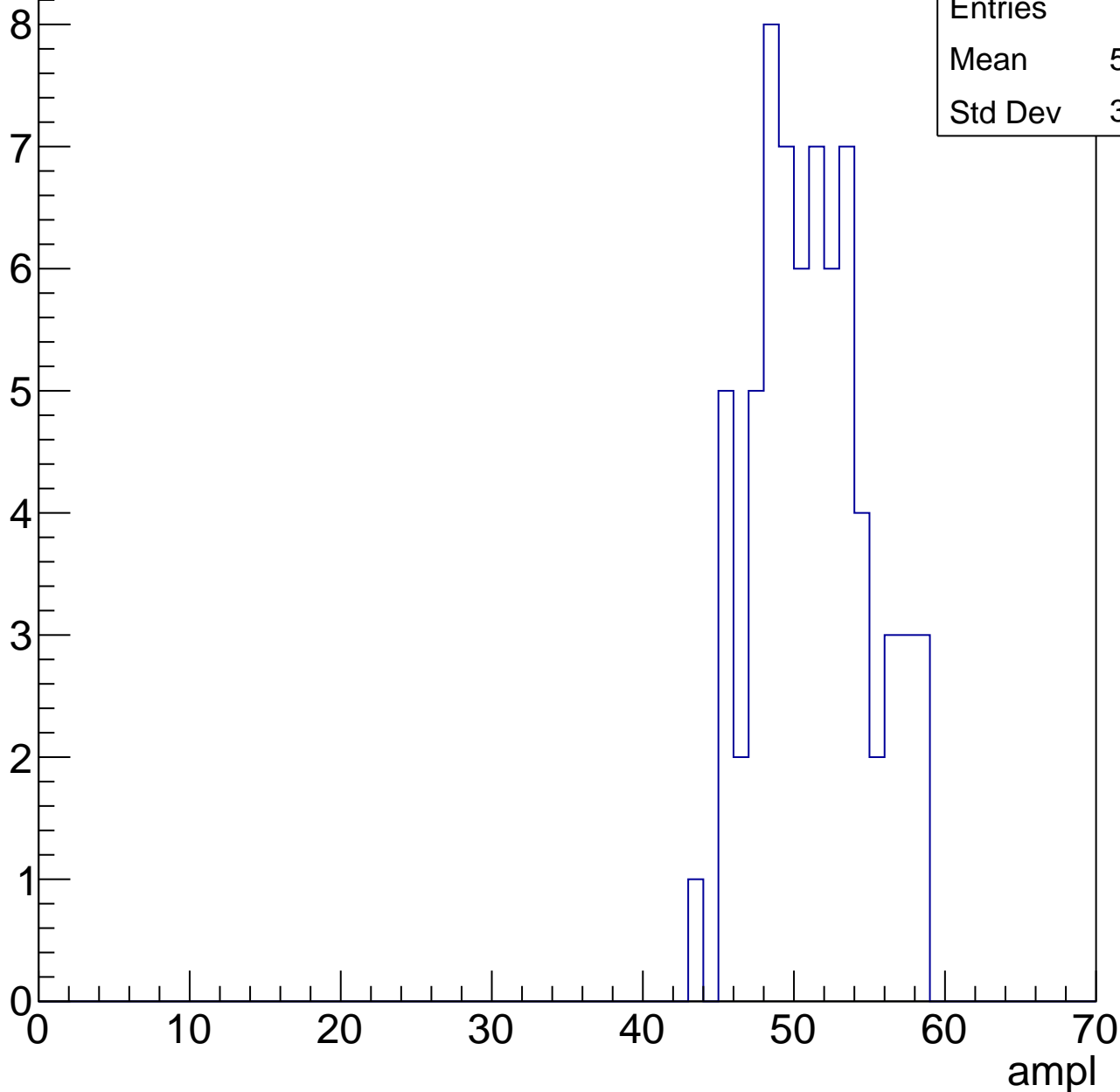


# B1L102S, U5-ch119, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	50.74
Std Dev	3.626

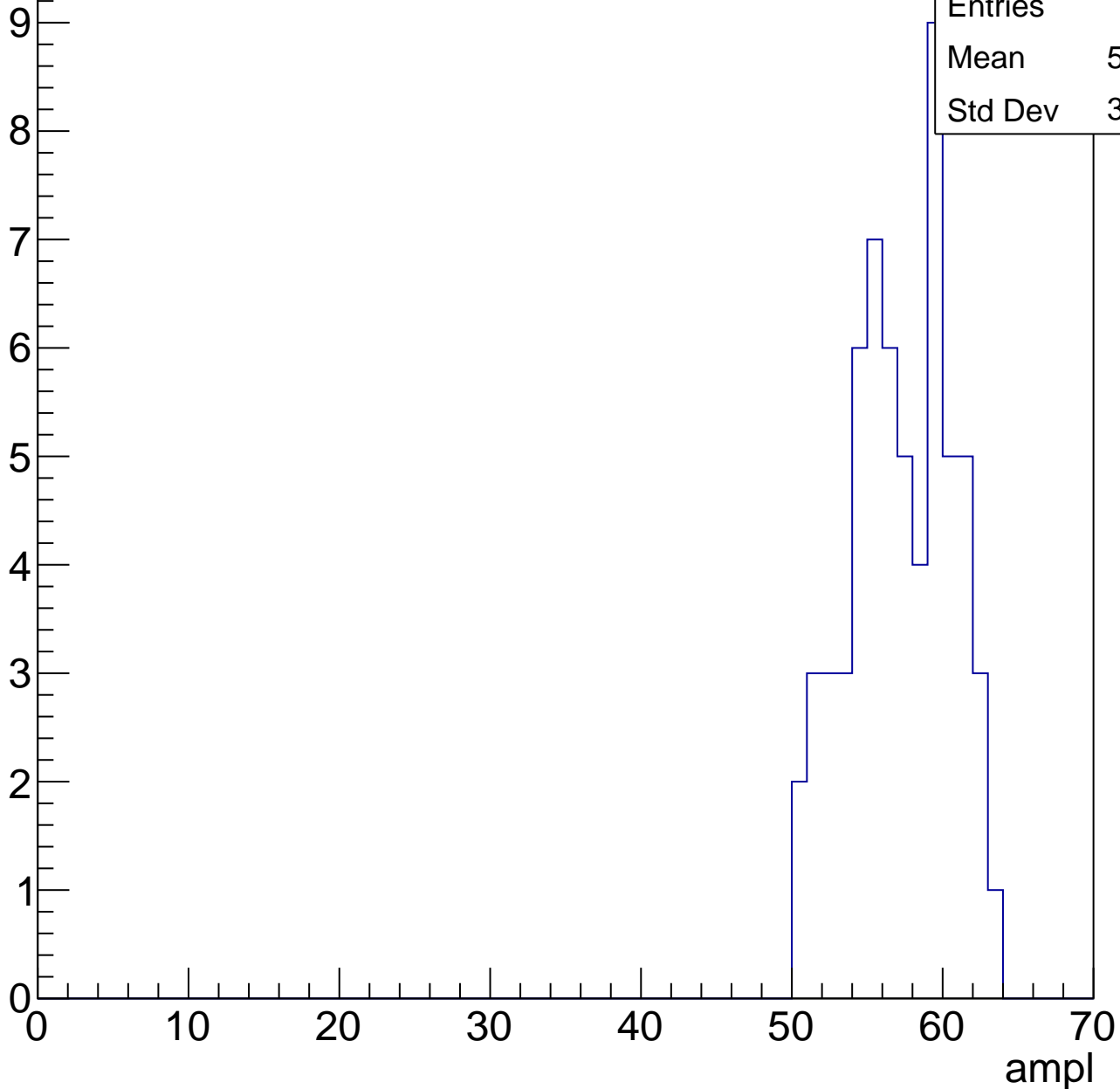


# B1L102S, U5-ch119, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	56.69
Std Dev	3.329

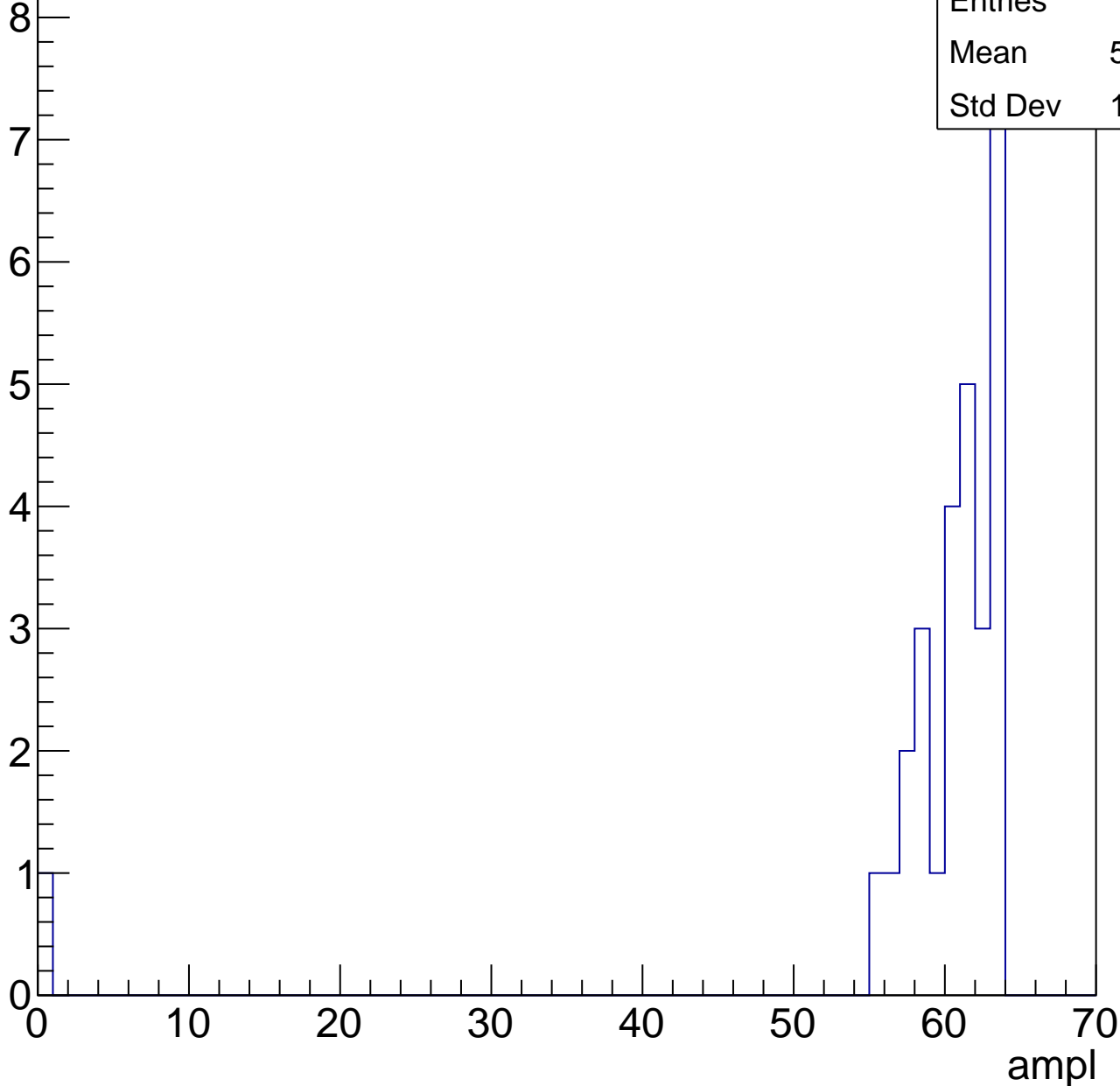


# B1L102S, U5-ch119, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

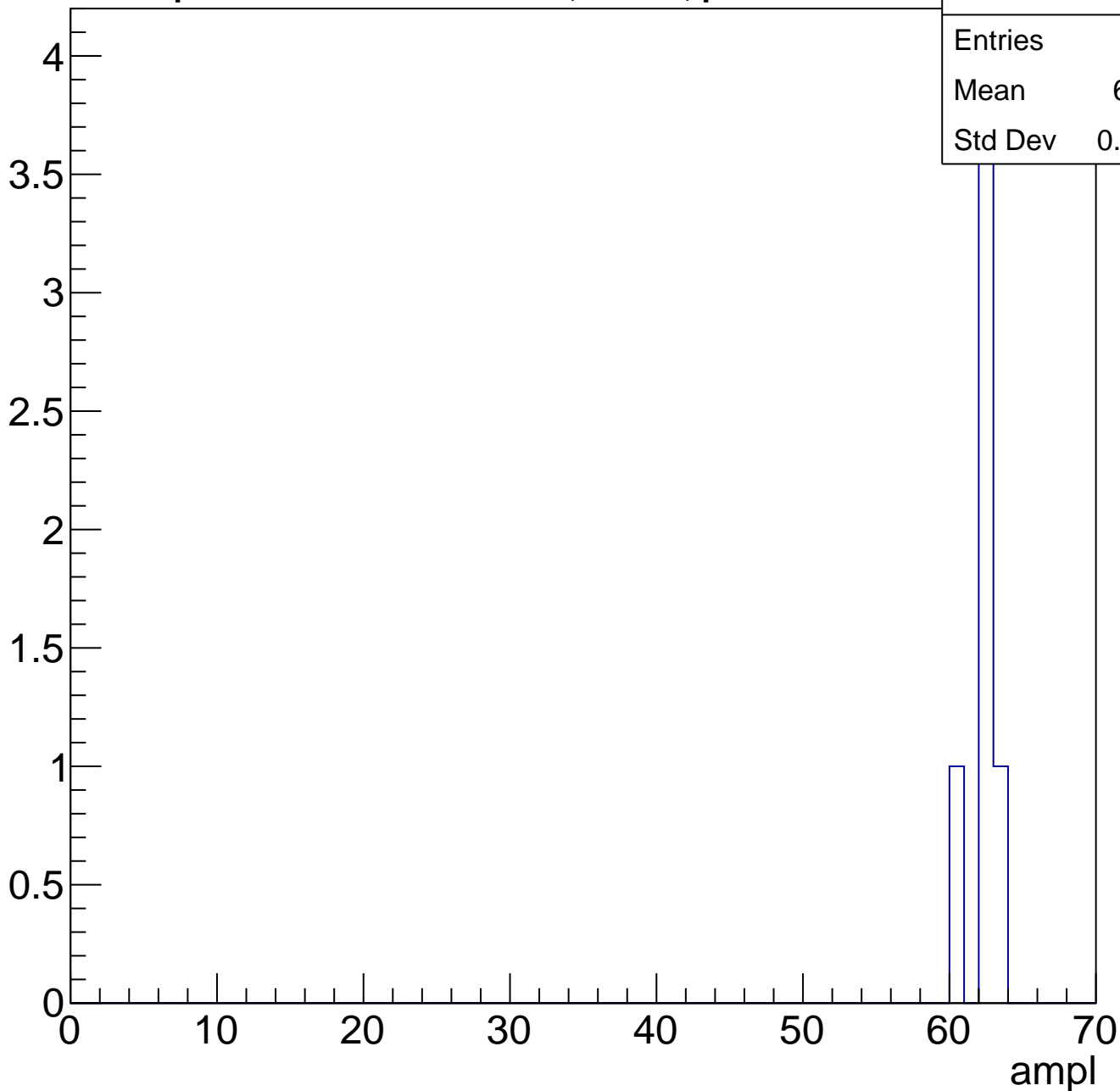
Entries	29
Mean	58.38
Std Dev	11.27



# B1L102S, U5-ch119, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U5-ch119, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L102S, U5-ch120, adc0

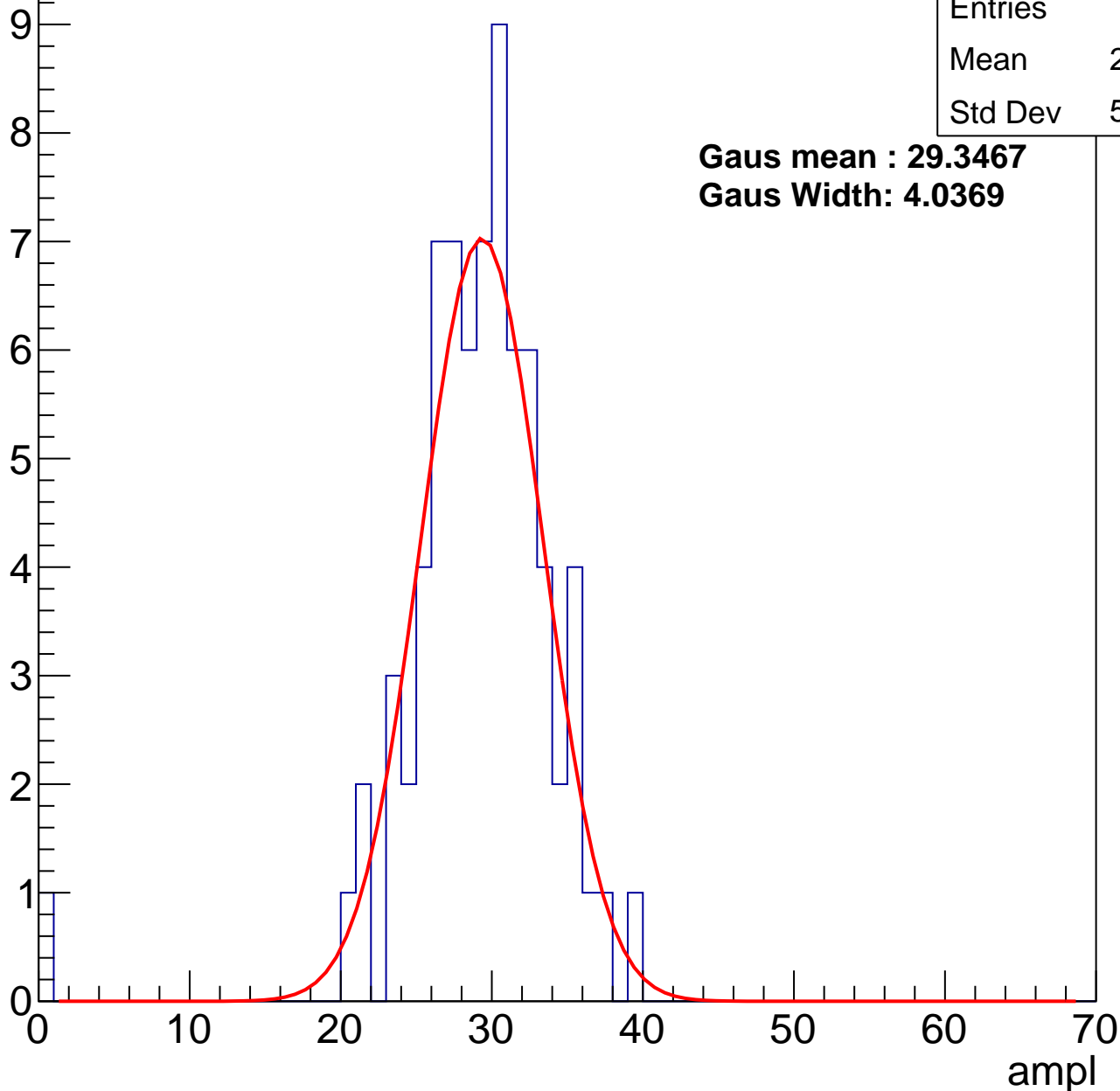
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	28.66
Std Dev	5.092

**Gaus mean : 29.3467**

**Gaus Width: 4.0369**



# B1L102S, U5-ch120, adc1

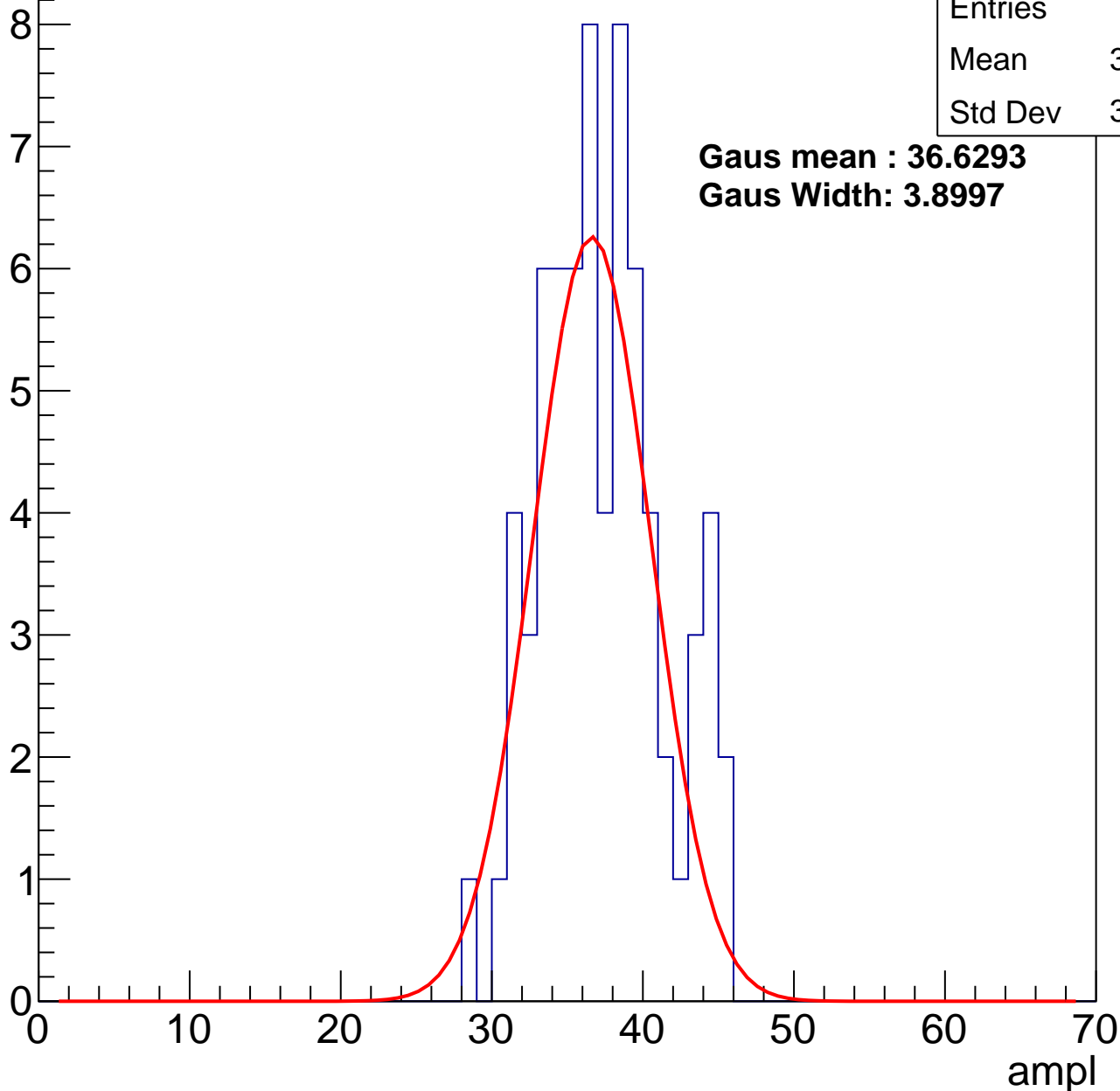
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	36.86
Std Dev	3.968

**Gaus mean : 36.6293**

**Gaus Width: 3.8997**



# B1L102S, U5-ch120, adc2

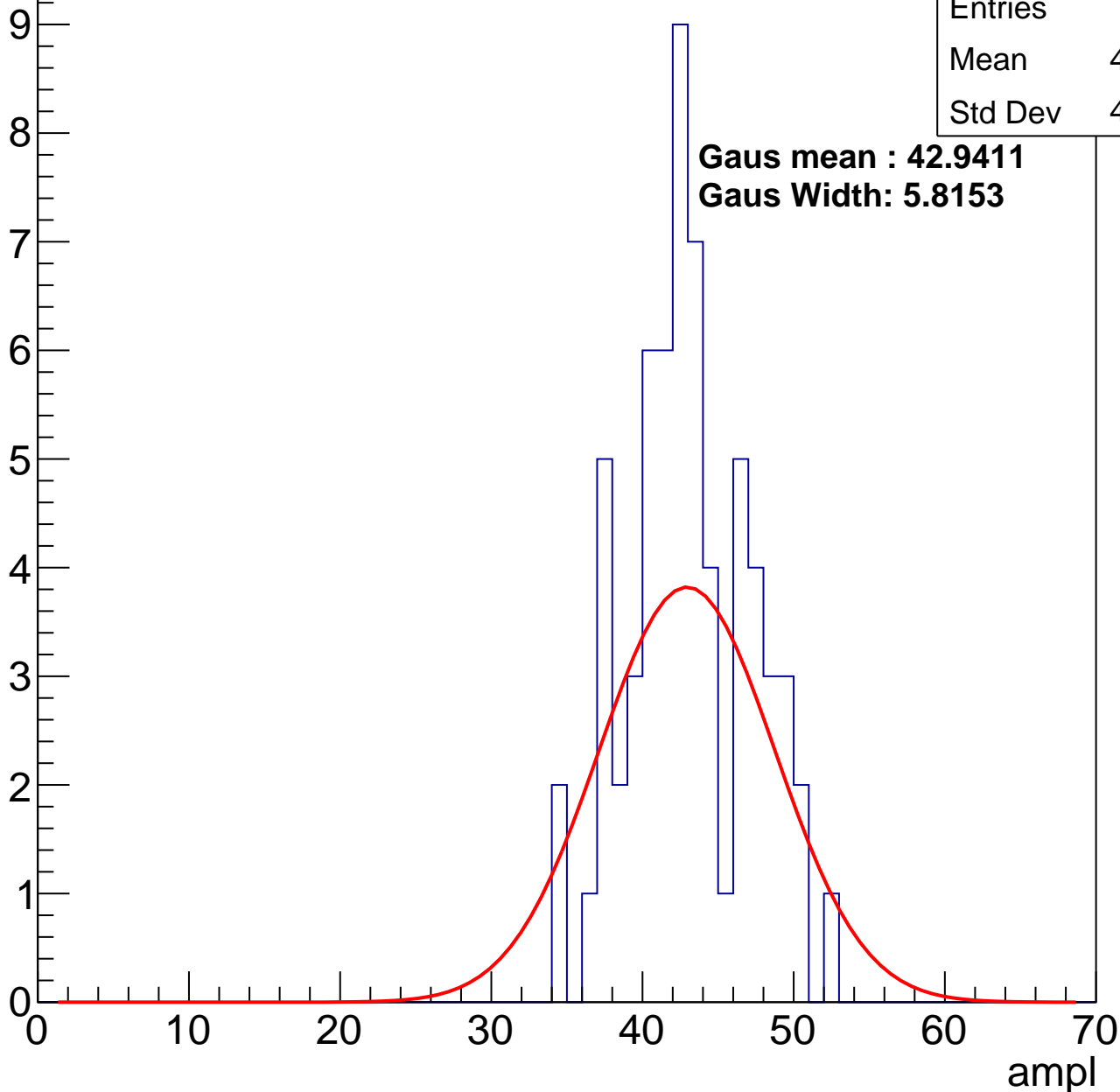
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	42.64
Std Dev	4.044

**Gaus mean : 42.9411**

**Gaus Width: 5.8153**

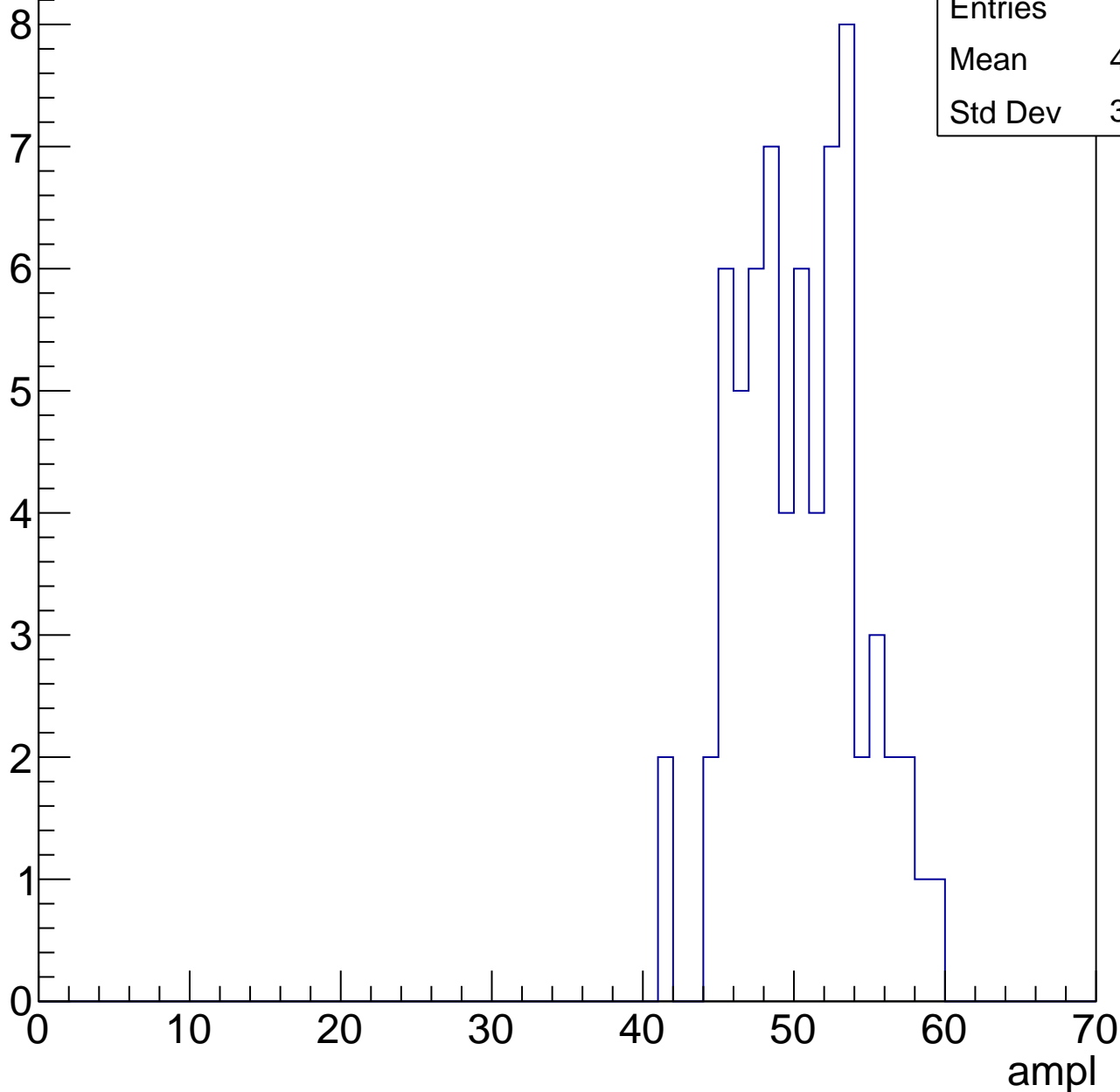


# B1L102S, U5-ch120, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	49.88
Std Dev	3.976

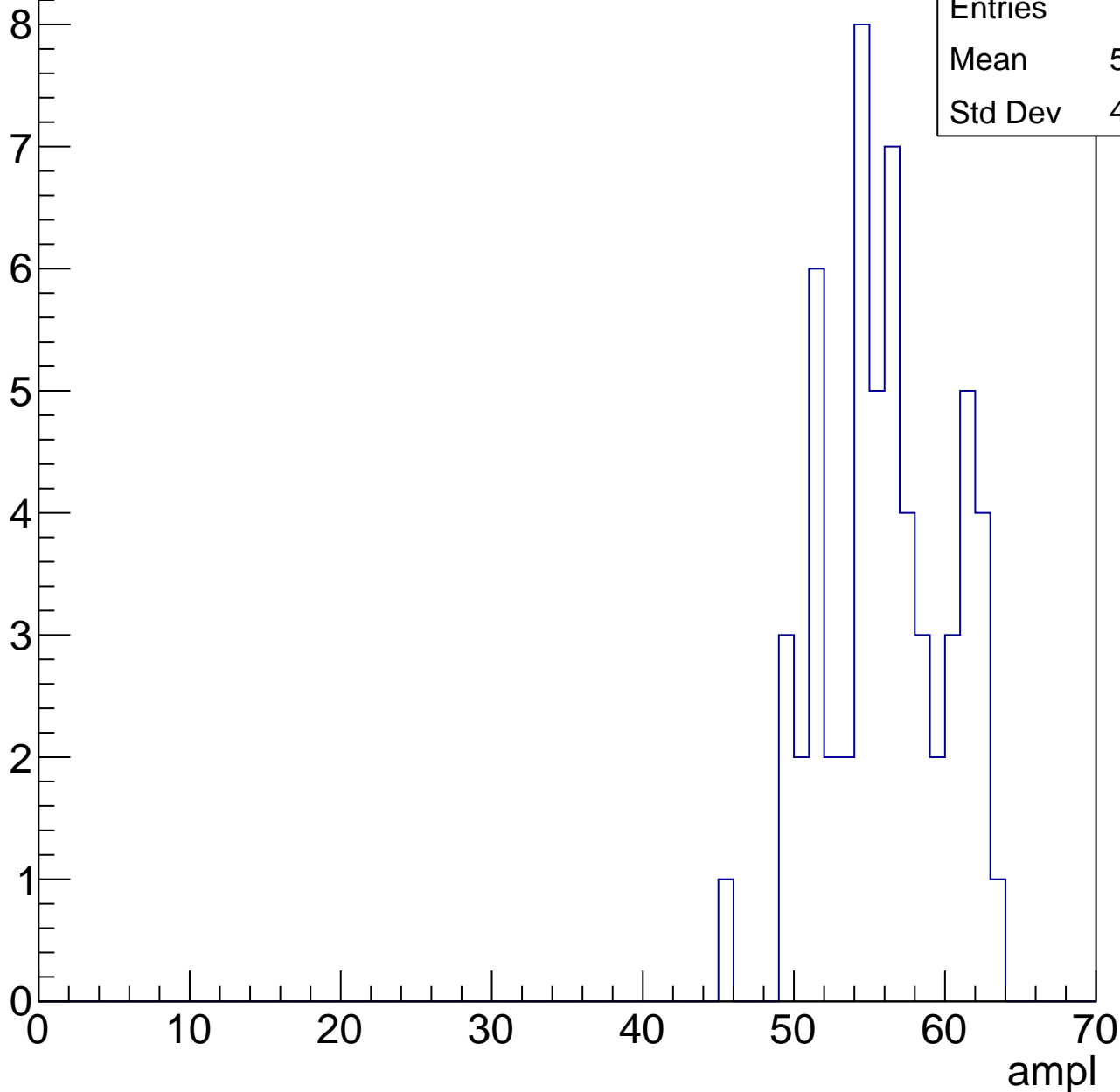


# B1L102S, U5-ch120, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	55.57
Std Dev	4.082



# B1L102S, U5-ch120, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

7  
6  
5  
4  
3  
2  
1  
0

Entries	39
Mean	58.15
Std Dev	9.694

ampl

0

10

20

30

40

50

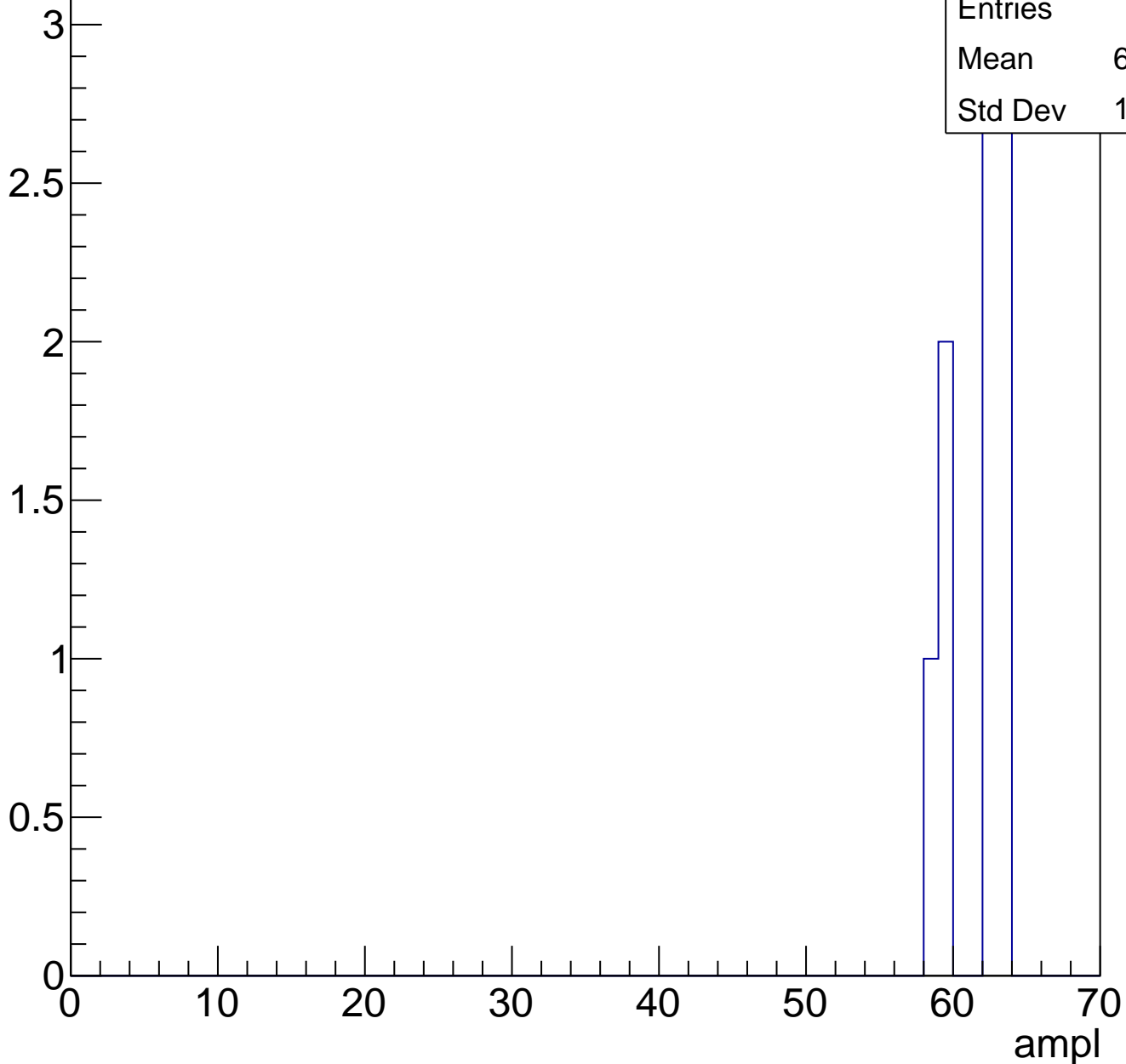
60

70

# B1L102S, U5-ch120, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U5-ch120, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U5-ch121, adc0

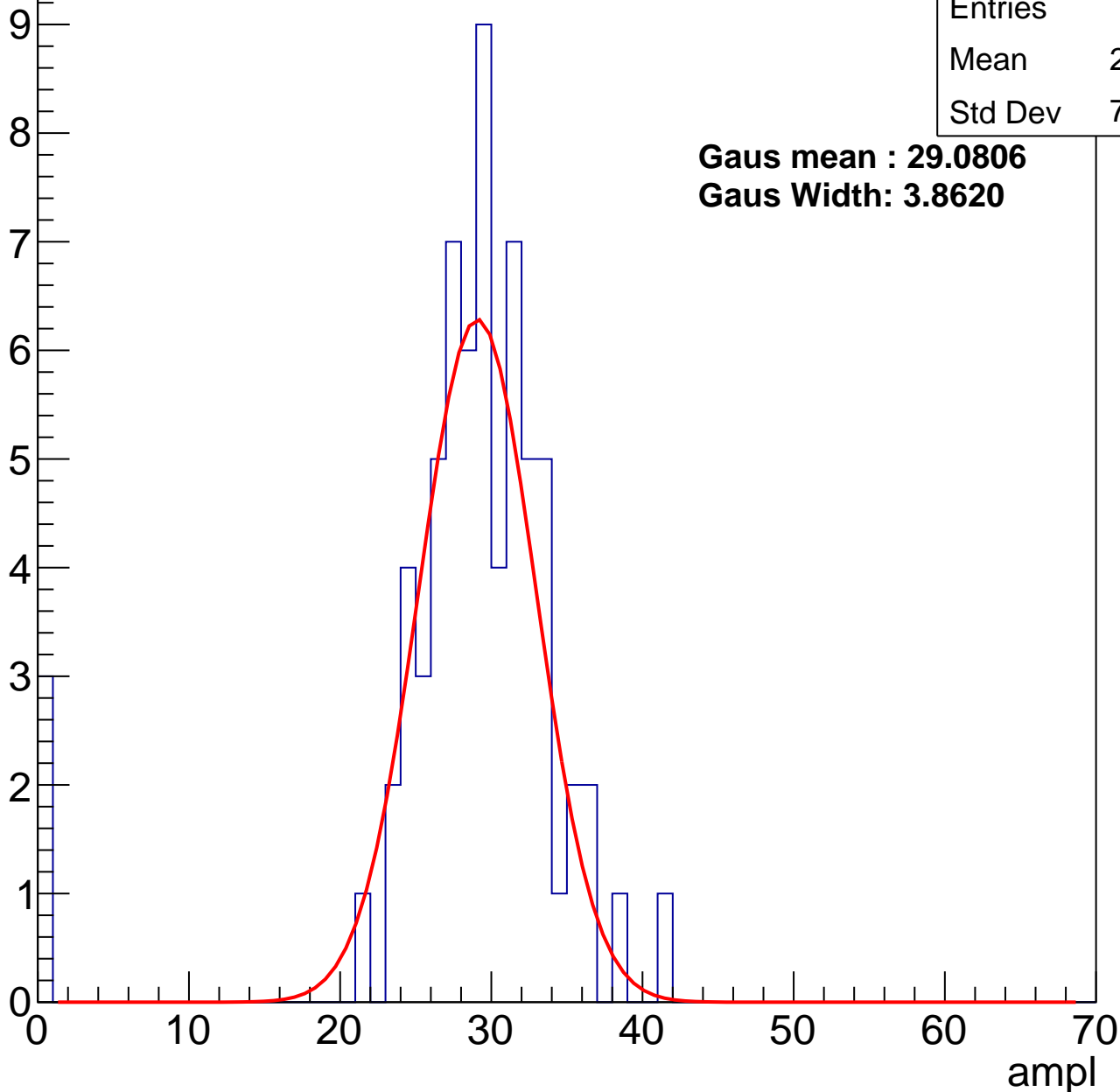
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	27.99
Std Dev	7.064

**Gaus mean : 29.0806**

**Gaus Width: 3.8620**



# B1L102S, U5-ch121, adc1

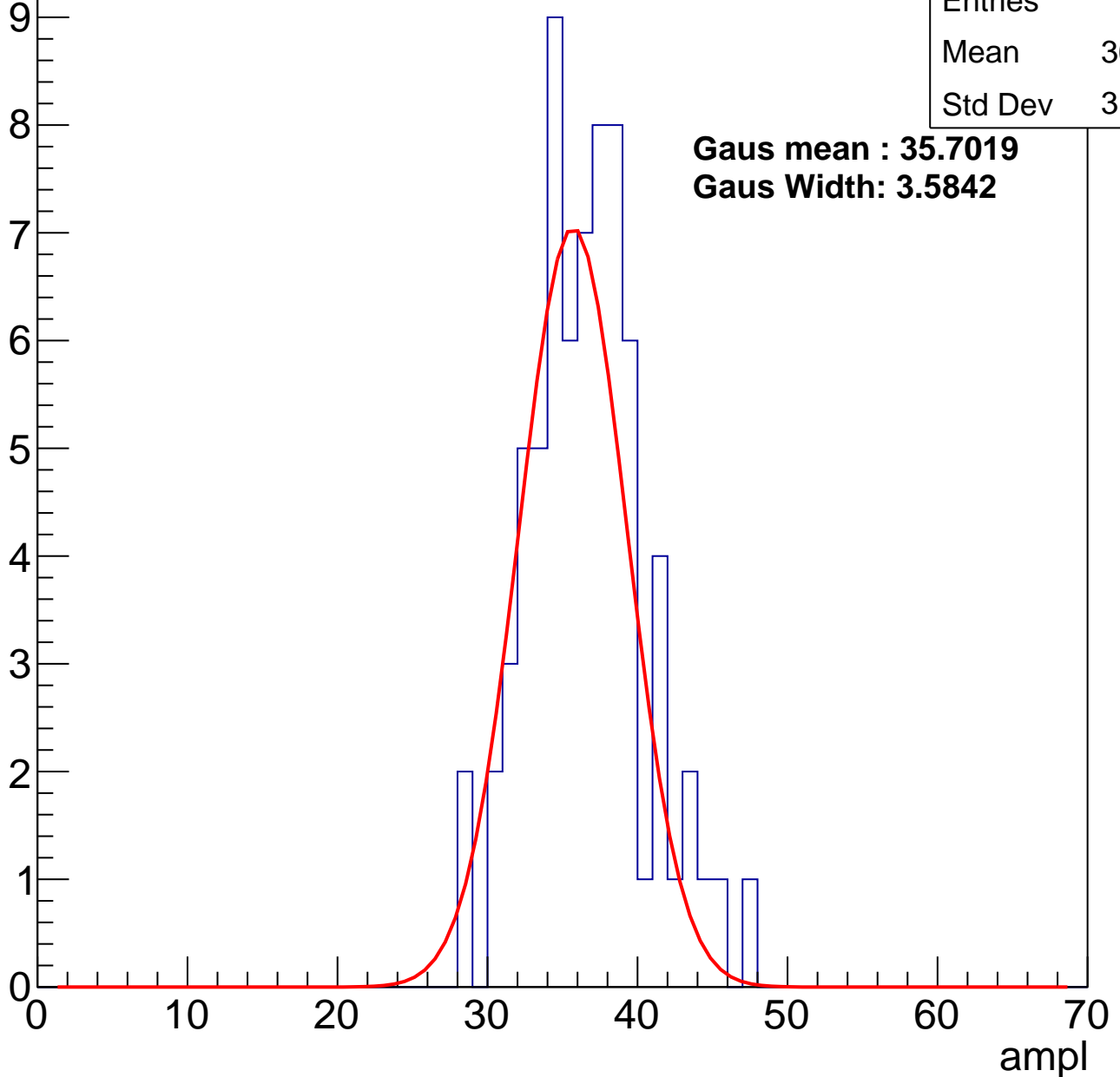
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	36.17
Std Dev	3.819

**Gaus mean : 35.7019**

**Gaus Width: 3.5842**



# B1L102S, U5-ch121, adc2

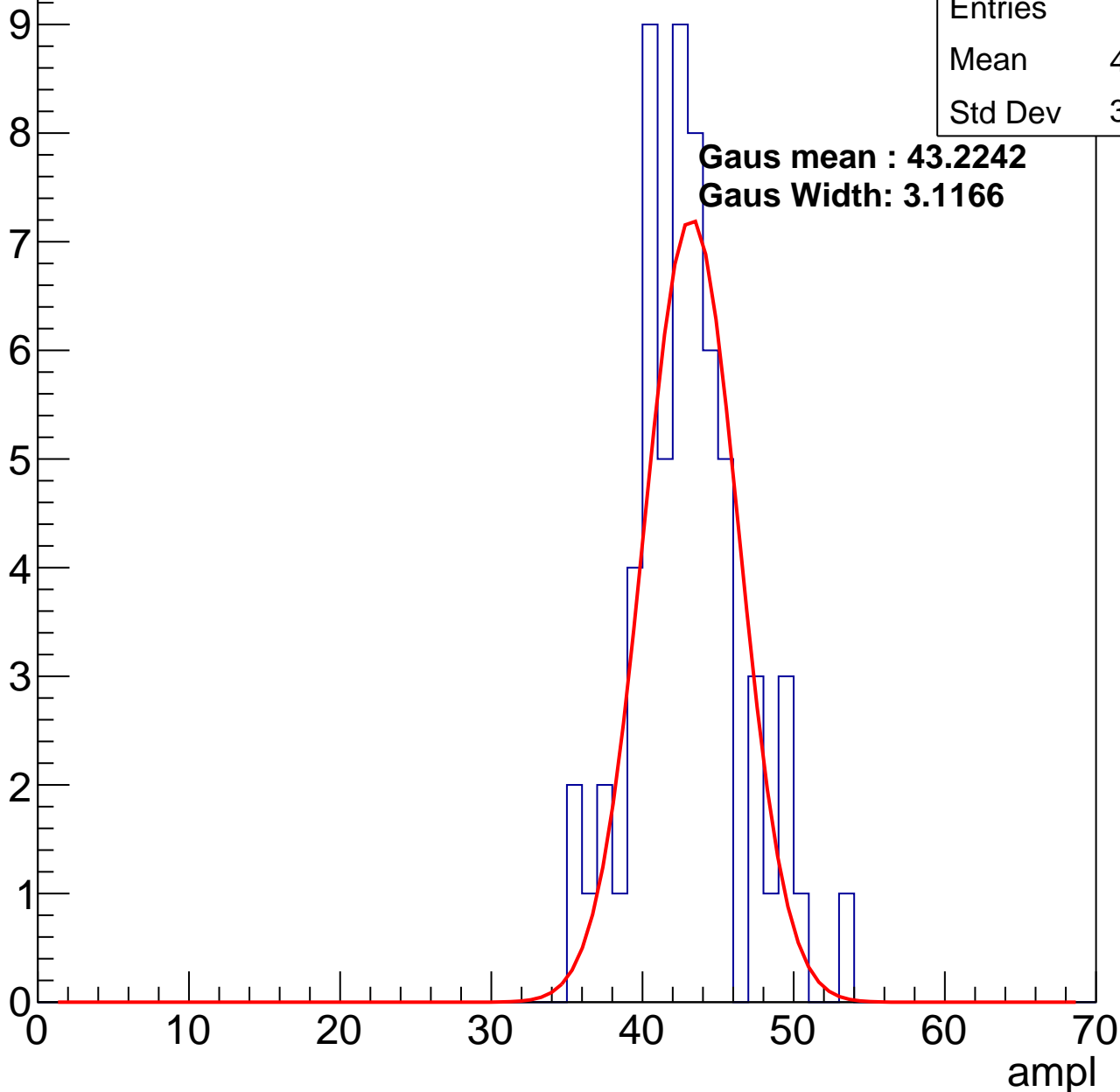
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	42.44
Std Dev	3.587

**Gaus mean : 43.2242**

**Gaus Width: 3.1166**

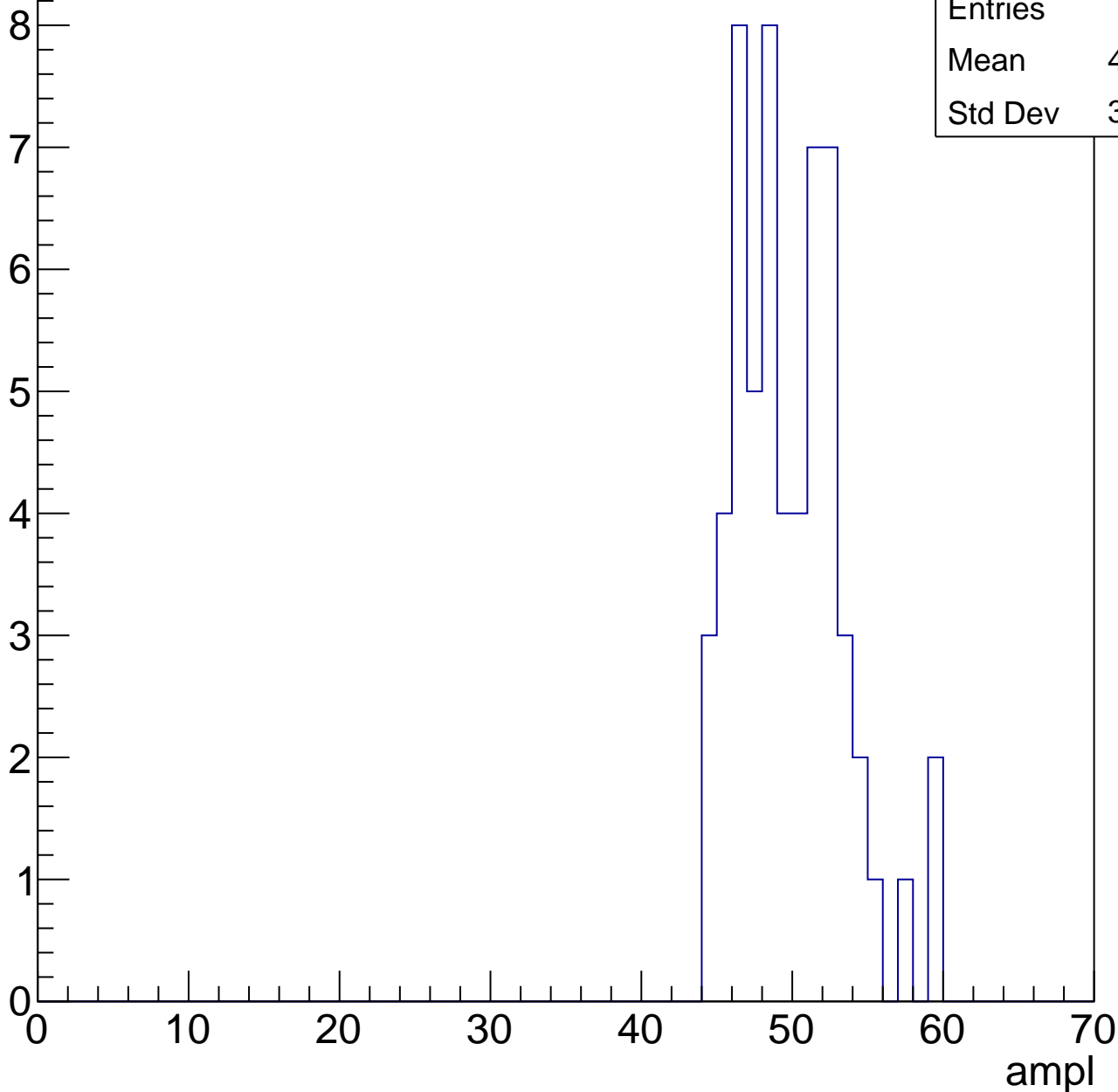


# B1L102S, U5-ch121, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	49.37
Std Dev	3.503

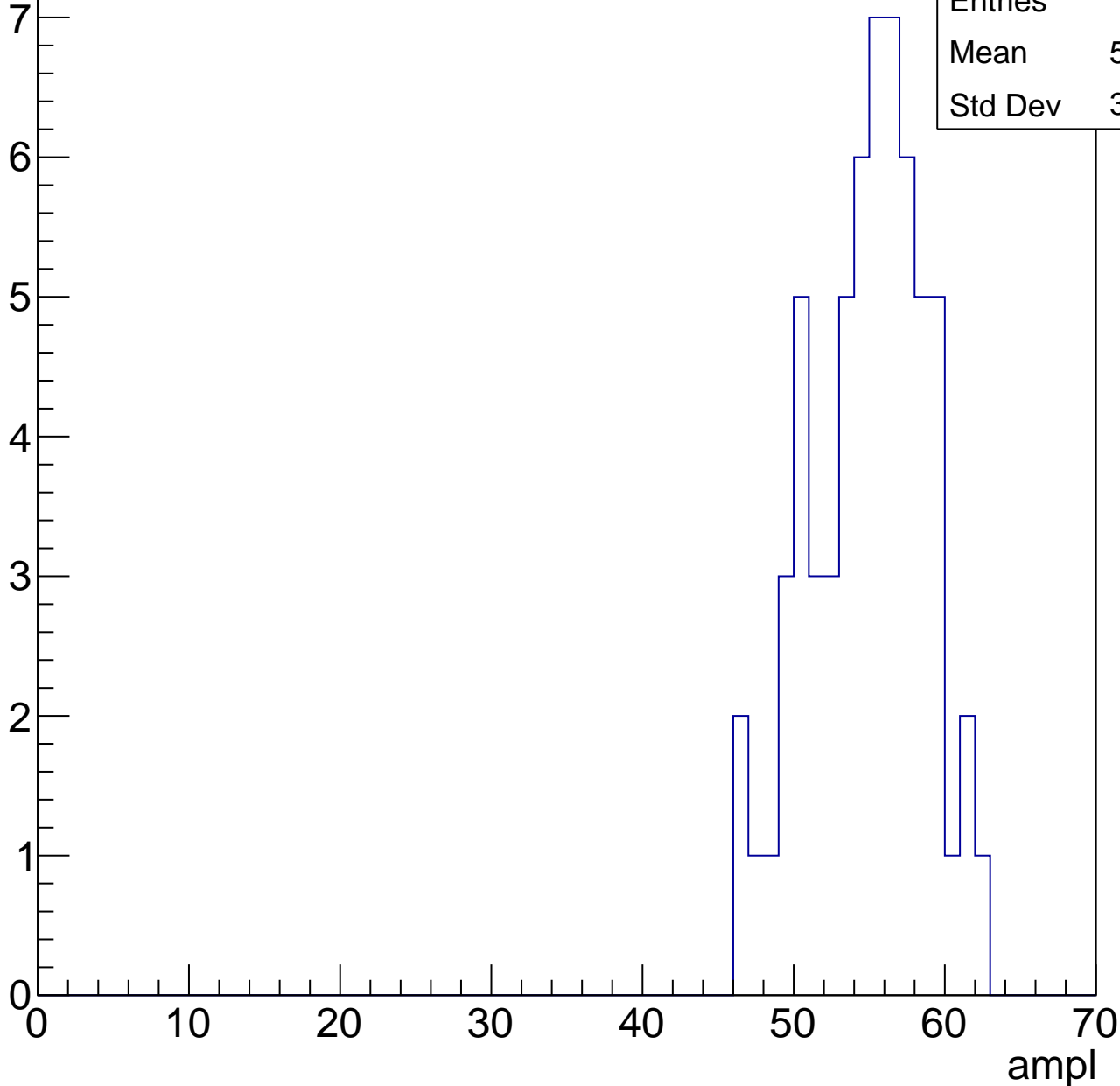


# B1L102S, U5-ch121, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	54.44
Std Dev	3.762

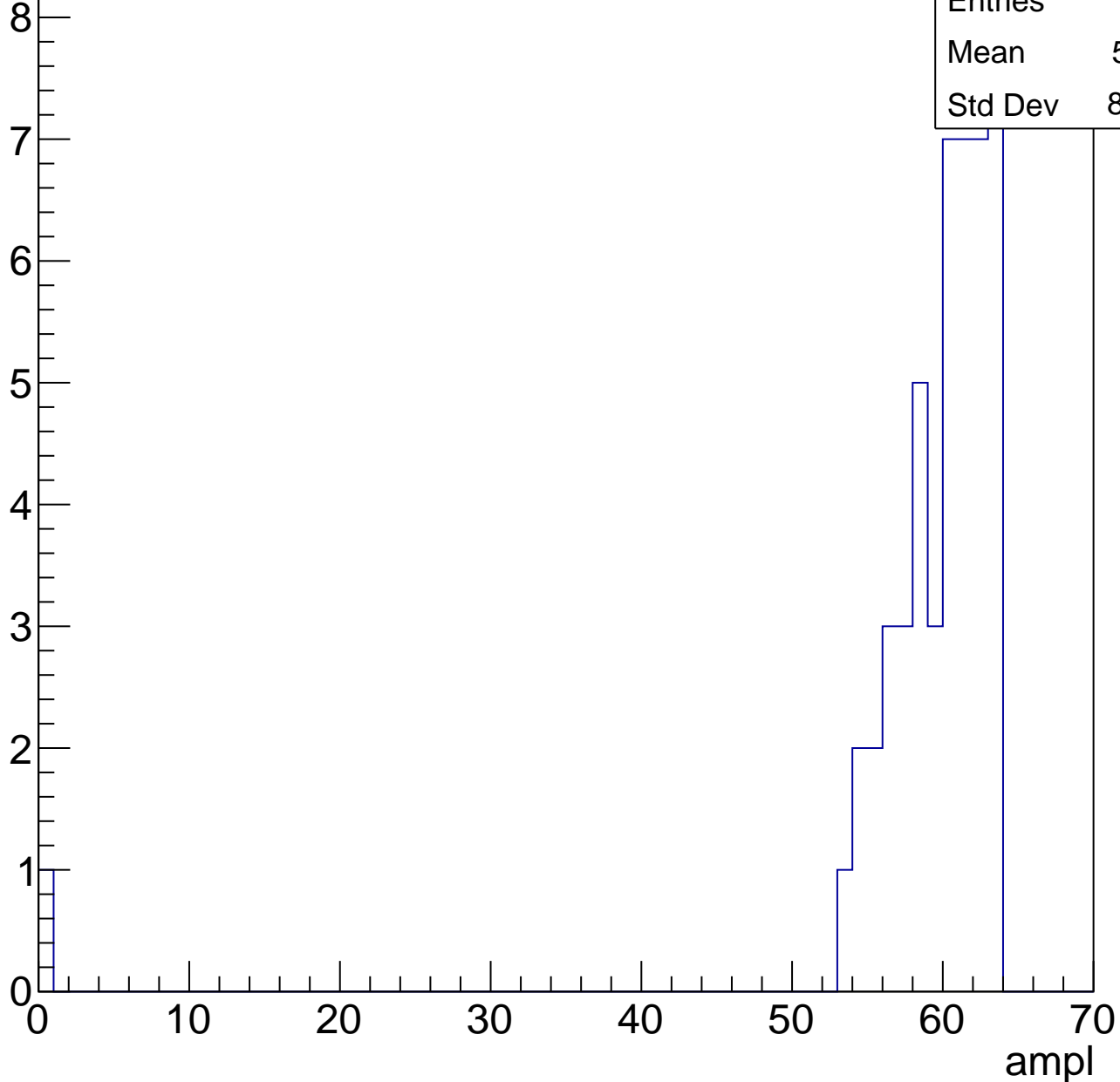


# B1L102S, U5-ch121, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	58.41
Std Dev	8.866



# B1L102S, U5-ch121, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

0

10

20

30

40

50

60

70

ampl

Entries	7
Mean	61.57
Std Dev	1.178



# B1L102S, U5-ch121, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	10.5
Std Dev	10.5

# B1L102S, U5-ch122, adc0

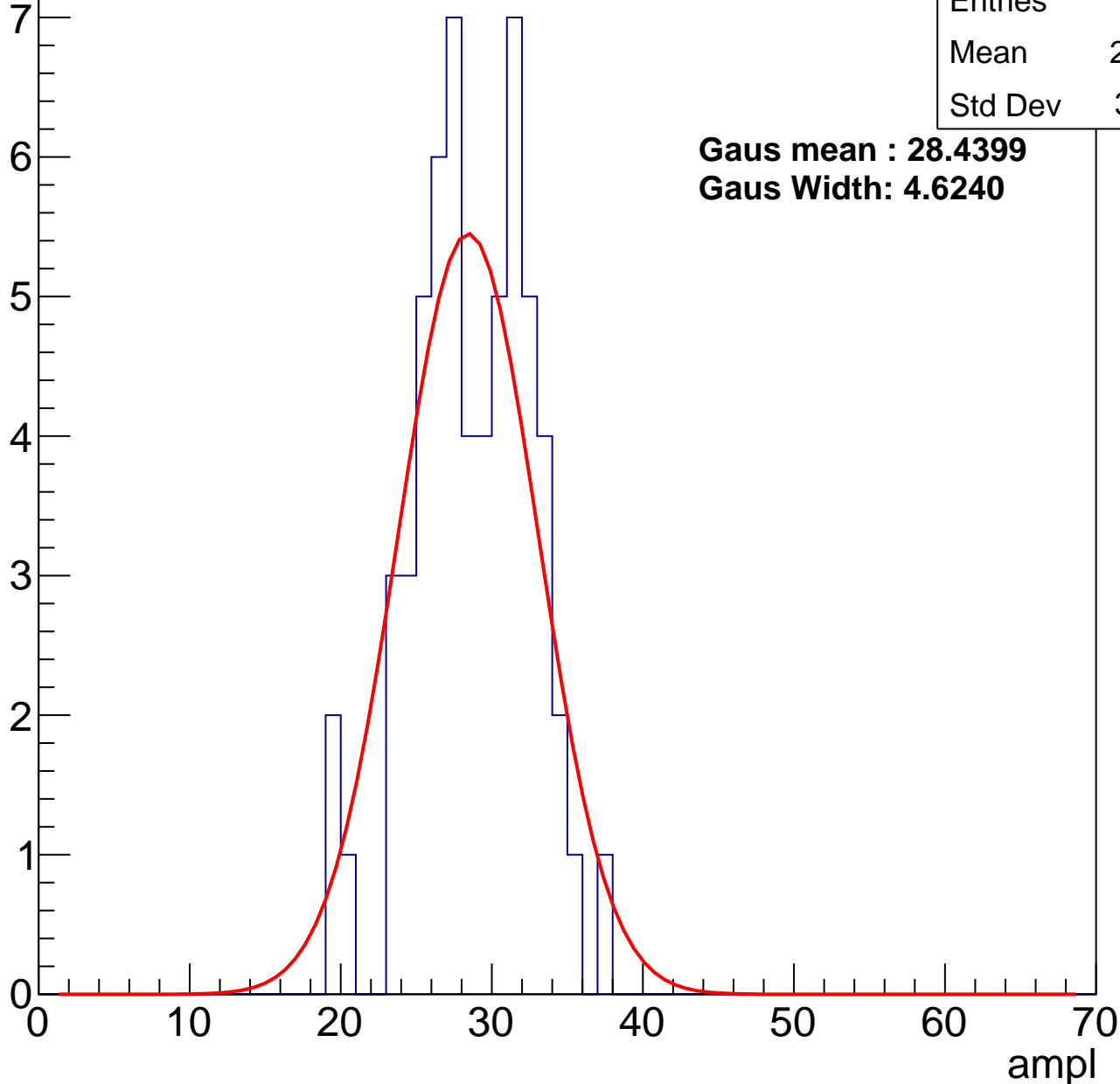
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	28.27
Std Dev	3.851

**Gaus mean : 28.4399**

**Gaus Width: 4.6240**



# B1L102S, U5-ch122, adc1

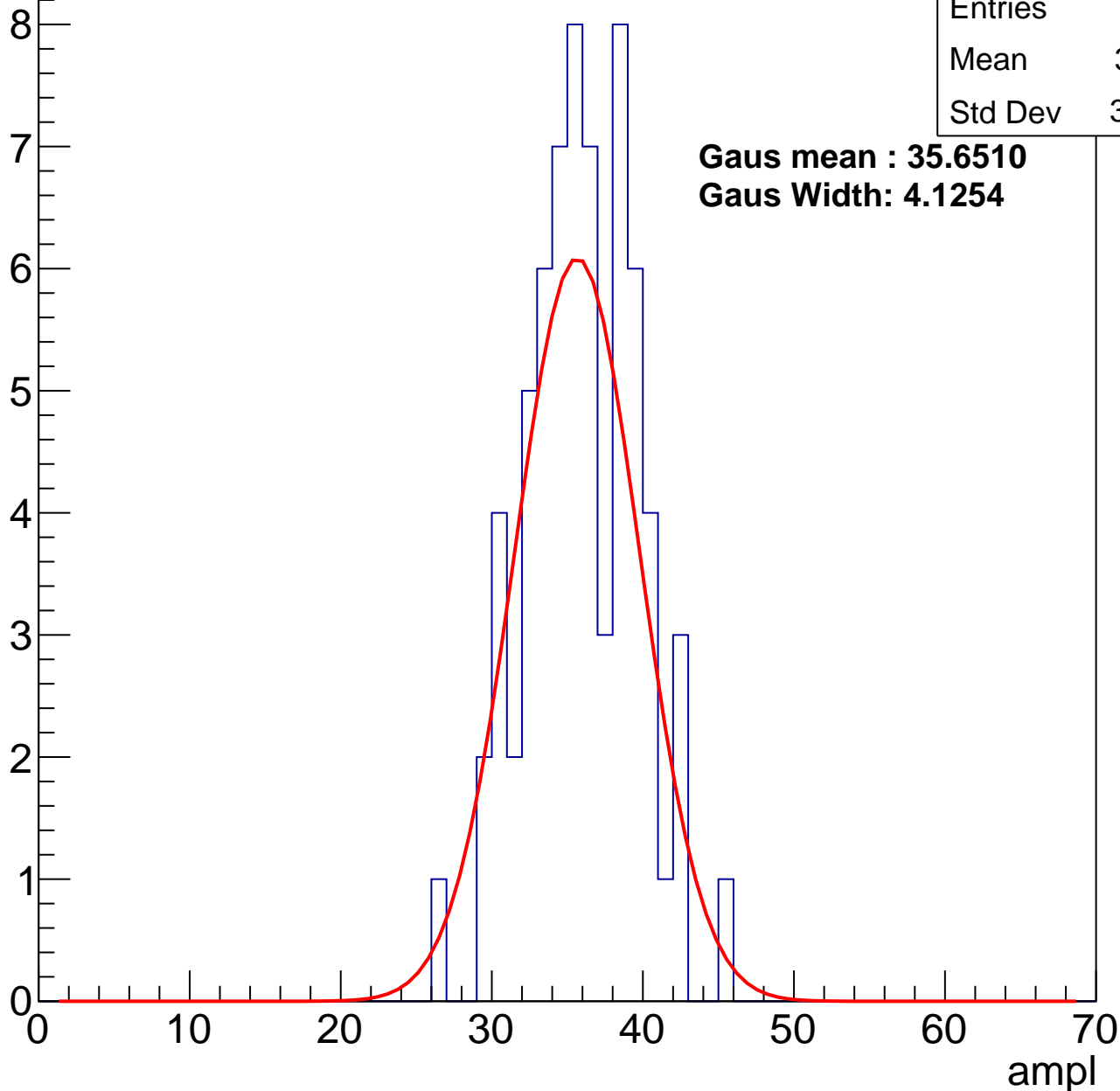
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	35.51
Std Dev	3.664

**Gaus mean : 35.6510**

**Gaus Width: 4.1254**



# B1L102S, U5-ch122, adc2

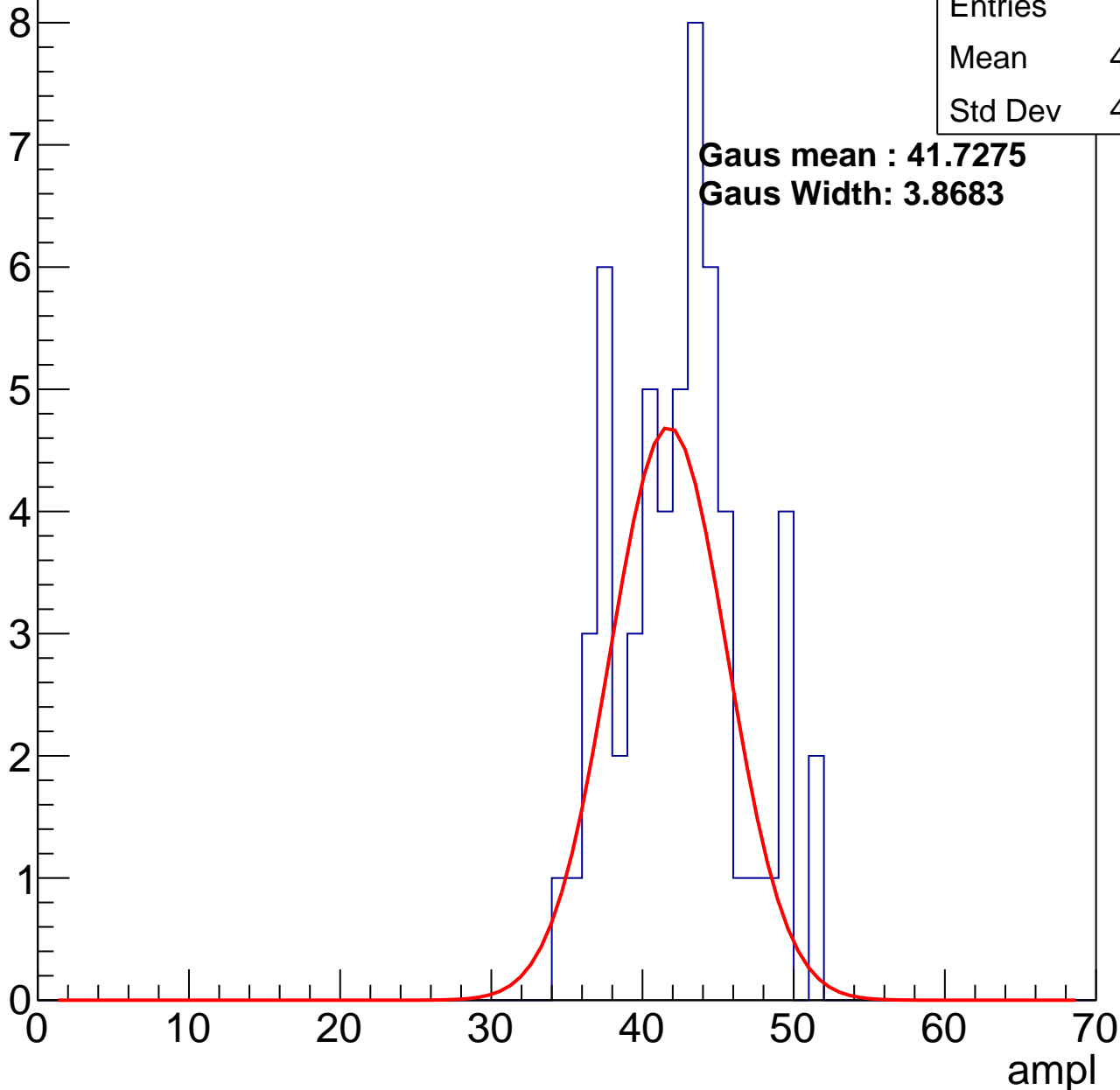
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	41.98
Std Dev	4.097

**Gaus mean : 41.7275**

**Gaus Width: 3.8683**

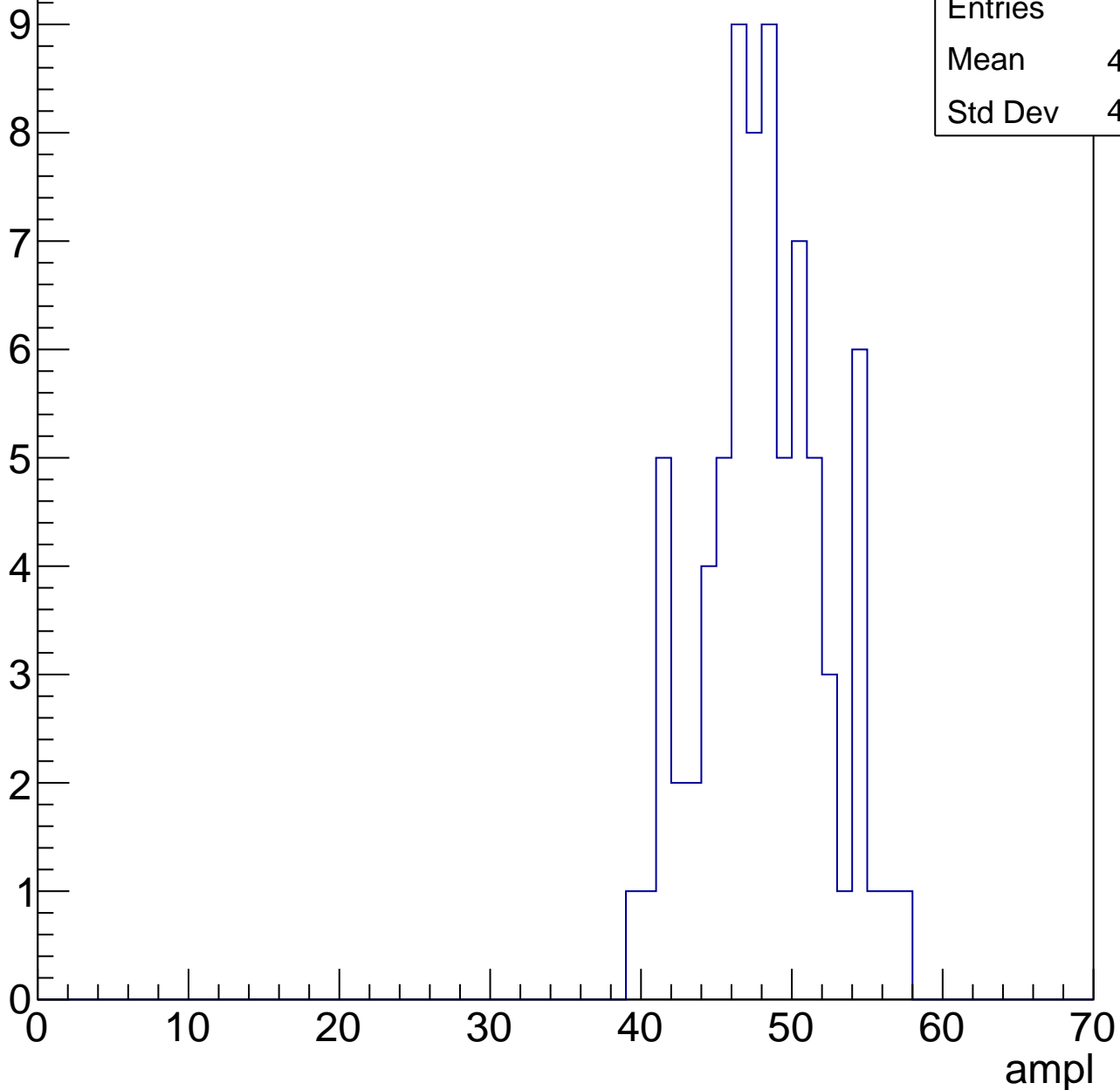


# B1L102S, U5-ch122, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	47.74
Std Dev	4.008

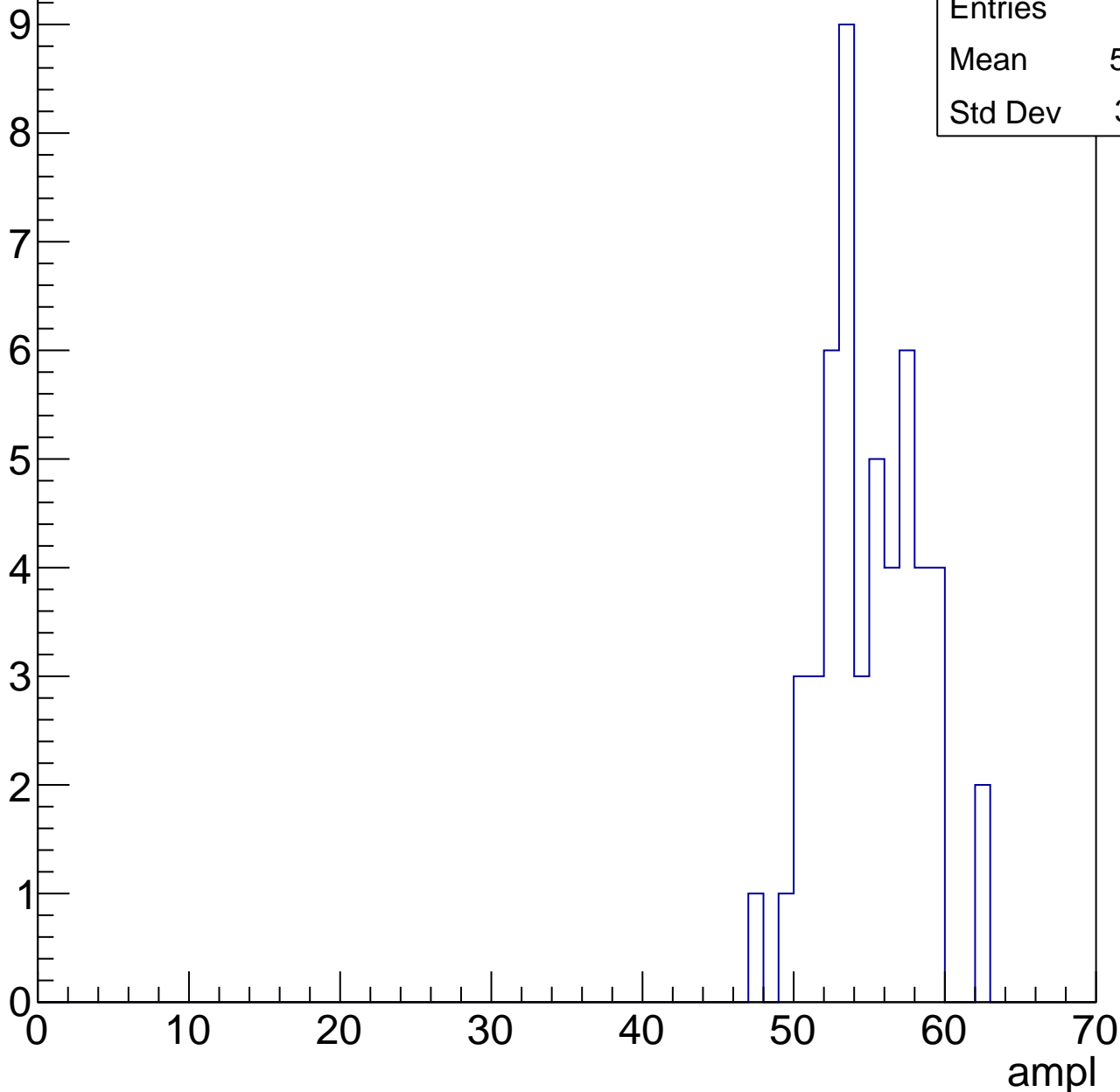


# B1L102S, U5-ch122, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	54.57
Std Dev	3.231

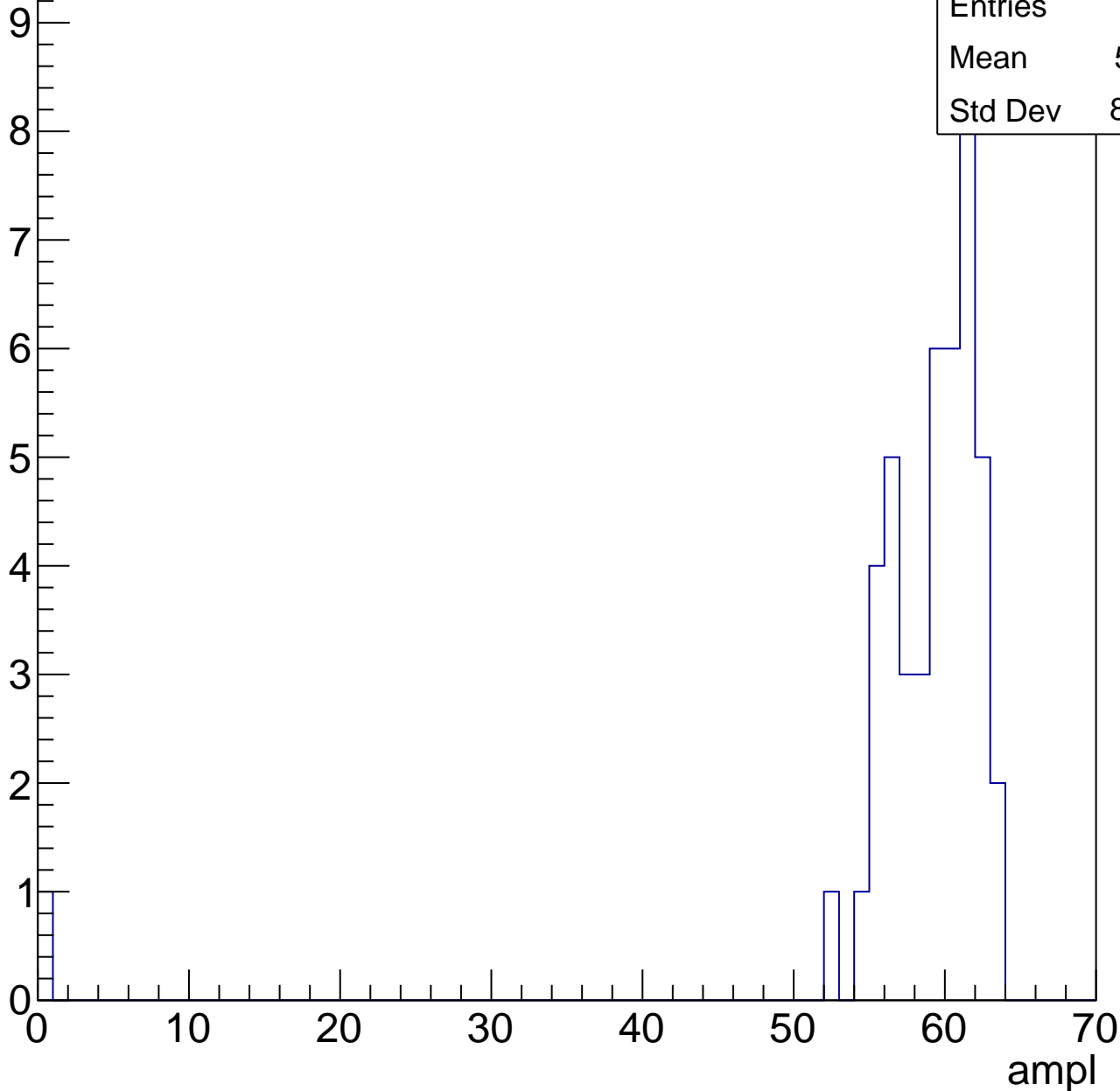


# B1L102S, U5-ch122, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	46
Mean	57.61
Std Dev	8.979

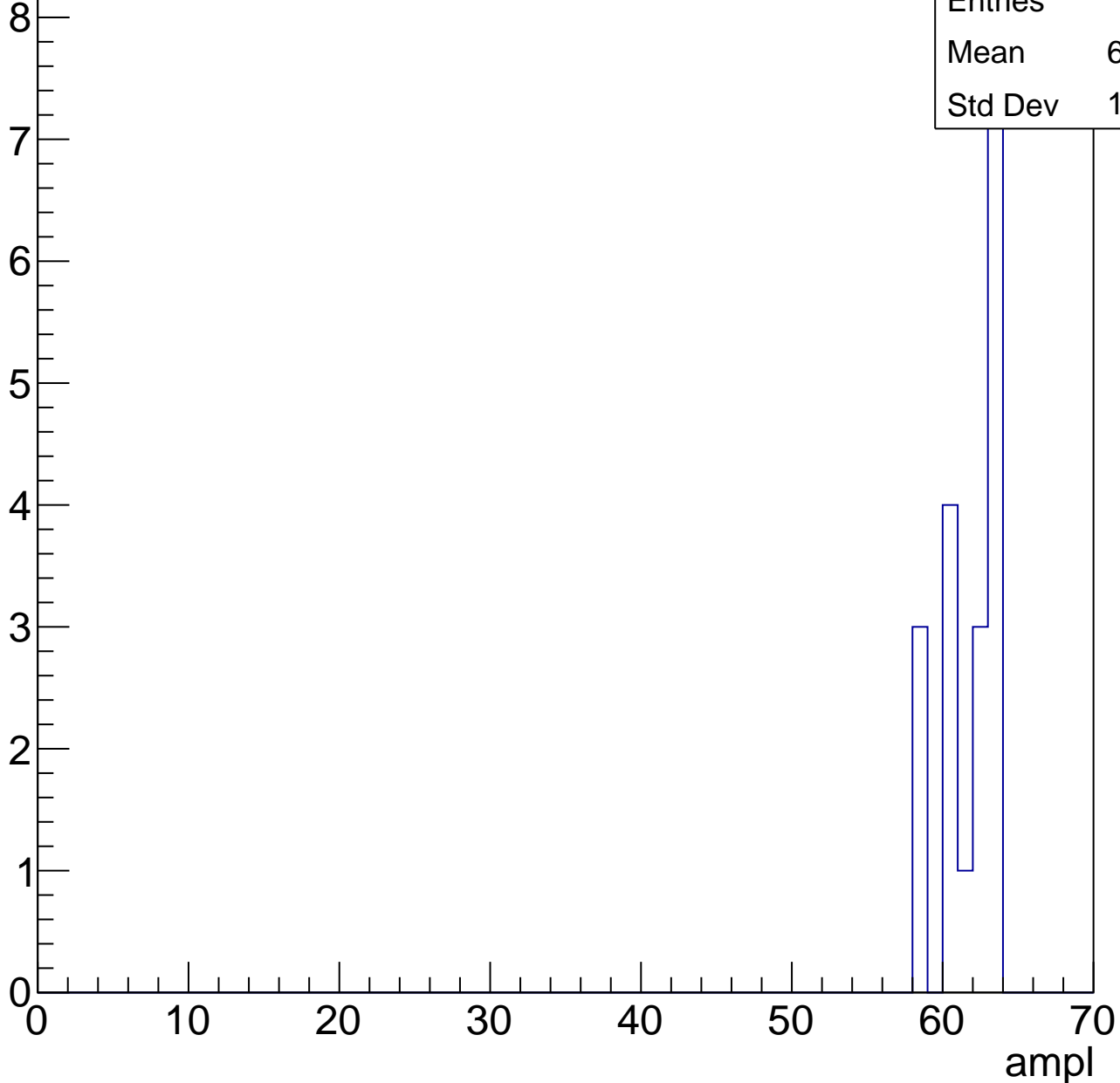


# B1L102S, U5-ch122, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	19
Mean	61.32
Std Dev	1.837





# B1L102S, U5-ch122, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U5-ch123, adc0

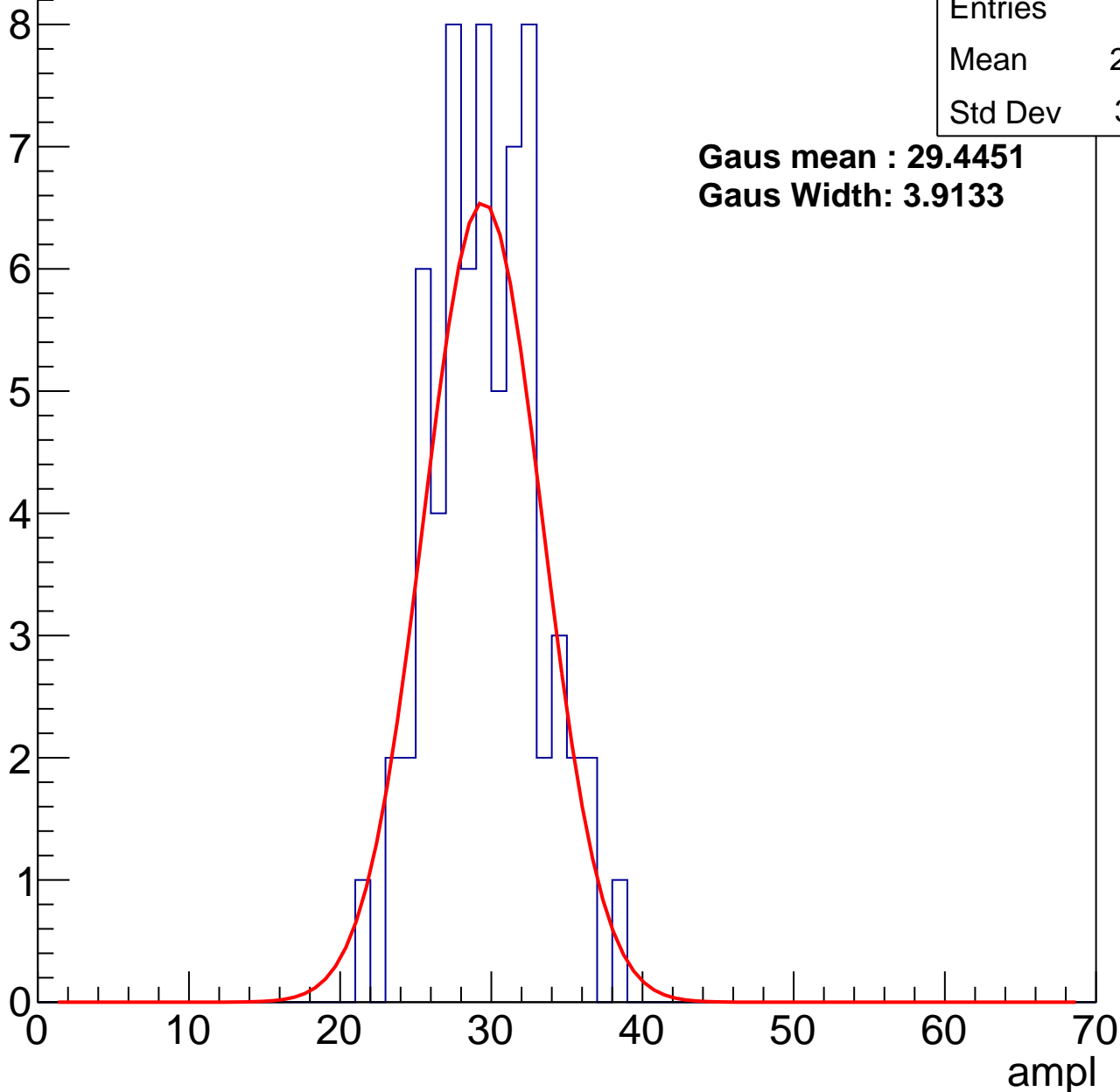
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	29.19
Std Dev	3.491

**Gaus mean : 29.4451**

**Gaus Width: 3.9133**



# B1L102S, U5-ch123, adc1

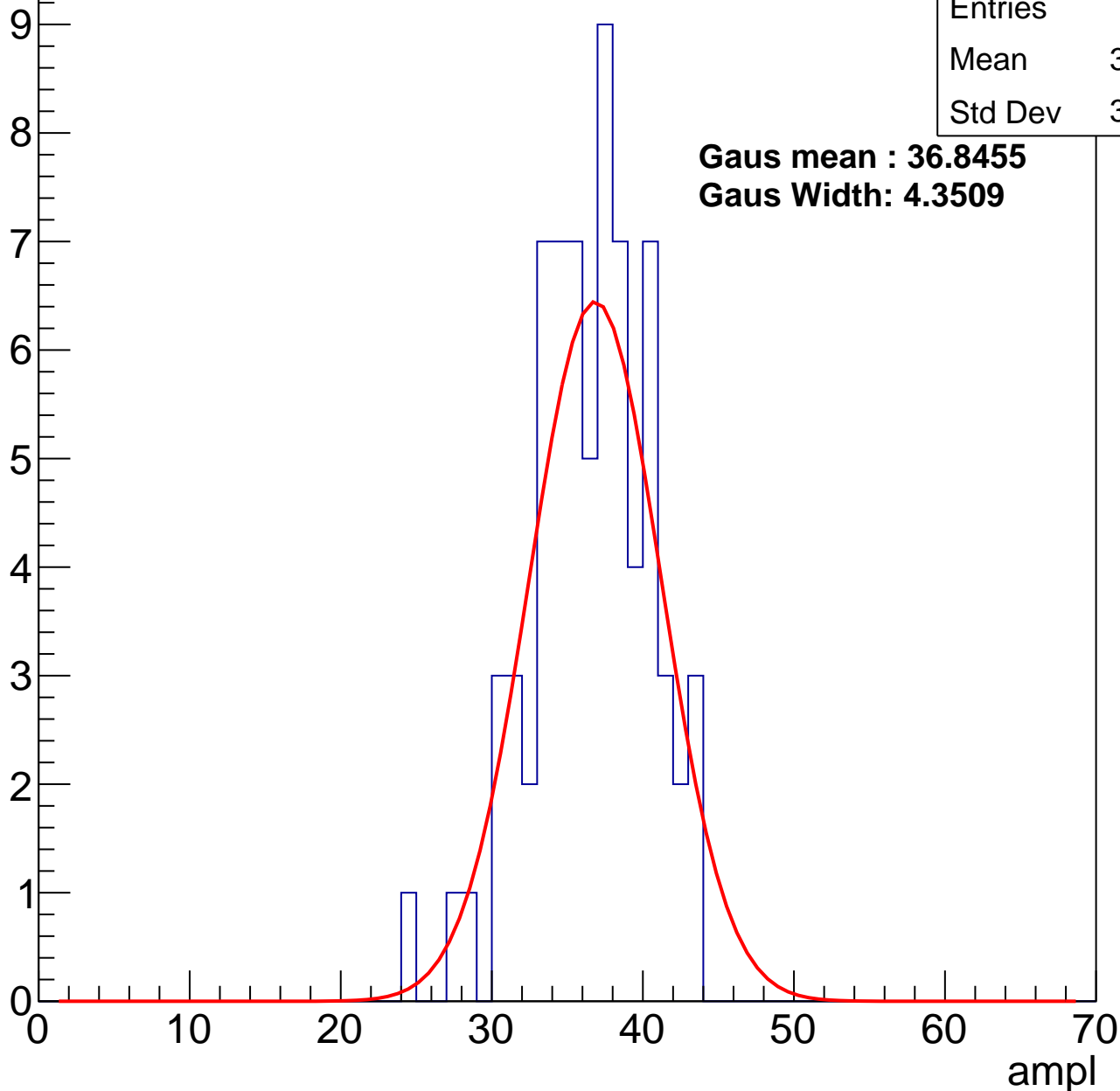
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	35.99
Std Dev	3.875

**Gaus mean : 36.8455**

**Gaus Width: 4.3509**



# B1L102S, U5-ch123, adc2

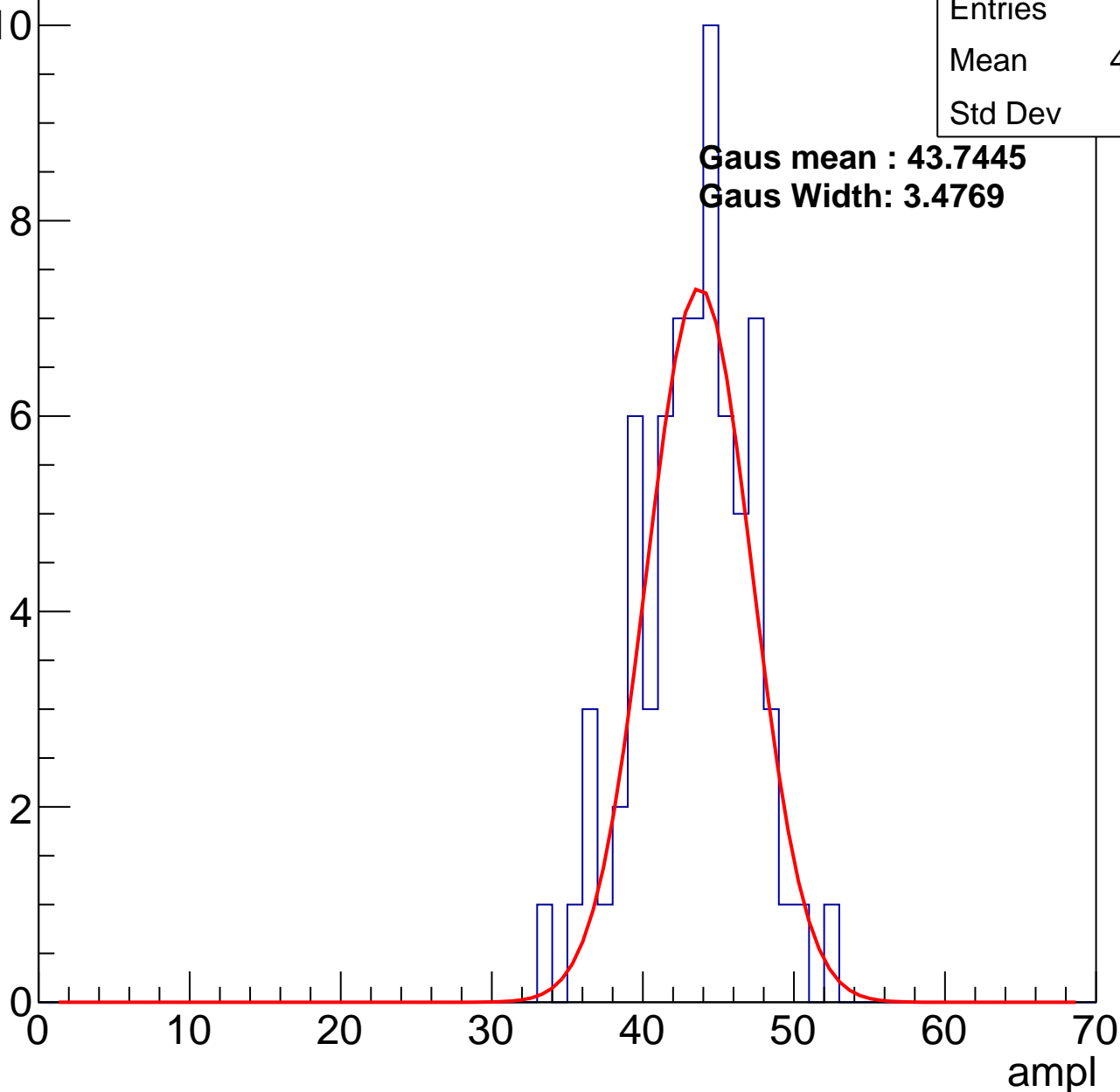
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	42.93
Std Dev	3.72

**Gaus mean : 43.7445**

**Gaus Width: 3.4769**

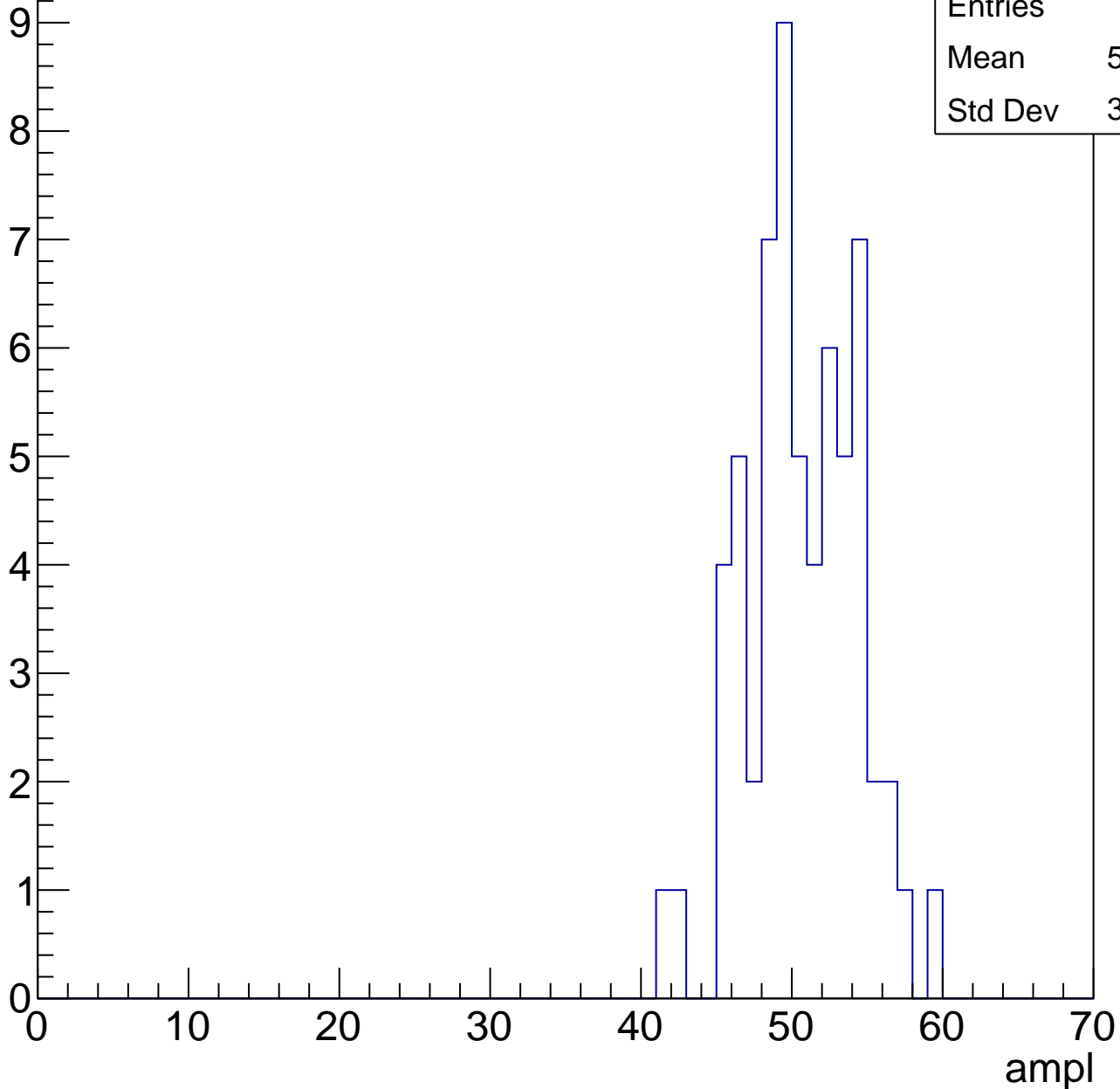


# B1L102S, U5-ch123, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	50.18
Std Dev	3.626

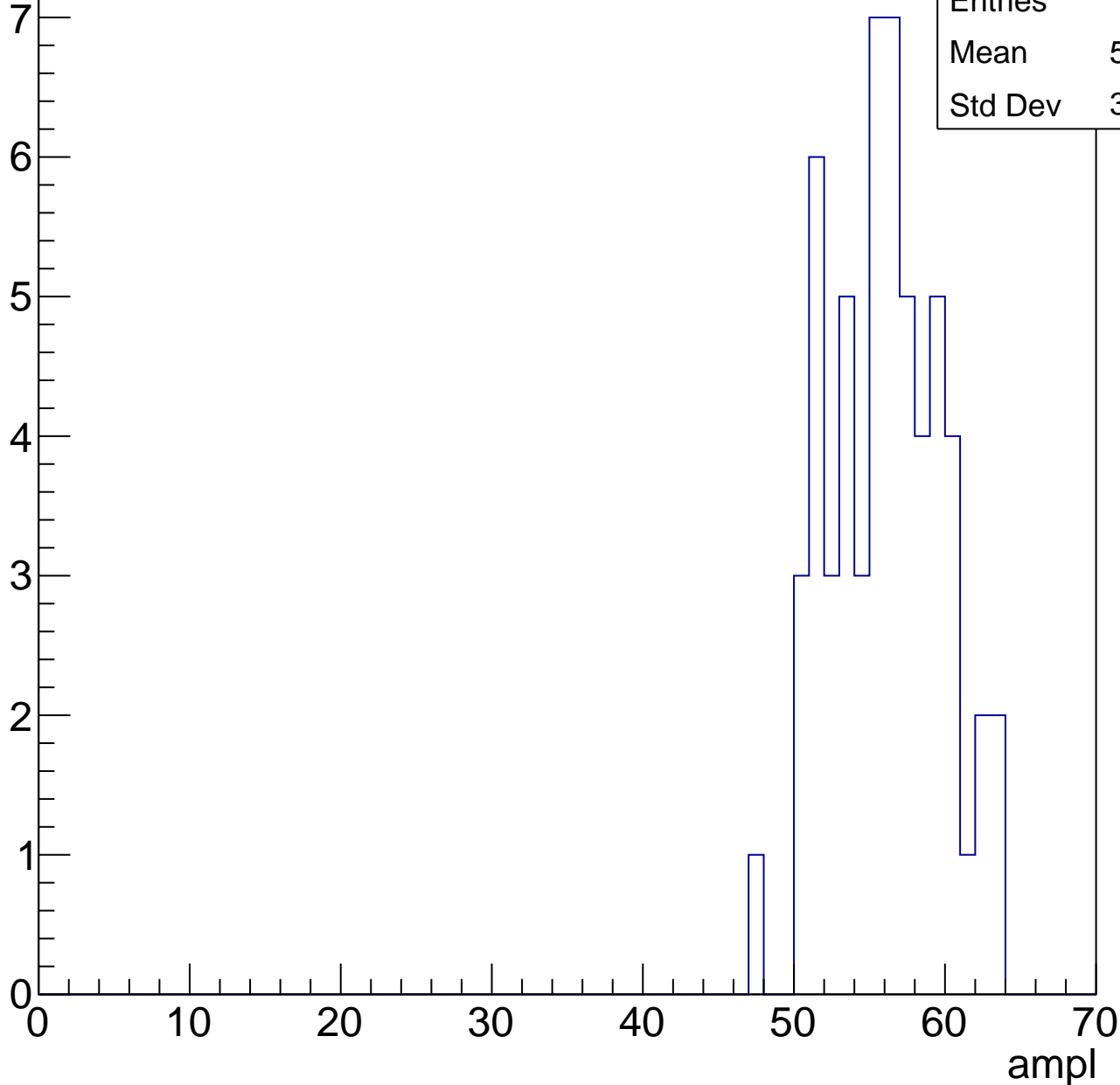


# B1L102S, U5-ch123, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	55.62
Std Dev	3.638

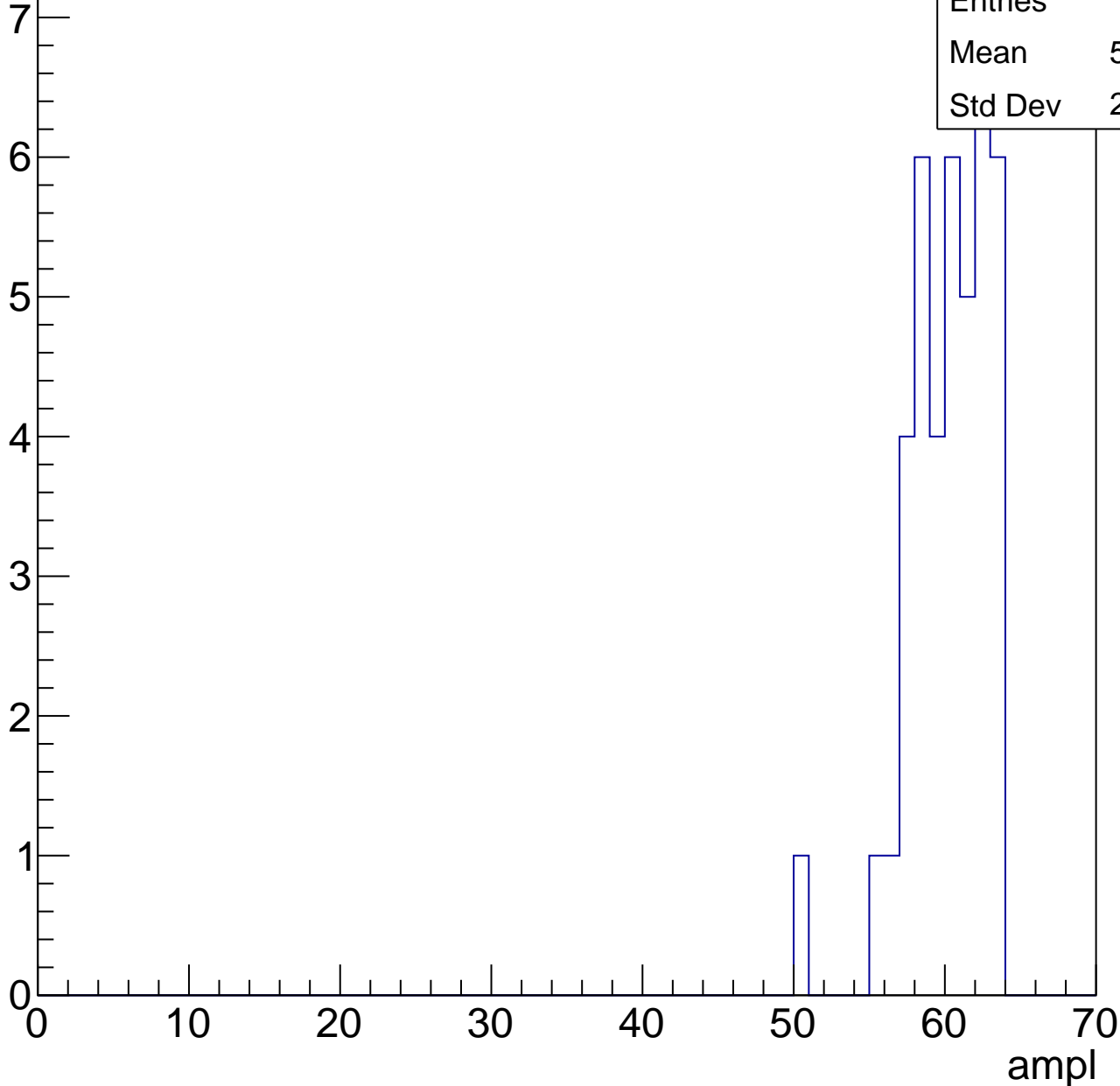


# B1L102S, U5-ch123, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

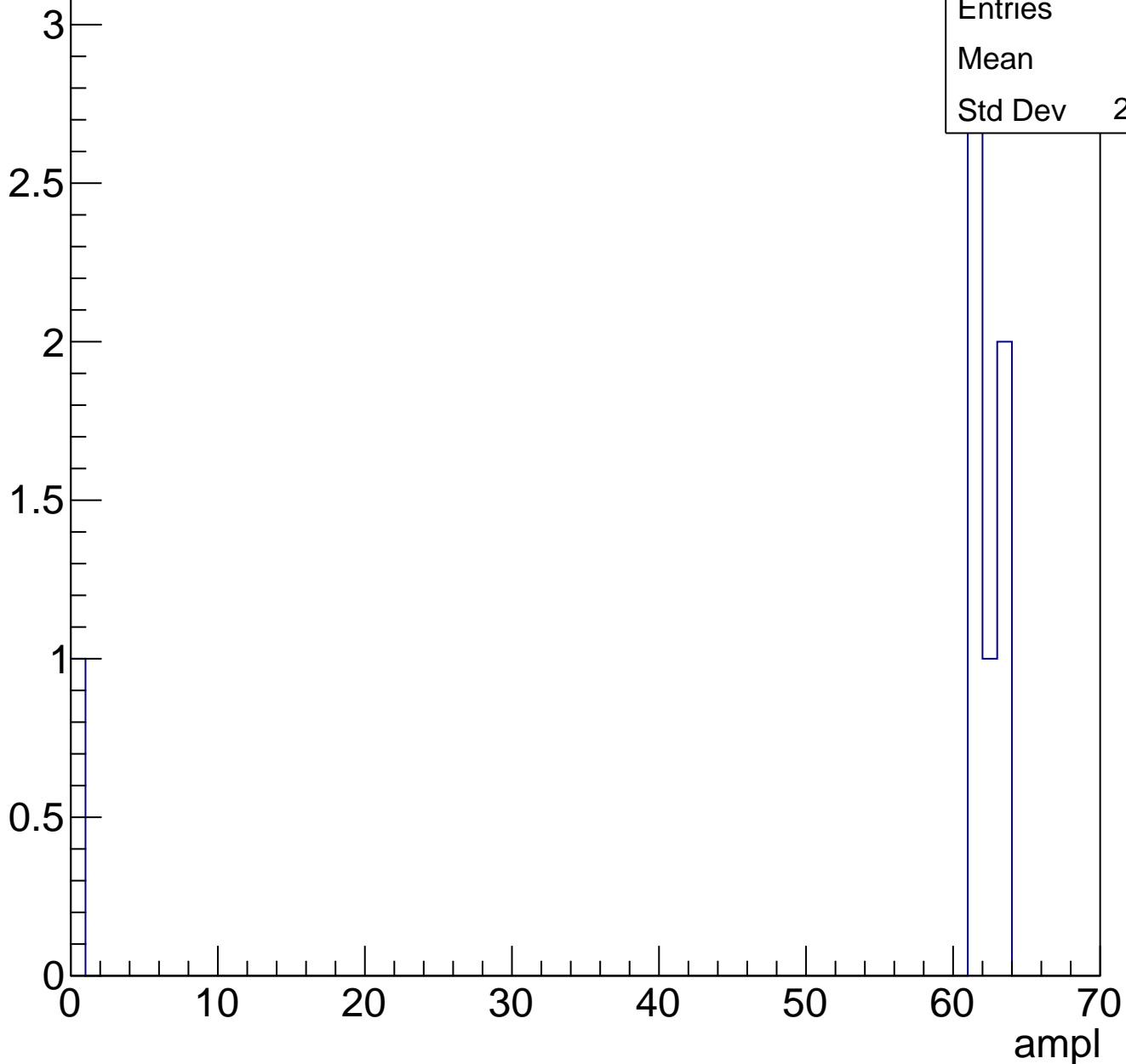
Entries	41
Mean	59.76
Std Dev	2.658



# B1L102S, U5-ch123, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



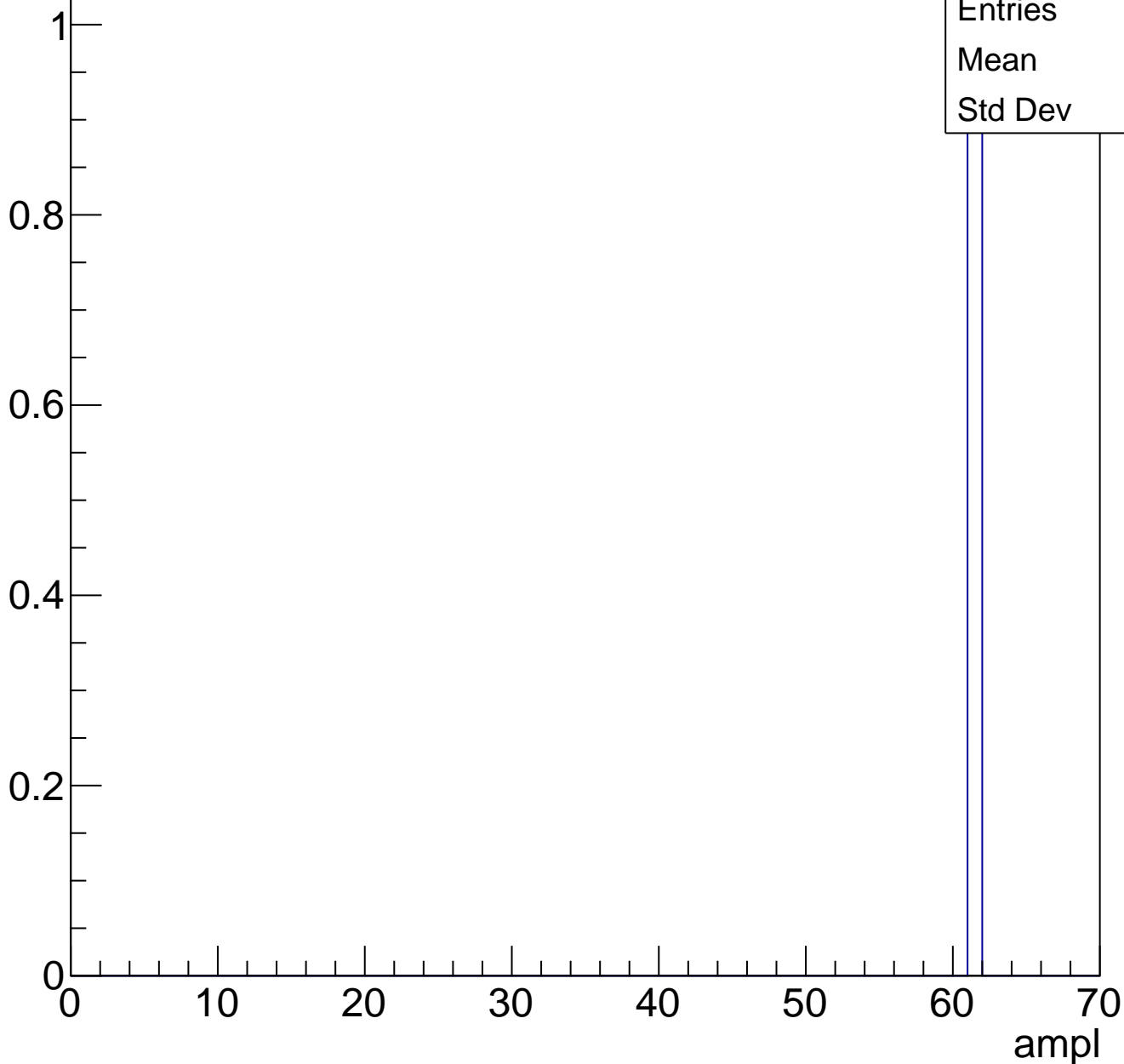
Entries	7
Mean	53
Std Dev	21.65



# B1L102S, U5-ch123, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U5-ch124, adc0

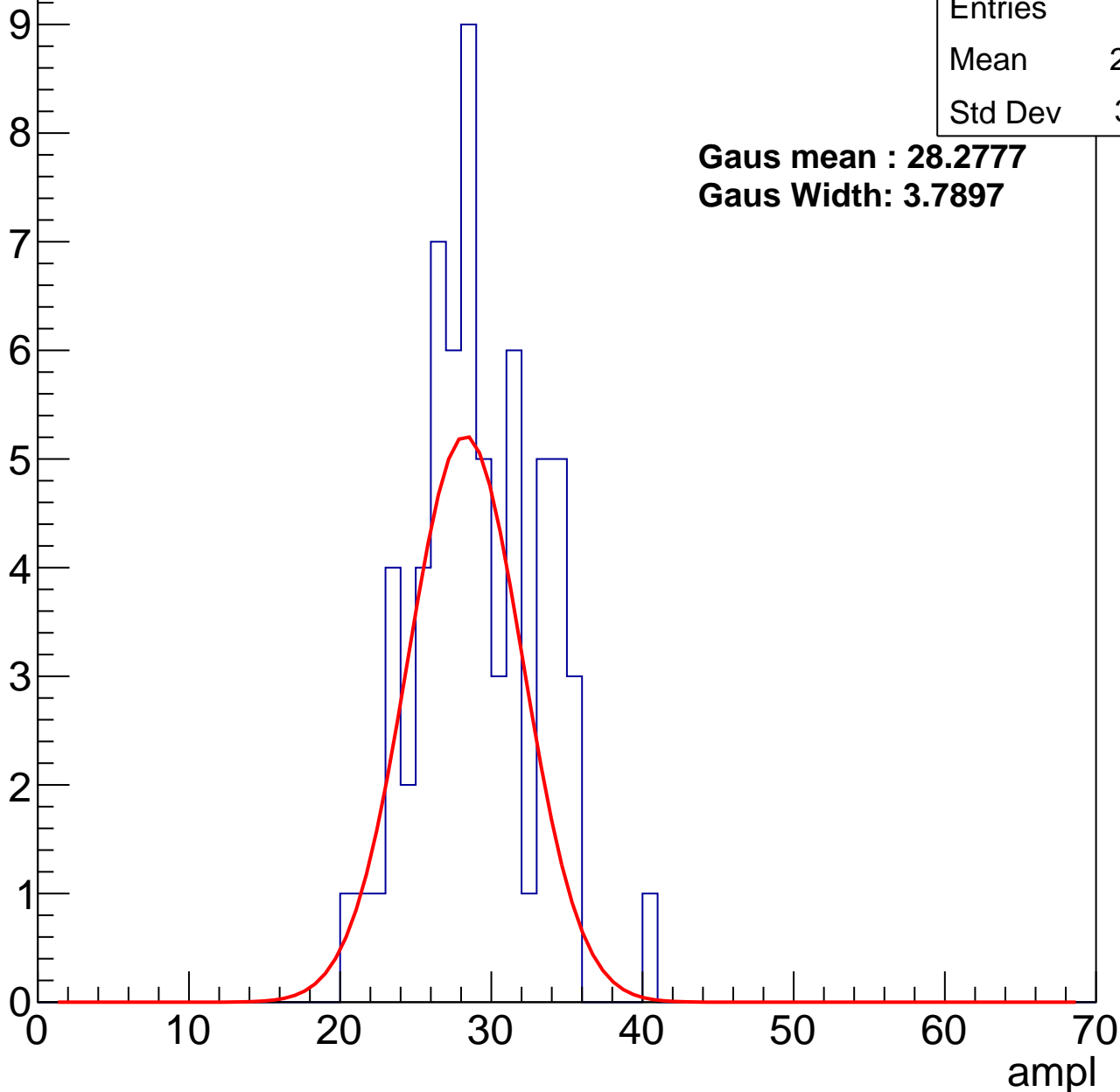
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	28.62
Std Dev	3.971

**Gaus mean : 28.2777**

**Gaus Width: 3.7897**



# B1L102S, U5-ch124, adc1

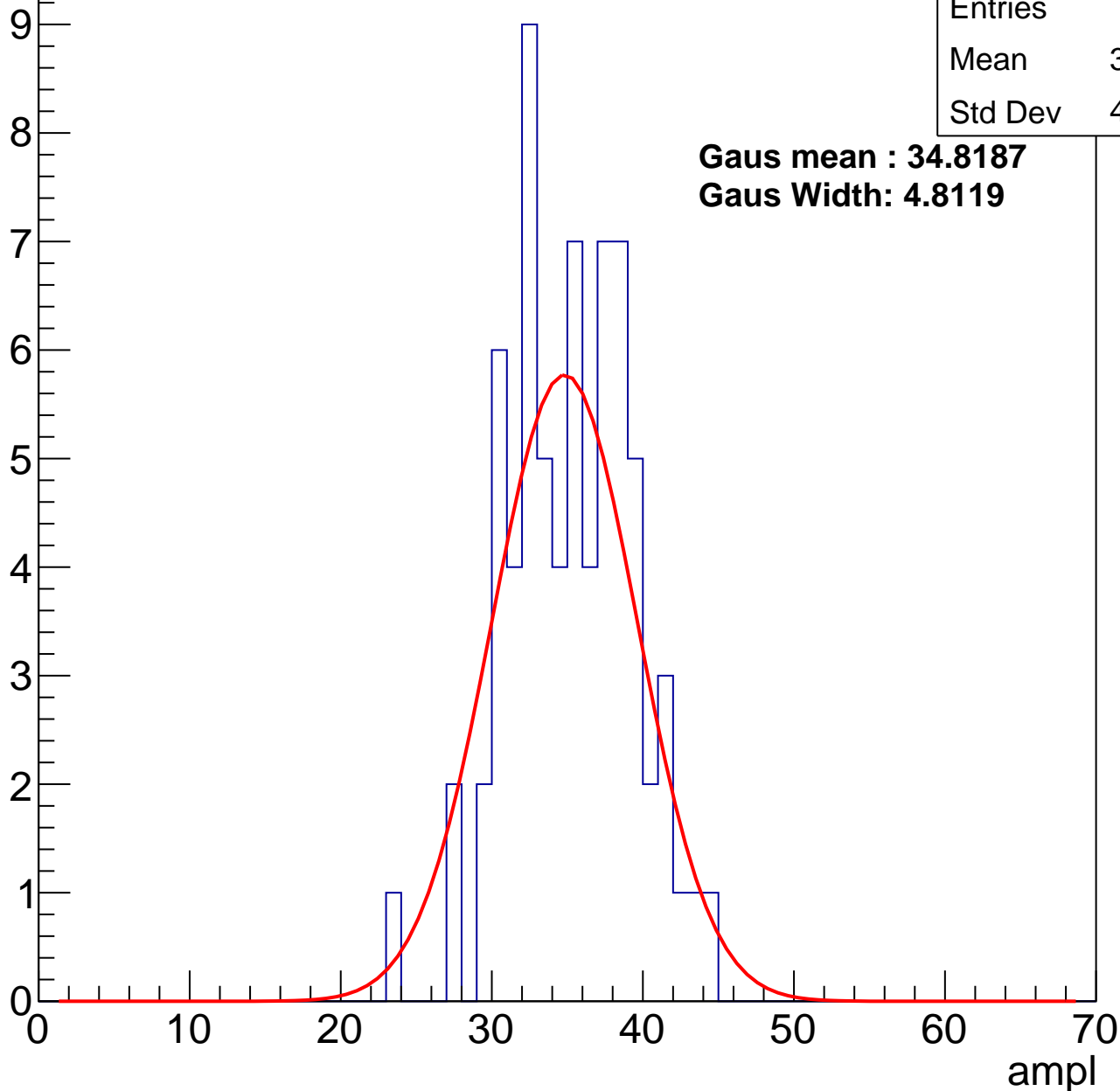
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	34.77
Std Dev	4.088

**Gaus mean : 34.8187**

**Gaus Width: 4.8119**



# B1L102S, U5-ch124, adc2

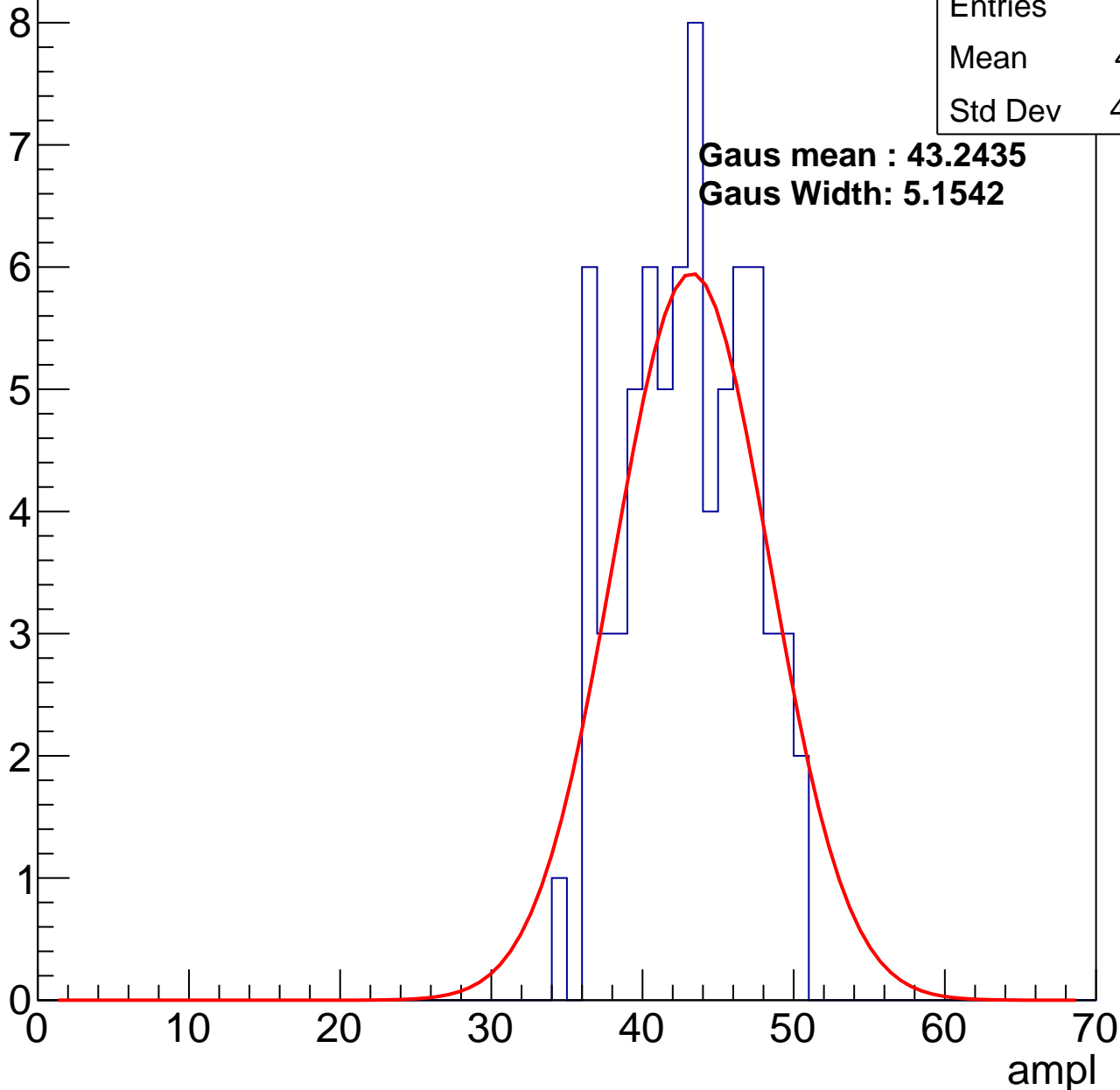
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	42.51
Std Dev	4.007

**Gaus mean : 43.2435**

**Gaus Width: 5.1542**

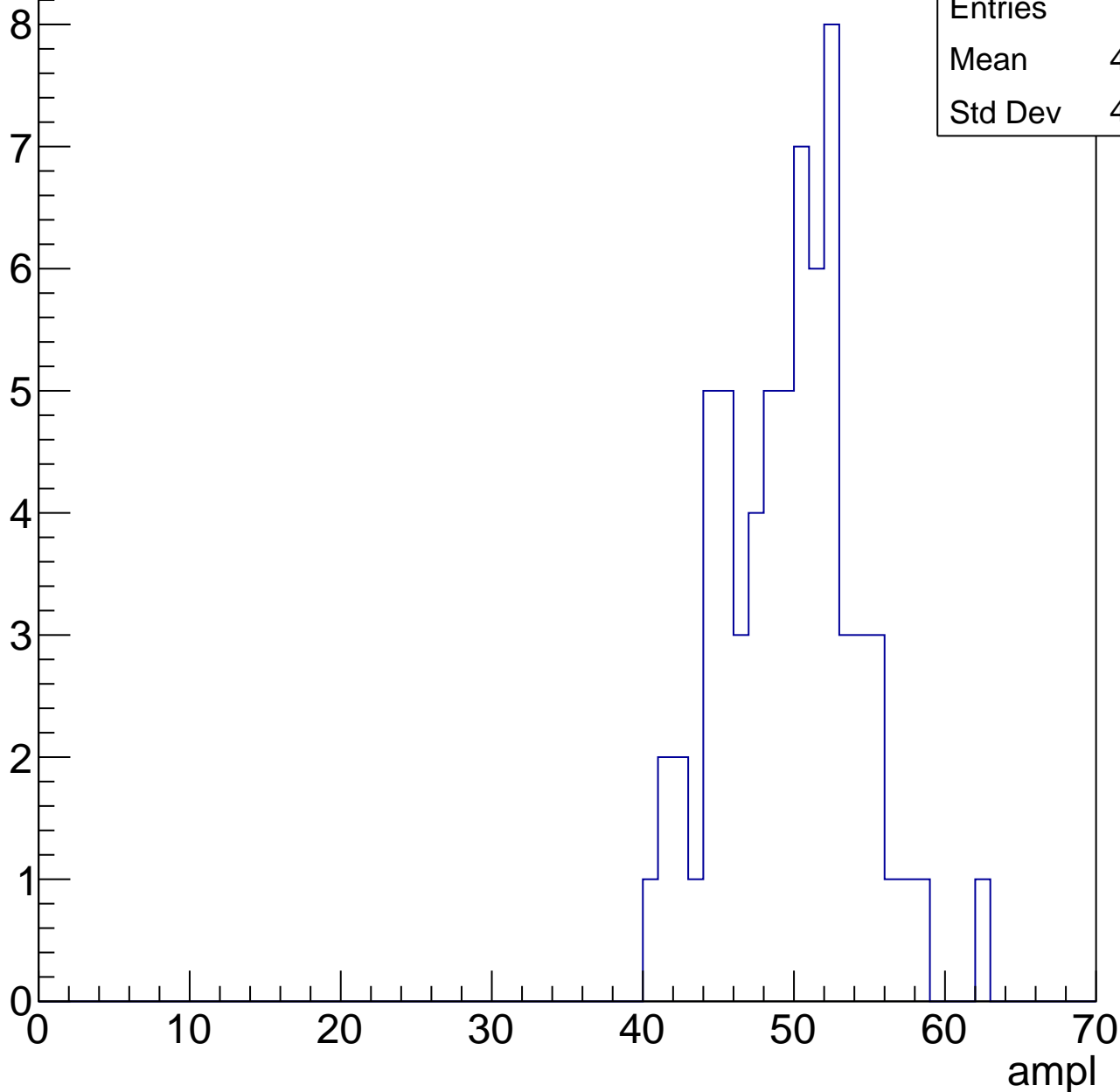


# B1L102S, U5-ch124, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	49.19
Std Dev	4.389

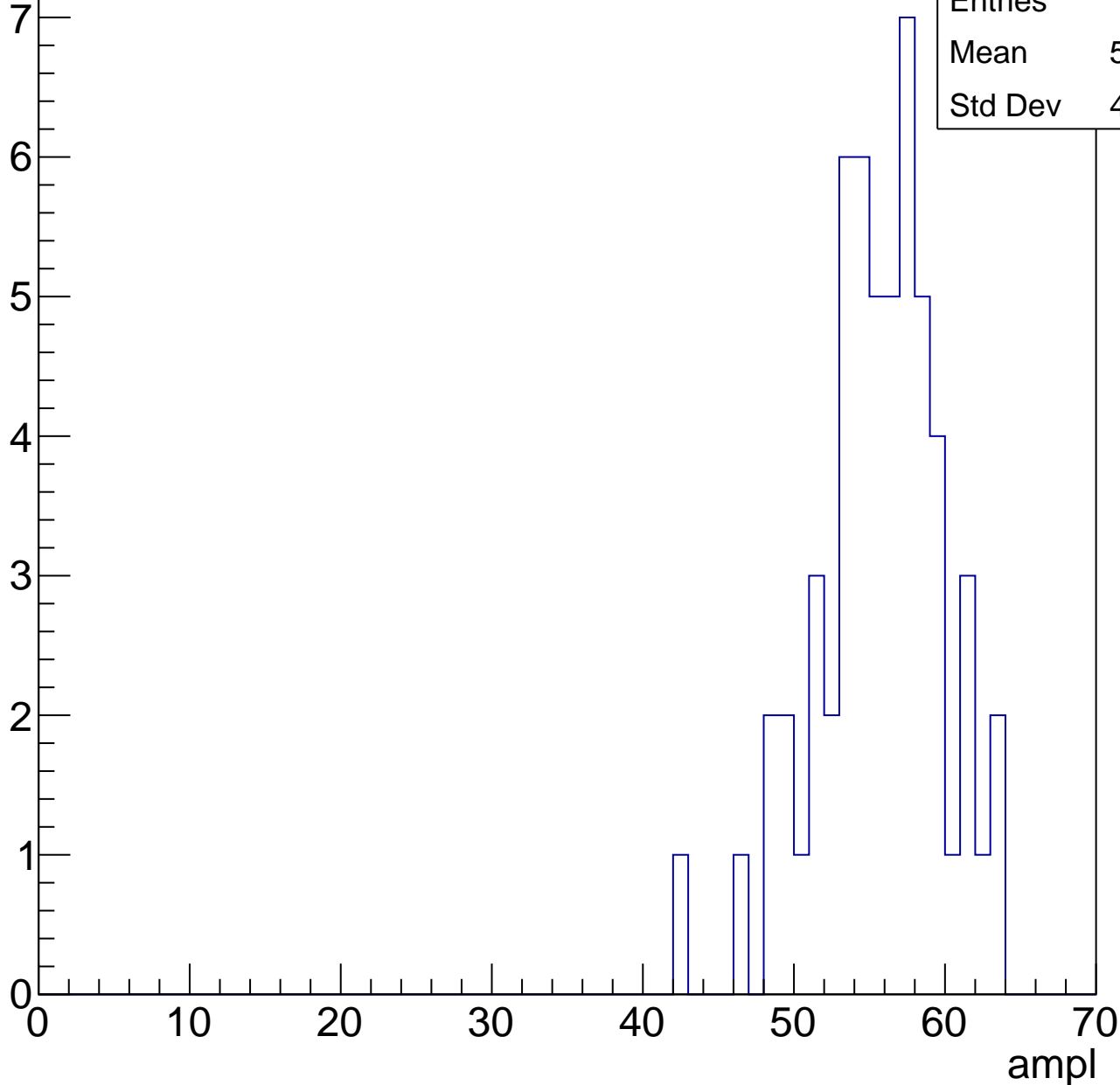


# B1L102S, U5-ch124, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	55.12
Std Dev	4.172

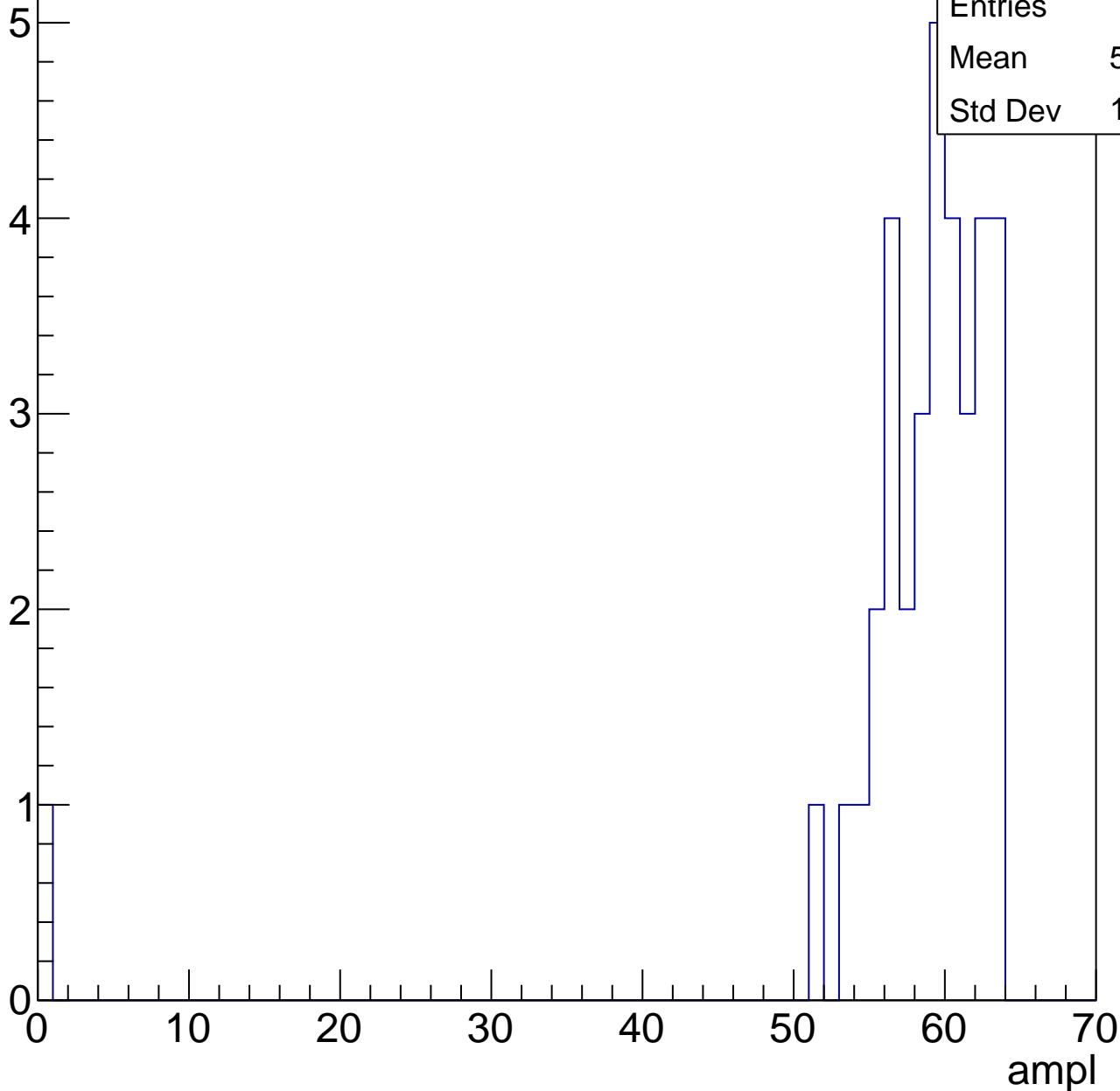


# B1L102S, U5-ch124, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	35
Mean	57.09
Std Dev	10.24

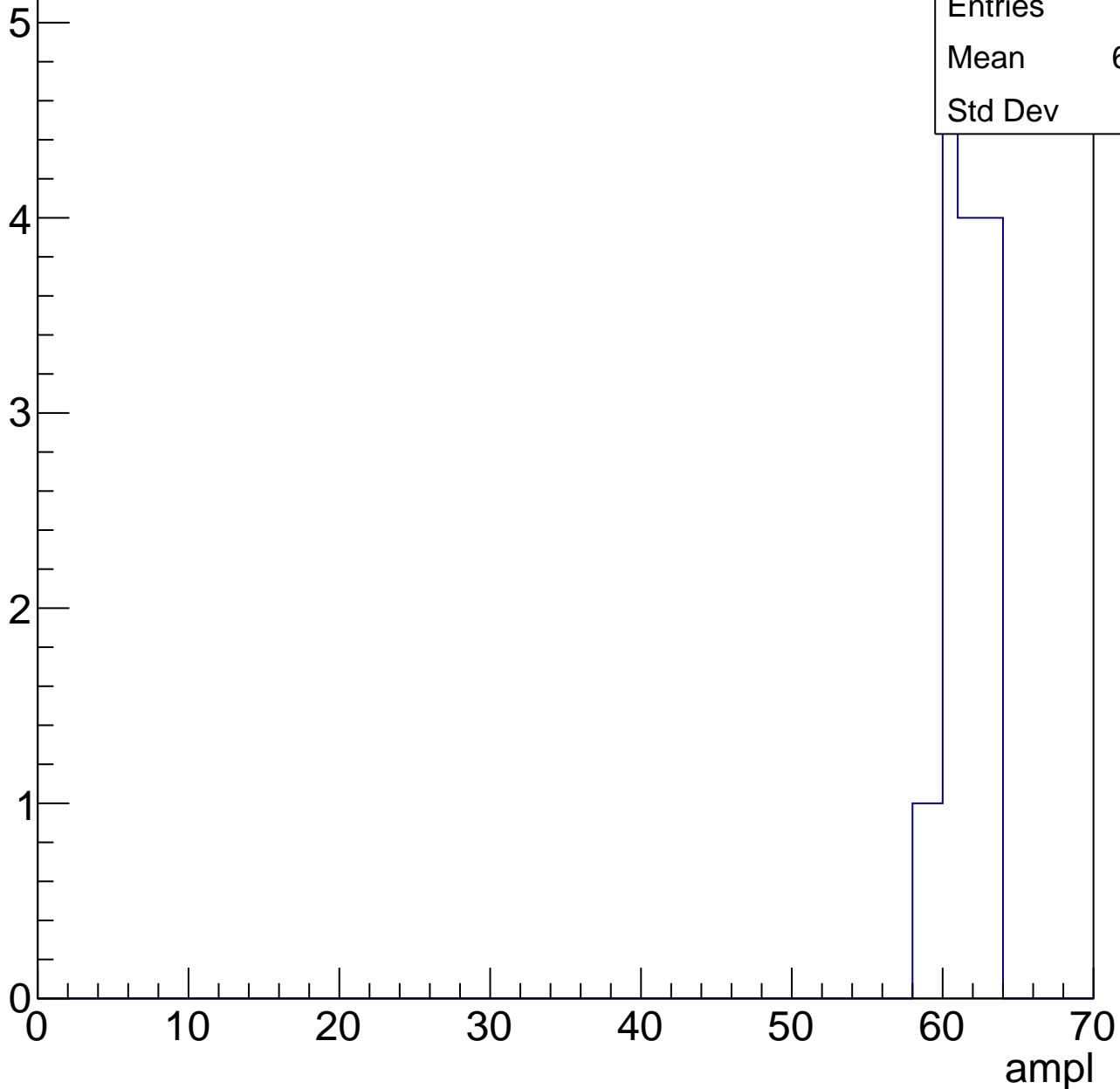


# B1L102S, U5-ch124, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	19
Mean	61.11
Std Dev	1.41





# B1L102S, U5-ch124, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U5-ch125, adc0

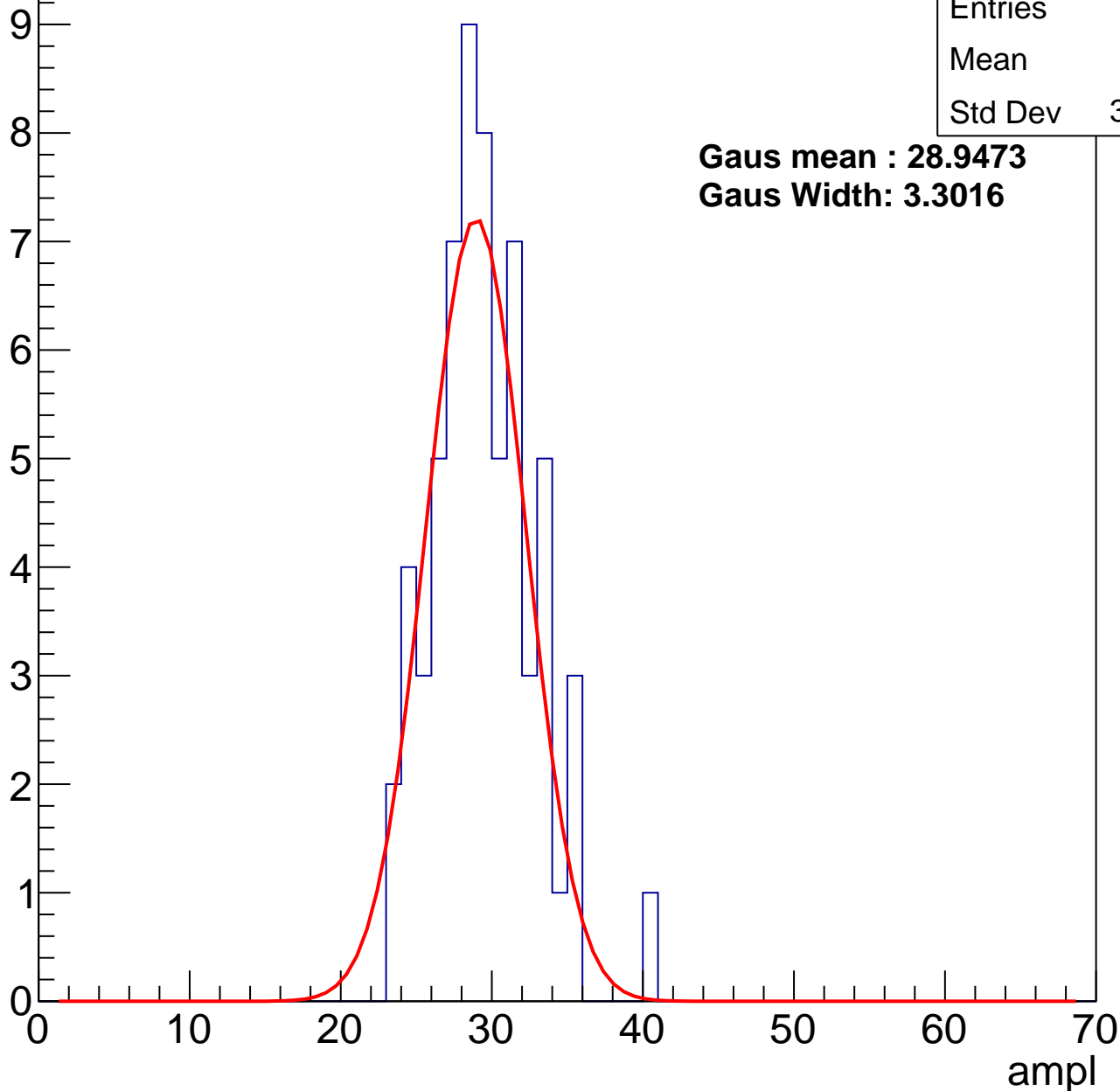
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	29
Std Dev	3.324

**Gaus mean : 28.9473**

**Gaus Width: 3.3016**



# B1L102S, U5-ch125, adc1

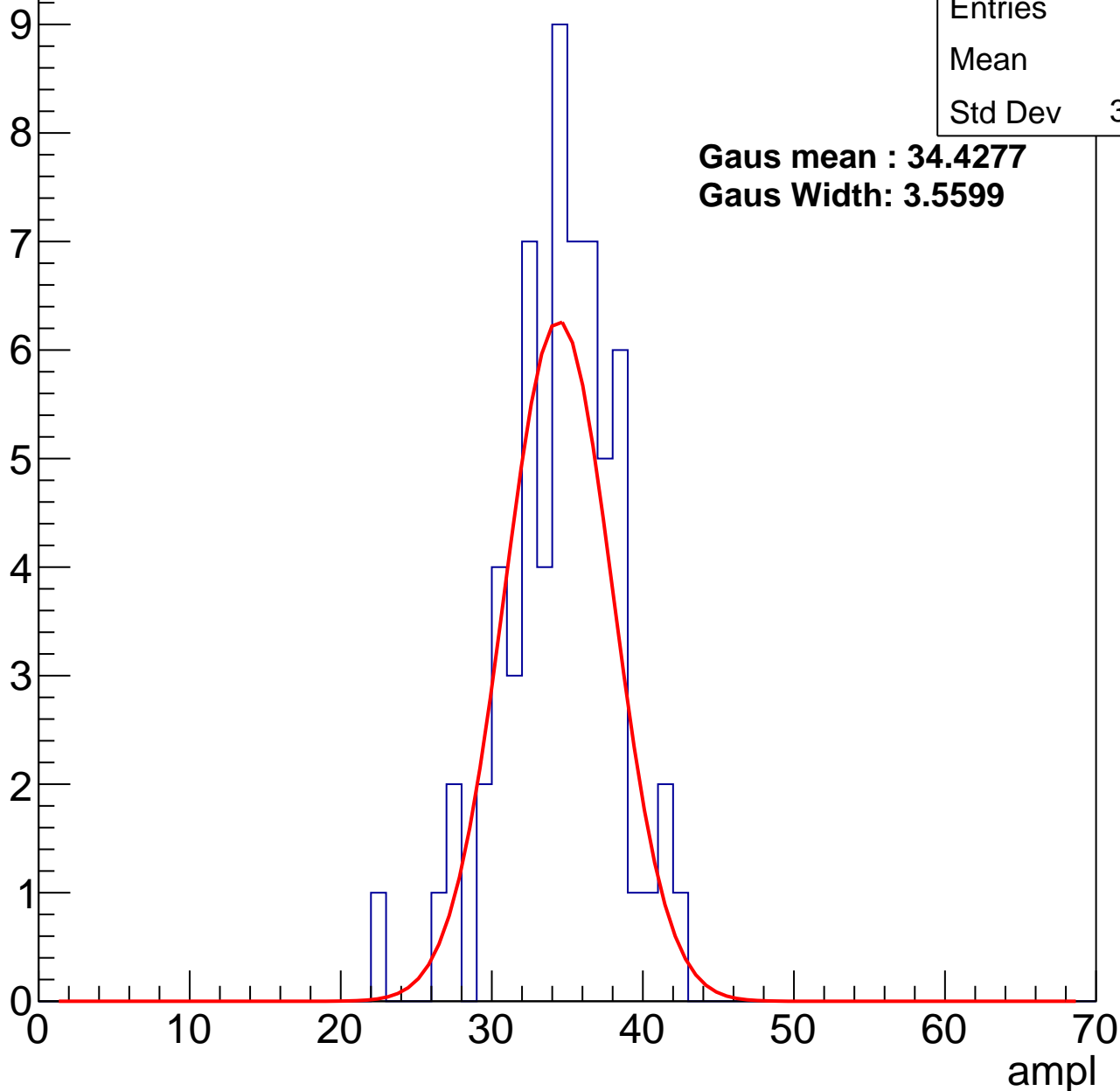
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	34.1
Std Dev	3.732

**Gaus mean : 34.4277**

**Gaus Width: 3.5599**



# B1L102S, U5-ch125, adc2

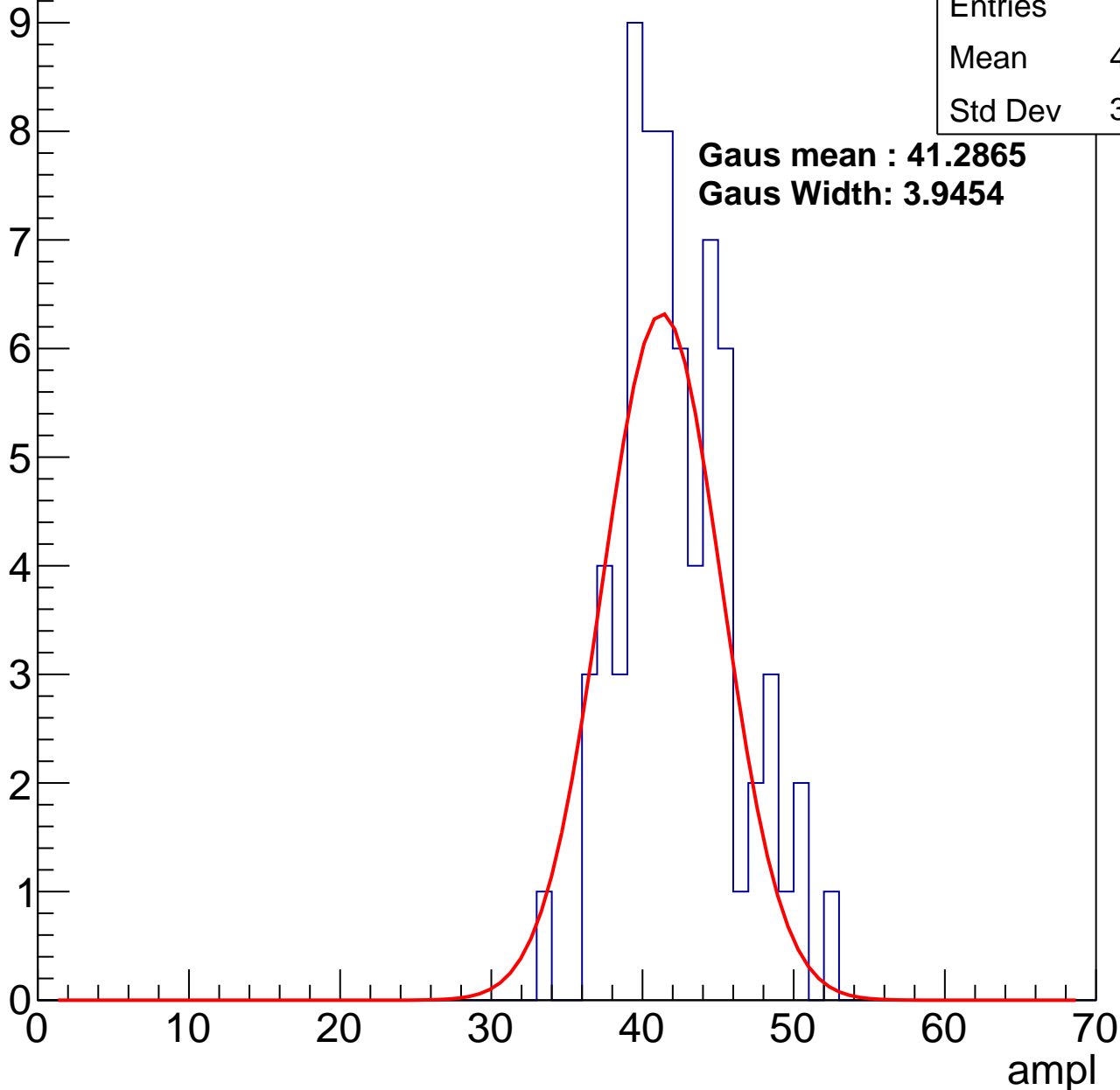
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	41.87
Std Dev	3.795

**Gaus mean : 41.2865**

**Gaus Width: 3.9454**

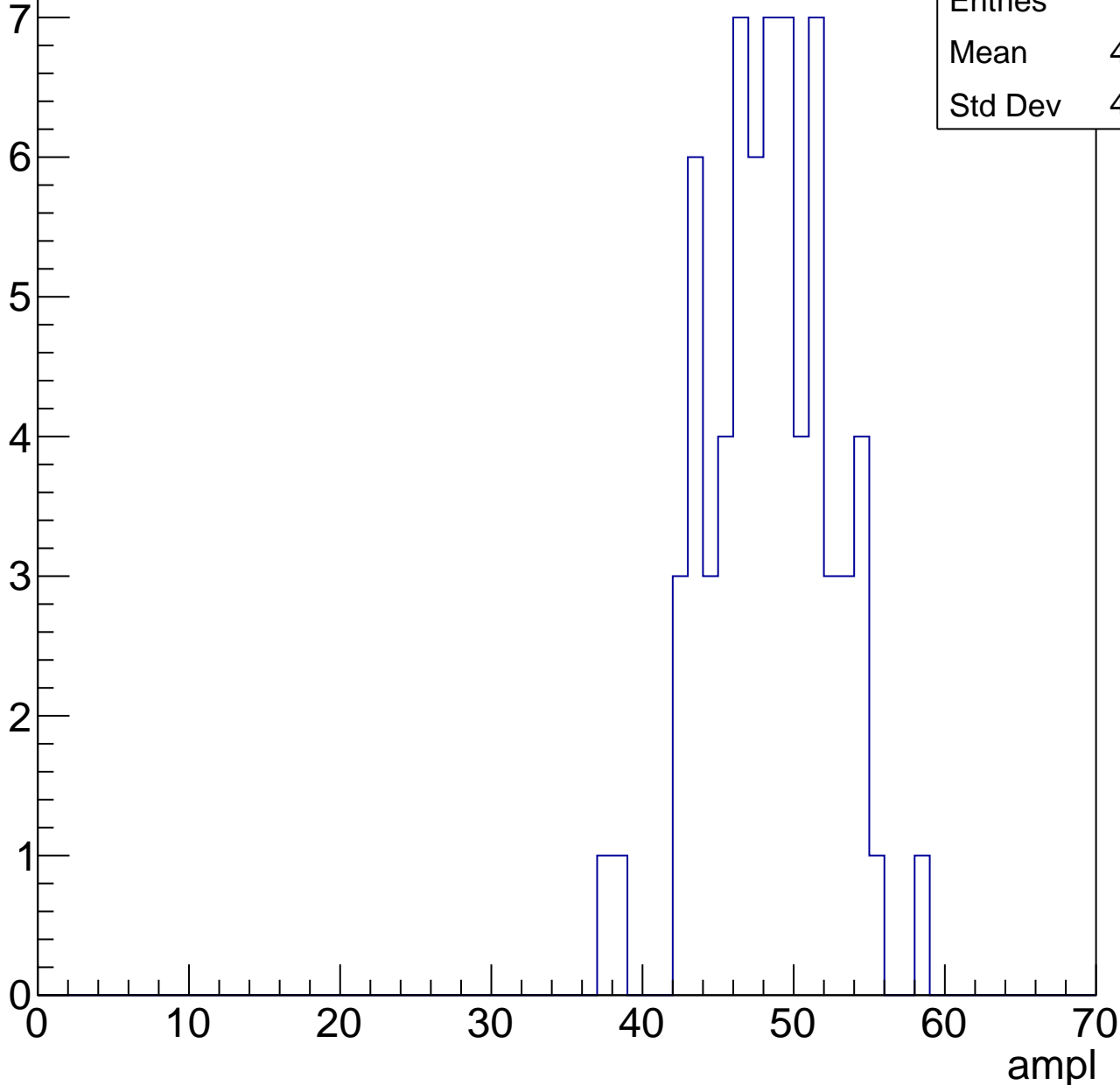


# B1L102S, U5-ch125, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	47.87
Std Dev	4.018

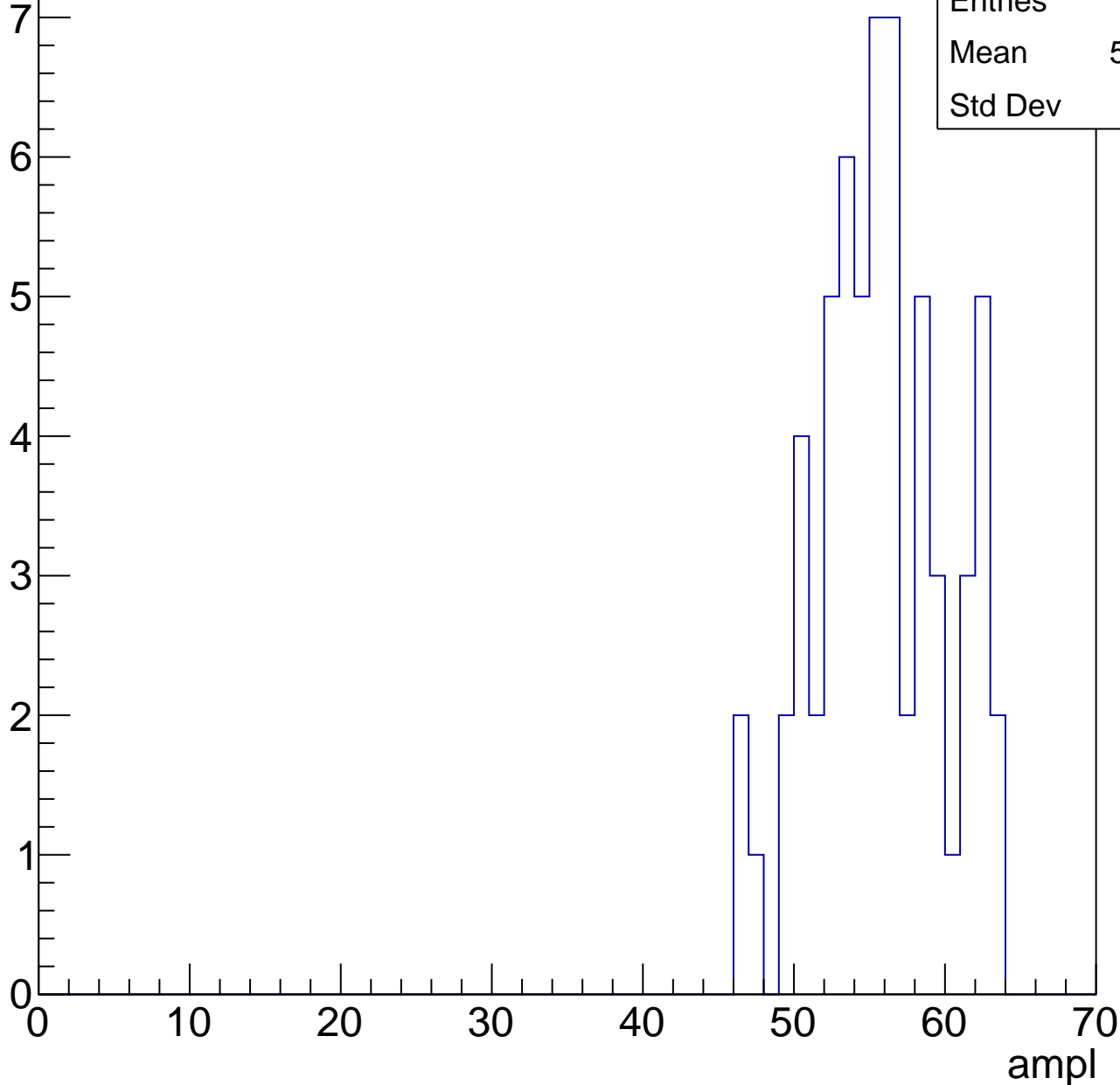


# B1L102S, U5-ch125, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

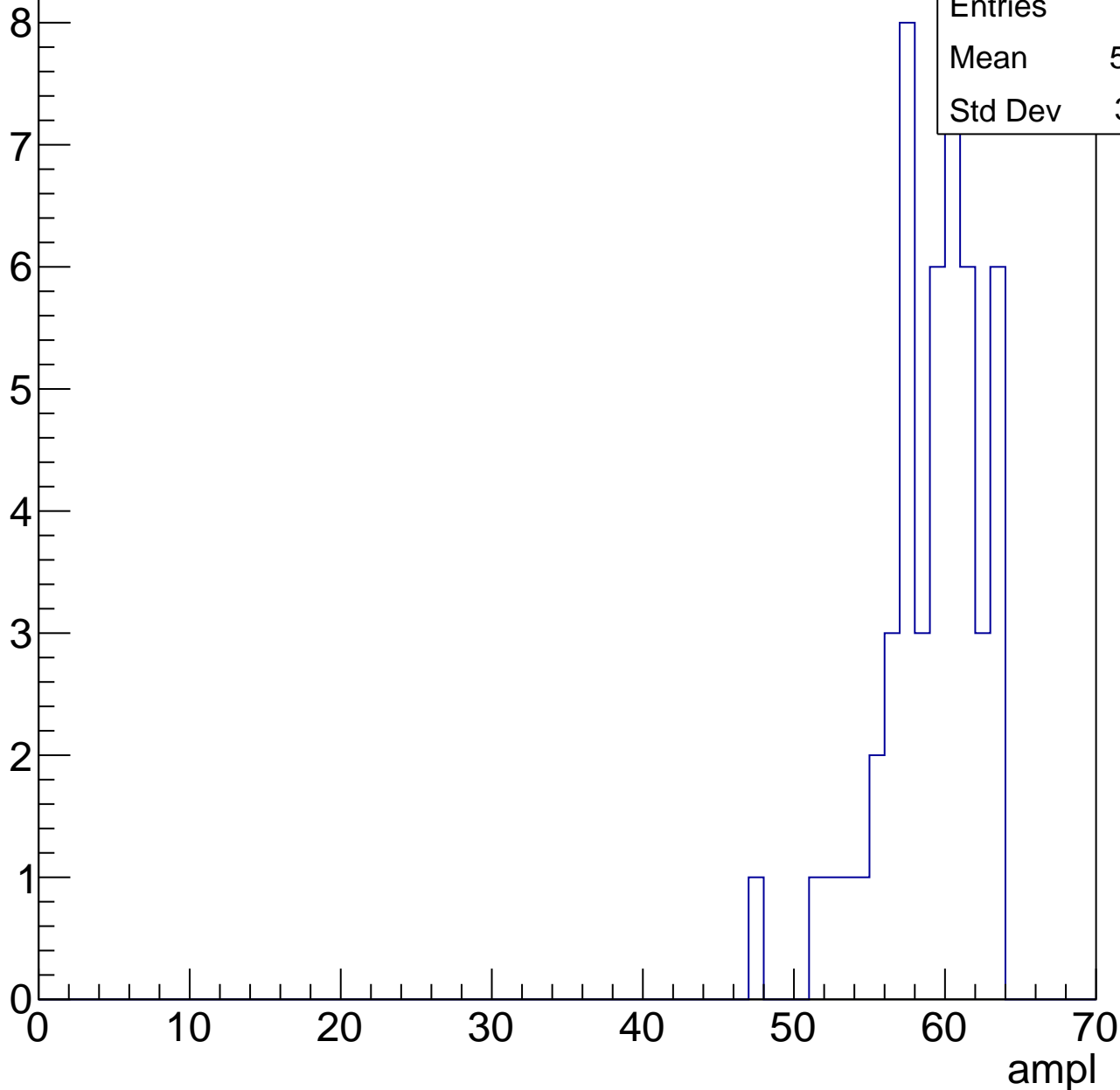
Entries	62
Mean	55.23
Std Dev	4.24



# B1L102S, U5-ch125, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U5-ch125, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

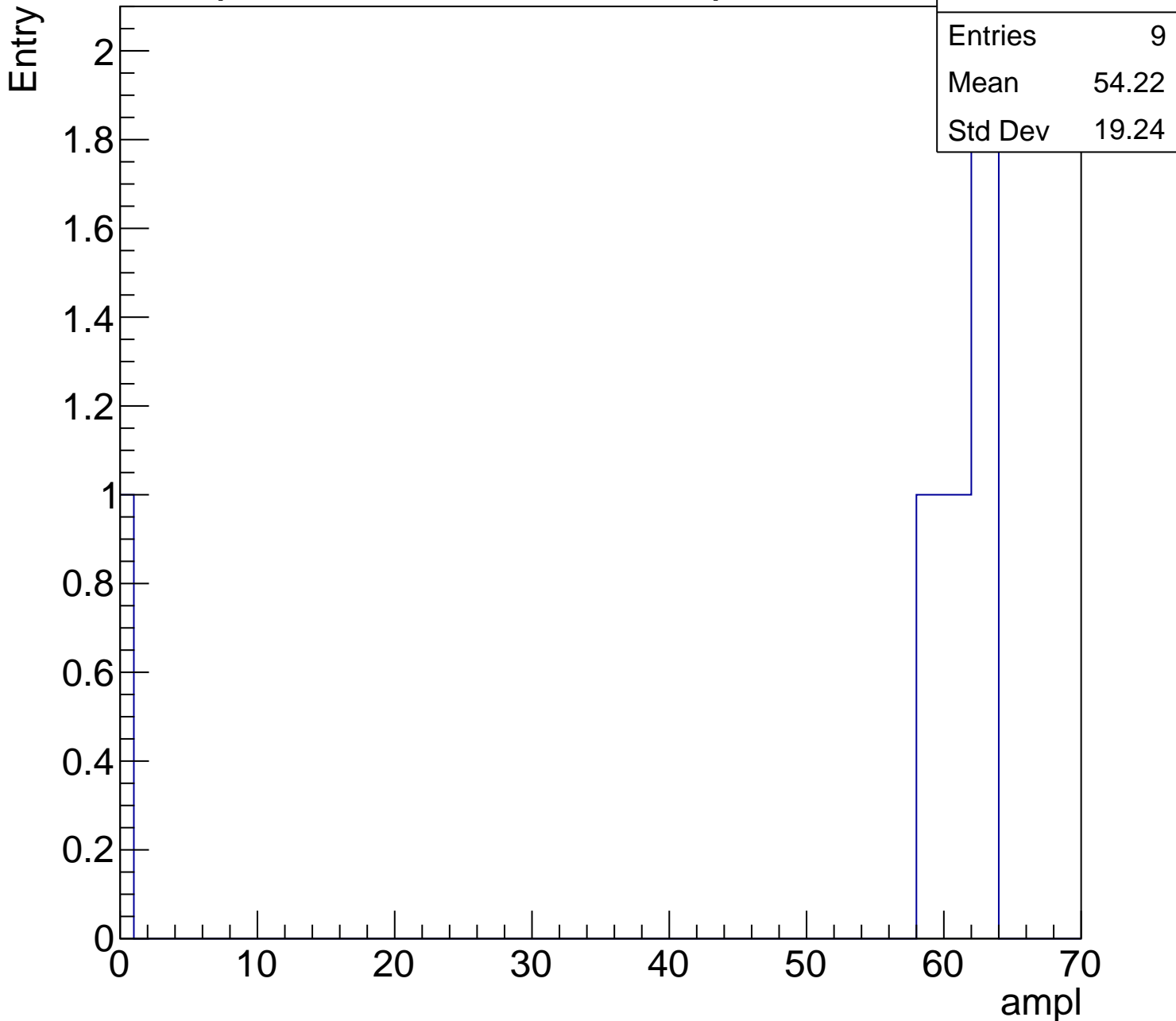
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	9
Mean	54.22
Std Dev	19.24

ampl

0 10 20 30 40 50 60 70





# B1L102S, U5-ch125, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U5-ch126, adc0

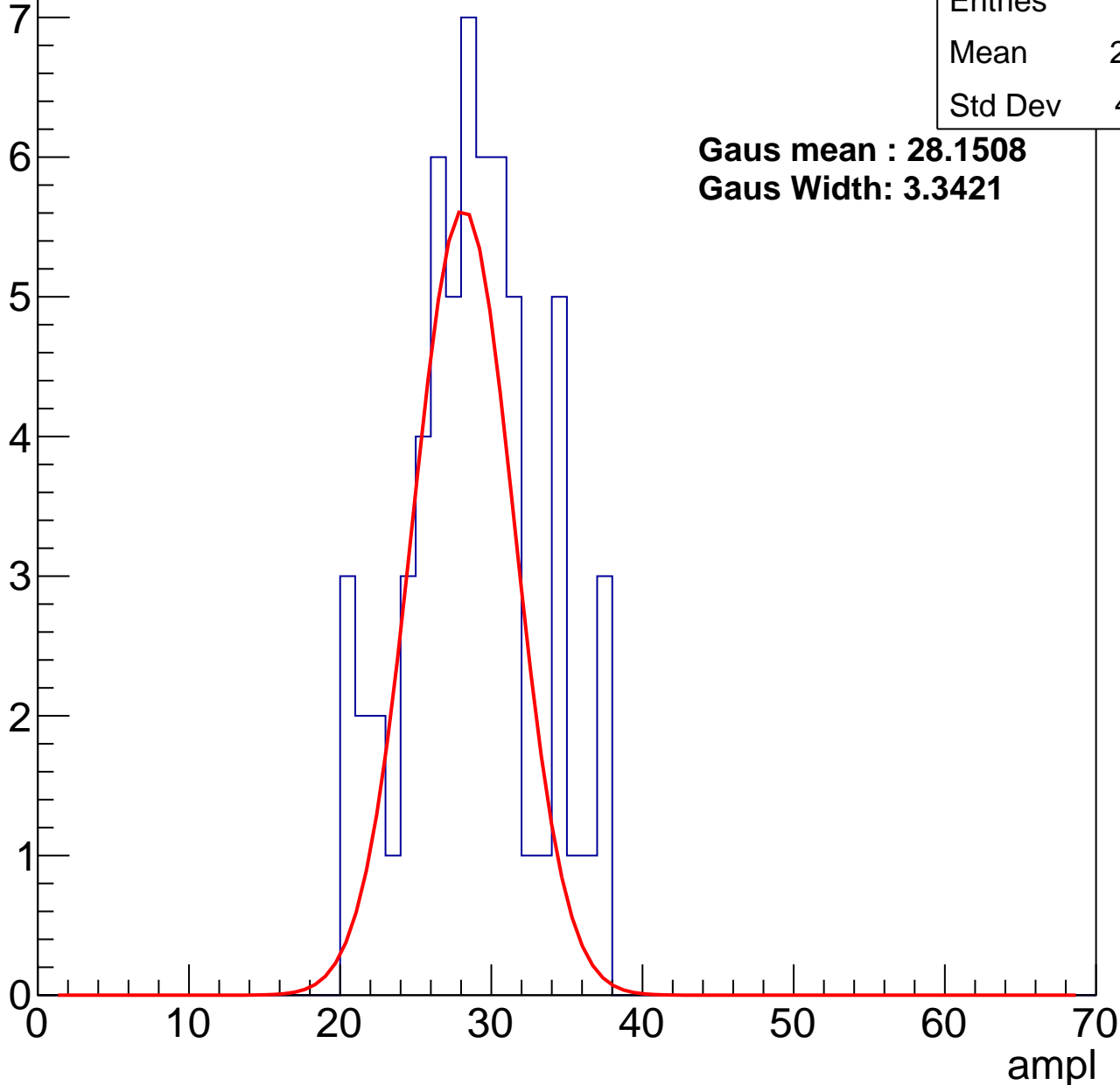
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	28.29
Std Dev	4.301

**Gaus mean : 28.1508**

**Gaus Width: 3.3421**



# B1L102S, U5-ch126, adc1

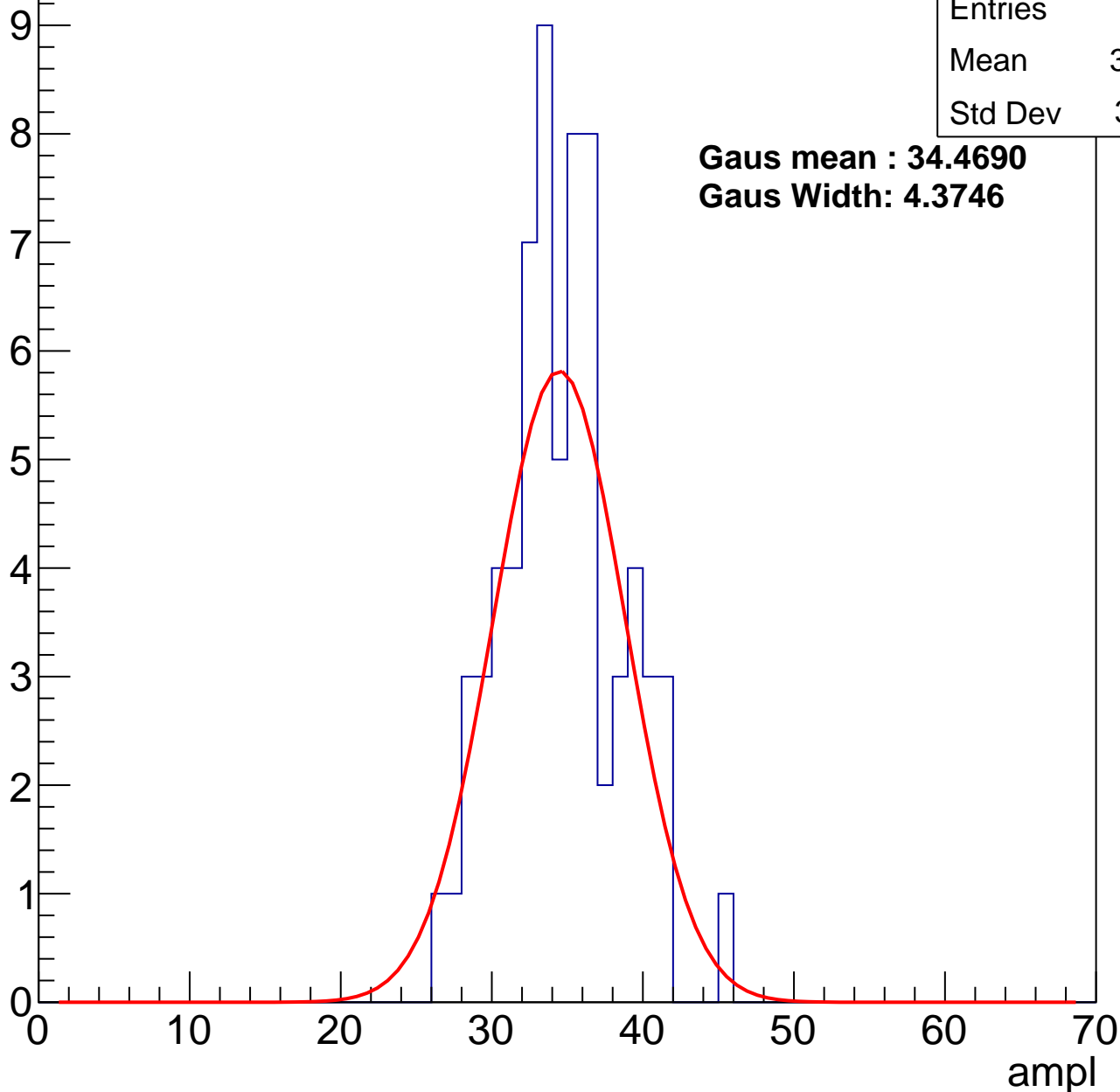
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	34.19
Std Dev	3.831

**Gaus mean : 34.4690**

**Gaus Width: 4.3746**



# B1L102S, U5-ch126, adc2

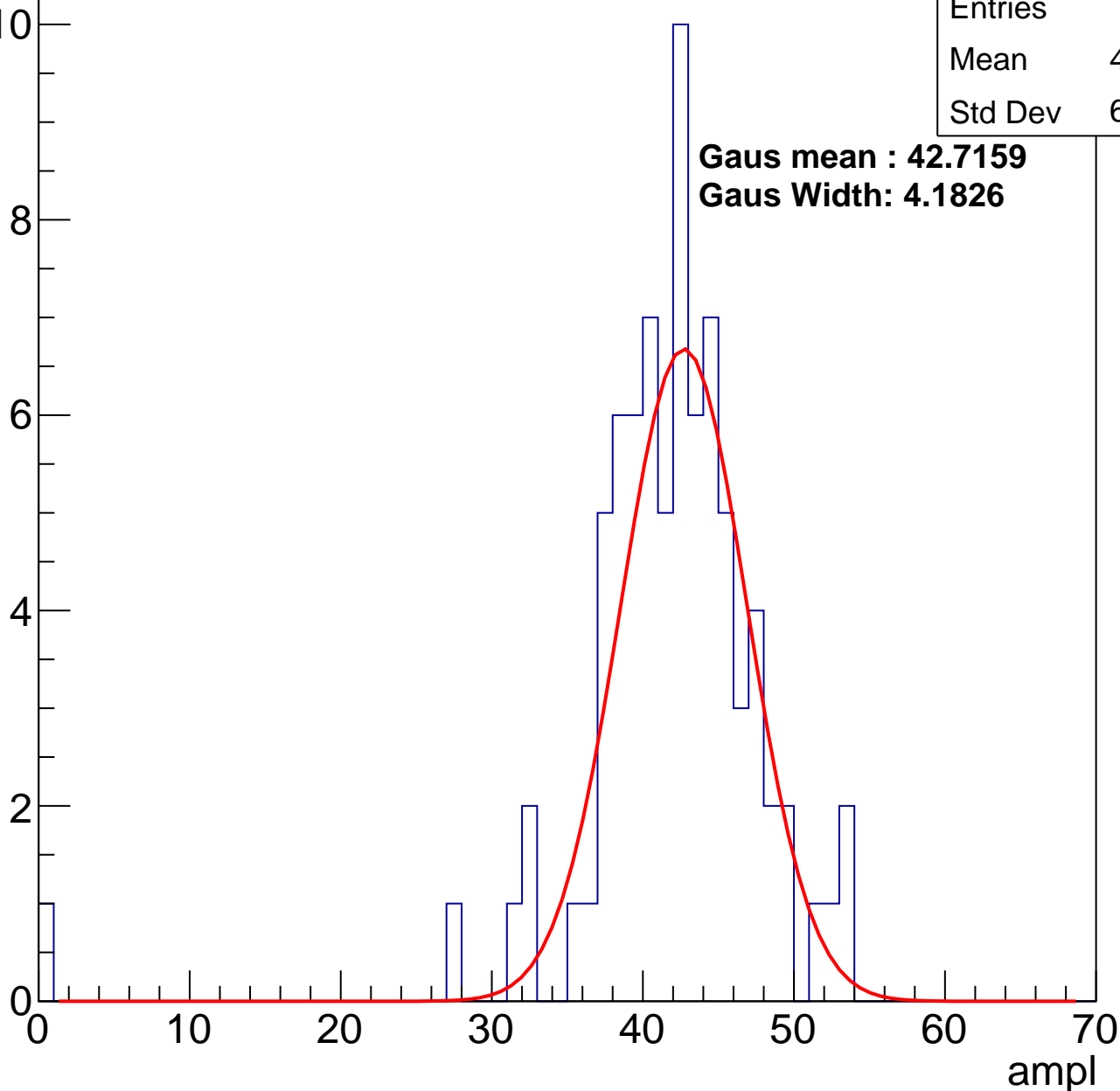
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	79
Mean	41.33
Std Dev	6.644

**Gaus mean : 42.7159**

**Gaus Width: 4.1826**

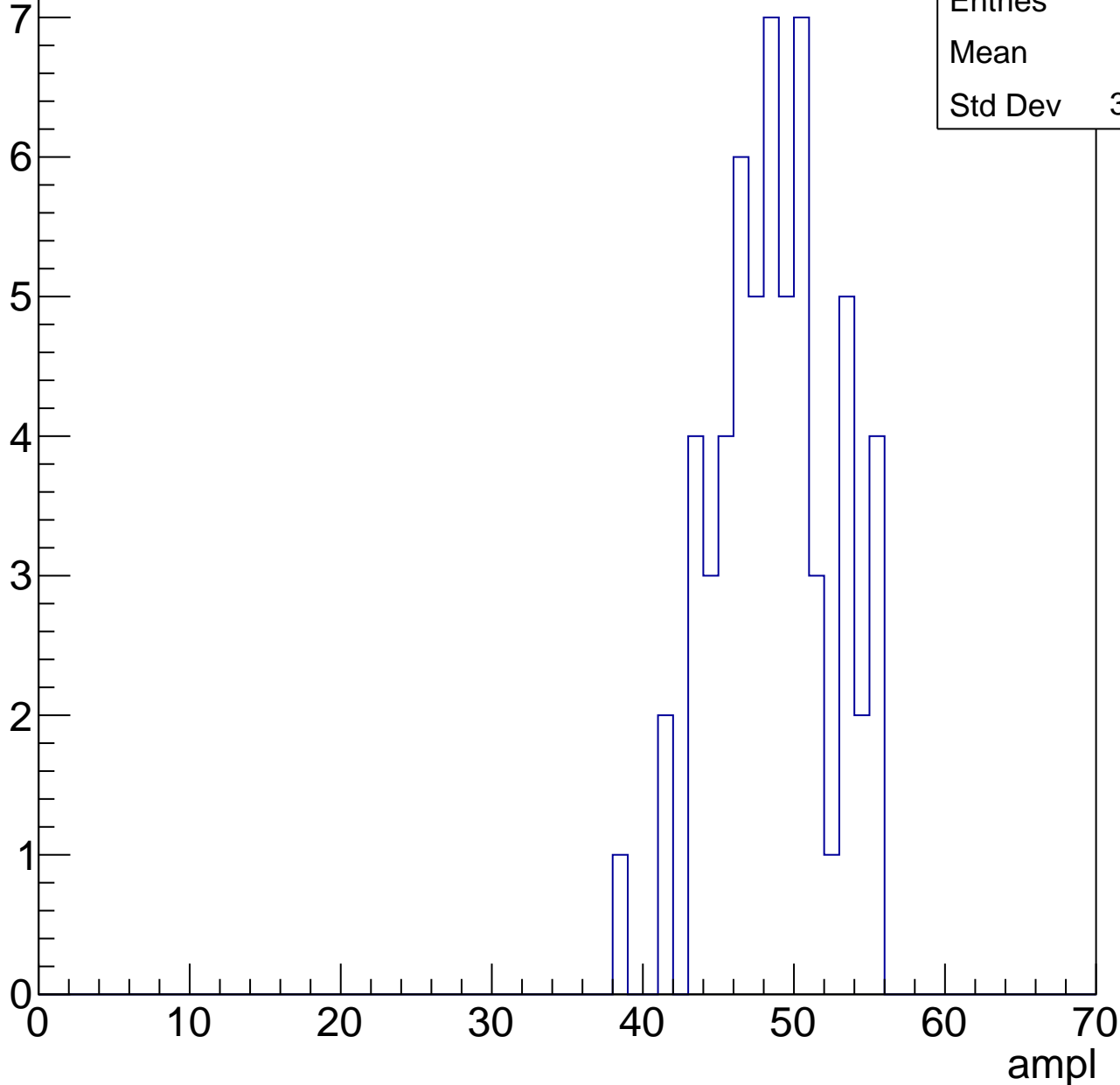


# B1L102S, U5-ch126, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	48.2
Std Dev	3.857

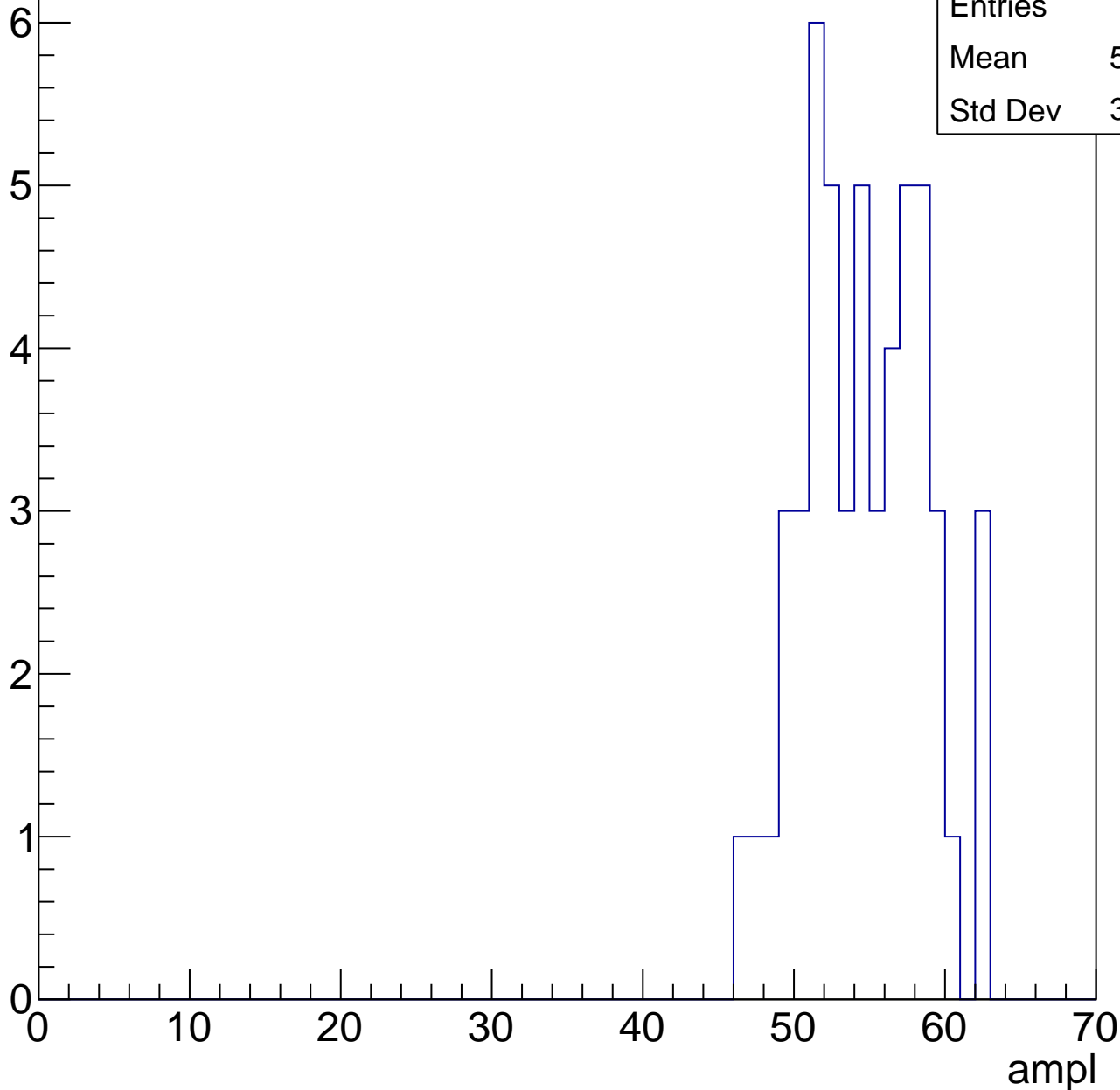


# B1L102S, U5-ch126, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	54.23
Std Dev	3.906

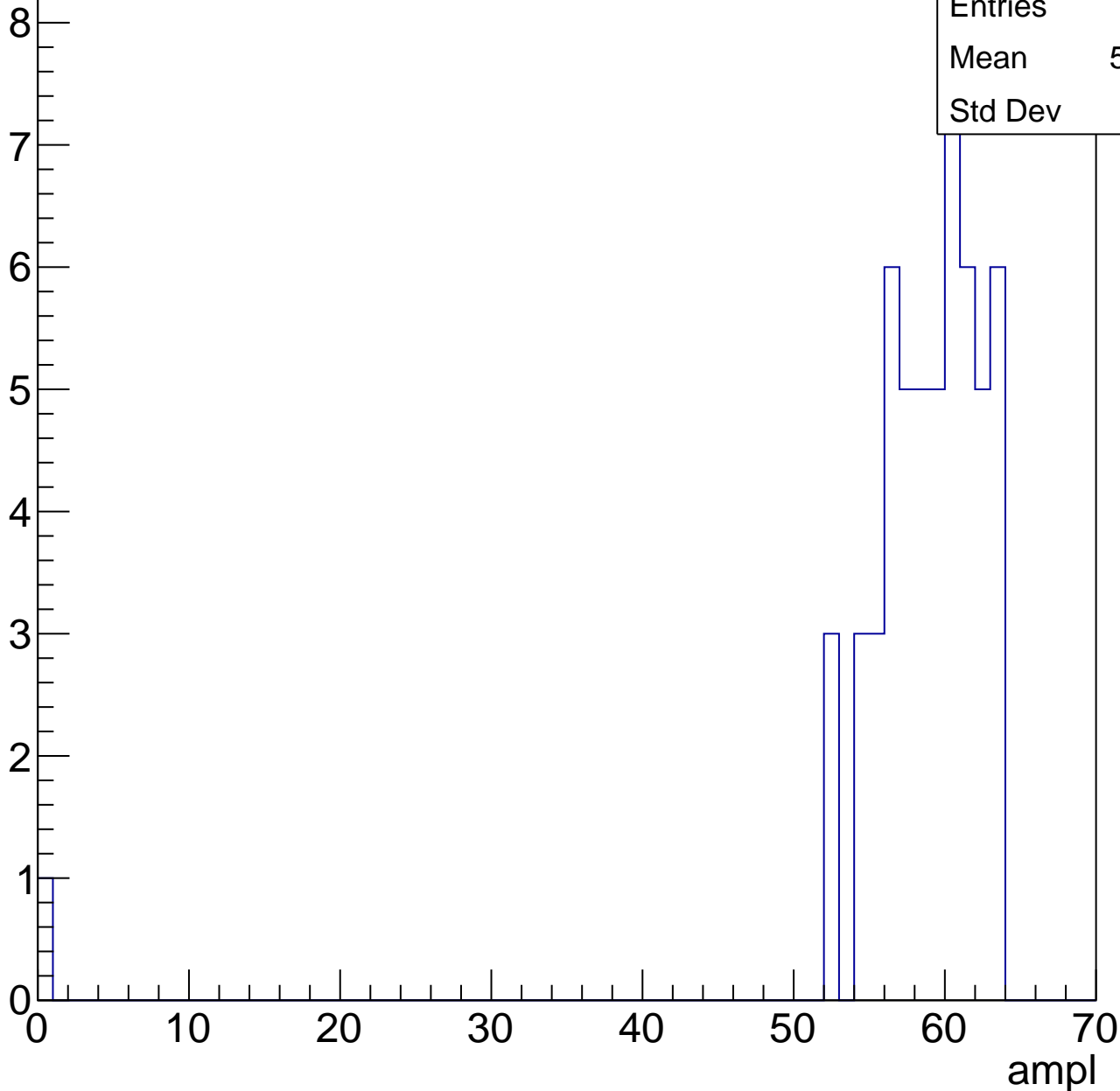


# B1L102S, U5-ch126, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

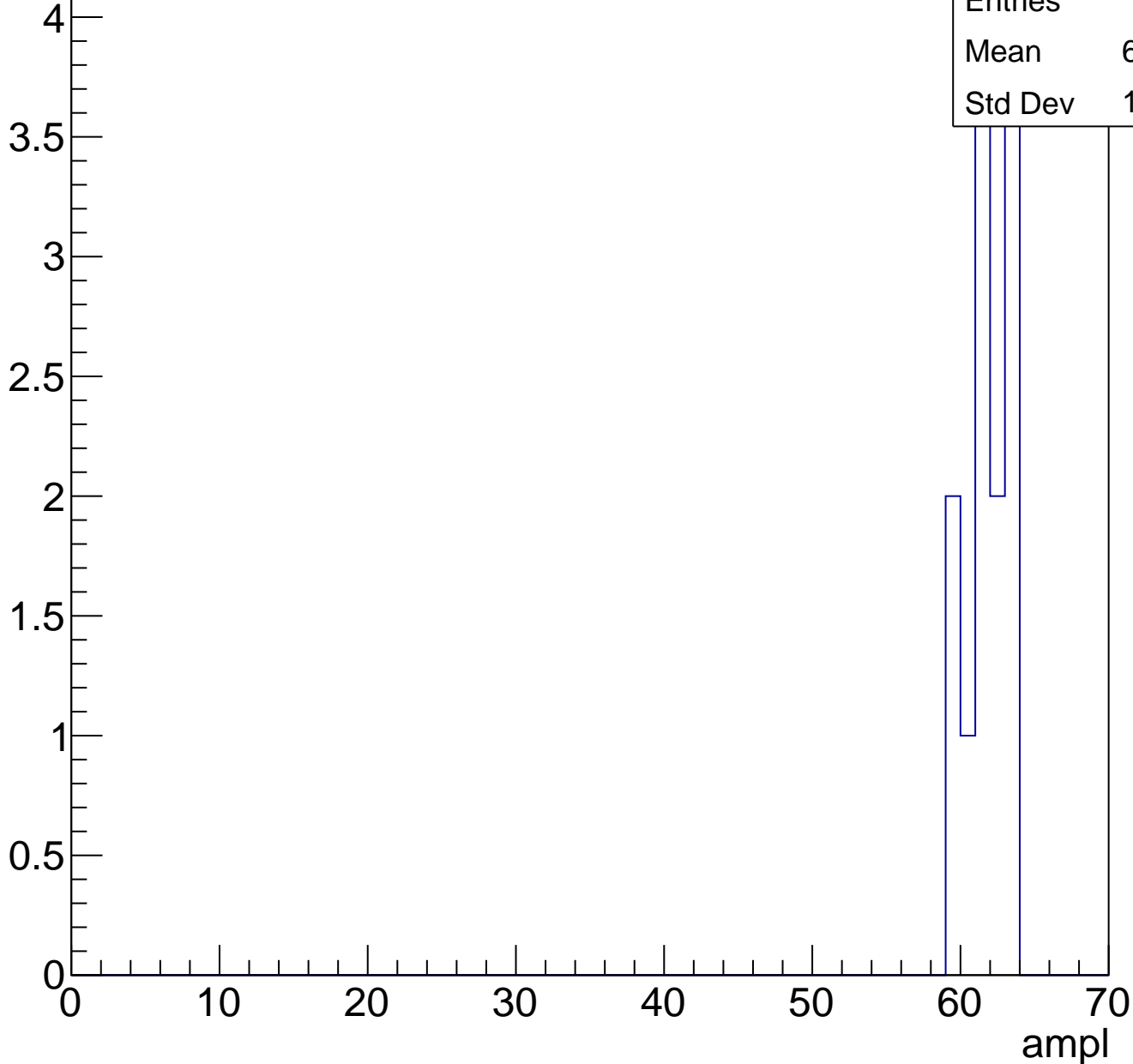
Entries	56
Mean	57.55
Std Dev	8.33



# B1L102S, U5-ch126, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U5-ch126, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	3
Mean	6
Std Dev	8.485

# B1L102S, U5-ch127, adc0

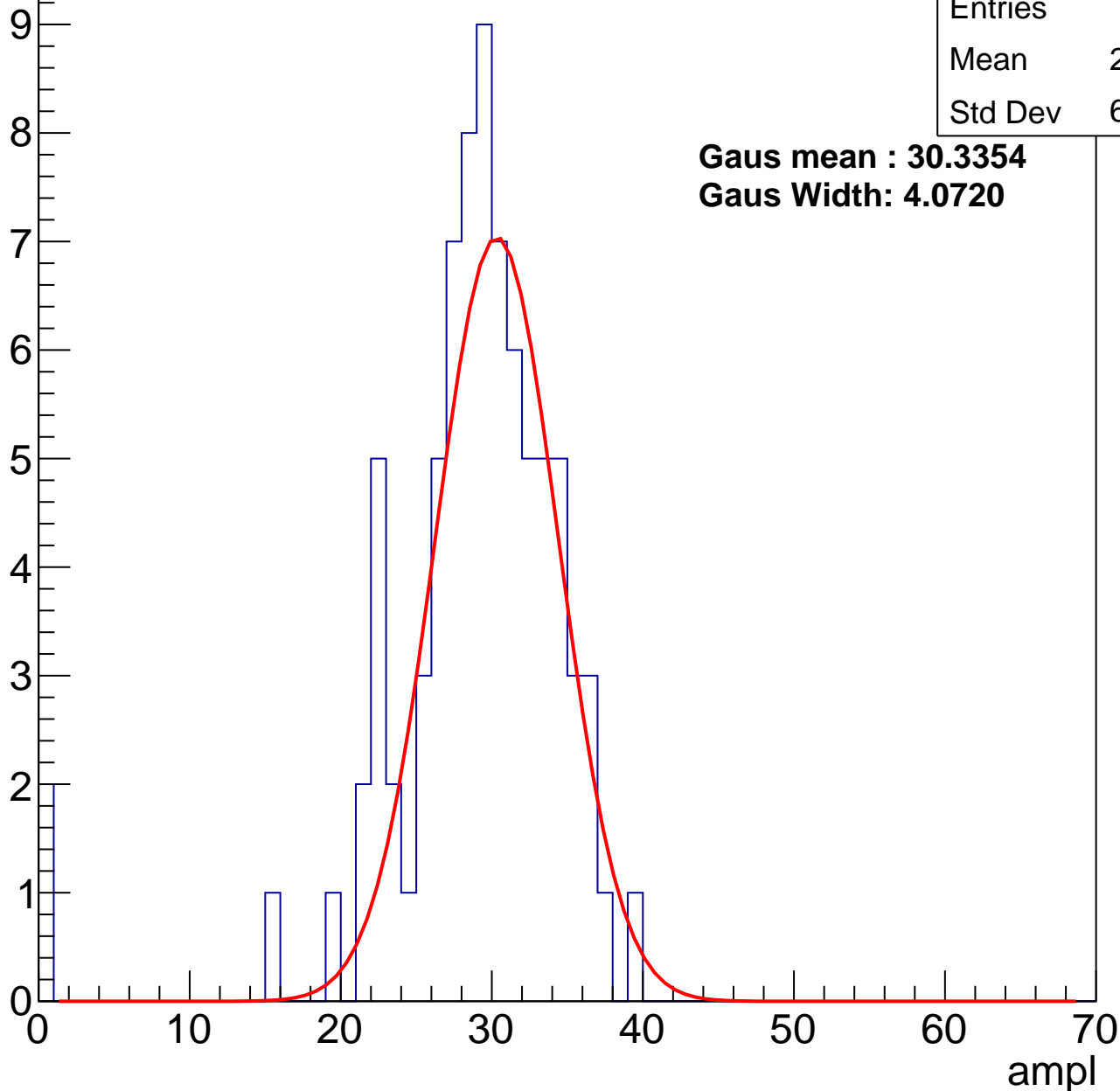
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	82
Mean	28.23
Std Dev	6.275

**Gaus mean : 30.3354**

**Gaus Width: 4.0720**



# B1L102S, U5-ch127, adc1

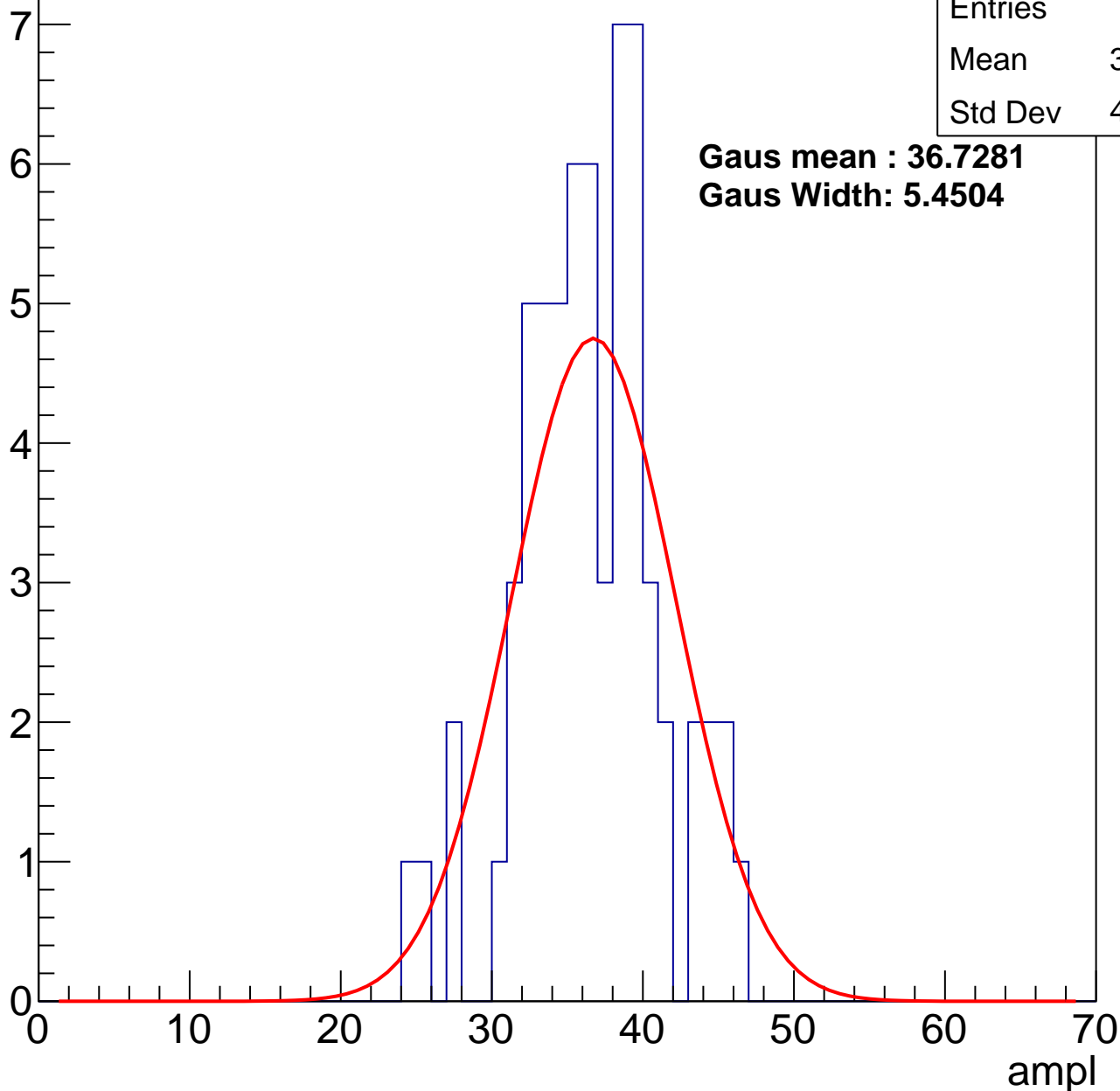
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	36.08
Std Dev	4.624

**Gaus mean : 36.7281**

**Gaus Width: 5.4504**



# B1L102S, U5-ch127, adc2

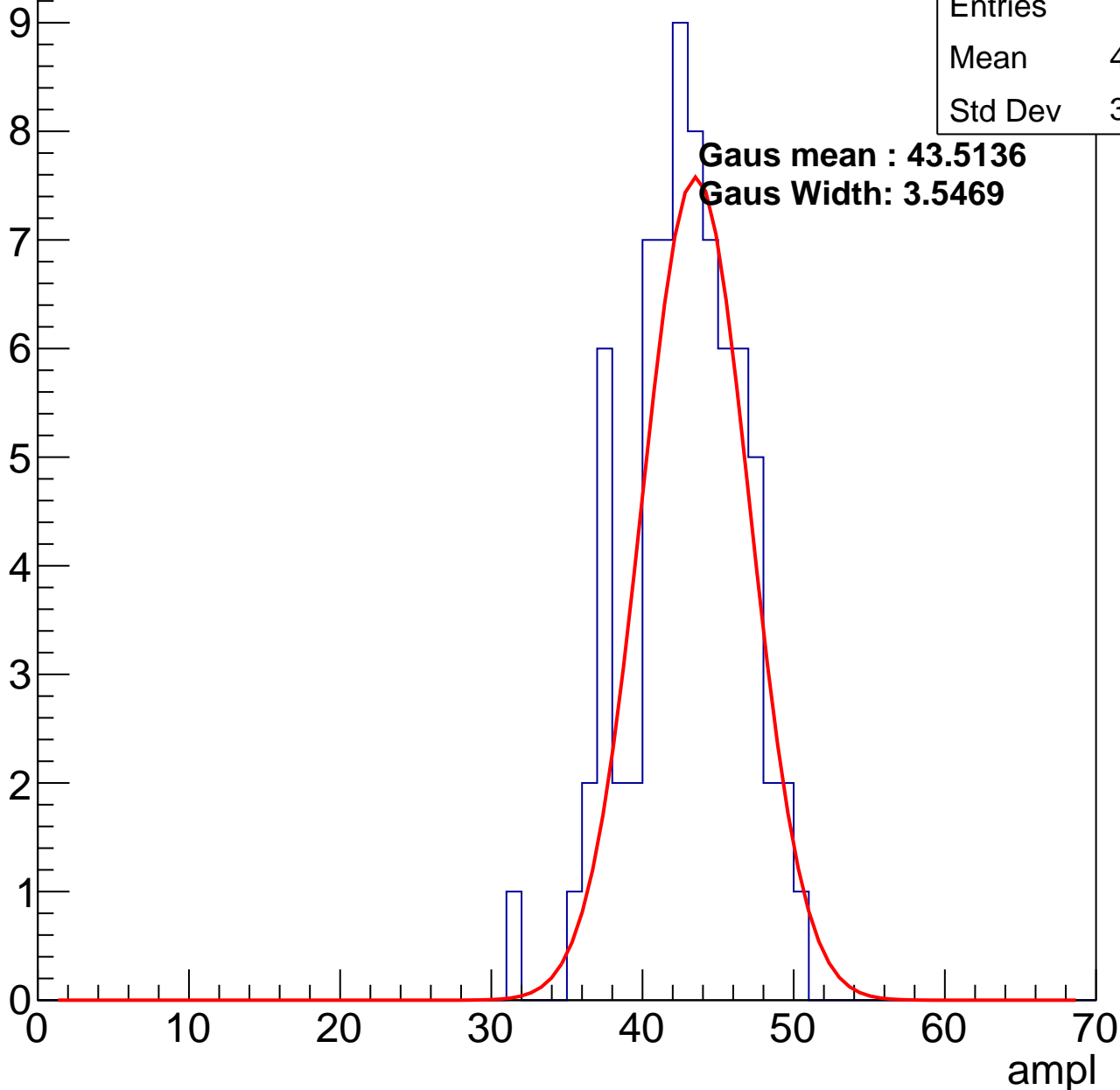
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	42.38
Std Dev	3.697

**Gaus mean : 43.5136**

**Gaus Width: 3.5469**

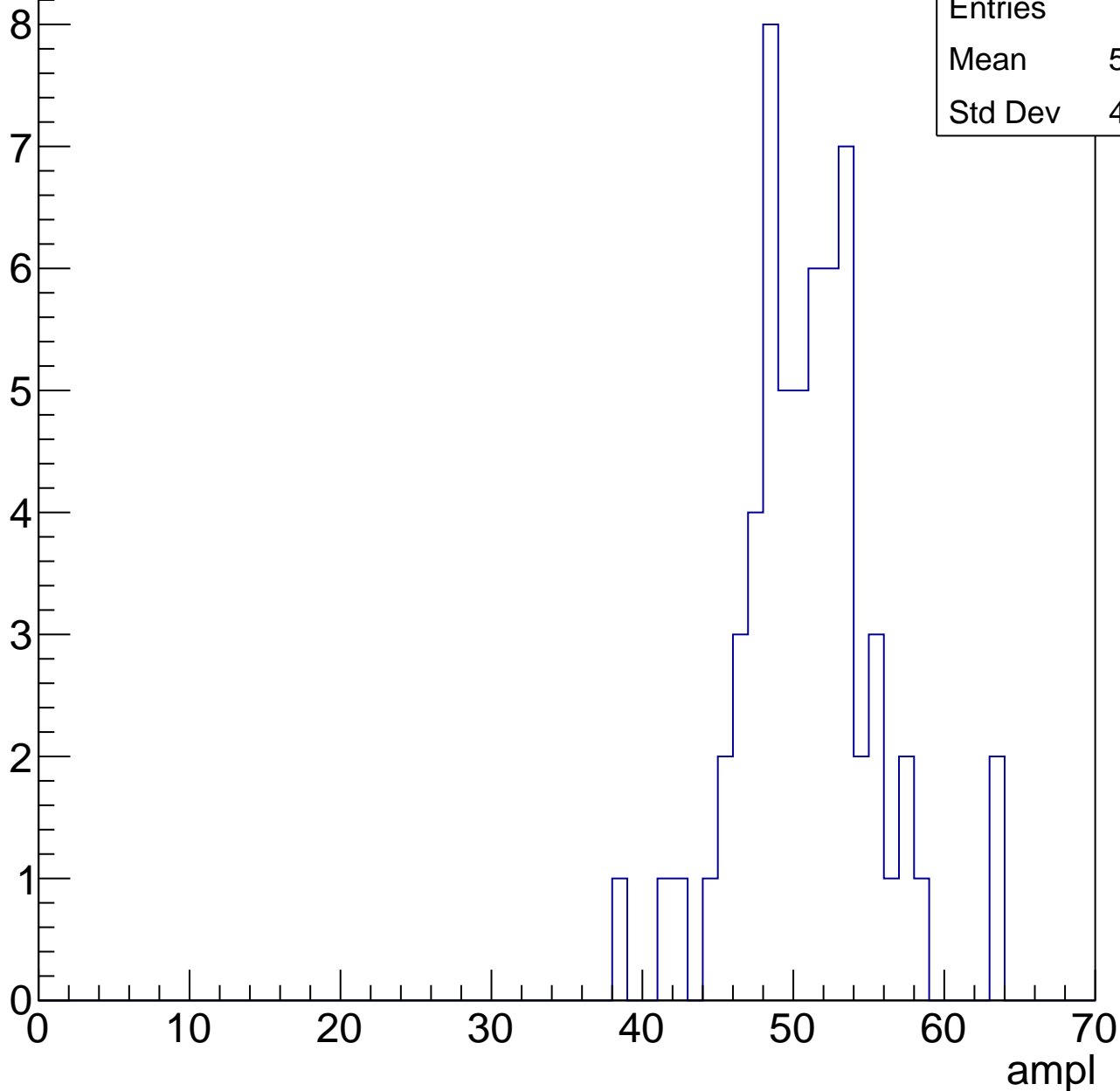


# B1L102S, U5-ch127, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	50.43
Std Dev	4.474

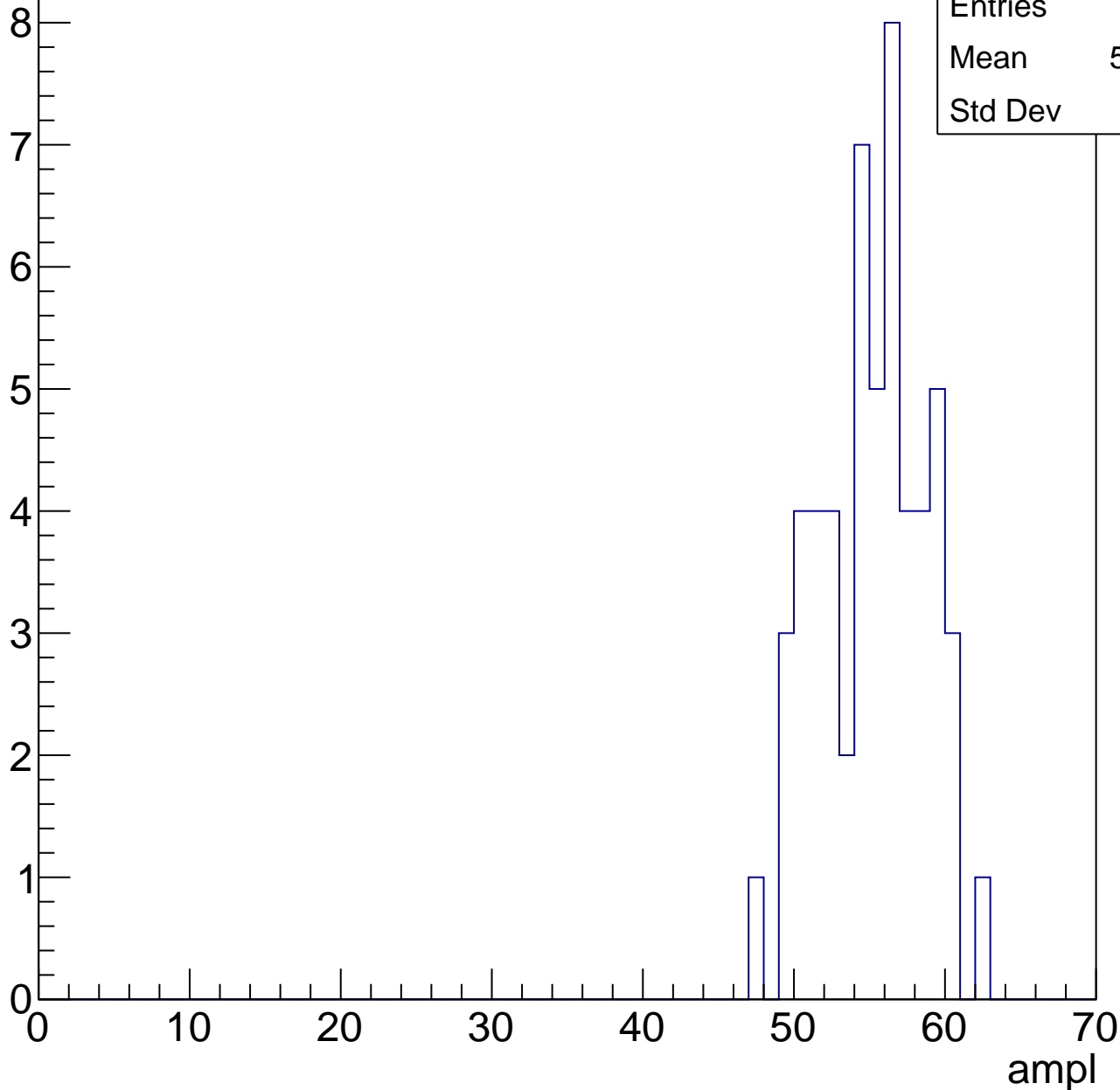


# B1L102S, U5-ch127, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	54.73
Std Dev	3.43

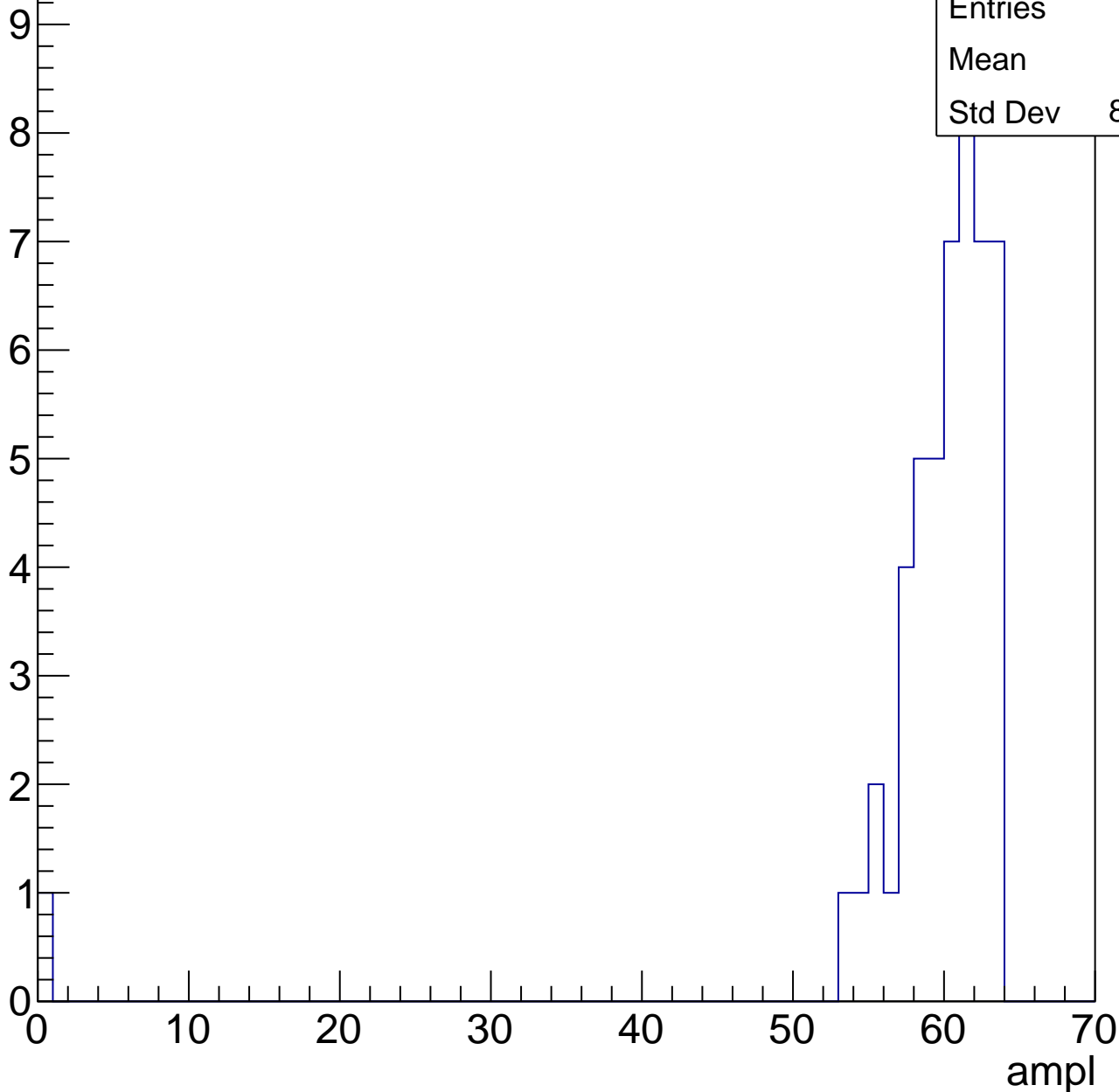


# B1L102S, U5-ch127, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	58.6
Std Dev	8.734



# B1L102S, U5-ch127, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	62
Std Dev	0.7071

ampl

0 10 20 30 40 50 60 70



# B1L102S, U5-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U5-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0