



# B0L100S, U18-ch0

calib\_packv5\_042523\_0143.root, FC#6, port A1

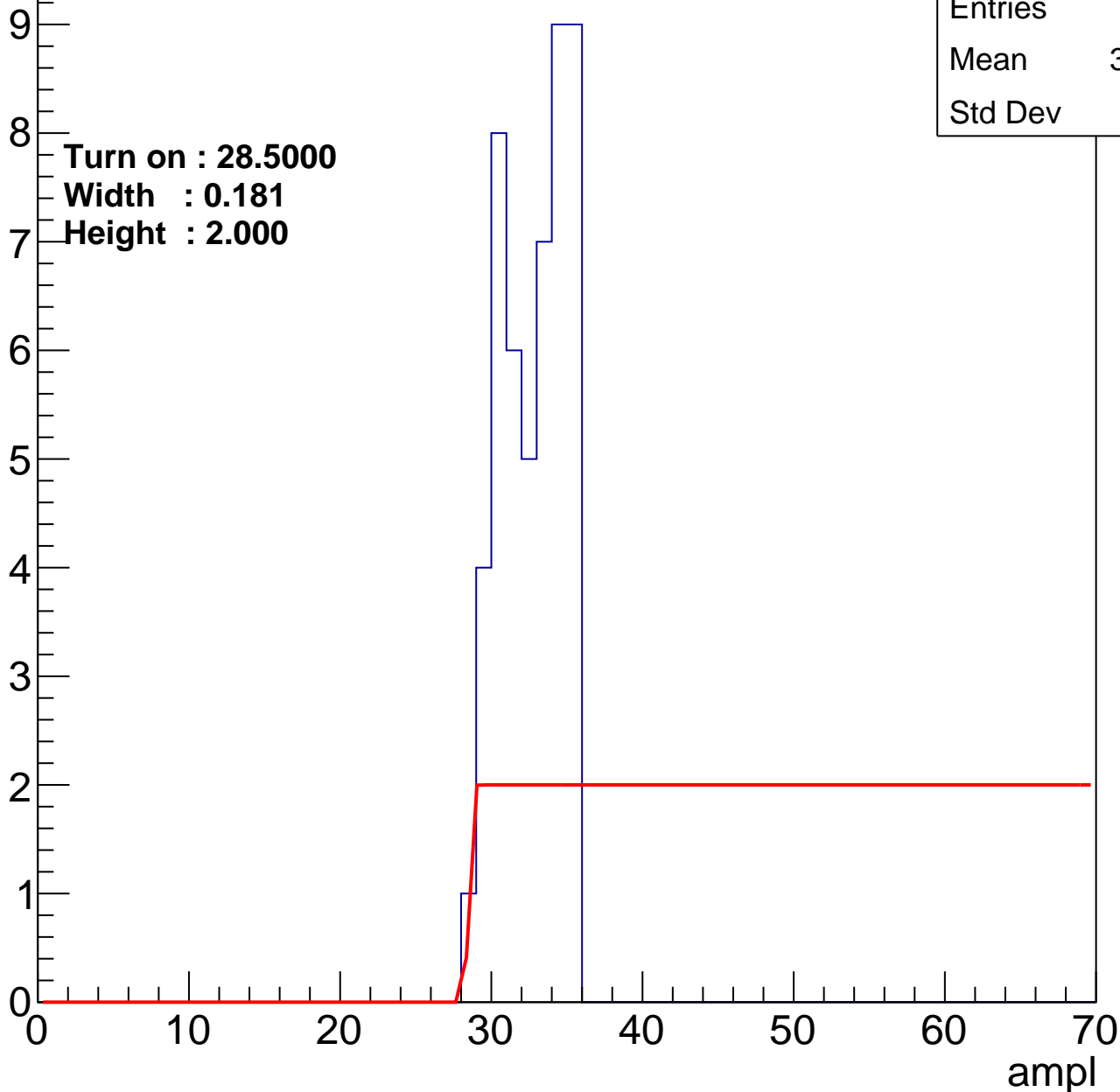
Entry

Entries	49
Mean	32.29
Std Dev	2.07

Turn on : 28.5000

Width : 0.181

Height : 2.000



# B0L100S, U18-ch1

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U18-ch2

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U18-ch3

calib\_packv5\_042523\_0143.root, FC#6, port A1

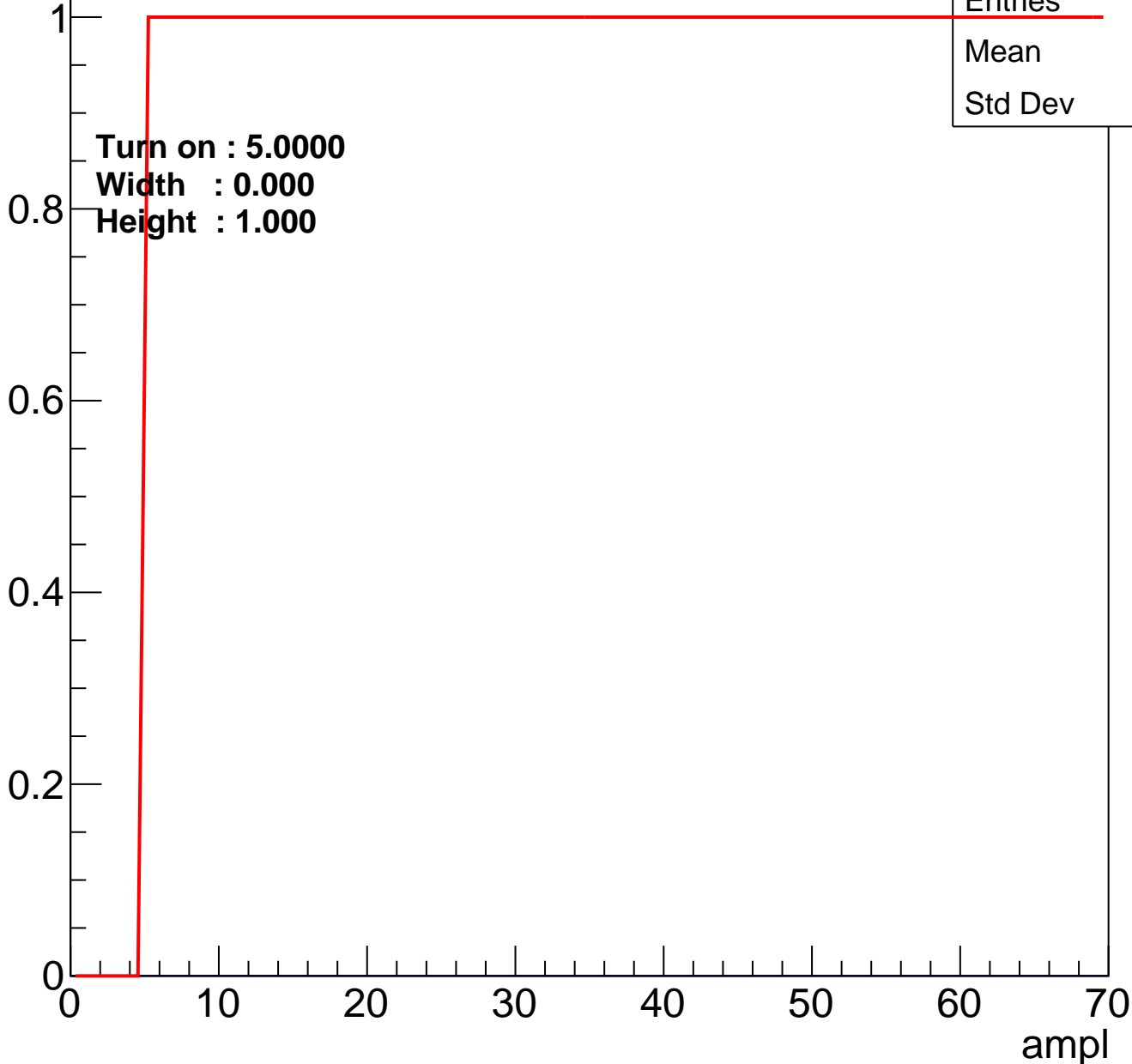
Entry



# B0L100S, U18-ch4

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U18-ch5

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U18-ch6

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



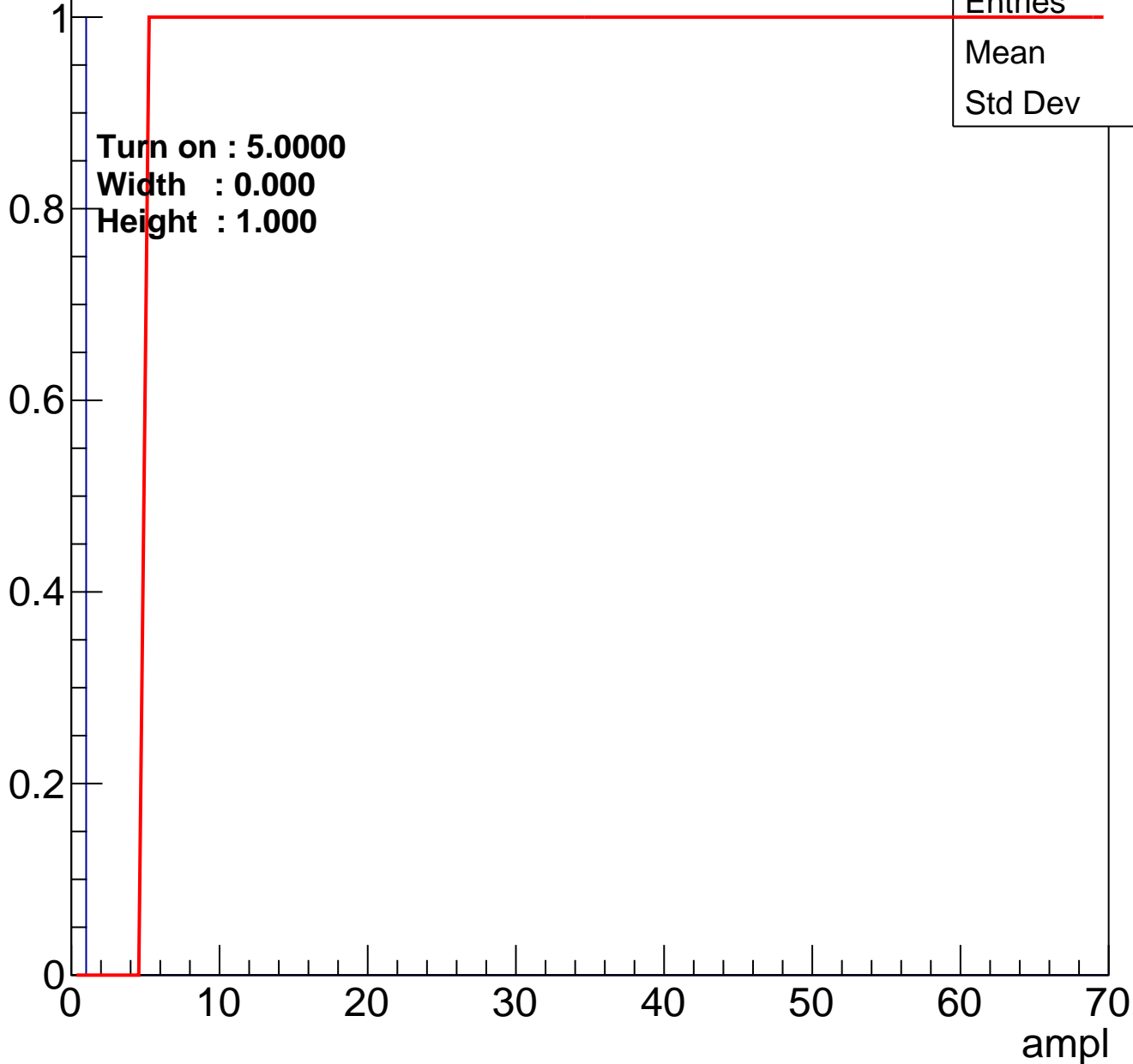
Entries	0
Mean	0
Std Dev	0



# B0L100S, U18-ch7

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



# B0L100S, U18-ch8

calib\_packv5\_042523\_0143.root, FC#6, port A1

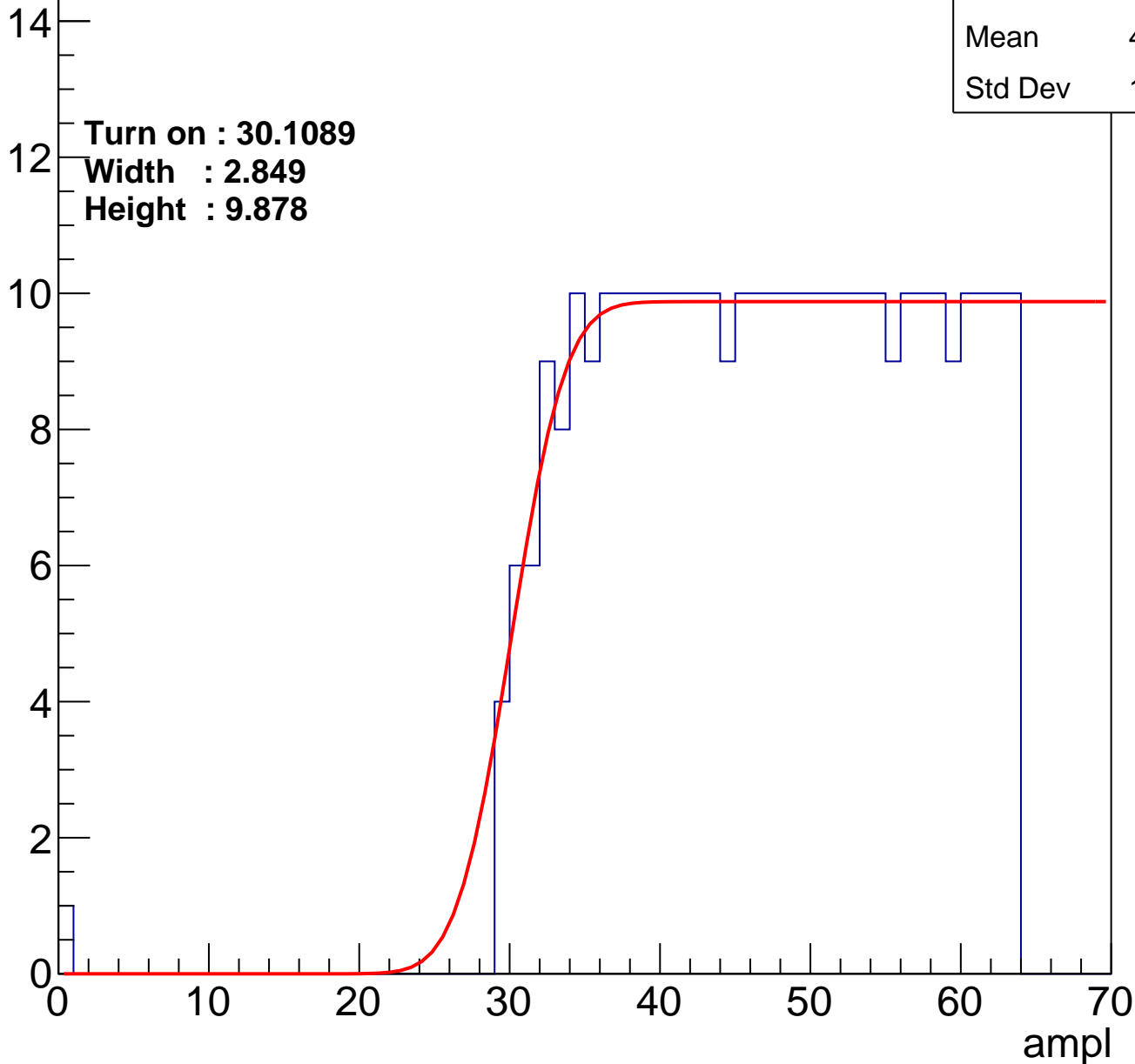
Entry

Entries	330
Mean	46.64
Std Dev	10.02

Turn on : 30.1089

Width : 2.849

Height : 9.878



# B0L100S, U18-ch9

calib\_packv5\_042523\_0143.root, FC#6, port A1

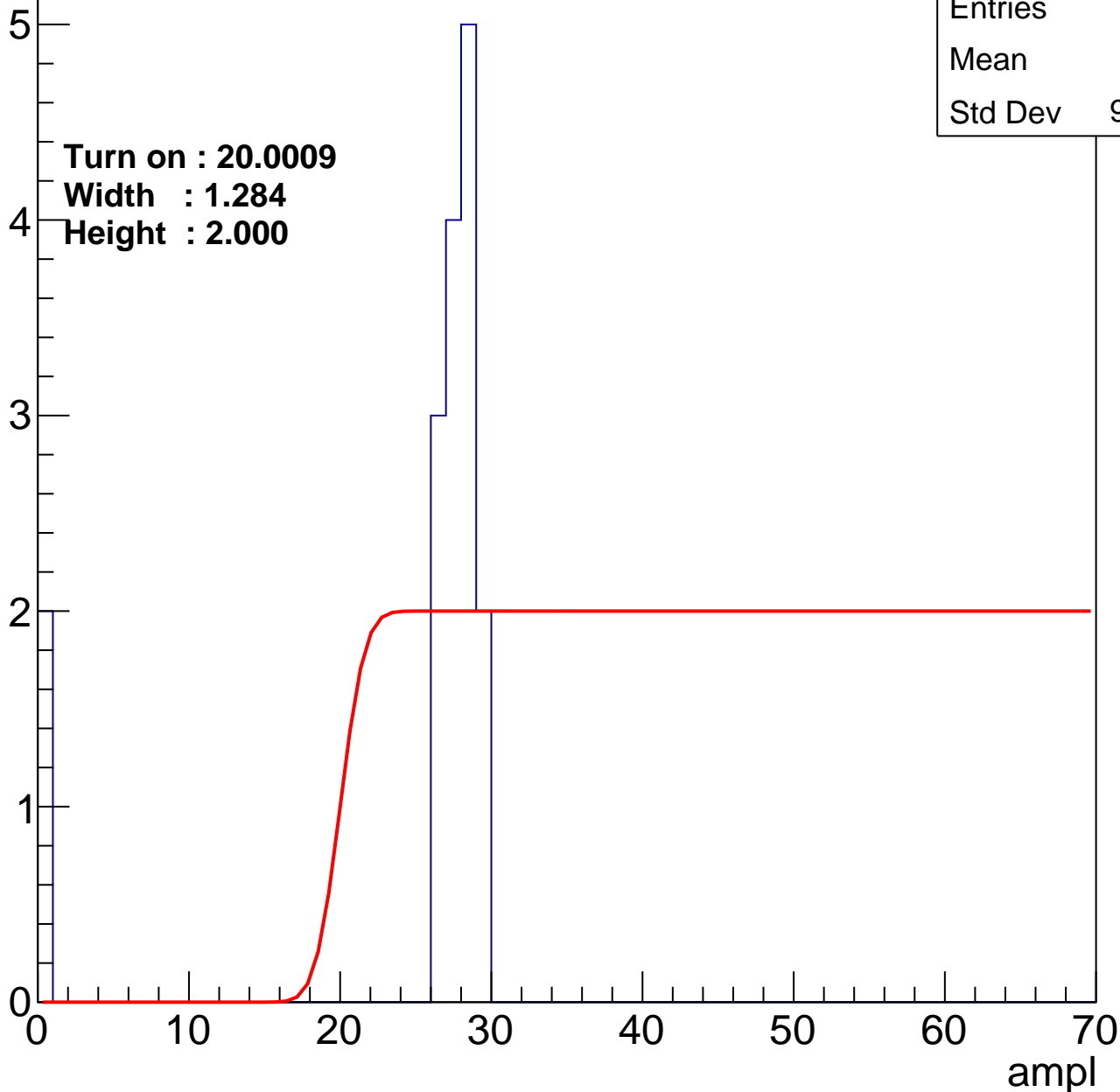
Entry

Entries	16
Mean	24
Std Dev	9.117

Turn on : 20.0009

Width : 1.284

Height : 2.000



# B0L100S, U18-ch10

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry

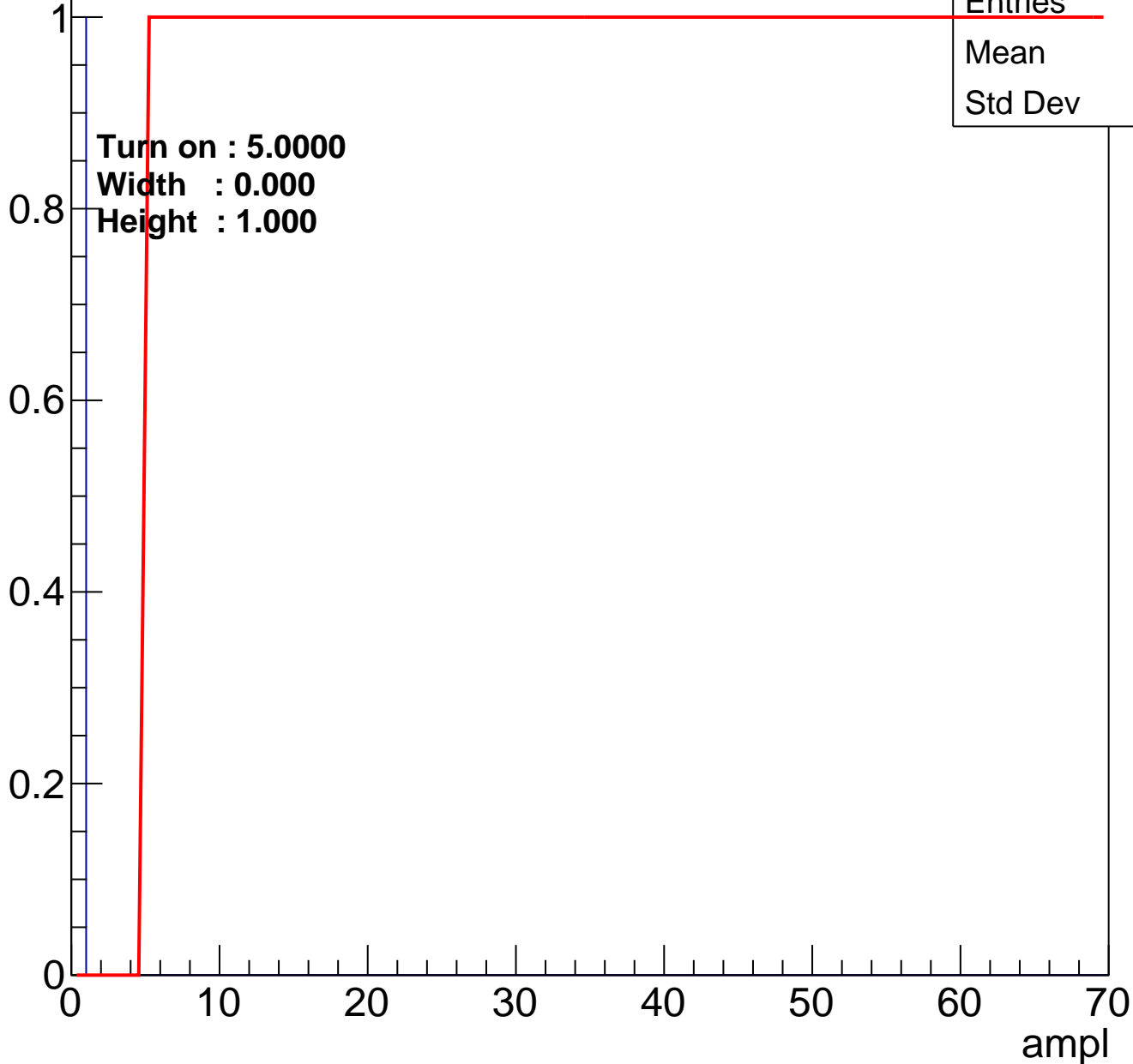


Entries	0
Mean	0
Std Dev	0

# B0L100S, U18-ch11

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



# B0L100S, U18-ch12

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U18-ch13

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry

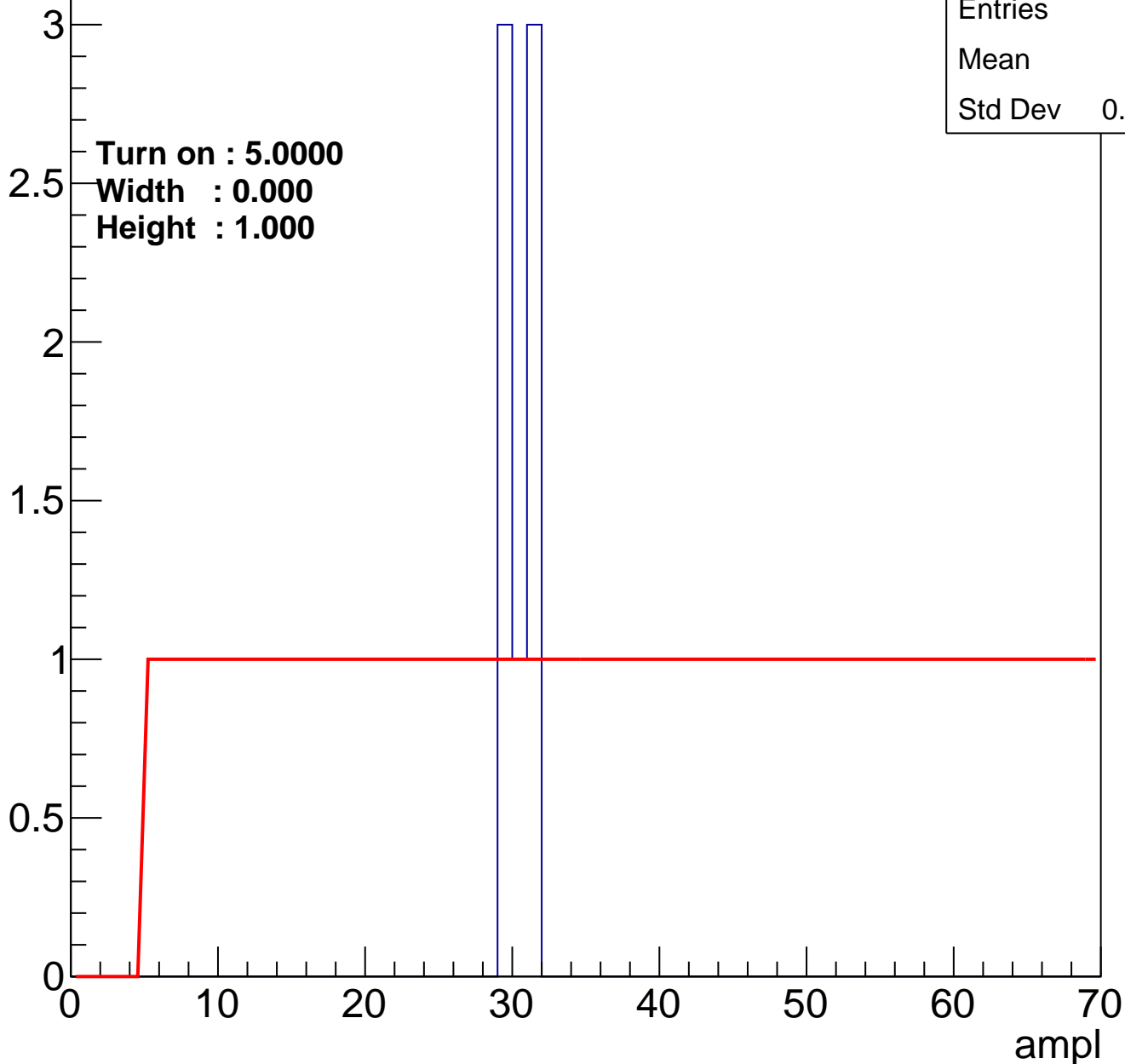


Entries	0
Mean	0
Std Dev	0

# B0L100S, U18-ch14

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry





# B0L100S, U18-ch15

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U18-ch16

calib\_packv5\_042523\_0143.root, FC#6, port A1

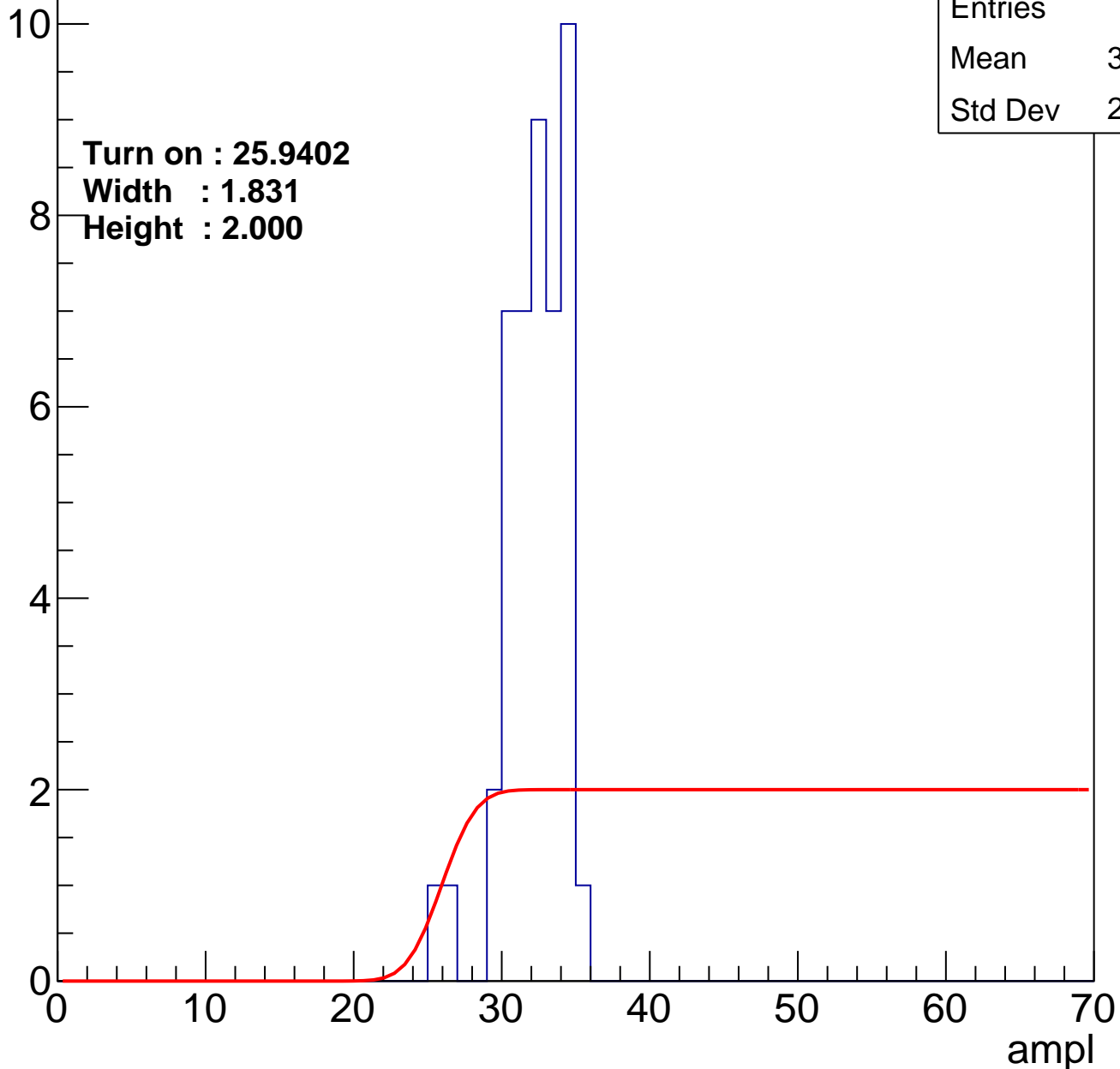
Entries	45
Mean	31.78
Std Dev	2.064

Turn on : 25.9402

Width : 1.831

Height : 2.000

Entry



# B0L100S, U18-ch17

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry

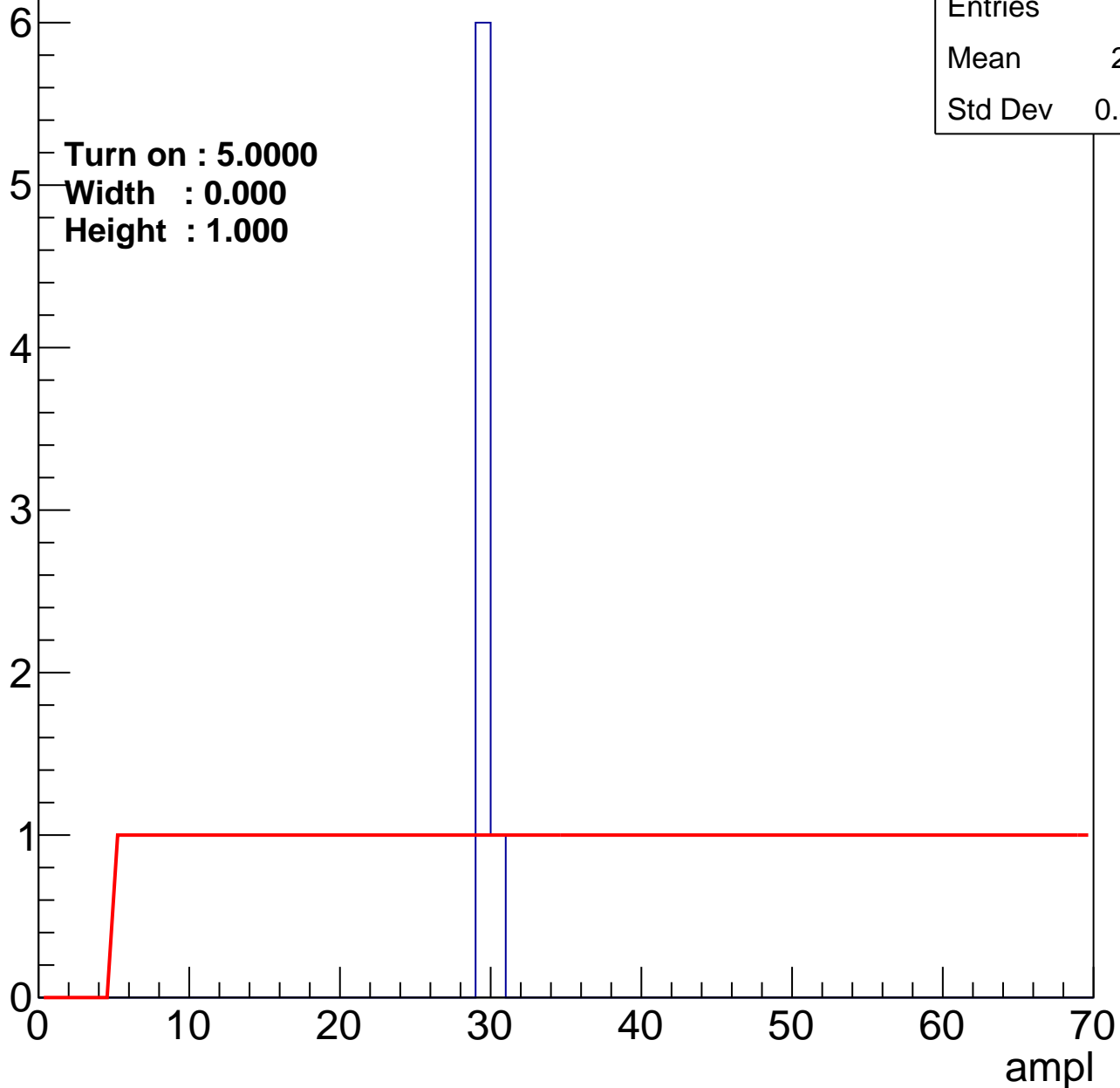


Entries	0
Mean	0
Std Dev	0

# B0L100S, U18-ch18

calib\_packv5\_042523\_0143.root, FC#6, port A1

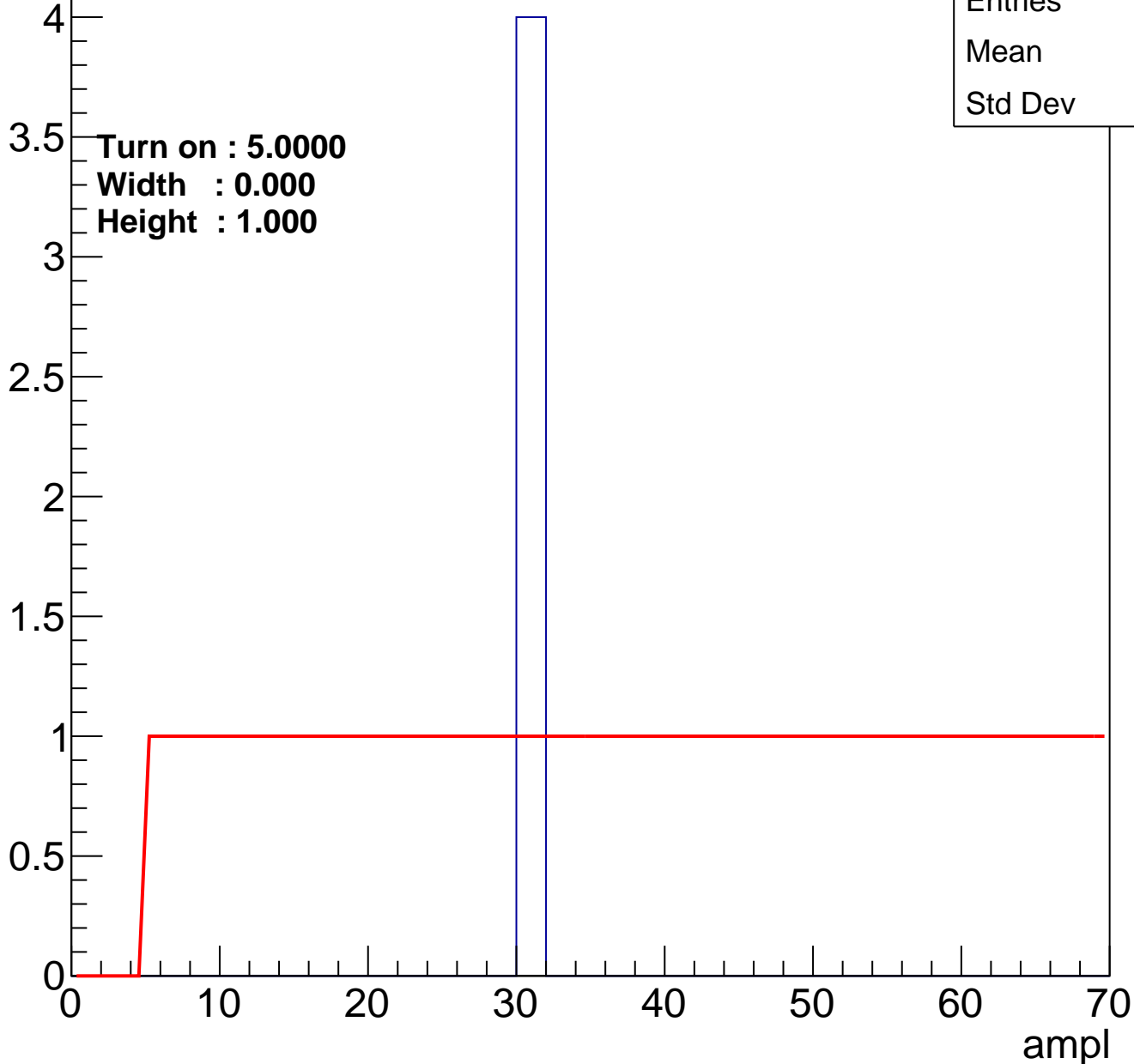
Entry



# B0L100S, U18-ch19

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



# B0L100S, U18-ch20

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U18-ch21

calib\_packv5\_042523\_0143.root, FC#6, port A1

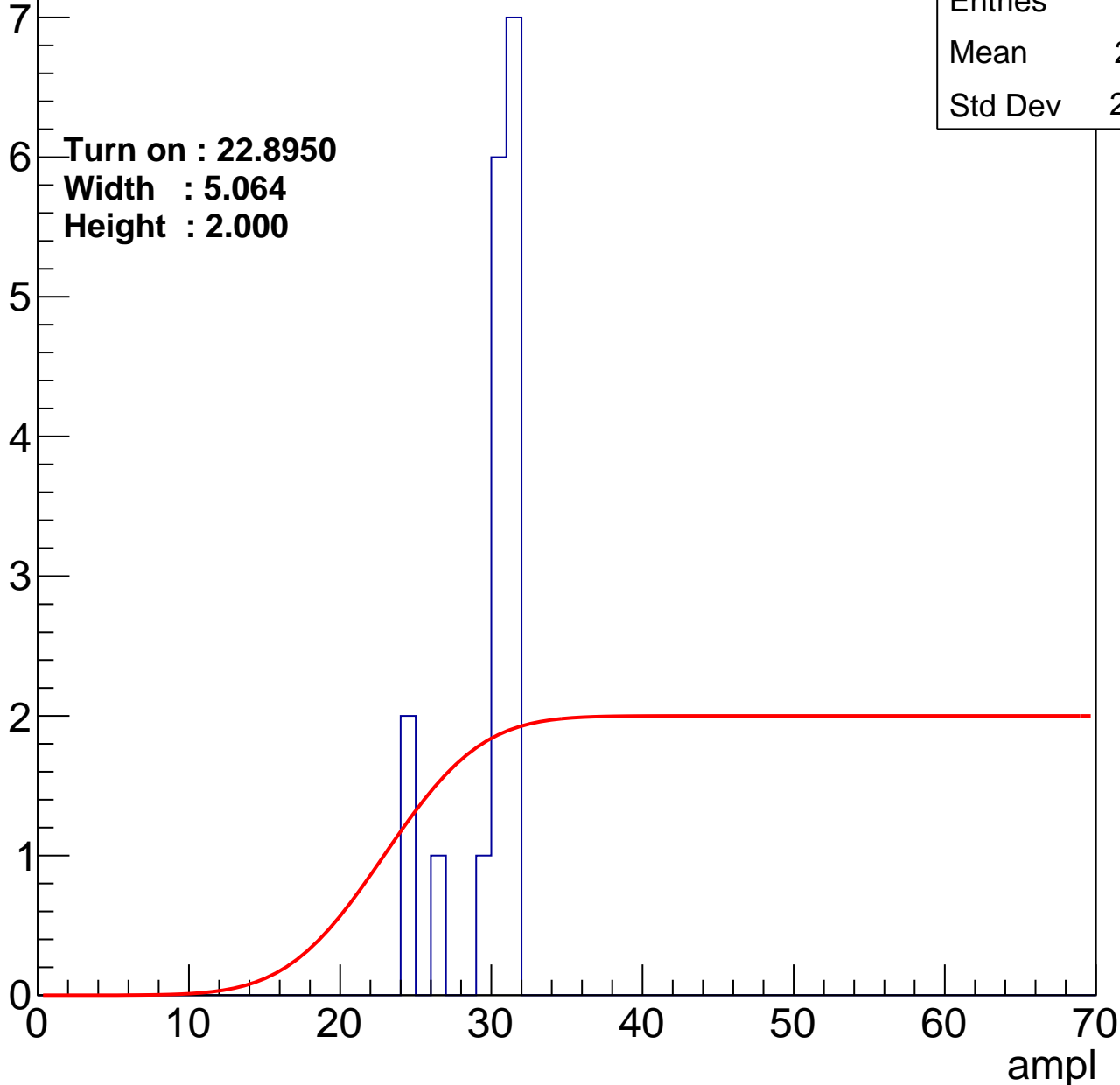
Entry

Entries	17
Mean	29.41
Std Dev	2.302

Turn on : 22.8950

Width : 5.064

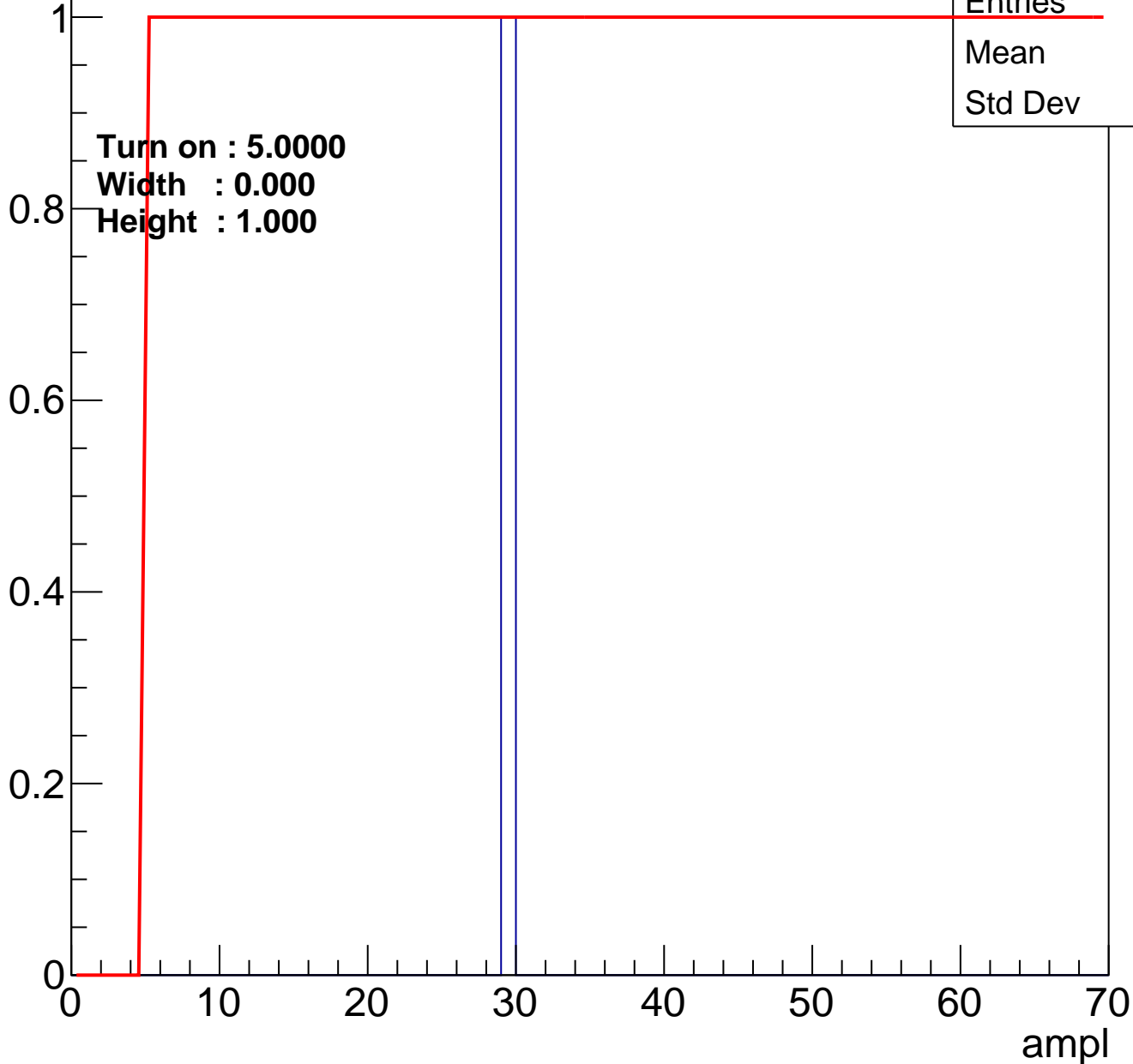
Height : 2.000



# B0L100S, U18-ch22

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry





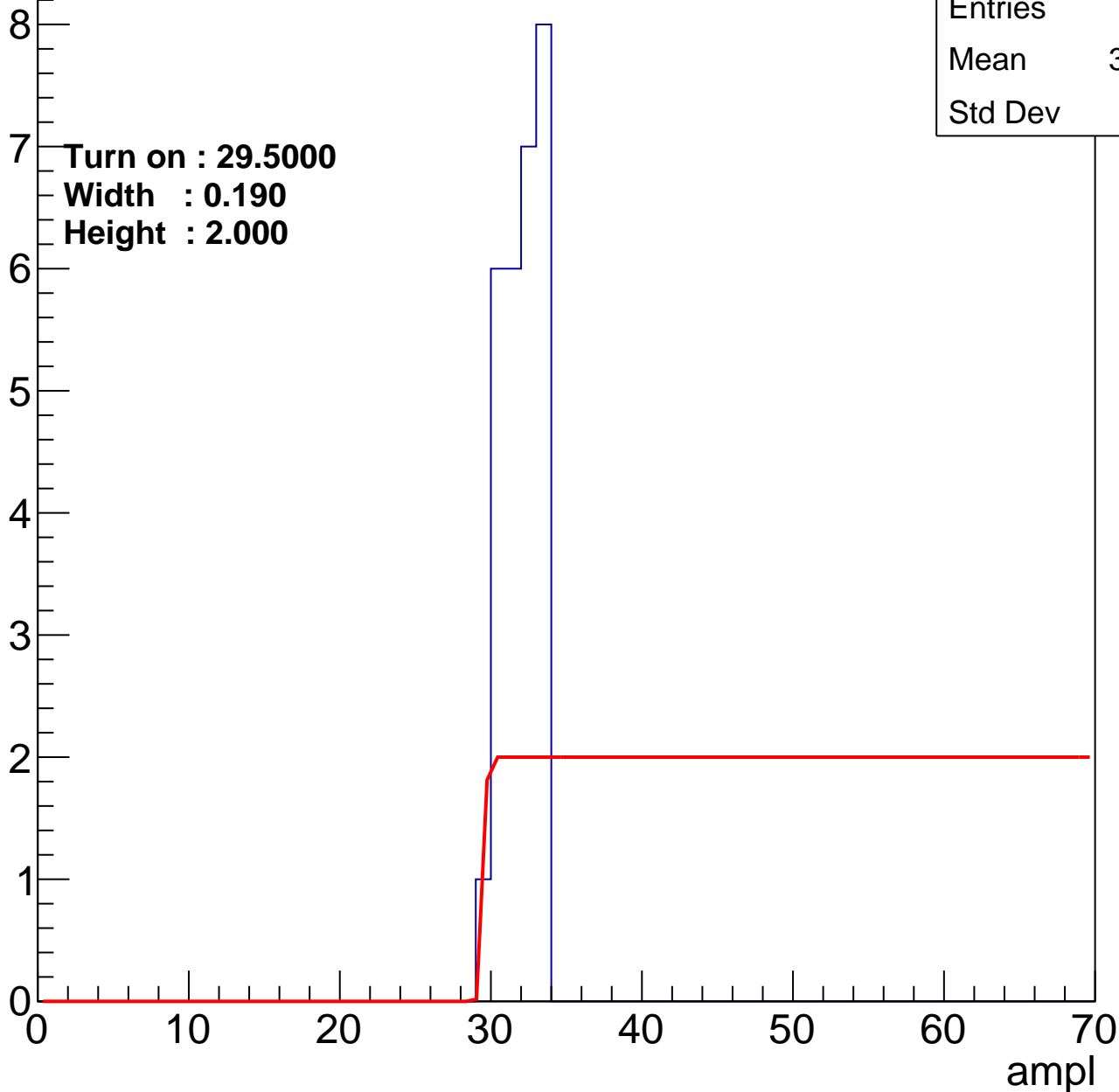
# B0L100S, U18-ch23

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry

Entries	28
Mean	31.54
Std Dev	1.21

Turn on : 29.5000  
Width : 0.190  
Height : 2.000



# B0L100S, U18-ch24

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U18-ch25

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U18-ch26

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U18-ch27

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

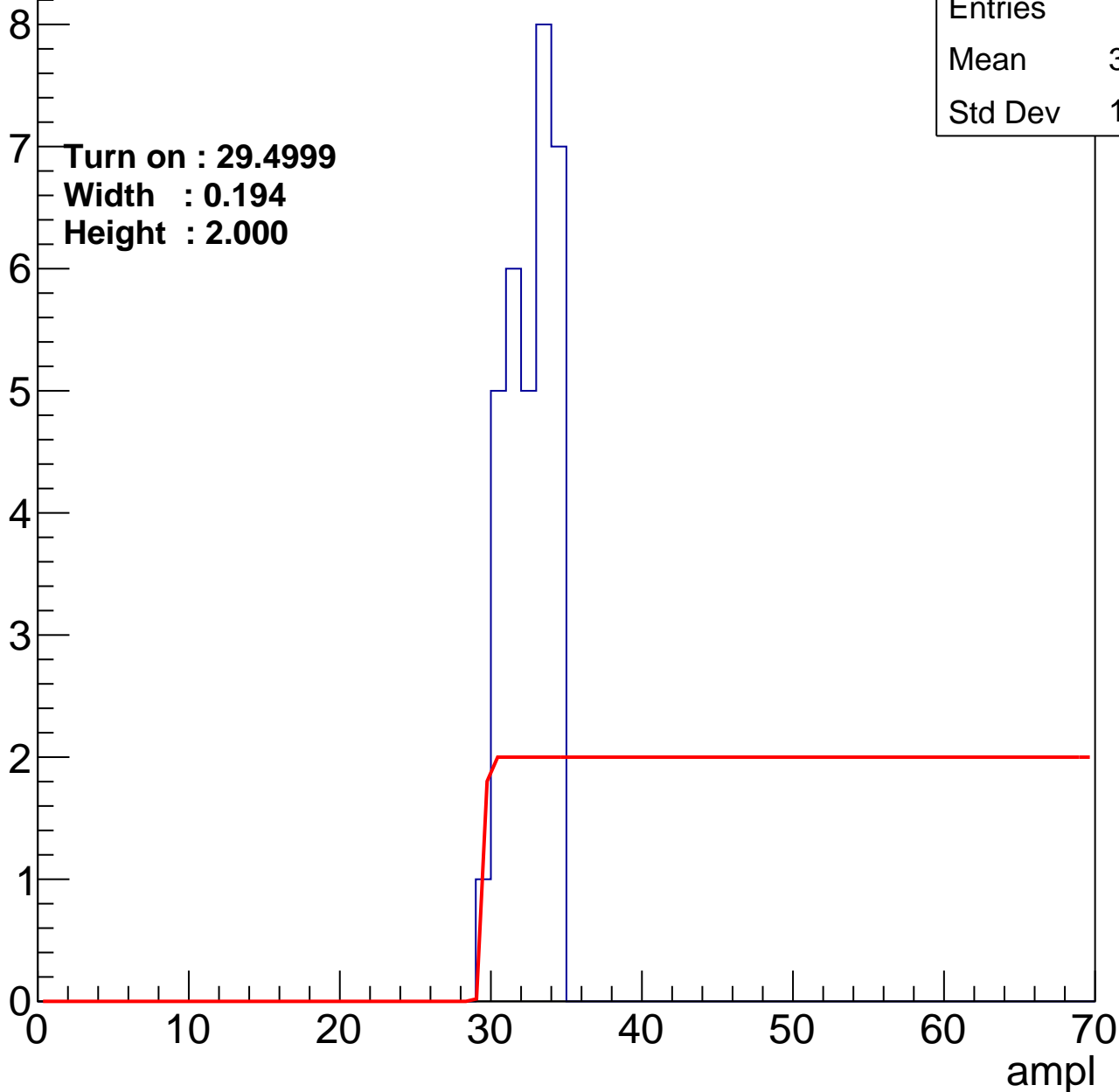
# B0L100S, U18-ch28

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry

Entries	32
Mean	32.09
Std Dev	1.487

Turn on : 29.4999  
Width : 0.194  
Height : 2.000



# B0L100S, U18-ch29

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U18-ch30

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L100S, U18-ch31

calib\_packv5\_042523\_0143.root, FC#6, port A1

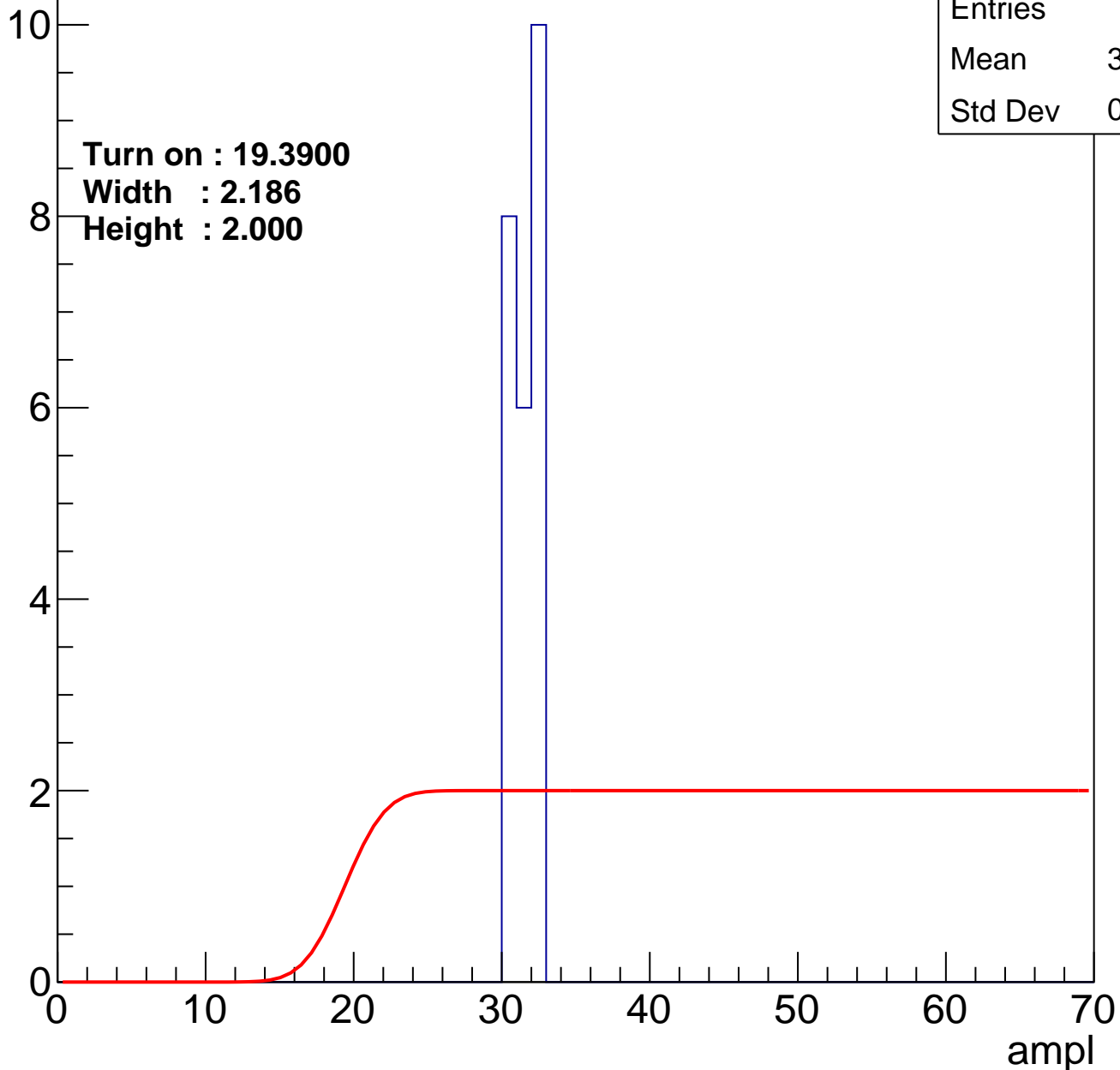
Entries	24
Mean	31.08
Std Dev	0.862

**Turn on : 19.3900**

**Width : 2.186**

**Height : 2.000**

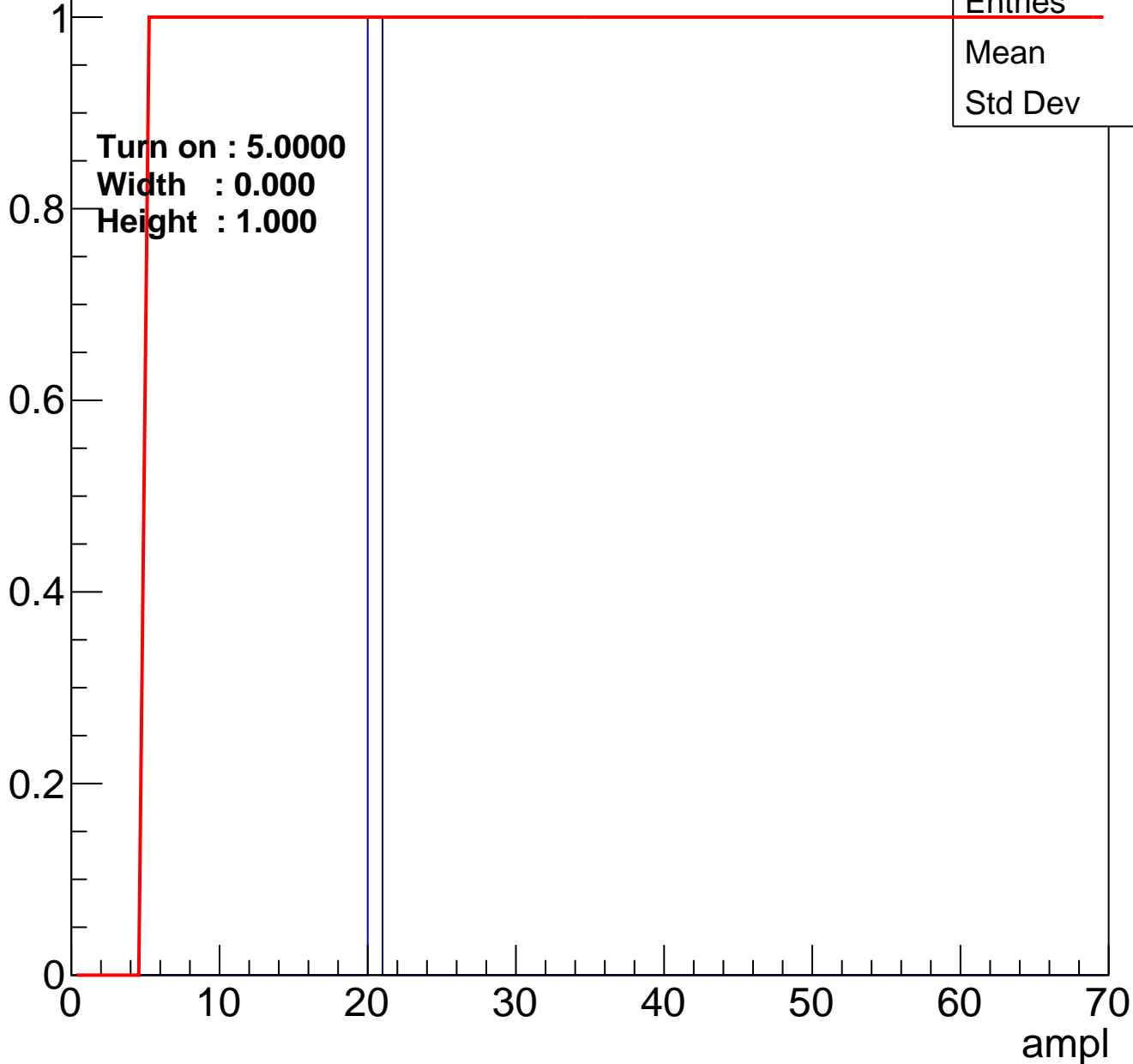
Entry



# B0L100S, U18-ch32

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	1
Mean	20
Std Dev	0

# B0L100S, U18-ch33

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U18-ch34

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U18-ch35

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L100S, U18-ch36

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U18-ch37

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

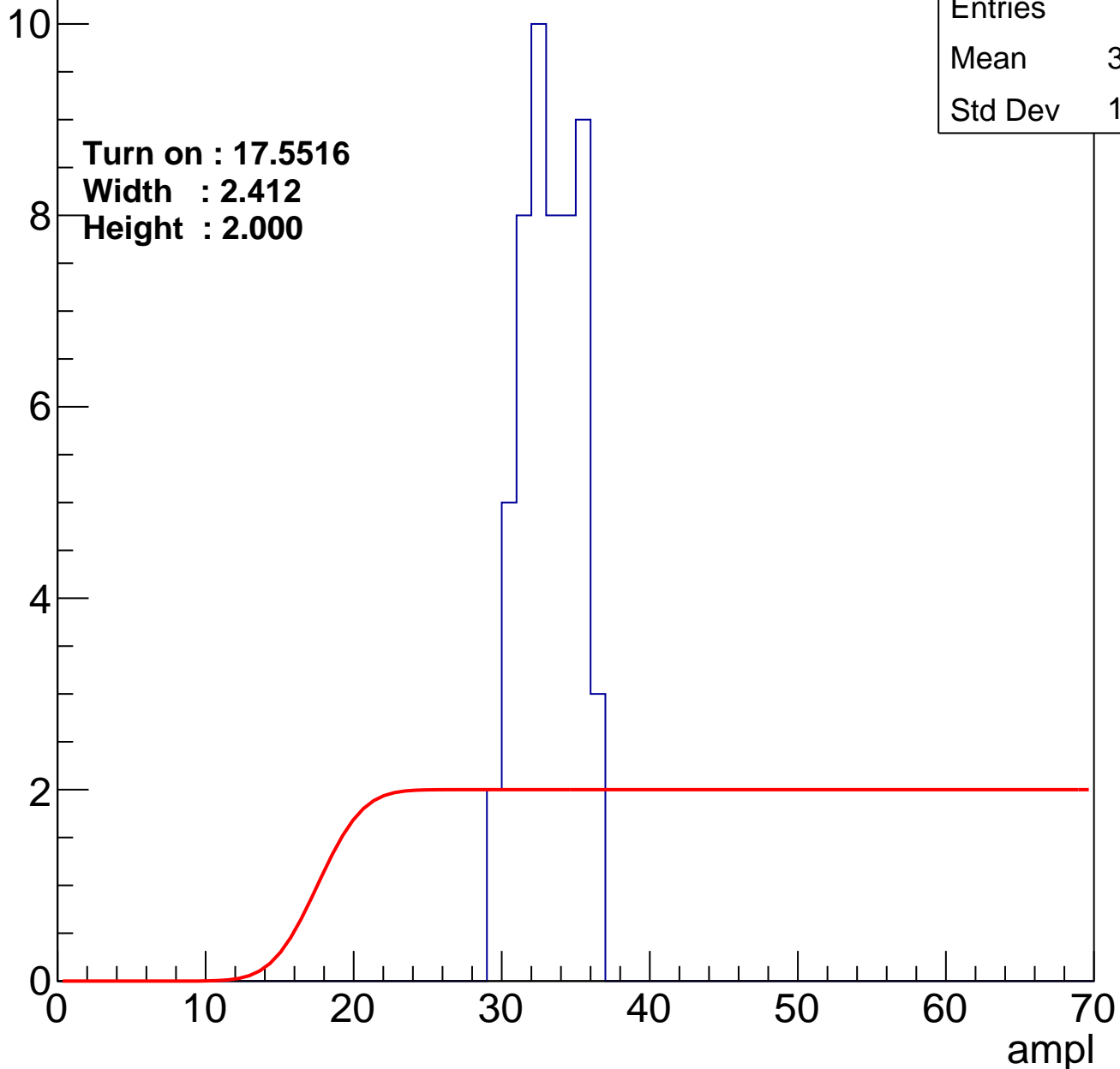
# B0L100S, U18-ch38

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entries	53
Mean	32.74
Std Dev	1.875

Turn on : 17.5516  
Width : 2.412  
Height : 2.000

Entry





# B0L100S, U18-ch39

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U18-ch40

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L100S, U18-ch41

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L100S, U18-ch42

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U18-ch43

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry

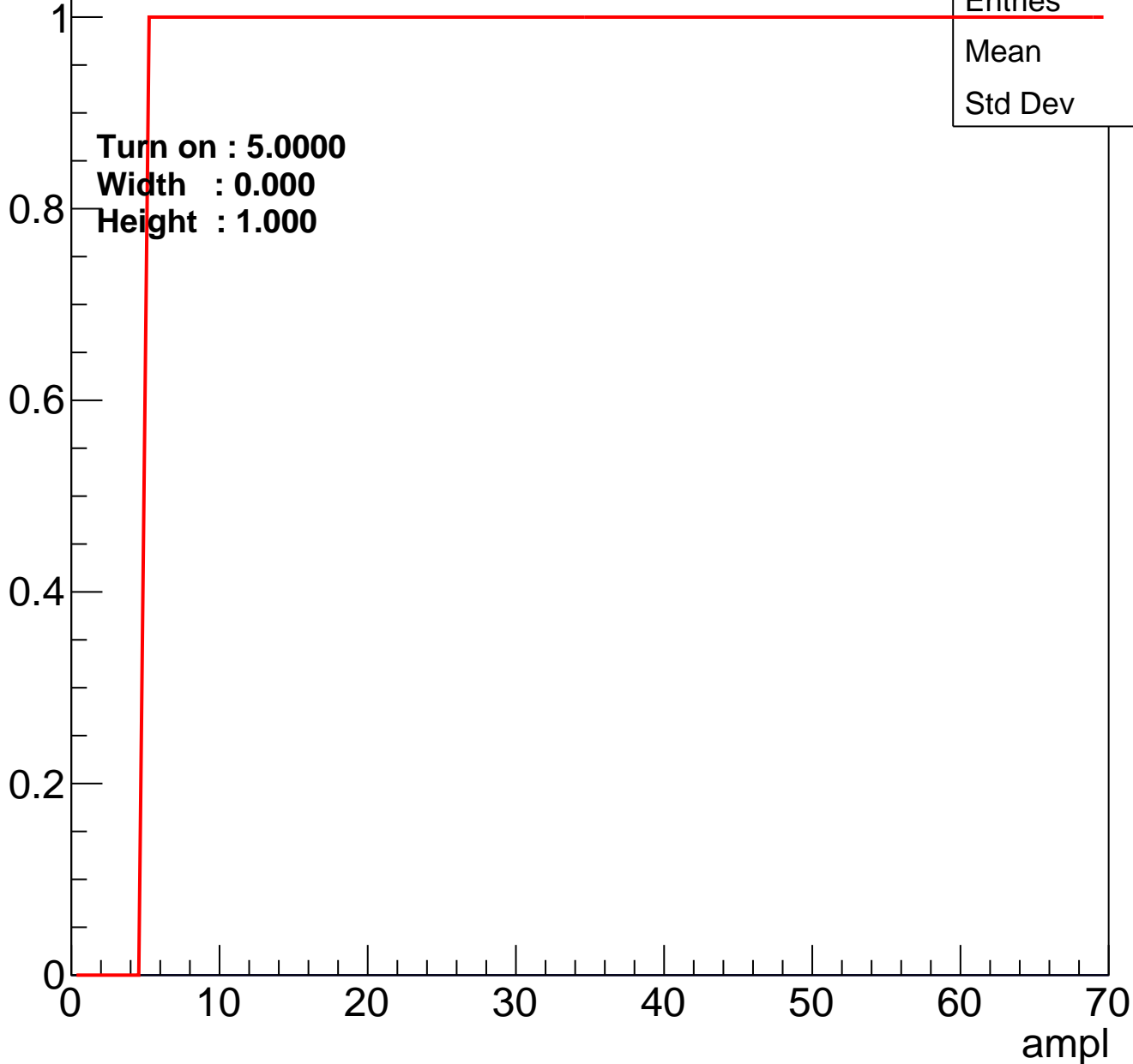


Entries	0
Mean	0
Std Dev	0

# B0L100S, U18-ch44

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry

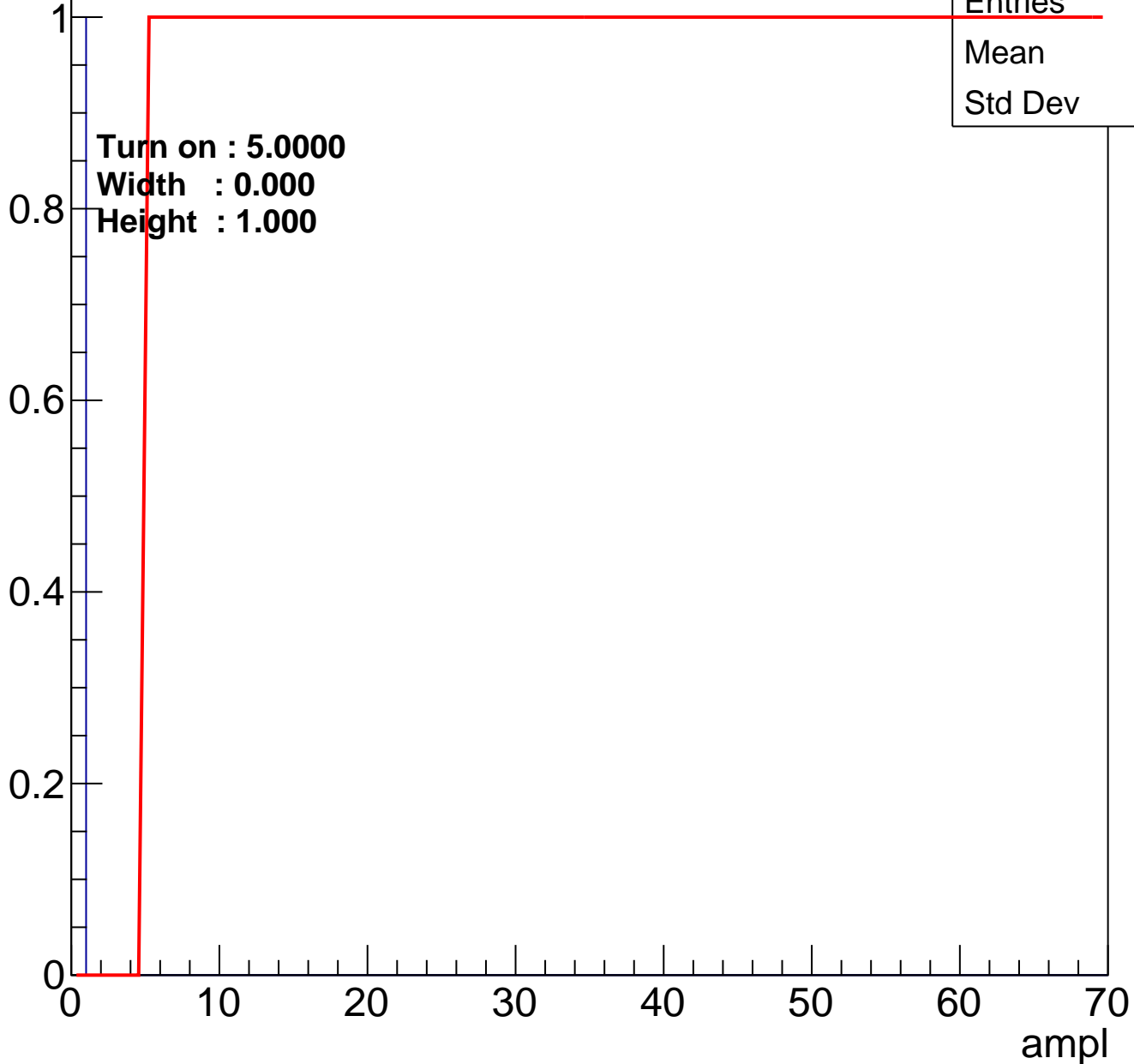


Entries	0
Mean	0
Std Dev	0

# B0L100S, U18-ch45

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	1
Mean	0
Std Dev	0

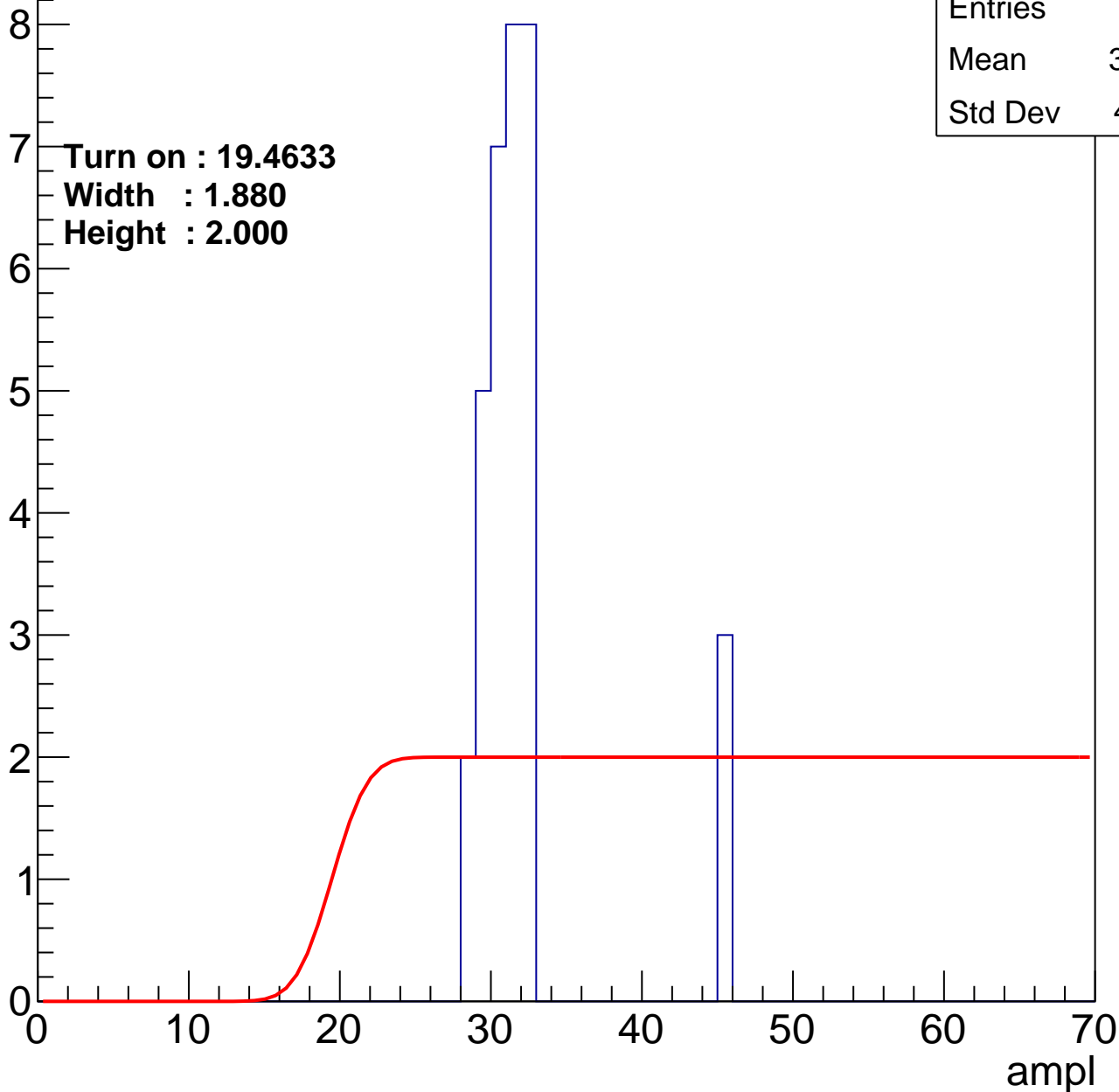
# B0L100S, U18-ch46

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry

Entries	33
Mean	31.82
Std Dev	4.331

Turn on : 19.4633  
Width : 1.880  
Height : 2.000





# B0L100S, U18-ch47

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U18-ch48

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U18-ch49

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U18-ch50

calib\_packv5\_042523\_0143.root, FC#6, port A1

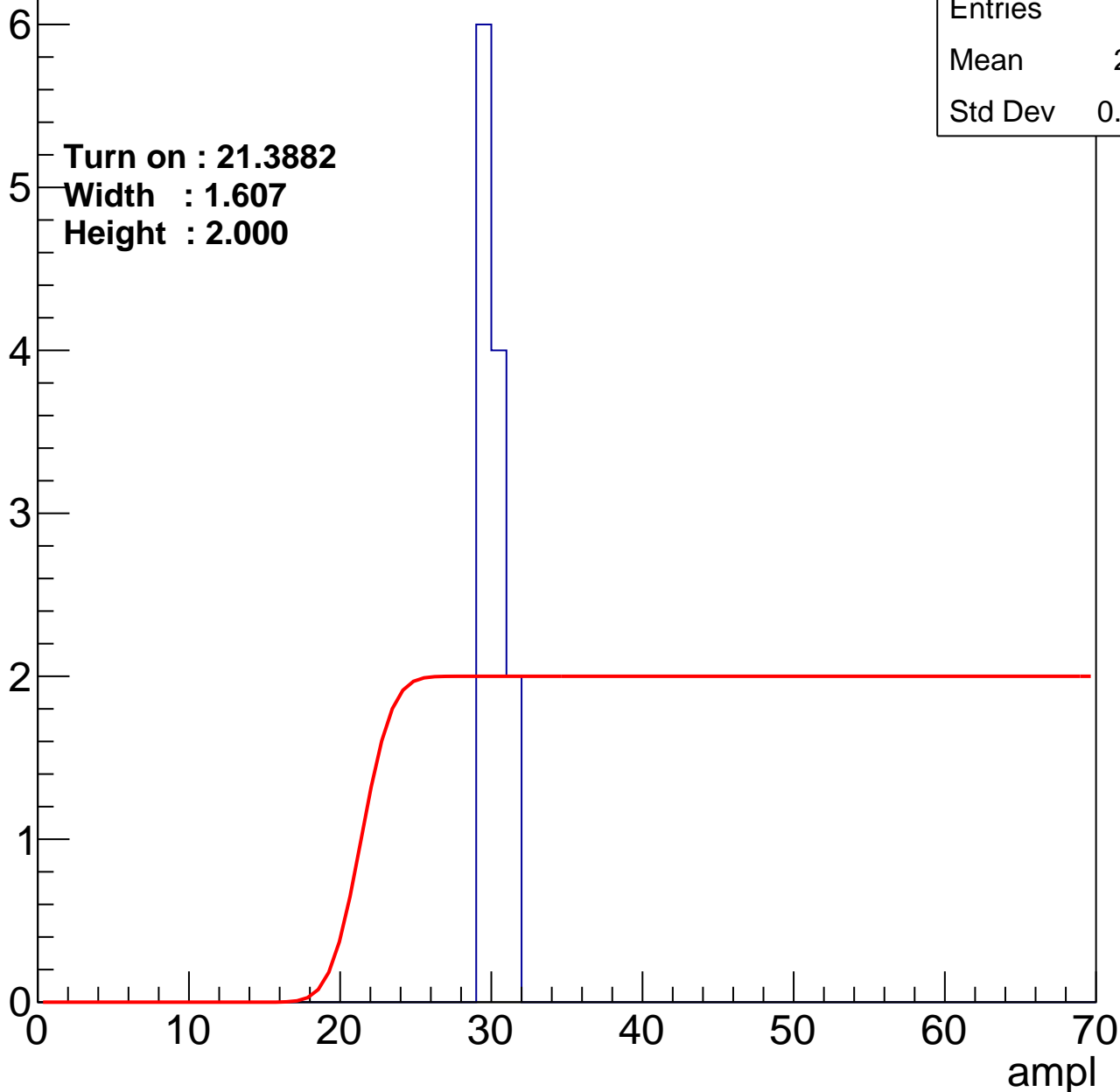
Entry

Entries	12
Mean	29.67
Std Dev	0.7454

Turn on : 21.3882

Width : 1.607

Height : 2.000



# B0L100S, U18-ch51

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U18-ch52

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U18-ch53

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U18-ch54

calib\_packv5\_042523\_0143.root, FC#6, port A1

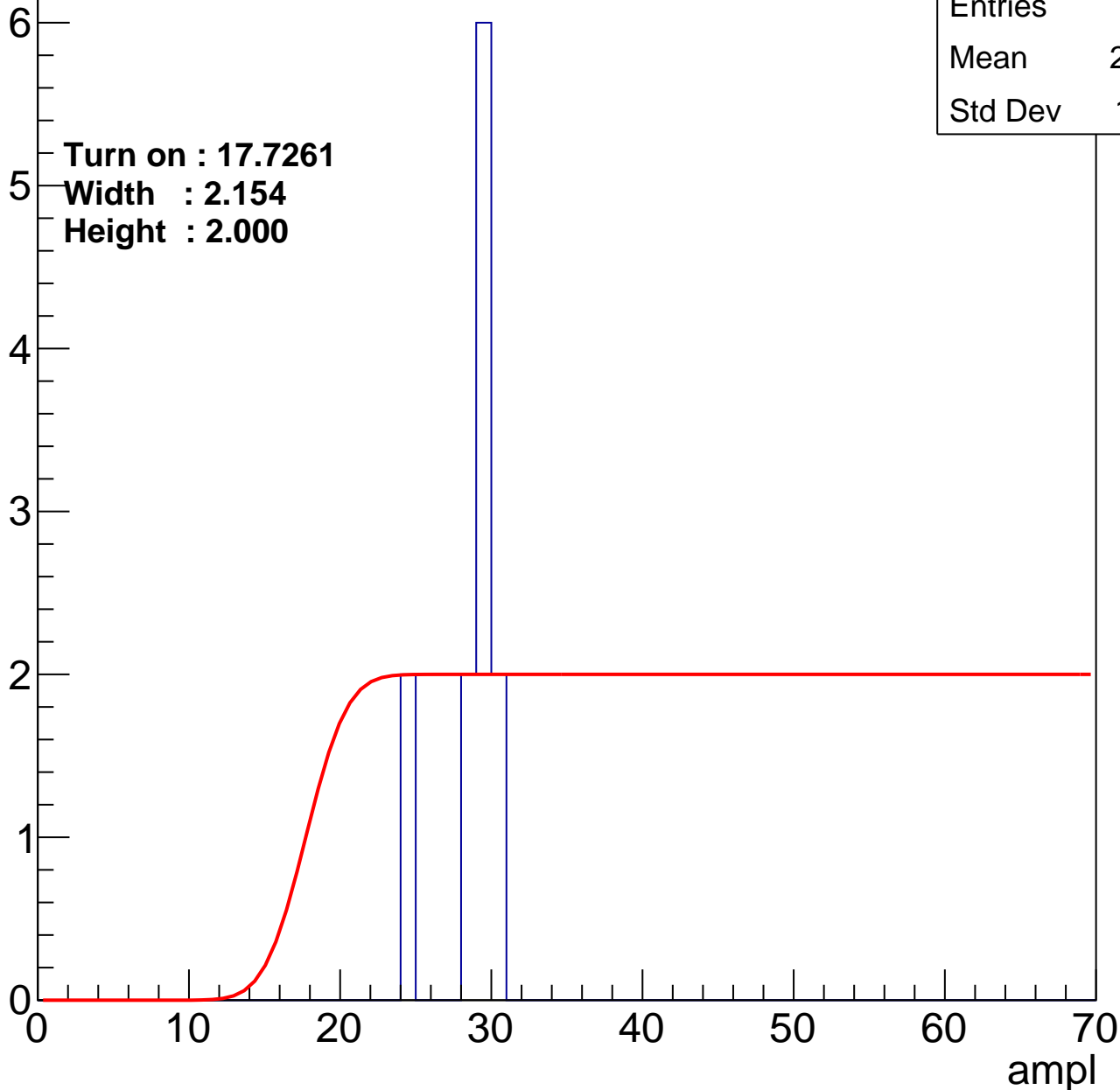
Entry

Entries	12
Mean	28.17
Std Dev	1.951

Turn on : 17.7261

Width : 2.154

Height : 2.000





# B0L100S, U18-ch55

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U18-ch56

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry

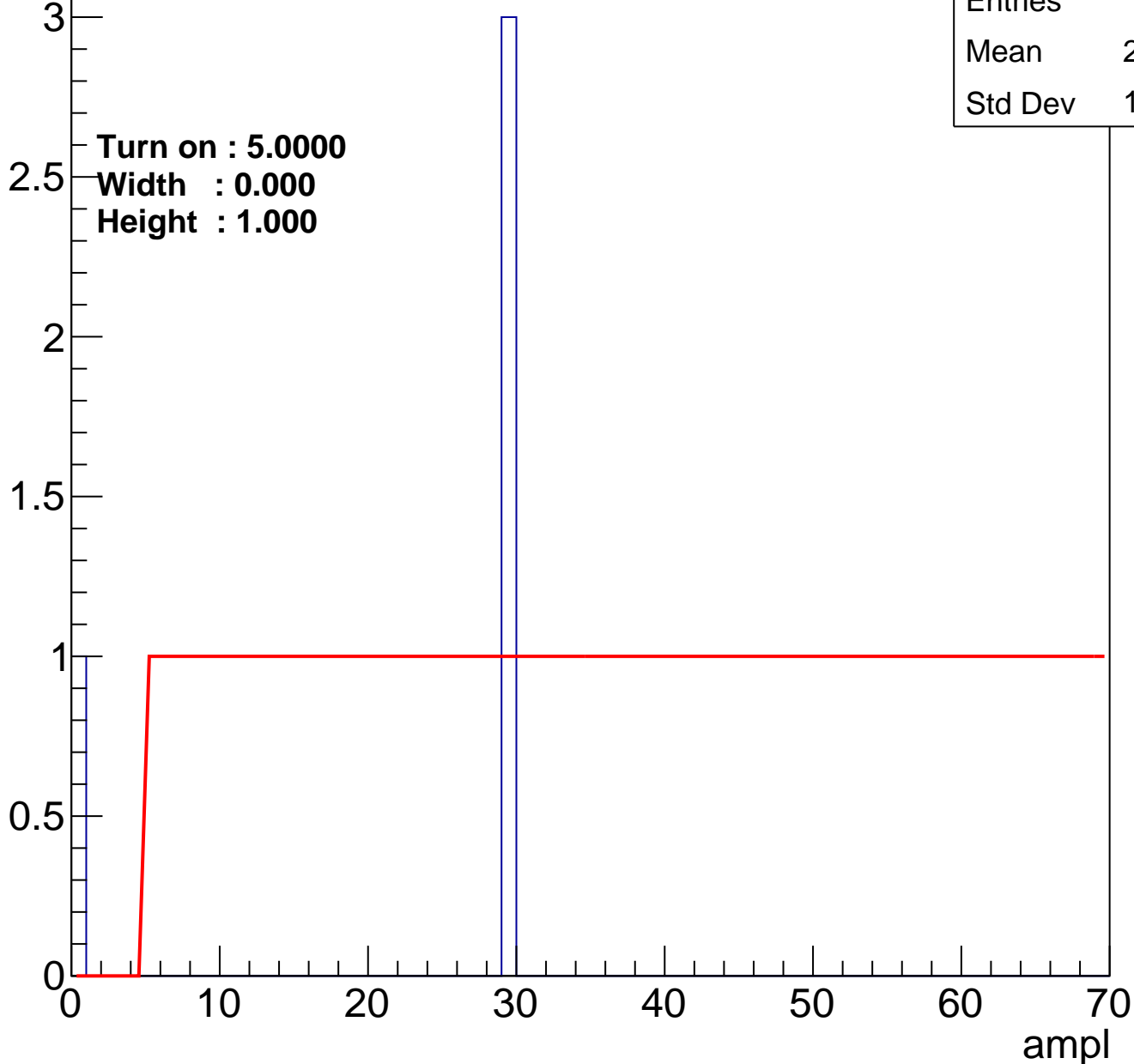


Entries	1
Mean	0
Std Dev	0

# B0L100S, U18-ch57

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



# B0L100S, U18-ch58

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U18-ch59

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U18-ch60

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



# B0L100S, U18-ch61

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry

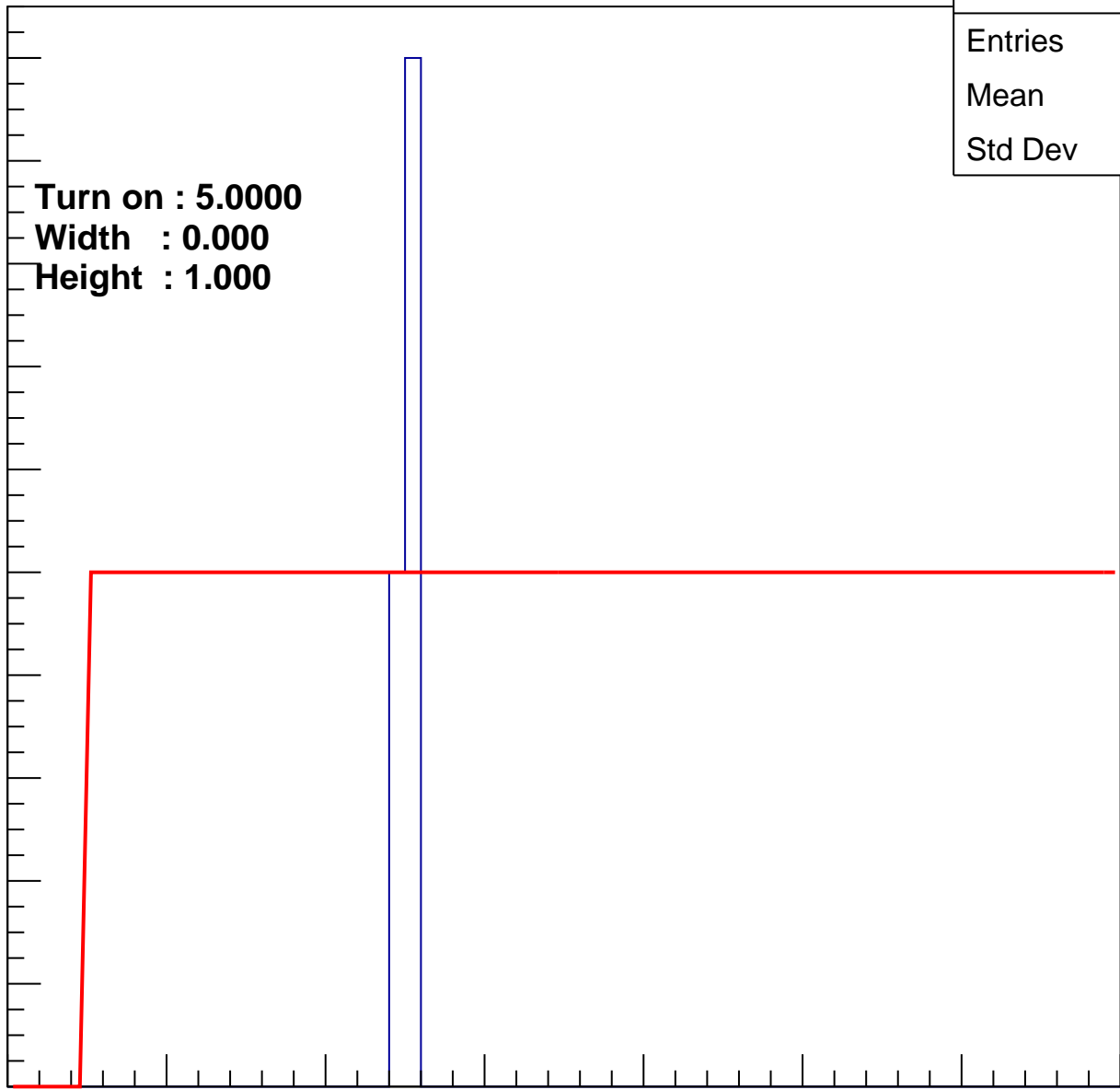
2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Turn on : 5.0000  
Width : 0.000  
Height : 1.000

Entries	3
Mean	24.67
Std Dev	0.4714

0 10 20 30 40 50 60 70

ampl



# B0L100S, U18-ch62

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L100S, U18-ch63

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry

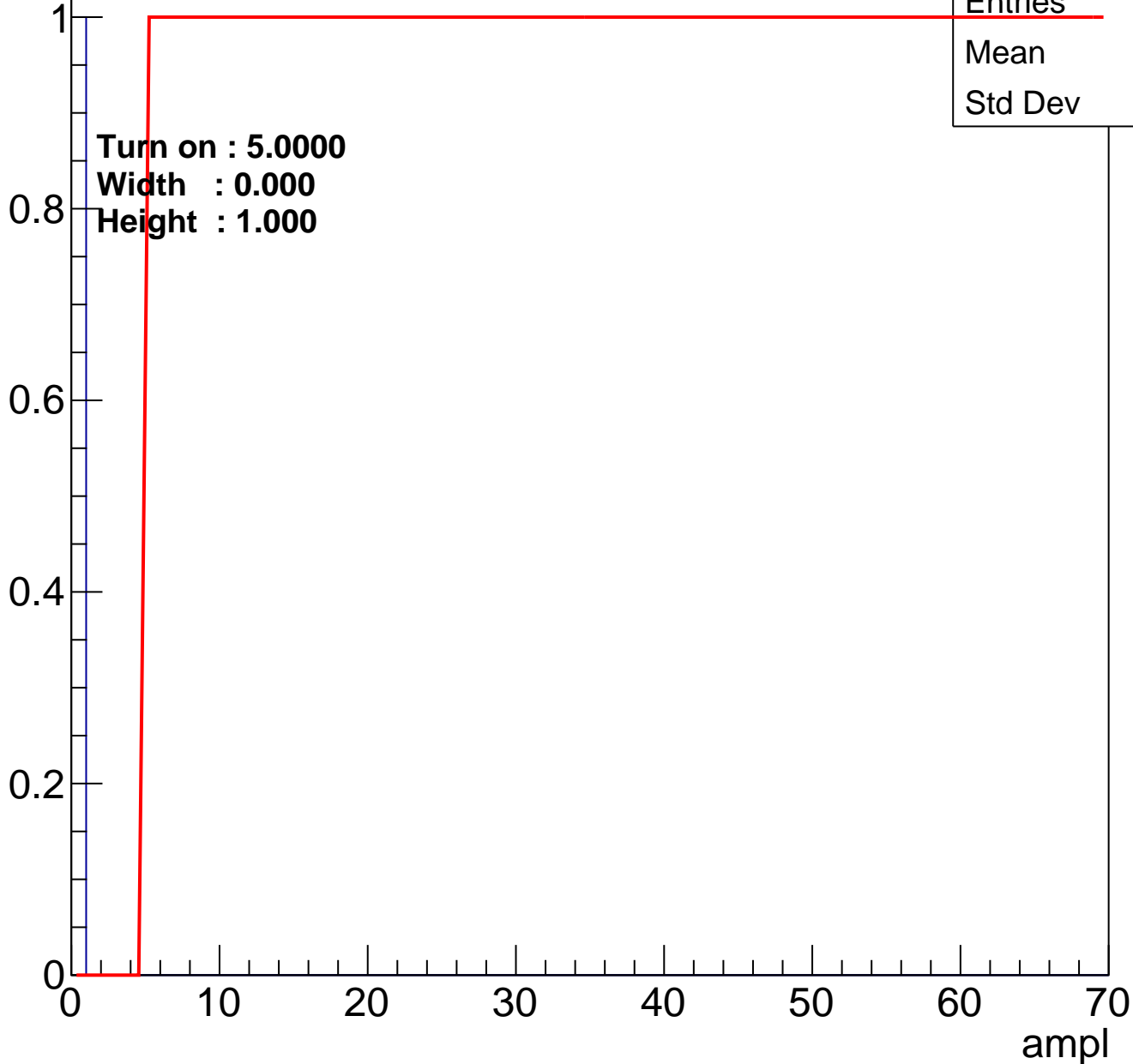


Entries	0
Mean	0
Std Dev	0

# B0L100S, U18-ch64

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



# B0L100S, U18-ch65

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U18-ch66

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U18-ch67

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U18-ch68

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L100S, U18-ch69

calib\_packv5\_042523\_0143.root, FC#6, port A1

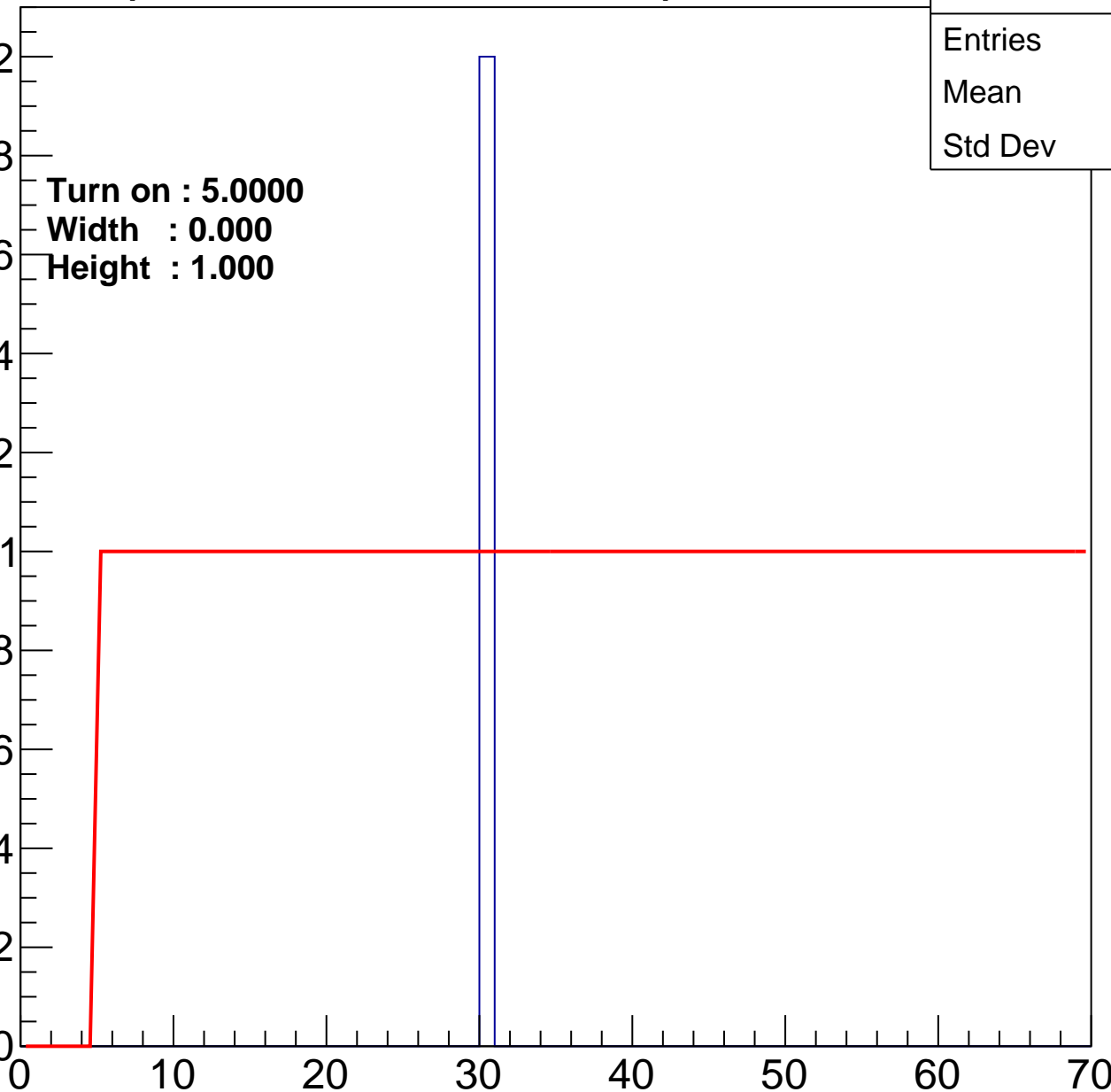
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Turn on : 5.0000  
Width : 0.000  
Height : 1.000

Entries	2
Mean	30
Std Dev	0

ampl



# B0L100S, U18-ch70

calib\_packv5\_042523\_0143.root, FC#6, port A1

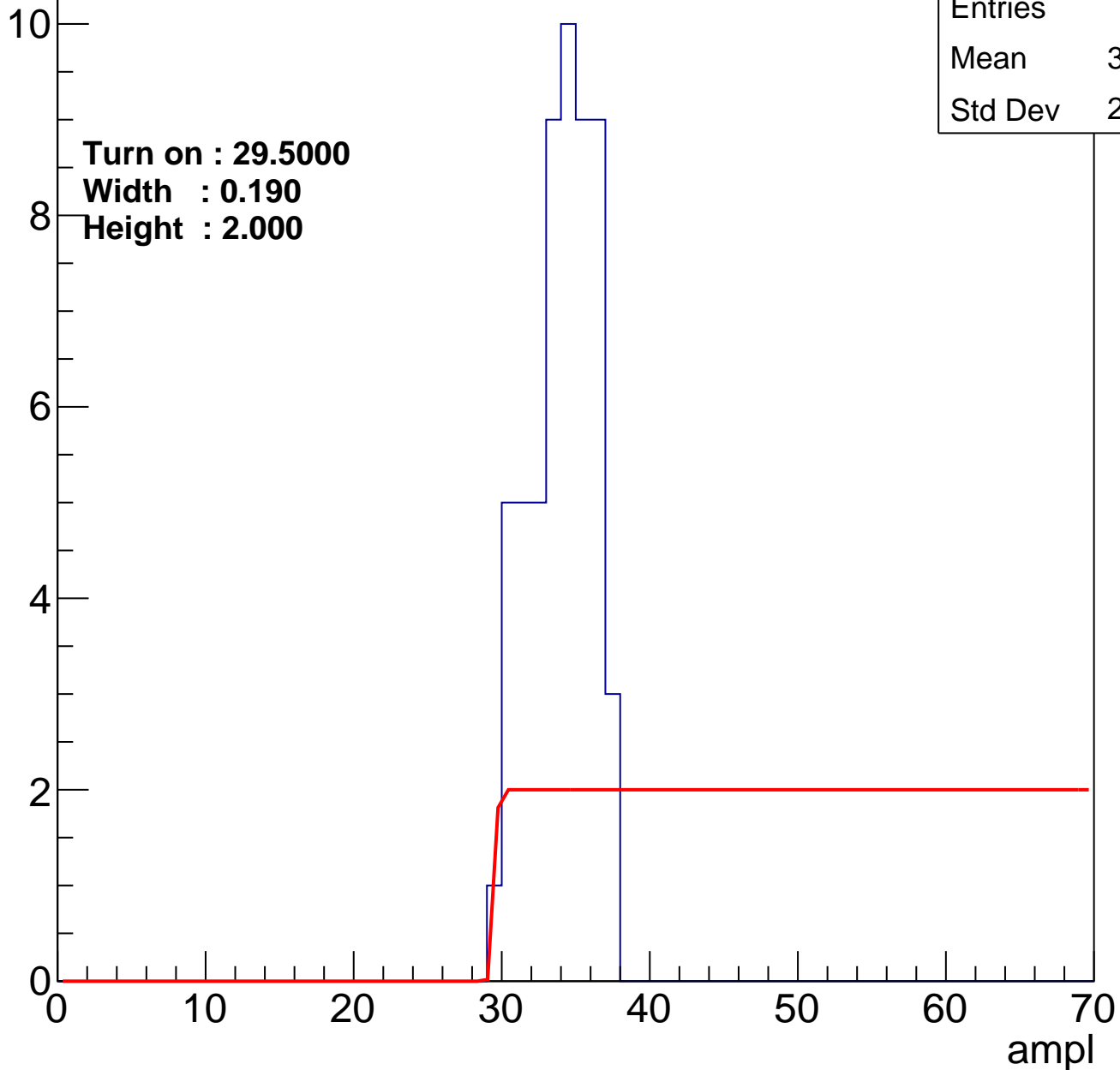
Entries	56
Mean	33.59
Std Dev	2.077

Turn on : 29.5000

Width : 0.190

Height : 2.000

Entry





# B0L100S, U18-ch71

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U18-ch72

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U18-ch73

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry

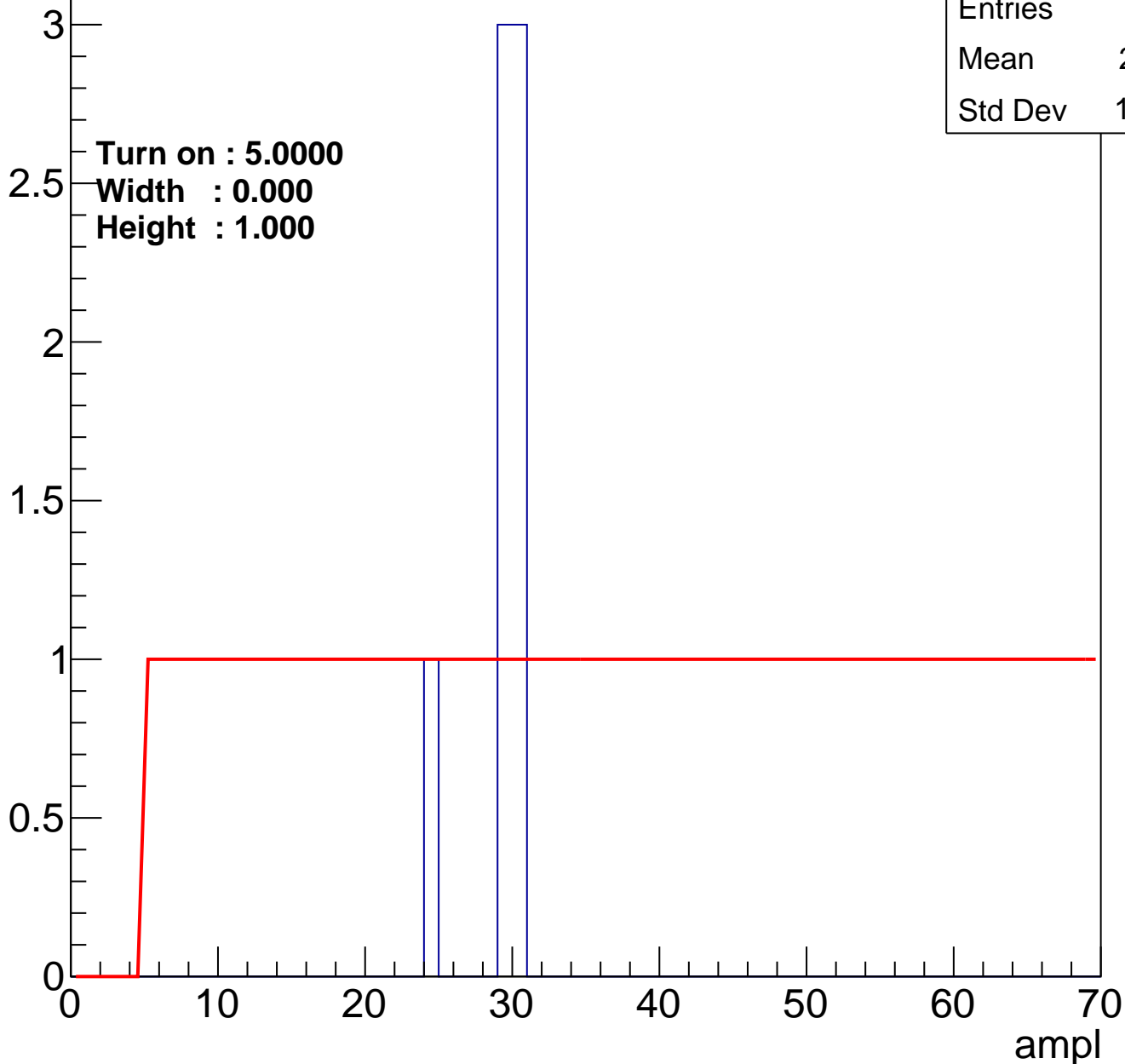


Entries	1
Mean	0
Std Dev	0

# B0L100S, U18-ch74

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



# B0L100S, U18-ch75

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U18-ch76

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U18-ch77

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U18-ch78

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



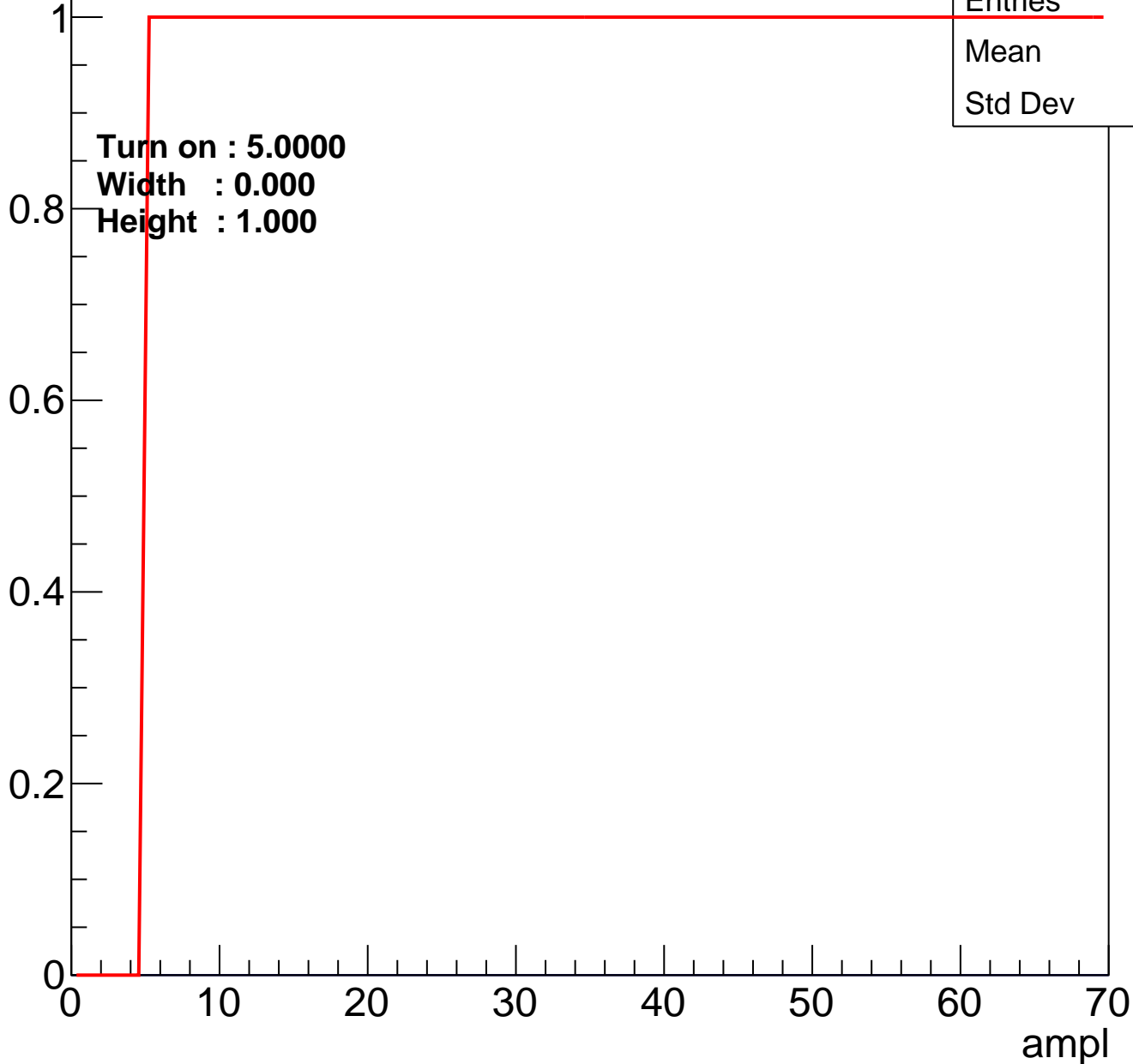
Entries	1
Mean	0
Std Dev	0



# B0L100S, U18-ch79

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U18-ch80

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U18-ch81

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



# B0L100S, U18-ch82

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

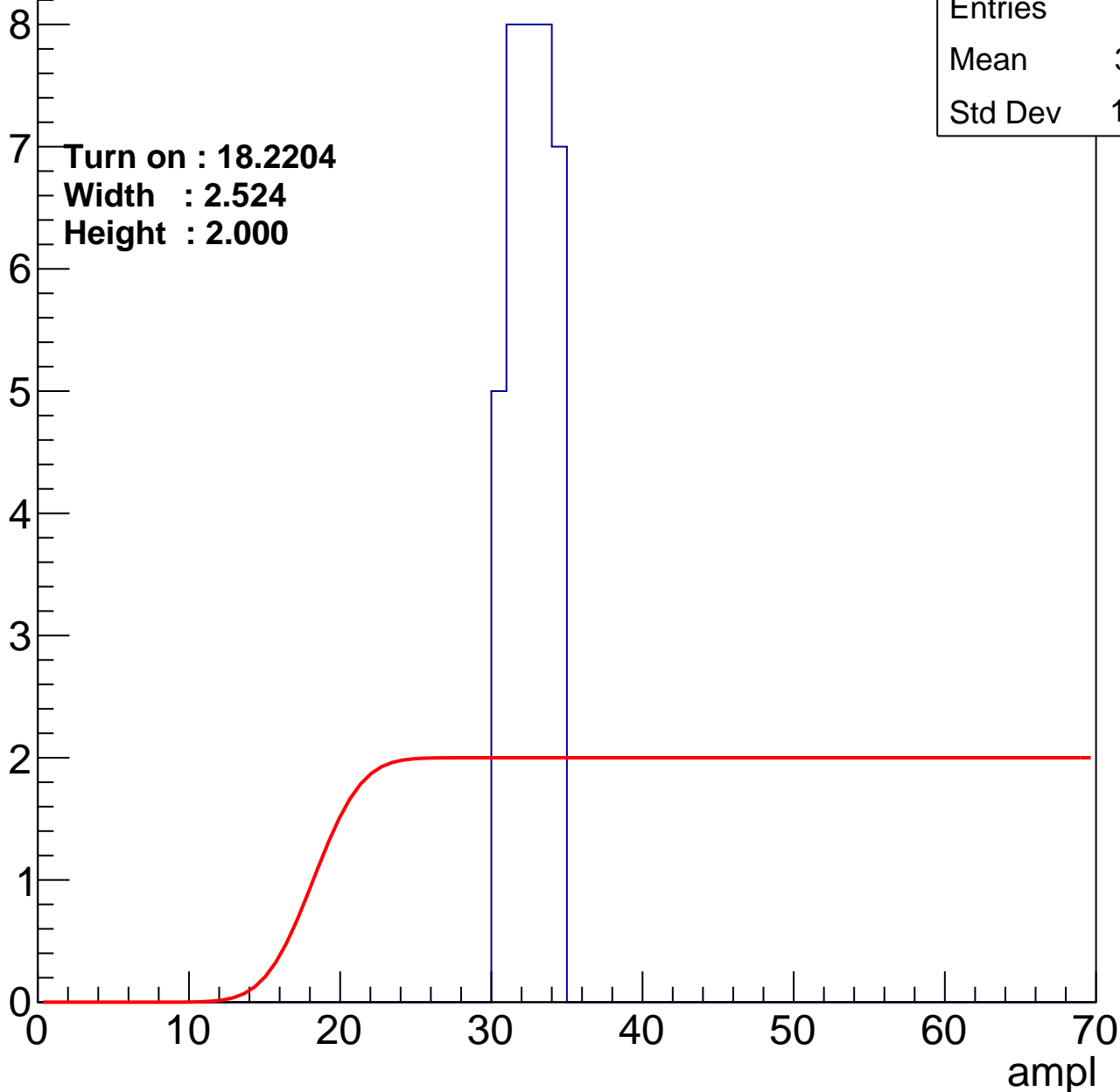
# B0L100S, U18-ch83

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry

Entries	36
Mean	32.11
Std Dev	1.329

Turn on : 18.2204  
Width : 2.524  
Height : 2.000



# B0L100S, U18-ch84

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U18-ch85

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry

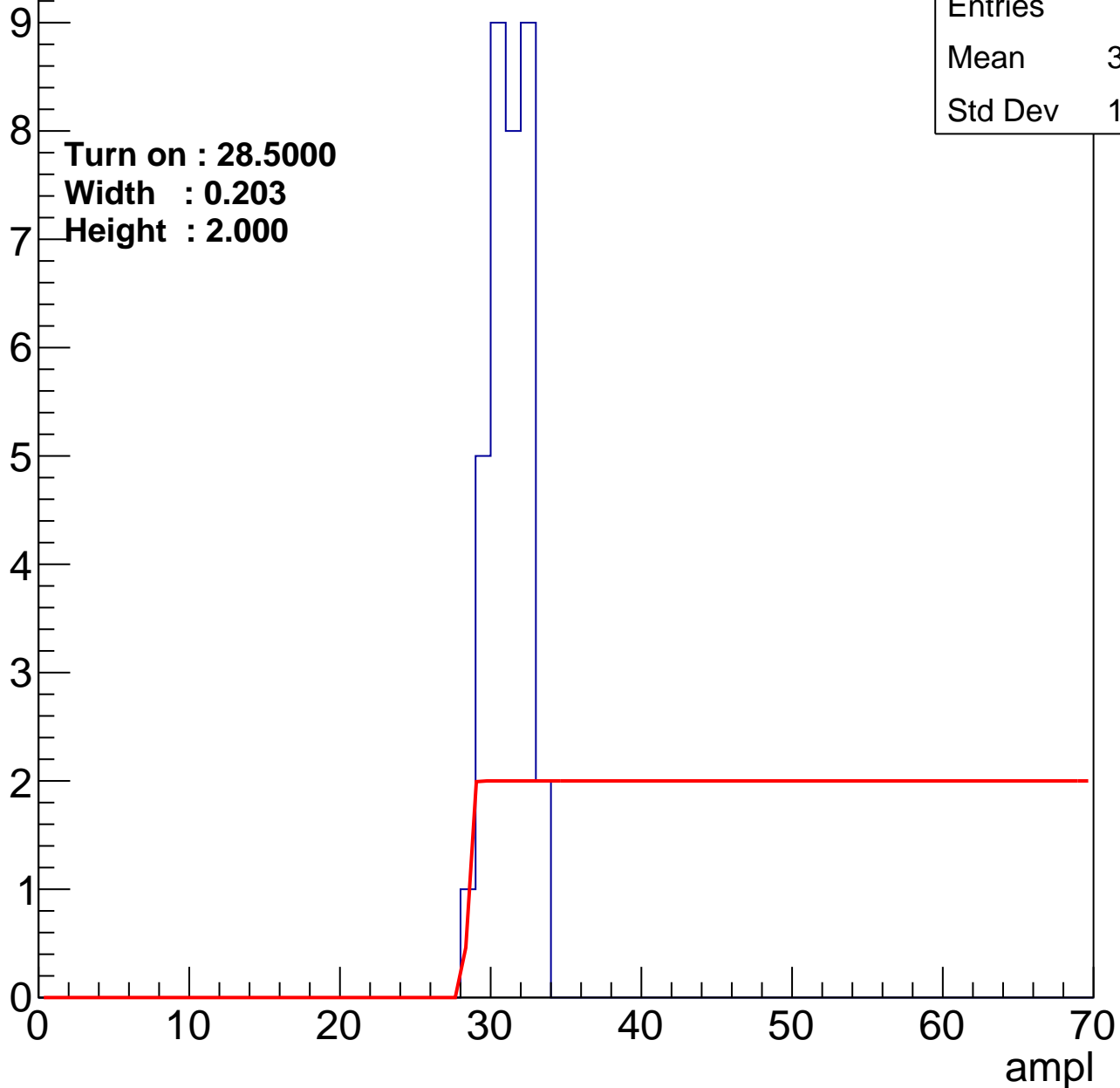


Entries	0
Mean	0
Std Dev	0

# B0L100S, U18-ch86

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	34
Mean	30.74
Std Dev	1.244



# B0L100S, U18-ch87

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry

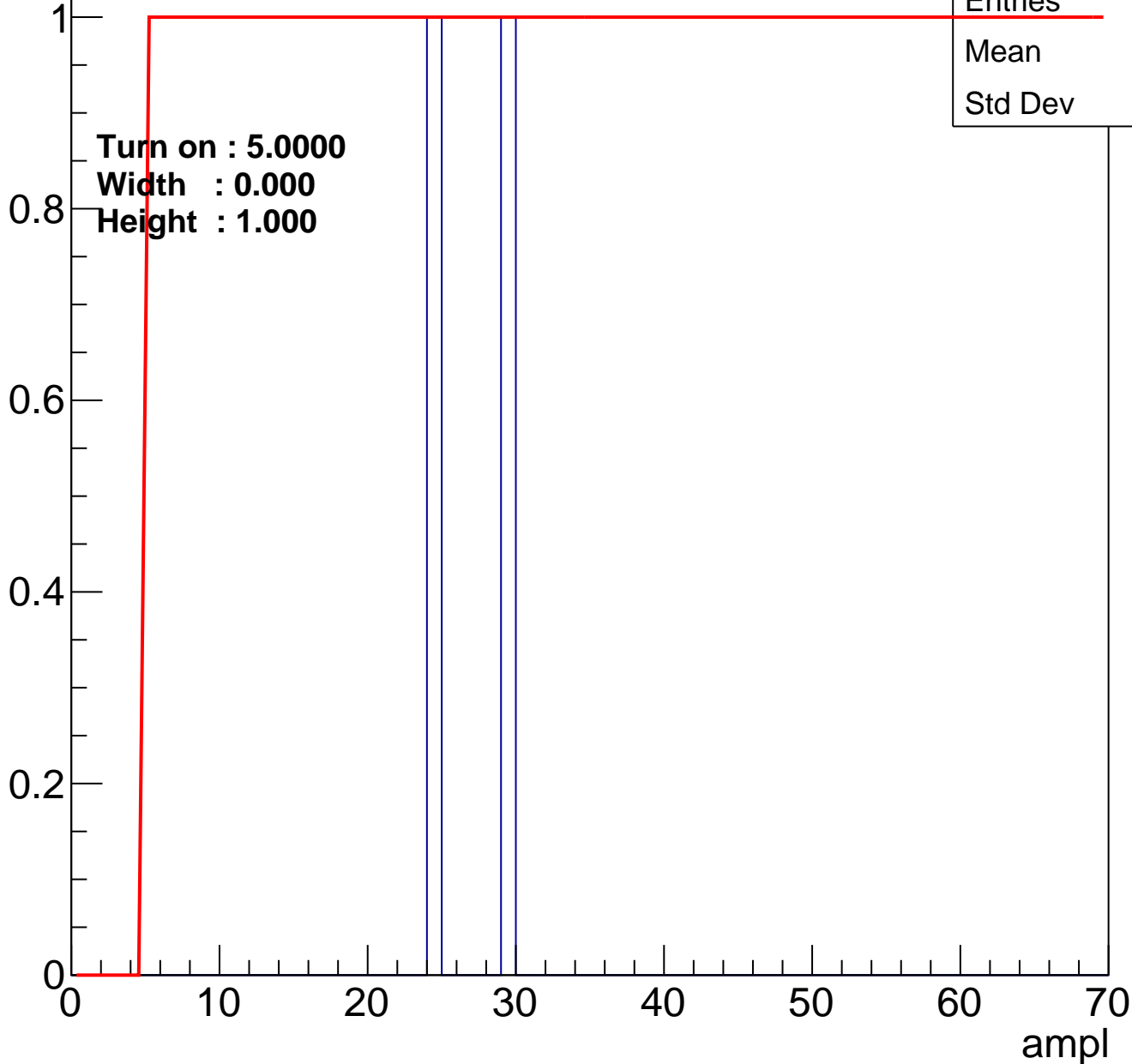


Entries	1
Mean	0
Std Dev	0

# B0L100S, U18-ch88

calib\_packv5\_042523\_0143.root, FC#6, port A1

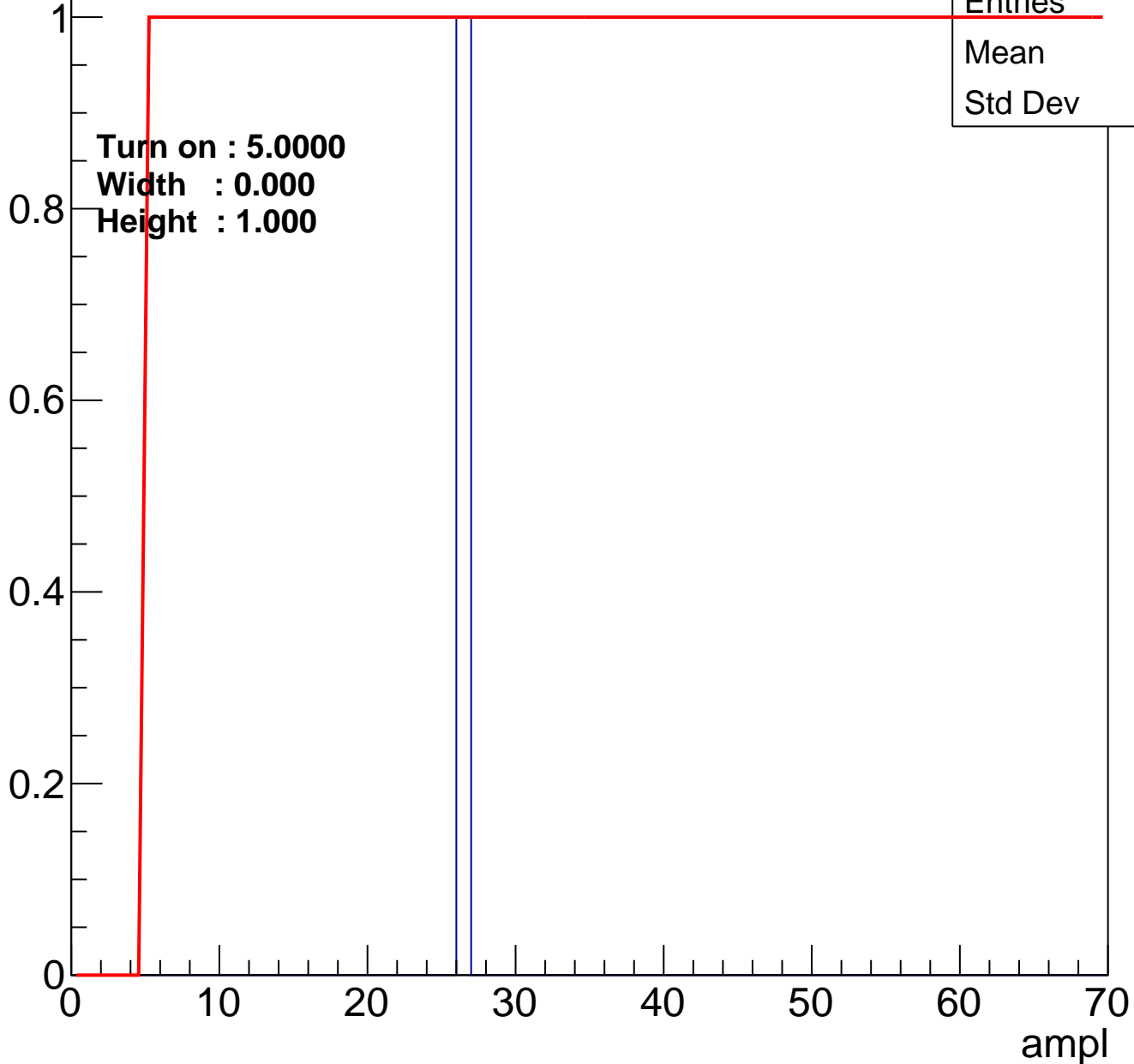
Entry



# B0L100S, U18-ch89

calib\_packv5\_042523\_0143.root, FC#6, port A1

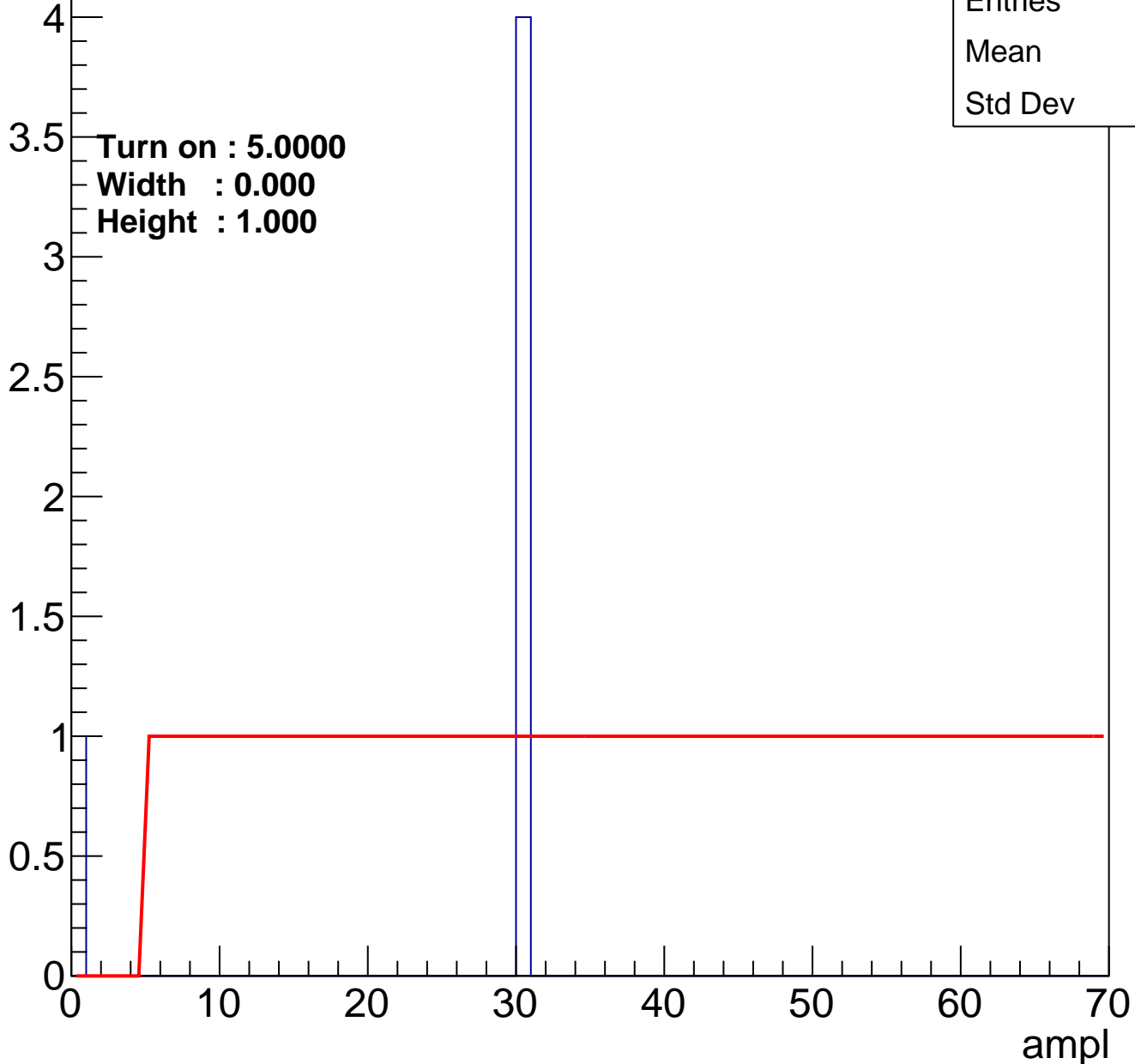
Entry



# B0L100S, U18-ch90

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry

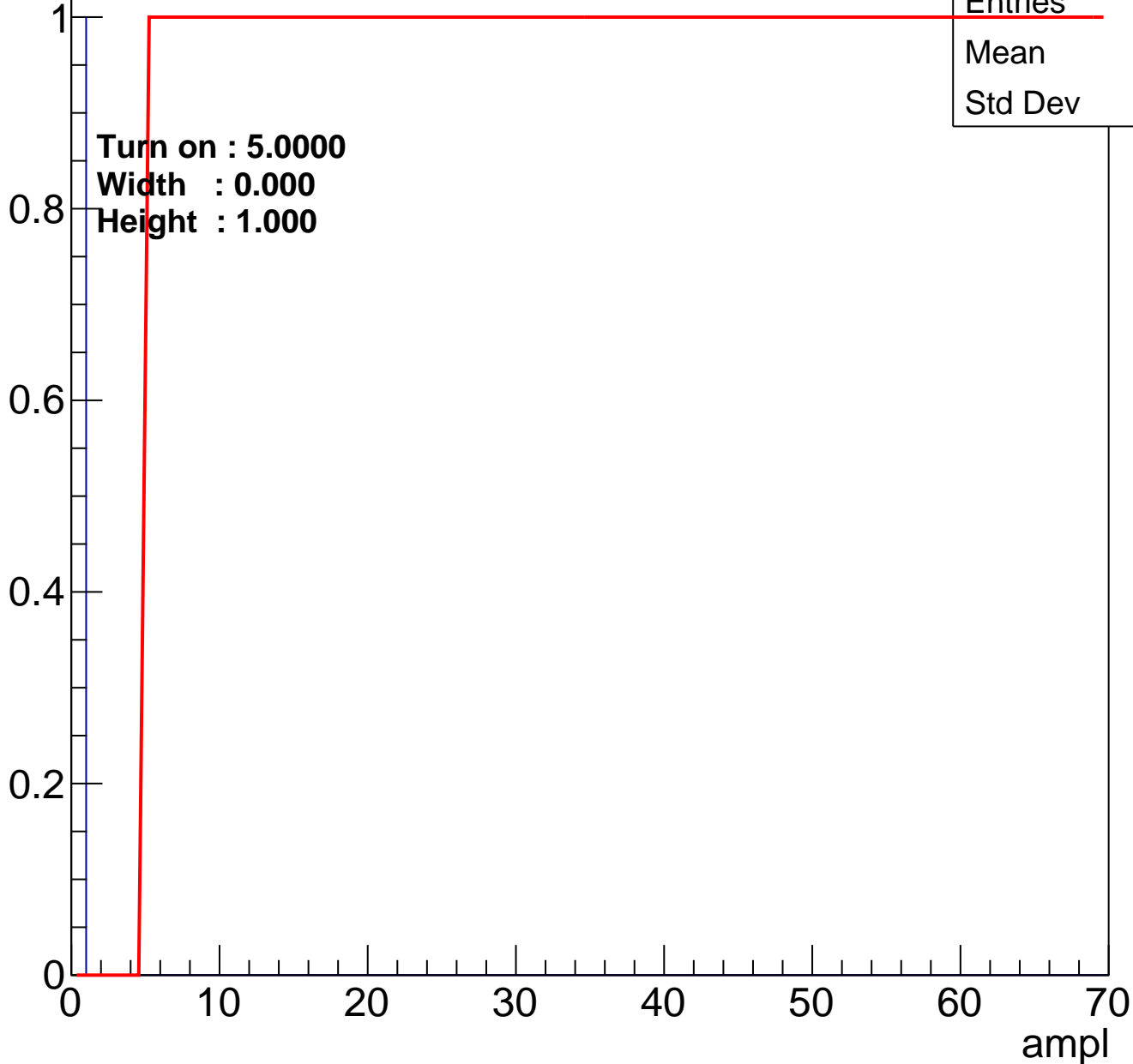


Entries	5
Mean	24
Std Dev	12

# B0L100S, U18-ch91

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



# B0L100S, U18-ch92

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry

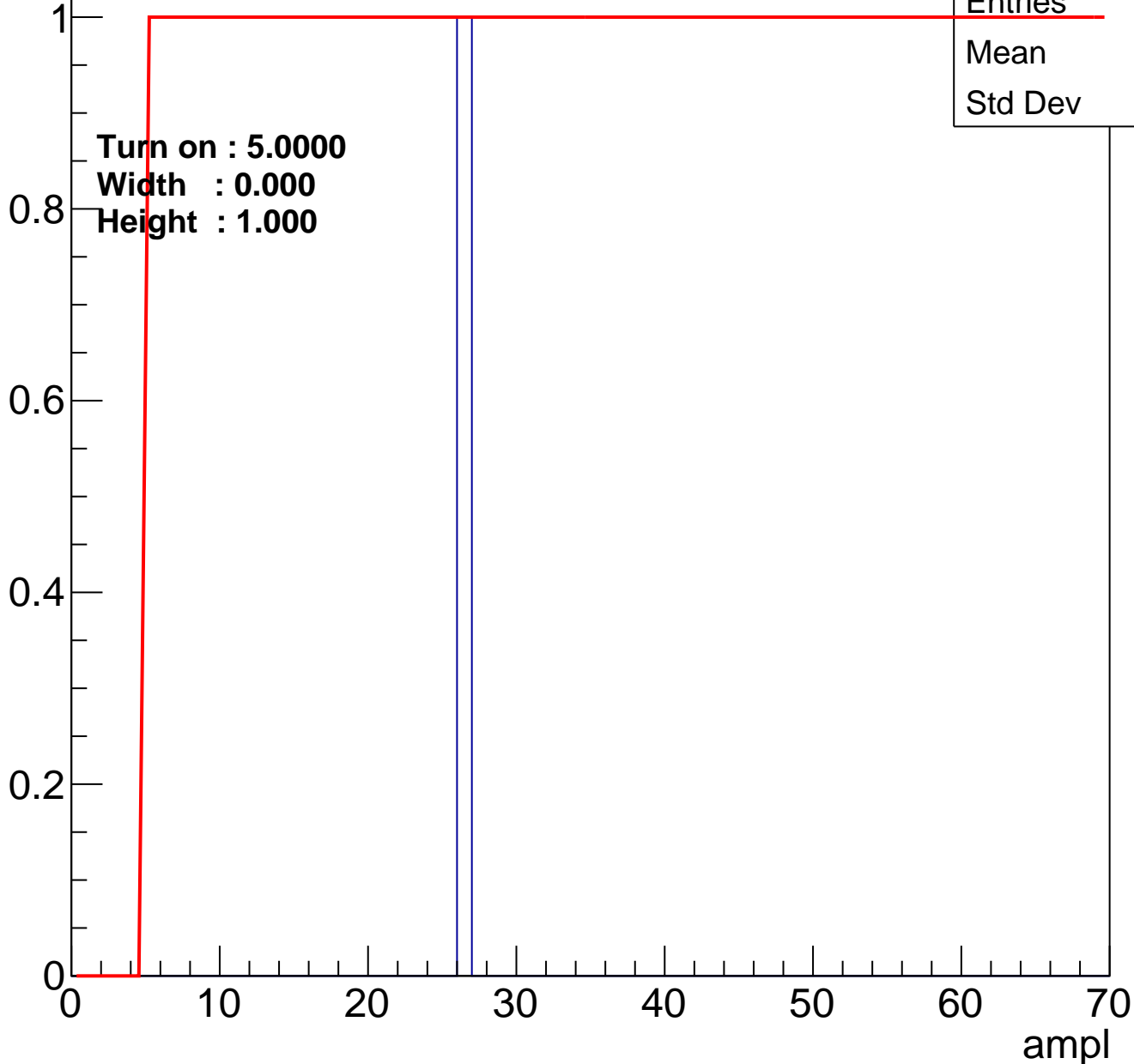


Entries	0
Mean	0
Std Dev	0

# B0L100S, U18-ch93

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	1
Mean	26
Std Dev	0

# B0L100S, U18-ch94

calib\_packv5\_042523\_0143.root, FC#6, port A1

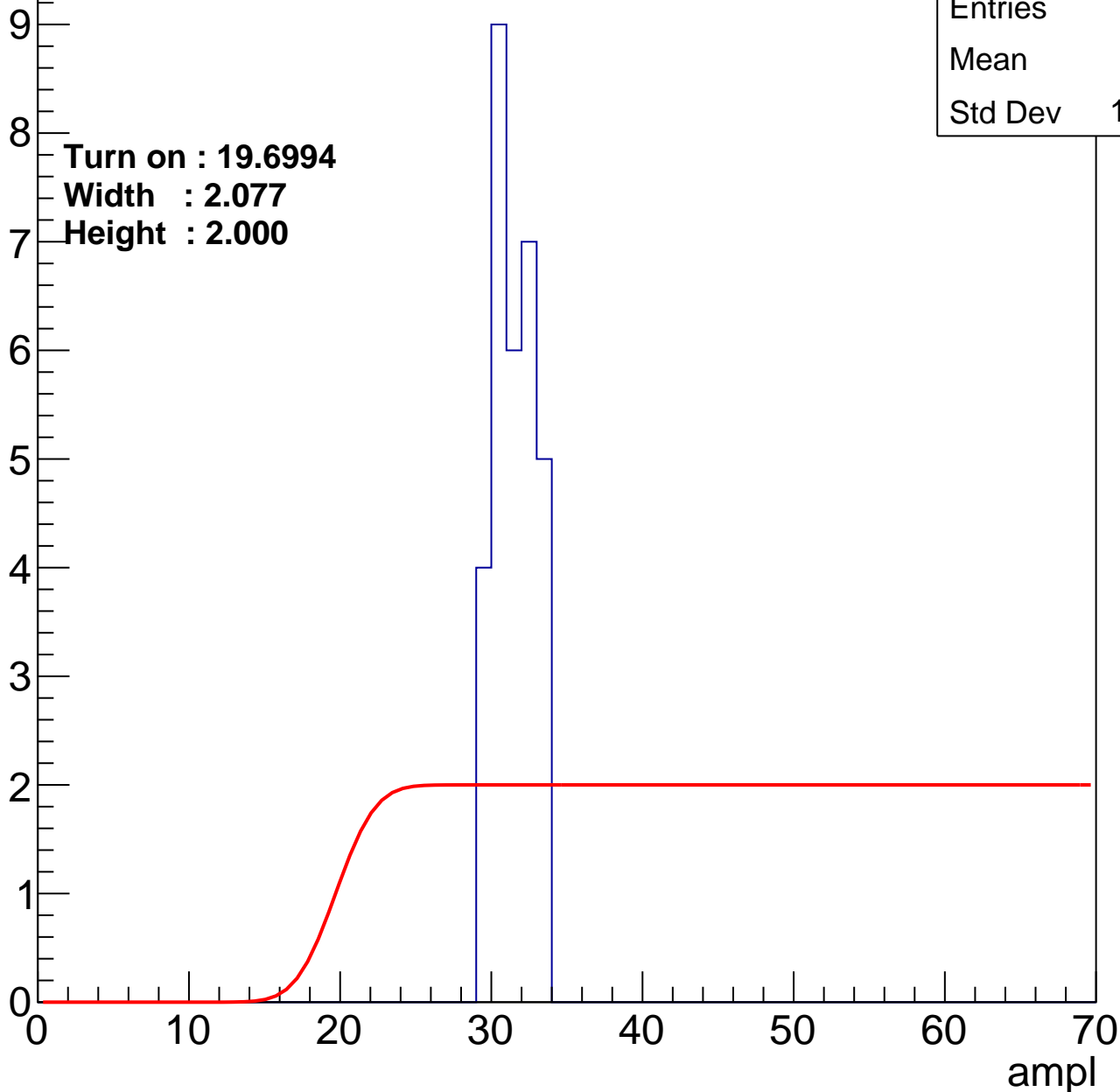
Entry

Entries	31
Mean	31
Std Dev	1.295

Turn on : 19.6994

Width : 2.077

Height : 2.000

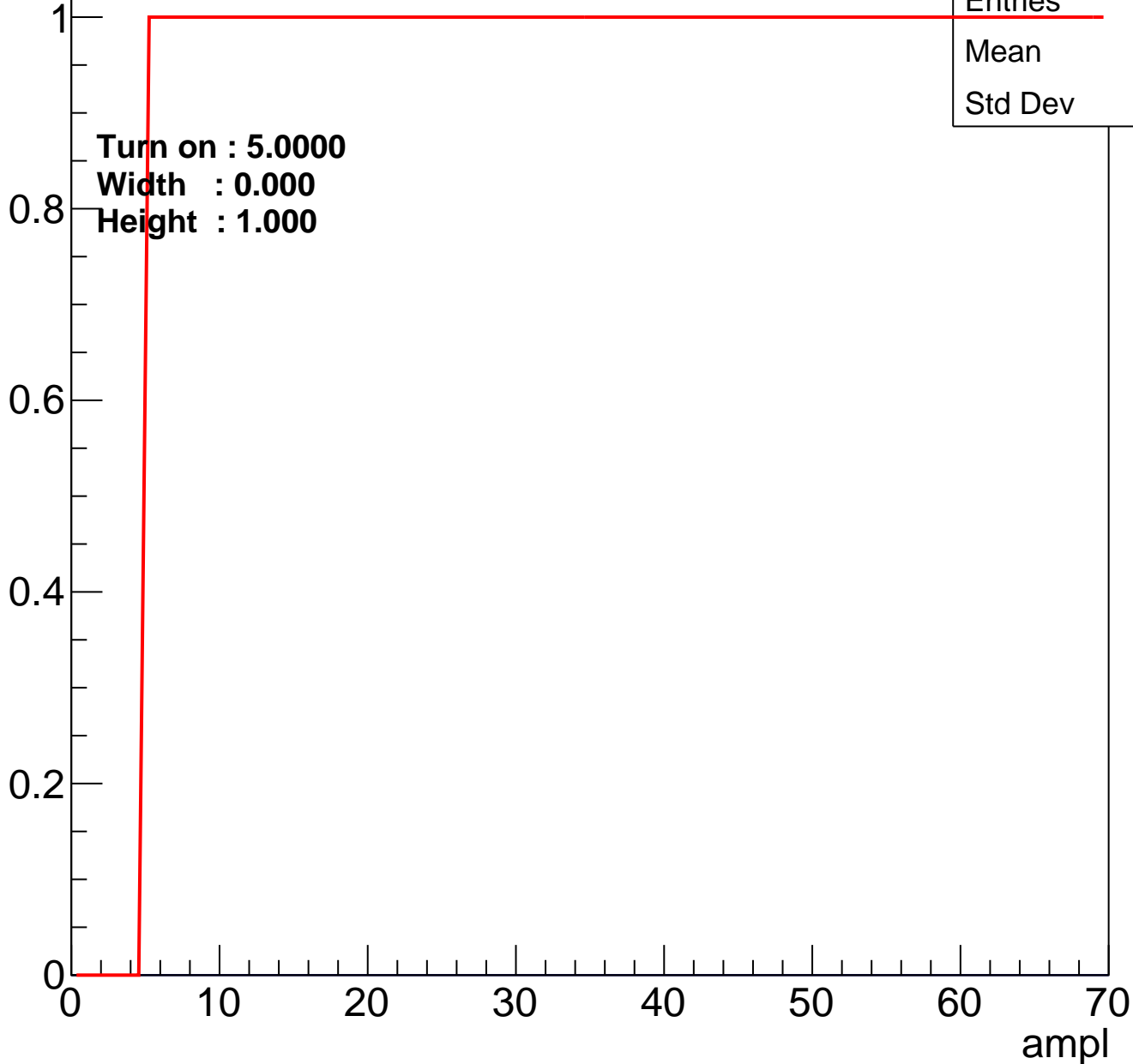




# B0L100S, U18-ch95

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U18-ch96

calib\_packv5\_042523\_0143.root, FC#6, port A1

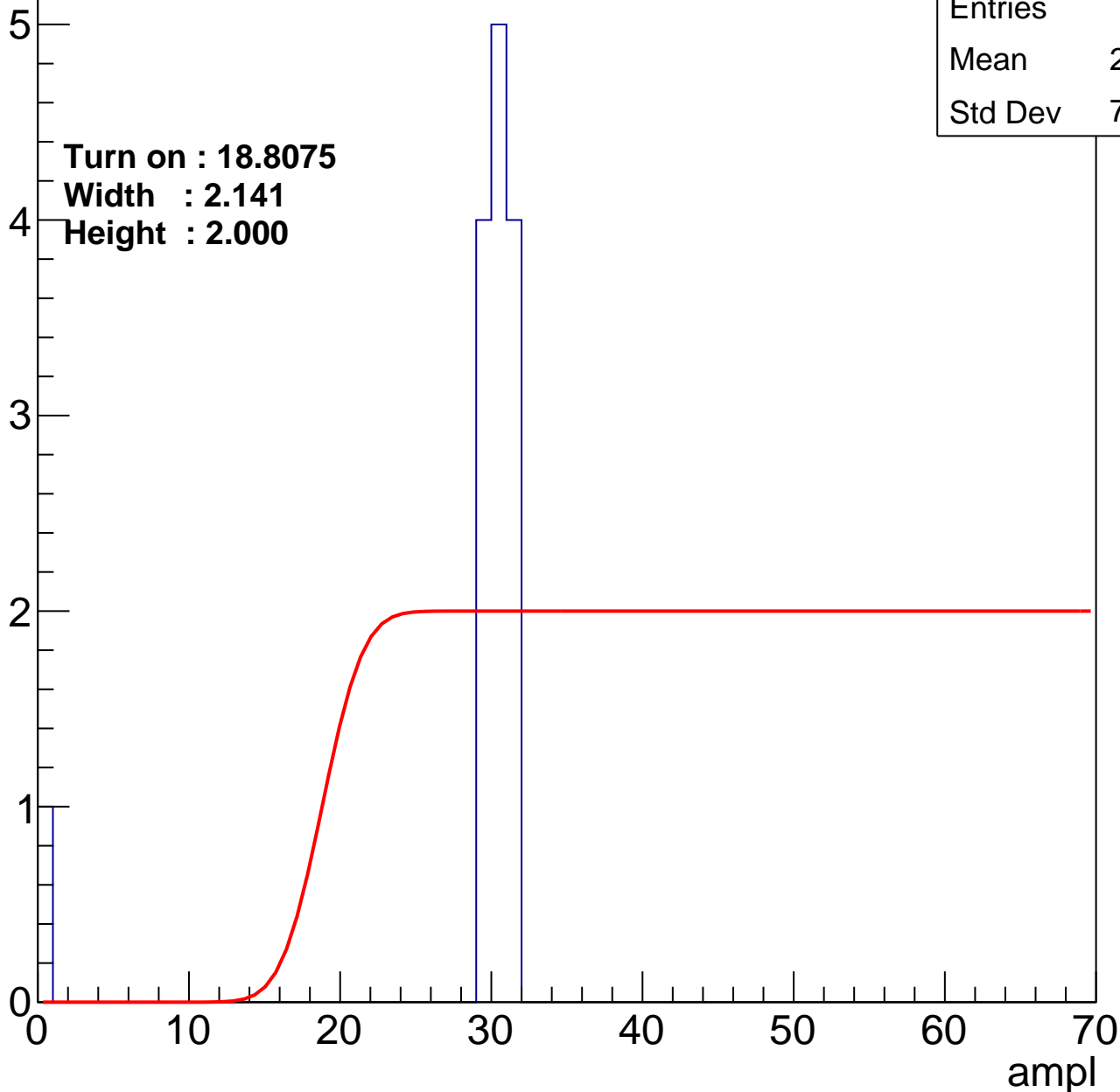
Entry

Entries	14
Mean	27.86
Std Dev	7.763

Turn on : 18.8075

Width : 2.141

Height : 2.000



# B0L100S, U18-ch97

calib\_packv5\_042523\_0143.root, FC#6, port A1

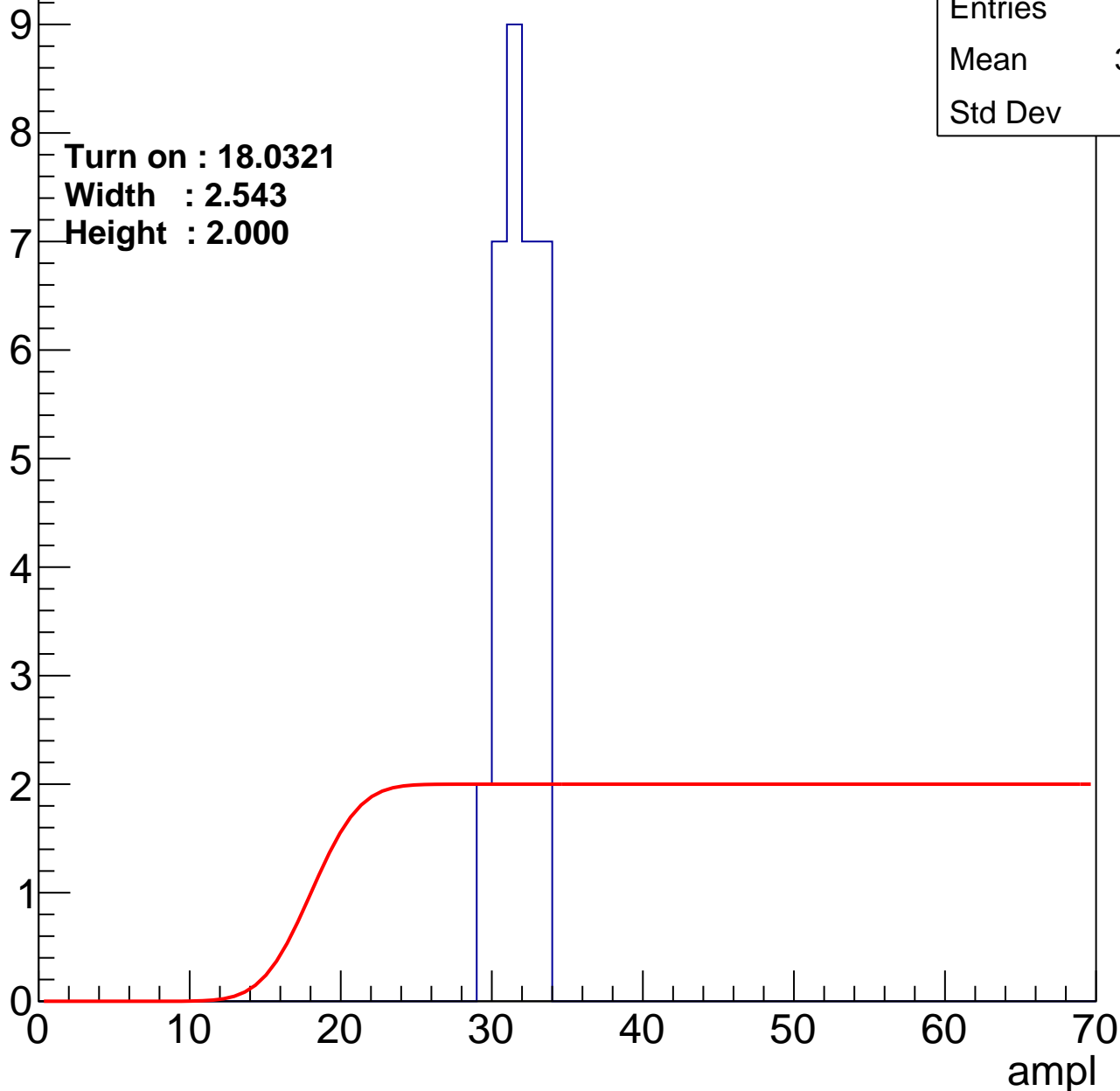
Entry

Entries	32
Mean	31.31
Std Dev	1.21

Turn on : 18.0321

Width : 2.543

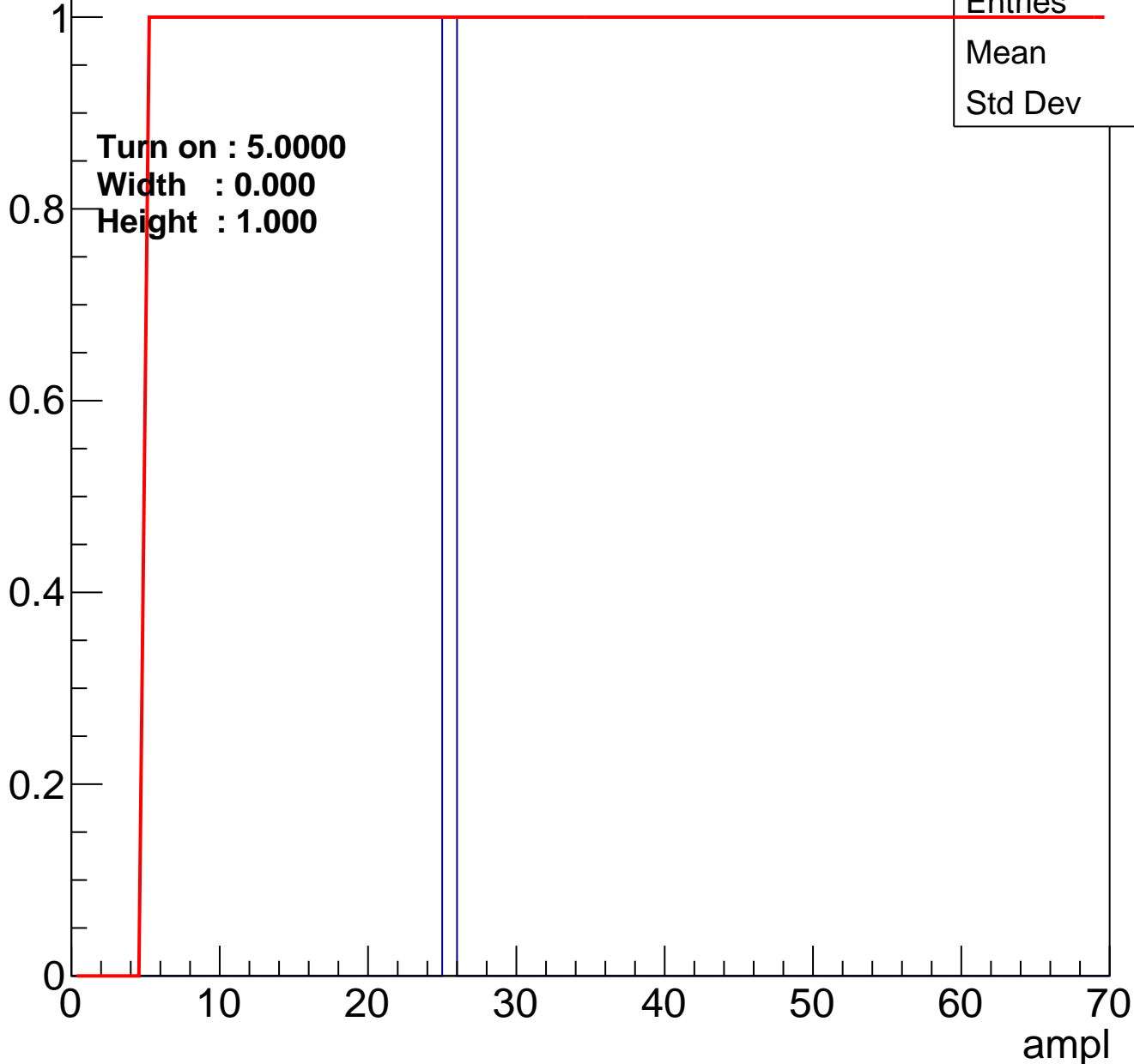
Height : 2.000



# B0L100S, U18-ch98

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	1
Mean	25
Std Dev	0

# B0L100S, U18-ch99

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U18-ch100

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U18-ch101

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U18-ch102

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L100S, U18-ch103

calib\_packv5\_042523\_0143.root, FC#6, port A1

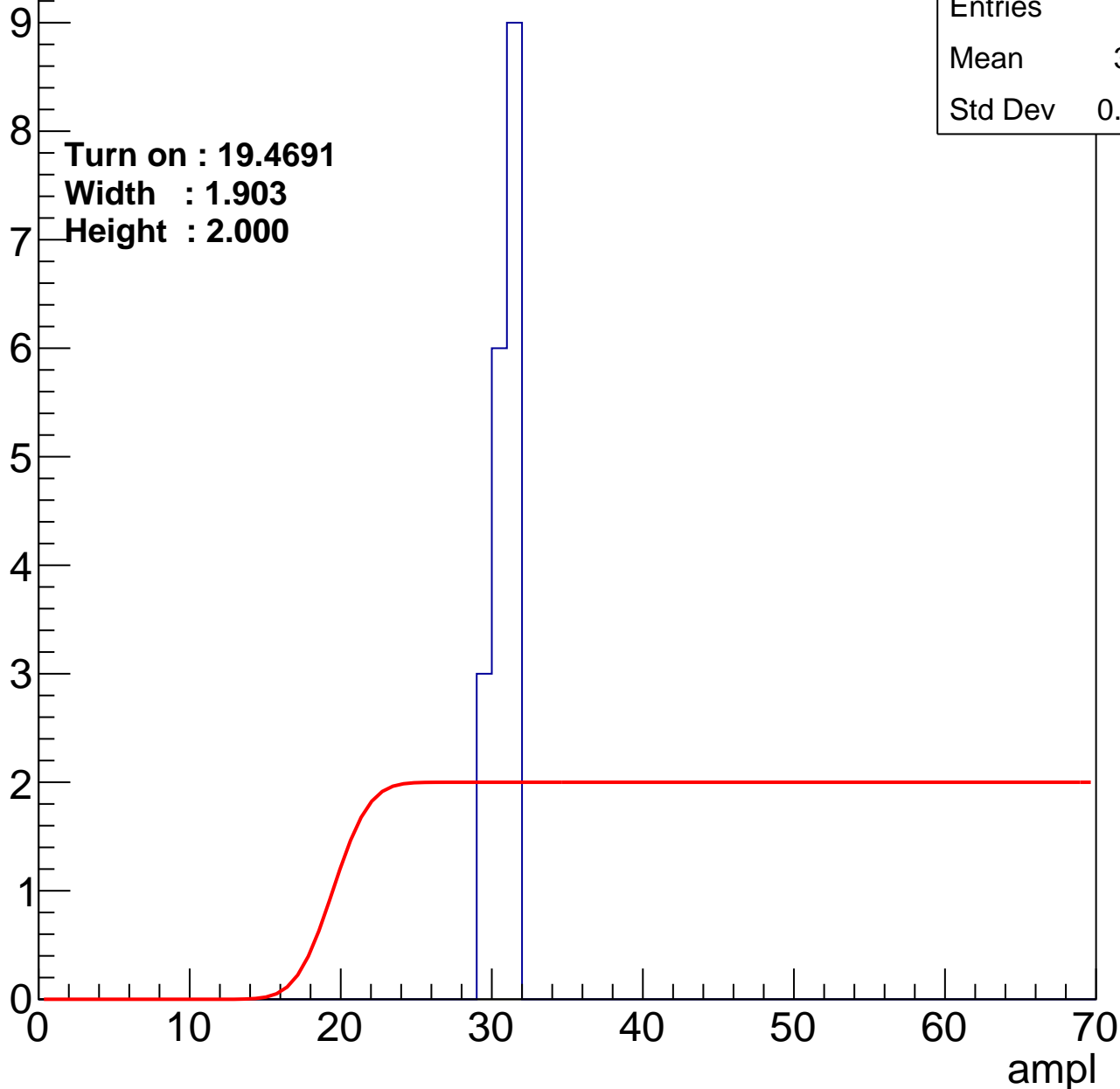
Entry



# B0L100S, U18-ch104

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



# B0L100S, U18-ch105

calib\_packv5\_042523\_0143.root, FC#6, port A1

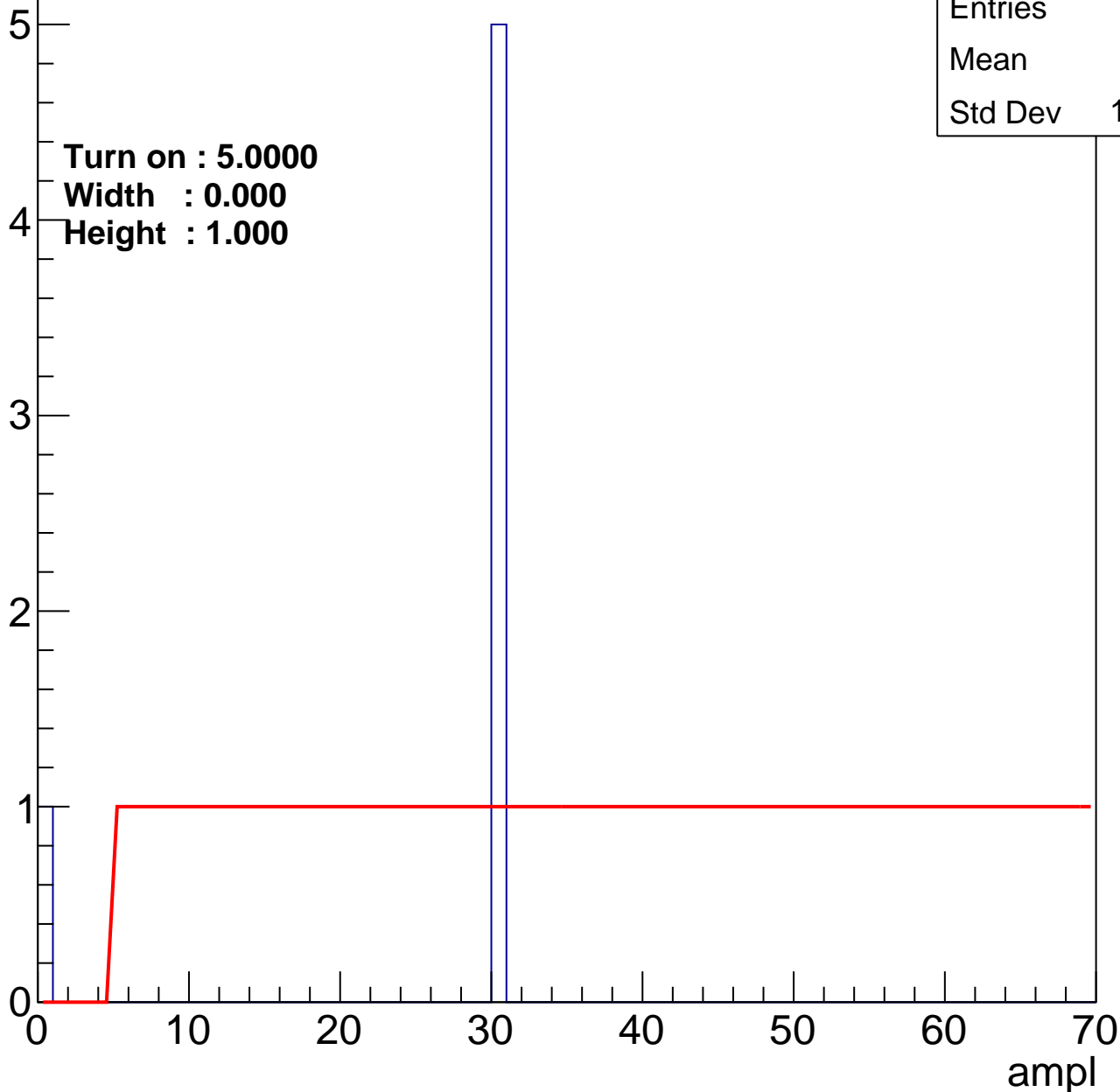
Entry

Entries	6
Mean	25
Std Dev	11.18

Turn on : 5.0000

Width : 0.000

Height : 1.000



# B0L100S, U18-ch106

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U18-ch107

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U18-ch108

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U18-ch109

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L100S, U18-ch110

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	1
Mean	0
Std Dev	0



# B0L100S, U18-ch111

calib\_packv5\_042523\_0143.root, FC#6, port A1

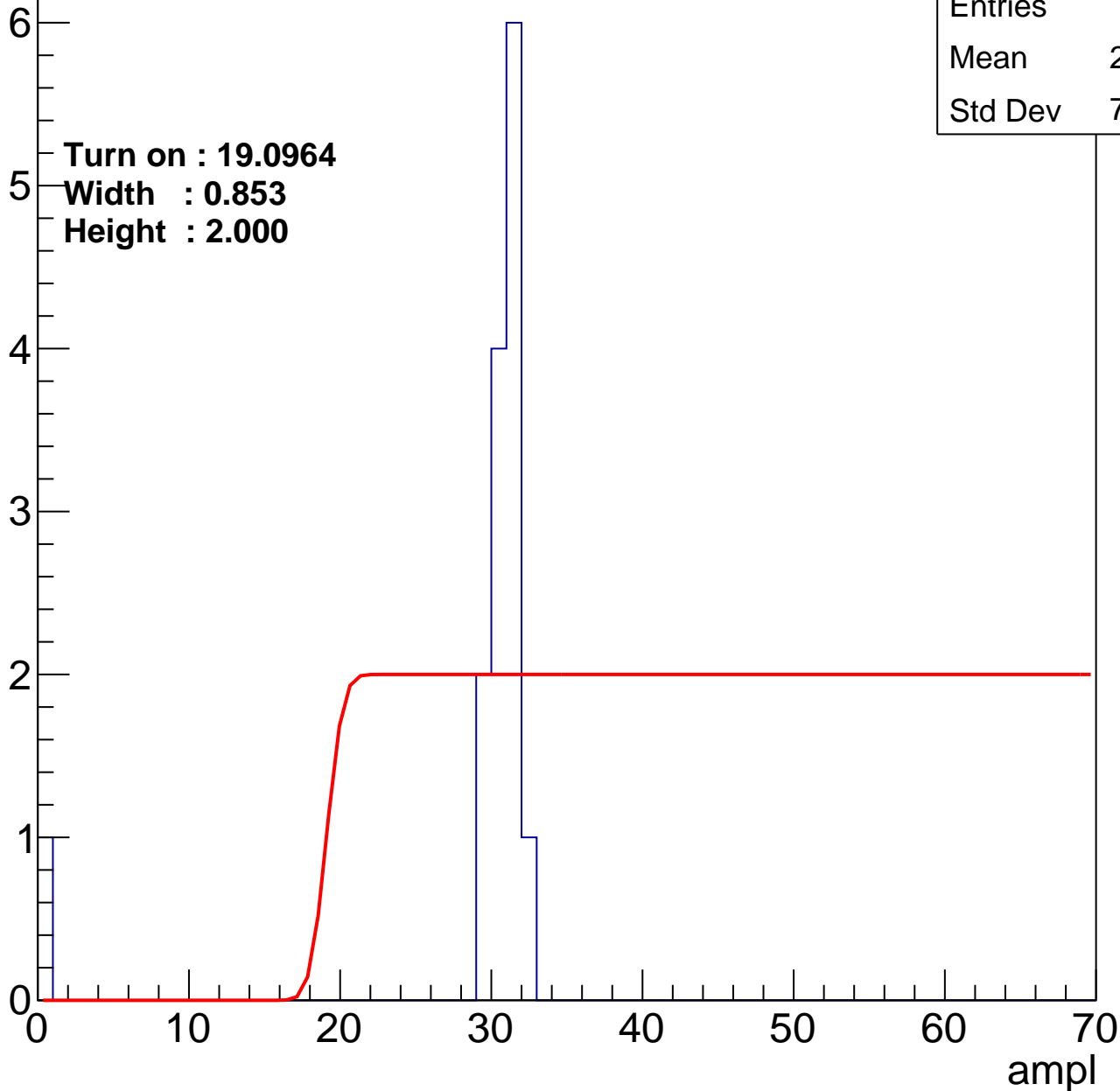
Entry

Entries	14
Mean	28.29
Std Dev	7.887

Turn on : 19.0964

Width : 0.853

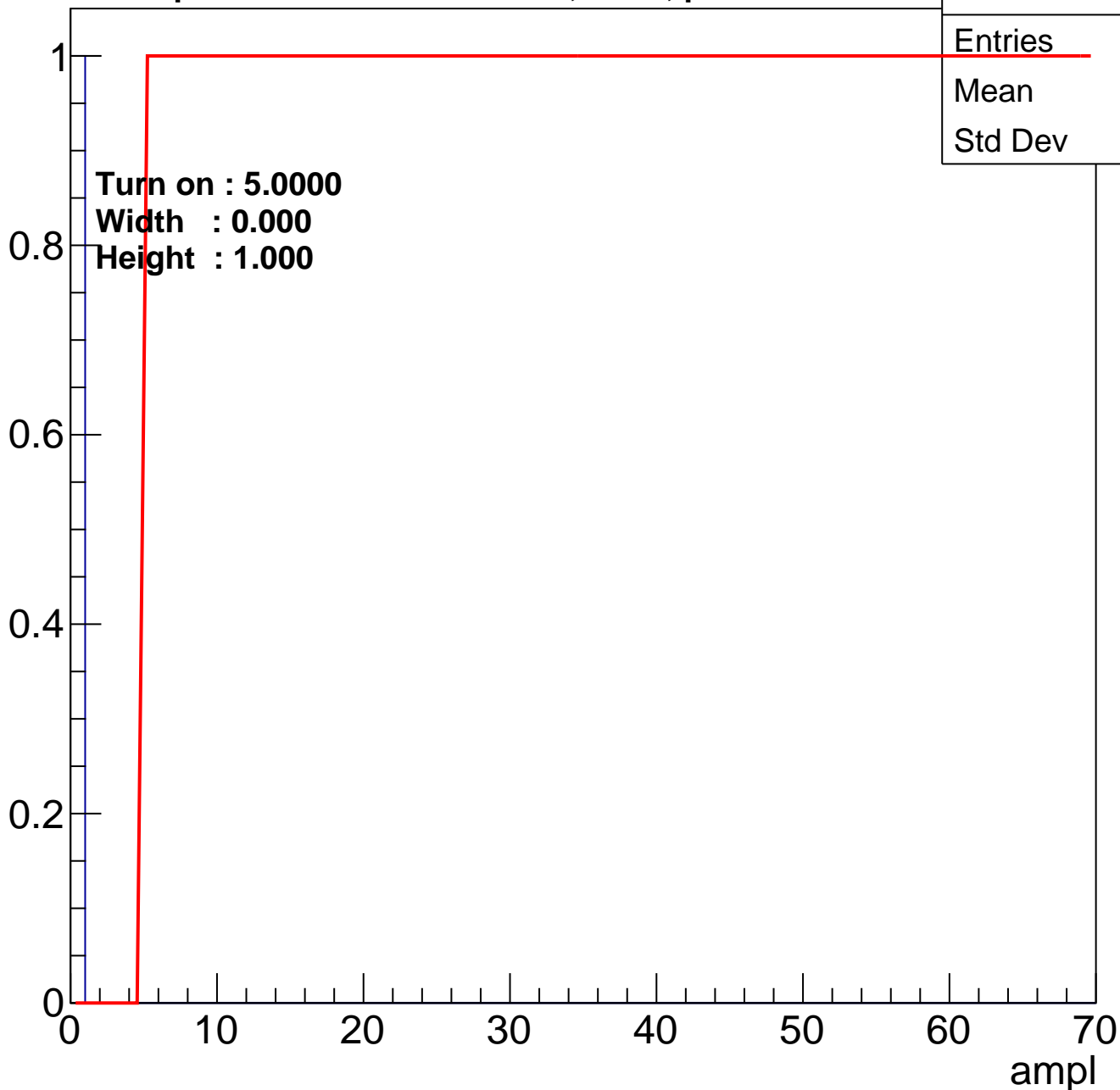
Height : 2.000



# B0L100S, U18-ch112

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L100S, U18-ch113

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U18-ch114

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



# B0L100S, U18-ch115

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U18-ch116

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L100S, U18-ch117

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U18-ch118

calib\_packv5\_042523\_0143.root, FC#6, port A1

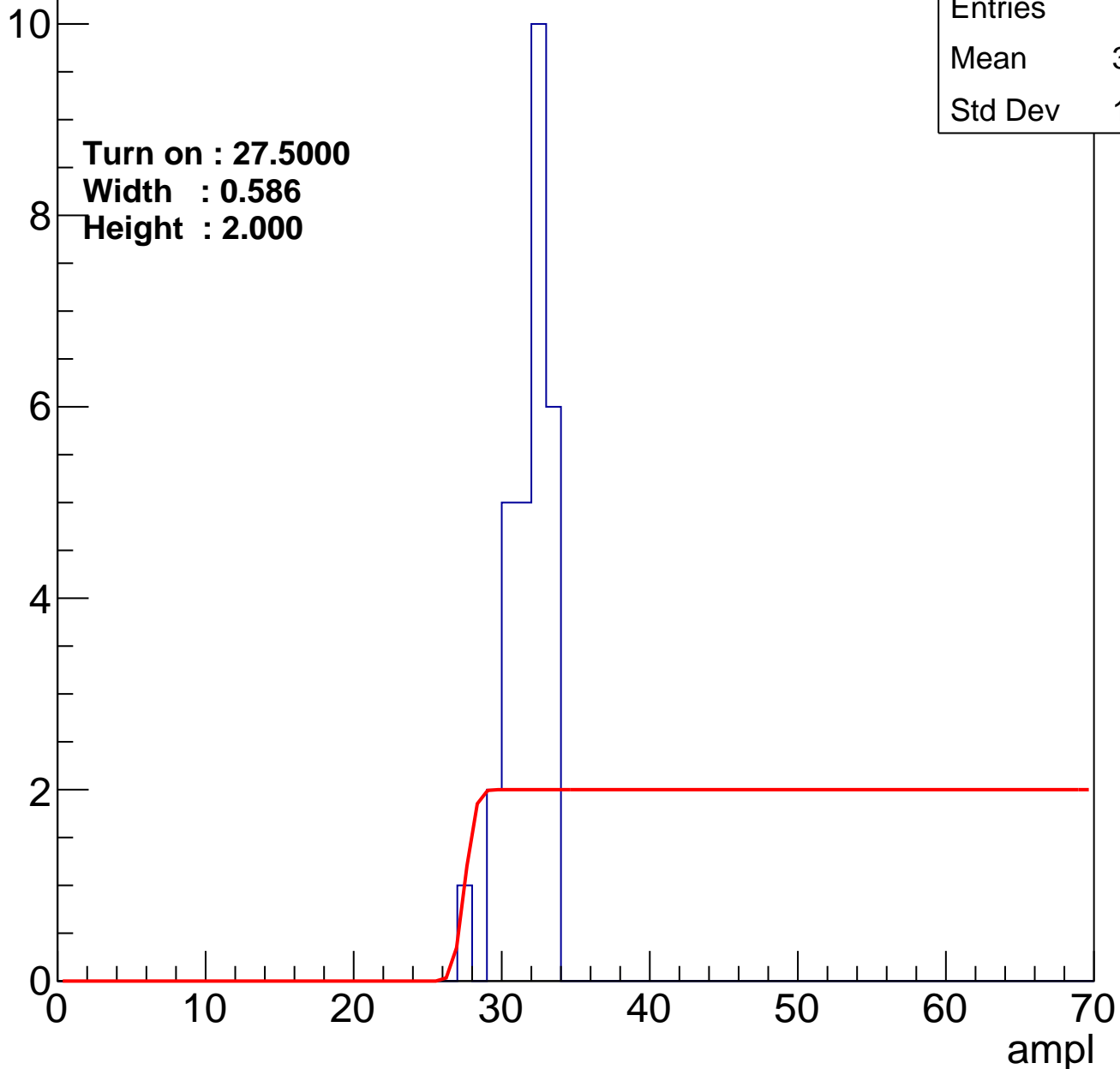
Entries	29
Mean	31.31
Std Dev	1.441

**Turn on : 27.5000**

**Width : 0.586**

**Height : 2.000**

Entry





# B0L100S, U18-ch119

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U18-ch120

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U18-ch121

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L100S, U18-ch122

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U18-ch123

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry

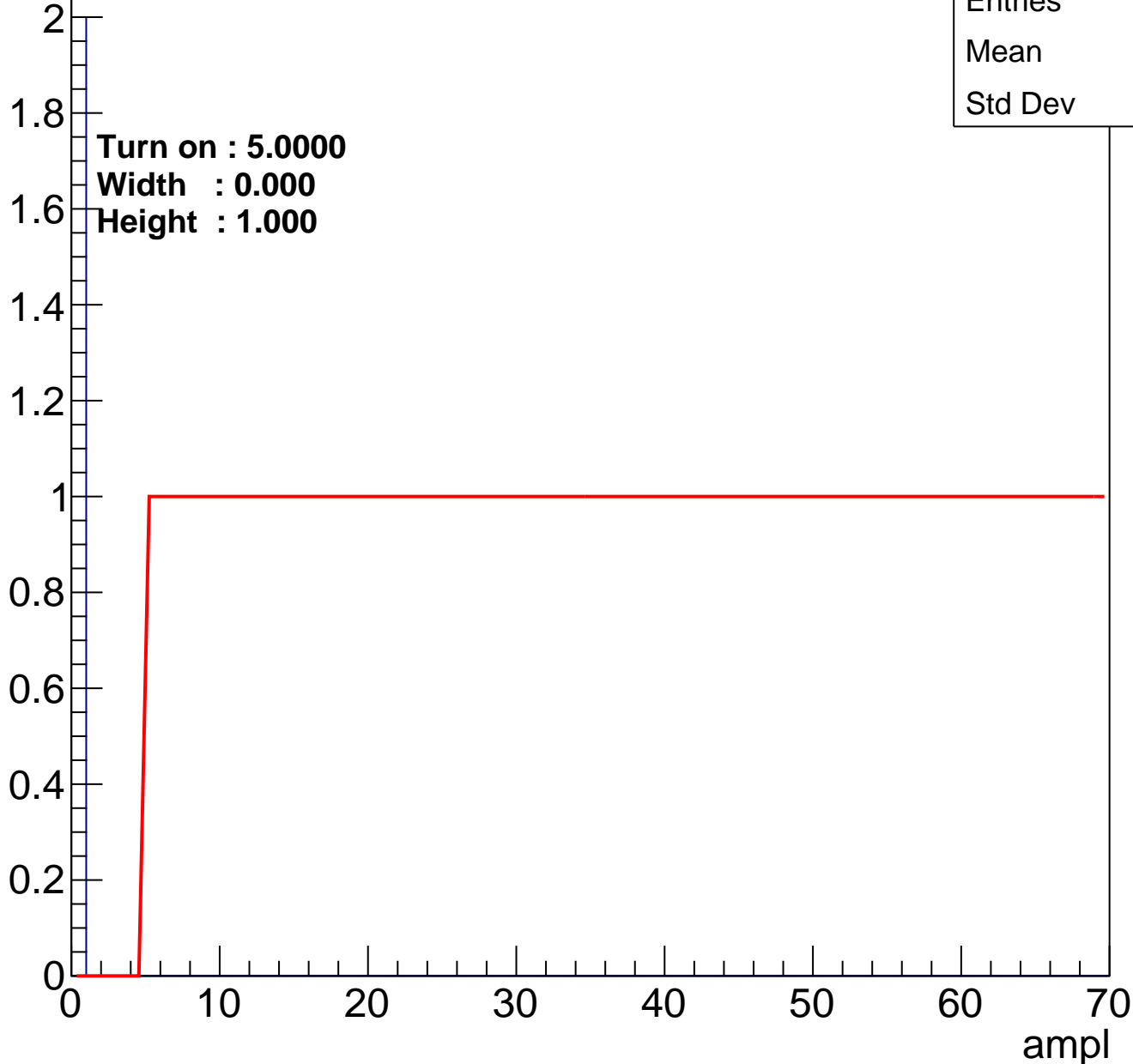


Entries	0
Mean	0
Std Dev	0

# B0L100S, U18-ch124

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L100S, U18-ch125

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



# B0L100S, U18-ch126

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L100S, U18-ch127

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry

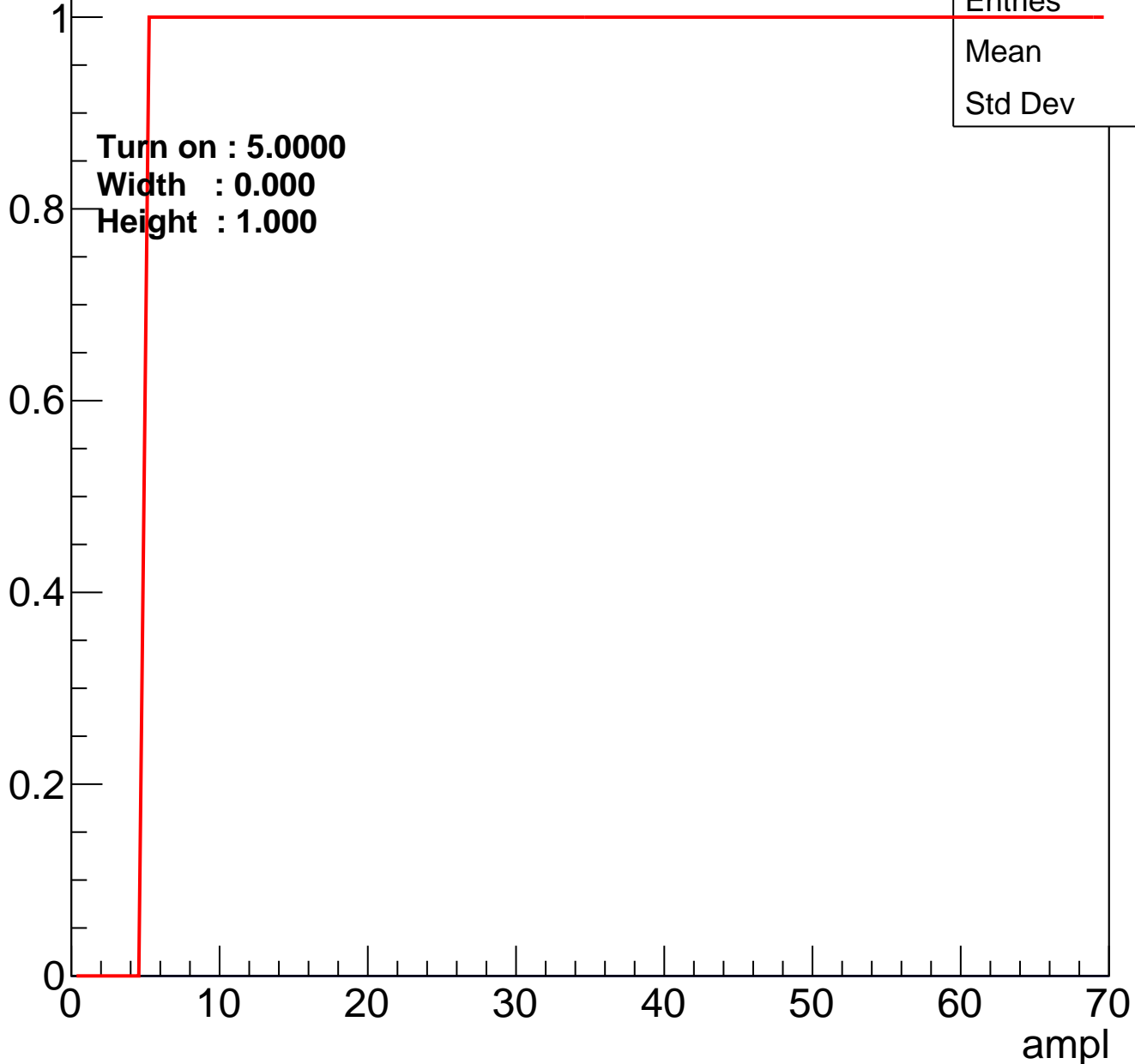


Entries	0
Mean	0
Std Dev	0

# B0L100S, U18-ch127

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0