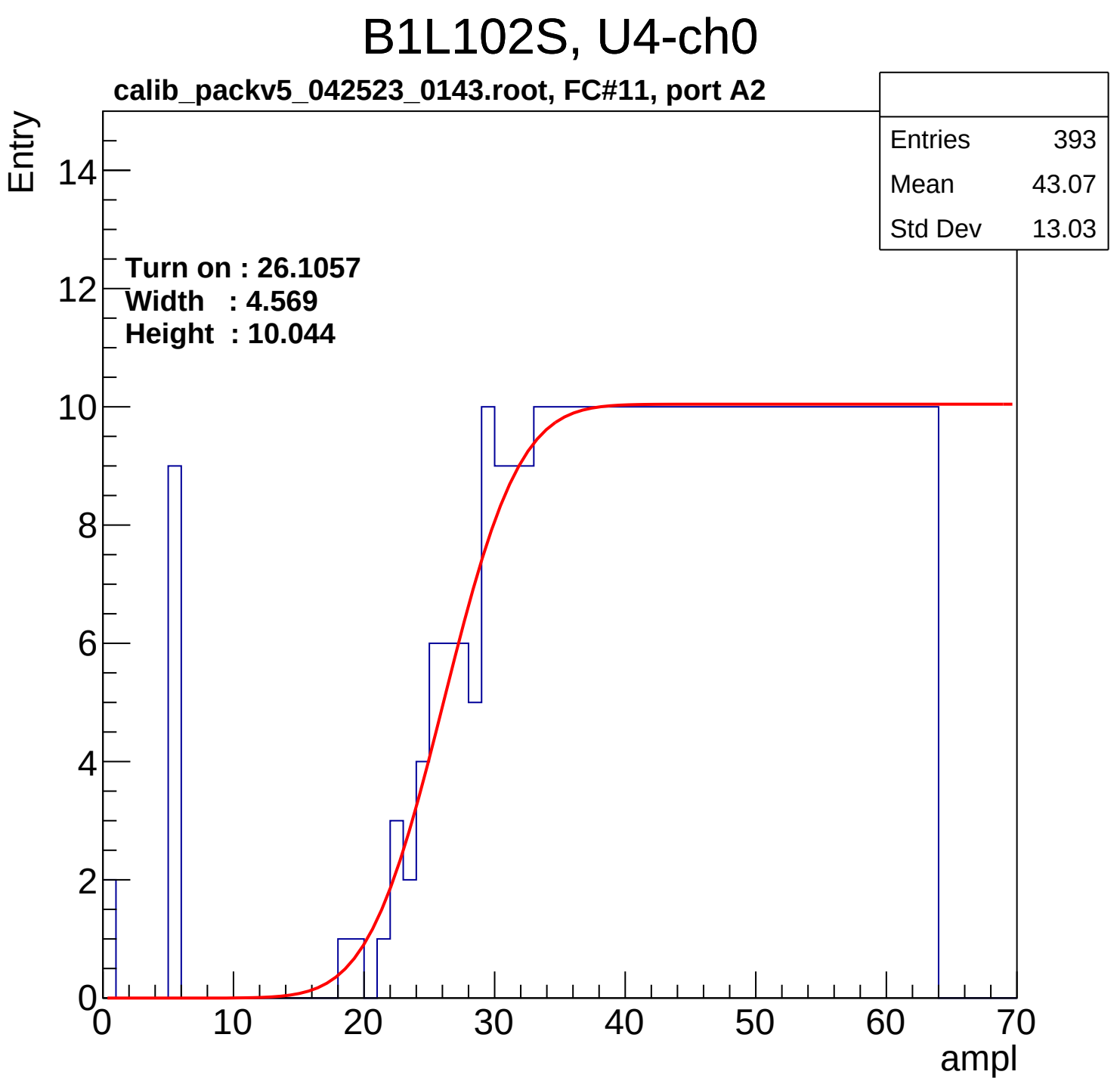
B1L102S, U4-ch0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 393
Mean 43.07
Std Dev 13.03
Turn on : 26.1057
Width : 4.569
Height : 10.044
Entry
ampl
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0
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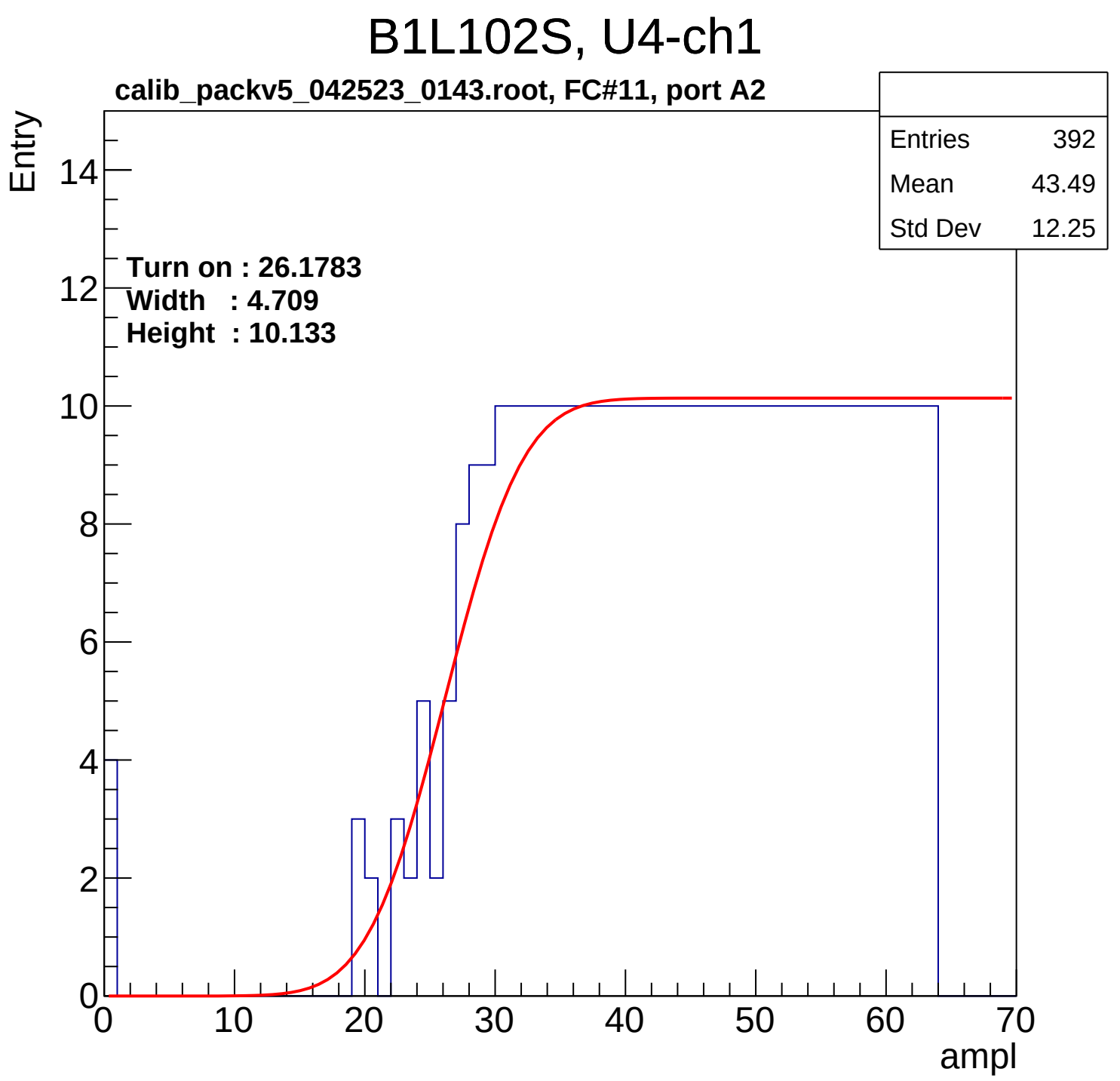
B1L102S, U4-ch1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 392
Mean 43.49
Std Dev 12.25
Turn on : 26.1783
Width : 4.709
Height : 10.133
Entry
ampl
0
2
4
6
8
10
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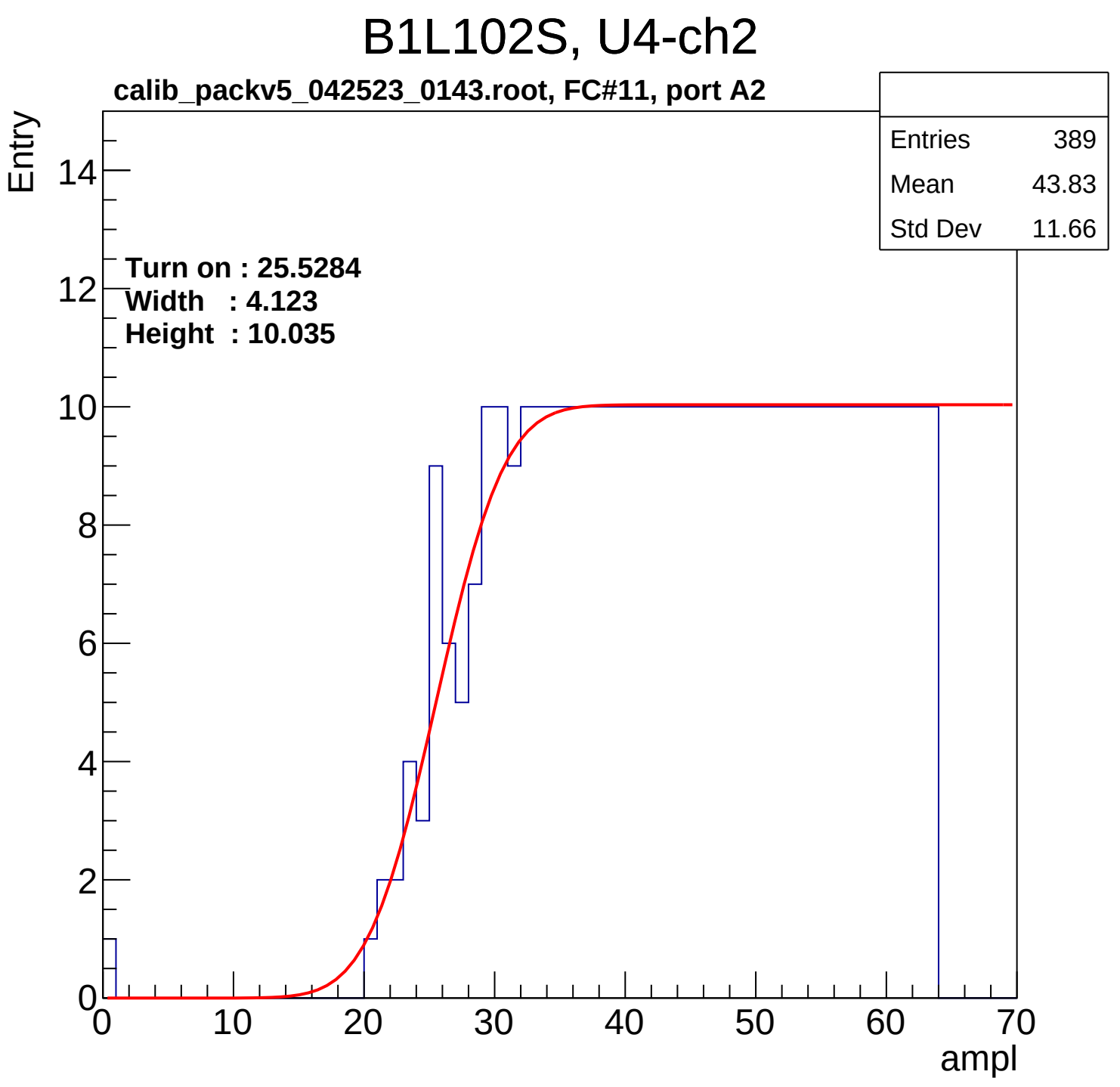
B1L102S, U4-ch2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 389
Mean 43.83
Std Dev 11.66
Turn on : 25.5284
Width : 4.123
Height : 10.035
Entry
ampl
0
2
4
6
8
10
12
14
0
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60
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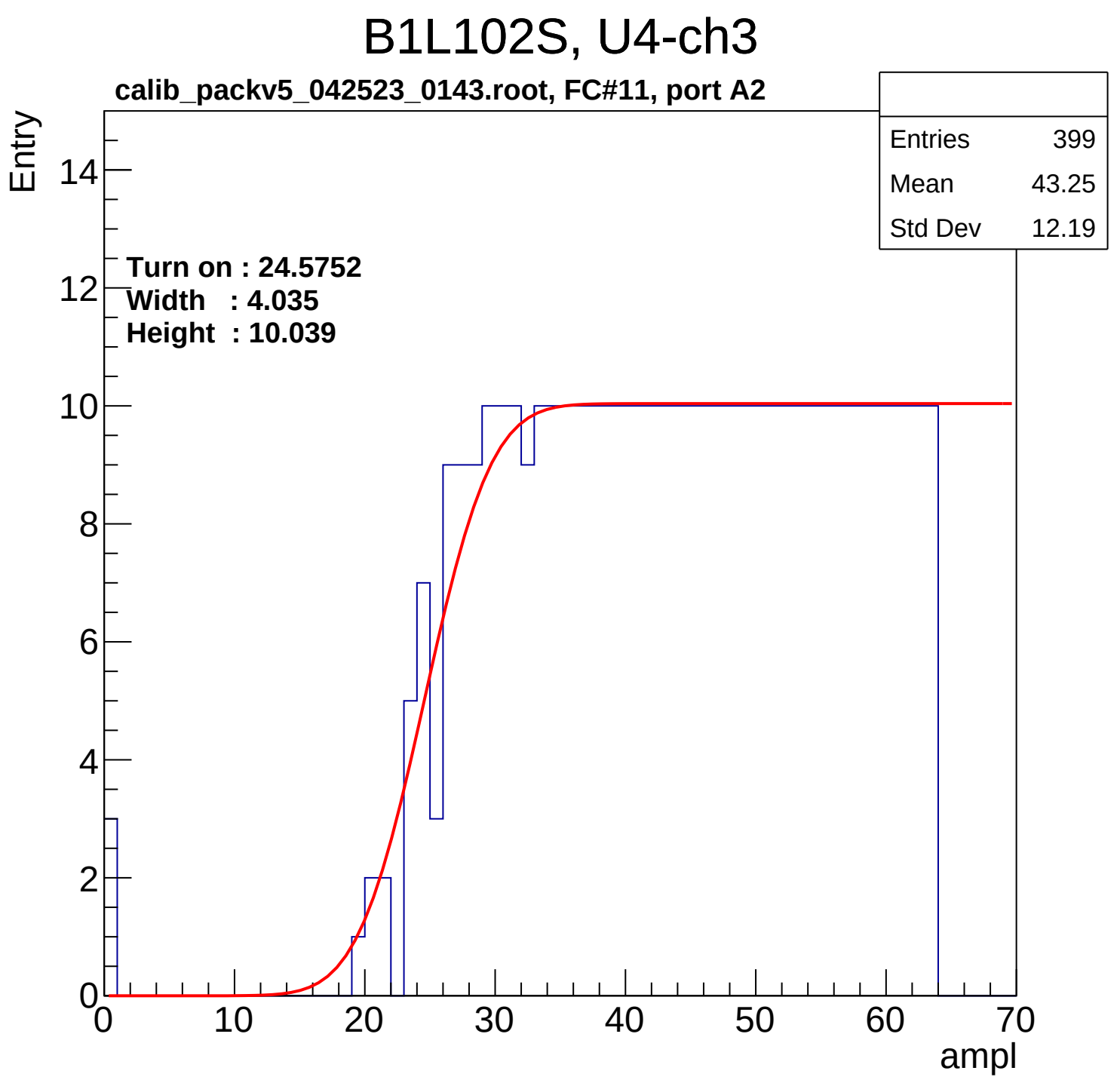
B1L102S, U4-ch3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 399
Mean 43.25
Std Dev 12.19
Turn on : 24.5752
Width : 4.035
Height : 10.039
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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60
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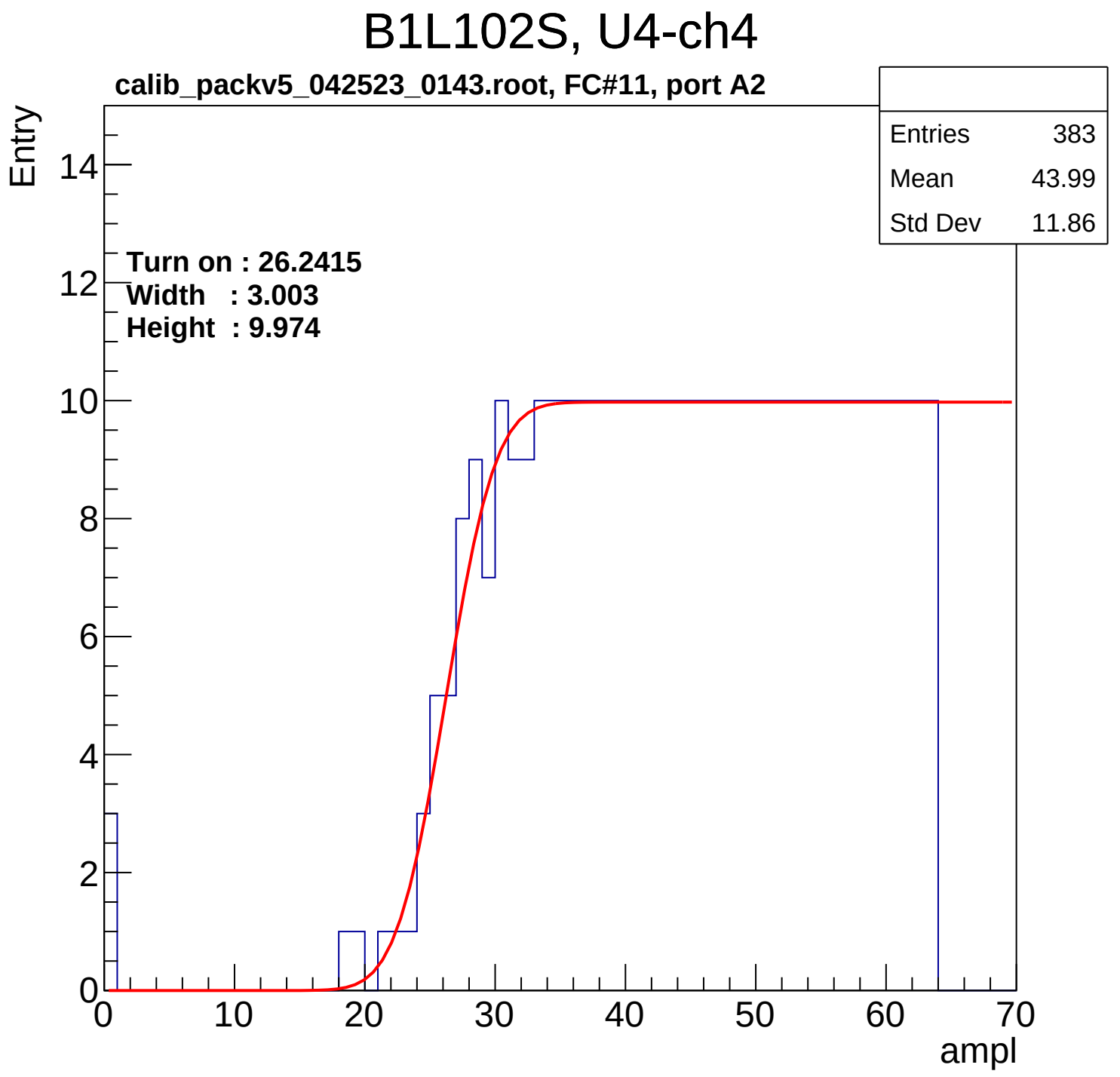
B1L102S, U4-ch4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 43.99
Std Dev 11.86
Turn on : 26.2415
Width : 3.003
Height : 9.974
Entry
ampl
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2
4
6
8
10
12
14
0
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60
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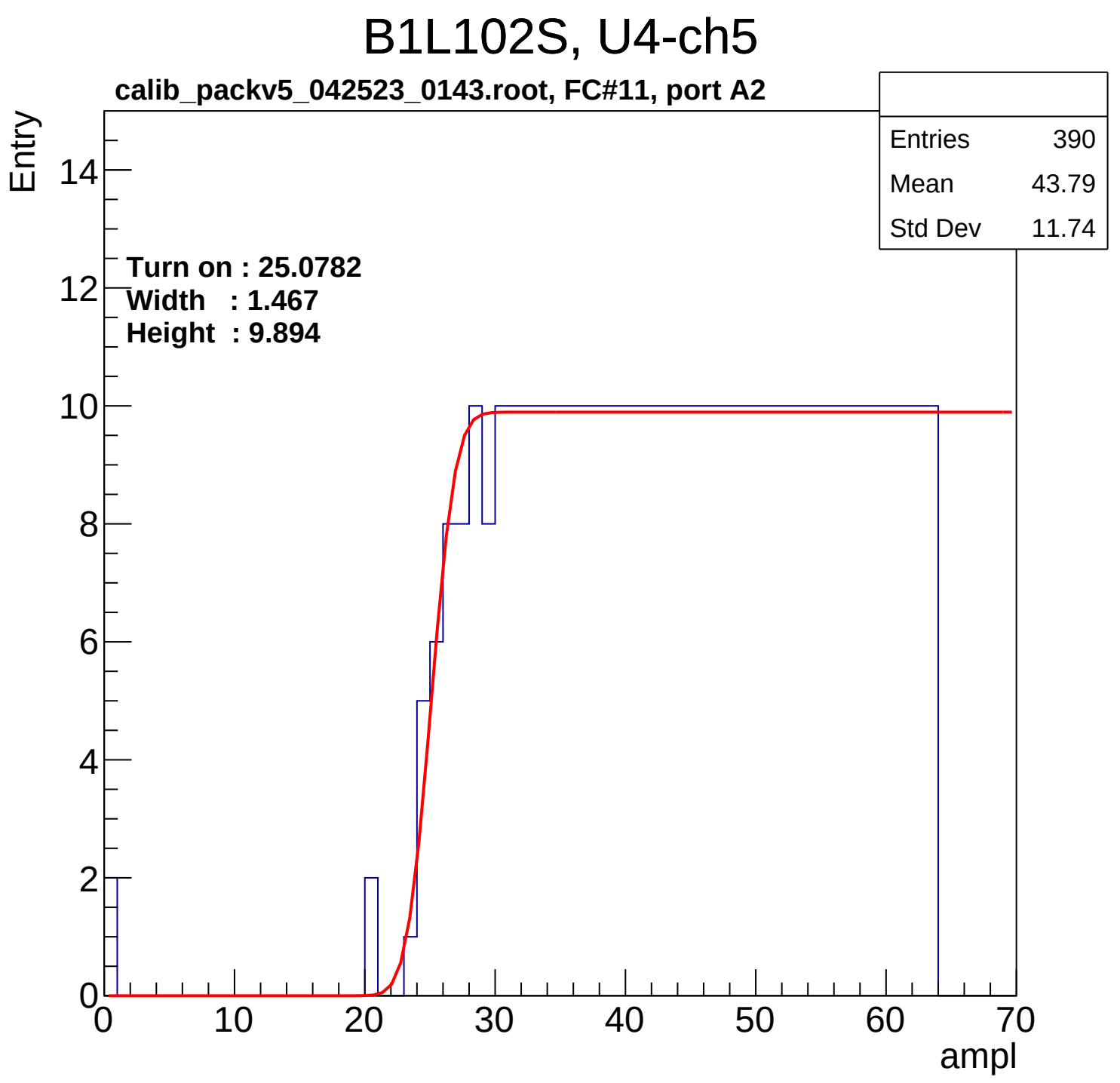
B1L102S, U4-ch5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 390
Mean 43.79
Std Dev 11.74
Turn on : 25.0782
Width : 1.467
Height : 9.894
Entry
ampl
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2
4
6
8
10
12
14
0
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60
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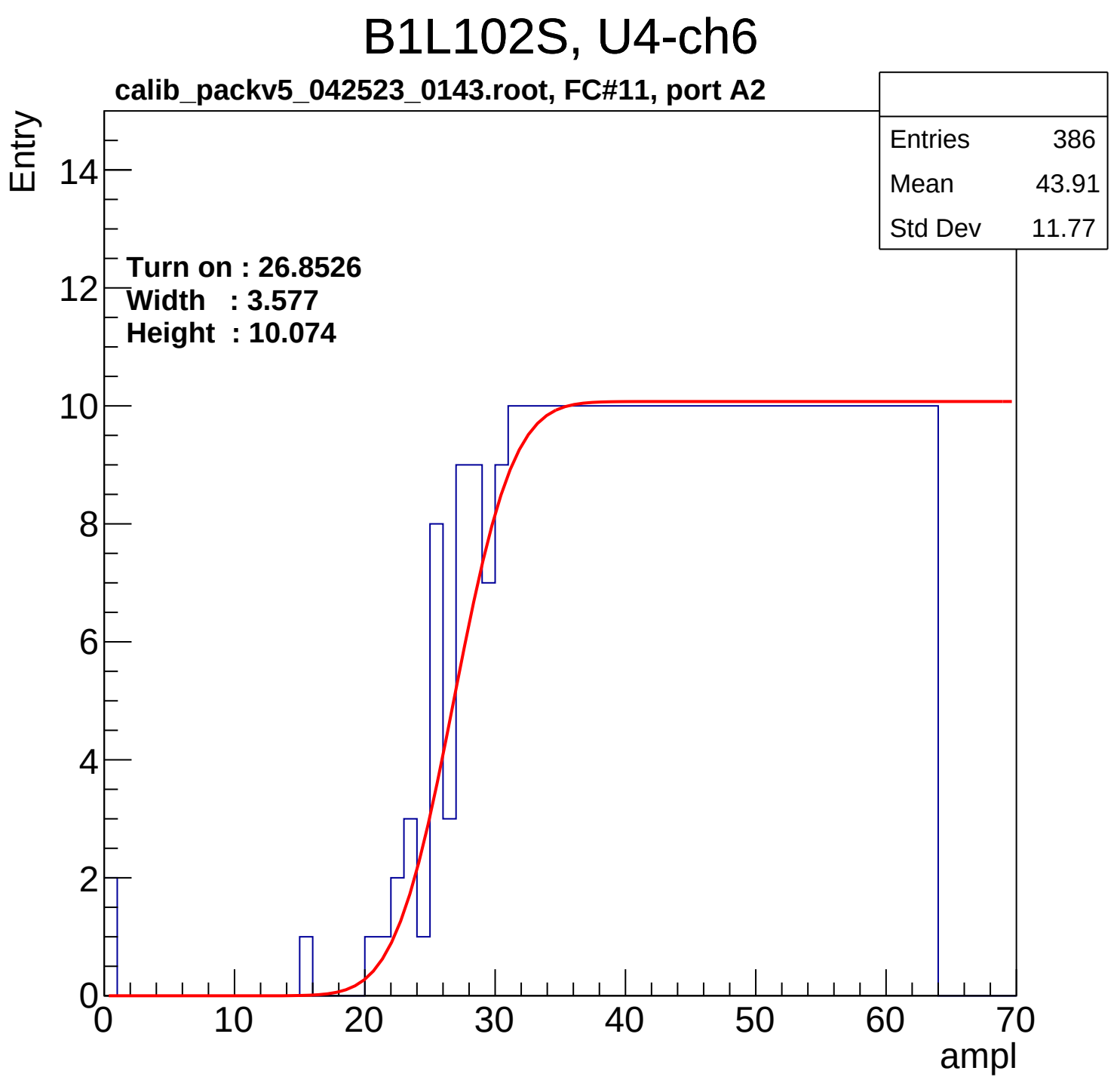
B1L102S, U4-ch6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 386
Mean 43.91
Std Dev 11.77
Turn on : 26.8526
Width : 3.577
Height : 10.074
Entry
ampl
0
2
4
6
8
10
12
14
0
10
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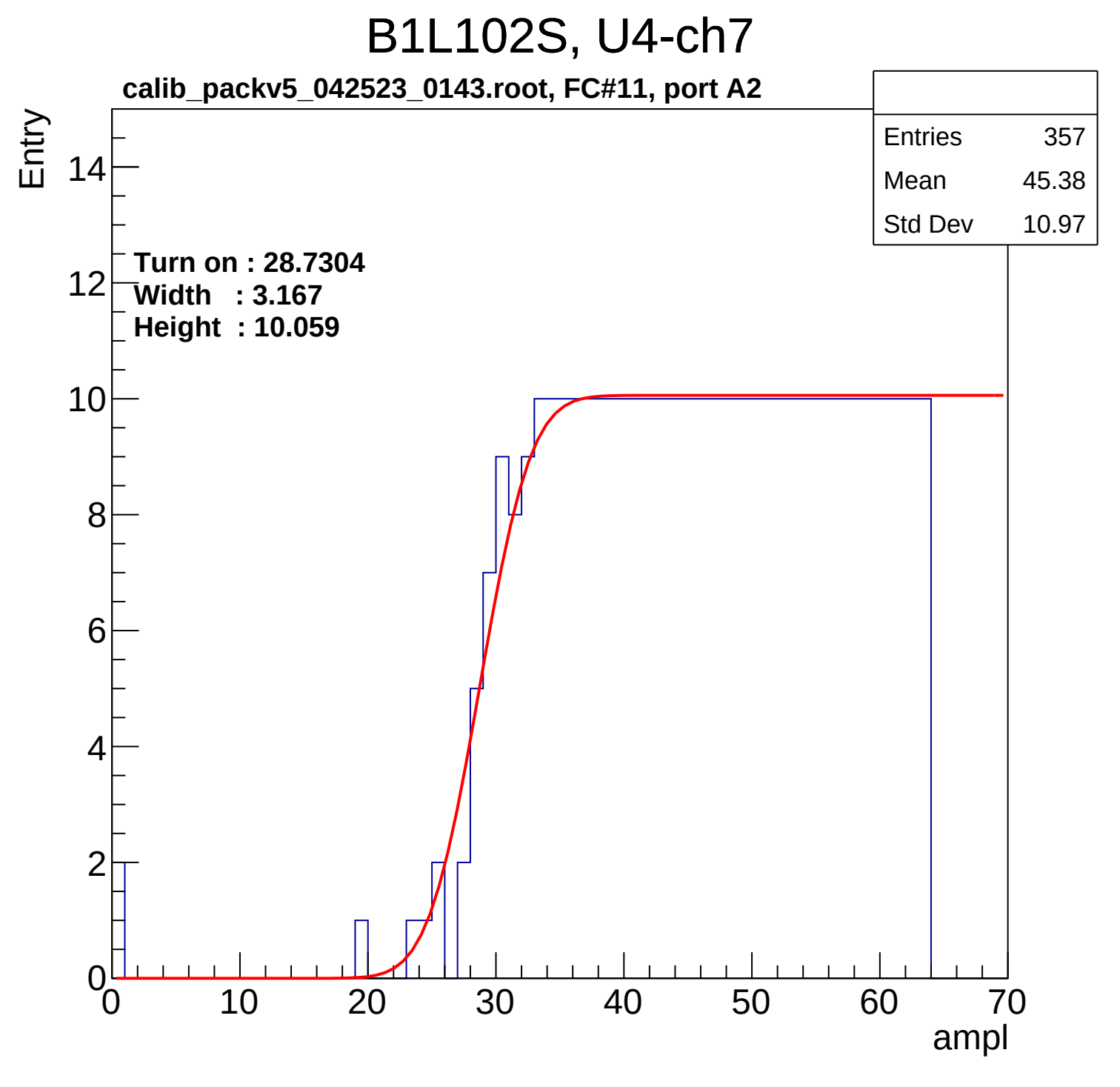
B1L102S, U4-ch7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 357
Mean 45.38
Std Dev 10.97
Turn on : 28.7304
Width : 3.167
Height : 10.059
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
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60
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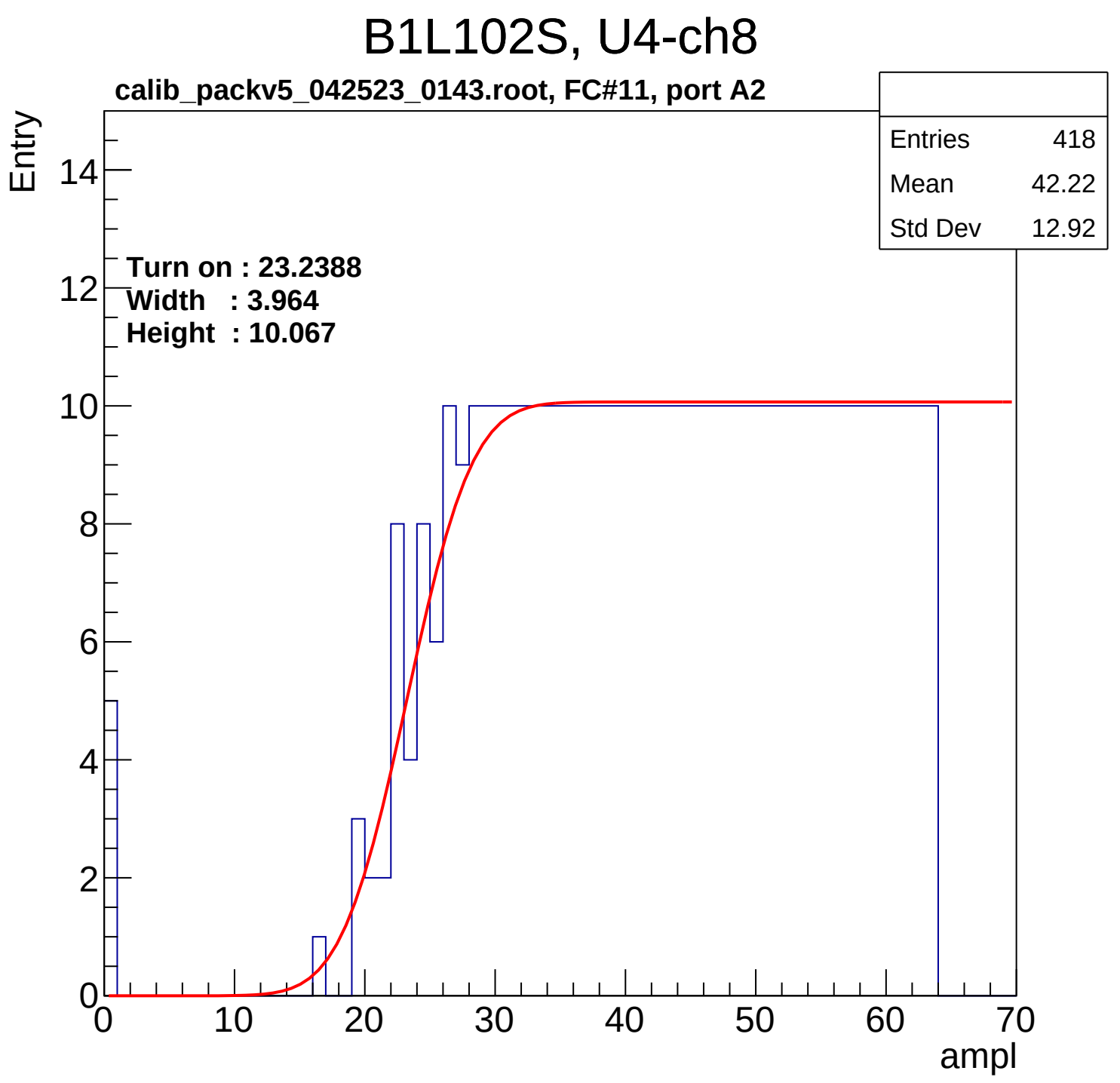
B1L102S, U4-ch8
calib_packv5_042523_0143.root, FC#11, port A2
Entries 418
Mean 42.22
Std Dev 12.92
Turn on : 23.2388
Width : 3.964
Height : 10.067
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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60
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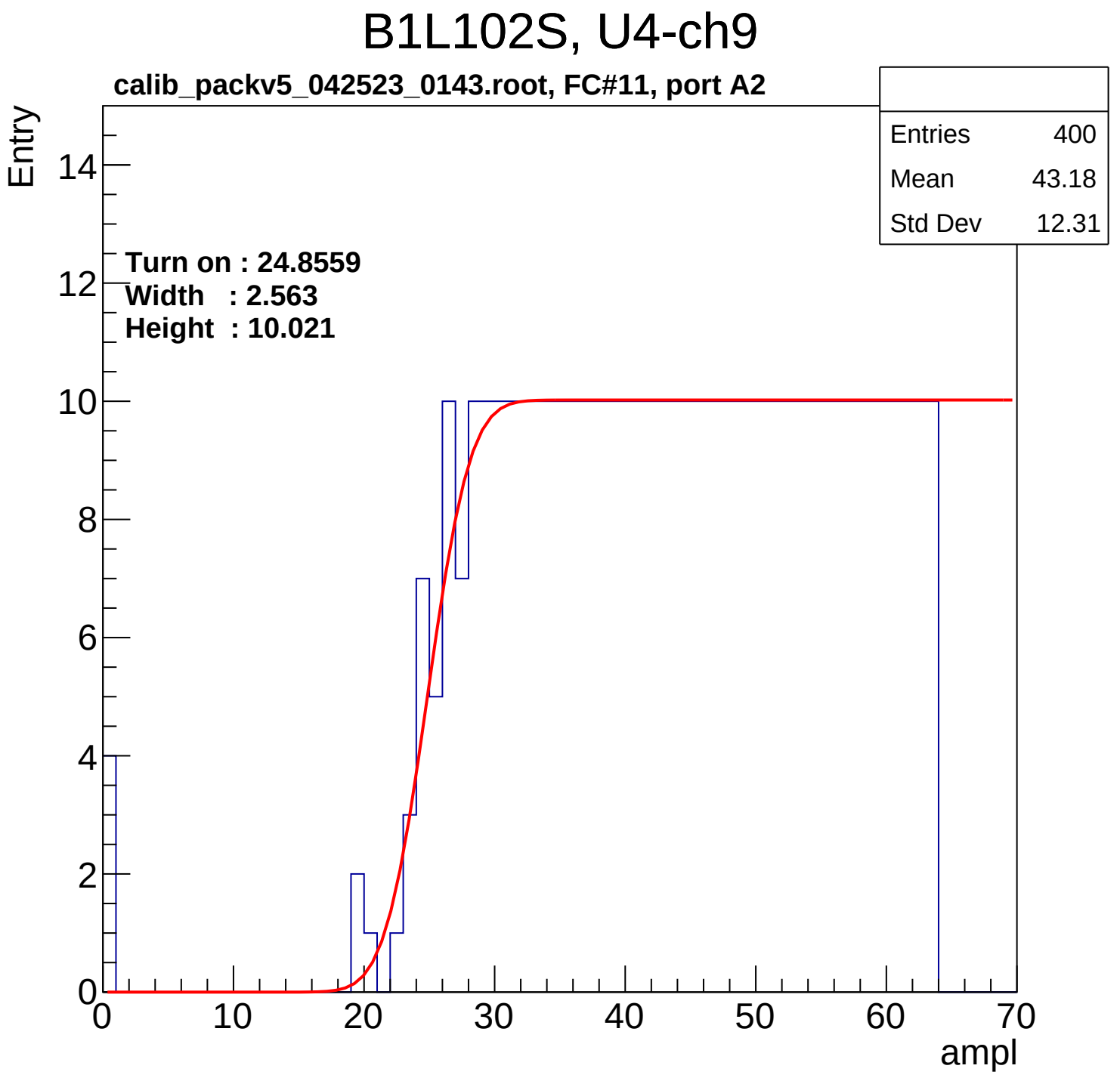
B1L102S, U4-ch9
calib_packv5_042523_0143.root, FC#11, port A2
Entries 400
Mean 43.18
Std Dev 12.31
Turn on : 24.8559
Width : 2.563
Height : 10.021
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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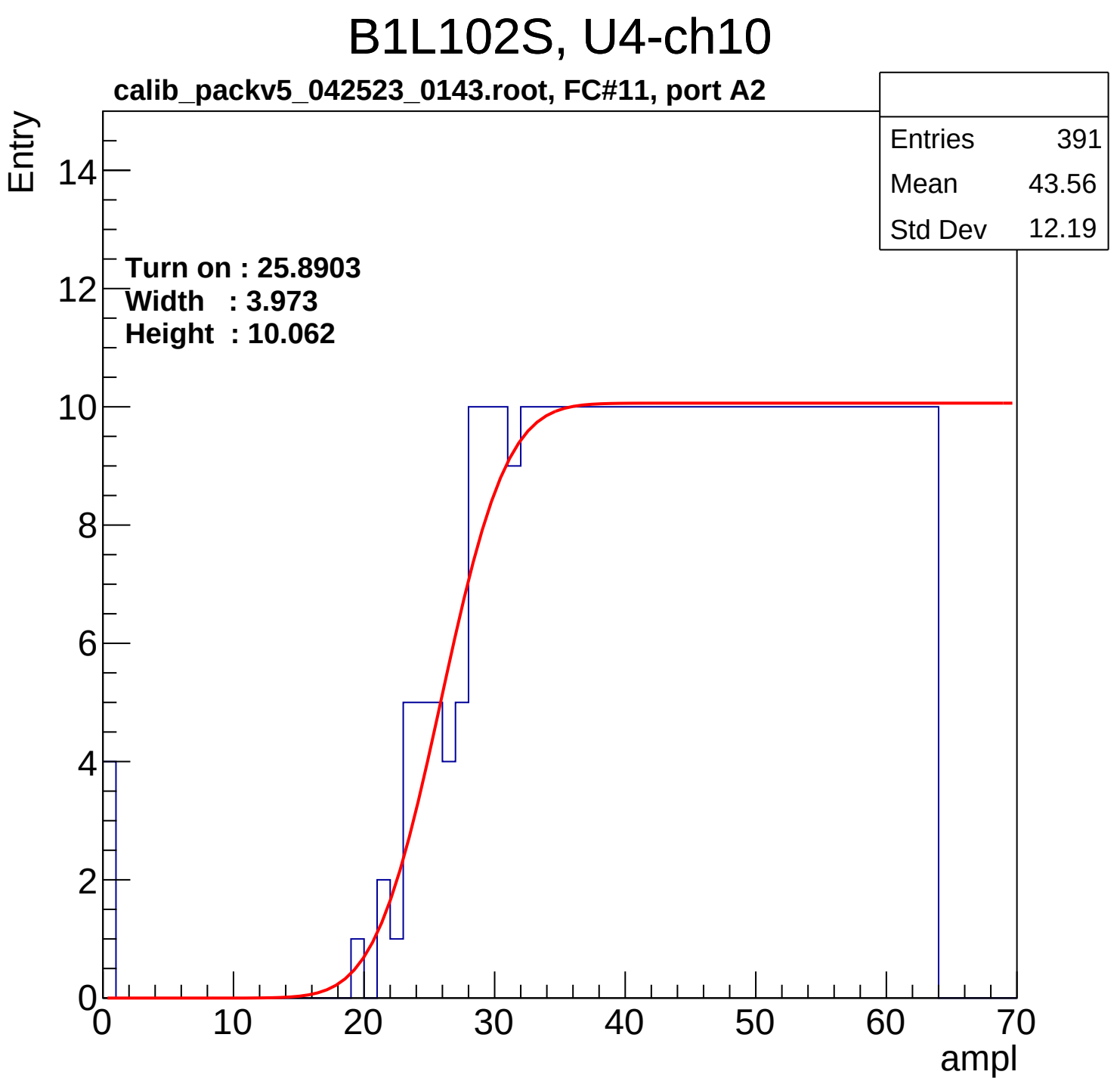
B1L102S, U4-ch10
calib_packv5_042523_0143.root, FC#11, port A2
Entries 391
Mean 43.56
Std Dev 12.19
Turn on : 25.8903
Width : 3.973
Height : 10.062
Entry
ampl
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4
6
8
10
12
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0
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20
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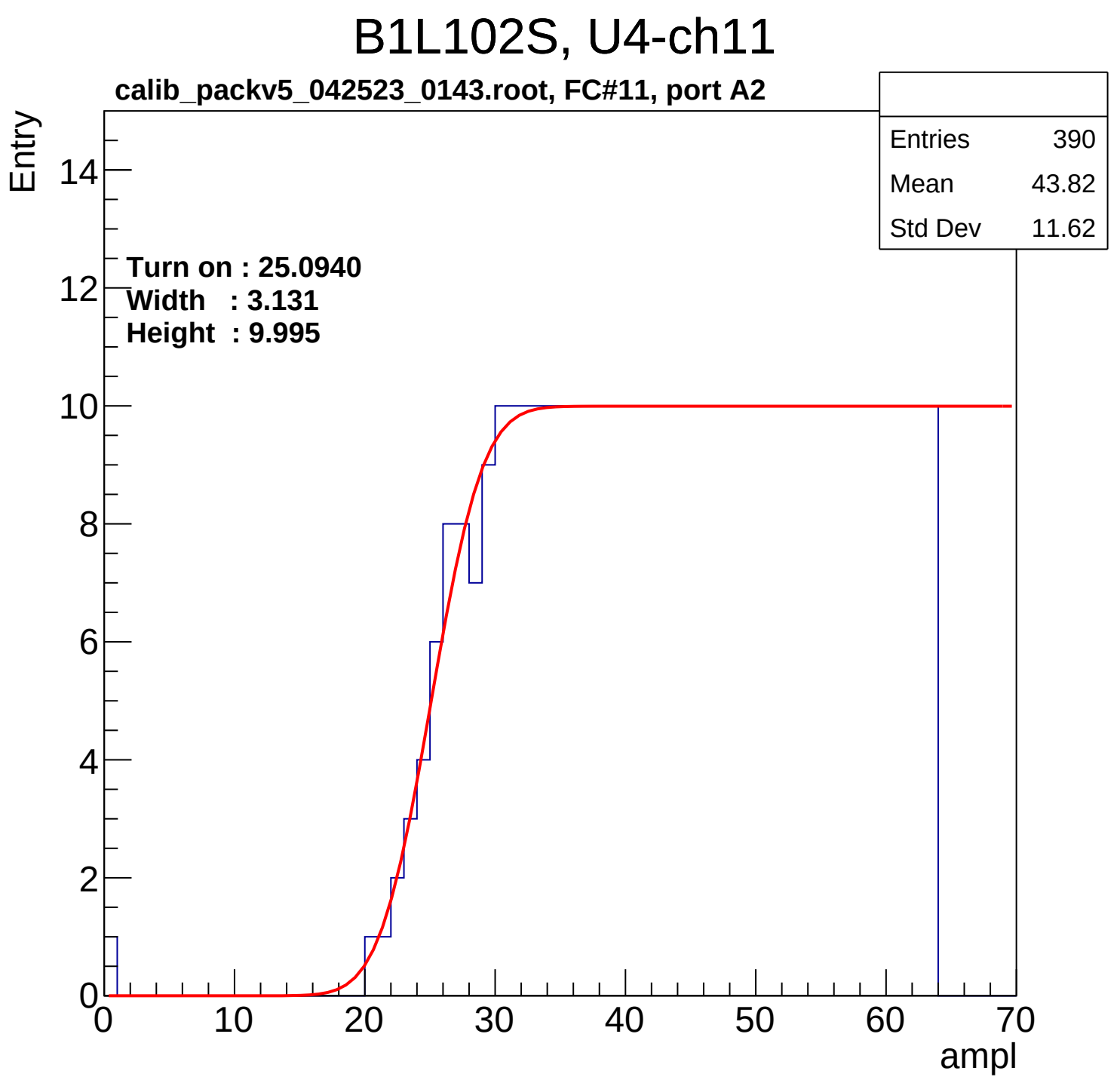
B1L102S, U4-ch11
calib_packv5_042523_0143.root, FC#11, port A2
Entries 390
Mean 43.82
Std Dev 11.62
Turn on : 25.0940
Width : 3.131
Height : 9.995
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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60
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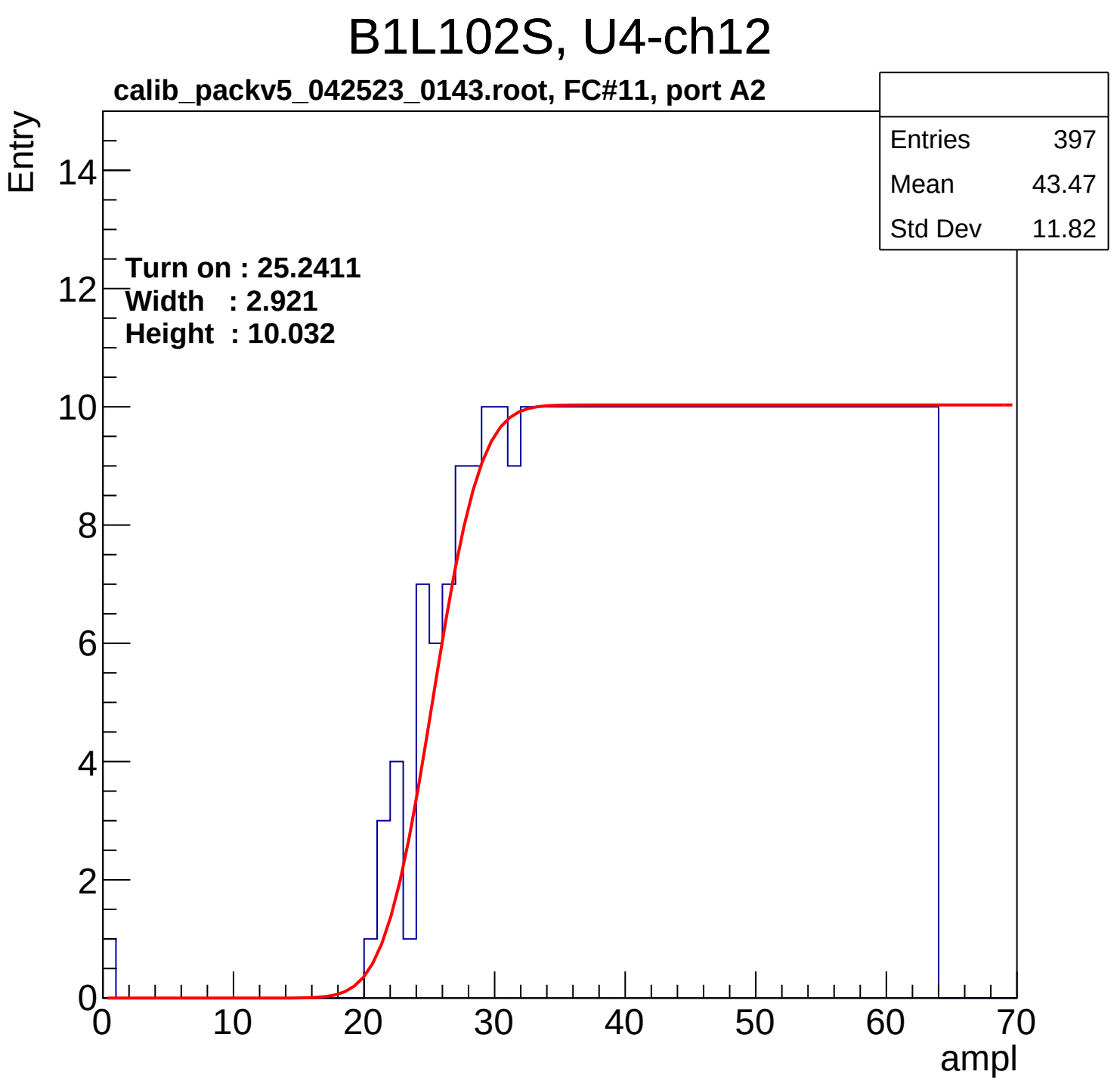
B1L102S, U4-ch12
calib_packv5_042523_0143.root, FC#11, port A2
Entries 397
Mean 43.47
Std Dev 11.82
Turn on : 25.2411
Width : 2.921
Height : 10.032
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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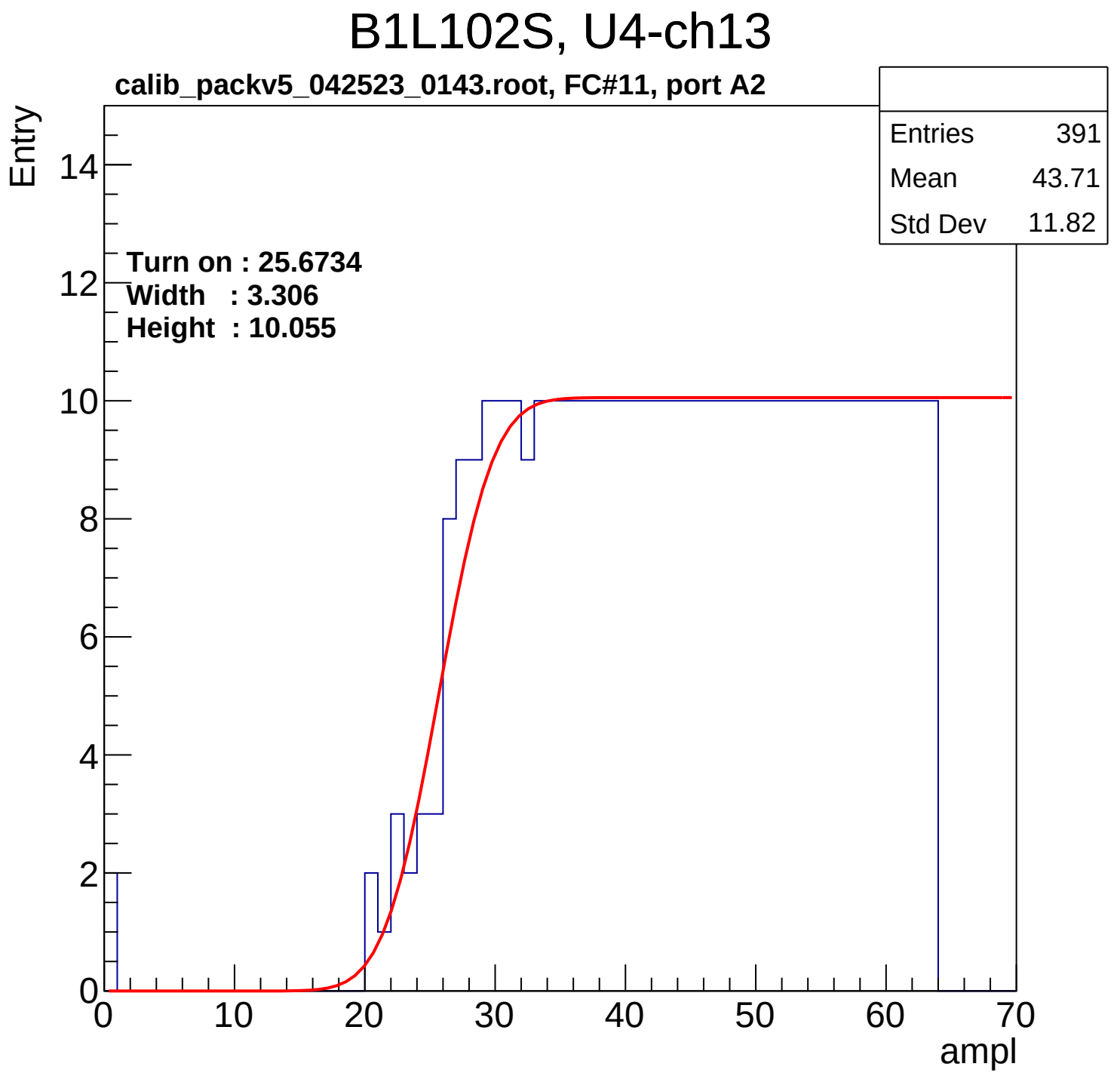
B1L102S, U4-ch13
calib_packv5_042523_0143.root, FC#11, port A2
Entries 391
Mean 43.71
Std Dev 11.82
Turn on : 25.6734
Width : 3.306
Height : 10.055
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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60
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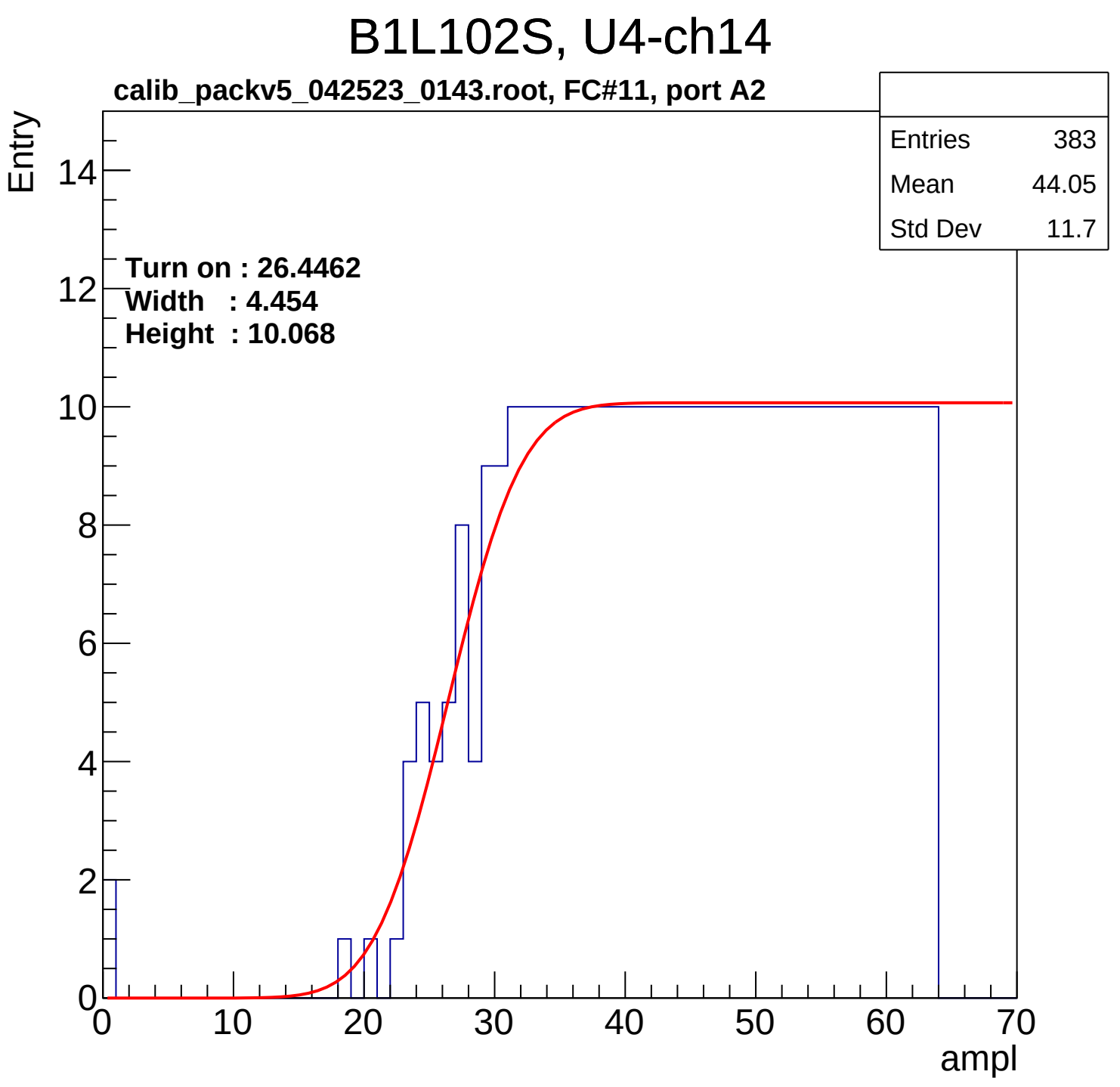
B1L102S, U4-ch14
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 44.05
Std Dev 11.7
Turn on : 26.4462
Width : 4.454
Height : 10.068
Entry
ampl
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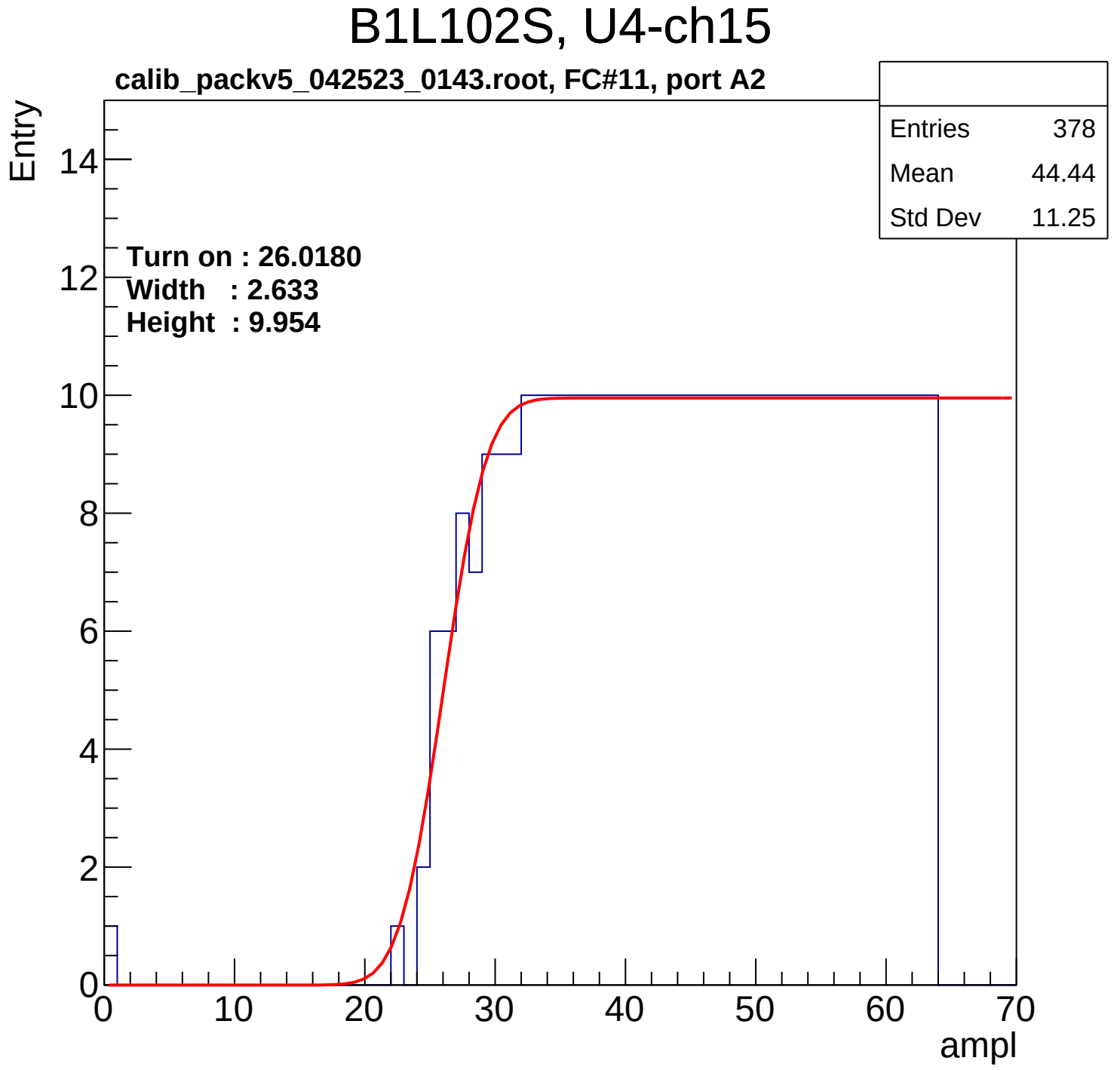
B1L102S, U4-ch15
calib_packv5_042523_0143.root, FC#11, port A2
Entries 378
Mean 44.44
Std Dev 11.25
Turn on : 26.0180
Width : 2.633
Height : 9.954
Entry
ampl
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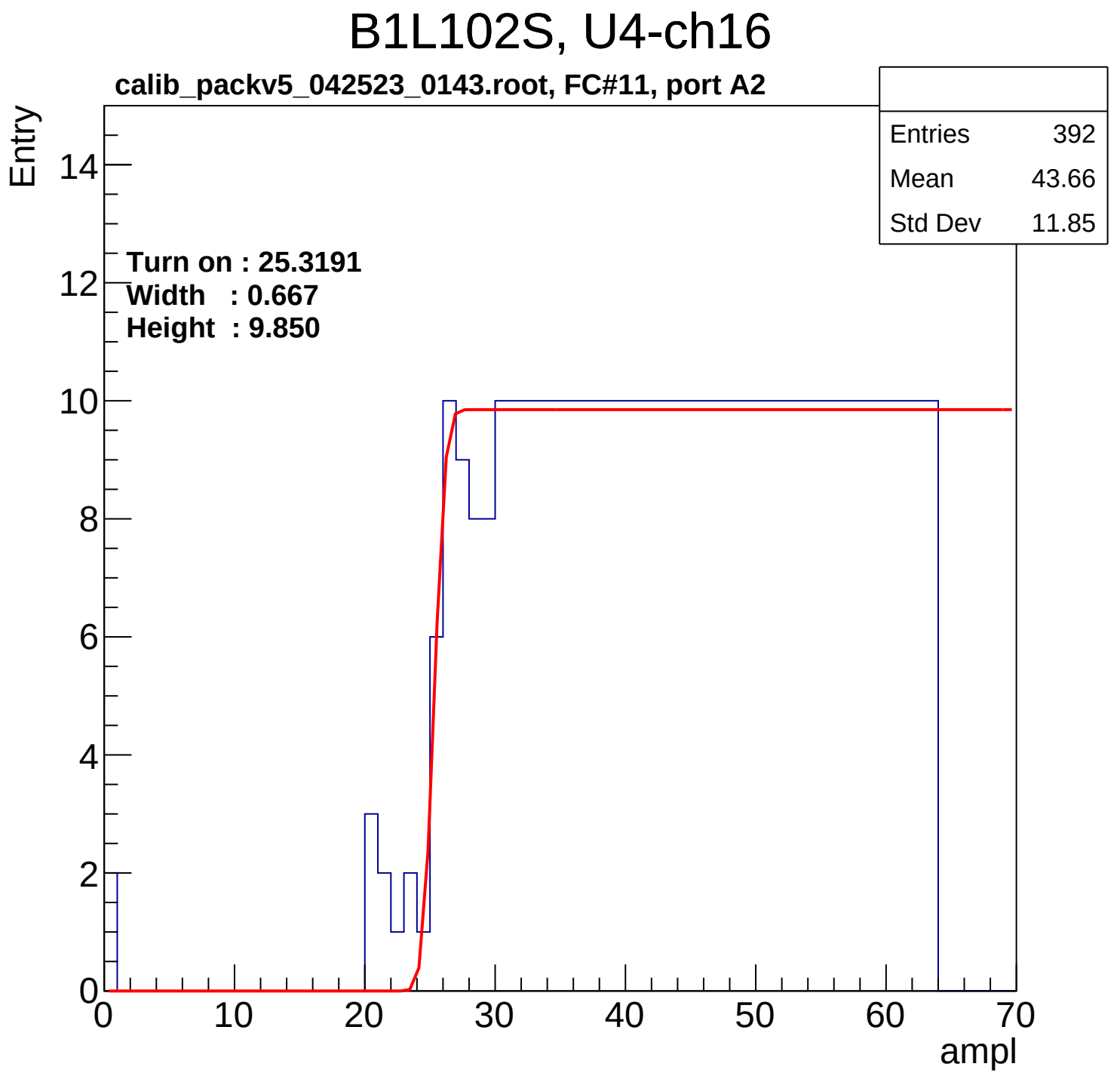
B1L102S, U4-ch16
calib_packv5_042523_0143.root, FC#11, port A2
Entries 392
Mean 43.66
Std Dev 11.85
Turn on : 25.3191
Width : 0.667
Height : 9.850
Entry
ampl
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2
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6
8
10
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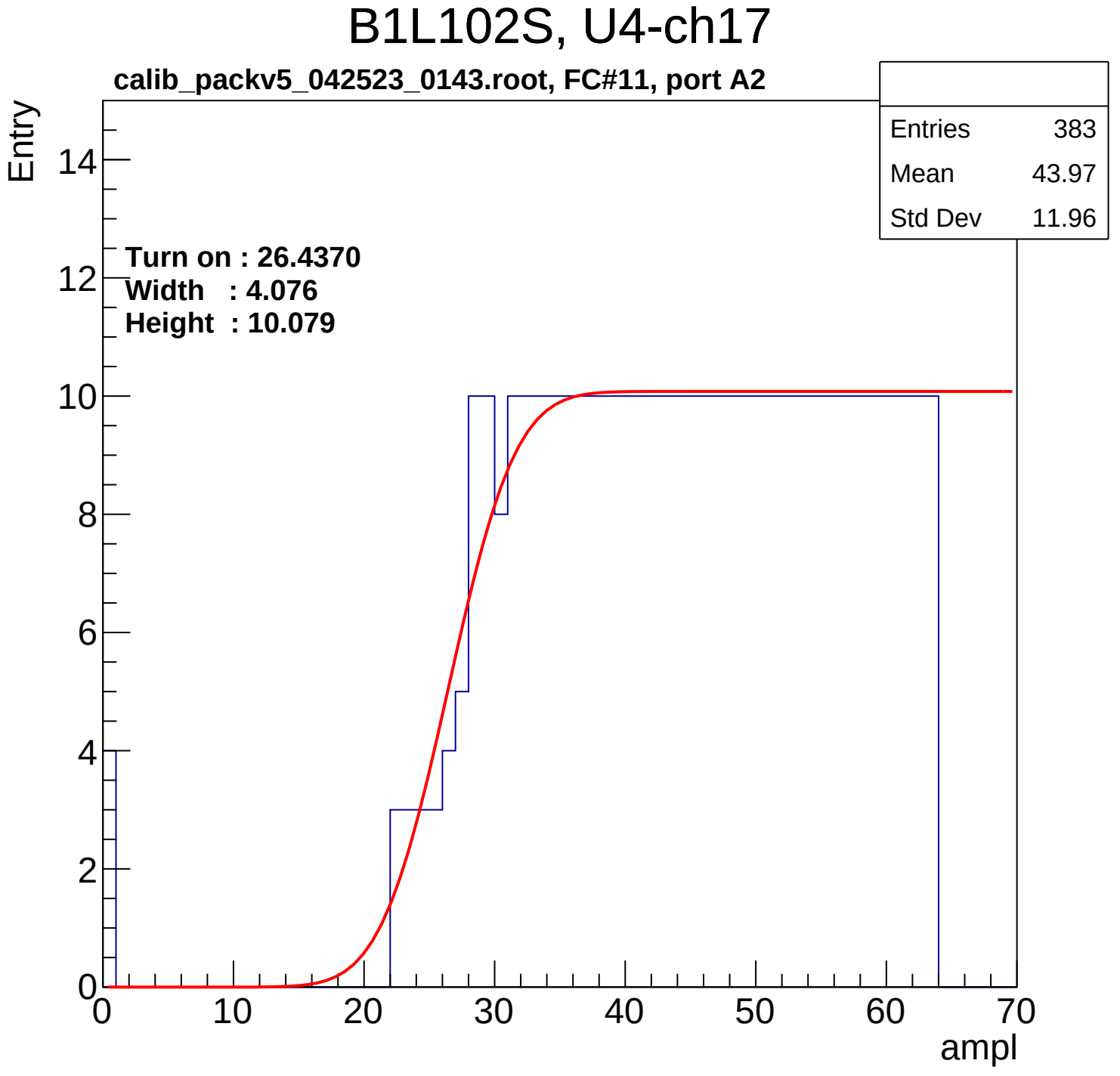
B1L102S, U4-ch17
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 43.97
Std Dev 11.96
Turn on : 26.4370
Width : 4.076
Height : 10.079
Entry
ampl
0
2
4
6
8
10
12
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0
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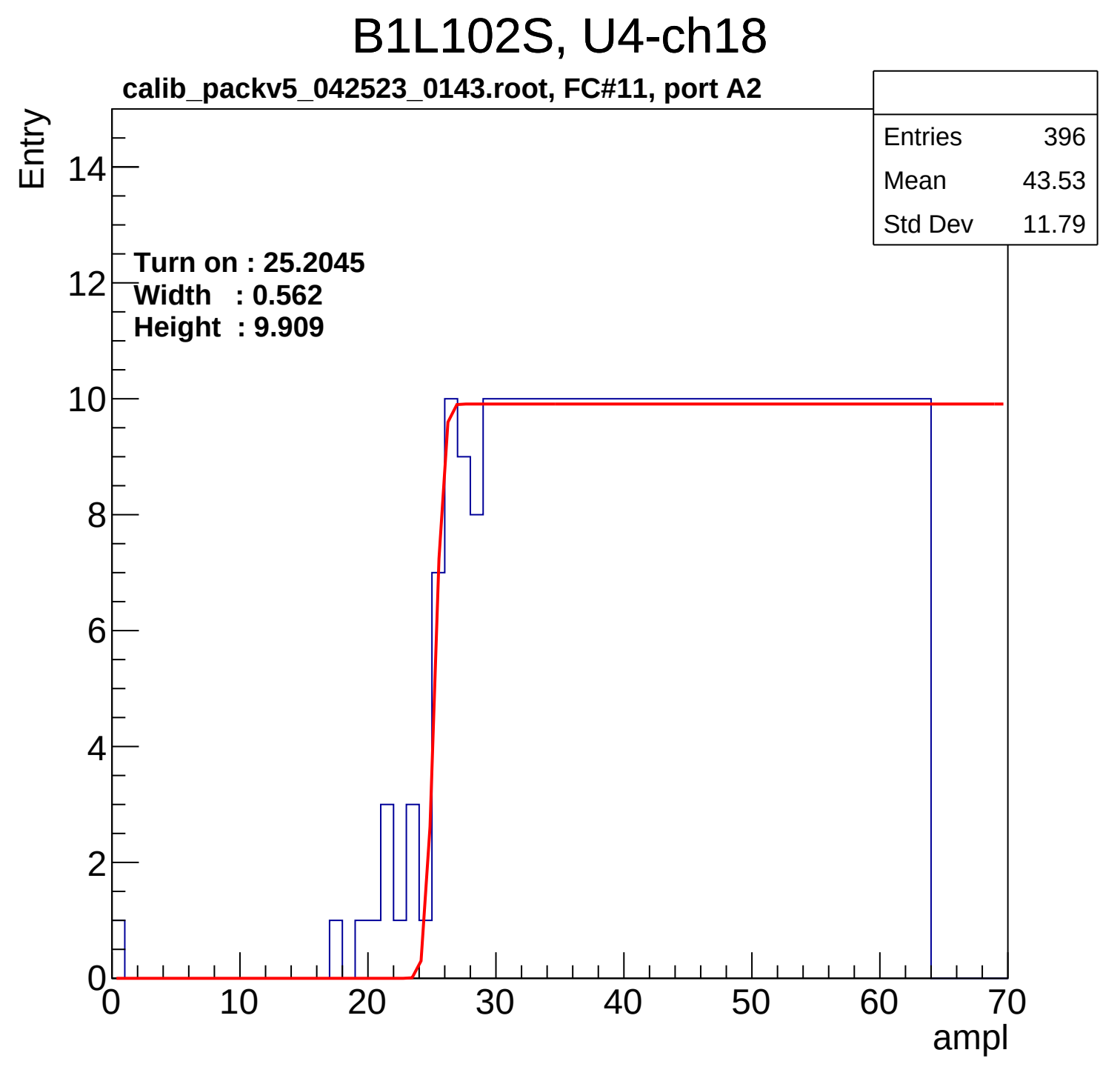
B1L102S, U4-ch18
calib_packv5_042523_0143.root, FC#11, port A2
Entries 396
Mean 43.53
Std Dev 11.79
Turn on : 25.2045
Width : 0.562
Height : 9.909
Entry
ampl
0
2
4
6
8
10
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0
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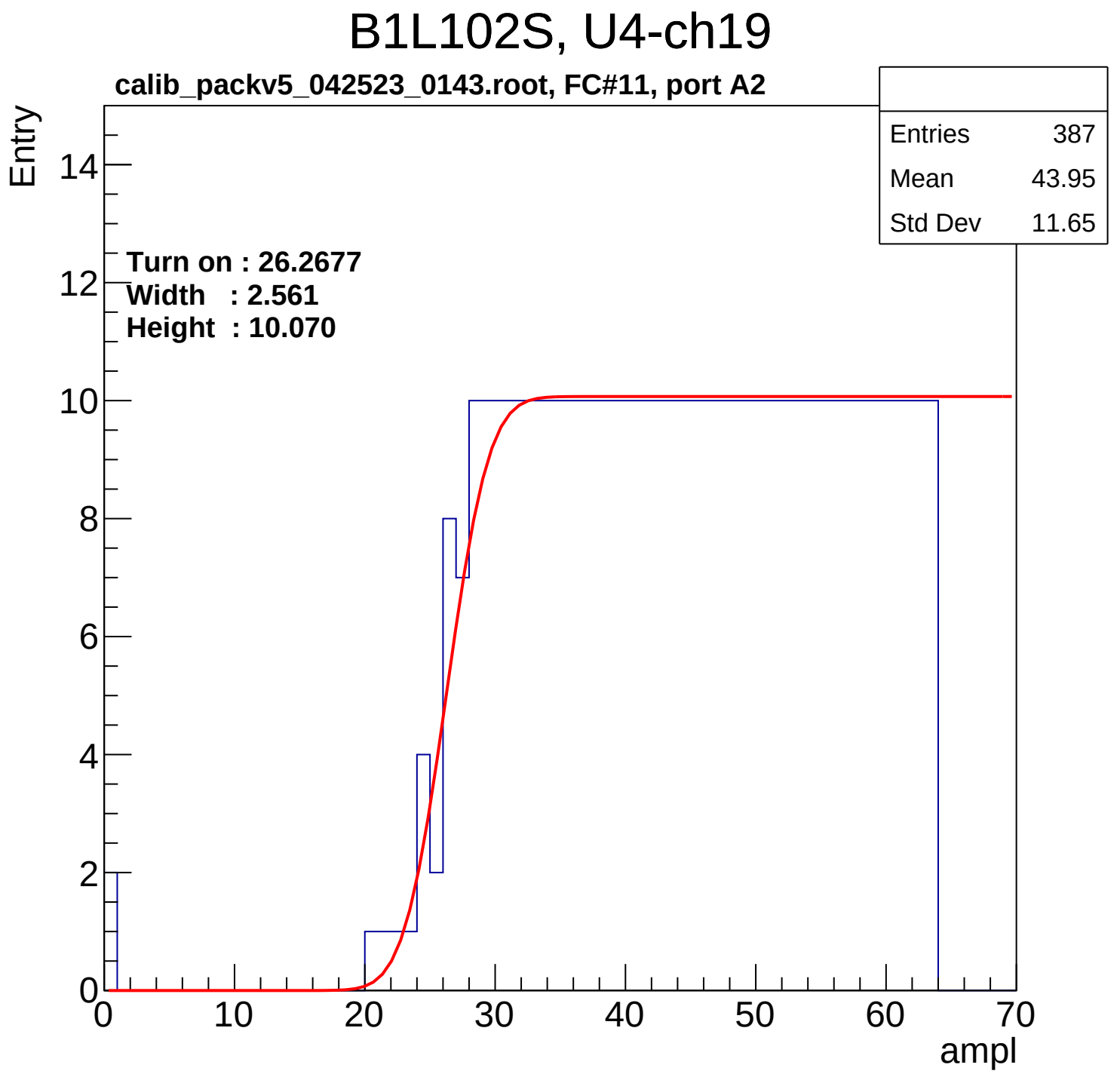
B1L102S, U4-ch19
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 43.95
Std Dev 11.65
Turn on : 26.2677
Width : 2.561
Height : 10.070
Entry
ampl
0
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6
8
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0
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60
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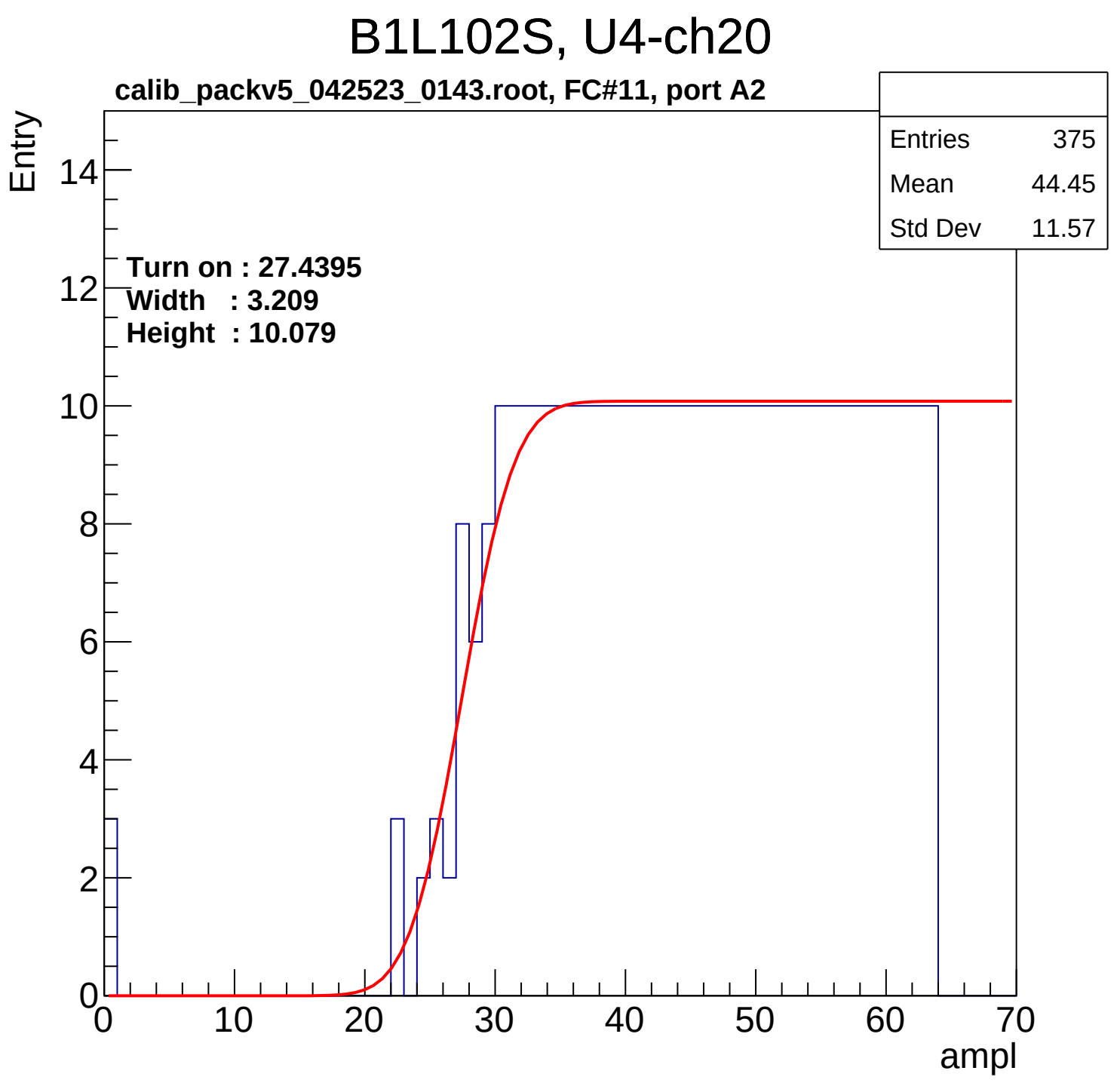
B1L102S, U4-ch20
calib_packv5_042523_0143.root, FC#11, port A2
Entries 375
Mean 44.45
Std Dev 11.57
Turn on : 27.4395
Width : 3.209
Height : 10.079
Entry
ampl
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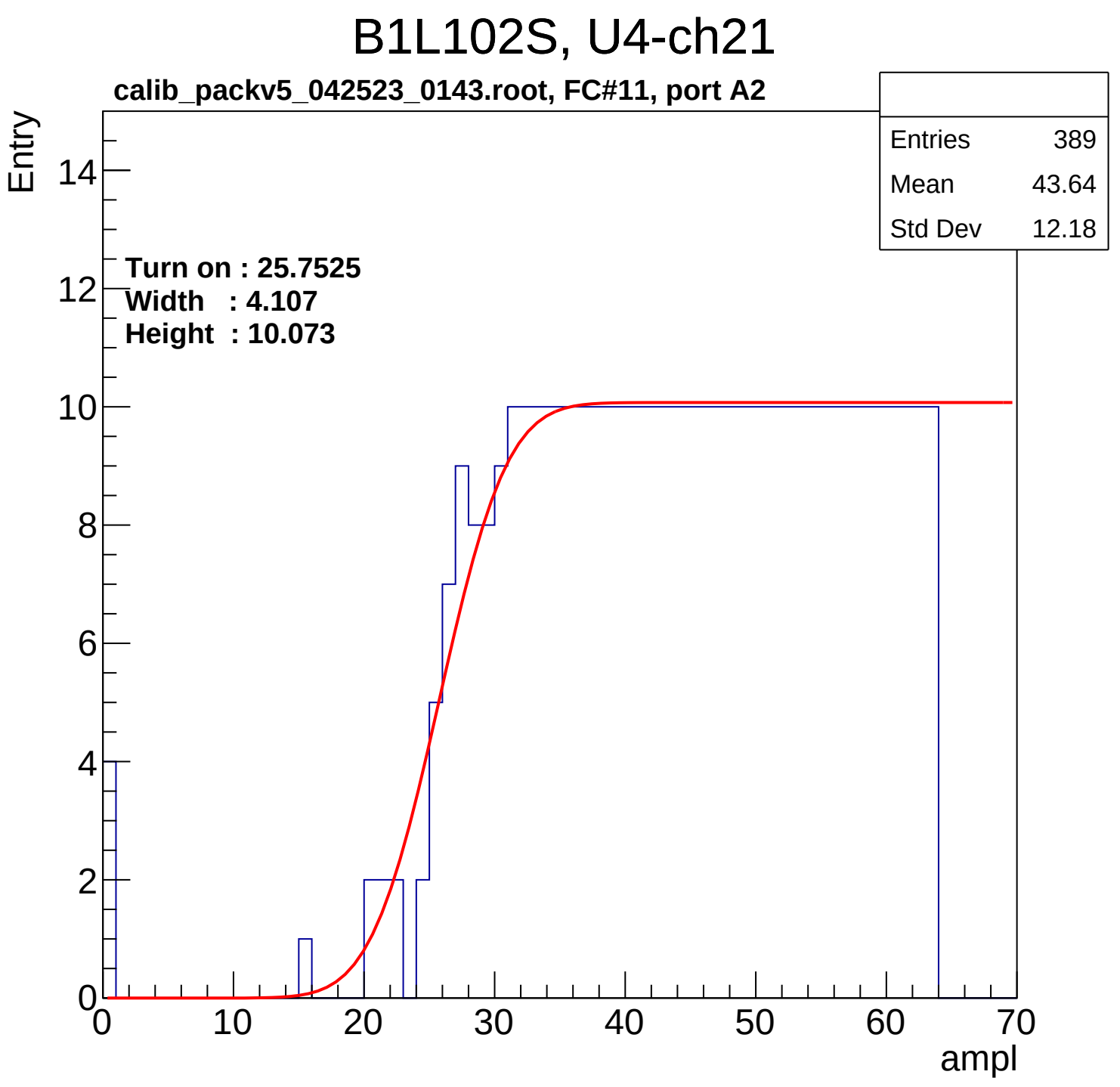
B1L102S, U4-ch21
calib_packv5_042523_0143.root, FC#11, port A2
Entries 389
Mean 43.64
Std Dev 12.18
Turn on : 25.7525
Width : 4.107
Height : 10.073
Entry
ampl
0
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0
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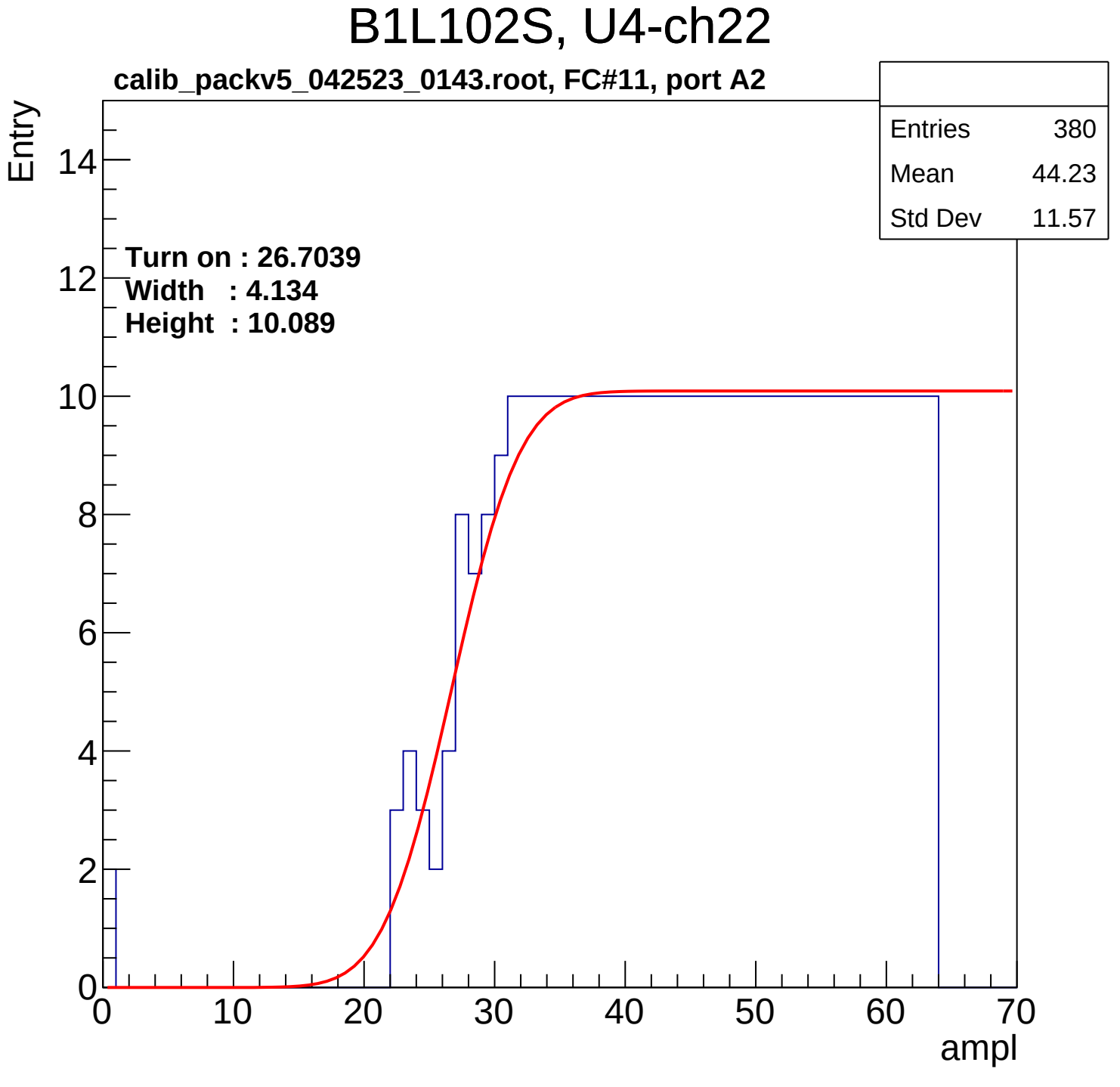
B1L102S, U4-ch22
calib_packv5_042523_0143.root, FC#11, port A2
Entries 380
Mean 44.23
Std Dev 11.57
Turn on : 26.7039
Width : 4.134
Height : 10.089
Entry
ampl
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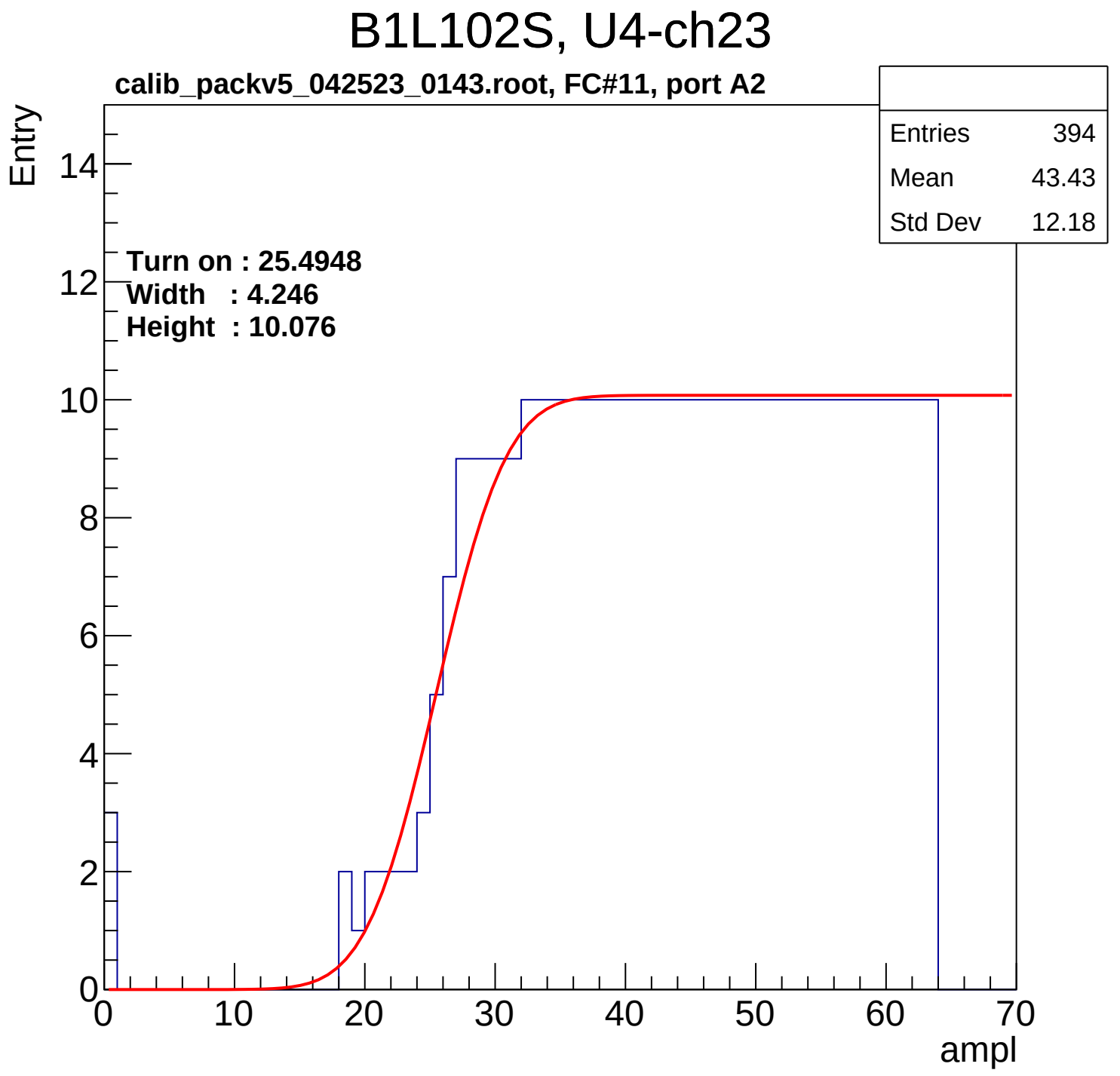
B1L102S, U4-ch23
calib_packv5_042523_0143.root, FC#11, port A2
Entries 394
Mean 43.43
Std Dev 12.18
Turn on : 25.4948
Width : 4.246
Height : 10.076
Entry
ampl
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2
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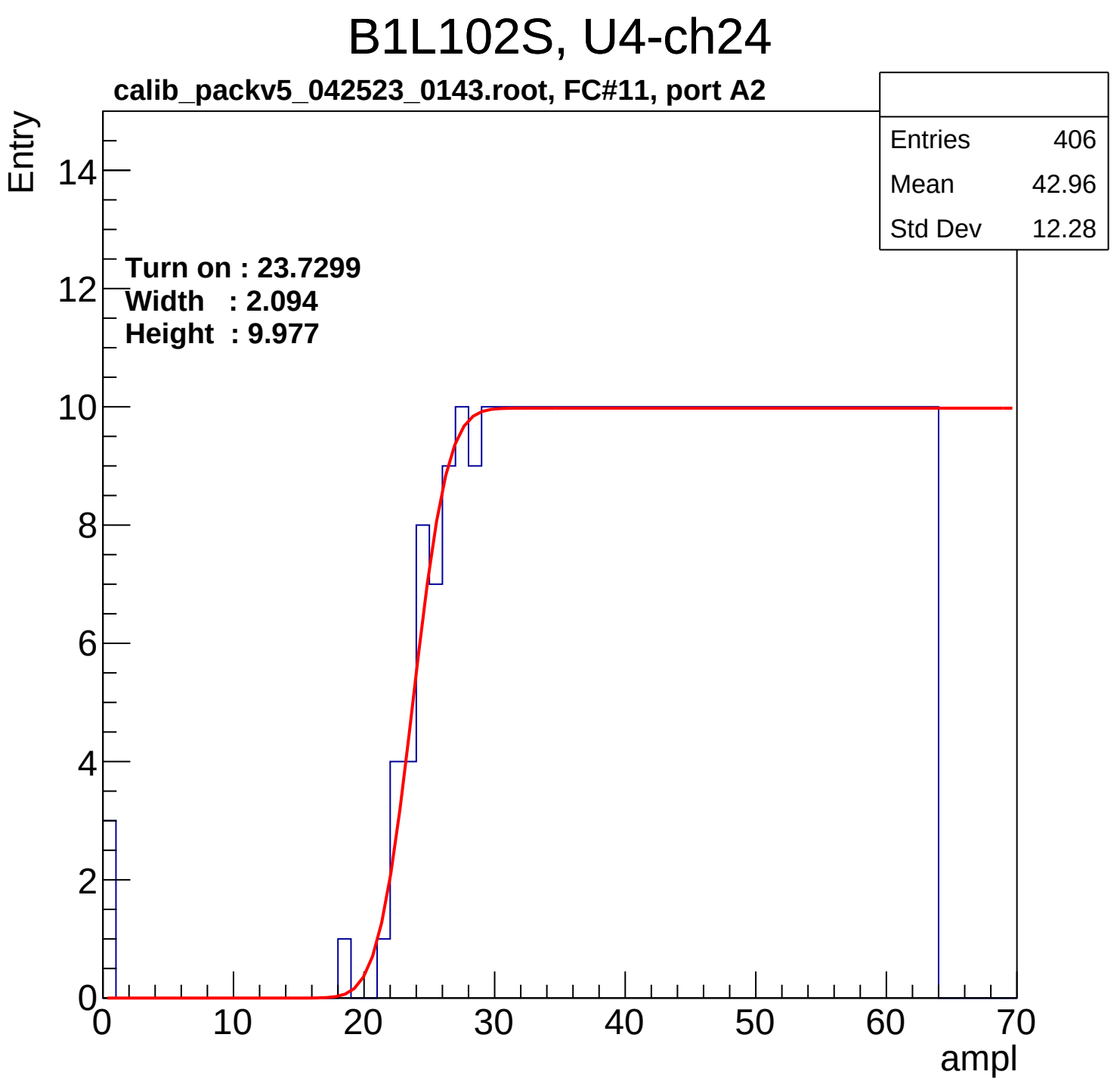
B1L102S, U4-ch24
calib_packv5_042523_0143.root, FC#11, port A2
Entries 406
Mean 42.96
Std Dev 12.28
Turn on : 23.7299
Width : 2.094
Height : 9.977
Entry
ampl
0
2
4
6
8
10
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20
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60
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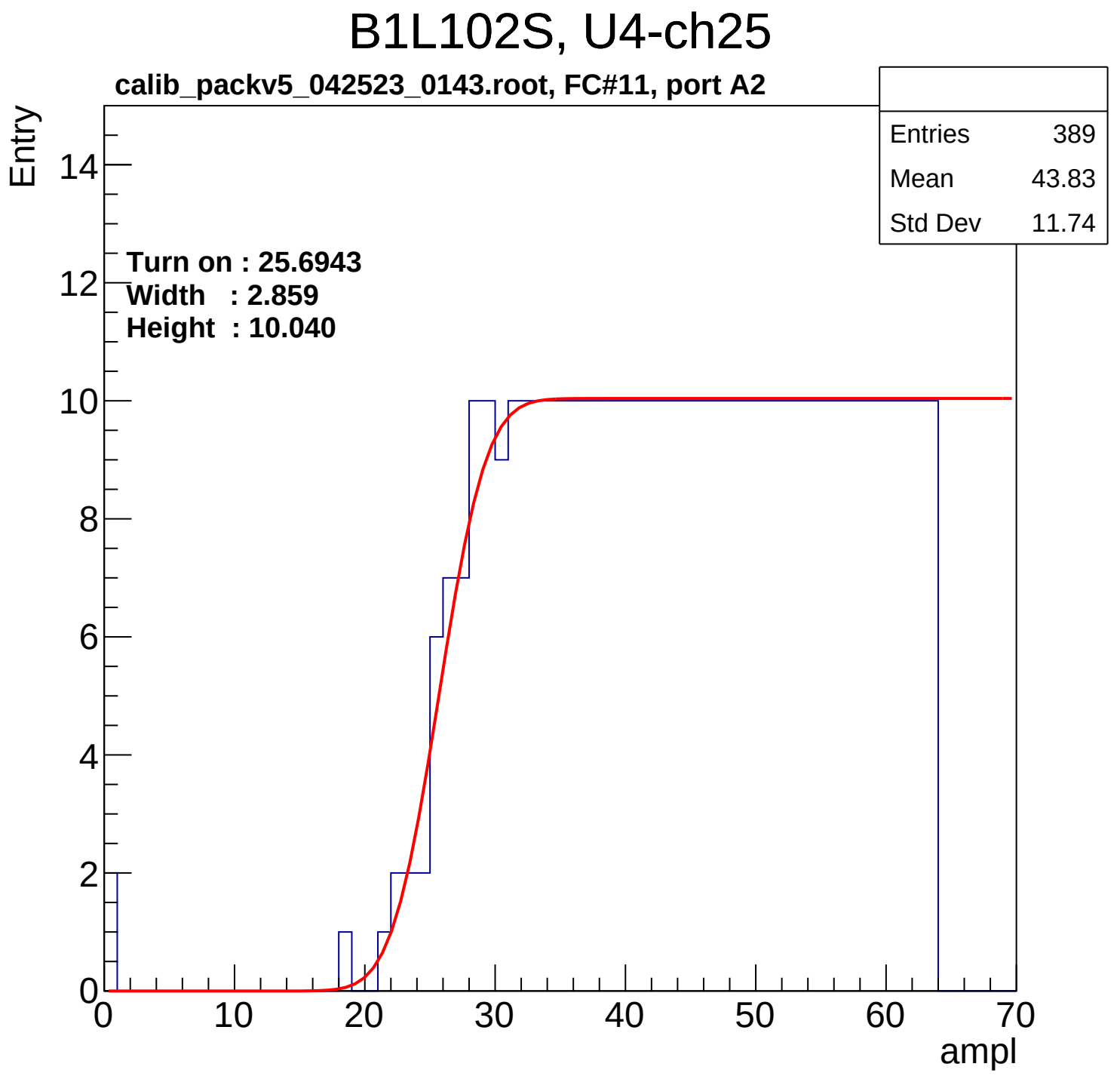
B1L102S, U4-ch25
calib_packv5_042523_0143.root, FC#11, port A2
Entries 389
Mean 43.83
Std Dev 11.74
Turn on : 25.6943
Width : 2.859
Height : 10.040
Entry
ampl
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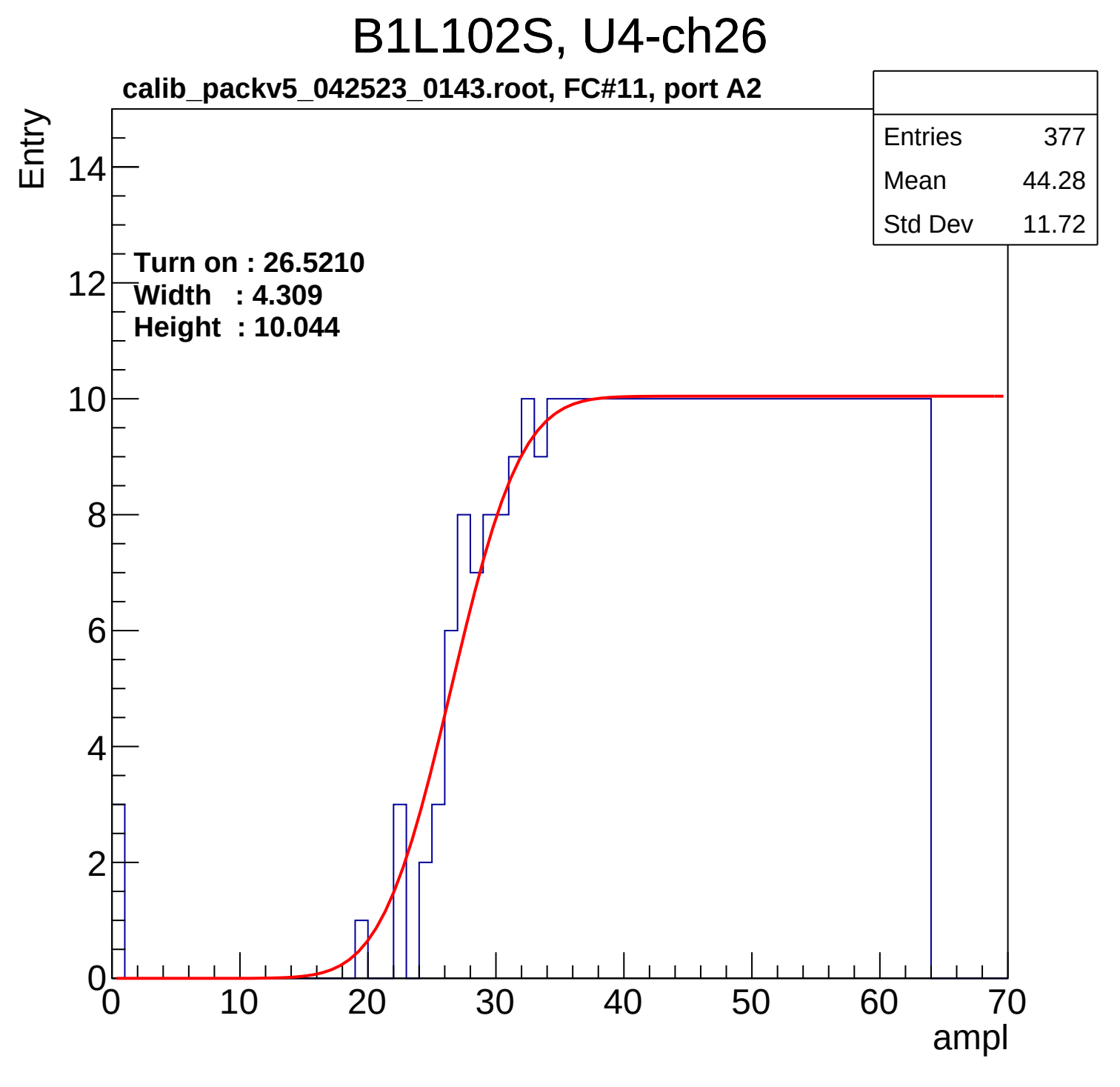
B1L102S, U4-ch26
calib_packv5_042523_0143.root, FC#11, port A2
Entries 377
Mean 44.28
Std Dev 11.72
Turn on : 26.5210
Width : 4.309
Height : 10.044
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ampl
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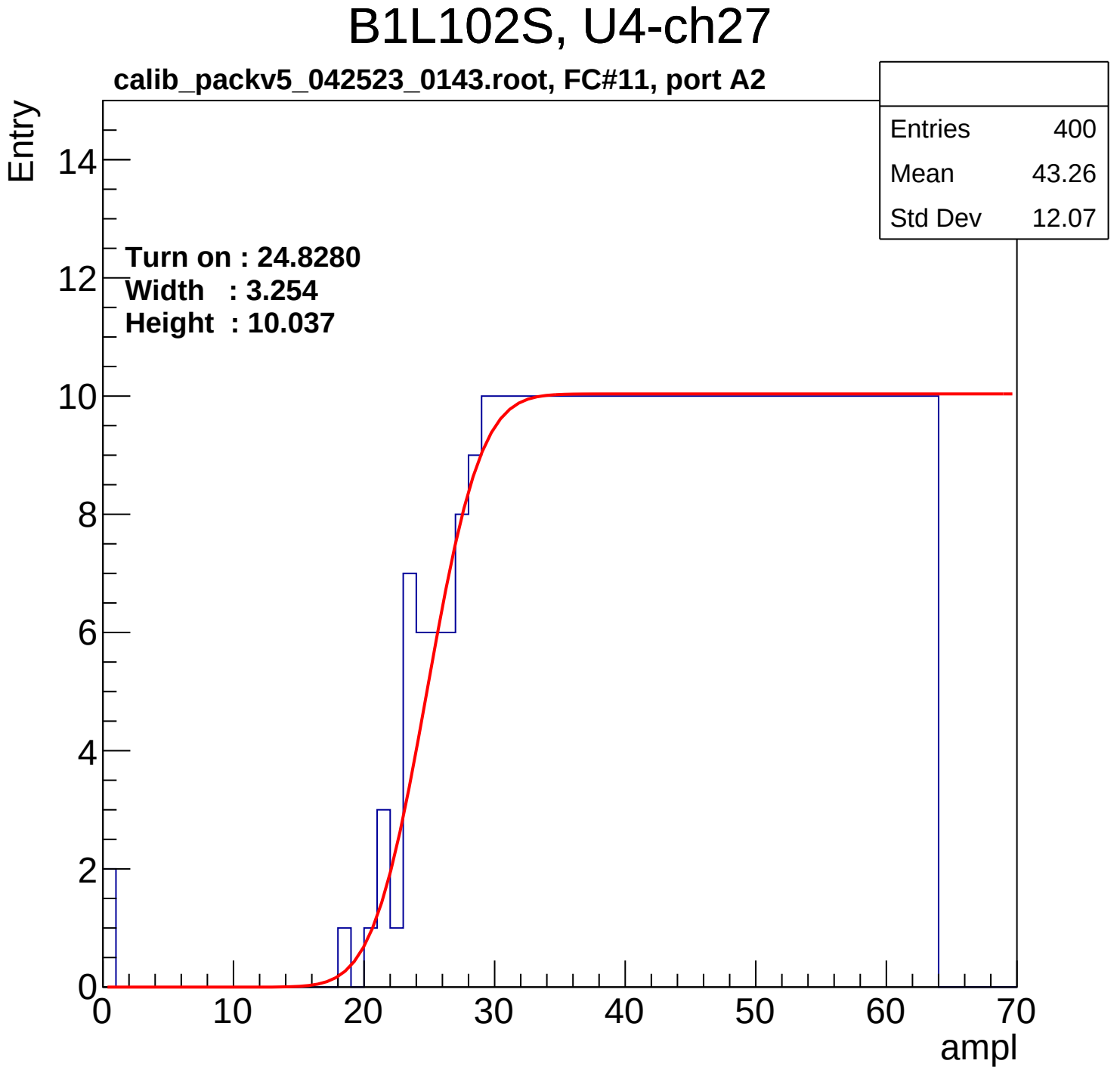
B1L102S, U4-ch27
calib_packv5_042523_0143.root, FC#11, port A2
Entries 400
Mean 43.26
Std Dev 12.07
Turn on : 24.8280
Width : 3.254
Height : 10.037
Entry
ampl
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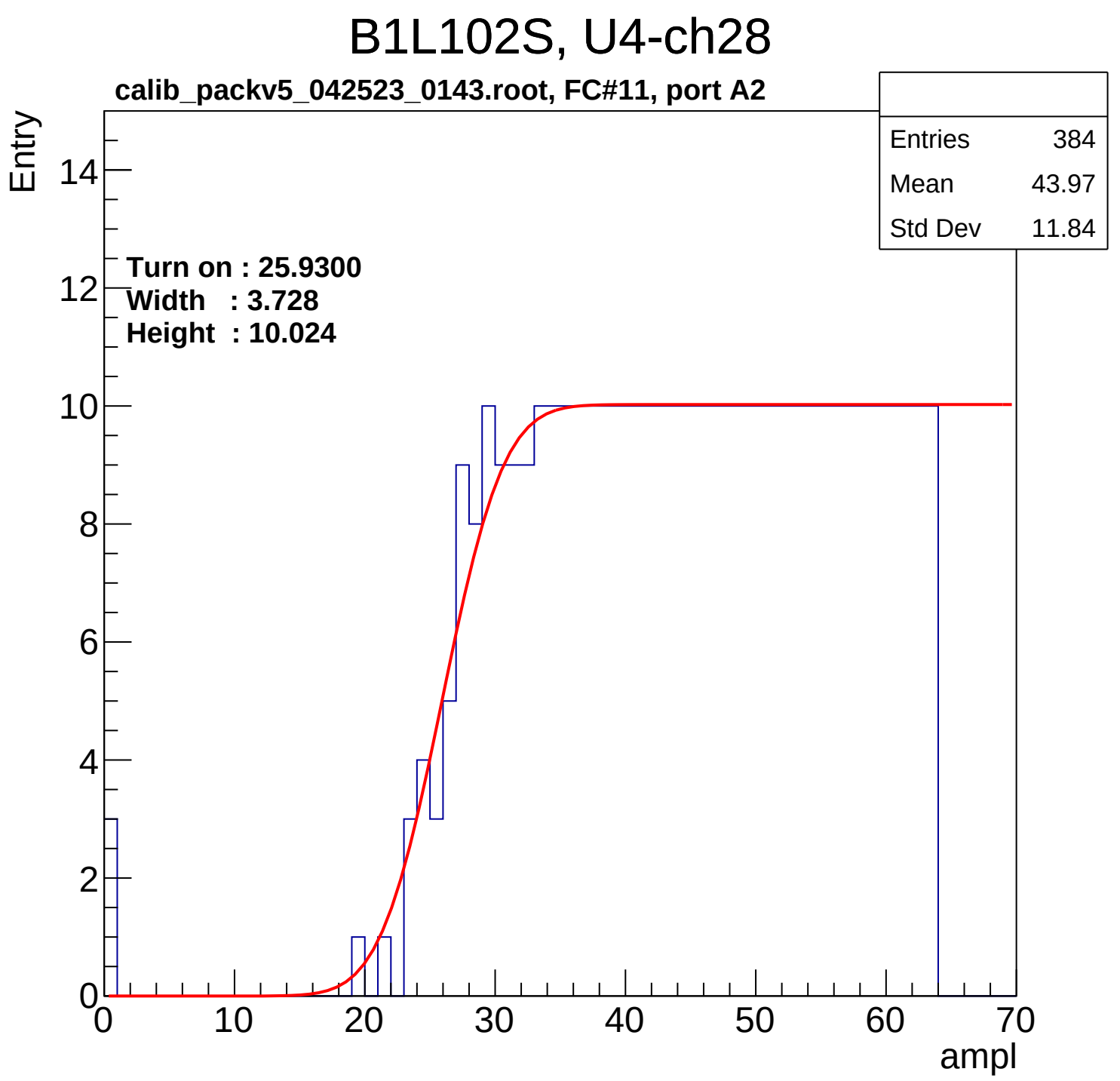
B1L102S, U4-ch28
calib_packv5_042523_0143.root, FC#11, port A2
Entries 384
Mean 43.97
Std Dev 11.84
Turn on : 25.9300
Width : 3.728
Height : 10.024
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
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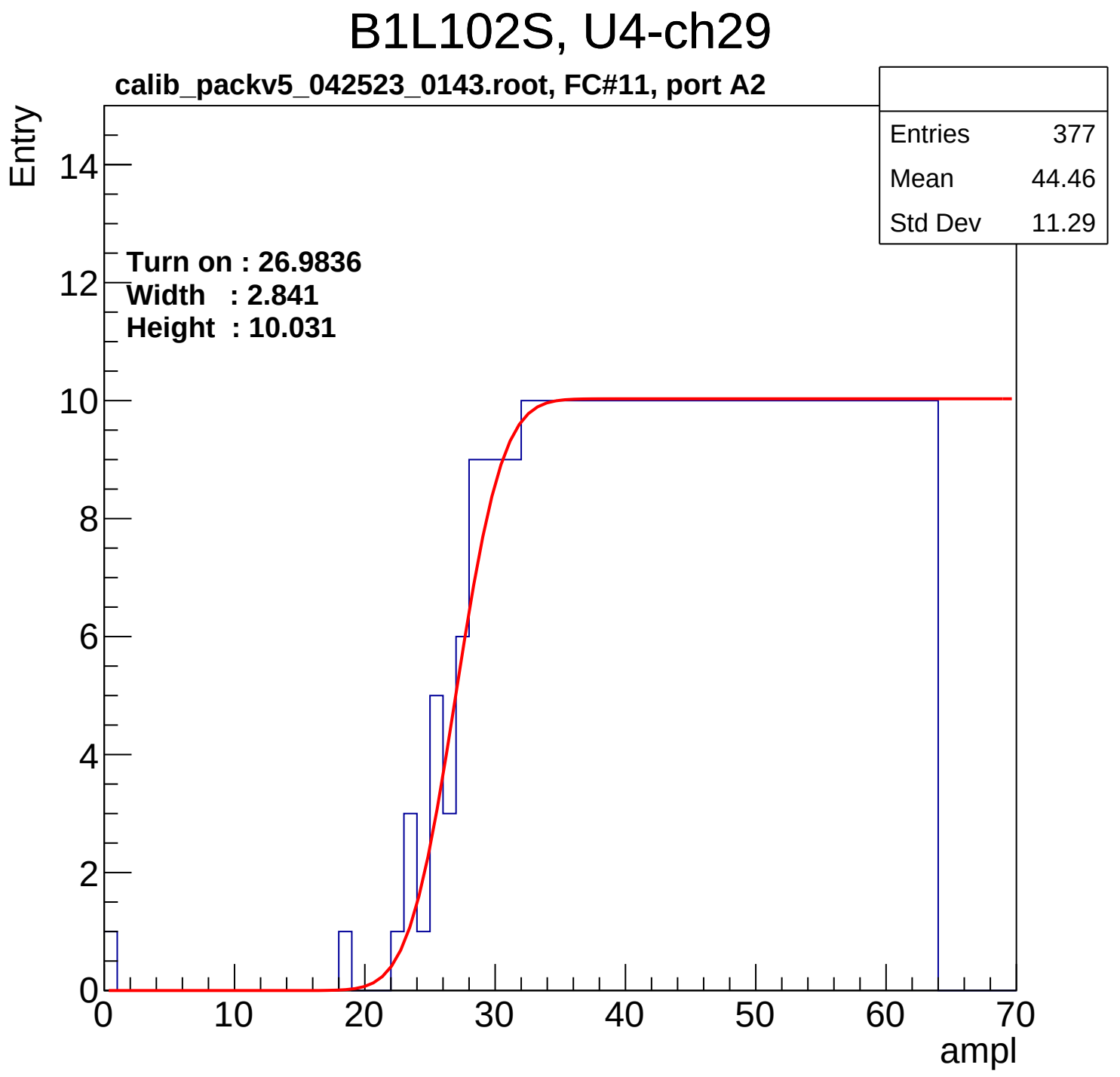
B1L102S, U4-ch29
calib_packv5_042523_0143.root, FC#11, port A2
Entries 377
Mean 44.46
Std Dev 11.29
Turn on : 26.9836
Width : 2.841
Height : 10.031
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ampl
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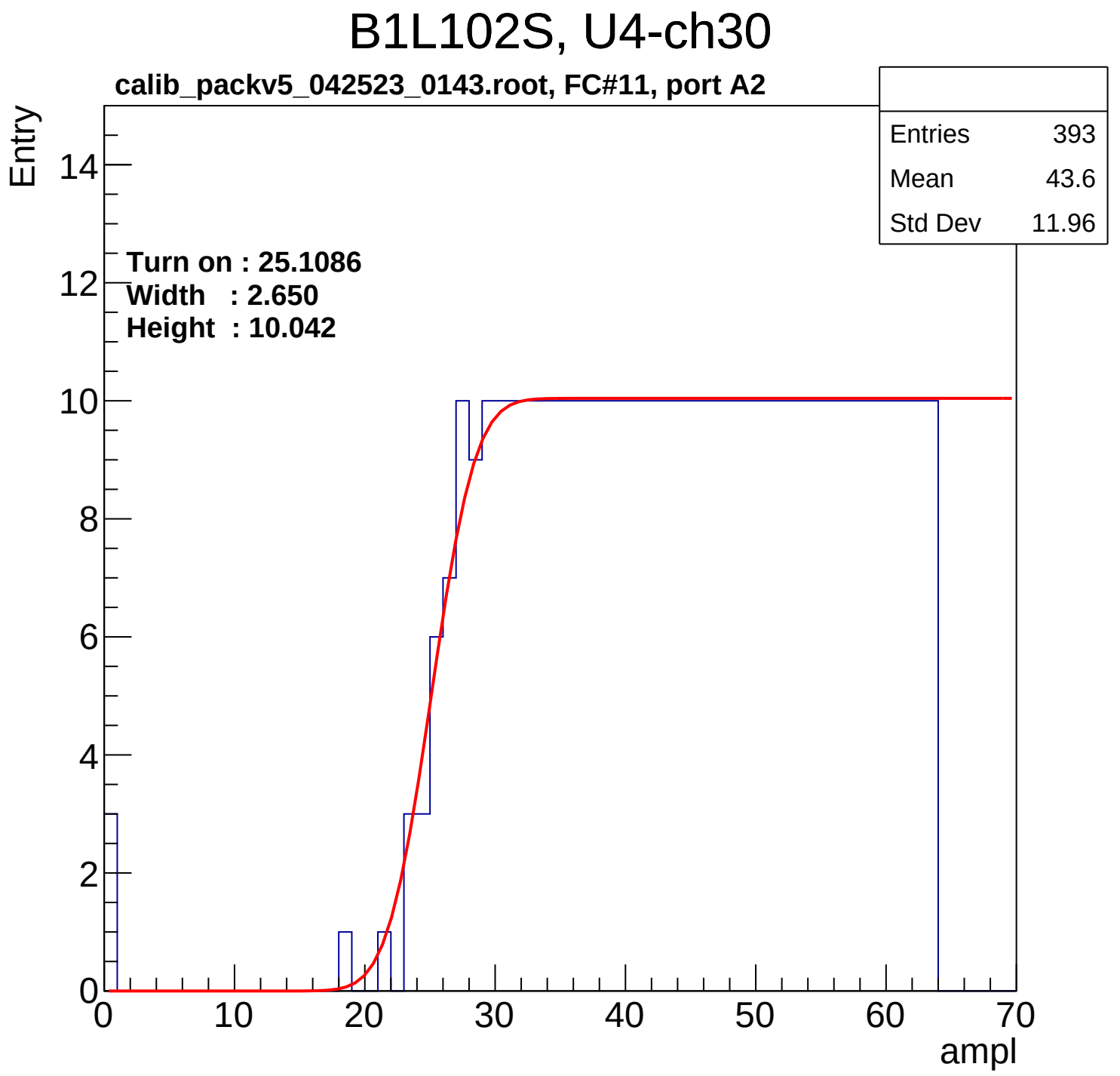
B1L102S, U4-ch30
calib_packv5_042523_0143.root, FC#11, port A2
Entries 393
Mean 43.6
Std Dev 11.96
Turn on : 25.1086
Width : 2.650
Height : 10.042
Entry
ampl
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2
4
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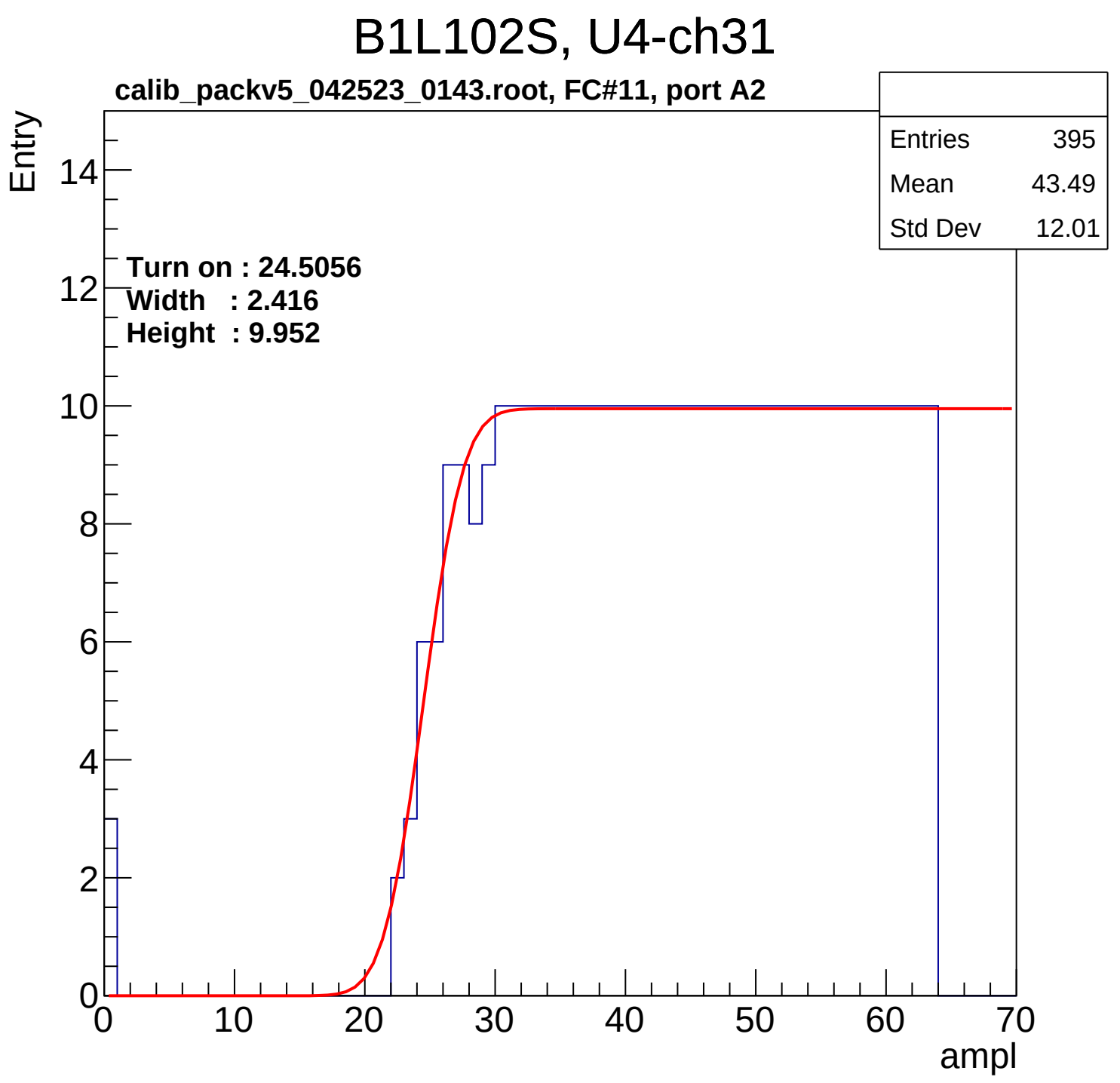
B1L102S, U4-ch31
calib_packv5_042523_0143.root, FC#11, port A2
Entries 395
Mean 43.49
Std Dev 12.01
Turn on : 24.5056
Width : 2.416
Height : 9.952
Entry
ampl
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2
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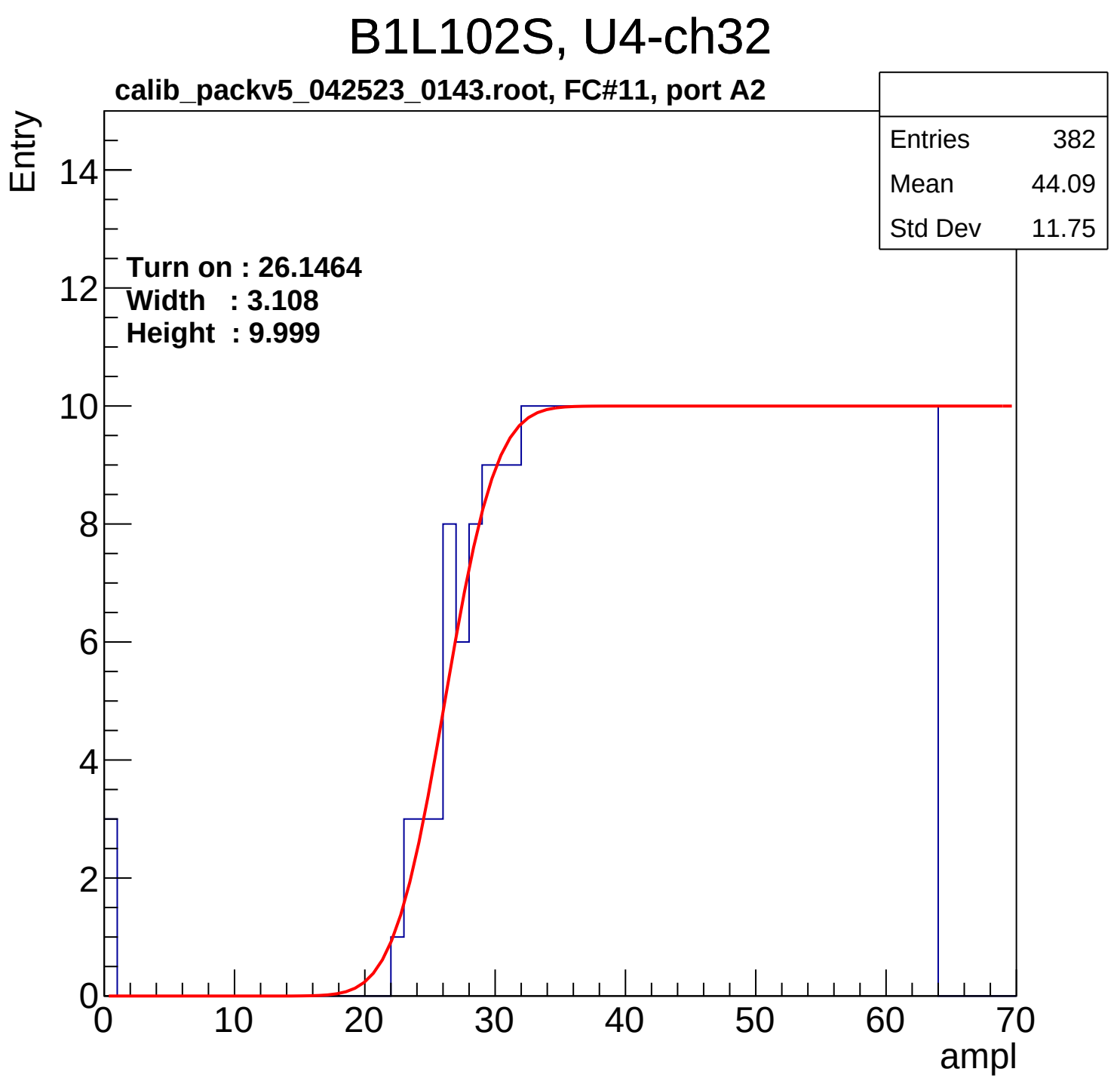
B1L102S, U4-ch32
calib_packv5_042523_0143.root, FC#11, port A2
Entries 382
Mean 44.09
Std Dev 11.75
Turn on : 26.1464
Width : 3.108
Height : 9.999
Entry
ampl
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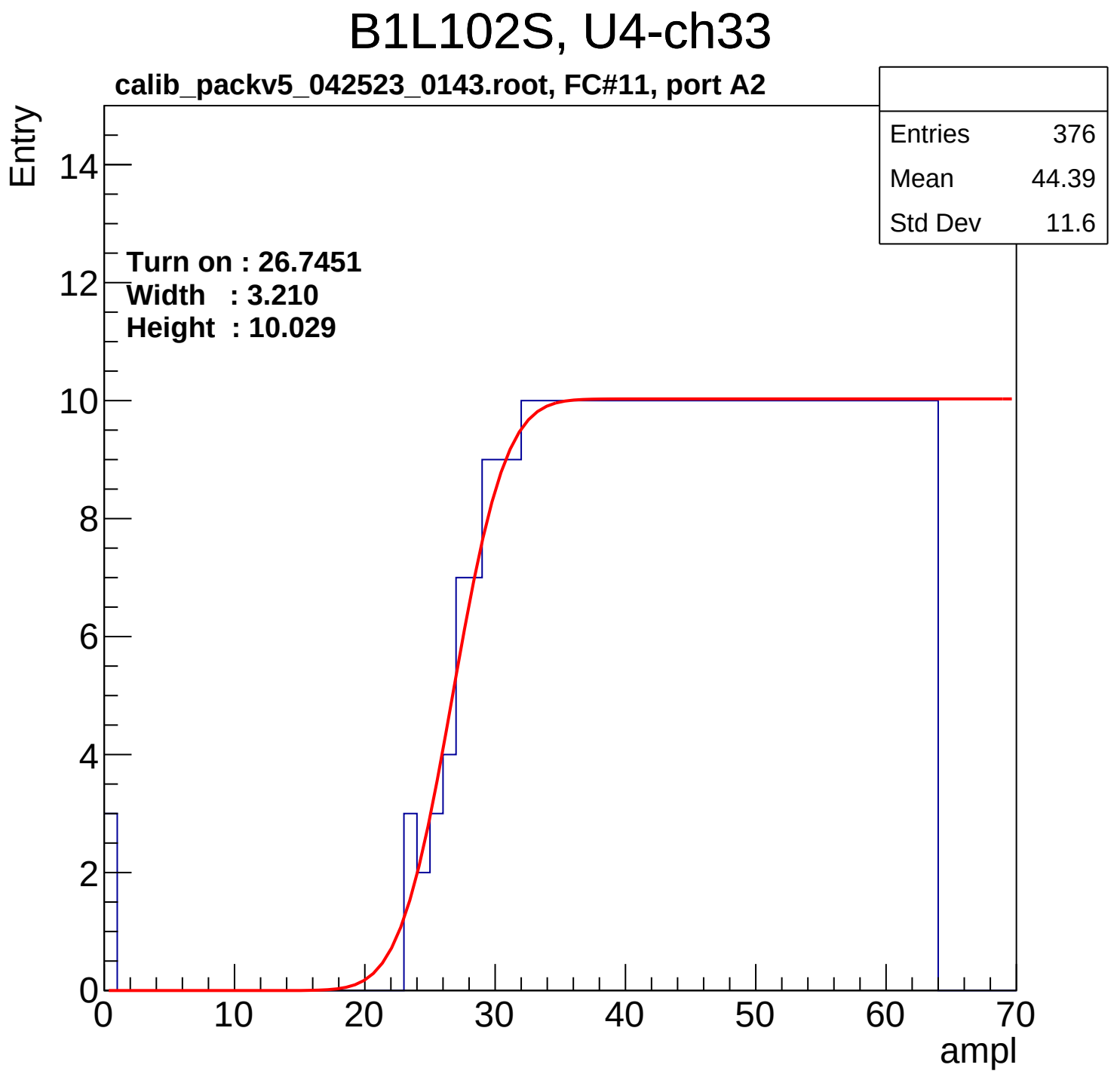
B1L102S, U4-ch33
calib_packv5_042523_0143.root, FC#11, port A2
Entries 376
Mean 44.39
Std Dev 11.6
Turn on : 26.7451
Width : 3.210
Height : 10.029
Entry
ampl
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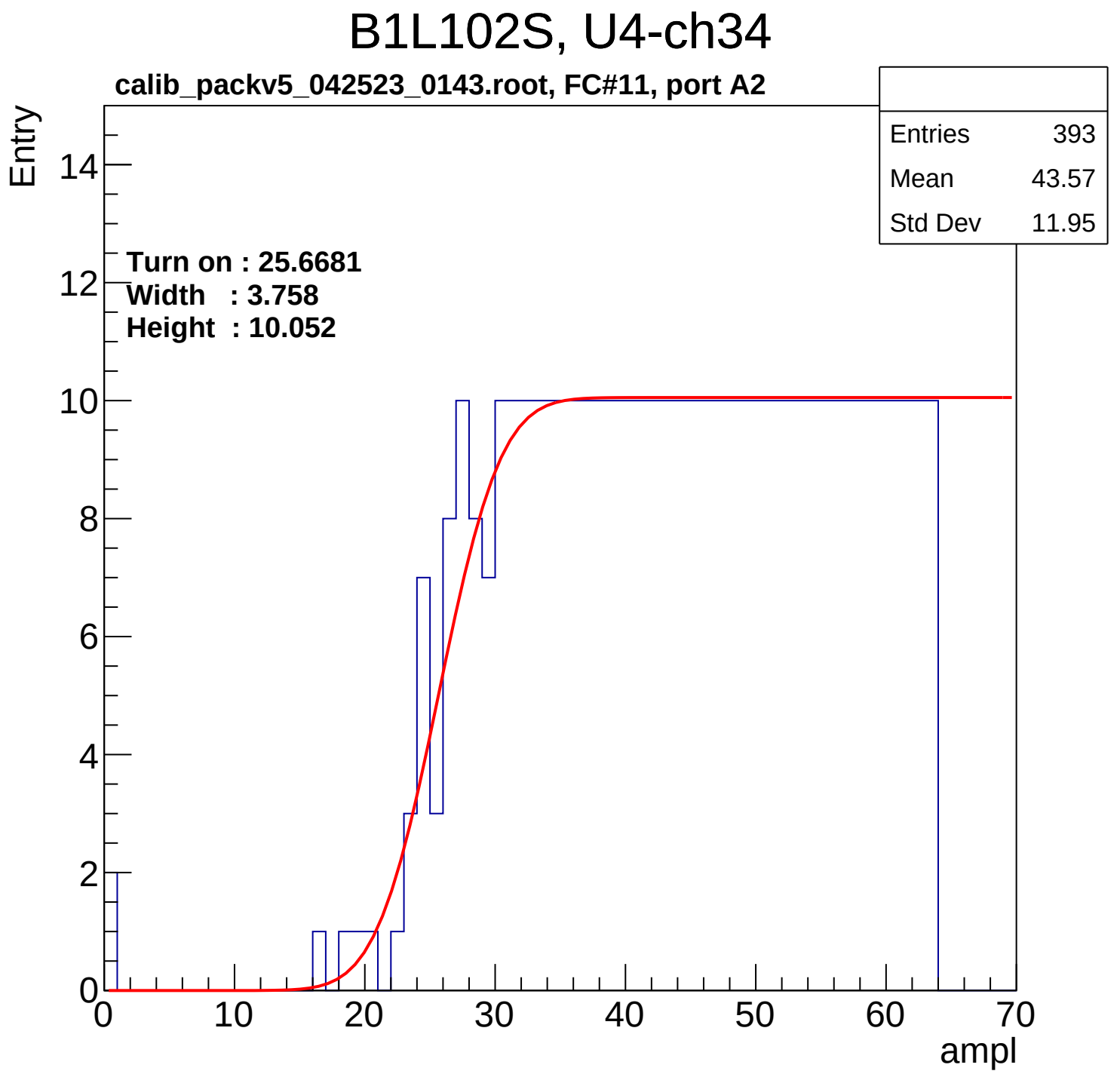
B1L102S, U4-ch34
calib_packv5_042523_0143.root, FC#11, port A2
Entries 393
Mean 43.57
Std Dev 11.95
Turn on : 25.6681
Width : 3.758
Height : 10.052
Entry
ampl
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4
6
8
10
12
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0
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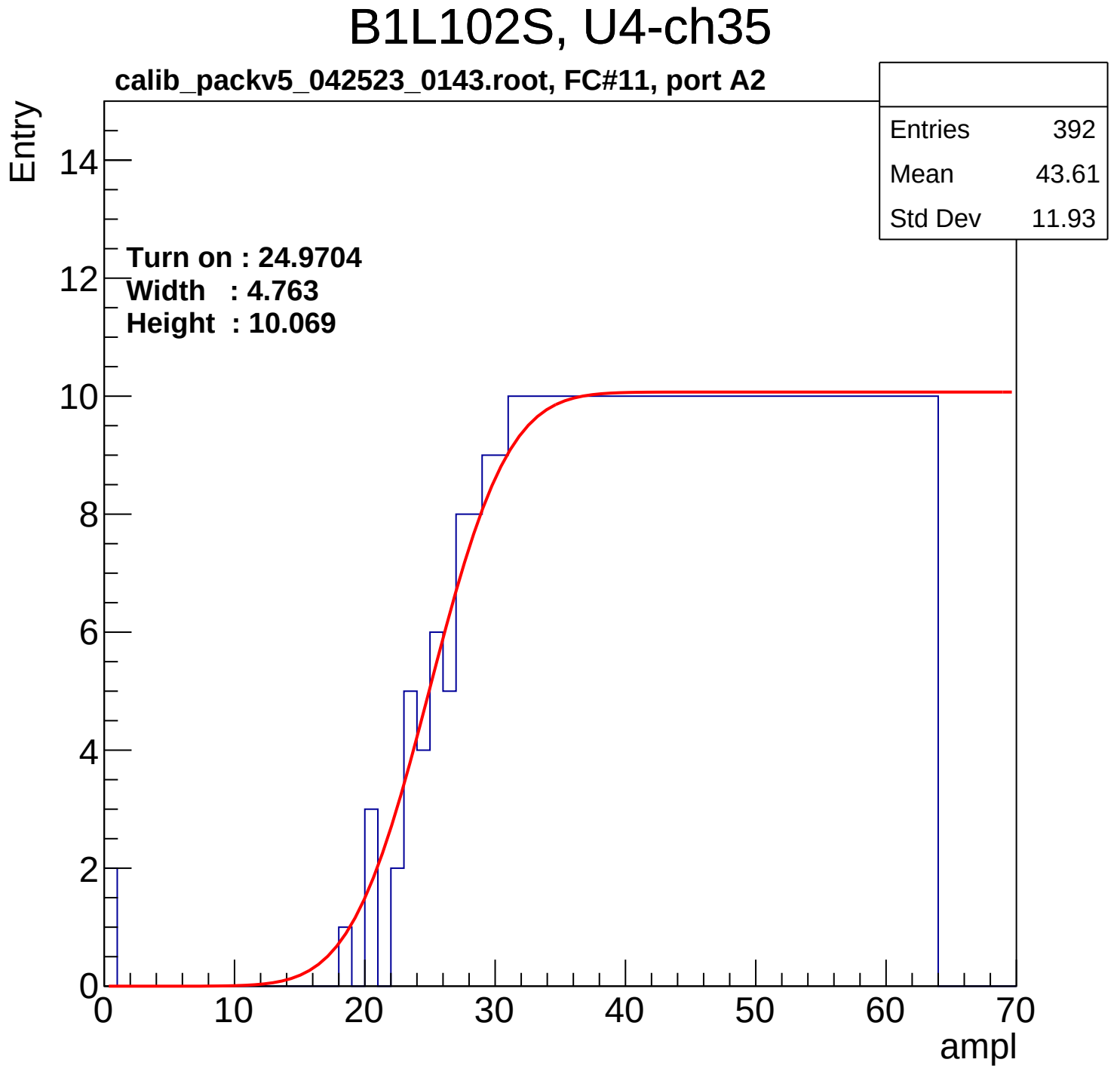
B1L102S, U4-ch35
calib_packv5_042523_0143.root, FC#11, port A2
Entries 392
Mean 43.61
Std Dev 11.93
Turn on : 24.9704
Width : 4.763
Height : 10.069
Entry
ampl
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6
8
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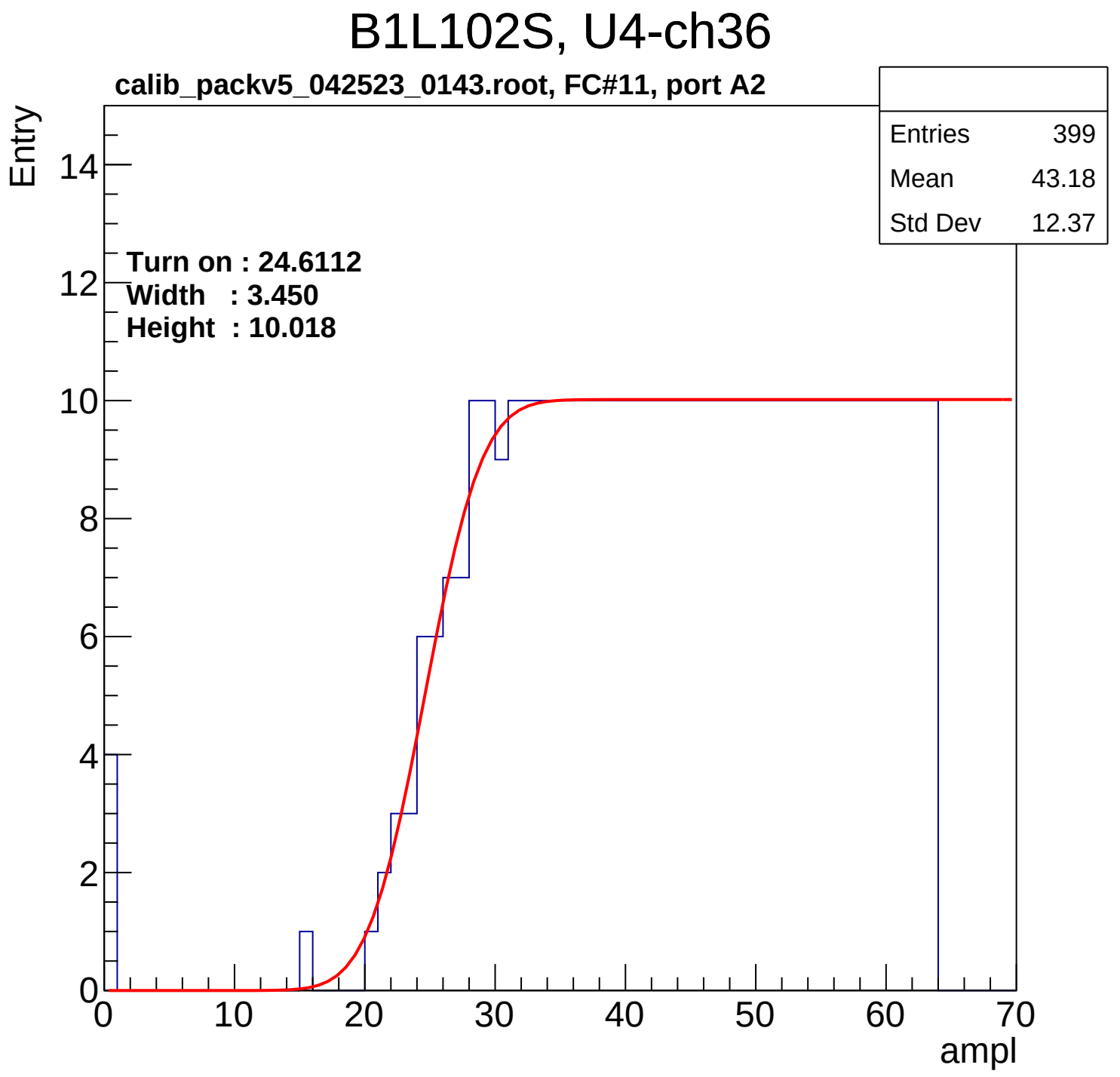
B1L102S, U4-ch36
calib_packv5_042523_0143.root, FC#11, port A2
Entries 399
Mean 43.18
Std Dev 12.37
Turn on : 24.6112
Width : 3.450
Height : 10.018
Entry
ampl
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2
4
6
8
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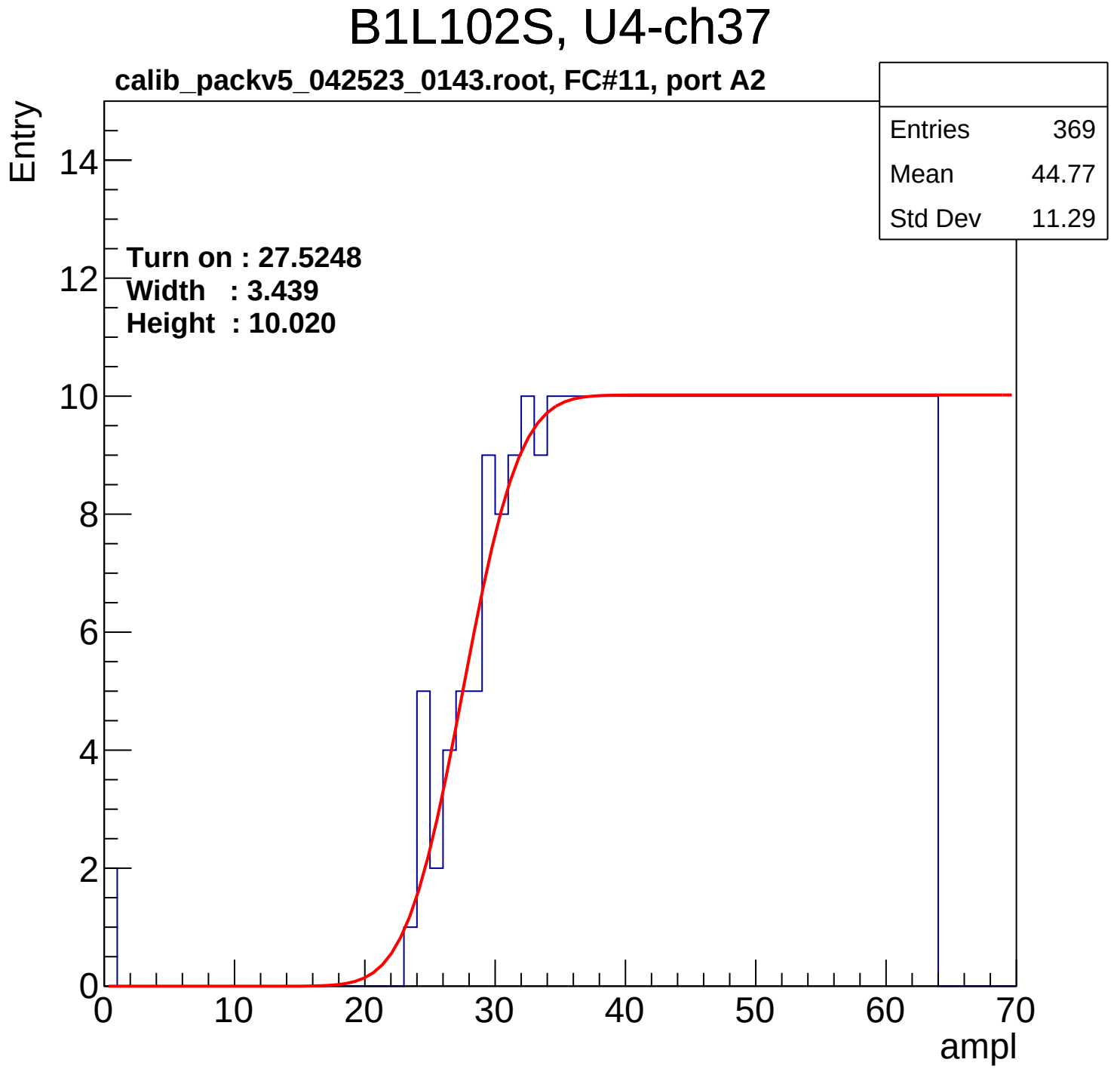
B1L102S, U4-ch37
calib_packv5_042523_0143.root, FC#11, port A2
Entries 369
Mean 44.77
Std Dev 11.29
Turn on : 27.5248
Width : 3.439
Height : 10.020
Entry
ampl
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6
8
10
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0
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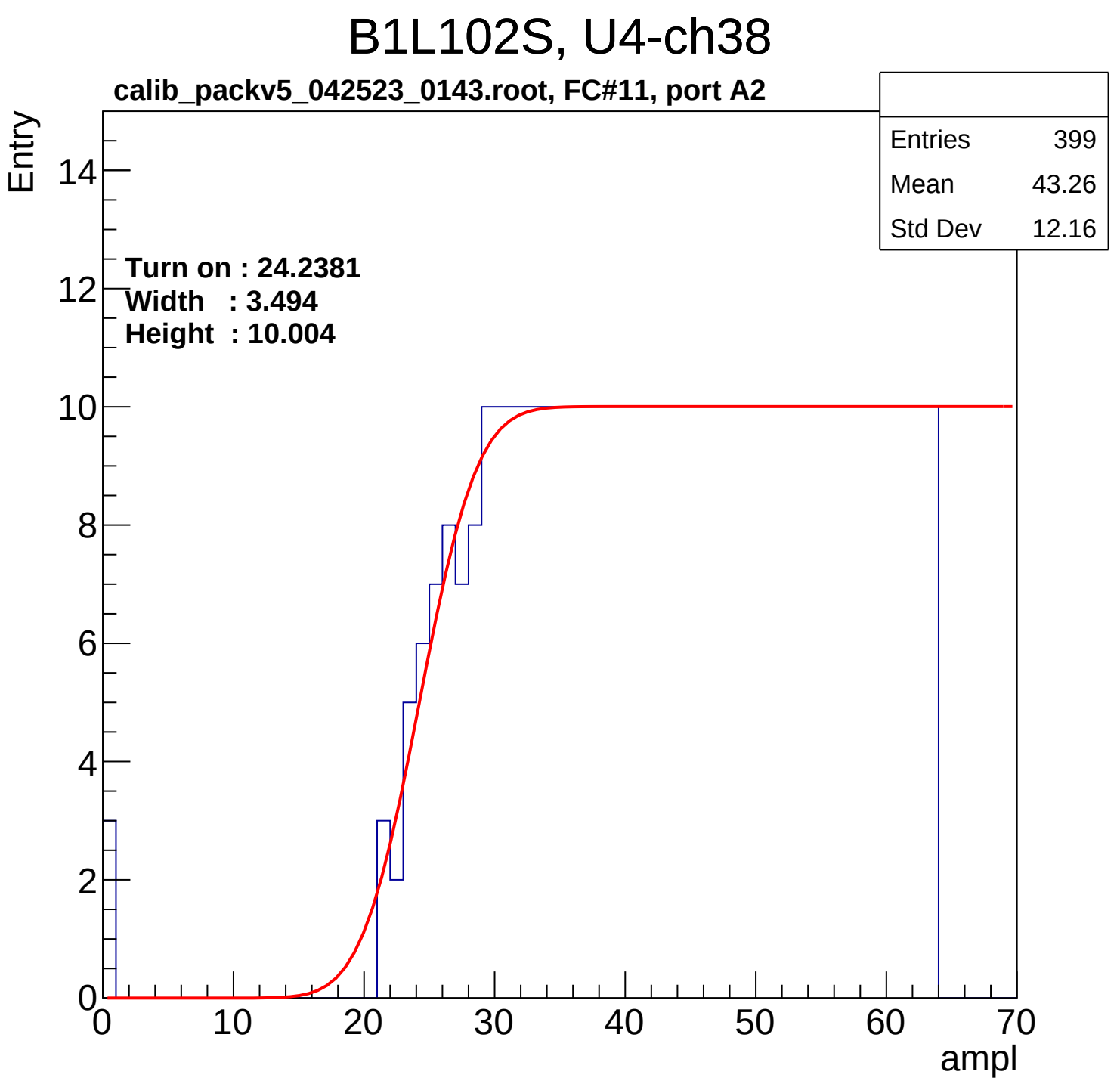
B1L102S, U4-ch38
calib_packv5_042523_0143.root, FC#11, port A2
Entries 399
Mean 43.26
Std Dev 12.16
Turn on : 24.2381
Width : 3.494
Height : 10.004
Entry
ampl
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6
8
10
12
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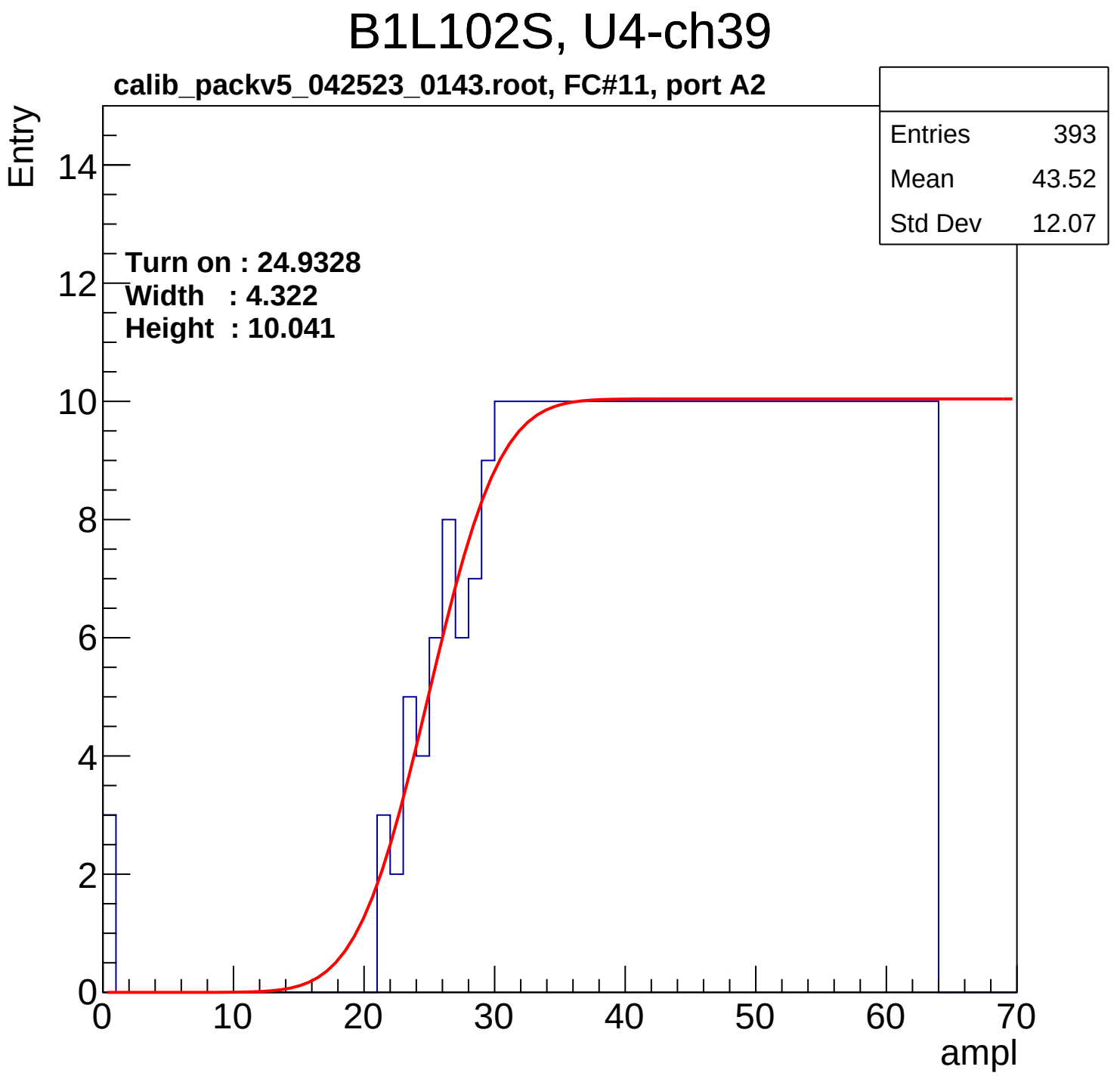
B1L102S, U4-ch39
calib_packv5_042523_0143.root, FC#11, port A2
Entries 393
Mean 43.52
Std Dev 12.07
Turn on : 24.9328
Width : 4.322
Height : 10.041
Entry
ampl
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6
8
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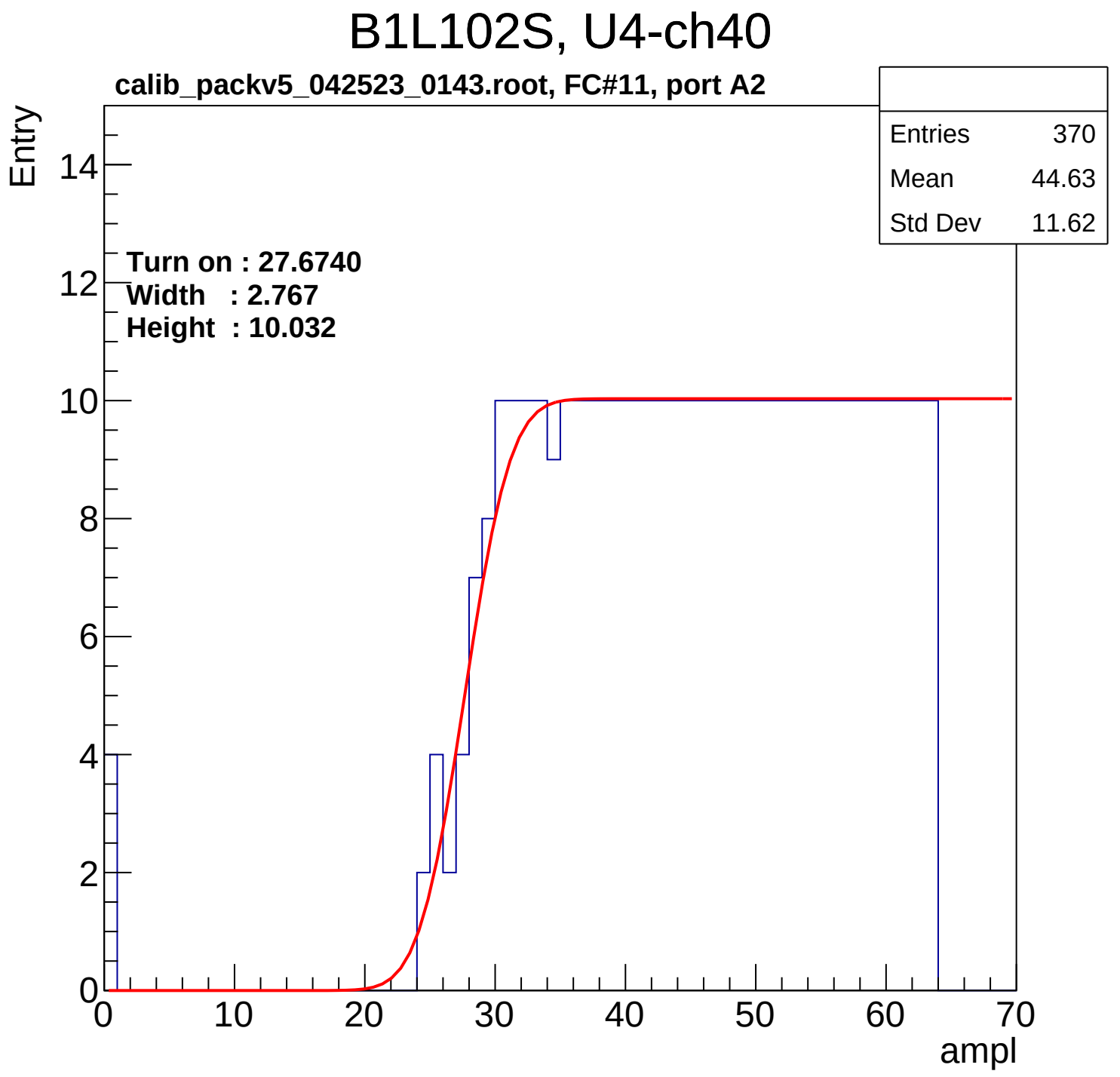
B1L102S, U4-ch40
calib_packv5_042523_0143.root, FC#11, port A2
Entries 370
Mean 44.63
Std Dev 11.62
Turn on : 27.6740
Width : 2.767
Height : 10.032
Entry
ampl
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6
8
10
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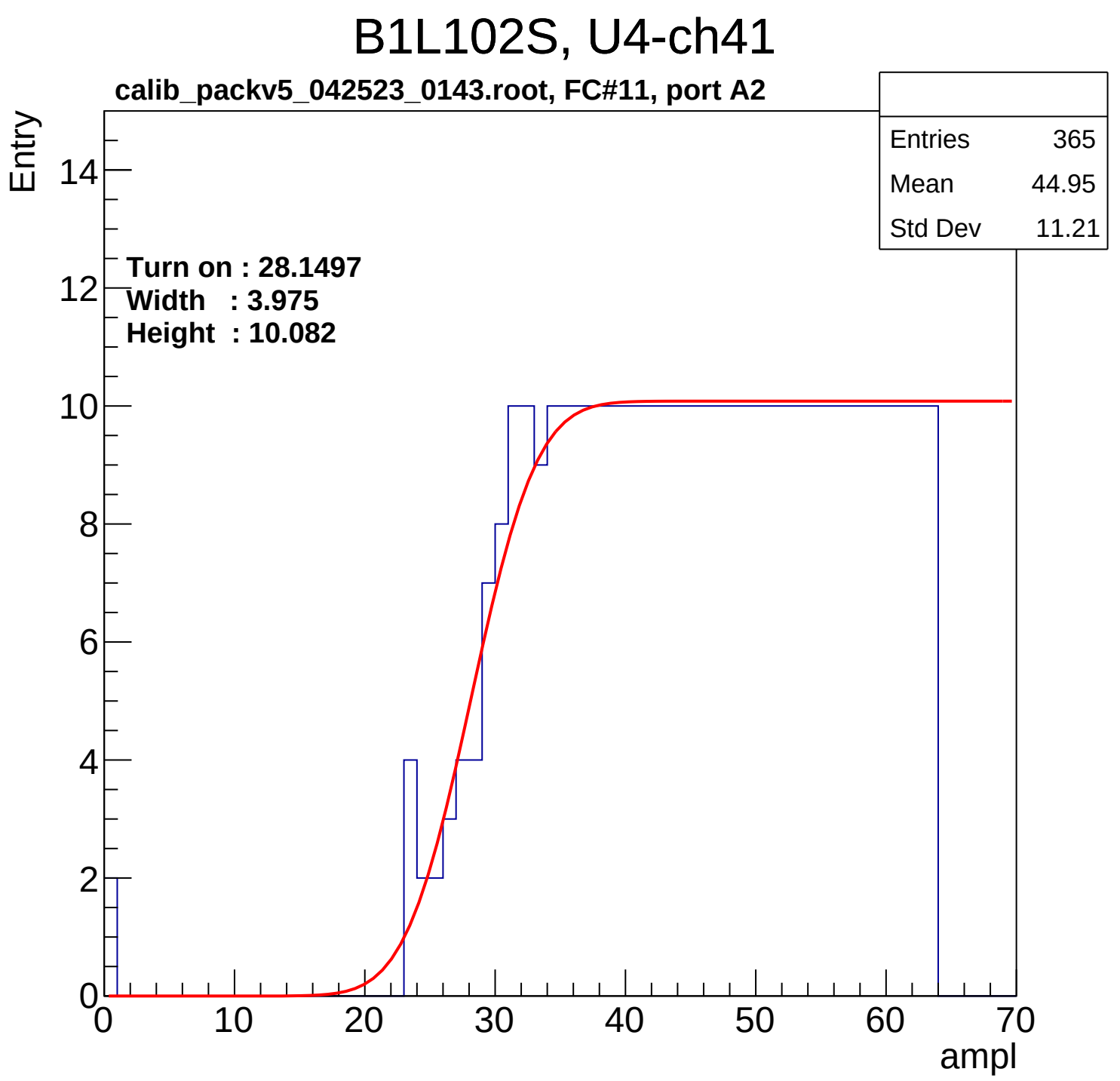
B1L102S, U4-ch41
calib_packv5_042523_0143.root, FC#11, port A2
Entries 365
Mean 44.95
Std Dev 11.21
Turn on : 28.1497
Width : 3.975
Height : 10.082
Entry
ampl
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6
8
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12
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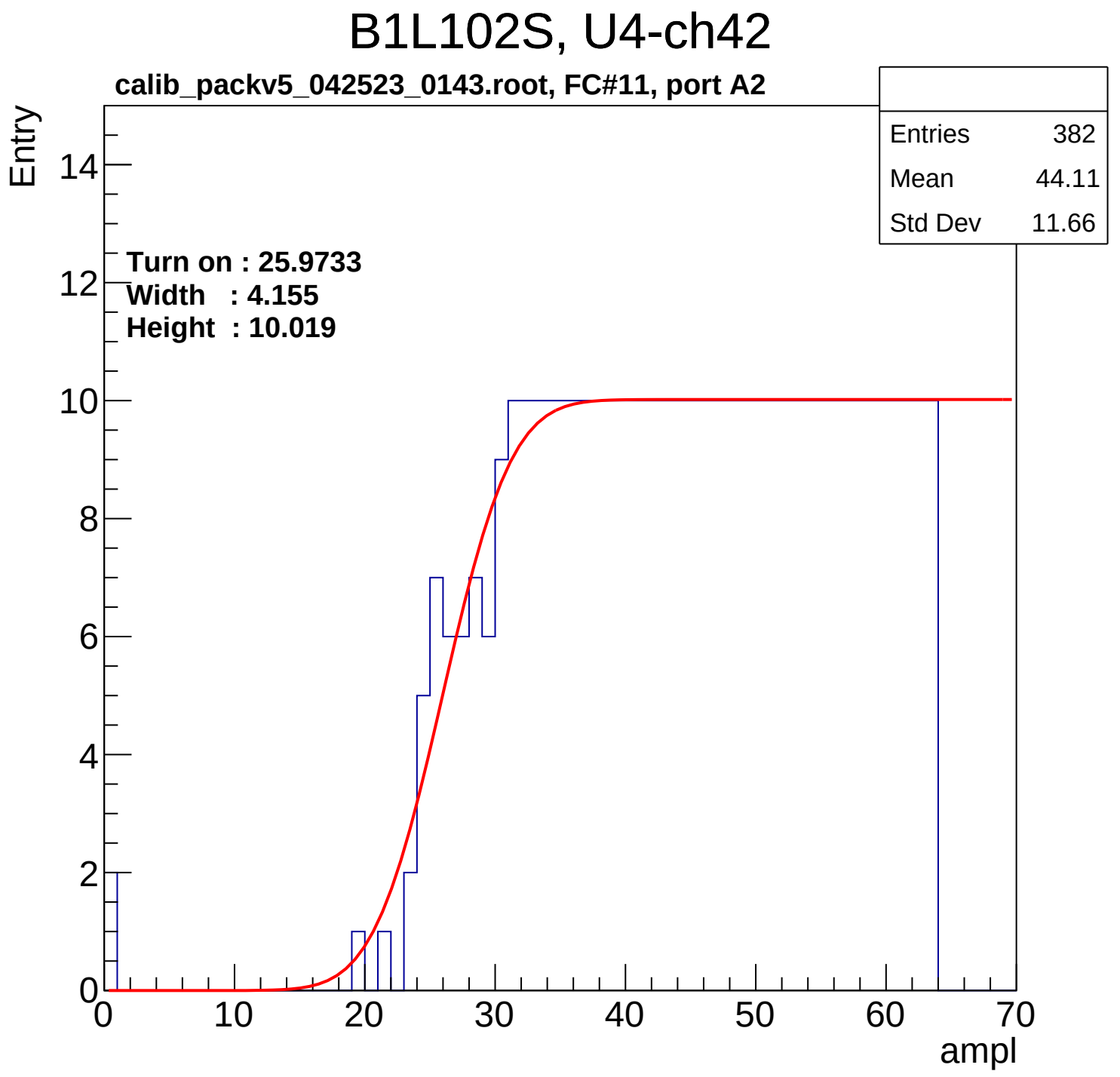
B1L102S, U4-ch42
calib_packv5_042523_0143.root, FC#11, port A2
Entries 382
Mean 44.11
Std Dev 11.66
Turn on : 25.9733
Width : 4.155
Height : 10.019
Entry
ampl
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4
6
8
10
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0
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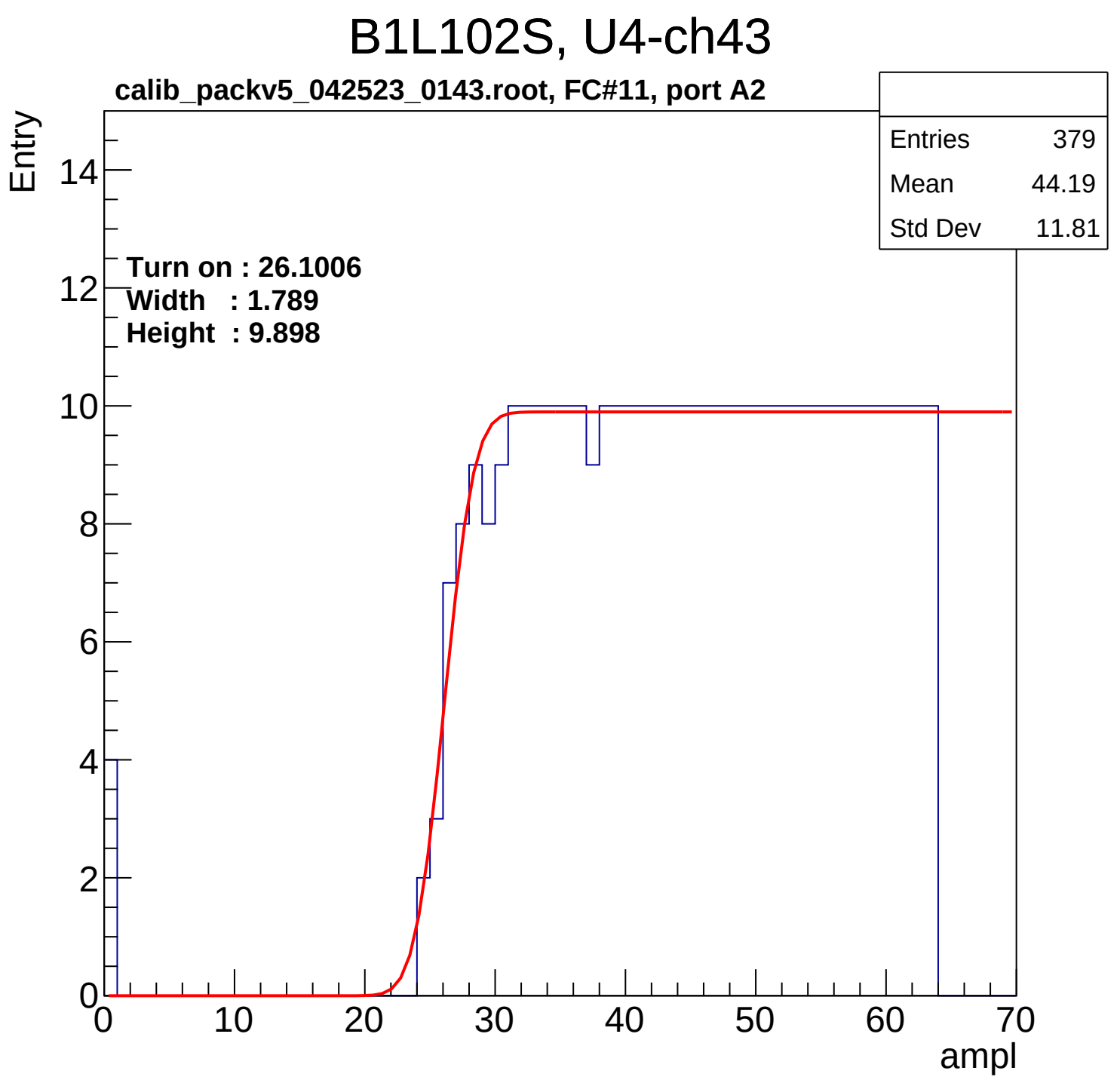
B1L102S, U4-ch43
calib_packv5_042523_0143.root, FC#11, port A2
Entries 379
Mean 44.19
Std Dev 11.81
Turn on : 26.1006
Width : 1.789
Height : 9.898
Entry
ampl
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6
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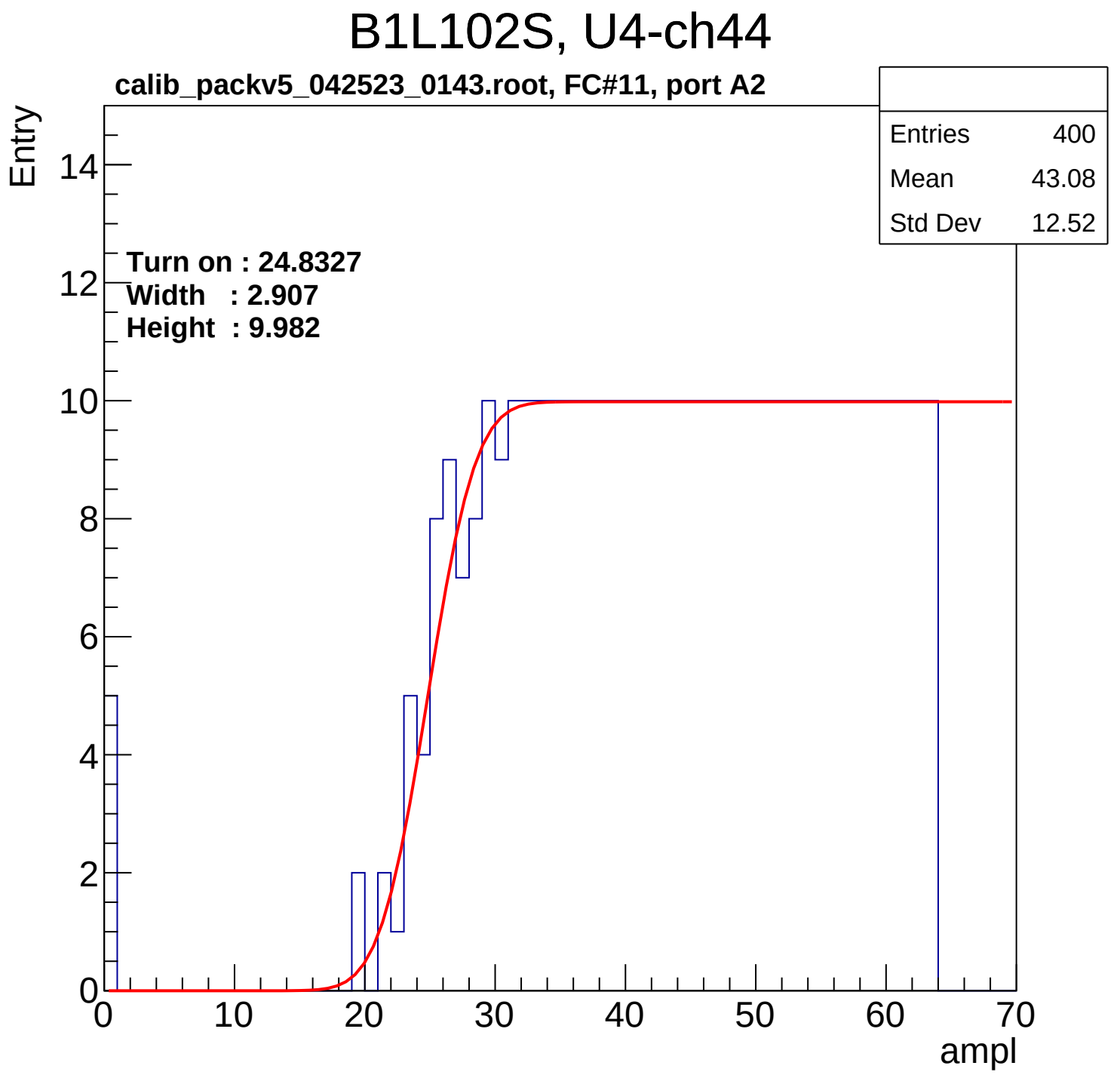
B1L102S, U4-ch44
calib_packv5_042523_0143.root, FC#11, port A2
Entries 400
Mean 43.08
Std Dev 12.52
Turn on : 24.8327
Width : 2.907
Height : 9.982
Entry
ampl
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6
8
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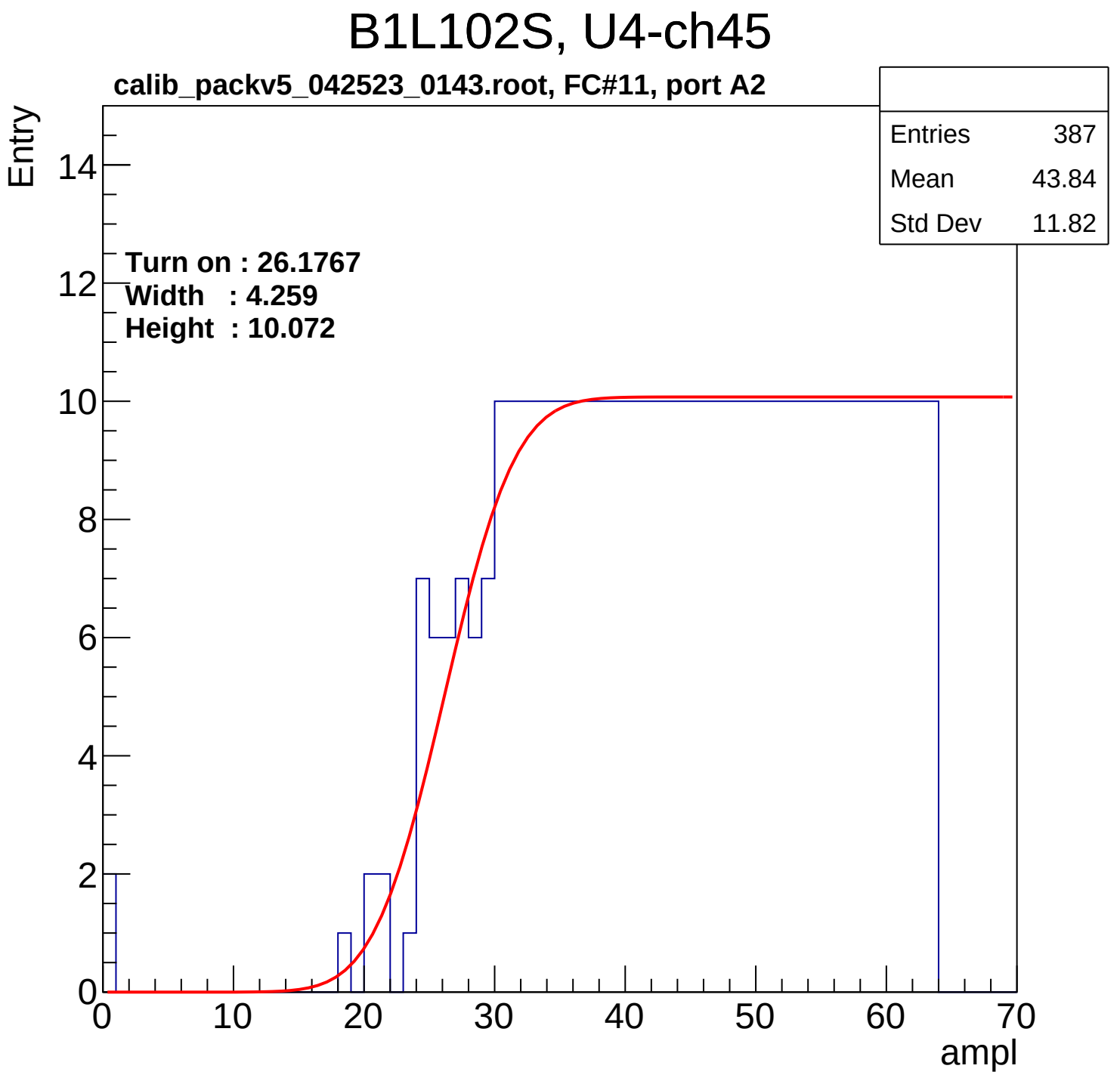
B1L102S, U4-ch45
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 43.84
Std Dev 11.82
Turn on : 26.1767
Width : 4.259
Height : 10.072
Entry
ampl
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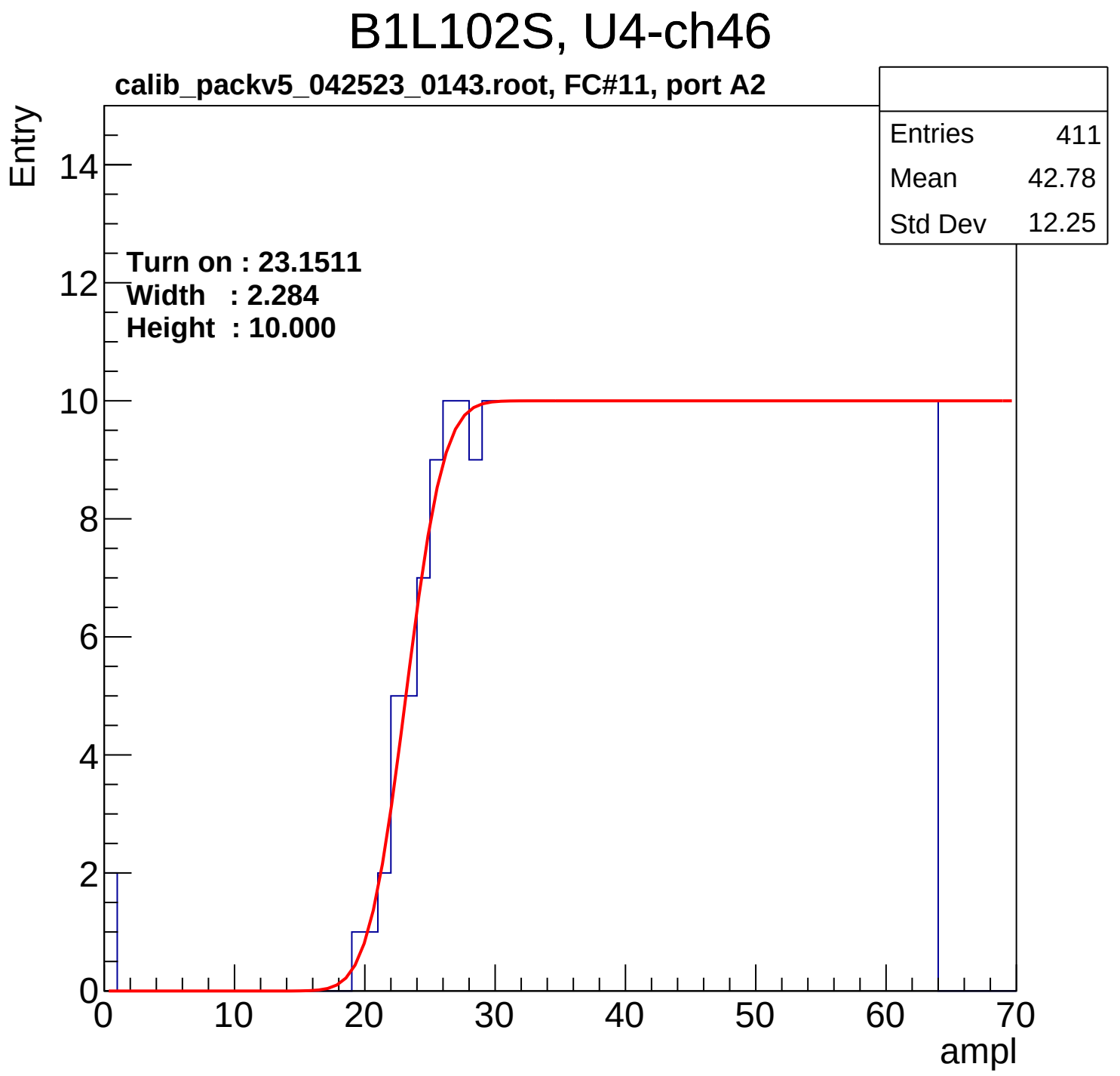
B1L102S, U4-ch46
calib_packv5_042523_0143.root, FC#11, port A2
Entries 411
Mean 42.78
Std Dev 12.25
Turn on : 23.1511
Width : 2.284
Height : 10.000
Entry
ampl
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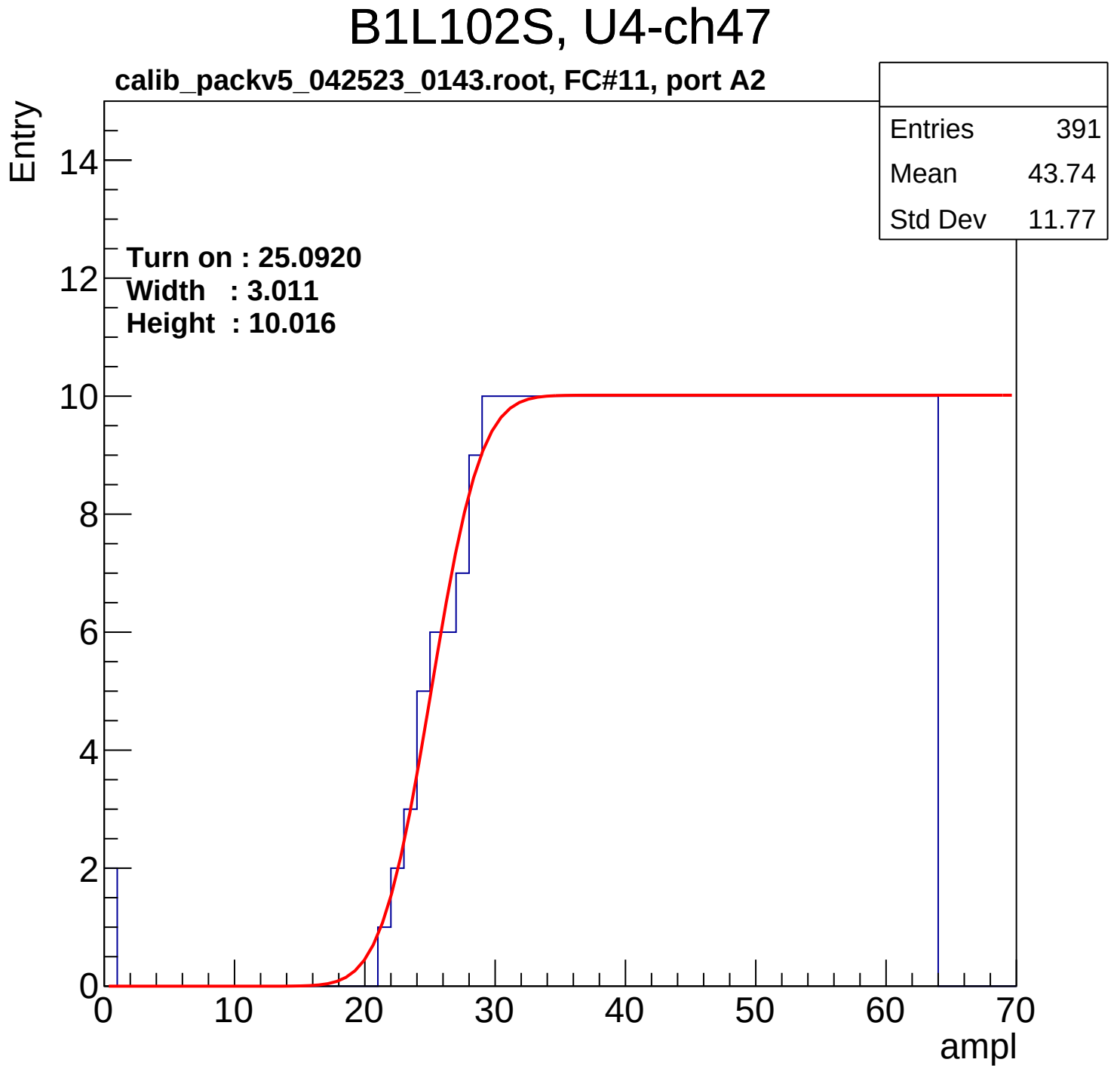
B1L102S, U4-ch47
calib_packv5_042523_0143.root, FC#11, port A2
Entries 391
Mean 43.74
Std Dev 11.77
Turn on : 25.0920
Width : 3.011
Height : 10.016
Entry
ampl
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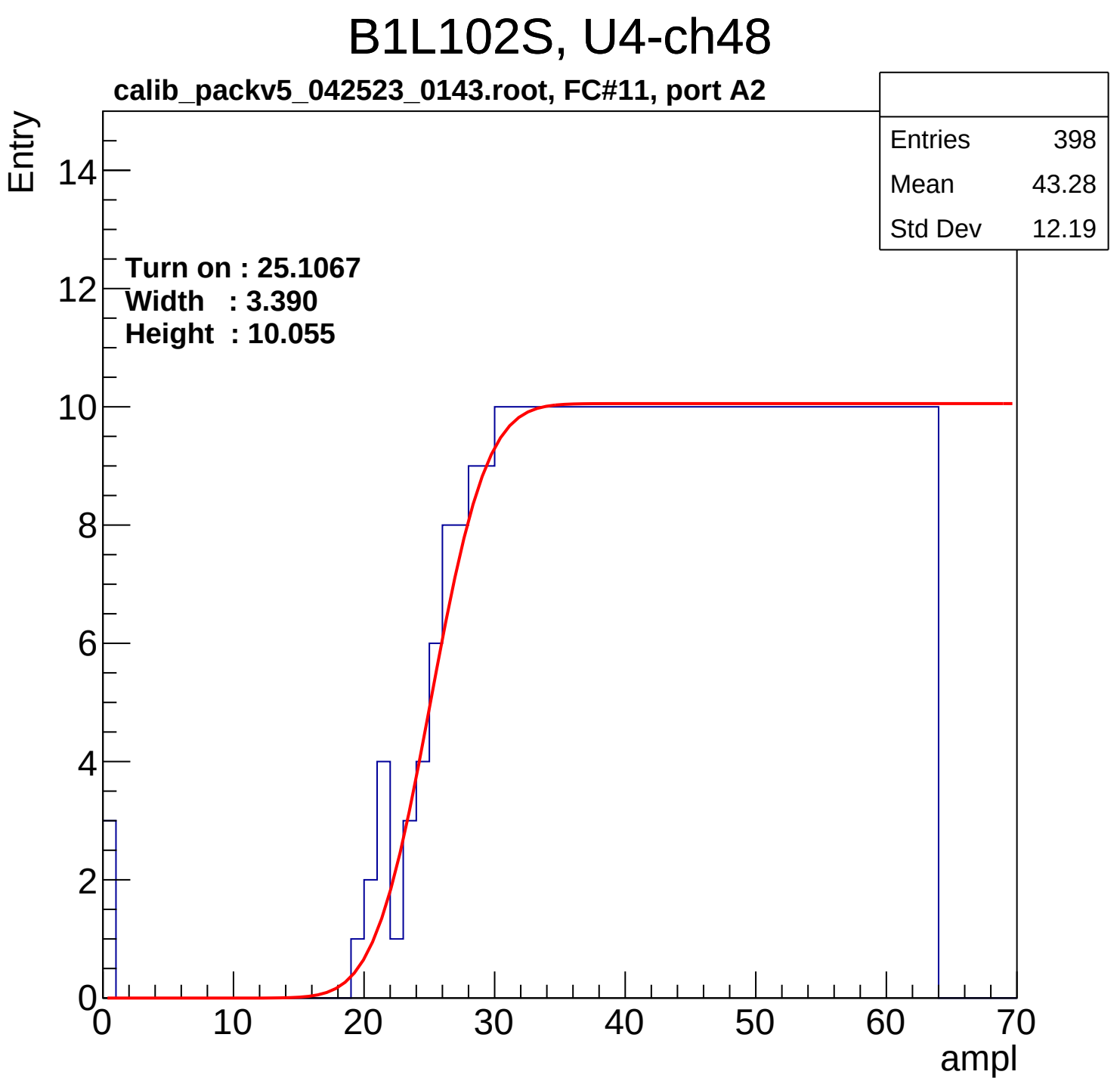
B1L102S, U4-ch48
calib_packv5_042523_0143.root, FC#11, port A2
Entries 398
Mean 43.28
Std Dev 12.19
Turn on : 25.1067
Width : 3.390
Height : 10.055
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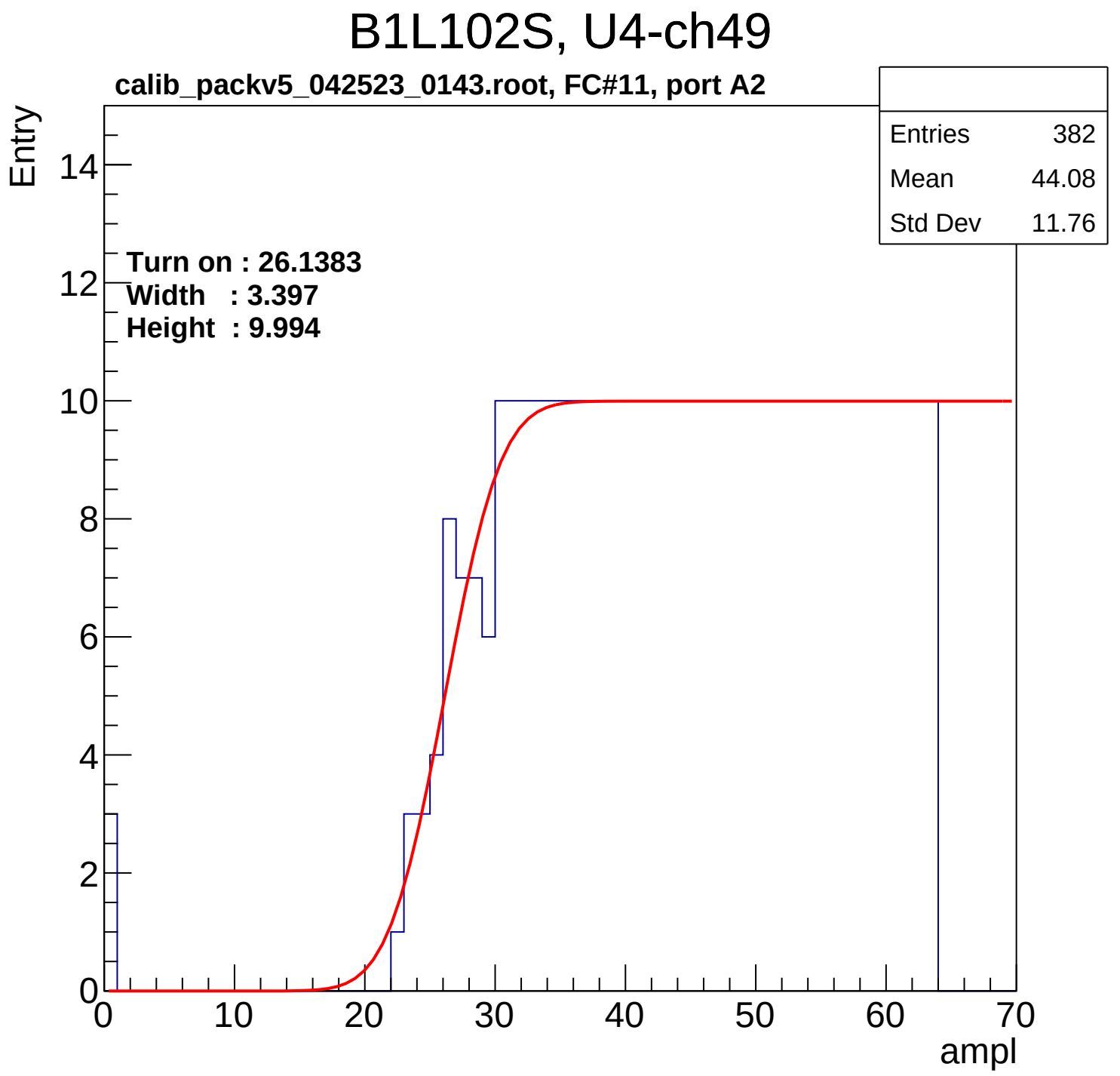
B1L102S, U4-ch49
calib_packv5_042523_0143.root, FC#11, port A2
Entries 382
Mean 44.08
Std Dev 11.76
Turn on : 26.1383
Width : 3.397
Height : 9.994
Entry
ampl
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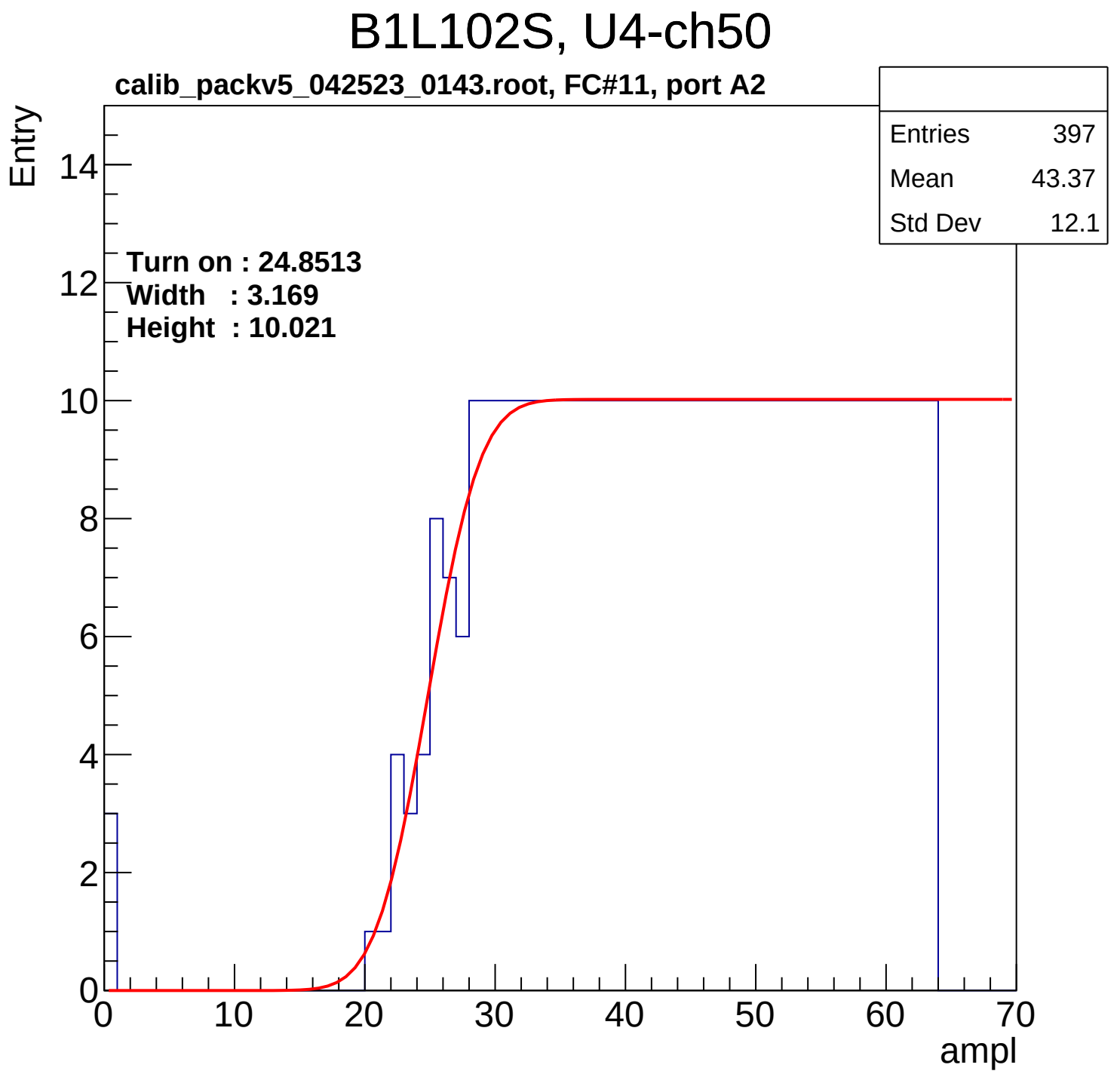
B1L102S, U4-ch50
calib_packv5_042523_0143.root, FC#11, port A2
Entries 397
Mean 43.37
Std Dev 12.1
Turn on : 24.8513
Width : 3.169
Height : 10.021
Entry
ampl
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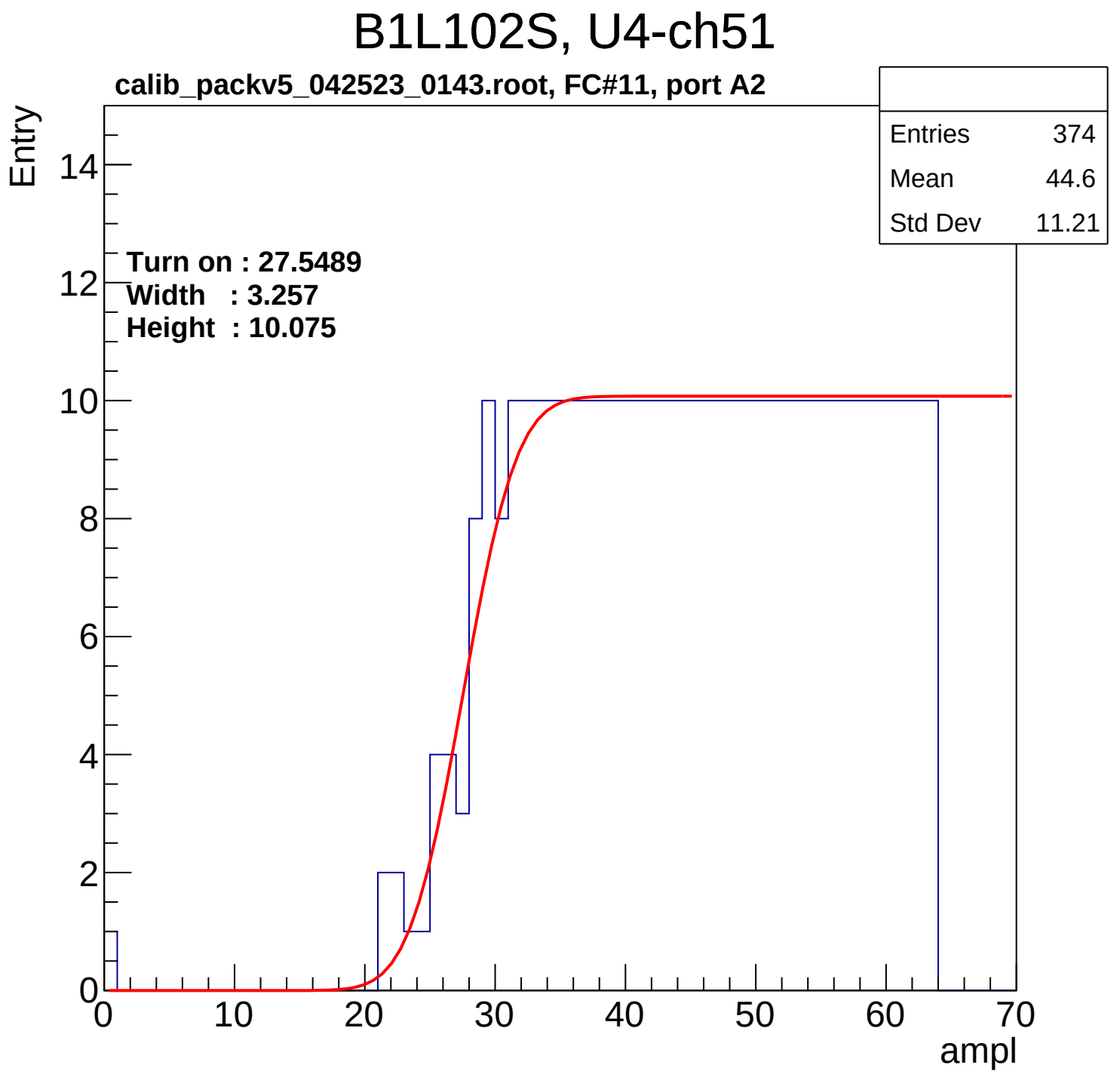
B1L102S, U4-ch51
calib_packv5_042523_0143.root, FC#11, port A2
Entries 374
Mean 44.6
Std Dev 11.21
Turn on : 27.5489
Width : 3.257
Height : 10.075
Entry
ampl
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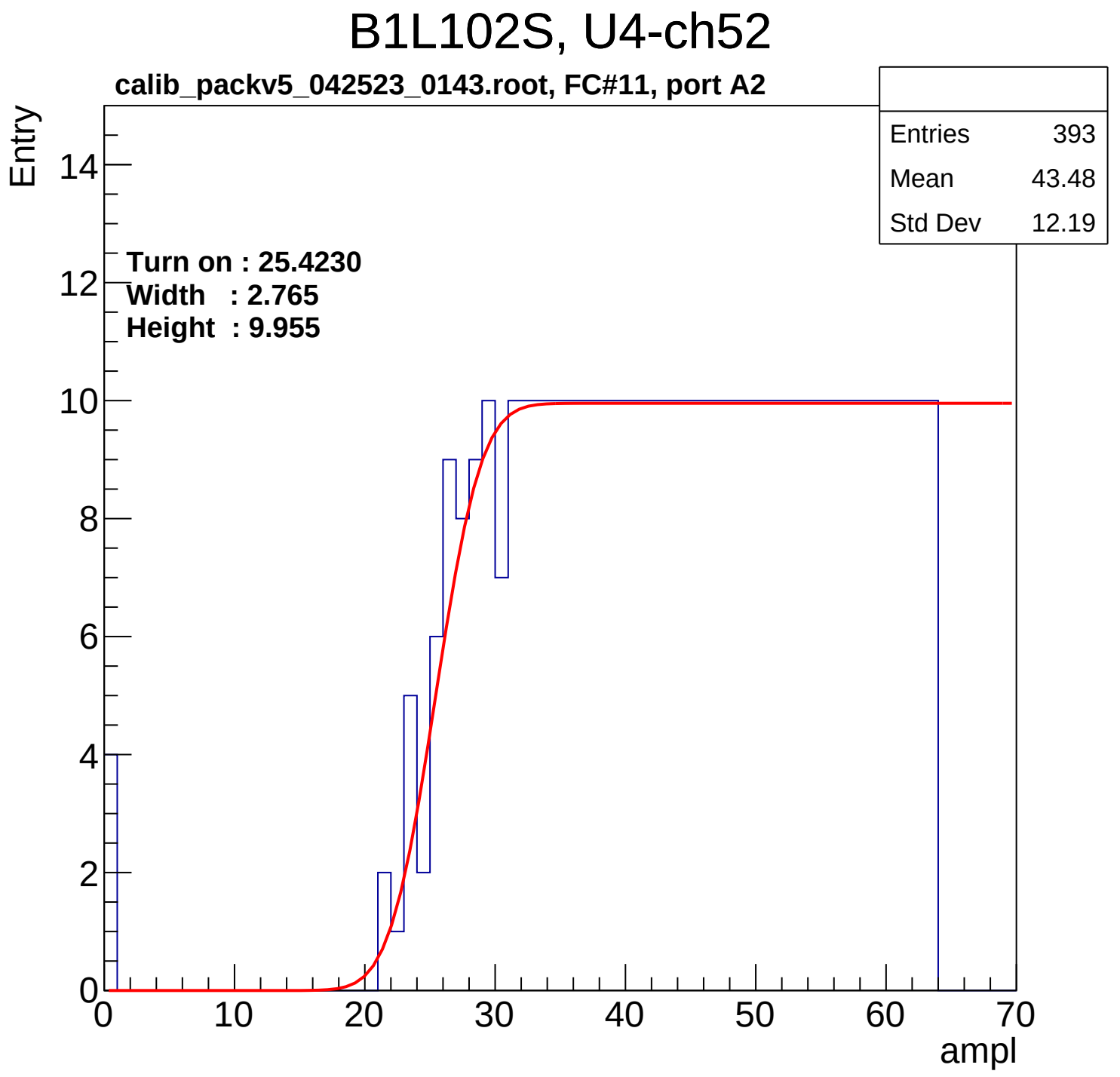
B1L102S, U4-ch52
calib_packv5_042523_0143.root, FC#11, port A2
Entries 393
Mean 43.48
Std Dev 12.19
Turn on : 25.4230
Width : 2.765
Height : 9.955
Entry
ampl
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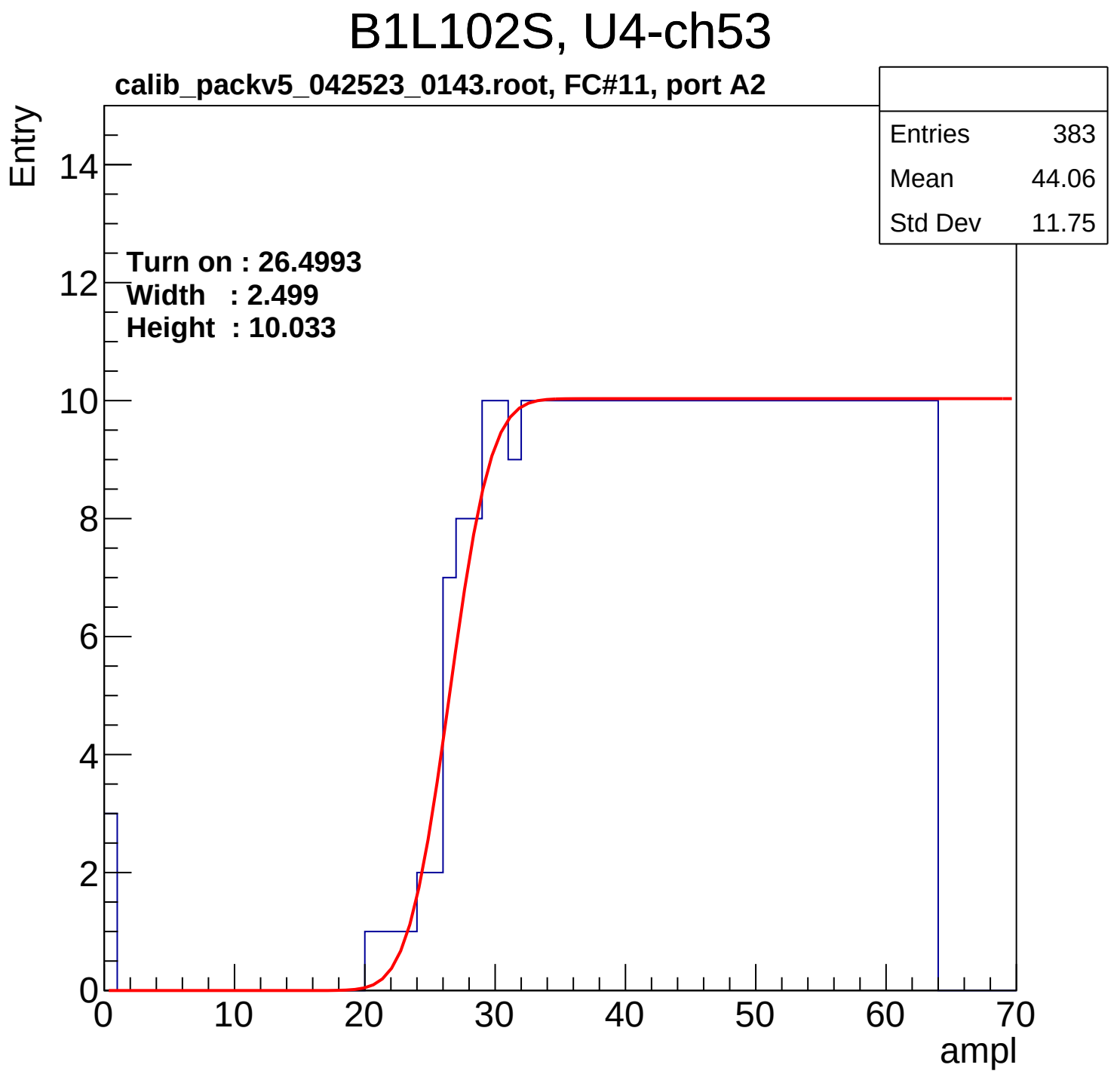
B1L102S, U4-ch53
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 44.06
Std Dev 11.75
Turn on : 26.4993
Width : 2.499
Height : 10.033
Entry
ampl
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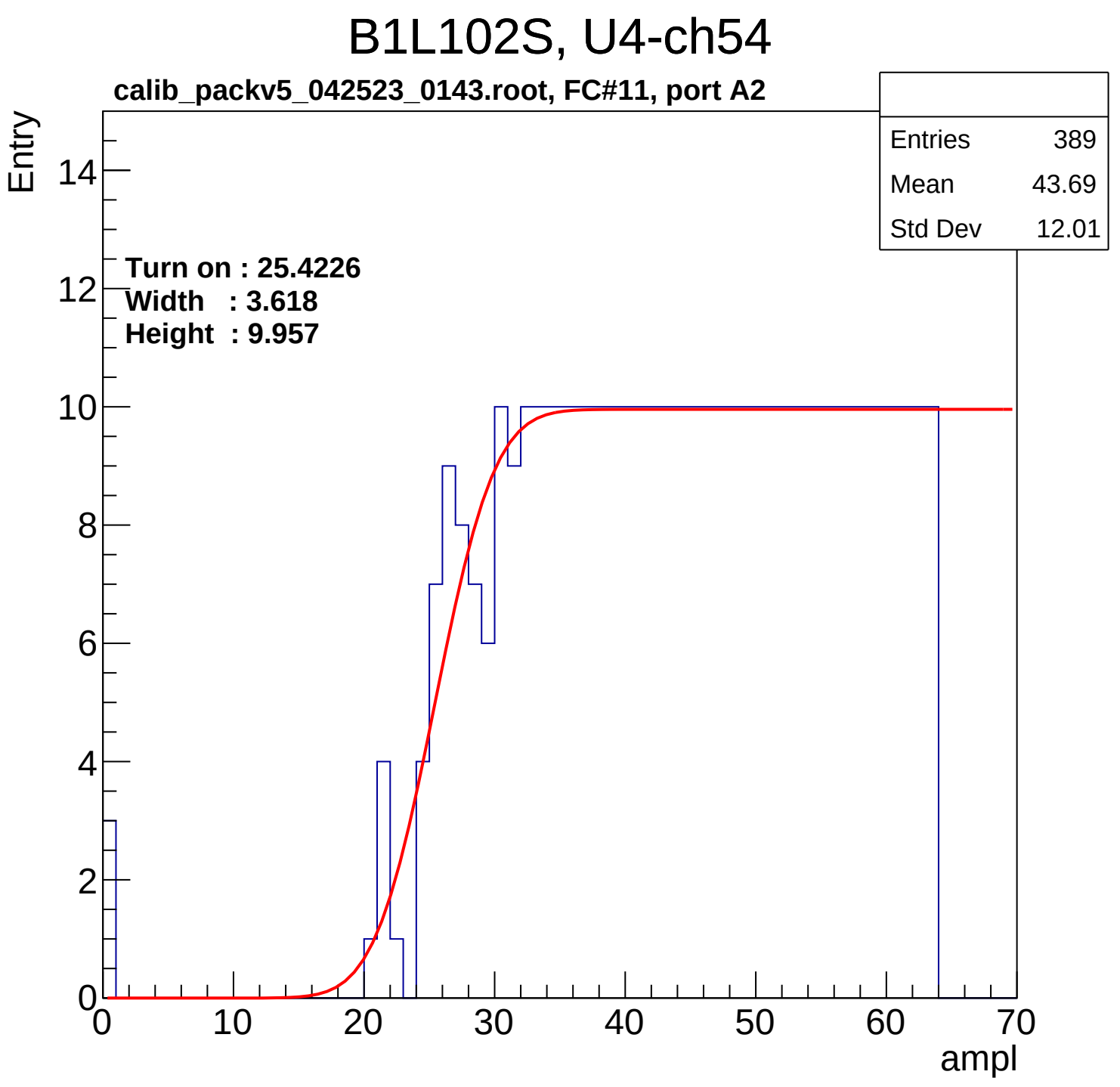
B1L102S, U4-ch54
calib_packv5_042523_0143.root, FC#11, port A2
Entries 389
Mean 43.69
Std Dev 12.01
Turn on : 25.4226
Width : 3.618
Height : 9.957
Entry
ampl
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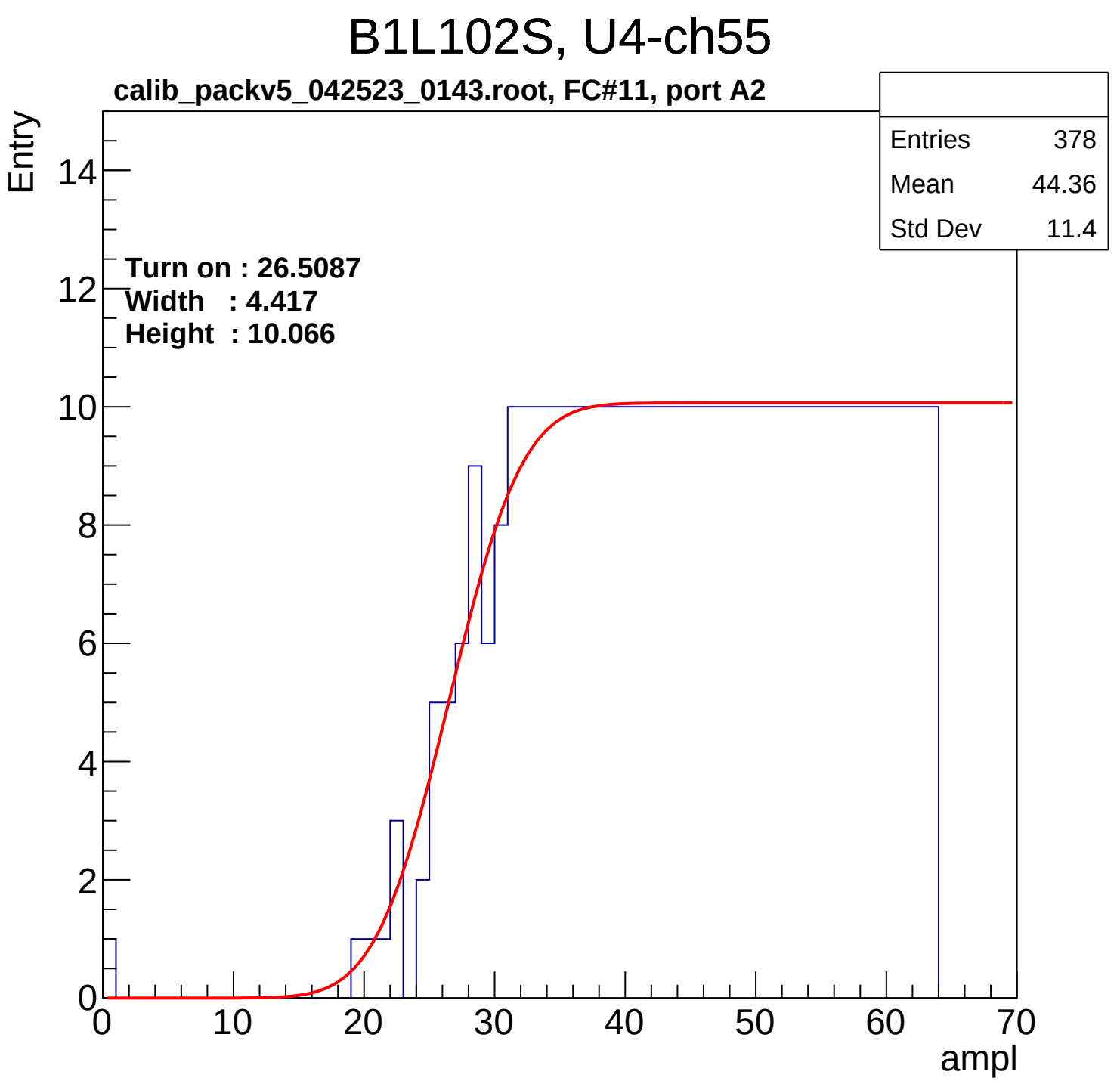
B1L102S, U4-ch55
calib_packv5_042523_0143.root, FC#11, port A2
Entries 378
Mean 44.36
Std Dev 11.4
Turn on : 26.5087
Width : 4.417
Height : 10.066
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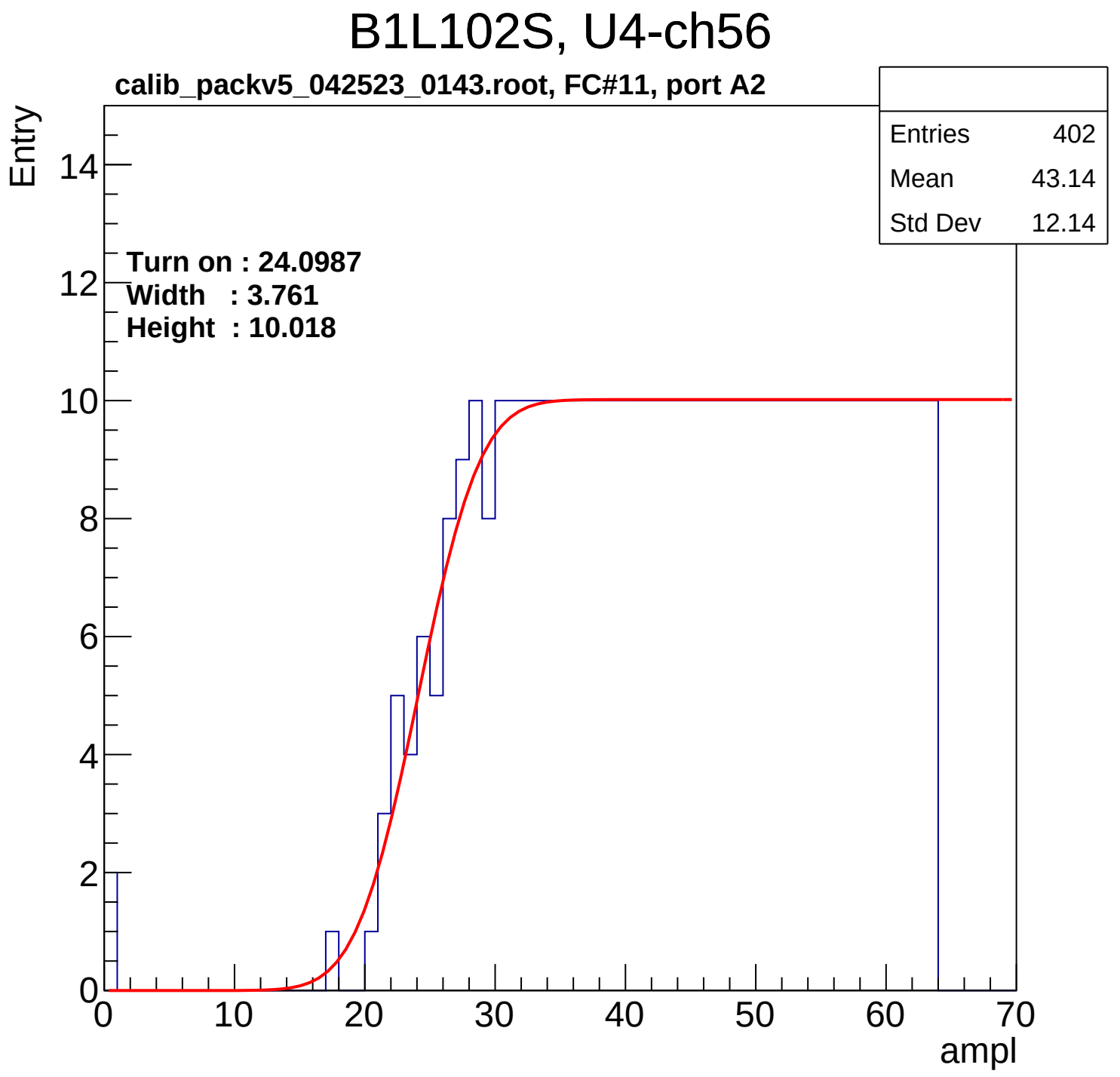
B1L102S, U4-ch56
calib_packv5_042523_0143.root, FC#11, port A2
Entries 402
Mean 43.14
Std Dev 12.14
Turn on : 24.0987
Width : 3.761
Height : 10.018
Entry
ampl
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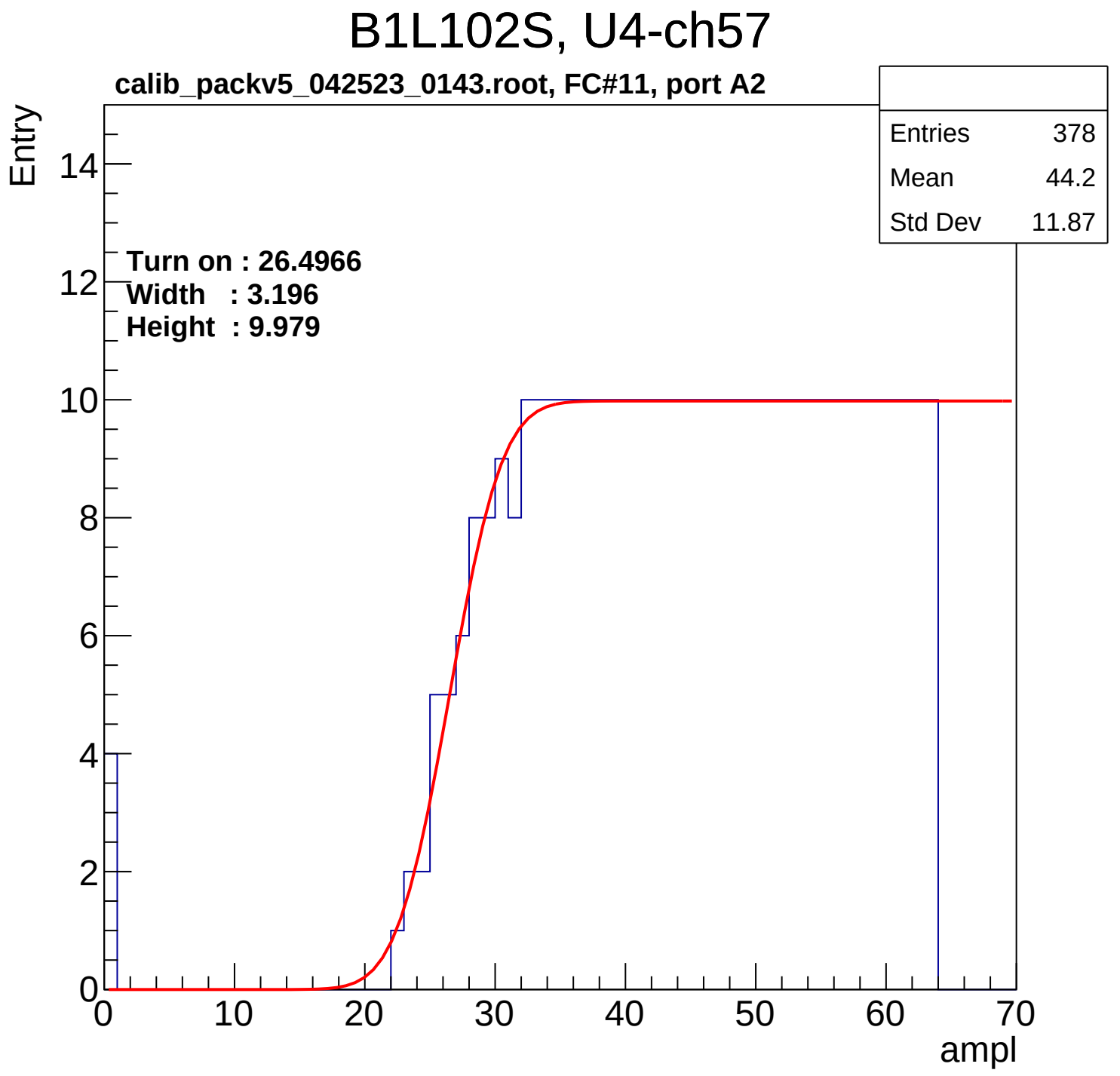
B1L102S, U4-ch57
calib_packv5_042523_0143.root, FC#11, port A2
Entries 378
Mean 44.2
Std Dev 11.87
Turn on : 26.4966
Width : 3.196
Height : 9.979
Entry
ampl
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6
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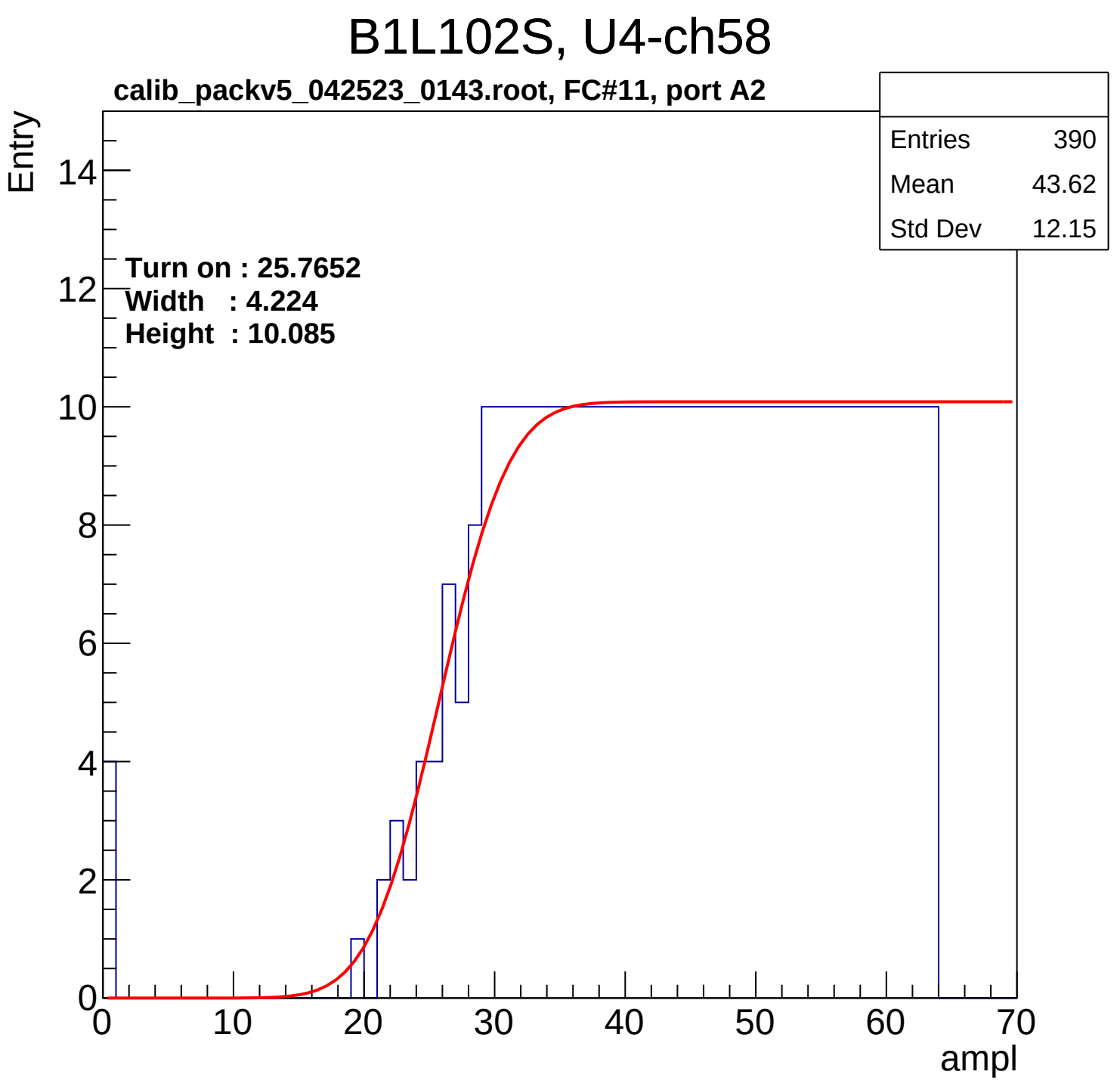
B1L102S, U4-ch58
calib_packv5_042523_0143.root, FC#11, port A2
Entries 390
Mean 43.62
Std Dev 12.15
Turn on : 25.7652
Width : 4.224
Height : 10.085
Entry
ampl
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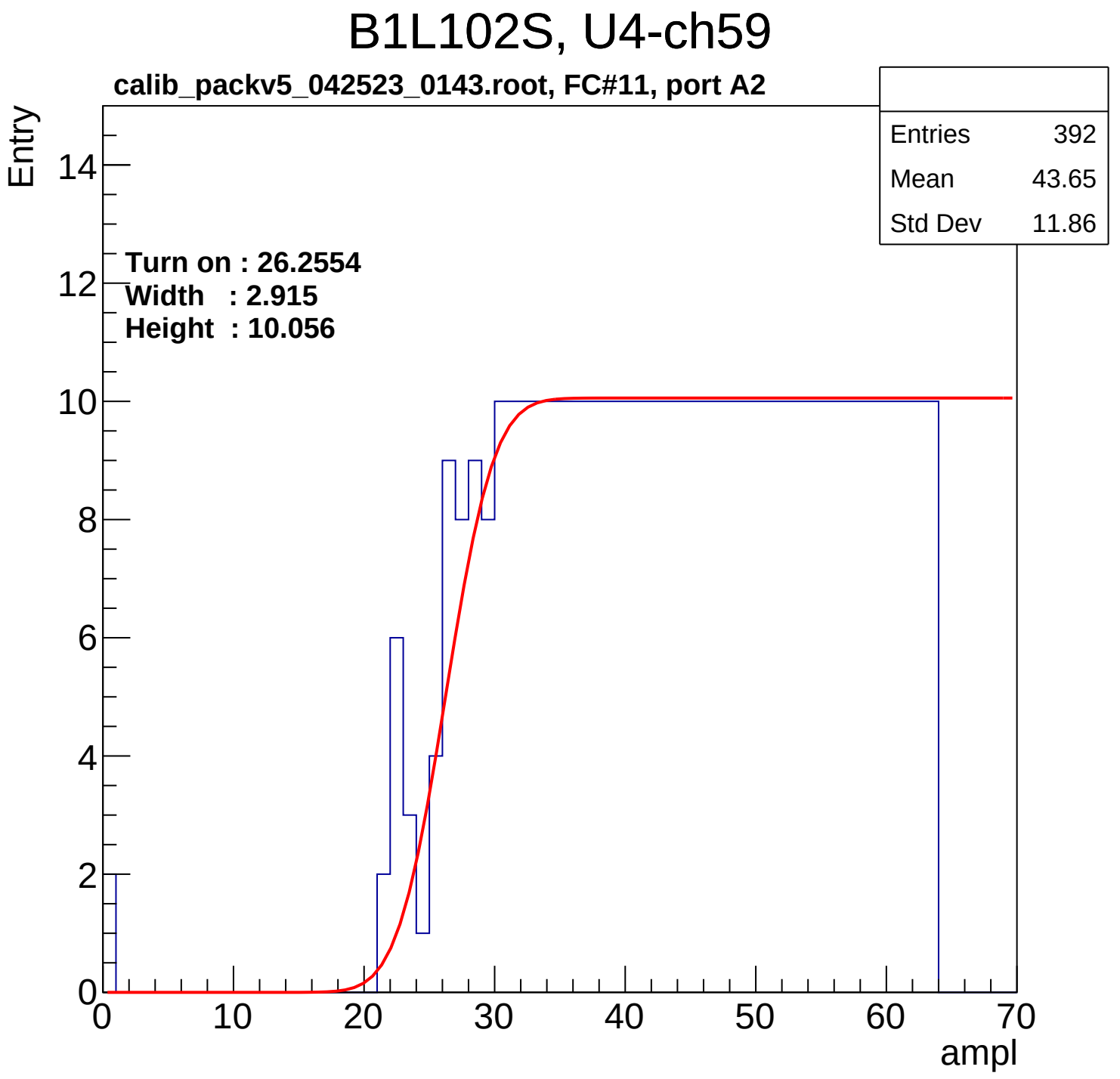
B1L102S, U4-ch59
calib_packv5_042523_0143.root, FC#11, port A2
Entries 392
Mean 43.65
Std Dev 11.86
Turn on : 26.2554
Width : 2.915
Height : 10.056
Entry
ampl
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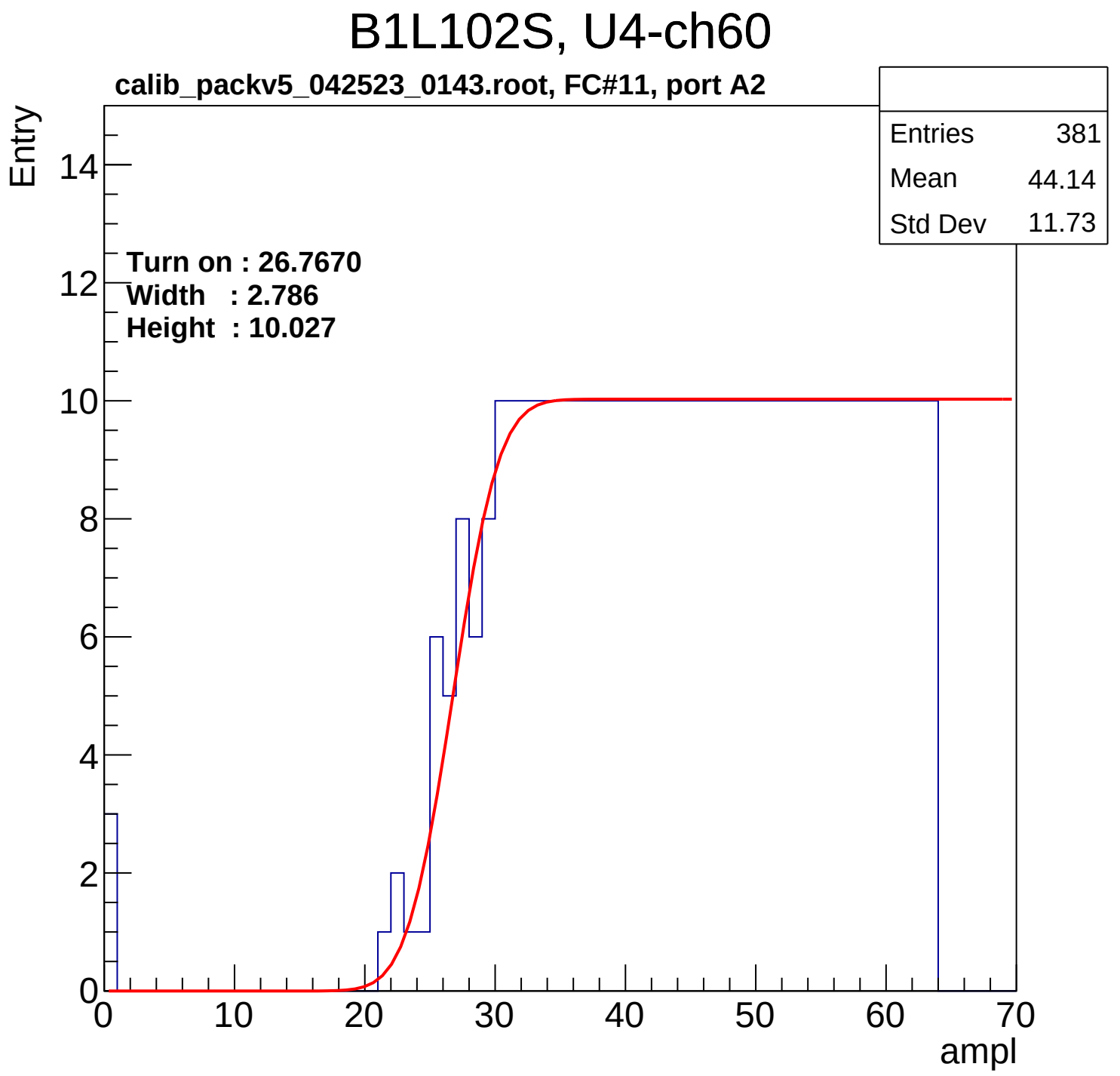
B1L102S, U4-ch60
calib_packv5_042523_0143.root, FC#11, port A2
Entries 381
Mean 44.14
Std Dev 11.73
Turn on : 26.7670
Width : 2.786
Height : 10.027
Entry
ampl
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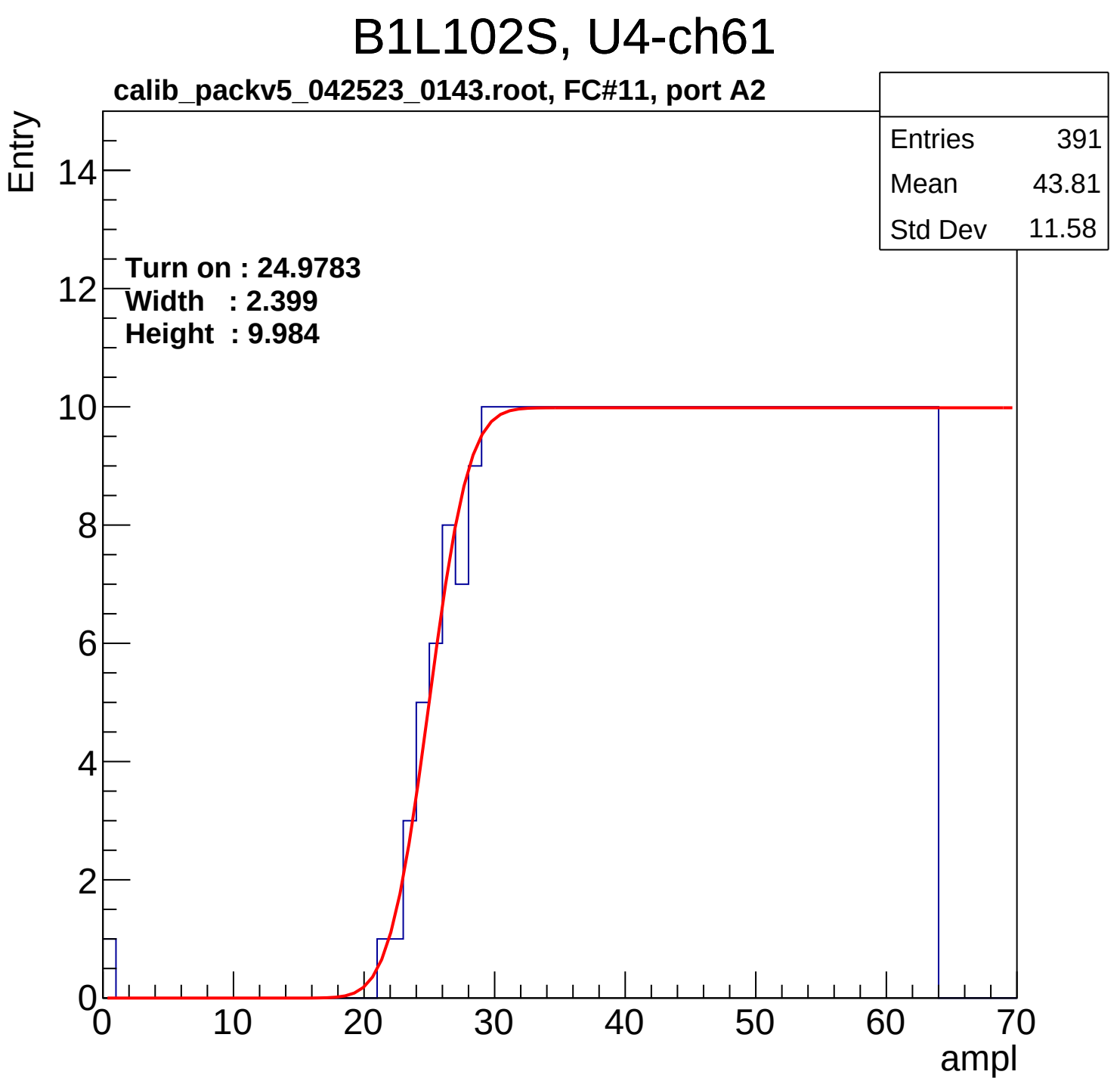
B1L102S, U4-ch61
calib_packv5_042523_0143.root, FC#11, port A2
Entries 391
Mean 43.81
Std Dev 11.58
Turn on : 24.9783
Width : 2.399
Height : 9.984
Entry
ampl
0
2
4
6
8
10
12
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0
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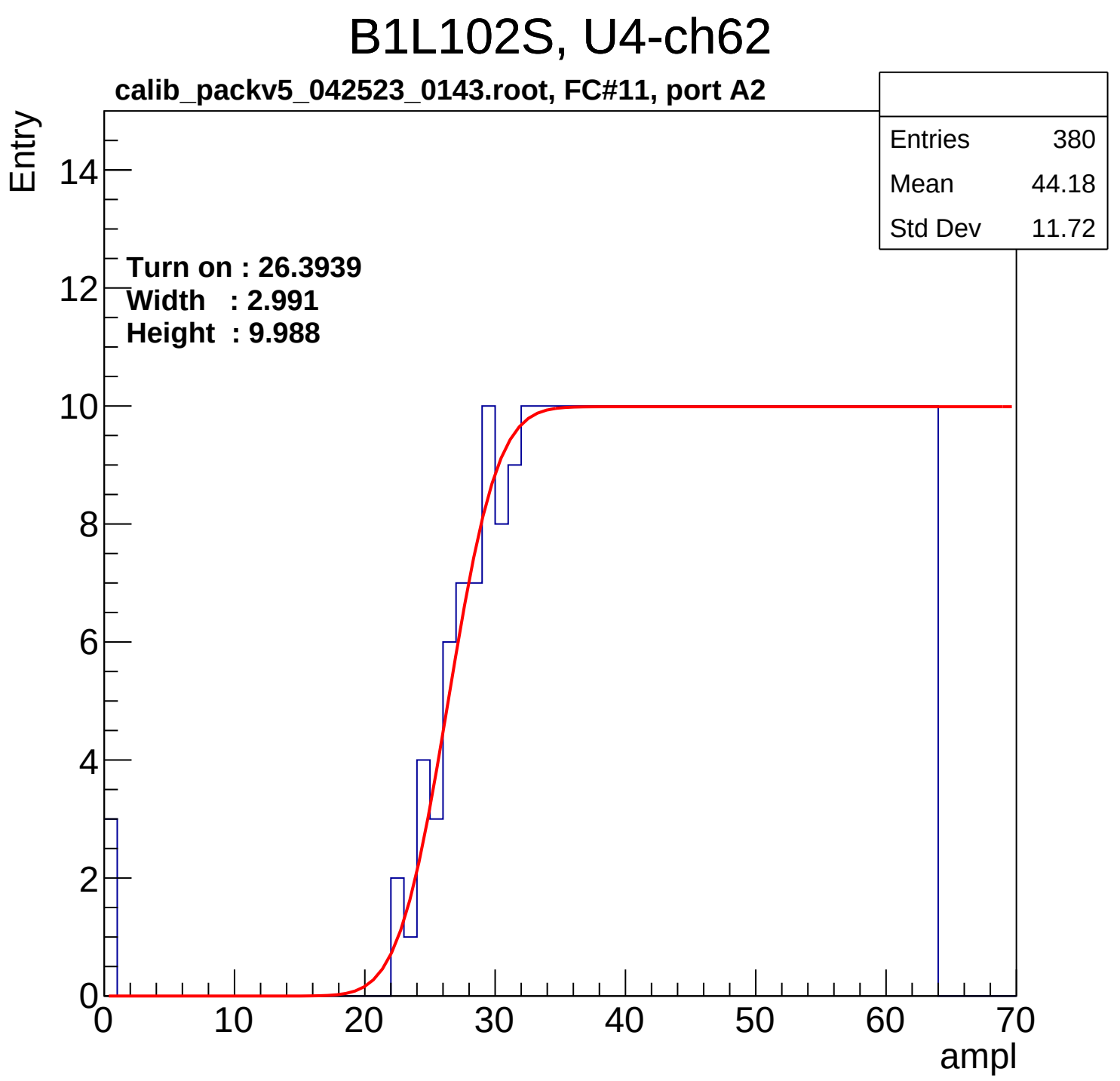
B1L102S, U4-ch62
calib_packv5_042523_0143.root, FC#11, port A2
Entries 380
Mean 44.18
Std Dev 11.72
Turn on : 26.3939
Width : 2.991
Height : 9.988
Entry
ampl
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2
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6
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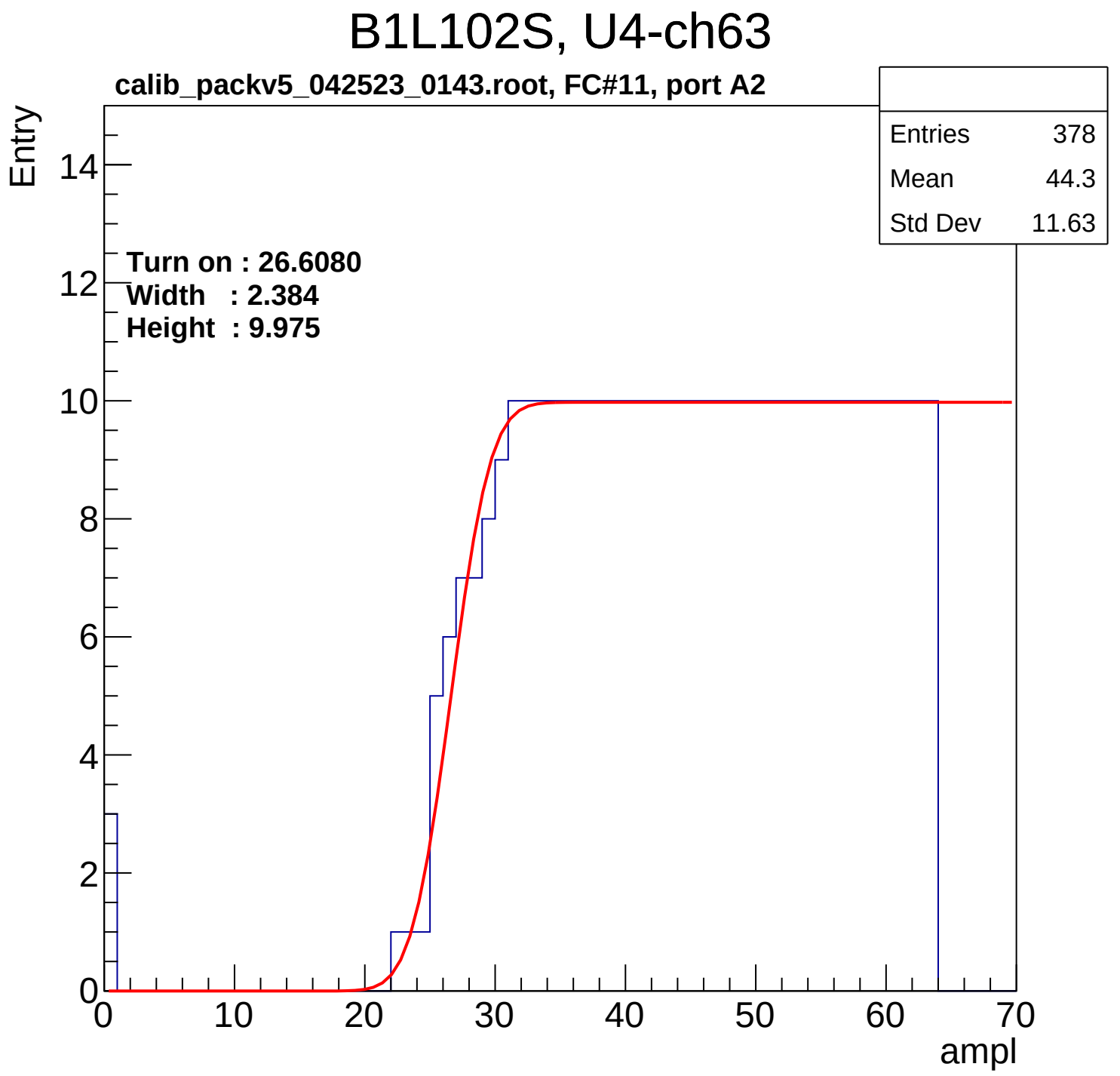
B1L102S, U4-ch63
calib_packv5_042523_0143.root, FC#11, port A2
Entries 378
Mean 44.3
Std Dev 11.63
Turn on : 26.6080
Width : 2.384
Height : 9.975
Entry
ampl
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2
4
6
8
10
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0
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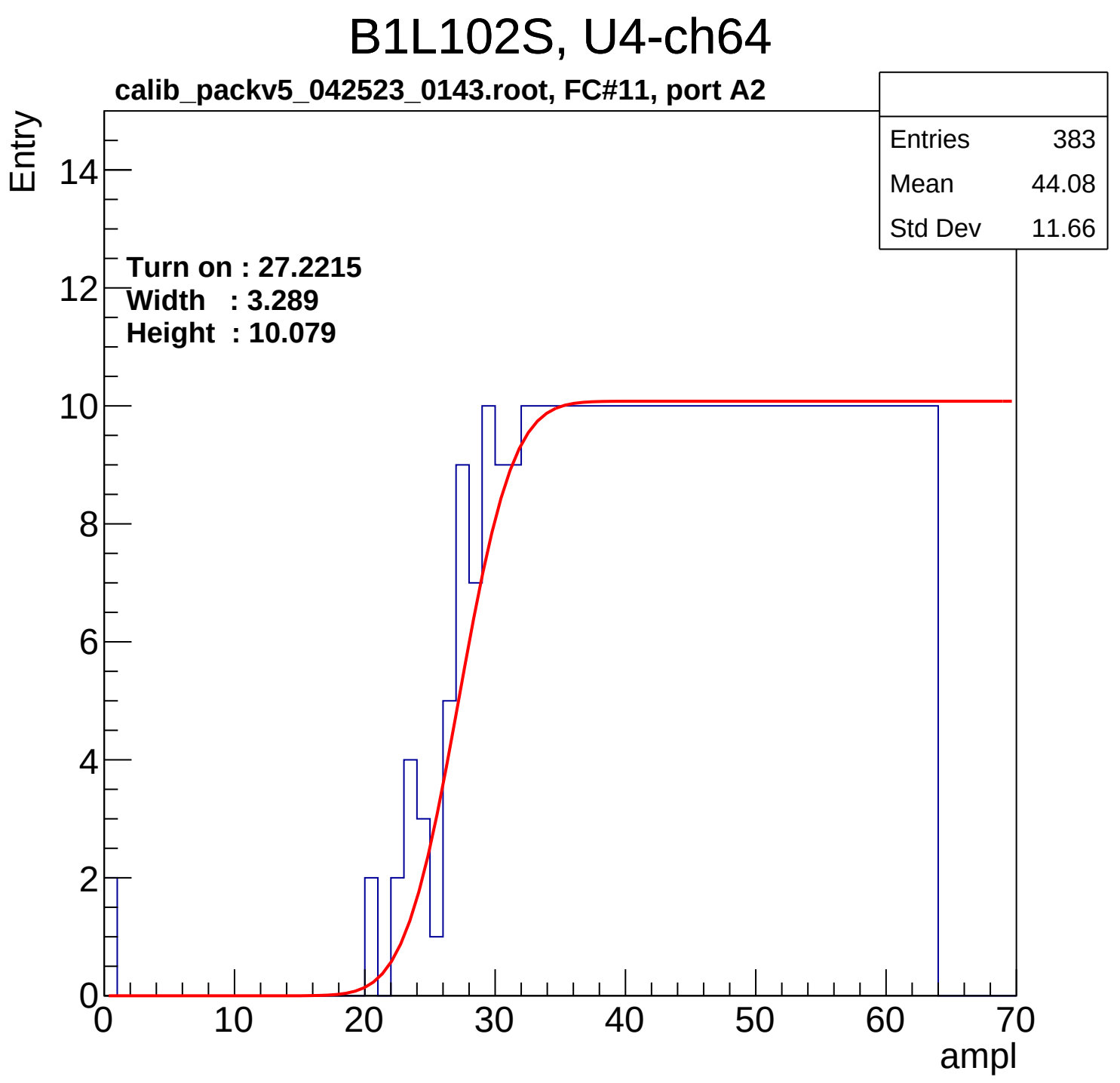
B1L102S, U4-ch64
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 44.08
Std Dev 11.66
Turn on : 27.2215
Width : 3.289
Height : 10.079
Entry
ampl
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6
8
10
12
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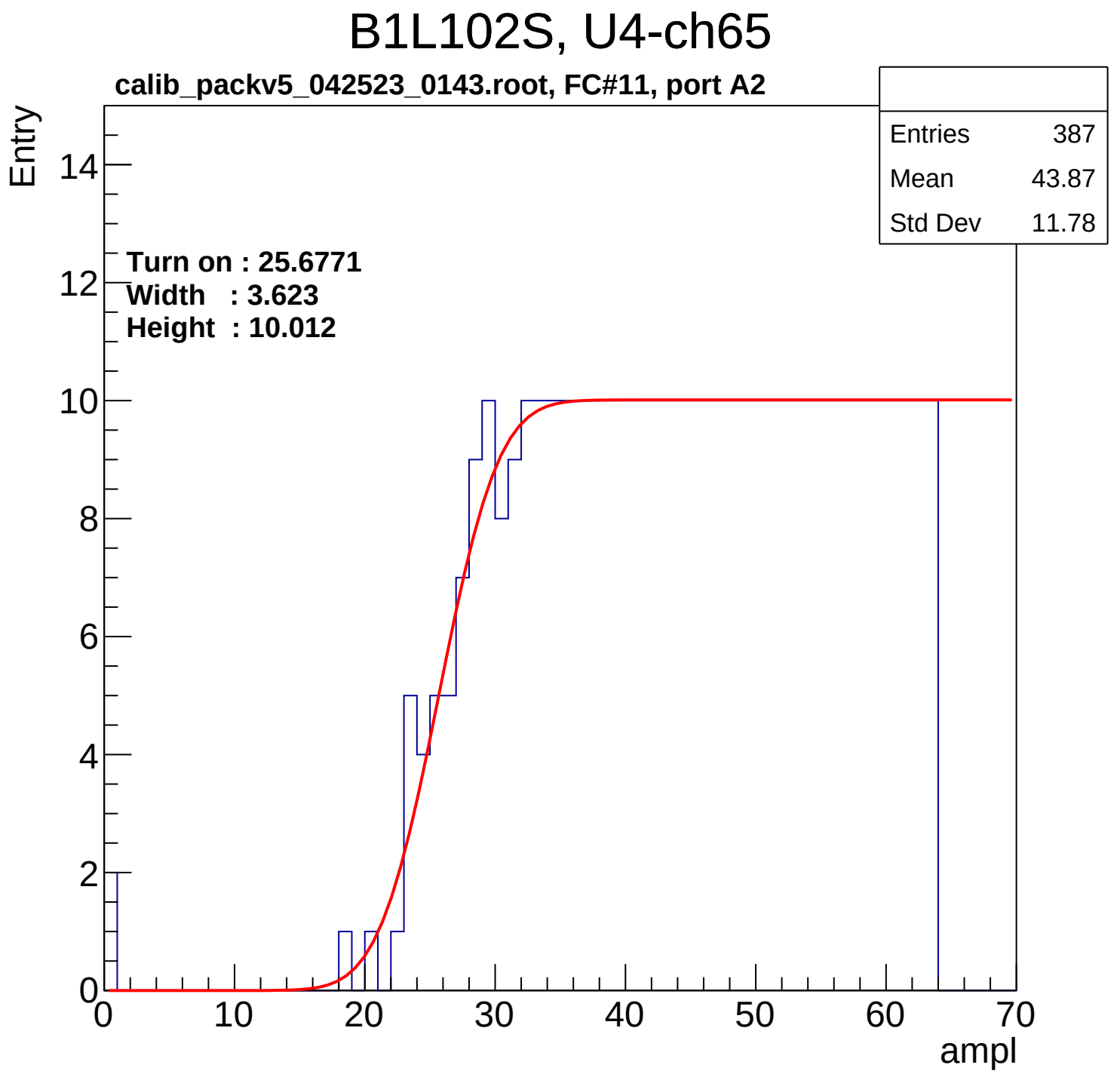
B1L102S, U4-ch65
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 43.87
Std Dev 11.78
Turn on : 25.6771
Width : 3.623
Height : 10.012
Entry
ampl
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4
6
8
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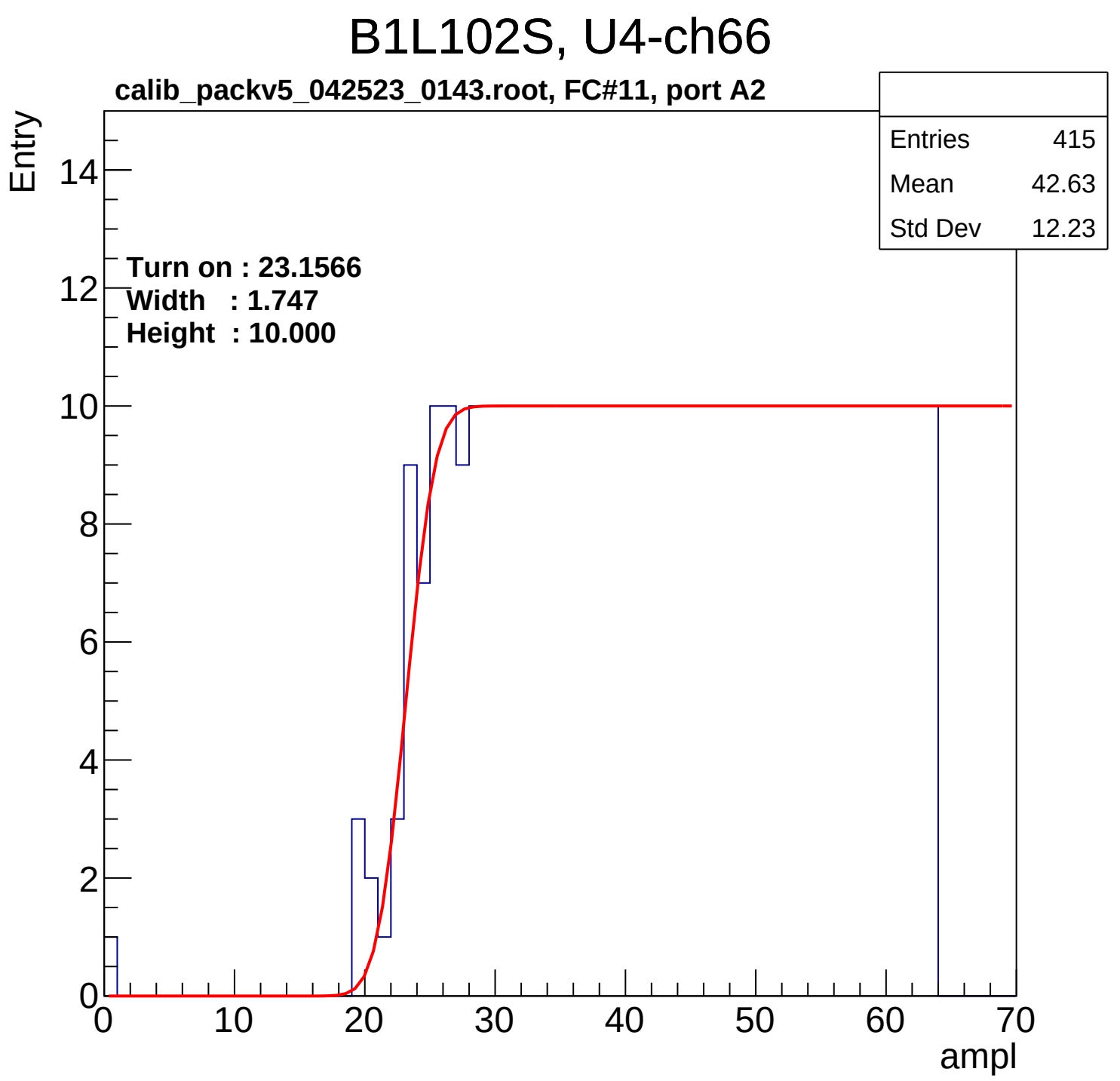
B1L102S, U4-ch66
calib_packv5_042523_0143.root, FC#11, port A2
Entries 415
Mean 42.63
Std Dev 12.23
Turn on : 23.1566
Width : 1.747
Height : 10.000
Entry
ampl
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4
6
8
10
12
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0
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60
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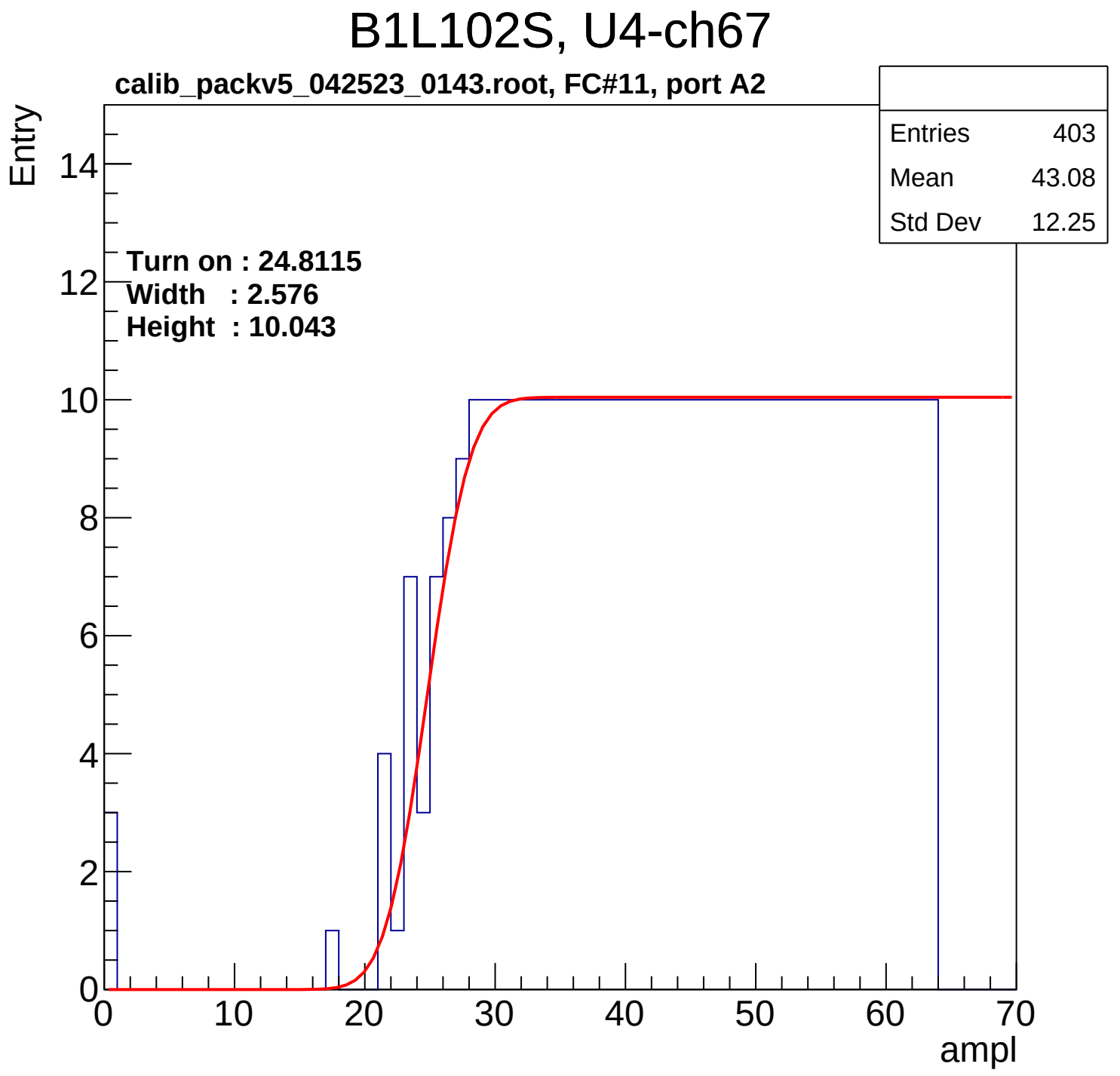
B1L102S, U4-ch67
calib_packv5_042523_0143.root, FC#11, port A2
Entries 403
Mean 43.08
Std Dev 12.25
Turn on : 24.8115
Width : 2.576
Height : 10.043
Entry
ampl
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4
6
8
10
12
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0
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20
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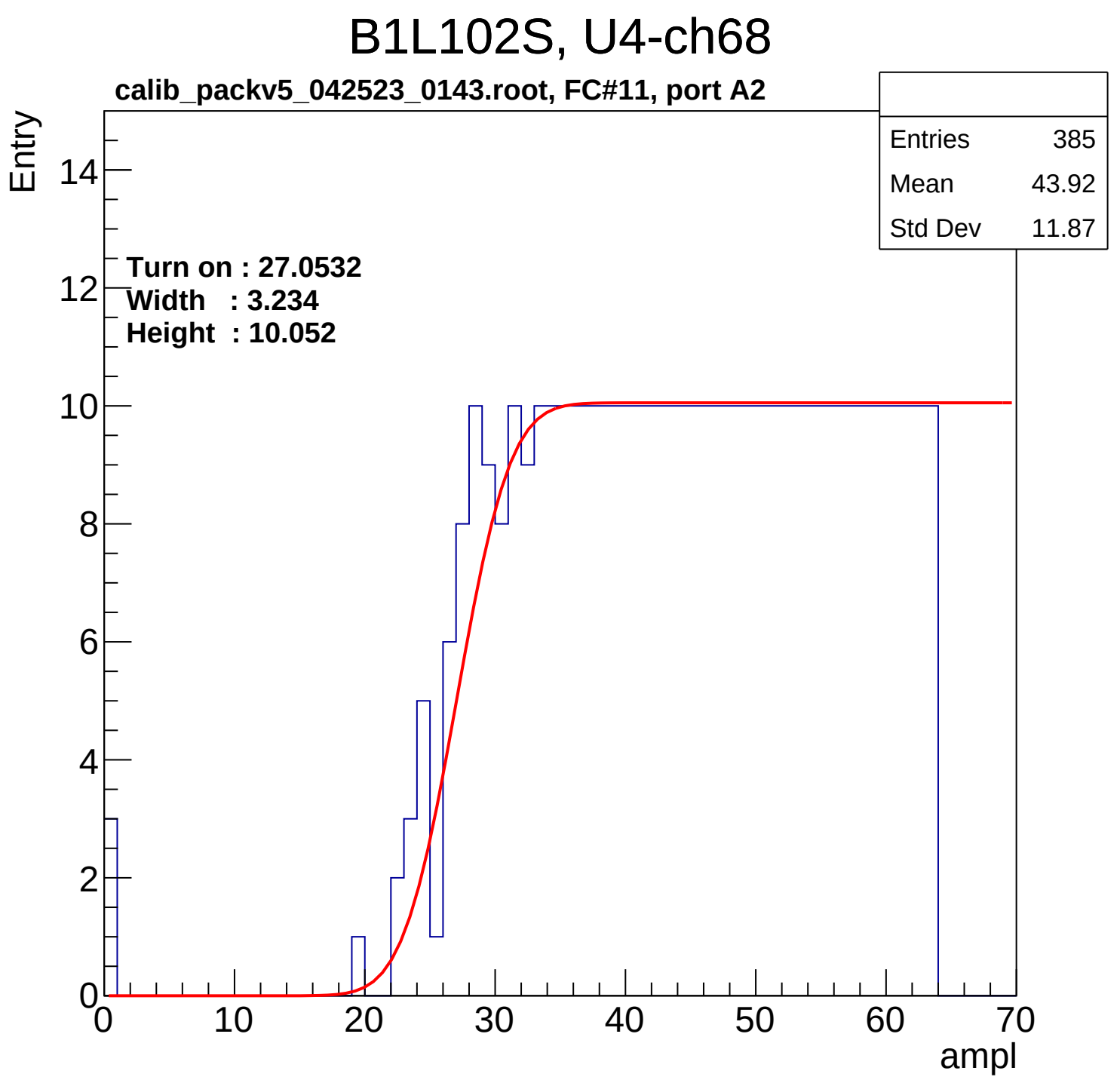
B1L102S, U4-ch68
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 43.92
Std Dev 11.87
Turn on : 27.0532
Width : 3.234
Height : 10.052
Entry
ampl
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4
6
8
10
12
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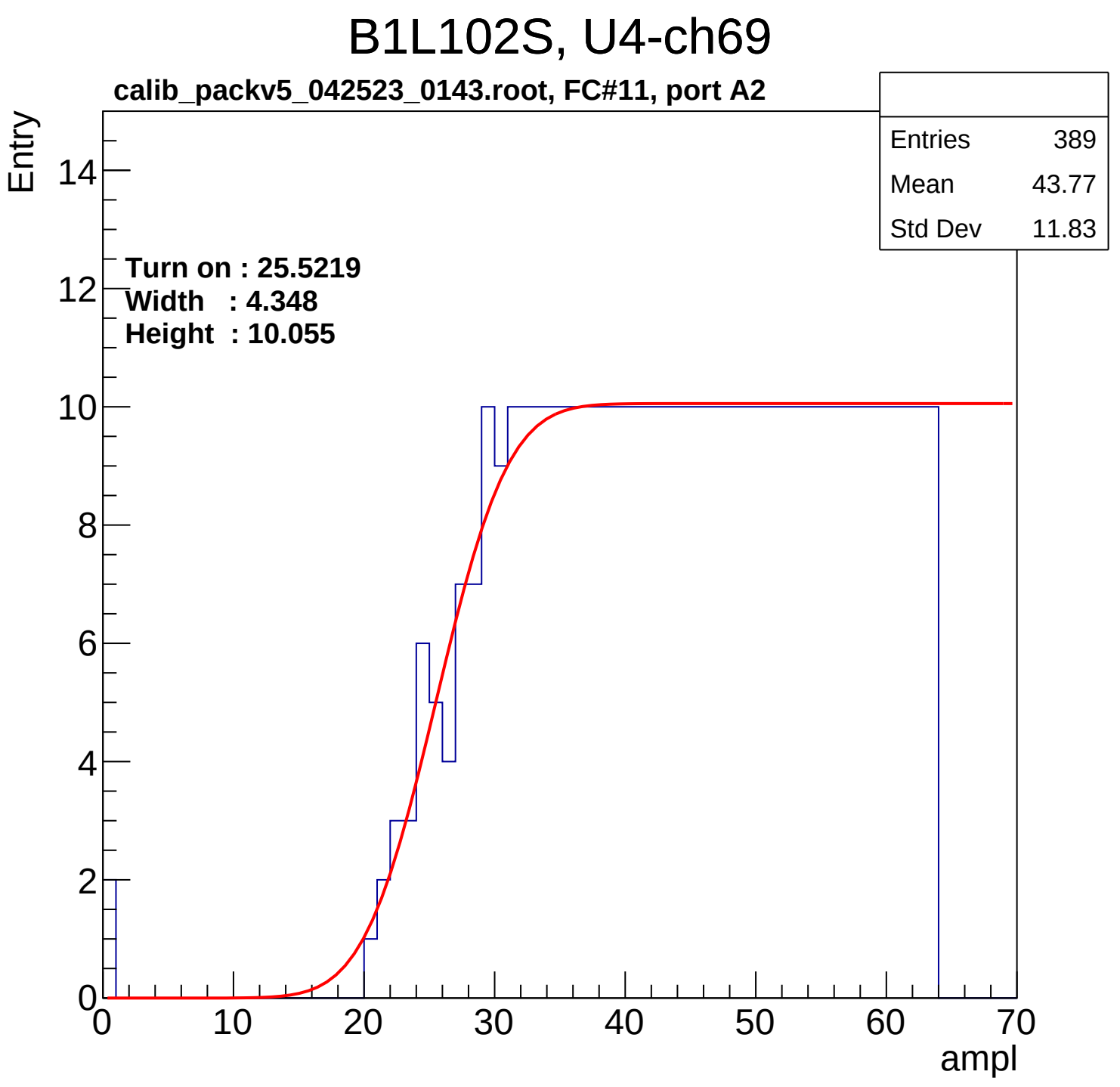
B1L102S, U4-ch69
calib_packv5_042523_0143.root, FC#11, port A2
Entries 389
Mean 43.77
Std Dev 11.83
Turn on : 25.5219
Width : 4.348
Height : 10.055
Entry
ampl
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2
4
6
8
10
12
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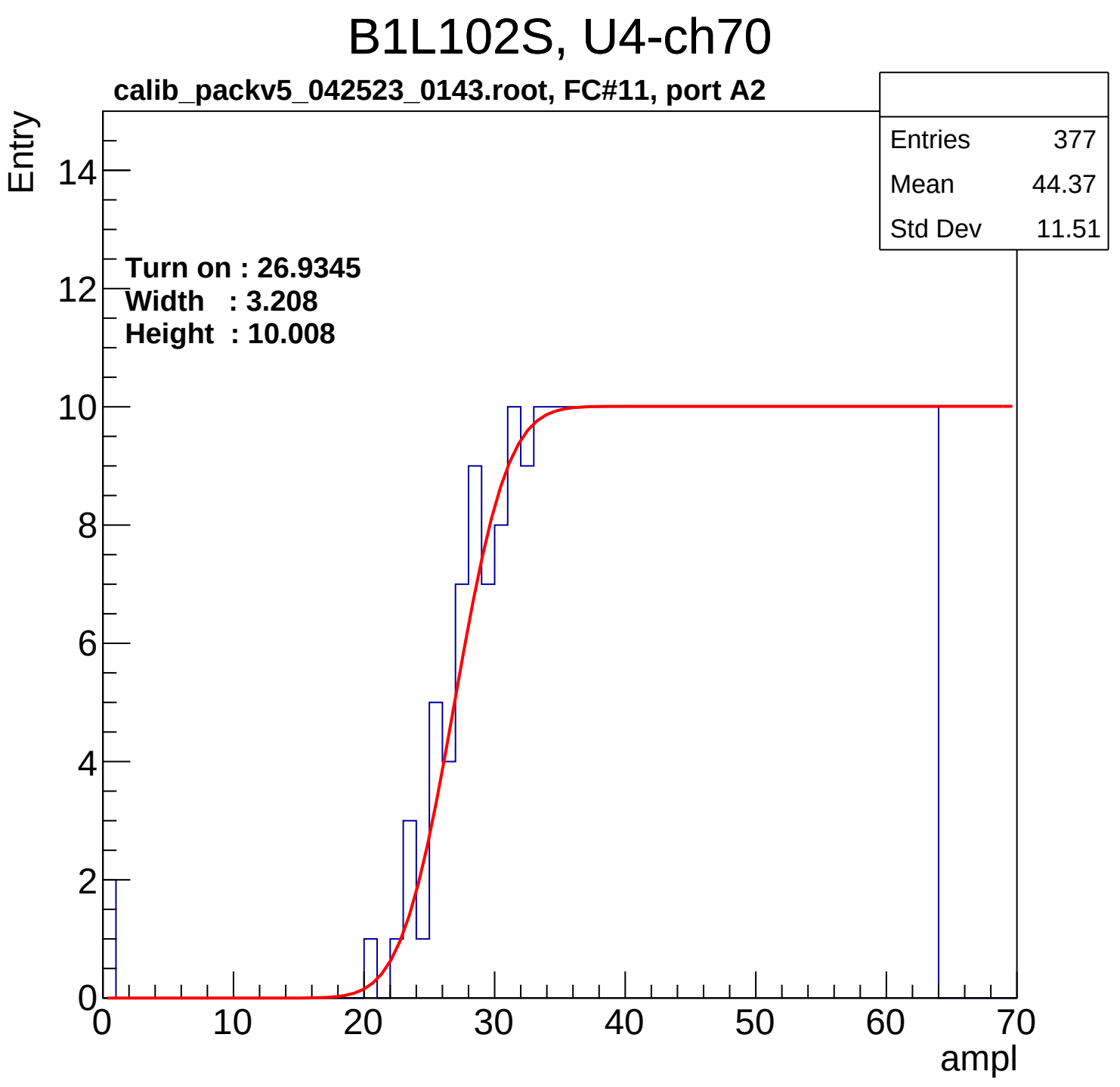
B1L102S, U4-ch70
calib_packv5_042523_0143.root, FC#11, port A2
Entries 377
Mean 44.37
Std Dev 11.51
Turn on : 26.9345
Width : 3.208
Height : 10.008
Entry
ampl
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2
4
6
8
10
12
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0
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20
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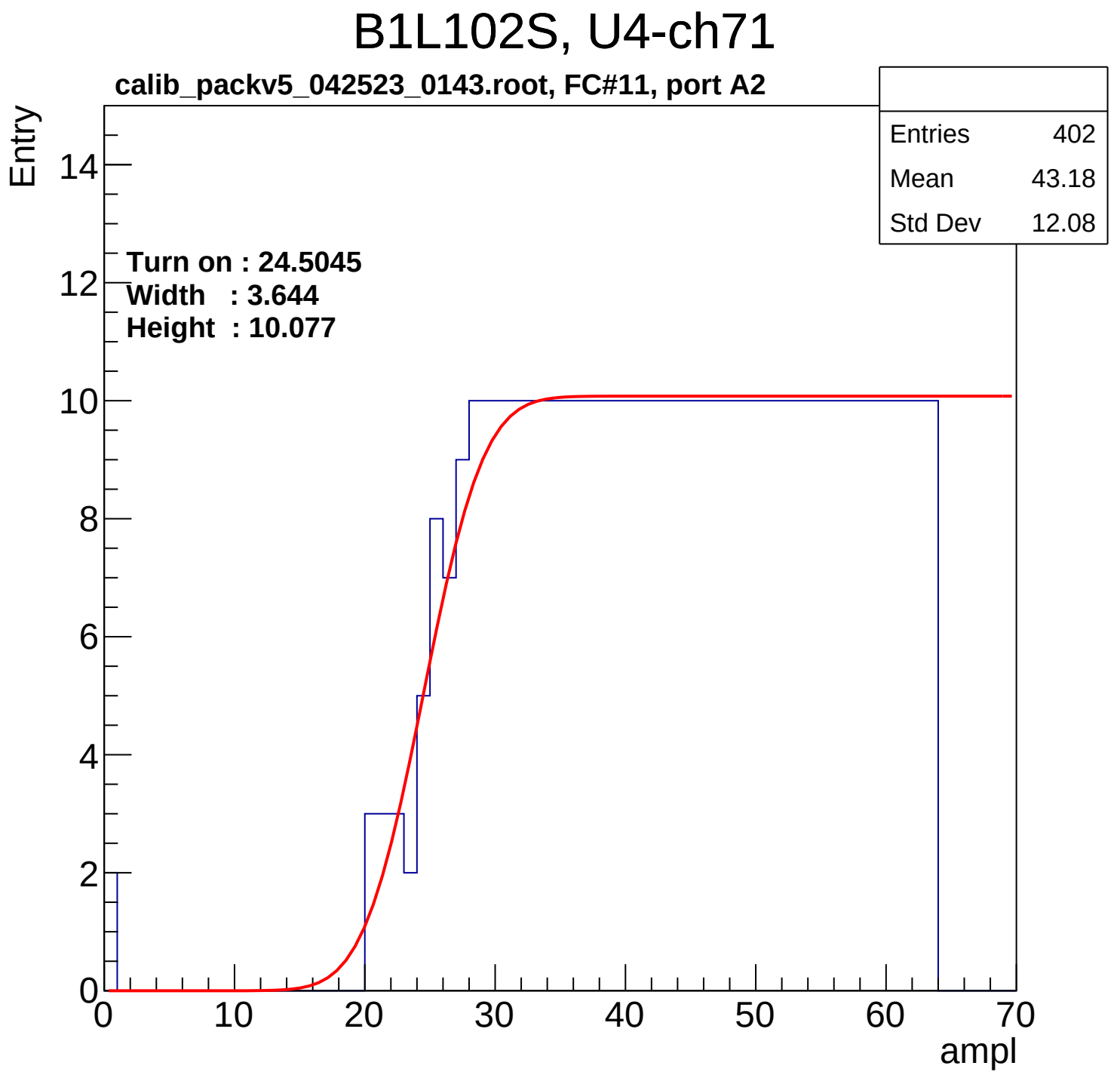
B1L102S, U4-ch71
calib_packv5_042523_0143.root, FC#11, port A2
Entries 402
Mean 43.18
Std Dev 12.08
Turn on : 24.5045
Width : 3.644
Height : 10.077
Entry
ampl
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6
8
10
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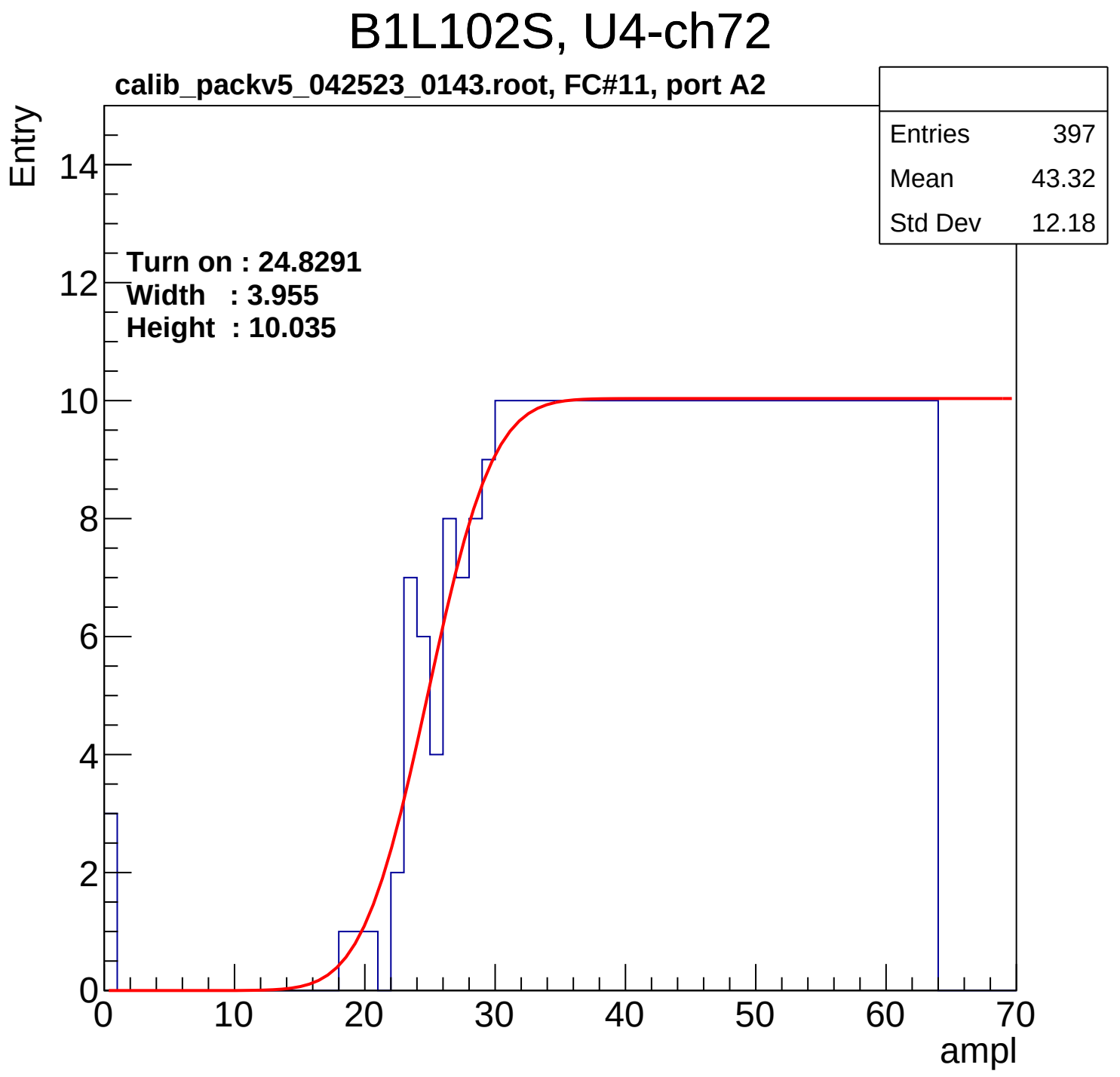
B1L102S, U4-ch72
calib_packv5_042523_0143.root, FC#11, port A2
Entries 397
Mean 43.32
Std Dev 12.18
Turn on : 24.8291
Width : 3.955
Height : 10.035
Entry
ampl
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6
8
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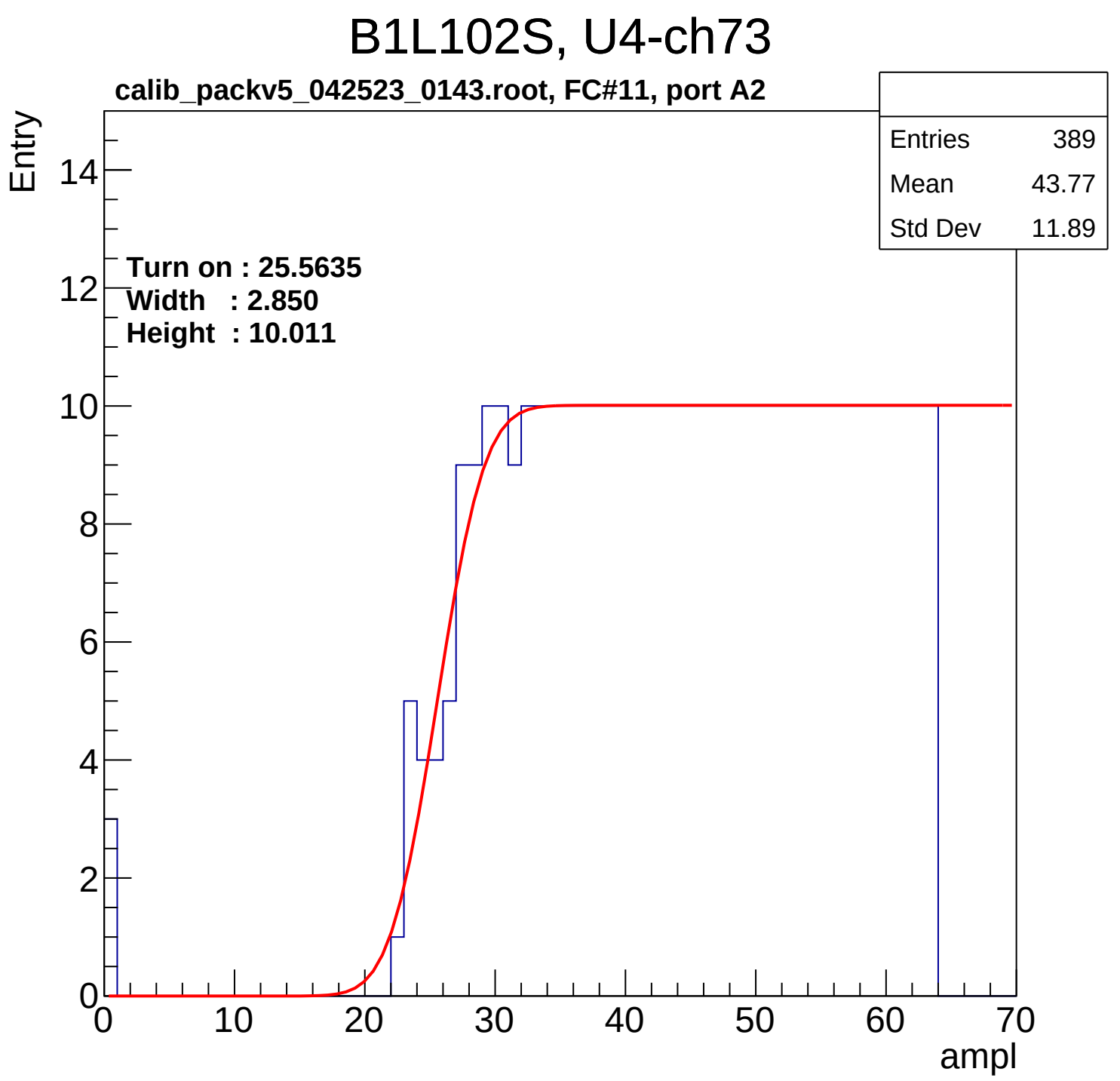
B1L102S, U4-ch73
calib_packv5_042523_0143.root, FC#11, port A2
Entries 389
Mean 43.77
Std Dev 11.89
Turn on : 25.5635
Width : 2.850
Height : 10.011
Entry
ampl
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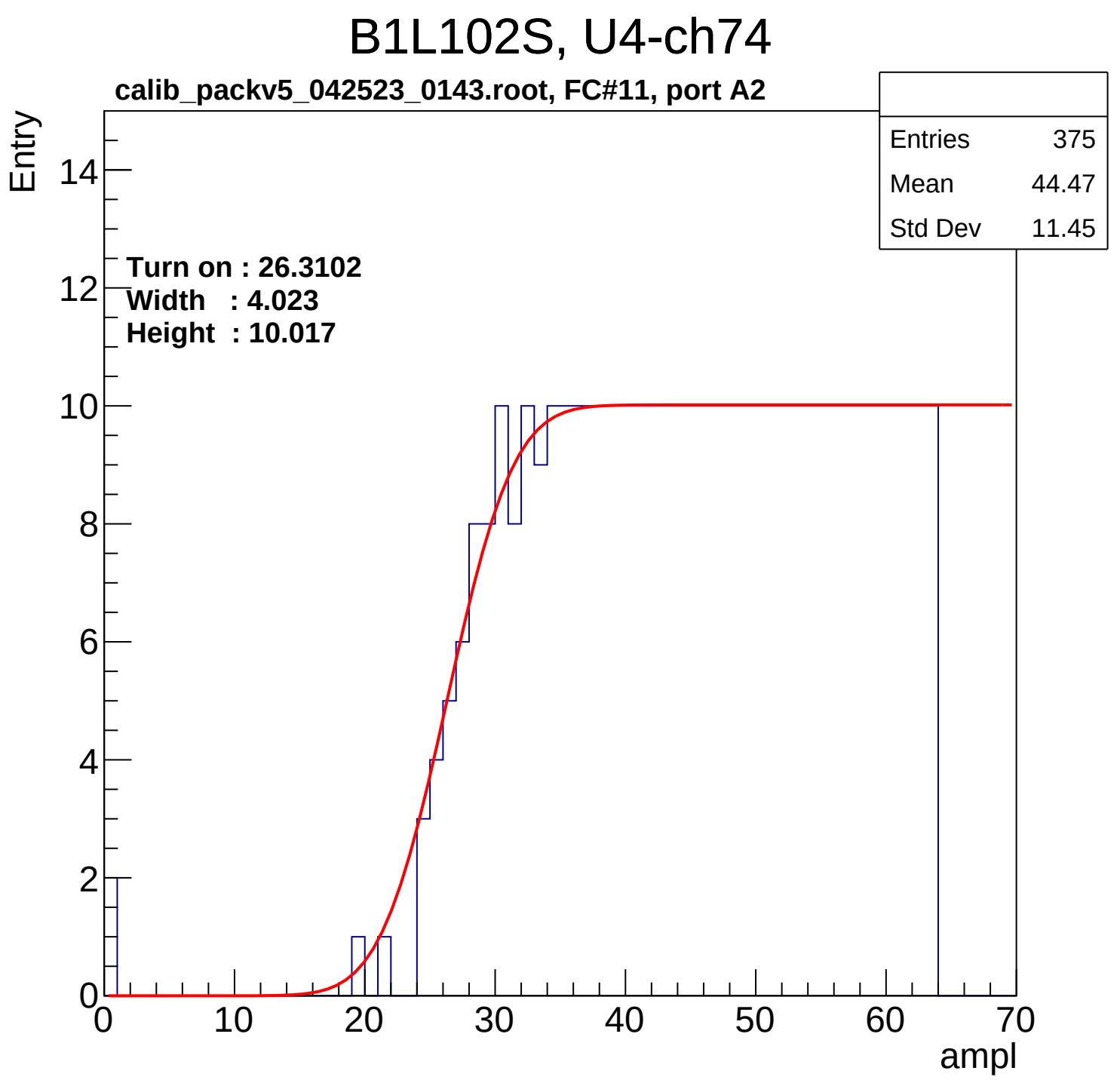
B1L102S, U4-ch74
calib_packv5_042523_0143.root, FC#11, port A2
Entries 375
Mean 44.47
Std Dev 11.45
Turn on : 26.3102
Width : 4.023
Height : 10.017
Entry
ampl
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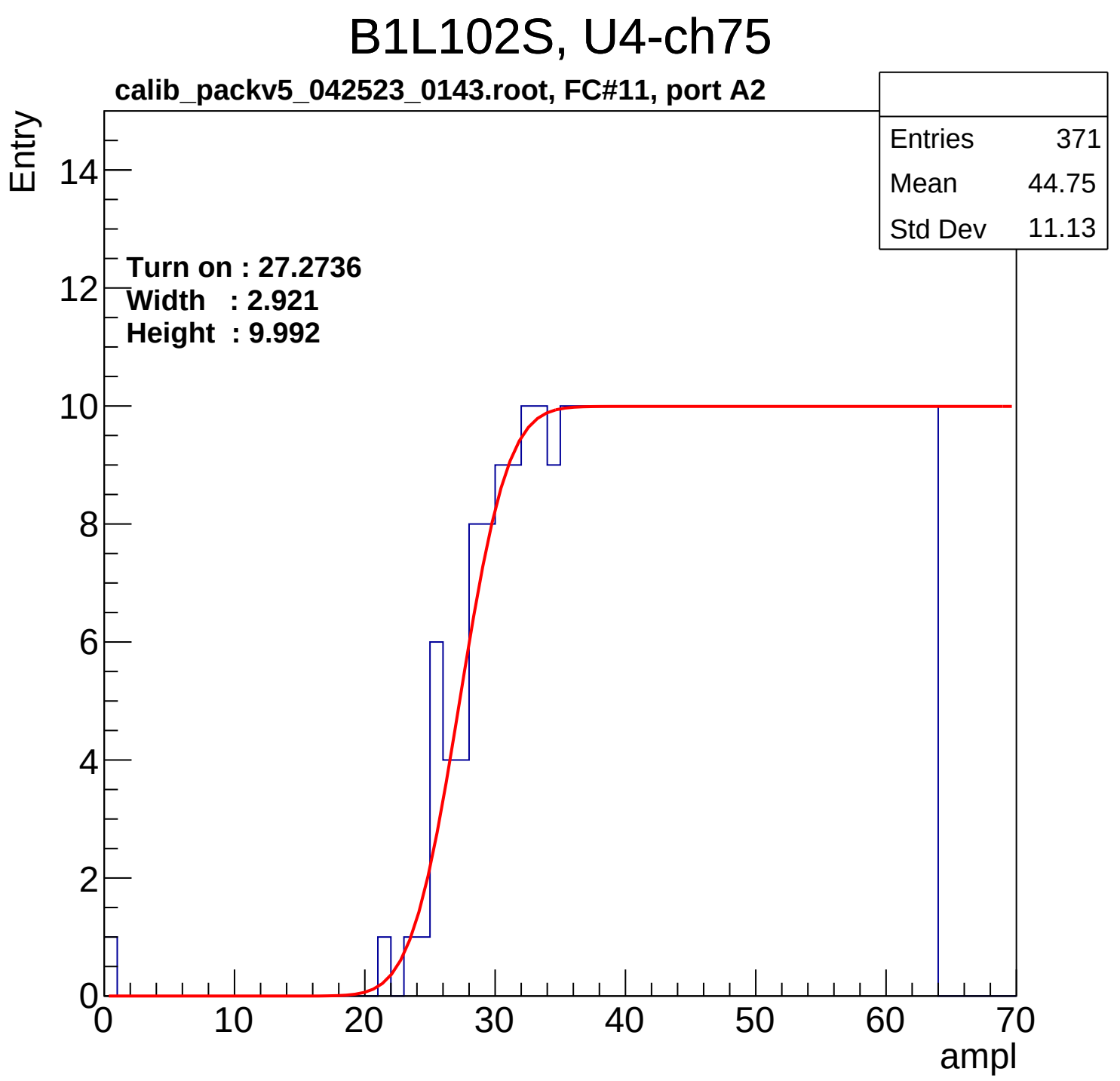
B1L102S, U4-ch75
calib_packv5_042523_0143.root, FC#11, port A2
Entries 371
Mean 44.75
Std Dev 11.13
Turn on : 27.2736
Width : 2.921
Height : 9.992
Entry
ampl
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2
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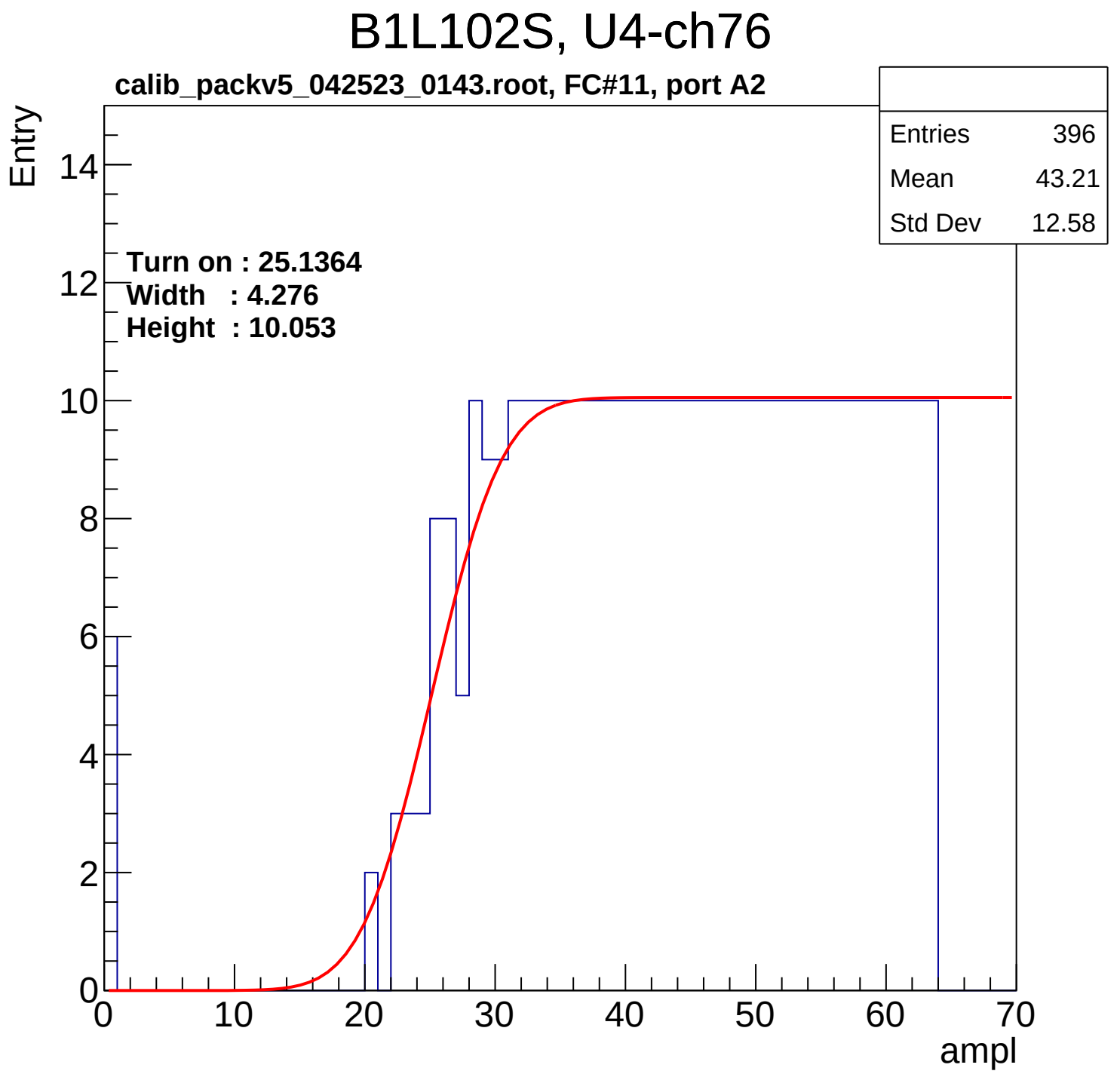
B1L102S, U4-ch76
calib_packv5_042523_0143.root, FC#11, port A2
Entries 396
Mean 43.21
Std Dev 12.58
Turn on : 25.1364
Width : 4.276
Height : 10.053
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ampl
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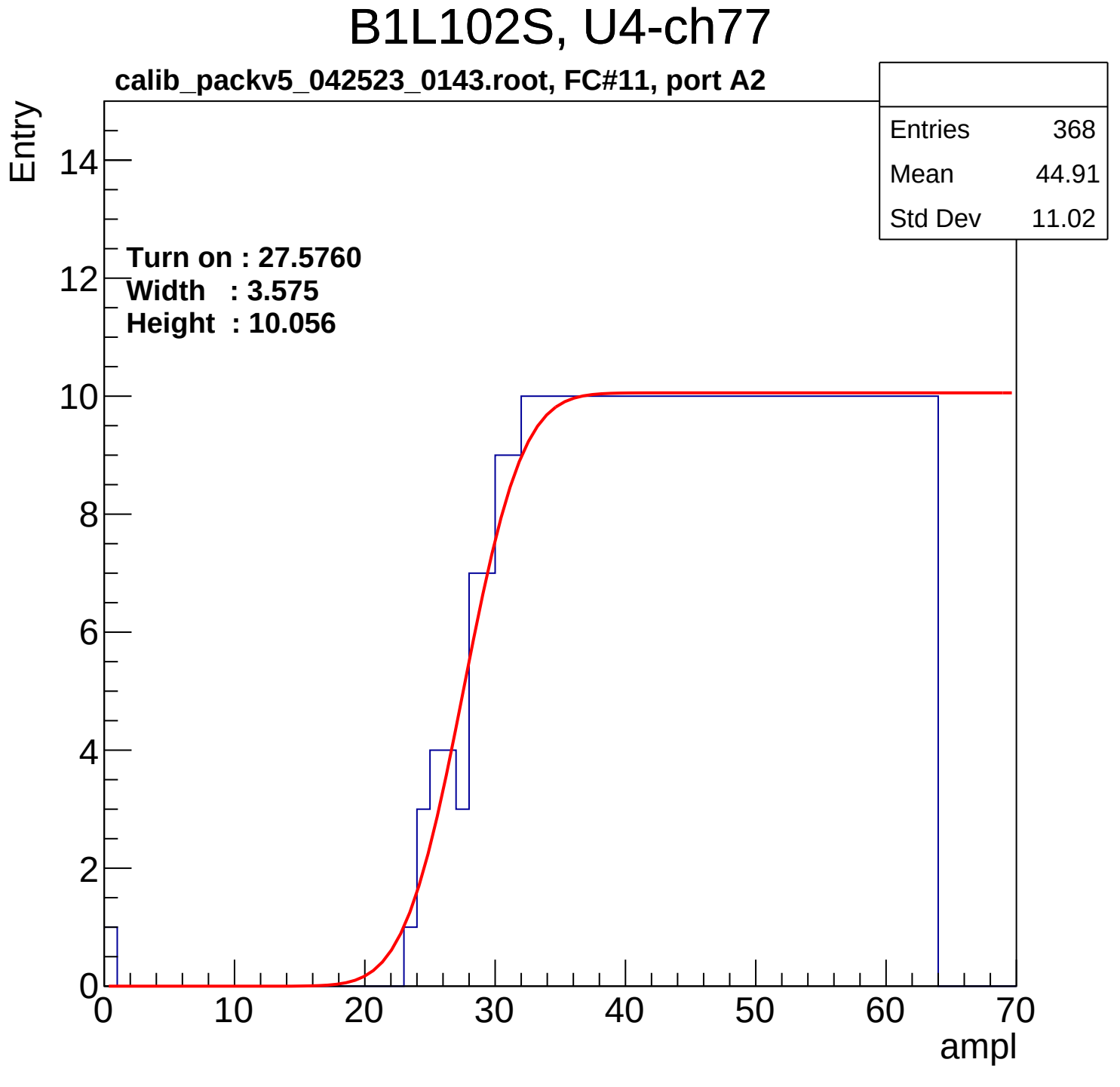
B1L102S, U4-ch77
calib_packv5_042523_0143.root, FC#11, port A2
Entries 368
Mean 44.91
Std Dev 11.02
Turn on : 27.5760
Width : 3.575
Height : 10.056
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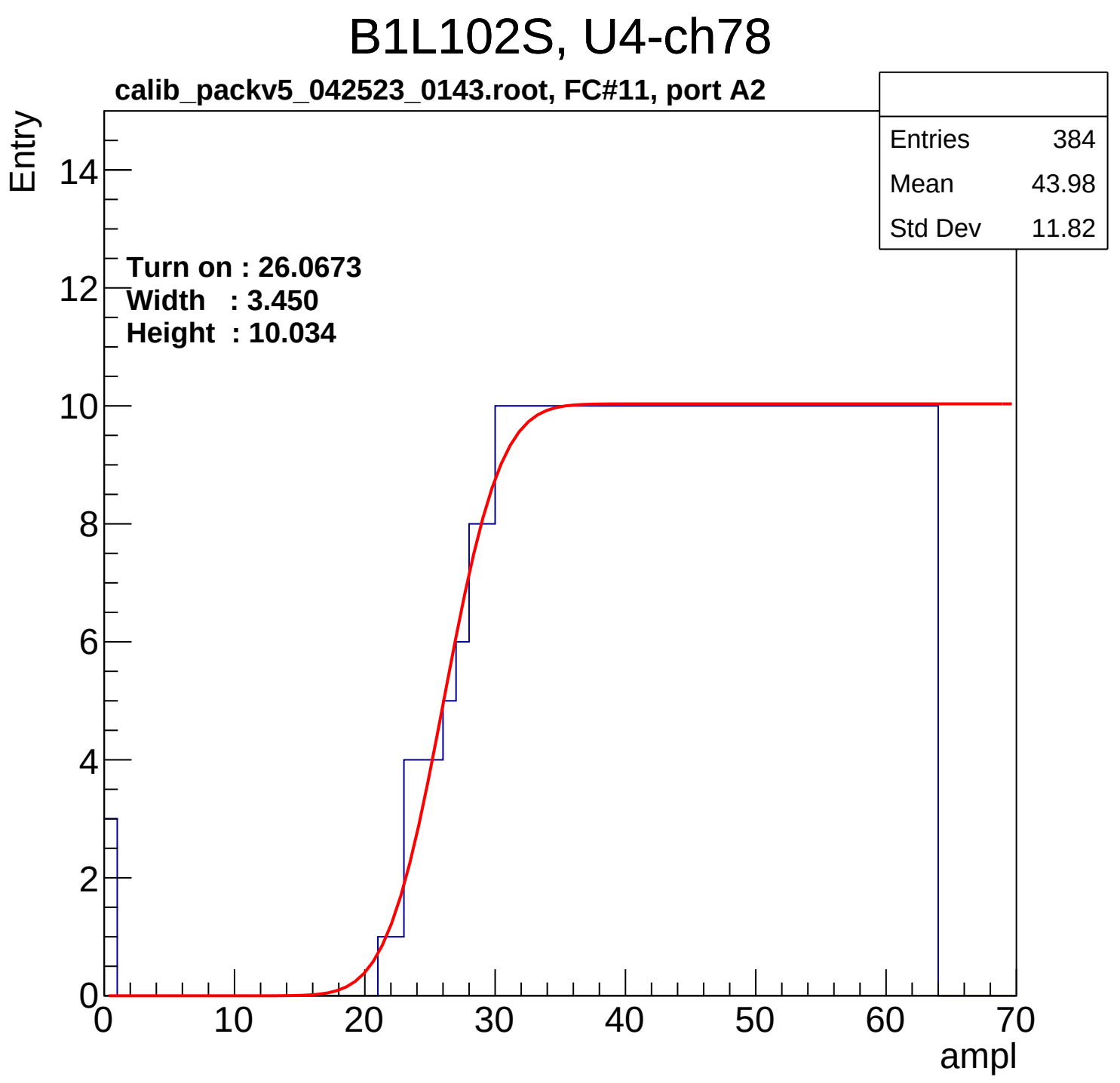
B1L102S, U4-ch78
calib_packv5_042523_0143.root, FC#11, port A2
Entries 384
Mean 43.98
Std Dev 11.82
Turn on : 26.0673
Width : 3.450
Height : 10.034
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ampl
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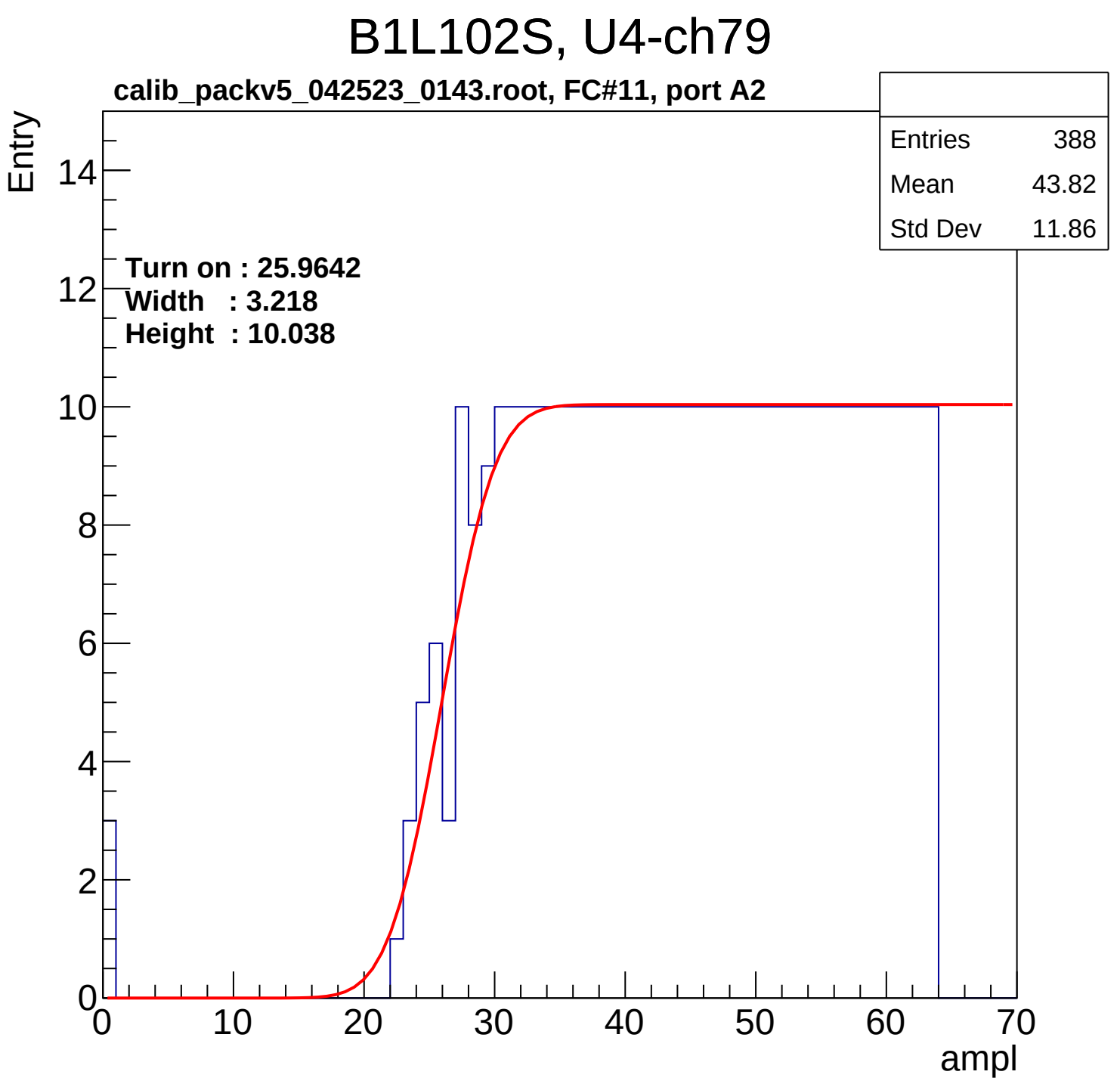
B1L102S, U4-ch79
calib_packv5_042523_0143.root, FC#11, port A2
Entries 388
Mean 43.82
Std Dev 11.86
Turn on : 25.9642
Width : 3.218
Height : 10.038
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ampl
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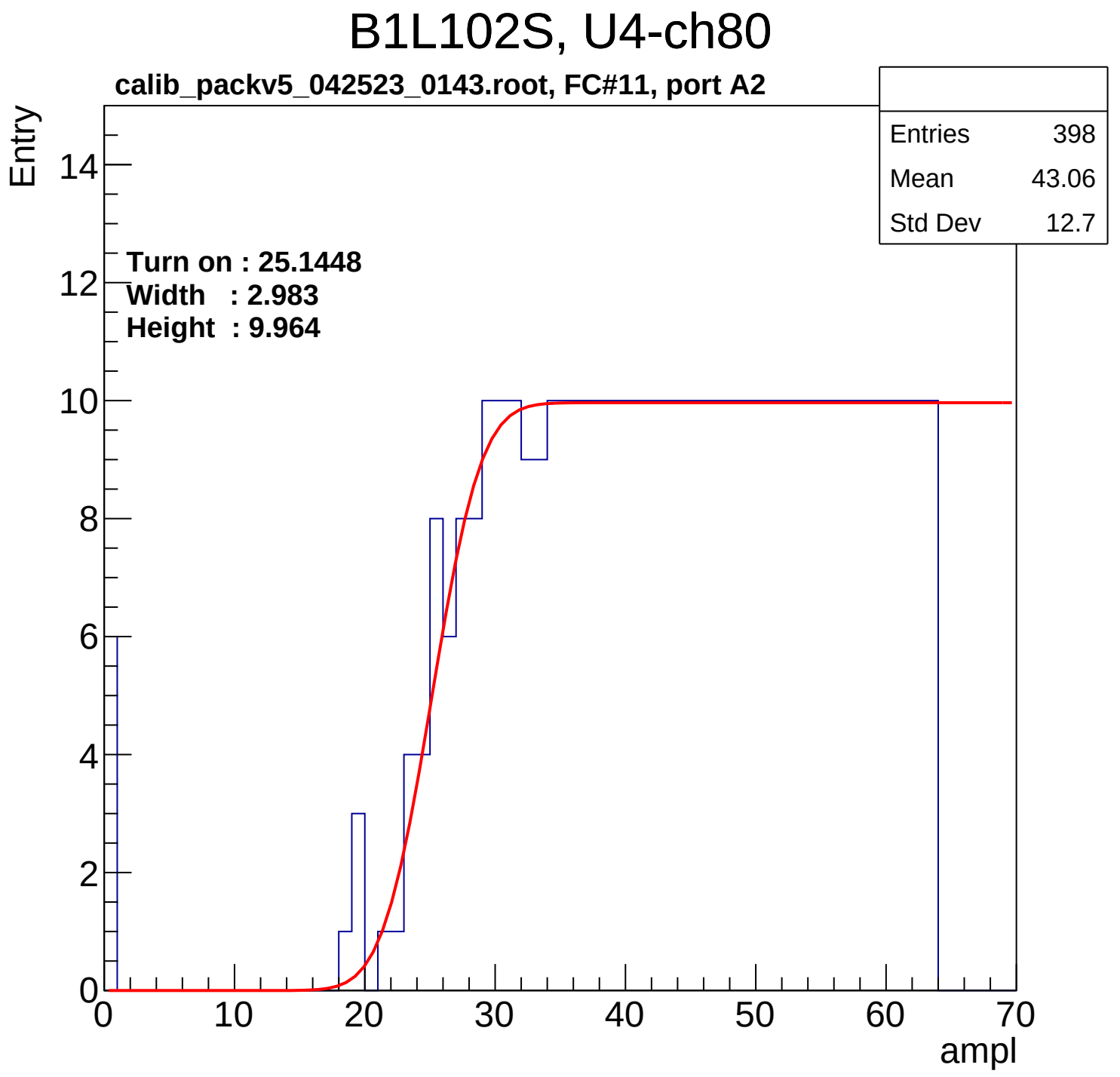
B1L102S, U4-ch80
calib_packv5_042523_0143.root, FC#11, port A2
Entries 398
Mean 43.06
Std Dev 12.7
Turn on : 25.1448
Width : 2.983
Height : 9.964
Entry
ampl
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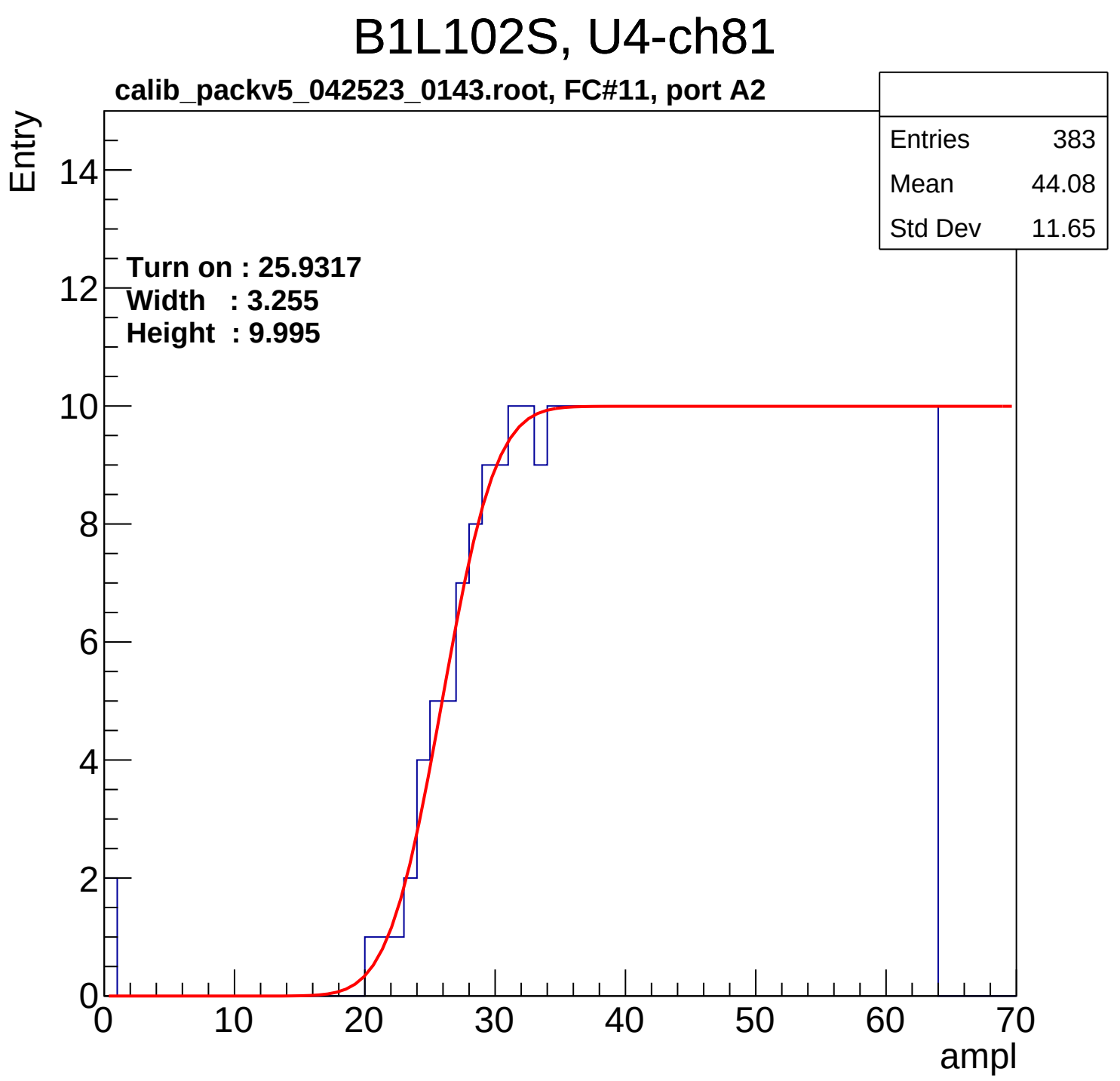
B1L102S, U4-ch81
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 44.08
Std Dev 11.65
Turn on : 25.9317
Width : 3.255
Height : 9.995
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ampl
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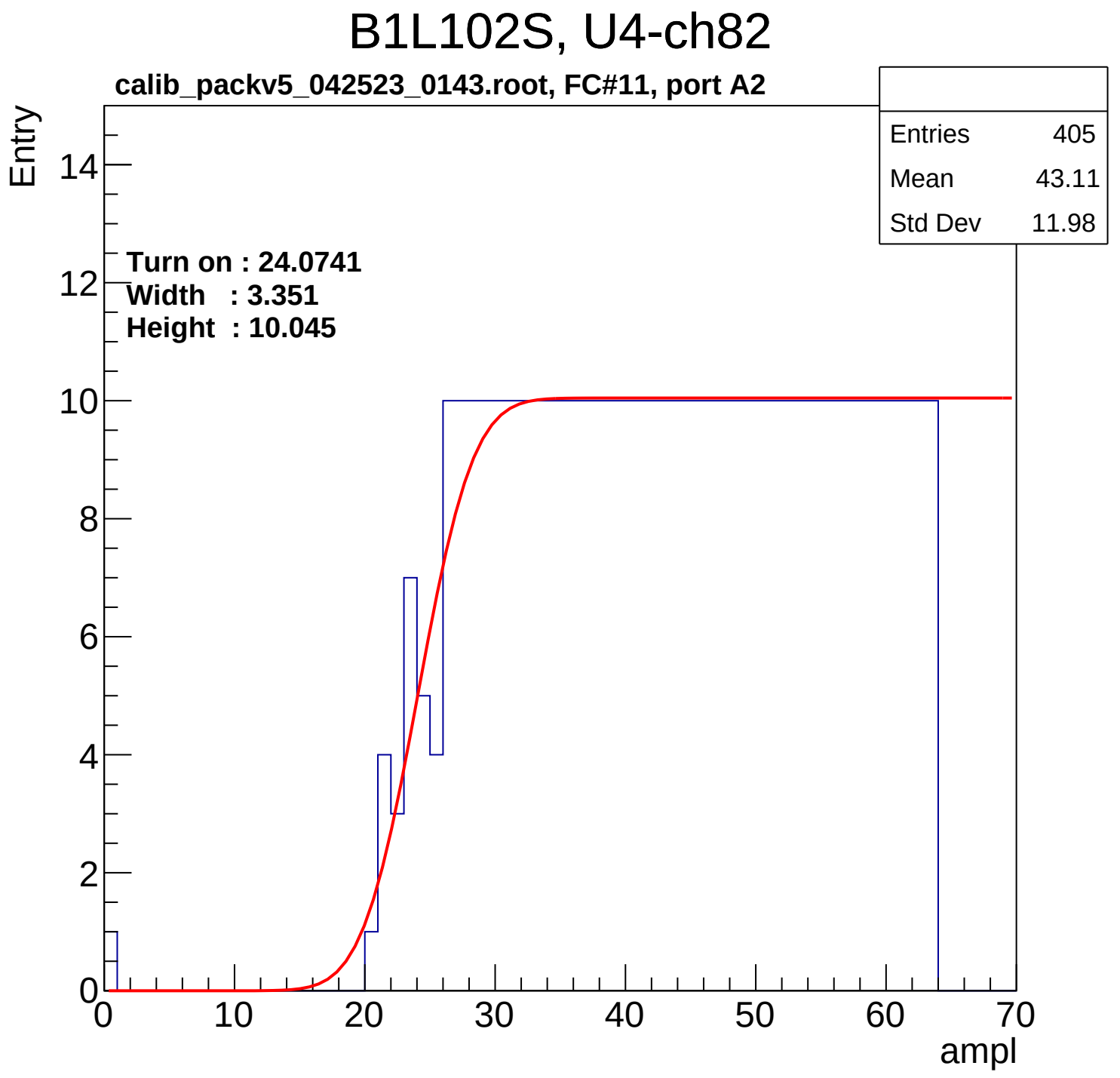
B1L102S, U4-ch82
calib_packv5_042523_0143.root, FC#11, port A2
Entries 405
Mean 43.11
Std Dev 11.98
Turn on : 24.0741
Width : 3.351
Height : 10.045
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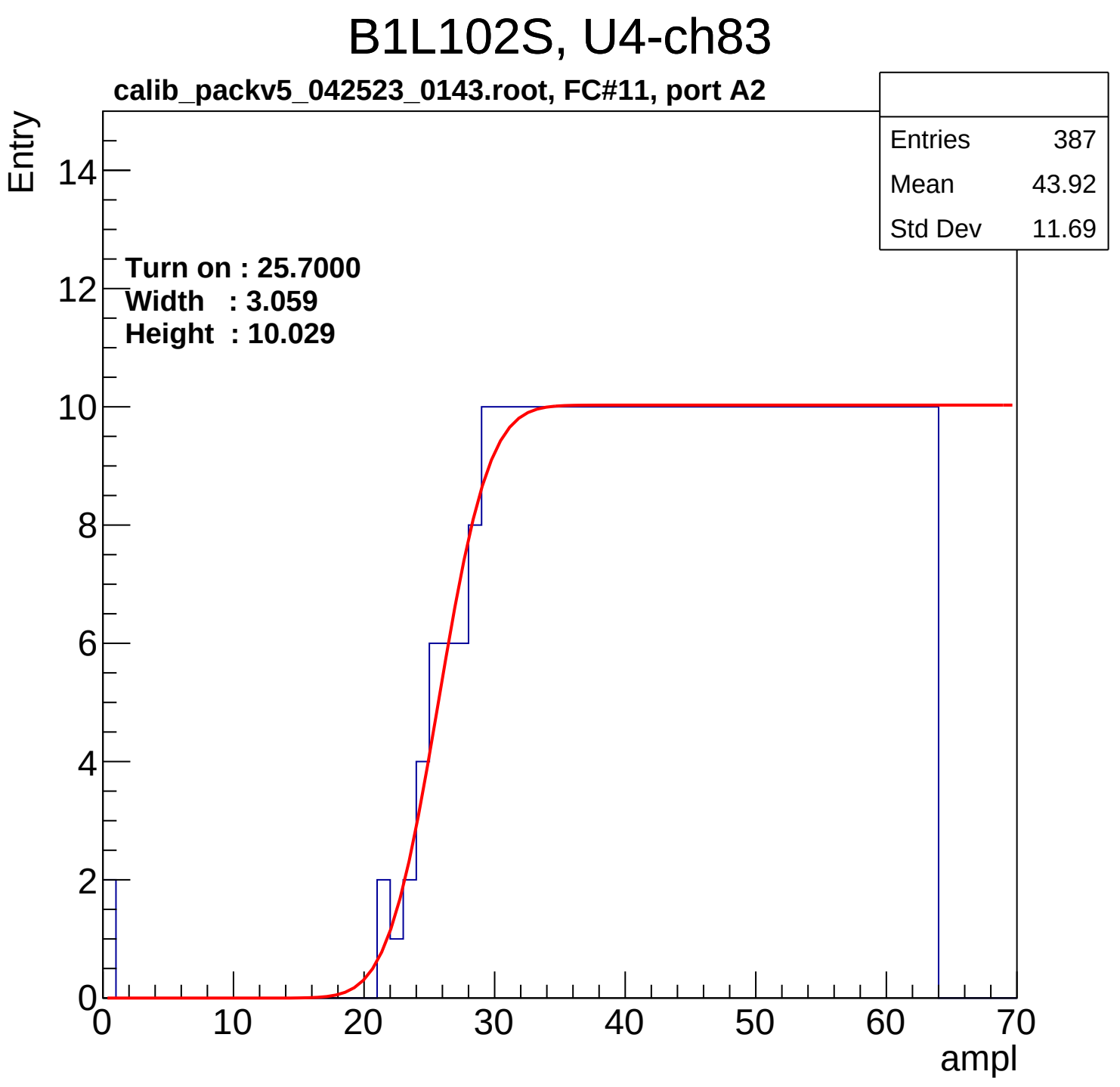
B1L102S, U4-ch83
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 43.92
Std Dev 11.69
Turn on : 25.7000
Width : 3.059
Height : 10.029
Entry
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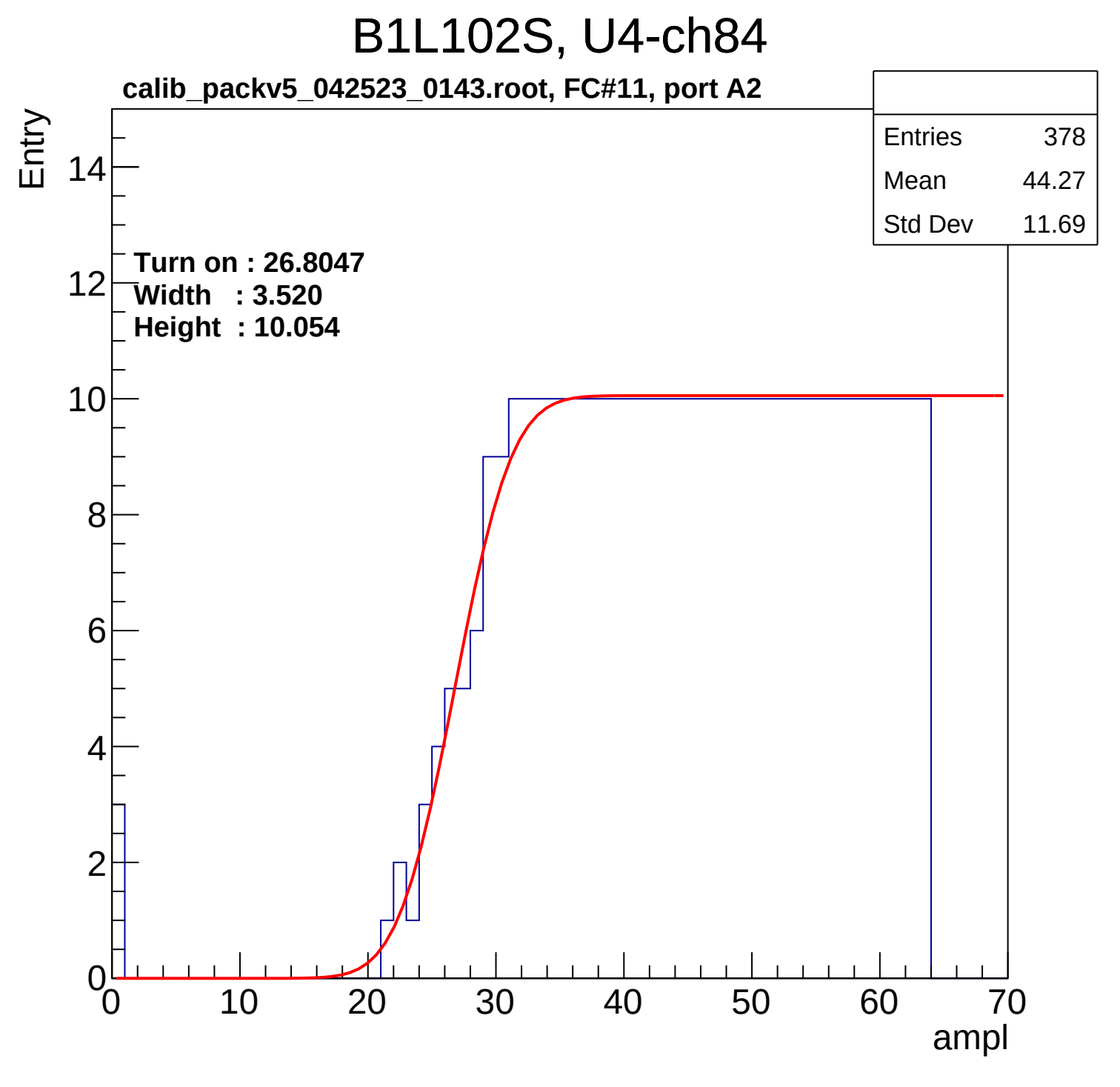
B1L102S, U4-ch84
calib_packv5_042523_0143.root, FC#11, port A2
Entries 378
Mean 44.27
Std Dev 11.69
Turn on : 26.8047
Width : 3.520
Height : 10.054
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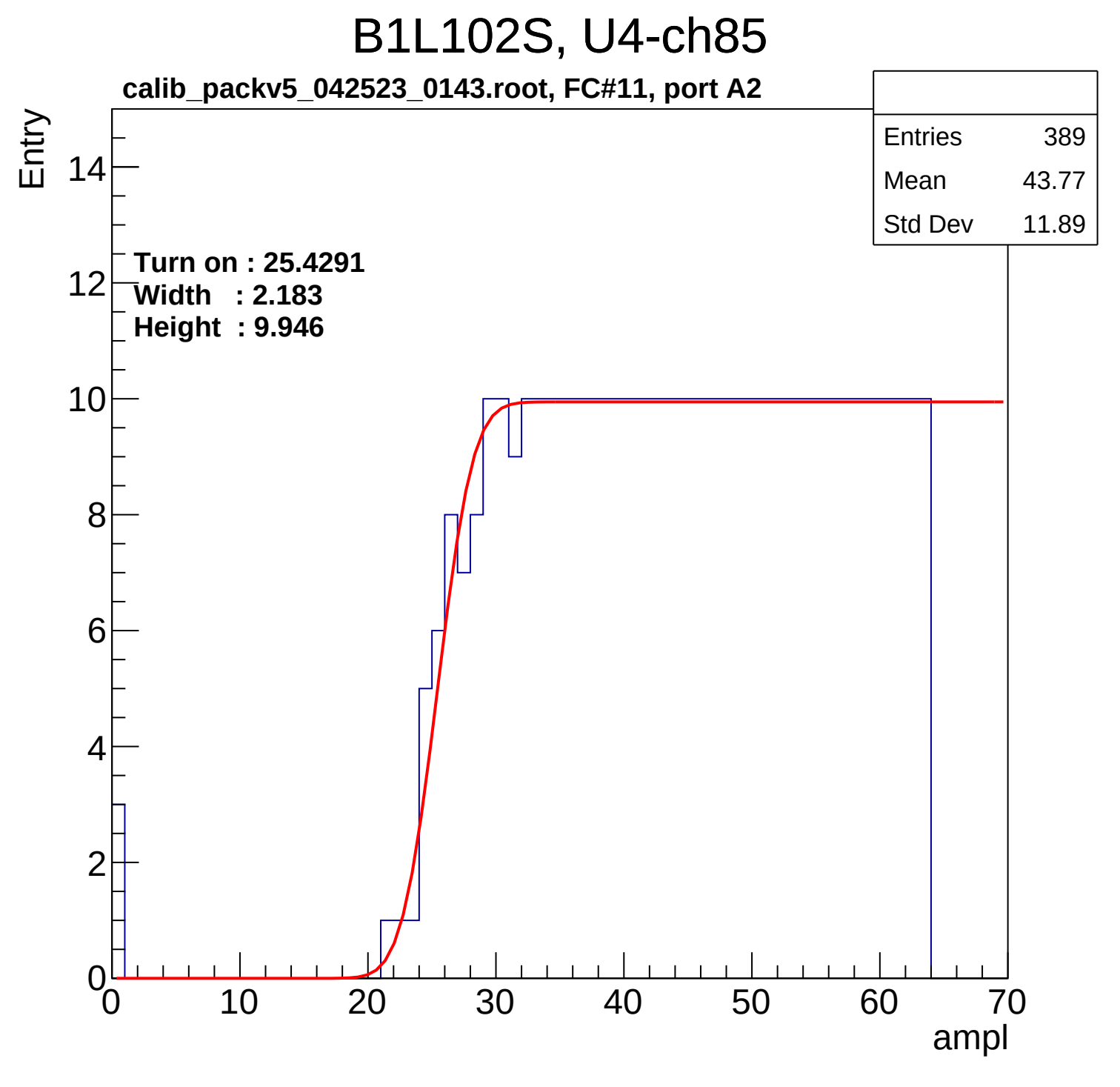
B1L102S, U4-ch85
calib_packv5_042523_0143.root, FC#11, port A2
Entries 389
Mean 43.77
Std Dev 11.89
Turn on : 25.4291
Width : 2.183
Height : 9.946
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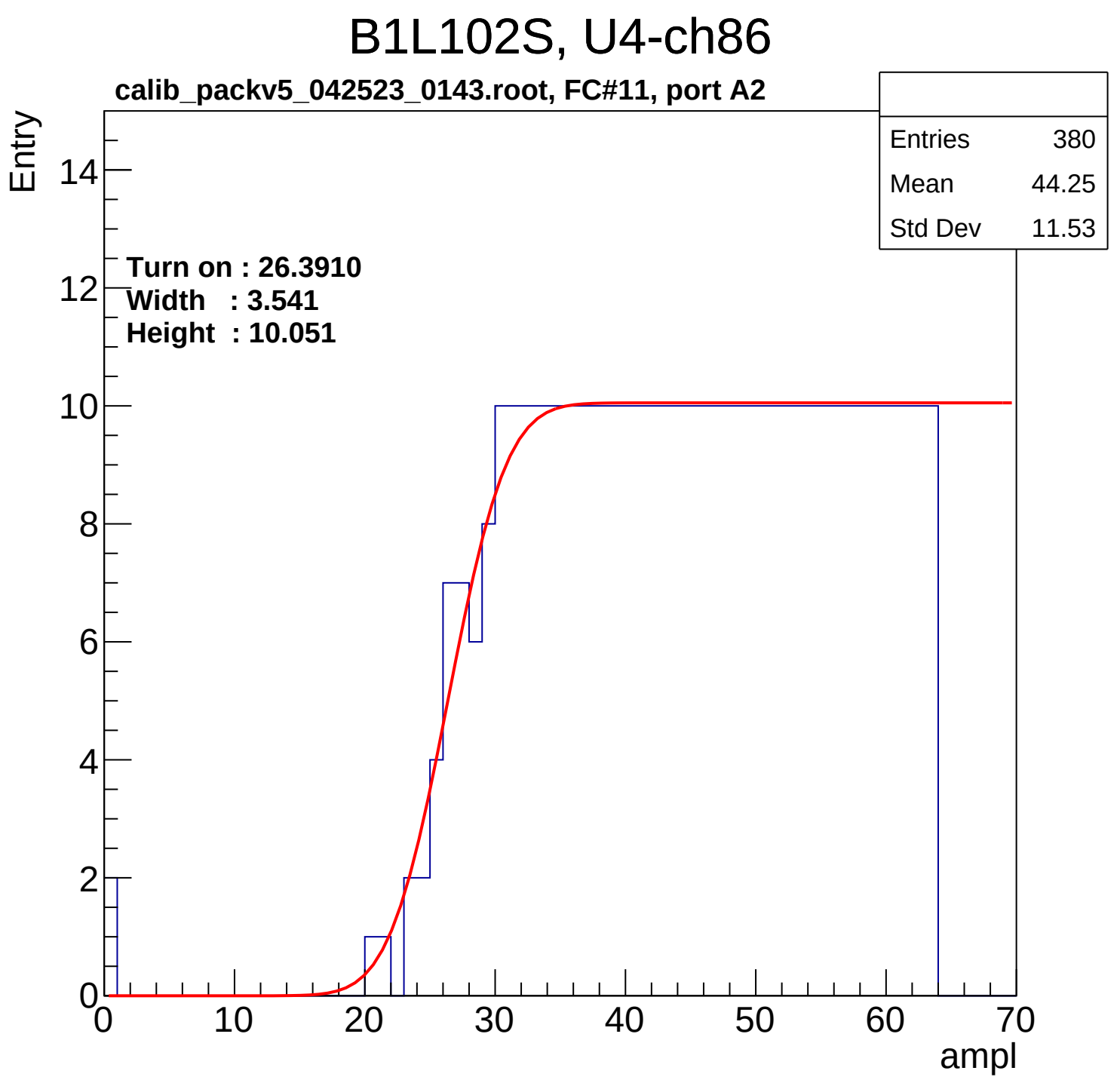
B1L102S, U4-ch86
calib_packv5_042523_0143.root, FC#11, port A2
Entries 380
Mean 44.25
Std Dev 11.53
Turn on : 26.3910
Width : 3.541
Height : 10.051
Entry
ampl
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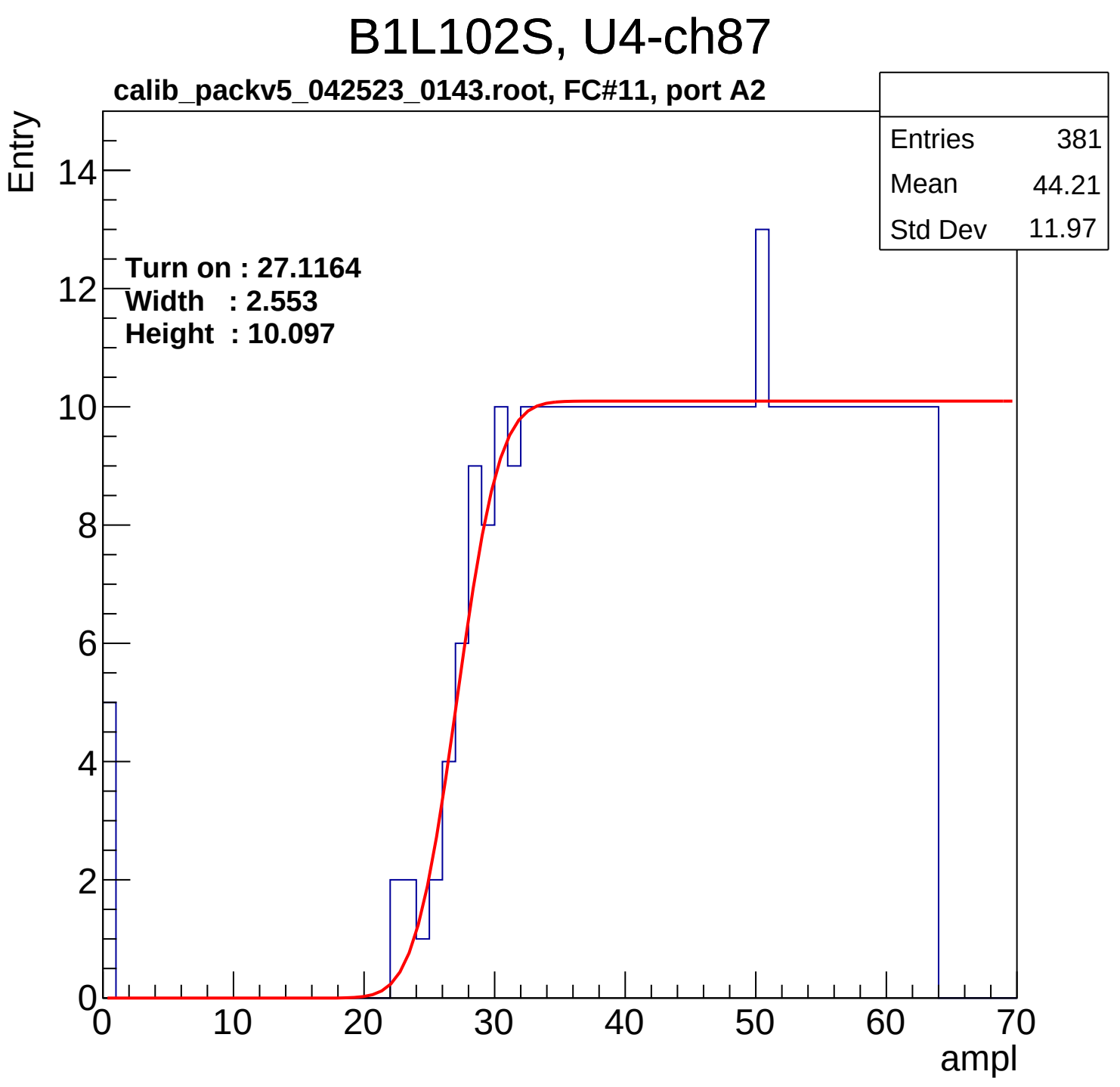
B1L102S, U4-ch87
calib_packv5_042523_0143.root, FC#11, port A2
Entries 381
Mean 44.21
Std Dev 11.97
Turn on : 27.1164
Width : 2.553
Height : 10.097
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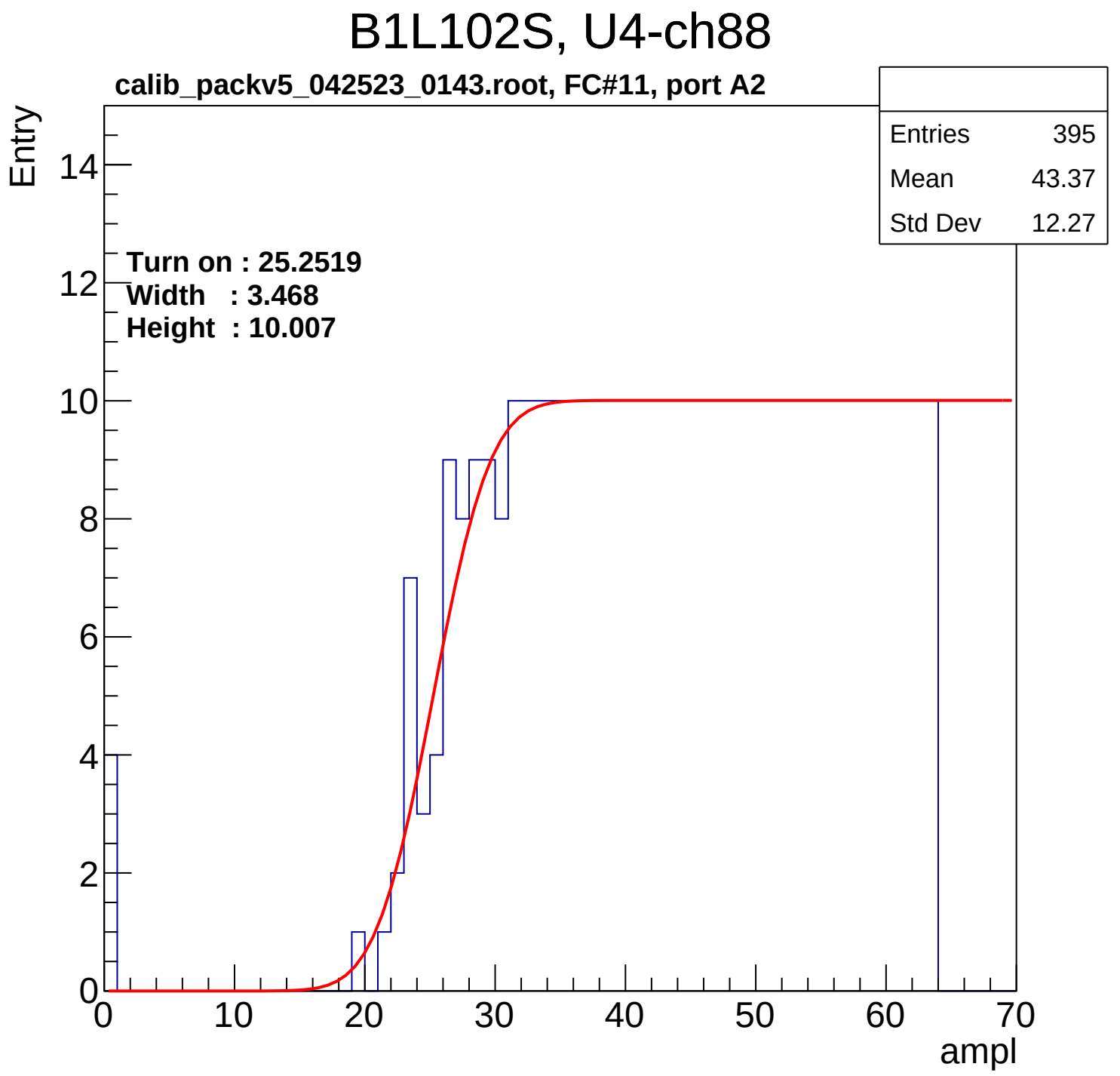
B1L102S, U4-ch88
calib_packv5_042523_0143.root, FC#11, port A2
Entries 395
Mean 43.37
Std Dev 12.27
Turn on : 25.2519
Width : 3.468
Height : 10.007
Entry
ampl
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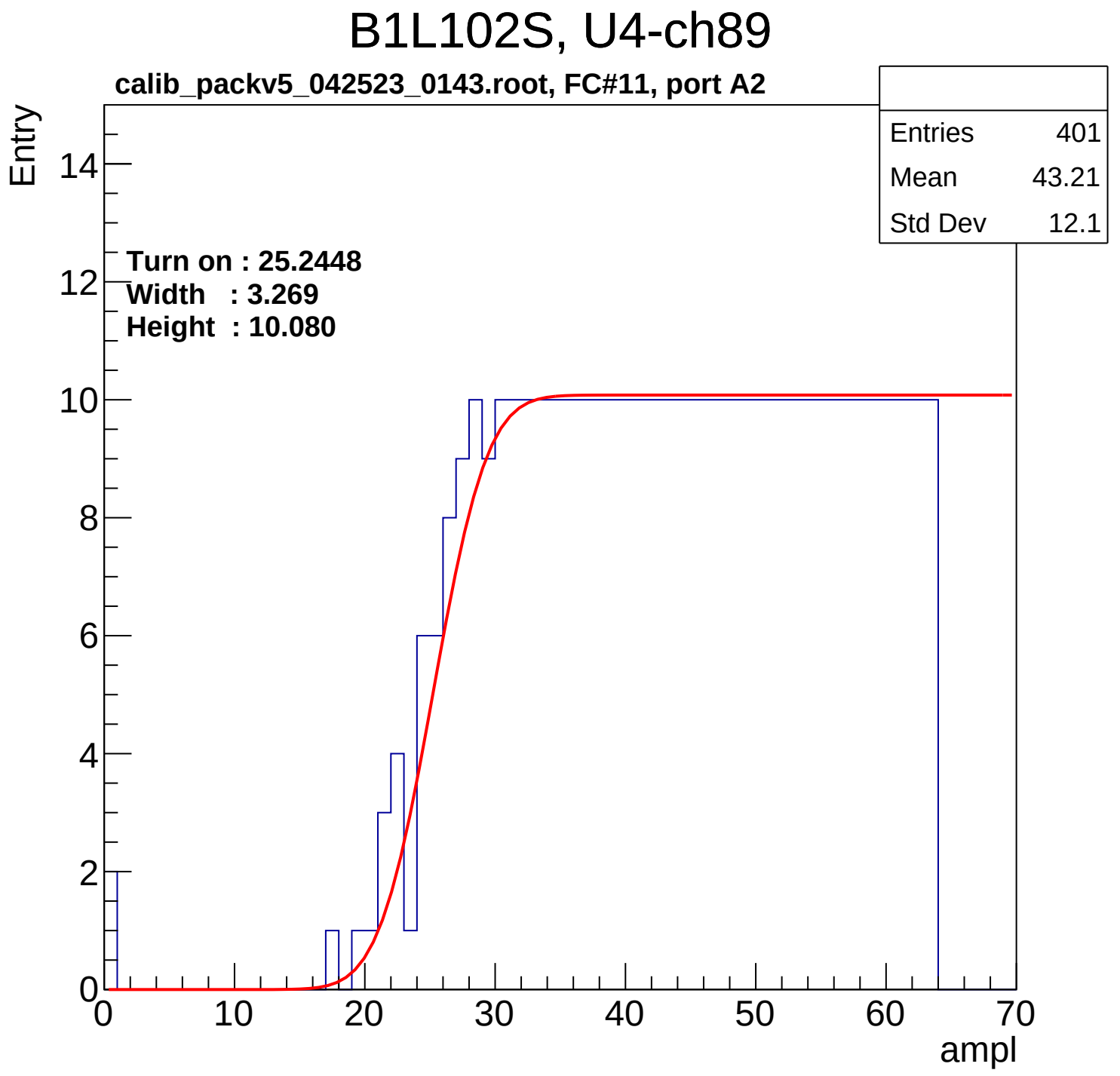
B1L102S, U4-ch89
calib_packv5_042523_0143.root, FC#11, port A2
Entries 401
Mean 43.21
Std Dev 12.1
Turn on : 25.2448
Width : 3.269
Height : 10.080
Entry
ampl
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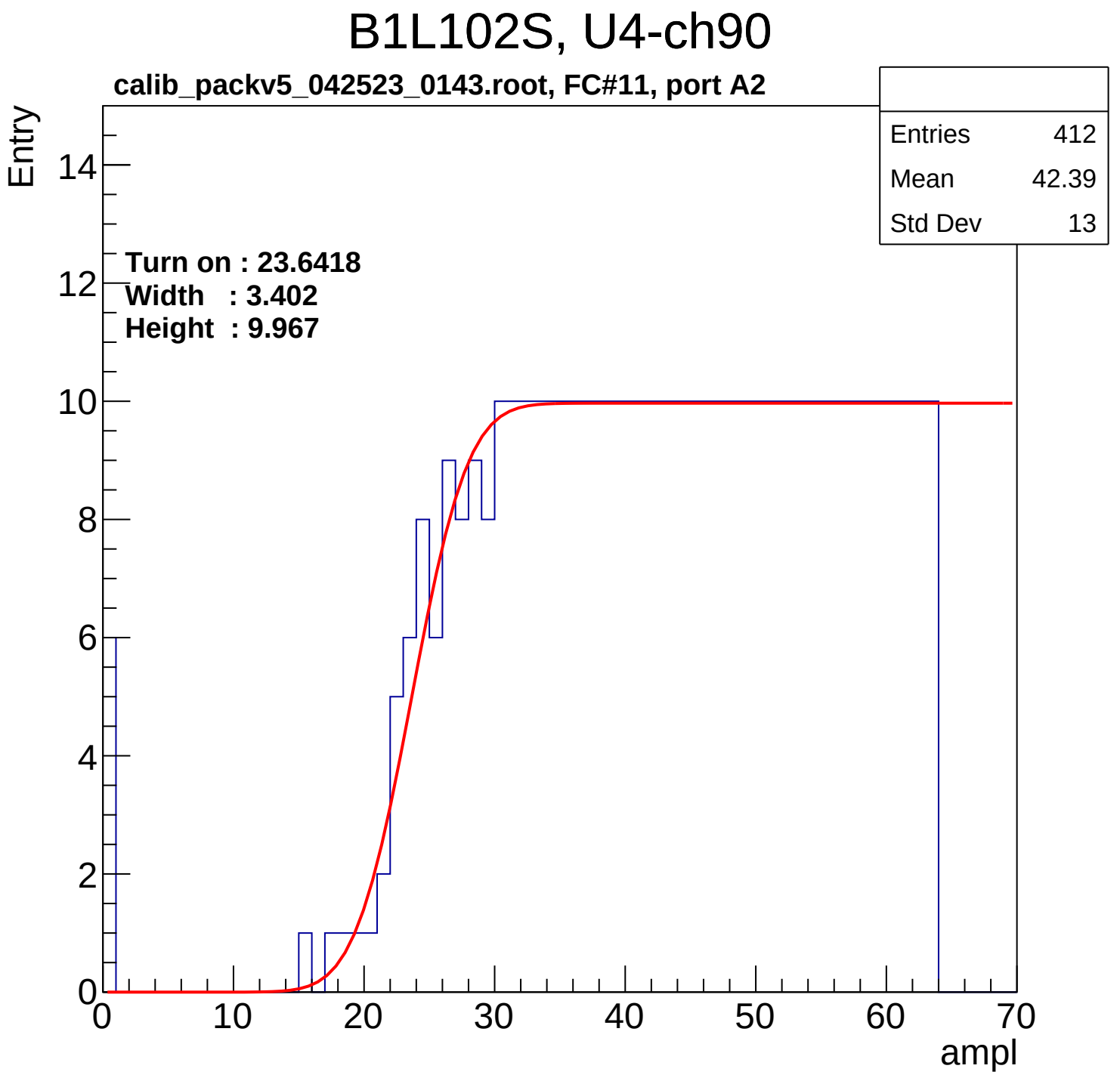
B1L102S, U4-ch90
calib_packv5_042523_0143.root, FC#11, port A2
Entries 412
Mean 42.39
Std Dev 13
Turn on : 23.6418
Width : 3.402
Height : 9.967
Entry
ampl
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2
4
6
8
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0
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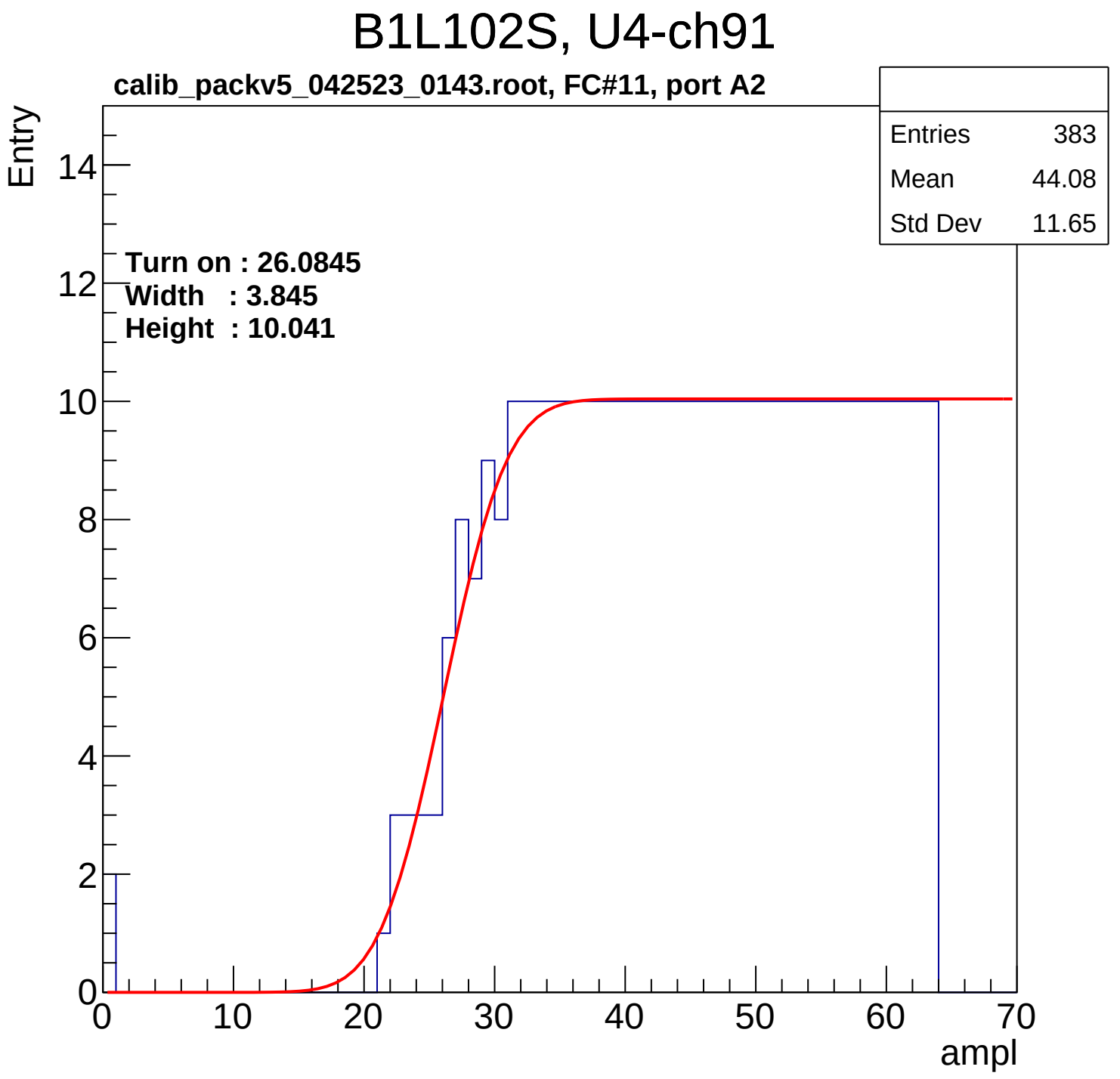
B1L102S, U4-ch91
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 44.08
Std Dev 11.65
Turn on : 26.0845
Width : 3.845
Height : 10.041
Entry
ampl
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8
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12
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0
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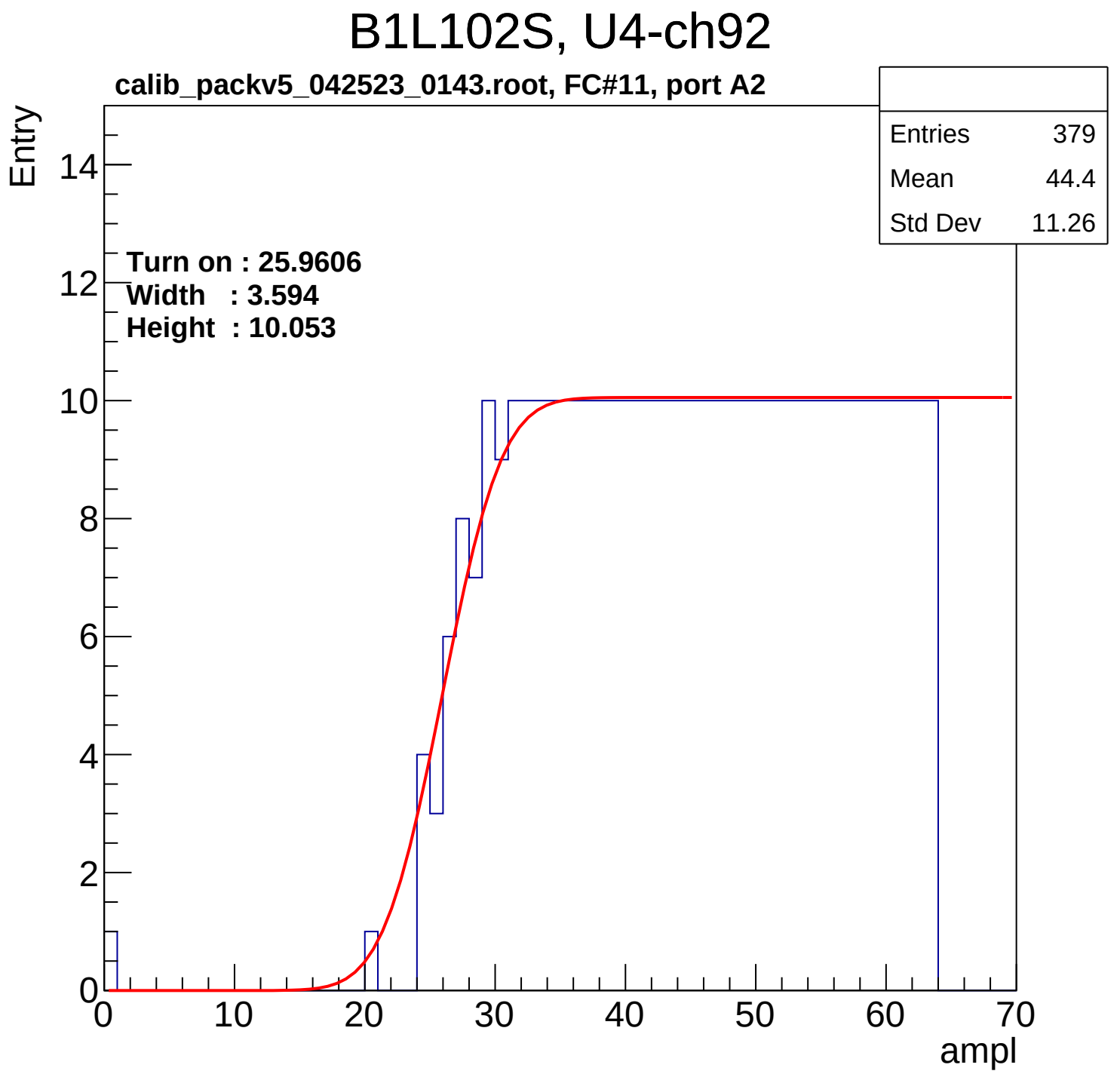
B1L102S, U4-ch92
calib_packv5_042523_0143.root, FC#11, port A2
Entries 379
Mean 44.4
Std Dev 11.26
Turn on : 25.9606
Width : 3.594
Height : 10.053
Entry
ampl
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2
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6
8
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12
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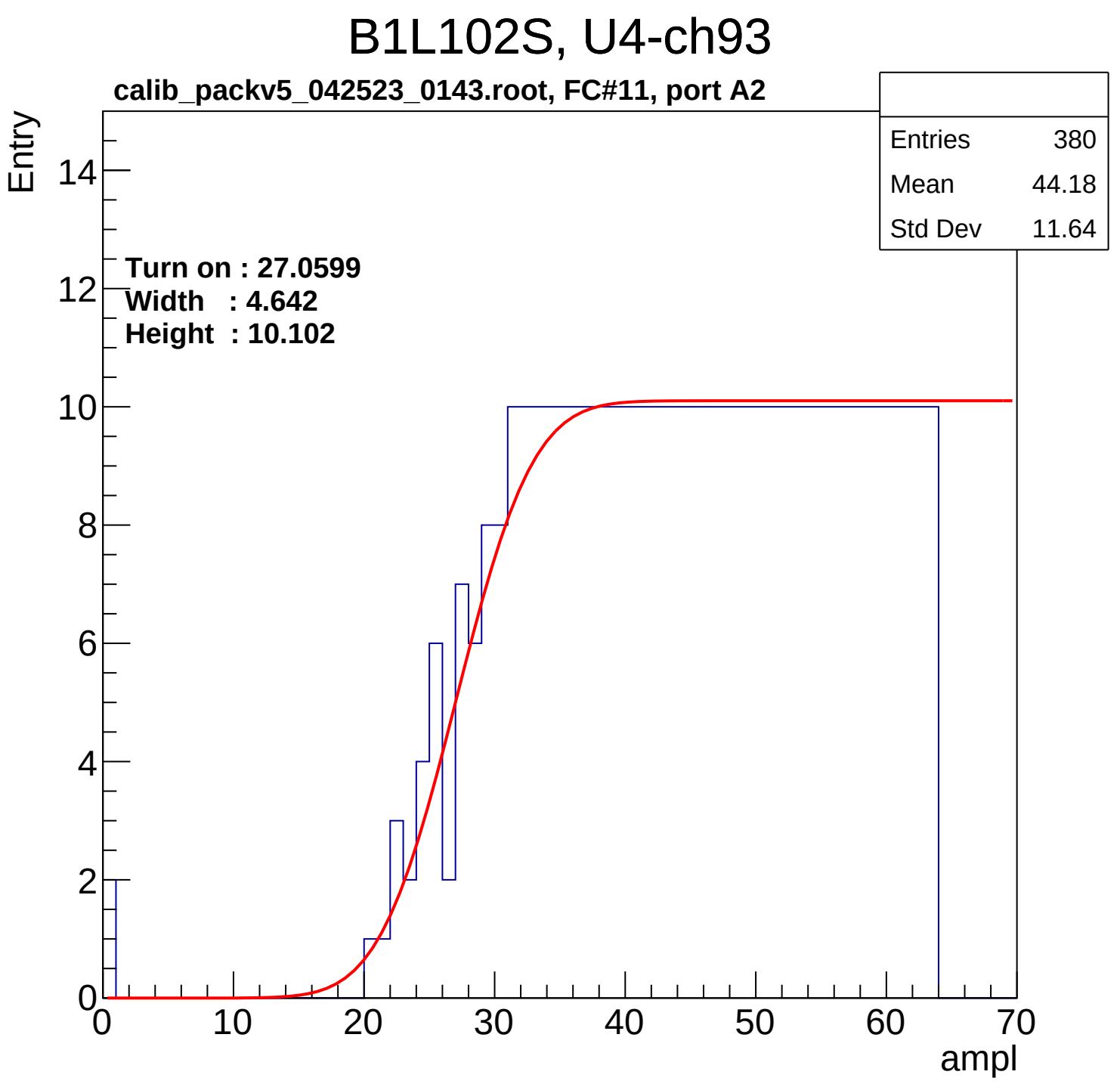
B1L102S, U4-ch93
calib_packv5_042523_0143.root, FC#11, port A2
Entries 380
Mean 44.18
Std Dev 11.64
Turn on : 27.0599
Width : 4.642
Height : 10.102
Entry
ampl
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4
6
8
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12
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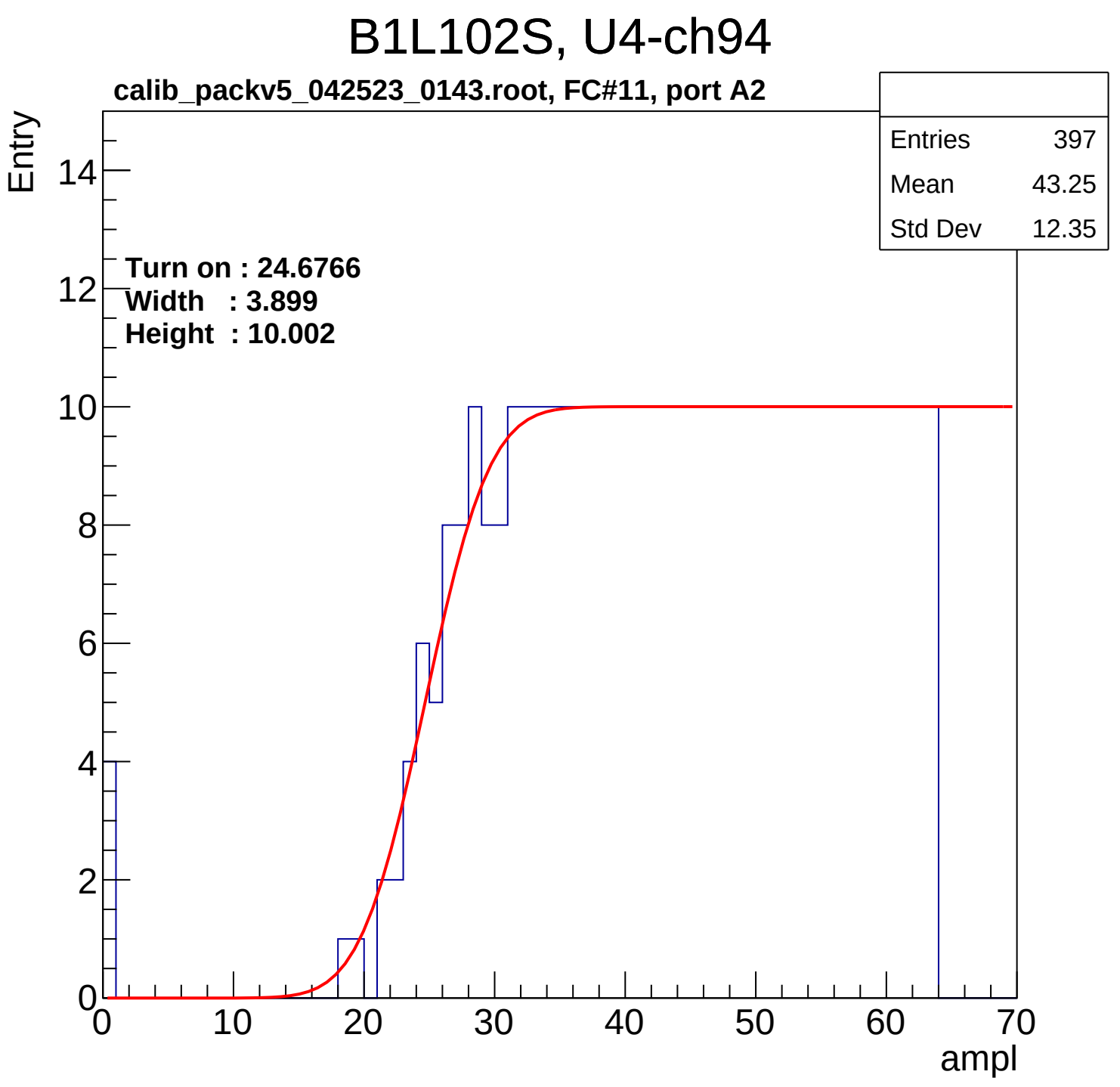
B1L102S, U4-ch94
calib_packv5_042523_0143.root, FC#11, port A2
Entries 397
Mean 43.25
Std Dev 12.35
Turn on : 24.6766
Width : 3.899
Height : 10.002
Entry
ampl
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2
4
6
8
10
12
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0
10
20
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40
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60
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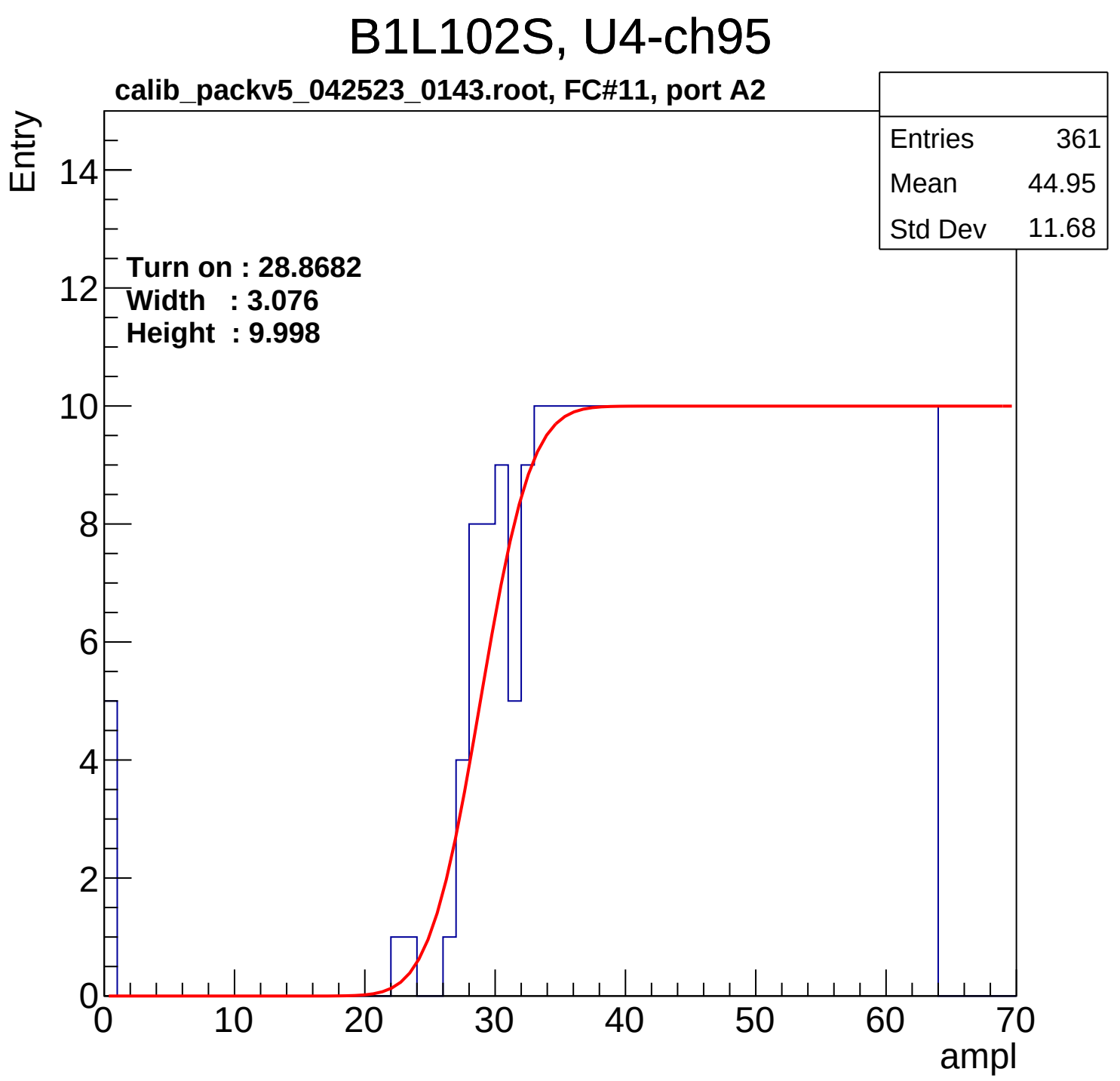
B1L102S, U4-ch95
calib_packv5_042523_0143.root, FC#11, port A2
Entries 361
Mean 44.95
Std Dev 11.68
Turn on : 28.8682
Width : 3.076
Height : 9.998
Entry
ampl
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8
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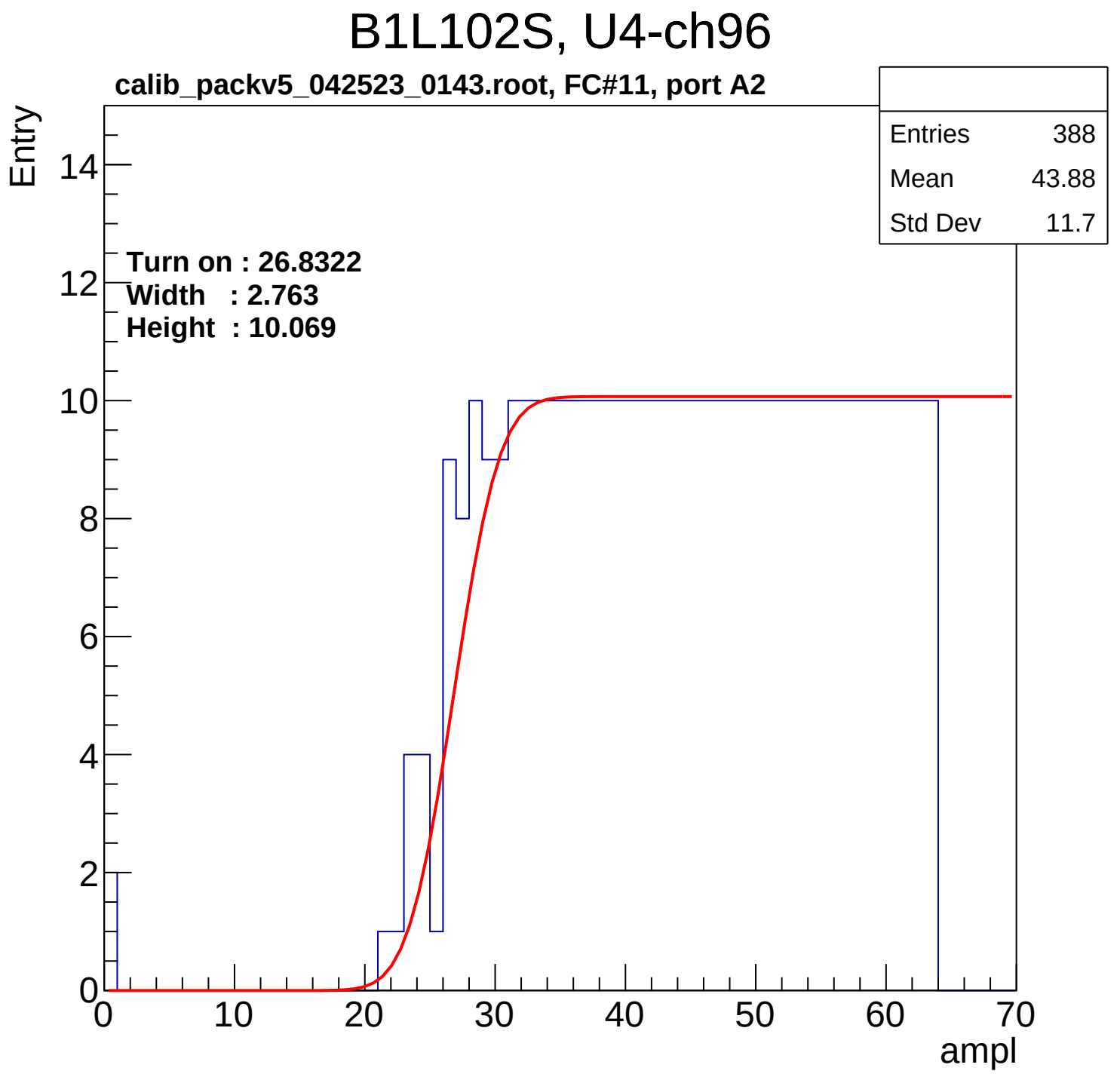
B1L102S, U4-ch96
calib_packv5_042523_0143.root, FC#11, port A2
Entries 388
Mean 43.88
Std Dev 11.7
Turn on : 26.8322
Width : 2.763
Height : 10.069
Entry
ampl
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6
8
10
12
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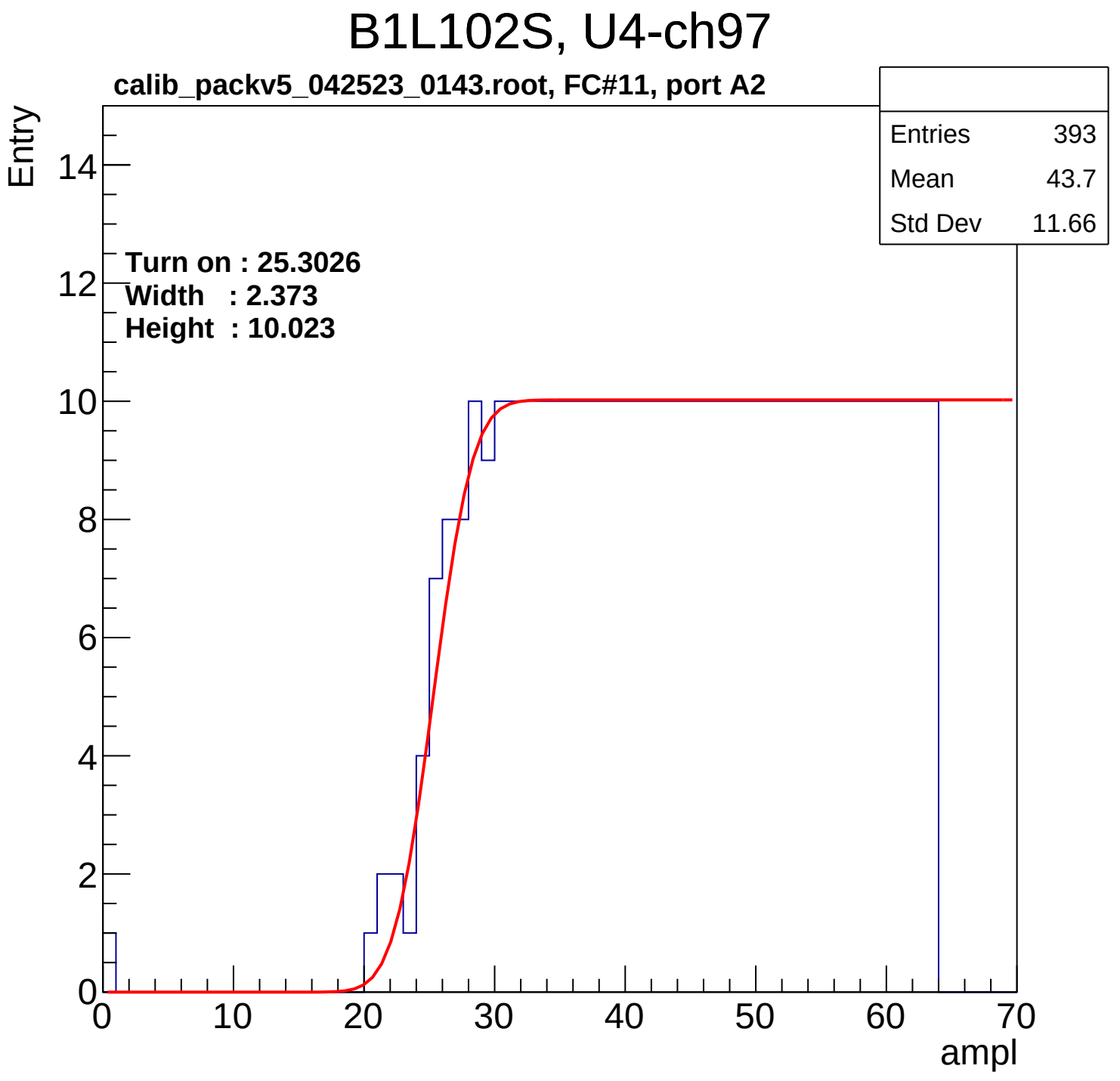
B1L102S, U4-ch97
calib_packv5_042523_0143.root, FC#11, port A2
Entries 393
Mean 43.7
Std Dev 11.66
Turn on : 25.3026
Width : 2.373
Height : 10.023
Entry
ampl
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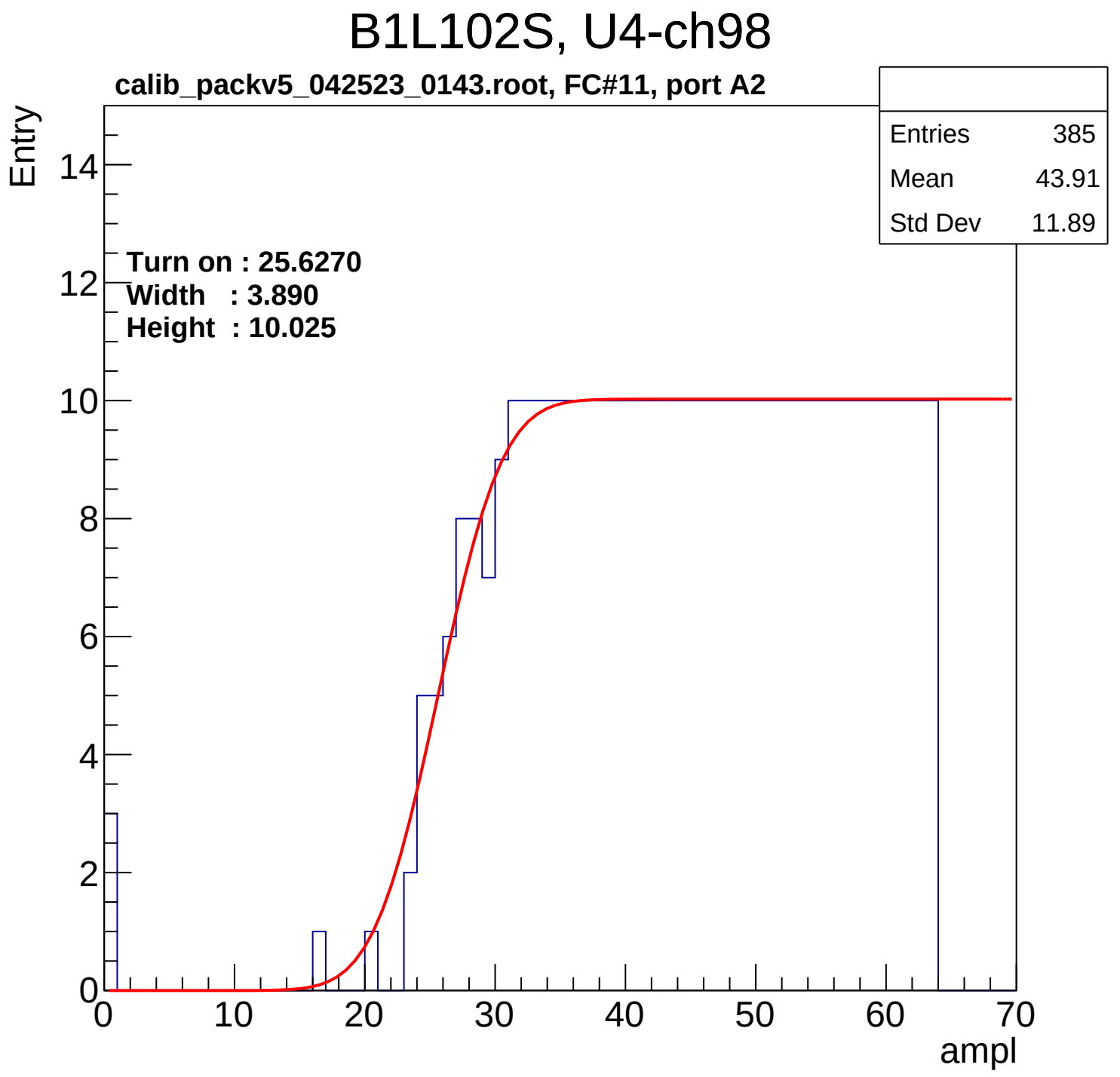
B1L102S, U4-ch98
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 43.91
Std Dev 11.89
Turn on : 25.6270
Width : 3.890
Height : 10.025
Entry
ampl
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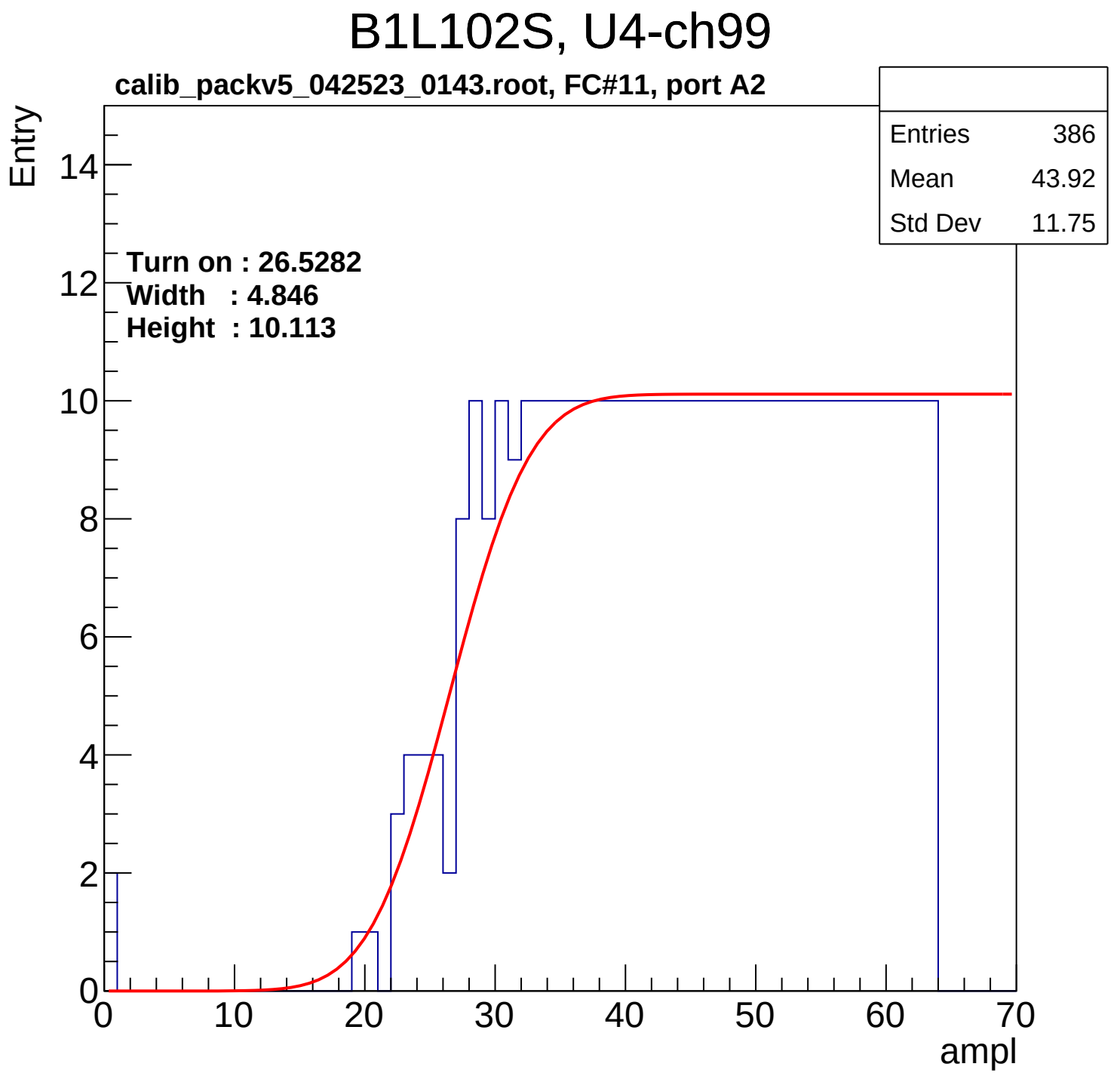
B1L102S, U4-ch99
calib_packv5_042523_0143.root, FC#11, port A2
Entries 386
Mean 43.92
Std Dev 11.75
Turn on : 26.5282
Width : 4.846
Height : 10.113
Entry
ampl
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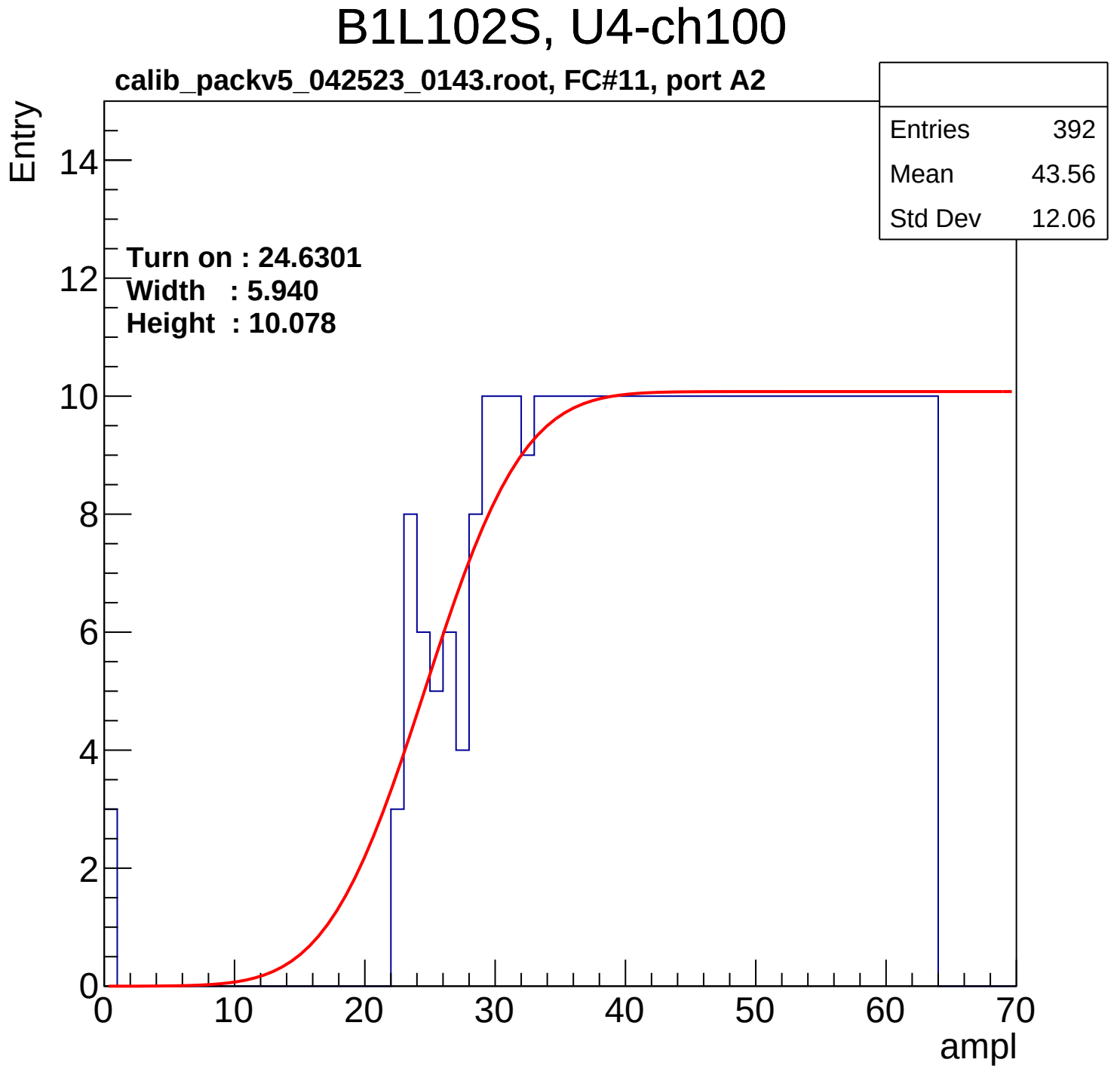
B1L102S, U4-ch100
calib_packv5_042523_0143.root, FC#11, port A2
Entries 392
Mean 43.56
Std Dev 12.06
Turn on : 24.6301
Width : 5.940
Height : 10.078
Entry
ampl
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6
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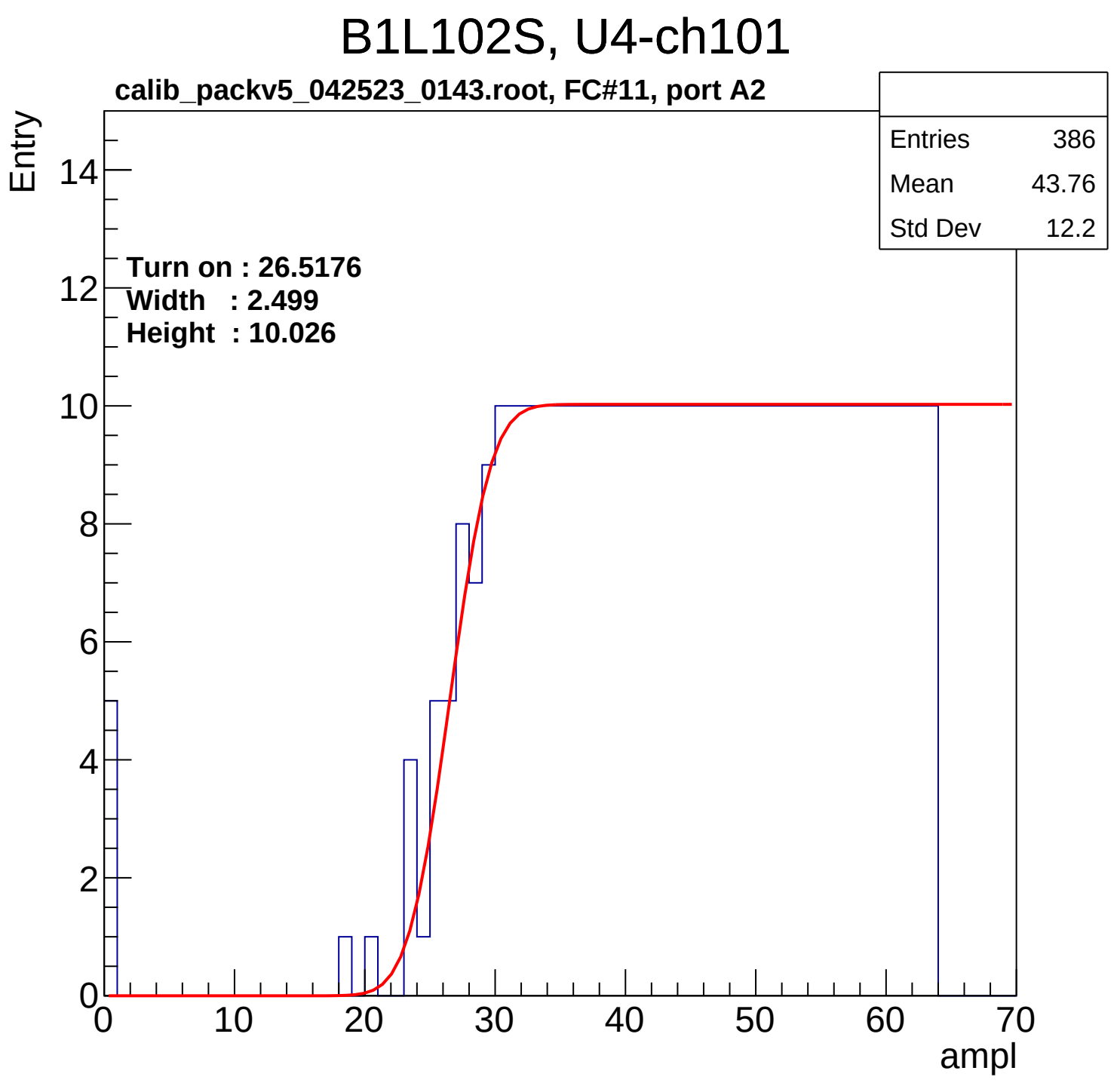
B1L102S, U4-ch101
calib_packv5_042523_0143.root, FC#11, port A2
Entries 386
Mean 43.76
Std Dev 12.2
Turn on : 26.5176
Width : 2.499
Height : 10.026
Entry
ampl
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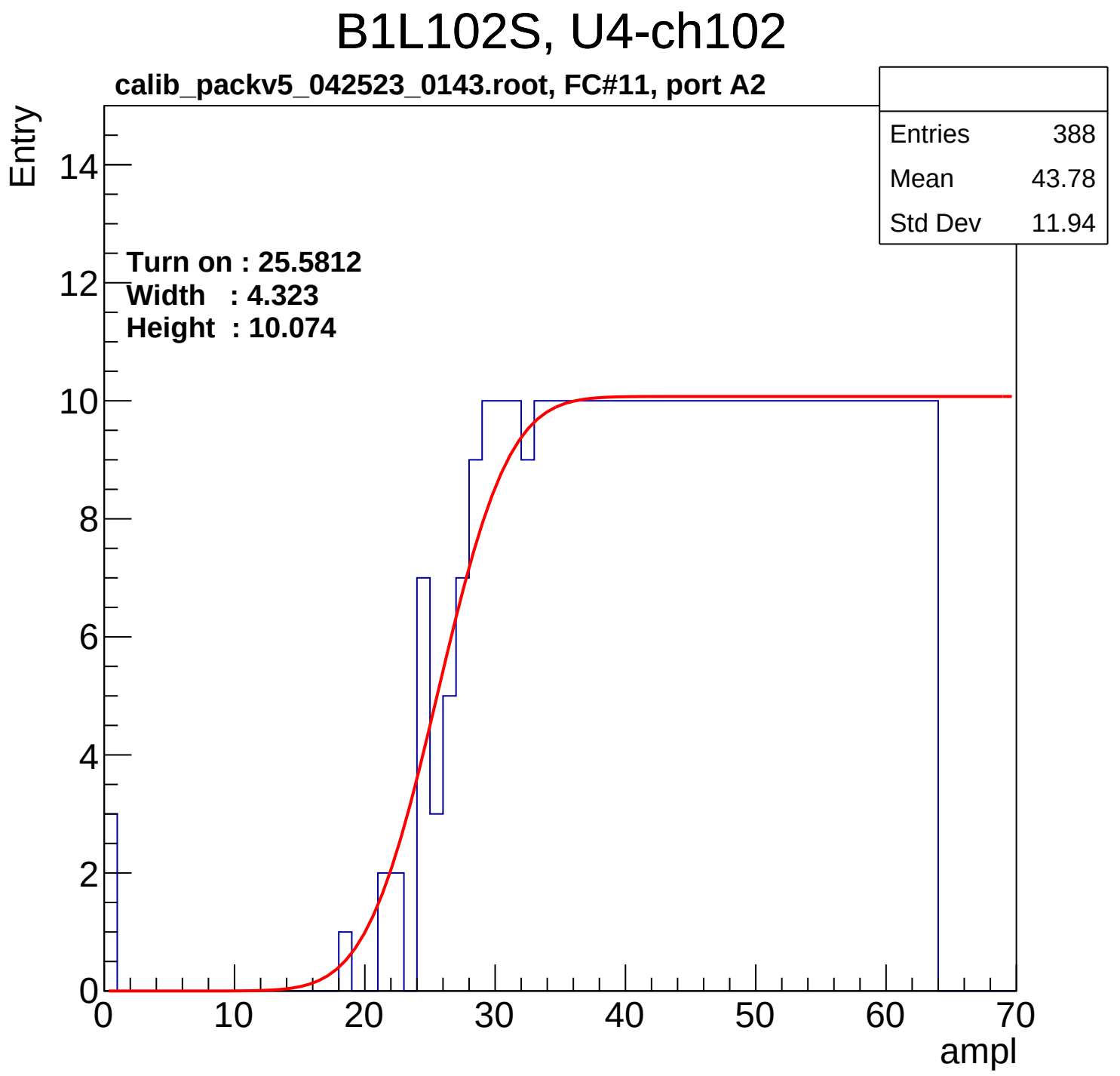
B1L102S, U4-ch102
calib_packv5_042523_0143.root, FC#11, port A2
Entries 388
Mean 43.78
Std Dev 11.94
Turn on : 25.5812
Width : 4.323
Height : 10.074
Entry
ampl
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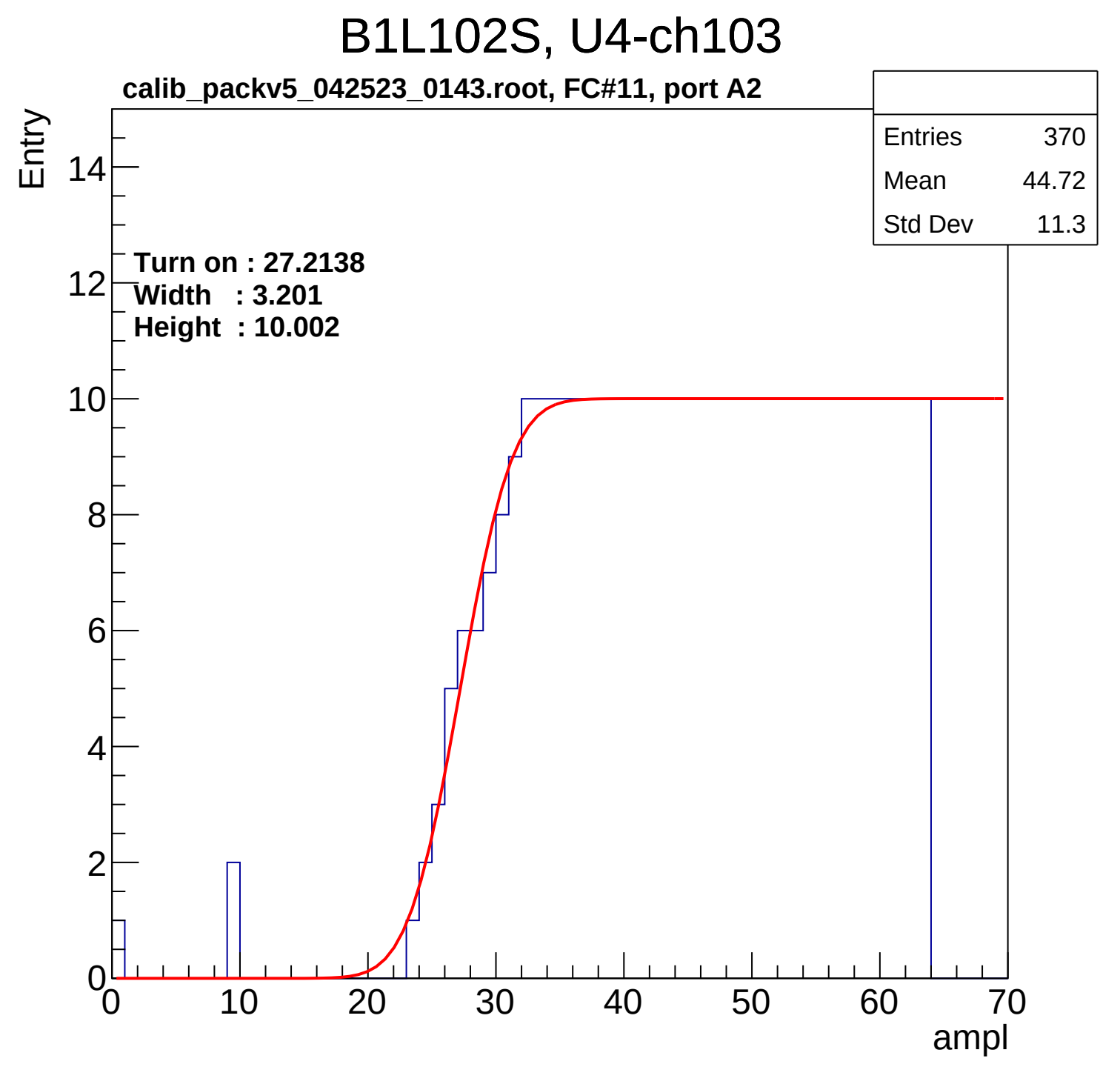
B1L102S, U4-ch103
calib_packv5_042523_0143.root, FC#11, port A2
Entries 370
Mean 44.72
Std Dev 11.3
Turn on : 27.2138
Width : 3.201
Height : 10.002
Entry
ampl
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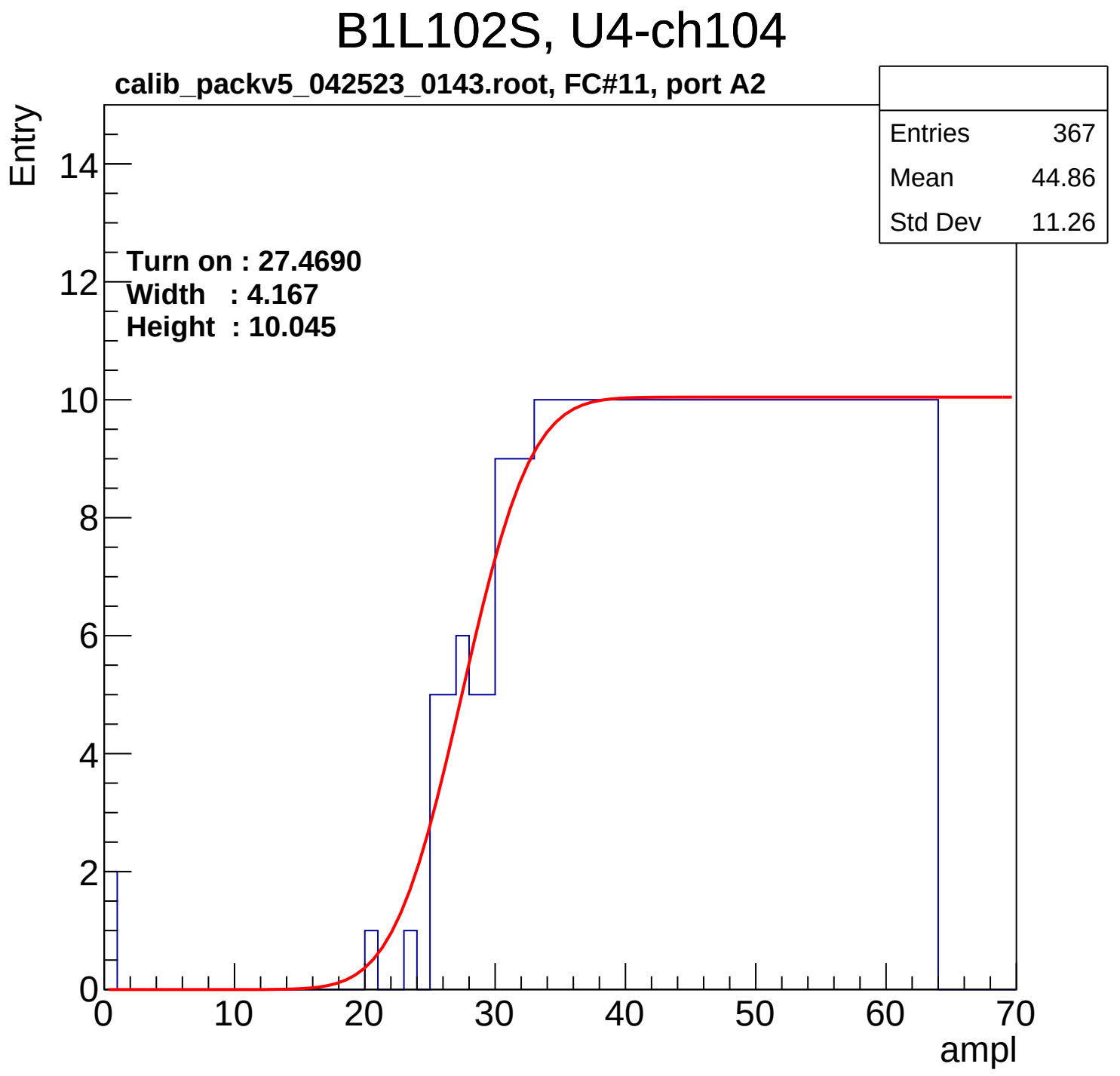
B1L102S, U4-ch104
calib_packv5_042523_0143.root, FC#11, port A2
Entries 367
Mean 44.86
Std Dev 11.26
Turn on : 27.4690
Width : 4.167
Height : 10.045
Entry
ampl
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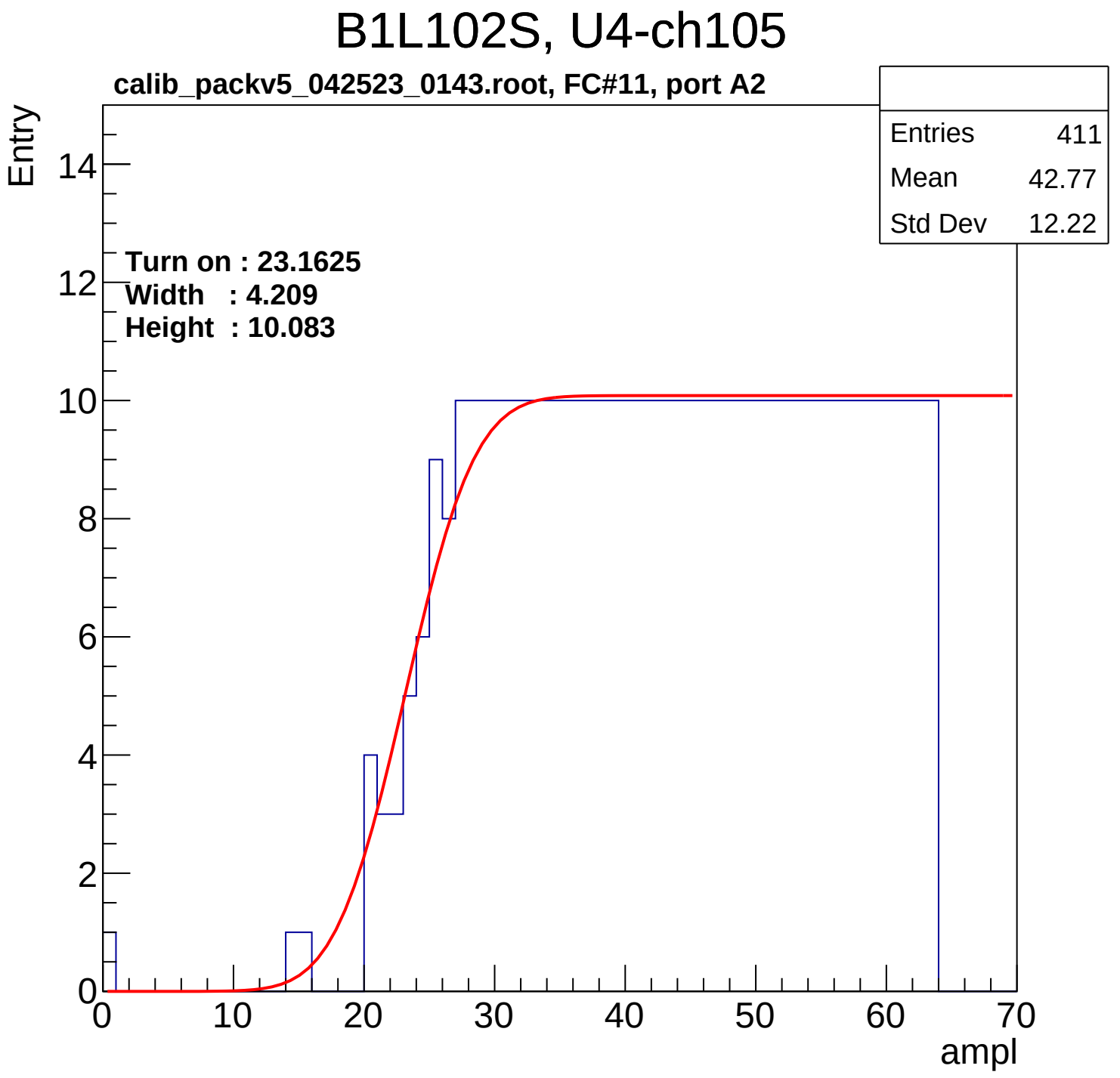
B1L102S, U4-ch105
calib_packv5_042523_0143.root, FC#11, port A2
Entries 411
Mean 42.77
Std Dev 12.22
Turn on : 23.1625
Width : 4.209
Height : 10.083
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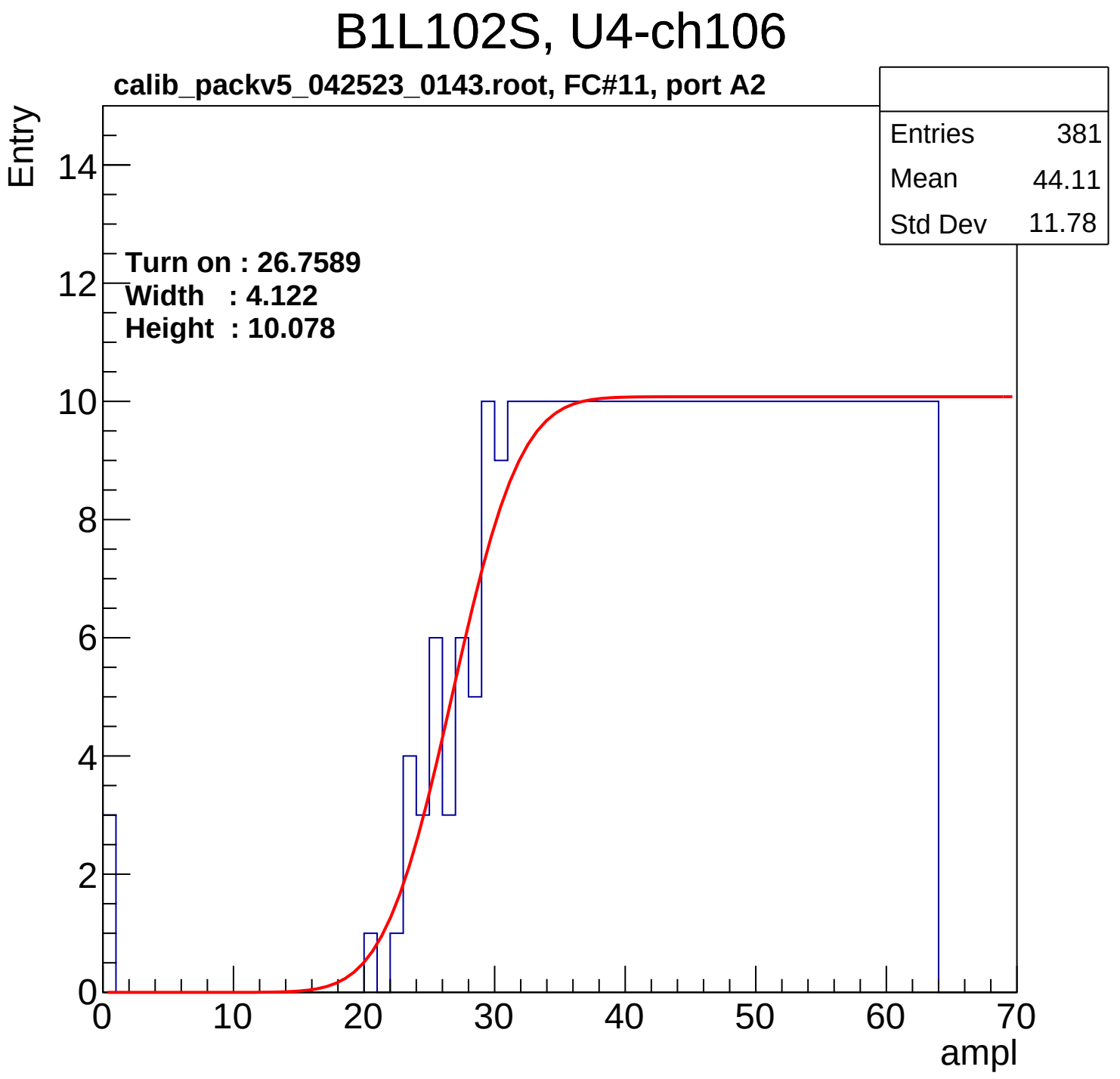
B1L102S, U4-ch106
calib_packv5_042523_0143.root, FC#11, port A2
Entries 381
Mean 44.11
Std Dev 11.78
Turn on : 26.7589
Width : 4.122
Height : 10.078
Entry
ampl
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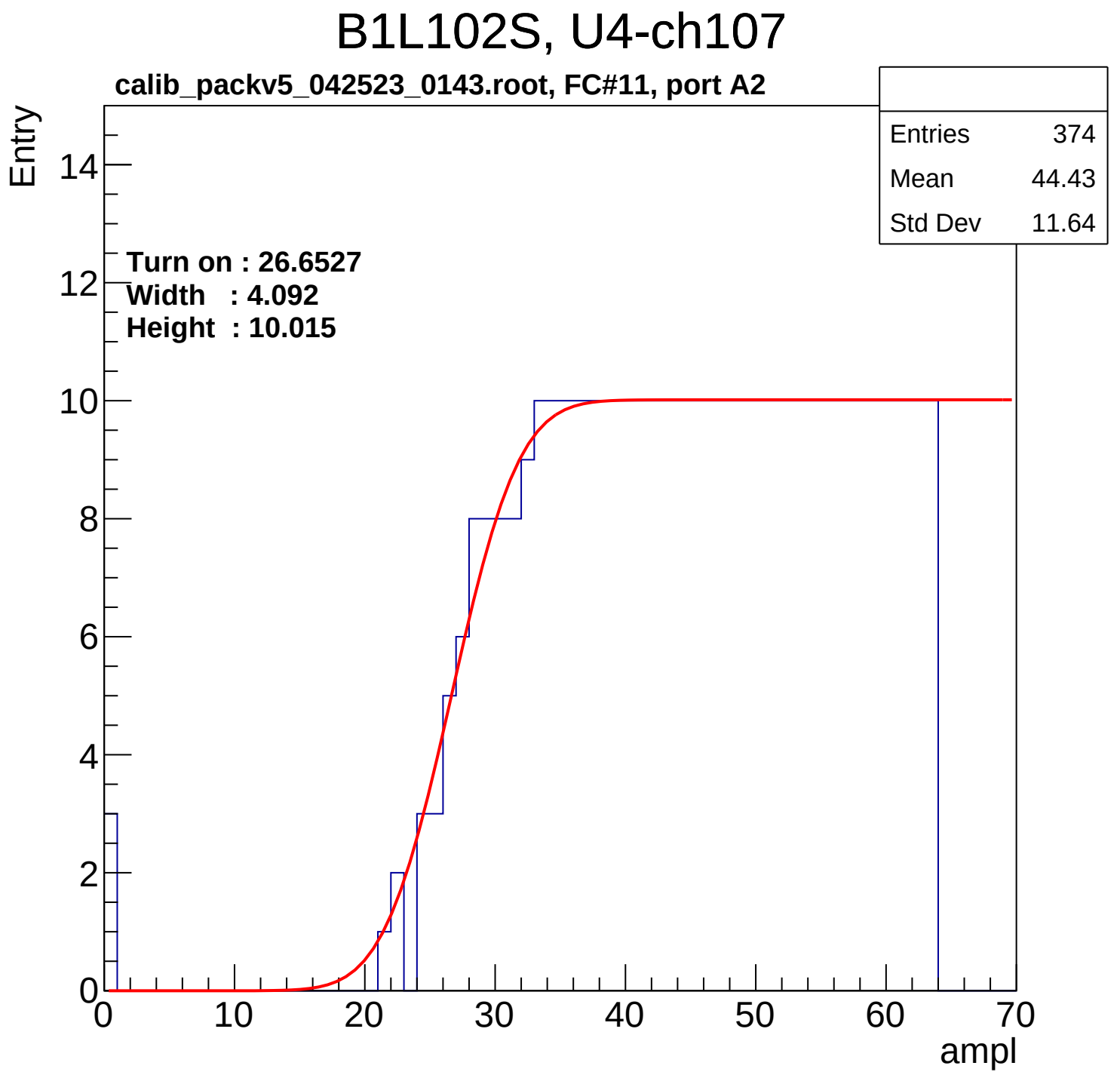
B1L102S, U4-ch107
calib_packv5_042523_0143.root, FC#11, port A2
Entries 374
Mean 44.43
Std Dev 11.64
Turn on : 26.6527
Width : 4.092
Height : 10.015
Entry
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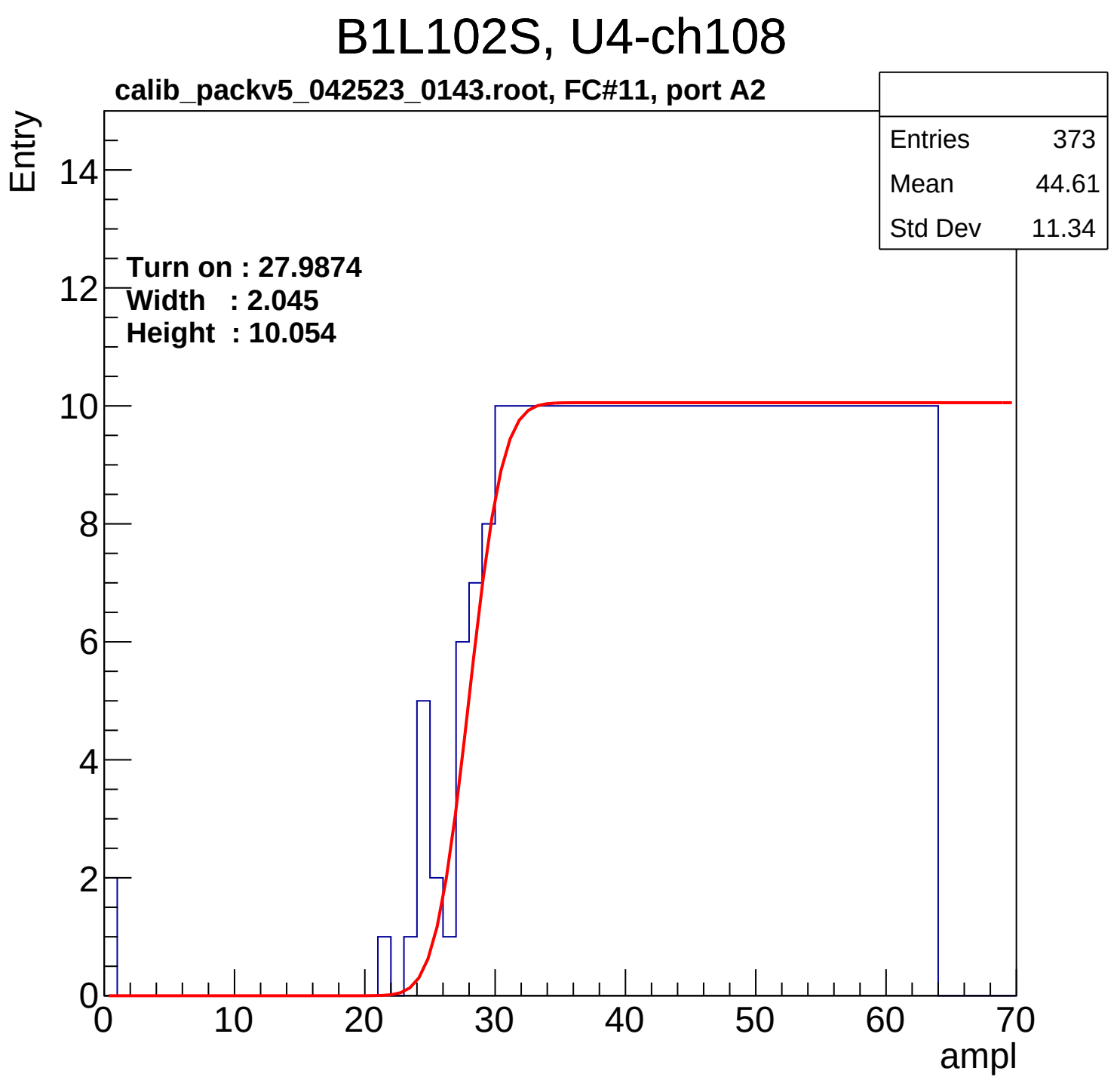
B1L102S, U4-ch108
calib_packv5_042523_0143.root, FC#11, port A2
Entries 373
Mean 44.61
Std Dev 11.34
Turn on : 27.9874
Width : 2.045
Height : 10.054
Entry
ampl
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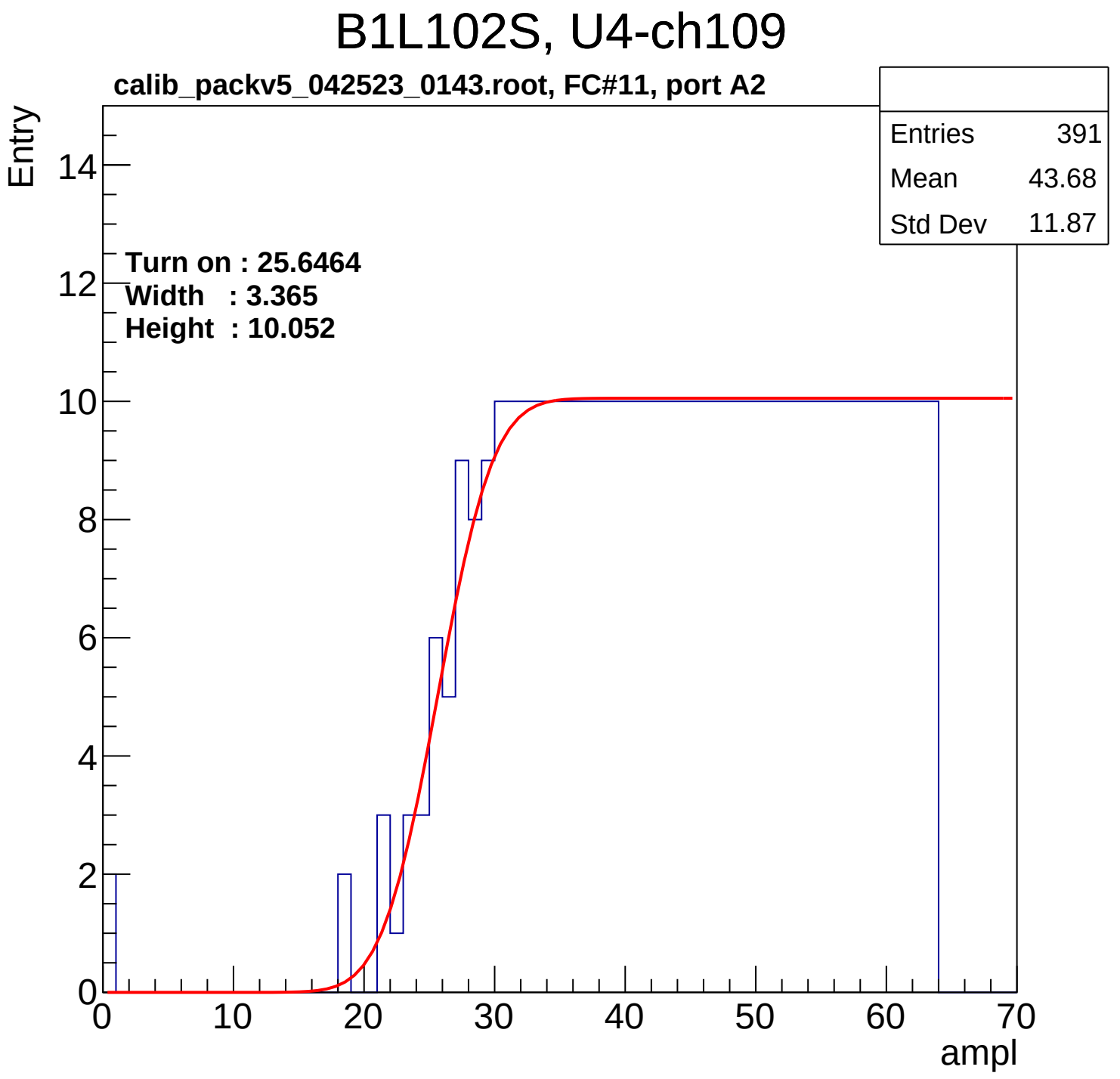
B1L102S, U4-ch109
calib_packv5_042523_0143.root, FC#11, port A2
Entries 391
Mean 43.68
Std Dev 11.87
Turn on : 25.6464
Width : 3.365
Height : 10.052
Entry
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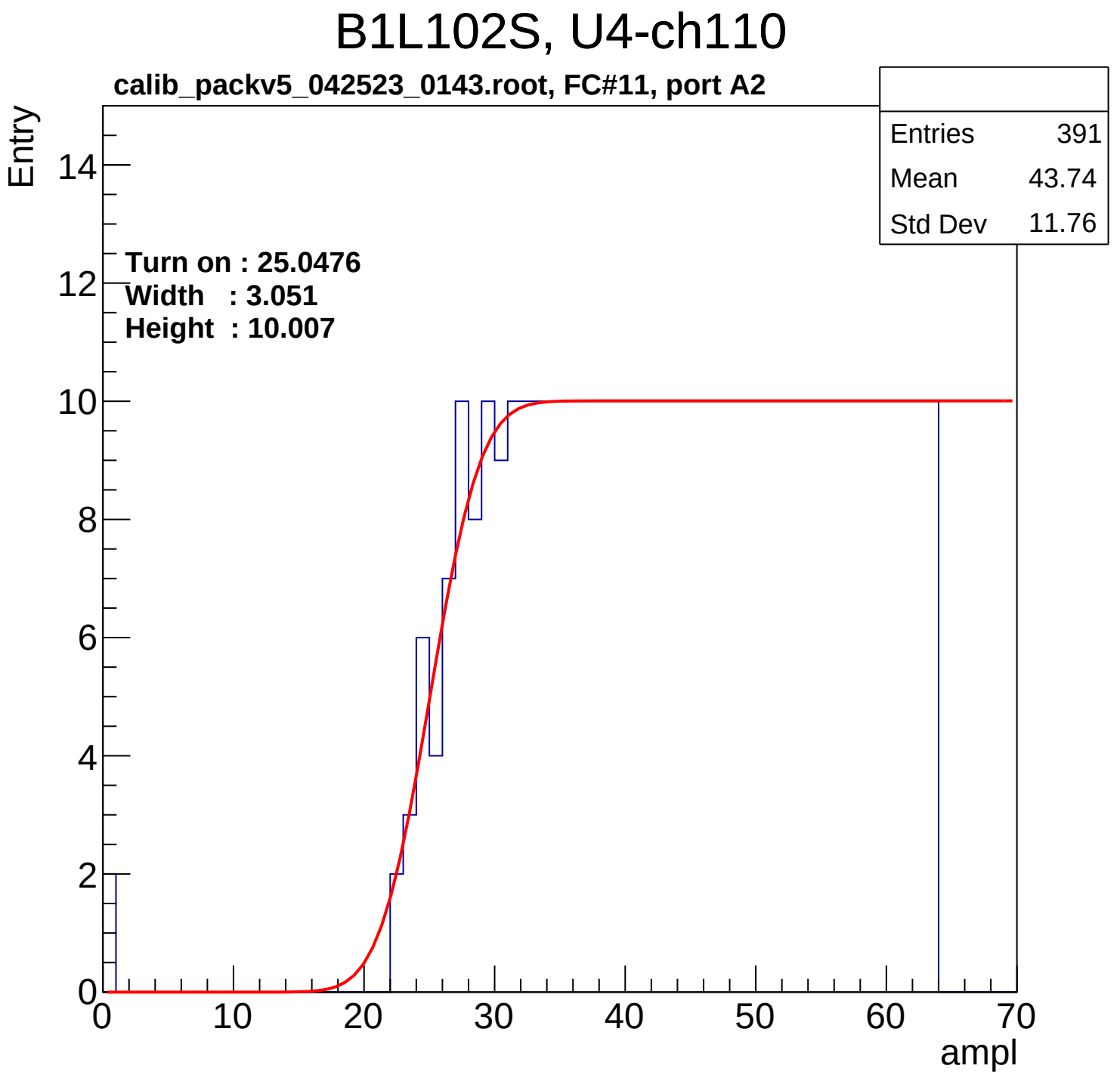
B1L102S, U4-ch110
calib_packv5_042523_0143.root, FC#11, port A2
Entries 391
Mean 43.74
Std Dev 11.76
Turn on : 25.0476
Width : 3.051
Height : 10.007
Entry
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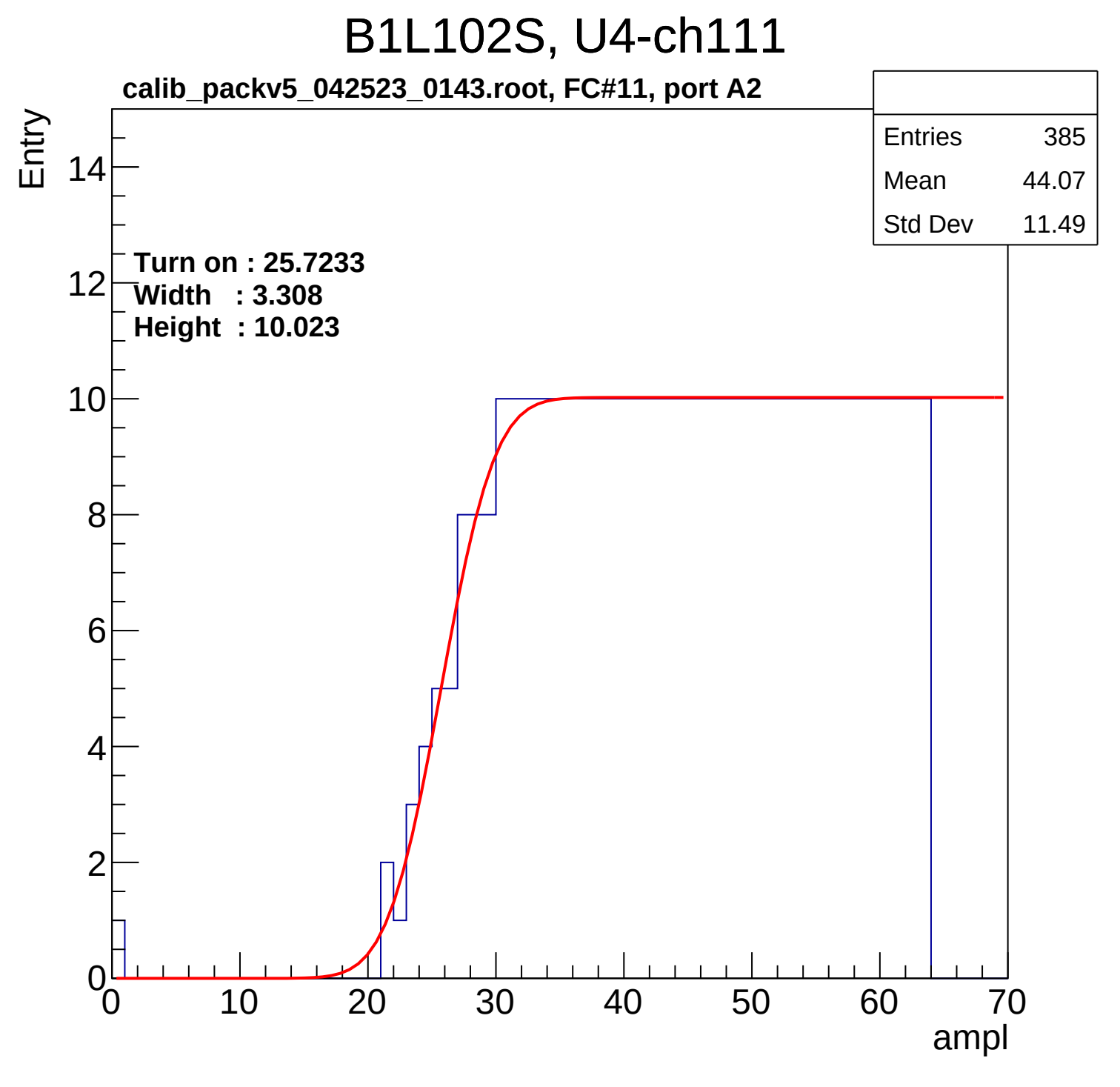
B1L102S, U4-ch111
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 44.07
Std Dev 11.49
Turn on : 25.7233
Width : 3.308
Height : 10.023
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ampl
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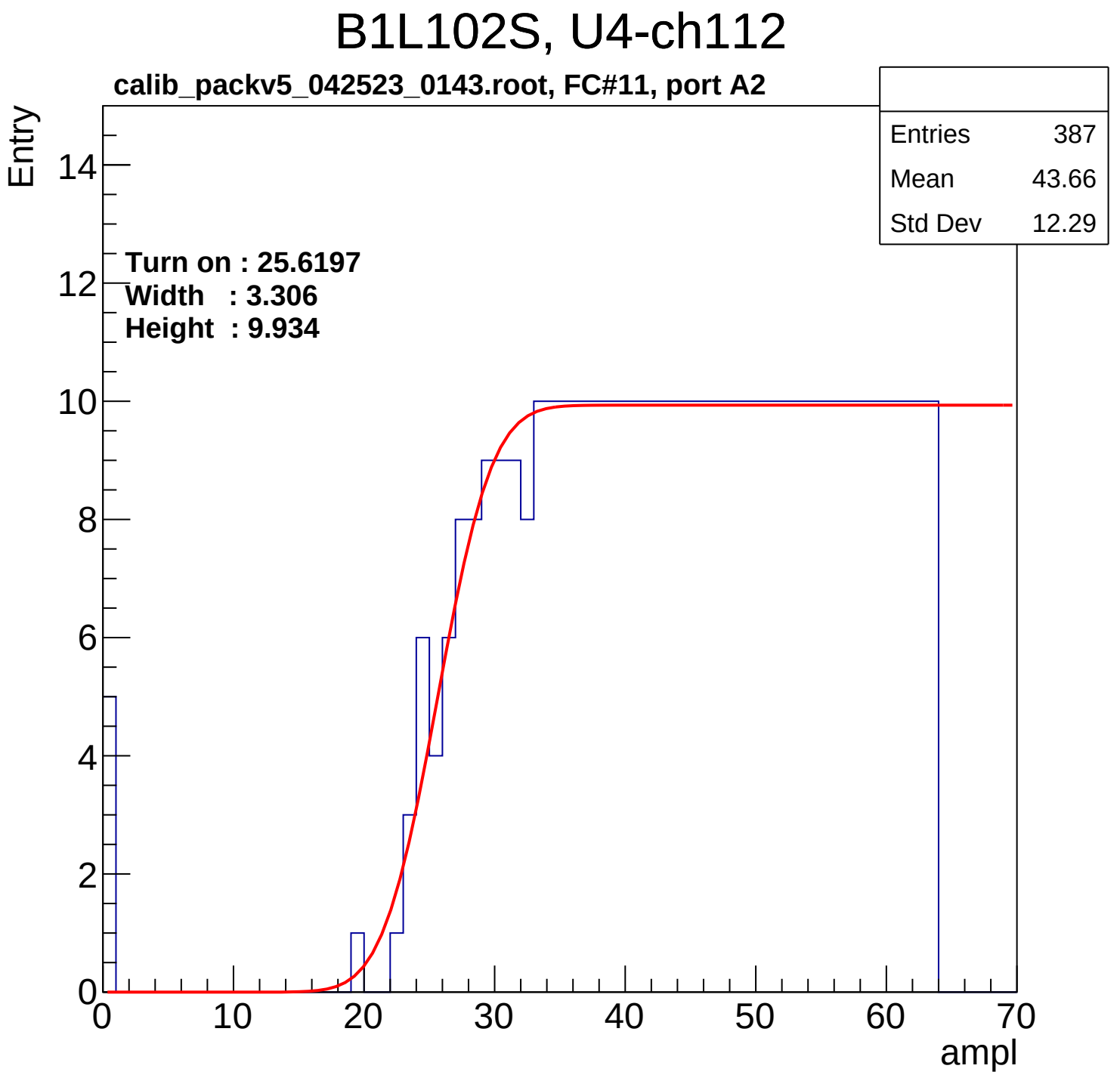
B1L102S, U4-ch112
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 43.66
Std Dev 12.29
Turn on : 25.6197
Width : 3.306
Height : 9.934
Entry
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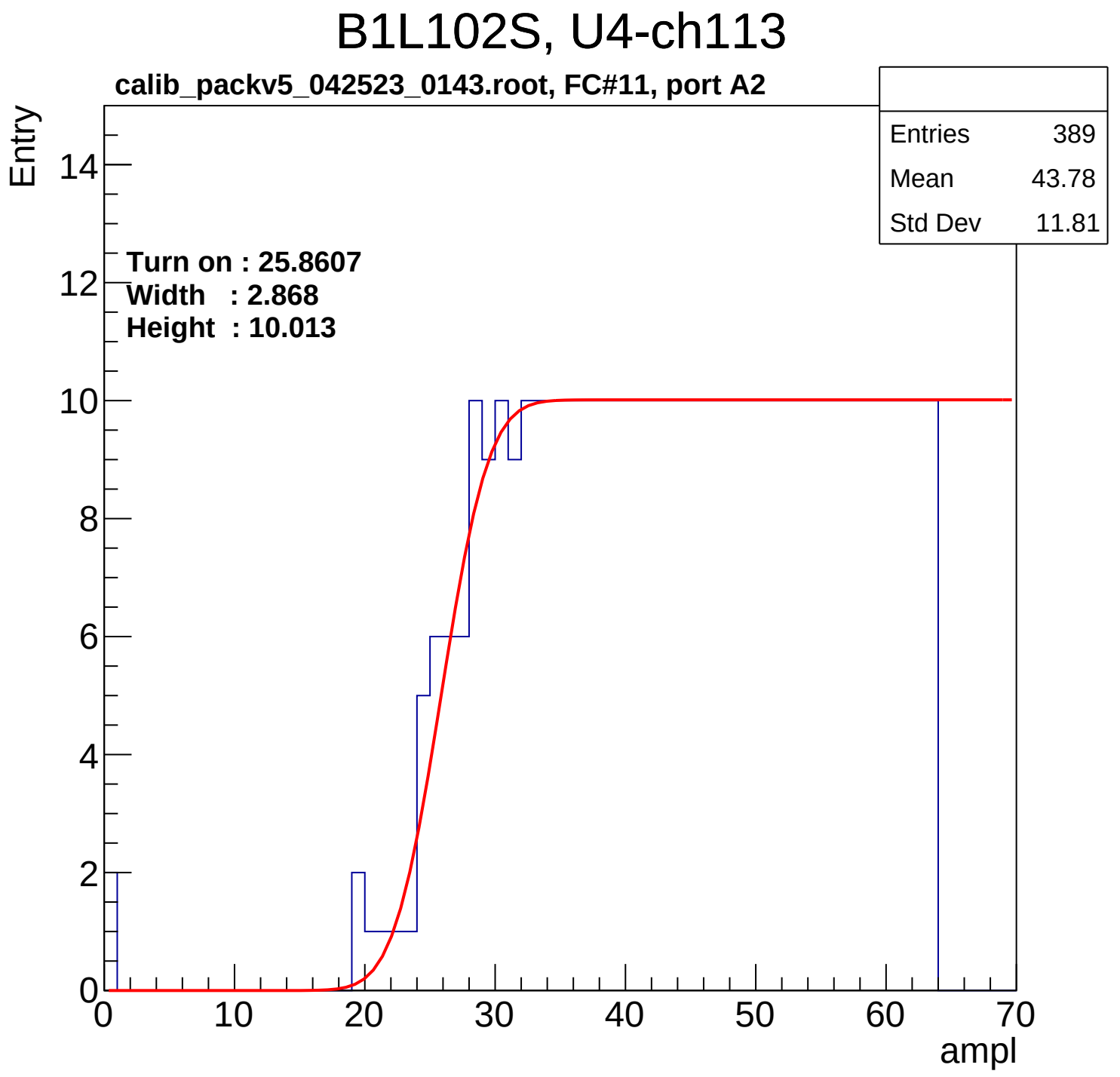
B1L102S, U4-ch113
calib_packv5_042523_0143.root, FC#11, port A2
Entries 389
Mean 43.78
Std Dev 11.81
Turn on : 25.8607
Width : 2.868
Height : 10.013
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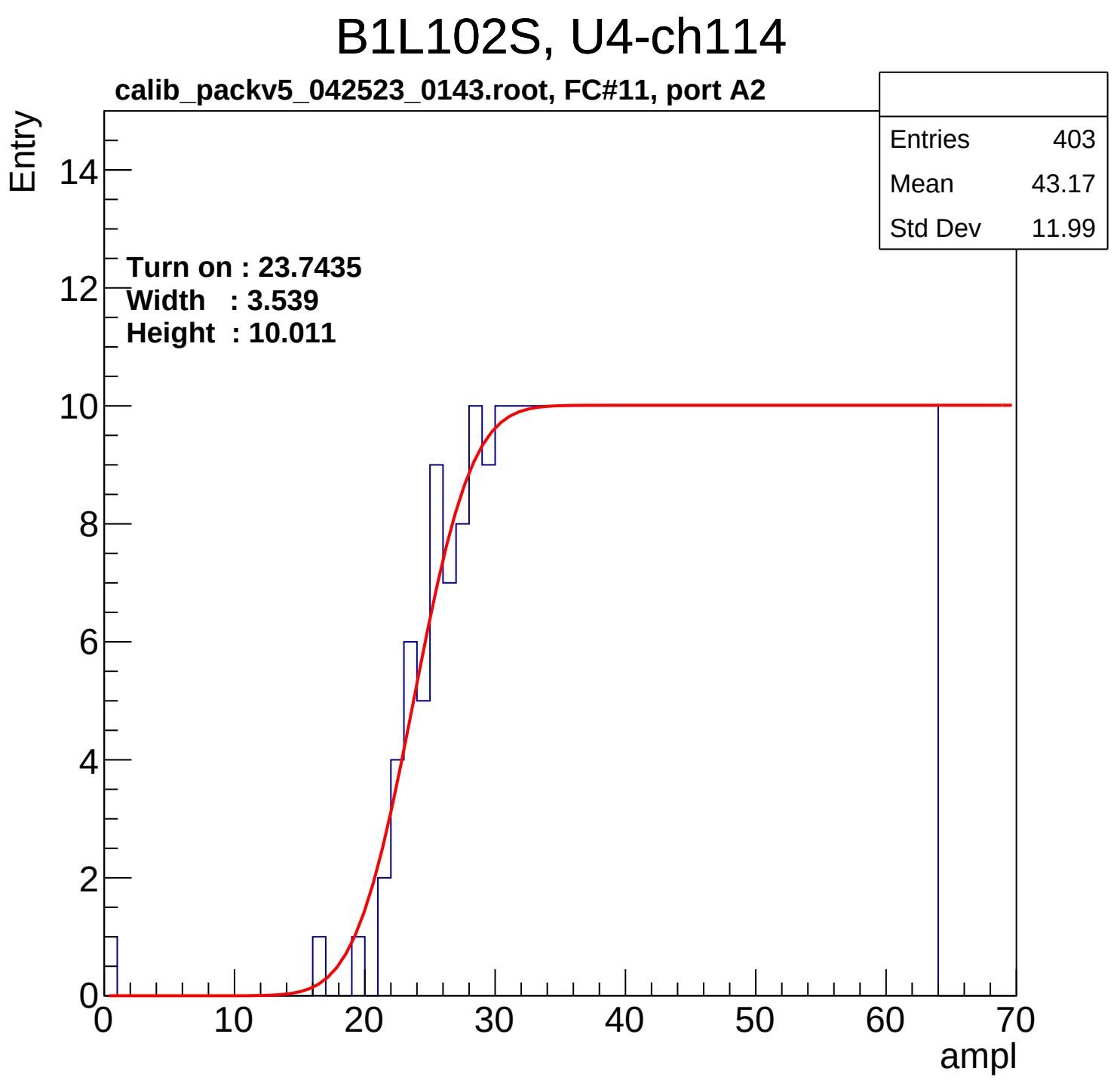
B1L102S, U4-ch114
calib_packv5_042523_0143.root, FC#11, port A2
Entries 403
Mean 43.17
Std Dev 11.99
Turn on : 23.7435
Width : 3.539
Height : 10.011
Entry
ampl
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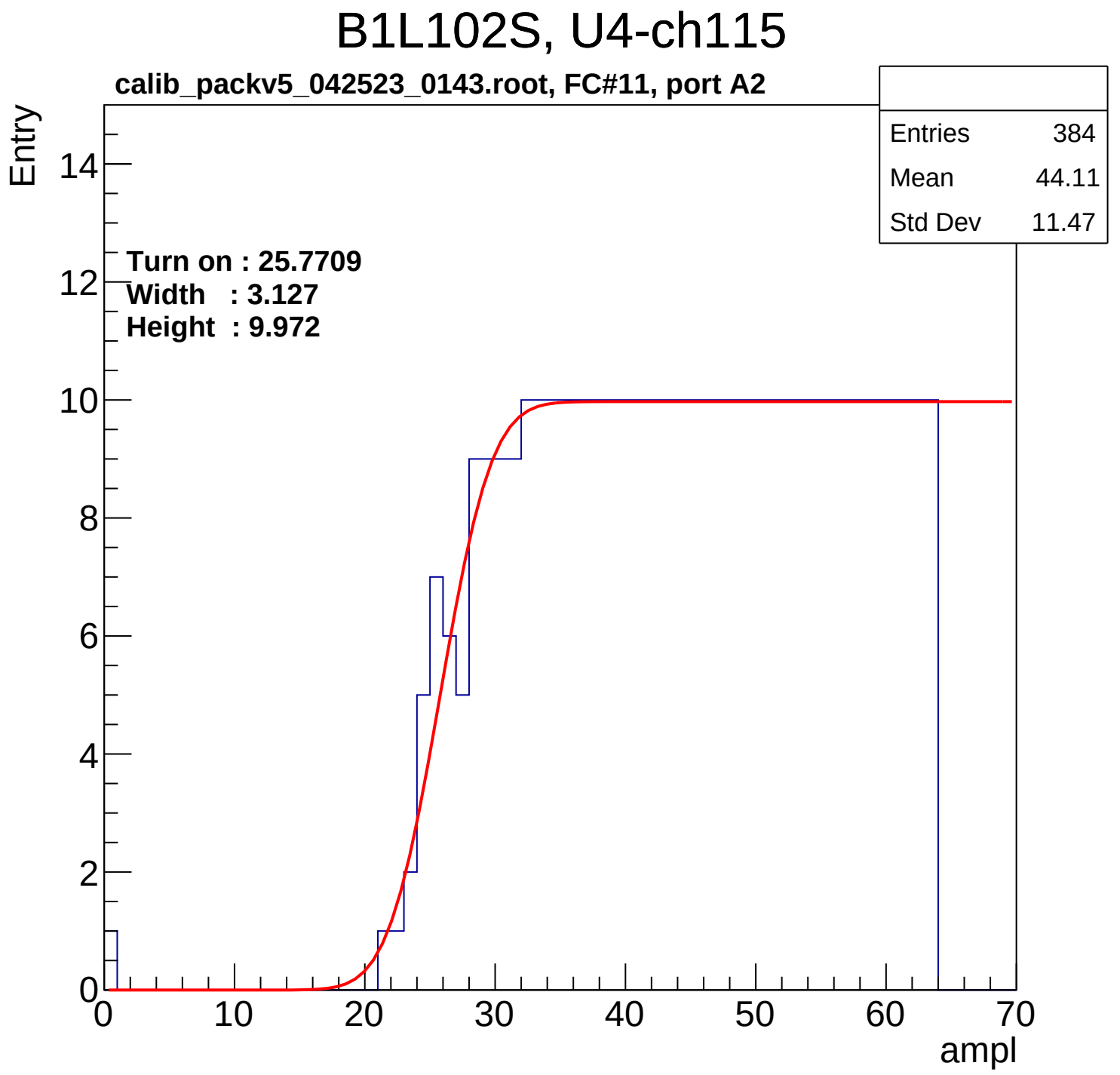
B1L102S, U4-ch115
calib_packv5_042523_0143.root, FC#11, port A2
Entries 384
Mean 44.11
Std Dev 11.47
Turn on : 25.7709
Width : 3.127
Height : 9.972
Entry
ampl
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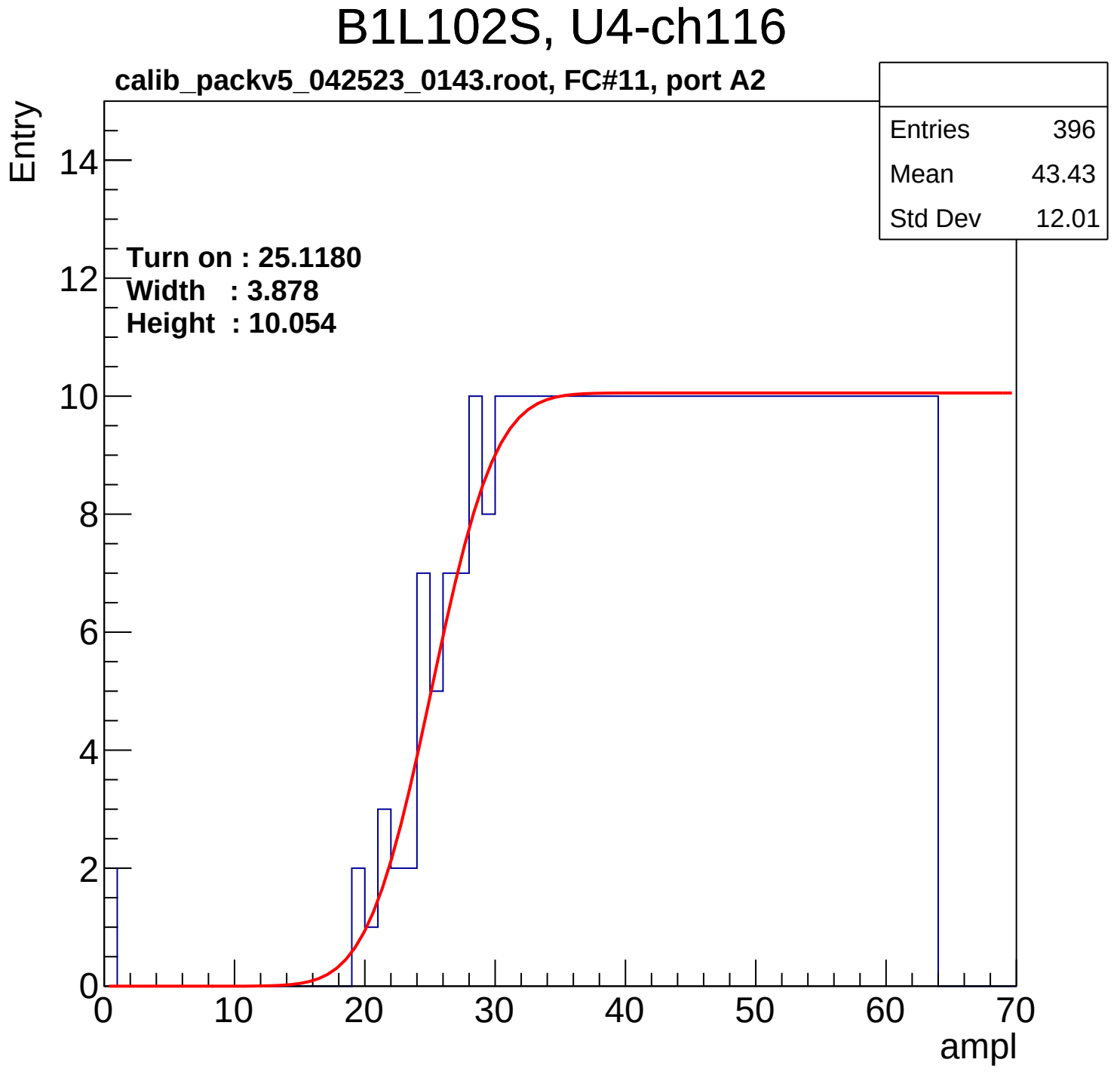
B1L102S, U4-ch116
calib_packv5_042523_0143.root, FC#11, port A2
Entries 396
Mean 43.43
Std Dev 12.01
Turn on : 25.1180
Width : 3.878
Height : 10.054
Entry
ampl
0
2
4
6
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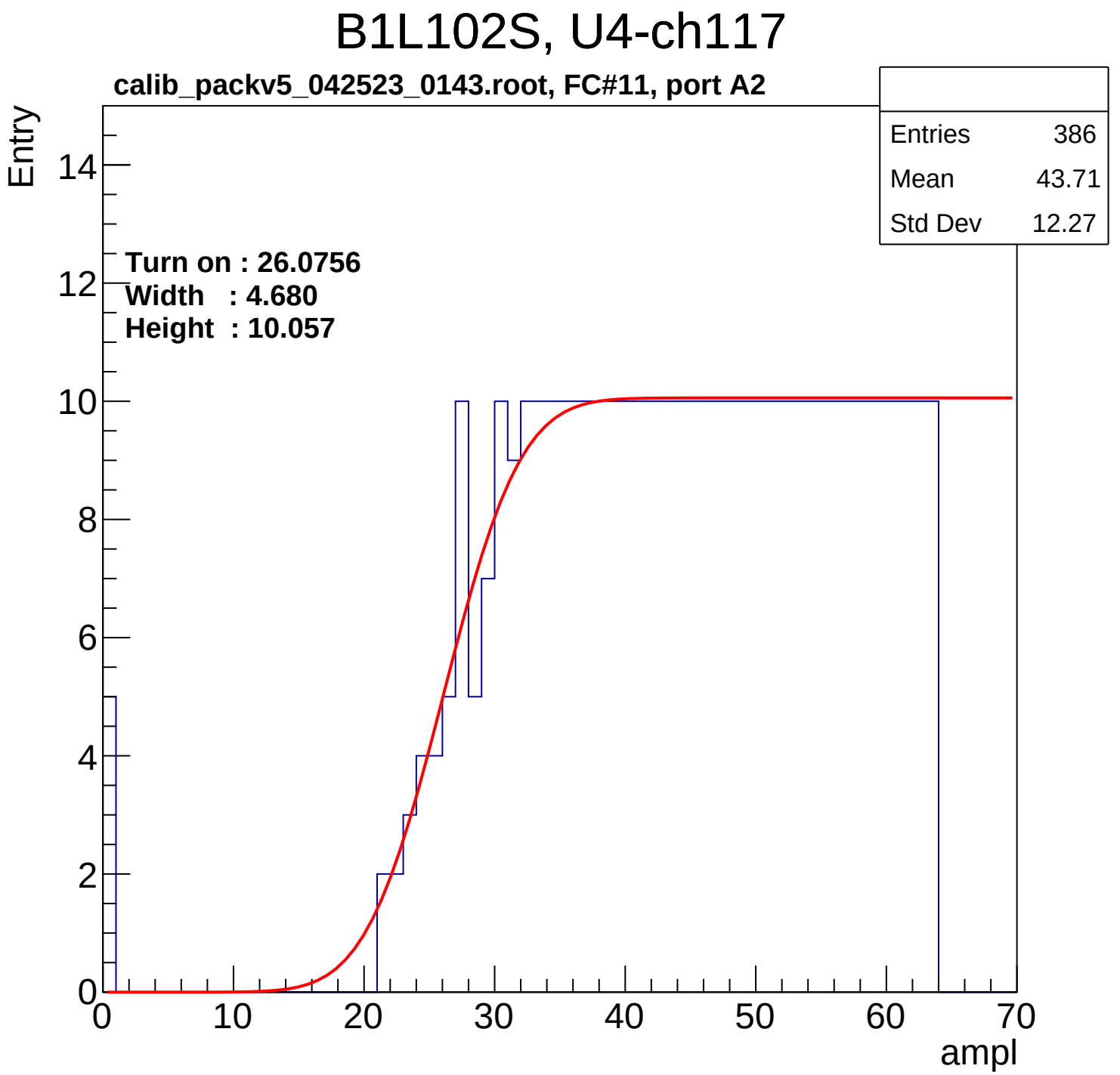
B1L102S, U4-ch117
calib_packv5_042523_0143.root, FC#11, port A2
Entries 386
Mean 43.71
Std Dev 12.27
Turn on : 26.0756
Width : 4.680
Height : 10.057
Entry
ampl
0
2
4
6
8
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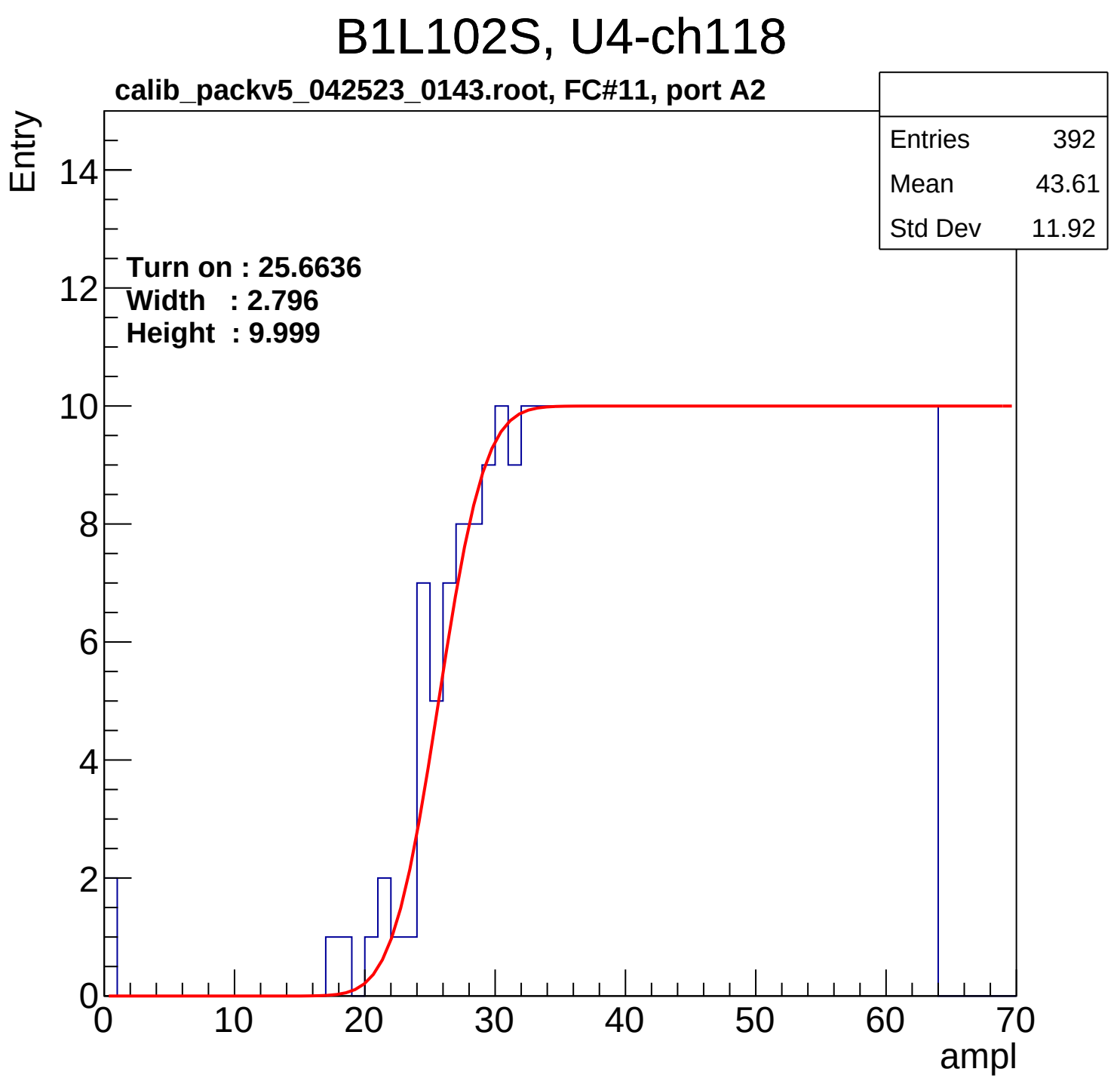
B1L102S, U4-ch118
calib_packv5_042523_0143.root, FC#11, port A2
Entries 392
Mean 43.61
Std Dev 11.92
Turn on : 25.6636
Width : 2.796
Height : 9.999
Entry
ampl
0
2
4
6
8
10
12
14
0
10
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40
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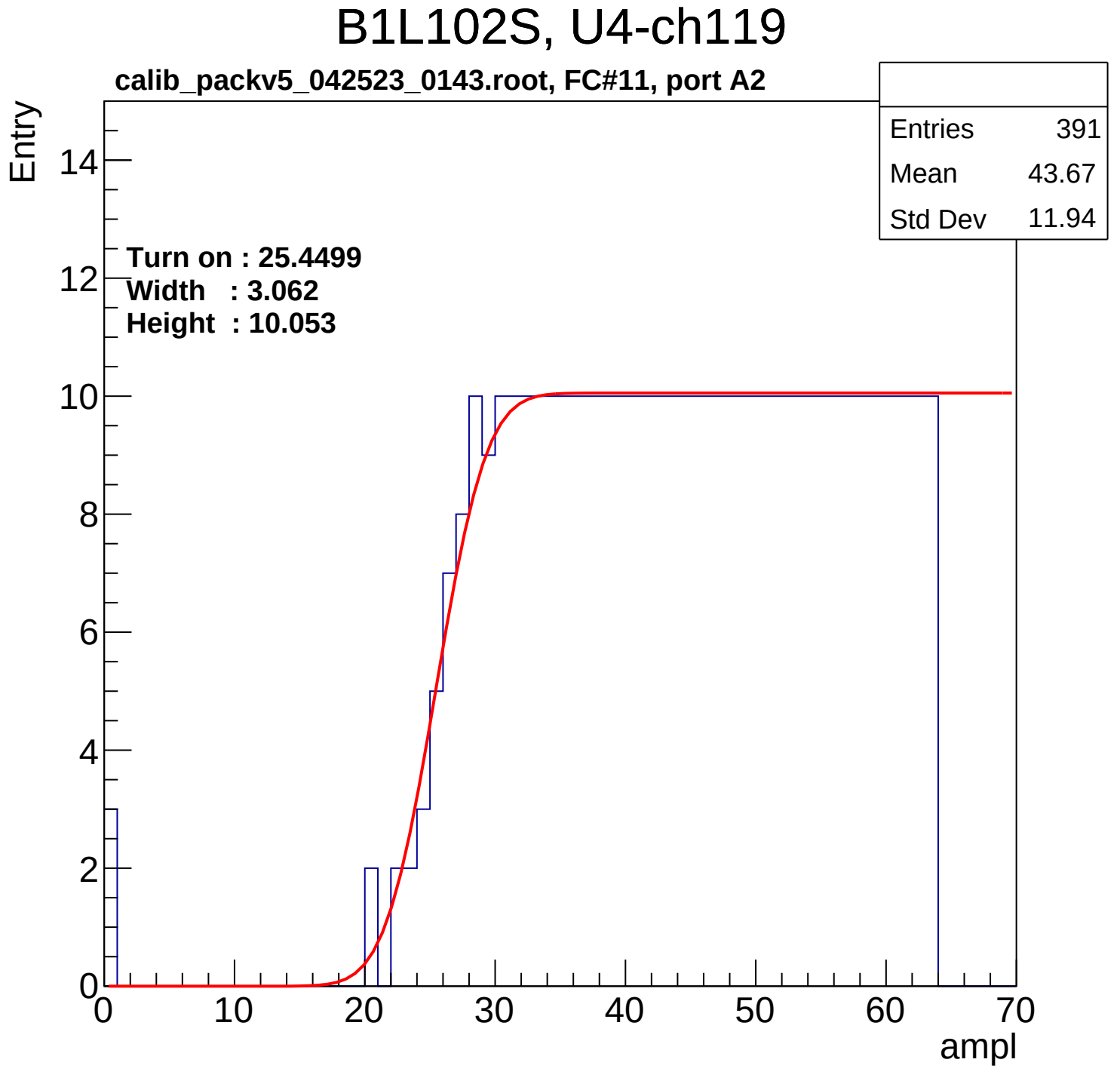
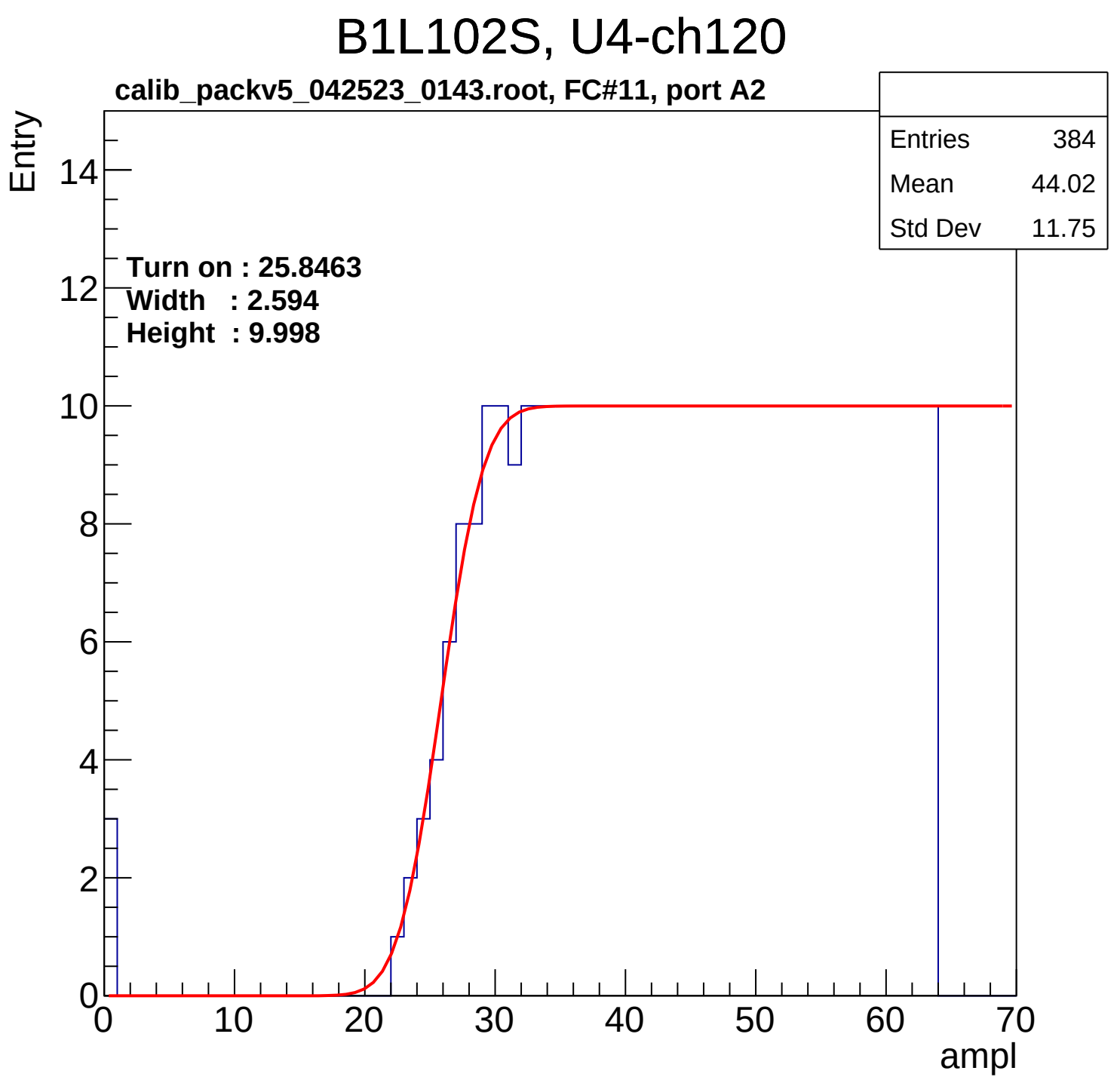

B1L102S, U4-ch119
calib_packv5_042523_0143.root, FC#11, port A2
Entries 391
Mean 43.67
Std Dev 11.94
Turn on : 25.4499
Width : 3.062
Height : 10.053
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L102S, U4-ch120
calib_packv5_042523_0143.root, FC#11, port A2
Entries 384
Mean 44.02
Std Dev 11.75
Turn on : 25.8463
Width : 2.594
Height : 9.998
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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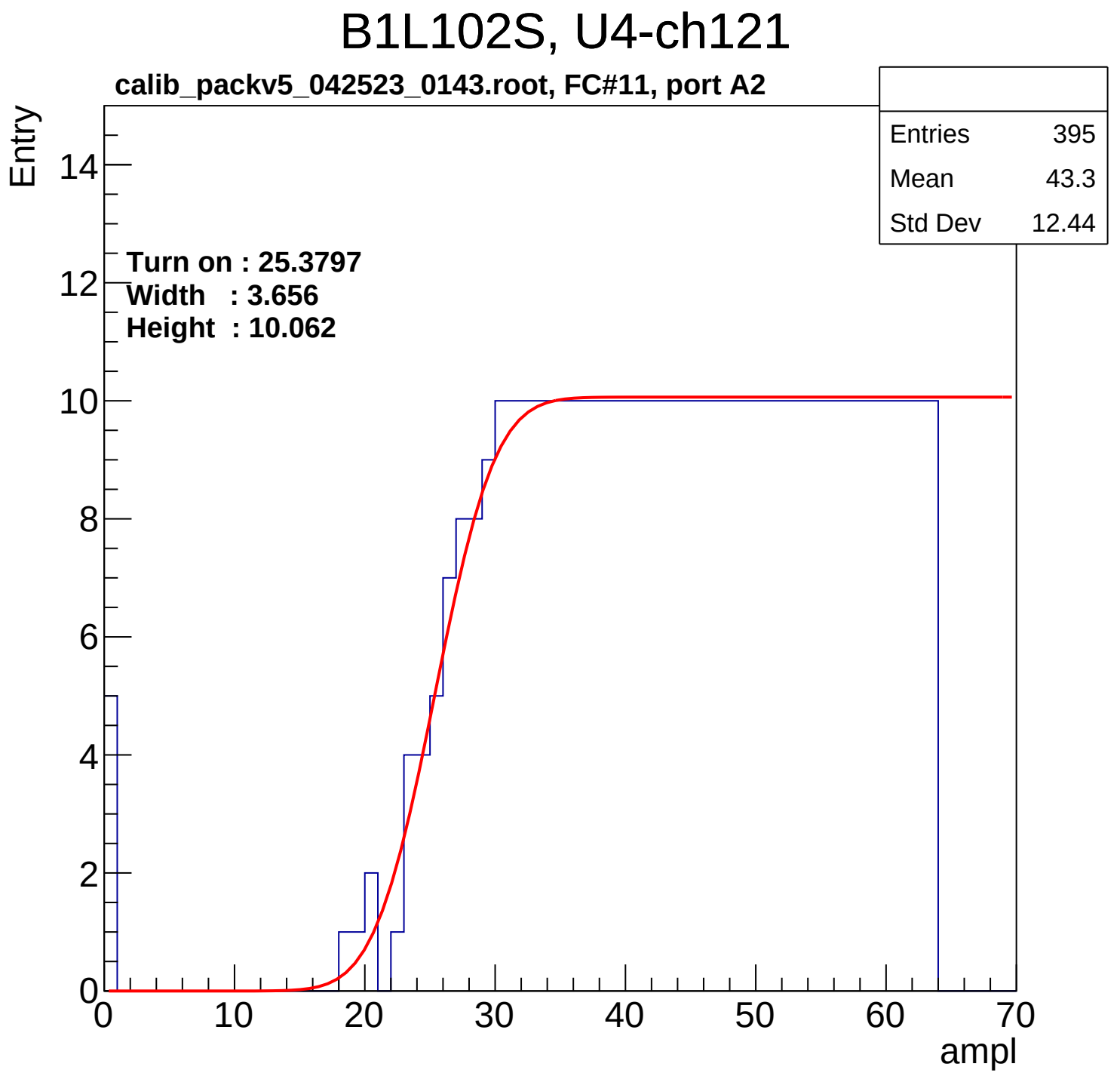
B1L102S, U4-ch121
calib_packv5_042523_0143.root, FC#11, port A2
Entries 395
Mean 43.3
Std Dev 12.44
Turn on : 25.3797
Width : 3.656
Height : 10.062
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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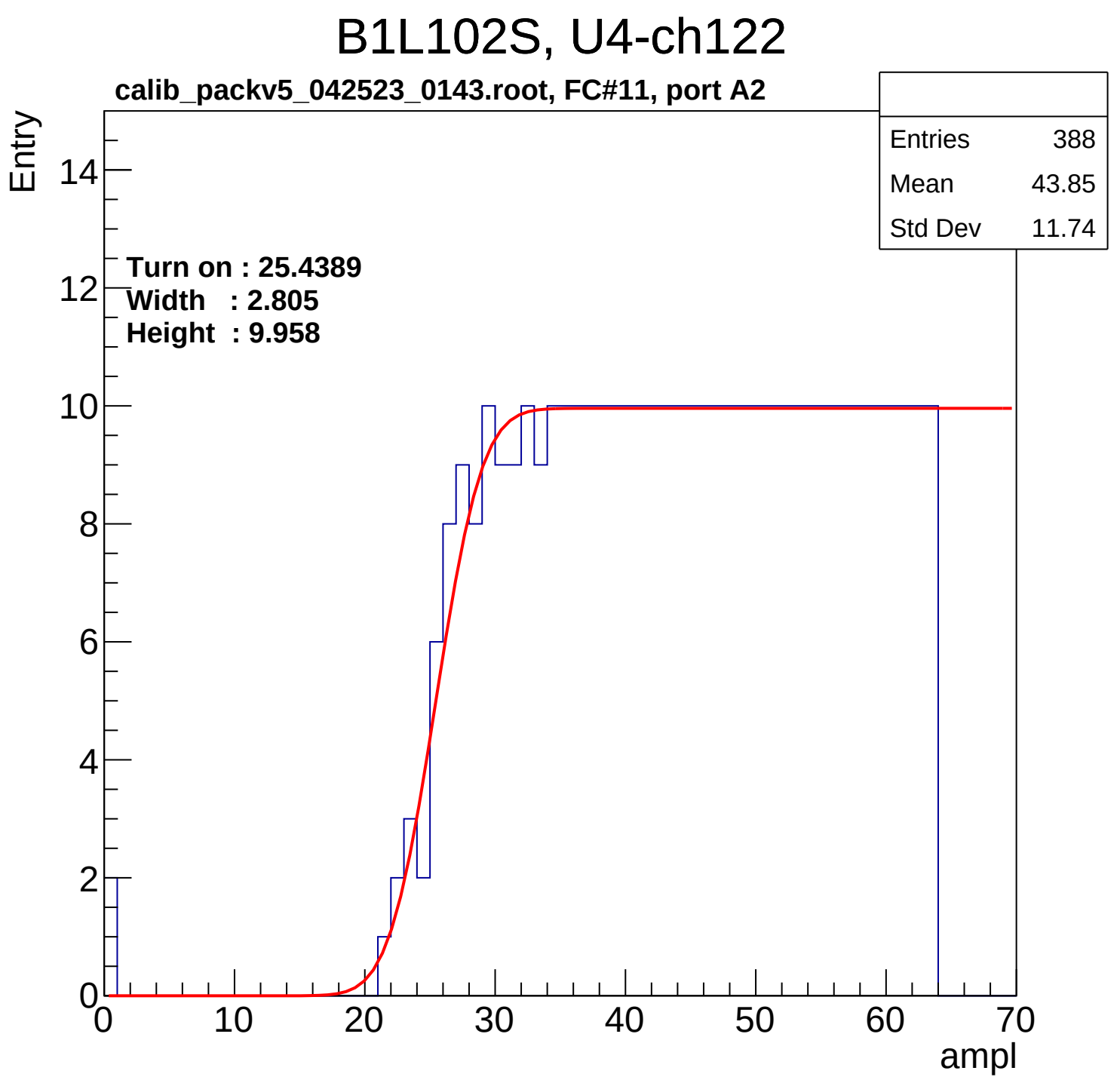
B1L102S, U4-ch122
calib_packv5_042523_0143.root, FC#11, port A2
Entries 388
Mean 43.85
Std Dev 11.74
Turn on : 25.4389
Width : 2.805
Height : 9.958
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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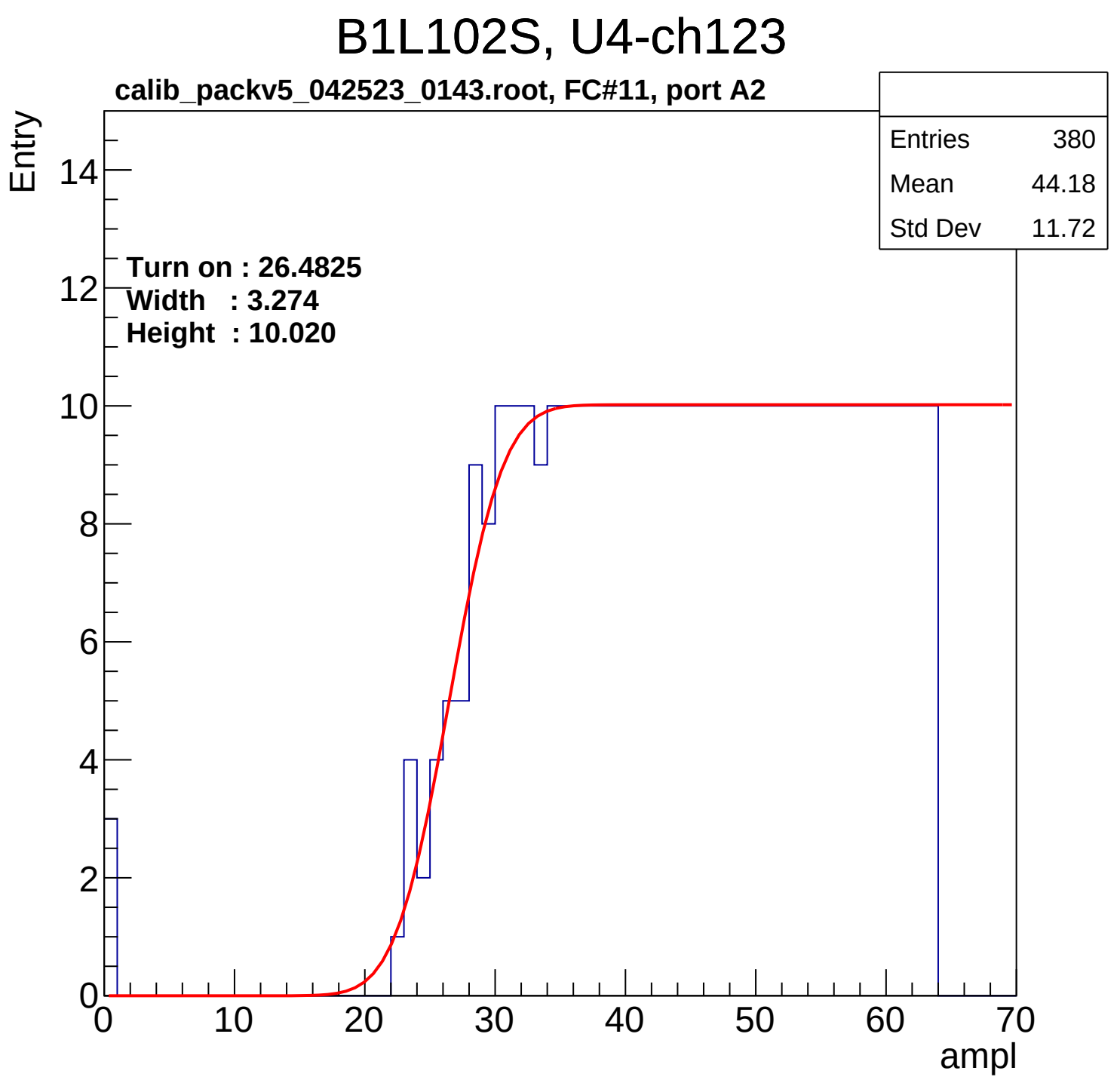
B1L102S, U4-ch123
calib_packv5_042523_0143.root, FC#11, port A2
Entries 380
Mean 44.18
Std Dev 11.72
Turn on : 26.4825
Width : 3.274
Height : 10.020
Entry
ampl
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2
4
6
8
10
12
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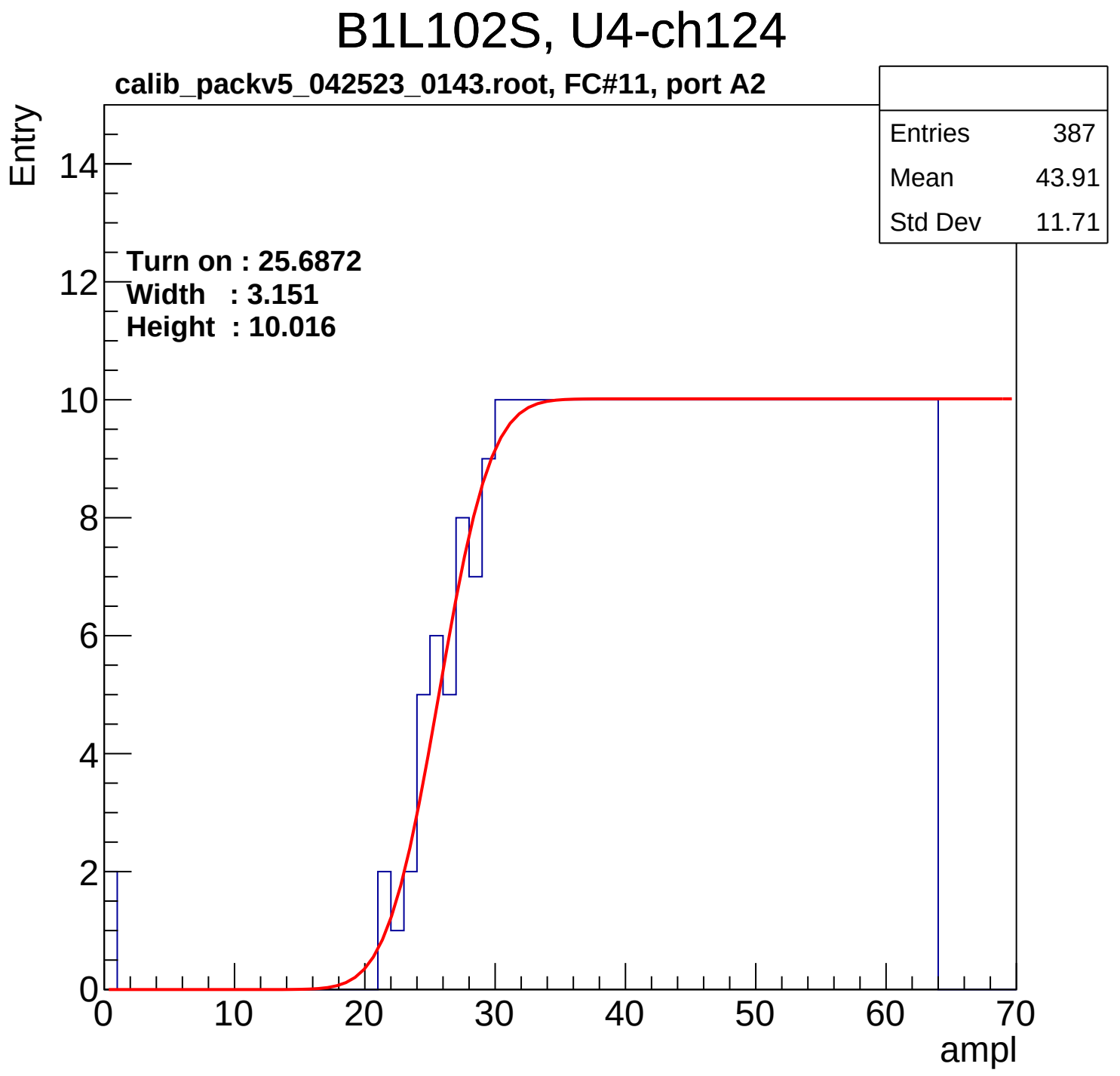
10
20
30
40
50
60
70


B1L102S, U4-ch124
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 43.91
Std Dev 11.71
Turn on : 25.6872
Width : 3.151
Height : 10.016
Entry
ampl
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2
4
6
8
10
12
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20
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40
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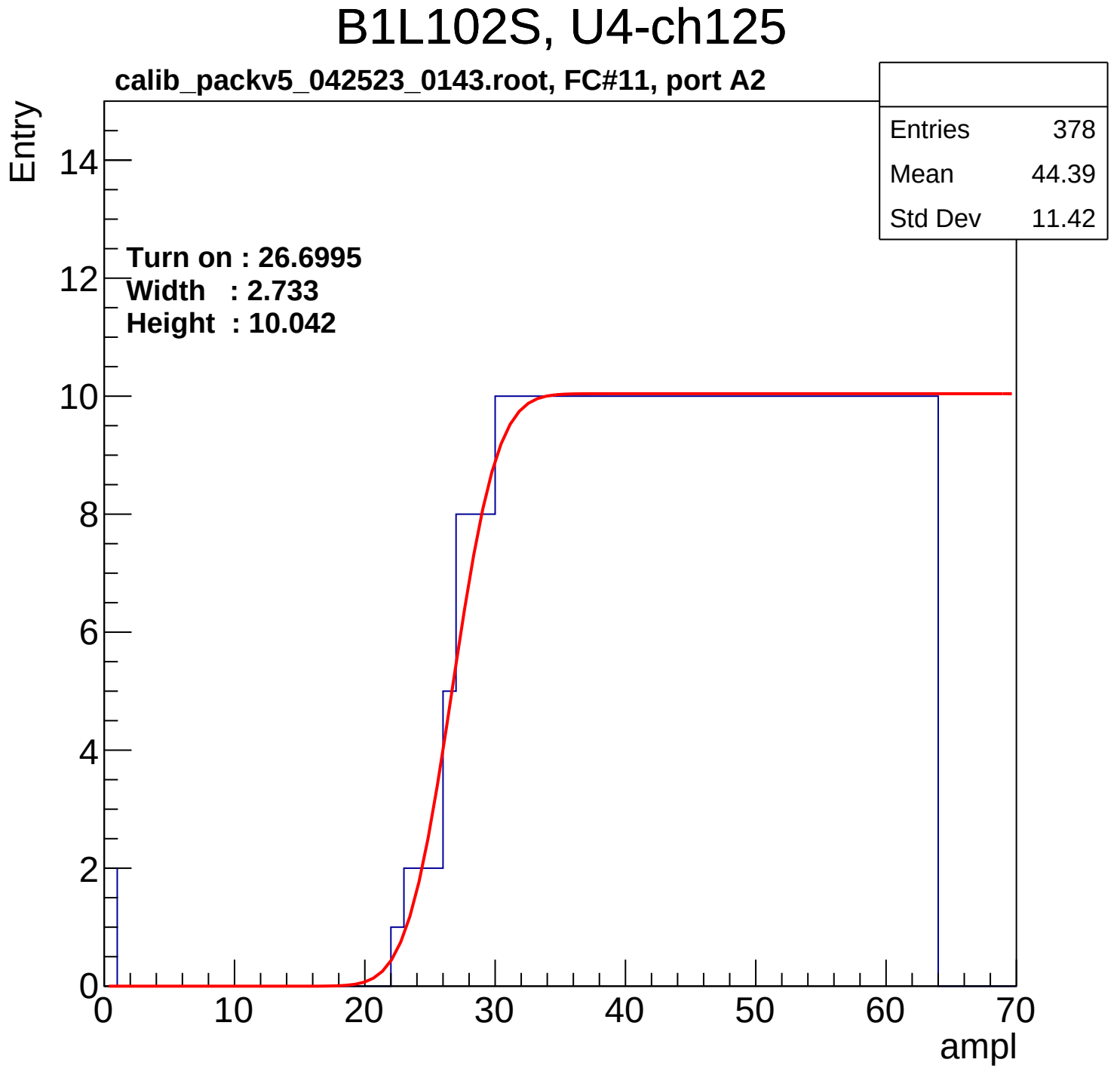
60
70


B1L102S, U4-ch125
calib_packv5_042523_0143.root, FC#11, port A2
Entries 378
Mean 44.39
Std Dev 11.42
Turn on : 26.6995
Width : 2.733
Height : 10.042
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
50
60
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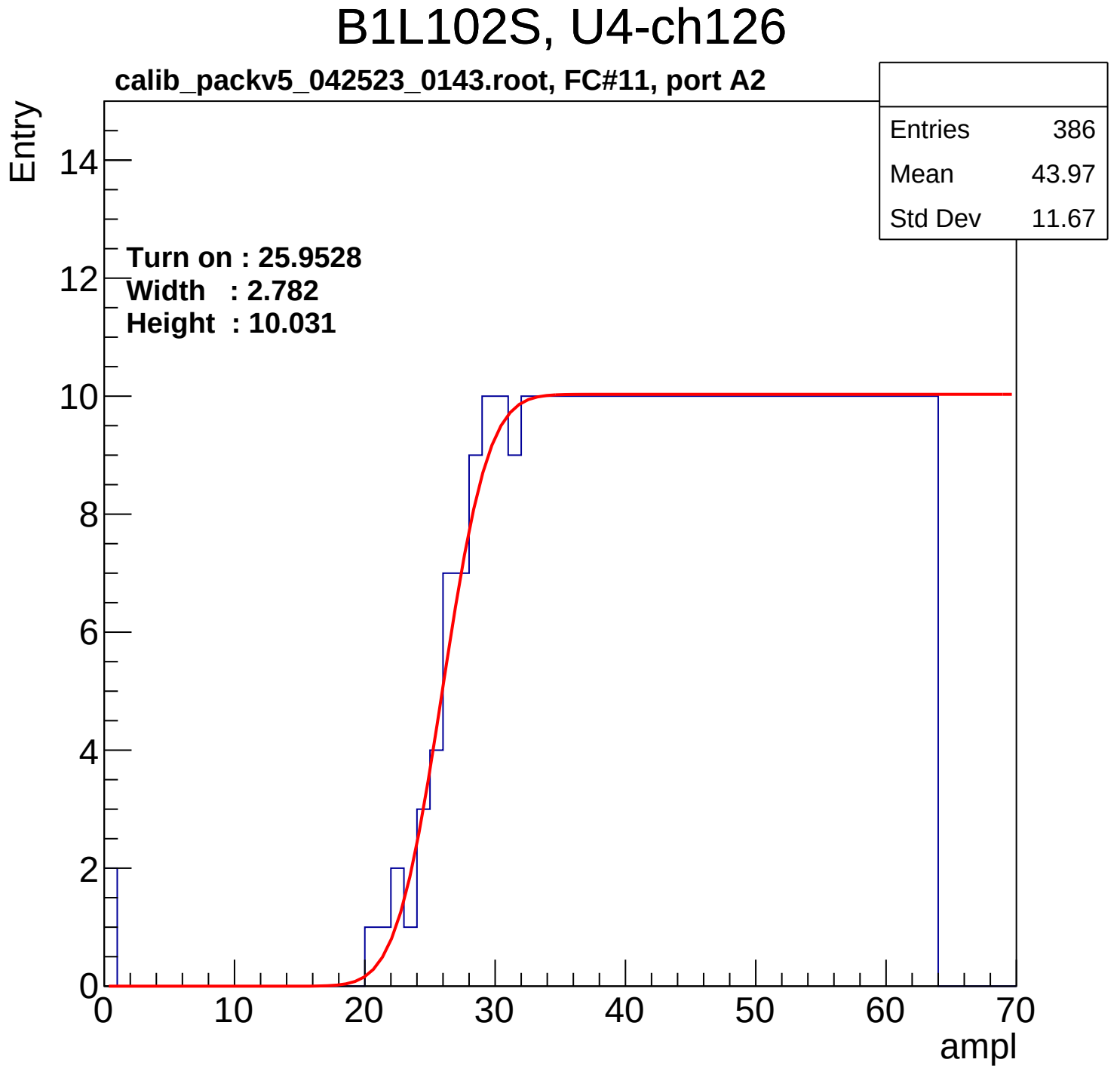
B1L102S, U4-ch126
calib_packv5_042523_0143.root, FC#11, port A2
Entries 386
Mean 43.97
Std Dev 11.67
Turn on : 25.9528
Width : 2.782
Height : 10.031
Entry
ampl
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2
4
6
8
10
12
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0
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20
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40
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60
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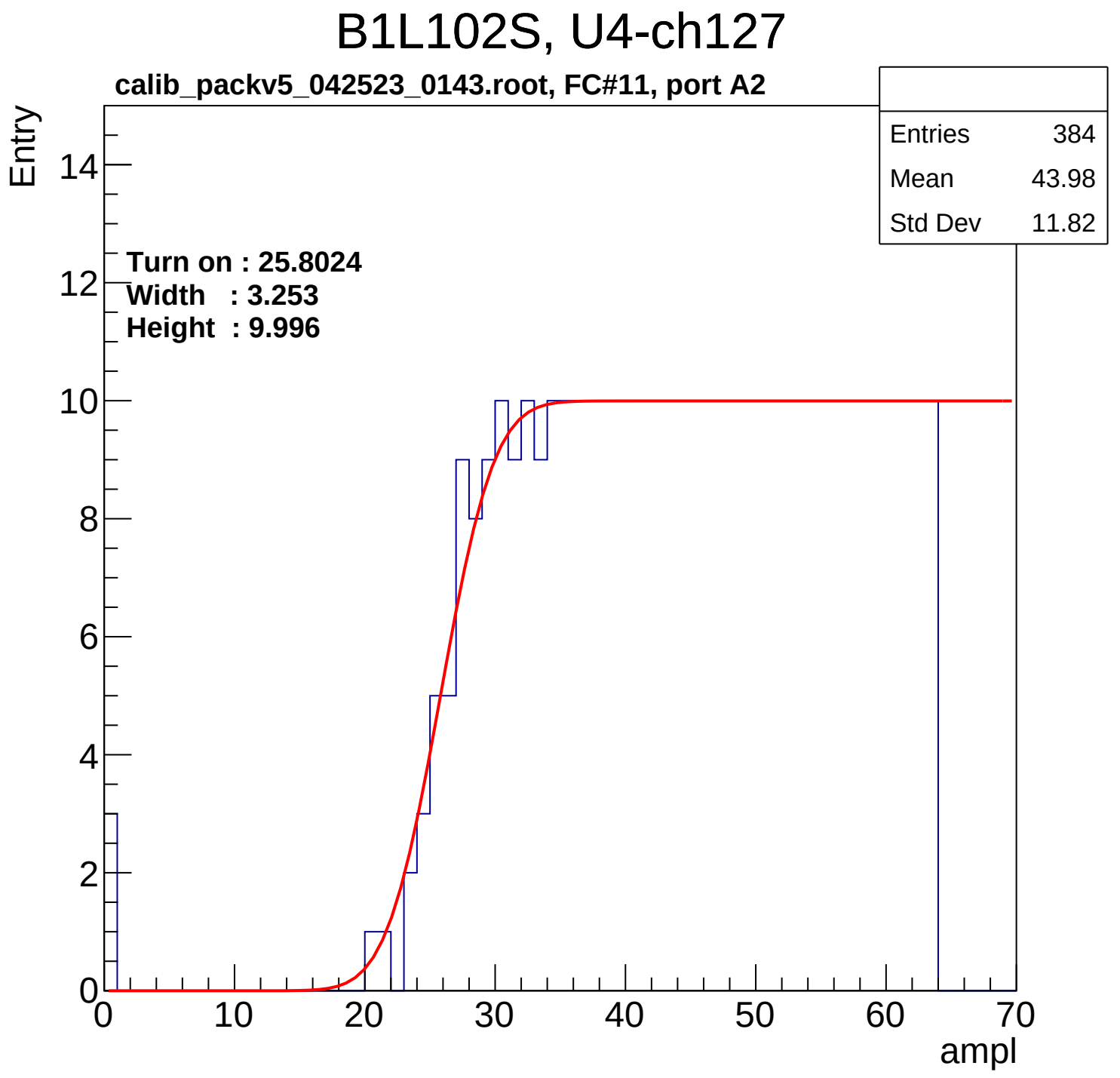
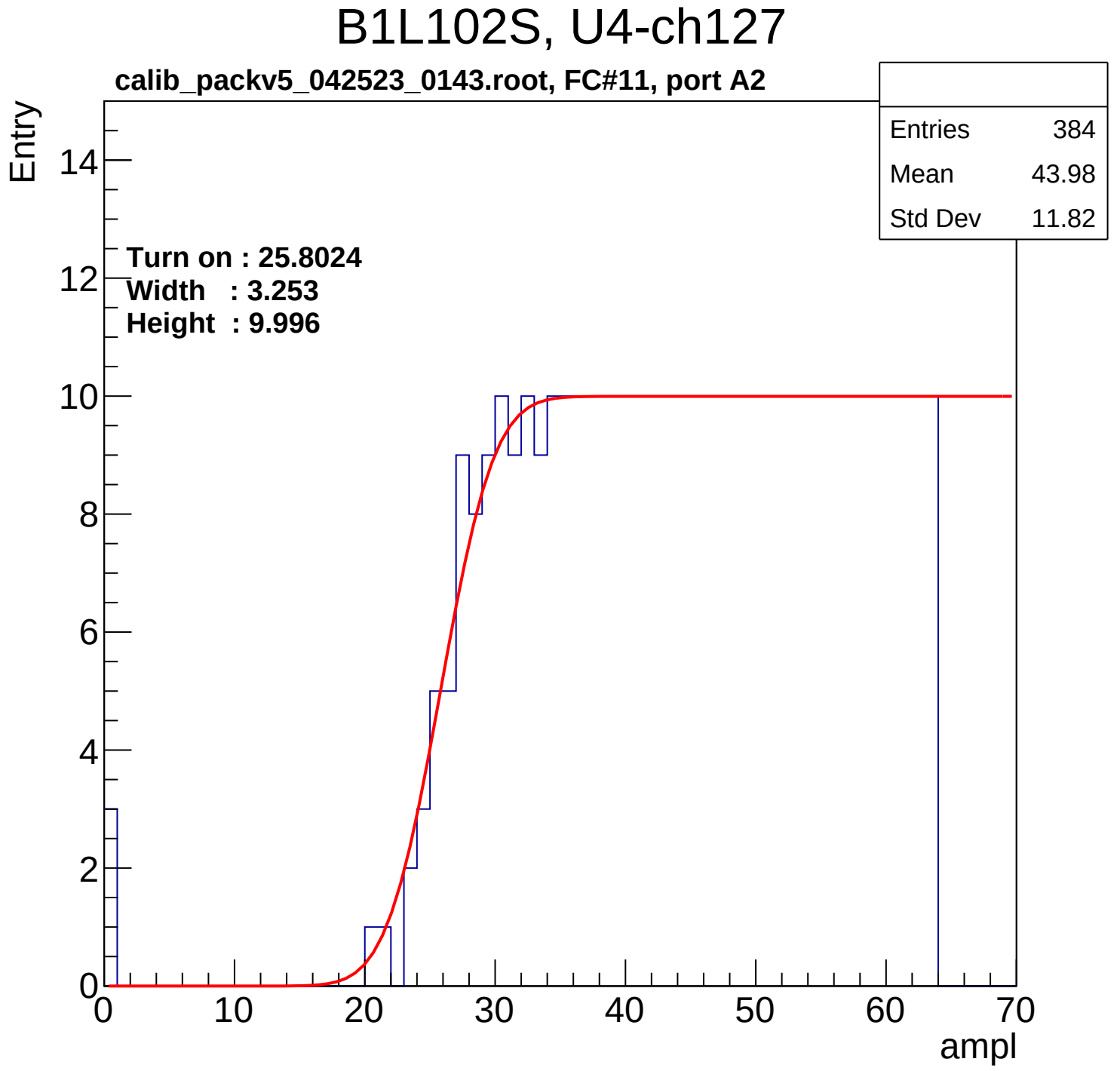

B1L102S, U4-ch127
calib_packv5_042523_0143.root, FC#11, port A2
Entries 384
Mean 43.98
Std Dev 11.82
Turn on : 25.8024
Width : 3.253
Height : 9.996
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L102S, U4-ch127
calib_packv5_042523_0143.root, FC#11, port A2
Entries 384
Mean 43.98
Std Dev 11.82
Turn on : 25.8024
Width : 3.253
Height : 9.996
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70