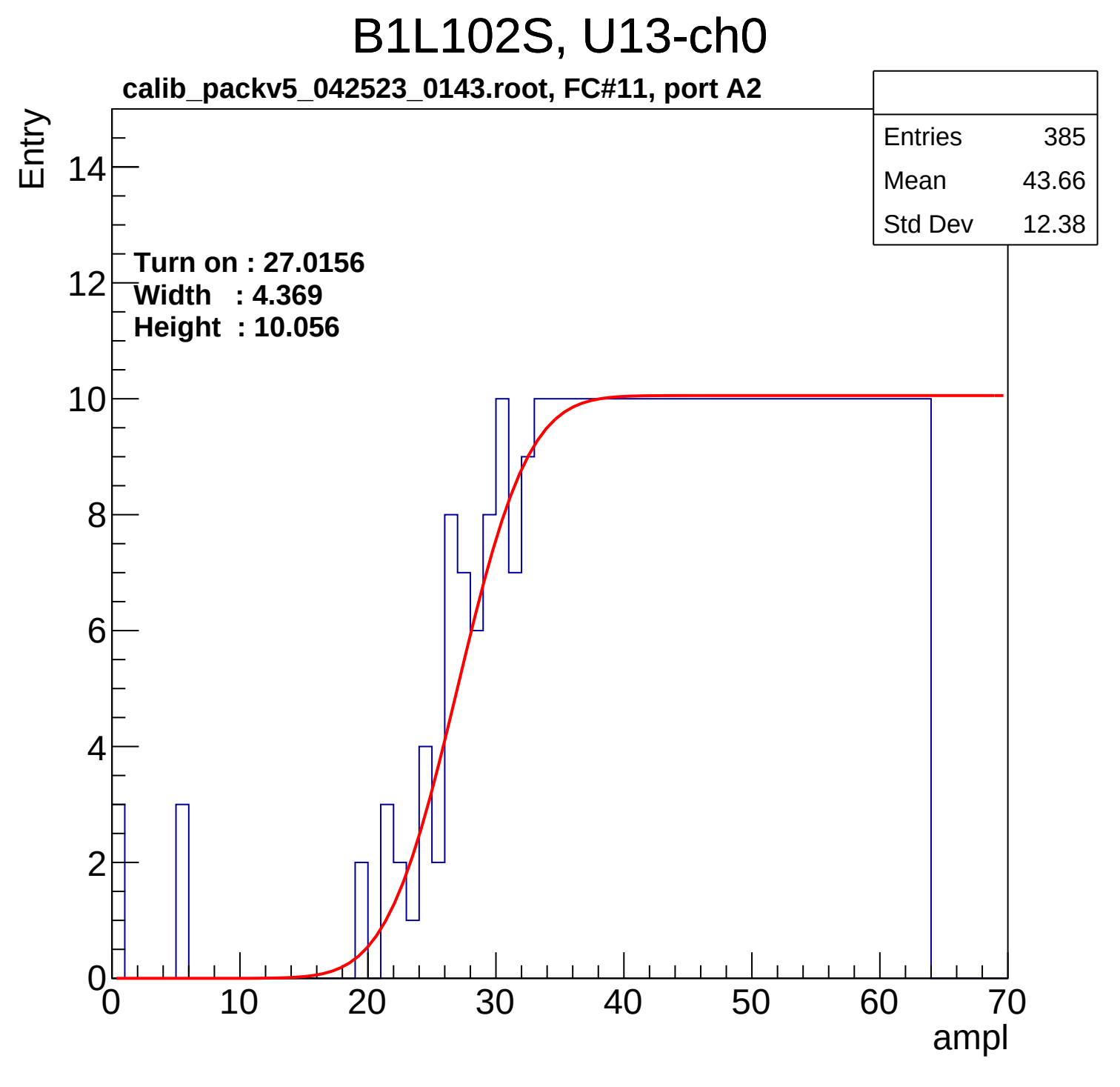
B1L102S, U13-ch0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 43.66
Std Dev 12.38
Turn on : 27.0156
Width : 4.369
Height : 10.056
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ampl
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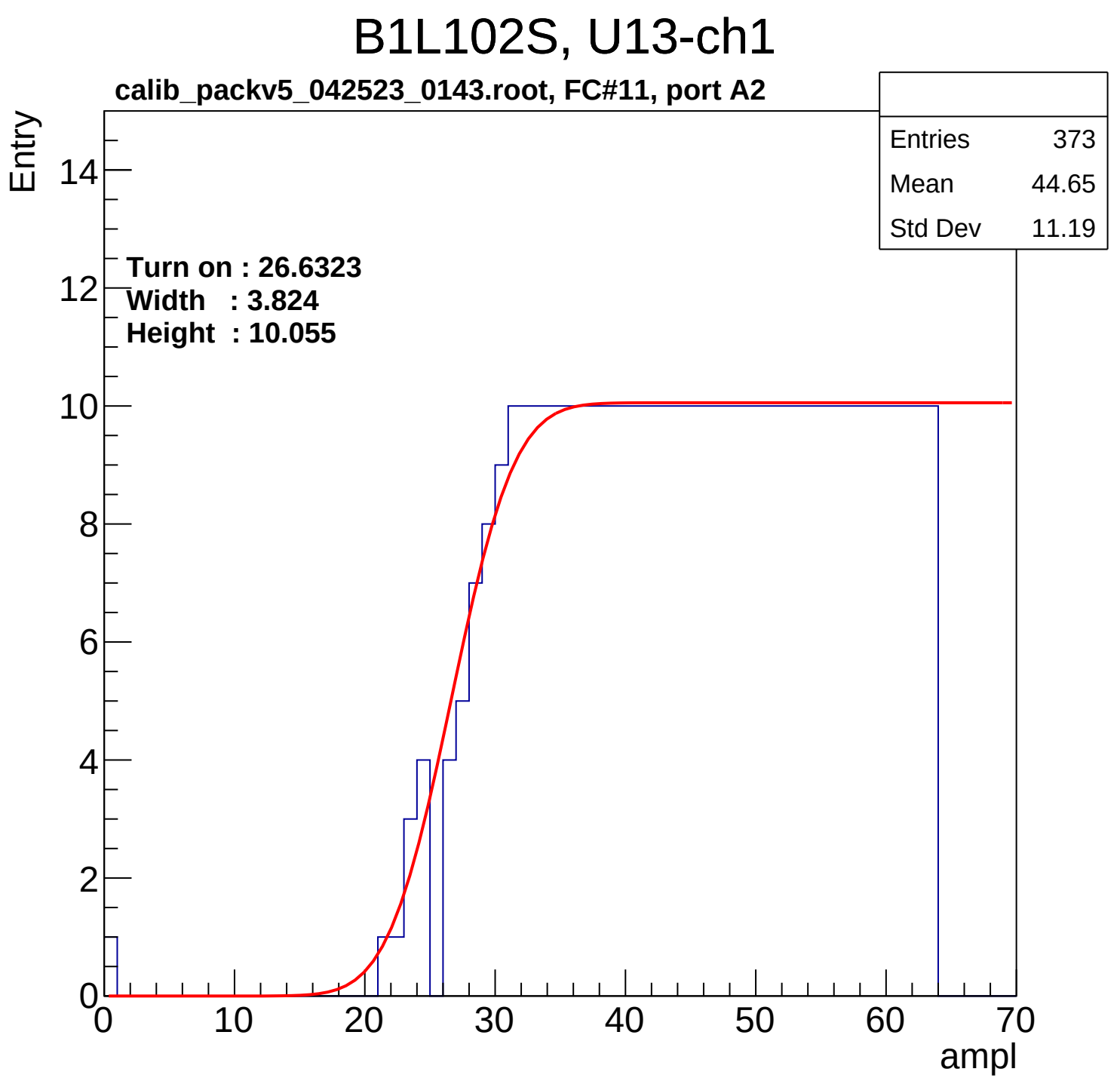
B1L102S, U13-ch1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 373
Mean 44.65
Std Dev 11.19
Turn on : 26.6323
Width : 3.824
Height : 10.055
Entry
ampl
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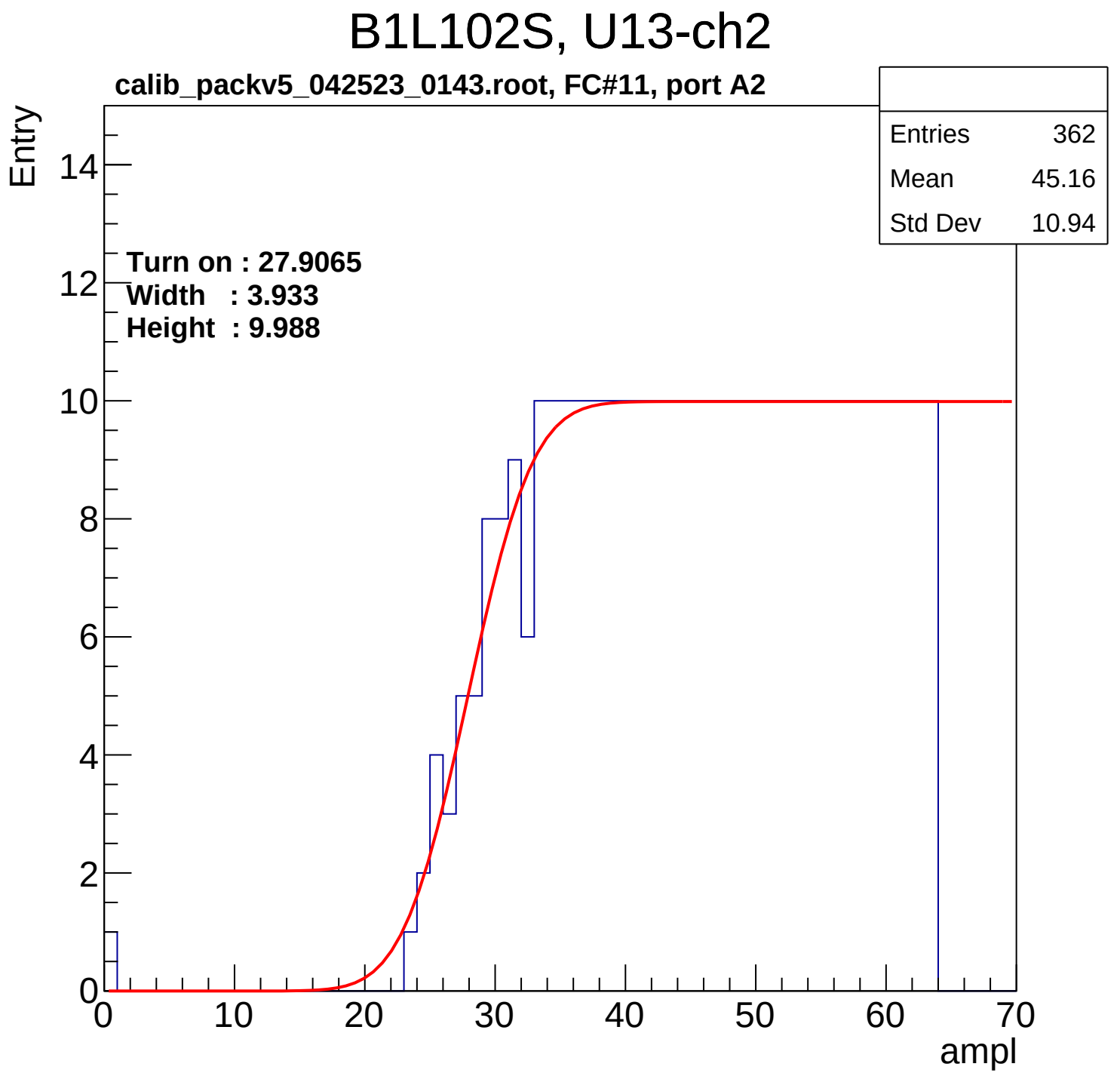
B1L102S, U13-ch2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 362
Mean 45.16
Std Dev 10.94
Turn on : 27.9065
Width : 3.933
Height : 9.988
Entry
ampl
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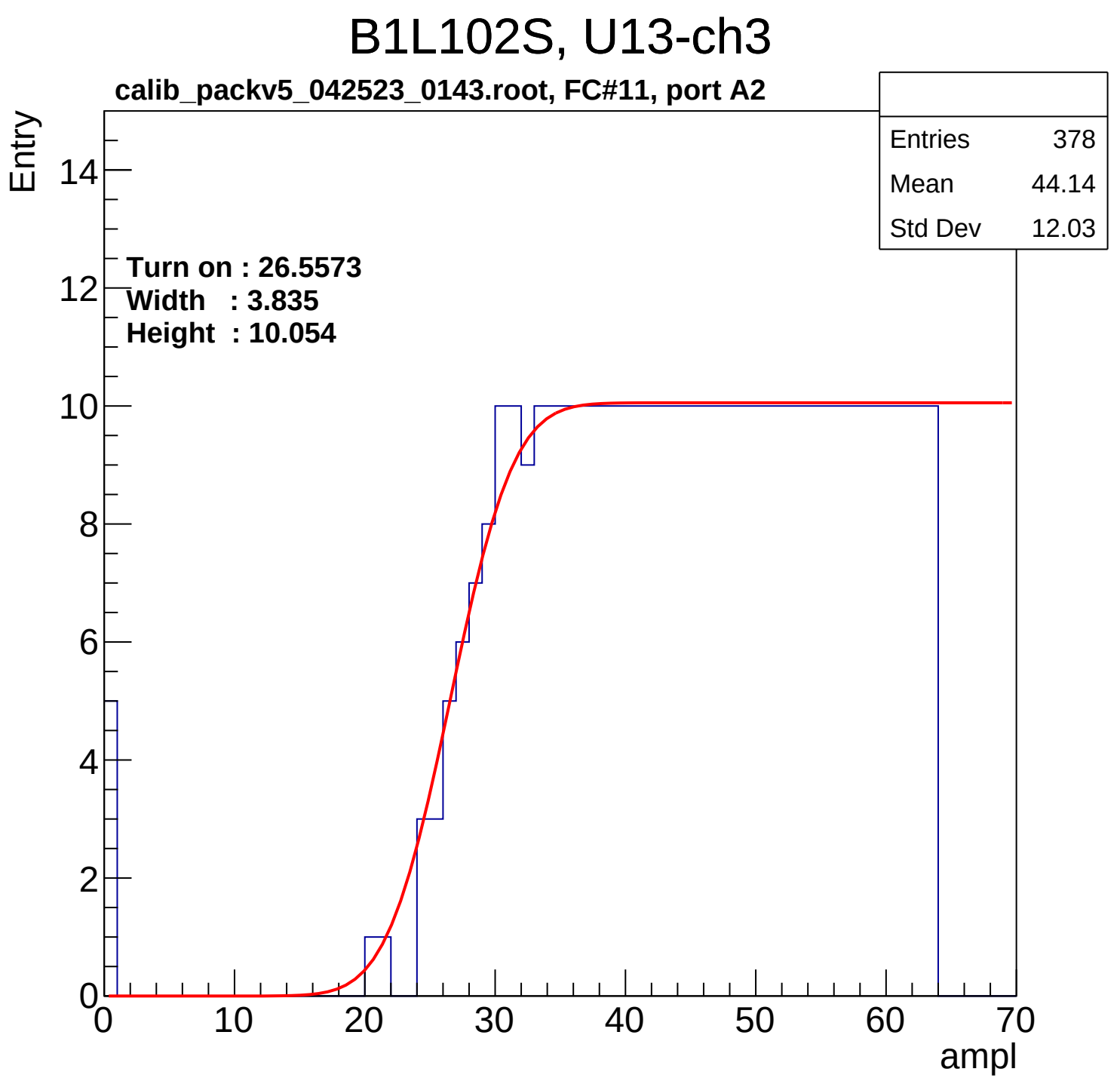
B1L102S, U13-ch3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 378
Mean 44.14
Std Dev 12.03
Turn on : 26.5573
Width : 3.835
Height : 10.054
Entry
ampl
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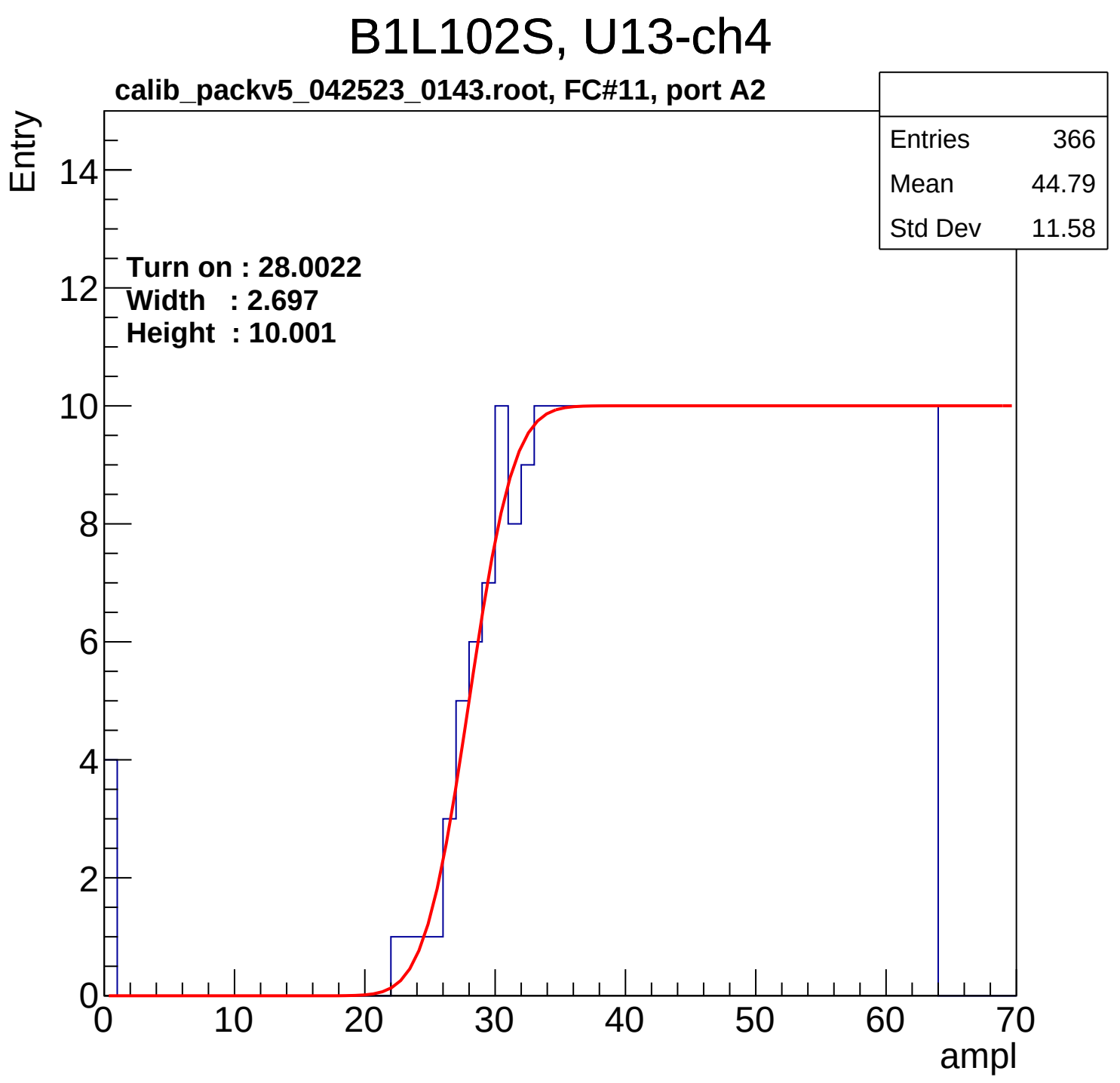
B1L102S, U13-ch4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 366
Mean 44.79
Std Dev 11.58
Turn on : 28.0022
Width : 2.697
Height : 10.001
Entry
ampl
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6
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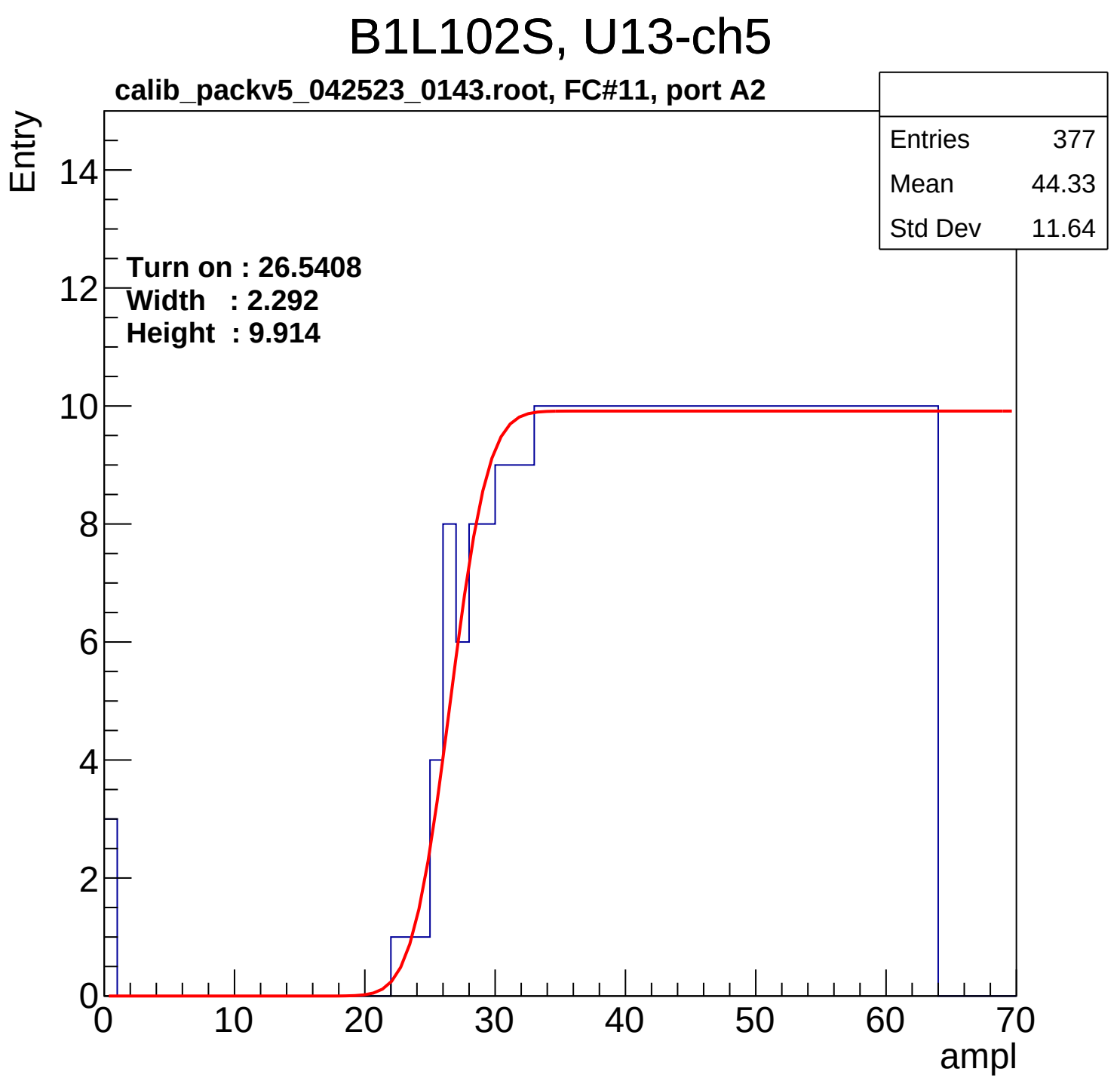
B1L102S, U13-ch5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 377
Mean 44.33
Std Dev 11.64
Turn on : 26.5408
Width : 2.292
Height : 9.914
Entry
ampl
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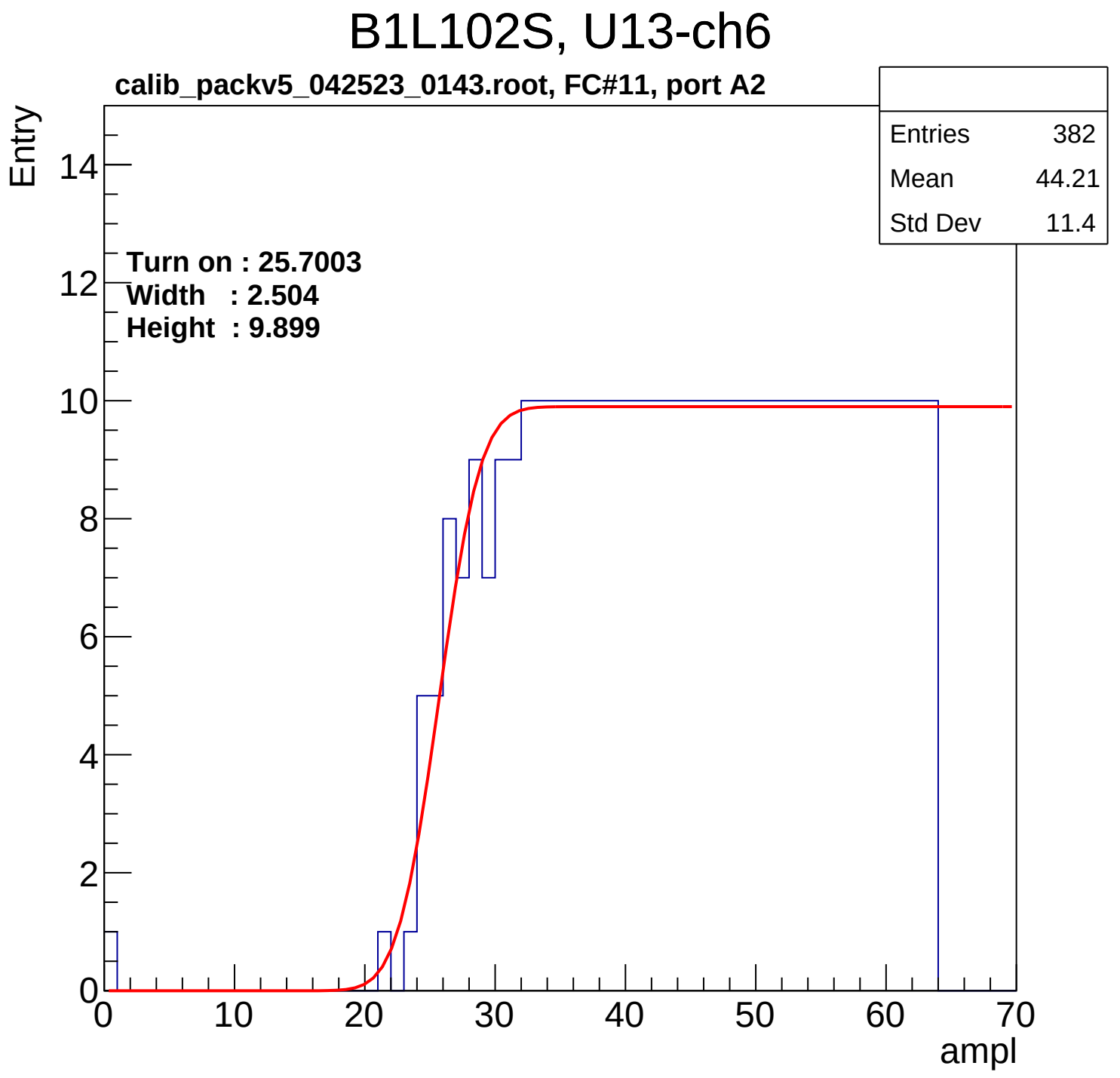
B1L102S, U13-ch6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 382
Mean 44.21
Std Dev 11.4
Turn on : 25.7003
Width : 2.504
Height : 9.899
Entry
ampl
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6
8
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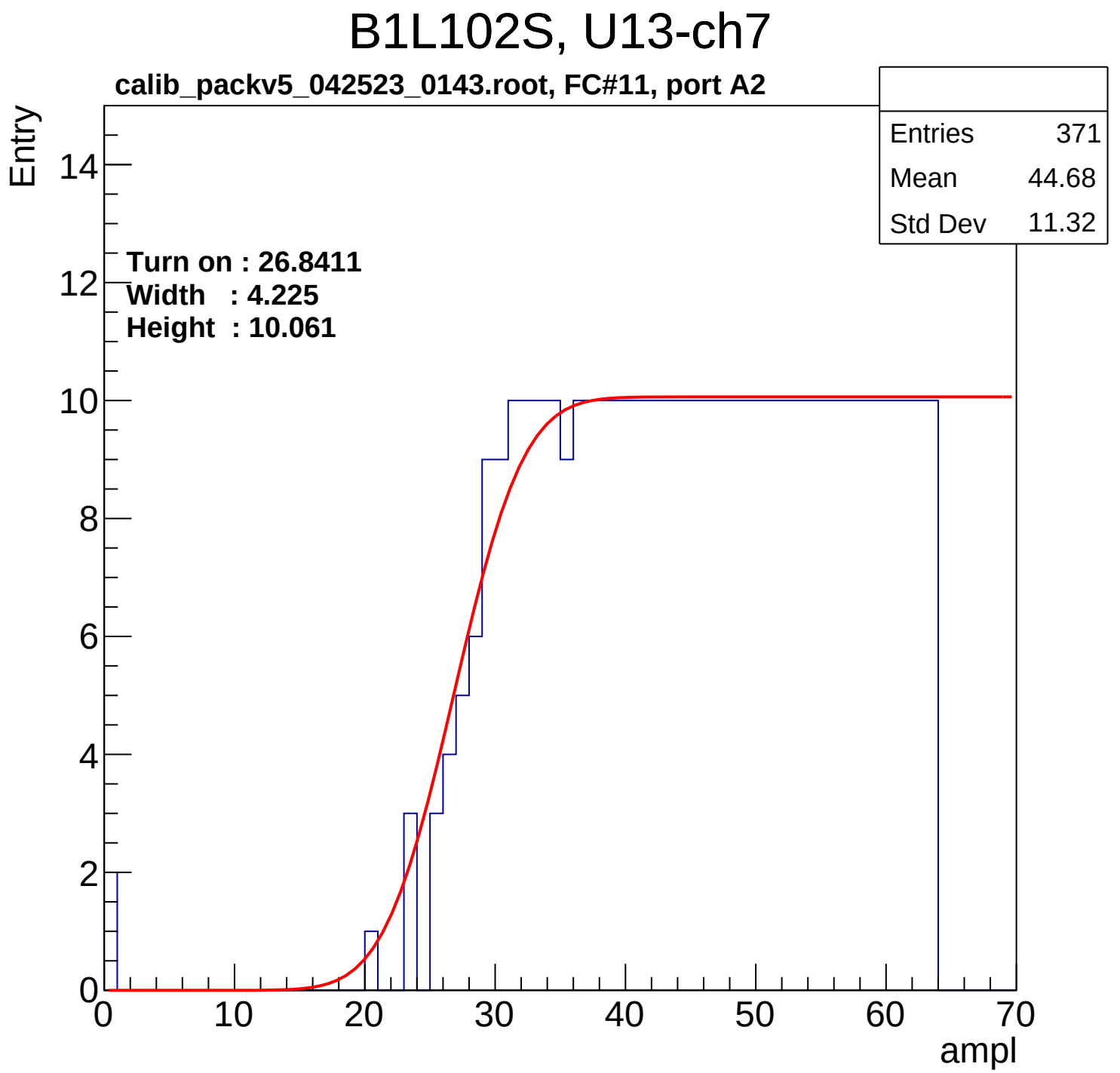
B1L102S, U13-ch7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 371
Mean 44.68
Std Dev 11.32
Turn on : 26.8411
Width : 4.225
Height : 10.061
Entry
ampl
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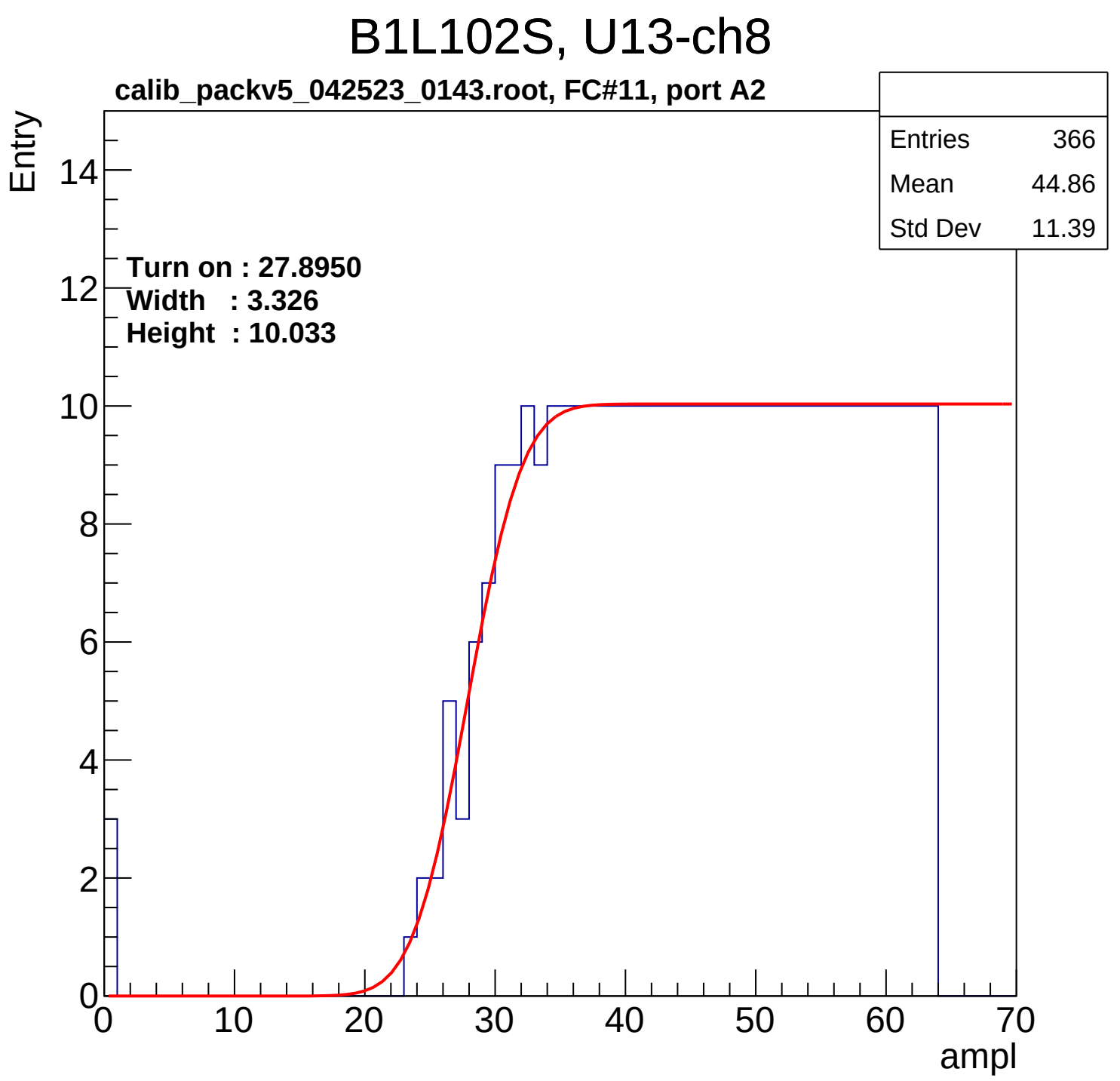
B1L102S, U13-ch8
calib_packv5_042523_0143.root, FC#11, port A2
Entries 366
Mean 44.86
Std Dev 11.39
Turn on : 27.8950
Width : 3.326
Height : 10.033
Entry
ampl
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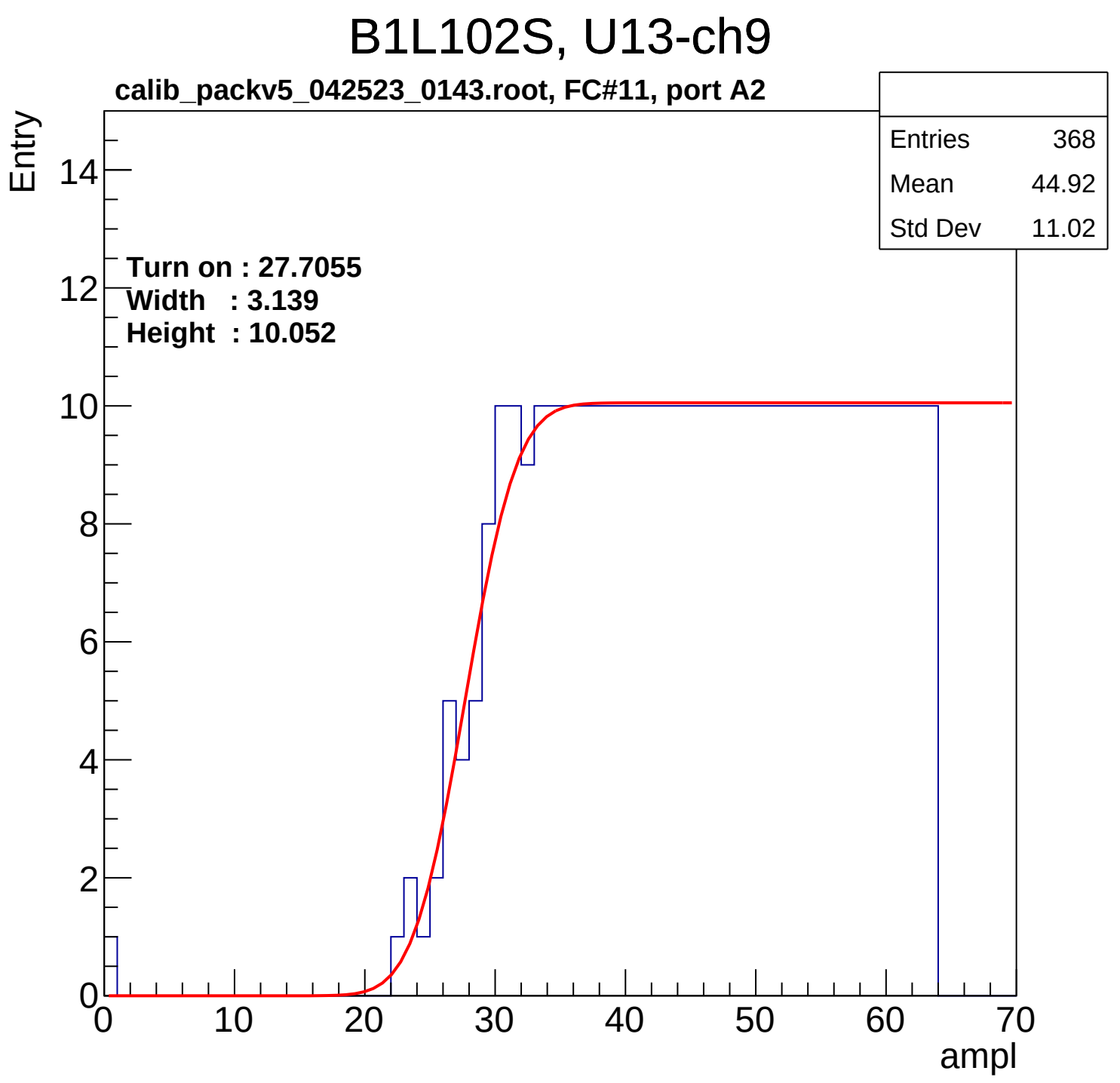
B1L102S, U13-ch9
calib_packv5_042523_0143.root, FC#11, port A2
Entries 368
Mean 44.92
Std Dev 11.02
Turn on : 27.7055
Width : 3.139
Height : 10.052
Entry
ampl
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8
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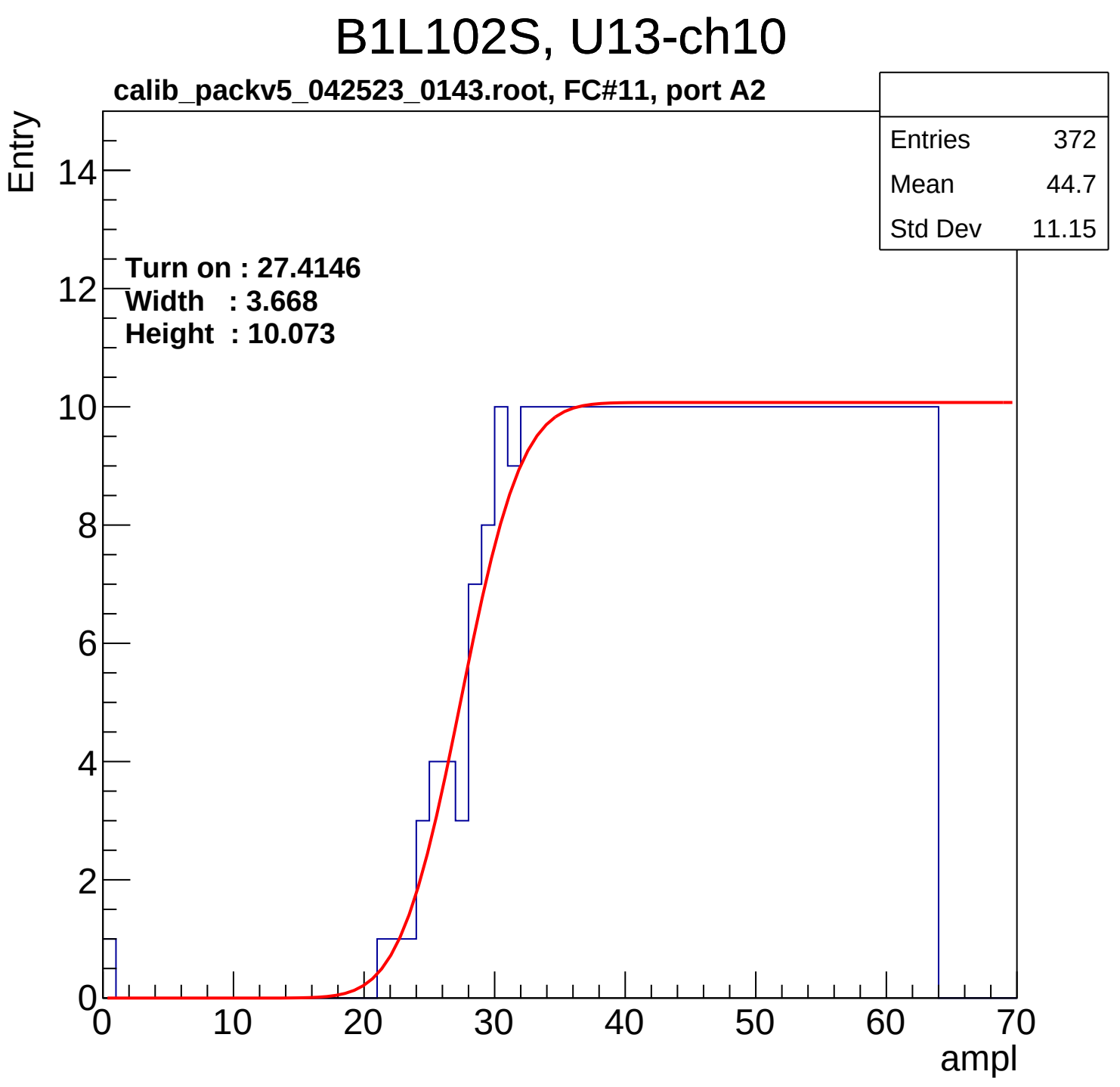
B1L102S, U13-ch10
calib_packv5_042523_0143.root, FC#11, port A2
Entries 372
Mean 44.7
Std Dev 11.15
Turn on : 27.4146
Width : 3.668
Height : 10.073
Entry
ampl
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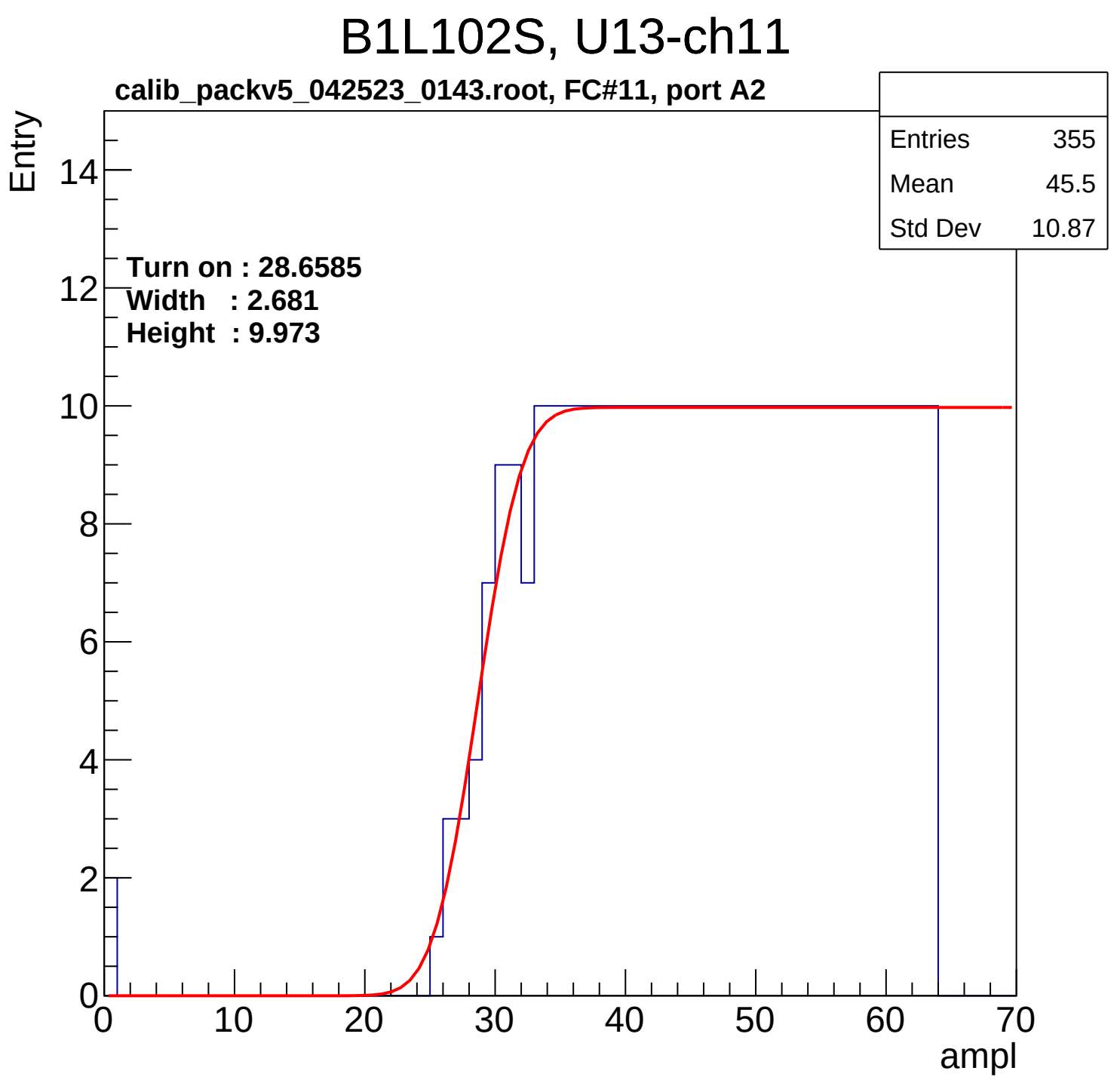
B1L102S, U13-ch11
calib_packv5_042523_0143.root, FC#11, port A2
Entries 355
Mean 45.5
Std Dev 10.87
Turn on : 28.6585
Width : 2.681
Height : 9.973
Entry
ampl
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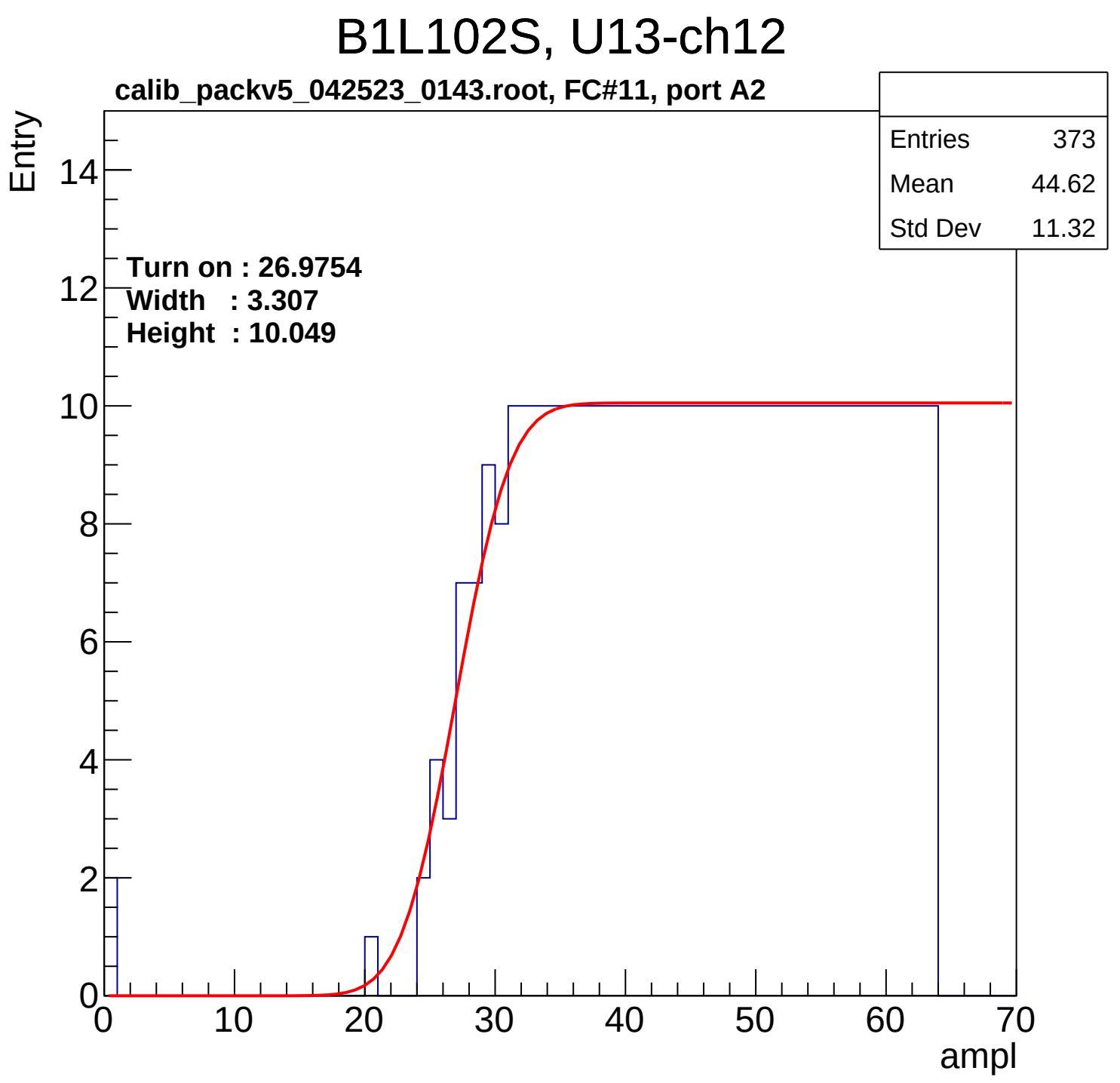
B1L102S, U13-ch12
calib_packv5_042523_0143.root, FC#11, port A2
Entries 373
Mean 44.62
Std Dev 11.32
Turn on : 26.9754
Width : 3.307
Height : 10.049
Entry
ampl
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8
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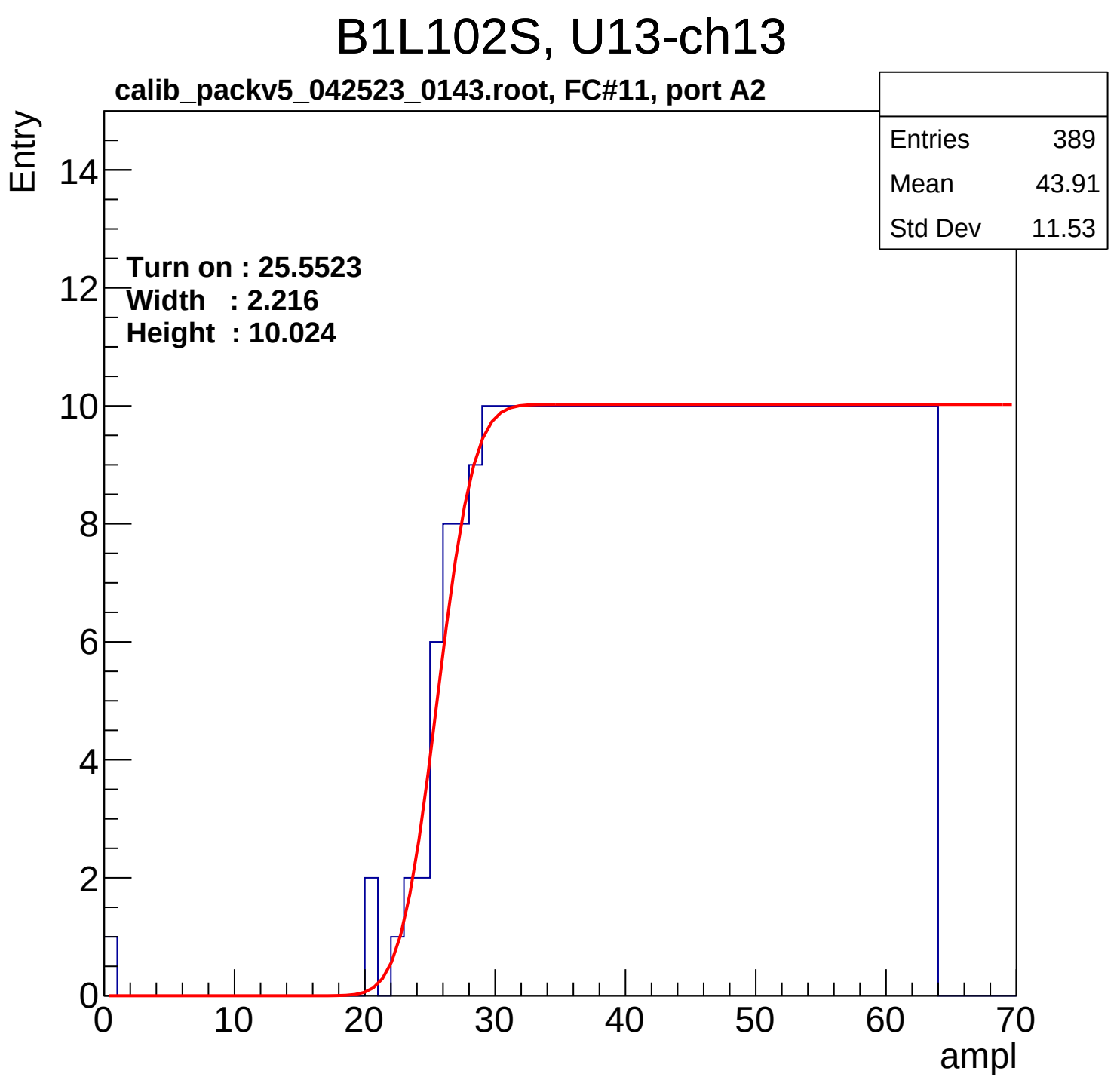
B1L102S, U13-ch13
calib_packv5_042523_0143.root, FC#11, port A2
Entries 389
Mean 43.91
Std Dev 11.53
Turn on : 25.5523
Width : 2.216
Height : 10.024
Entry
ampl
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6
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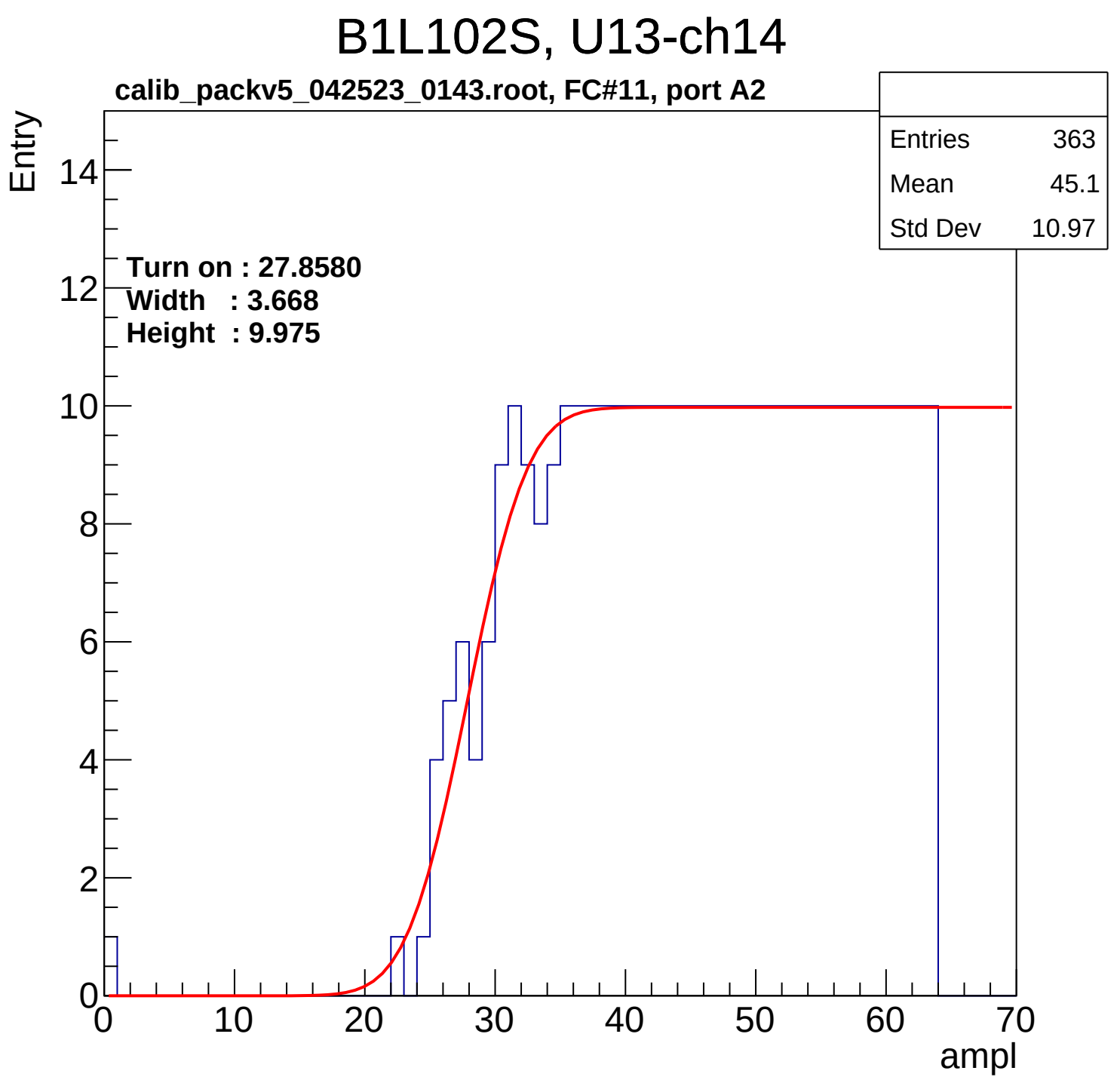
B1L102S, U13-ch14
calib_packv5_042523_0143.root, FC#11, port A2
Entries 363
Mean 45.1
Std Dev 10.97
Turn on : 27.8580
Width : 3.668
Height : 9.975
Entry
ampl
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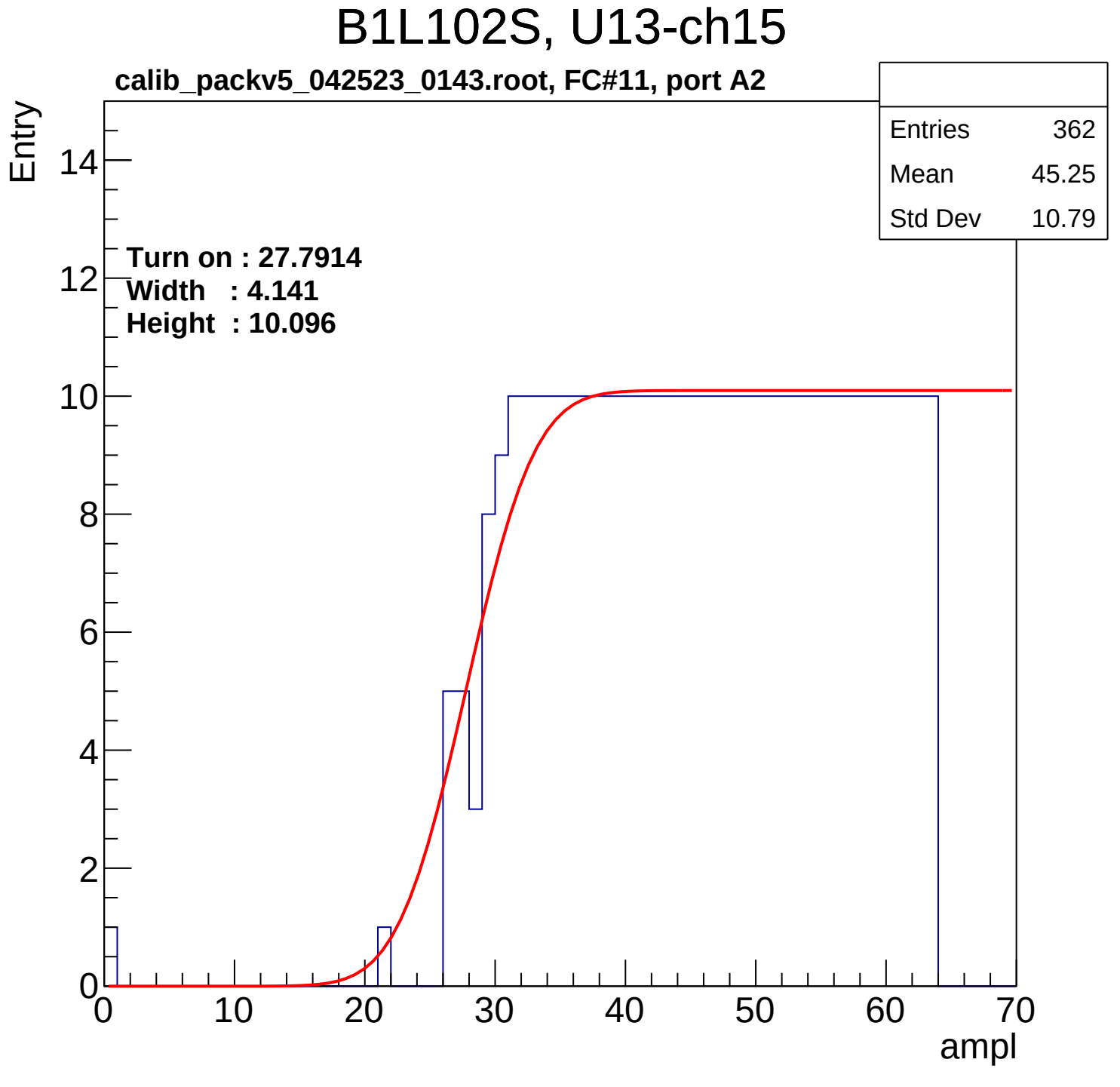
B1L102S, U13-ch15
calib_packv5_042523_0143.root, FC#11, port A2
Entries 362
Mean 45.25
Std Dev 10.79
Turn on : 27.7914
Width : 4.141
Height : 10.096
Entry
ampl
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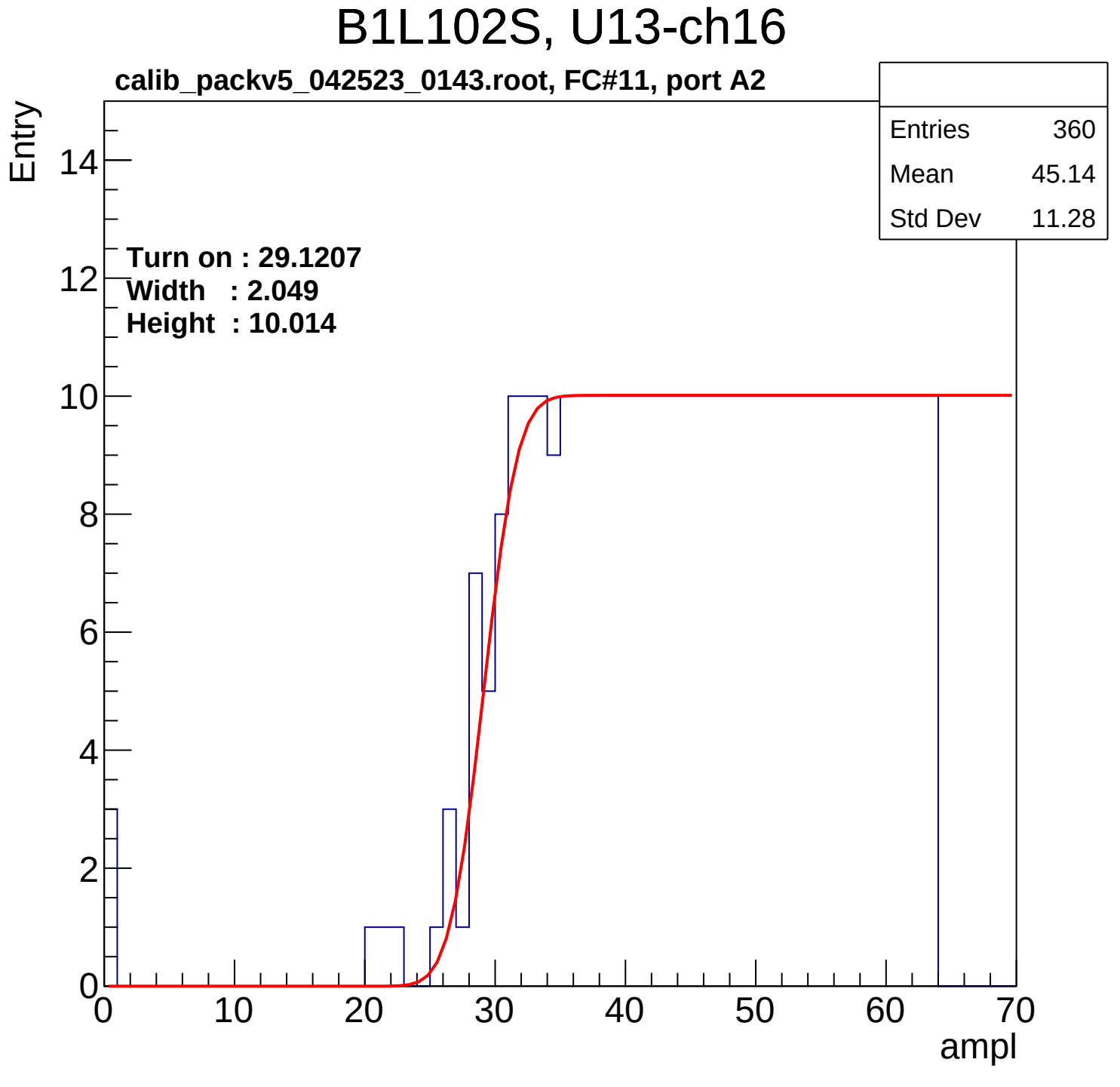
B1L102S, U13-ch16
calib_packv5_042523_0143.root, FC#11, port A2
Entries 360
Mean 45.14
Std Dev 11.28
Turn on : 29.1207
Width : 2.049
Height : 10.014
Entry
ampl
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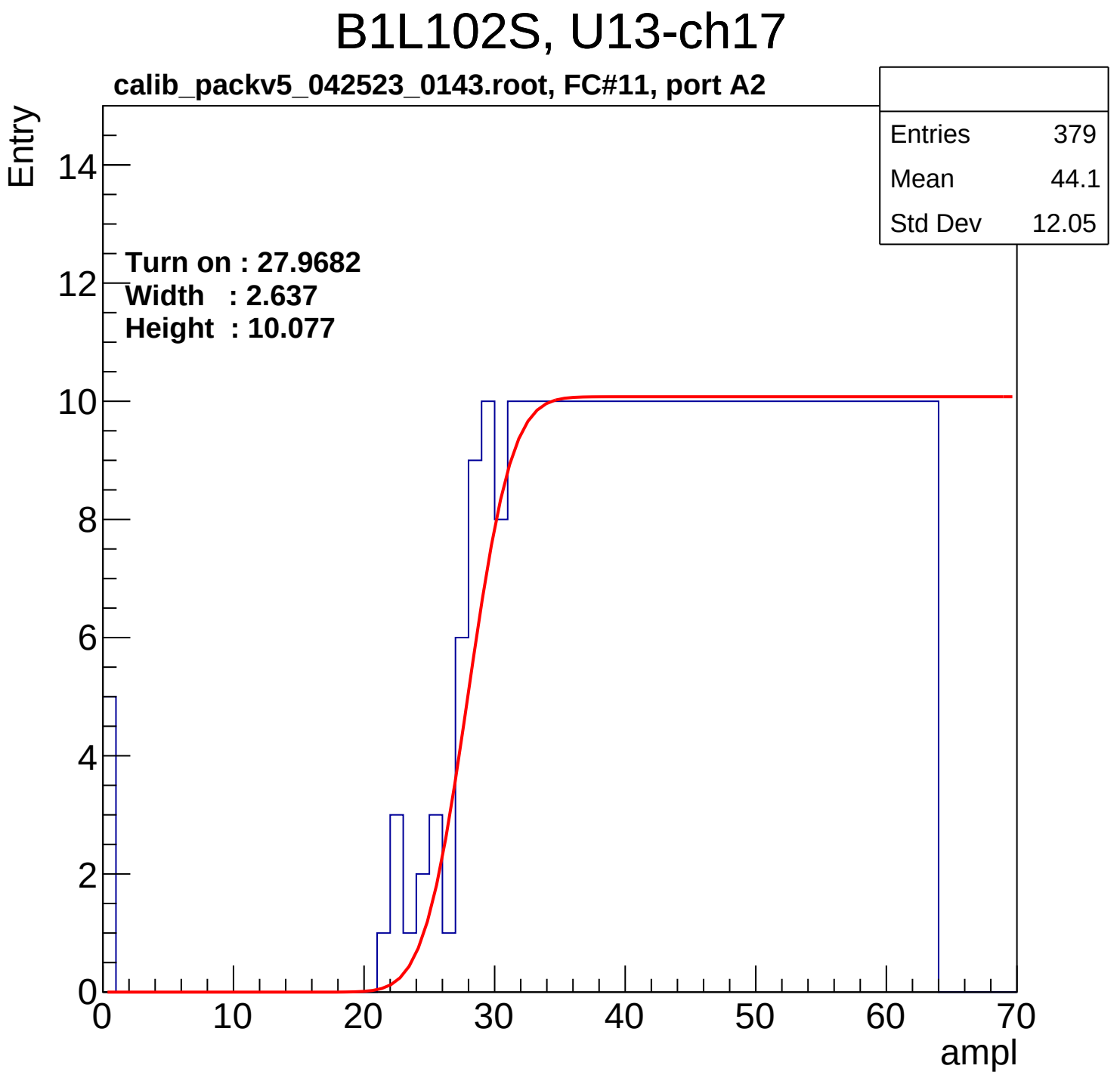
B1L102S, U13-ch17
calib_packv5_042523_0143.root, FC#11, port A2
Entries 379
Mean 44.1
Std Dev 12.05
Turn on : 27.9682
Width : 2.637
Height : 10.077
Entry
ampl
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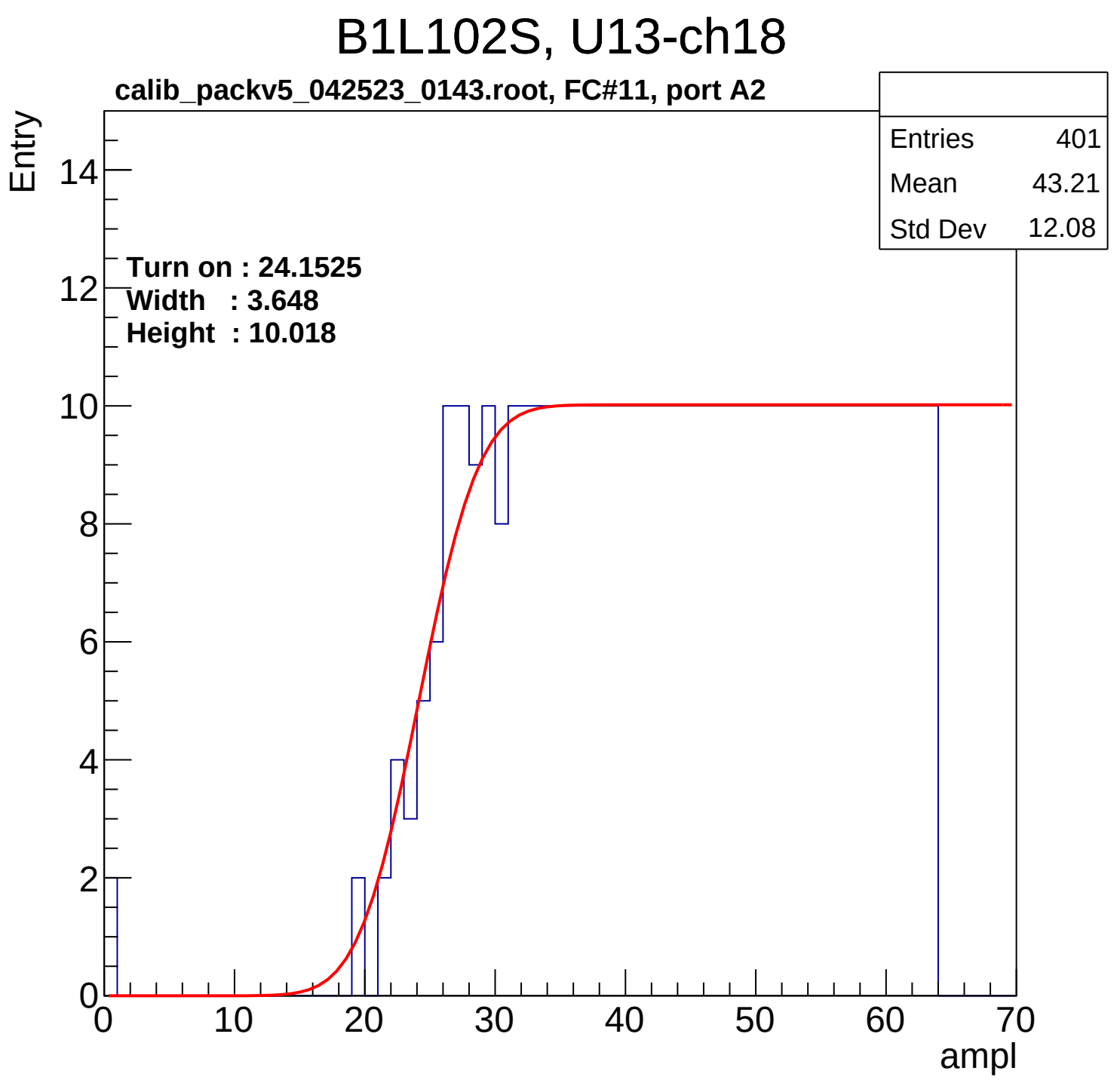
B1L102S, U13-ch18
calib_packv5_042523_0143.root, FC#11, port A2
Entries 401
Mean 43.21
Std Dev 12.08
Turn on : 24.1525
Width : 3.648
Height : 10.018
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ampl
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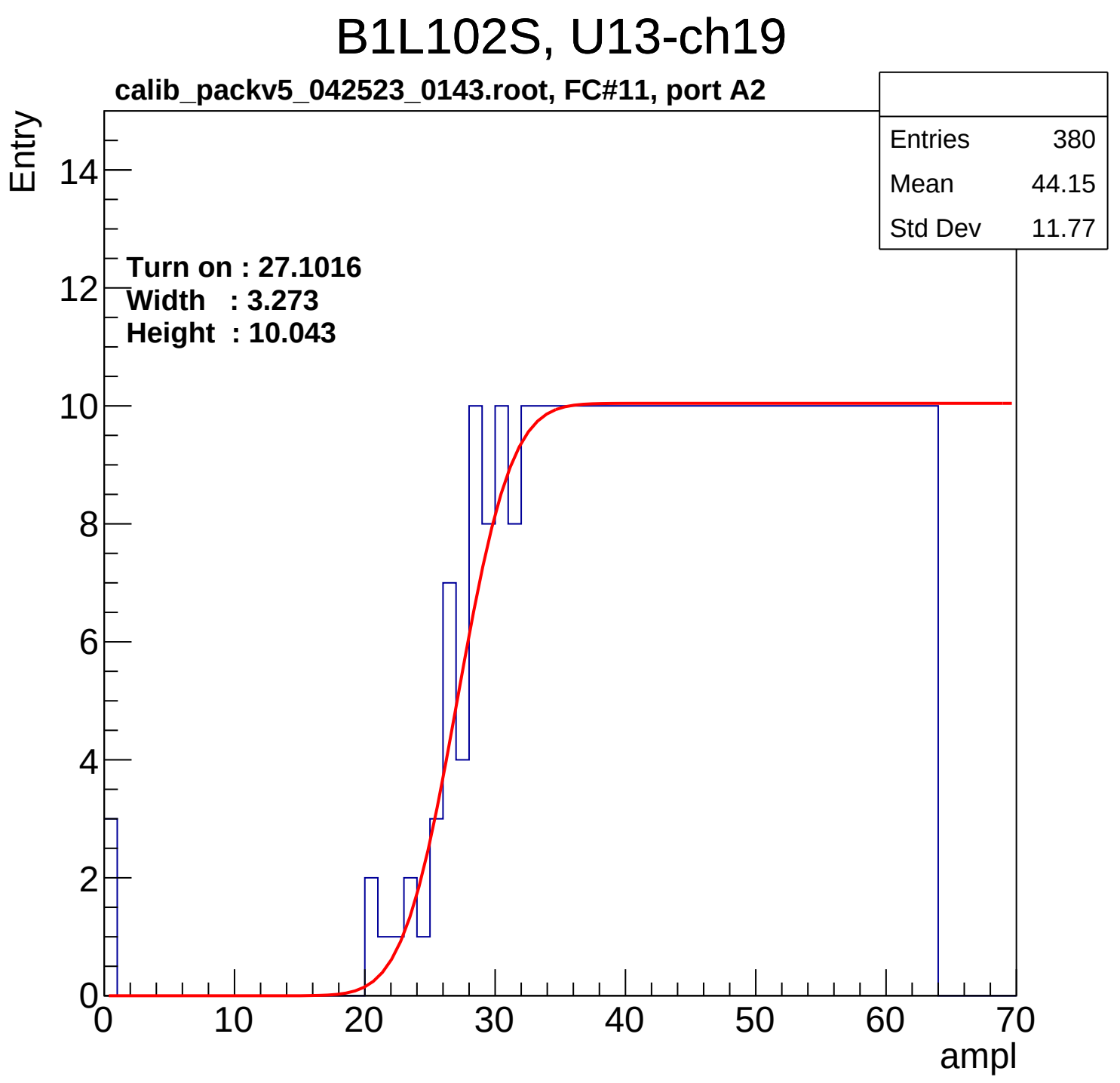
B1L102S, U13-ch19
calib_packv5_042523_0143.root, FC#11, port A2
Entries 380
Mean 44.15
Std Dev 11.77
Turn on : 27.1016
Width : 3.273
Height : 10.043
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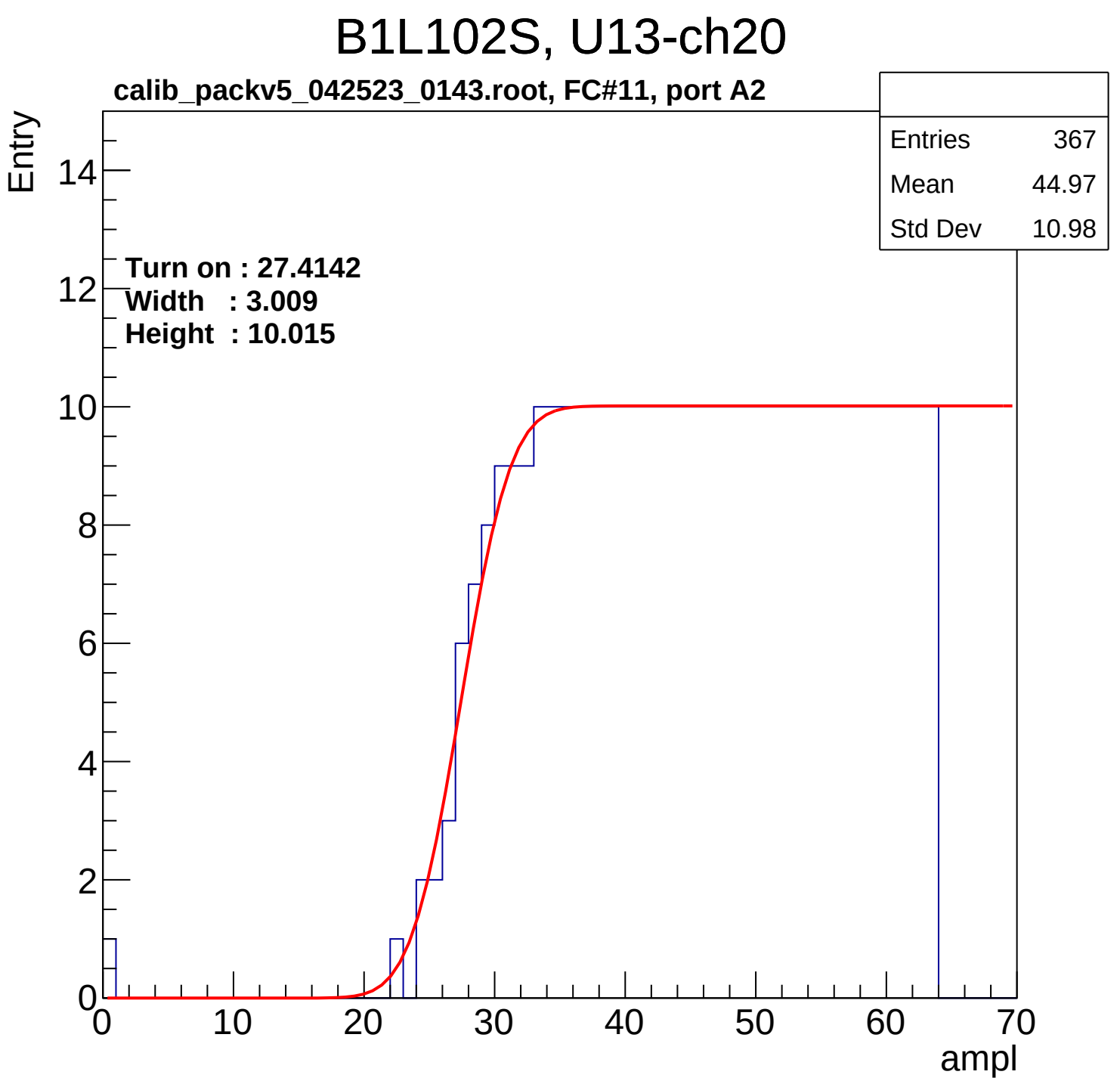
B1L102S, U13-ch20
calib_packv5_042523_0143.root, FC#11, port A2
Entries 367
Mean 44.97
Std Dev 10.98
Turn on : 27.4142
Width : 3.009
Height : 10.015
Entry
ampl
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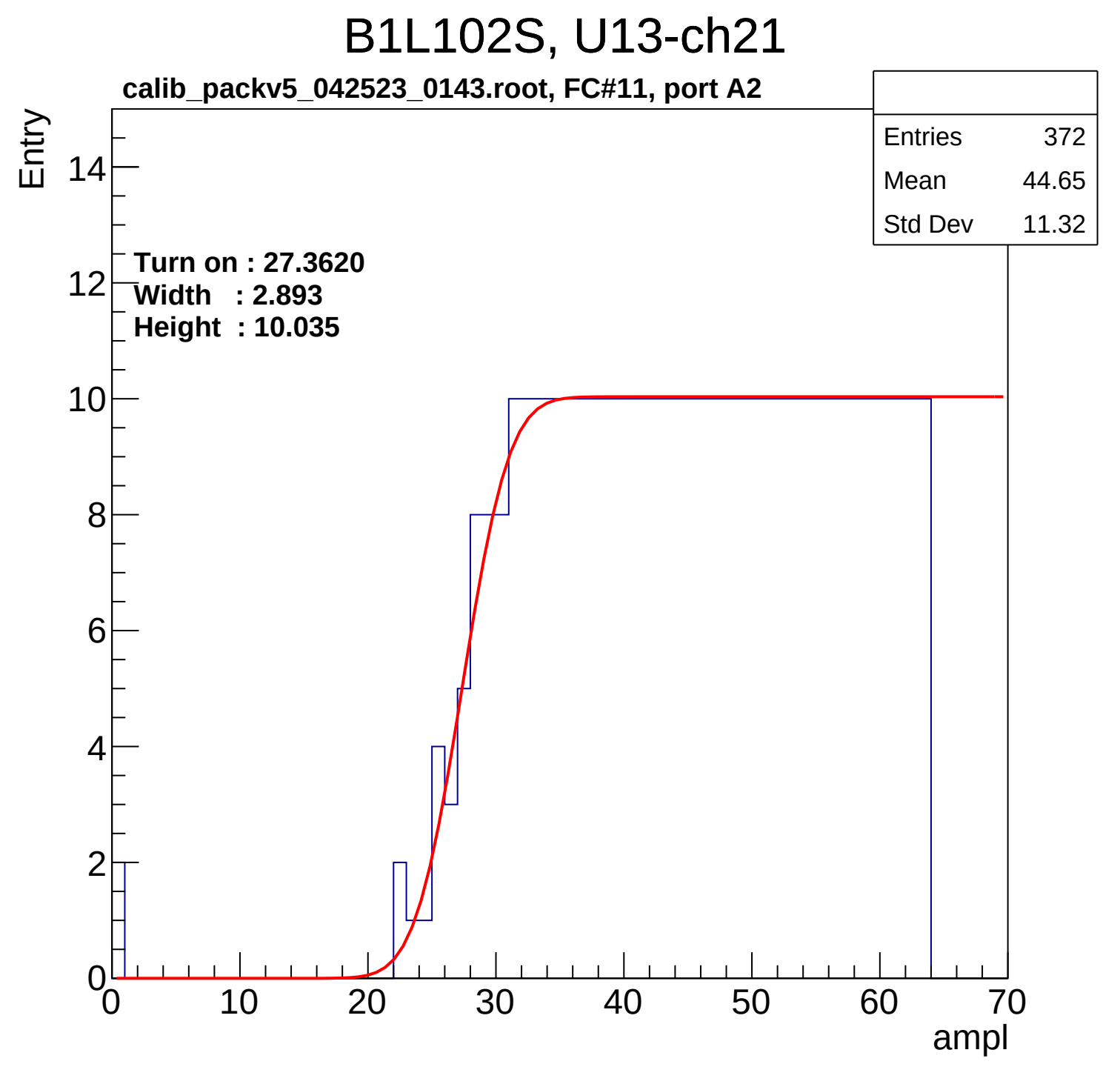
B1L102S, U13-ch21
calib_packv5_042523_0143.root, FC#11, port A2
Entries 372
Mean 44.65
Std Dev 11.32
Turn on : 27.3620
Width : 2.893
Height : 10.035
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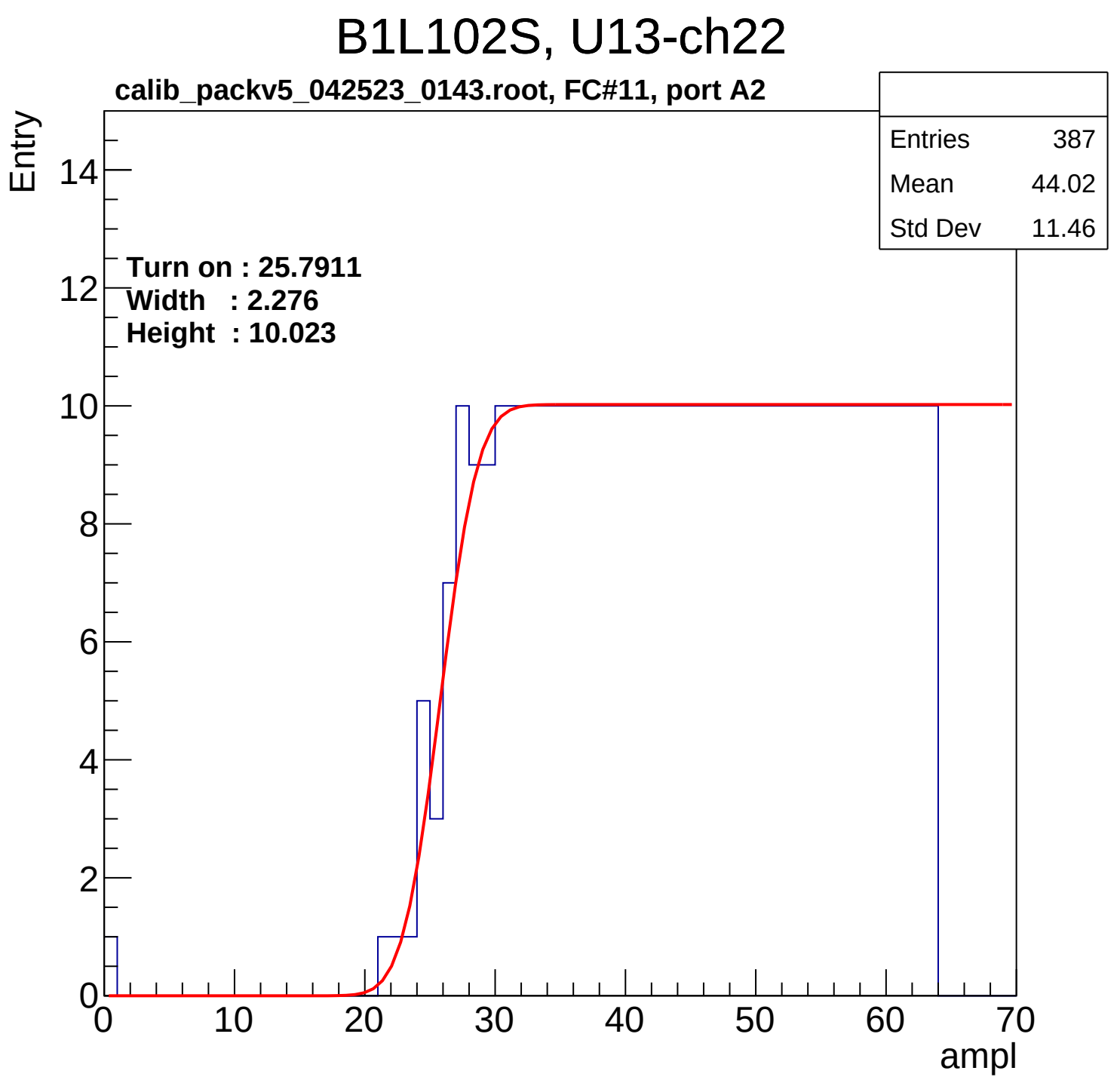
B1L102S, U13-ch22
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 44.02
Std Dev 11.46
Turn on : 25.7911
Width : 2.276
Height : 10.023
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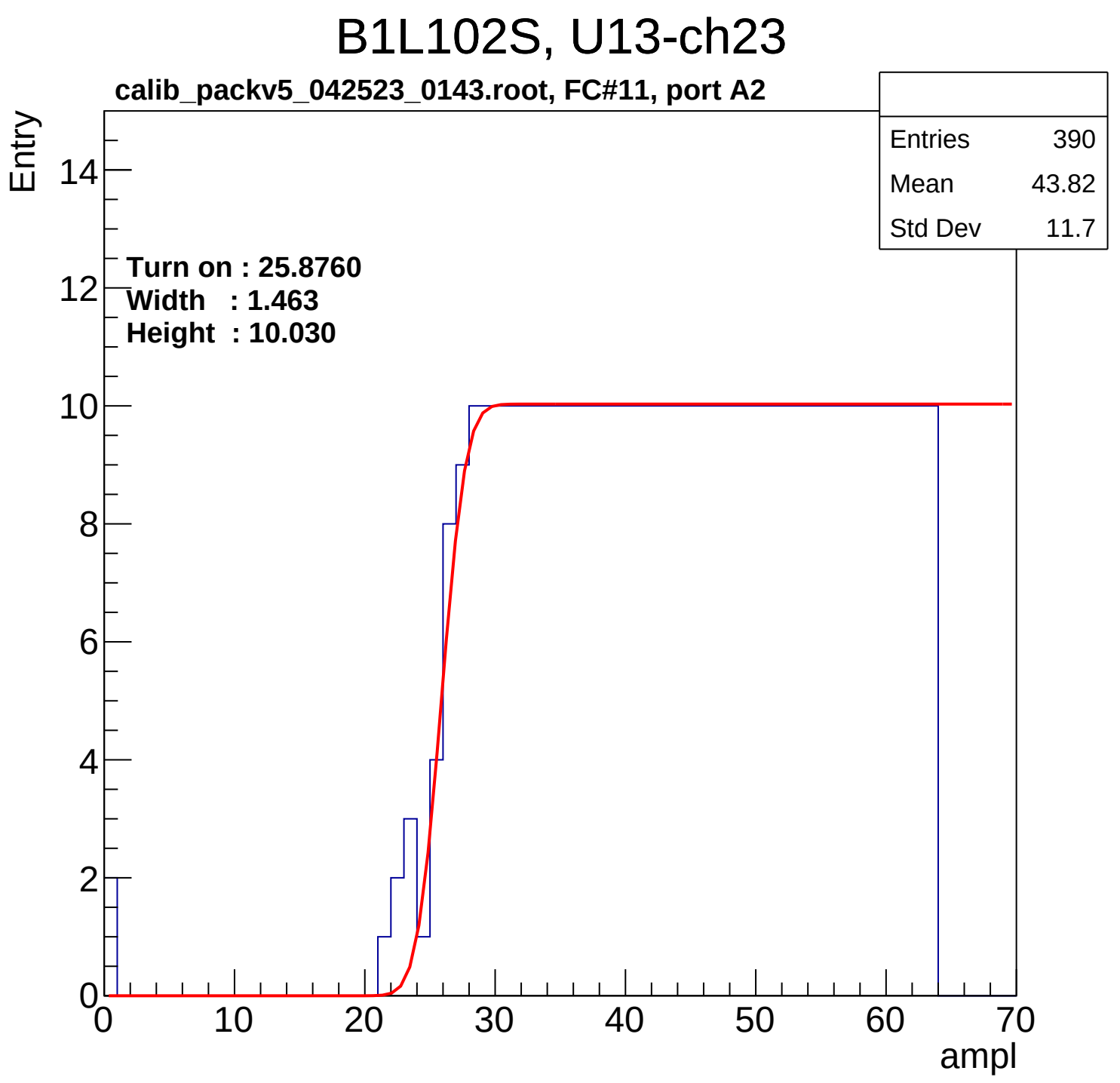
B1L102S, U13-ch23
calib_packv5_042523_0143.root, FC#11, port A2
Entries 390
Mean 43.82
Std Dev 11.7
Turn on : 25.8760
Width : 1.463
Height : 10.030
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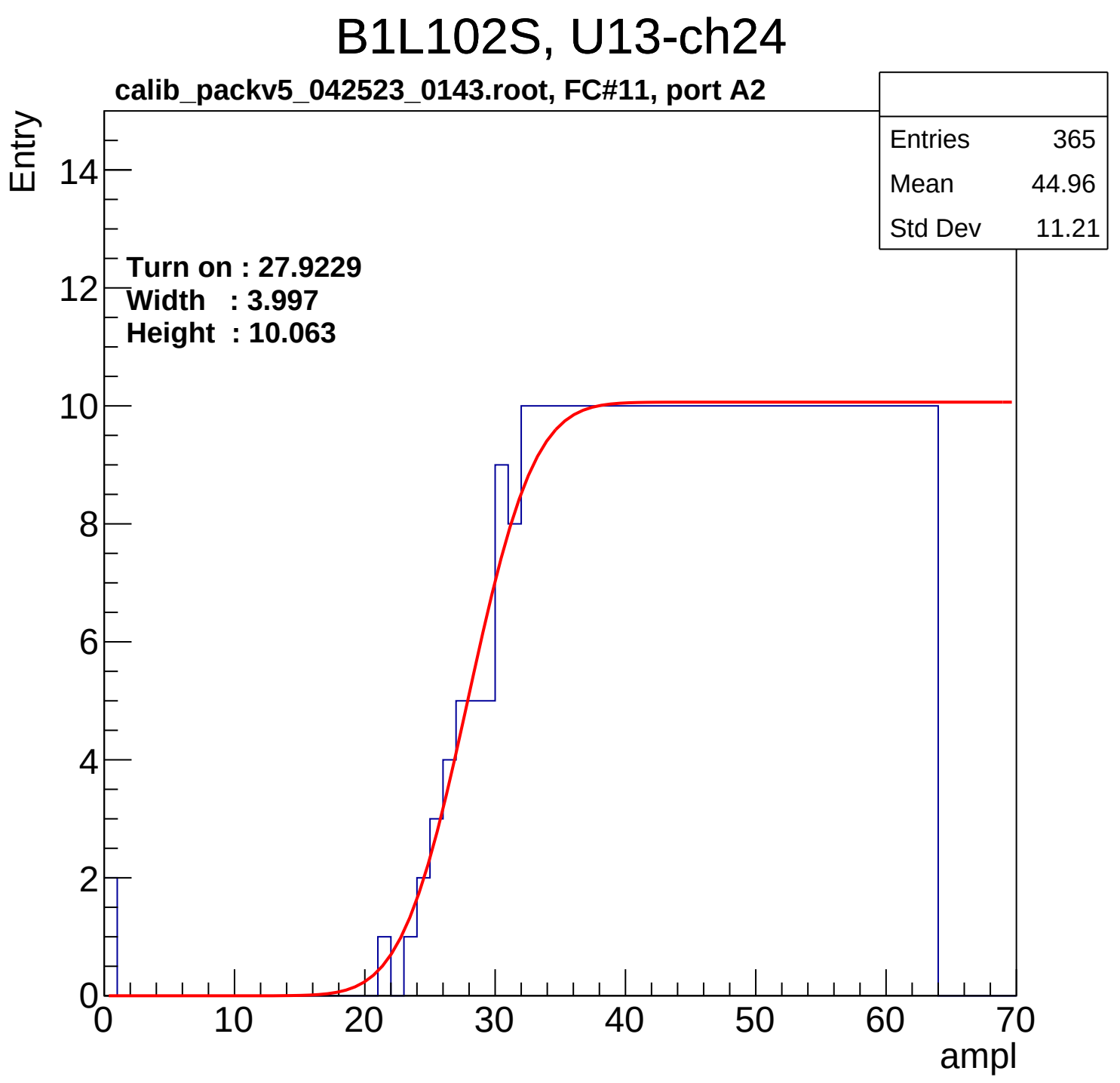
B1L102S, U13-ch24
calib_packv5_042523_0143.root, FC#11, port A2
Entries 365
Mean 44.96
Std Dev 11.21
Turn on : 27.9229
Width : 3.997
Height : 10.063
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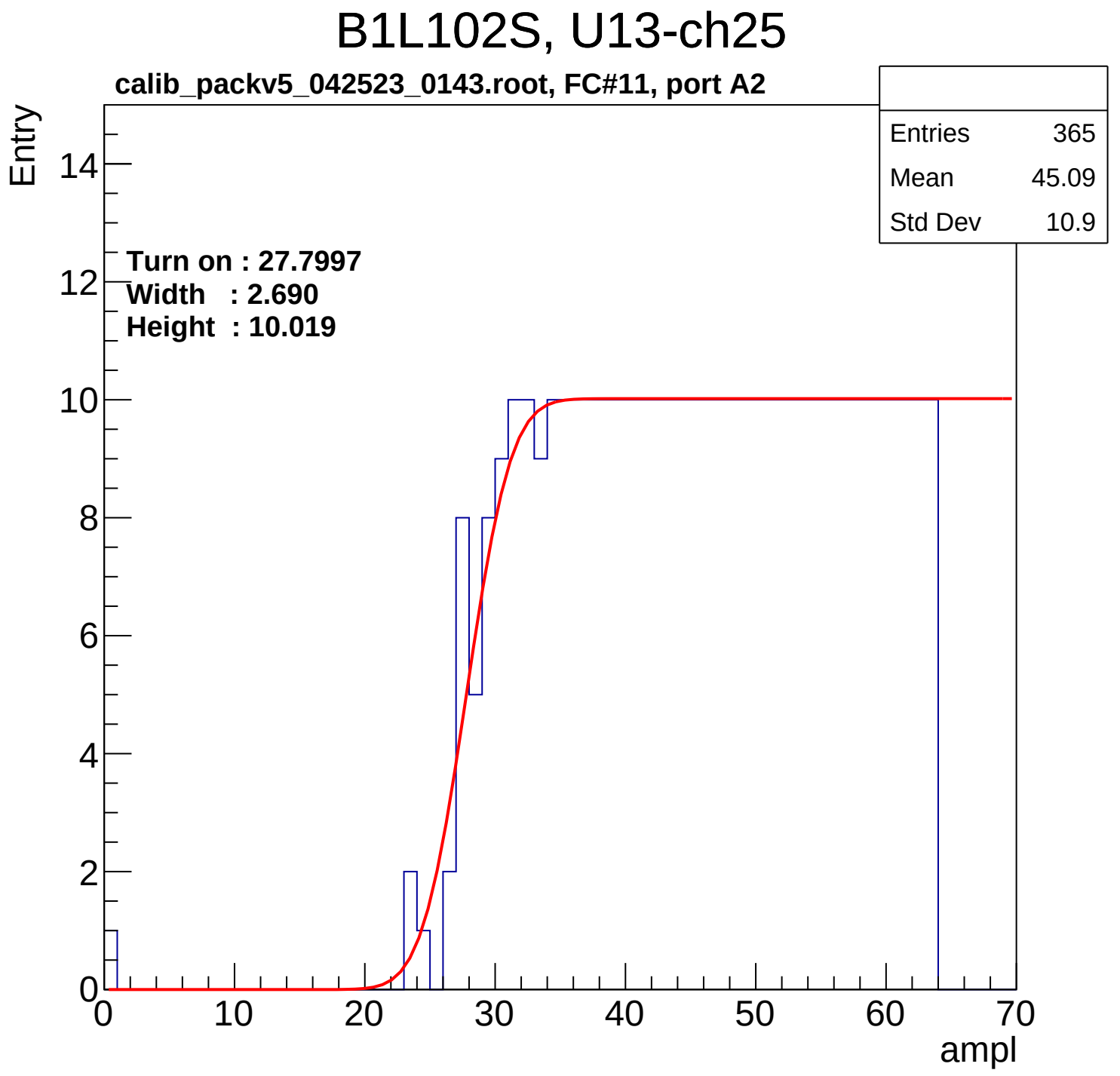
B1L102S, U13-ch25
calib_packv5_042523_0143.root, FC#11, port A2
Entries 365
Mean 45.09
Std Dev 10.9
Turn on : 27.7997
Width : 2.690
Height : 10.019
Entry
ampl
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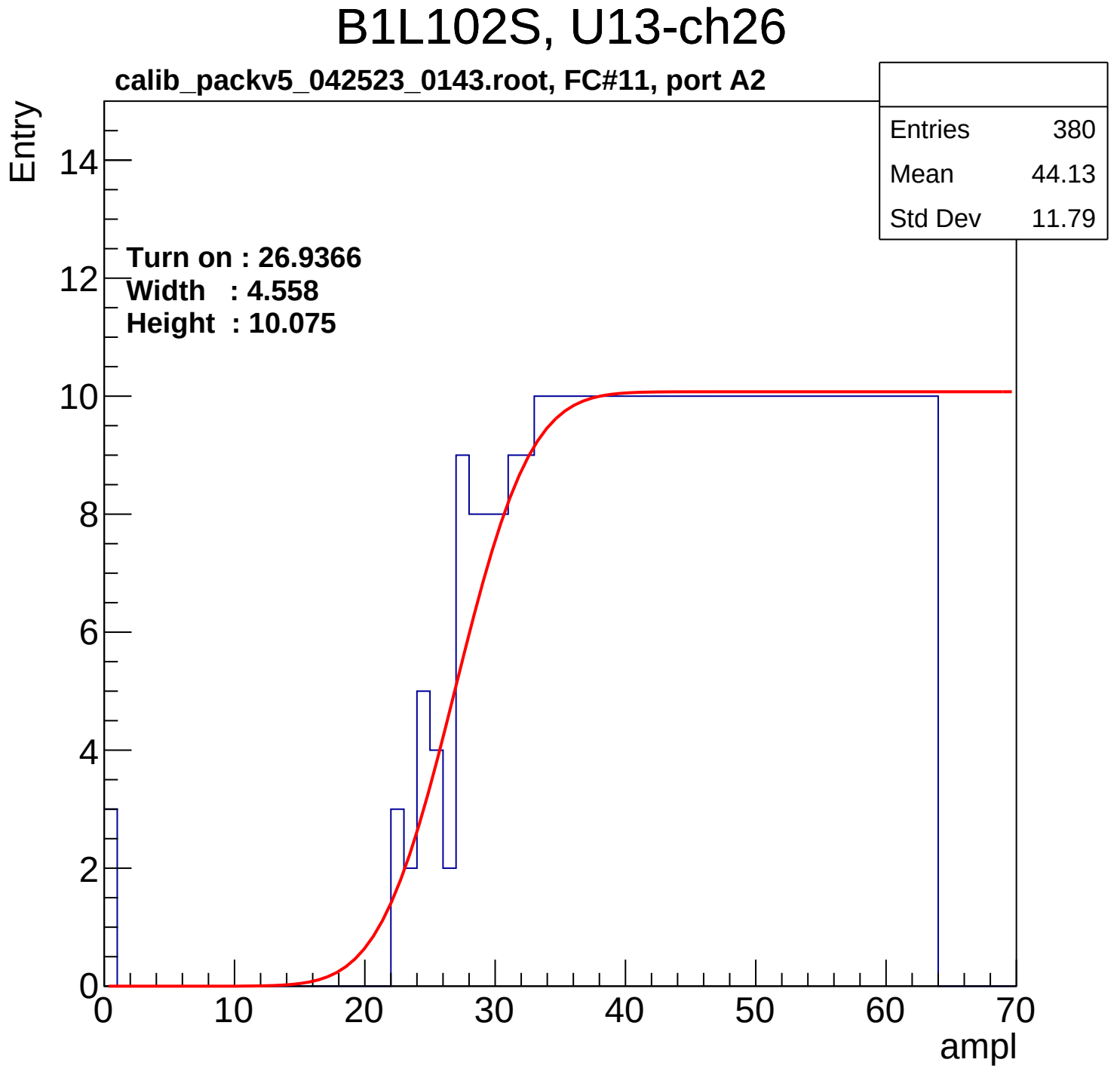
B1L102S, U13-ch26
calib_packv5_042523_0143.root, FC#11, port A2
Entries 380
Mean 44.13
Std Dev 11.79
Turn on : 26.9366
Width : 4.558
Height : 10.075
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ampl
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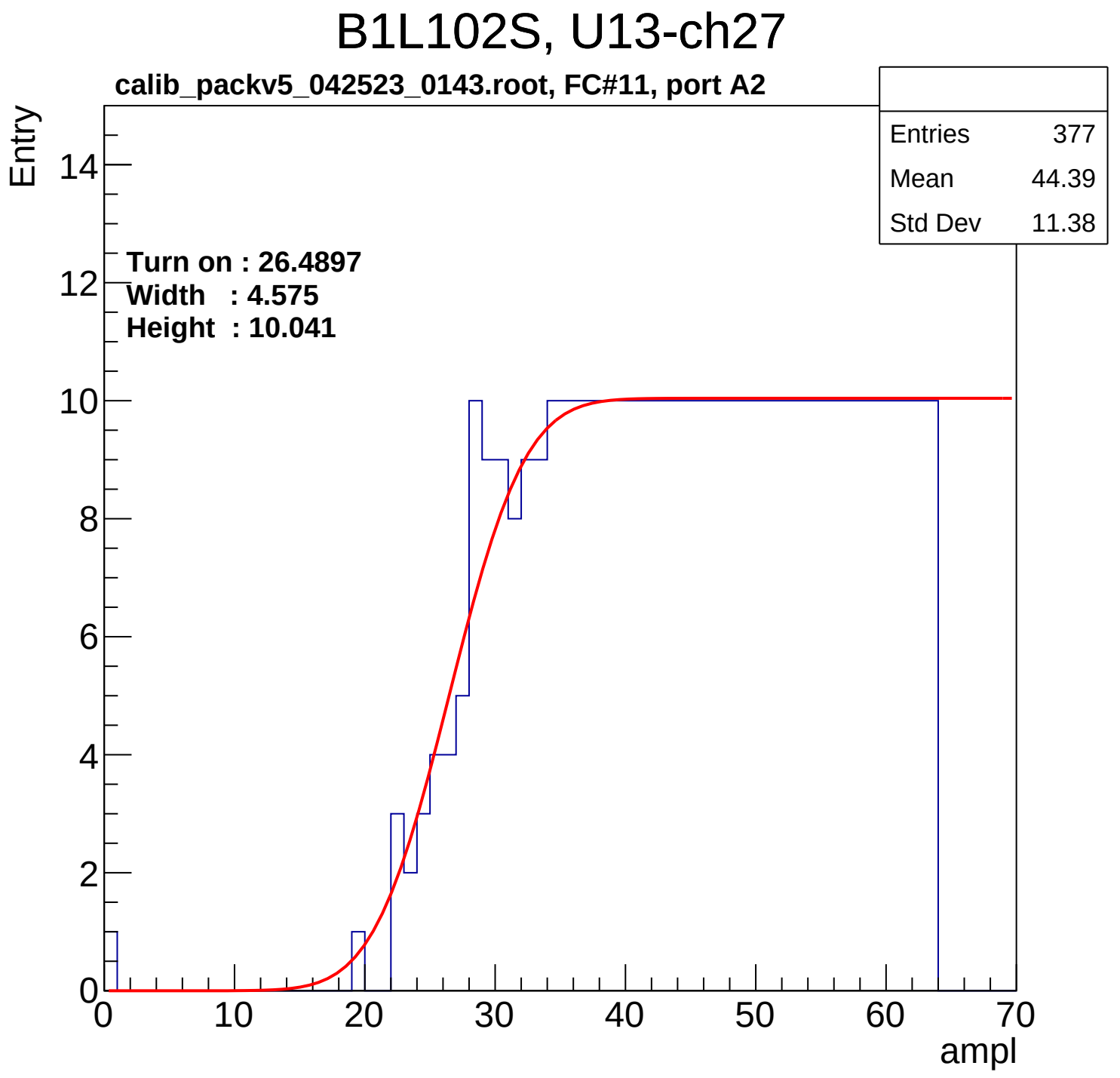
B1L102S, U13-ch27
calib_packv5_042523_0143.root, FC#11, port A2
Entries 377
Mean 44.39
Std Dev 11.38
Turn on : 26.4897
Width : 4.575
Height : 10.041
Entry
ampl
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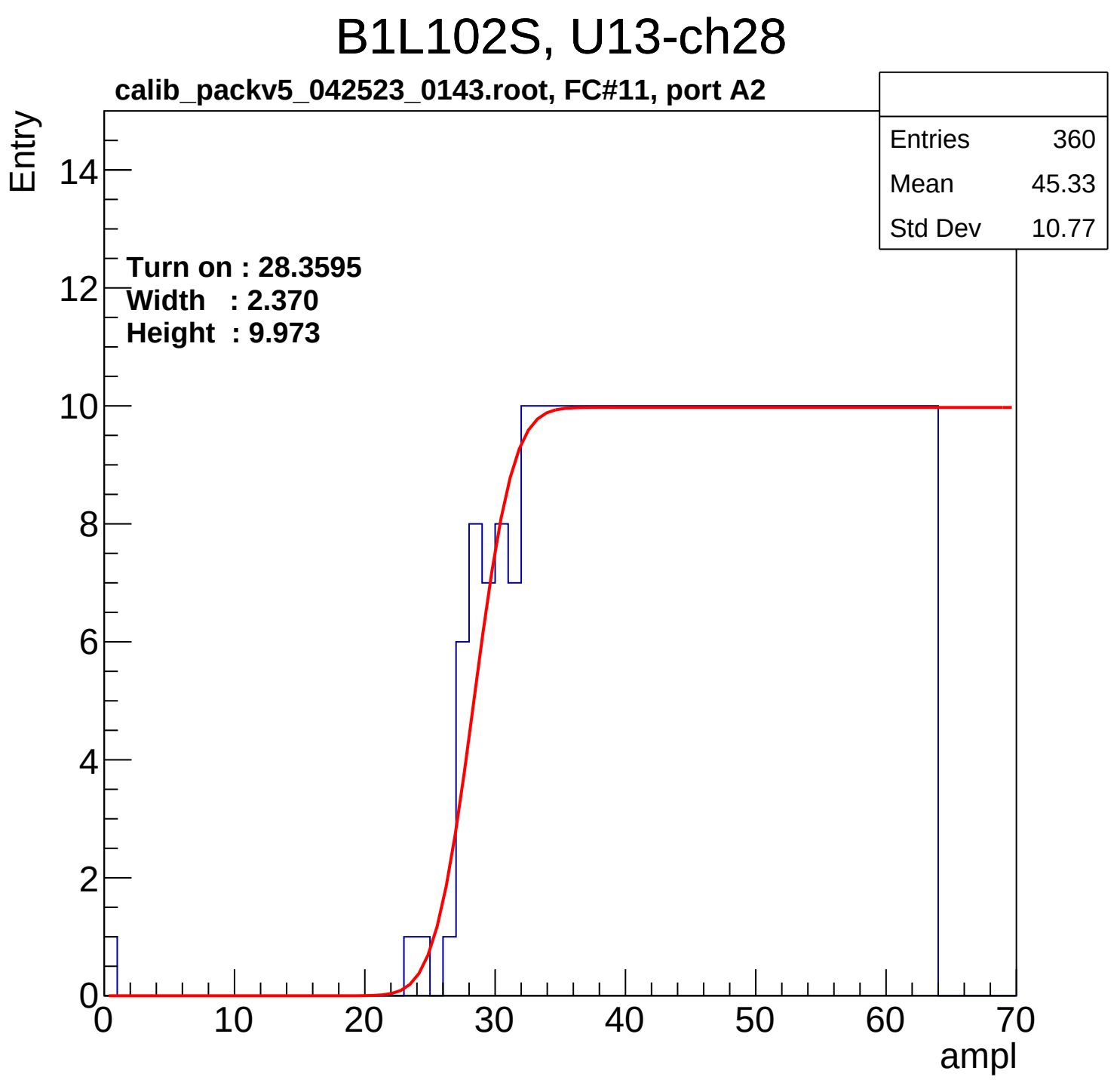
B1L102S, U13-ch28
calib_packv5_042523_0143.root, FC#11, port A2
Entries 360
Mean 45.33
Std Dev 10.77
Turn on : 28.3595
Width : 2.370
Height : 9.973
Entry
ampl
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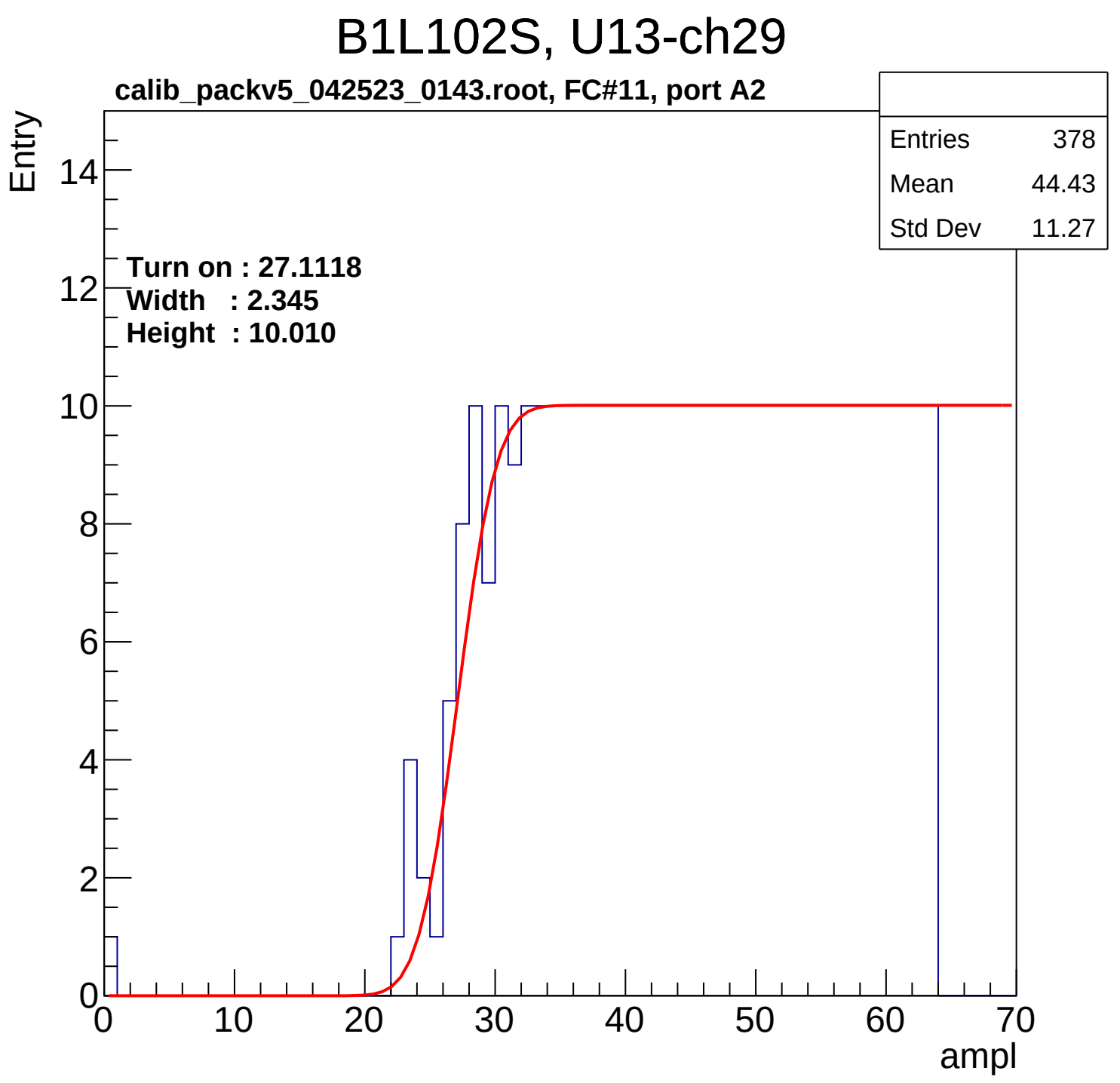
B1L102S, U13-ch29
calib_packv5_042523_0143.root, FC#11, port A2
Entries 378
Mean 44.43
Std Dev 11.27
Turn on : 27.1118
Width : 2.345
Height : 10.010
Entry
ampl
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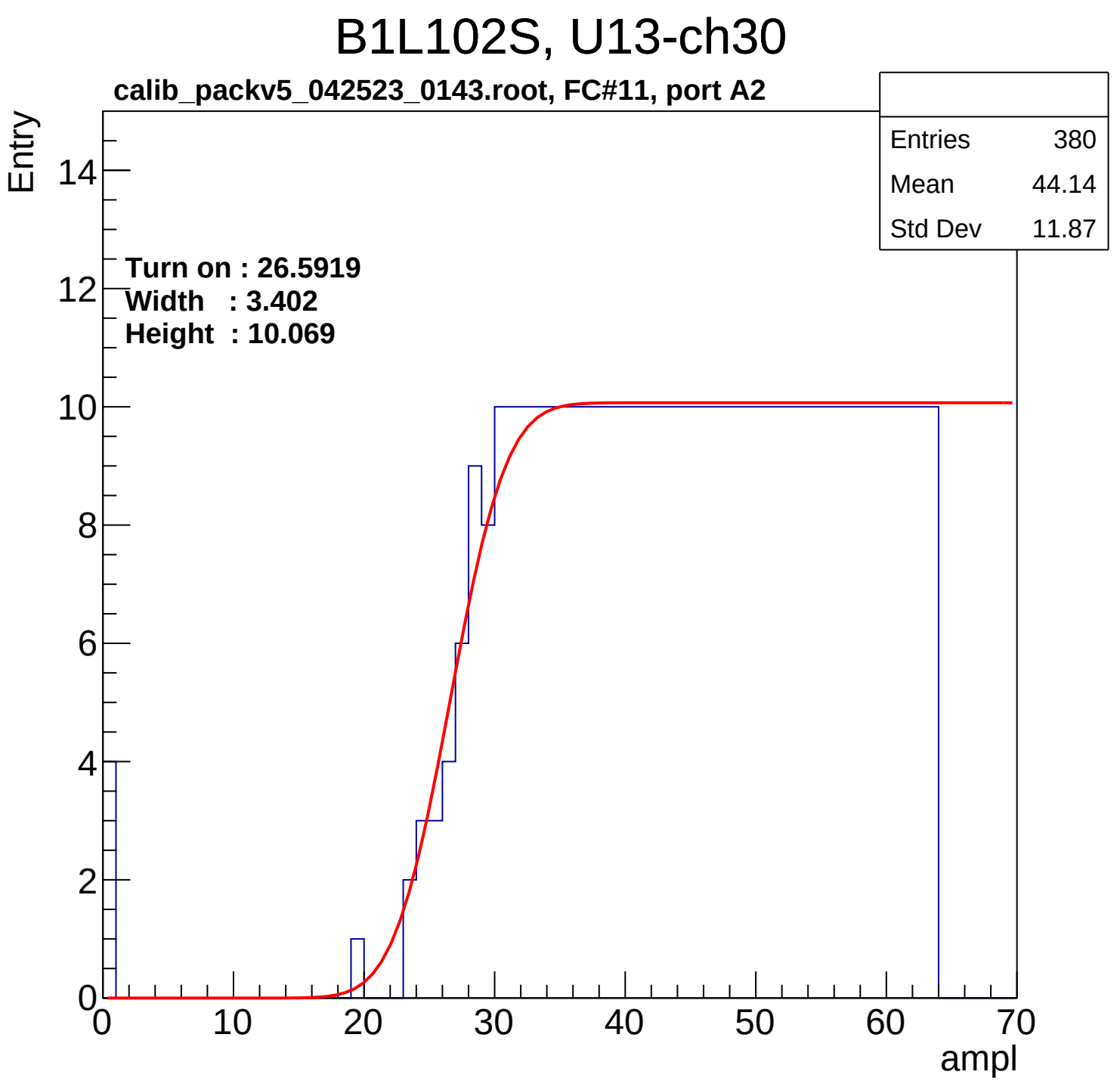
B1L102S, U13-ch30
calib_packv5_042523_0143.root, FC#11, port A2
Entries 380
Mean 44.14
Std Dev 11.87
Turn on : 26.5919
Width : 3.402
Height : 10.069
Entry
ampl
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6
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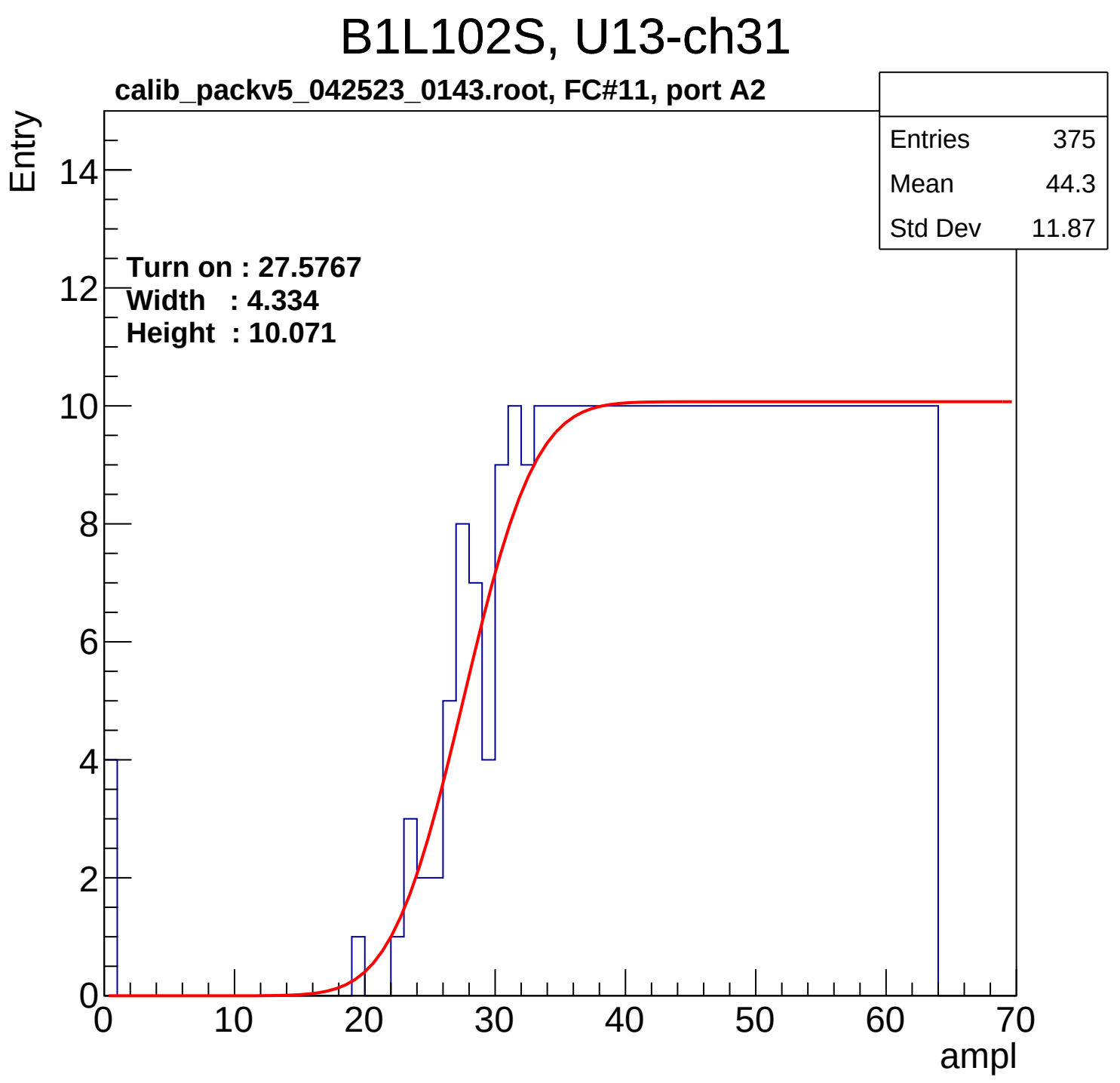
B1L102S, U13-ch31
calib_packv5_042523_0143.root, FC#11, port A2
Entries 375
Mean 44.3
Std Dev 11.87
Turn on : 27.5767
Width : 4.334
Height : 10.071
Entry
ampl
0
2
4
6
8
10
12
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60
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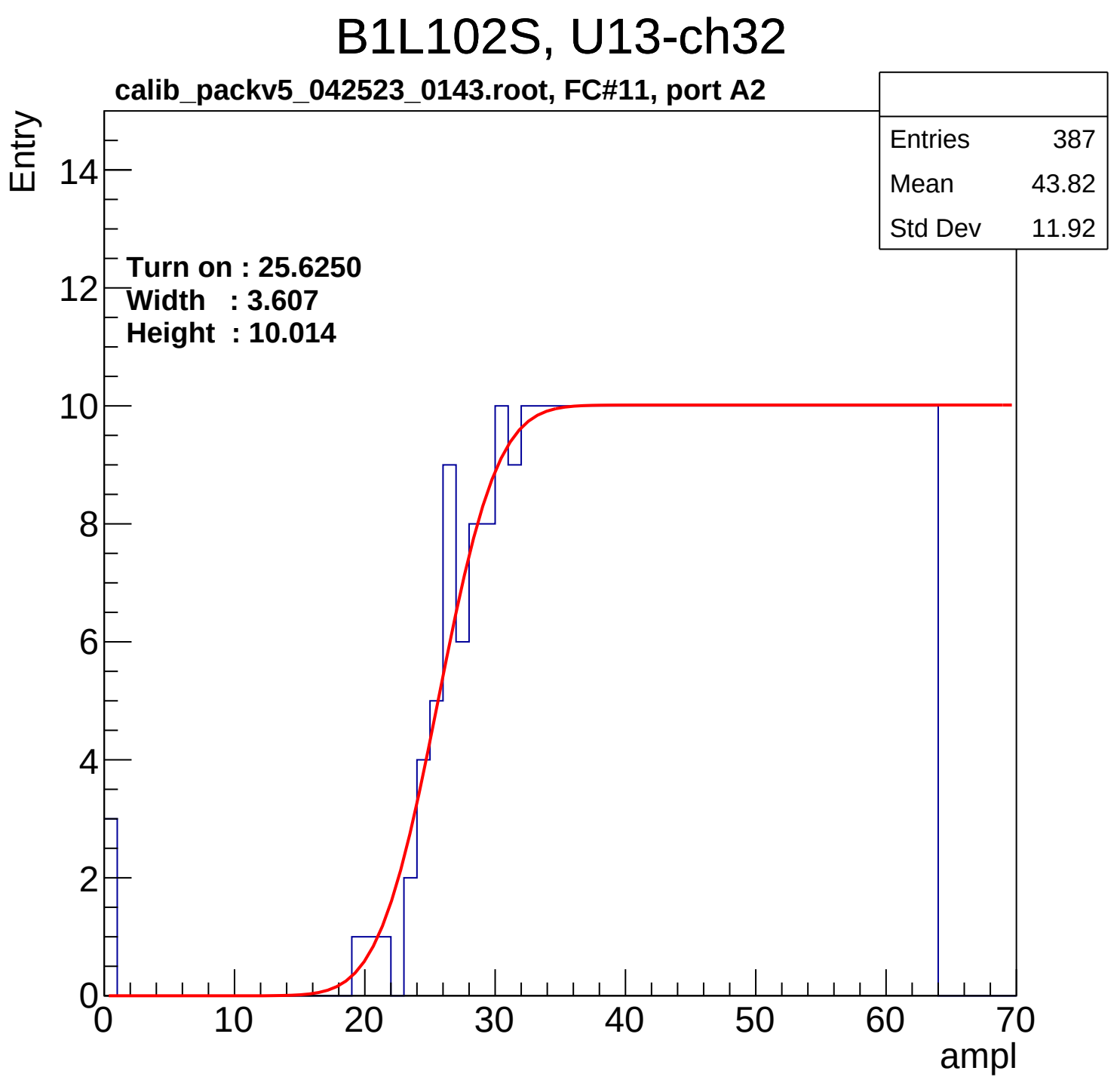
B1L102S, U13-ch32
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 43.82
Std Dev 11.92
Turn on : 25.6250
Width : 3.607
Height : 10.014
Entry
ampl
0
2
4
6
8
10
12
14
0
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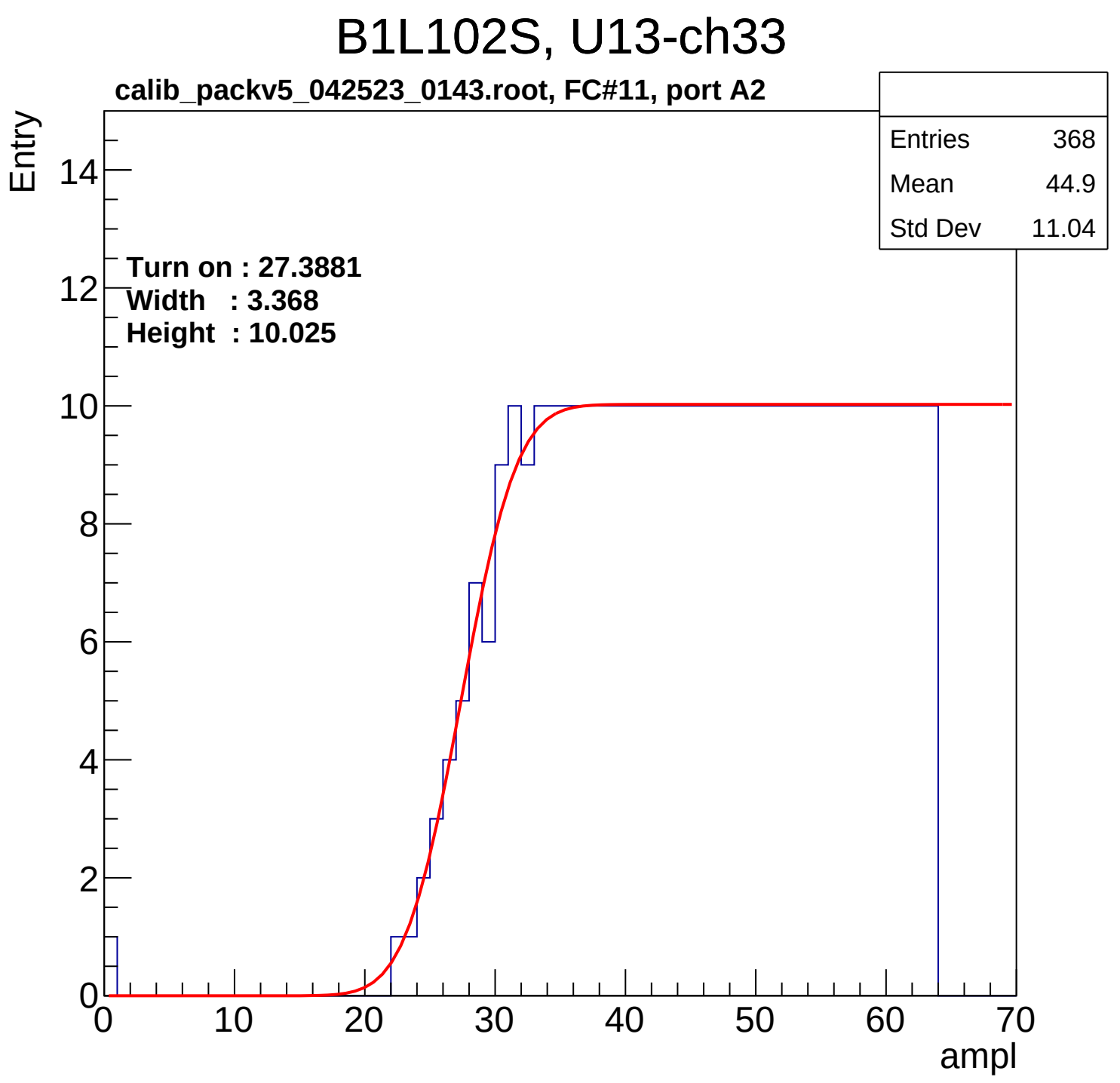
B1L102S, U13-ch33
calib_packv5_042523_0143.root, FC#11, port A2
Entries 368
Mean 44.9
Std Dev 11.04
Turn on : 27.3881
Width : 3.368
Height : 10.025
Entry
ampl
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4
6
8
10
12
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0
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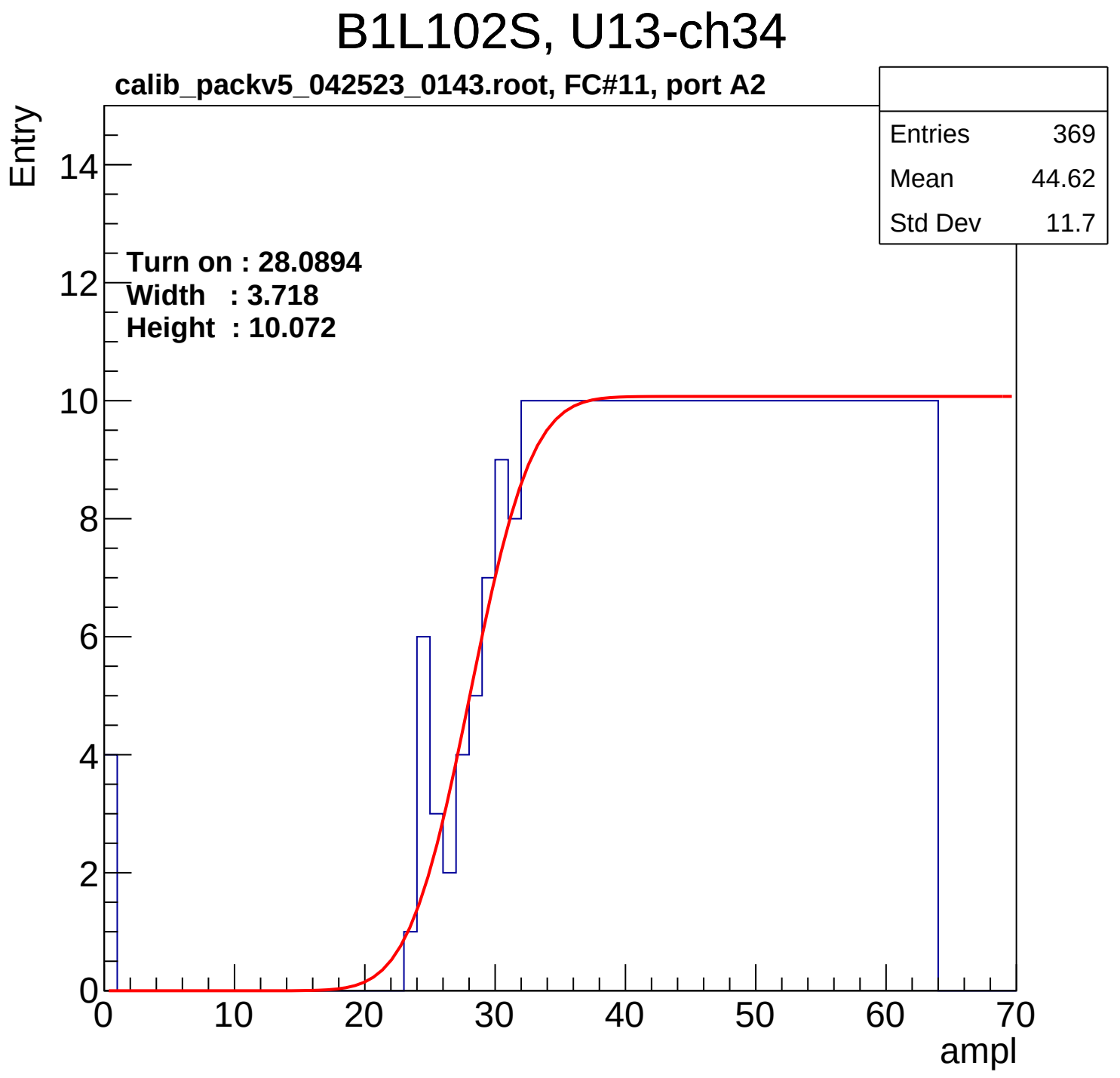
B1L102S, U13-ch34
calib_packv5_042523_0143.root, FC#11, port A2
Entries 369
Mean 44.62
Std Dev 11.7
Turn on : 28.0894
Width : 3.718
Height : 10.072
Entry
ampl
0
2
4
6
8
10
12
14
0
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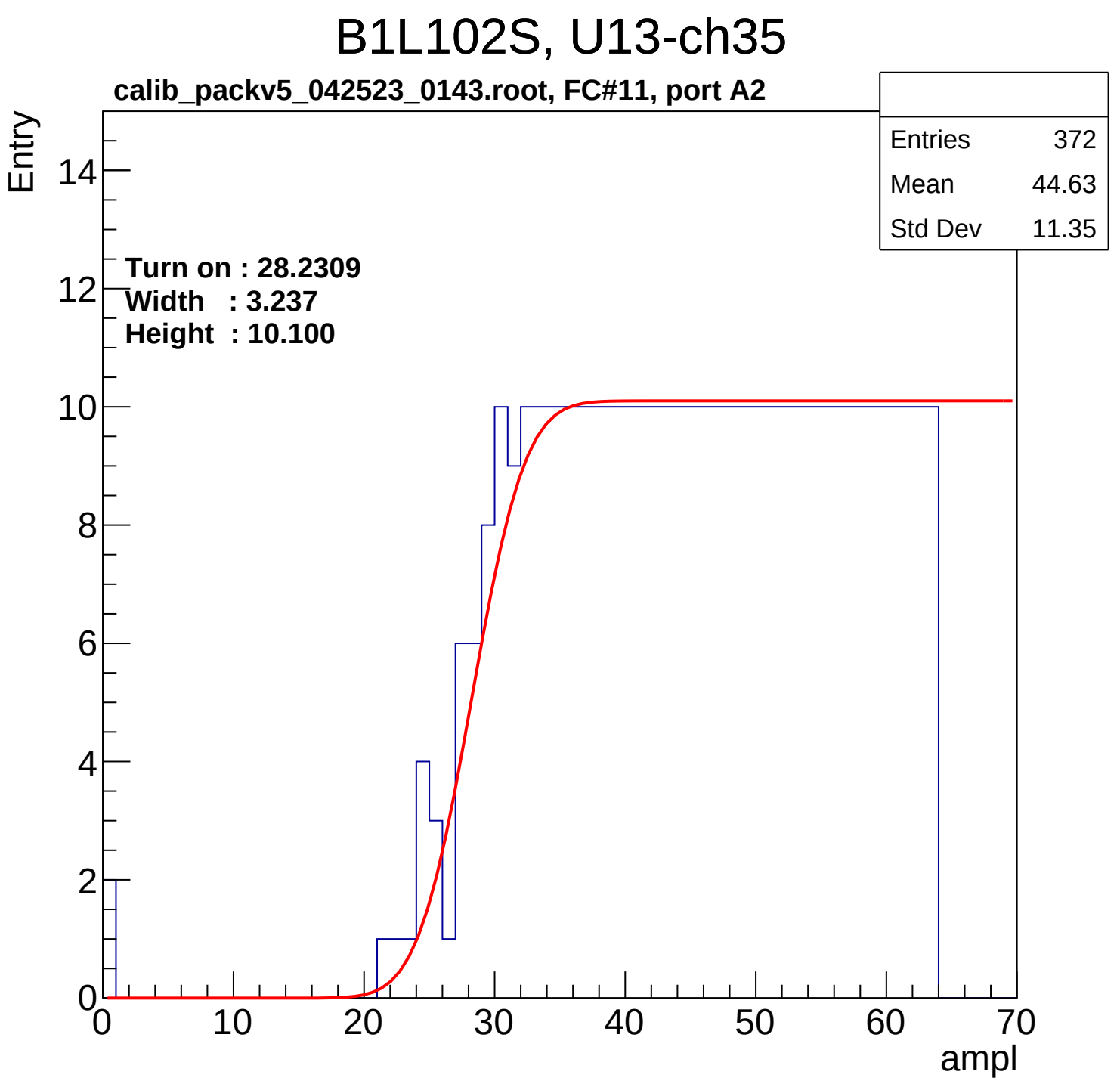
B1L102S, U13-ch35
calib_packv5_042523_0143.root, FC#11, port A2
Entries 372
Mean 44.63
Std Dev 11.35
Turn on : 28.2309
Width : 3.237
Height : 10.100
Entry
ampl
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6
8
10
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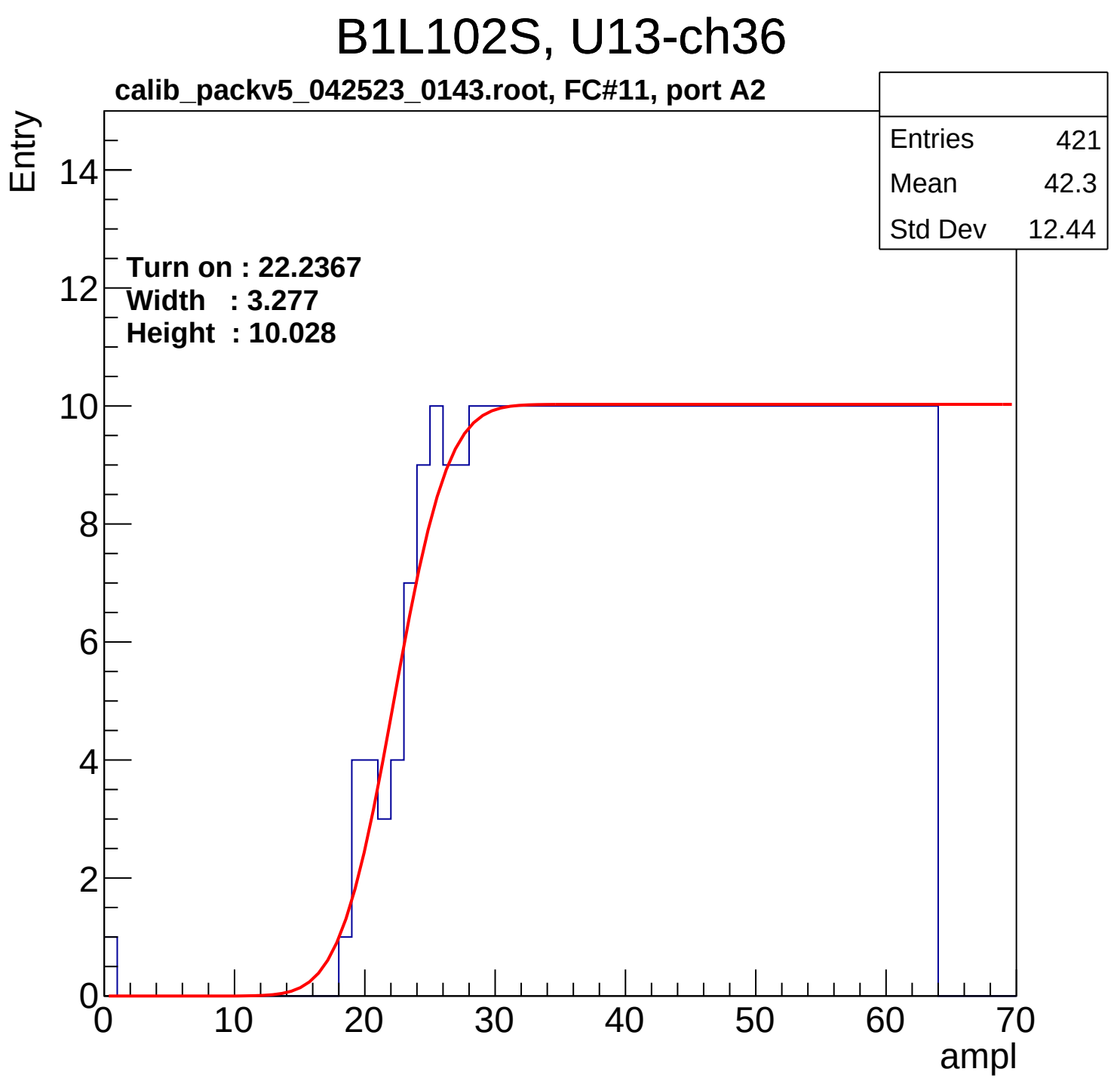
B1L102S, U13-ch36
calib_packv5_042523_0143.root, FC#11, port A2
Entries 421
Mean 42.3
Std Dev 12.44
Turn on : 22.2367
Width : 3.277
Height : 10.028
Entry
ampl
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2
4
6
8
10
12
14
0
10
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40
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60
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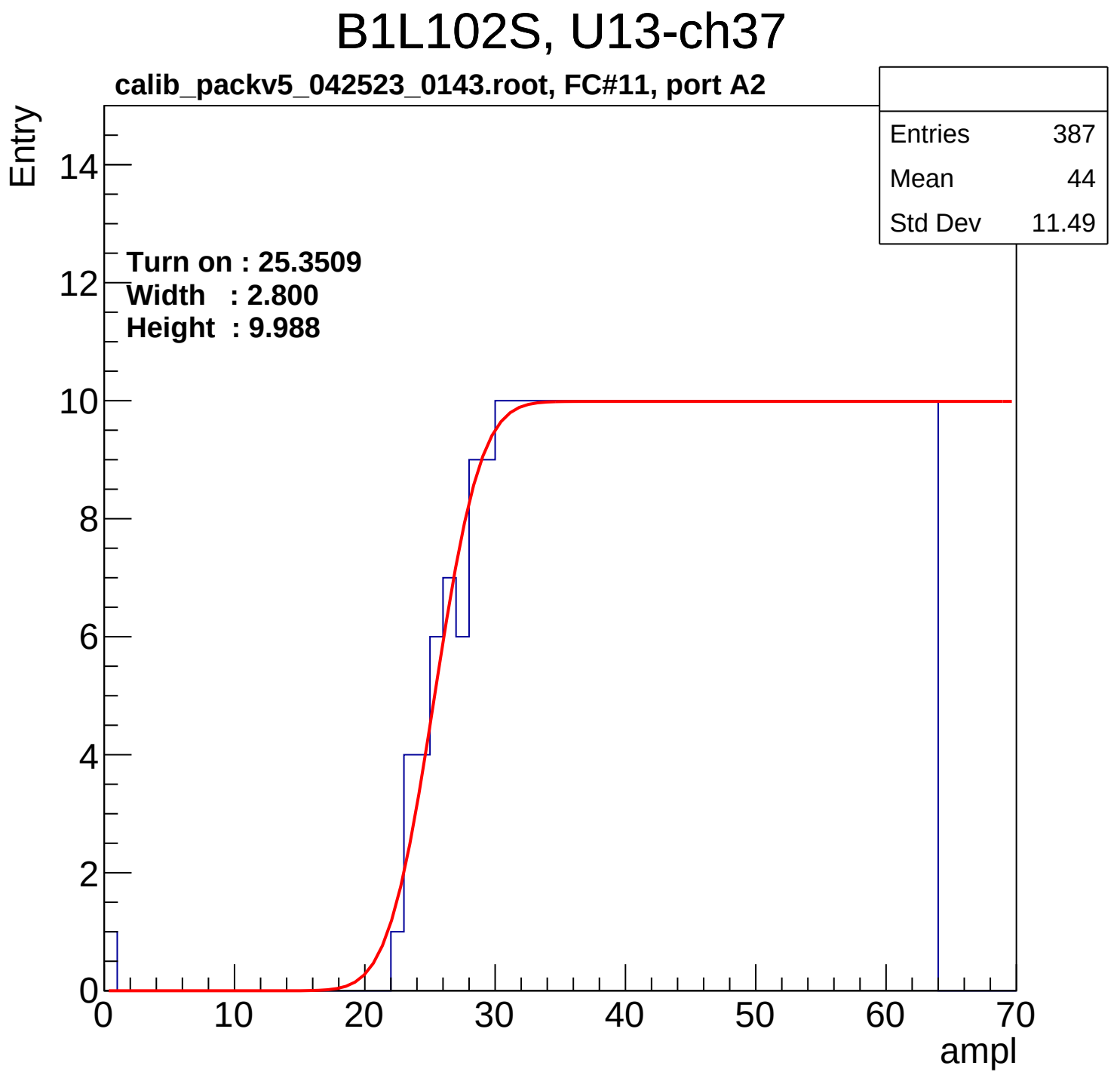
B1L102S, U13-ch37
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 44
Std Dev 11.49
Turn on : 25.3509
Width : 2.800
Height : 9.988
Entry
ampl
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2
4
6
8
10
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0
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60
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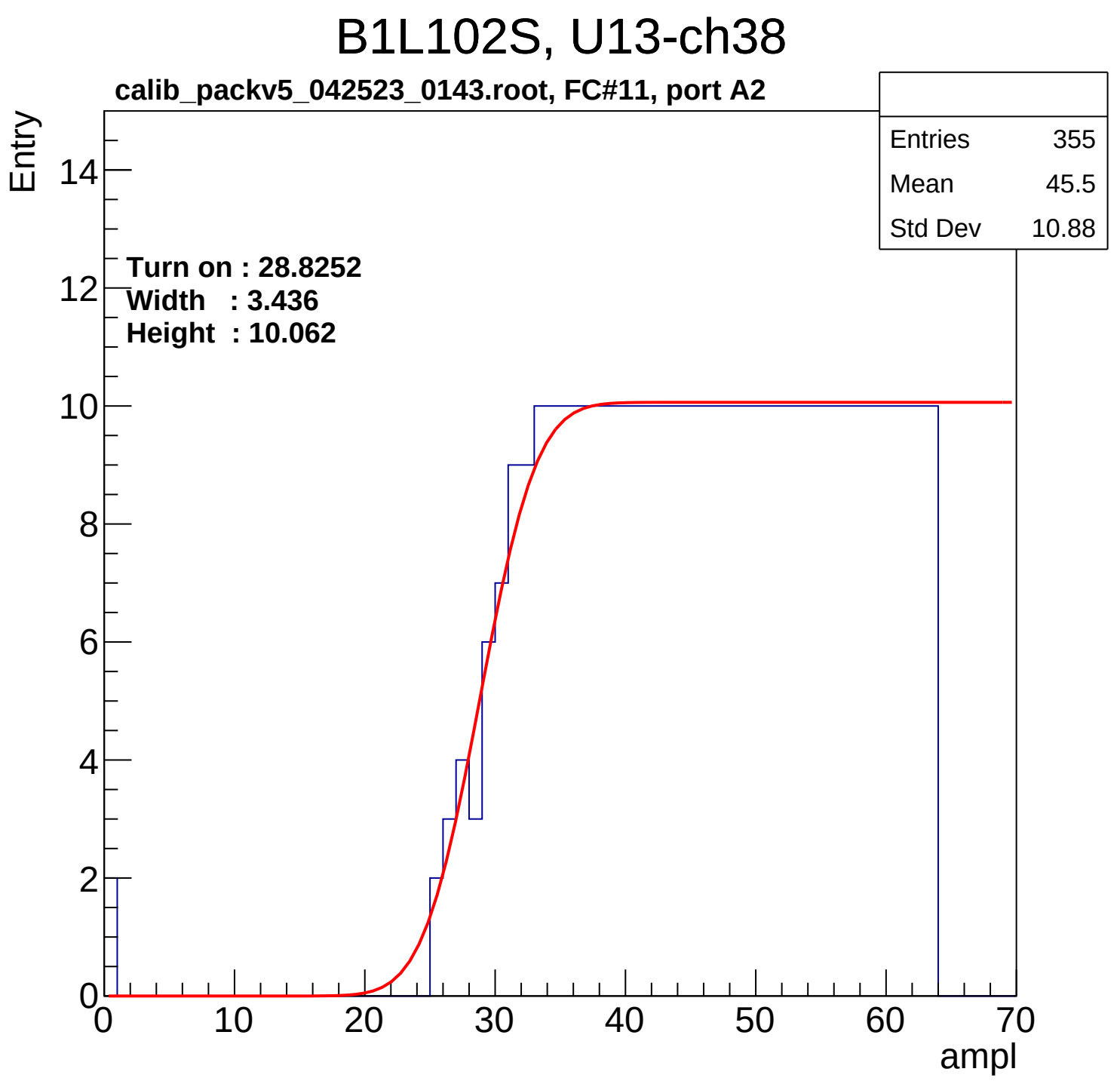
B1L102S, U13-ch38
calib_packv5_042523_0143.root, FC#11, port A2
Entries 355
Mean 45.5
Std Dev 10.88
Turn on : 28.8252
Width : 3.436
Height : 10.062
Entry
ampl
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4
6
8
10
12
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0
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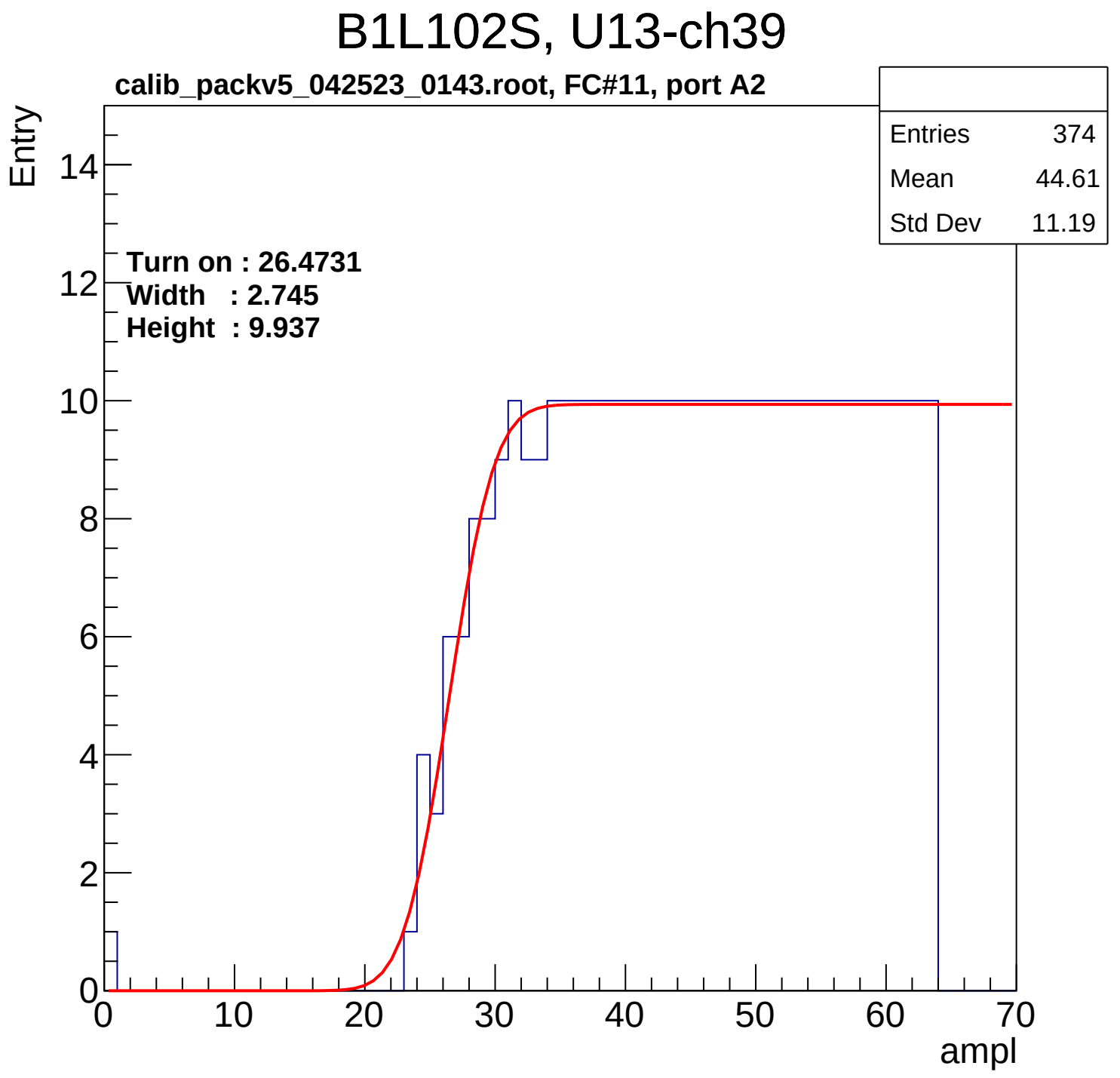
B1L102S, U13-ch39
calib_packv5_042523_0143.root, FC#11, port A2
Entries 374
Mean 44.61
Std Dev 11.19
Turn on : 26.4731
Width : 2.745
Height : 9.937
Entry
ampl
0
2
4
6
8
10
12
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0
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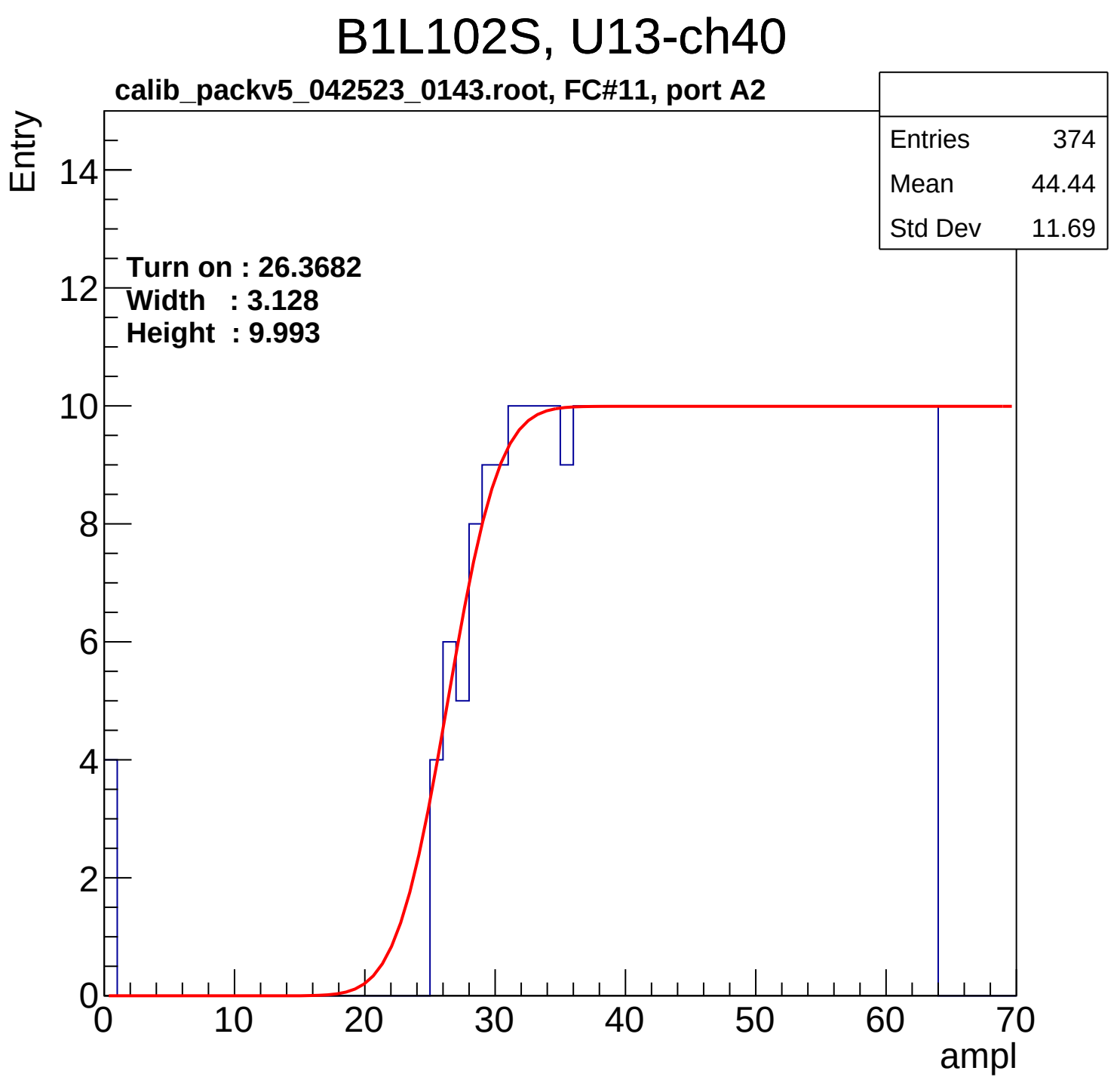
B1L102S, U13-ch40
calib_packv5_042523_0143.root, FC#11, port A2
Entries 374
Mean 44.44
Std Dev 11.69
Turn on : 26.3682
Width : 3.128
Height : 9.993
Entry
ampl
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2
4
6
8
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12
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0
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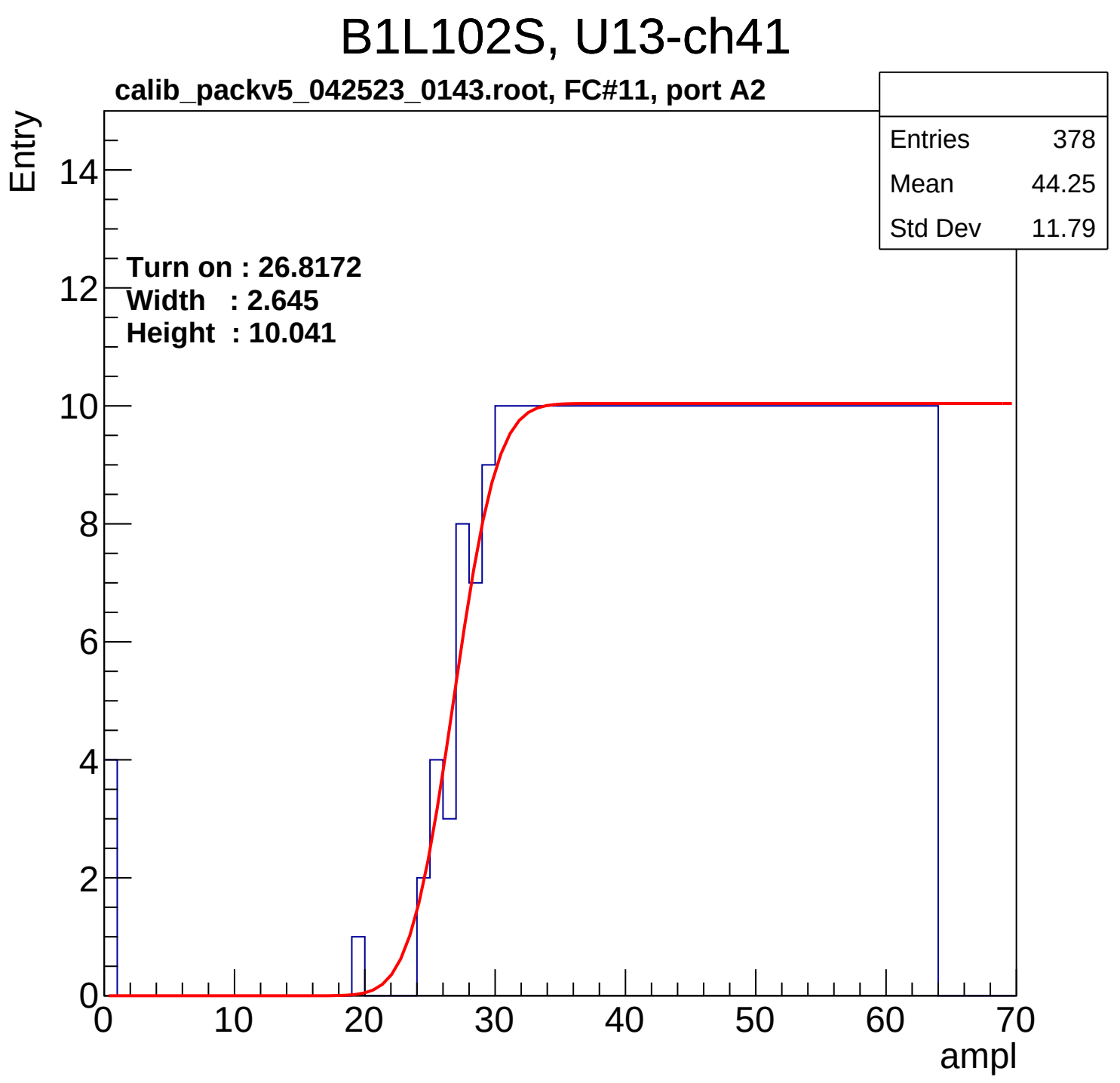
B1L102S, U13-ch41
calib_packv5_042523_0143.root, FC#11, port A2
Entries 378
Mean 44.25
Std Dev 11.79
Turn on : 26.8172
Width : 2.645
Height : 10.041
Entry
ampl
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6
8
10
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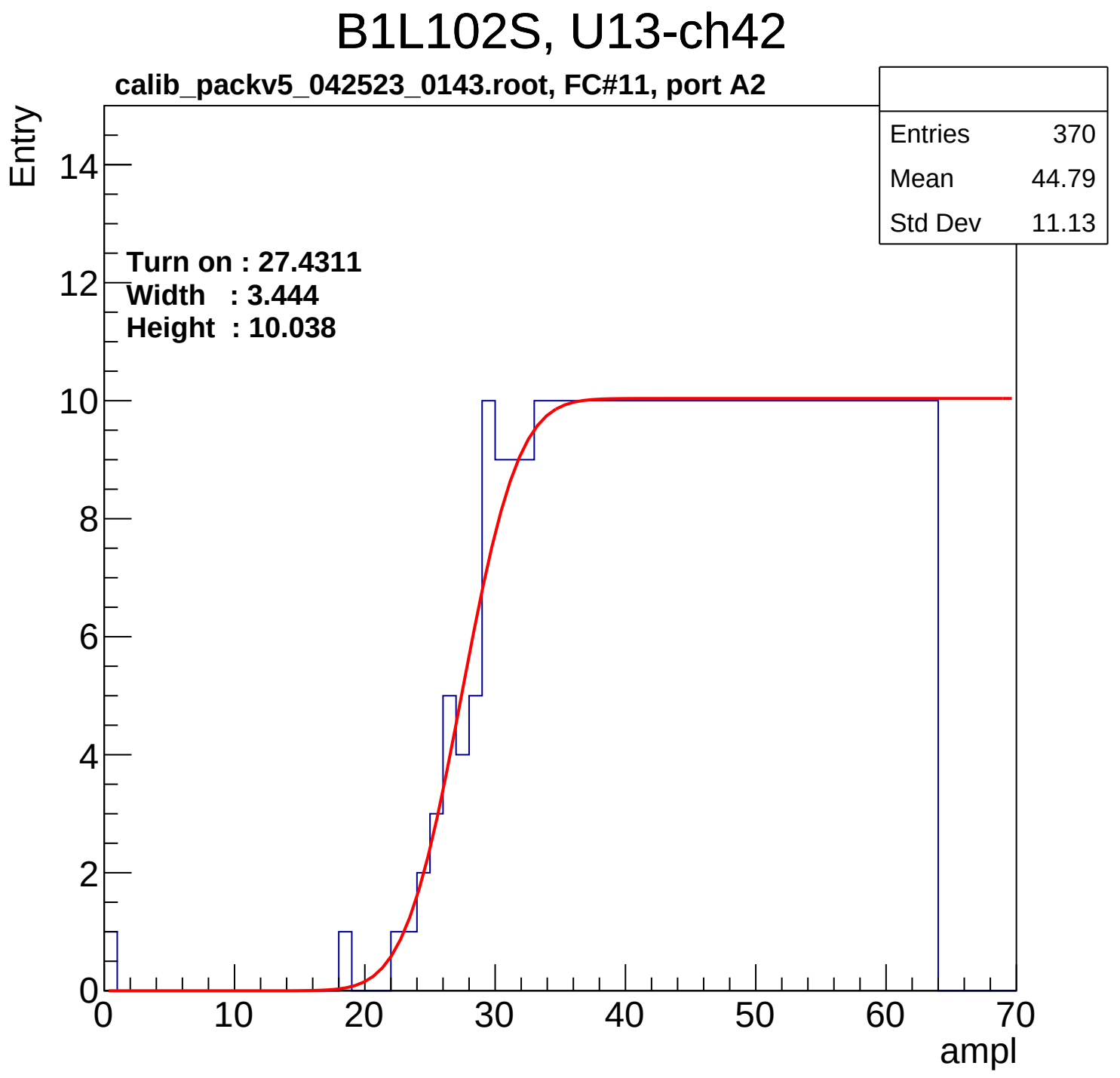
B1L102S, U13-ch42
calib_packv5_042523_0143.root, FC#11, port A2
Entries 370
Mean 44.79
Std Dev 11.13
Turn on : 27.4311
Width : 3.444
Height : 10.038
Entry
ampl
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2
4
6
8
10
12
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0
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20
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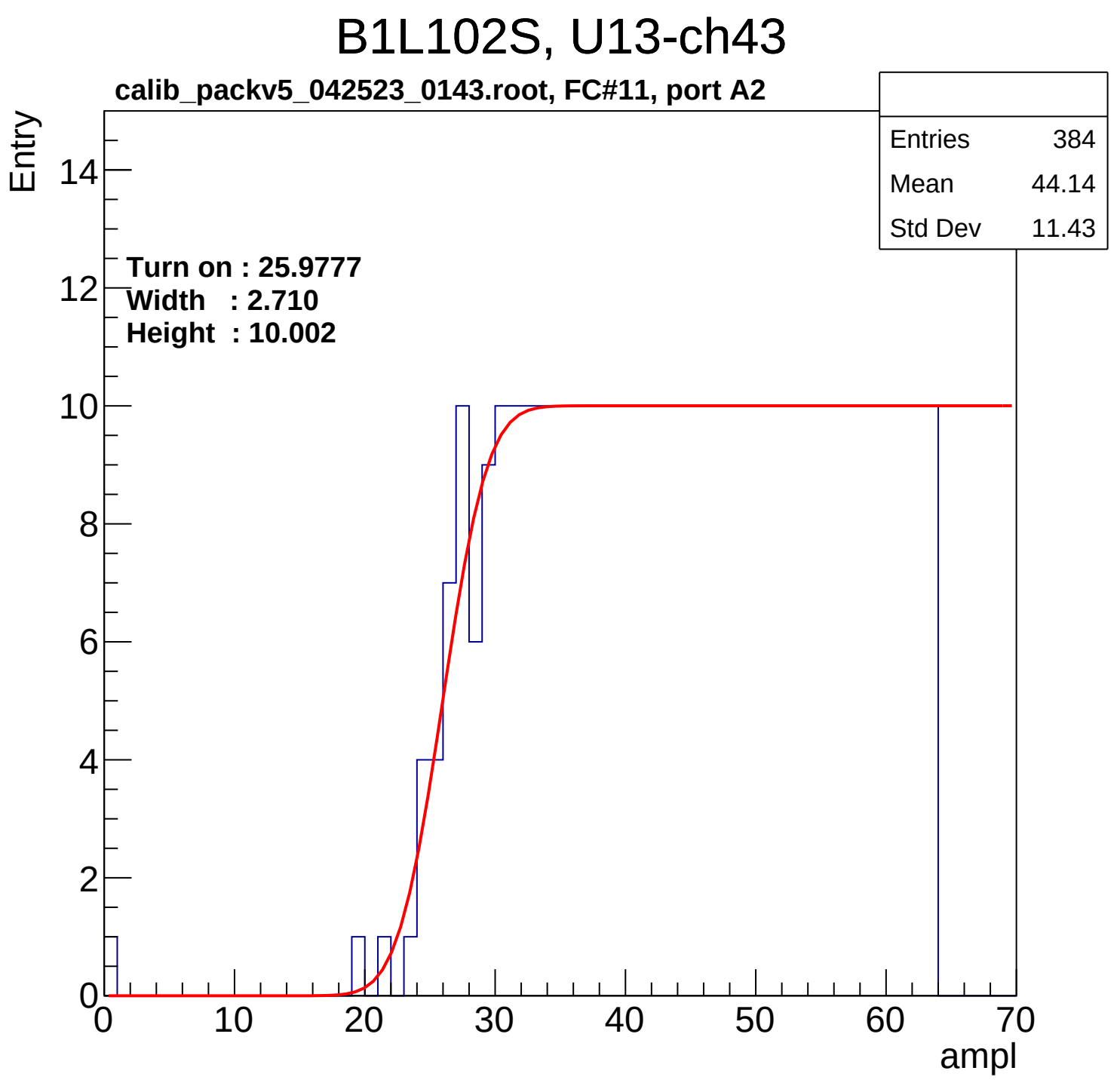
B1L102S, U13-ch43
calib_packv5_042523_0143.root, FC#11, port A2
Entries 384
Mean 44.14
Std Dev 11.43
Turn on : 25.9777
Width : 2.710
Height : 10.002
Entry
ampl
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6
8
10
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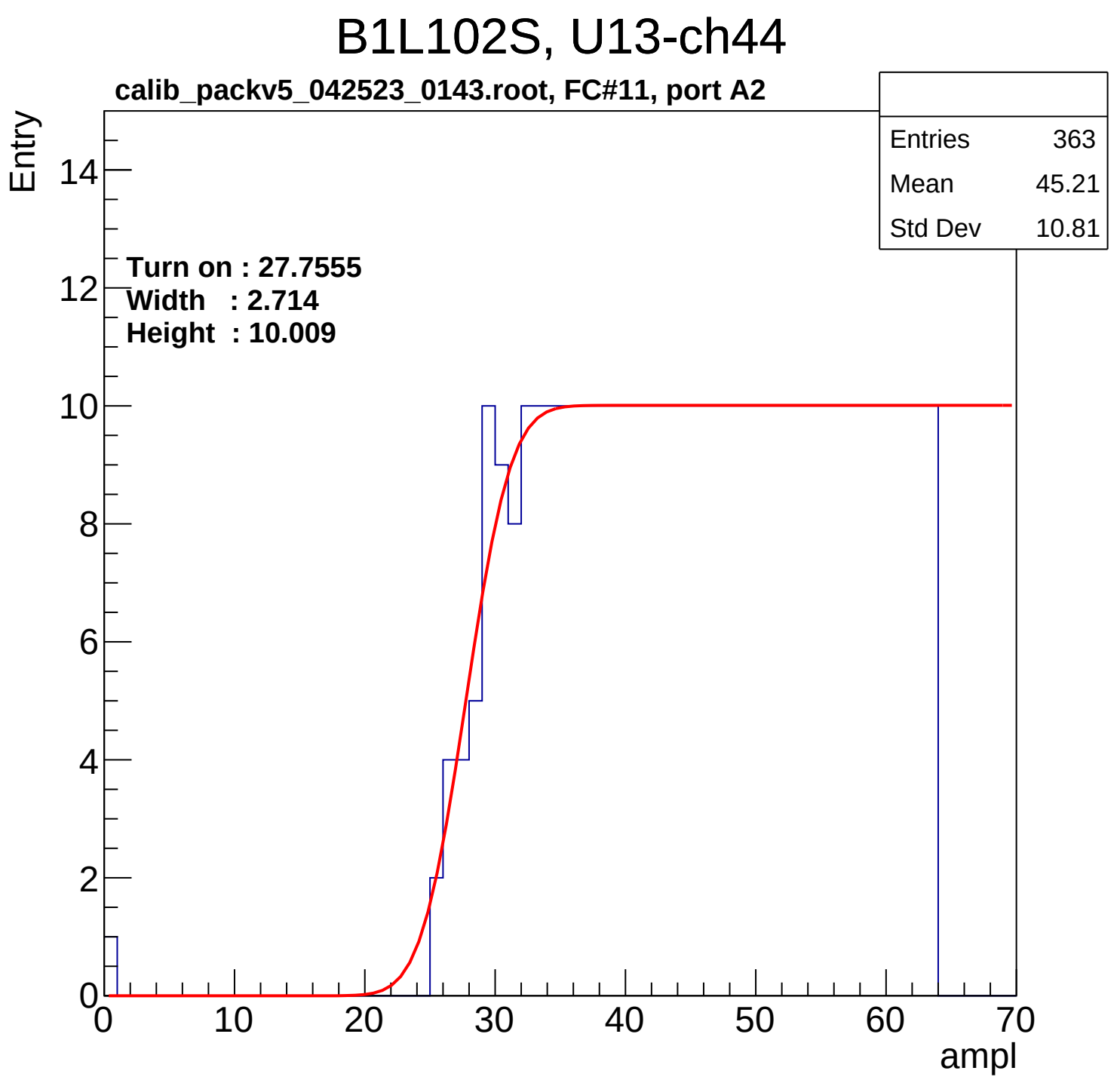
B1L102S, U13-ch44
calib_packv5_042523_0143.root, FC#11, port A2
Entries 363
Mean 45.21
Std Dev 10.81
Turn on : 27.7555
Width : 2.714
Height : 10.009
Entry
ampl
0
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6
8
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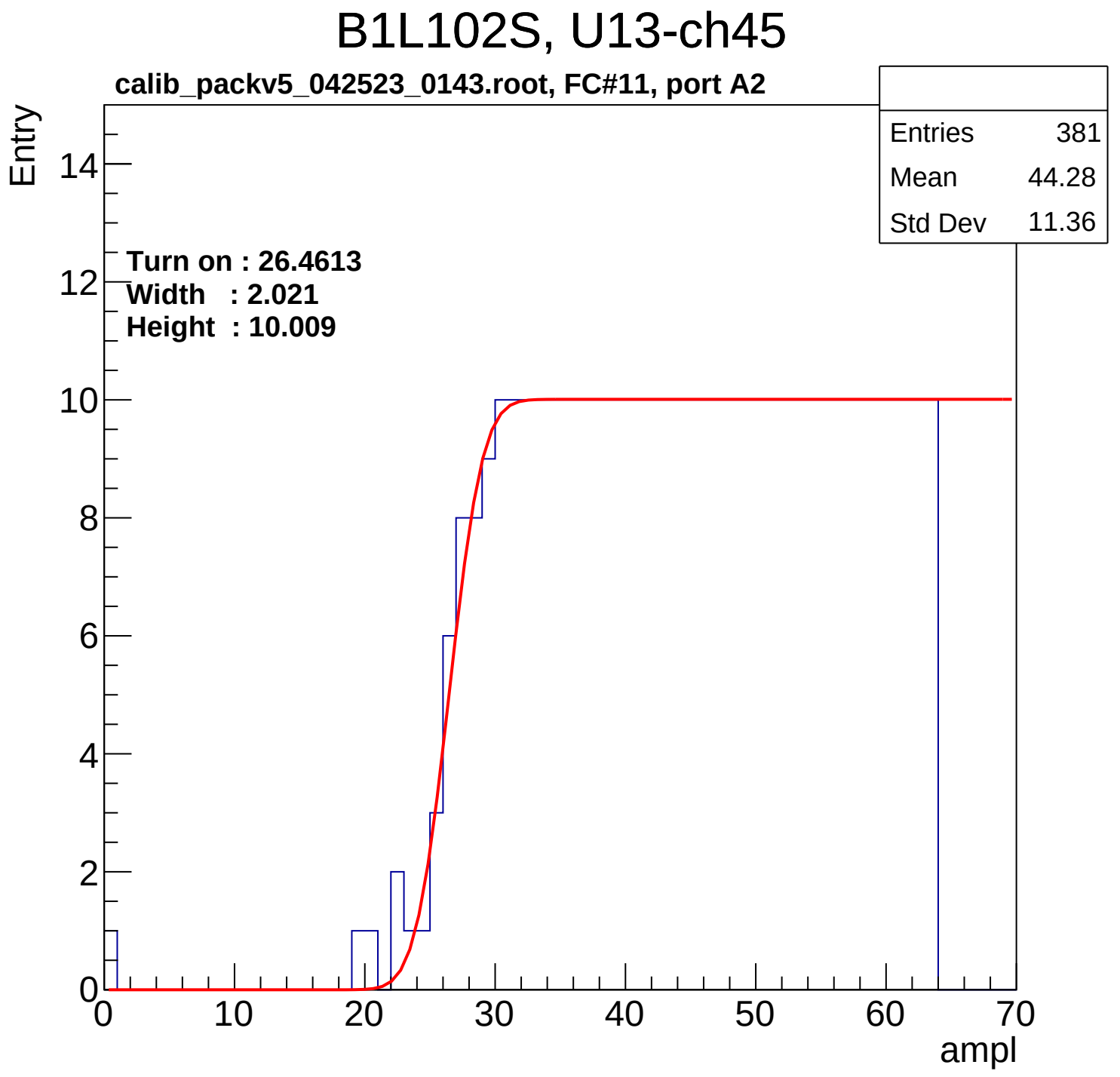
B1L102S, U13-ch45
calib_packv5_042523_0143.root, FC#11, port A2
Entries 381
Mean 44.28
Std Dev 11.36
Turn on : 26.4613
Width : 2.021
Height : 10.009
Entry
ampl
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2
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6
8
10
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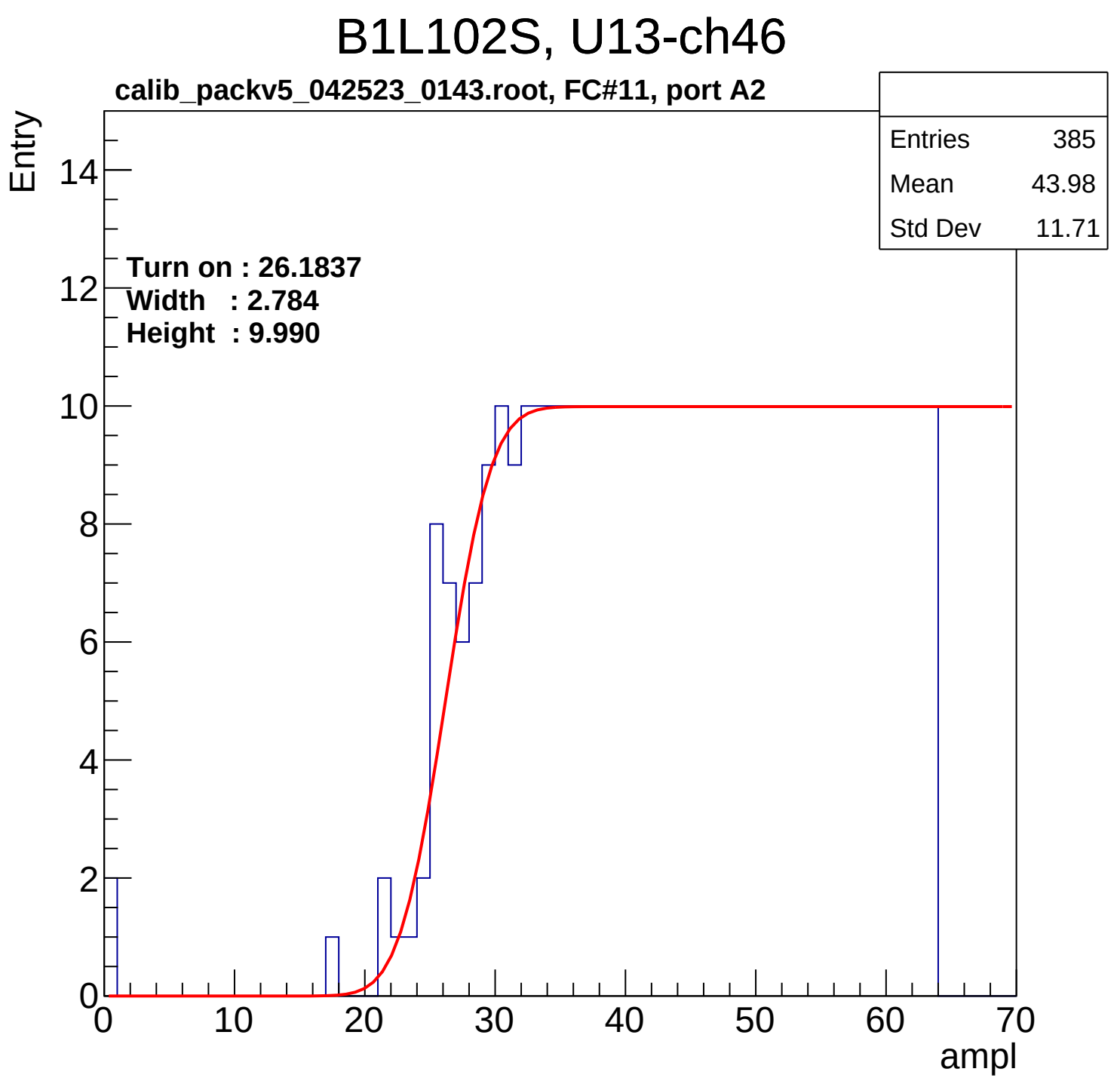
B1L102S, U13-ch46
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 43.98
Std Dev 11.71
Turn on : 26.1837
Width : 2.784
Height : 9.990
Entry
ampl
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2
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6
8
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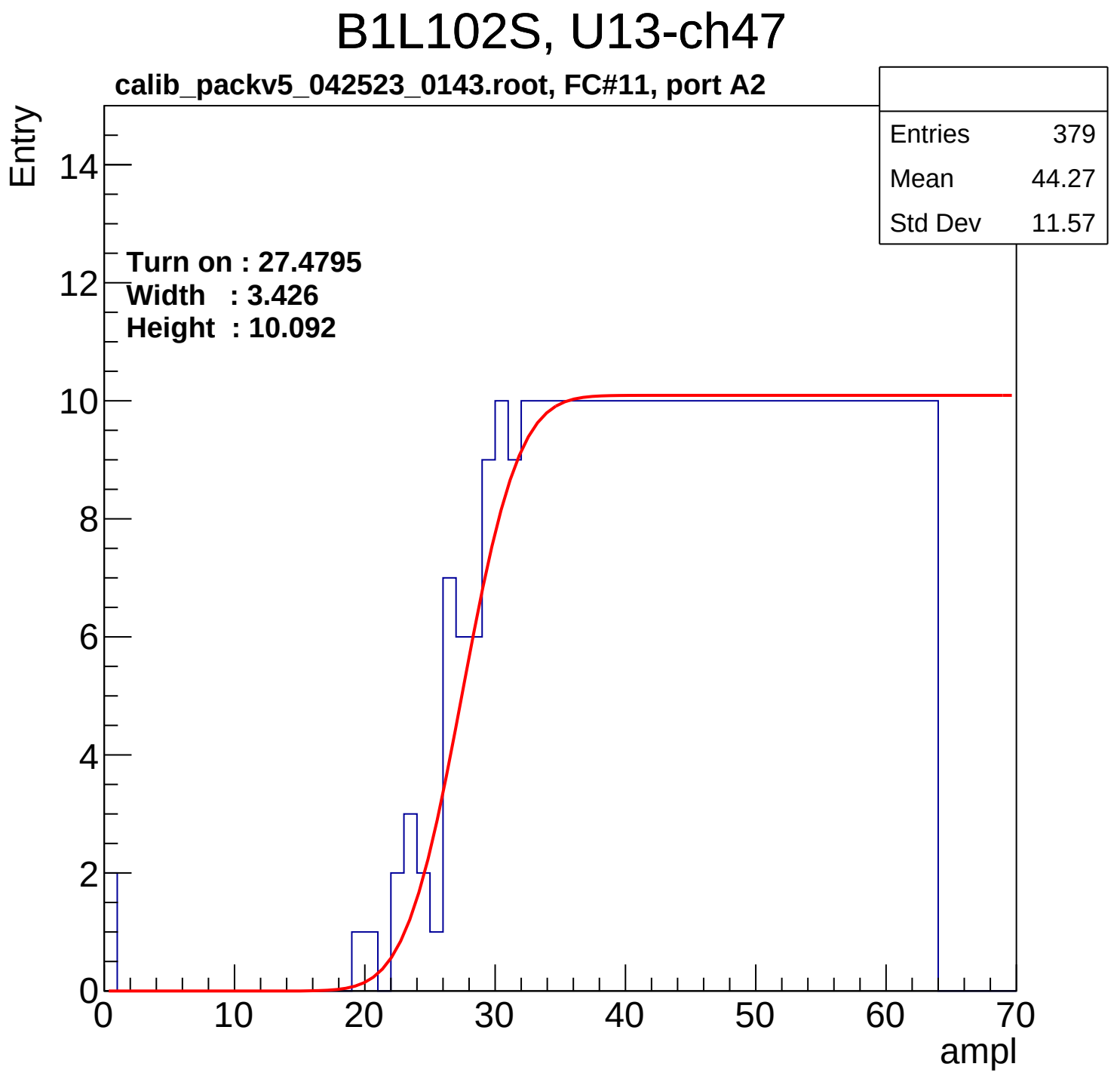
B1L102S, U13-ch47
calib_packv5_042523_0143.root, FC#11, port A2
Entries 379
Mean 44.27
Std Dev 11.57
Turn on : 27.4795
Width : 3.426
Height : 10.092
Entry
ampl
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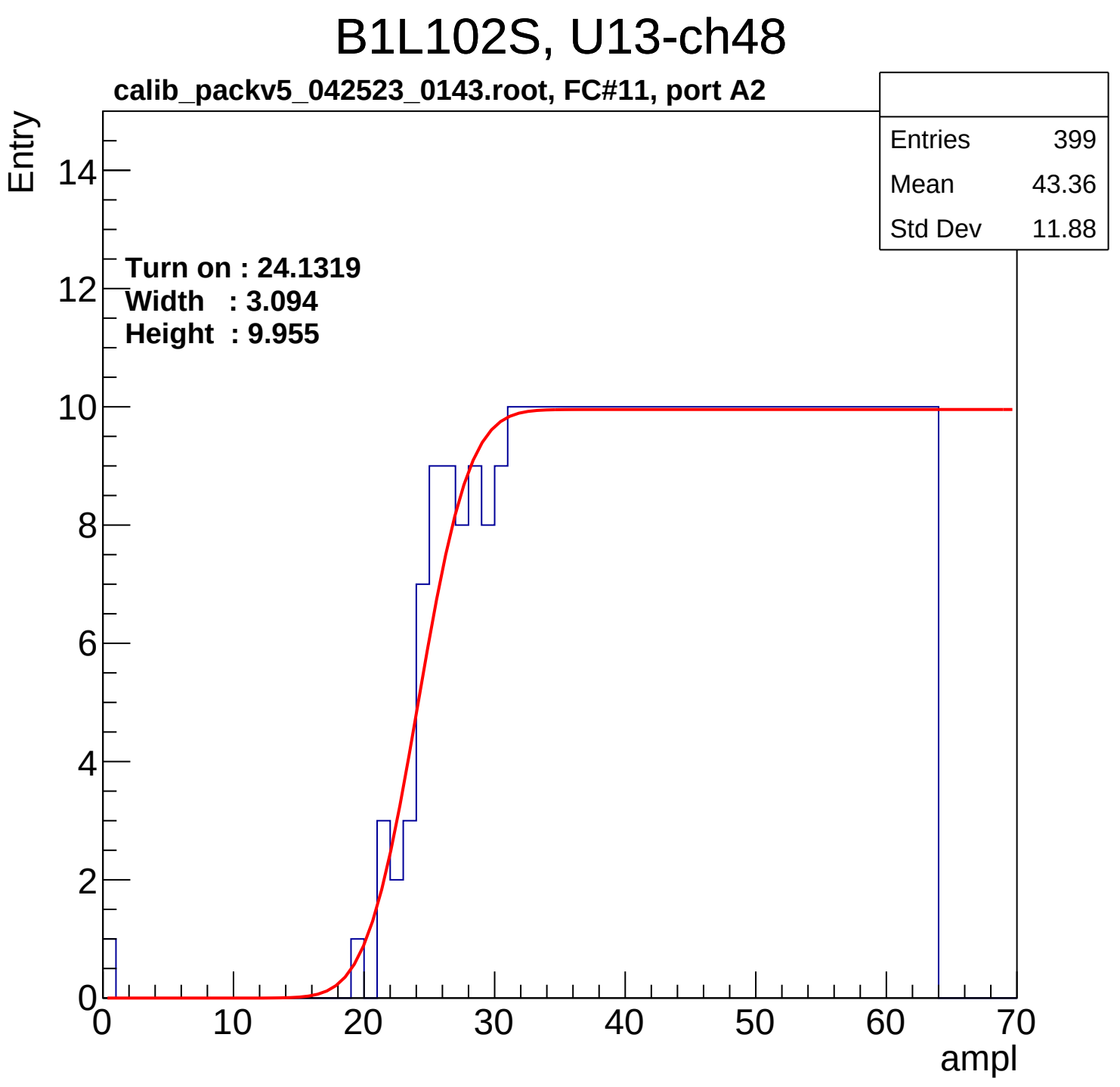
B1L102S, U13-ch48
calib_packv5_042523_0143.root, FC#11, port A2
Entries 399
Mean 43.36
Std Dev 11.88
Turn on : 24.1319
Width : 3.094
Height : 9.955
Entry
ampl
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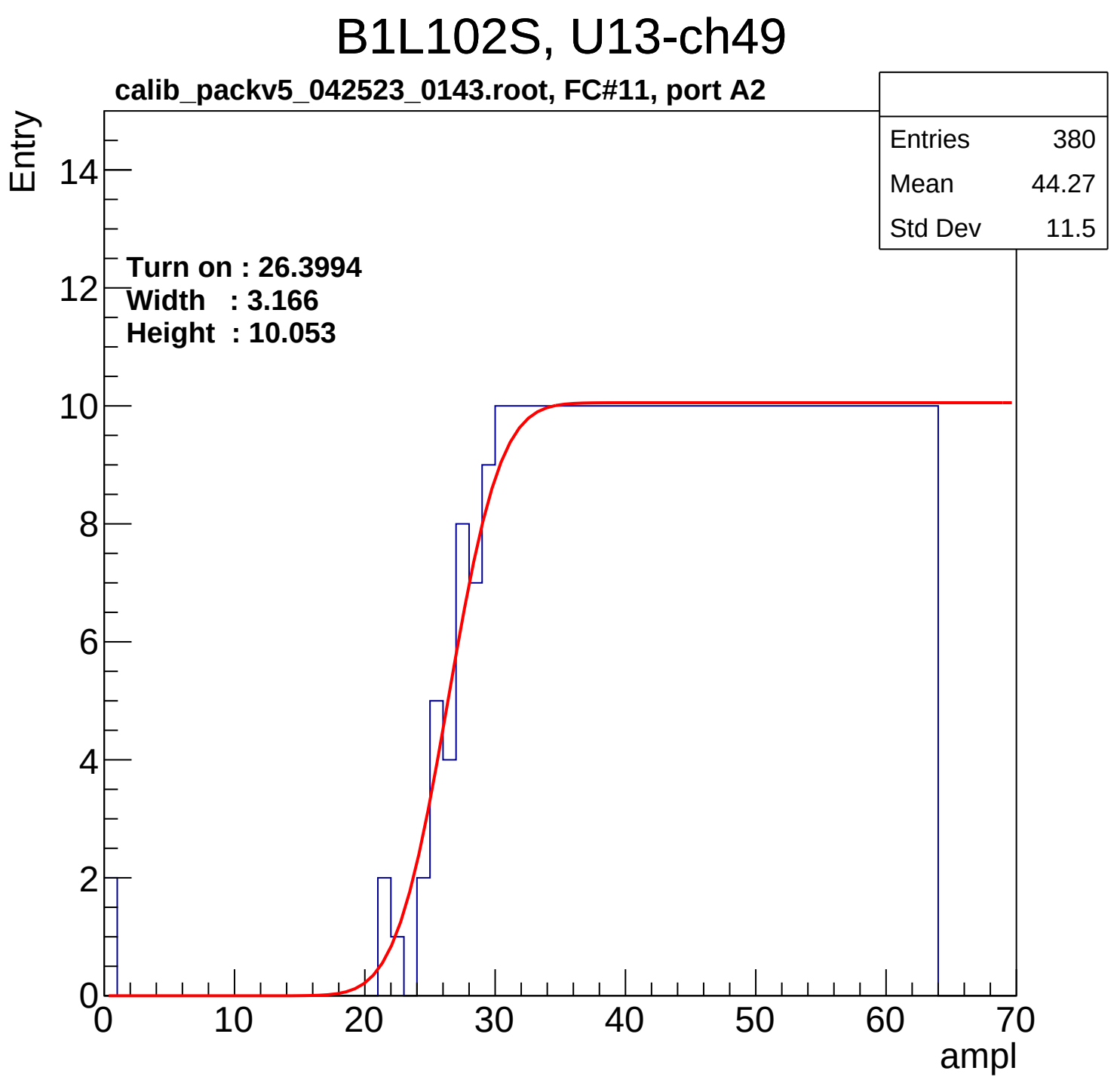
B1L102S, U13-ch49
calib_packv5_042523_0143.root, FC#11, port A2
Entries 380
Mean 44.27
Std Dev 11.5
Turn on : 26.3994
Width : 3.166
Height : 10.053
Entry
ampl
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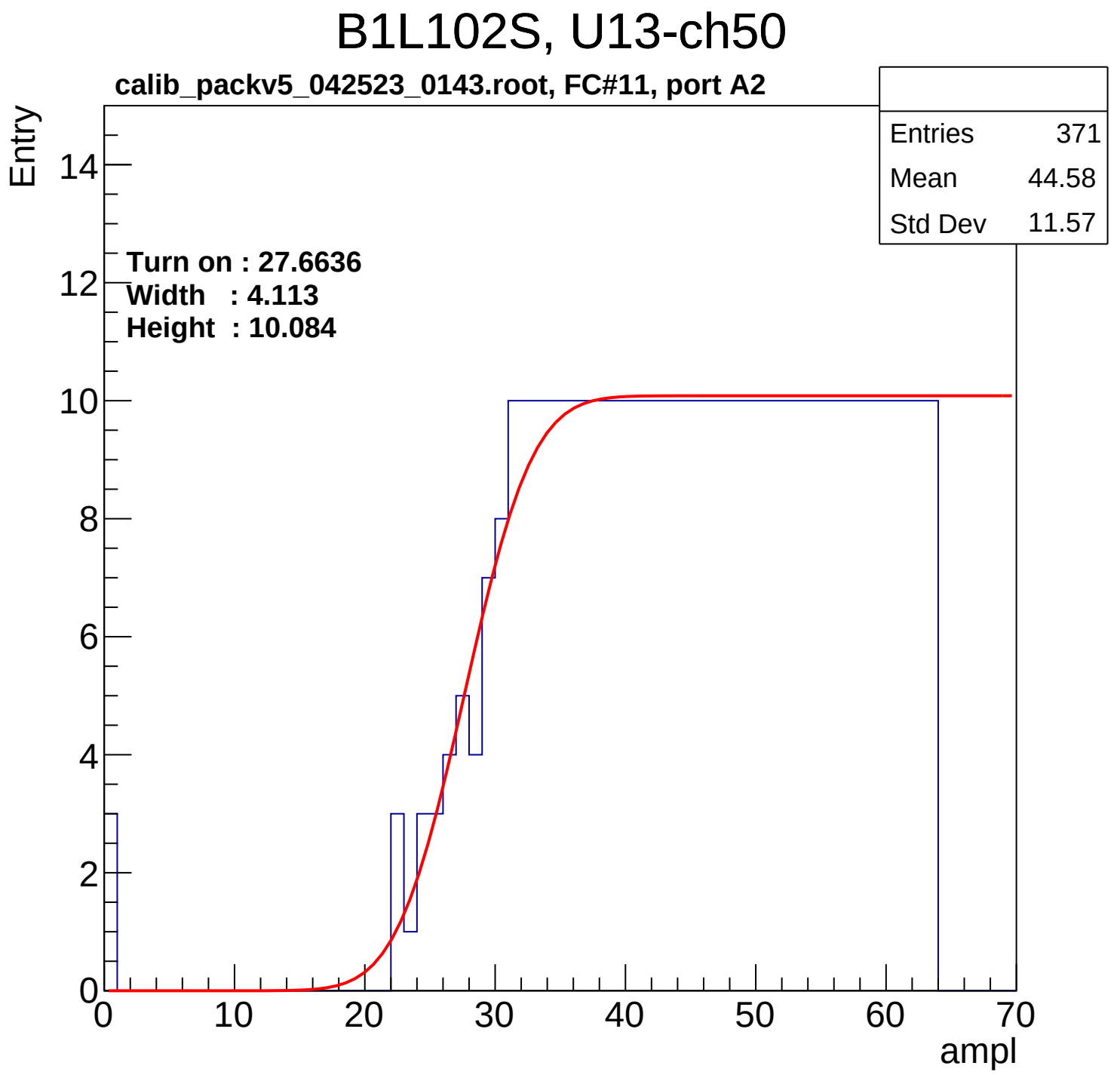
B1L102S, U13-ch50
calib_packv5_042523_0143.root, FC#11, port A2
Entries 371
Mean 44.58
Std Dev 11.57
Turn on : 27.6636
Width : 4.113
Height : 10.084
Entry
ampl
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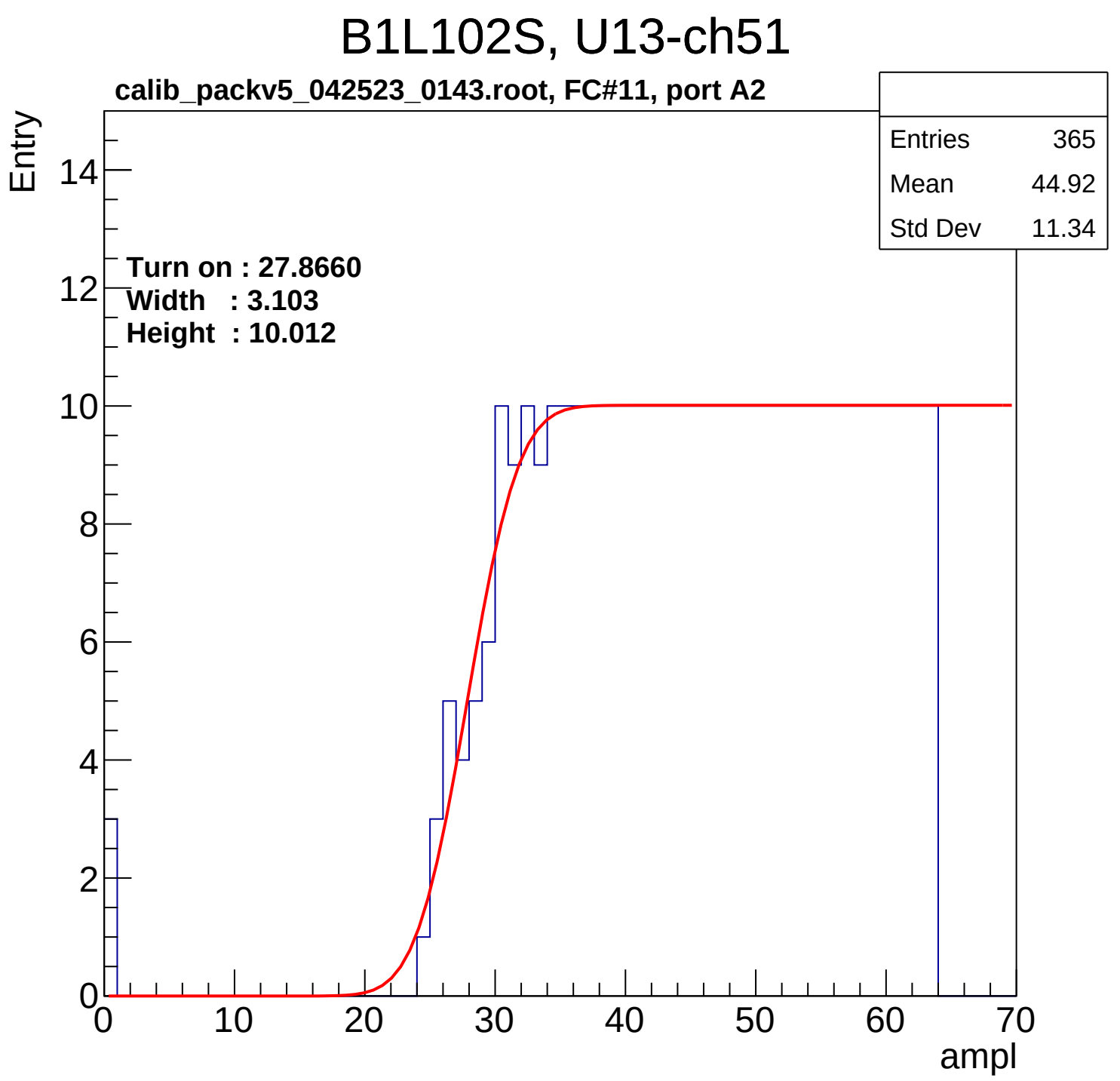
B1L102S, U13-ch51
calib_packv5_042523_0143.root, FC#11, port A2
Entries 365
Mean 44.92
Std Dev 11.34
Turn on : 27.8660
Width : 3.103
Height : 10.012
Entry
ampl
0
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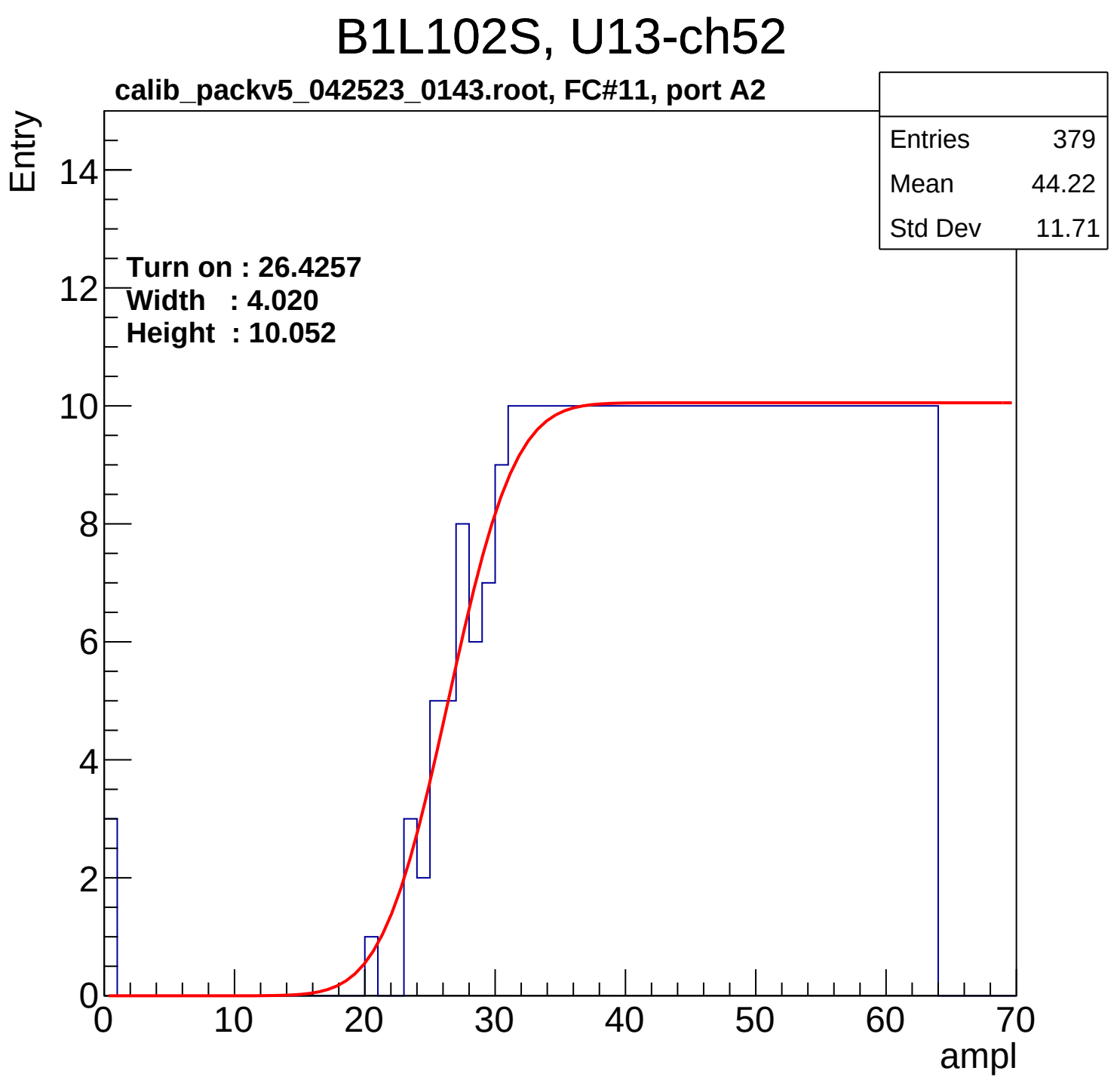
B1L102S, U13-ch52
calib_packv5_042523_0143.root, FC#11, port A2
Entries 379
Mean 44.22
Std Dev 11.71
Turn on : 26.4257
Width : 4.020
Height : 10.052
Entry
ampl
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8
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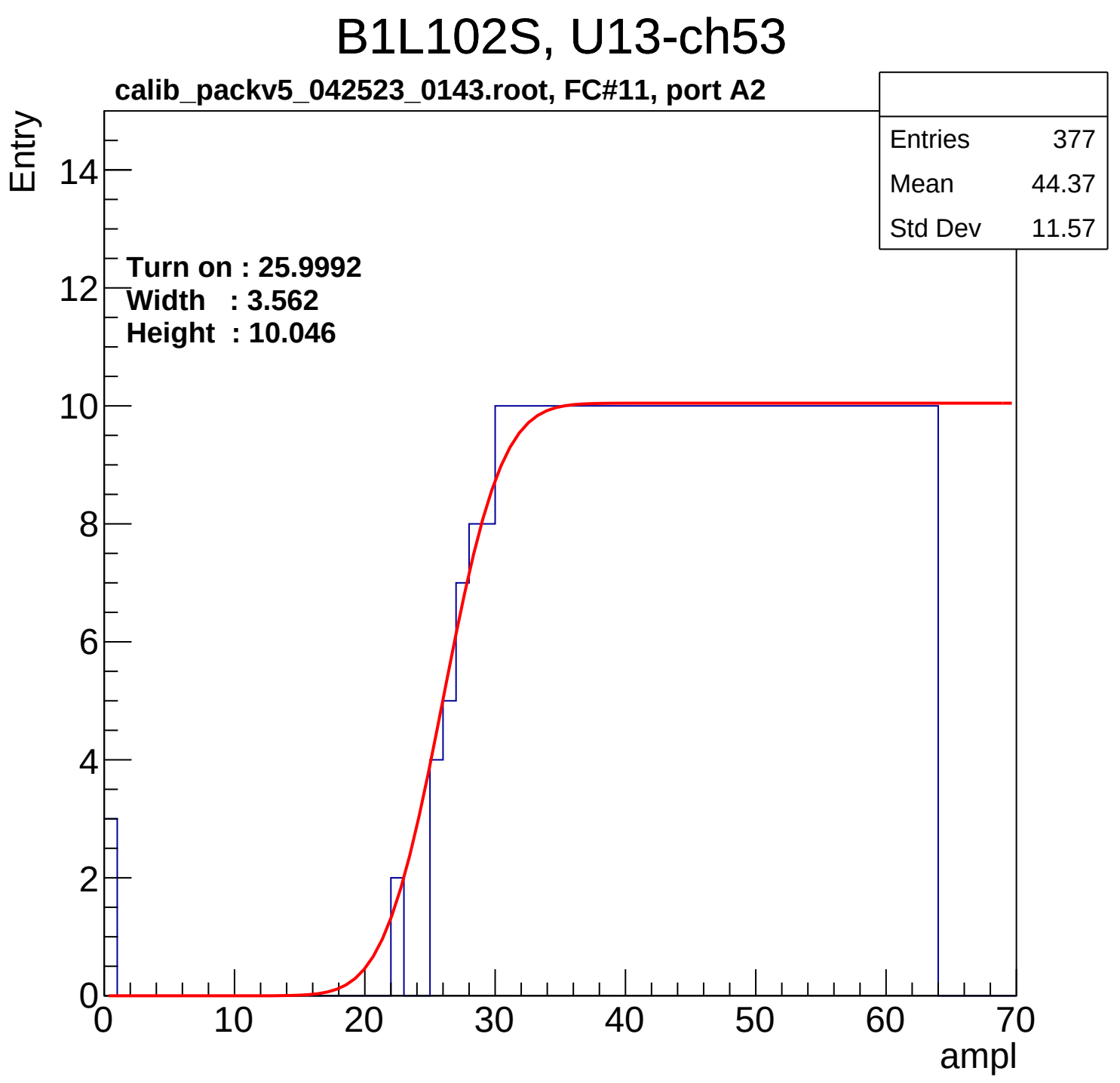
B1L102S, U13-ch53
calib_packv5_042523_0143.root, FC#11, port A2
Entries 377
Mean 44.37
Std Dev 11.57
Turn on : 25.9992
Width : 3.562
Height : 10.046
Entry
ampl
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6
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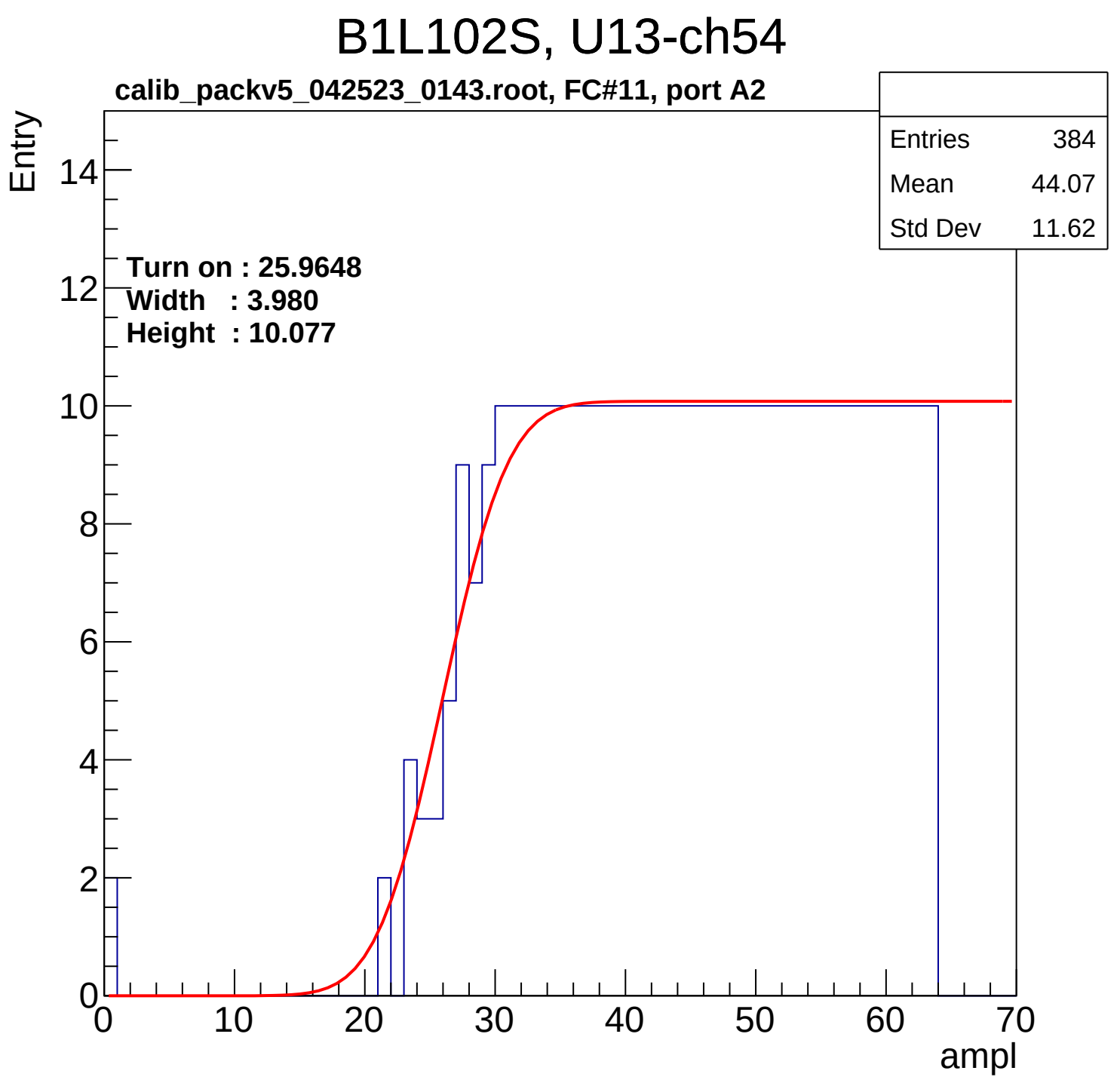
B1L102S, U13-ch54
calib_packv5_042523_0143.root, FC#11, port A2
Entries 384
Mean 44.07
Std Dev 11.62
Turn on : 25.9648
Width : 3.980
Height : 10.077
Entry
ampl
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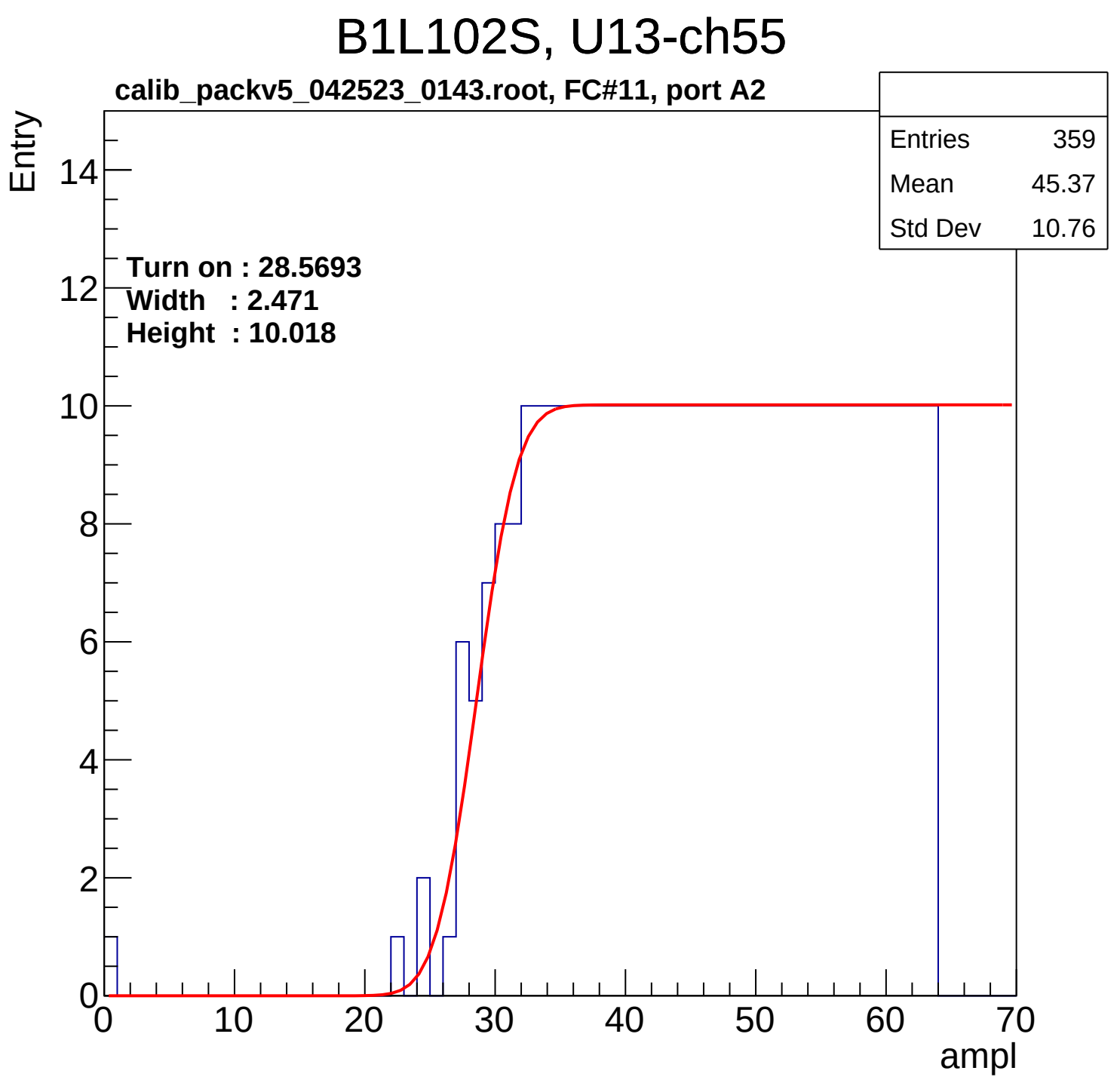
B1L102S, U13-ch55
calib_packv5_042523_0143.root, FC#11, port A2
Entries 359
Mean 45.37
Std Dev 10.76
Turn on : 28.5693
Width : 2.471
Height : 10.018
Entry
ampl
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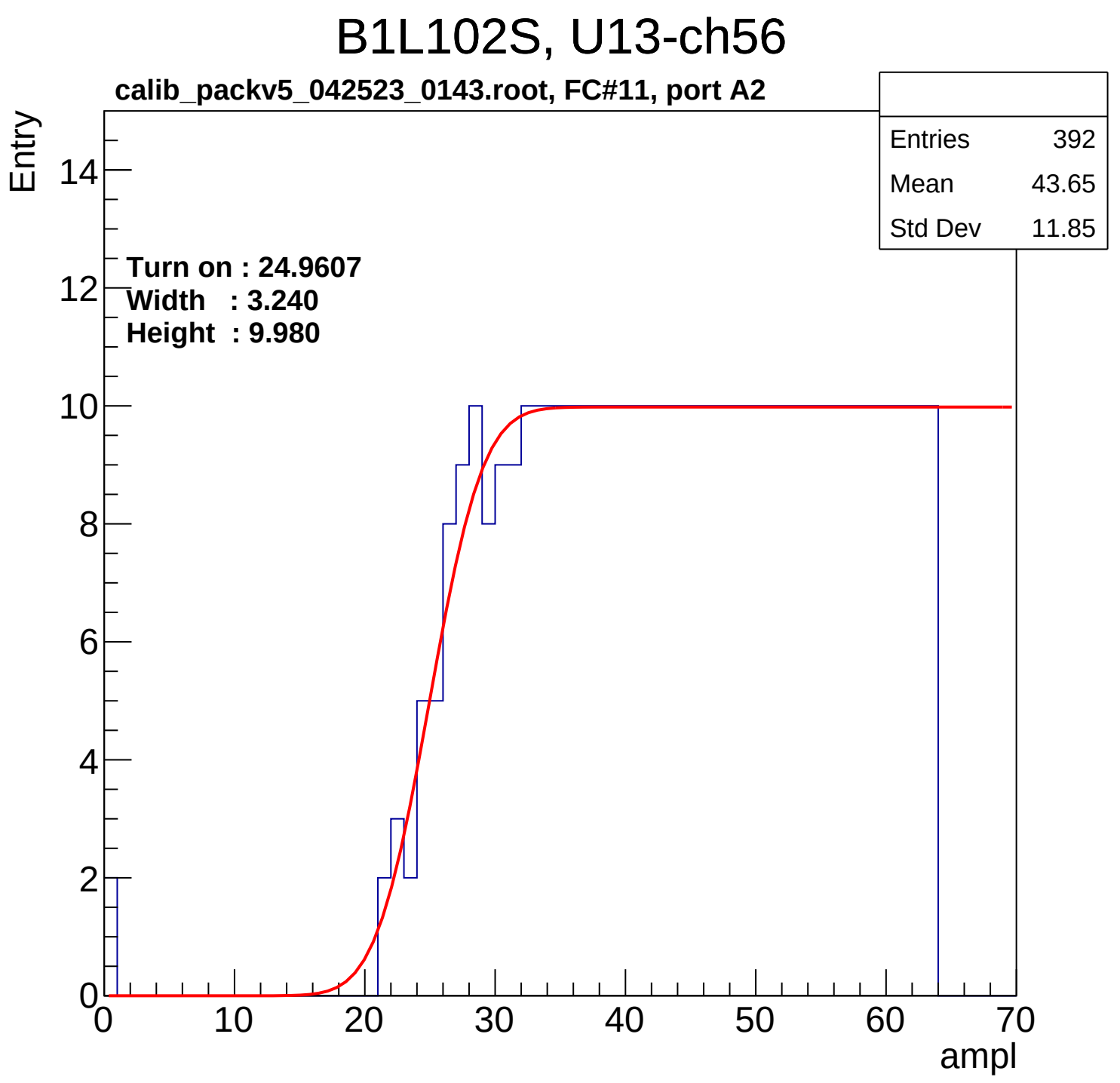
B1L102S, U13-ch56
calib_packv5_042523_0143.root, FC#11, port A2
Entries 392
Mean 43.65
Std Dev 11.85
Turn on : 24.9607
Width : 3.240
Height : 9.980
Entry
ampl
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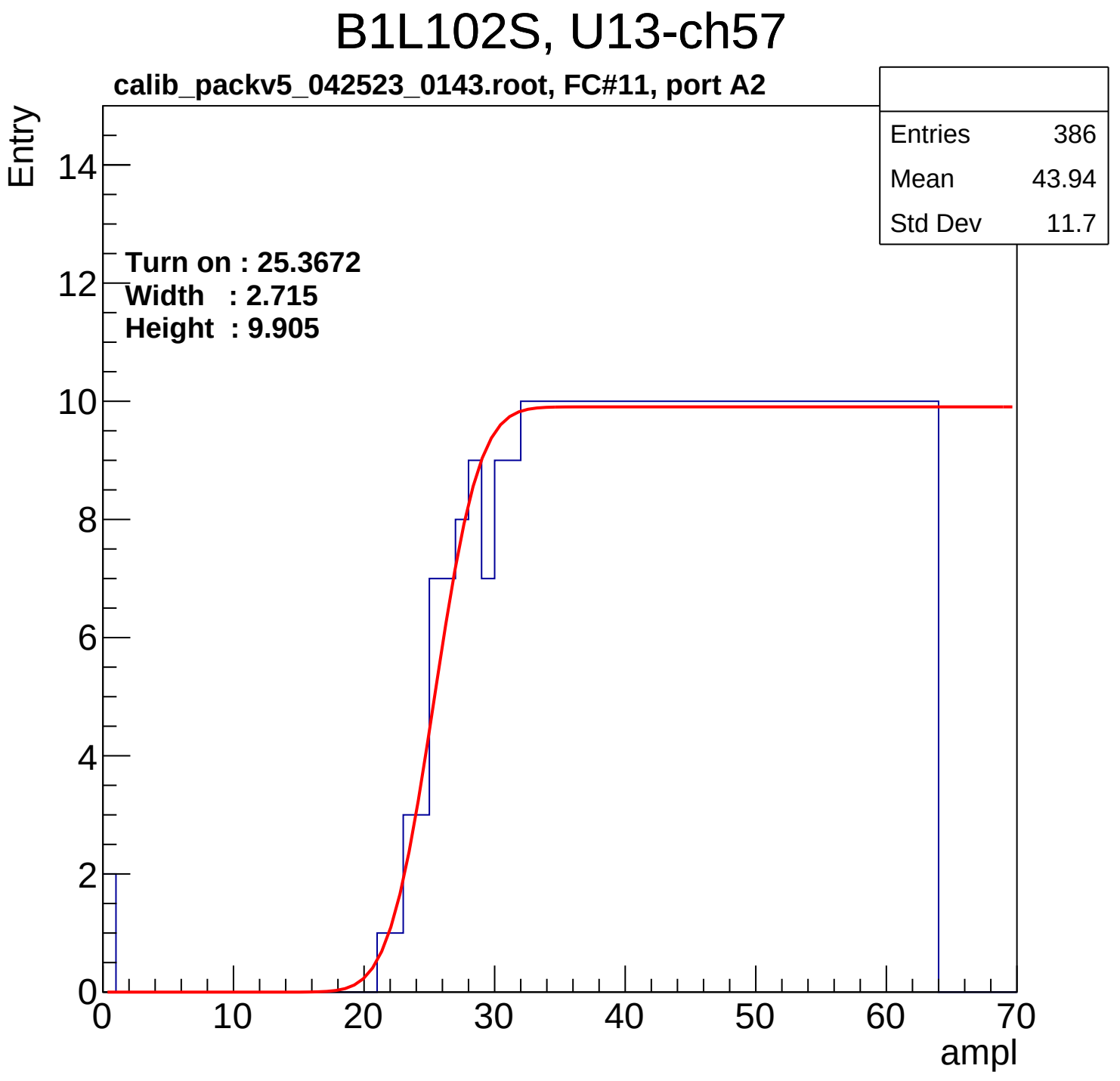
B1L102S, U13-ch57
calib_packv5_042523_0143.root, FC#11, port A2
Entries 386
Mean 43.94
Std Dev 11.7
Turn on : 25.3672
Width : 2.715
Height : 9.905
Entry
ampl
0
2
4
6
8
10
12
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10
20
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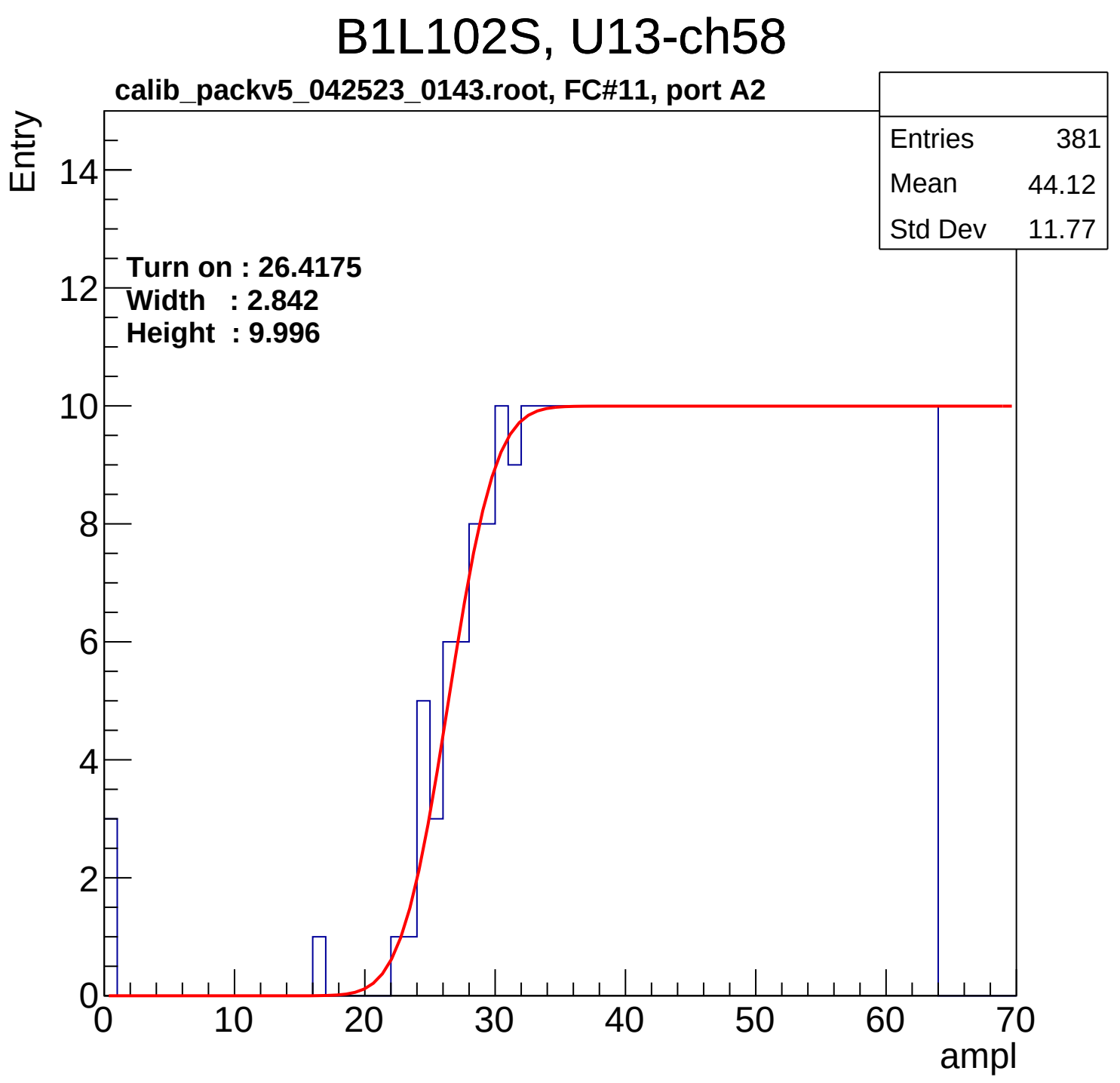
B1L102S, U13-ch58
calib_packv5_042523_0143.root, FC#11, port A2
Entries 381
Mean 44.12
Std Dev 11.77
Turn on : 26.4175
Width : 2.842
Height : 9.996
Entry
ampl
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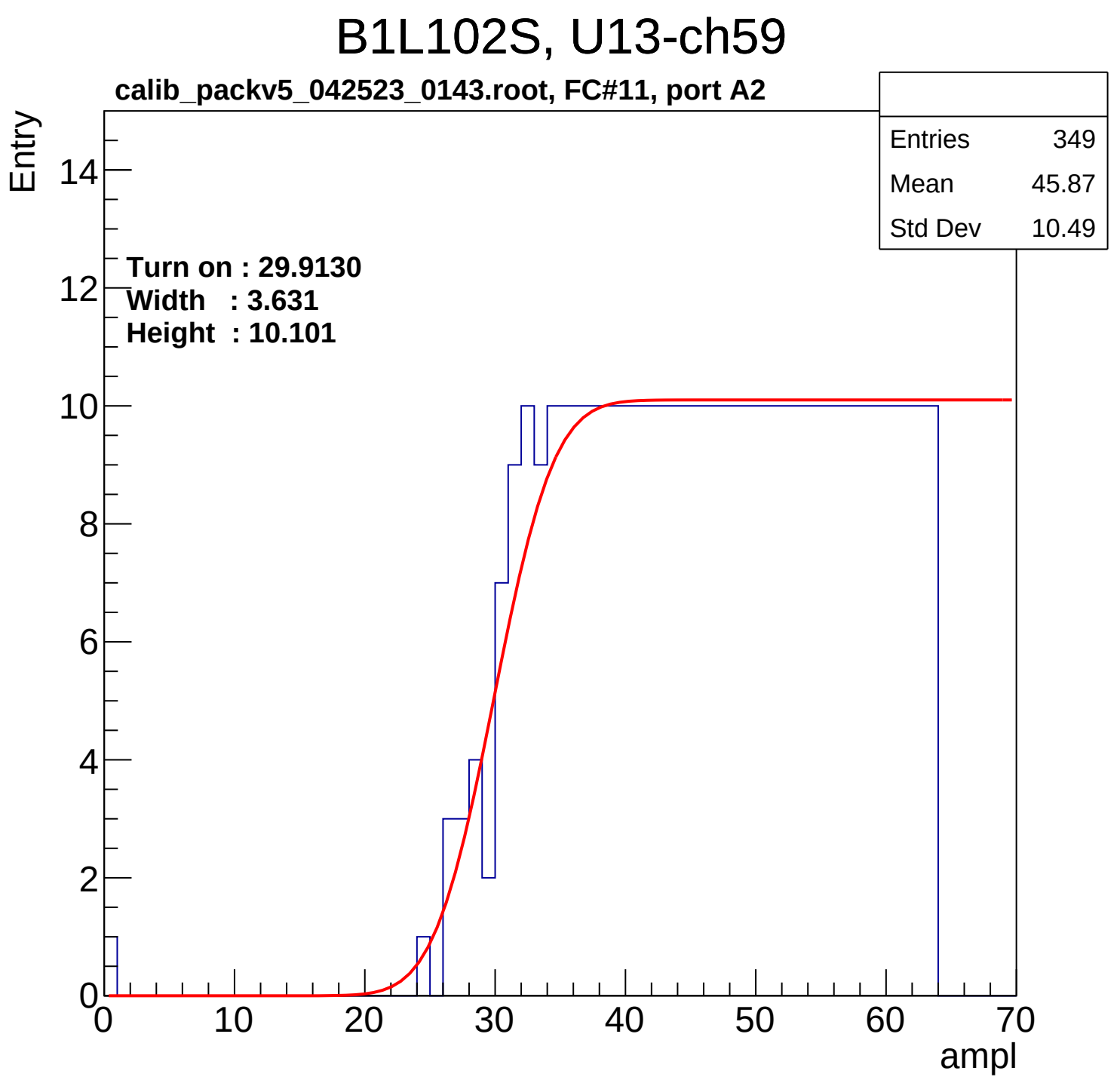
B1L102S, U13-ch59
calib_packv5_042523_0143.root, FC#11, port A2
Entries 349
Mean 45.87
Std Dev 10.49
Turn on : 29.9130
Width : 3.631
Height : 10.101
Entry
ampl
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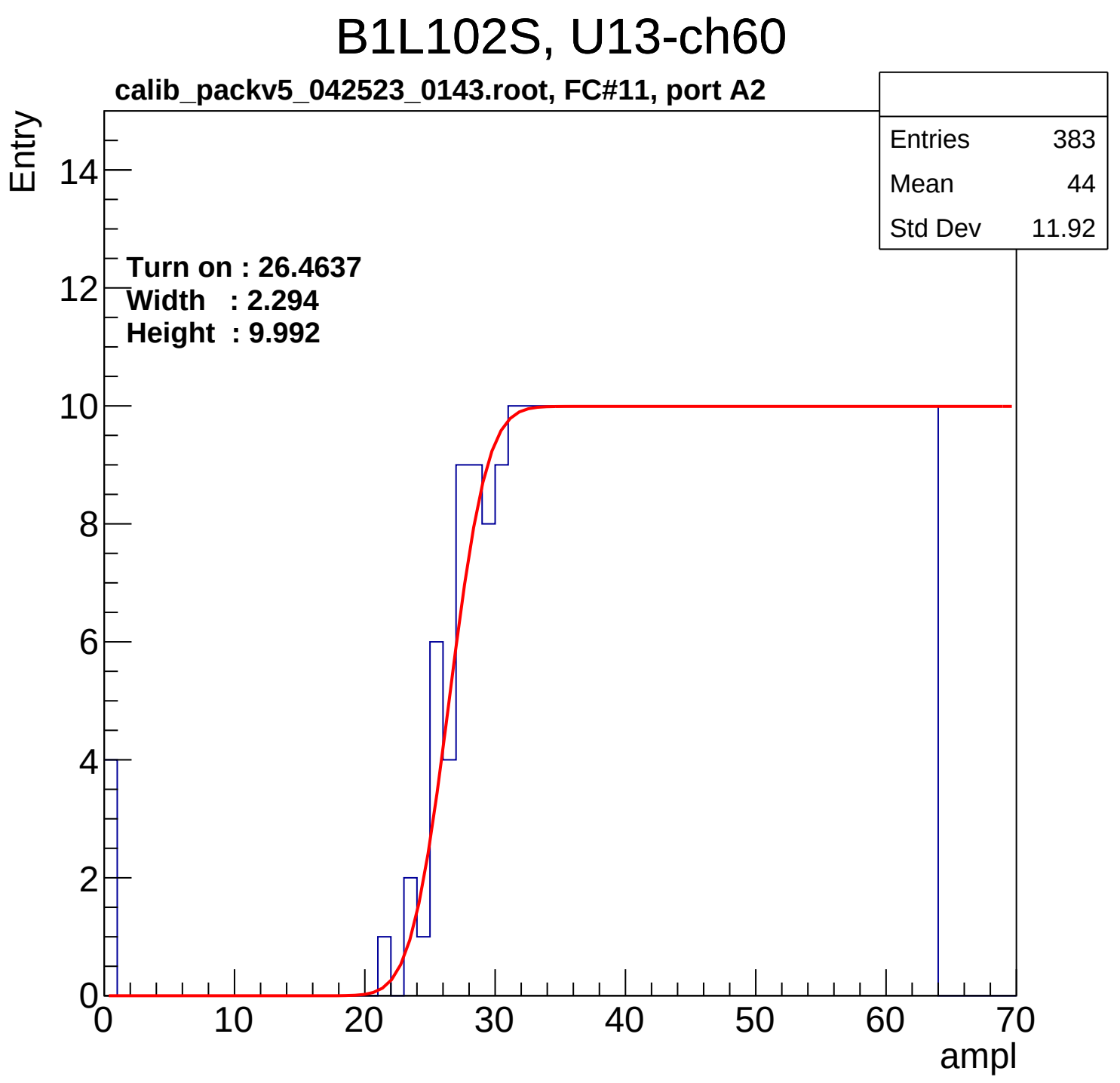
B1L102S, U13-ch60
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 44
Std Dev 11.92
Turn on : 26.4637
Width : 2.294
Height : 9.992
Entry
ampl
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2
4
6
8
10
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0
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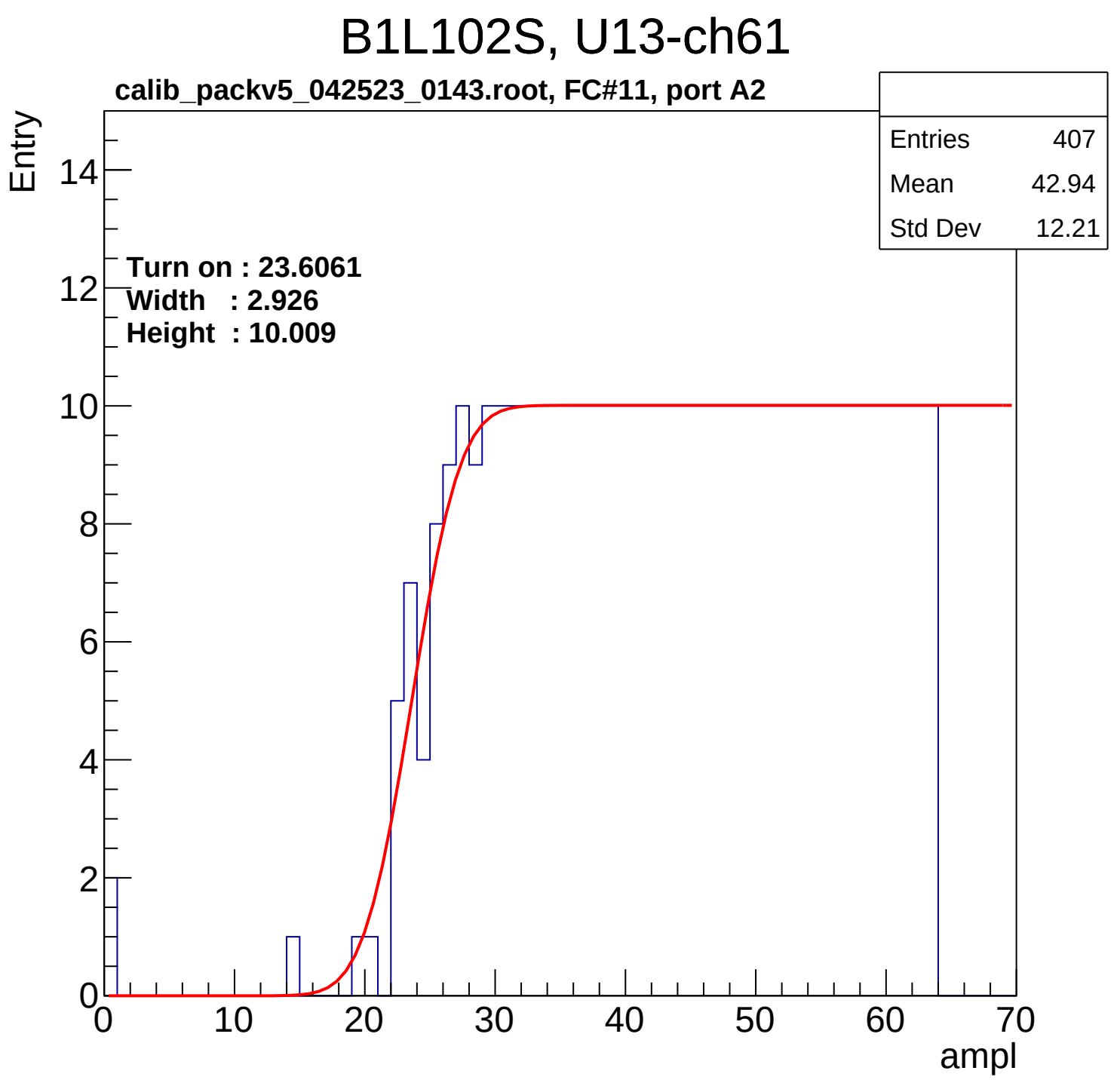
B1L102S, U13-ch61
calib_packv5_042523_0143.root, FC#11, port A2
Entries 407
Mean 42.94
Std Dev 12.21
Turn on : 23.6061
Width : 2.926
Height : 10.009
Entry
ampl
0
2
4
6
8
10
12
14
0
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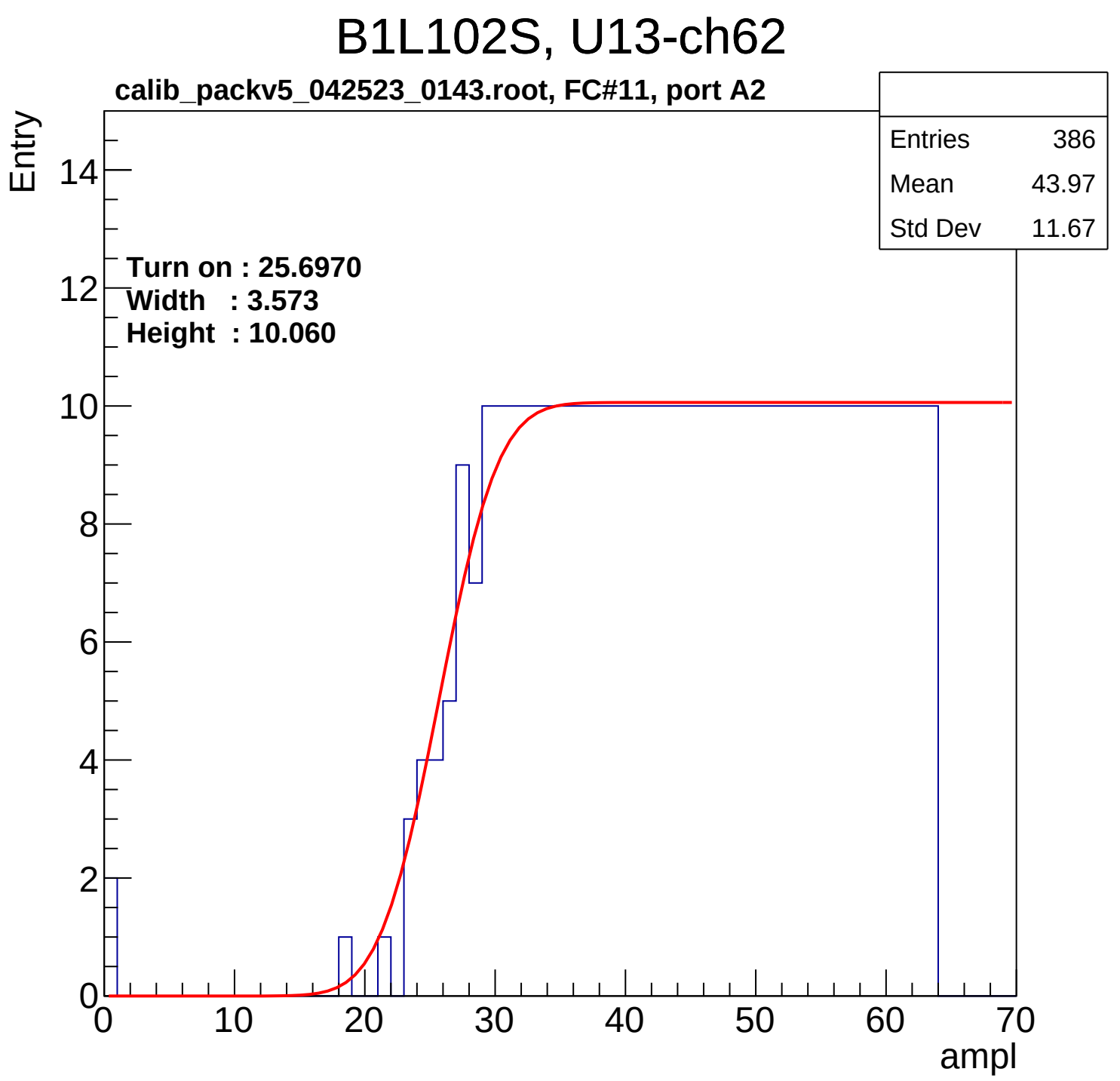
B1L102S, U13-ch62
calib_packv5_042523_0143.root, FC#11, port A2
Entries 386
Mean 43.97
Std Dev 11.67
Turn on : 25.6970
Width : 3.573
Height : 10.060
Entry
ampl
0
2
4
6
8
10
12
14
0
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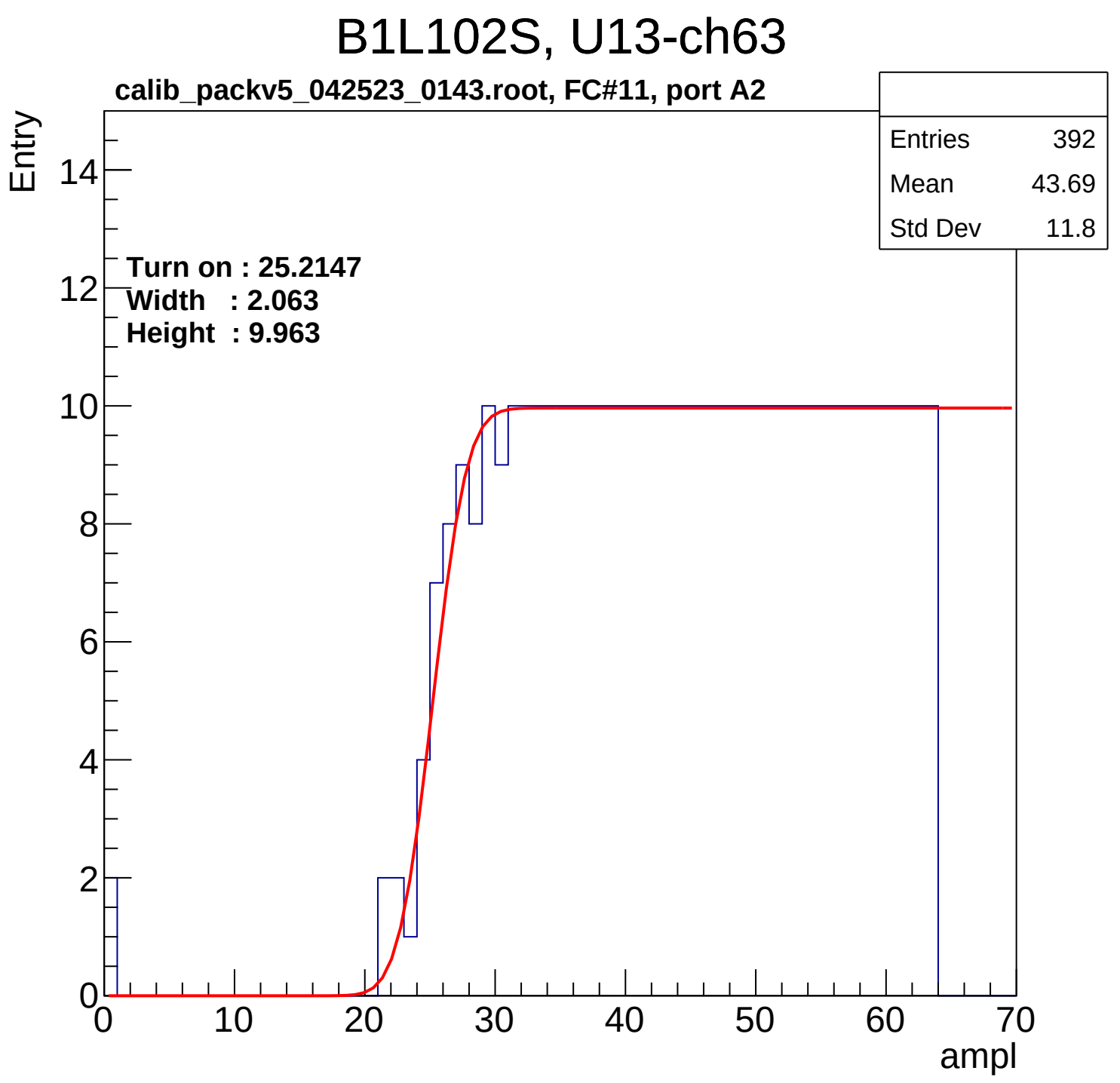
B1L102S, U13-ch63
calib_packv5_042523_0143.root, FC#11, port A2
Entries 392
Mean 43.69
Std Dev 11.8
Turn on : 25.2147
Width : 2.063
Height : 9.963
Entry
ampl
0
2
4
6
8
10
12
14
0
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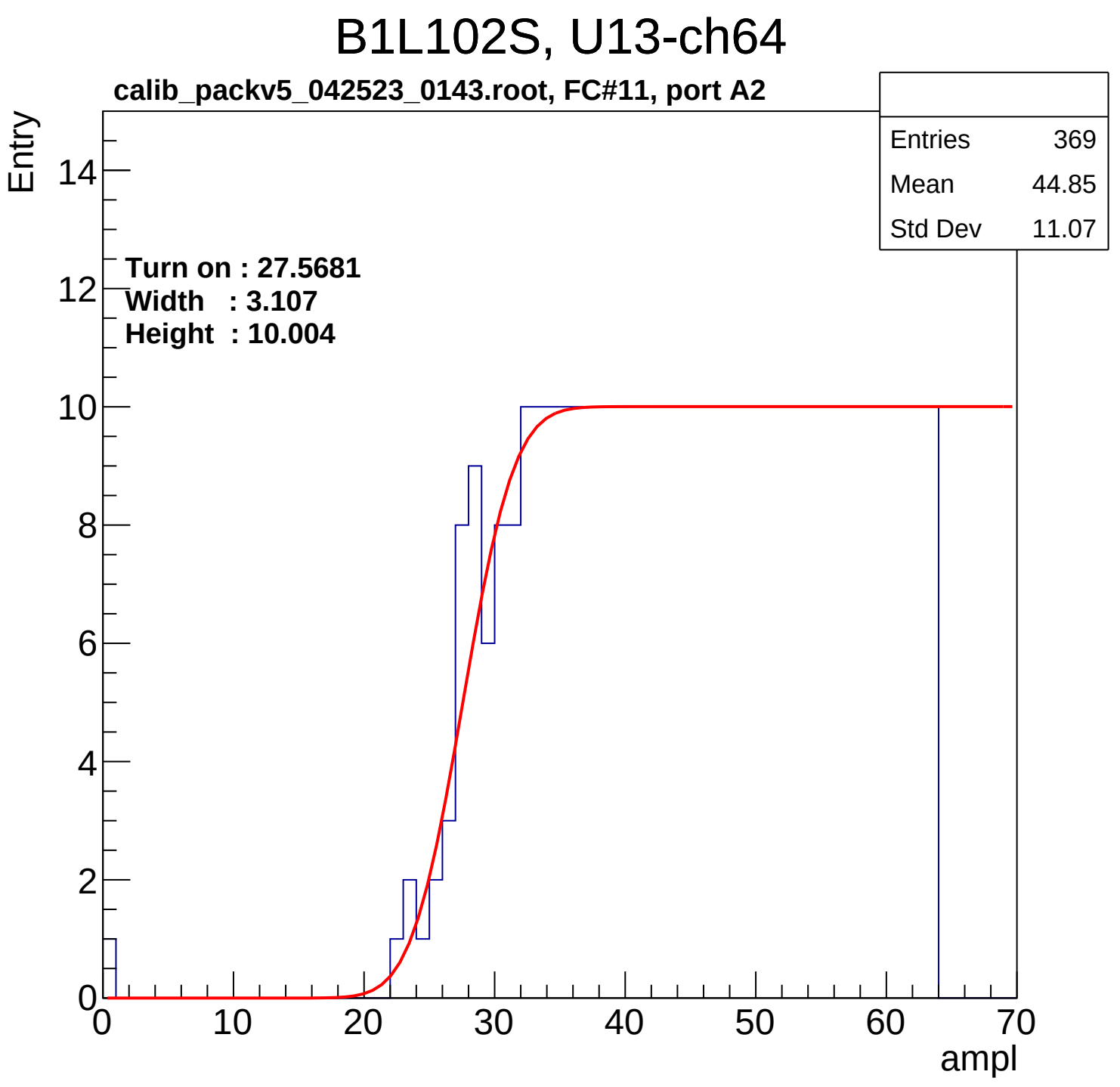
B1L102S, U13-ch64
calib_packv5_042523_0143.root, FC#11, port A2
Entries 369
Mean 44.85
Std Dev 11.07
Turn on : 27.5681
Width : 3.107
Height : 10.004
Entry
ampl
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2
4
6
8
10
12
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0
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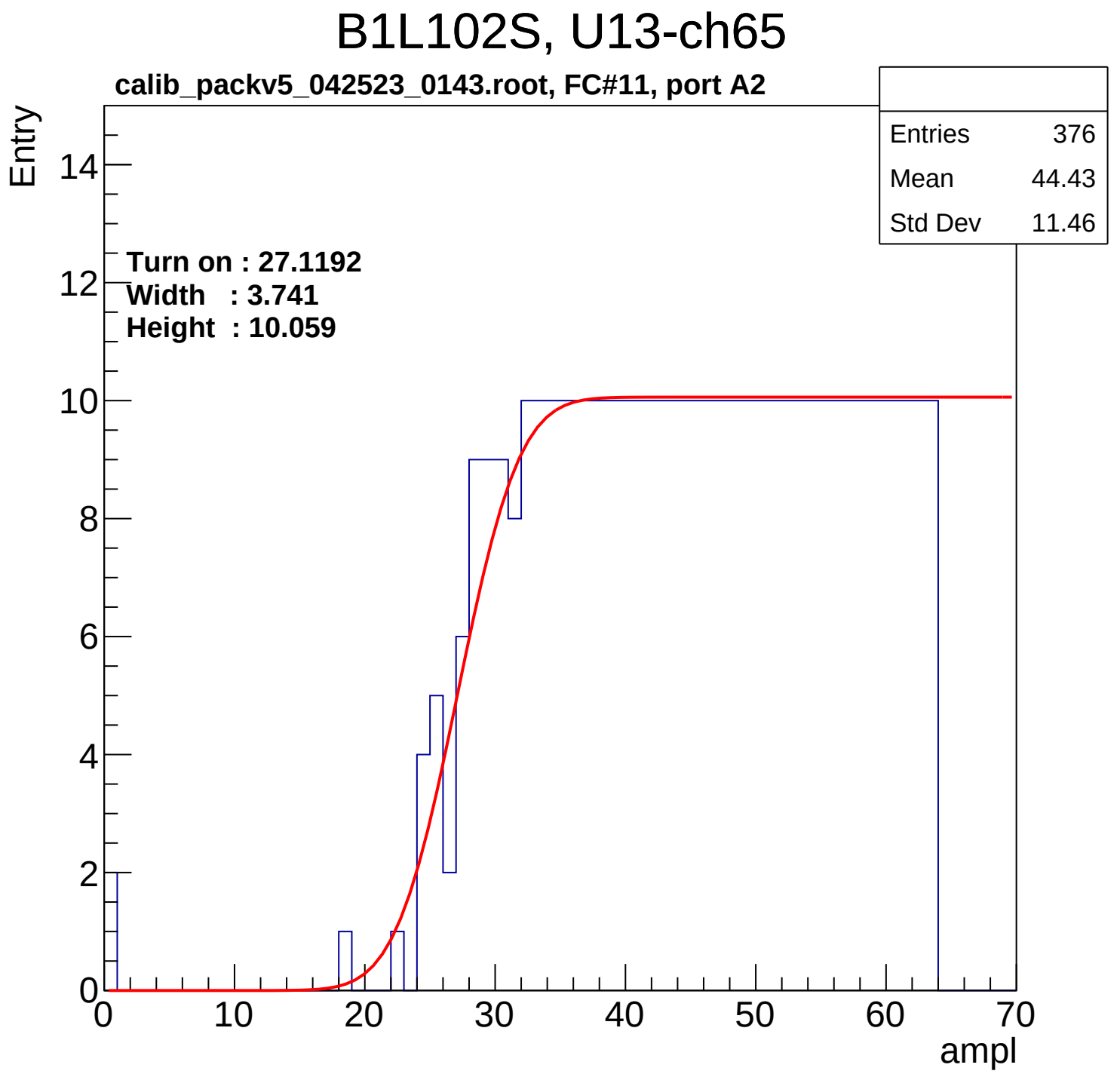
B1L102S, U13-ch65
calib_packv5_042523_0143.root, FC#11, port A2
Entries 376
Mean 44.43
Std Dev 11.46
Turn on : 27.1192
Width : 3.741
Height : 10.059
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
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60
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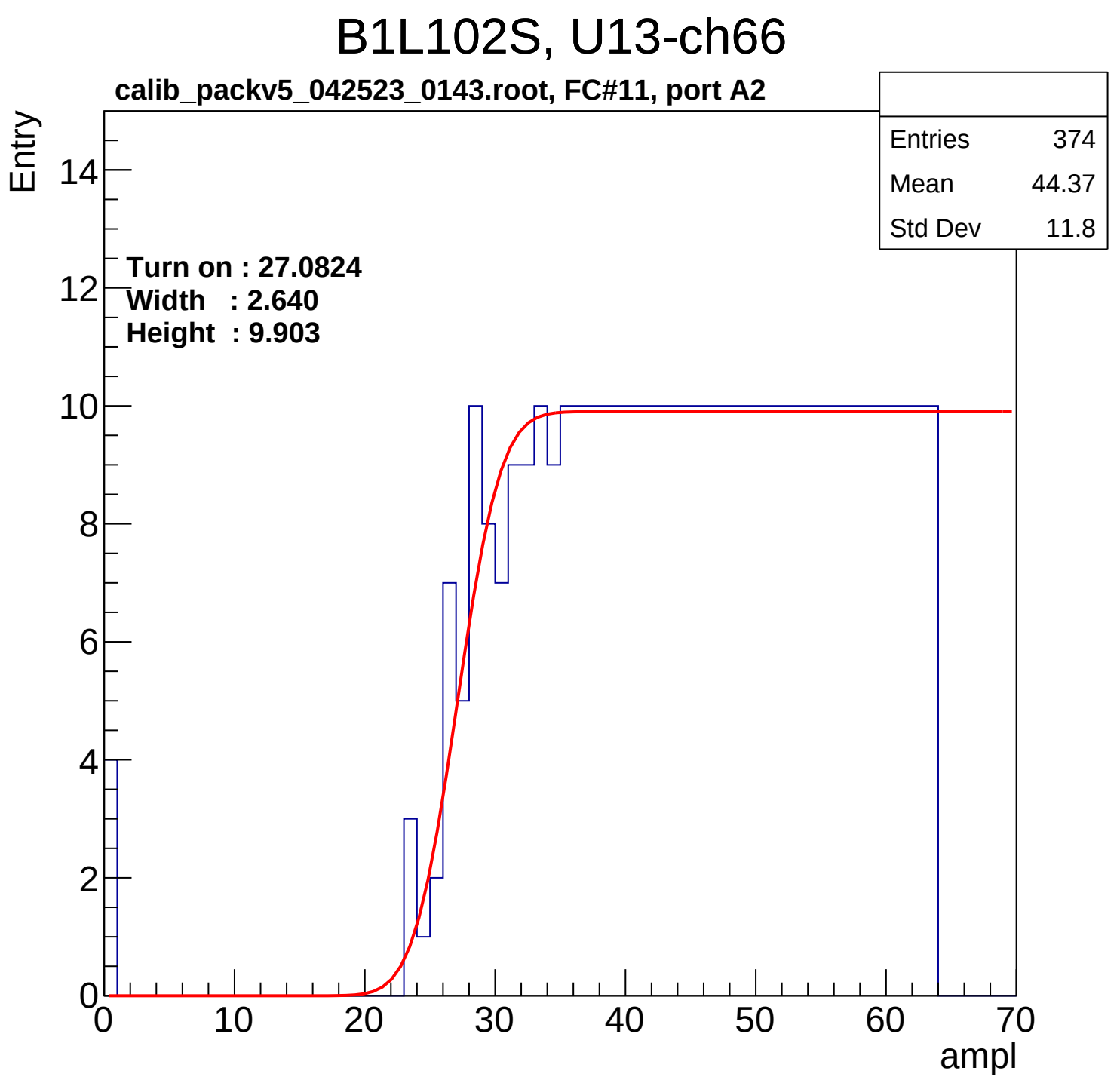
B1L102S, U13-ch66
calib_packv5_042523_0143.root, FC#11, port A2
Entries 374
Mean 44.37
Std Dev 11.8
Turn on : 27.0824
Width : 2.640
Height : 9.903
Entry
ampl
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4
6
8
10
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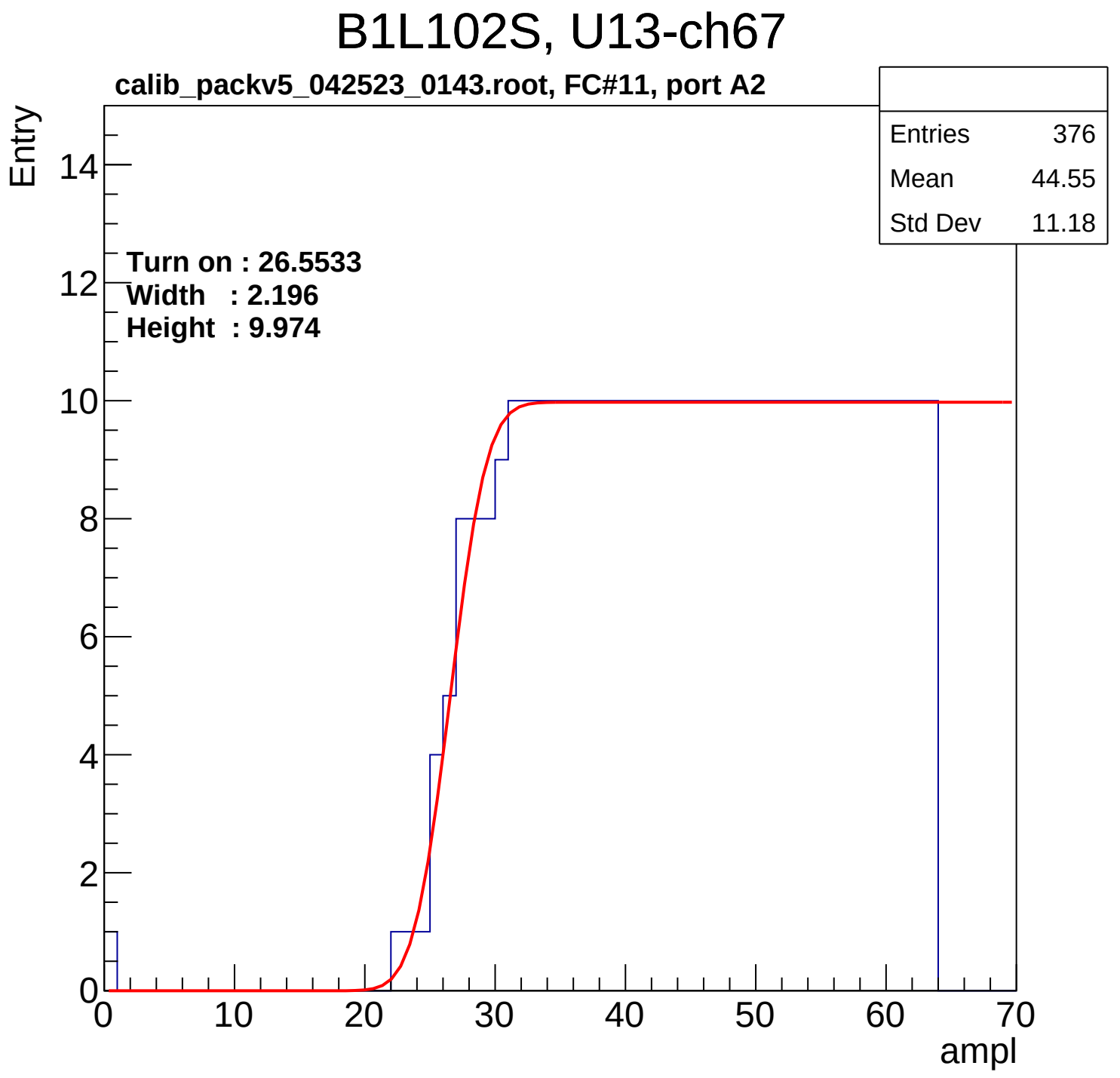
B1L102S, U13-ch67
calib_packv5_042523_0143.root, FC#11, port A2
Entries 376
Mean 44.55
Std Dev 11.18
Turn on : 26.5533
Width : 2.196
Height : 9.974
Entry
ampl
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2
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6
8
10
12
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0
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60
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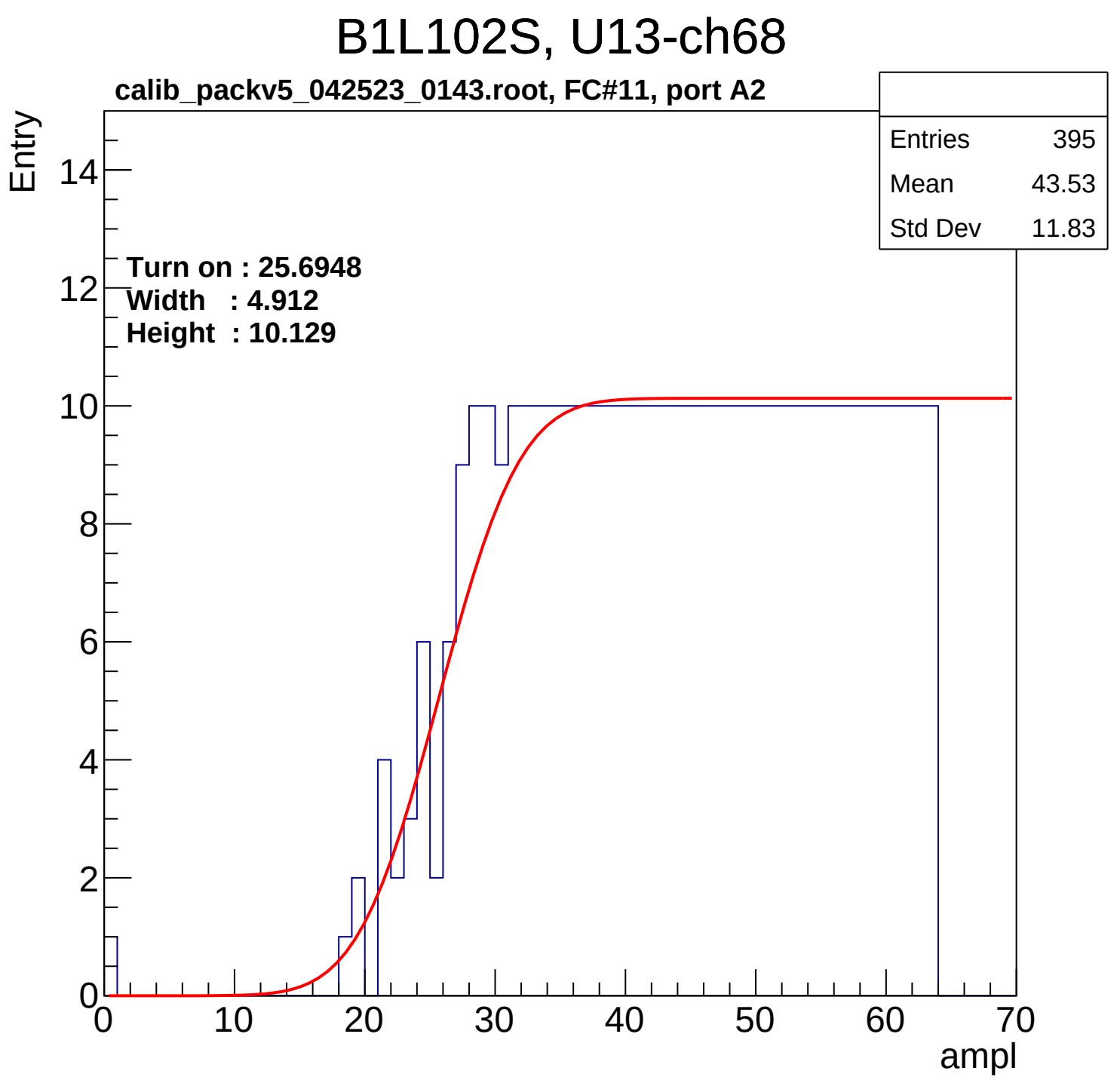
B1L102S, U13-ch68
calib_packv5_042523_0143.root, FC#11, port A2
Entries 395
Mean 43.53
Std Dev 11.83
Turn on : 25.6948
Width : 4.912
Height : 10.129
Entry
ampl
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6
8
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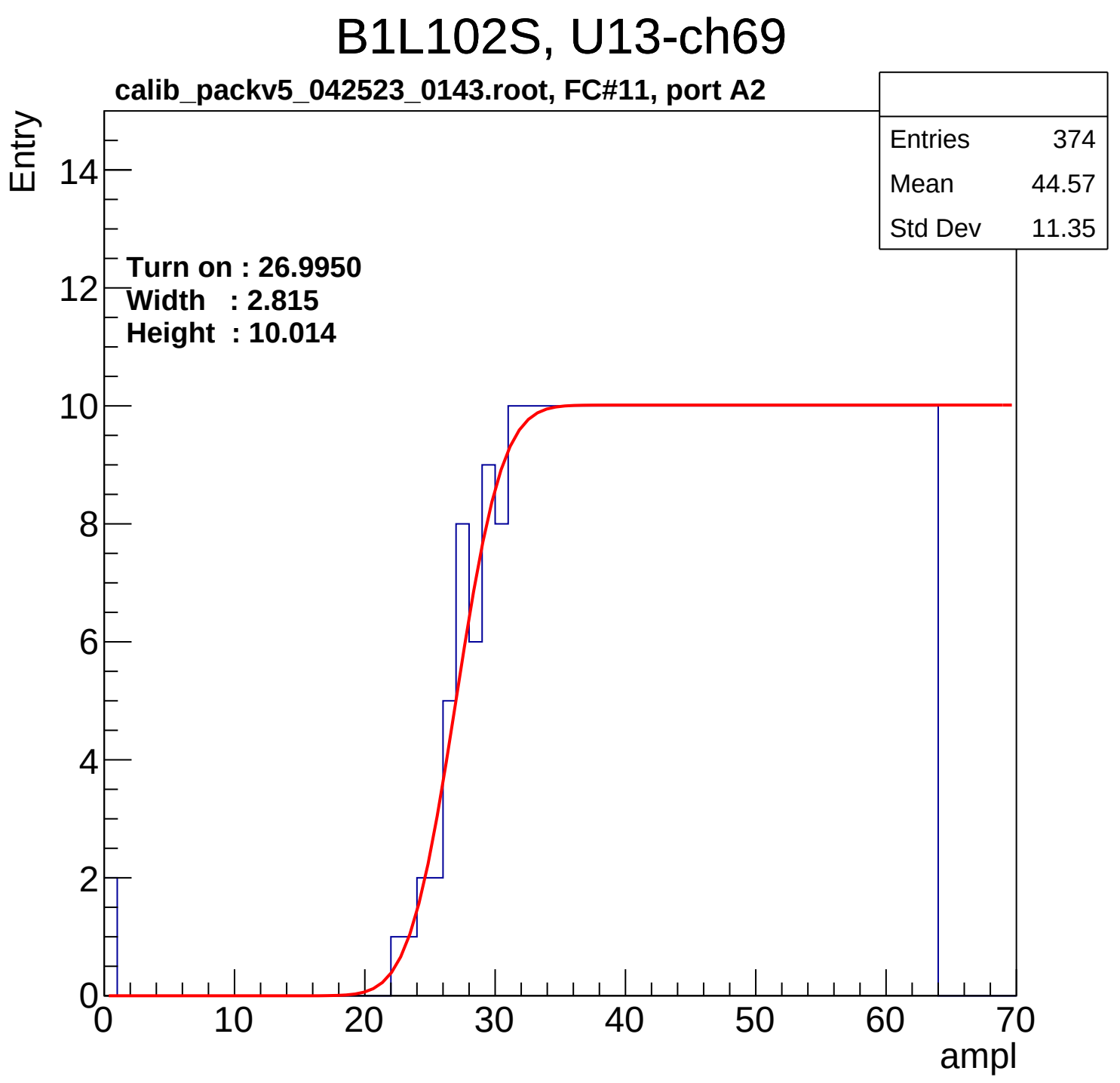
B1L102S, U13-ch69
calib_packv5_042523_0143.root, FC#11, port A2
Entries 374
Mean 44.57
Std Dev 11.35
Turn on : 26.9950
Width : 2.815
Height : 10.014
Entry
ampl
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6
8
10
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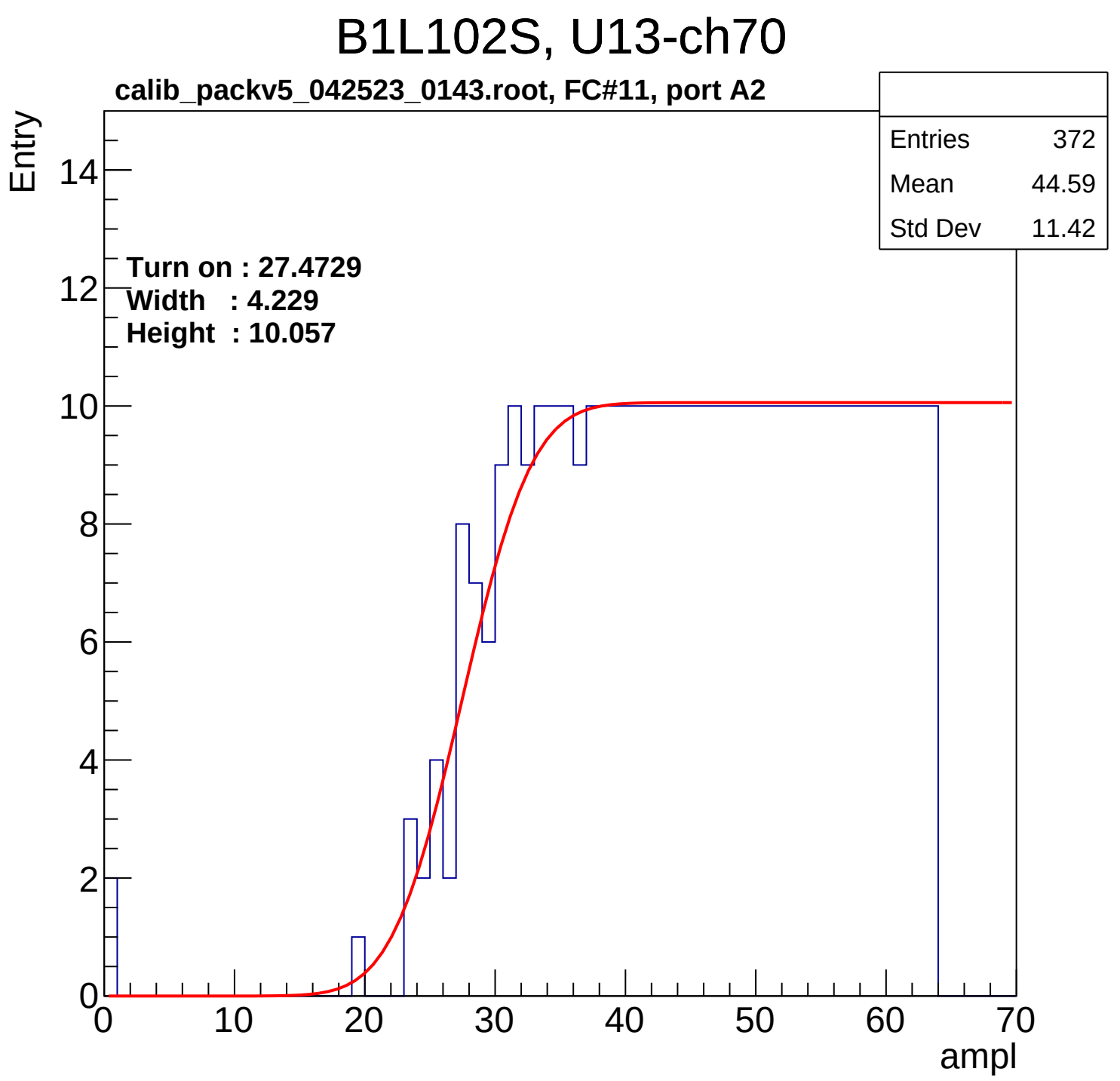
B1L102S, U13-ch70
calib_packv5_042523_0143.root, FC#11, port A2
Entries 372
Mean 44.59
Std Dev 11.42
Turn on : 27.4729
Width : 4.229
Height : 10.057
Entry
ampl
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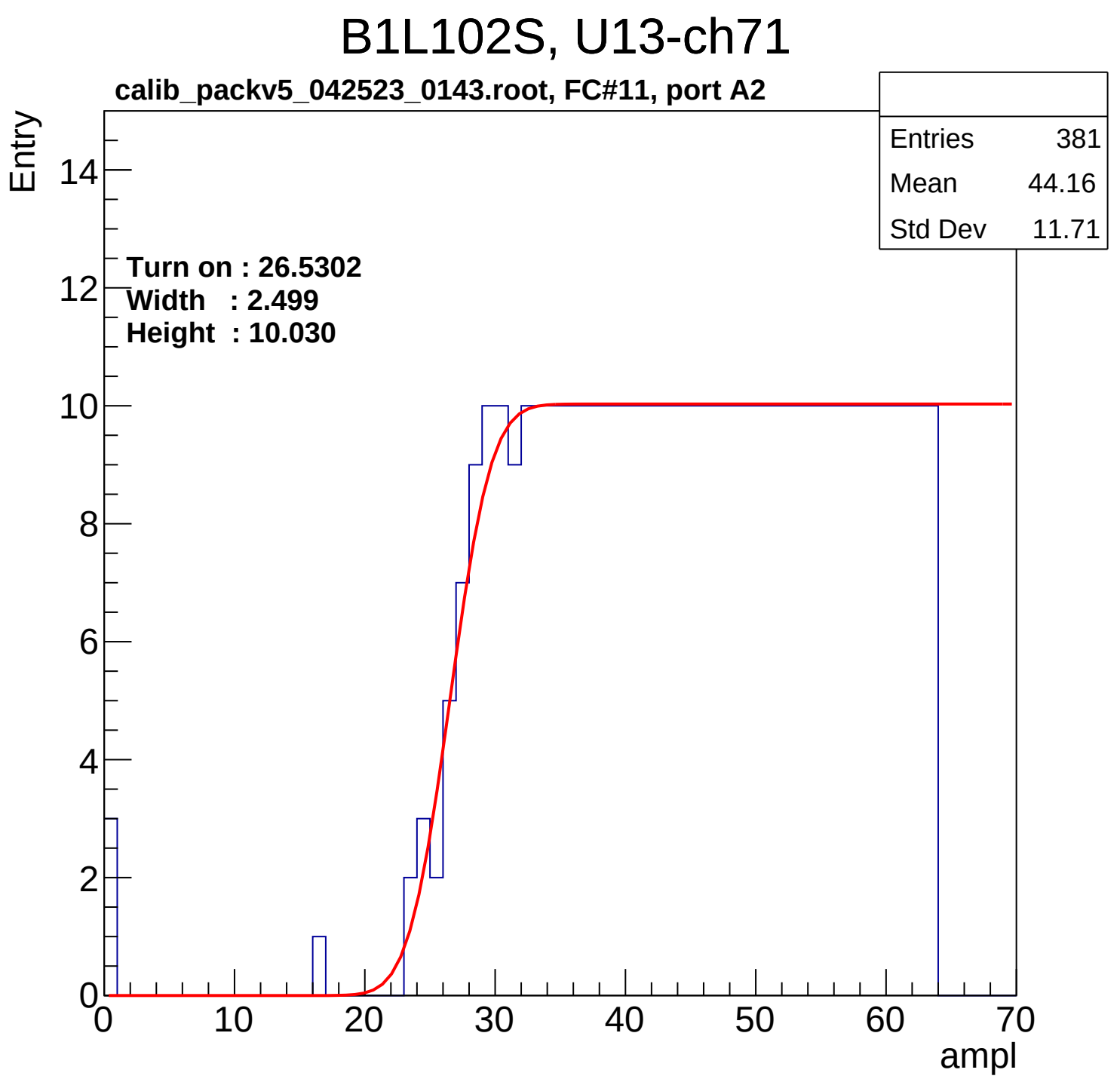
B1L102S, U13-ch71
calib_packv5_042523_0143.root, FC#11, port A2
Entries 381
Mean 44.16
Std Dev 11.71
Turn on : 26.5302
Width : 2.499
Height : 10.030
Entry
ampl
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6
8
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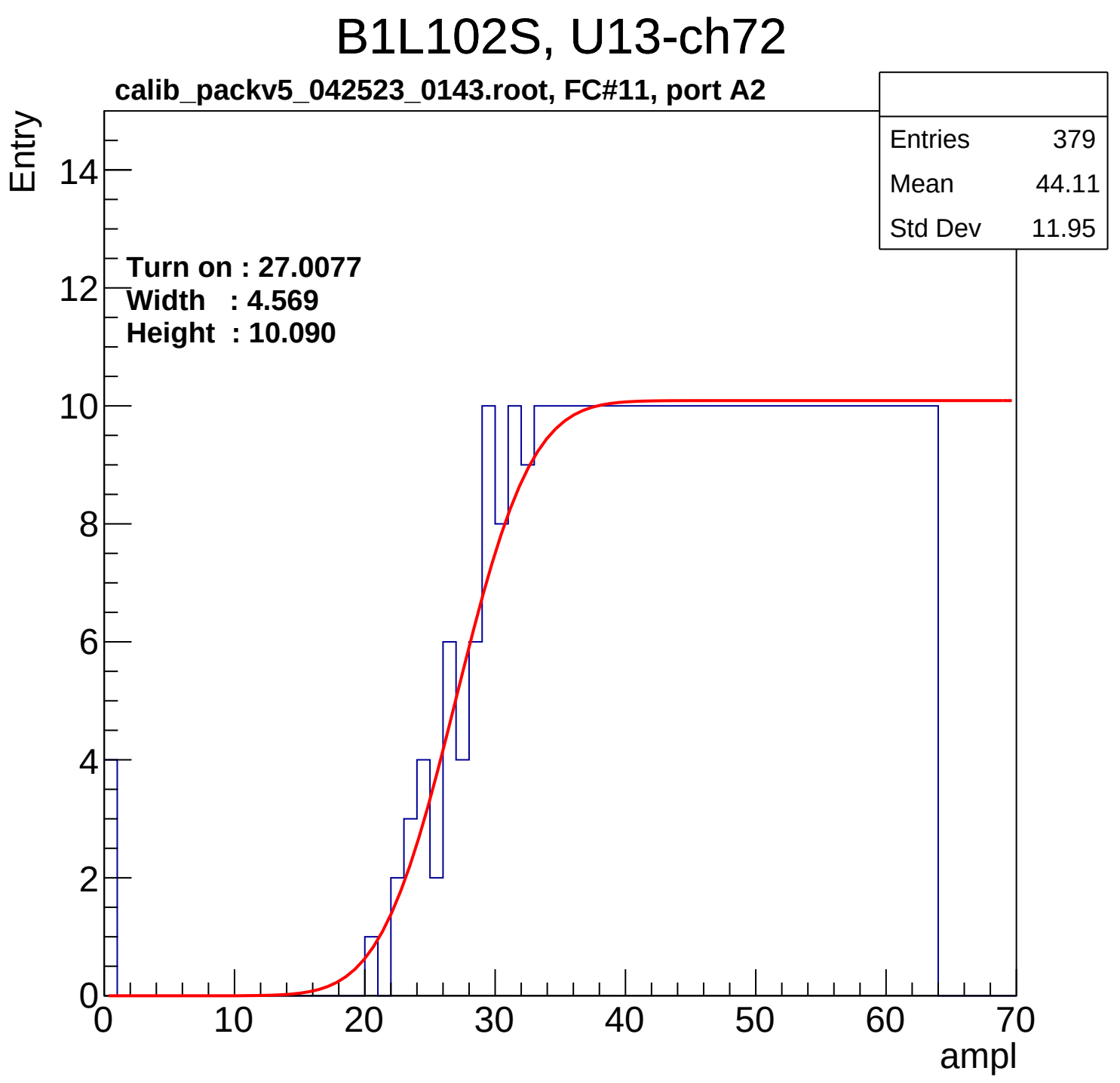
B1L102S, U13-ch72
calib_packv5_042523_0143.root, FC#11, port A2
Entries 379
Mean 44.11
Std Dev 11.95
Turn on : 27.0077
Width : 4.569
Height : 10.090
Entry
ampl
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6
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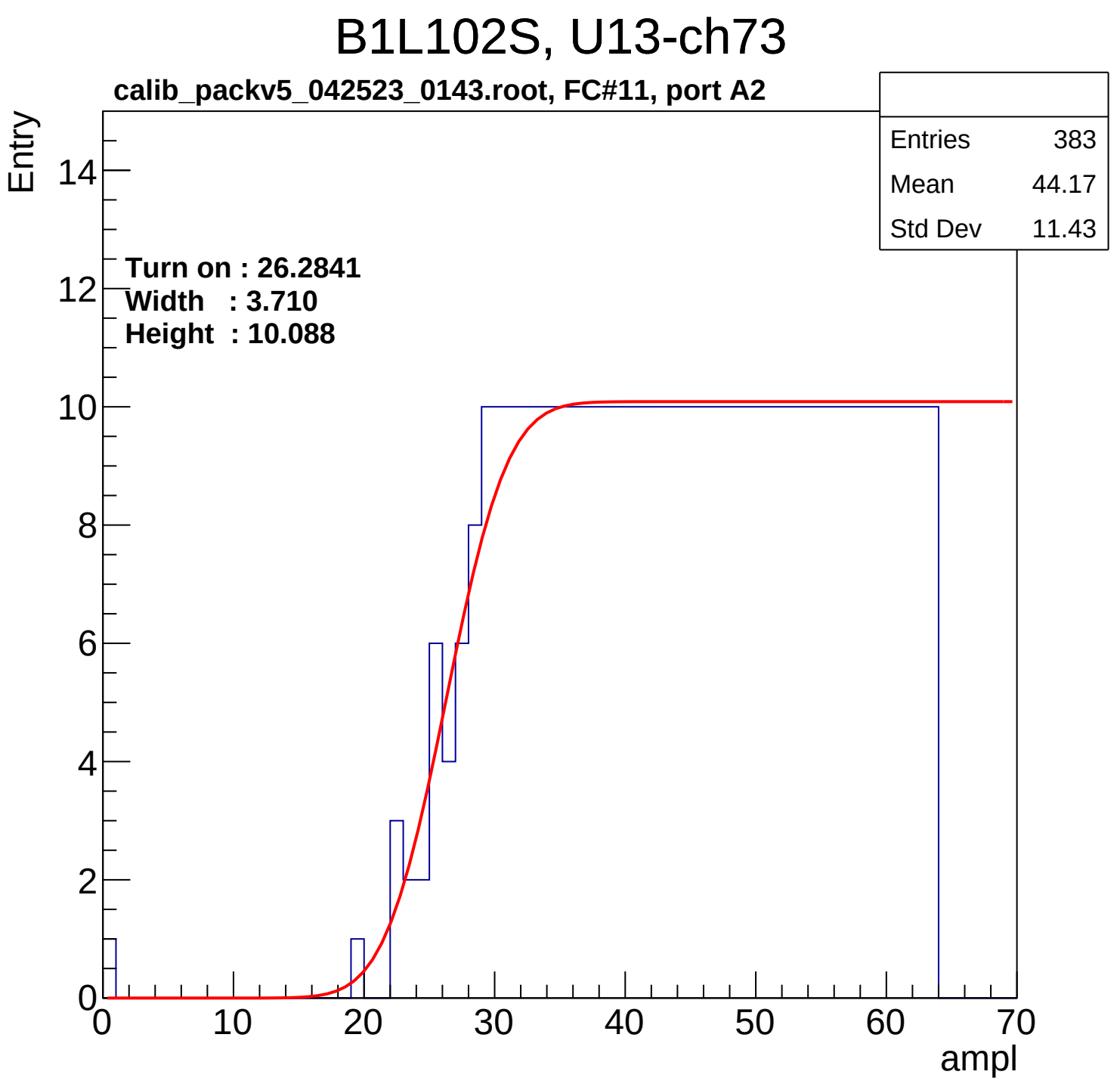
B1L102S, U13-ch73
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 44.17
Std Dev 11.43
Turn on : 26.2841
Width : 3.710
Height : 10.088
Entry
ampl
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6
8
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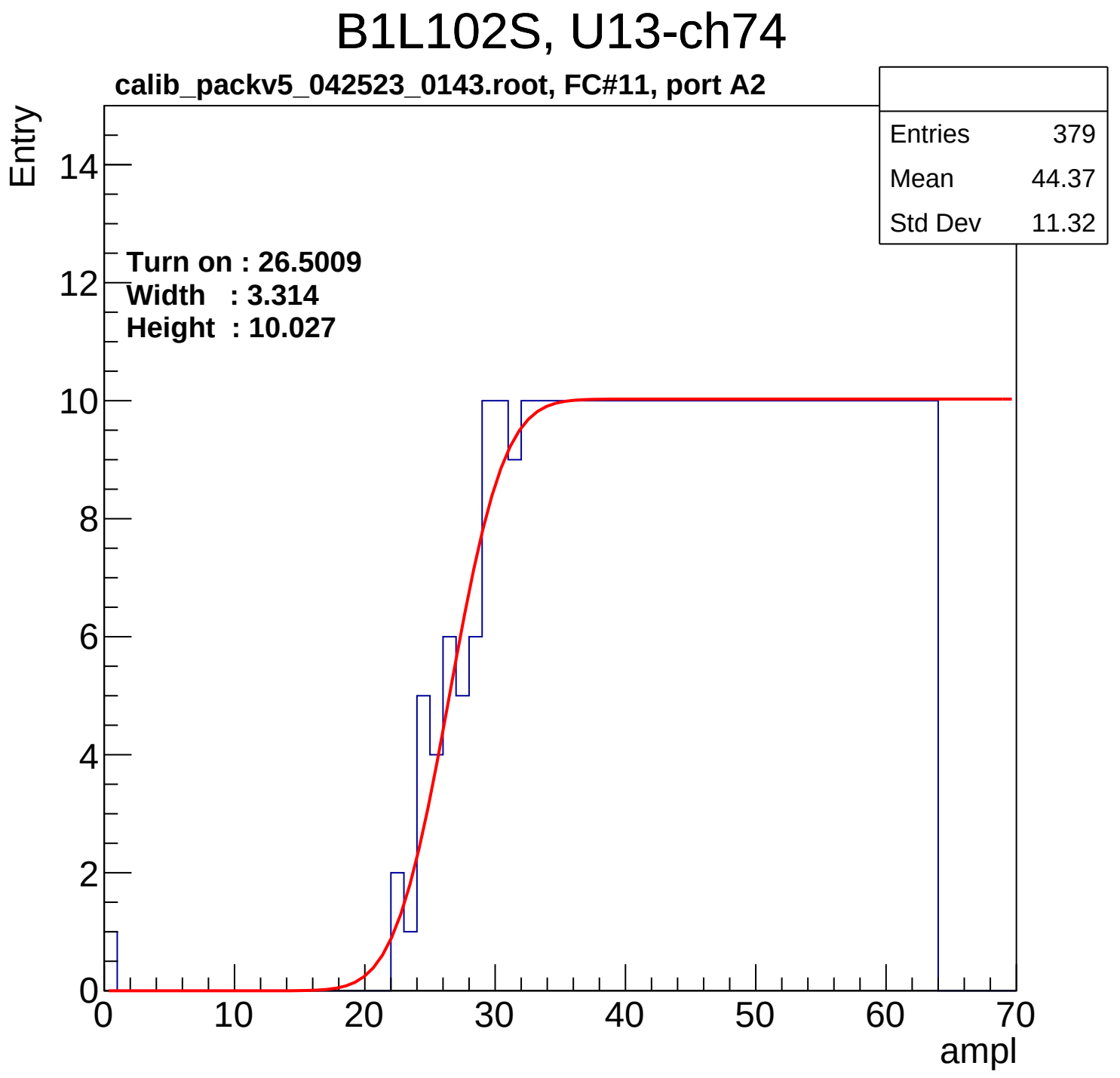
B1L102S, U13-ch74
calib_packv5_042523_0143.root, FC#11, port A2
Entries 379
Mean 44.37
Std Dev 11.32
Turn on : 26.5009
Width : 3.314
Height : 10.027
Entry
ampl
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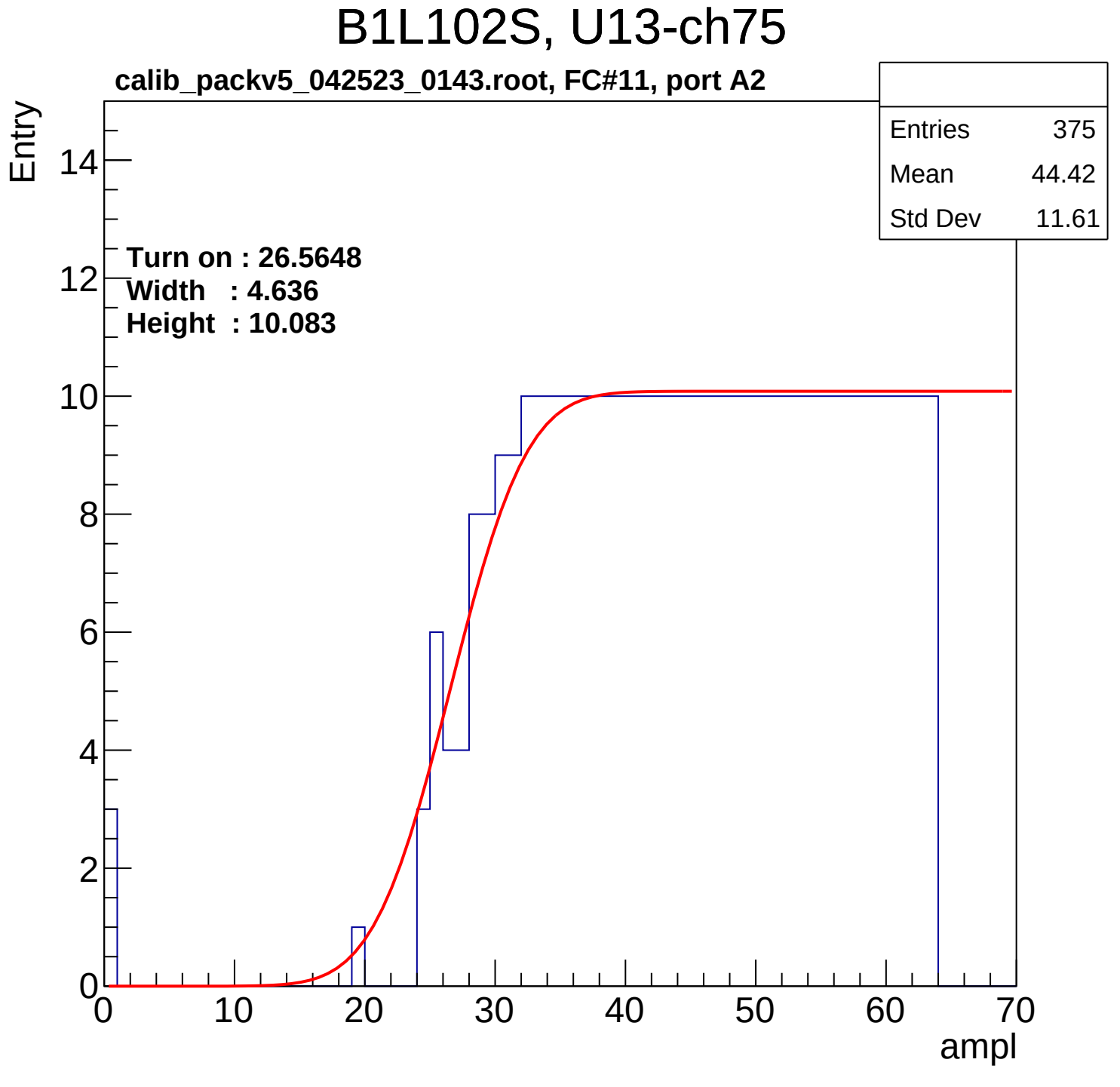
B1L102S, U13-ch75
calib_packv5_042523_0143.root, FC#11, port A2
Entries 375
Mean 44.42
Std Dev 11.61
Turn on : 26.5648
Width : 4.636
Height : 10.083
Entry
ampl
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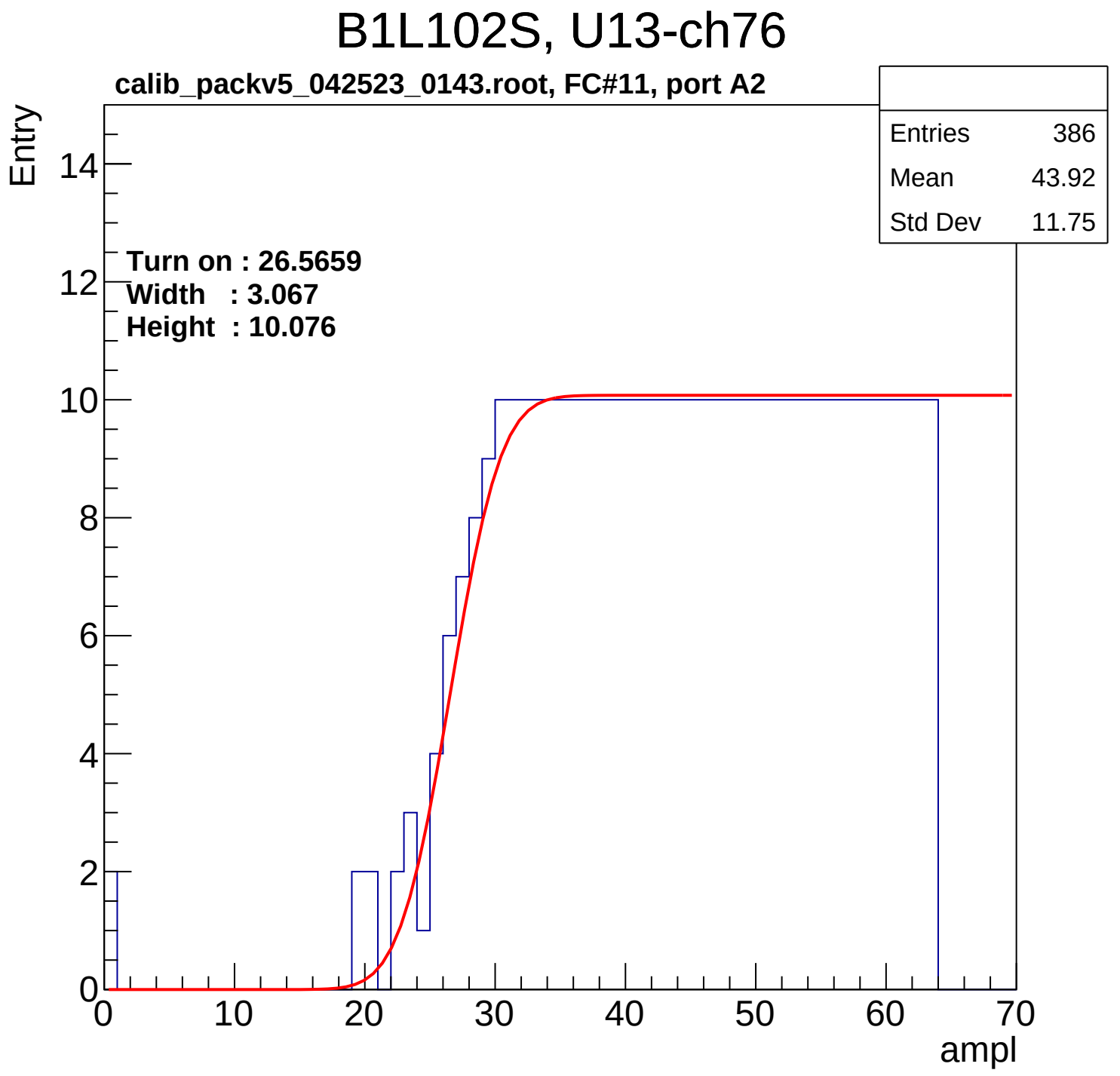
B1L102S, U13-ch76
calib_packv5_042523_0143.root, FC#11, port A2
Entries 386
Mean 43.92
Std Dev 11.75
Turn on : 26.5659
Width : 3.067
Height : 10.076
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ampl
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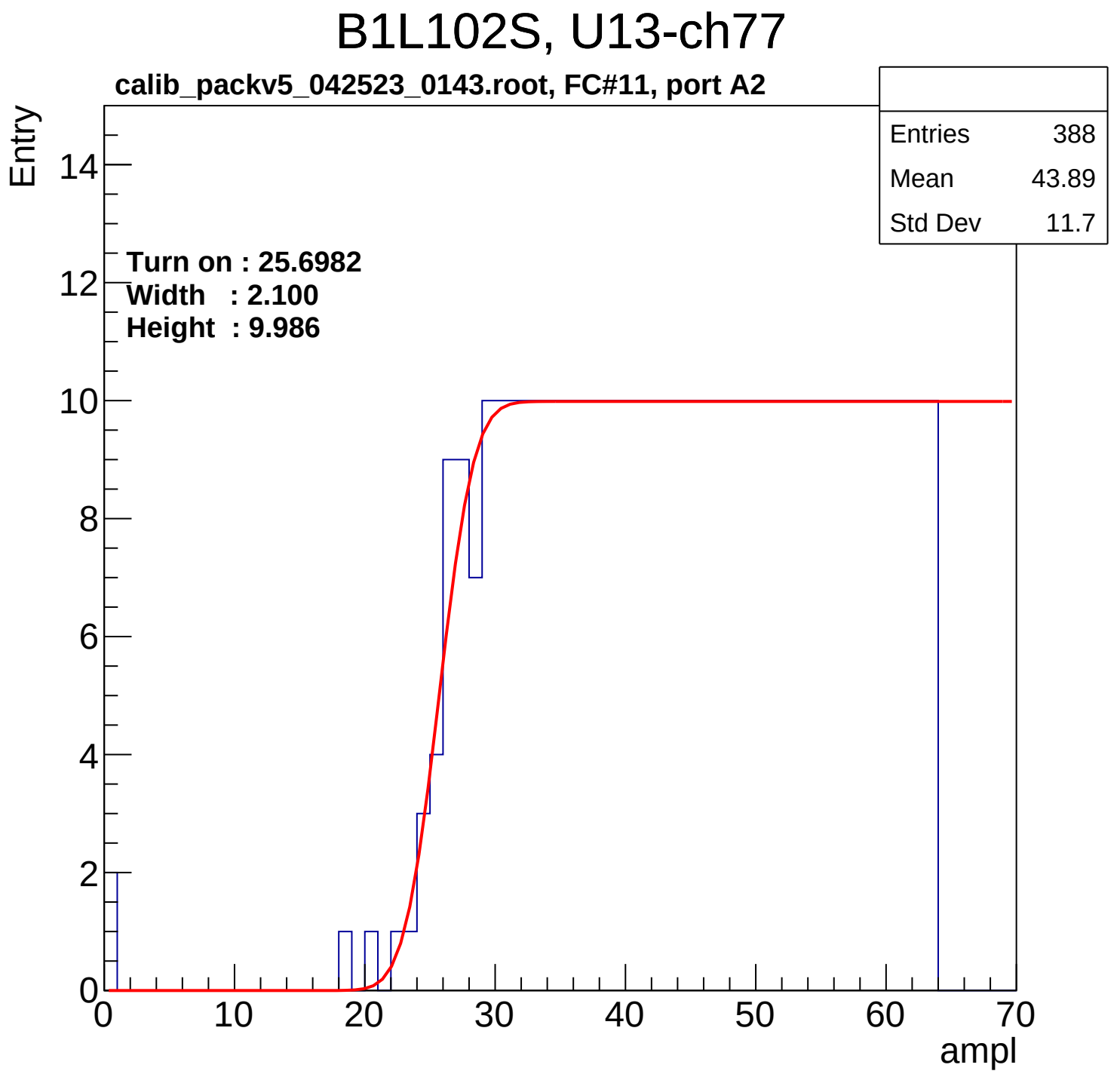
B1L102S, U13-ch77
calib_packv5_042523_0143.root, FC#11, port A2
Entries 388
Mean 43.89
Std Dev 11.7
Turn on : 25.6982
Width : 2.100
Height : 9.986
Entry
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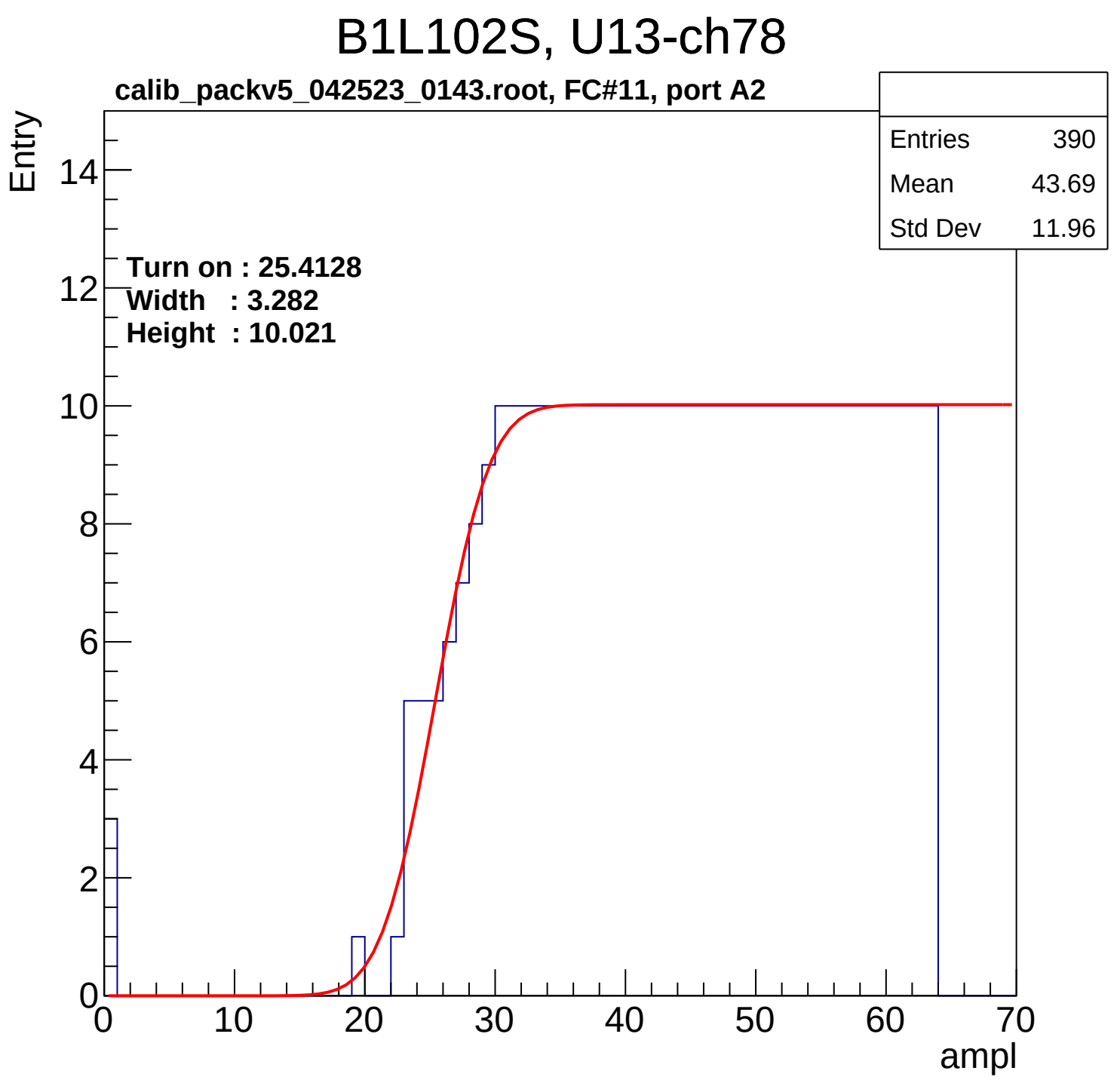
B1L102S, U13-ch78
calib_packv5_042523_0143.root, FC#11, port A2
Entries 390
Mean 43.69
Std Dev 11.96
Turn on : 25.4128
Width : 3.282
Height : 10.021
Entry
ampl
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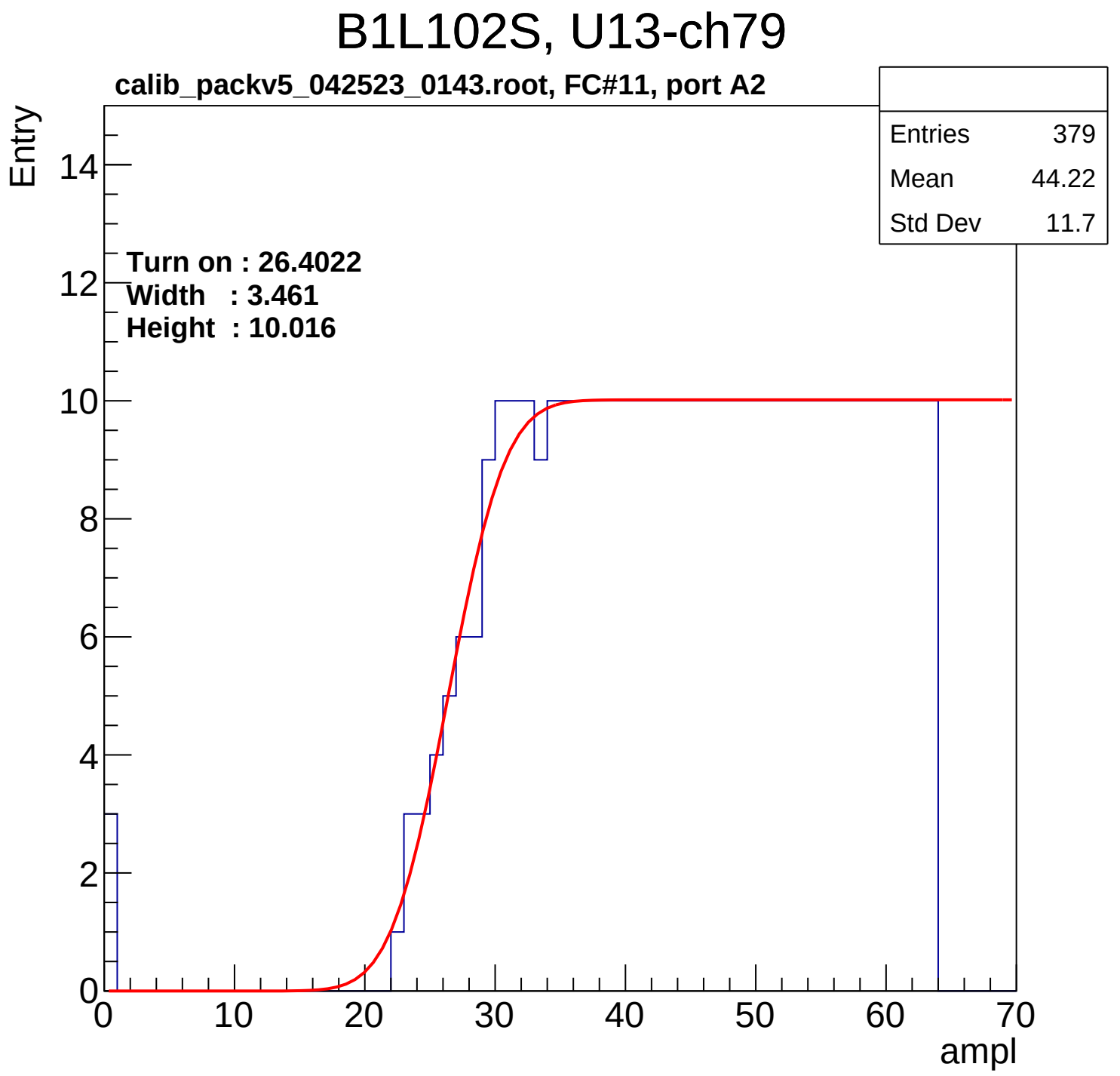
B1L102S, U13-ch79
calib_packv5_042523_0143.root, FC#11, port A2
Entries 379
Mean 44.22
Std Dev 11.7
Turn on : 26.4022
Width : 3.461
Height : 10.016
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ampl
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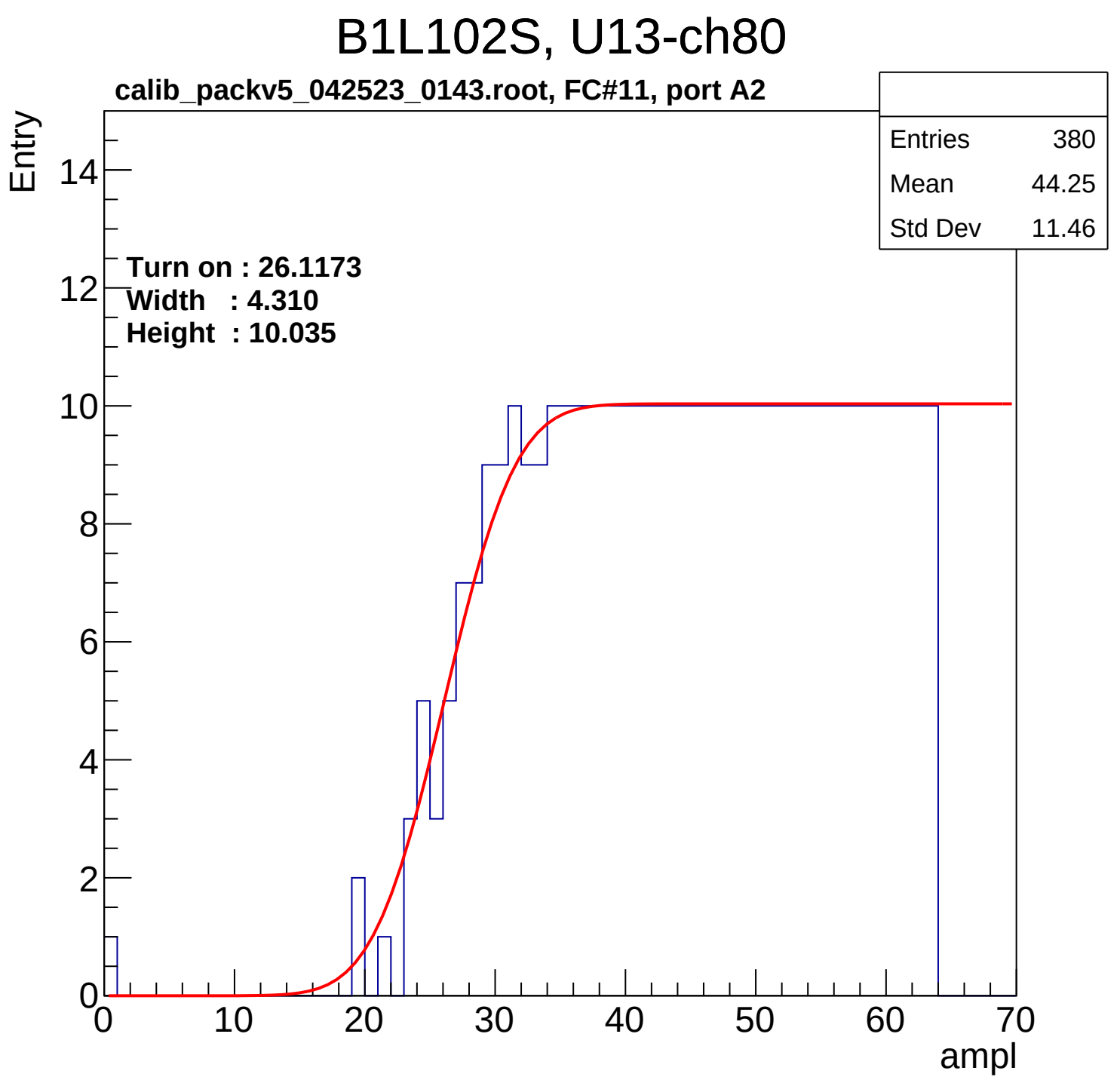
B1L102S, U13-ch80
calib_packv5_042523_0143.root, FC#11, port A2
Entries 380
Mean 44.25
Std Dev 11.46
Turn on : 26.1173
Width : 4.310
Height : 10.035
Entry
ampl
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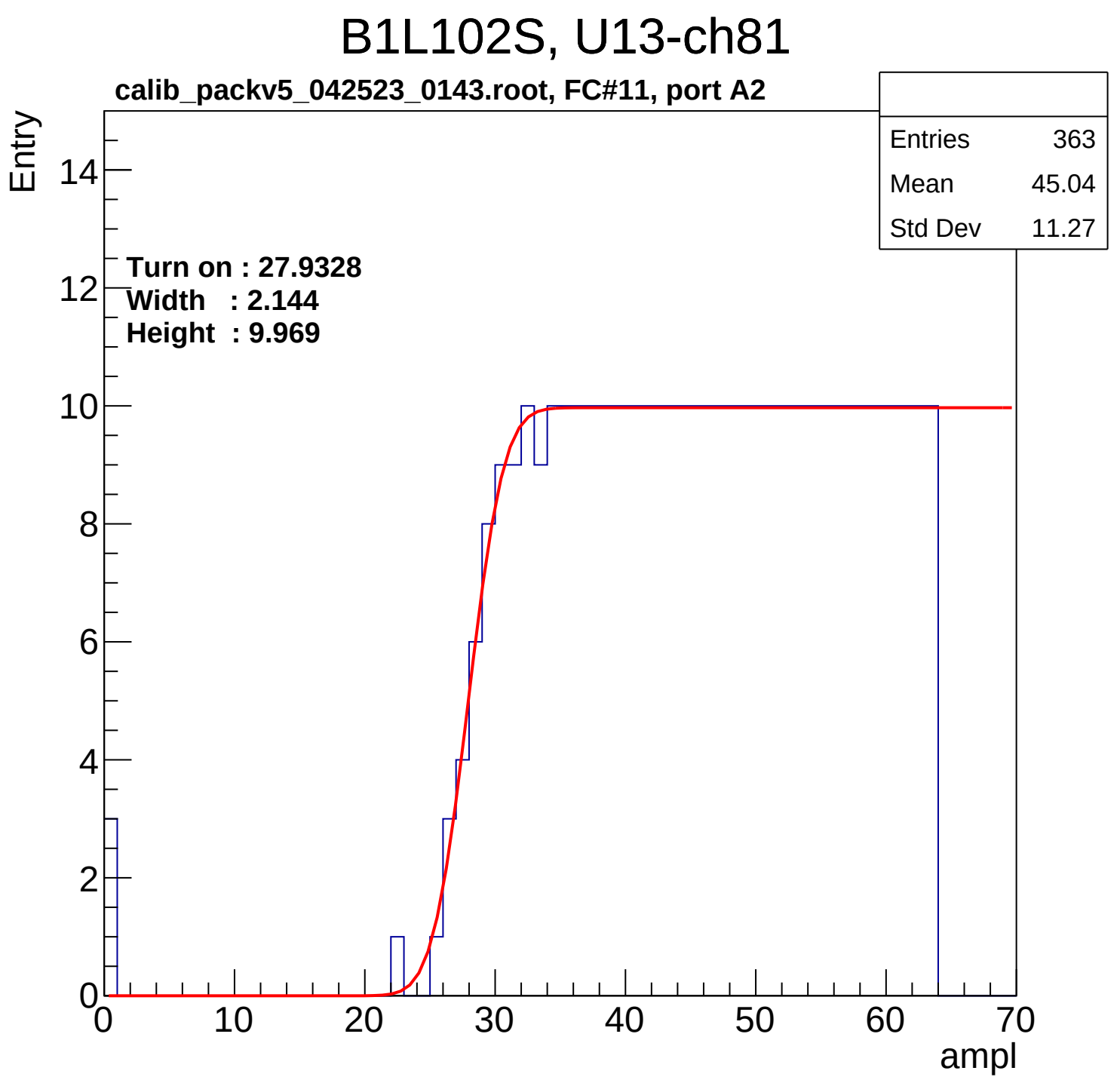
B1L102S, U13-ch81
calib_packv5_042523_0143.root, FC#11, port A2
Entries 363
Mean 45.04
Std Dev 11.27
Turn on : 27.9328
Width : 2.144
Height : 9.969
Entry
ampl
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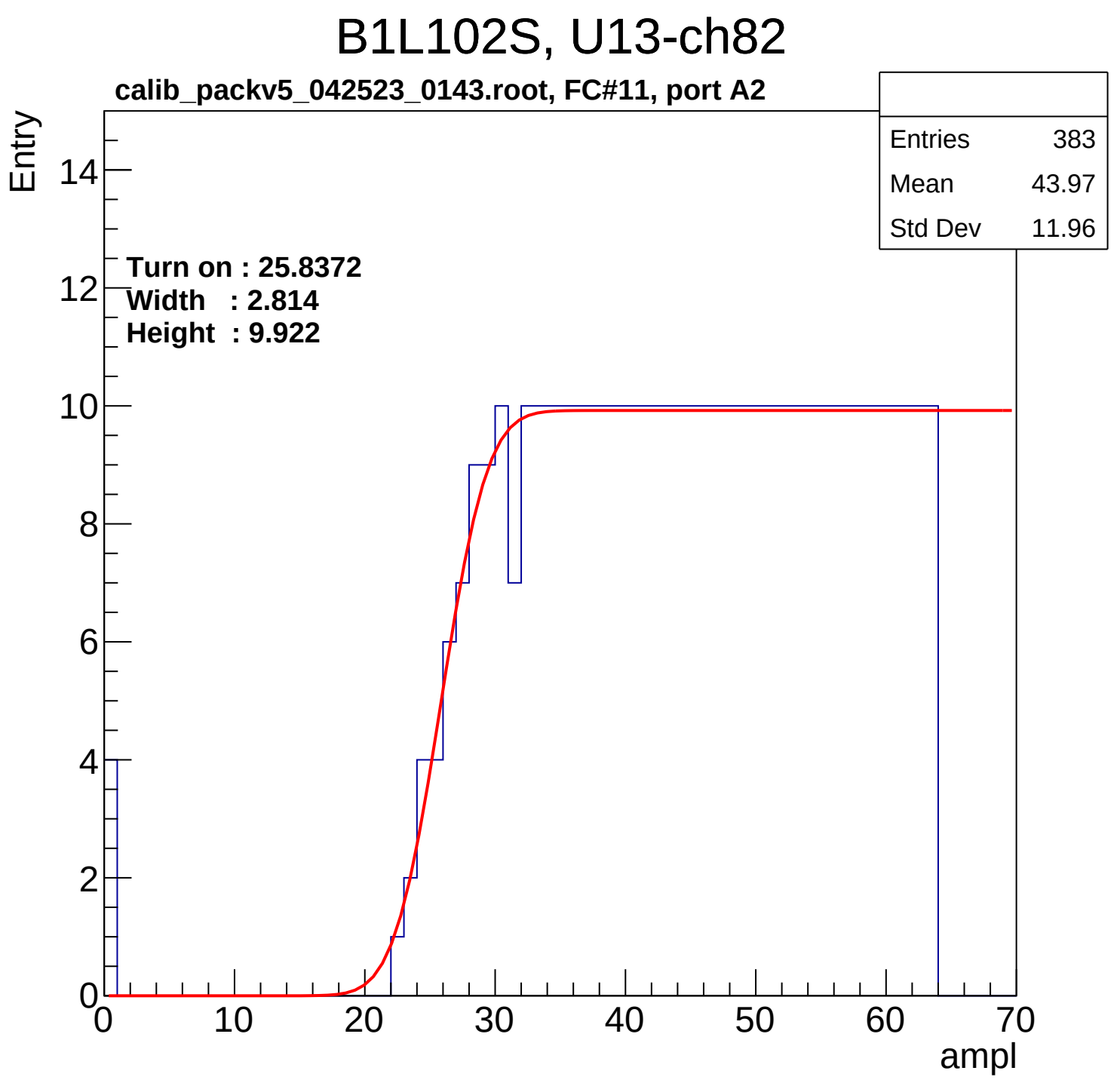
B1L102S, U13-ch82
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 43.97
Std Dev 11.96
Turn on : 25.8372
Width : 2.814
Height : 9.922
Entry
ampl
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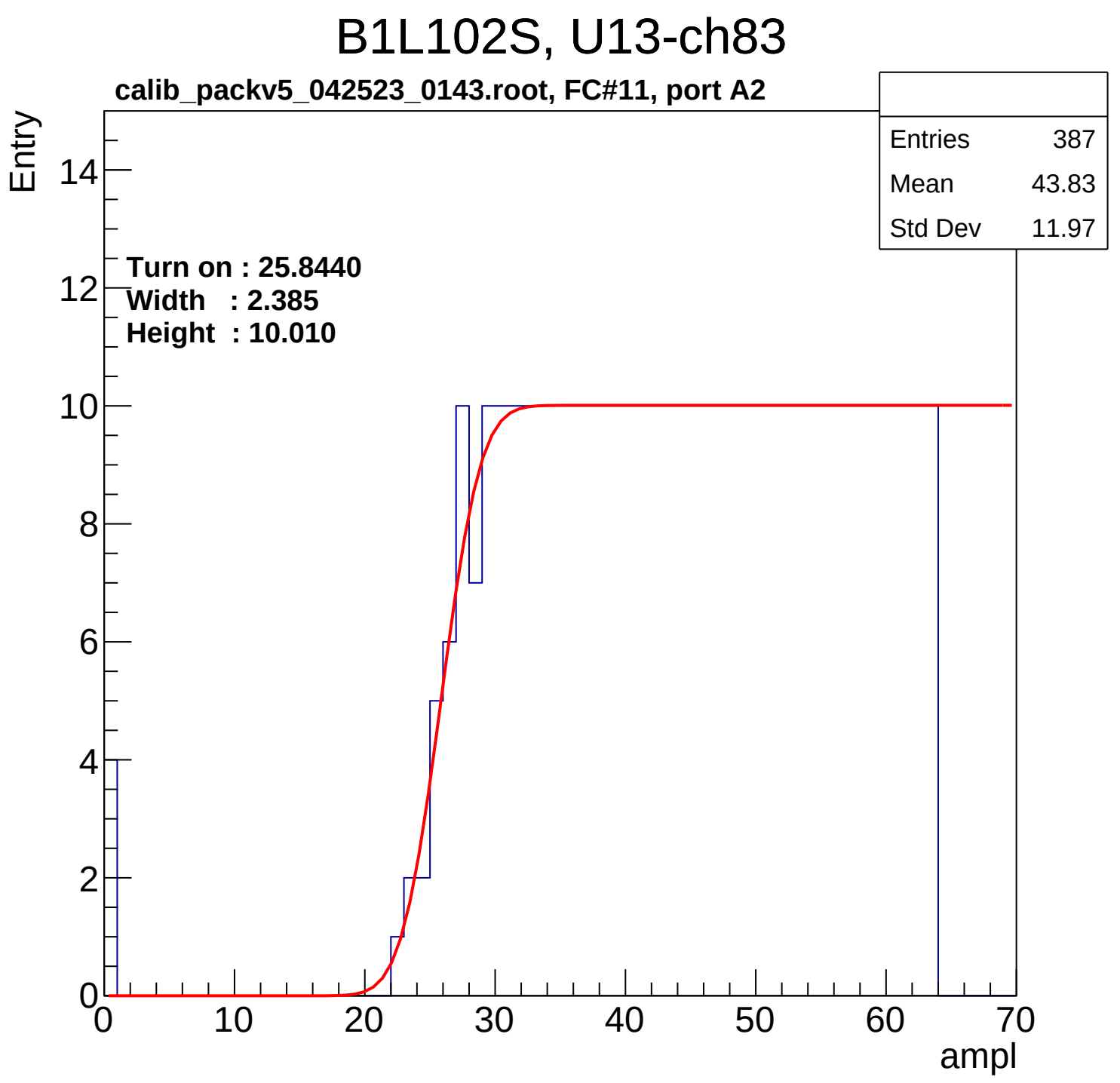
B1L102S, U13-ch83
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 43.83
Std Dev 11.97
Turn on : 25.8440
Width : 2.385
Height : 10.010
Entry
ampl
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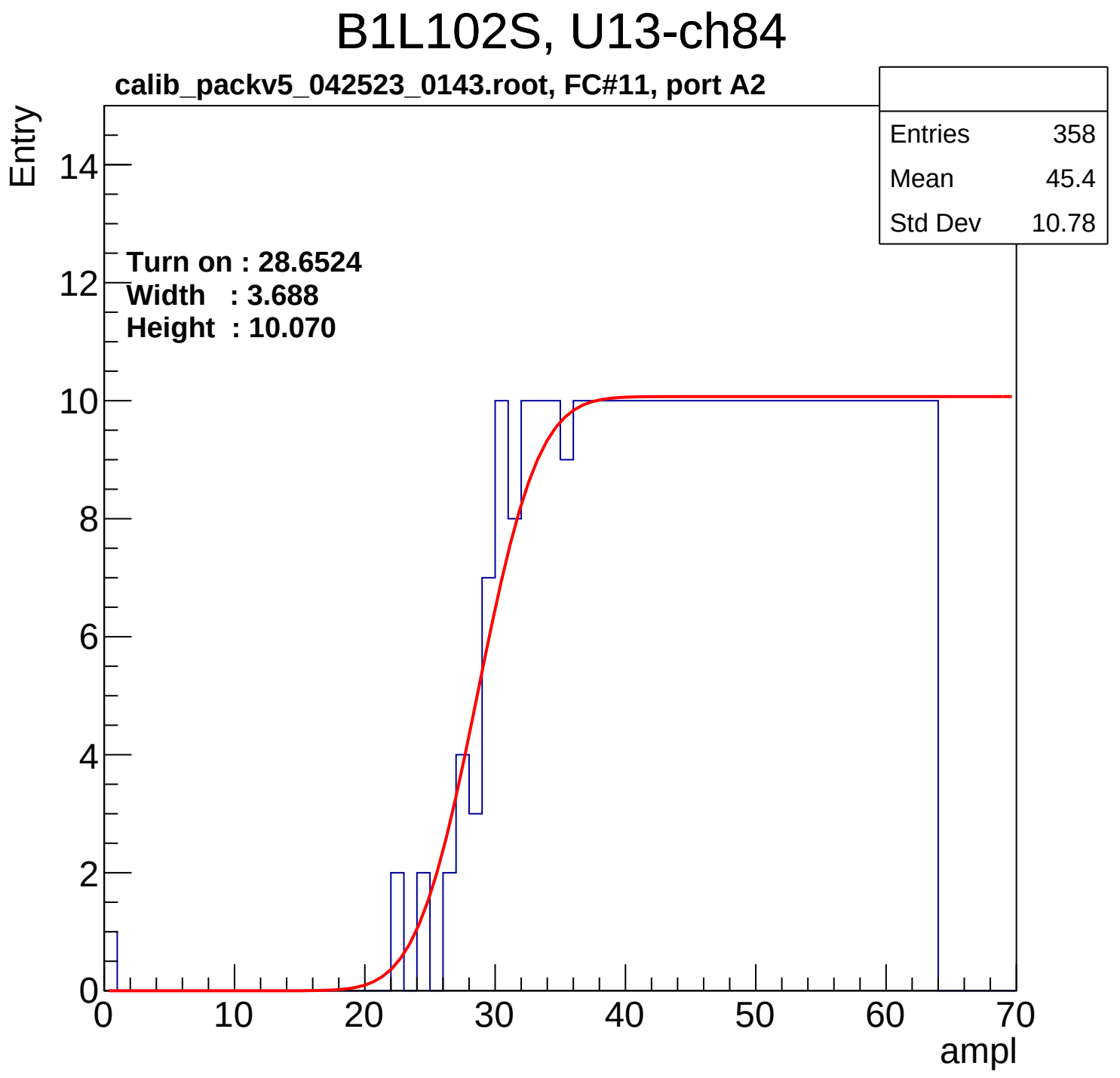
B1L102S, U13-ch84
calib_packv5_042523_0143.root, FC#11, port A2
Entries 358
Mean 45.4
Std Dev 10.78
Turn on : 28.6524
Width : 3.688
Height : 10.070
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ampl
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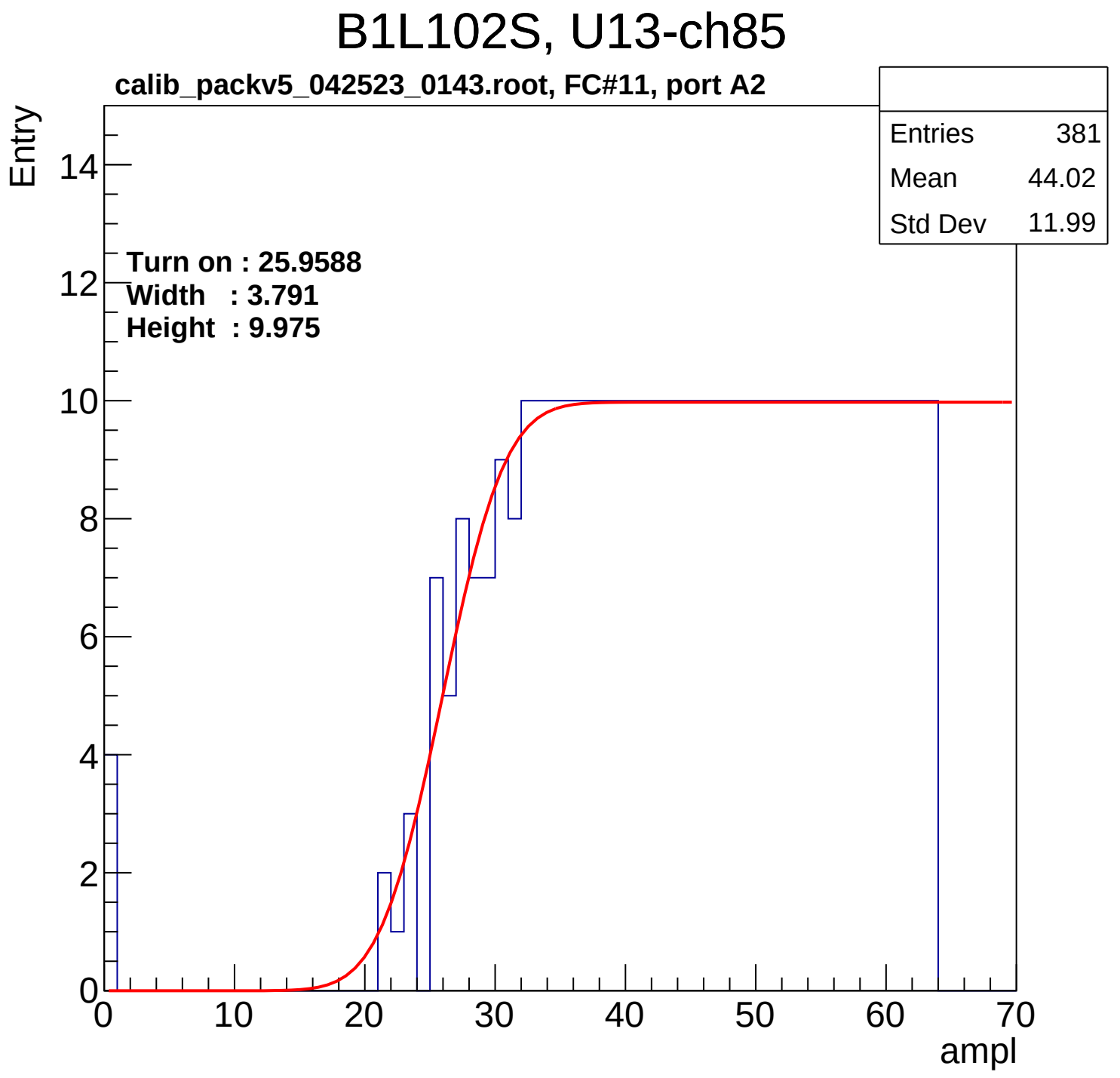
B1L102S, U13-ch85
calib_packv5_042523_0143.root, FC#11, port A2
Entries 381
Mean 44.02
Std Dev 11.99
Turn on : 25.9588
Width : 3.791
Height : 9.975
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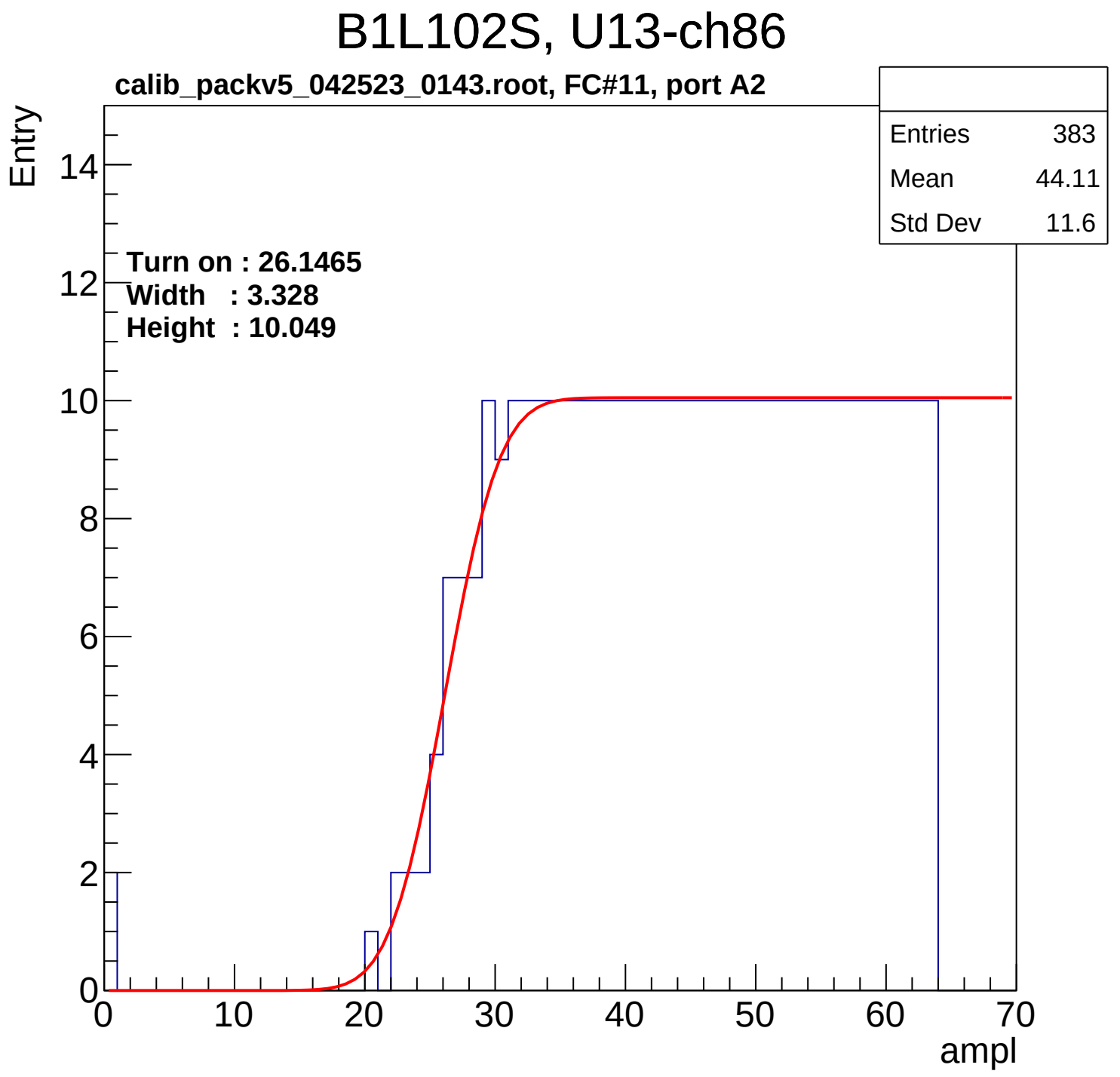
B1L102S, U13-ch86
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 44.11
Std Dev 11.6
Turn on : 26.1465
Width : 3.328
Height : 10.049
Entry
ampl
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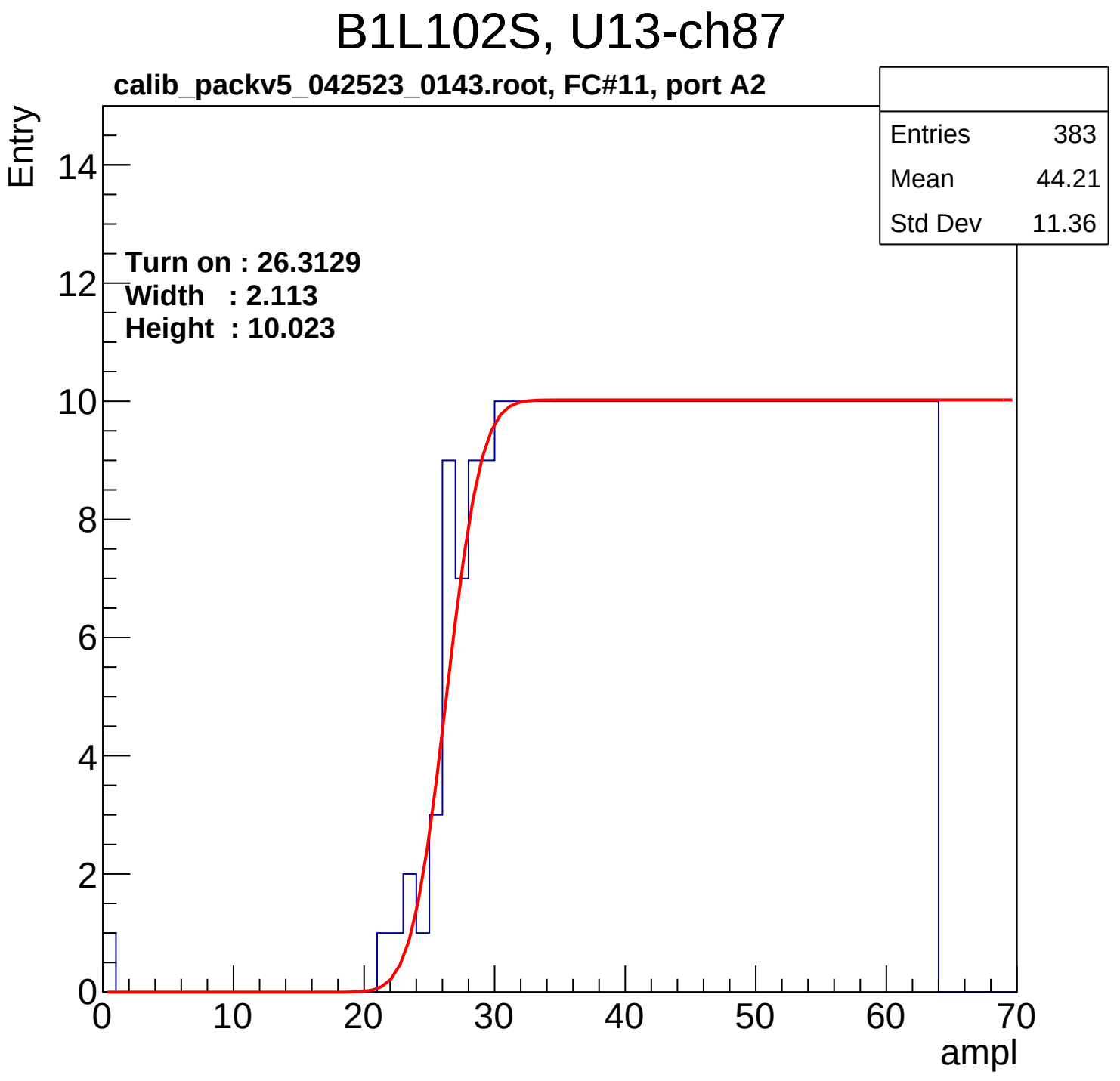
B1L102S, U13-ch87
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 44.21
Std Dev 11.36
Turn on : 26.3129
Width : 2.113
Height : 10.023
Entry
ampl
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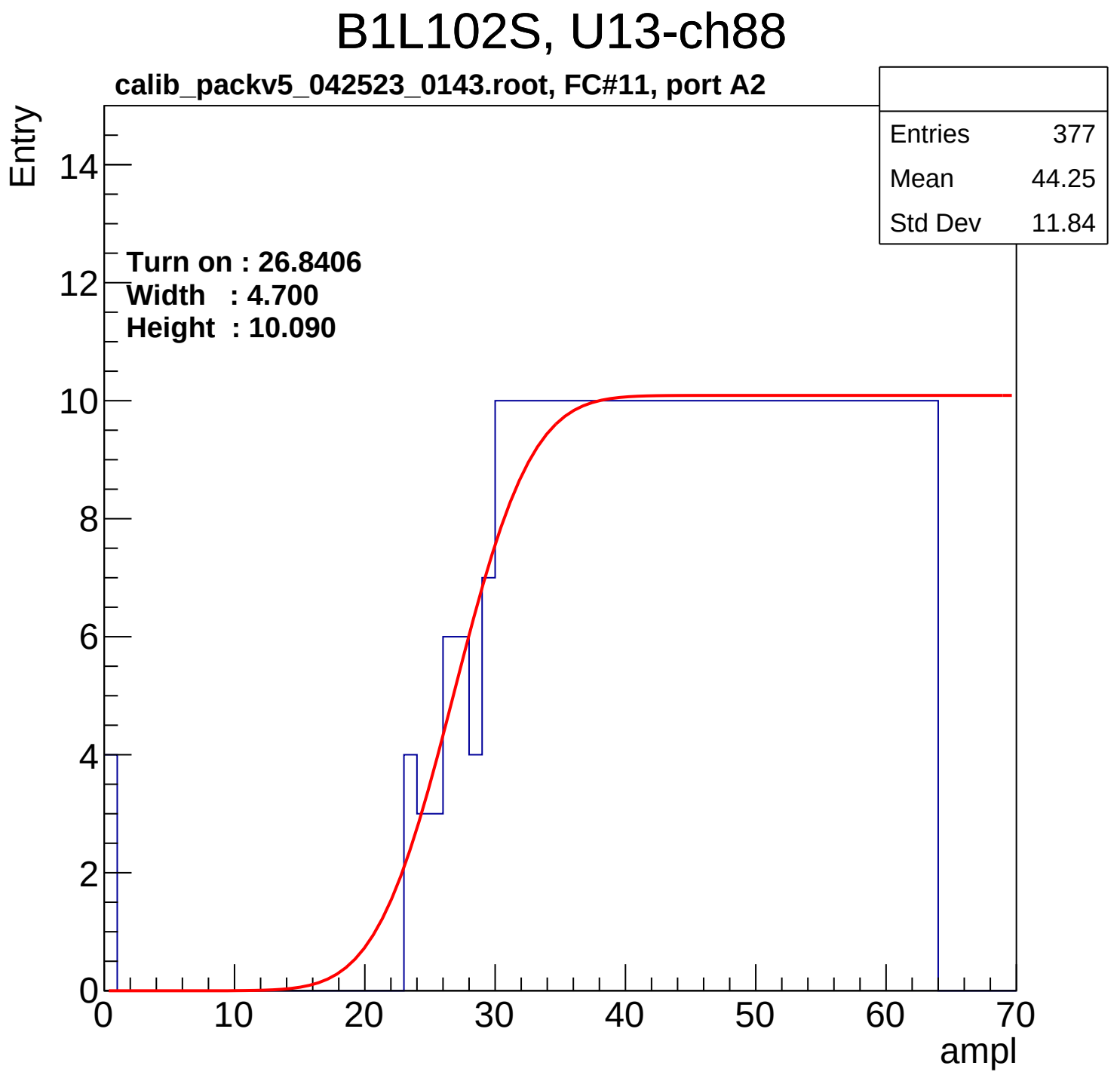
B1L102S, U13-ch88
calib_packv5_042523_0143.root, FC#11, port A2
Entries 377
Mean 44.25
Std Dev 11.84
Turn on : 26.8406
Width : 4.700
Height : 10.090
Entry
ampl
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4
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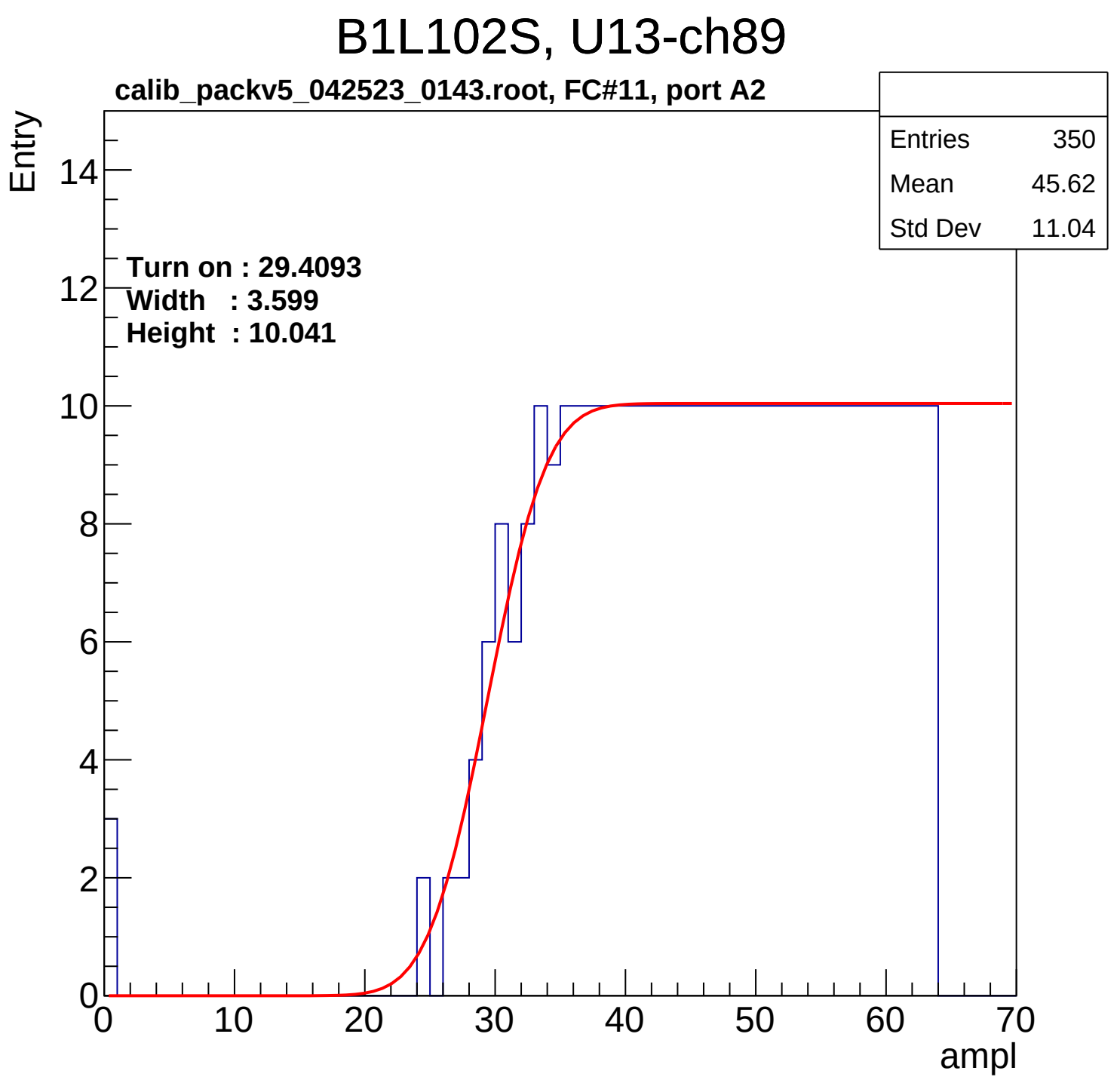
B1L102S, U13-ch89
calib_packv5_042523_0143.root, FC#11, port A2
Entries 350
Mean 45.62
Std Dev 11.04
Turn on : 29.4093
Width : 3.599
Height : 10.041
Entry
ampl
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2
4
6
8
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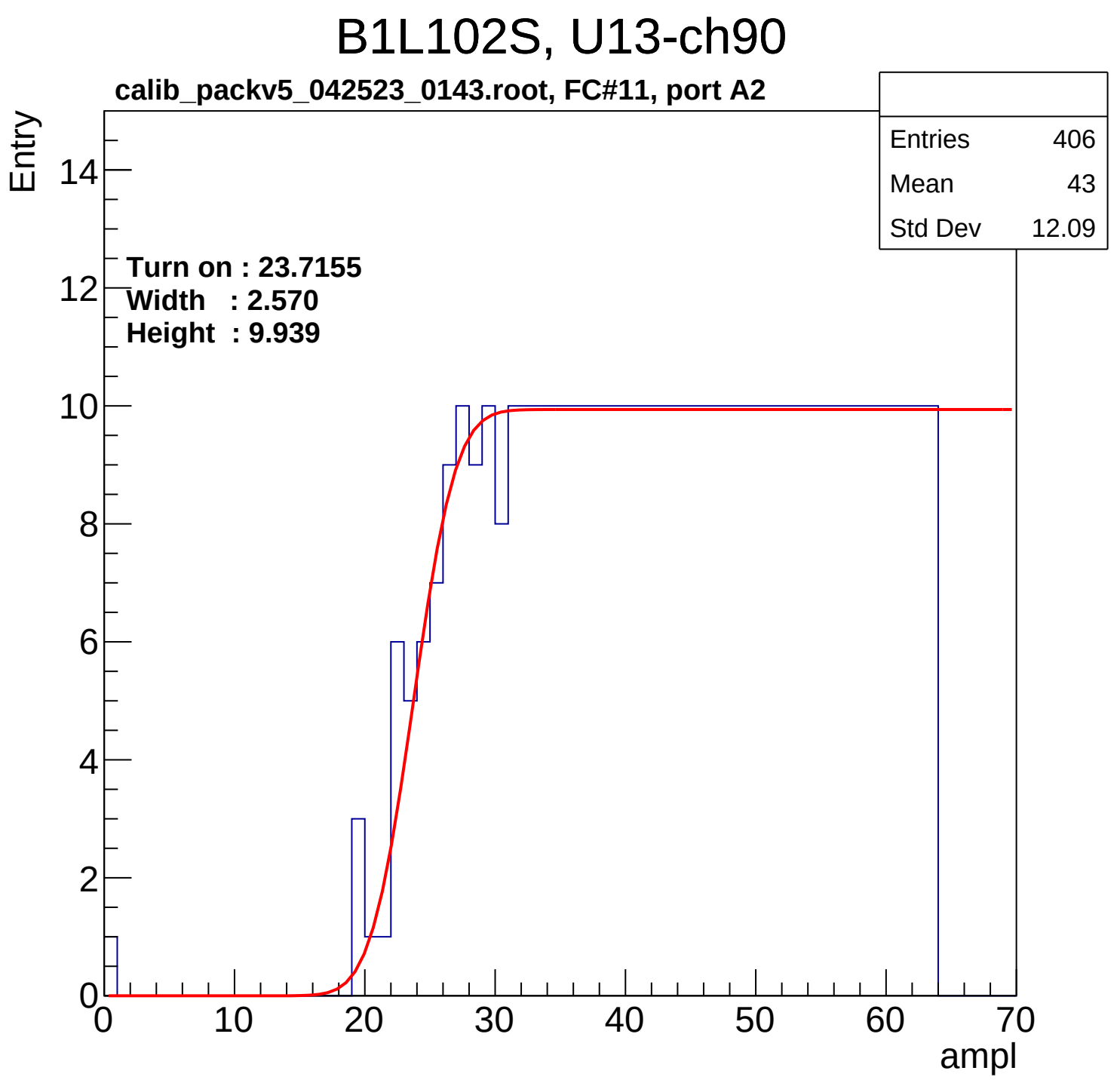
B1L102S, U13-ch90
calib_packv5_042523_0143.root, FC#11, port A2
Entries 406
Mean 43
Std Dev 12.09
Turn on : 23.7155
Width : 2.570
Height : 9.939
Entry
ampl
0
2
4
6
8
10
12
14
0
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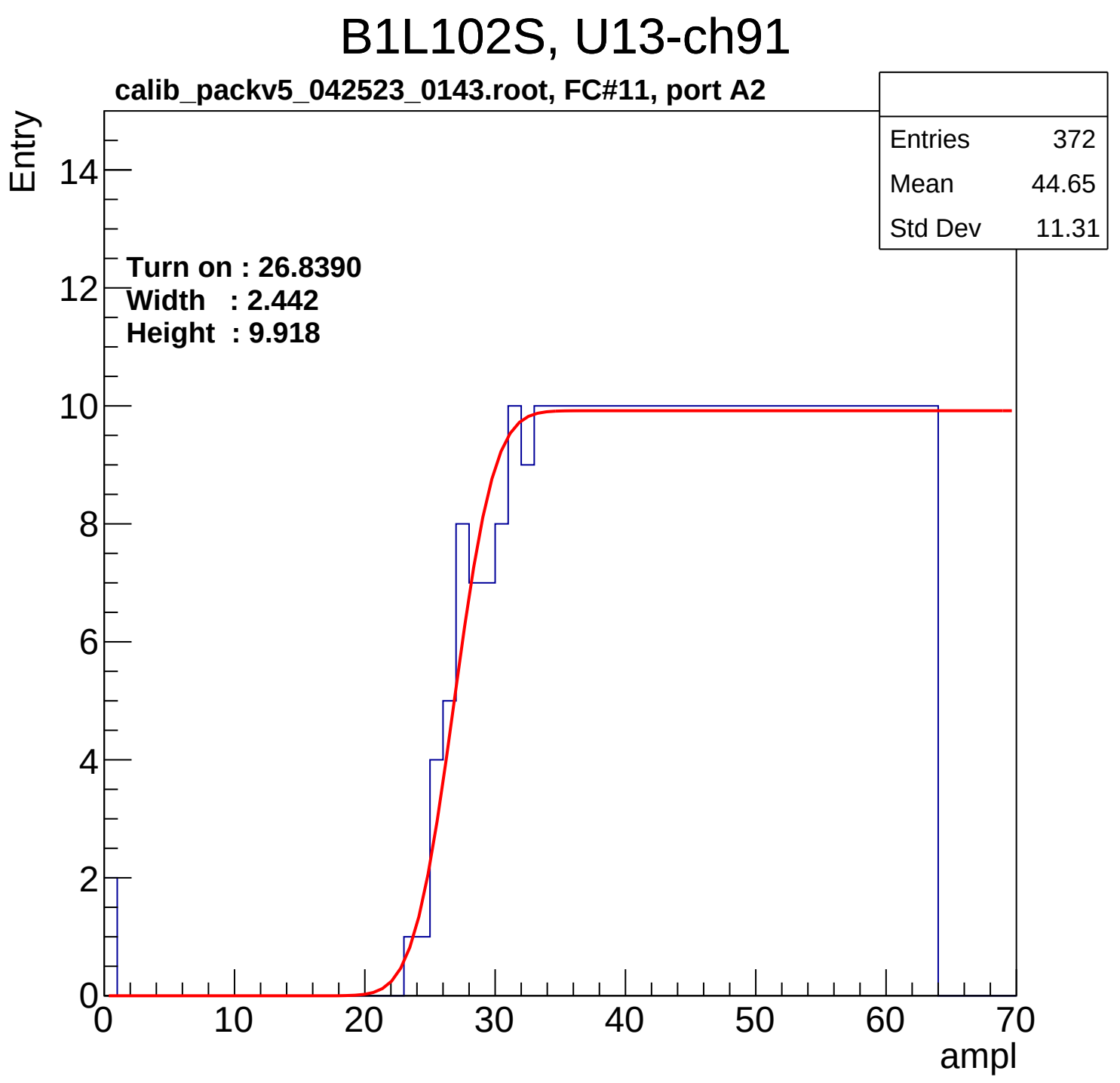
B1L102S, U13-ch91
calib_packv5_042523_0143.root, FC#11, port A2
Entries 372
Mean 44.65
Std Dev 11.31
Turn on : 26.8390
Width : 2.442
Height : 9.918
Entry
ampl
0
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4
6
8
10
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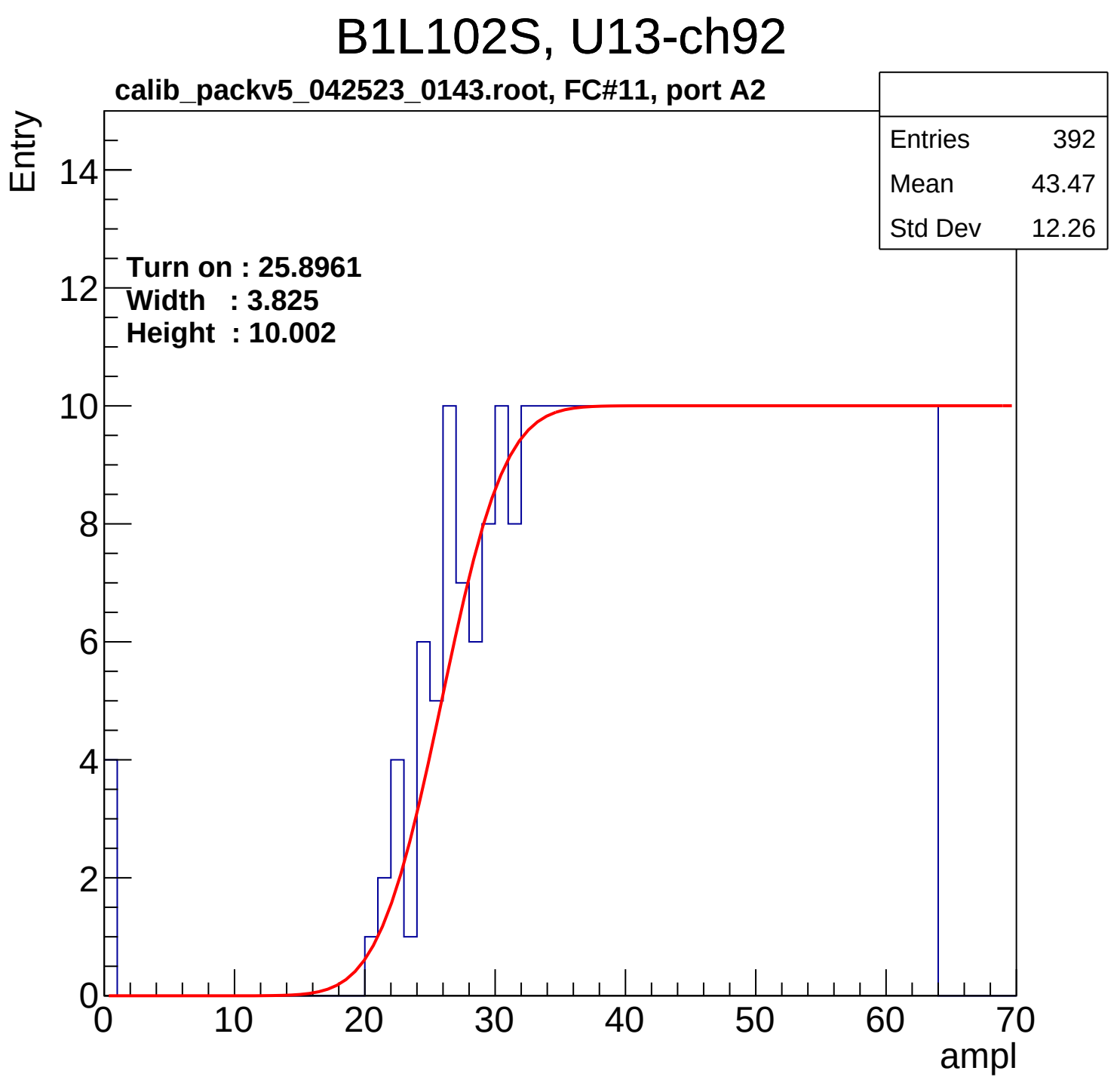
B1L102S, U13-ch92
calib_packv5_042523_0143.root, FC#11, port A2
Entries 392
Mean 43.47
Std Dev 12.26
Turn on : 25.8961
Width : 3.825
Height : 10.002
Entry
ampl
0
2
4
6
8
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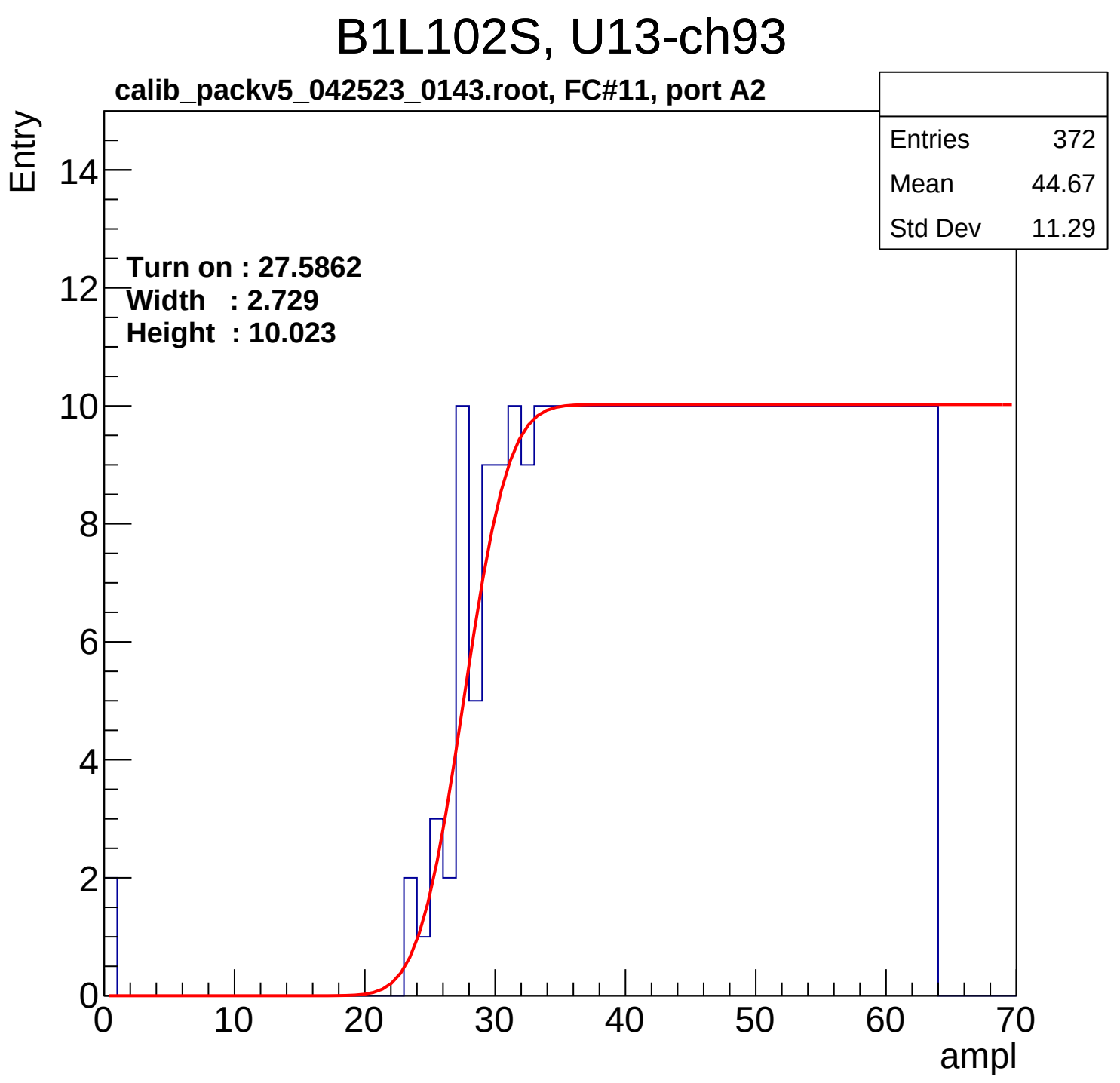
B1L102S, U13-ch93
calib_packv5_042523_0143.root, FC#11, port A2
Entries 372
Mean 44.67
Std Dev 11.29
Turn on : 27.5862
Width : 2.729
Height : 10.023
Entry
ampl
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4
6
8
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14
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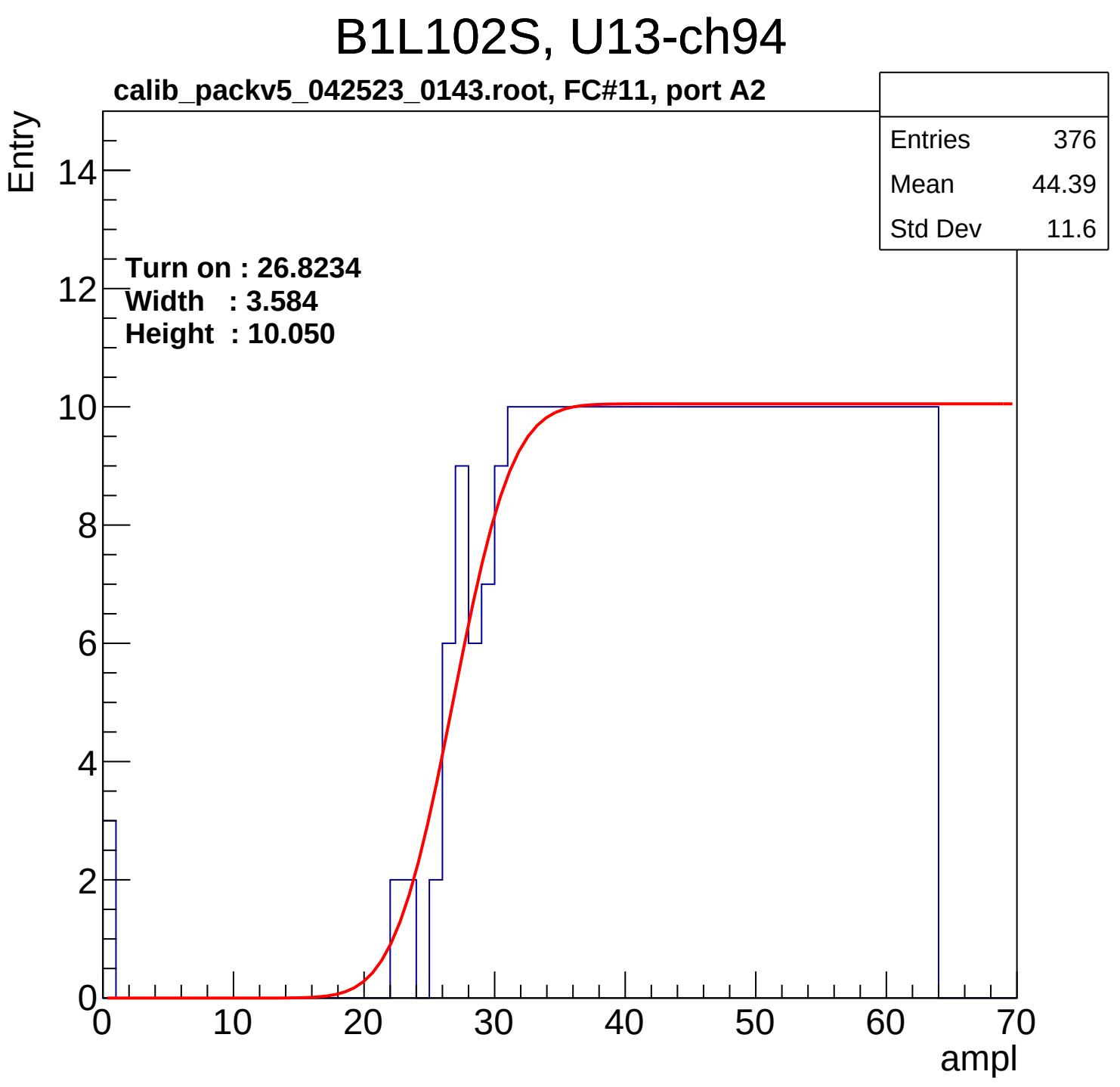
B1L102S, U13-ch94
calib_packv5_042523_0143.root, FC#11, port A2
Entries 376
Mean 44.39
Std Dev 11.6
Turn on : 26.8234
Width : 3.584
Height : 10.050
Entry
ampl
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2
4
6
8
10
12
14
0
10
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40
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60
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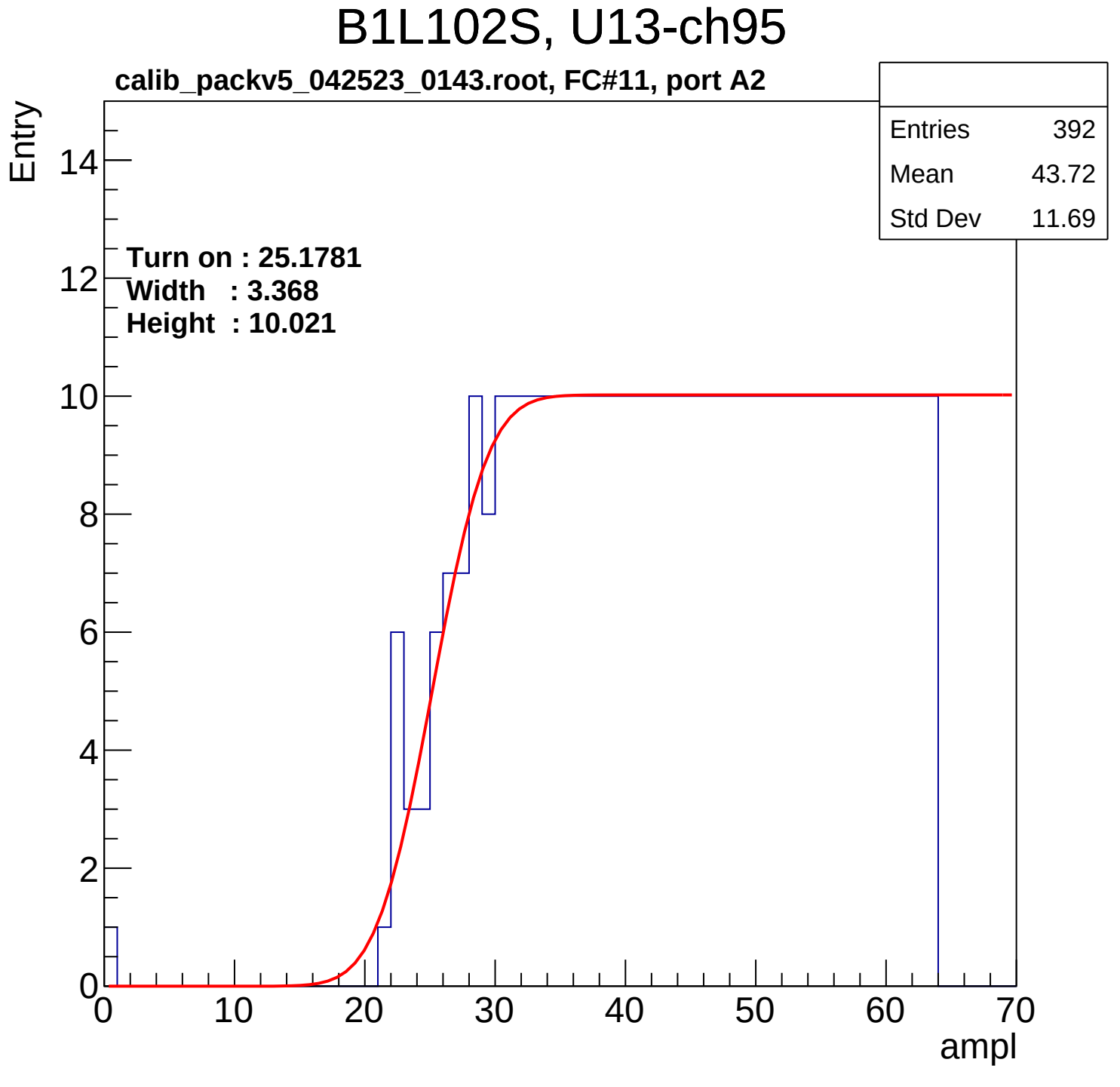
B1L102S, U13-ch95
calib_packv5_042523_0143.root, FC#11, port A2
Entries 392
Mean 43.72
Std Dev 11.69
Turn on : 25.1781
Width : 3.368
Height : 10.021
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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60
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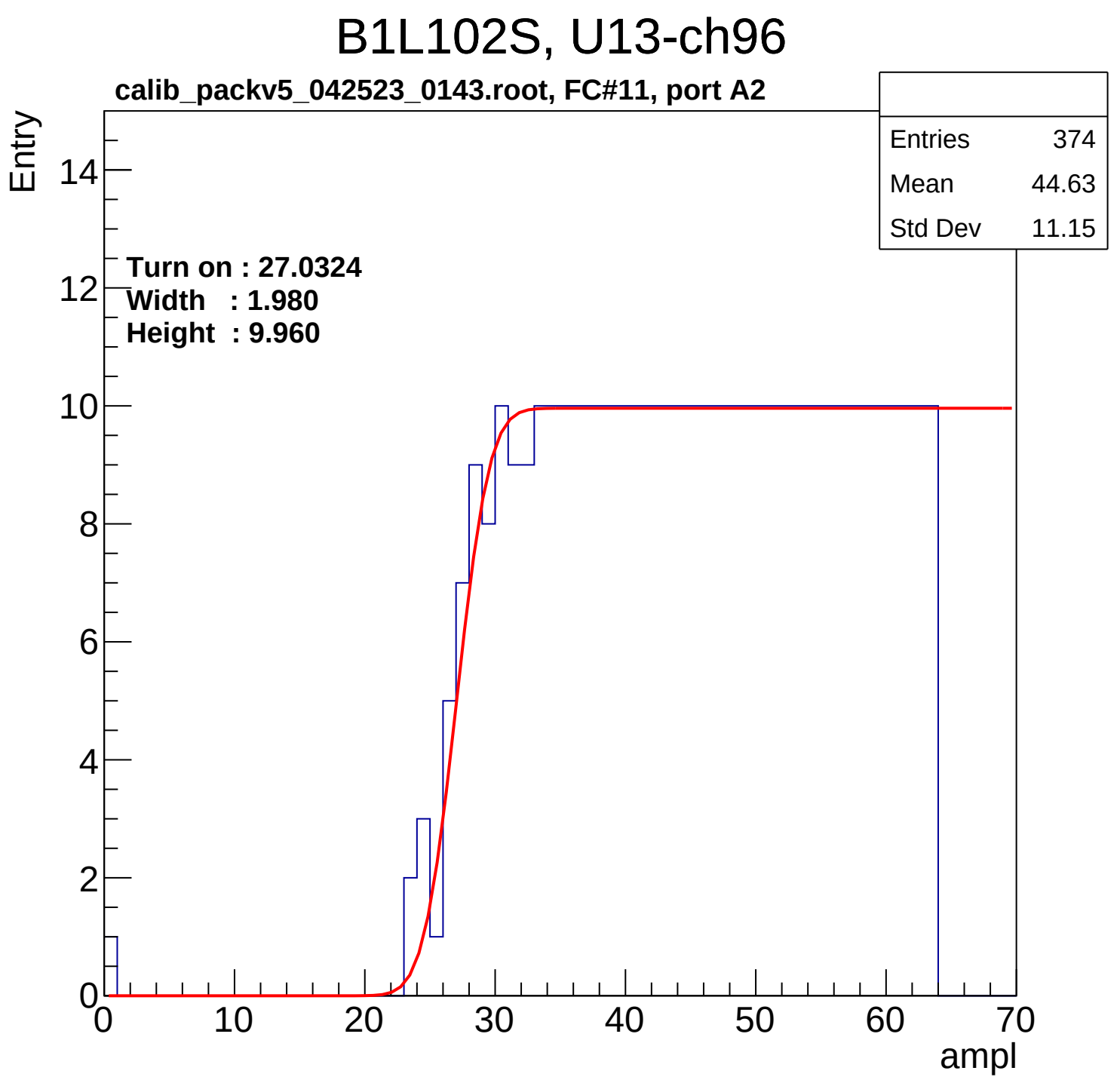
B1L102S, U13-ch96
calib_packv5_042523_0143.root, FC#11, port A2
Entries 374
Mean 44.63
Std Dev 11.15
Turn on : 27.0324
Width : 1.980
Height : 9.960
Entry
ampl
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2
4
6
8
10
12
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0
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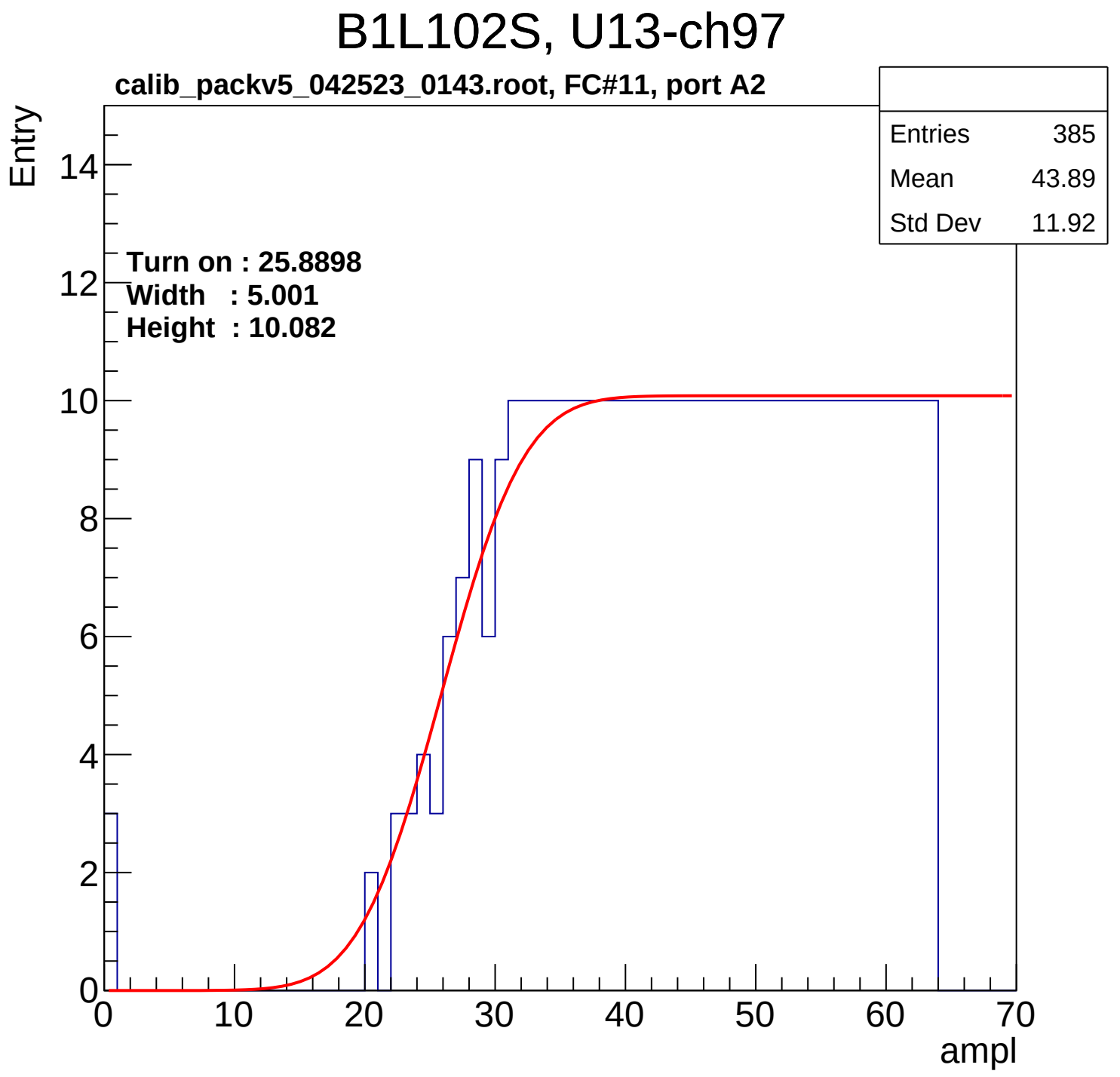
B1L102S, U13-ch97
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 43.89
Std Dev 11.92
Turn on : 25.8898
Width : 5.001
Height : 10.082
Entry
ampl
0
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4
6
8
10
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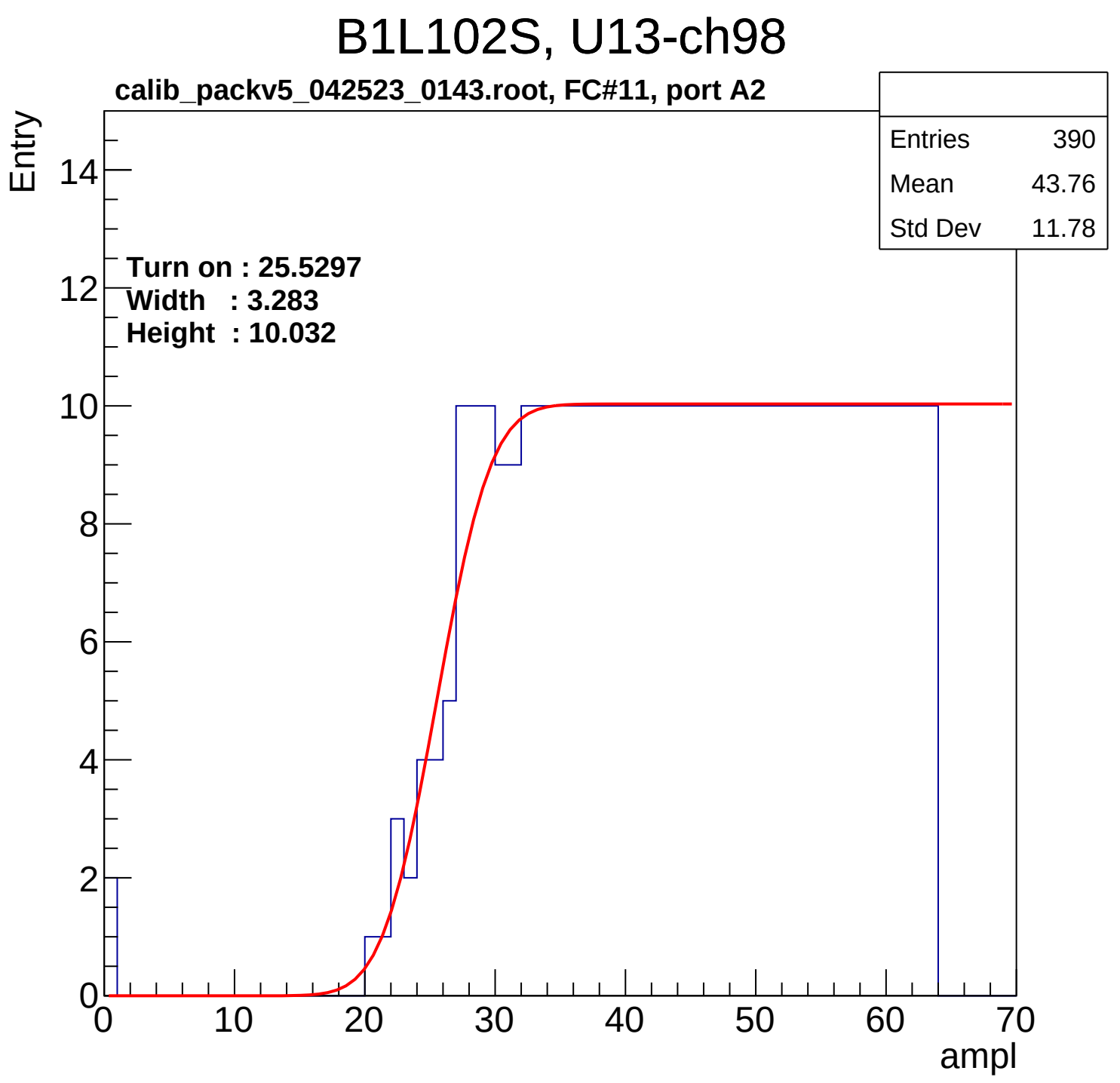
B1L102S, U13-ch98
calib_packv5_042523_0143.root, FC#11, port A2
Entries 390
Mean 43.76
Std Dev 11.78
Turn on : 25.5297
Width : 3.283
Height : 10.032
Entry
ampl
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6
8
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0
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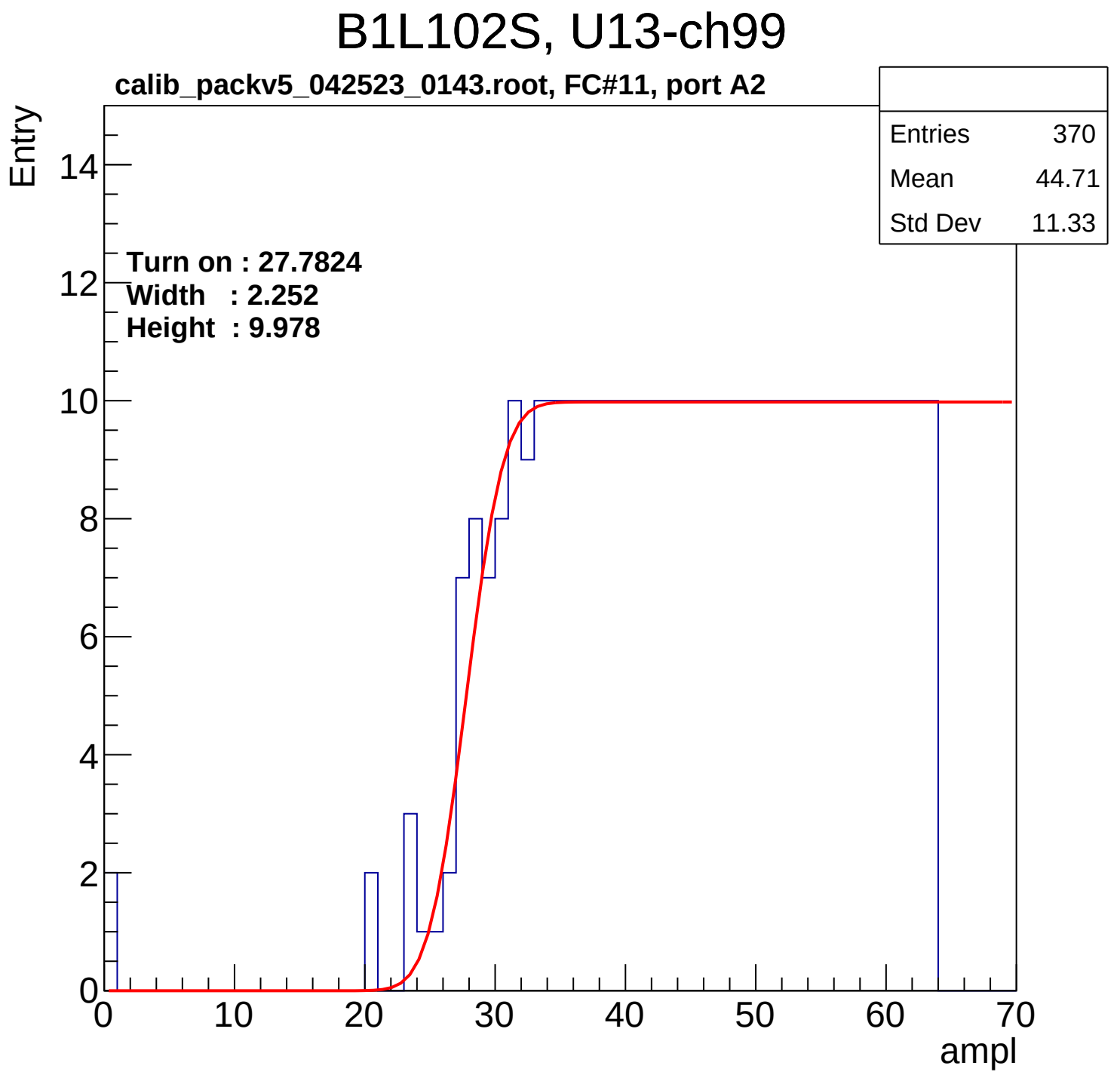
B1L102S, U13-ch99
calib_packv5_042523_0143.root, FC#11, port A2
Entries 370
Mean 44.71
Std Dev 11.33
Turn on : 27.7824
Width : 2.252
Height : 9.978
Entry
ampl
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2
4
6
8
10
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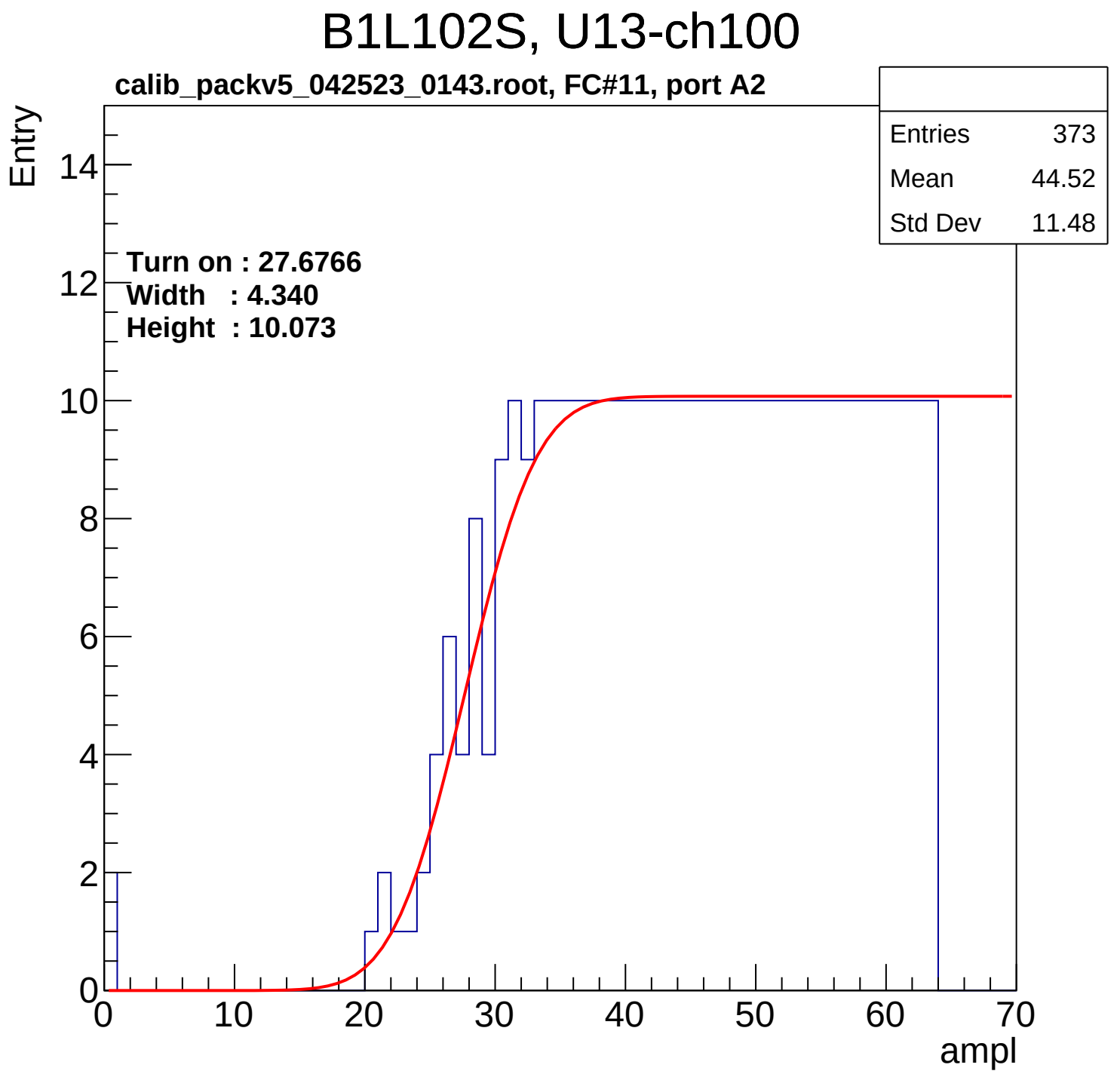
B1L102S, U13-ch100
calib_packv5_042523_0143.root, FC#11, port A2
Entries 373
Mean 44.52
Std Dev 11.48
Turn on : 27.6766
Width : 4.340
Height : 10.073
Entry
ampl
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6
8
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0
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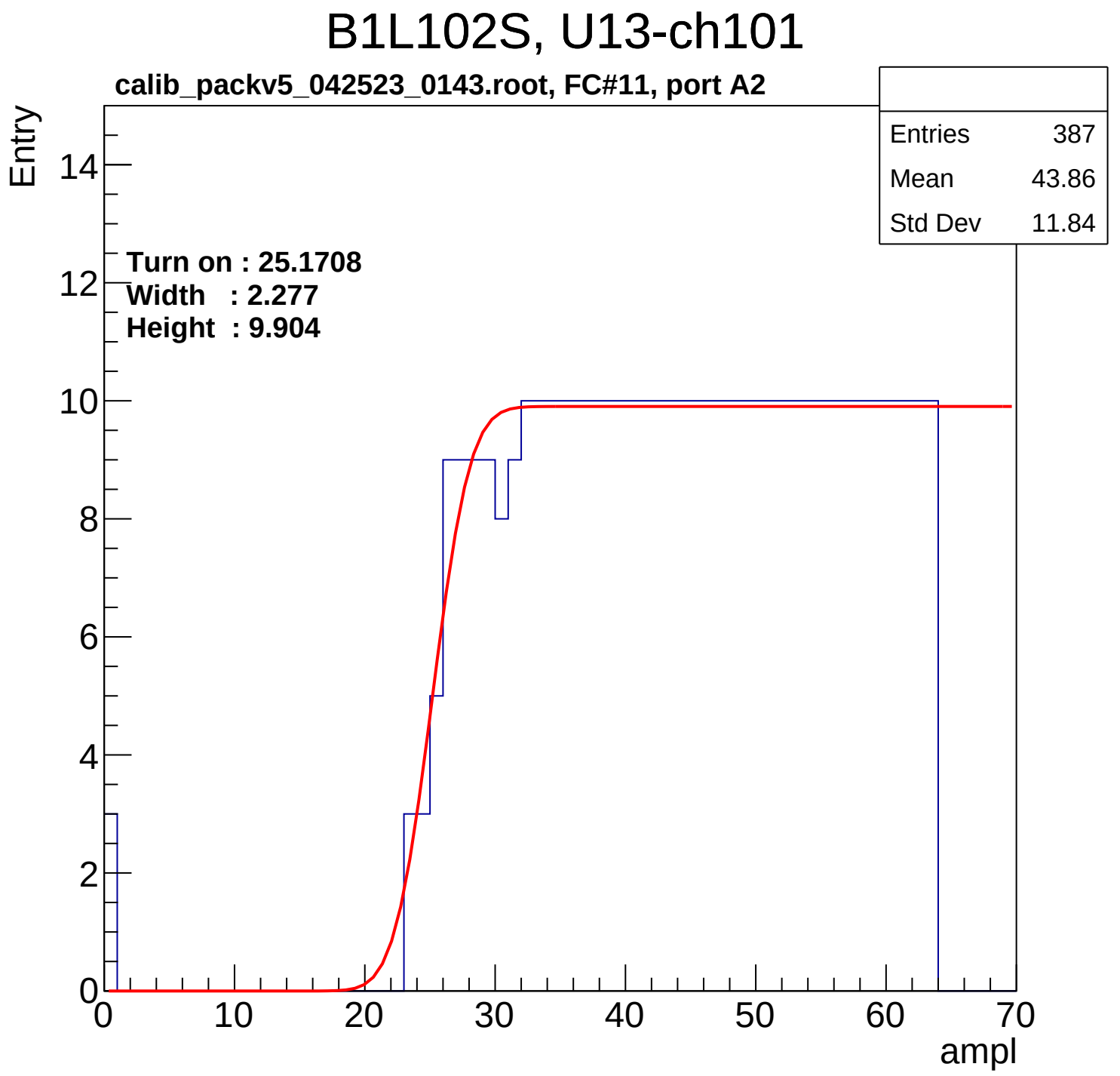
B1L102S, U13-ch101
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 43.86
Std Dev 11.84
Turn on : 25.1708
Width : 2.277
Height : 9.904
Entry
ampl
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6
8
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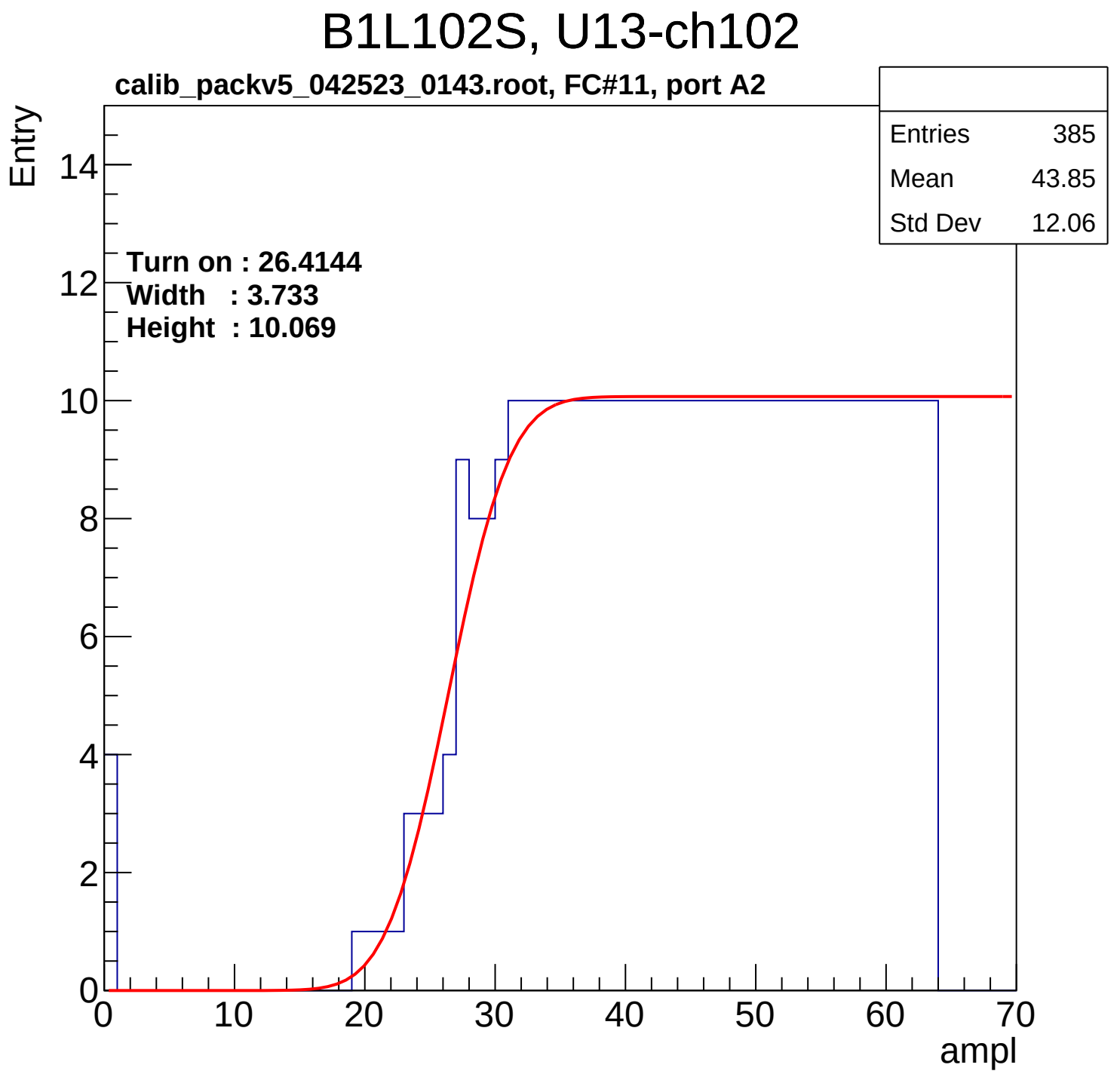
B1L102S, U13-ch102
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 43.85
Std Dev 12.06
Turn on : 26.4144
Width : 3.733
Height : 10.069
Entry
ampl
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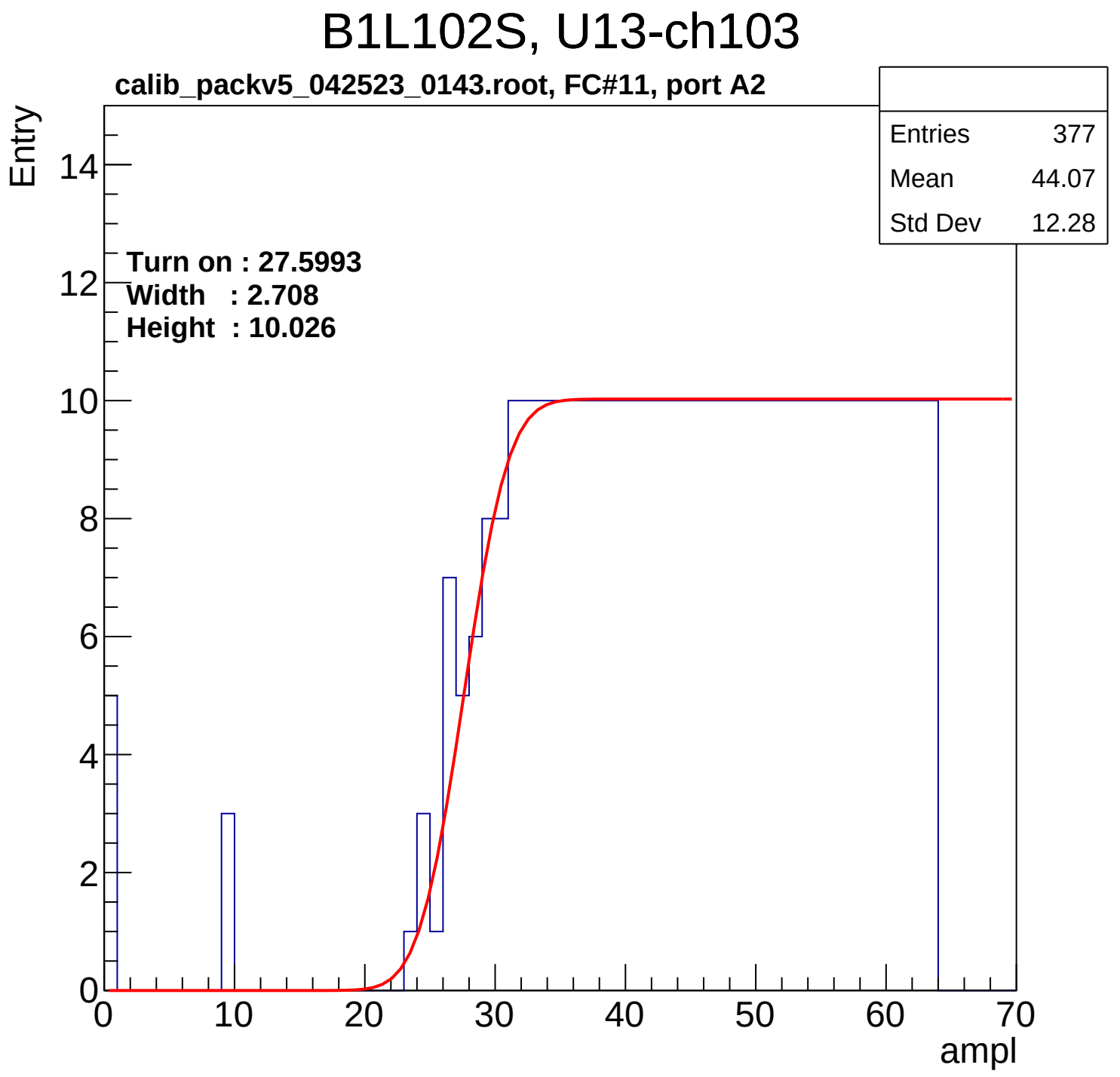
B1L102S, U13-ch103
calib_packv5_042523_0143.root, FC#11, port A2
Entries 377
Mean 44.07
Std Dev 12.28
Turn on : 27.5993
Width : 2.708
Height : 10.026
Entry
ampl
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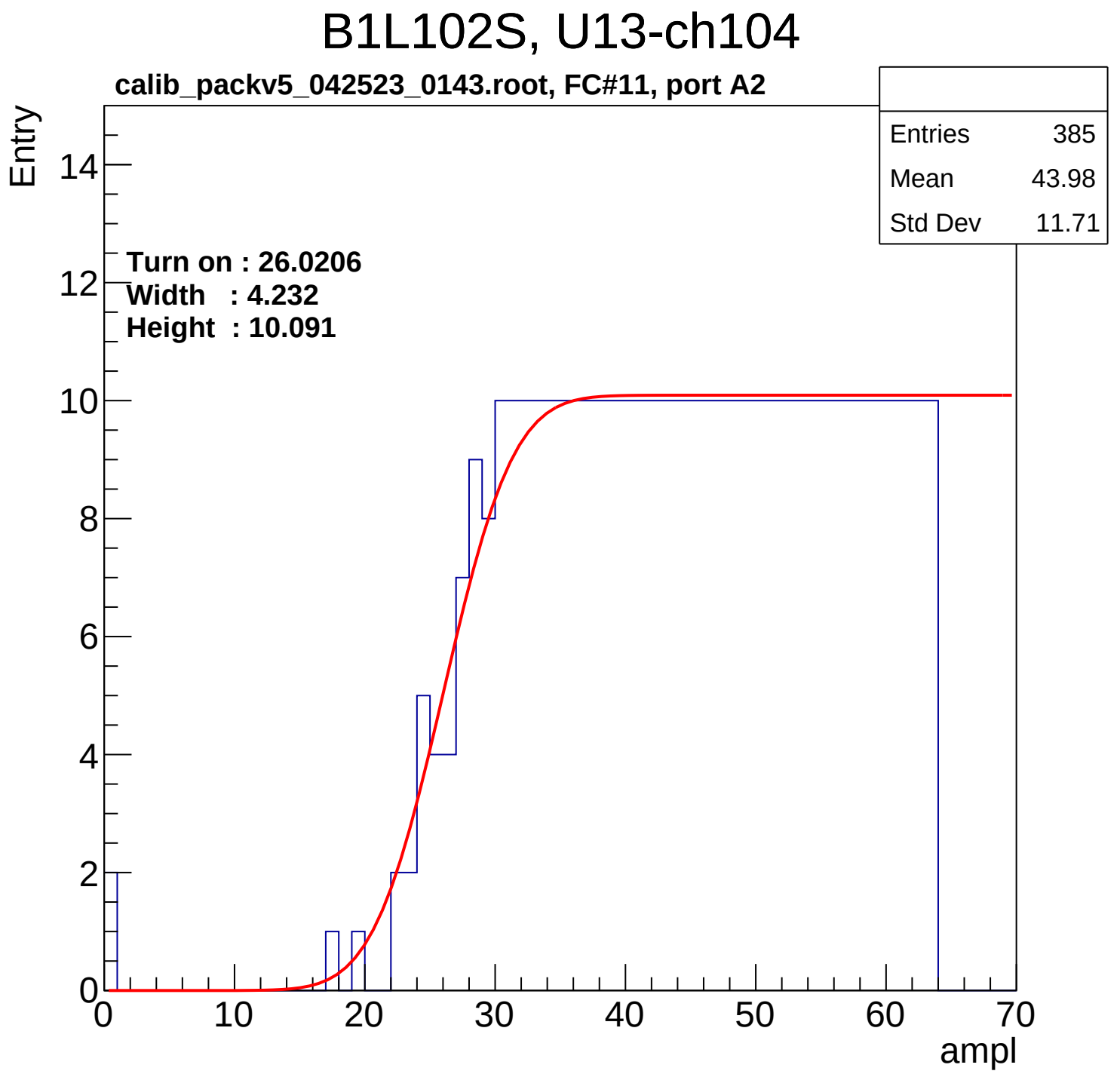
B1L102S, U13-ch104
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 43.98
Std Dev 11.71
Turn on : 26.0206
Width : 4.232
Height : 10.091
Entry
ampl
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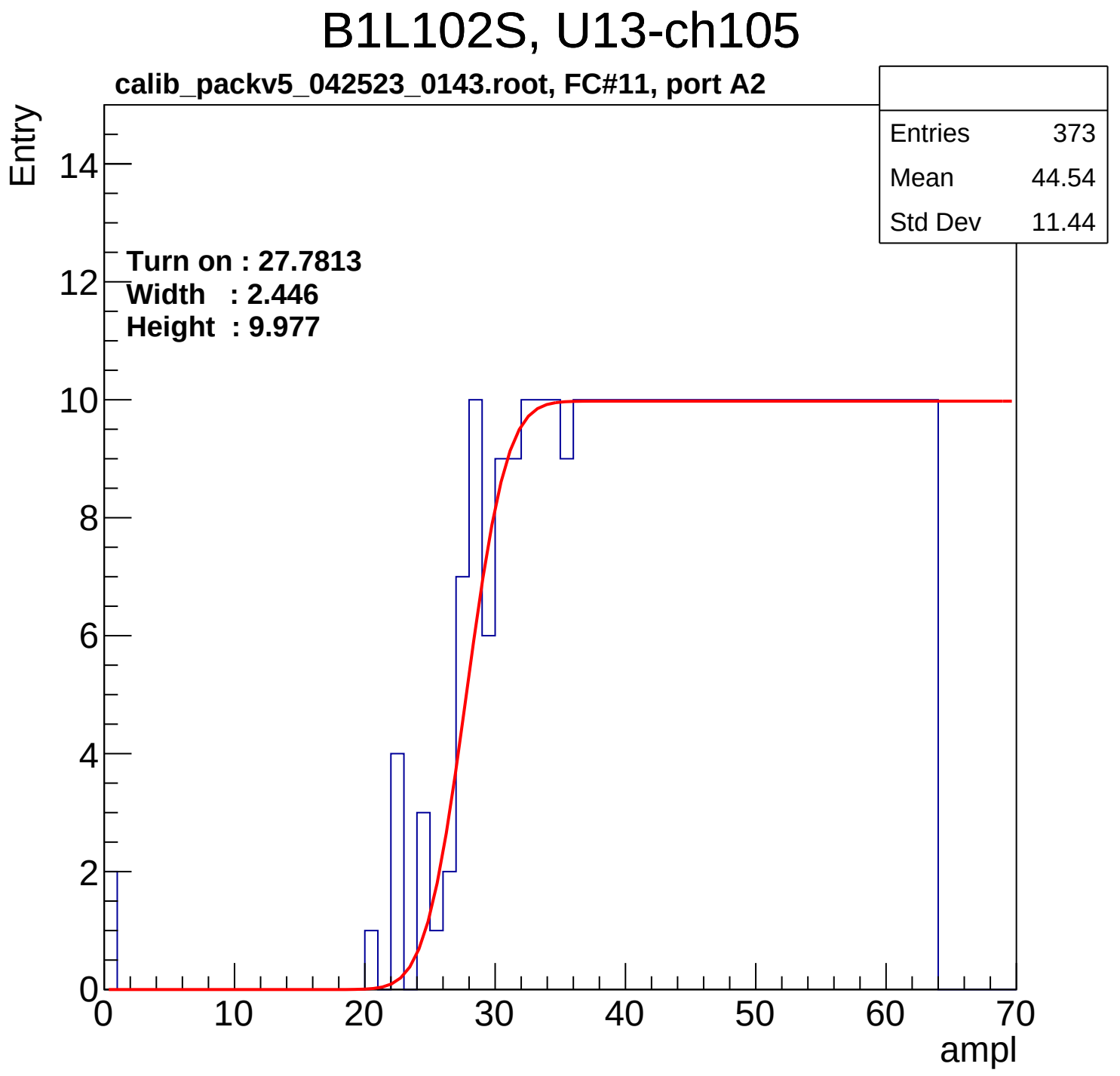
B1L102S, U13-ch105
calib_packv5_042523_0143.root, FC#11, port A2
Entries 373
Mean 44.54
Std Dev 11.44
Turn on : 27.7813
Width : 2.446
Height : 9.977
Entry
ampl
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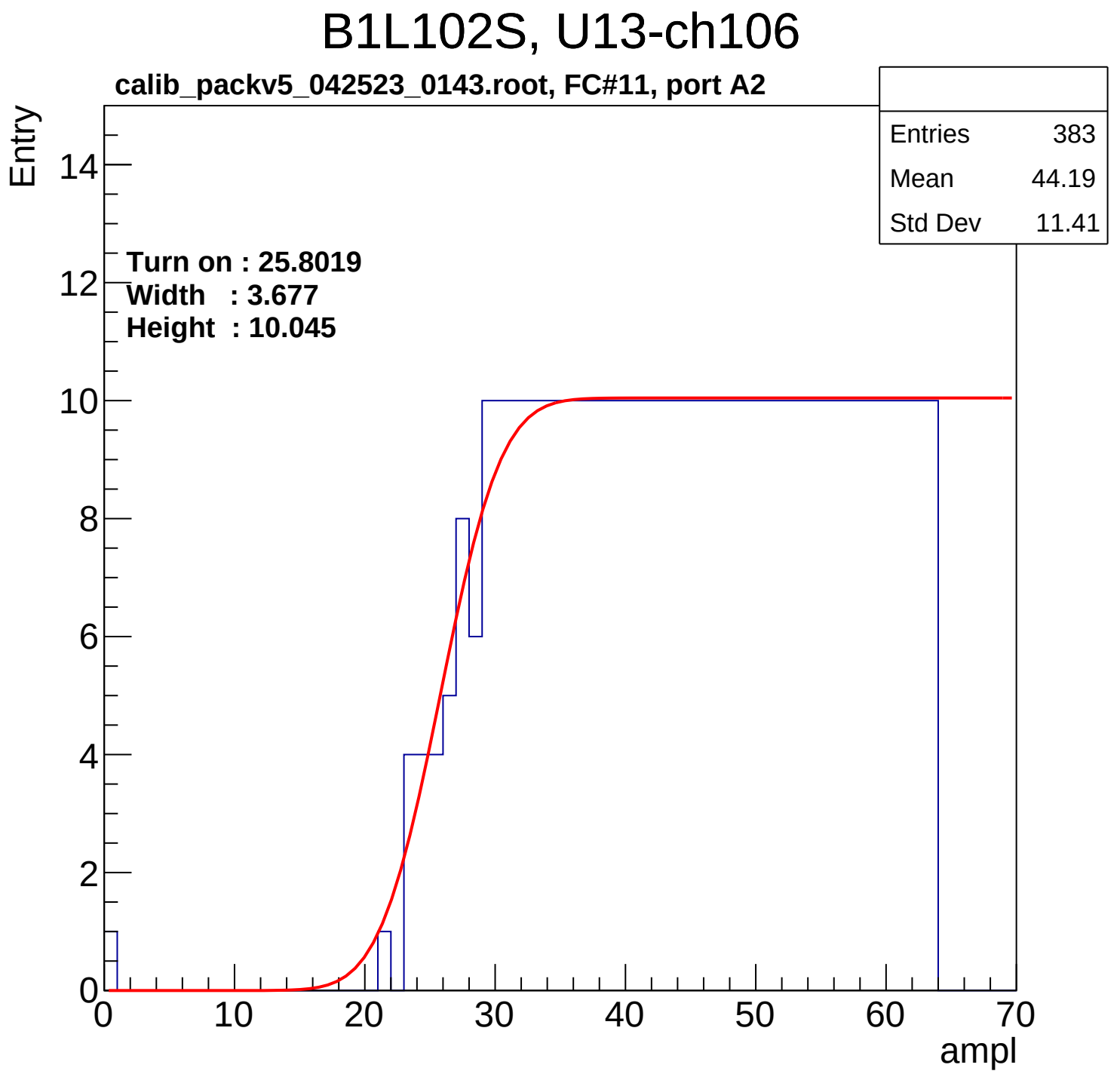
B1L102S, U13-ch106
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 44.19
Std Dev 11.41
Turn on : 25.8019
Width : 3.677
Height : 10.045
Entry
ampl
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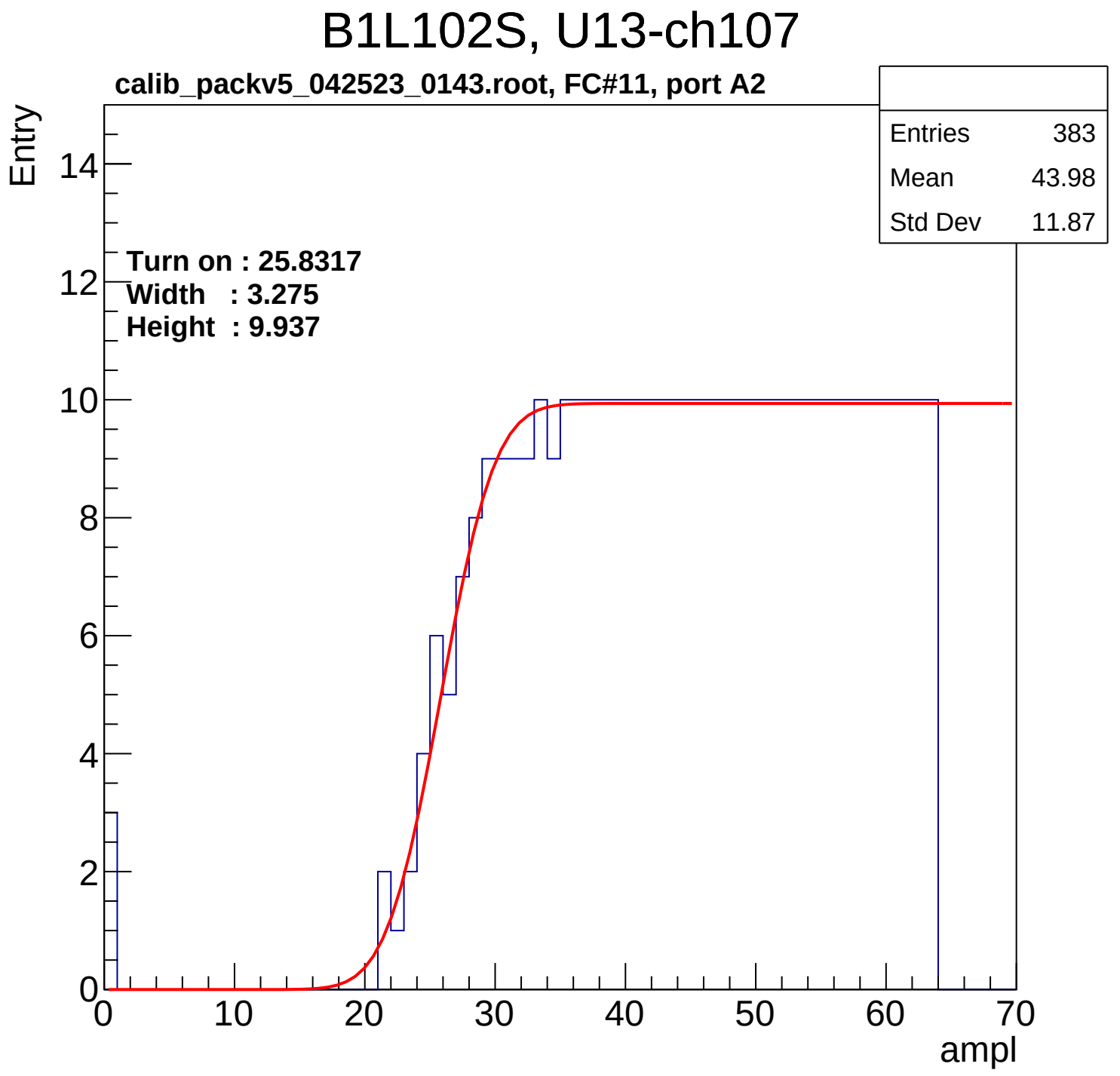
B1L102S, U13-ch107
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 43.98
Std Dev 11.87
Turn on : 25.8317
Width : 3.275
Height : 9.937
Entry
ampl
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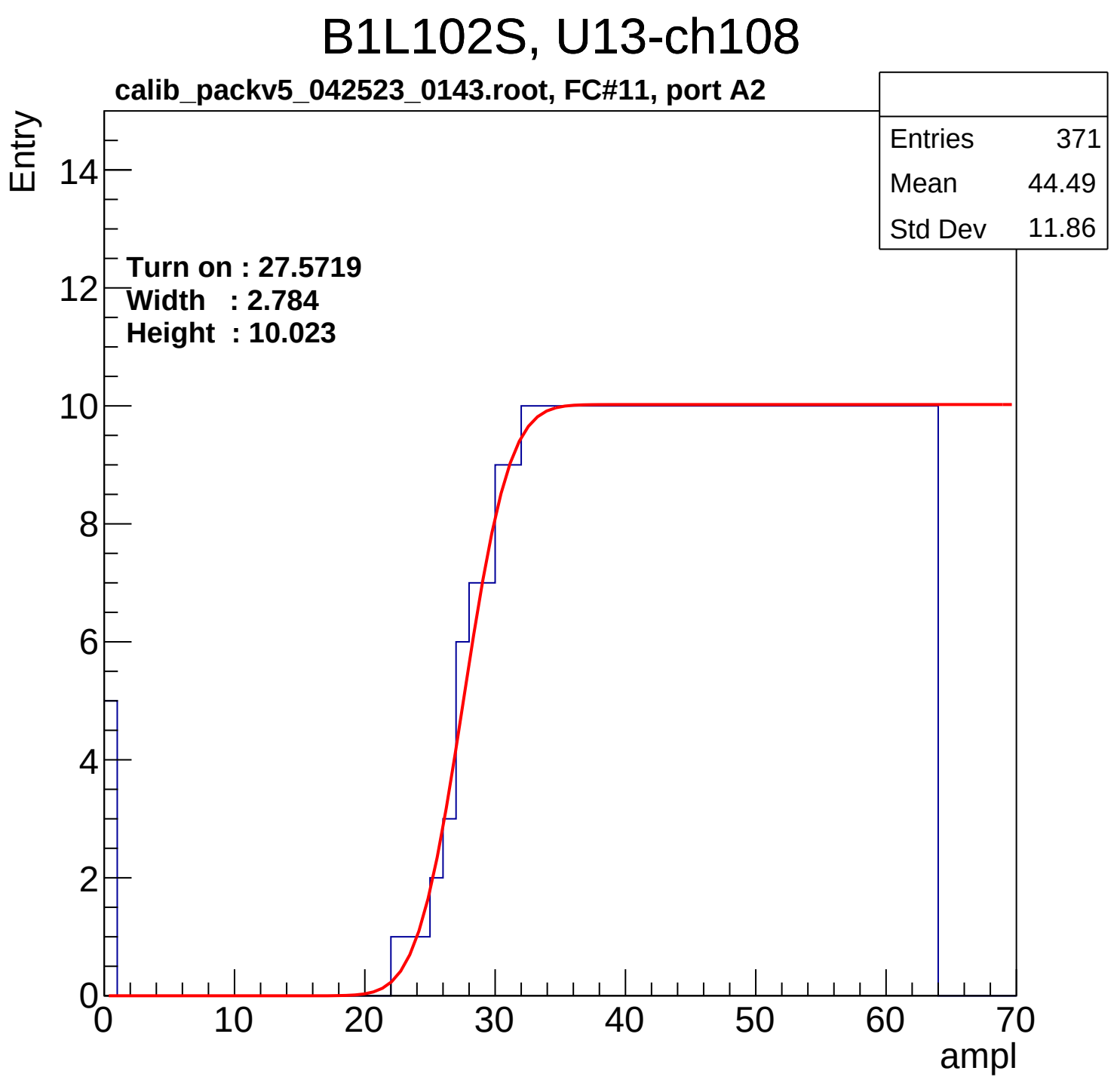
B1L102S, U13-ch108
calib_packv5_042523_0143.root, FC#11, port A2
Entries 371
Mean 44.49
Std Dev 11.86
Turn on : 27.5719
Width : 2.784
Height : 10.023
Entry
ampl
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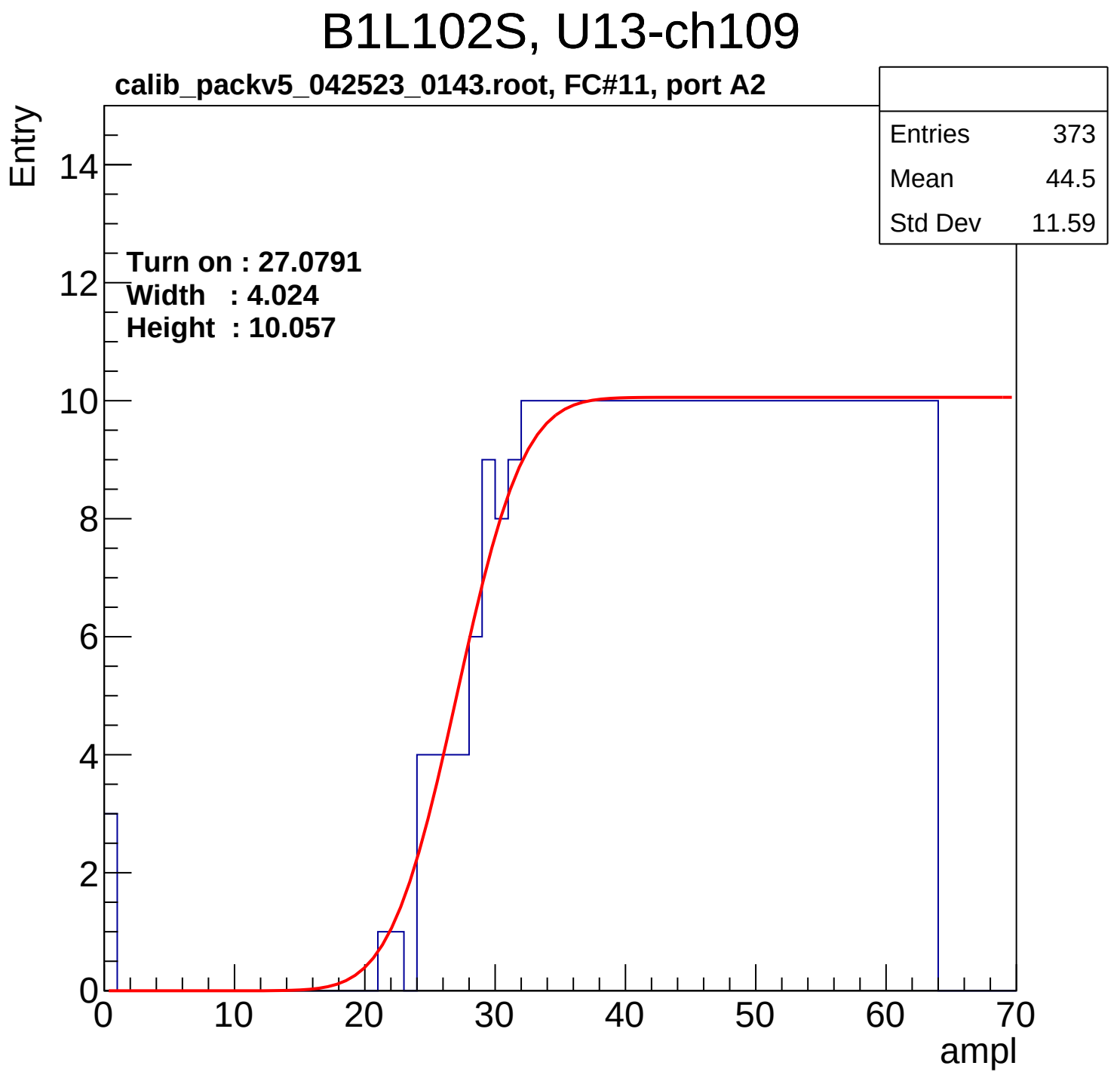
B1L102S, U13-ch109
calib_packv5_042523_0143.root, FC#11, port A2
Entries 373
Mean 44.5
Std Dev 11.59
Turn on : 27.0791
Width : 4.024
Height : 10.057
Entry
ampl
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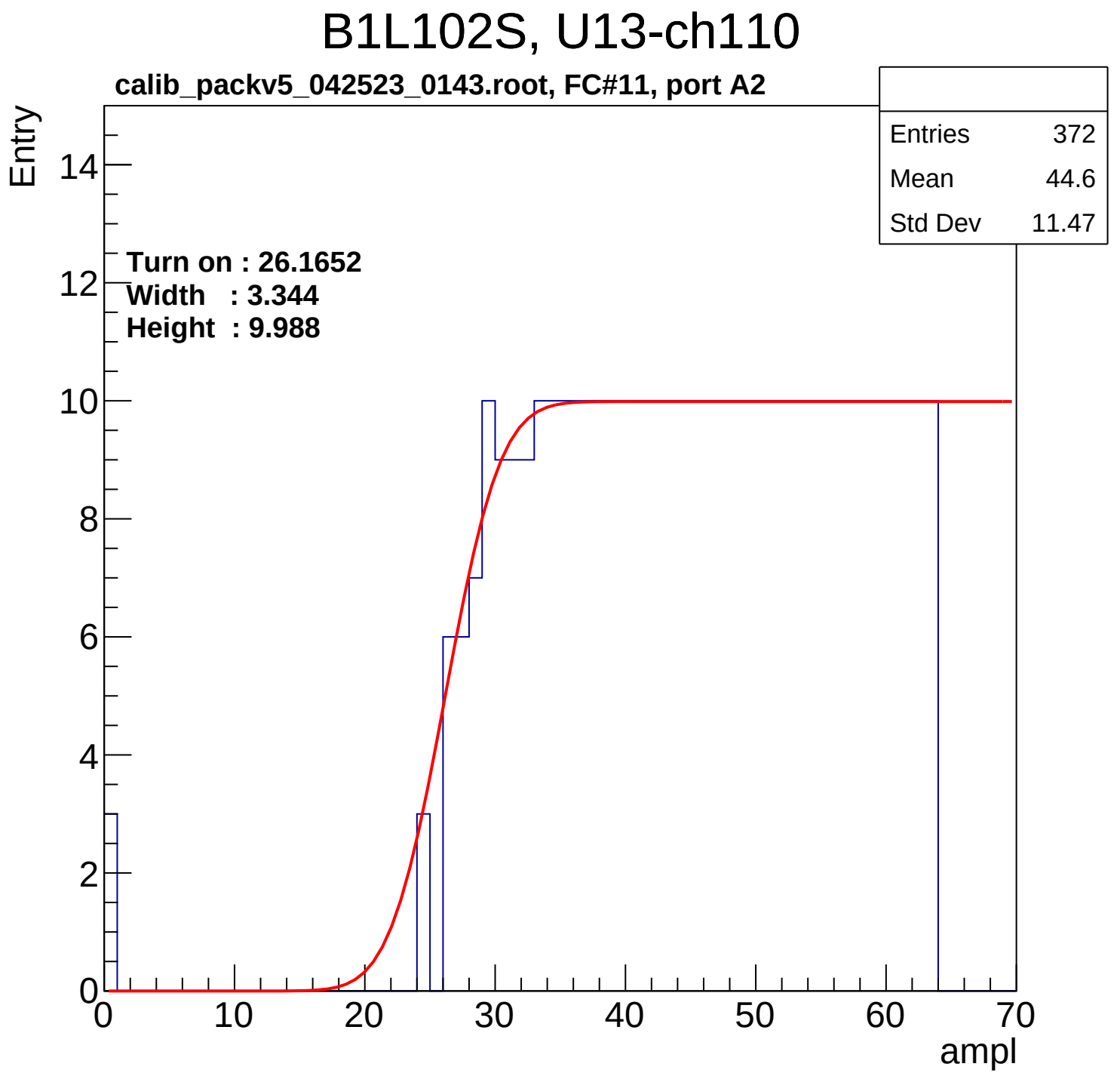
B1L102S, U13-ch110
calib_packv5_042523_0143.root, FC#11, port A2
Entries 372
Mean 44.6
Std Dev 11.47
Turn on : 26.1652
Width : 3.344
Height : 9.988
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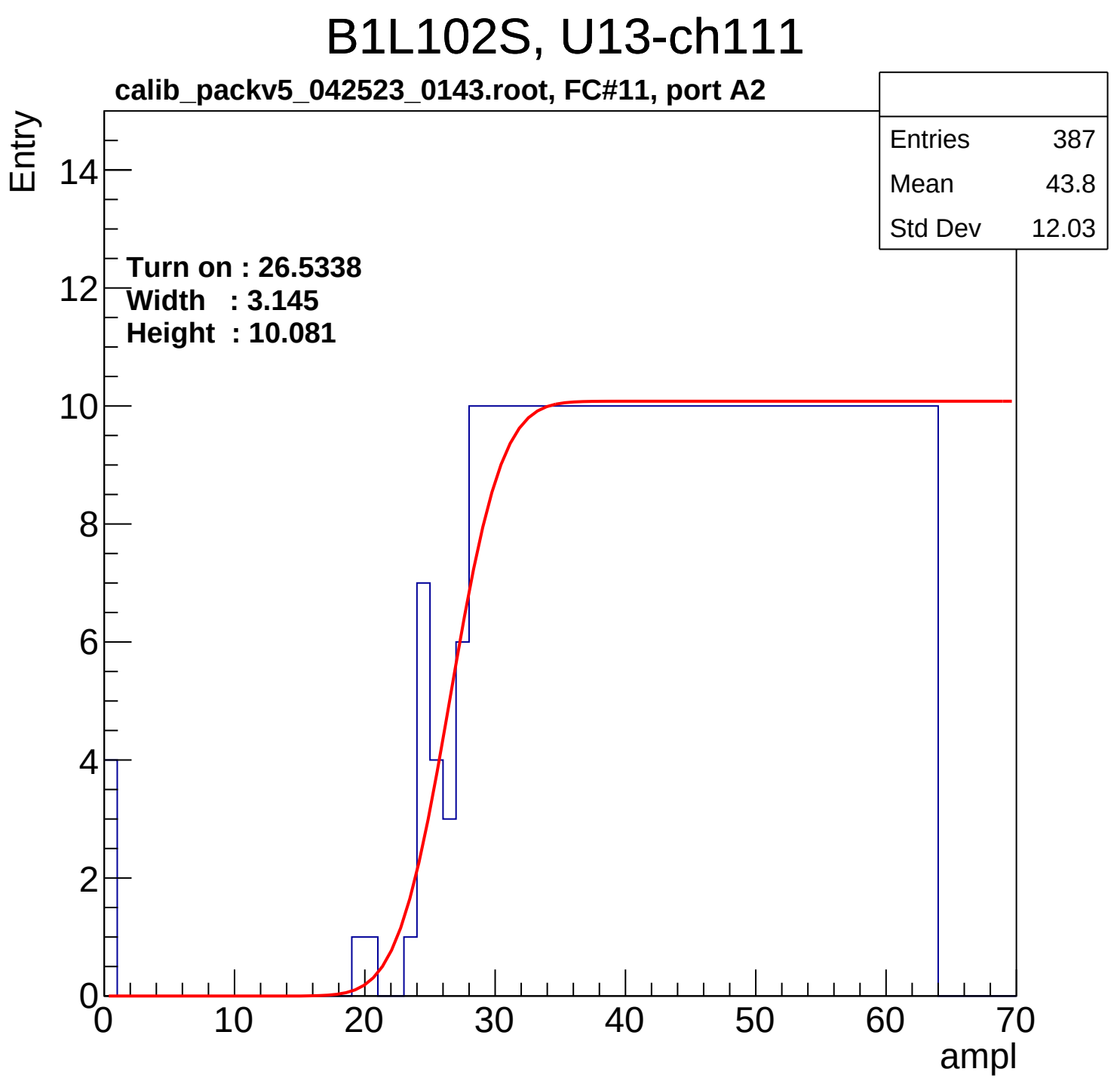
B1L102S, U13-ch111
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 43.8
Std Dev 12.03
Turn on : 26.5338
Width : 3.145
Height : 10.081
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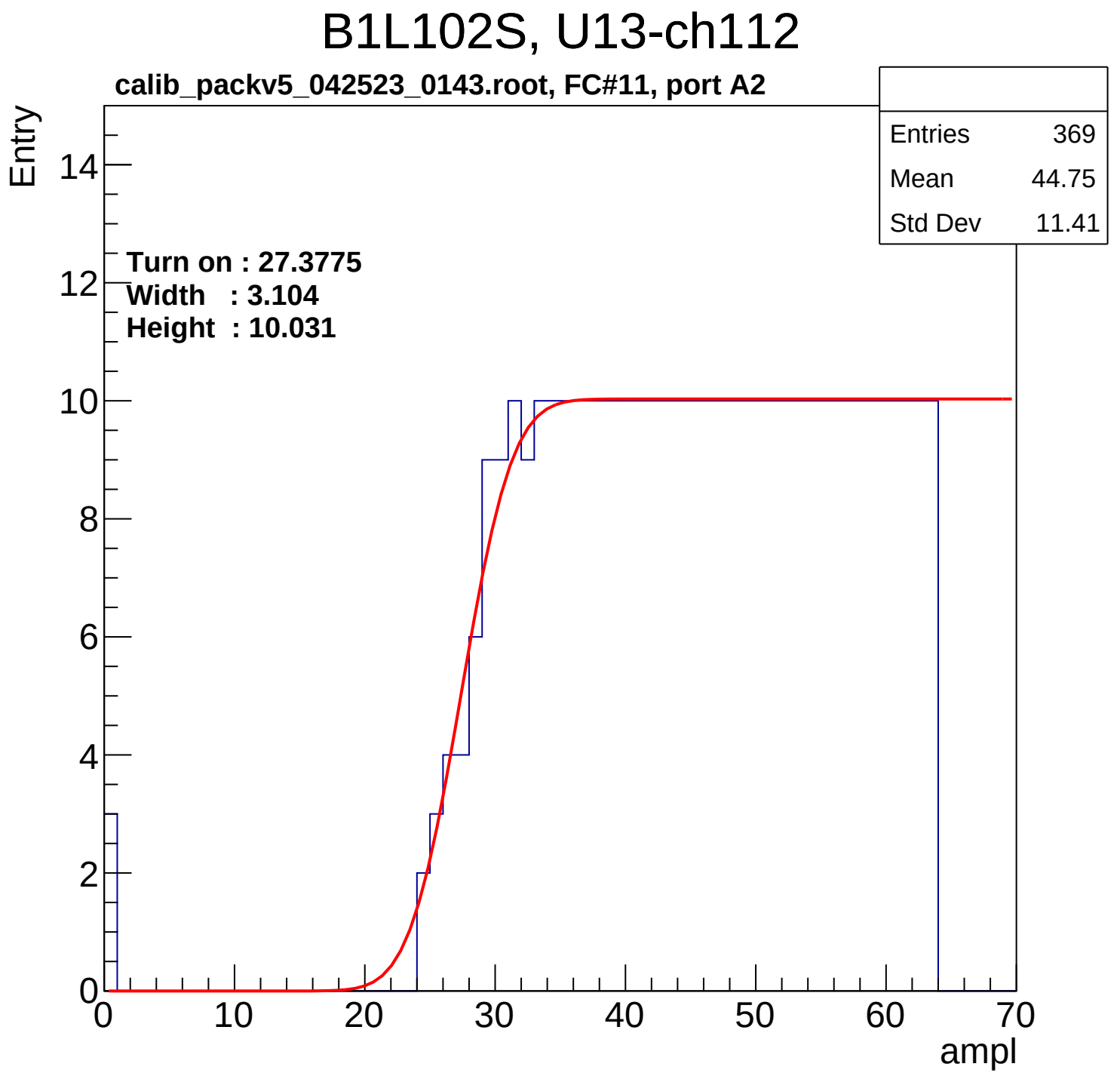
B1L102S, U13-ch112
calib_packv5_042523_0143.root, FC#11, port A2
Entries 369
Mean 44.75
Std Dev 11.41
Turn on : 27.3775
Width : 3.104
Height : 10.031
Entry
ampl
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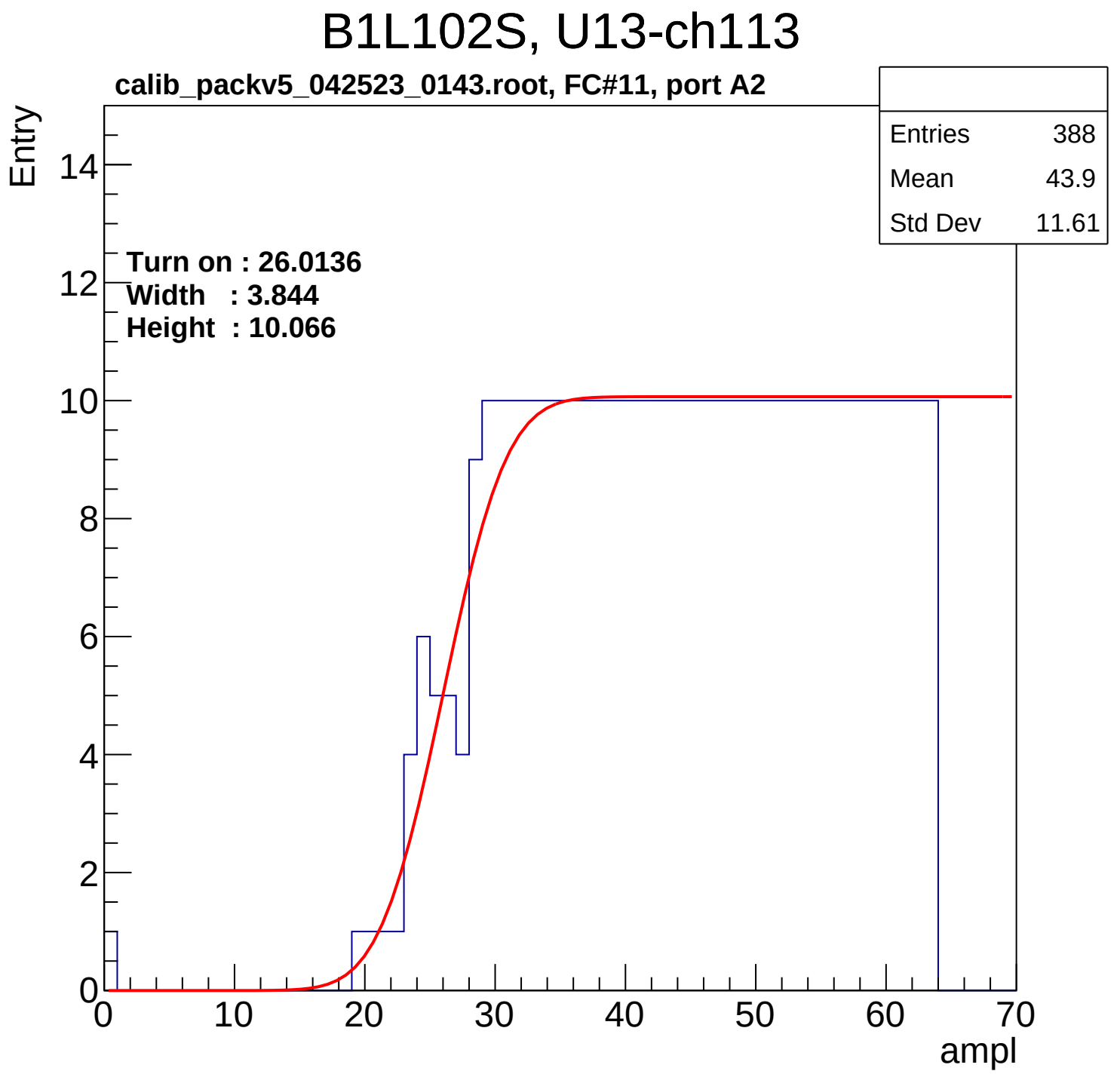
B1L102S, U13-ch113
calib_packv5_042523_0143.root, FC#11, port A2
Entries 388
Mean 43.9
Std Dev 11.61
Turn on : 26.0136
Width : 3.844
Height : 10.066
Entry
ampl
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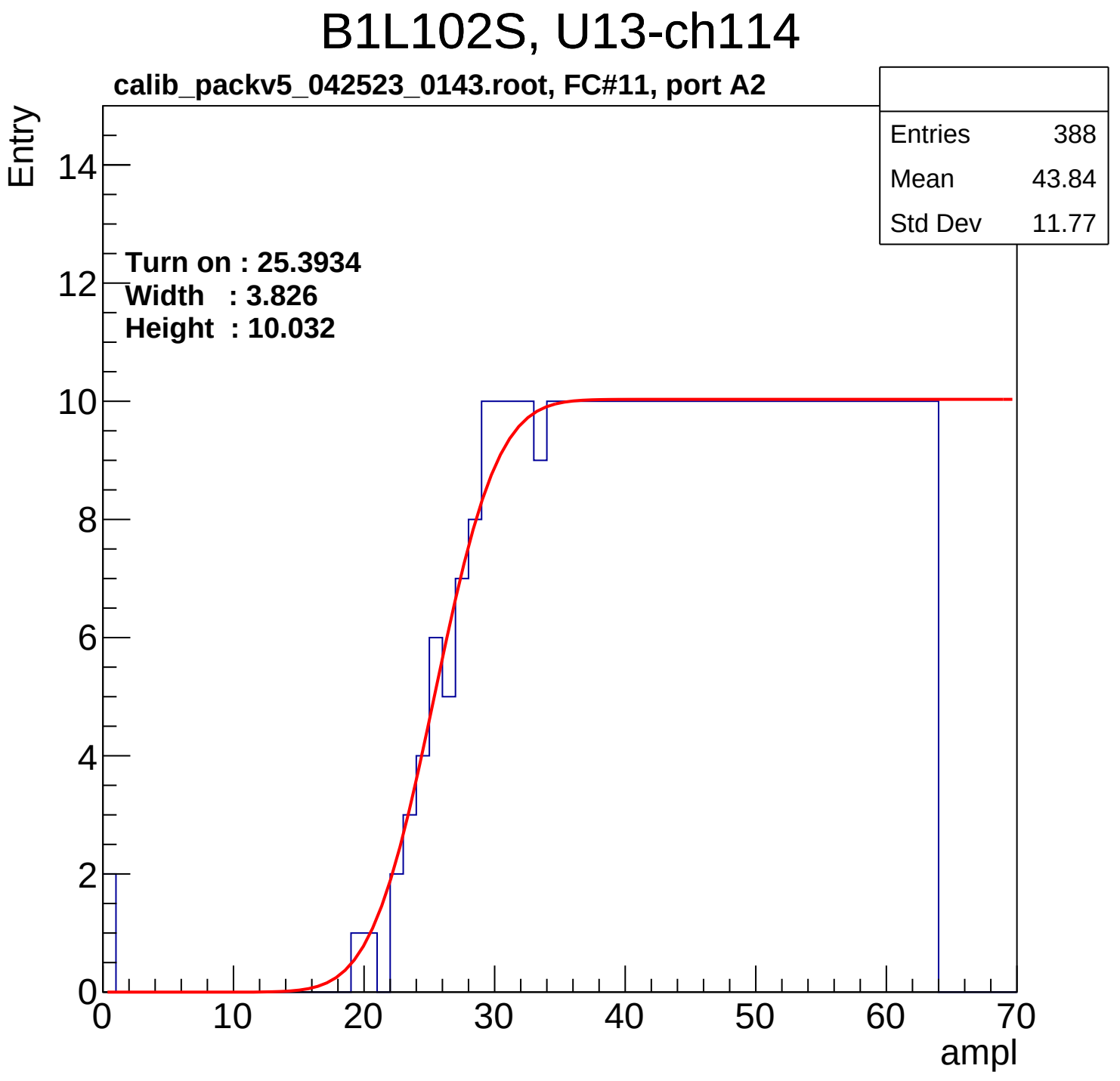
B1L102S, U13-ch114
calib_packv5_042523_0143.root, FC#11, port A2
Entries 388
Mean 43.84
Std Dev 11.77
Turn on : 25.3934
Width : 3.826
Height : 10.032
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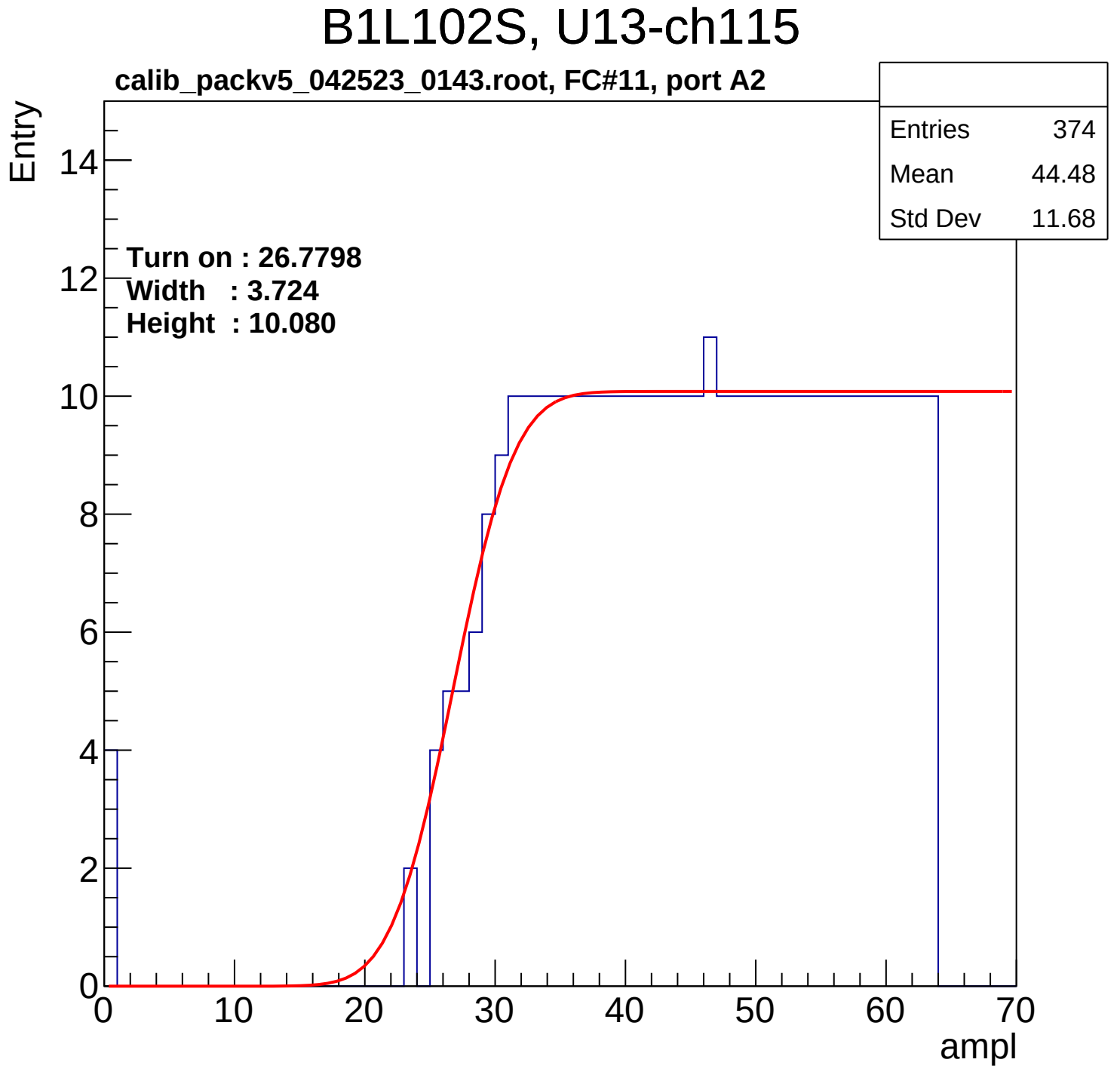
B1L102S, U13-ch115
calib_packv5_042523_0143.root, FC#11, port A2
Entries 374
Mean 44.48
Std Dev 11.68
Turn on : 26.7798
Width : 3.724
Height : 10.080
Entry
ampl
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4
6
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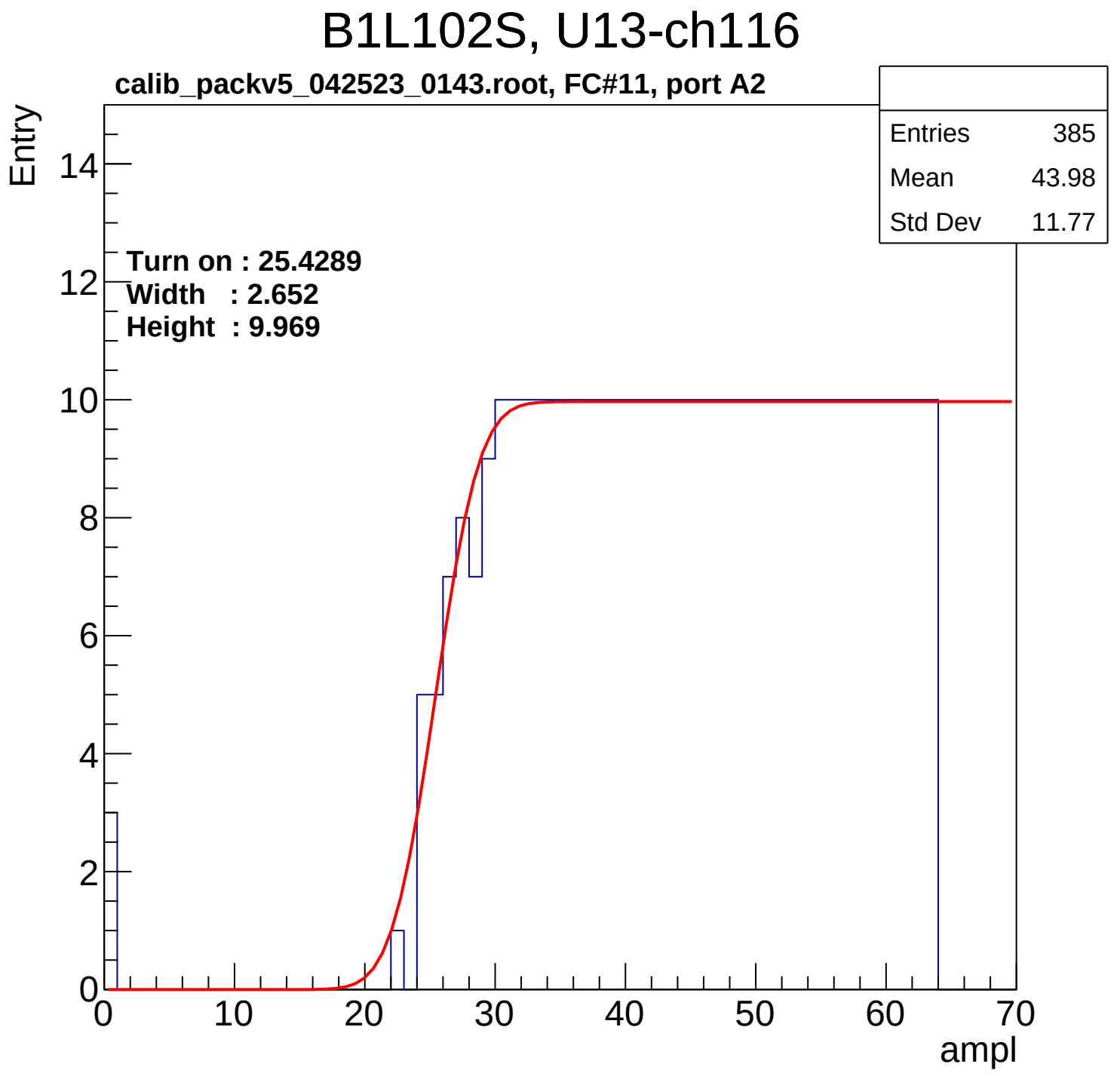
B1L102S, U13-ch116
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 43.98
Std Dev 11.77
Turn on : 25.4289
Width : 2.652
Height : 9.969
Entry
ampl
0
2
4
6
8
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12
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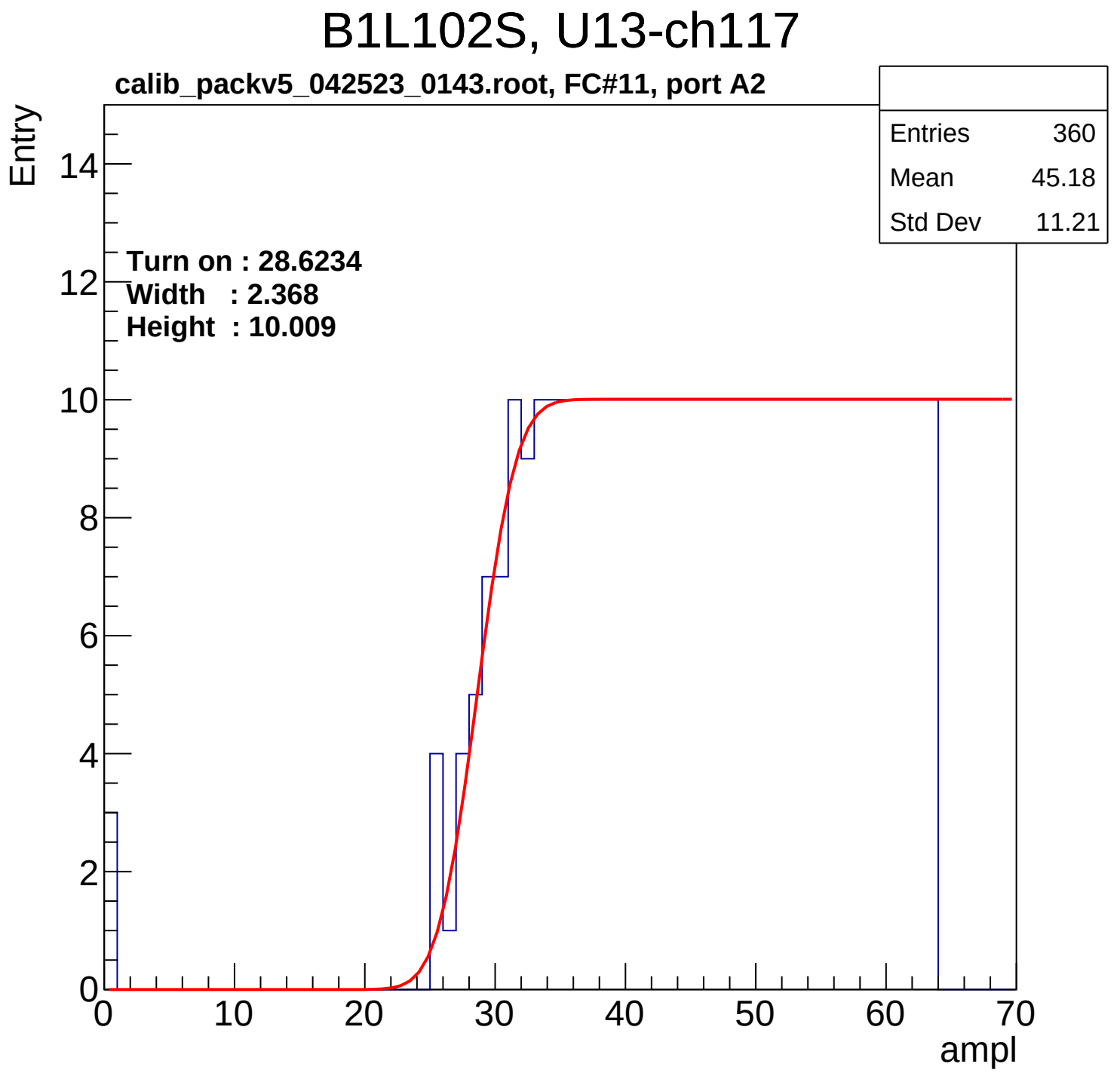
B1L102S, U13-ch117
calib_packv5_042523_0143.root, FC#11, port A2
Entries 360
Mean 45.18
Std Dev 11.21
Turn on : 28.6234
Width : 2.368
Height : 10.009
Entry
ampl
0
2
4
6
8
10
12
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0
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20
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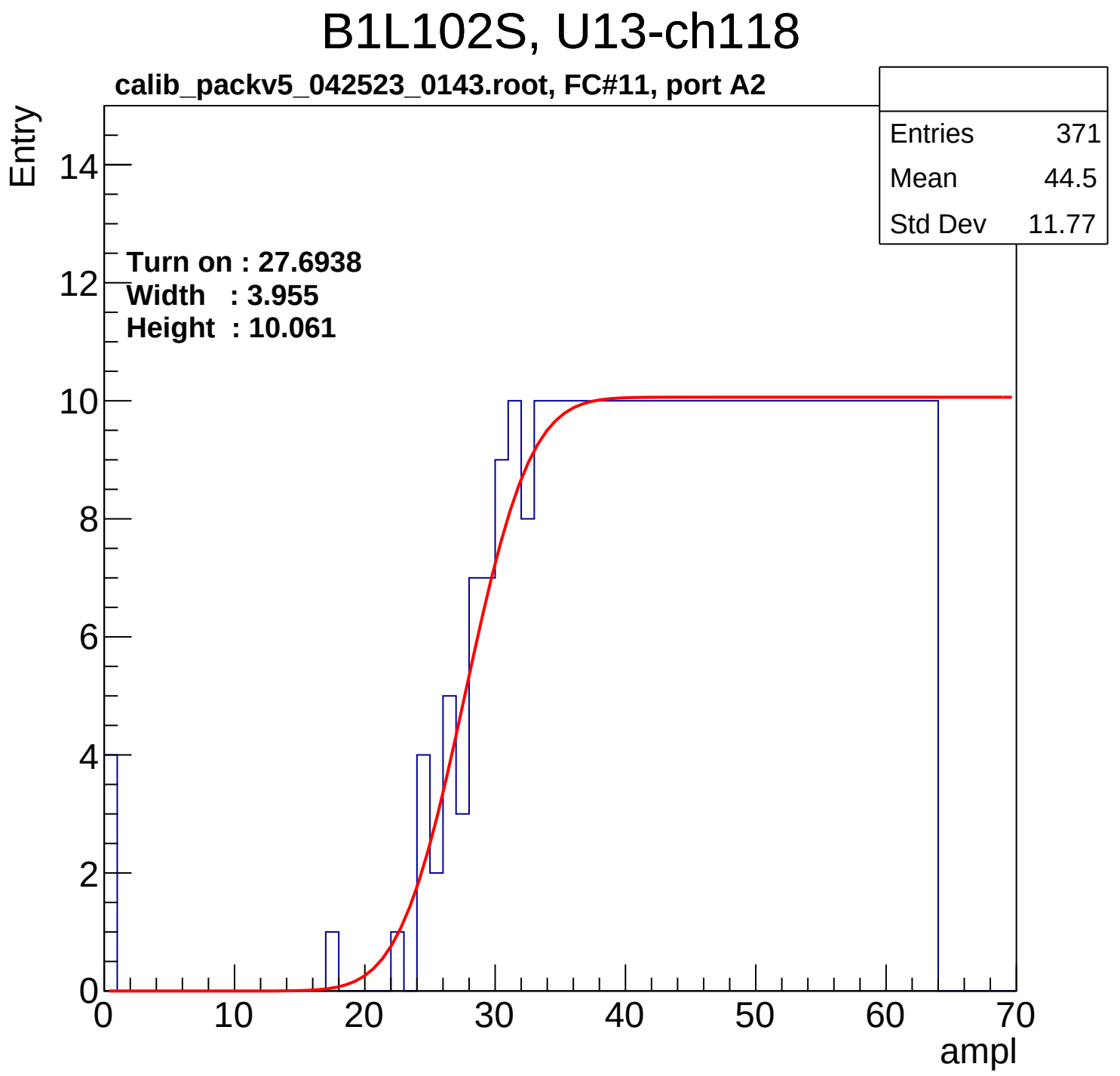
B1L102S, U13-ch118
calib_packv5_042523_0143.root, FC#11, port A2
Entries 371
Mean 44.5
Std Dev 11.77
Turn on : 27.6938
Width : 3.955
Height : 10.061
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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60
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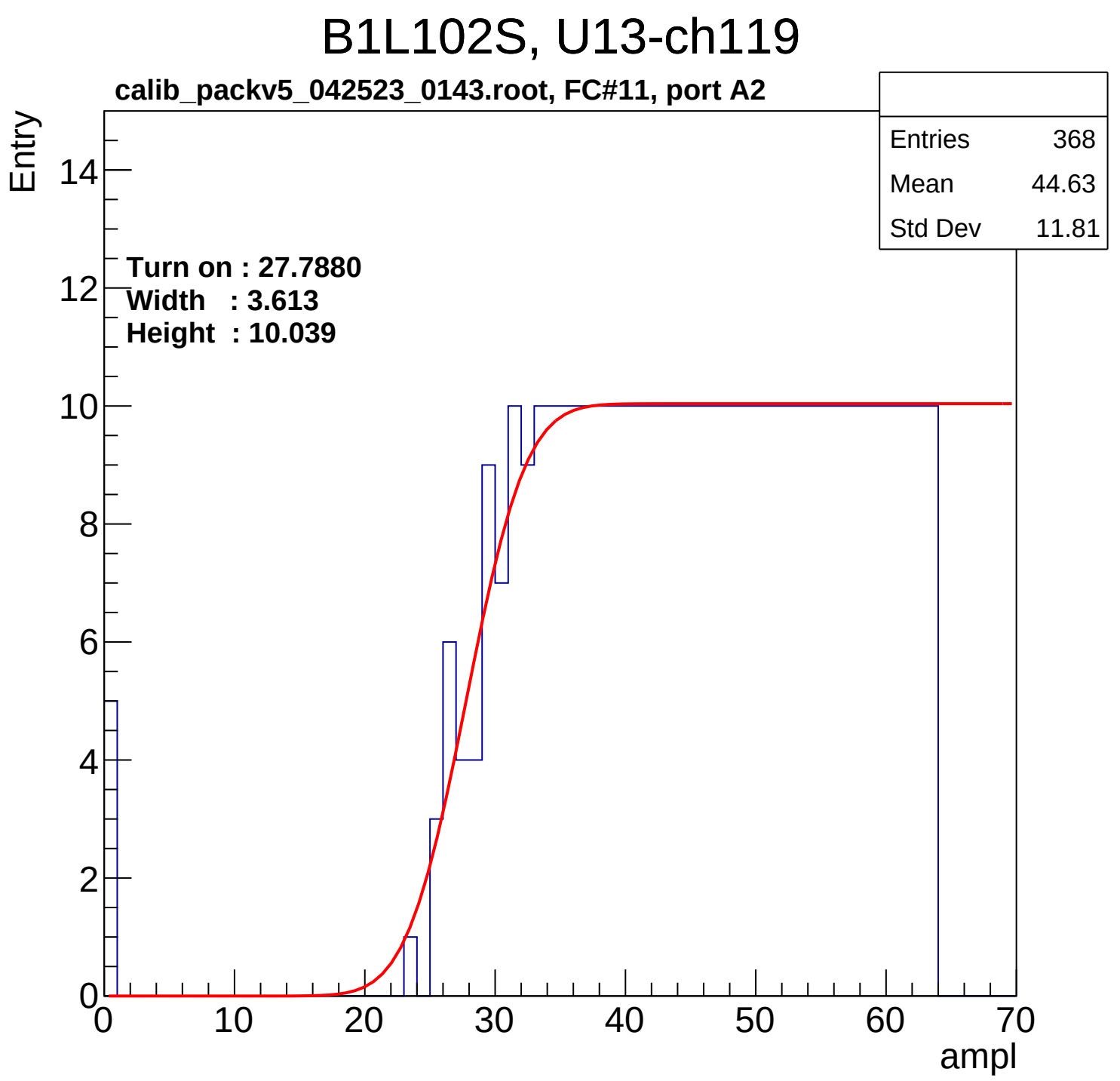
B1L102S, U13-ch119
calib_packv5_042523_0143.root, FC#11, port A2
Entries 368
Mean 44.63
Std Dev 11.81
Turn on : 27.7880
Width : 3.613
Height : 10.039
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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60
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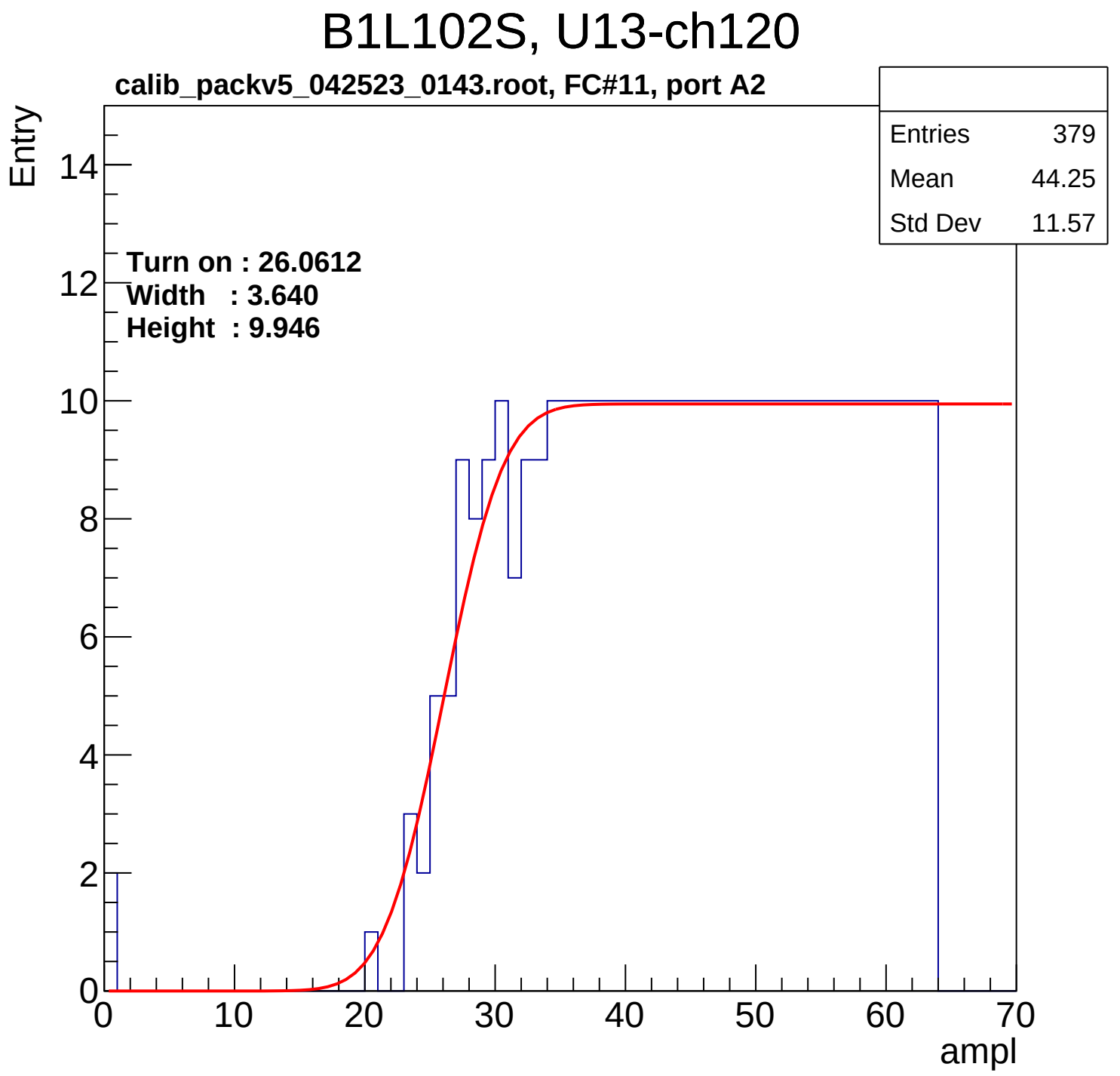
B1L102S, U13-ch120
calib_packv5_042523_0143.root, FC#11, port A2
Entries 379
Mean 44.25
Std Dev 11.57
Turn on : 26.0612
Width : 3.640
Height : 9.946
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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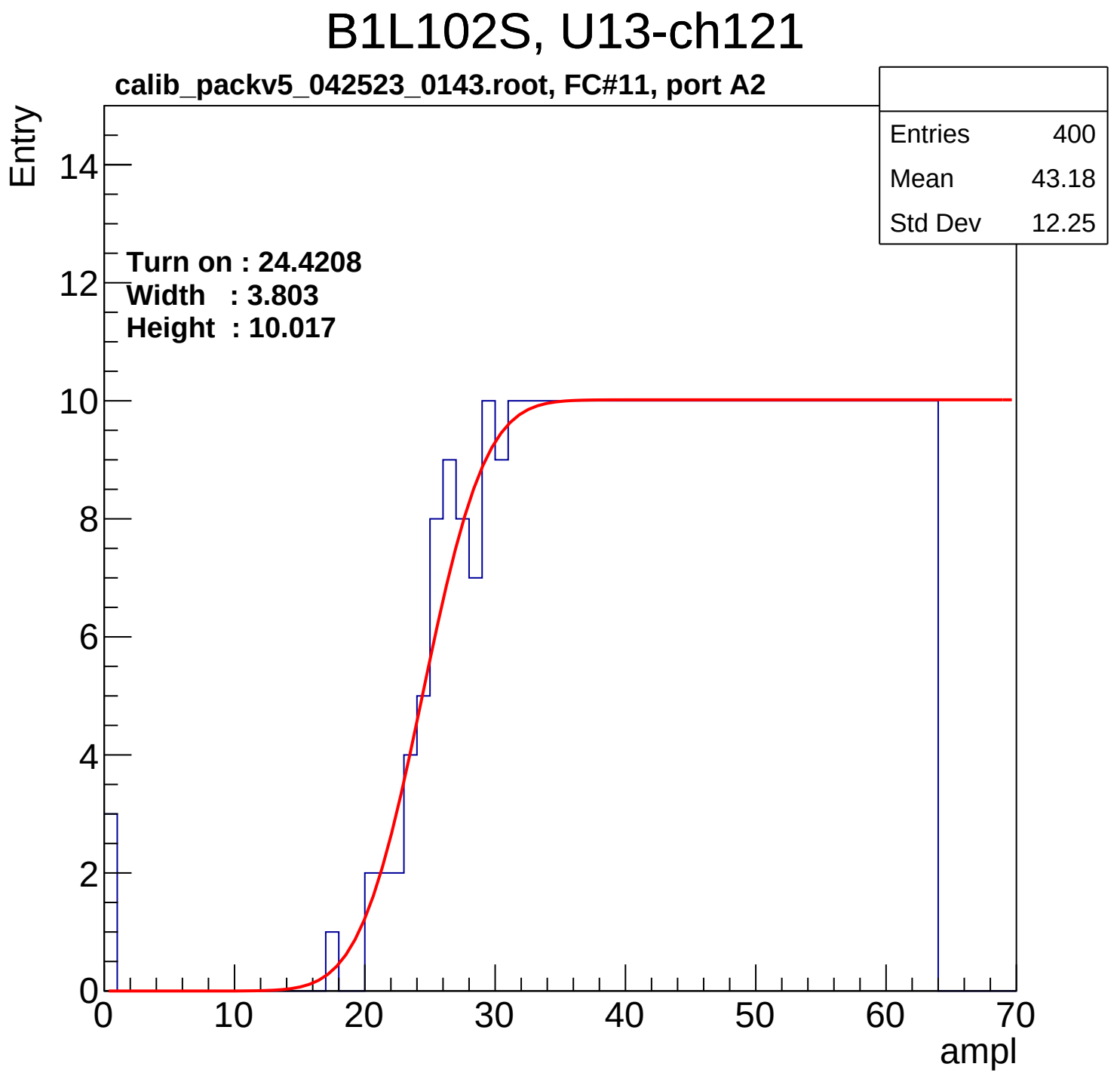
B1L102S, U13-ch121
calib_packv5_042523_0143.root, FC#11, port A2
Entries 400
Mean 43.18
Std Dev 12.25
Turn on : 24.4208
Width : 3.803
Height : 10.017
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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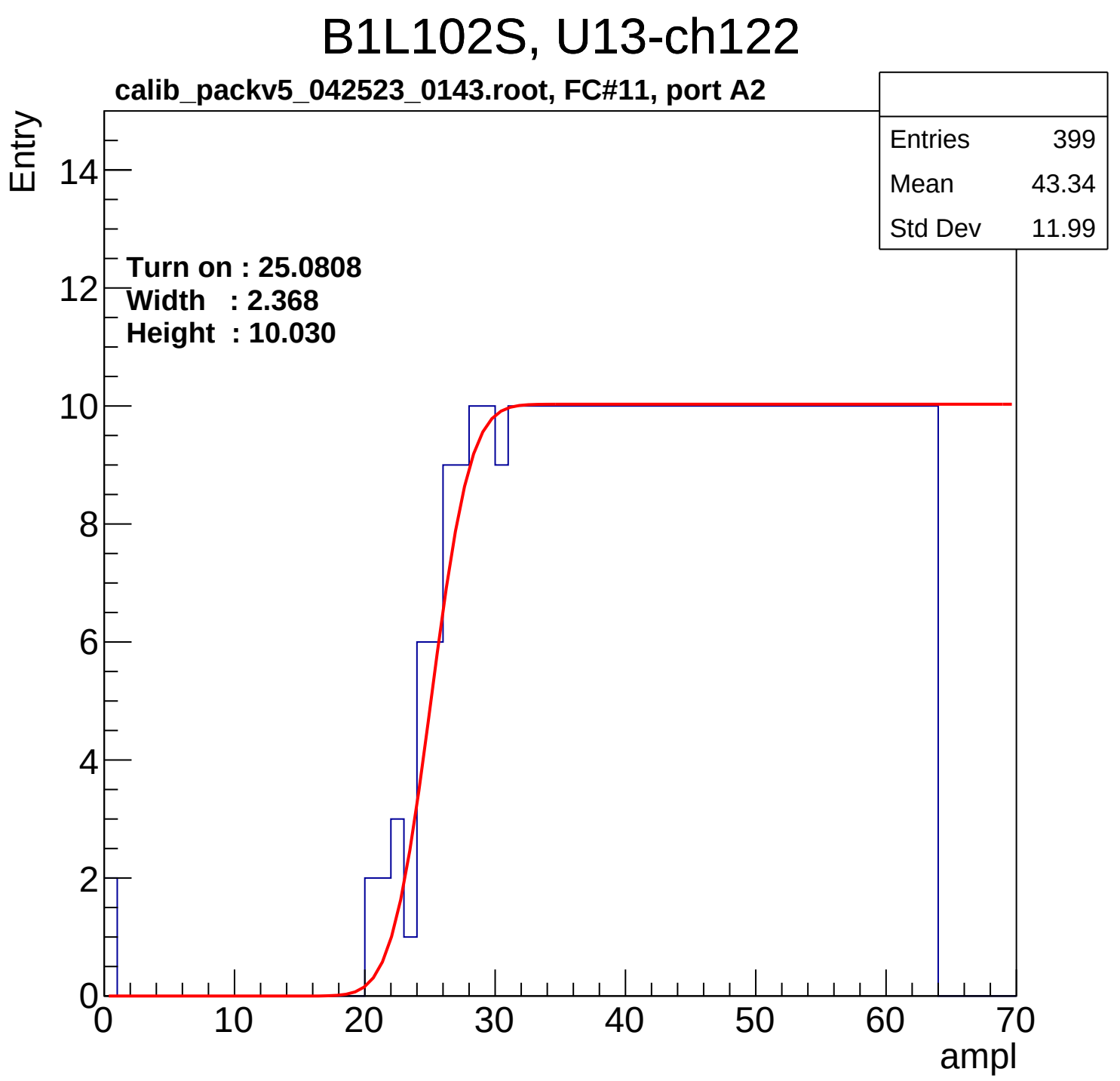
B1L102S, U13-ch122
calib_packv5_042523_0143.root, FC#11, port A2
Entries 399
Mean 43.34
Std Dev 11.99
Turn on : 25.0808
Width : 2.368
Height : 10.030
Entry
ampl
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4
6
8
10
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0
10
20
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40
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60
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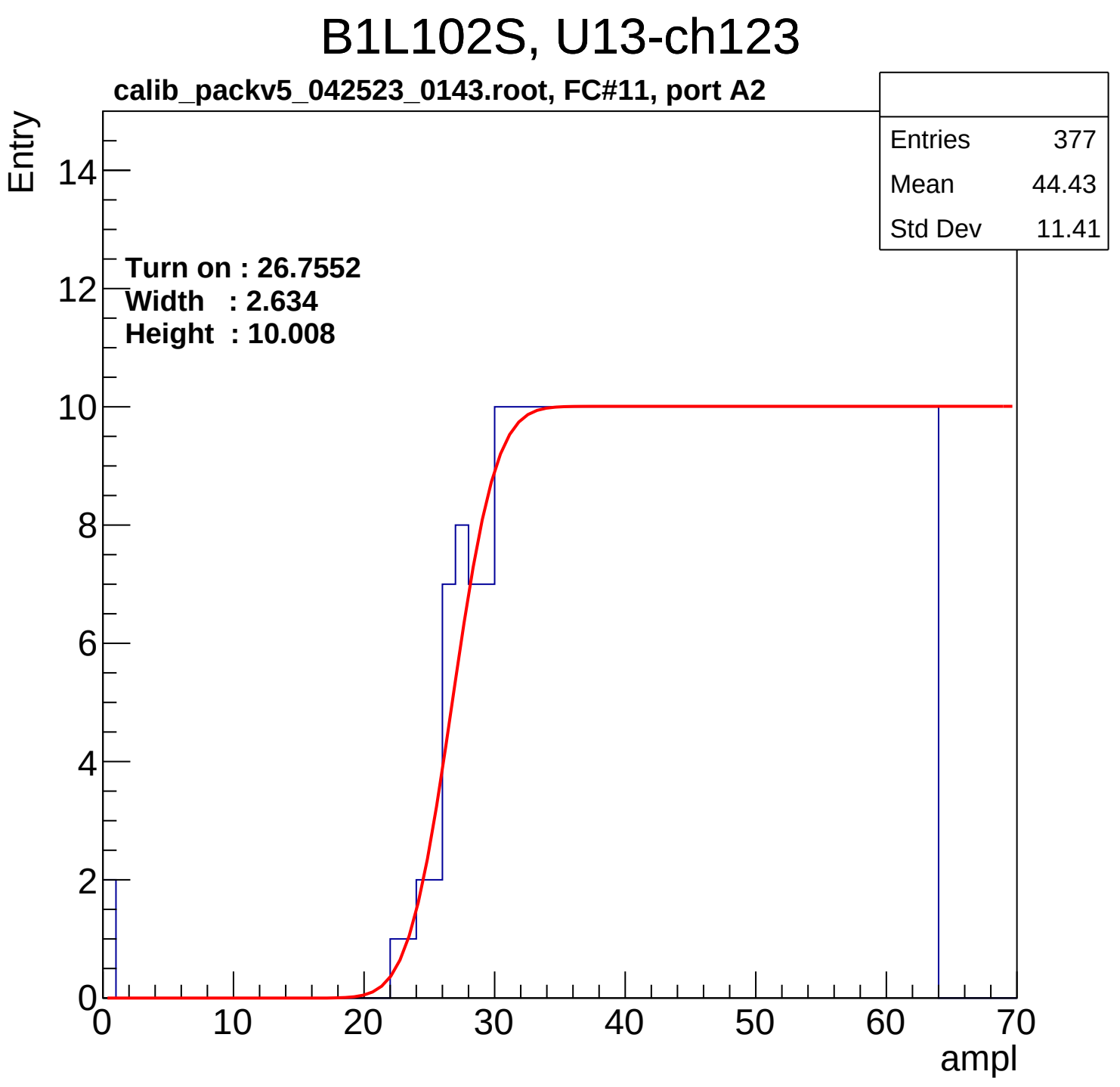
B1L102S, U13-ch123
calib_packv5_042523_0143.root, FC#11, port A2
Entries 377
Mean 44.43
Std Dev 11.41
Turn on : 26.7552
Width : 2.634
Height : 10.008
Entry
ampl
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4
6
8
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0
10
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40
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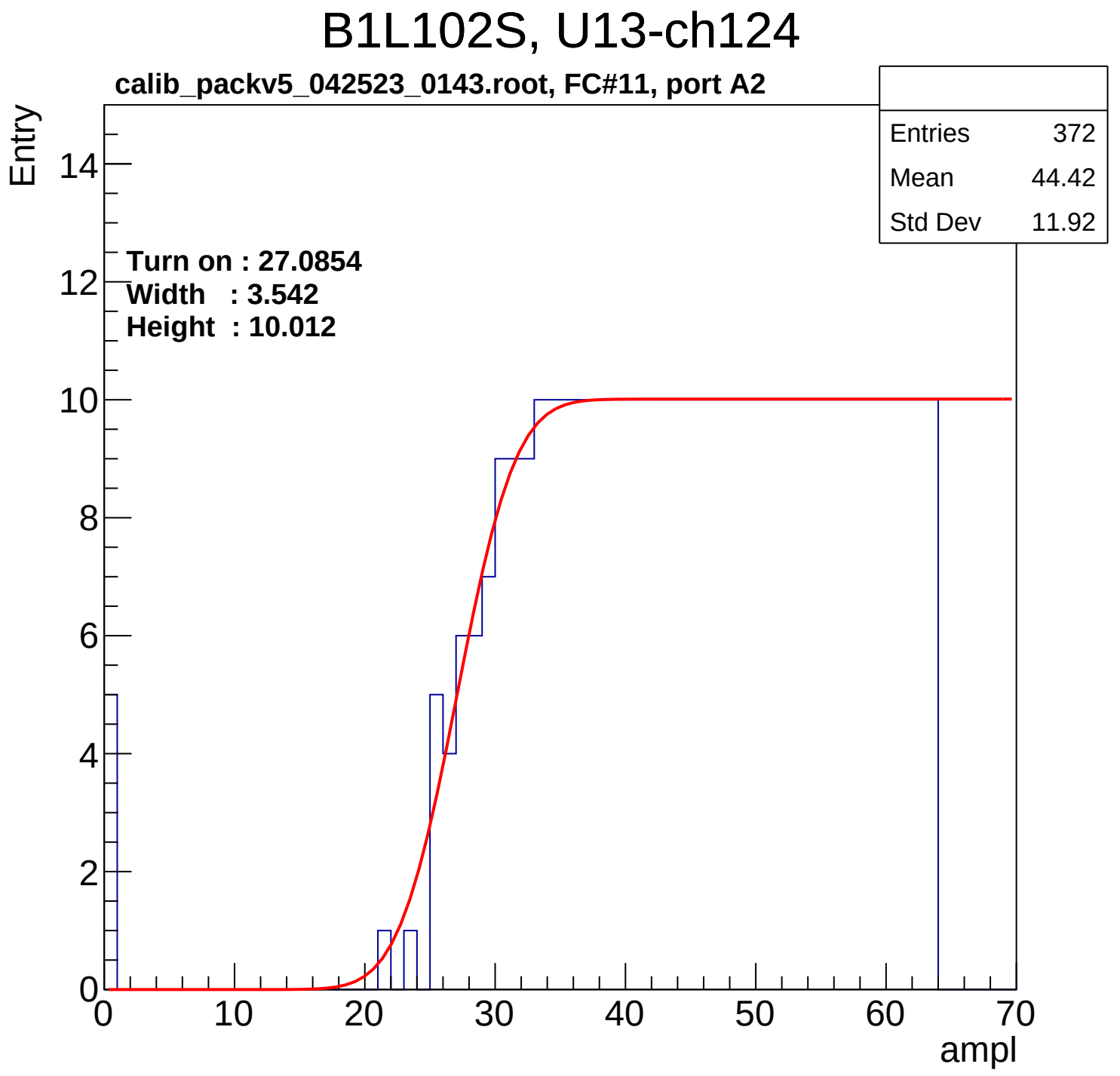
60
70


B1L102S, U13-ch124
calib_packv5_042523_0143.root, FC#11, port A2
Entries 372
Mean 44.42
Std Dev 11.92
Turn on : 27.0854
Width : 3.542
Height : 10.012
Entry
ampl
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2
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6
8
10
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20
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40
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60
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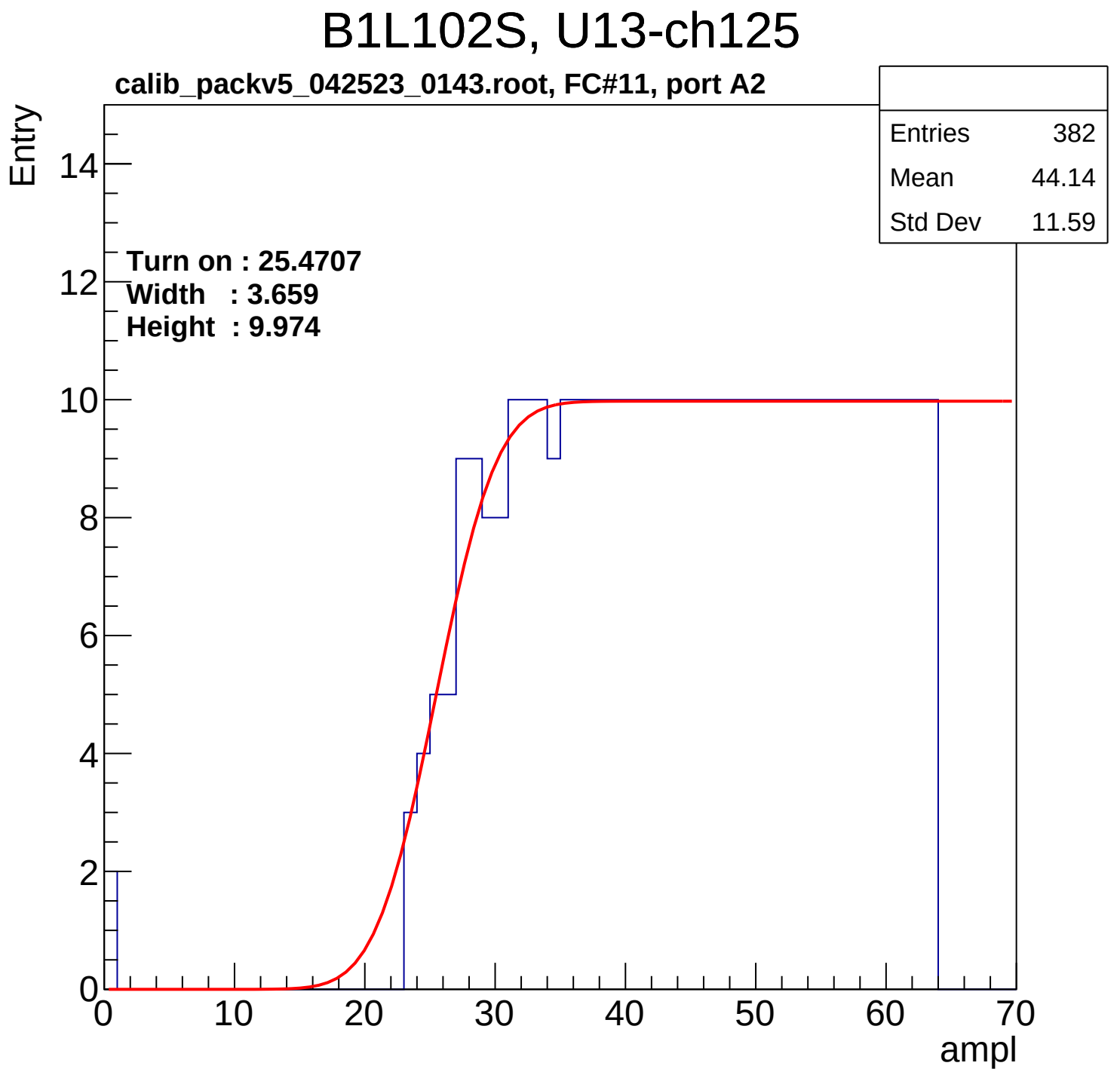
B1L102S, U13-ch125
calib_packv5_042523_0143.root, FC#11, port A2
Entries 382
Mean 44.14
Std Dev 11.59
Turn on : 25.4707
Width : 3.659
Height : 9.974
Entry
ampl
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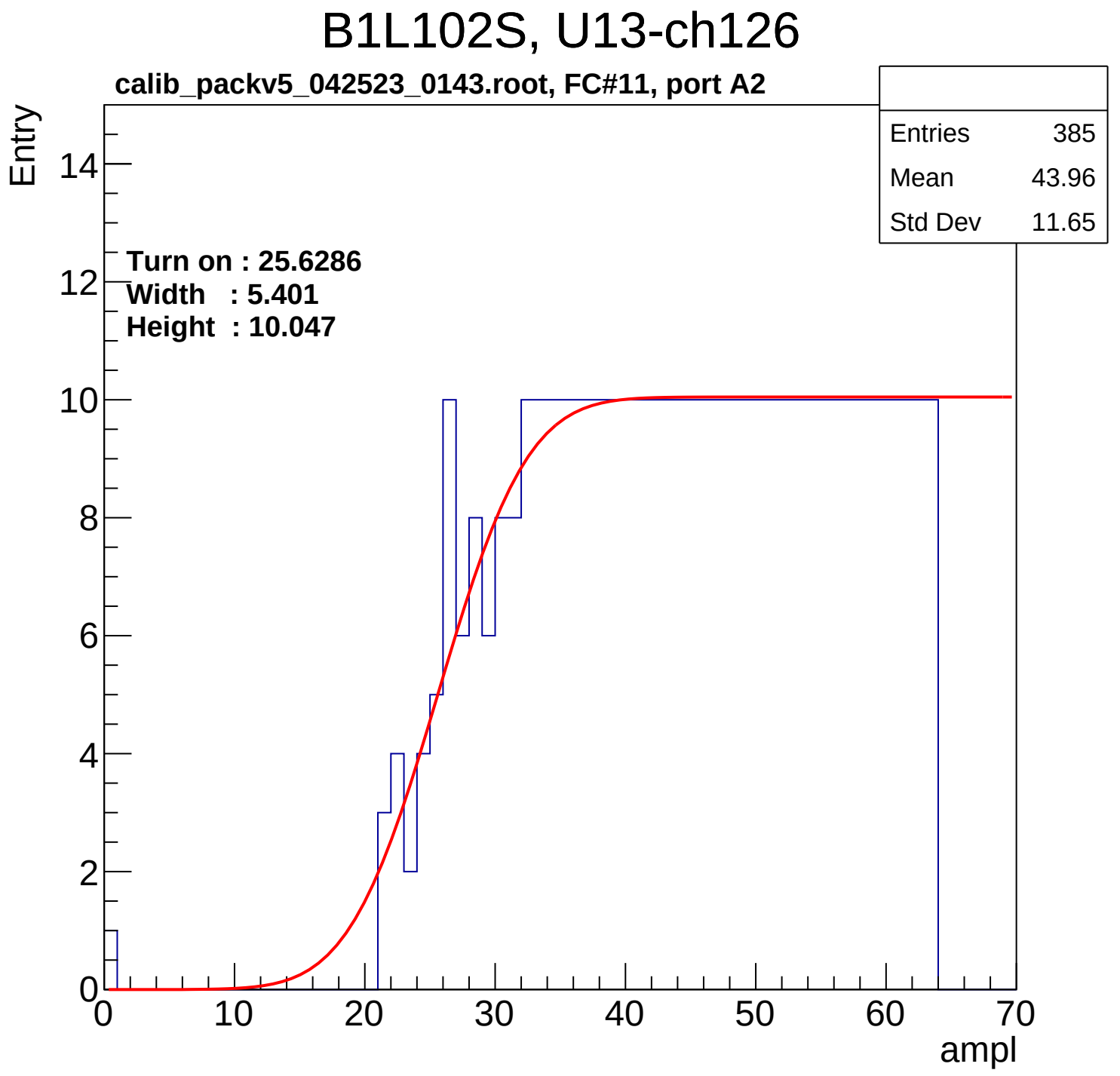
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L102S, U13-ch126
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 43.96
Std Dev 11.65
Turn on : 25.6286
Width : 5.401
Height : 10.047
Entry
ampl
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4
6
8
10
12
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0
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20
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60
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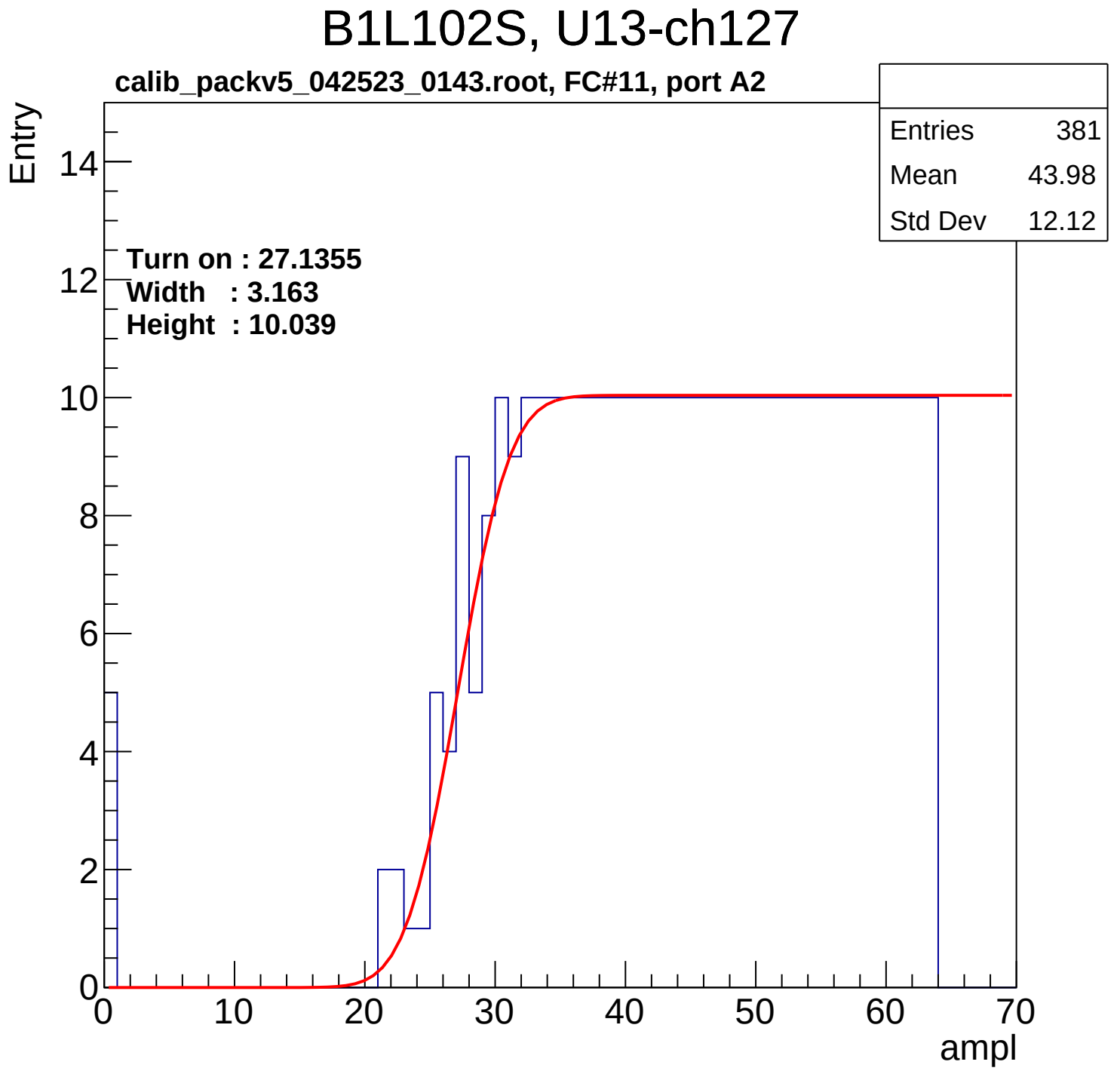
B1L102S, U13-ch127
calib_packv5_042523_0143.root, FC#11, port A2
Entries 381
Mean 43.98
Std Dev 12.12
Turn on : 27.1355
Width : 3.163
Height : 10.039
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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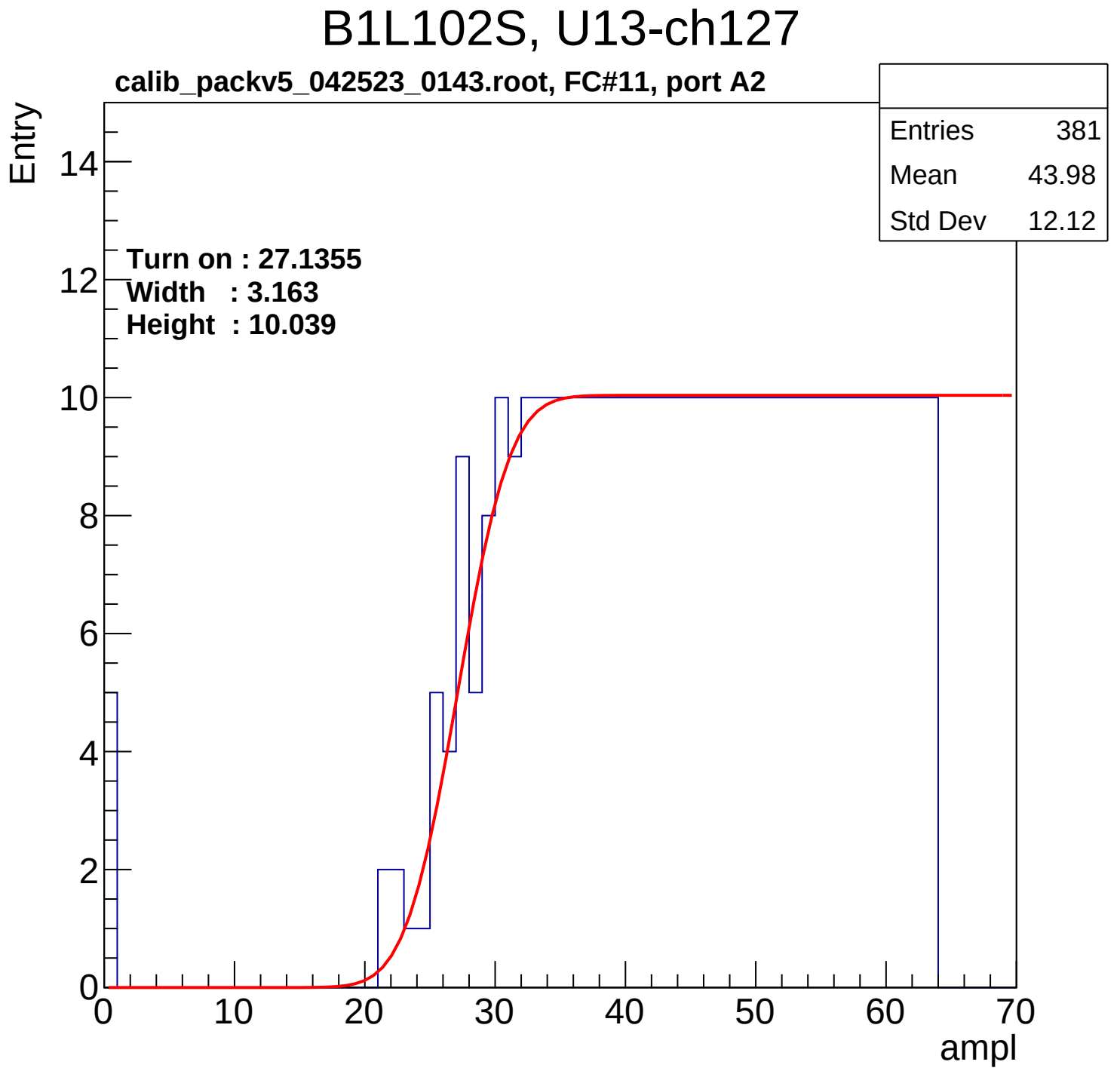
60
70


B1L102S, U13-ch127
calib_packv5_042523_0143.root, FC#11, port A2
Entries 381
Mean 43.98
Std Dev 12.12
Turn on : 27.1355
Width : 3.163
Height : 10.039
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70