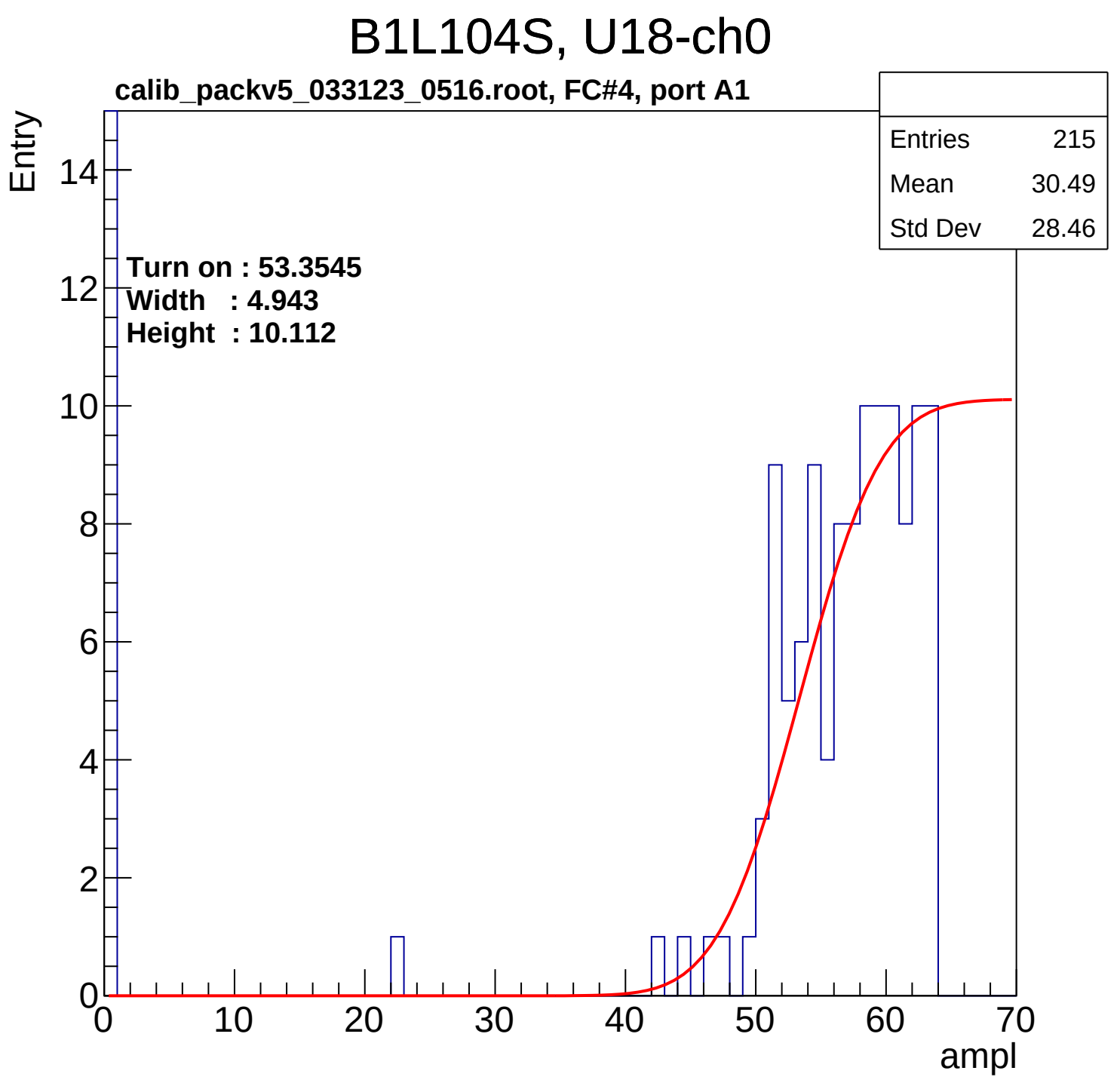
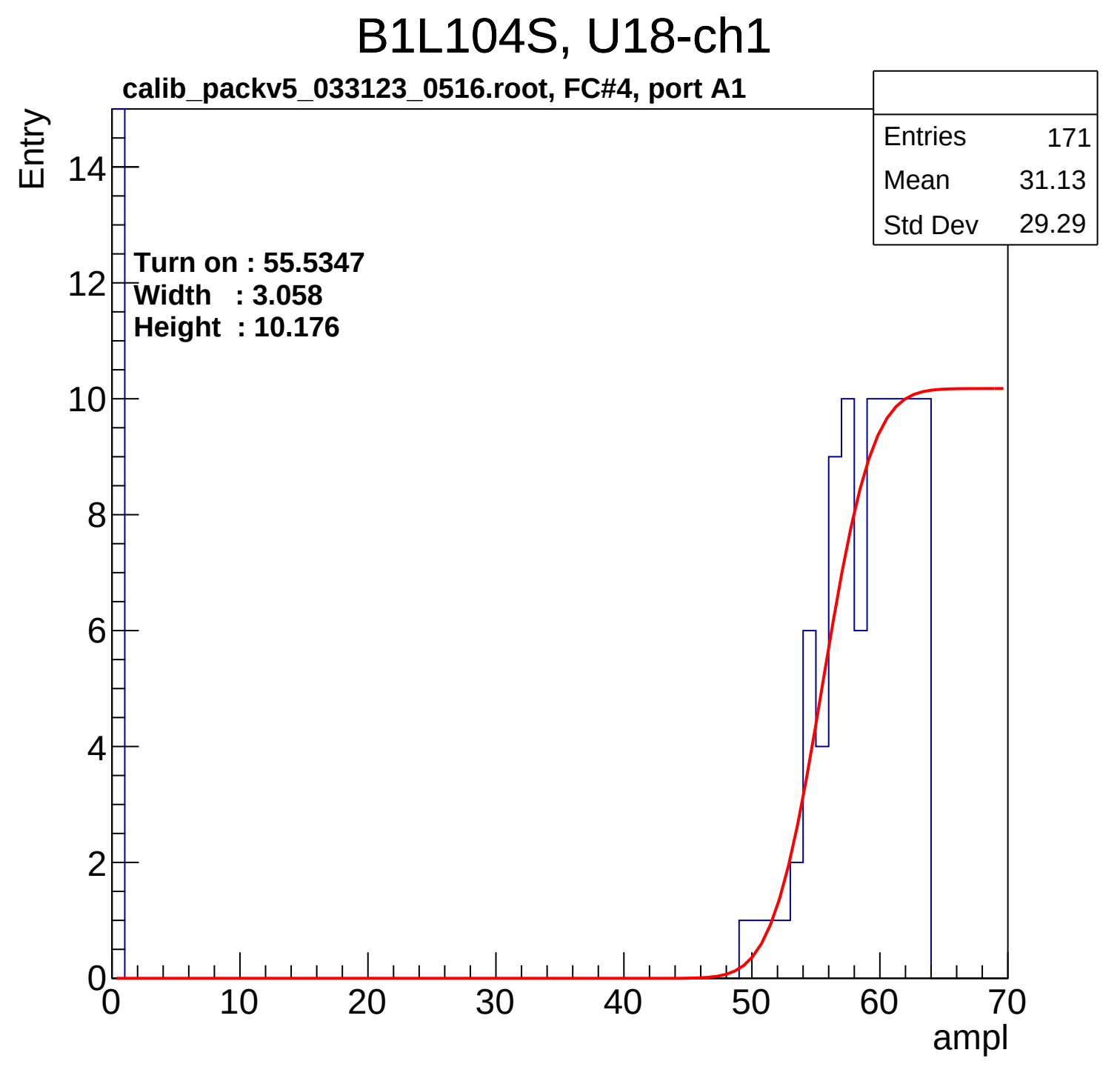
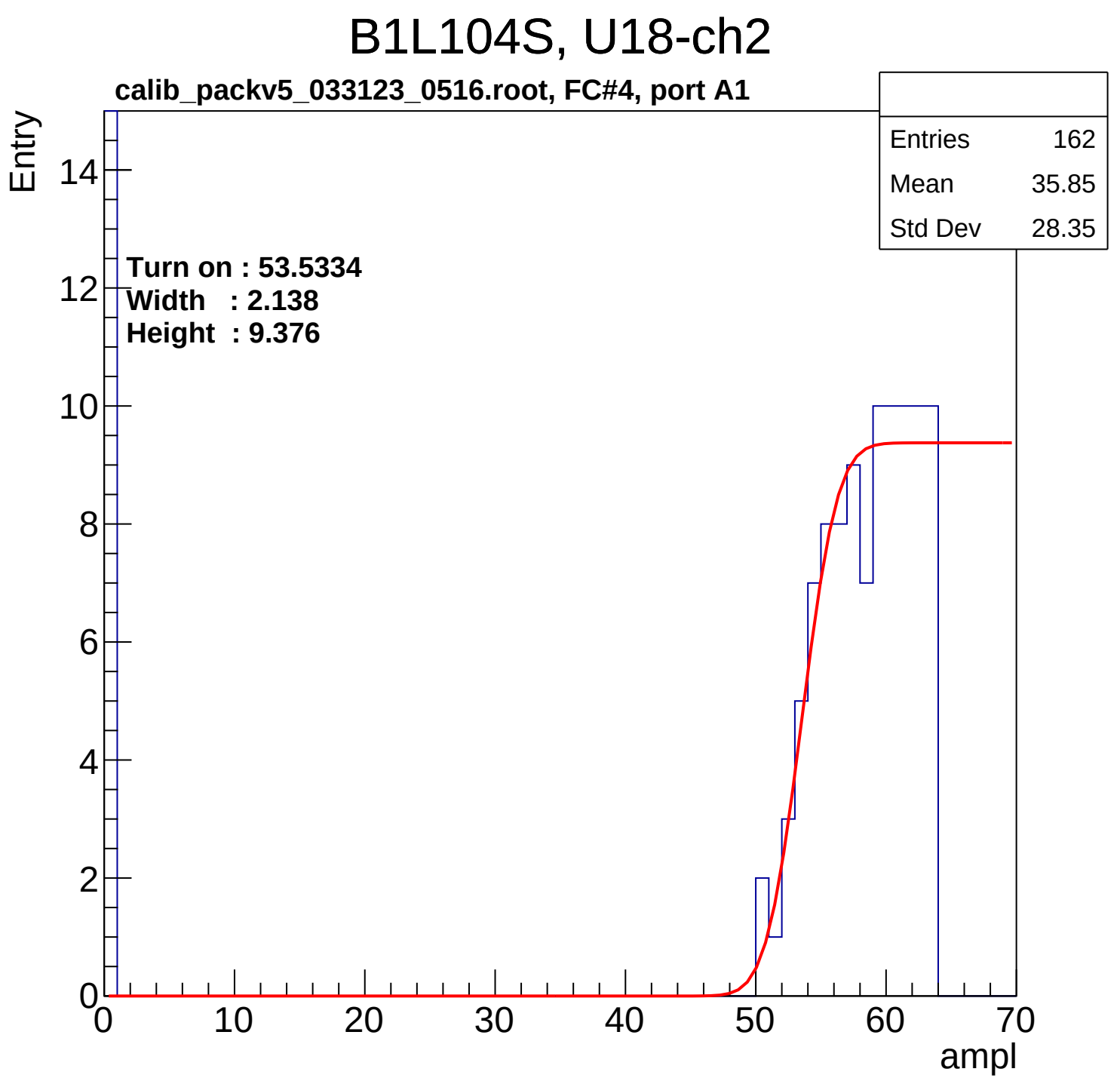
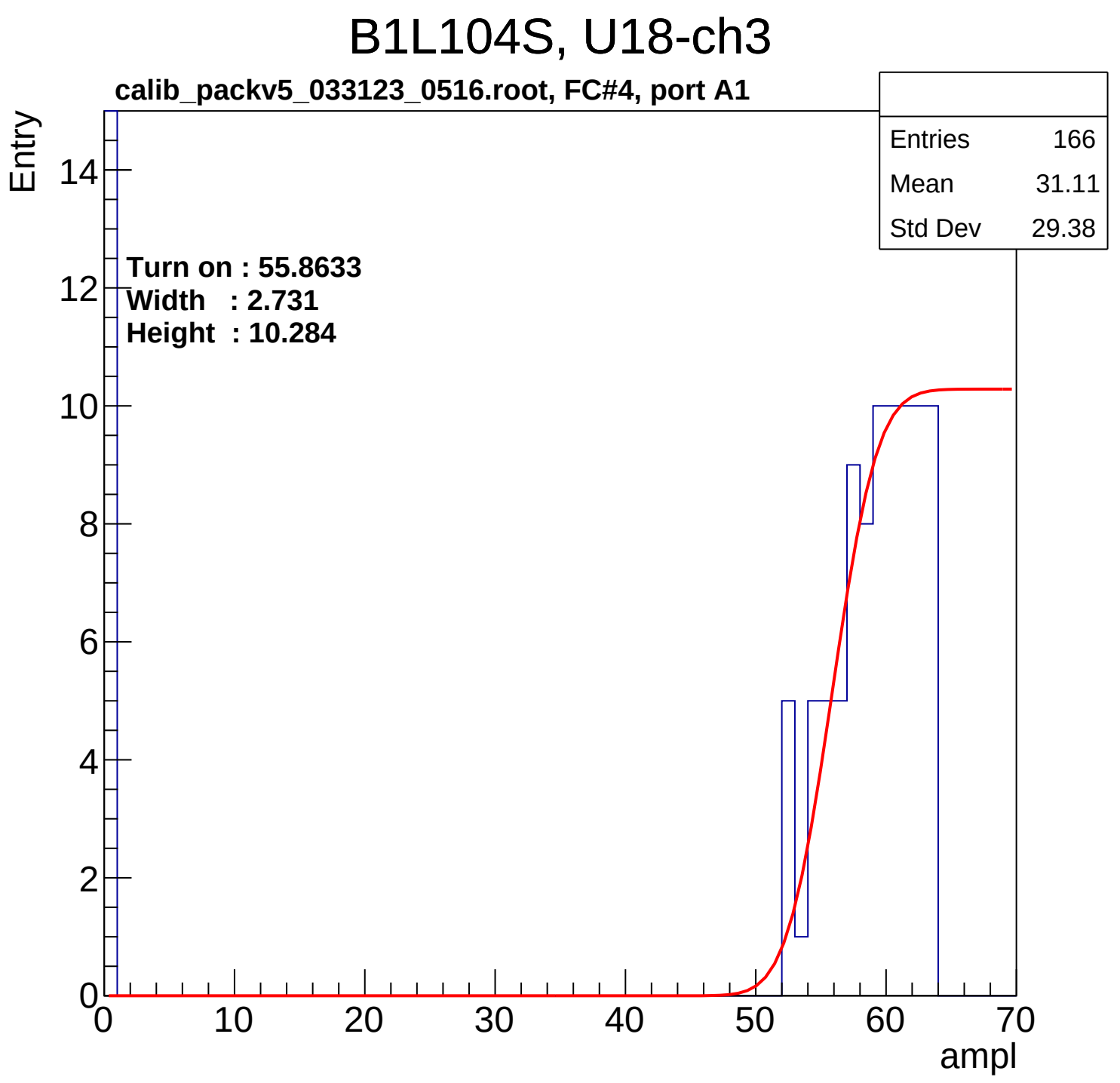
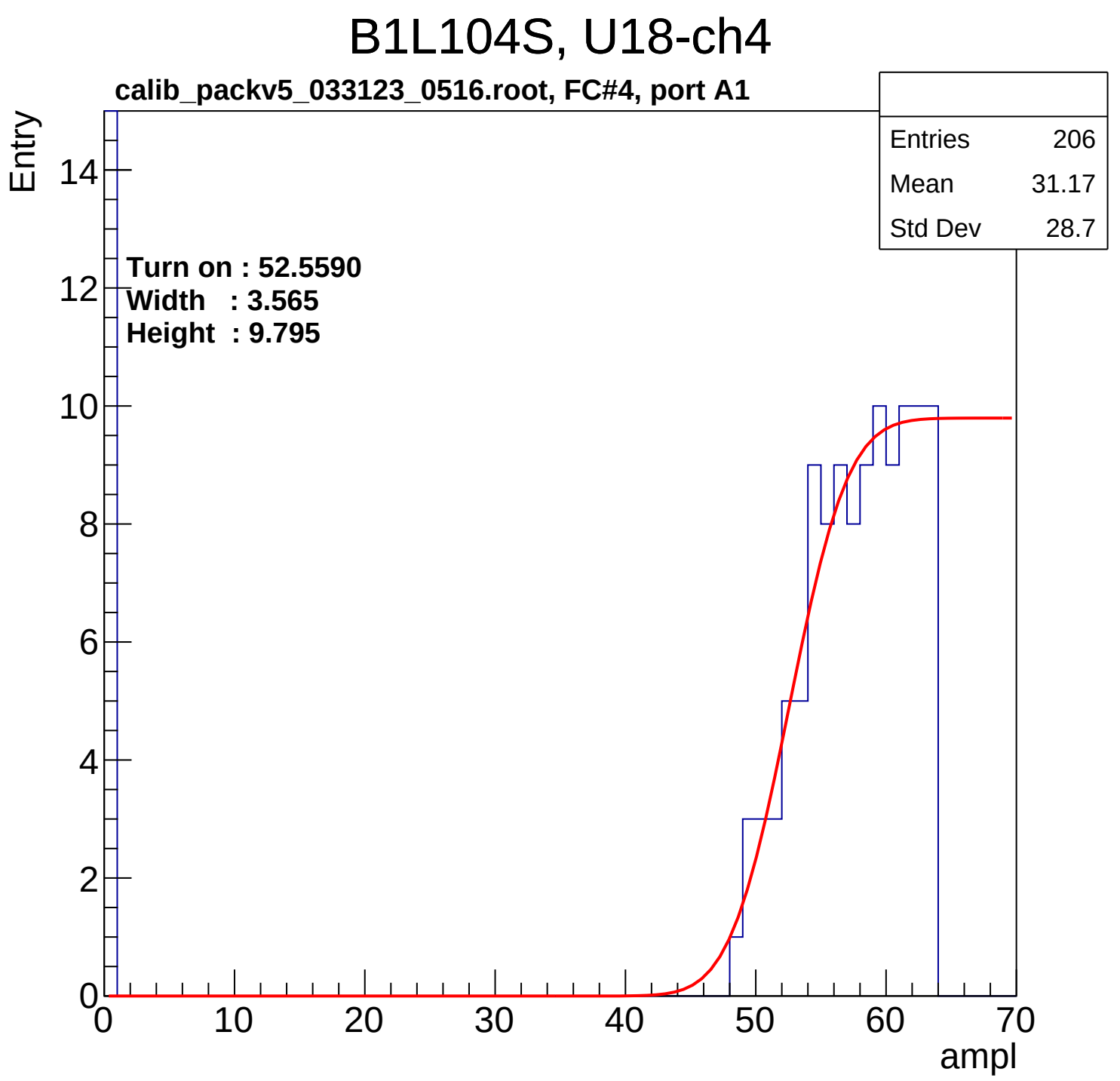
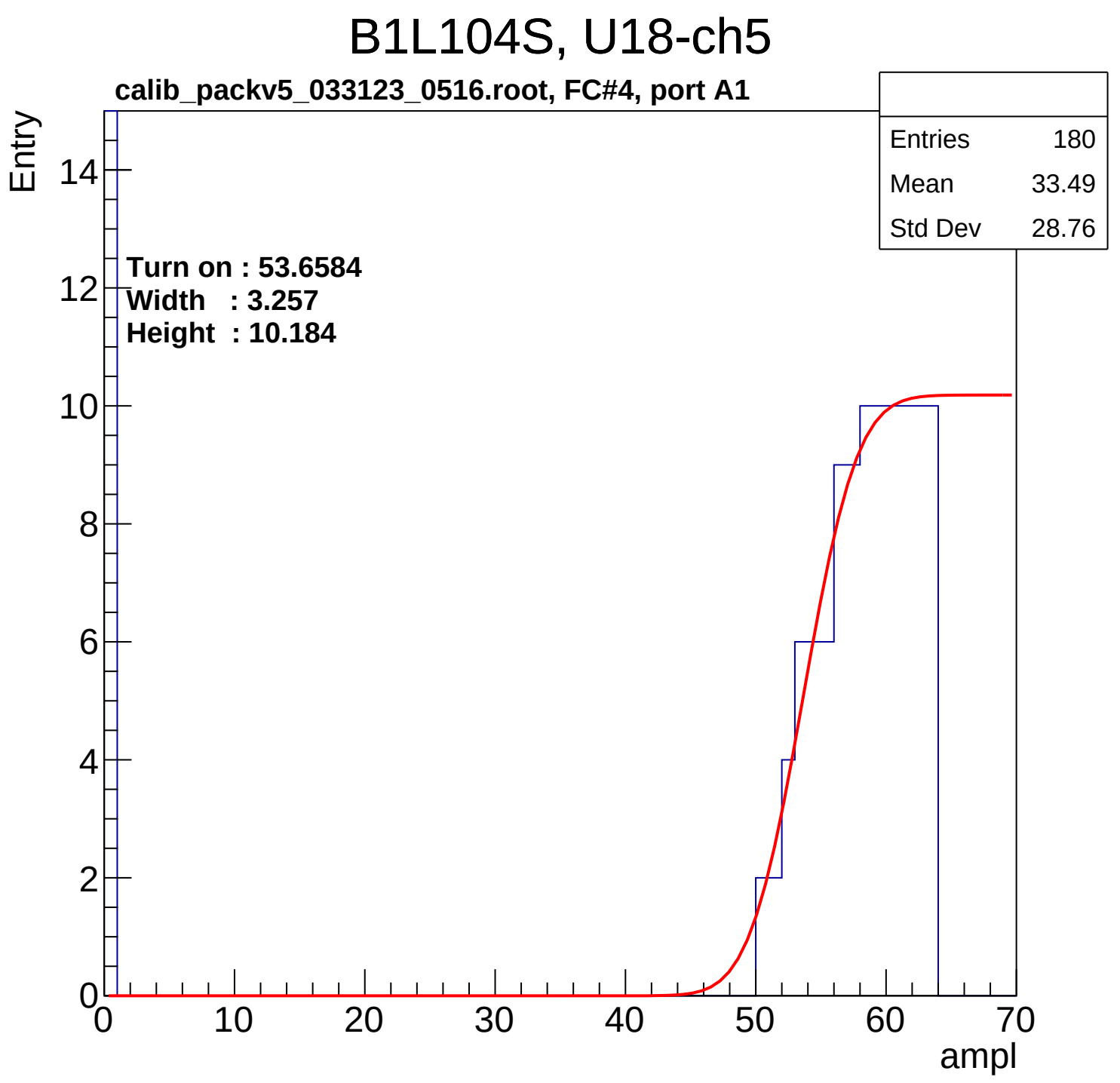

B1L104S, U18-ch0
calib_packv5_033123_0516.root, FC#4, port A1
Entries 215
Mean 30.49
Std Dev 28.46
Turn on : 53.3545
Width : 4.943
Height : 10.112
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

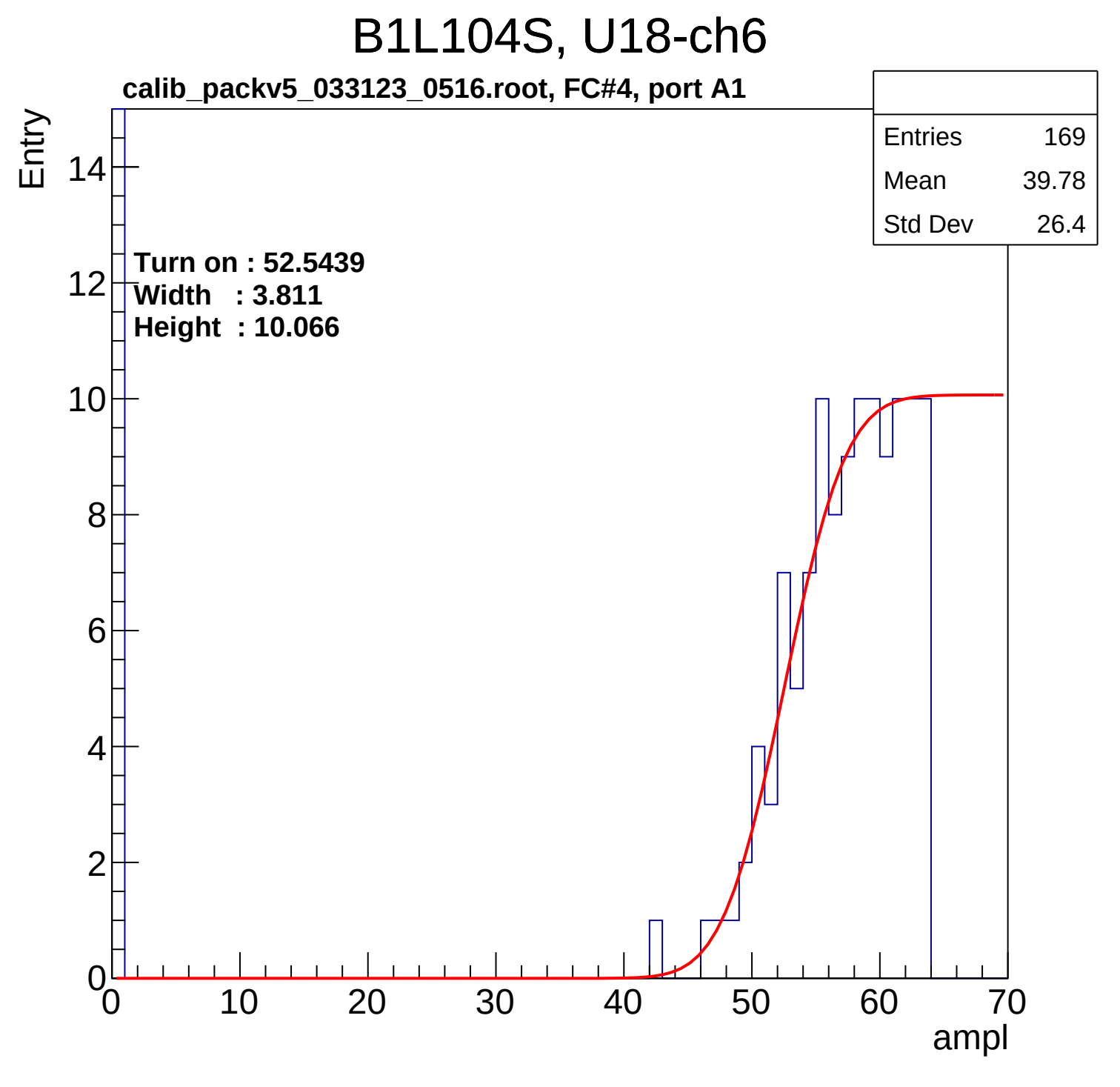

B1L104S, U18-ch1
calib_packv5_033123_0516.root, FC#4, port A1
Entries 171
Mean 31.13
Std Dev 29.29
Turn on : 55.5347
Width : 3.058
Height : 10.176
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

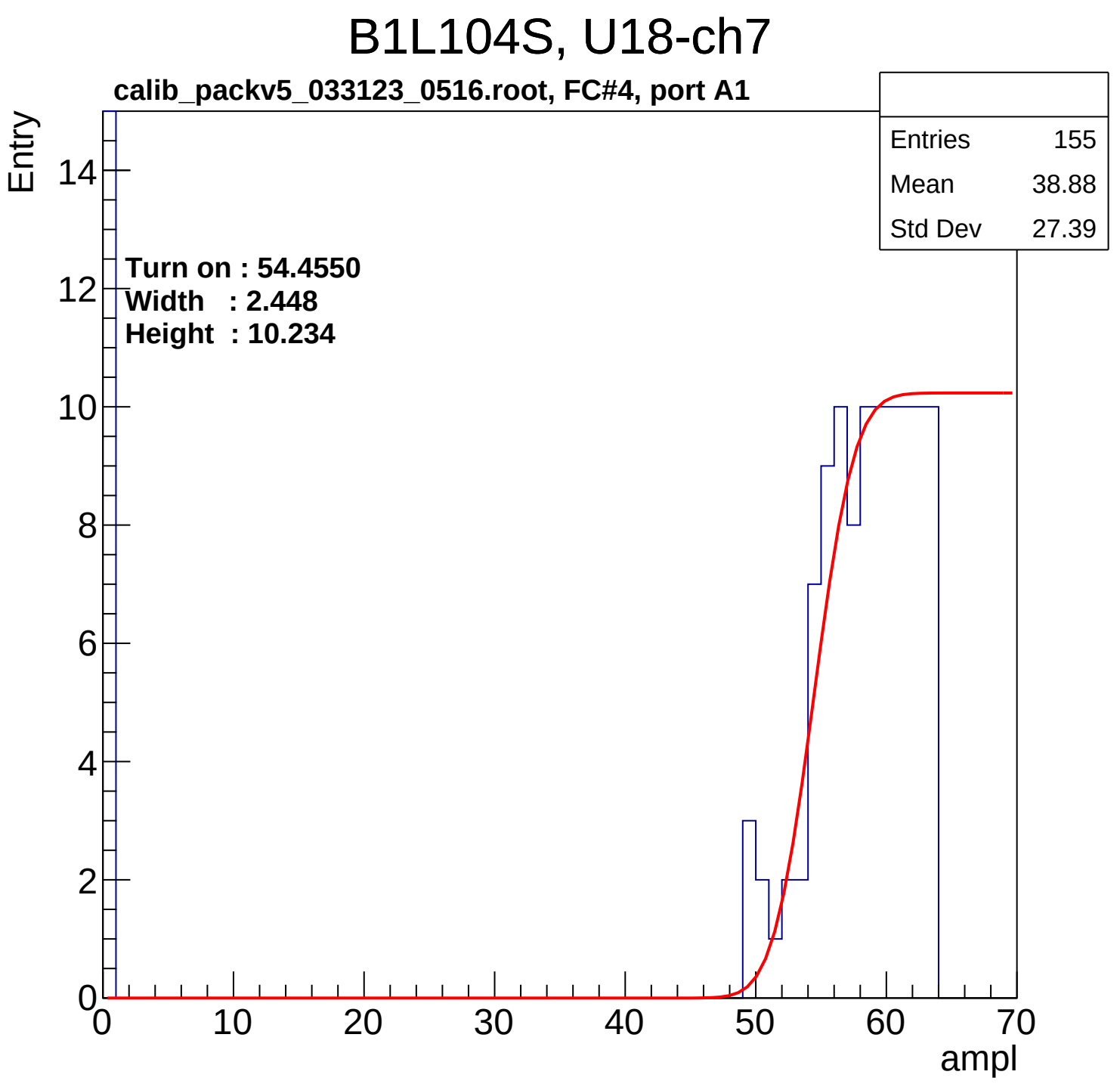

B1L104S, U18-ch2
calib_packv5_033123_0516.root, FC#4, port A1
Entries 162
Mean 35.85
Std Dev 28.35
Turn on : 53.5334
Width : 2.138
Height : 9.376
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

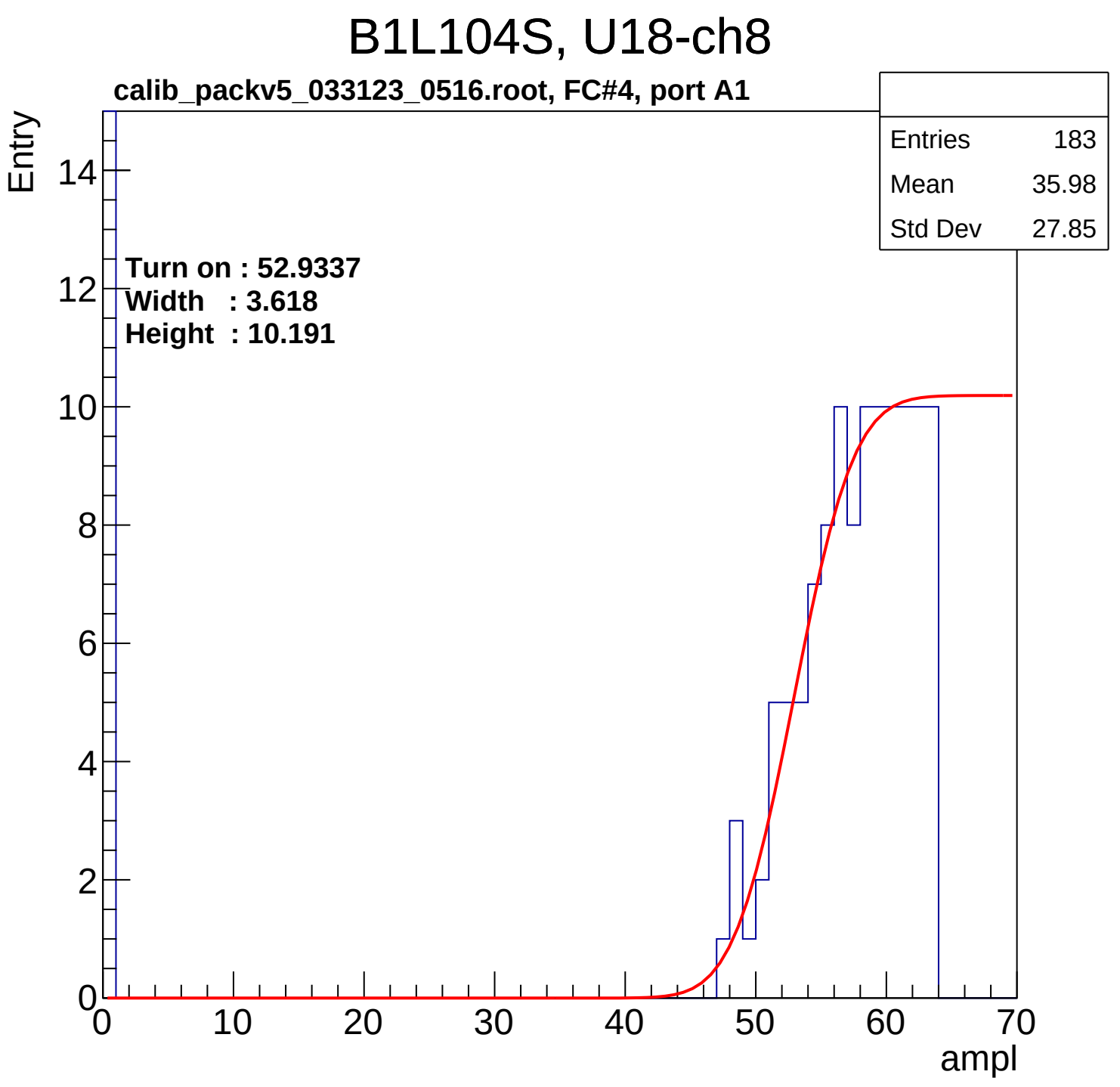

B1L104S, U18-ch3
calib_packv5_033123_0516.root, FC#4, port A1
Entries 166
Mean 31.11
Std Dev 29.38
Turn on : 55.8633
Width : 2.731
Height : 10.284
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

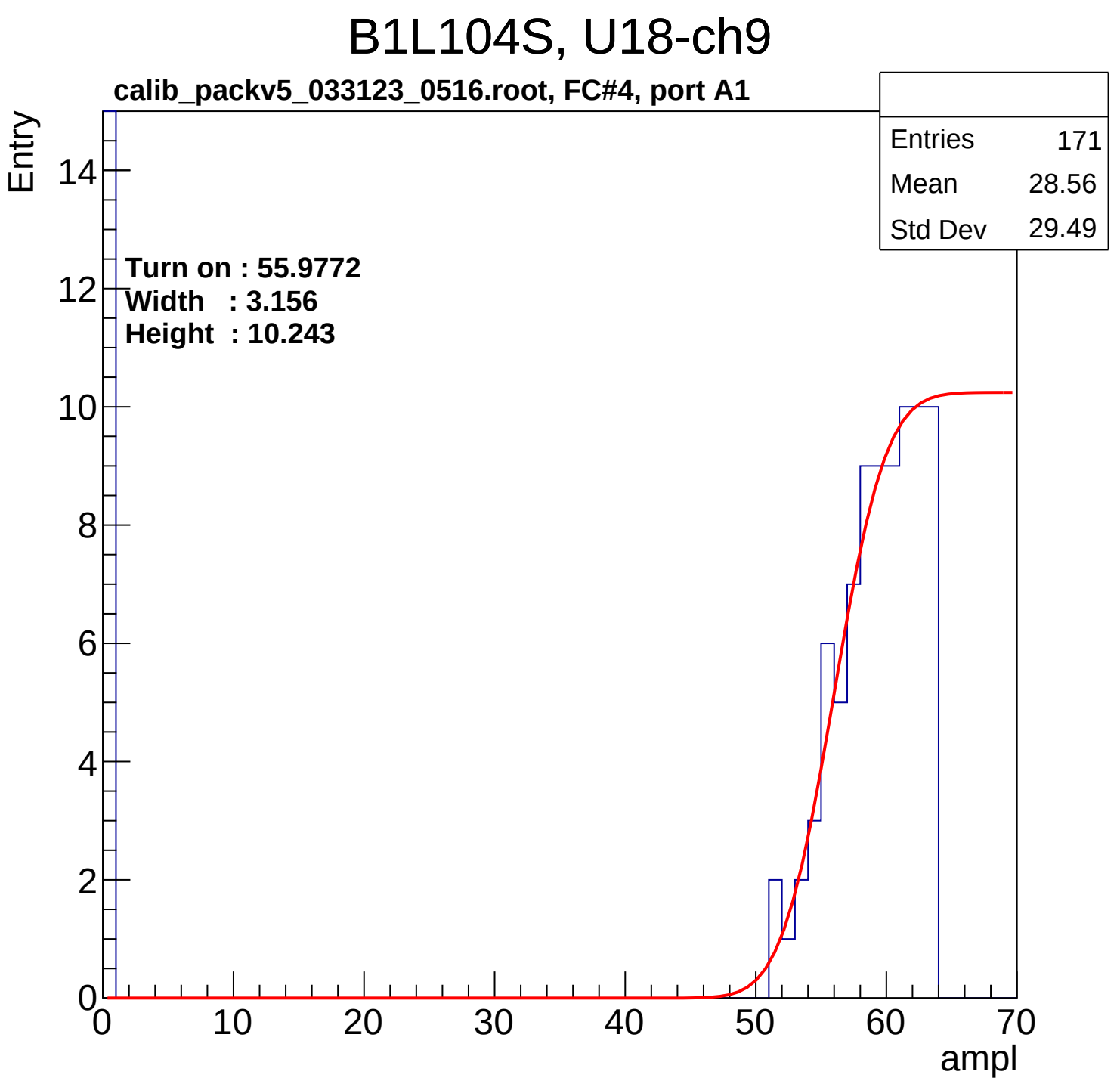

B1L104S, U18-ch4
calib_packv5_033123_0516.root, FC#4, port A1
Entries 206
Mean 31.17
Std Dev 28.7
Turn on : 52.5590
Width : 3.565
Height : 9.795
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

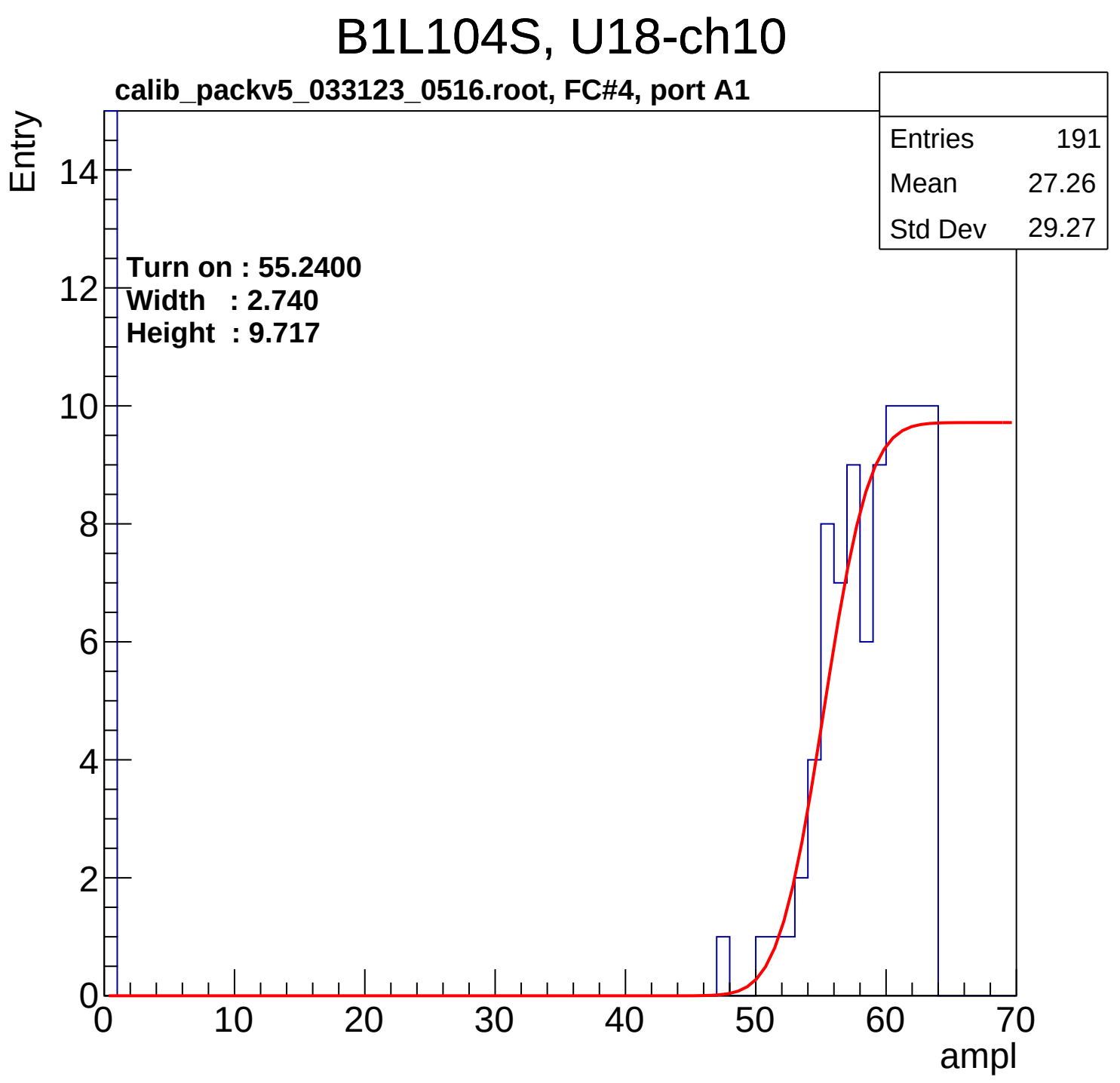

B1L104S, U18-ch5
calib_packv5_033123_0516.root, FC#4, port A1
Entries 180
Mean 33.49
Std Dev 28.76
Turn on : 53.6584
Width : 3.257
Height : 10.184
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

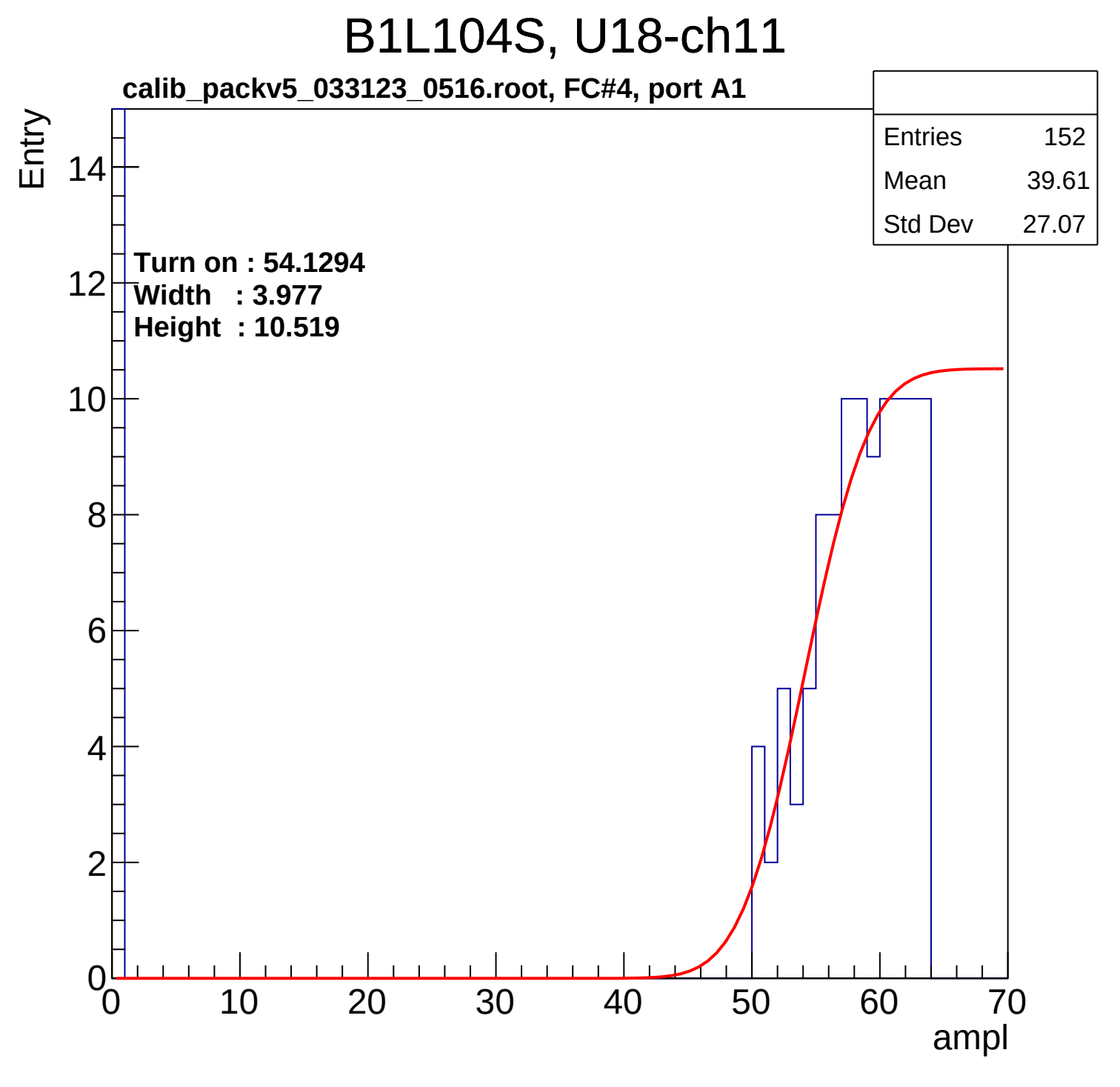

B1L104S, U18-ch6
calib_packv5_033123_0516.root, FC#4, port A1
Entries 169
Mean 39.78
Std Dev 26.4
Turn on : 52.5439
Width : 3.811
Height : 10.066
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

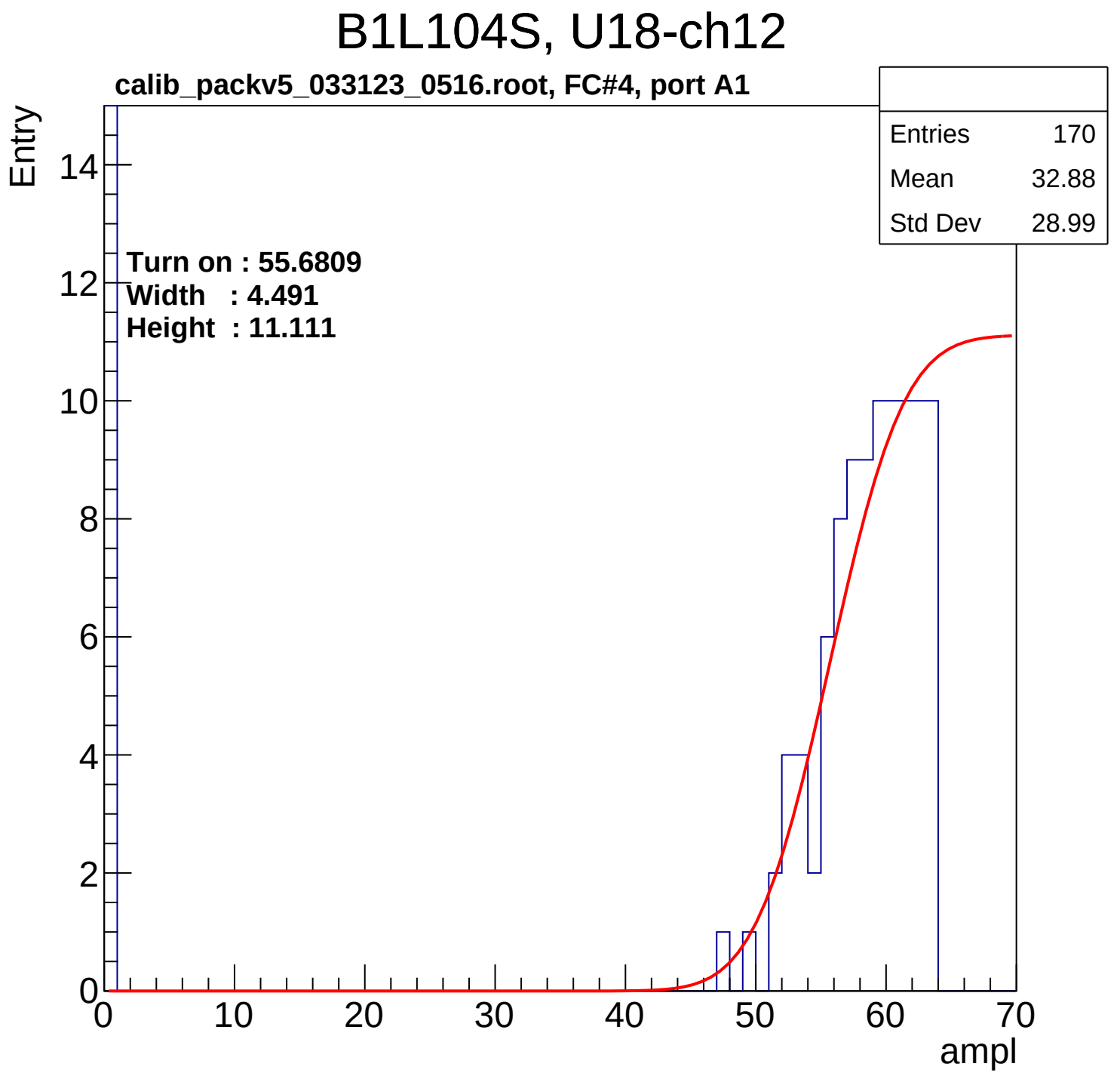

B1L104S, U18-ch7
calib_packv5_033123_0516.root, FC#4, port A1
Entries 155
Mean 38.88
Std Dev 27.39
Turn on : 54.4550
Width : 2.448
Height : 10.234
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

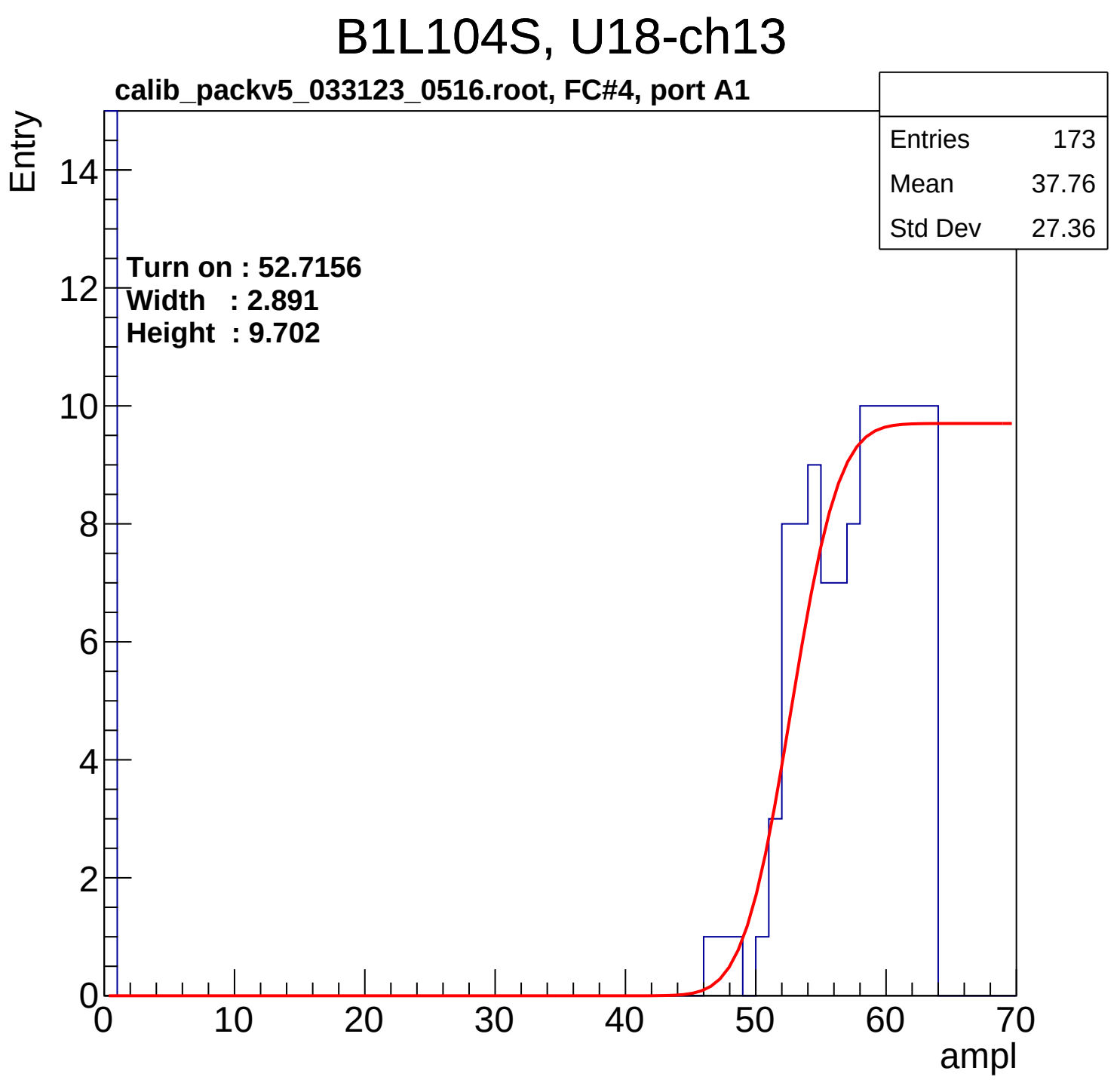

B1L104S, U18-ch8
calib_packv5_033123_0516.root, FC#4, port A1
Entries 183
Mean 35.98
Std Dev 27.85
Turn on : 52.9337
Width : 3.618
Height : 10.191
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

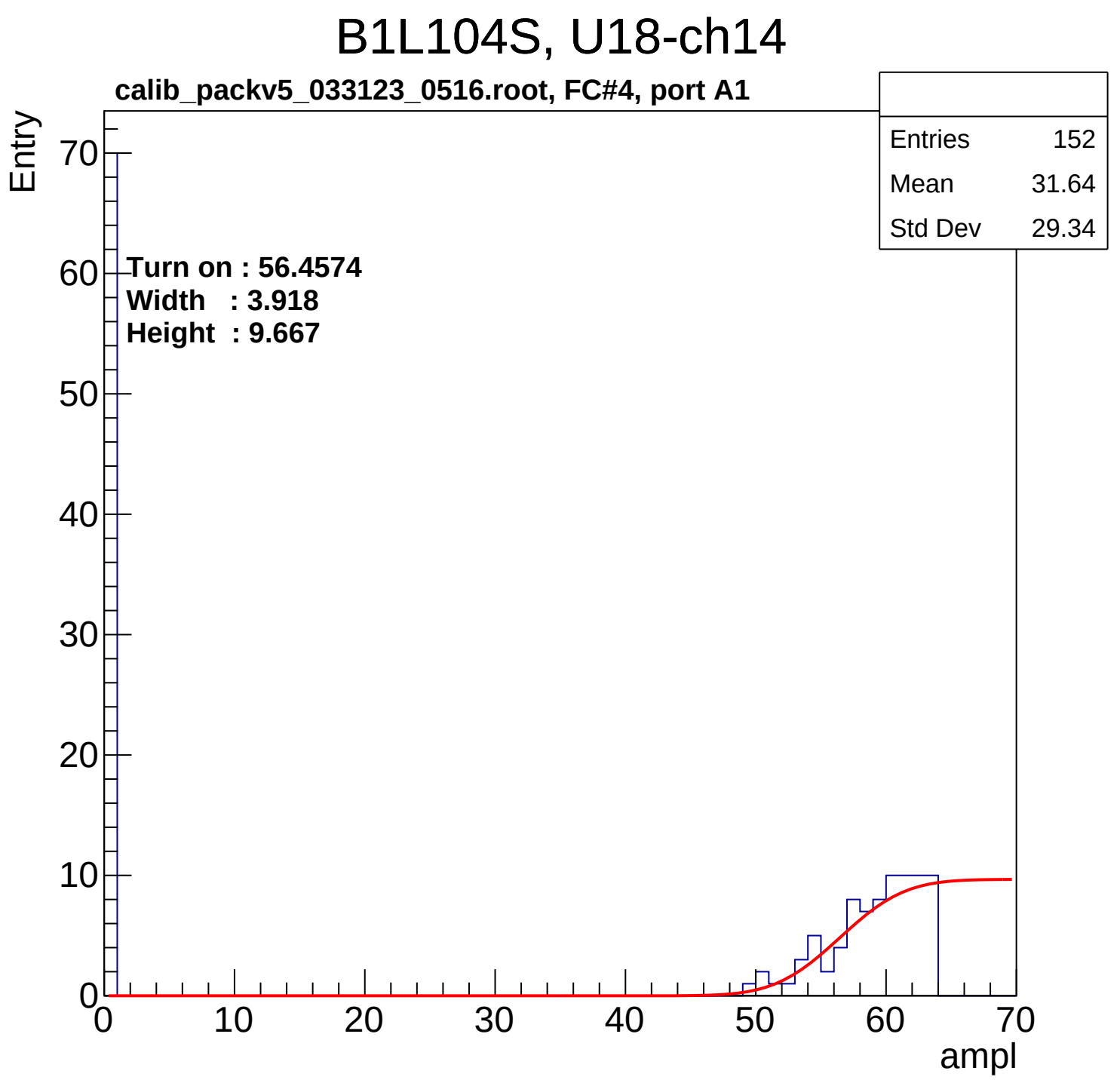

B1L104S, U18-ch9
calib_packv5_033123_0516.root, FC#4, port A1
Entries 171
Mean 28.56
Std Dev 29.49
Turn on : 55.9772
Width : 3.156
Height : 10.243
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

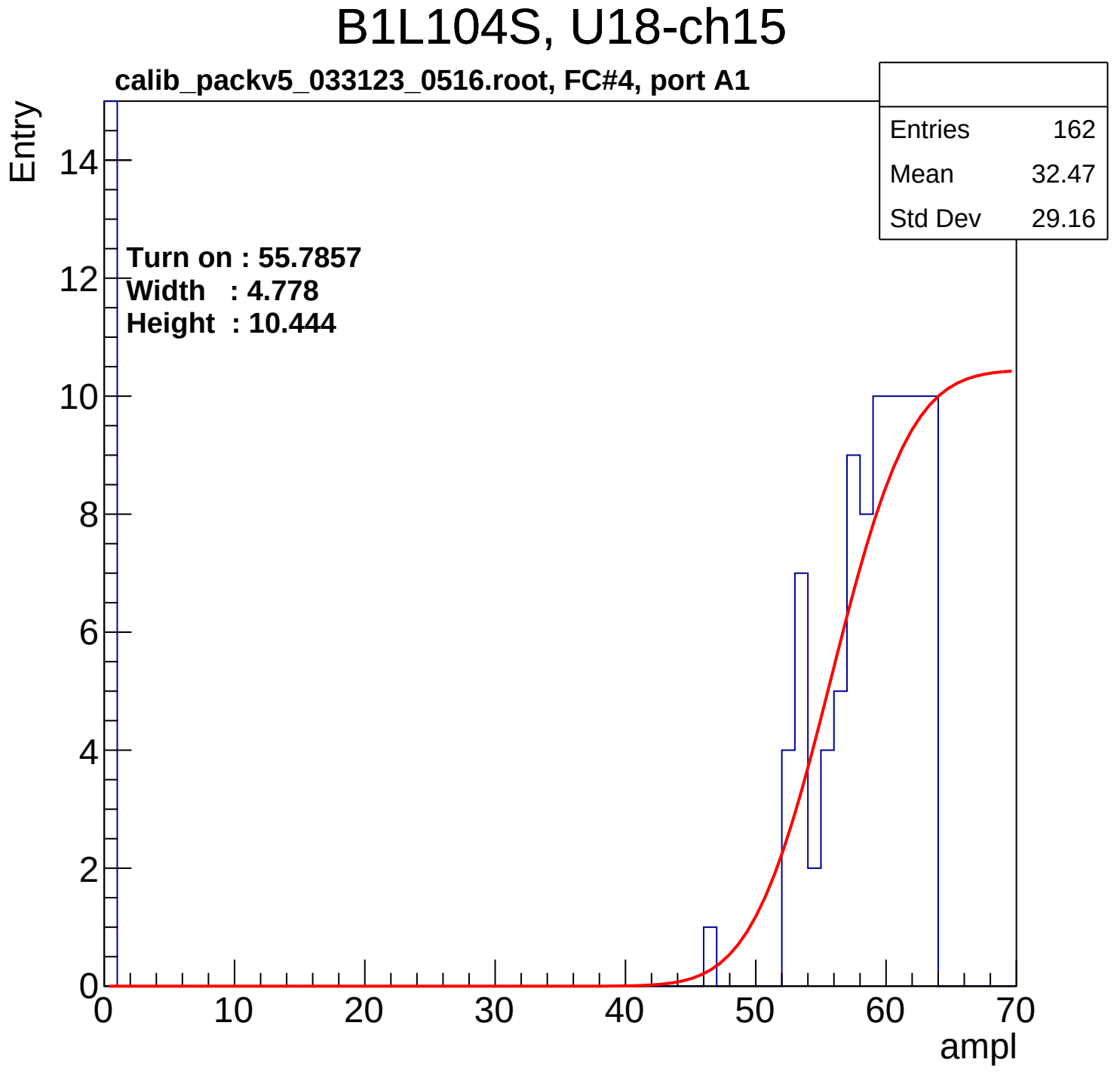

B1L104S, U18-ch10
calib_packv5_033123_0516.root, FC#4, port A1
Entries 191
Mean 27.26
Std Dev 29.27
Turn on : 55.2400
Width : 2.740
Height : 9.717
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

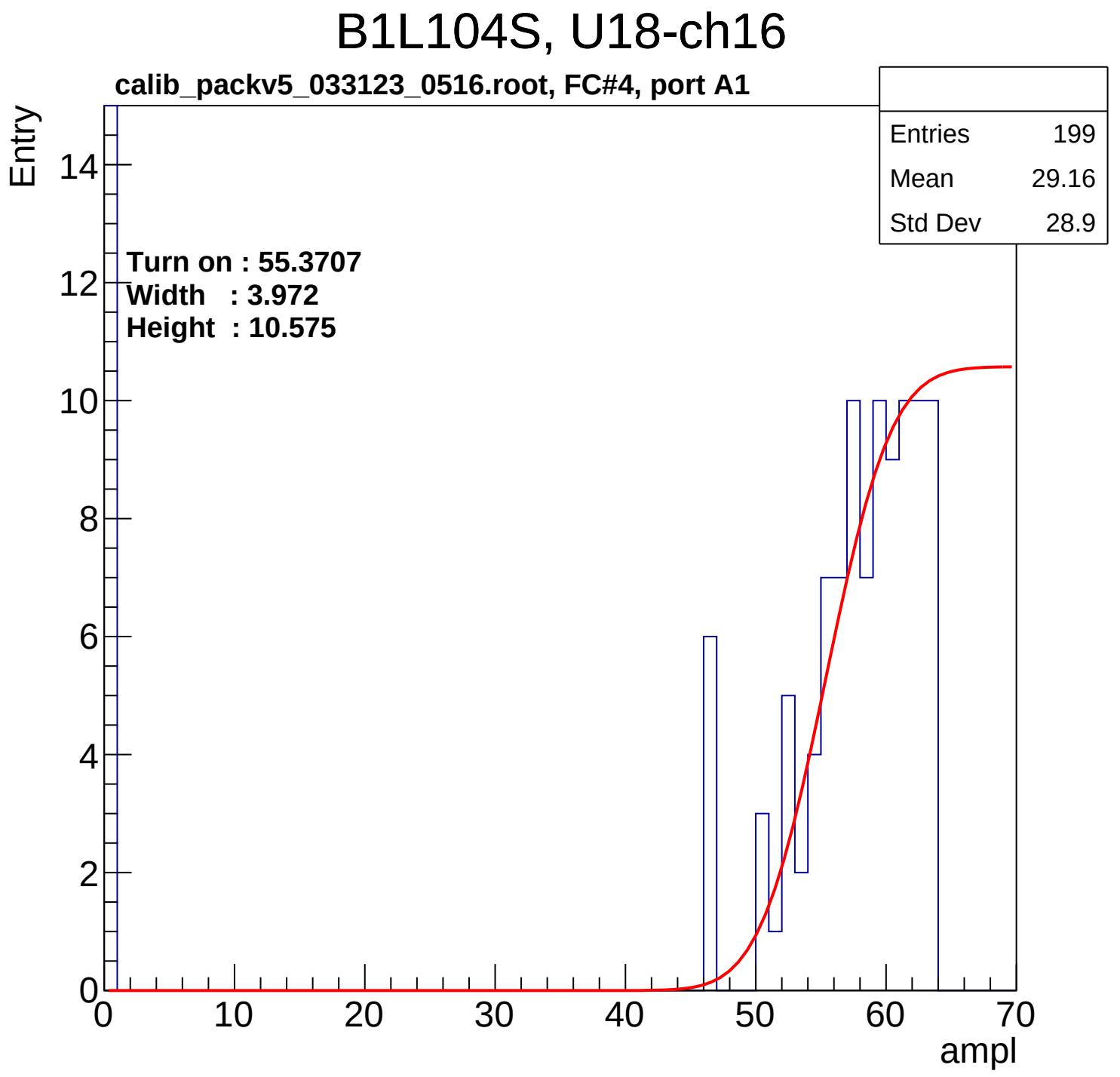

B1L104S, U18-ch11
calib_packv5_033123_0516.root, FC#4, port A1
Entries 152
Mean 39.61
Std Dev 27.07
Turn on : 54.1294
Width : 3.977
Height : 10.519
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

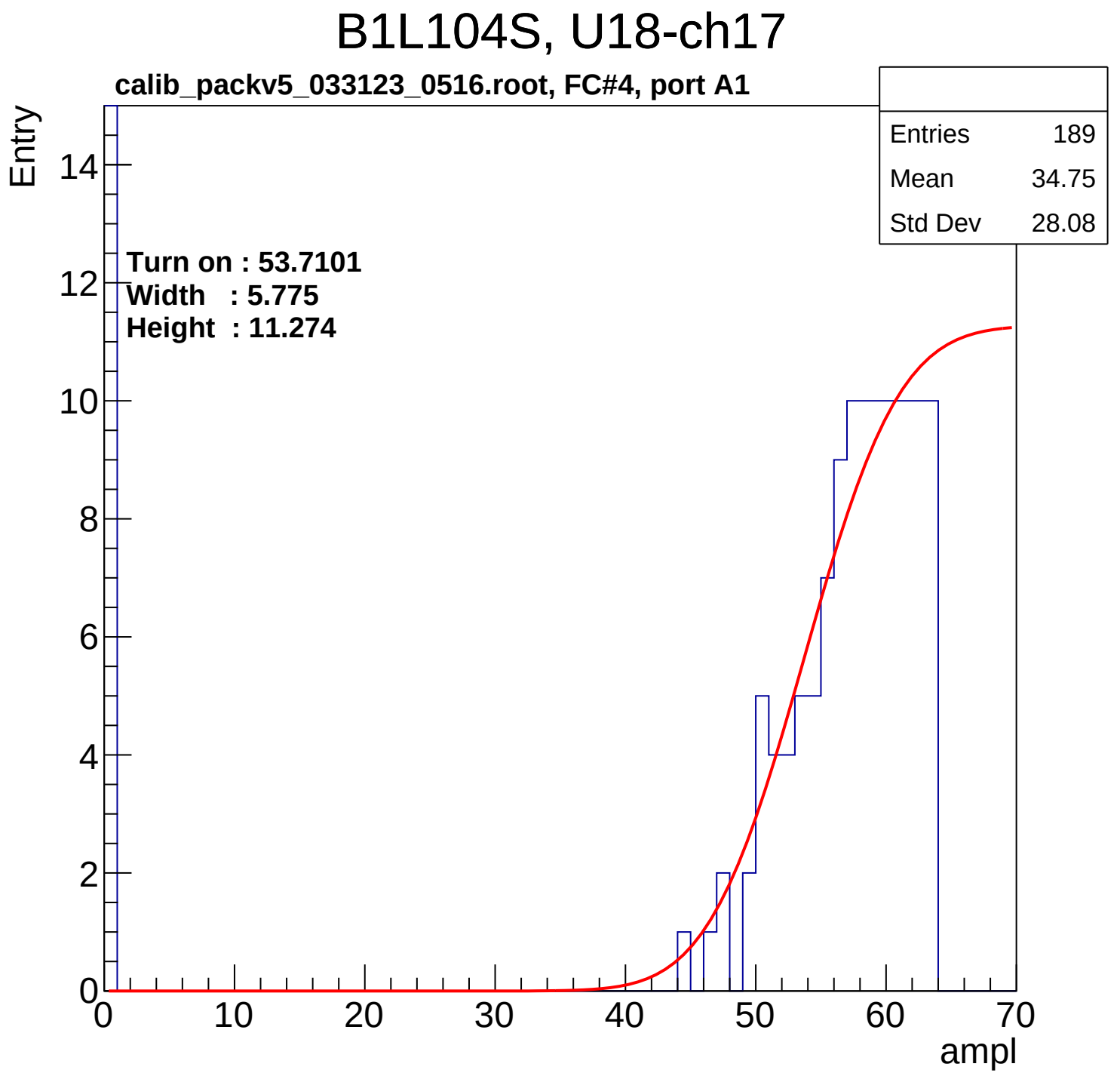

B1L104S, U18-ch12
calib_packv5_033123_0516.root, FC#4, port A1
Entries 170
Mean 32.88
Std Dev 28.99
Turn on : 55.6809
Width : 4.491
Height : 11.111
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

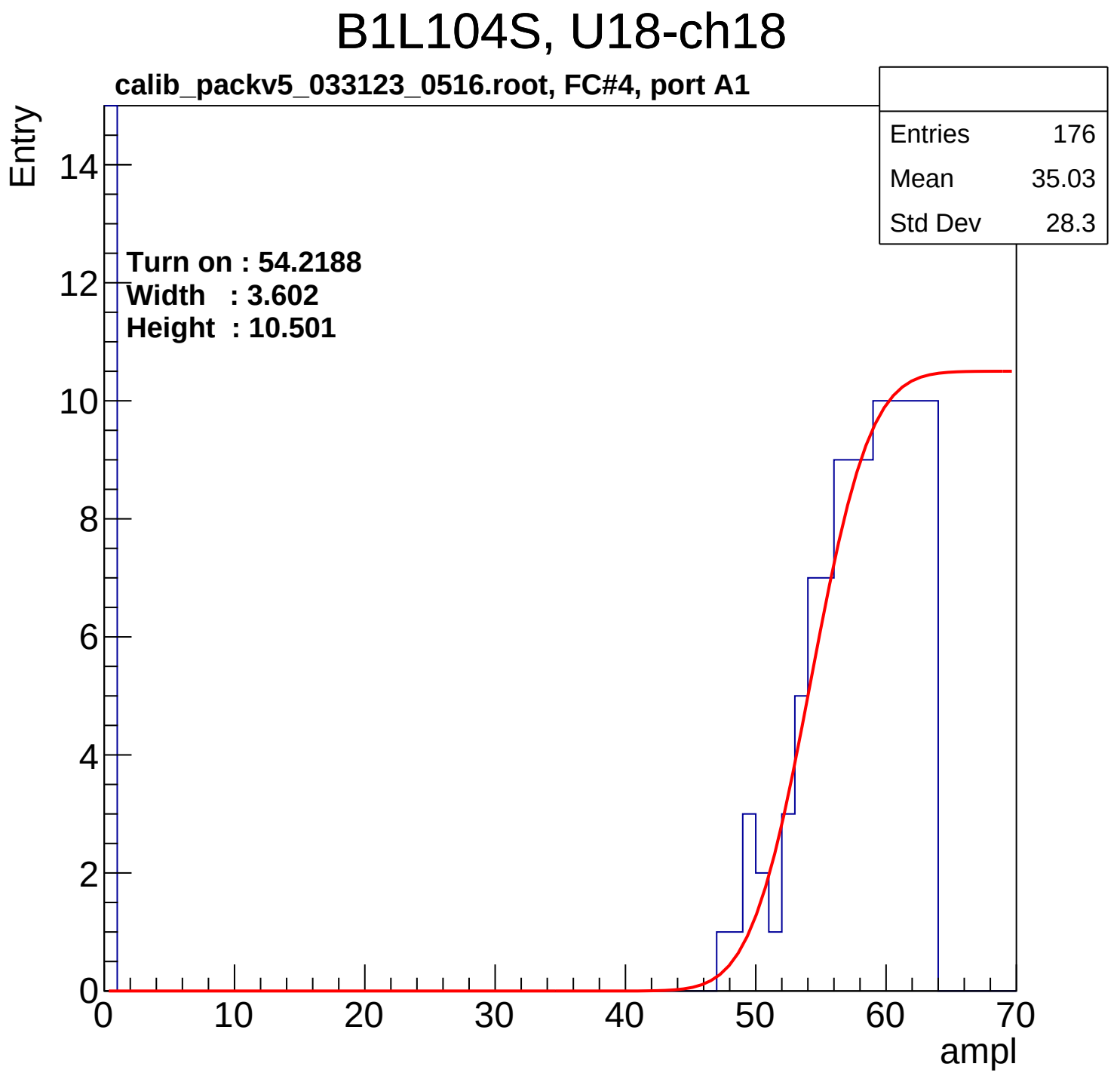

B1L104S, U18-ch13
calib_packv5_033123_0516.root, FC#4, port A1
Entries 173
Mean 37.76
Std Dev 27.36
Turn on : 52.7156
Width : 2.891
Height : 9.702
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

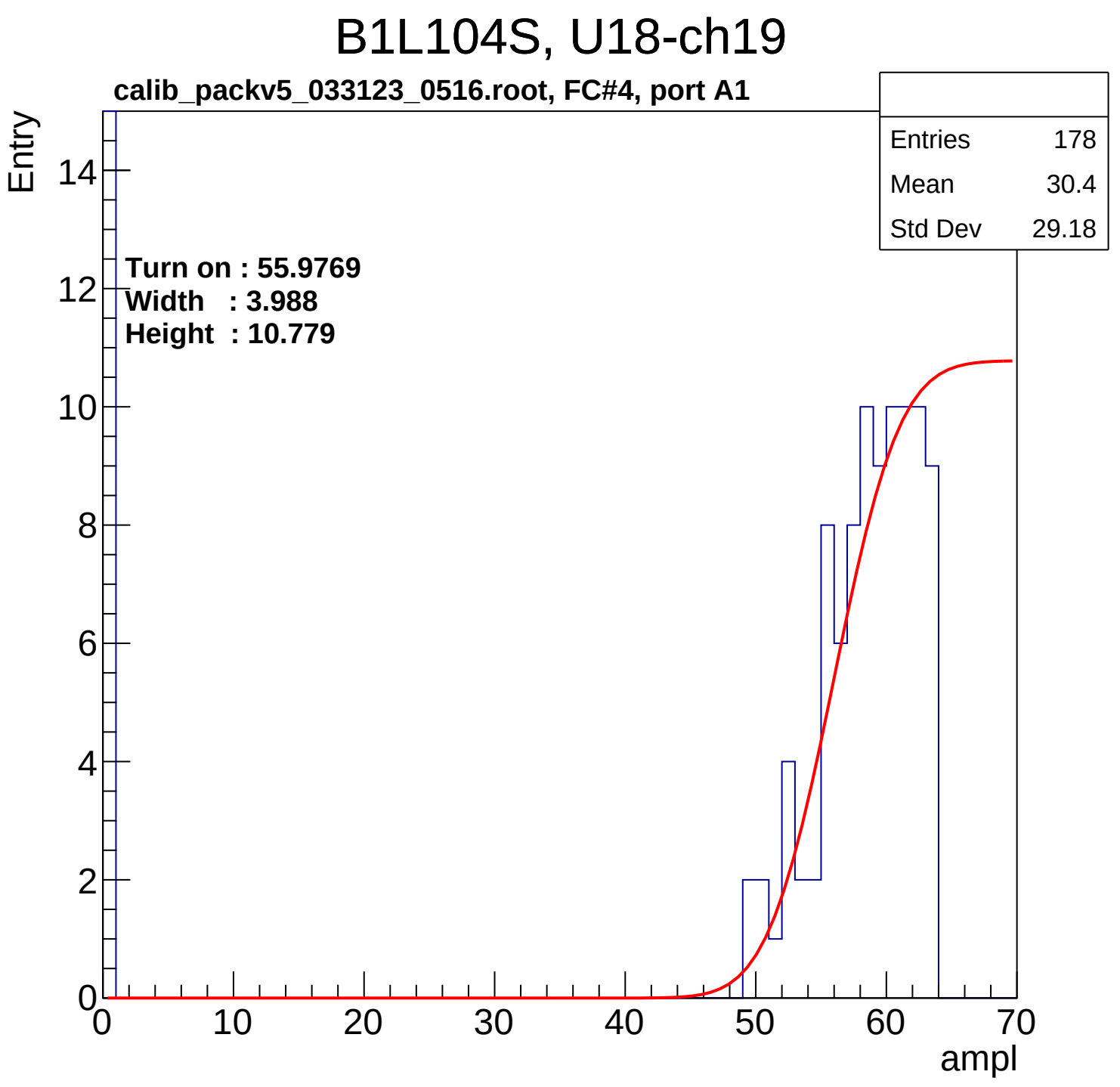

B1L104S, U18-ch14
calib_packv5_033123_0516.root, FC#4, port A1
Entries 152
Mean 31.64
Std Dev 29.34
Turn on : 56.4574
Width : 3.918
Height : 9.667
Entry
ampl
0
10
20
30
40
50
60
70

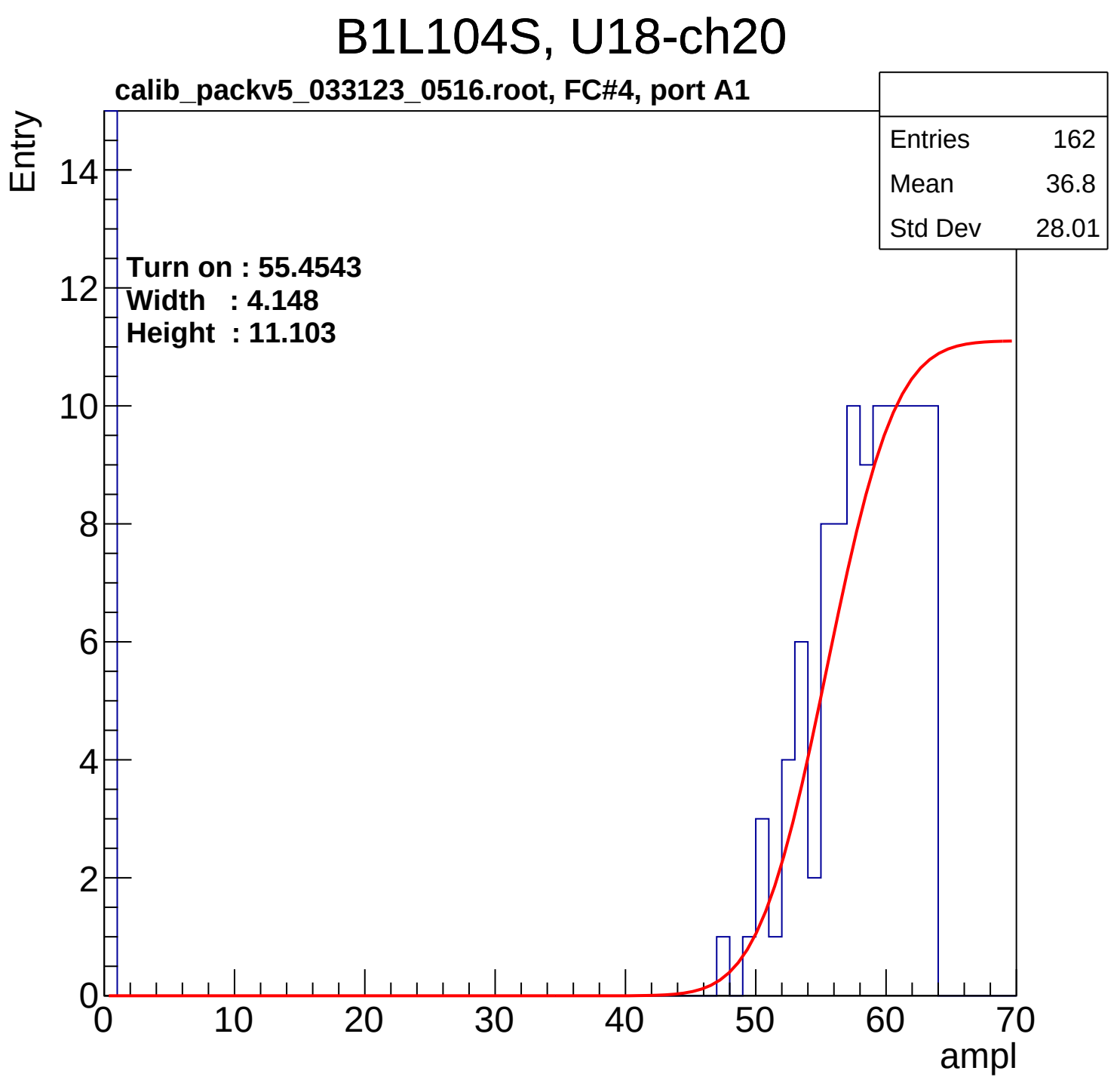

B1L104S, U18-ch15
calib_packv5_033123_0516.root, FC#4, port A1
Entries 162
Mean 32.47
Std Dev 29.16
Turn on : 55.7857
Width : 4.778
Height : 10.444
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

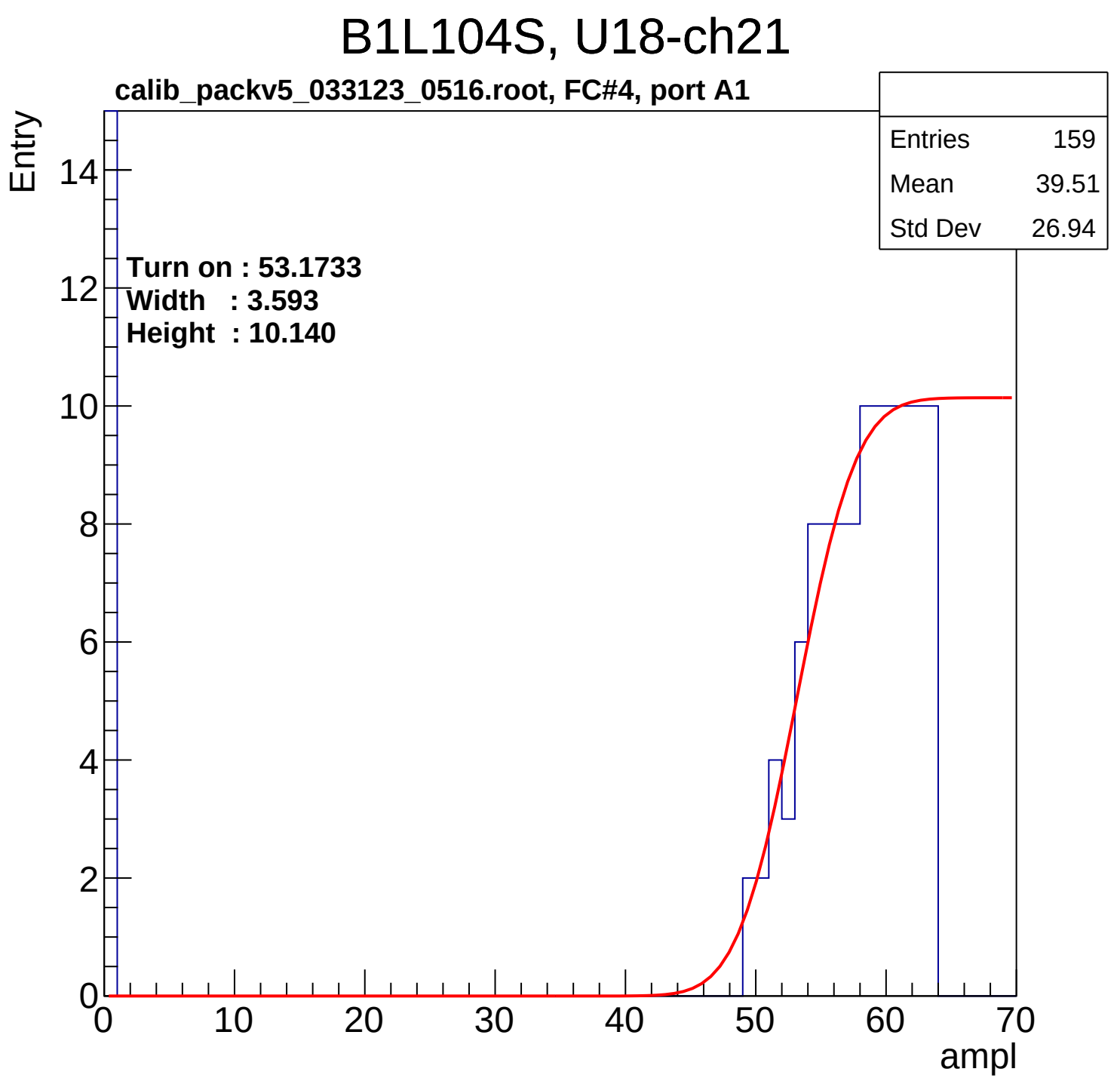

B1L104S, U18-ch16
calib_packv5_033123_0516.root, FC#4, port A1
Entries 199
Mean 29.16
Std Dev 28.9
Turn on : 55.3707
Width : 3.972
Height : 10.575
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

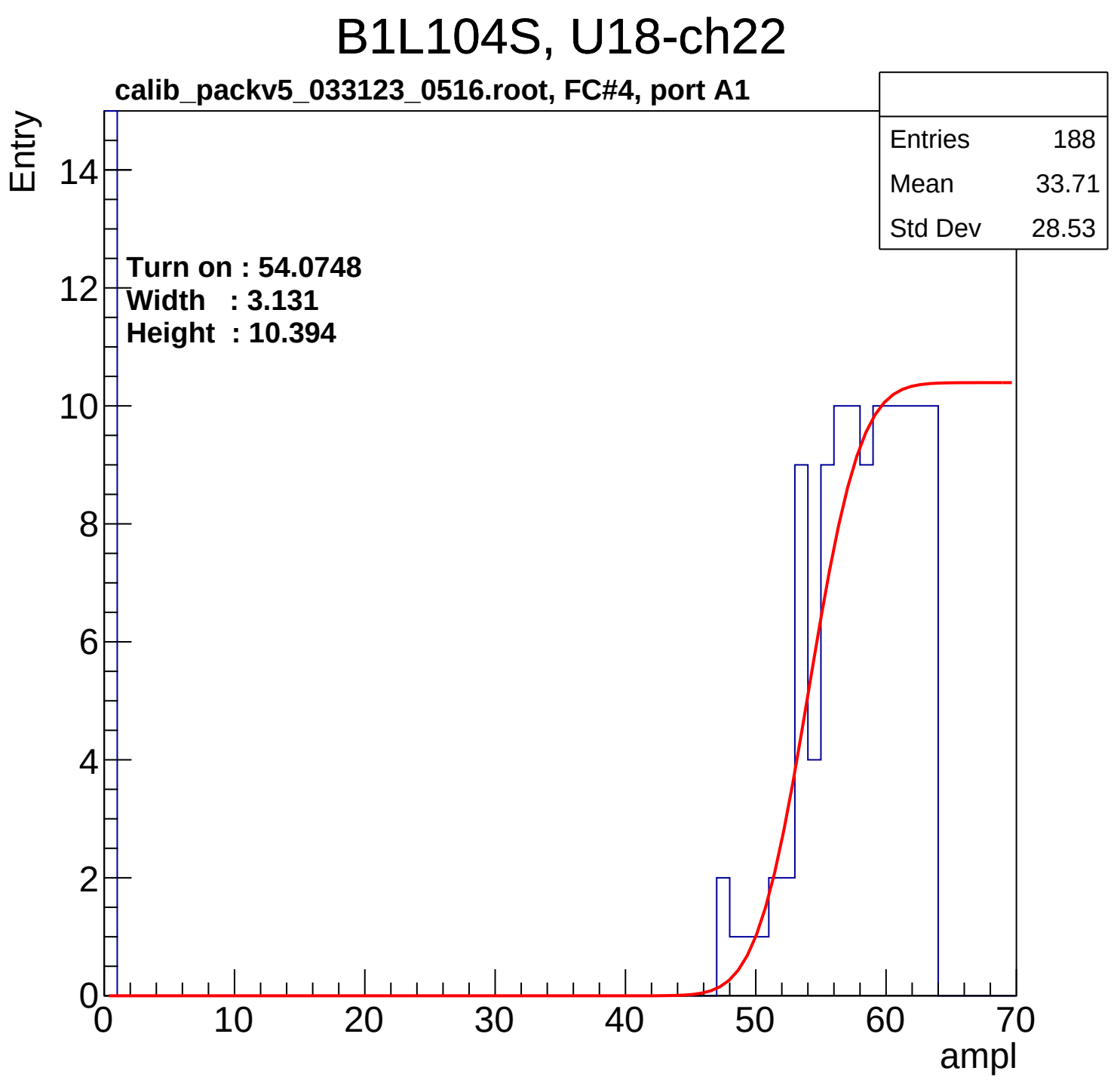

B1L104S, U18-ch17
calib_packv5_033123_0516.root, FC#4, port A1
Entries 189
Mean 34.75
Std Dev 28.08
Turn on : 53.7101
Width : 5.775
Height : 11.274
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

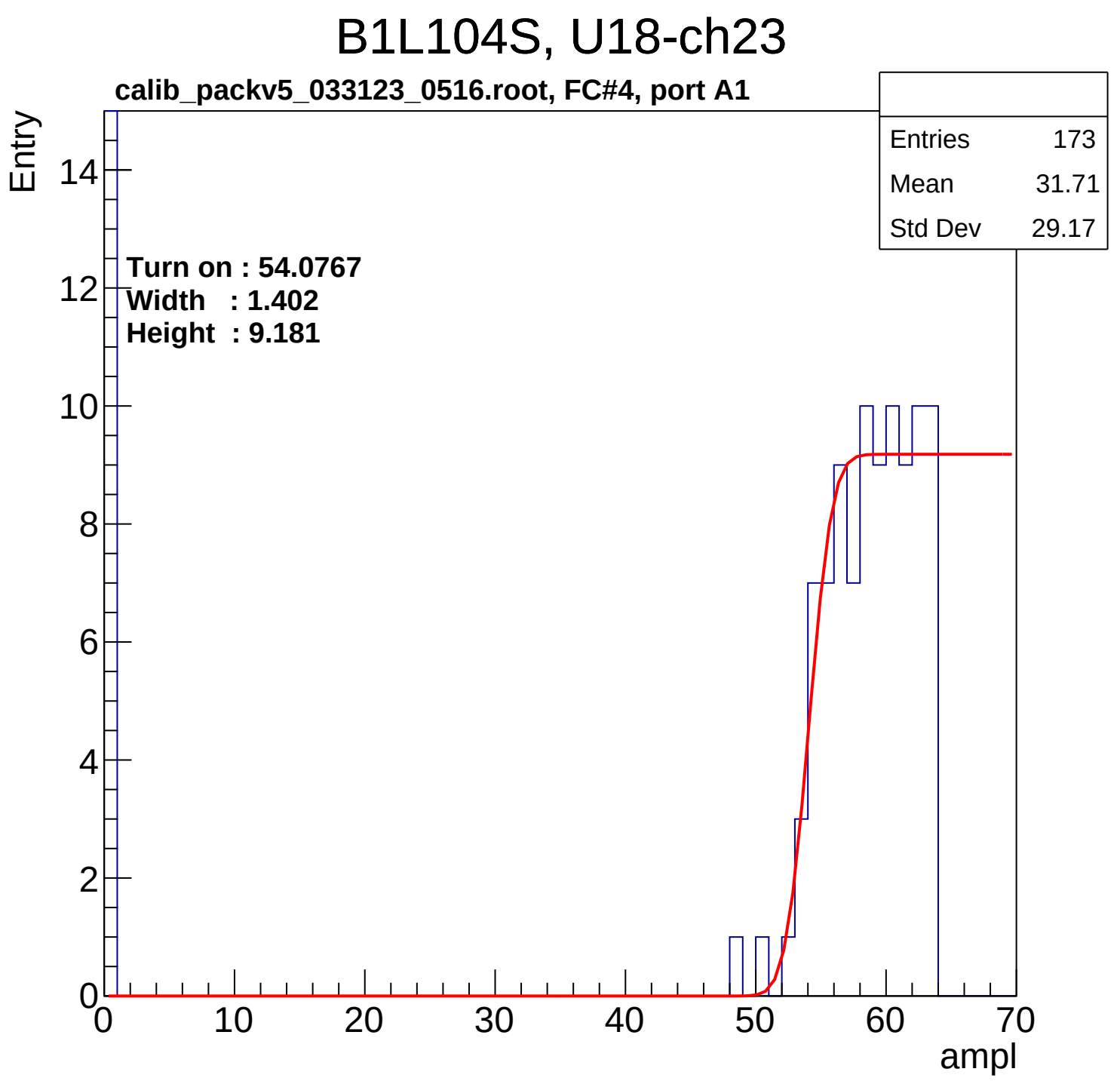

B1L104S, U18-ch18
calib_packv5_033123_0516.root, FC#4, port A1
Entries 176
Mean 35.03
Std Dev 28.3
Turn on : 54.2188
Width : 3.602
Height : 10.501
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

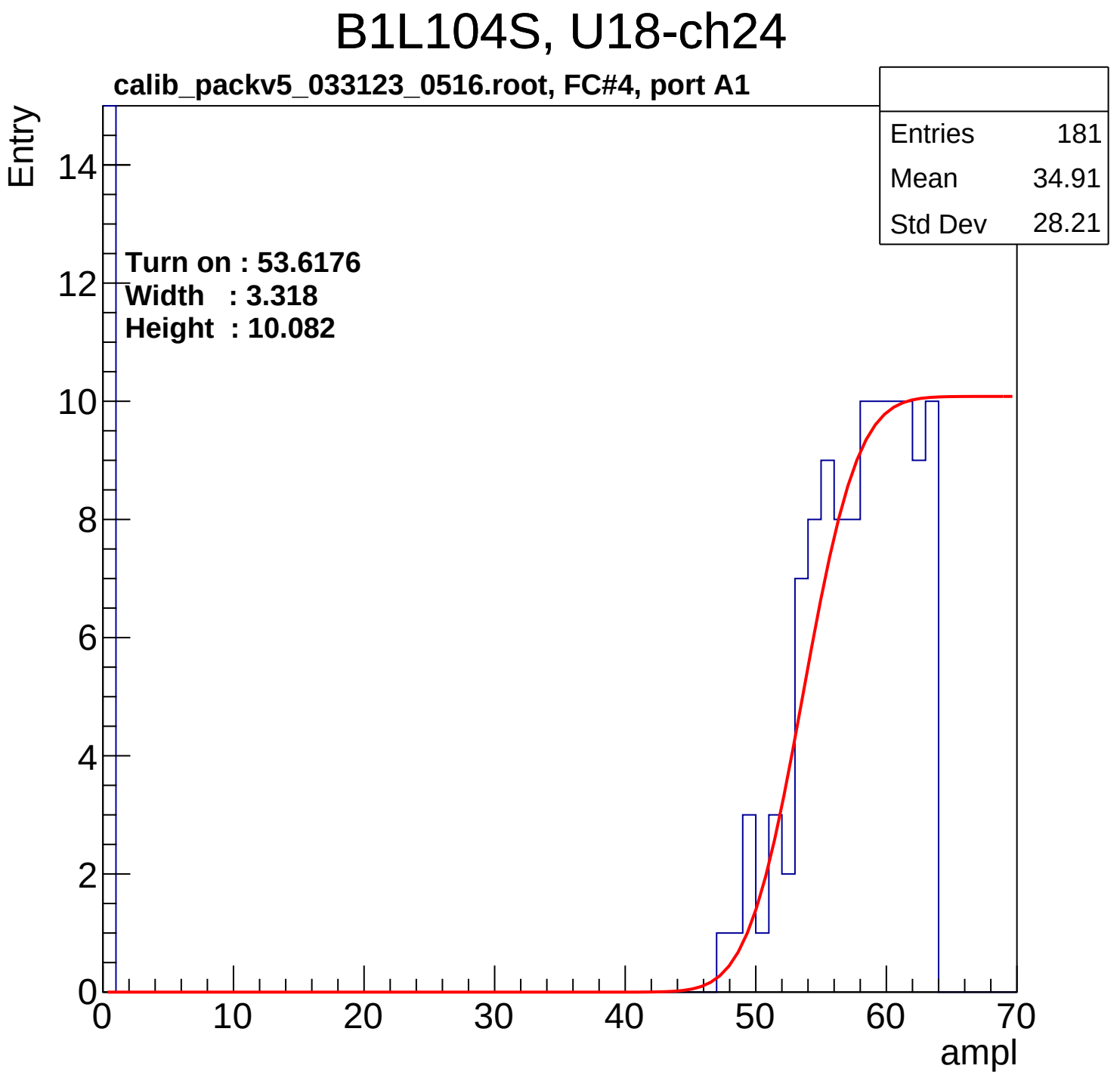

B1L104S, U18-ch19
calib_packv5_033123_0516.root, FC#4, port A1
Entries 178
Mean 30.4
Std Dev 29.18
Turn on : 55.9769
Width : 3.988
Height : 10.779
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

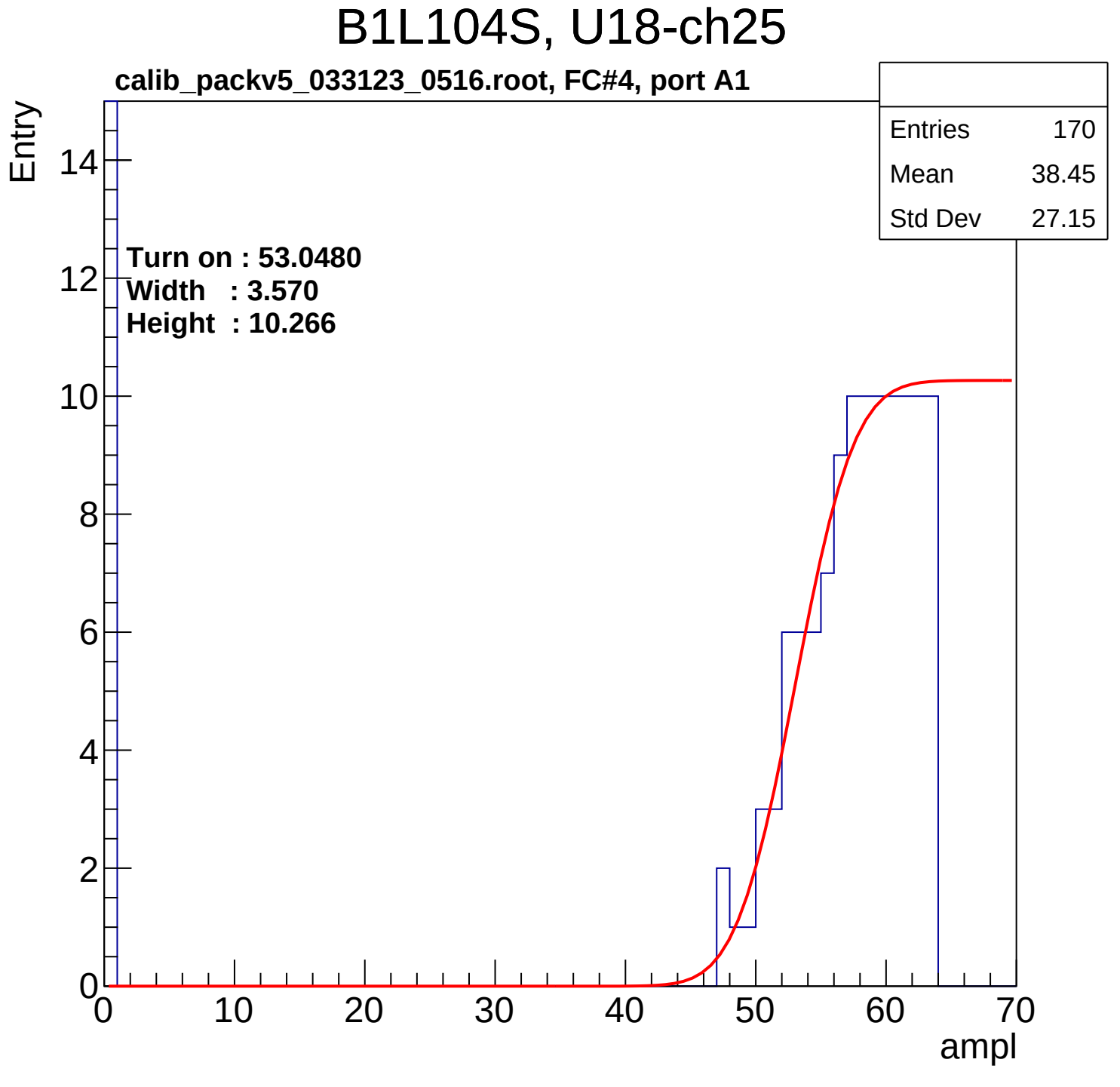

B1L104S, U18-ch20
calib_packv5_033123_0516.root, FC#4, port A1
Entries 162
Mean 36.8
Std Dev 28.01
Turn on : 55.4543
Width : 4.148
Height : 11.103
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

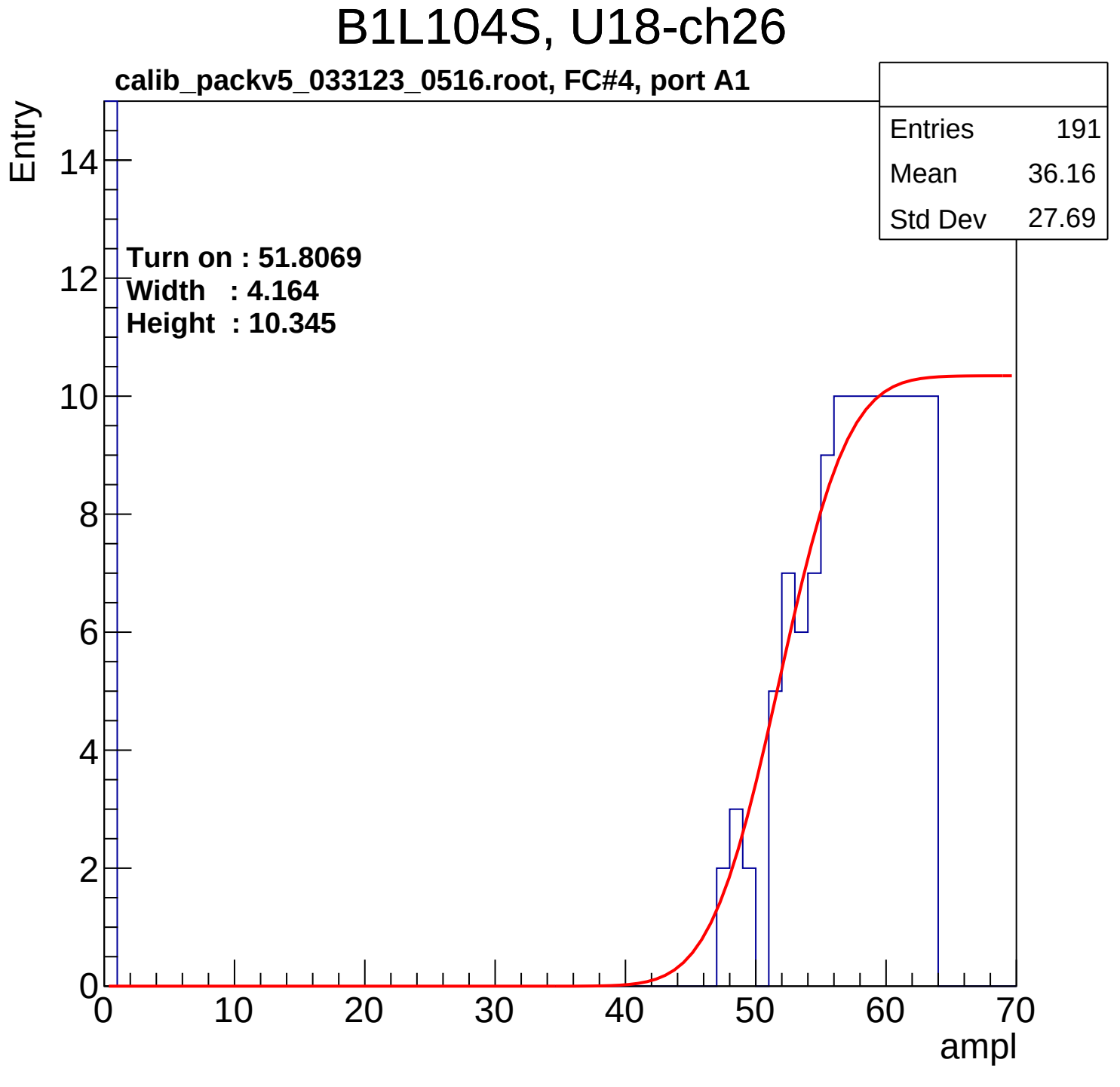

B1L104S, U18-ch21
calib_packv5_033123_0516.root, FC#4, port A1
Entries 159
Mean 39.51
Std Dev 26.94
Turn on : 53.1733
Width : 3.593
Height : 10.140
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

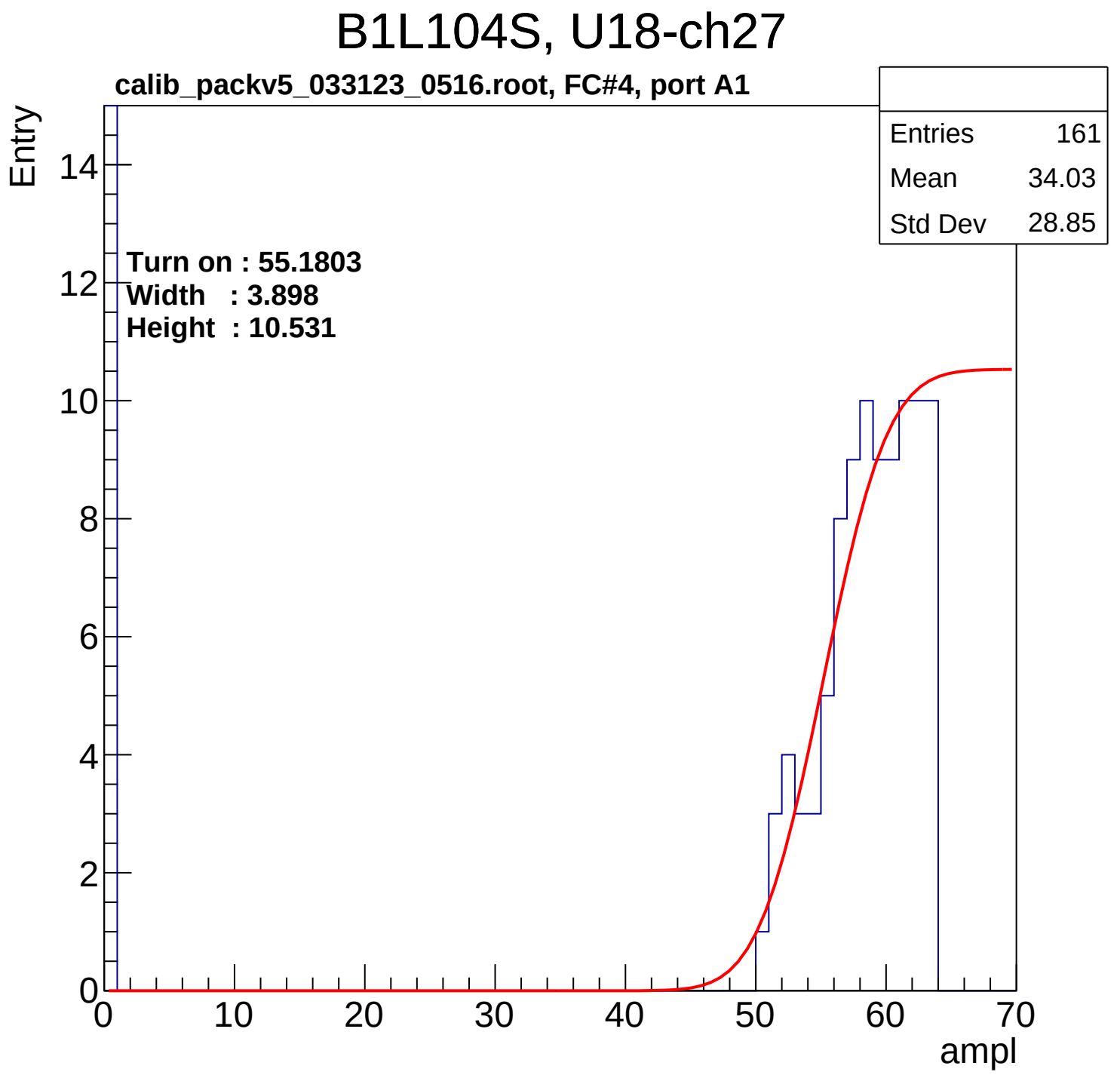

B1L104S, U18-ch22
calib_packv5_033123_0516.root, FC#4, port A1
Entries 188
Mean 33.71
Std Dev 28.53
Turn on : 54.0748
Width : 3.131
Height : 10.394
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

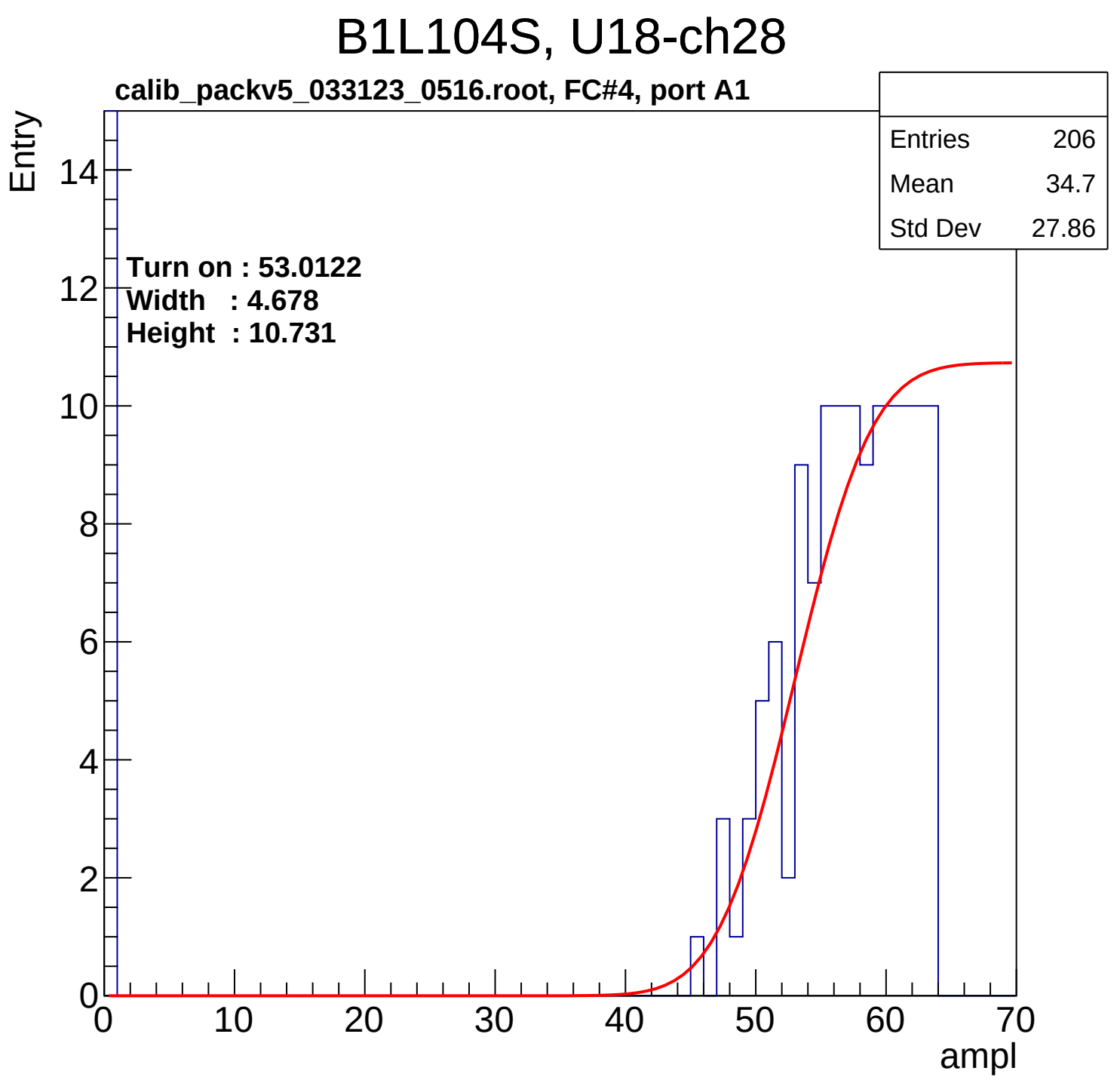

B1L104S, U18-ch23
calib_packv5_033123_0516.root, FC#4, port A1
Entries 173
Mean 31.71
Std Dev 29.17
Turn on : 54.0767
Width : 1.402
Height : 9.181
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

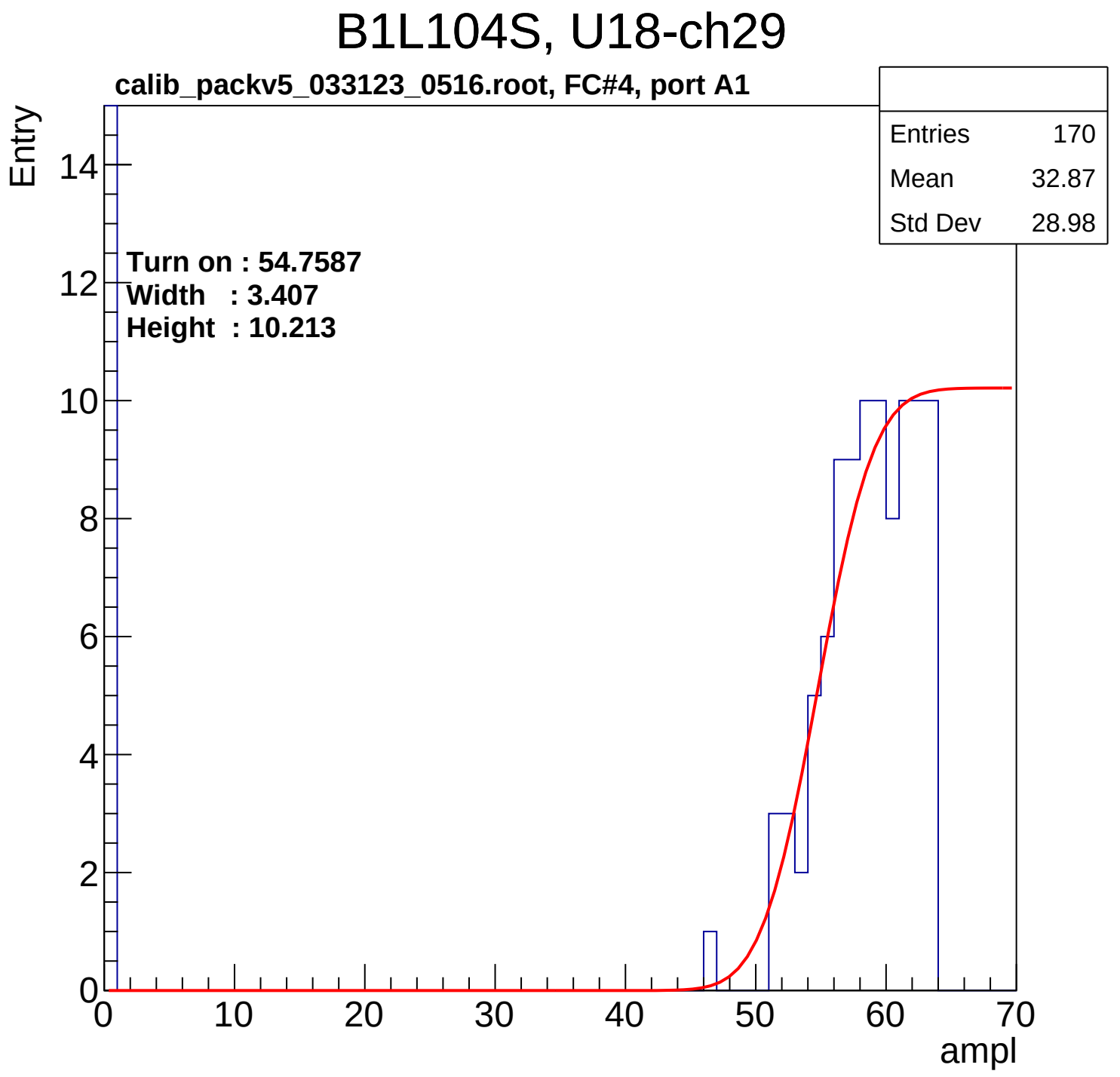

B1L104S, U18-ch24
calib_packv5_033123_0516.root, FC#4, port A1
Entries 181
Mean 34.91
Std Dev 28.21
Turn on : 53.6176
Width : 3.318
Height : 10.082
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

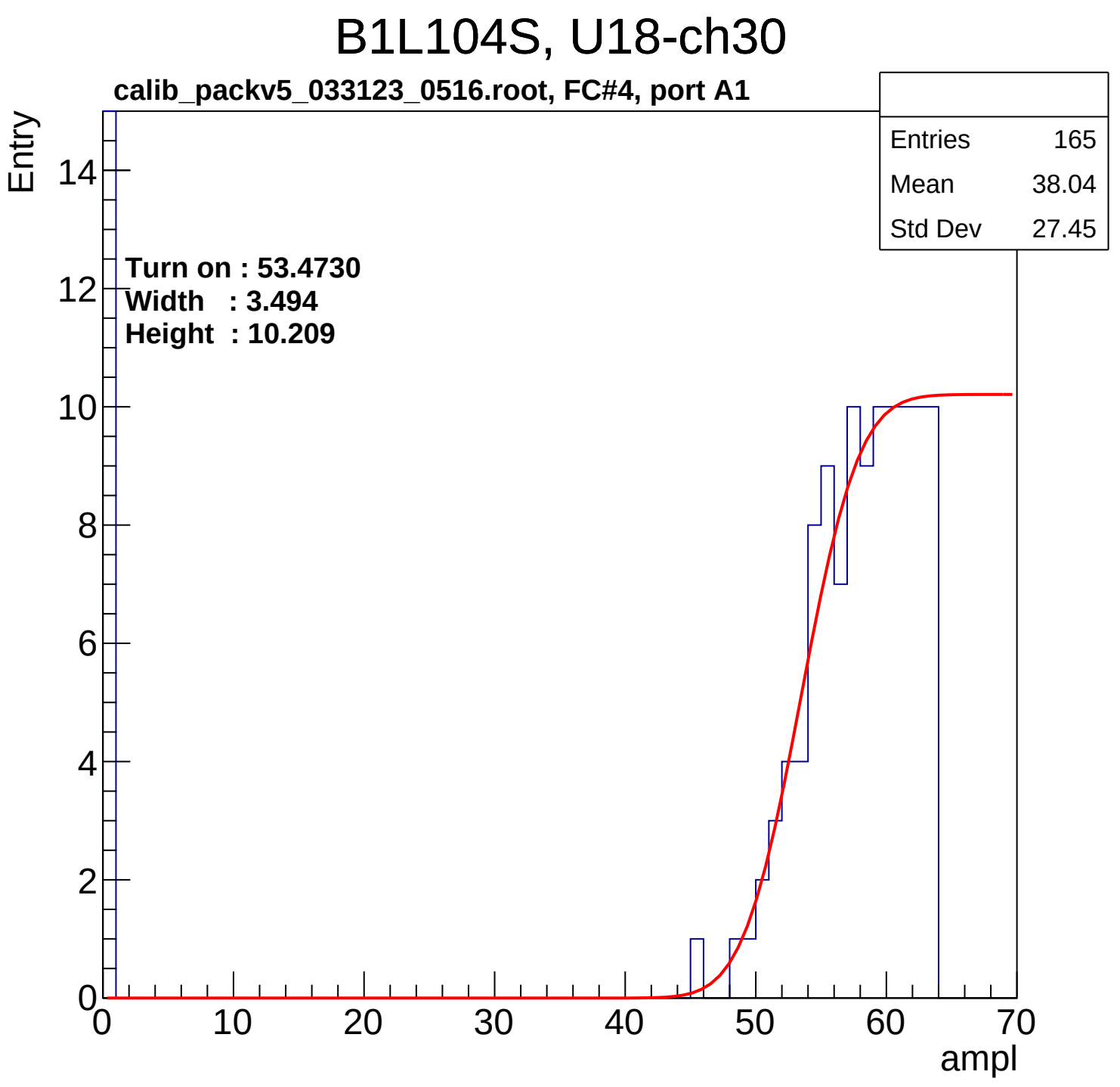

B1L104S, U18-ch25
calib_packv5_033123_0516.root, FC#4, port A1
Entries 170
Mean 38.45
Std Dev 27.15
Turn on : 53.0480
Width : 3.570
Height : 10.266
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

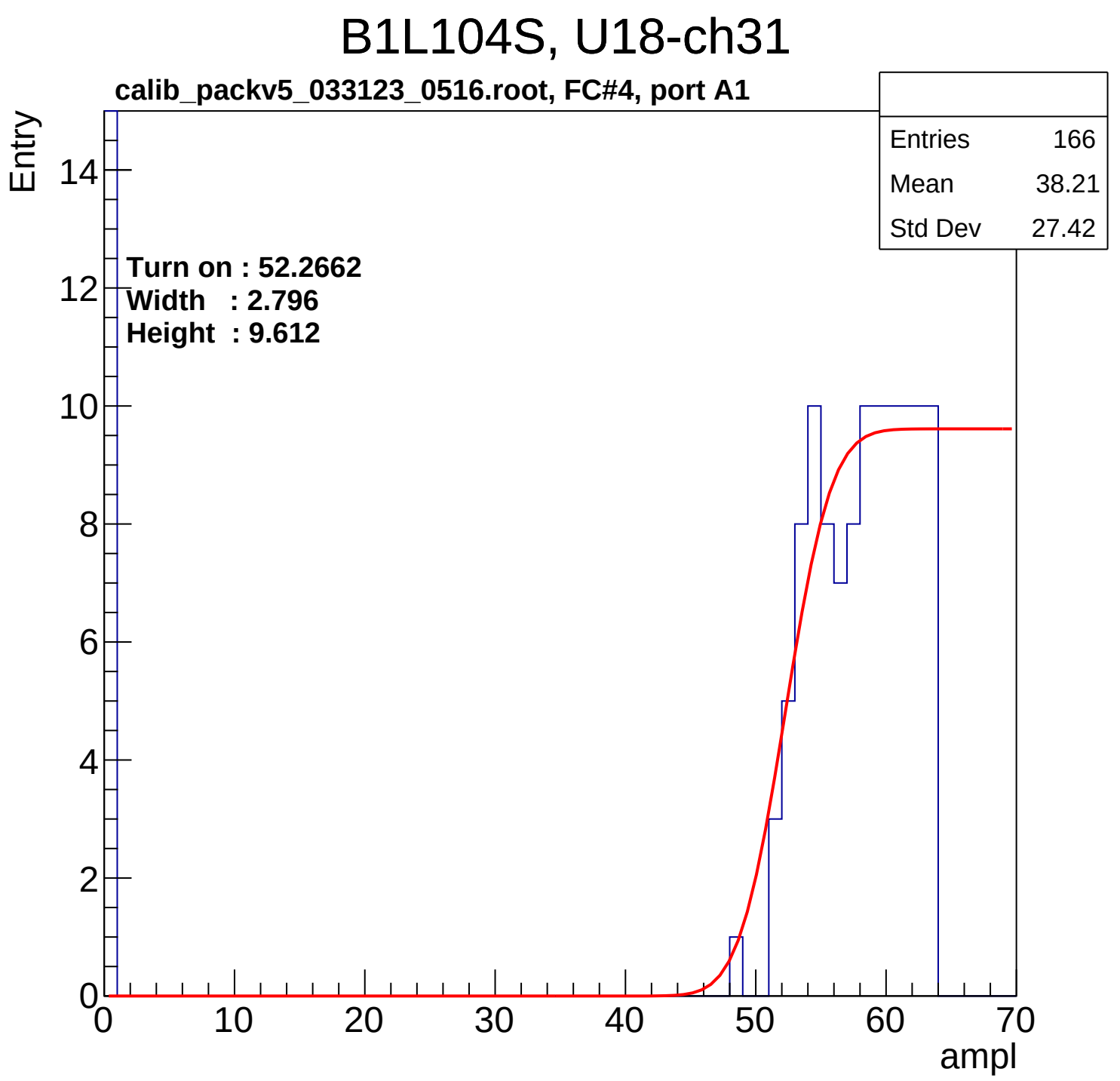

B1L104S, U18-ch26
calib_packv5_033123_0516.root, FC#4, port A1
Entries 191
Mean 36.16
Std Dev 27.69
Turn on : 51.8069
Width : 4.164
Height : 10.345
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

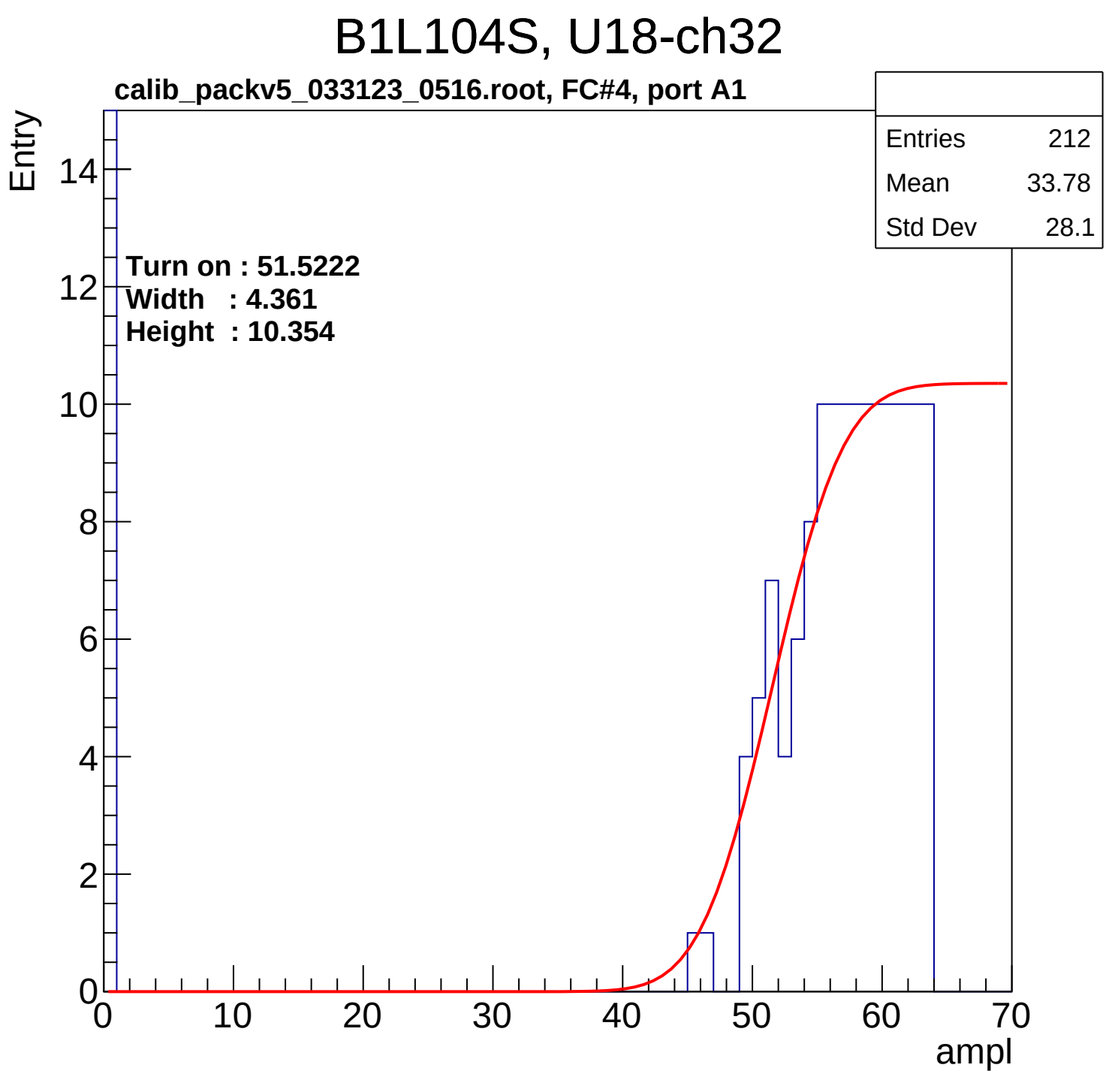

B1L104S, U18-ch27
calib_packv5_033123_0516.root, FC#4, port A1
Entries 161
Mean 34.03
Std Dev 28.85
Turn on : 55.1803
Width : 3.898
Height : 10.531
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

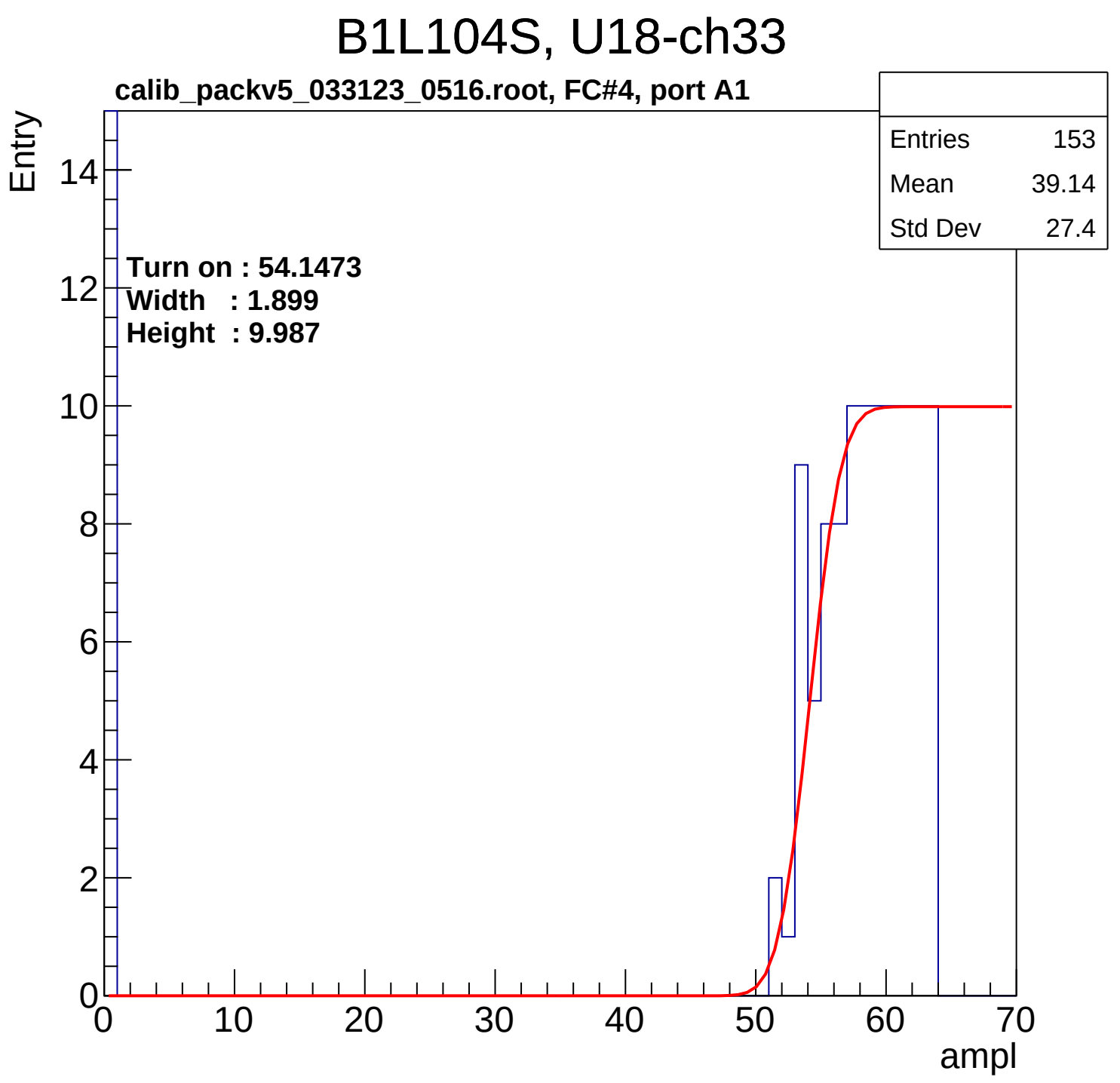

B1L104S, U18-ch28
calib_packv5_033123_0516.root, FC#4, port A1
Entries 206
Mean 34.7
Std Dev 27.86
Turn on : 53.0122
Width : 4.678
Height : 10.731
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

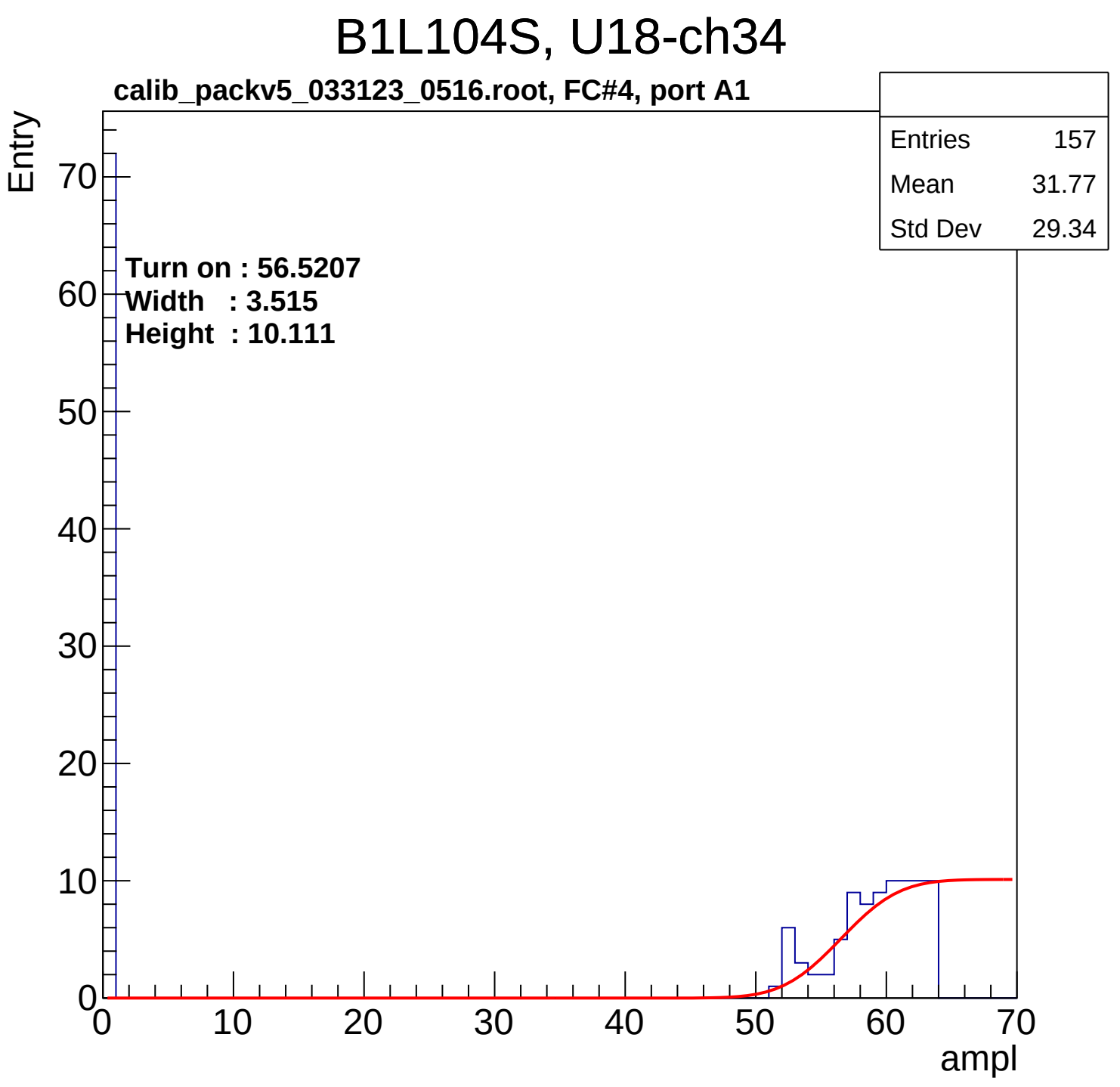

B1L104S, U18-ch29
calib_packv5_033123_0516.root, FC#4, port A1
Entries 170
Mean 32.87
Std Dev 28.98
Turn on : 54.7587
Width : 3.407
Height : 10.213
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

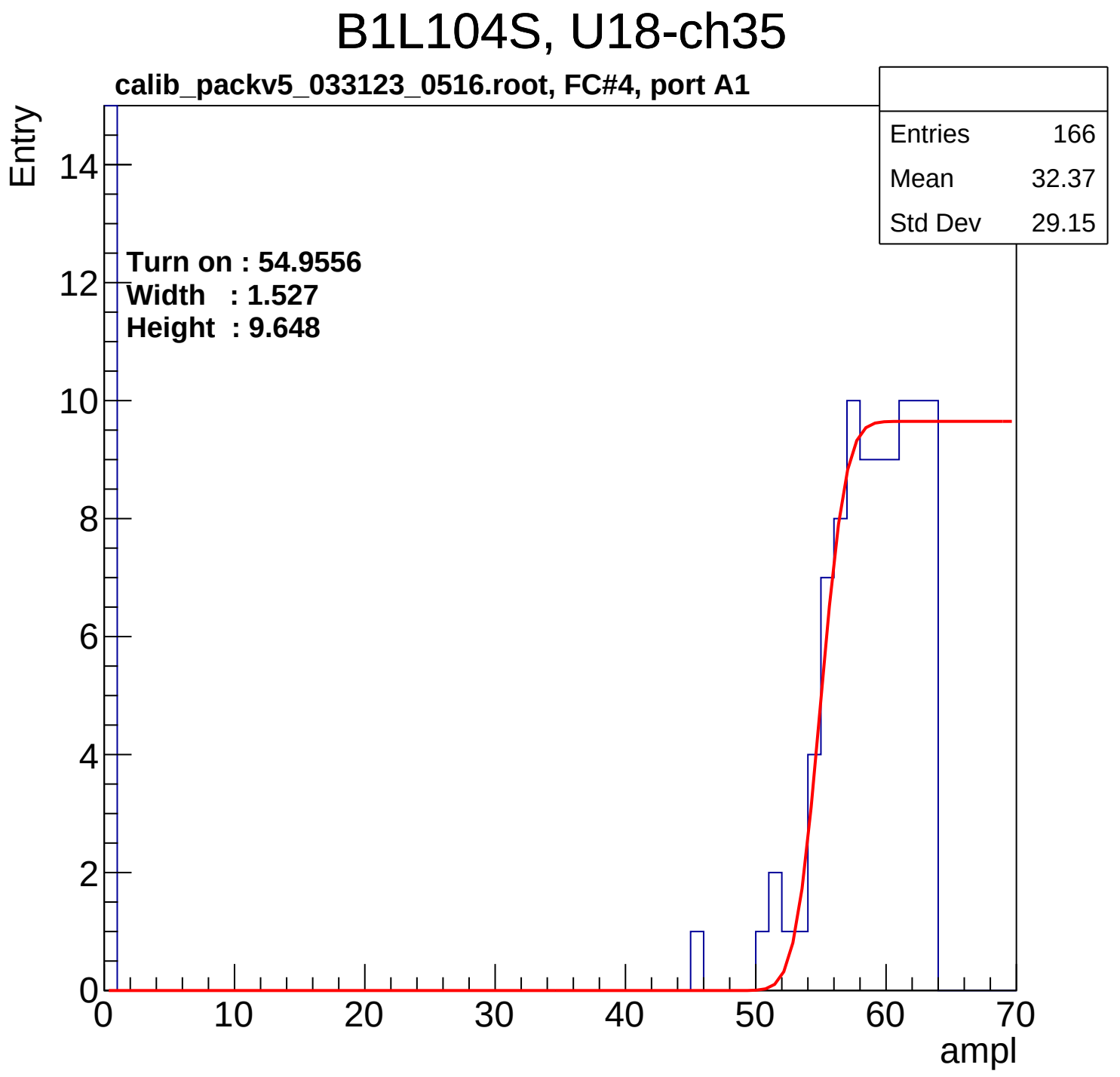

B1L104S, U18-ch30
calib_packv5_033123_0516.root, FC#4, port A1
Entries 165
Mean 38.04
Std Dev 27.45
Turn on : 53.4730
Width : 3.494
Height : 10.209
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

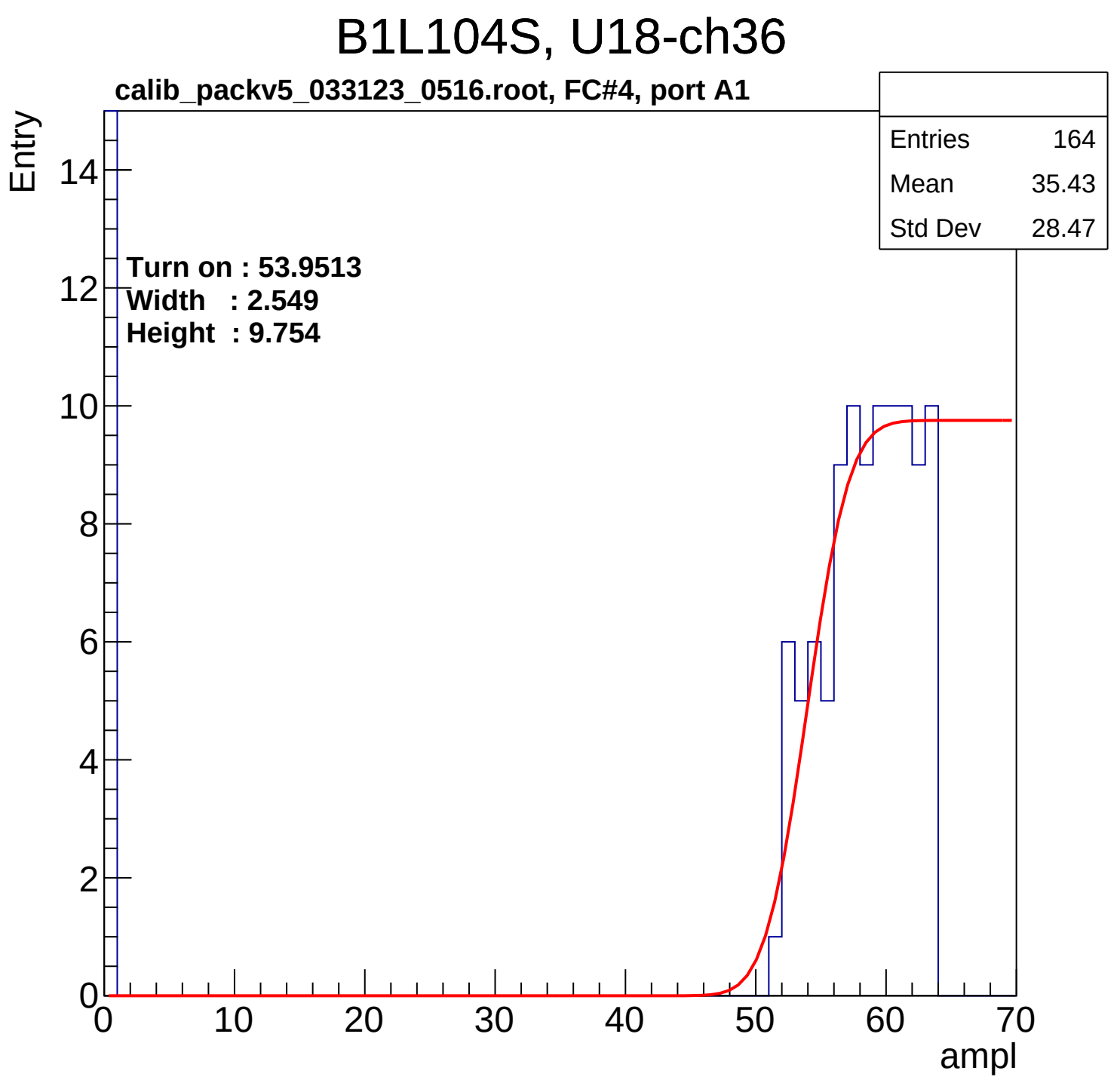

B1L104S, U18-ch31
calib_packv5_033123_0516.root, FC#4, port A1
Entries 166
Mean 38.21
Std Dev 27.42
Turn on : 52.2662
Width : 2.796
Height : 9.612
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

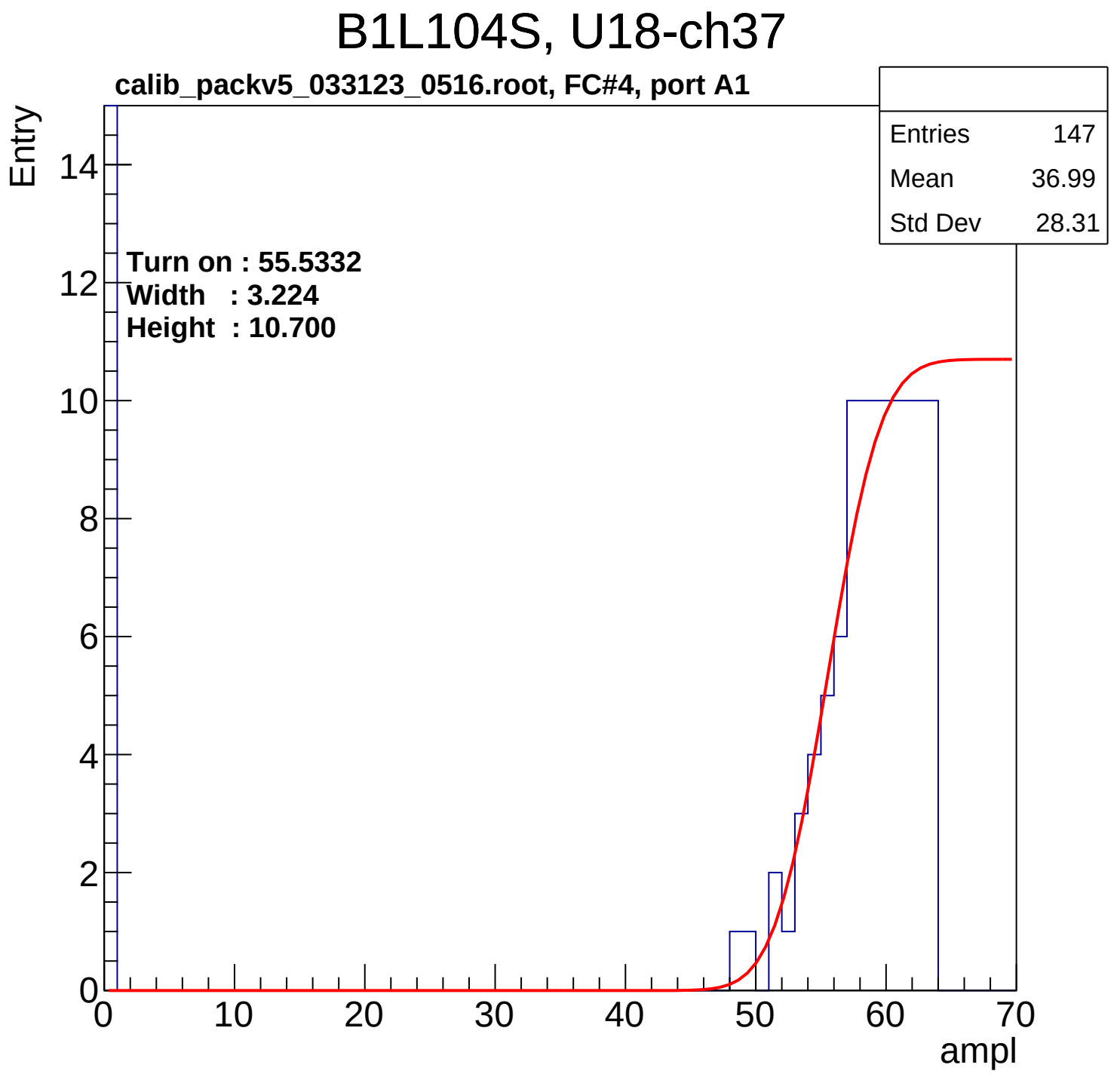

B1L104S, U18-ch32
calib_packv5_033123_0516.root, FC#4, port A1
Entries 212
Mean 33.78
Std Dev 28.1
Turn on : 51.5222
Width : 4.361
Height : 10.354
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

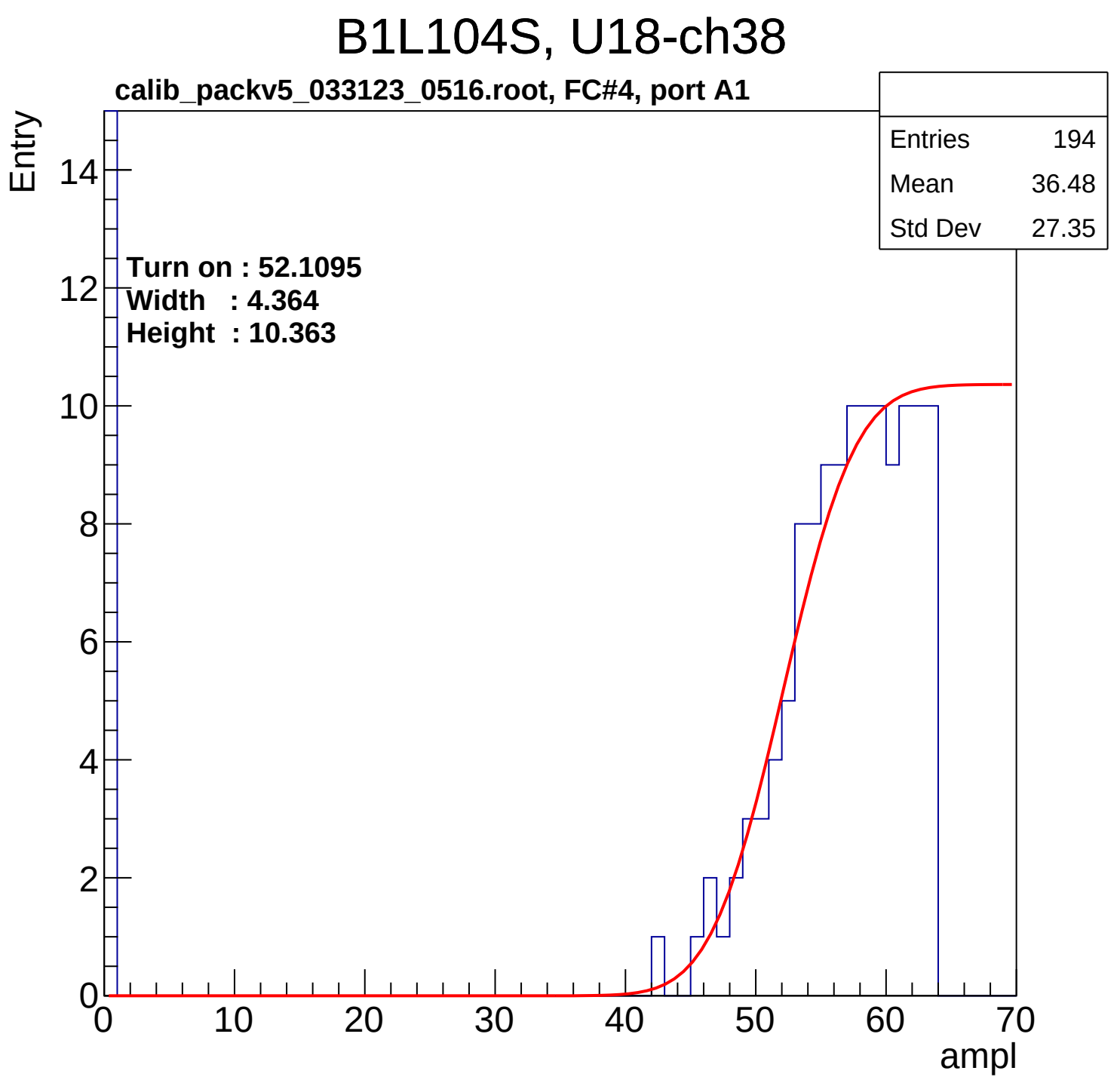

B1L104S, U18-ch33
calib_packv5_033123_0516.root, FC#4, port A1
Entries 153
Mean 39.14
Std Dev 27.4
Turn on : 54.1473
Width : 1.899
Height : 9.987
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

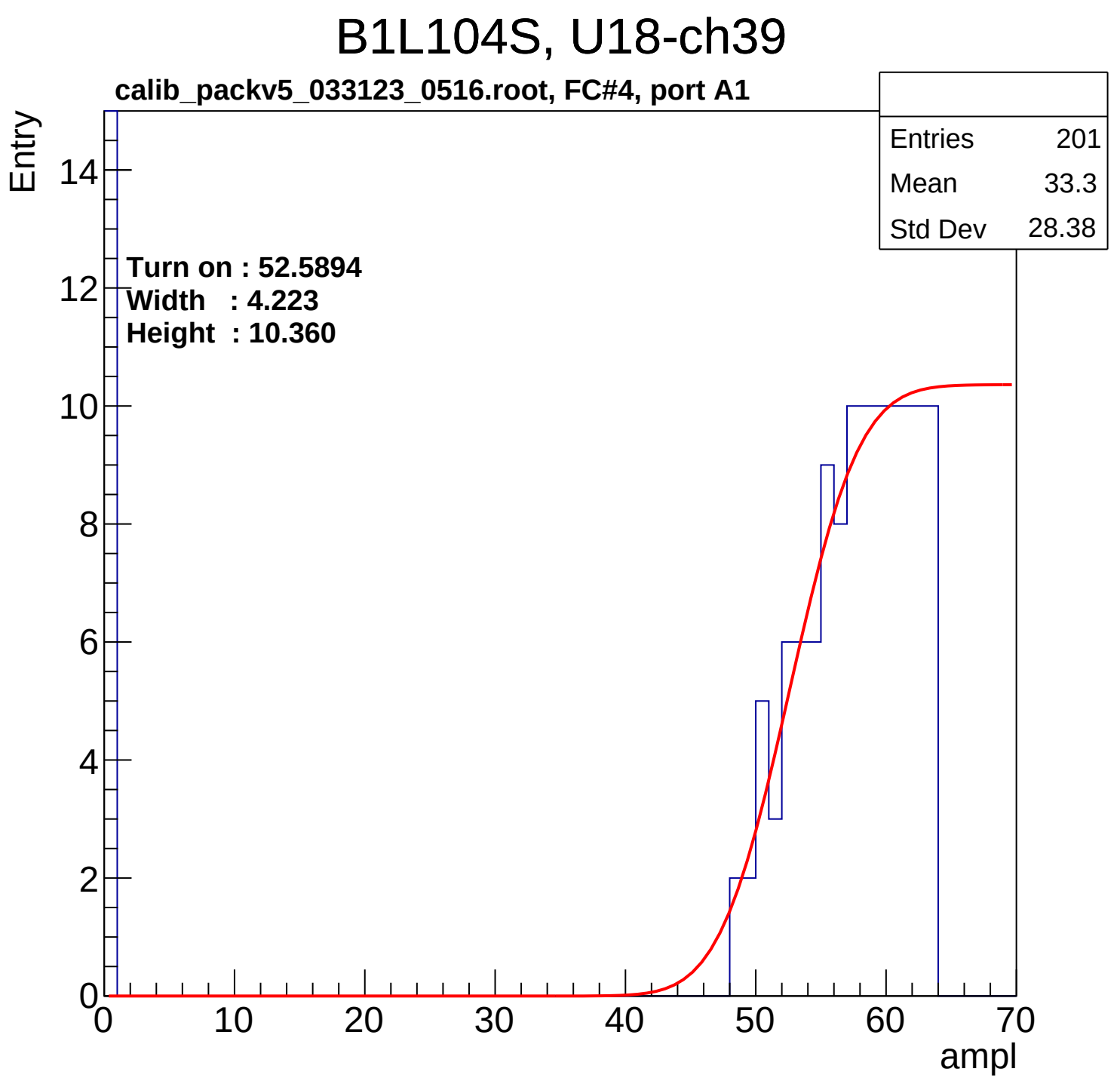

B1L104S, U18-ch34
calib_packv5_033123_0516.root, FC#4, port A1
Entries 157
Mean 31.77
Std Dev 29.34
Turn on : 56.5207
Width : 3.515
Height : 10.111
Entry
ampl
0
10
20
30
40
50
60
70

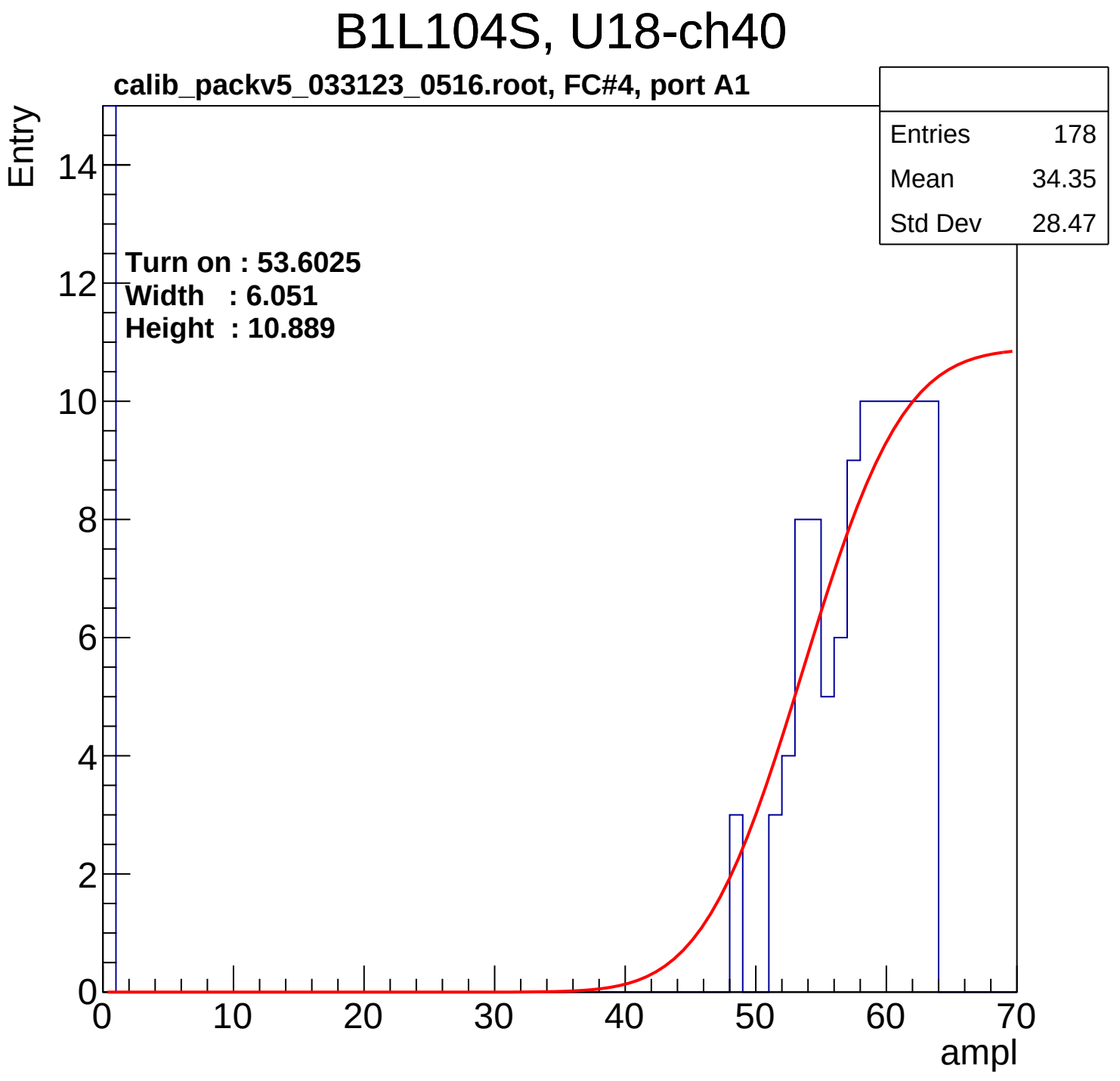

B1L104S, U18-ch35
calib_packv5_033123_0516.root, FC#4, port A1
Entries 166
Mean 32.37
Std Dev 29.15
Turn on : 54.9556
Width : 1.527
Height : 9.648
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

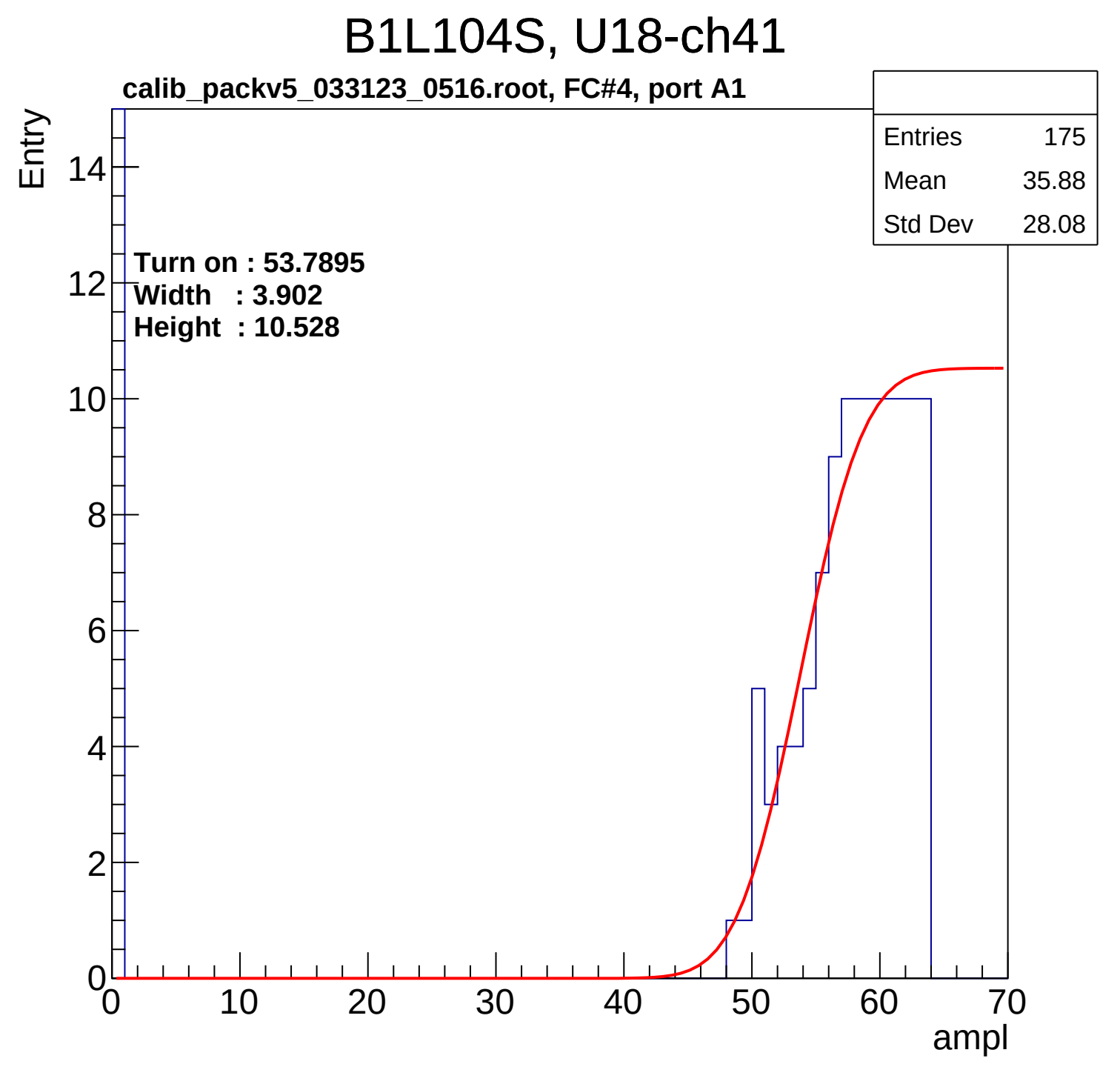

B1L104S, U18-ch36
calib_packv5_033123_0516.root, FC#4, port A1
Entries 164
Mean 35.43
Std Dev 28.47
Turn on : 53.9513
Width : 2.549
Height : 9.754
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

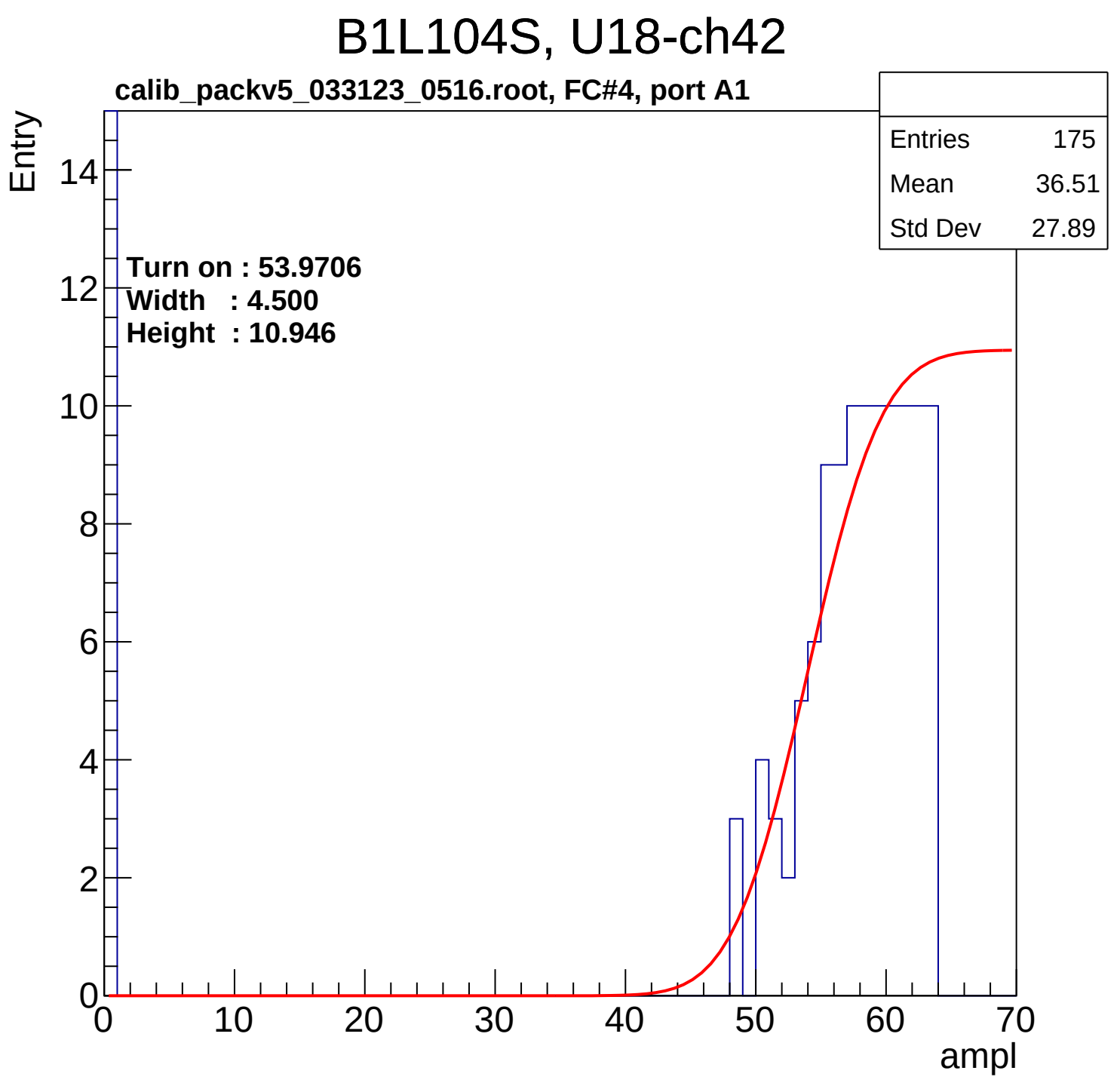

B1L104S, U18-ch37
calib_packv5_033123_0516.root, FC#4, port A1
Entries 147
Mean 36.99
Std Dev 28.31
Turn on : 55.5332
Width : 3.224
Height : 10.700
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

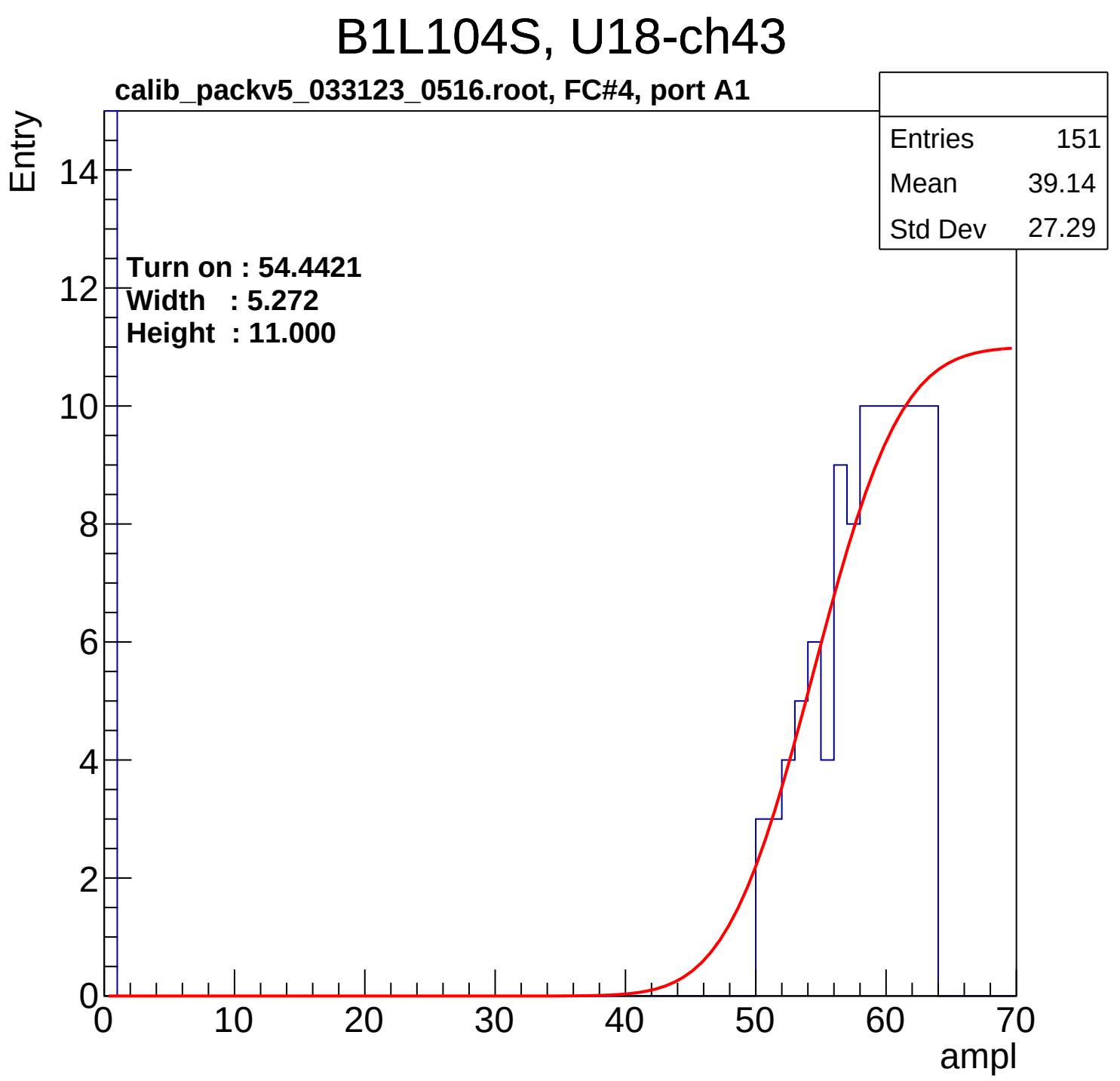

B1L104S, U18-ch38
calib_packv5_033123_0516.root, FC#4, port A1
Entries 194
Mean 36.48
Std Dev 27.35
Turn on : 52.1095
Width : 4.364
Height : 10.363
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

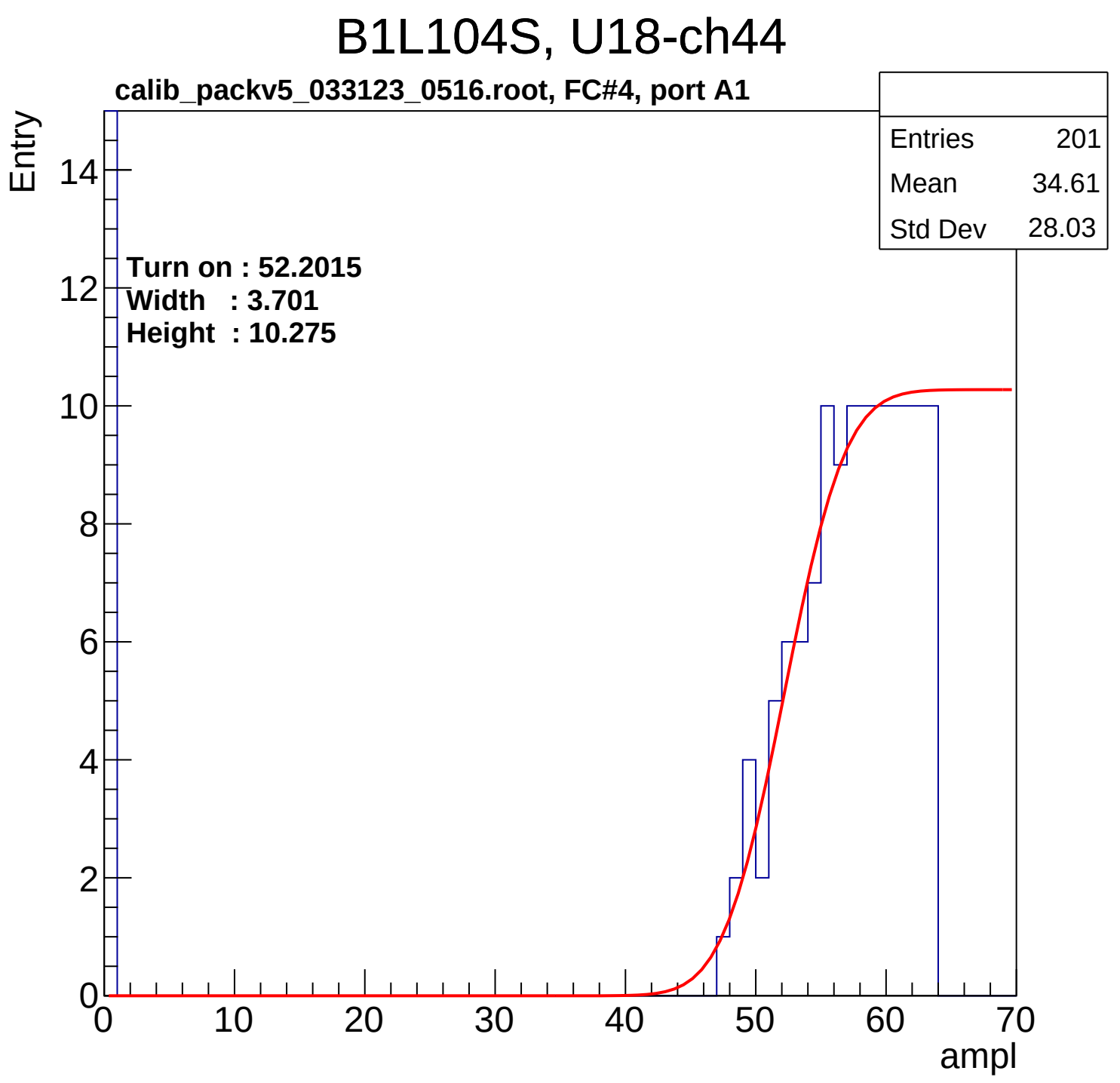

B1L104S, U18-ch39
calib_packv5_033123_0516.root, FC#4, port A1
Entries 201
Mean 33.3
Std Dev 28.38
Turn on : 52.5894
Width : 4.223
Height : 10.360
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

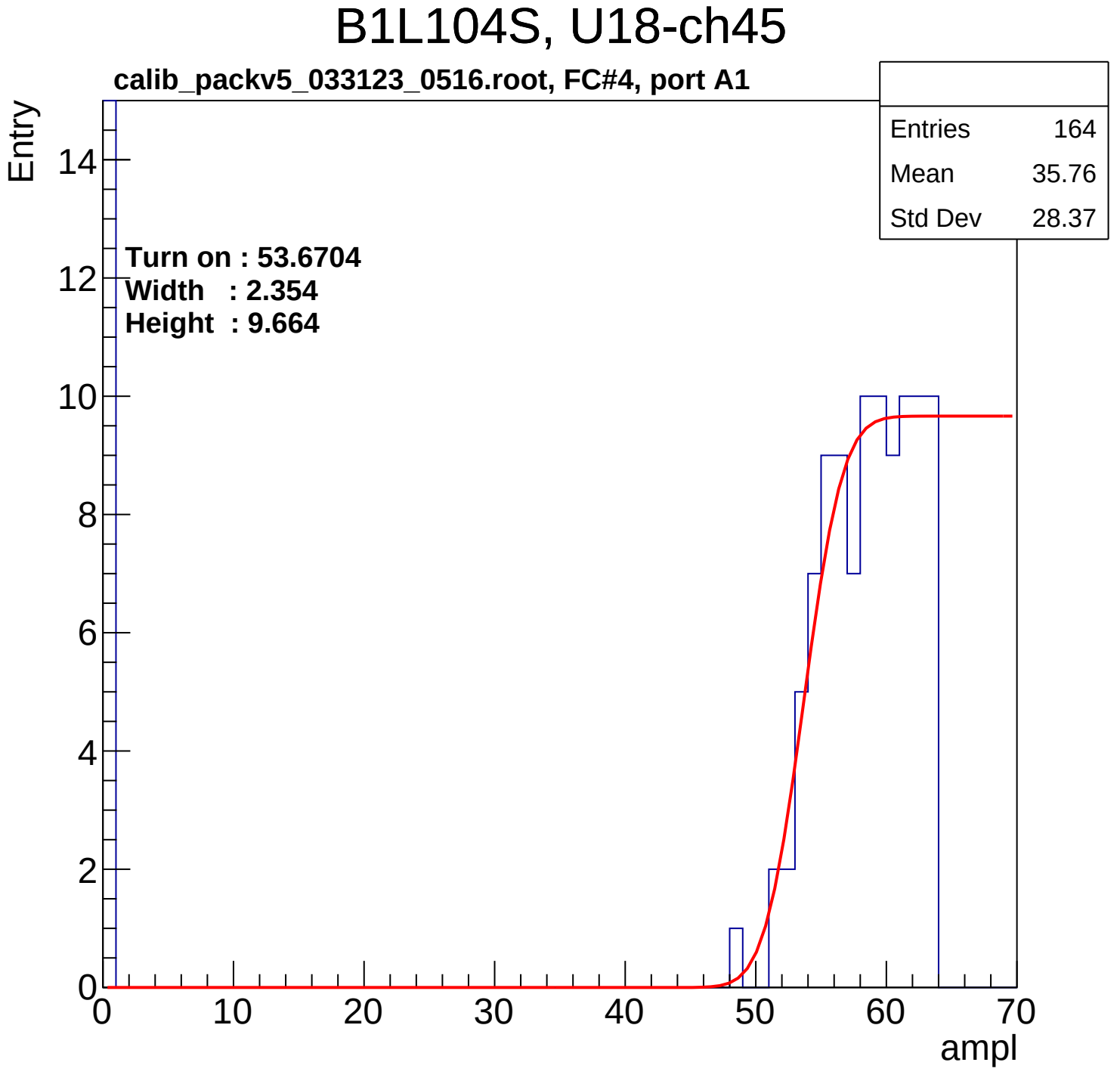

B1L104S, U18-ch40
calib_packv5_033123_0516.root, FC#4, port A1
Entries 178
Mean 34.35
Std Dev 28.47
Turn on : 53.6025
Width : 6.051
Height : 10.889
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

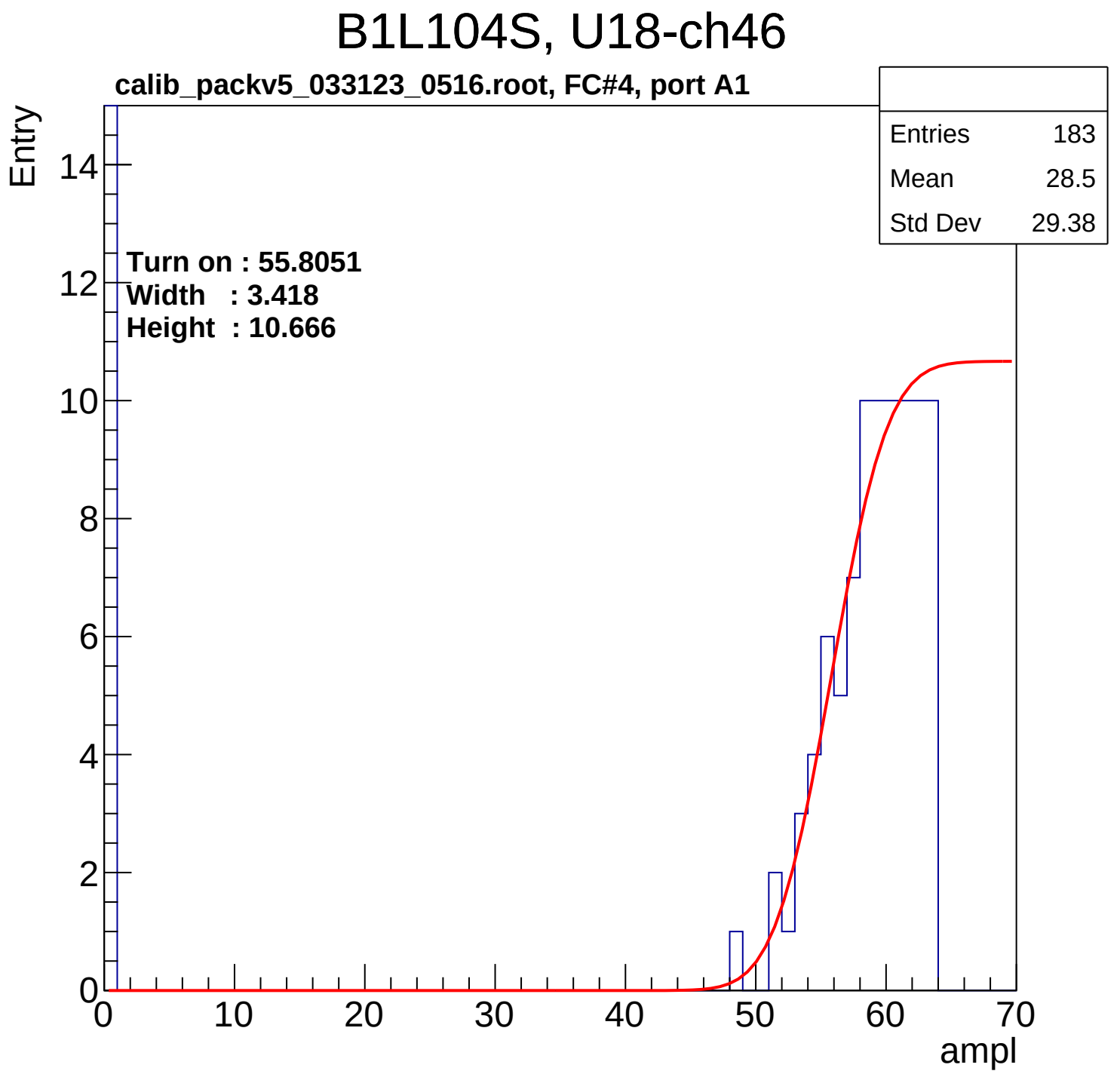

B1L104S, U18-ch41
calib_packv5_033123_0516.root, FC#4, port A1
Entries 175
Mean 35.88
Std Dev 28.08
Turn on : 53.7895
Width : 3.902
Height : 10.528
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

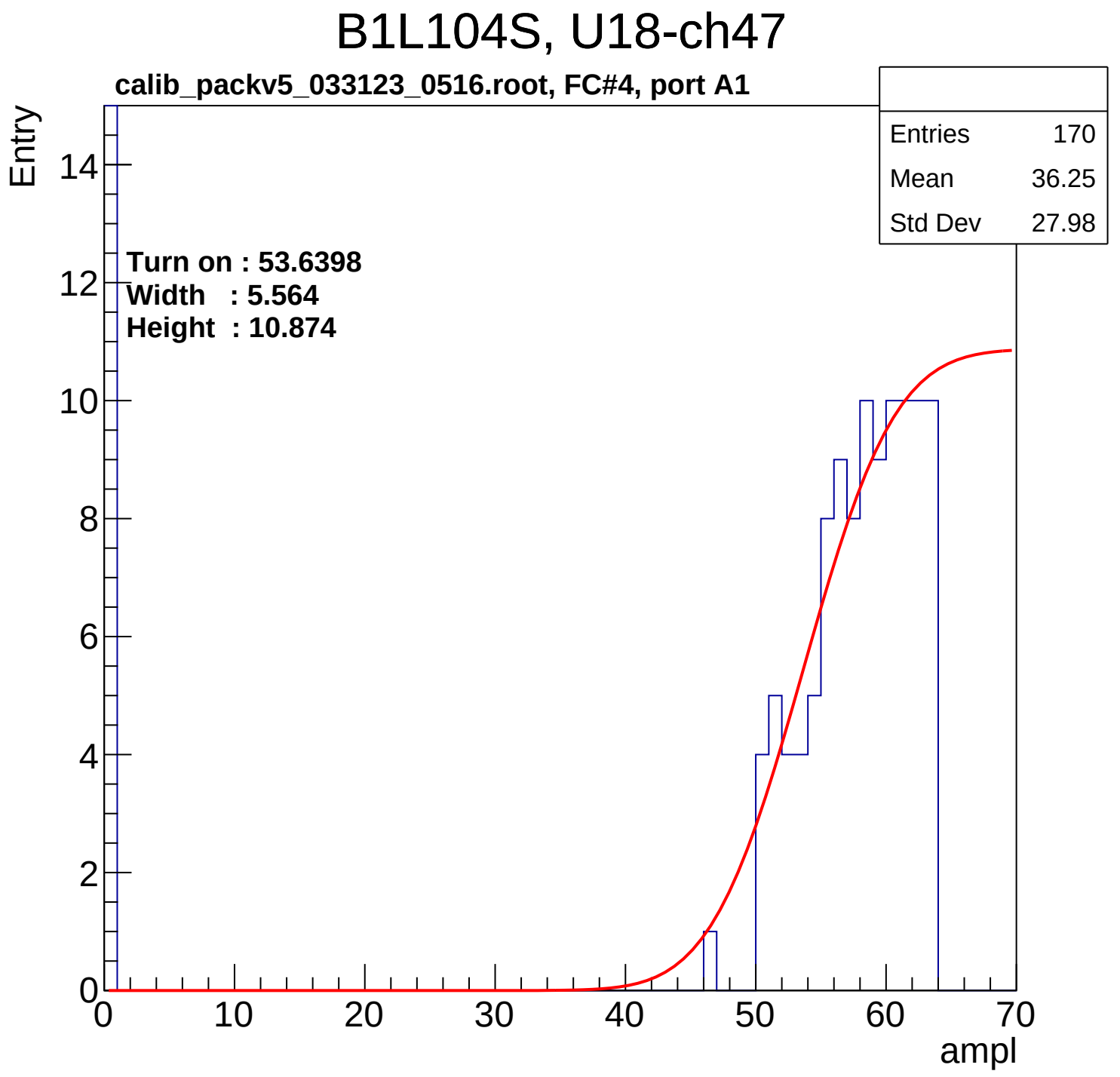

B1L104S, U18-ch42
calib_packv5_033123_0516.root, FC#4, port A1
Entries 175
Mean 36.51
Std Dev 27.89
Turn on : 53.9706
Width : 4.500
Height : 10.946
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

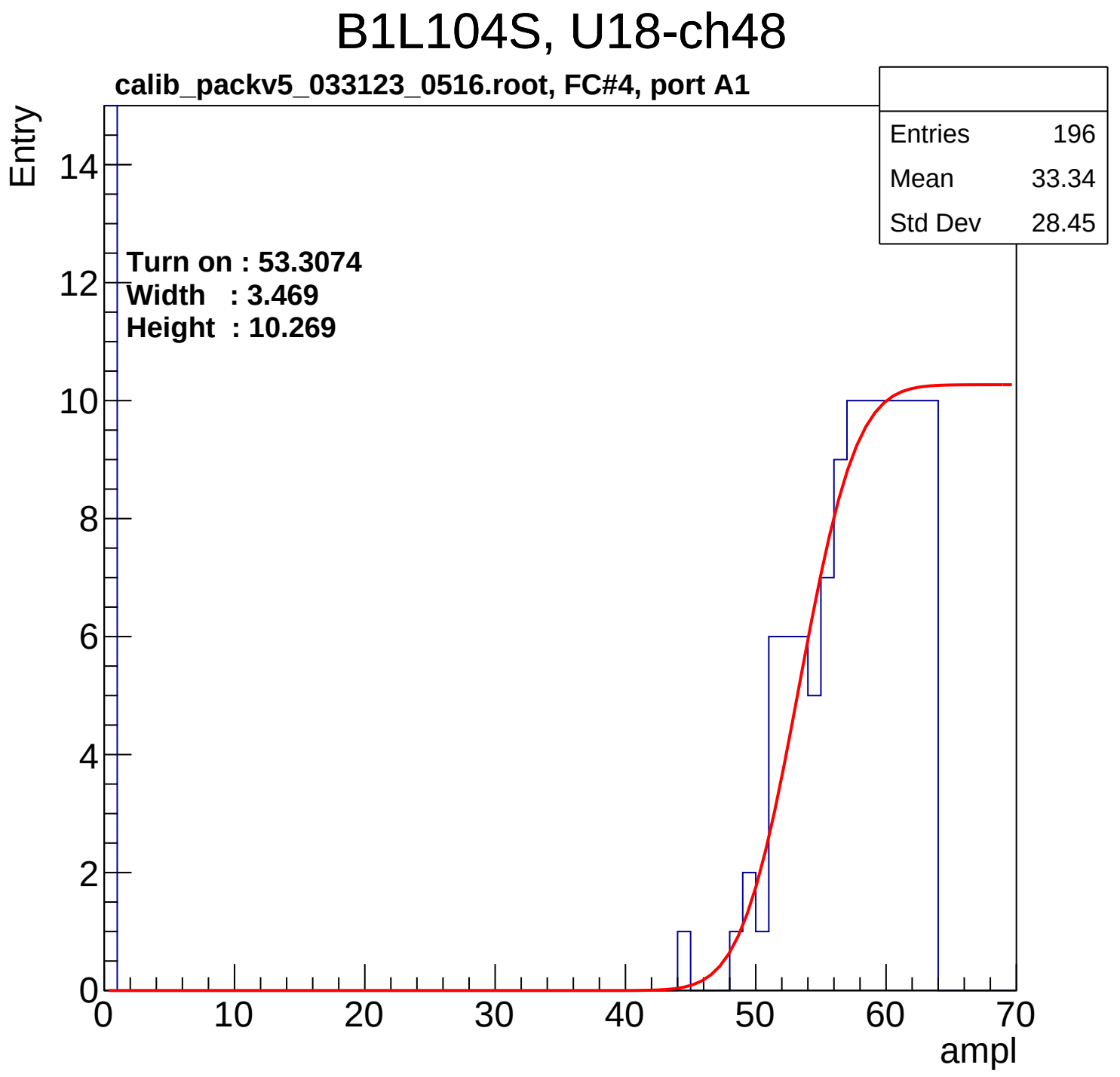

B1L104S, U18-ch43
calib_packv5_033123_0516.root, FC#4, port A1
Entries 151
Mean 39.14
Std Dev 27.29
Turn on : 54.4421
Width : 5.272
Height : 11.000
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

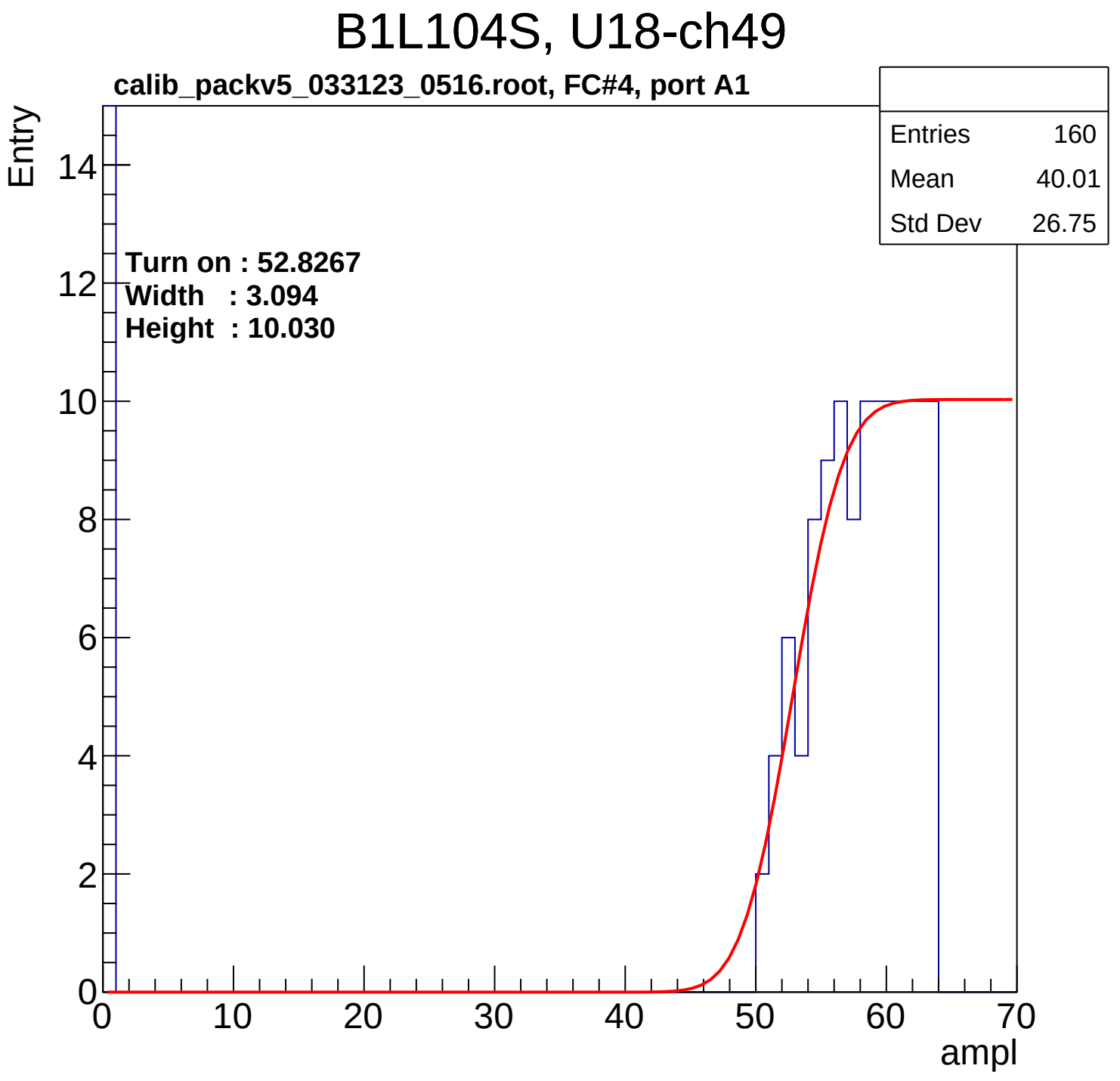

B1L104S, U18-ch44
calib_packv5_033123_0516.root, FC#4, port A1
Entries 201
Mean 34.61
Std Dev 28.03
Turn on : 52.2015
Width : 3.701
Height : 10.275
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

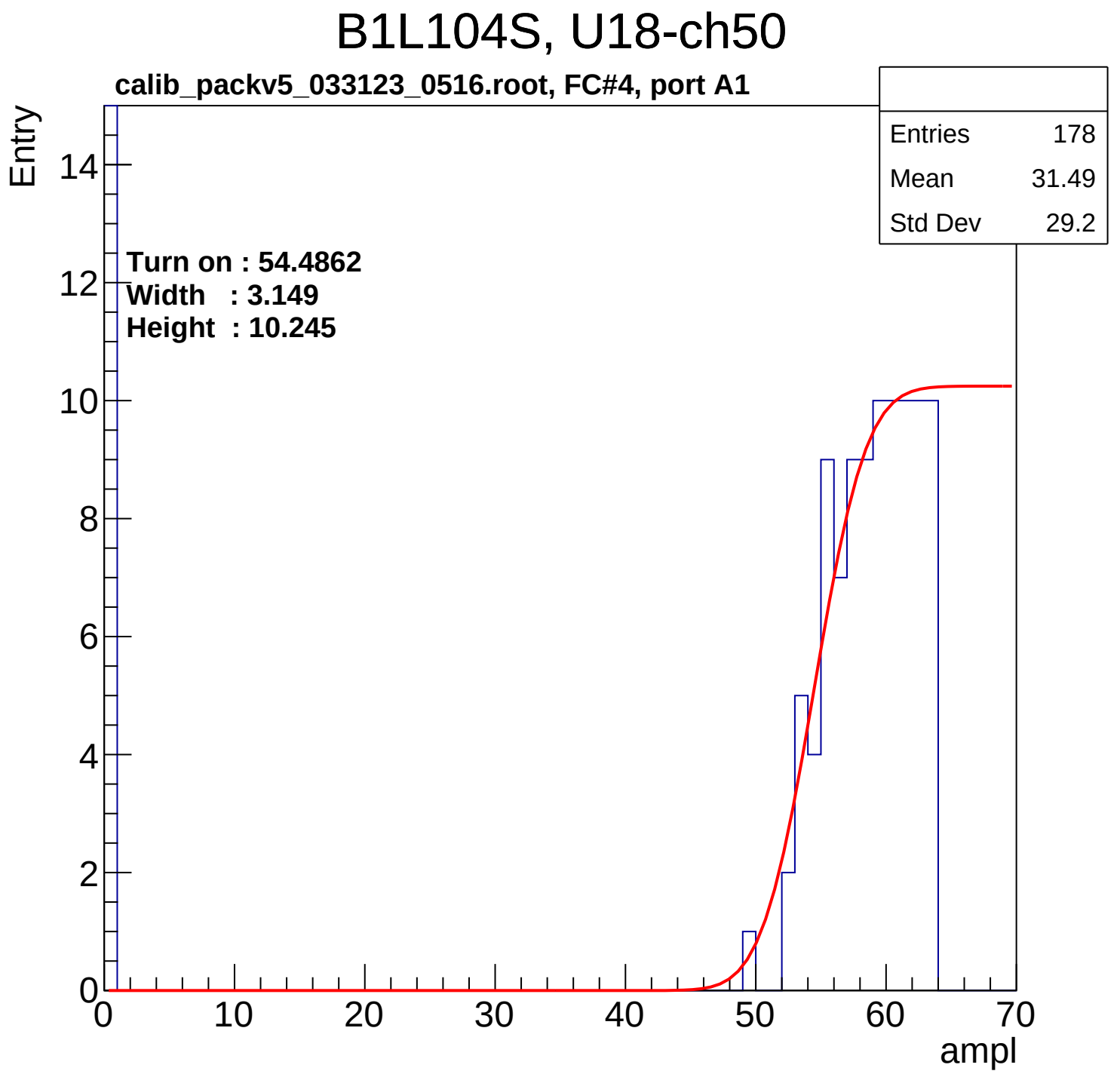

B1L104S, U18-ch45
calib_packv5_033123_0516.root, FC#4, port A1
Entries 164
Mean 35.76
Std Dev 28.37
Turn on : 53.6704
Width : 2.354
Height : 9.664
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

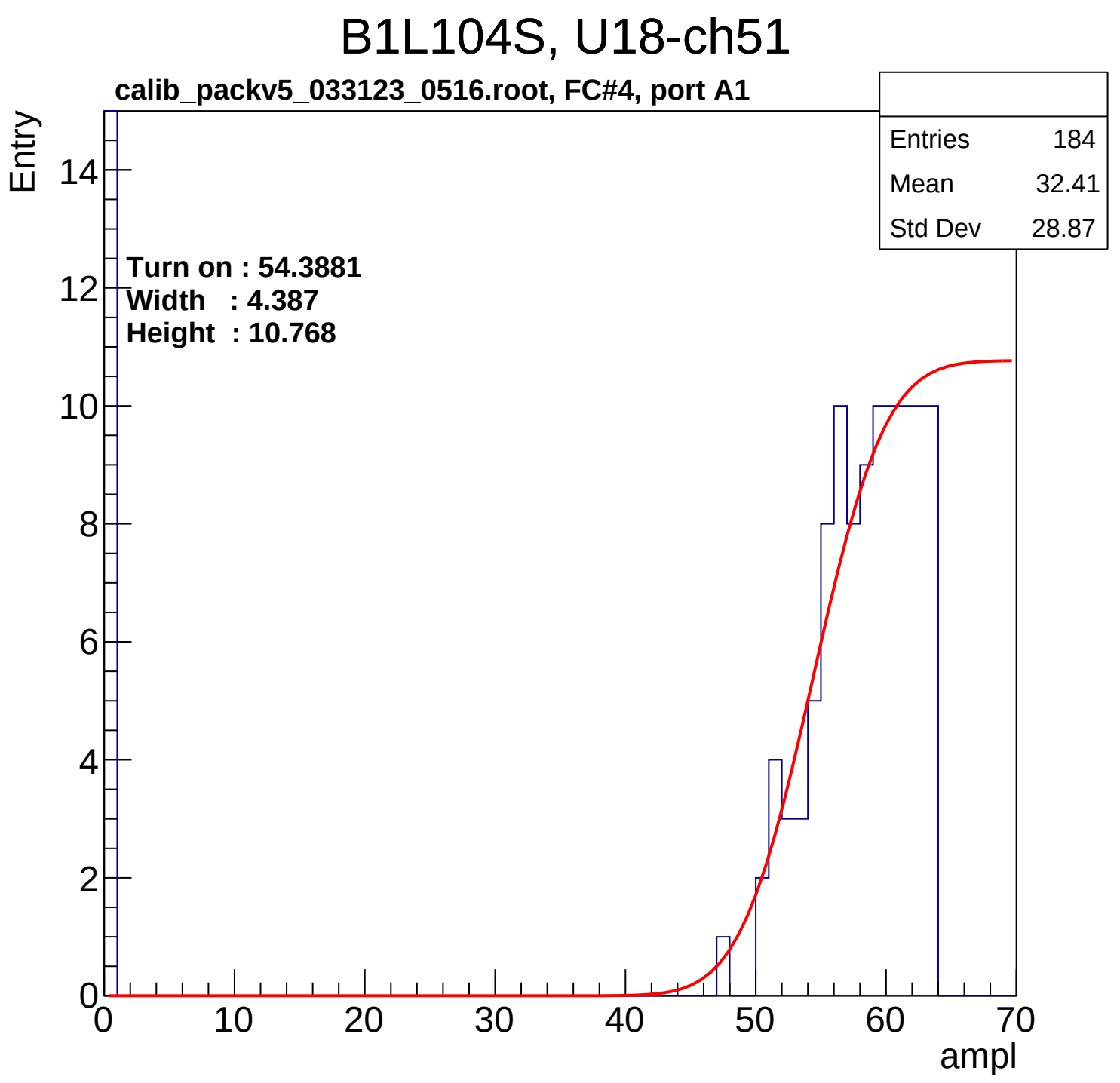

B1L104S, U18-ch46
calib_packv5_033123_0516.root, FC#4, port A1
Entries 183
Mean 28.5
Std Dev 29.38
Turn on : 55.8051
Width : 3.418
Height : 10.666
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

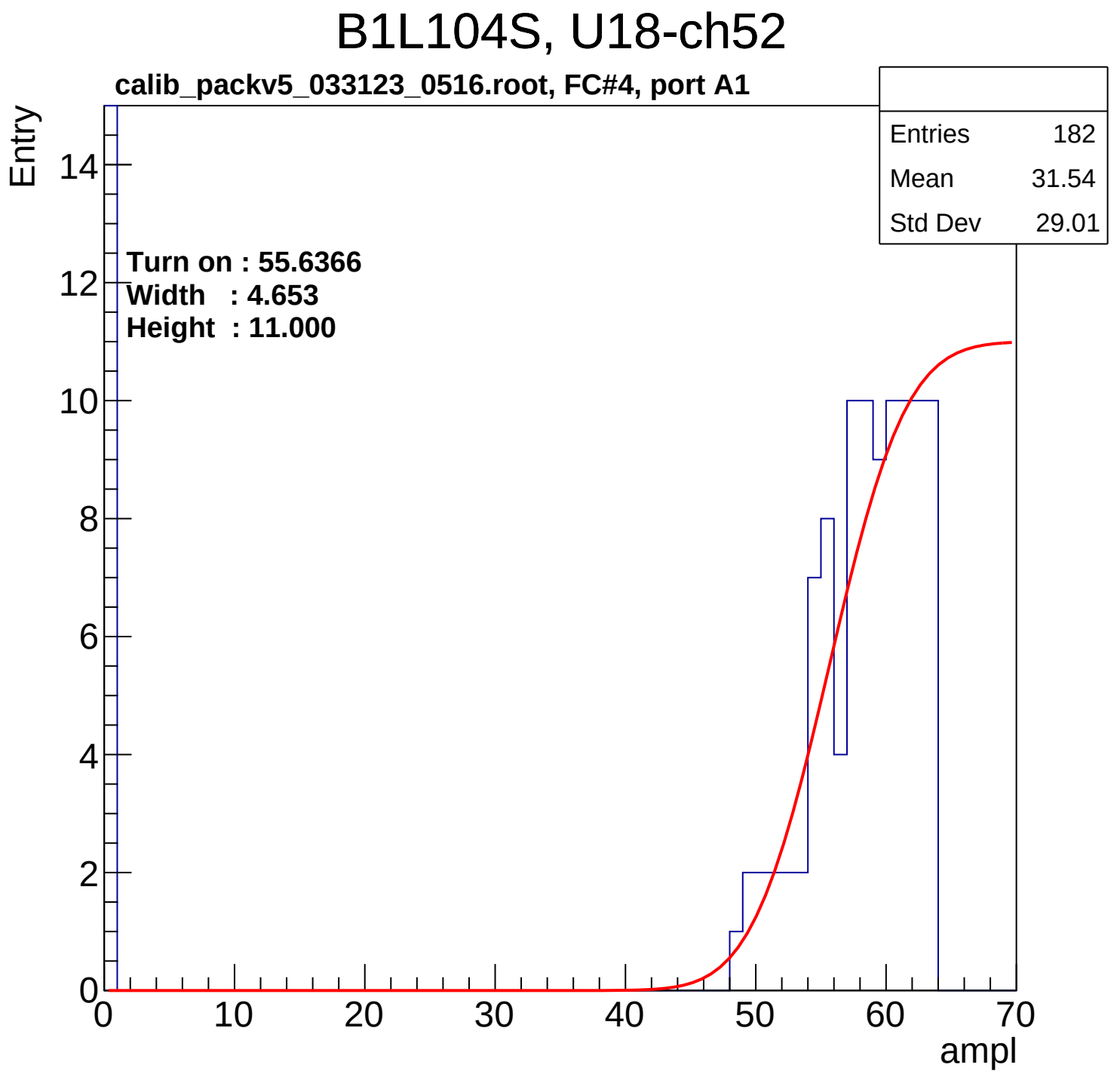

B1L104S, U18-ch47
calib_packv5_033123_0516.root, FC#4, port A1
Entries 170
Mean 36.25
Std Dev 27.98
Turn on : 53.6398
Width : 5.564
Height : 10.874
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

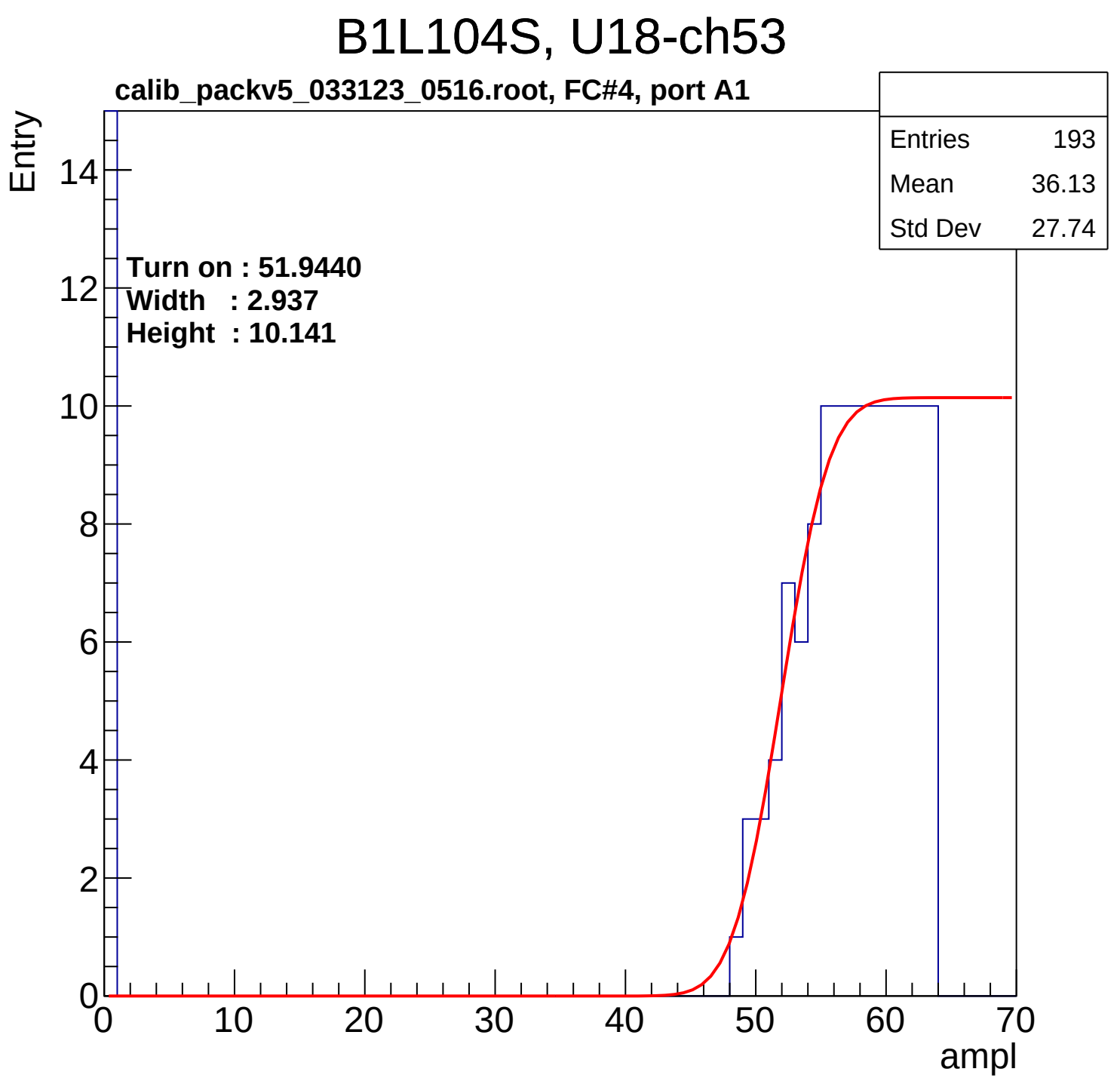

B1L104S, U18-ch48
calib_packv5_033123_0516.root, FC#4, port A1
Entries 196
Mean 33.34
Std Dev 28.45
Turn on : 53.3074
Width : 3.469
Height : 10.269
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

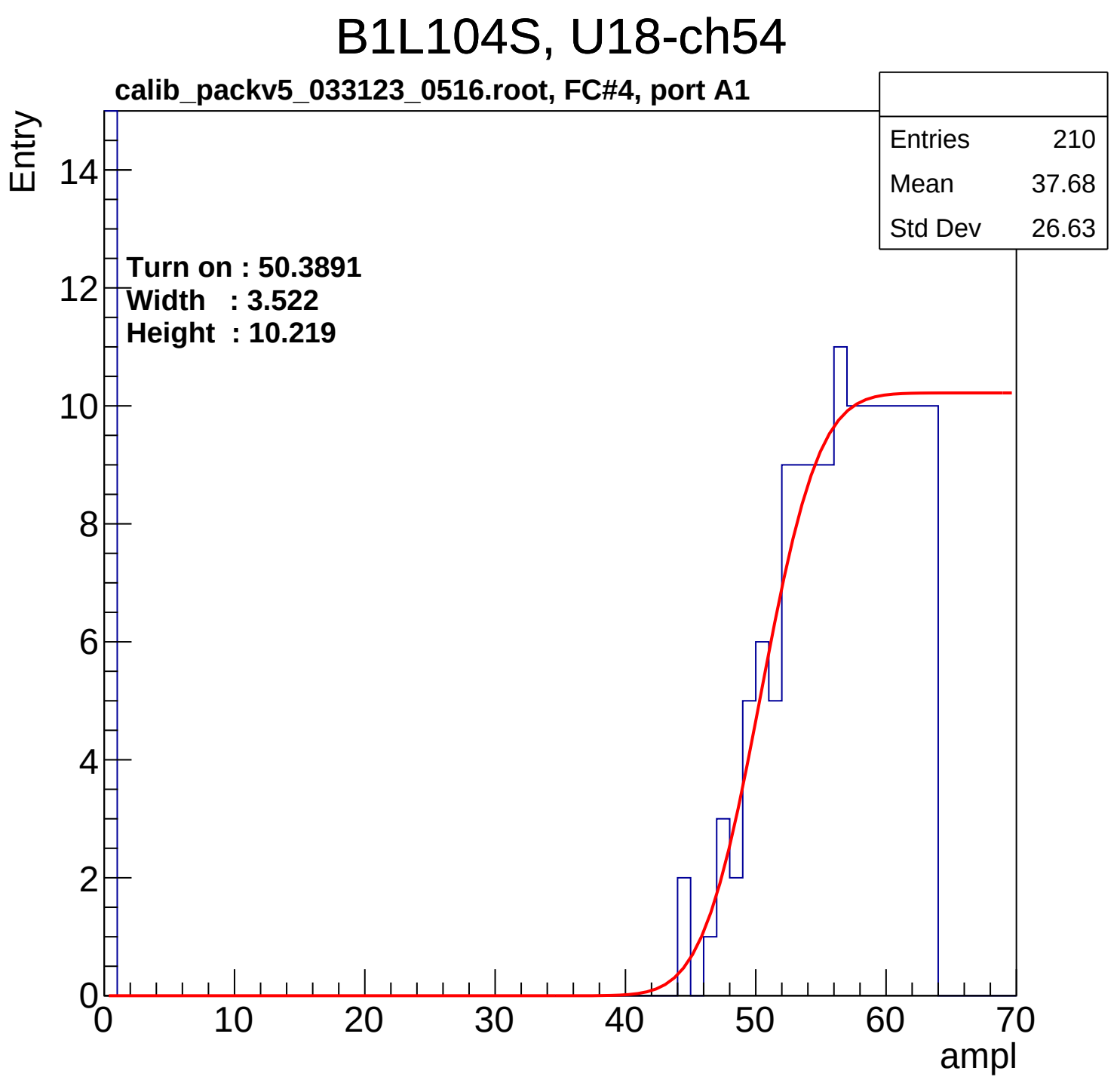

B1L104S, U18-ch49
calib_packv5_033123_0516.root, FC#4, port A1
Entries 160
Mean 40.01
Std Dev 26.75
Turn on : 52.8267
Width : 3.094
Height : 10.030
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

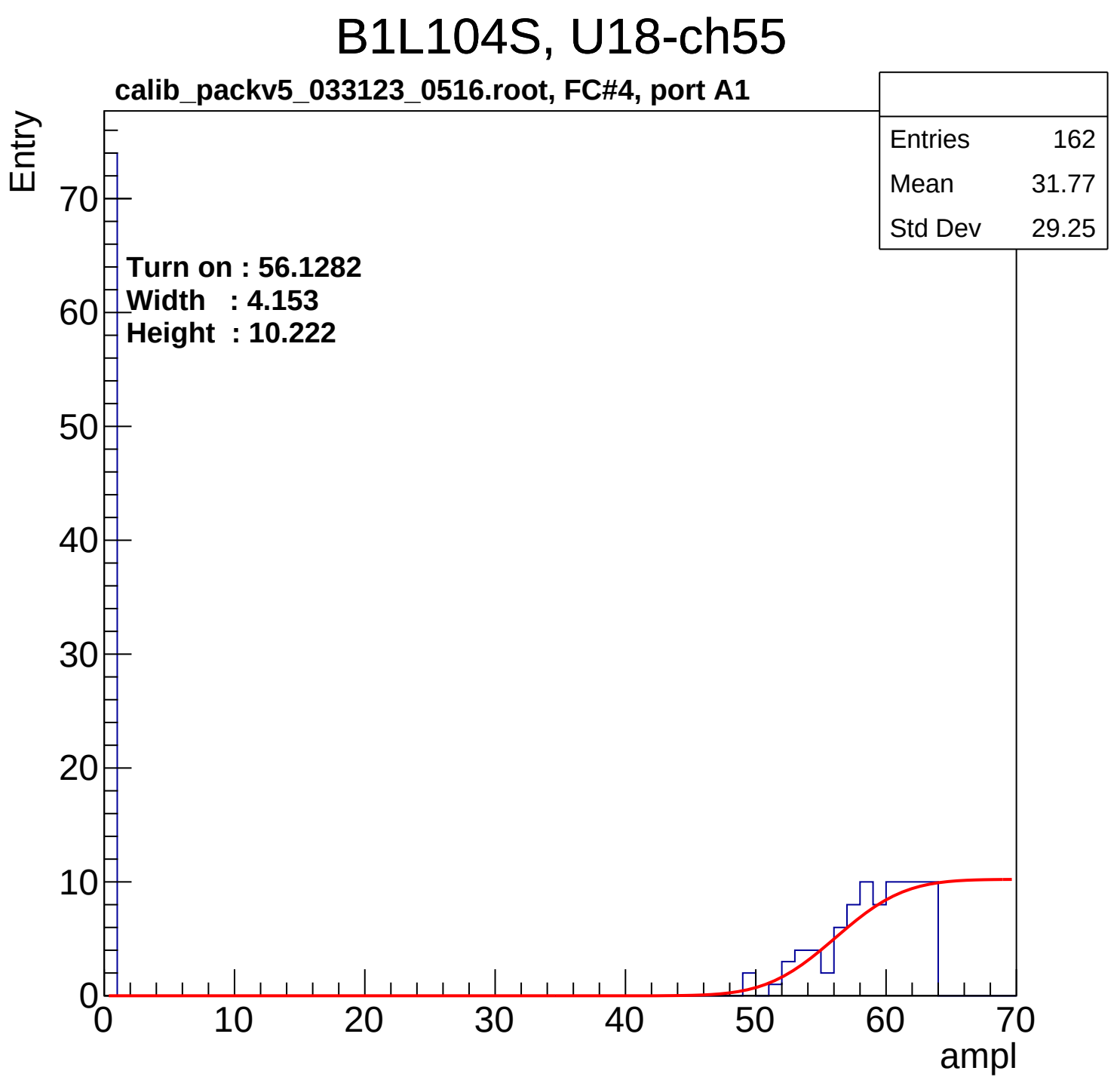

B1L104S, U18-ch50
calib_packv5_033123_0516.root, FC#4, port A1
Entries 178
Mean 31.49
Std Dev 29.2
Turn on : 54.4862
Width : 3.149
Height : 10.245
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

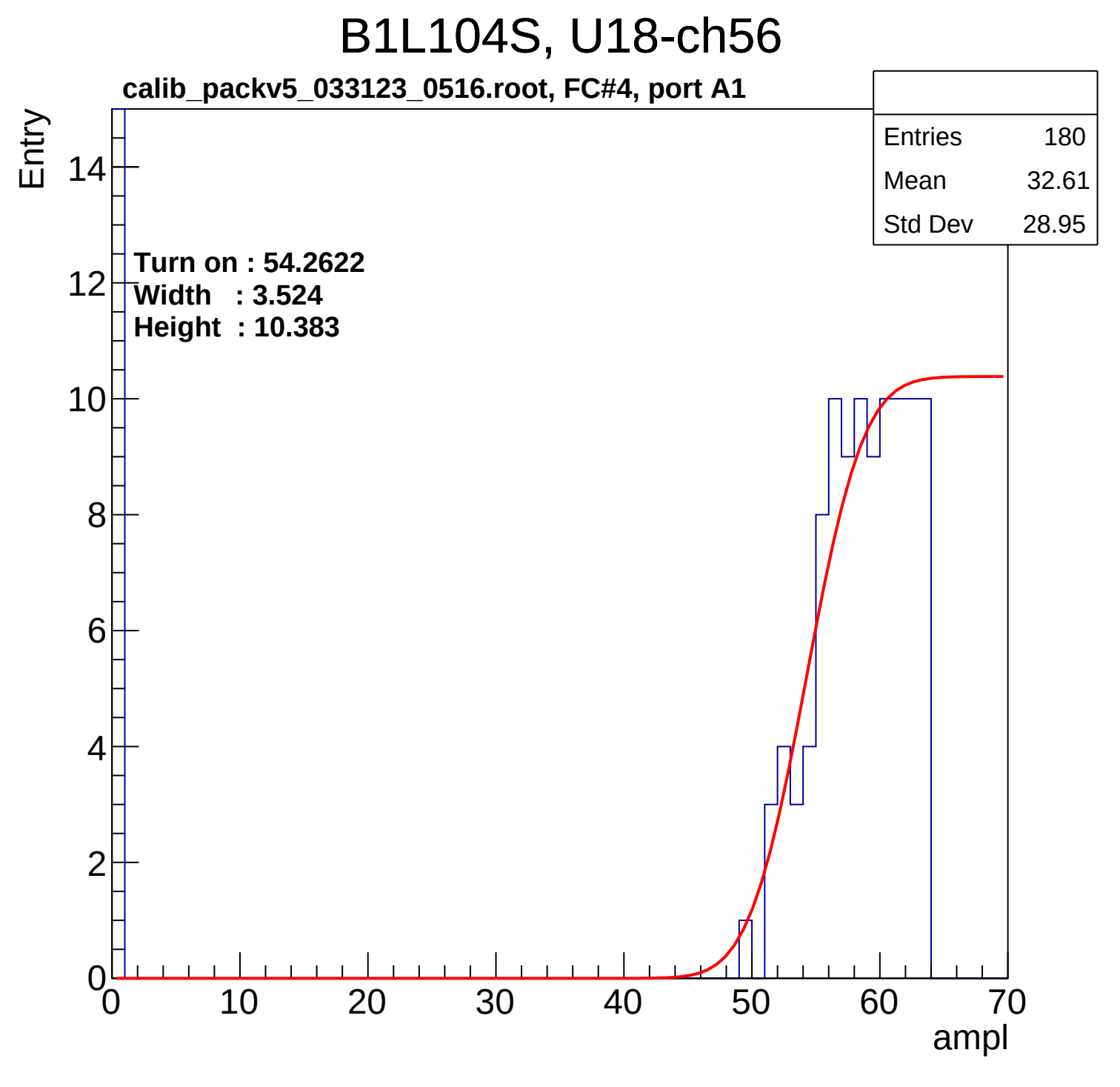

B1L104S, U18-ch51
calib_packv5_033123_0516.root, FC#4, port A1
Entries 184
Mean 32.41
Std Dev 28.87
Turn on : 54.3881
Width : 4.387
Height : 10.768
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

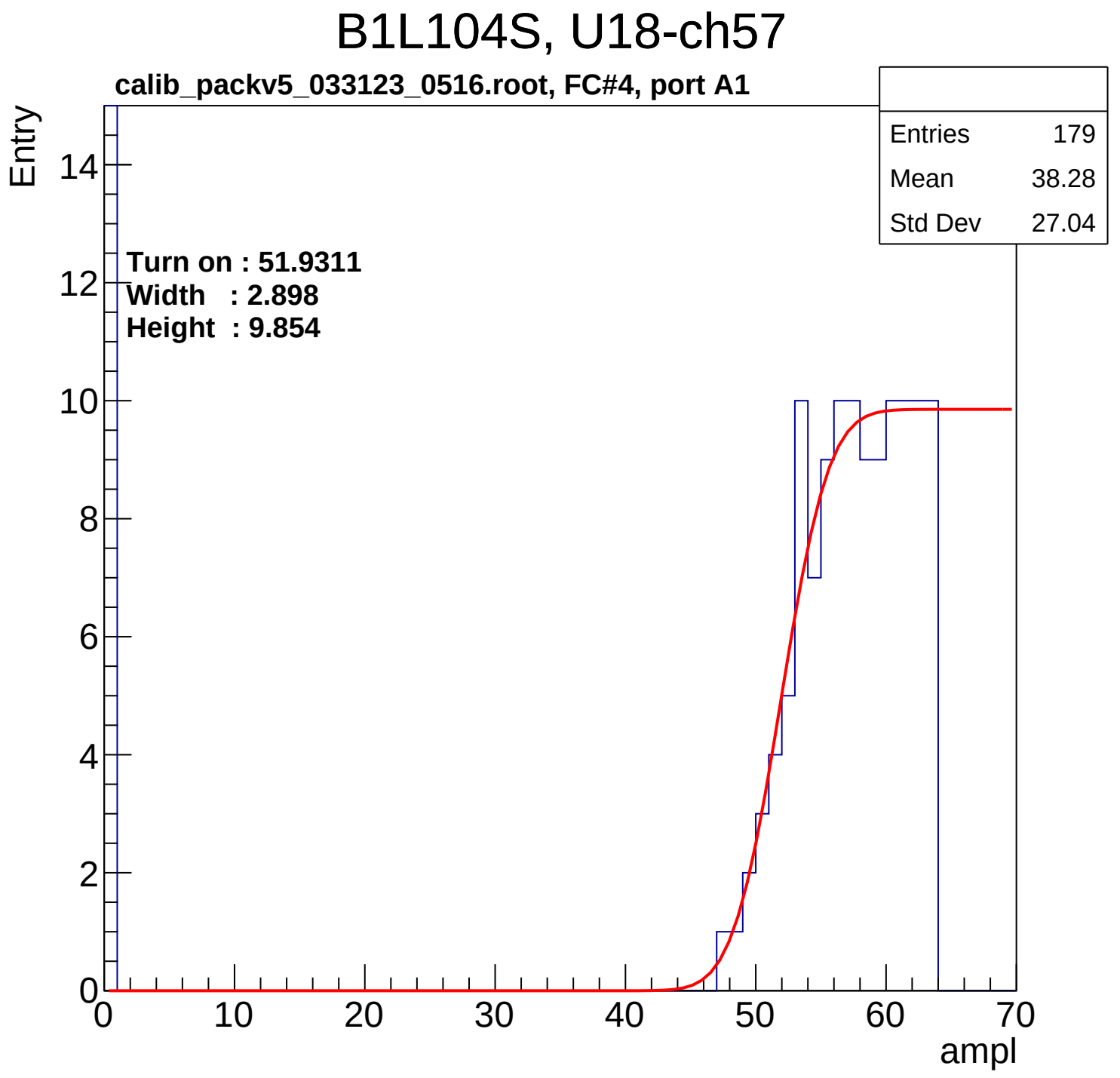

B1L104S, U18-ch52
calib_packv5_033123_0516.root, FC#4, port A1
Entries 182
Mean 31.54
Std Dev 29.01
Turn on : 55.6366
Width : 4.653
Height : 11.000
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

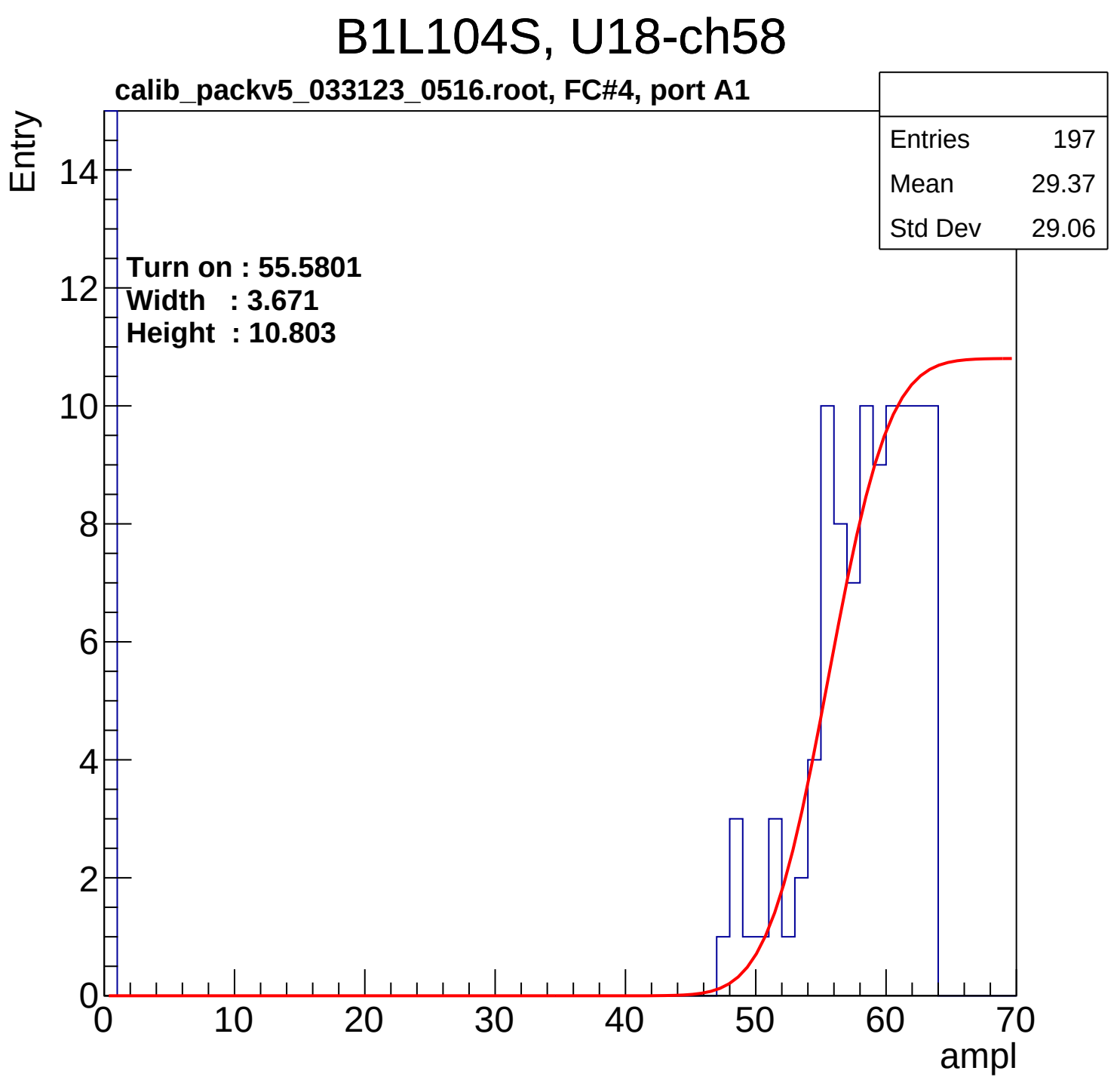

B1L104S, U18-ch53
calib_packv5_033123_0516.root, FC#4, port A1
Entries 193
Mean 36.13
Std Dev 27.74
Turn on : 51.9440
Width : 2.937
Height : 10.141
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

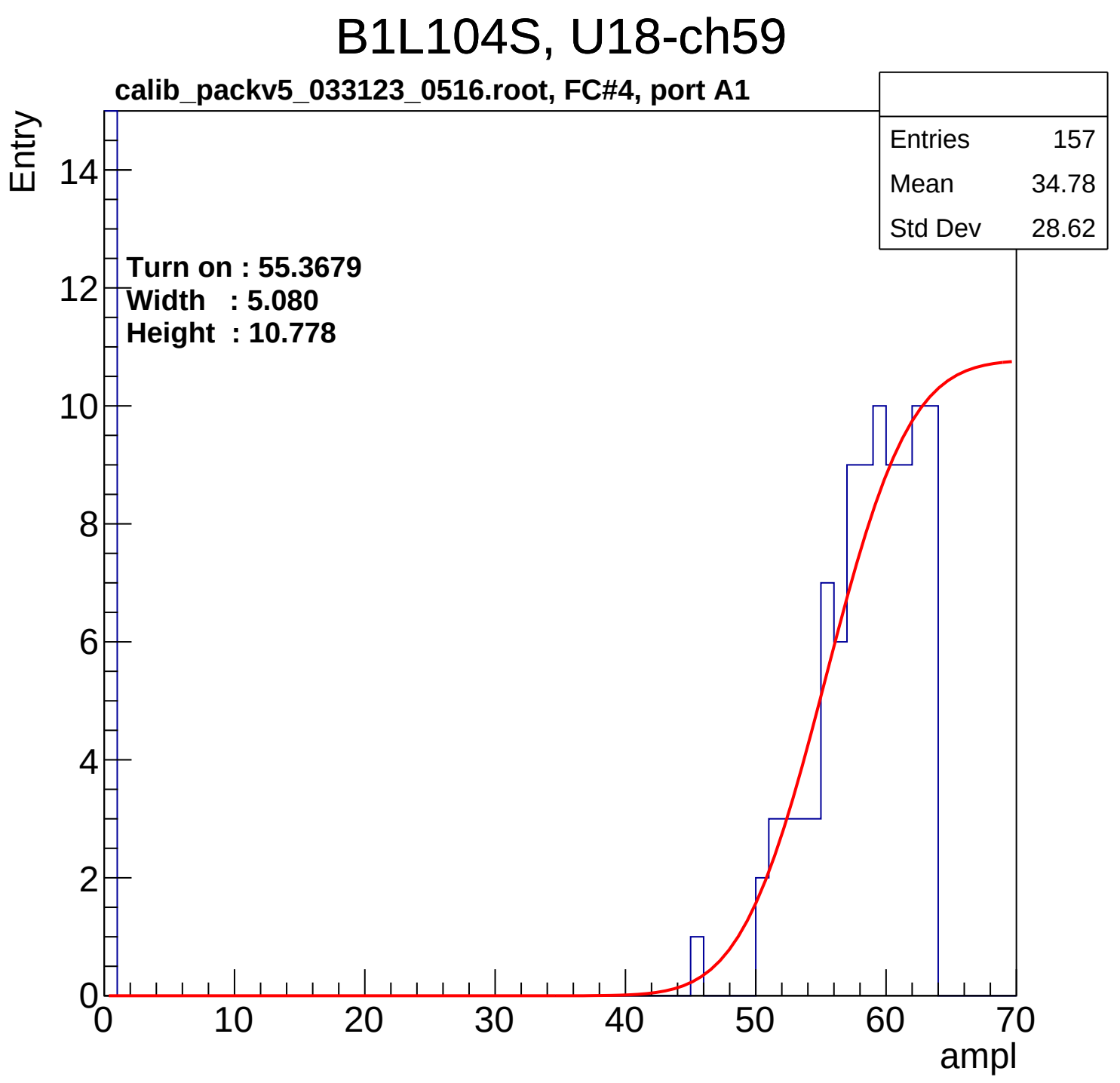

B1L104S, U18-ch54
calib_packv5_033123_0516.root, FC#4, port A1
Entries 210
Mean 37.68
Std Dev 26.63
Turn on : 50.3891
Width : 3.522
Height : 10.219
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

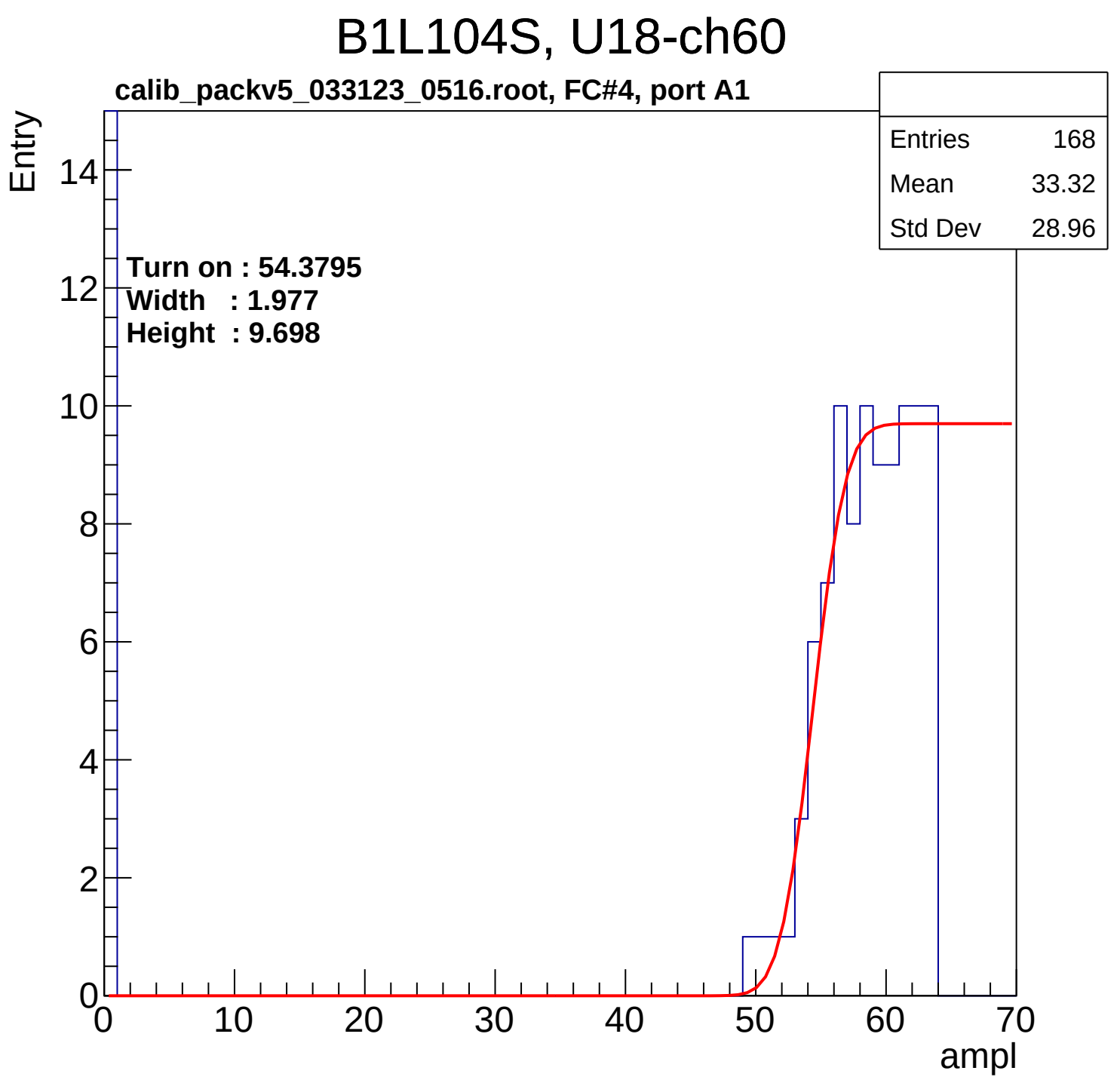

B1L104S, U18-ch55
calib_packv5_033123_0516.root, FC#4, port A1
Entries 162
Mean 31.77
Std Dev 29.25
Turn on : 56.1282
Width : 4.153
Height : 10.222
Entry
ampl
0
10
20
30
40
50
60
70

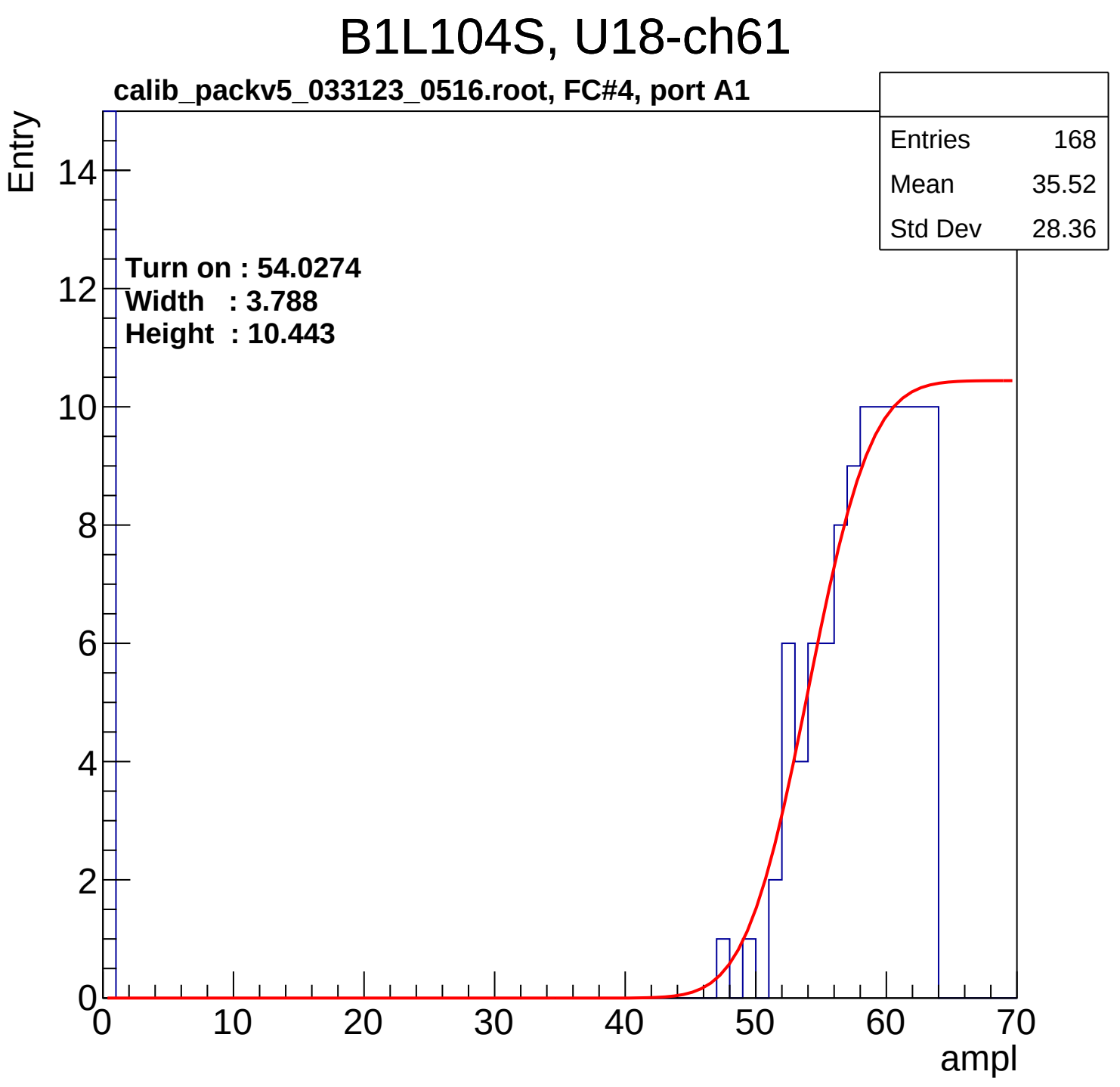

B1L104S, U18-ch56
calib_packv5_033123_0516.root, FC#4, port A1
Entries 180
Mean 32.61
Std Dev 28.95
Turn on : 54.2622
Width : 3.524
Height : 10.383
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

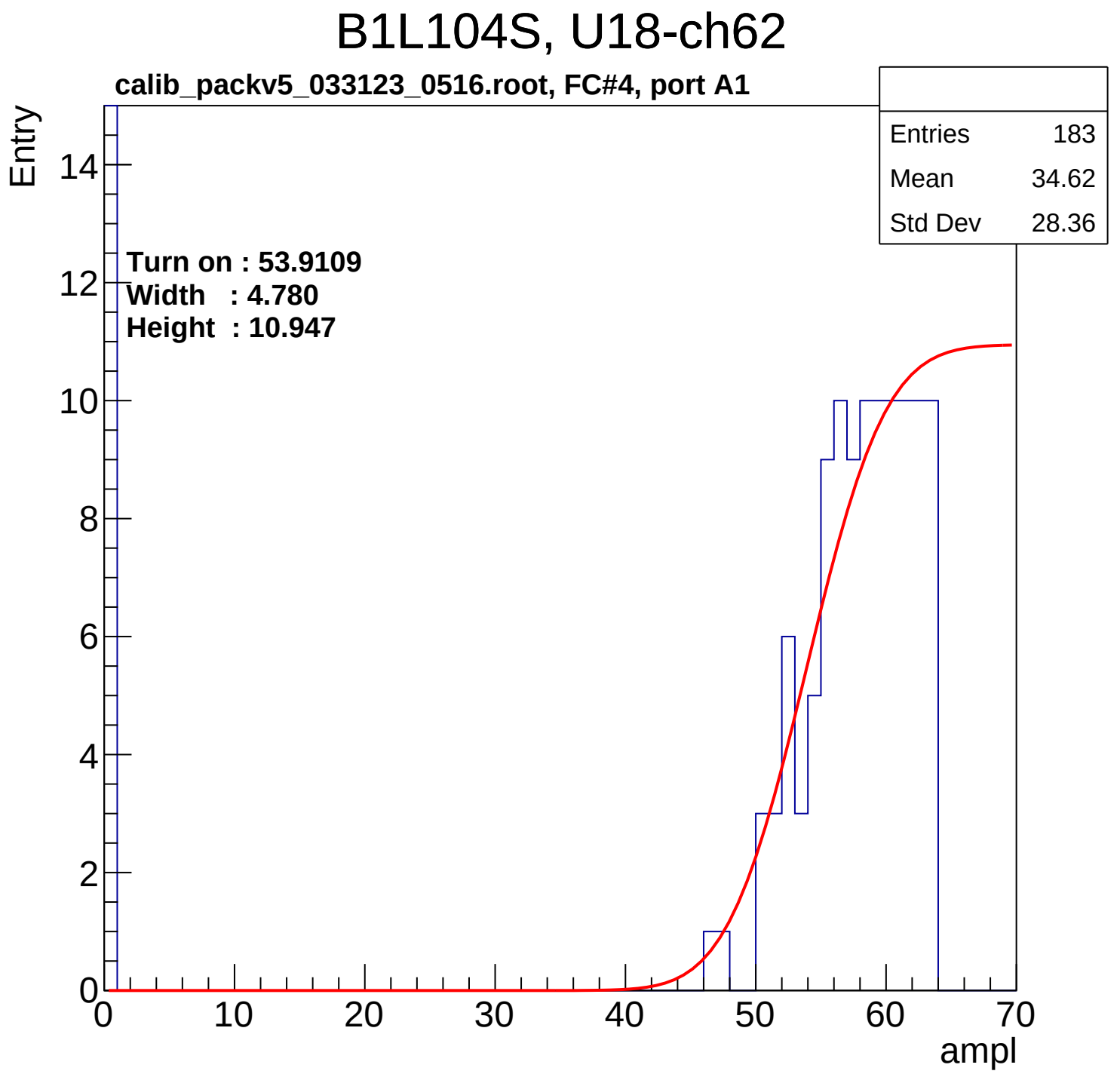

B1L104S, U18-ch57
calib_packv5_033123_0516.root, FC#4, port A1
Entries 179
Mean 38.28
Std Dev 27.04
Turn on : 51.9311
Width : 2.898
Height : 9.854
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

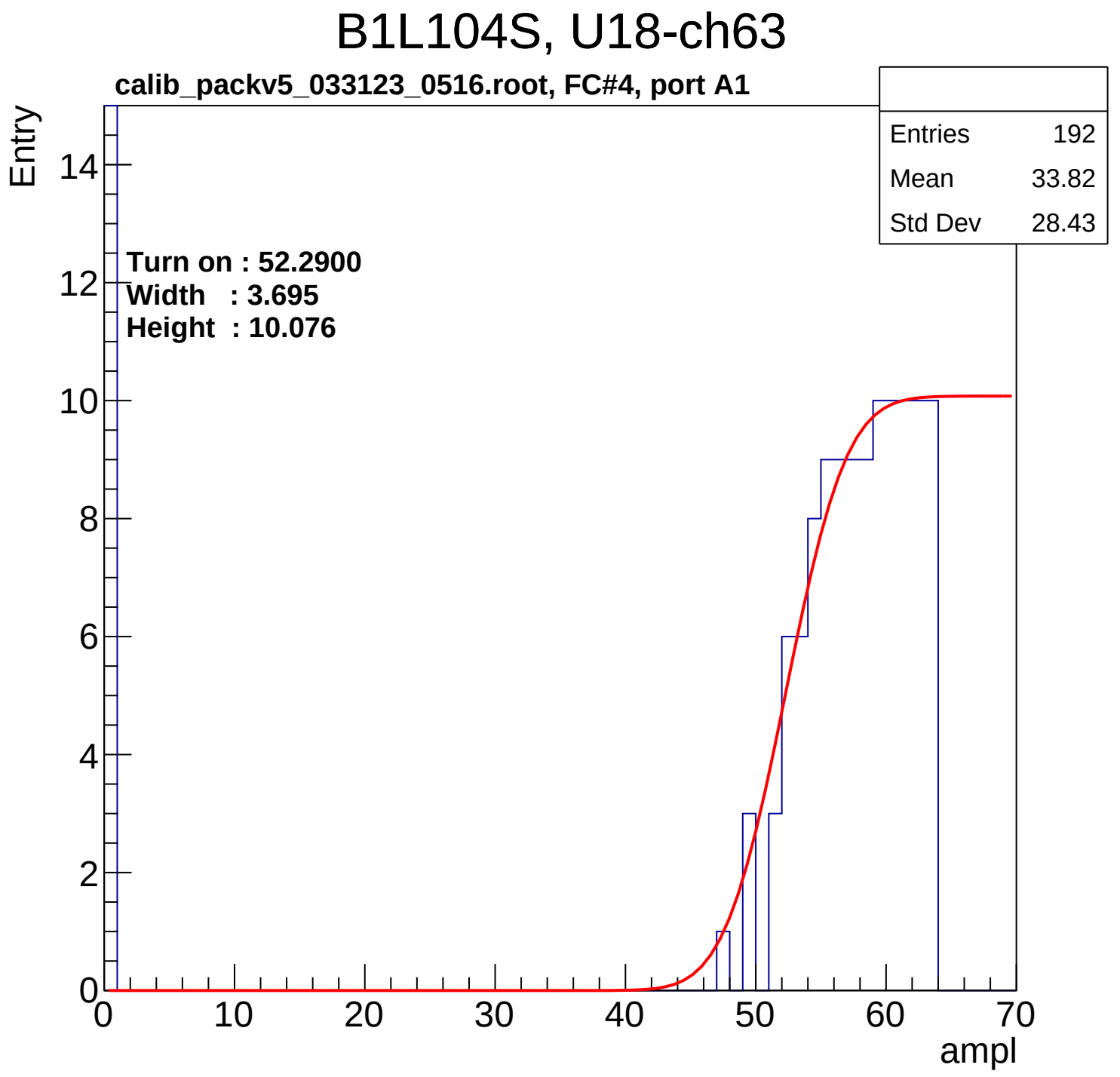

B1L104S, U18-ch58
calib_packv5_033123_0516.root, FC#4, port A1
Entries 197
Mean 29.37
Std Dev 29.06
Turn on : 55.5801
Width : 3.671
Height : 10.803
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

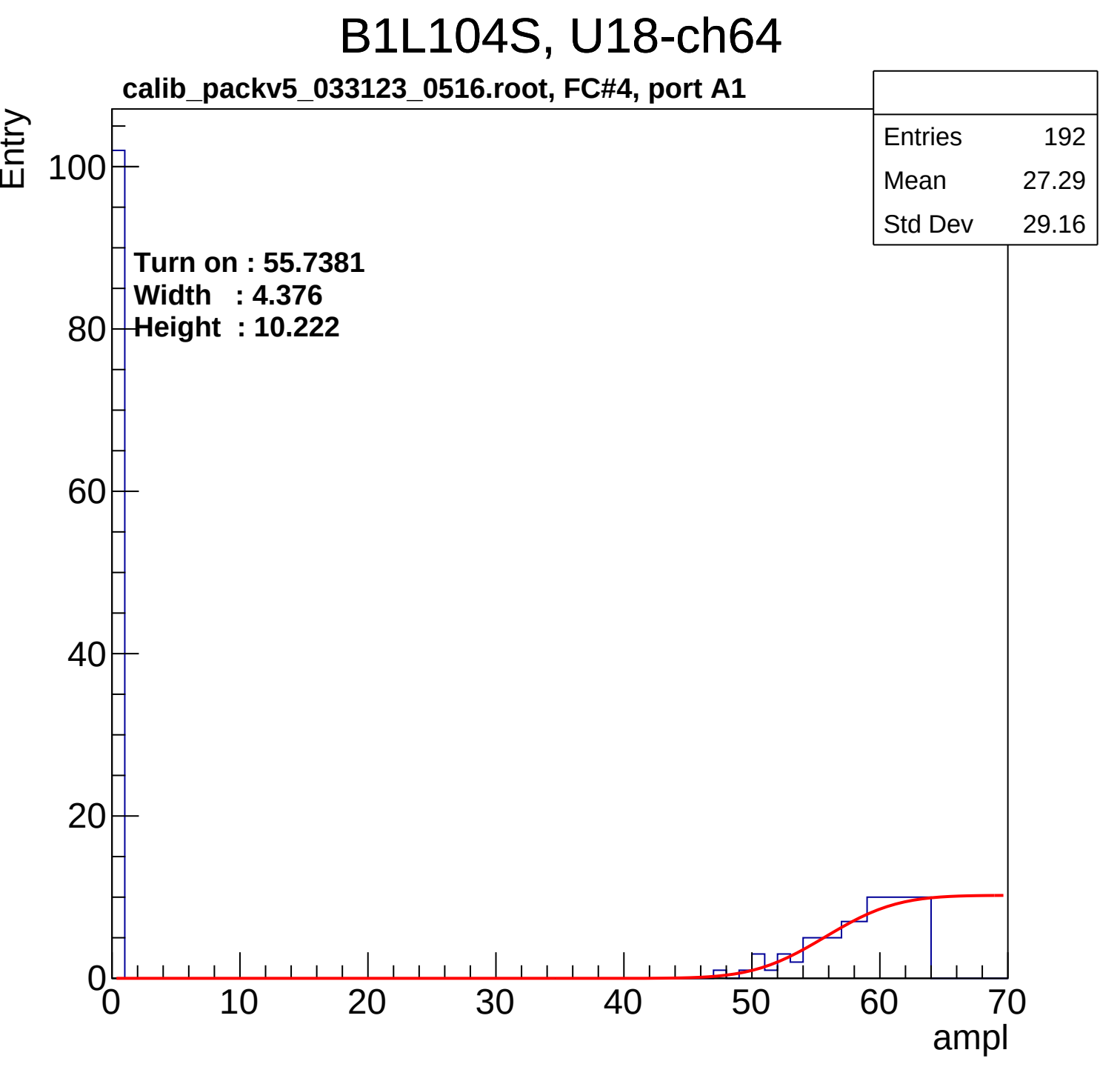

B1L104S, U18-ch59
calib_packv5_033123_0516.root, FC#4, port A1
Entries 157
Mean 34.78
Std Dev 28.62
Turn on : 55.3679
Width : 5.080
Height : 10.778
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

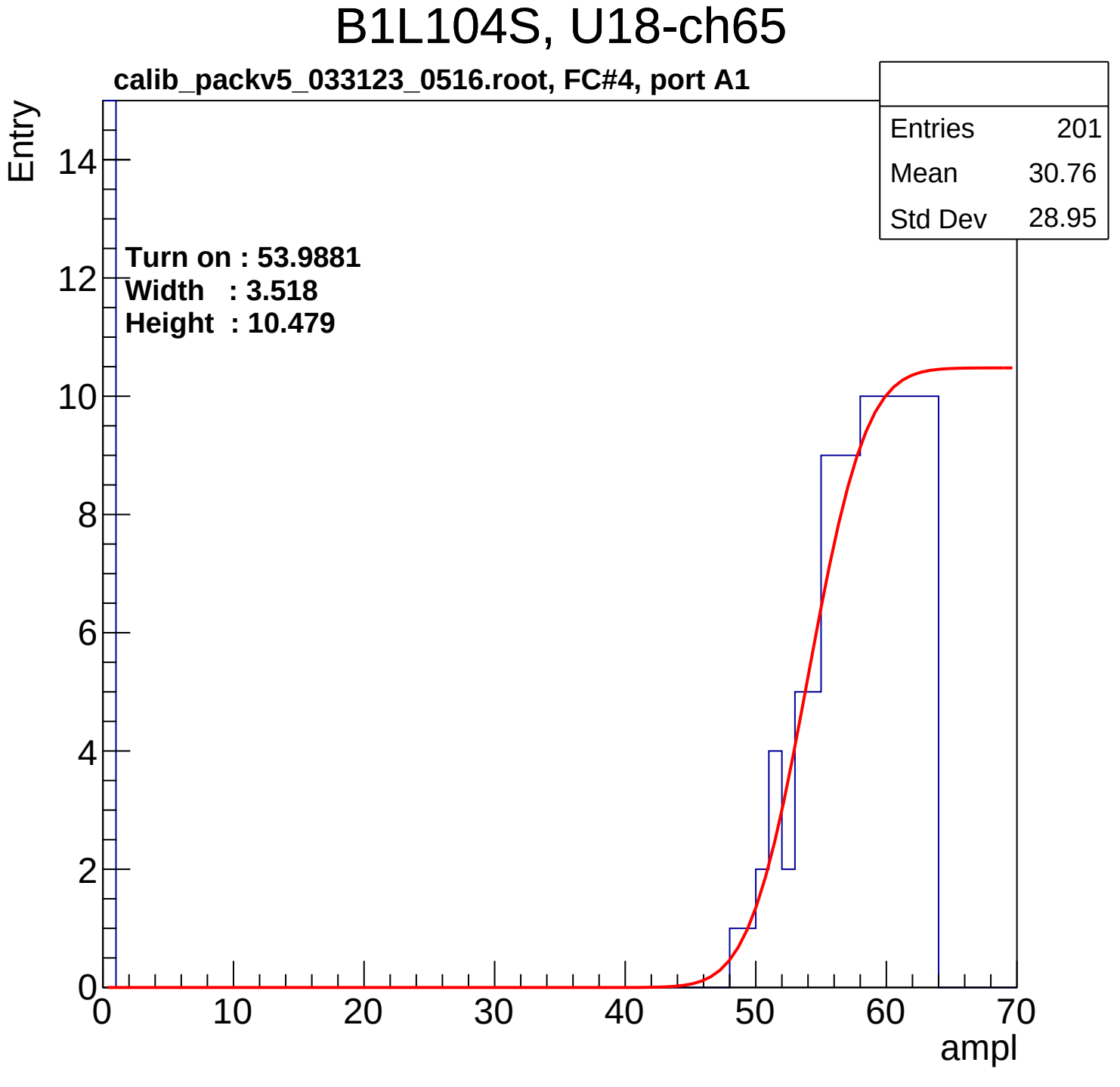

B1L104S, U18-ch60
calib_packv5_033123_0516.root, FC#4, port A1
Entries 168
Mean 33.32
Std Dev 28.96
Turn on : 54.3795
Width : 1.977
Height : 9.698
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

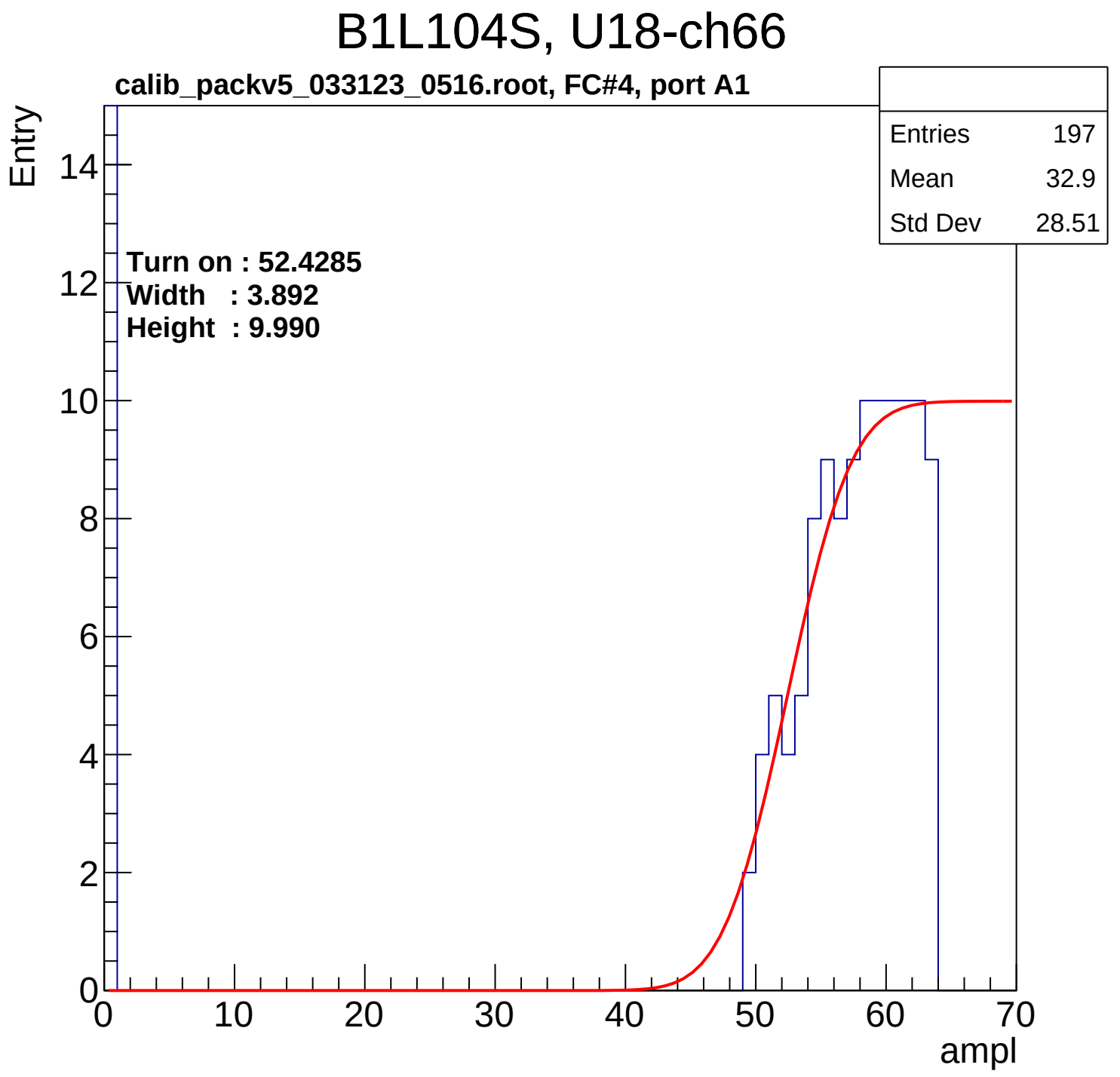

B1L104S, U18-ch61
calib_packv5_033123_0516.root, FC#4, port A1
Entries 168
Mean 35.52
Std Dev 28.36
Turn on : 54.0274
Width : 3.788
Height : 10.443
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

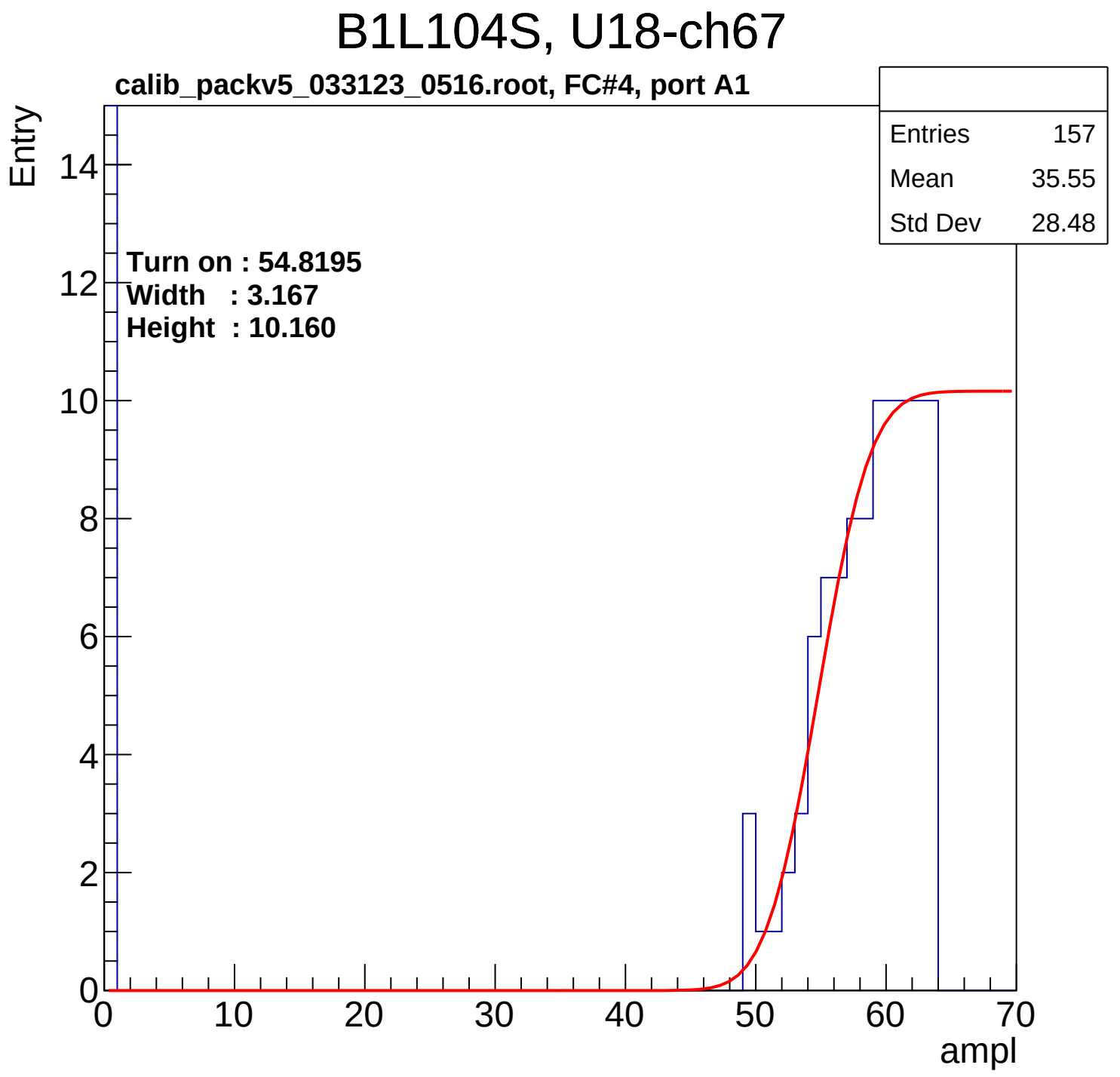

B1L104S, U18-ch62
calib_packv5_033123_0516.root, FC#4, port A1
Entries 183
Mean 34.62
Std Dev 28.36
Turn on : 53.9109
Width : 4.780
Height : 10.947
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

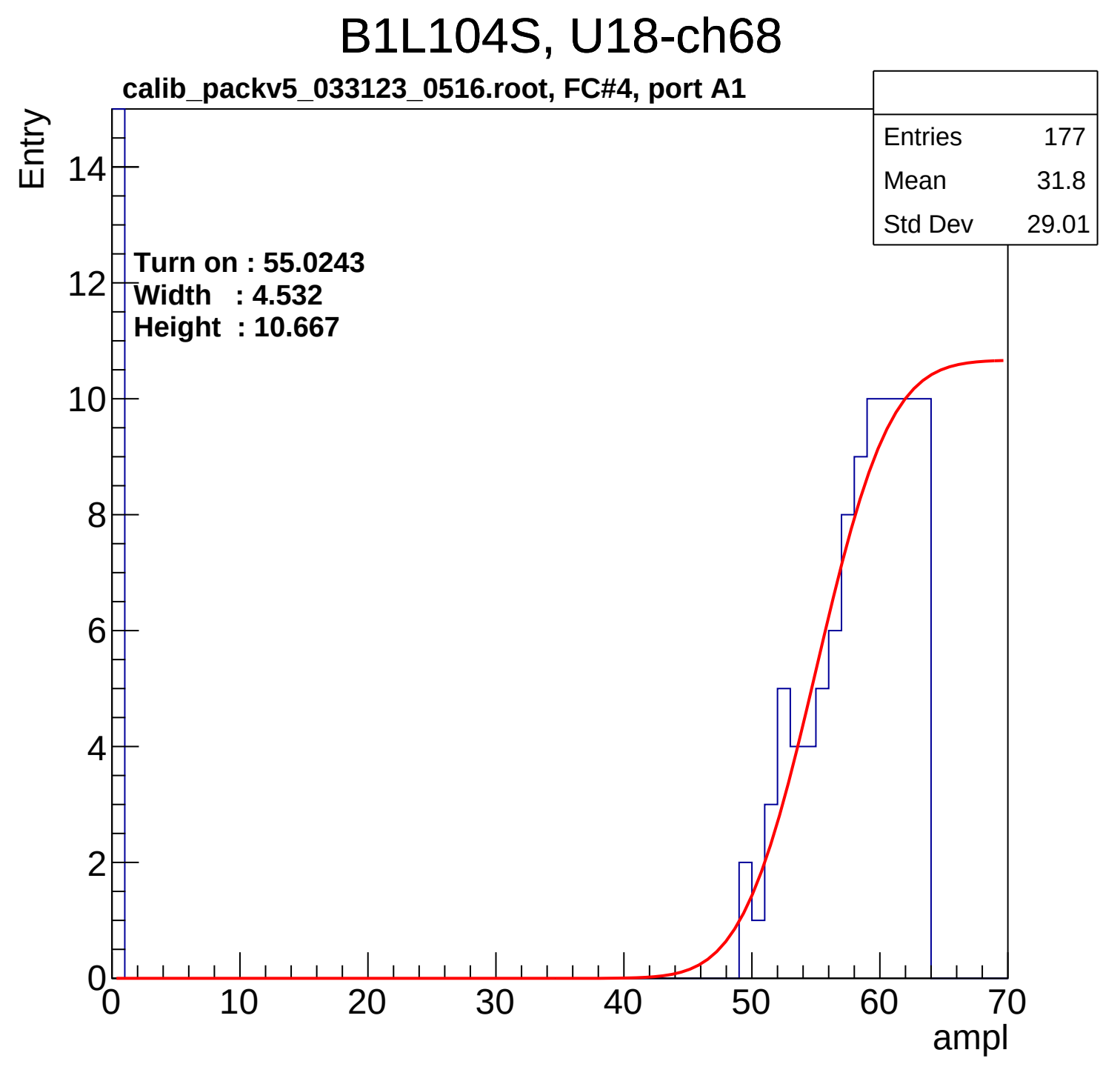

B1L104S, U18-ch63
calib_packv5_033123_0516.root, FC#4, port A1
Entries 192
Mean 33.82
Std Dev 28.43
Turn on : 52.2900
Width : 3.695
Height : 10.076
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

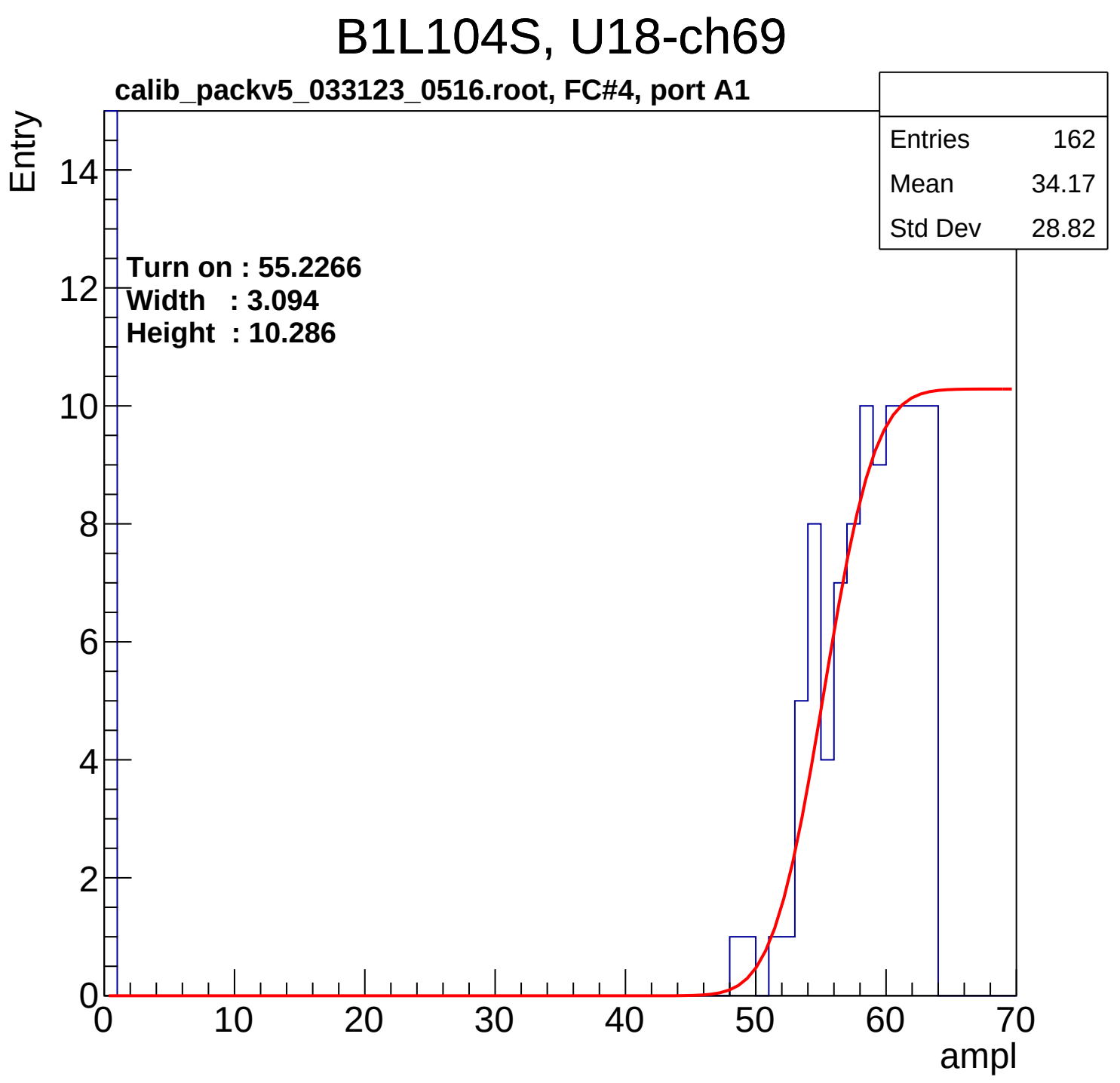

B1L104S, U18-ch64
calib_packv5_033123_0516.root, FC#4, port A1
Entries 192
Mean 27.29
Std Dev 29.16
Turn on : 55.7381
Width : 4.376
Height : 10.222
Entry
ampl
0
20
40
60
80
100
0
10
20
30
40
50
60
70

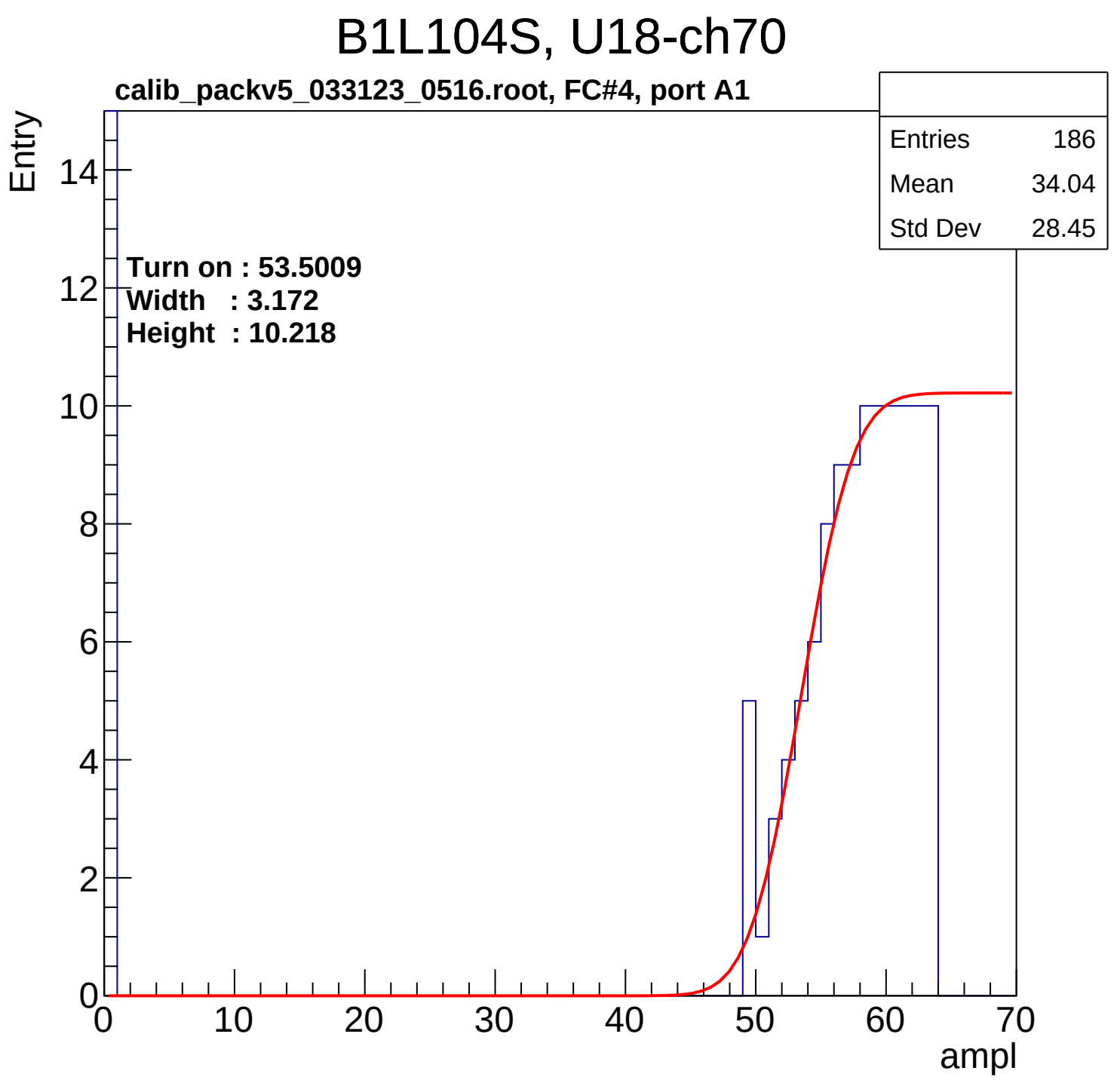

B1L104S, U18-ch65
calib_packv5_033123_0516.root, FC#4, port A1
Entries 201
Mean 30.76
Std Dev 28.95
Turn on : 53.9881
Width : 3.518
Height : 10.479
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

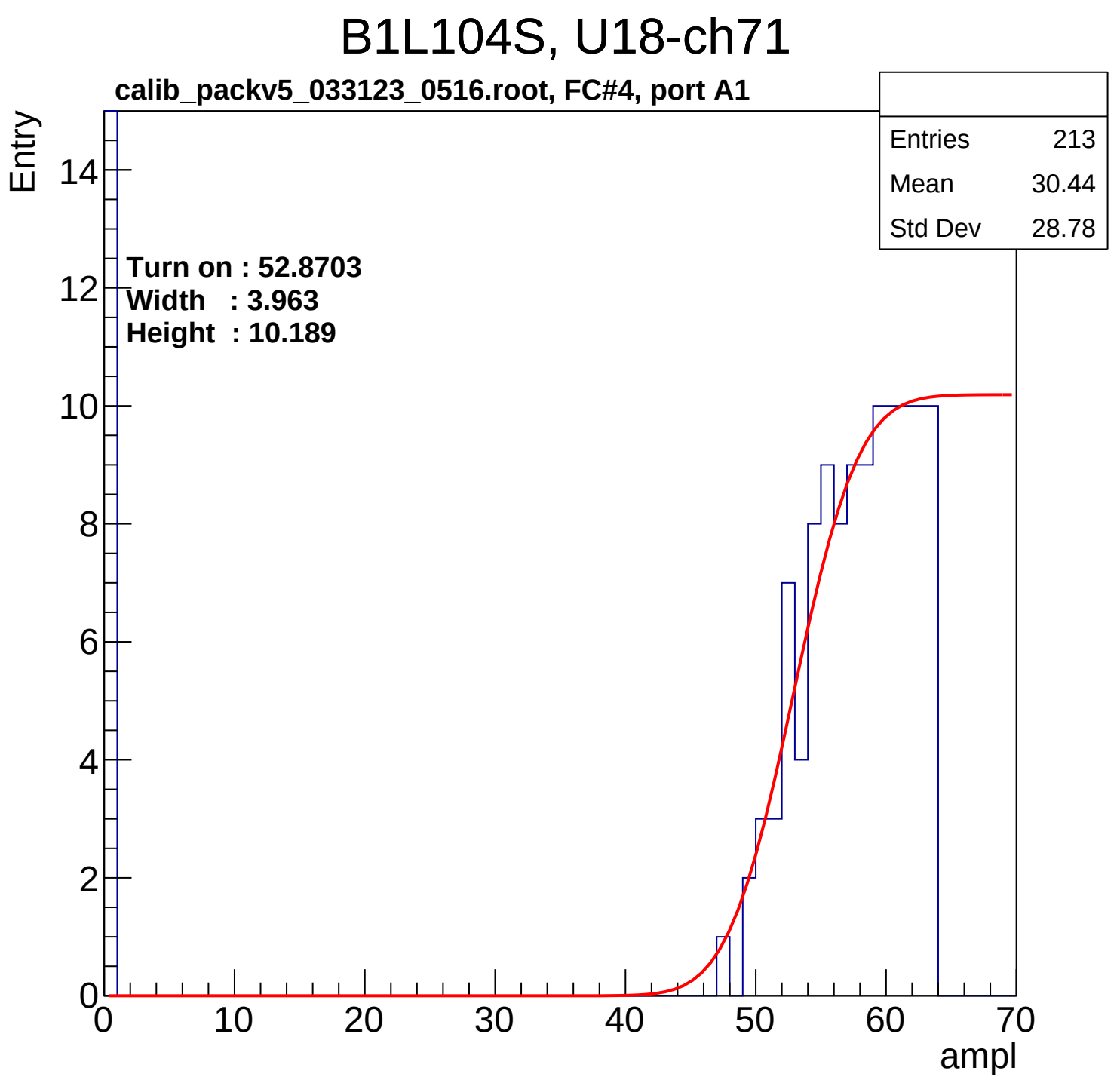

B1L104S, U18-ch66
calib_packv5_033123_0516.root, FC#4, port A1
Entries 197
Mean 32.9
Std Dev 28.51
Turn on : 52.4285
Width : 3.892
Height : 9.990
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

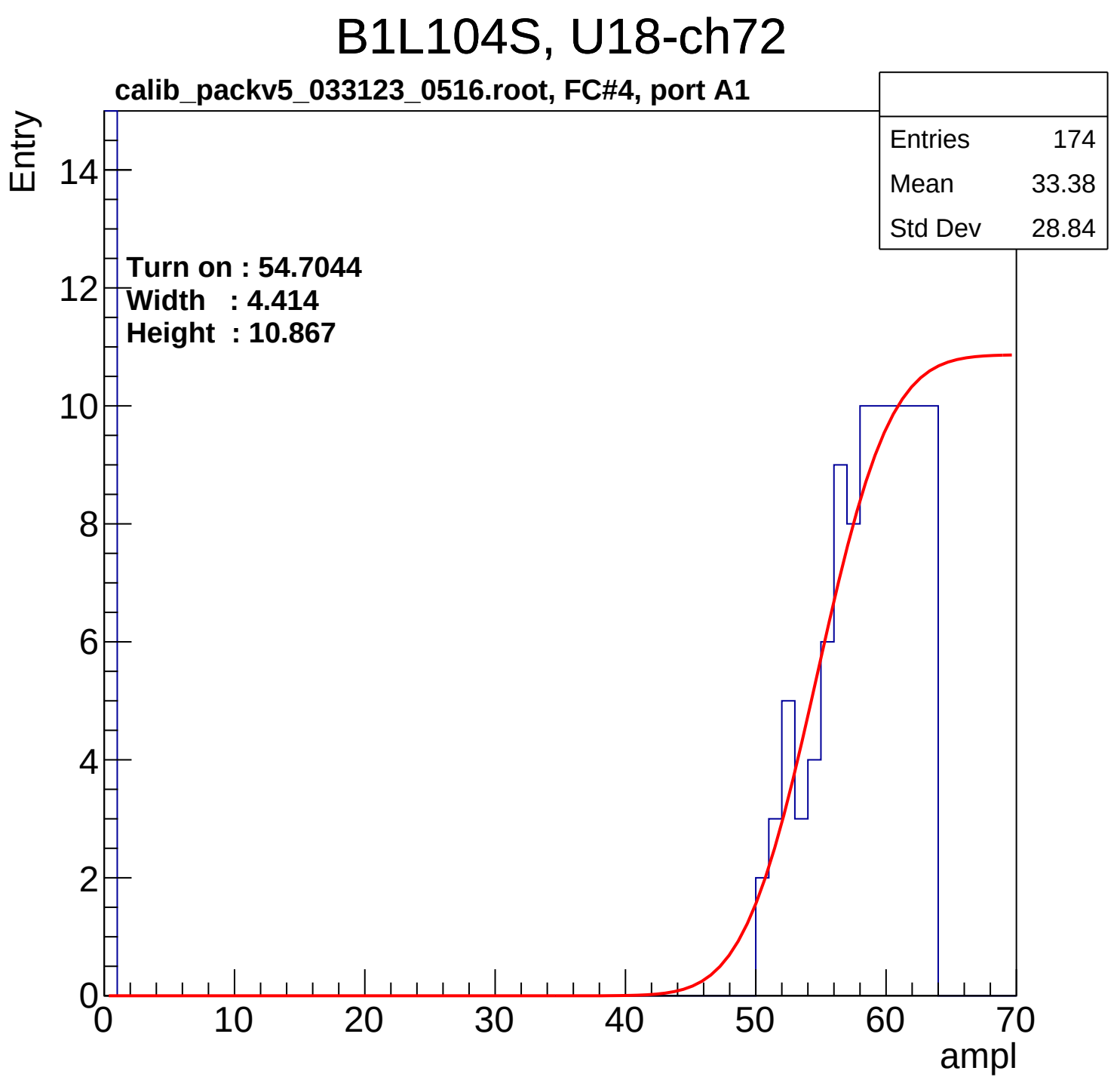

B1L104S, U18-ch67
calib_packv5_033123_0516.root, FC#4, port A1
Entries 157
Mean 35.55
Std Dev 28.48
Turn on : 54.8195
Width : 3.167
Height : 10.160
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

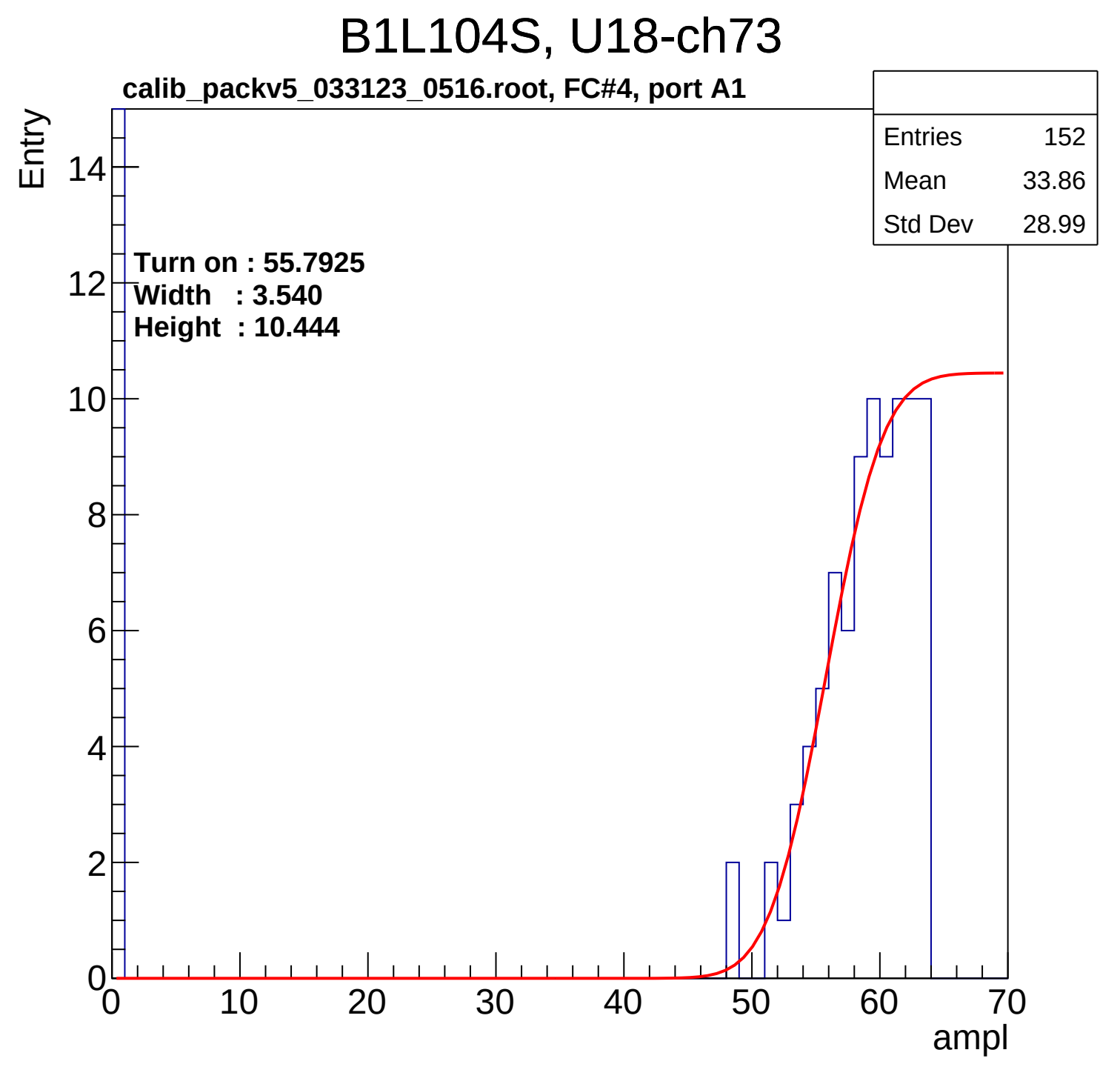

B1L104S, U18-ch68
calib_packv5_033123_0516.root, FC#4, port A1
Entries 177
Mean 31.8
Std Dev 29.01
Turn on : 55.0243
Width : 4.532
Height : 10.667
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

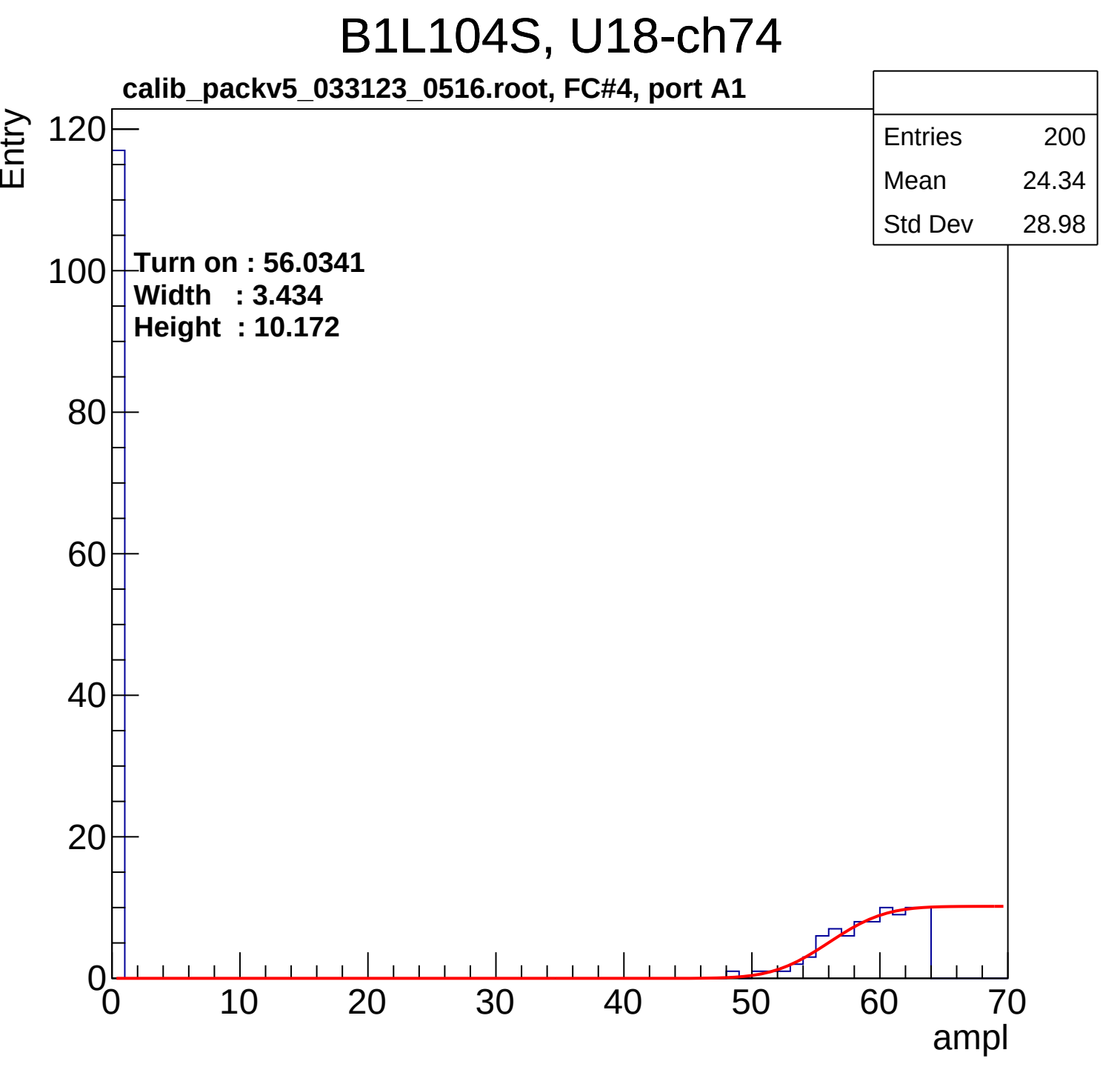

B1L104S, U18-ch69
calib_packv5_033123_0516.root, FC#4, port A1
Entries 162
Mean 34.17
Std Dev 28.82
Turn on : 55.2266
Width : 3.094
Height : 10.286
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

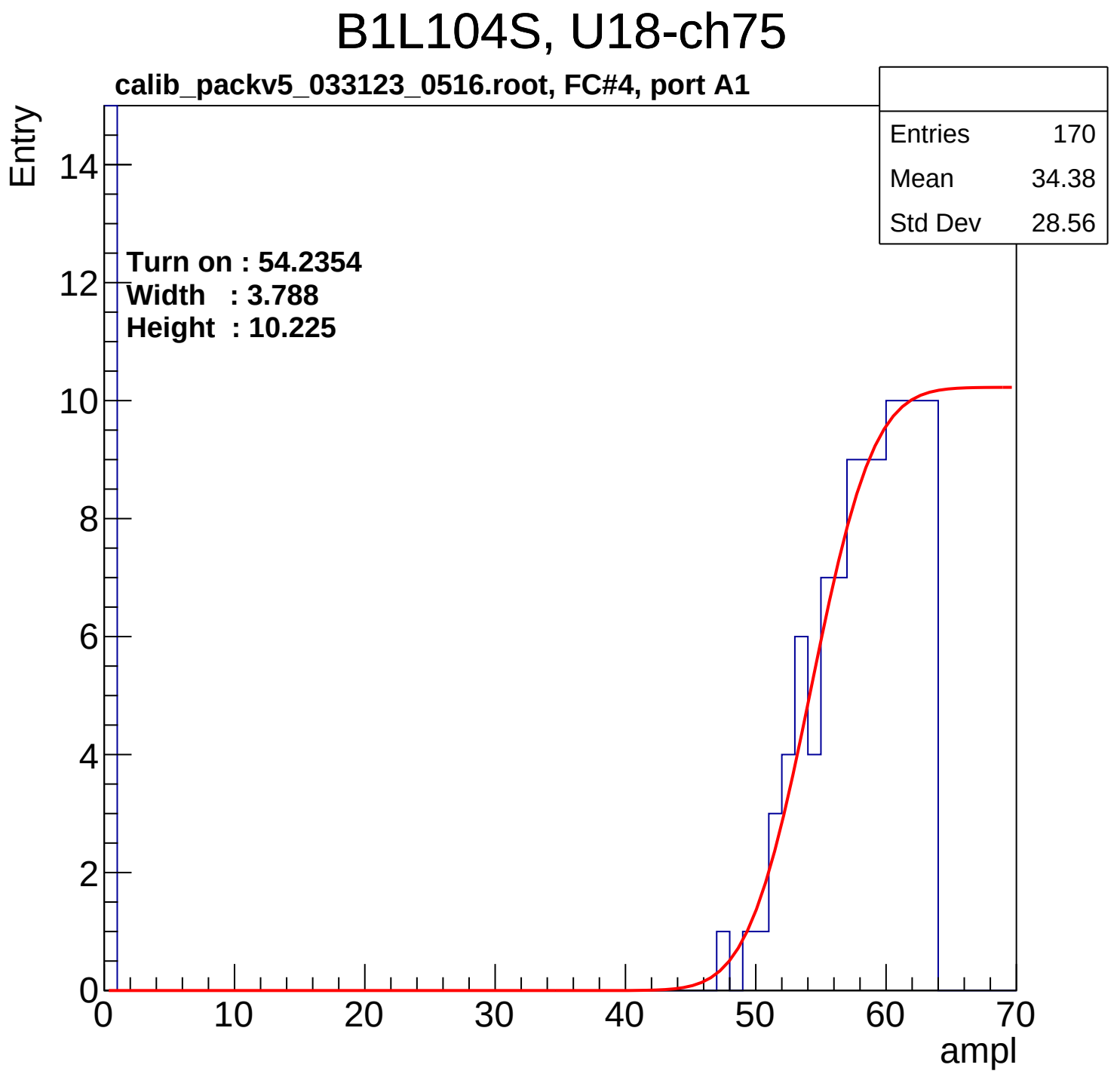

B1L104S, U18-ch70
calib_packv5_033123_0516.root, FC#4, port A1
Entries 186
Mean 34.04
Std Dev 28.45
Turn on : 53.5009
Width : 3.172
Height : 10.218
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

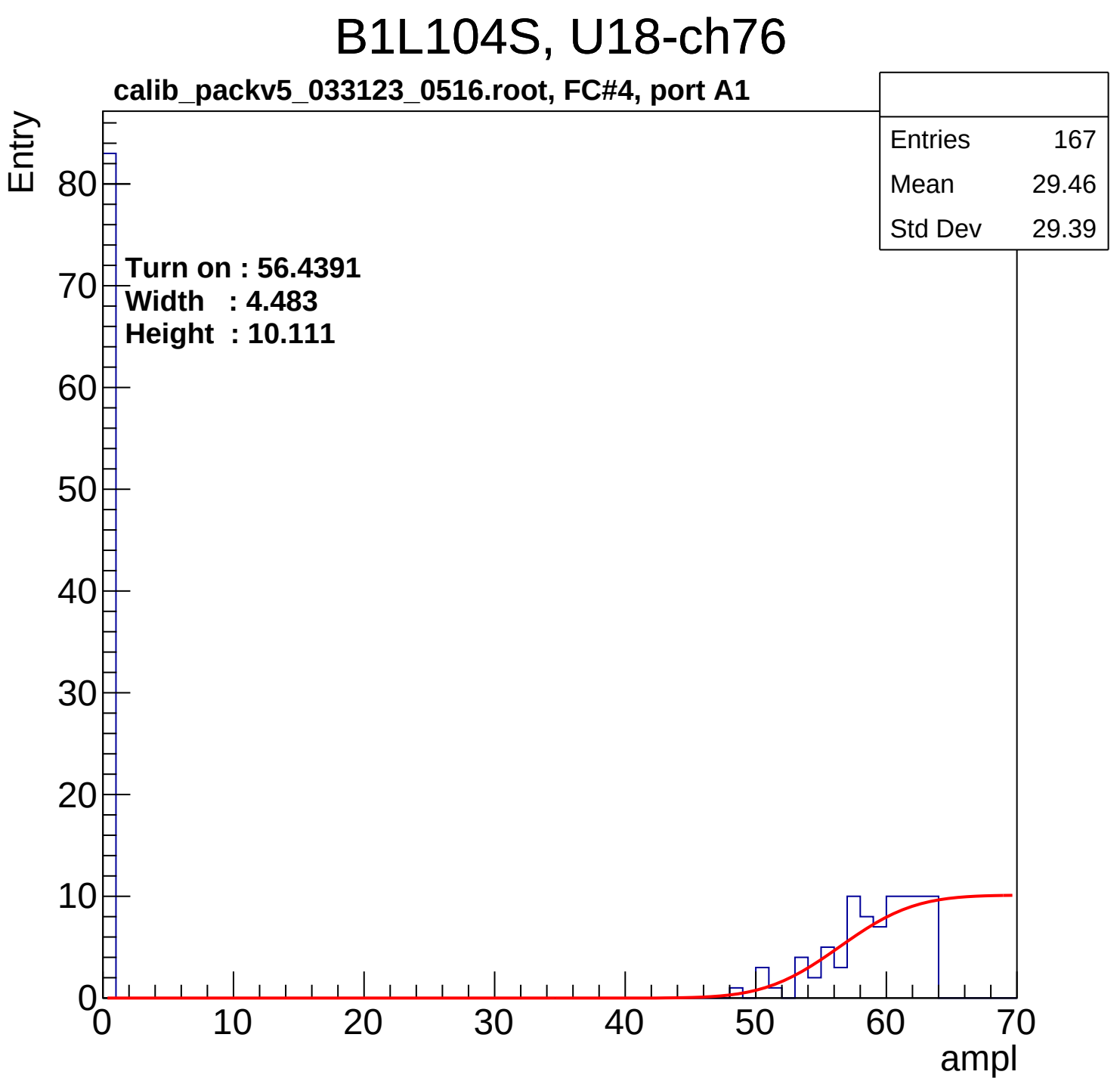

B1L104S, U18-ch71
calib_packv5_033123_0516.root, FC#4, port A1
Entries 213
Mean 30.44
Std Dev 28.78
Turn on : 52.8703
Width : 3.963
Height : 10.189
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

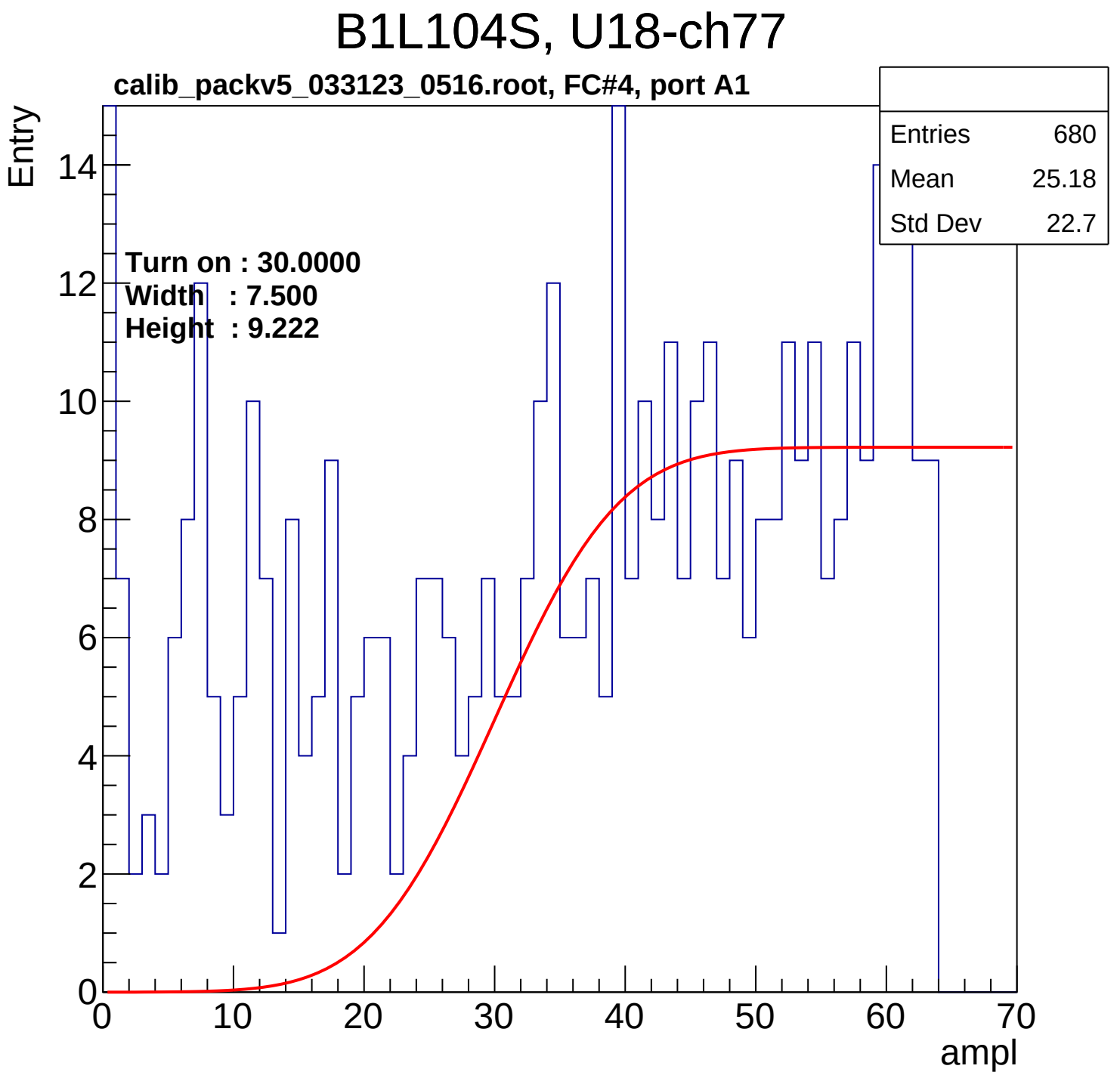

B1L104S, U18-ch72
calib_packv5_033123_0516.root, FC#4, port A1
Entries 174
Mean 33.38
Std Dev 28.84
Turn on : 54.7044
Width : 4.414
Height : 10.867
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

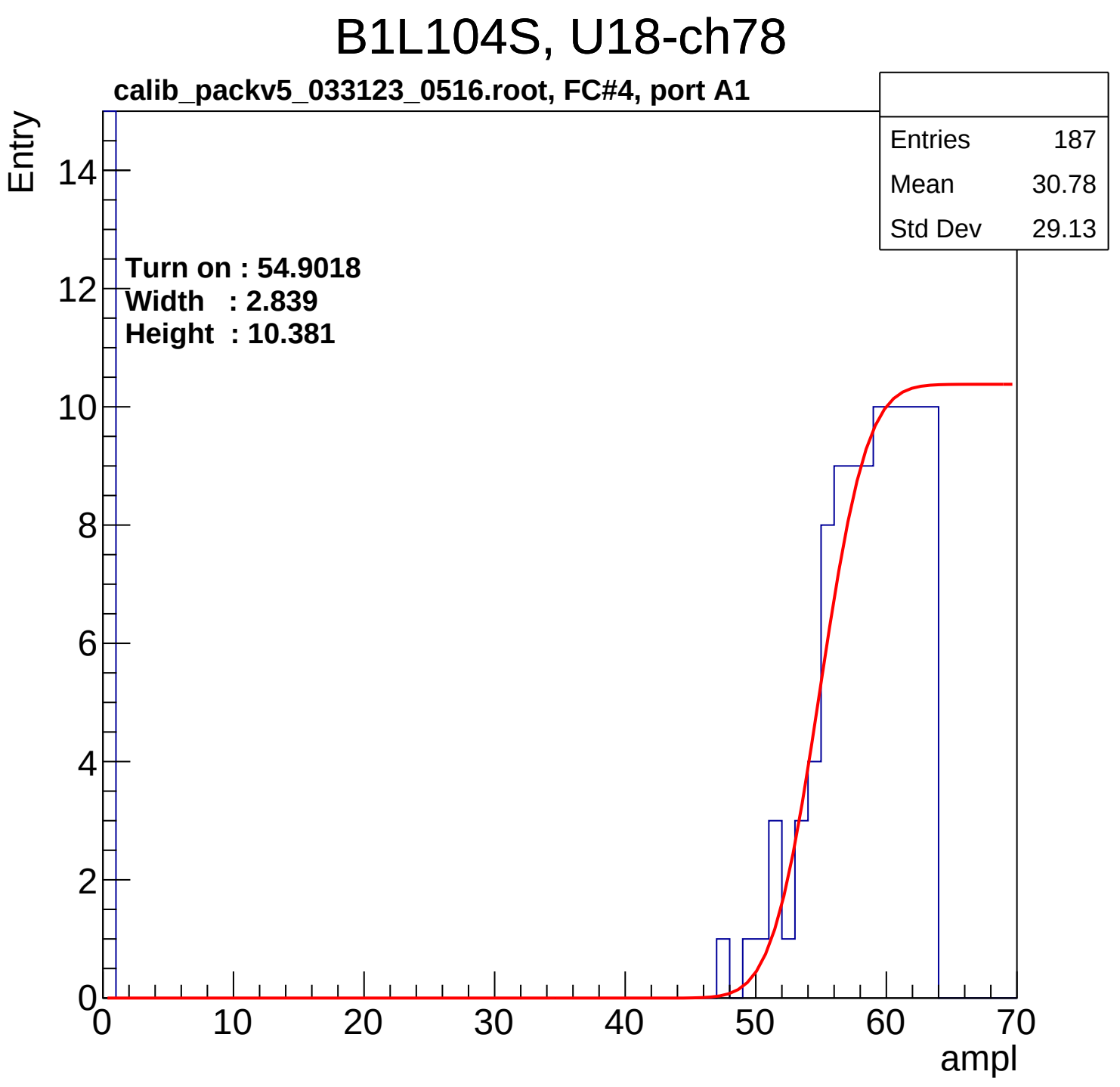

B1L104S, U18-ch73
calib_packv5_033123_0516.root, FC#4, port A1
Entries 152
Mean 33.86
Std Dev 28.99
Turn on : 55.7925
Width : 3.540
Height : 10.444
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

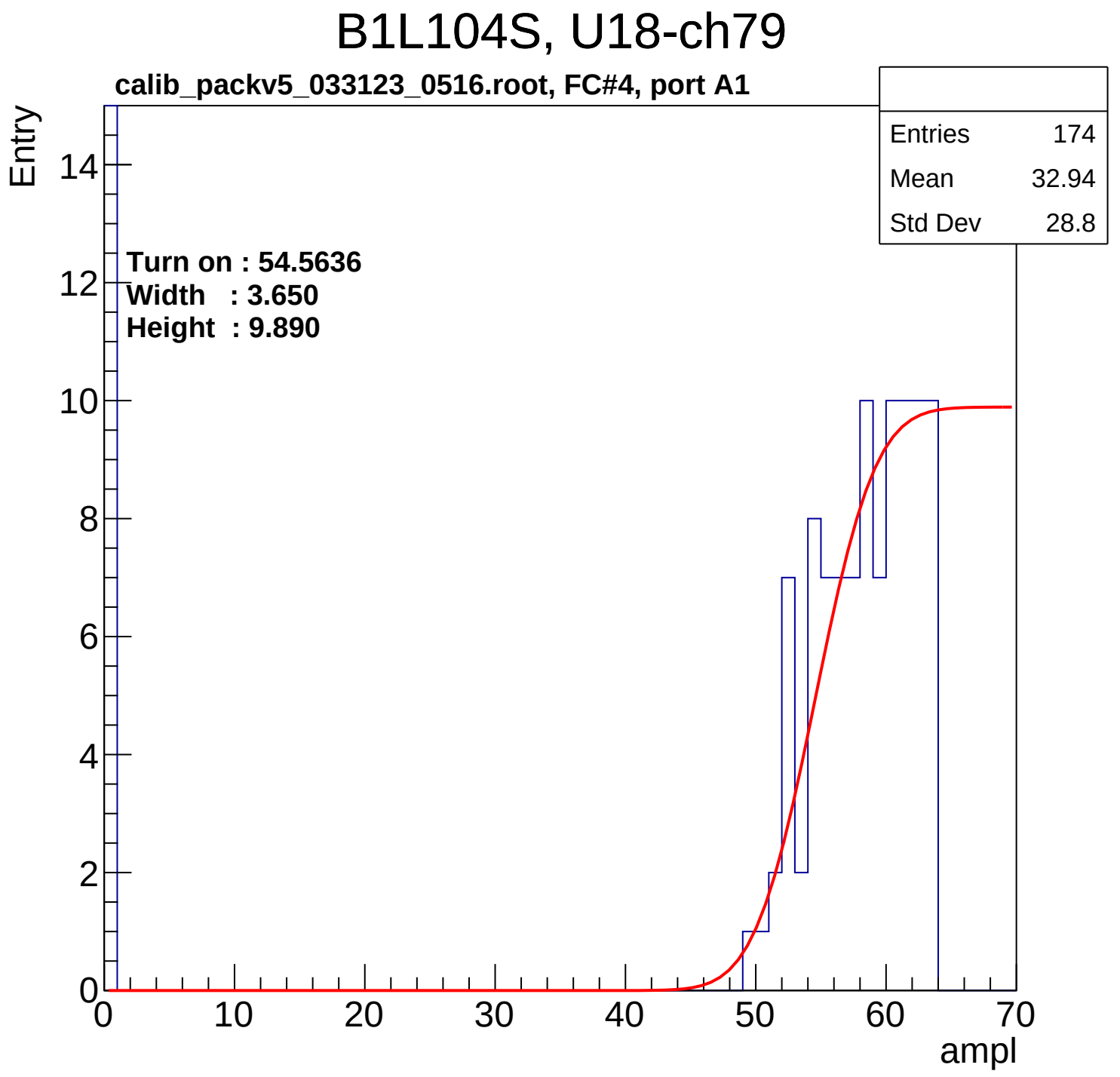

B1L104S, U18-ch74
calib_packv5_033123_0516.root, FC#4, port A1
Entries 200
Mean 24.34
Std Dev 28.98
Turn on : 56.0341
Width : 3.434
Height : 10.172
Entry
ampl
0
20
40
60
80
100
120
0
10
20
30
40
50
60
70

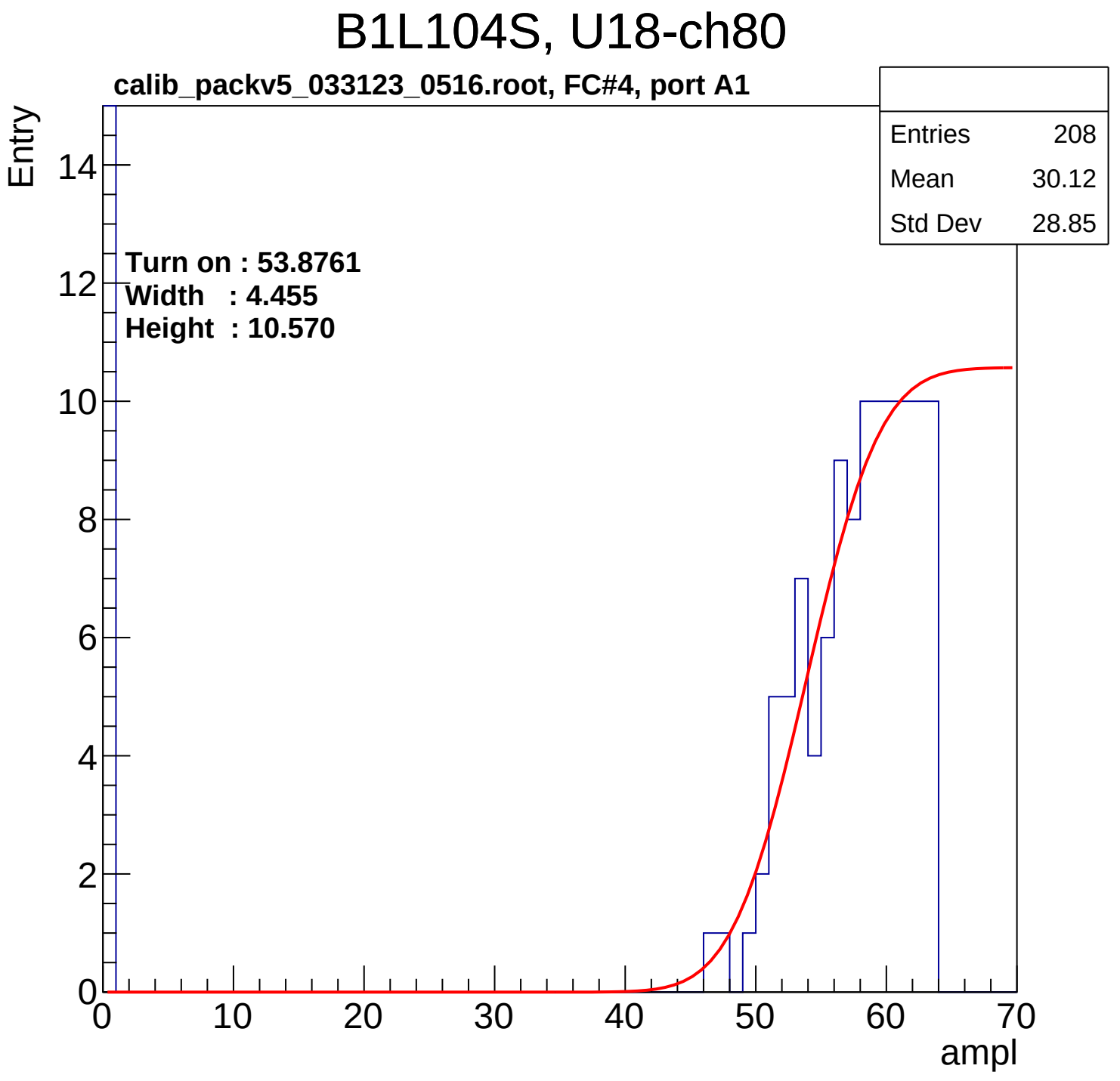

B1L104S, U18-ch75
calib_packv5_033123_0516.root, FC#4, port A1
Entries 170
Mean 34.38
Std Dev 28.56
Turn on : 54.2354
Width : 3.788
Height : 10.225
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

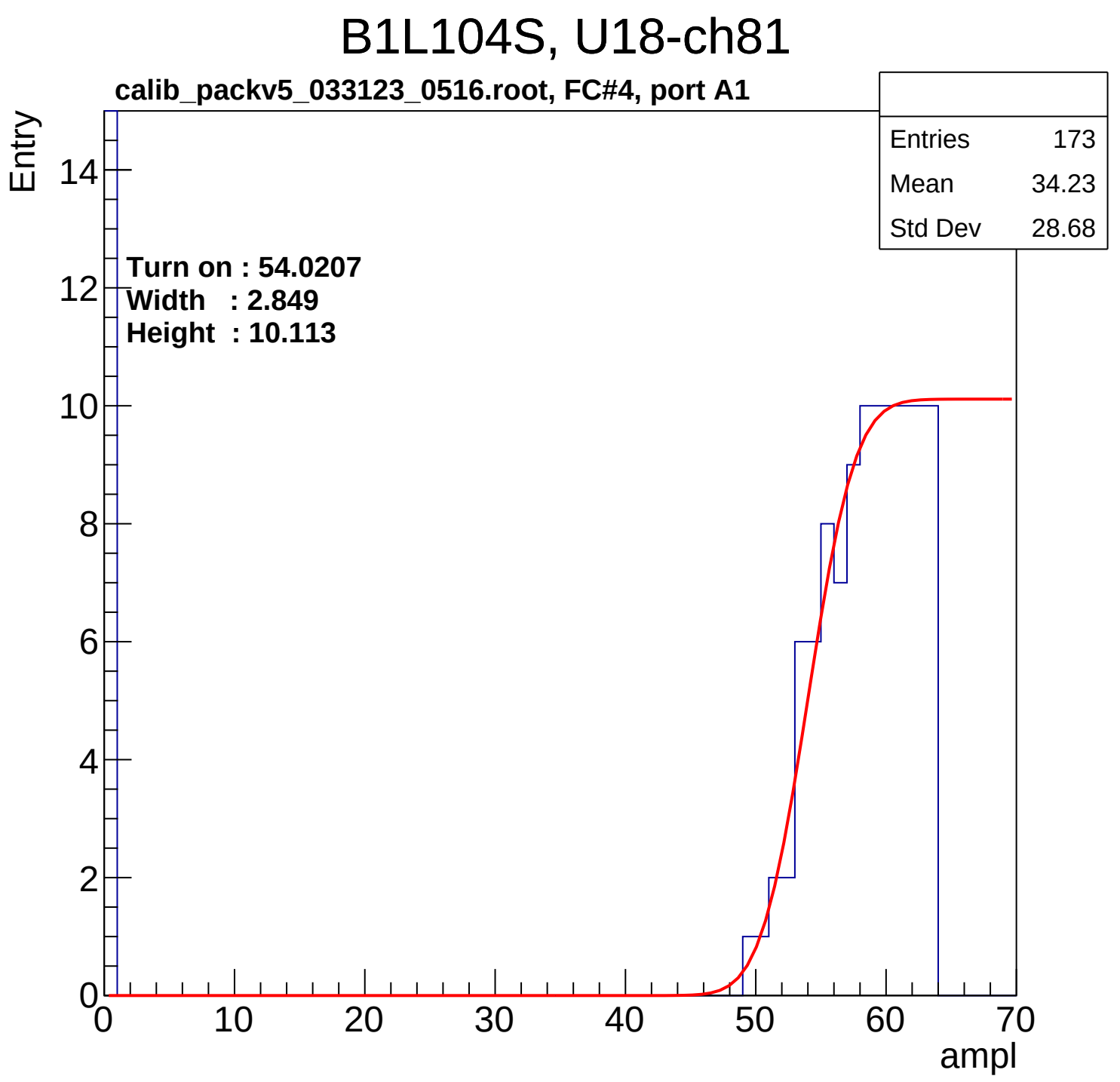

B1L104S, U18-ch76
calib_packv5_033123_0516.root, FC#4, port A1
Entries 167
Mean 29.46
Std Dev 29.39
Turn on : 56.4391
Width : 4.483
Height : 10.111
Entry
ampl
0
10
20
30
40
50
60
70
80

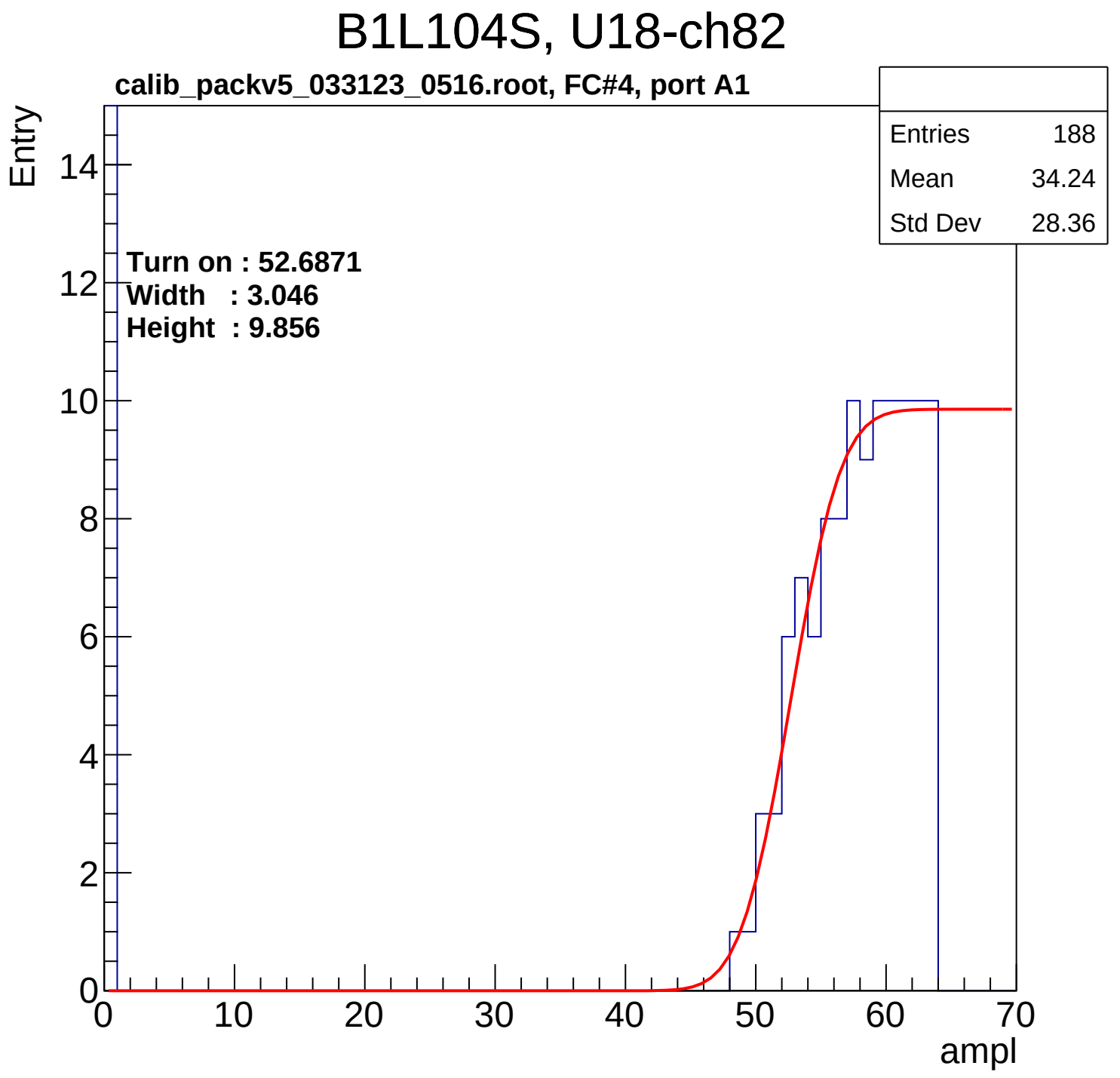

B1L104S, U18-ch77
calib_packv5_033123_0516.root, FC#4, port A1
Entries 680
Mean 25.18
Std Dev 22.7
Turn on : 30.0000
Width : 7.500
Height : 9.222
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

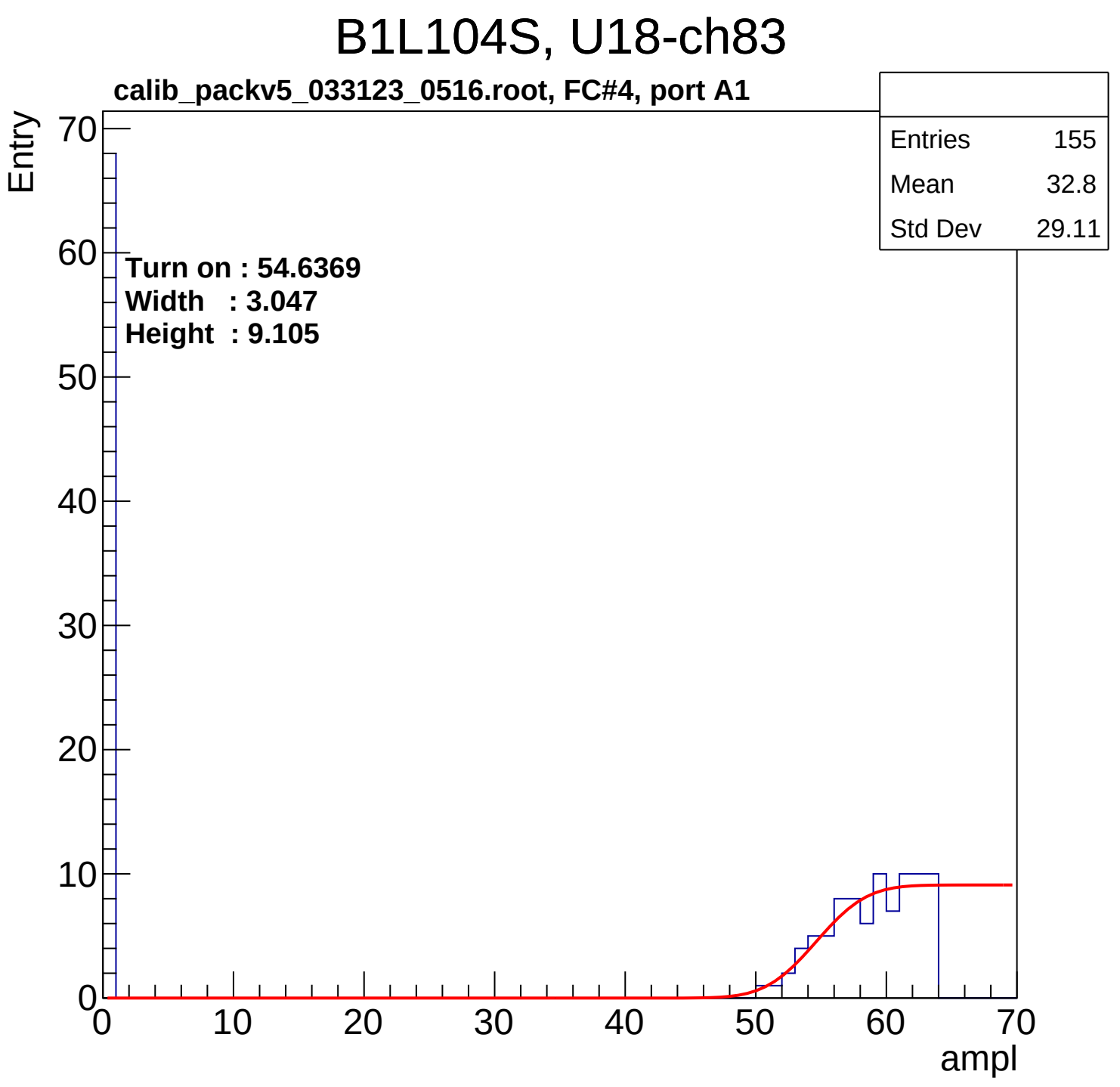

B1L104S, U18-ch78
calib_packv5_033123_0516.root, FC#4, port A1
Entries 187
Mean 30.78
Std Dev 29.13
Turn on : 54.9018
Width : 2.839
Height : 10.381
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

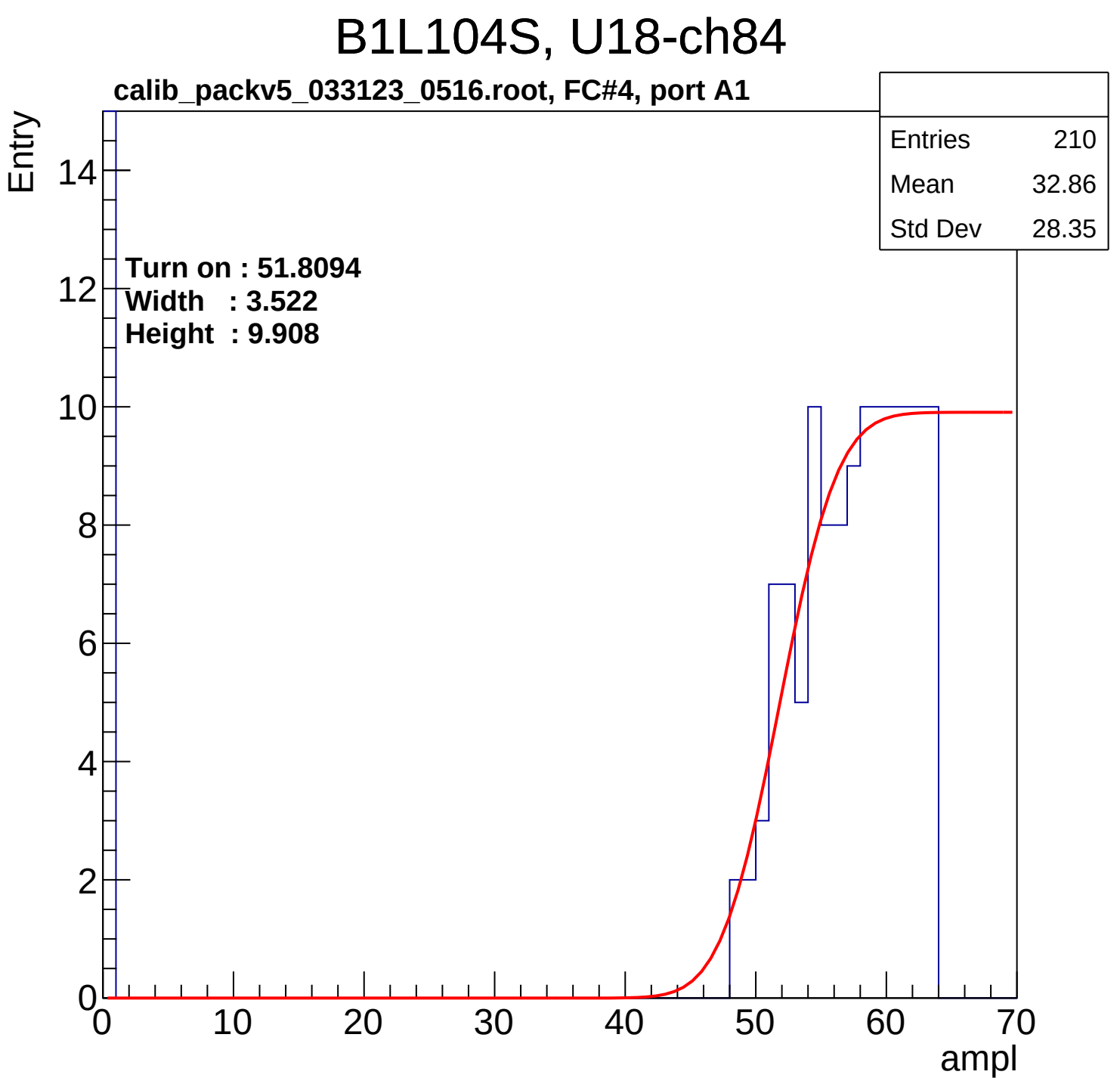

B1L104S, U18-ch79
calib_packv5_033123_0516.root, FC#4, port A1
Entries 174
Mean 32.94
Std Dev 28.8
Turn on : 54.5636
Width : 3.650
Height : 9.890
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

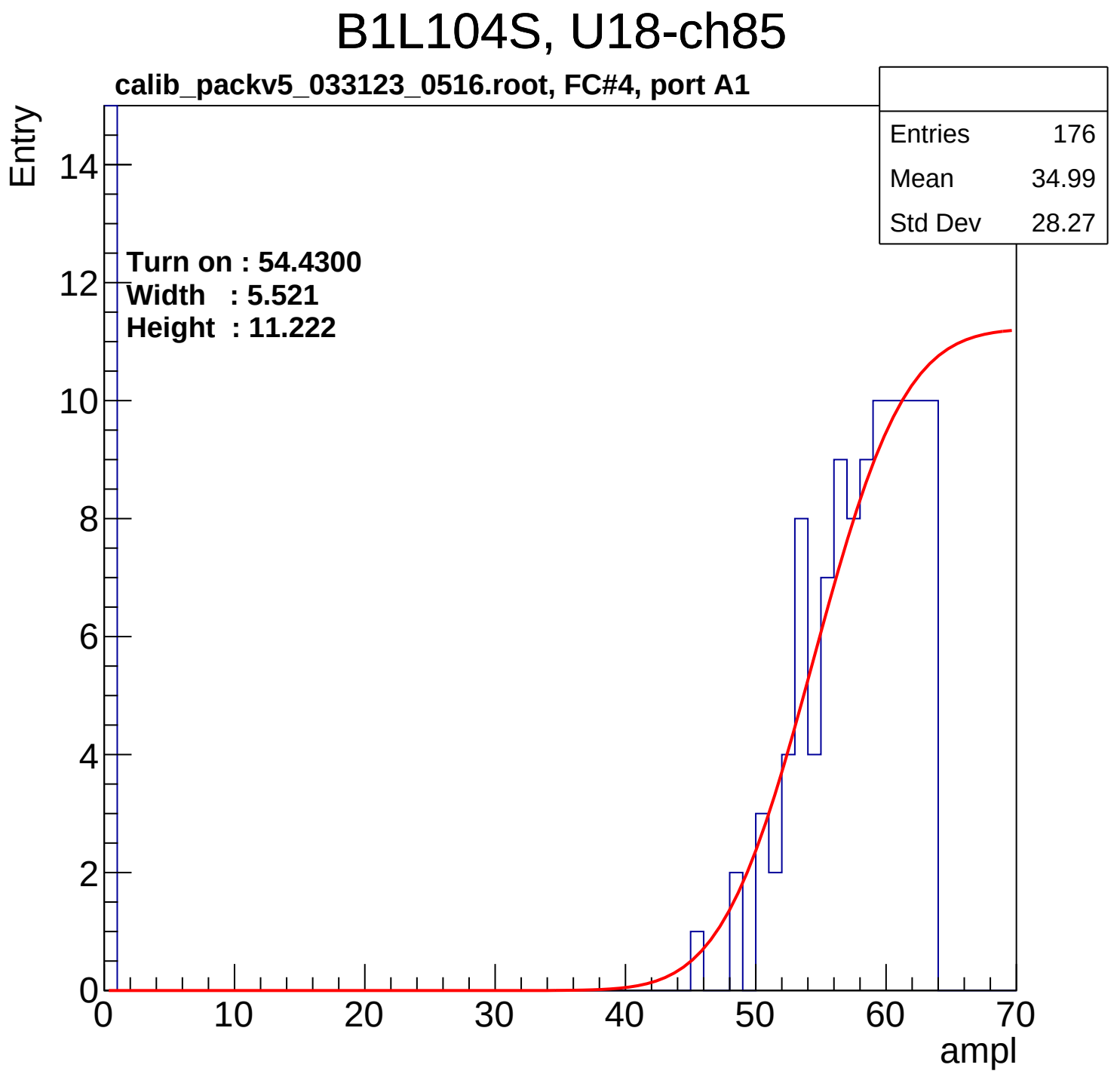

B1L104S, U18-ch80
calib_packv5_033123_0516.root, FC#4, port A1
Entries 208
Mean 30.12
Std Dev 28.85
Turn on : 53.8761
Width : 4.455
Height : 10.570
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

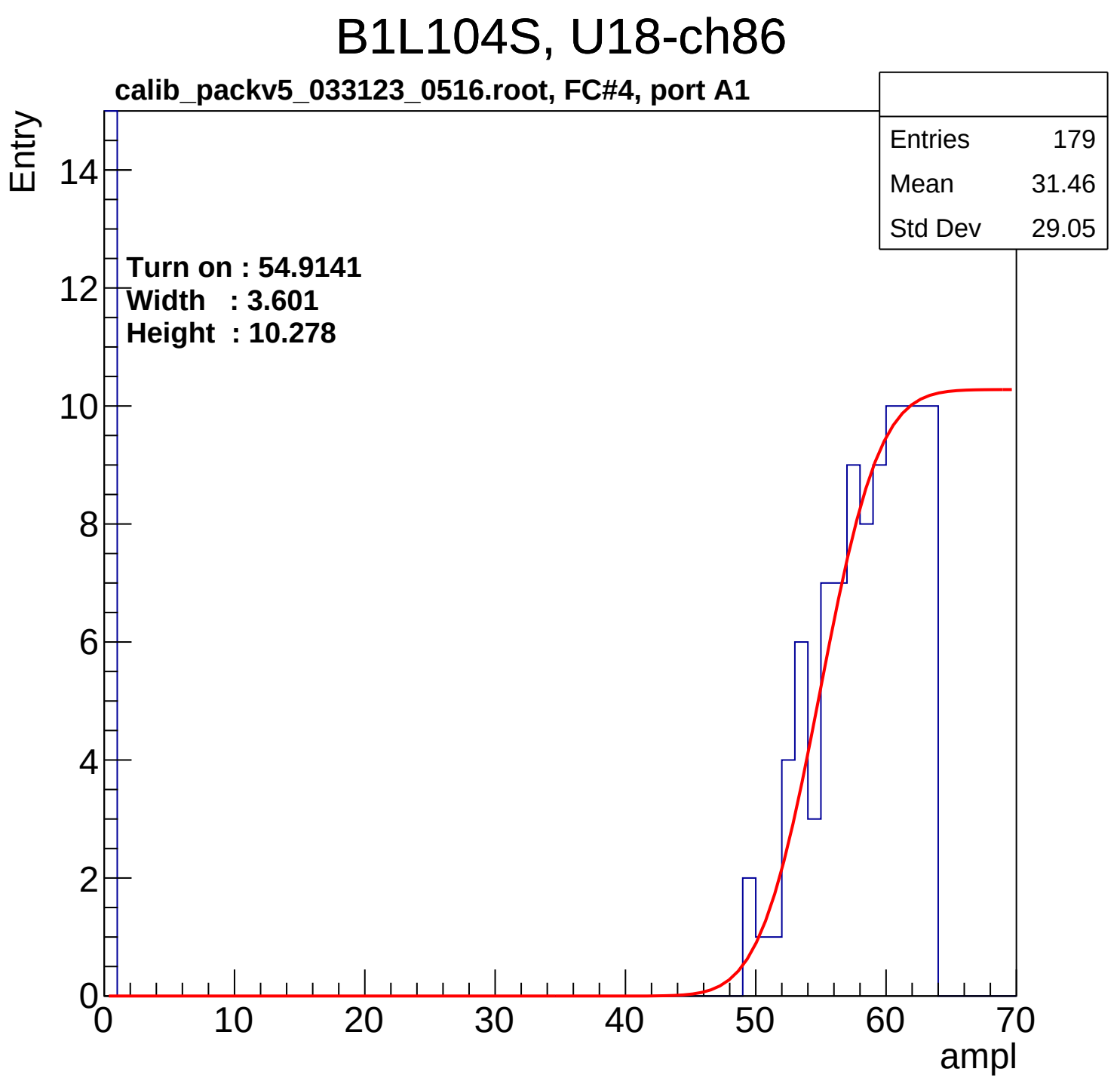

B1L104S, U18-ch81
calib_packv5_033123_0516.root, FC#4, port A1
Entries 173
Mean 34.23
Std Dev 28.68
Turn on : 54.0207
Width : 2.849
Height : 10.113
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

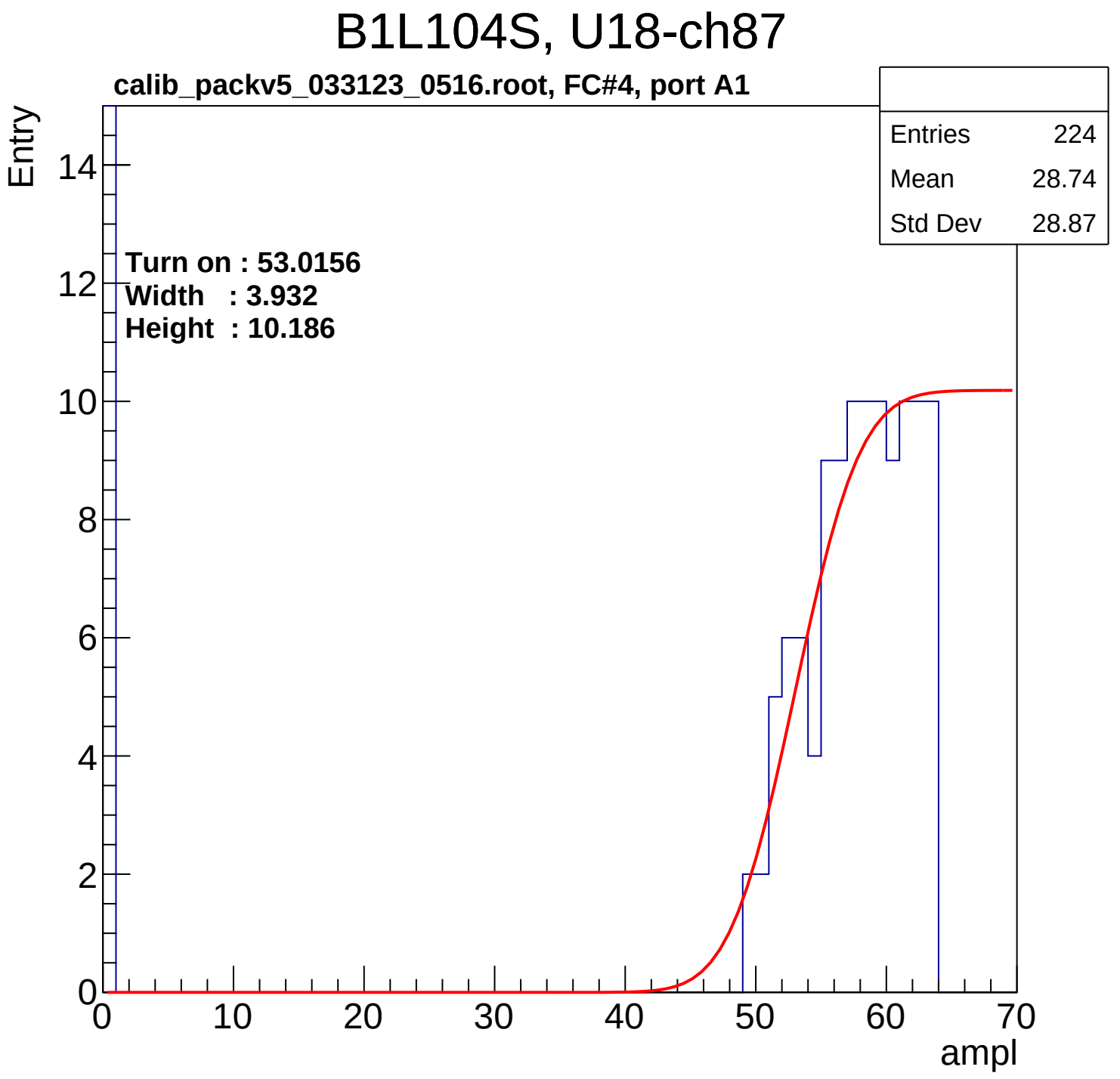

B1L104S, U18-ch82
calib_packv5_033123_0516.root, FC#4, port A1
Entries 188
Mean 34.24
Std Dev 28.36
Turn on : 52.6871
Width : 3.046
Height : 9.856
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

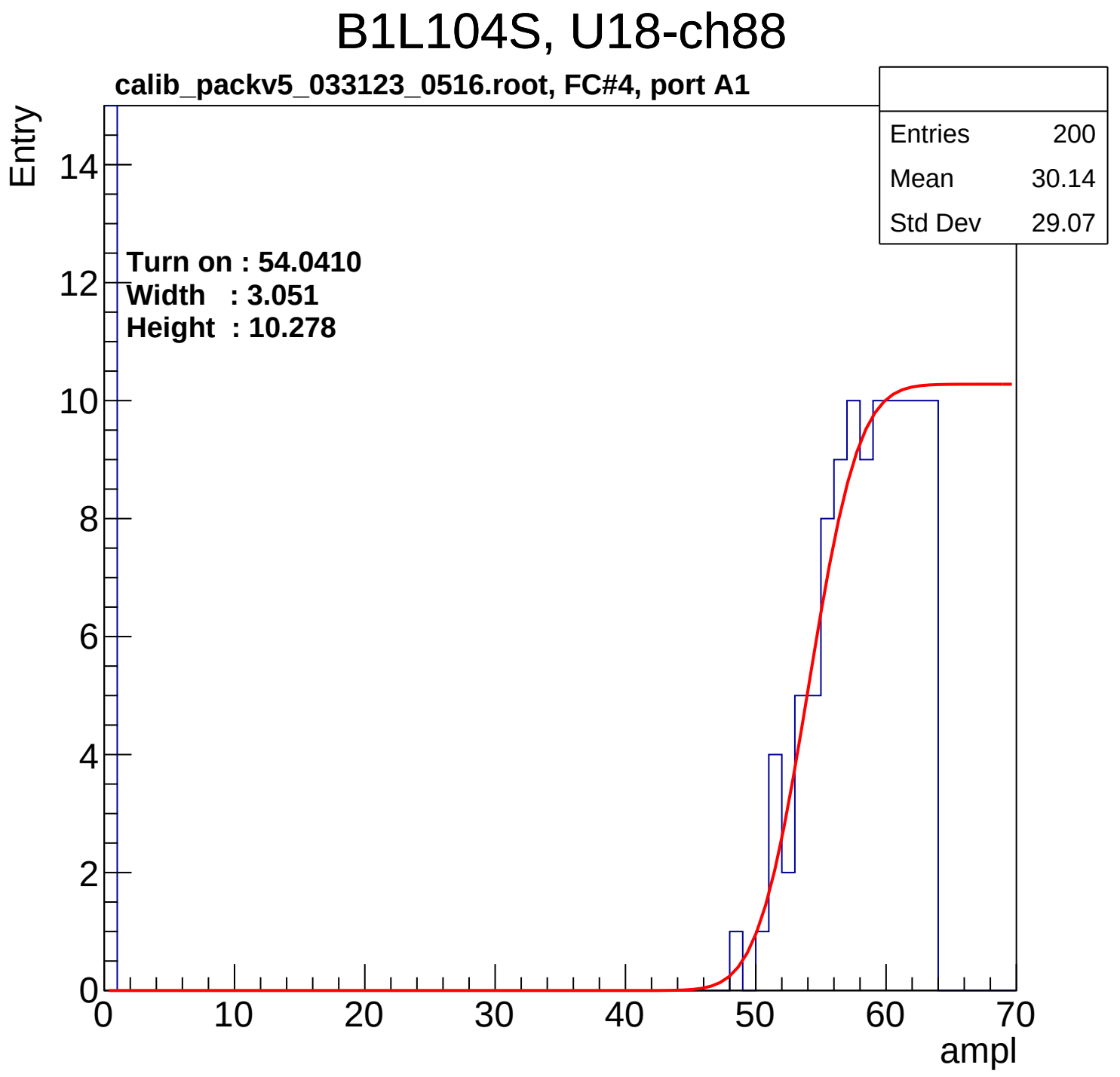

B1L104S, U18-ch83
calib_packv5_033123_0516.root, FC#4, port A1
Entries 155
Mean 32.8
Std Dev 29.11
Turn on : 54.6369
Width : 3.047
Height : 9.105
Entry
ampl
0
10
20
30
40
50
60
70

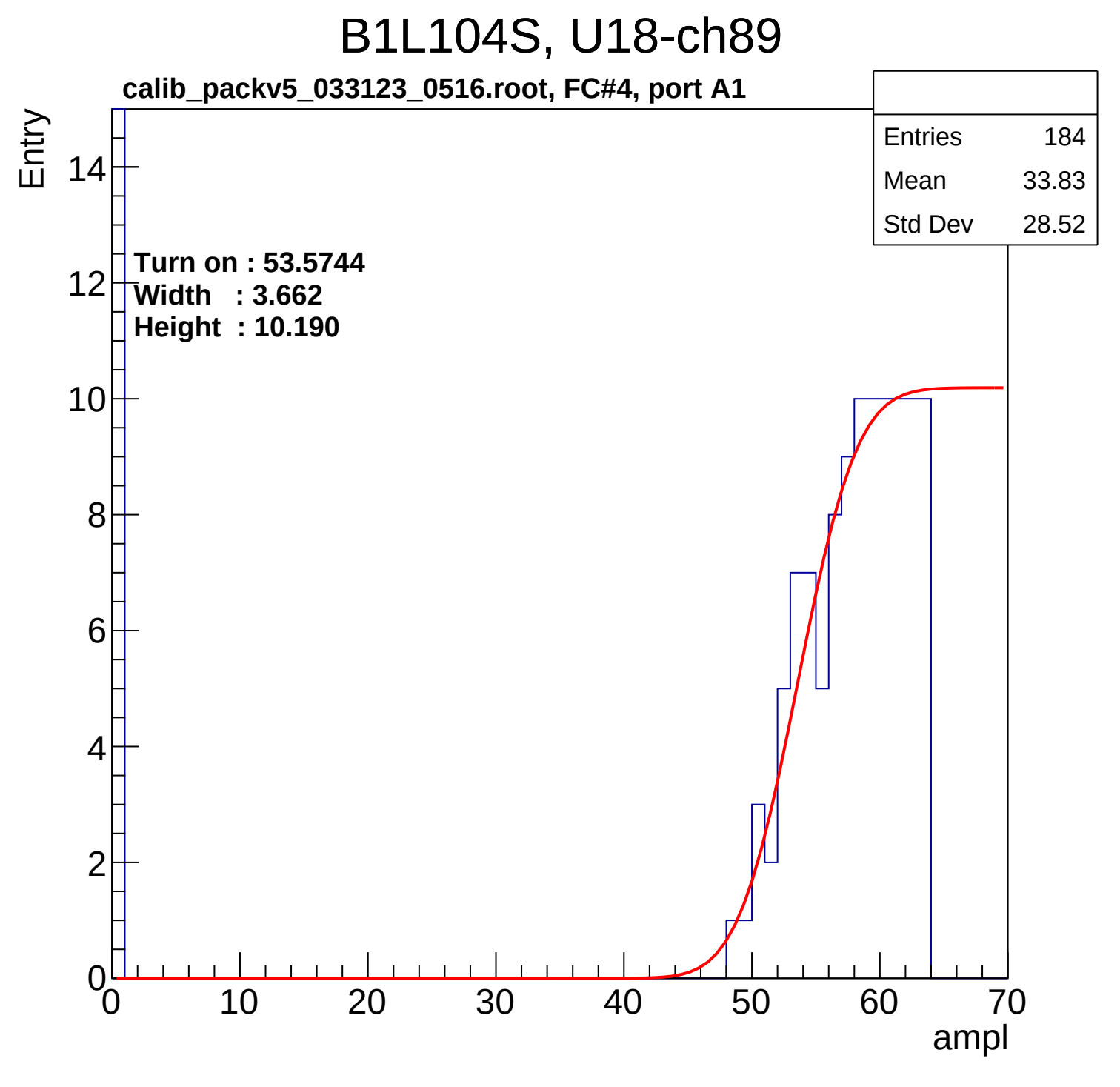

B1L104S, U18-ch84
calib_packv5_033123_0516.root, FC#4, port A1
Entries 210
Mean 32.86
Std Dev 28.35
Turn on : 51.8094
Width : 3.522
Height : 9.908
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

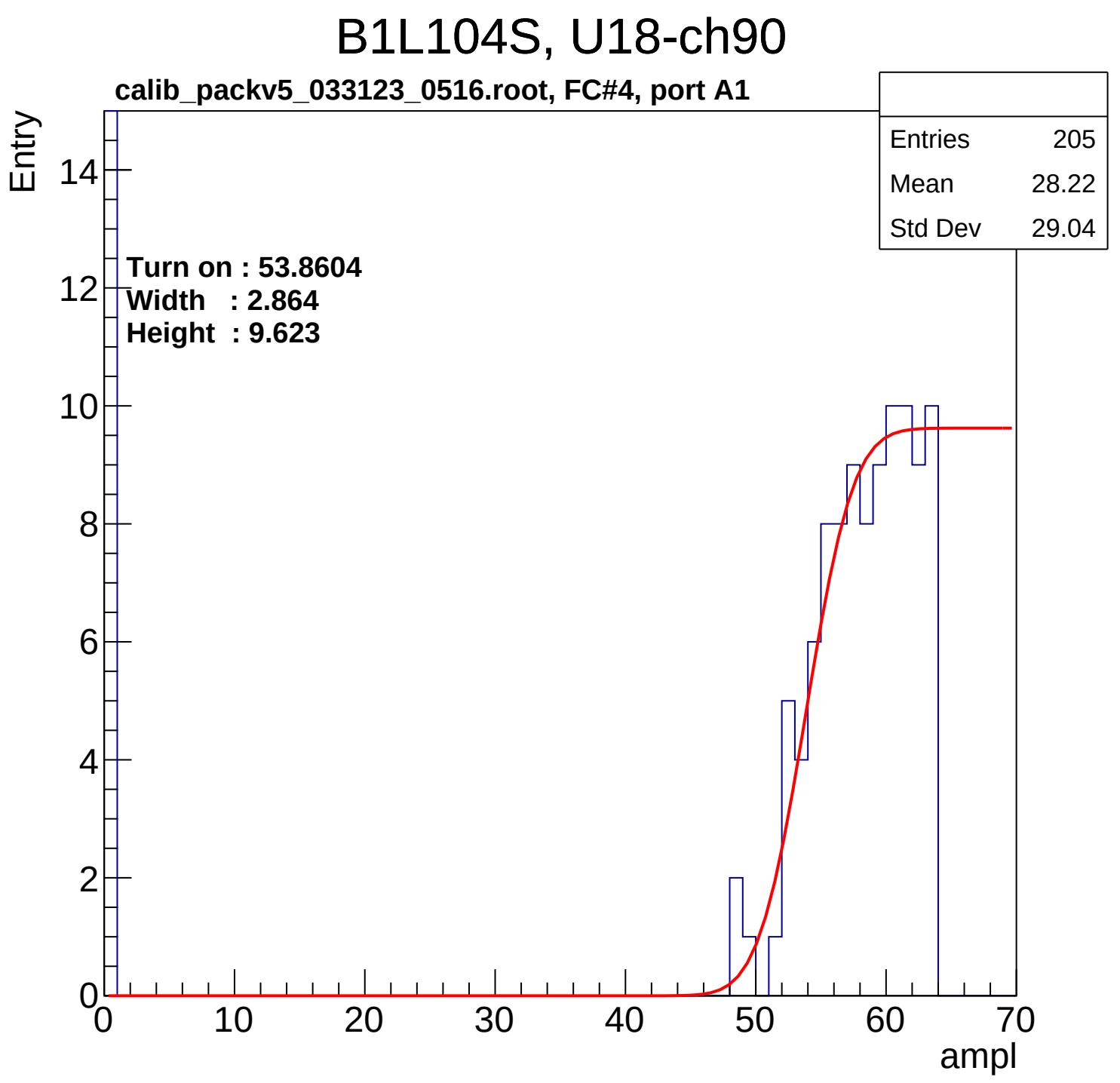

B1L104S, U18-ch85
calib_packv5_033123_0516.root, FC#4, port A1
Entries 176
Mean 34.99
Std Dev 28.27
Turn on : 54.4300
Width : 5.521
Height : 11.222
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

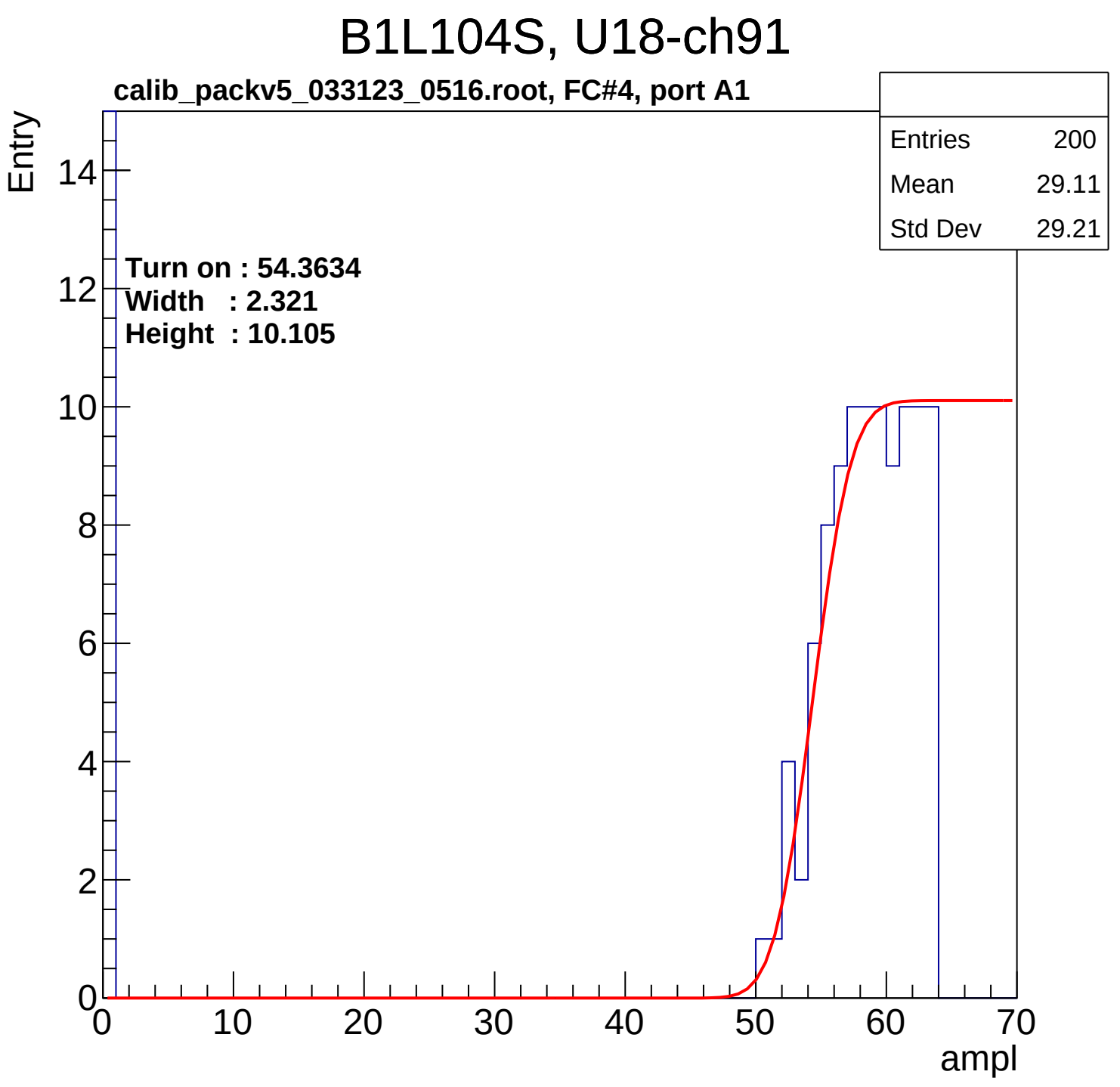

B1L104S, U18-ch86
calib_packv5_033123_0516.root, FC#4, port A1
Entries 179
Mean 31.46
Std Dev 29.05
Turn on : 54.9141
Width : 3.601
Height : 10.278
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

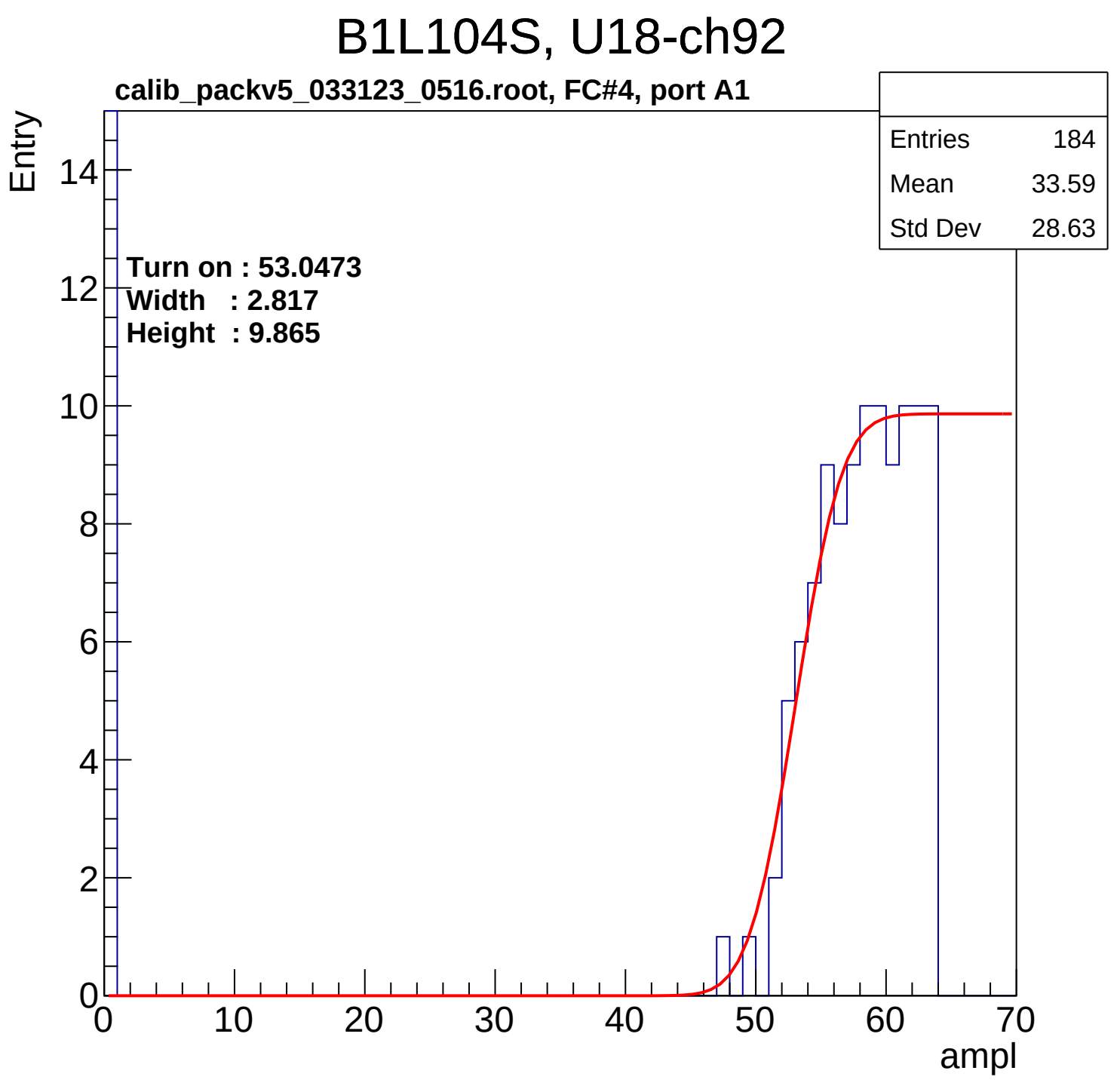

B1L104S, U18-ch87
calib_packv5_033123_0516.root, FC#4, port A1
Entries 224
Mean 28.74
Std Dev 28.87
Turn on : 53.0156
Width : 3.932
Height : 10.186
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

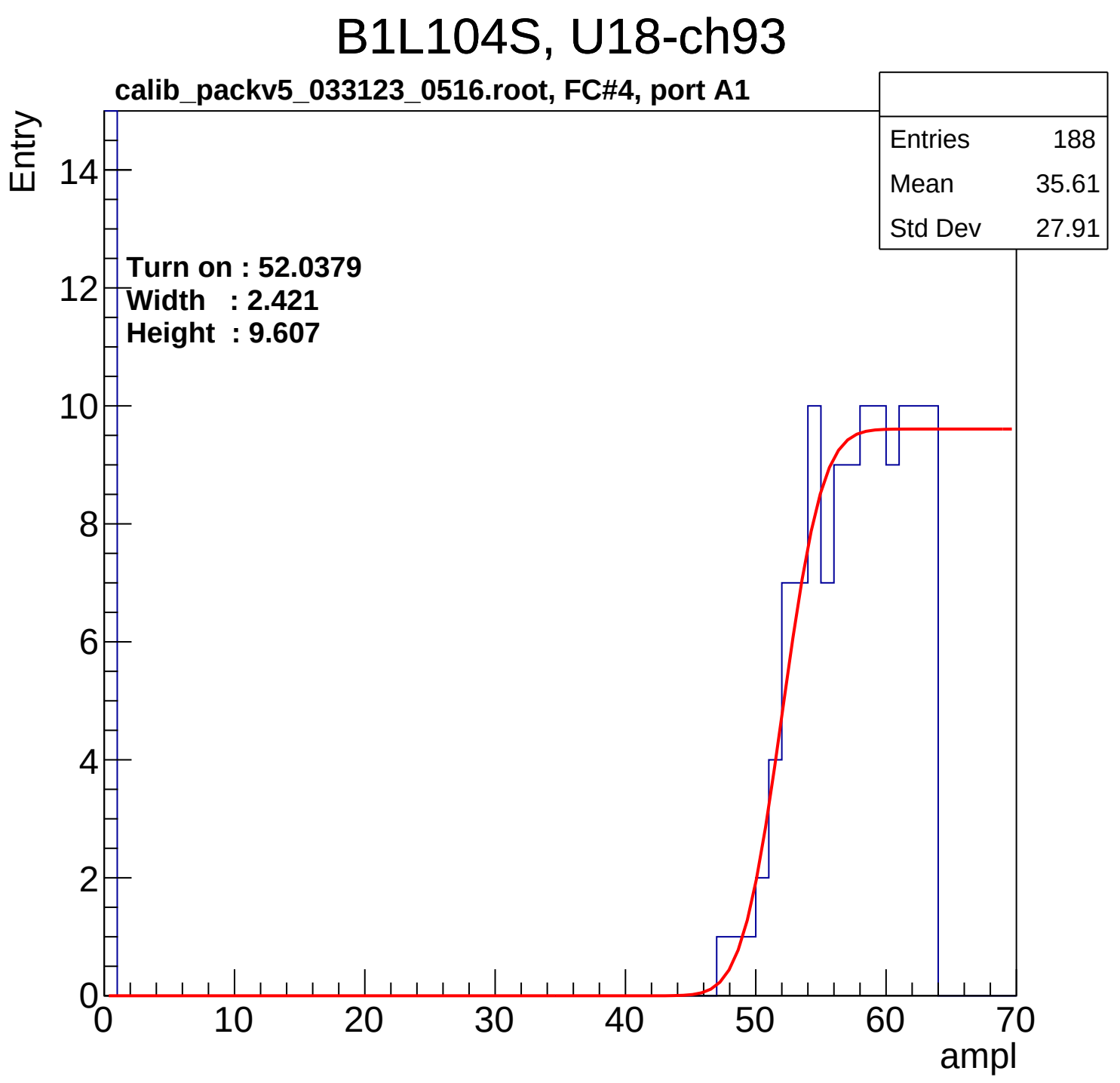

B1L104S, U18-ch88
calib_packv5_033123_0516.root, FC#4, port A1
Entries 200
Mean 30.14
Std Dev 29.07
Turn on : 54.0410
Width : 3.051
Height : 10.278
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

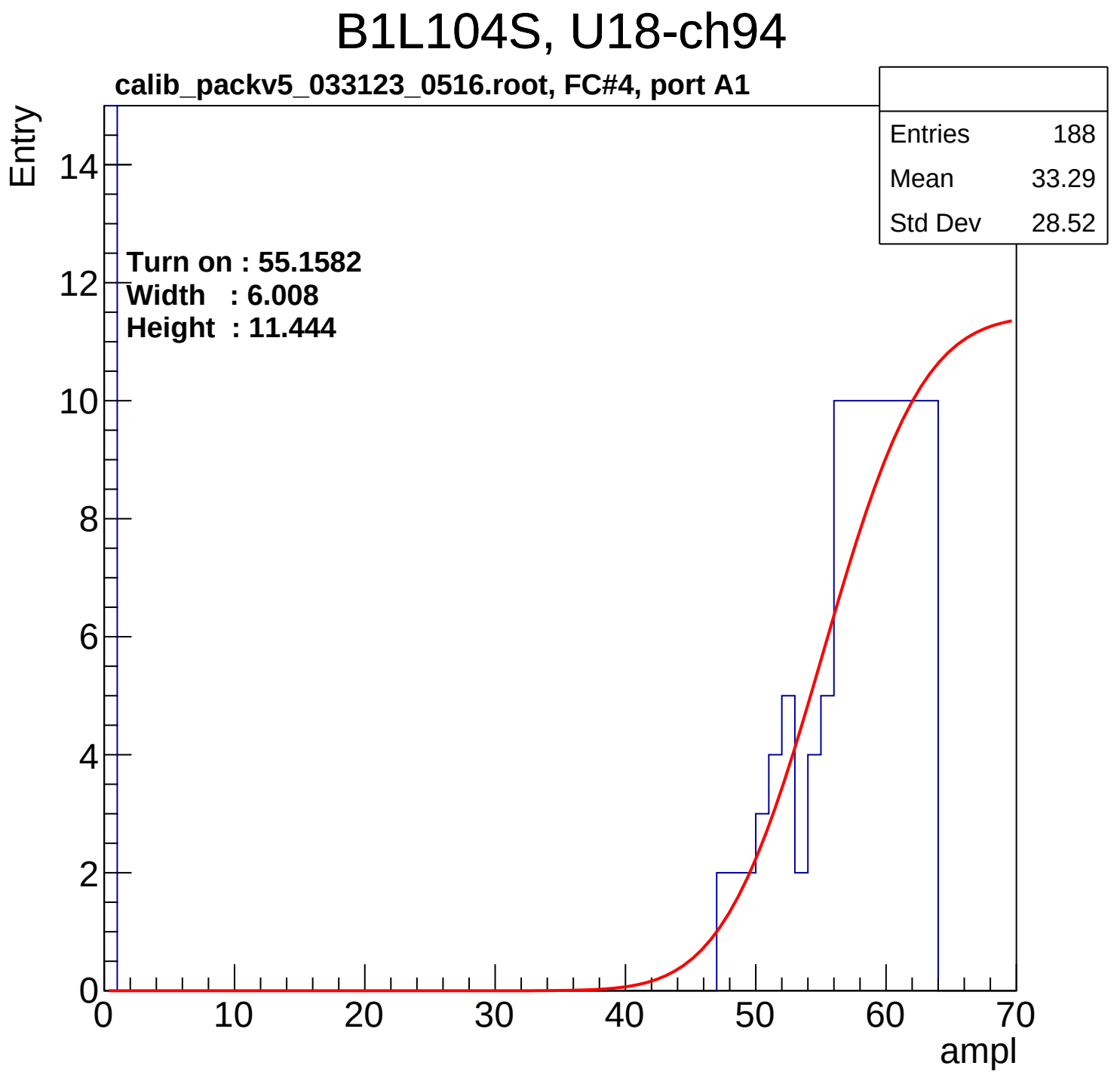

B1L104S, U18-ch89
calib_packv5_033123_0516.root, FC#4, port A1
Entries 184
Mean 33.83
Std Dev 28.52
Turn on : 53.5744
Width : 3.662
Height : 10.190
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

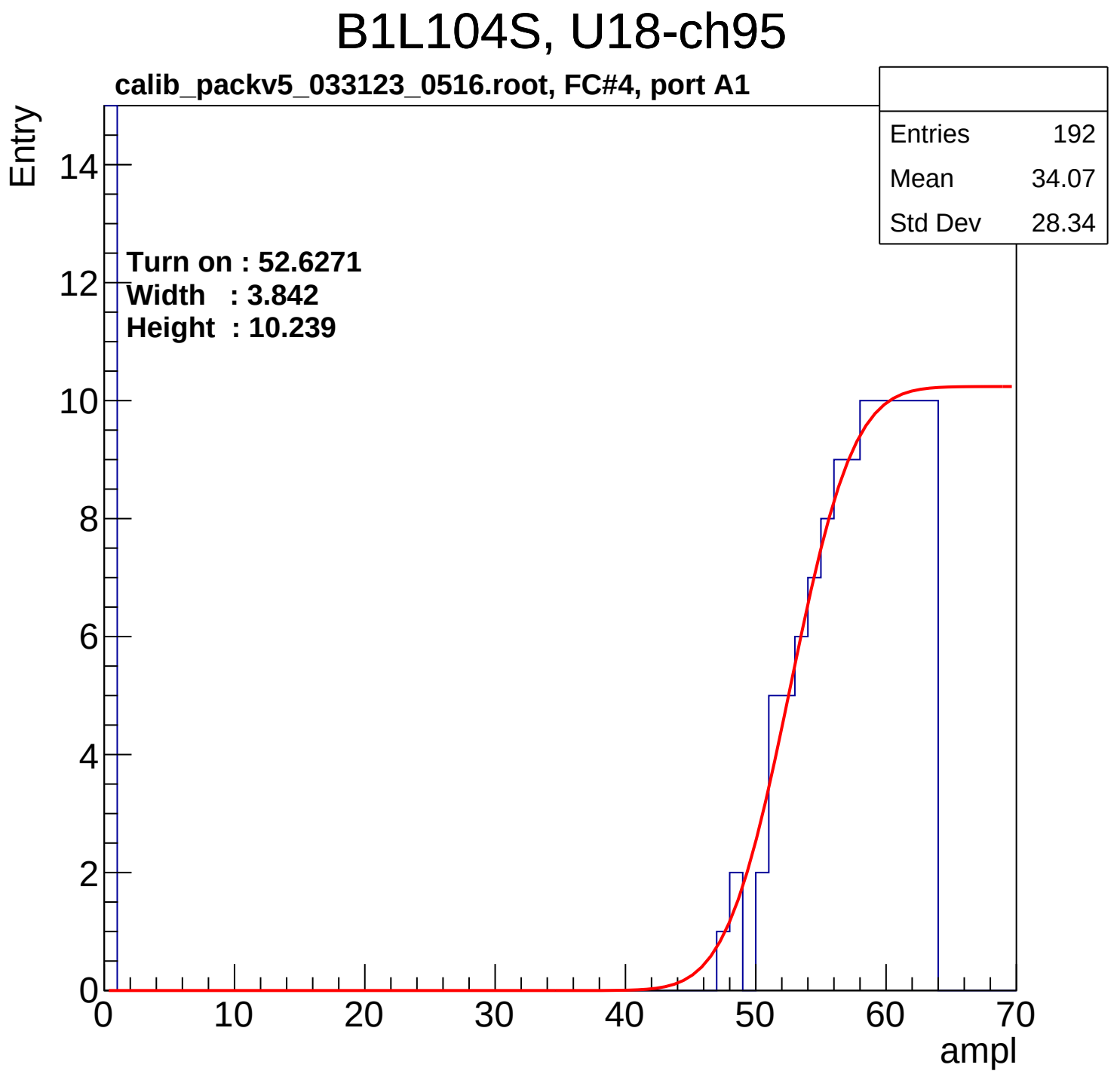

B1L104S, U18-ch90
calib_packv5_033123_0516.root, FC#4, port A1
Entries 205
Mean 28.22
Std Dev 29.04
Turn on : 53.8604
Width : 2.864
Height : 9.623
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

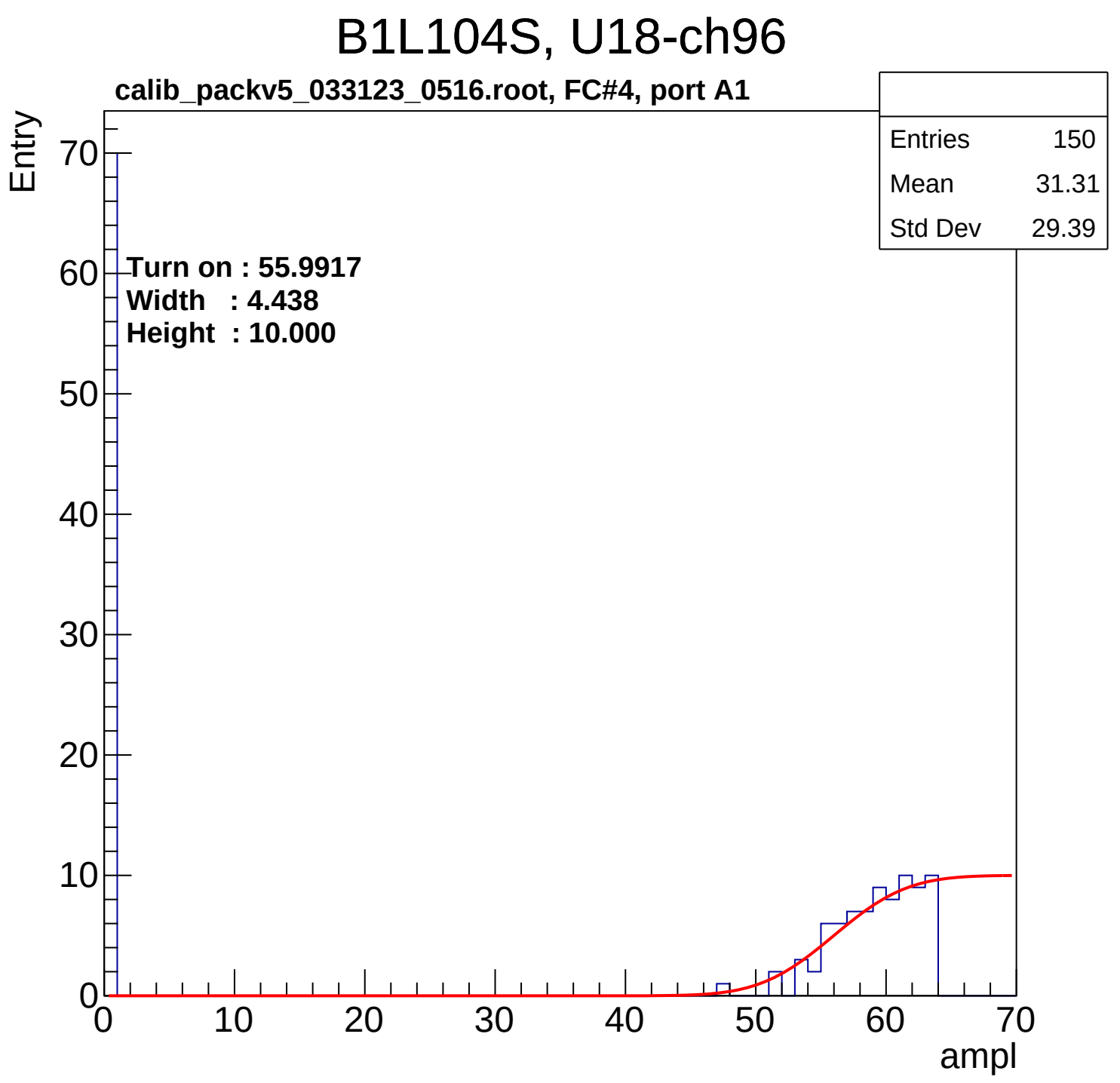

B1L104S, U18-ch91
calib_packv5_033123_0516.root, FC#4, port A1
Entries 200
Mean 29.11
Std Dev 29.21
Turn on : 54.3634
Width : 2.321
Height : 10.105
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

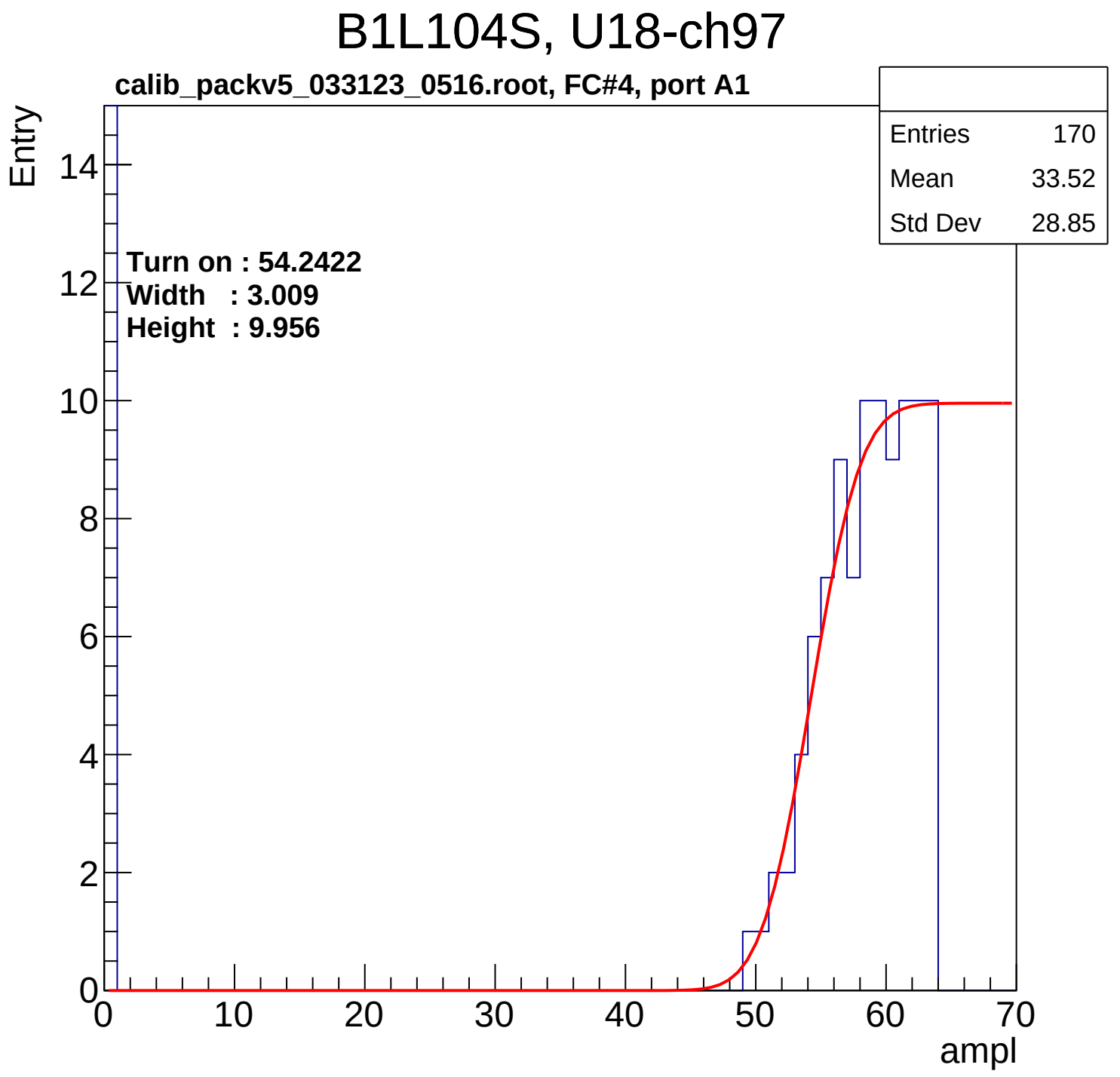

B1L104S, U18-ch92
calib_packv5_033123_0516.root, FC#4, port A1
Entries 184
Mean 33.59
Std Dev 28.63
Turn on : 53.0473
Width : 2.817
Height : 9.865
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

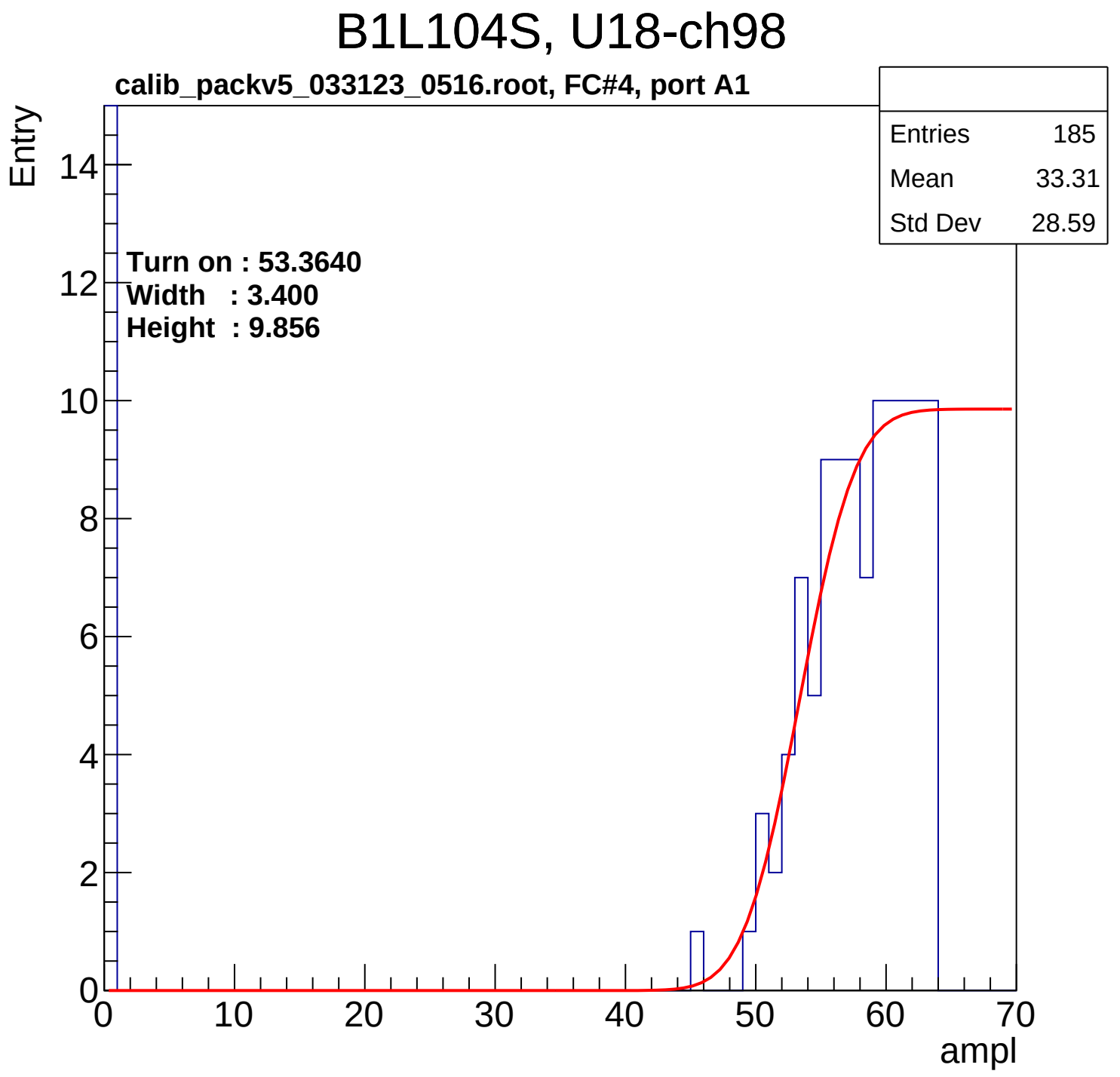

B1L104S, U18-ch93
calib_packv5_033123_0516.root, FC#4, port A1
Entries 188
Mean 35.61
Std Dev 27.91
Turn on : 52.0379
Width : 2.421
Height : 9.607
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

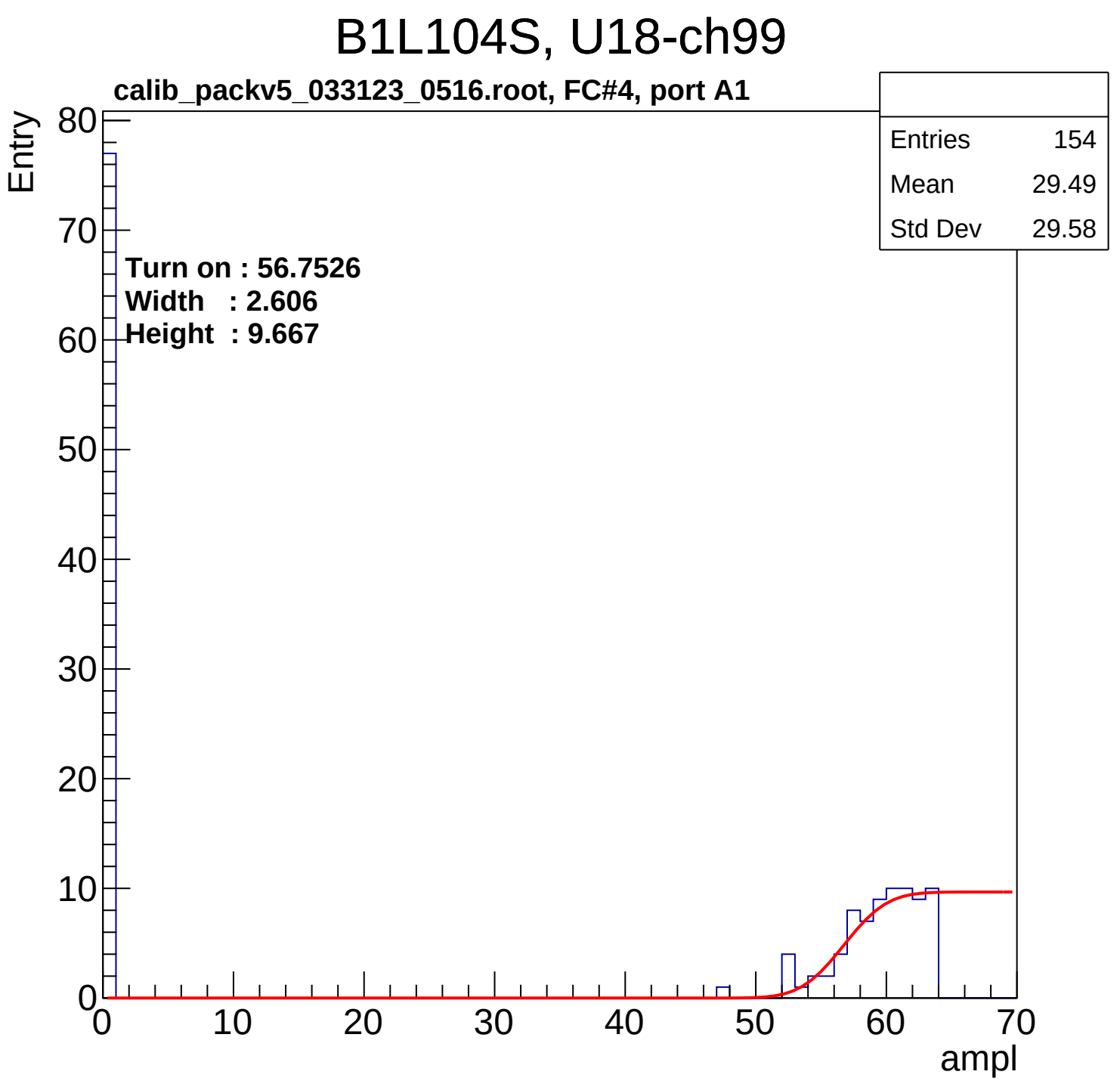

B1L104S, U18-ch94
calib_packv5_033123_0516.root, FC#4, port A1
Entries 188
Mean 33.29
Std Dev 28.52
Turn on : 55.1582
Width : 6.008
Height : 11.444
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

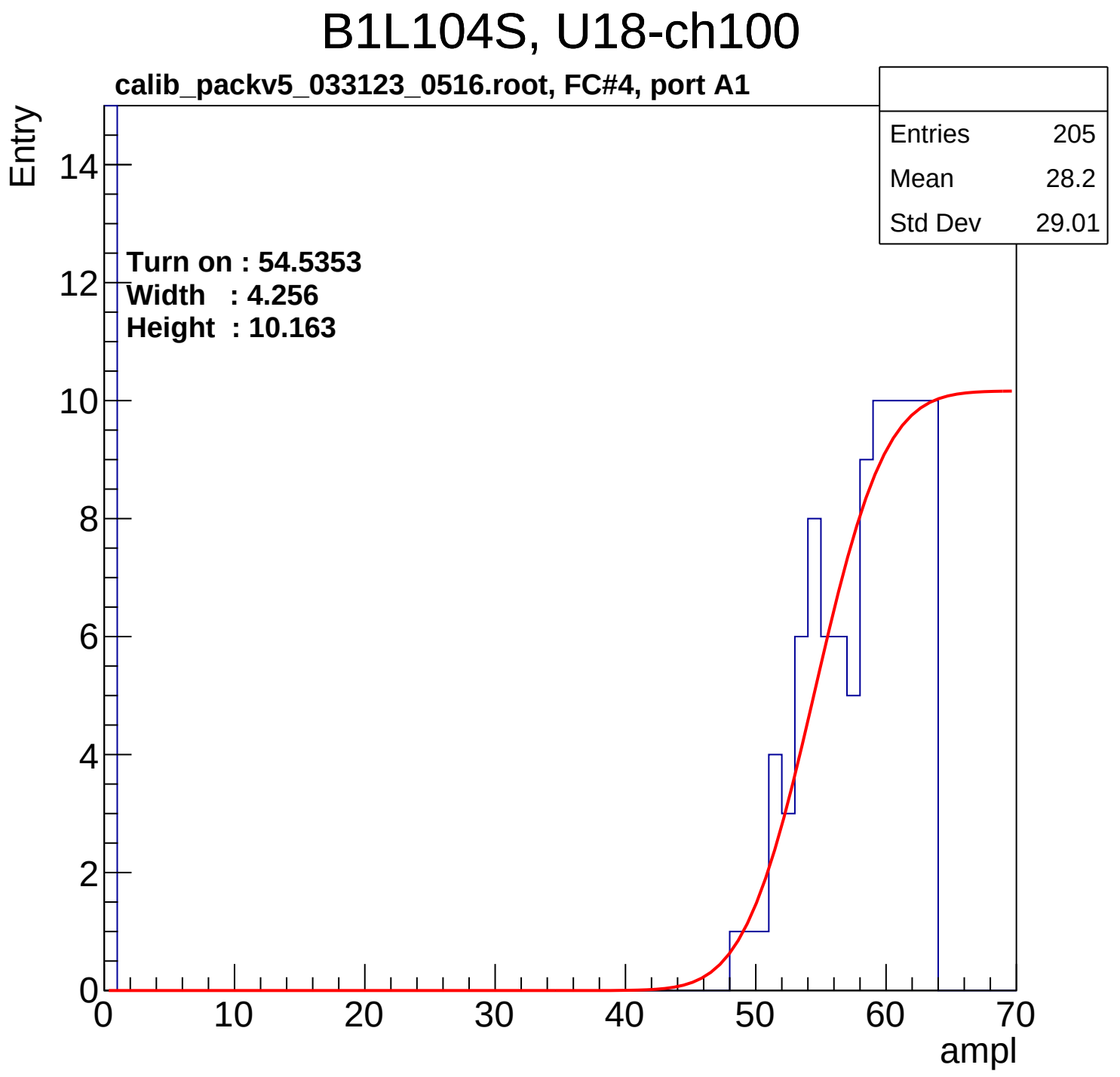

B1L104S, U18-ch95
calib_packv5_033123_0516.root, FC#4, port A1
Entries 192
Mean 34.07
Std Dev 28.34
Turn on : 52.6271
Width : 3.842
Height : 10.239
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

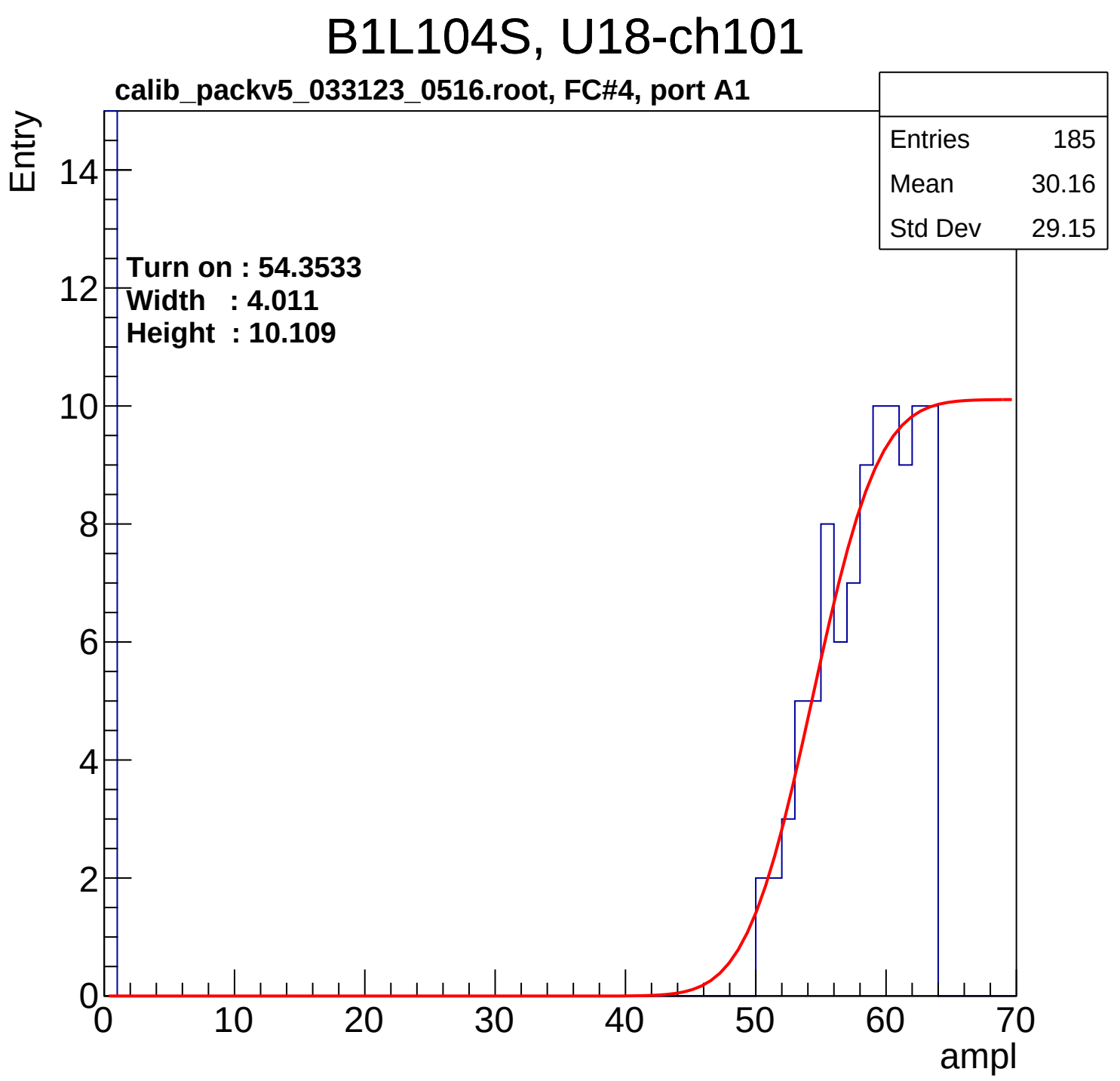

B1L104S, U18-ch96
calib_packv5_033123_0516.root, FC#4, port A1
Entries 150
Mean 31.31
Std Dev 29.39
Turn on : 55.9917
Width : 4.438
Height : 10.000
Entry
ampl
0
10
20
30
40
50
60
70

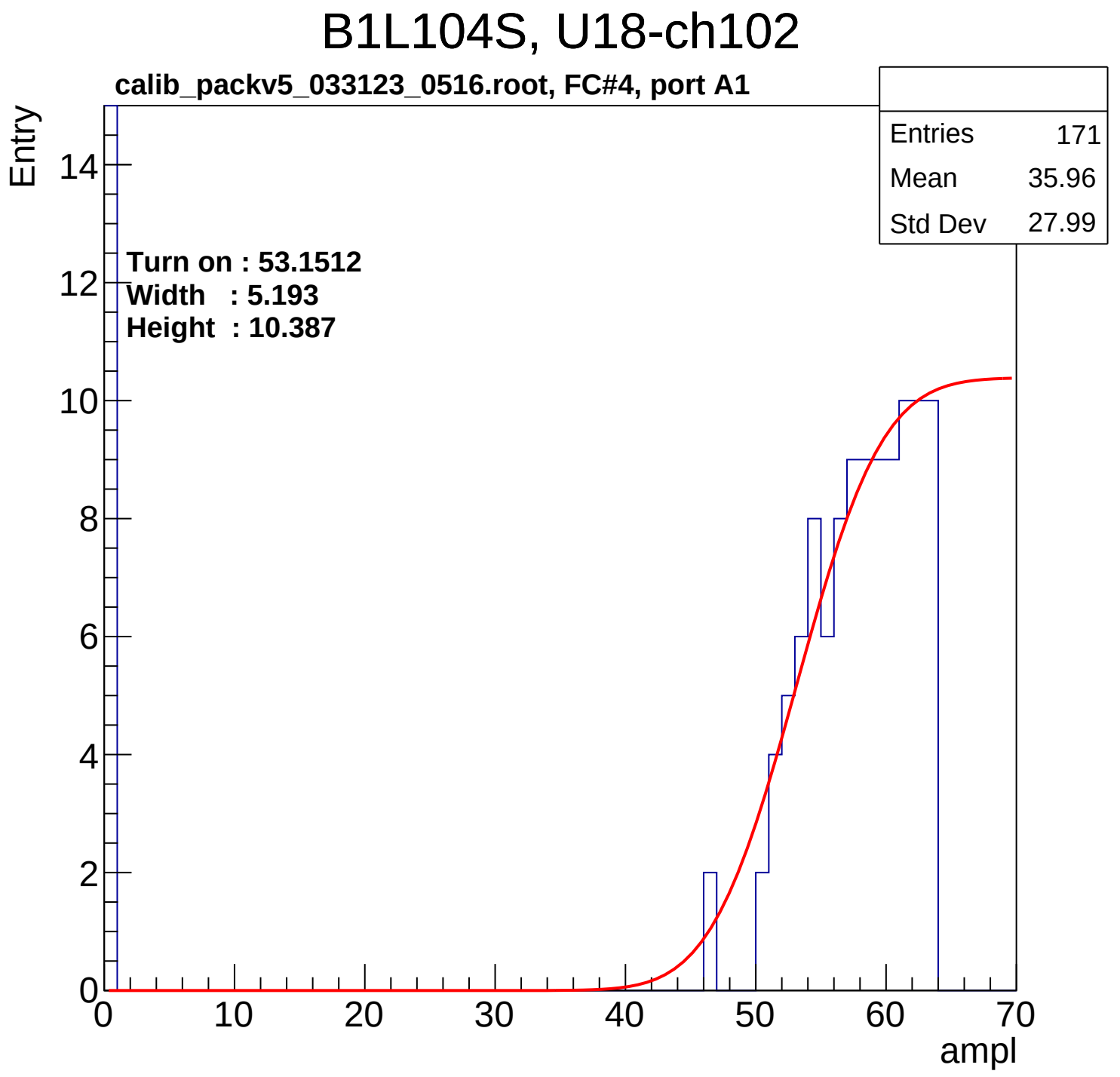

B1L104S, U18-ch97
calib_packv5_033123_0516.root, FC#4, port A1
Entries 170
Mean 33.52
Std Dev 28.85
Turn on : 54.2422
Width : 3.009
Height : 9.956
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

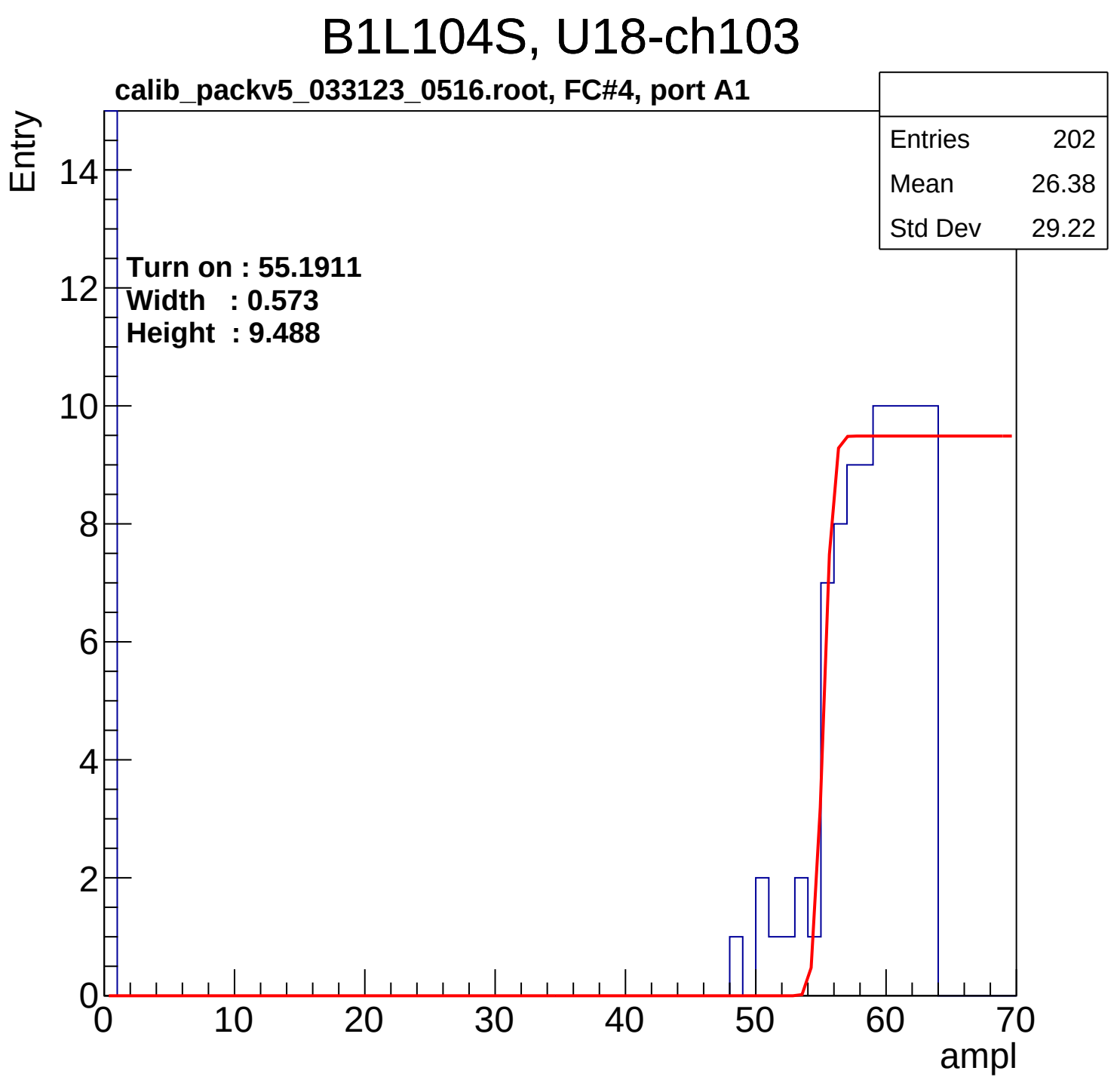

B1L104S, U18-ch98
calib_packv5_033123_0516.root, FC#4, port A1
Entries 185
Mean 33.31
Std Dev 28.59
Turn on : 53.3640
Width : 3.400
Height : 9.856
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

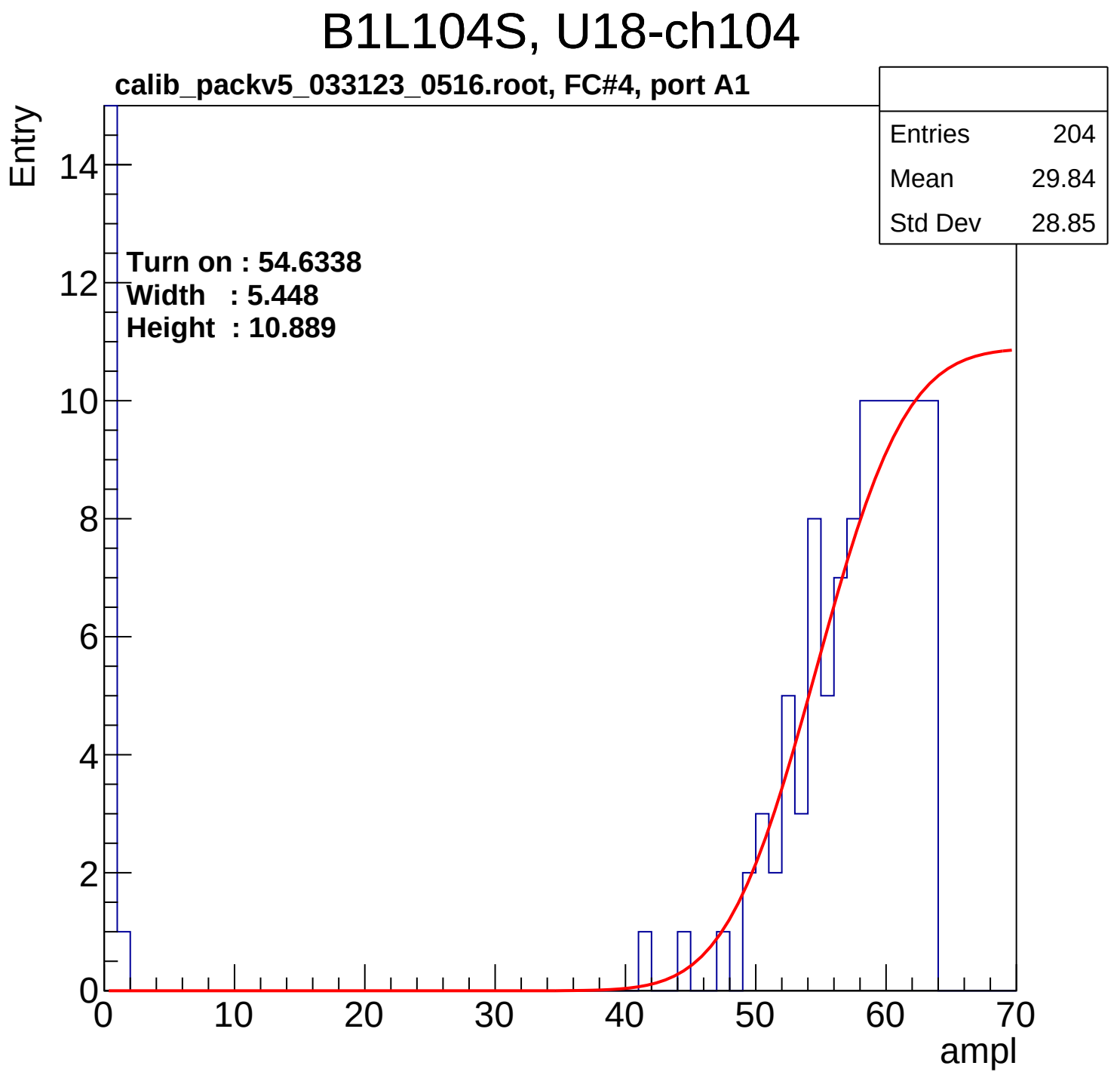

B1L104S, U18-ch99
calib_packv5_033123_0516.root, FC#4, port A1
Entries 154
Mean 29.49
Std Dev 29.58
Turn on : 56.7526
Width : 2.606
Height : 9.667
Entry
ampl
0
10
20
30
40
50
60
70
80

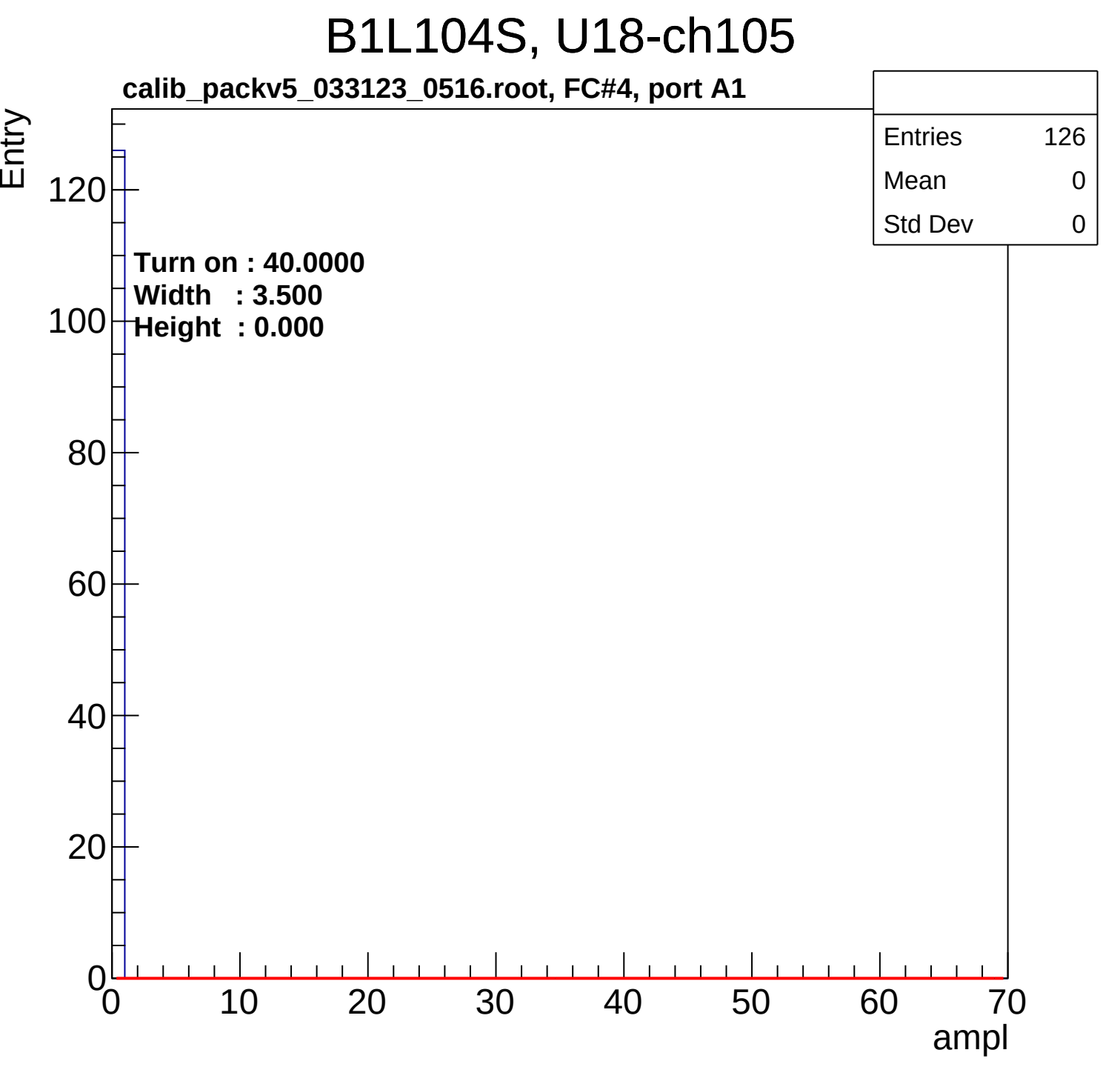

B1L104S, U18-ch100
calib_packv5_033123_0516.root, FC#4, port A1
Entries 205
Mean 28.2
Std Dev 29.01
Turn on : 54.5353
Width : 4.256
Height : 10.163
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

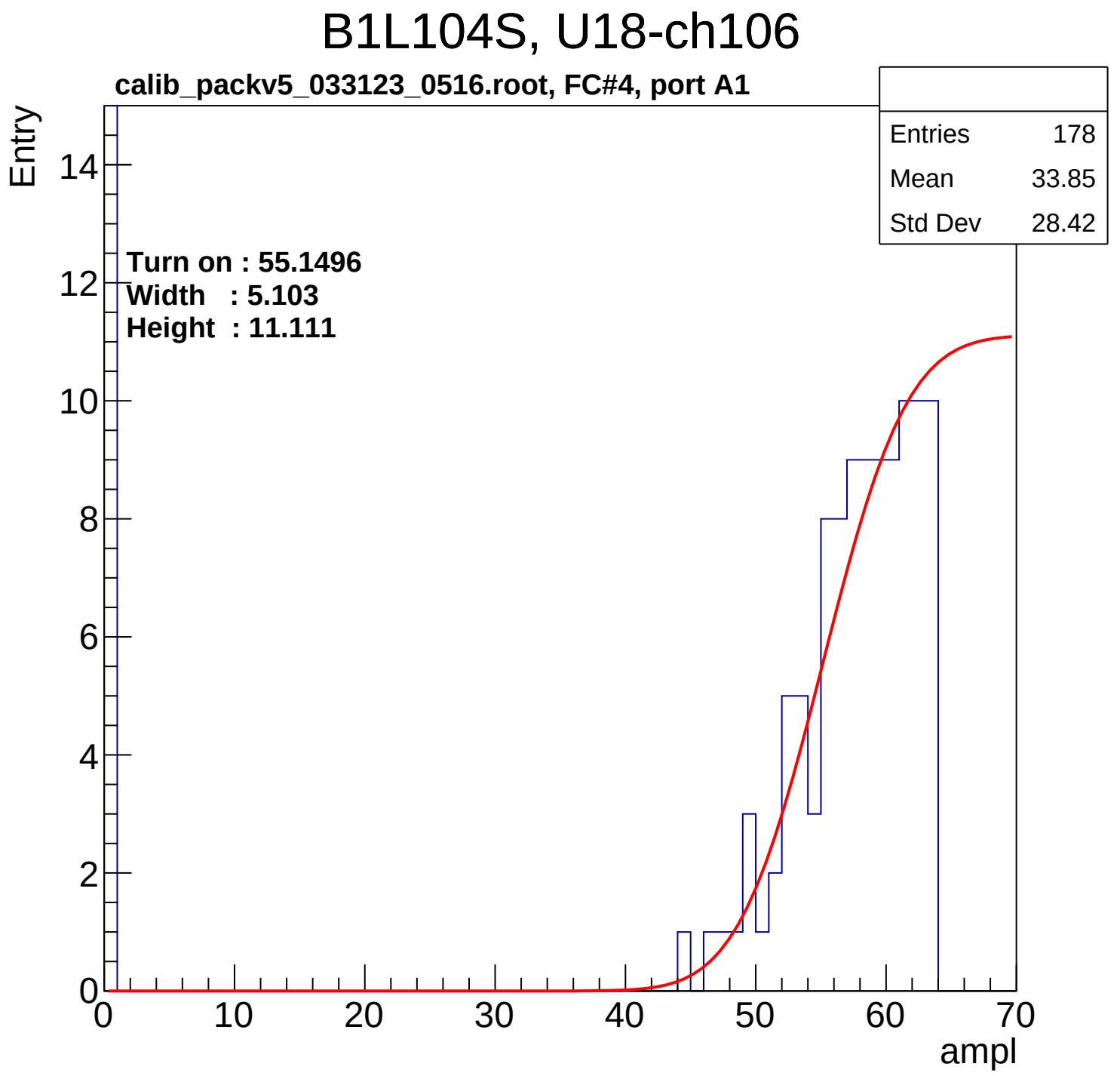

B1L104S, U18-ch101
calib_packv5_033123_0516.root, FC#4, port A1
Entries 185
Mean 30.16
Std Dev 29.15
Turn on : 54.3533
Width : 4.011
Height : 10.109
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

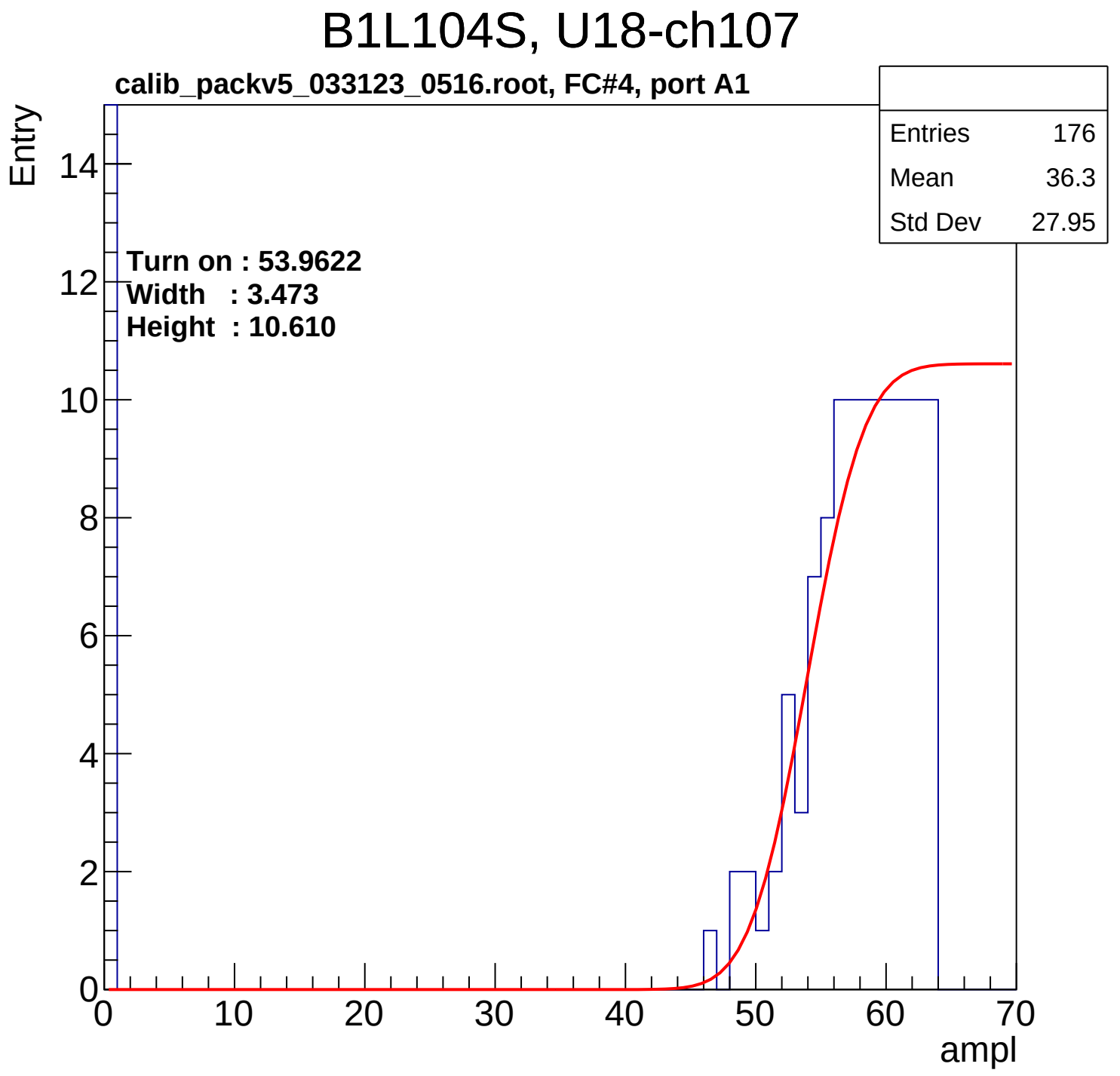

B1L104S, U18-ch102
calib_packv5_033123_0516.root, FC#4, port A1
Entries 171
Mean 35.96
Std Dev 27.99
Turn on : 53.1512
Width : 5.193
Height : 10.387
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

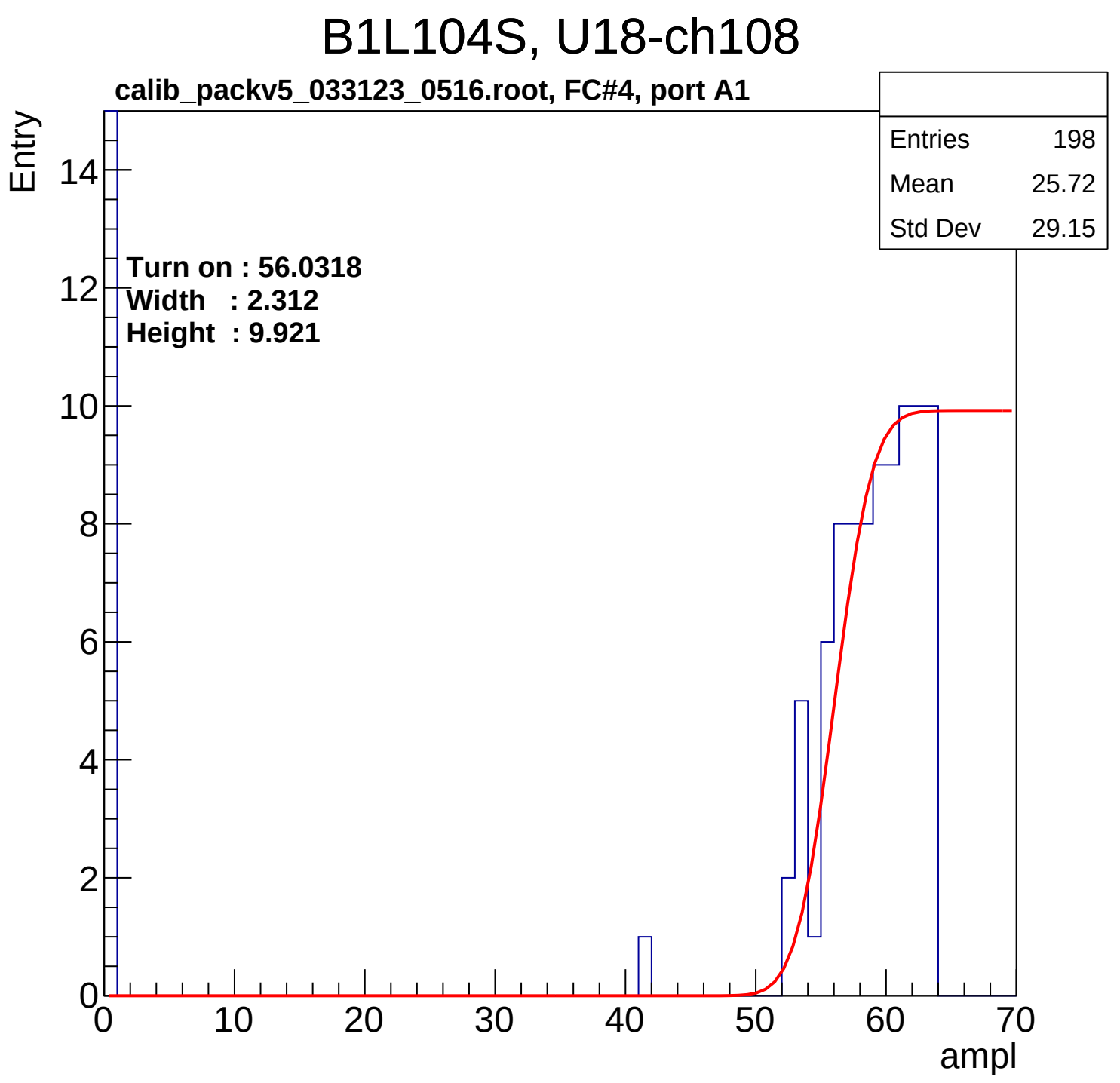

B1L104S, U18-ch103
calib_packv5_033123_0516.root, FC#4, port A1
Entries 202
Mean 26.38
Std Dev 29.22
Turn on : 55.1911
Width : 0.573
Height : 9.488
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

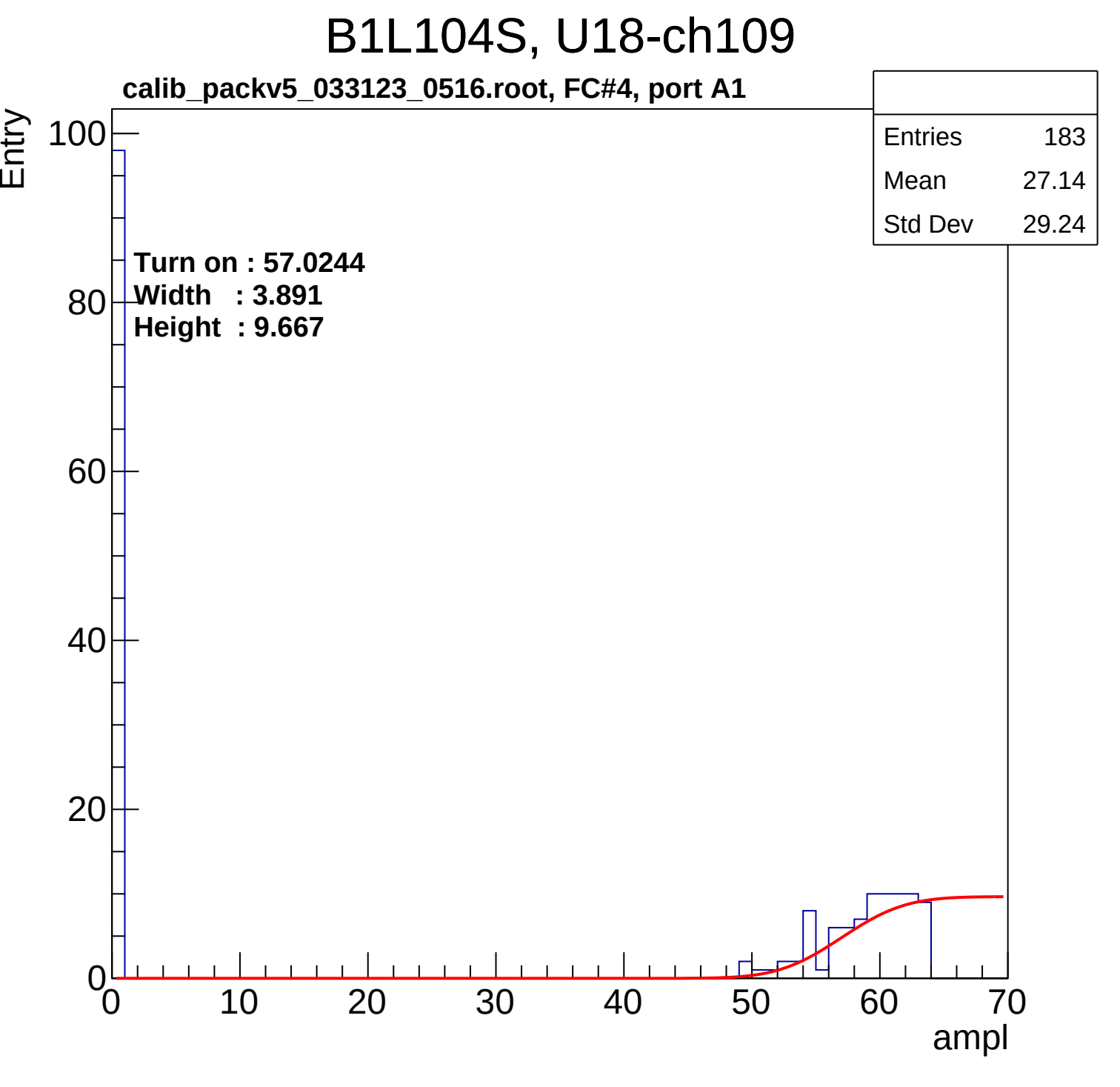

B1L104S, U18-ch104
calib_packv5_033123_0516.root, FC#4, port A1
Entries 204
Mean 29.84
Std Dev 28.85
Turn on : 54.6338
Width : 5.448
Height : 10.889
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

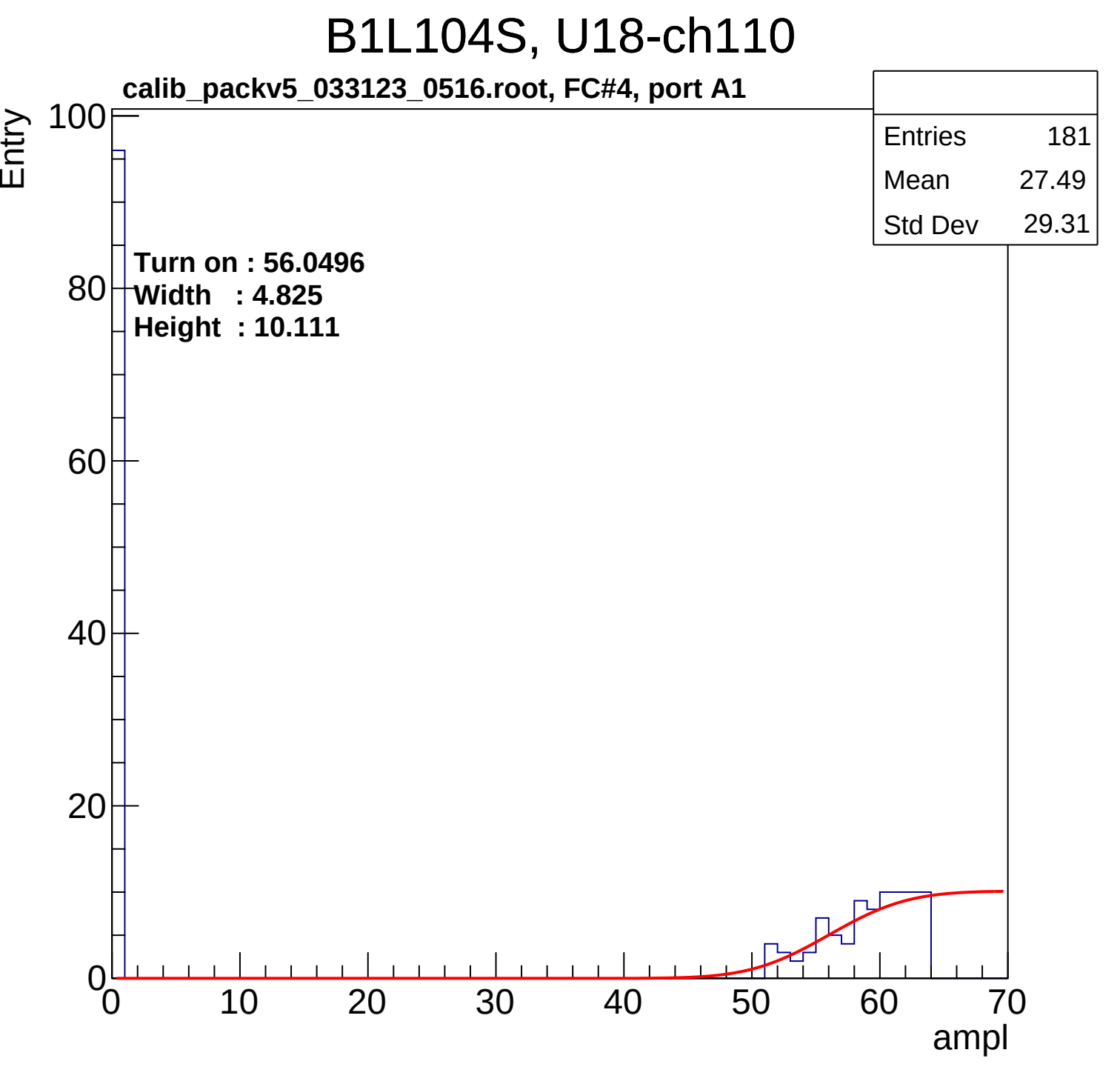

B1L104S, U18-ch105
calib_packv5_033123_0516.root, FC#4, port A1
Entries 126
Mean 0
Std Dev 0
Turn on : 40.0000
Width : 3.500
Height : 0.000
Entry
0
20
40
60
80
100
120
0
10
20
30
40
50
60
70
ampl

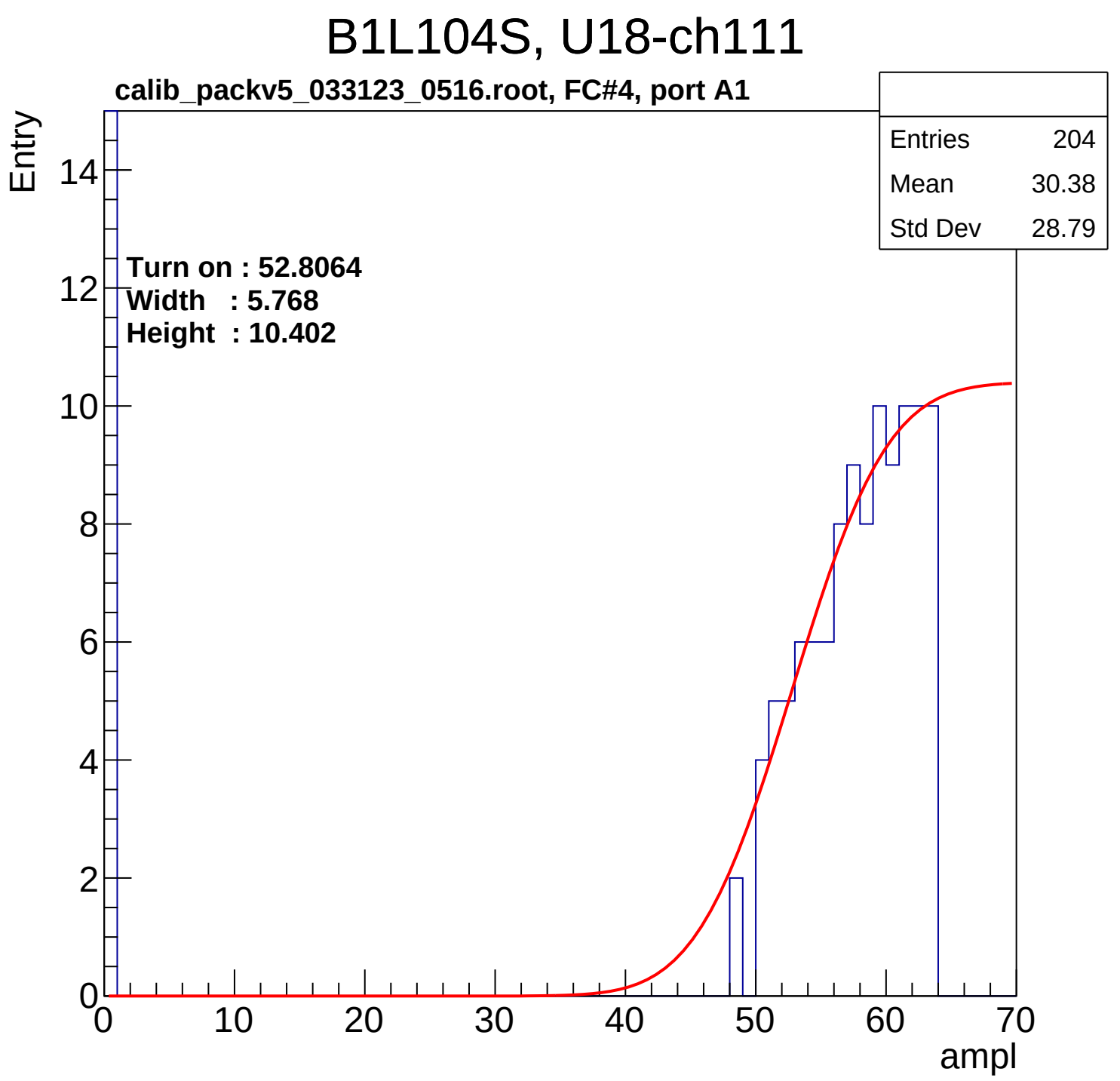

B1L104S, U18-ch106
calib_packv5_033123_0516.root, FC#4, port A1
Entries 178
Mean 33.85
Std Dev 28.42
Turn on : 55.1496
Width : 5.103
Height : 11.111
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

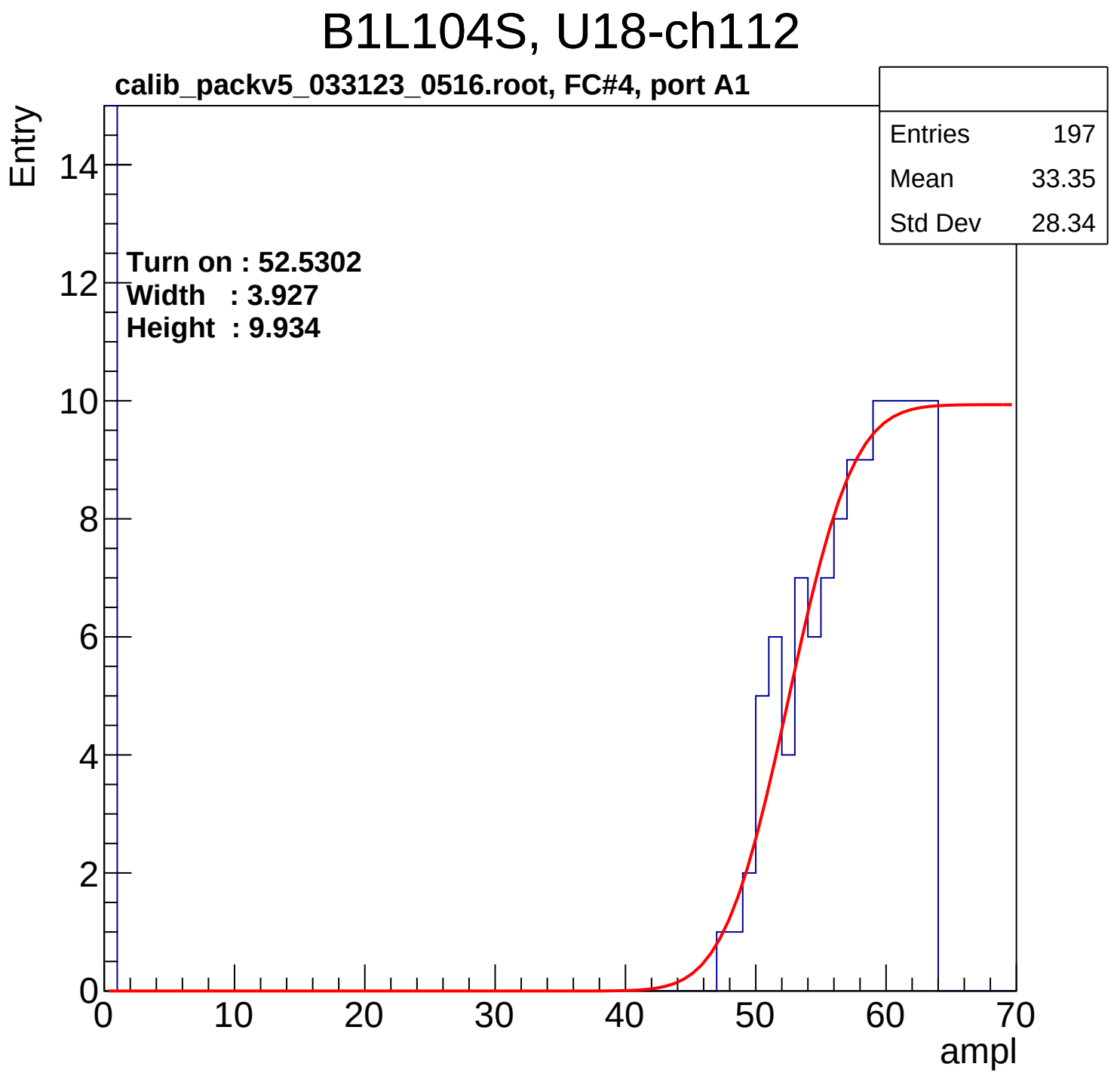

B1L104S, U18-ch107
calib_packv5_033123_0516.root, FC#4, port A1
Entries 176
Mean 36.3
Std Dev 27.95
Turn on : 53.9622
Width : 3.473
Height : 10.610
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

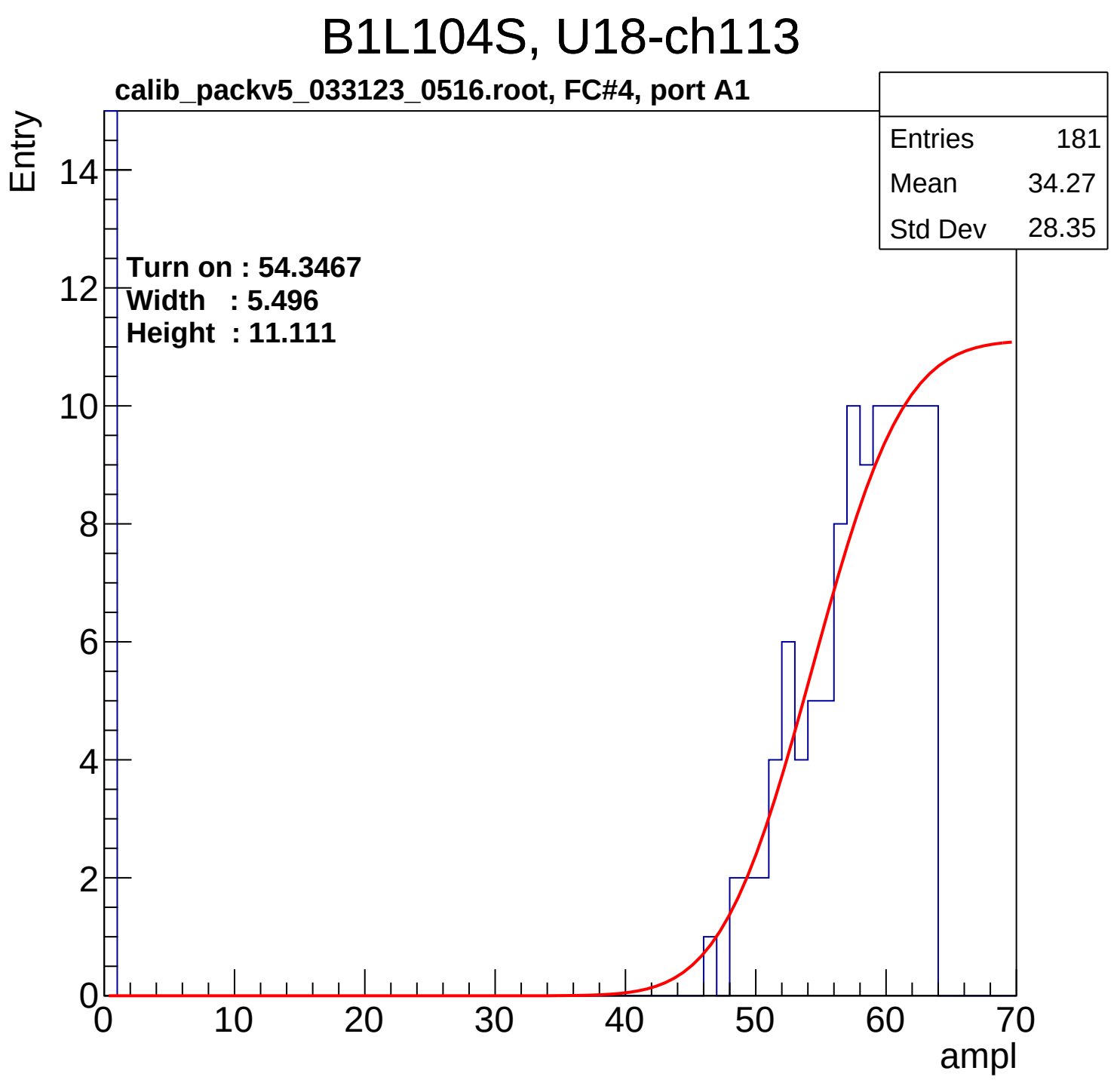

B1L104S, U18-ch108
calib_packv5_033123_0516.root, FC#4, port A1
Entries 198
Mean 25.72
Std Dev 29.15
Turn on : 56.0318
Width : 2.312
Height : 9.921
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

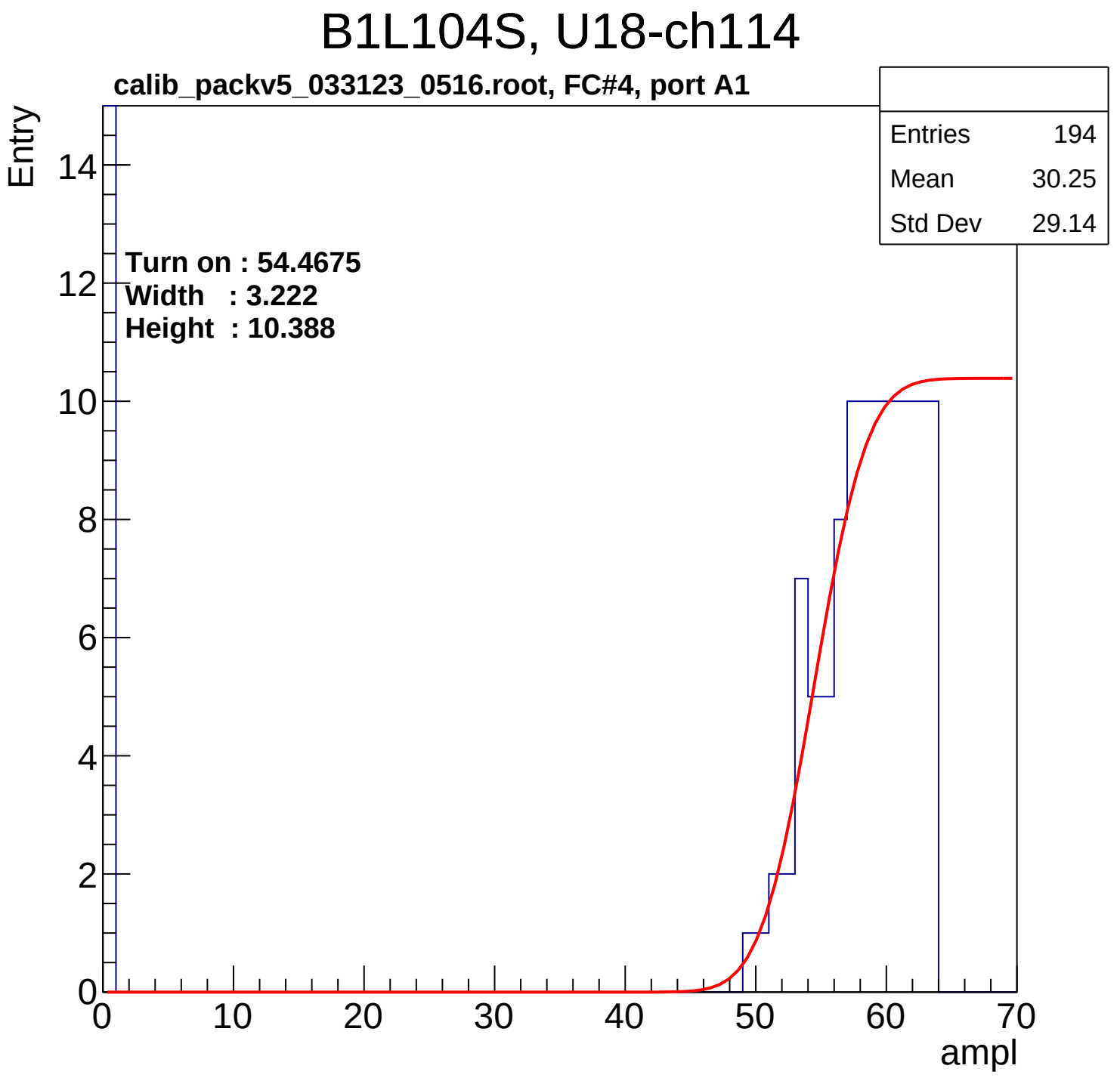

B1L104S, U18-ch109
calib_packv5_033123_0516.root, FC#4, port A1
Entries 183
Mean 27.14
Std Dev 29.24
Turn on : 57.0244
Width : 3.891
Height : 9.667
Entry
ampl
0
20
40
60
80
100
0
10
20
30
40
50
60
70

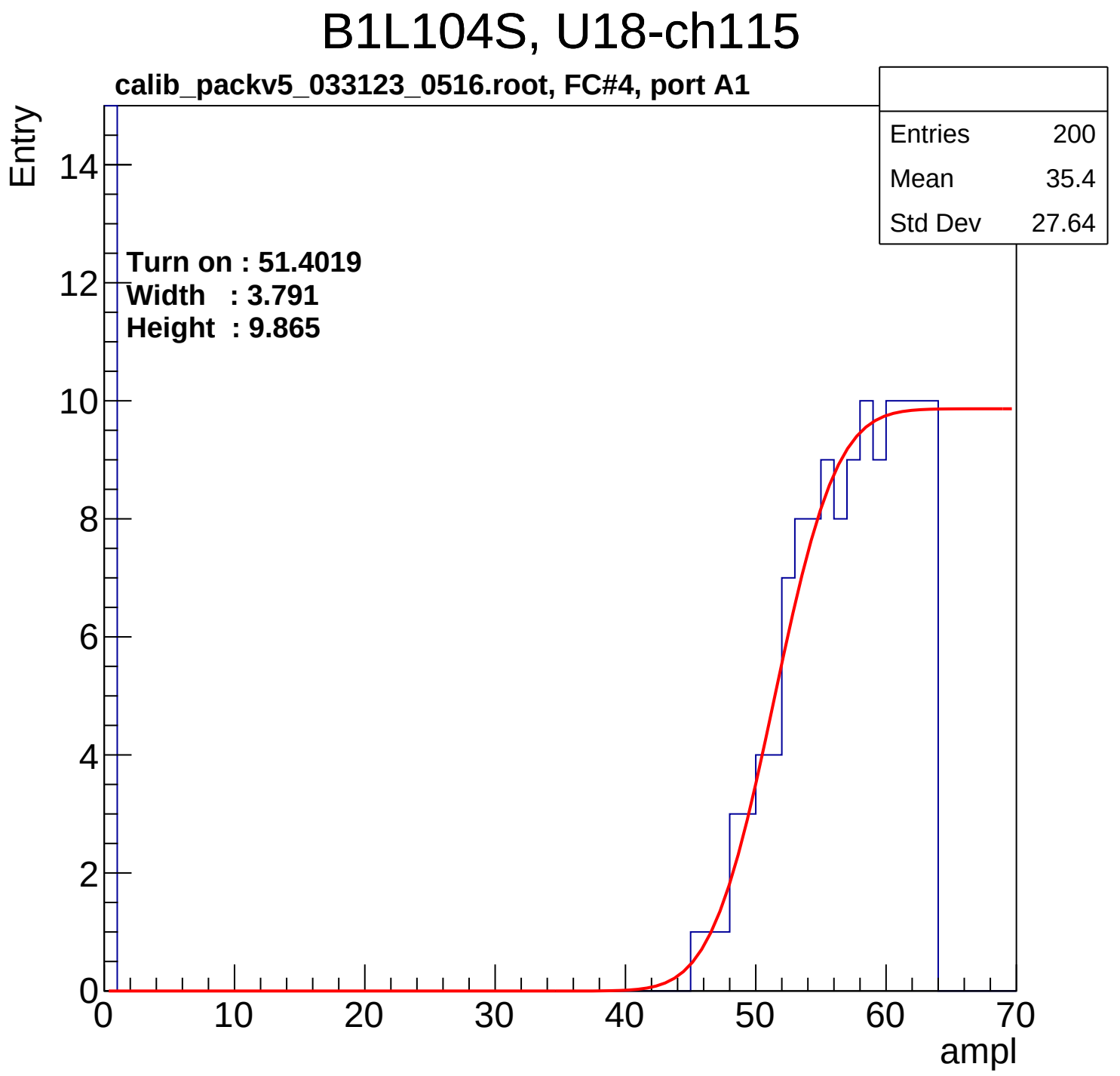

B1L104S, U18-ch110
calib_packv5_033123_0516.root, FC#4, port A1
Entries 181
Mean 27.49
Std Dev 29.31
Turn on : 56.0496
Width : 4.825
Height : 10.111
Entry
ampl
0
20
40
60
80
100
0
10
20
30
40
50
60
70

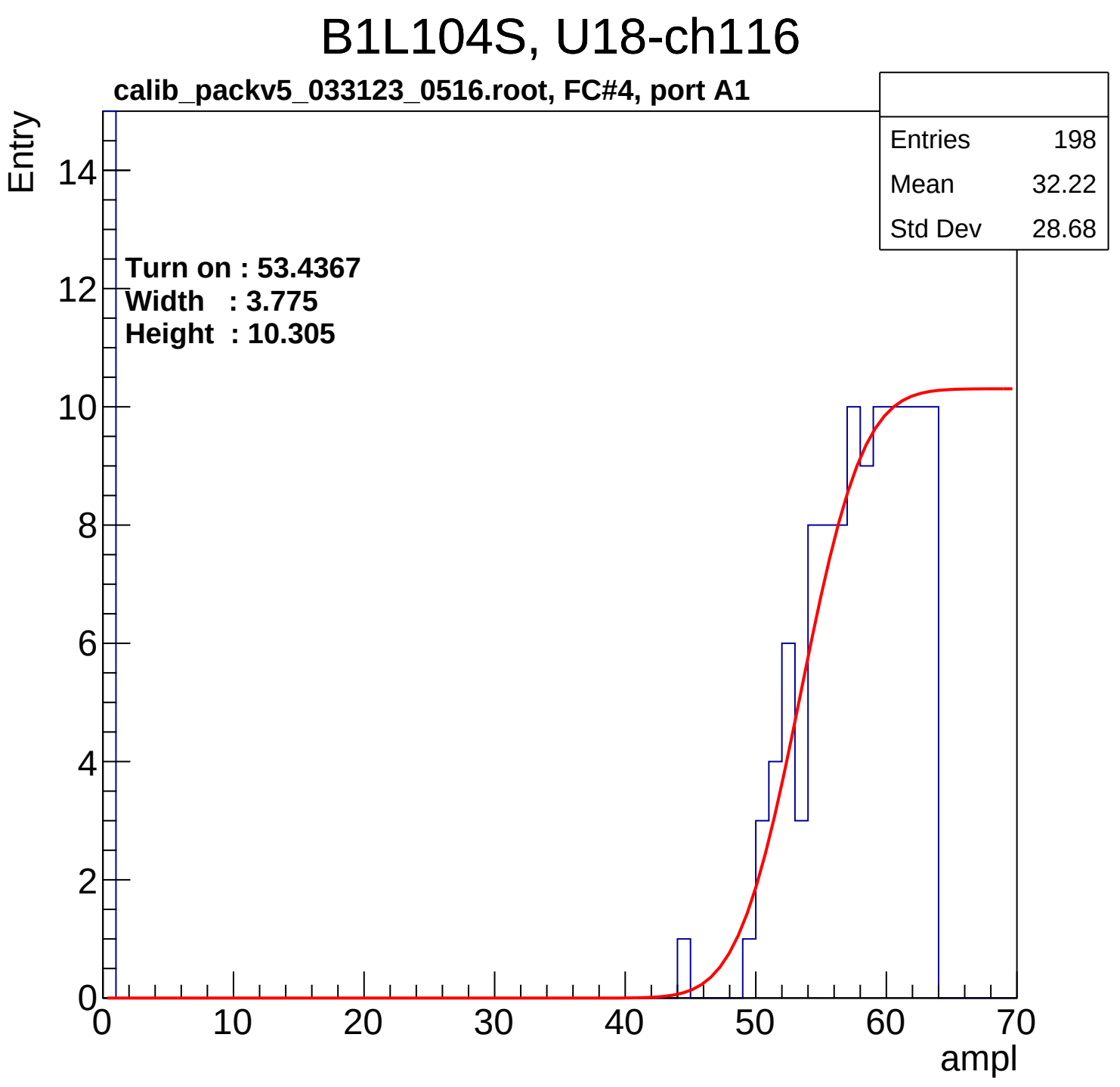

B1L104S, U18-ch111
calib_packv5_033123_0516.root, FC#4, port A1
Entries 204
Mean 30.38
Std Dev 28.79
Turn on : 52.8064
Width : 5.768
Height : 10.402
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

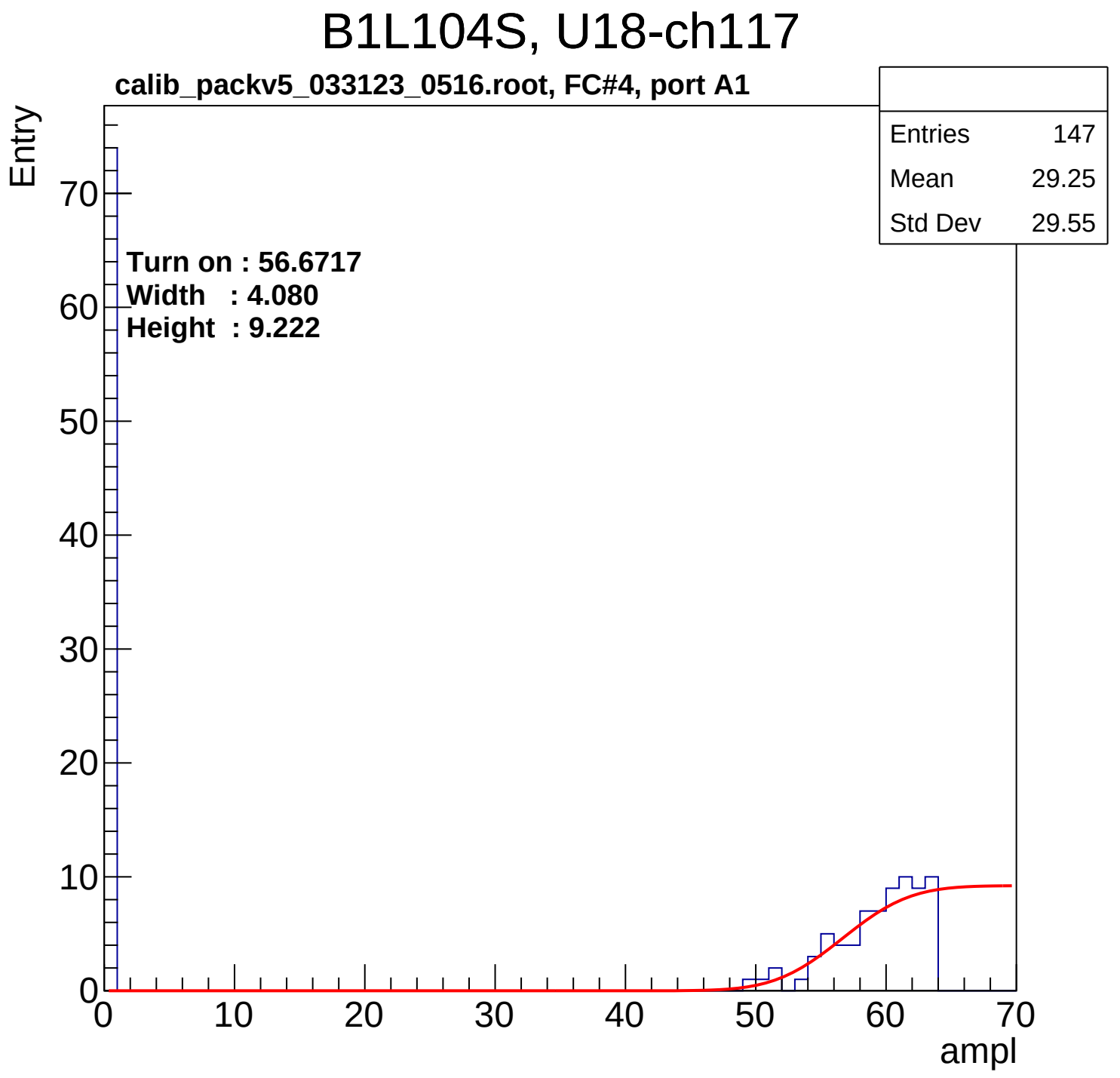

B1L104S, U18-ch112
calib_packv5_033123_0516.root, FC#4, port A1
Entries 197
Mean 33.35
Std Dev 28.34
Turn on : 52.5302
Width : 3.927
Height : 9.934
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

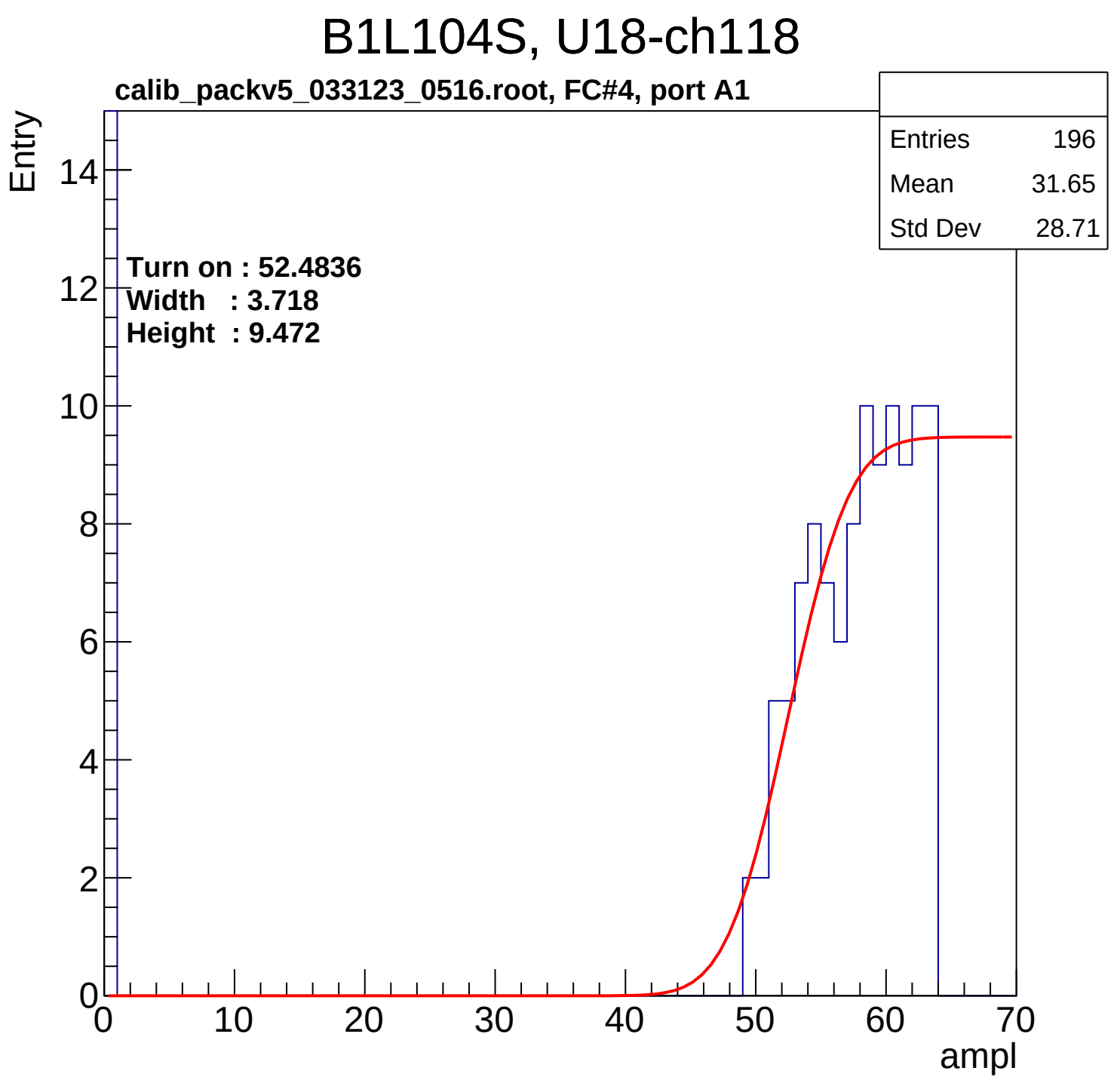

B1L104S, U18-ch113
calib_packv5_033123_0516.root, FC#4, port A1
Entries 181
Mean 34.27
Std Dev 28.35
Turn on : 54.3467
Width : 5.496
Height : 11.111
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

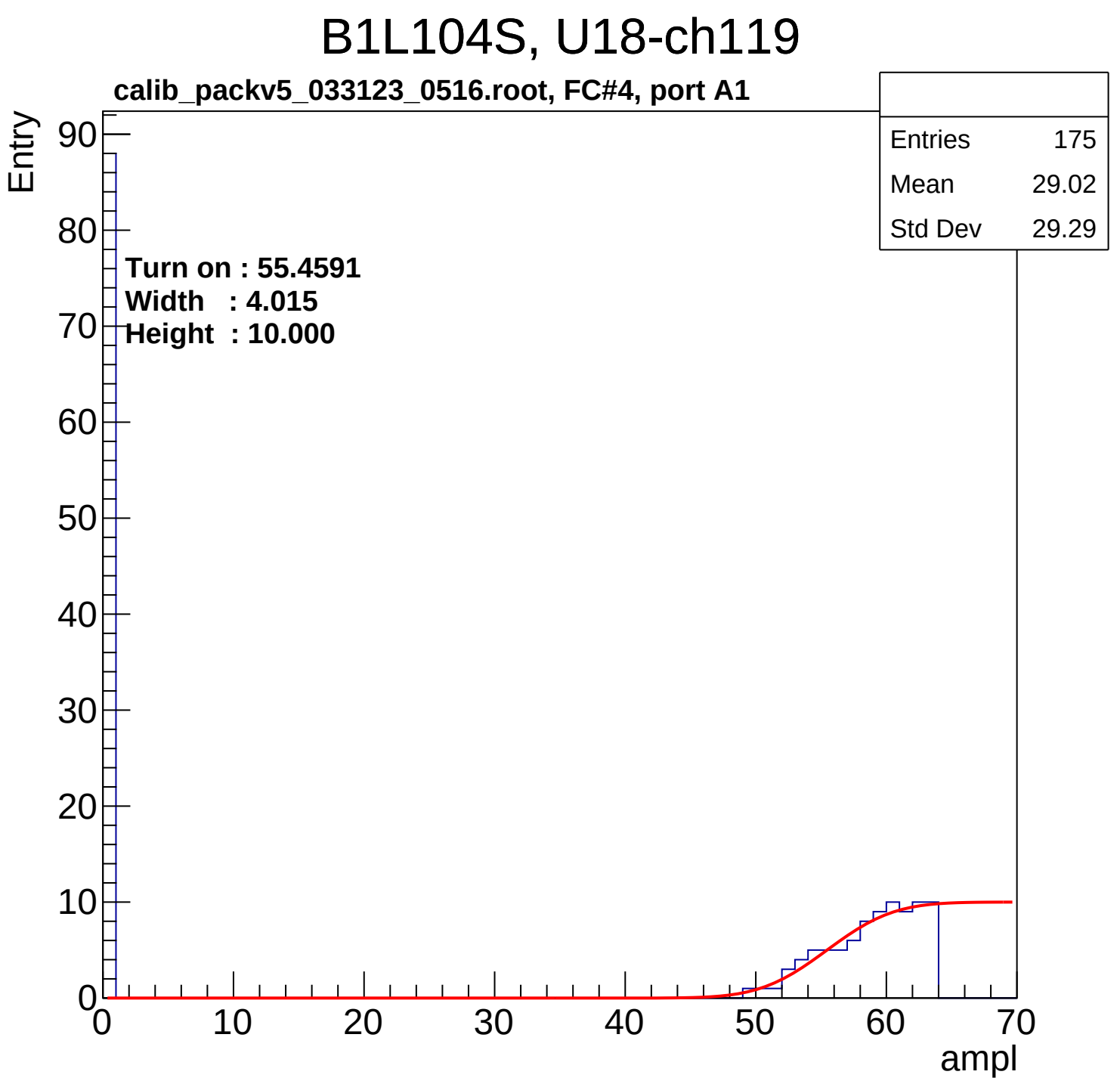

B1L104S, U18-ch114
calib_packv5_033123_0516.root, FC#4, port A1
Entries 194
Mean 30.25
Std Dev 29.14
Turn on : 54.4675
Width : 3.222
Height : 10.388
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

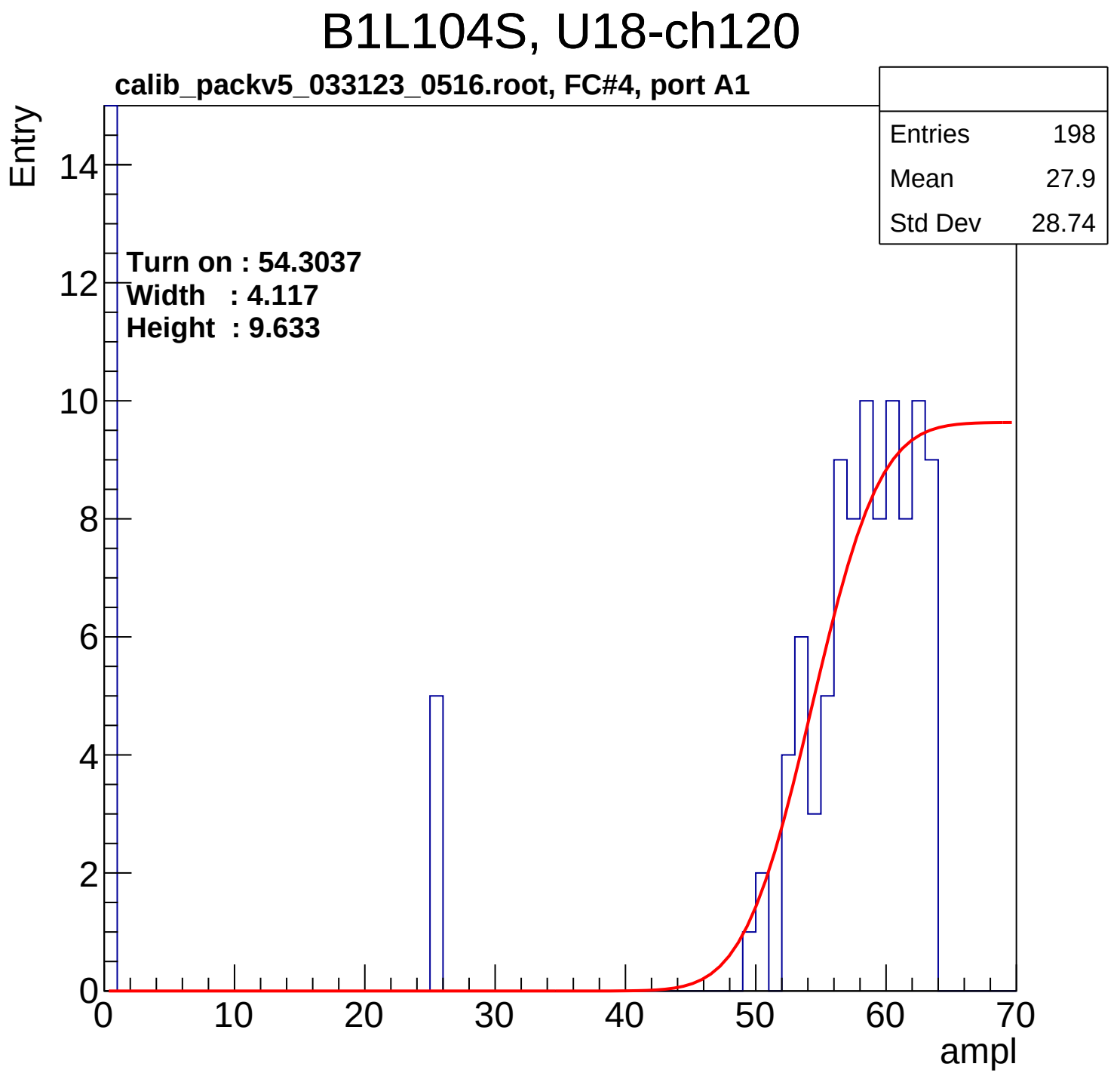

B1L104S, U18-ch115
calib_packv5_033123_0516.root, FC#4, port A1
Entries 200
Mean 35.4
Std Dev 27.64
Turn on : 51.4019
Width : 3.791
Height : 9.865
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

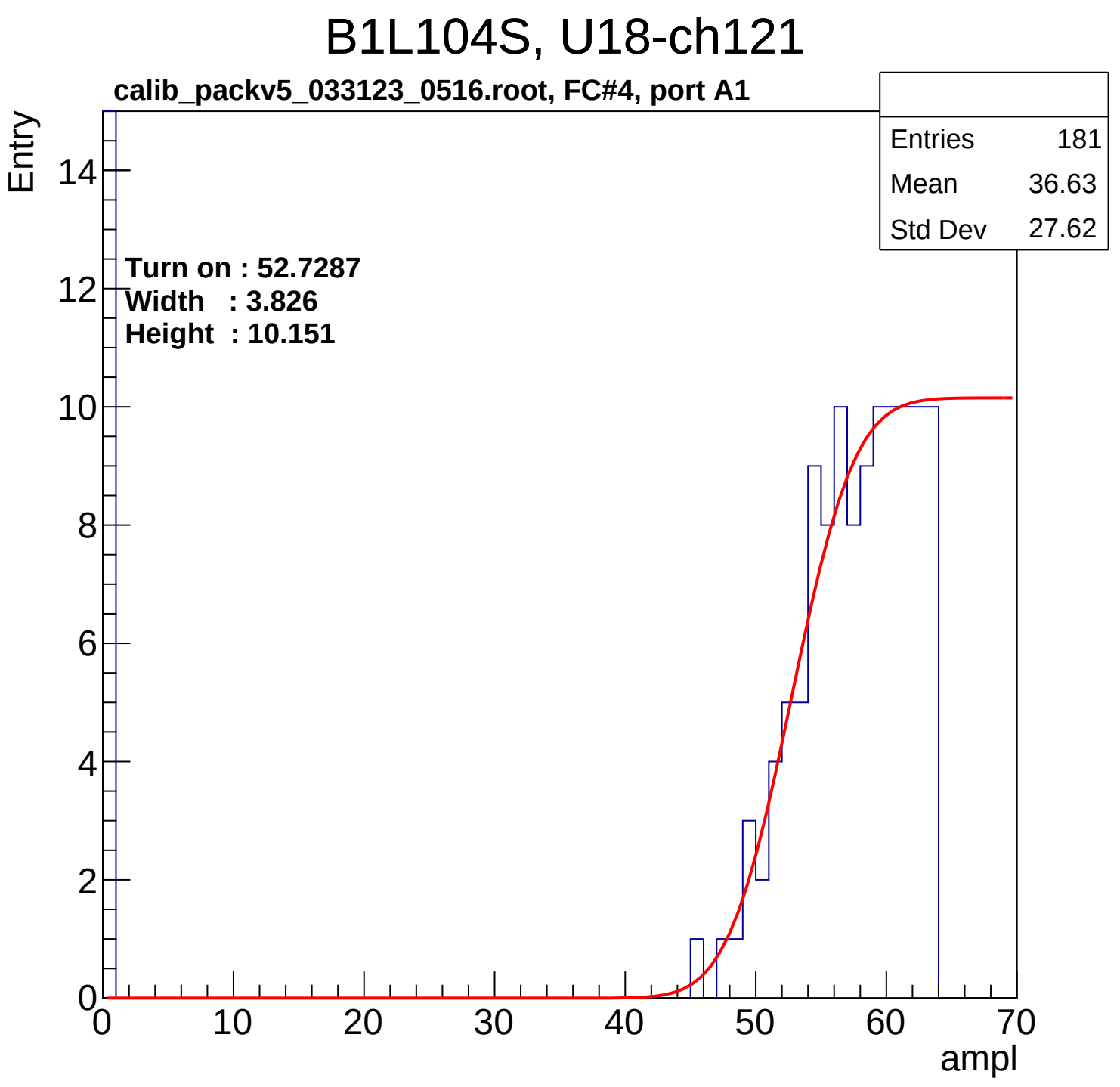

B1L104S, U18-ch116
calib_packv5_033123_0516.root, FC#4, port A1
Entries 198
Mean 32.22
Std Dev 28.68
Turn on : 53.4367
Width : 3.775
Height : 10.305
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

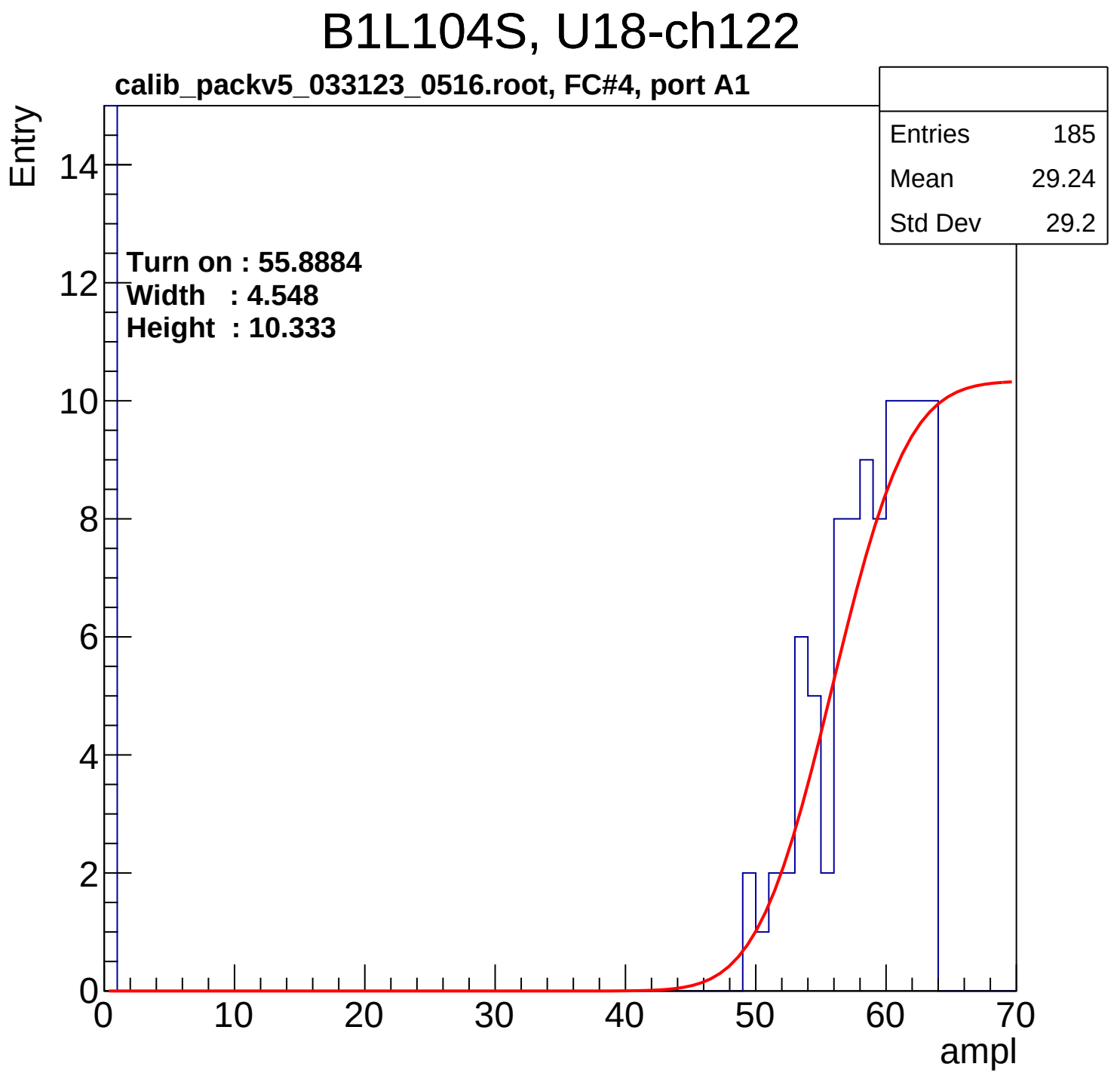

B1L104S, U18-ch117
calib_packv5_033123_0516.root, FC#4, port A1
Entries 147
Mean 29.25
Std Dev 29.55
Turn on : 56.6717
Width : 4.080
Height : 9.222
Entry
ampl
0
10
20
30
40
50
60
70

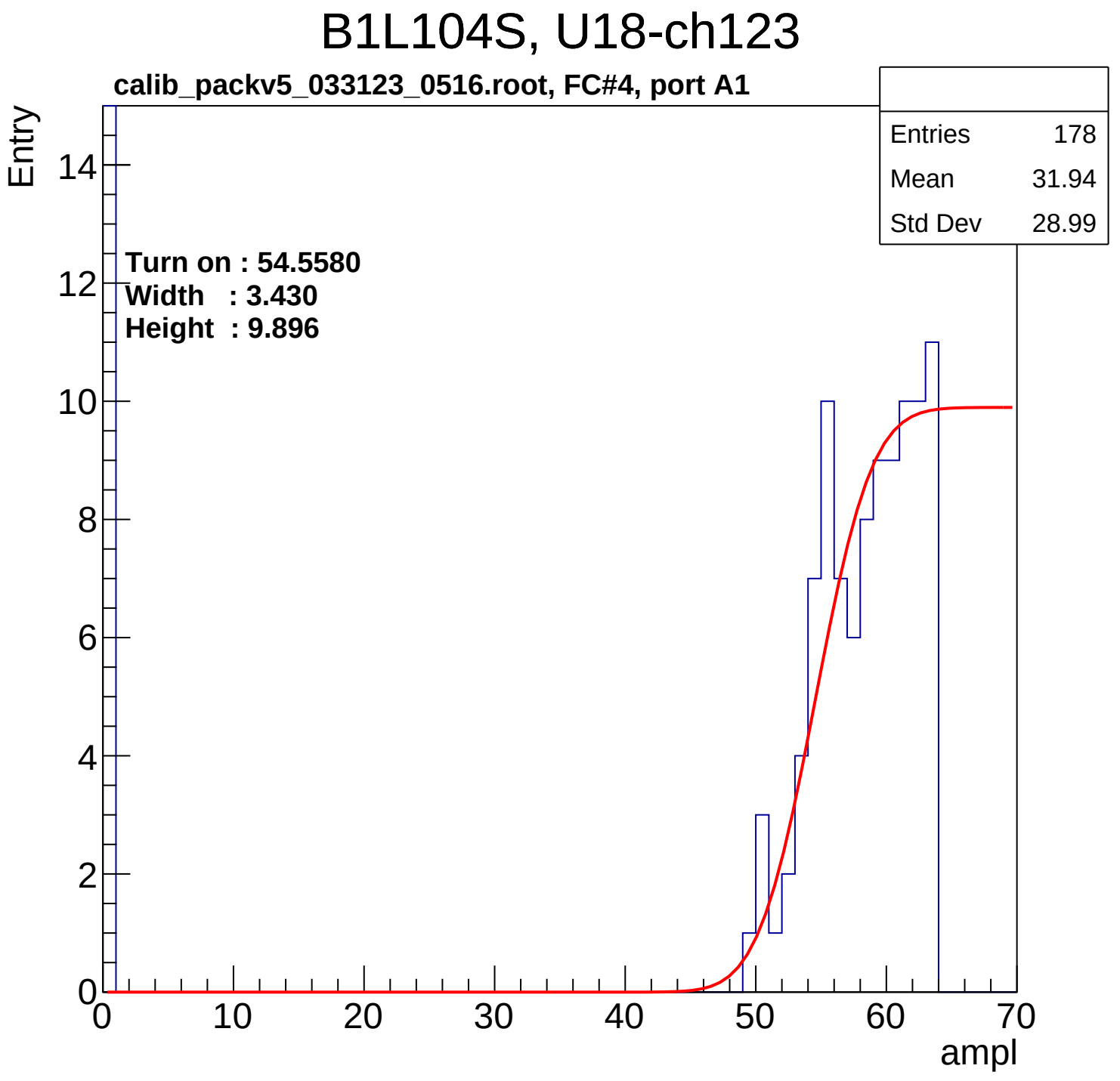

B1L104S, U18-ch118
calib_packv5_033123_0516.root, FC#4, port A1
Entries 196
Mean 31.65
Std Dev 28.71
Turn on : 52.4836
Width : 3.718
Height : 9.472
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

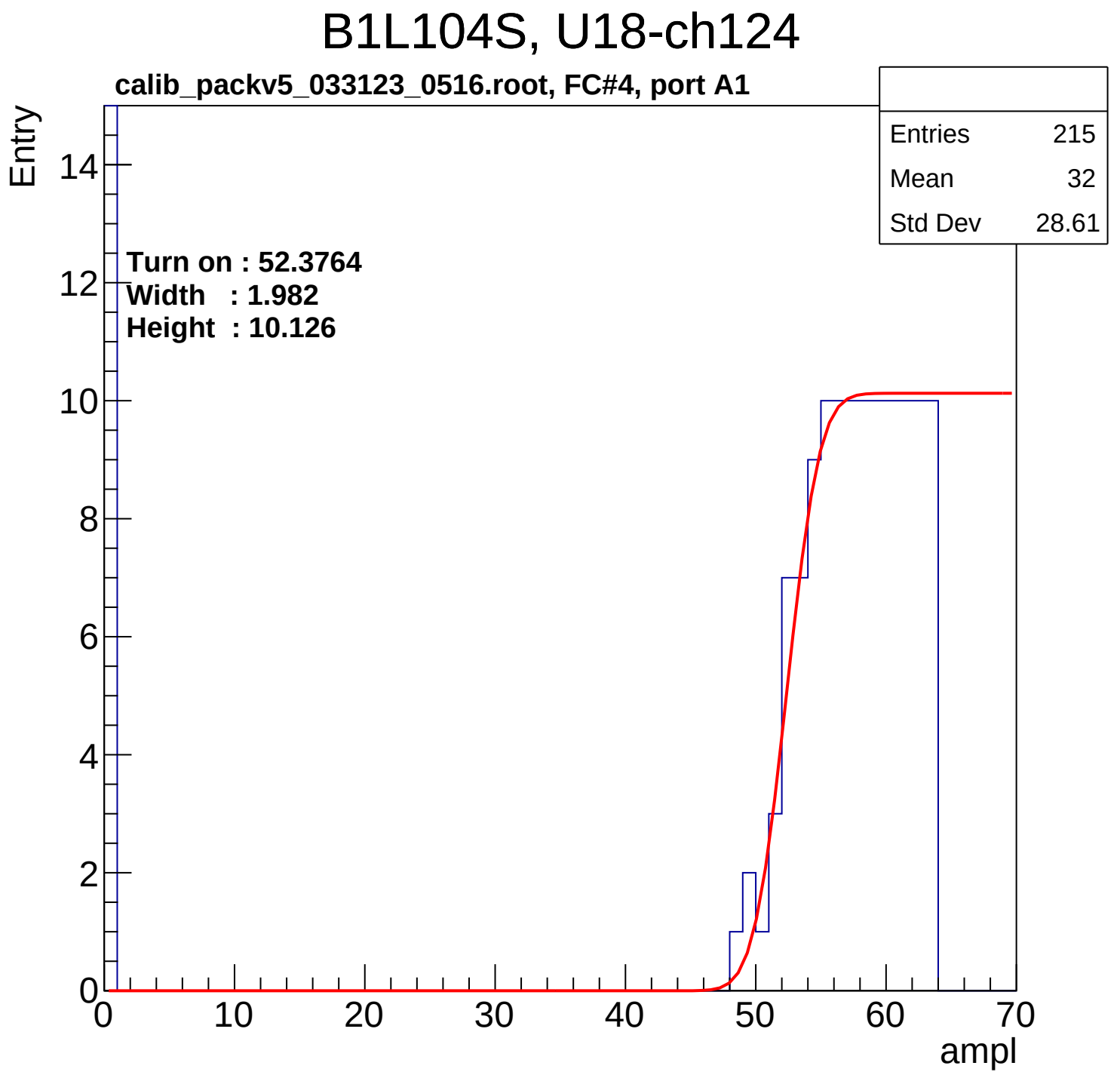

B1L104S, U18-ch119
calib_packv5_033123_0516.root, FC#4, port A1
Entries 175
Mean 29.02
Std Dev 29.29
Turn on : 55.4591
Width : 4.015
Height : 10.000
Entry
ampl
0
10
20
30
40
50
60
70
80
90

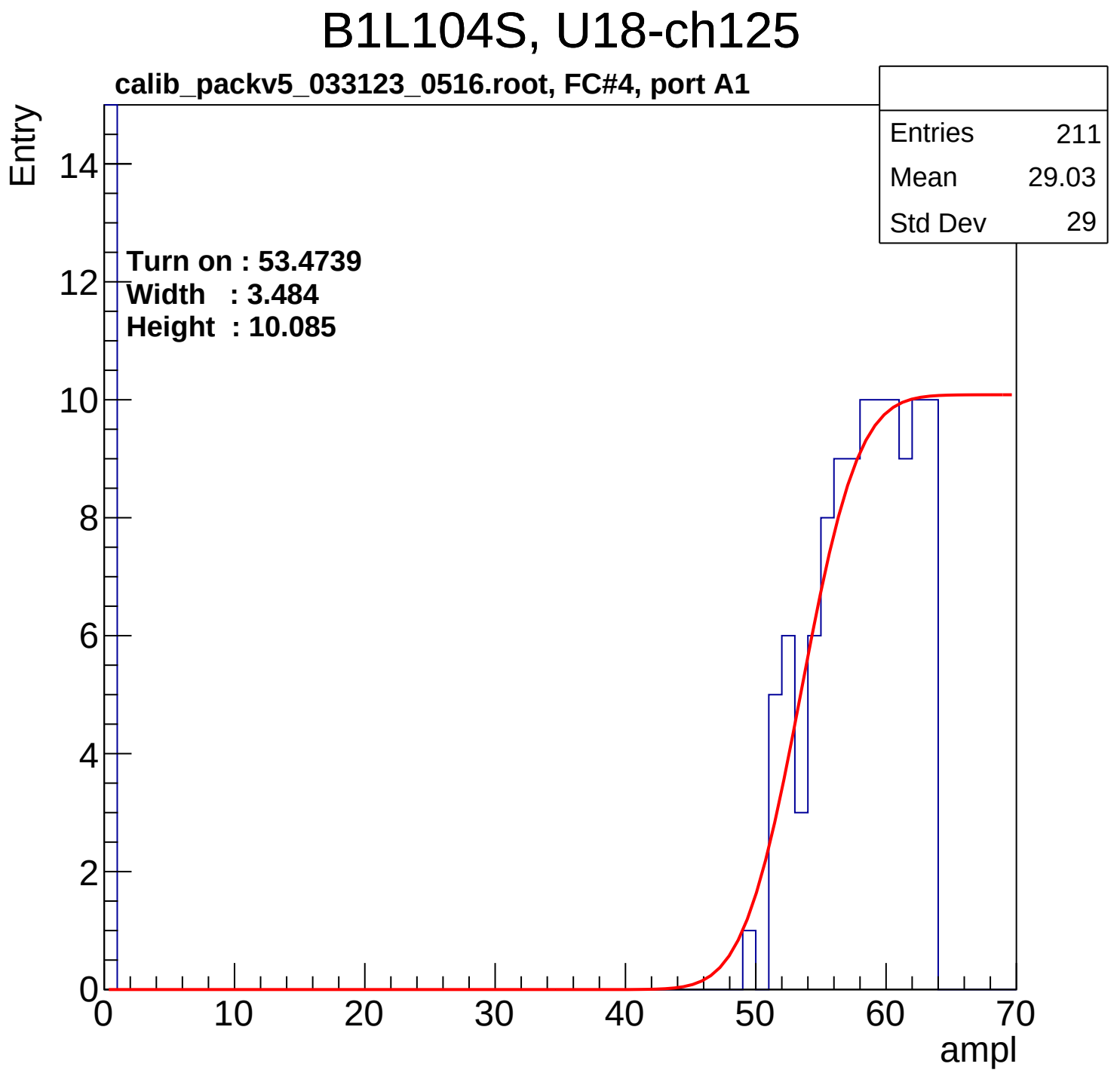

B1L104S, U18-ch120
calib_packv5_033123_0516.root, FC#4, port A1
Entries 198
Mean 27.9
Std Dev 28.74
Turn on : 54.3037
Width : 4.117
Height : 9.633
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

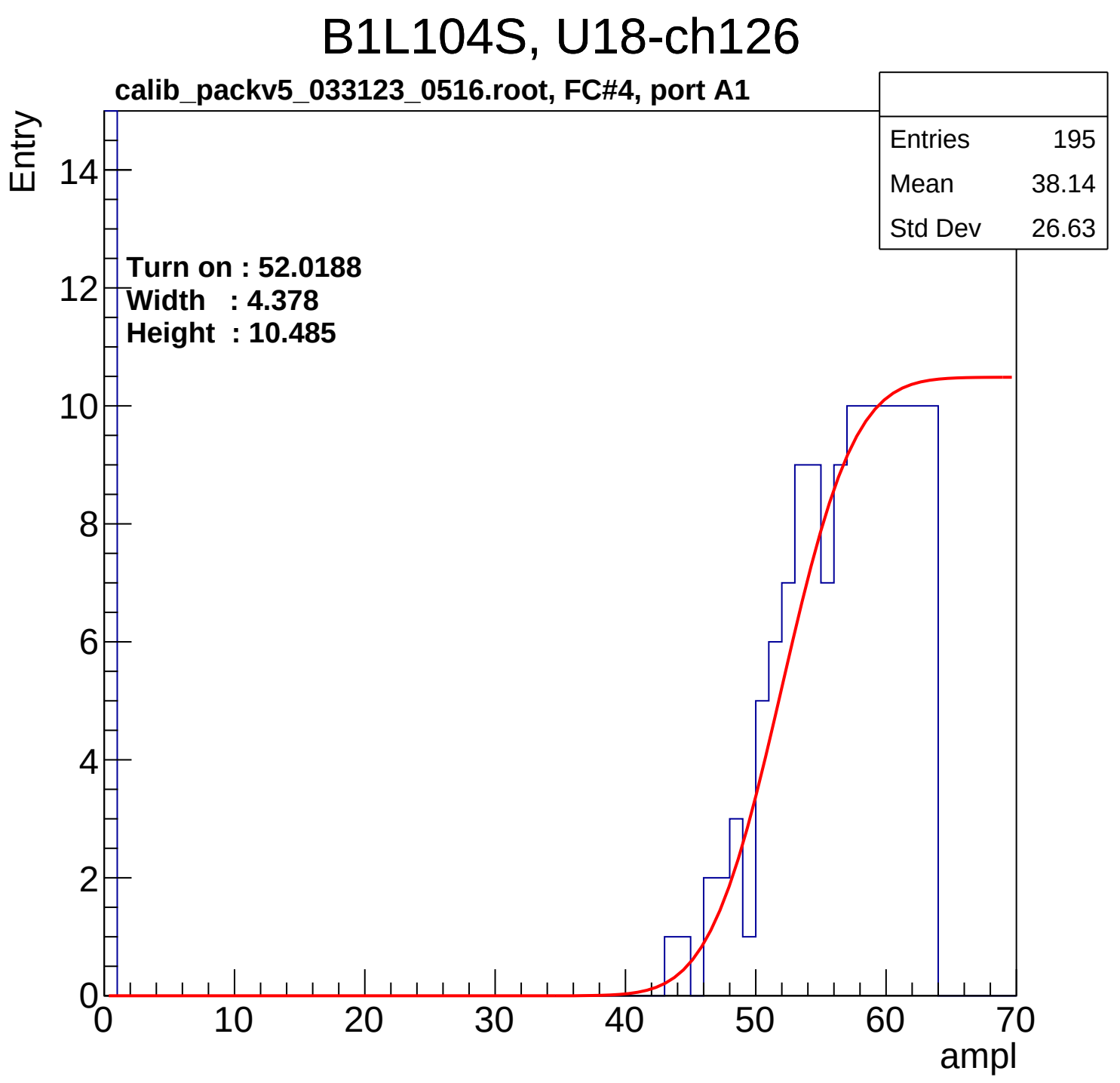

B1L104S, U18-ch121
calib_packv5_033123_0516.root, FC#4, port A1
Entries 181
Mean 36.63
Std Dev 27.62
Turn on : 52.7287
Width : 3.826
Height : 10.151
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

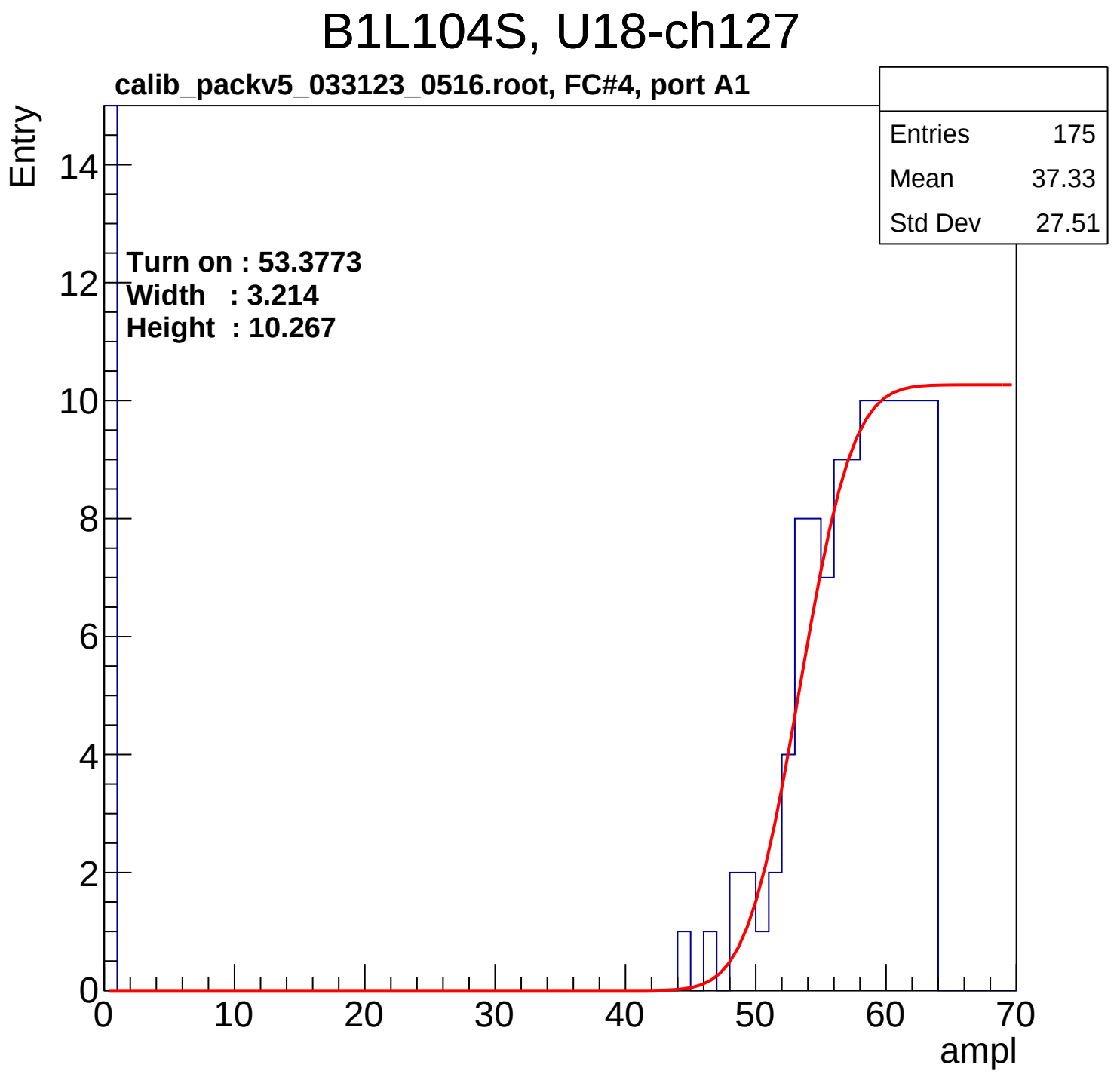

B1L104S, U18-ch122
calib_packv5_033123_0516.root, FC#4, port A1
Entries 185
Mean 29.24
Std Dev 29.2
Turn on : 55.8884
Width : 4.548
Height : 10.333
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

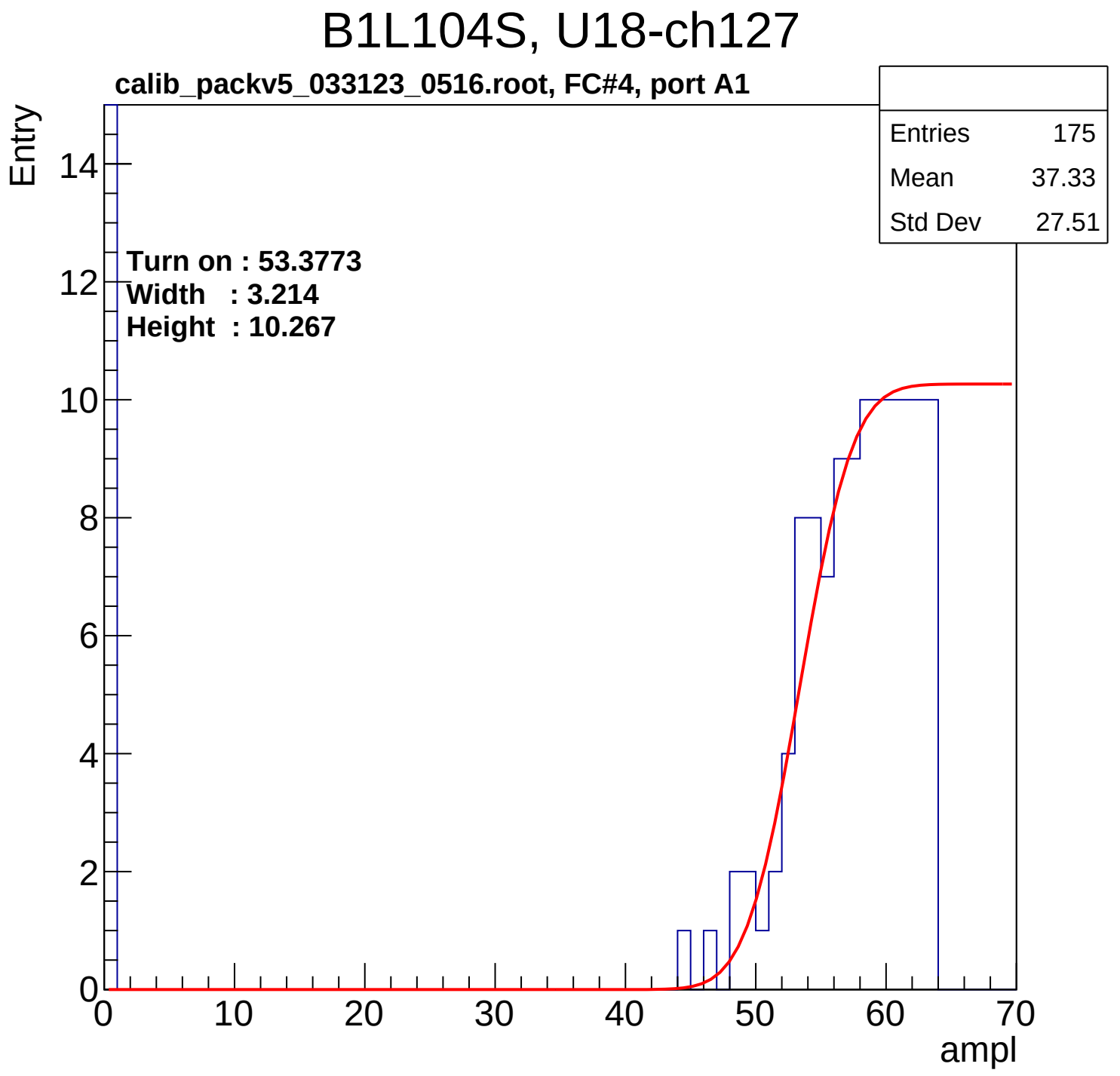

B1L104S, U18-ch123
calib_packv5_033123_0516.root, FC#4, port A1
Entries 178
Mean 31.94
Std Dev 28.99
Turn on : 54.5580
Width : 3.430
Height : 9.896
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L104S, U18-ch124
calib_packv5_033123_0516.root, FC#4, port A1
Entries 215
Mean 32
Std Dev 28.61
Turn on : 52.3764
Width : 1.982
Height : 10.126
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L104S, U18-ch125
calib_packv5_033123_0516.root, FC#4, port A1
Entries 211
Mean 29.03
Std Dev 29
Turn on : 53.4739
Width : 3.484
Height : 10.085
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L104S, U18-ch126
calib_packv5_033123_0516.root, FC#4, port A1
Entries 195
Mean 38.14
Std Dev 26.63
Turn on : 52.0188
Width : 4.378
Height : 10.485
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L104S, U18-ch127
calib_packv5_033123_0516.root, FC#4, port A1
Entries 175
Mean 37.33
Std Dev 27.51
Turn on : 53.3773
Width : 3.214
Height : 10.267
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L104S, U18-ch127
calib_packv5_033123_0516.root, FC#4, port A1
Entries 175
Mean 37.33
Std Dev 27.51
Turn on : 53.3773
Width : 3.214
Height : 10.267
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70