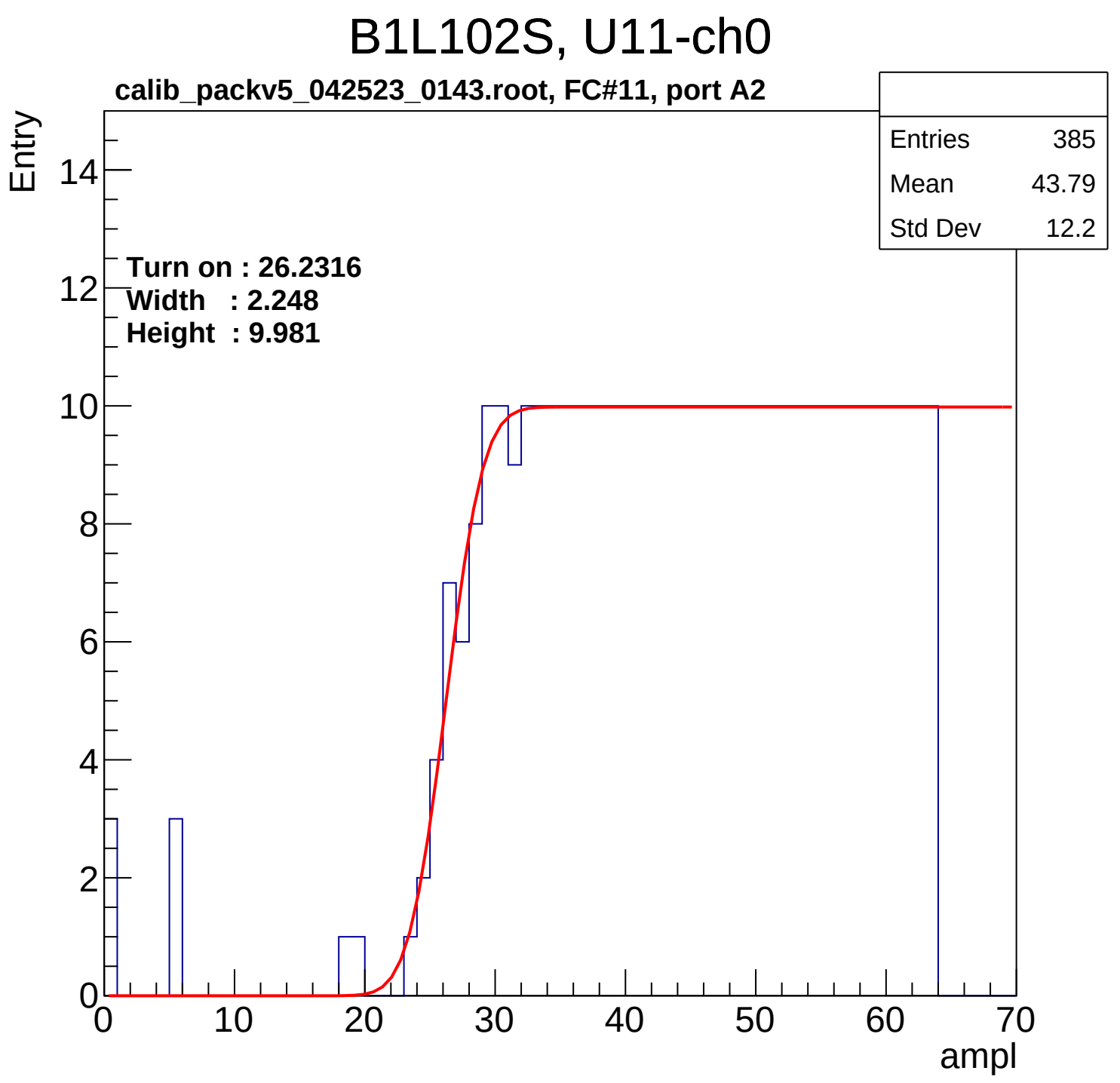
B1L102S, U11-ch0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 43.79
Std Dev 12.2
Turn on : 26.2316
Width : 2.248
Height : 9.981
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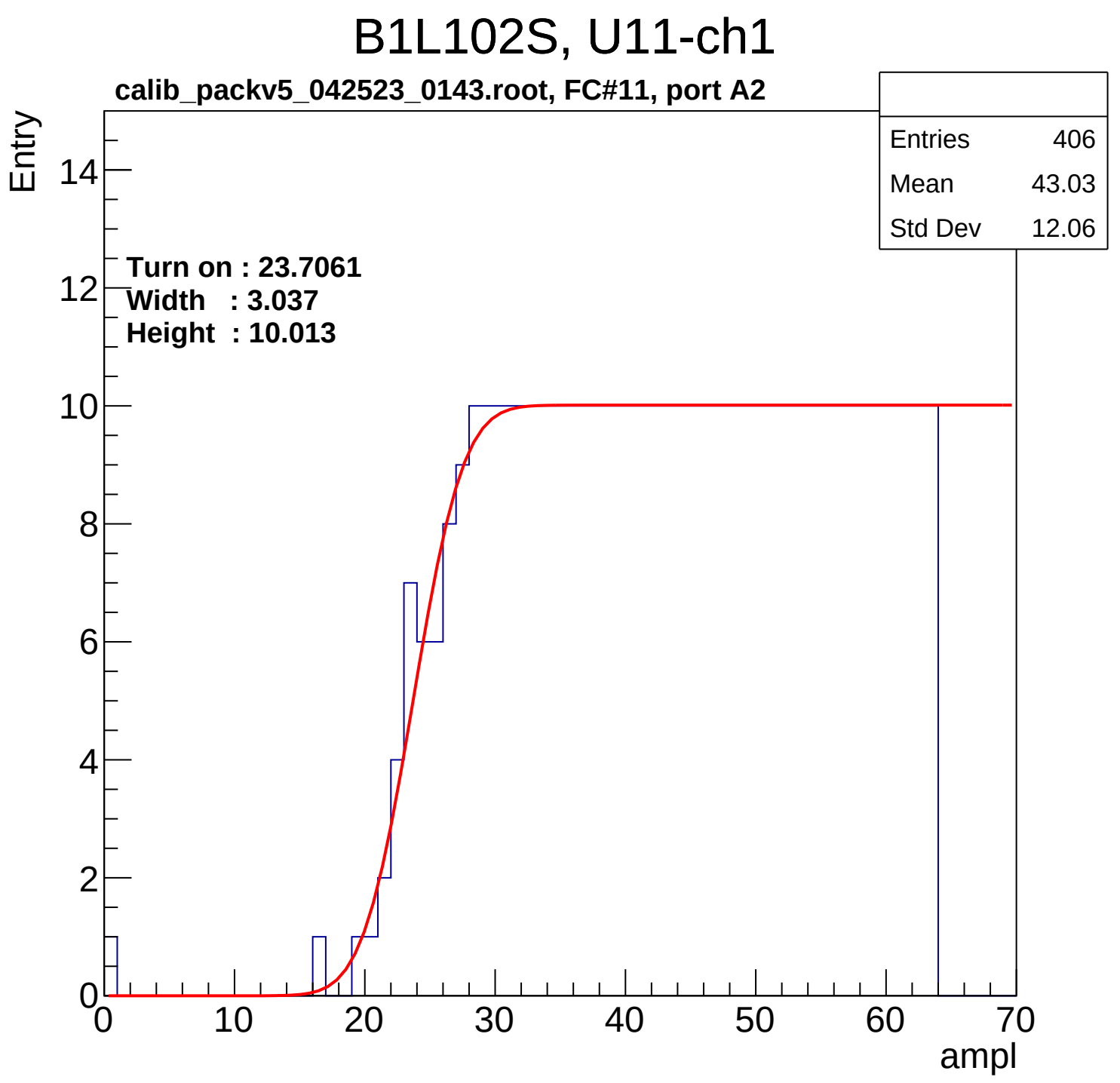
B1L102S, U11-ch1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 406
Mean 43.03
Std Dev 12.06
Turn on : 23.7061
Width : 3.037
Height : 10.013
Entry
ampl
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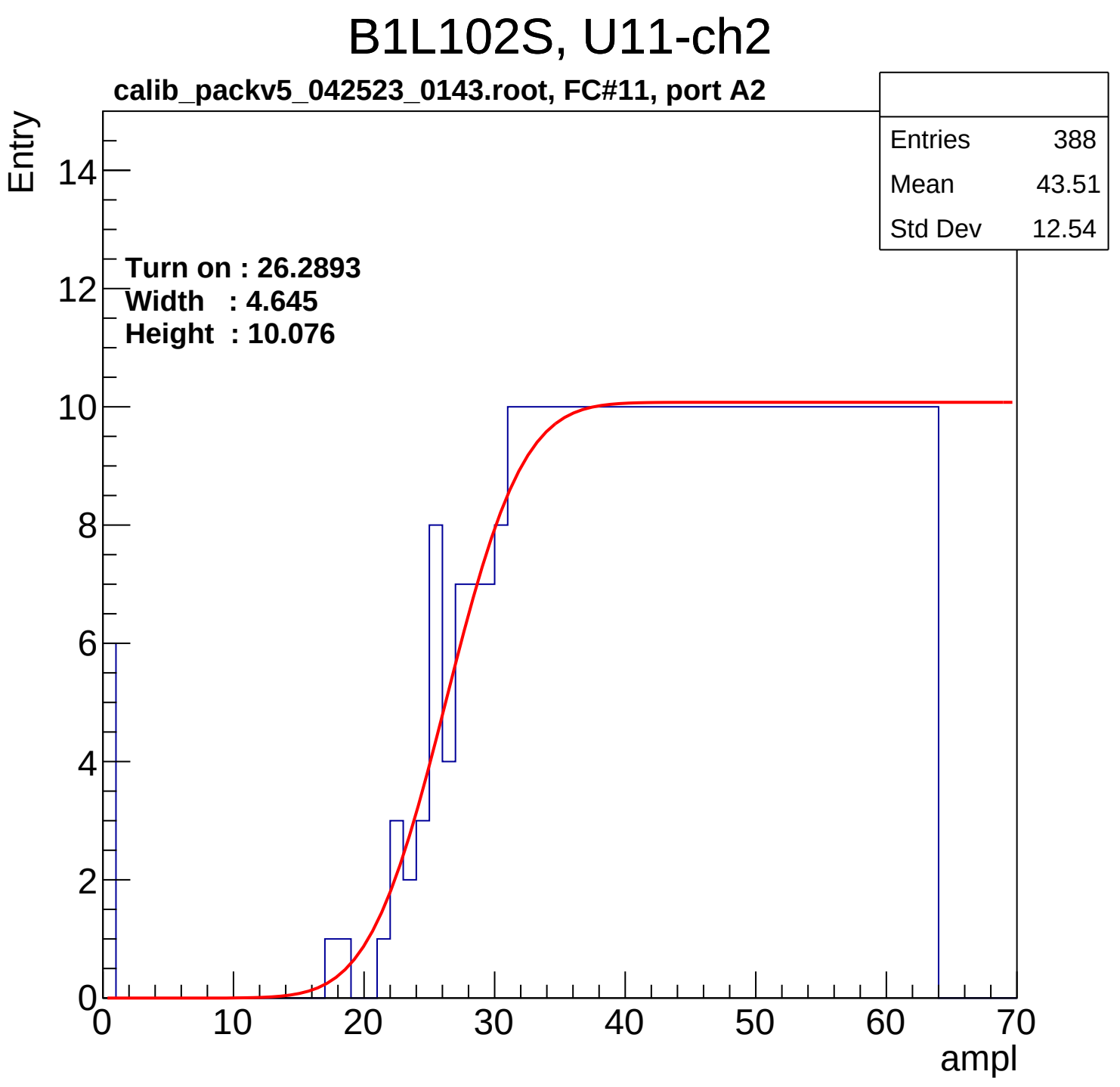
B1L102S, U11-ch2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 388
Mean 43.51
Std Dev 12.54
Turn on : 26.2893
Width : 4.645
Height : 10.076
Entry
ampl
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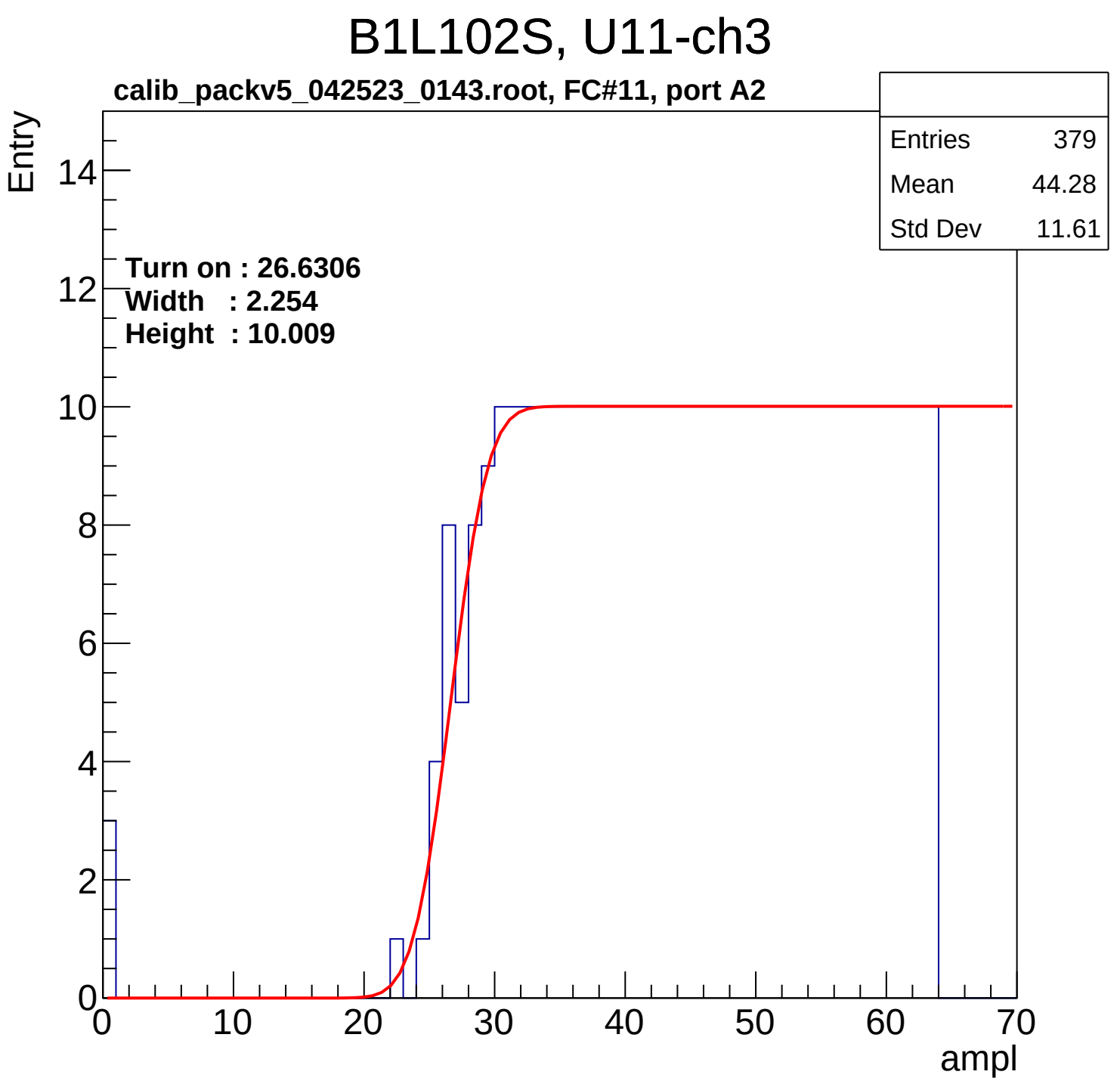
B1L102S, U11-ch3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 379
Mean 44.28
Std Dev 11.61
Turn on : 26.6306
Width : 2.254
Height : 10.009
Entry
ampl
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2
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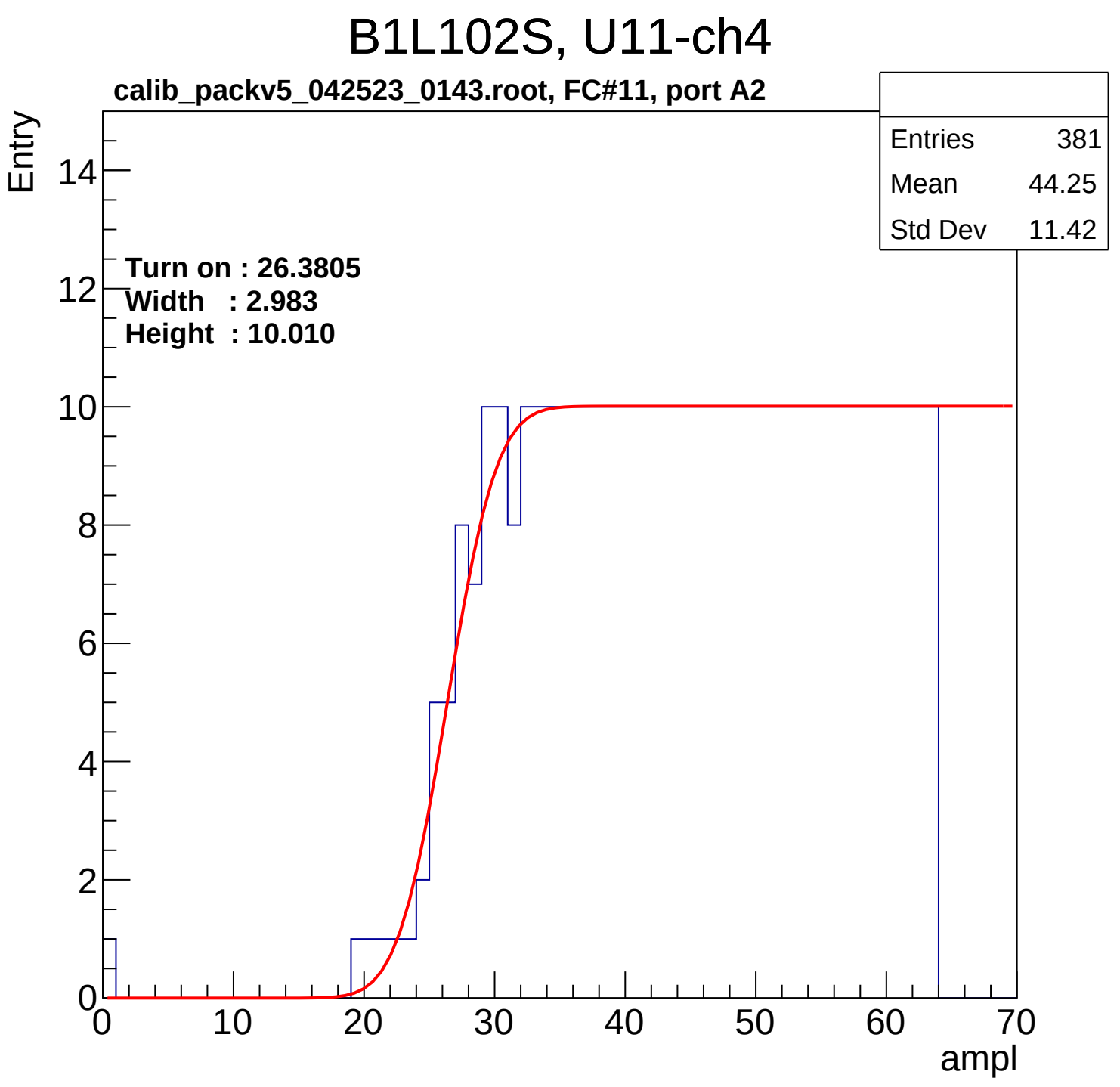
B1L102S, U11-ch4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 381
Mean 44.25
Std Dev 11.42
Turn on : 26.3805
Width : 2.983
Height : 10.010
Entry
ampl
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2
4
6
8
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0
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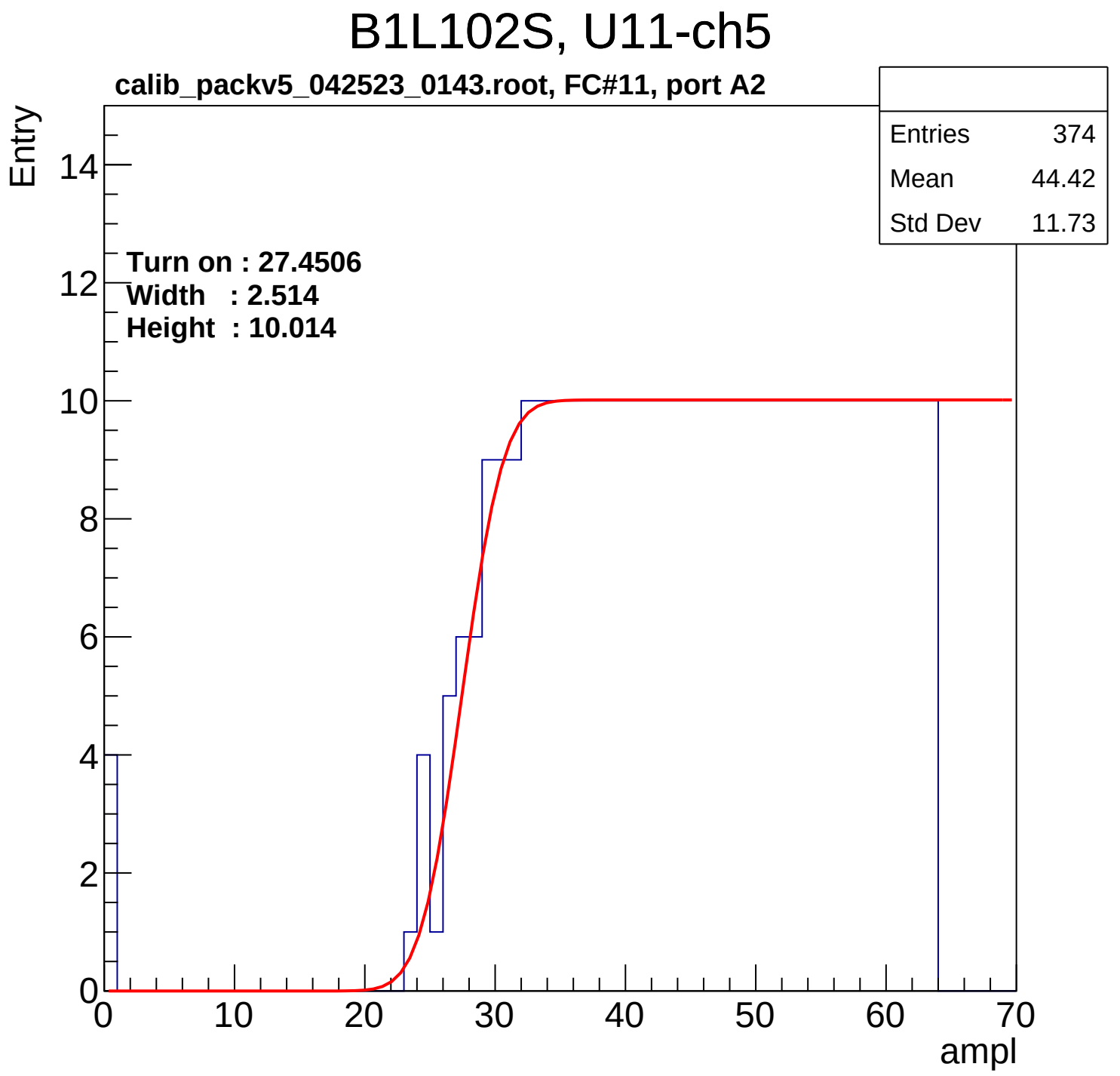
B1L102S, U11-ch5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 374
Mean 44.42
Std Dev 11.73
Turn on : 27.4506
Width : 2.514
Height : 10.014
Entry
ampl
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2
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6
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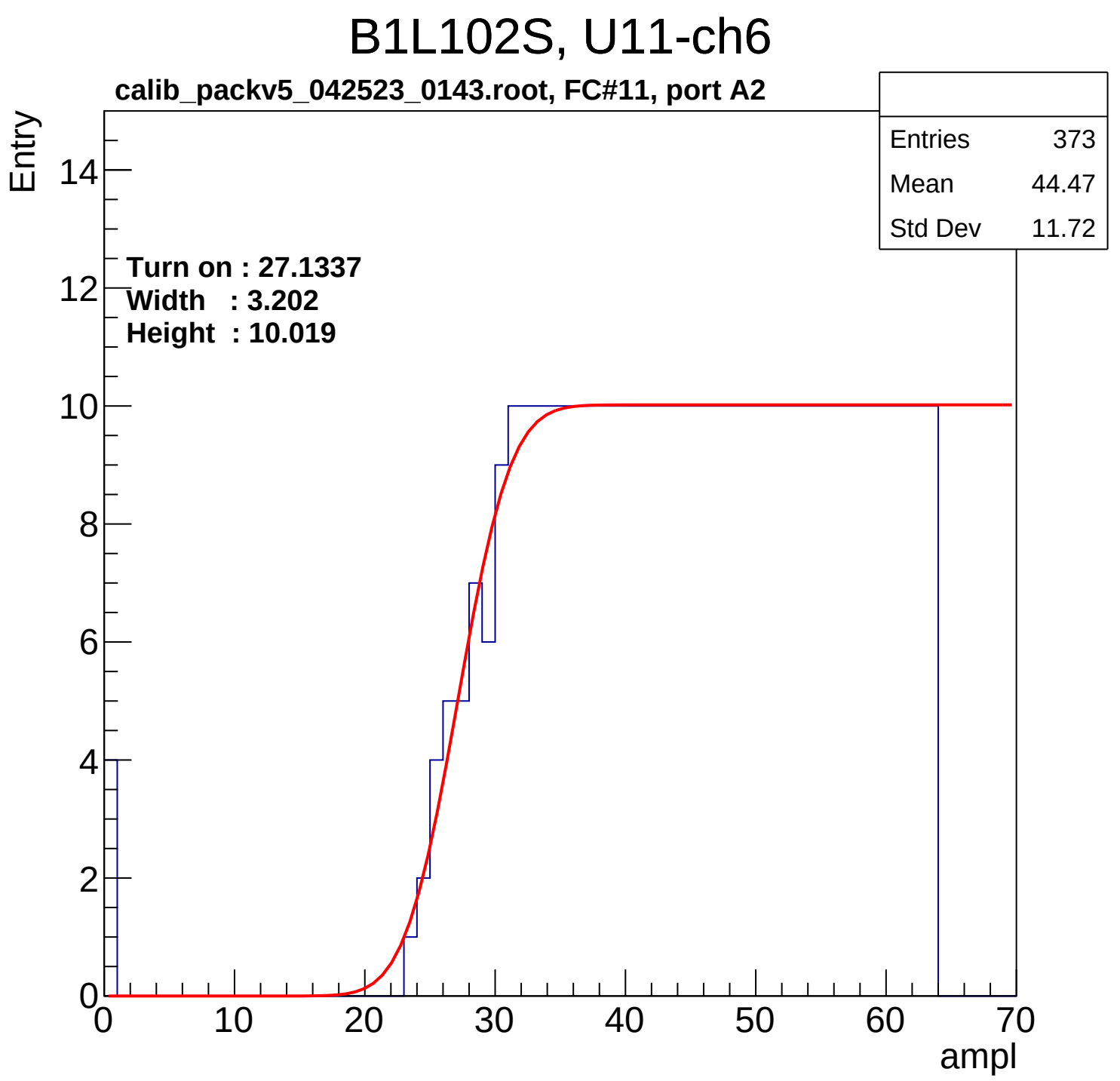
B1L102S, U11-ch6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 373
Mean 44.47
Std Dev 11.72
Turn on : 27.1337
Width : 3.202
Height : 10.019
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ampl
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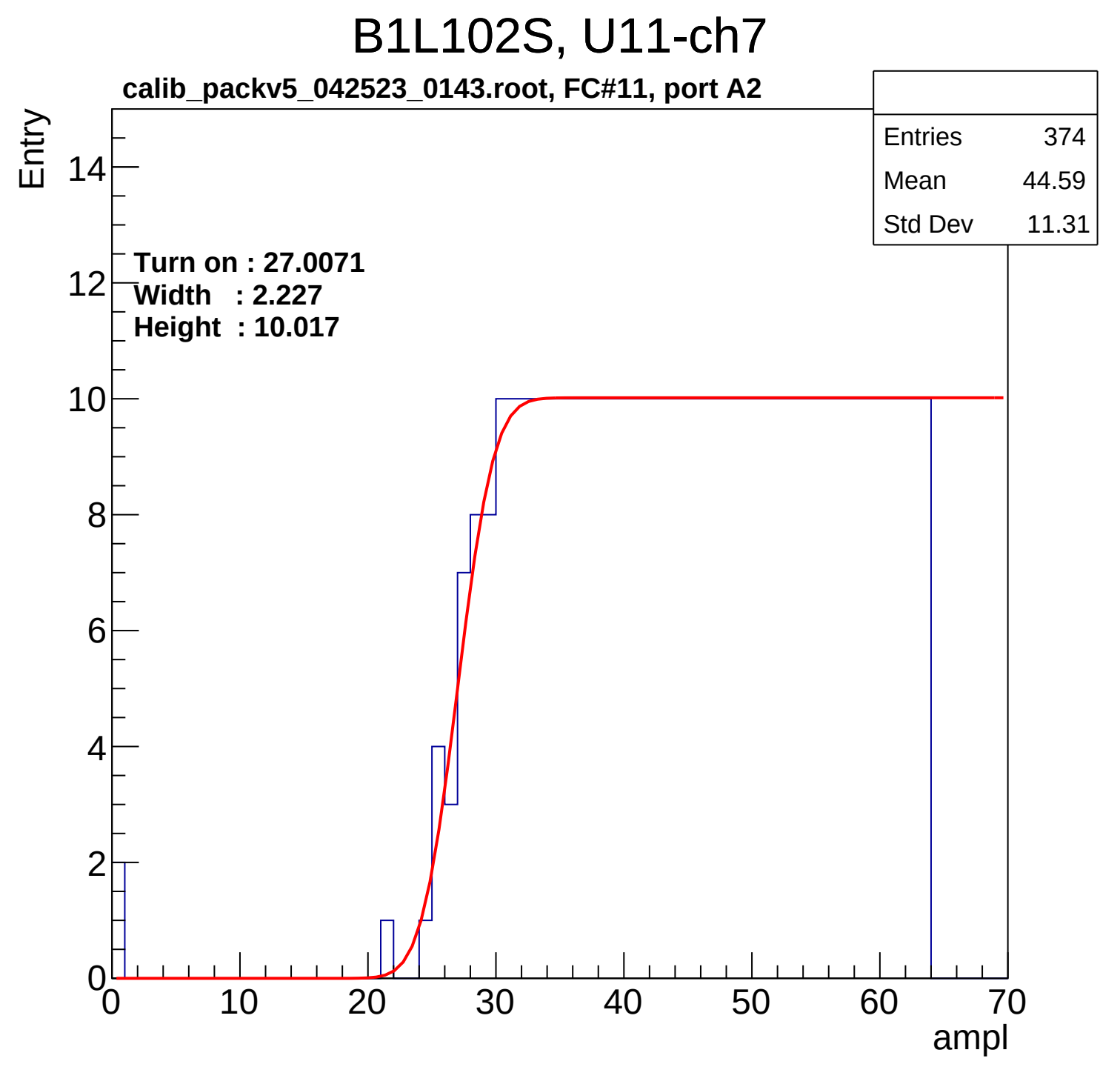
B1L102S, U11-ch7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 374
Mean 44.59
Std Dev 11.31
Turn on : 27.0071
Width : 2.227
Height : 10.017
Entry
ampl
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6
8
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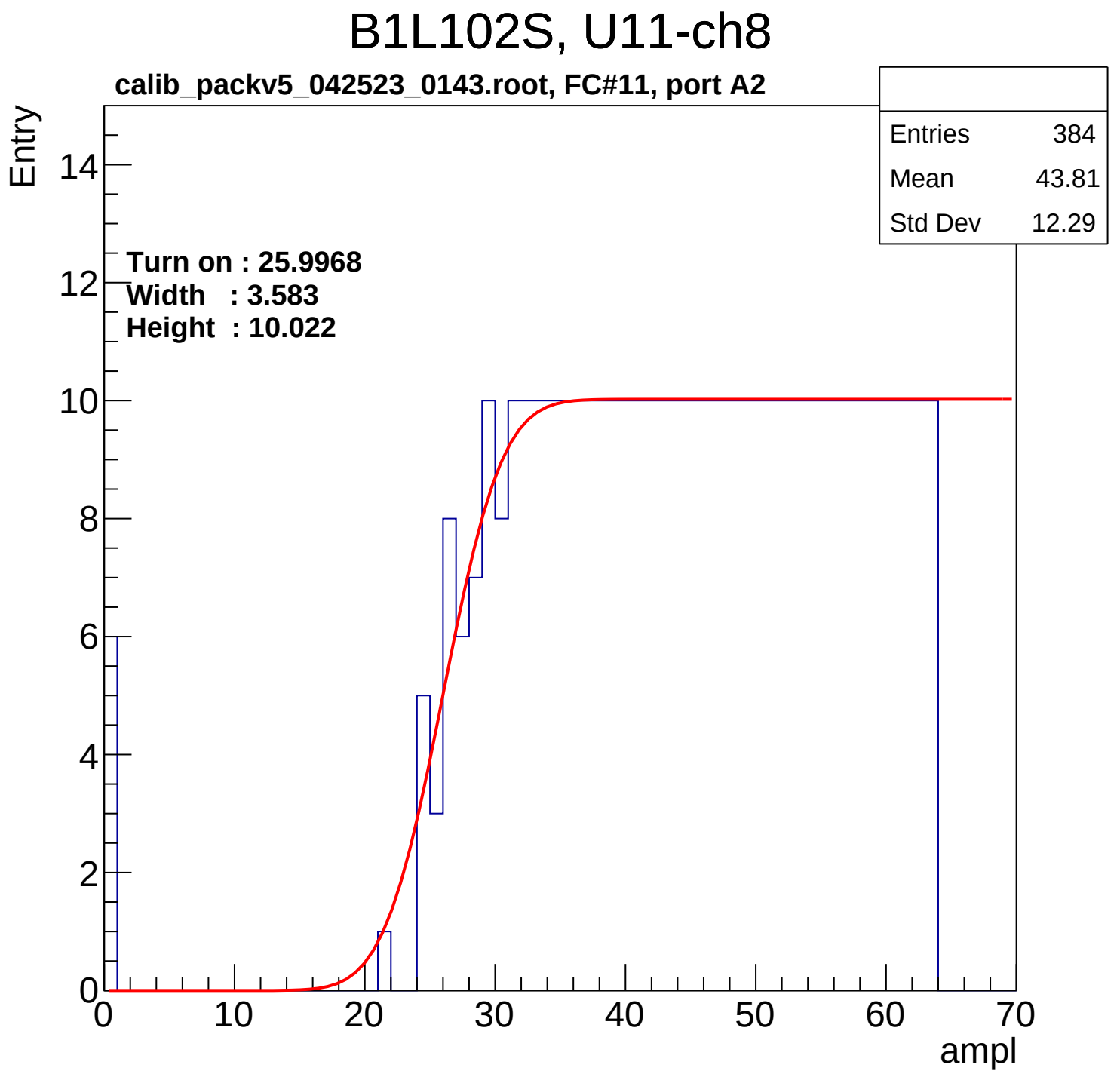
B1L102S, U11-ch8
calib_packv5_042523_0143.root, FC#11, port A2
Entries 384
Mean 43.81
Std Dev 12.29
Turn on : 25.9968
Width : 3.583
Height : 10.022
Entry
ampl
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2
4
6
8
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60
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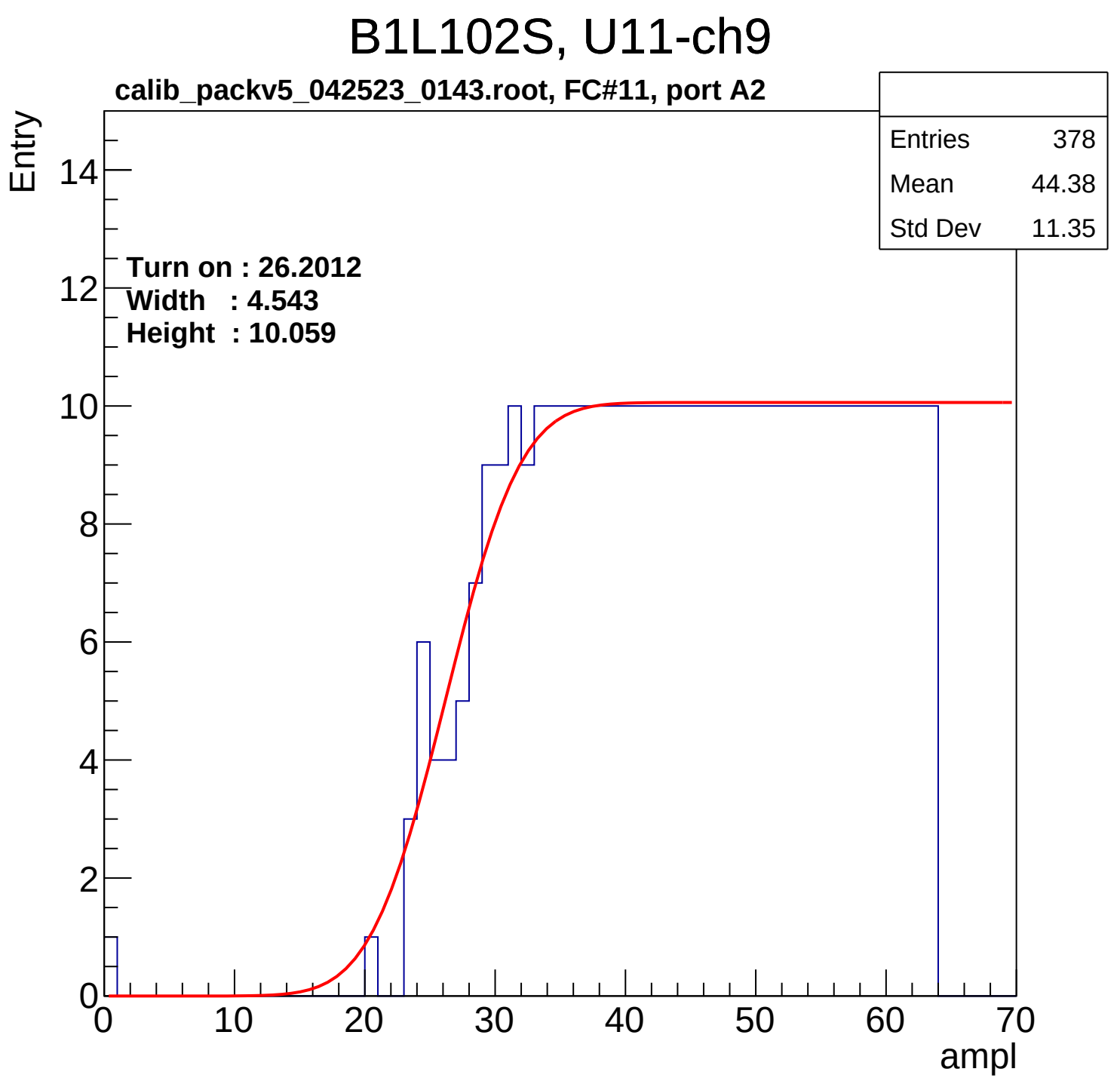
B1L102S, U11-ch9
calib_packv5_042523_0143.root, FC#11, port A2
Entries 378
Mean 44.38
Std Dev 11.35
Turn on : 26.2012
Width : 4.543
Height : 10.059
Entry
ampl
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2
4
6
8
10
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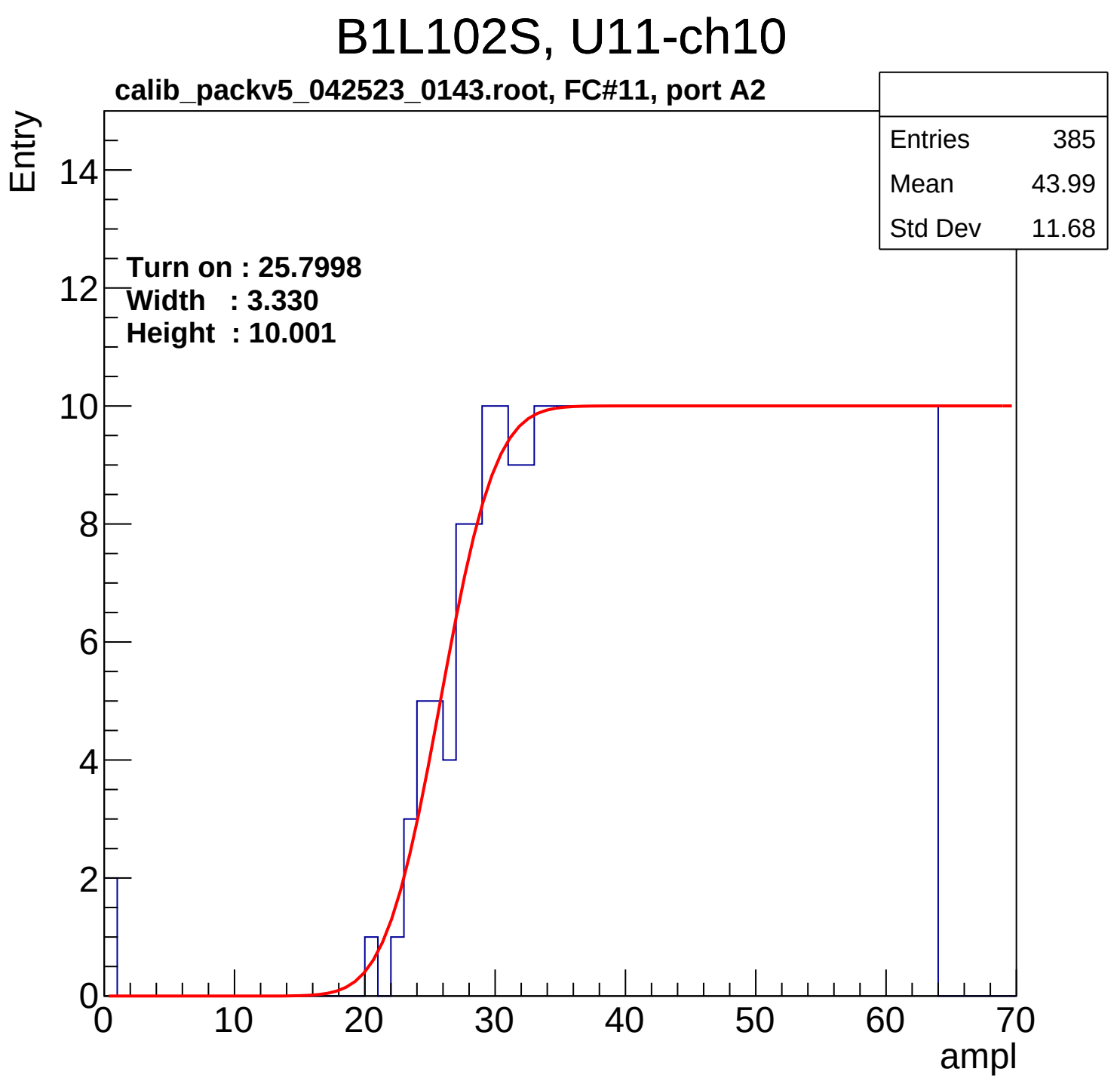
B1L102S, U11-ch10
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 43.99
Std Dev 11.68
Turn on : 25.7998
Width : 3.330
Height : 10.001
Entry
ampl
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6
8
10
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0
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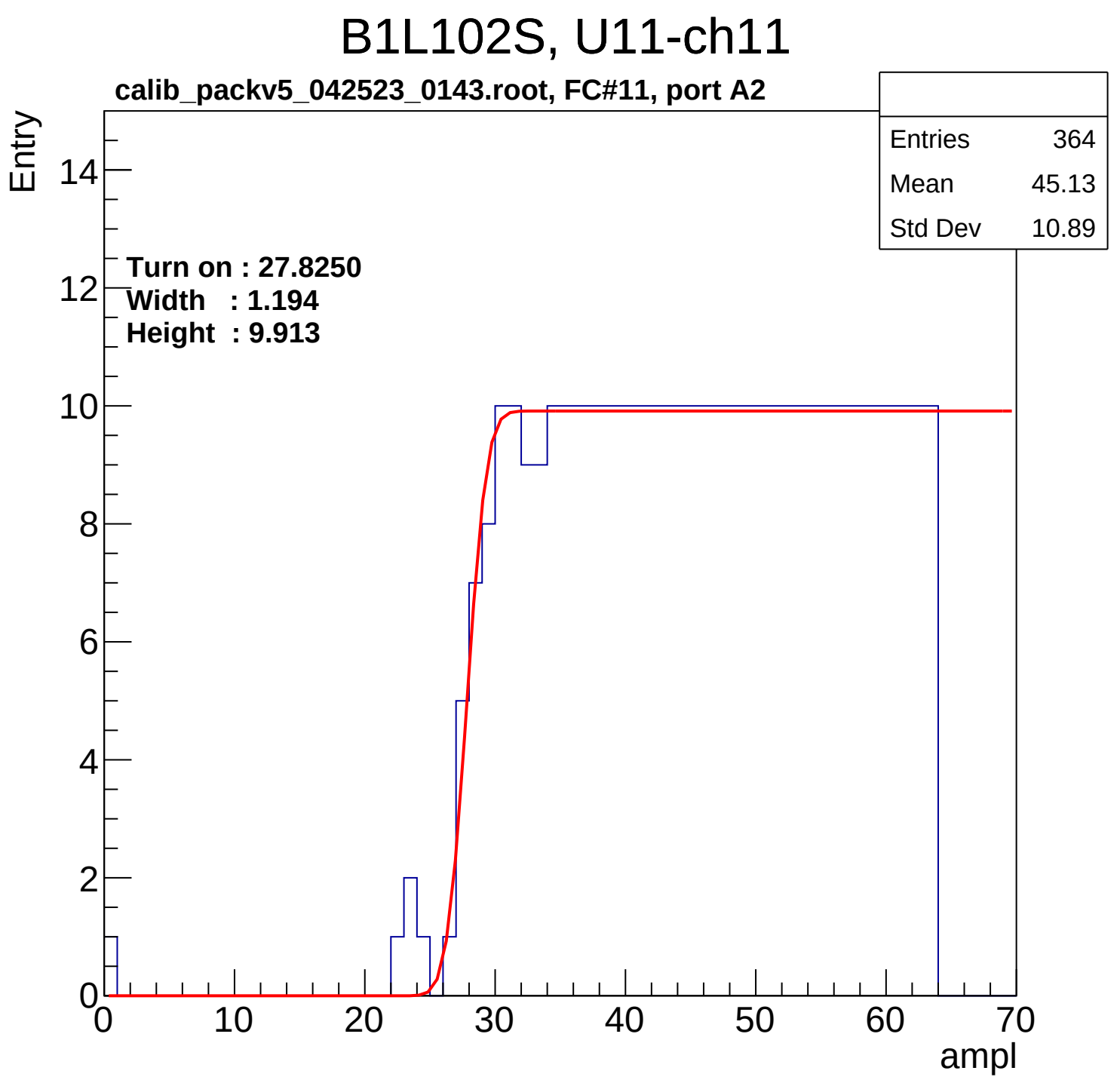
B1L102S, U11-ch11
calib_packv5_042523_0143.root, FC#11, port A2
Entries 364
Mean 45.13
Std Dev 10.89
Turn on : 27.8250
Width : 1.194
Height : 9.913
Entry
ampl
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6
8
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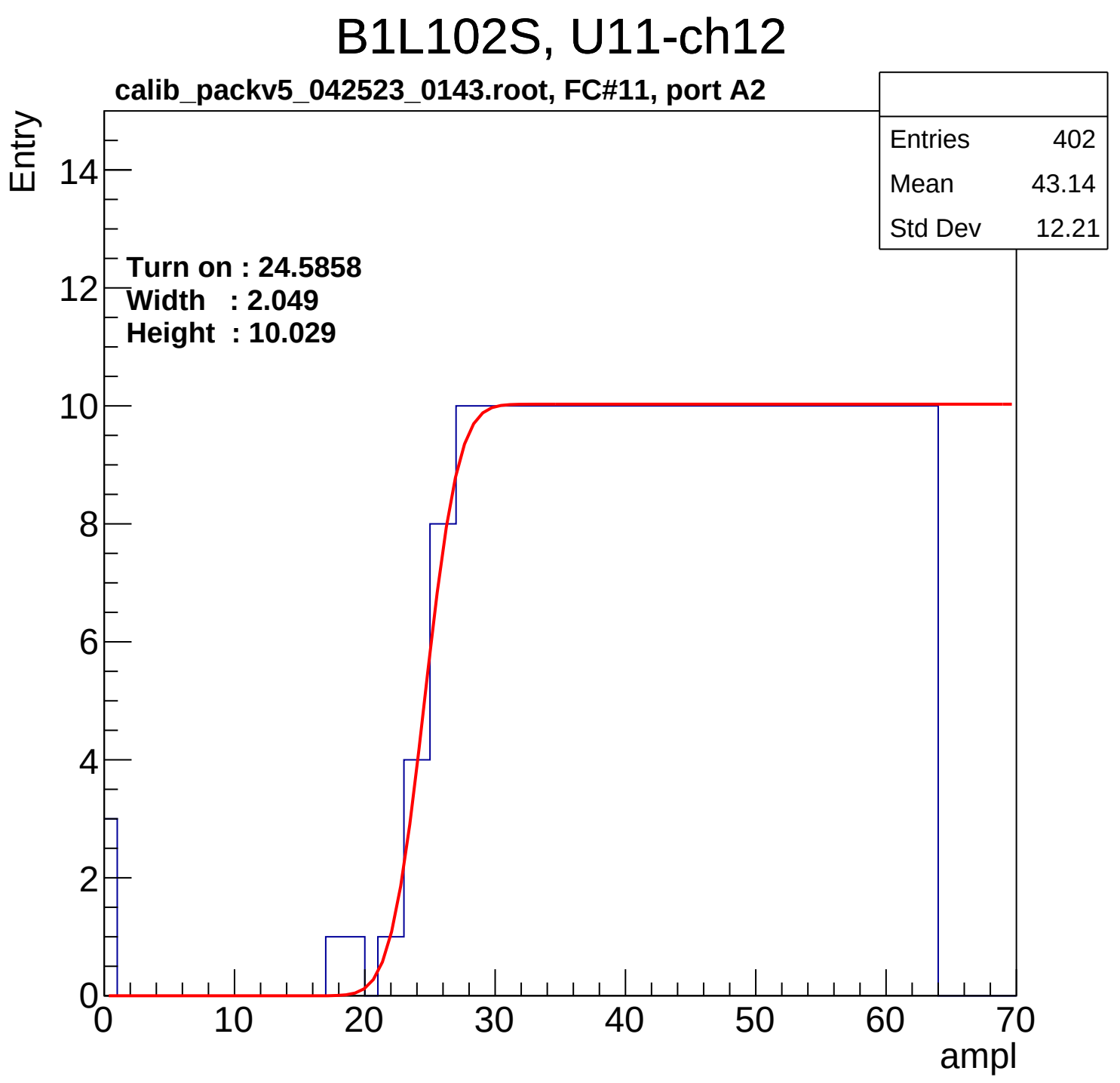
B1L102S, U11-ch12
calib_packv5_042523_0143.root, FC#11, port A2
Entries 402
Mean 43.14
Std Dev 12.21
Turn on : 24.5858
Width : 2.049
Height : 10.029
Entry
ampl
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2
4
6
8
10
12
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0
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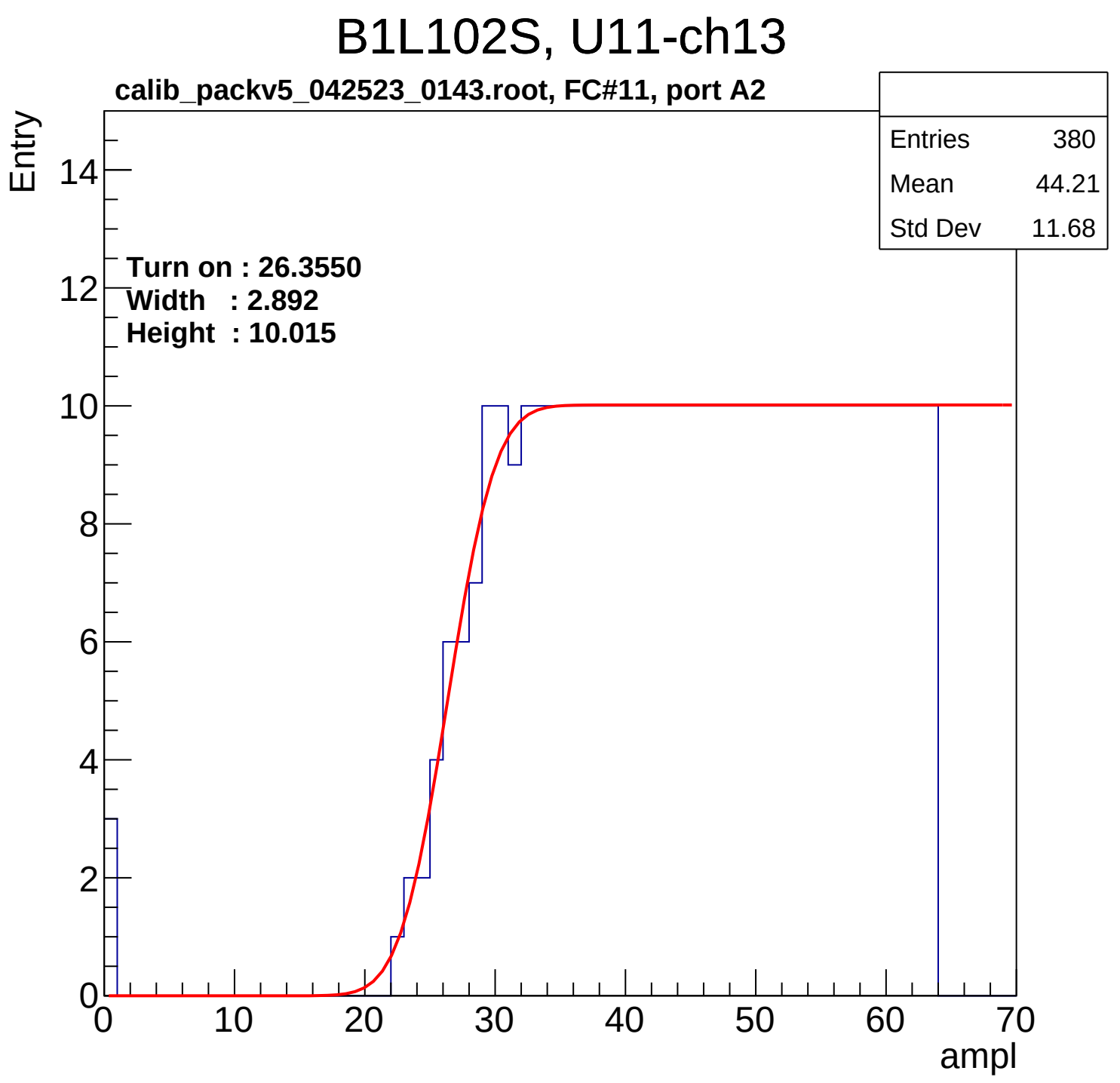
B1L102S, U11-ch13
calib_packv5_042523_0143.root, FC#11, port A2
Entries 380
Mean 44.21
Std Dev 11.68
Turn on : 26.3550
Width : 2.892
Height : 10.015
Entry
ampl
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6
8
10
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0
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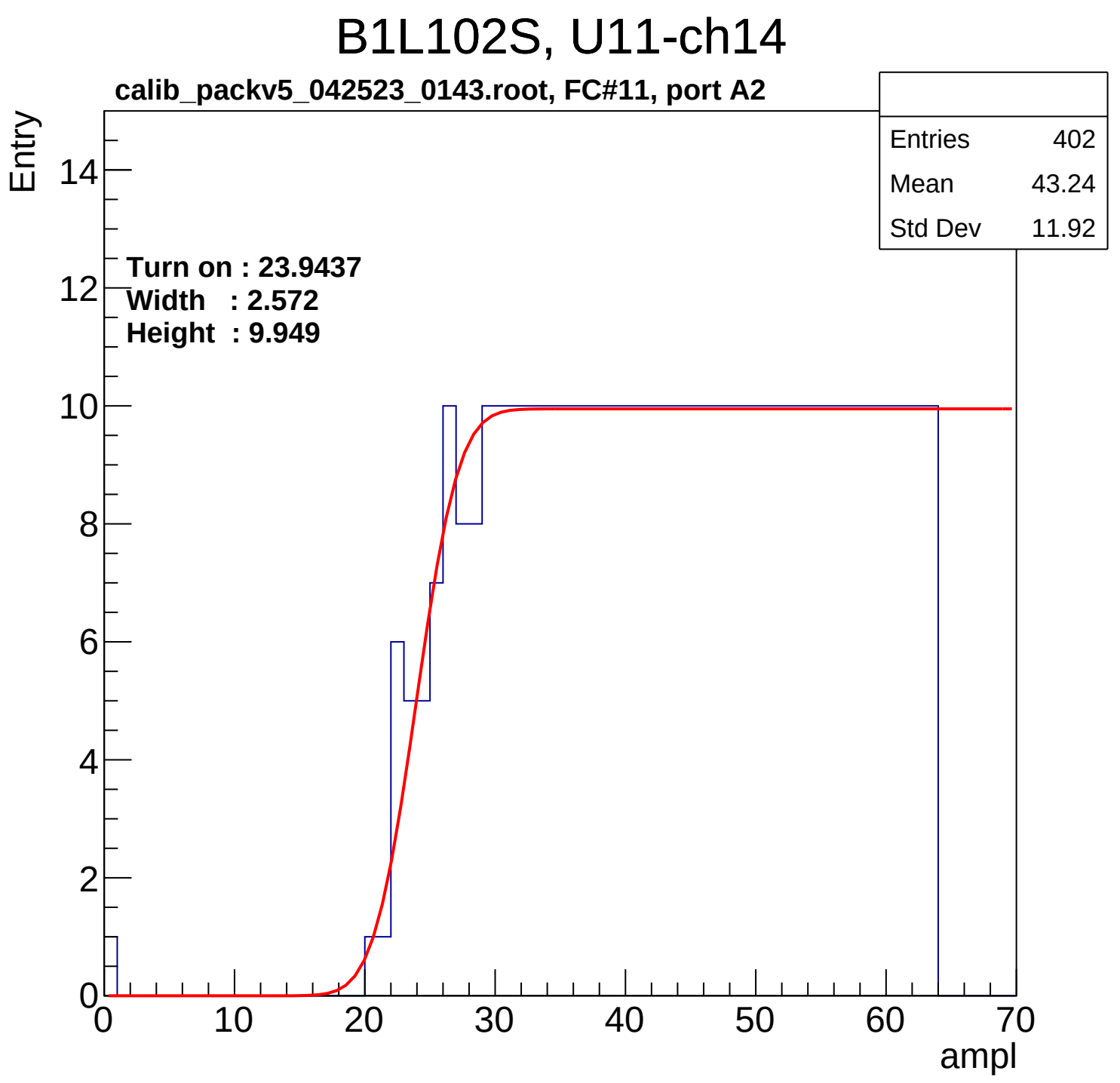
B1L102S, U11-ch14
calib_packv5_042523_0143.root, FC#11, port A2
Entries 402
Mean 43.24
Std Dev 11.92
Turn on : 23.9437
Width : 2.572
Height : 9.949
Entry
ampl
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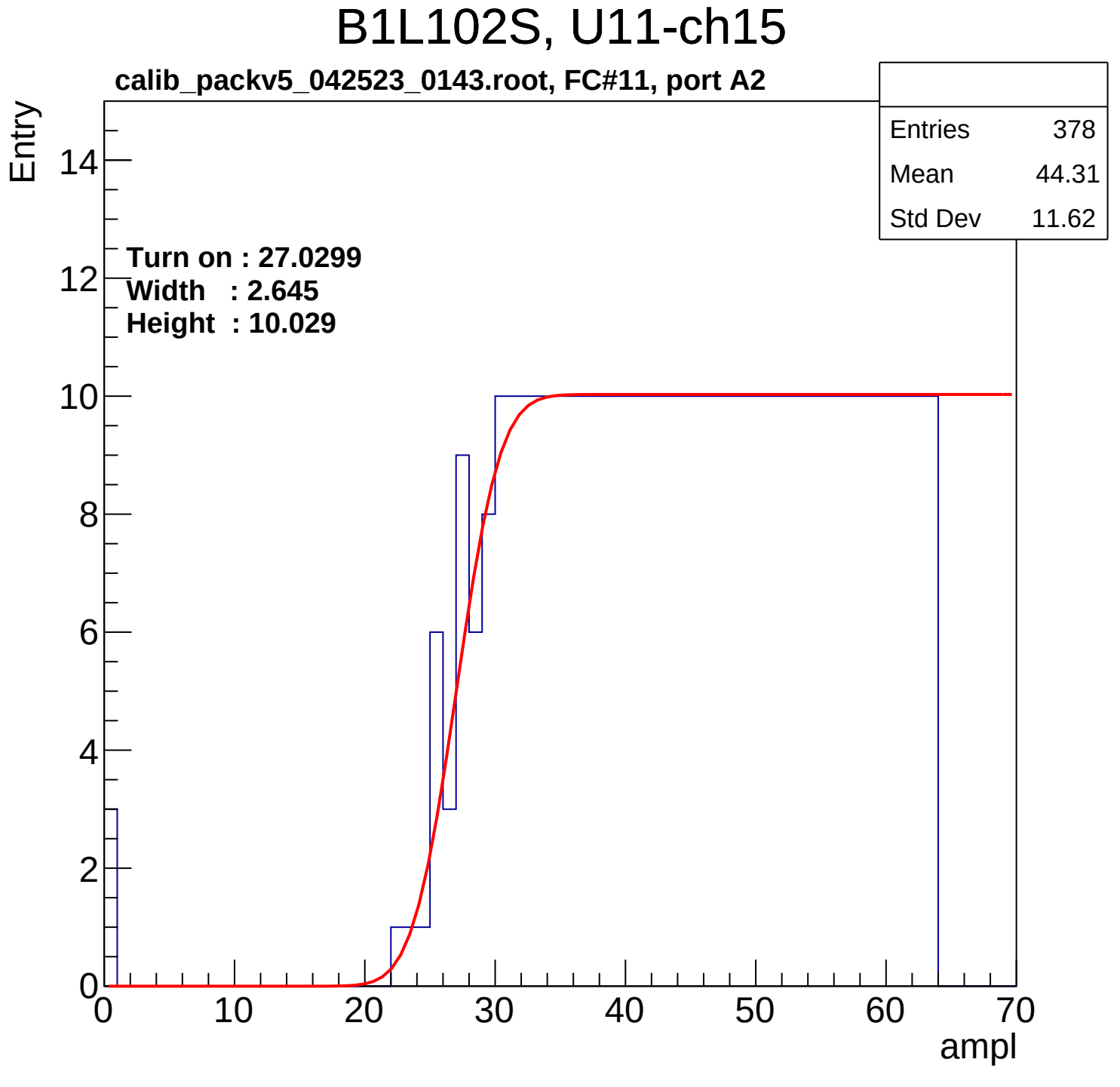
B1L102S, U11-ch15
calib_packv5_042523_0143.root, FC#11, port A2
Entries 378
Mean 44.31
Std Dev 11.62
Turn on : 27.0299
Width : 2.645
Height : 10.029
Entry
ampl
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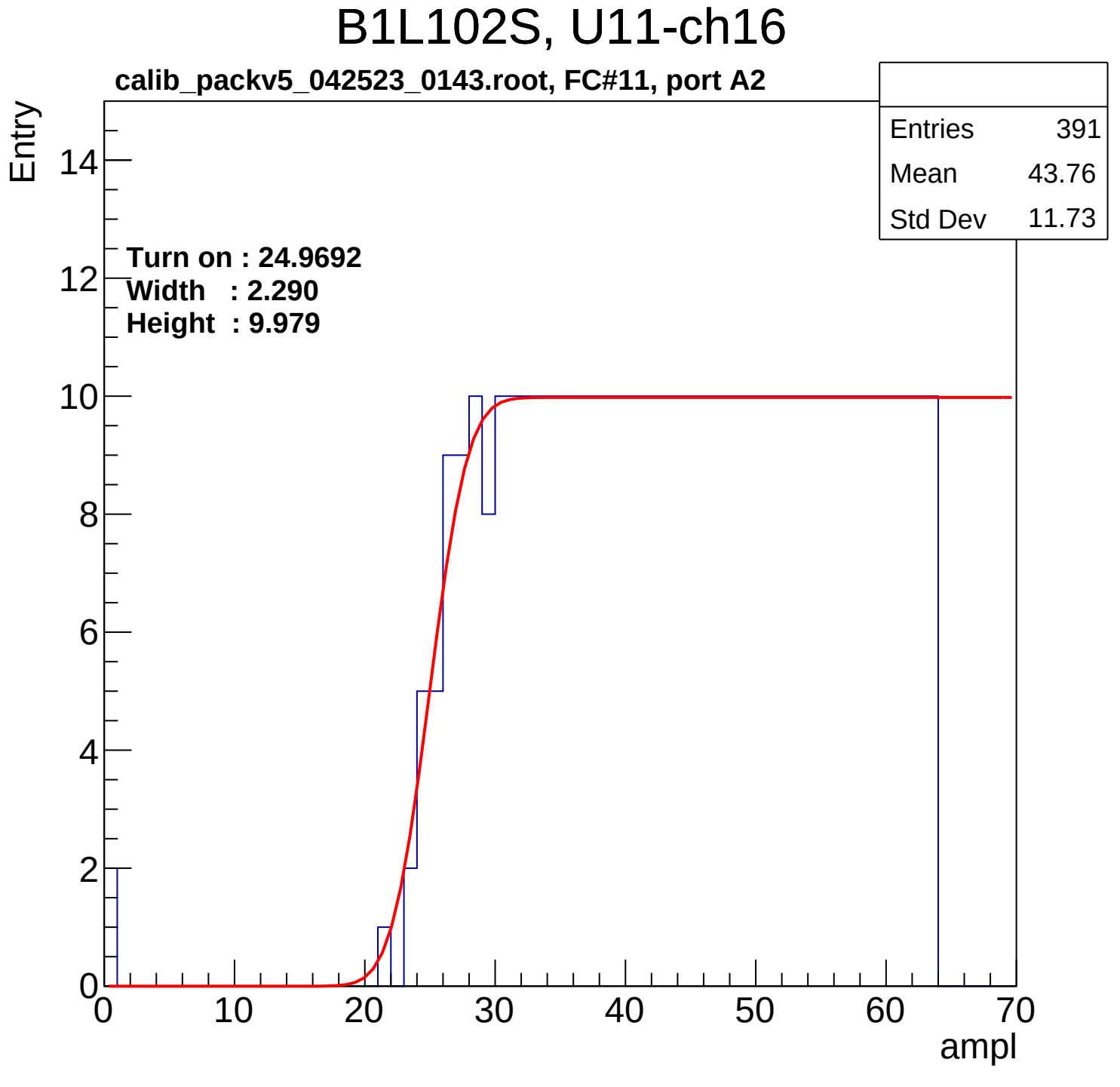
B1L102S, U11-ch16
calib_packv5_042523_0143.root, FC#11, port A2
Entries 391
Mean 43.76
Std Dev 11.73
Turn on : 24.9692
Width : 2.290
Height : 9.979
Entry
ampl
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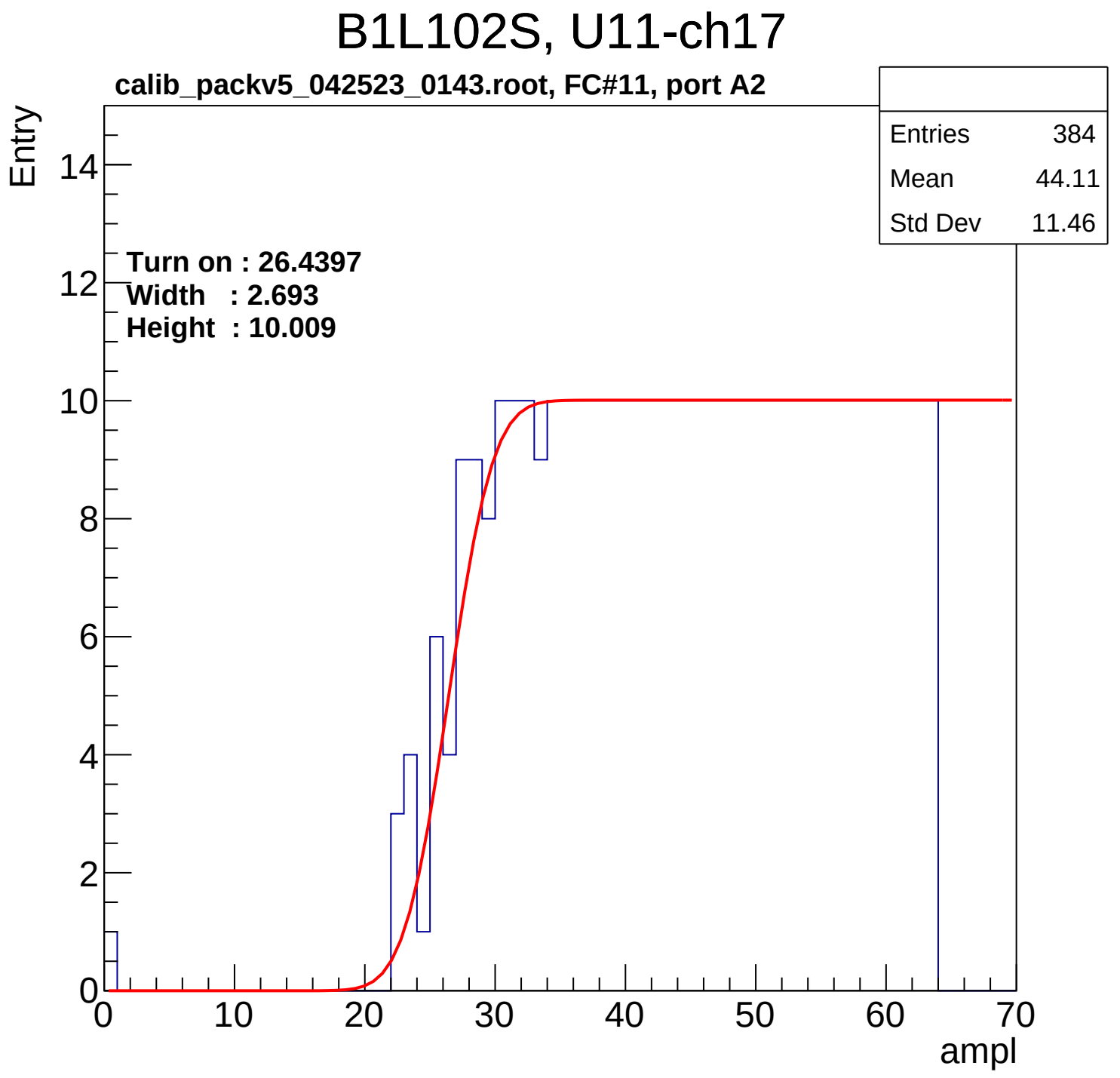
B1L102S, U11-ch17
calib_packv5_042523_0143.root, FC#11, port A2
Entries 384
Mean 44.11
Std Dev 11.46
Turn on : 26.4397
Width : 2.693
Height : 10.009
Entry
ampl
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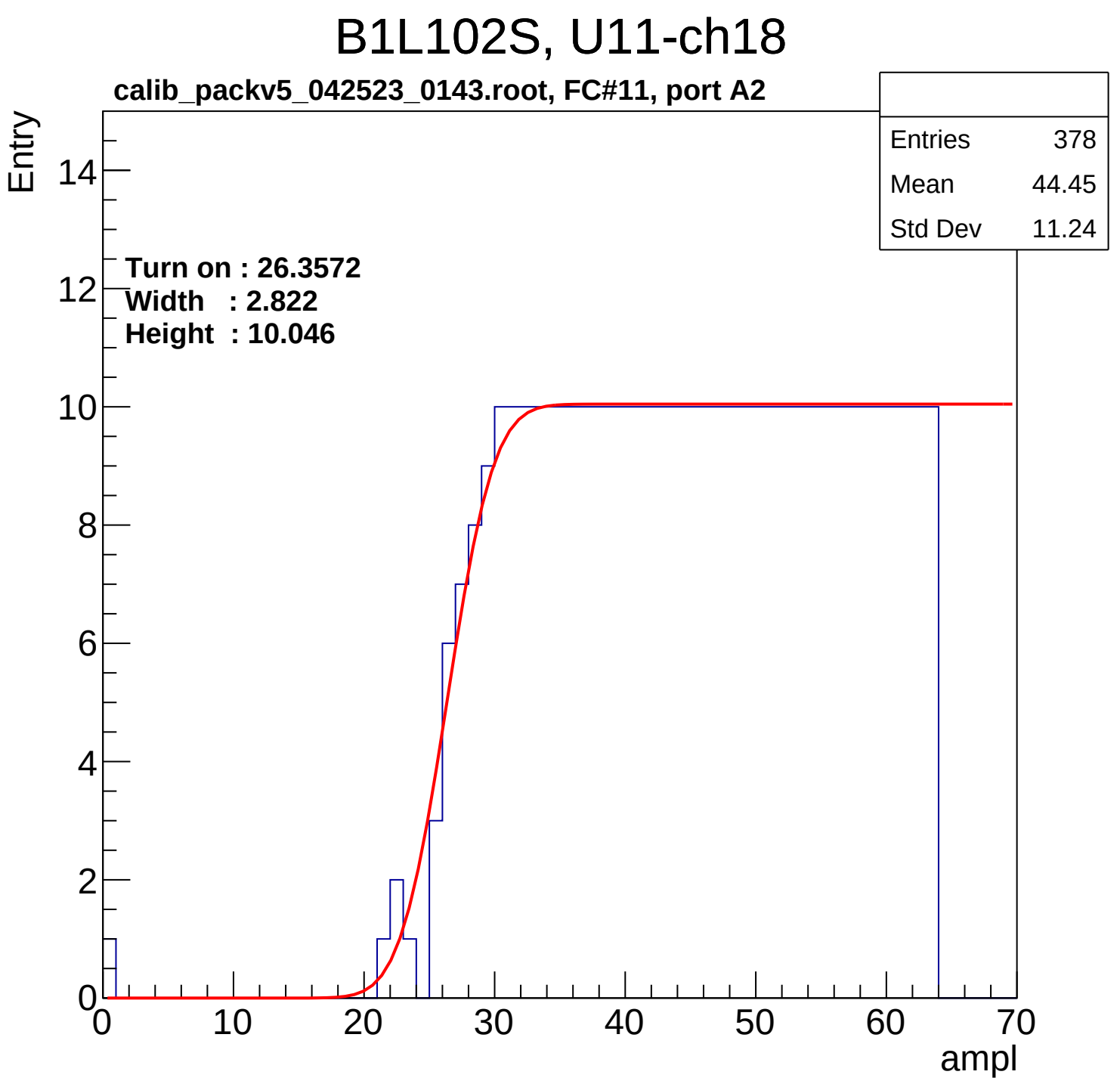
B1L102S, U11-ch18
calib_packv5_042523_0143.root, FC#11, port A2
Entries 378
Mean 44.45
Std Dev 11.24
Turn on : 26.3572
Width : 2.822
Height : 10.046
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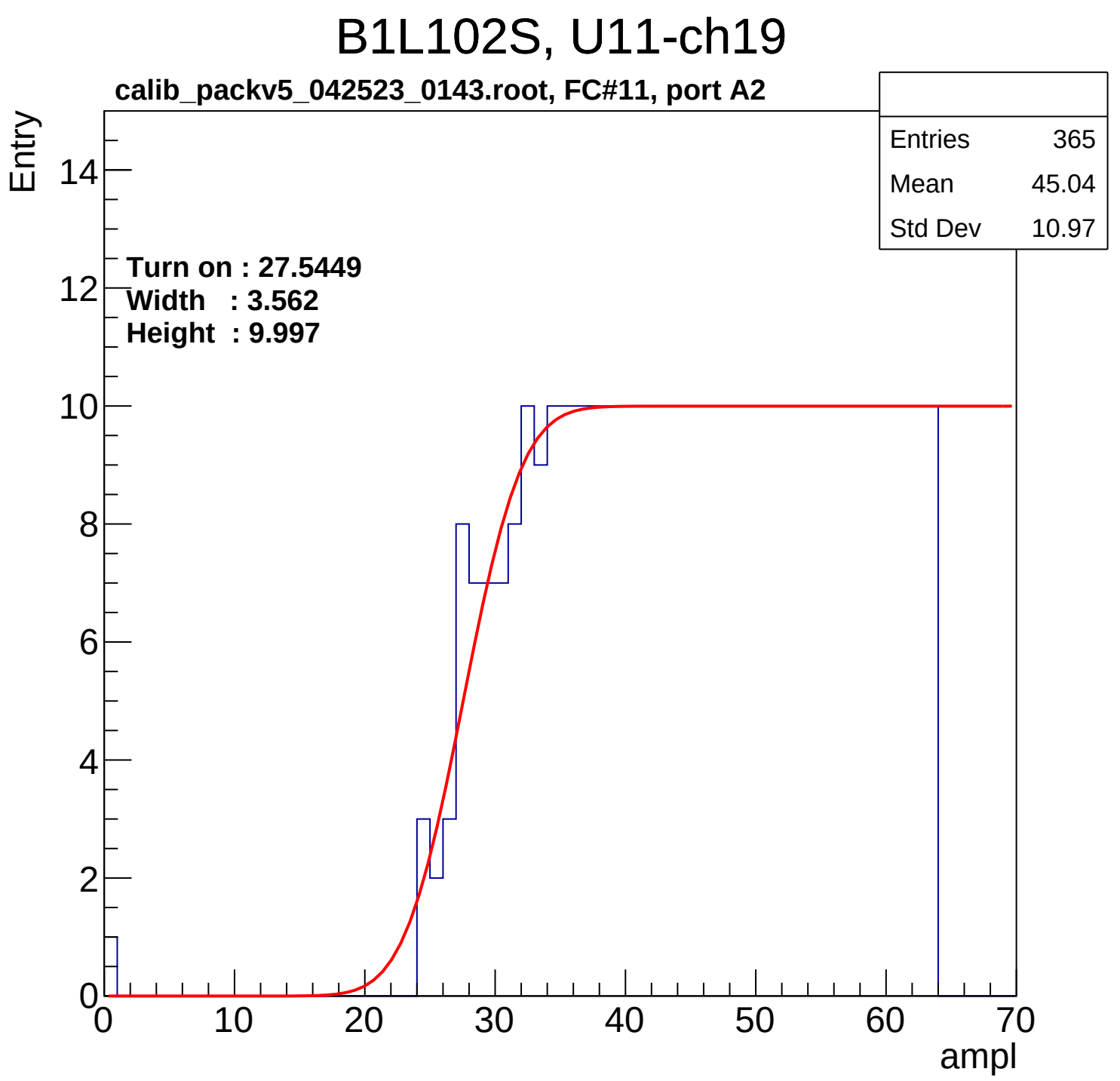
B1L102S, U11-ch19
calib_packv5_042523_0143.root, FC#11, port A2
Entries 365
Mean 45.04
Std Dev 10.97
Turn on : 27.5449
Width : 3.562
Height : 9.997
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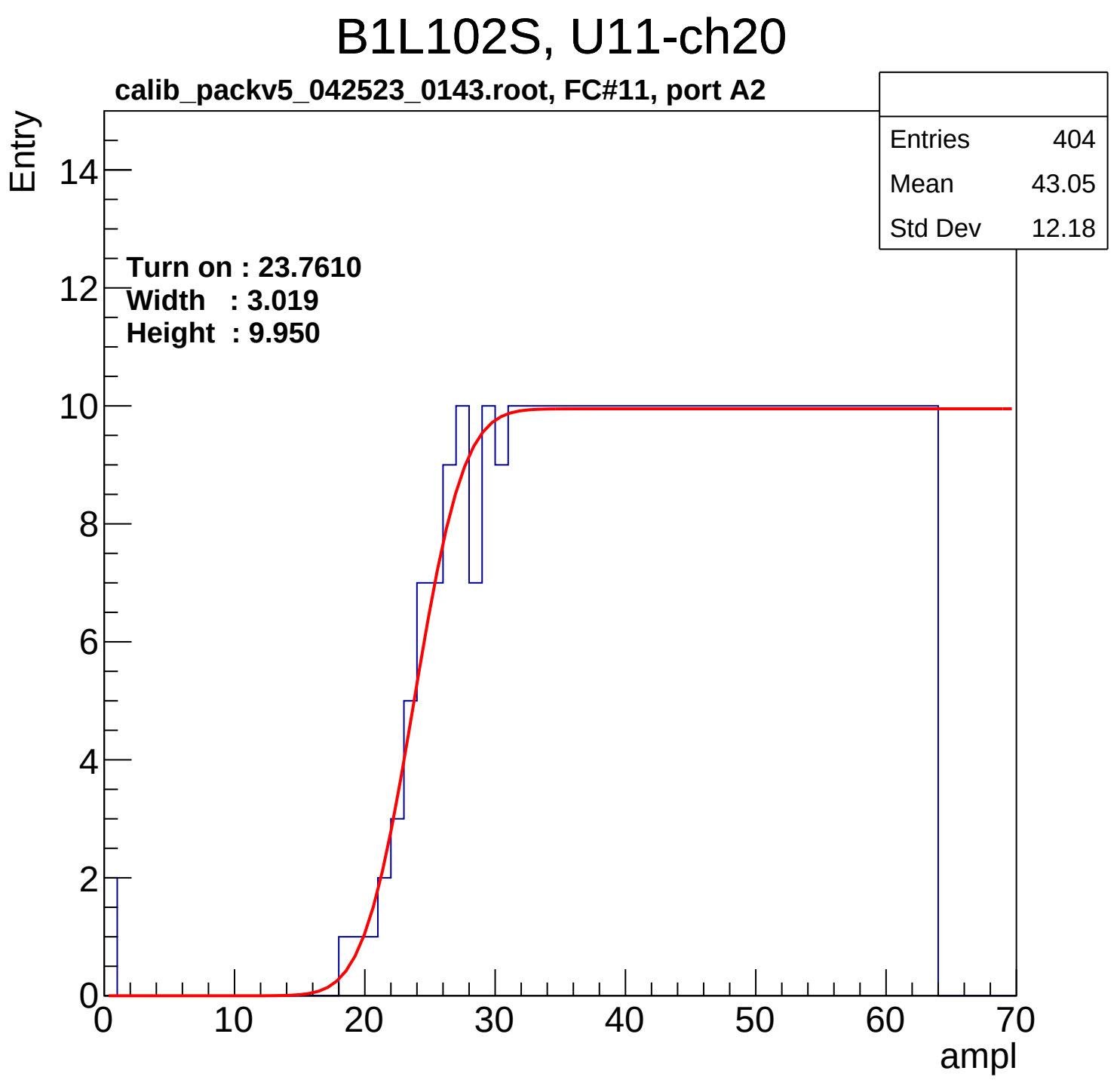
B1L102S, U11-ch20
calib_packv5_042523_0143.root, FC#11, port A2
Entries 404
Mean 43.05
Std Dev 12.18
Turn on : 23.7610
Width : 3.019
Height : 9.950
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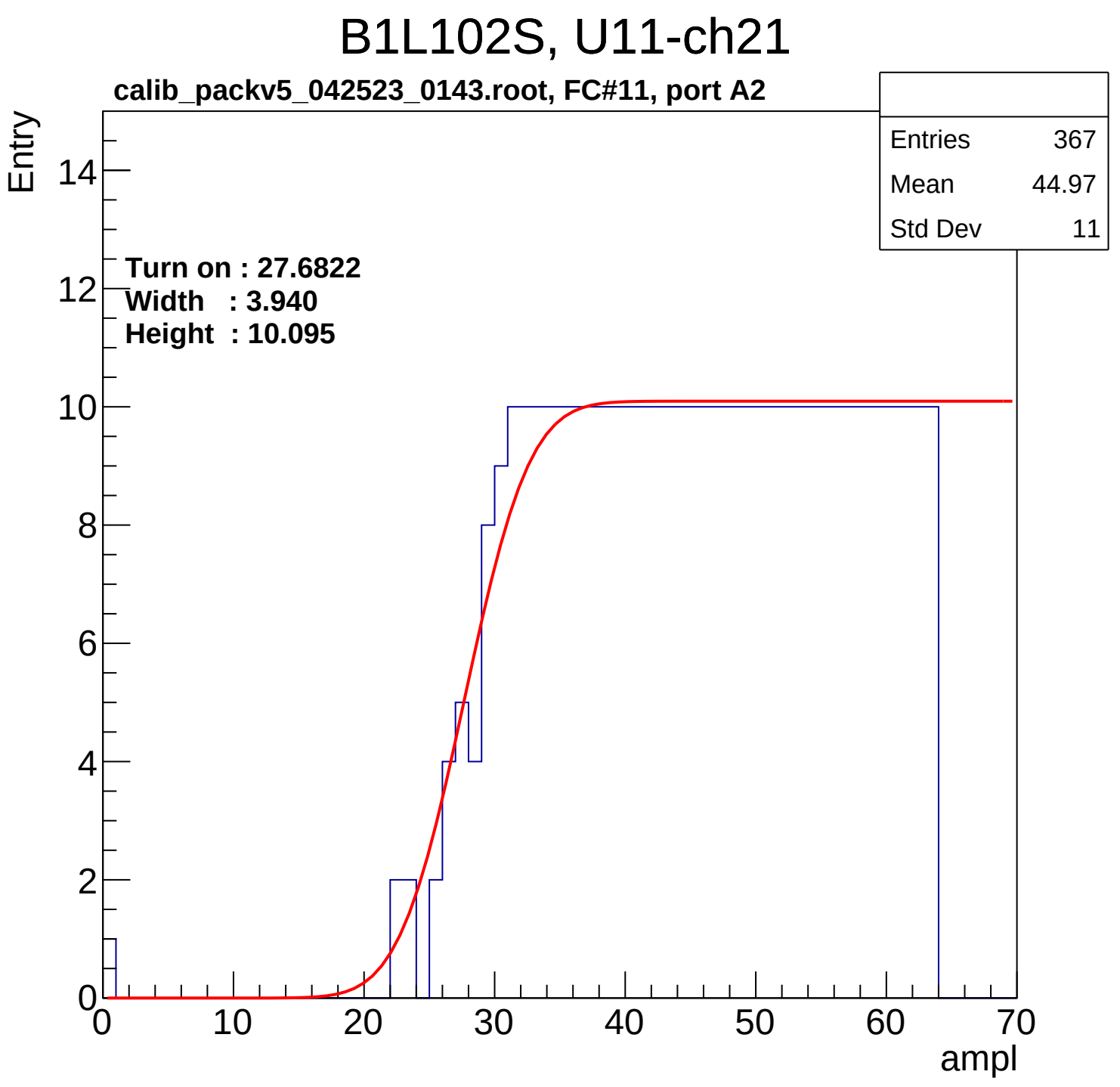
B1L102S, U11-ch21
calib_packv5_042523_0143.root, FC#11, port A2
Entries 367
Mean 44.97
Std Dev 11
Turn on : 27.6822
Width : 3.940
Height : 10.095
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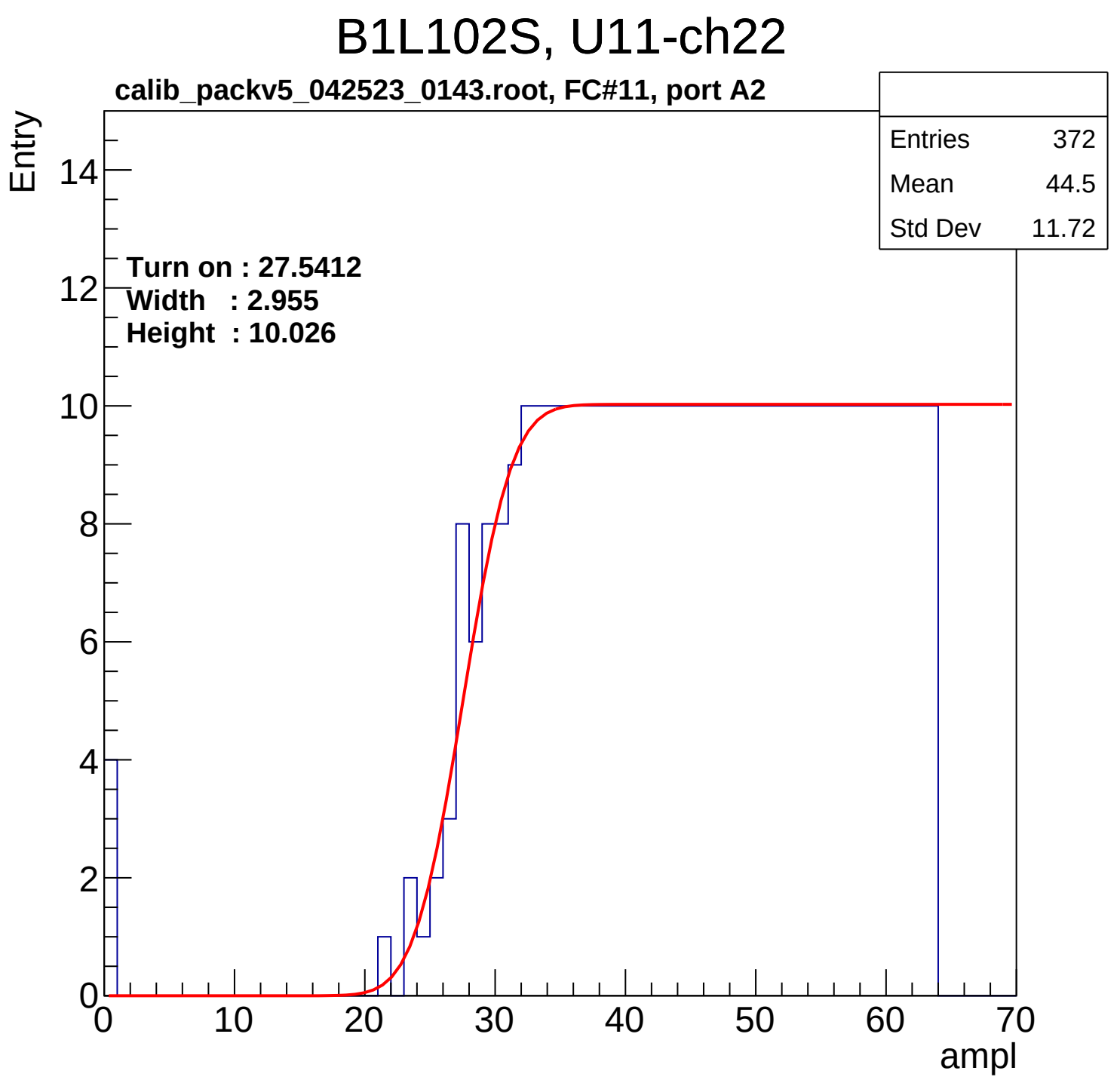
B1L102S, U11-ch22
calib_packv5_042523_0143.root, FC#11, port A2
Entries 372
Mean 44.5
Std Dev 11.72
Turn on : 27.5412
Width : 2.955
Height : 10.026
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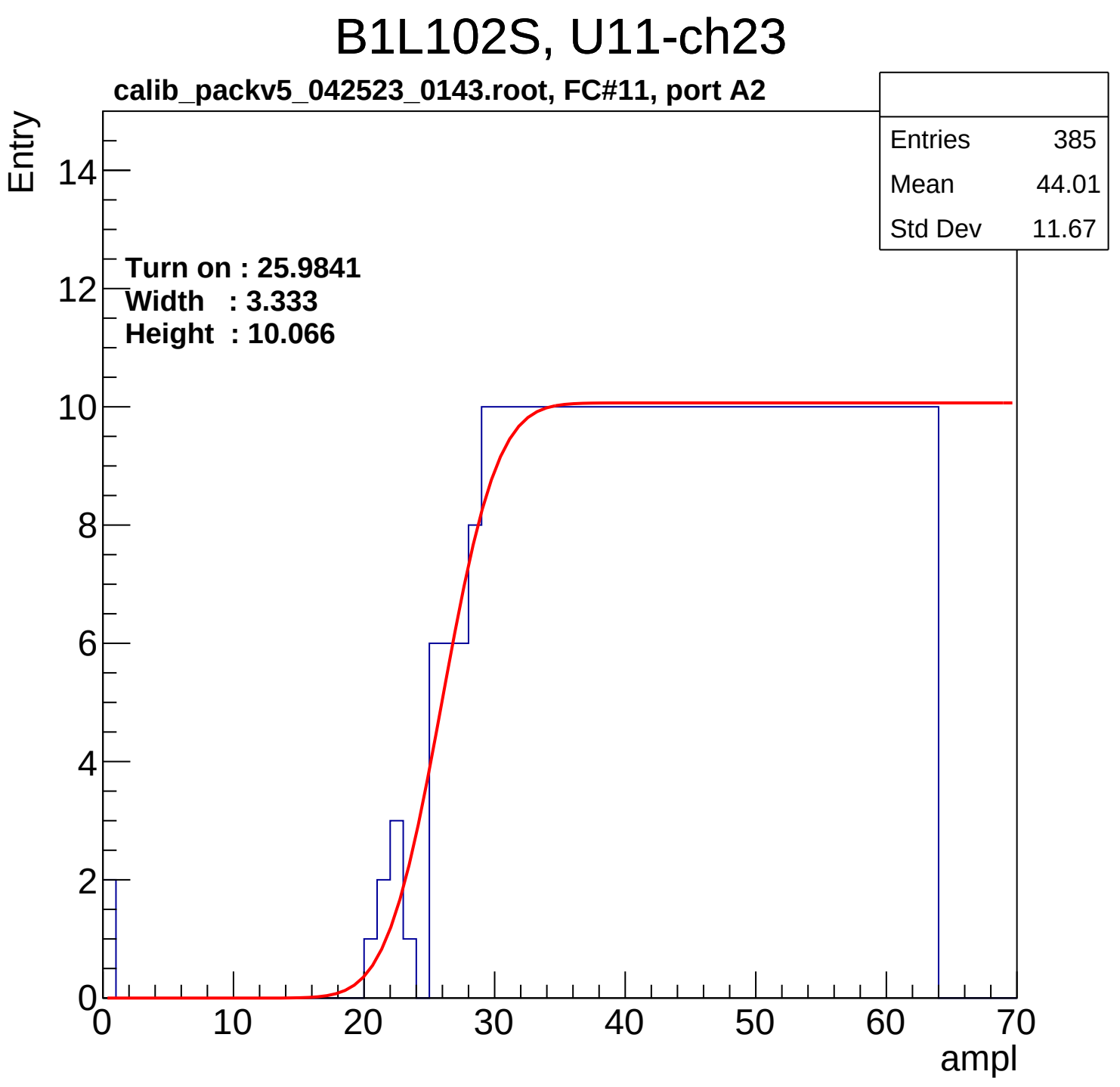
B1L102S, U11-ch23
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 44.01
Std Dev 11.67
Turn on : 25.9841
Width : 3.333
Height : 10.066
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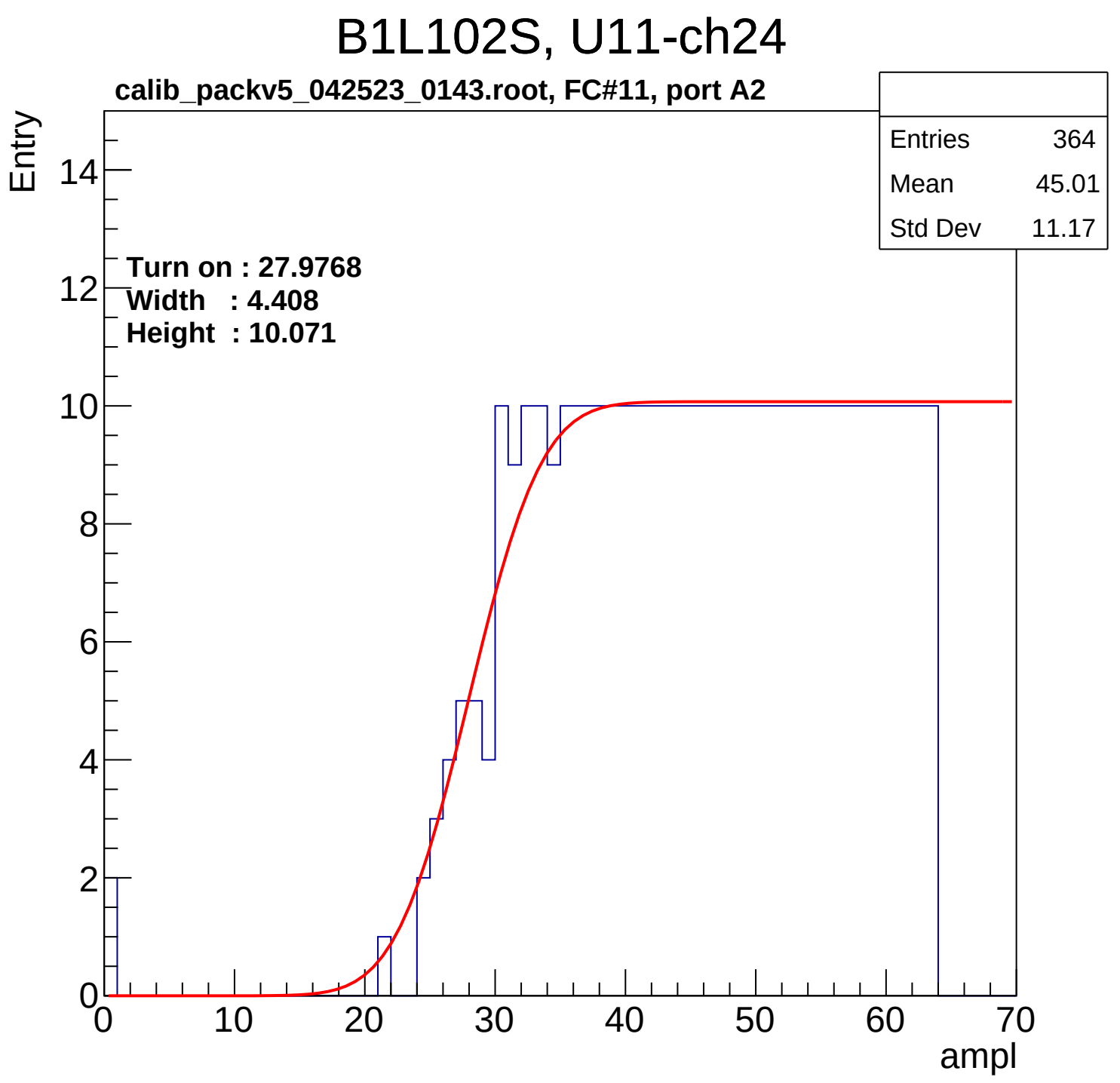
B1L102S, U11-ch24
calib_packv5_042523_0143.root, FC#11, port A2
Entries 364
Mean 45.01
Std Dev 11.17
Turn on : 27.9768
Width : 4.408
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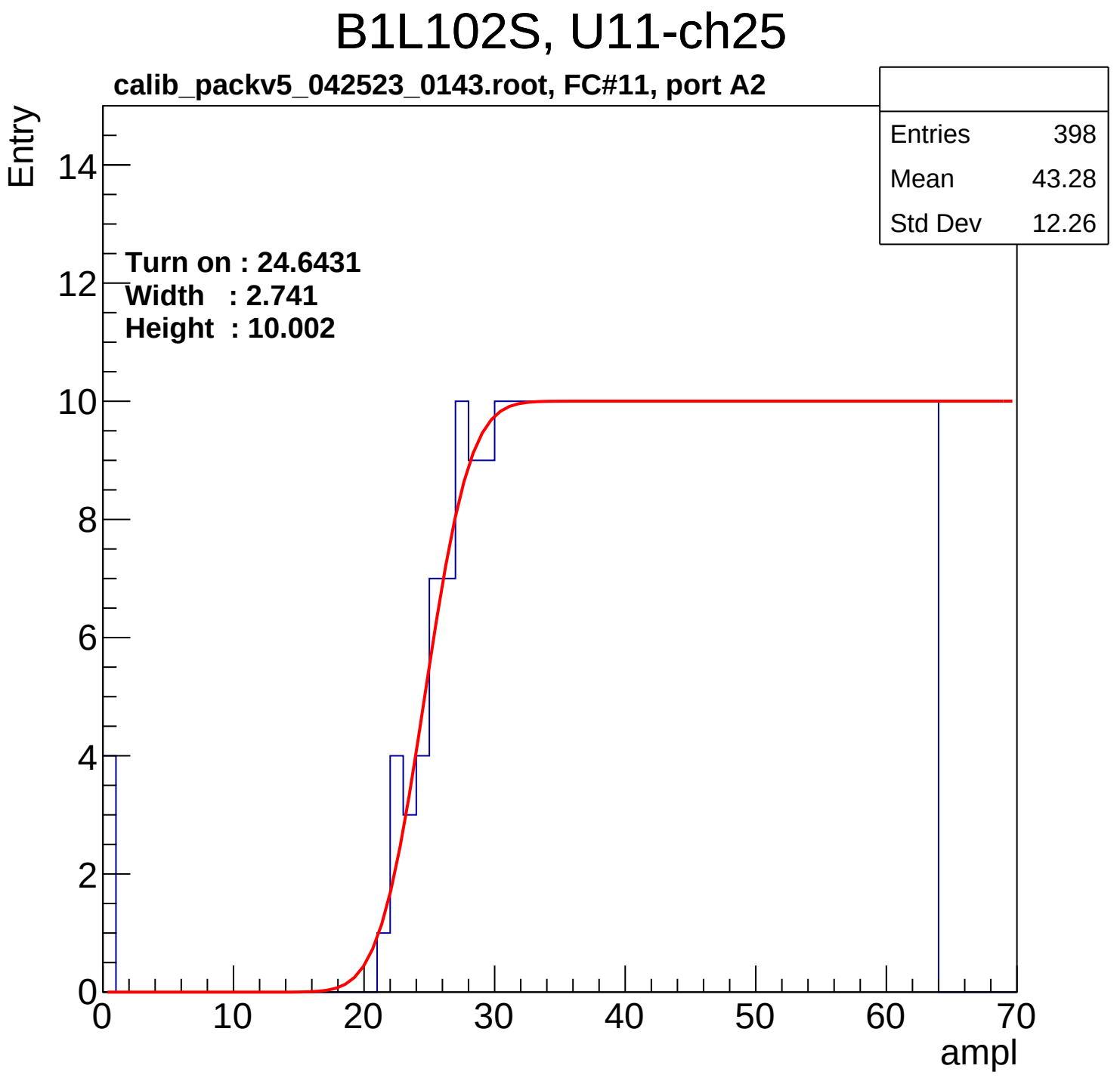
B1L102S, U11-ch25
calib_packv5_042523_0143.root, FC#11, port A2
Entries 398
Mean 43.28
Std Dev 12.26
Turn on : 24.6431
Width : 2.741
Height : 10.002
Entry
ampl
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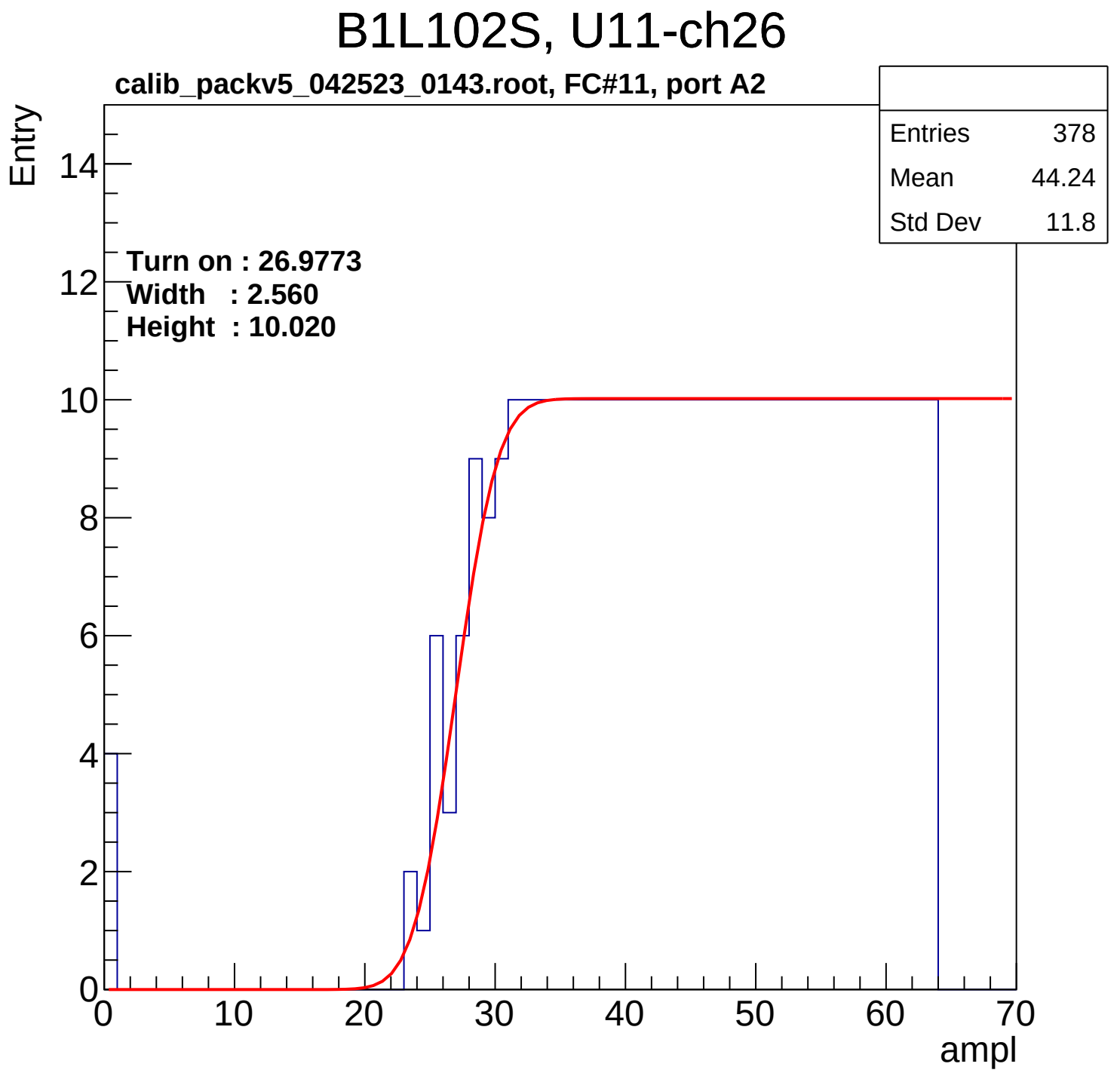
B1L102S, U11-ch26
calib_packv5_042523_0143.root, FC#11, port A2
Entries 378
Mean 44.24
Std Dev 11.8
Turn on : 26.9773
Width : 2.560
Height : 10.020
Entry
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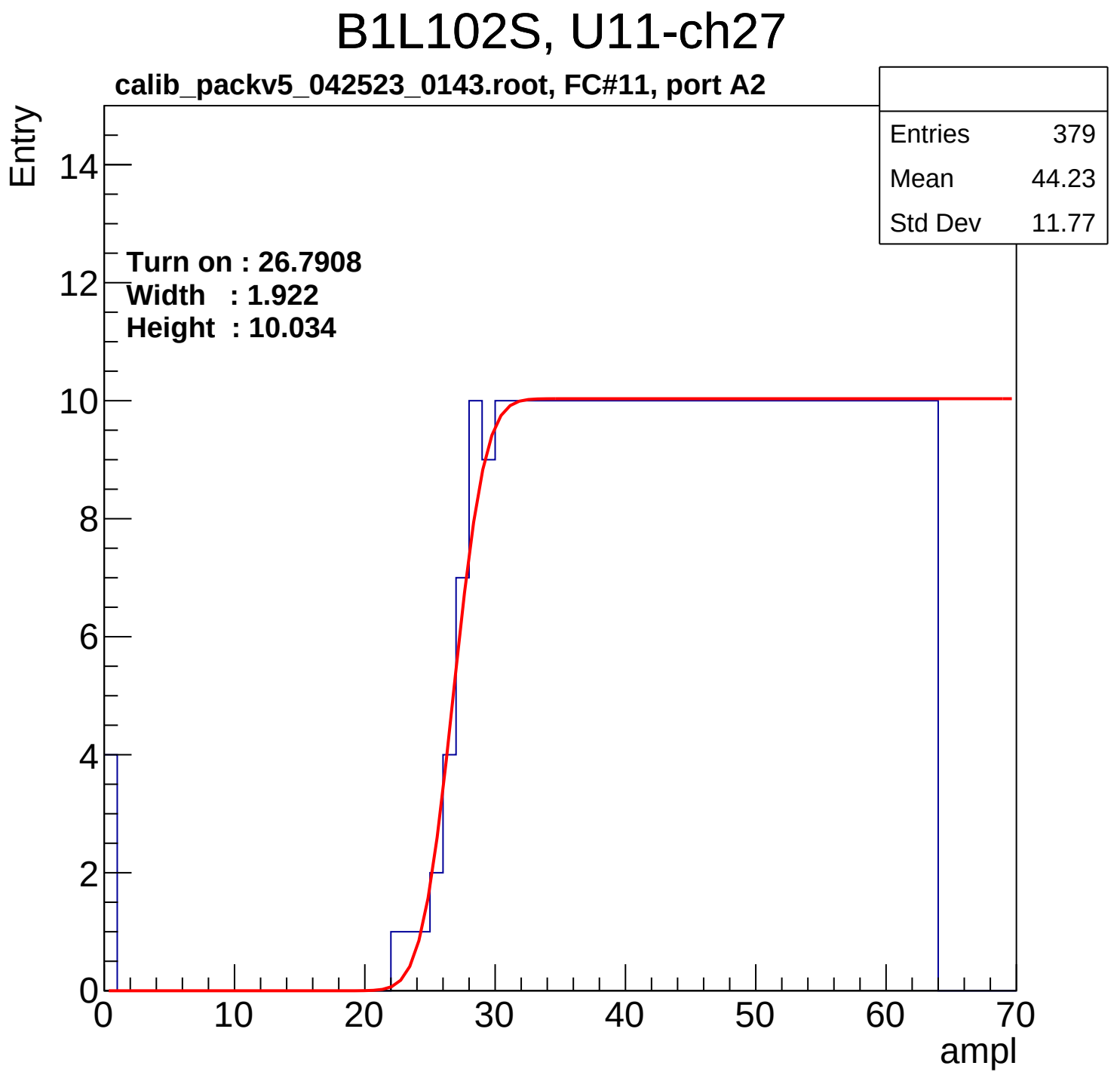
B1L102S, U11-ch27
calib_packv5_042523_0143.root, FC#11, port A2
Entries 379
Mean 44.23
Std Dev 11.77
Turn on : 26.7908
Width : 1.922
Height : 10.034
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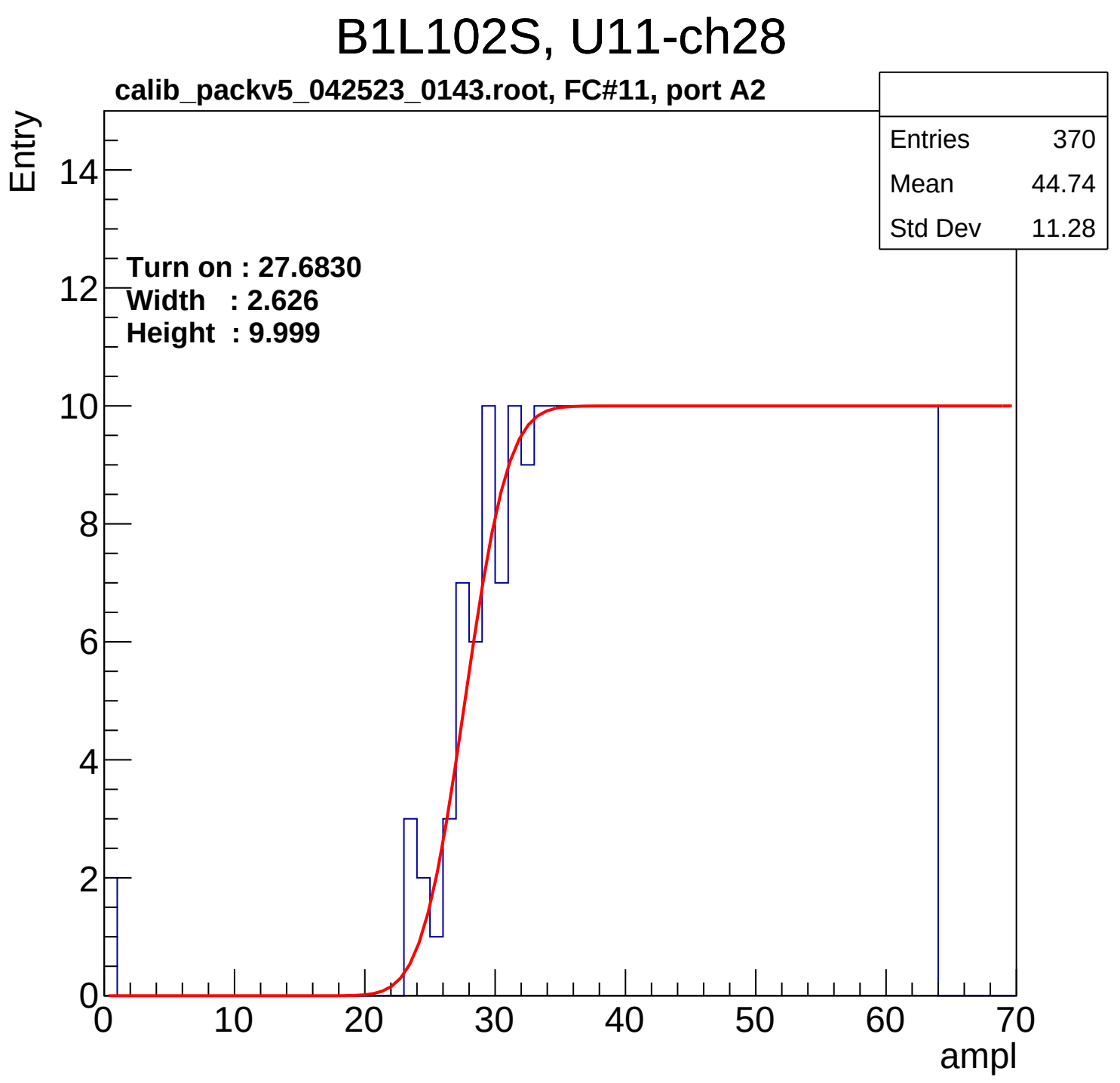
B1L102S, U11-ch28
calib_packv5_042523_0143.root, FC#11, port A2
Entries 370
Mean 44.74
Std Dev 11.28
Turn on : 27.6830
Width : 2.626
Height : 9.999
Entry
ampl
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4
6
8
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0
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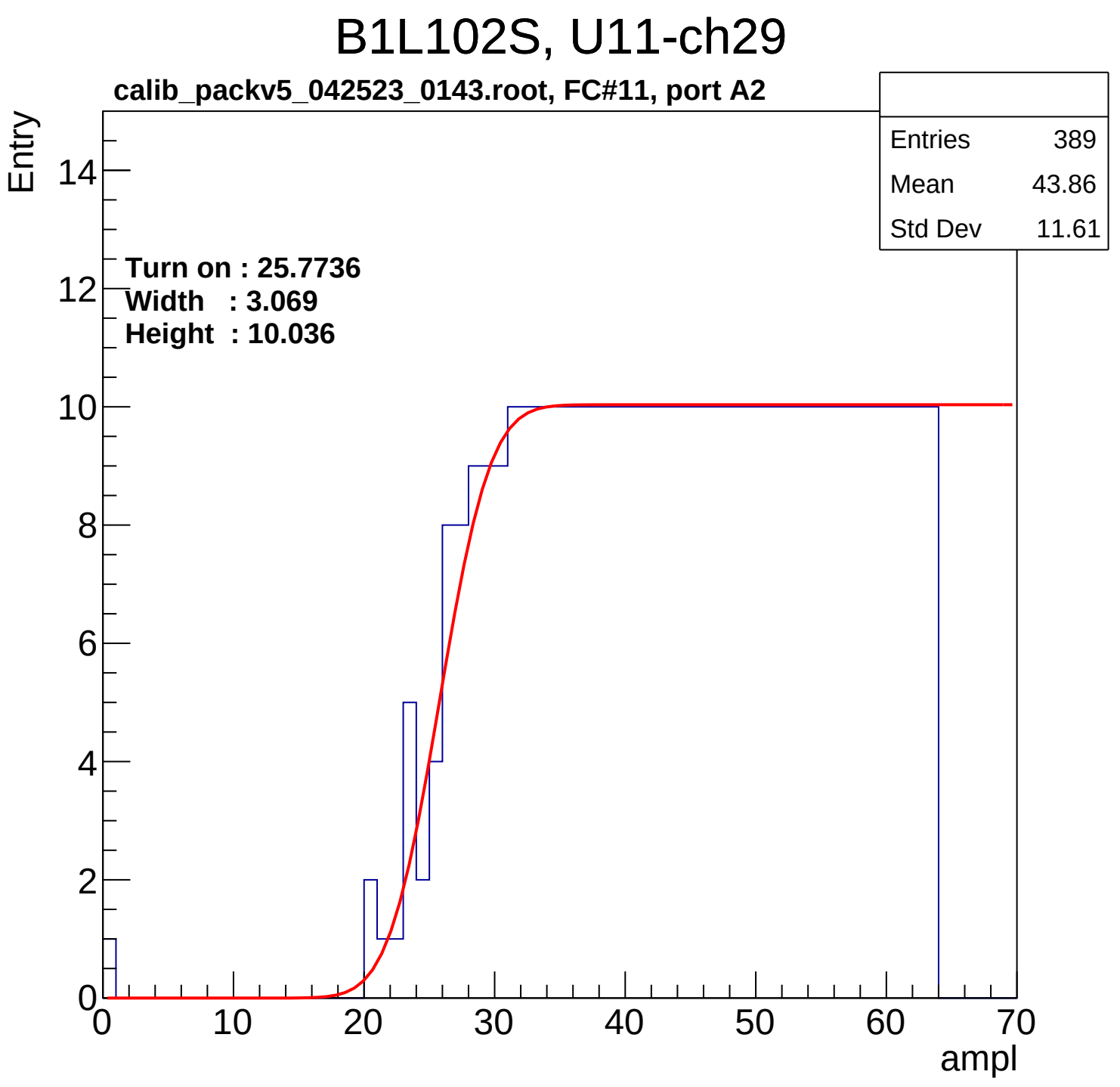
B1L102S, U11-ch29
calib_packv5_042523_0143.root, FC#11, port A2
Entries 389
Mean 43.86
Std Dev 11.61
Turn on : 25.7736
Width : 3.069
Height : 10.036
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ampl
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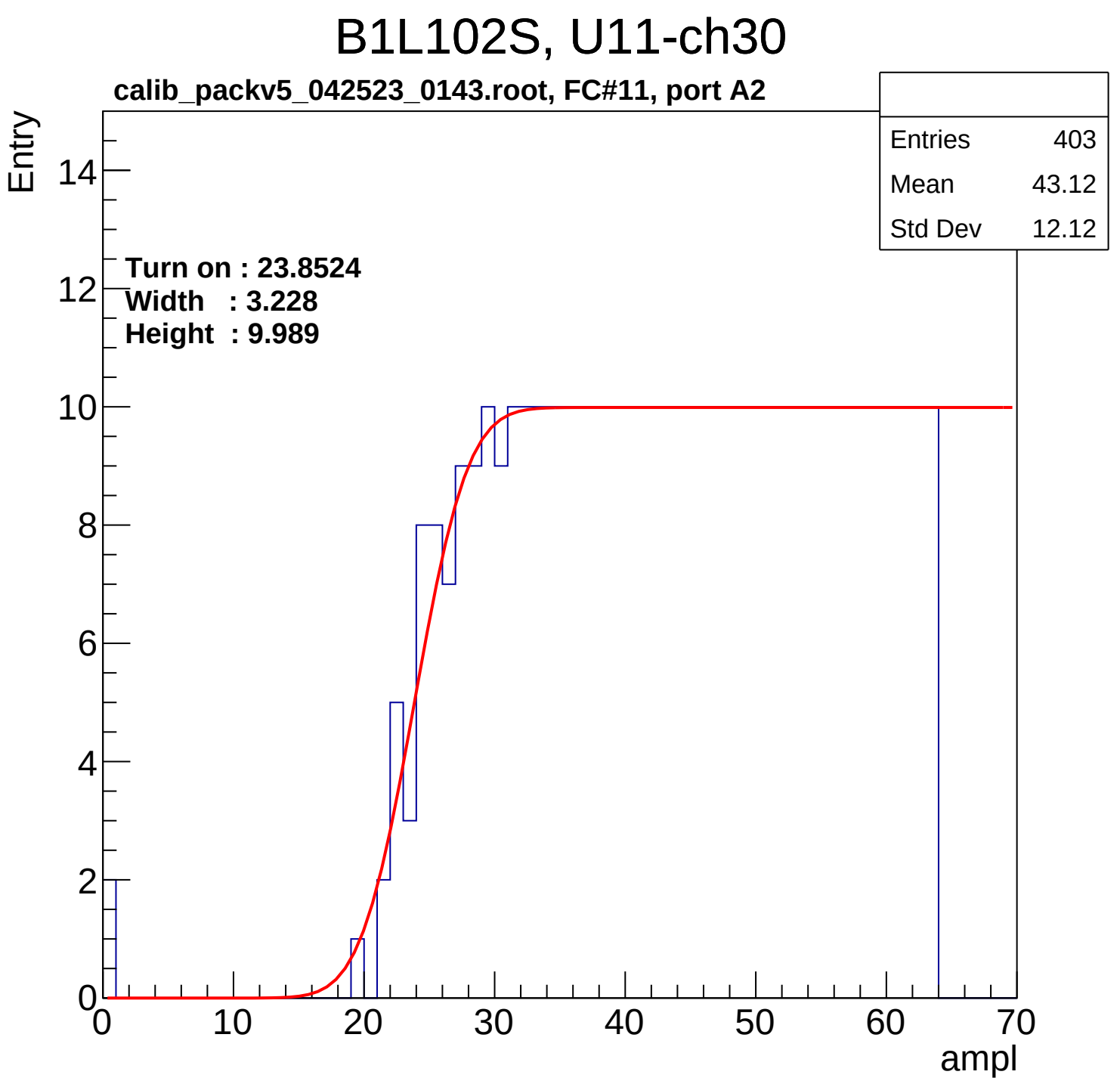
B1L102S, U11-ch30
calib_packv5_042523_0143.root, FC#11, port A2
Entries 403
Mean 43.12
Std Dev 12.12
Turn on : 23.8524
Width : 3.228
Height : 9.989
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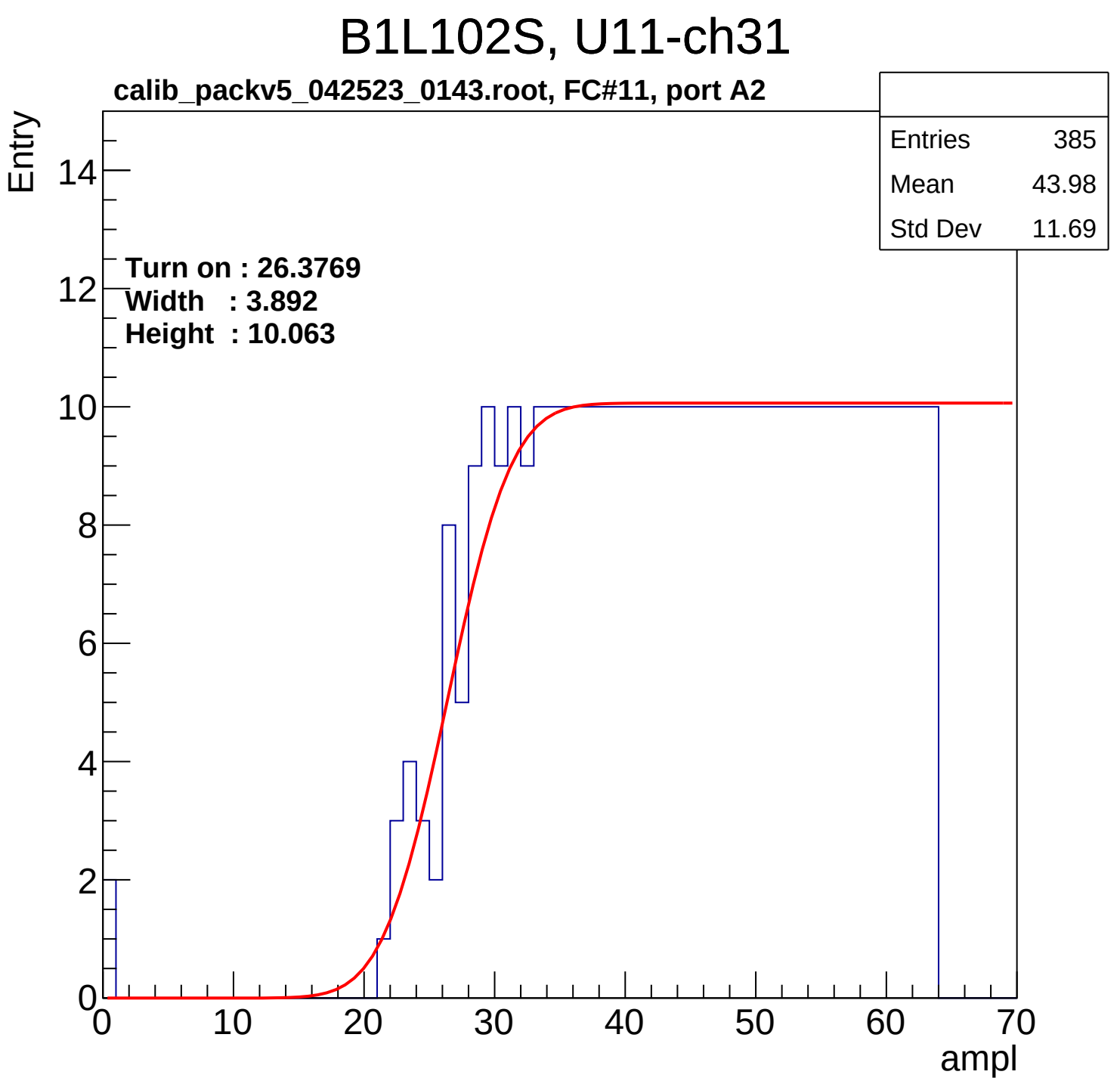
B1L102S, U11-ch31
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 43.98
Std Dev 11.69
Turn on : 26.3769
Width : 3.892
Height : 10.063
Entry
ampl
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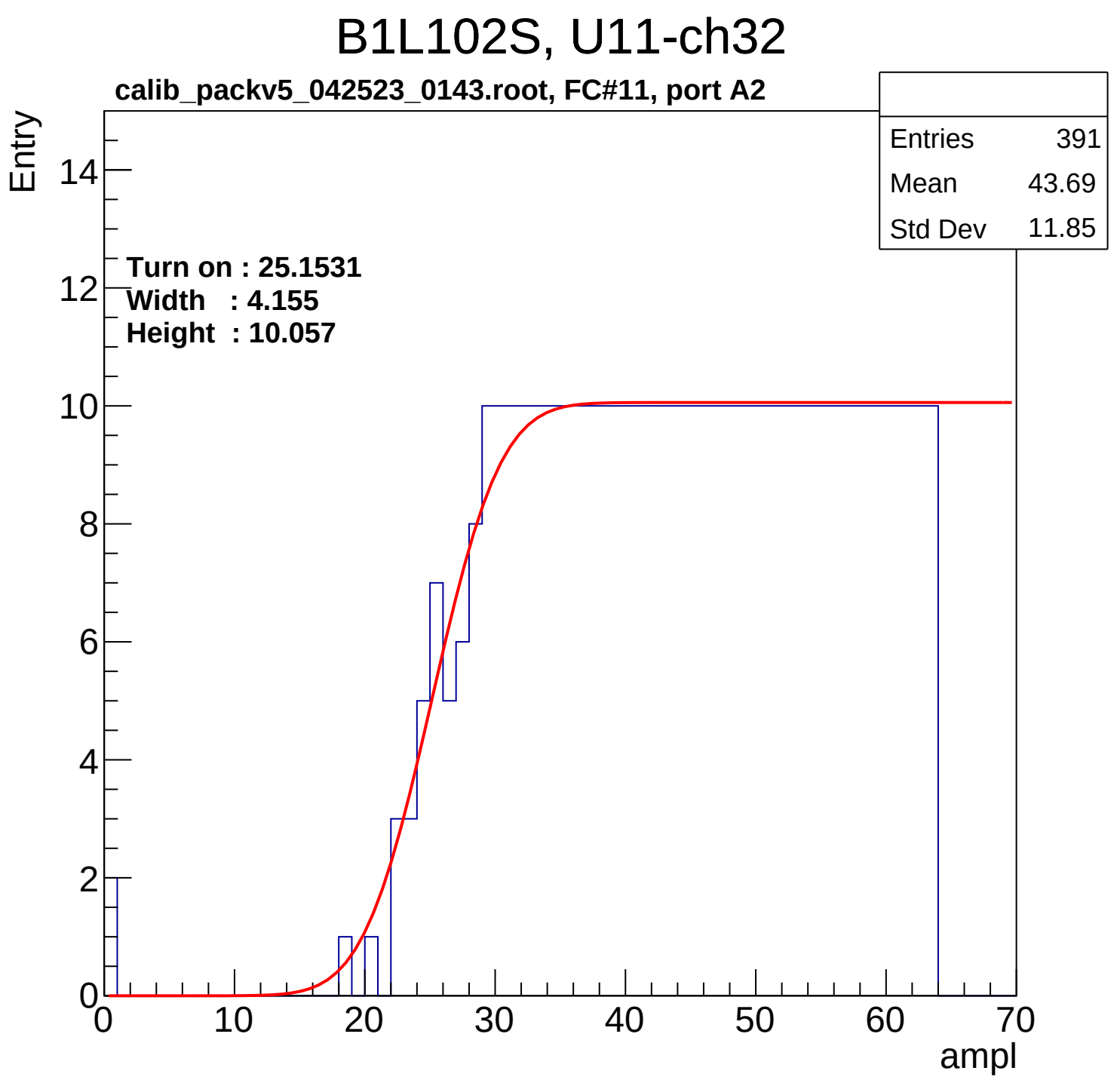
B1L102S, U11-ch32
calib_packv5_042523_0143.root, FC#11, port A2
Entries 391
Mean 43.69
Std Dev 11.85
Turn on : 25.1531
Width : 4.155
Height : 10.057
Entry
ampl
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4
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8
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12
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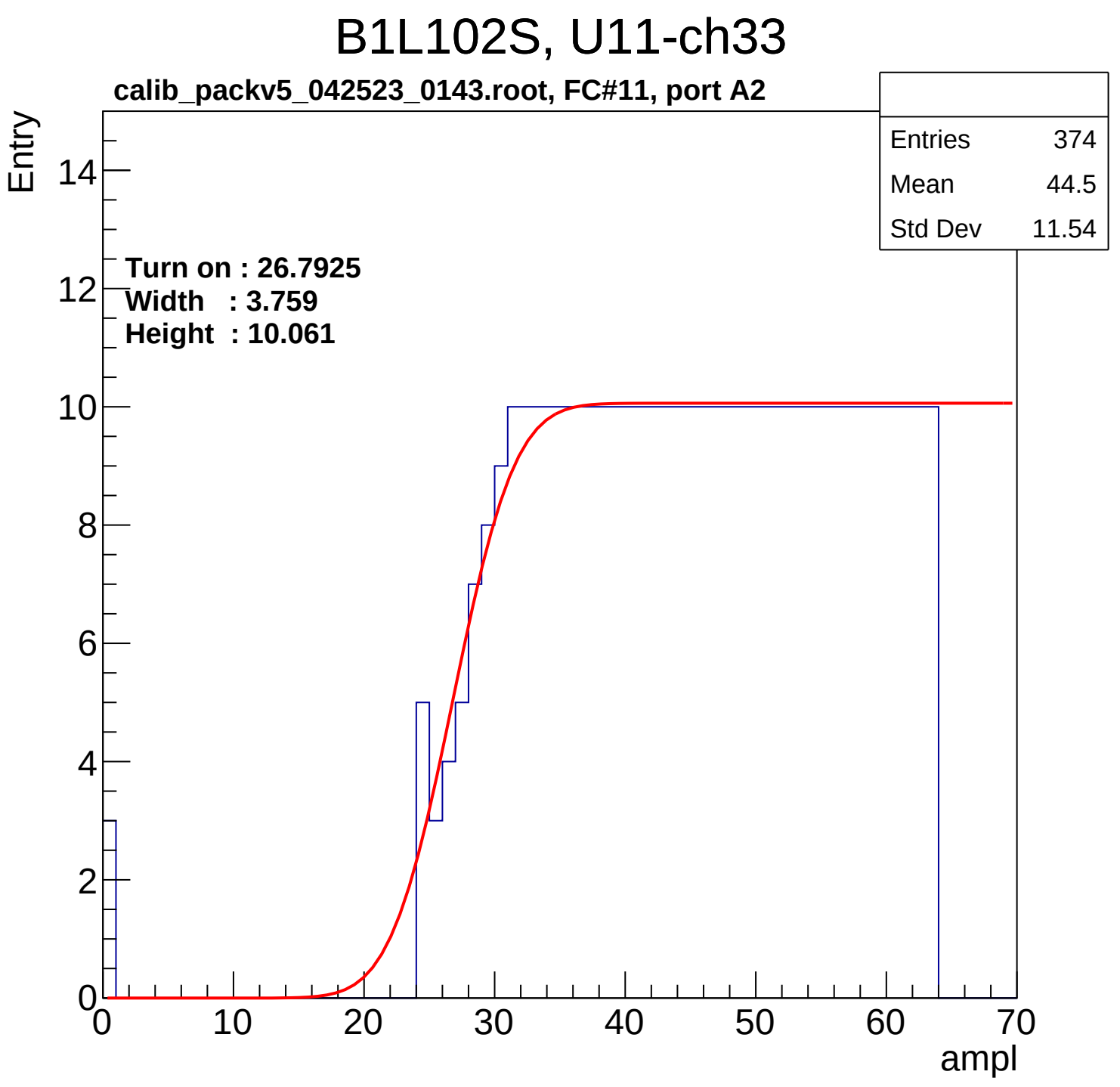
B1L102S, U11-ch33
calib_packv5_042523_0143.root, FC#11, port A2
Entries 374
Mean 44.5
Std Dev 11.54
Turn on : 26.7925
Width : 3.759
Height : 10.061
Entry
ampl
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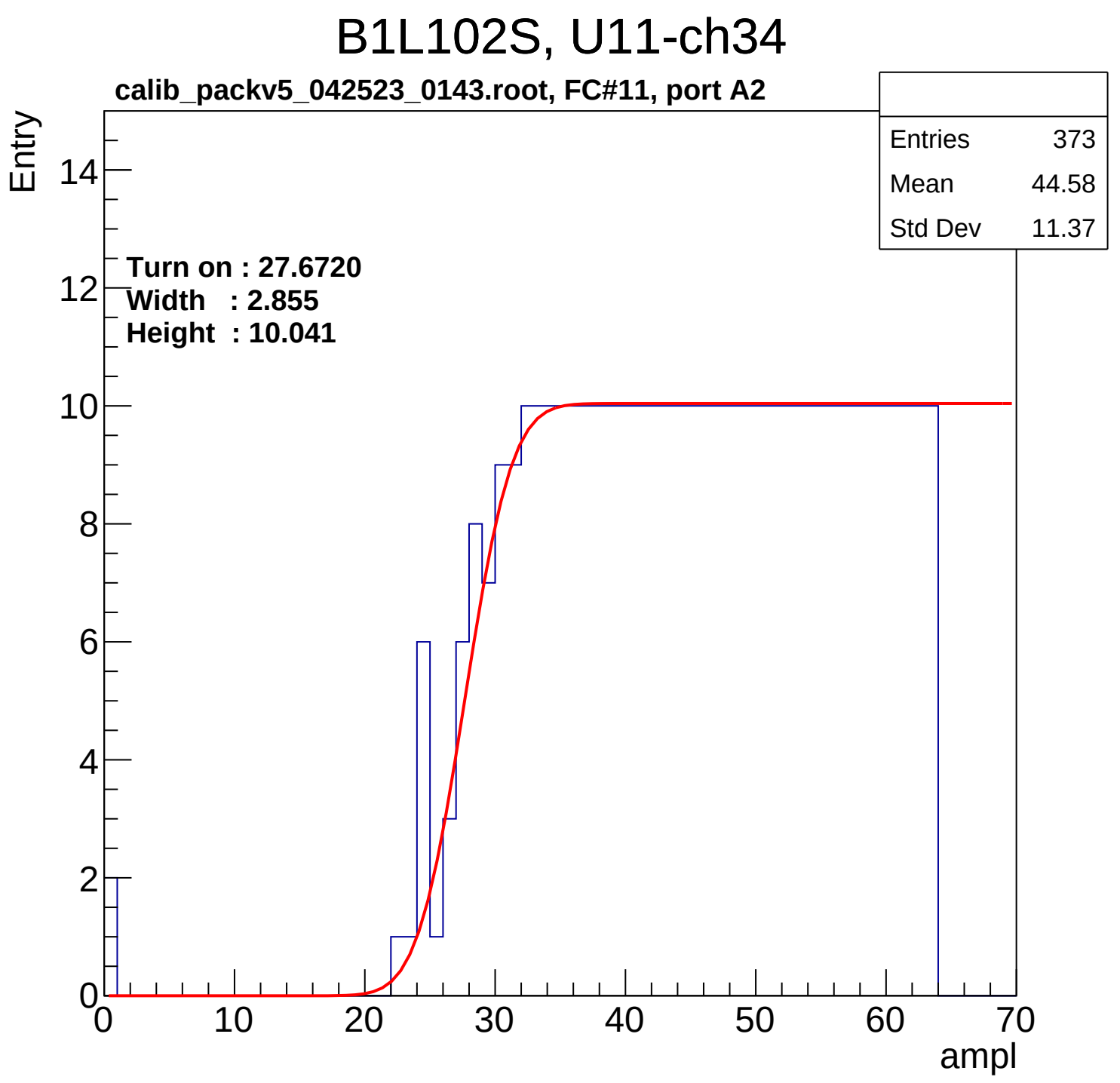
B1L102S, U11-ch34
calib_packv5_042523_0143.root, FC#11, port A2
Entries 373
Mean 44.58
Std Dev 11.37
Turn on : 27.6720
Width : 2.855
Height : 10.041
Entry
ampl
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2
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8
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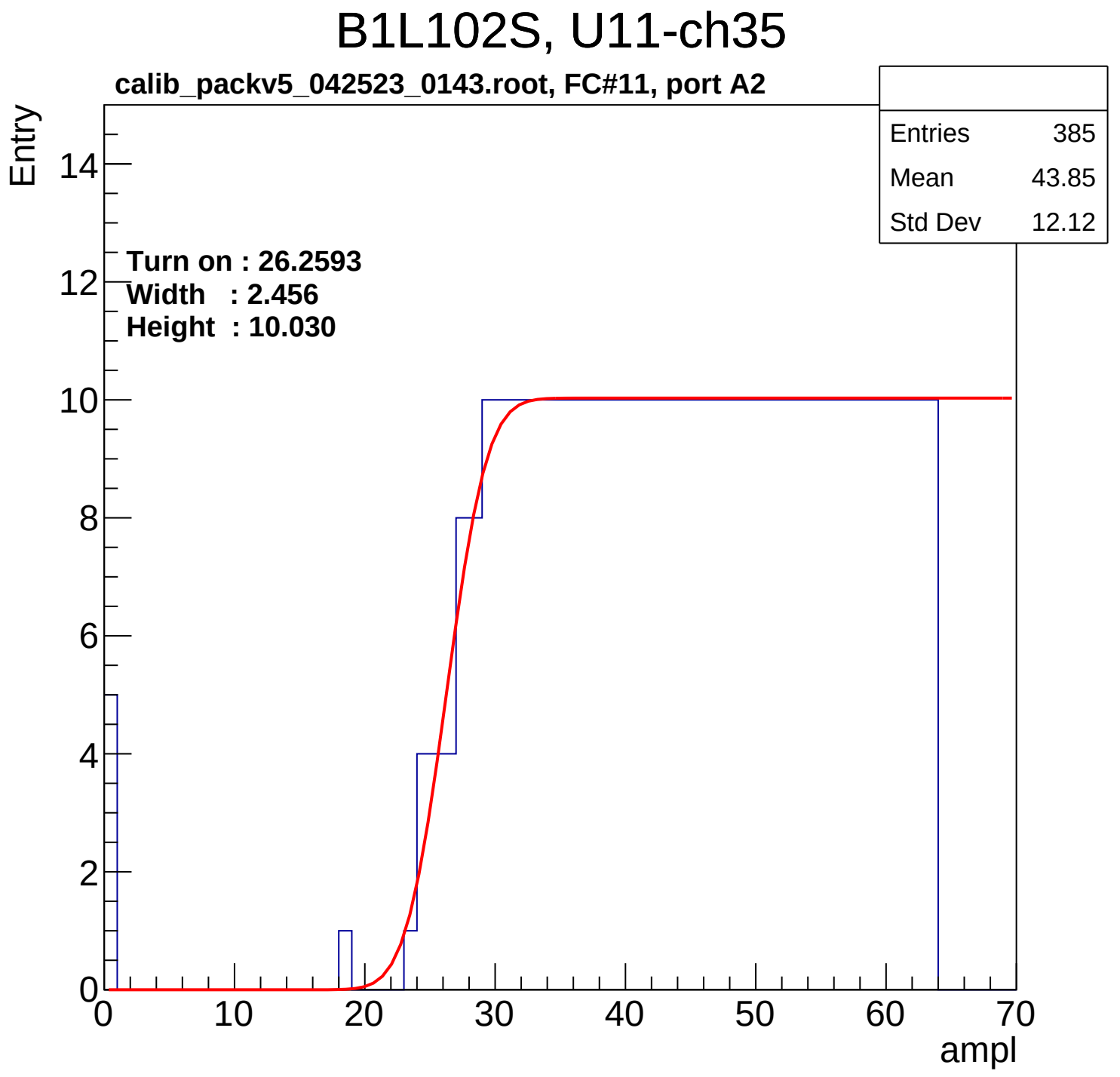
B1L102S, U11-ch35
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 43.85
Std Dev 12.12
Turn on : 26.2593
Width : 2.456
Height : 10.030
Entry
ampl
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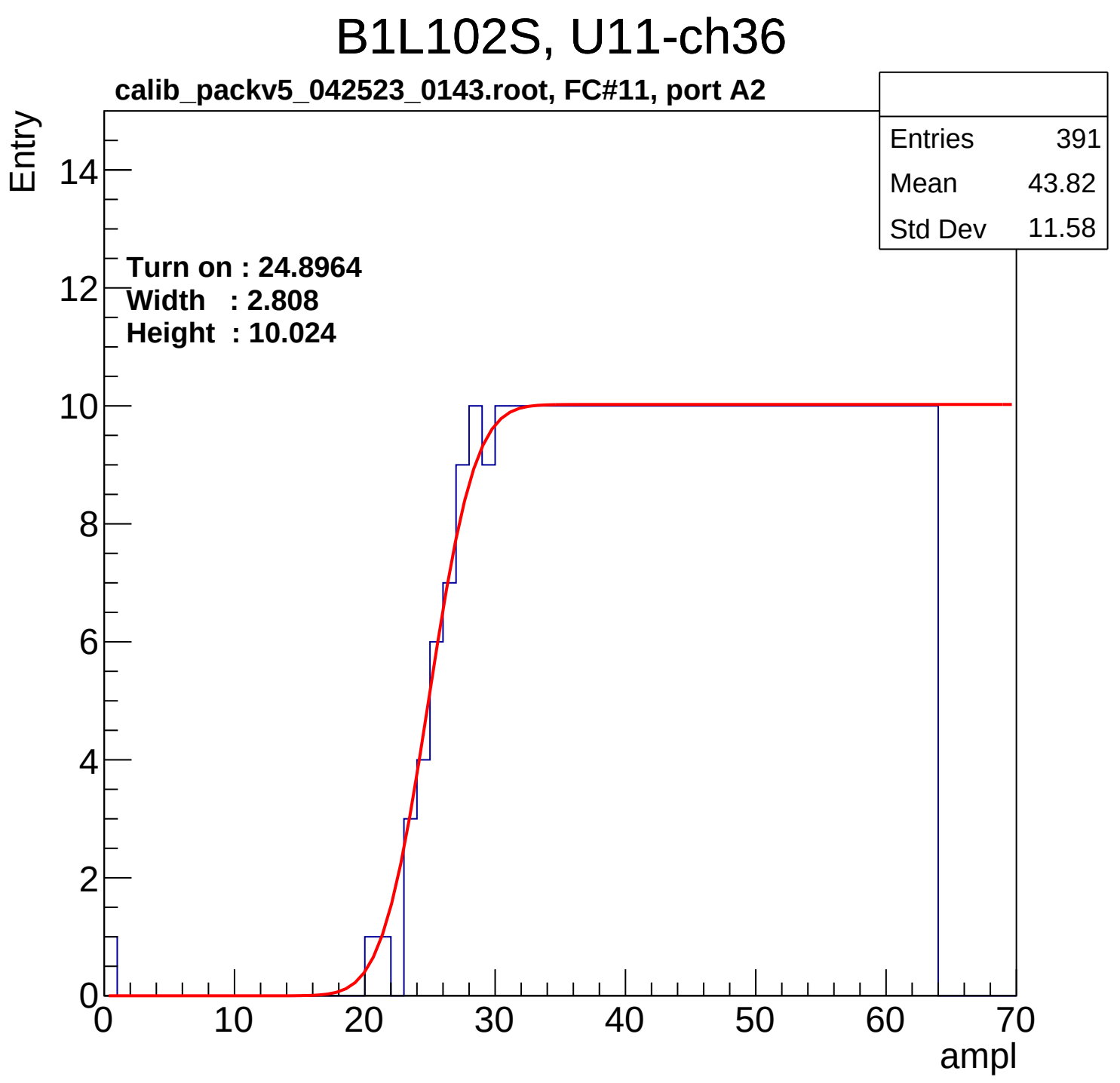
B1L102S, U11-ch36
calib_packv5_042523_0143.root, FC#11, port A2
Entries 391
Mean 43.82
Std Dev 11.58
Turn on : 24.8964
Width : 2.808
Height : 10.024
Entry
ampl
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6
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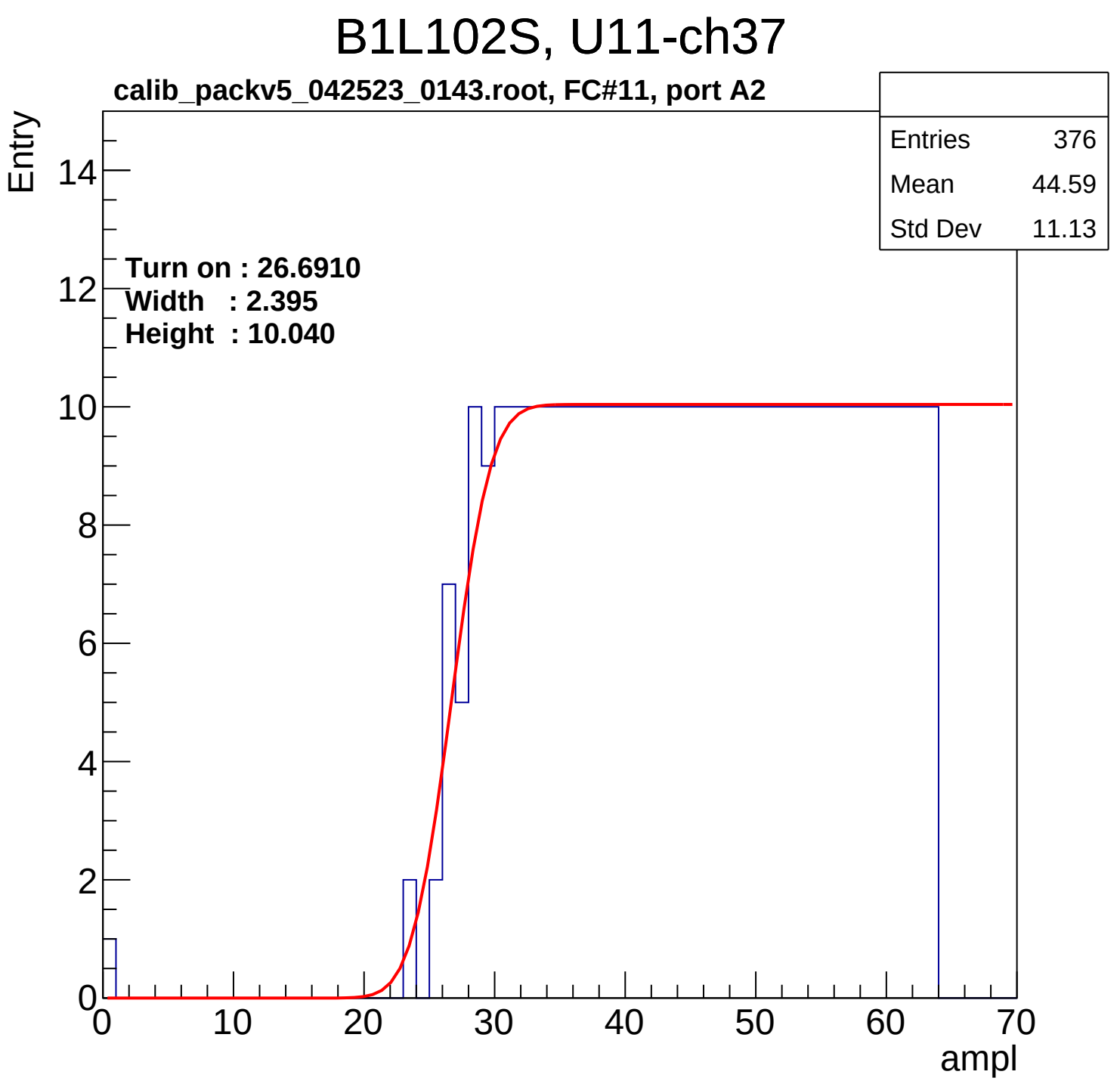
B1L102S, U11-ch37
calib_packv5_042523_0143.root, FC#11, port A2
Entries 376
Mean 44.59
Std Dev 11.13
Turn on : 26.6910
Width : 2.395
Height : 10.040
Entry
ampl
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6
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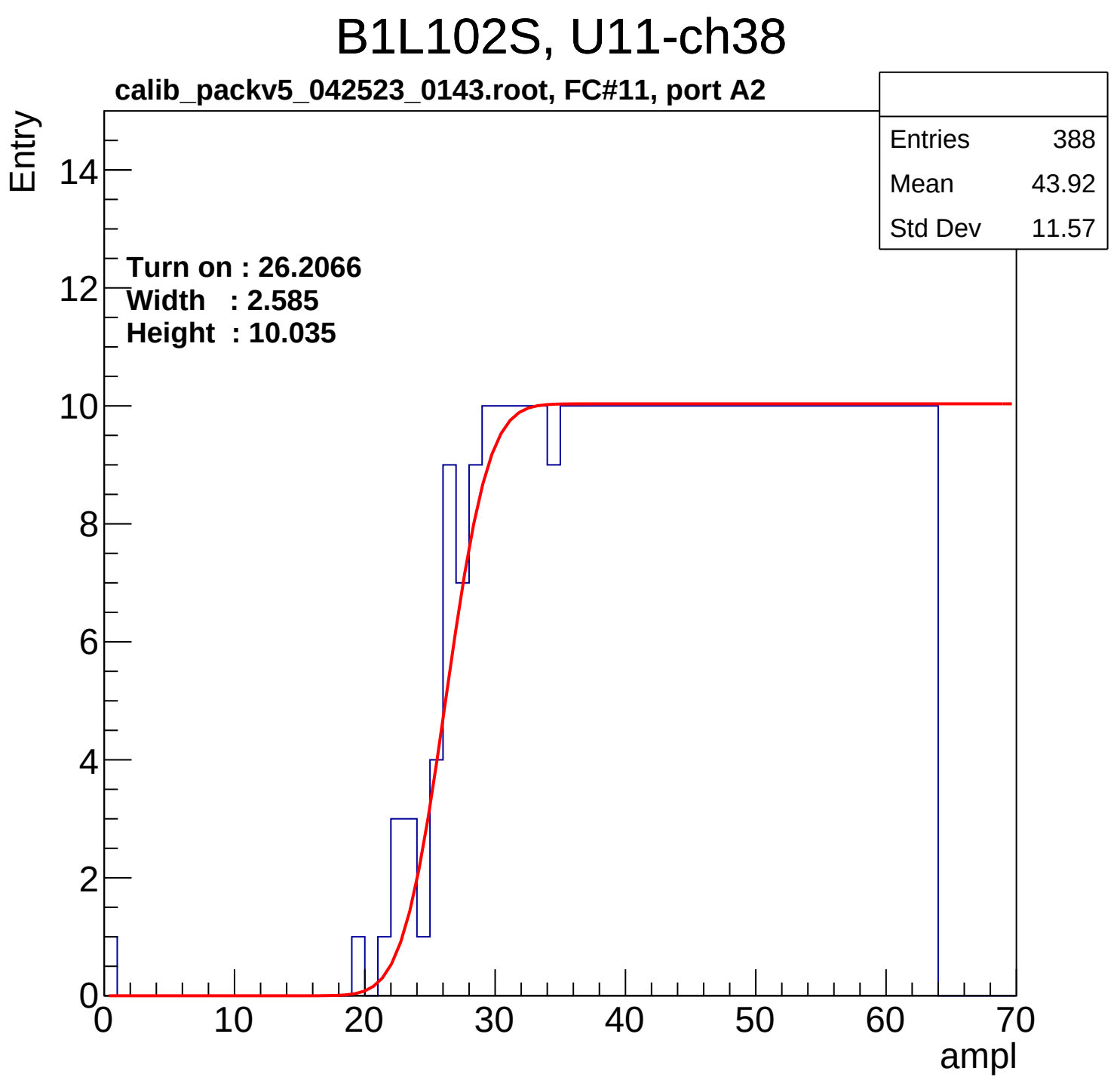
B1L102S, U11-ch38
calib_packv5_042523_0143.root, FC#11, port A2
Entries 388
Mean 43.92
Std Dev 11.57
Turn on : 26.2066
Width : 2.585
Height : 10.035
Entry
ampl
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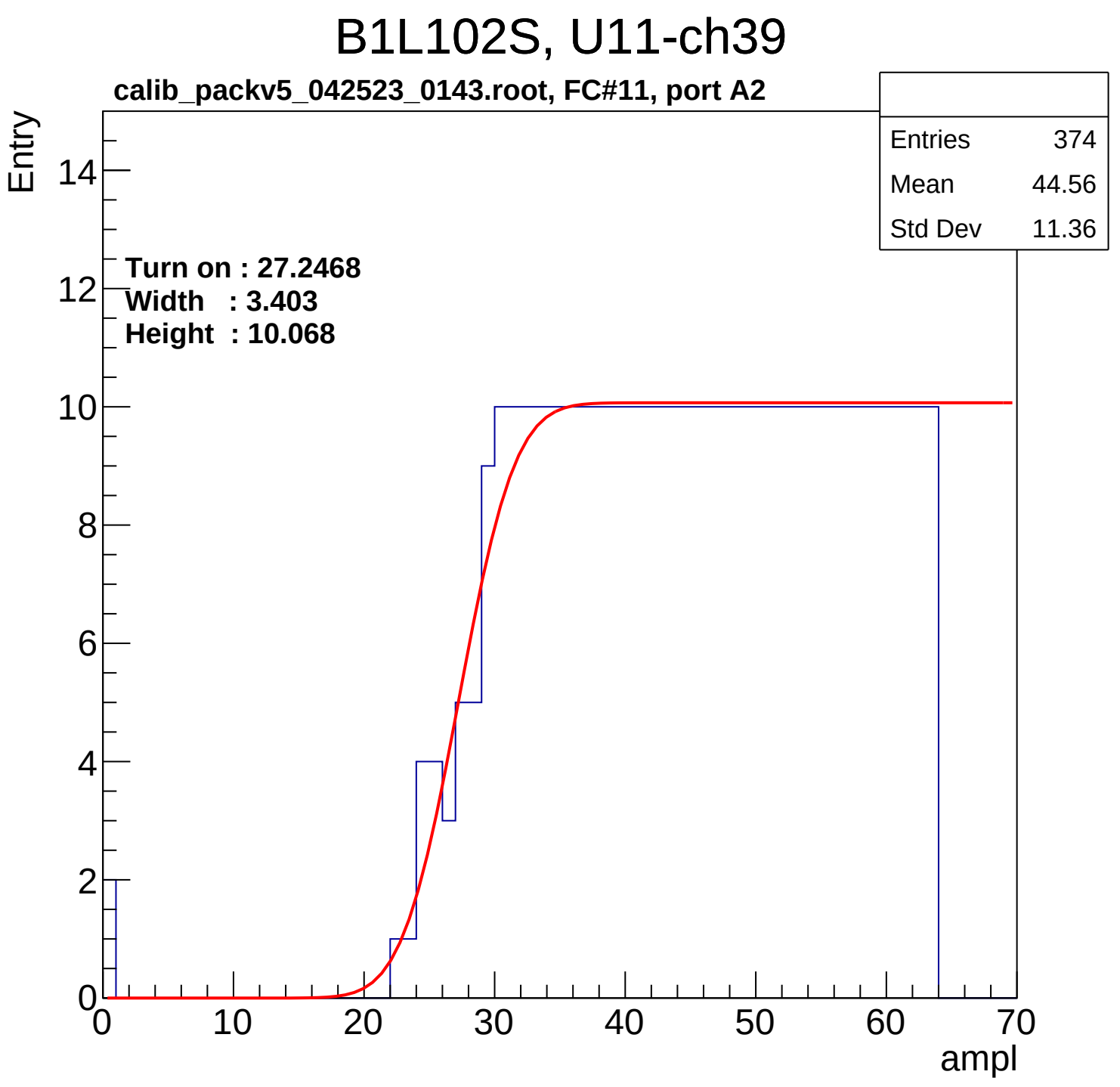
B1L102S, U11-ch39
calib_packv5_042523_0143.root, FC#11, port A2
Entries 374
Mean 44.56
Std Dev 11.36
Turn on : 27.2468
Width : 3.403
Height : 10.068
Entry
ampl
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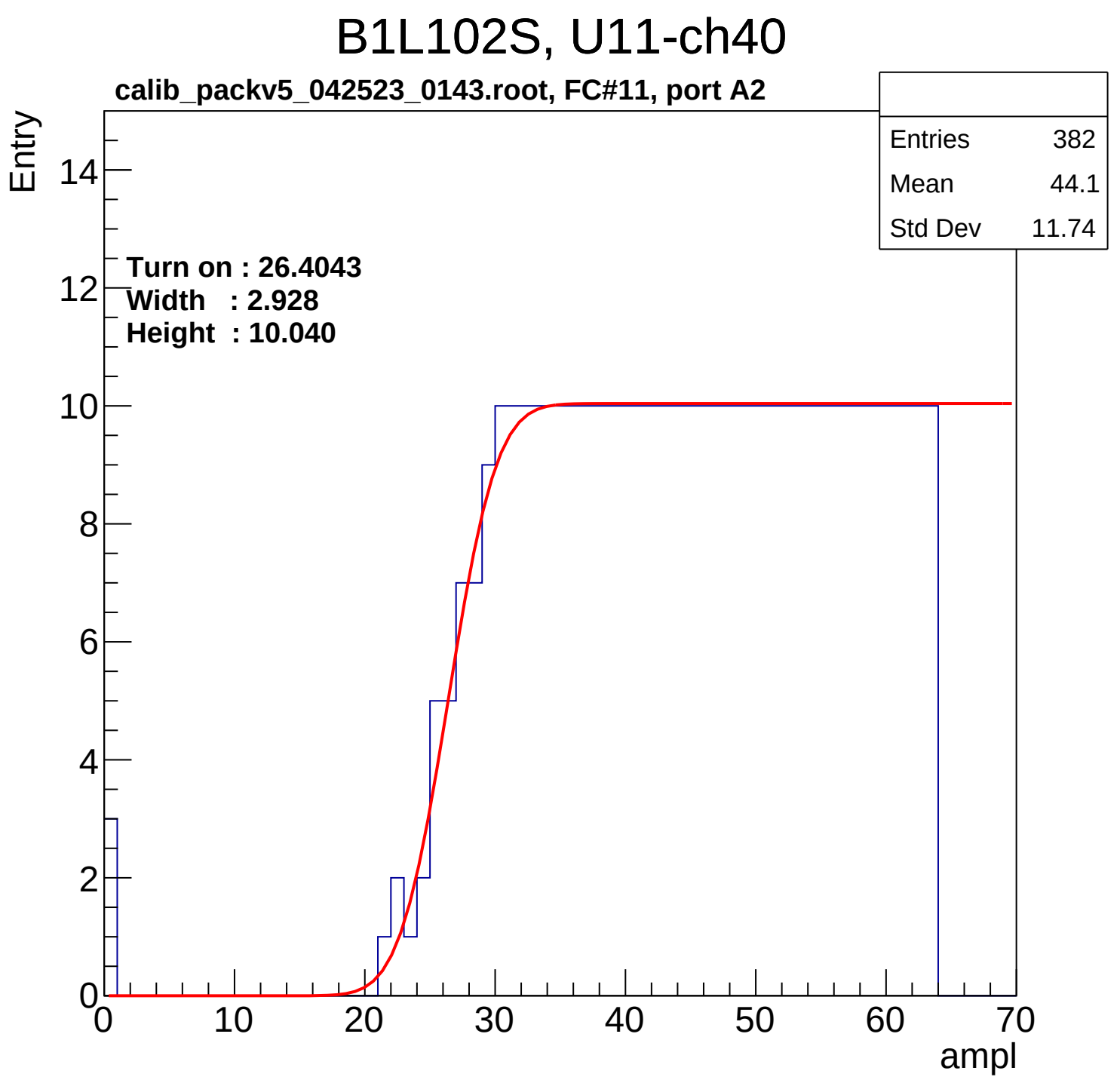
B1L102S, U11-ch40
calib_packv5_042523_0143.root, FC#11, port A2
Entries 382
Mean 44.1
Std Dev 11.74
Turn on : 26.4043
Width : 2.928
Height : 10.040
Entry
ampl
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6
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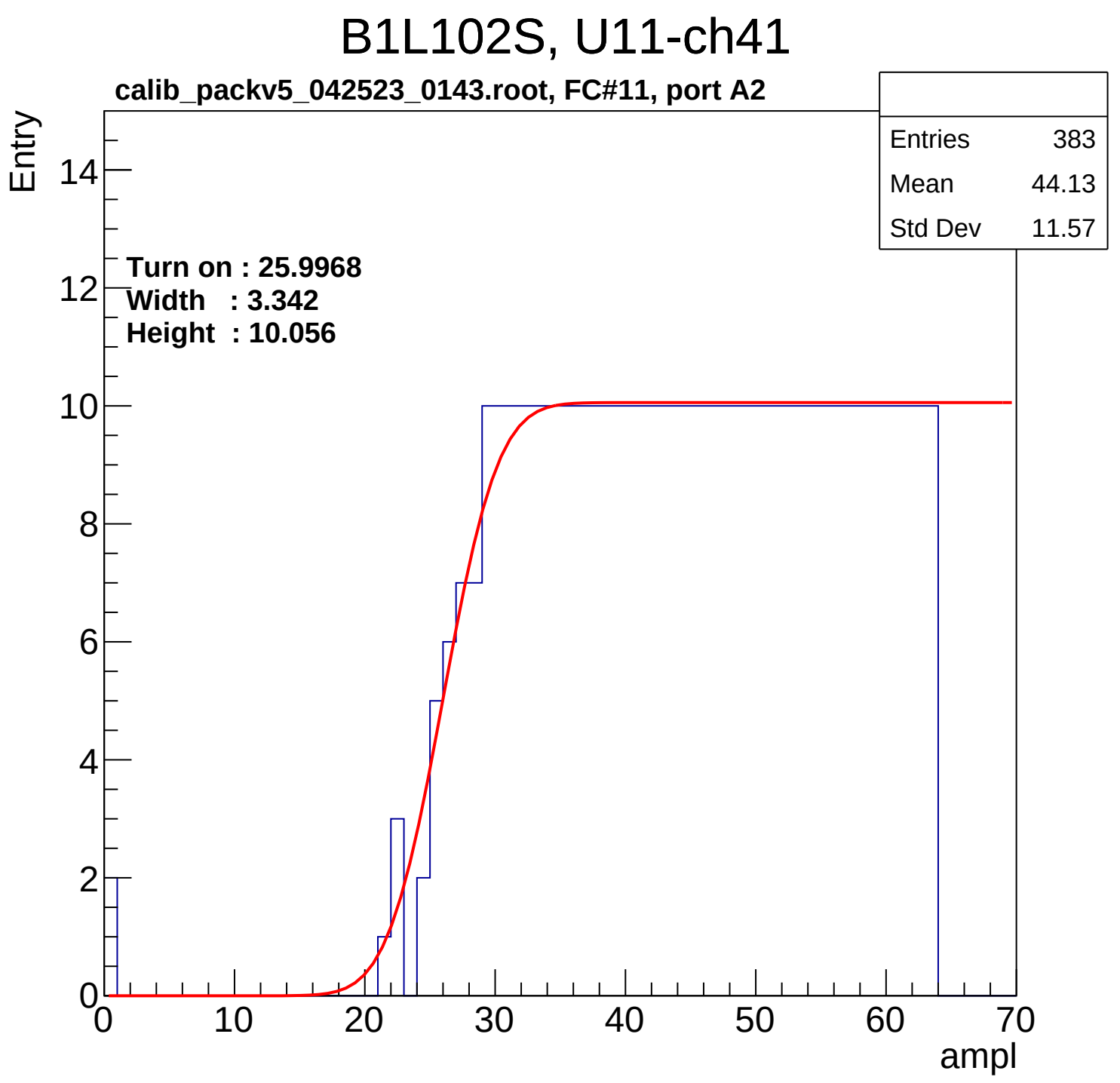
B1L102S, U11-ch41
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 44.13
Std Dev 11.57
Turn on : 25.9968
Width : 3.342
Height : 10.056
Entry
ampl
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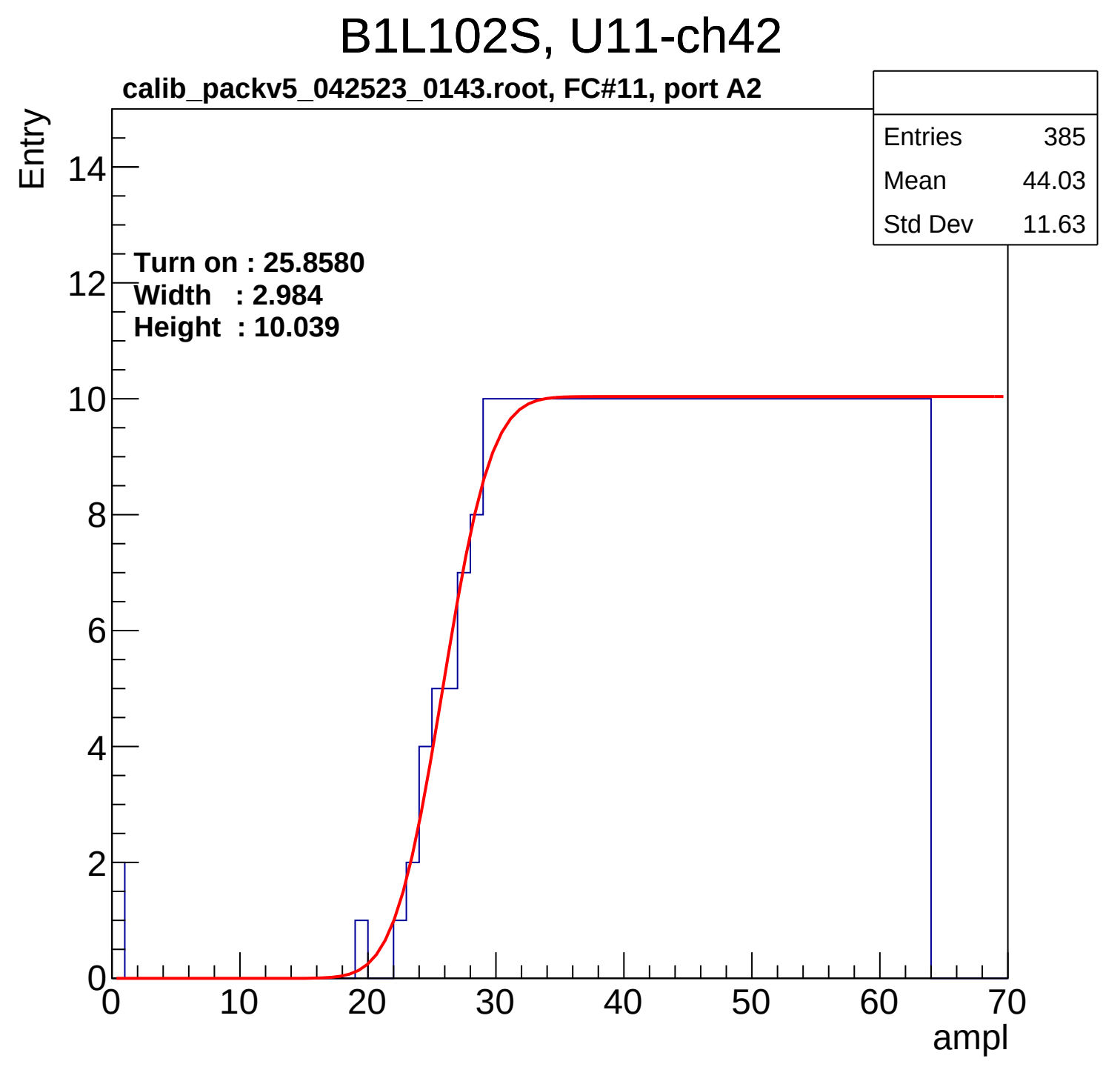
B1L102S, U11-ch42
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 44.03
Std Dev 11.63
Turn on : 25.8580
Width : 2.984
Height : 10.039
Entry
ampl
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6
8
10
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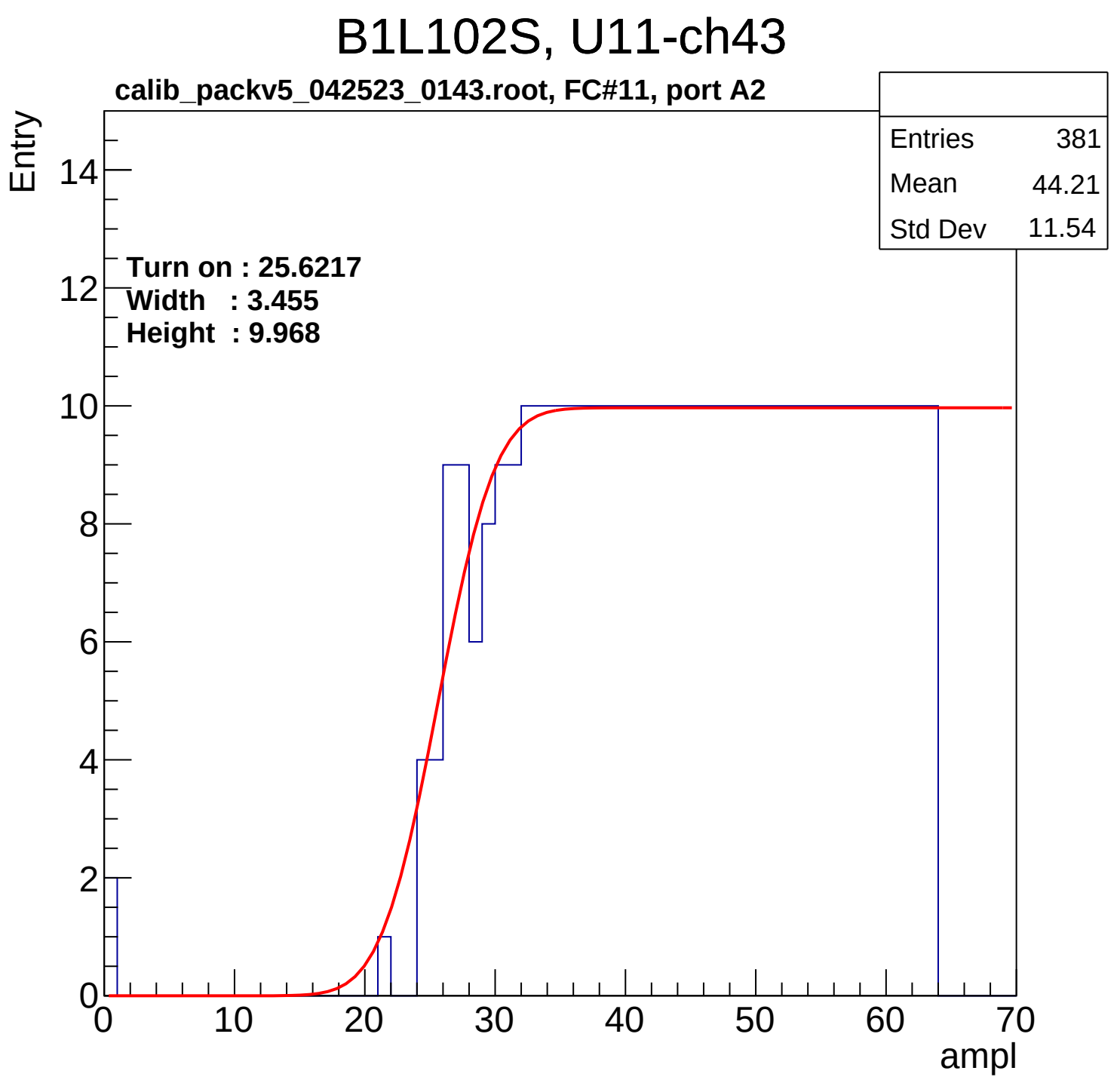
B1L102S, U11-ch43
calib_packv5_042523_0143.root, FC#11, port A2
Entries 381
Mean 44.21
Std Dev 11.54
Turn on : 25.6217
Width : 3.455
Height : 9.968
Entry
ampl
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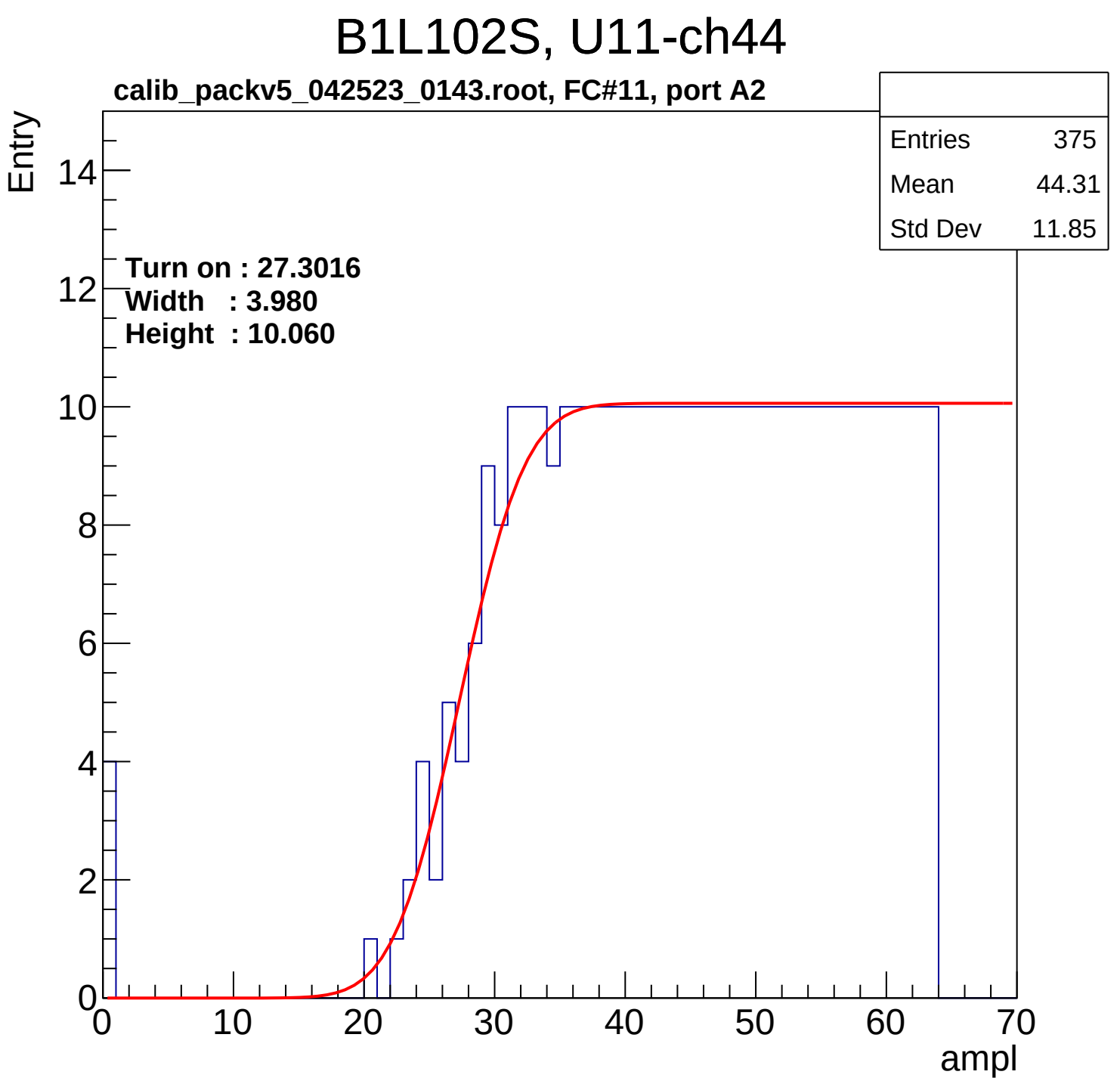
B1L102S, U11-ch44
calib_packv5_042523_0143.root, FC#11, port A2
Entries 375
Mean 44.31
Std Dev 11.85
Turn on : 27.3016
Width : 3.980
Height : 10.060
Entry
ampl
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8
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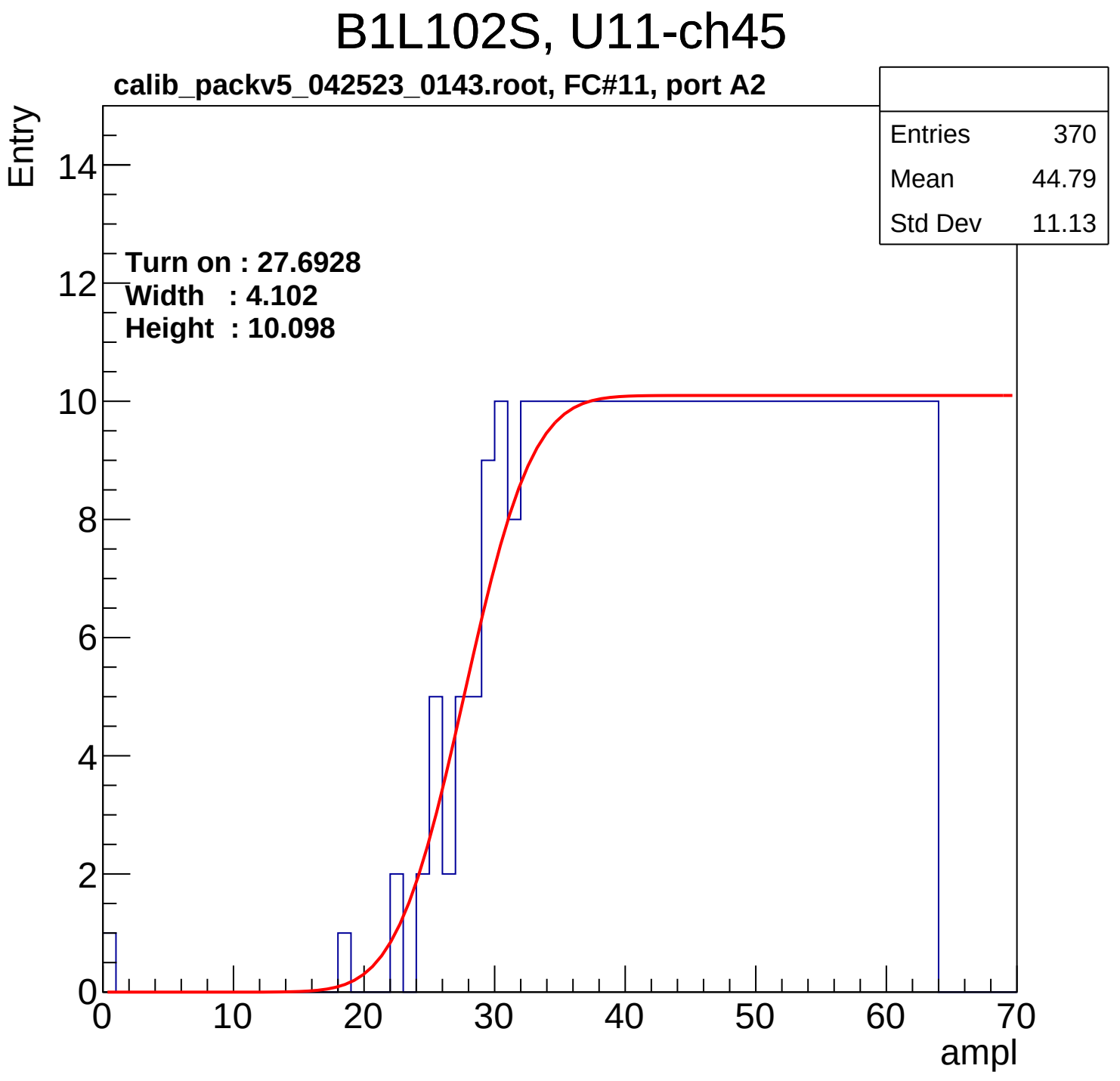
B1L102S, U11-ch45
calib_packv5_042523_0143.root, FC#11, port A2
Entries 370
Mean 44.79
Std Dev 11.13
Turn on : 27.6928
Width : 4.102
Height : 10.098
Entry
ampl
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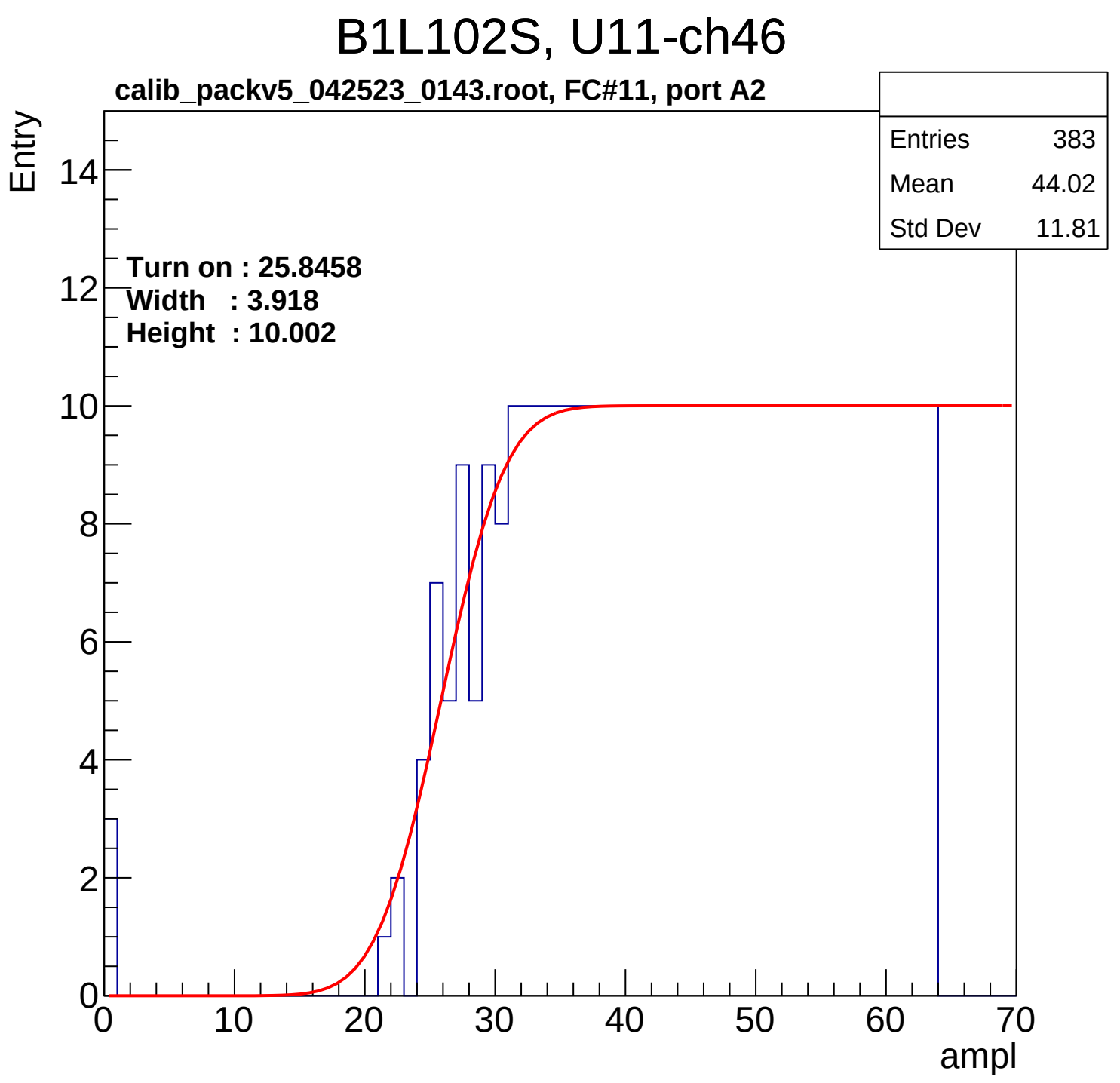
B1L102S, U11-ch46
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 44.02
Std Dev 11.81
Turn on : 25.8458
Width : 3.918
Height : 10.002
Entry
ampl
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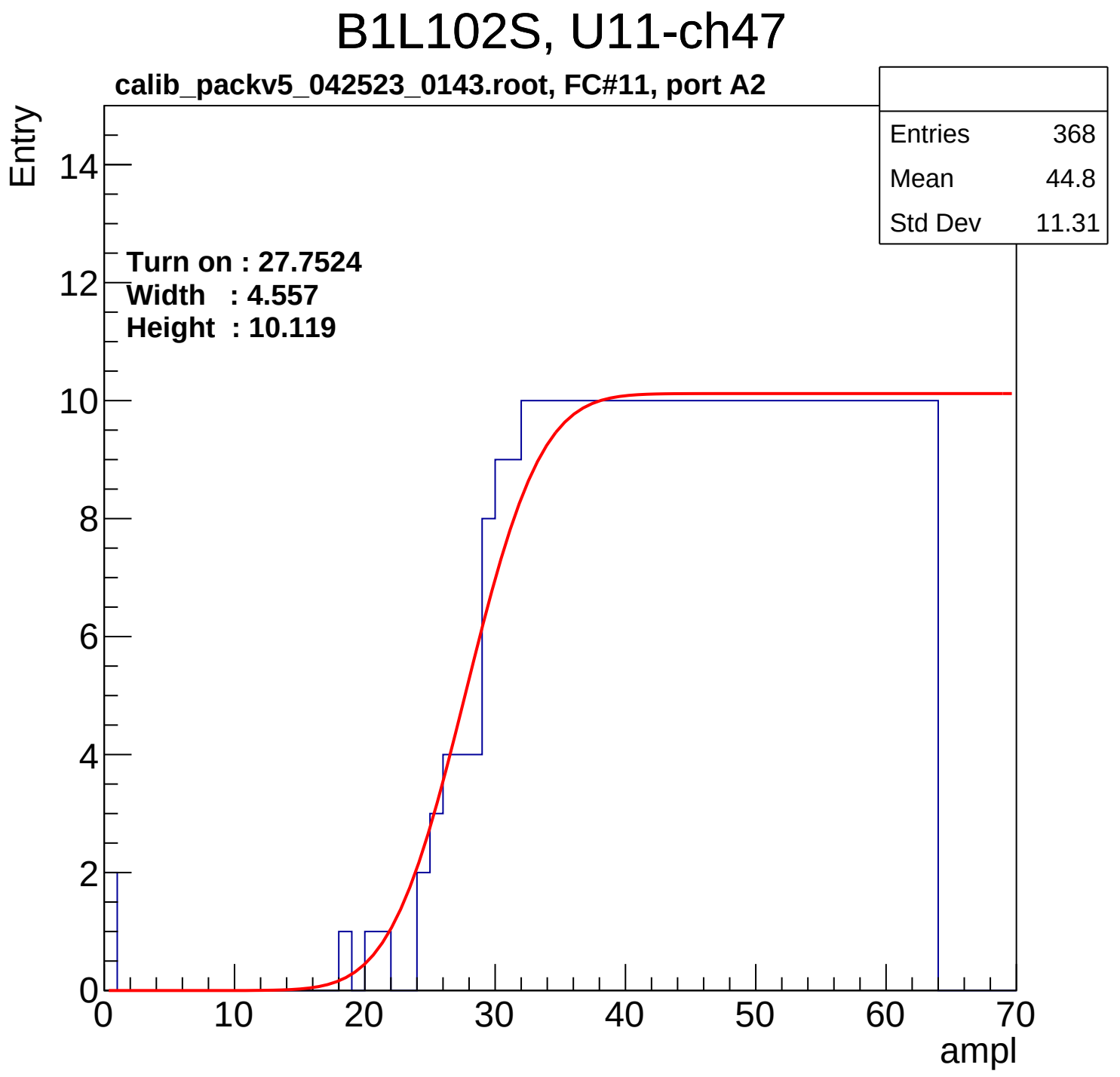
B1L102S, U11-ch47
calib_packv5_042523_0143.root, FC#11, port A2
Entries 368
Mean 44.8
Std Dev 11.31
Turn on : 27.7524
Width : 4.557
Height : 10.119
Entry
ampl
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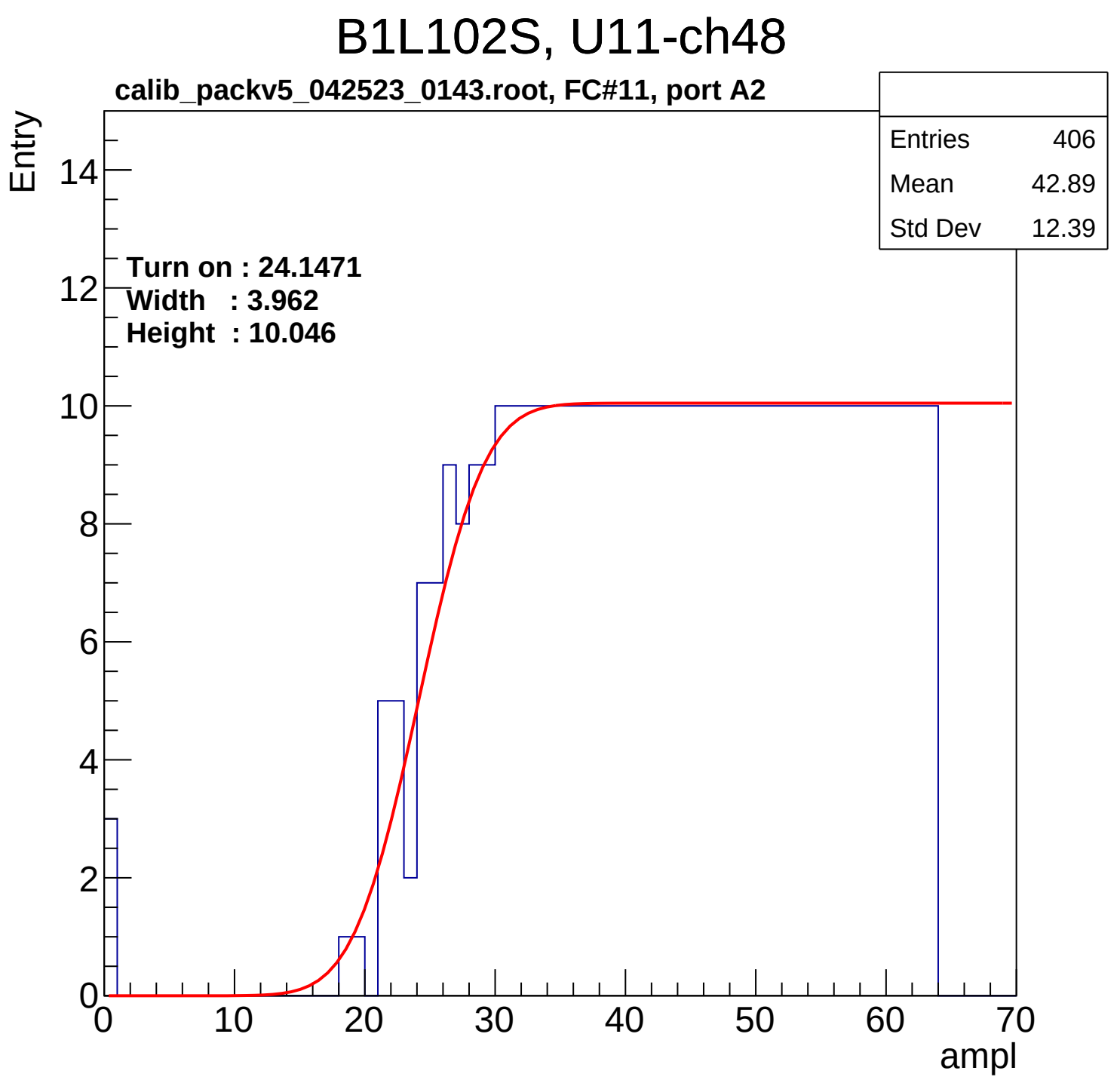
B1L102S, U11-ch48
calib_packv5_042523_0143.root, FC#11, port A2
Entries 406
Mean 42.89
Std Dev 12.39
Turn on : 24.1471
Width : 3.962
Height : 10.046
Entry
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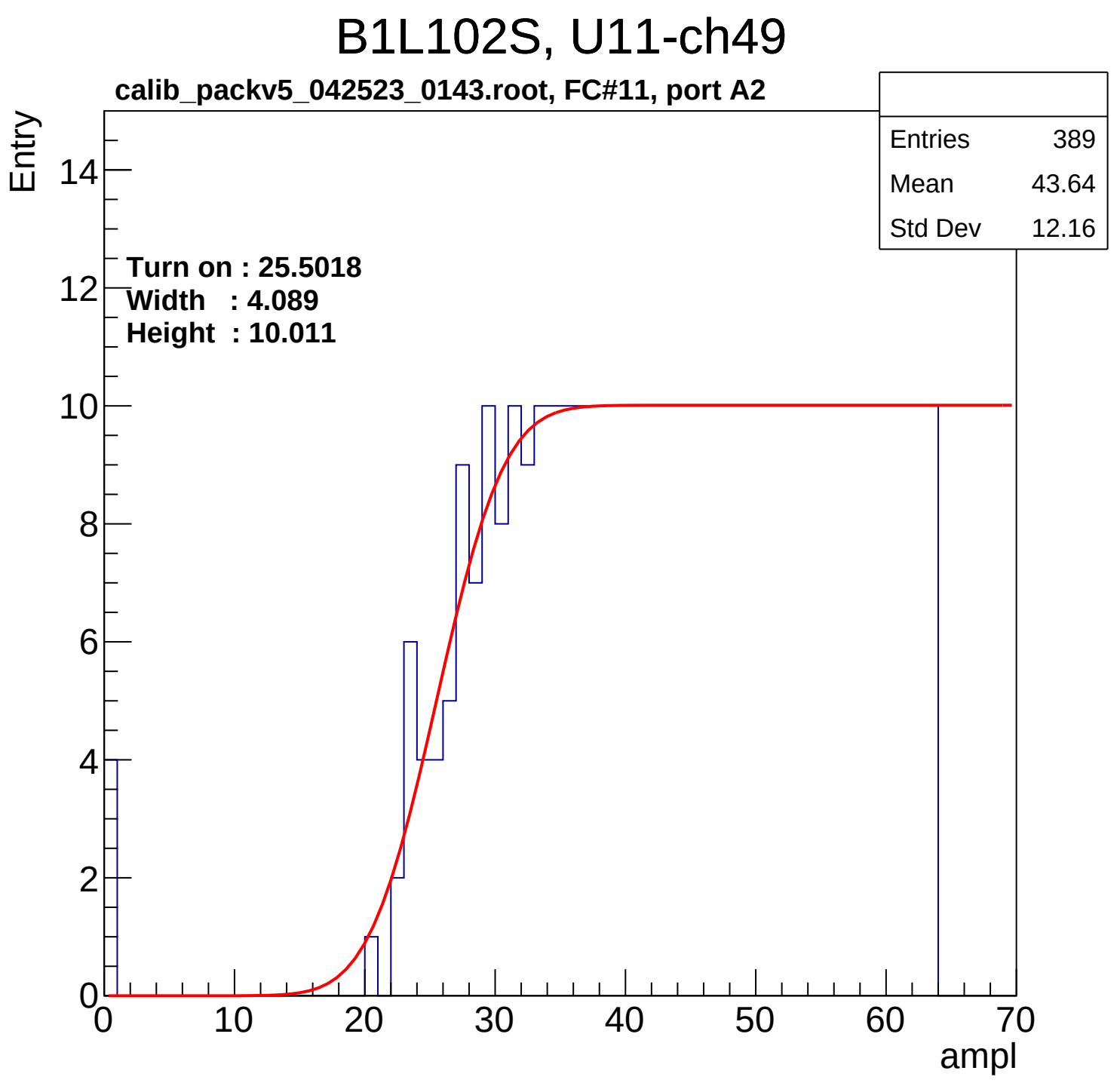
B1L102S, U11-ch49
calib_packv5_042523_0143.root, FC#11, port A2
Entries 389
Mean 43.64
Std Dev 12.16
Turn on : 25.5018
Width : 4.089
Height : 10.011
Entry
ampl
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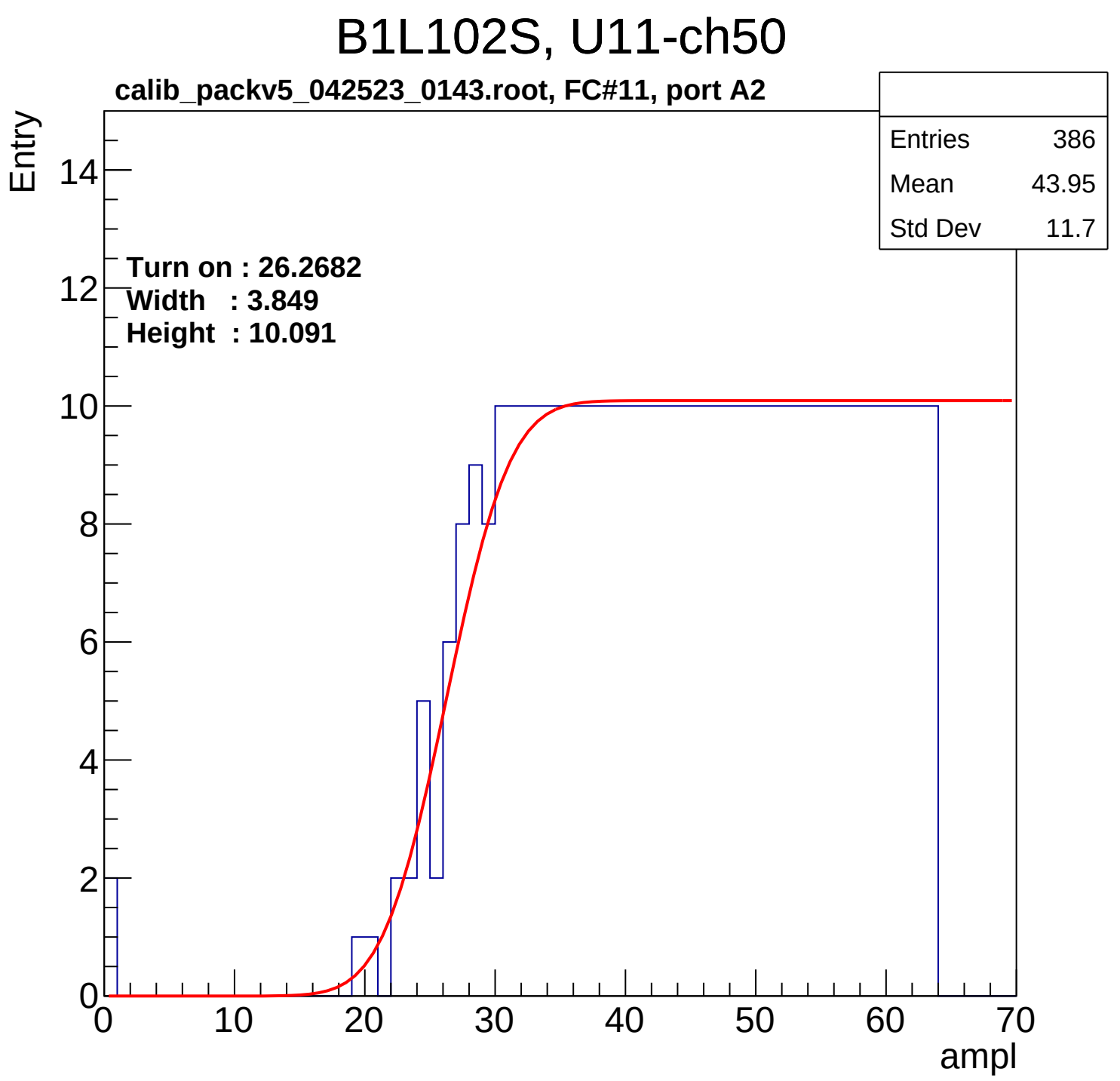
B1L102S, U11-ch50
calib_packv5_042523_0143.root, FC#11, port A2
Entries 386
Mean 43.95
Std Dev 11.7
Turn on : 26.2682
Width : 3.849
Height : 10.091
Entry
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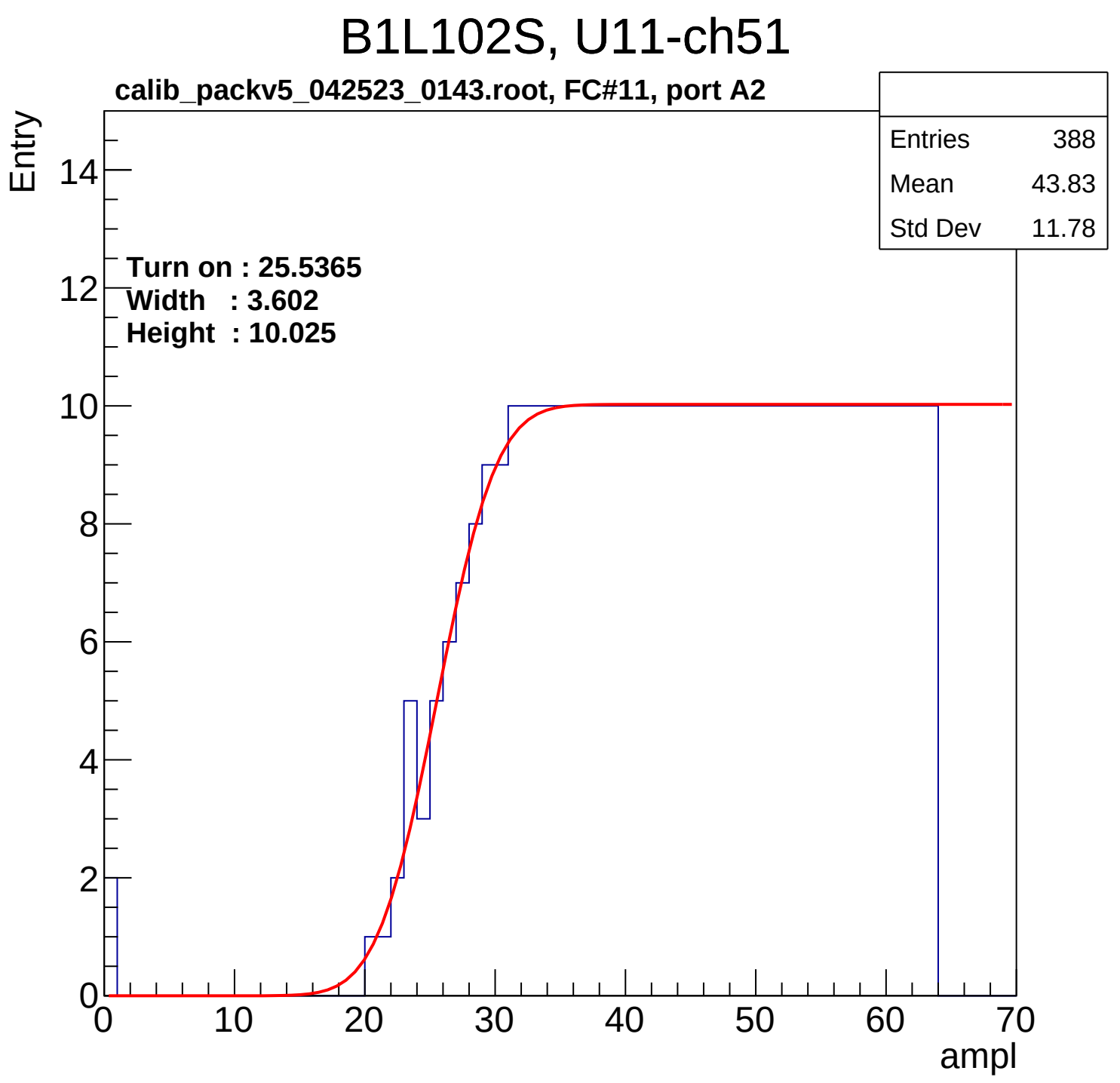
B1L102S, U11-ch51
calib_packv5_042523_0143.root, FC#11, port A2
Entries 388
Mean 43.83
Std Dev 11.78
Turn on : 25.5365
Width : 3.602
Height : 10.025
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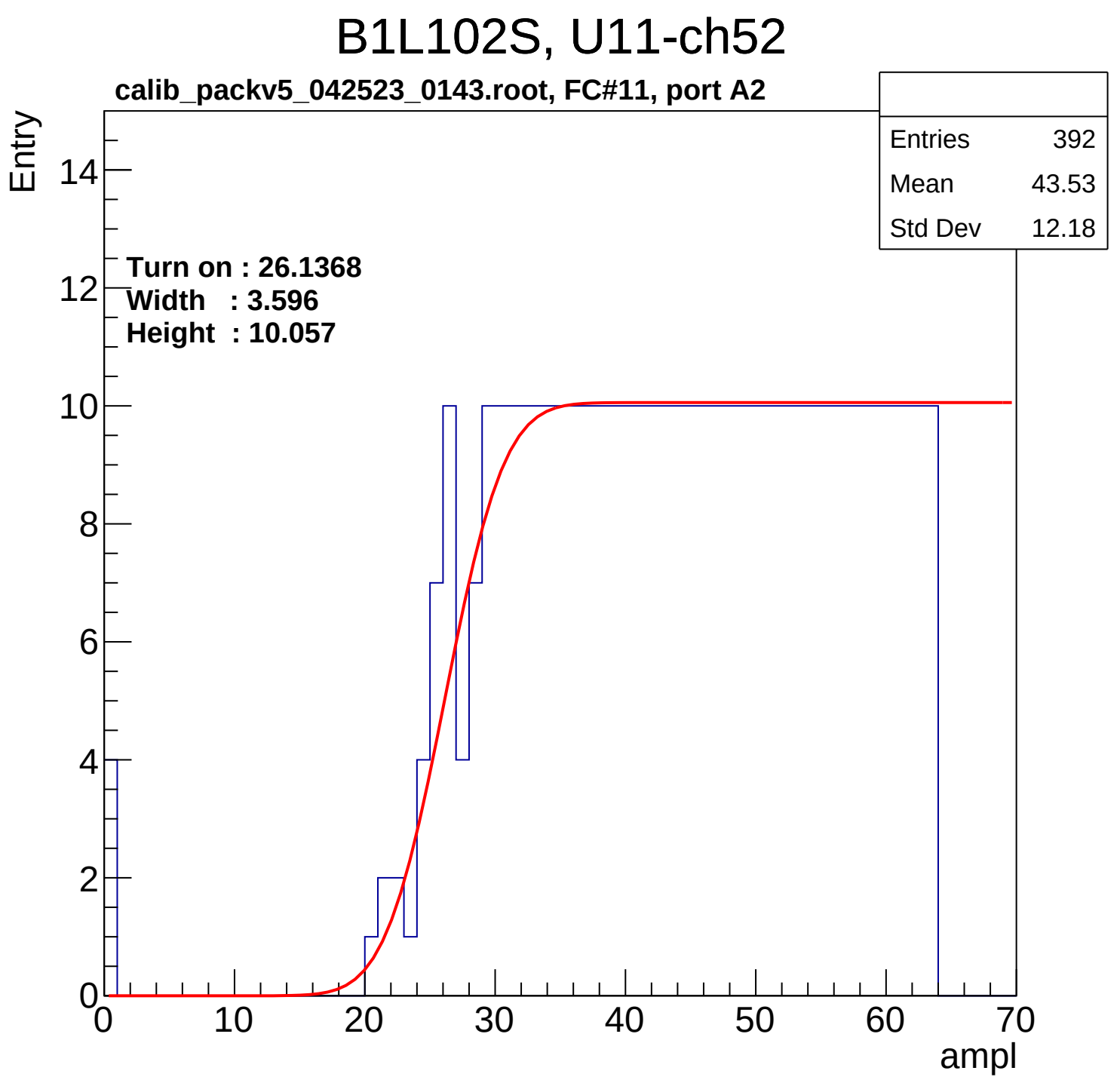
B1L102S, U11-ch52
calib_packv5_042523_0143.root, FC#11, port A2
Entries 392
Mean 43.53
Std Dev 12.18
Turn on : 26.1368
Width : 3.596
Height : 10.057
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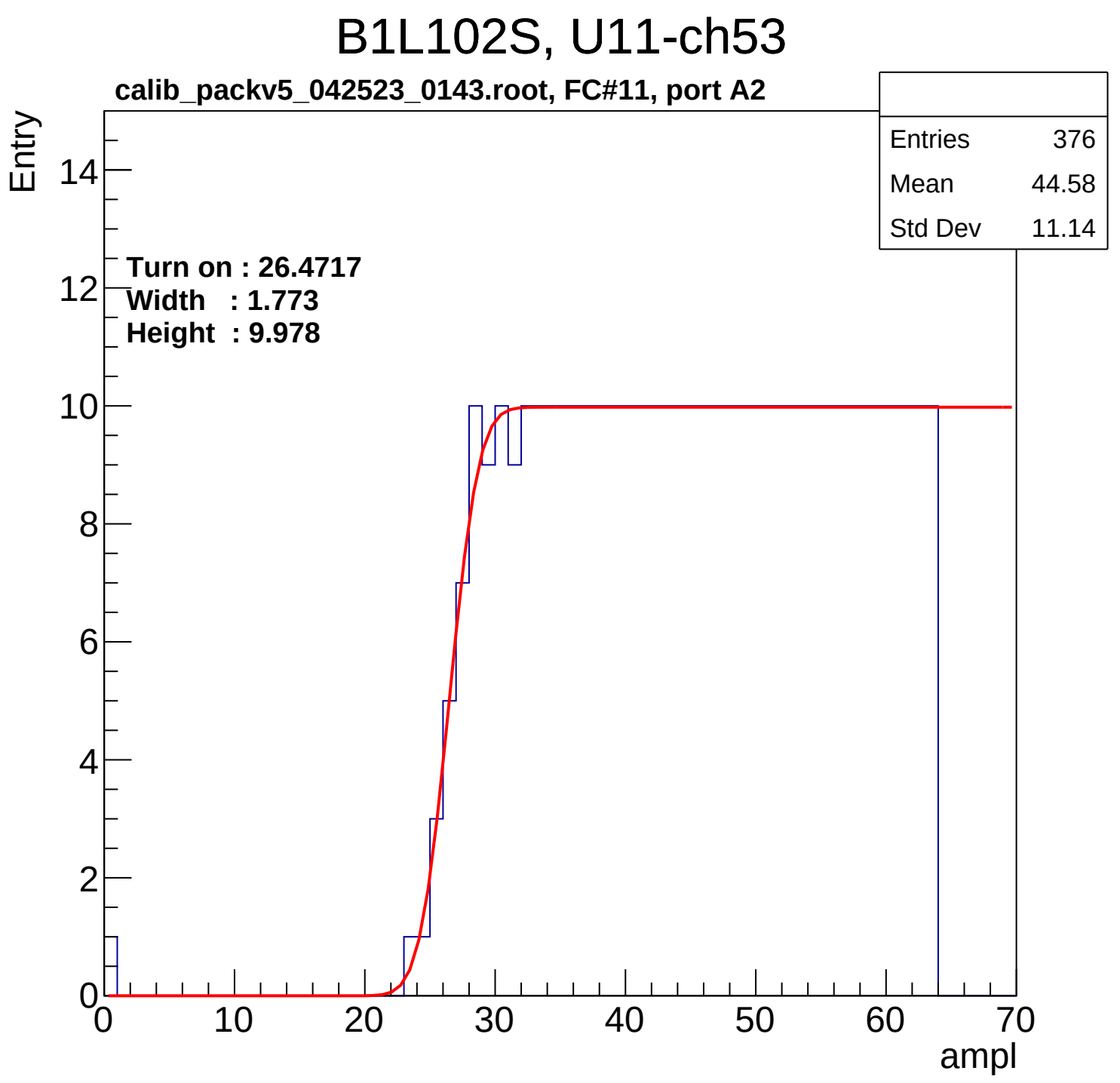
B1L102S, U11-ch53
calib_packv5_042523_0143.root, FC#11, port A2
Entries 376
Mean 44.58
Std Dev 11.14
Turn on : 26.4717
Width : 1.773
Height : 9.978
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ampl
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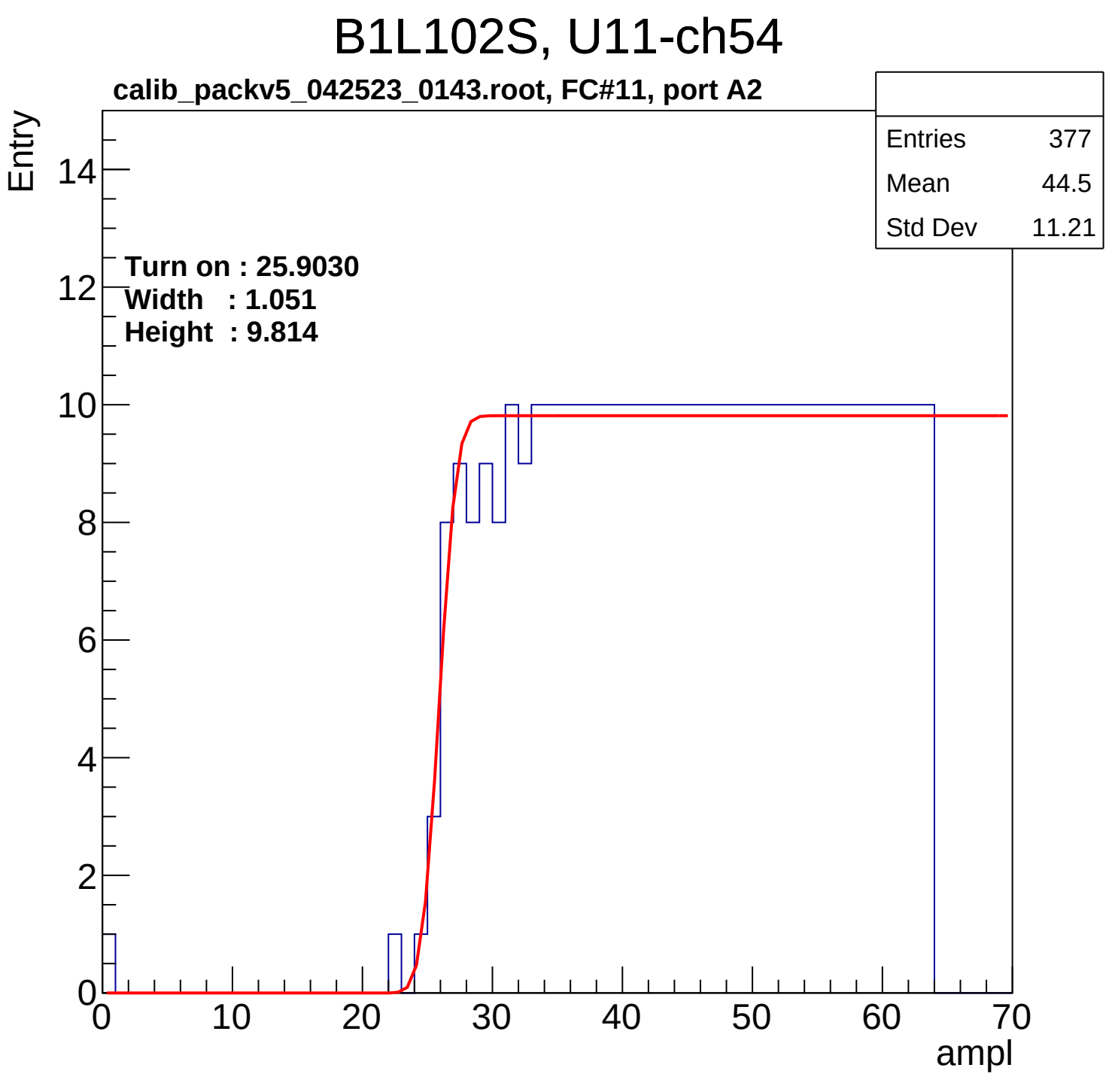
B1L102S, U11-ch54
calib_packv5_042523_0143.root, FC#11, port A2
Entries 377
Mean 44.5
Std Dev 11.21
Turn on : 25.9030
Width : 1.051
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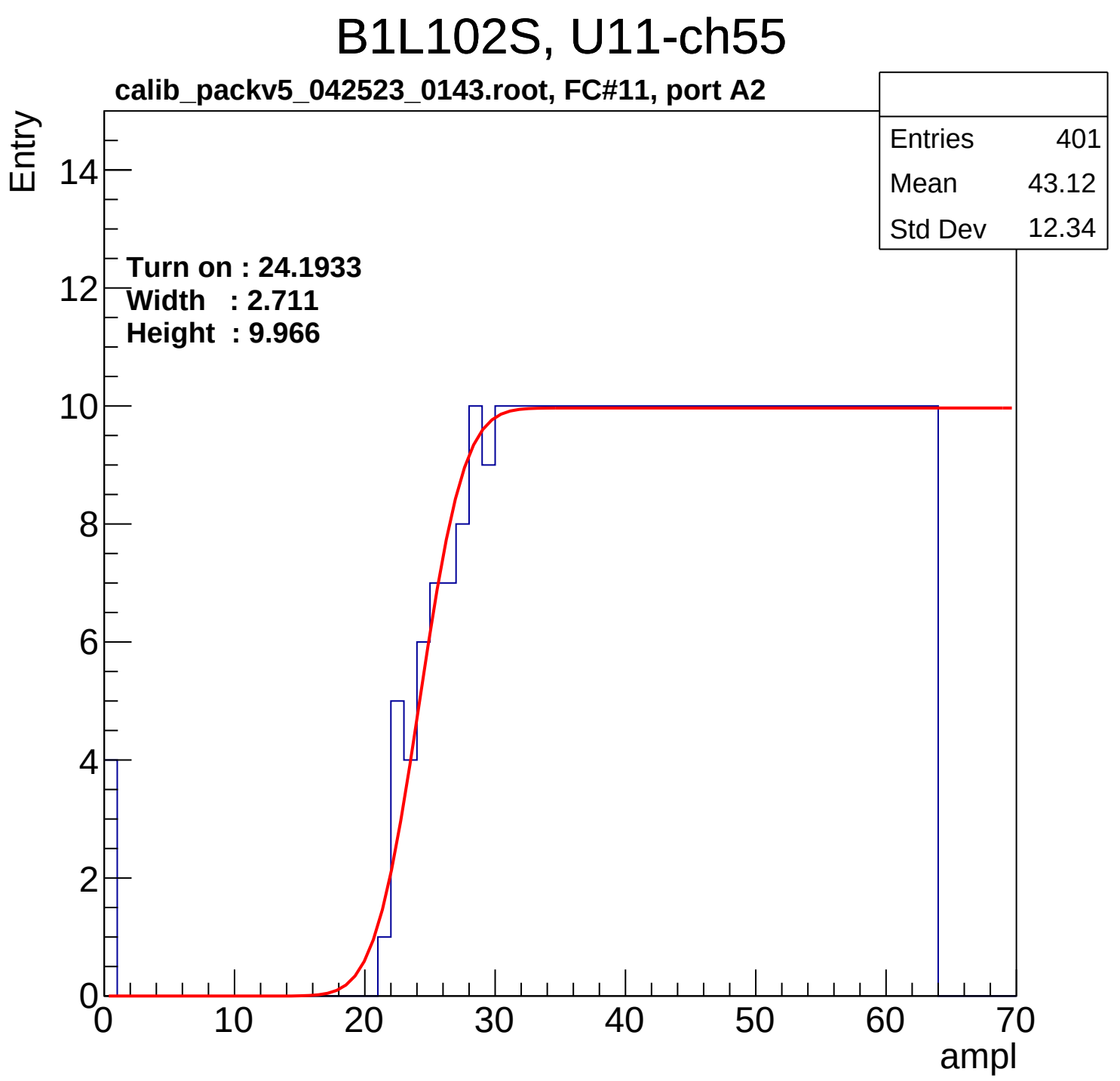
B1L102S, U11-ch55
calib_packv5_042523_0143.root, FC#11, port A2
Entries 401
Mean 43.12
Std Dev 12.34
Turn on : 24.1933
Width : 2.711
Height : 9.966
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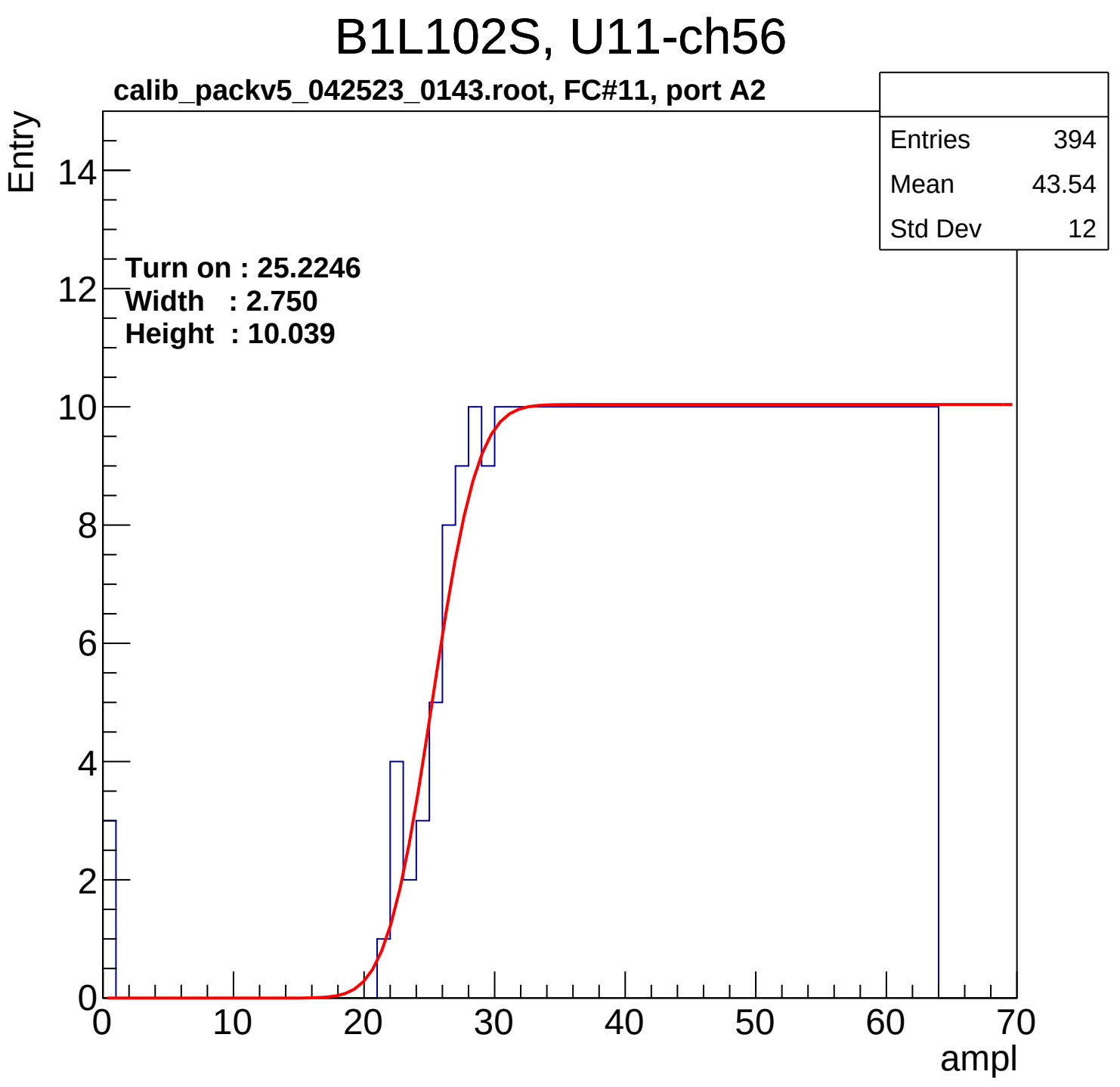
B1L102S, U11-ch56
calib_packv5_042523_0143.root, FC#11, port A2
Entries 394
Mean 43.54
Std Dev 12
Turn on : 25.2246
Width : 2.750
Height : 10.039
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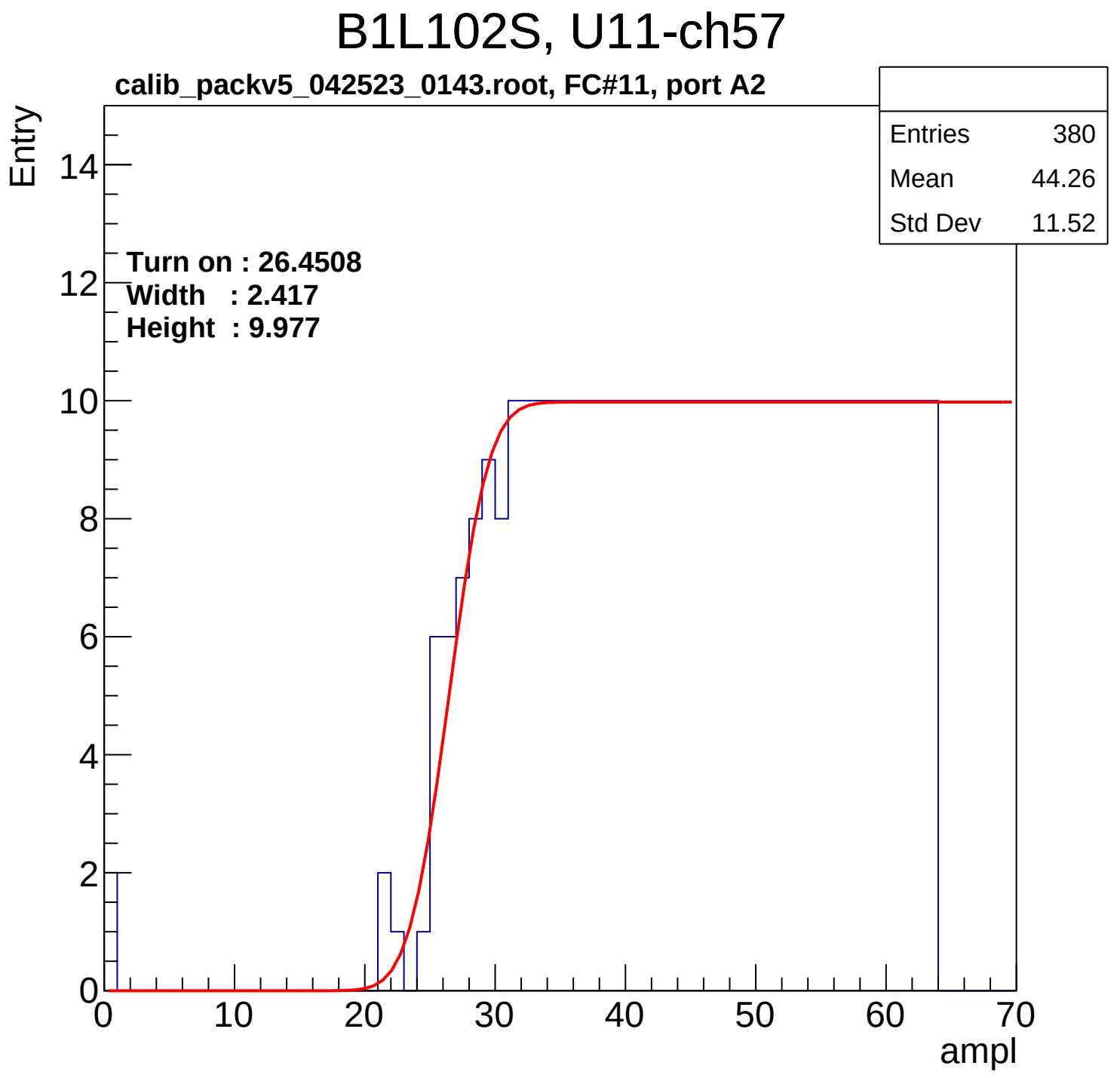
B1L102S, U11-ch57
calib_packv5_042523_0143.root, FC#11, port A2
Entries 380
Mean 44.26
Std Dev 11.52
Turn on : 26.4508
Width : 2.417
Height : 9.977
Entry
ampl
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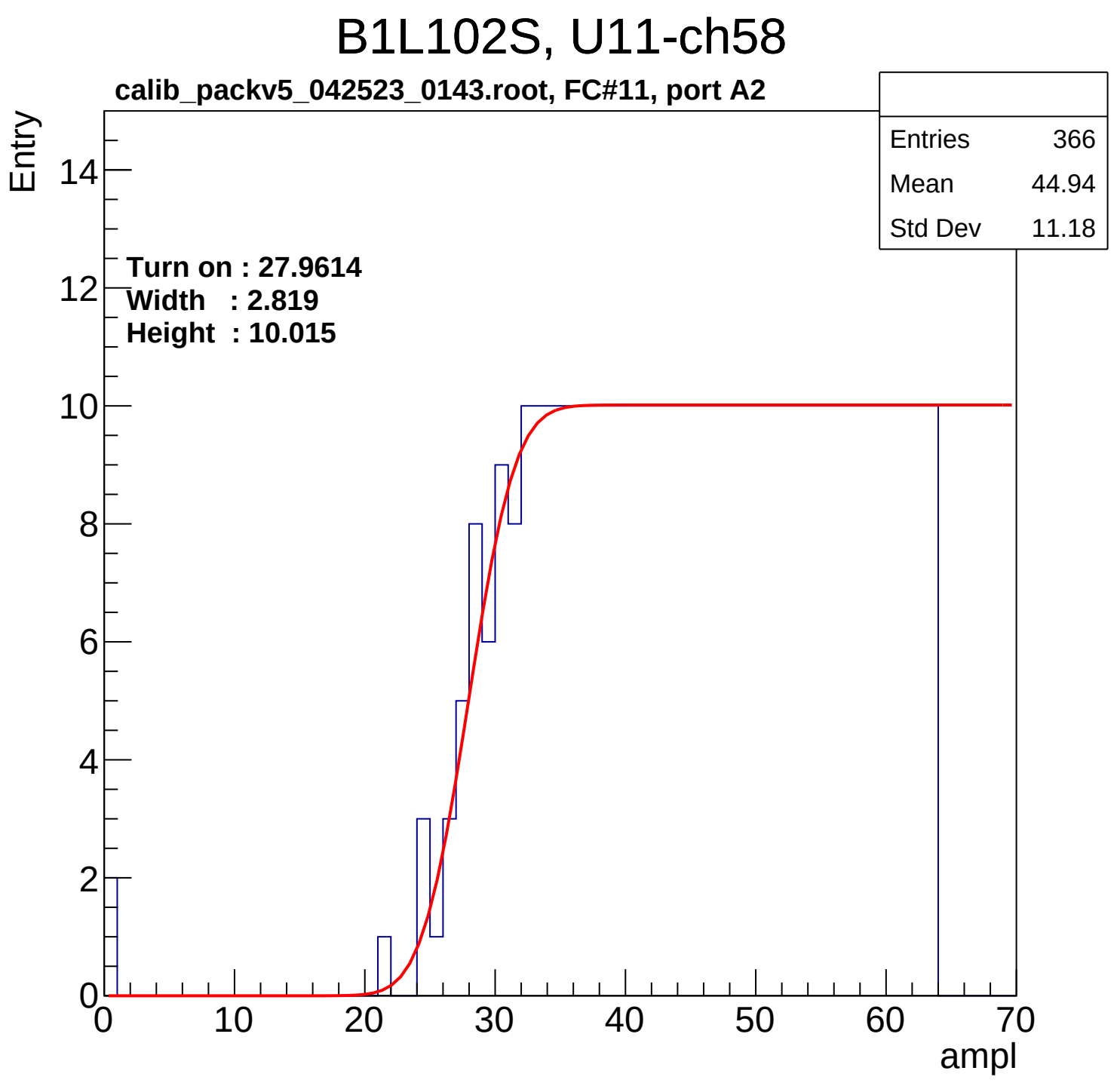
B1L102S, U11-ch58
calib_packv5_042523_0143.root, FC#11, port A2
Entries 366
Mean 44.94
Std Dev 11.18
Turn on : 27.9614
Width : 2.819
Height : 10.015
Entry
ampl
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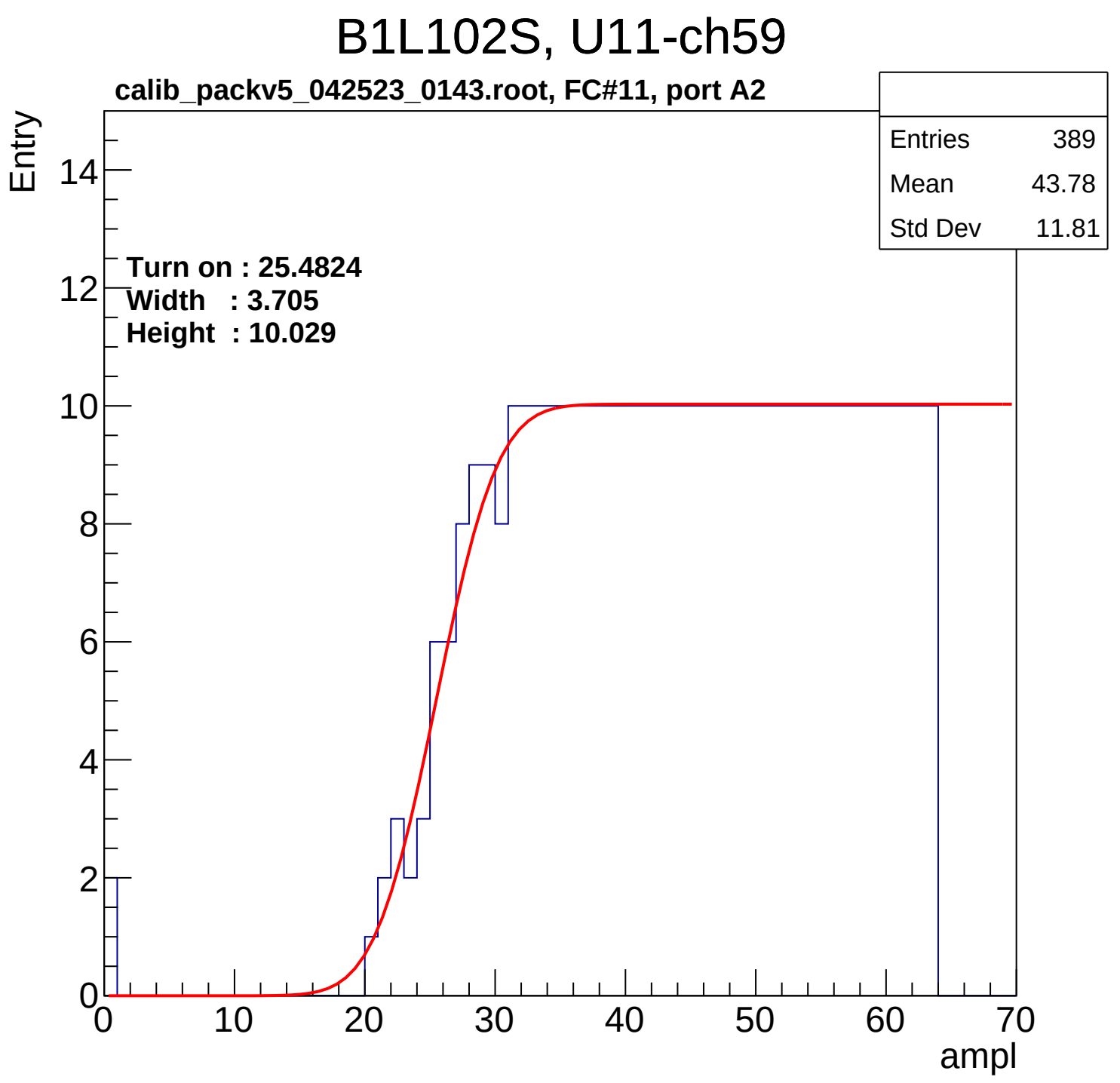
B1L102S, U11-ch59
calib_packv5_042523_0143.root, FC#11, port A2
Entries 389
Mean 43.78
Std Dev 11.81
Turn on : 25.4824
Width : 3.705
Height : 10.029
Entry
ampl
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2
4
6
8
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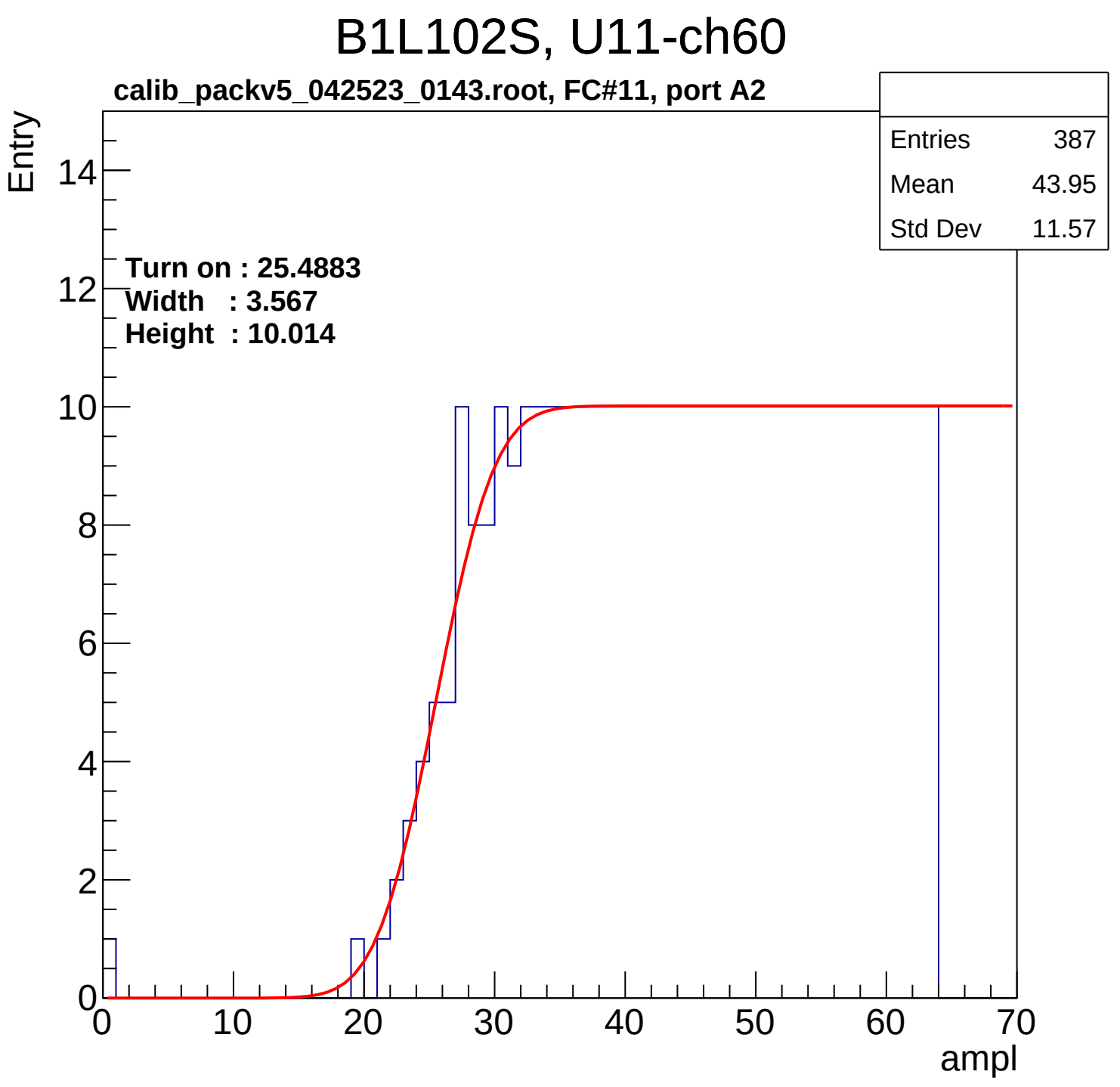
B1L102S, U11-ch60
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 43.95
Std Dev 11.57
Turn on : 25.4883
Width : 3.567
Height : 10.014
Entry
ampl
0
2
4
6
8
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0
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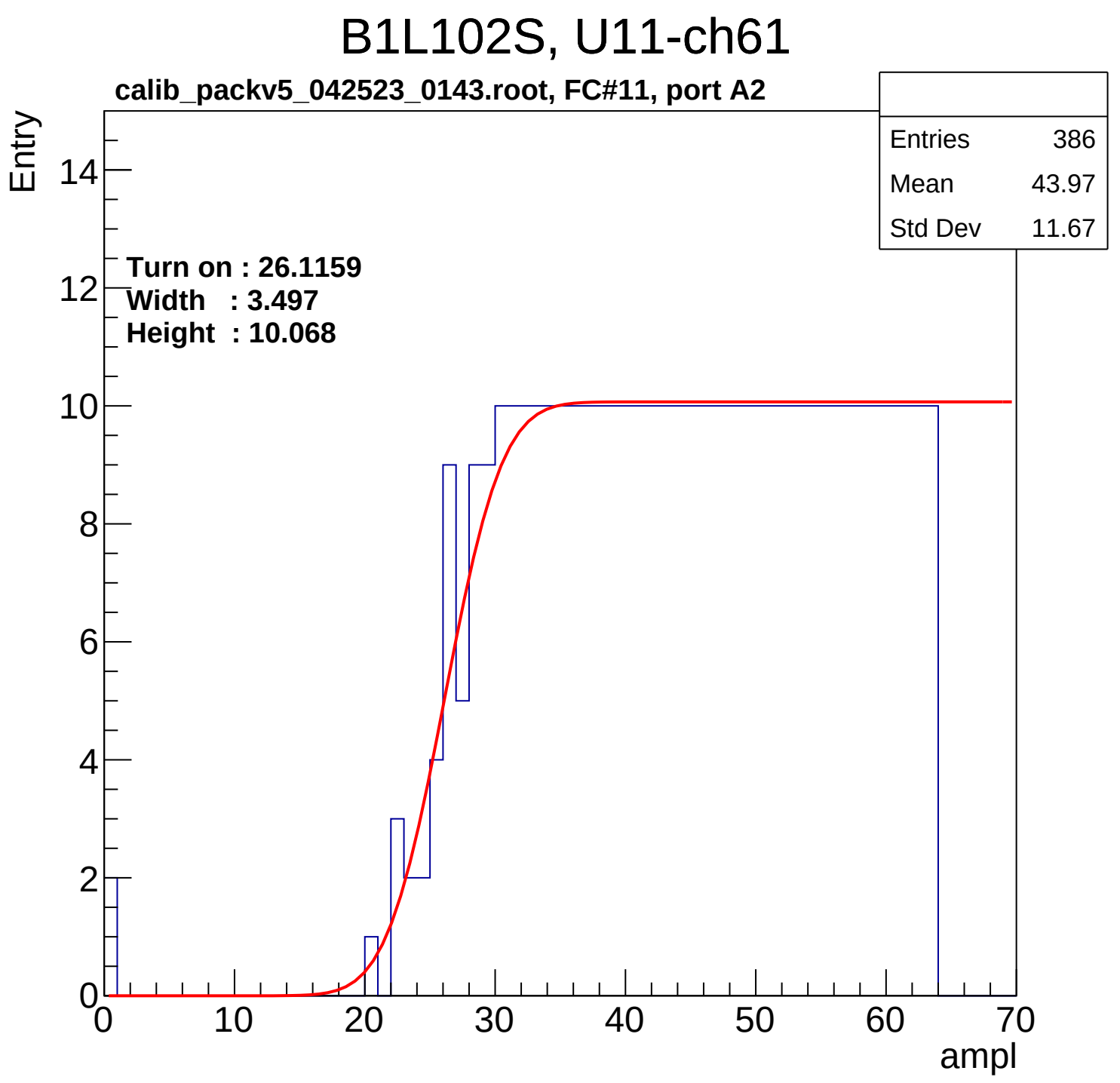
B1L102S, U11-ch61
calib_packv5_042523_0143.root, FC#11, port A2
Entries 386
Mean 43.97
Std Dev 11.67
Turn on : 26.1159
Width : 3.497
Height : 10.068
Entry
ampl
0
2
4
6
8
10
12
14
0
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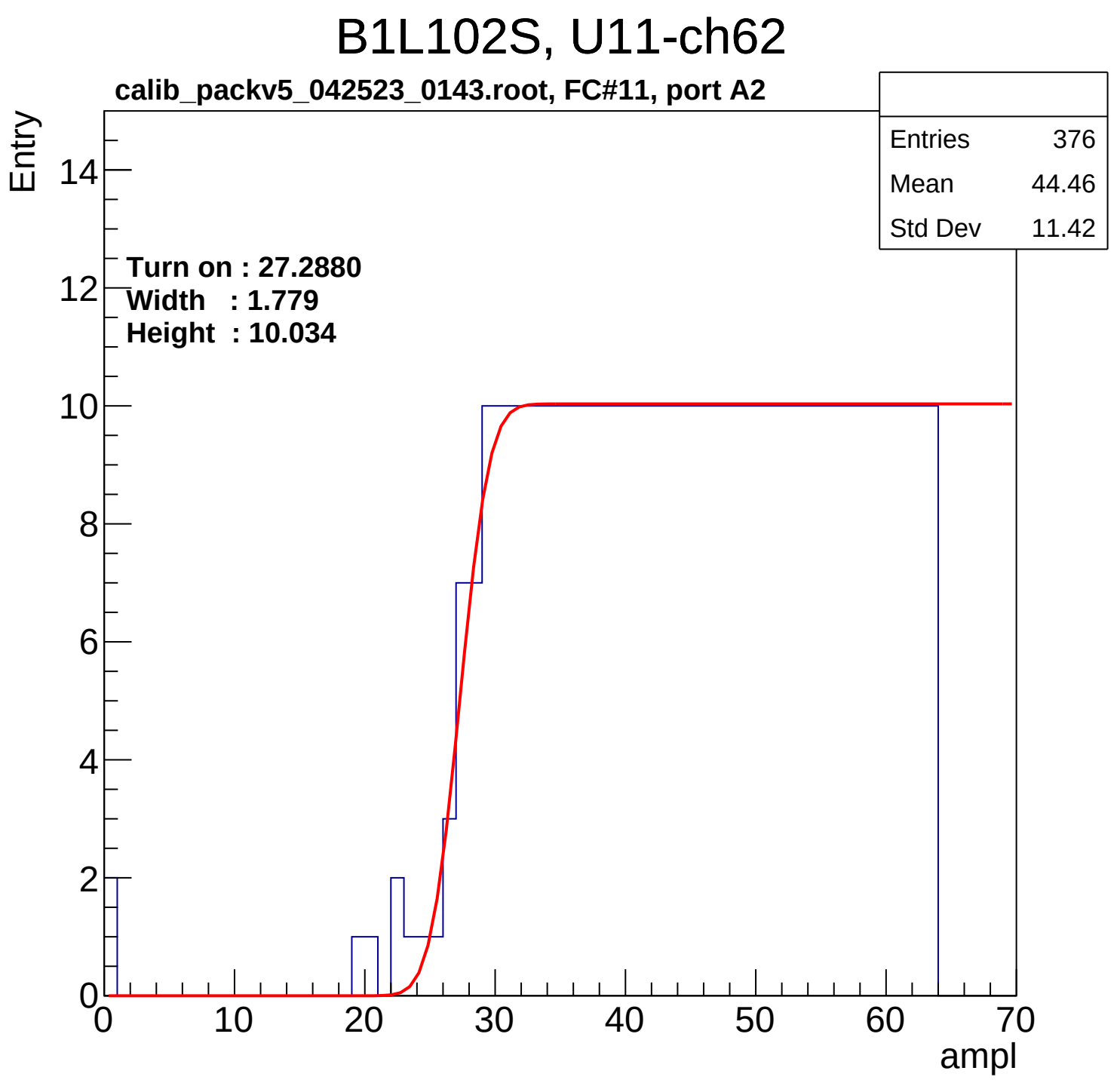
B1L102S, U11-ch62
calib_packv5_042523_0143.root, FC#11, port A2
Entries 376
Mean 44.46
Std Dev 11.42
Turn on : 27.2880
Width : 1.779
Height : 10.034
Entry
ampl
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4
6
8
10
12
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0
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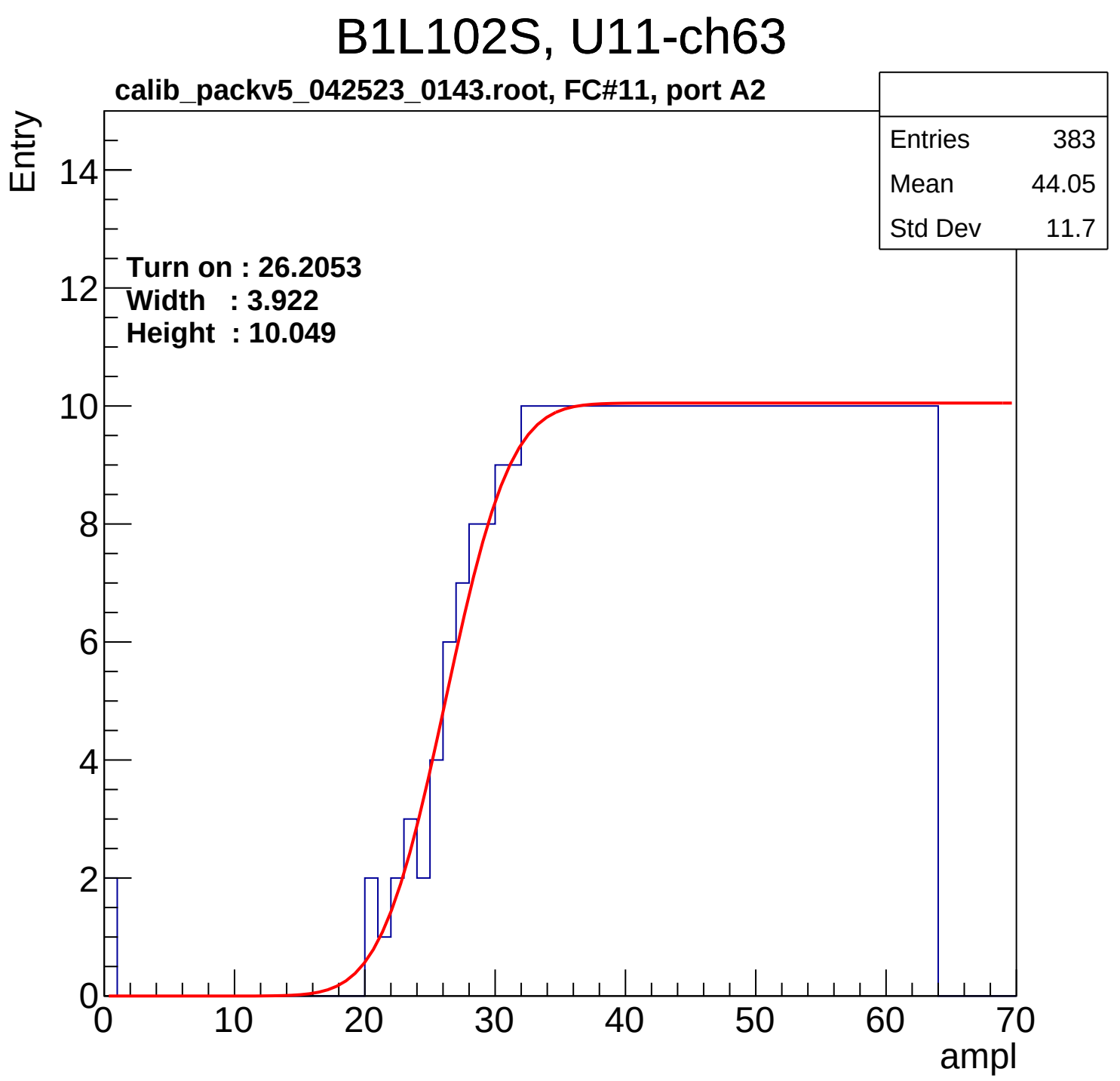
B1L102S, U11-ch63
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 44.05
Std Dev 11.7
Turn on : 26.2053
Width : 3.922
Height : 10.049
Entry
ampl
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2
4
6
8
10
12
14
0
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60
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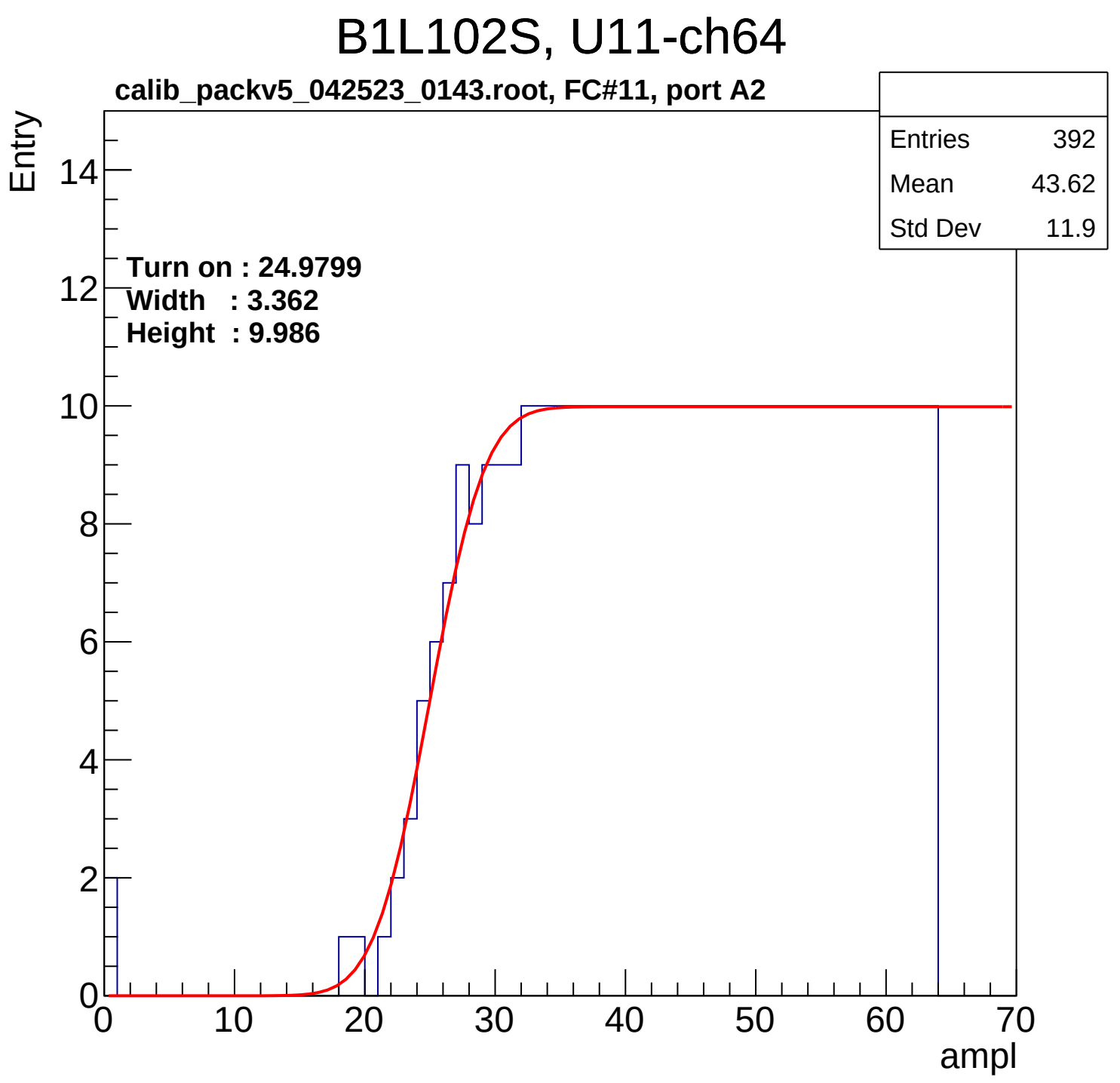
B1L102S, U11-ch64
calib_packv5_042523_0143.root, FC#11, port A2
Entries 392
Mean 43.62
Std Dev 11.9
Turn on : 24.9799
Width : 3.362
Height : 9.986
Entry
ampl
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2
4
6
8
10
12
14
0
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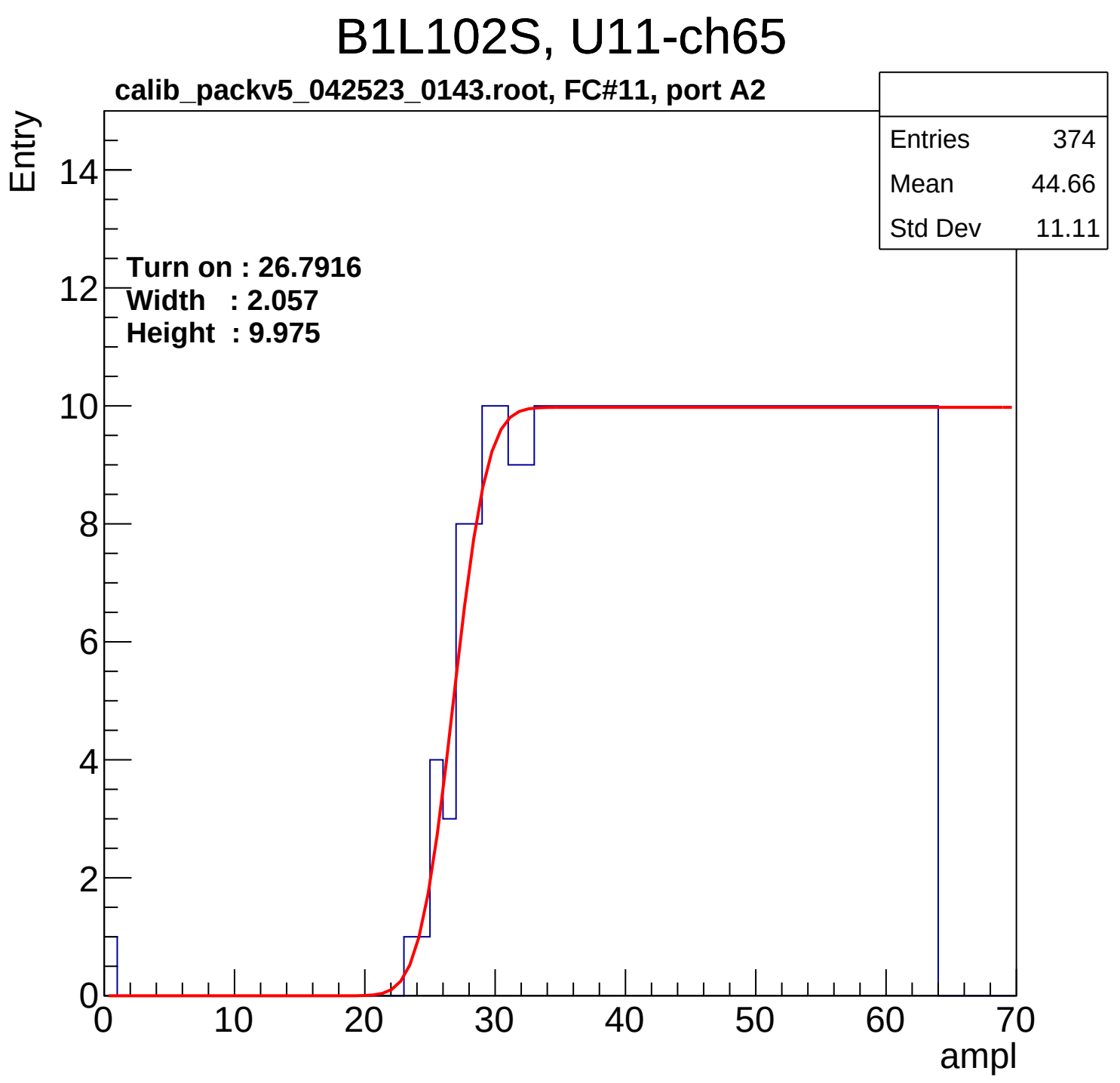
B1L102S, U11-ch65
calib_packv5_042523_0143.root, FC#11, port A2
Entries 374
Mean 44.66
Std Dev 11.11
Turn on : 26.7916
Width : 2.057
Height : 9.975
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
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60
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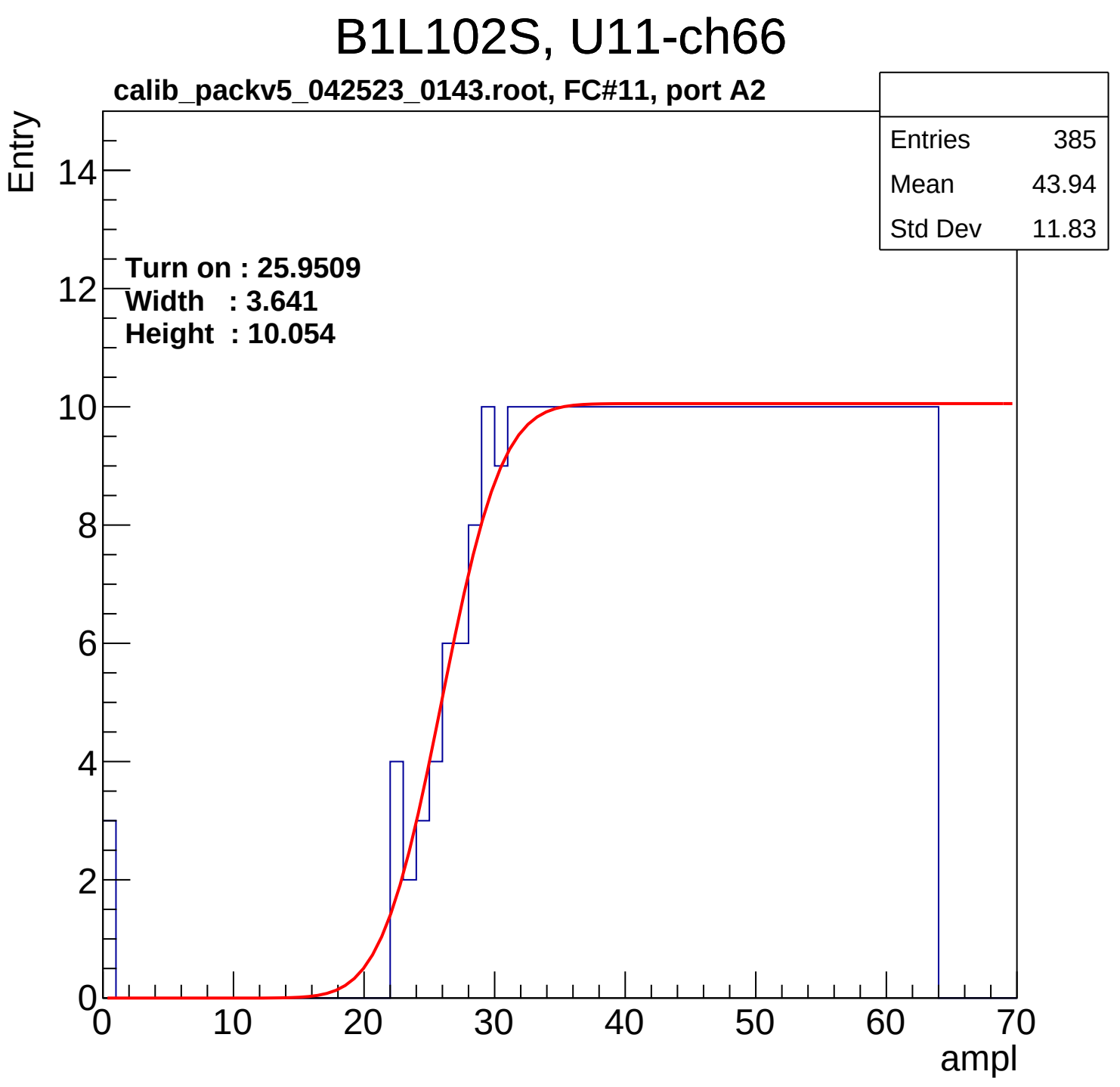
B1L102S, U11-ch66
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 43.94
Std Dev 11.83
Turn on : 25.9509
Width : 3.641
Height : 10.054
Entry
ampl
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6
8
10
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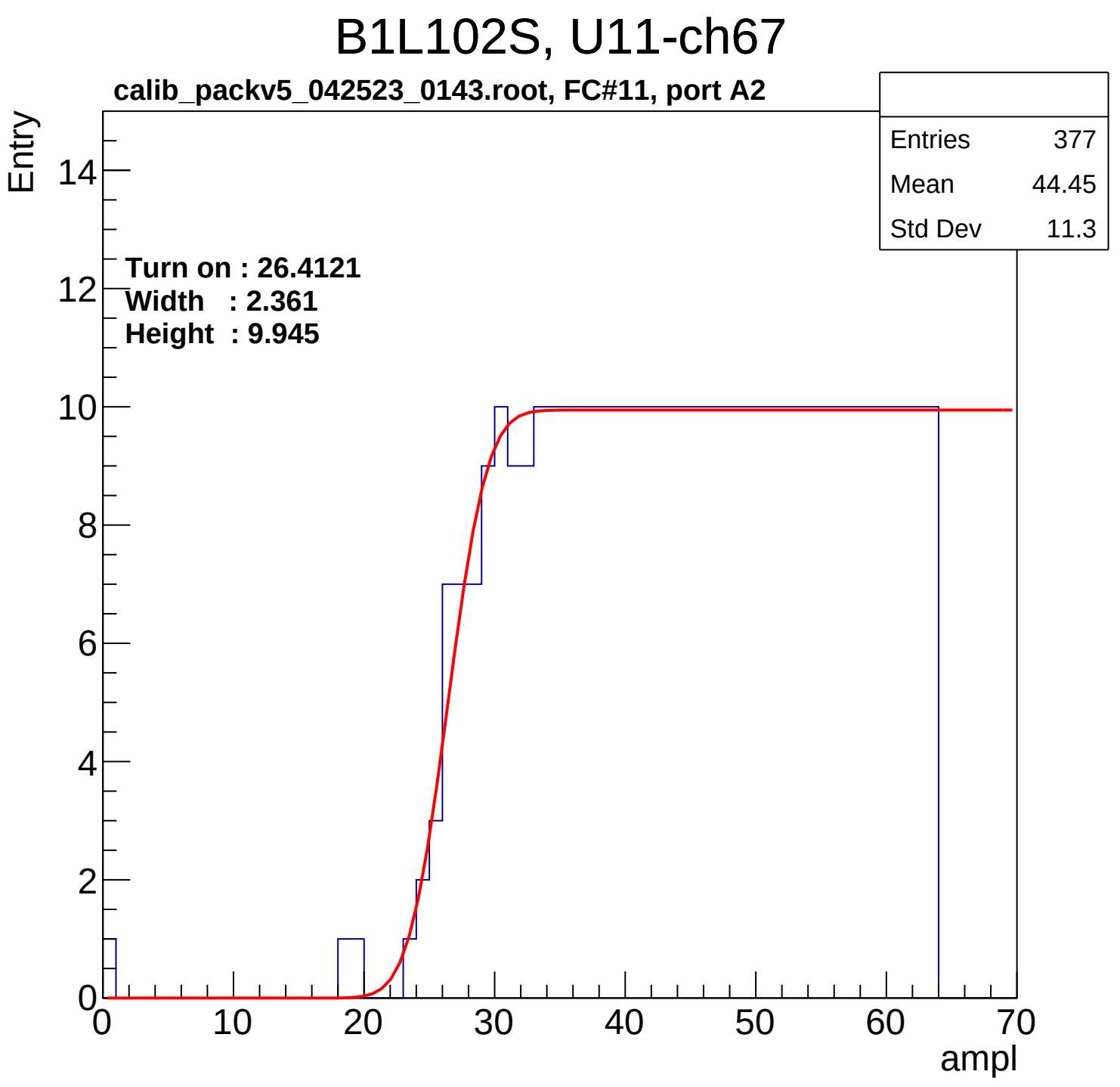
B1L102S, U11-ch67
calib_packv5_042523_0143.root, FC#11, port A2
Entries 377
Mean 44.45
Std Dev 11.3
Turn on : 26.4121
Width : 2.361
Height : 9.945
Entry
ampl
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2
4
6
8
10
12
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60
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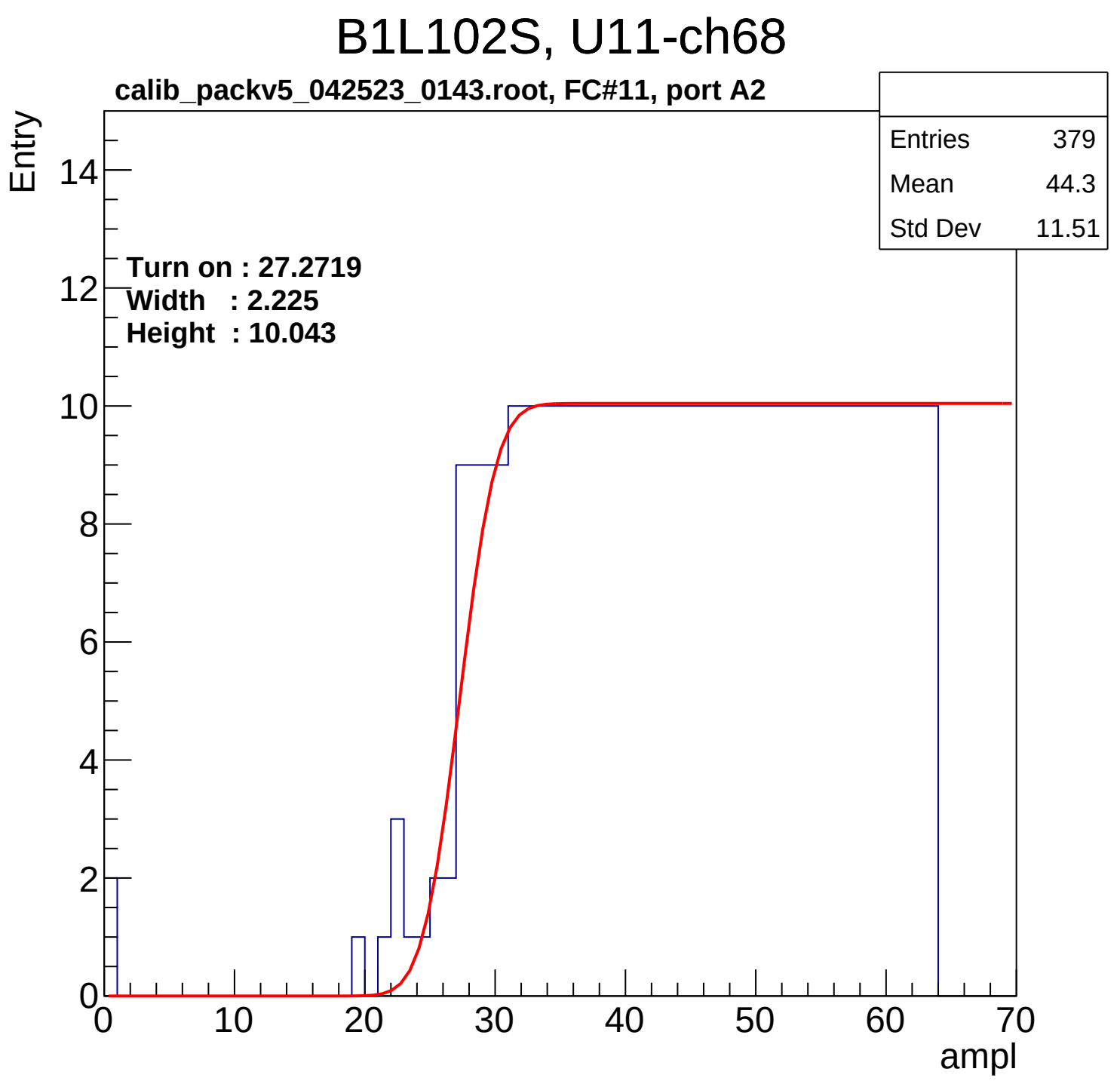
B1L102S, U11-ch68
calib_packv5_042523_0143.root, FC#11, port A2
Entries 379
Mean 44.3
Std Dev 11.51
Turn on : 27.2719
Width : 2.225
Height : 10.043
Entry
ampl
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6
8
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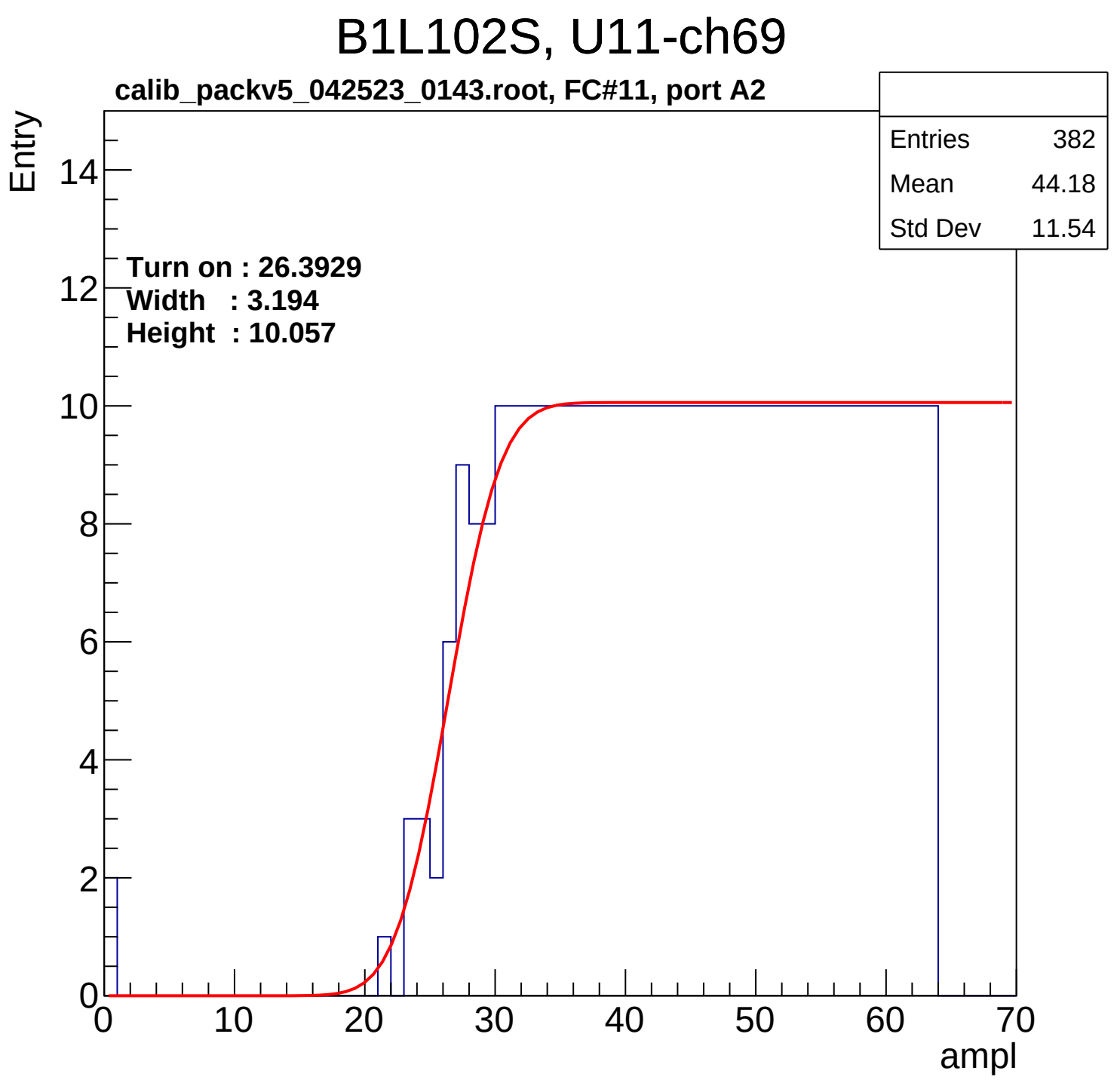
B1L102S, U11-ch69
calib_packv5_042523_0143.root, FC#11, port A2
Entries 382
Mean 44.18
Std Dev 11.54
Turn on : 26.3929
Width : 3.194
Height : 10.057
Entry
ampl
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6
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10
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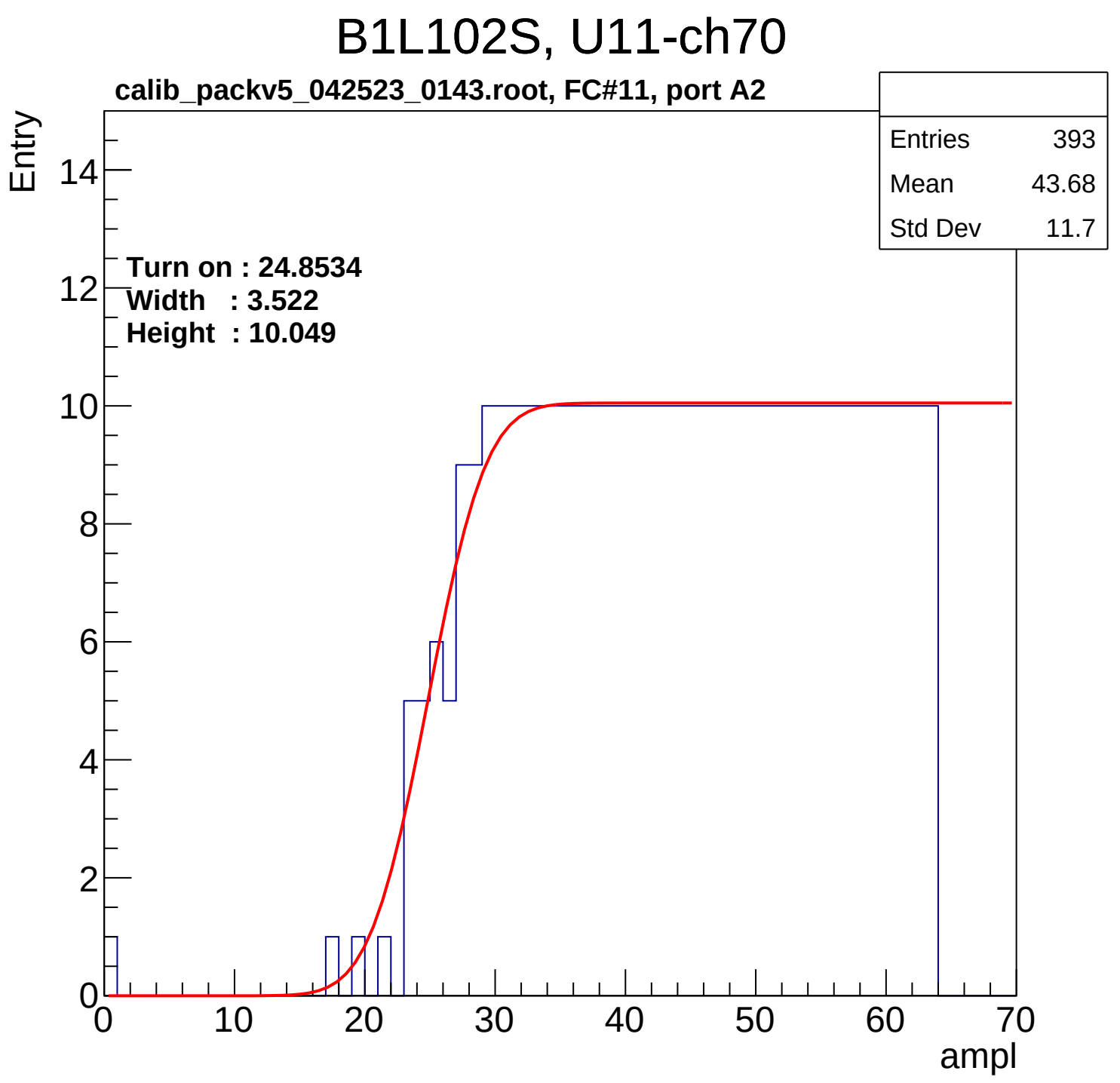
B1L102S, U11-ch70
calib_packv5_042523_0143.root, FC#11, port A2
Entries 393
Mean 43.68
Std Dev 11.7
Turn on : 24.8534
Width : 3.522
Height : 10.049
Entry
ampl
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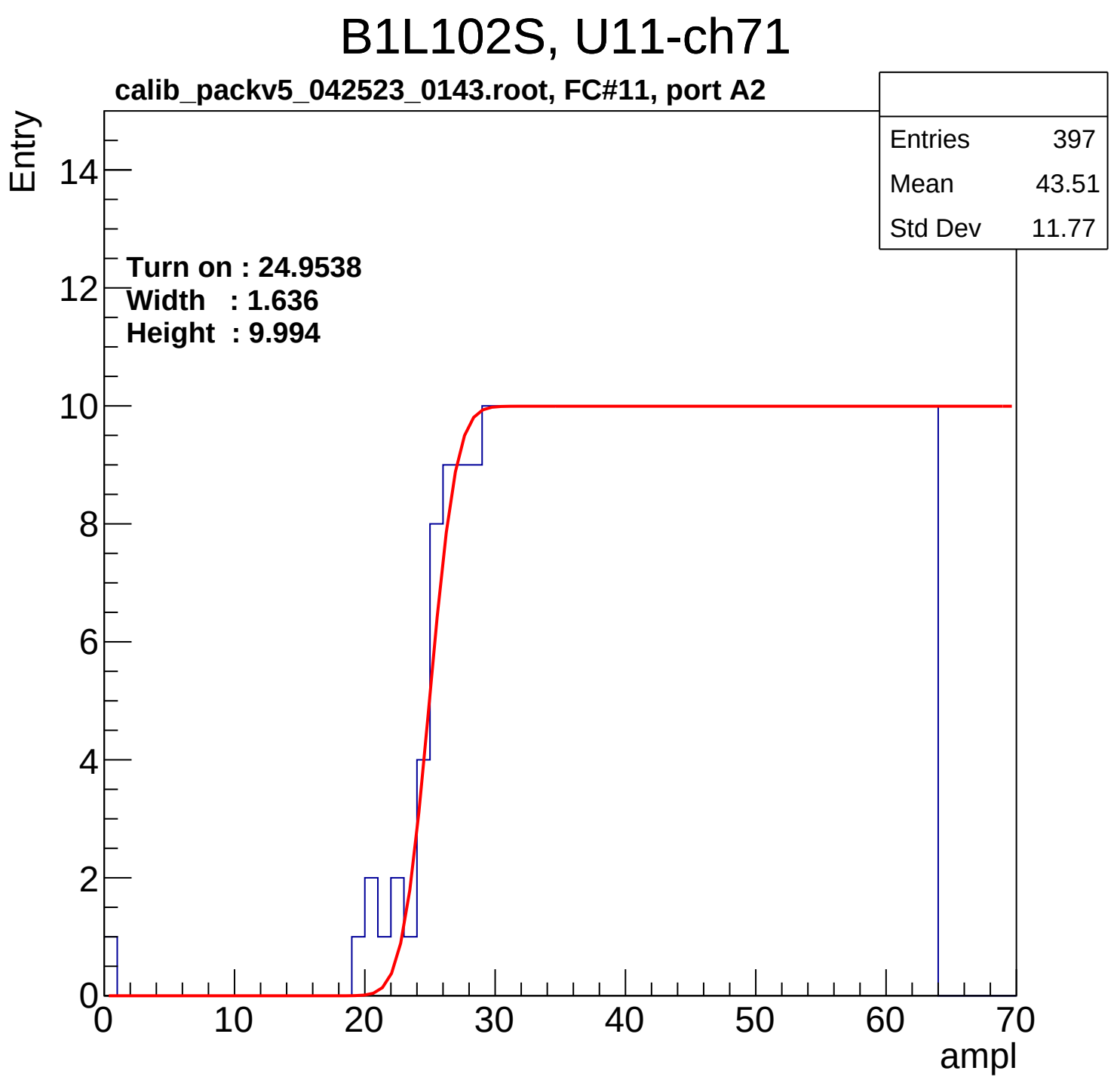
B1L102S, U11-ch71
calib_packv5_042523_0143.root, FC#11, port A2
Entries 397
Mean 43.51
Std Dev 11.77
Turn on : 24.9538
Width : 1.636
Height : 9.994
Entry
ampl
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6
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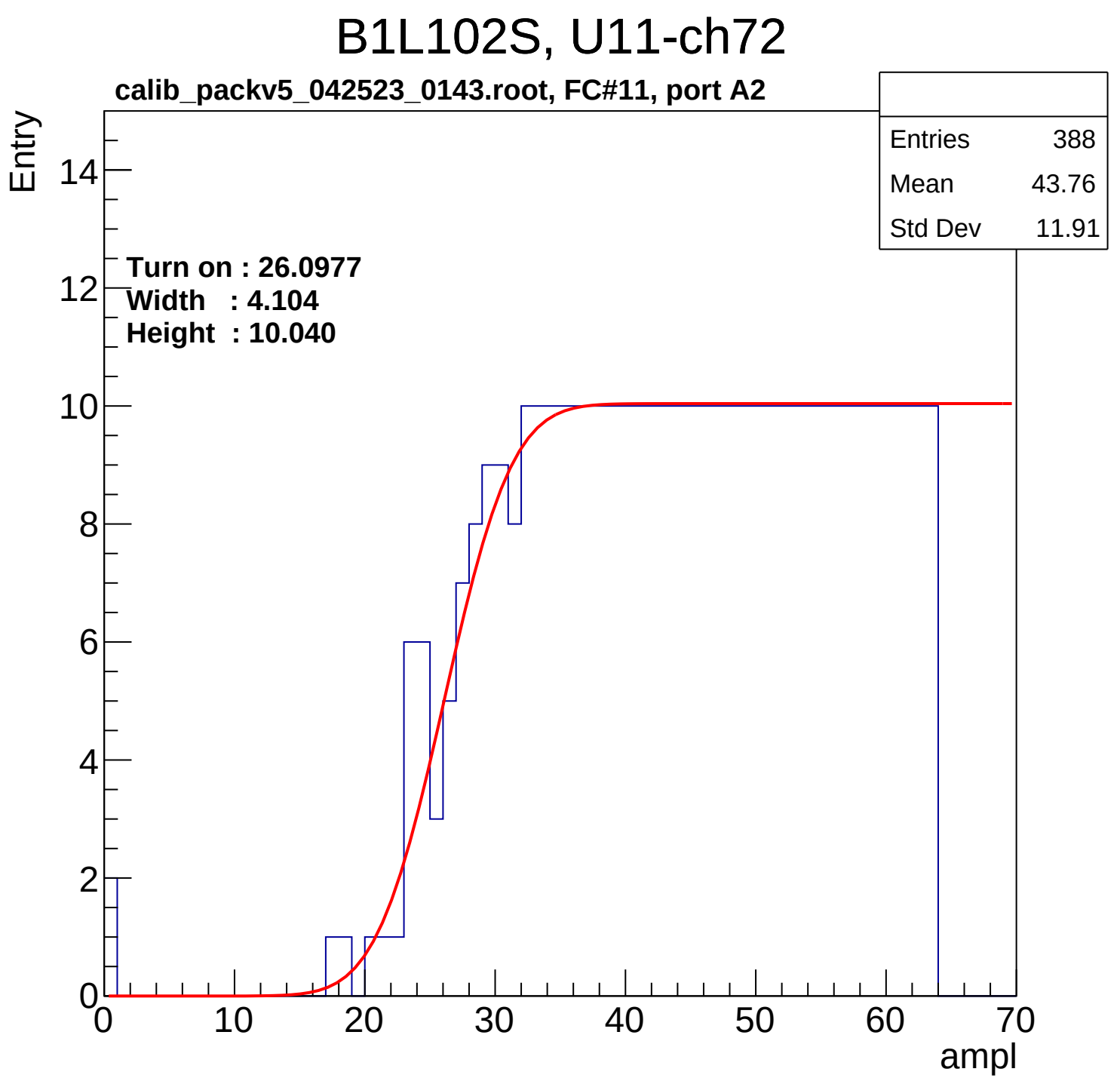
B1L102S, U11-ch72
calib_packv5_042523_0143.root, FC#11, port A2
Entries 388
Mean 43.76
Std Dev 11.91
Turn on : 26.0977
Width : 4.104
Height : 10.040
Entry
ampl
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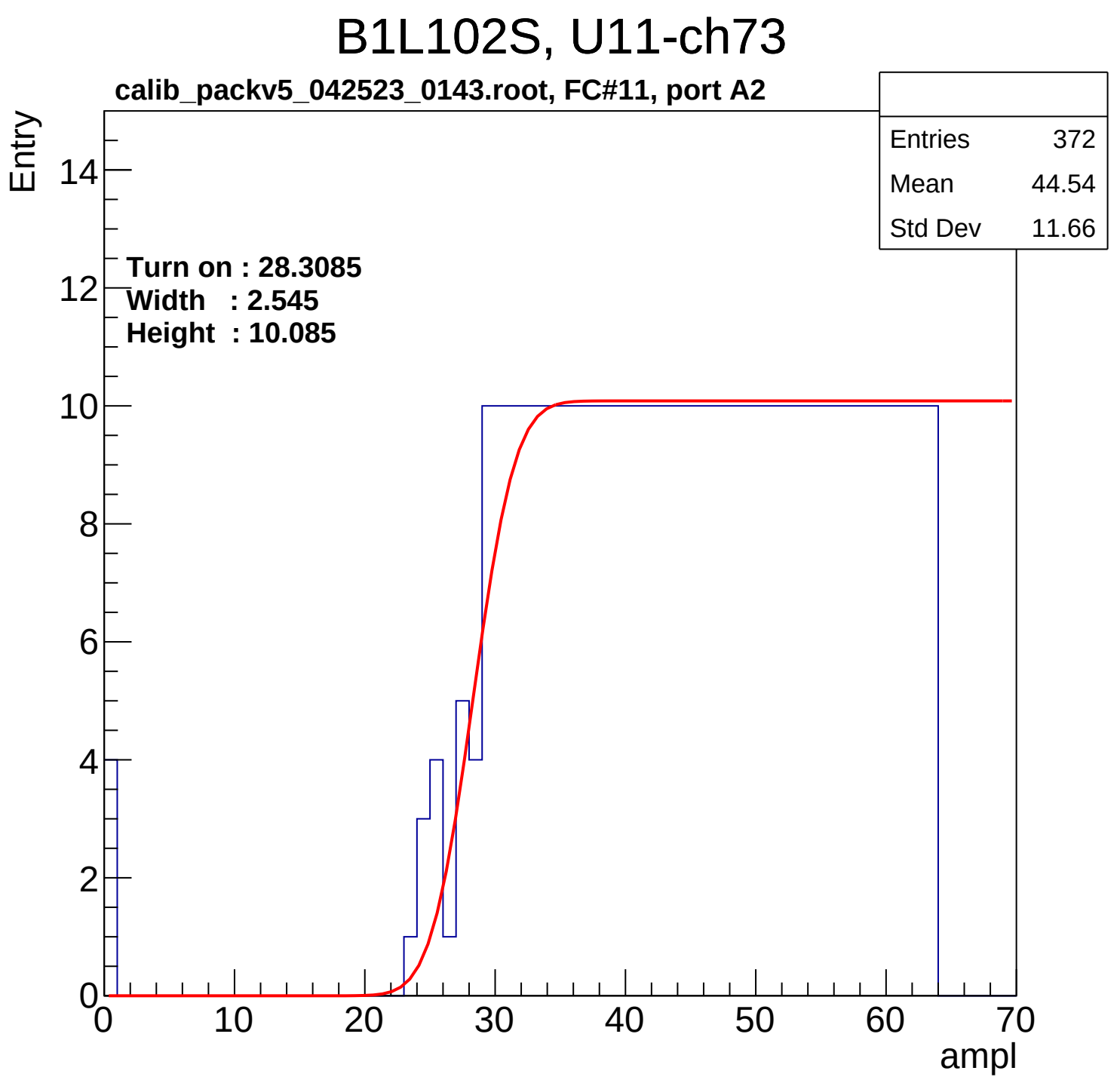
B1L102S, U11-ch73
calib_packv5_042523_0143.root, FC#11, port A2
Entries 372
Mean 44.54
Std Dev 11.66
Turn on : 28.3085
Width : 2.545
Height : 10.085
Entry
ampl
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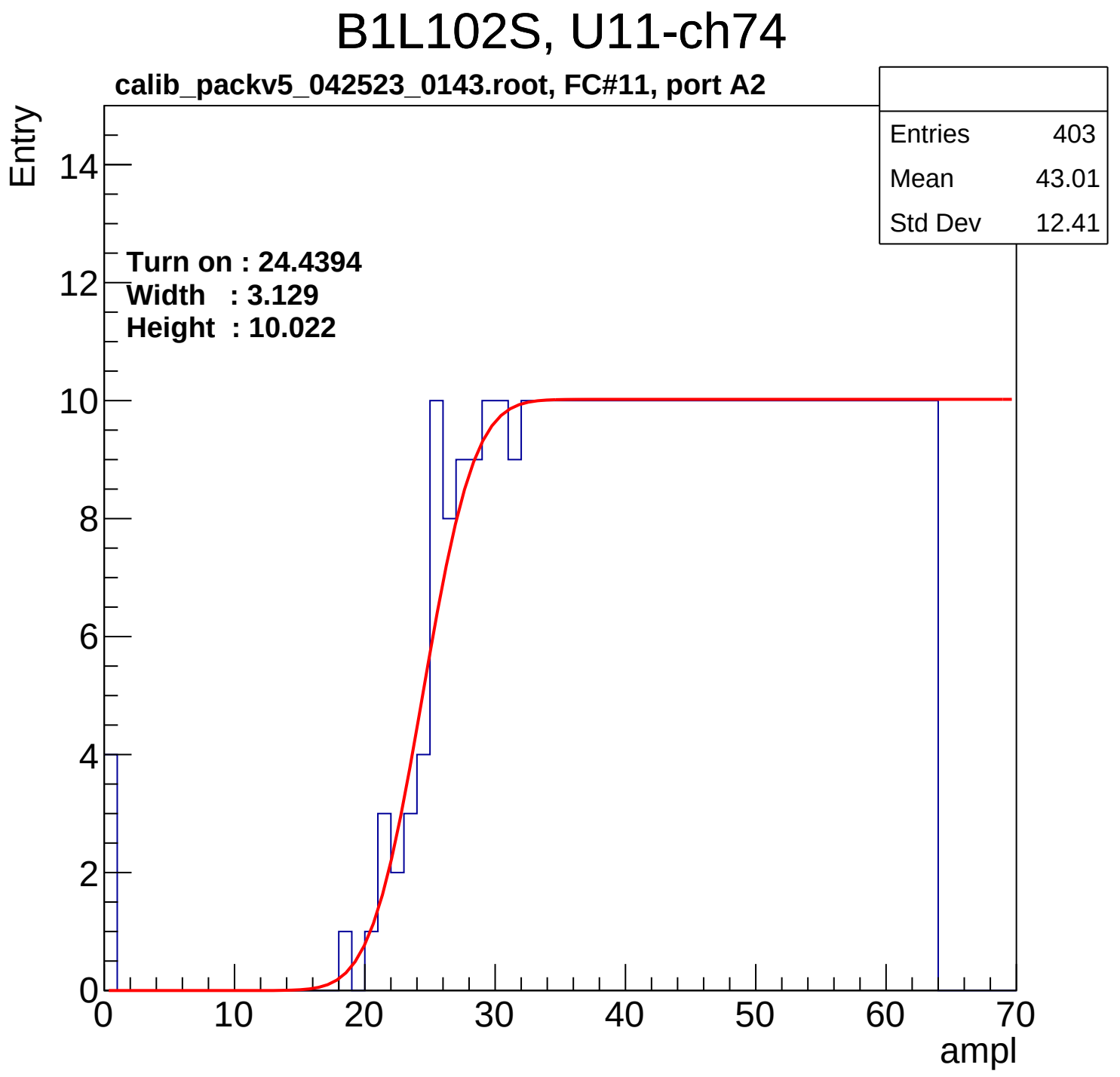
B1L102S, U11-ch74
calib_packv5_042523_0143.root, FC#11, port A2
Entries 403
Mean 43.01
Std Dev 12.41
Turn on : 24.4394
Width : 3.129
Height : 10.022
Entry
ampl
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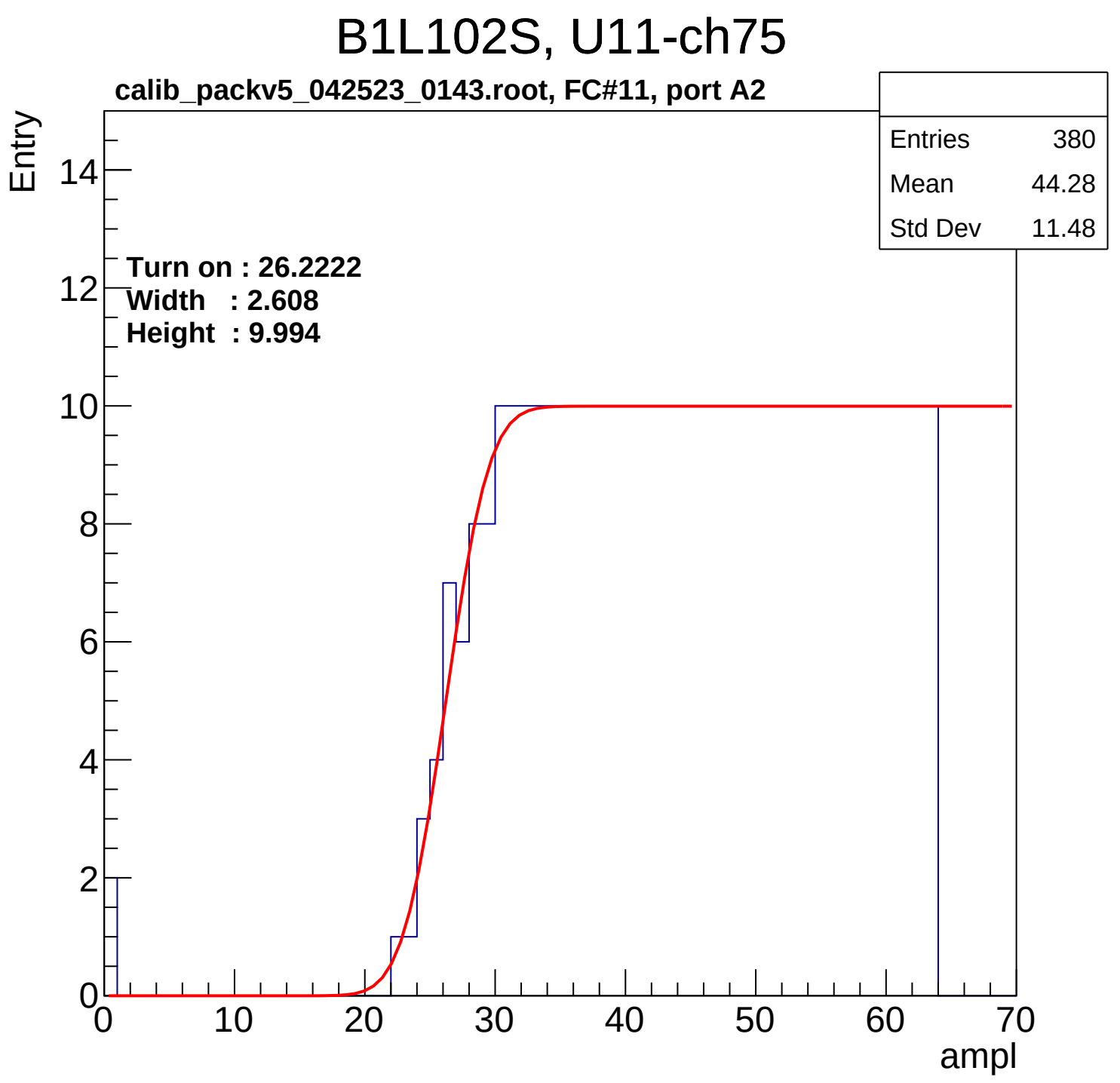
B1L102S, U11-ch75
calib_packv5_042523_0143.root, FC#11, port A2
Entries 380
Mean 44.28
Std Dev 11.48
Turn on : 26.2222
Width : 2.608
Height : 9.994
Entry
ampl
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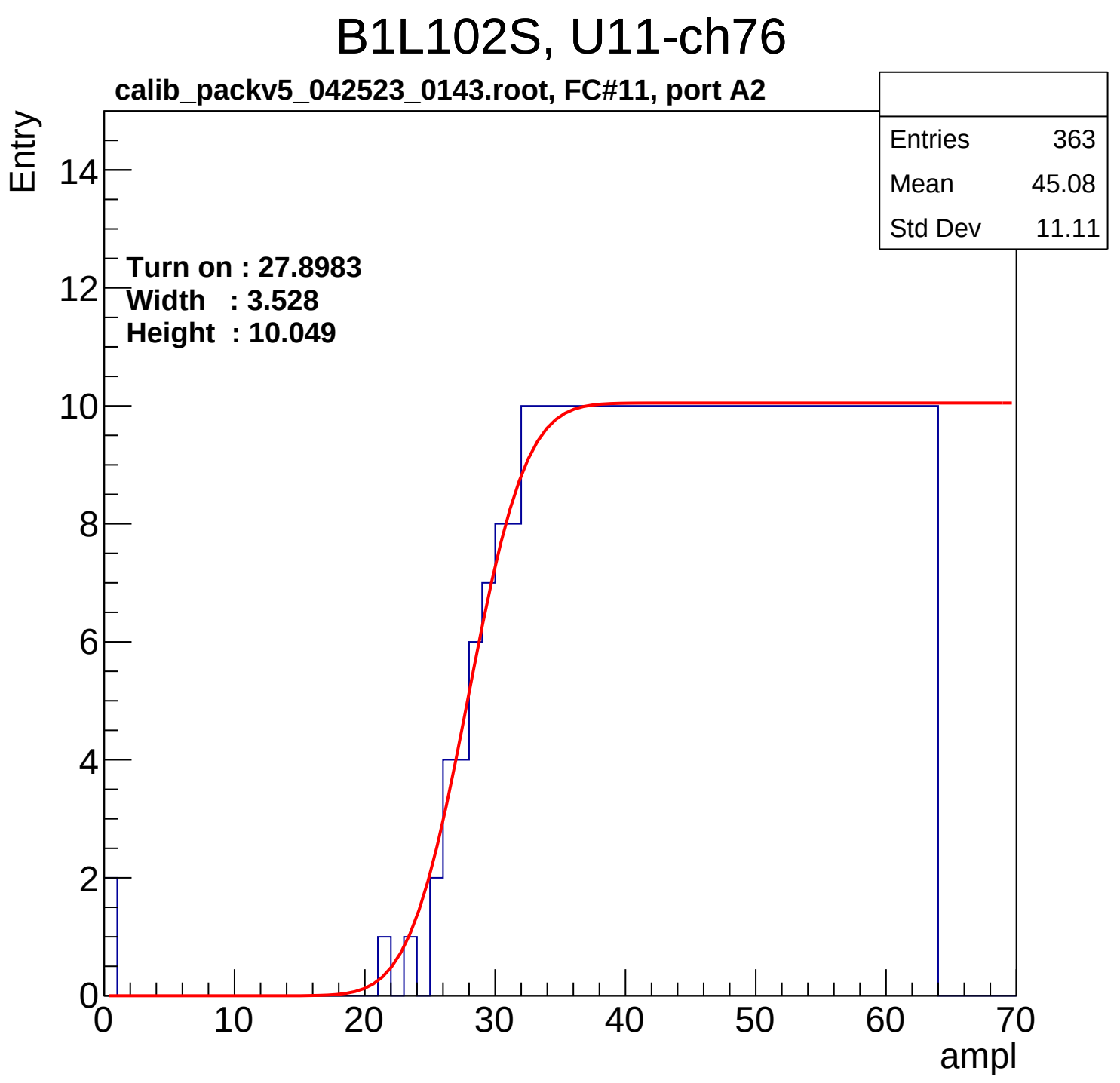
B1L102S, U11-ch76
calib_packv5_042523_0143.root, FC#11, port A2
Entries 363
Mean 45.08
Std Dev 11.11
Turn on : 27.8983
Width : 3.528
Height : 10.049
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ampl
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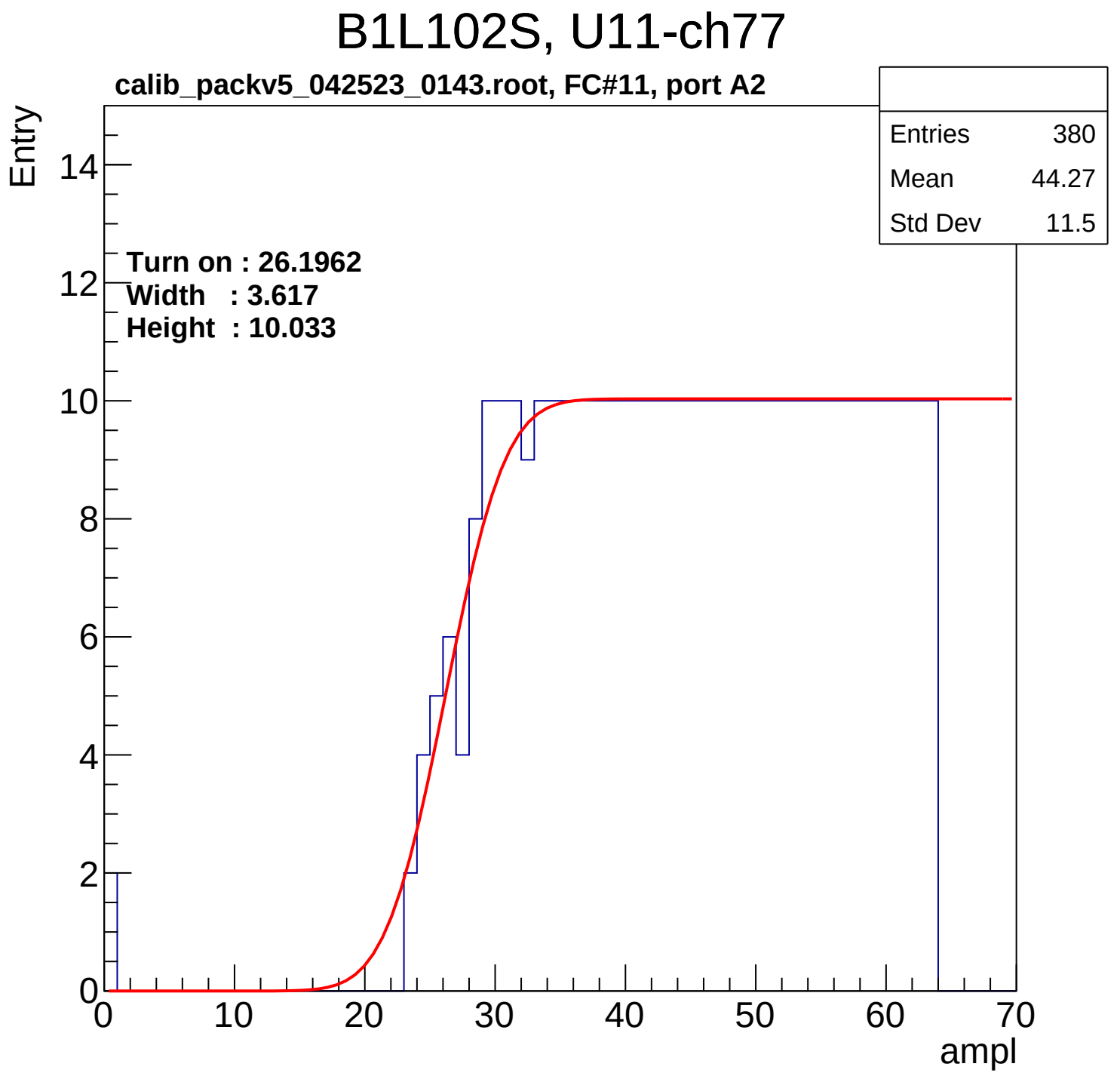
B1L102S, U11-ch77
calib_packv5_042523_0143.root, FC#11, port A2
Entries 380
Mean 44.27
Std Dev 11.5
Turn on : 26.1962
Width : 3.617
Height : 10.033
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ampl
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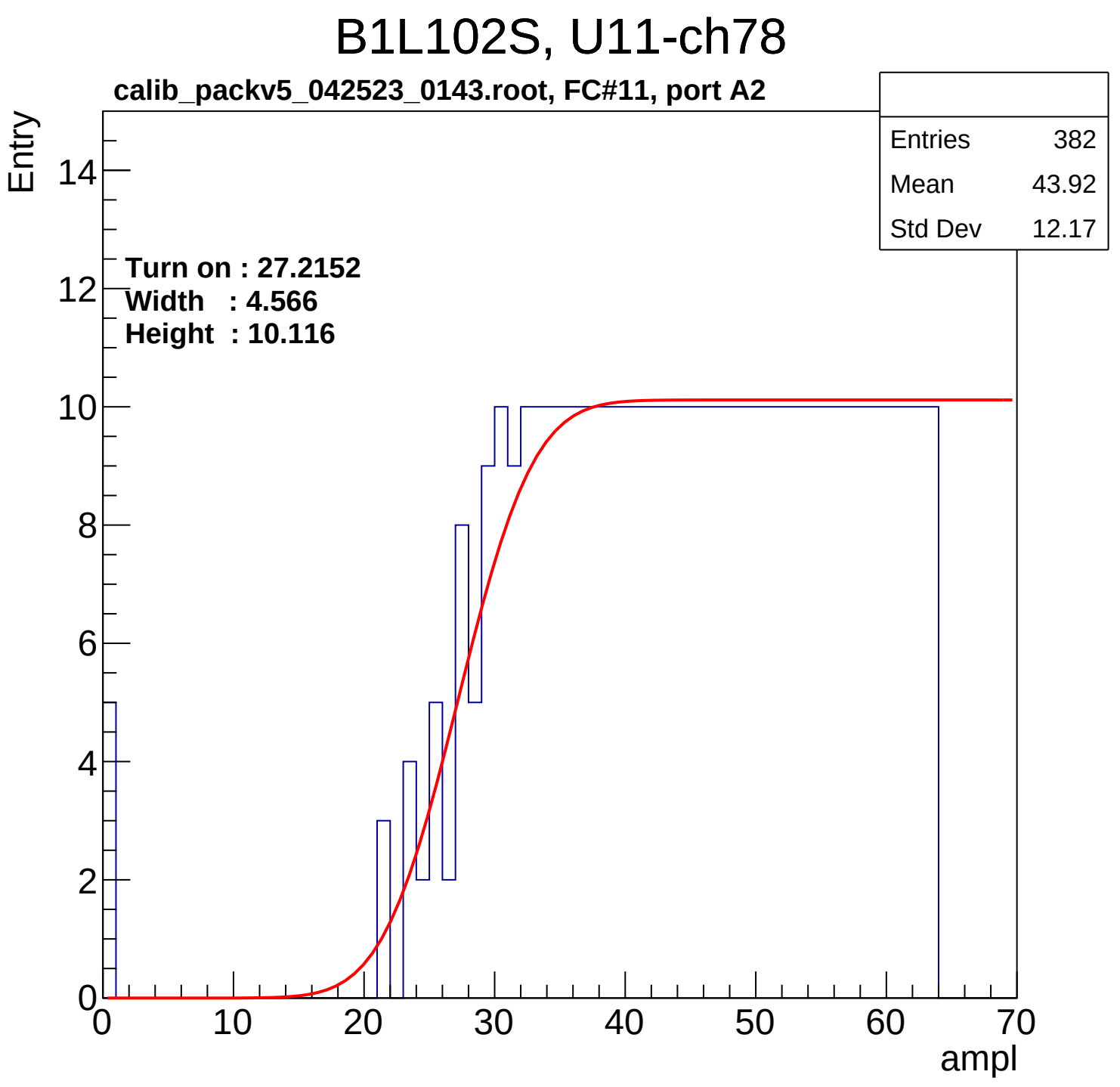
B1L102S, U11-ch78
calib_packv5_042523_0143.root, FC#11, port A2
Entries 382
Mean 43.92
Std Dev 12.17
Turn on : 27.2152
Width : 4.566
Height : 10.116
Entry
ampl
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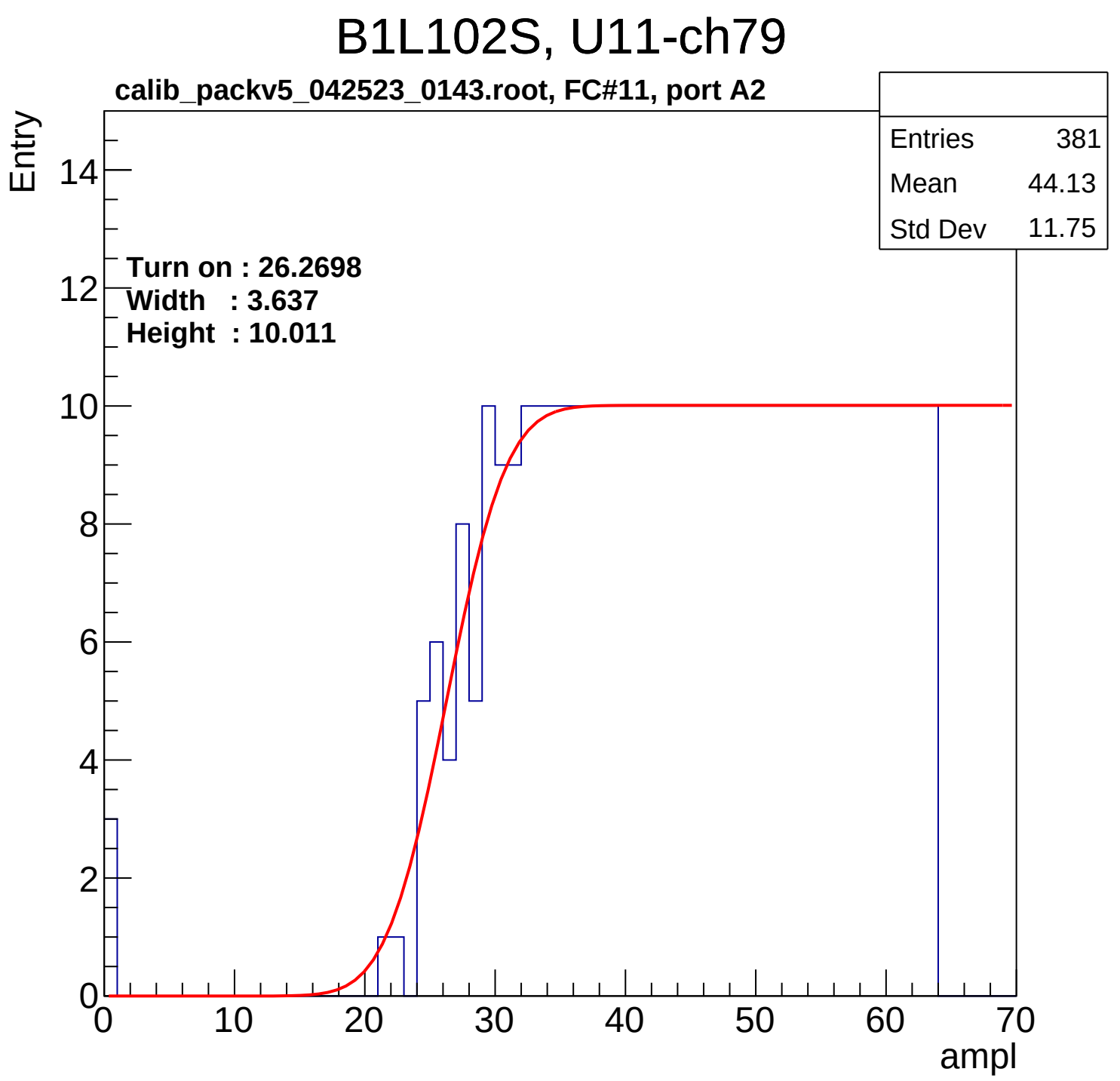
B1L102S, U11-ch79
calib_packv5_042523_0143.root, FC#11, port A2
Entries 381
Mean 44.13
Std Dev 11.75
Turn on : 26.2698
Width : 3.637
Height : 10.011
Entry
ampl
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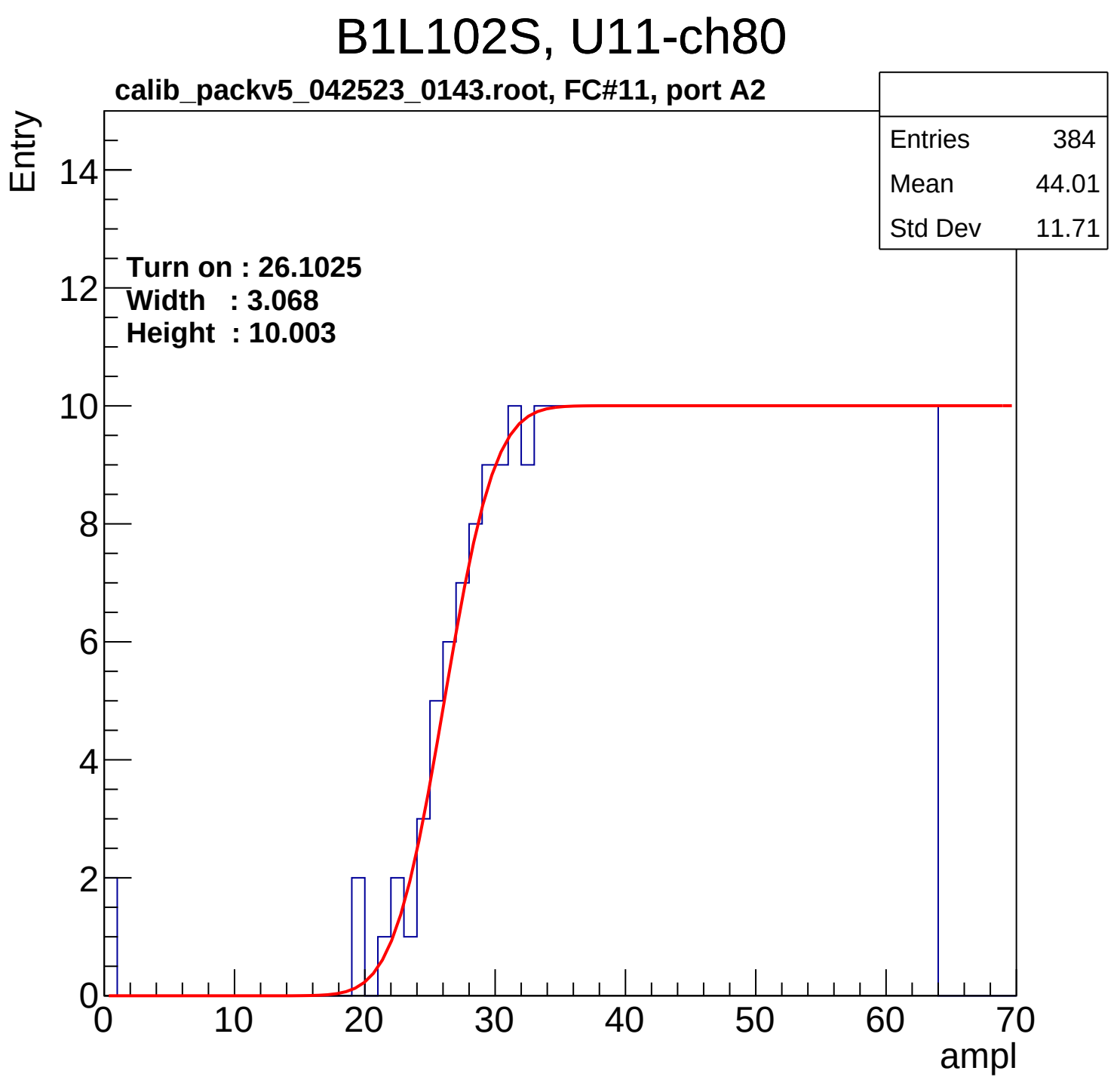
B1L102S, U11-ch80
calib_packv5_042523_0143.root, FC#11, port A2
Entries 384
Mean 44.01
Std Dev 11.71
Turn on : 26.1025
Width : 3.068
Height : 10.003
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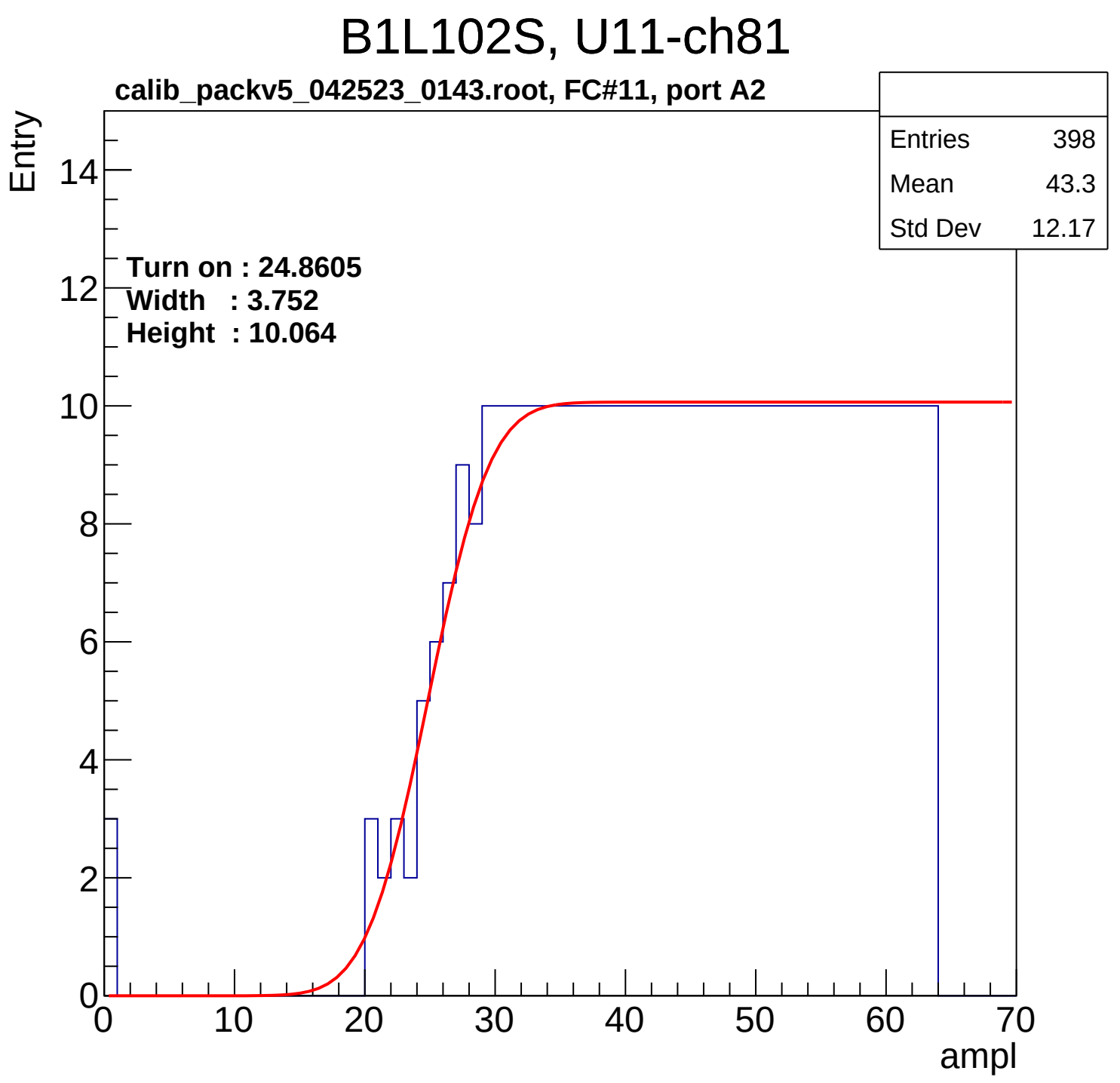
B1L102S, U11-ch81
calib_packv5_042523_0143.root, FC#11, port A2
Entries 398
Mean 43.3
Std Dev 12.17
Turn on : 24.8605
Width : 3.752
Height : 10.064
Entry
ampl
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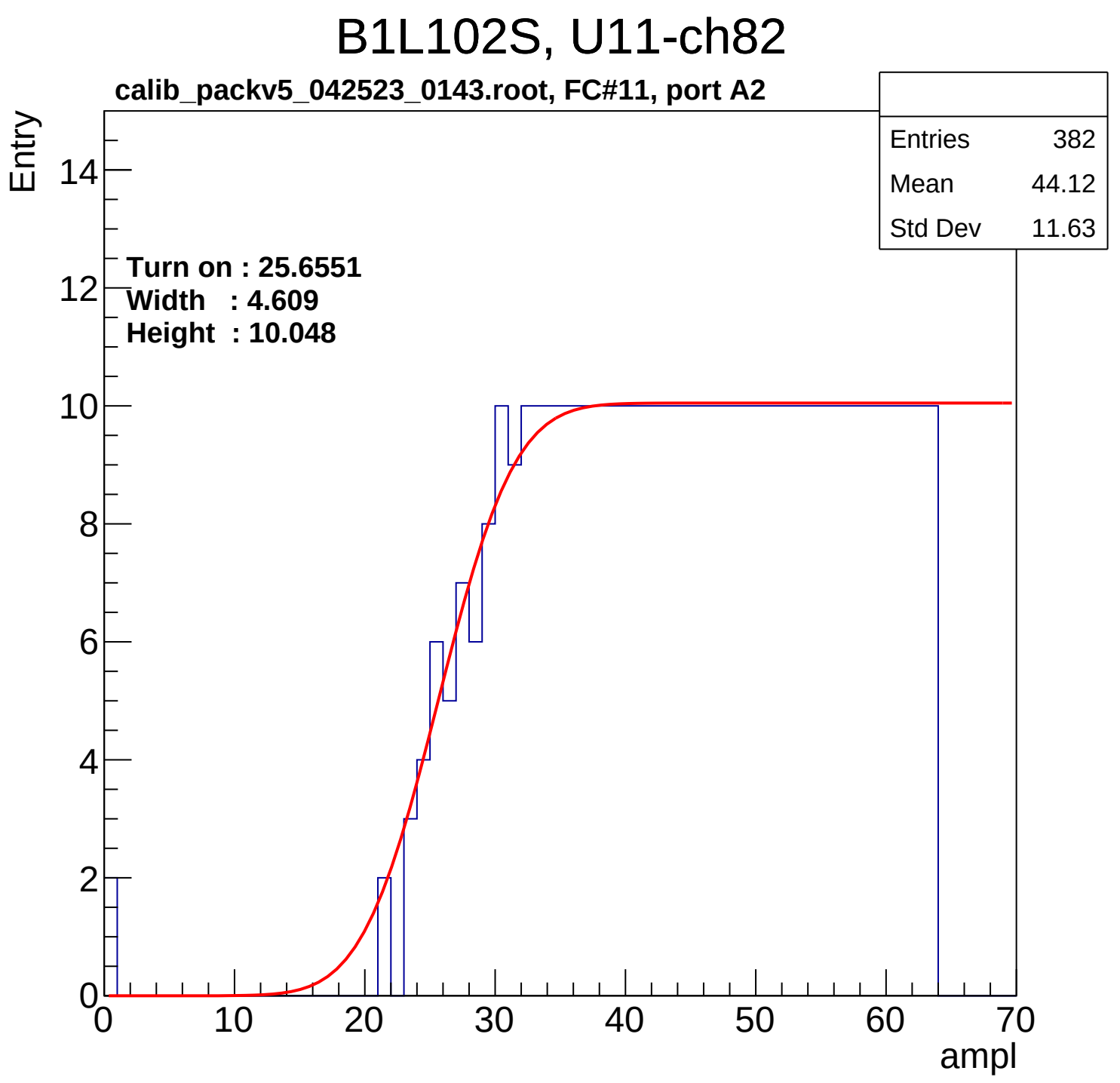
B1L102S, U11-ch82
calib_packv5_042523_0143.root, FC#11, port A2
Entries 382
Mean 44.12
Std Dev 11.63
Turn on : 25.6551
Width : 4.609
Height : 10.048
Entry
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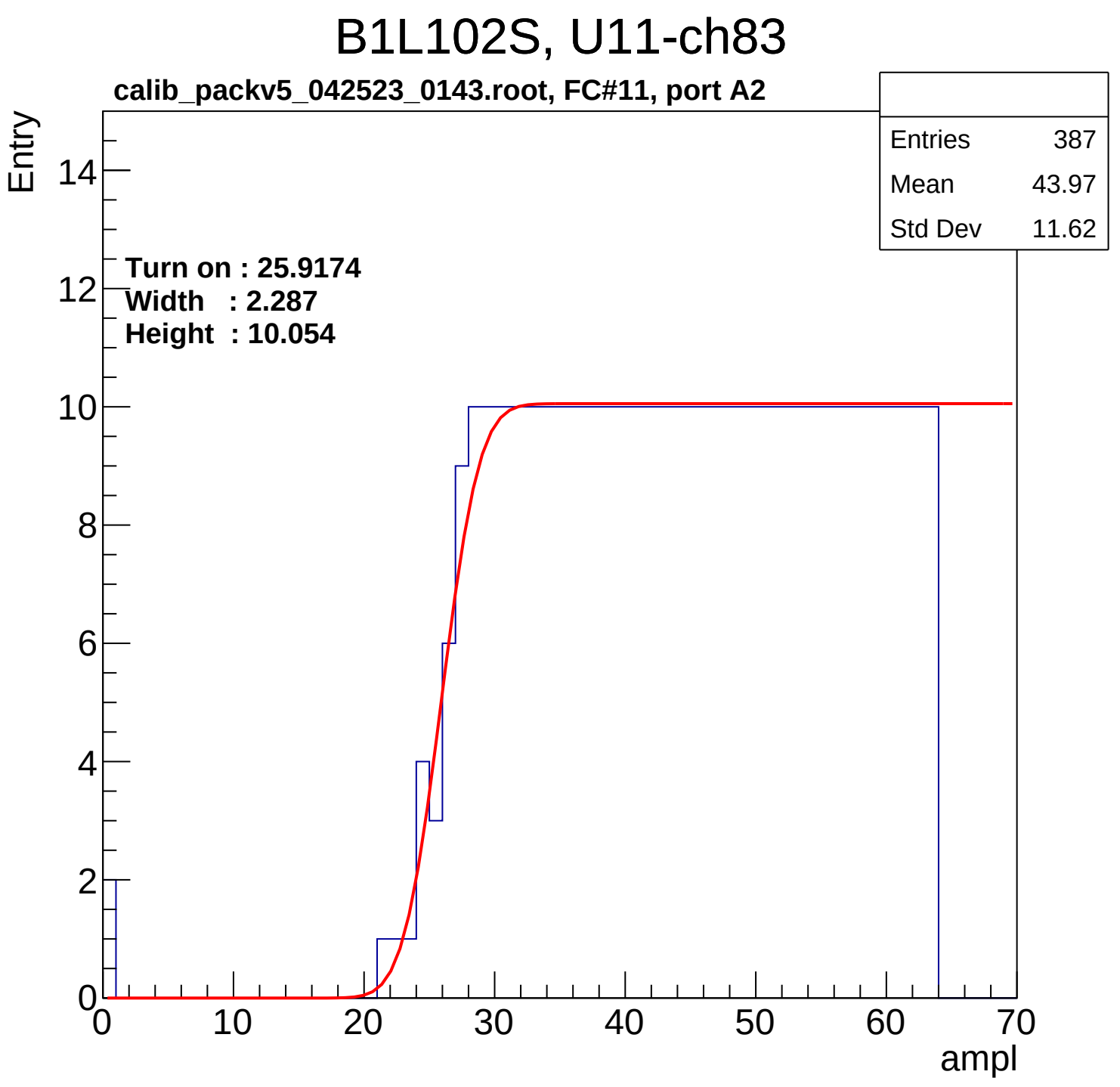
B1L102S, U11-ch83
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 43.97
Std Dev 11.62
Turn on : 25.9174
Width : 2.287
Height : 10.054
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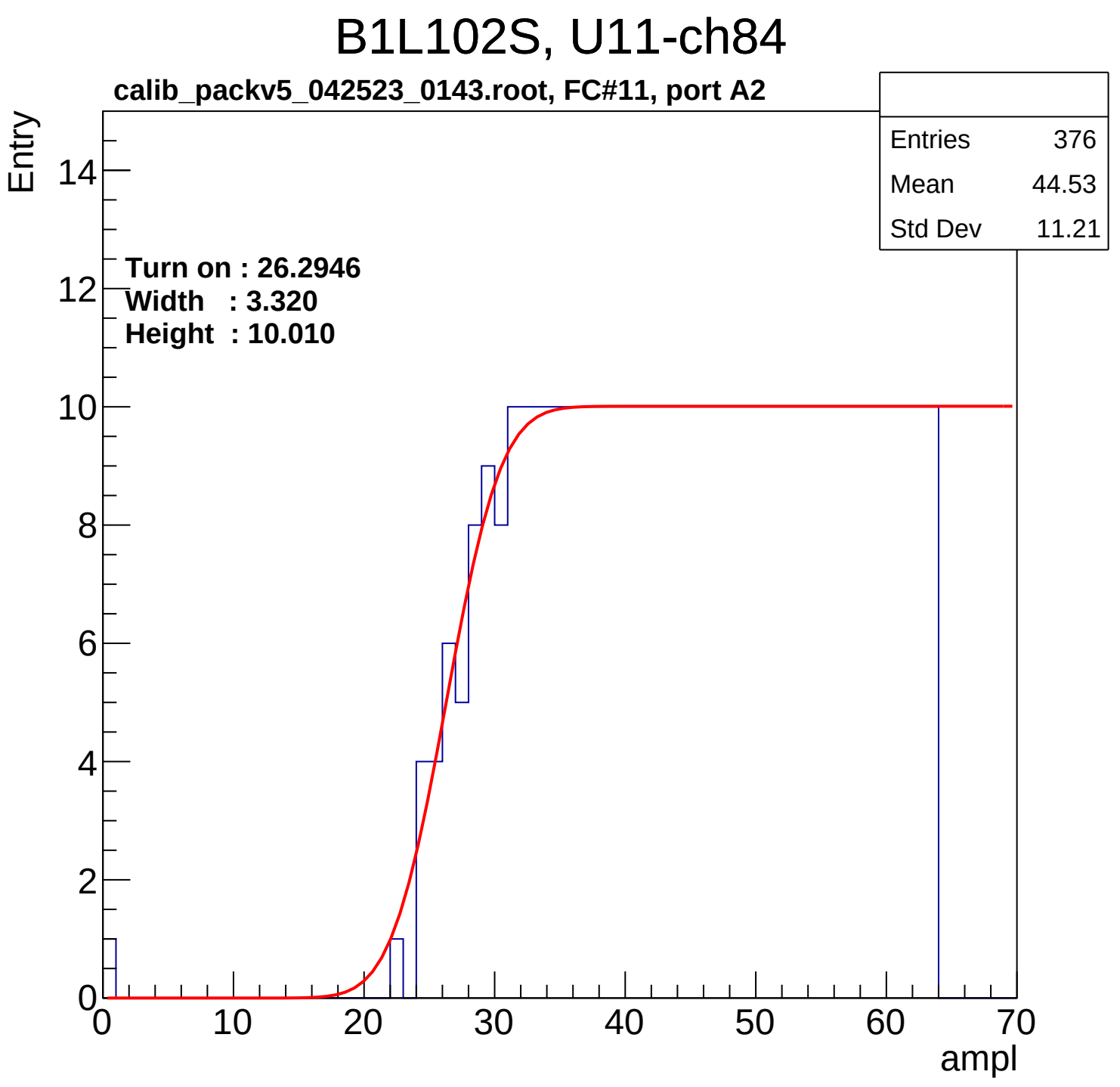
B1L102S, U11-ch84
calib_packv5_042523_0143.root, FC#11, port A2
Entries 376
Mean 44.53
Std Dev 11.21
Turn on : 26.2946
Width : 3.320
Height : 10.010
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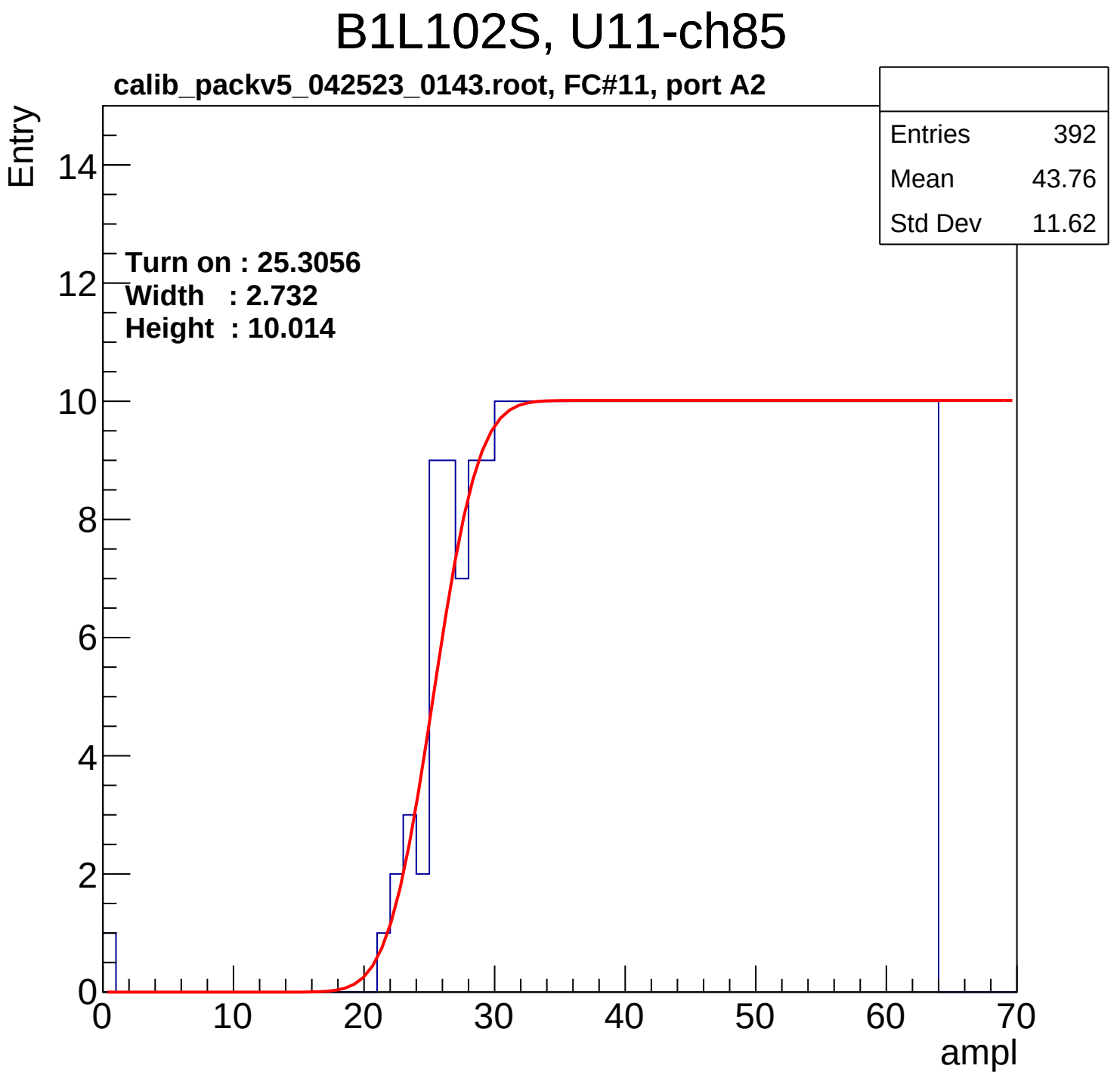
B1L102S, U11-ch85
calib_packv5_042523_0143.root, FC#11, port A2
Entries 392
Mean 43.76
Std Dev 11.62
Turn on : 25.3056
Width : 2.732
Height : 10.014
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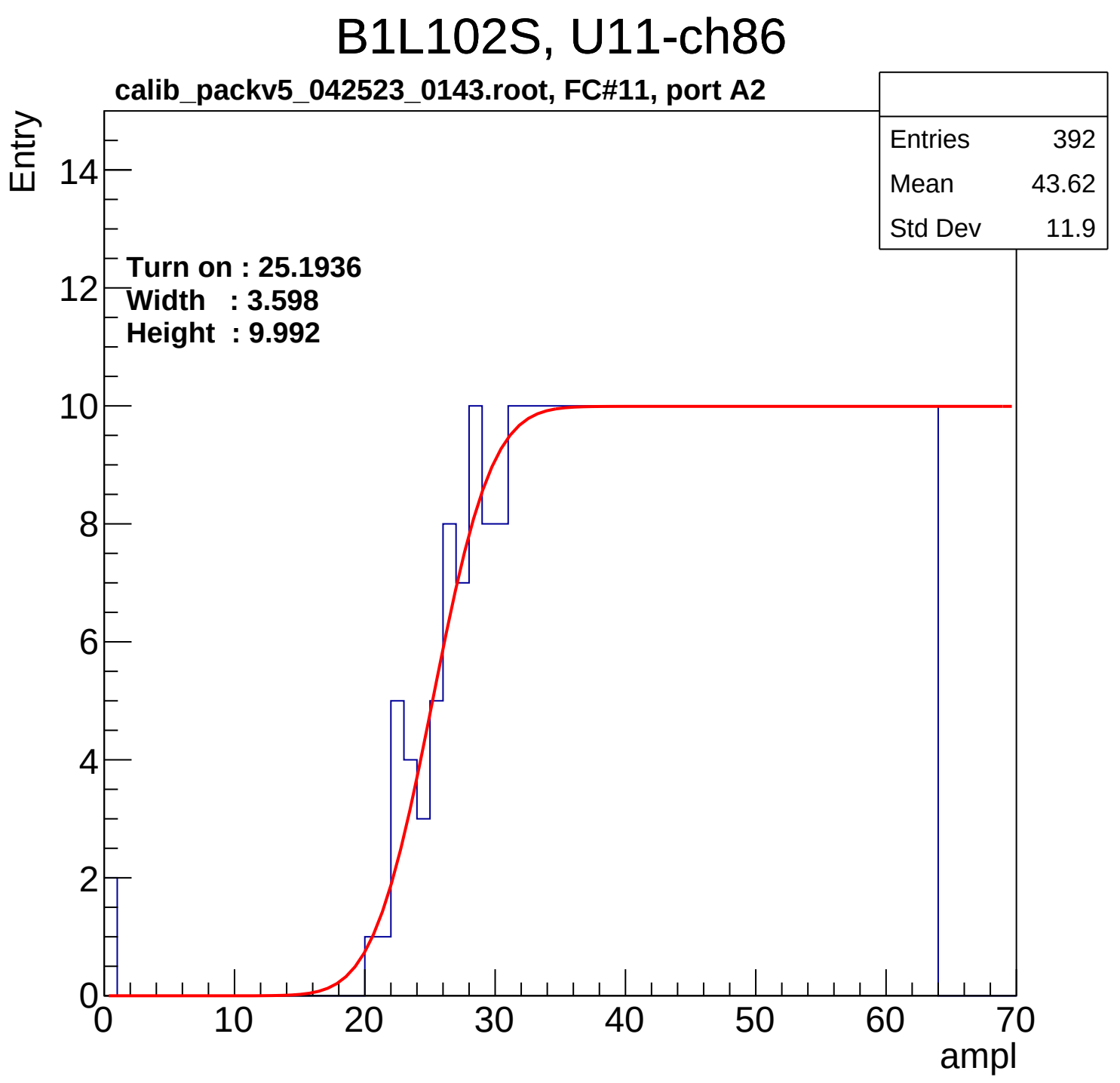
B1L102S, U11-ch86
calib_packv5_042523_0143.root, FC#11, port A2
Entries 392
Mean 43.62
Std Dev 11.9
Turn on : 25.1936
Width : 3.598
Height : 9.992
Entry
ampl
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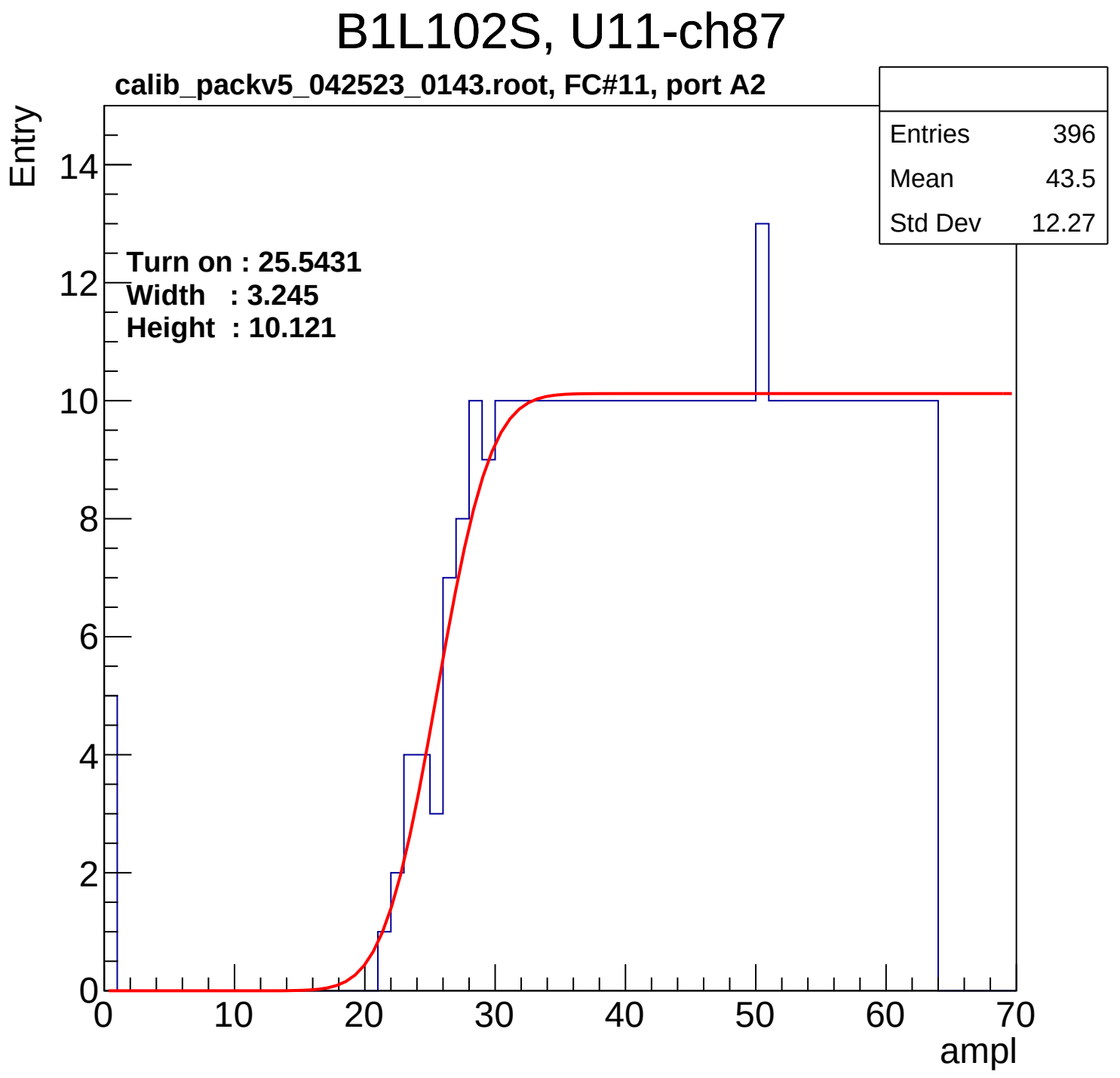
B1L102S, U11-ch87
calib_packv5_042523_0143.root, FC#11, port A2
Entries 396
Mean 43.5
Std Dev 12.27
Turn on : 25.5431
Width : 3.245
Height : 10.121
Entry
ampl
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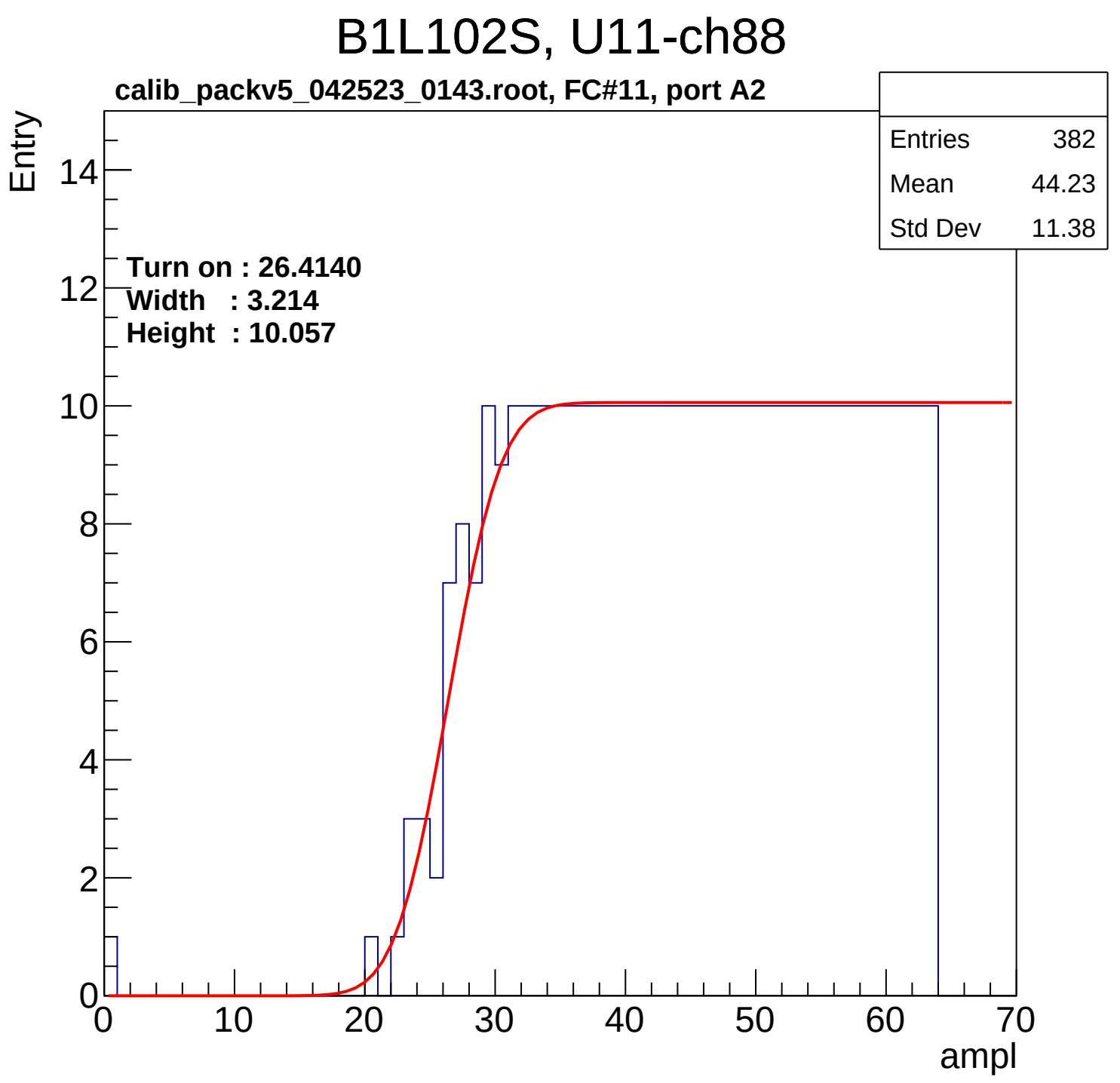
B1L102S, U11-ch88
calib_packv5_042523_0143.root, FC#11, port A2
Entries 382
Mean 44.23
Std Dev 11.38
Turn on : 26.4140
Width : 3.214
Height : 10.057
Entry
ampl
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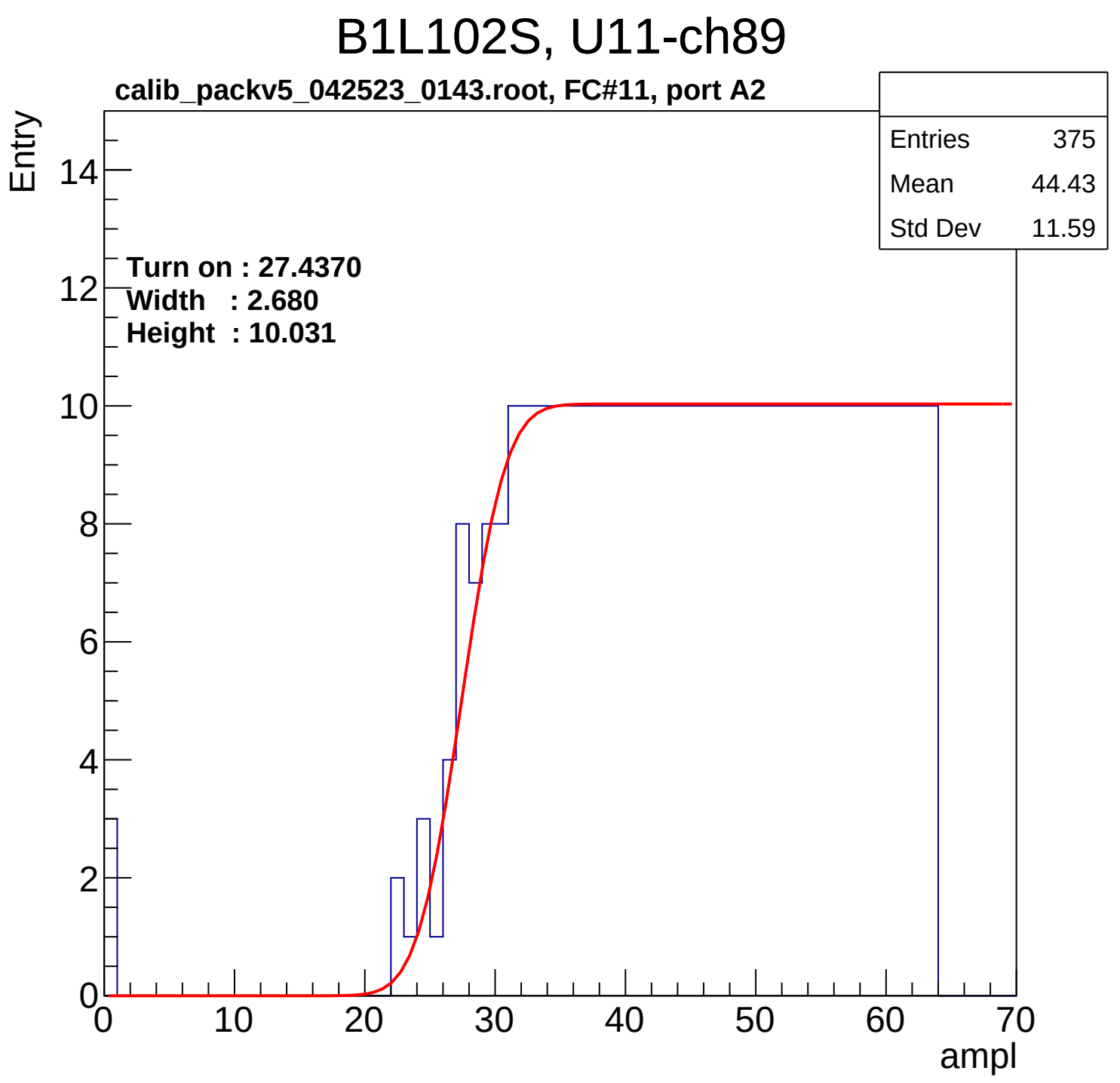
B1L102S, U11-ch89
calib_packv5_042523_0143.root, FC#11, port A2
Entries 375
Mean 44.43
Std Dev 11.59
Turn on : 27.4370
Width : 2.680
Height : 10.031
Entry
ampl
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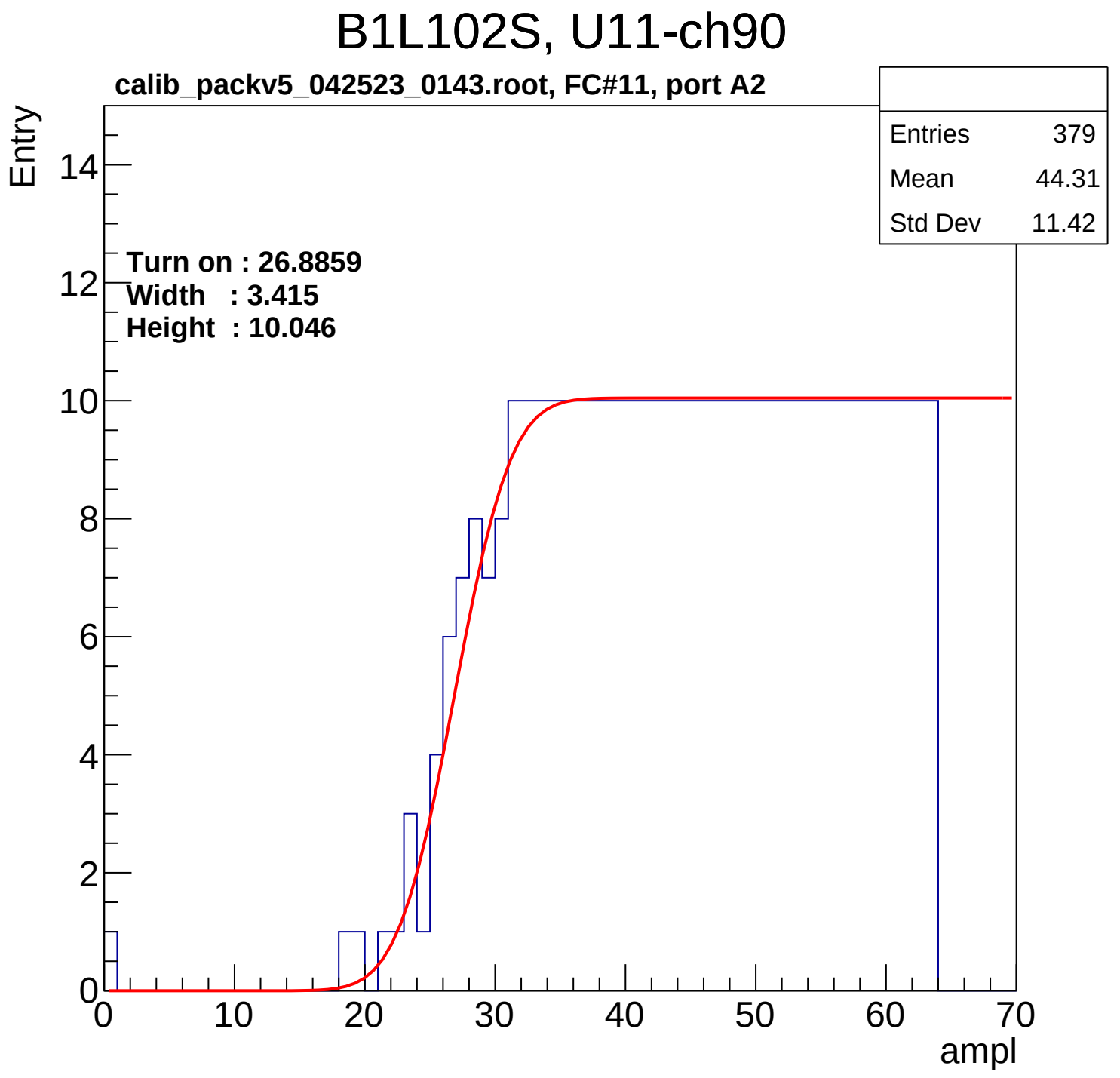
B1L102S, U11-ch90
calib_packv5_042523_0143.root, FC#11, port A2
Entries 379
Mean 44.31
Std Dev 11.42
Turn on : 26.8859
Width : 3.415
Height : 10.046
Entry
ampl
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2
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8
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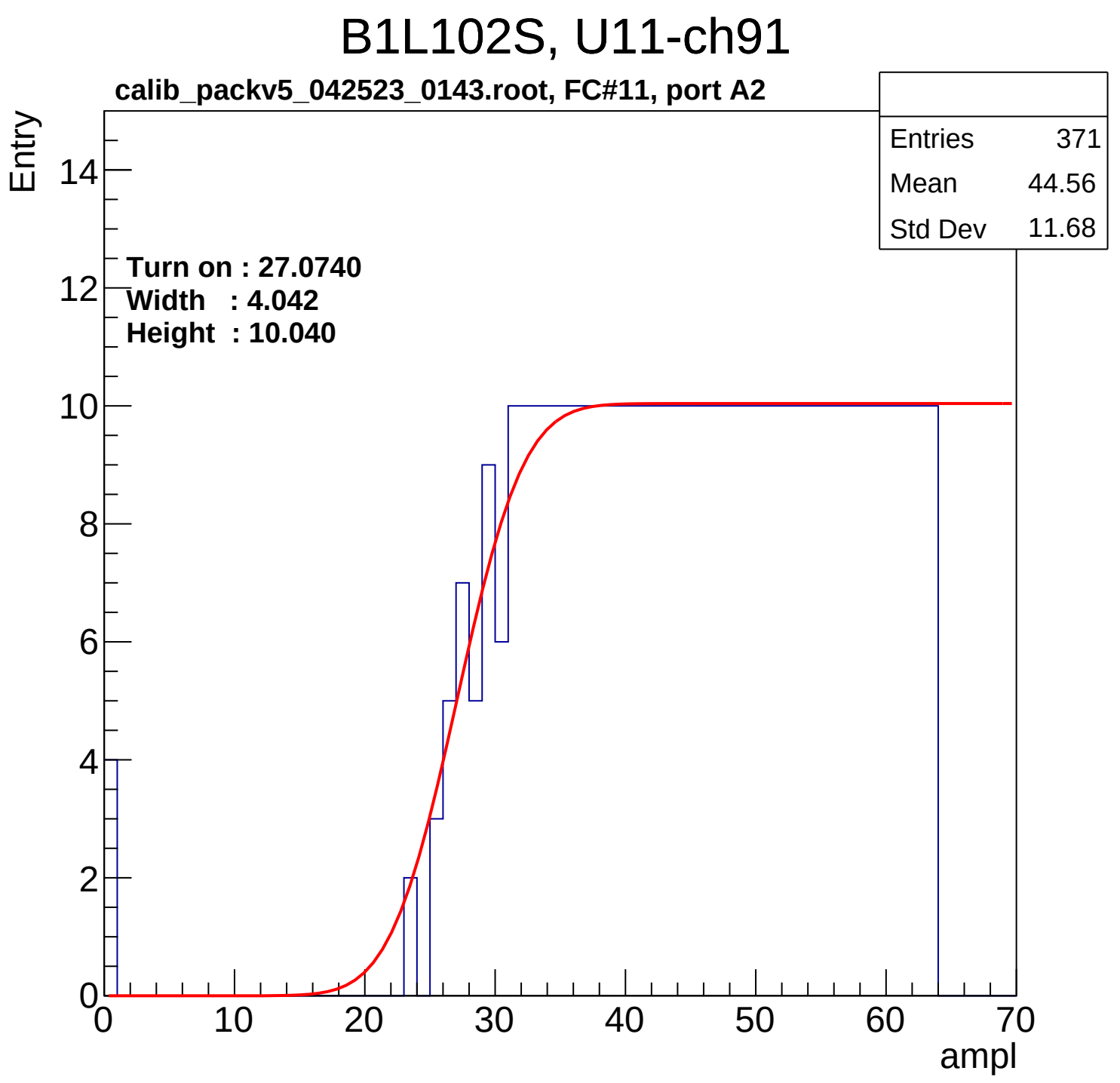
B1L102S, U11-ch91
calib_packv5_042523_0143.root, FC#11, port A2
Entries 371
Mean 44.56
Std Dev 11.68
Turn on : 27.0740
Width : 4.042
Height : 10.040
Entry
ampl
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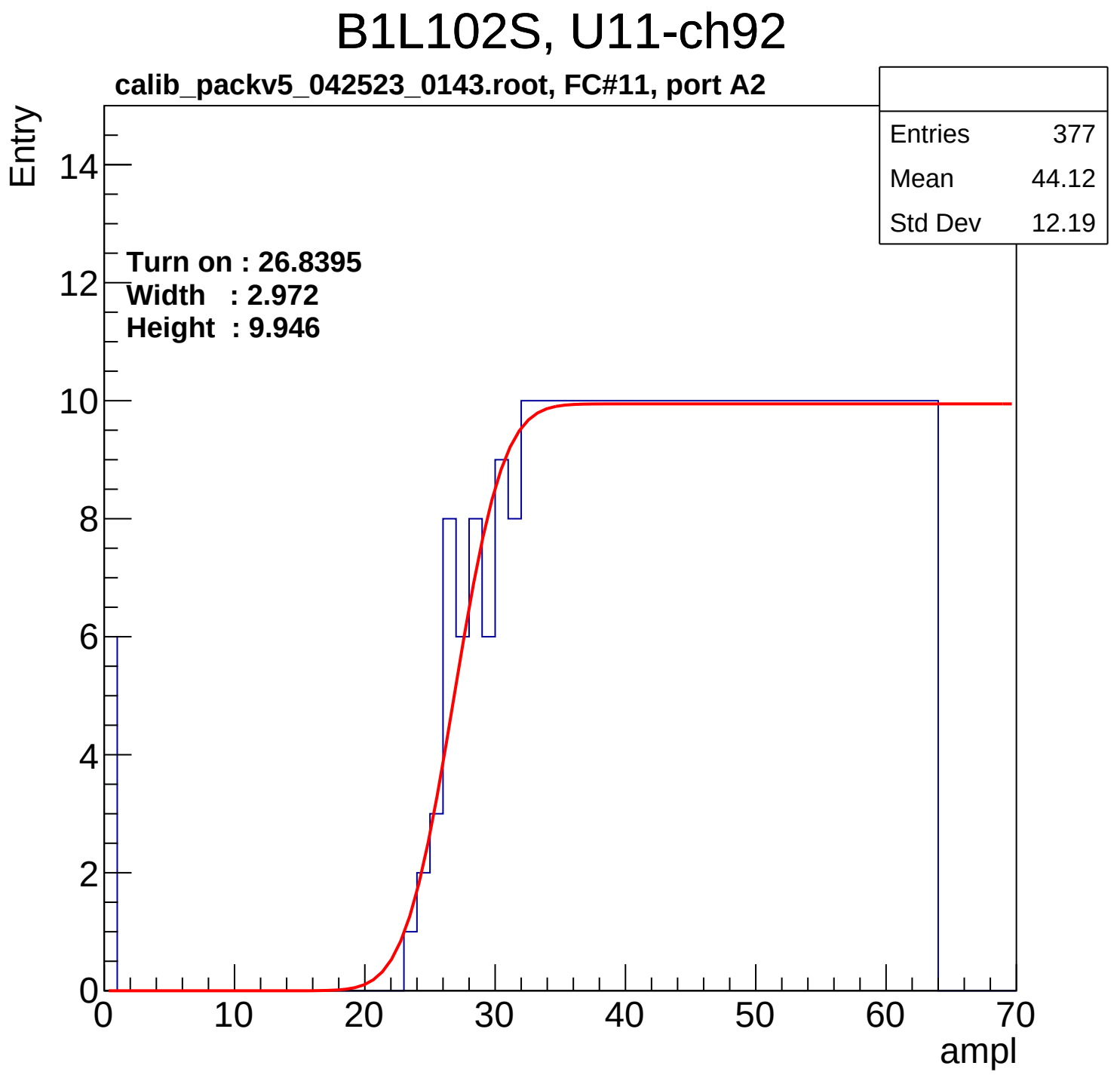
B1L102S, U11-ch92
calib_packv5_042523_0143.root, FC#11, port A2
Entries 377
Mean 44.12
Std Dev 12.19
Turn on : 26.8395
Width : 2.972
Height : 9.946
Entry
ampl
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2
4
6
8
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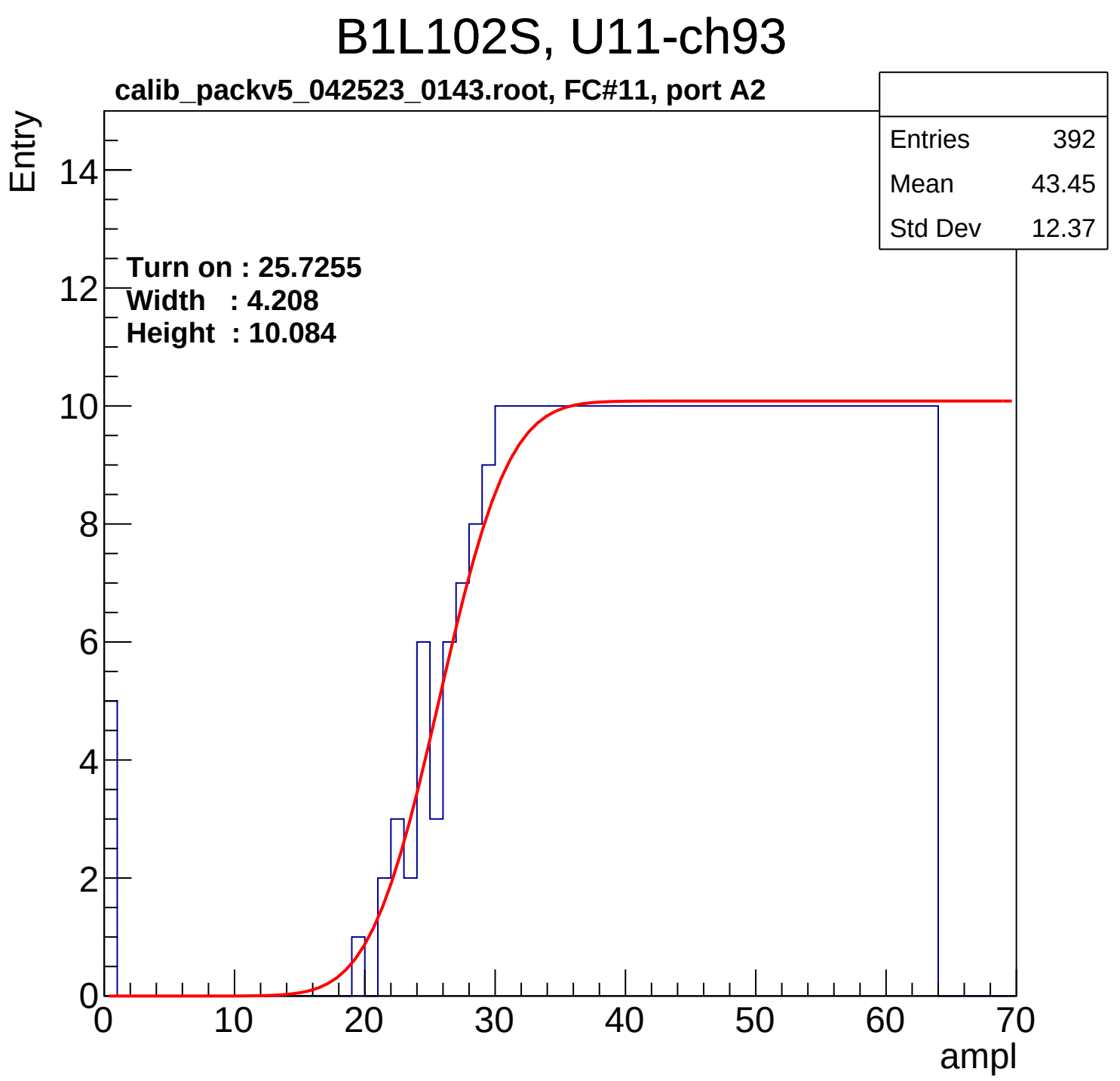
B1L102S, U11-ch93
calib_packv5_042523_0143.root, FC#11, port A2
Entries 392
Mean 43.45
Std Dev 12.37
Turn on : 25.7255
Width : 4.208
Height : 10.084
Entry
ampl
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8
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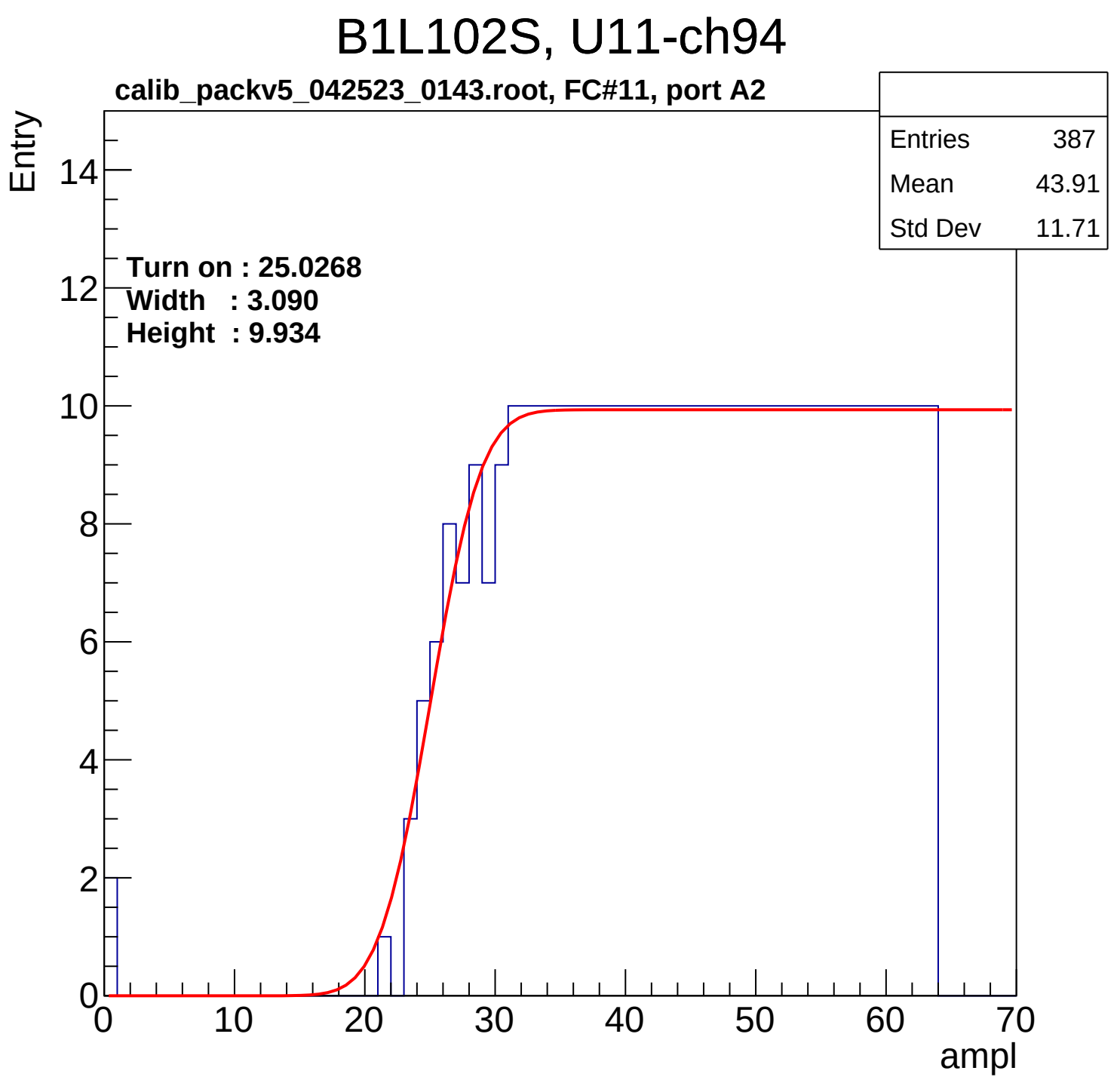
B1L102S, U11-ch94
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 43.91
Std Dev 11.71
Turn on : 25.0268
Width : 3.090
Height : 9.934
Entry
ampl
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2
4
6
8
10
12
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0
10
20
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40
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60
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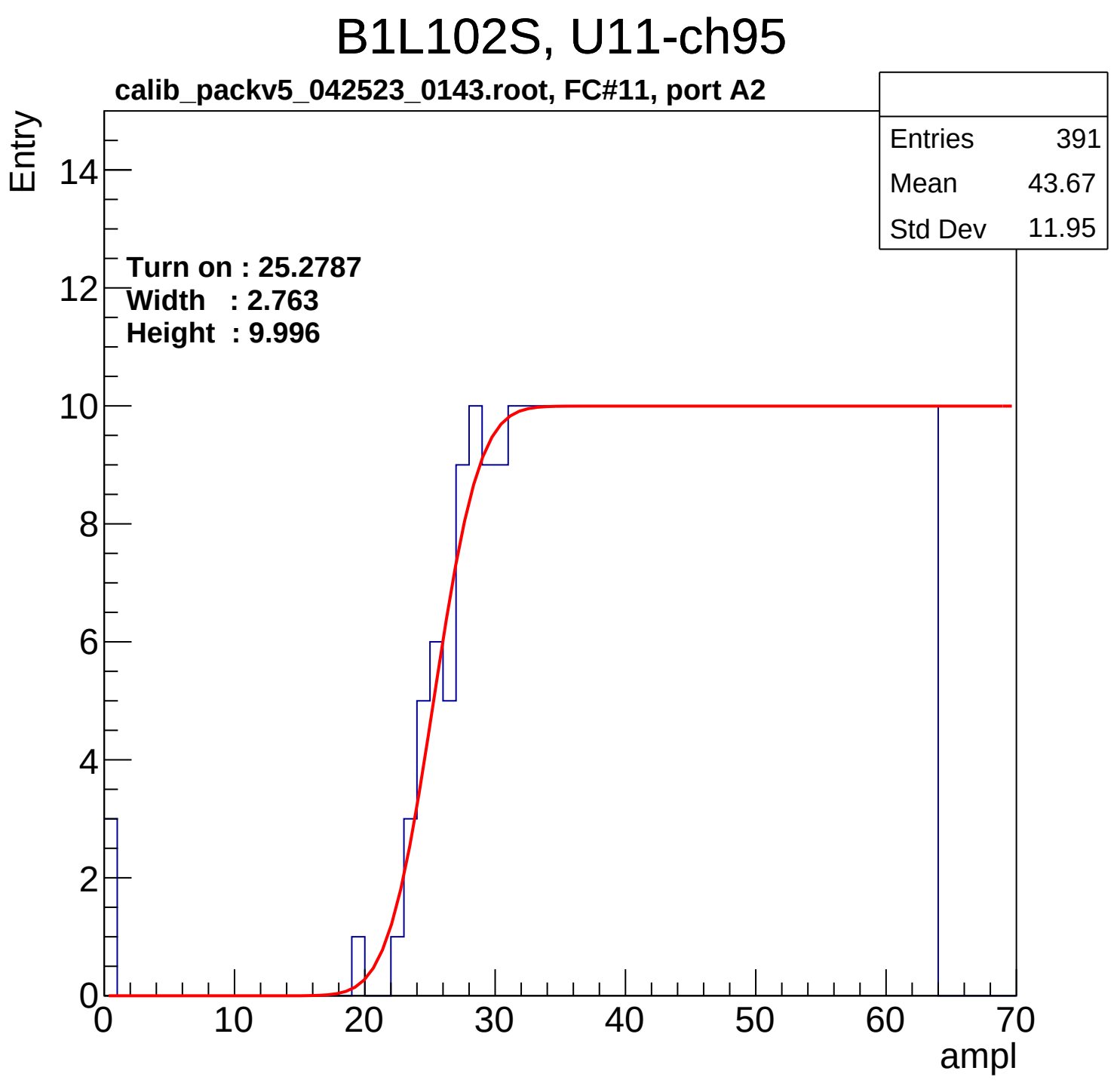
B1L102S, U11-ch95
calib_packv5_042523_0143.root, FC#11, port A2
Entries 391
Mean 43.67
Std Dev 11.95
Turn on : 25.2787
Width : 2.763
Height : 9.996
Entry
ampl
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2
4
6
8
10
12
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0
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60
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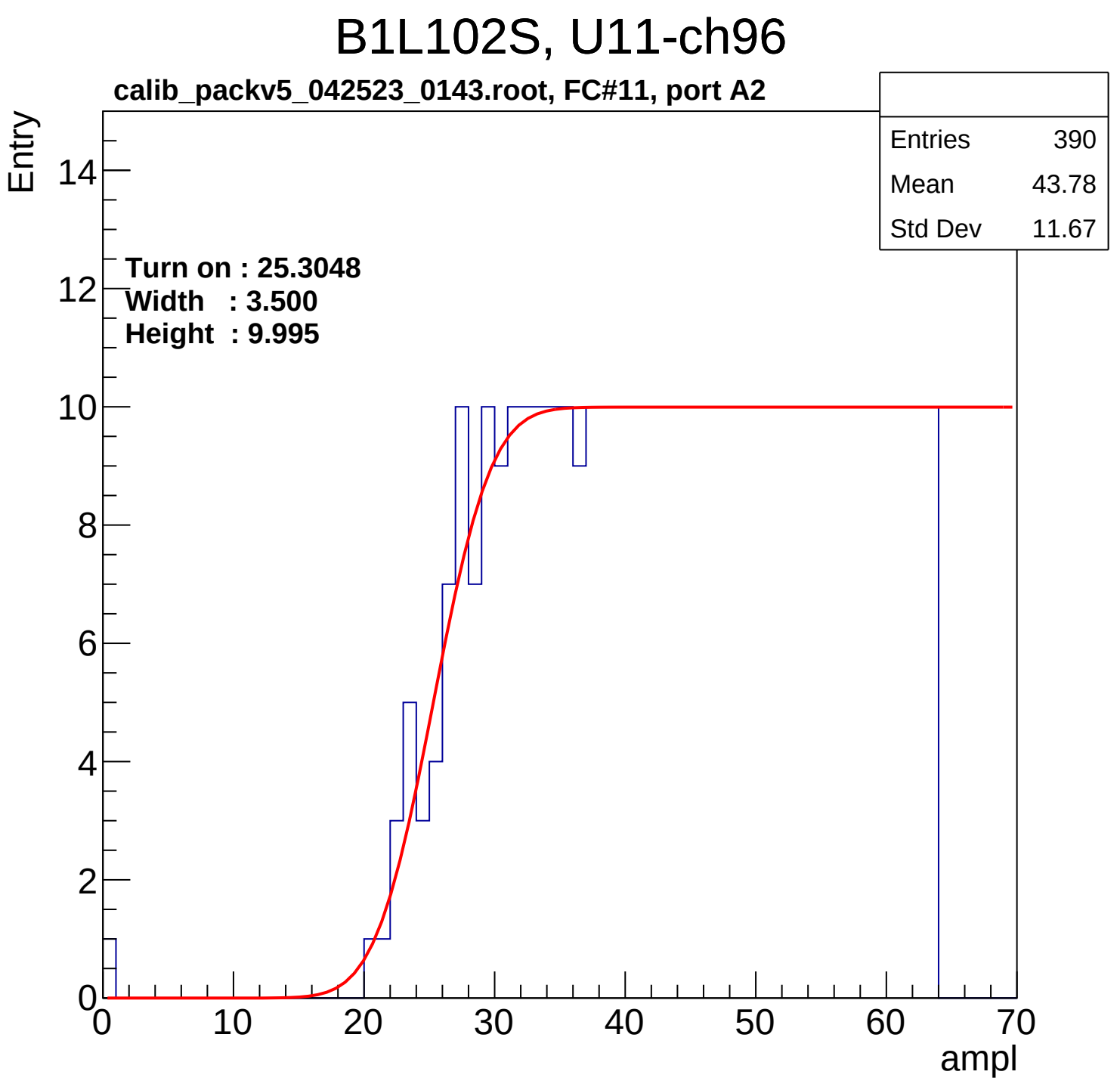
B1L102S, U11-ch96
calib_packv5_042523_0143.root, FC#11, port A2
Entries 390
Mean 43.78
Std Dev 11.67
Turn on : 25.3048
Width : 3.500
Height : 9.995
Entry
ampl
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6
8
10
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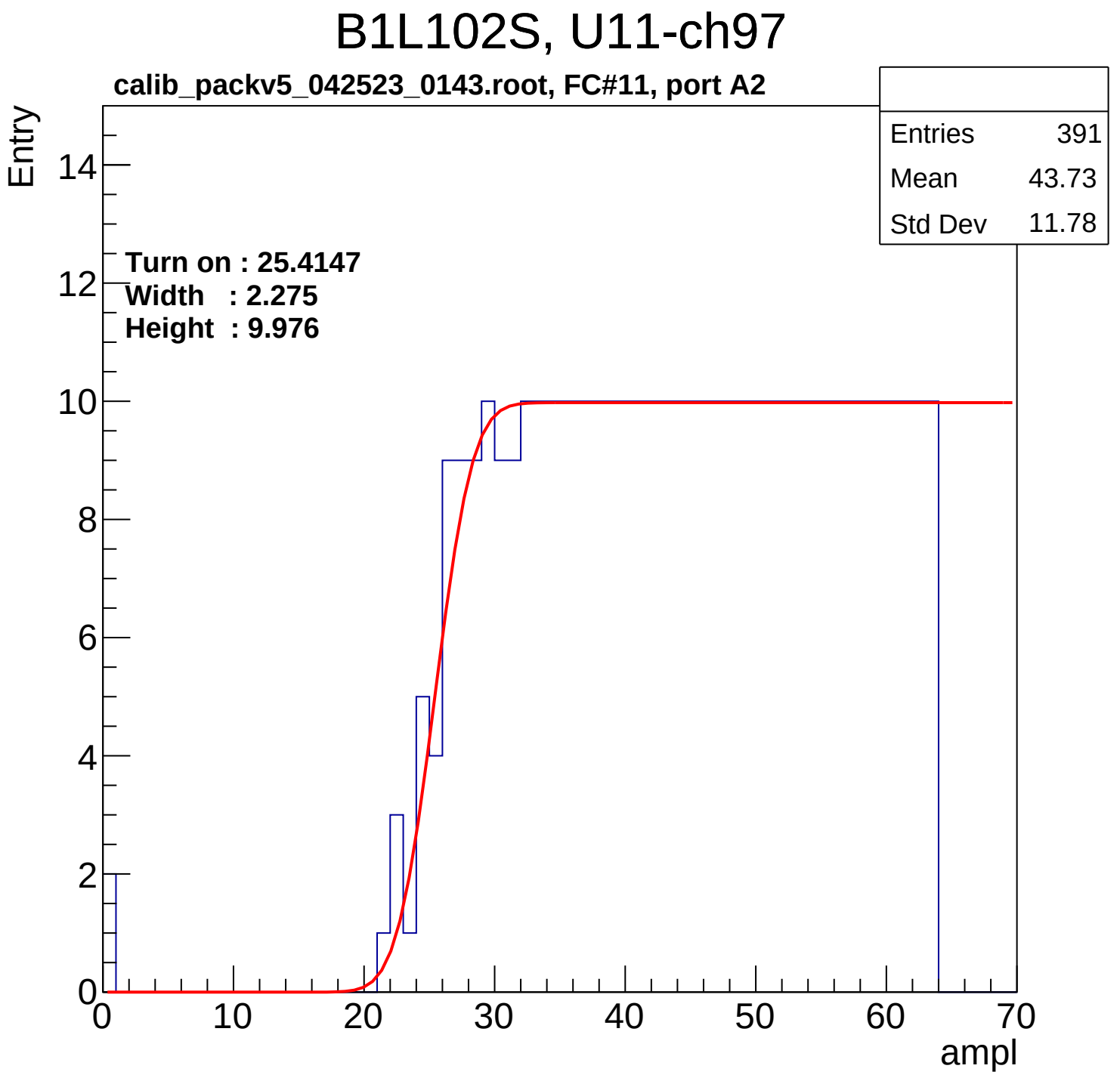
B1L102S, U11-ch97
calib_packv5_042523_0143.root, FC#11, port A2
Entries 391
Mean 43.73
Std Dev 11.78
Turn on : 25.4147
Width : 2.275
Height : 9.976
Entry
ampl
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6
8
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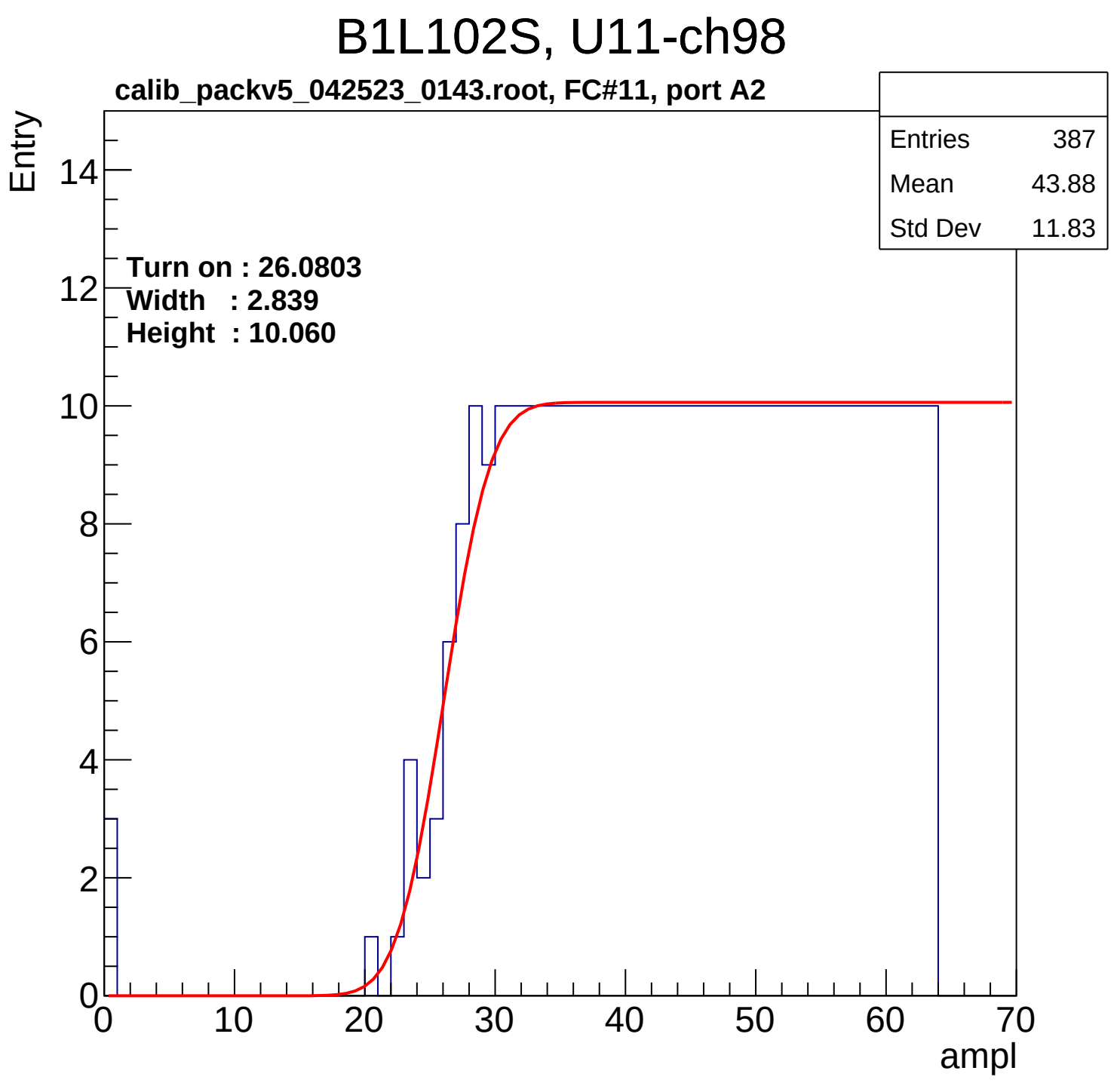
B1L102S, U11-ch98
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 43.88
Std Dev 11.83
Turn on : 26.0803
Width : 2.839
Height : 10.060
Entry
ampl
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6
8
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12
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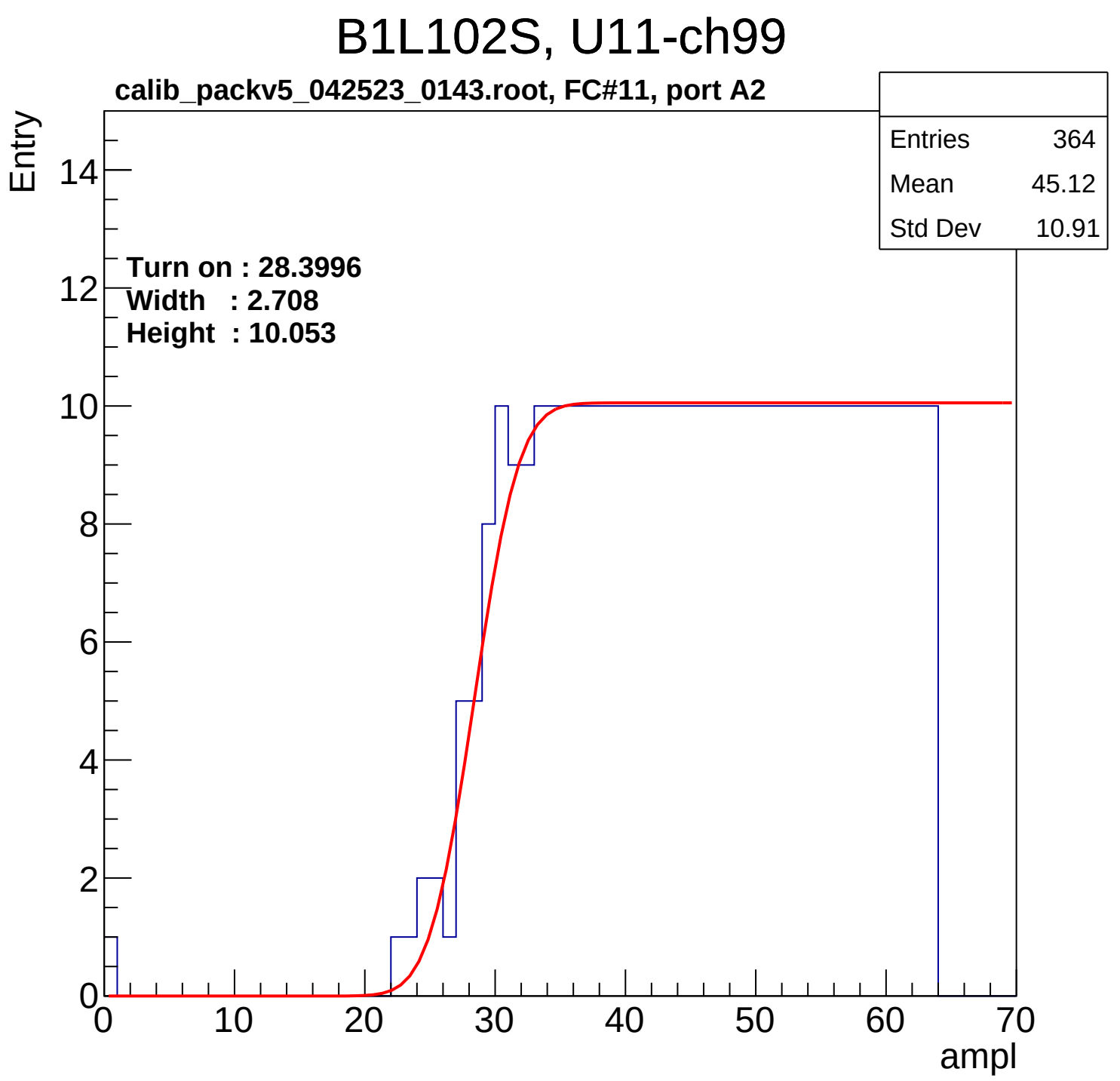
B1L102S, U11-ch99
calib_packv5_042523_0143.root, FC#11, port A2
Entries 364
Mean 45.12
Std Dev 10.91
Turn on : 28.3996
Width : 2.708
Height : 10.053
Entry
ampl
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6
8
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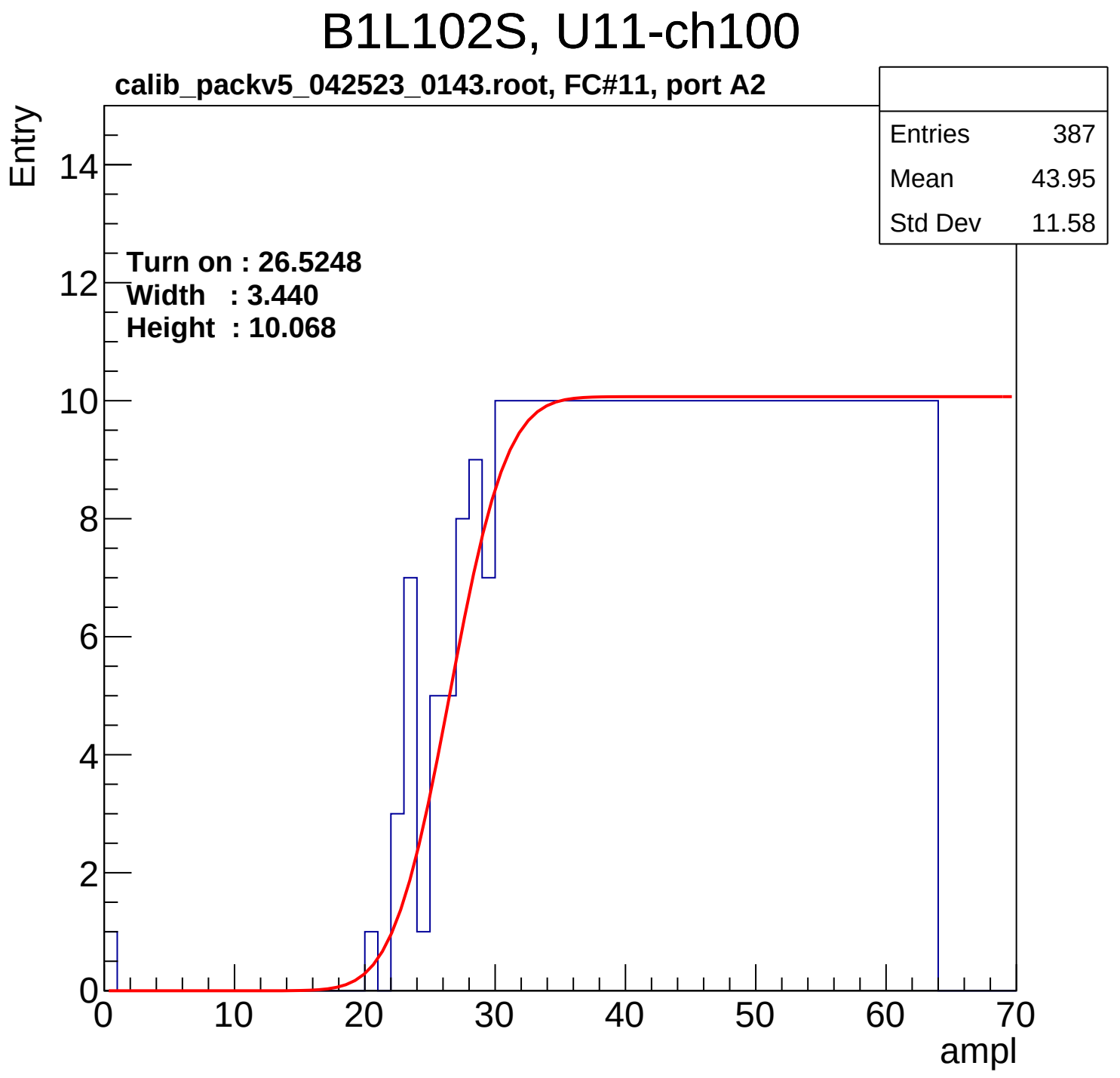
B1L102S, U11-ch100
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 43.95
Std Dev 11.58
Turn on : 26.5248
Width : 3.440
Height : 10.068
Entry
ampl
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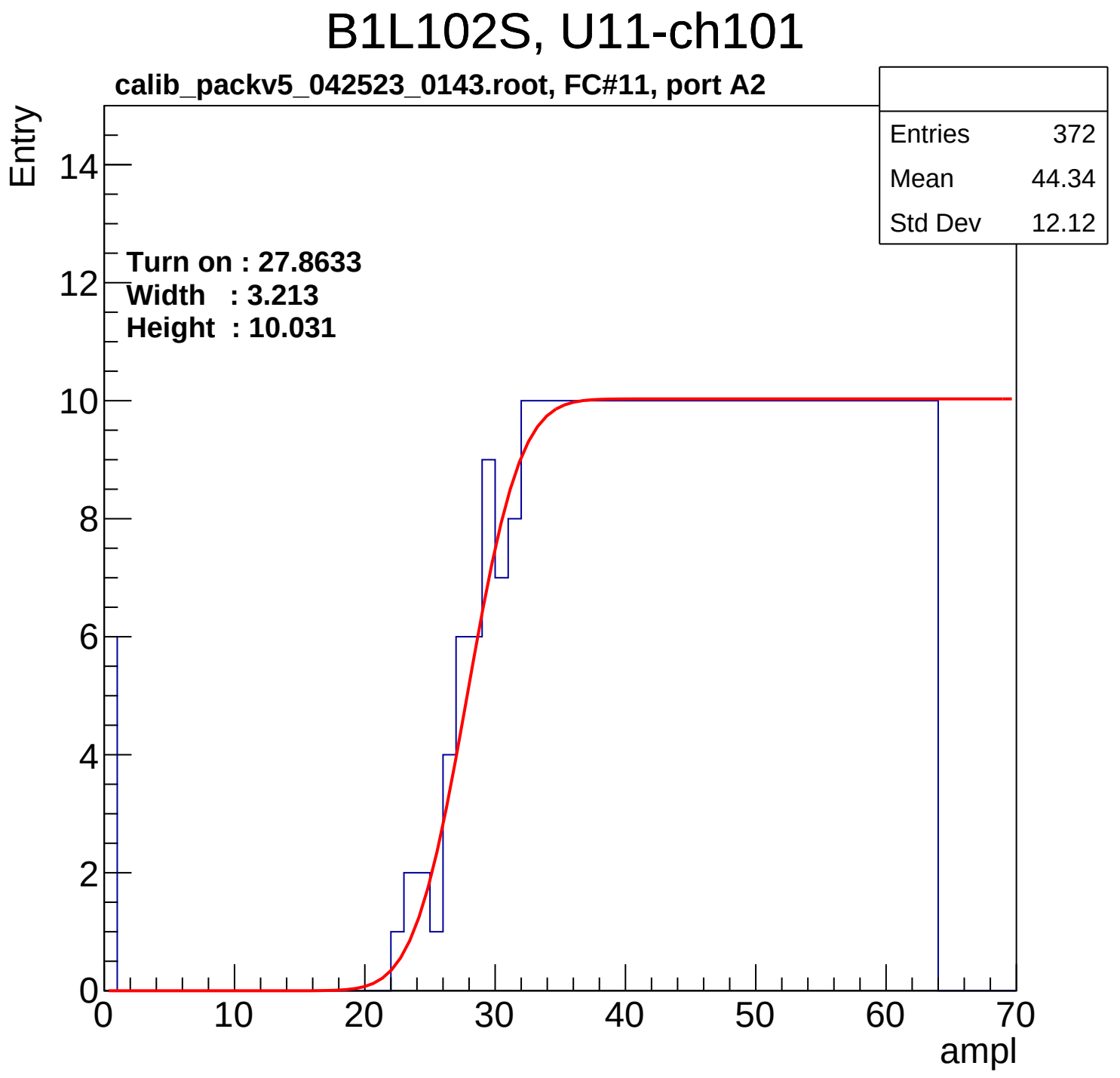
B1L102S, U11-ch101
calib_packv5_042523_0143.root, FC#11, port A2
Entries 372
Mean 44.34
Std Dev 12.12
Turn on : 27.8633
Width : 3.213
Height : 10.031
Entry
ampl
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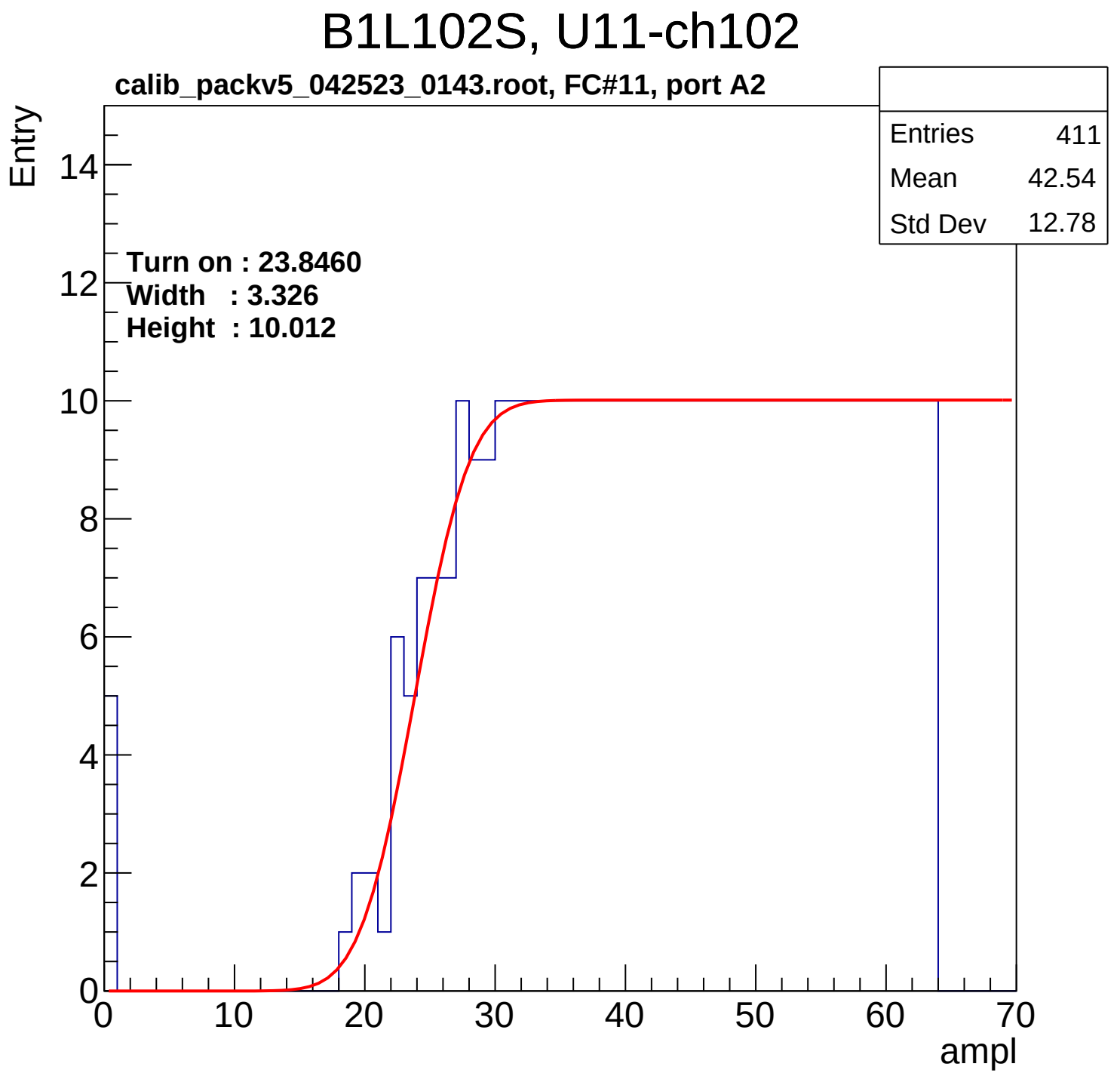
B1L102S, U11-ch102
calib_packv5_042523_0143.root, FC#11, port A2
Entries 411
Mean 42.54
Std Dev 12.78
Turn on : 23.8460
Width : 3.326
Height : 10.012
Entry
ampl
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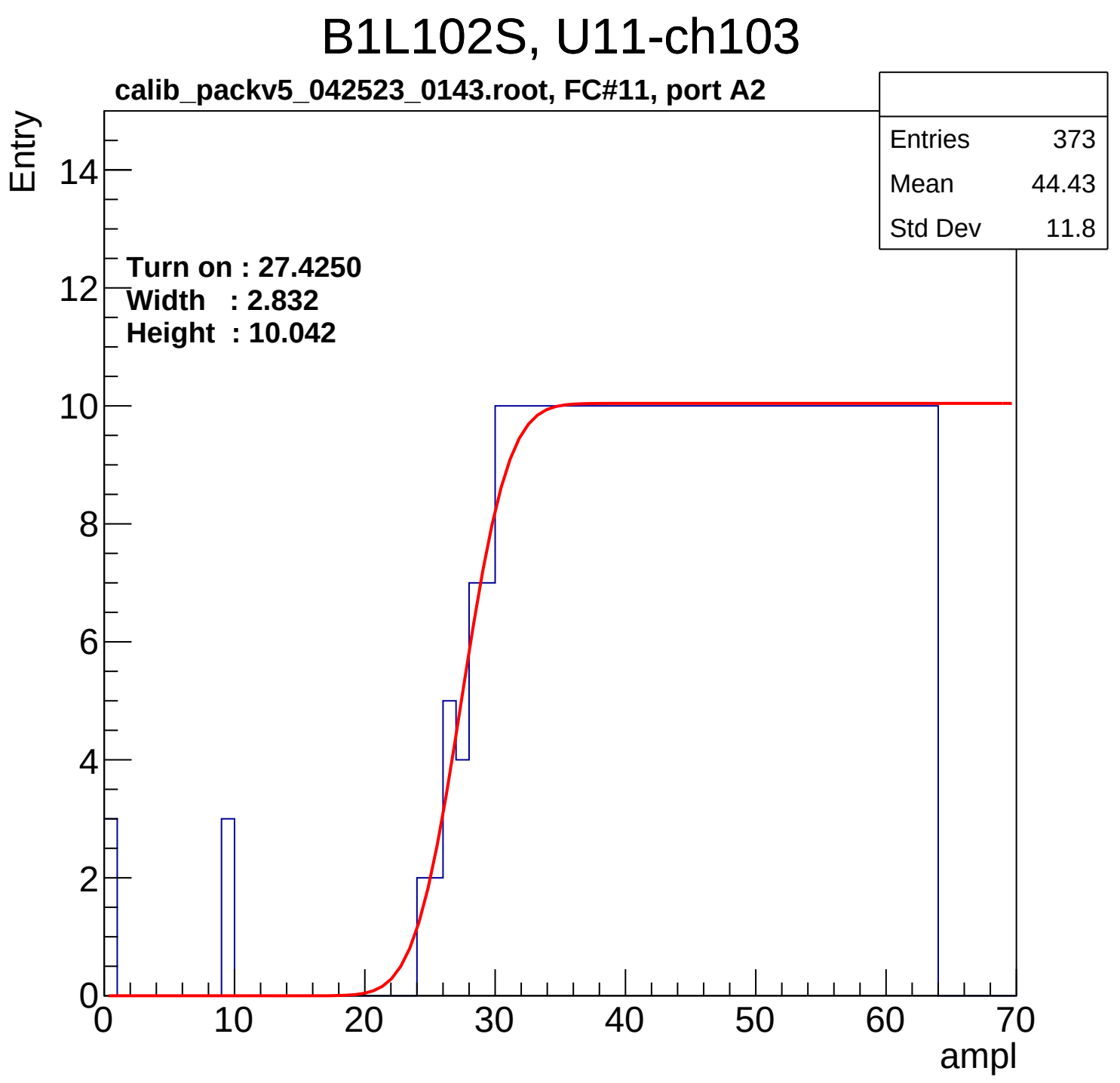
B1L102S, U11-ch103
calib_packv5_042523_0143.root, FC#11, port A2
Entries 373
Mean 44.43
Std Dev 11.8
Turn on : 27.4250
Width : 2.832
Height : 10.042
Entry
ampl
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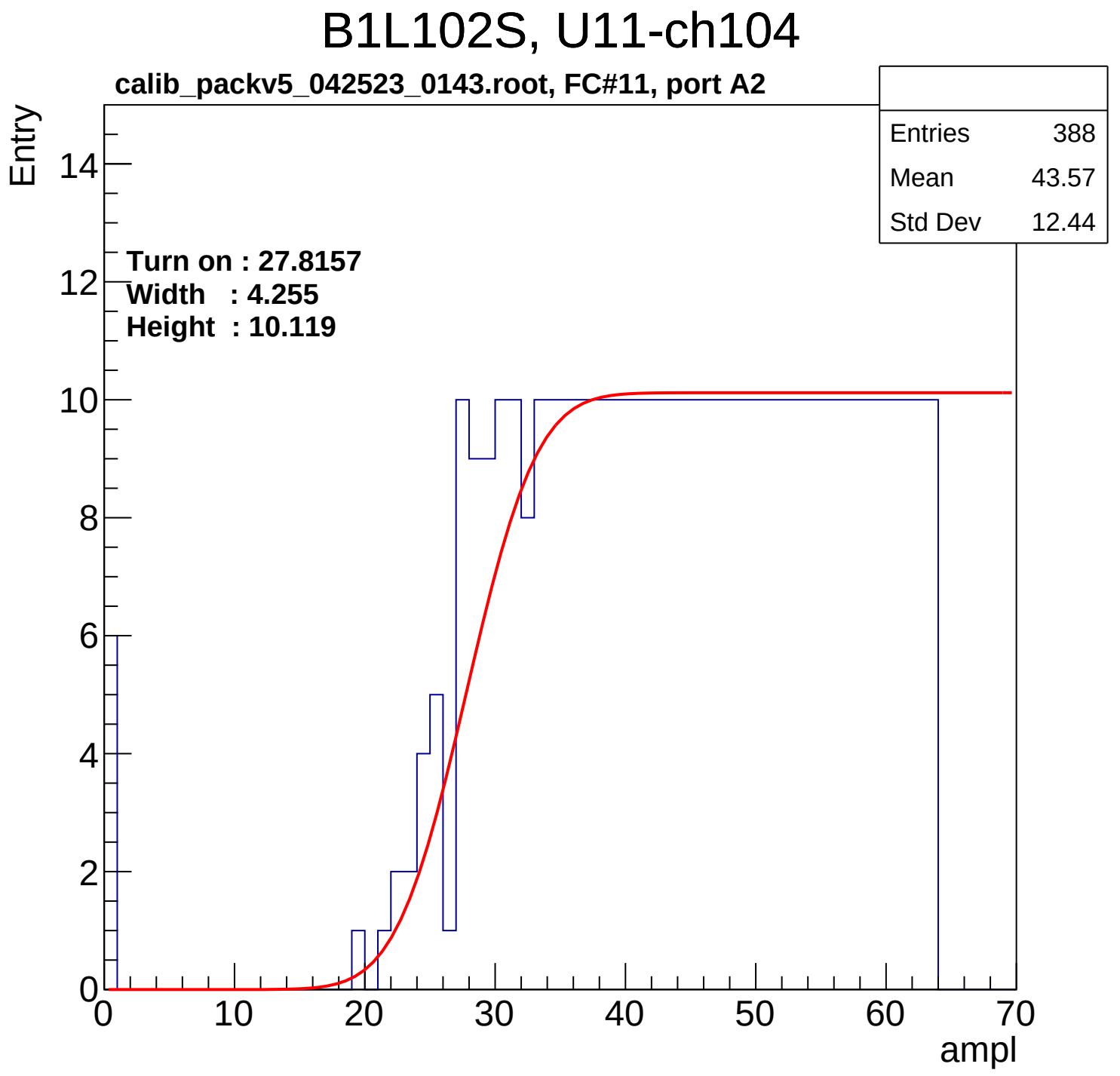
B1L102S, U11-ch104
calib_packv5_042523_0143.root, FC#11, port A2
Entries 388
Mean 43.57
Std Dev 12.44
Turn on : 27.8157
Width : 4.255
Height : 10.119
Entry
ampl
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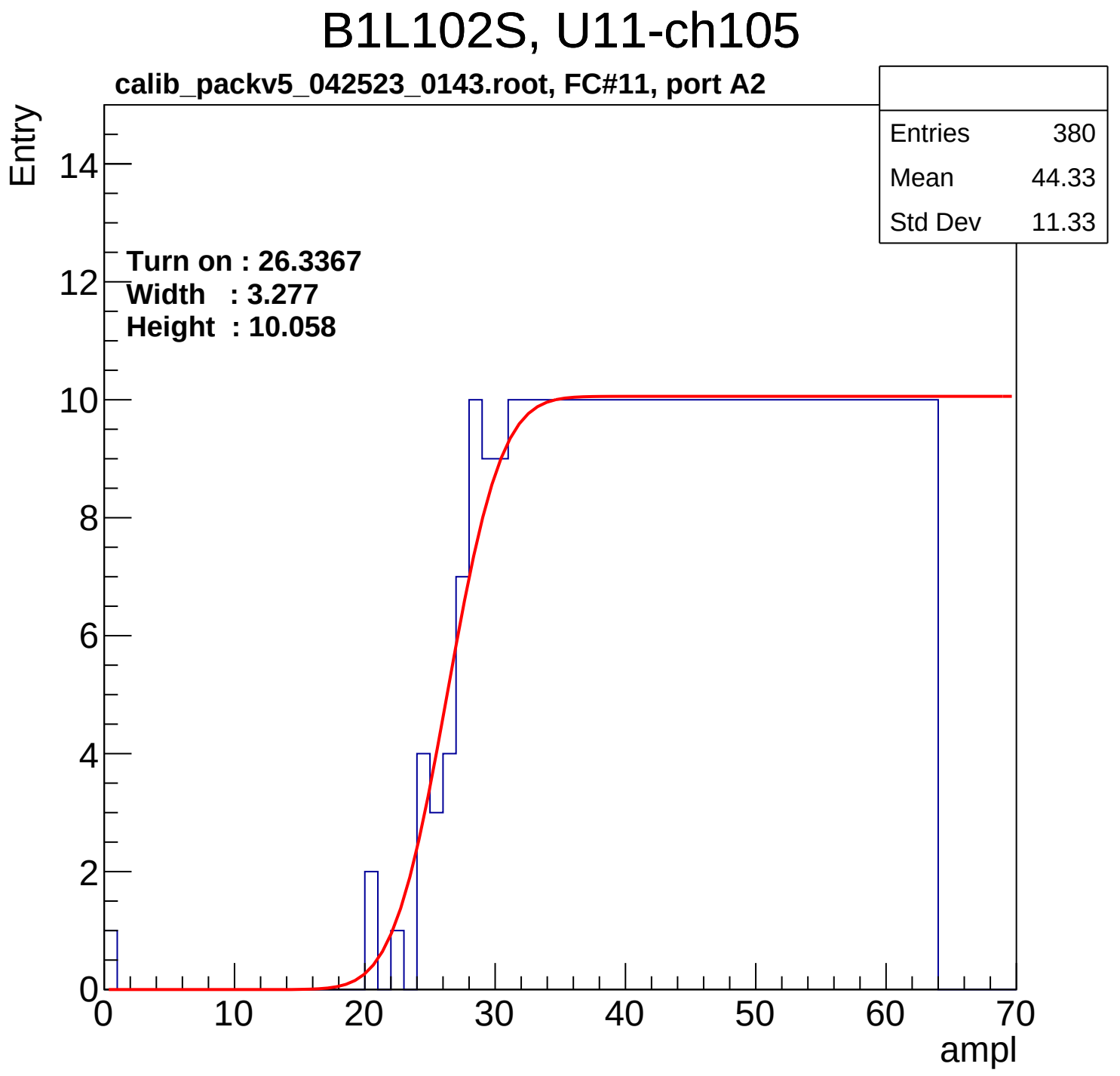
B1L102S, U11-ch105
calib_packv5_042523_0143.root, FC#11, port A2
Entries 380
Mean 44.33
Std Dev 11.33
Turn on : 26.3367
Width : 3.277
Height : 10.058
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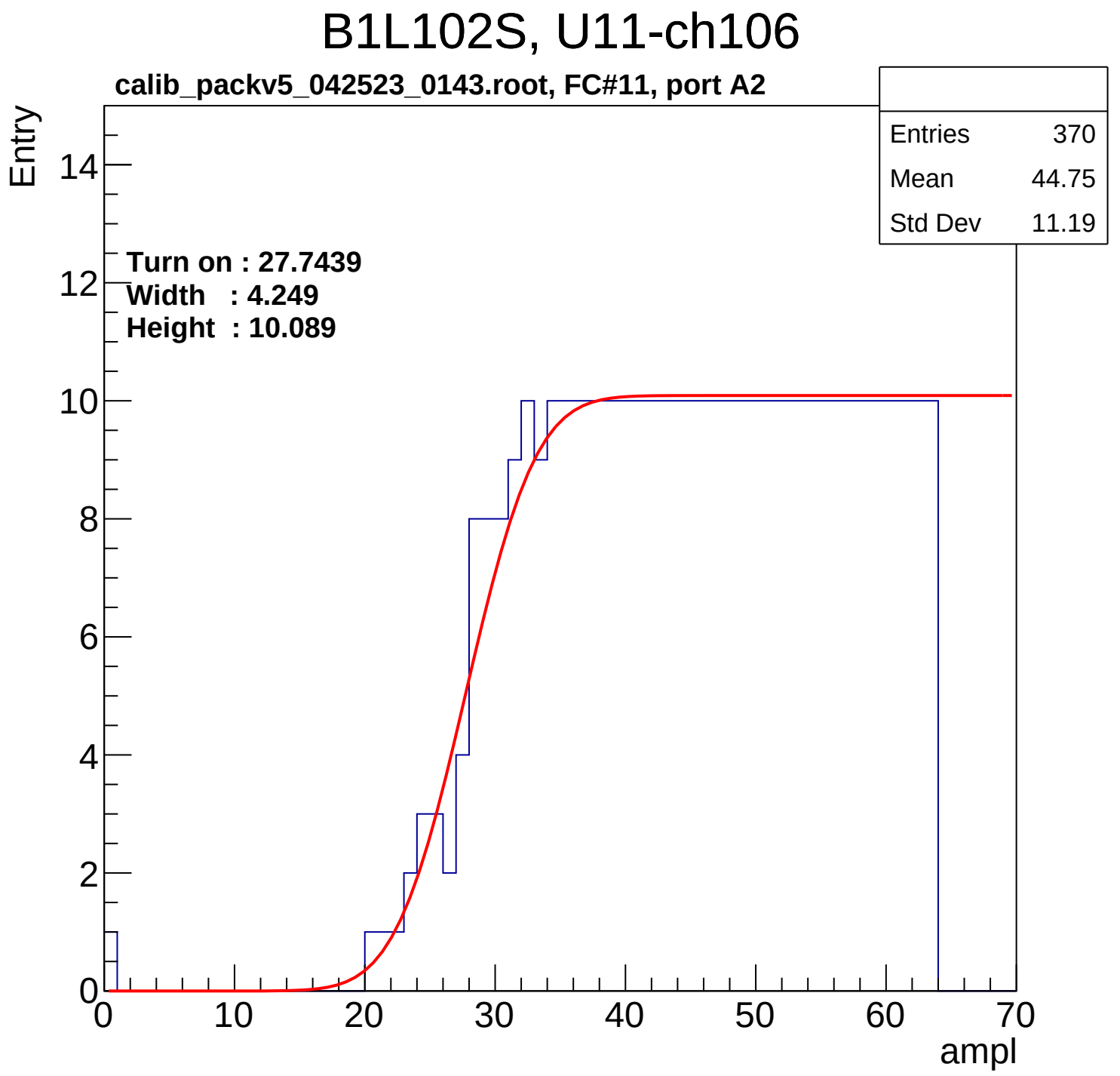
B1L102S, U11-ch106
calib_packv5_042523_0143.root, FC#11, port A2
Entries 370
Mean 44.75
Std Dev 11.19
Turn on : 27.7439
Width : 4.249
Height : 10.089
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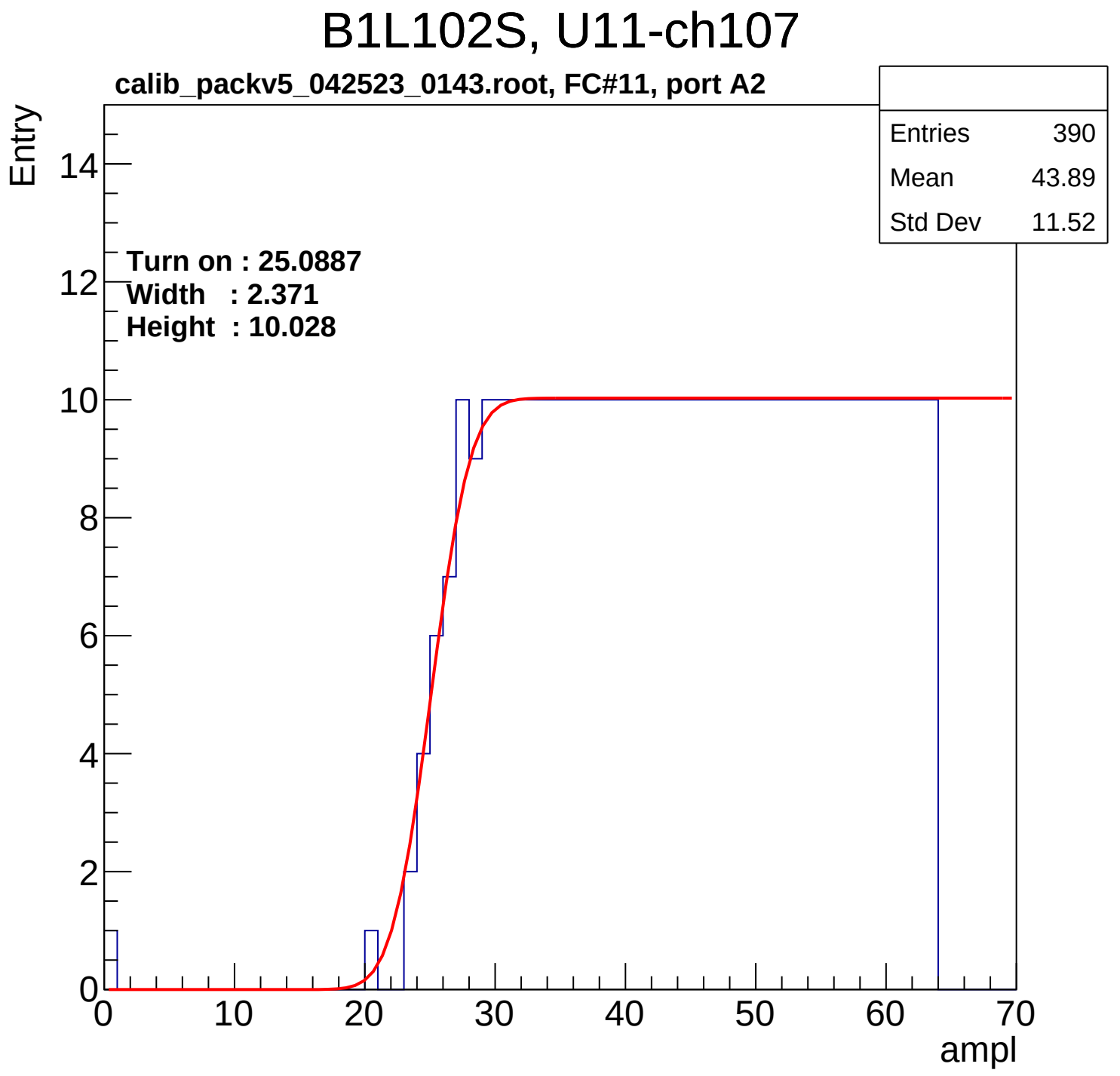
B1L102S, U11-ch107
calib_packv5_042523_0143.root, FC#11, port A2
Entries 390
Mean 43.89
Std Dev 11.52
Turn on : 25.0887
Width : 2.371
Height : 10.028
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ampl
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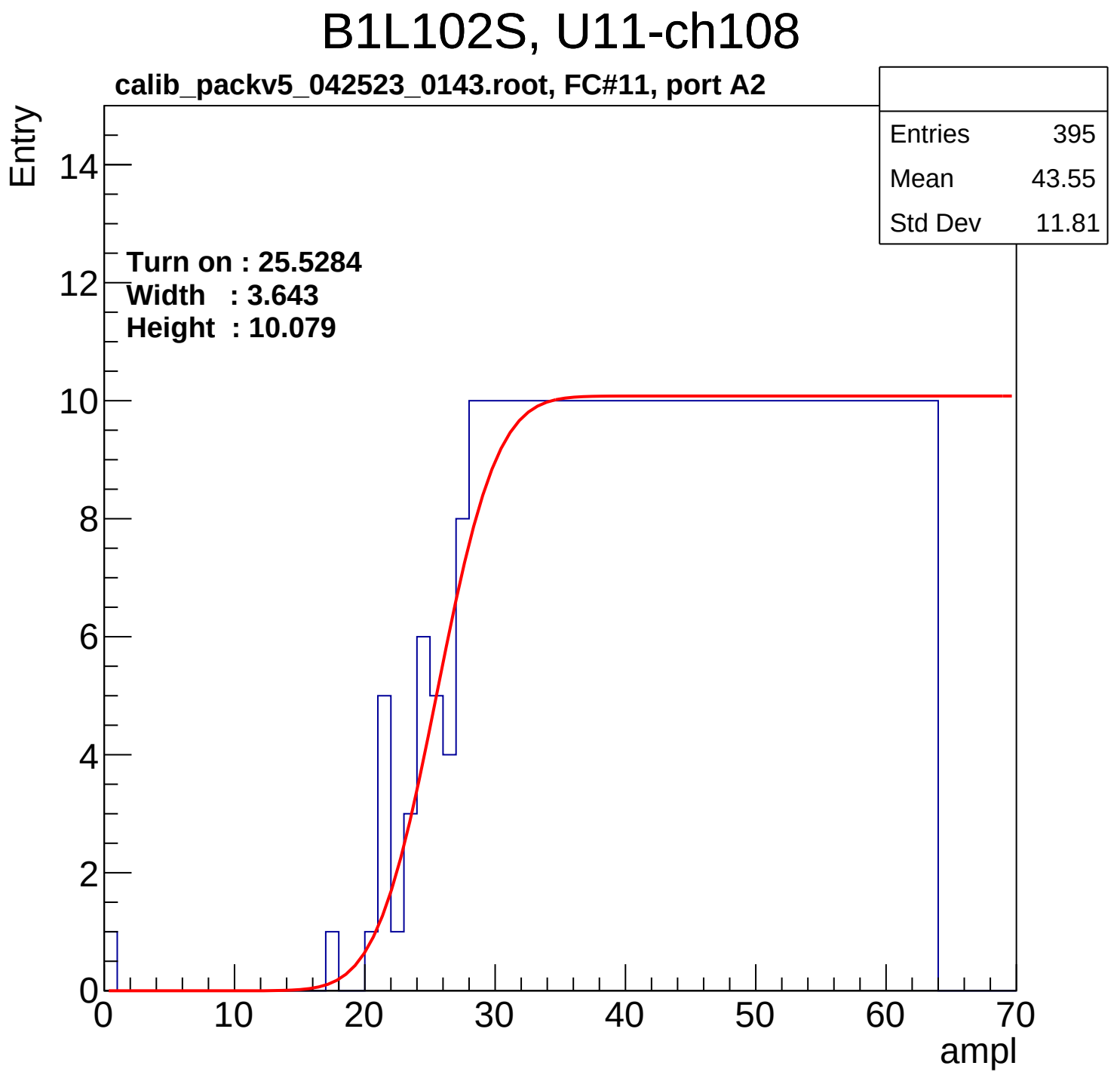
B1L102S, U11-ch108
calib_packv5_042523_0143.root, FC#11, port A2
Entries 395
Mean 43.55
Std Dev 11.81
Turn on : 25.5284
Width : 3.643
Height : 10.079
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ampl
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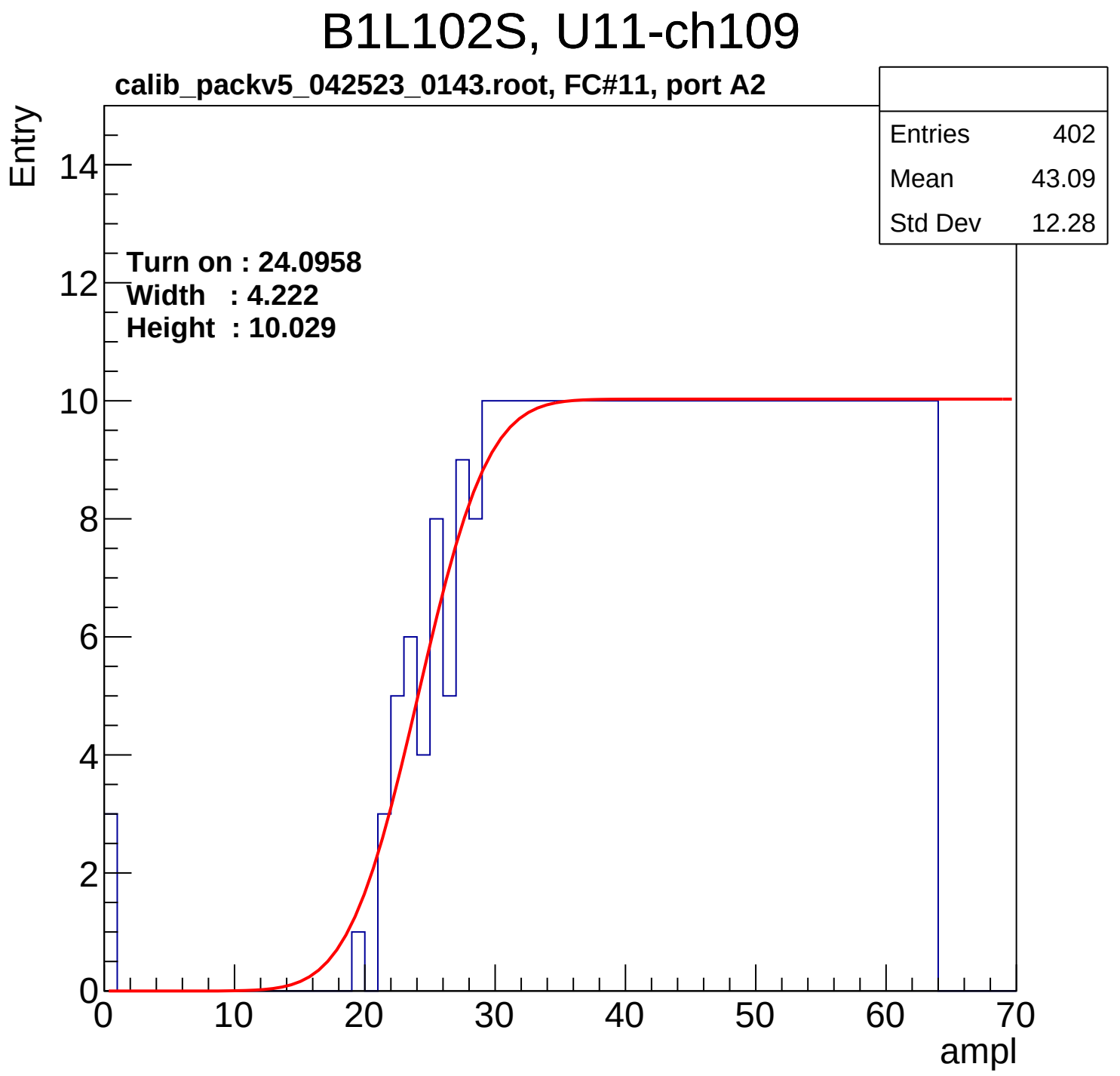
B1L102S, U11-ch109
calib_packv5_042523_0143.root, FC#11, port A2
Entries 402
Mean 43.09
Std Dev 12.28
Turn on : 24.0958
Width : 4.222
Height : 10.029
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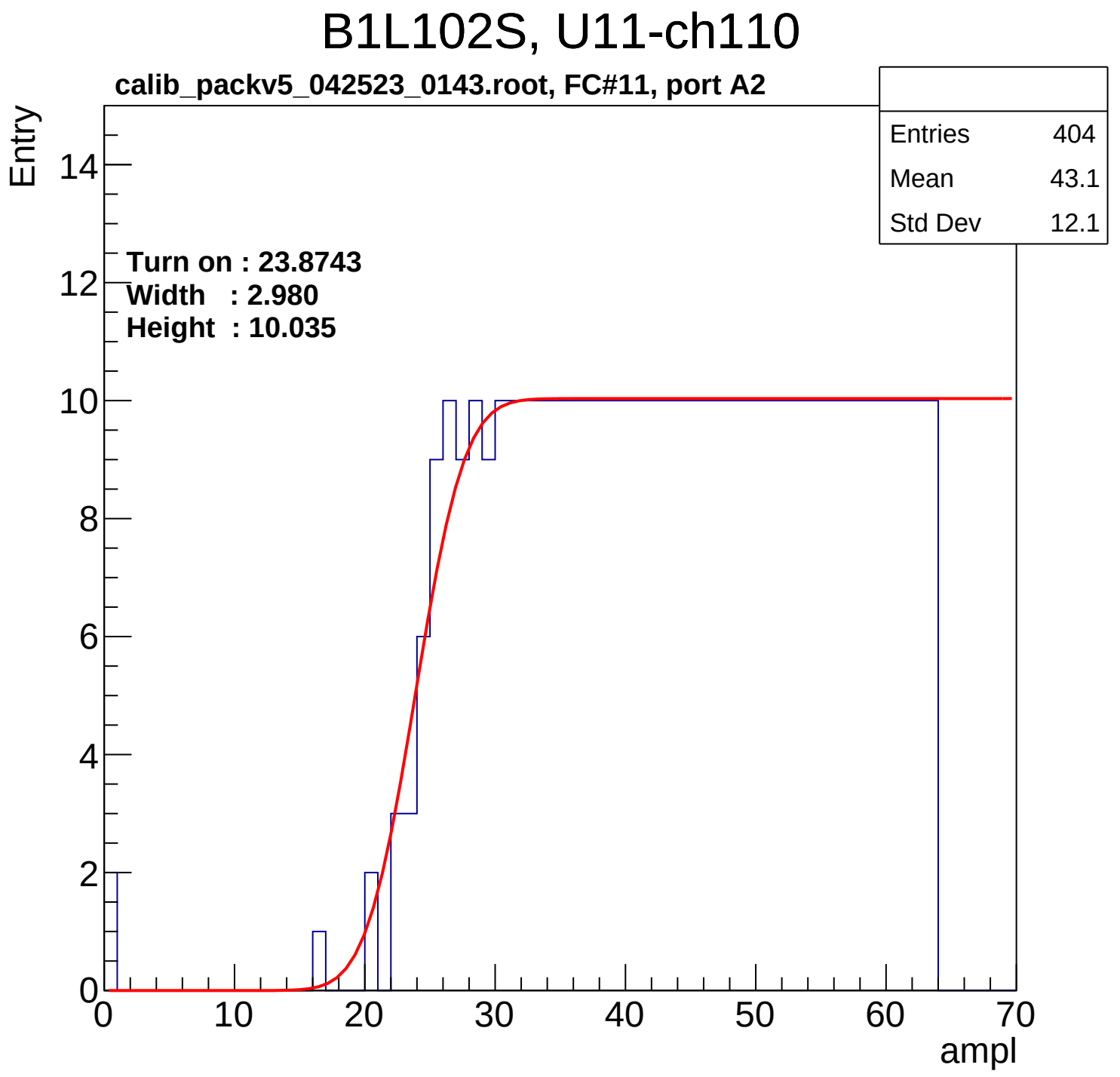
B1L102S, U11-ch110
calib_packv5_042523_0143.root, FC#11, port A2
Entries 404
Mean 43.1
Std Dev 12.1
Turn on : 23.8743
Width : 2.980
Height : 10.035
Entry
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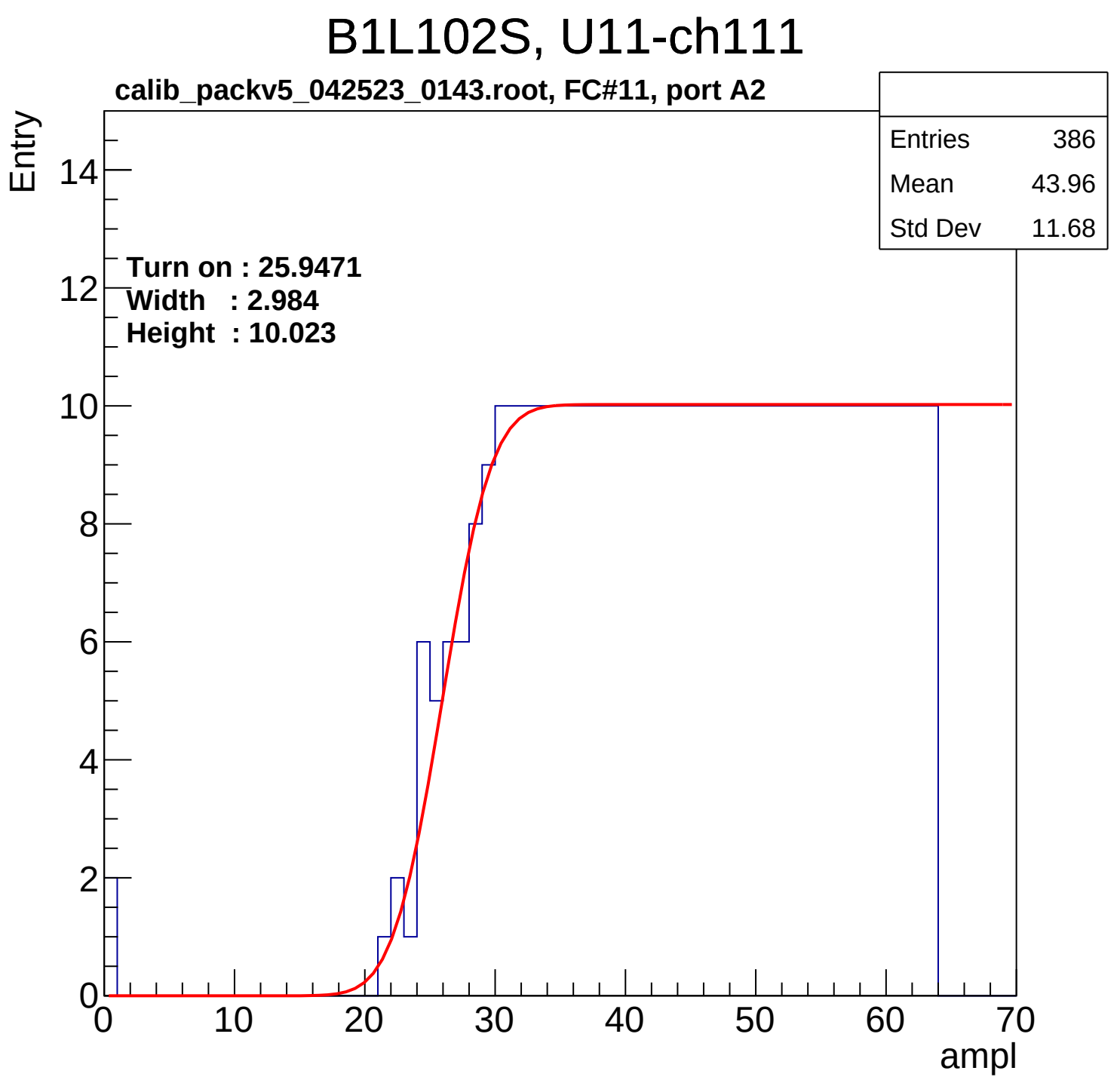
B1L102S, U11-ch111
calib_packv5_042523_0143.root, FC#11, port A2
Entries 386
Mean 43.96
Std Dev 11.68
Turn on : 25.9471
Width : 2.984
Height : 10.023
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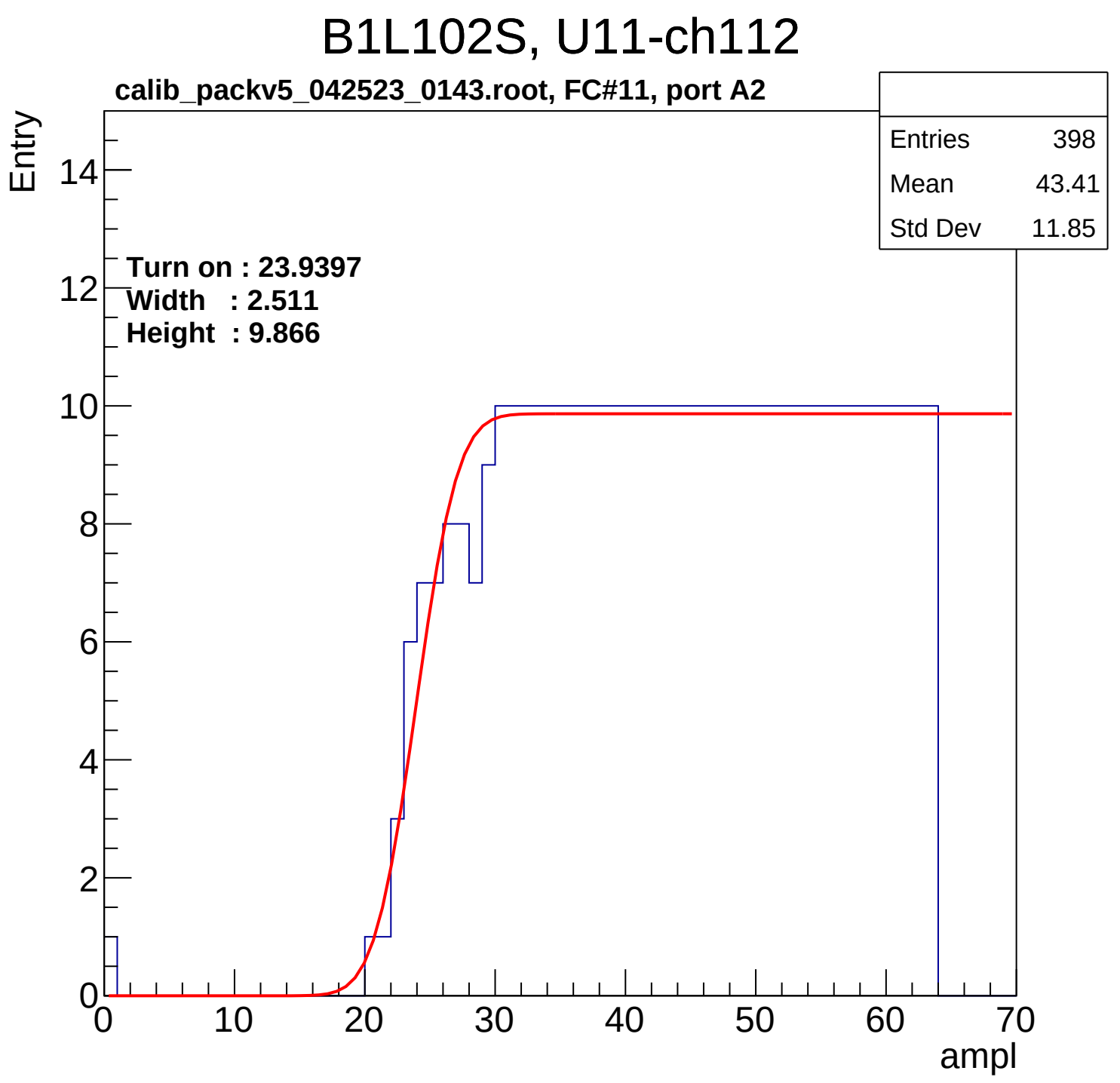
B1L102S, U11-ch112
calib_packv5_042523_0143.root, FC#11, port A2
Entries 398
Mean 43.41
Std Dev 11.85
Turn on : 23.9397
Width : 2.511
Height : 9.866
Entry
ampl
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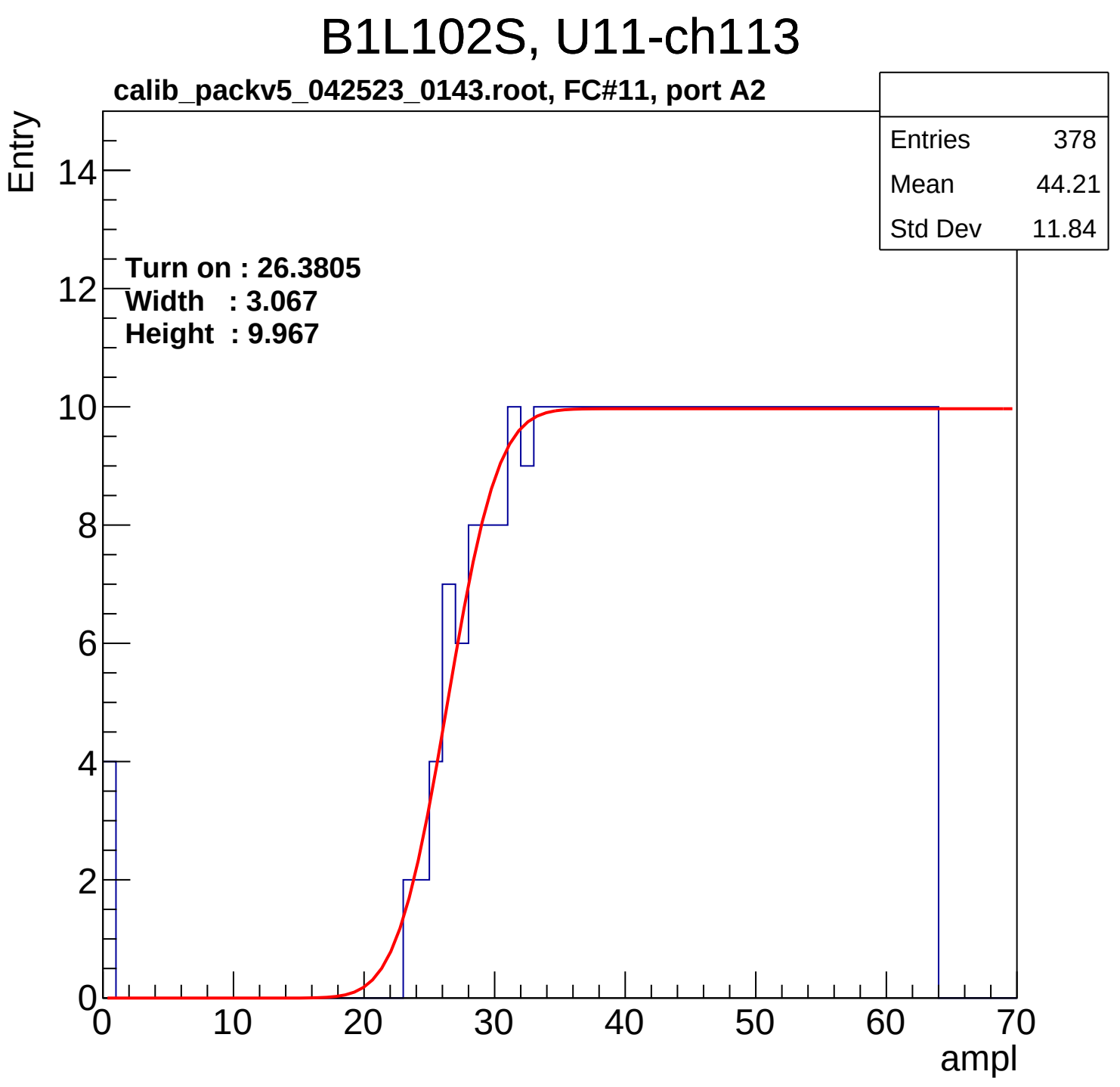
B1L102S, U11-ch113
calib_packv5_042523_0143.root, FC#11, port A2
Entries 378
Mean 44.21
Std Dev 11.84
Turn on : 26.3805
Width : 3.067
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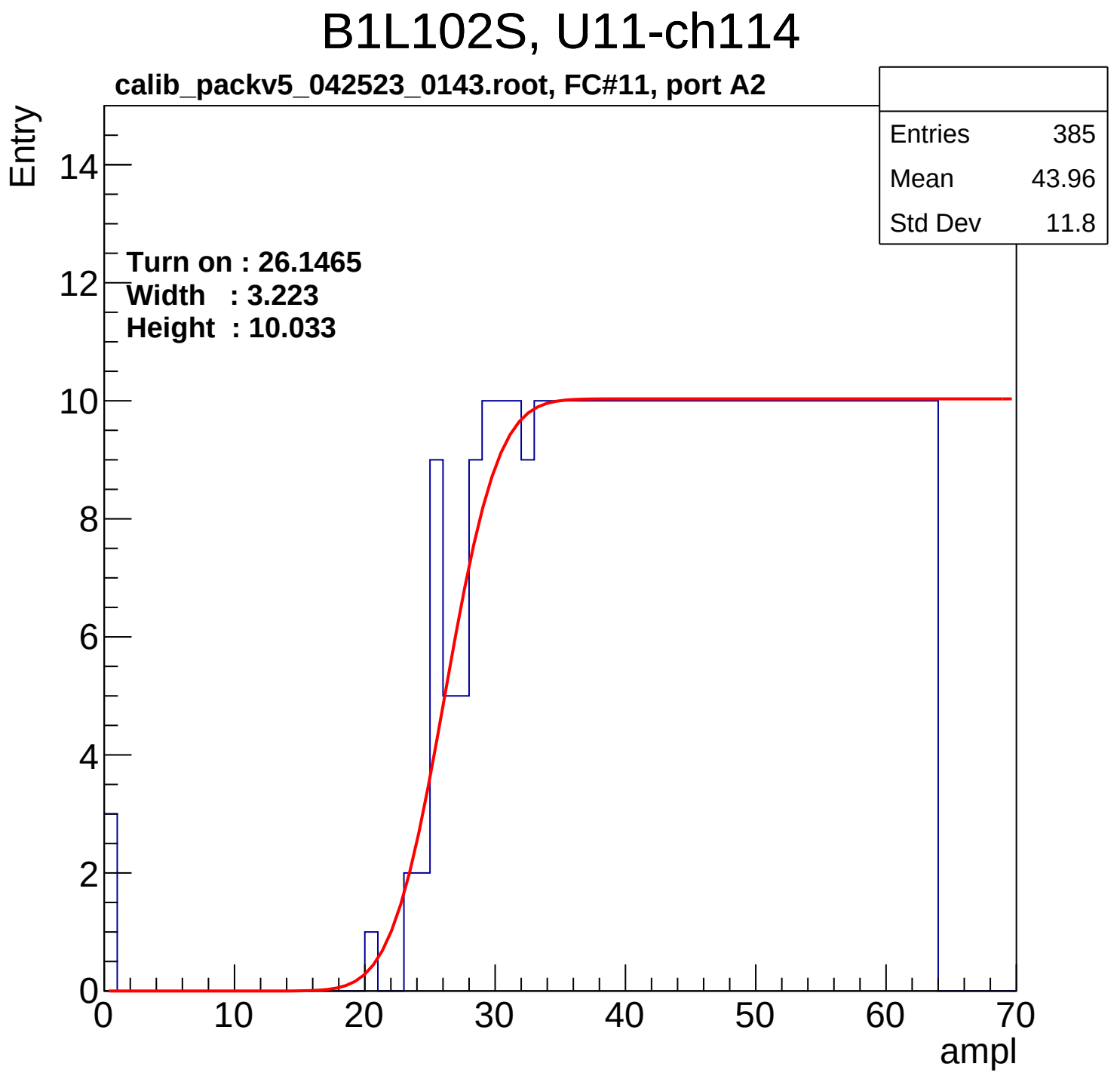
B1L102S, U11-ch114
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 43.96
Std Dev 11.8
Turn on : 26.1465
Width : 3.223
Height : 10.033
Entry
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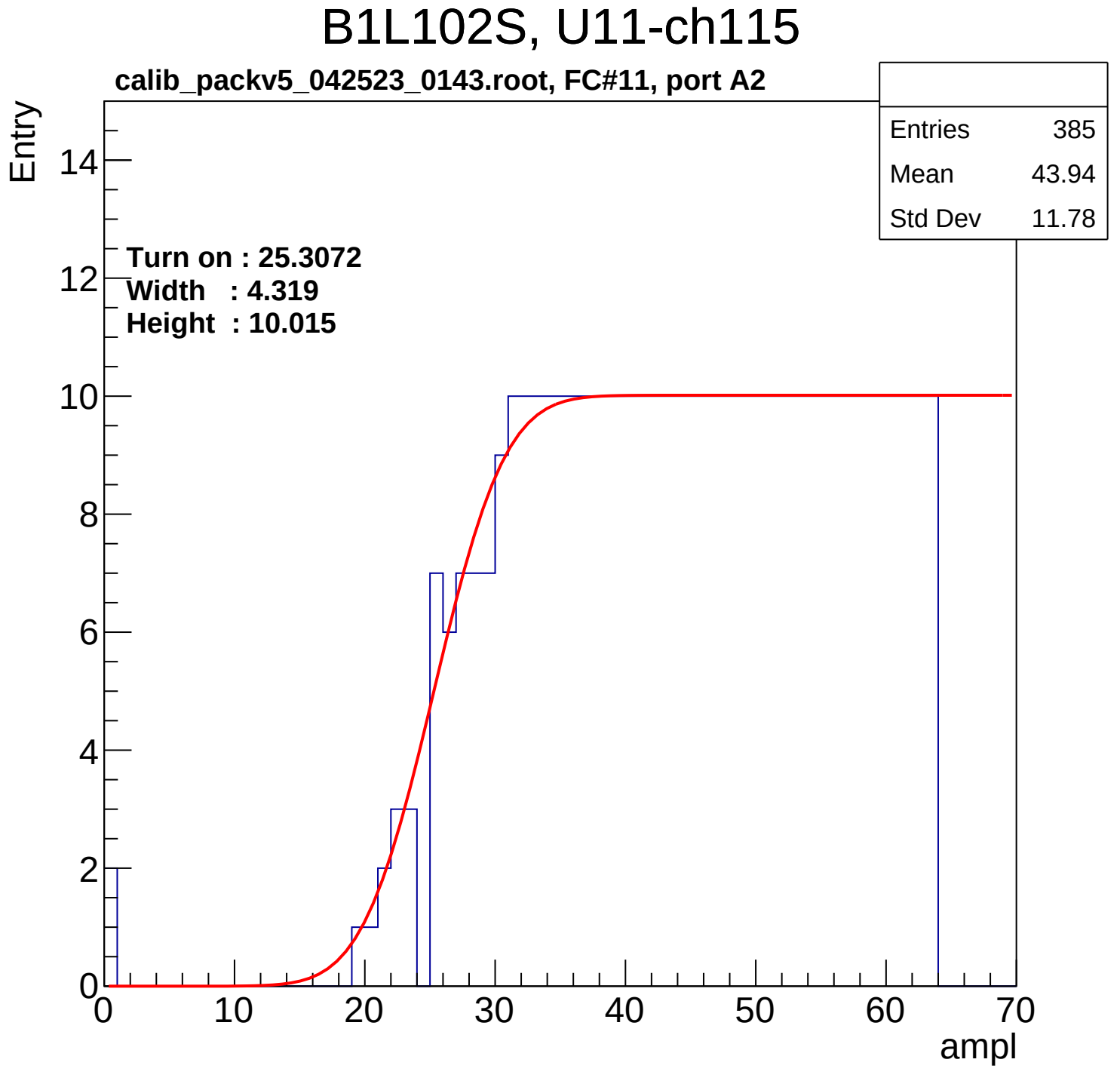
B1L102S, U11-ch115
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 43.94
Std Dev 11.78
Turn on : 25.3072
Width : 4.319
Height : 10.015
Entry
ampl
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6
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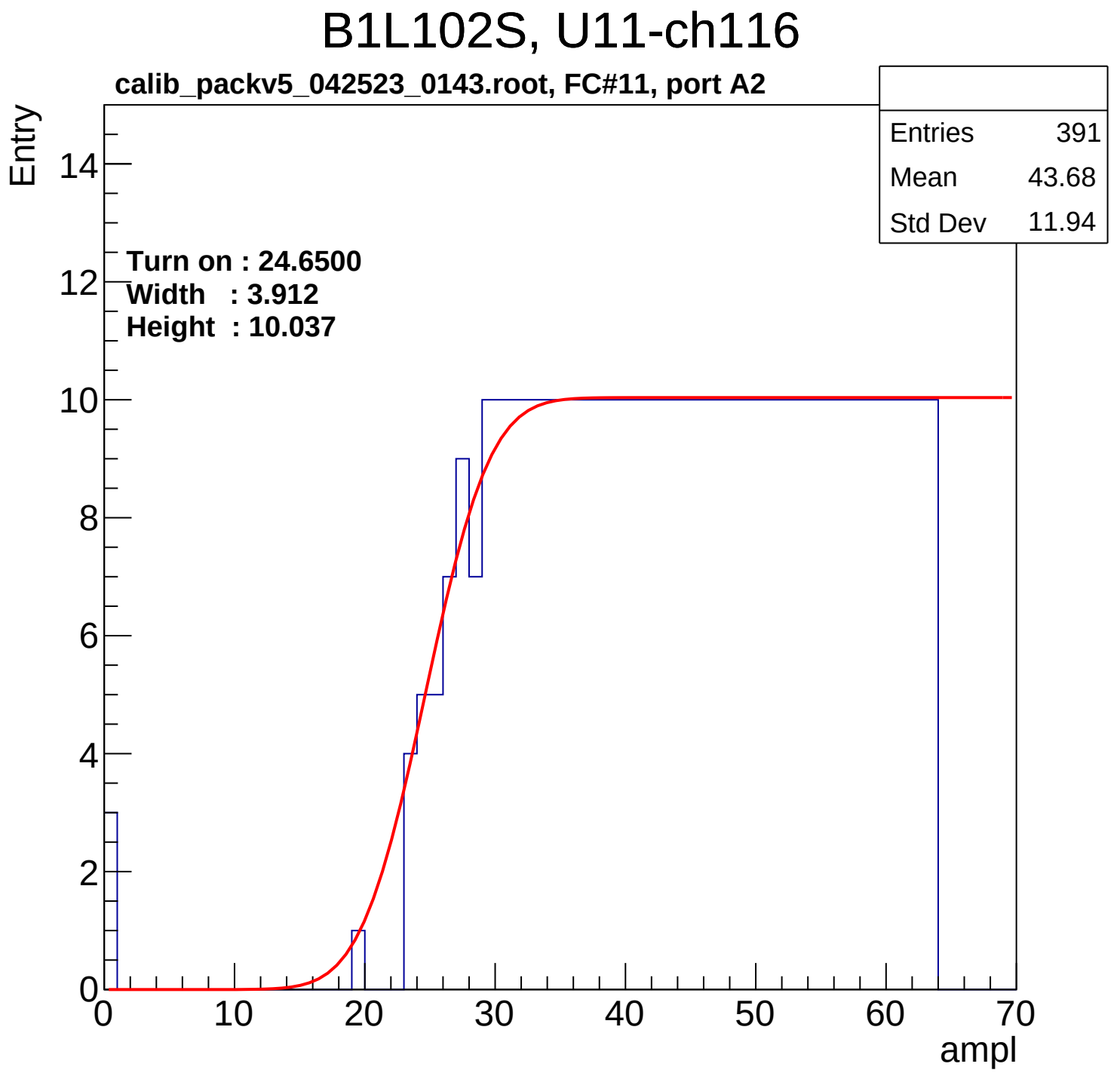
B1L102S, U11-ch116
calib_packv5_042523_0143.root, FC#11, port A2
Entries 391
Mean 43.68
Std Dev 11.94
Turn on : 24.6500
Width : 3.912
Height : 10.037
Entry
ampl
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2
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8
10
12
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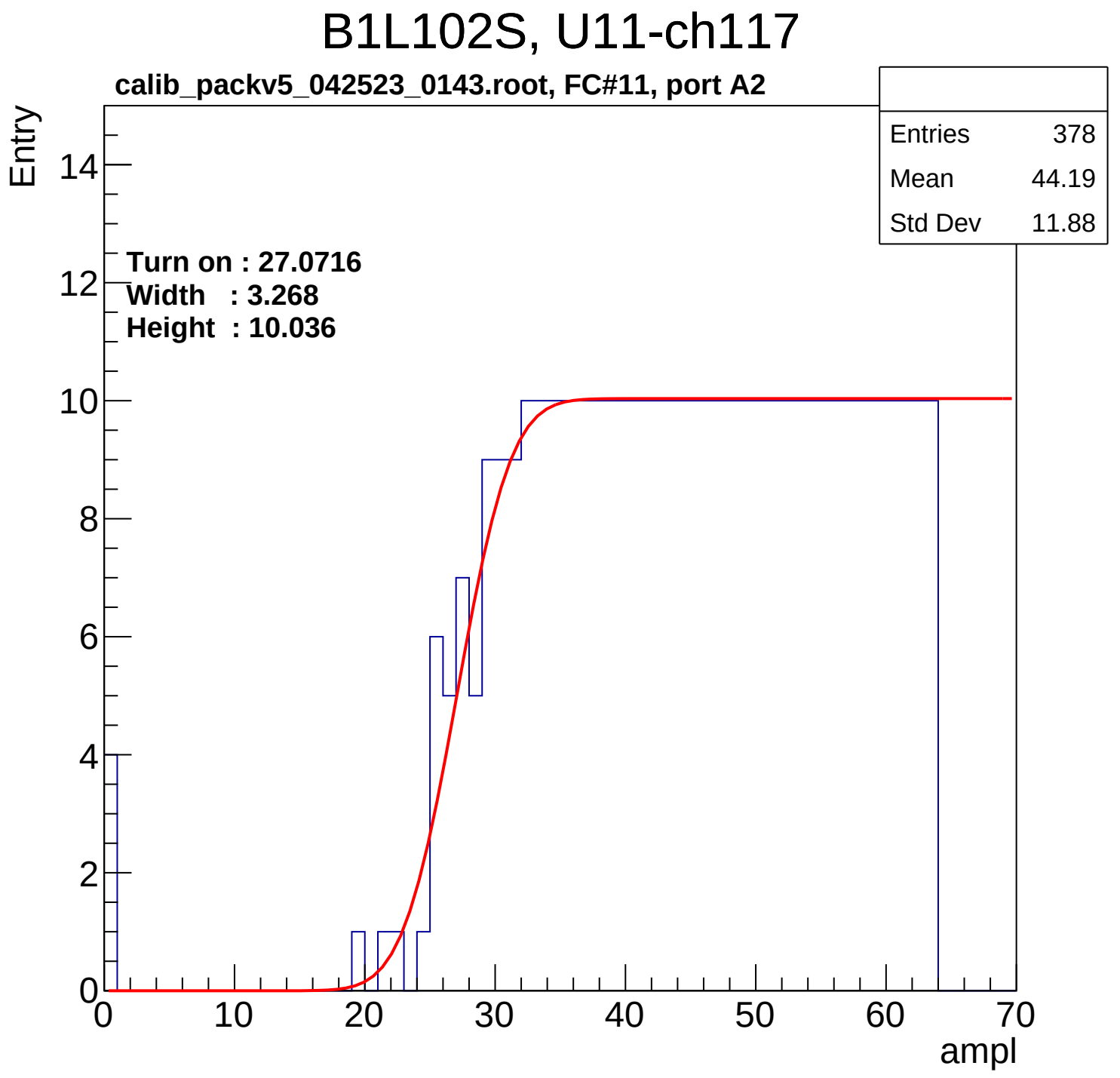
B1L102S, U11-ch117
calib_packv5_042523_0143.root, FC#11, port A2
Entries 378
Mean 44.19
Std Dev 11.88
Turn on : 27.0716
Width : 3.268
Height : 10.036
Entry
ampl
0
2
4
6
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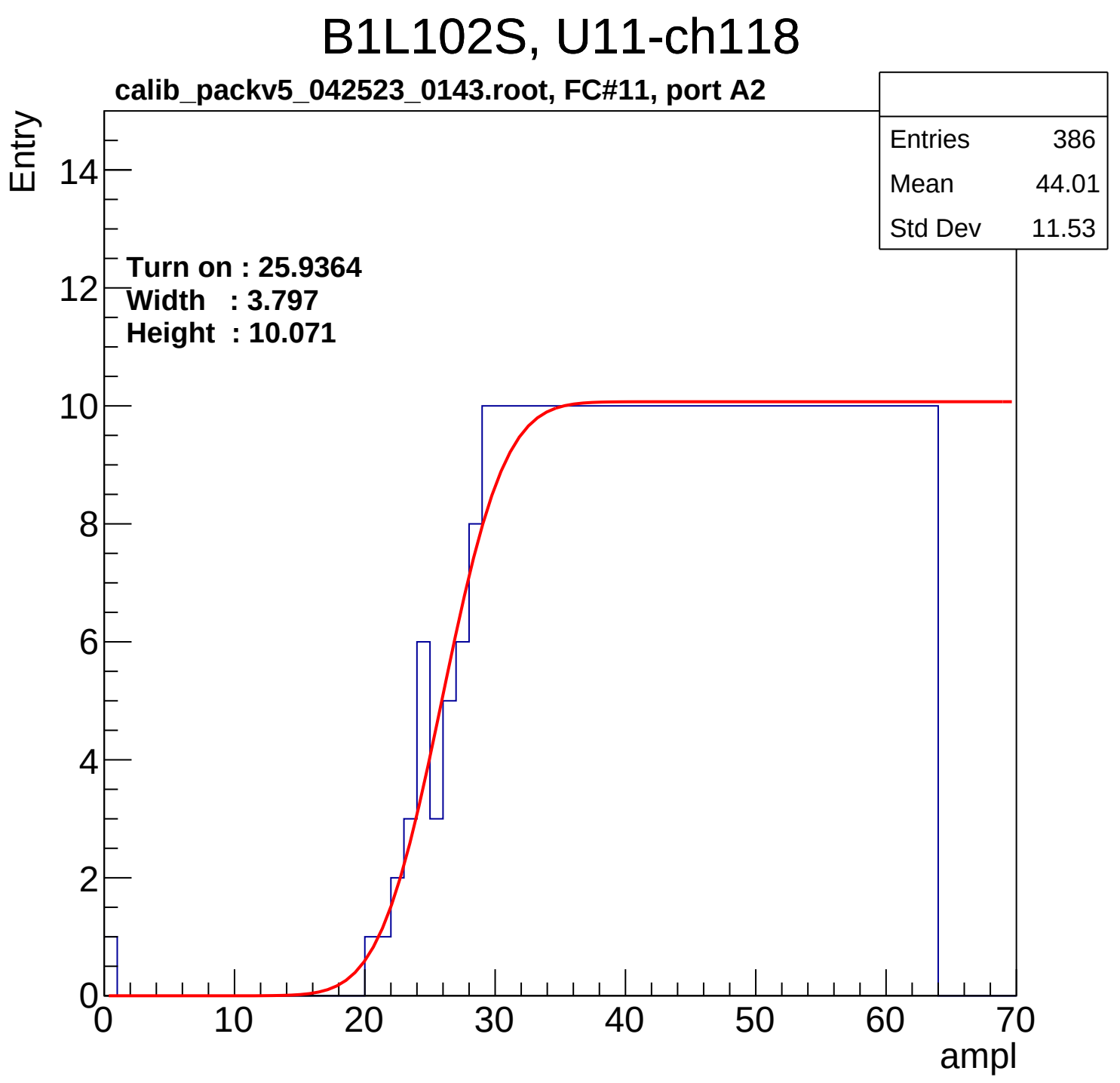
B1L102S, U11-ch118
calib_packv5_042523_0143.root, FC#11, port A2
Entries 386
Mean 44.01
Std Dev 11.53
Turn on : 25.9364
Width : 3.797
Height : 10.071
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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40
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60
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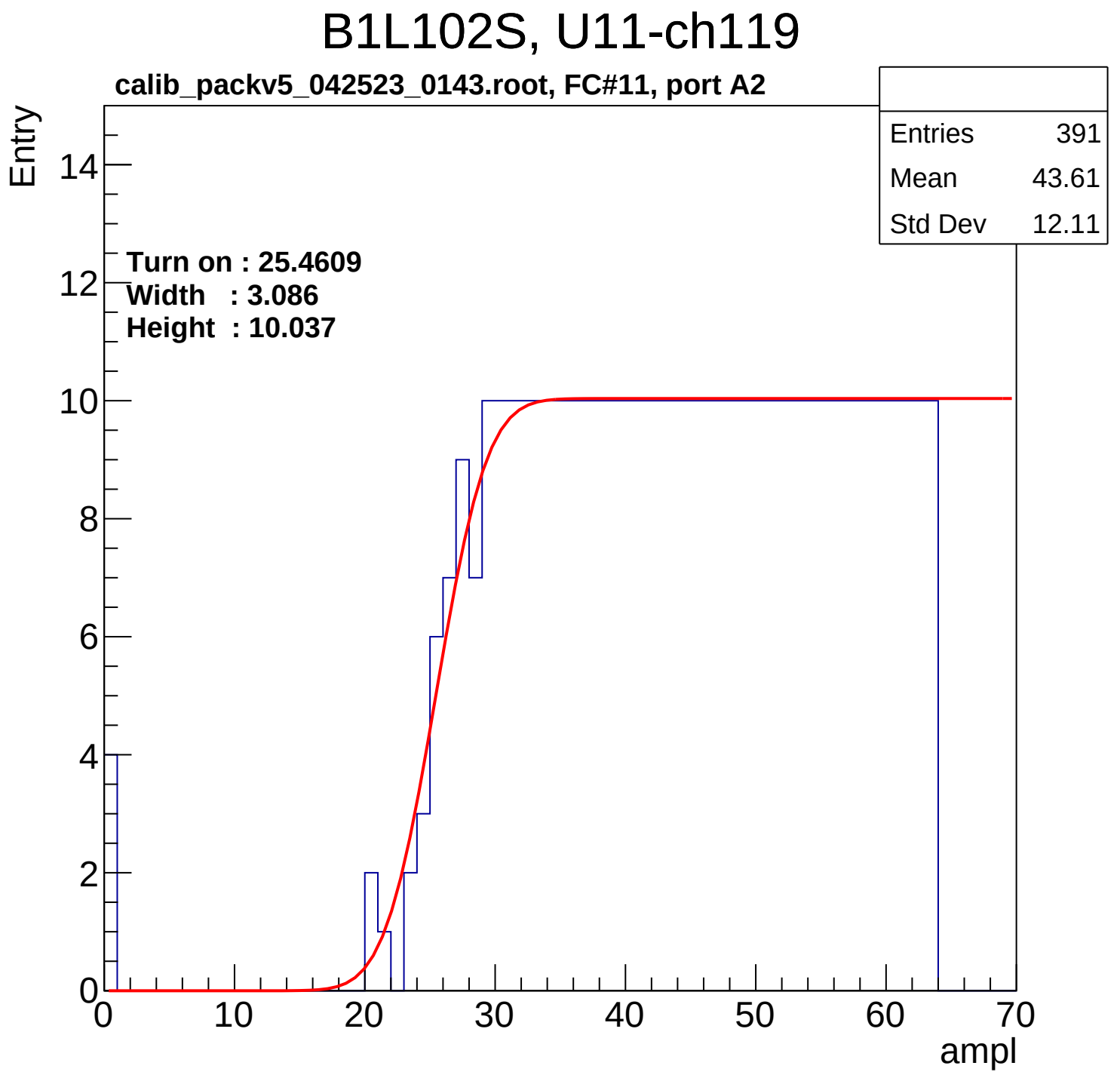
B1L102S, U11-ch119
calib_packv5_042523_0143.root, FC#11, port A2
Entries 391
Mean 43.61
Std Dev 12.11
Turn on : 25.4609
Width : 3.086
Height : 10.037
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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60
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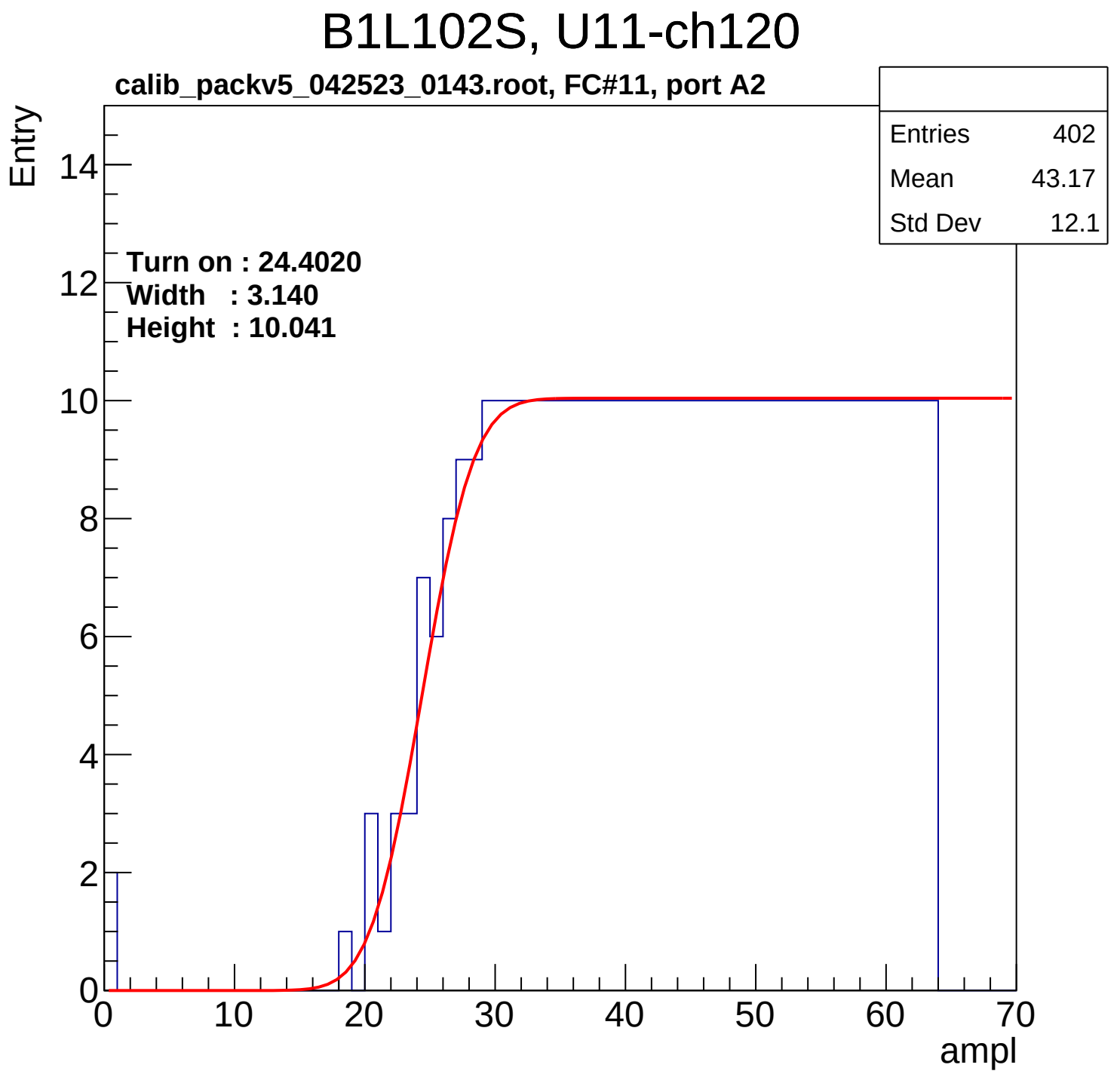
B1L102S, U11-ch120
calib_packv5_042523_0143.root, FC#11, port A2
Entries 402
Mean 43.17
Std Dev 12.1
Turn on : 24.4020
Width : 3.140
Height : 10.041
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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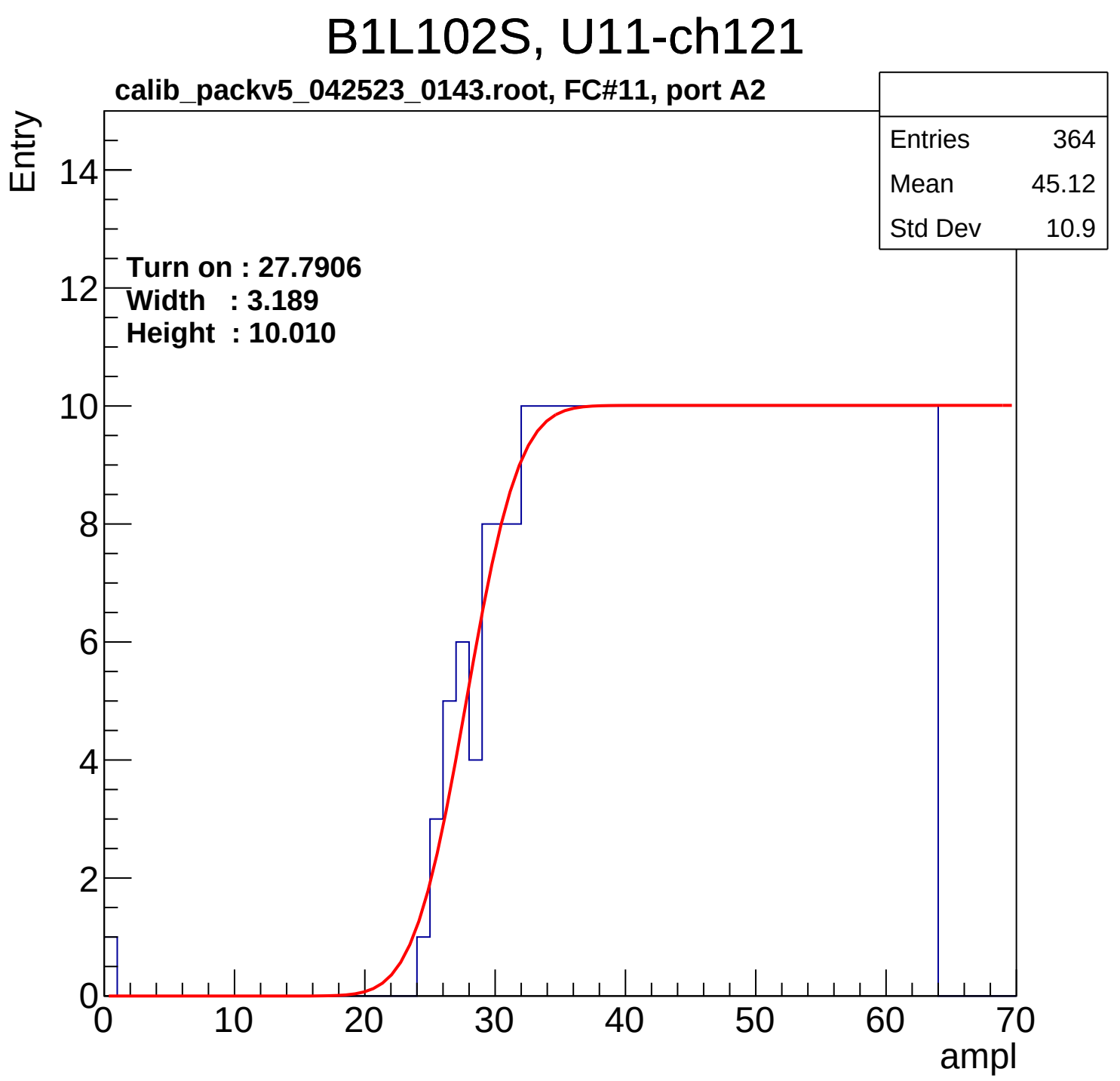
B1L102S, U11-ch121
calib_packv5_042523_0143.root, FC#11, port A2
Entries 364
Mean 45.12
Std Dev 10.9
Turn on : 27.7906
Width : 3.189
Height : 10.010
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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60
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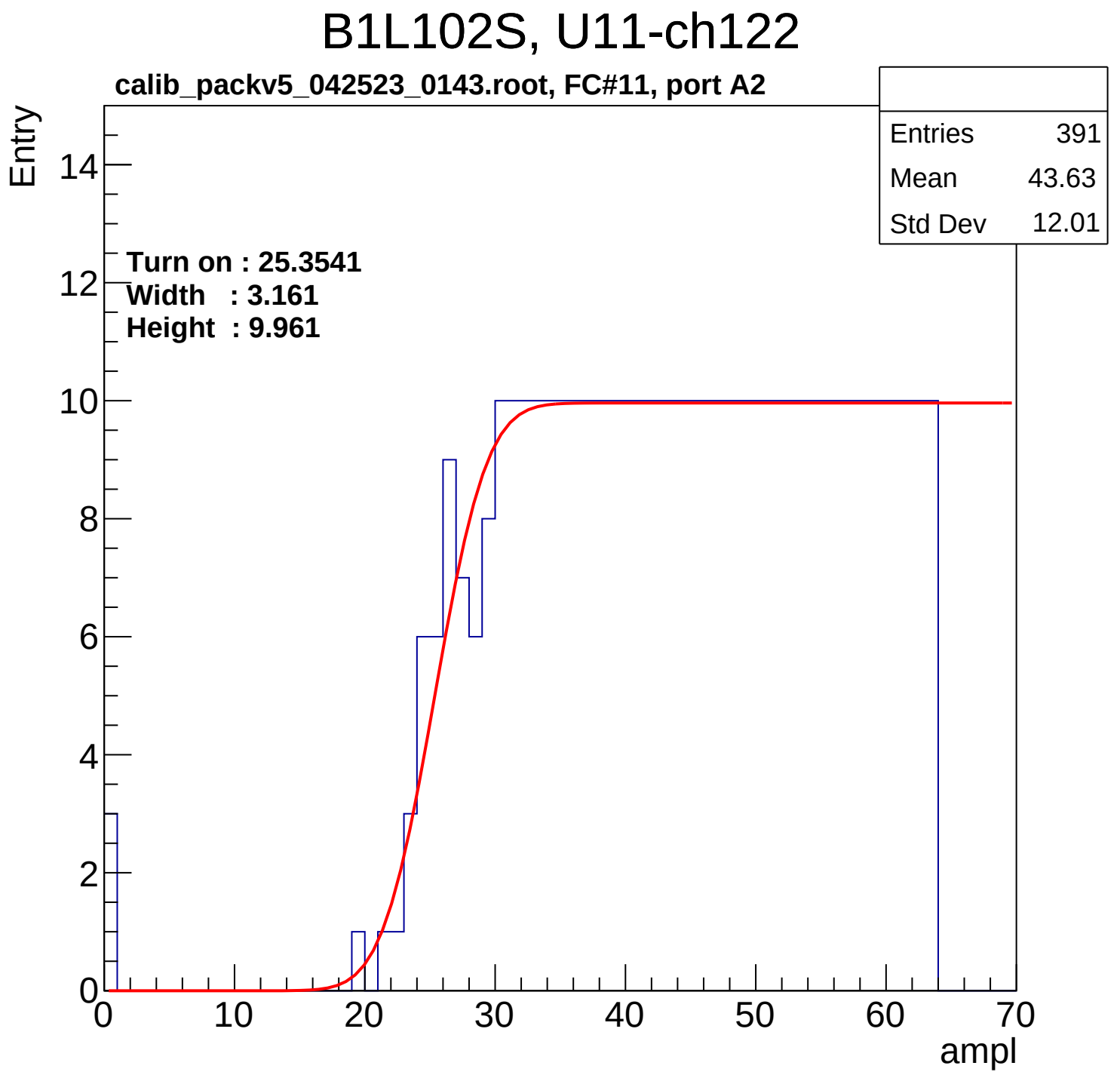
B1L102S, U11-ch122
calib_packv5_042523_0143.root, FC#11, port A2
Entries 391
Mean 43.63
Std Dev 12.01
Turn on : 25.3541
Width : 3.161
Height : 9.961
Entry
ampl
0
2
4
6
8
10
12
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0
10
20
30
40
50
60
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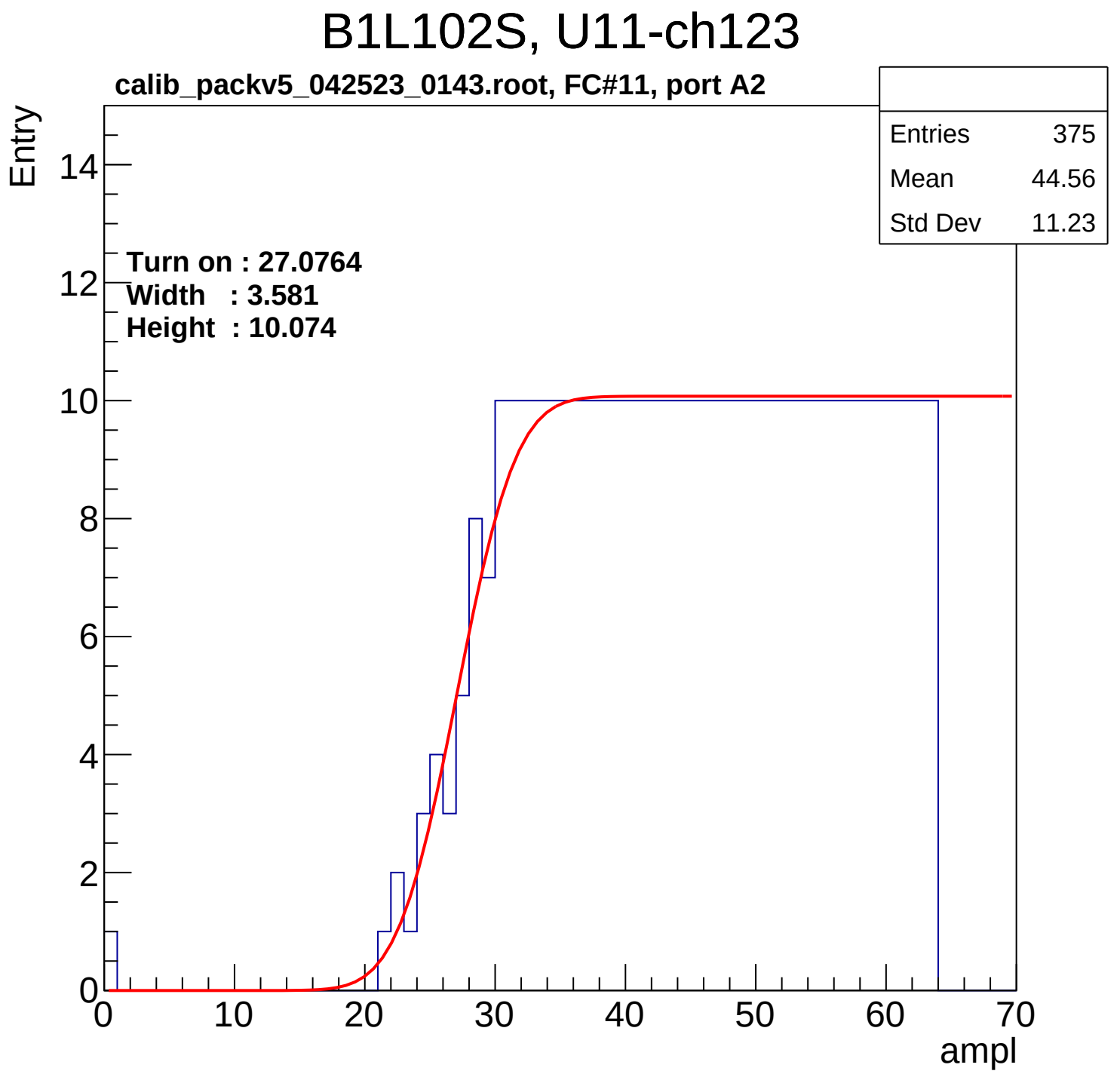
B1L102S, U11-ch123
calib_packv5_042523_0143.root, FC#11, port A2
Entries 375
Mean 44.56
Std Dev 11.23
Turn on : 27.0764
Width : 3.581
Height : 10.074
Entry
ampl
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4
6
8
10
12
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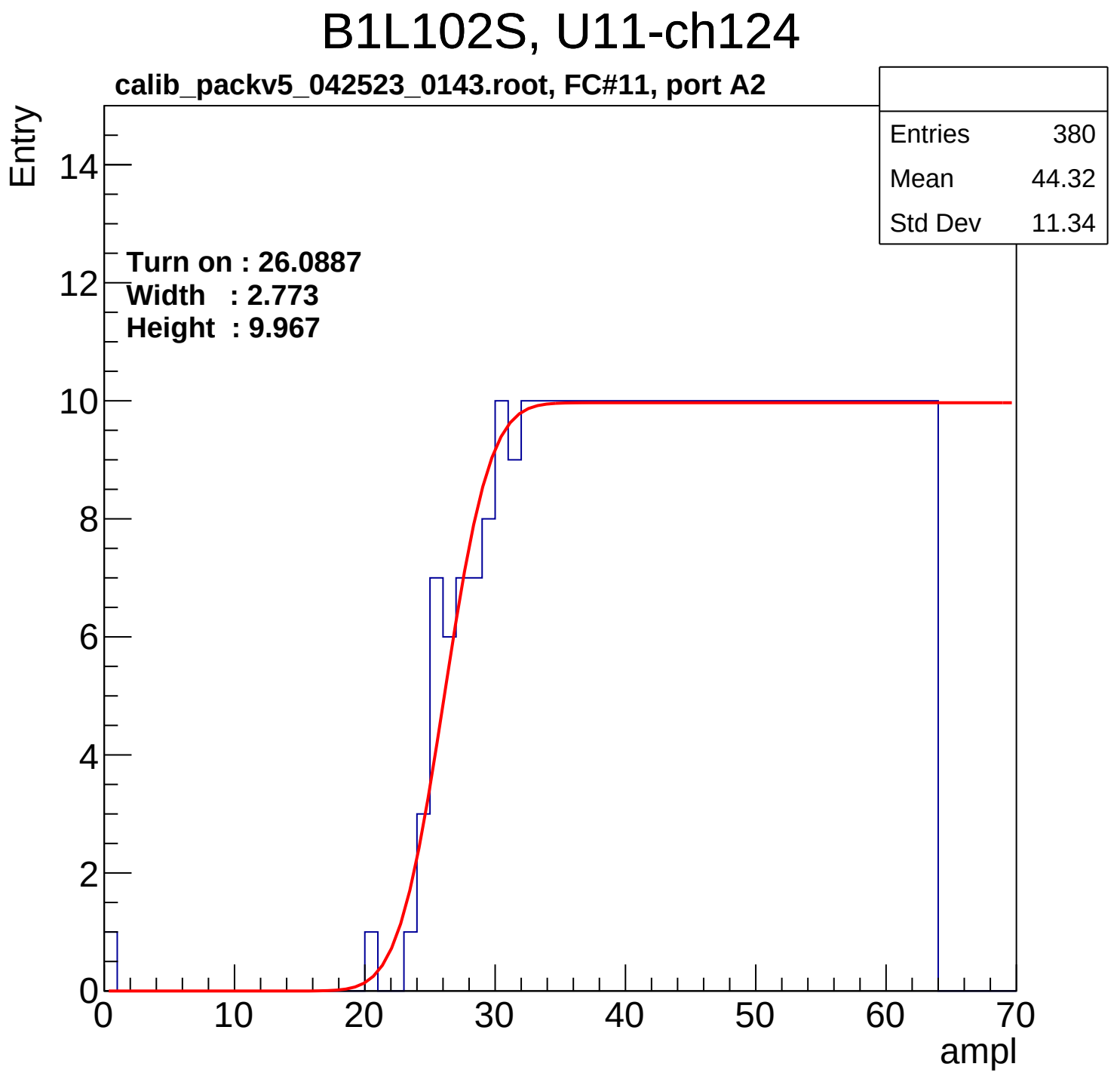
0
10
20
30
40
50
60
70


B1L102S, U11-ch124
calib_packv5_042523_0143.root, FC#11, port A2
Entries 380
Mean 44.32
Std Dev 11.34
Turn on : 26.0887
Width : 2.773
Height : 9.967
Entry
ampl
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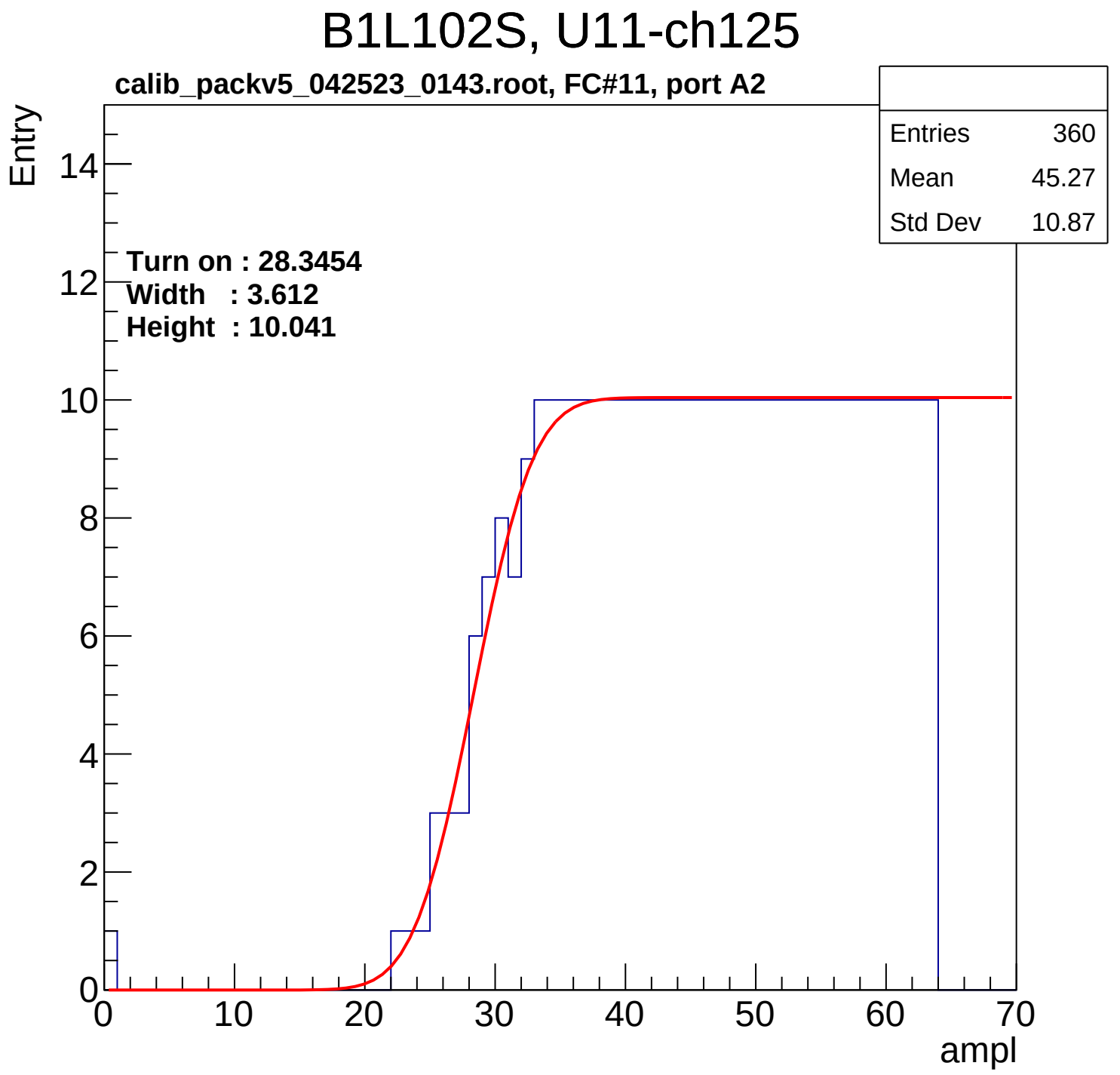
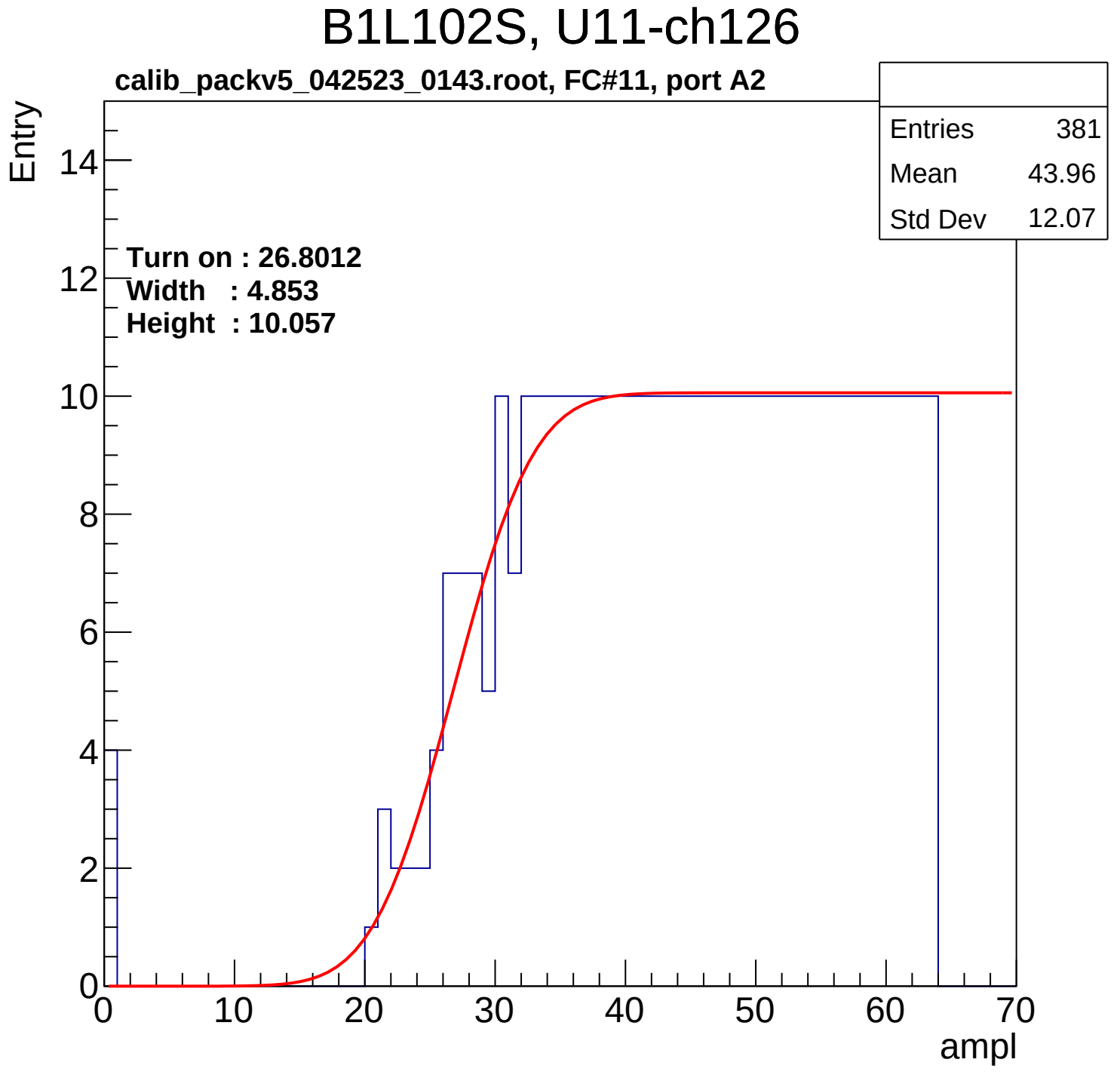
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L102S, U11-ch125
calib_packv5_042523_0143.root, FC#11, port A2
Entries 360
Mean 45.27
Std Dev 10.87
Turn on : 28.3454
Width : 3.612
Height : 10.041
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L102S, U11-ch126
calib_packv5_042523_0143.root, FC#11, port A2
Entries 381
Mean 43.96
Std Dev 12.07
Turn on : 26.8012
Width : 4.853
Height : 10.057
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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40
50
60
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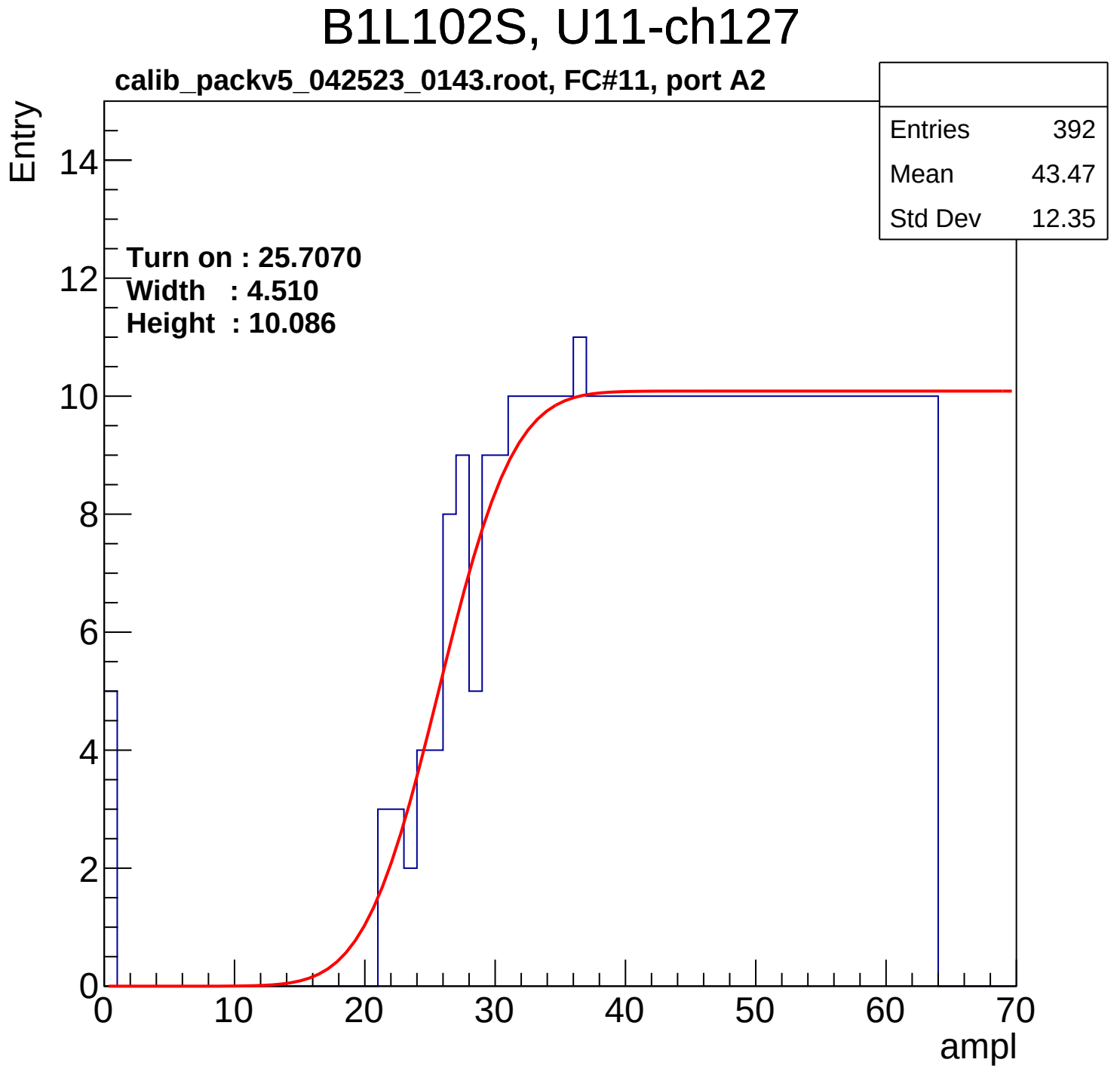
B1L102S, U11-ch127
calib_packv5_042523_0143.root, FC#11, port A2
Entries 392
Mean 43.47
Std Dev 12.35
Turn on : 25.7070
Width : 4.510
Height : 10.086
Entry
ampl
0
2
4
6
8
10
12
14
0
10
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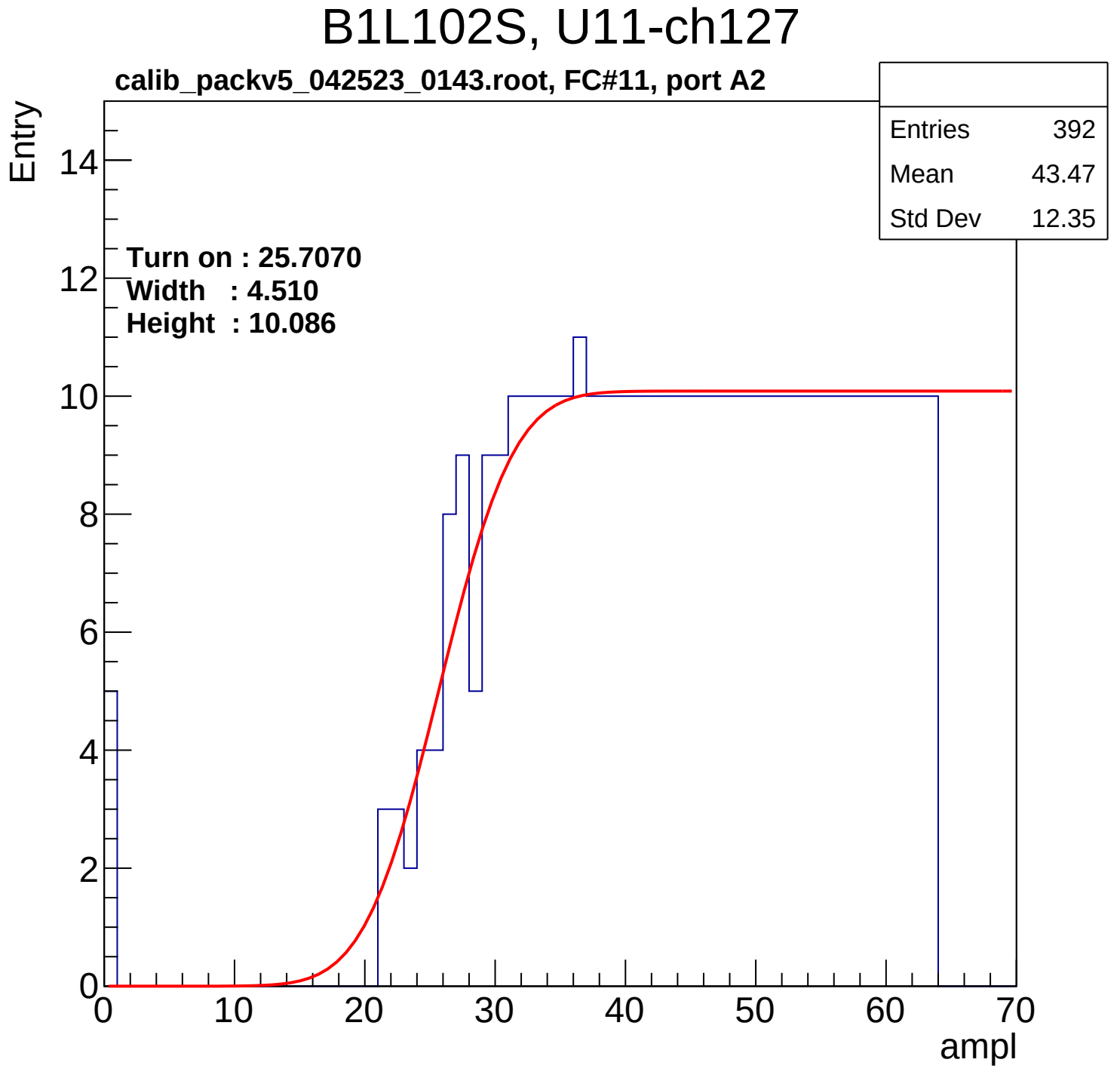
B1L102S, U11-ch127
calib_packv5_042523_0143.root, FC#11, port A2
Entries 392
Mean 43.47
Std Dev 12.35
Turn on : 25.7070
Width : 4.510
Height : 10.086
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70