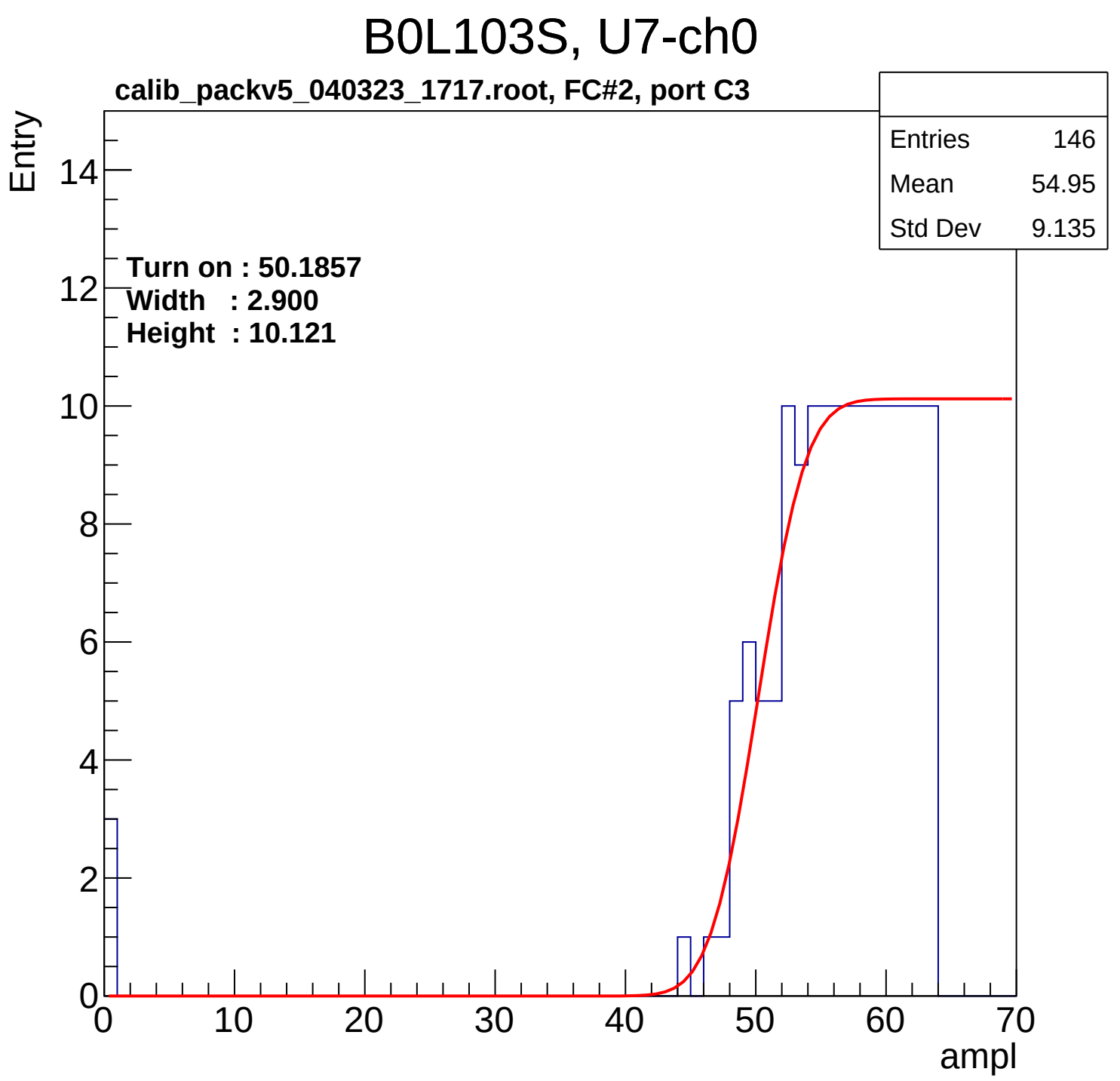
B0L103S, U7-ch0
calib_packv5_040323_1717.root, FC#2, port C3
Entries 146
Mean 54.95
Std Dev 9.135
Turn on : 50.1857
Width : 2.900
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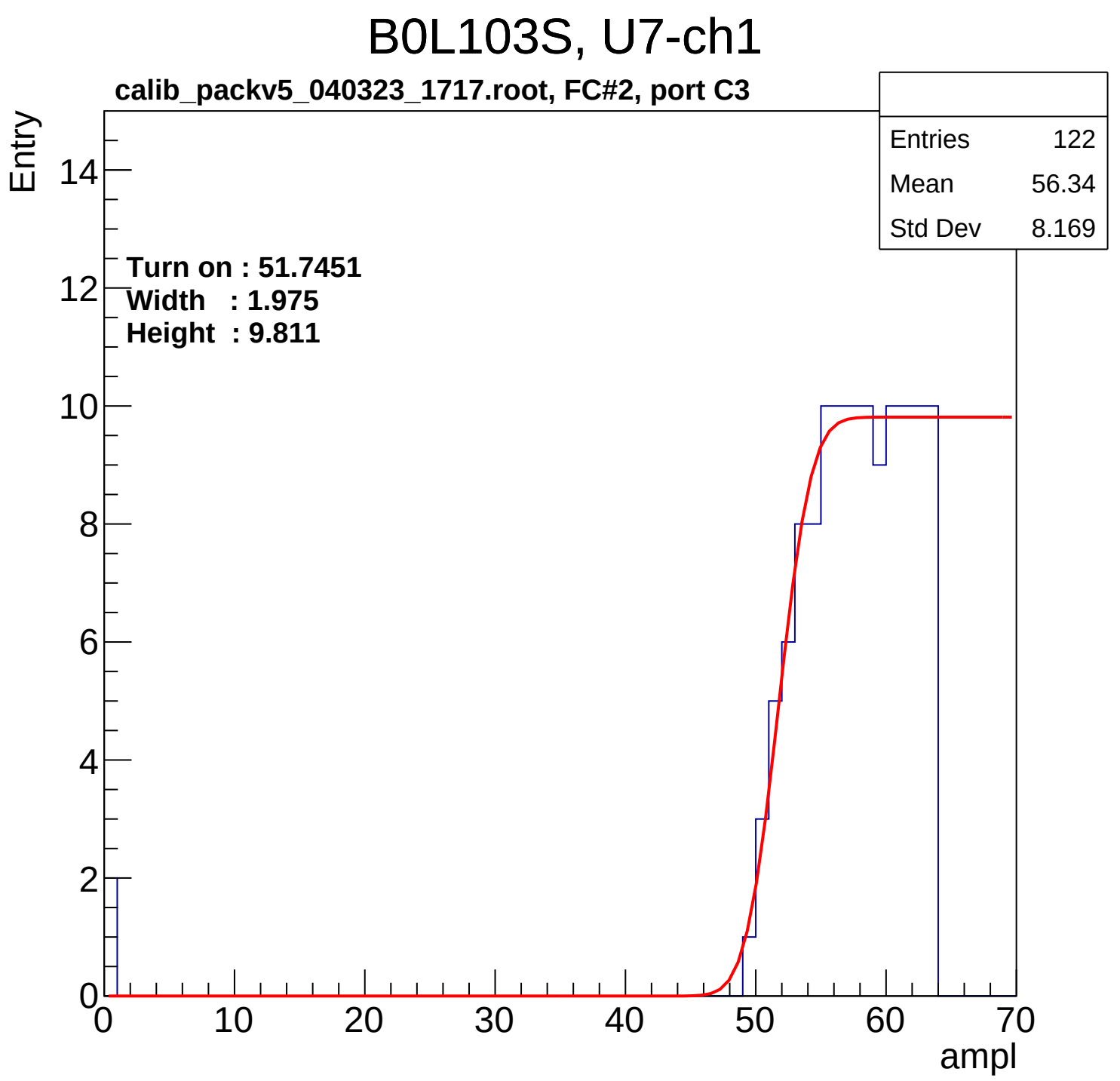
B0L103S, U7-ch1
calib_packv5_040323_1717.root, FC#2, port C3
Entries 122
Mean 56.34
Std Dev 8.169
Turn on : 51.7451
Width : 1.975
Height : 9.811
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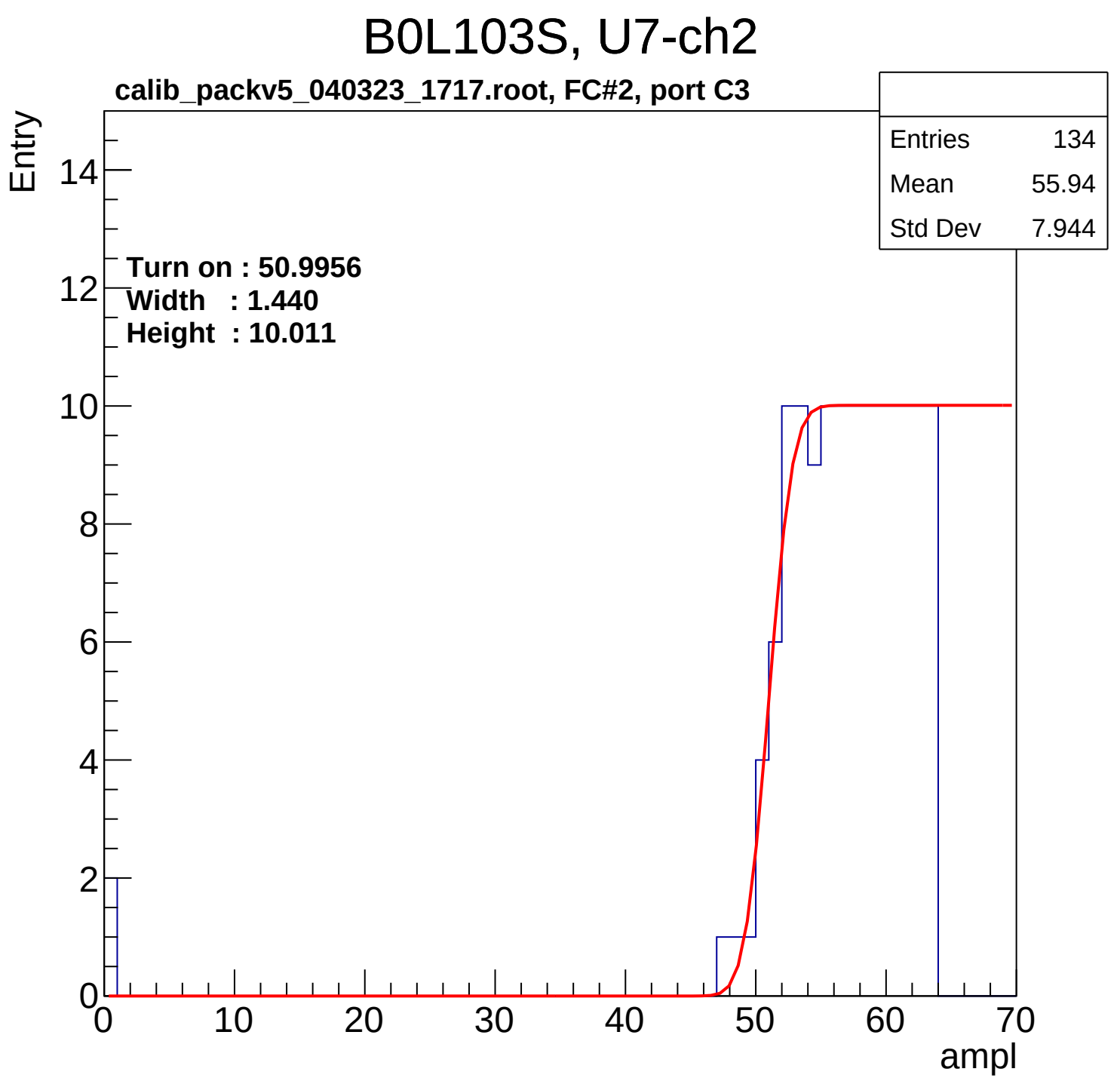
B0L103S, U7-ch2
calib_packv5_040323_1717.root, FC#2, port C3
Entries 134
Mean 55.94
Std Dev 7.944
Turn on : 50.9956
Width : 1.440
Height : 10.011
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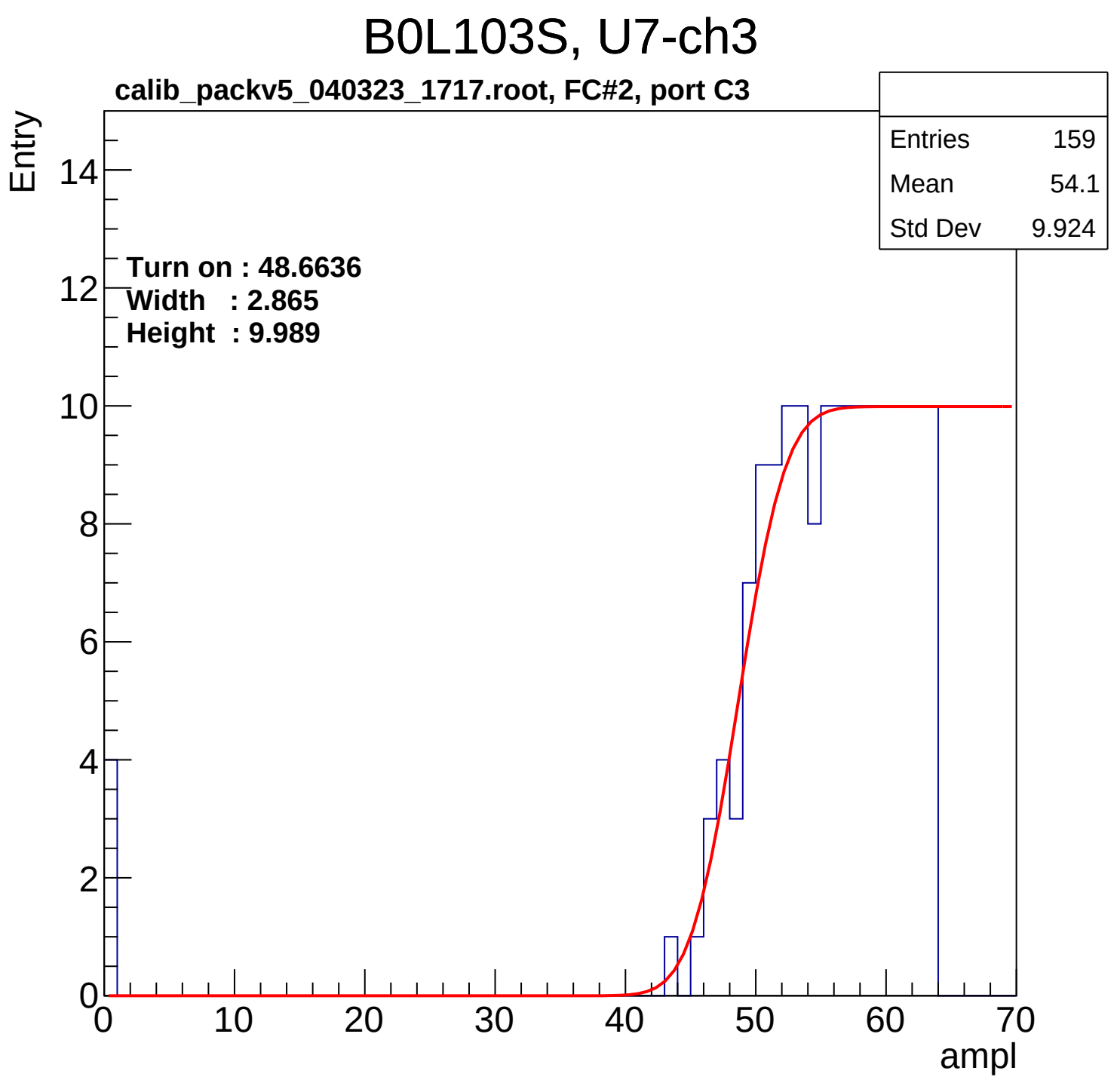
B0L103S, U7-ch3
calib_packv5_040323_1717.root, FC#2, port C3
Entries 159
Mean 54.1
Std Dev 9.924
Turn on : 48.6636
Width : 2.865
Height : 9.989
Entry
ampl
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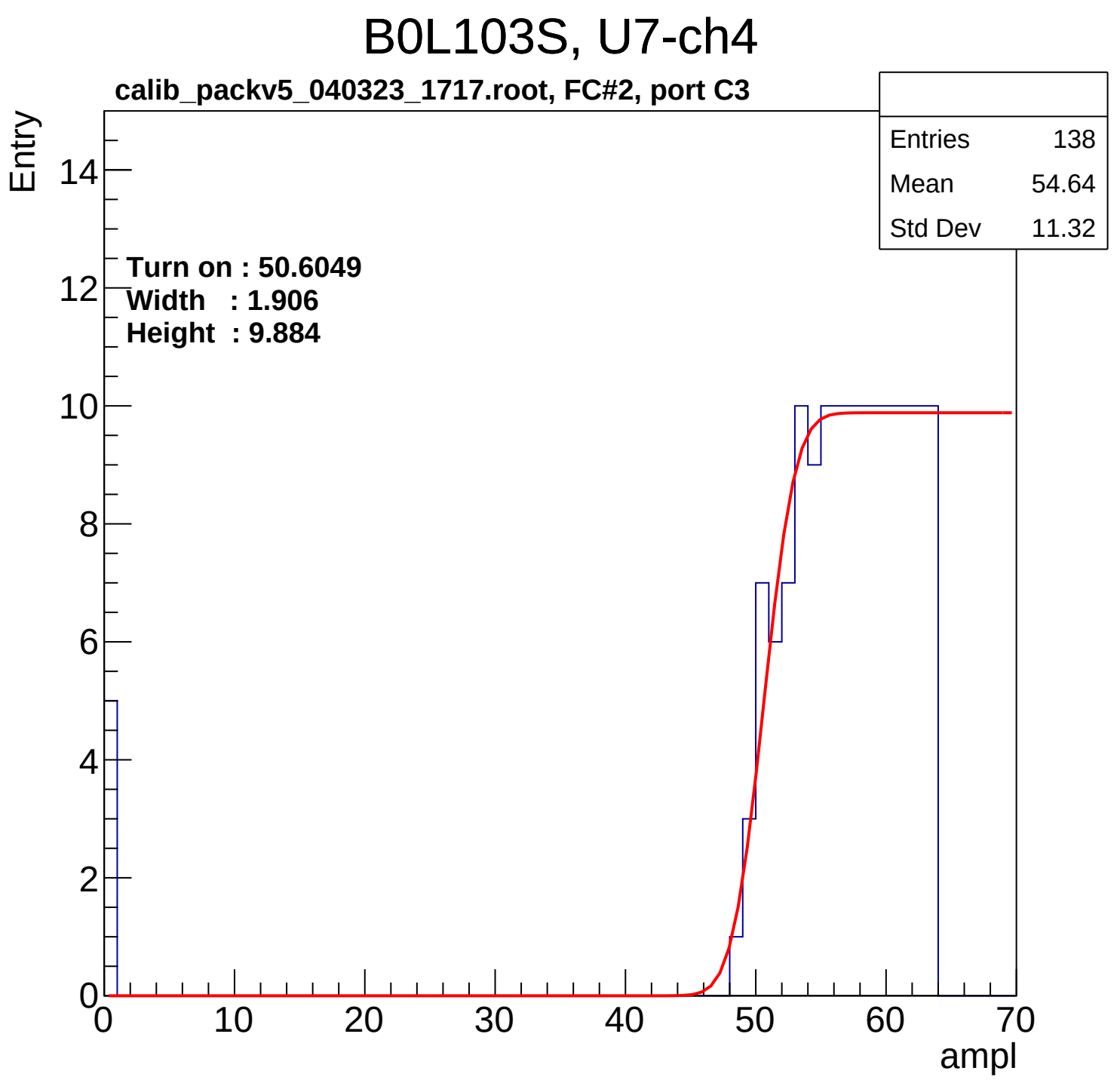
B0L103S, U7-ch4
calib_packv5_040323_1717.root, FC#2, port C3
Entries 138
Mean 54.64
Std Dev 11.32
Turn on : 50.6049
Width : 1.906
Height : 9.884
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ampl
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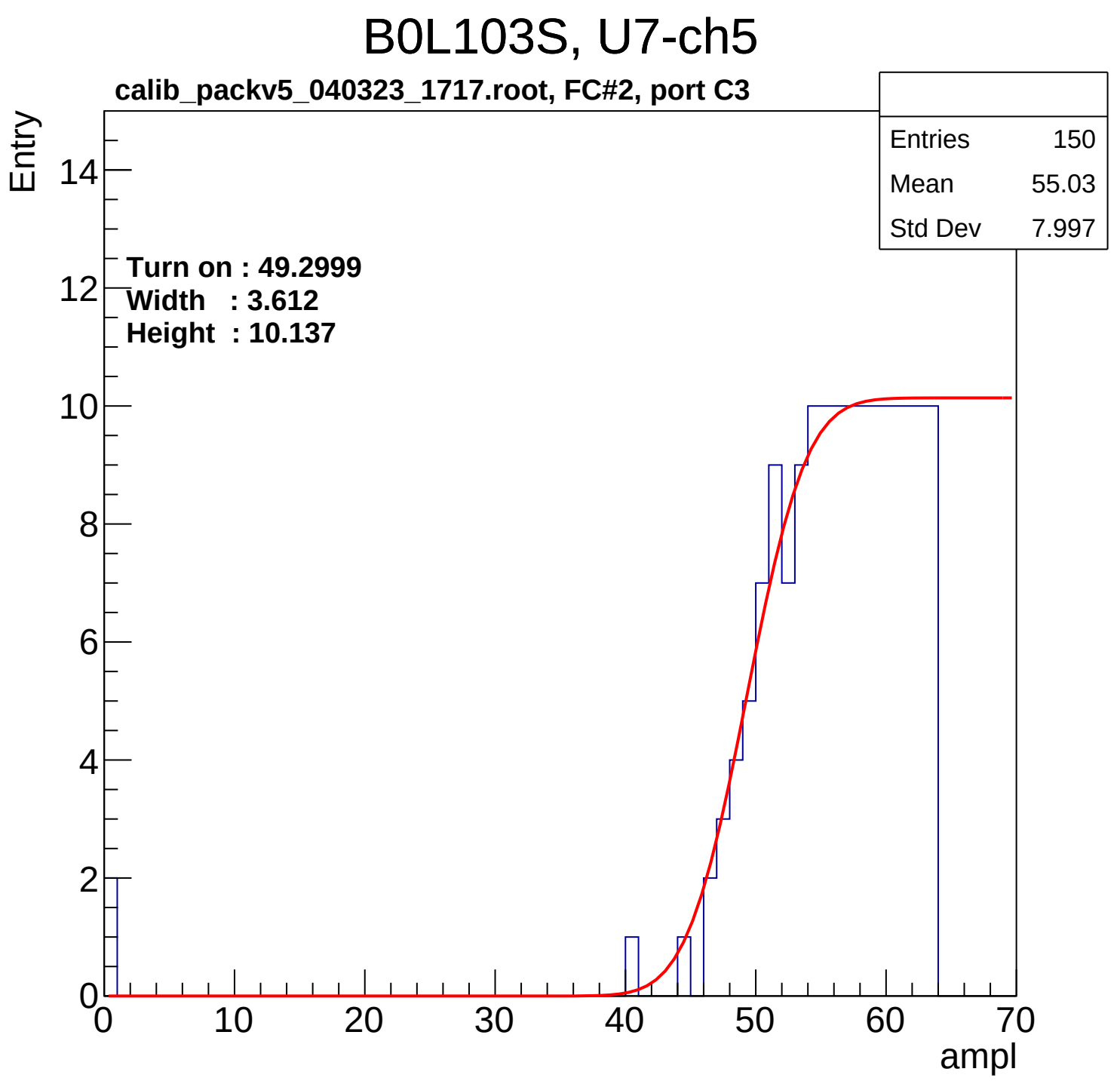
B0L103S, U7-ch5
calib_packv5_040323_1717.root, FC#2, port C3
Entries 150
Mean 55.03
Std Dev 7.997
Turn on : 49.2999
Width : 3.612
Height : 10.137
Entry
ampl
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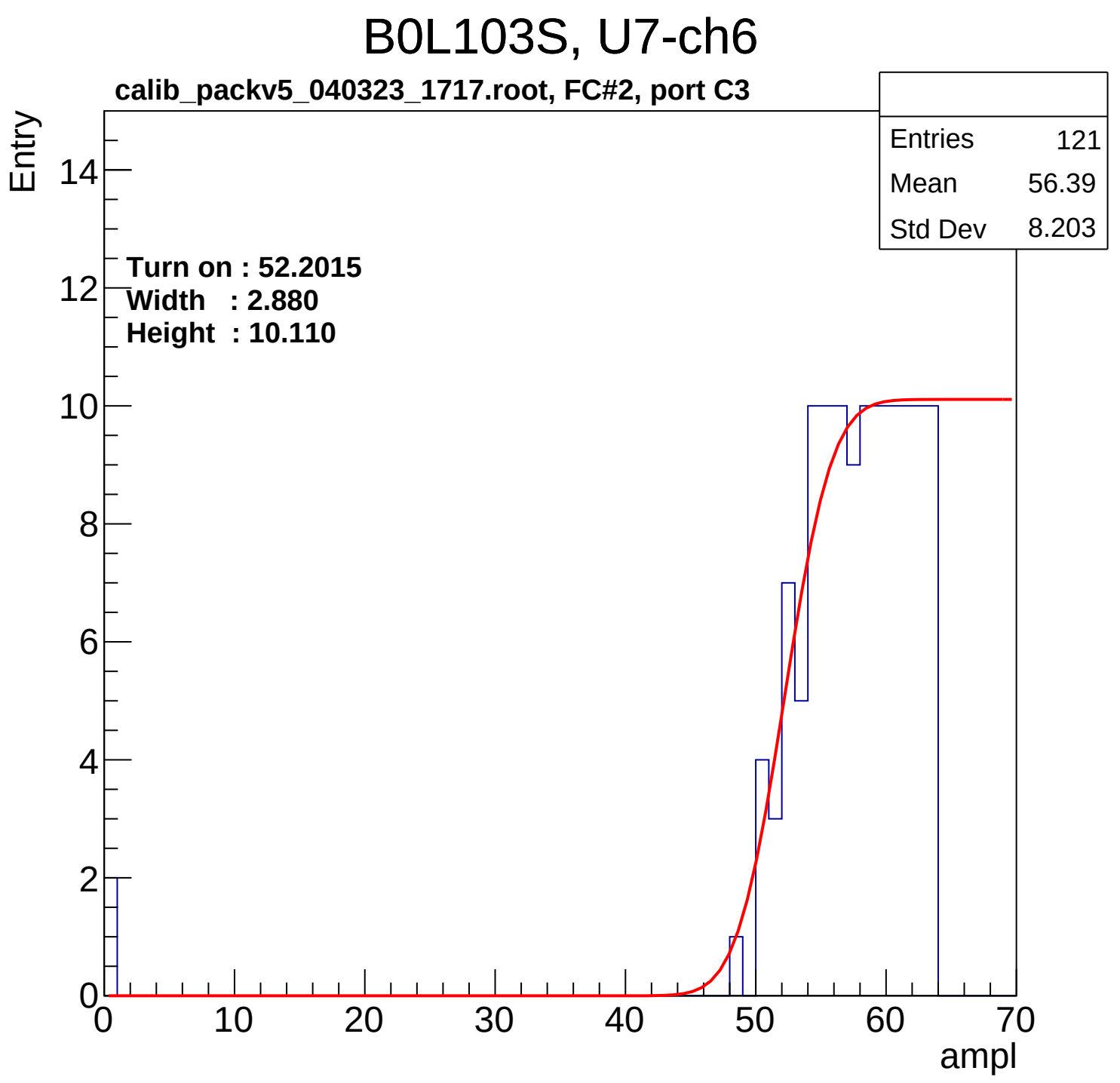
B0L103S, U7-ch6
calib_packv5_040323_1717.root, FC#2, port C3
Entries 121
Mean 56.39
Std Dev 8.203
Turn on : 52.2015
Width : 2.880
Height : 10.110
Entry
ampl
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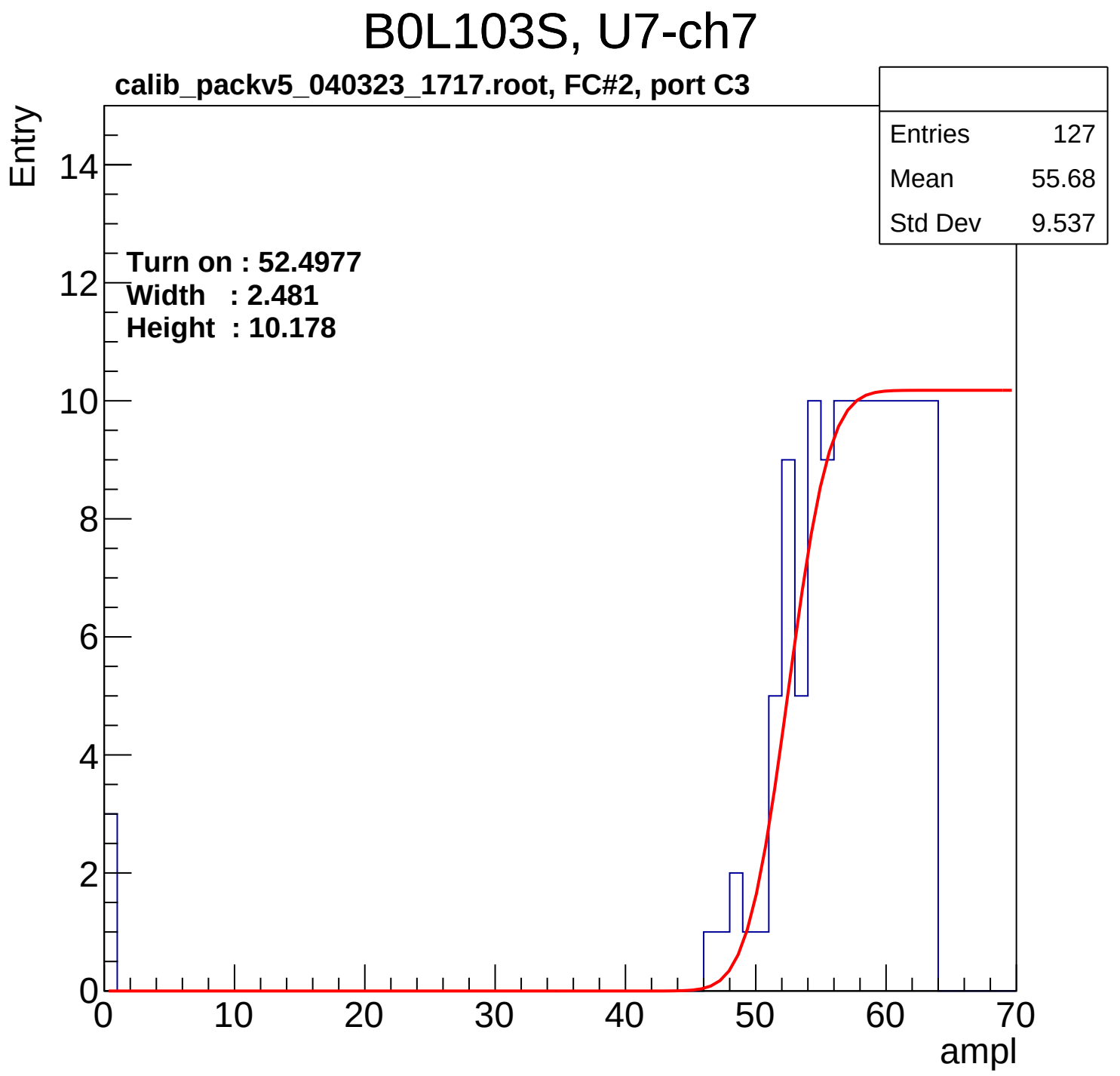
B0L103S, U7-ch7
calib_packv5_040323_1717.root, FC#2, port C3
Entries 127
Mean 55.68
Std Dev 9.537
Turn on : 52.4977
Width : 2.481
Height : 10.178
Entry
ampl
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6
8
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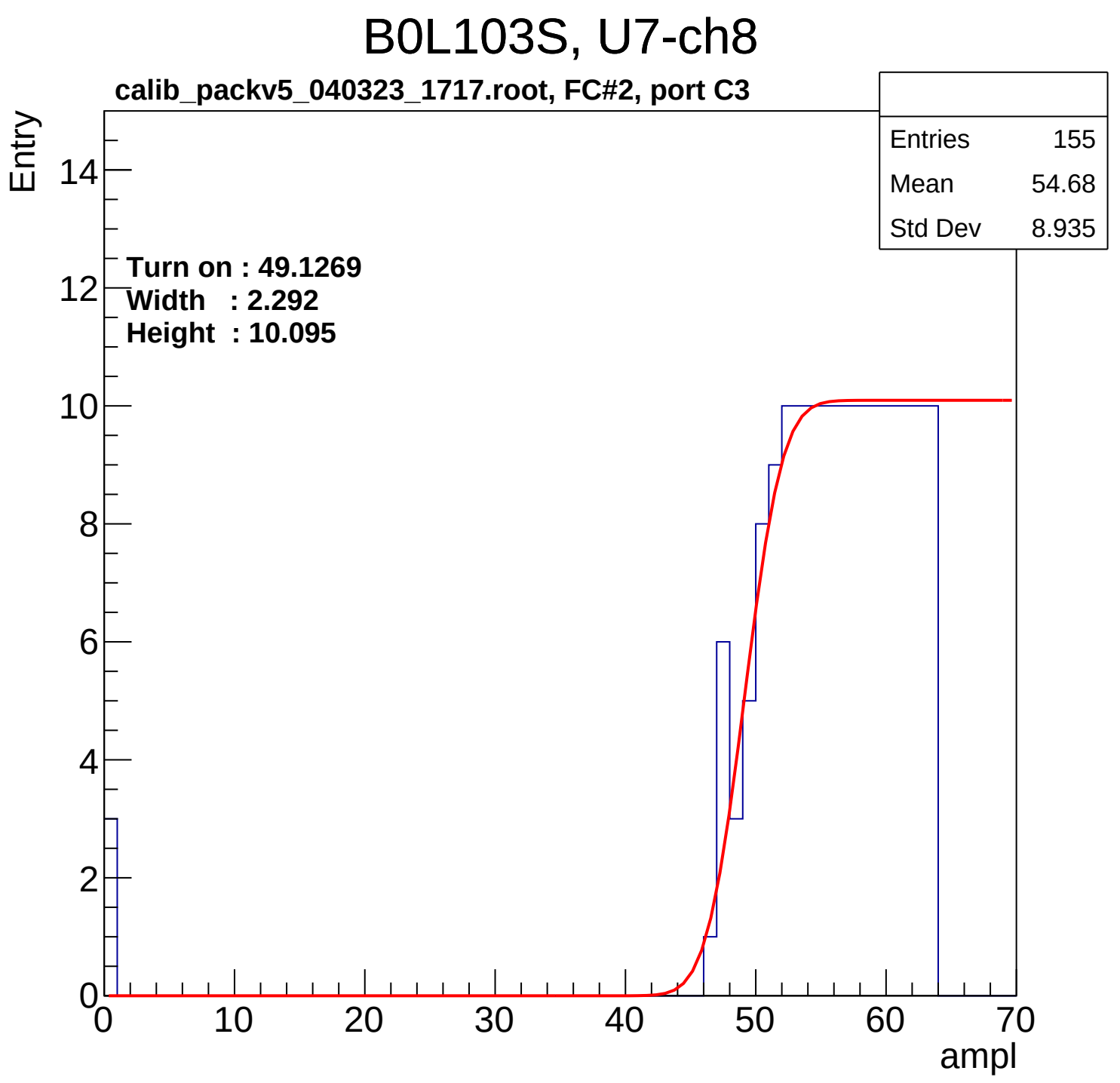
B0L103S, U7-ch8
calib_packv5_040323_1717.root, FC#2, port C3
Entries 155
Mean 54.68
Std Dev 8.935
Turn on : 49.1269
Width : 2.292
Height : 10.095
Entry
ampl
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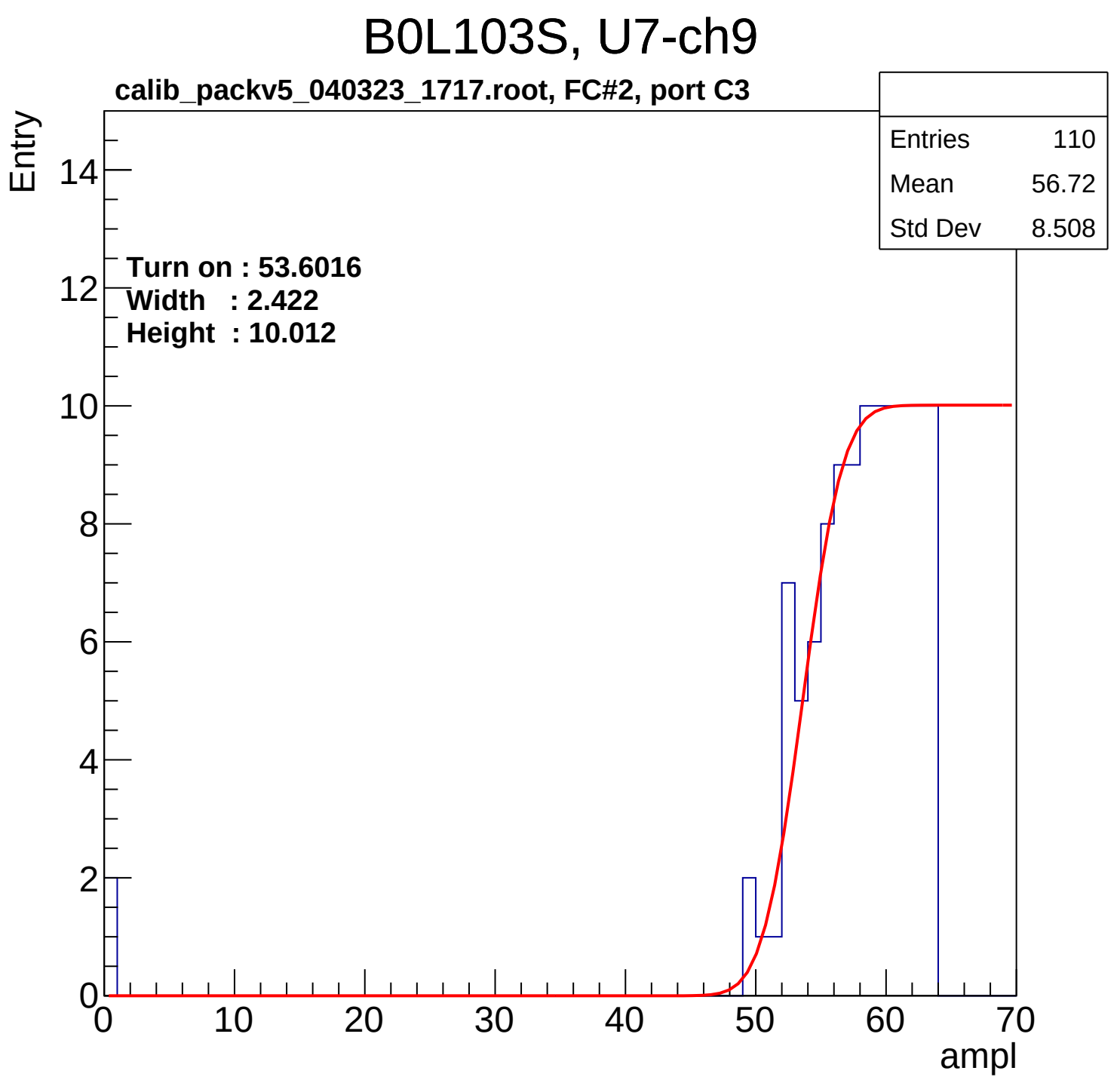
B0L103S, U7-ch9
calib_packv5_040323_1717.root, FC#2, port C3
Entries 110
Mean 56.72
Std Dev 8.508
Turn on : 53.6016
Width : 2.422
Height : 10.012
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ampl
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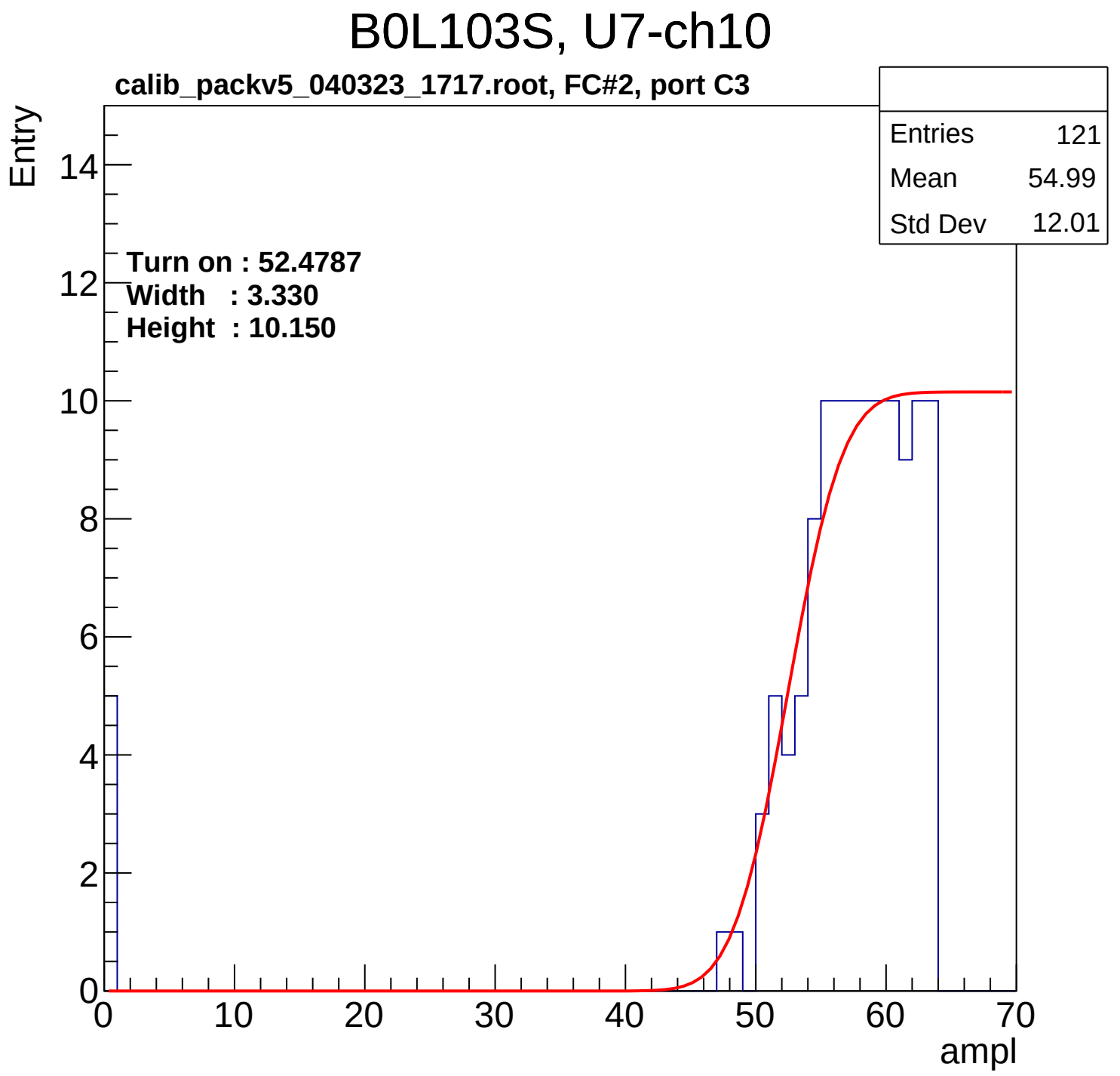
B0L103S, U7-ch10
calib_packv5_040323_1717.root, FC#2, port C3
Entries 121
Mean 54.99
Std Dev 12.01
Turn on : 52.4787
Width : 3.330
Height : 10.150
Entry
ampl
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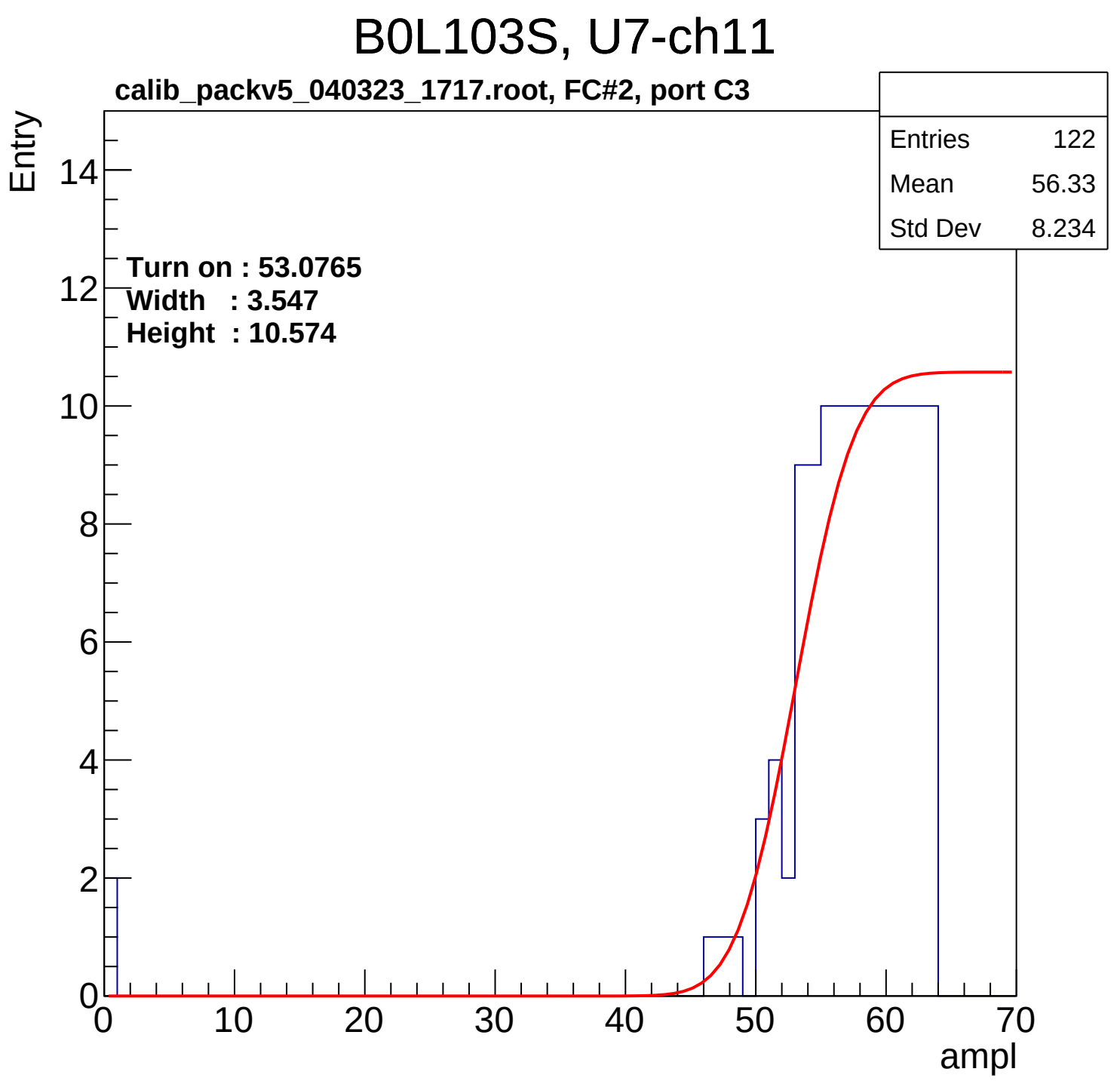
B0L103S, U7-ch11
calib_packv5_040323_1717.root, FC#2, port C3
Entries 122
Mean 56.33
Std Dev 8.234
Turn on : 53.0765
Width : 3.547
Height : 10.574
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ampl
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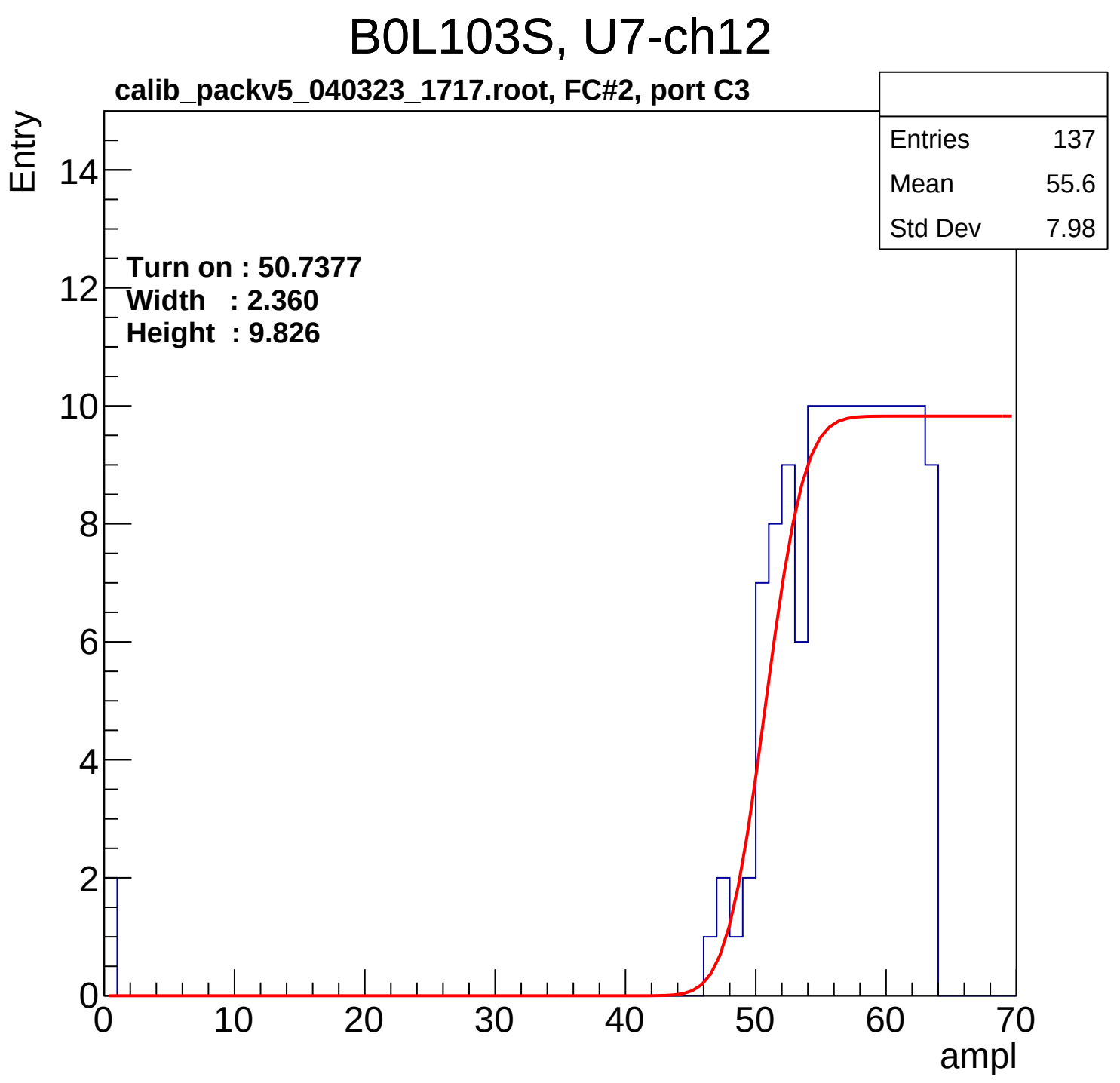
B0L103S, U7-ch12
calib_packv5_040323_1717.root, FC#2, port C3
Entries 137
Mean 55.6
Std Dev 7.98
Turn on : 50.7377
Width : 2.360
Height : 9.826
Entry
ampl
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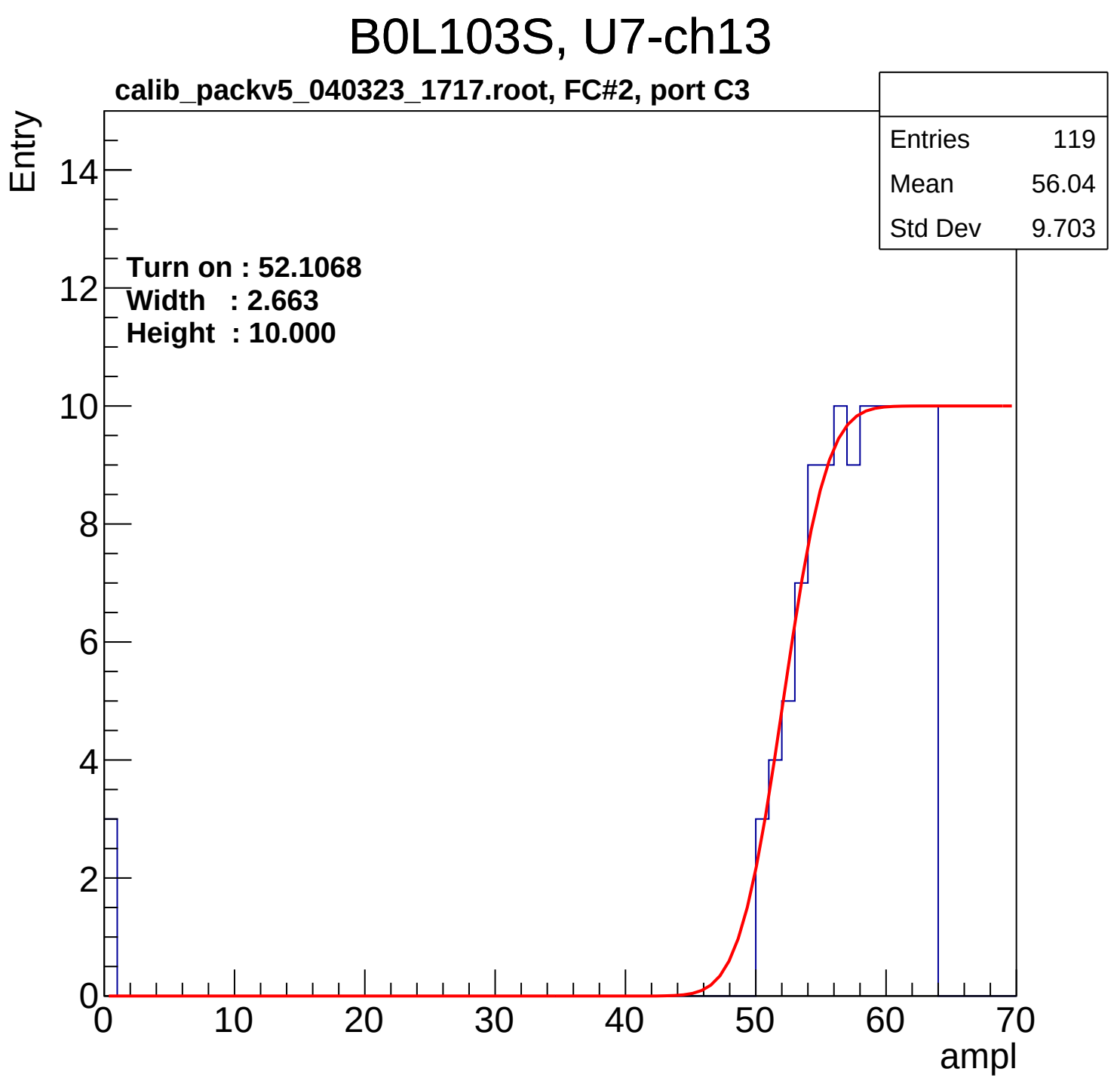
B0L103S, U7-ch13
calib_packv5_040323_1717.root, FC#2, port C3
Entries 119
Mean 56.04
Std Dev 9.703
Turn on : 52.1068
Width : 2.663
Height : 10.000
Entry
ampl
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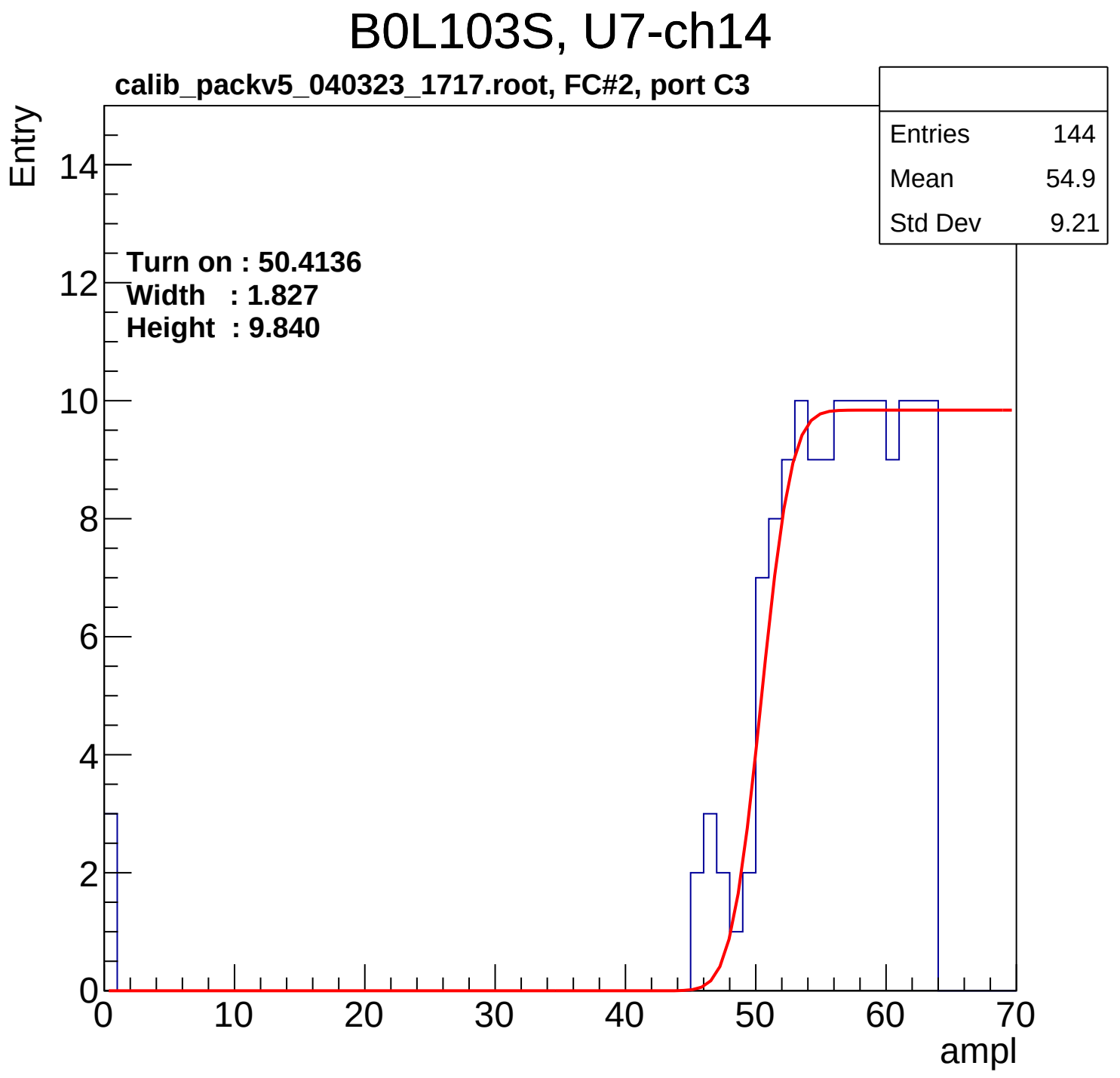
B0L103S, U7-ch14
calib_packv5_040323_1717.root, FC#2, port C3
Entries 144
Mean 54.9
Std Dev 9.21
Turn on : 50.4136
Width : 1.827
Height : 9.840
Entry
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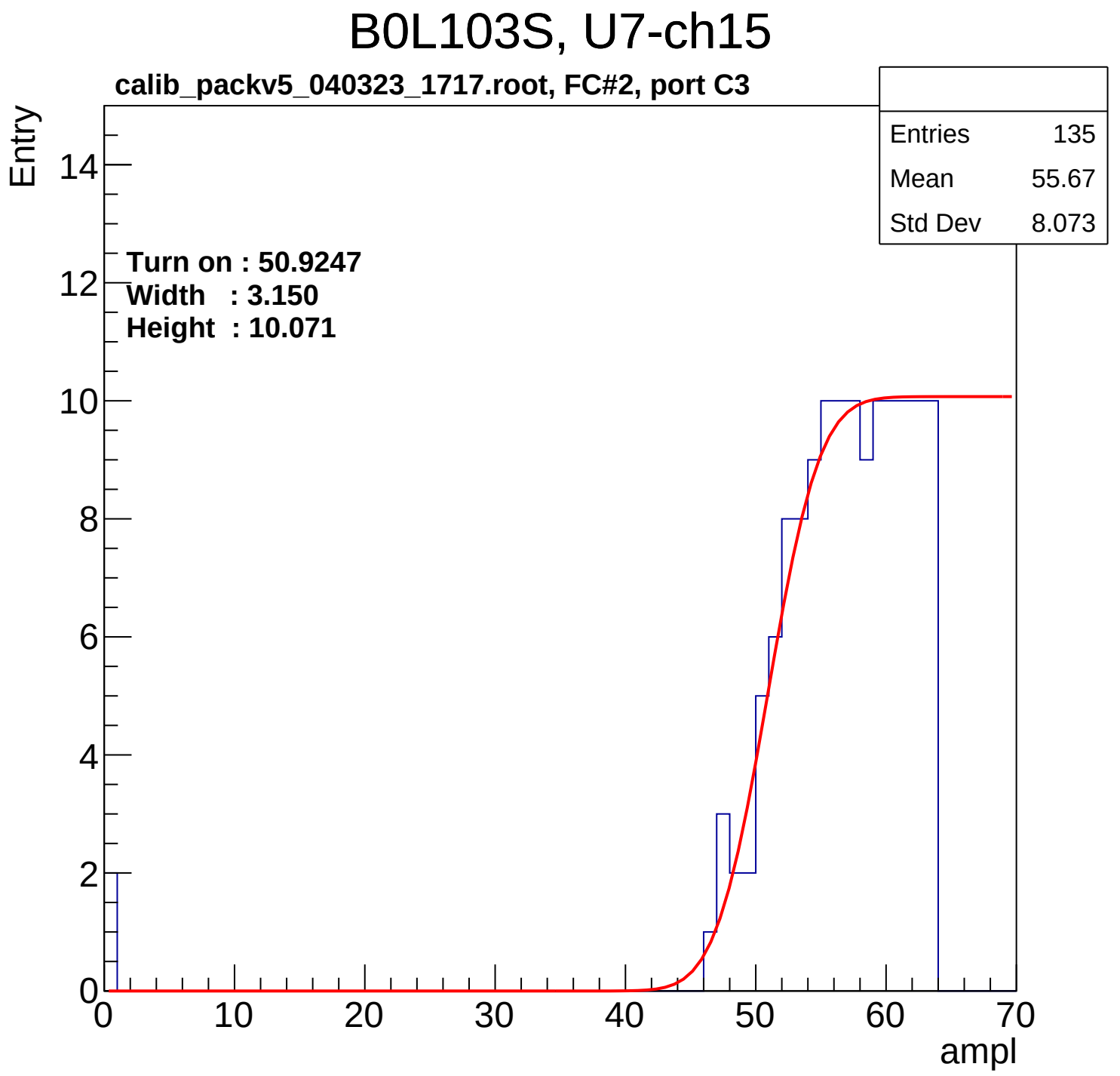
B0L103S, U7-ch15
calib_packv5_040323_1717.root, FC#2, port C3
Entries 135
Mean 55.67
Std Dev 8.073
Turn on : 50.9247
Width : 3.150
Height : 10.071
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ampl
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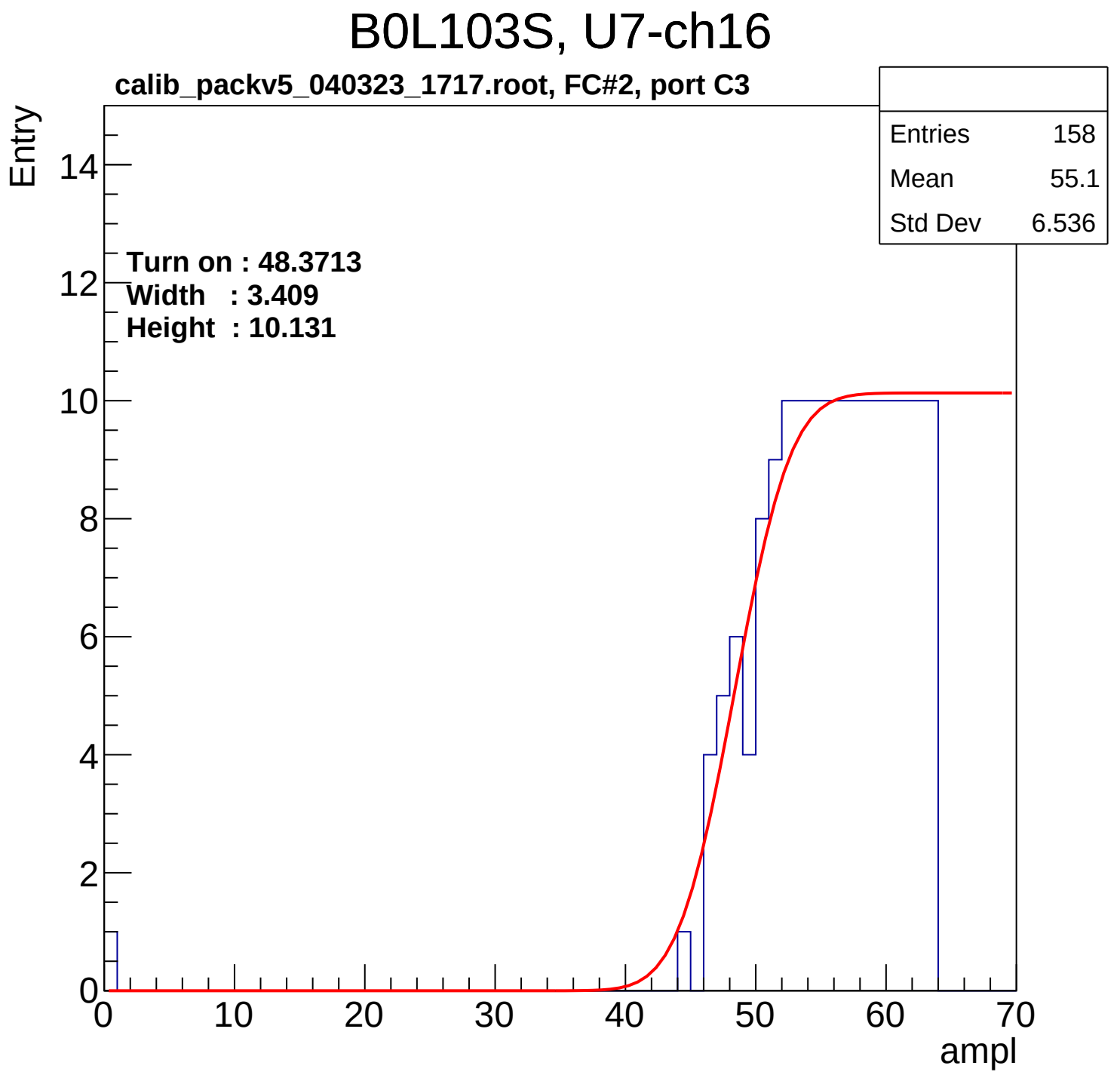
B0L103S, U7-ch16
calib_packv5_040323_1717.root, FC#2, port C3
Entries 158
Mean 55.1
Std Dev 6.536
Turn on : 48.3713
Width : 3.409
Height : 10.131
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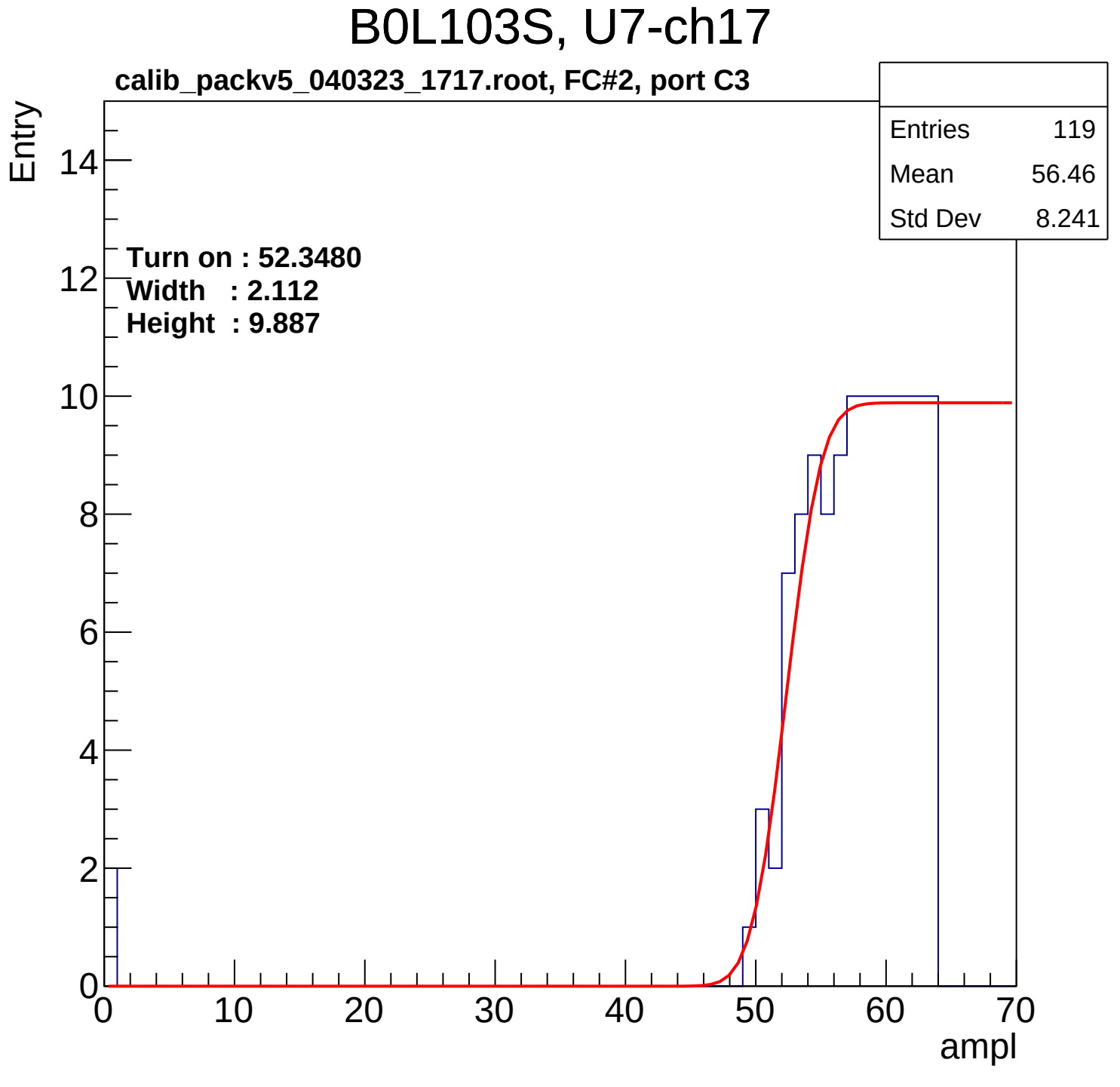
B0L103S, U7-ch17
calib_packv5_040323_1717.root, FC#2, port C3
Entries 119
Mean 56.46
Std Dev 8.241
Turn on : 52.3480
Width : 2.112
Height : 9.887
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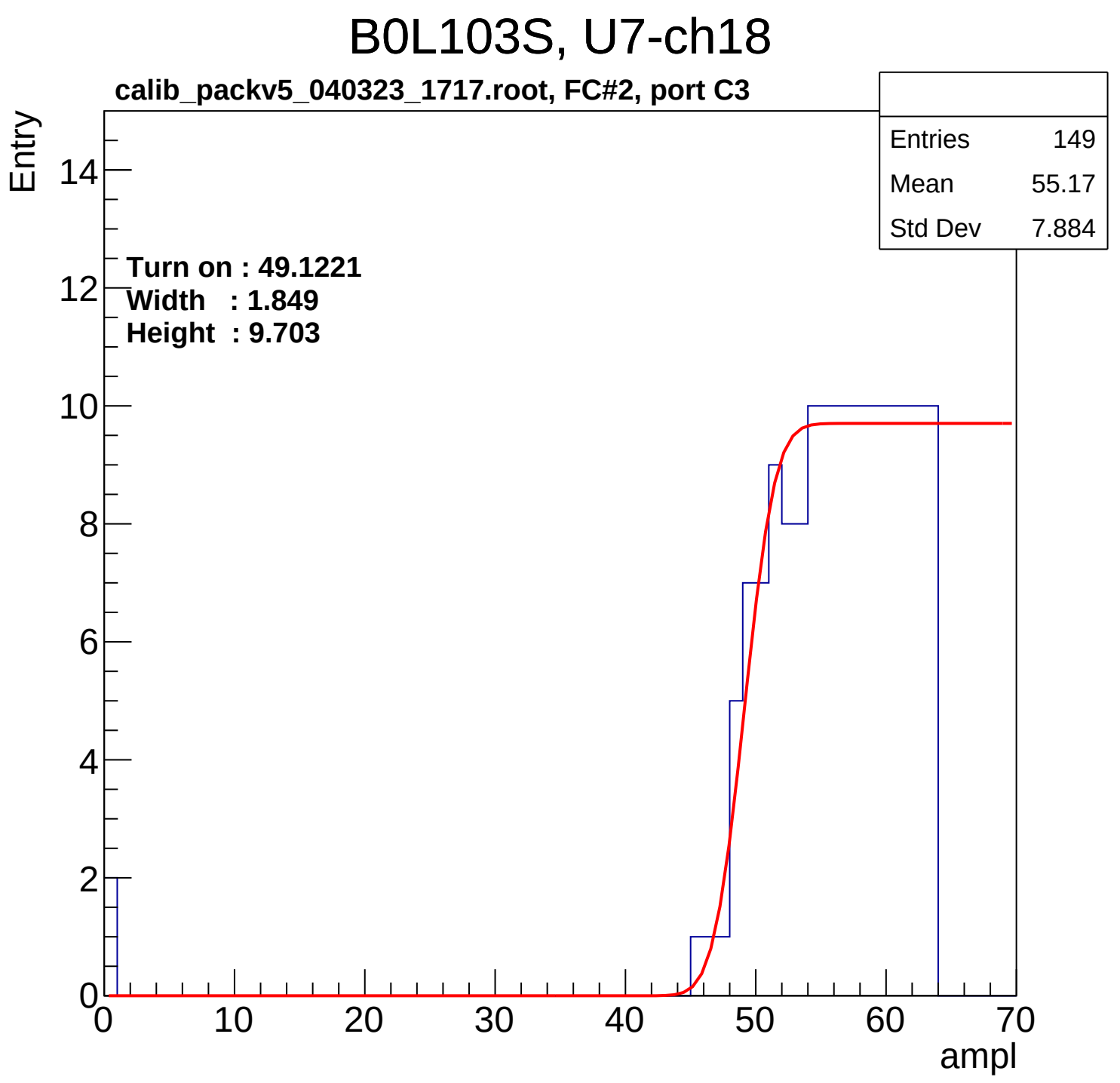
B0L103S, U7-ch18
calib_packv5_040323_1717.root, FC#2, port C3
Entries 149
Mean 55.17
Std Dev 7.884
Turn on : 49.1221
Width : 1.849
Height : 9.703
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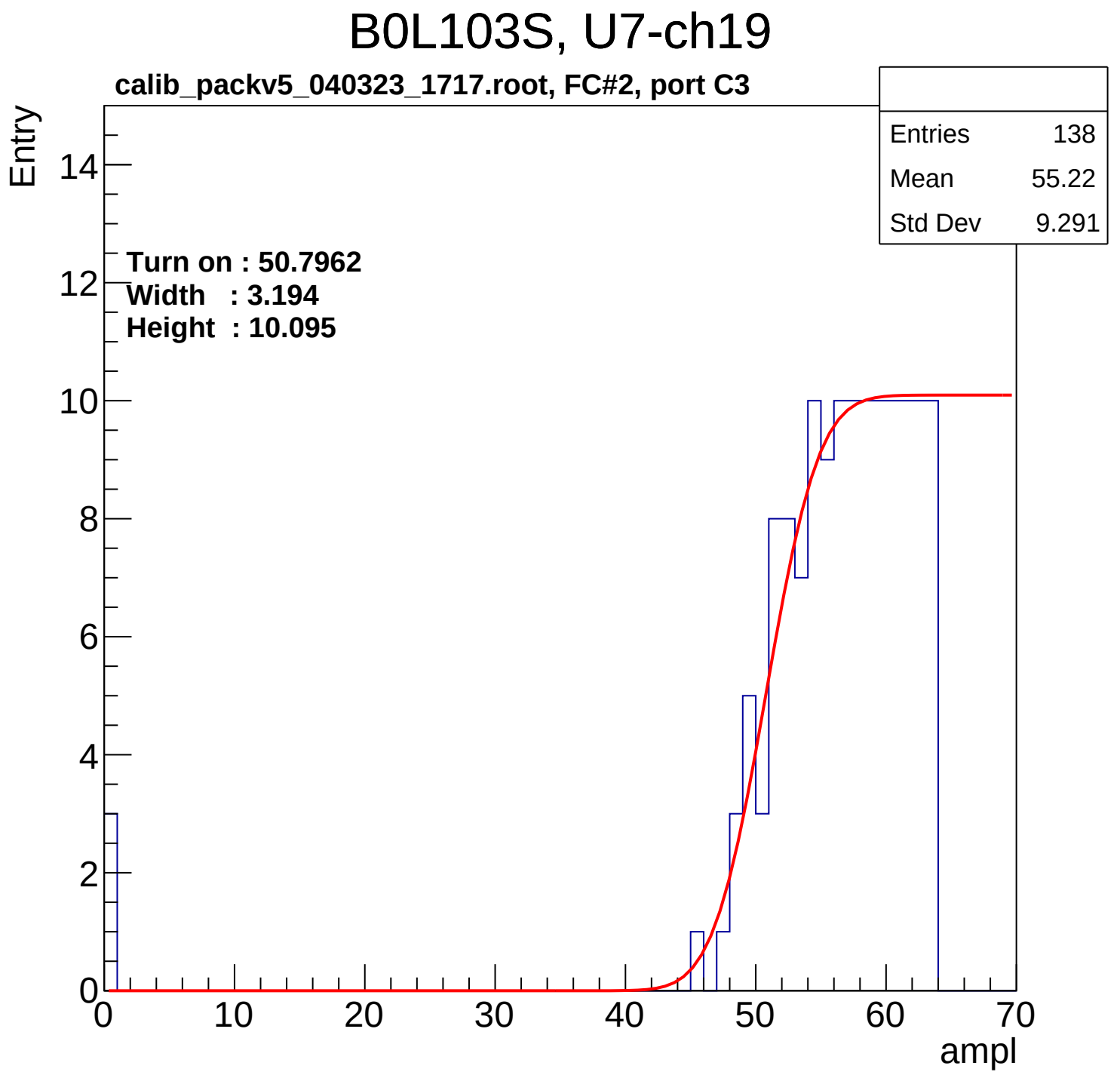
B0L103S, U7-ch19
calib_packv5_040323_1717.root, FC#2, port C3
Entries 138
Mean 55.22
Std Dev 9.291
Turn on : 50.7962
Width : 3.194
Height : 10.095
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ampl
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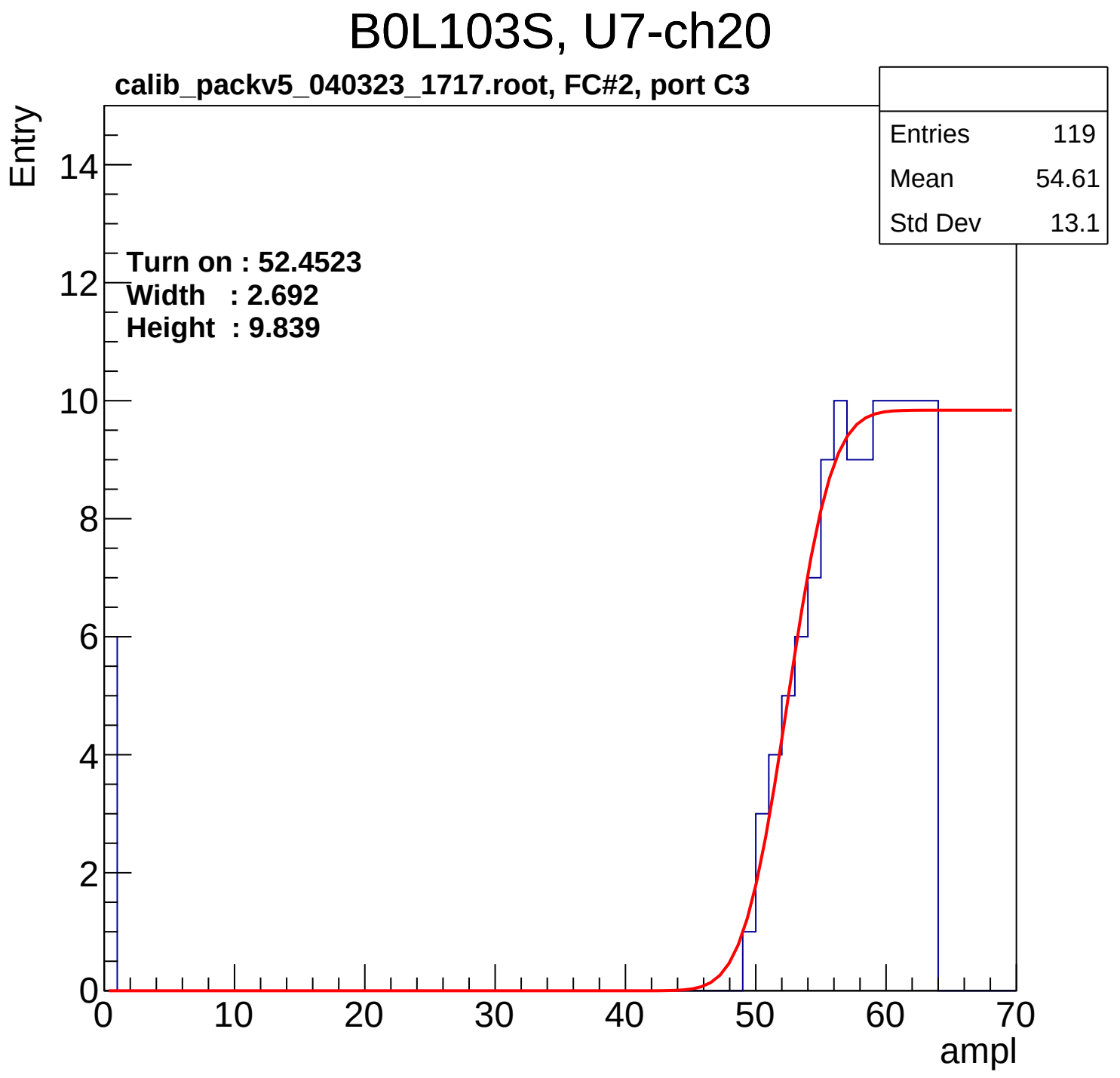
B0L103S, U7-ch20
calib_packv5_040323_1717.root, FC#2, port C3
Entries 119
Mean 54.61
Std Dev 13.1
Turn on : 52.4523
Width : 2.692
Height : 9.839
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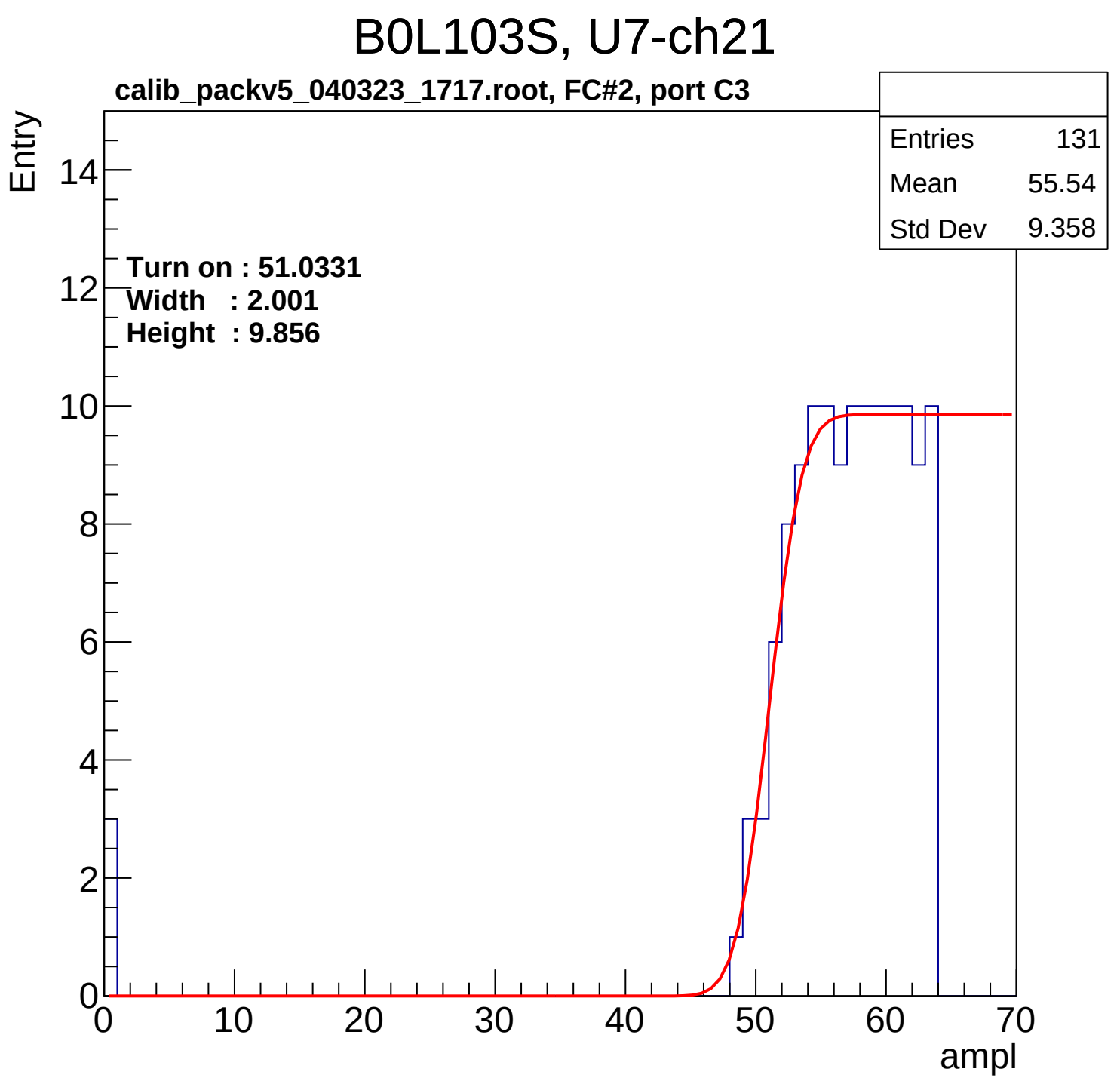
B0L103S, U7-ch21
calib_packv5_040323_1717.root, FC#2, port C3
Entries 131
Mean 55.54
Std Dev 9.358
Turn on : 51.0331
Width : 2.001
Height : 9.856
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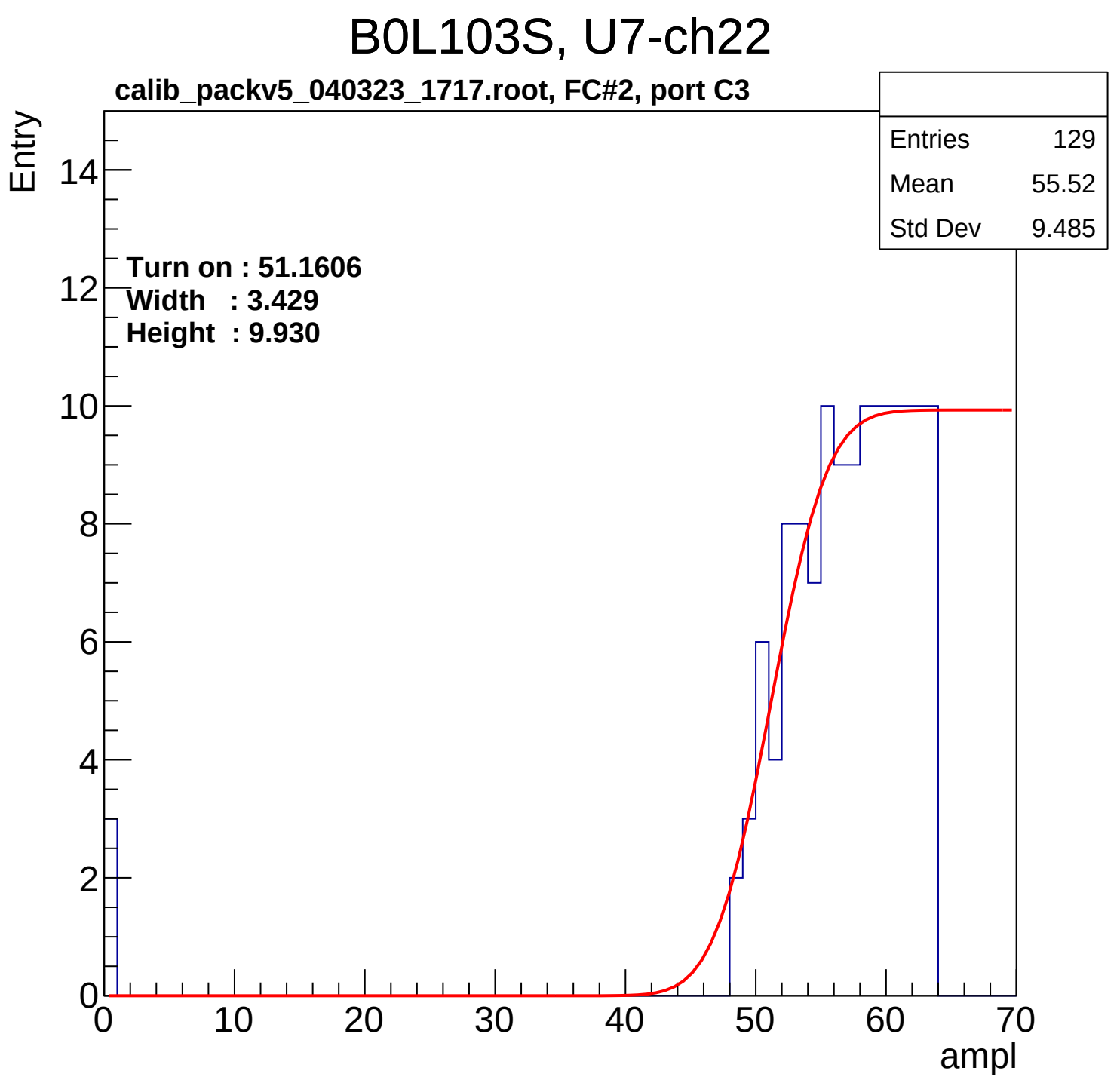
B0L103S, U7-ch22
calib_packv5_040323_1717.root, FC#2, port C3
Entries 129
Mean 55.52
Std Dev 9.485
Turn on : 51.1606
Width : 3.429
Height : 9.930
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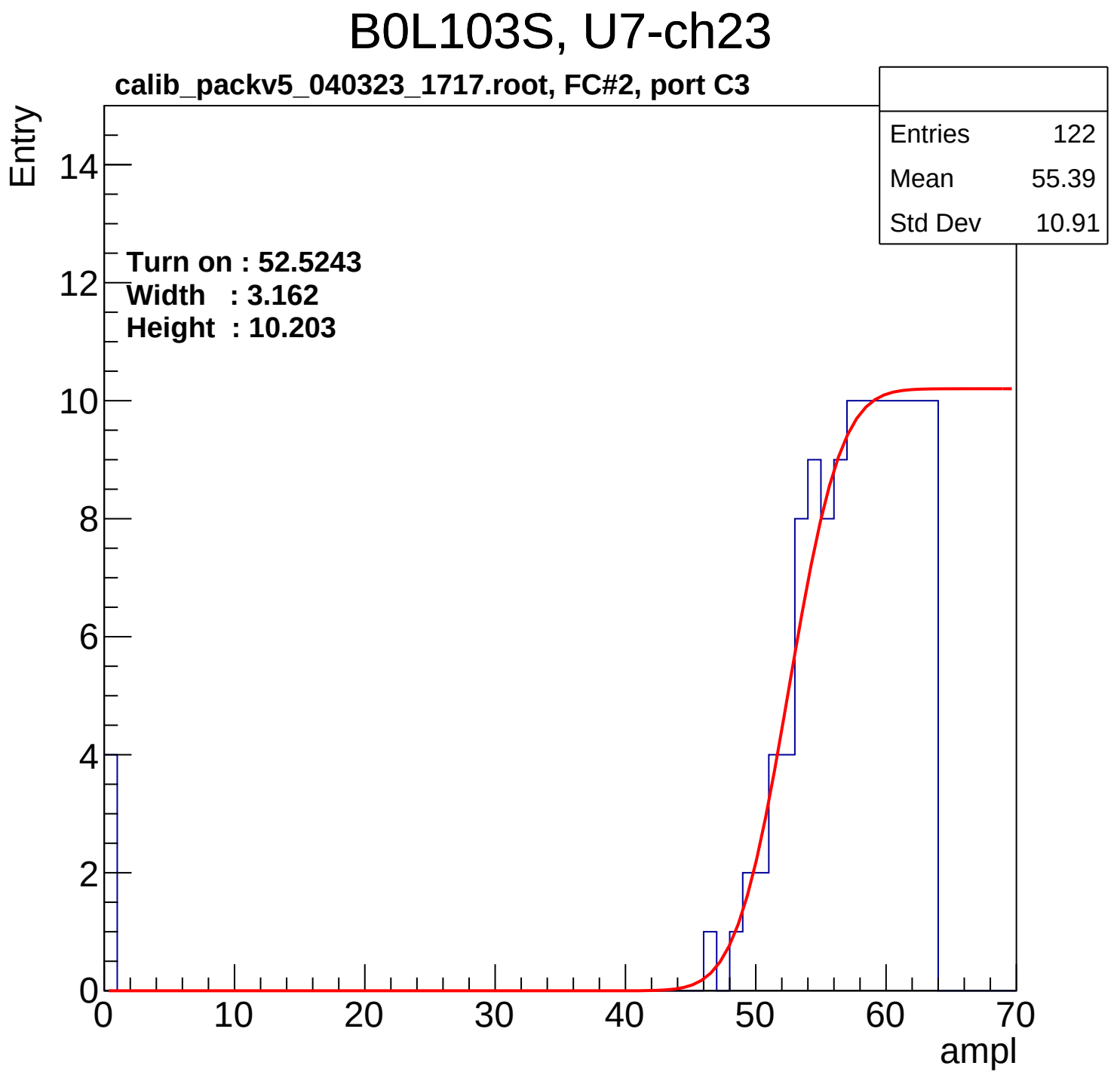
B0L103S, U7-ch23
calib_packv5_040323_1717.root, FC#2, port C3
Entries 122
Mean 55.39
Std Dev 10.91
Turn on : 52.5243
Width : 3.162
Height : 10.203
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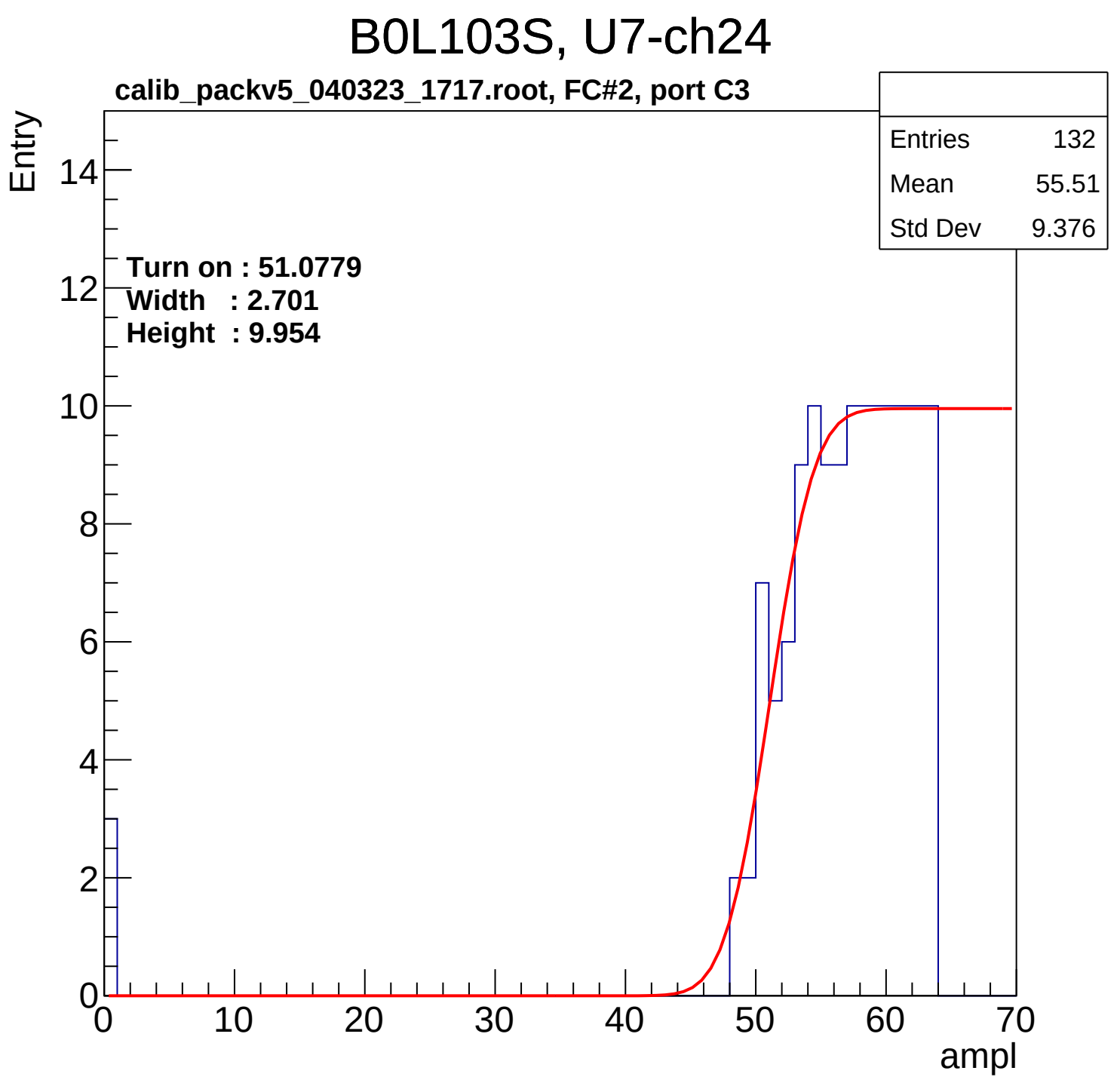
B0L103S, U7-ch24
calib_packv5_040323_1717.root, FC#2, port C3
Entries 132
Mean 55.51
Std Dev 9.376
Turn on : 51.0779
Width : 2.701
Height : 9.954
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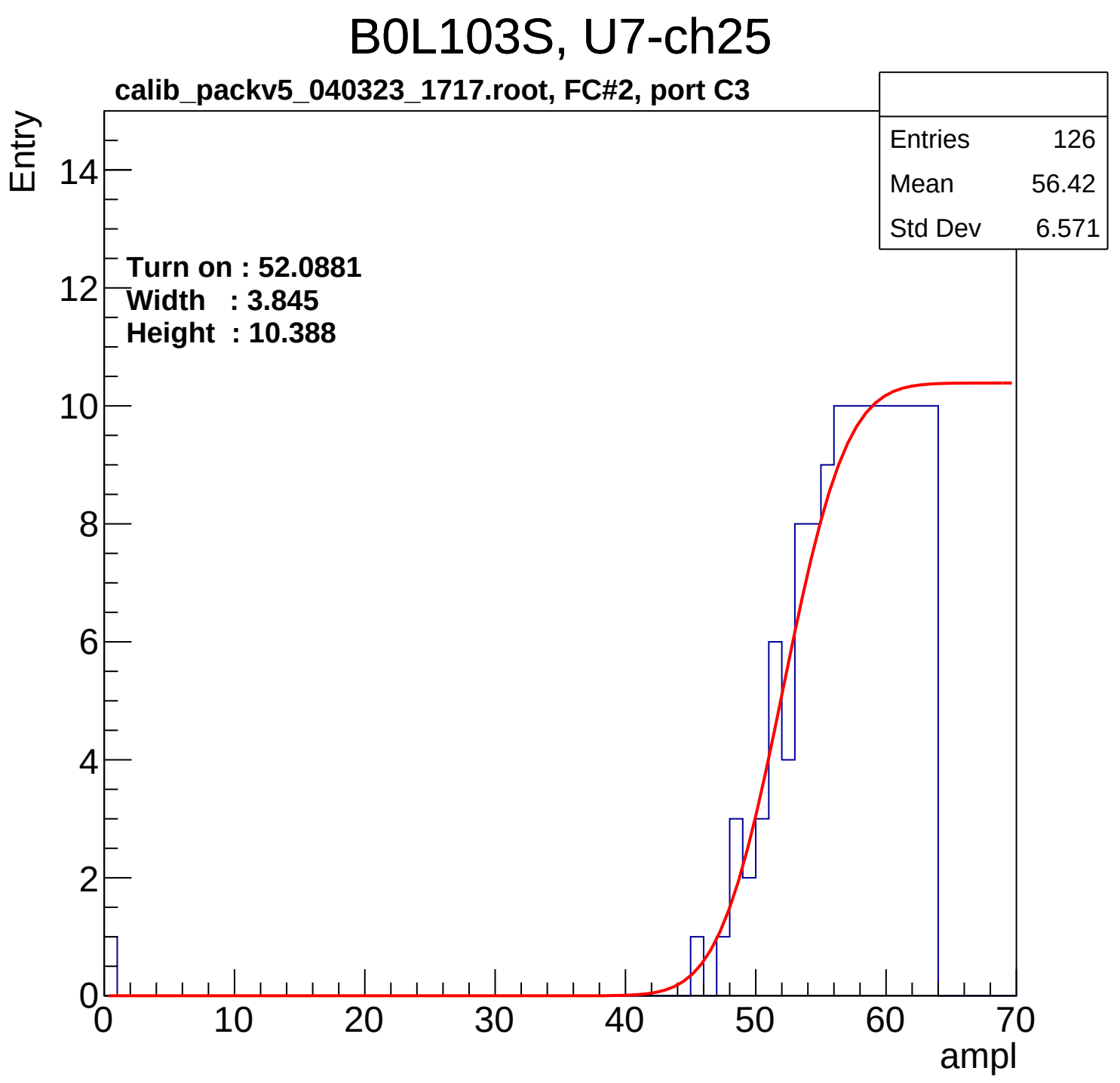
B0L103S, U7-ch25
calib_packv5_040323_1717.root, FC#2, port C3
Entries 126
Mean 56.42
Std Dev 6.571
Turn on : 52.0881
Width : 3.845
Height : 10.388
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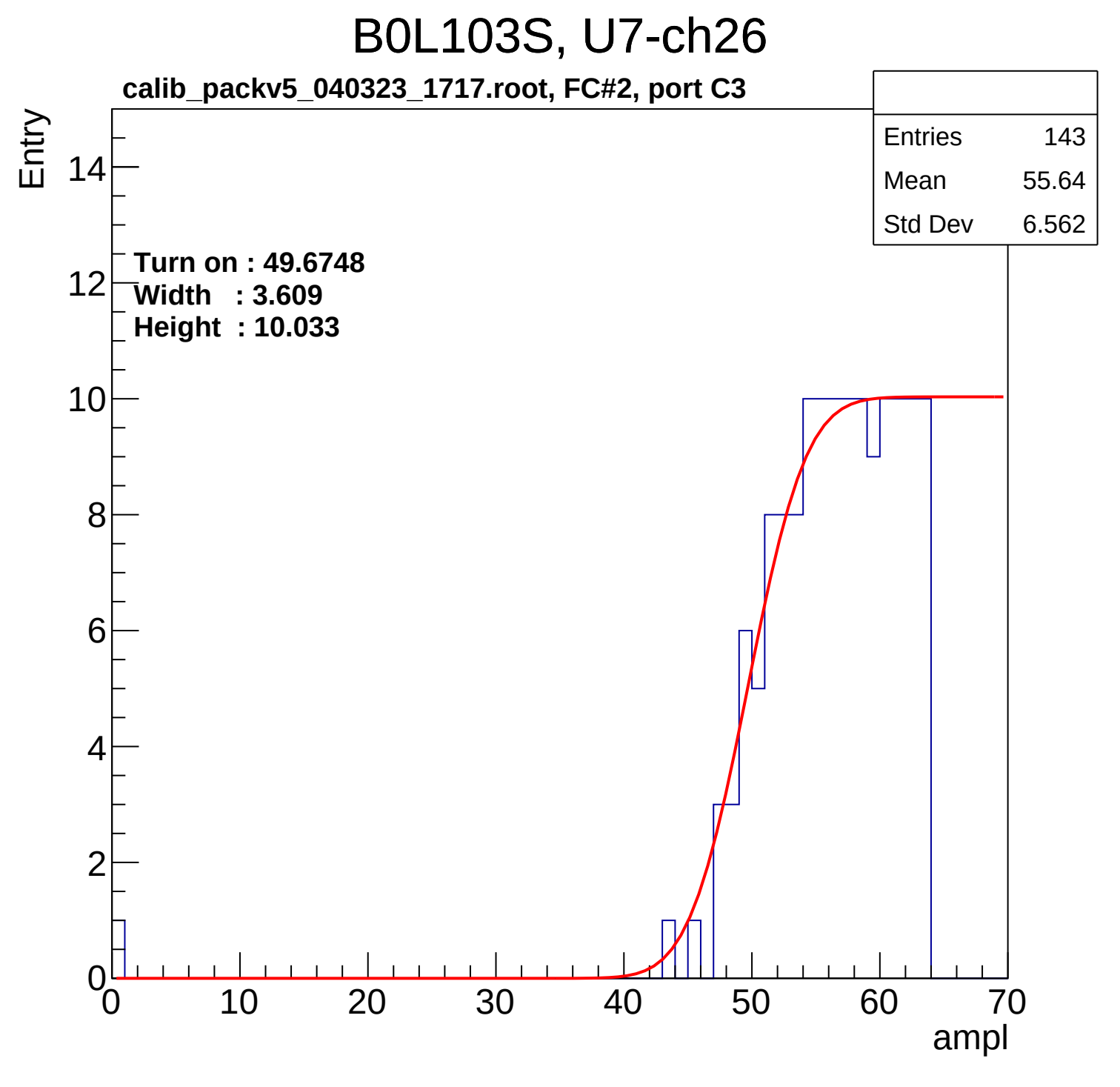
B0L103S, U7-ch26
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 55.64
Std Dev 6.562
Turn on : 49.6748
Width : 3.609
Height : 10.033
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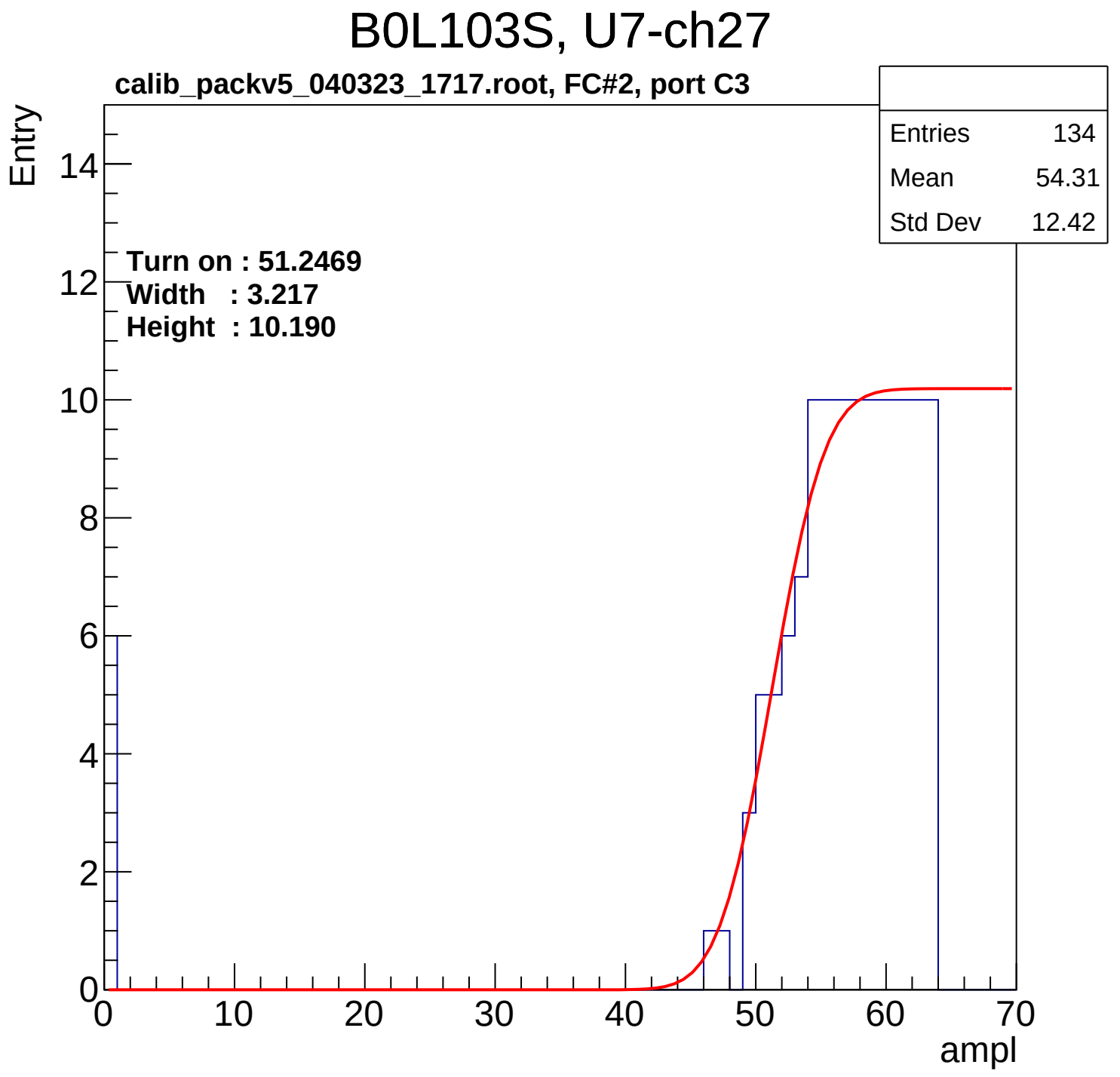
B0L103S, U7-ch27
calib_packv5_040323_1717.root, FC#2, port C3
Entries 134
Mean 54.31
Std Dev 12.42
Turn on : 51.2469
Width : 3.217
Height : 10.190
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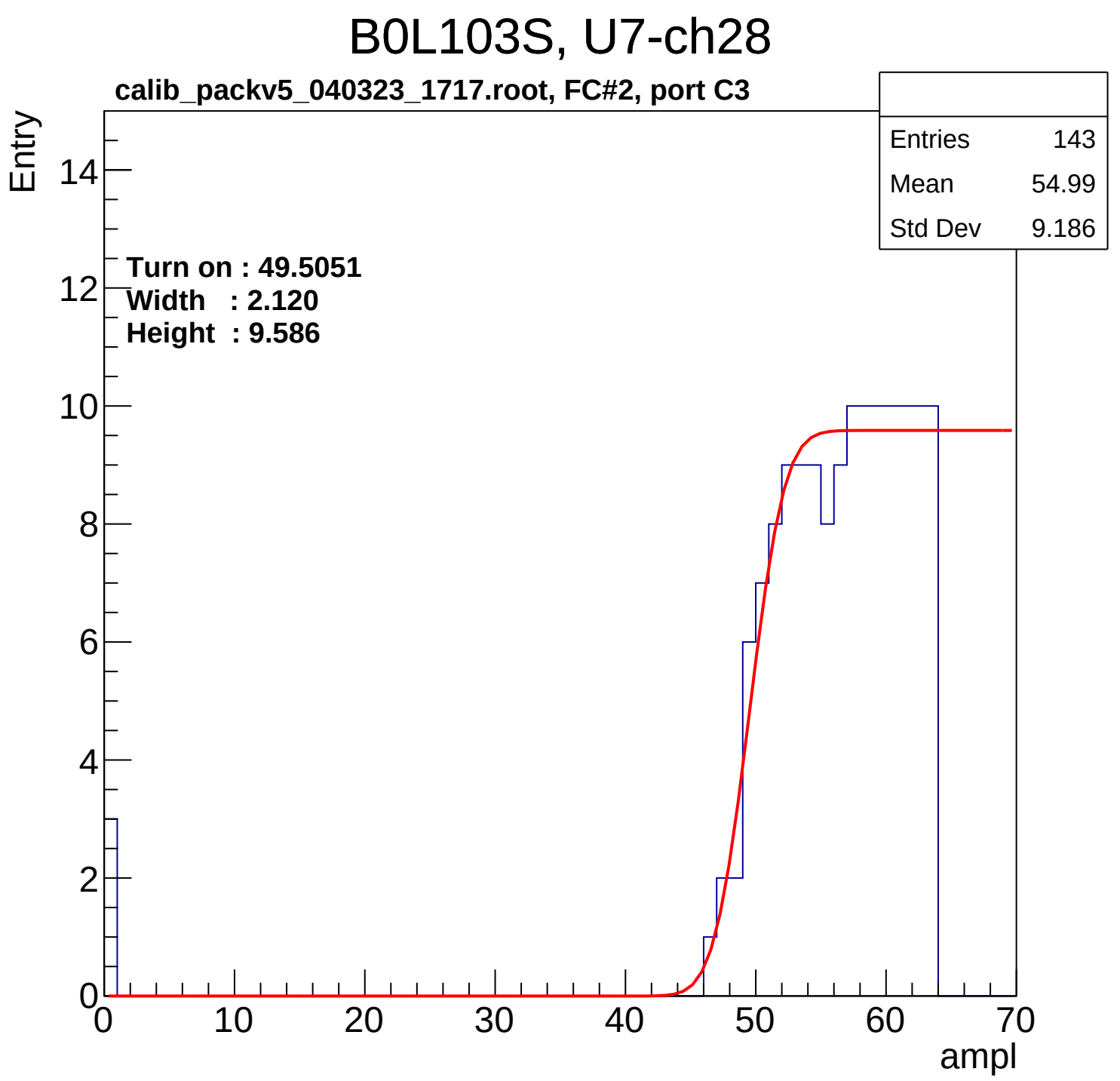
B0L103S, U7-ch28
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 54.99
Std Dev 9.186
Turn on : 49.5051
Width : 2.120
Height : 9.586
Entry
ampl
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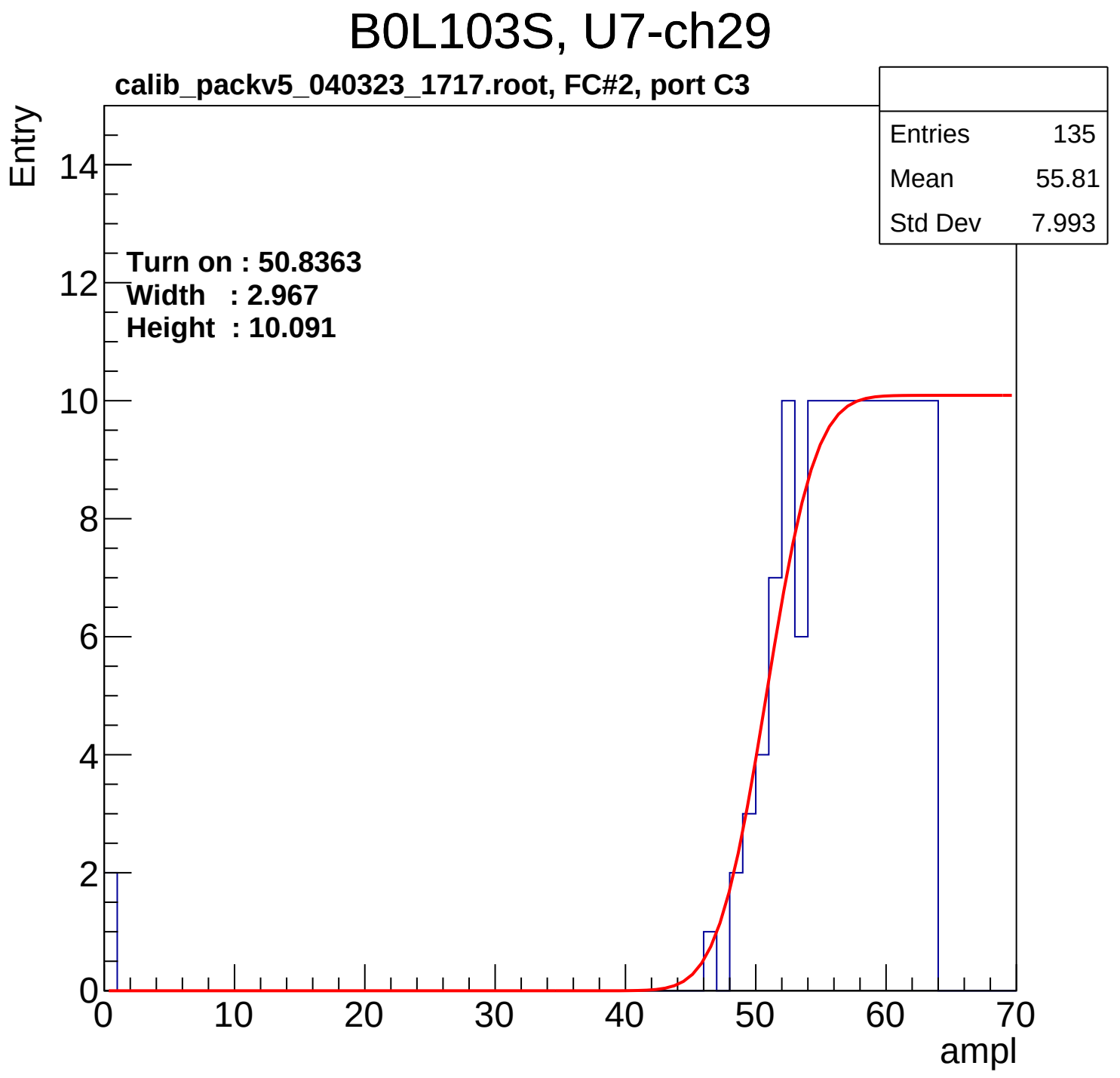
B0L103S, U7-ch29
calib_packv5_040323_1717.root, FC#2, port C3
Entries 135
Mean 55.81
Std Dev 7.993
Turn on : 50.8363
Width : 2.967
Height : 10.091
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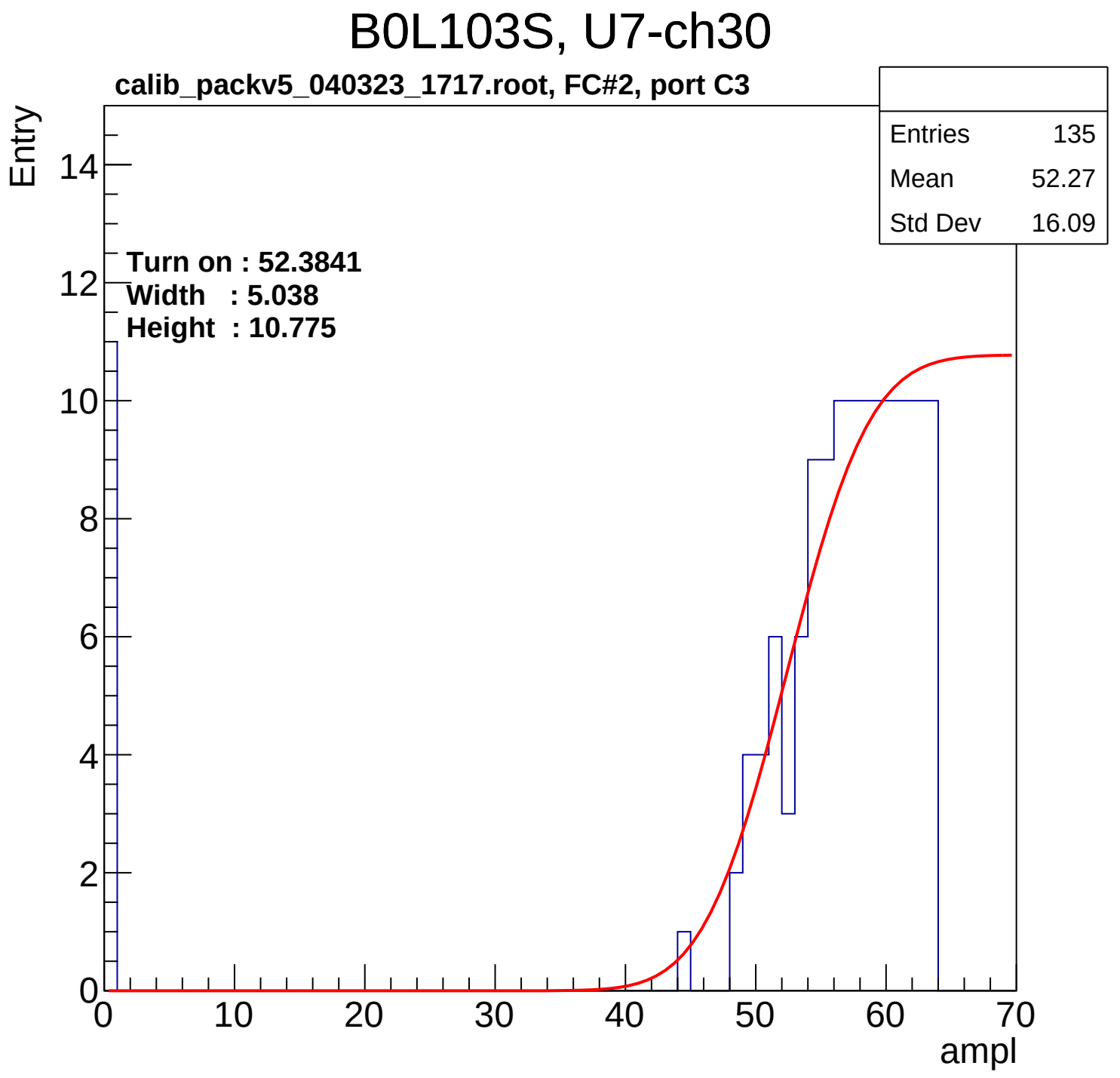
B0L103S, U7-ch30
calib_packv5_040323_1717.root, FC#2, port C3
Entries 135
Mean 52.27
Std Dev 16.09
Turn on : 52.3841
Width : 5.038
Height : 10.775
Entry
ampl
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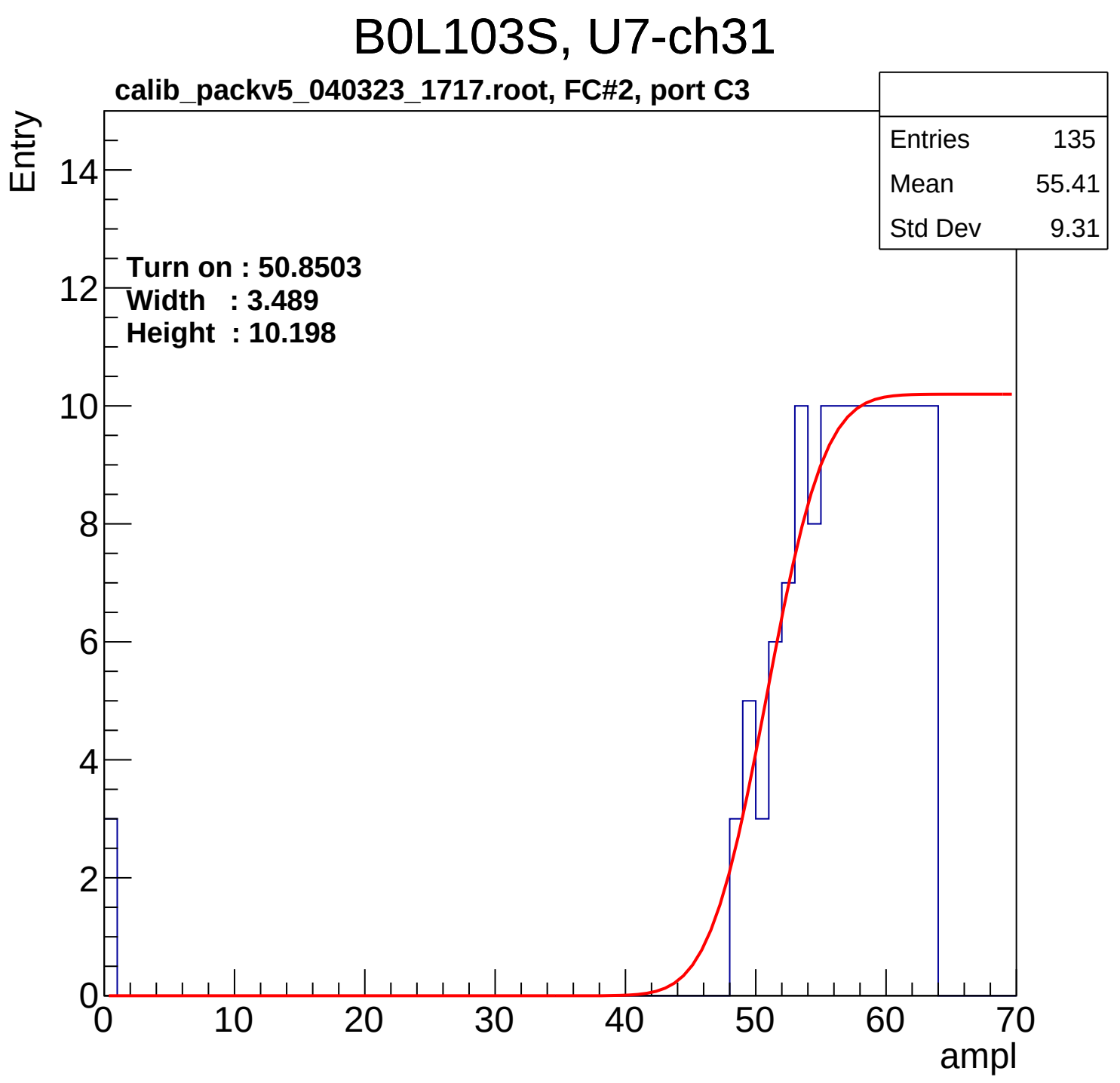
B0L103S, U7-ch31
calib_packv5_040323_1717.root, FC#2, port C3
Entries 135
Mean 55.41
Std Dev 9.31
Turn on : 50.8503
Width : 3.489
Height : 10.198
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ampl
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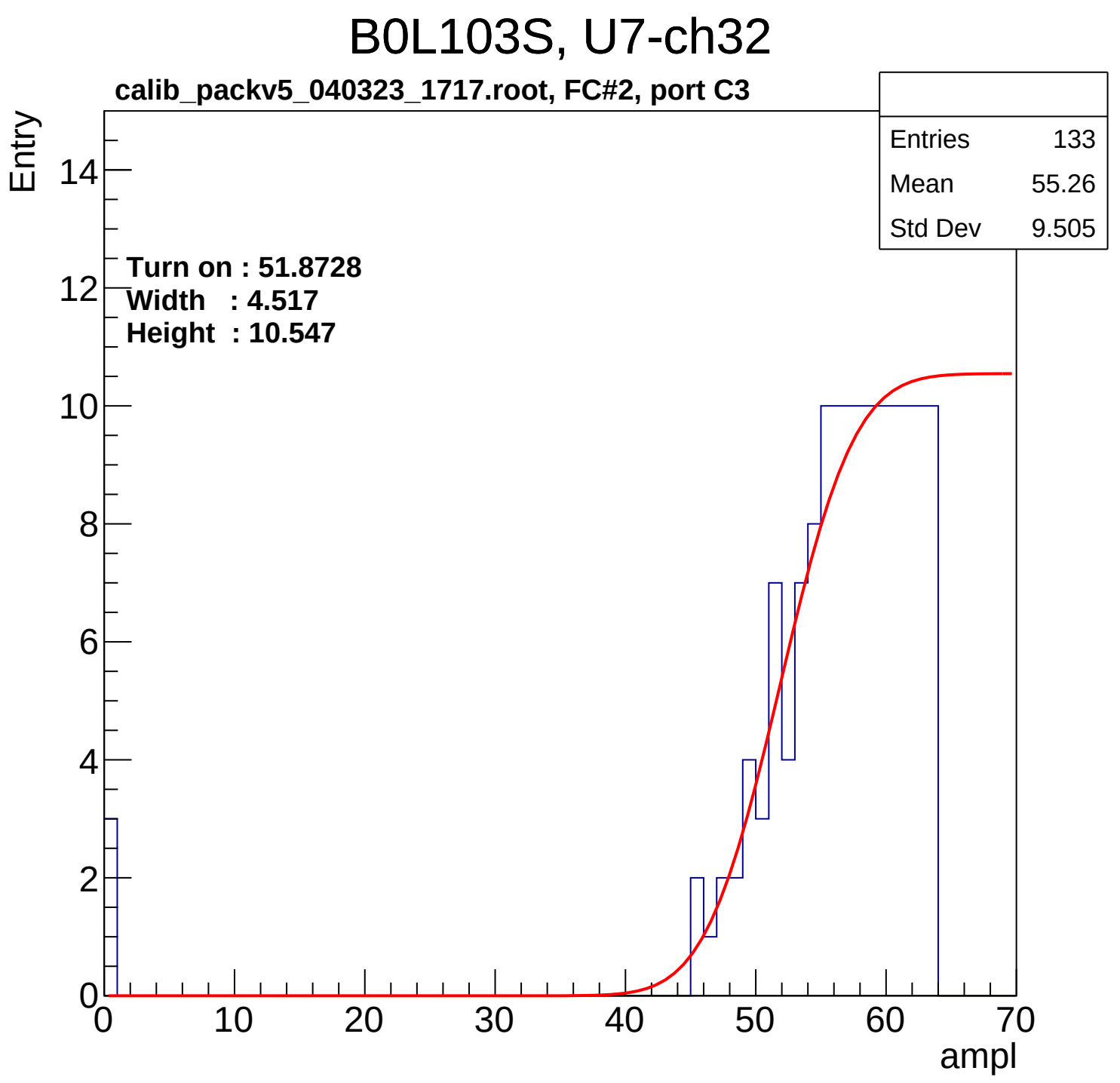
B0L103S, U7-ch32
calib_packv5_040323_1717.root, FC#2, port C3
Entries 133
Mean 55.26
Std Dev 9.505
Turn on : 51.8728
Width : 4.517
Height : 10.547
Entry
ampl
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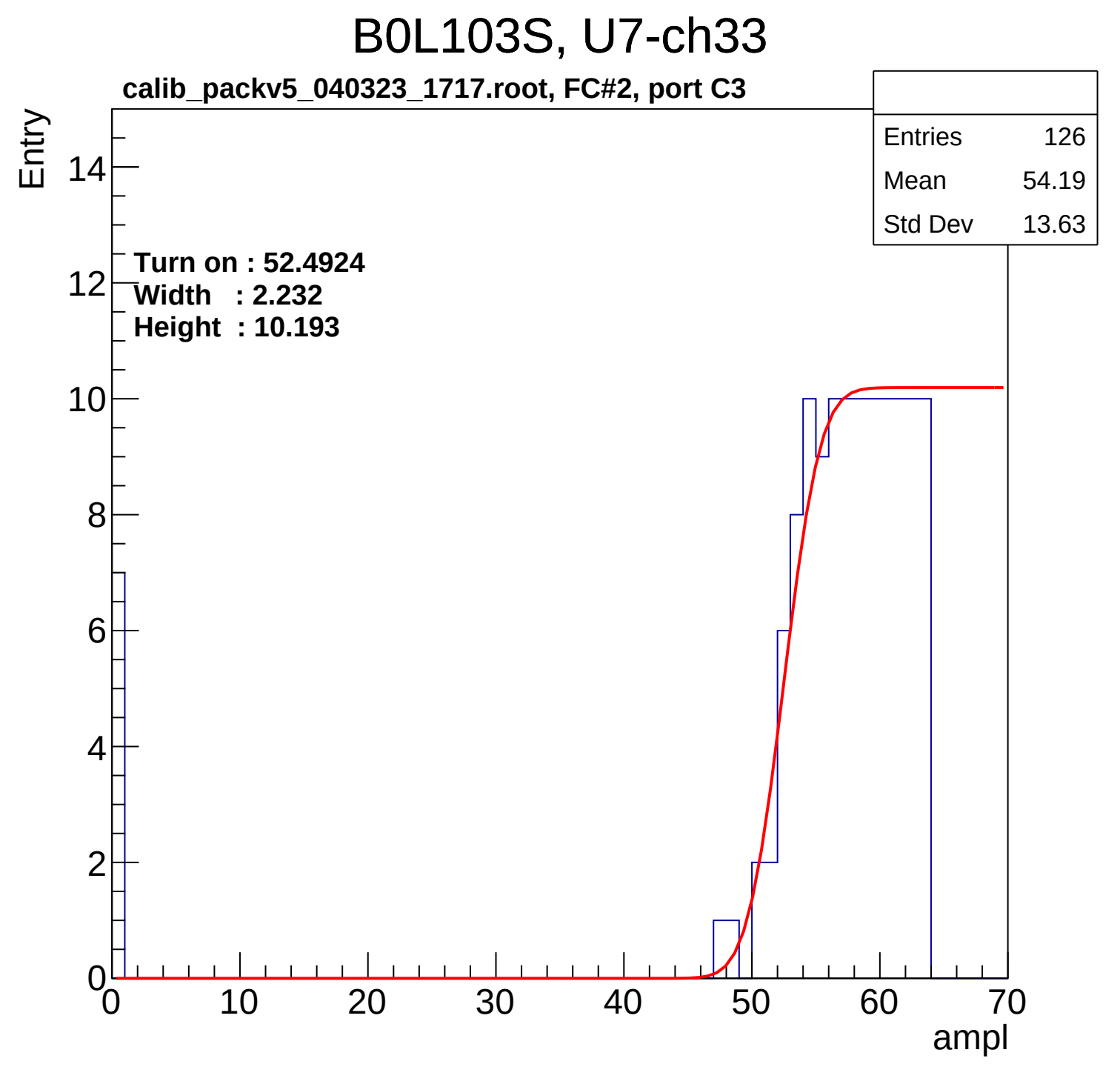
B0L103S, U7-ch33
calib_packv5_040323_1717.root, FC#2, port C3
Entries 126
Mean 54.19
Std Dev 13.63
Turn on : 52.4924
Width : 2.232
Height : 10.193
Entry
ampl
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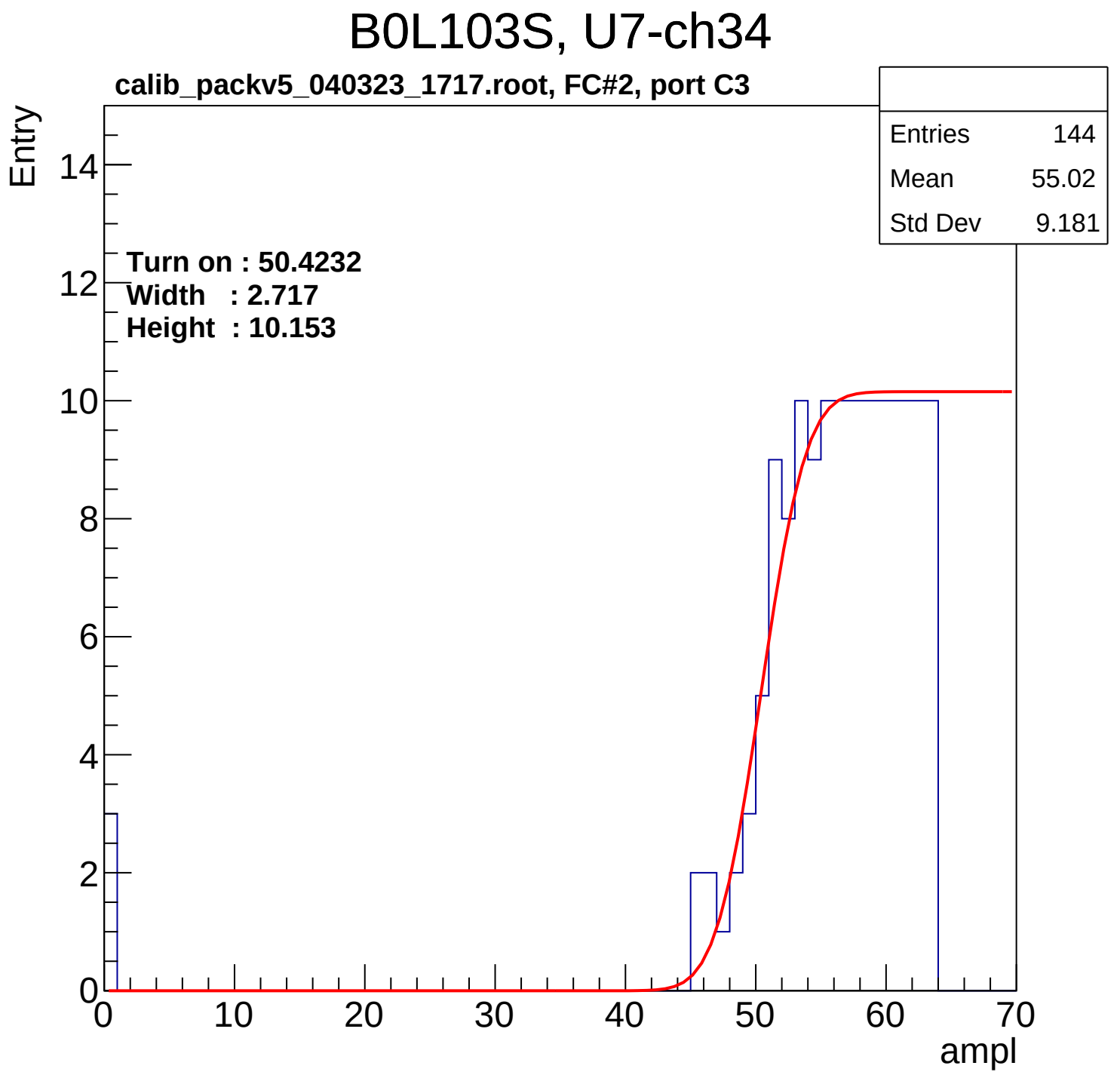
B0L103S, U7-ch34
calib_packv5_040323_1717.root, FC#2, port C3
Entries 144
Mean 55.02
Std Dev 9.181
Turn on : 50.4232
Width : 2.717
Height : 10.153
Entry
ampl
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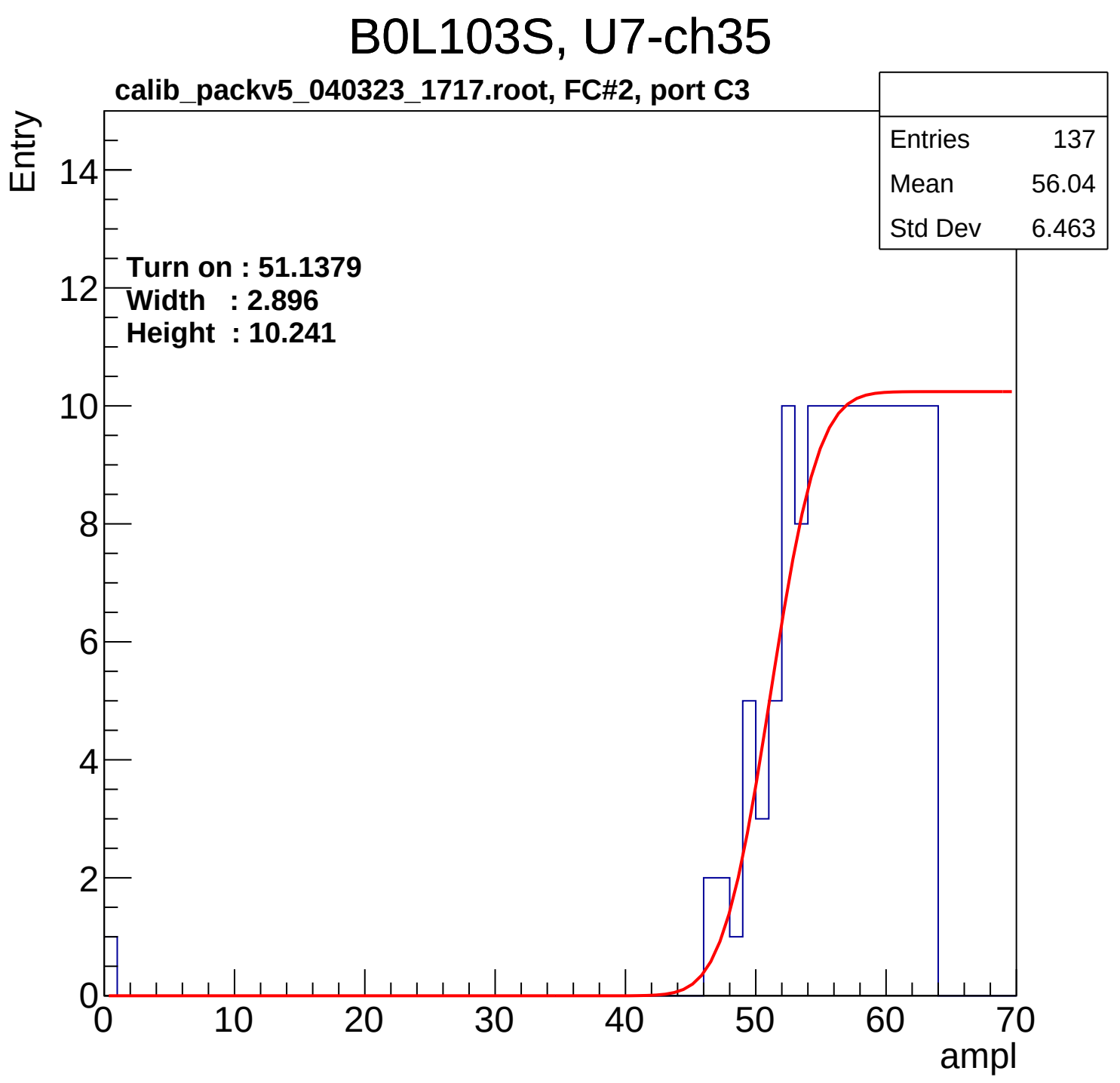
B0L103S, U7-ch35
calib_packv5_040323_1717.root, FC#2, port C3
Entries 137
Mean 56.04
Std Dev 6.463
Turn on : 51.1379
Width : 2.896
Height : 10.241
Entry
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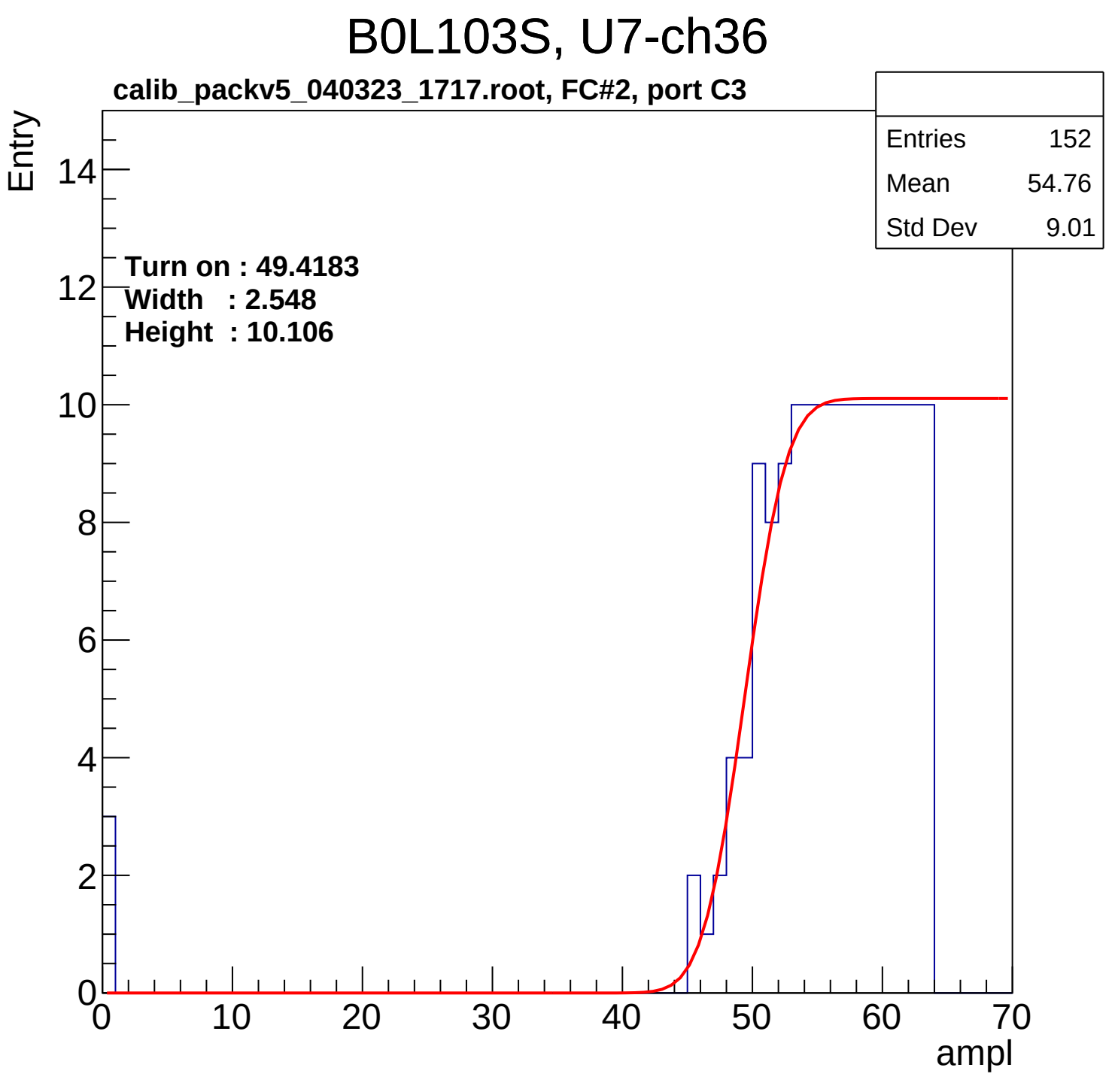
B0L103S, U7-ch36
calib_packv5_040323_1717.root, FC#2, port C3
Entries 152
Mean 54.76
Std Dev 9.01
Turn on : 49.4183
Width : 2.548
Height : 10.106
Entry
ampl
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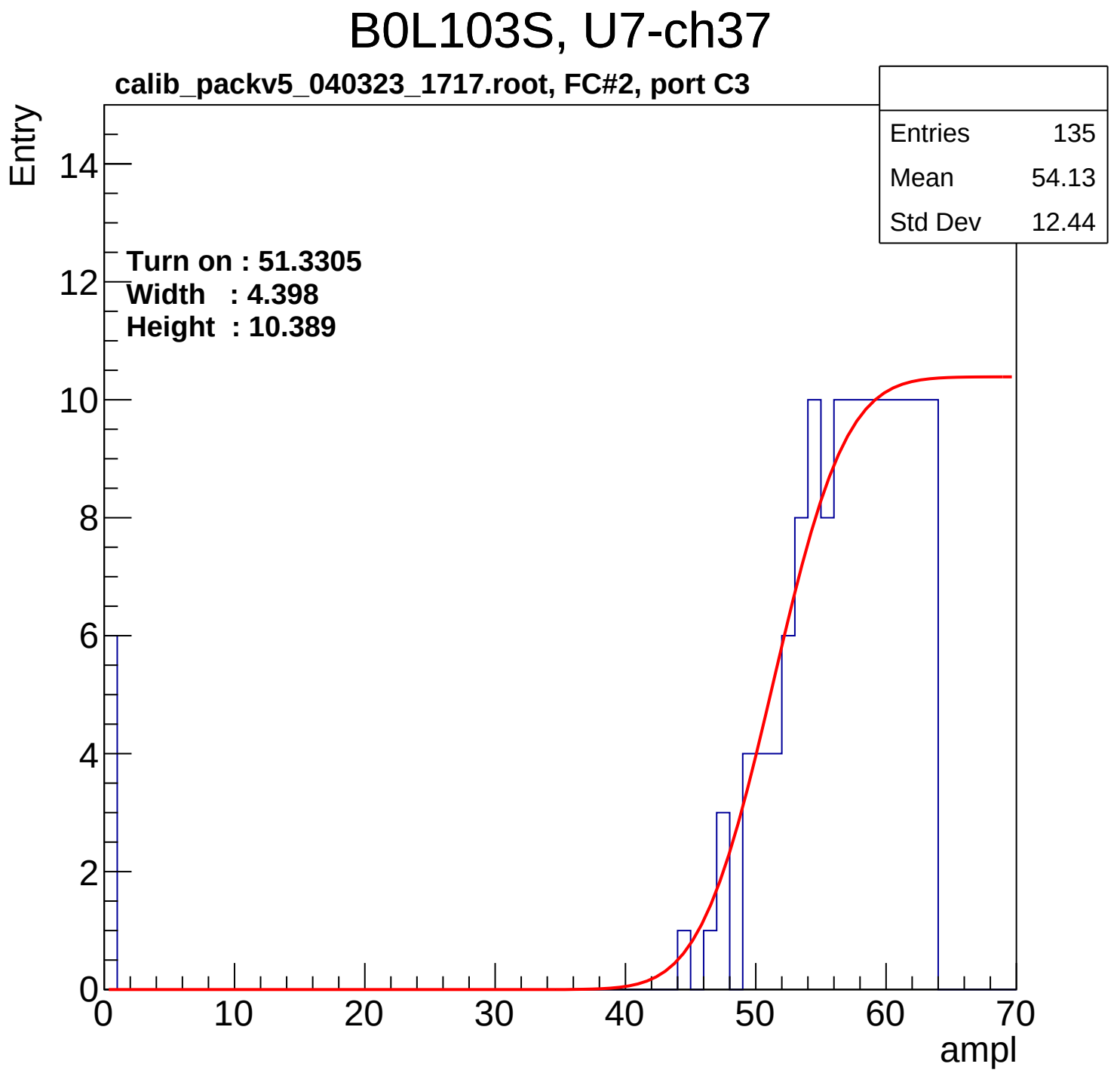
B0L103S, U7-ch37
calib_packv5_040323_1717.root, FC#2, port C3
Entries 135
Mean 54.13
Std Dev 12.44
Turn on : 51.3305
Width : 4.398
Height : 10.389
Entry
ampl
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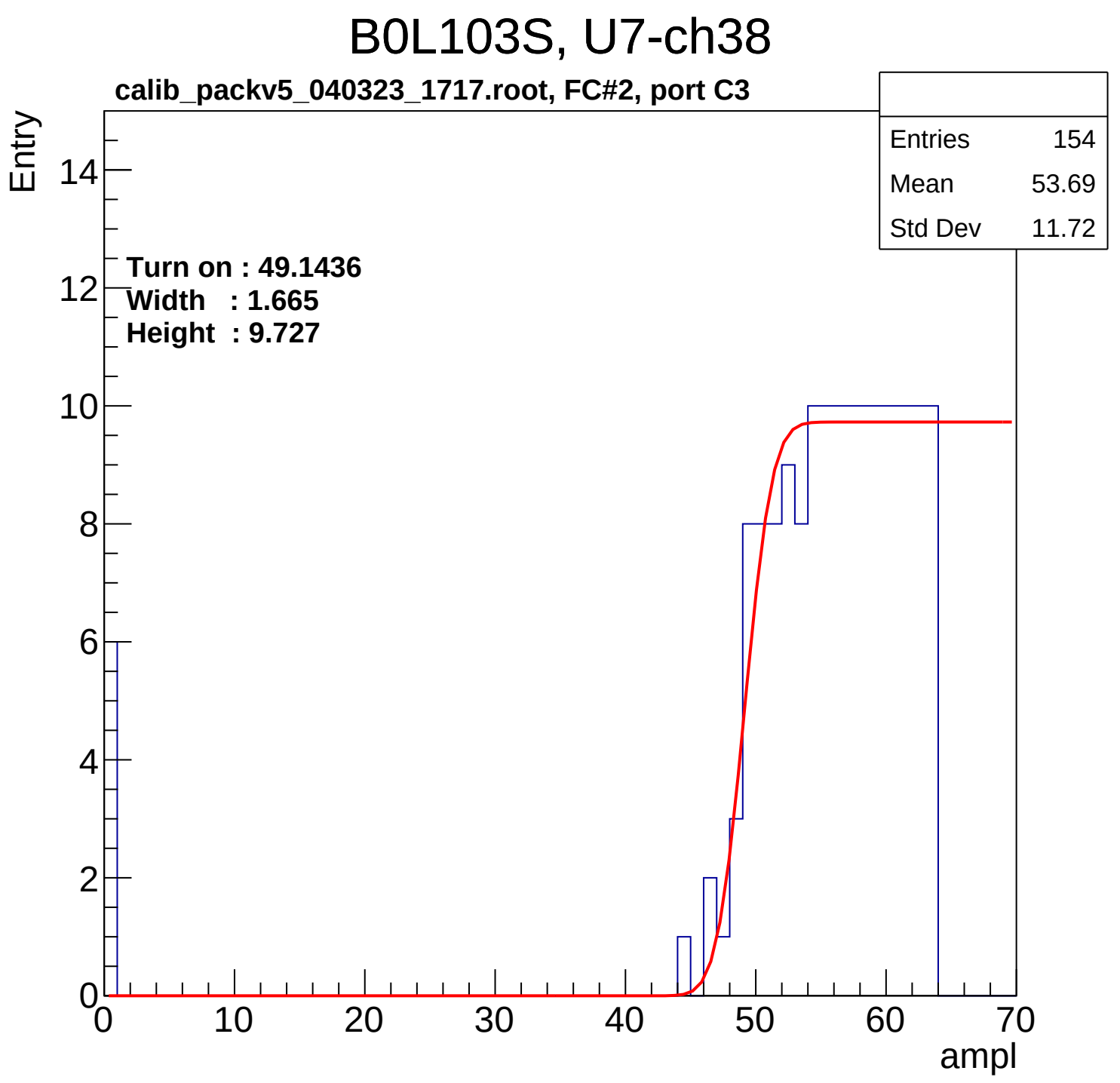
B0L103S, U7-ch38
calib_packv5_040323_1717.root, FC#2, port C3
Entries 154
Mean 53.69
Std Dev 11.72
Turn on : 49.1436
Width : 1.665
Height : 9.727
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ampl
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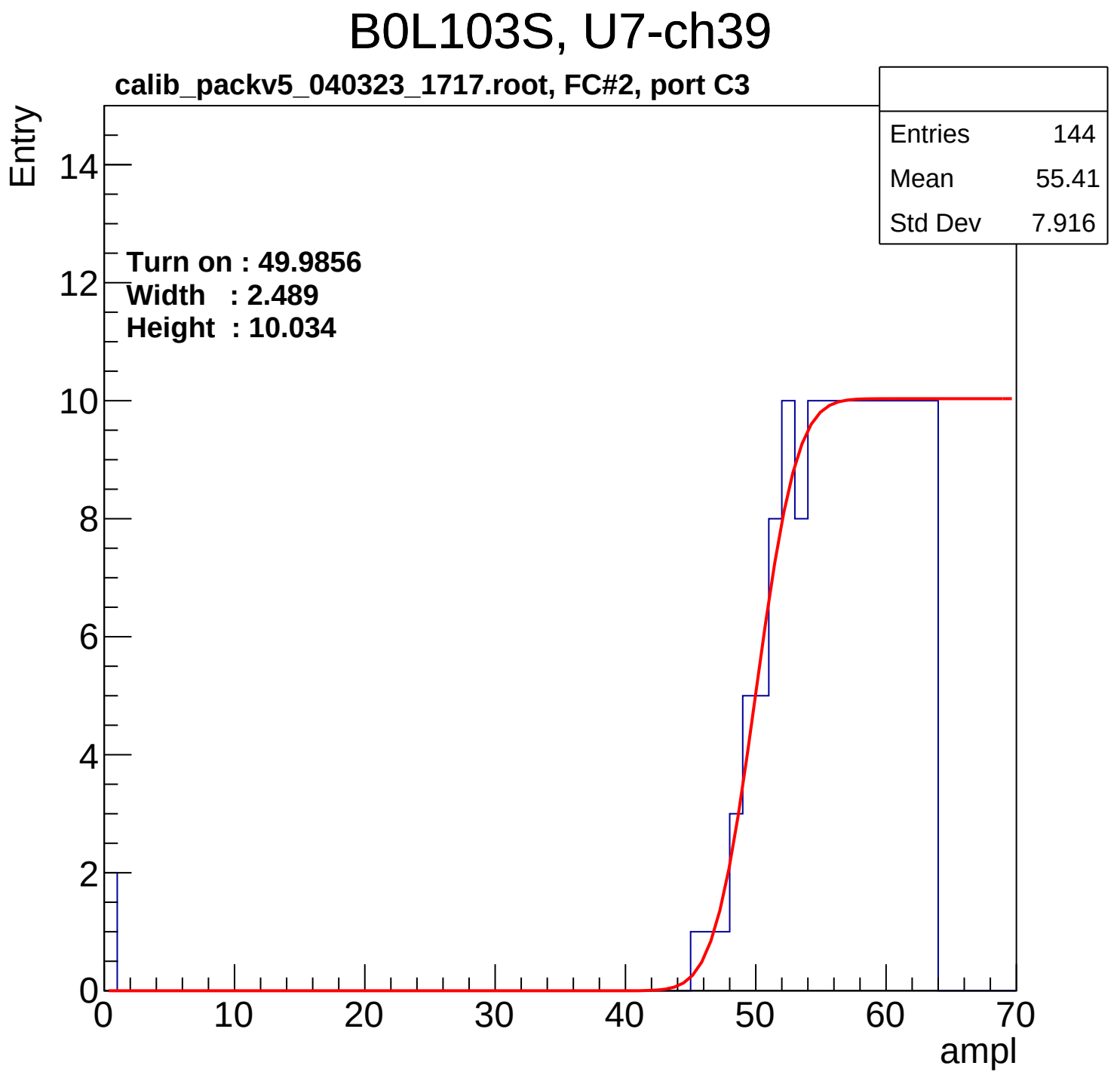
B0L103S, U7-ch39
calib_packv5_040323_1717.root, FC#2, port C3
Entries 144
Mean 55.41
Std Dev 7.916
Turn on : 49.9856
Width : 2.489
Height : 10.034
Entry
ampl
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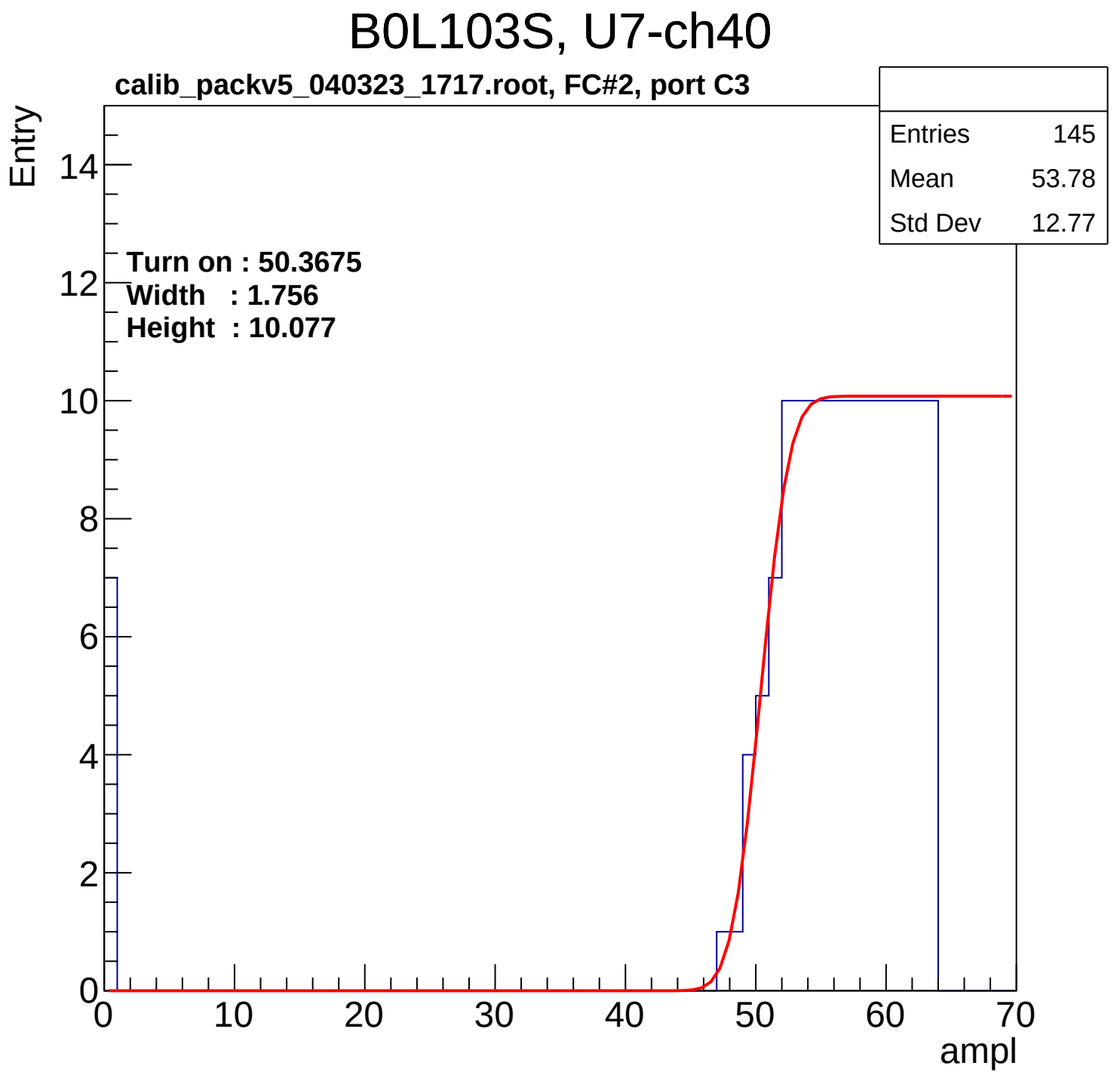
B0L103S, U7-ch40
calib_packv5_040323_1717.root, FC#2, port C3
Entries 145
Mean 53.78
Std Dev 12.77
Turn on : 50.3675
Width : 1.756
Height : 10.077
Entry
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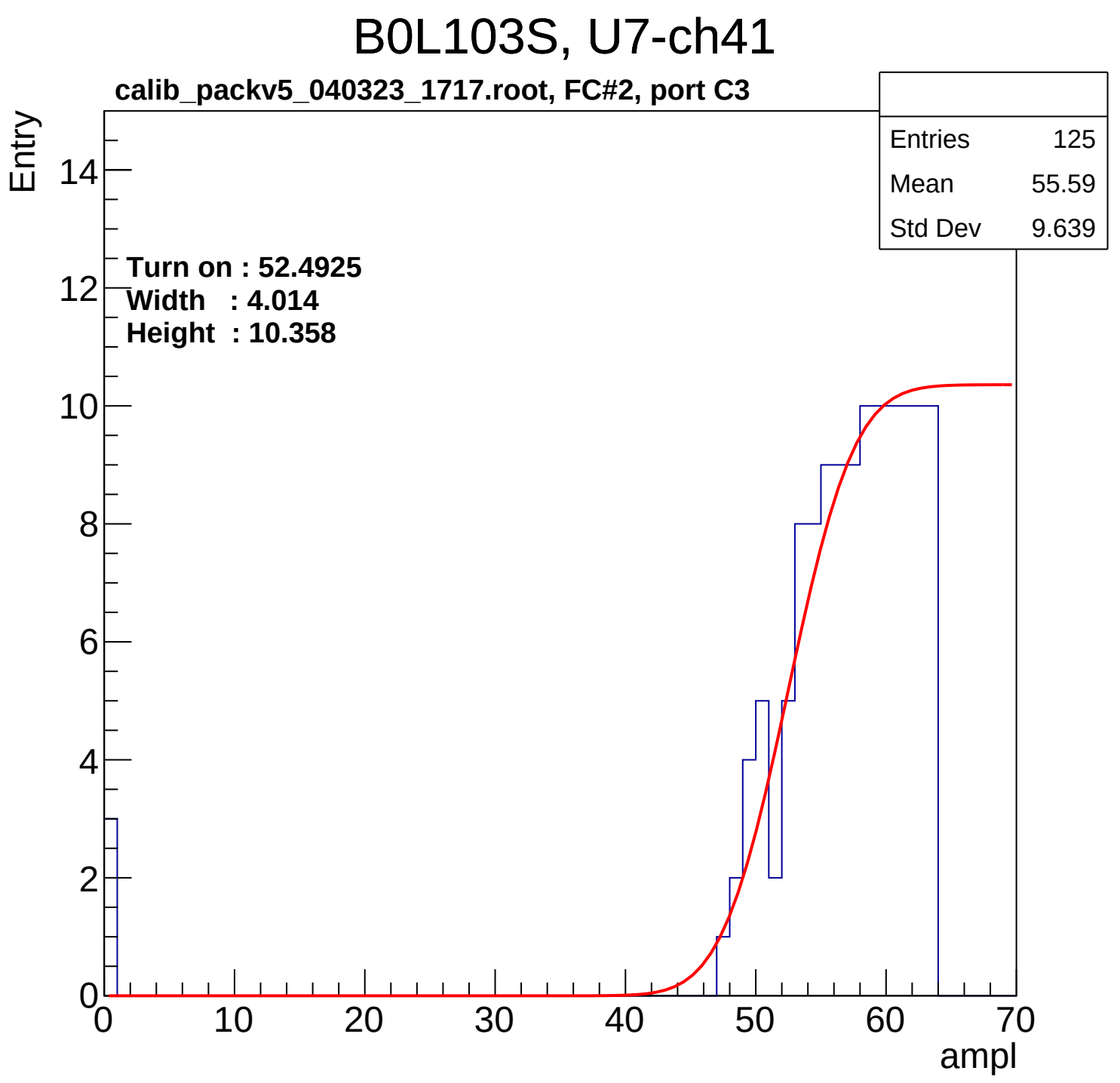
B0L103S, U7-ch41
calib_packv5_040323_1717.root, FC#2, port C3
Entries 125
Mean 55.59
Std Dev 9.639
Turn on : 52.4925
Width : 4.014
Height : 10.358
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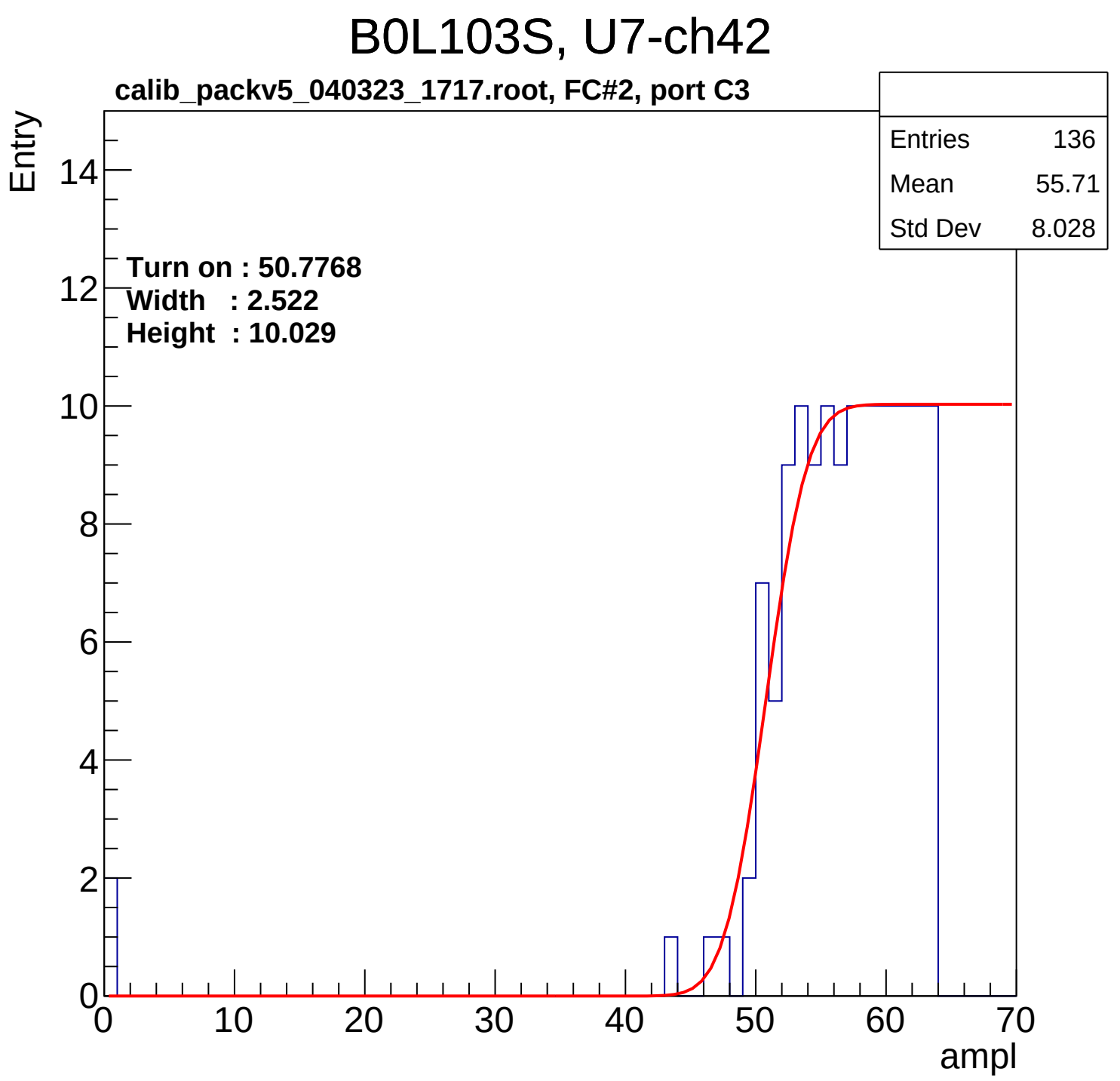
B0L103S, U7-ch42
calib_packv5_040323_1717.root, FC#2, port C3
Entries 136
Mean 55.71
Std Dev 8.028
Turn on : 50.7768
Width : 2.522
Height : 10.029
Entry
ampl
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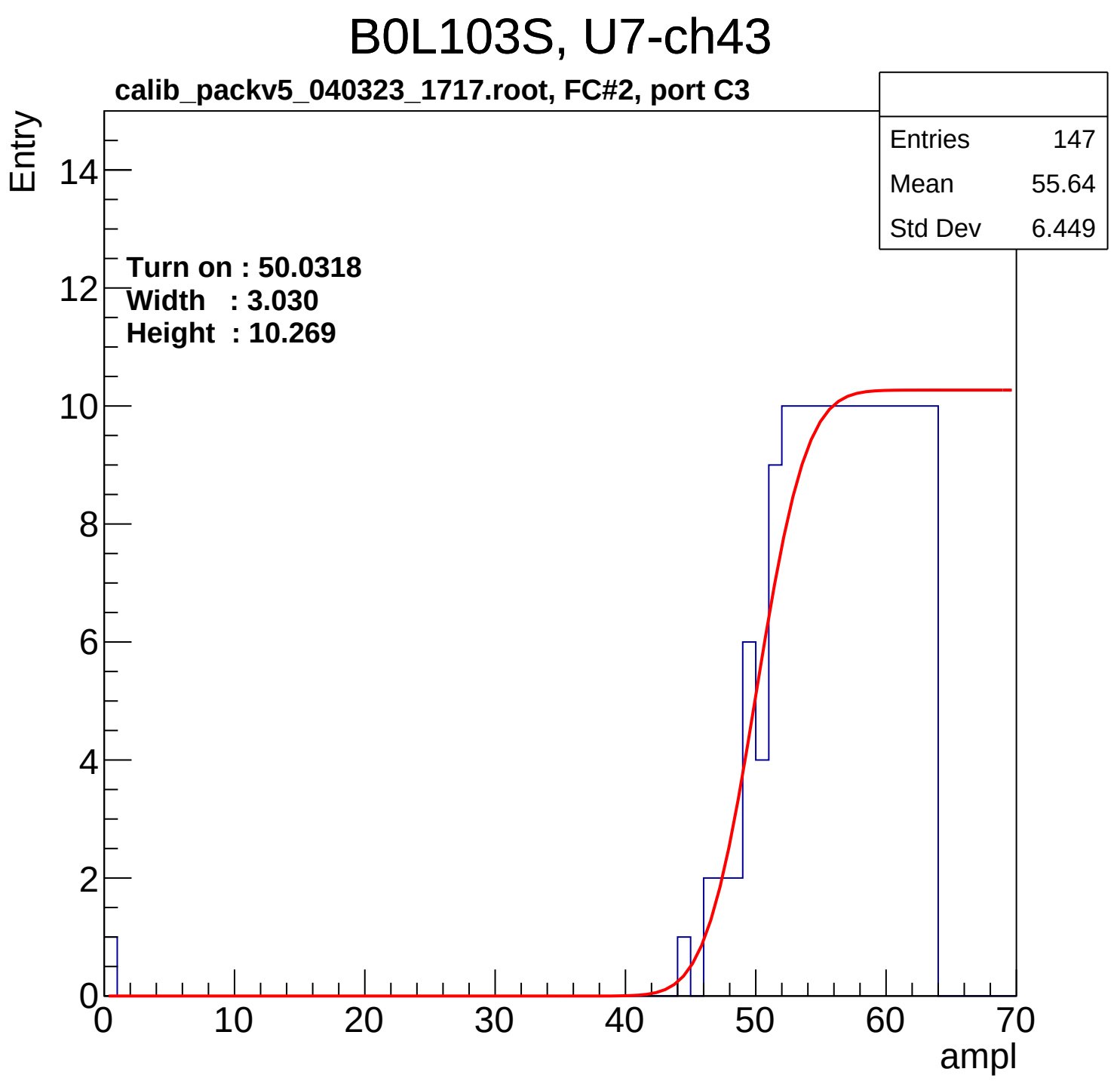
B0L103S, U7-ch43
calib_packv5_040323_1717.root, FC#2, port C3
Entries 147
Mean 55.64
Std Dev 6.449
Turn on : 50.0318
Width : 3.030
Height : 10.269
Entry
ampl
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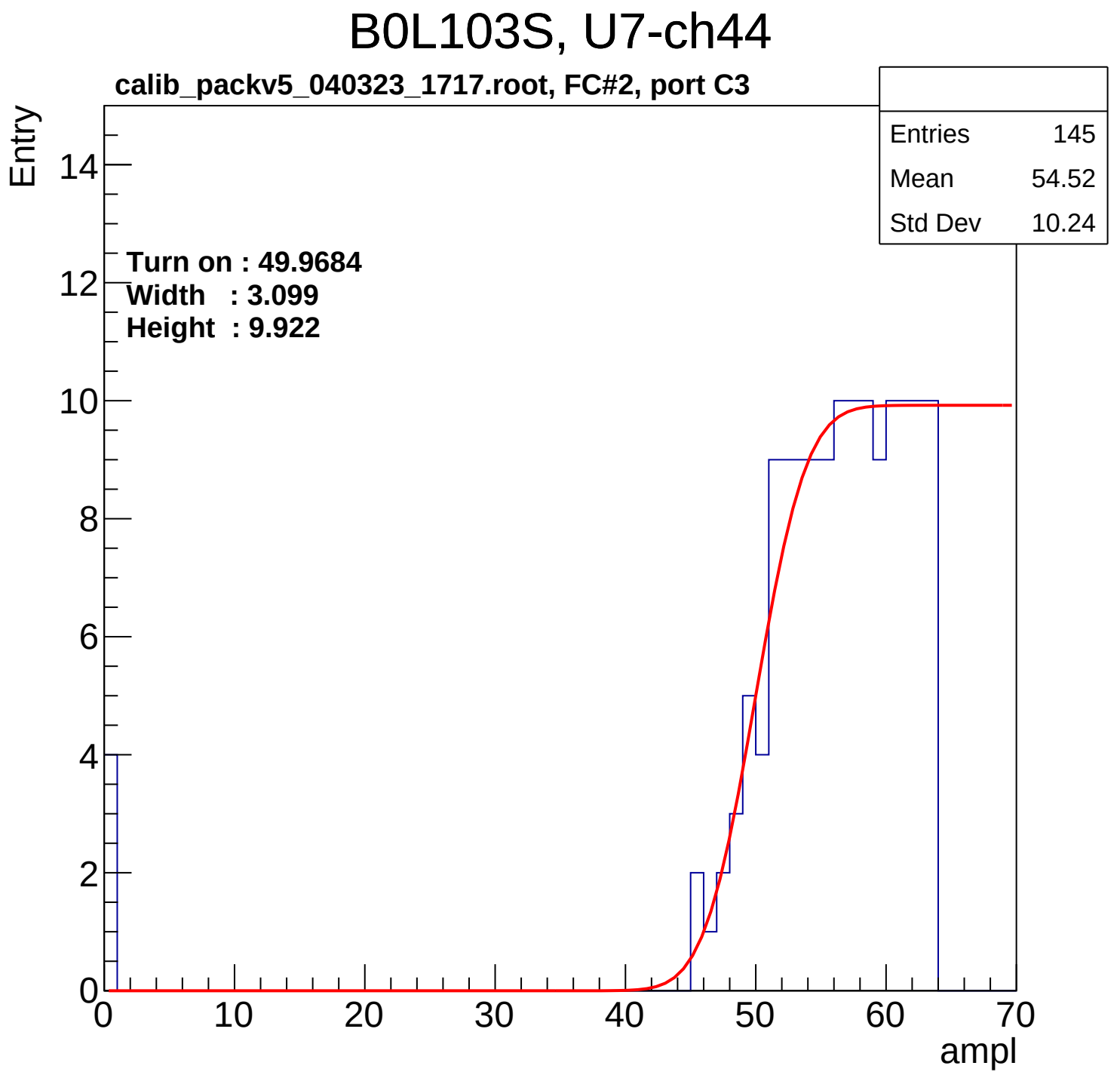
B0L103S, U7-ch44
calib_packv5_040323_1717.root, FC#2, port C3
Entries 145
Mean 54.52
Std Dev 10.24
Turn on : 49.9684
Width : 3.099
Height : 9.922
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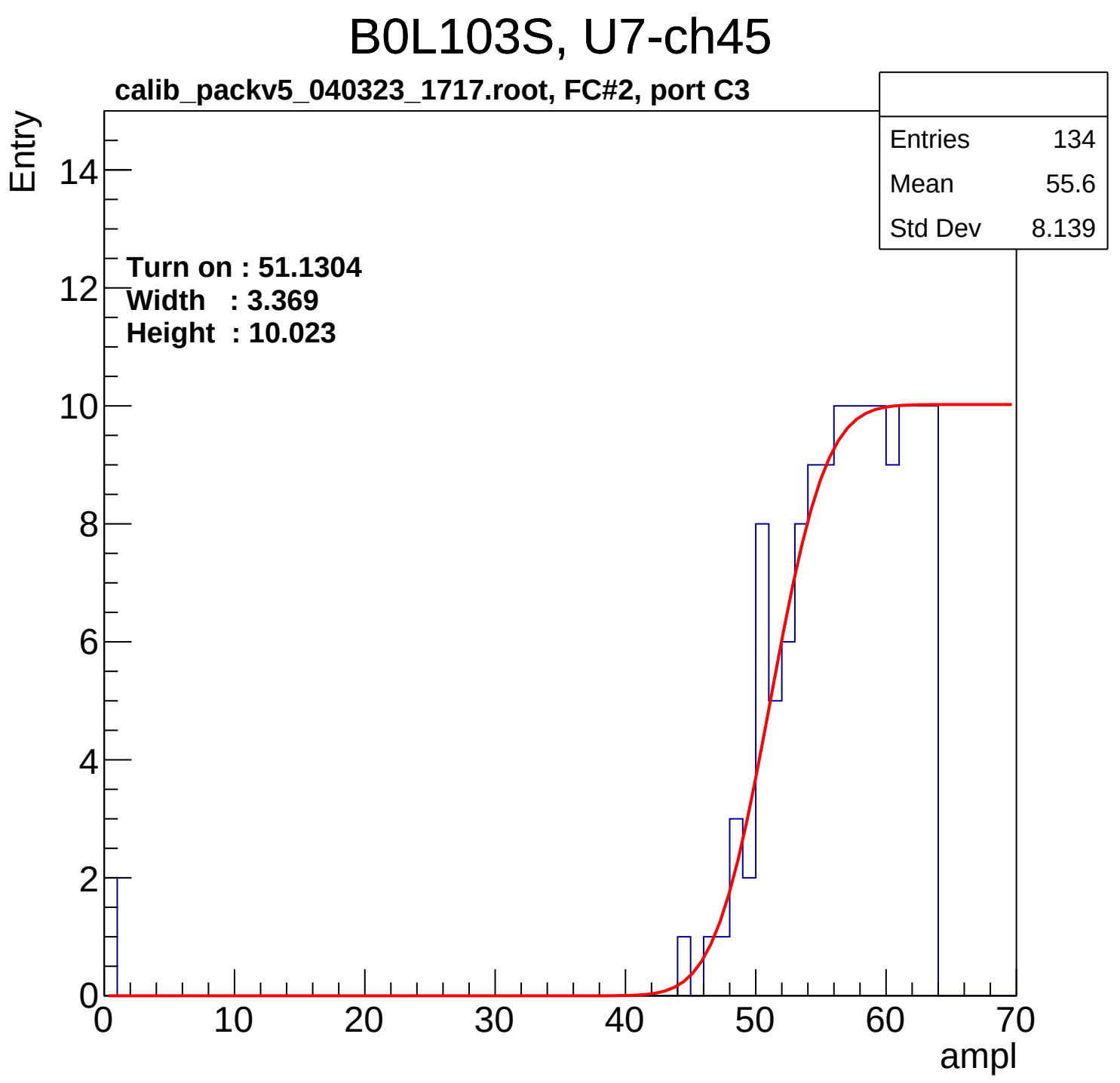
B0L103S, U7-ch45
calib_packv5_040323_1717.root, FC#2, port C3
Entries 134
Mean 55.6
Std Dev 8.139
Turn on : 51.1304
Width : 3.369
Height : 10.023
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ampl
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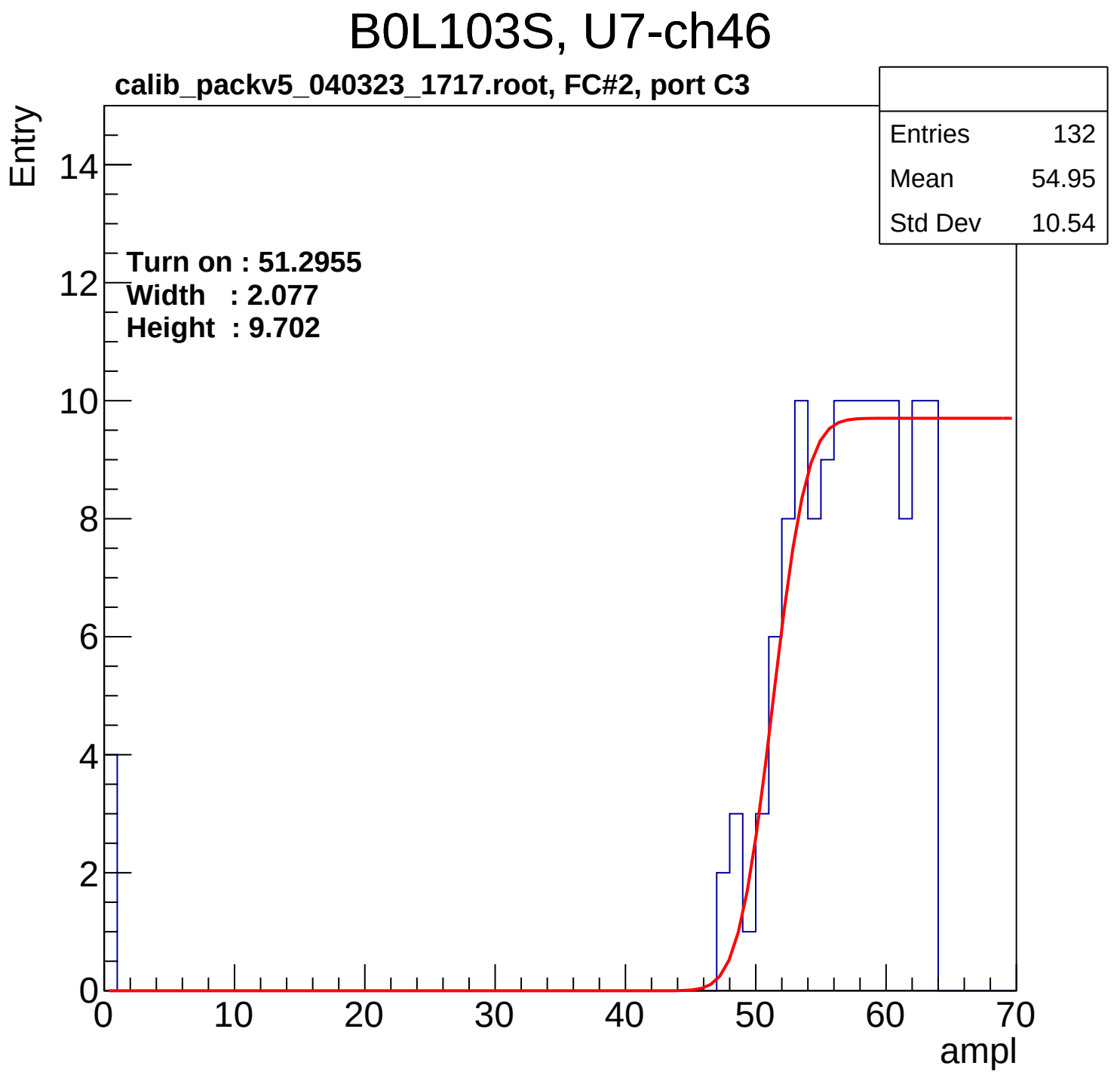
B0L103S, U7-ch46
calib_packv5_040323_1717.root, FC#2, port C3
Entries 132
Mean 54.95
Std Dev 10.54
Turn on : 51.2955
Width : 2.077
Height : 9.702
Entry
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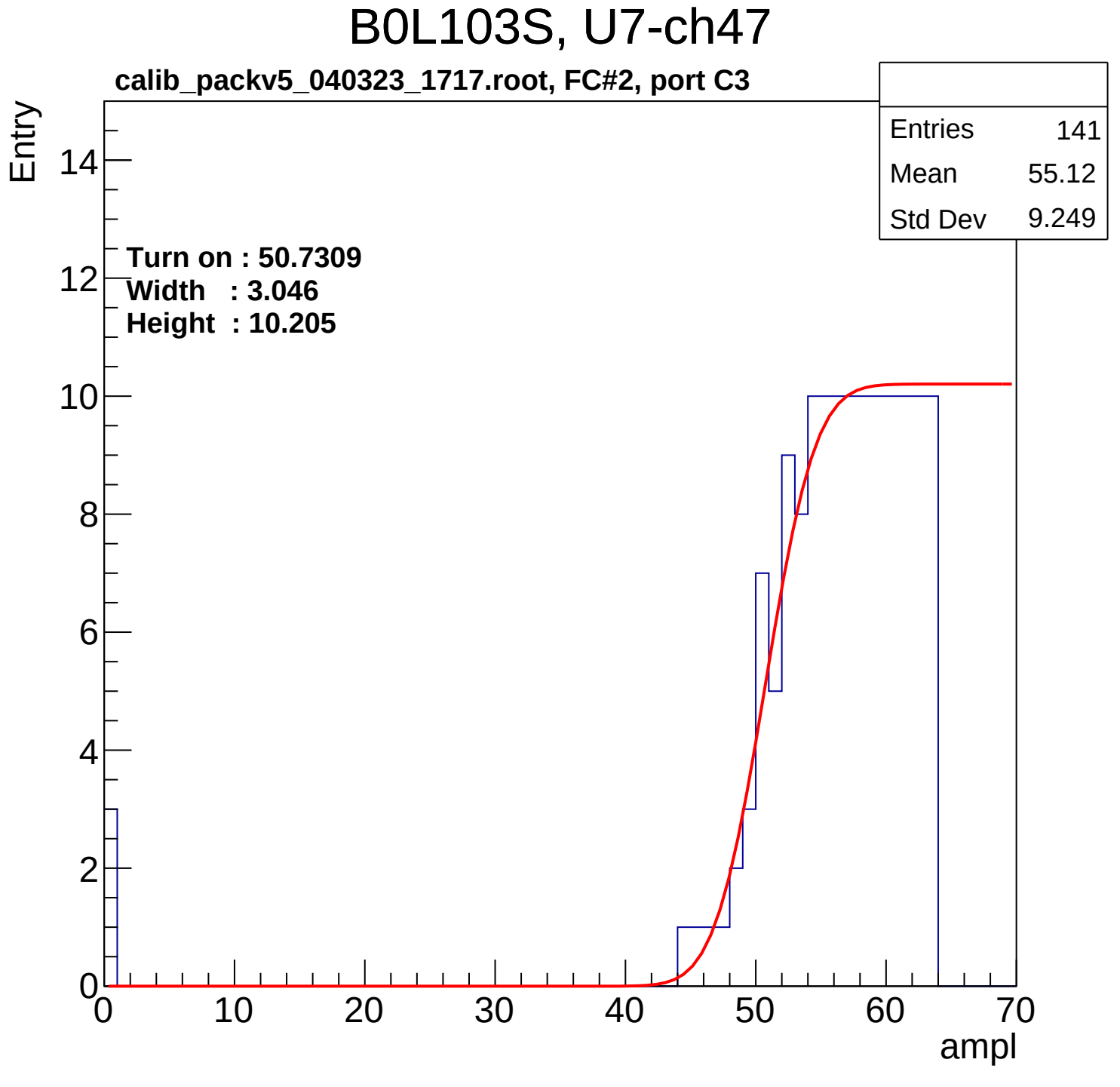
B0L103S, U7-ch47
calib_packv5_040323_1717.root, FC#2, port C3
Entries 141
Mean 55.12
Std Dev 9.249
Turn on : 50.7309
Width : 3.046
Height : 10.205
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ampl
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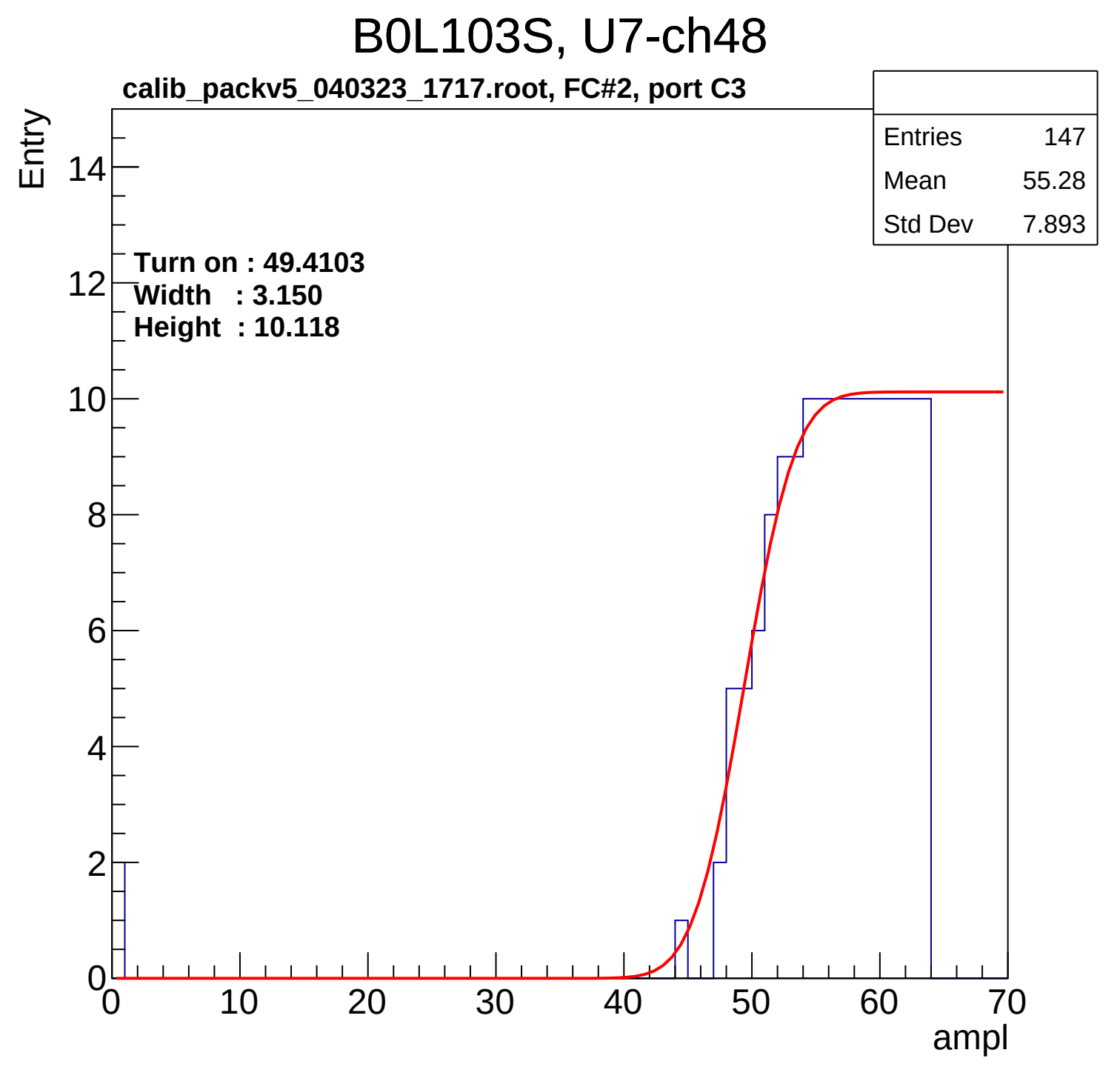
B0L103S, U7-ch48
calib_packv5_040323_1717.root, FC#2, port C3
Entries 147
Mean 55.28
Std Dev 7.893
Turn on : 49.4103
Width : 3.150
Height : 10.118
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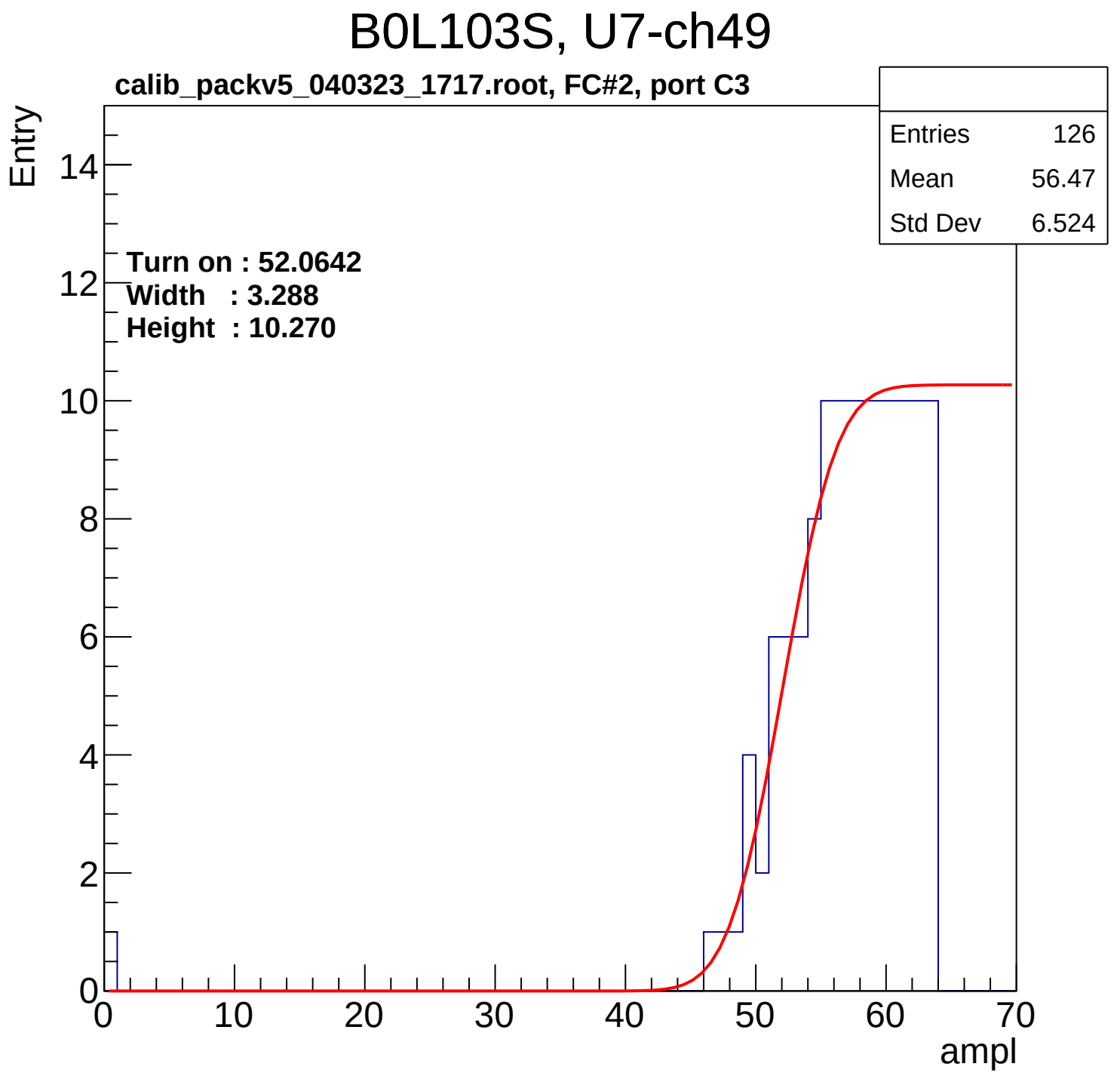
B0L103S, U7-ch49
calib_packv5_040323_1717.root, FC#2, port C3
Entries 126
Mean 56.47
Std Dev 6.524
Turn on : 52.0642
Width : 3.288
Height : 10.270
Entry
ampl
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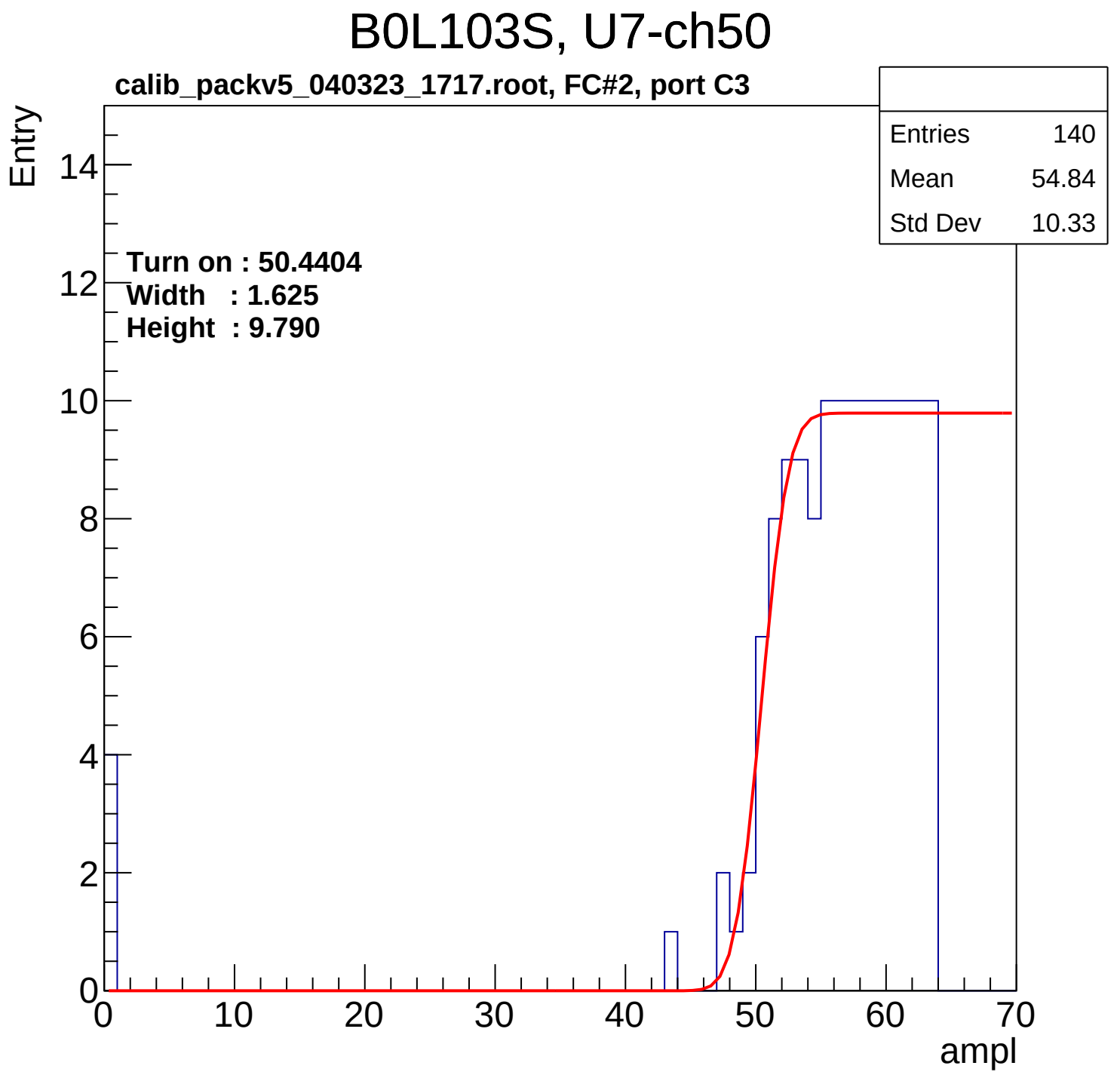
B0L103S, U7-ch50
calib_packv5_040323_1717.root, FC#2, port C3
Entries 140
Mean 54.84
Std Dev 10.33
Turn on : 50.4404
Width : 1.625
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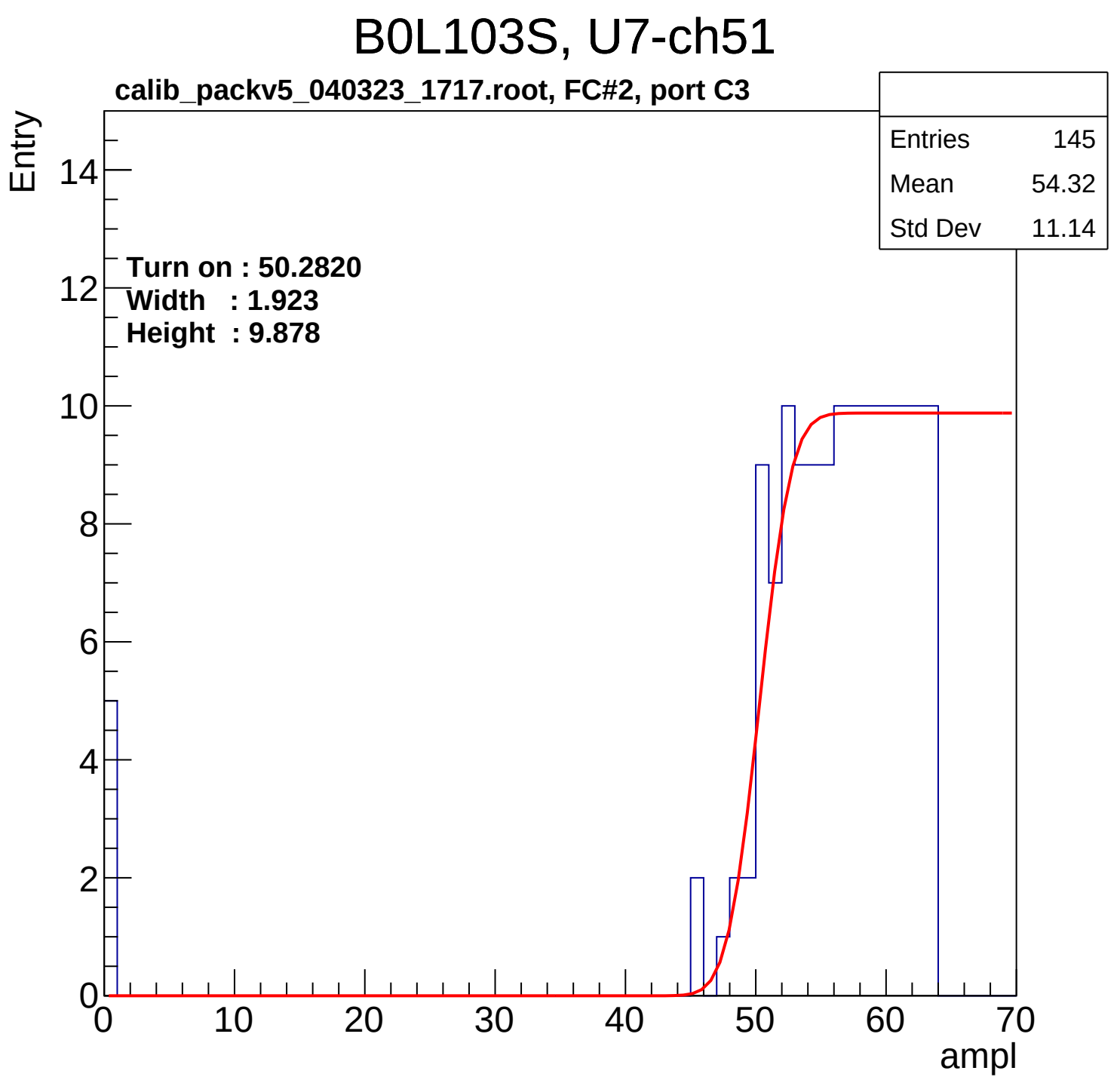
B0L103S, U7-ch51
calib_packv5_040323_1717.root, FC#2, port C3
Entries 145
Mean 54.32
Std Dev 11.14
Turn on : 50.2820
Width : 1.923
Height : 9.878
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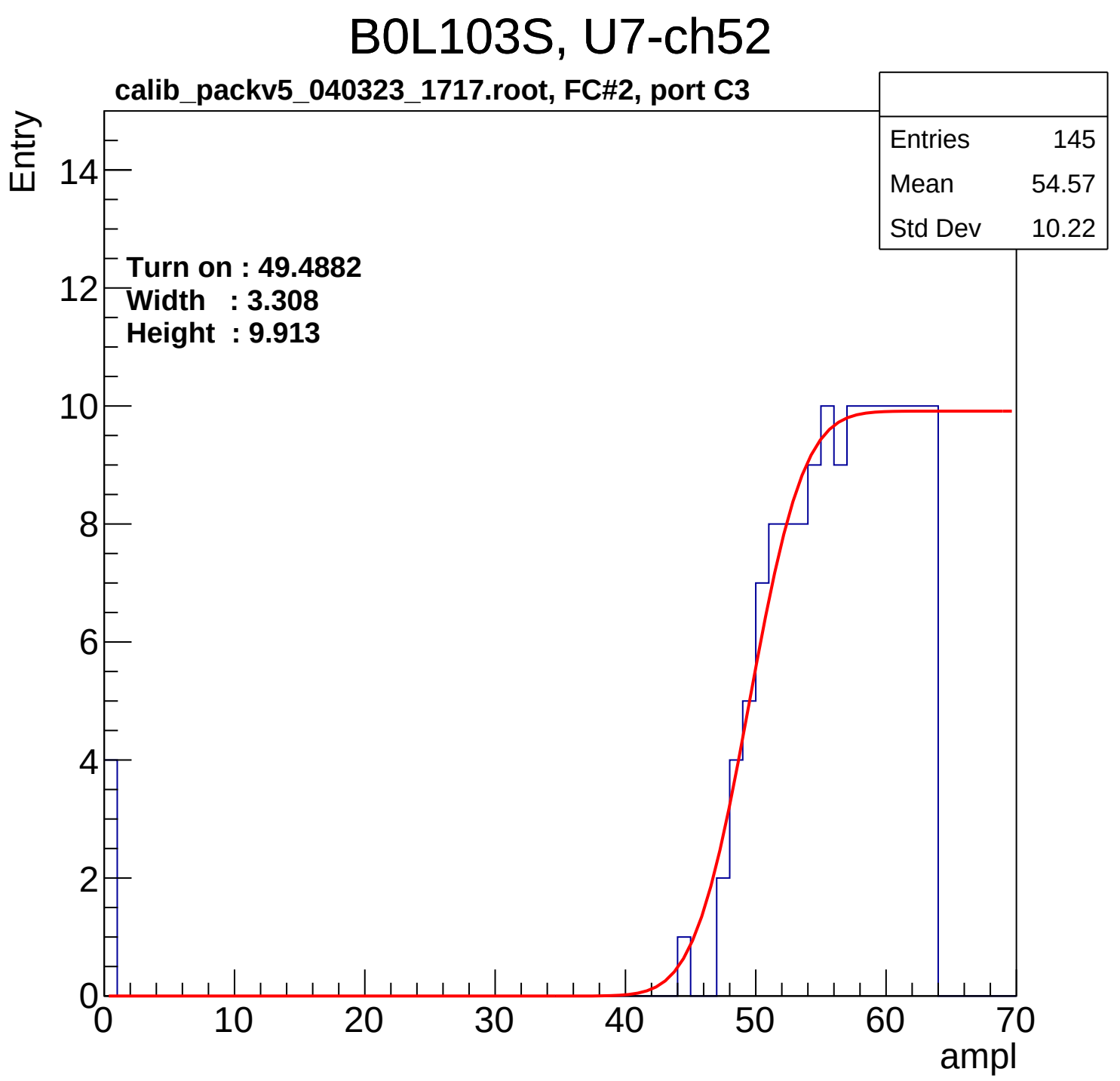
B0L103S, U7-ch52
calib_packv5_040323_1717.root, FC#2, port C3
Entries 145
Mean 54.57
Std Dev 10.22
Turn on : 49.4882
Width : 3.308
Height : 9.913
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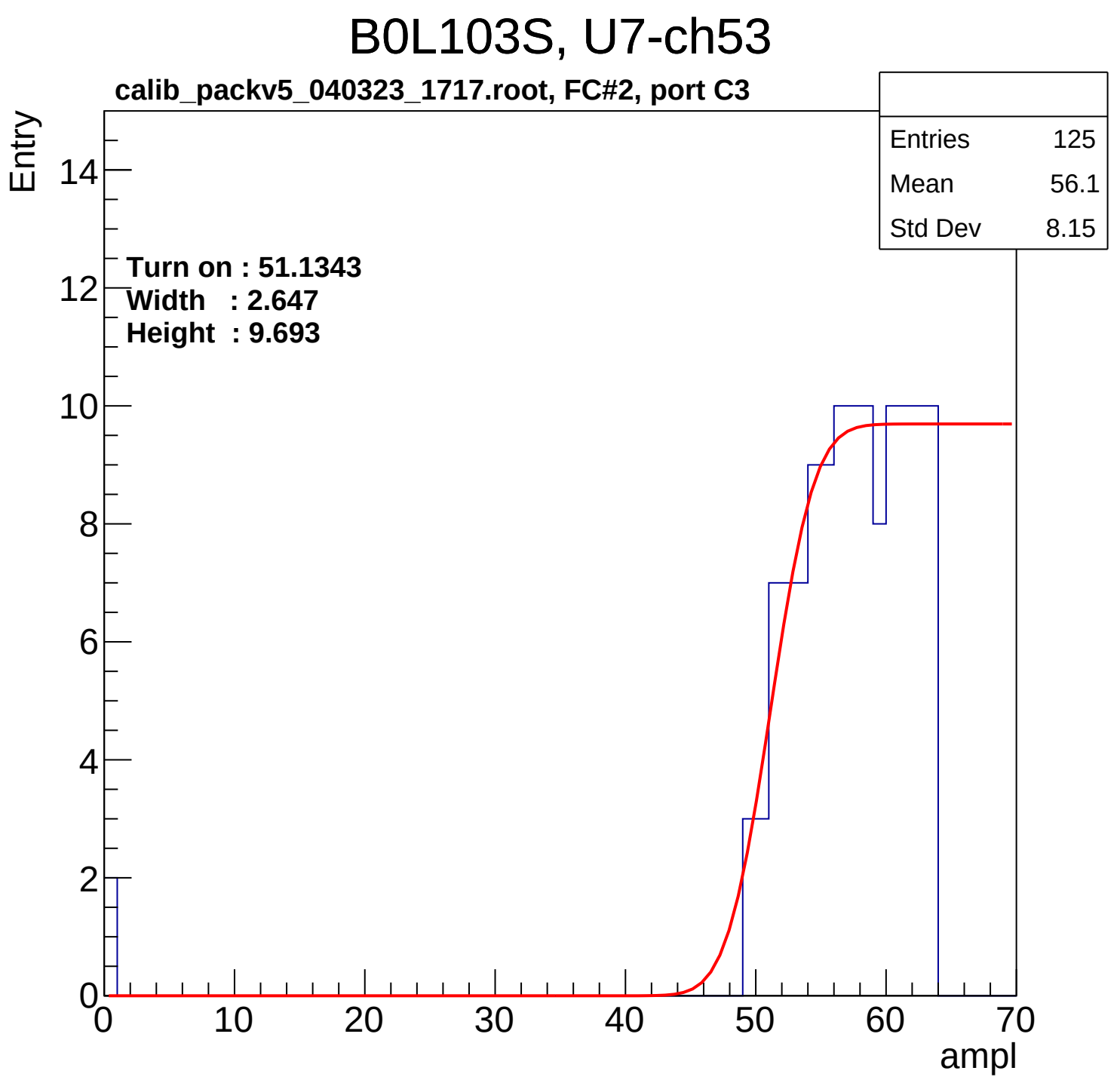
B0L103S, U7-ch53
calib_packv5_040323_1717.root, FC#2, port C3
Entries 125
Mean 56.1
Std Dev 8.15
Turn on : 51.1343
Width : 2.647
Height : 9.693
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ampl
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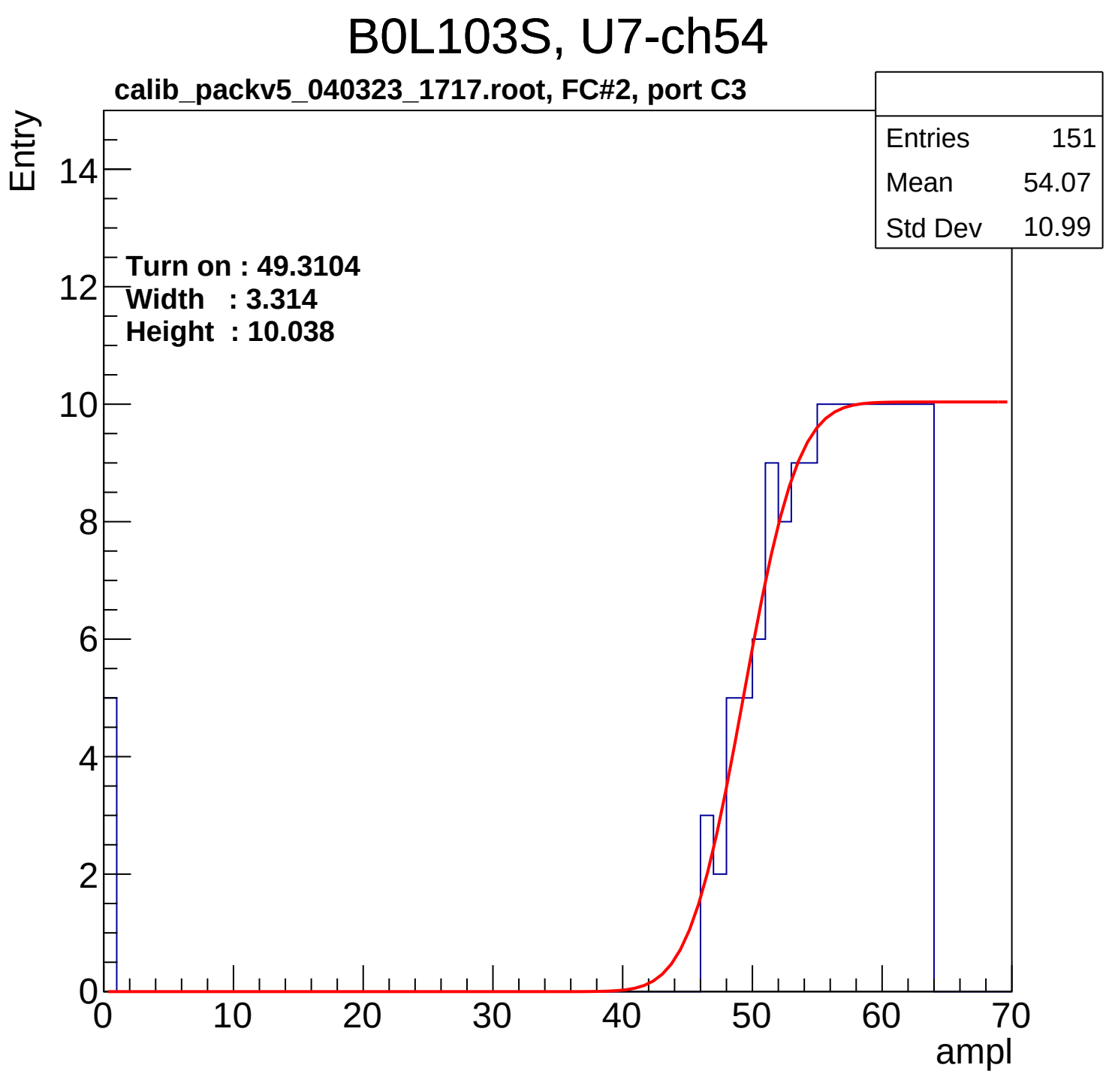
B0L103S, U7-ch54
calib_packv5_040323_1717.root, FC#2, port C3
Entries 151
Mean 54.07
Std Dev 10.99
Turn on : 49.3104
Width : 3.314
Height : 10.038
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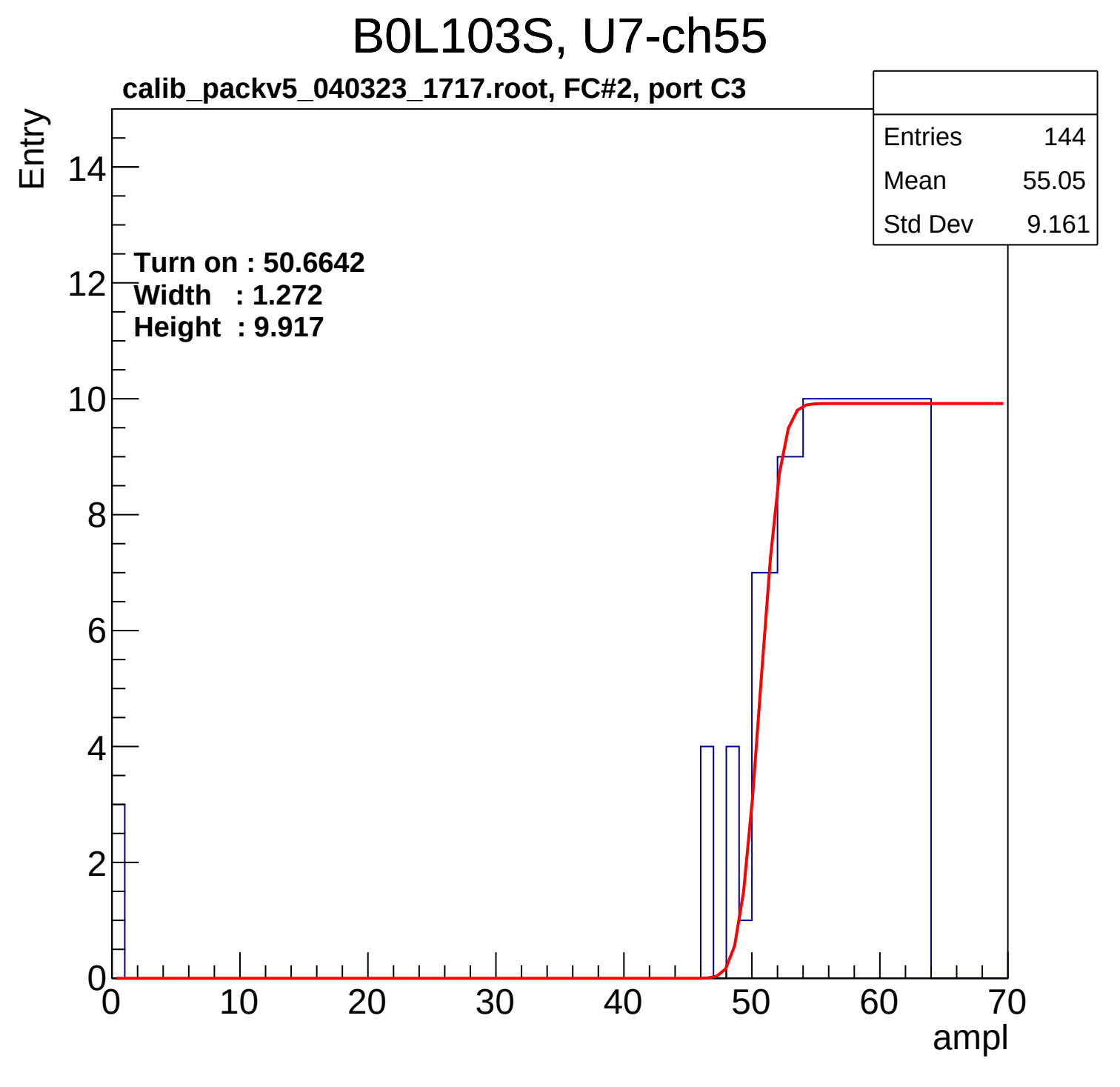
B0L103S, U7-ch55
calib_packv5_040323_1717.root, FC#2, port C3
Entries 144
Mean 55.05
Std Dev 9.161
Turn on : 50.6642
Width : 1.272
Height : 9.917
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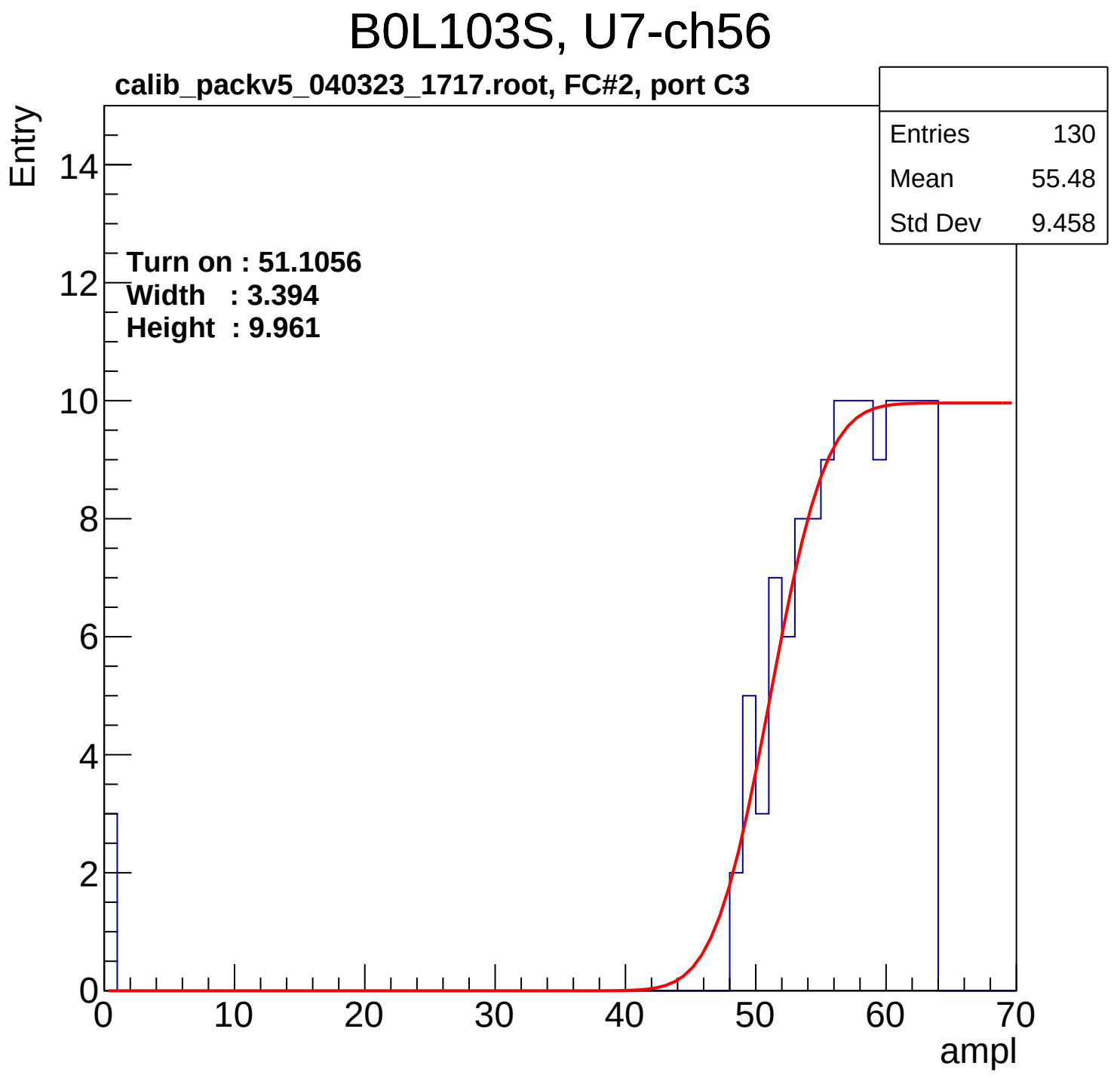
B0L103S, U7-ch56
calib_packv5_040323_1717.root, FC#2, port C3
Entries 130
Mean 55.48
Std Dev 9.458
Turn on : 51.1056
Width : 3.394
Height : 9.961
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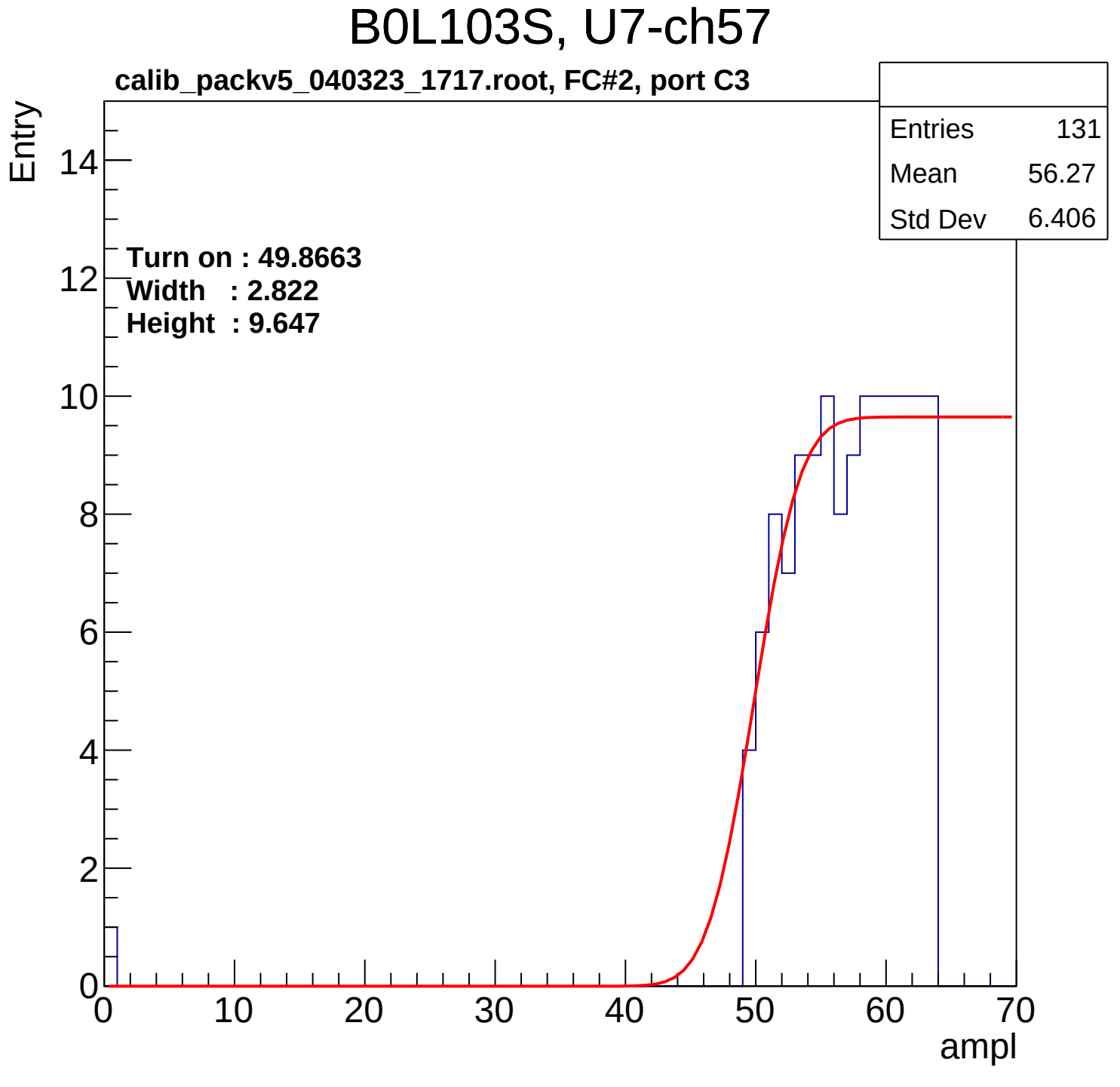
B0L103S, U7-ch57
calib_packv5_040323_1717.root, FC#2, port C3
Entries 131
Mean 56.27
Std Dev 6.406
Turn on : 49.8663
Width : 2.822
Height : 9.647
Entry
ampl
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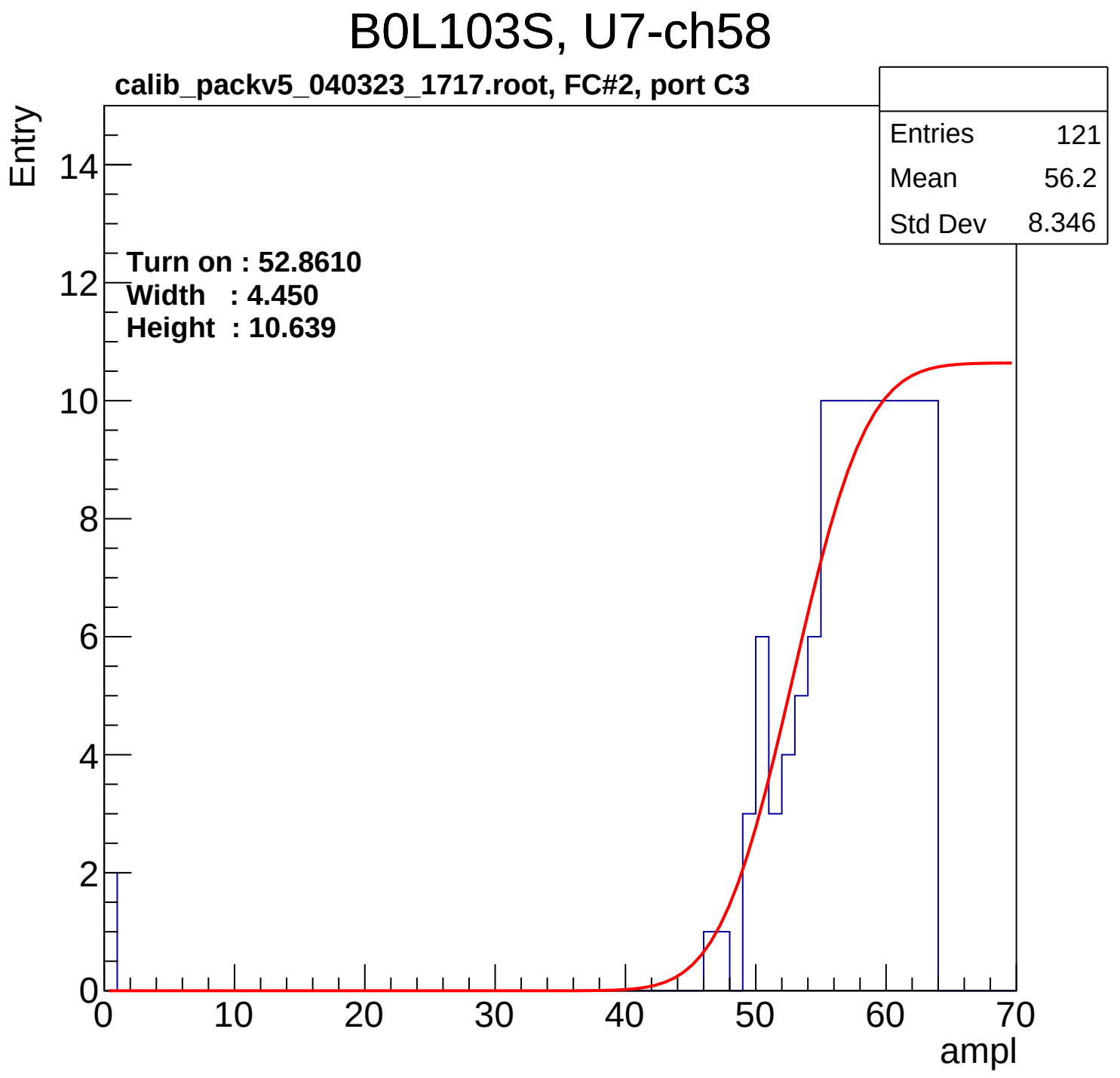
B0L103S, U7-ch58
calib_packv5_040323_1717.root, FC#2, port C3
Entries 121
Mean 56.2
Std Dev 8.346
Turn on : 52.8610
Width : 4.450
Height : 10.639
Entry
ampl
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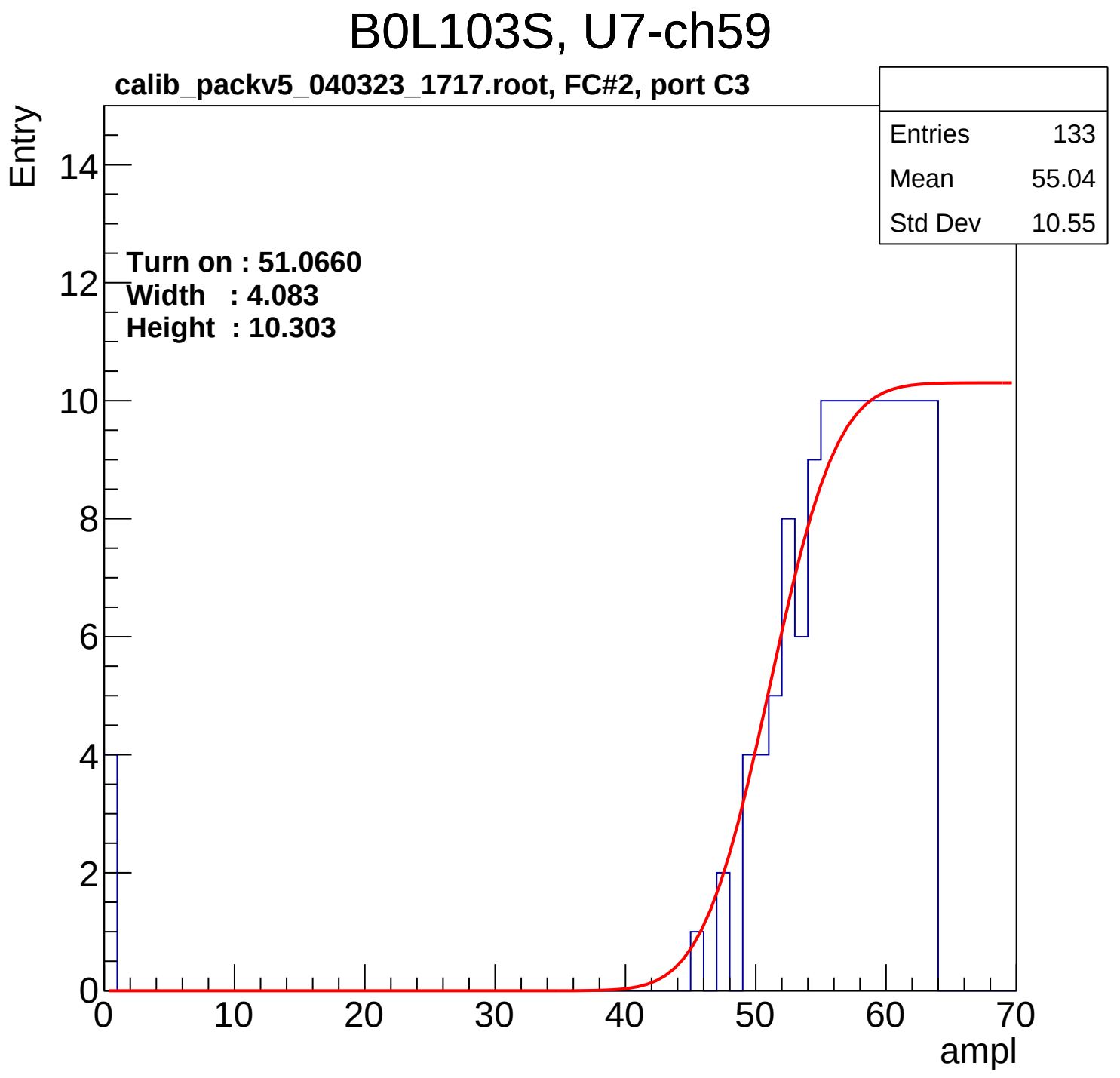
B0L103S, U7-ch59
calib_packv5_040323_1717.root, FC#2, port C3
Entries 133
Mean 55.04
Std Dev 10.55
Turn on : 51.0660
Width : 4.083
Height : 10.303
Entry
ampl
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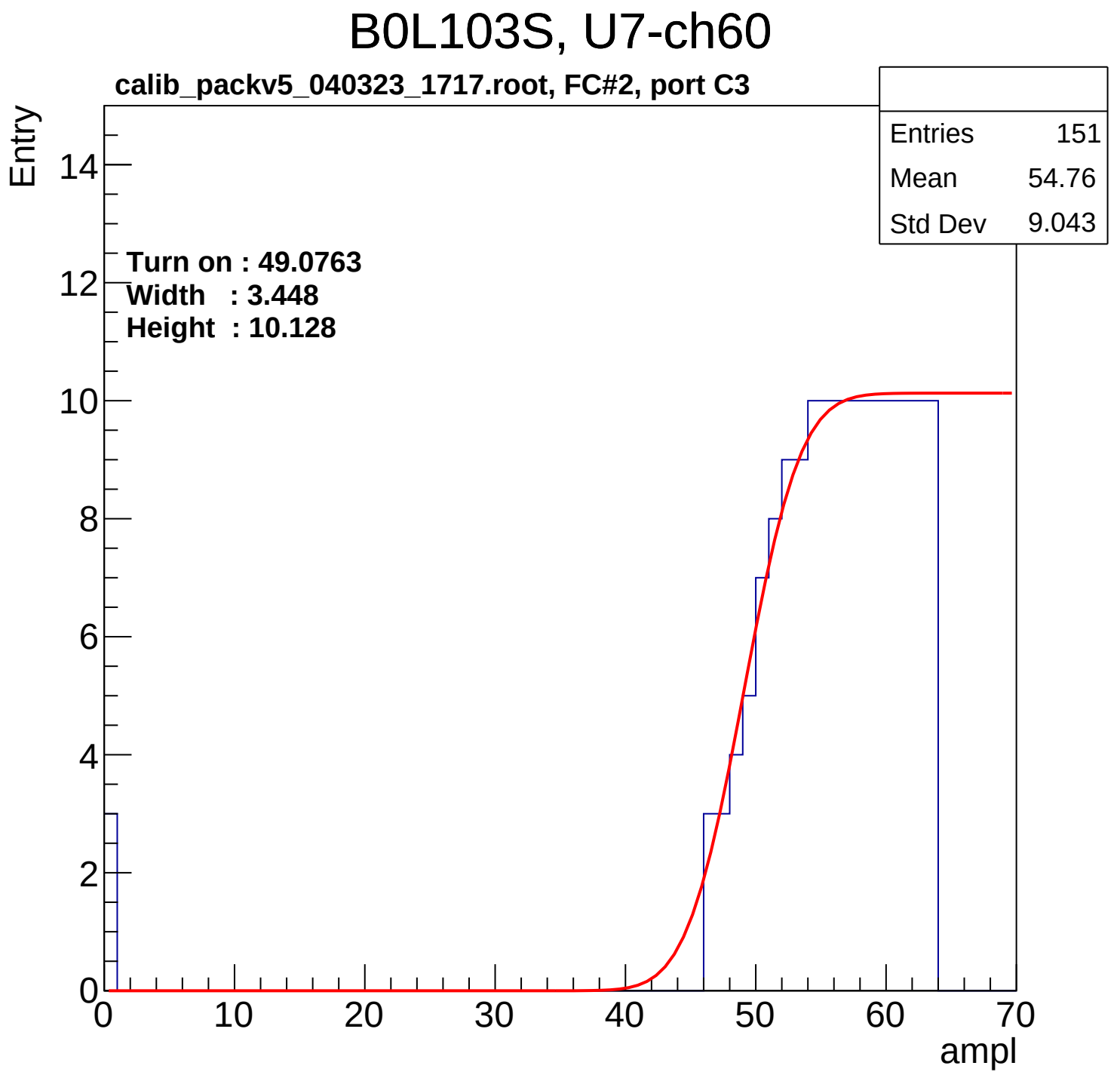
B0L103S, U7-ch60
calib_packv5_040323_1717.root, FC#2, port C3
Entries 151
Mean 54.76
Std Dev 9.043
Turn on : 49.0763
Width : 3.448
Height : 10.128
Entry
ampl
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2
4
6
8
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12
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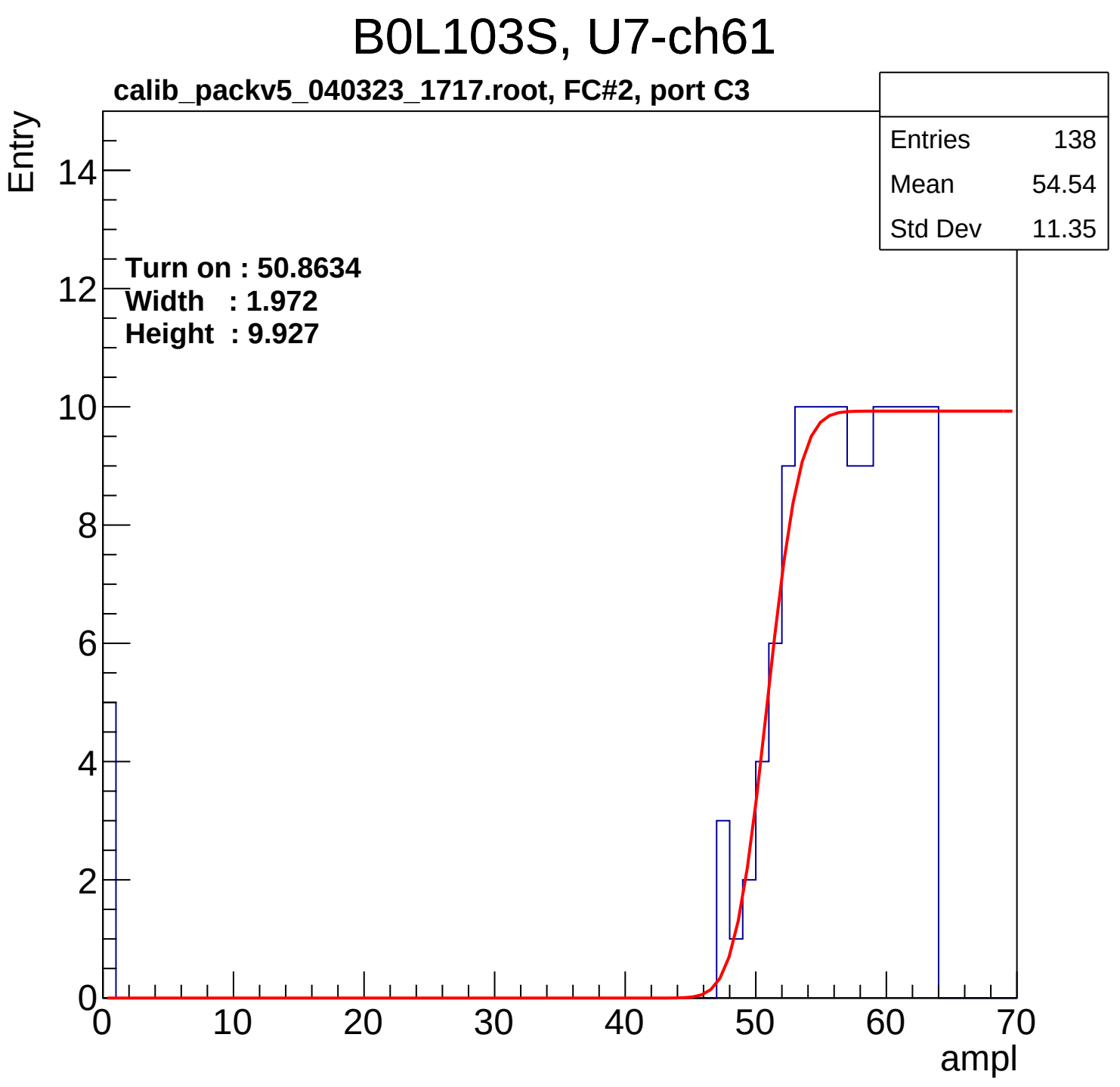
B0L103S, U7-ch61
calib_packv5_040323_1717.root, FC#2, port C3
Entries 138
Mean 54.54
Std Dev 11.35
Turn on : 50.8634
Width : 1.972
Height : 9.927
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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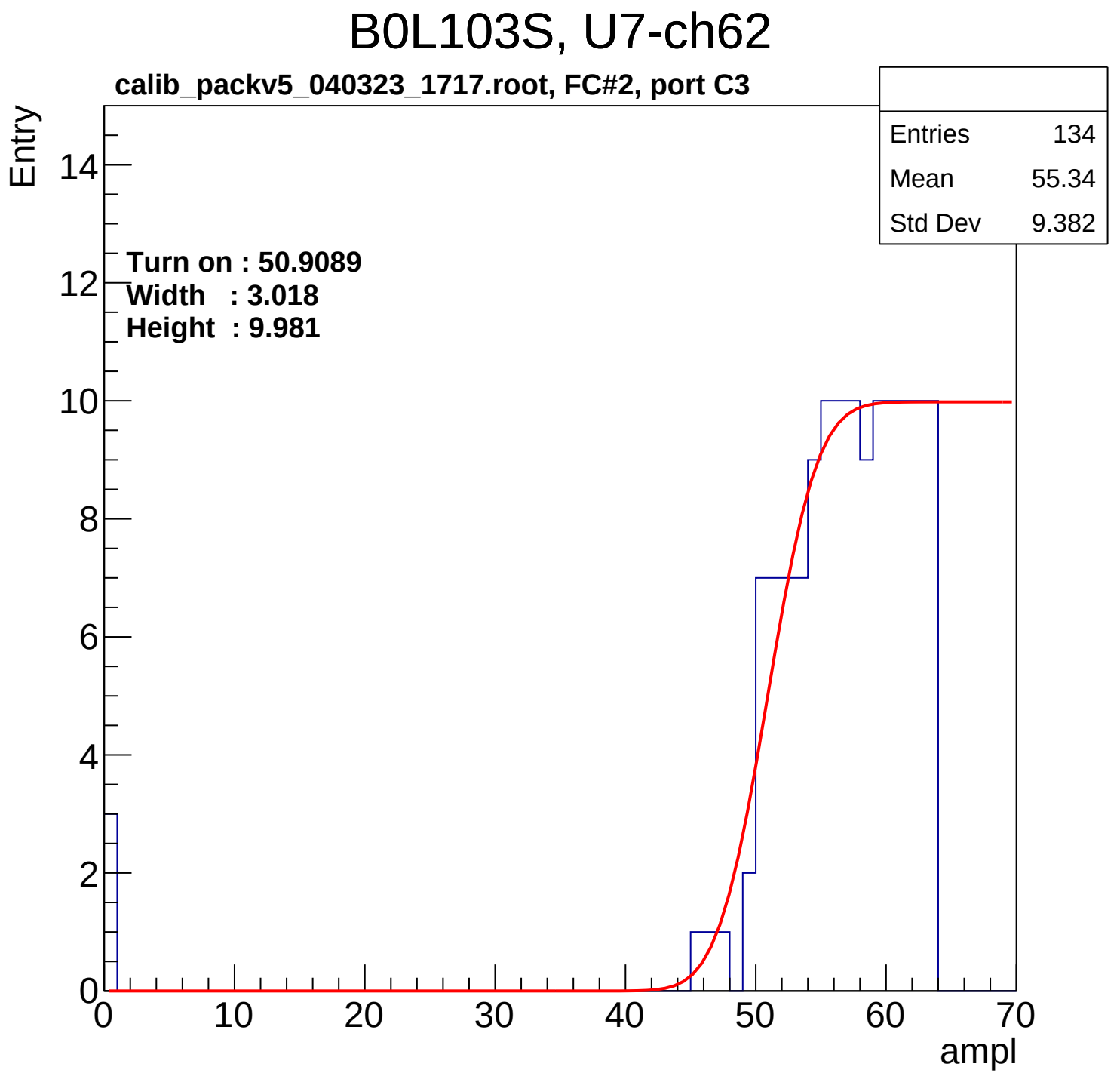
B0L103S, U7-ch62
calib_packv5_040323_1717.root, FC#2, port C3
Entries 134
Mean 55.34
Std Dev 9.382
Turn on : 50.9089
Width : 3.018
Height : 9.981
Entry
ampl
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4
6
8
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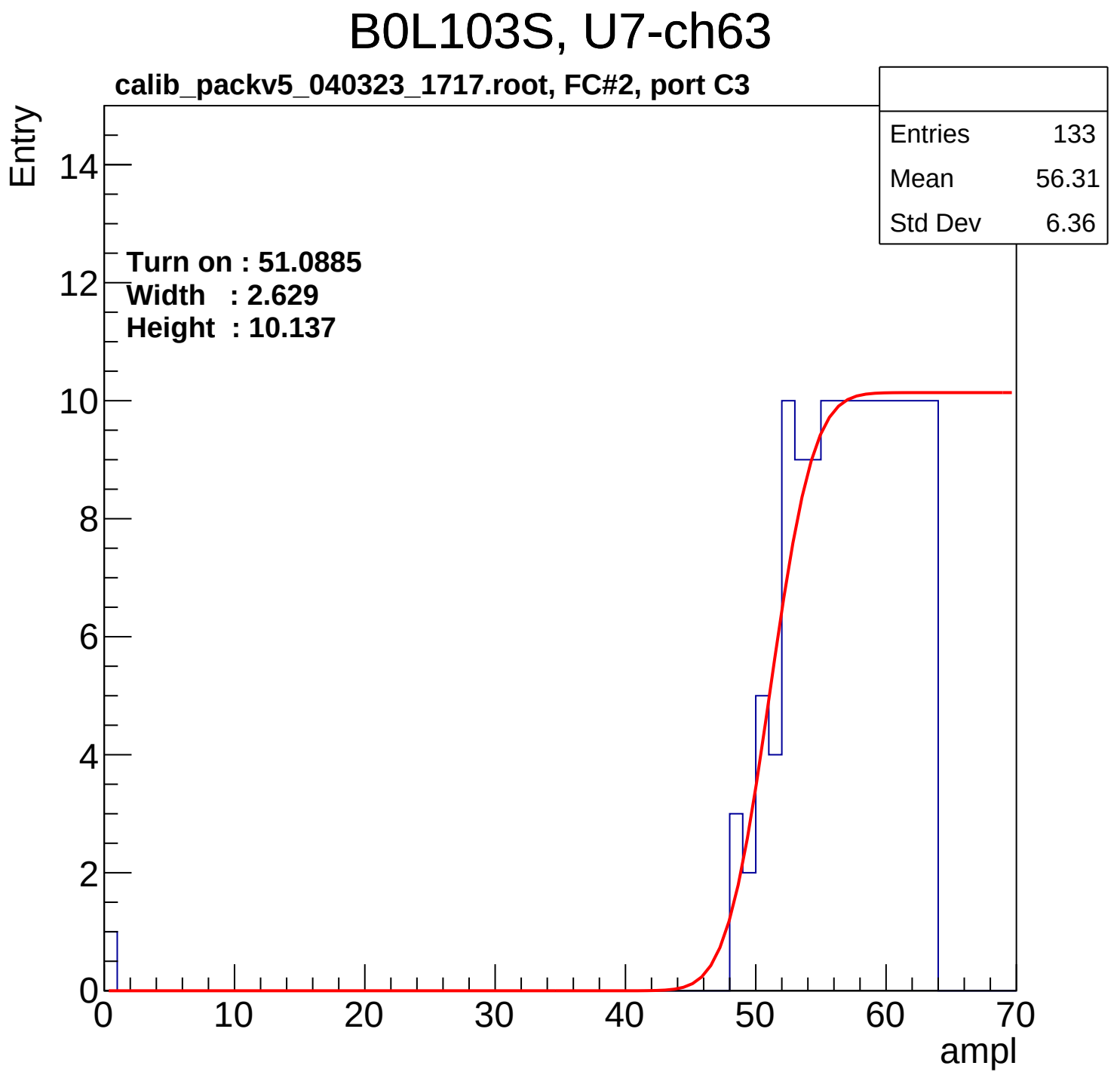
B0L103S, U7-ch63
calib_packv5_040323_1717.root, FC#2, port C3
Entries 133
Mean 56.31
Std Dev 6.36
Turn on : 51.0885
Width : 2.629
Height : 10.137
Entry
ampl
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2
4
6
8
10
12
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0
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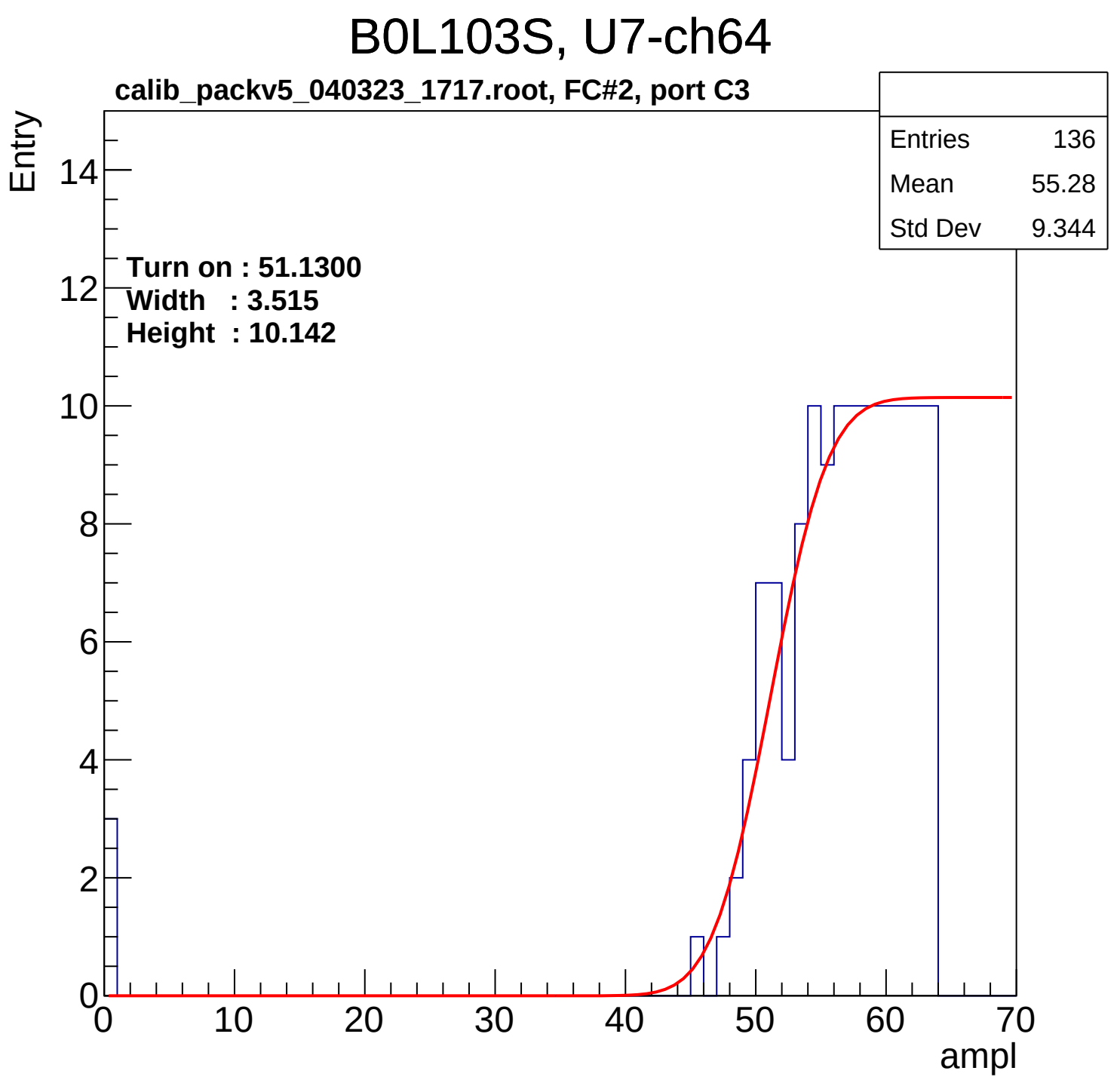
B0L103S, U7-ch64
calib_packv5_040323_1717.root, FC#2, port C3
Entries 136
Mean 55.28
Std Dev 9.344
Turn on : 51.1300
Width : 3.515
Height : 10.142
Entry
ampl
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4
6
8
10
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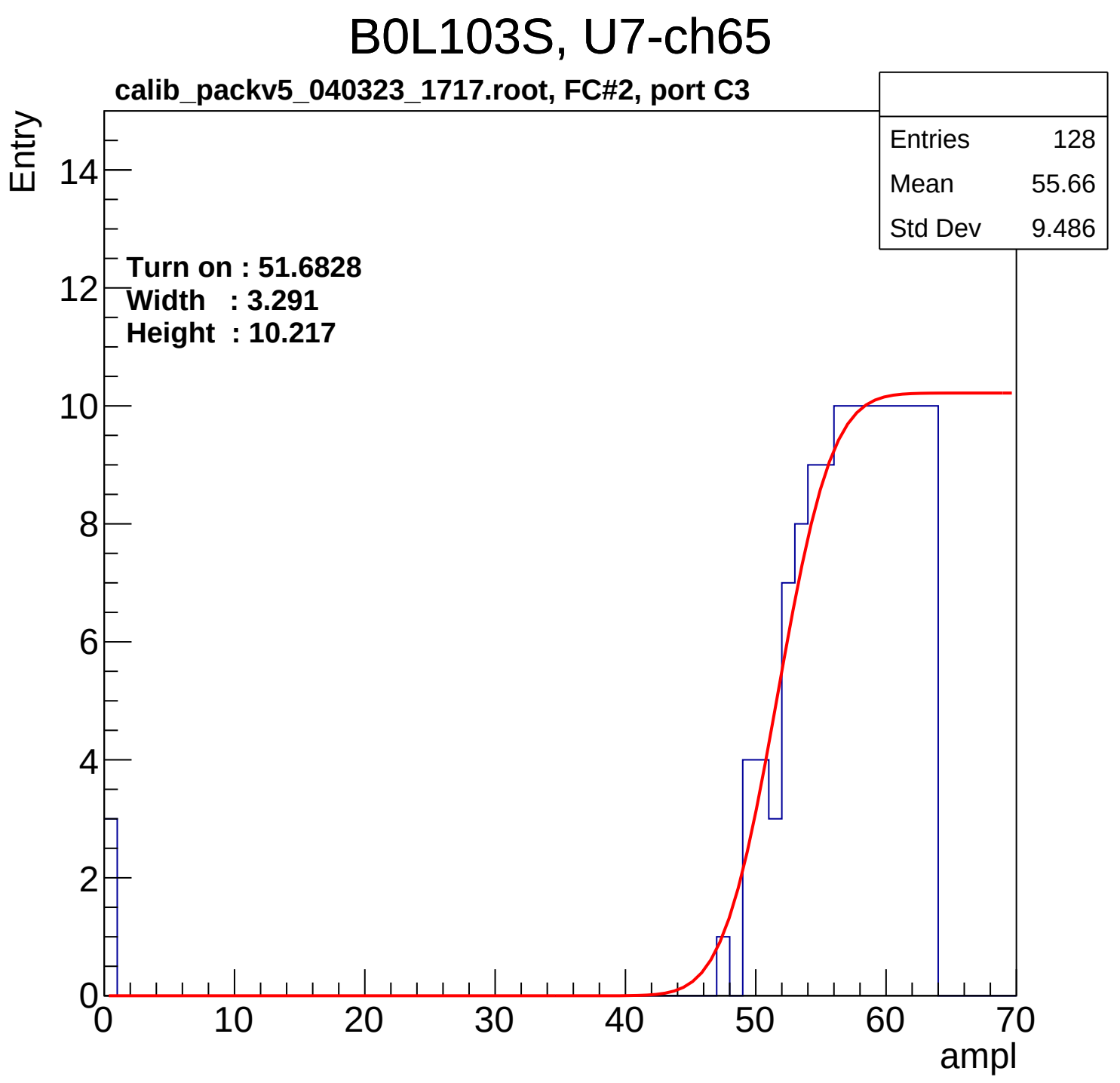
B0L103S, U7-ch65
calib_packv5_040323_1717.root, FC#2, port C3
Entries 128
Mean 55.66
Std Dev 9.486
Turn on : 51.6828
Width : 3.291
Height : 10.217
Entry
ampl
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2
4
6
8
10
12
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20
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60
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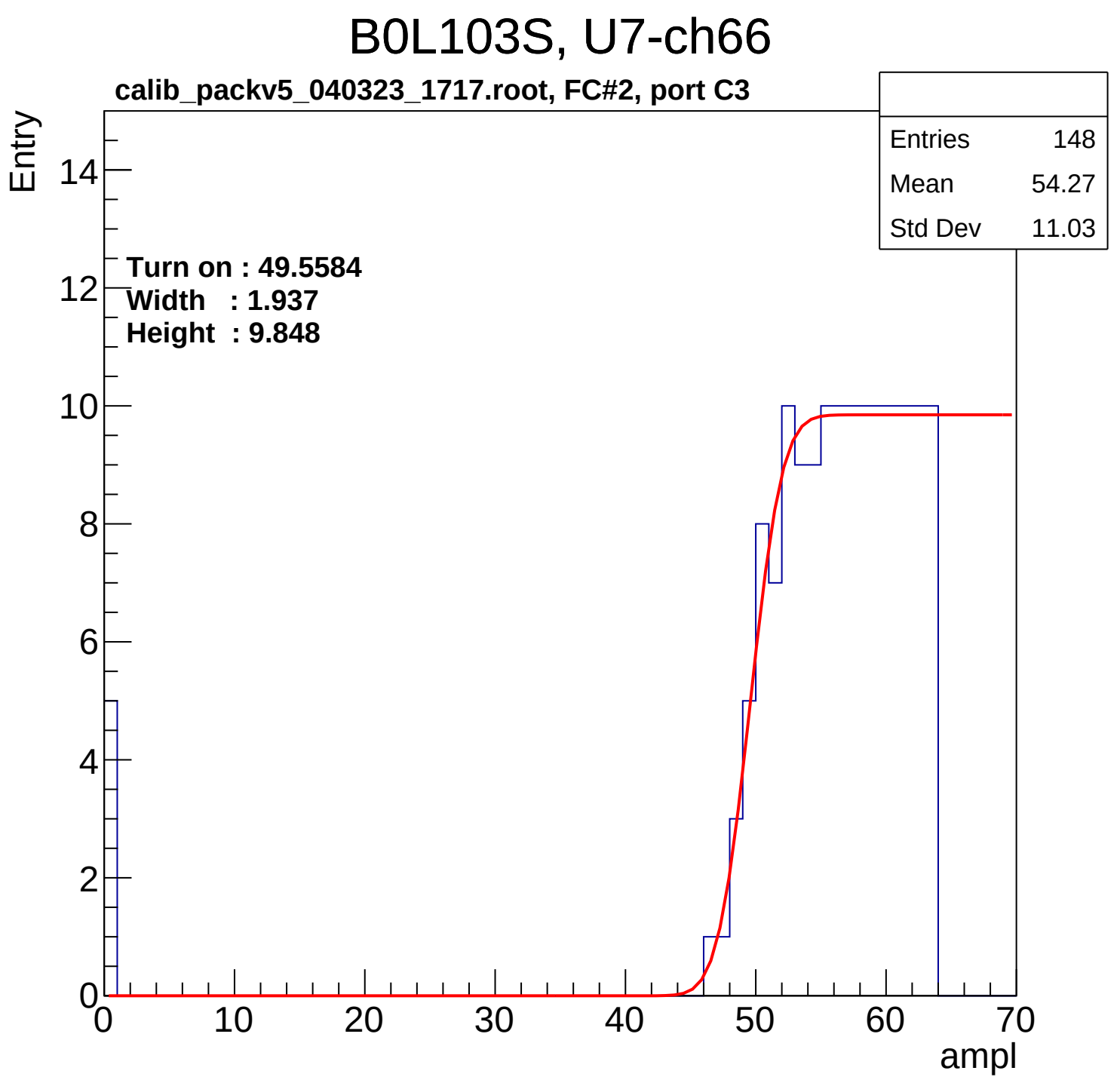
B0L103S, U7-ch66
calib_packv5_040323_1717.root, FC#2, port C3
Entries 148
Mean 54.27
Std Dev 11.03
Turn on : 49.5584
Width : 1.937
Height : 9.848
Entry
ampl
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6
8
10
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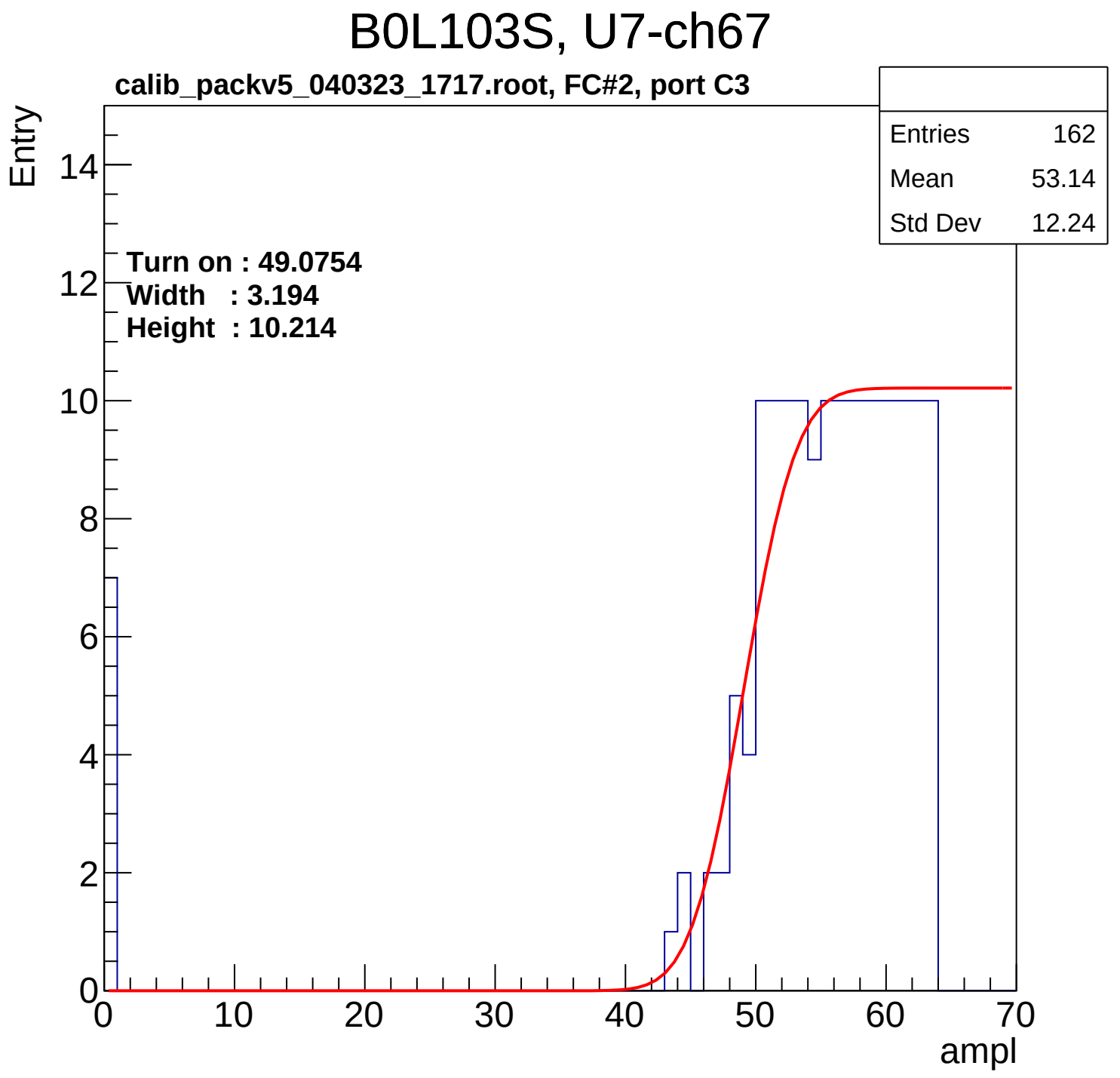
B0L103S, U7-ch67
calib_packv5_040323_1717.root, FC#2, port C3
Entries 162
Mean 53.14
Std Dev 12.24
Turn on : 49.0754
Width : 3.194
Height : 10.214
Entry
ampl
0
2
4
6
8
10
12
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0
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20
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40
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60
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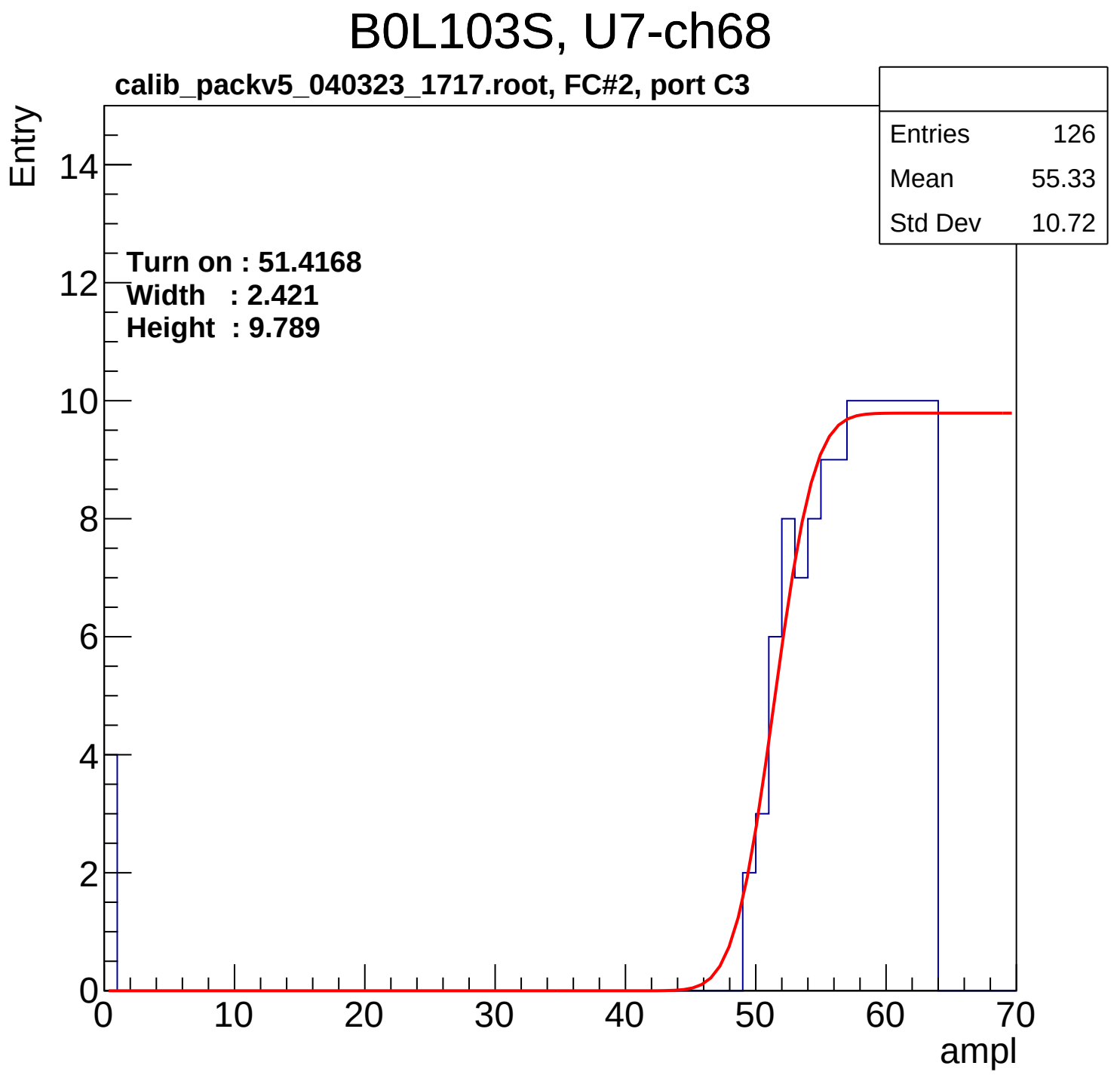
B0L103S, U7-ch68
calib_packv5_040323_1717.root, FC#2, port C3
Entries 126
Mean 55.33
Std Dev 10.72
Turn on : 51.4168
Width : 2.421
Height : 9.789
Entry
ampl
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6
8
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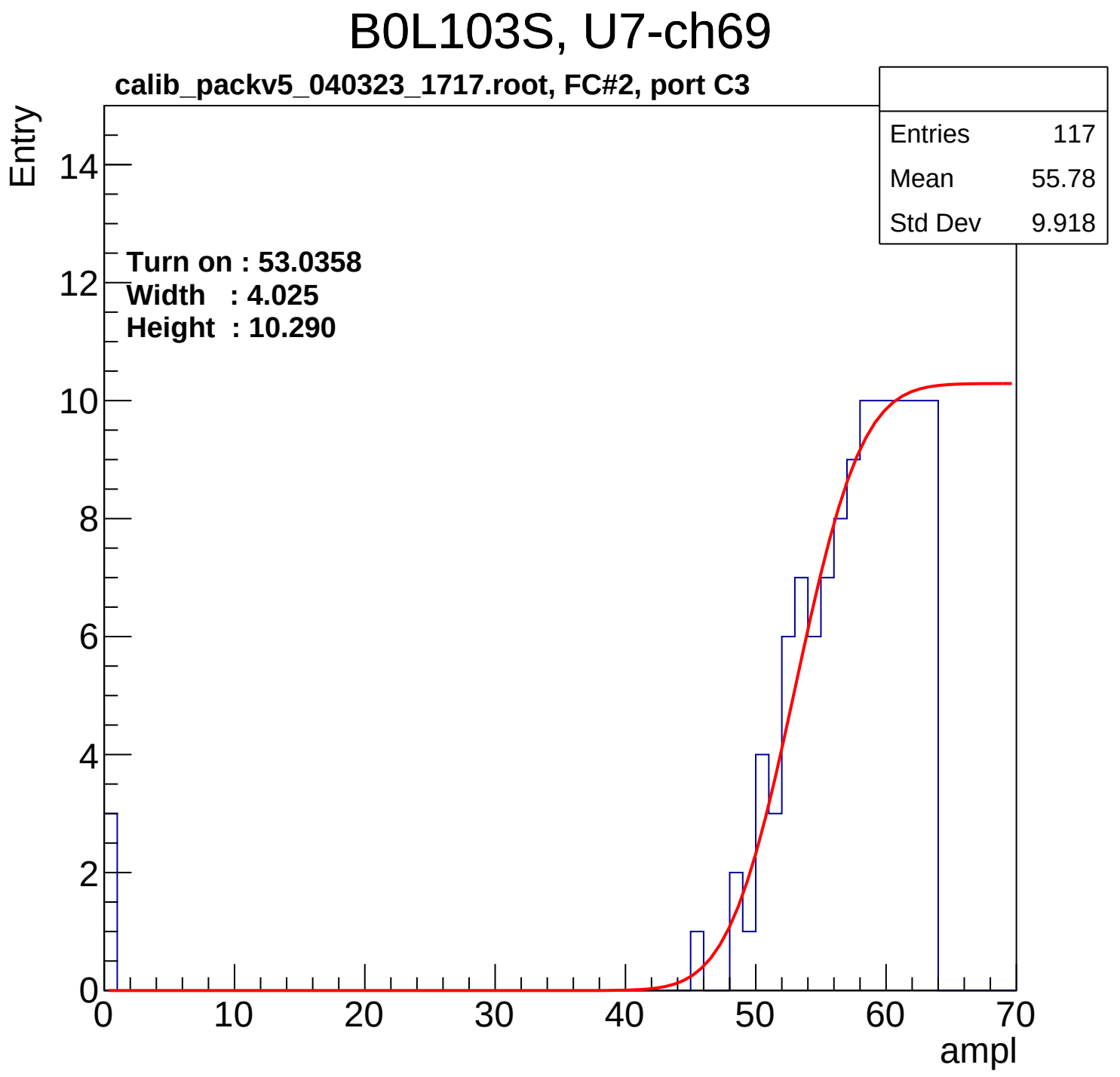
B0L103S, U7-ch69
calib_packv5_040323_1717.root, FC#2, port C3
Entries 117
Mean 55.78
Std Dev 9.918
Turn on : 53.0358
Width : 4.025
Height : 10.290
Entry
ampl
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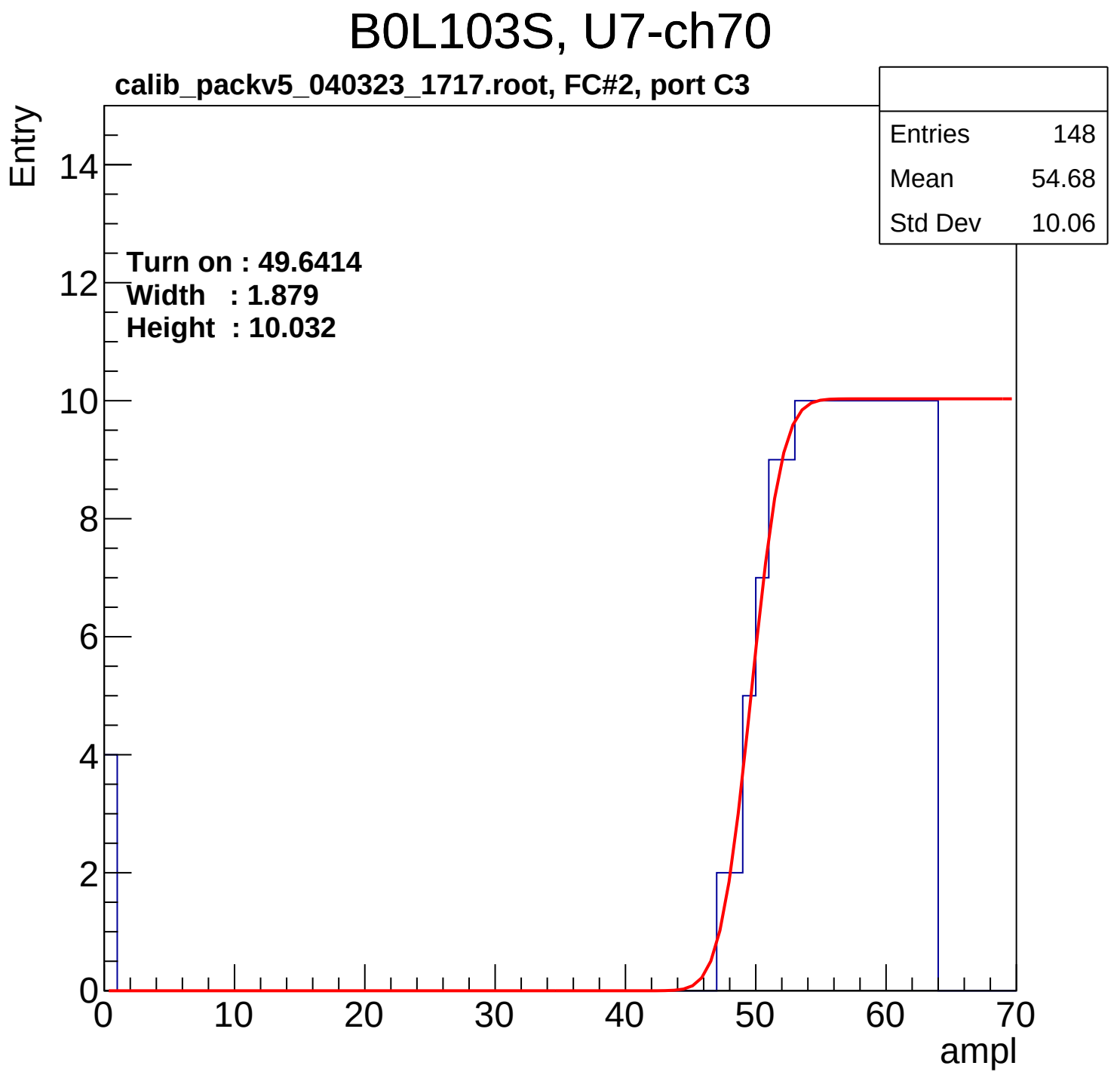
B0L103S, U7-ch70
calib_packv5_040323_1717.root, FC#2, port C3
Entries 148
Mean 54.68
Std Dev 10.06
Turn on : 49.6414
Width : 1.879
Height : 10.032
Entry
ampl
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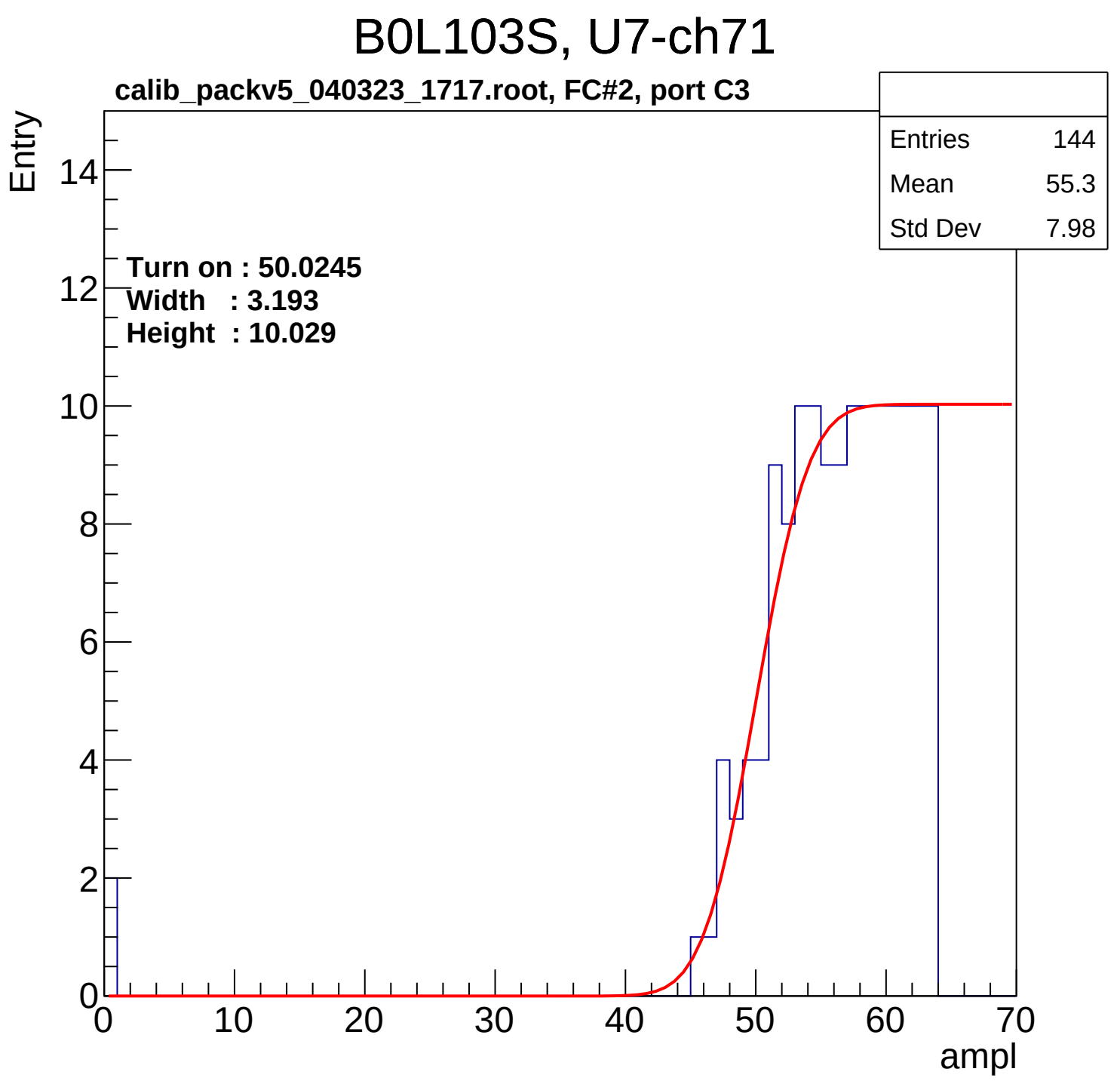
B0L103S, U7-ch71
calib_packv5_040323_1717.root, FC#2, port C3
Entries 144
Mean 55.3
Std Dev 7.98
Turn on : 50.0245
Width : 3.193
Height : 10.029
Entry
ampl
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6
8
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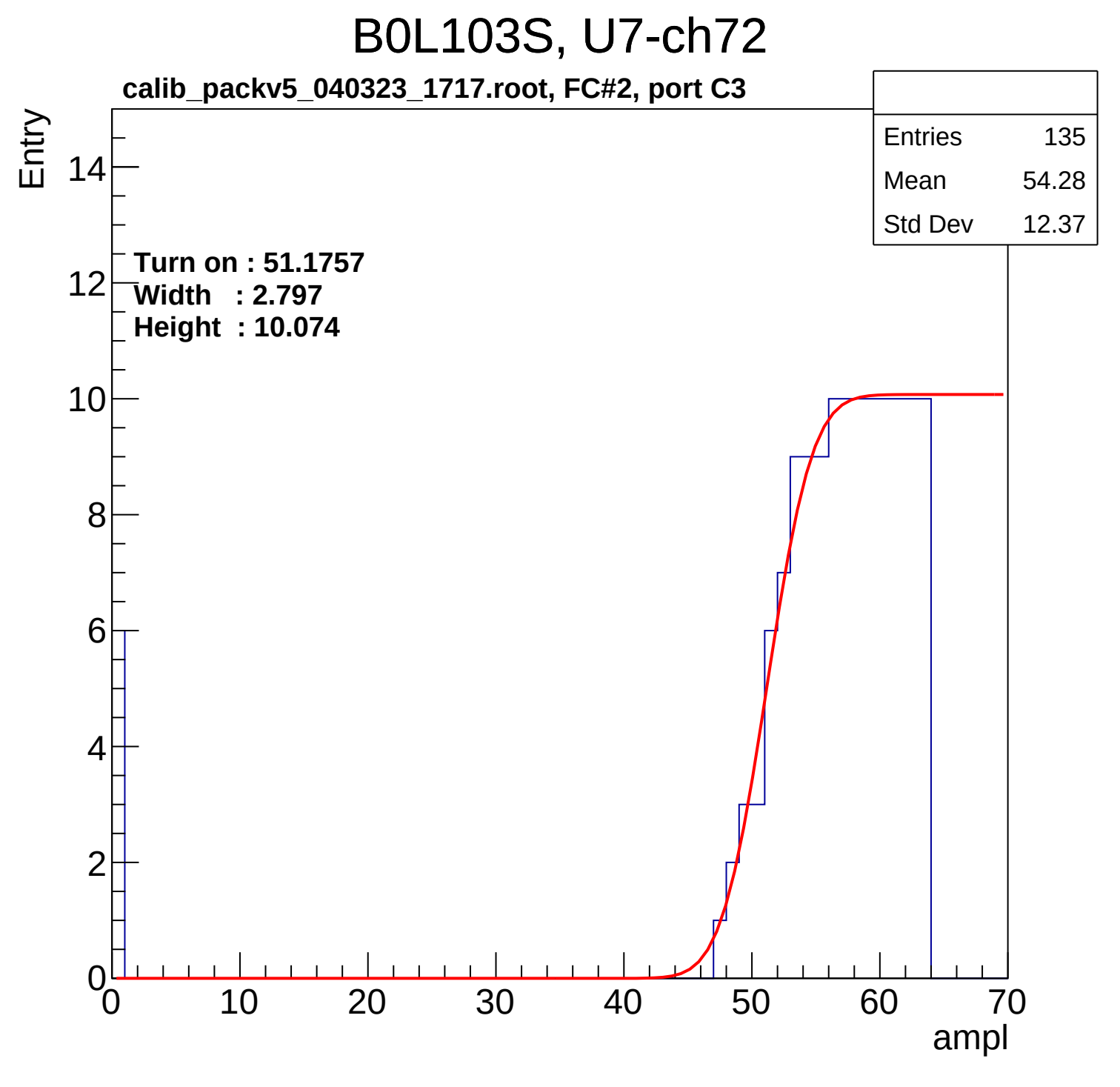
B0L103S, U7-ch72
calib_packv5_040323_1717.root, FC#2, port C3
Entries 135
Mean 54.28
Std Dev 12.37
Turn on : 51.1757
Width : 2.797
Height : 10.074
Entry
ampl
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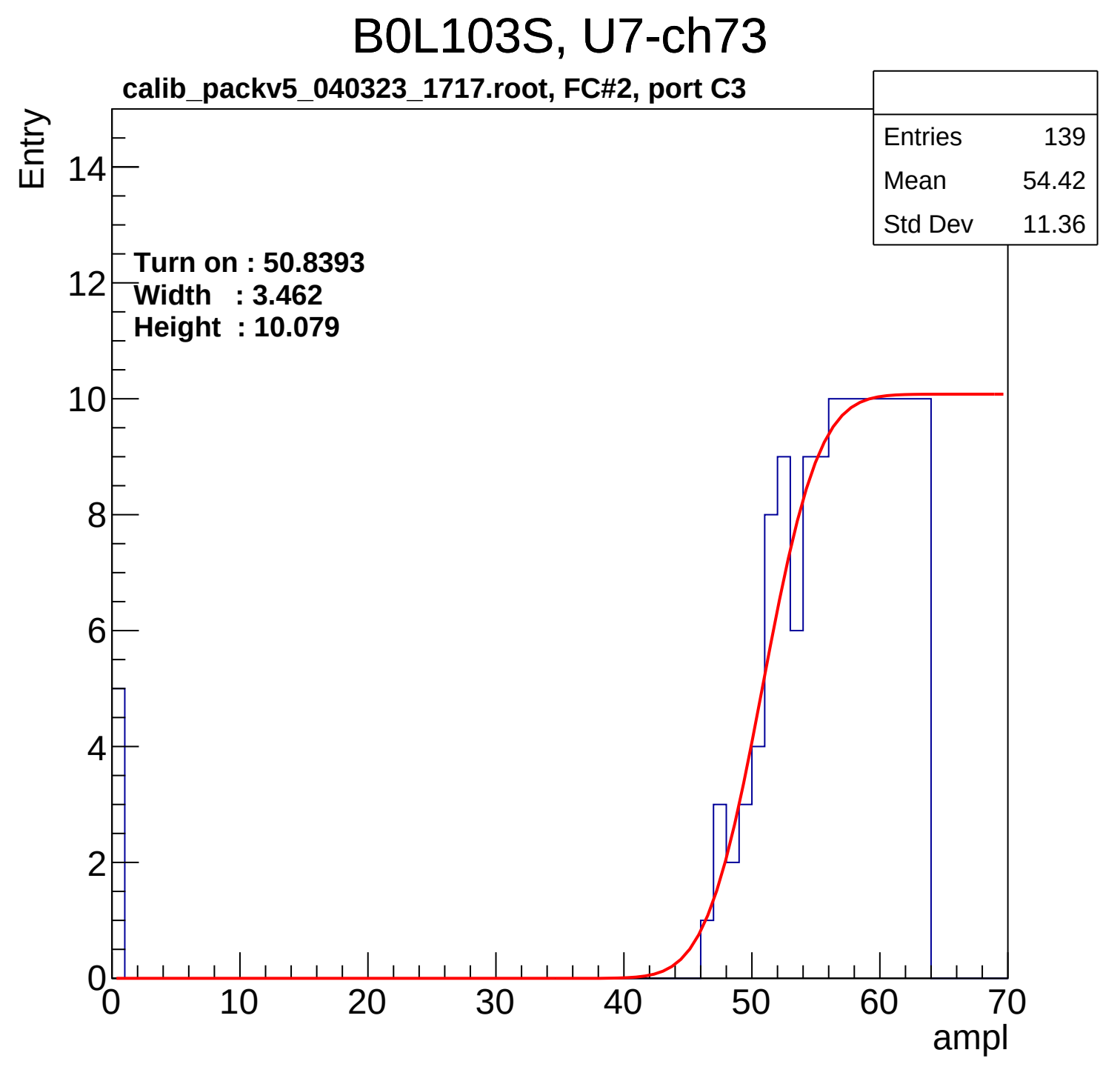
B0L103S, U7-ch73
calib_packv5_040323_1717.root, FC#2, port C3
Entries 139
Mean 54.42
Std Dev 11.36
Turn on : 50.8393
Width : 3.462
Height : 10.079
Entry
ampl
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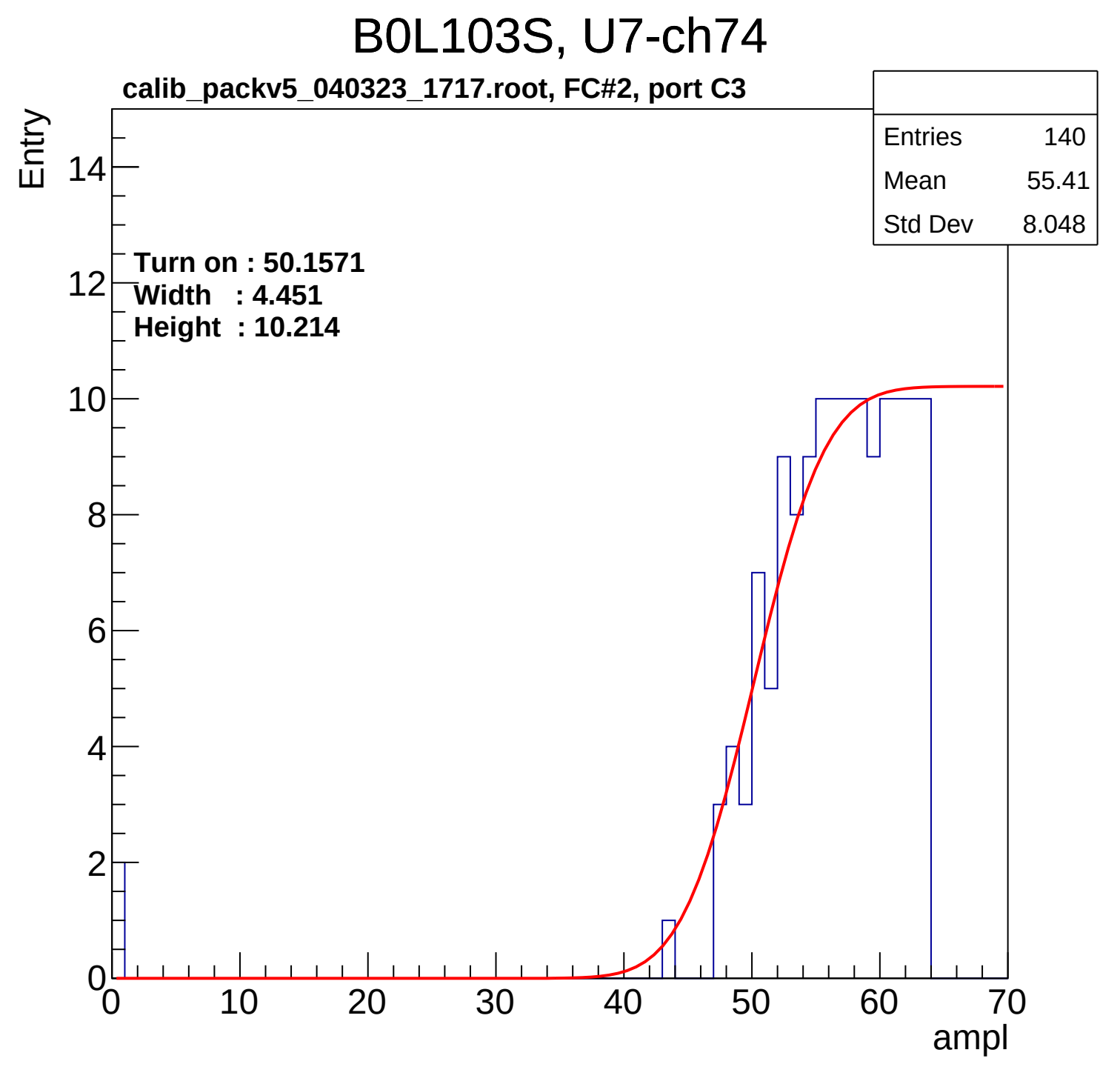
B0L103S, U7-ch74
calib_packv5_040323_1717.root, FC#2, port C3
Entries 140
Mean 55.41
Std Dev 8.048
Turn on : 50.1571
Width : 4.451
Height : 10.214
Entry
ampl
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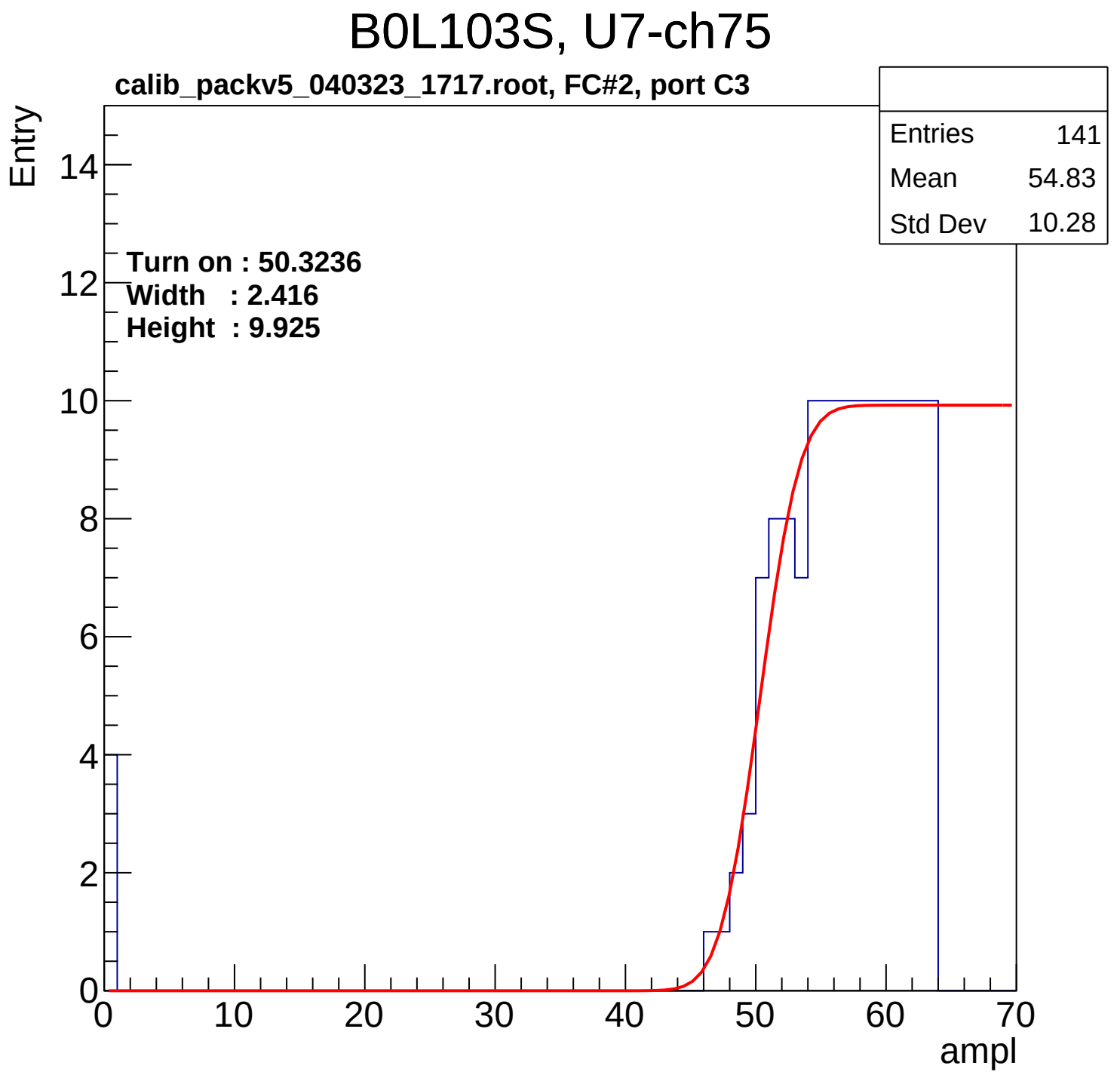
B0L103S, U7-ch75
calib_packv5_040323_1717.root, FC#2, port C3
Entries 141
Mean 54.83
Std Dev 10.28
Turn on : 50.3236
Width : 2.416
Height : 9.925
Entry
ampl
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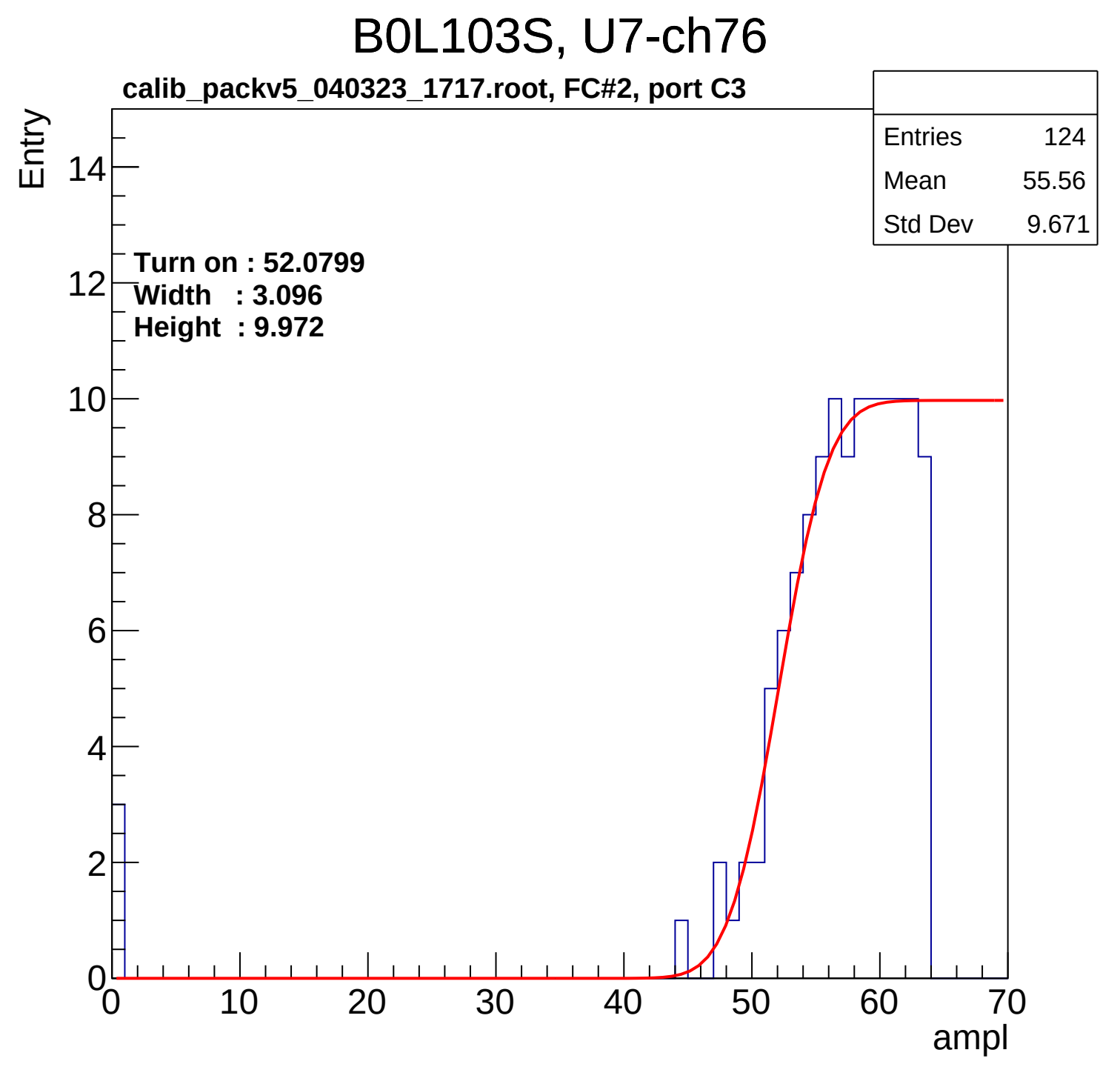
B0L103S, U7-ch76
calib_packv5_040323_1717.root, FC#2, port C3
Entries 124
Mean 55.56
Std Dev 9.671
Turn on : 52.0799
Width : 3.096
Height : 9.972
Entry
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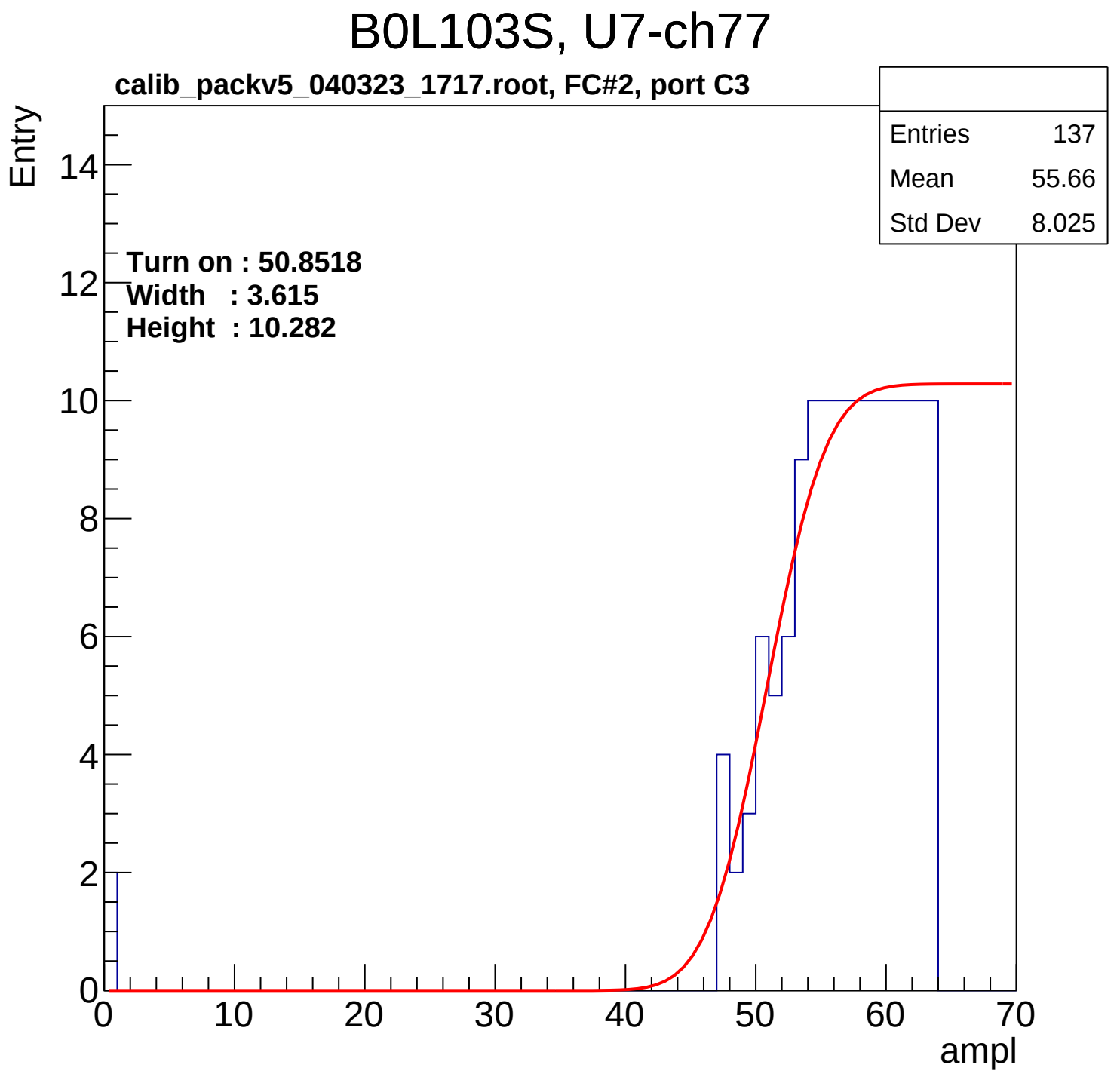
B0L103S, U7-ch77
calib_packv5_040323_1717.root, FC#2, port C3
Entries 137
Mean 55.66
Std Dev 8.025
Turn on : 50.8518
Width : 3.615
Height : 10.282
Entry
ampl
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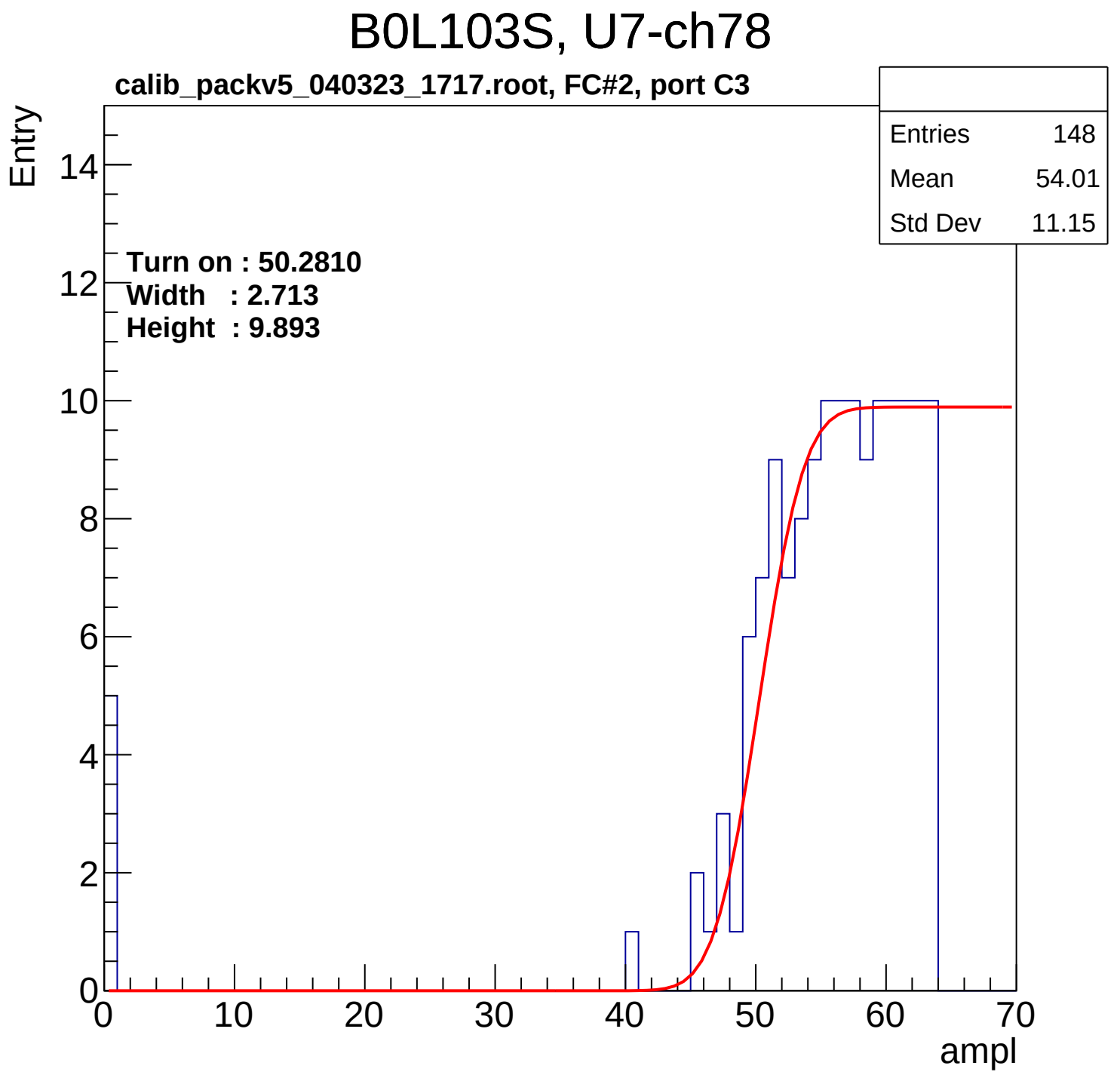
B0L103S, U7-ch78
calib_packv5_040323_1717.root, FC#2, port C3
Entries 148
Mean 54.01
Std Dev 11.15
Turn on : 50.2810
Width : 2.713
Height : 9.893
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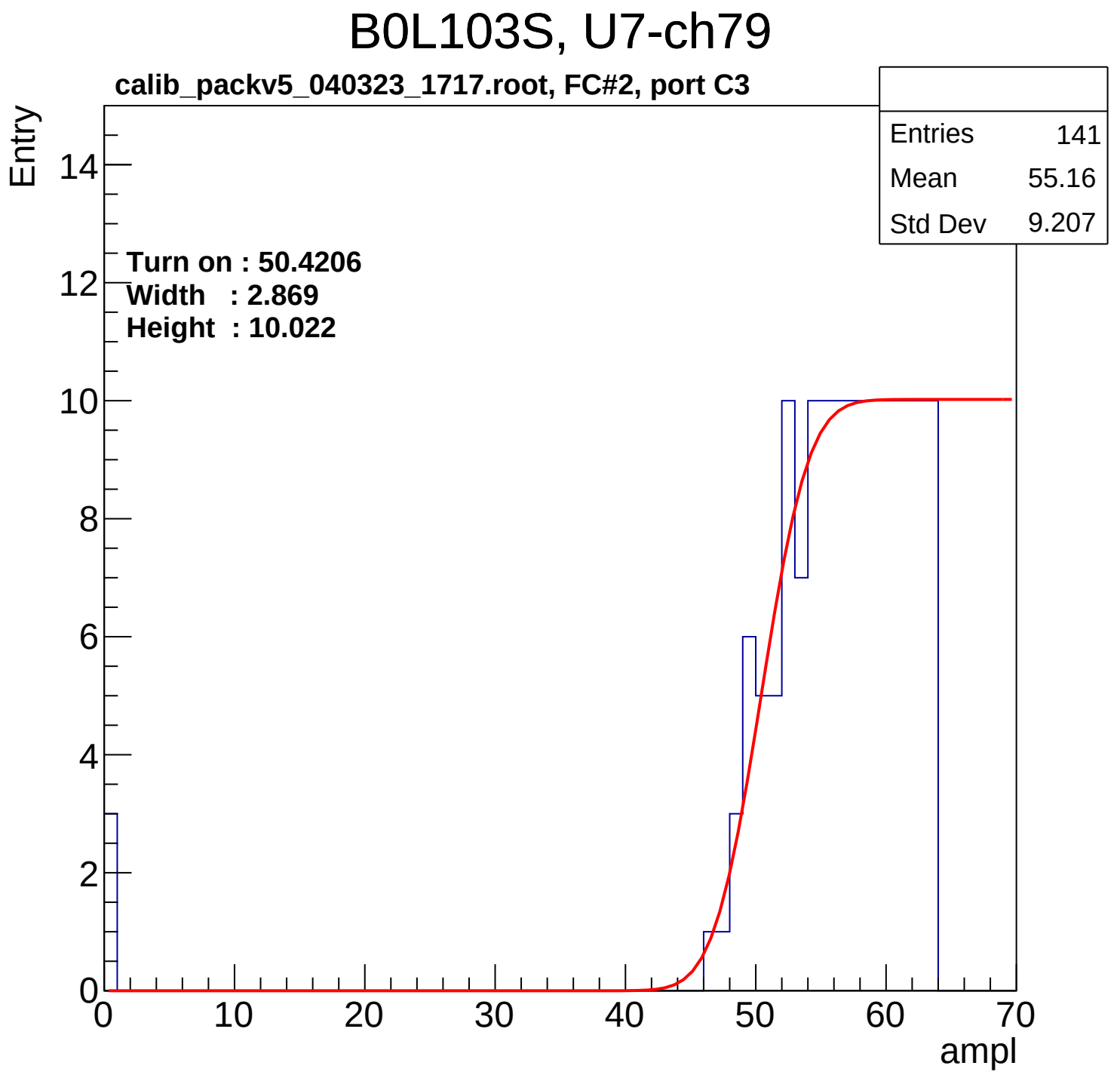
B0L103S, U7-ch79
calib_packv5_040323_1717.root, FC#2, port C3
Entries 141
Mean 55.16
Std Dev 9.207
Turn on : 50.4206
Width : 2.869
Height : 10.022
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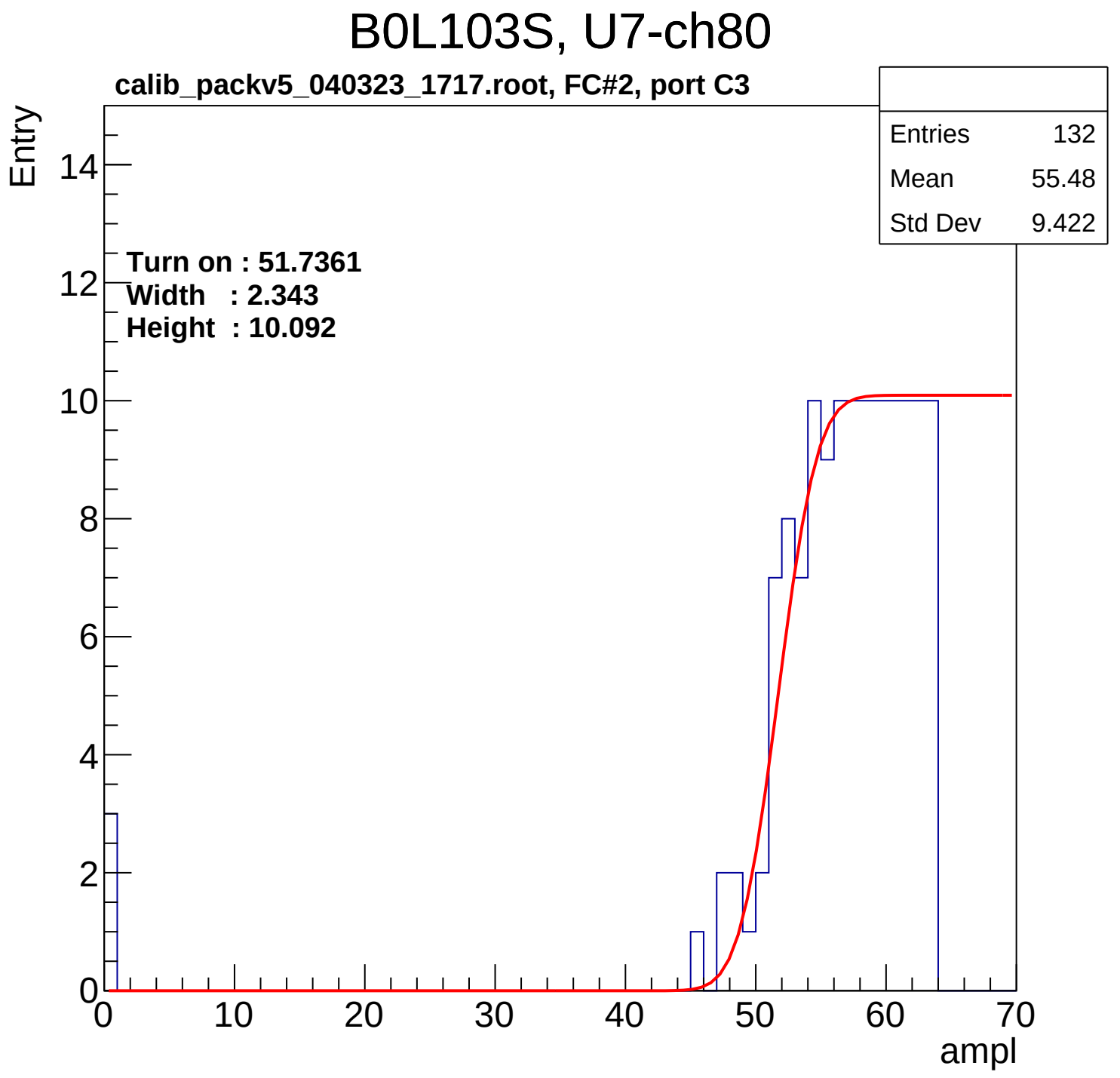
B0L103S, U7-ch80
calib_packv5_040323_1717.root, FC#2, port C3
Entries 132
Mean 55.48
Std Dev 9.422
Turn on : 51.7361
Width : 2.343
Height : 10.092
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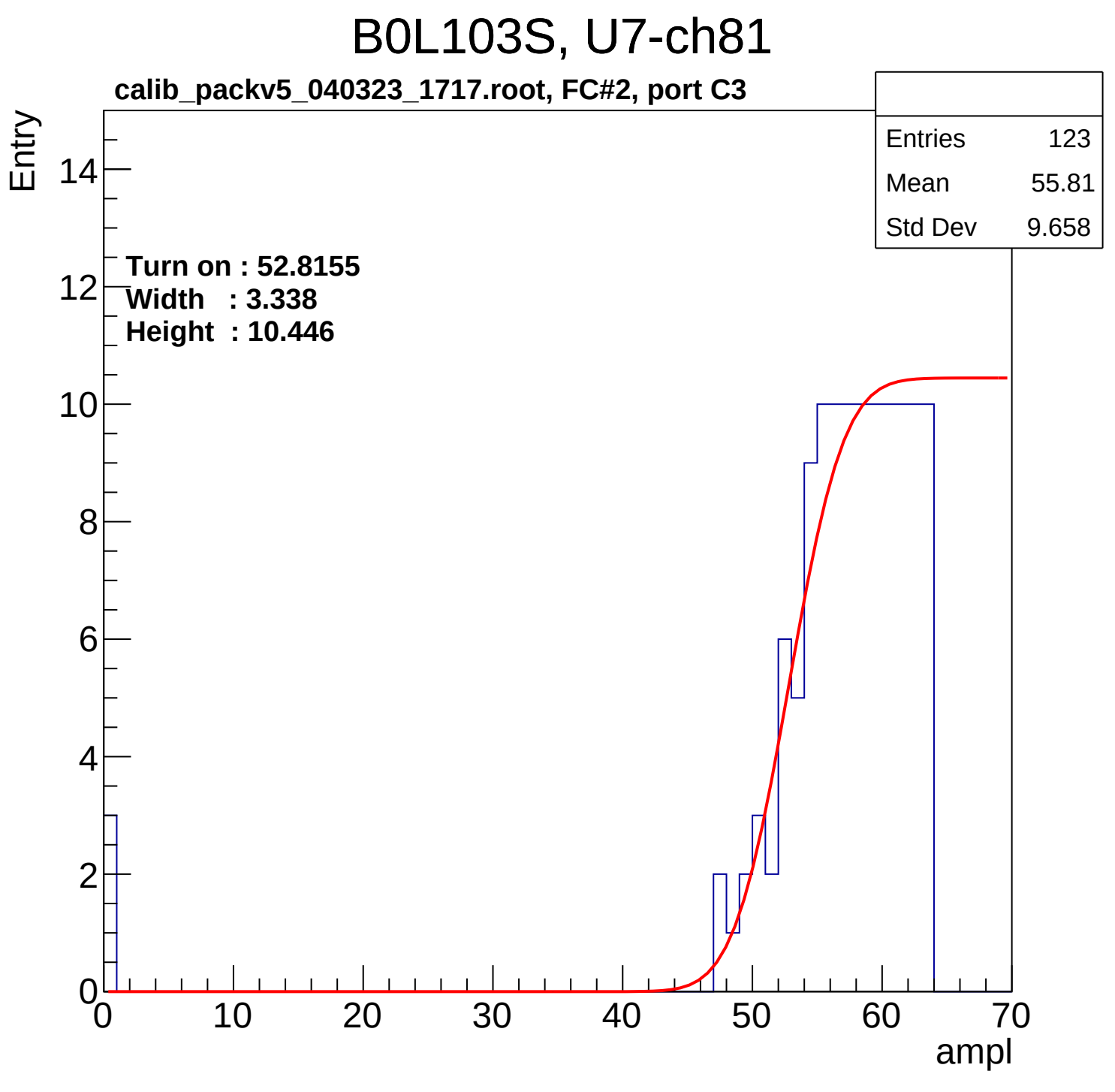
B0L103S, U7-ch81
calib_packv5_040323_1717.root, FC#2, port C3
Entries 123
Mean 55.81
Std Dev 9.658
Turn on : 52.8155
Width : 3.338
Height : 10.446
Entry
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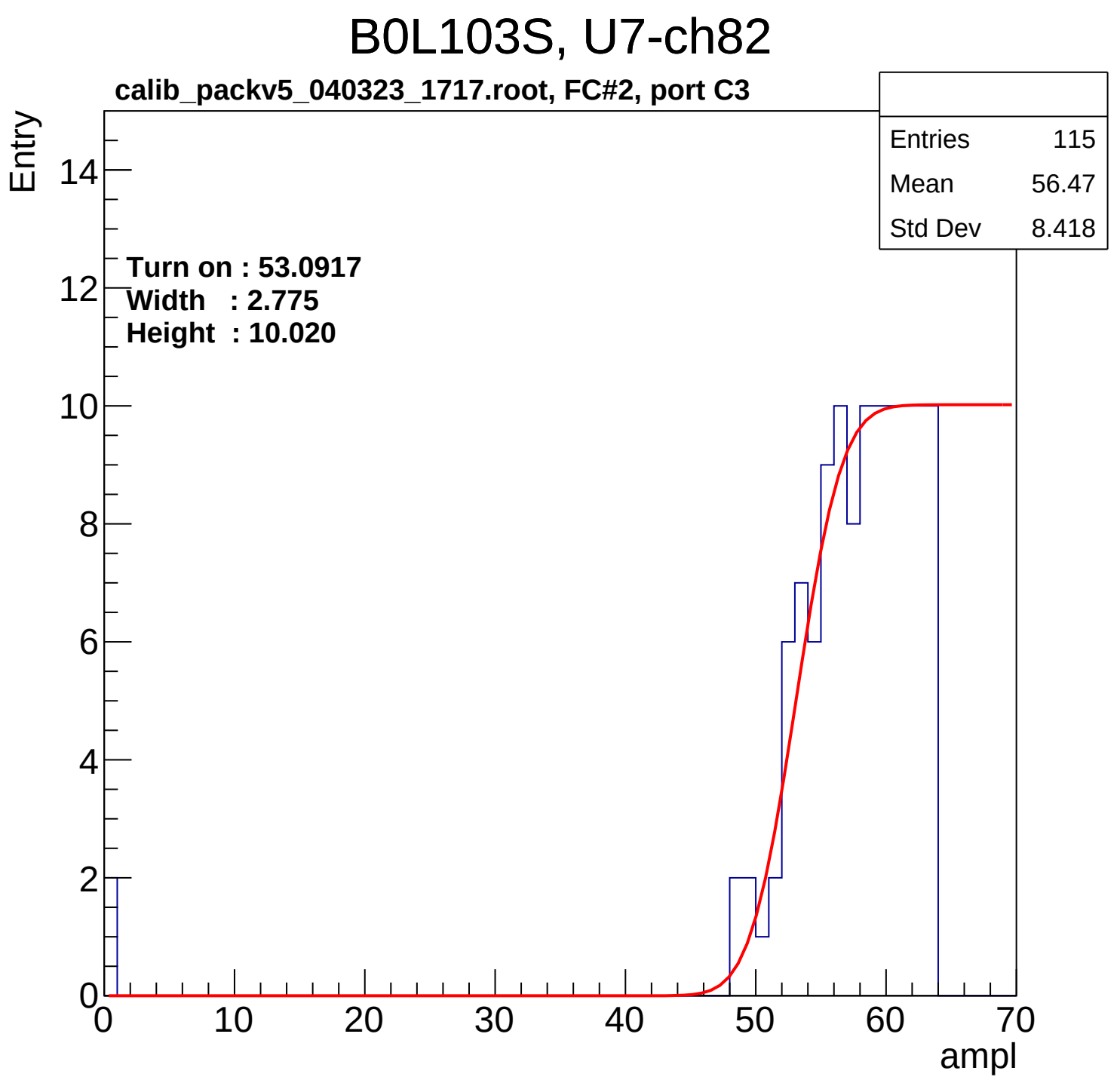
B0L103S, U7-ch82
calib_packv5_040323_1717.root, FC#2, port C3
Entries 115
Mean 56.47
Std Dev 8.418
Turn on : 53.0917
Width : 2.775
Height : 10.020
Entry
ampl
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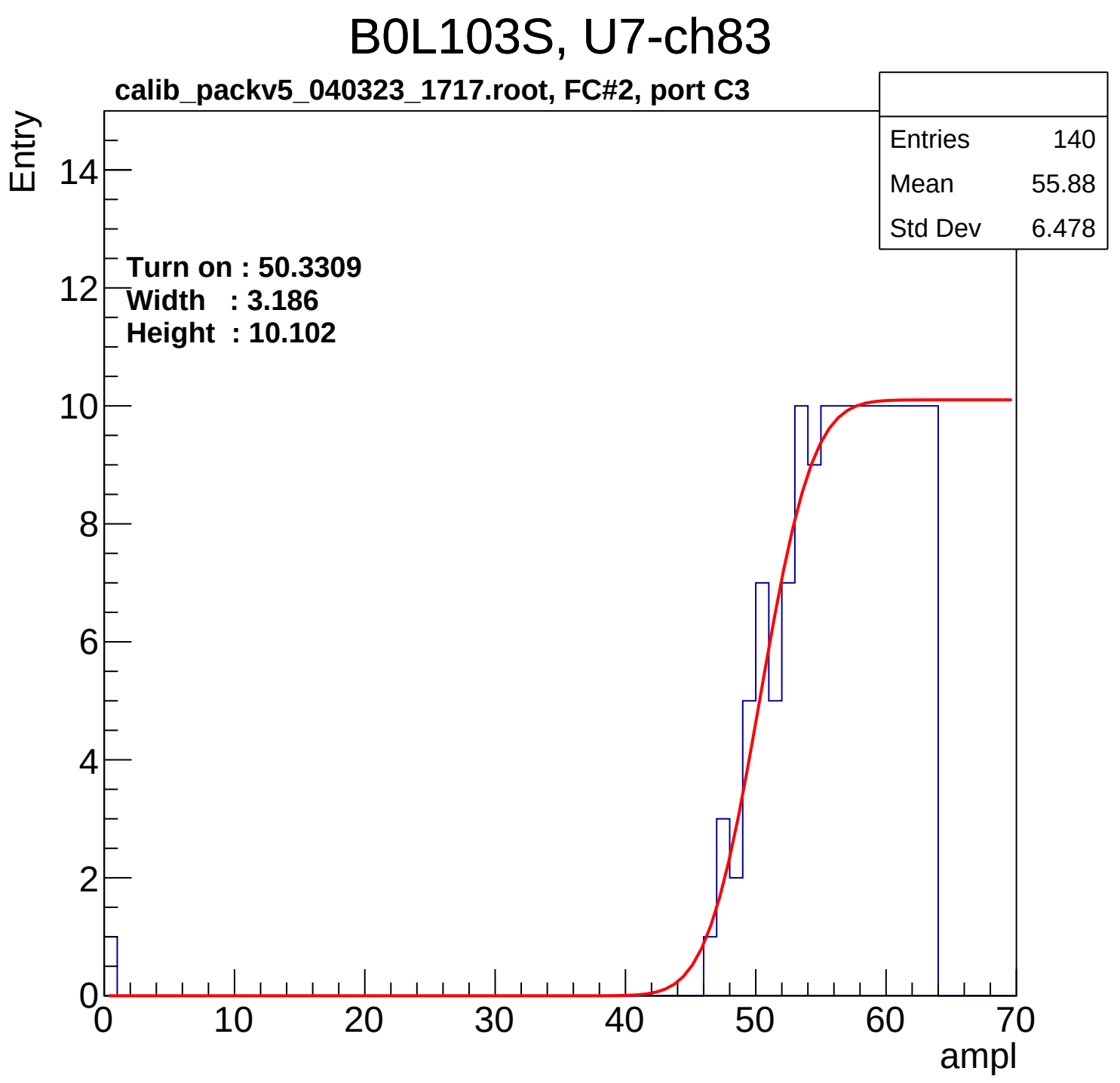
B0L103S, U7-ch83
calib_packv5_040323_1717.root, FC#2, port C3
Entries 140
Mean 55.88
Std Dev 6.478
Turn on : 50.3309
Width : 3.186
Height : 10.102
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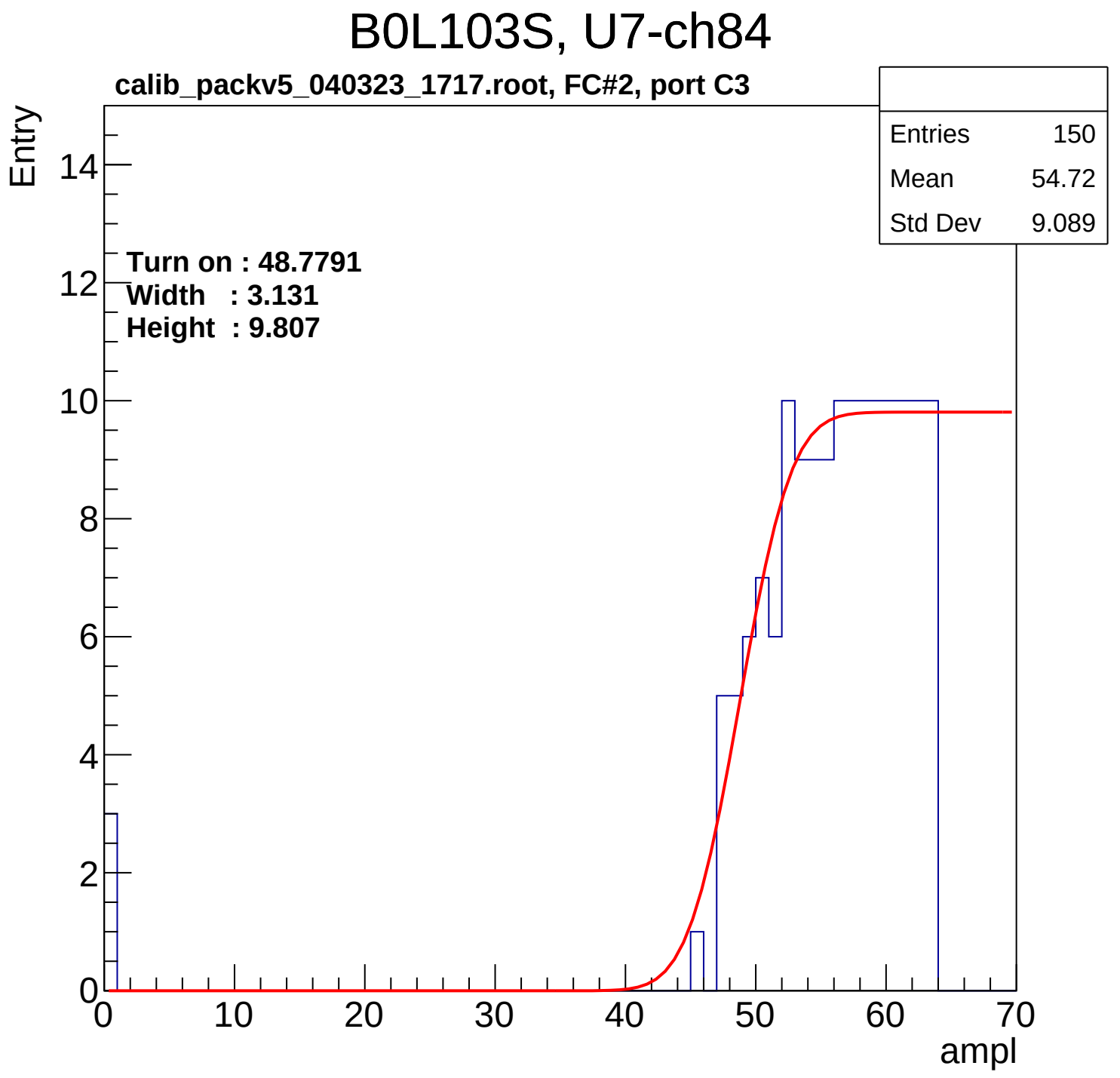
B0L103S, U7-ch84
calib_packv5_040323_1717.root, FC#2, port C3
Entries 150
Mean 54.72
Std Dev 9.089
Turn on : 48.7791
Width : 3.131
Height : 9.807
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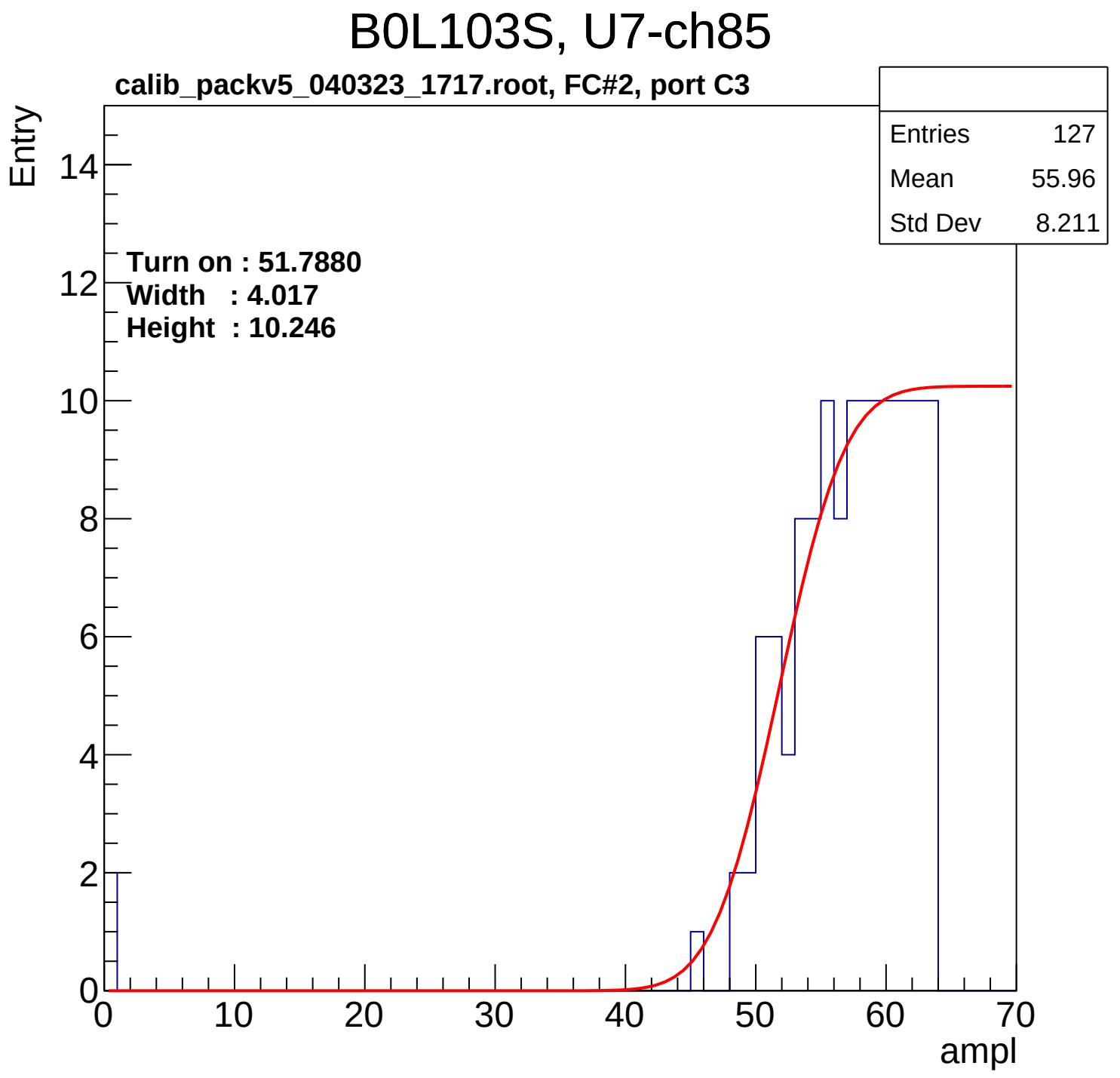
B0L103S, U7-ch85
calib_packv5_040323_1717.root, FC#2, port C3
Entries 127
Mean 55.96
Std Dev 8.211
Turn on : 51.7880
Width : 4.017
Height : 10.246
Entry
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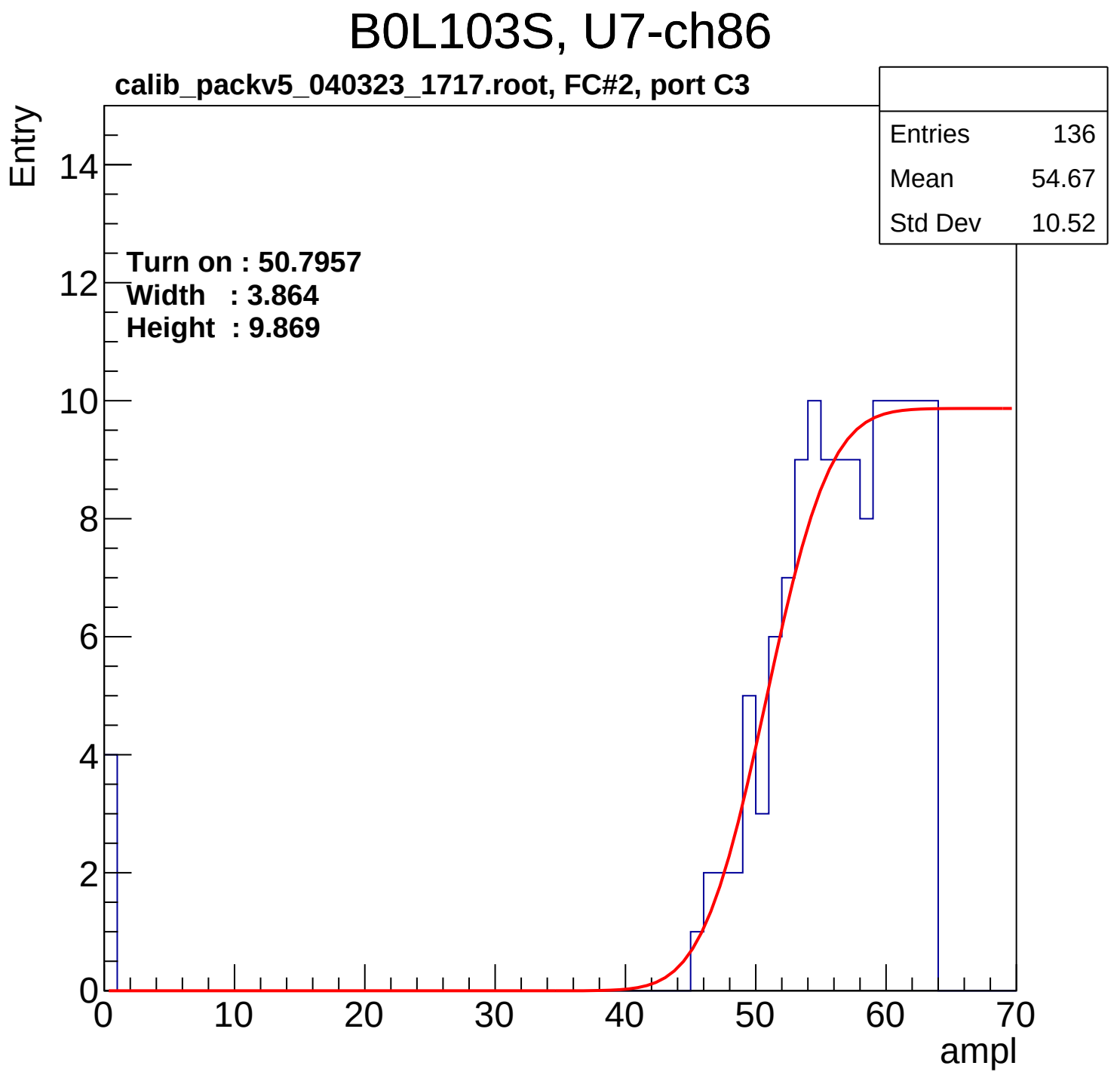
B0L103S, U7-ch86
calib_packv5_040323_1717.root, FC#2, port C3
Entries 136
Mean 54.67
Std Dev 10.52
Turn on : 50.7957
Width : 3.864
Height : 9.869
Entry
ampl
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4
6
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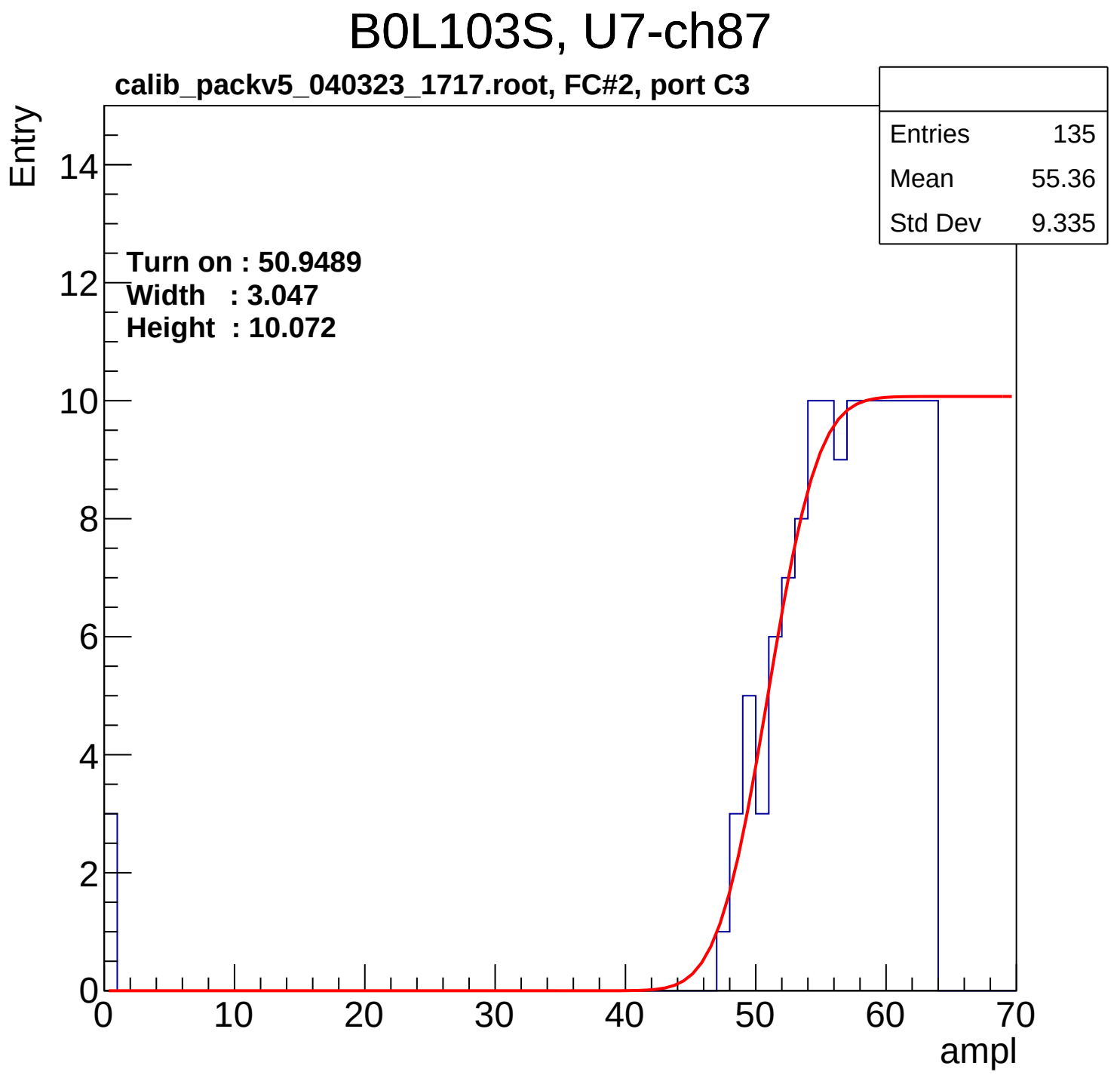
B0L103S, U7-ch87
calib_packv5_040323_1717.root, FC#2, port C3
Entries 135
Mean 55.36
Std Dev 9.335
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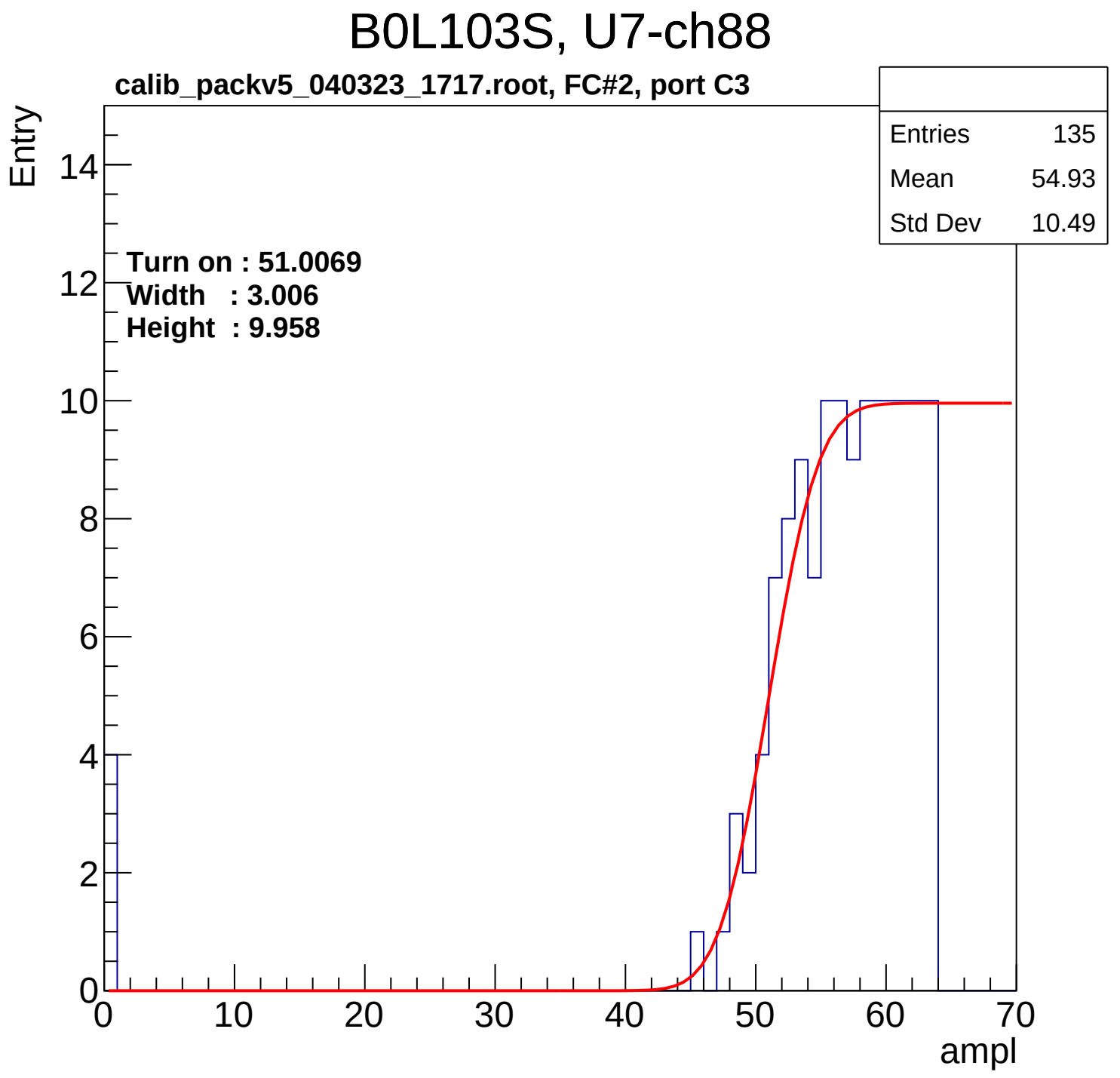
B0L103S, U7-ch88
calib_packv5_040323_1717.root, FC#2, port C3
Entries 135
Mean 54.93
Std Dev 10.49
Turn on : 51.0069
Width : 3.006
Height : 9.958
Entry
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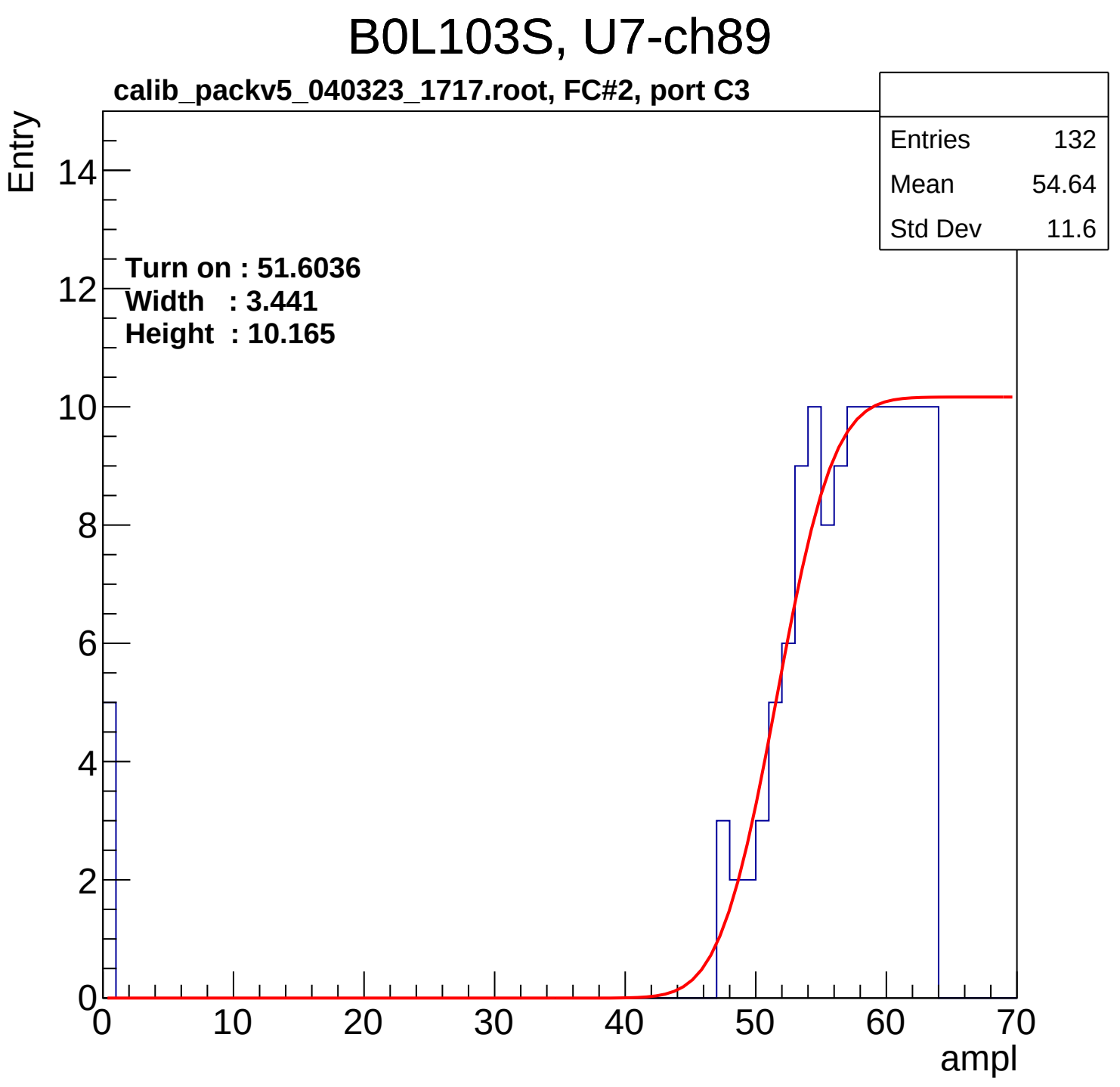
B0L103S, U7-ch89
calib_packv5_040323_1717.root, FC#2, port C3
Entries 132
Mean 54.64
Std Dev 11.6
Turn on : 51.6036
Width : 3.441
Height : 10.165
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ampl
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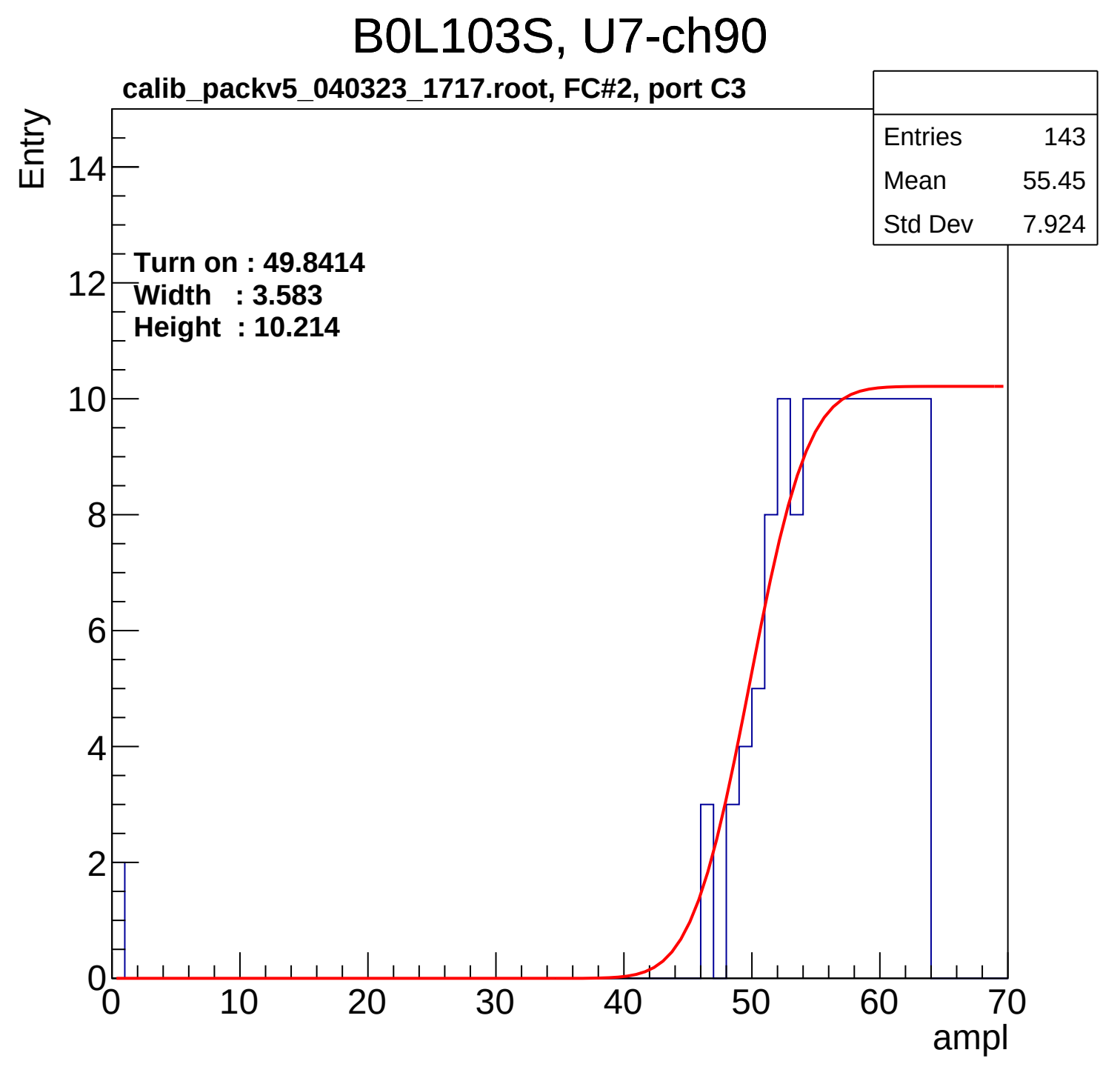
B0L103S, U7-ch90
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 55.45
Std Dev 7.924
Turn on : 49.8414
Width : 3.583
Height : 10.214
Entry
ampl
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6
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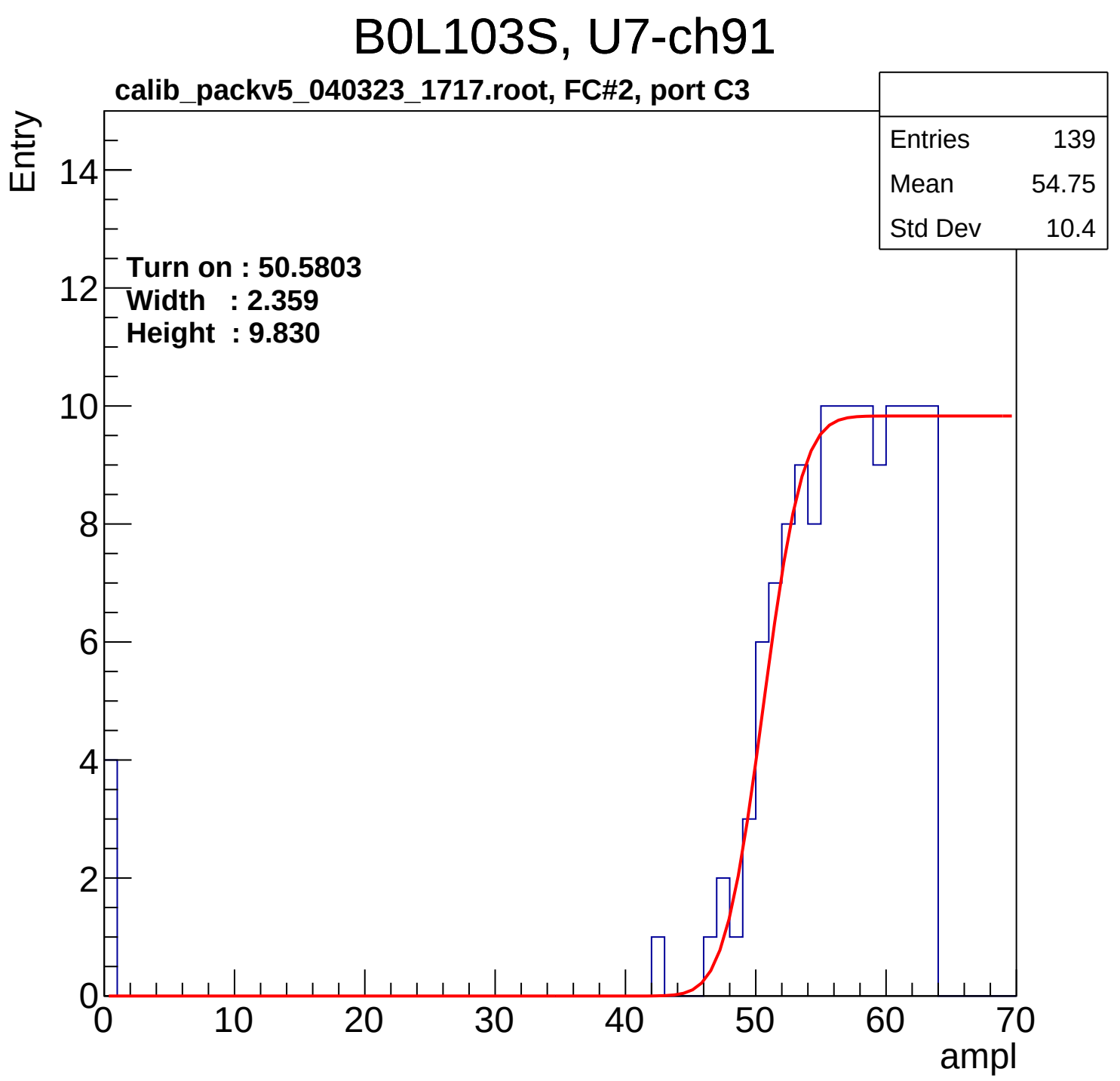
B0L103S, U7-ch91
calib_packv5_040323_1717.root, FC#2, port C3
Entries 139
Mean 54.75
Std Dev 10.4
Turn on : 50.5803
Width : 2.359
Height : 9.830
Entry
ampl
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6
8
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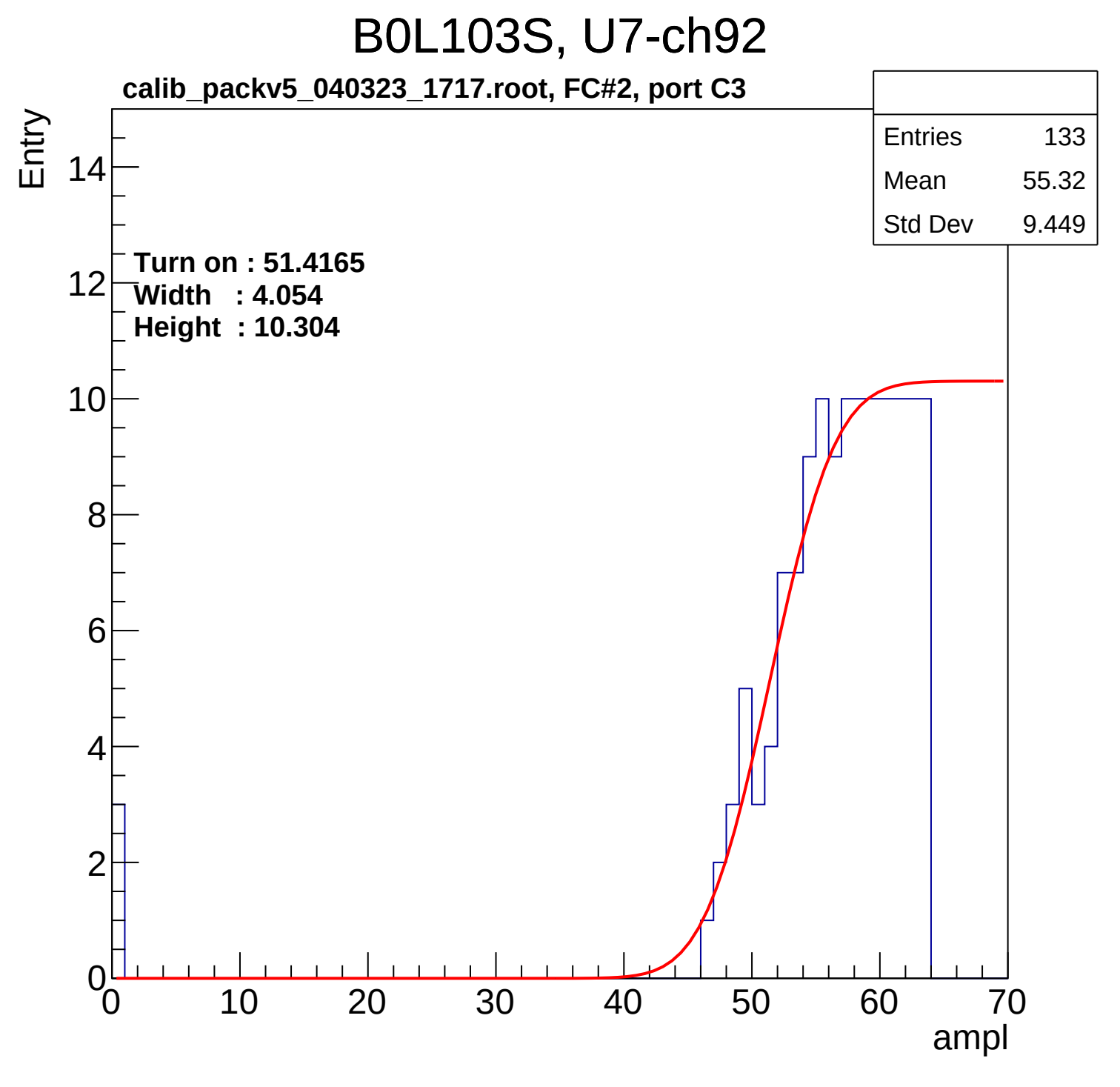
B0L103S, U7-ch92
calib_packv5_040323_1717.root, FC#2, port C3
Entries 133
Mean 55.32
Std Dev 9.449
Turn on : 51.4165
Width : 4.054
Height : 10.304
Entry
ampl
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4
6
8
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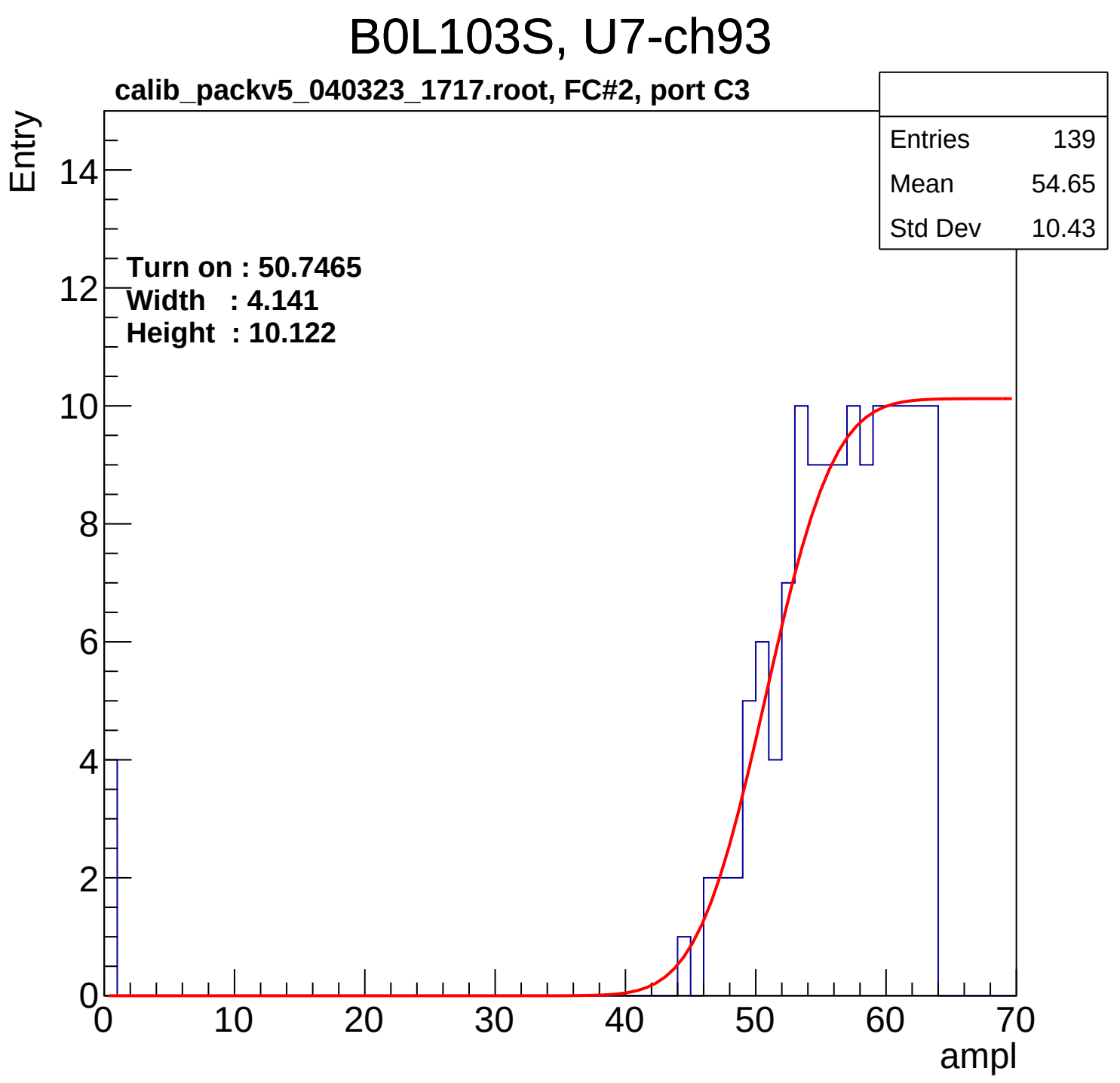
B0L103S, U7-ch93
calib_packv5_040323_1717.root, FC#2, port C3
Entries 139
Mean 54.65
Std Dev 10.43
Turn on : 50.7465
Width : 4.141
Height : 10.122
Entry
ampl
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6
8
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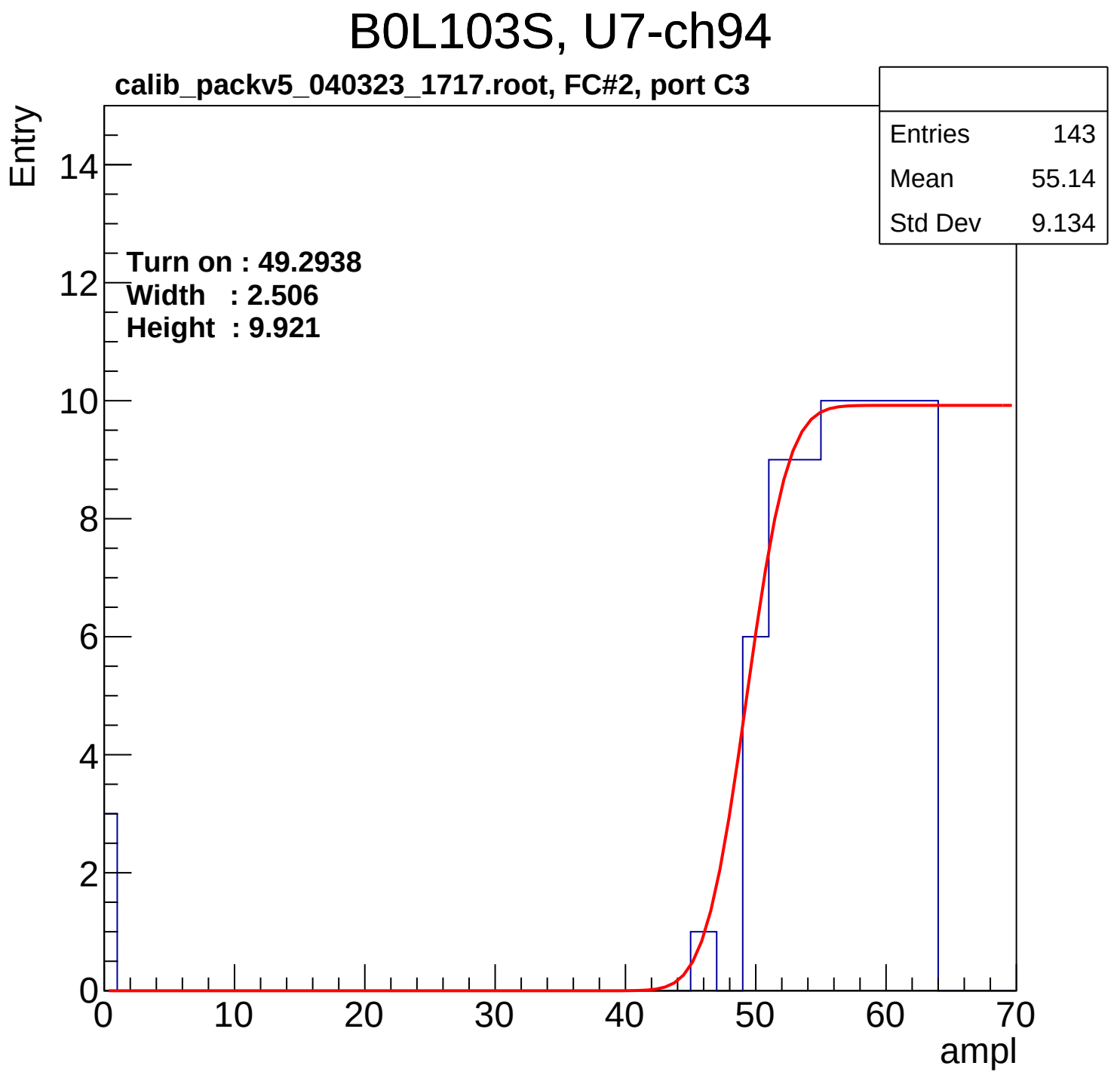
B0L103S, U7-ch94
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 55.14
Std Dev 9.134
Turn on : 49.2938
Width : 2.506
Height : 9.921
Entry
ampl
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2
4
6
8
10
12
14
0
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20
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60
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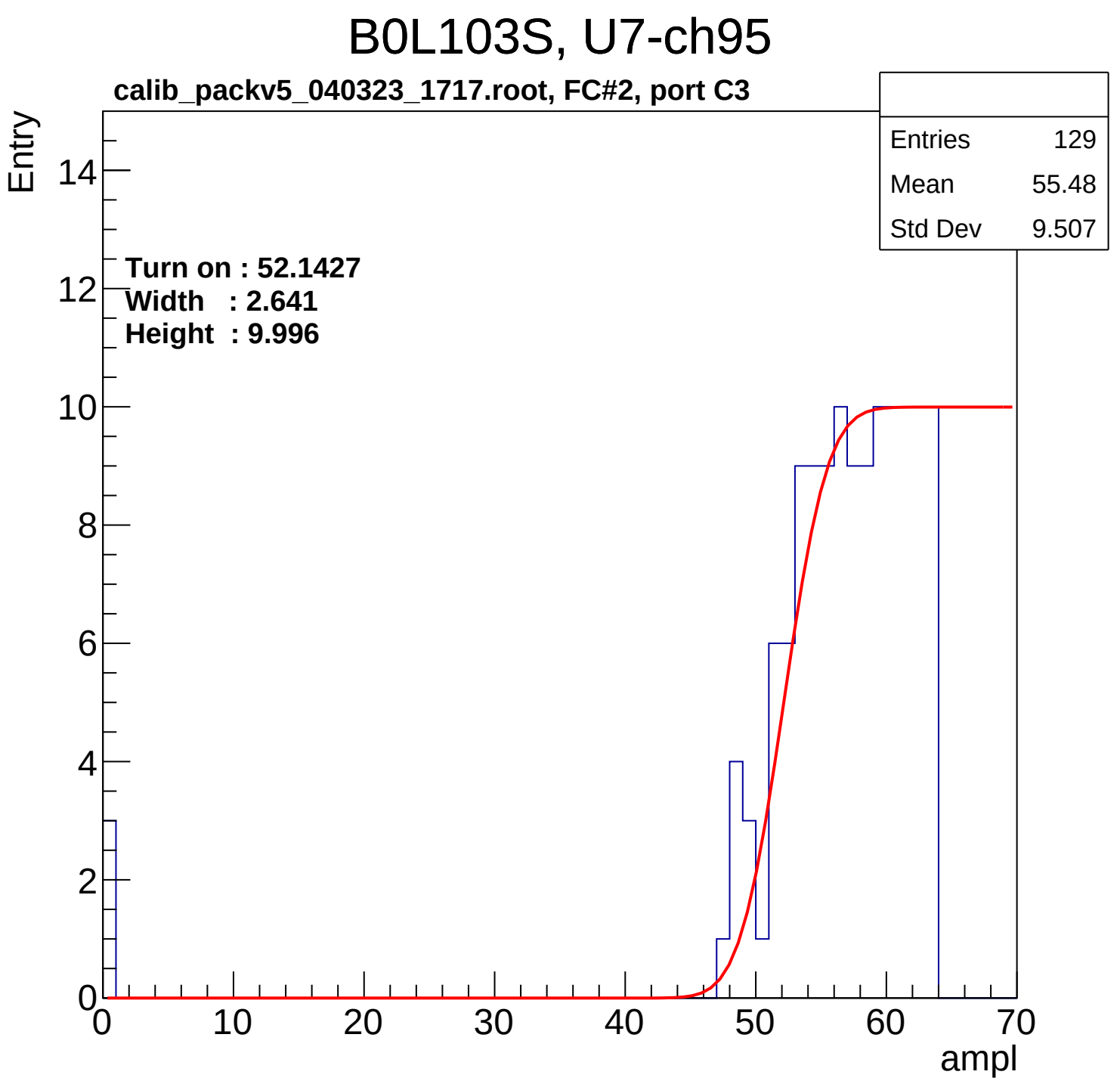
B0L103S, U7-ch95
calib_packv5_040323_1717.root, FC#2, port C3
Entries 129
Mean 55.48
Std Dev 9.507
Turn on : 52.1427
Width : 2.641
Height : 9.996
Entry
ampl
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6
8
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12
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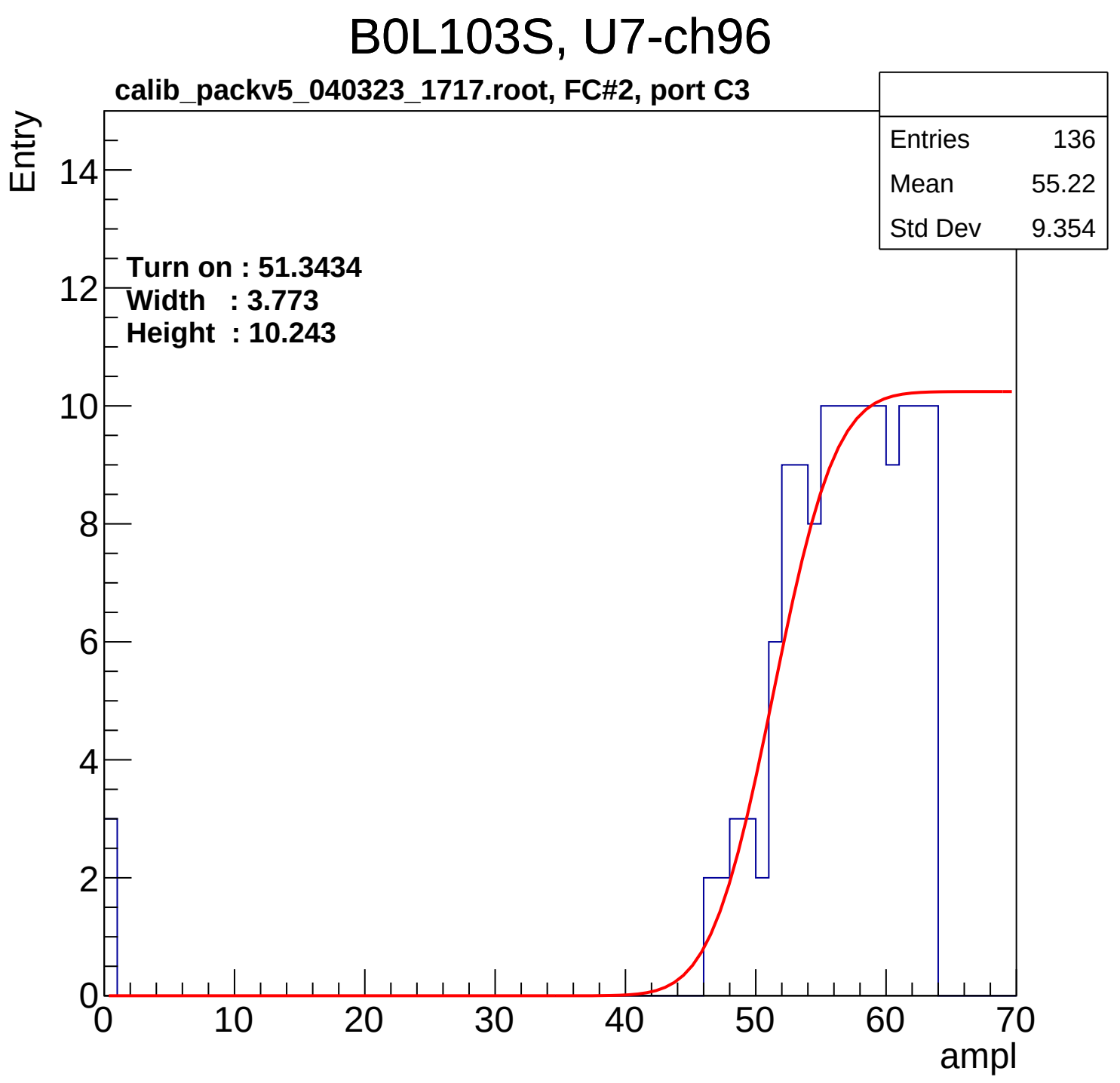
B0L103S, U7-ch96
calib_packv5_040323_1717.root, FC#2, port C3
Entries 136
Mean 55.22
Std Dev 9.354
Turn on : 51.3434
Width : 3.773
Height : 10.243
Entry
ampl
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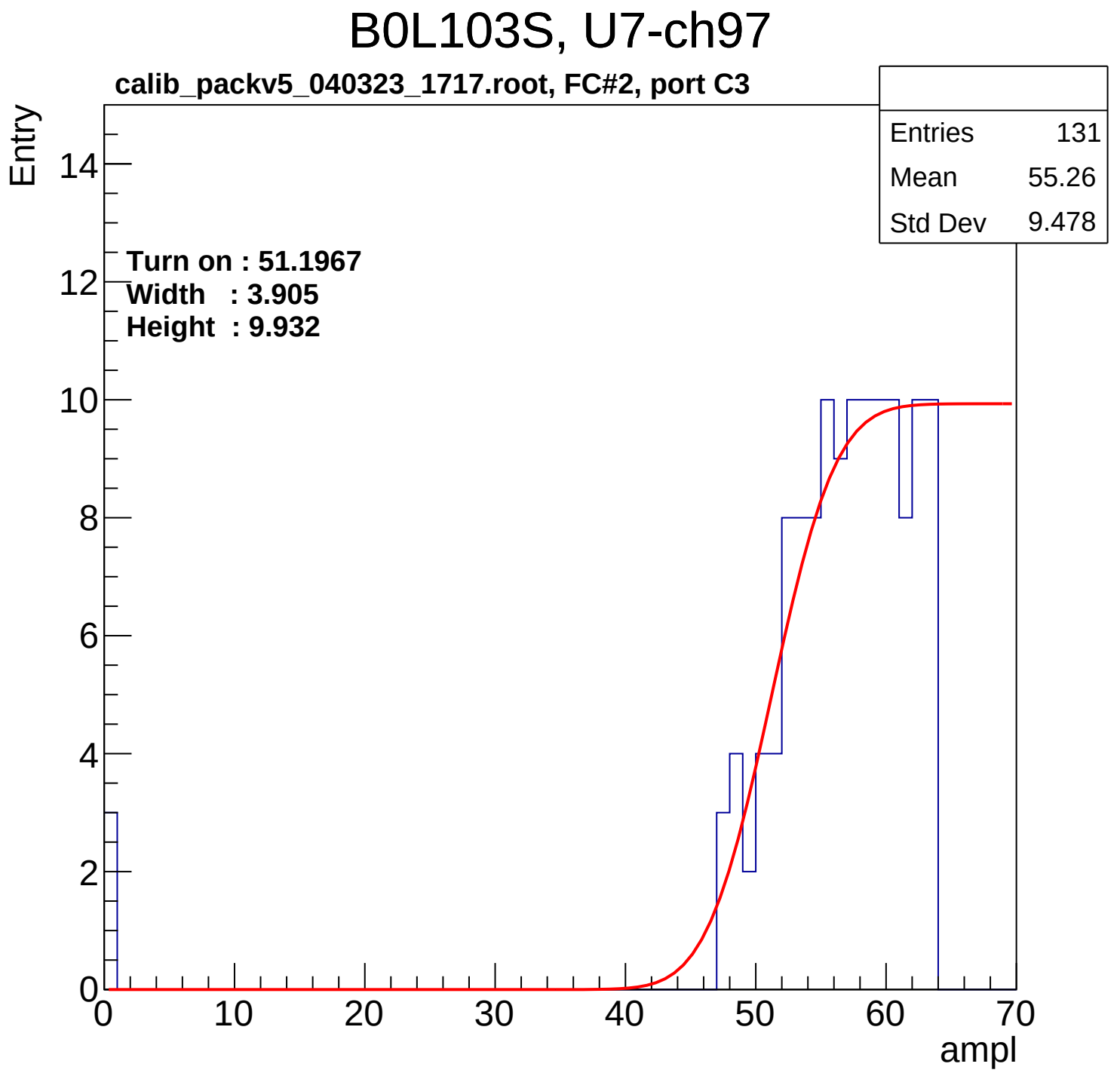
B0L103S, U7-ch97
calib_packv5_040323_1717.root, FC#2, port C3
Entries 131
Mean 55.26
Std Dev 9.478
Turn on : 51.1967
Width : 3.905
Height : 9.932
Entry
ampl
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6
8
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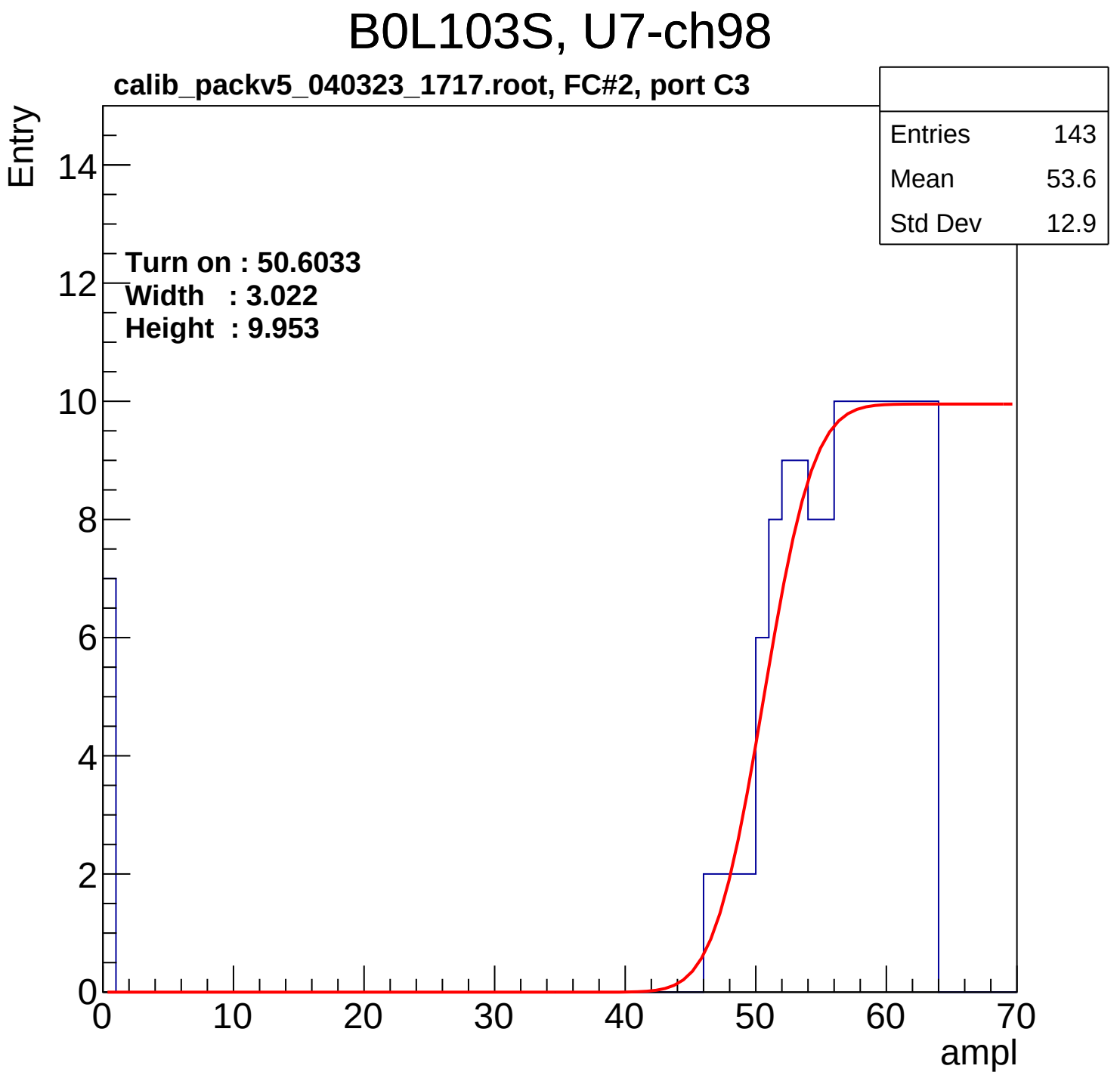
B0L103S, U7-ch98
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 53.6
Std Dev 12.9
Turn on : 50.6033
Width : 3.022
Height : 9.953
Entry
ampl
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10
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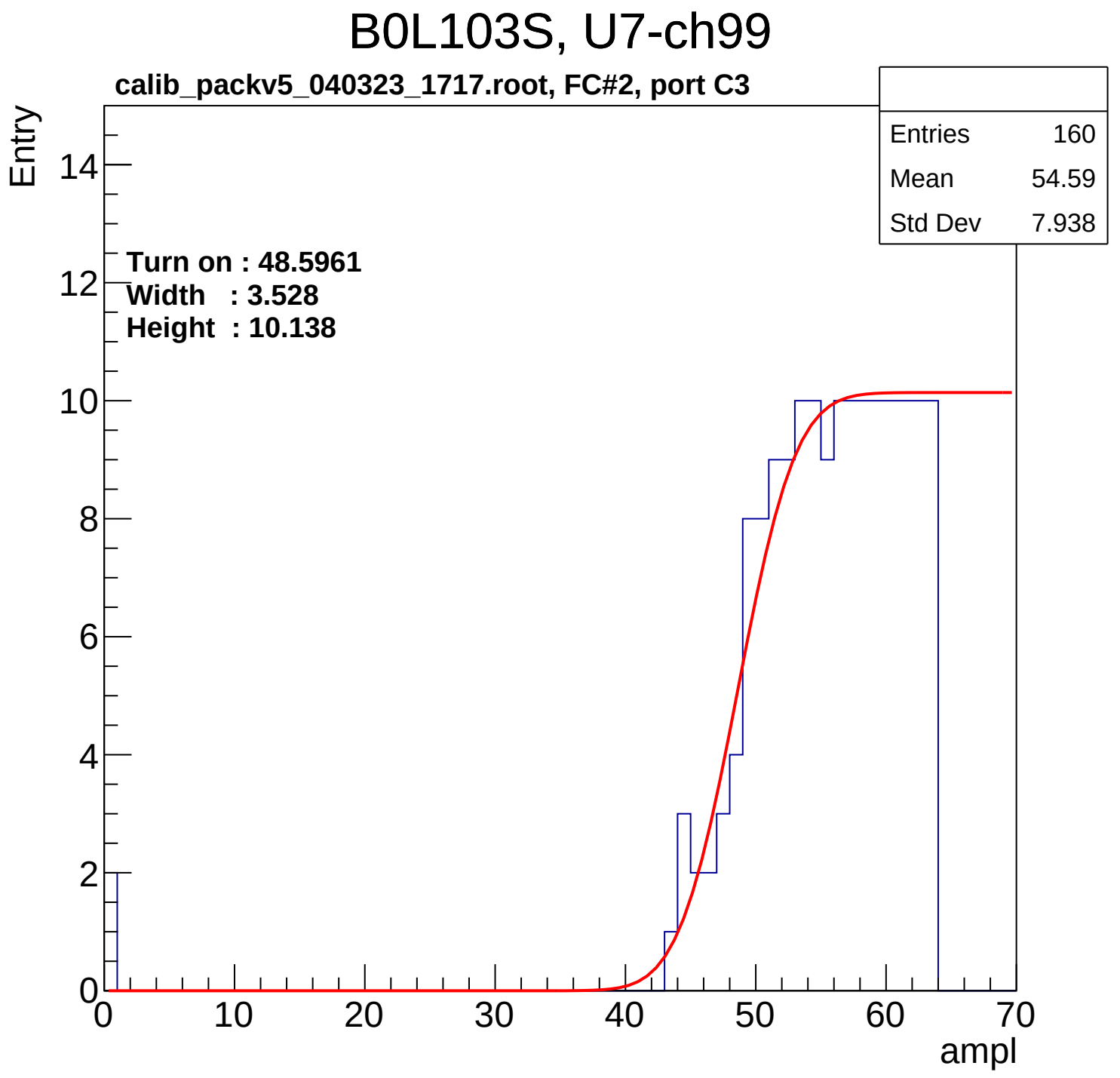
B0L103S, U7-ch99
calib_packv5_040323_1717.root, FC#2, port C3
Entries 160
Mean 54.59
Std Dev 7.938
Turn on : 48.5961
Width : 3.528
Height : 10.138
Entry
ampl
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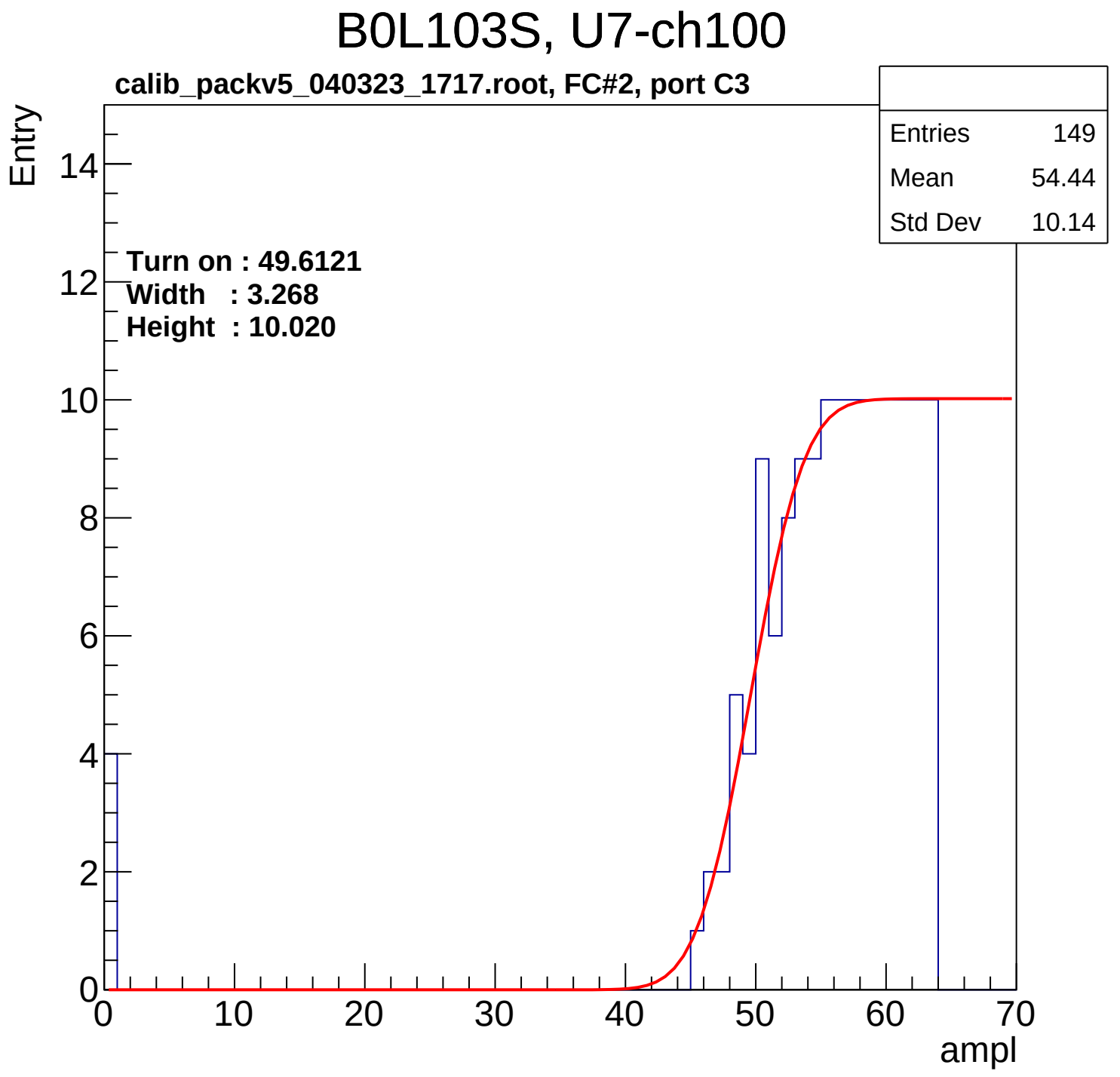
B0L103S, U7-ch100
calib_packv5_040323_1717.root, FC#2, port C3
Entries 149
Mean 54.44
Std Dev 10.14
Turn on : 49.6121
Width : 3.268
Height : 10.020
Entry
ampl
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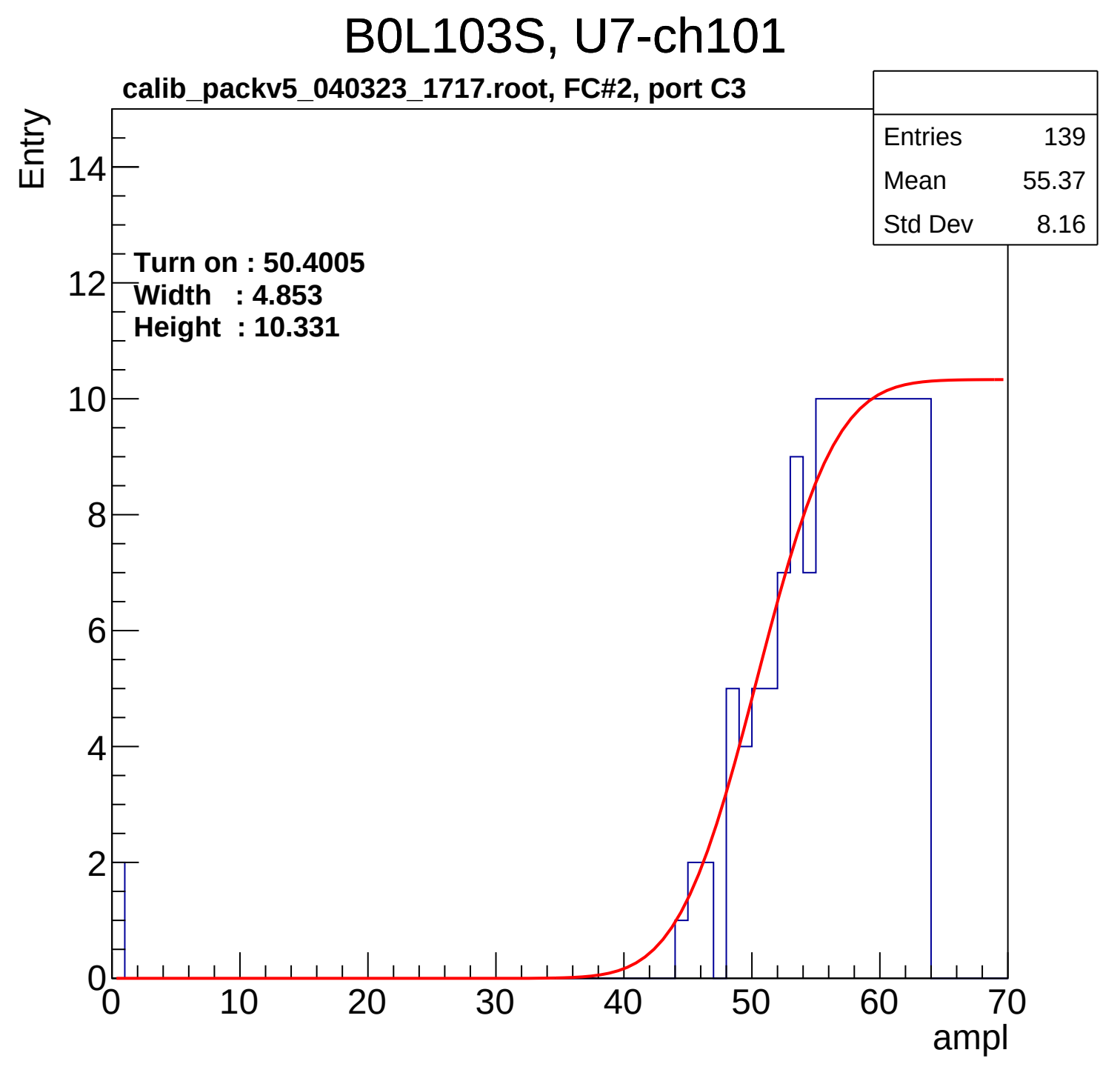
B0L103S, U7-ch101
calib_packv5_040323_1717.root, FC#2, port C3
Entries 139
Mean 55.37
Std Dev 8.16
Turn on : 50.4005
Width : 4.853
Height : 10.331
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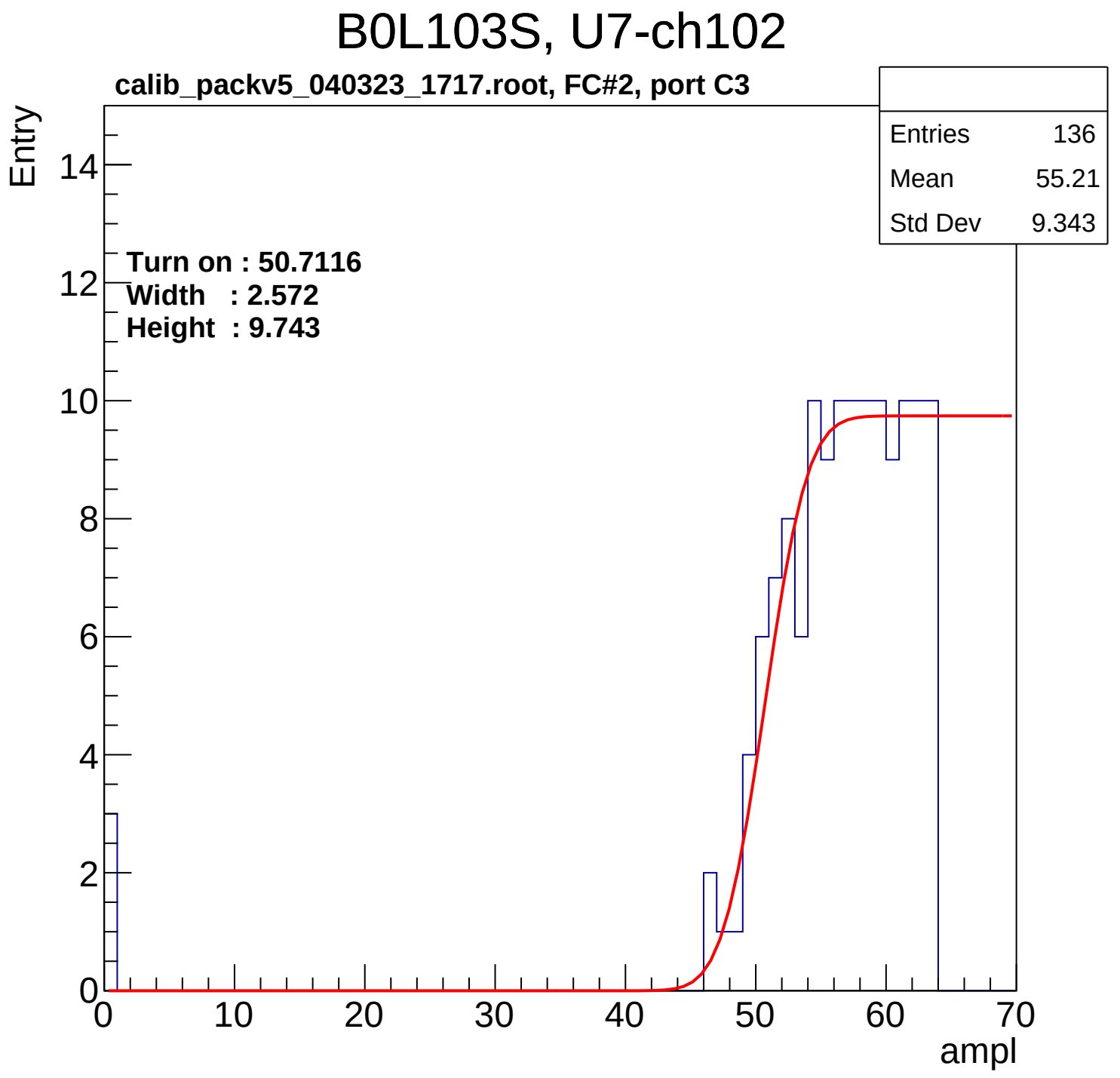
B0L103S, U7-ch102
calib_packv5_040323_1717.root, FC#2, port C3
Entries 136
Mean 55.21
Std Dev 9.343
Turn on : 50.7116
Width : 2.572
Height : 9.743
Entry
ampl
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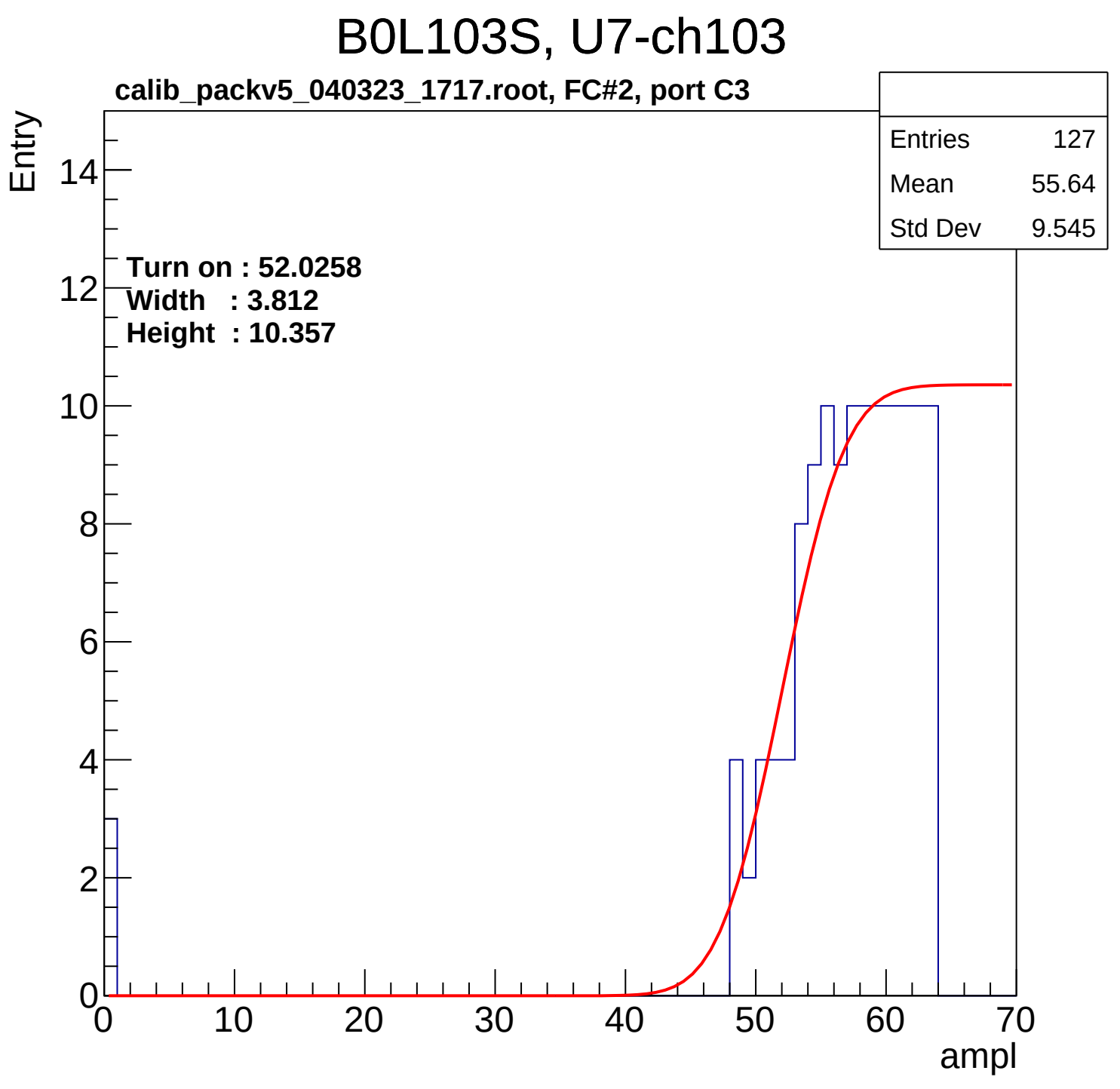
B0L103S, U7-ch103
calib_packv5_040323_1717.root, FC#2, port C3
Entries 127
Mean 55.64
Std Dev 9.545
Turn on : 52.0258
Width : 3.812
Height : 10.357
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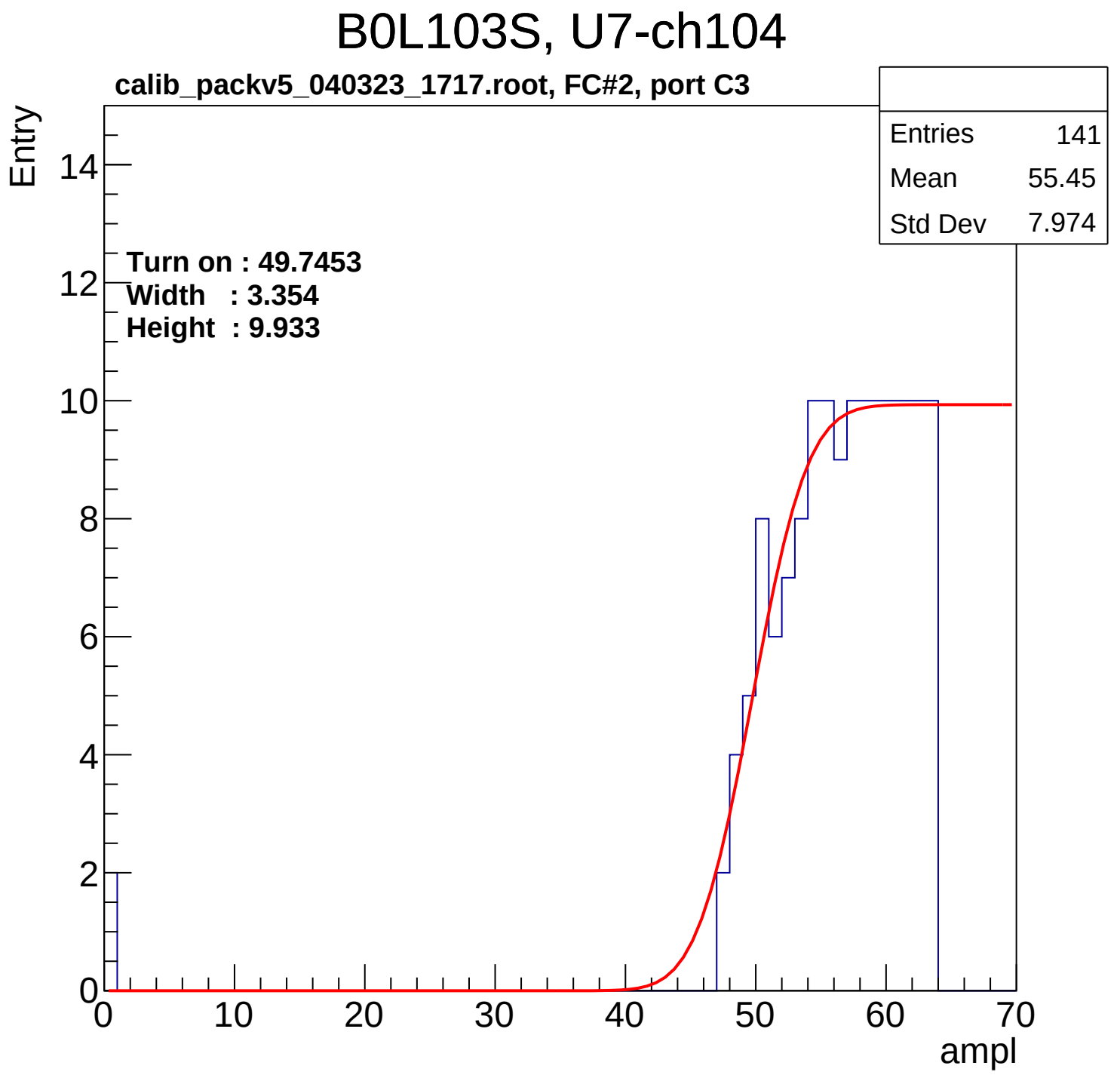
B0L103S, U7-ch104
calib_packv5_040323_1717.root, FC#2, port C3
Entries 141
Mean 55.45
Std Dev 7.974
Turn on : 49.7453
Width : 3.354
Height : 9.933
Entry
ampl
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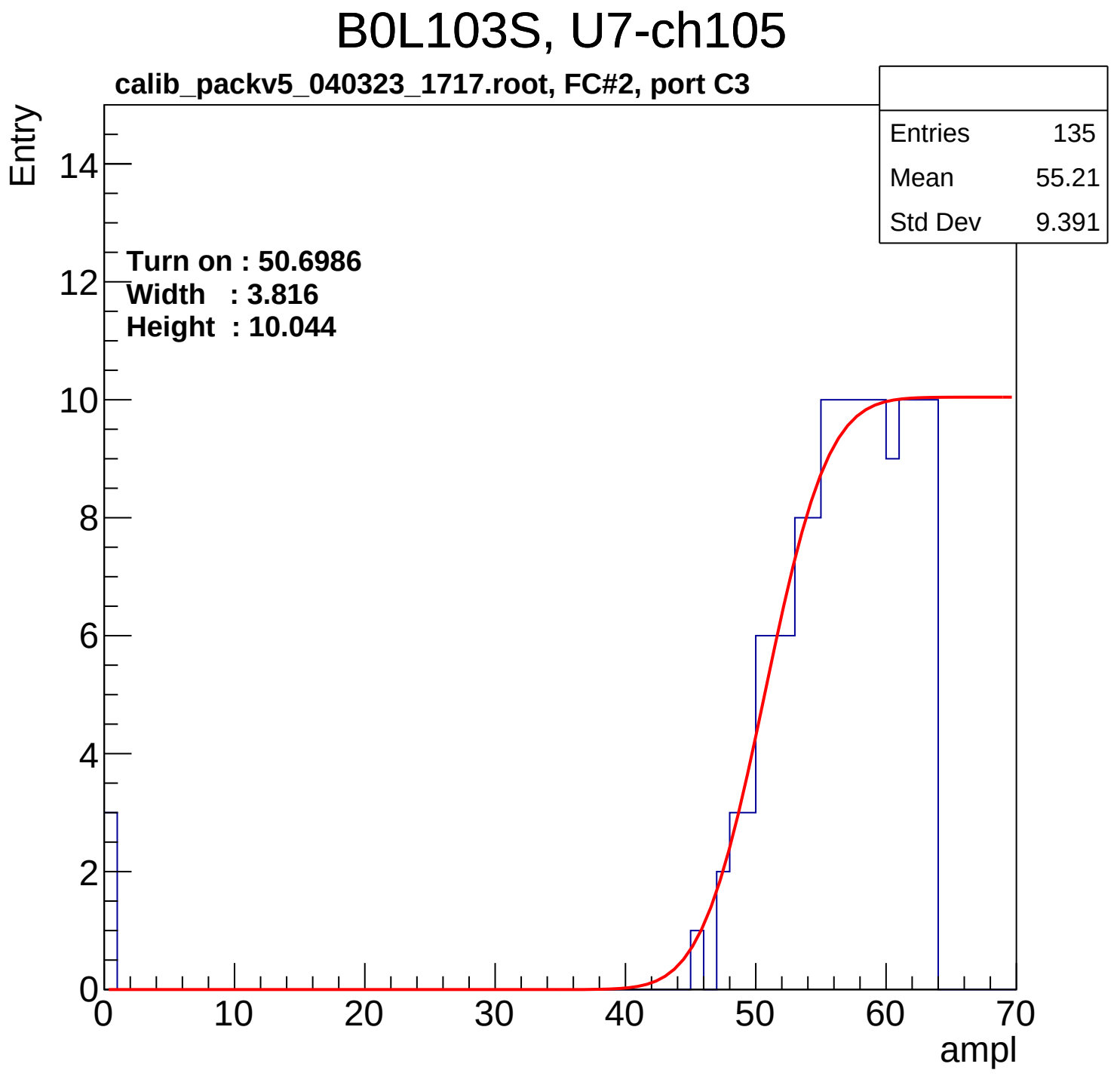
B0L103S, U7-ch105
calib_packv5_040323_1717.root, FC#2, port C3
Entries 135
Mean 55.21
Std Dev 9.391
Turn on : 50.6986
Width : 3.816
Height : 10.044
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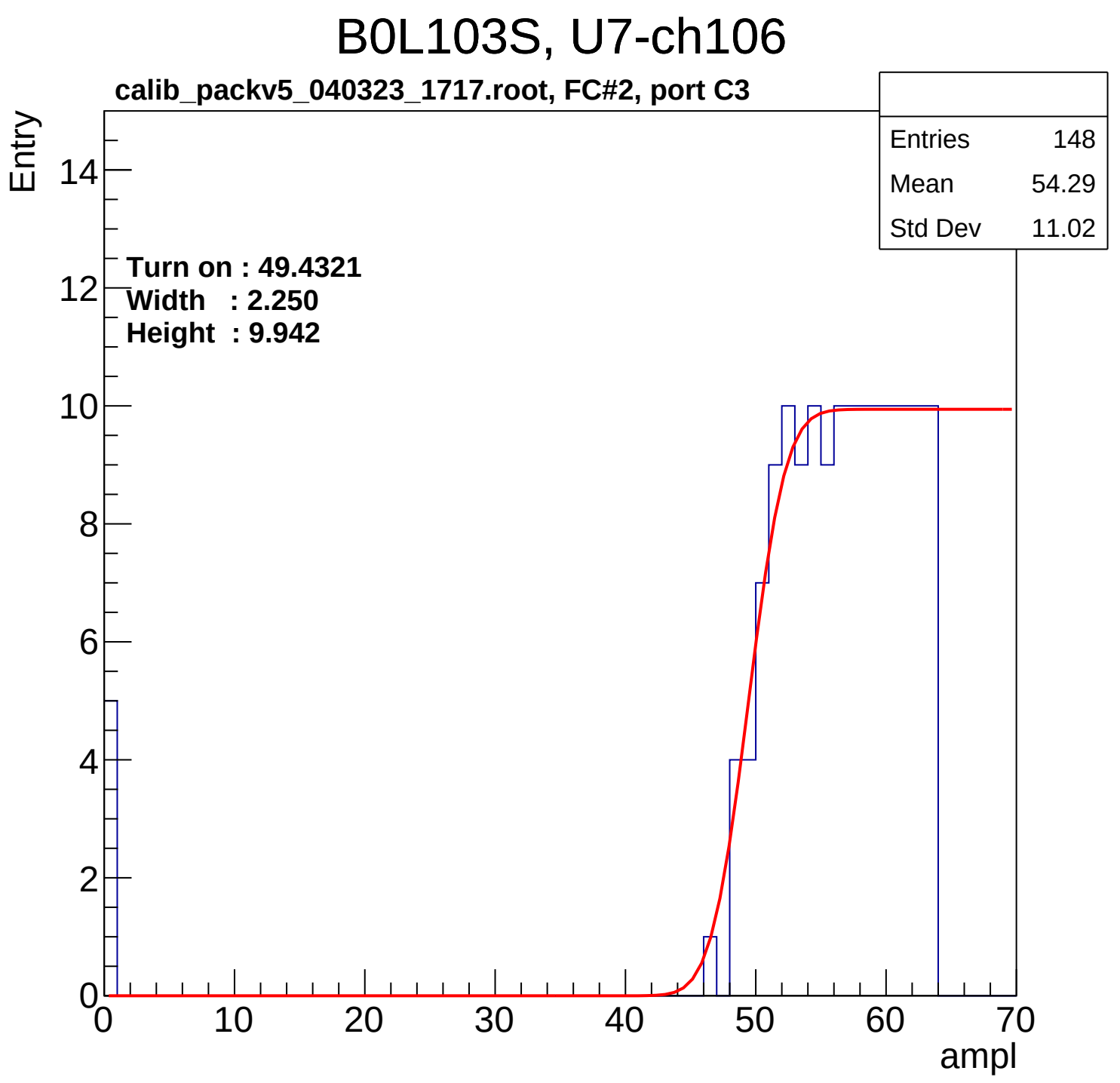
B0L103S, U7-ch106
calib_packv5_040323_1717.root, FC#2, port C3
Entries 148
Mean 54.29
Std Dev 11.02
Turn on : 49.4321
Width : 2.250
Height : 9.942
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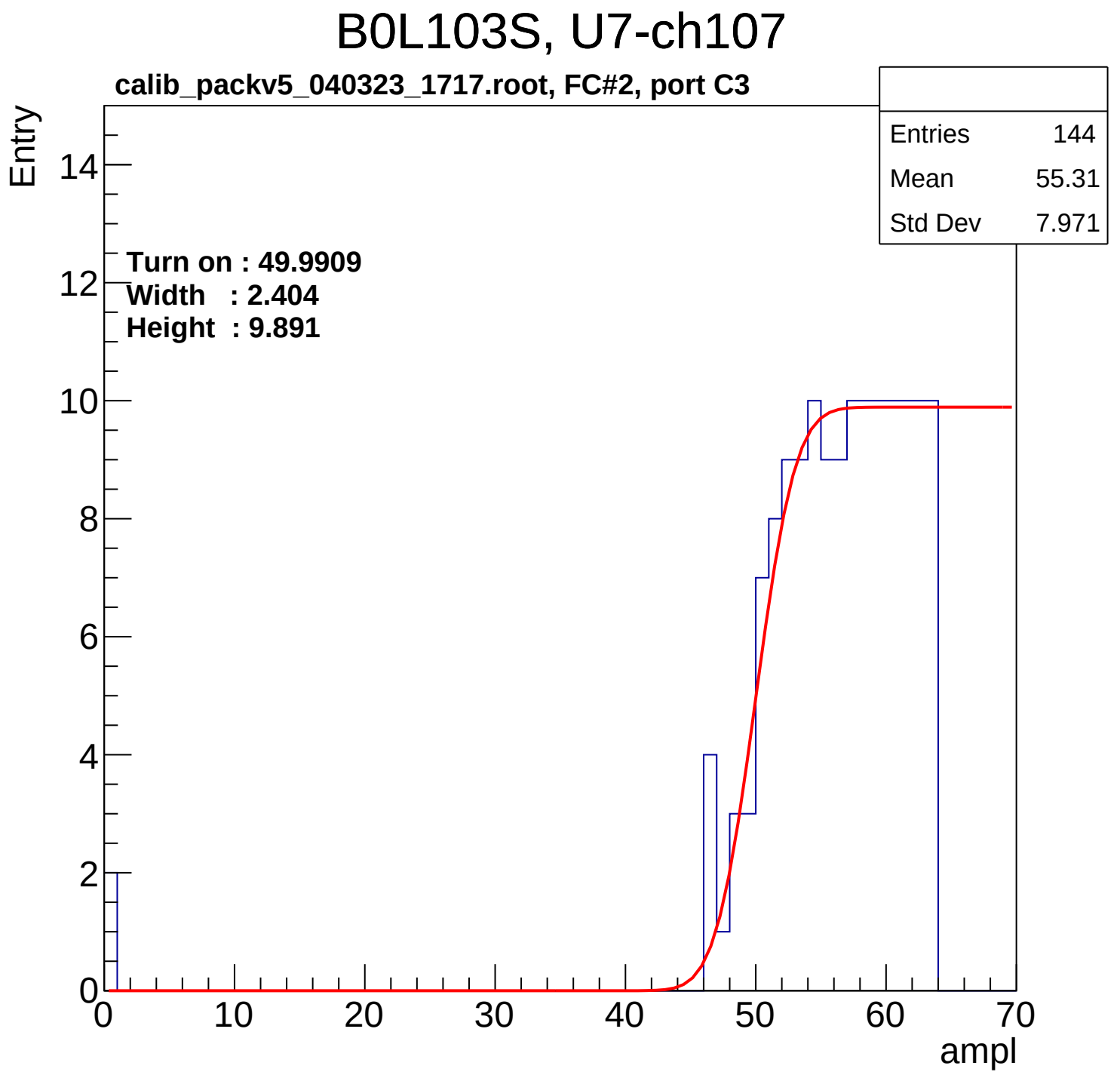
B0L103S, U7-ch107
calib_packv5_040323_1717.root, FC#2, port C3
Entries 144
Mean 55.31
Std Dev 7.971
Turn on : 49.9909
Width : 2.404
Height : 9.891
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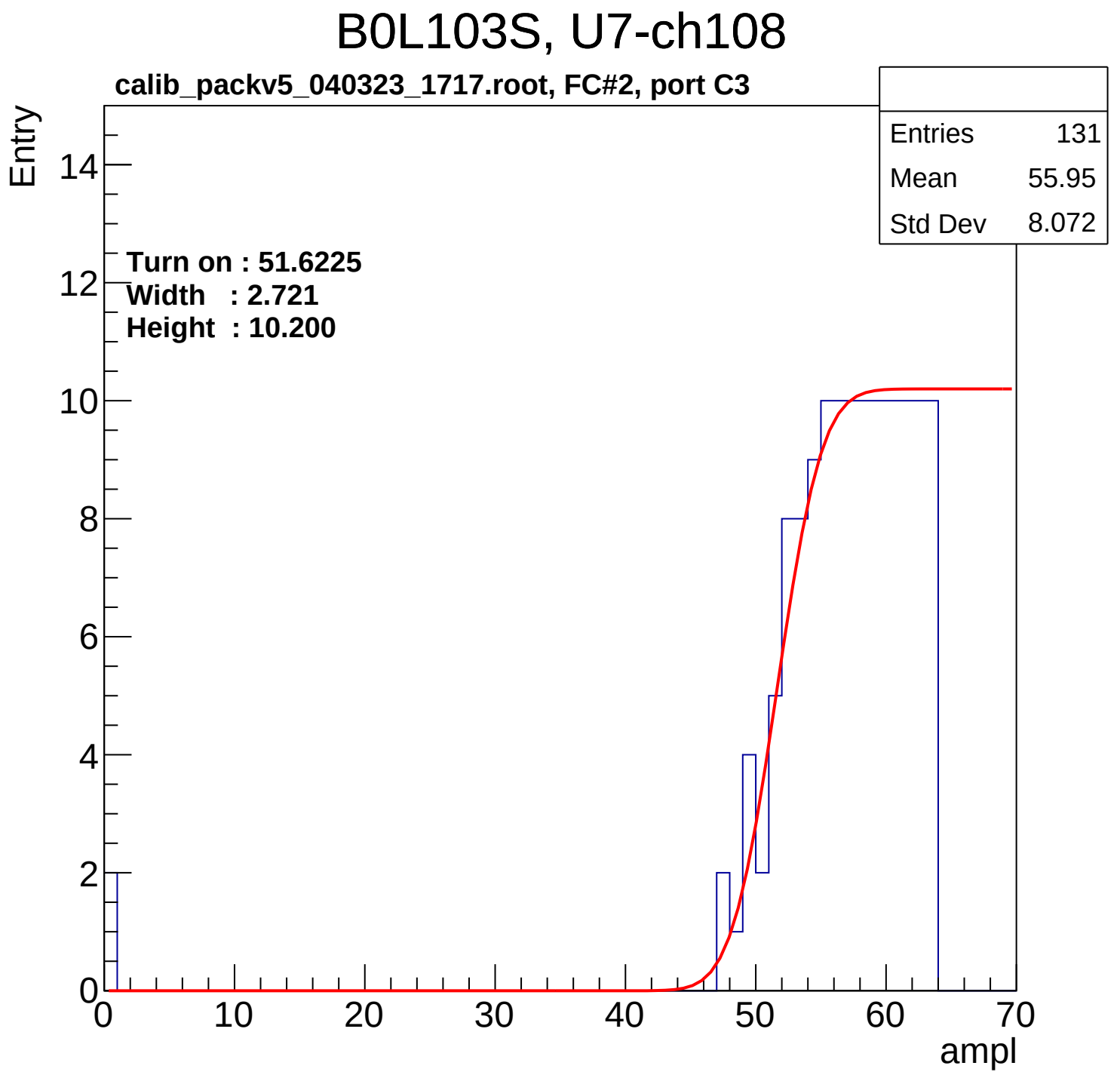
B0L103S, U7-ch108
calib_packv5_040323_1717.root, FC#2, port C3
Entries 131
Mean 55.95
Std Dev 8.072
Turn on : 51.6225
Width : 2.721
Height : 10.200
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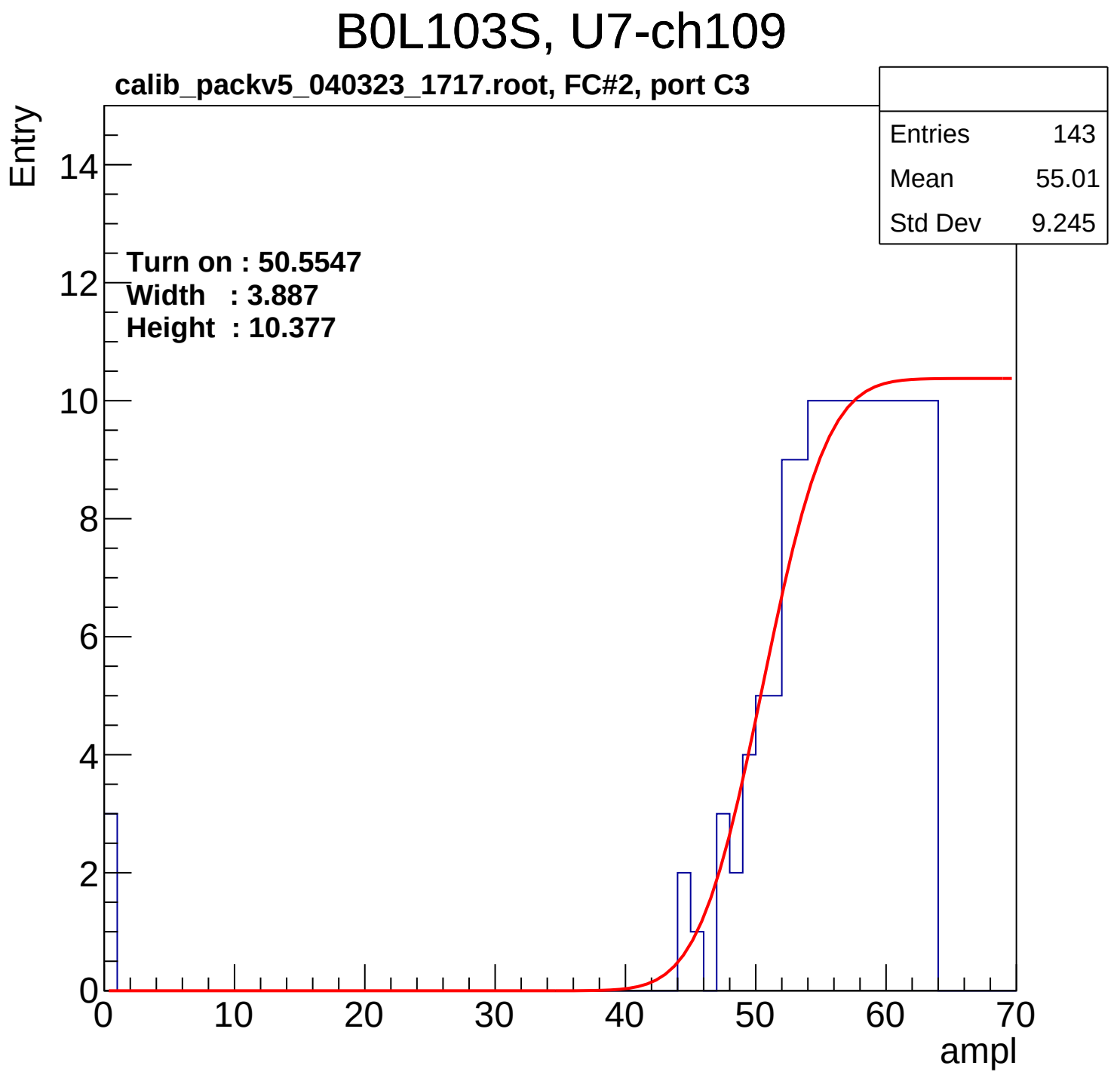
B0L103S, U7-ch109
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 55.01
Std Dev 9.245
Turn on : 50.5547
Width : 3.887
Height : 10.377
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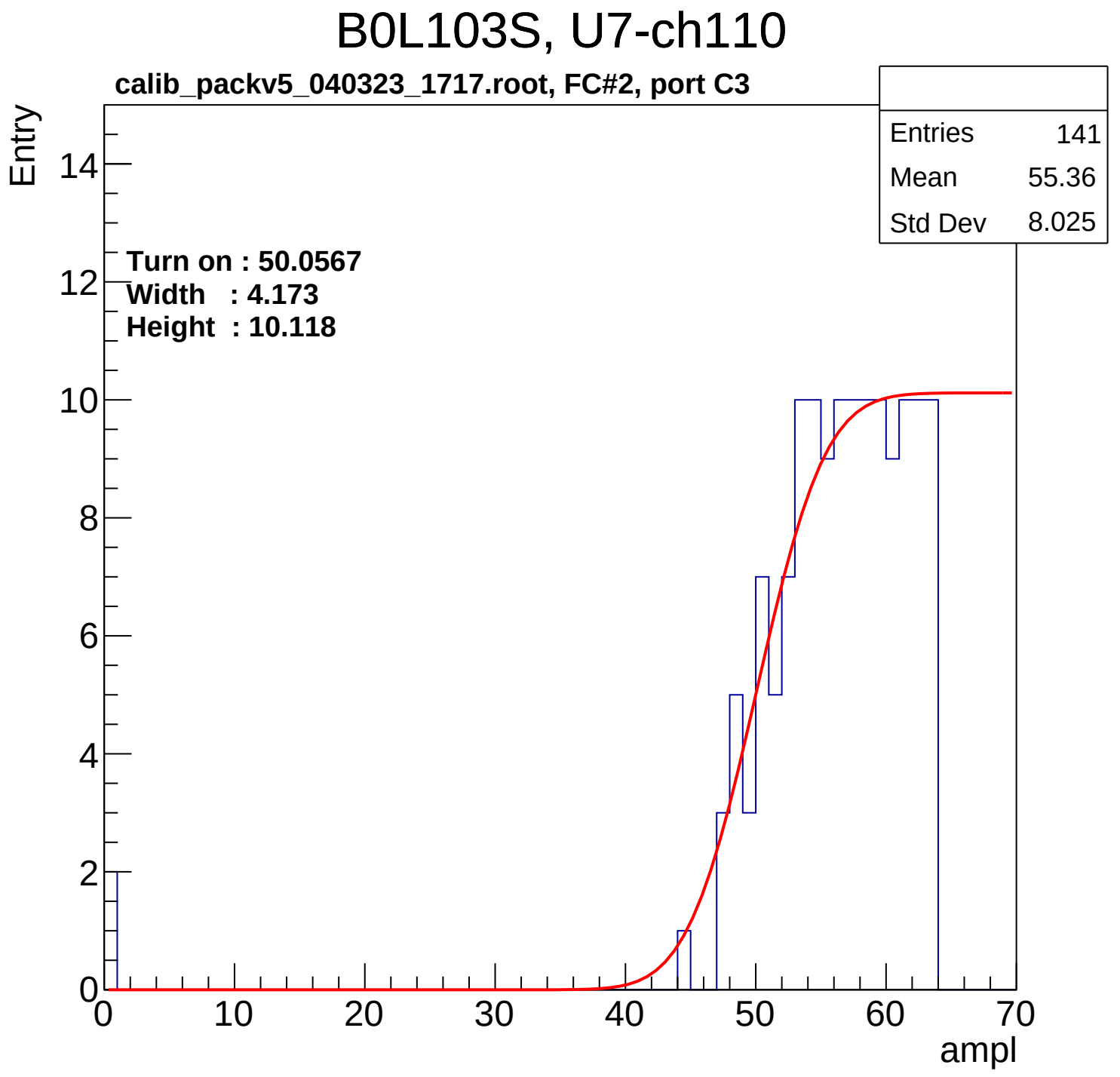
B0L103S, U7-ch110
calib_packv5_040323_1717.root, FC#2, port C3
Entries 141
Mean 55.36
Std Dev 8.025
Turn on : 50.0567
Width : 4.173
Height : 10.118
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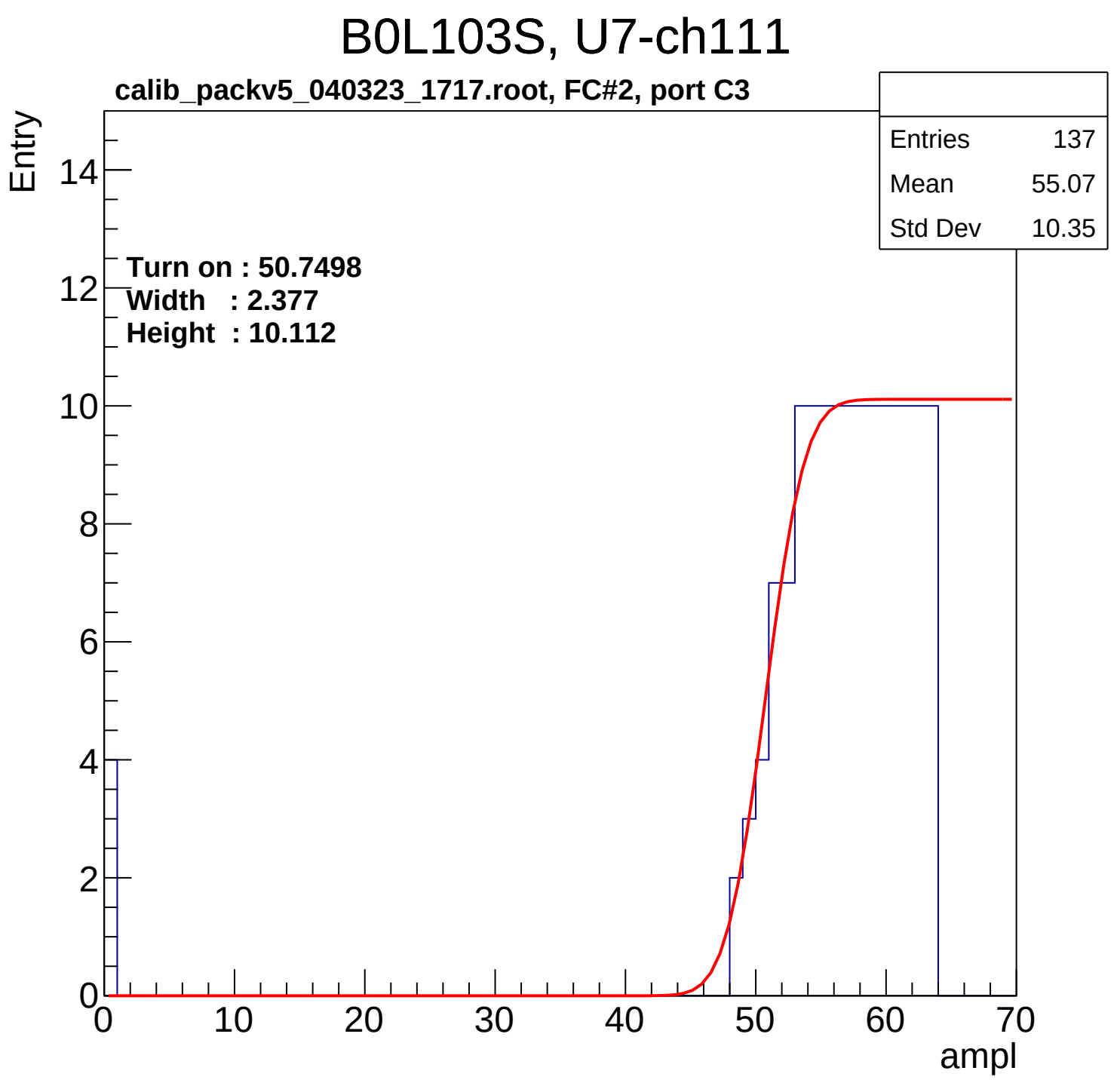
B0L103S, U7-ch111
calib_packv5_040323_1717.root, FC#2, port C3
Entries 137
Mean 55.07
Std Dev 10.35
Turn on : 50.7498
Width : 2.377
Height : 10.112
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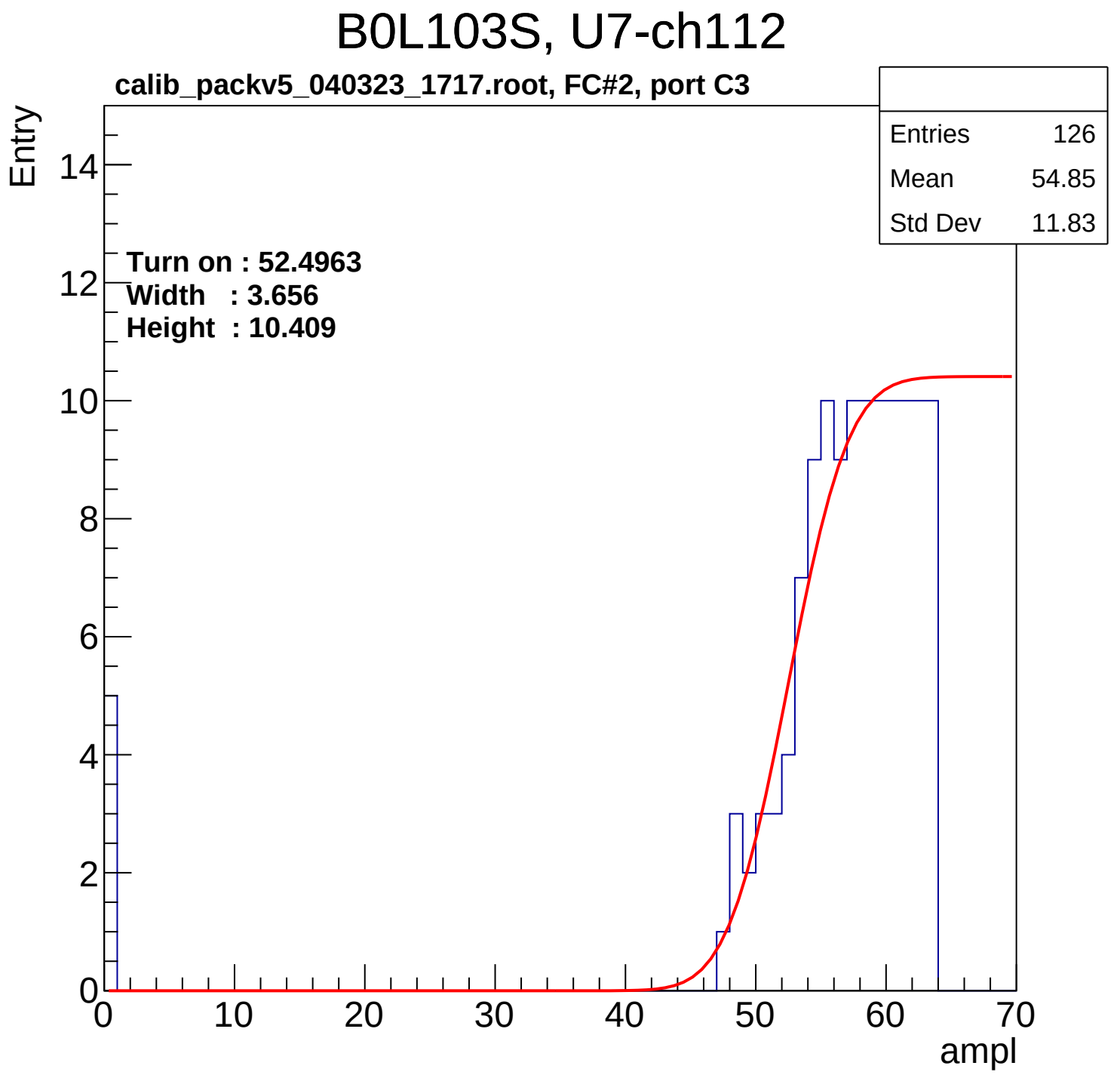
B0L103S, U7-ch112
calib_packv5_040323_1717.root, FC#2, port C3
Entries 126
Mean 54.85
Std Dev 11.83
Turn on : 52.4963
Width : 3.656
Height : 10.409
Entry
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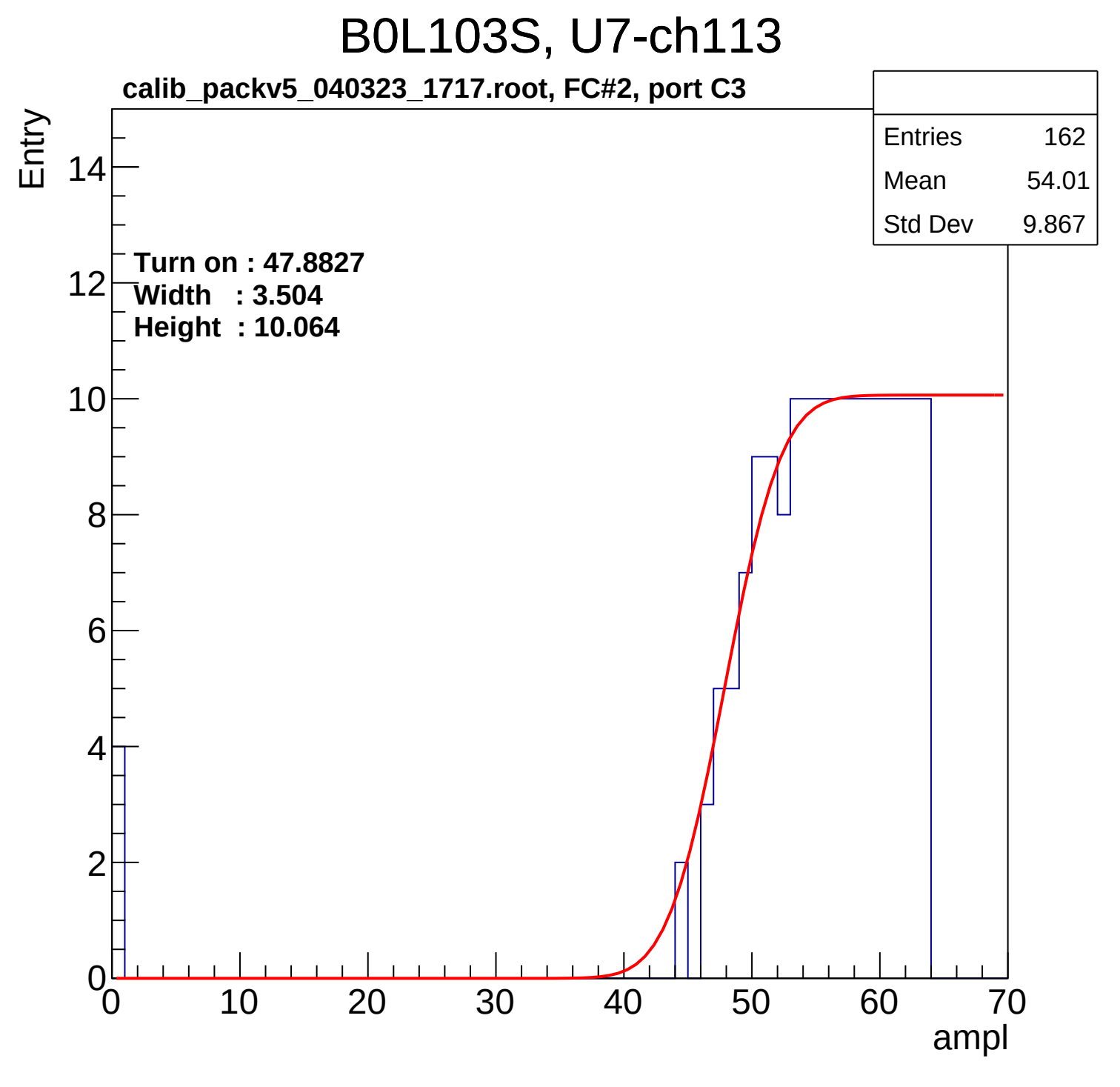
B0L103S, U7-ch113
calib_packv5_040323_1717.root, FC#2, port C3
Entries 162
Mean 54.01
Std Dev 9.867
Turn on : 47.8827
Width : 3.504
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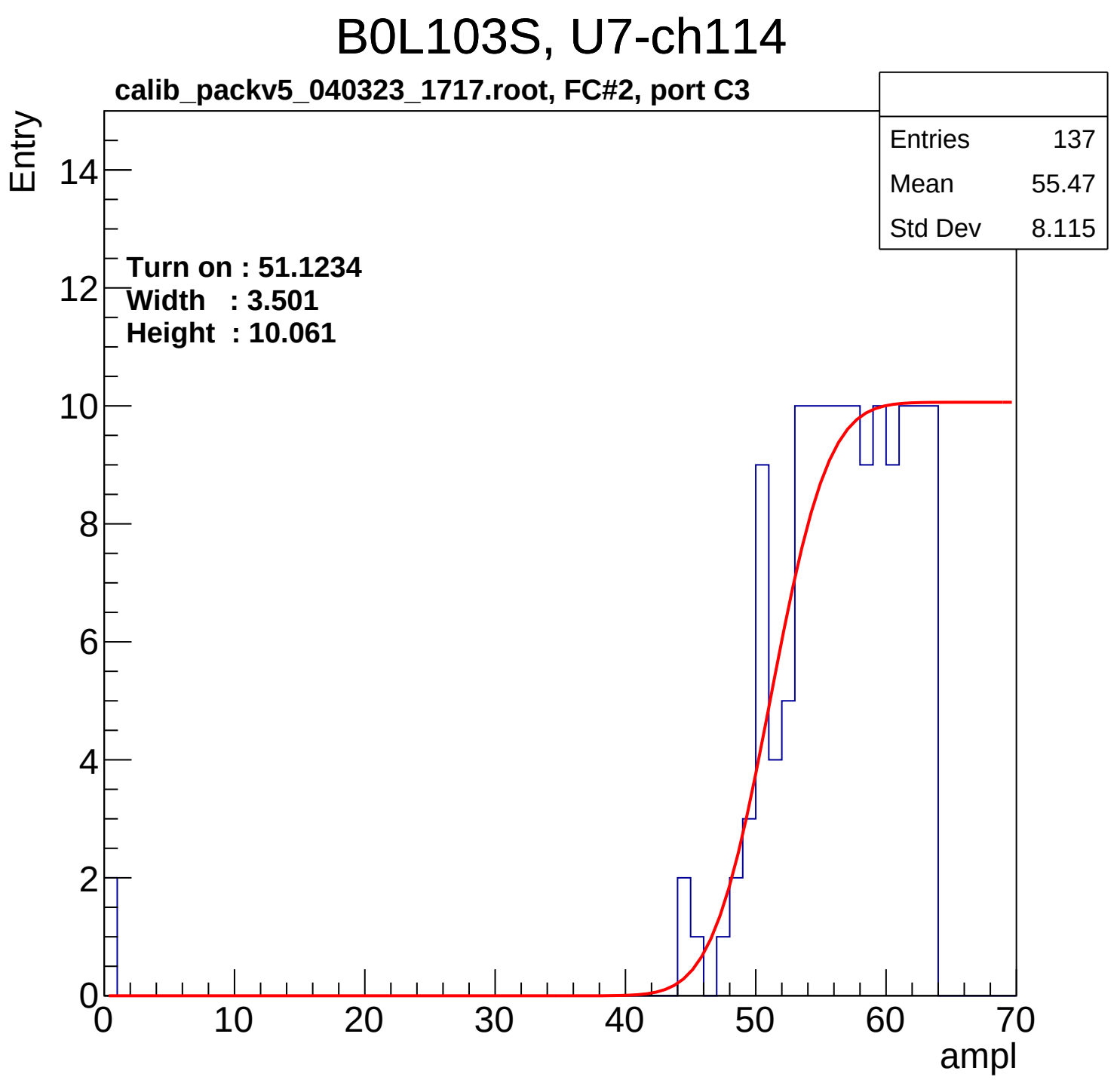
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calib_packv5_040323_1717.root, FC#2, port C3
Entries 137
Mean 55.47
Std Dev 8.115
Turn on : 51.1234
Width : 3.501
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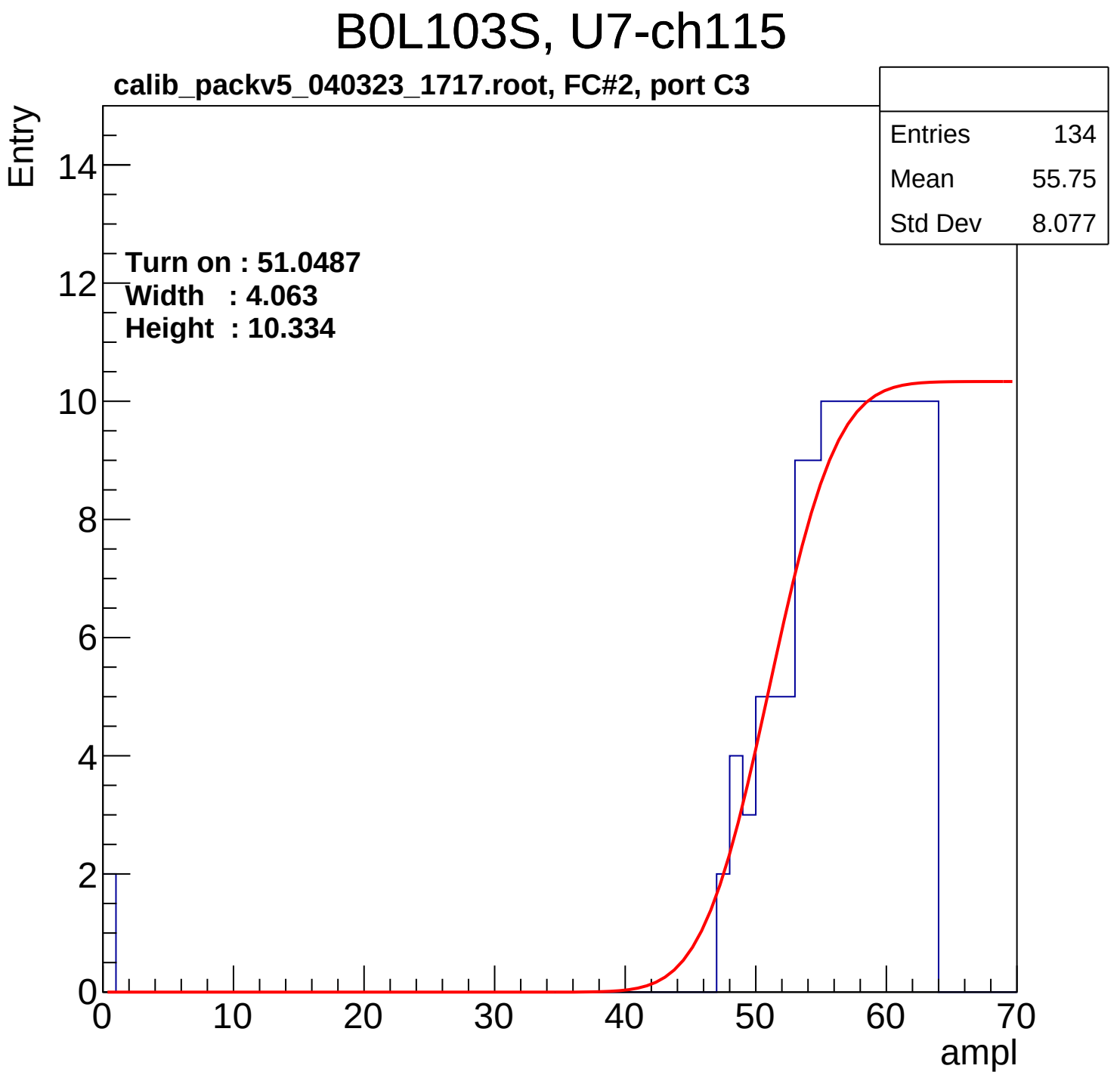
B0L103S, U7-ch115
calib_packv5_040323_1717.root, FC#2, port C3
Entries 134
Mean 55.75
Std Dev 8.077
Turn on : 51.0487
Width : 4.063
Height : 10.334
Entry
ampl
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4
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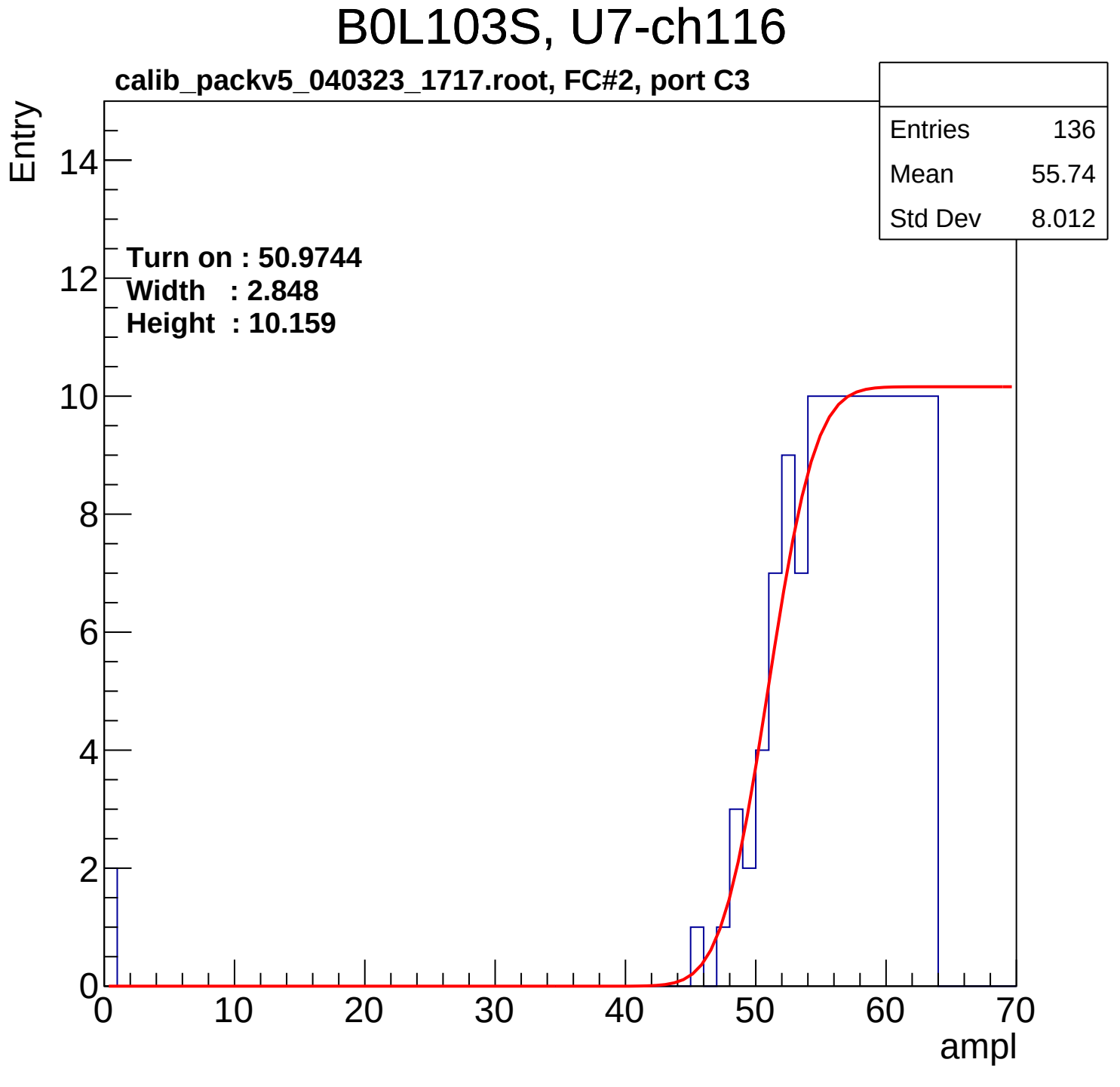
B0L103S, U7-ch116
calib_packv5_040323_1717.root, FC#2, port C3
Entries 136
Mean 55.74
Std Dev 8.012
Turn on : 50.9744
Width : 2.848
Height : 10.159
Entry
ampl
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2
4
6
8
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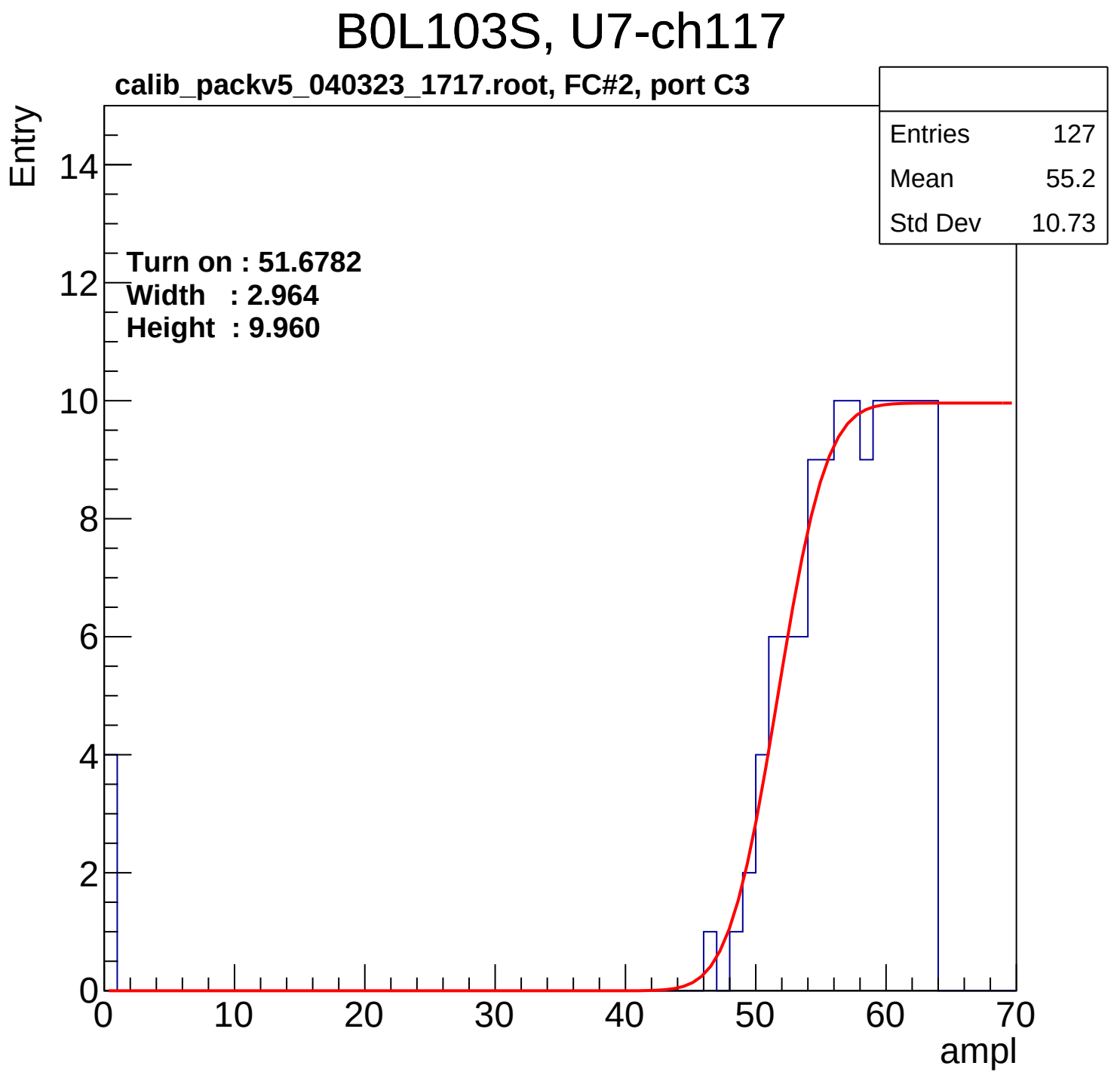
B0L103S, U7-ch117
calib_packv5_040323_1717.root, FC#2, port C3
Entries 127
Mean 55.2
Std Dev 10.73
Turn on : 51.6782
Width : 2.964
Height : 9.960
Entry
ampl
0
2
4
6
8
10
12
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10
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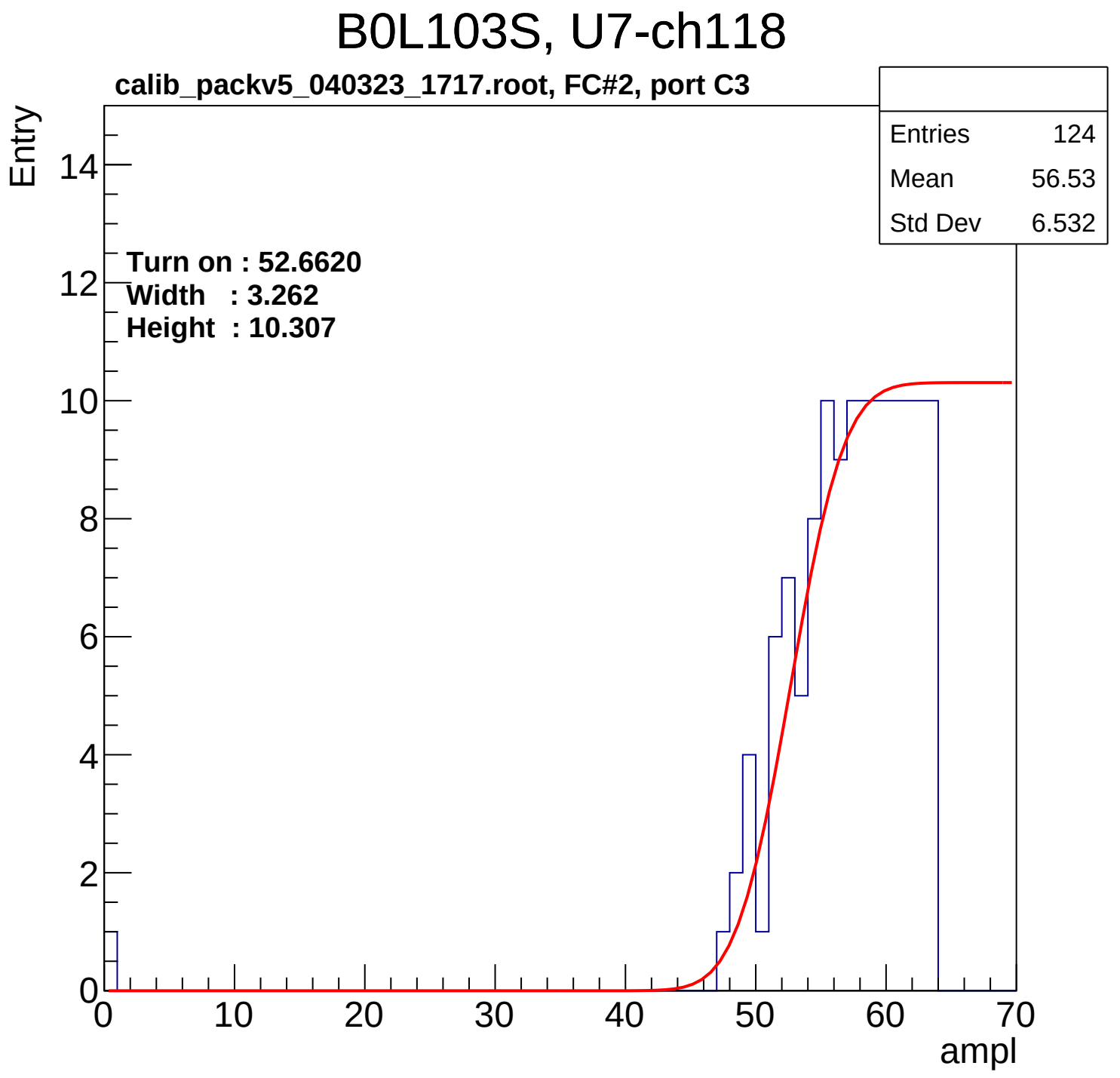
B0L103S, U7-ch118
calib_packv5_040323_1717.root, FC#2, port C3
Entries 124
Mean 56.53
Std Dev 6.532
Turn on : 52.6620
Width : 3.262
Height : 10.307
Entry
ampl
0
2
4
6
8
10
12
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0
10
20
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40
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60
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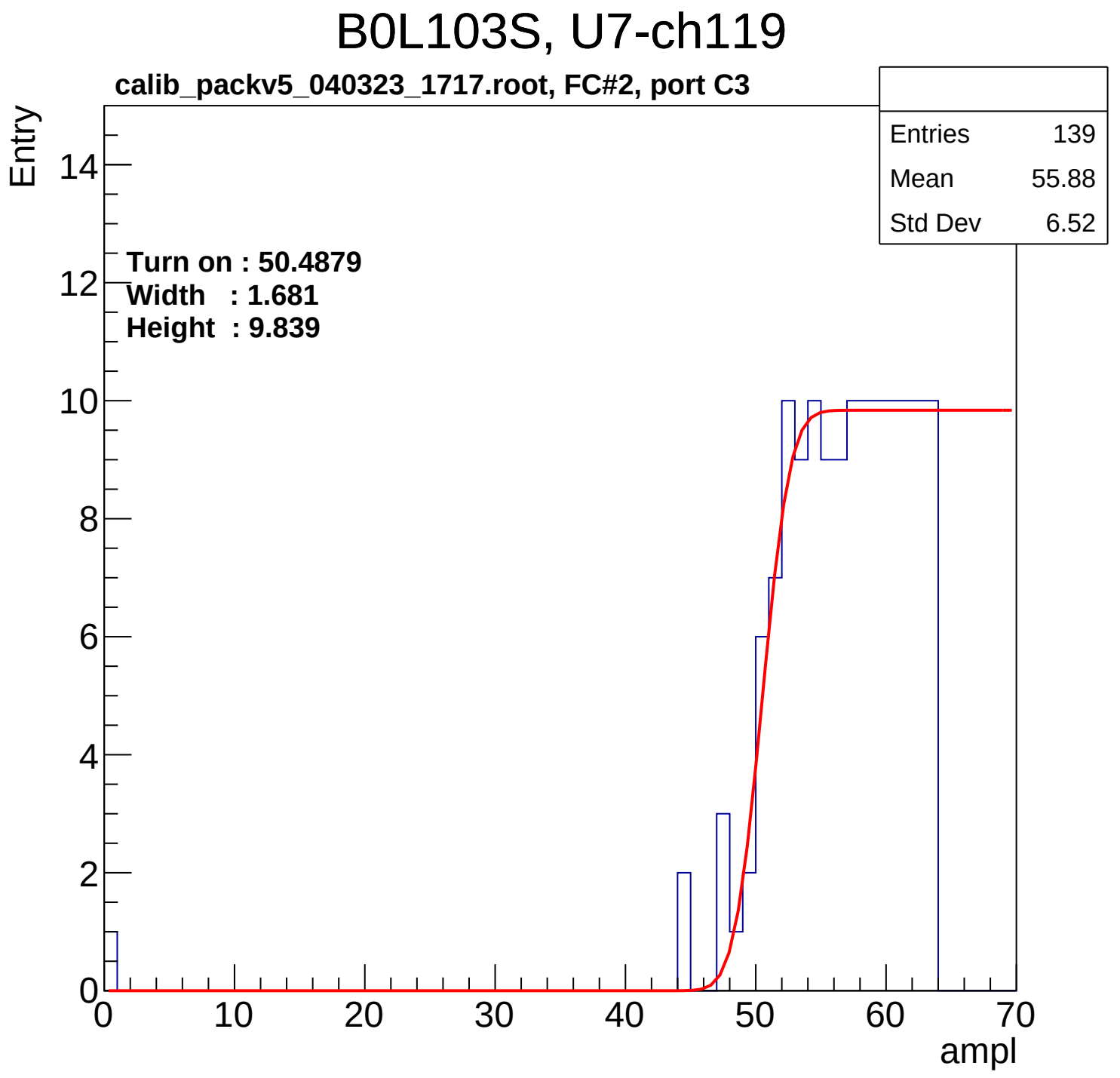
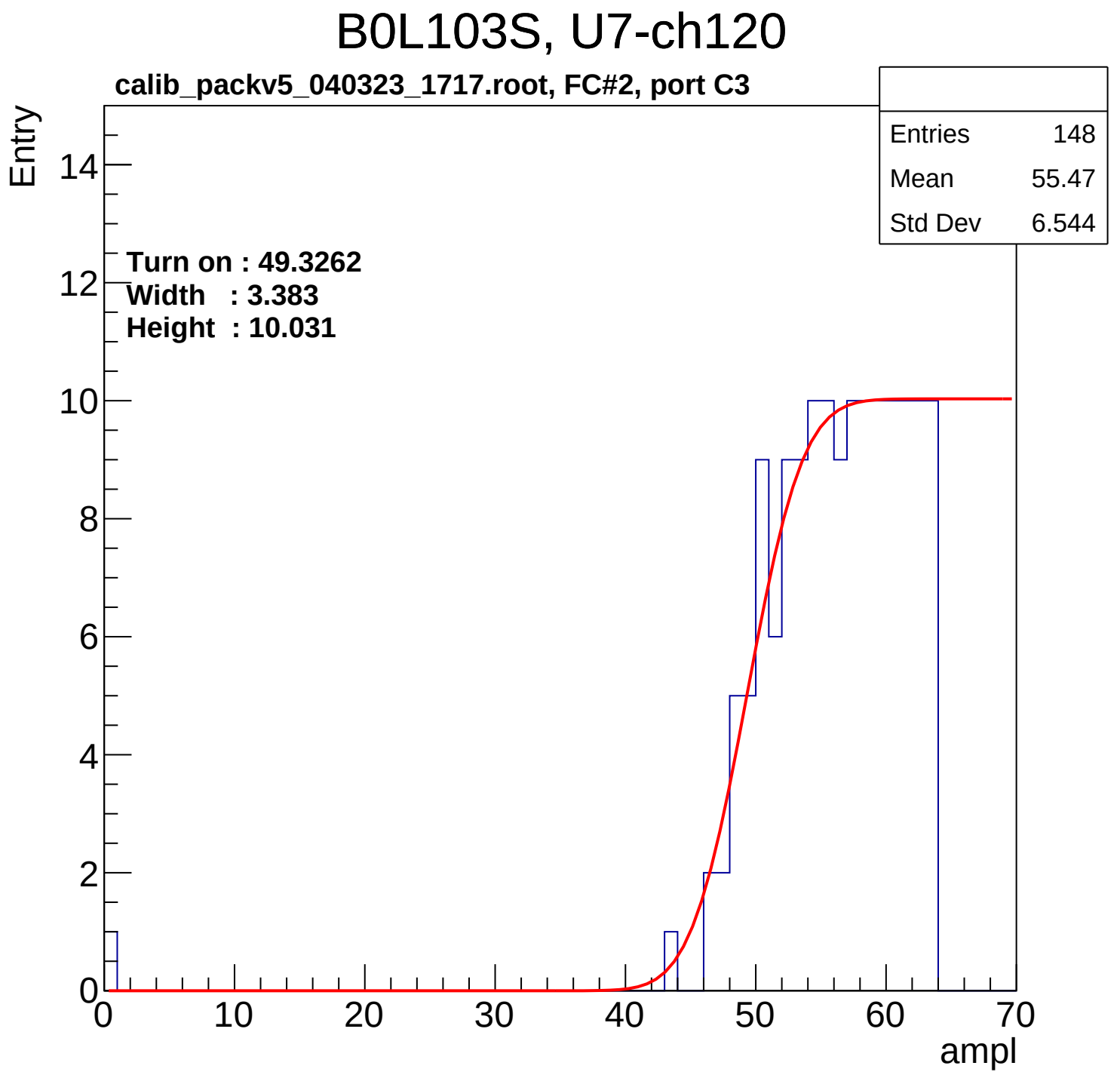

B0L103S, U7-ch119
calib_packv5_040323_1717.root, FC#2, port C3
Entries 139
Mean 55.88
Std Dev 6.52
Turn on : 50.4879
Width : 1.681
Height : 9.839
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L103S, U7-ch120
calib_packv5_040323_1717.root, FC#2, port C3
Entries 148
Mean 55.47
Std Dev 6.544
Turn on : 49.3262
Width : 3.383
Height : 10.031
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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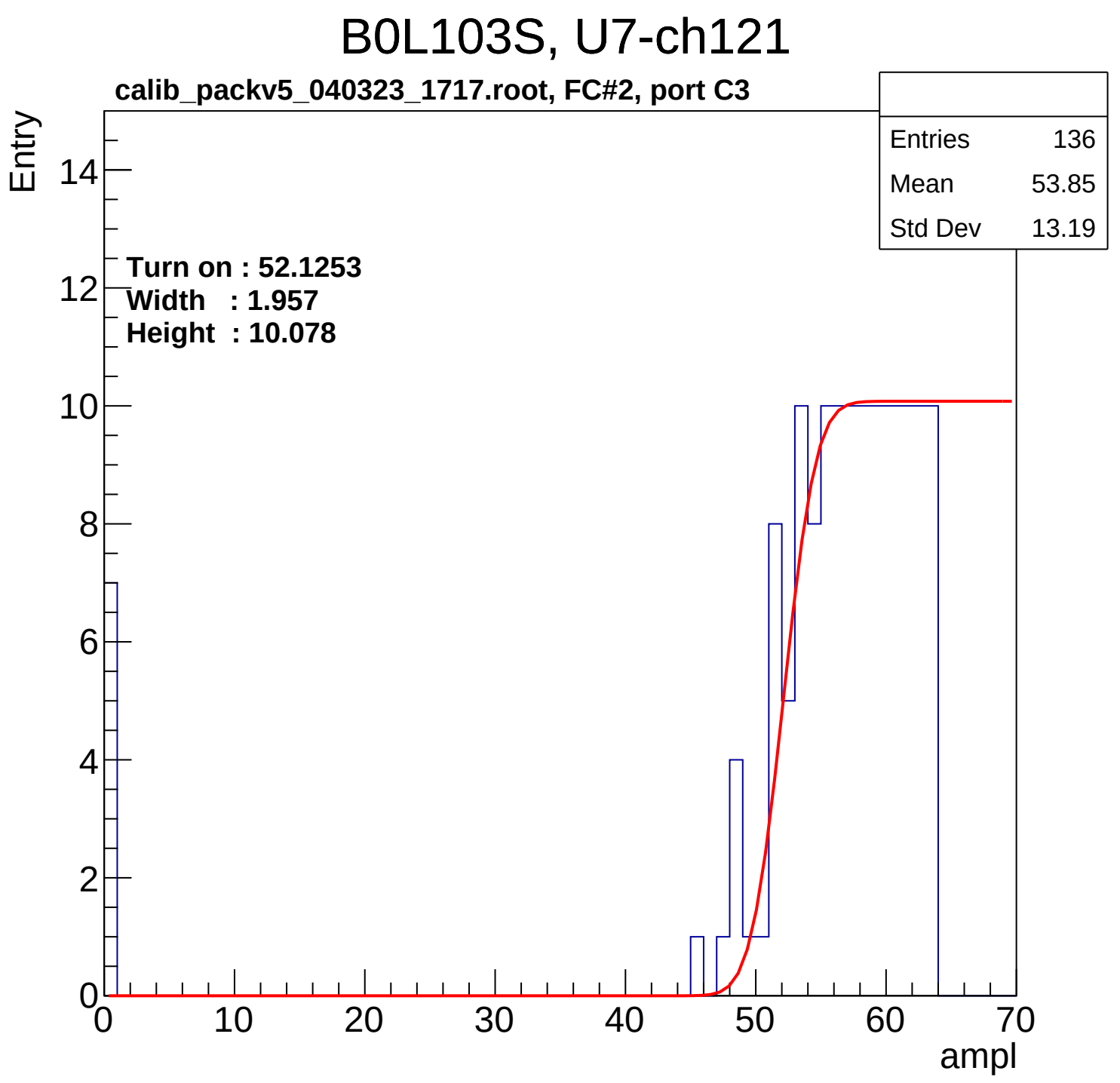
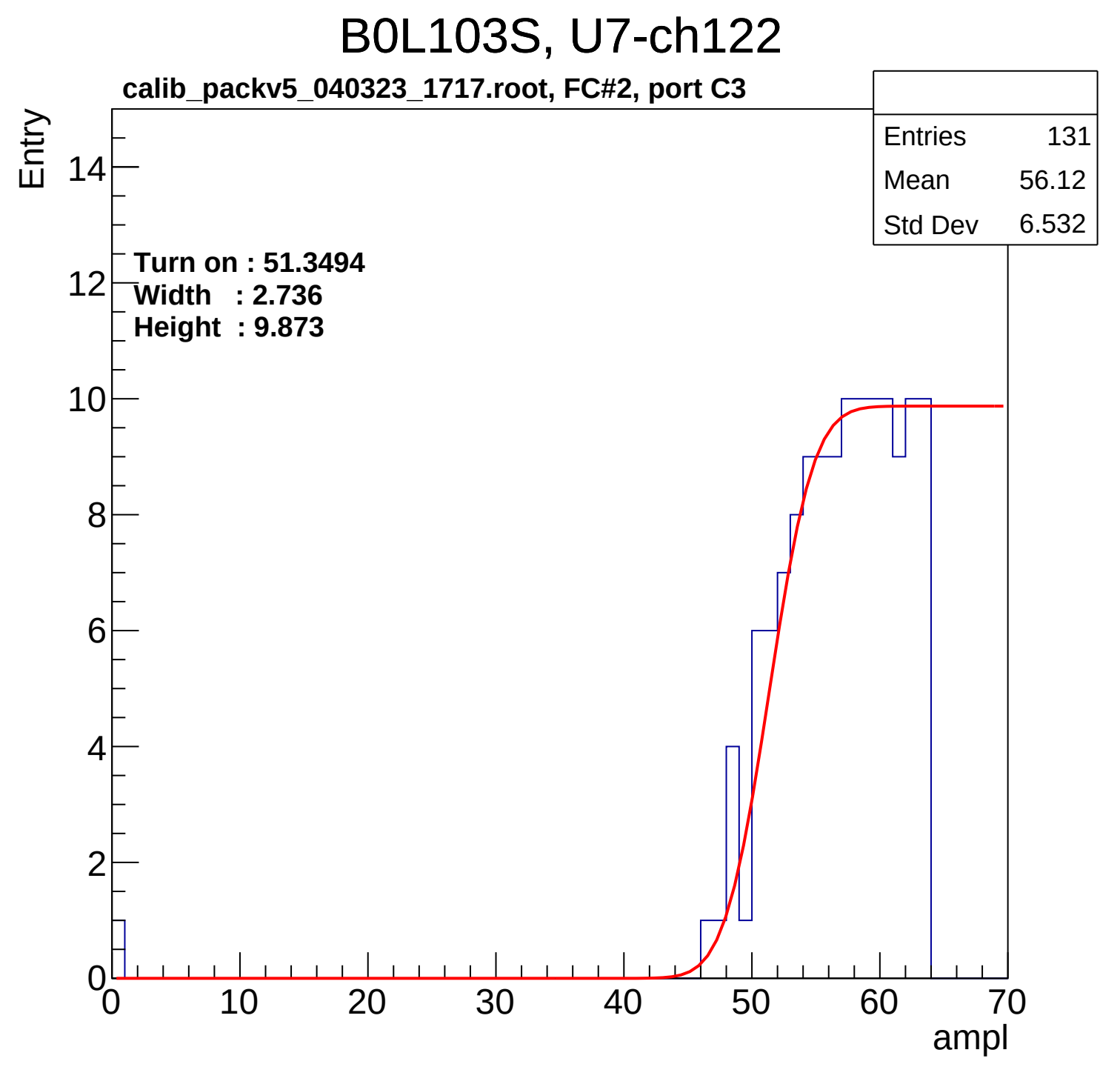

B0L103S, U7-ch121
calib_packv5_040323_1717.root, FC#2, port C3
Entries 136
Mean 53.85
Std Dev 13.19
Turn on : 52.1253
Width : 1.957
Height : 10.078
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L103S, U7-ch122
calib_packv5_040323_1717.root, FC#2, port C3
Entries 131
Mean 56.12
Std Dev 6.532
Turn on : 51.3494
Width : 2.736
Height : 9.873
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
30
40
50
60
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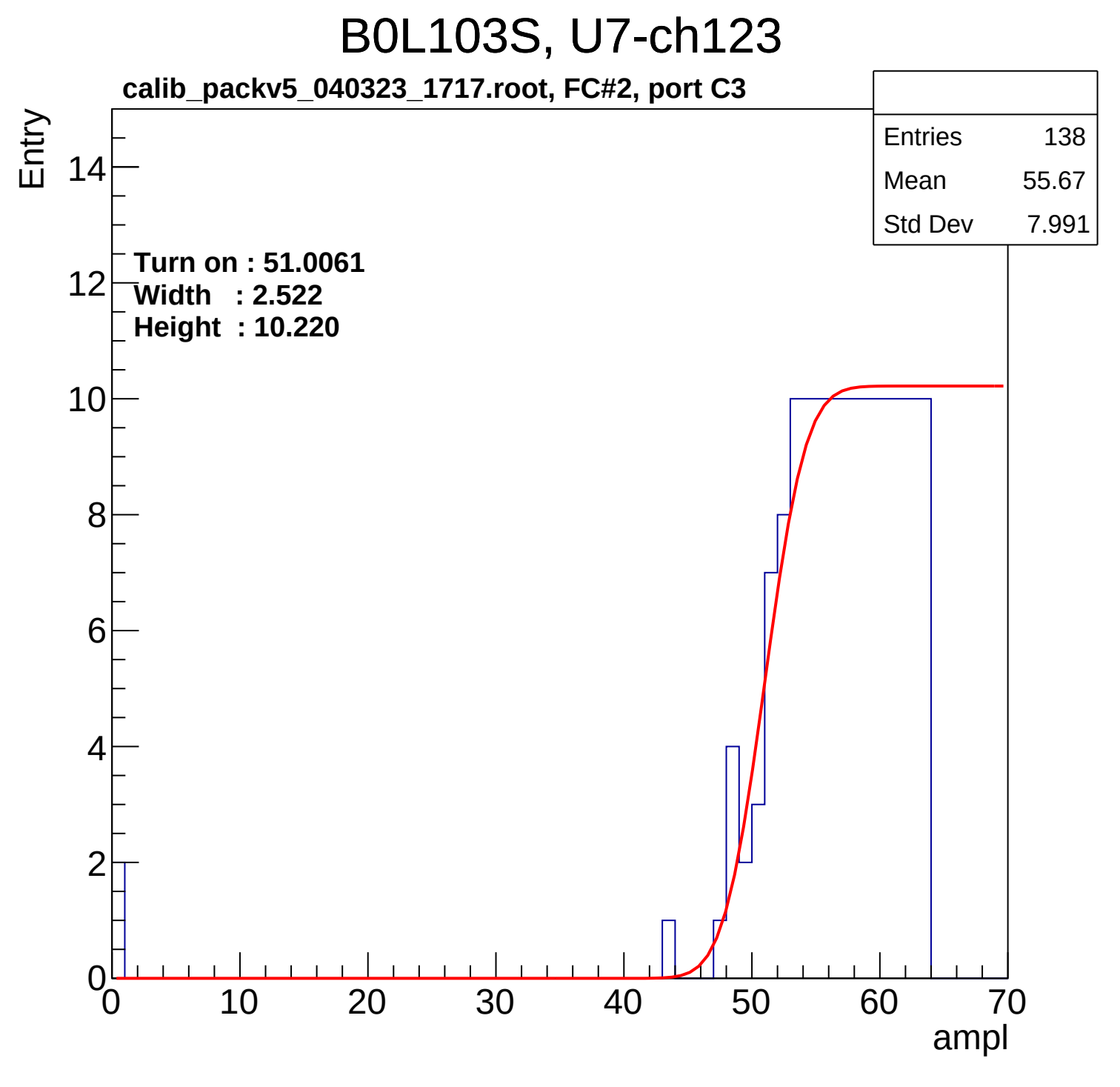
B0L103S, U7-ch123
calib_packv5_040323_1717.root, FC#2, port C3
Entries 138
Mean 55.67
Std Dev 7.991
Turn on : 51.0061
Width : 2.522
Height : 10.220
Entry
ampl
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2
4
6
8
10
12
14
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10
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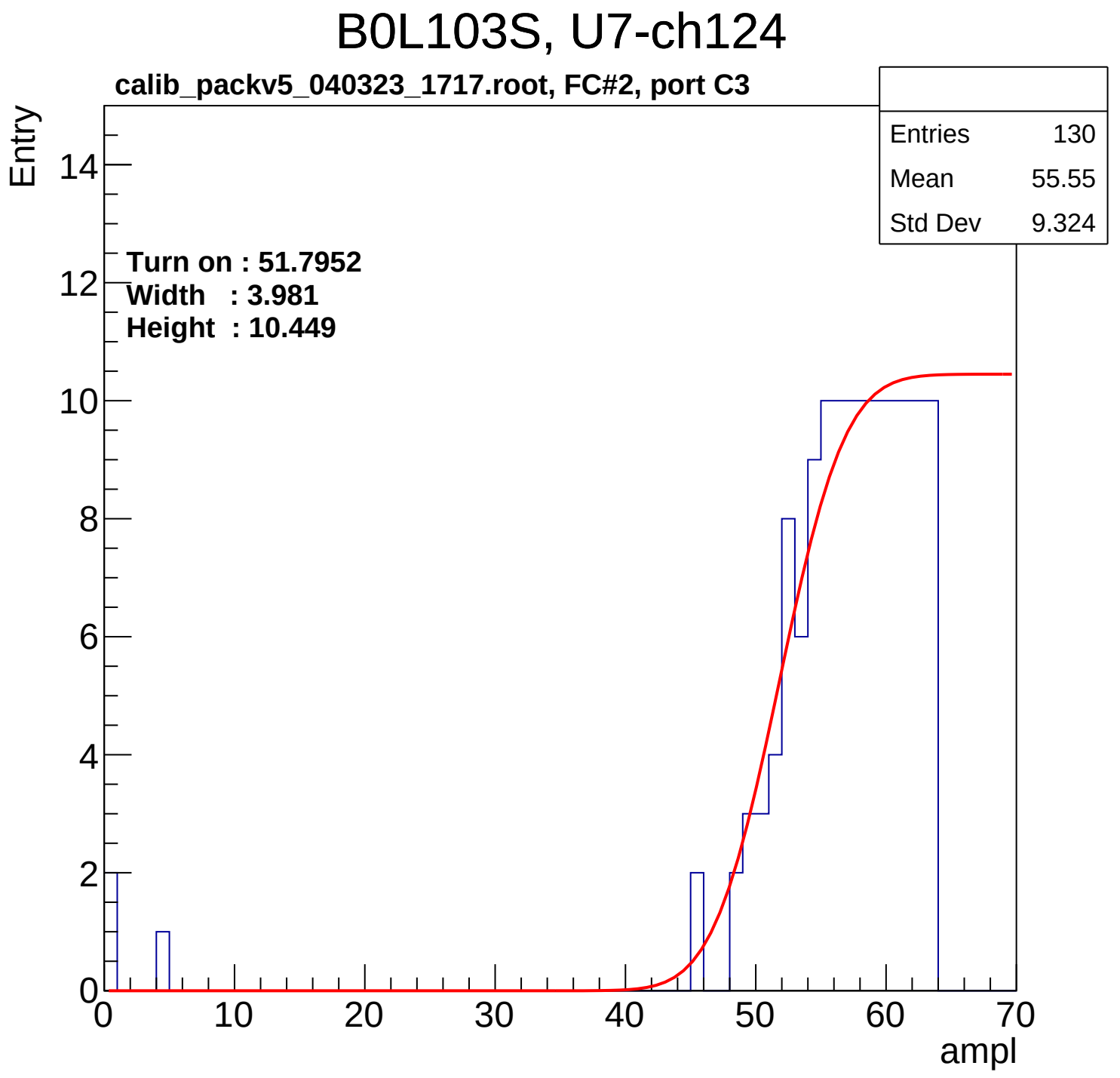
B0L103S, U7-ch124
calib_packv5_040323_1717.root, FC#2, port C3
Entries 130
Mean 55.55
Std Dev 9.324
Turn on : 51.7952
Width : 3.981
Height : 10.449
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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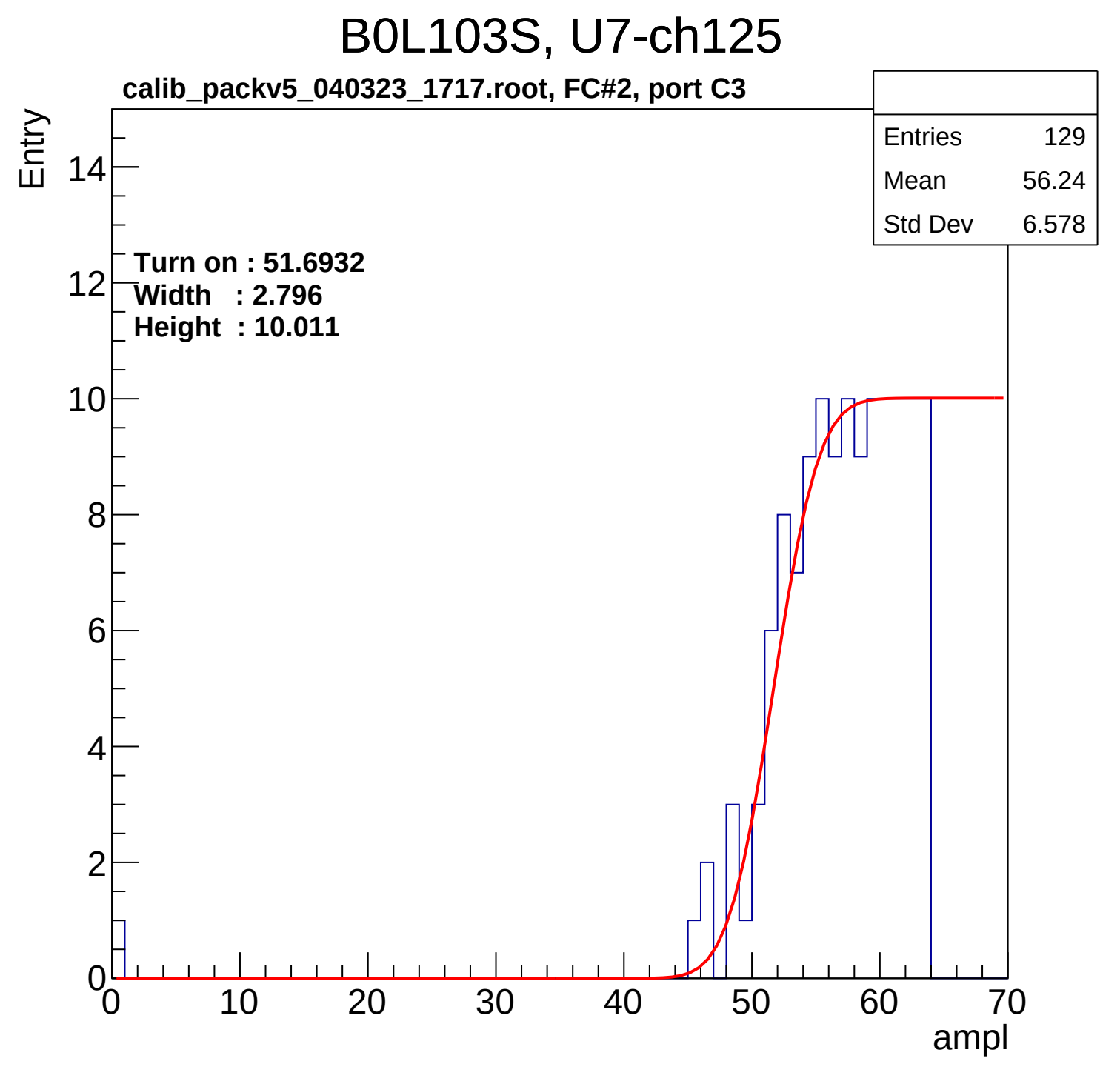
B0L103S, U7-ch125
calib_packv5_040323_1717.root, FC#2, port C3
Entries 129
Mean 56.24
Std Dev 6.578
Turn on : 51.6932
Width : 2.796
Height : 10.011
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
50
60
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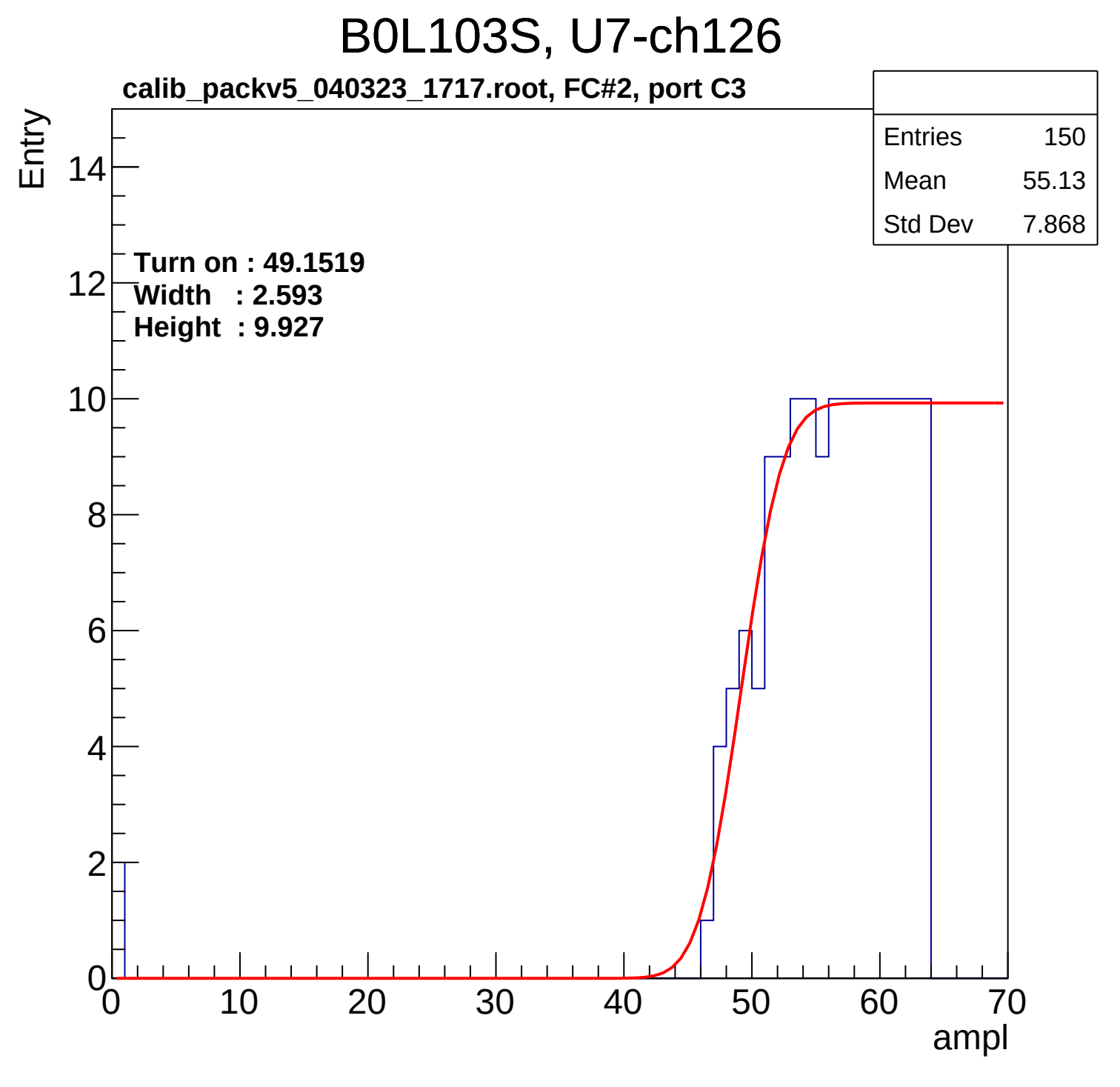
B0L103S, U7-ch126
calib_packv5_040323_1717.root, FC#2, port C3
Entries 150
Mean 55.13
Std Dev 7.868
Turn on : 49.1519
Width : 2.593
Height : 9.927
Entry
ampl
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2
4
6
8
10
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0
10
20
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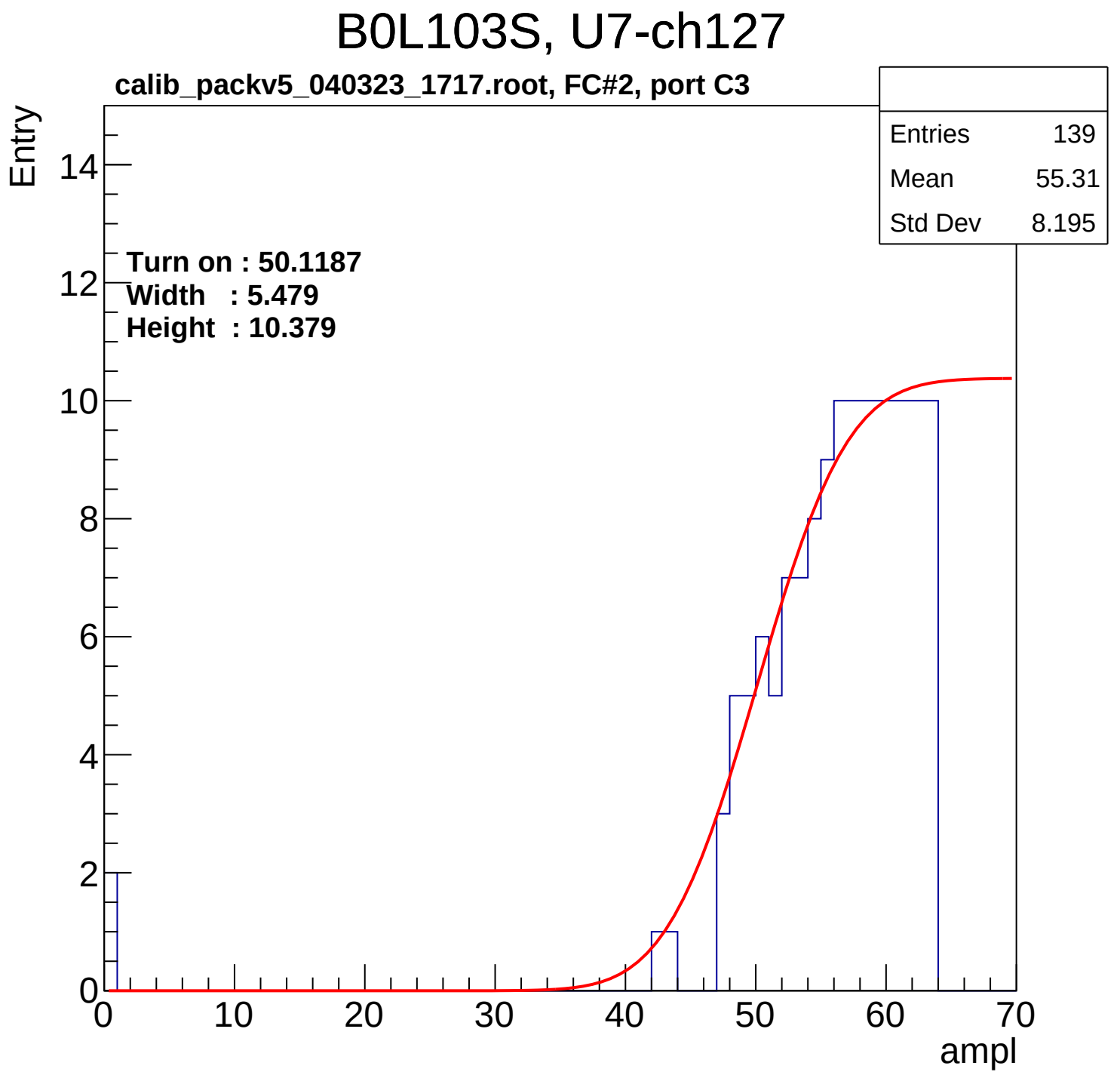
B0L103S, U7-ch127
calib_packv5_040323_1717.root, FC#2, port C3
Entries 139
Mean 55.31
Std Dev 8.195
Turn on : 50.1187
Width : 5.479
Height : 10.379
Entry
ampl
0
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8
10
12
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0
10
20
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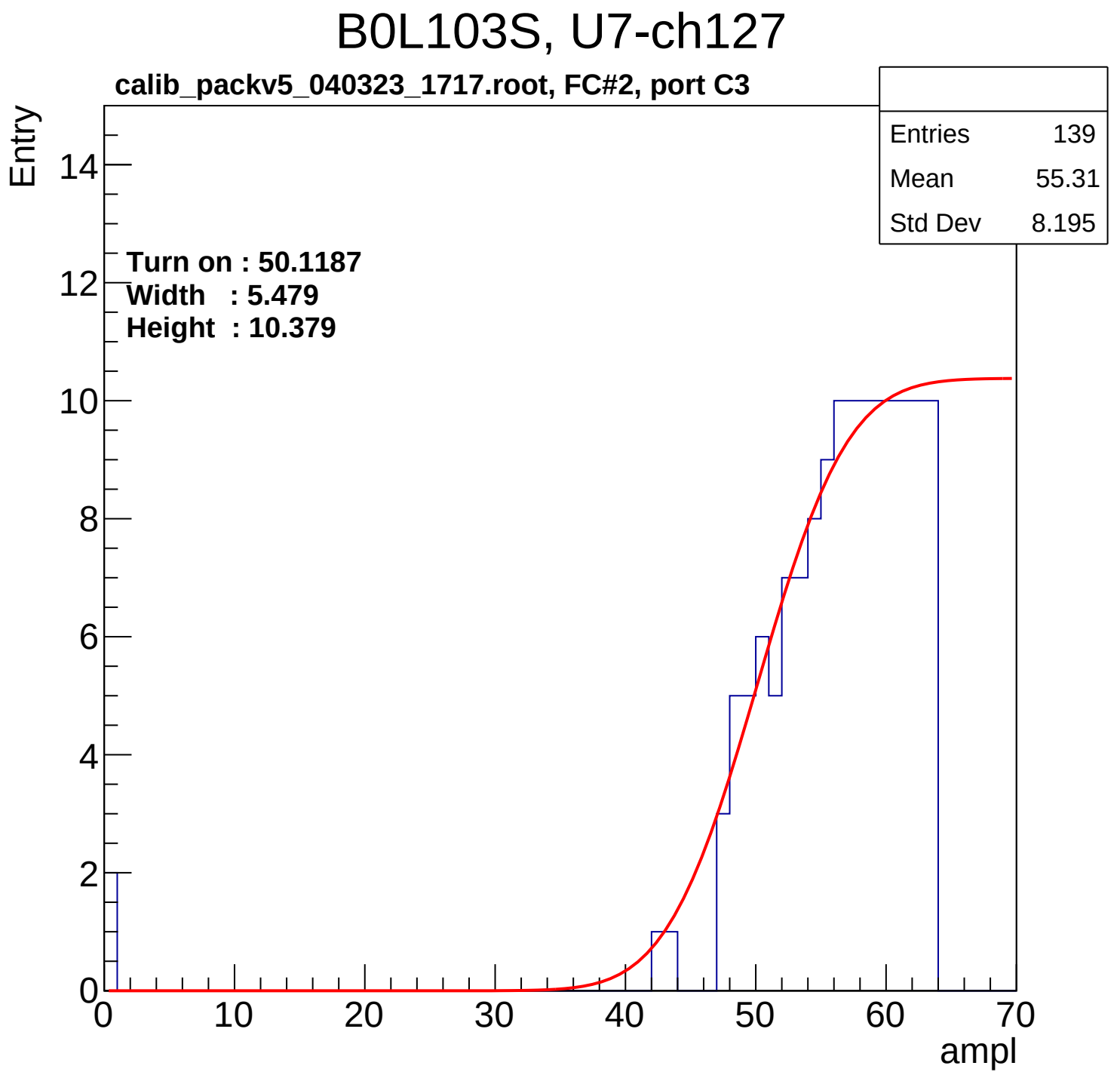
B0L103S, U7-ch127
calib_packv5_040323_1717.root, FC#2, port C3
Entries 139
Mean 55.31
Std Dev 8.195
Turn on : 50.1187
Width : 5.479
Height : 10.379
Entry
ampl
0
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10
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14
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