

B1L100S, U5-ch0

calib_packv5_042523_0143.root, FC#4, port A2

Entries	375
Mean	44.45
Std Dev	11.56

Turn on : 26.6851

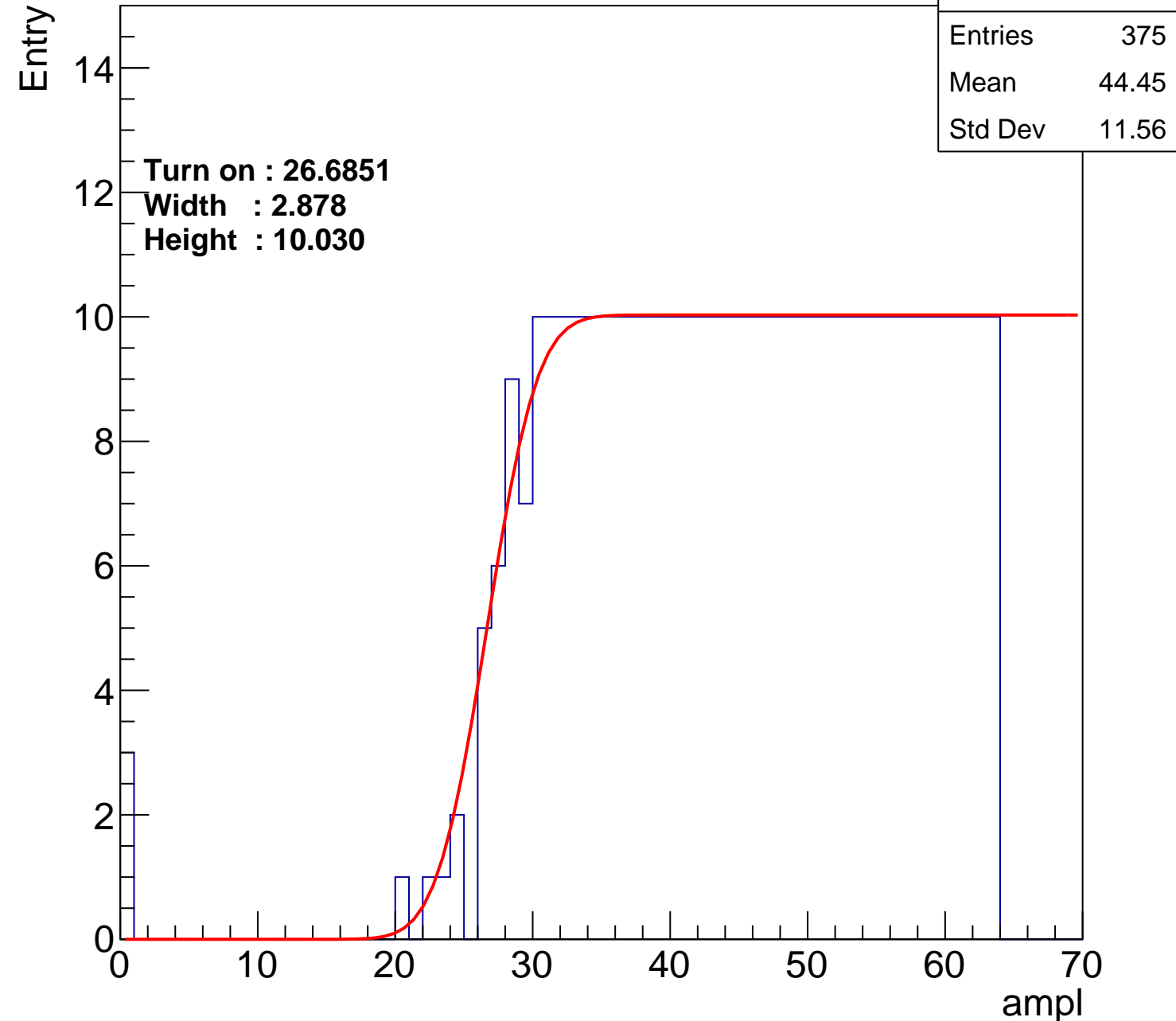
Width : 2.878

Height : 10.030

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch1

calib_packv5_042523_0143.root, FC#4, port A2

Entries	390
Mean	43.83
Std Dev	11.61

Turn on : 25.5148

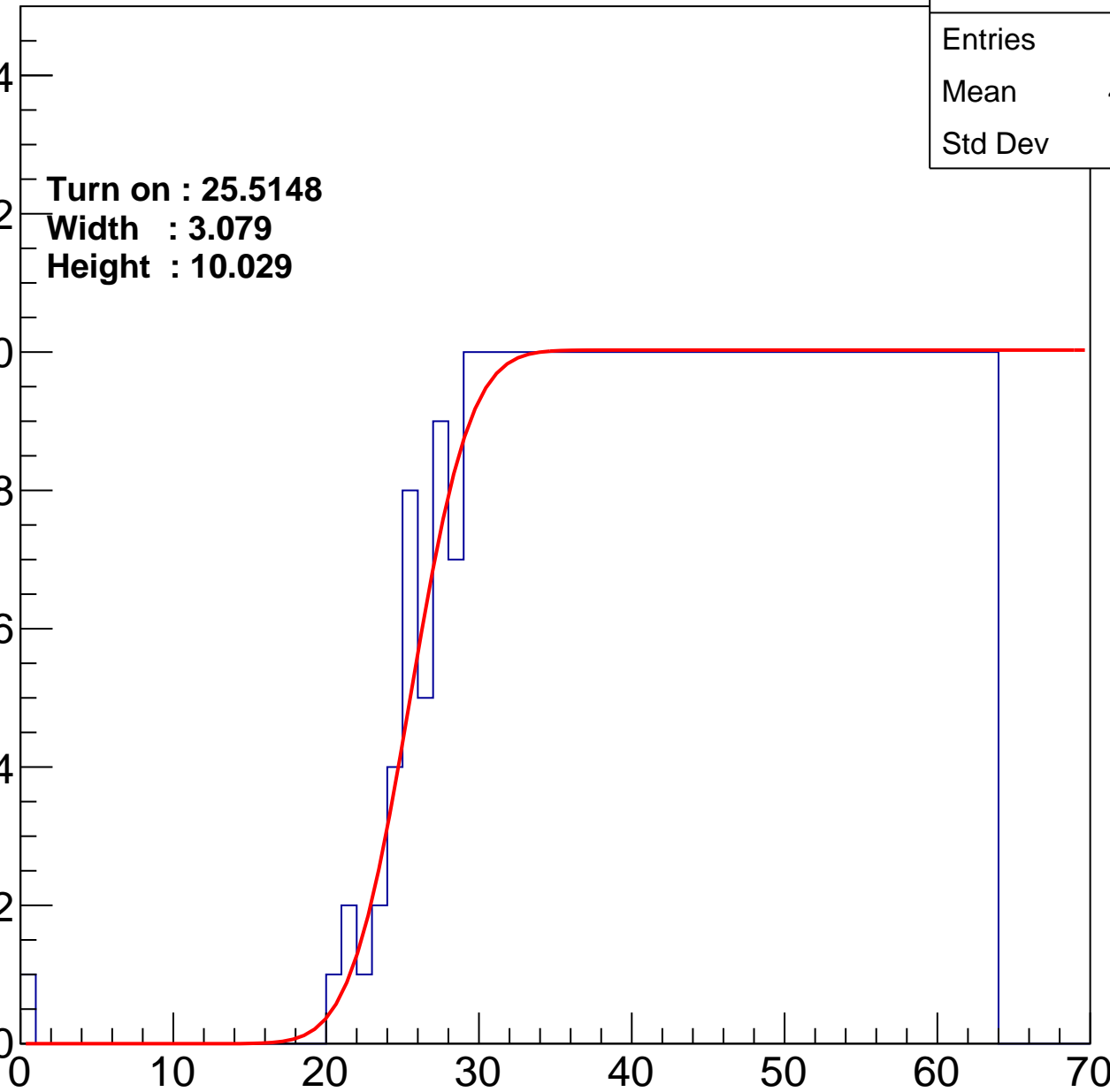
Width : 3.079

Height : 10.029

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch2

calib_packv5_042523_0143.root, FC#4, port A2

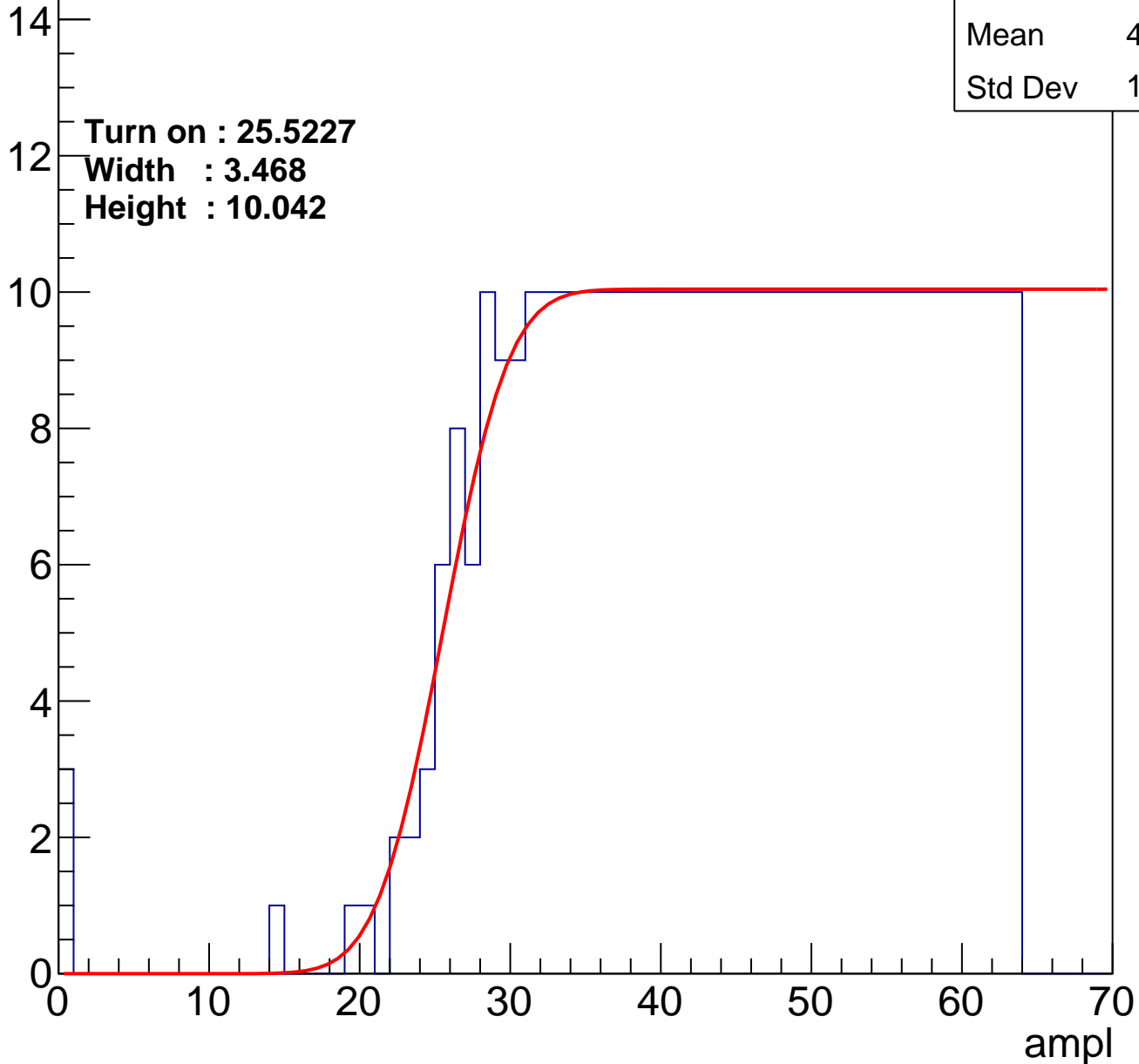
Entries	391
Mean	43.62
Std Dev	12.04

Turn on : 25.5227

Width : 3.468

Height : 10.042

Entry



B1L100S, U5-ch3

calib_packv5_042523_0143.root, FC#4, port A2

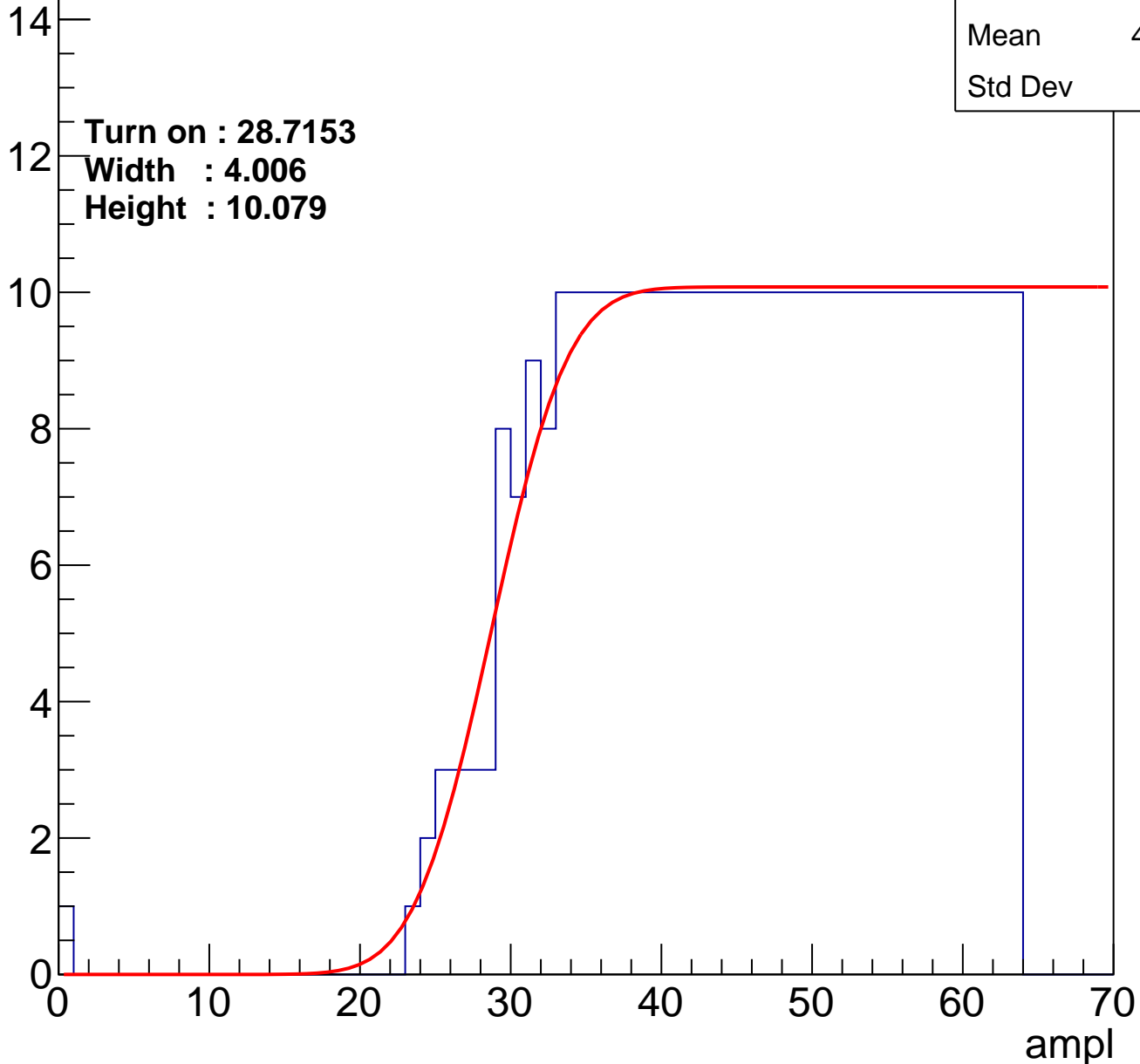
Entries	358
Mean	45.38
Std Dev	10.8

Turn on : 28.7153

Width : 4.006

Height : 10.079

Entry



B1L100S, U5-ch4

calib_packv5_042523_0143.root, FC#4, port A2

Entries	385
Mean	44
Std Dev	11.68

Turn on : 25.9509

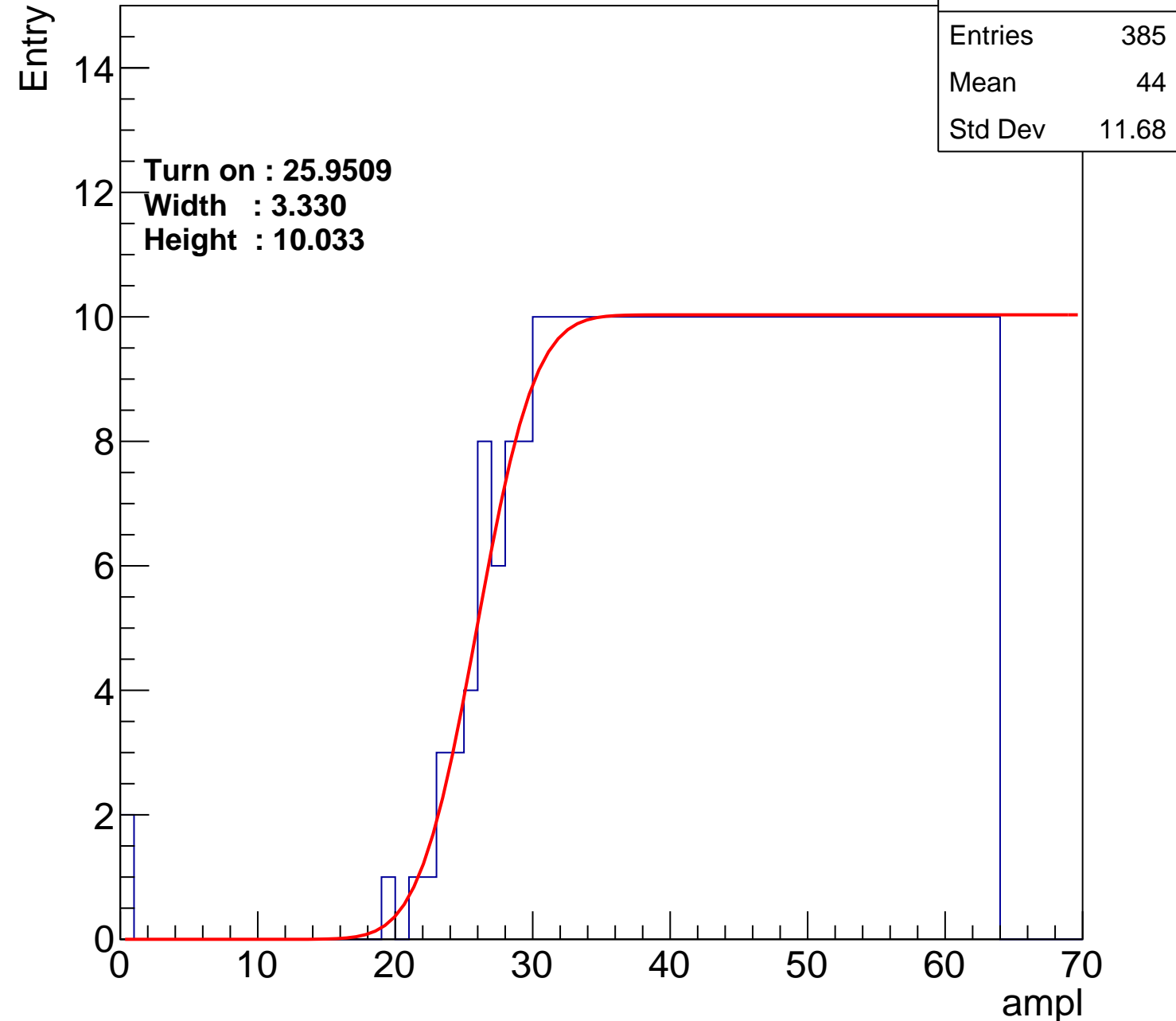
Width : 3.330

Height : 10.033

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch5

calib_packv5_042523_0143.root, FC#4, port A2

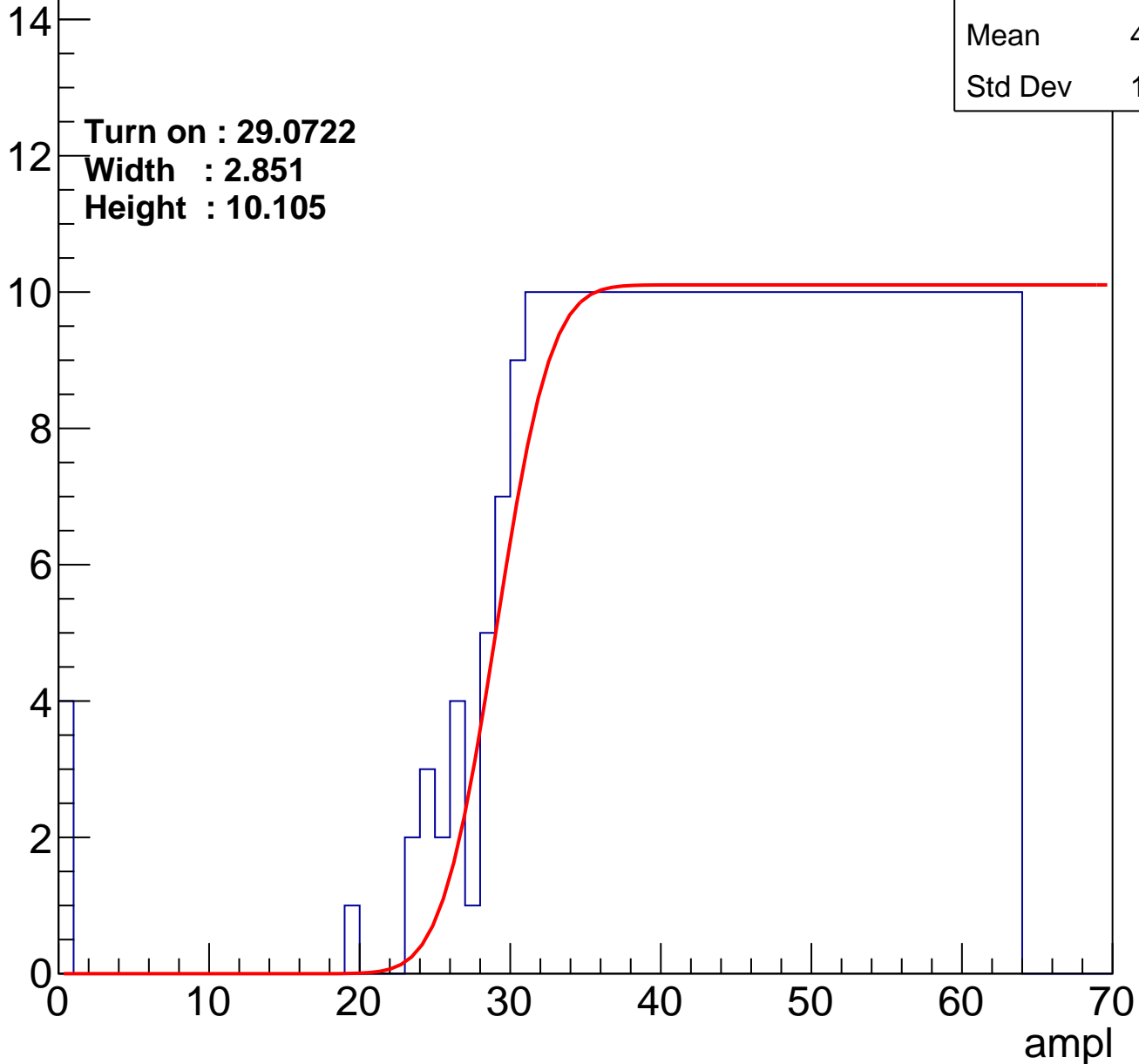
Entries	368
Mean	44.68
Std Dev	11.67

Turn on : 29.0722

Width : 2.851

Height : 10.105

Entry



B1L100S, U5-ch6

calib_packv5_042523_0143.root, FC#4, port A2

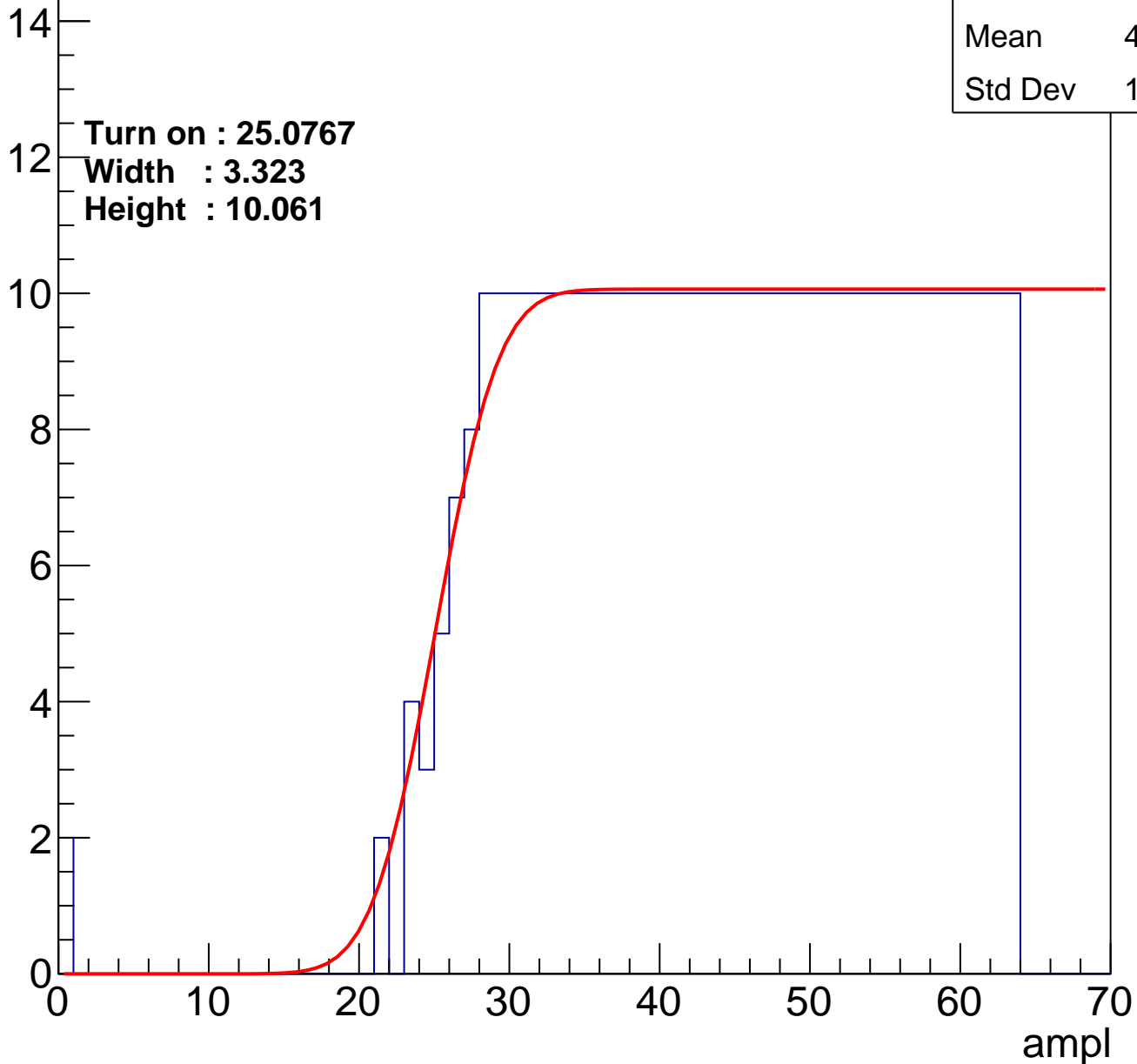
Entries	391
Mean	43.76
Std Dev	11.74

Turn on : 25.0767

Width : 3.323

Height : 10.061

Entry



B1L100S, U5-ch7

calib_packv5_042523_0143.root, FC#4, port A2

Entries	384
Mean	43.93
Std Dev	11.98

Turn on : 26.5570

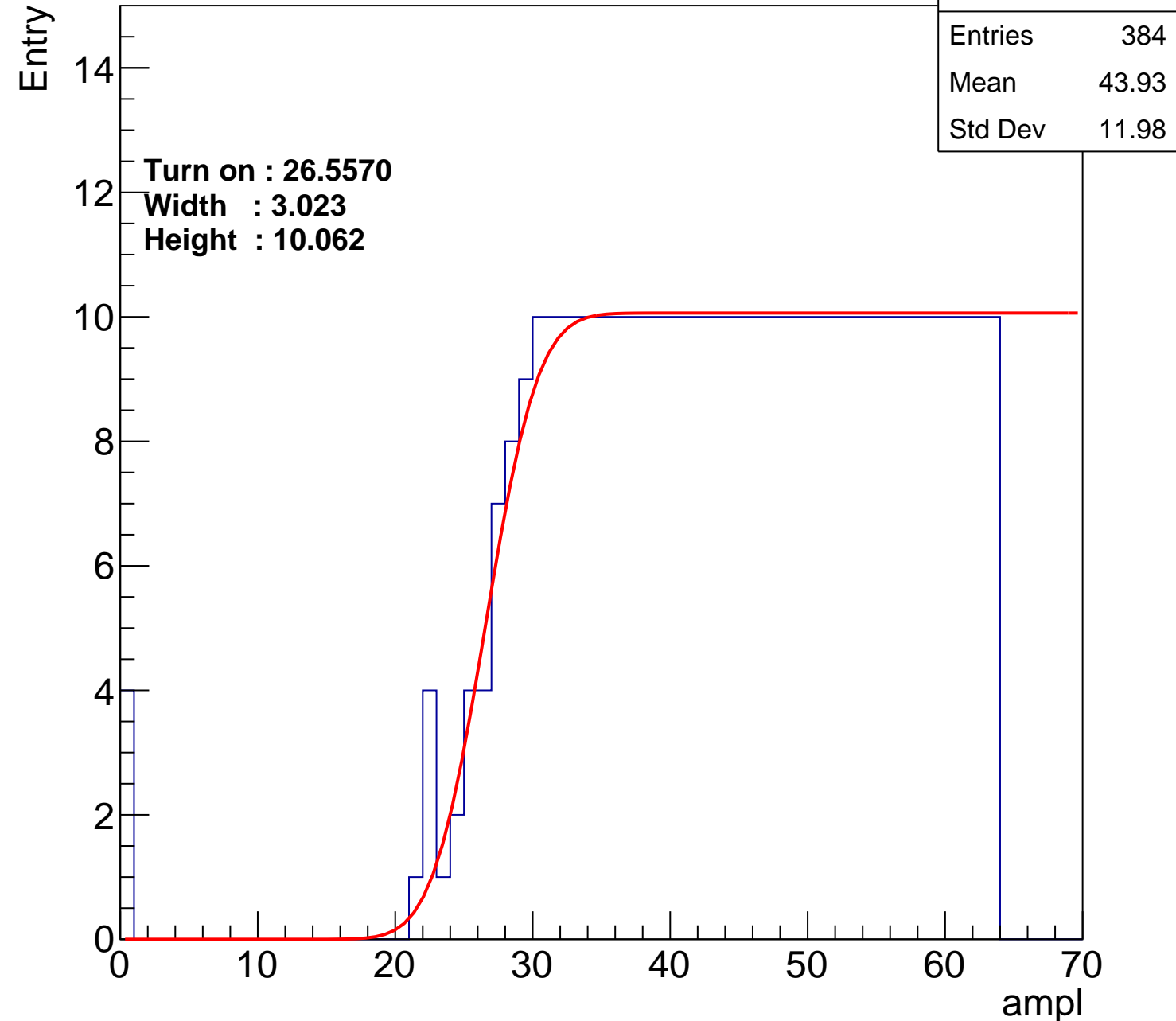
Width : 3.023

Height : 10.062

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch8

calib_packv5_042523_0143.root, FC#4, port A2

Entries	387
Mean	43.9
Std Dev	11.74

Turn on : 26.2402

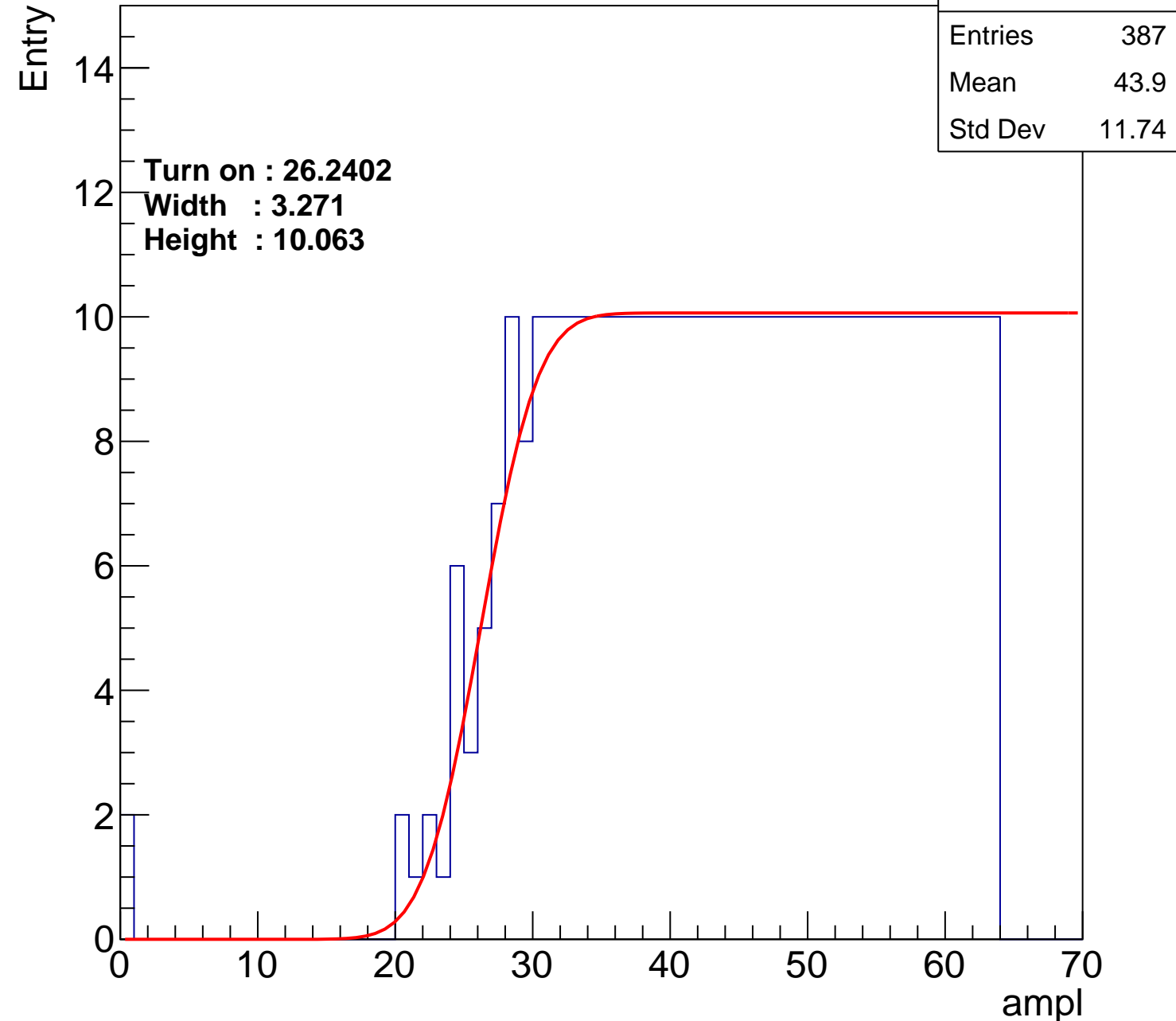
Width : 3.271

Height : 10.063

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch9

calib_packv5_042523_0143.root, FC#4, port A2

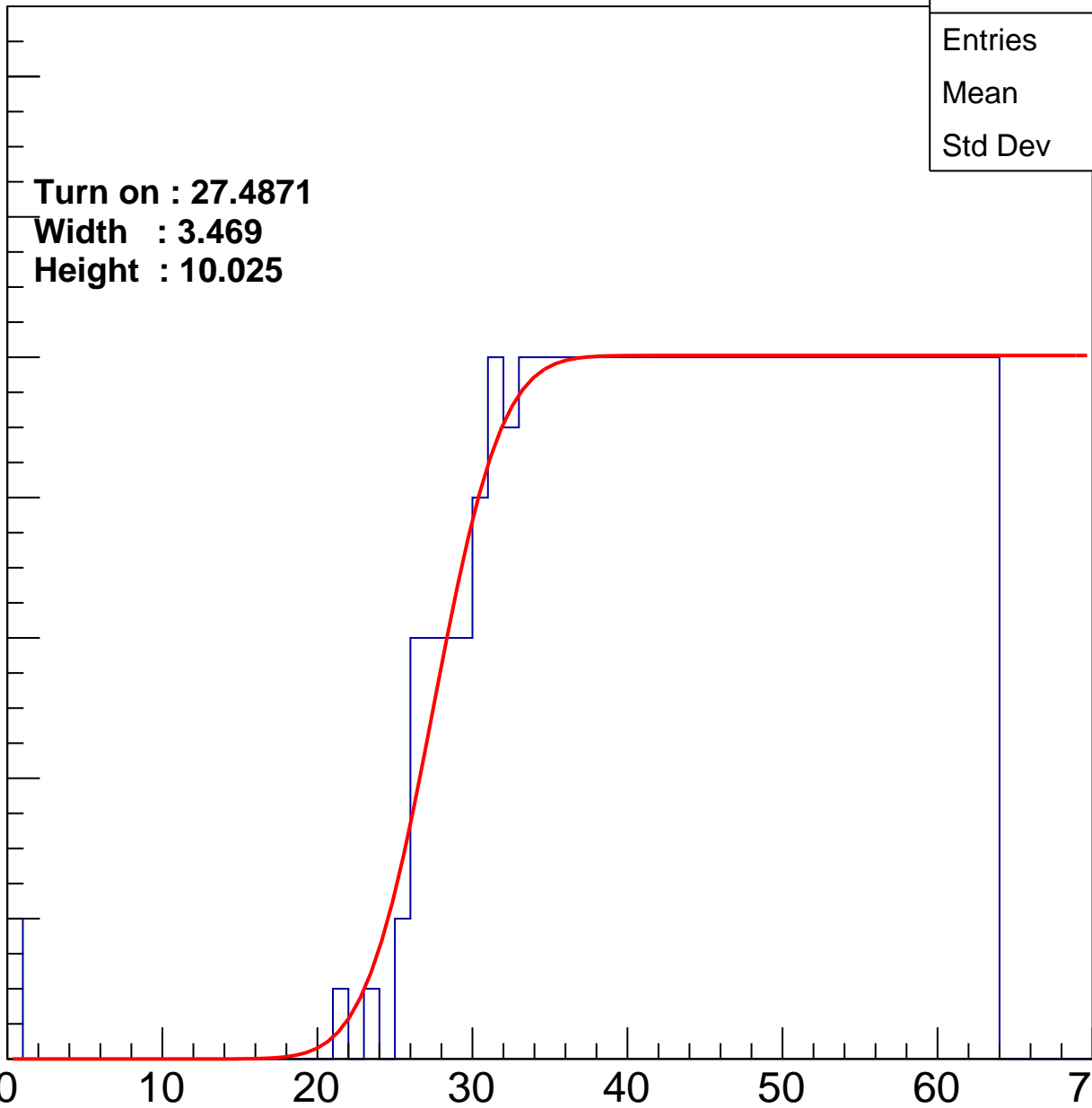
Entry

14
12
10
8
6
4
2
0

Turn on : 27.4871
Width : 3.469
Height : 10.025

Entries	367
Mean	44.88
Std Dev	11.21

ampl



B1L100S, U5-ch10

calib_packv5_042523_0143.root, FC#4, port A2

Entries	373
Mean	44.38
Std Dev	11.85

Turn on : 28.4473

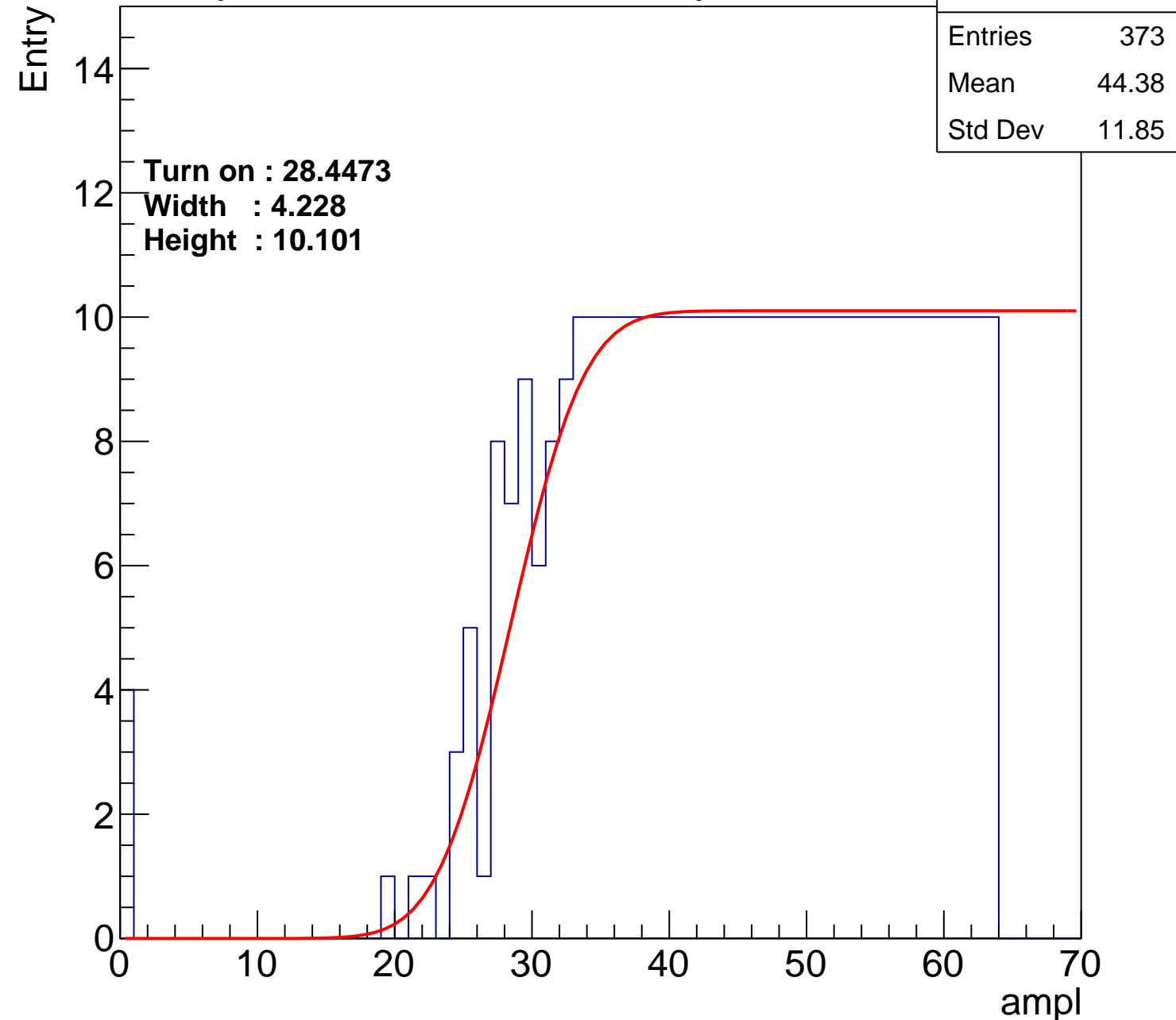
Width : 4.228

Height : 10.101

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch11

calib_packv5_042523_0143.root, FC#4, port A2

Entries	386
Mean	43.83
Std Dev	12.01

Turn on : 25.8109

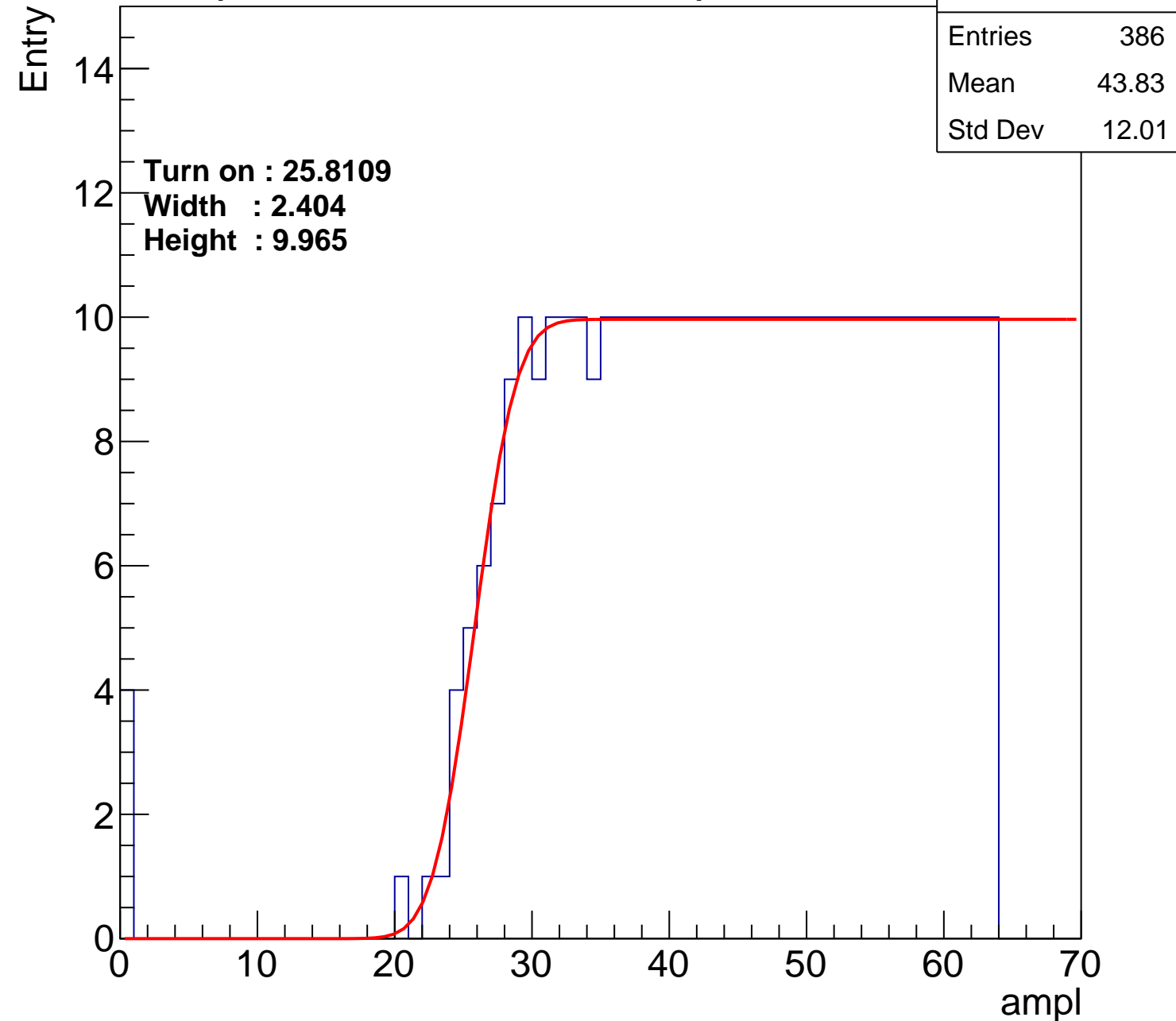
Width : 2.404

Height : 9.965

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch12

calib_packv5_042523_0143.root, FC#4, port A2

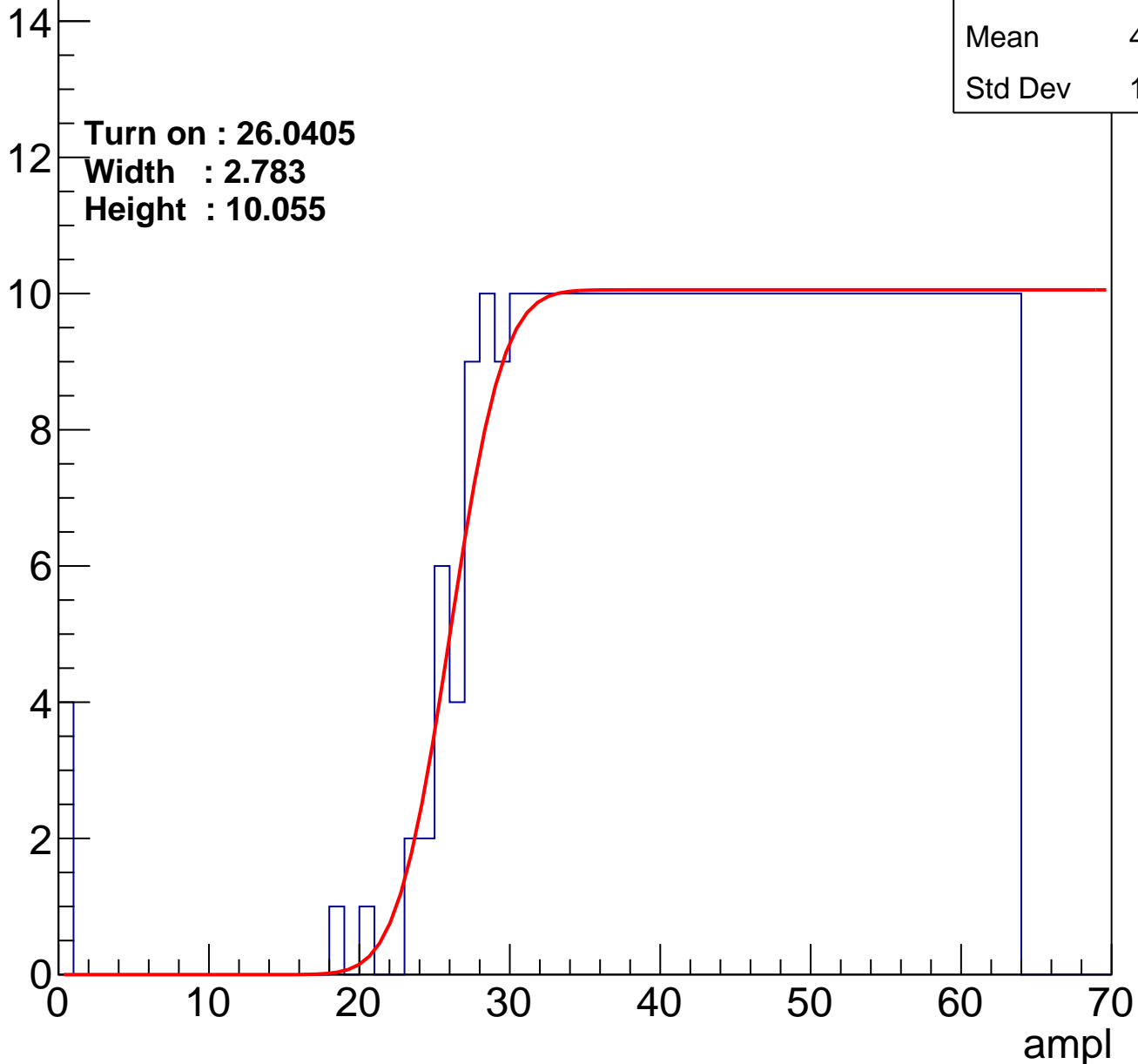
Entries	388
Mean	43.76
Std Dev	12.03

Turn on : 26.0405

Width : 2.783

Height : 10.055

Entry



B1L100S, U5-ch13

calib_packv5_042523_0143.root, FC#4, port A2

Entries	388
Mean	43.85
Std Dev	11.83

Turn on : 25.9204

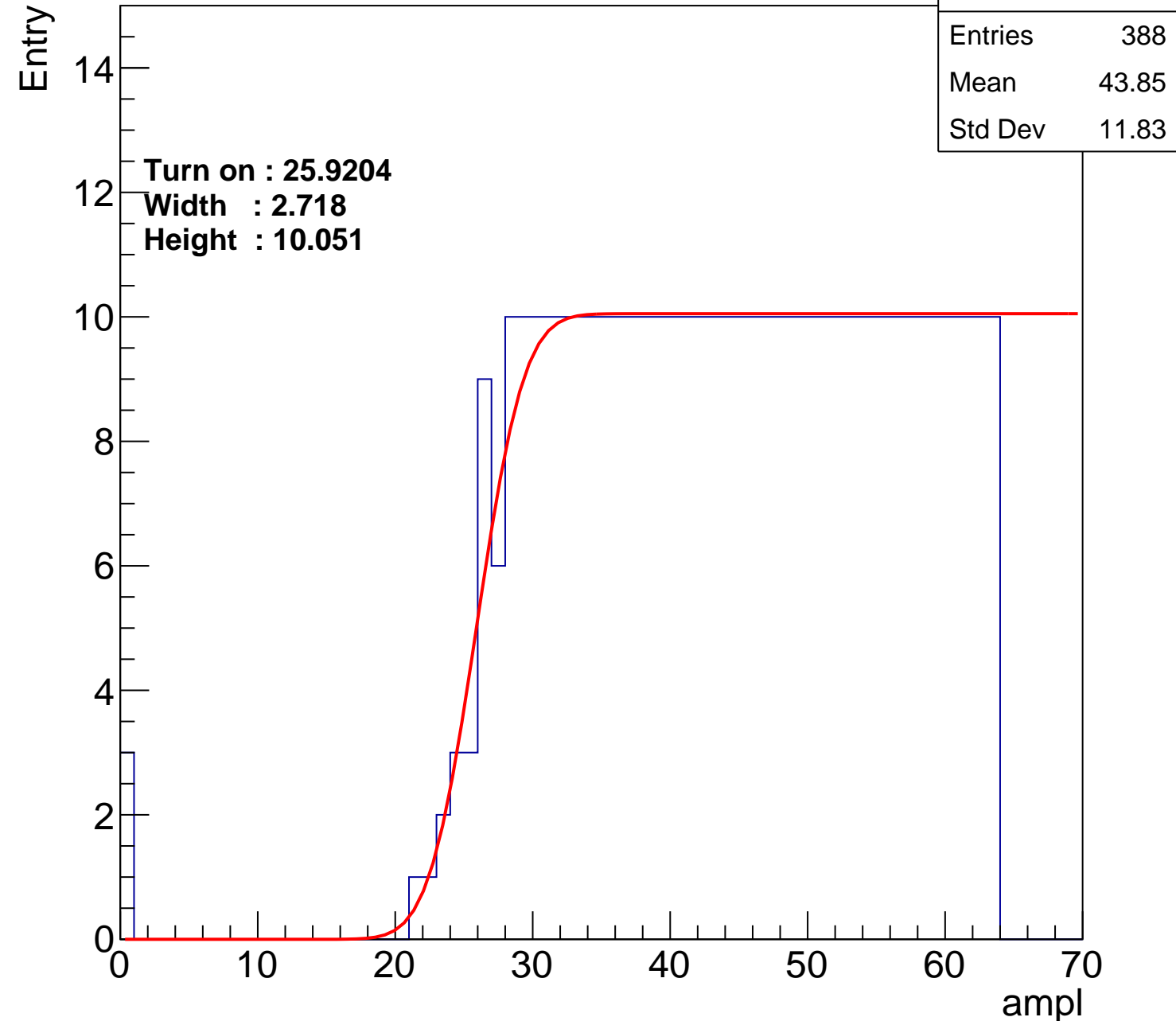
Width : 2.718

Height : 10.051

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch14

calib_packv5_042523_0143.root, FC#4, port A2

Entries	374
Mean	44.63
Std Dev	11.16

Turn on : 27.1311

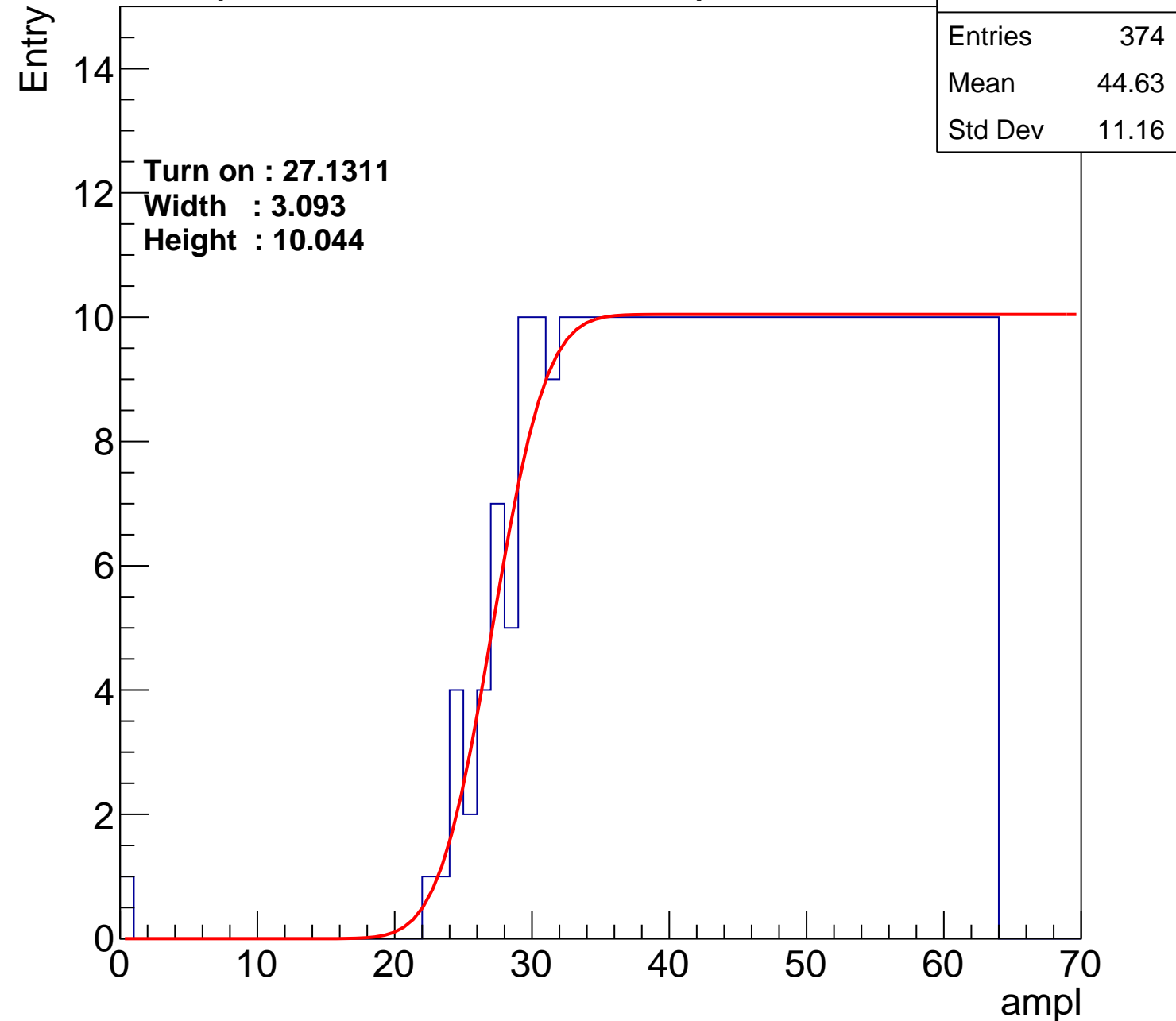
Width : 3.093

Height : 10.044

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch15

calib_packv5_042523_0143.root, FC#4, port A2

Entries	399
Mean	43.26
Std Dev	12.17

Turn on : 24.6892

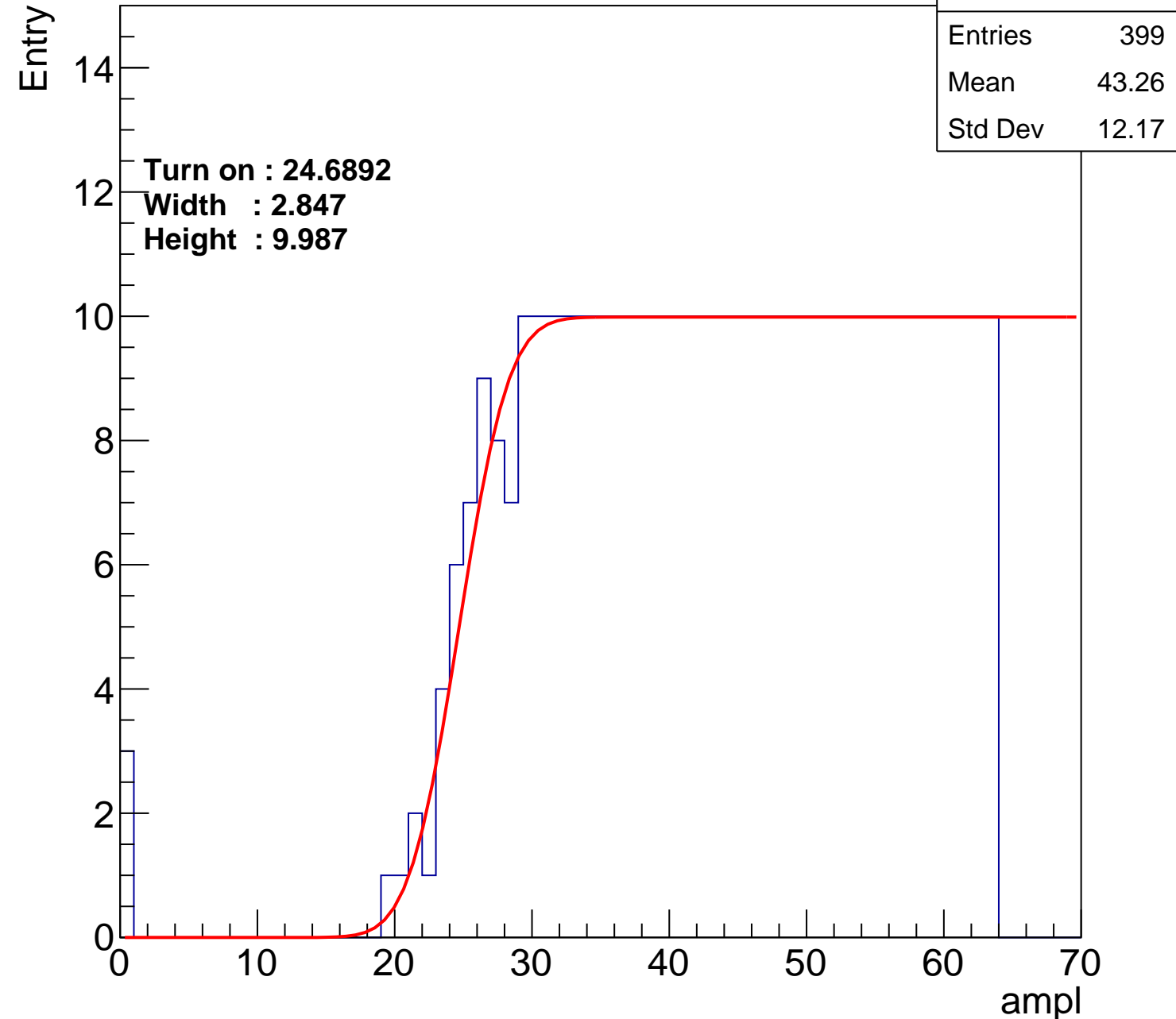
Width : 2.847

Height : 9.987

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch16

calib_packv5_042523_0143.root, FC#4, port A2

Entries	386
Mean	43.91
Std Dev	11.83

Turn on : 26.3277

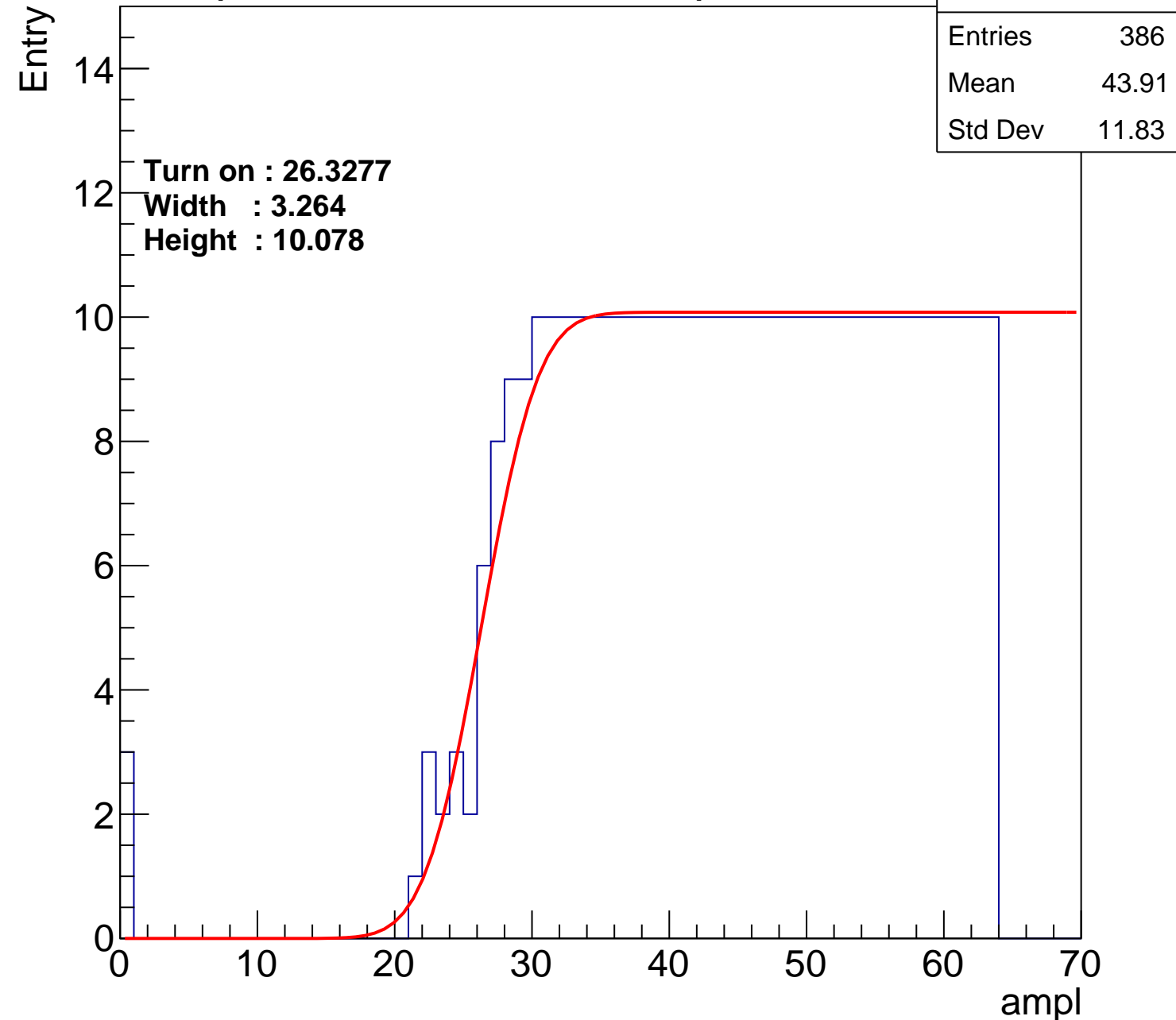
Width : 3.264

Height : 10.078

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch17

calib_packv5_042523_0143.root, FC#4, port A2

Entries	379
Mean	44.28
Std Dev	11.62

Turn on : 26.2307

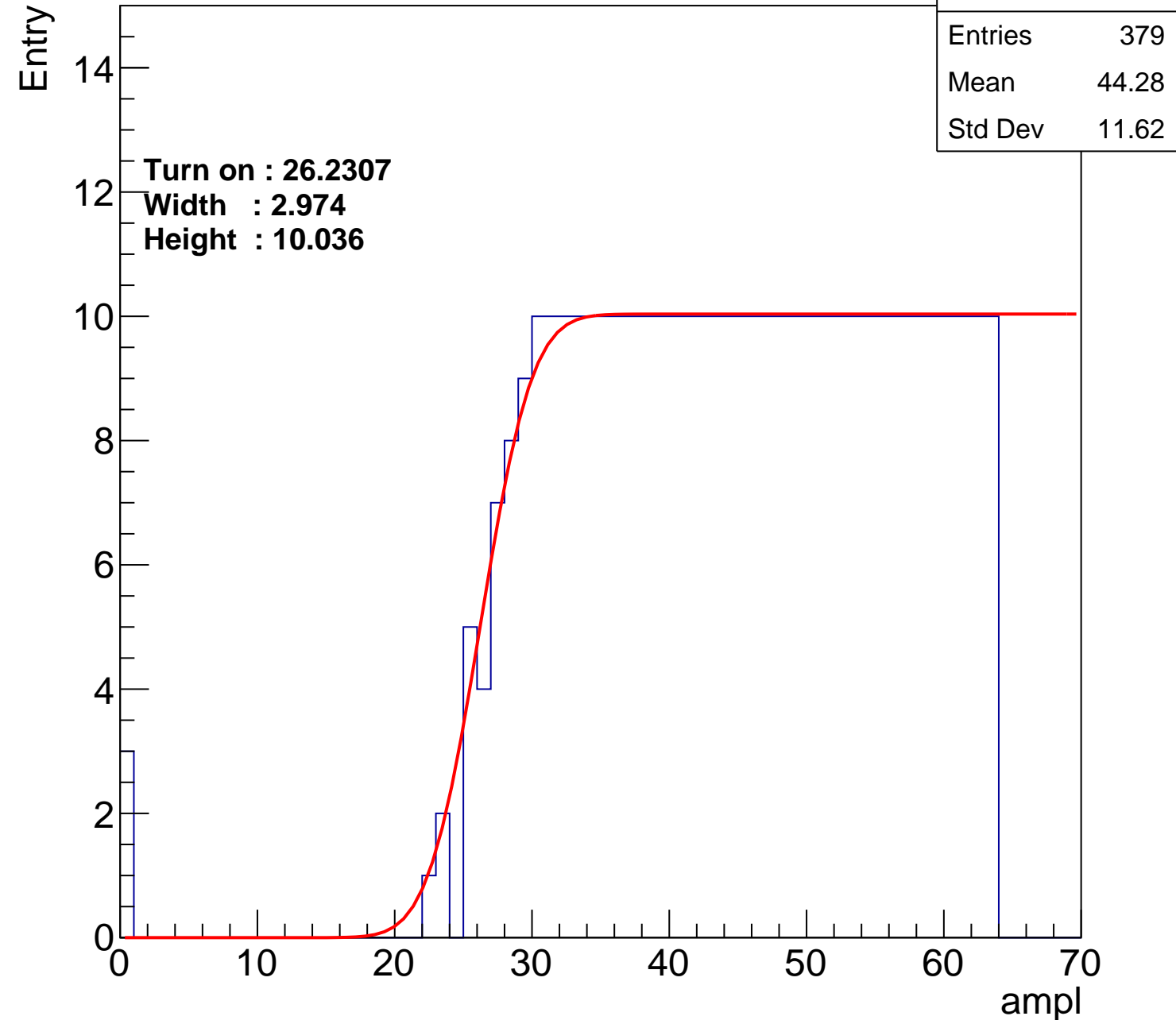
Width : 2.974

Height : 10.036

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch18

calib_packv5_042523_0143.root, FC#4, port A2

Entries	369
Mean	44.9
Std Dev	10.99

Turn on : 27.0872

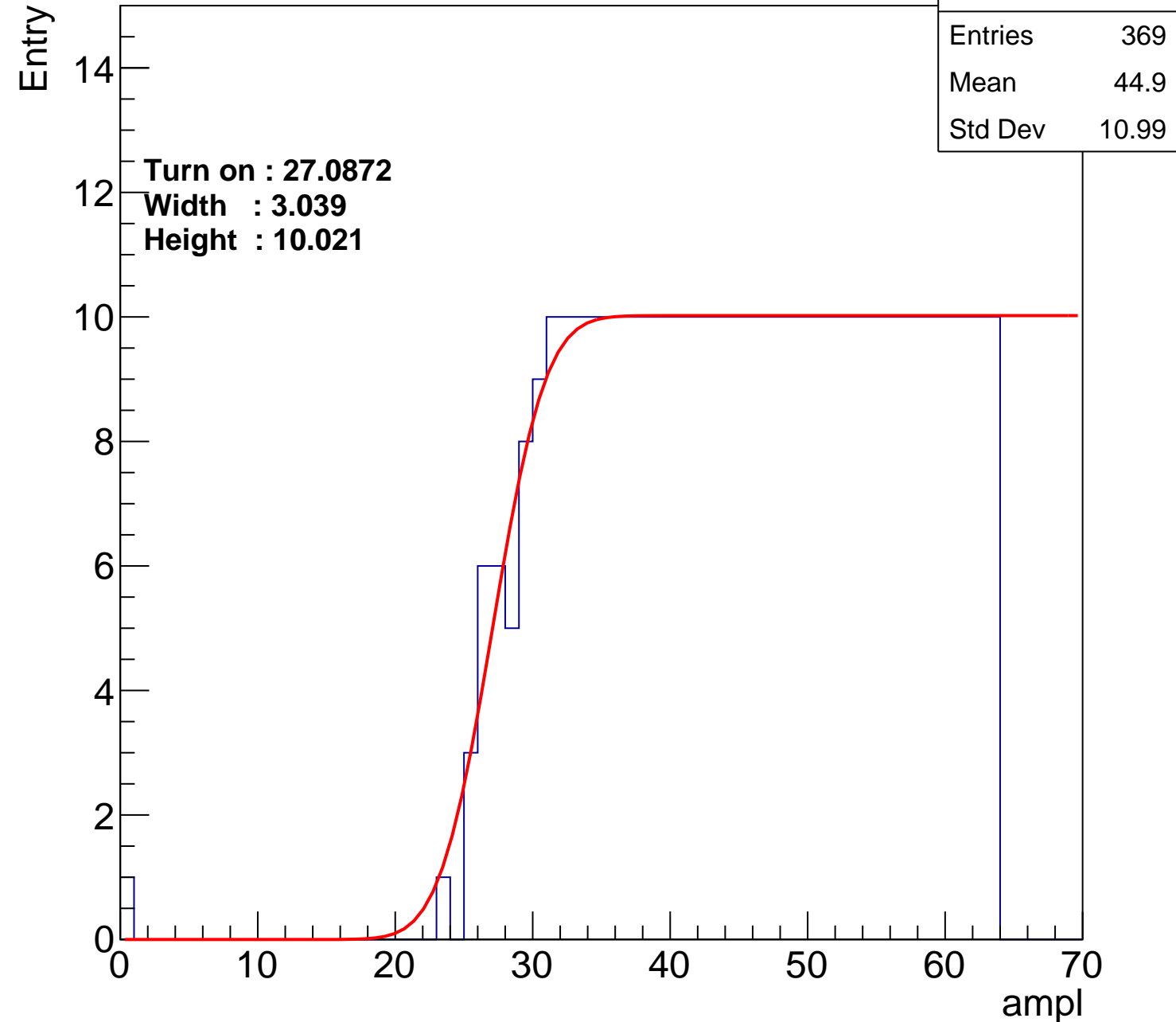
Width : 3.039

Height : 10.021

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch19

calib_packv5_042523_0143.root, FC#4, port A2

Entries	369
Mean	44.91
Std Dev	10.98

Turn on : 27.0187

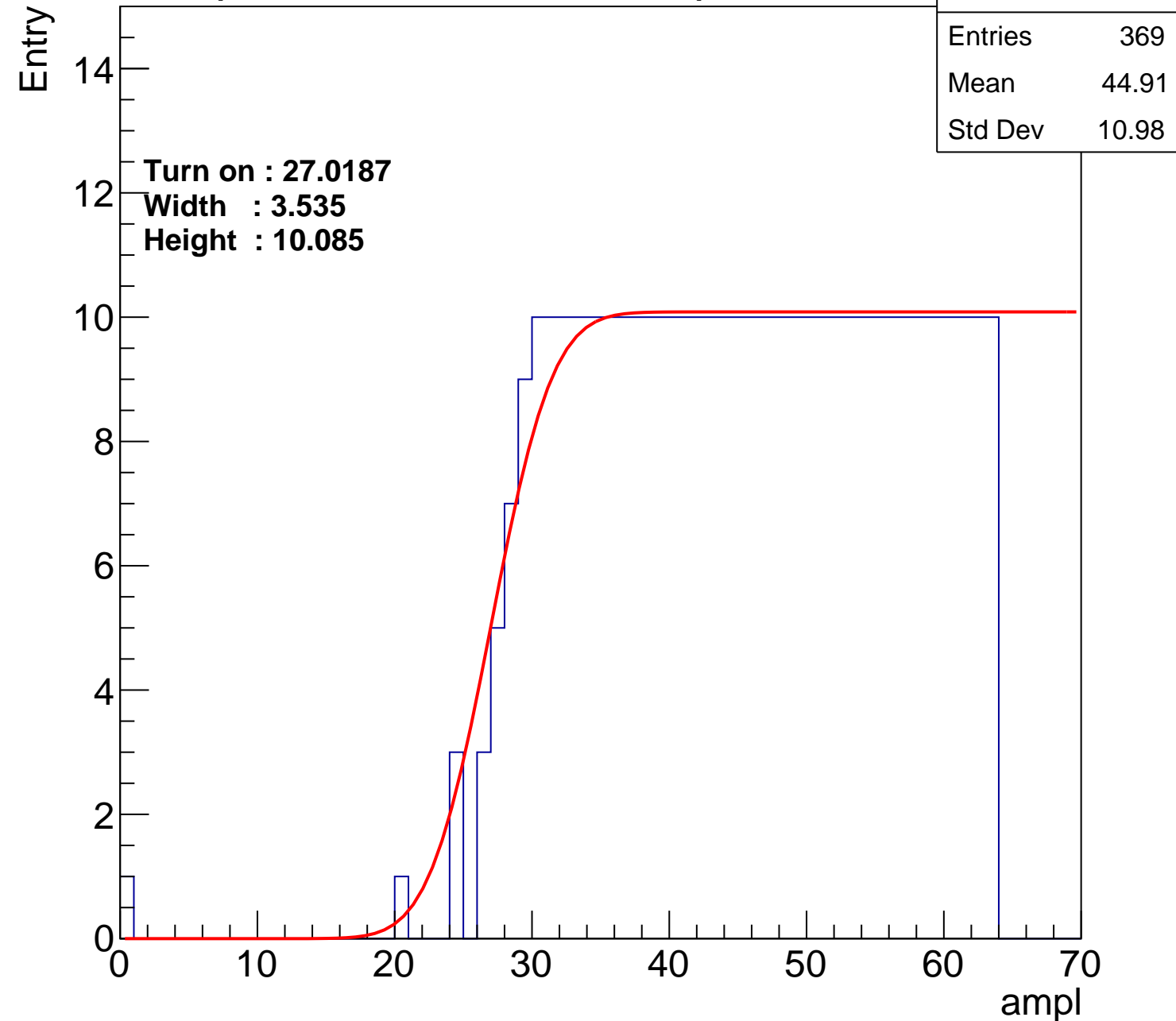
Width : 3.535

Height : 10.085

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch20

calib_packv5_042523_0143.root, FC#4, port A2

Entries	398
Mean	43.25
Std Dev	12.3

Turn on : 25.0571

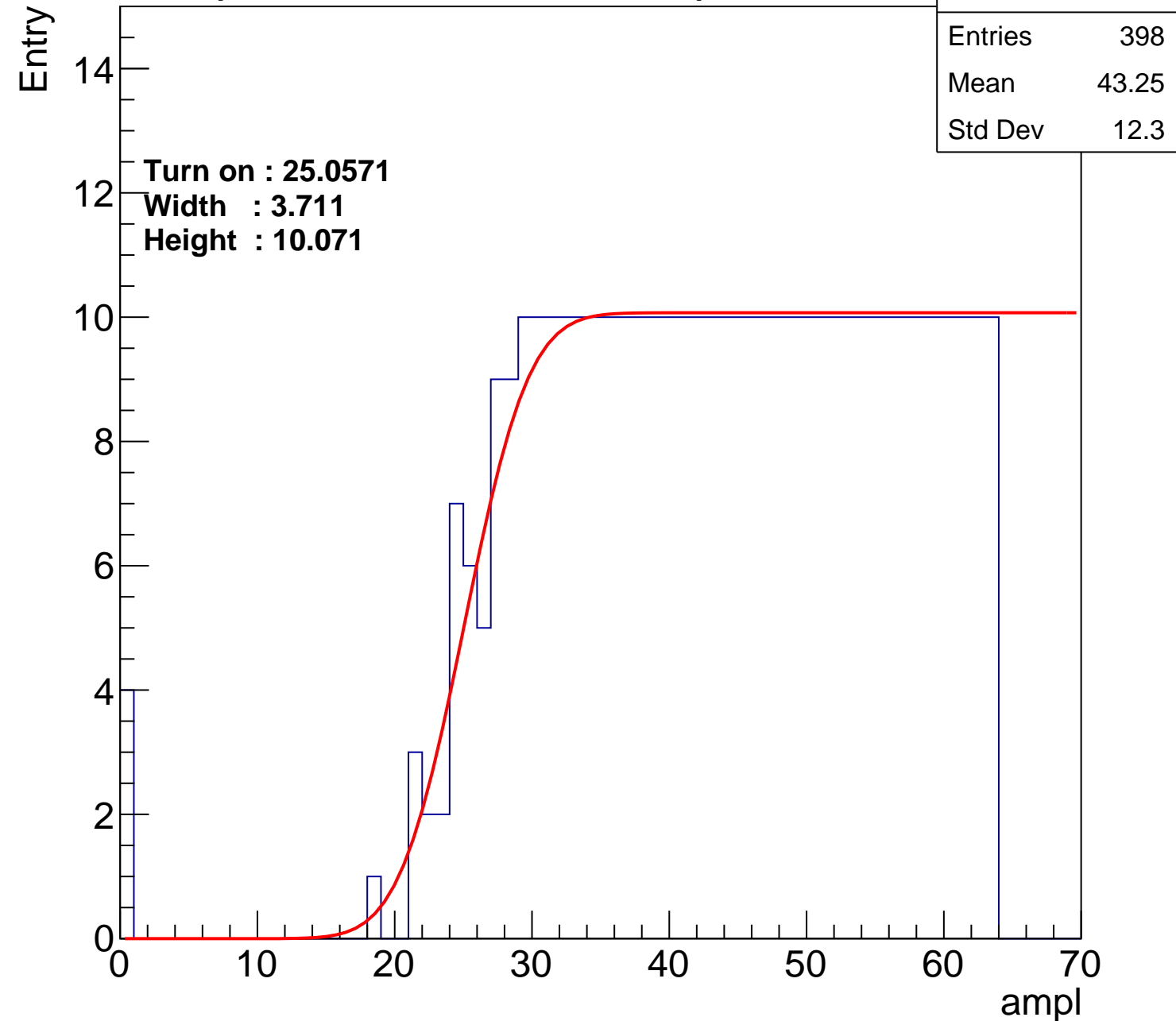
Width : 3.711

Height : 10.071

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch21

calib_packv5_042523_0143.root, FC#4, port A2

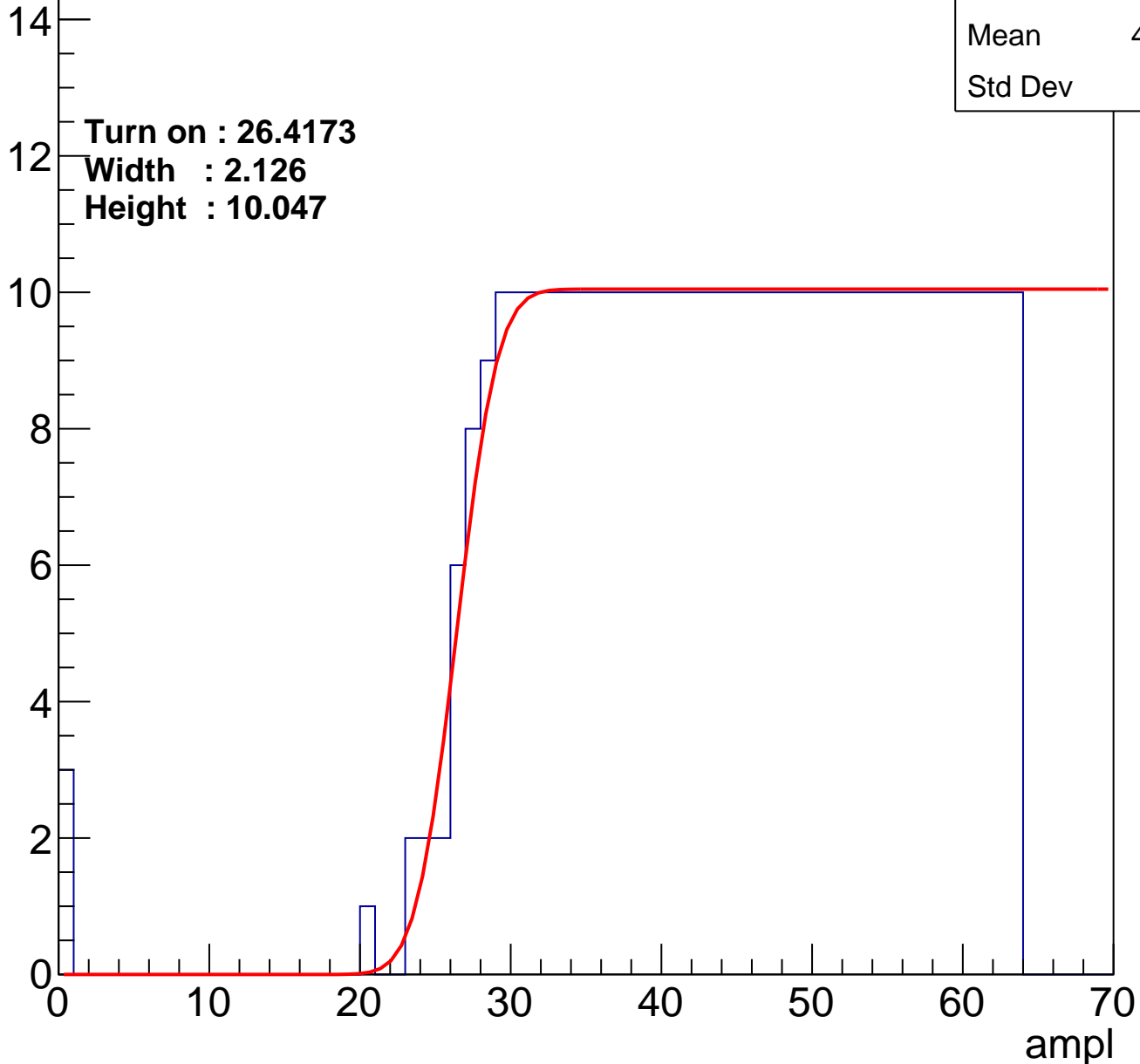
Entries	383
Mean	44.09
Std Dev	11.7

Turn on : 26.4173

Width : 2.126

Height : 10.047

Entry



B1L100S, U5-ch22

calib_packv5_042523_0143.root, FC#4, port A2

Entries	381
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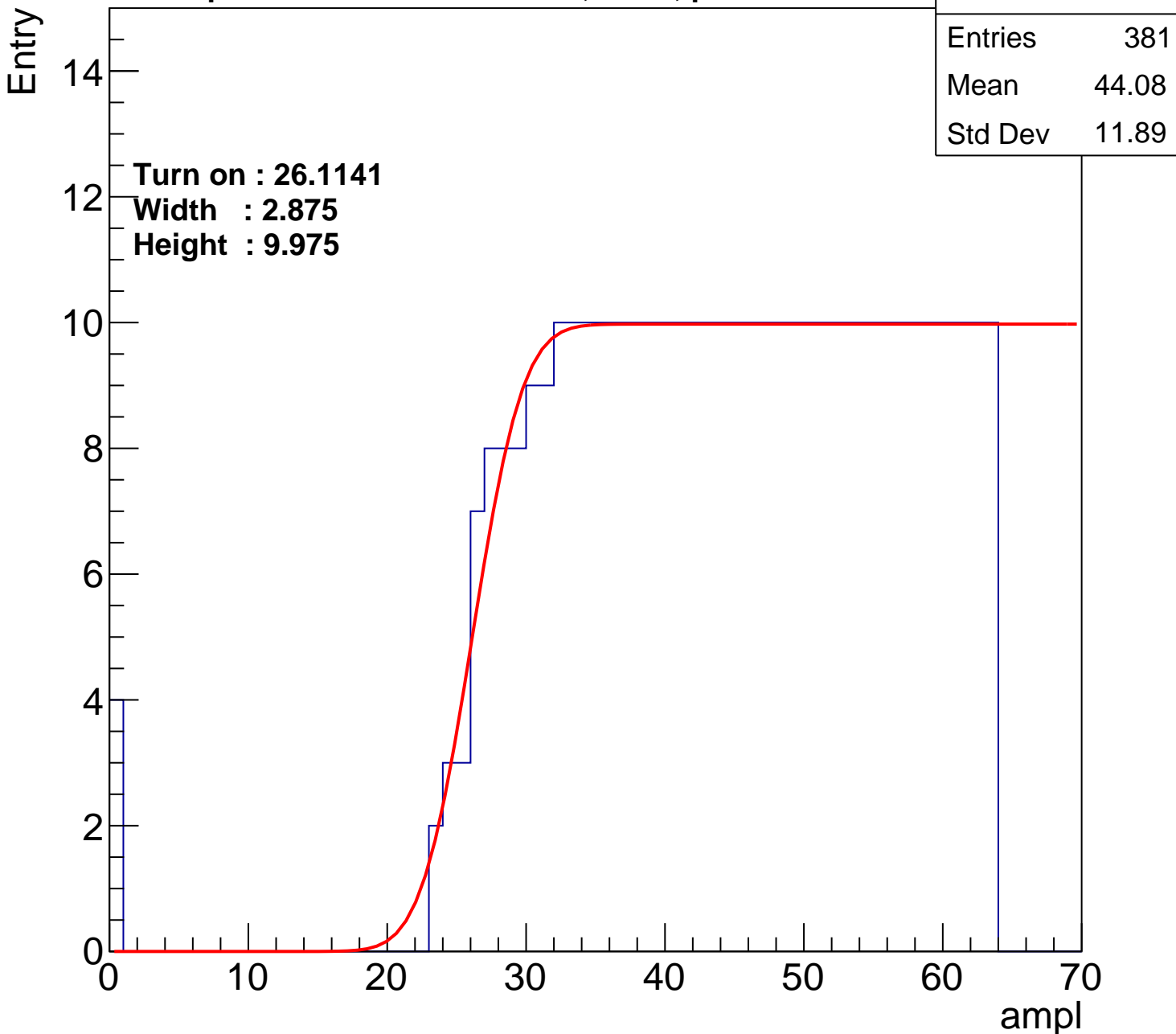
Mean	44.08
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Std Dev	11.89
---------	-------

Turn on : 26.1141

Width : 2.875

Height : 9.975



B1L100S, U5-ch23

calib_packv5_042523_0143.root, FC#4, port A2

Entries	388
Mean	43.78
Std Dev	11.93

Turn on : 26.3464

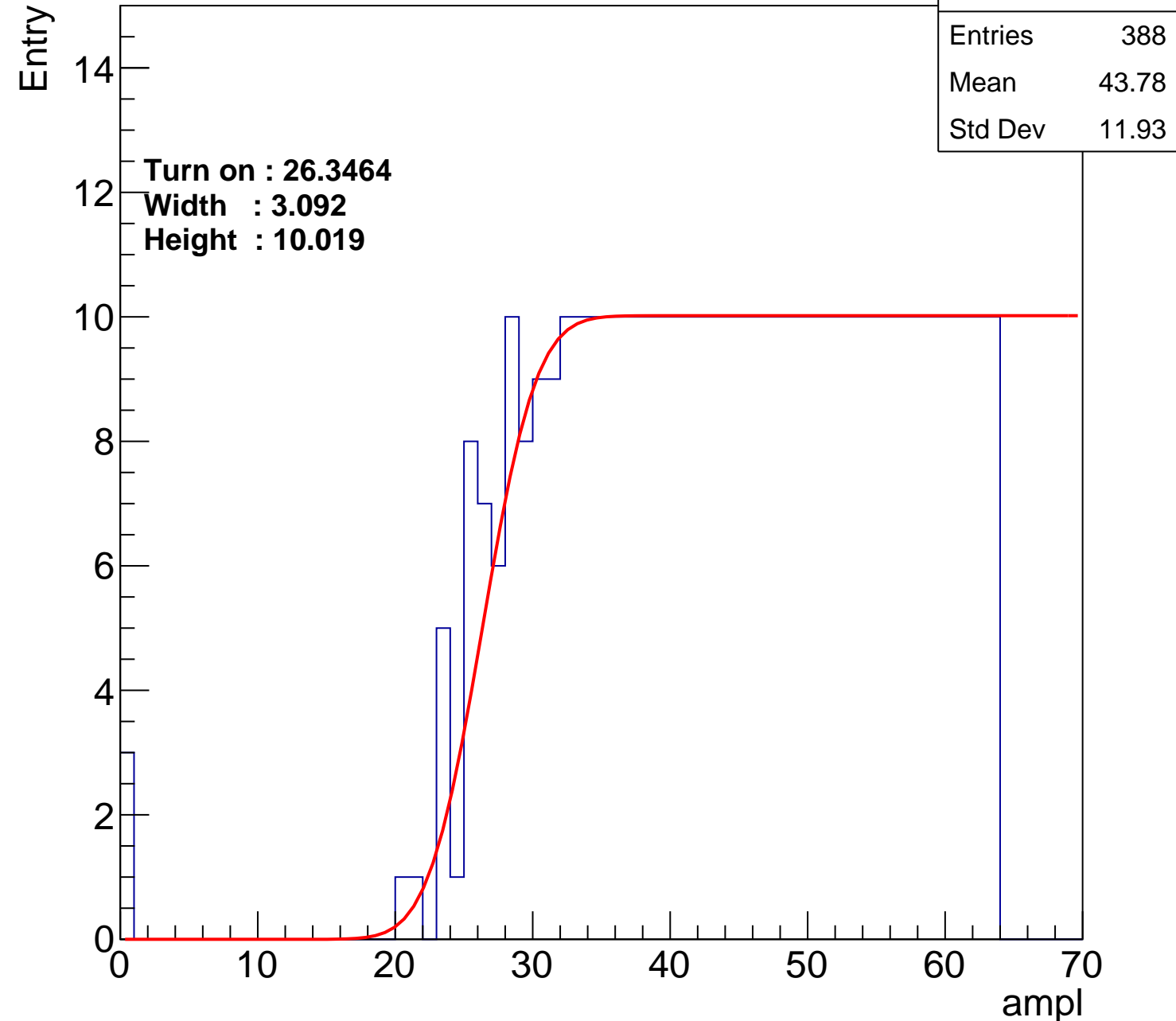
Width : 3.092

Height : 10.019

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch24

calib_packv5_042523_0143.root, FC#4, port A2

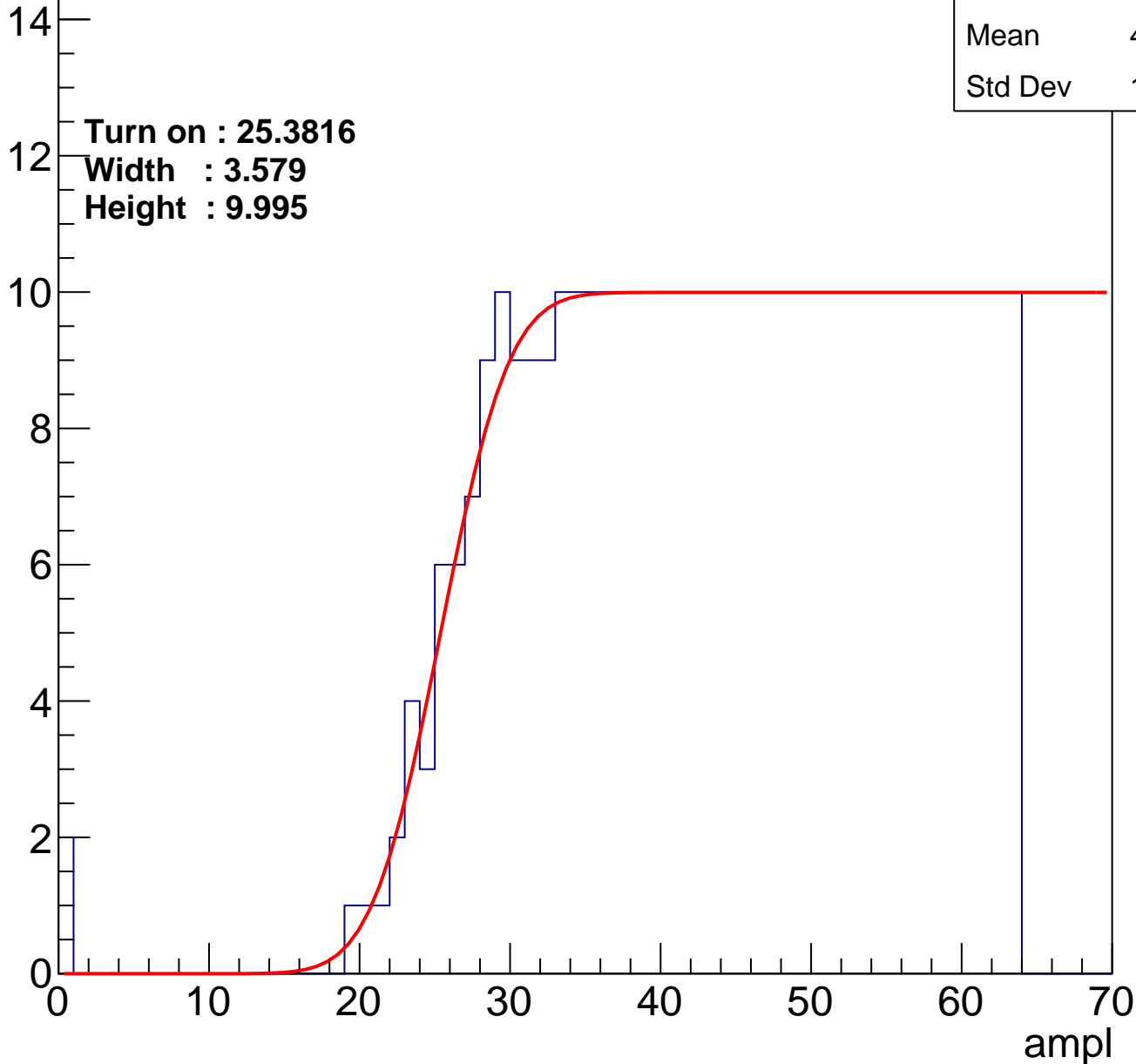
Entries	389
Mean	43.76
Std Dev	11.84

Turn on : 25.3816

Width : 3.579

Height : 9.995

Entry



B1L100S, U5-ch25

calib_packv5_042523_0143.root, FC#4, port A2

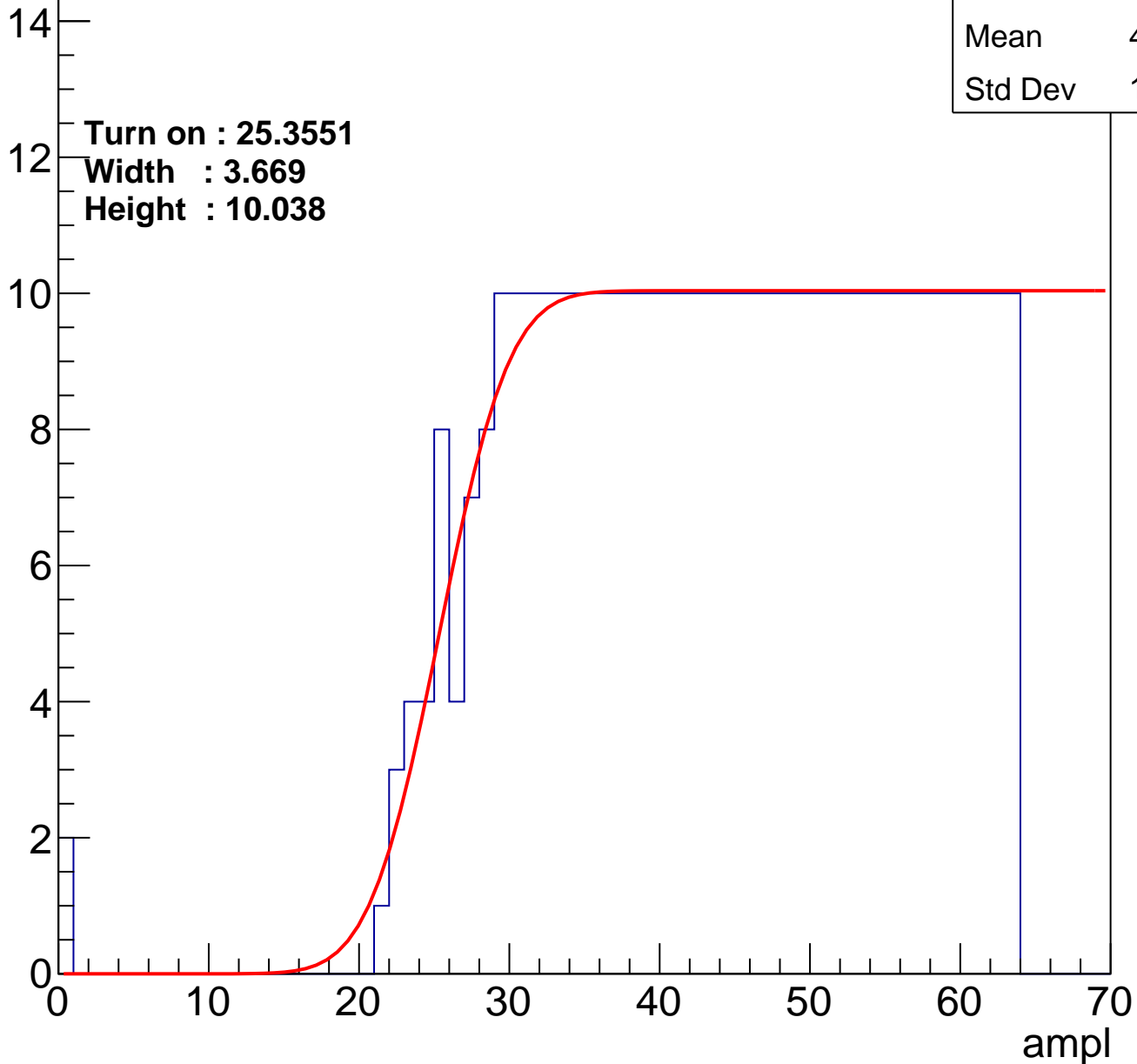
Entries	391
Mean	43.71
Std Dev	11.81

Turn on : 25.3551

Width : 3.669

Height : 10.038

Entry



B1L100S, U5-ch26

calib_packv5_042523_0143.root, FC#4, port A2

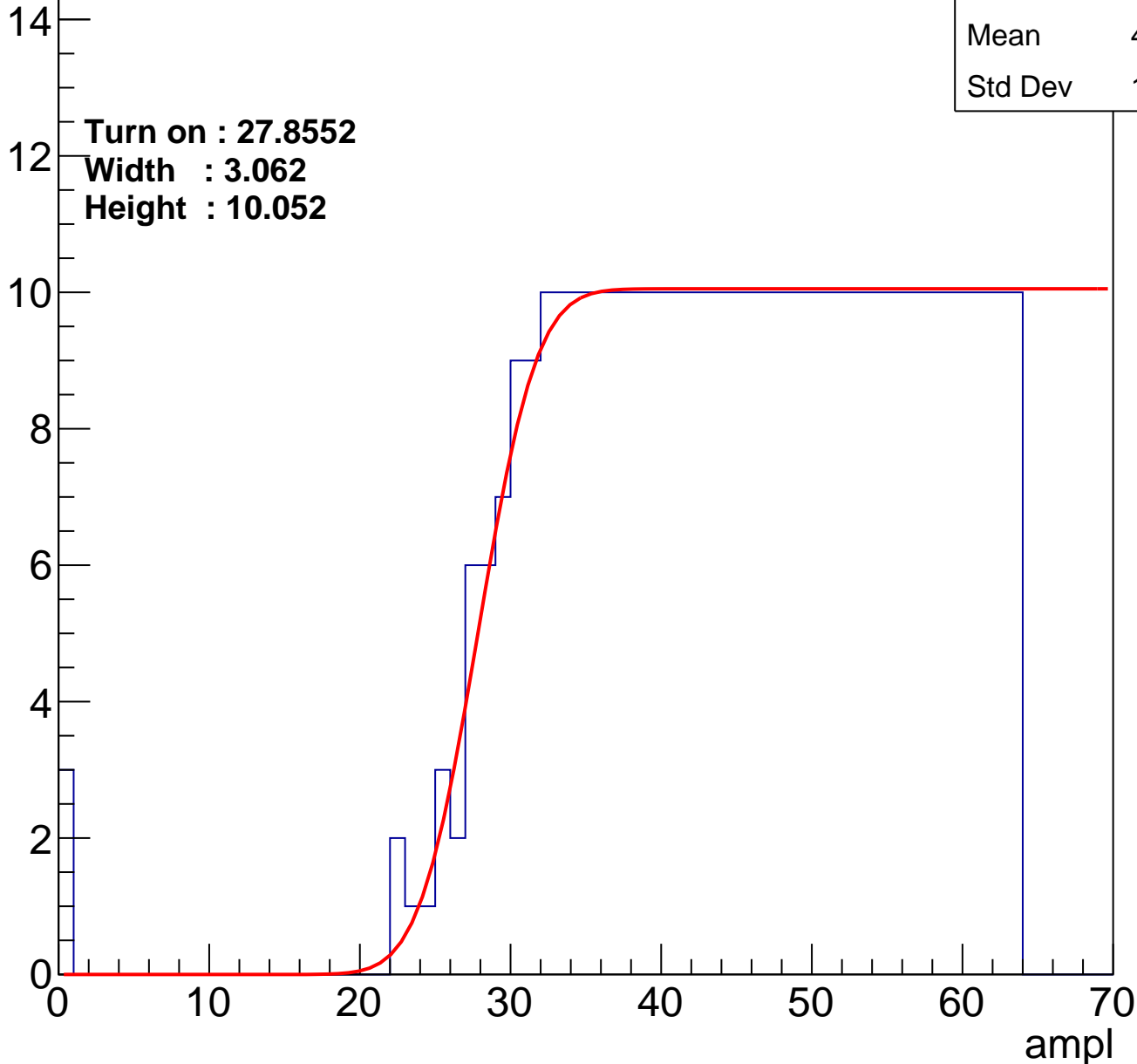
Entries	369
Mean	44.72
Std Dev	11.46

Turn on : 27.8552

Width : 3.062

Height : 10.052

Entry



B1L100S, U5-ch27

calib_packv5_042523_0143.root, FC#4, port A2

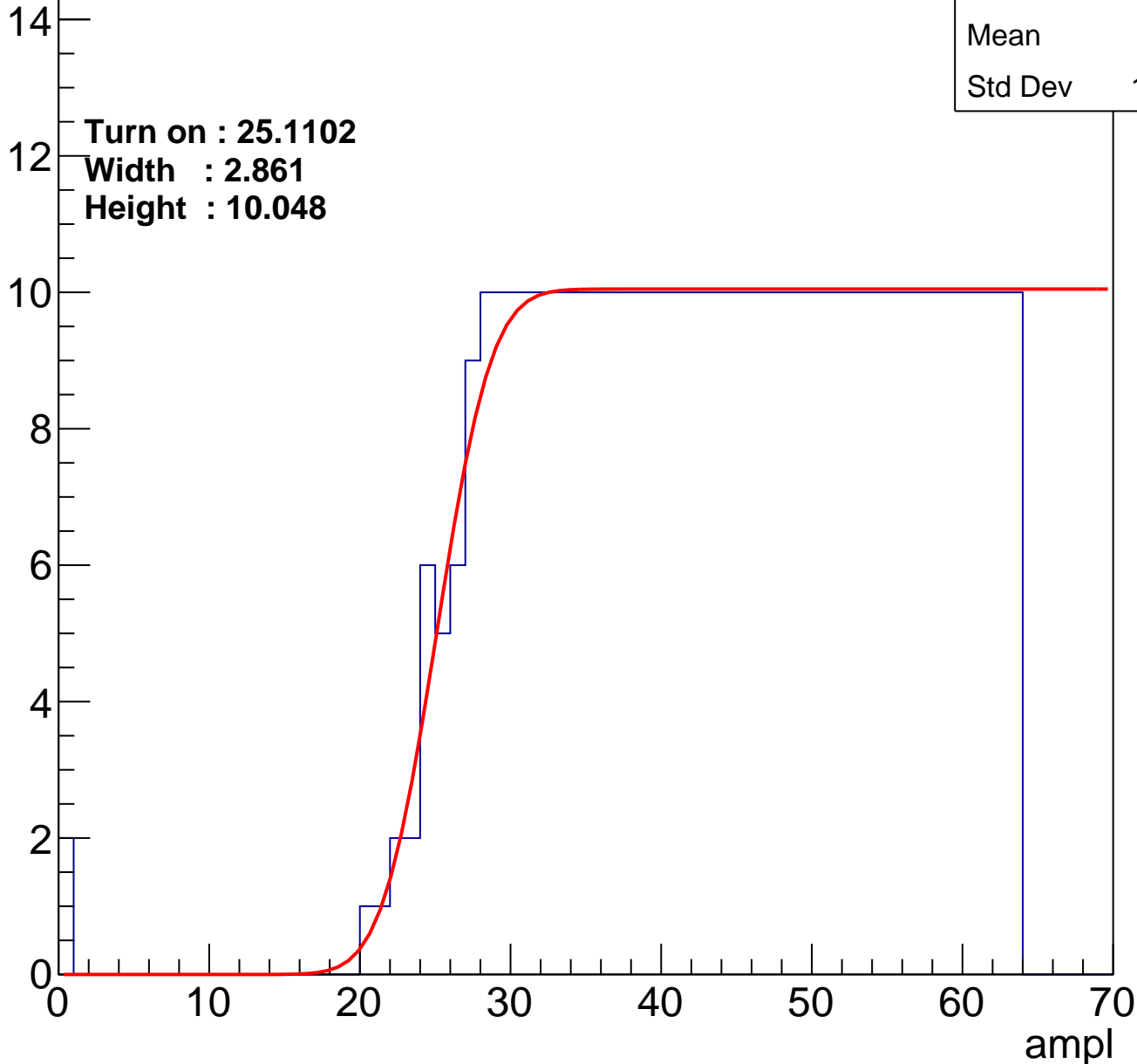
Entries	394
Mean	43.6
Std Dev	11.83

Turn on : 25.1102

Width : 2.861

Height : 10.048

Entry



B1L100S, U5-ch28

calib_packv5_042523_0143.root, FC#4, port A2

Entries	394
Mean	43.46
Std Dev	12.18

Turn on : 25.0317

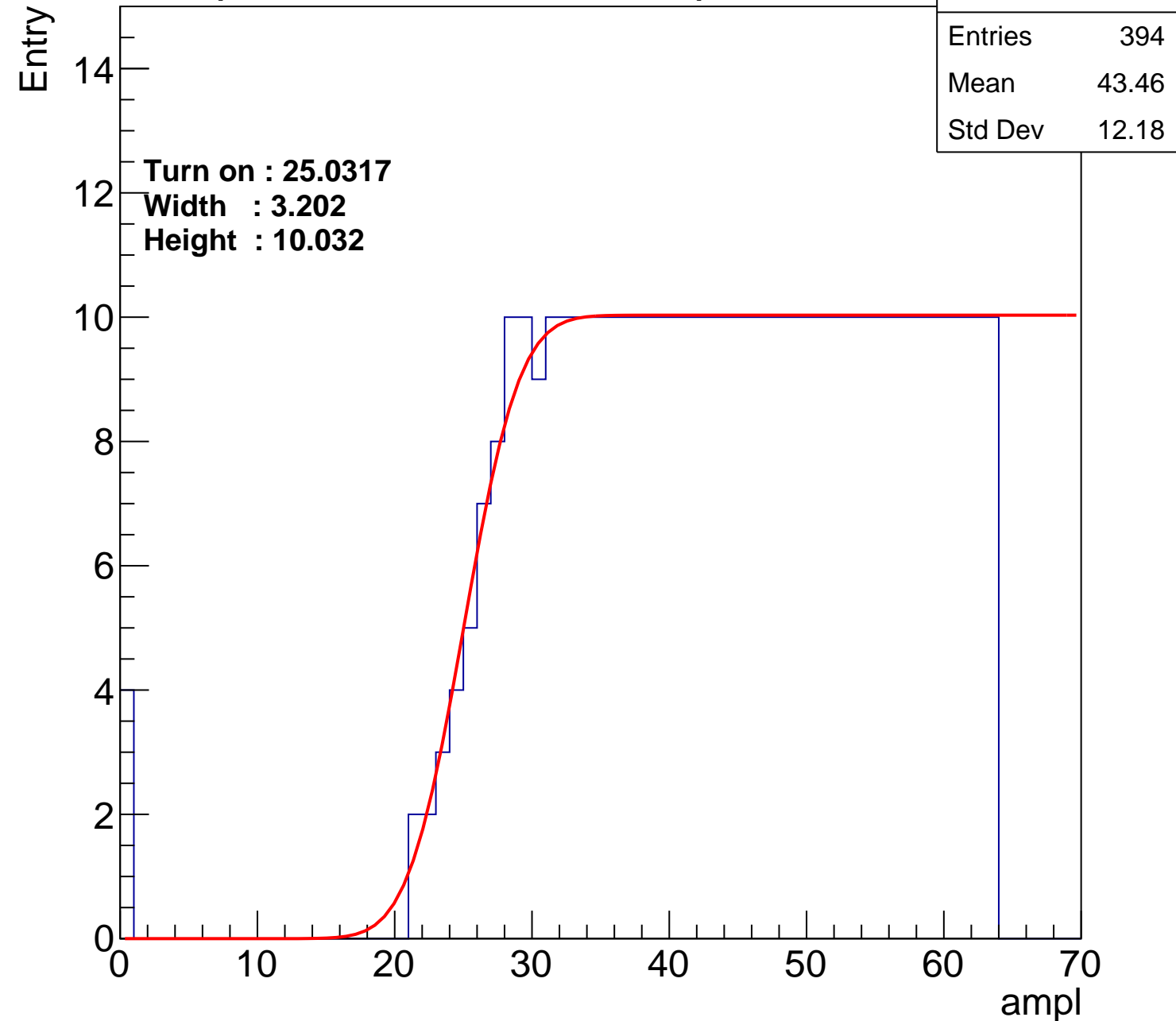
Width : 3.202

Height : 10.032

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch29

calib_packv5_042523_0143.root, FC#4, port A2

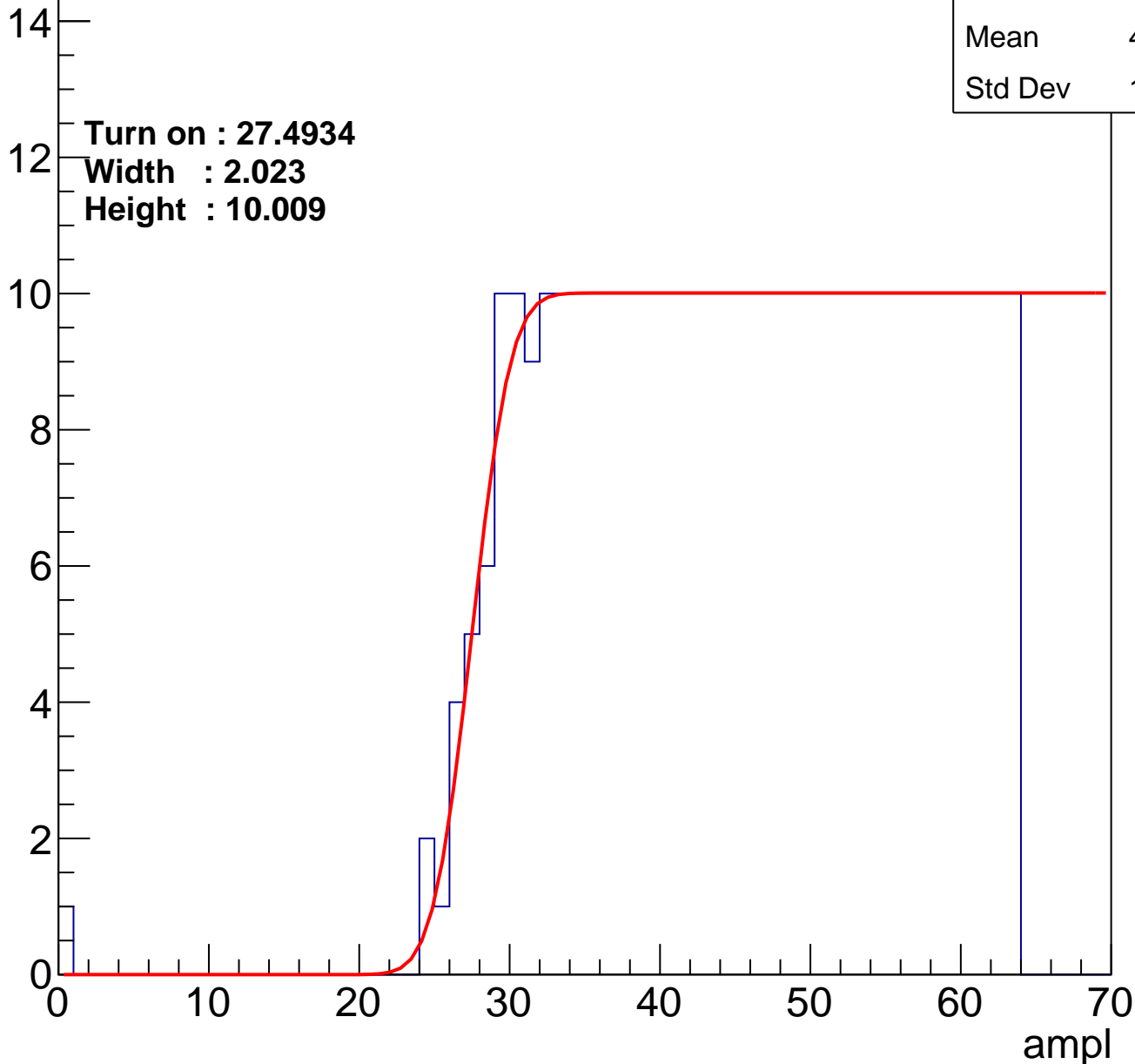
Entry

Entries	368
Mean	44.97
Std Dev	10.93

Turn on : 27.4934

Width : 2.023

Height : 10.009



B1L100S, U5-ch30

calib_packv5_042523_0143.root, FC#4, port A2

Entries	395
Mean	43.46
Std Dev	12.07

Turn on : 25.1858

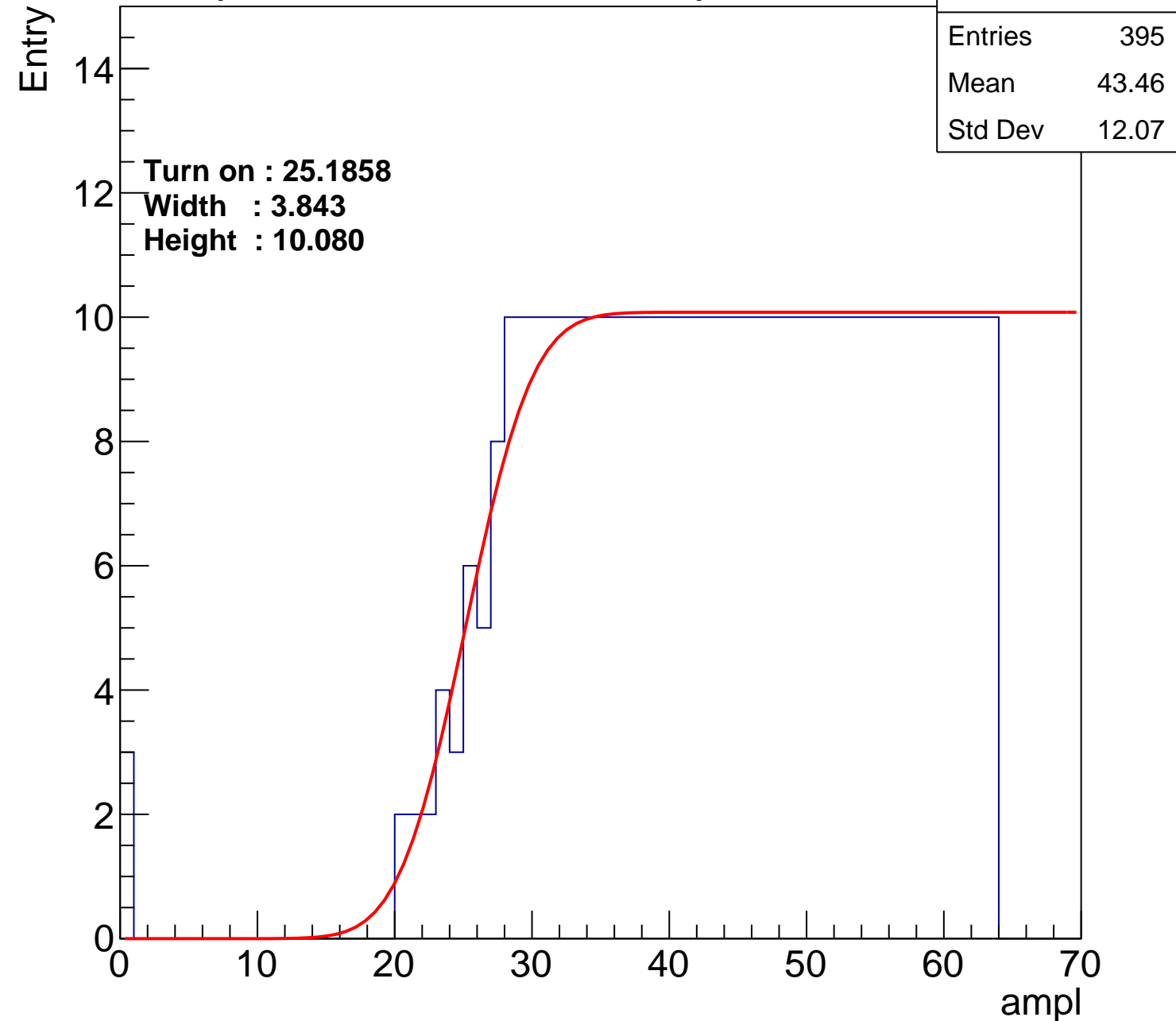
Width : 3.843

Height : 10.080

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch31

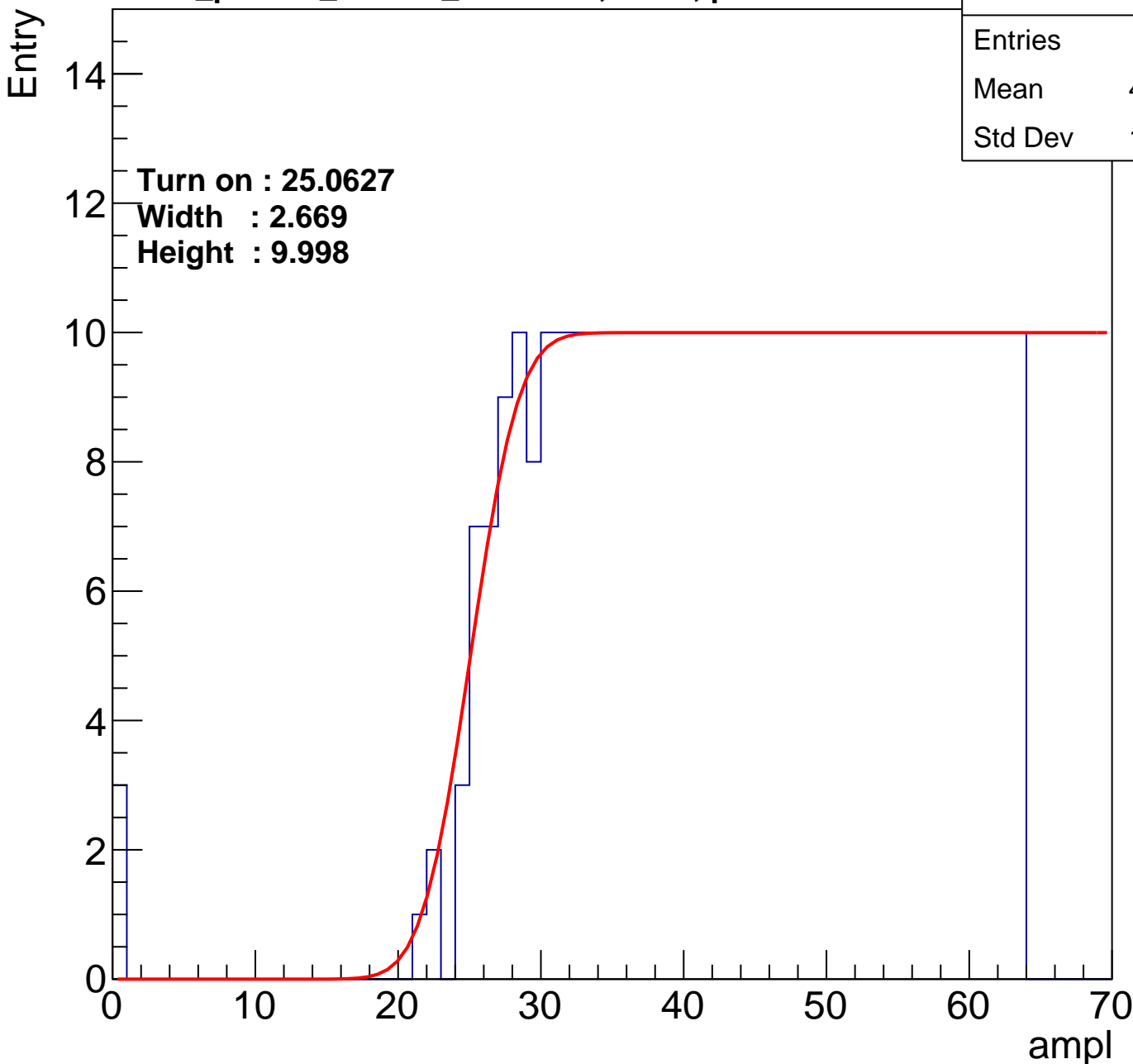
calib_packv5_042523_0143.root, FC#4, port A2

Entries	390
Mean	43.74
Std Dev	11.88

Turn on : 25.0627

Width : 2.669

Height : 9.998



B1L100S, U5-ch32

calib_packv5_042523_0143.root, FC#4, port A2

Entries	385
Mean	43.95
Std Dev	11.81

Turn on : 25.8099

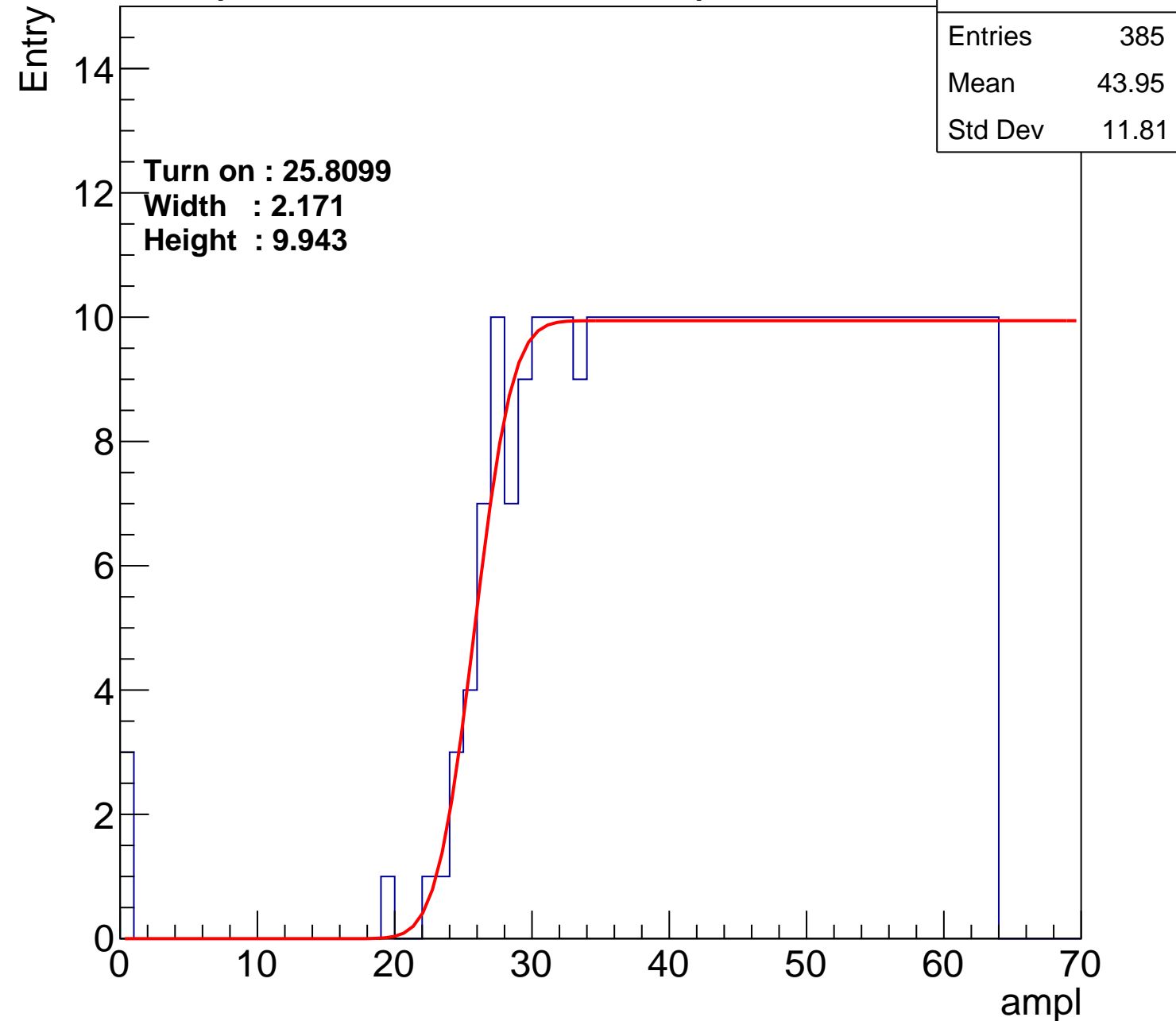
Width : 2.171

Height : 9.943

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch33

calib_packv5_042523_0143.root, FC#4, port A2

Entries	377
Mean	44.37
Std Dev	11.58

Turn on : 26.4068

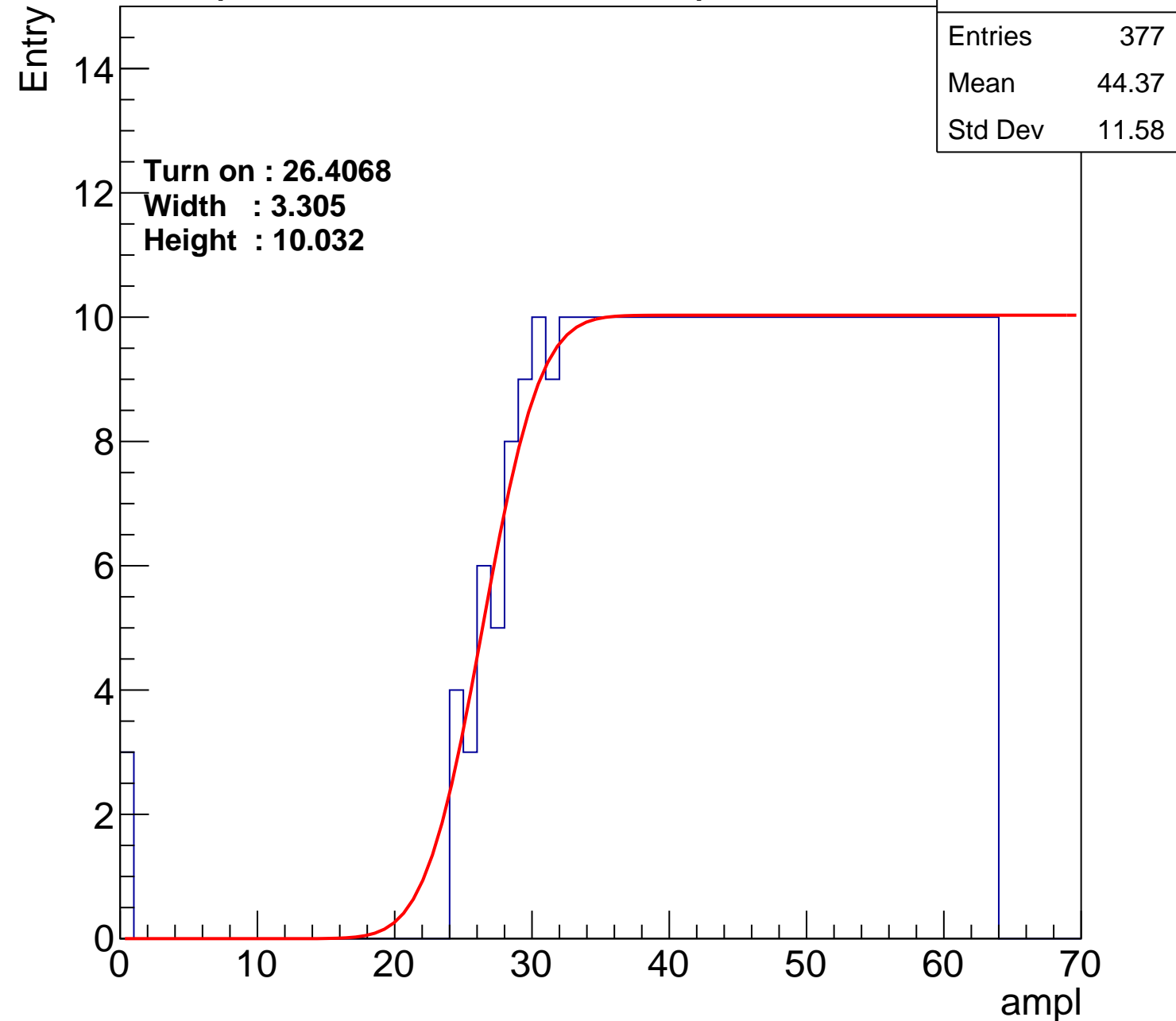
Width : 3.305

Height : 10.032

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch34

calib_packv5_042523_0143.root, FC#4, port A2

Entries	392
Mean	43.67
Std Dev	11.82

Turn on : 25.0502

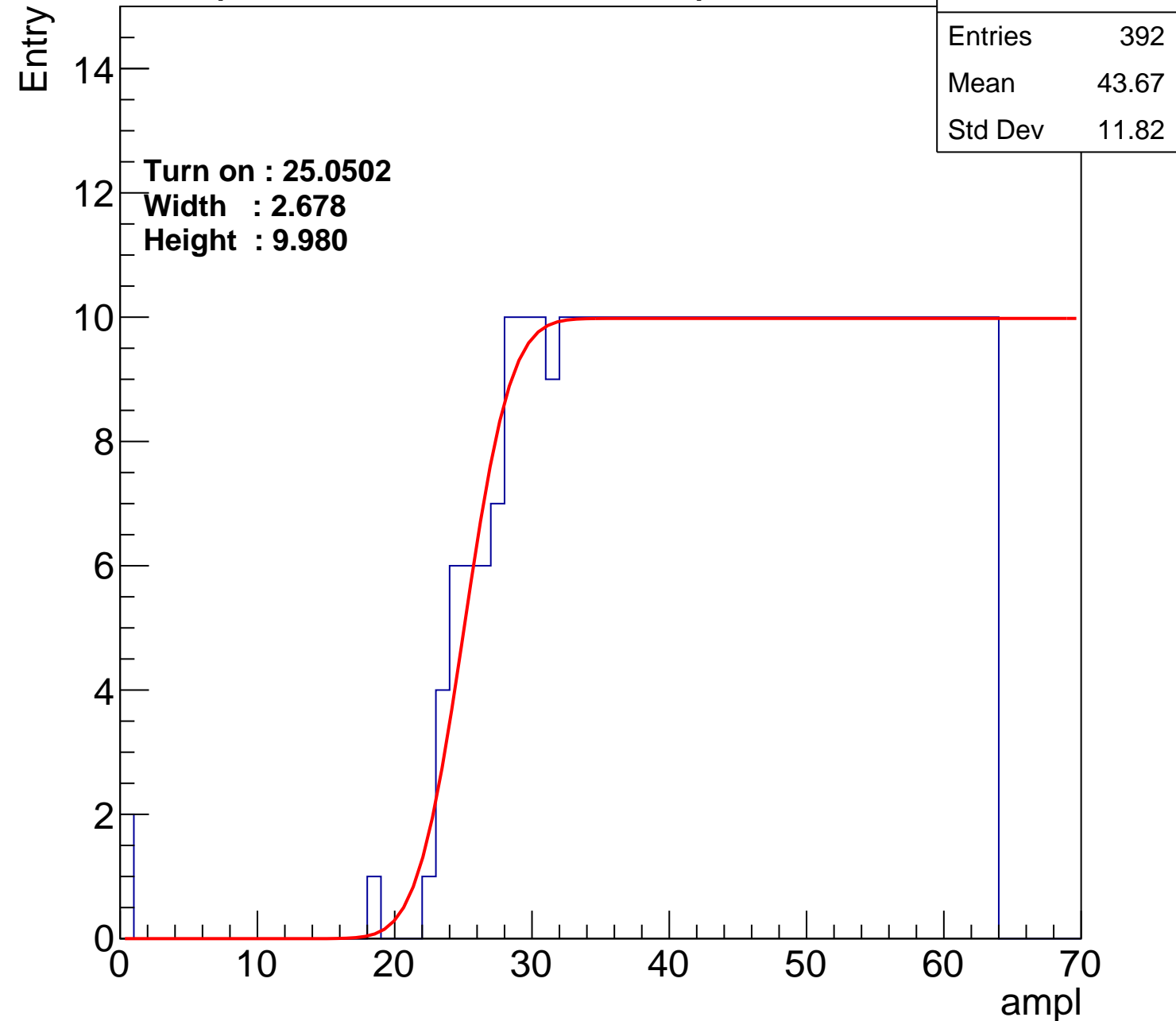
Width : 2.678

Height : 9.980

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch35

calib_packv5_042523_0143.root, FC#4, port A2

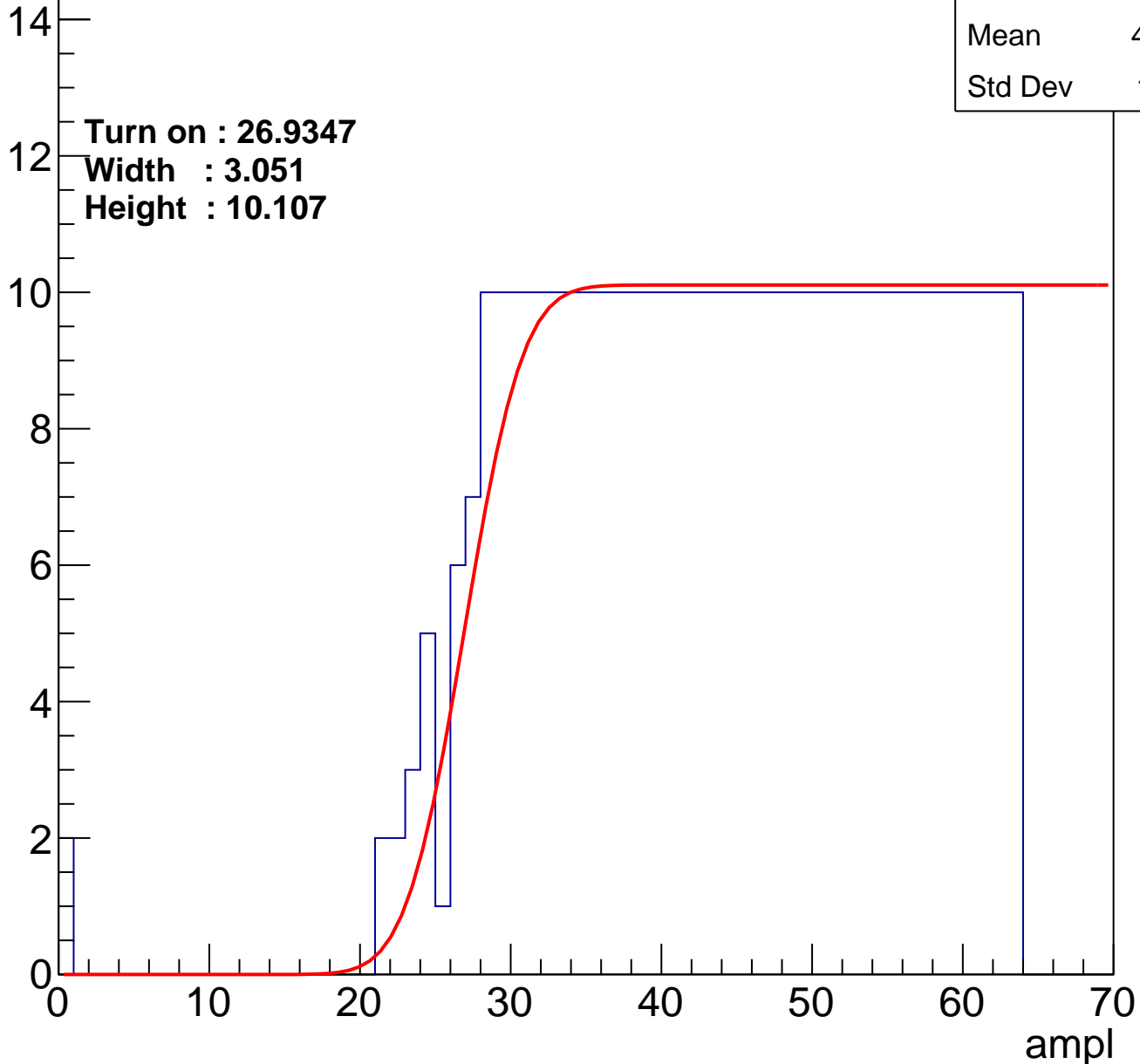
Entries	388
Mean	43.88
Std Dev	11.71

Turn on : 26.9347

Width : 3.051

Height : 10.107

Entry



B1L100S, U5-ch36

calib_packv5_042523_0143.root, FC#4, port A2

Entries	399
Mean	43.3
Std Dev	12.12

Turn on : 24.6961

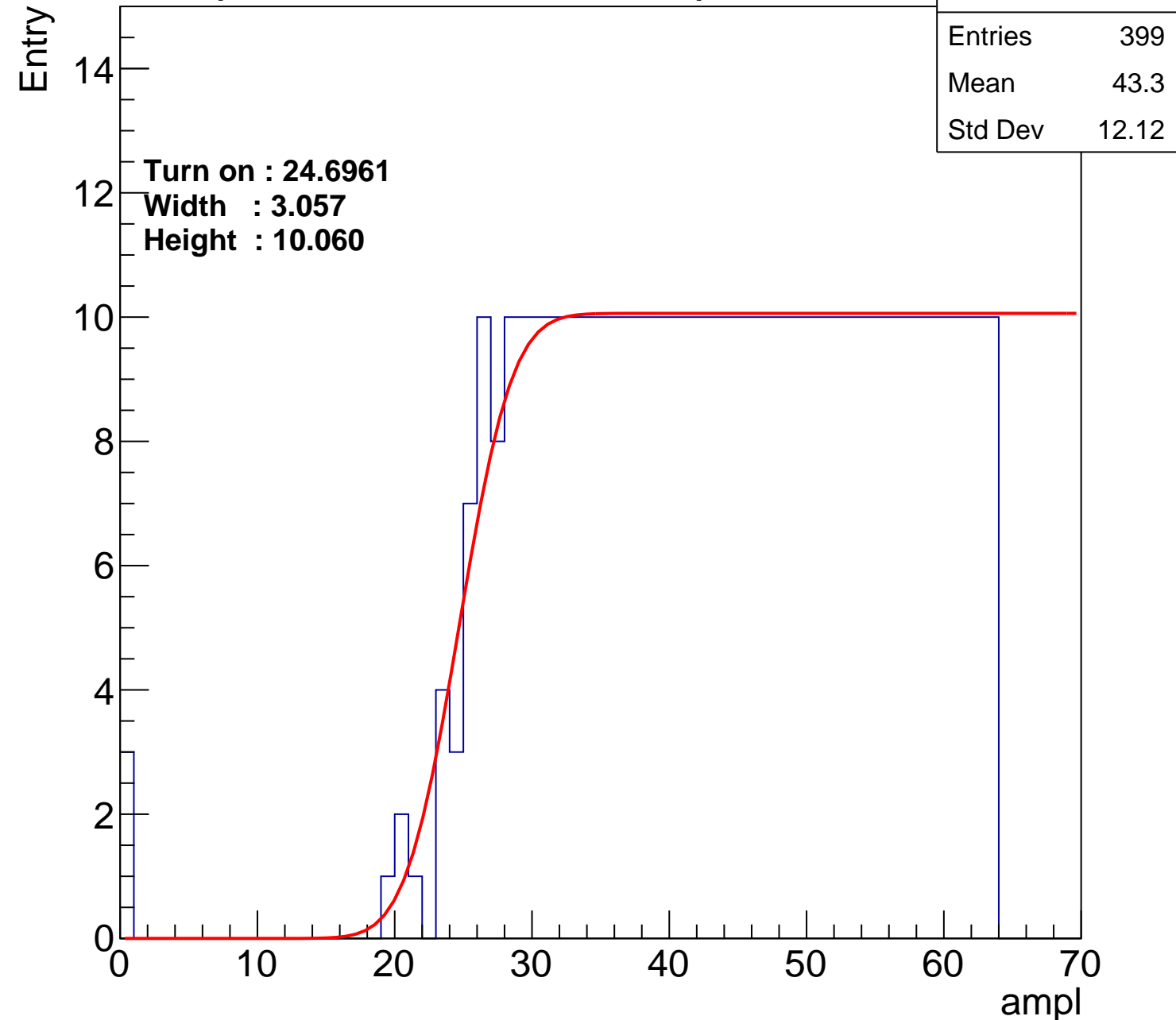
Width : 3.057

Height : 10.060

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch37

calib_packv5_042523_0143.root, FC#4, port A2

Entries	390
Mean	43.87
Std Dev	11.53

Turn on : 24.9729

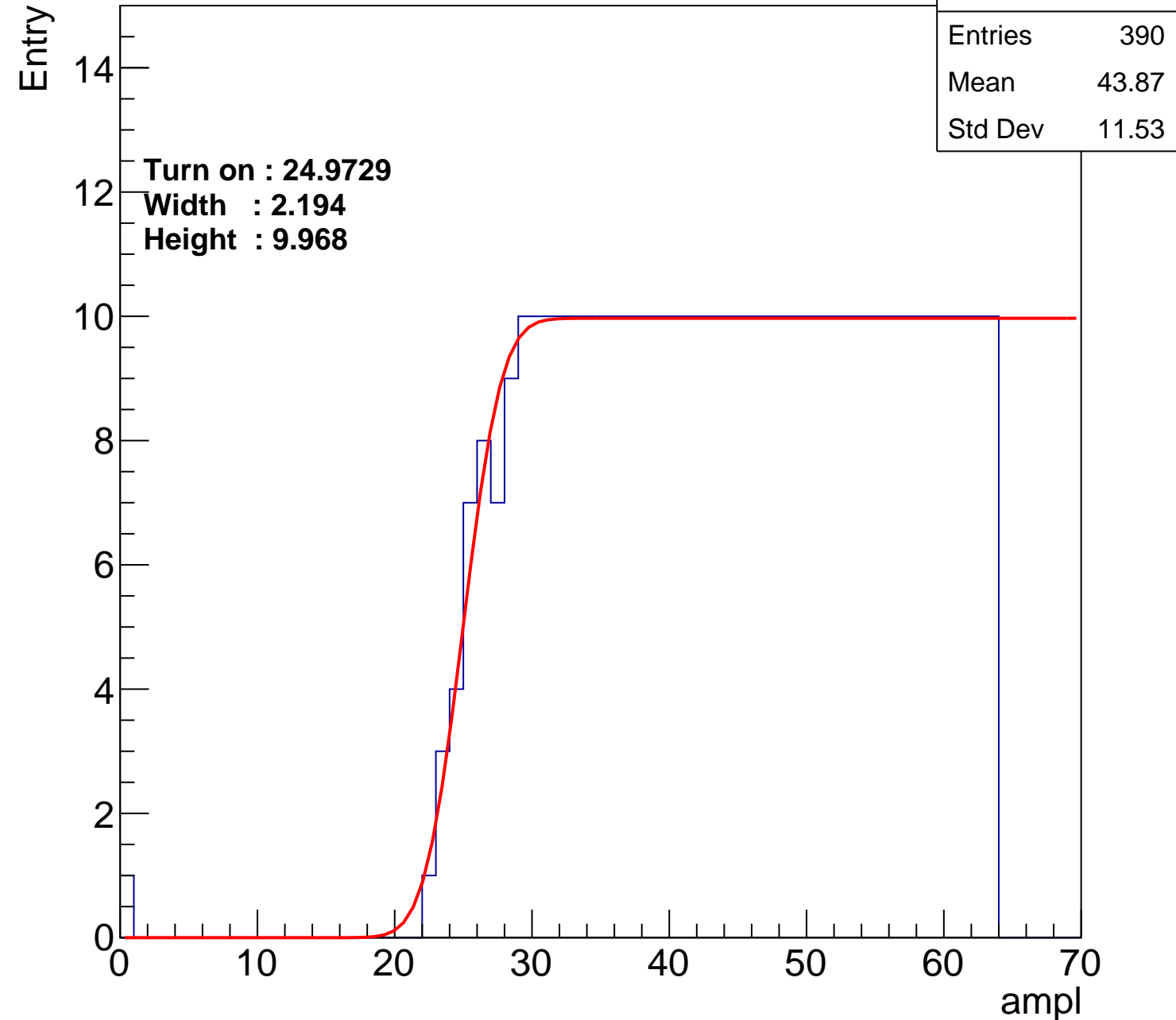
Width : 2.194

Height : 9.968

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch38

calib_packv5_042523_0143.root, FC#4, port A2

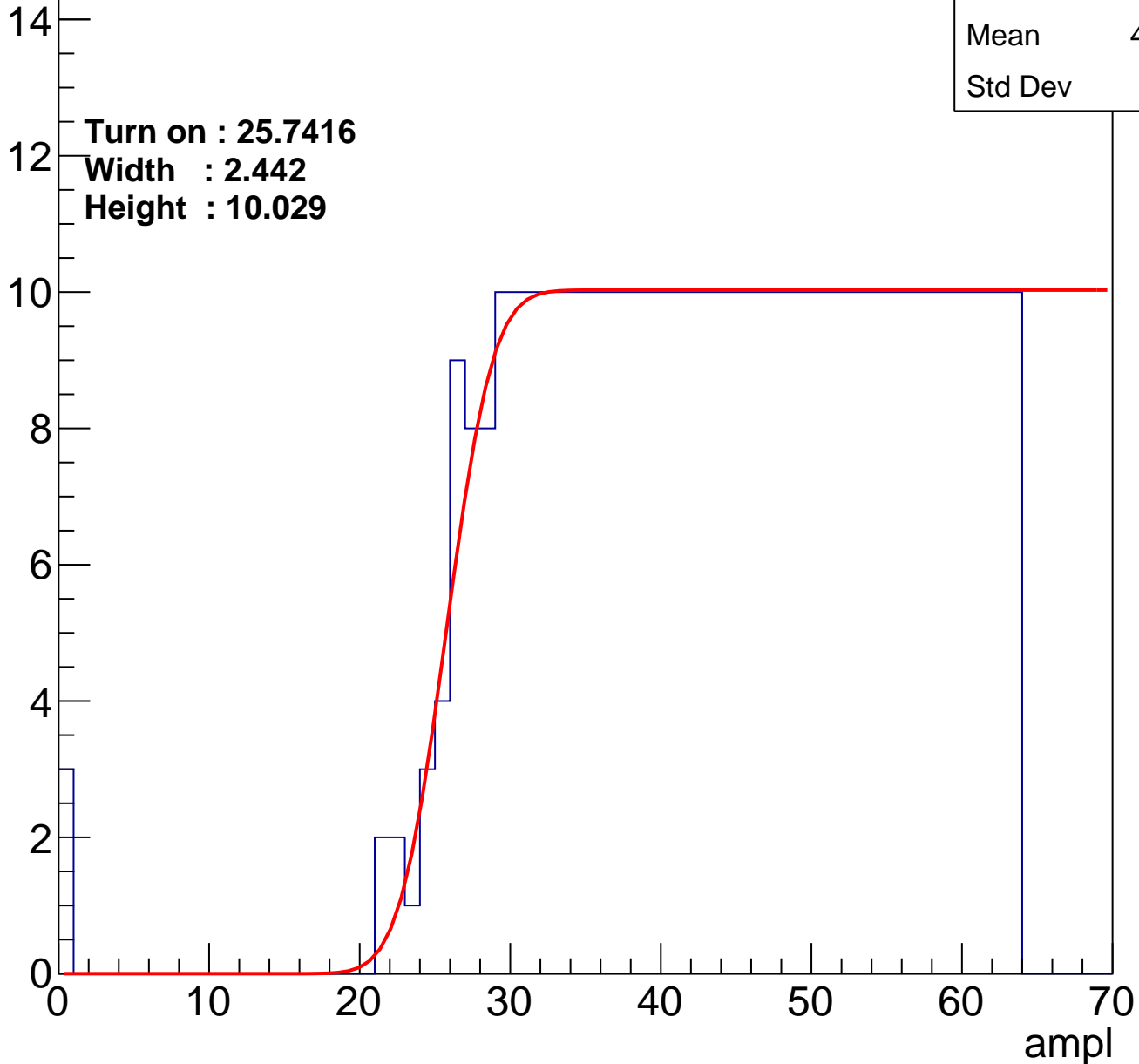
Entries	390
Mean	43.73
Std Dev	11.9

Turn on : 25.7416

Width : 2.442

Height : 10.029

Entry



B1L100S, U5-ch39

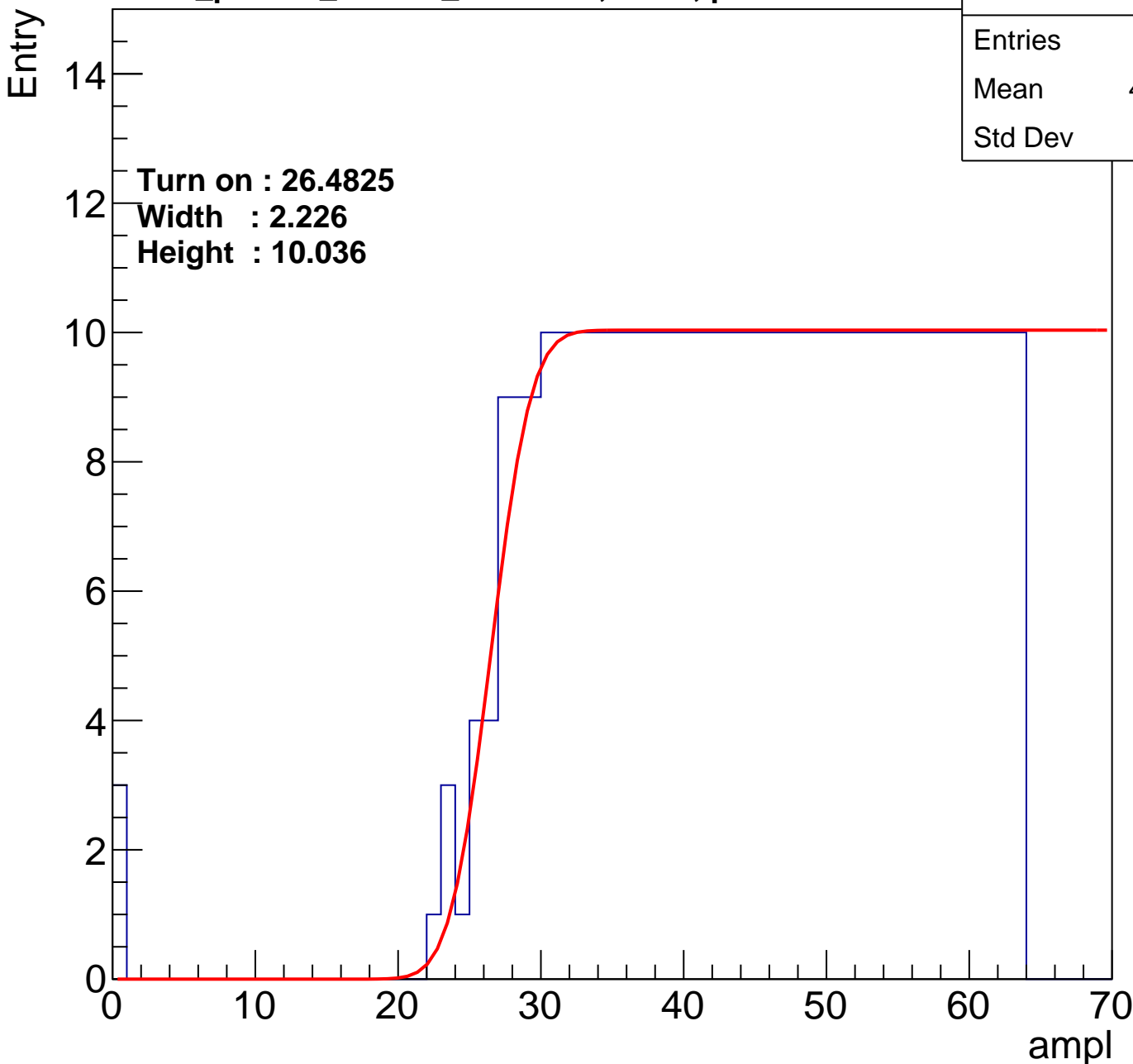
calib_packv5_042523_0143.root, FC#4, port A2

Entries	383
Mean	44.09
Std Dev	11.71

Turn on : 26.4825

Width : 2.226

Height : 10.036



B1L100S, U5-ch40

calib_packv5_042523_0143.root, FC#4, port A2

Entries	402
Mean	43.14
Std Dev	12.2

Turn on : 24.2655

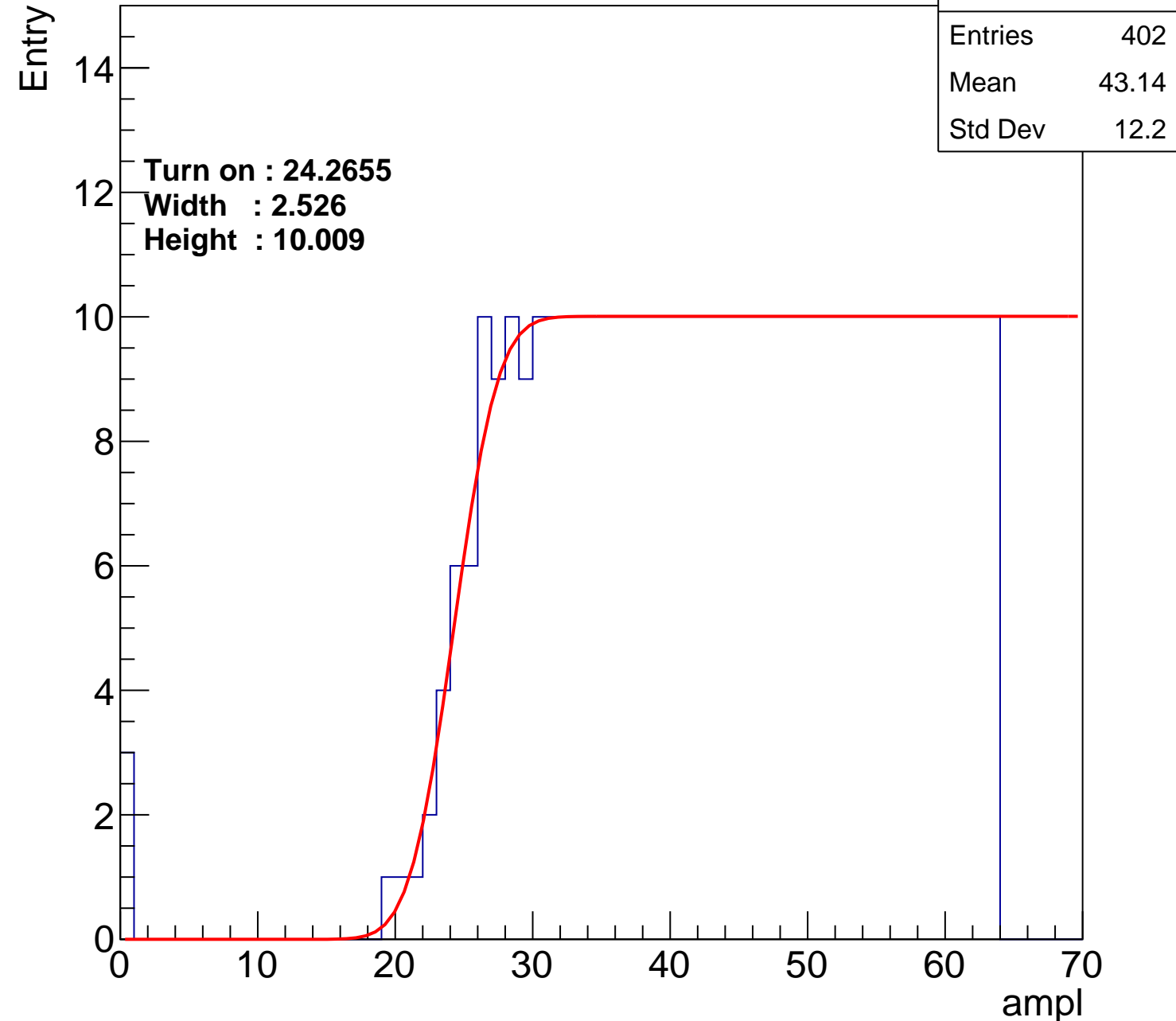
Width : 2.526

Height : 10.009

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch41

calib_packv5_042523_0143.root, FC#4, port A2

Entries	379
Mean	44.41
Std Dev	11.26

Turn on : 26.1265

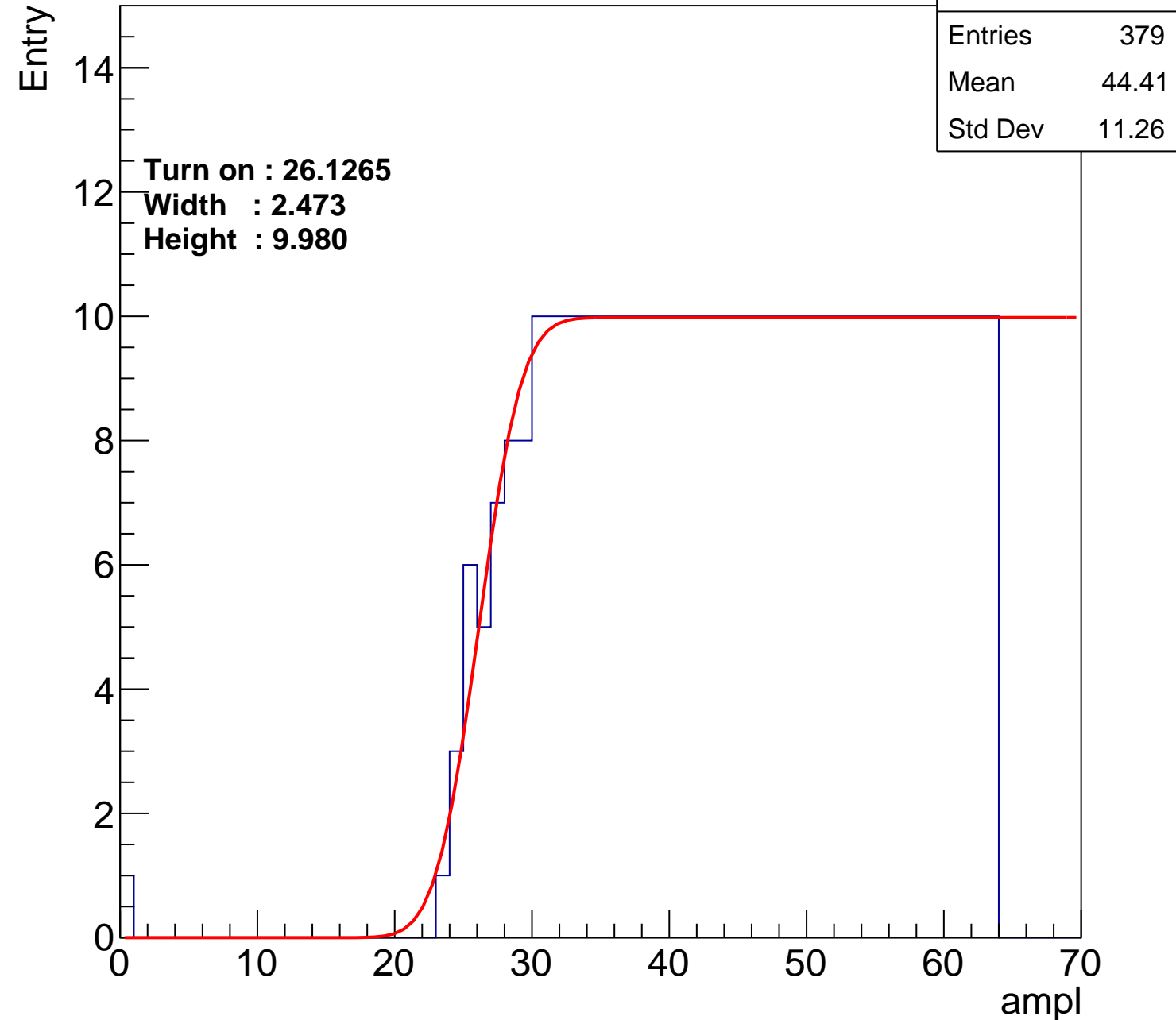
Width : 2.473

Height : 9.980

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch42

calib_packv5_042523_0143.root, FC#4, port A2

Entries	378
Mean	44.38
Std Dev	11.43

Turn on : 26.4623

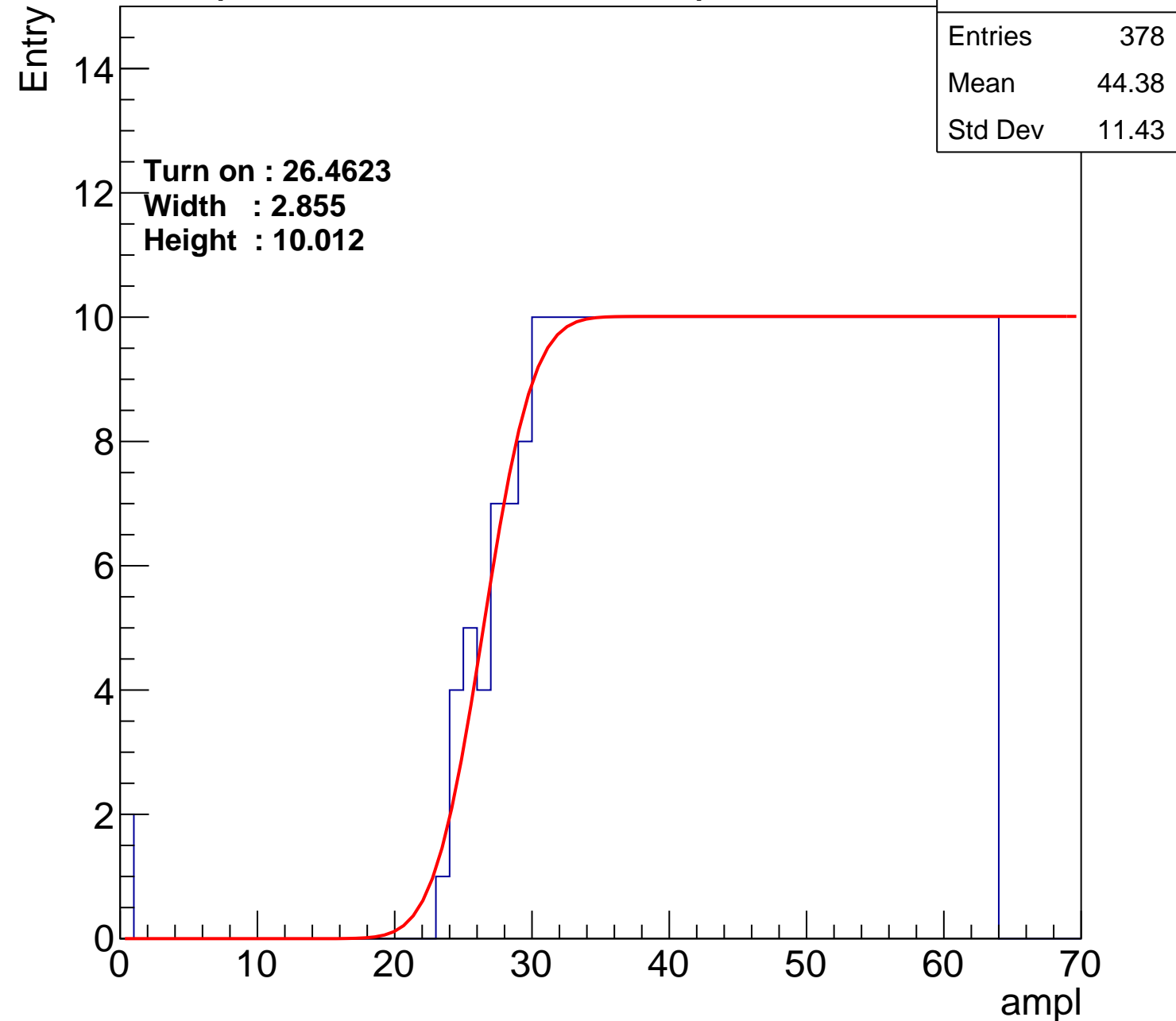
Width : 2.855

Height : 10.012

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch43

calib_packv5_042523_0143.root, FC#4, port A2

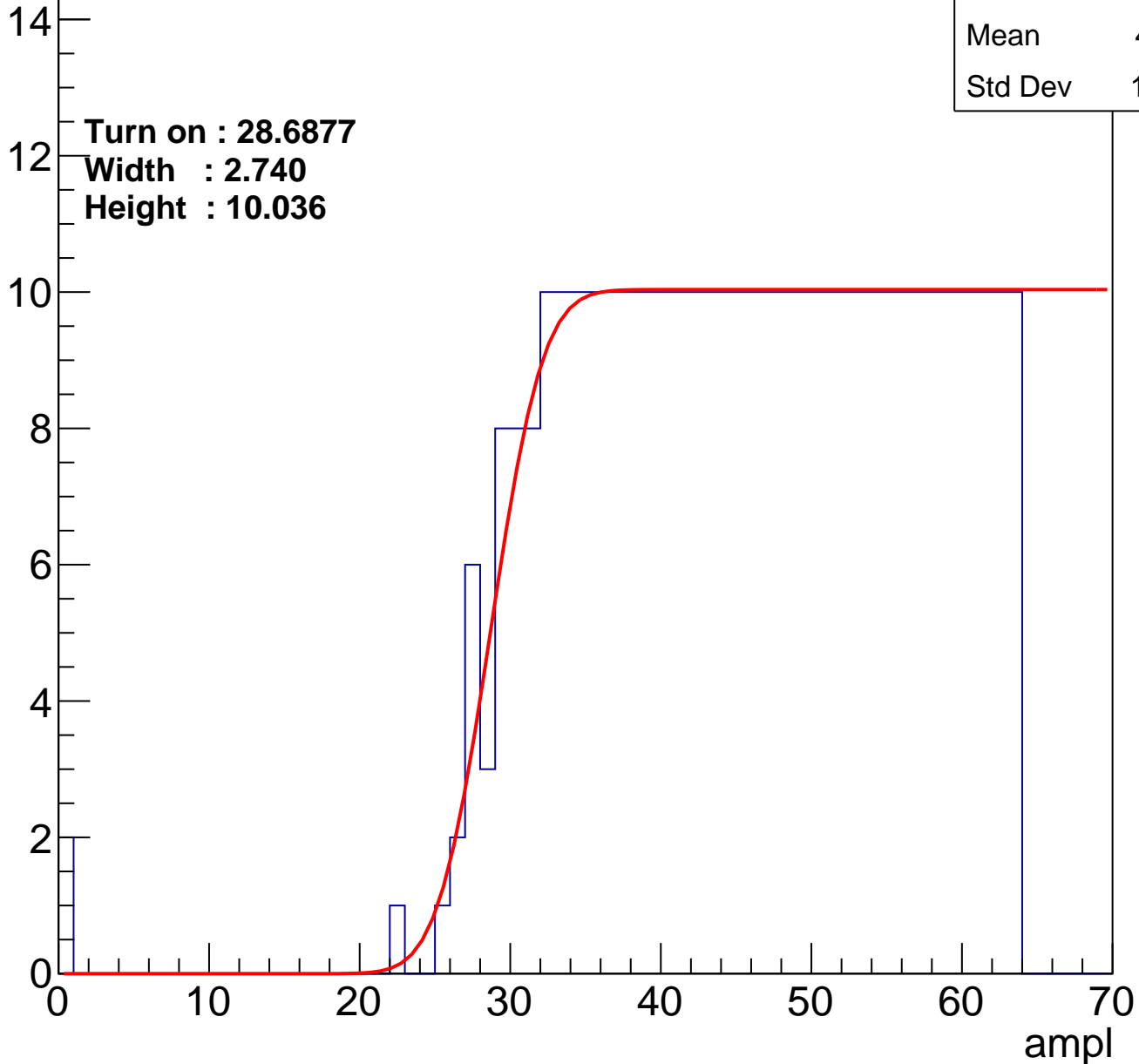
Entries	359
Mean	45.31
Std Dev	10.97

Turn on : 28.6877

Width : 2.740

Height : 10.036

Entry



B1L100S, U5-ch44

calib_packv5_042523_0143.root, FC#4, port A2

Entries	389
Mean	43.59
Std Dev	12.37

Turn on : 26.1731

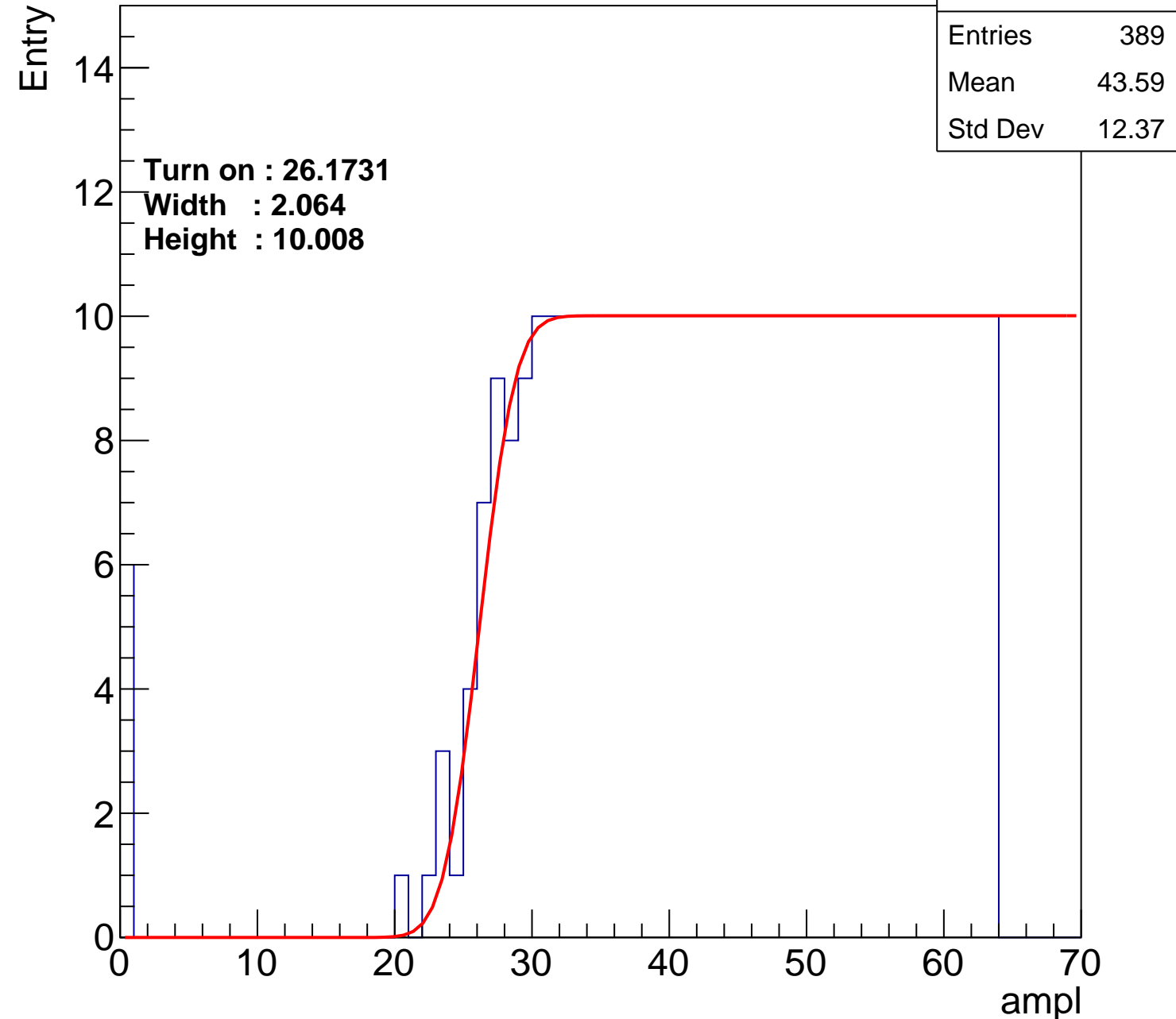
Width : 2.064

Height : 10.008

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch45

calib_packv5_042523_0143.root, FC#4, port A2

Entries	379
Mean	44.1
Std Dev	12.04

Turn on : 26.8702

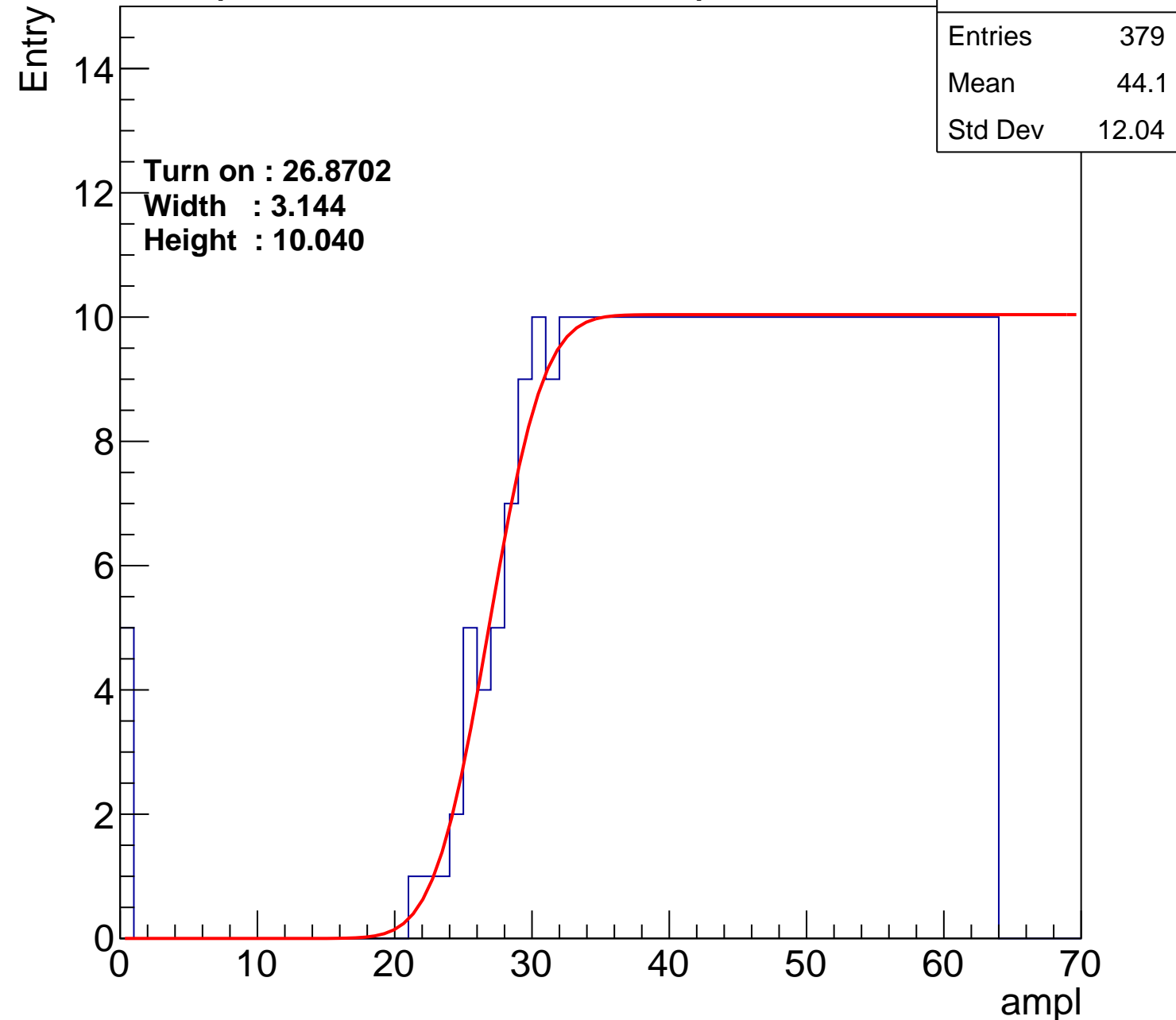
Width : 3.144

Height : 10.040

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch46

calib_packv5_042523_0143.root, FC#4, port A2

Entries	376
Mean	44.31
Std Dev	11.74

Turn on : 27.3768

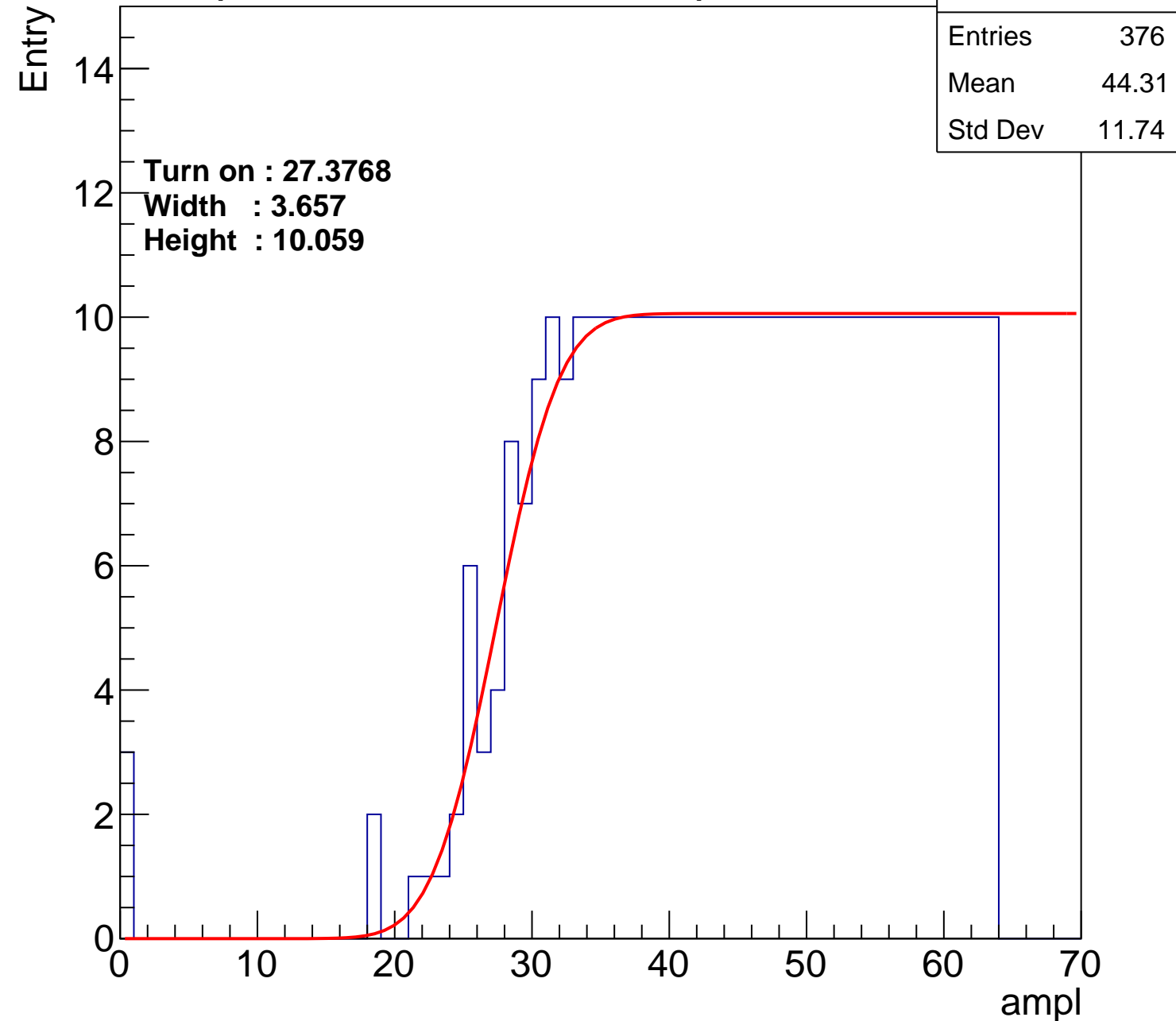
Width : 3.657

Height : 10.059

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch47

calib_packv5_042523_0143.root, FC#4, port A2

Entries	367
Mean	44.94
Std Dev	11.04

Turn on : 27.7785

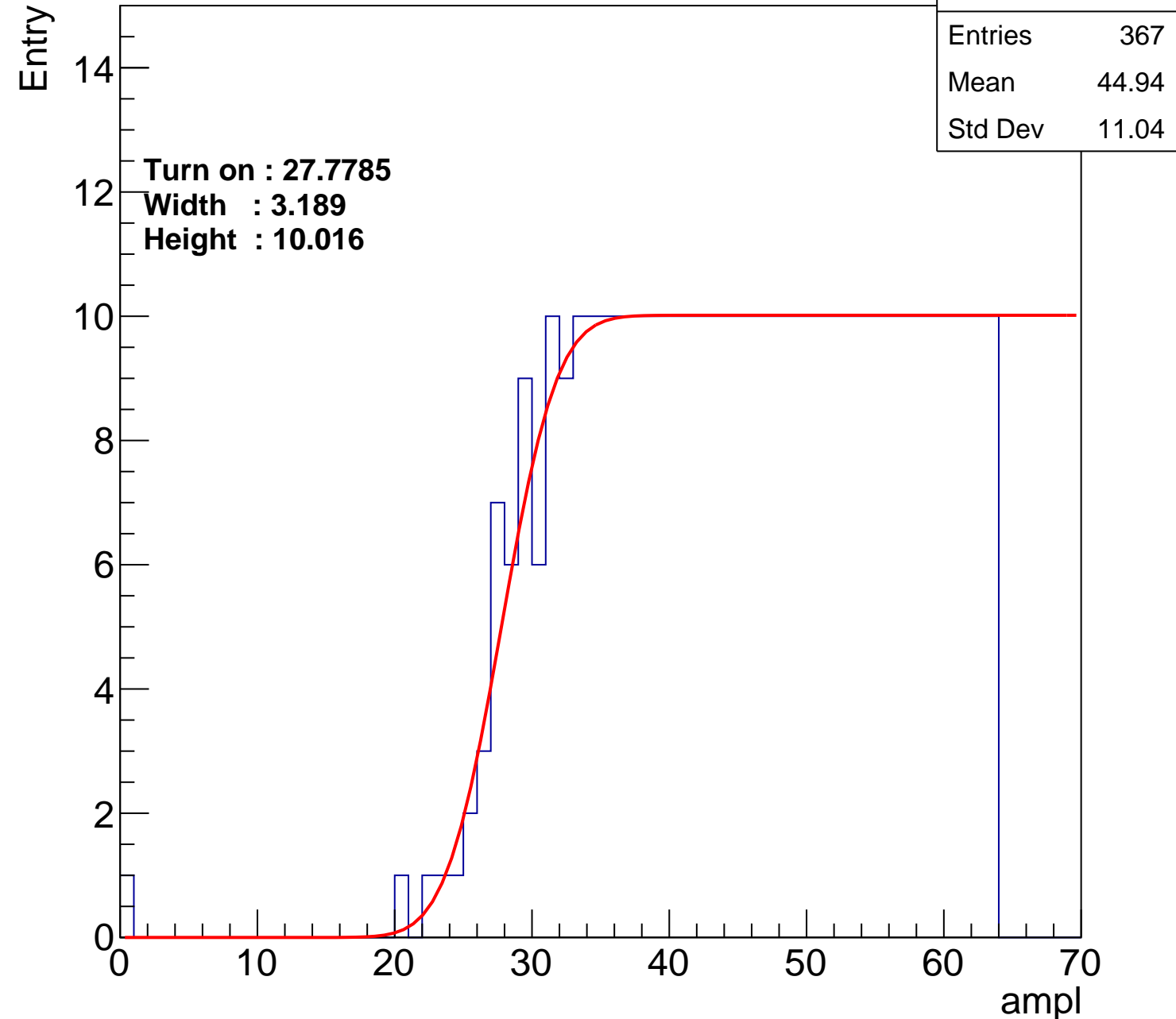
Width : 3.189

Height : 10.016

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch48

calib_packv5_042523_0143.root, FC#4, port A2

Entries	364
Mean	45.11
Std Dev	10.92

Turn on : 27.7831

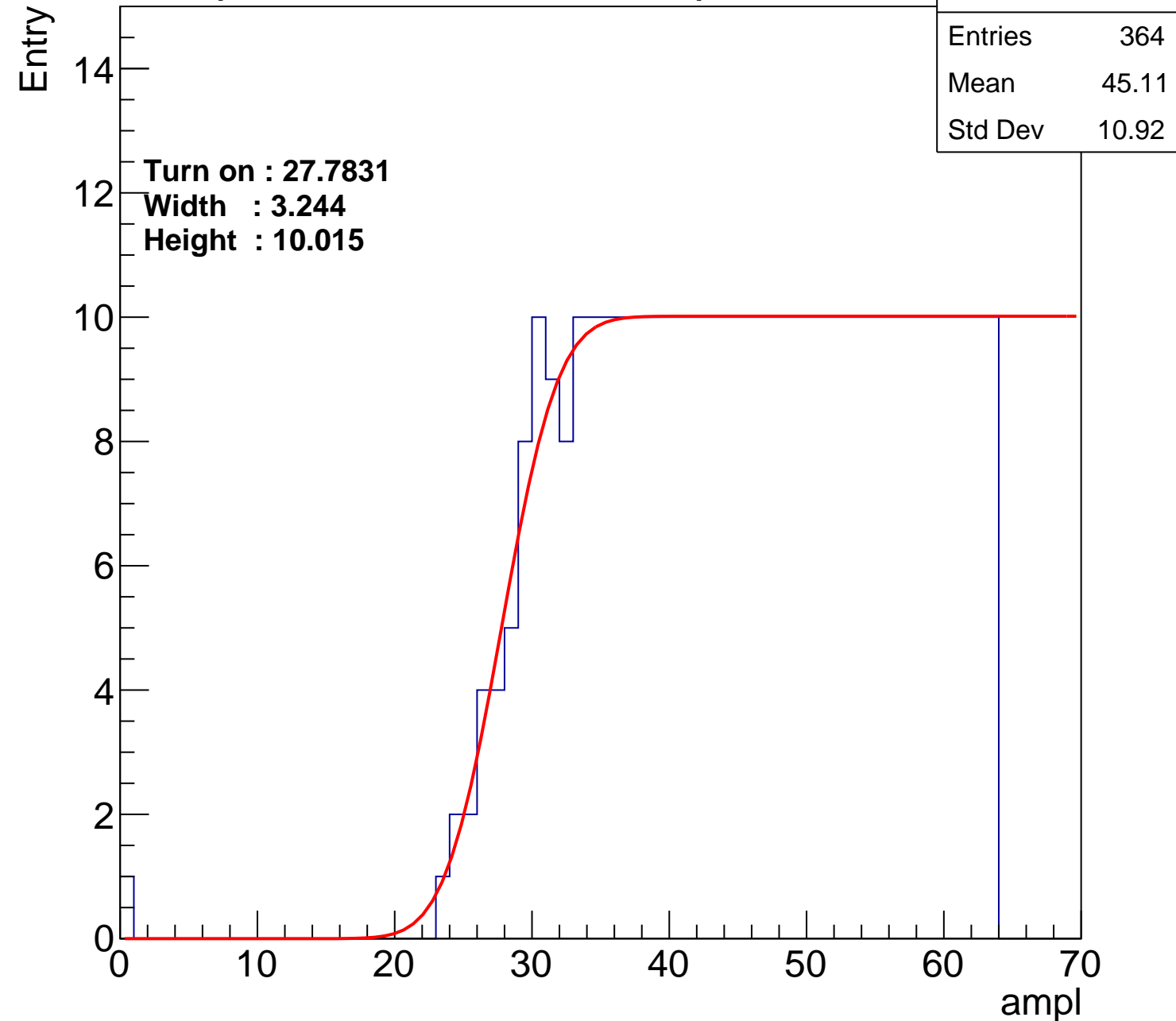
Width : 3.244

Height : 10.015

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch49

calib_packv5_042523_0143.root, FC#4, port A2

Entries	390
Mean	43.78
Std Dev	11.75

Turn on : 24.9126

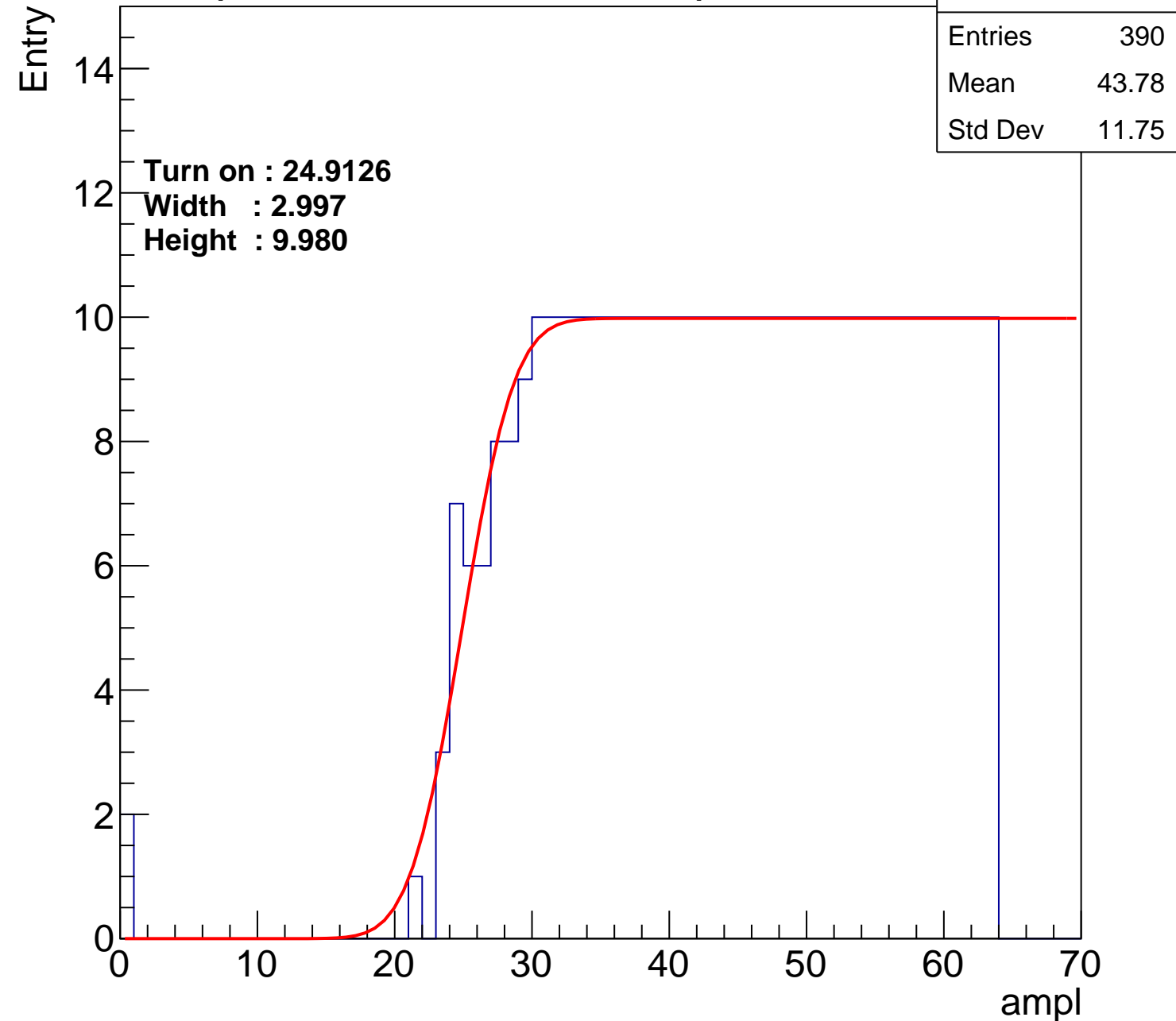
Width : 2.997

Height : 9.980

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch50

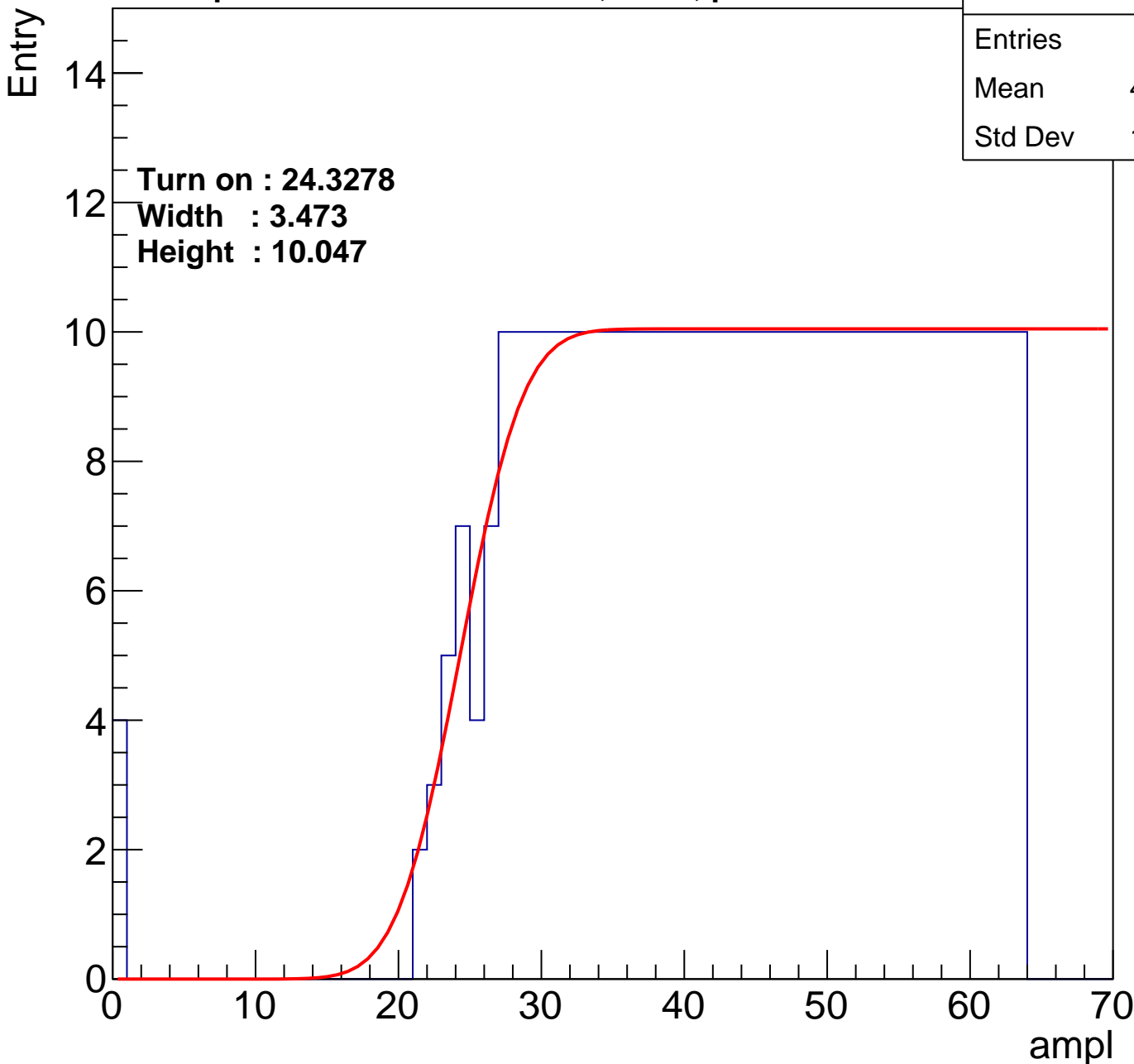
calib_packv5_042523_0143.root, FC#4, port A2

Entries	402
Mean	43.09
Std Dev	12.34

Turn on : 24.3278

Width : 3.473

Height : 10.047



B1L100S, U5-ch51

calib_packv5_042523_0143.root, FC#4, port A2

Entries	370
Mean	44.55
Std Dev	11.82

Turn on : 27.6985

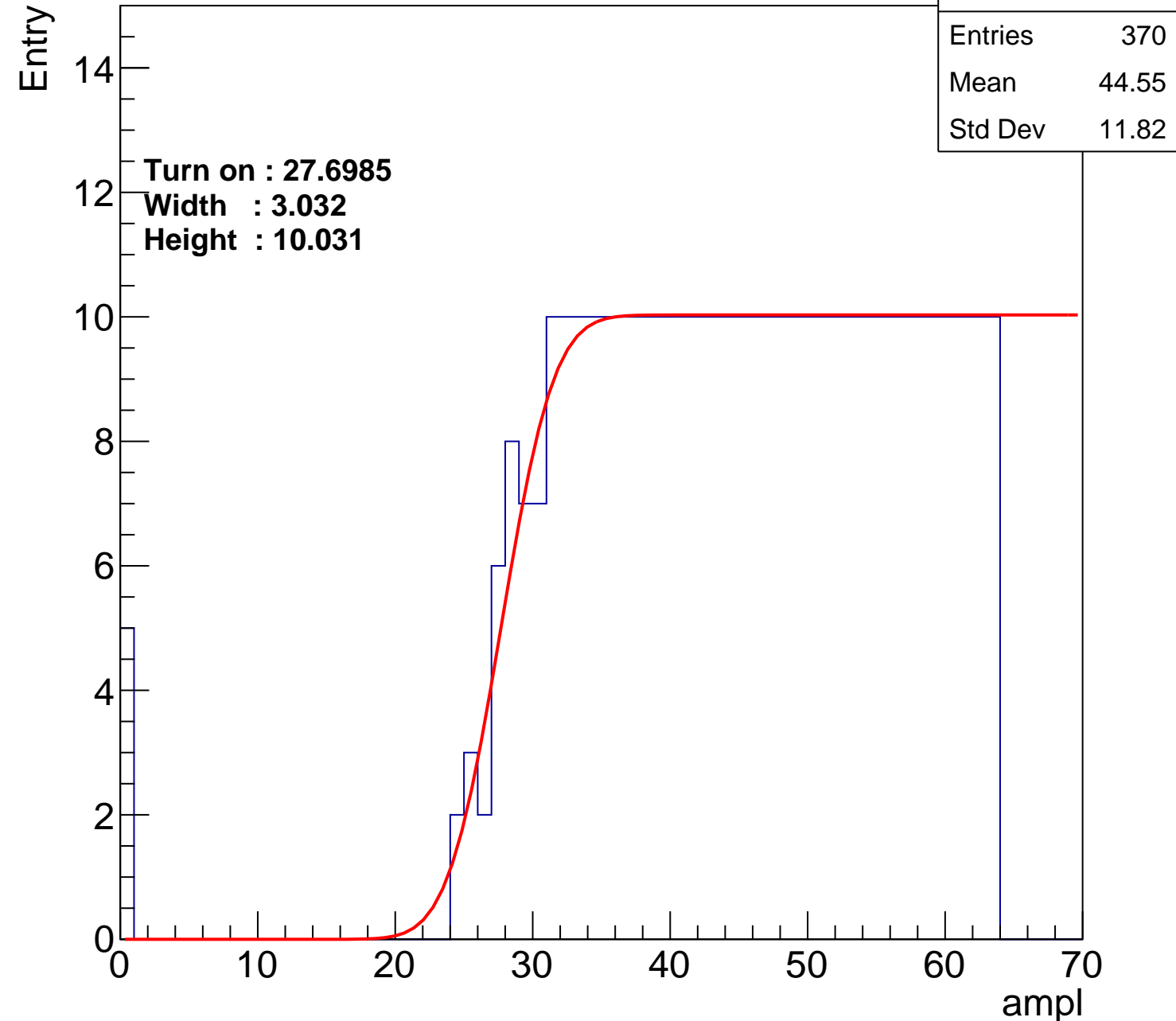
Width : 3.032

Height : 10.031

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch52

calib_packv5_042523_0143.root, FC#4, port A2

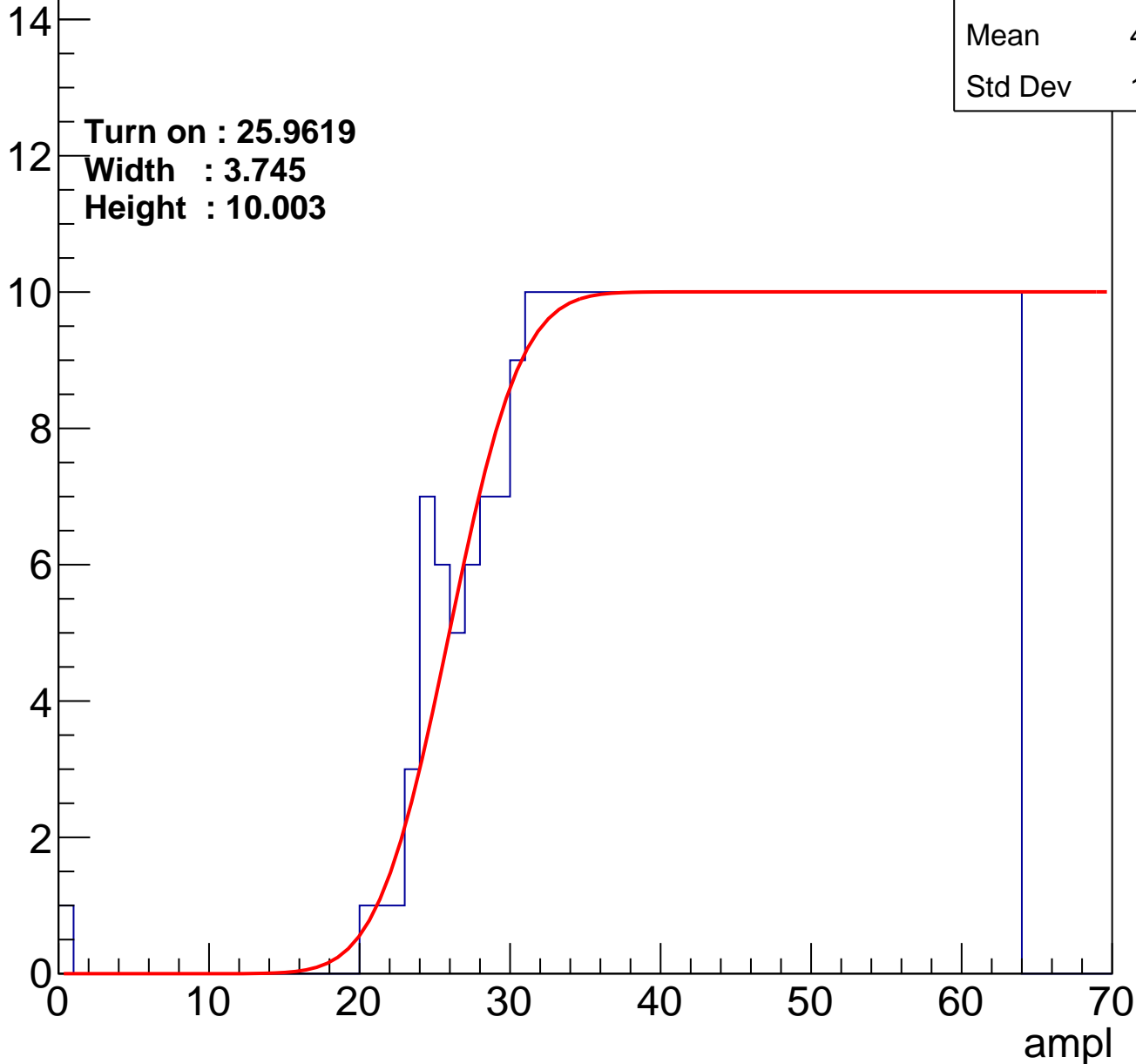
Entries	384
Mean	44.07
Std Dev	11.55

Turn on : 25.9619

Width : 3.745

Height : 10.003

Entry



B1L100S, U5-ch53

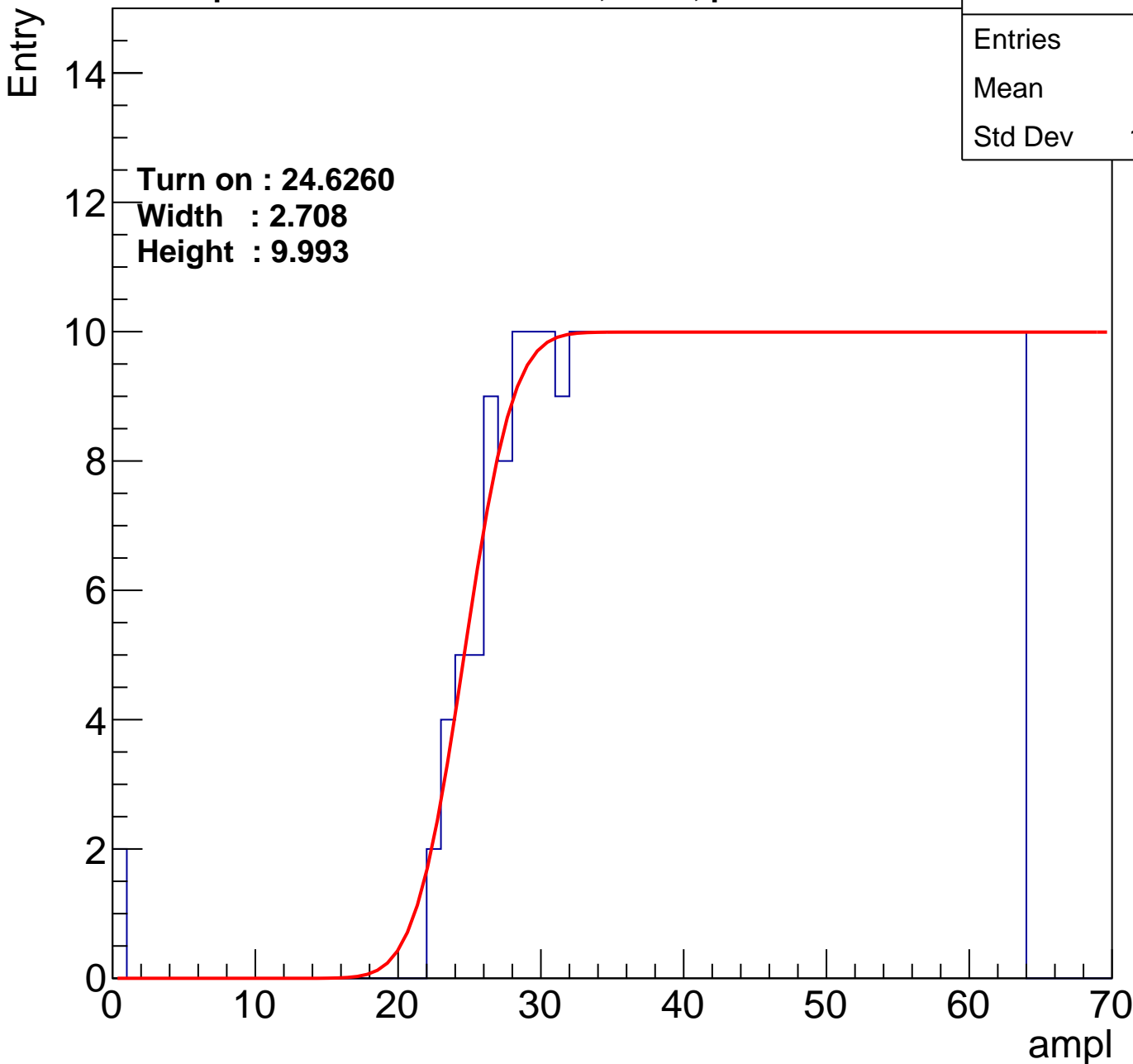
calib_packv5_042523_0143.root, FC#4, port A2

Entries	394
Mean	43.6
Std Dev	11.82

Turn on : 24.6260

Width : 2.708

Height : 9.993



B1L100S, U5-ch54

calib_packv5_042523_0143.root, FC#4, port A2

Entries	373
Mean	44.69
Std Dev	11.13

Turn on : 26.9555

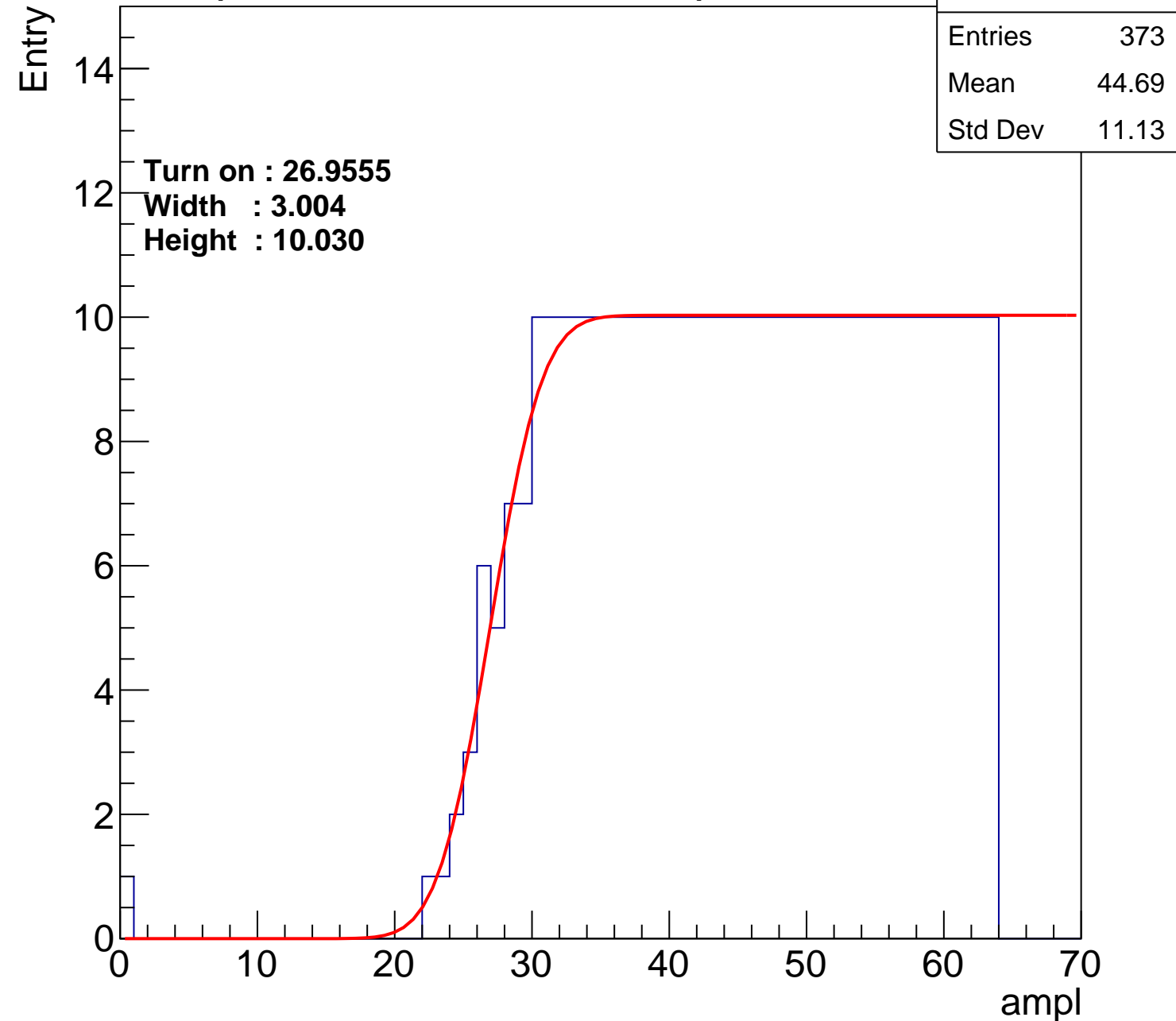
Width : 3.004

Height : 10.030

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch55

calib_packv5_042523_0143.root, FC#4, port A2

Entries	385
Mean	43.98
Std Dev	11.77

Turn on : 25.6451

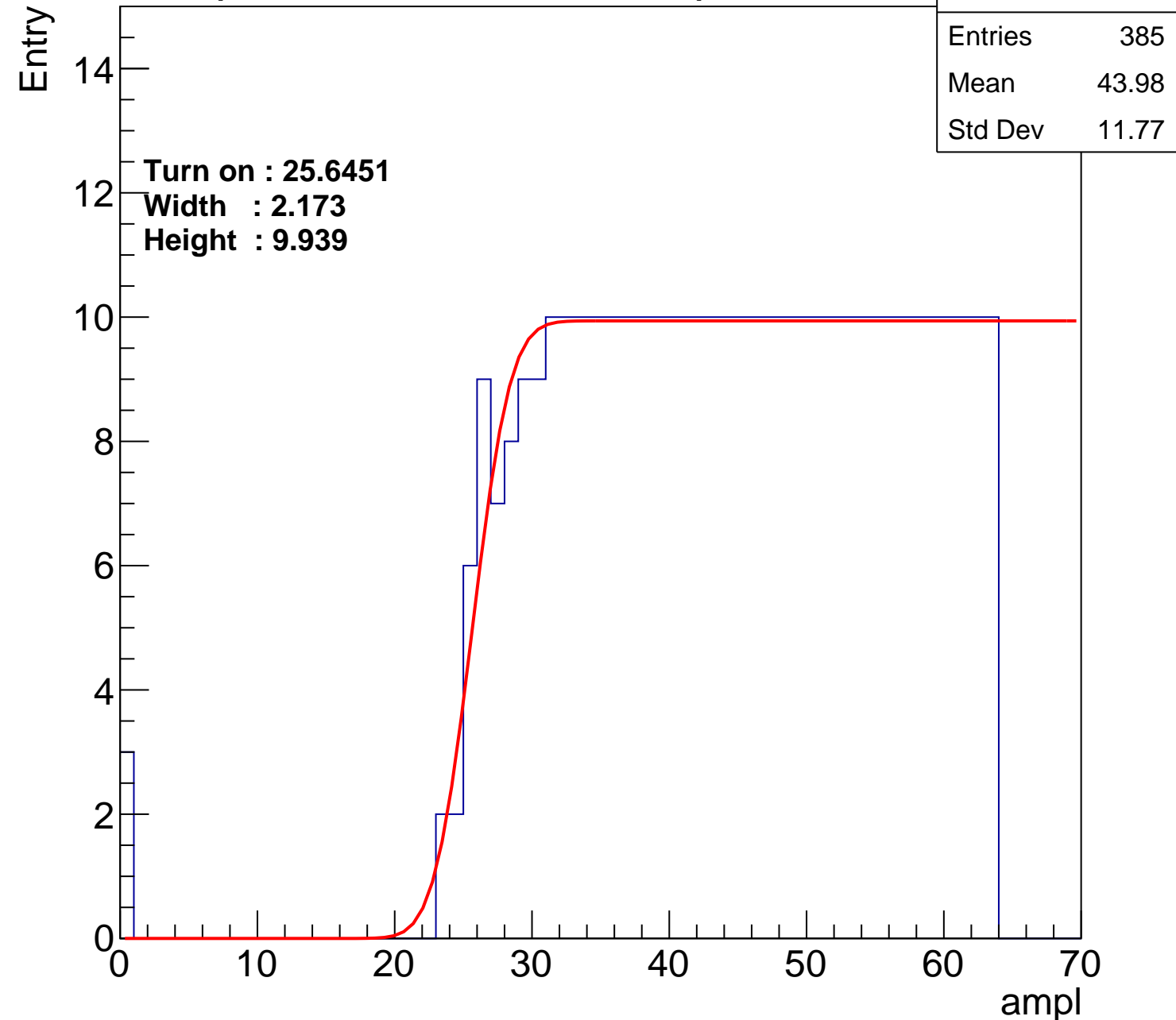
Width : 2.173

Height : 9.939

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch56

calib_packv5_042523_0143.root, FC#4, port A2

Entries	380
Mean	44.37
Std Dev	11.27

Turn on : 26.5161

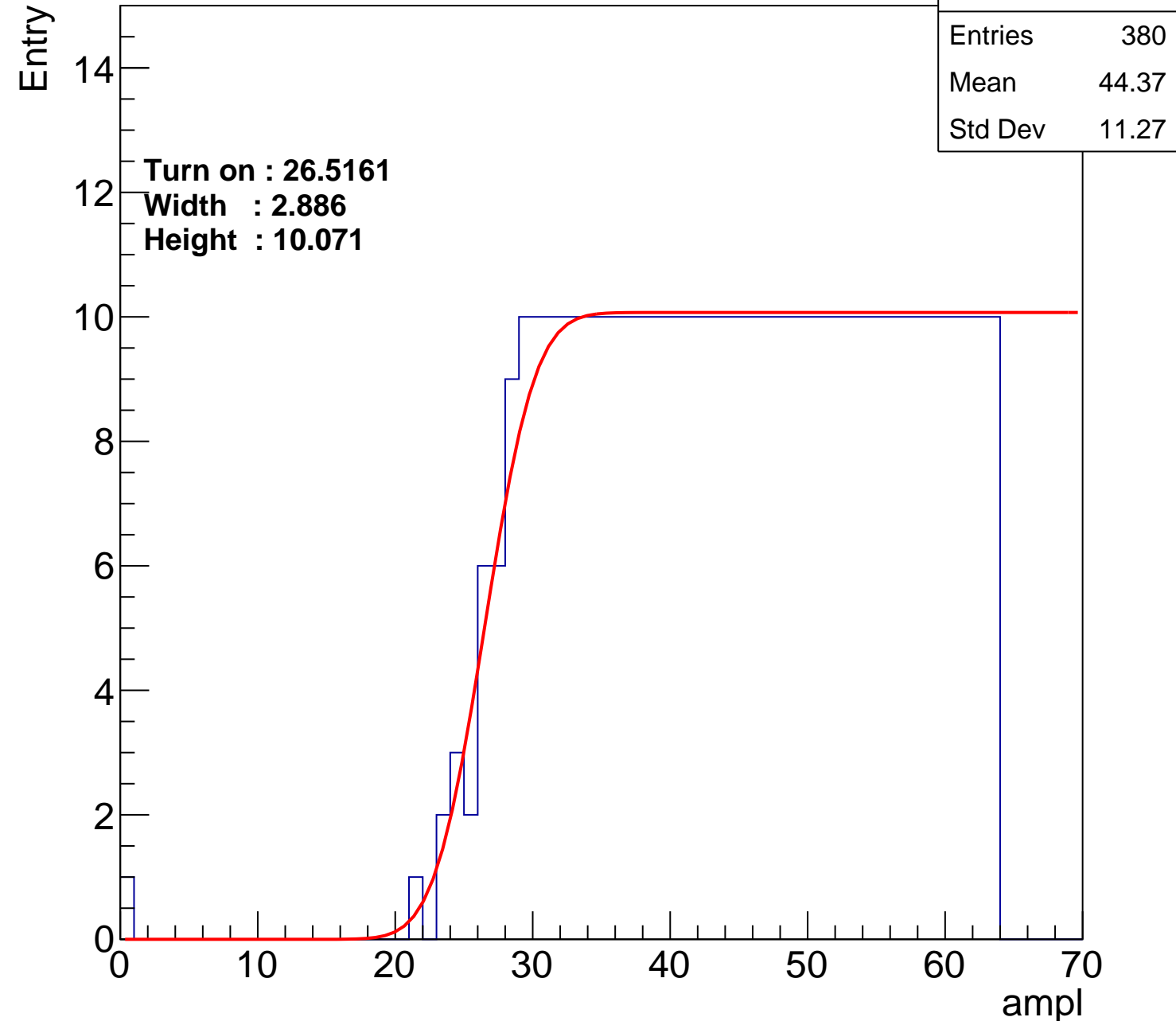
Width : 2.886

Height : 10.071

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch57

calib_packv5_042523_0143.root, FC#4, port A2

Entries	381
Mean	44.03
Std Dev	12.05

Turn on : 26.3092

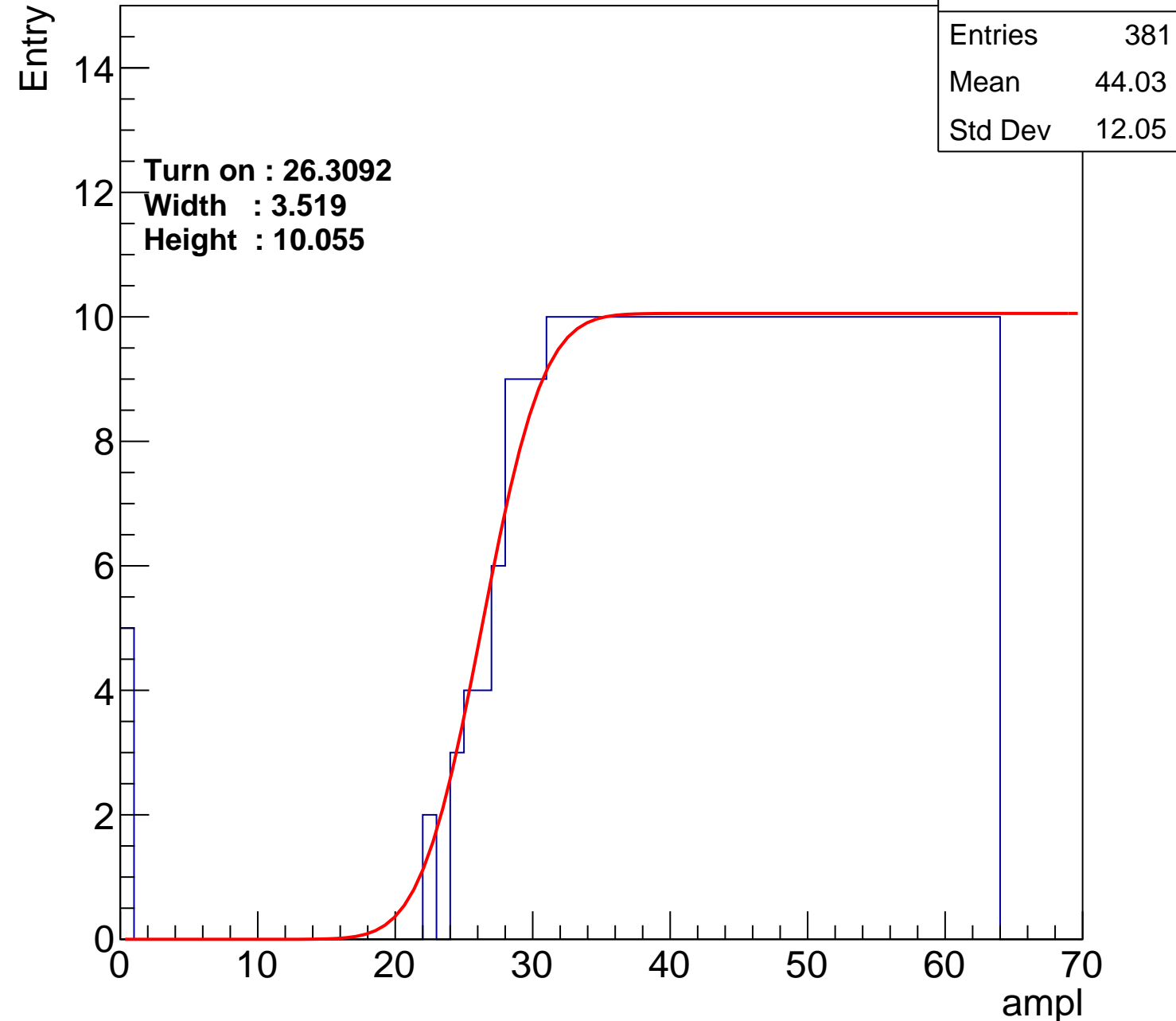
Width : 3.519

Height : 10.055

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch58

calib_packv5_042523_0143.root, FC#4, port A2

Entries	391
Mean	43.7
Std Dev	11.83

Turn on : 24.9113

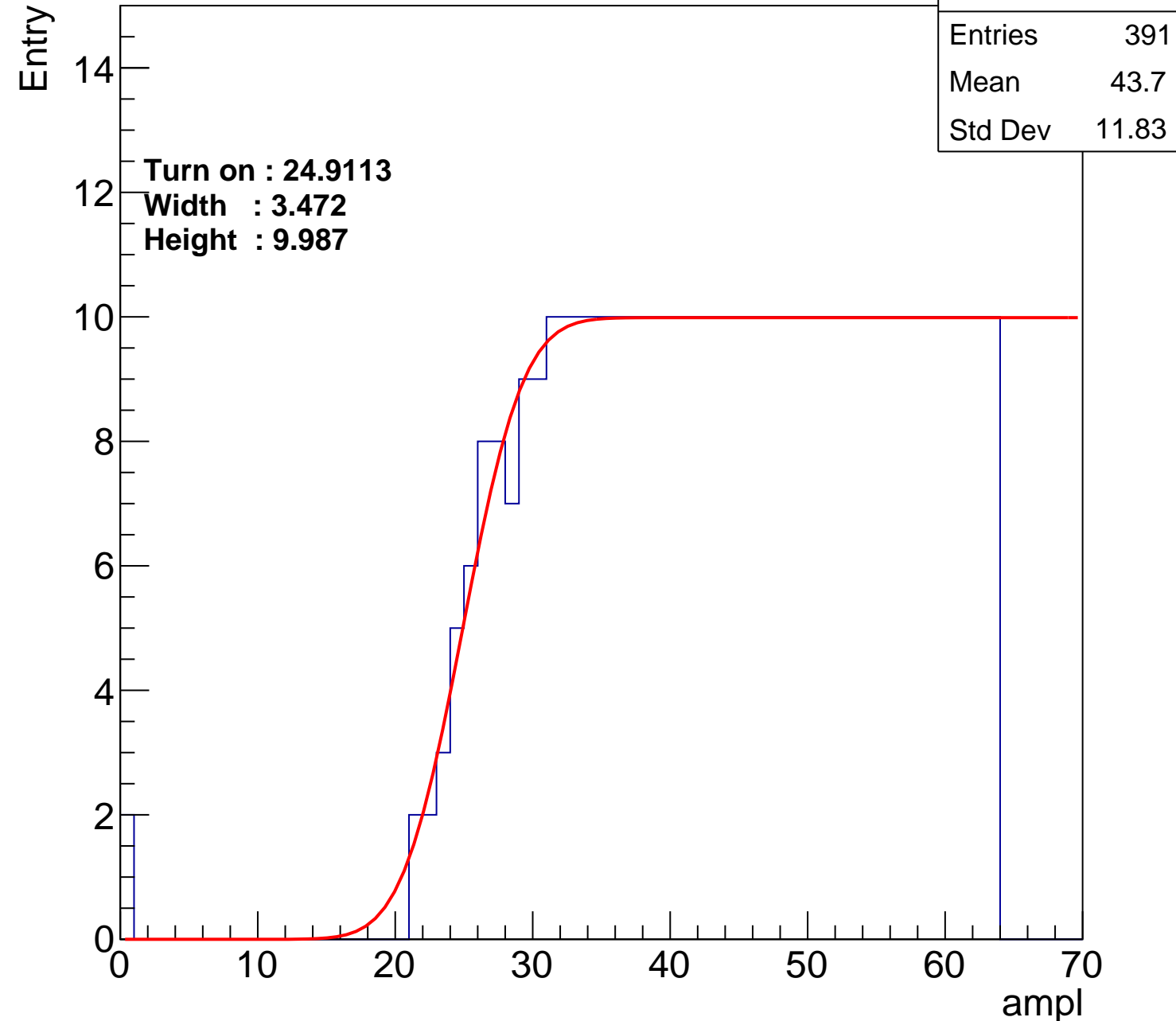
Width : 3.472

Height : 9.987

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch59

calib_packv5_042523_0143.root, FC#4, port A2

Entries	386
Mean	43.83
Std Dev	12.03

Turn on : 25.9537

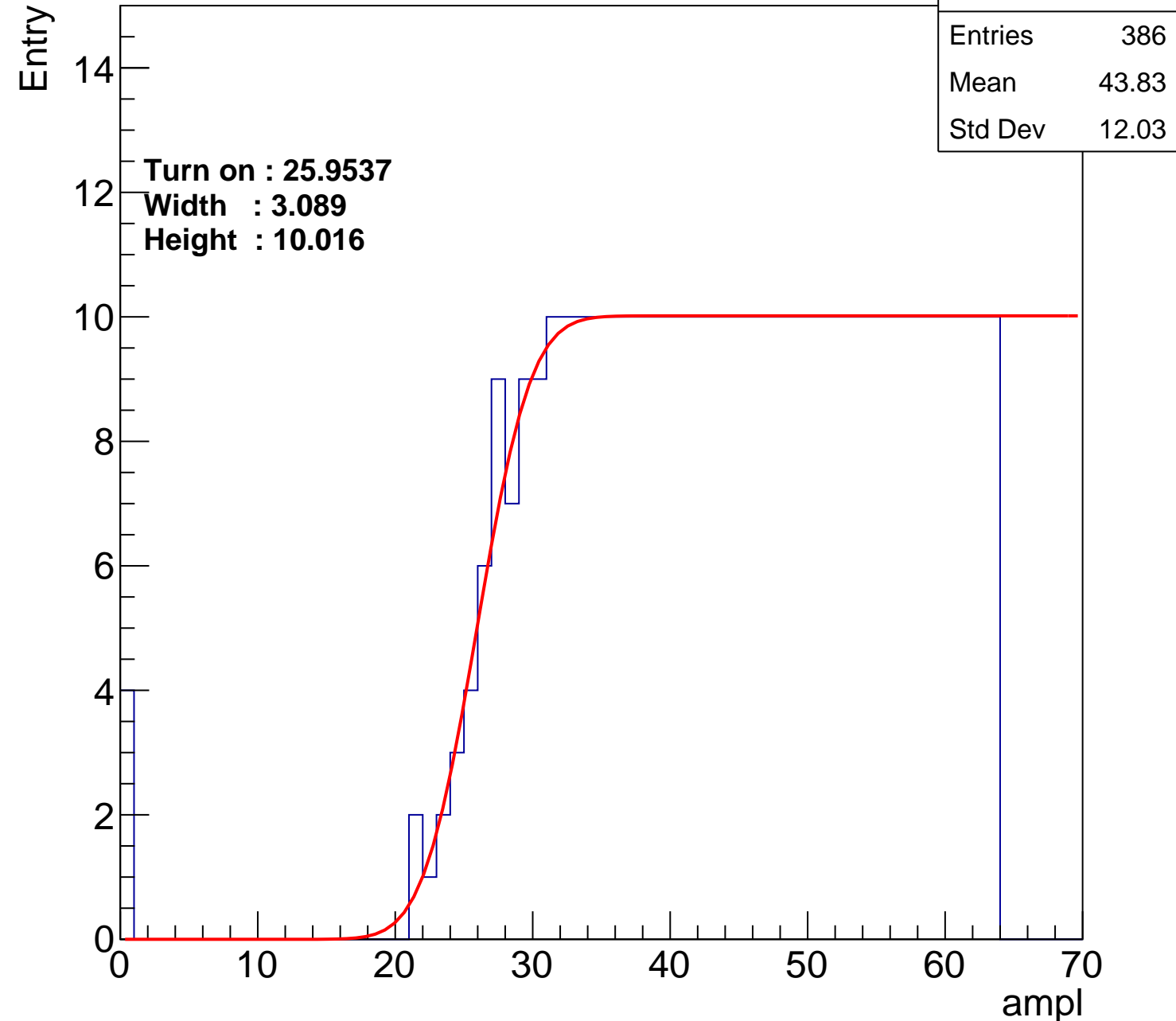
Width : 3.089

Height : 10.016

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch60

calib_packv5_042523_0143.root, FC#4, port A2

Entries	404
Mean	42.96
Std Dev	12.45

Turn on : 24.3681

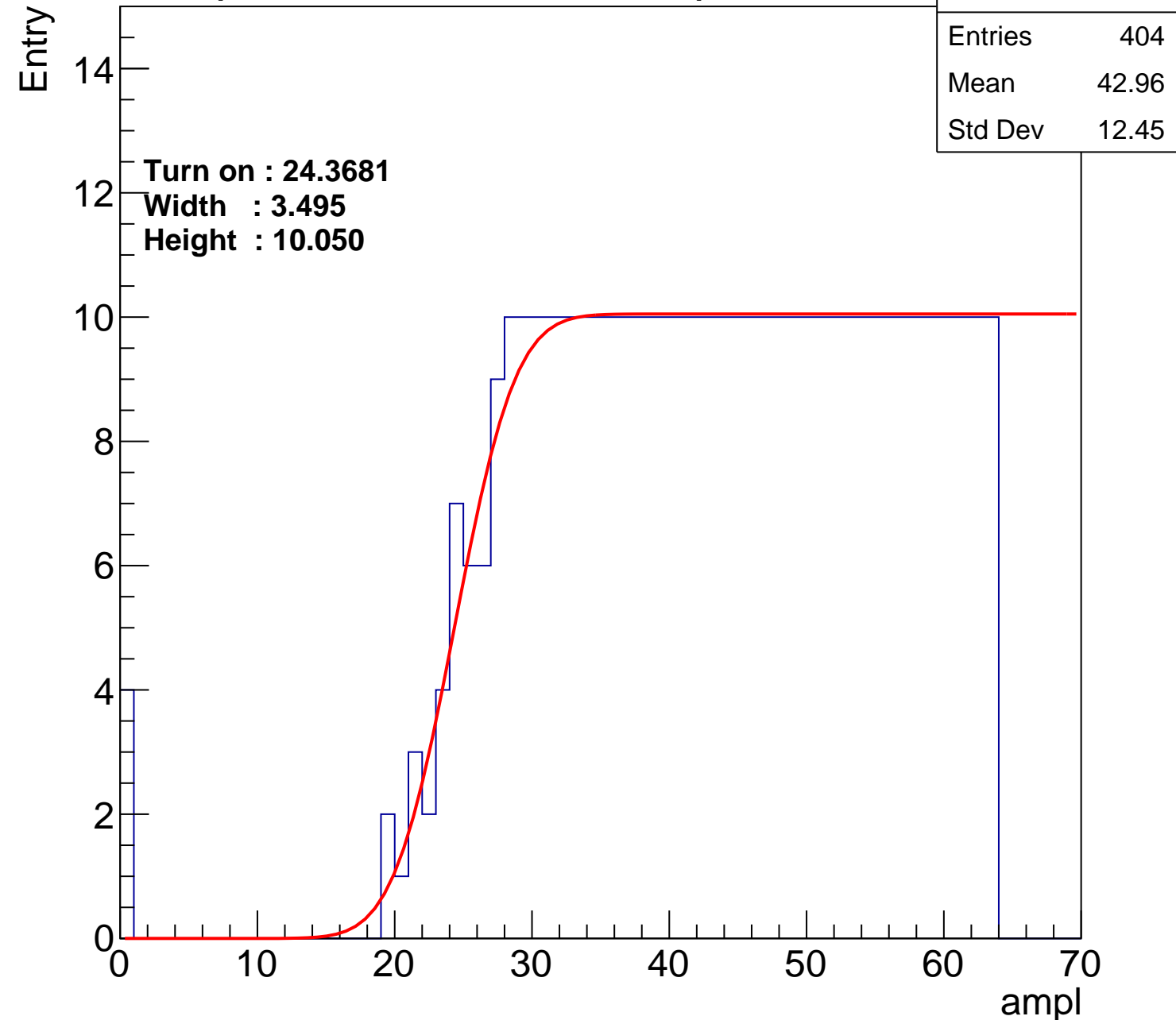
Width : 3.495

Height : 10.050

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch61

calib_packv5_042523_0143.root, FC#4, port A2

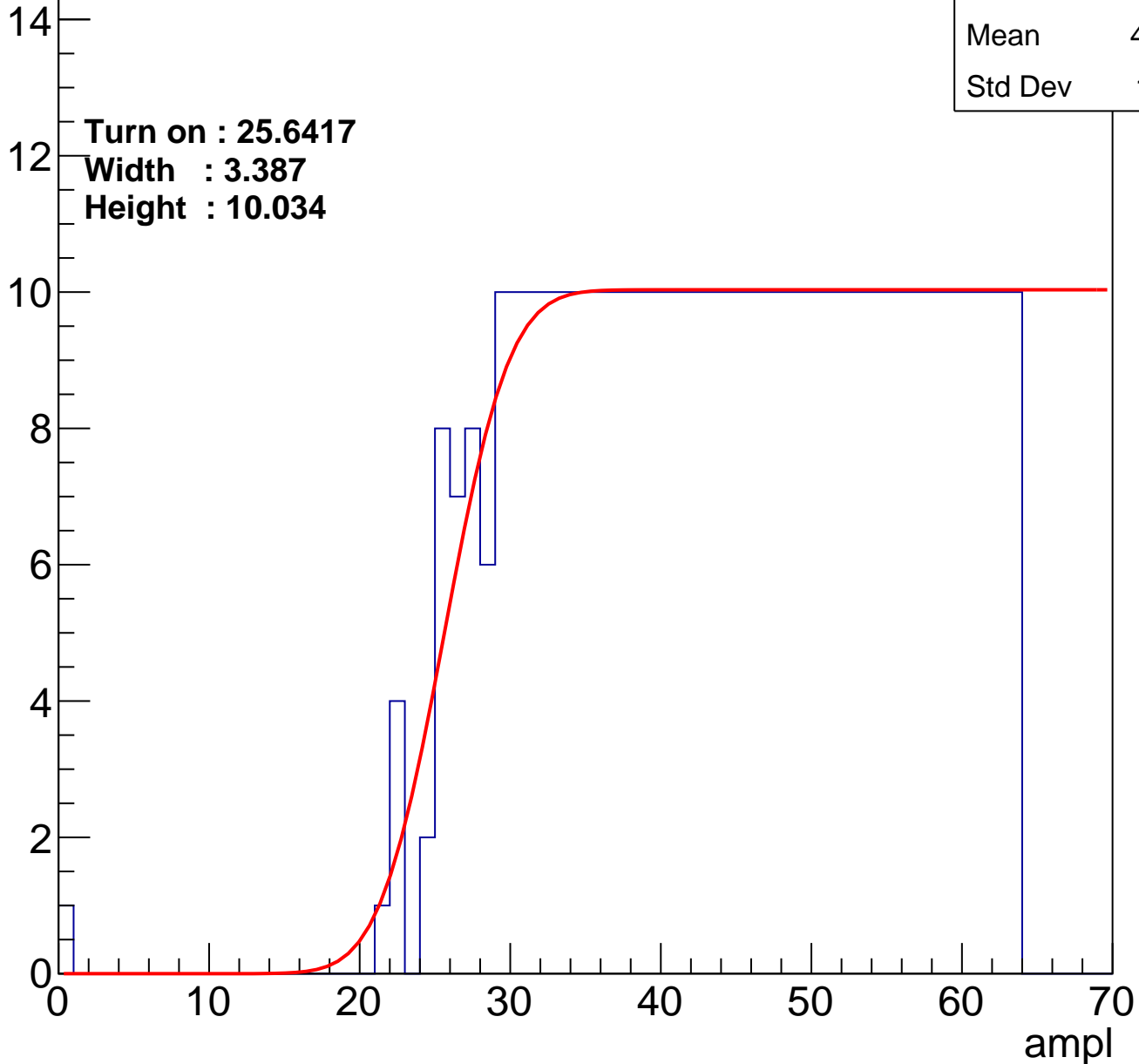
Entries	387
Mean	43.99
Std Dev	11.51

Turn on : 25.6417

Width : 3.387

Height : 10.034

Entry



B1L100S, U5-ch62

calib_packv5_042523_0143.root, FC#4, port A2

Entries	380
Mean	44.3
Std Dev	11.46

Turn on : 26.2695

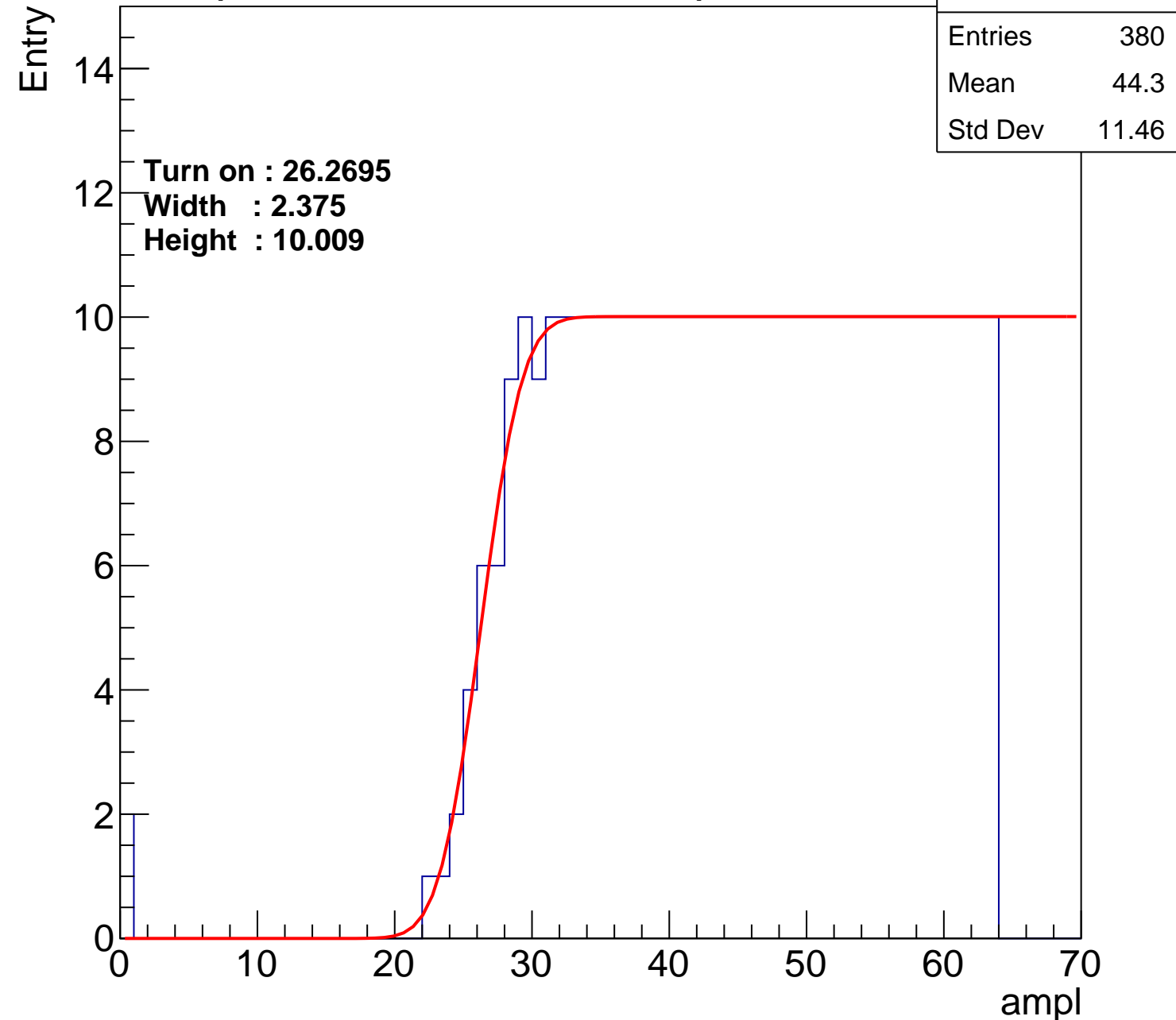
Width : 2.375

Height : 10.009

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch63

calib_packv5_042523_0143.root, FC#4, port A2

Entries	374
Mean	44.45
Std Dev	11.61

Turn on : 27.0672

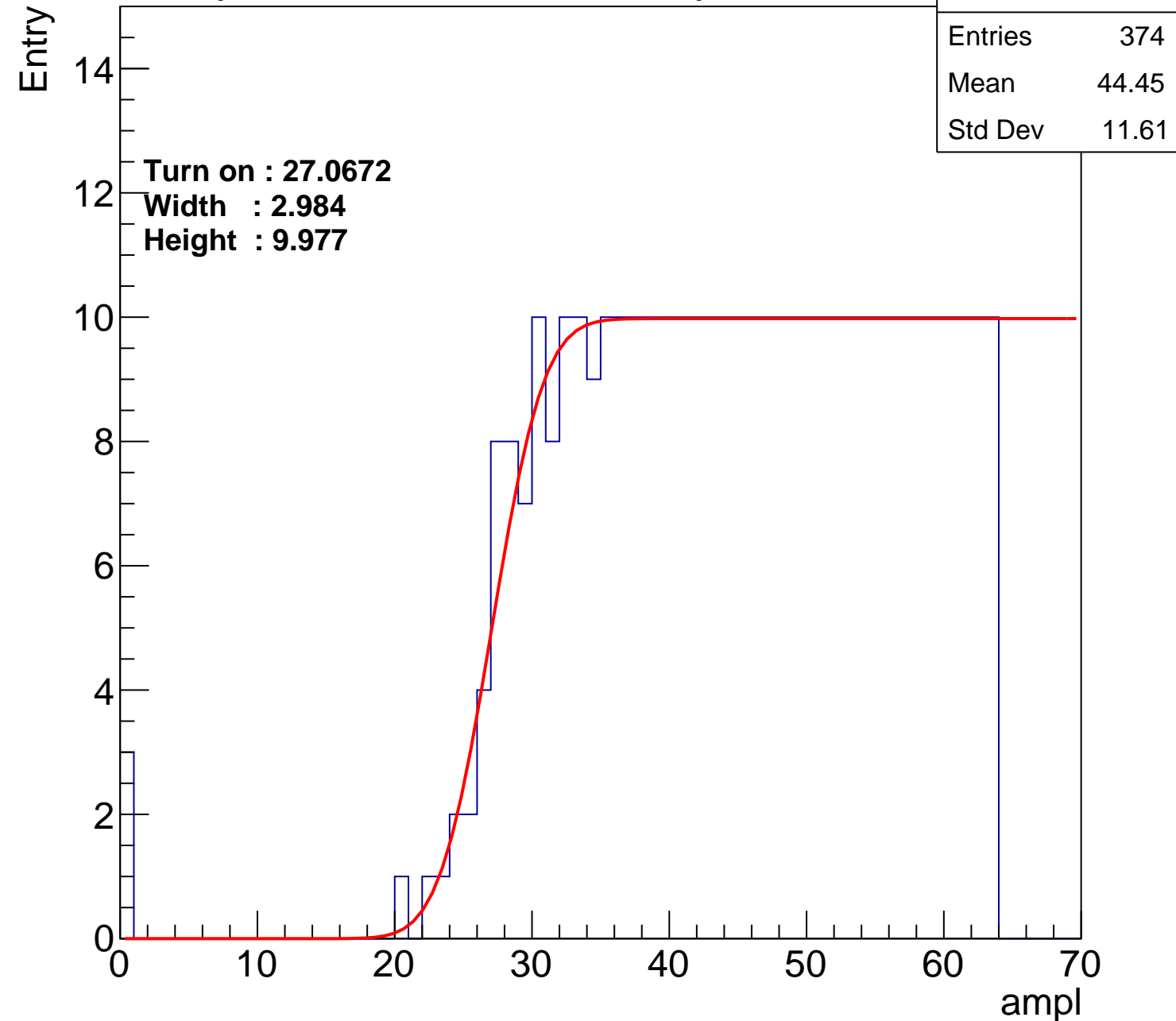
Width : 2.984

Height : 9.977

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch64

calib_packv5_042523_0143.root, FC#4, port A2

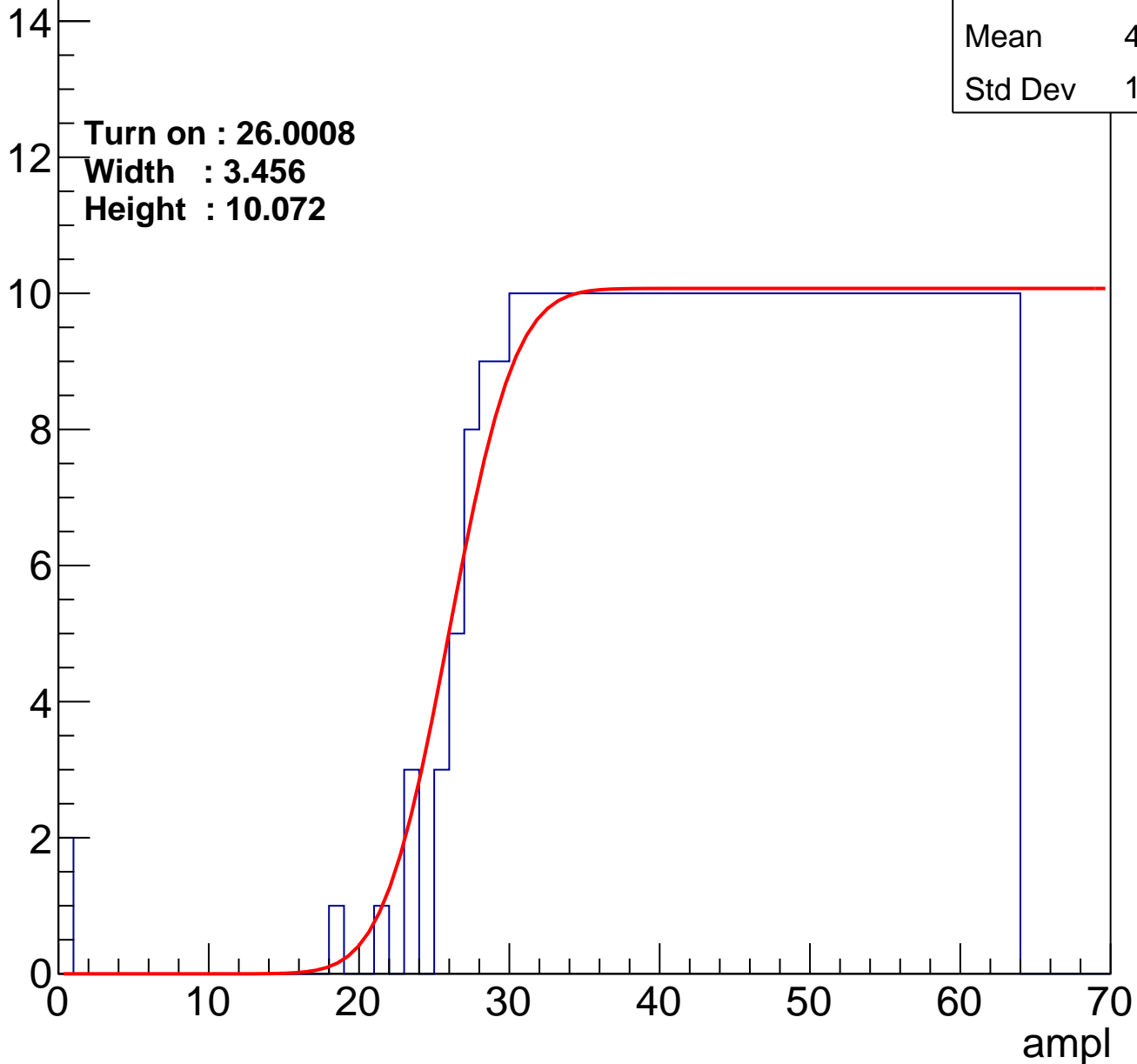
Entries	381
Mean	44.23
Std Dev	11.52

Turn on : 26.0008

Width : 3.456

Height : 10.072

Entry



B1L100S, U5-ch65

calib_packv5_042523_0143.root, FC#4, port A2

Entries	378
Mean	44.22
Std Dev	11.84

Turn on : 26.6200

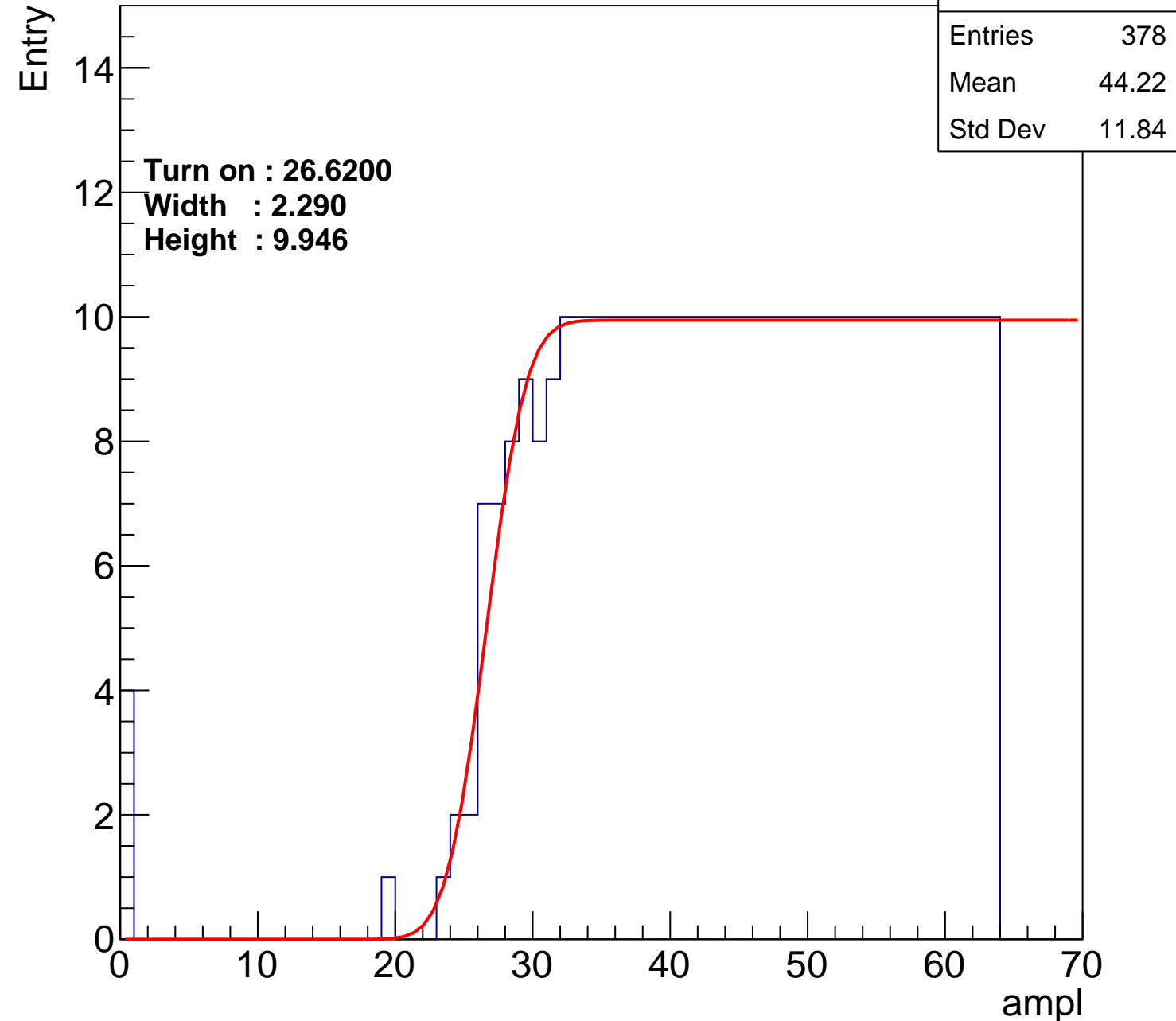
Width : 2.290

Height : 9.946

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch66

calib_packv5_042523_0143.root, FC#4, port A2

Entries	379
Mean	44.21
Std Dev	11.64

Turn on : 26.6862

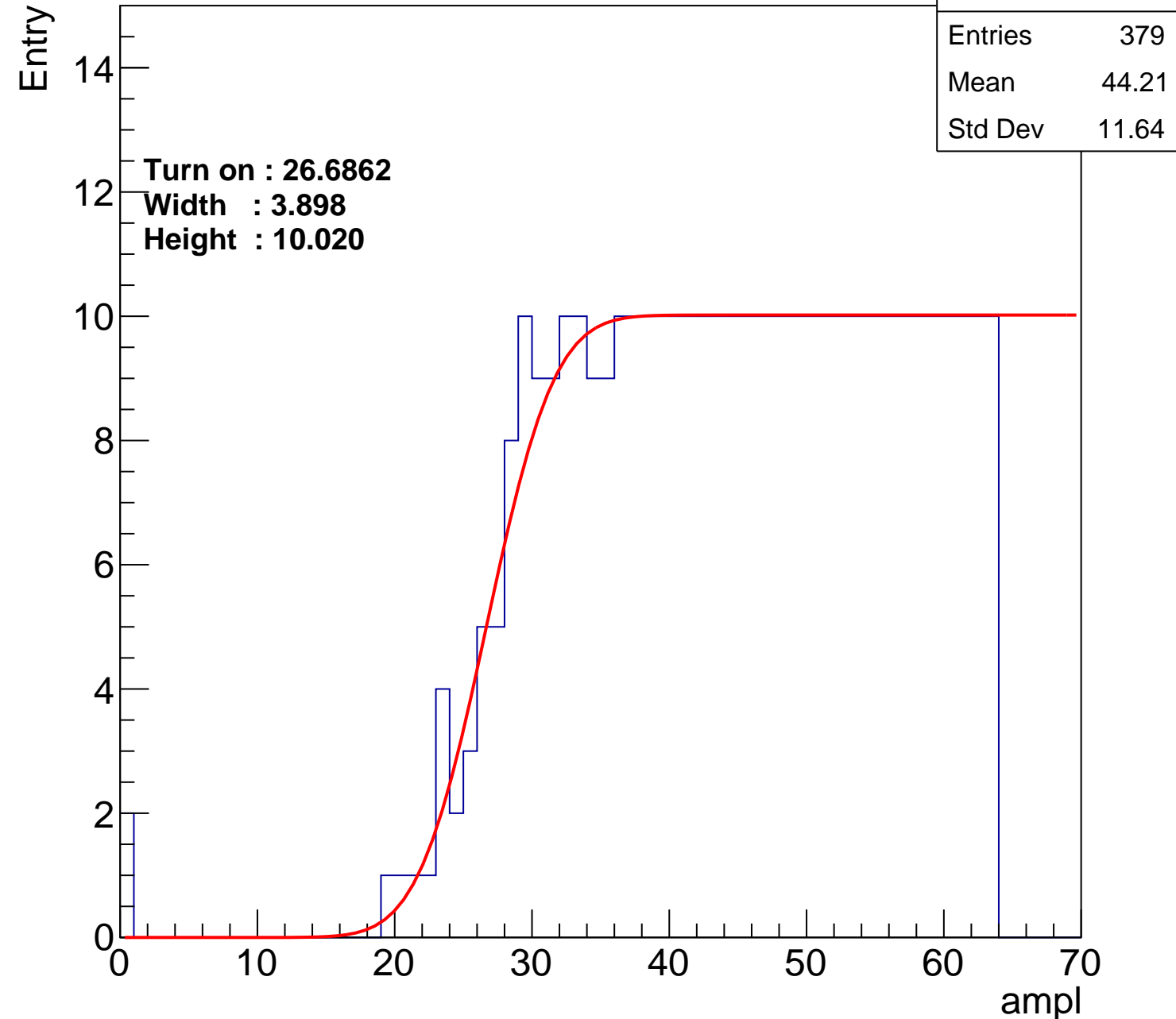
Width : 3.898

Height : 10.020

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch67

calib_packv5_042523_0143.root, FC#4, port A2

Entries	385
Mean	44
Std Dev	11.68

Turn on : 25.6051

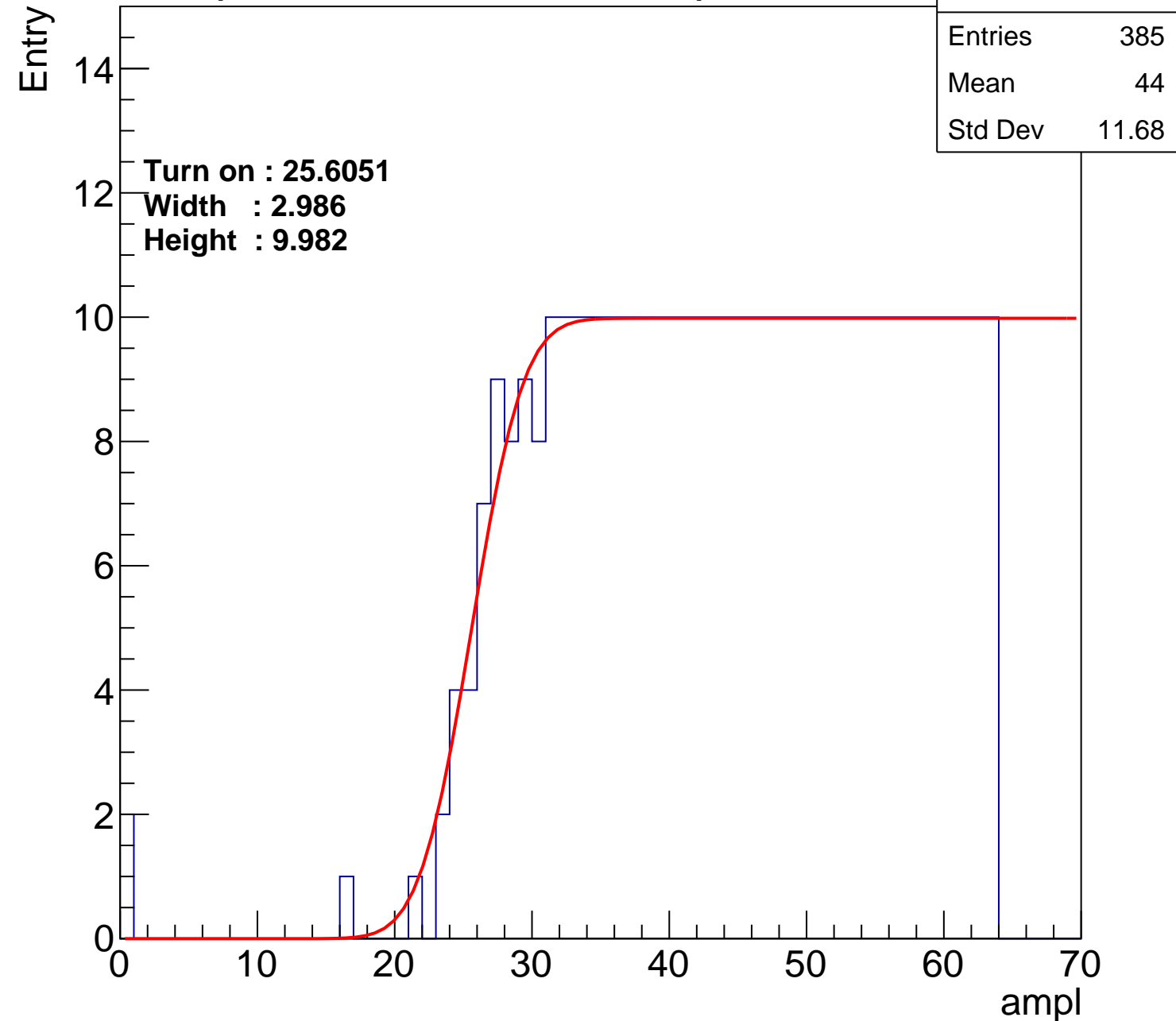
Width : 2.986

Height : 9.982

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch68

calib_packv5_042523_0143.root, FC#4, port A2

Entries	399
Mean	43.31
Std Dev	12.02

Turn on : 23.7671

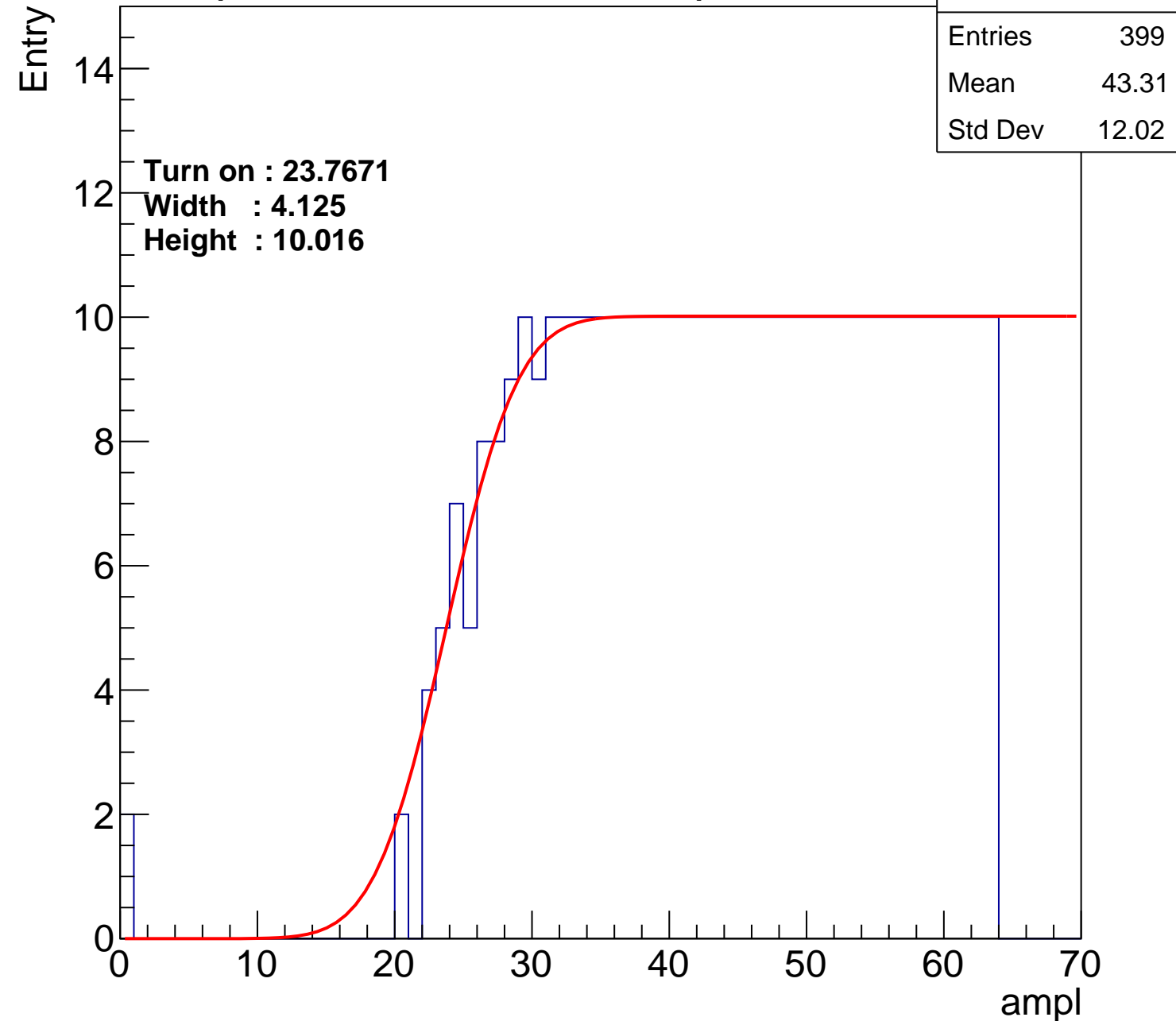
Width : 4.125

Height : 10.016

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch69

calib_packv5_042523_0143.root, FC#4, port A2

Entries	389
Mean	43.66
Std Dev	12.08

Turn on : 26.3341

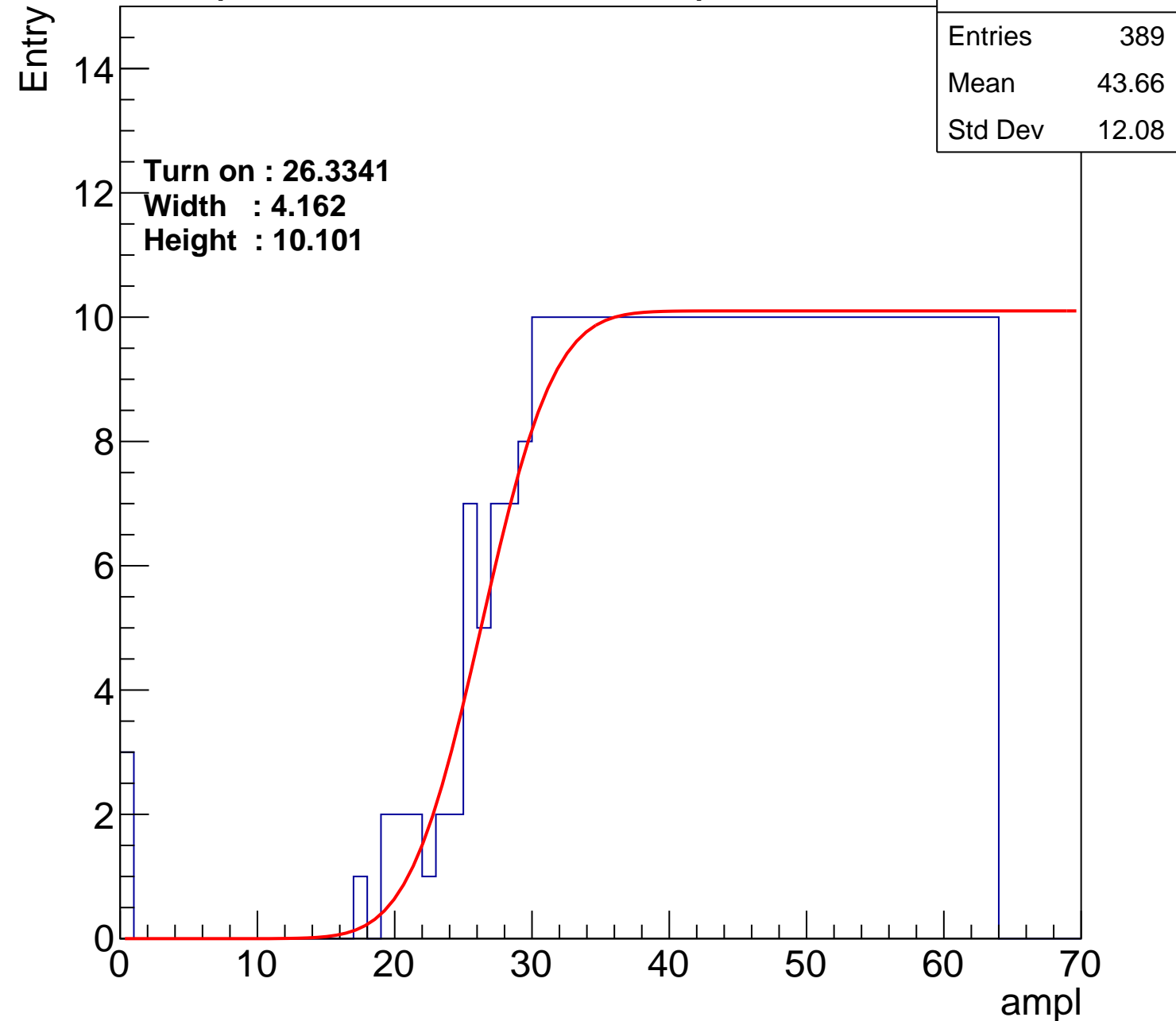
Width : 4.162

Height : 10.101

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch70

calib_packv5_042523_0143.root, FC#4, port A2

Entries	371
Mean	44.68
Std Dev	11.32

Turn on : 27.1452

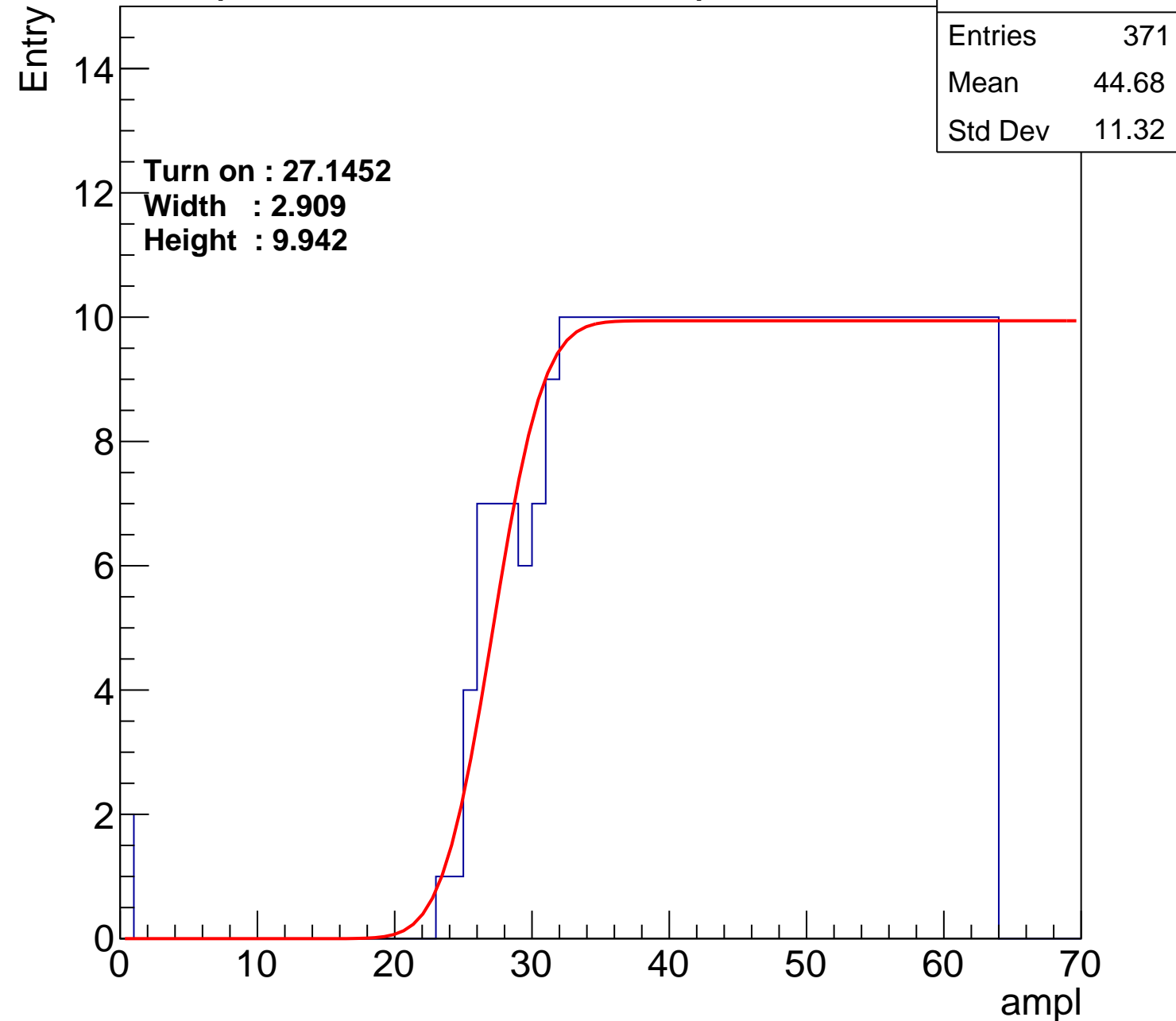
Width : 2.909

Height : 9.942

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch71

calib_packv5_042523_0143.root, FC#4, port A2

Entries	362
Mean	44.92
Std Dev	11.68

Turn on : 28.5082

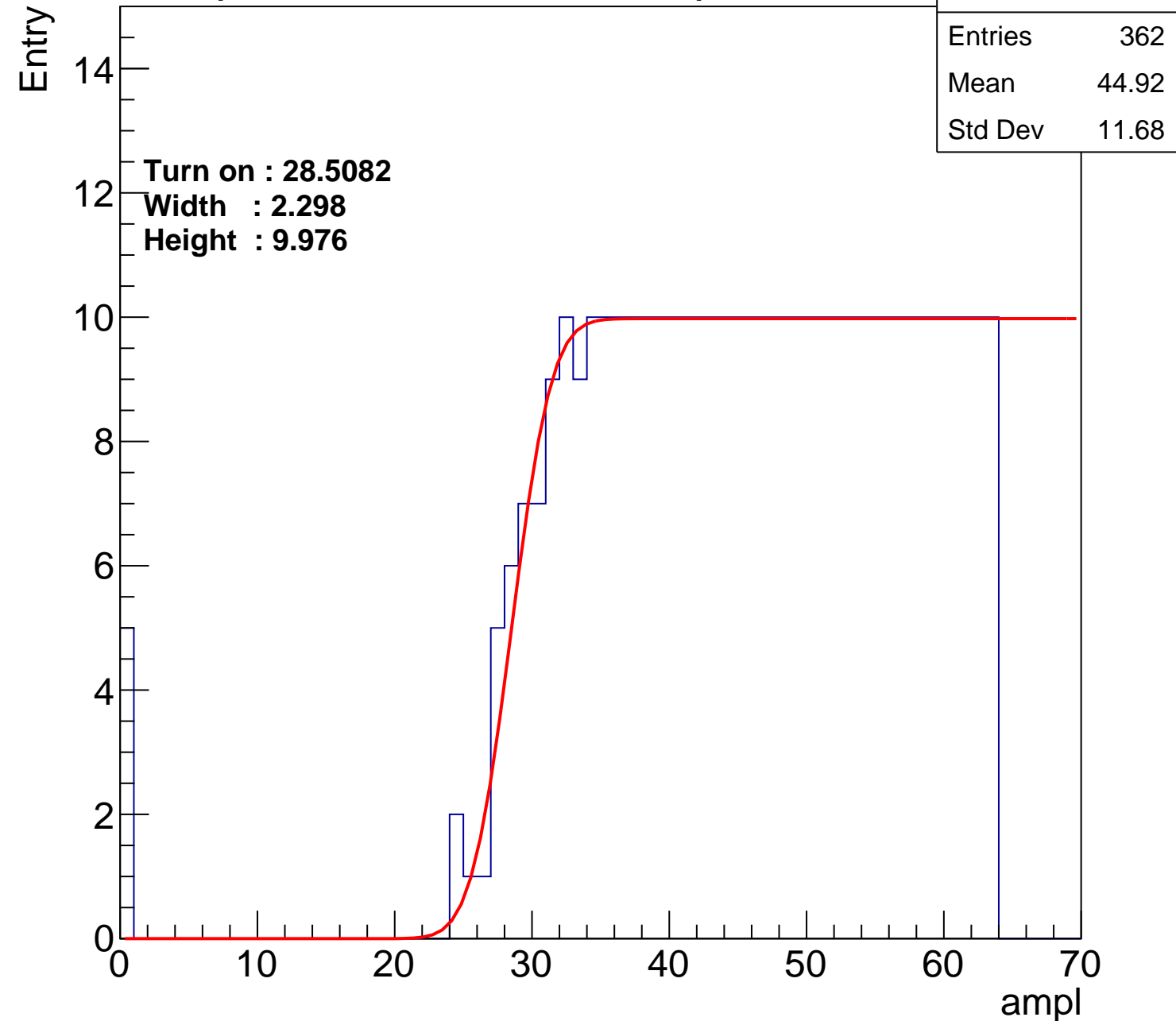
Width : 2.298

Height : 9.976

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch72

calib_packv5_042523_0143.root, FC#4, port A2

Entries	405
Mean	42.82
Std Dev	12.71

Turn on : 23.9797

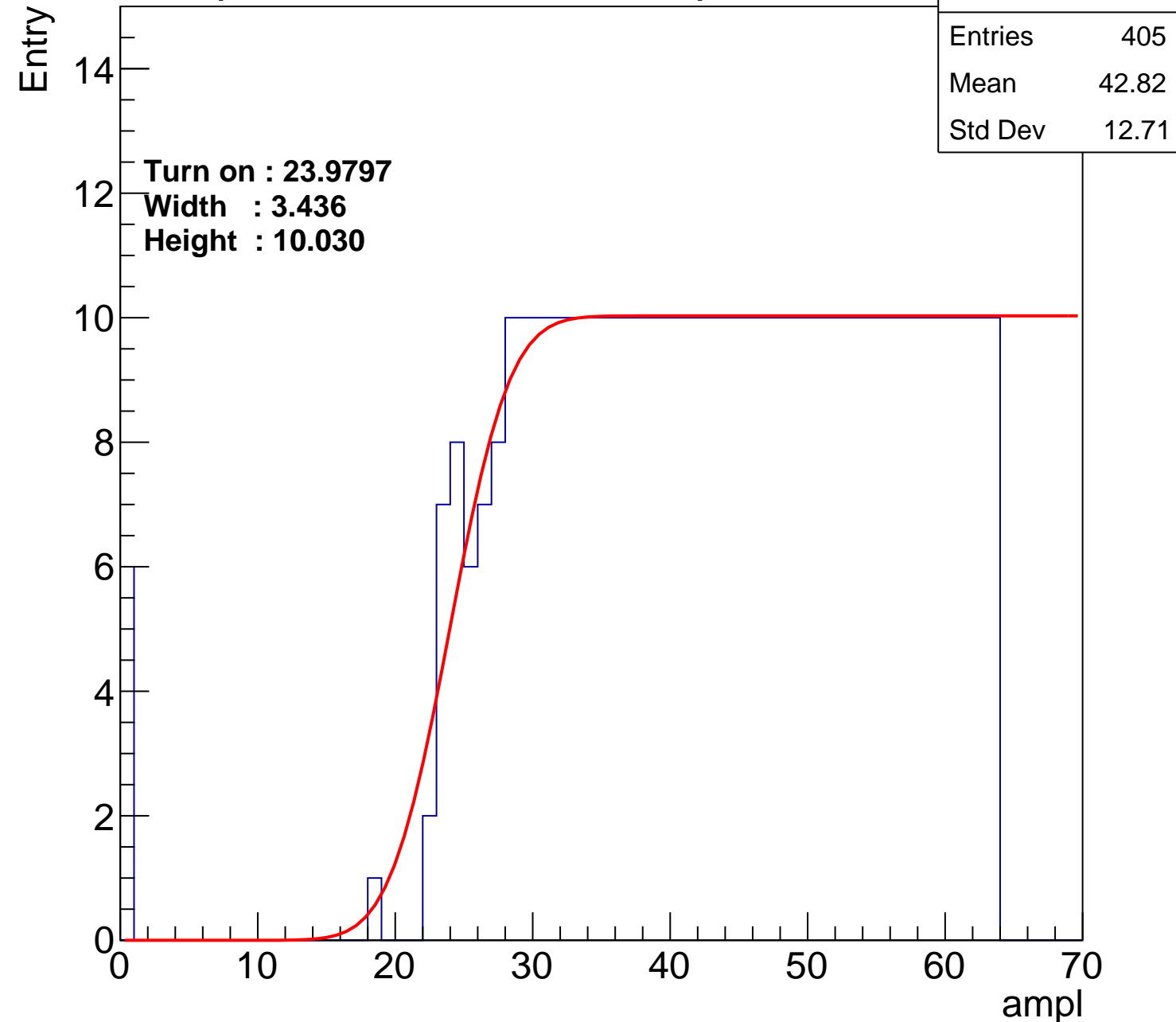
Width : 3.436

Height : 10.030

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch73

calib_packv5_042523_0143.root, FC#4, port A2

Entries	371
Mean	44.68
Std Dev	11.32

Turn on : 27.0567

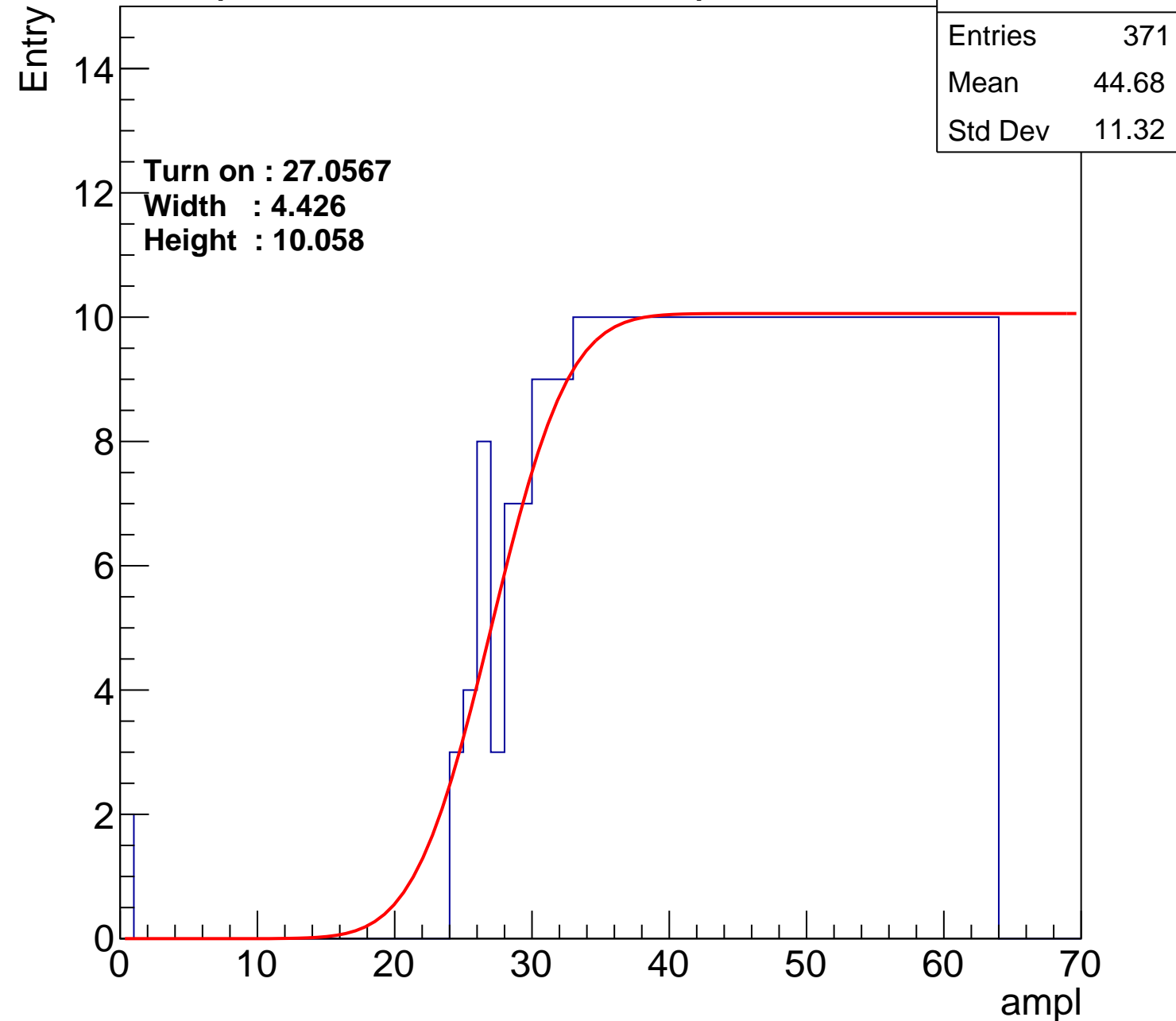
Width : 4.426

Height : 10.058

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch74

calib_packv5_042523_0143.root, FC#4, port A2

Entries	374
Mean	44.51
Std Dev	11.51

Turn on : 26.8978

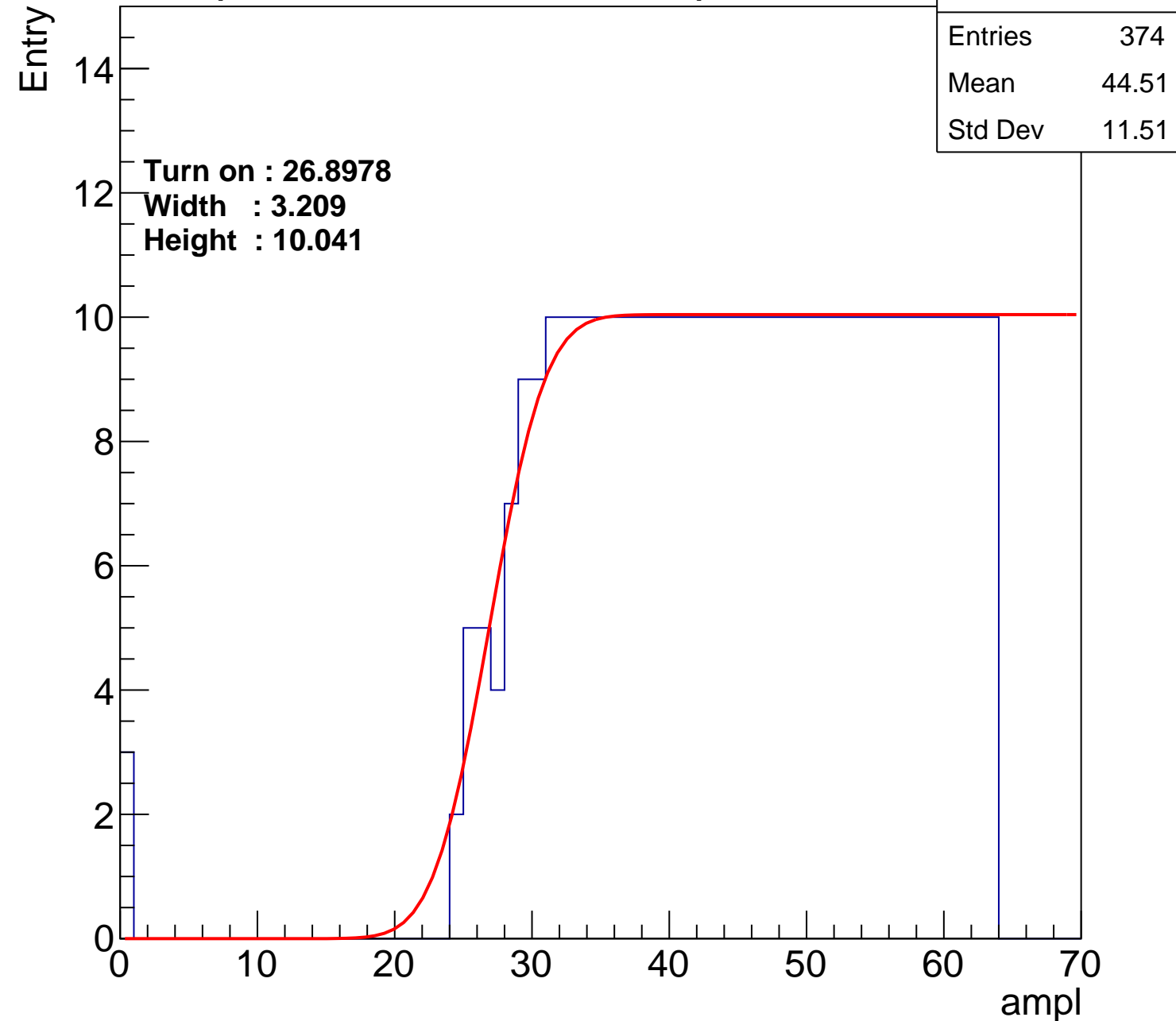
Width : 3.209

Height : 10.041

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch75

calib_packv5_042523_0143.root, FC#4, port A2

Entries	384
Mean	44.11
Std Dev	11.47

Turn on : 26.0861

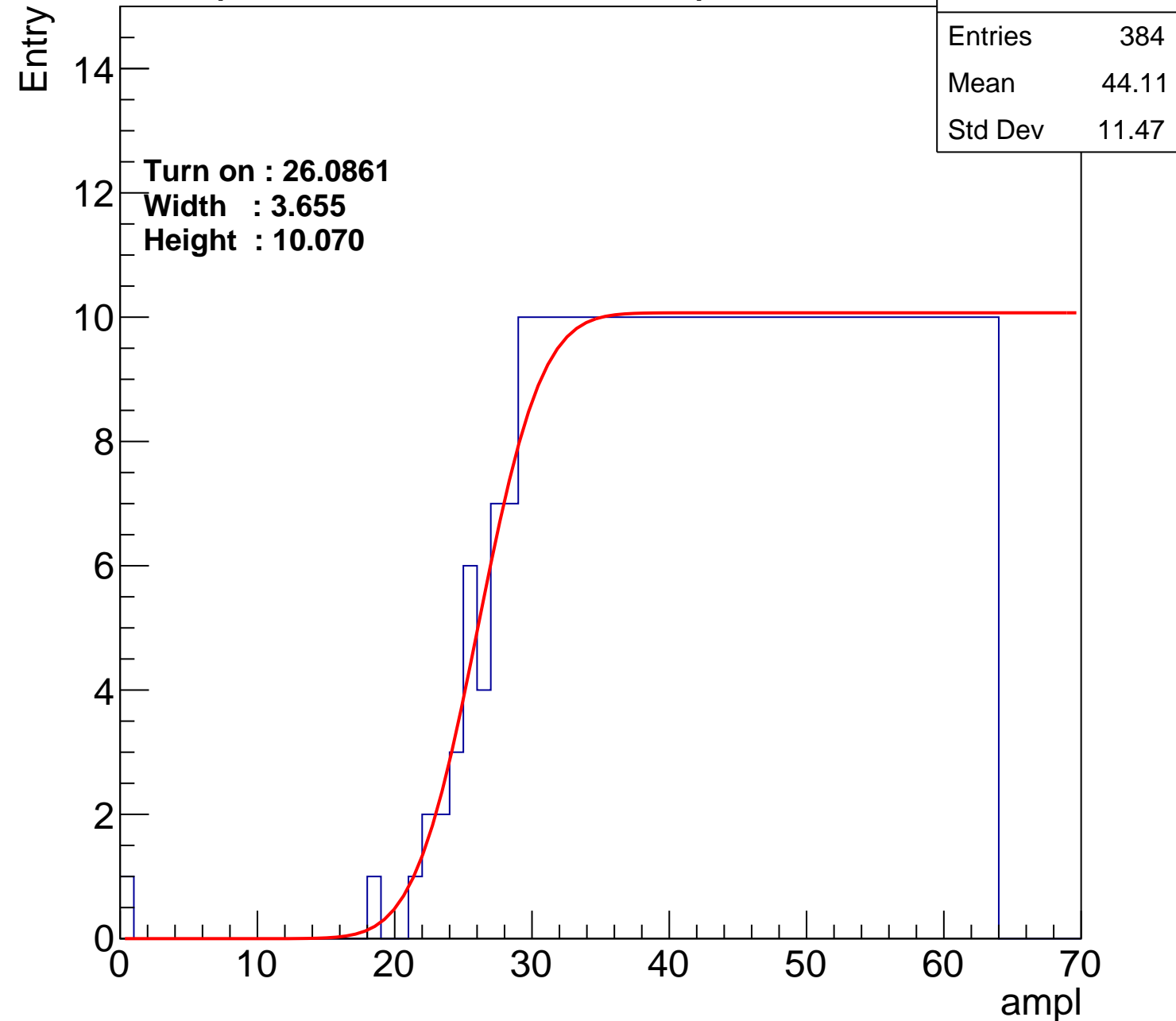
Width : 3.655

Height : 10.070

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch76

calib_packv5_042523_0143.root, FC#4, port A2

Entries	372
Mean	44.65
Std Dev	11.24

Turn on : 27.2554

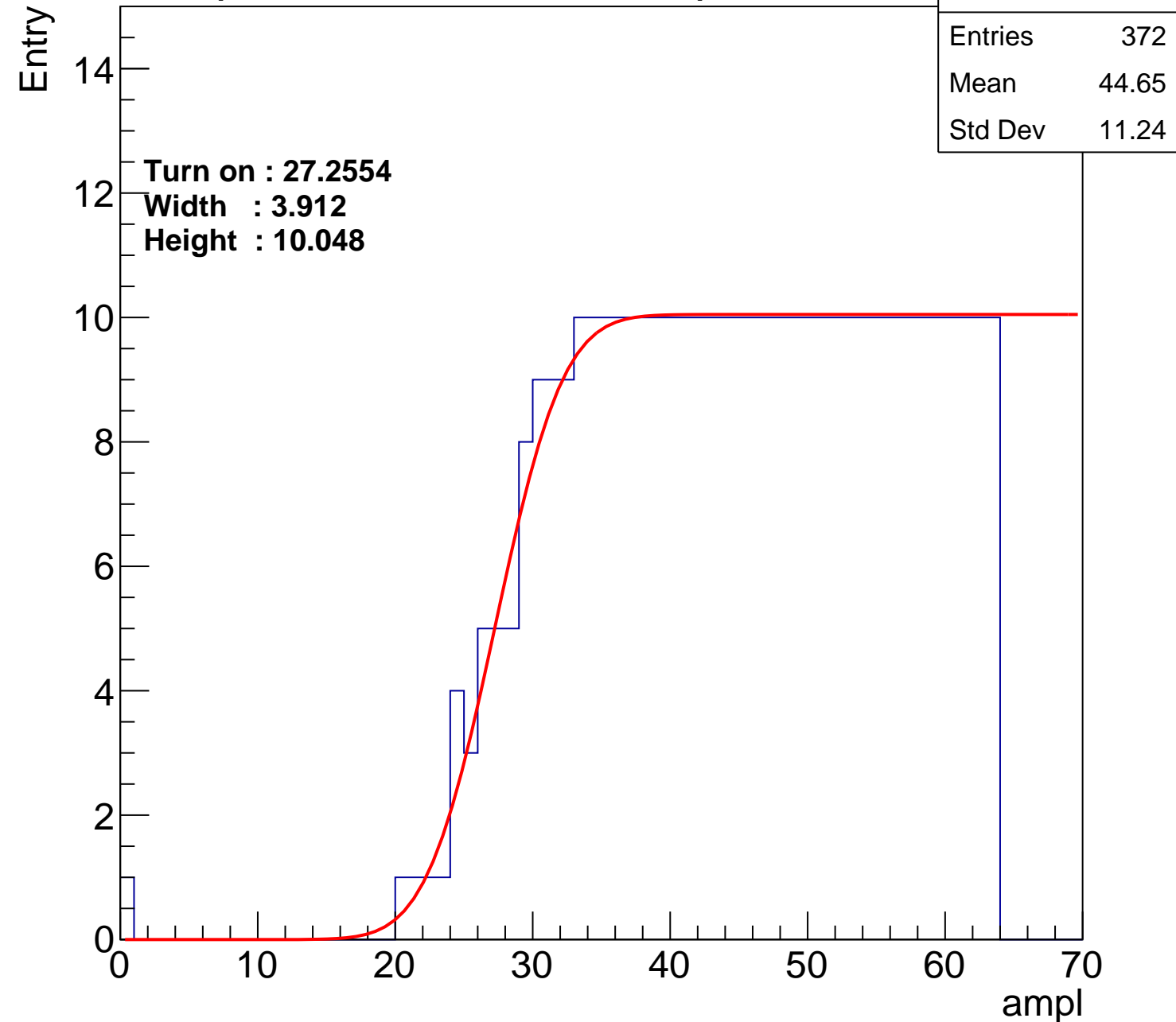
Width : 3.912

Height : 10.048

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch77

calib_packv5_042523_0143.root, FC#4, port A2

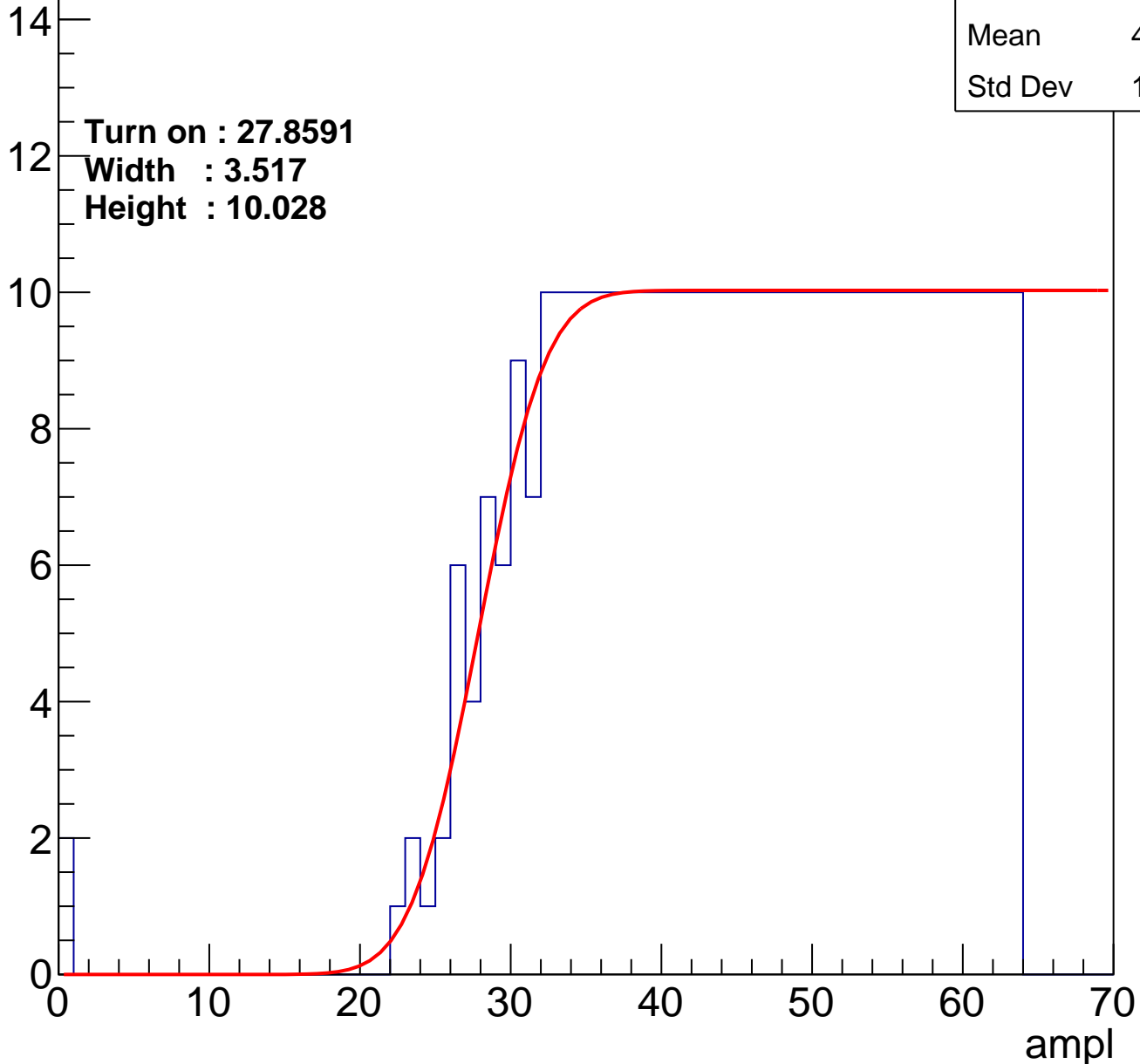
Entries	367
Mean	44.86
Std Dev	11.25

Turn on : 27.8591

Width : 3.517

Height : 10.028

Entry



B1L100S, U5-ch78

calib_packv5_042523_0143.root, FC#4, port A2

Entries	393
Mean	43.54
Std Dev	12.04

Turn on : 24.9296

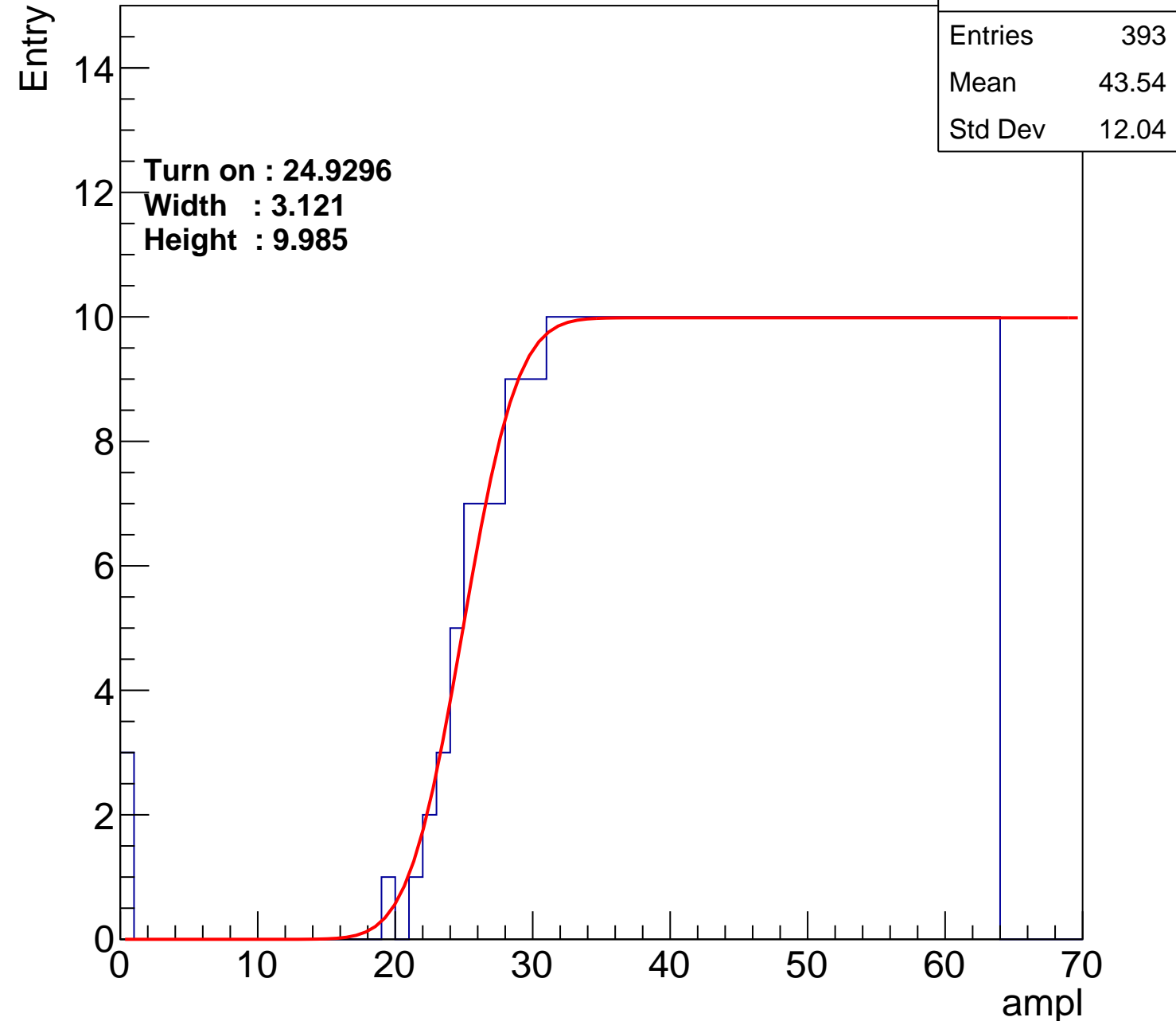
Width : 3.121

Height : 9.985

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch79

calib_packv5_042523_0143.root, FC#4, port A2

Entries	383
Mean	43.85
Std Dev	12.23

Turn on : 26.8588

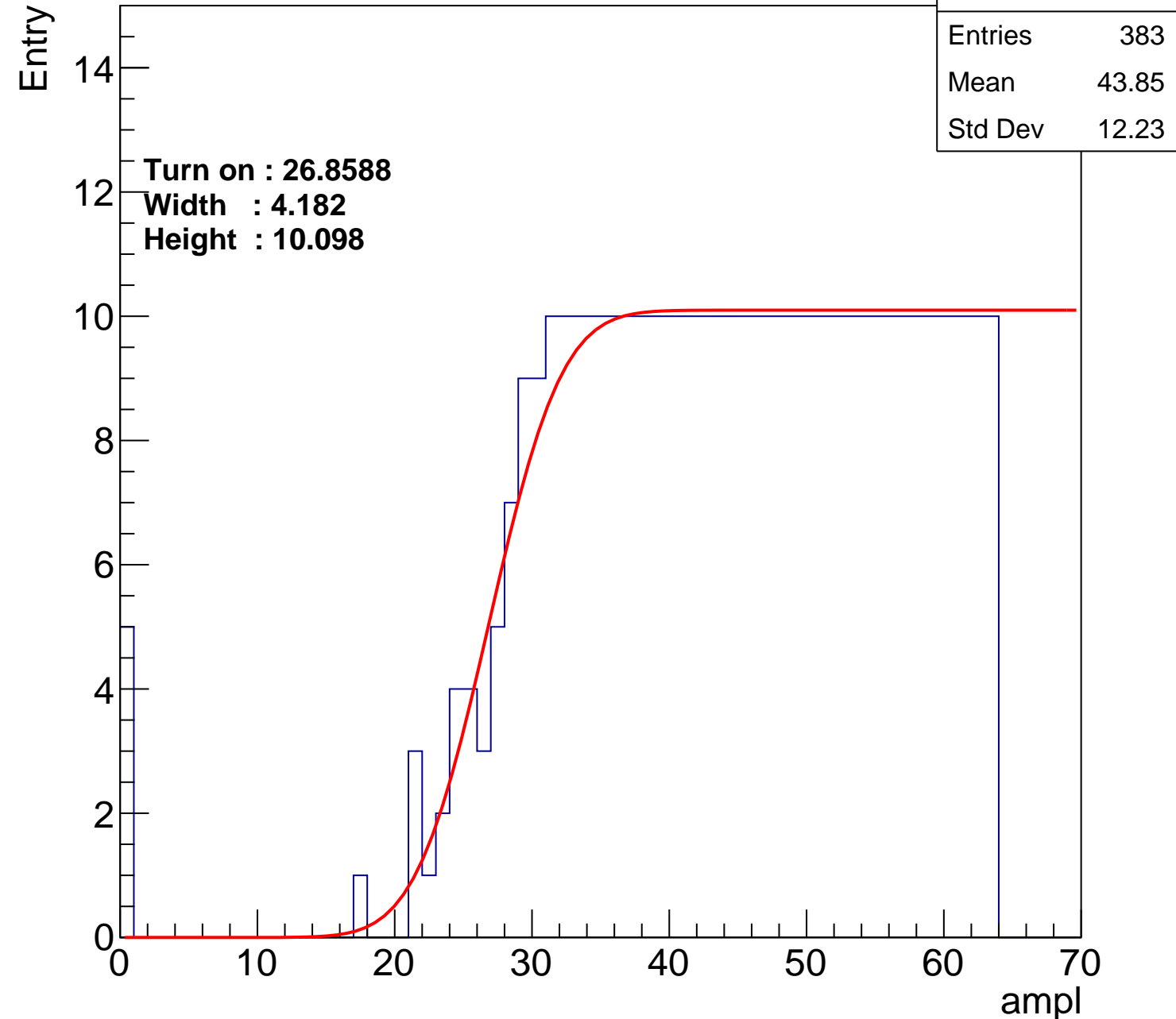
Width : 4.182

Height : 10.098

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch80

calib_packv5_042523_0143.root, FC#4, port A2

Entries	364
Mean	44.98
Std Dev	11.21

Turn on : 28.3391

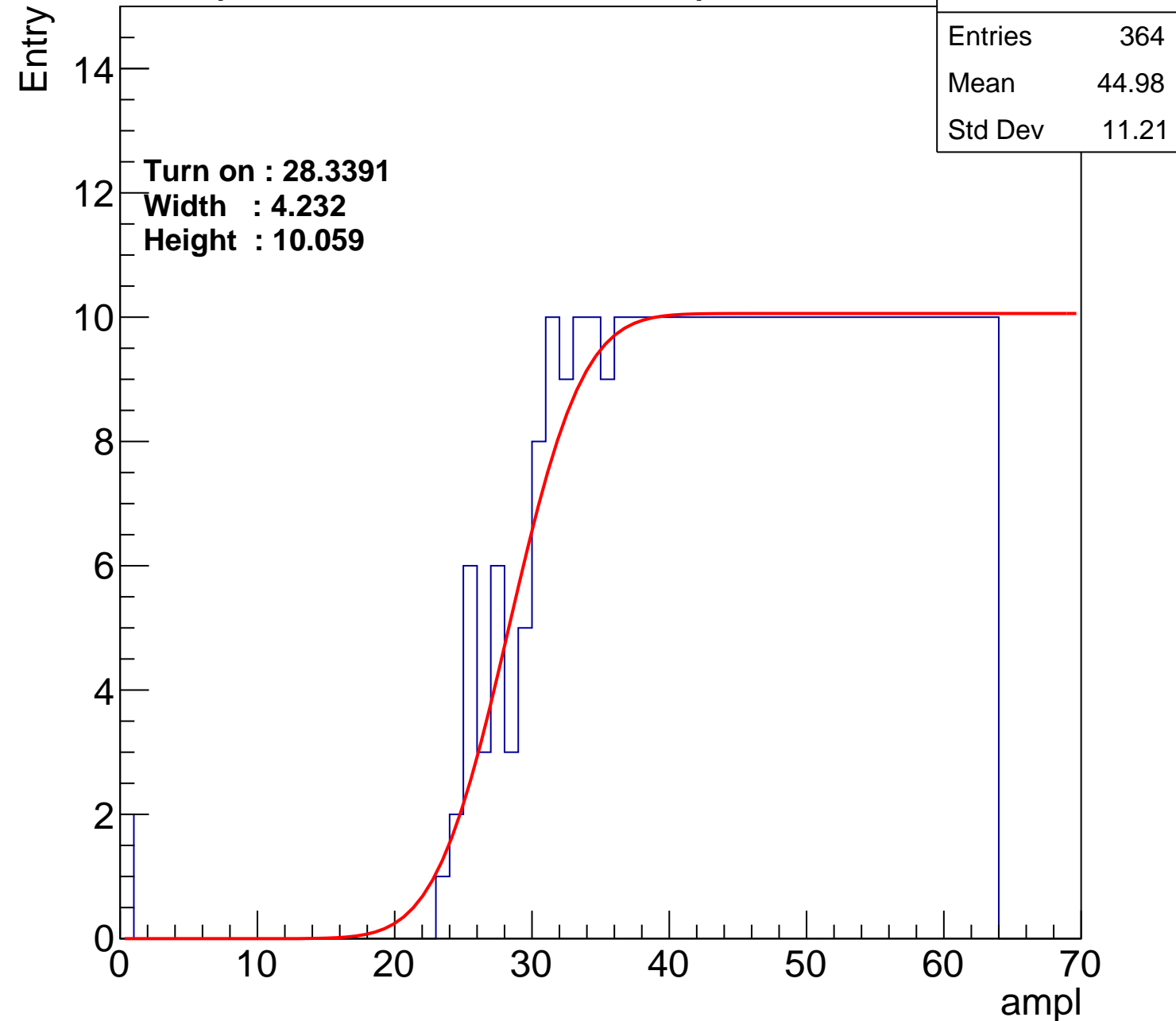
Width : 4.232

Height : 10.059

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch81

calib_packv5_042523_0143.root, FC#4, port A2

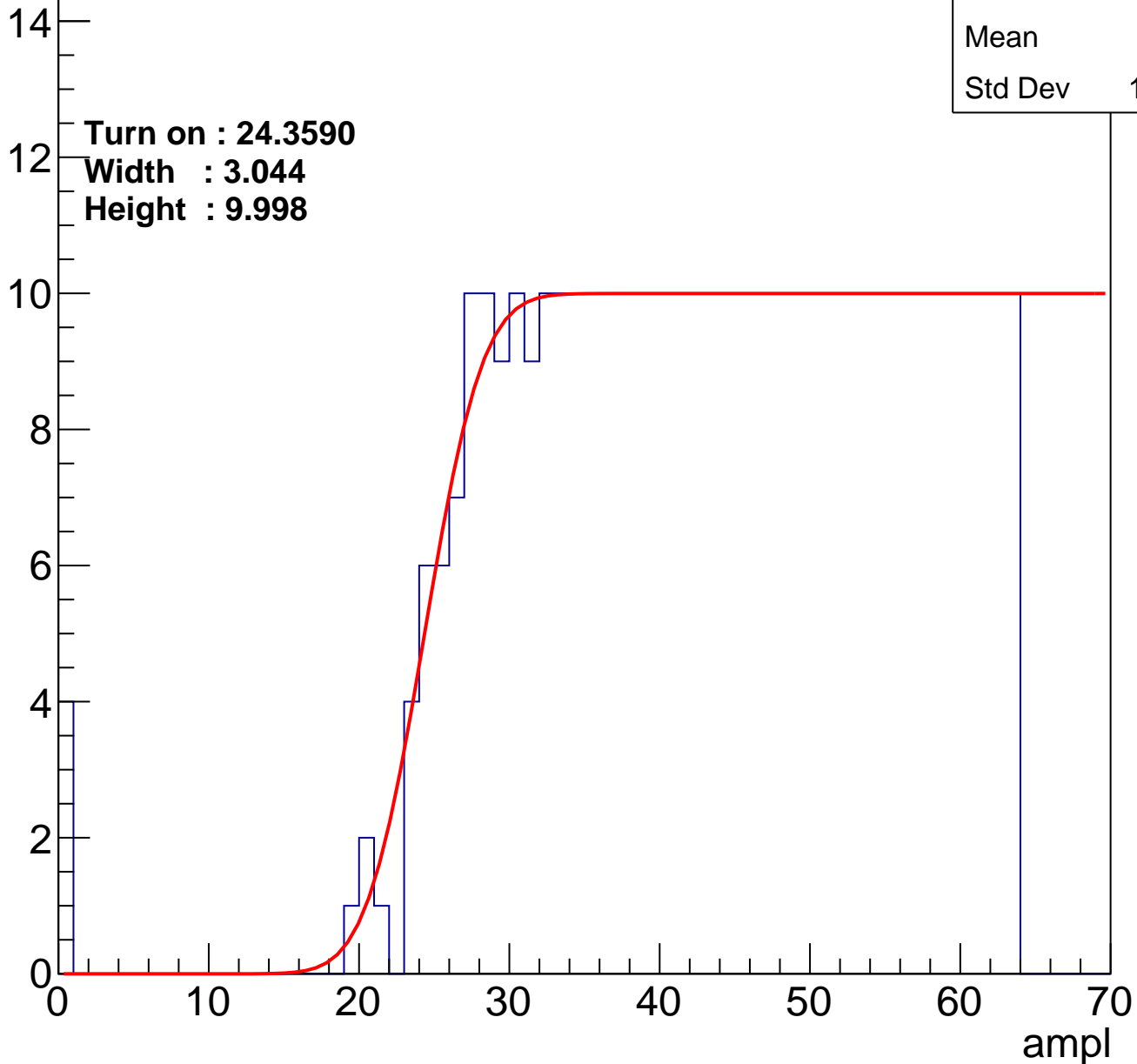
Entries	399
Mean	43.2
Std Dev	12.32

Turn on : 24.3590

Width : 3.044

Height : 9.998

Entry



B1L100S, U5-ch82

calib_packv5_042523_0143.root, FC#4, port A2

Entries	379
Mean	44.34
Std Dev	11.44

Turn on : 26.5165

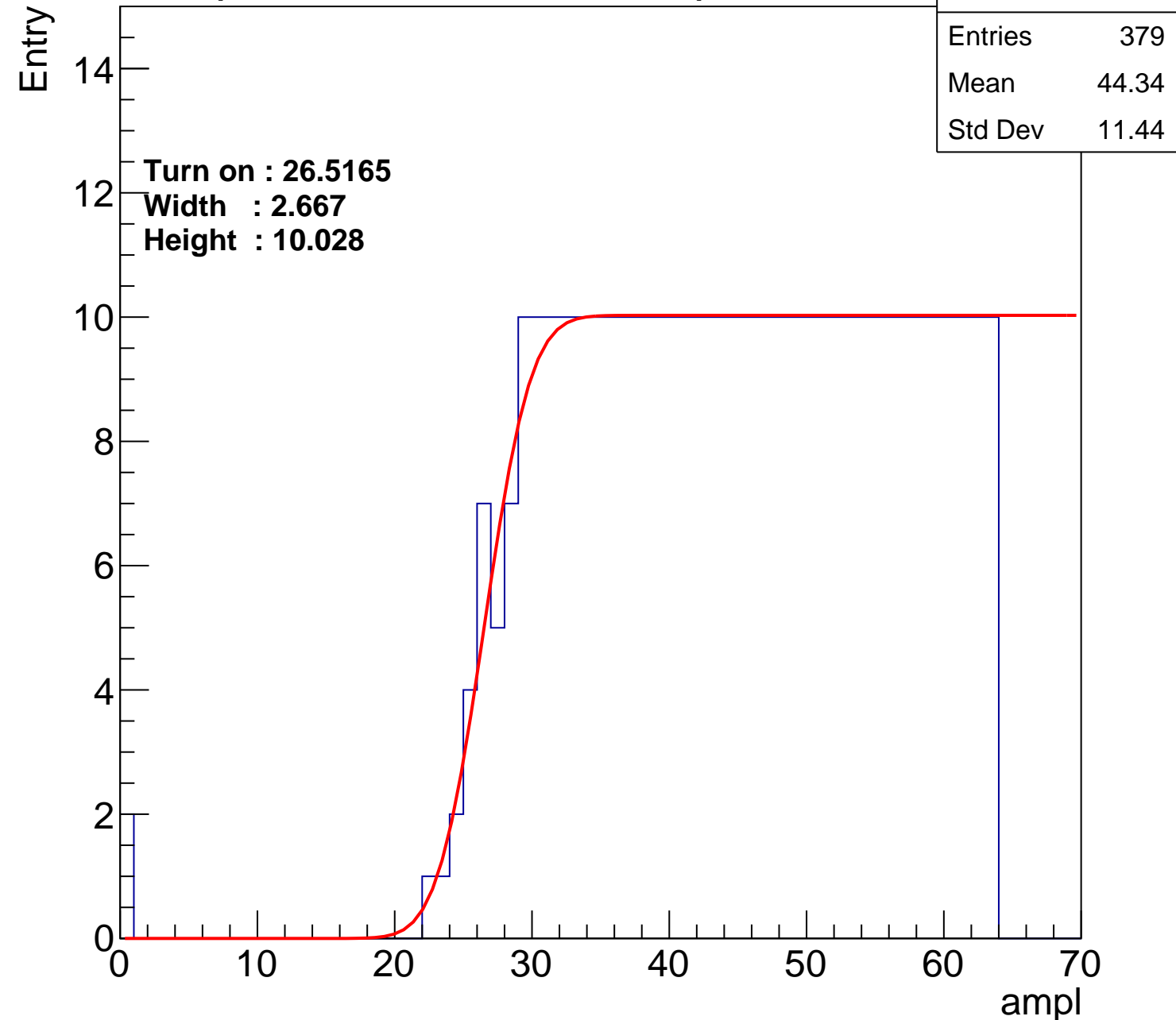
Width : 2.667

Height : 10.028

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch83

calib_packv5_042523_0143.root, FC#4, port A2

Entries	367
Mean	44.87
Std Dev	11.25

Turn on : 28.8341

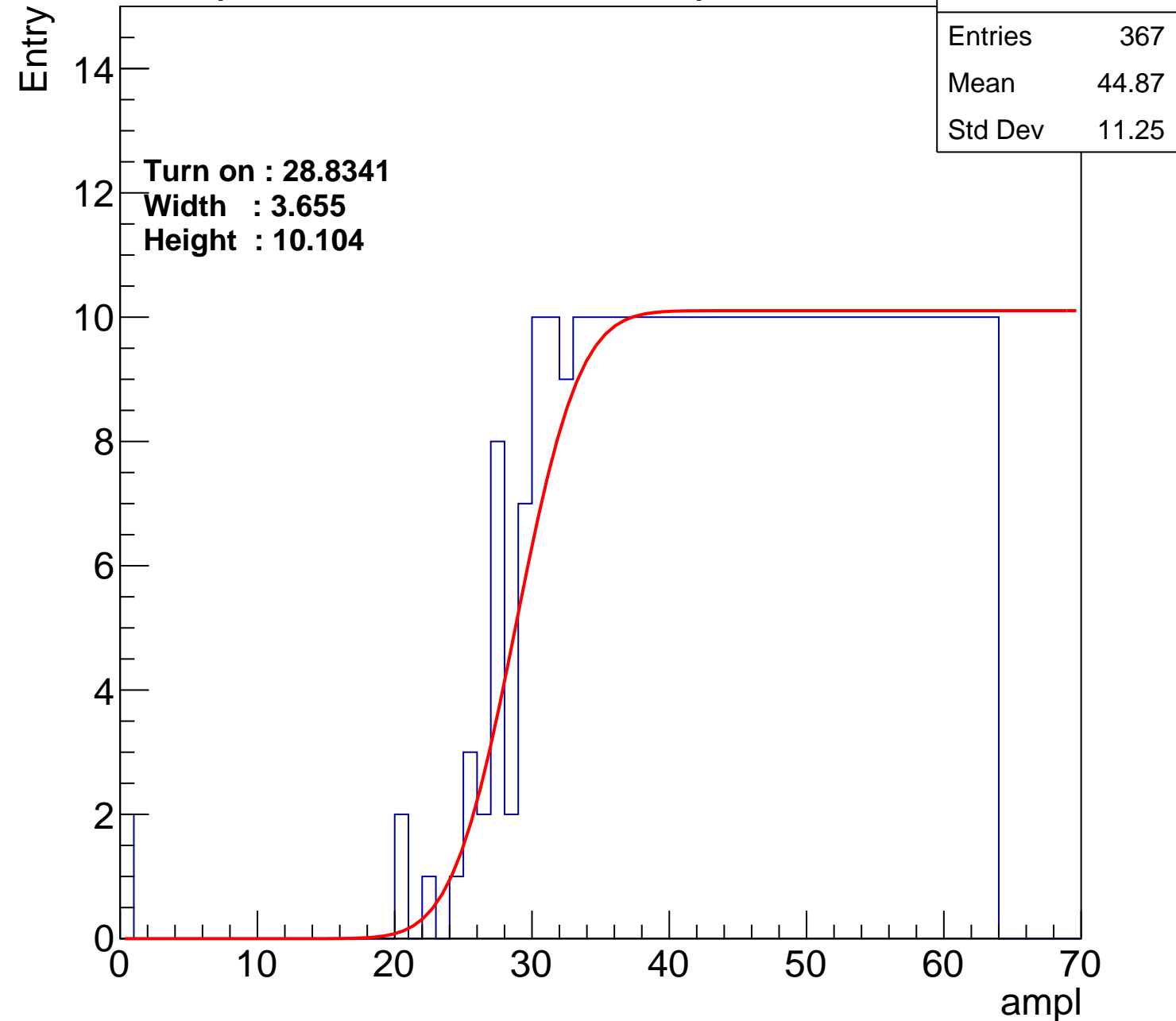
Width : 3.655

Height : 10.104

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch84

calib_packv5_042523_0143.root, FC#4, port A2

Entries	397
Mean	43.35
Std Dev	12.13

Turn on : 24.0563

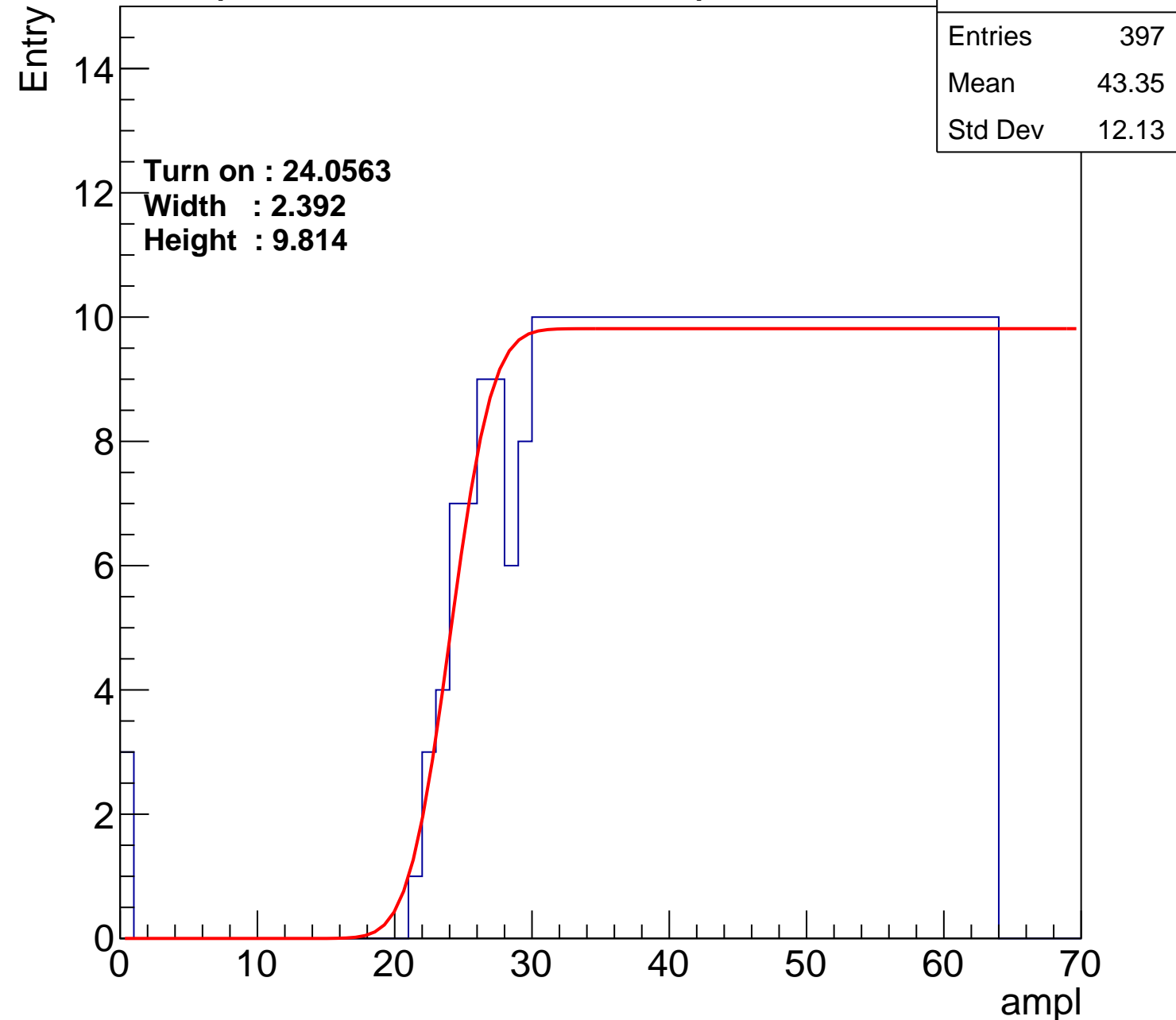
Width : 2.392

Height : 9.814

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch85

calib_packv5_042523_0143.root, FC#4, port A2

Entries	379
Mean	44.23
Std Dev	11.7

Turn on : 26.8348

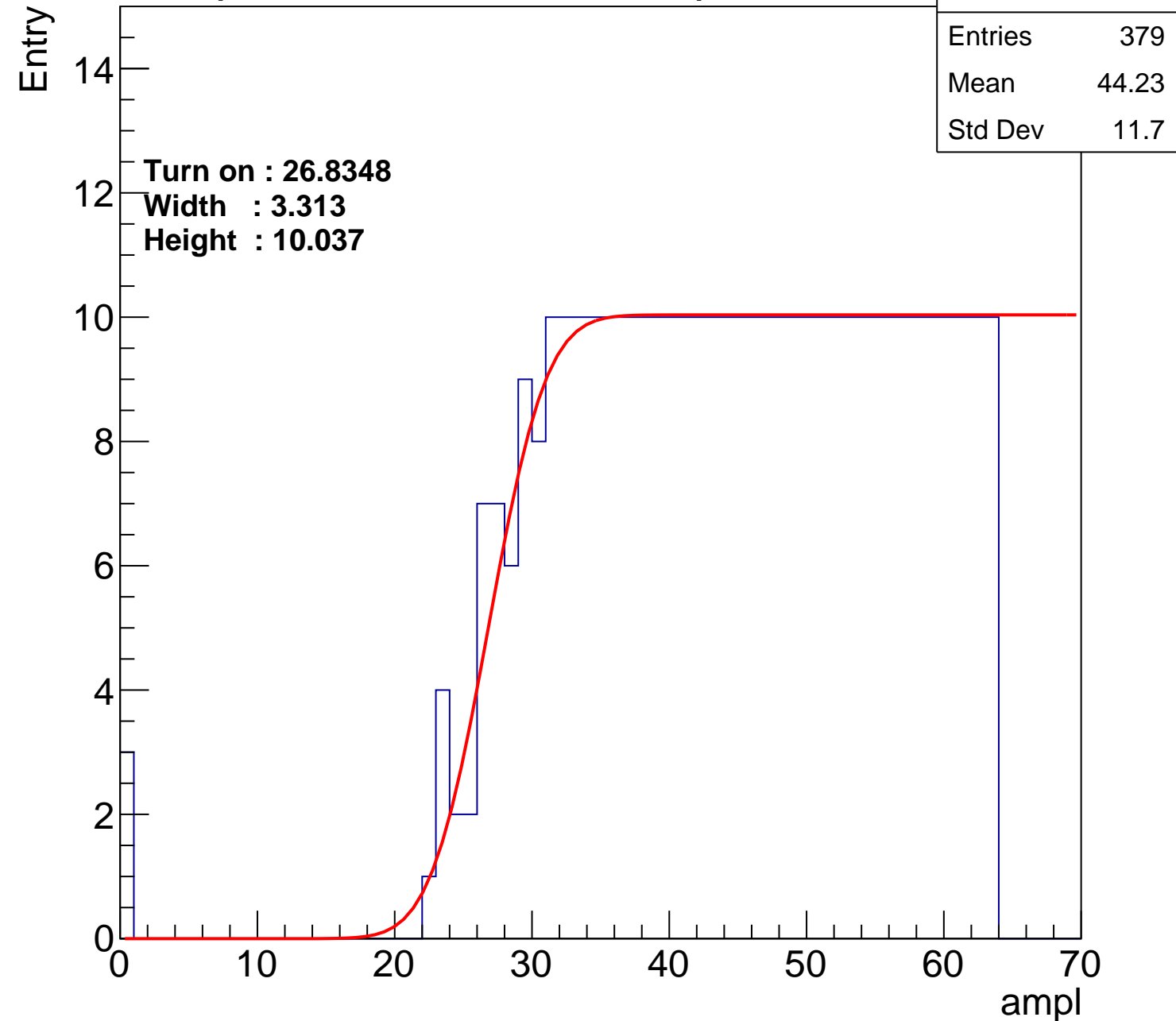
Width : 3.313

Height : 10.037

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch86

calib_packv5_042523_0143.root, FC#4, port A2

Entries	374
Mean	44.26
Std Dev	12.13

Turn on : 27.5219

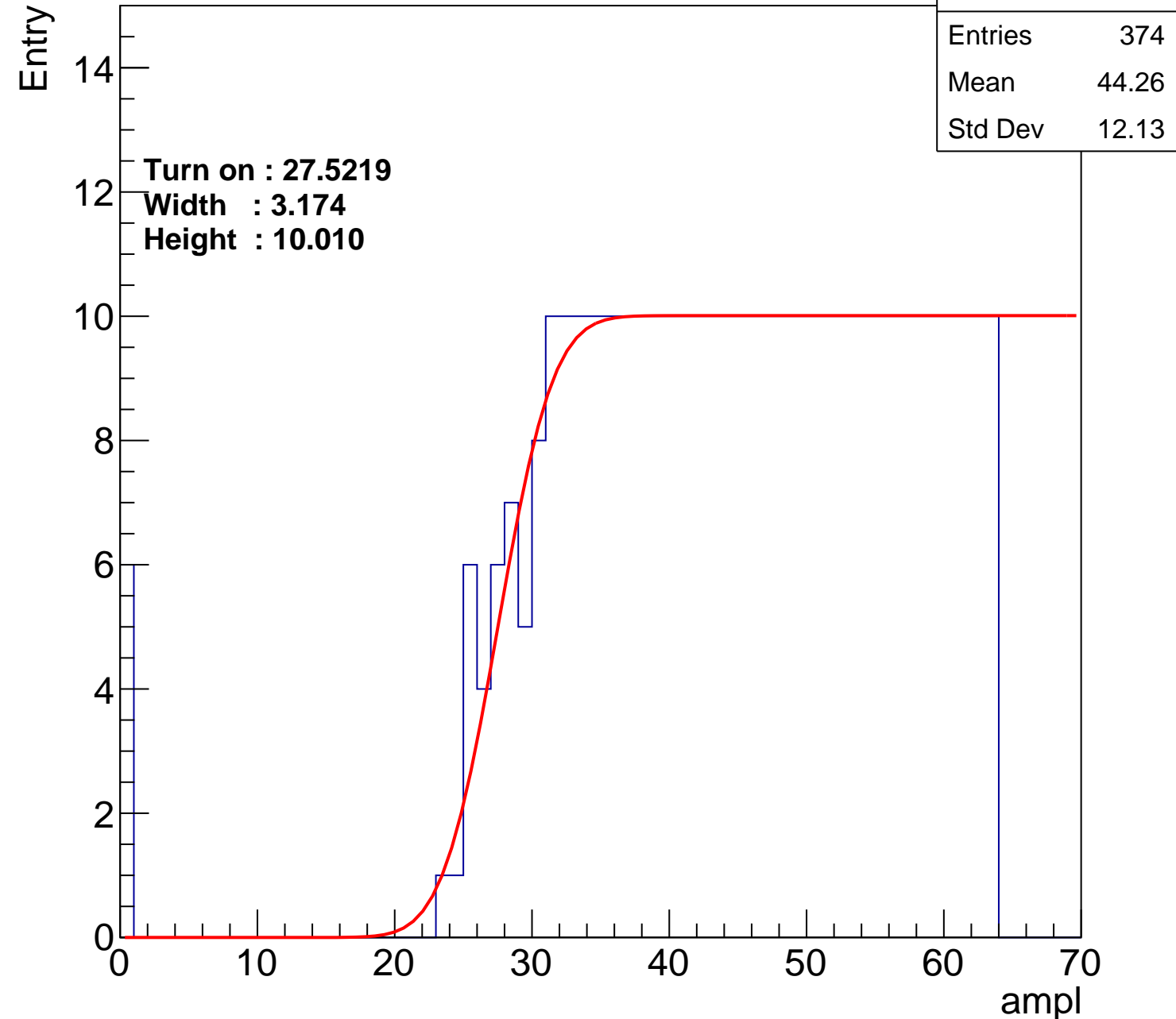
Width : 3.174

Height : 10.010

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch87

calib_packv5_042523_0143.root, FC#4, port A2

Entries	385
Mean	43.89
Std Dev	11.99

Turn on : 26.5362

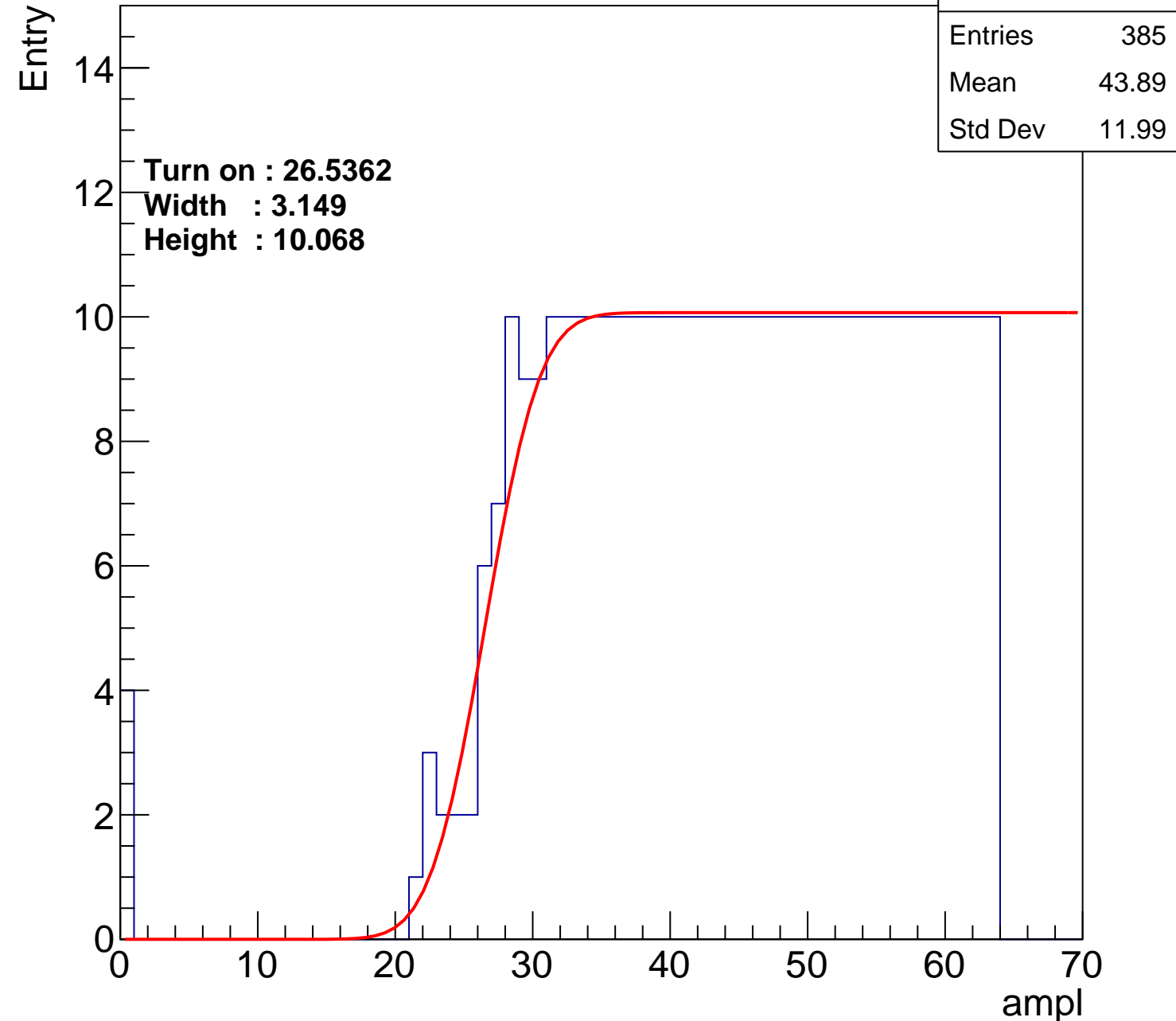
Width : 3.149

Height : 10.068

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch88

calib_packv5_042523_0143.root, FC#4, port A2

Entries	380
Mean	43.9
Std Dev	12.44

Turn on : 27.6264

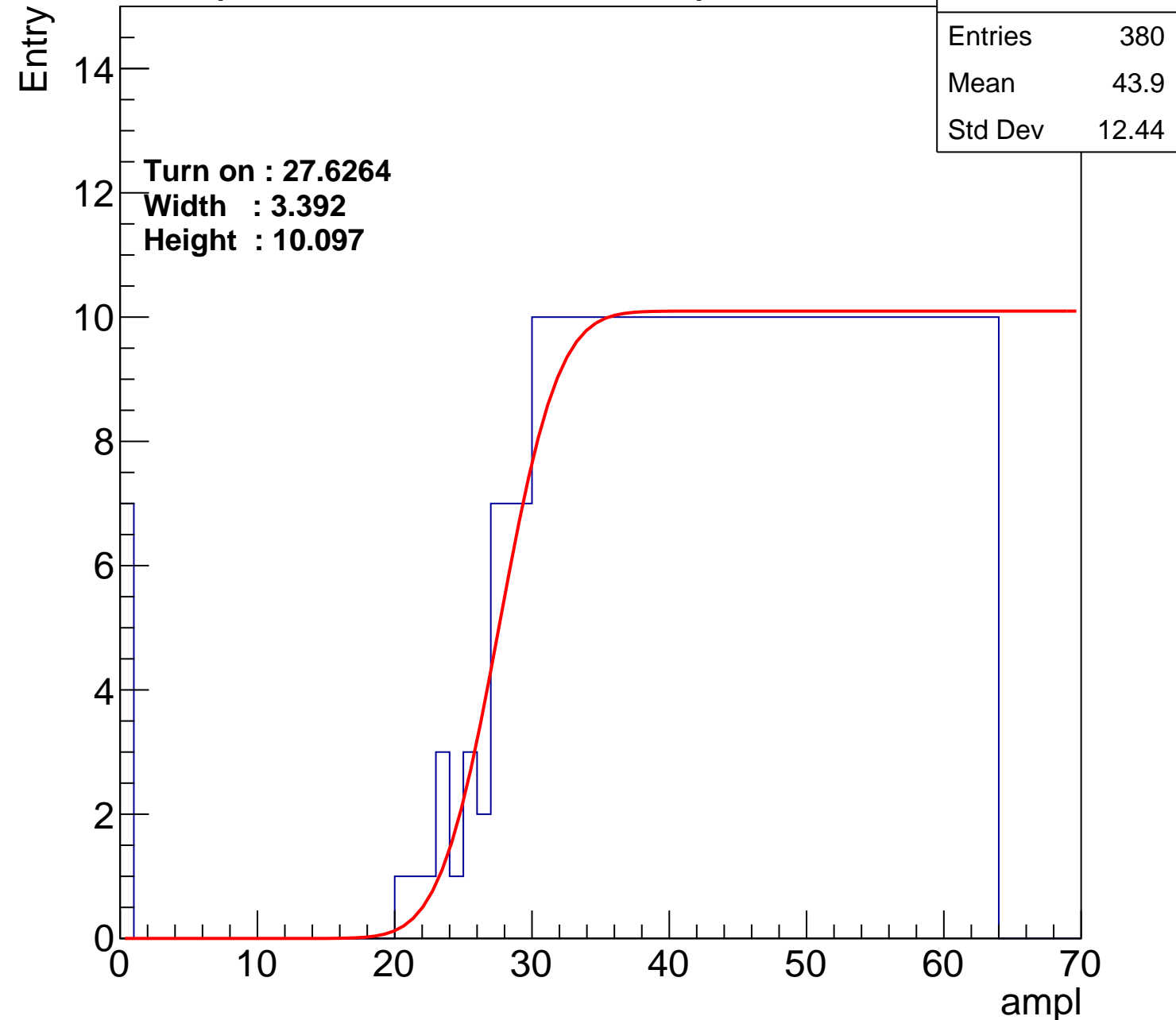
Width : 3.392

Height : 10.097

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch89

calib_packv5_042523_0143.root, FC#4, port A2

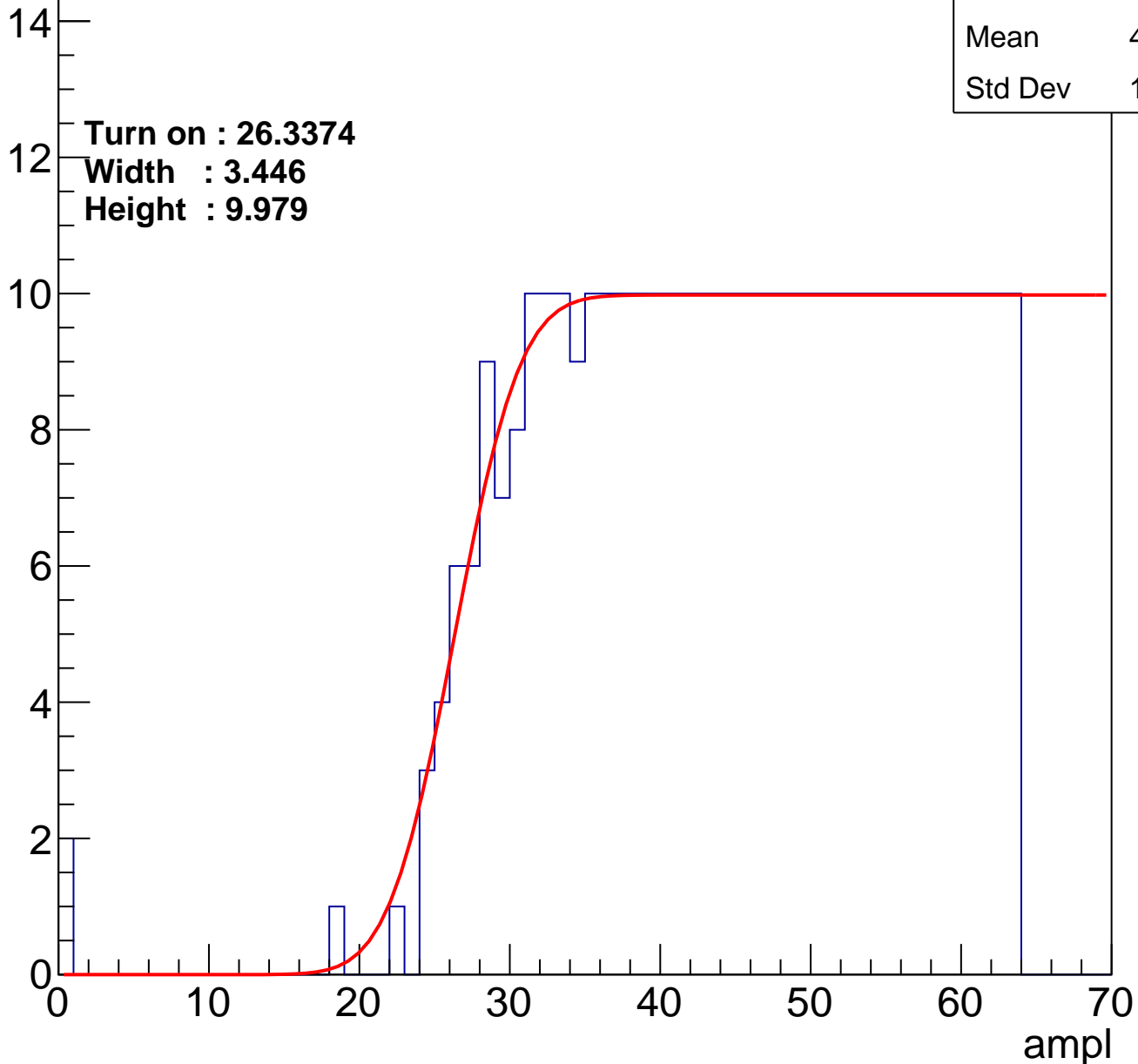
Entries	376
Mean	44.42
Std Dev	11.48

Turn on : 26.3374

Width : 3.446

Height : 9.979

Entry



B1L100S, U5-ch90

calib_packv5_042523_0143.root, FC#4, port A2

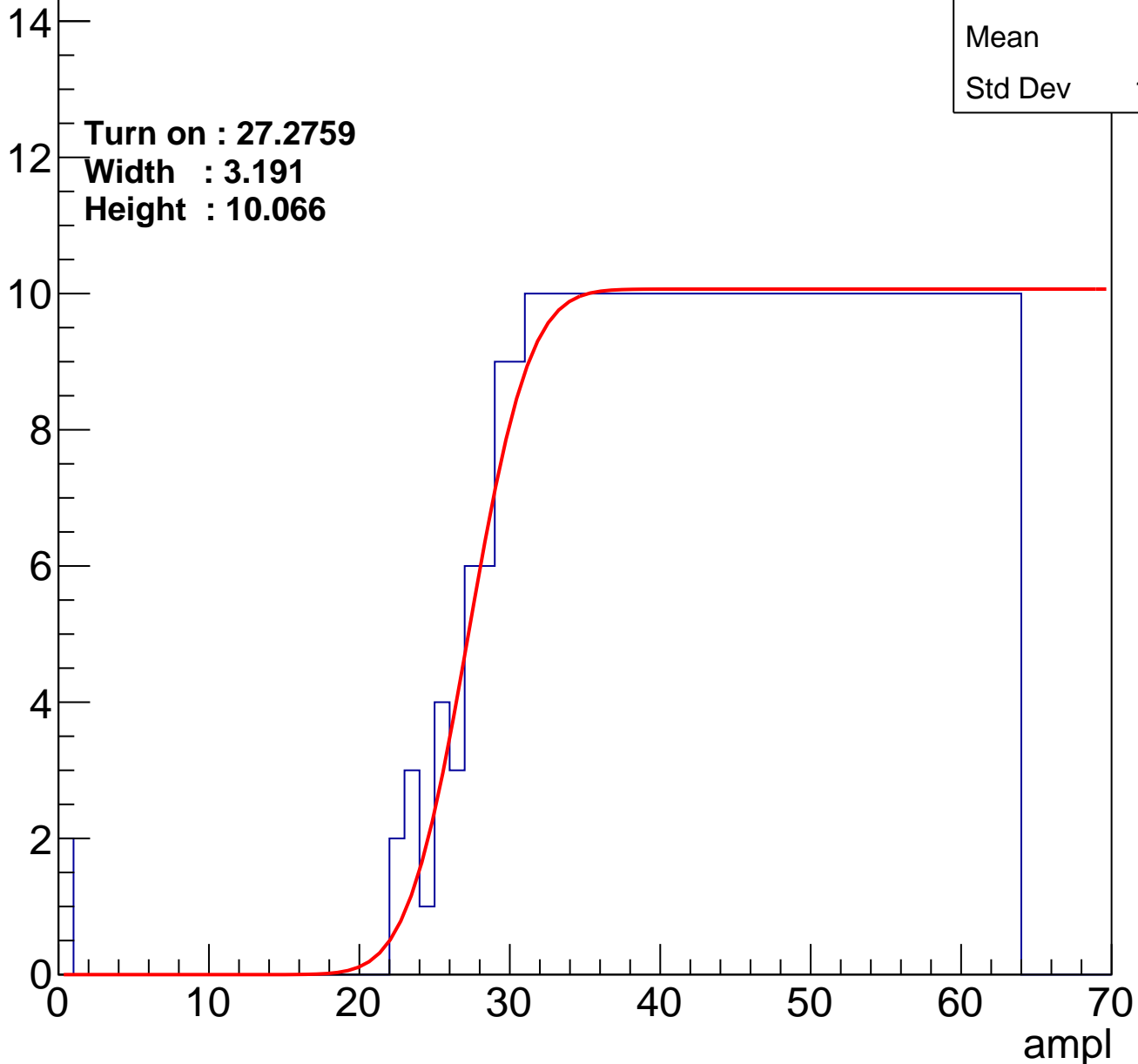
Entries	375
Mean	44.5
Std Dev	11.41

Turn on : 27.2759

Width : 3.191

Height : 10.066

Entry



B1L100S, U5-ch91

calib_packv5_042523_0143.root, FC#4, port A2

Entries	385
Mean	43.88
Std Dev	11.92

Turn on : 26.2946

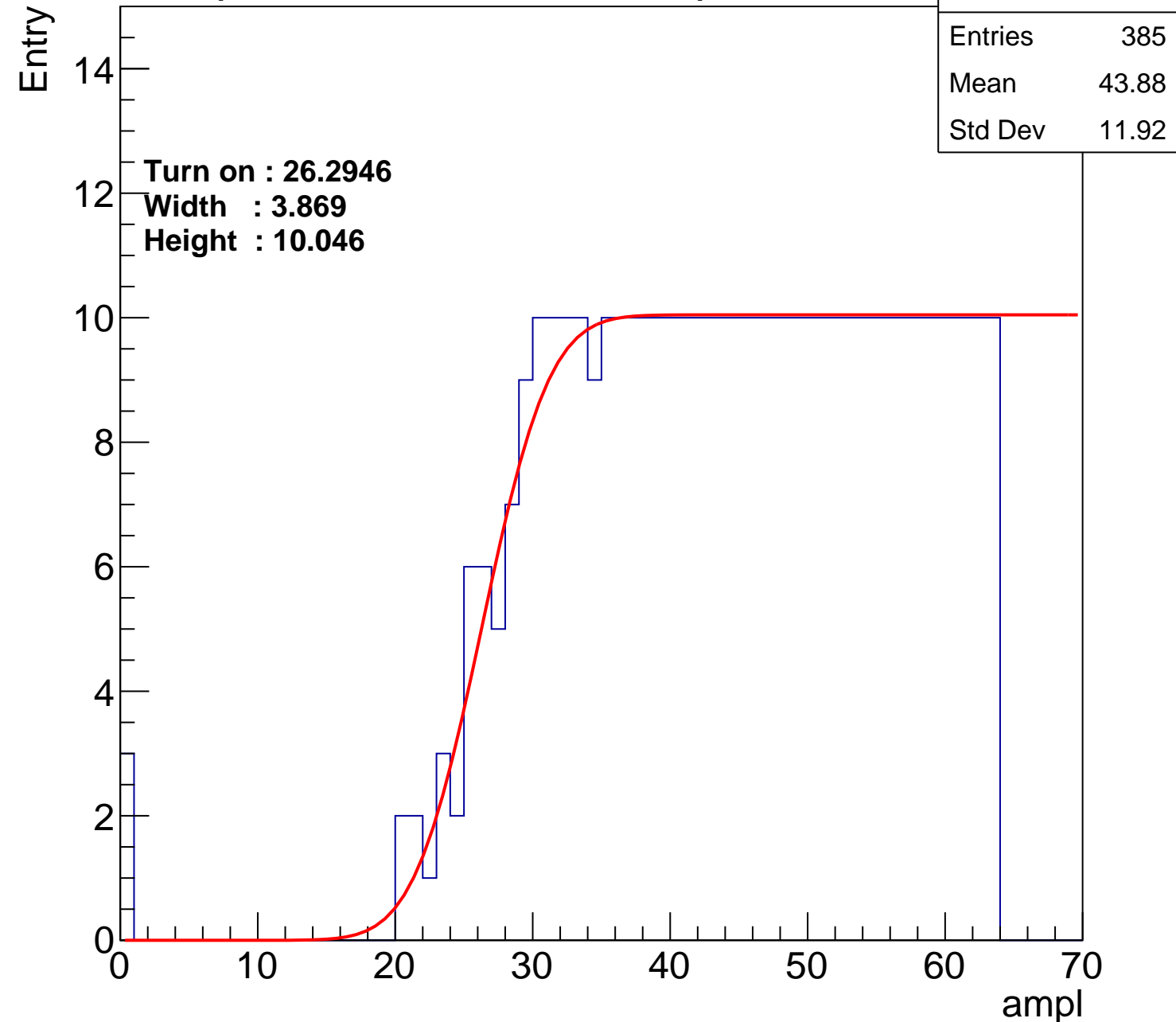
Width : 3.869

Height : 10.046

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch92

calib_packv5_042523_0143.root, FC#4, port A2

Entries	391
Mean	43.77
Std Dev	11.72

Turn on : 25.2557

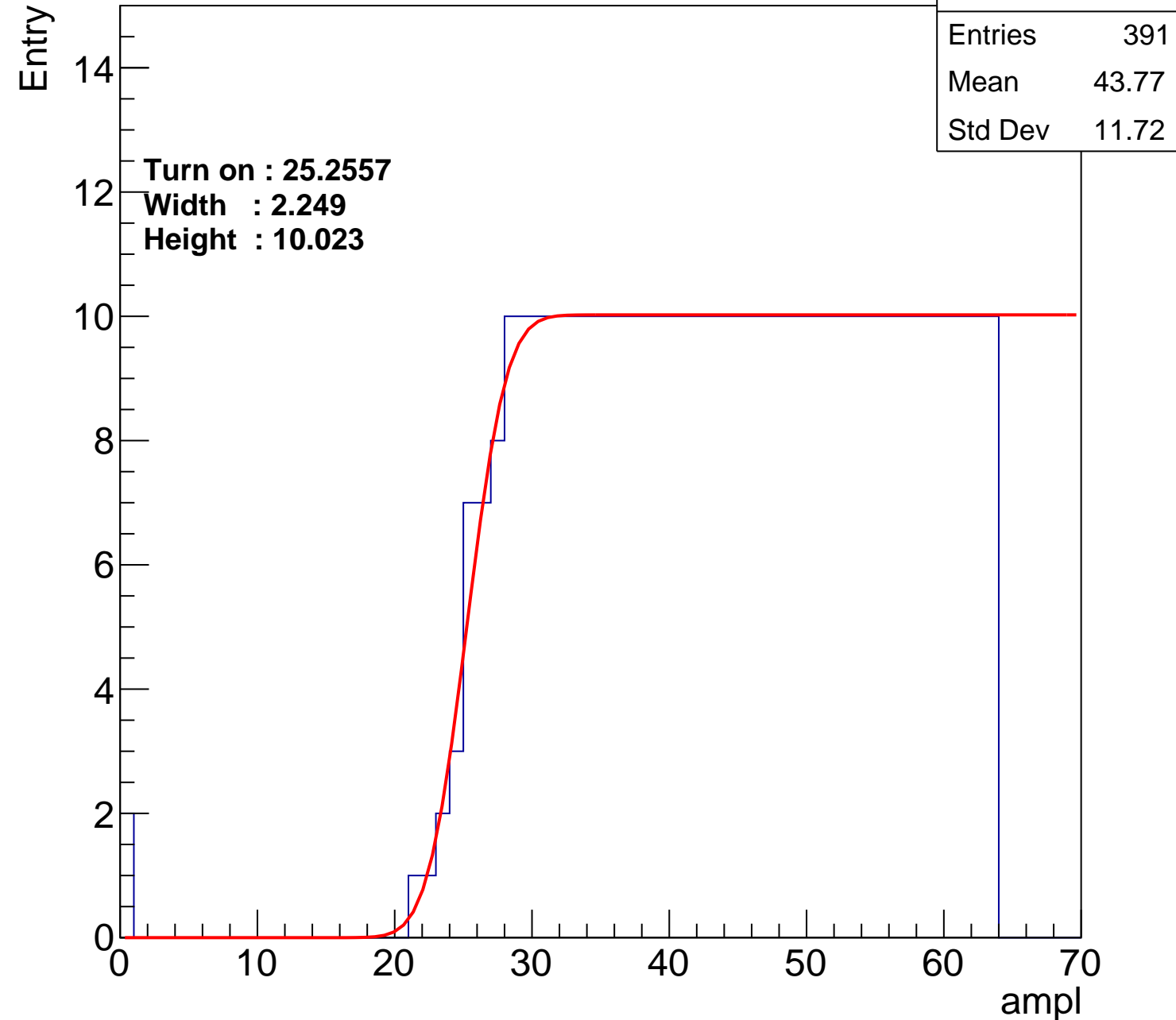
Width : 2.249

Height : 10.023

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch93

calib_packv5_042523_0143.root, FC#4, port A2

Entries	366
Mean	44.76
Std Dev	11.62

Turn on : 27.8756

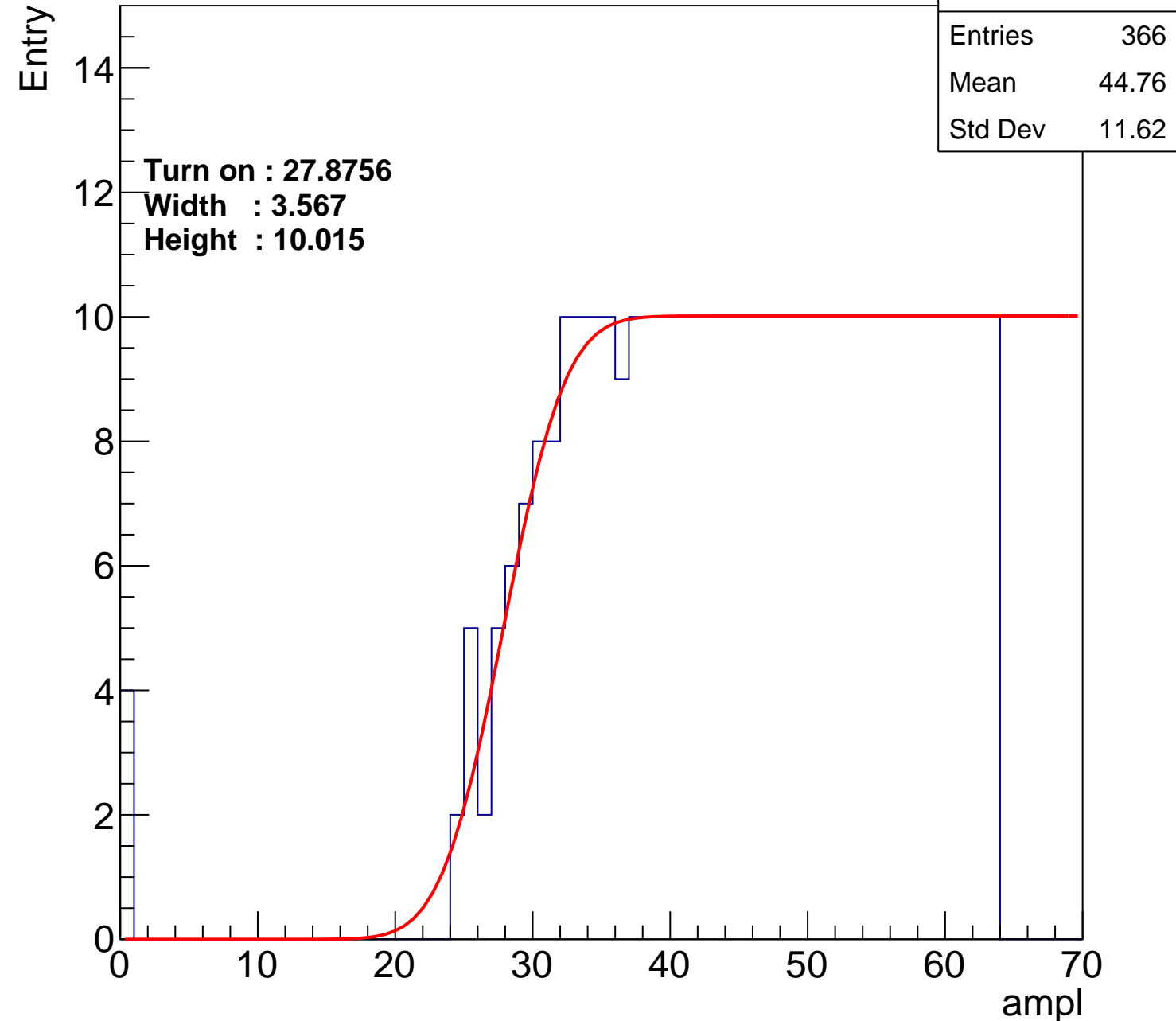
Width : 3.567

Height : 10.015

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch94

calib_packv5_042523_0143.root, FC#4, port A2

Entries	378
Mean	44.01
Std Dev	12.3

Turn on : 27.3016

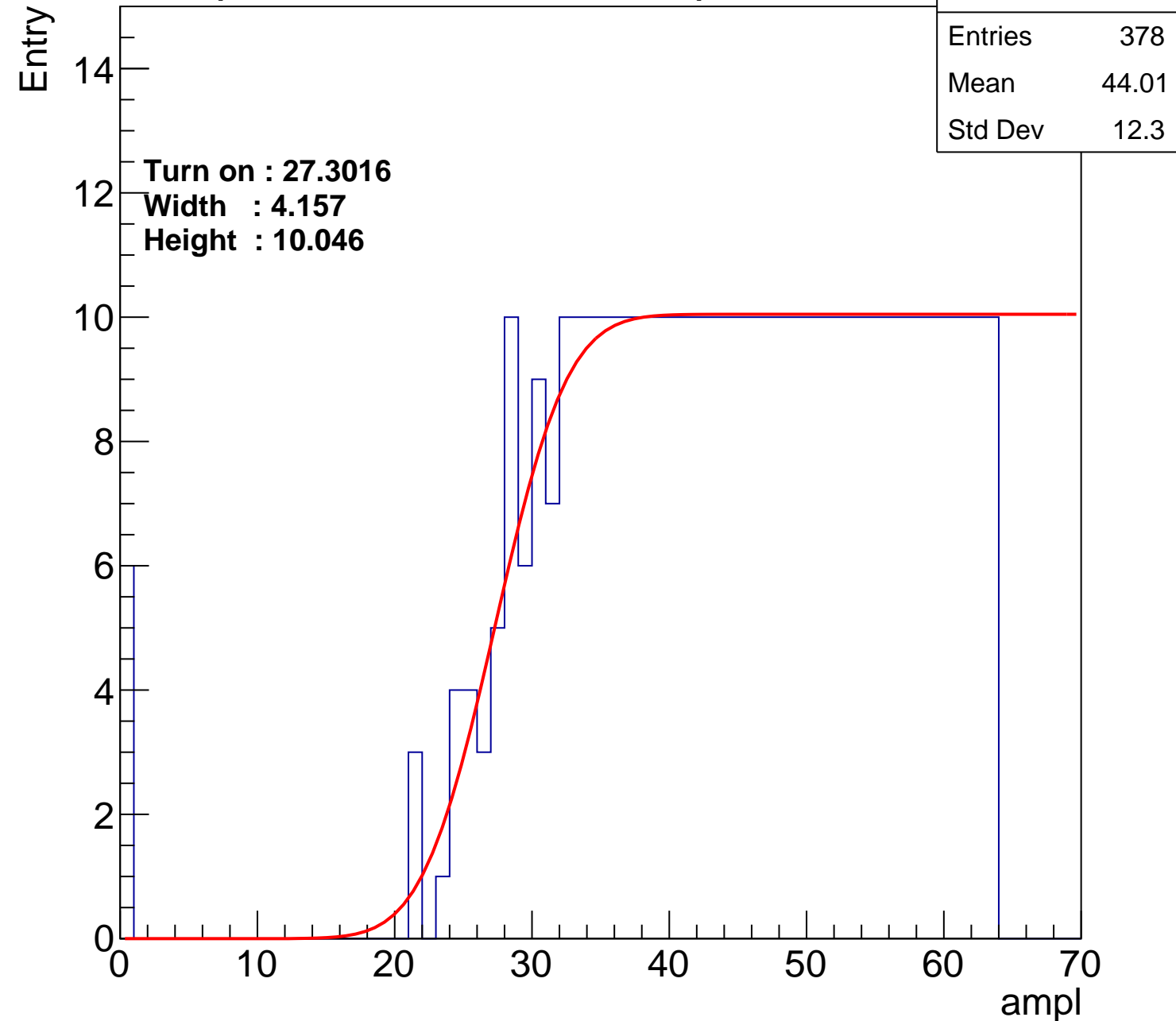
Width : 4.157

Height : 10.046

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch95

calib_packv5_042523_0143.root, FC#4, port A2

Entries	369
Mean	44.72
Std Dev	11.37

Turn on : 27.5297

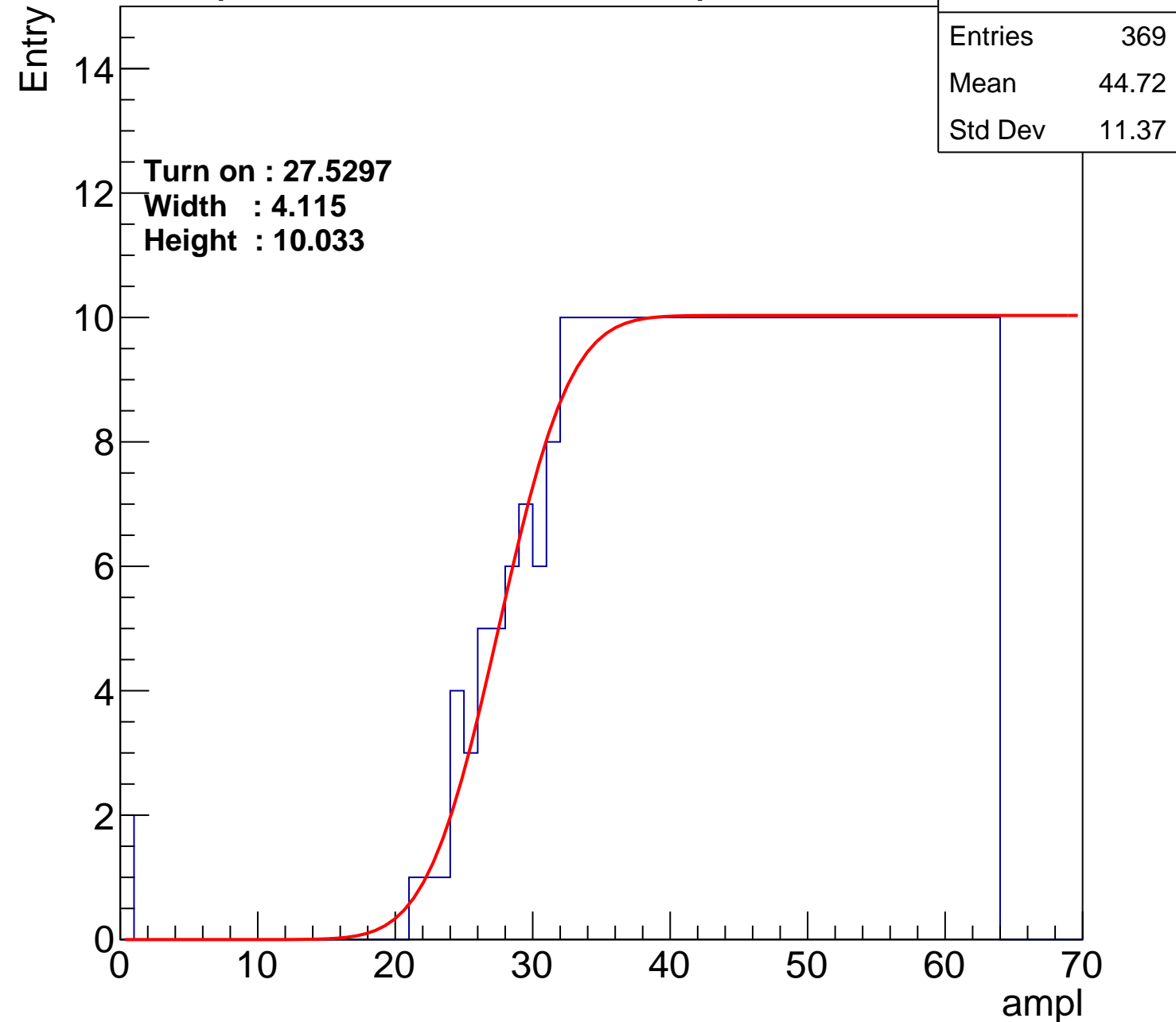
Width : 4.115

Height : 10.033

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch96

calib_packv5_042523_0143.root, FC#4, port A2

Entries	383
Mean	44.06
Std Dev	11.69

Turn on : 26.3909

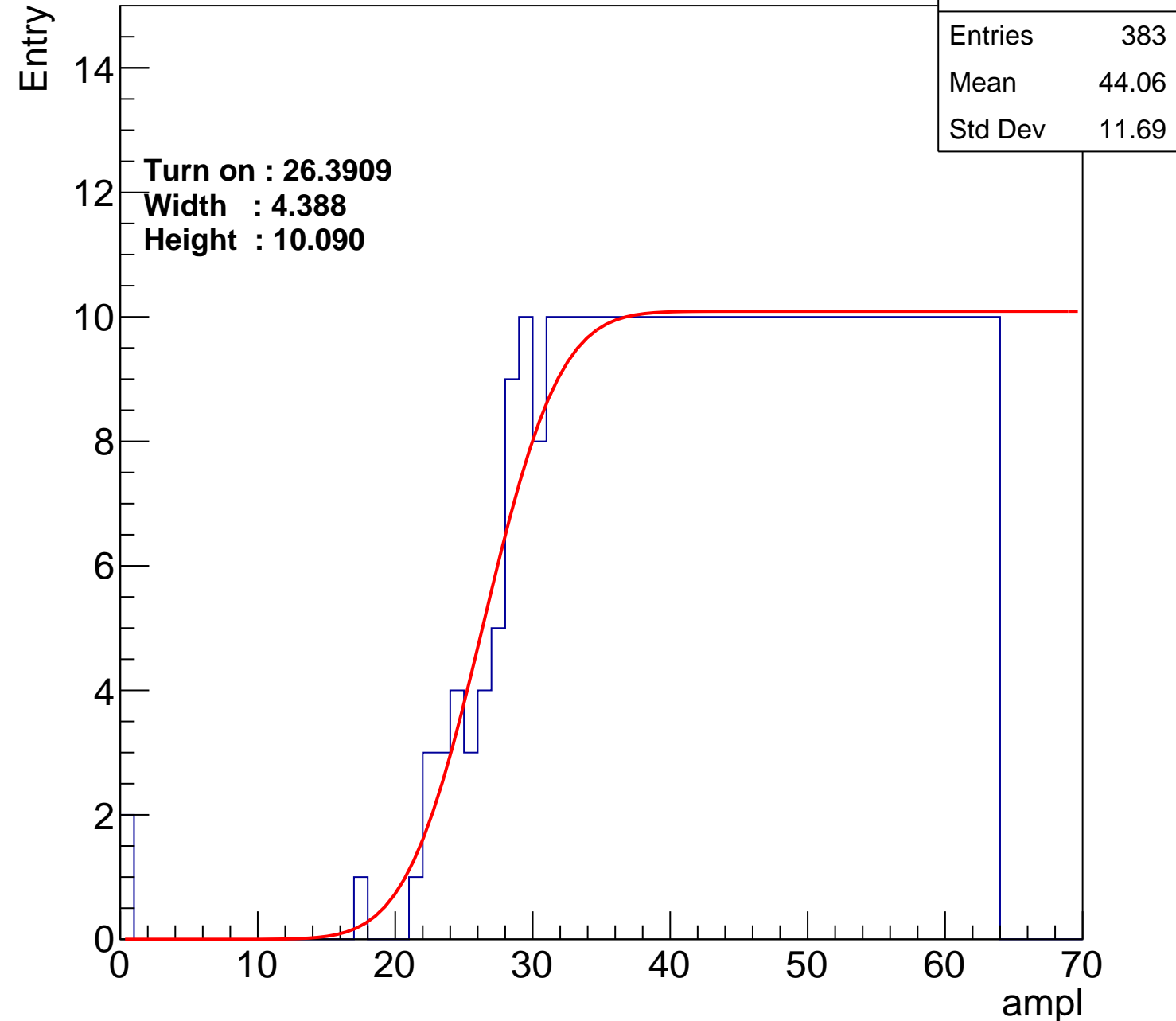
Width : 4.388

Height : 10.090

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch97

calib_packv5_042523_0143.root, FC#4, port A2

Entries	398
Mean	43.3
Std Dev	12.16

Turn on : 23.6685

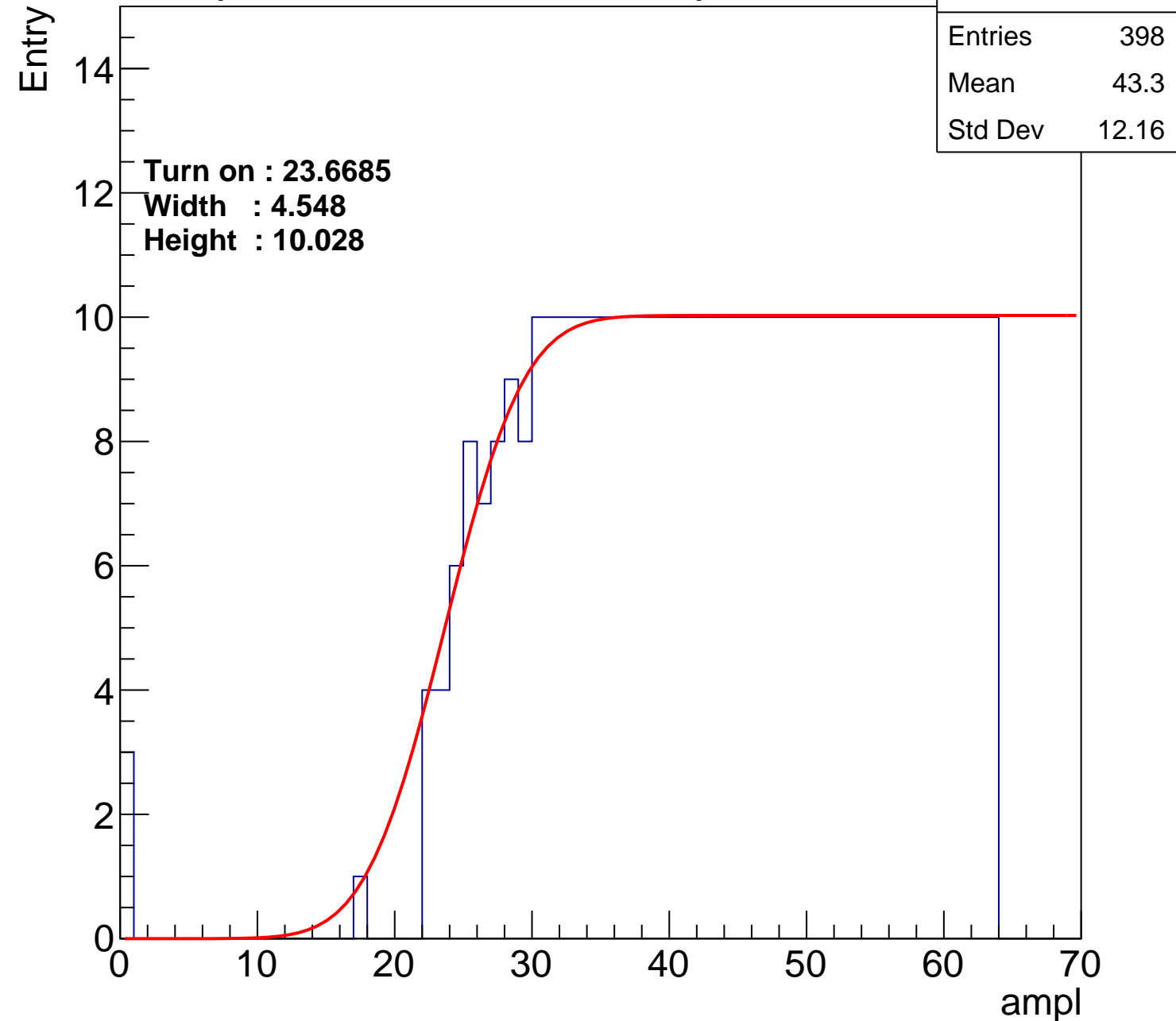
Width : 4.548

Height : 10.028

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch98

calib_packv5_042523_0143.root, FC#4, port A2

Entries	399
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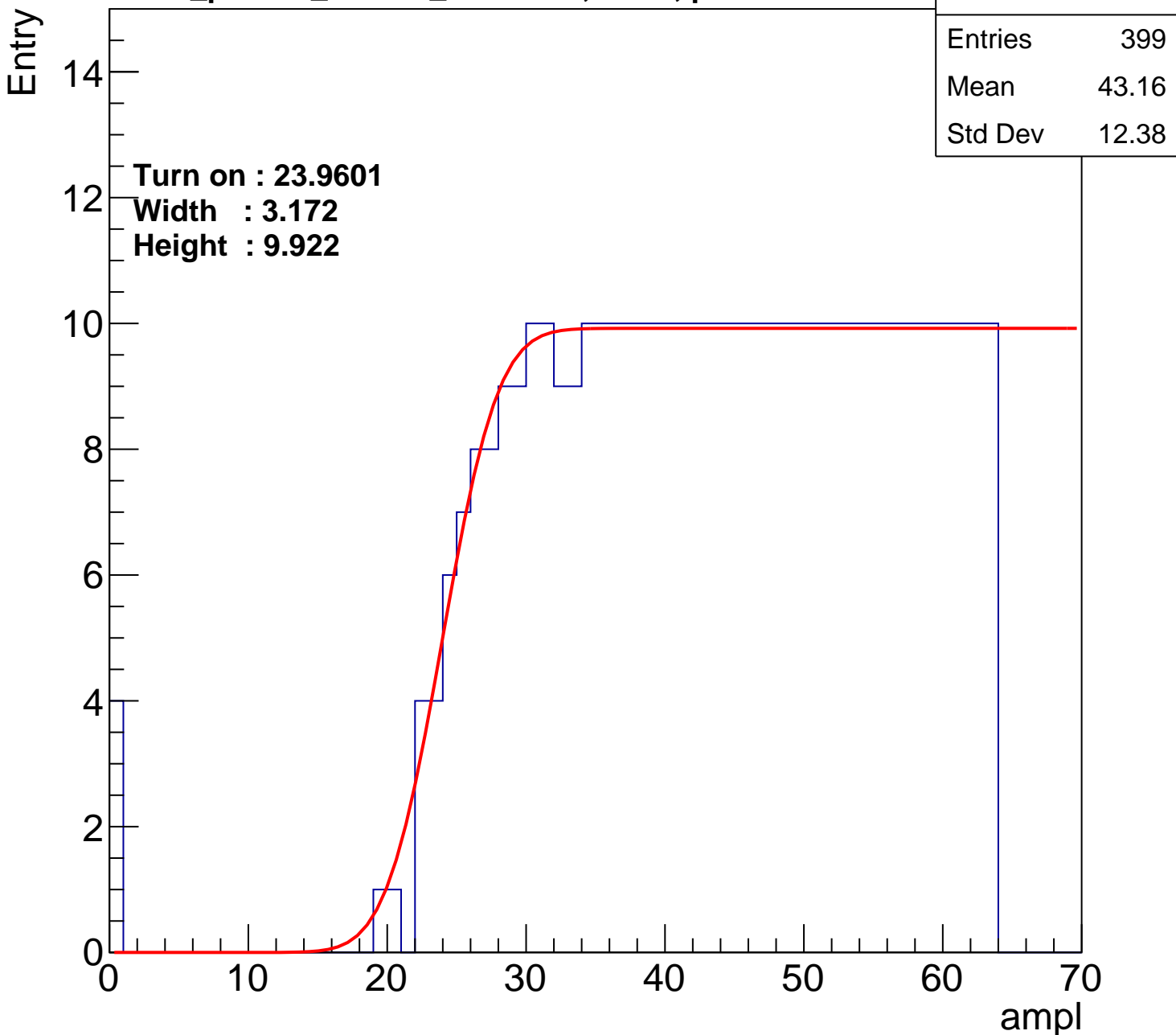
Mean	43.16
------	-------

Std Dev	12.38
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Turn on : 23.9601

Width : 3.172

Height : 9.922



B1L100S, U5-ch99

calib_packv5_042523_0143.root, FC#4, port A2

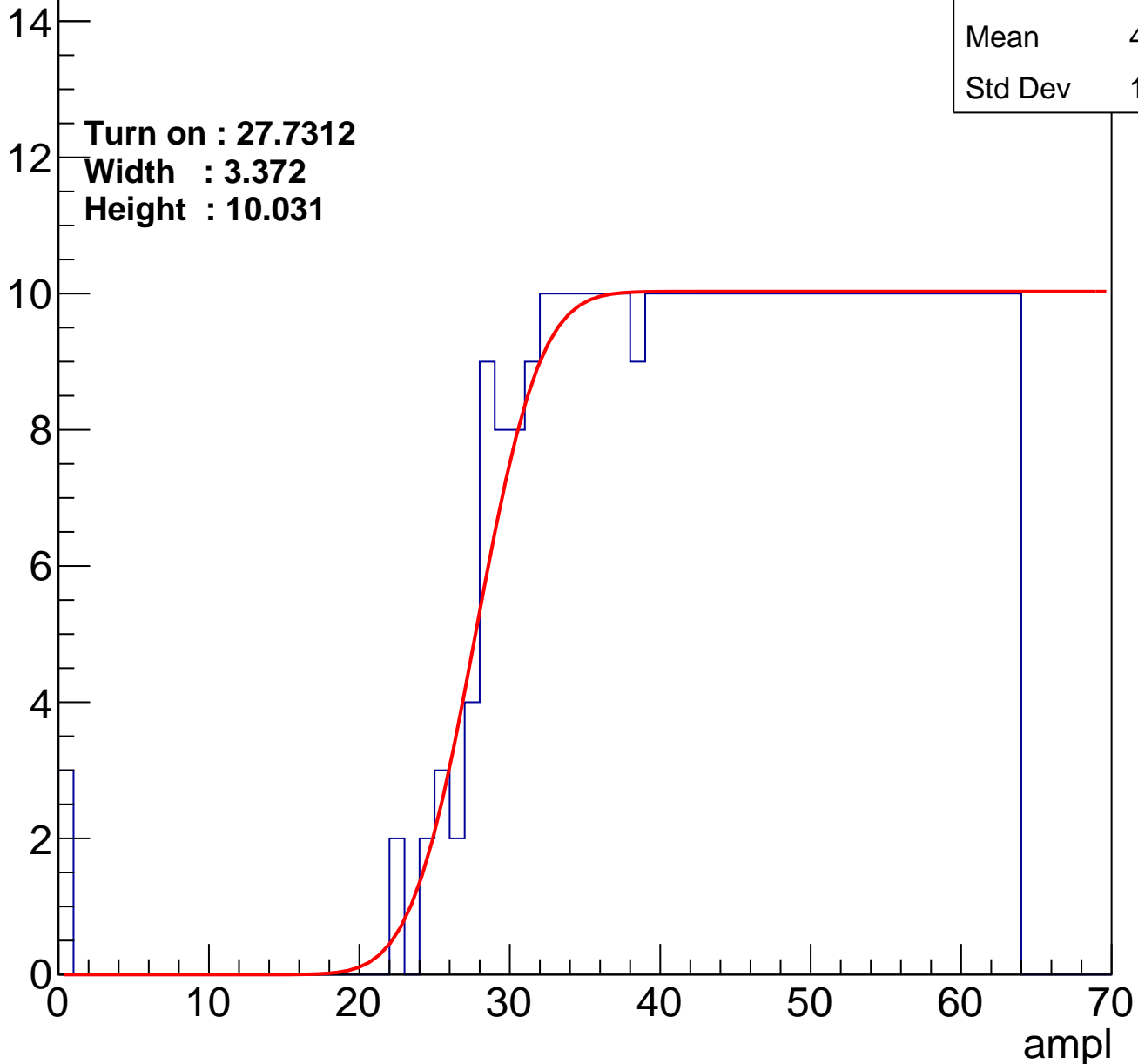
Entries	369
Mean	44.69
Std Dev	11.48

Turn on : 27.7312

Width : 3.372

Height : 10.031

Entry



B1L100S, U5-ch100

calib_packv5_042523_0143.root, FC#4, port A2

Entries	393
Mean	43.58
Std Dev	11.97

Turn on : 25.0054

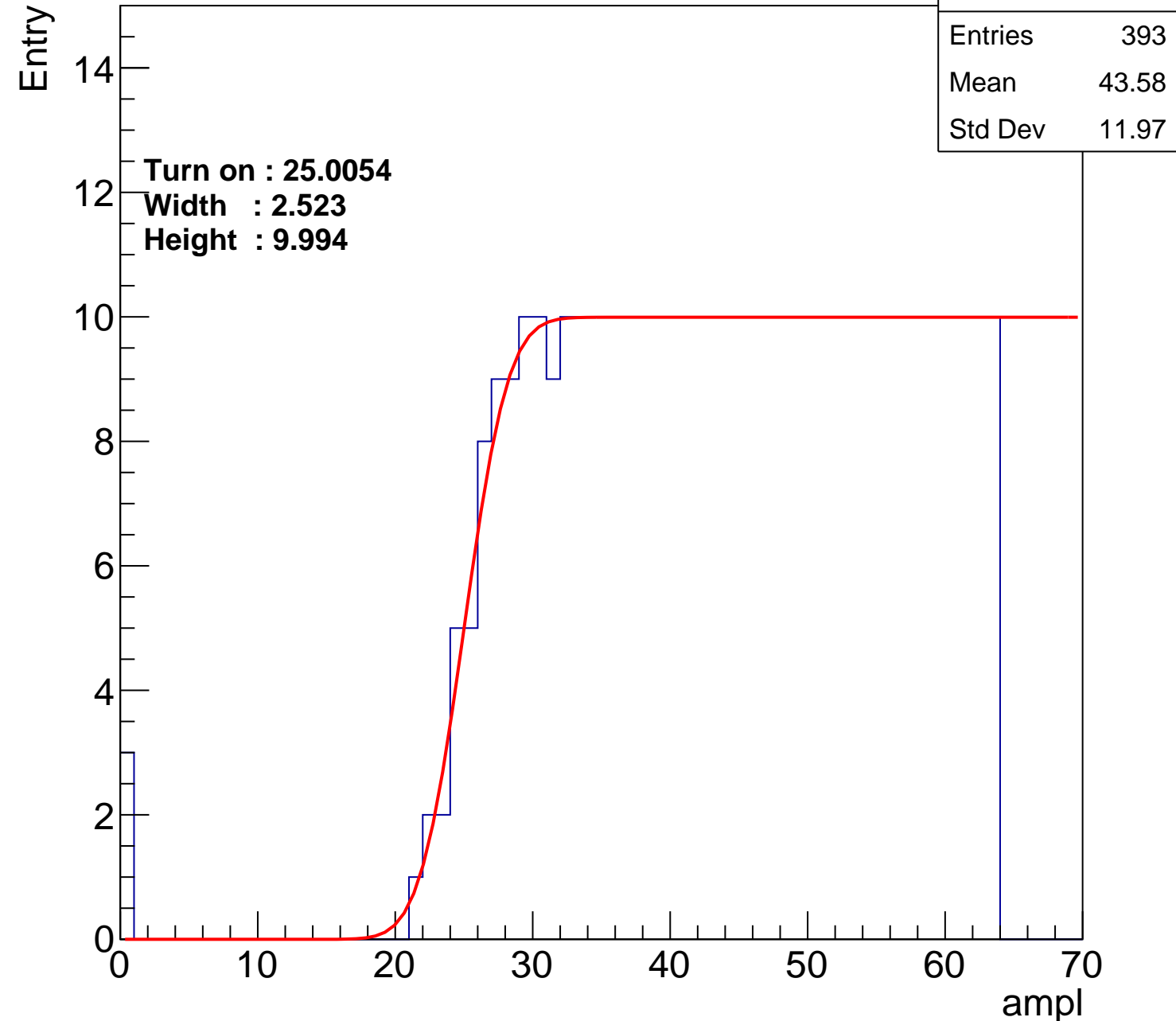
Width : 2.523

Height : 9.994

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch101

calib_packv5_042523_0143.root, FC#4, port A2

Entries	389
Mean	43.75
Std Dev	11.93

Turn on : 26.0985

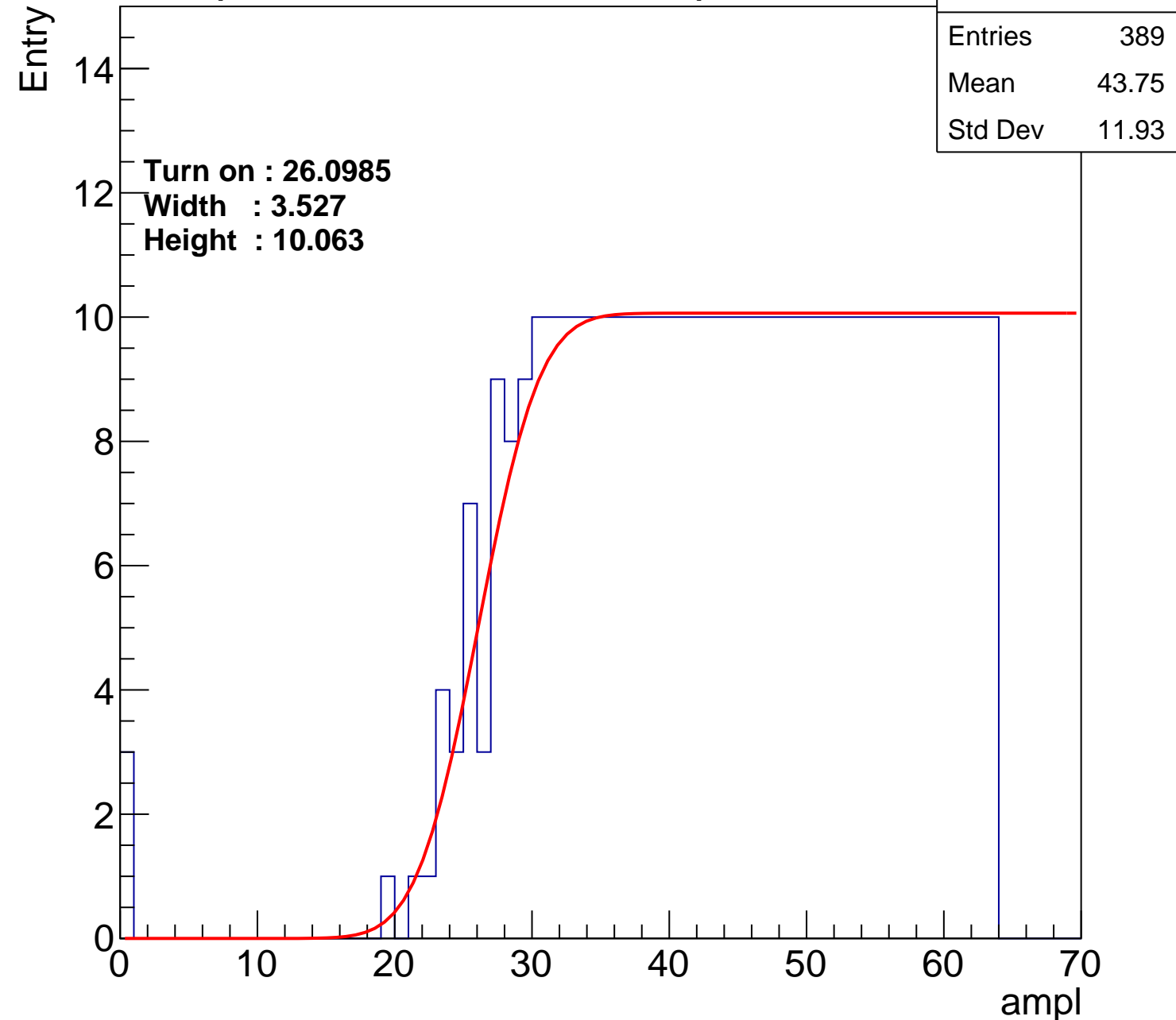
Width : 3.527

Height : 10.063

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch102

calib_packv5_042523_0143.root, FC#4, port A2

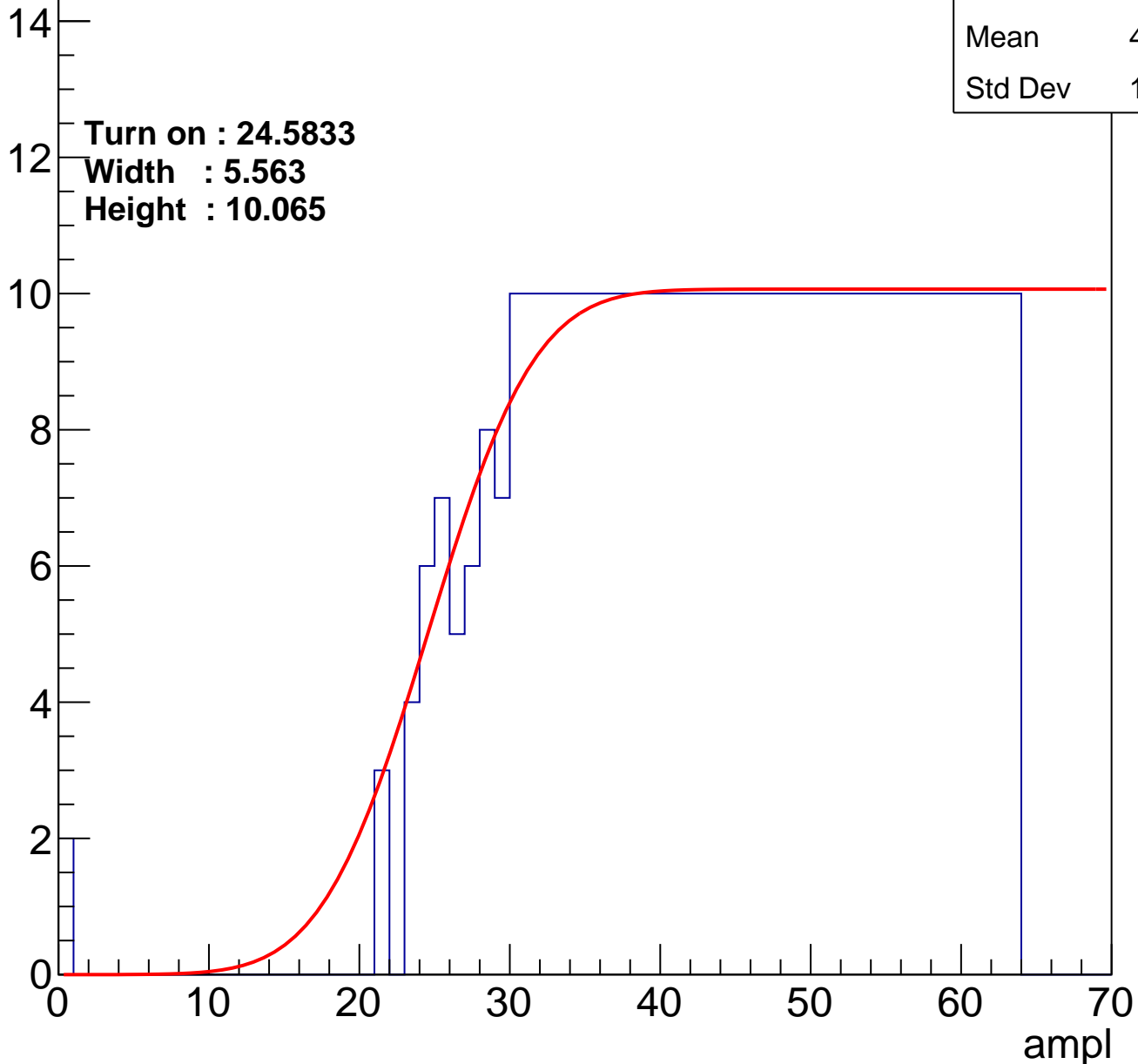
Entries	388
Mean	43.82
Std Dev	11.79

Turn on : 24.5833

Width : 5.563

Height : 10.065

Entry



B1L100S, U5-ch103

calib_packv5_042523_0143.root, FC#4, port A2

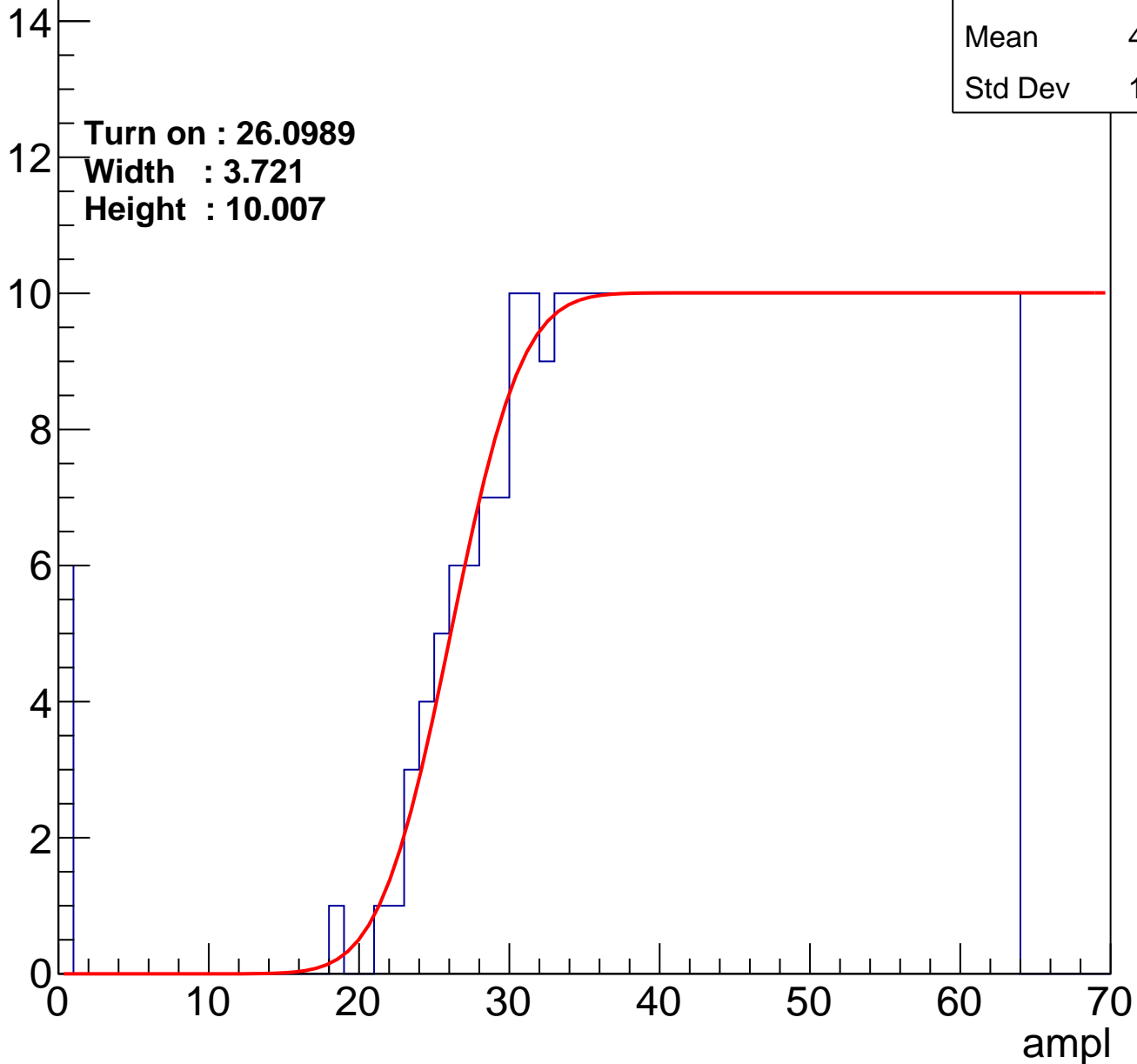
Entries	386
Mean	43.64
Std Dev	12.44

Turn on : 26.0989

Width : 3.721

Height : 10.007

Entry



B1L100S, U5-ch104

calib_packv5_042523_0143.root, FC#4, port A2

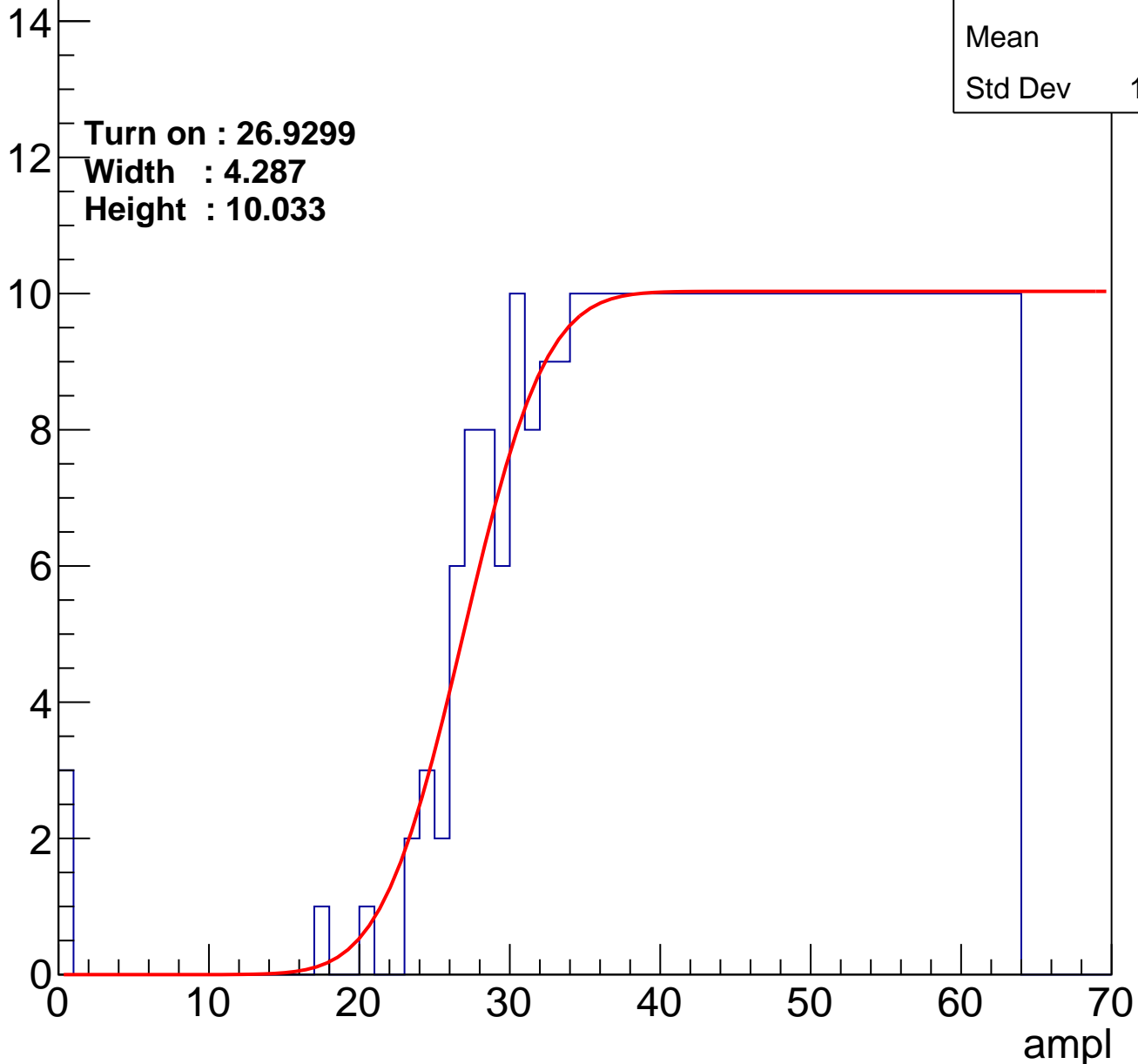
Entries	376
Mean	44.3
Std Dev	11.74

Turn on : 26.9299

Width : 4.287

Height : 10.033

Entry



B1L100S, U5-ch105

calib_packv5_042523_0143.root, FC#4, port A2

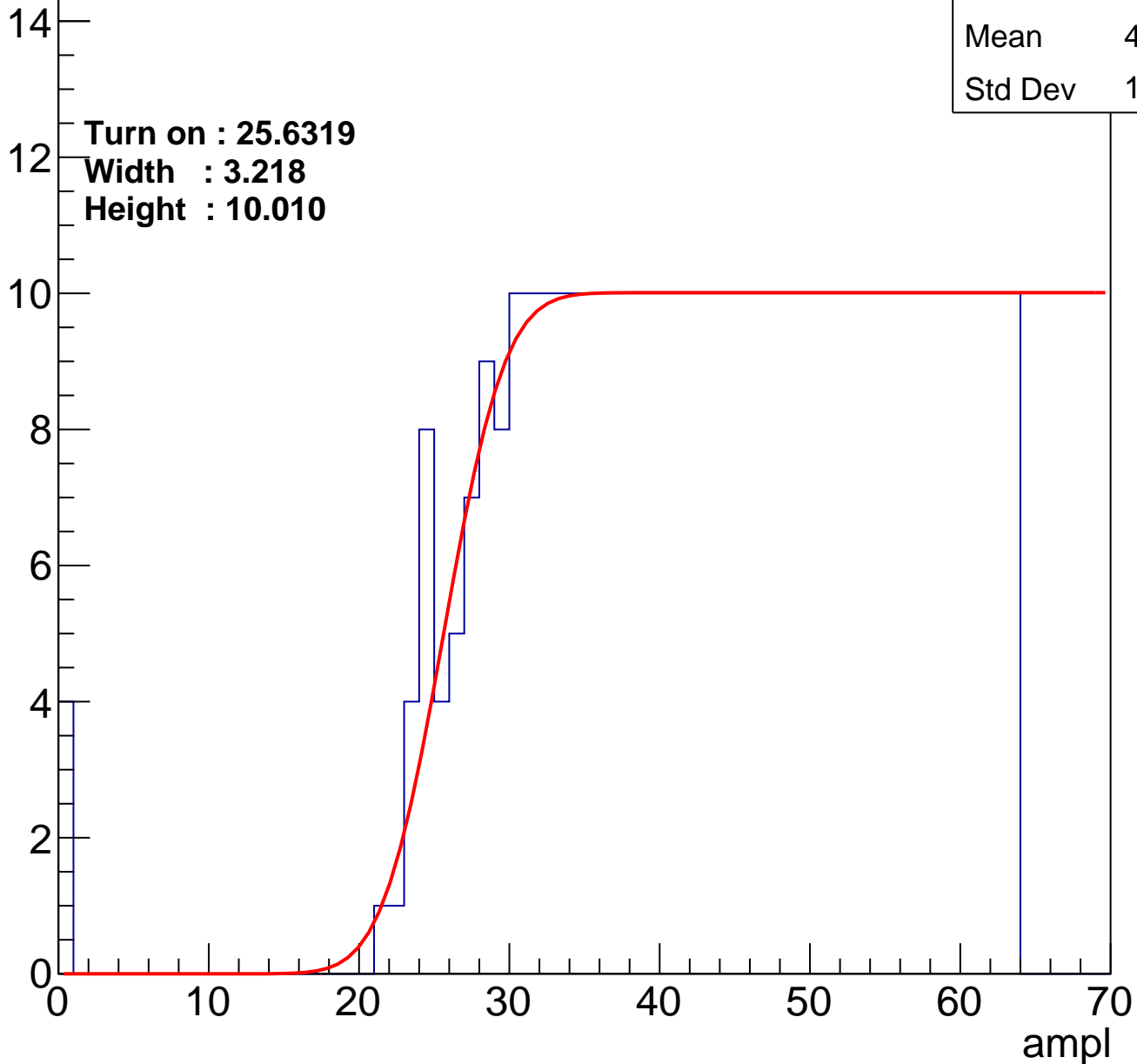
Entries	391
Mean	43.58
Std Dev	12.15

Turn on : 25.6319

Width : 3.218

Height : 10.010

Entry



B1L100S, U5-ch106

calib_packv5_042523_0143.root, FC#4, port A2

Entries	381
Mean	44.11
Std Dev	11.78

Turn on : 26.5453

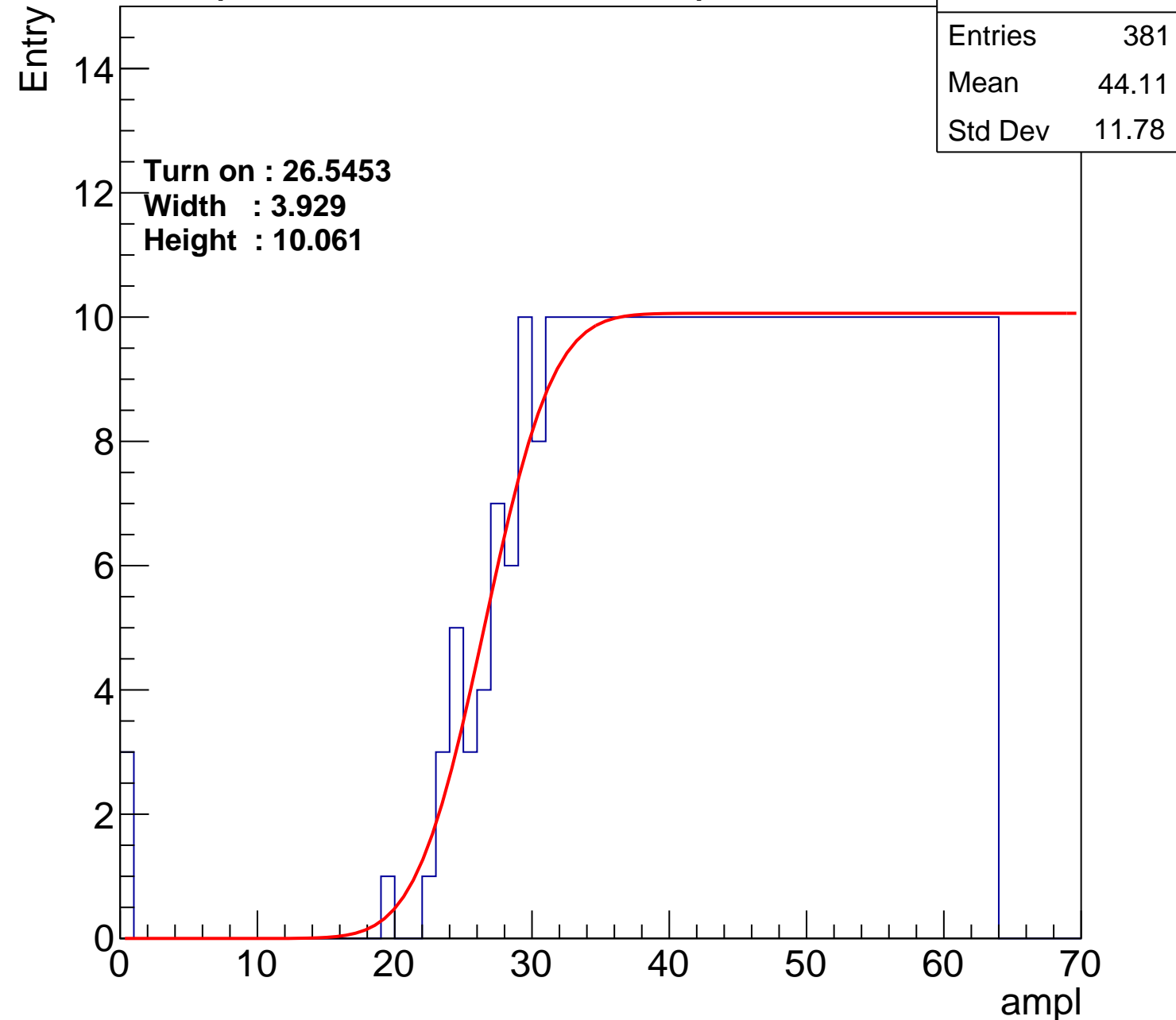
Width : 3.929

Height : 10.061

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch107

calib_packv5_042523_0143.root, FC#4, port A2

Entries	380
Mean	44.28
Std Dev	11.42

Turn on : 26.2413

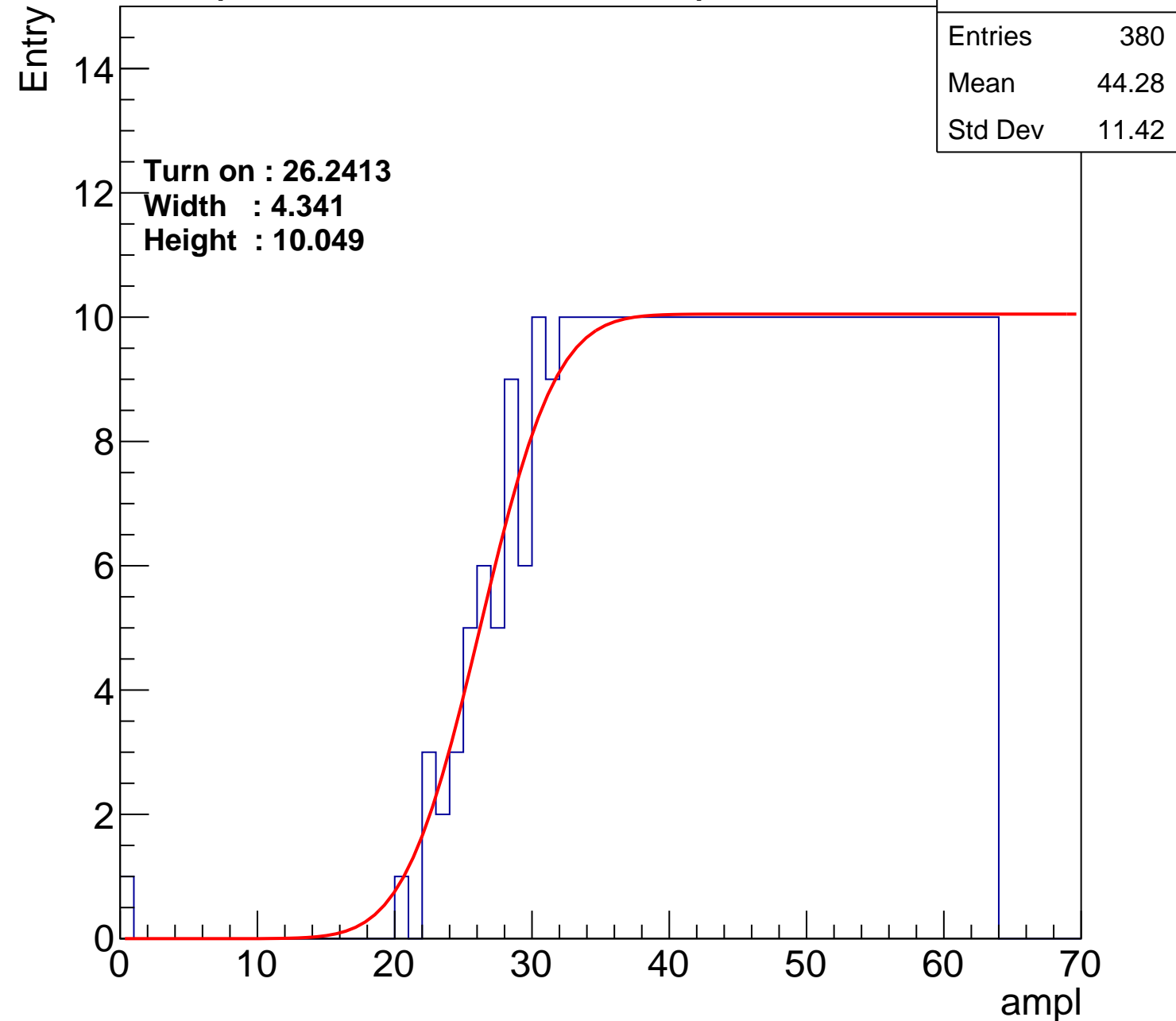
Width : 4.341

Height : 10.049

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch108

calib_packv5_042523_0143.root, FC#4, port A2

Entries	390
Mean	43.64
Std Dev	12.11

Turn on : 26.0468

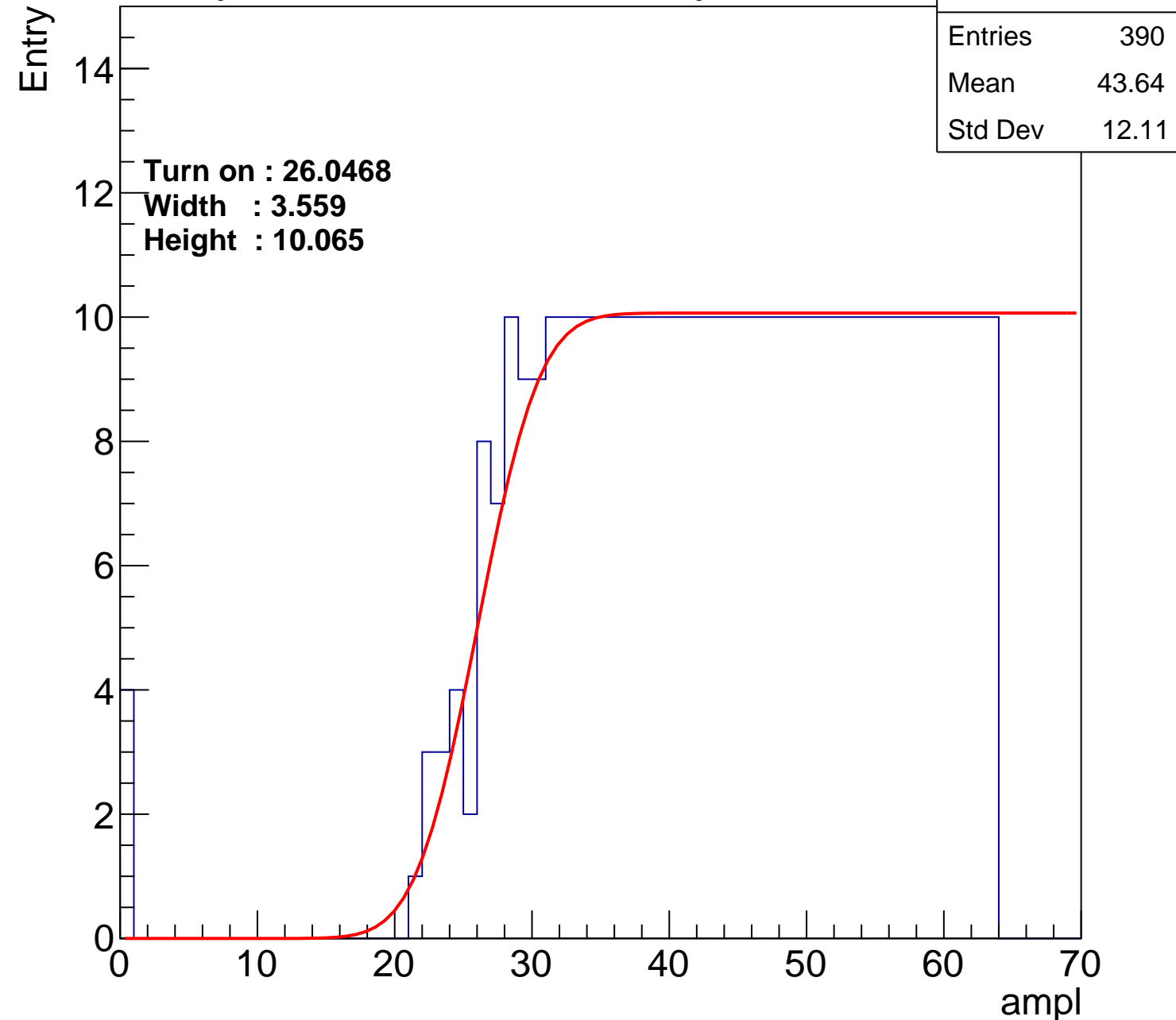
Width : 3.559

Height : 10.065

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch109

calib_packv5_042523_0143.root, FC#4, port A2

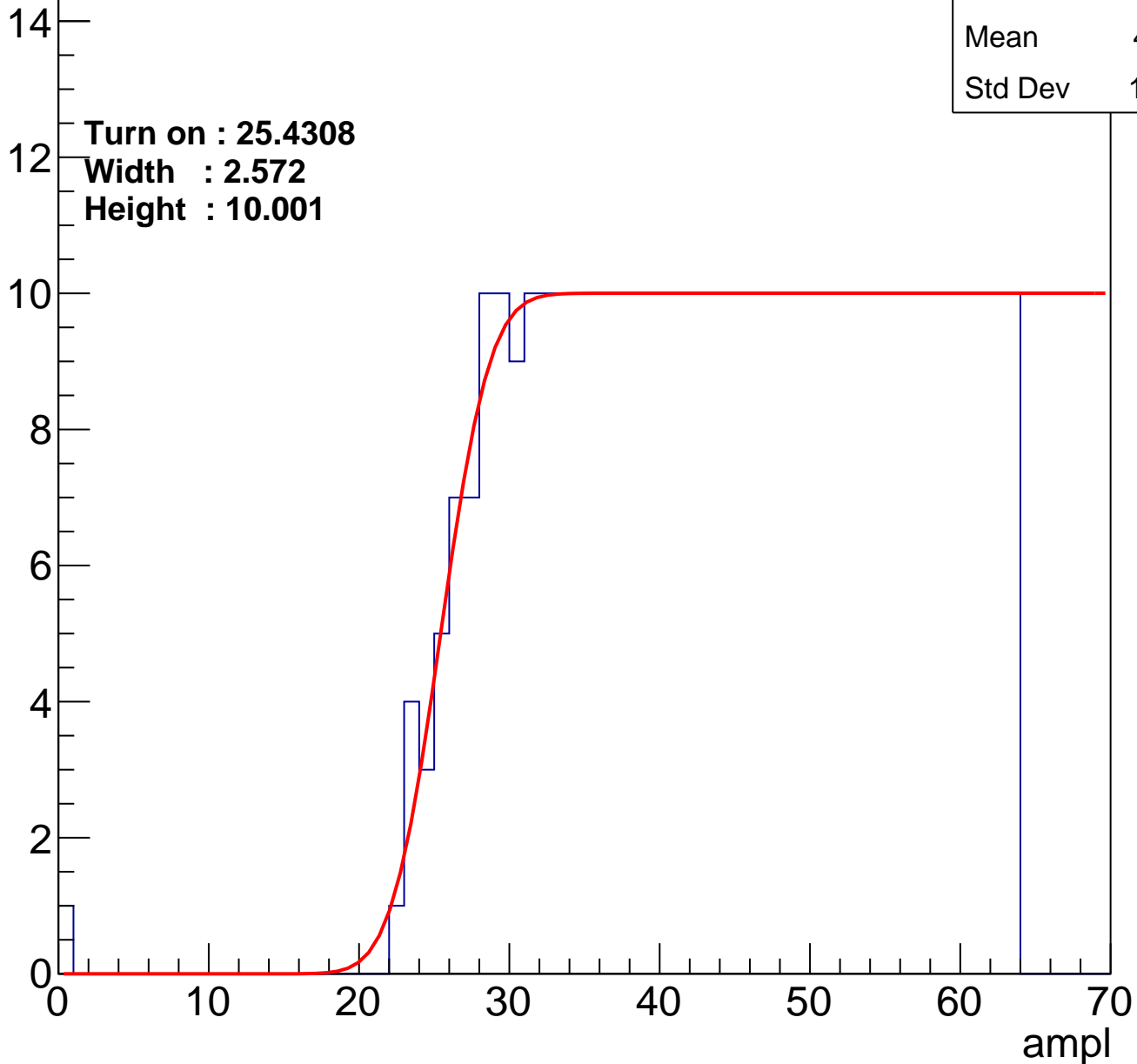
Entries	387
Mean	44.01
Std Dev	11.47

Turn on : 25.4308

Width : 2.572

Height : 10.001

Entry



B1L100S, U5-ch110

calib_packv5_042523_0143.root, FC#4, port A2

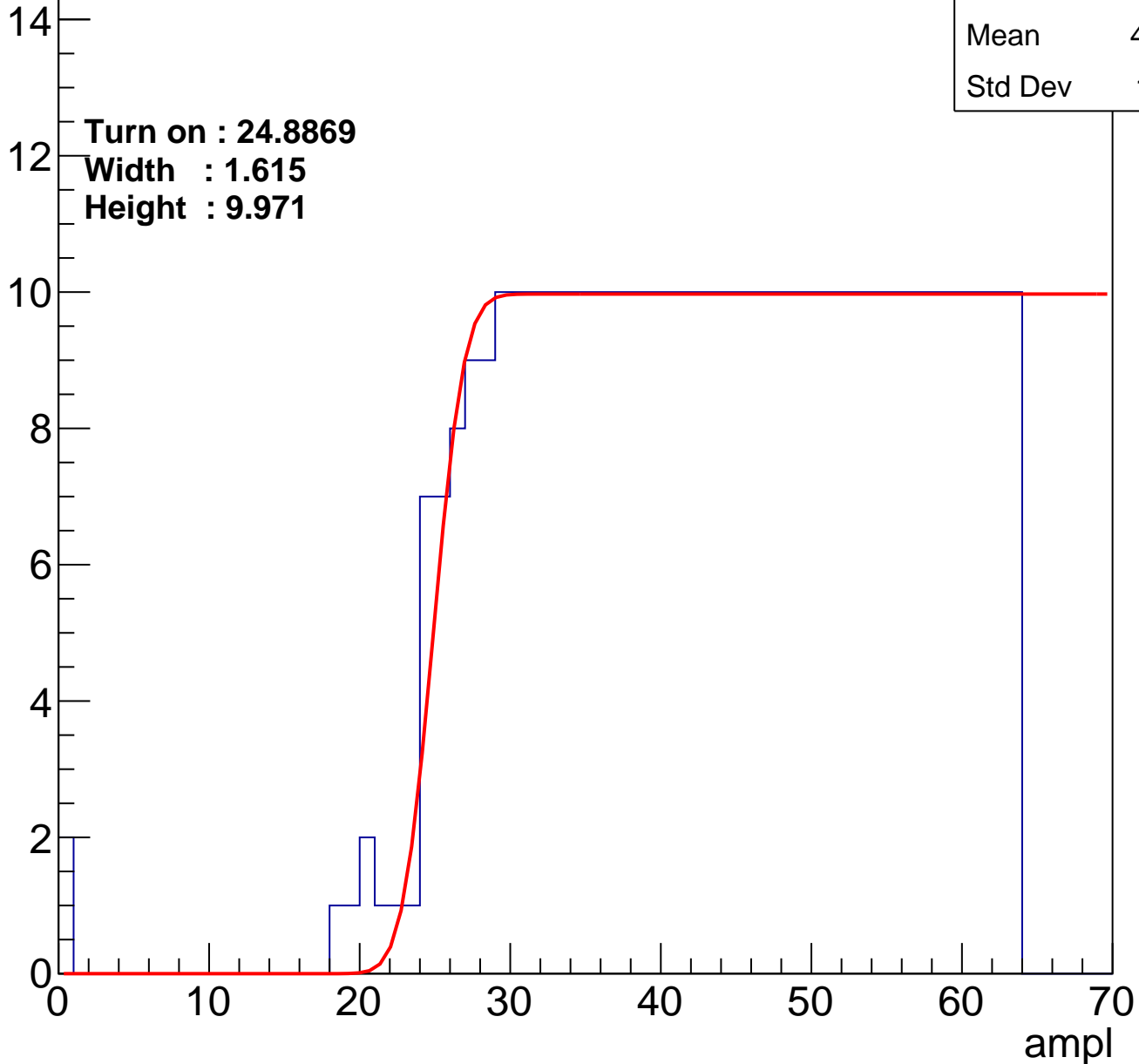
Entries	399
Mean	43.33
Std Dev	12.01

Turn on : 24.8869

Width : 1.615

Height : 9.971

Entry



B1L100S, U5-ch111

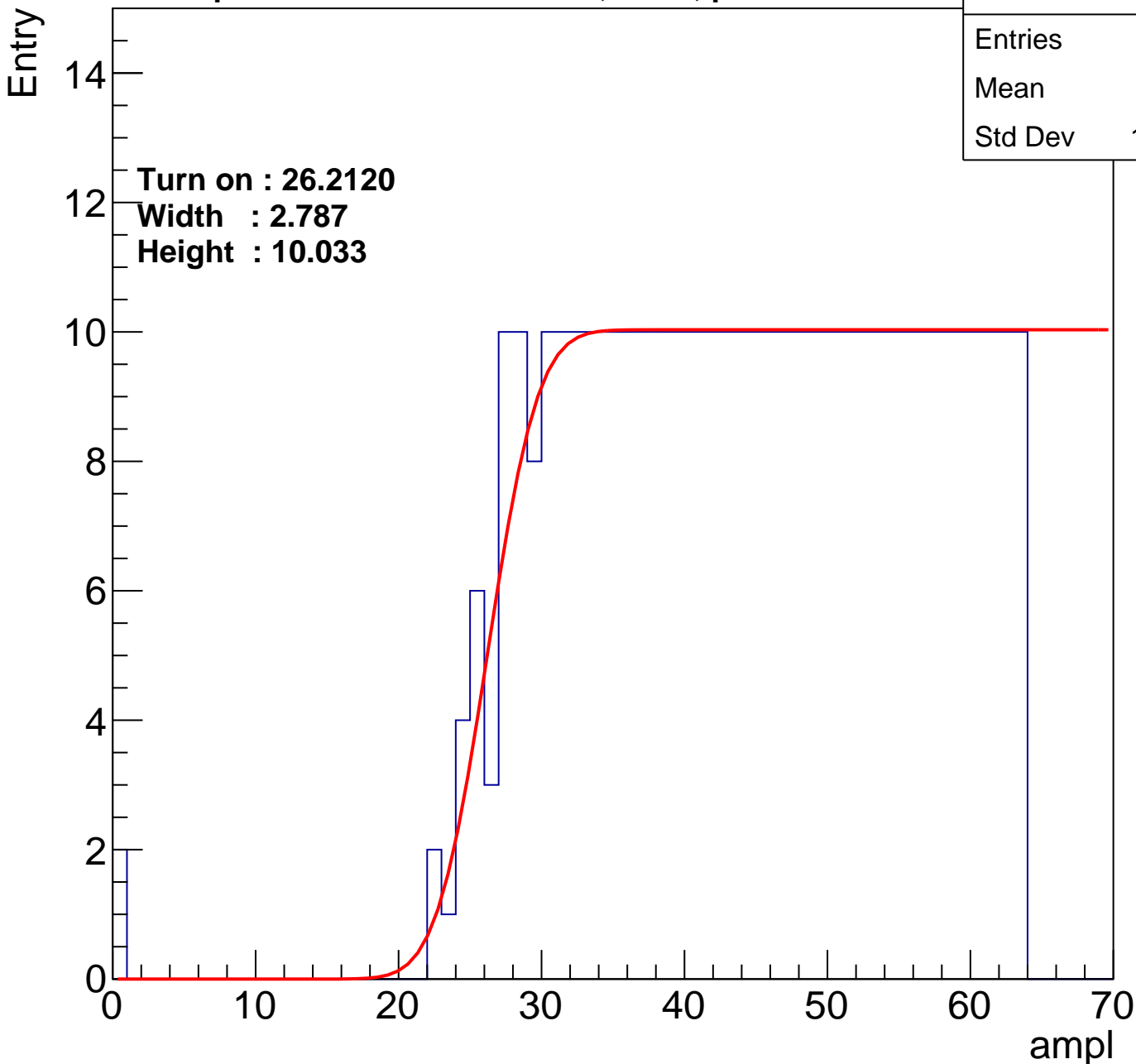
calib_packv5_042523_0143.root, FC#4, port A2

Entries	386
Mean	44
Std Dev	11.62

Turn on : 26.2120

Width : 2.787

Height : 10.033



B1L100S, U5-ch112

calib_packv5_042523_0143.root, FC#4, port A2

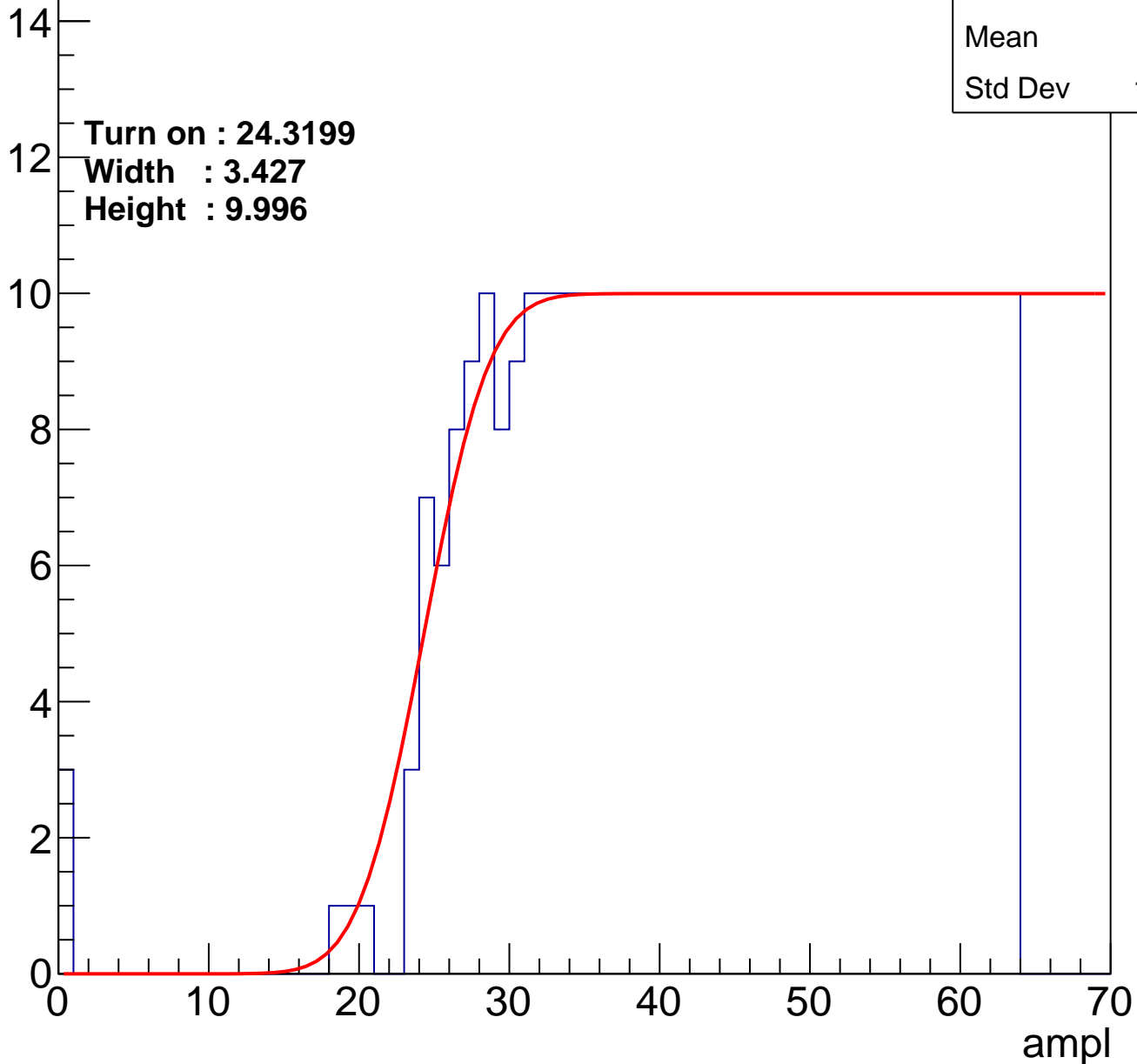
Entries	396
Mean	43.4
Std Dev	12.11

Turn on : 24.3199

Width : 3.427

Height : 9.996

Entry



B1L100S, U5-ch113

calib_packv5_042523_0143.root, FC#4, port A2

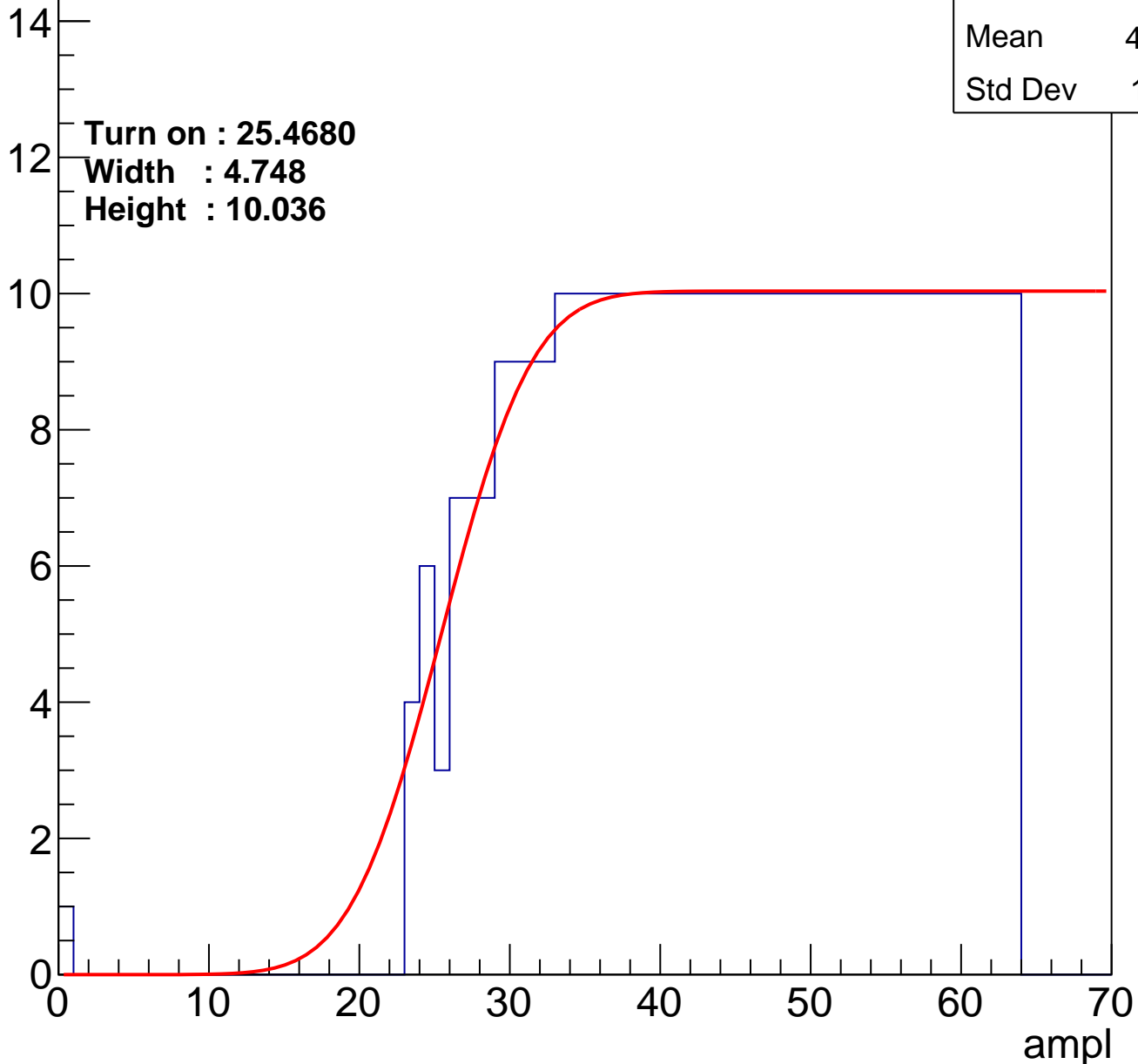
Entries	381
Mean	44.24
Std Dev	11.41

Turn on : 25.4680

Width : 4.748

Height : 10.036

Entry



B1L100S, U5-ch114

calib_packv5_042523_0143.root, FC#4, port A2

Entries	387
Mean	43.86
Std Dev	11.86

Turn on : 25.9545

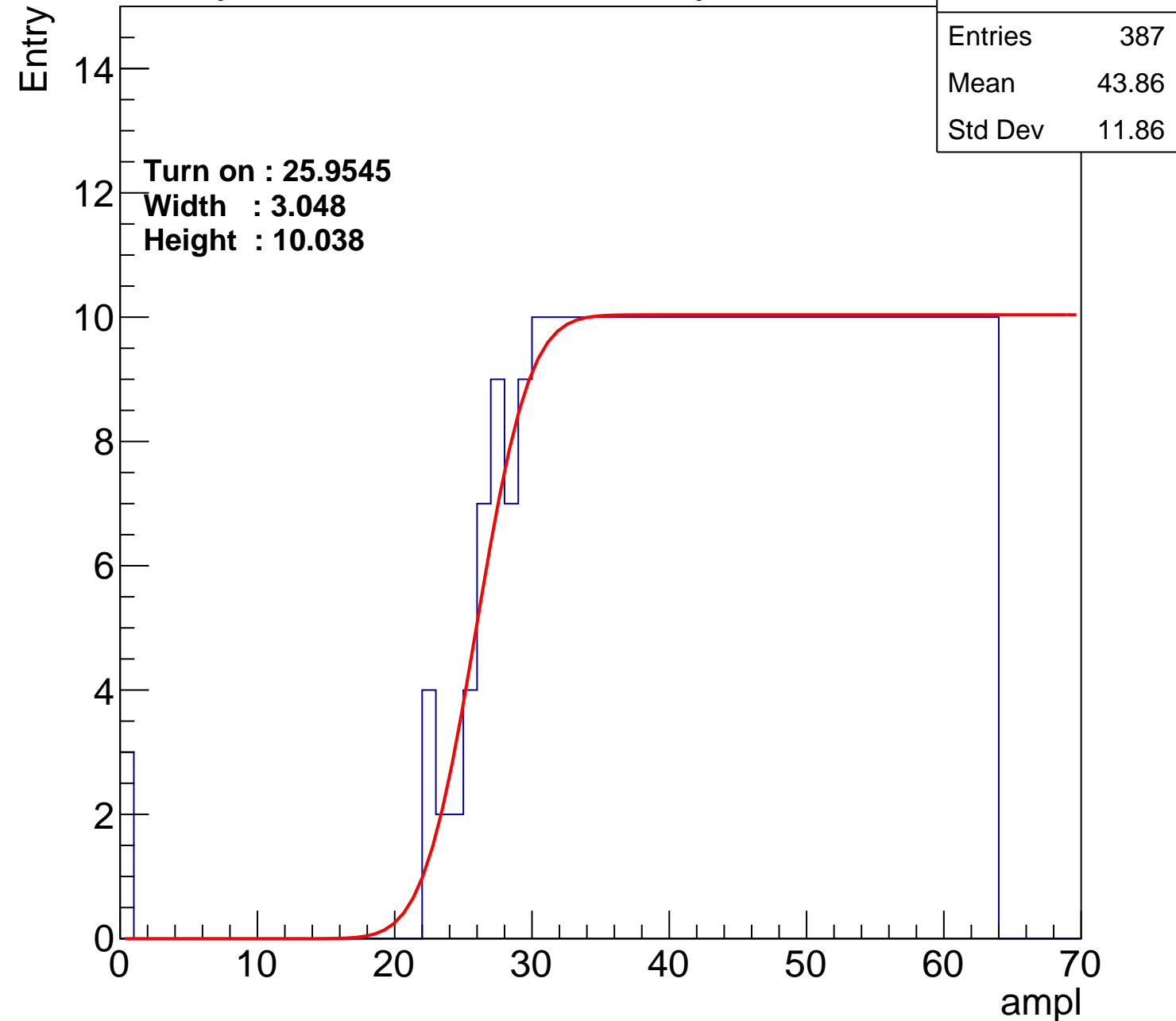
Width : 3.048

Height : 10.038

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch115

calib_packv5_042523_0143.root, FC#4, port A2

Entries	373
Mean	44.51
Std Dev	11.56

Turn on : 26.9593

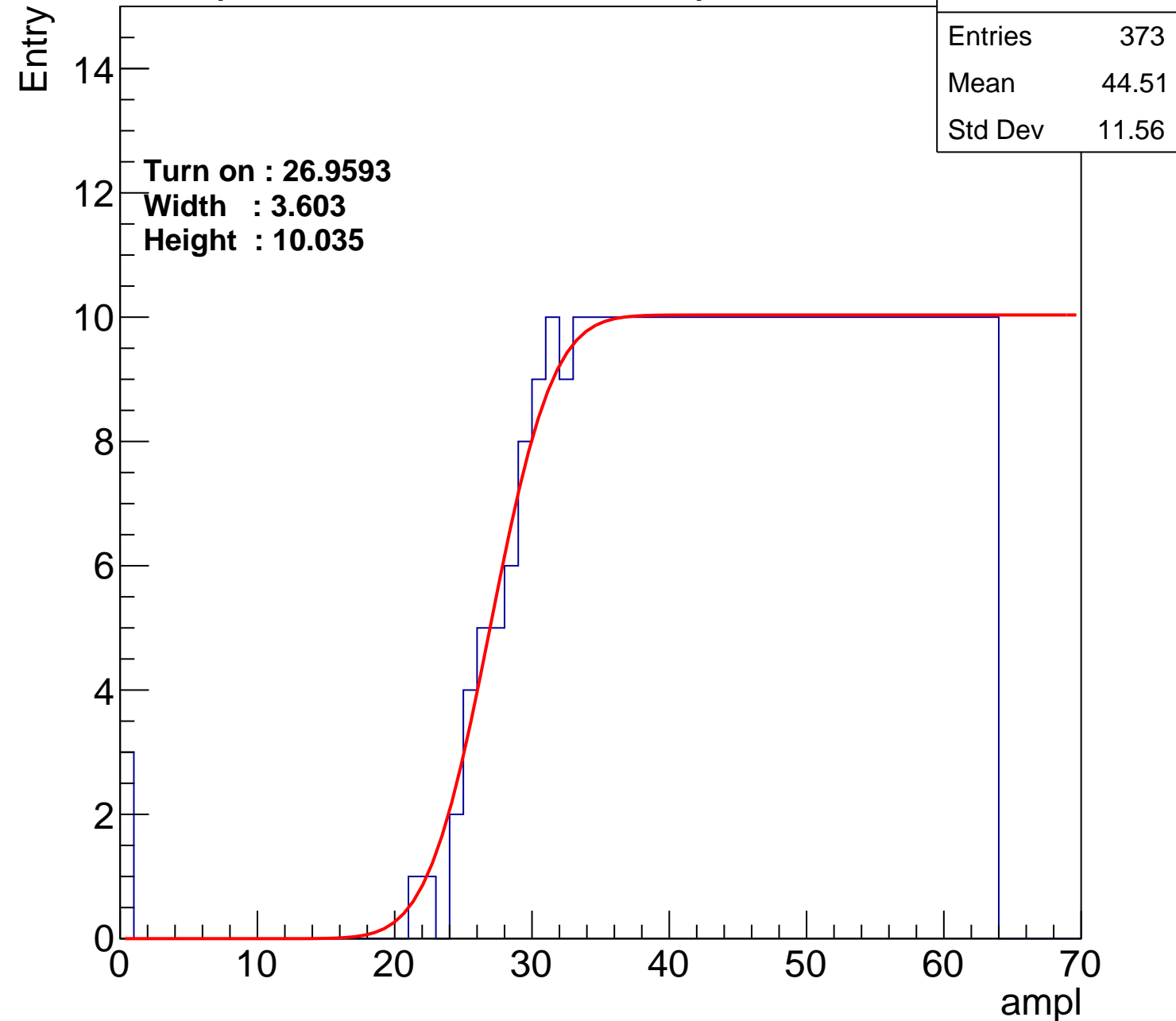
Width : 3.603

Height : 10.035

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch116

calib_packv5_042523_0143.root, FC#4, port A2

Entries	382
Mean	44.03
Std Dev	11.92

Turn on : 26.2936

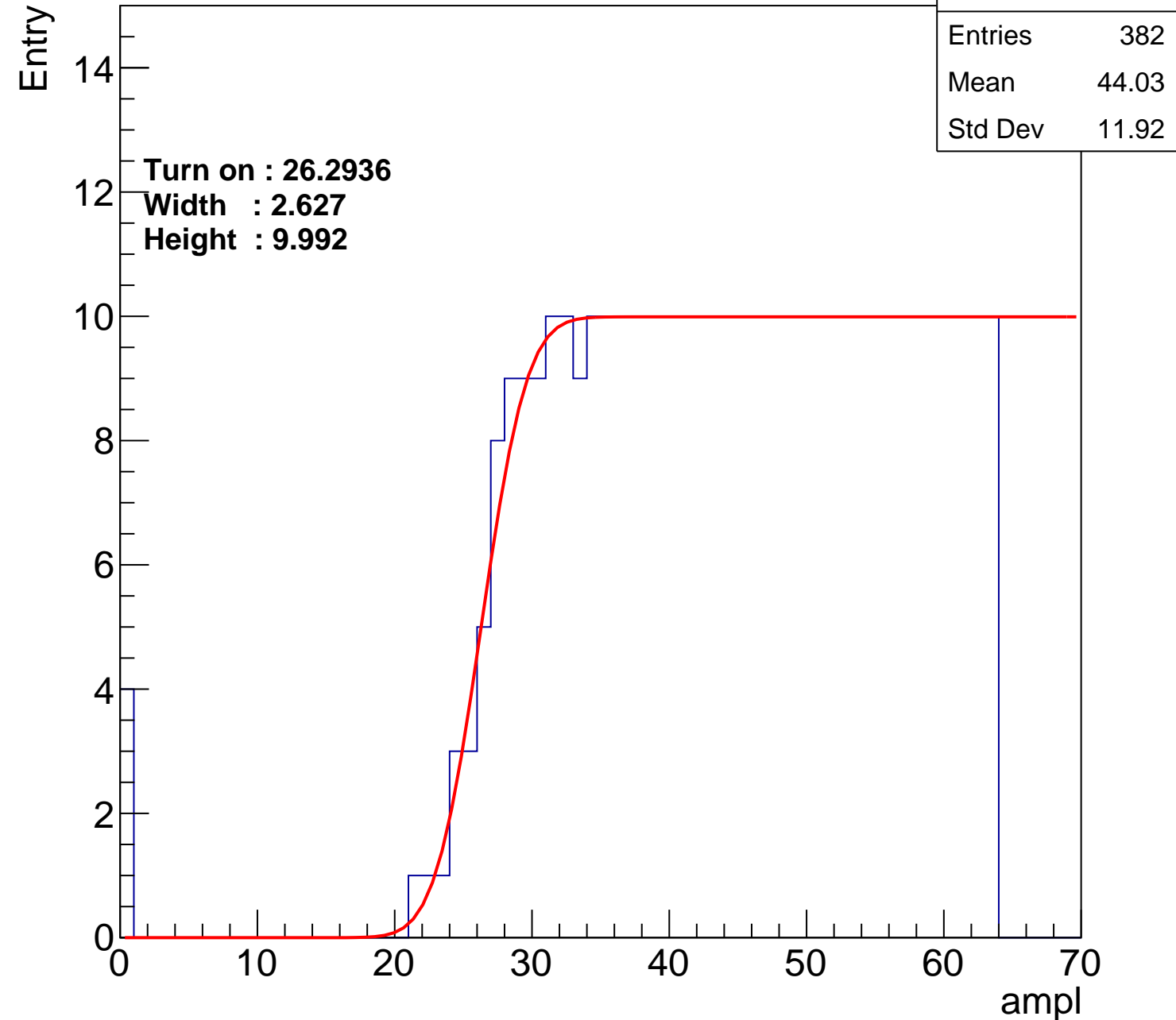
Width : 2.627

Height : 9.992

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch117

calib_packv5_042523_0143.root, FC#4, port A2

Entries	371
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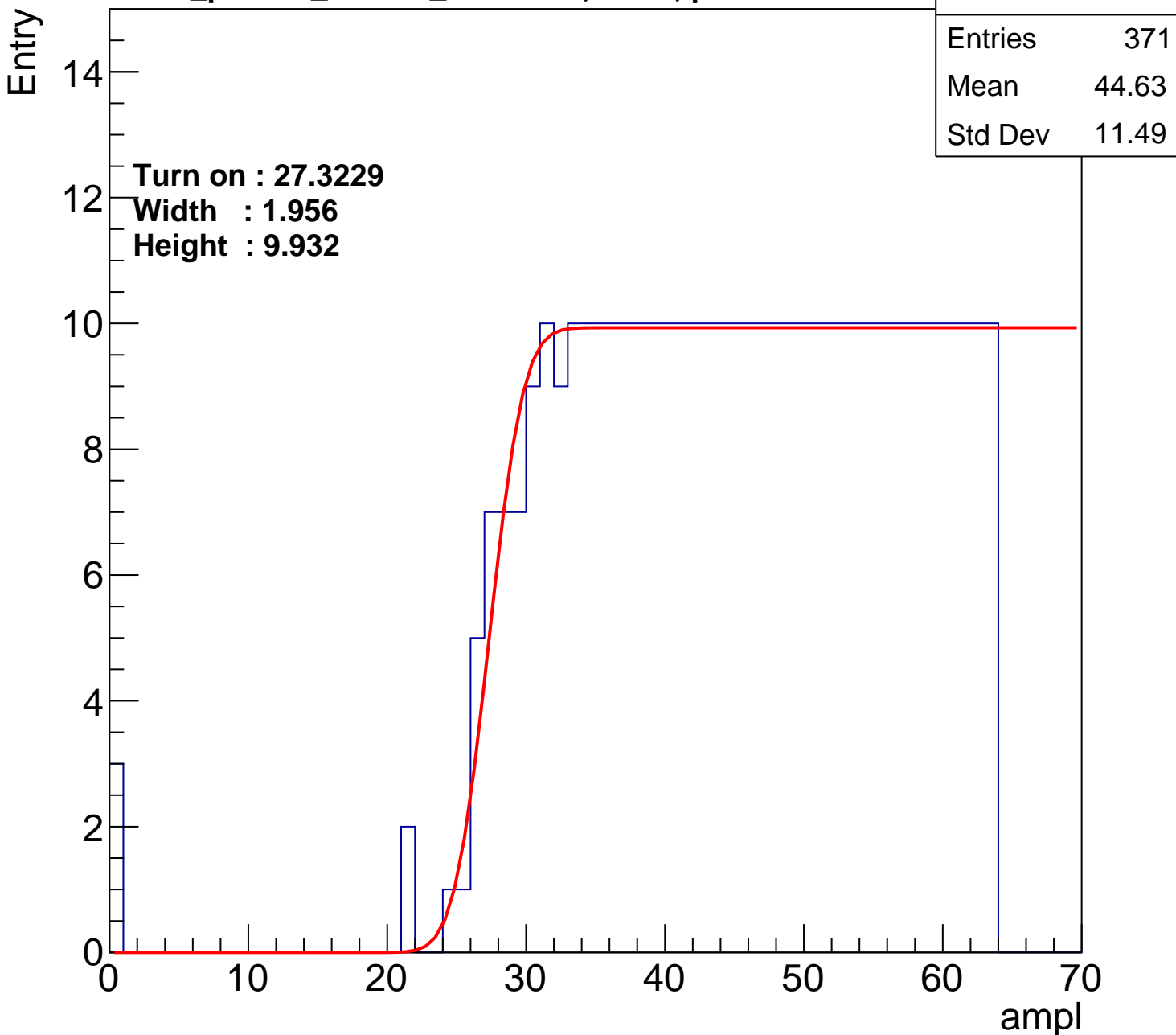
Mean	44.63
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Std Dev	11.49
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Turn on : 27.3229

Width : 1.956

Height : 9.932



B1L100S, U5-ch118

calib_packv5_042523_0143.root, FC#4, port A2

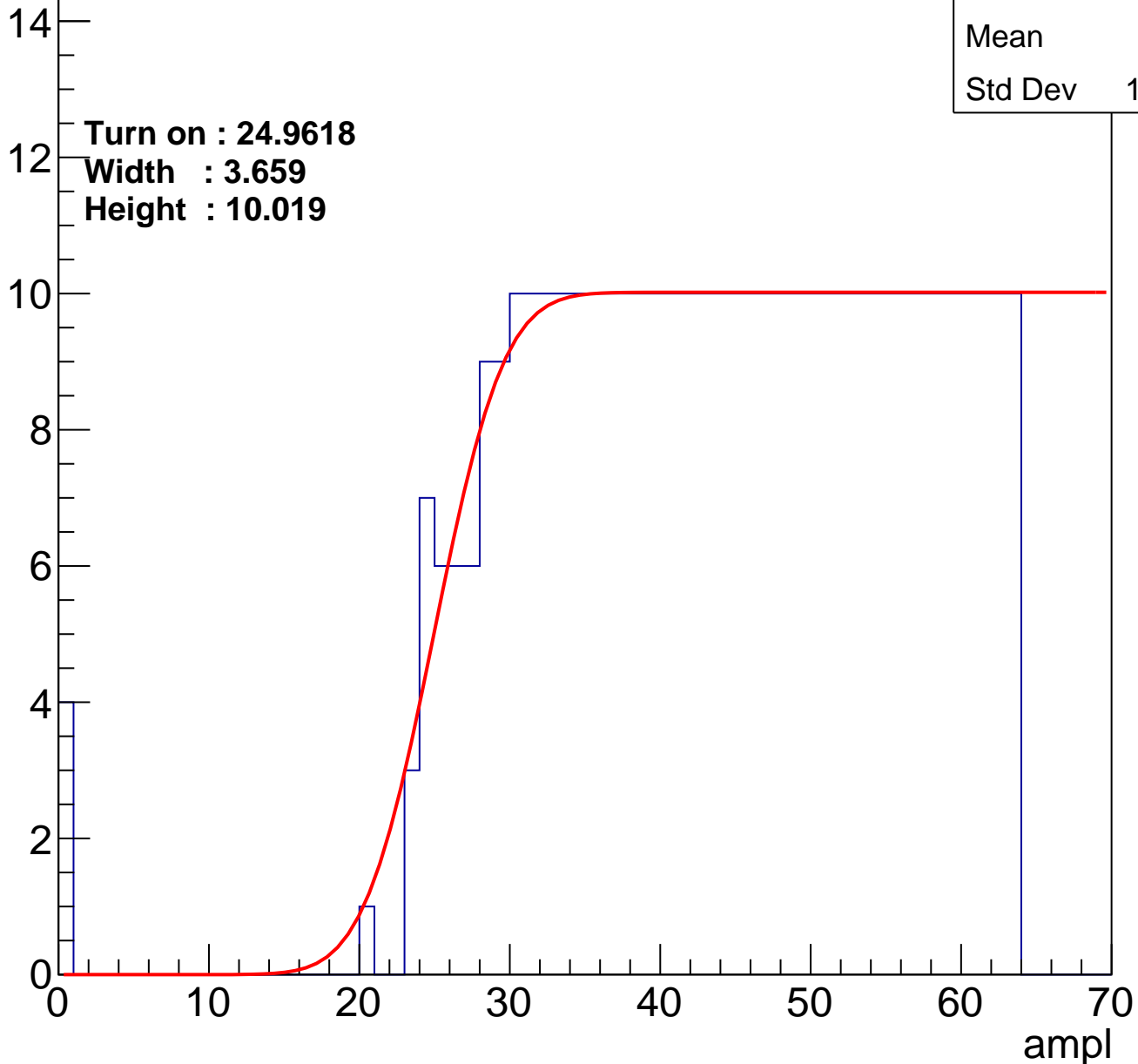
Entries	391
Mean	43.6
Std Dev	12.12

Turn on : 24.9618

Width : 3.659

Height : 10.019

Entry



B1L100S, U5-ch119

calib_packv5_042523_0143.root, FC#4, port A2

Entries	393
Mean	43.59
Std Dev	11.9

Turn on : 25.3182

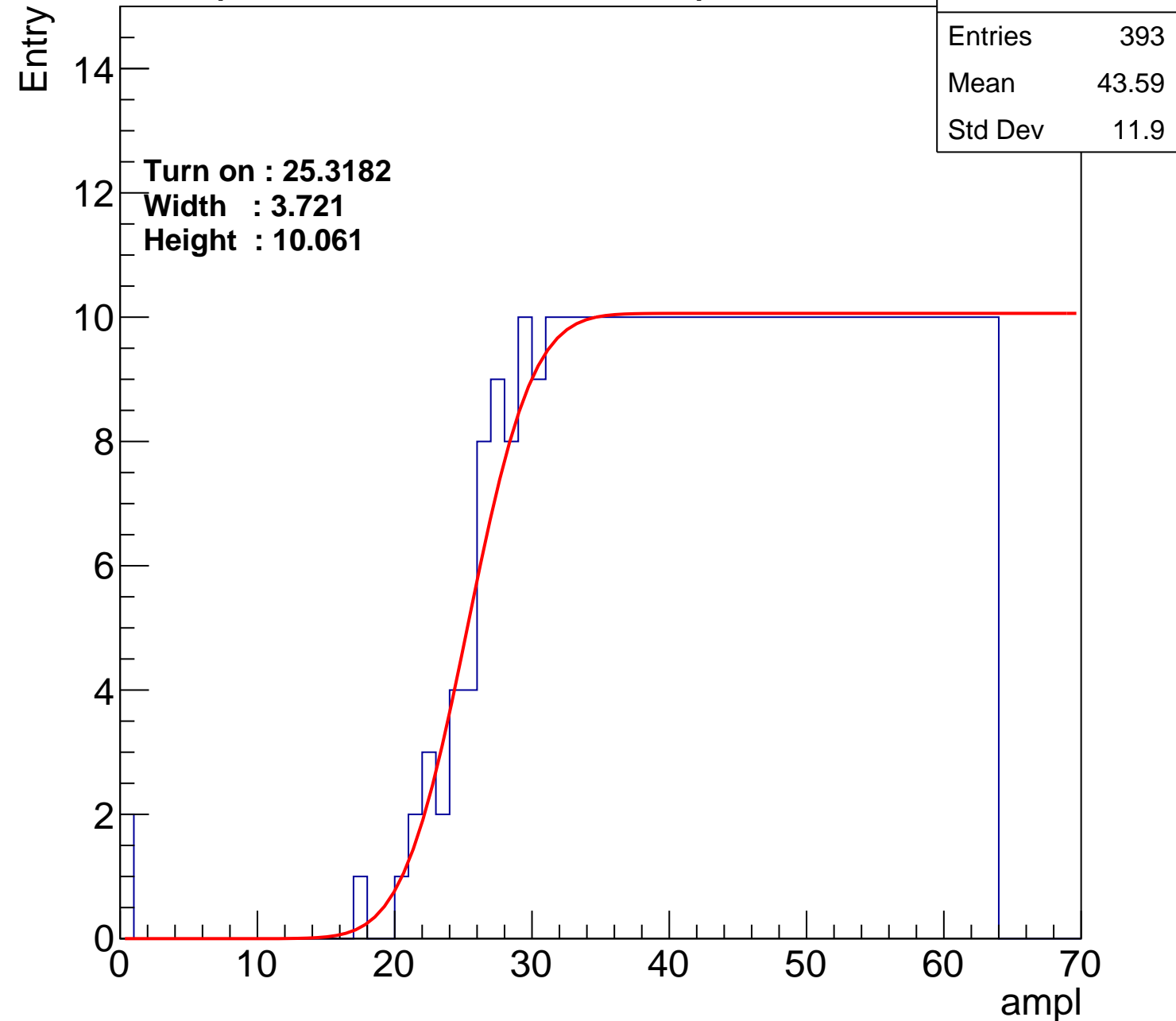
Width : 3.721

Height : 10.061

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch120

calib_packv5_042523_0143.root, FC#4, port A2

Entries	365
Mean	45.07
Std Dev	10.93

Turn on : 27.8139

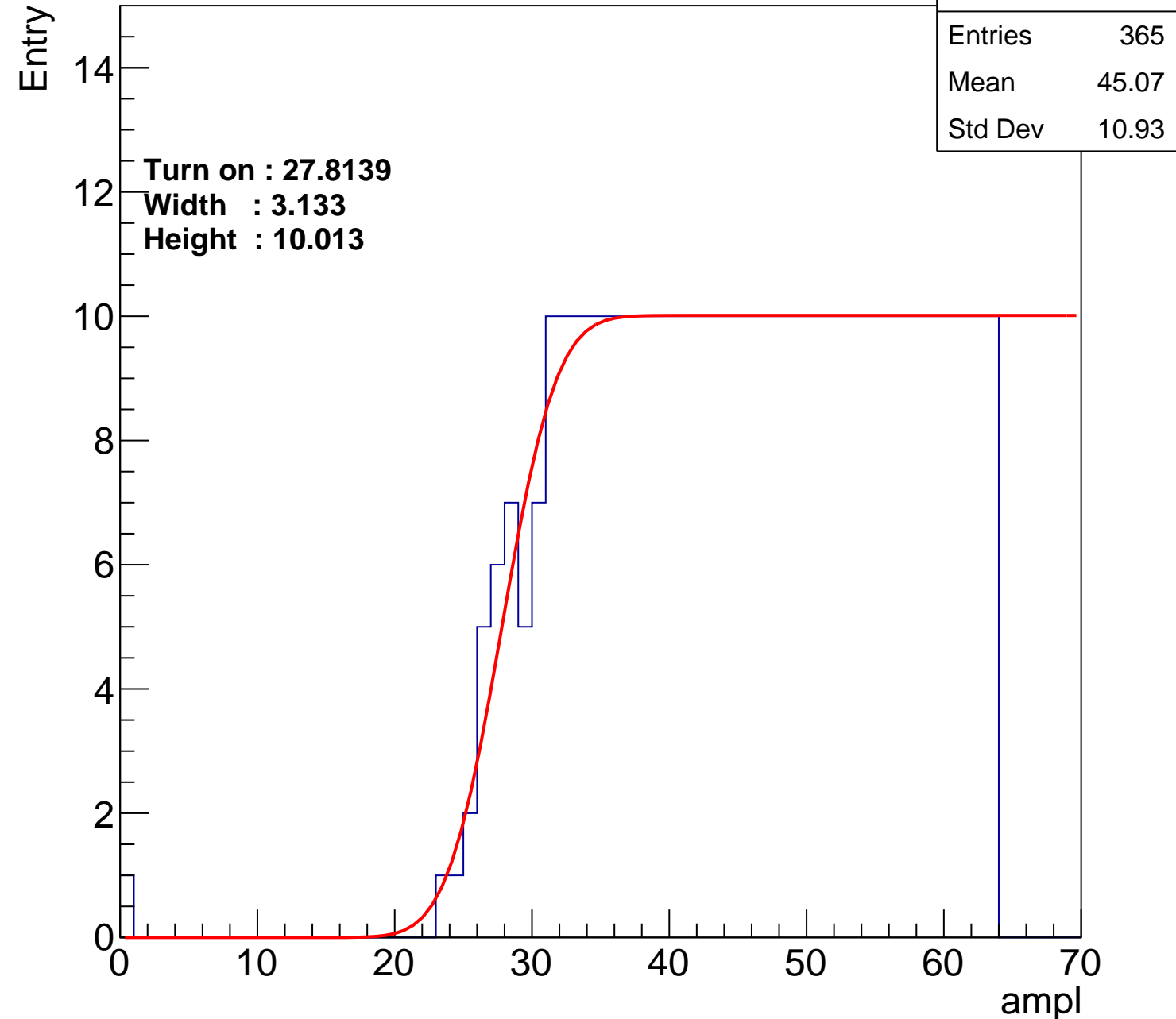
Width : 3.133

Height : 10.013

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch121

calib_packv5_042523_0143.root, FC#4, port A2

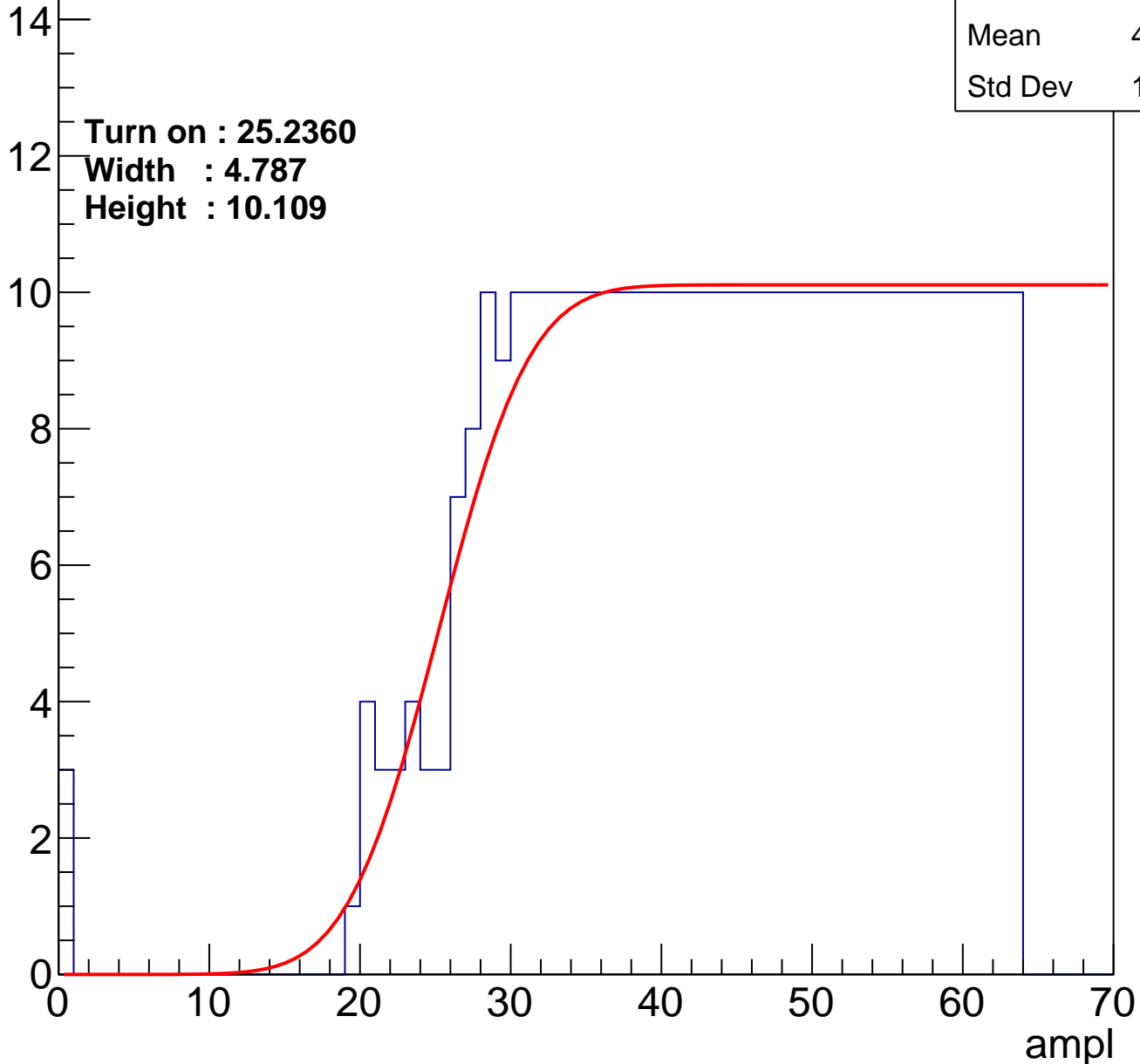
Entries	398
Mean	43.26
Std Dev	12.24

Turn on : 25.2360

Width : 4.787

Height : 10.109

Entry



B1L100S, U5-ch122

calib_packv5_042523_0143.root, FC#4, port A2

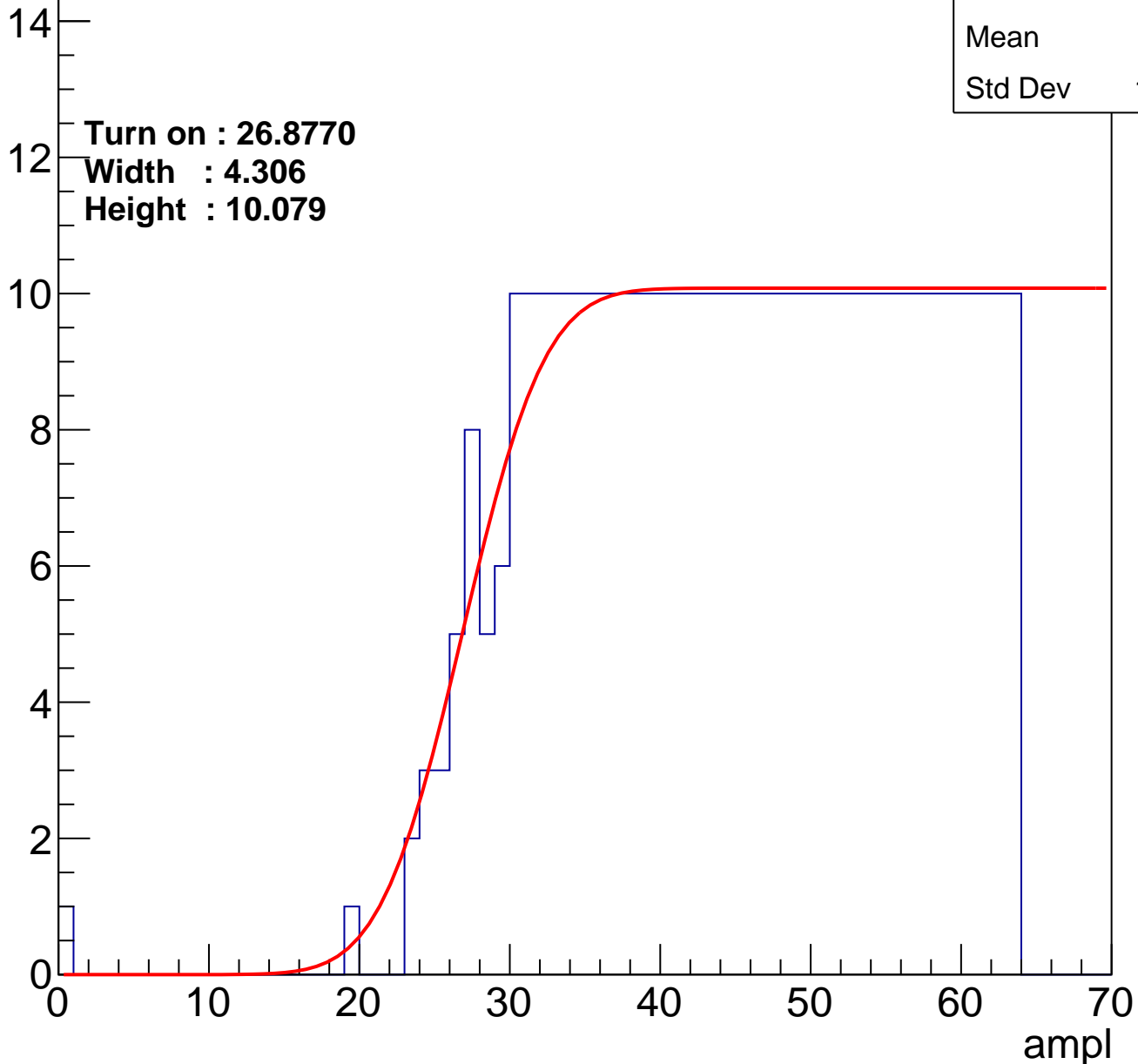
Entries	374
Mean	44.6
Std Dev	11.21

Turn on : 26.8770

Width : 4.306

Height : 10.079

Entry



calib_packv5_042523_0143.root, FC#4, port A2

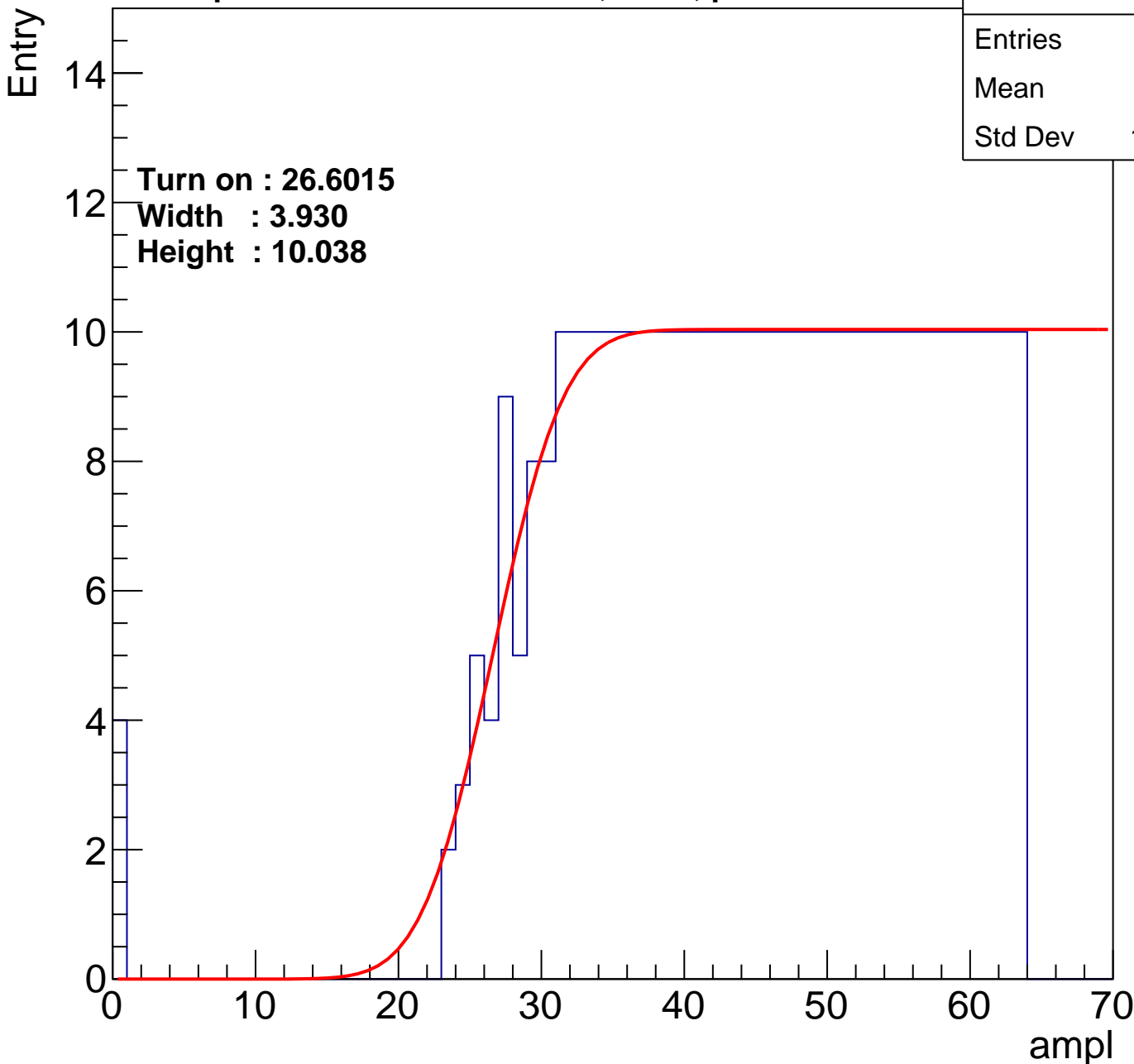
Entries	378
Mean	44.21
Std Dev	11.85

Mean	44.21
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Std Dev	11.85
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Width : 3.930

Height : 10.038



B1L100S, U5-ch124

calib_packv5_042523_0143.root, FC#4, port A2

Entries	369
Mean	44.73
Std Dev	11.43

Turn on : 27.4973

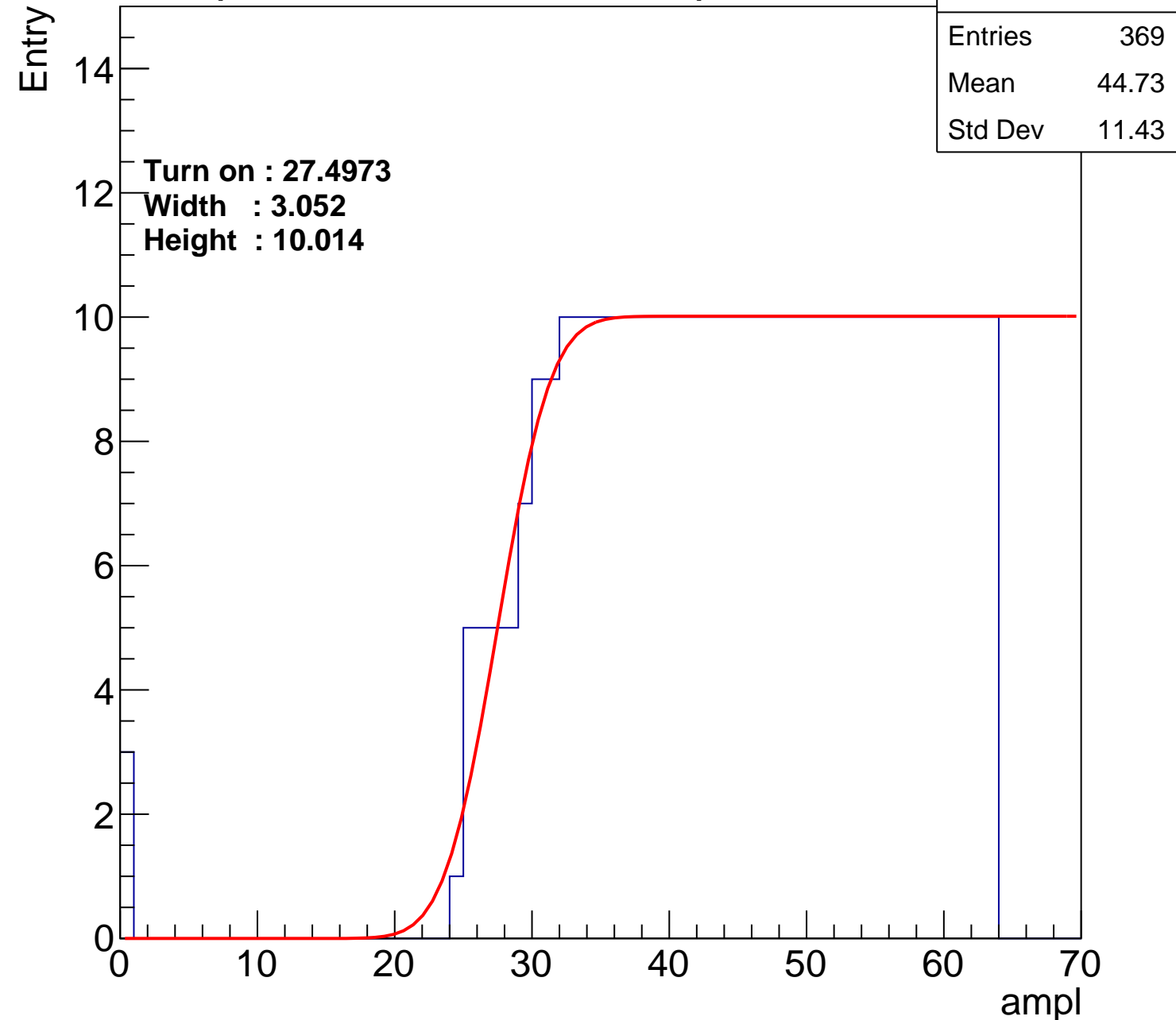
Width : 3.052

Height : 10.014

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch125

calib_packv5_042523_0143.root, FC#4, port A2

Entries	408
Mean	42.85
Std Dev	12.35

Turn on : 23.8419

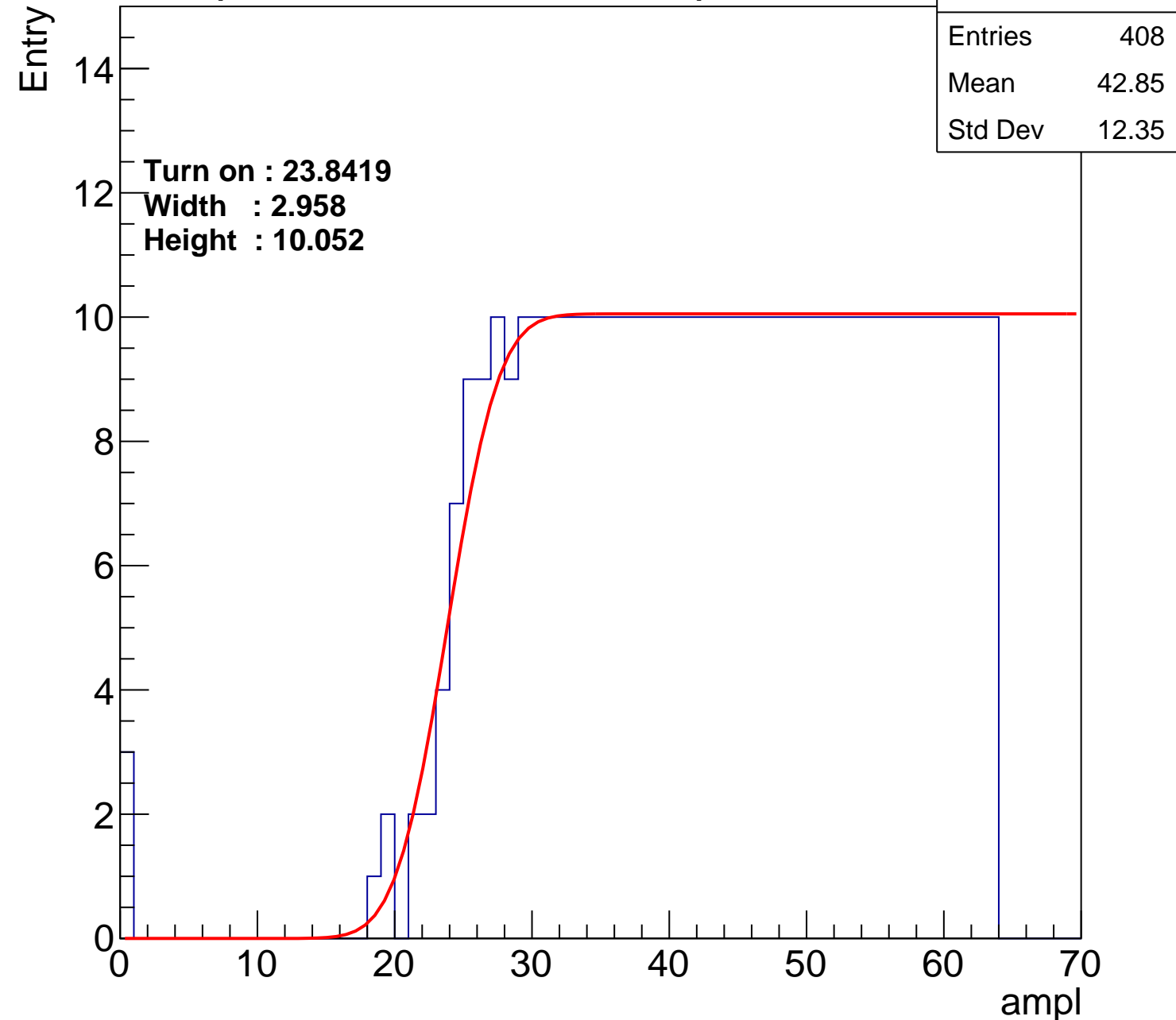
Width : 2.958

Height : 10.052

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch126

calib_packv5_042523_0143.root, FC#4, port A2

Entries	388
Mean	43.77
Std Dev	11.94

Turn on : 25.4373

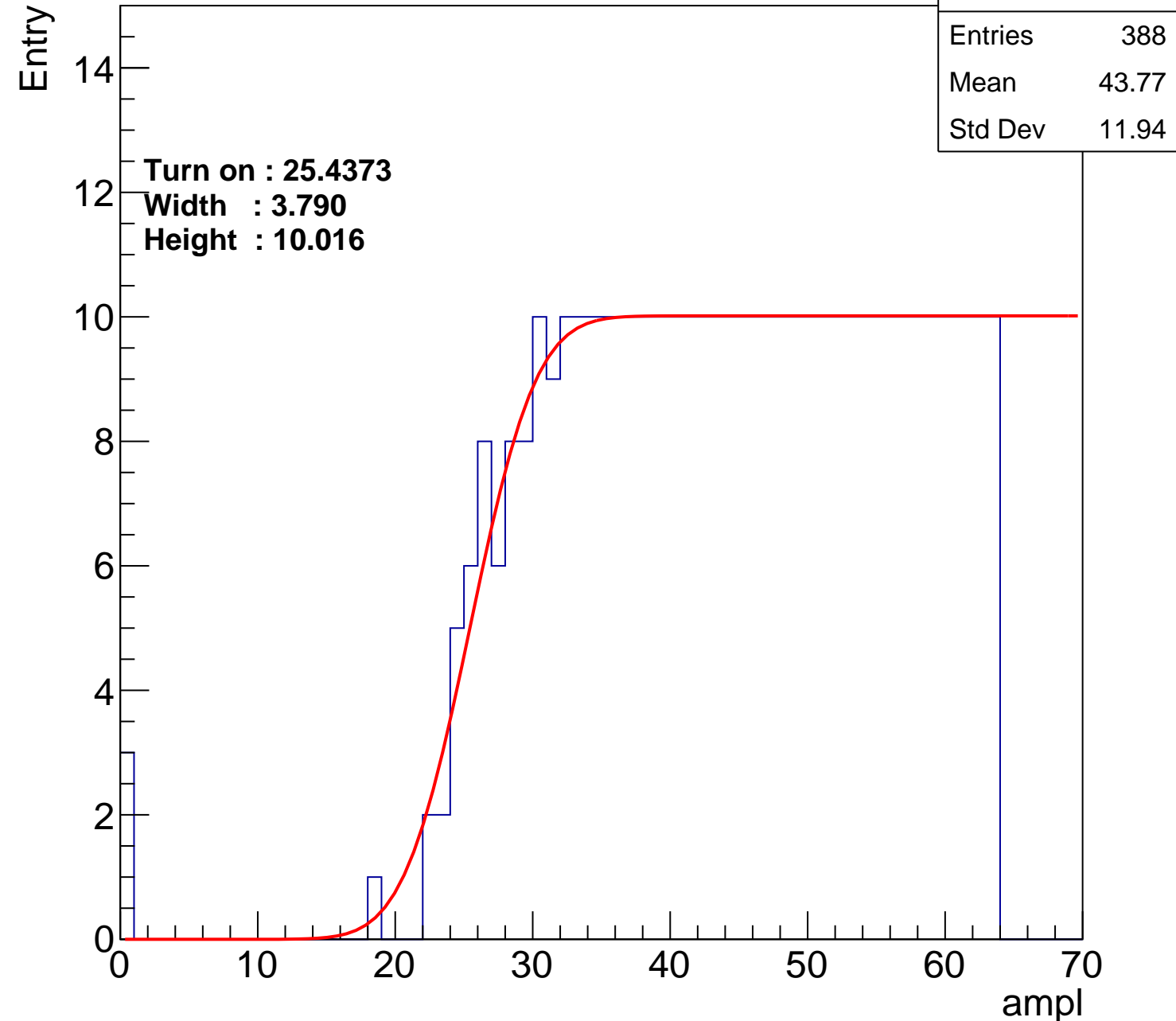
Width : 3.790

Height : 10.016

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch127

calib_packv5_042523_0143.root, FC#4, port A2

Entries	365
Mean	45.01
Std Dev	11.13

Turn on : 28.1186

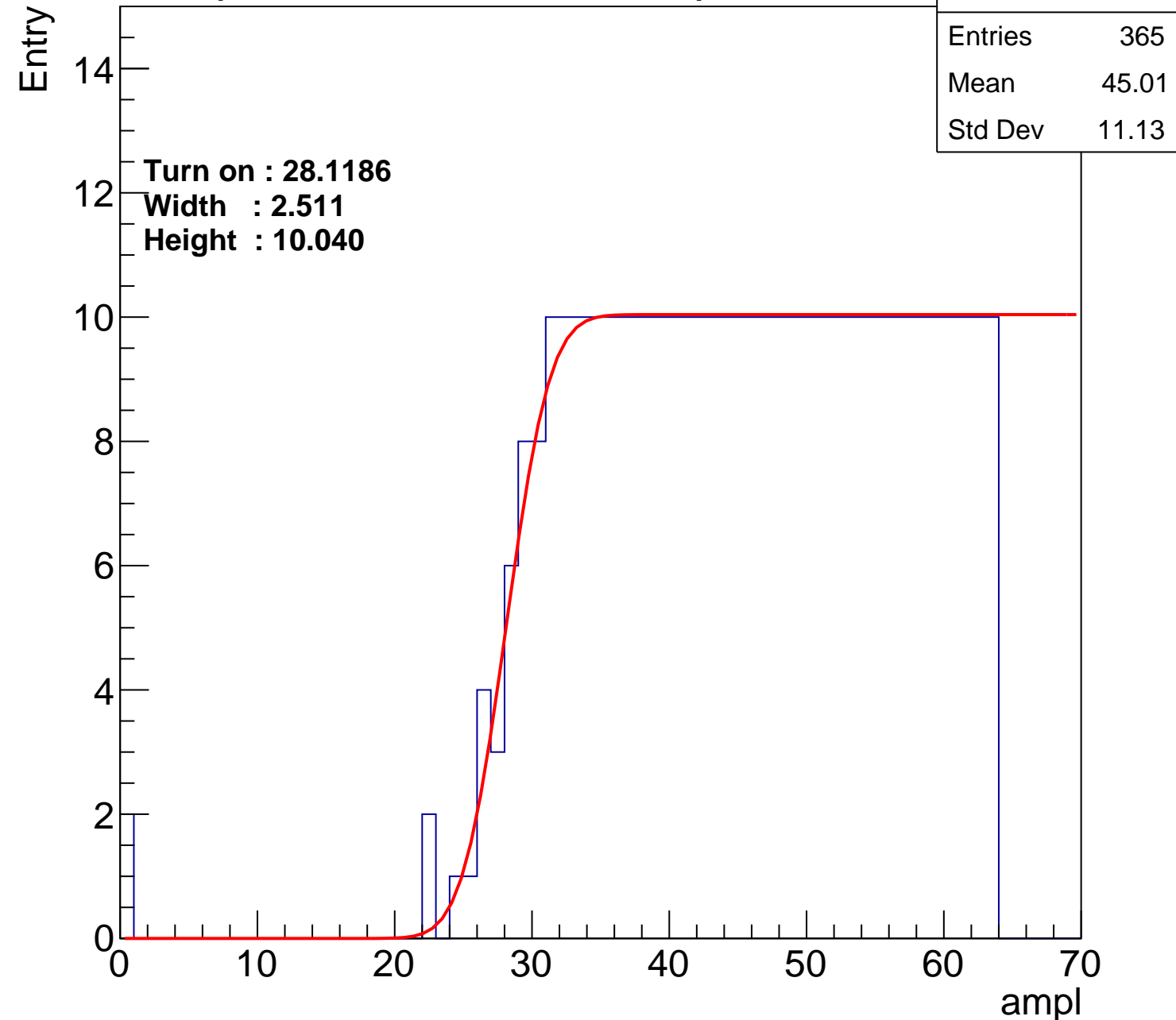
Width : 2.511

Height : 10.040

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U5-ch127

calib_packv5_042523_0143.root, FC#4, port A2

Entries	365
Mean	45.01
Std Dev	11.13

Turn on : 28.1186

Width : 2.511

Height : 10.040

Entry

14
12
10
8
6
4
2
0

ampl

