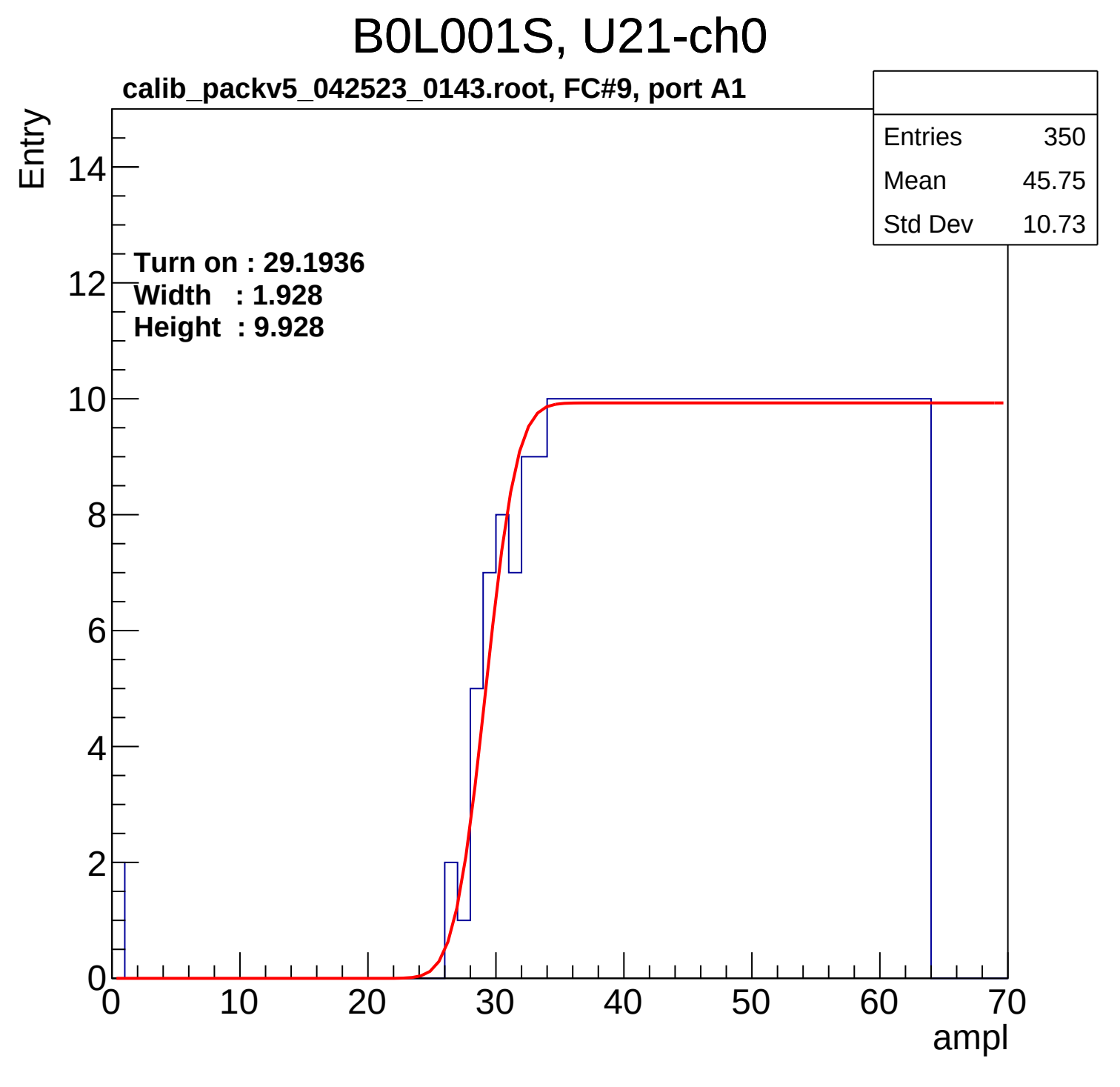
B0L001S, U21-ch0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 350
Mean 45.75
Std Dev 10.73
Turn on : 29.1936
Width : 1.928
Height : 9.928
Entry
ampl
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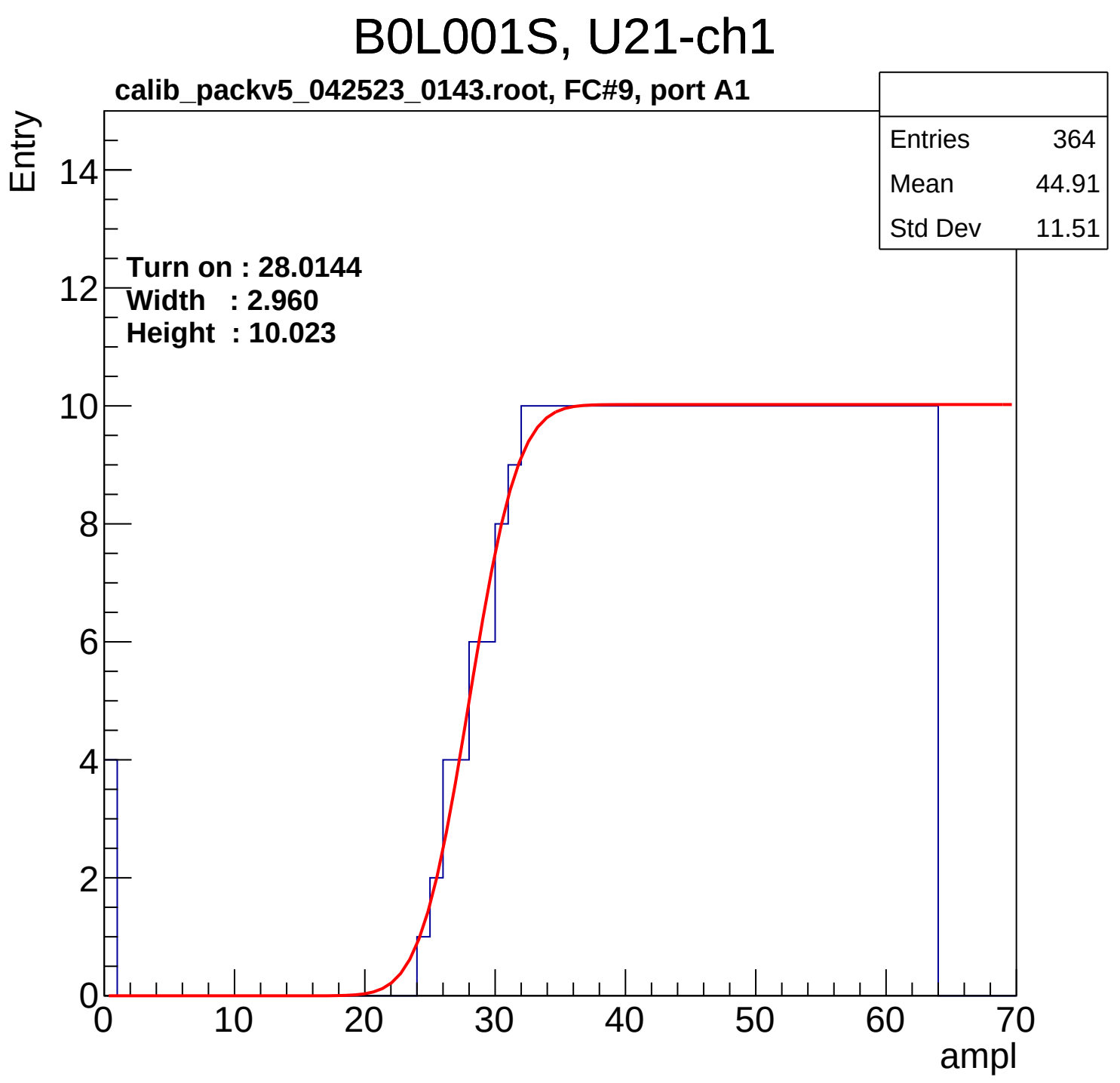
B0L001S, U21-ch1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 44.91
Std Dev 11.51
Turn on : 28.0144
Width : 2.960
Height : 10.023
Entry
ampl
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2
4
6
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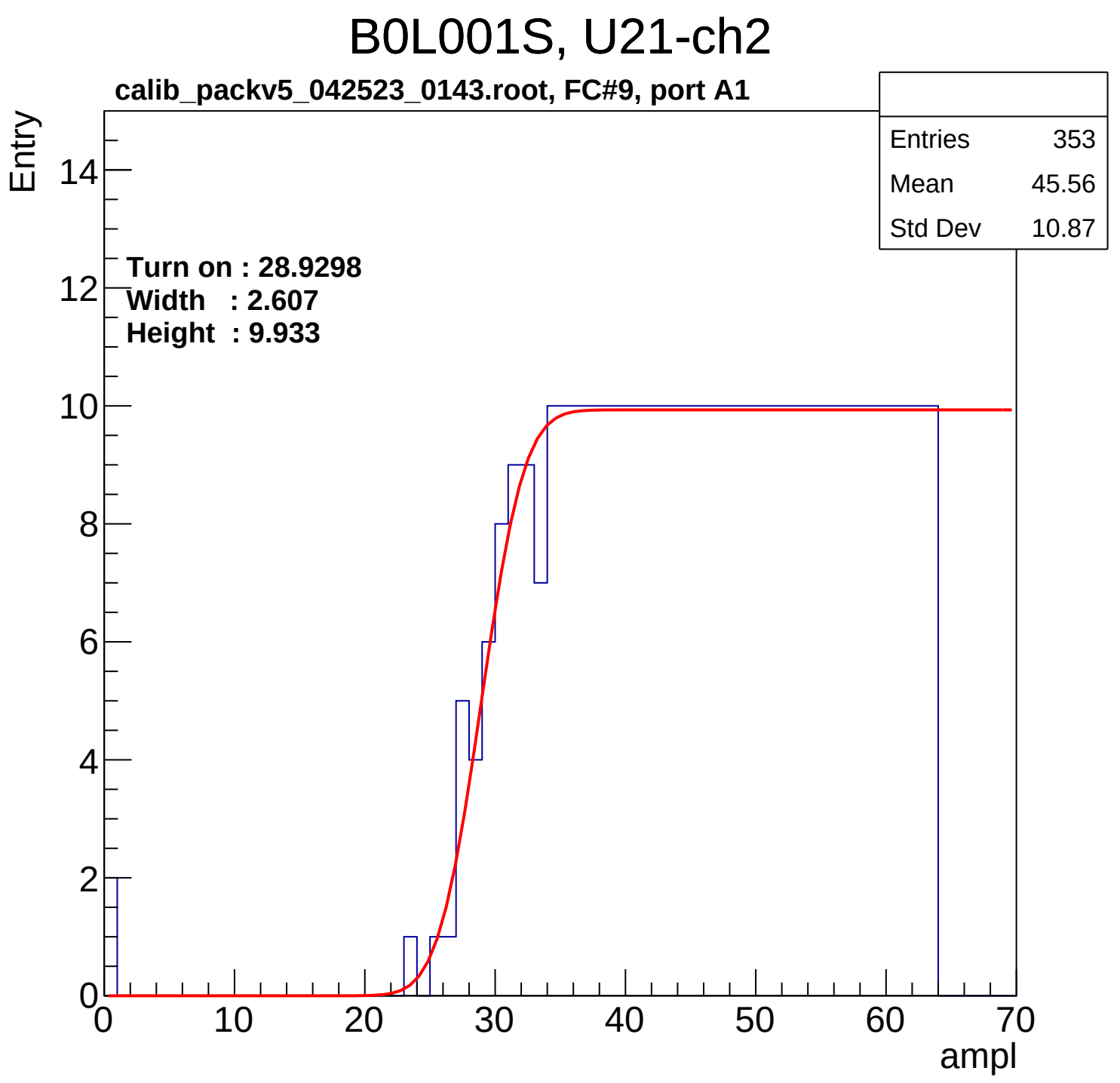
B0L001S, U21-ch2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 353
Mean 45.56
Std Dev 10.87
Turn on : 28.9298
Width : 2.607
Height : 9.933
Entry
ampl
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2
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6
8
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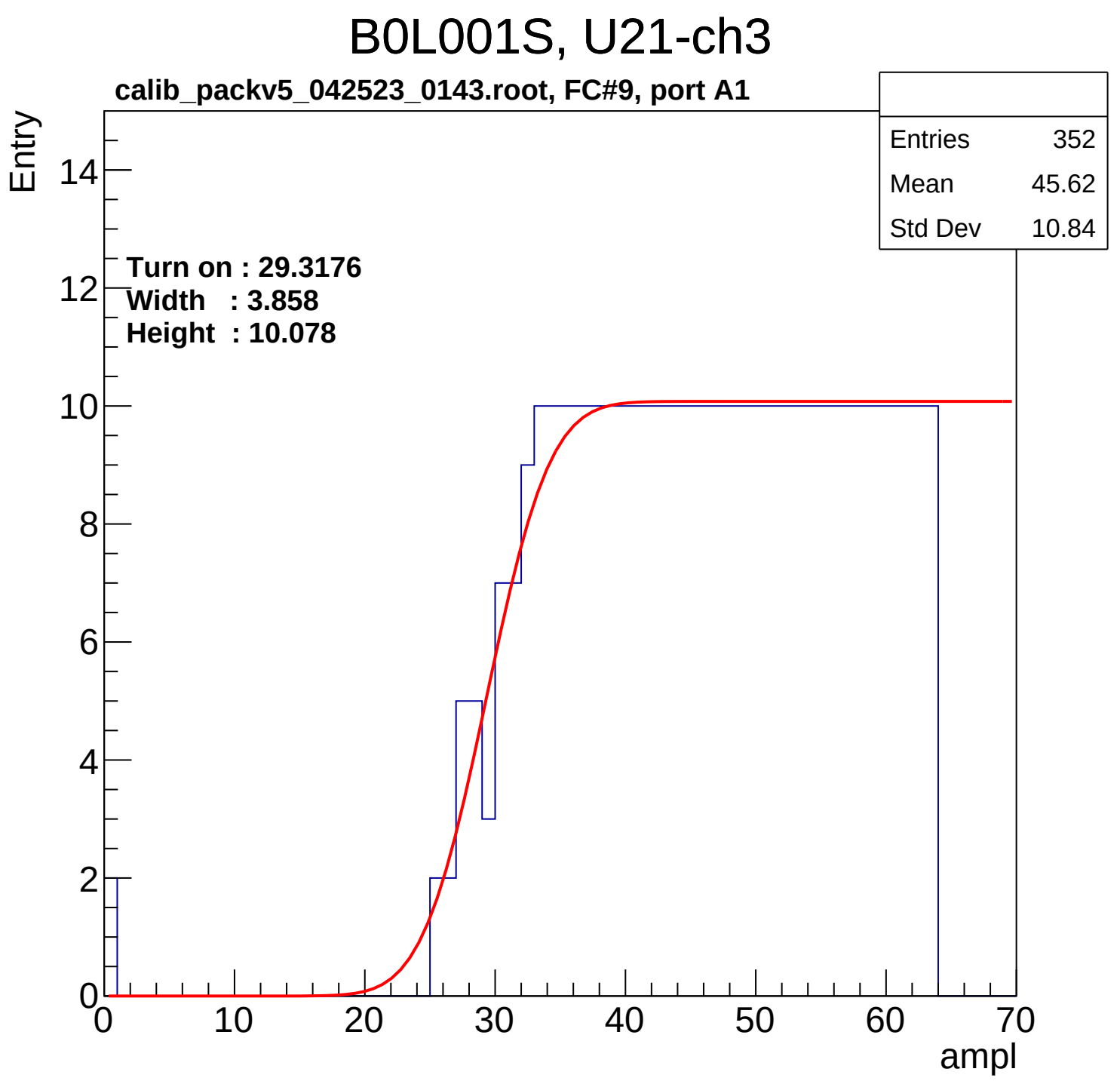
B0L001S, U21-ch3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 352
Mean 45.62
Std Dev 10.84
Turn on : 29.3176
Width : 3.858
Height : 10.078
Entry
ampl
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2
4
6
8
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0
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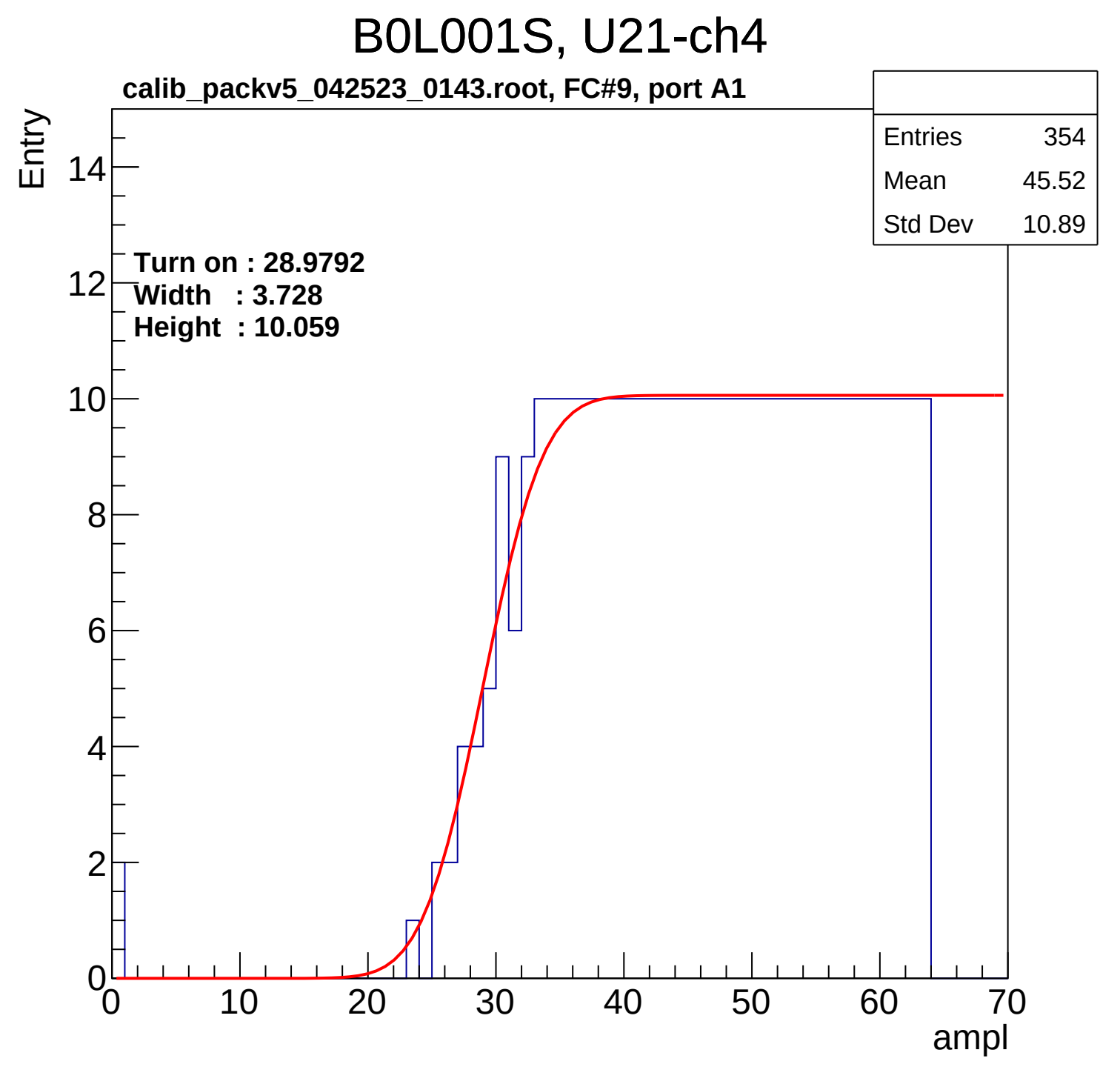
B0L001S, U21-ch4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 354
Mean 45.52
Std Dev 10.89
Turn on : 28.9792
Width : 3.728
Height : 10.059
Entry
ampl
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2
4
6
8
10
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0
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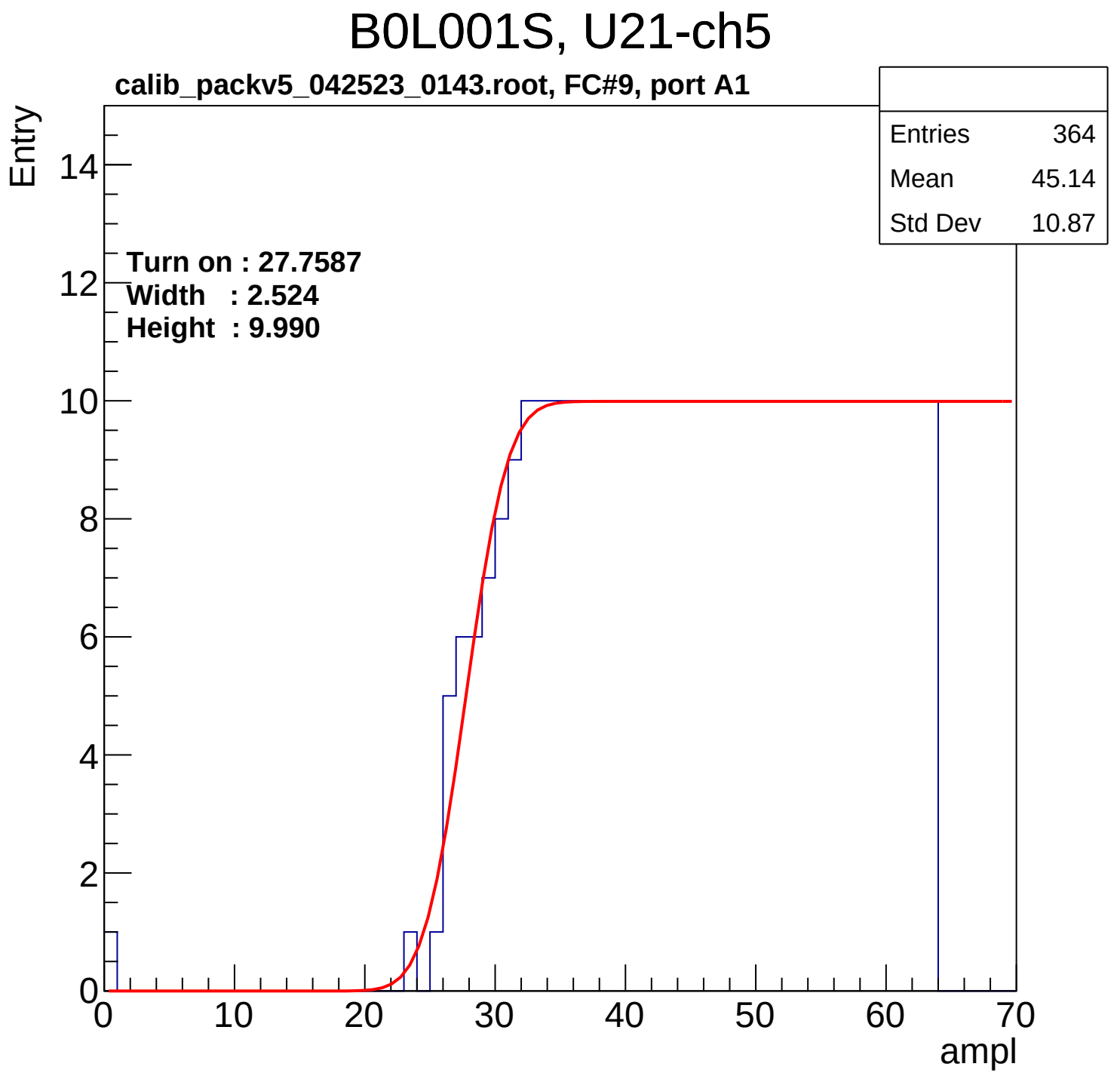
B0L001S, U21-ch5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 45.14
Std Dev 10.87
Turn on : 27.7587
Width : 2.524
Height : 9.990
Entry
ampl
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2
4
6
8
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12
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0
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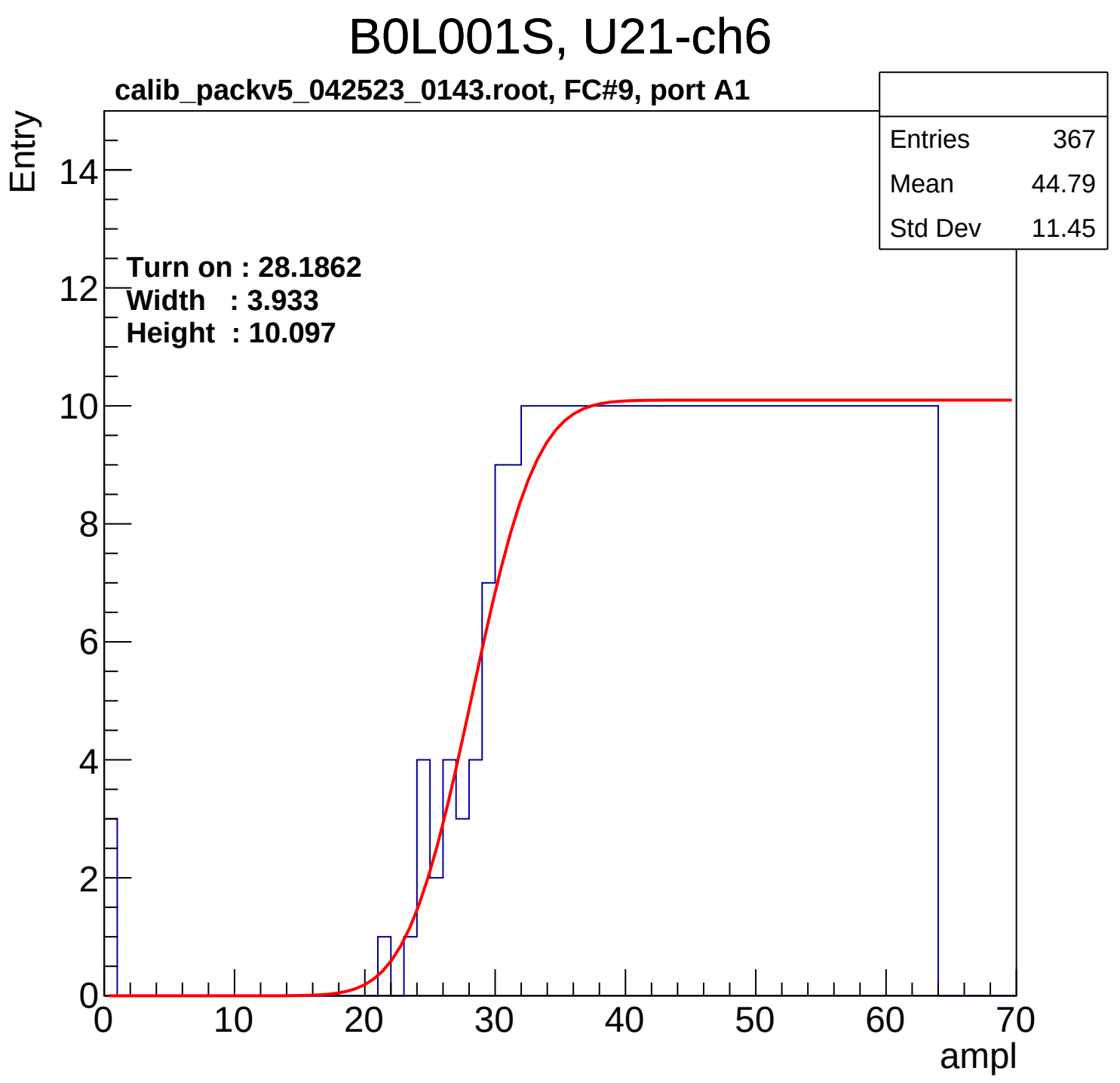
B0L001S, U21-ch6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.79
Std Dev 11.45
Turn on : 28.1862
Width : 3.933
Height : 10.097
Entry
ampl
0
2
4
6
8
10
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0
10
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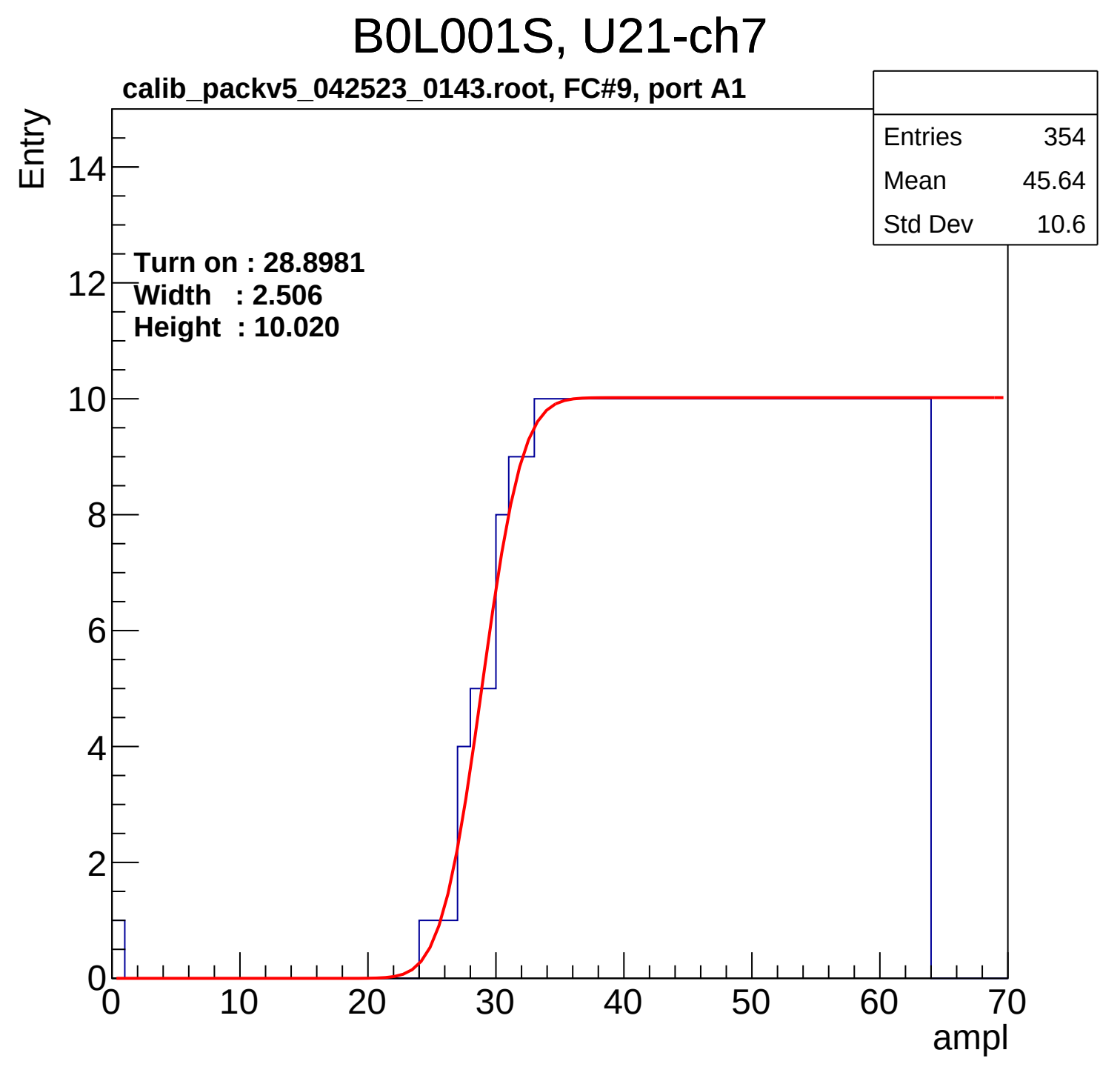
B0L001S, U21-ch7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 354
Mean 45.64
Std Dev 10.6
Turn on : 28.8981
Width : 2.506
Height : 10.020
Entry
ampl
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2
4
6
8
10
12
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0
10
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60
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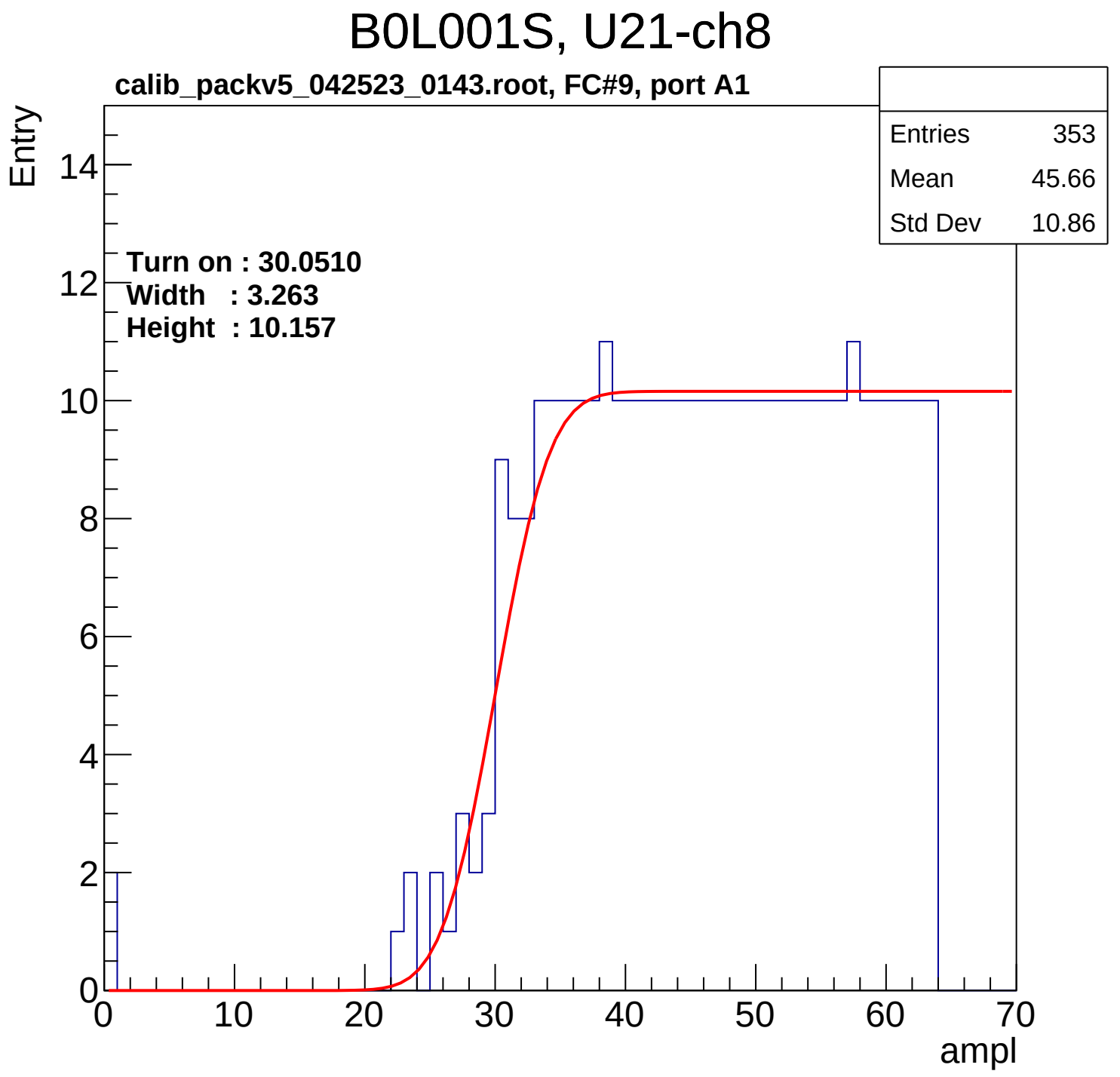
B0L001S, U21-ch8
calib_packv5_042523_0143.root, FC#9, port A1
Entries 353
Mean 45.66
Std Dev 10.86
Turn on : 30.0510
Width : 3.263
Height : 10.157
Entry
ampl
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2
4
6
8
10
12
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0
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20
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60
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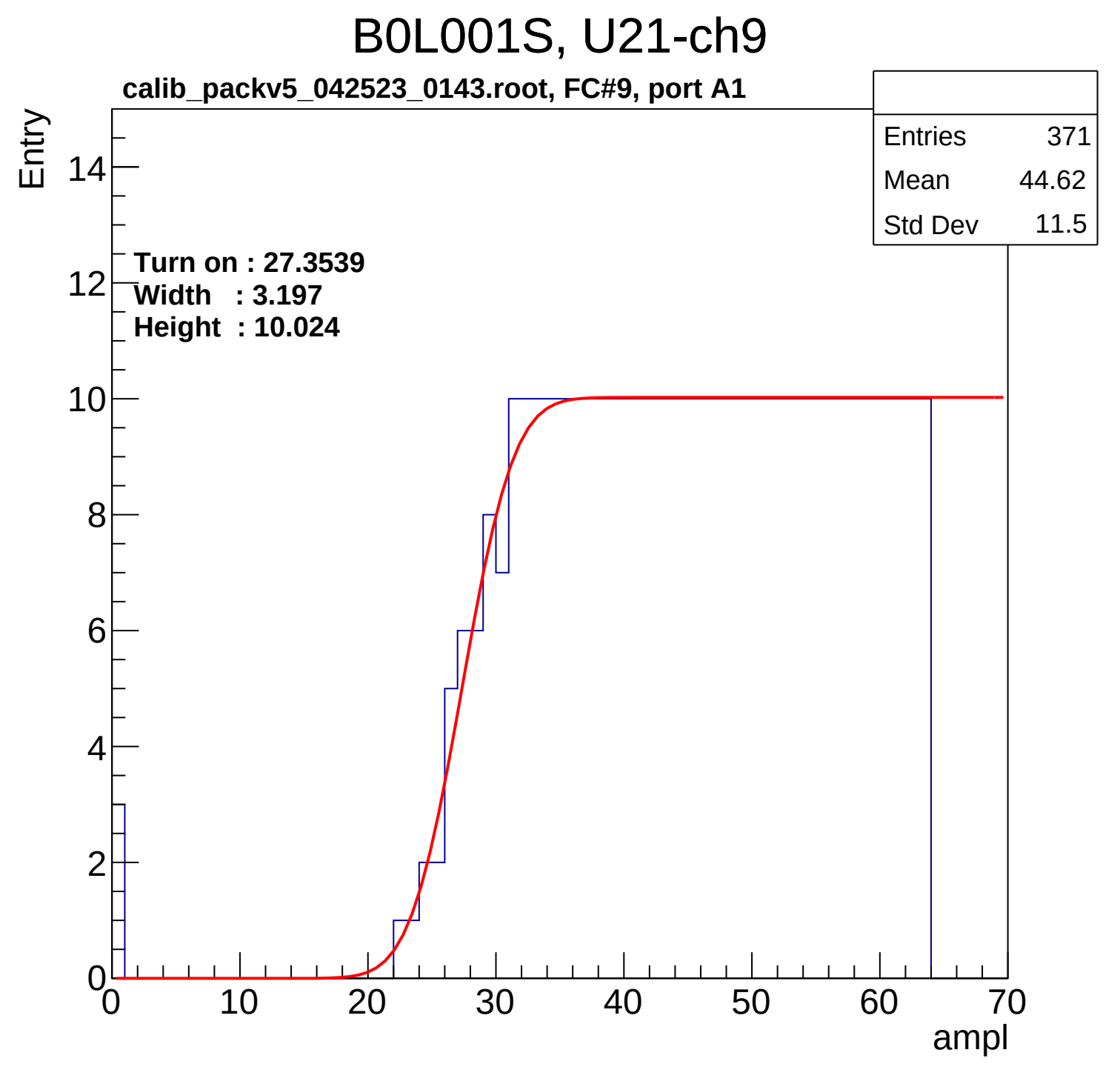
B0L001S, U21-ch9
calib_packv5_042523_0143.root, FC#9, port A1
Entries 371
Mean 44.62
Std Dev 11.5
Turn on : 27.3539
Width : 3.197
Height : 10.024
Entry
ampl
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4
6
8
10
12
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0
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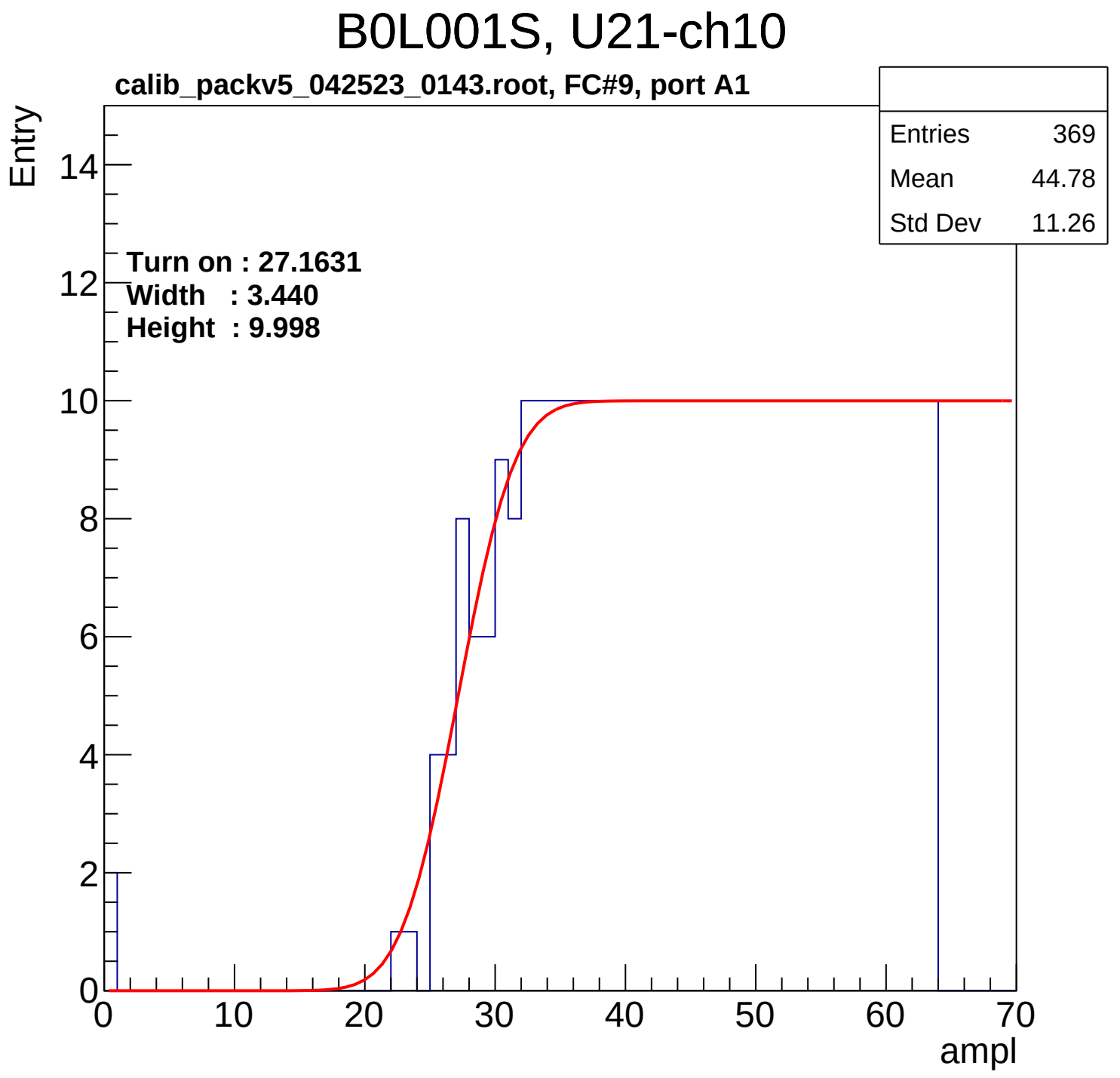
B0L001S, U21-ch10
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.78
Std Dev 11.26
Turn on : 27.1631
Width : 3.440
Height : 9.998
Entry
ampl
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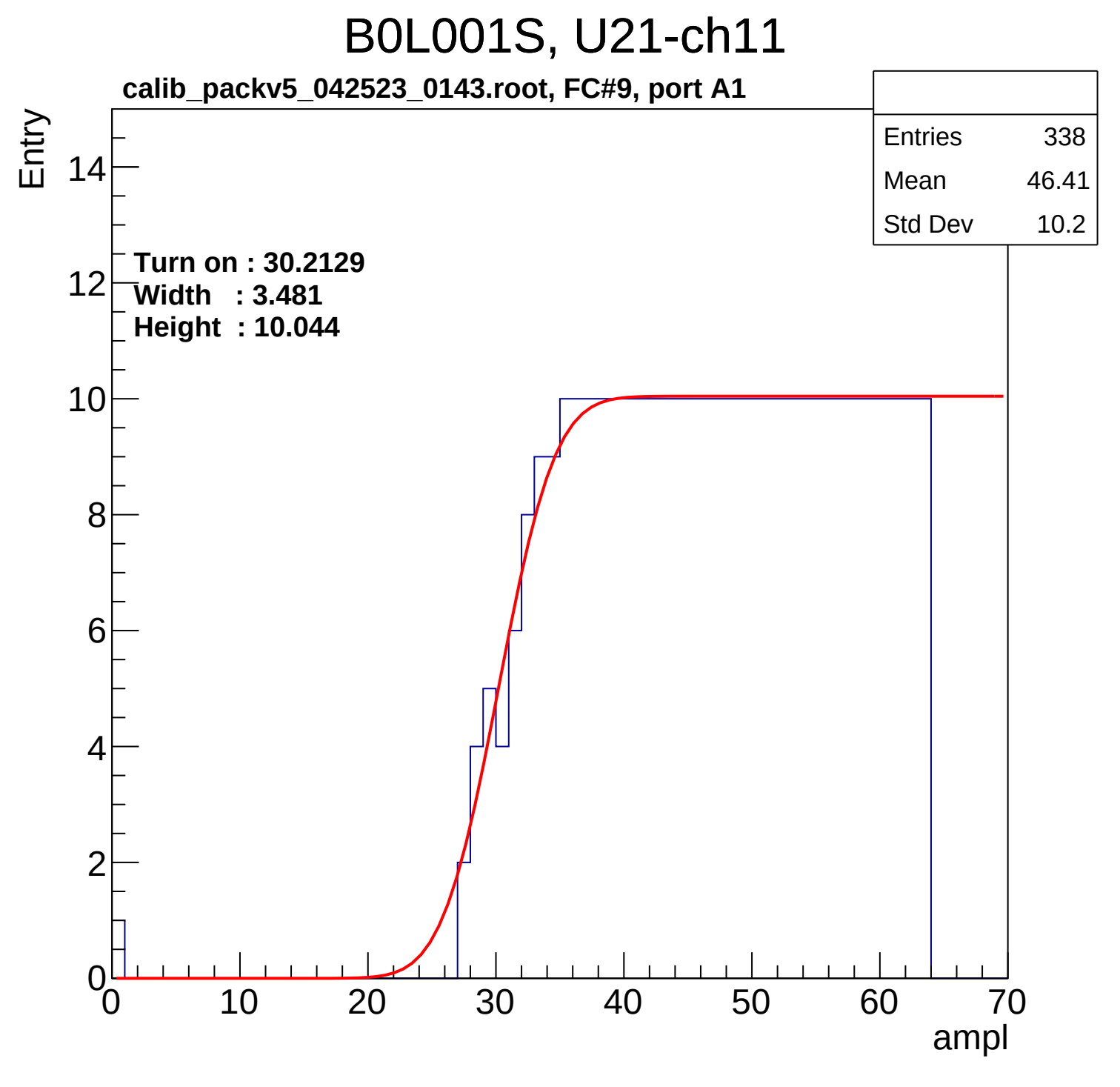
B0L001S, U21-ch11
calib_packv5_042523_0143.root, FC#9, port A1
Entries 338
Mean 46.41
Std Dev 10.2
Turn on : 30.2129
Width : 3.481
Height : 10.044
Entry
ampl
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2
4
6
8
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12
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0
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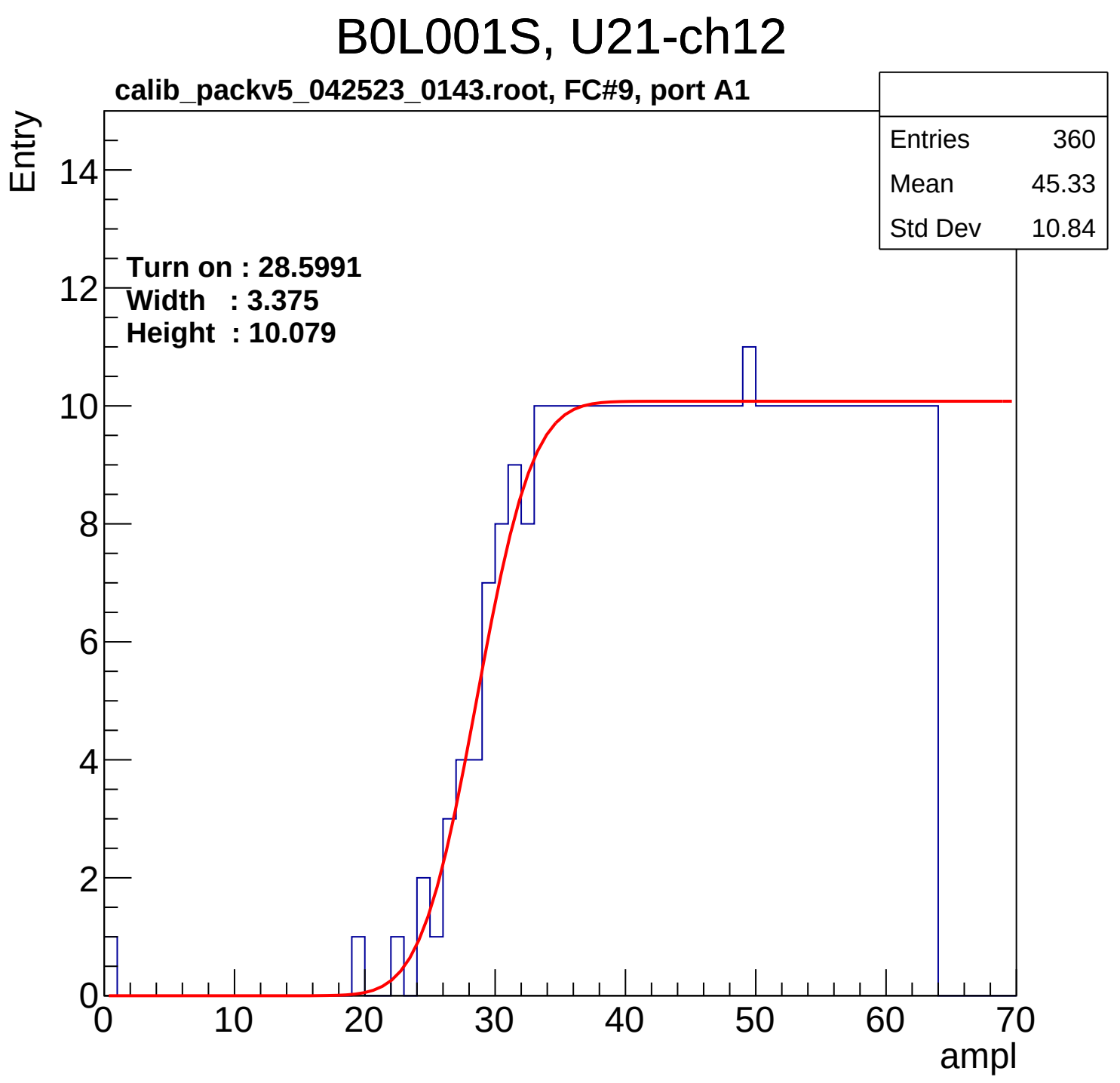
B0L001S, U21-ch12
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 45.33
Std Dev 10.84
Turn on : 28.5991
Width : 3.375
Height : 10.079
Entry
ampl
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4
6
8
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0
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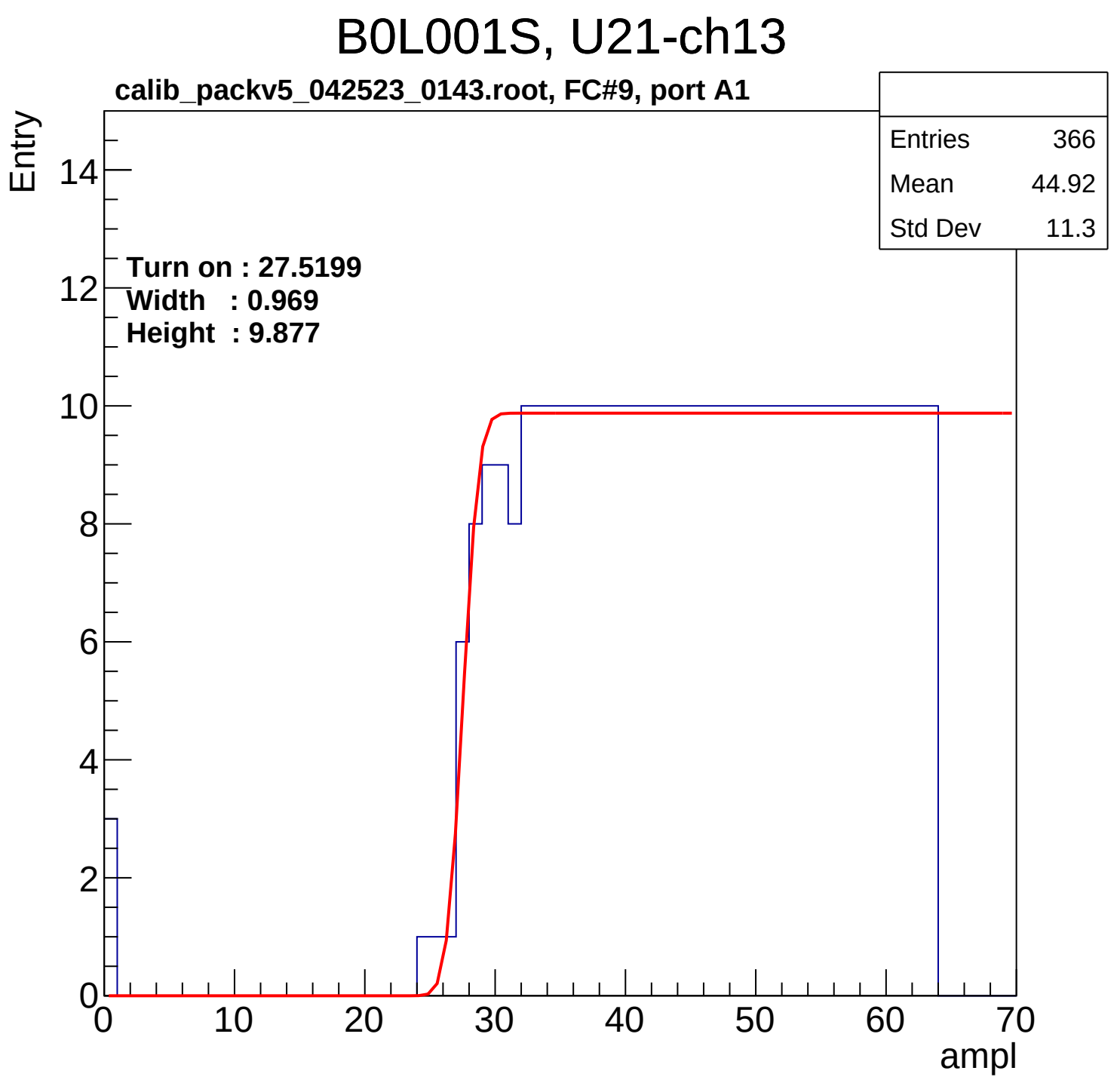
B0L001S, U21-ch13
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.92
Std Dev 11.3
Turn on : 27.5199
Width : 0.969
Height : 9.877
Entry
ampl
0
2
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6
8
10
12
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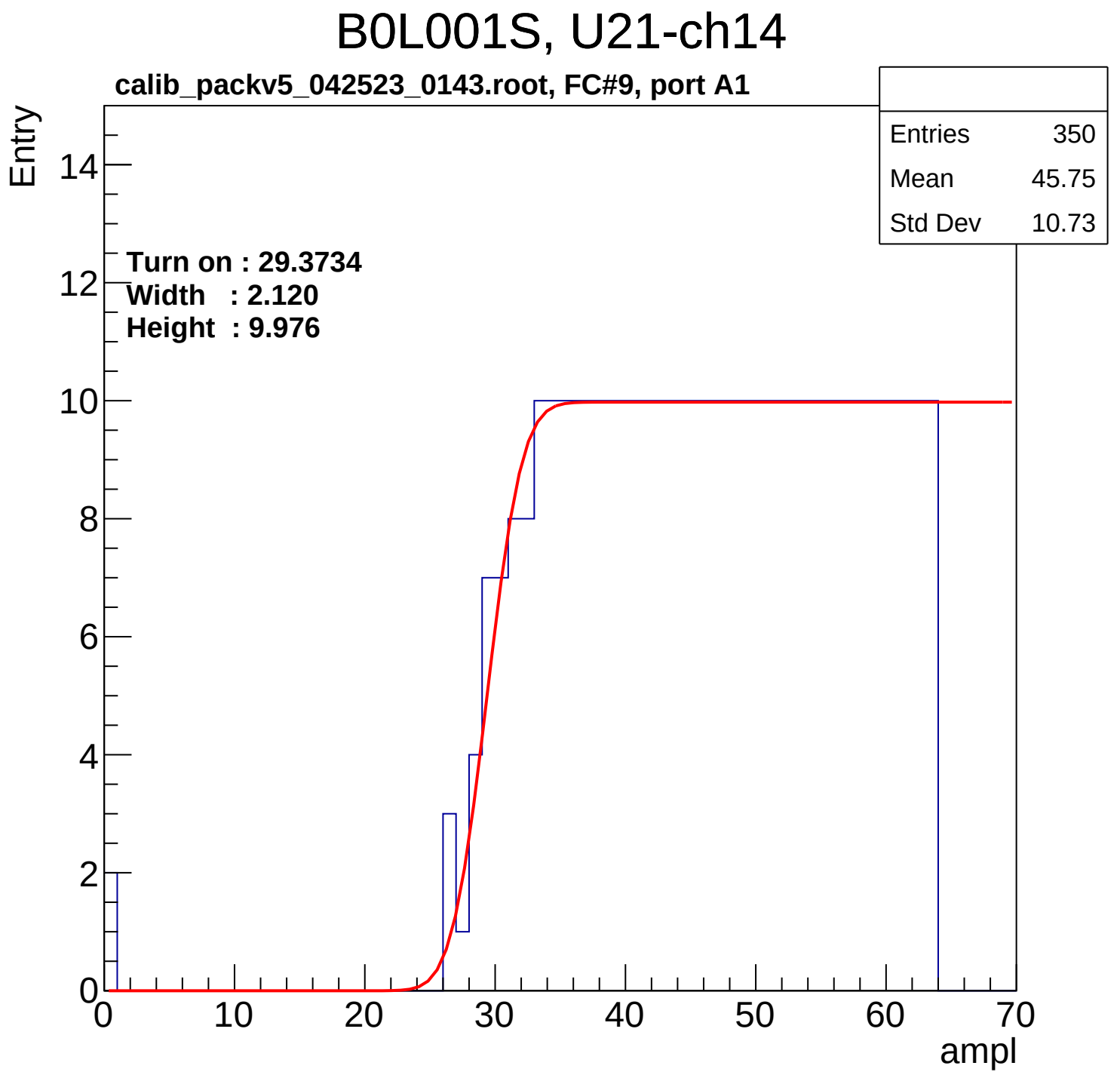
B0L001S, U21-ch14
calib_packv5_042523_0143.root, FC#9, port A1
Entries 350
Mean 45.75
Std Dev 10.73
Turn on : 29.3734
Width : 2.120
Height : 9.976
Entry
ampl
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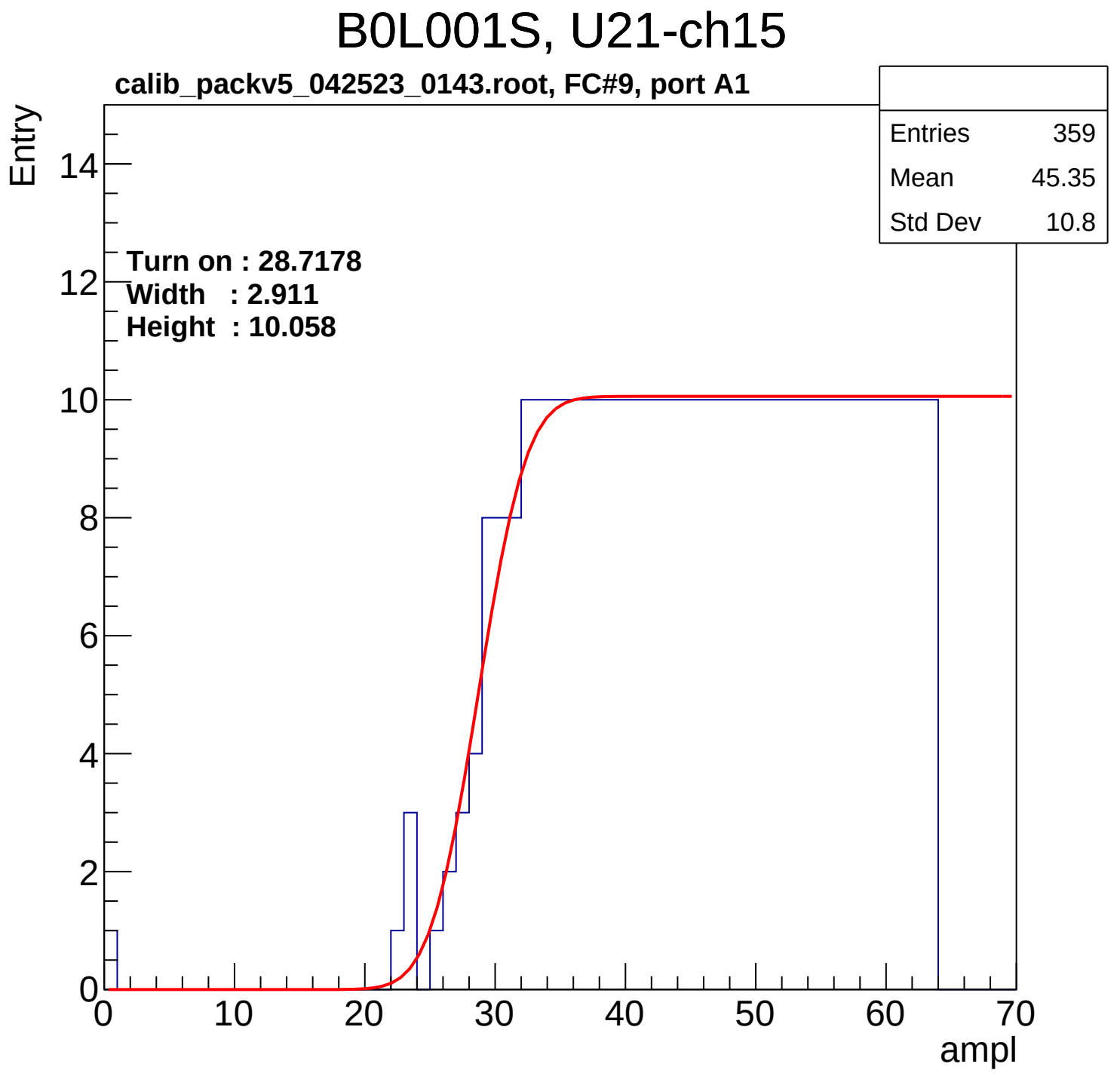
B0L001S, U21-ch15
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 45.35
Std Dev 10.8
Turn on : 28.7178
Width : 2.911
Height : 10.058
Entry
ampl
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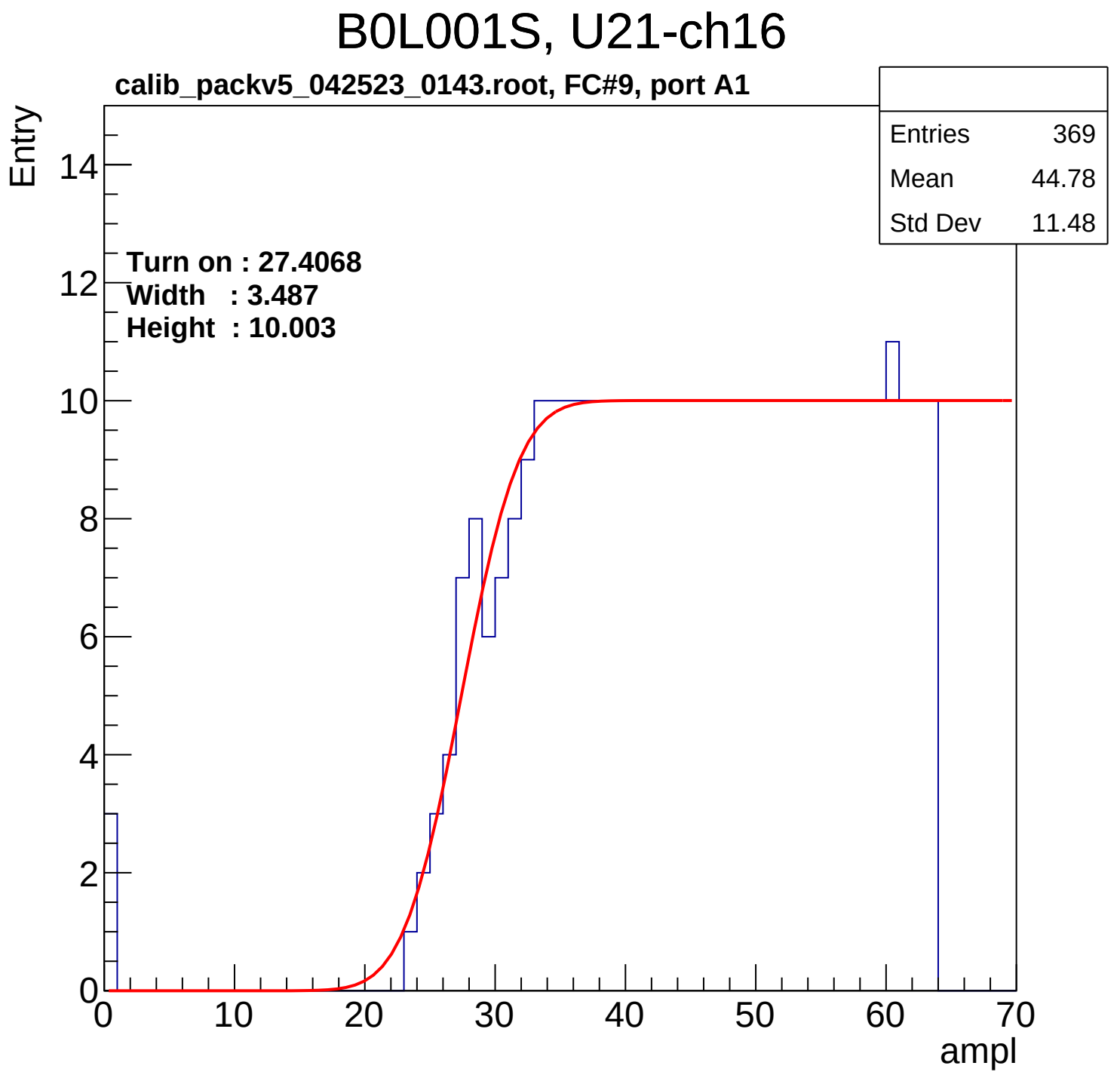
B0L001S, U21-ch16
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.78
Std Dev 11.48
Turn on : 27.4068
Width : 3.487
Height : 10.003
Entry
ampl
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8
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0
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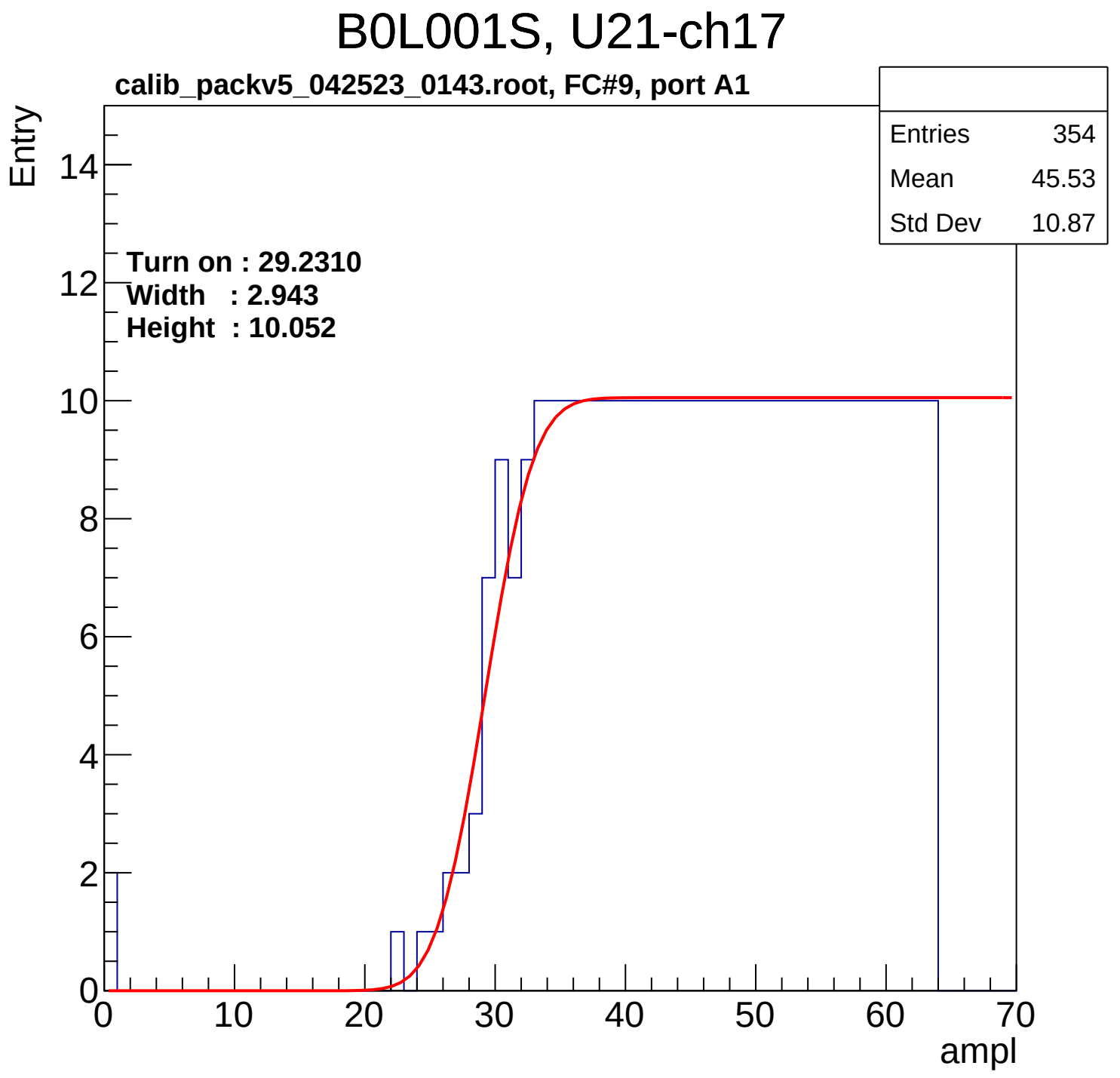
B0L001S, U21-ch17
calib_packv5_042523_0143.root, FC#9, port A1
Entries 354
Mean 45.53
Std Dev 10.87
Turn on : 29.2310
Width : 2.943
Height : 10.052
Entry
ampl
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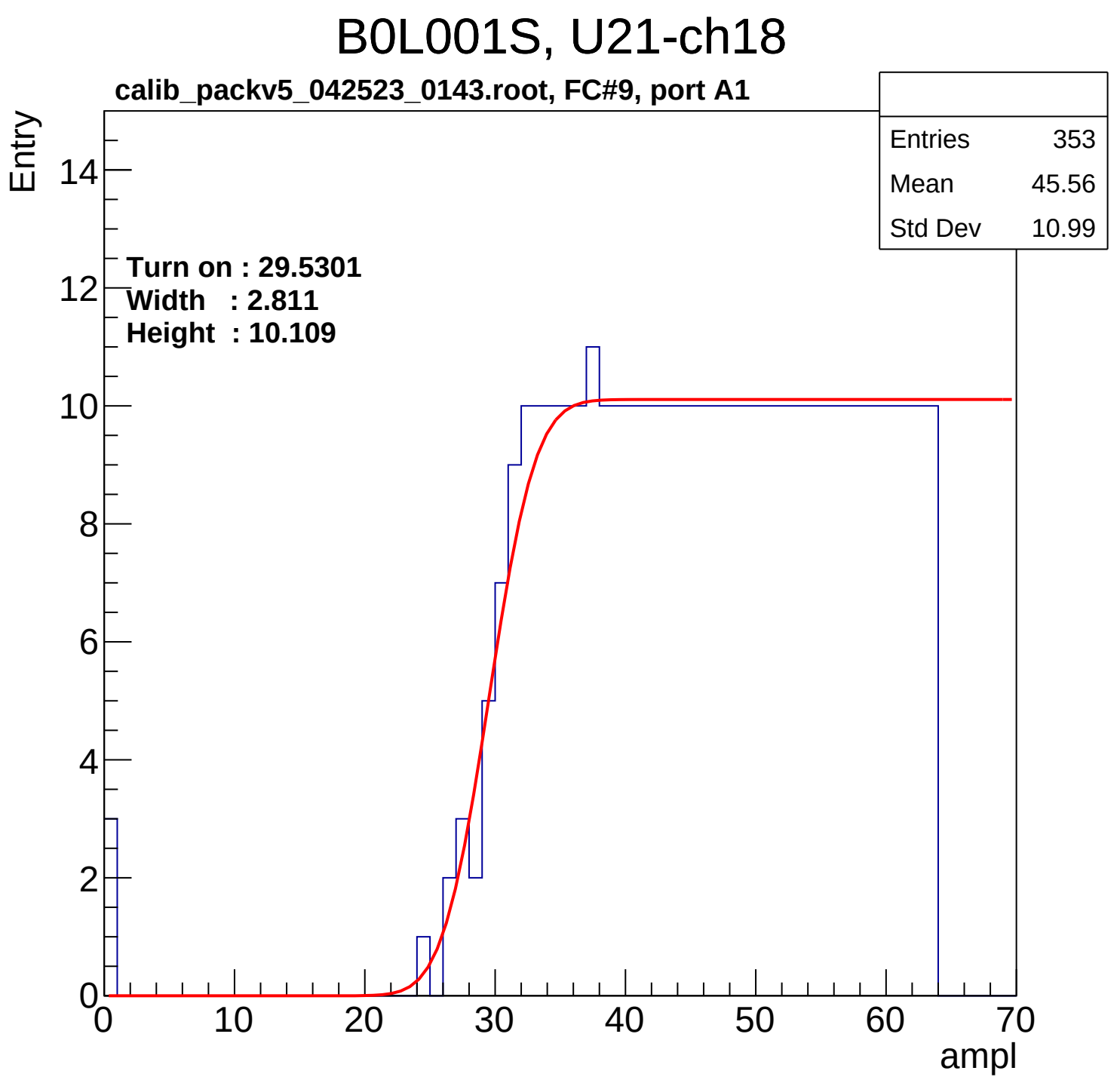
B0L001S, U21-ch18
calib_packv5_042523_0143.root, FC#9, port A1
Entries 353
Mean 45.56
Std Dev 10.99
Turn on : 29.5301
Width : 2.811
Height : 10.109
Entry
ampl
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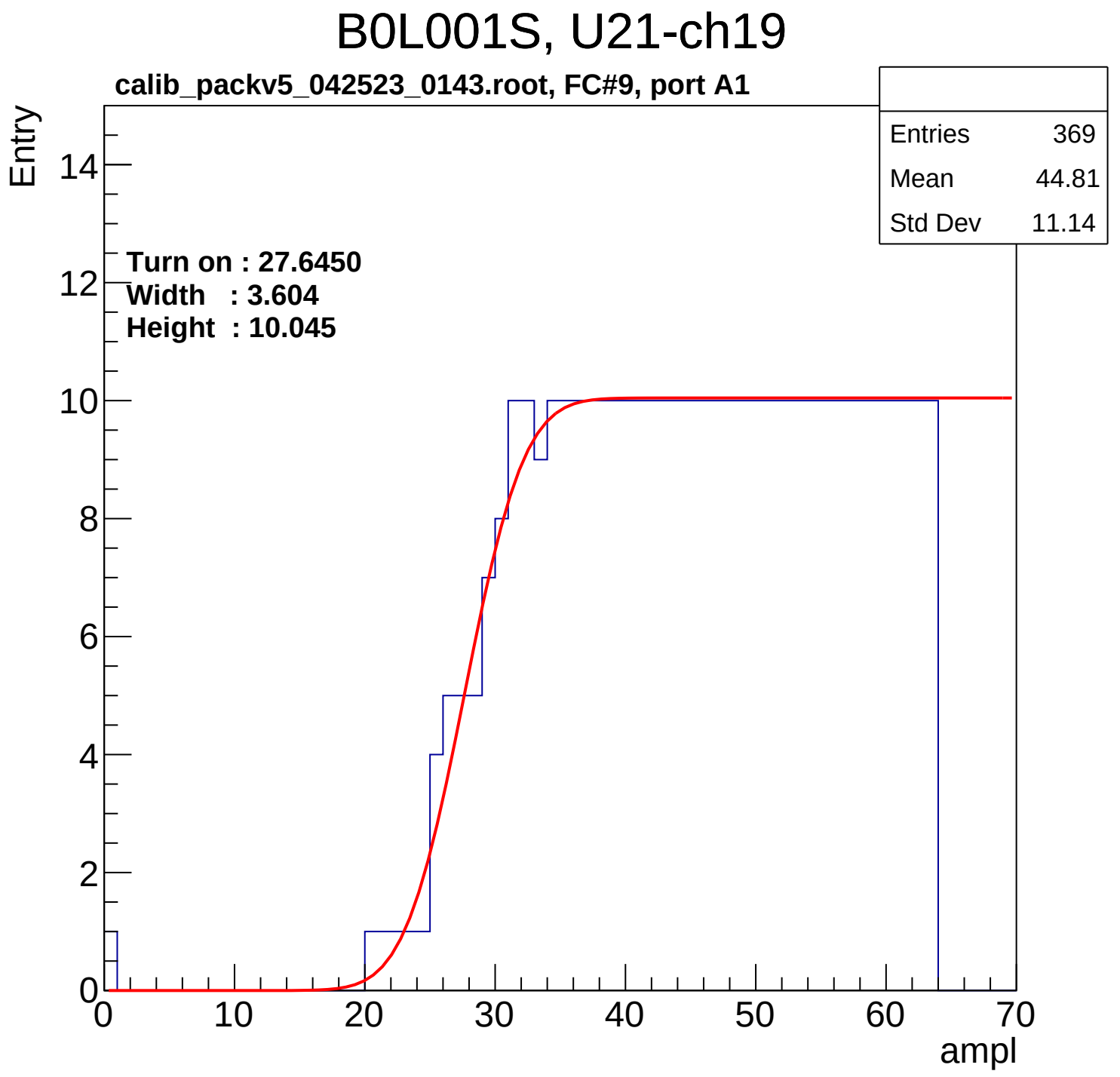
B0L001S, U21-ch19
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.81
Std Dev 11.14
Turn on : 27.6450
Width : 3.604
Height : 10.045
Entry
ampl
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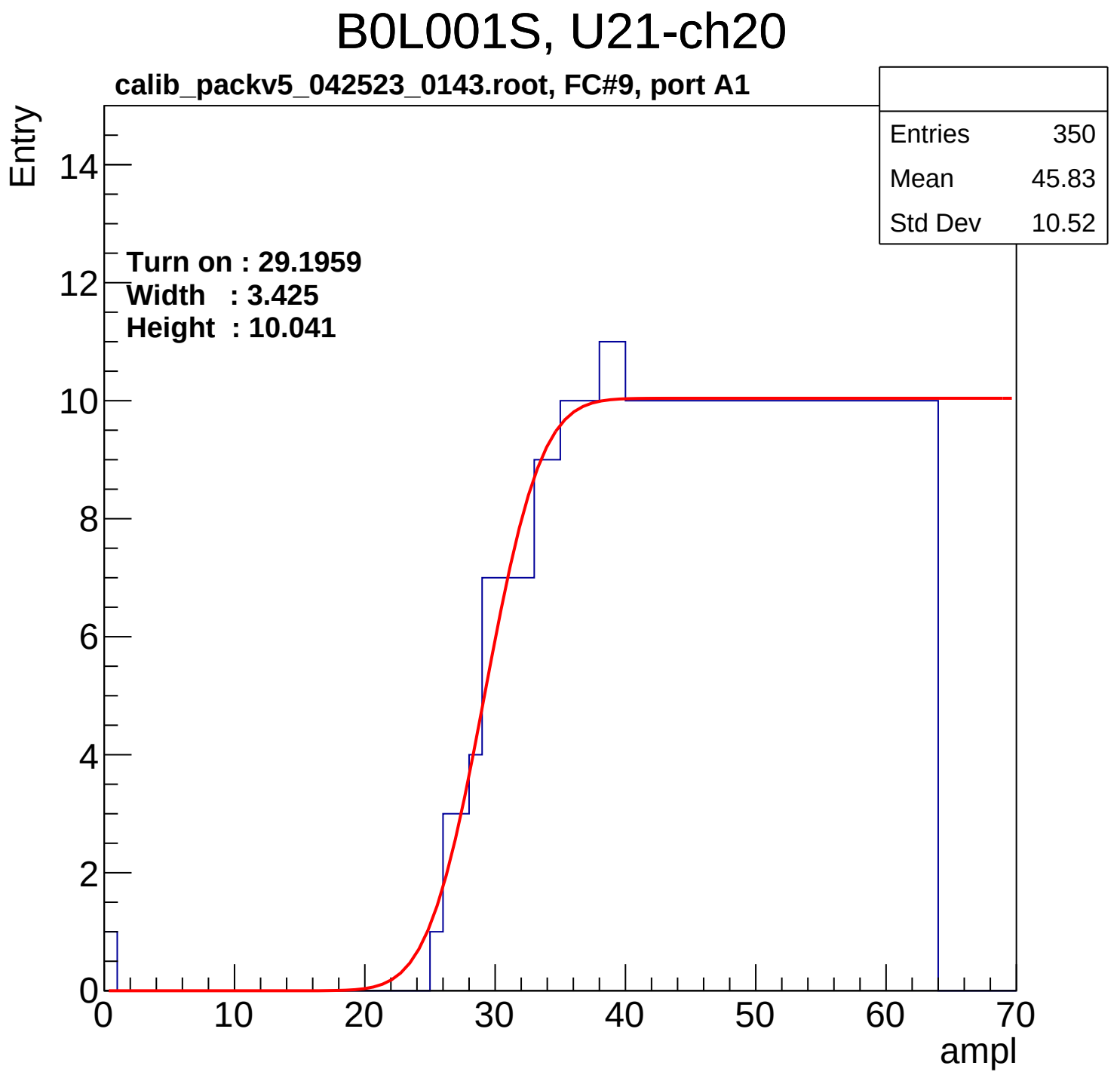
B0L001S, U21-ch20
calib_packv5_042523_0143.root, FC#9, port A1
Entries 350
Mean 45.83
Std Dev 10.52
Turn on : 29.1959
Width : 3.425
Height : 10.041
Entry
ampl
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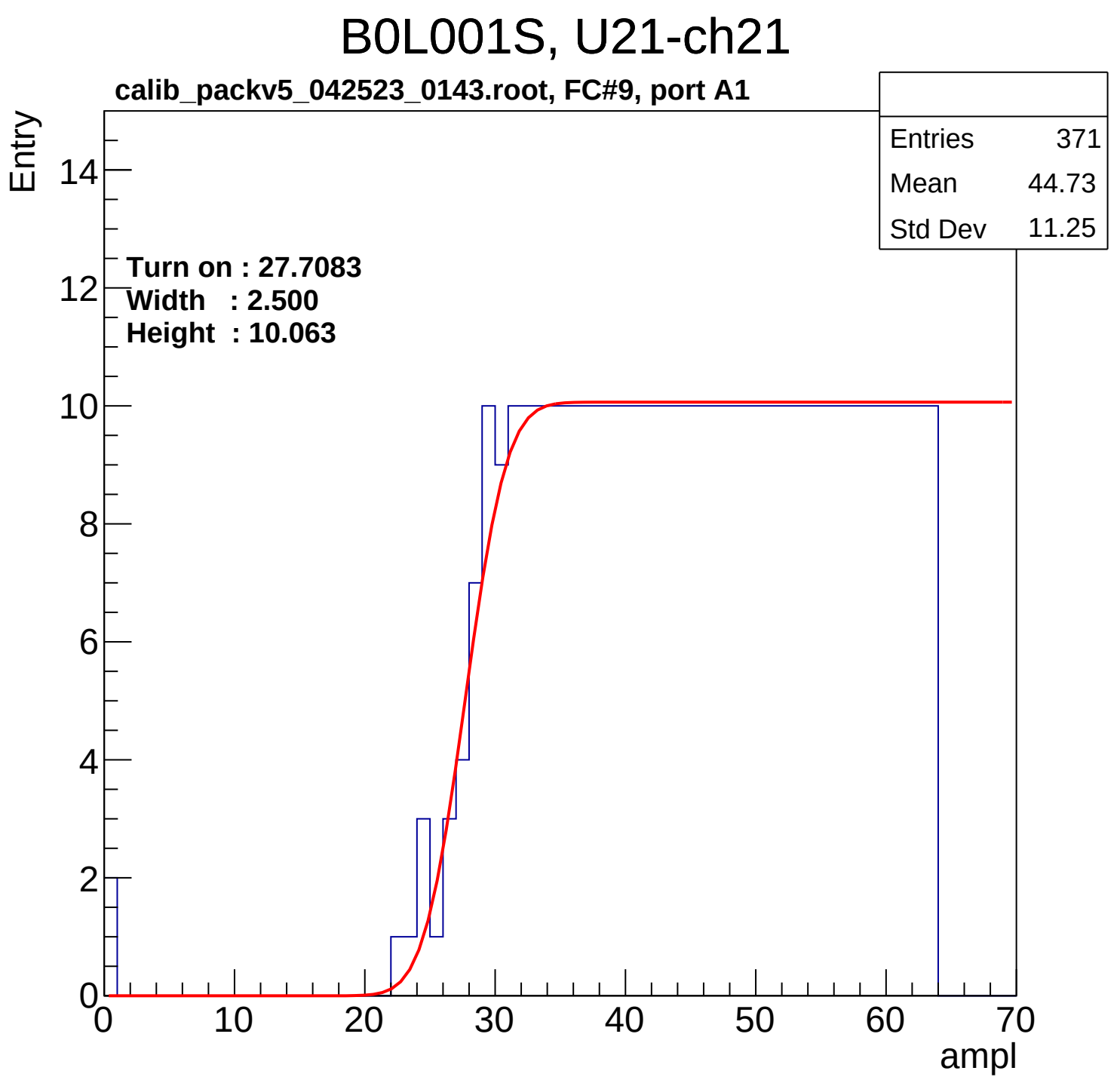
B0L001S, U21-ch21
calib_packv5_042523_0143.root, FC#9, port A1
Entries 371
Mean 44.73
Std Dev 11.25
Turn on : 27.7083
Width : 2.500
Height : 10.063
Entry
ampl
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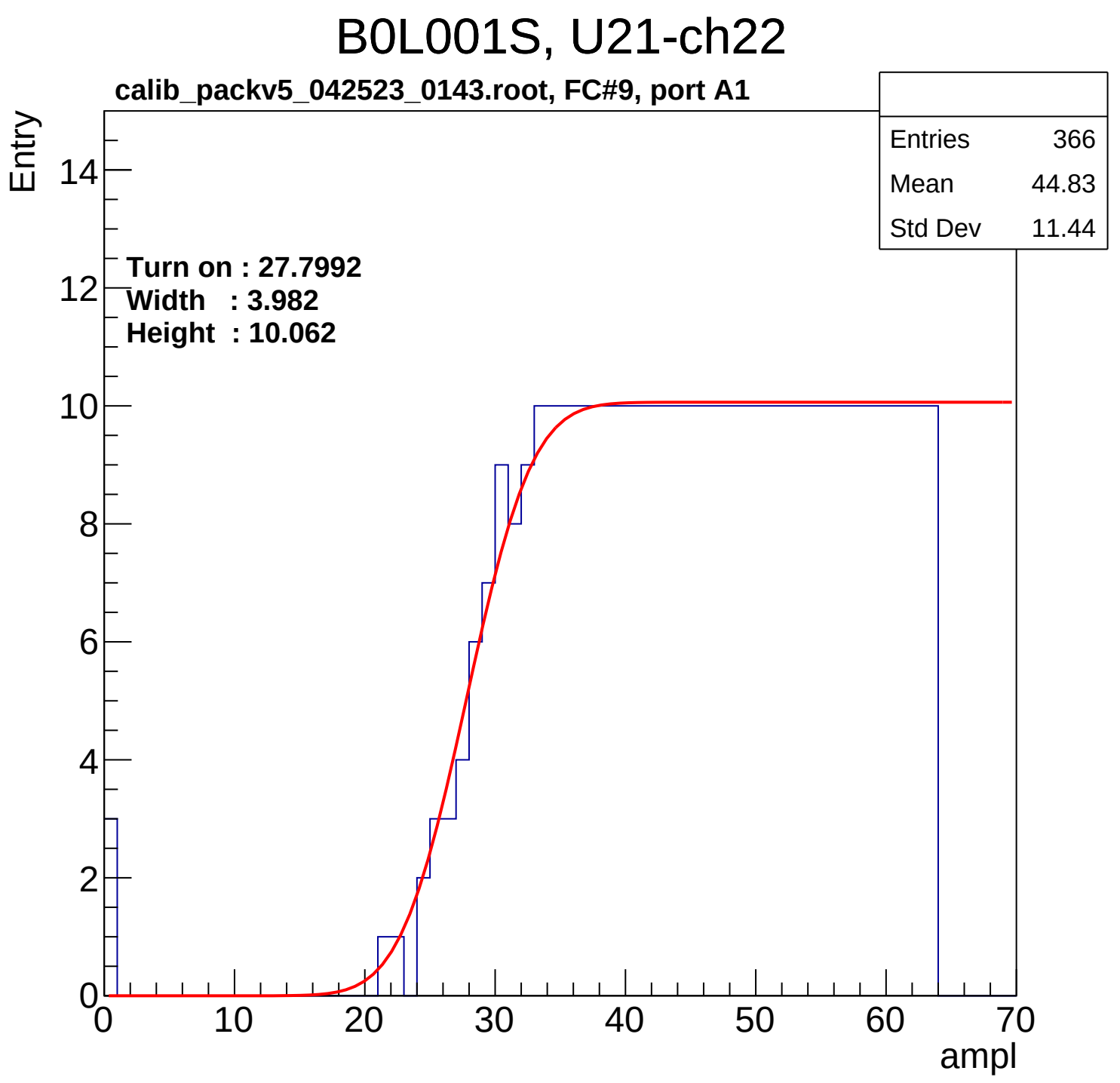
B0L001S, U21-ch22
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.83
Std Dev 11.44
Turn on : 27.7992
Width : 3.982
Height : 10.062
Entry
ampl
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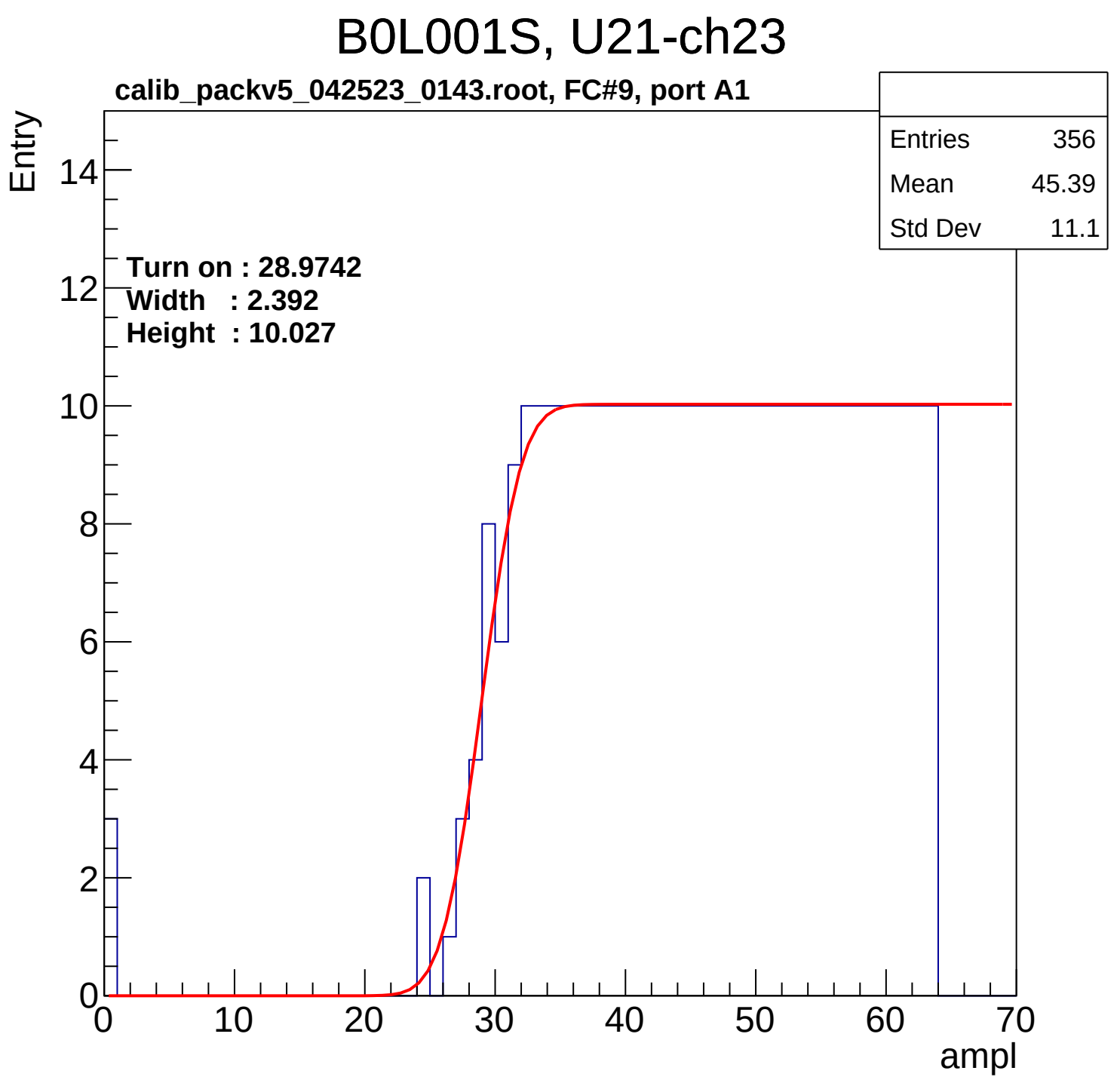
B0L001S, U21-ch23
calib_packv5_042523_0143.root, FC#9, port A1
Entries 356
Mean 45.39
Std Dev 11.1
Turn on : 28.9742
Width : 2.392
Height : 10.027
Entry
ampl
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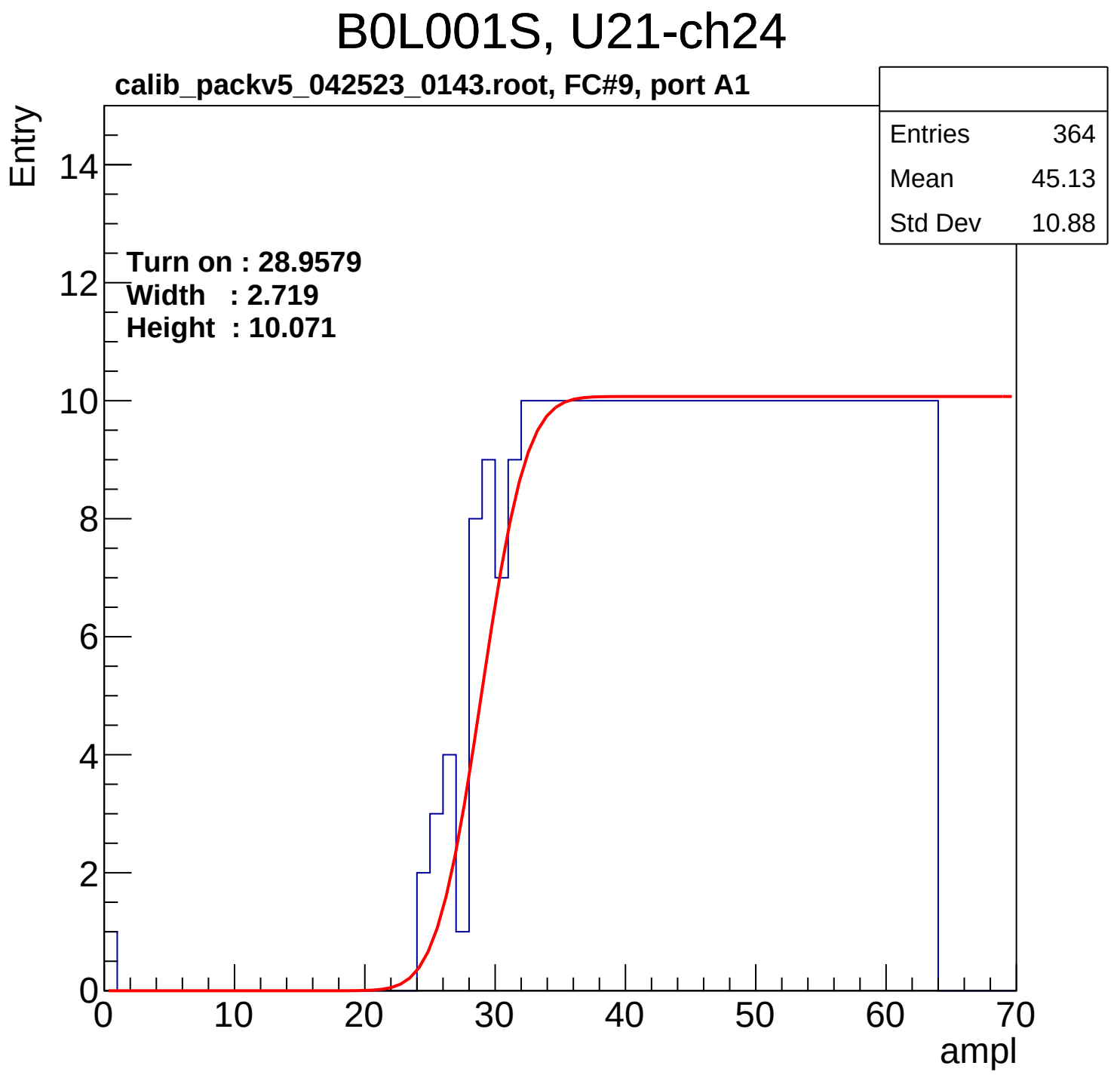
B0L001S, U21-ch24
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 45.13
Std Dev 10.88
Turn on : 28.9579
Width : 2.719
Height : 10.071
Entry
ampl
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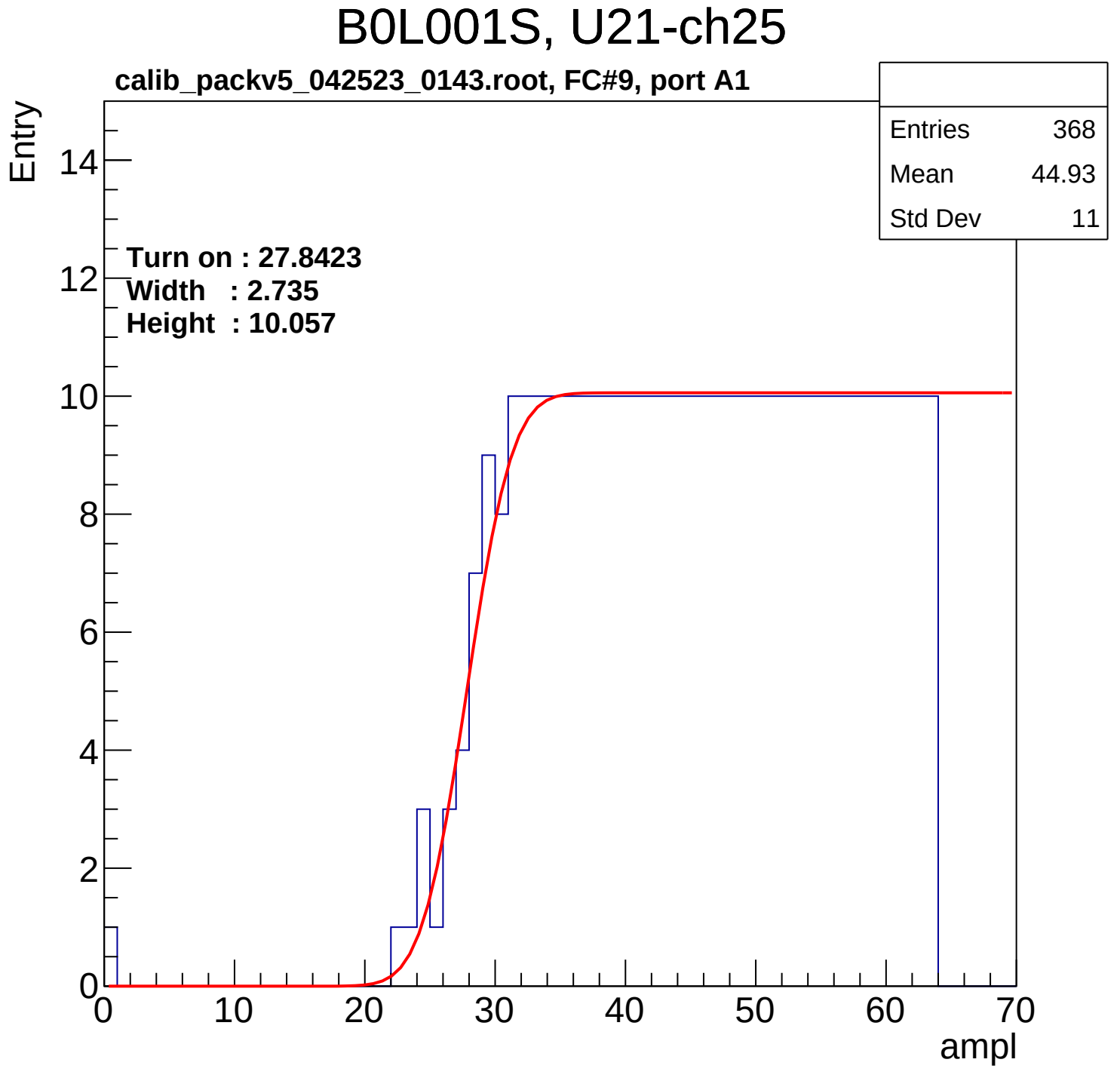
B0L001S, U21-ch25
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.93
Std Dev 11
Turn on : 27.8423
Width : 2.735
Height : 10.057
Entry
ampl
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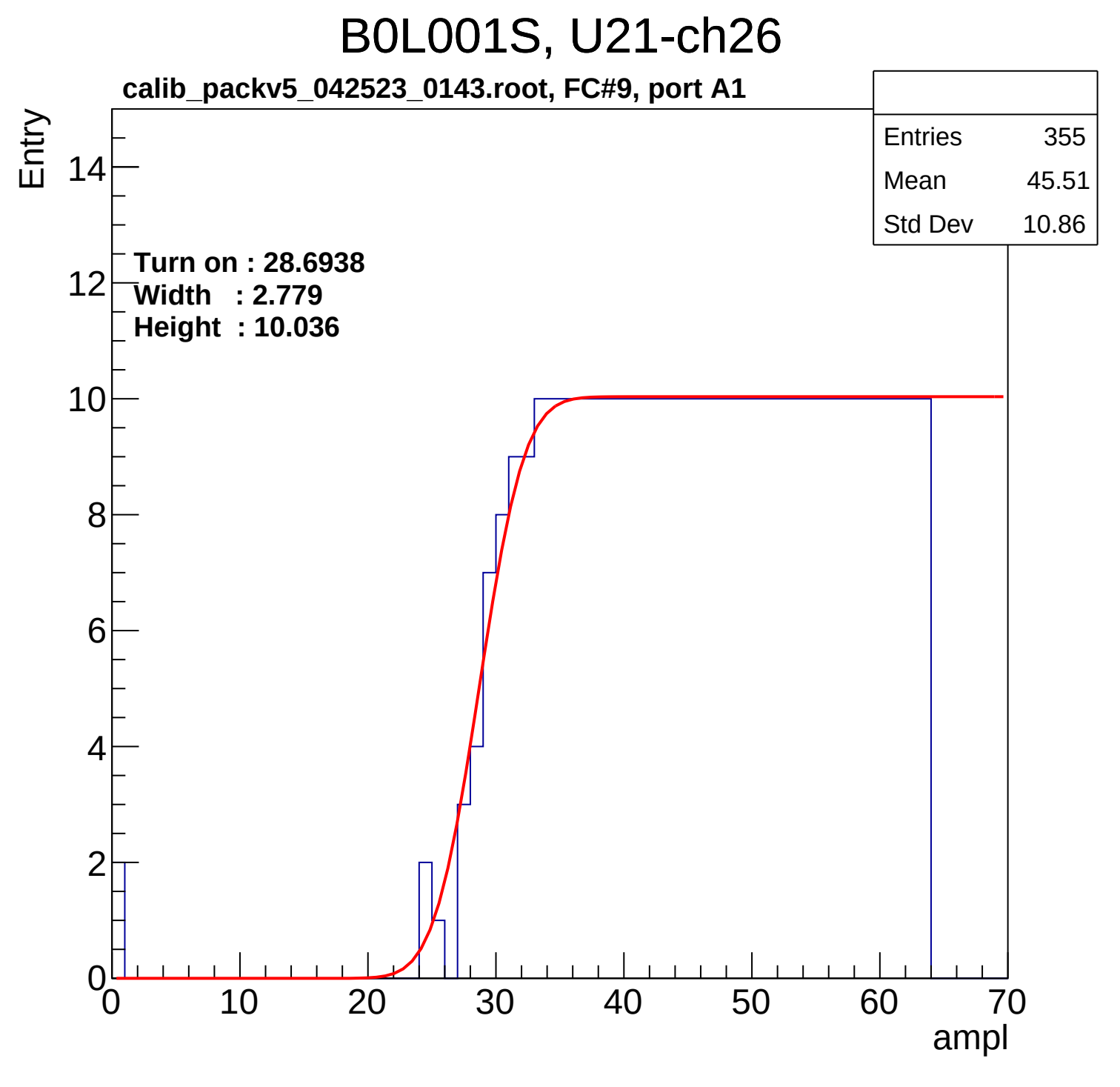
B0L001S, U21-ch26
calib_packv5_042523_0143.root, FC#9, port A1
Entries 355
Mean 45.51
Std Dev 10.86
Turn on : 28.6938
Width : 2.779
Height : 10.036
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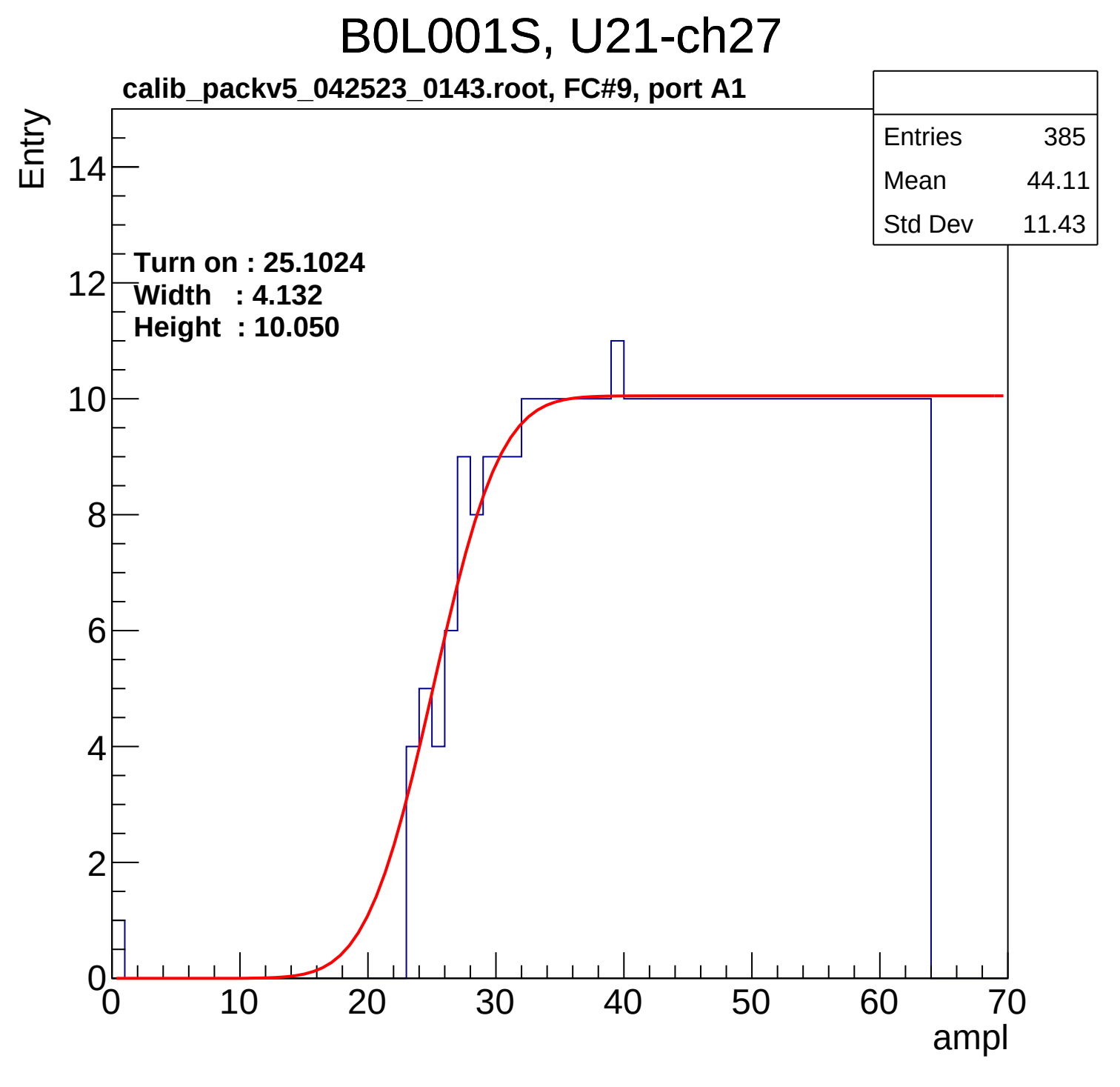
B0L001S, U21-ch27
calib_packv5_042523_0143.root, FC#9, port A1
Entries 385
Mean 44.11
Std Dev 11.43
Turn on : 25.1024
Width : 4.132
Height : 10.050
Entry
ampl
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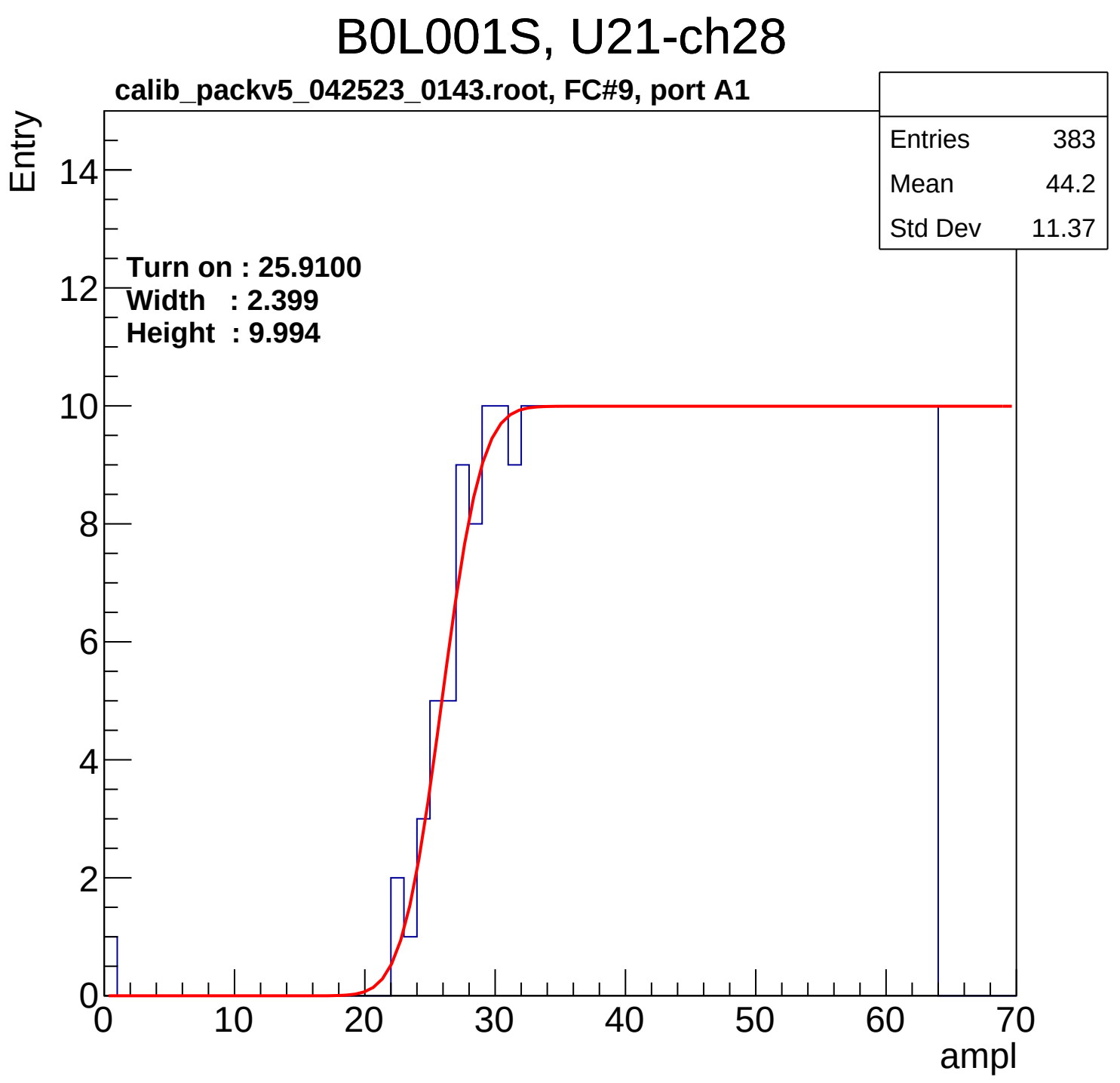
B0L001S, U21-ch28
calib_packv5_042523_0143.root, FC#9, port A1
Entries 383
Mean 44.2
Std Dev 11.37
Turn on : 25.9100
Width : 2.399
Height : 9.994
Entry
ampl
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4
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12
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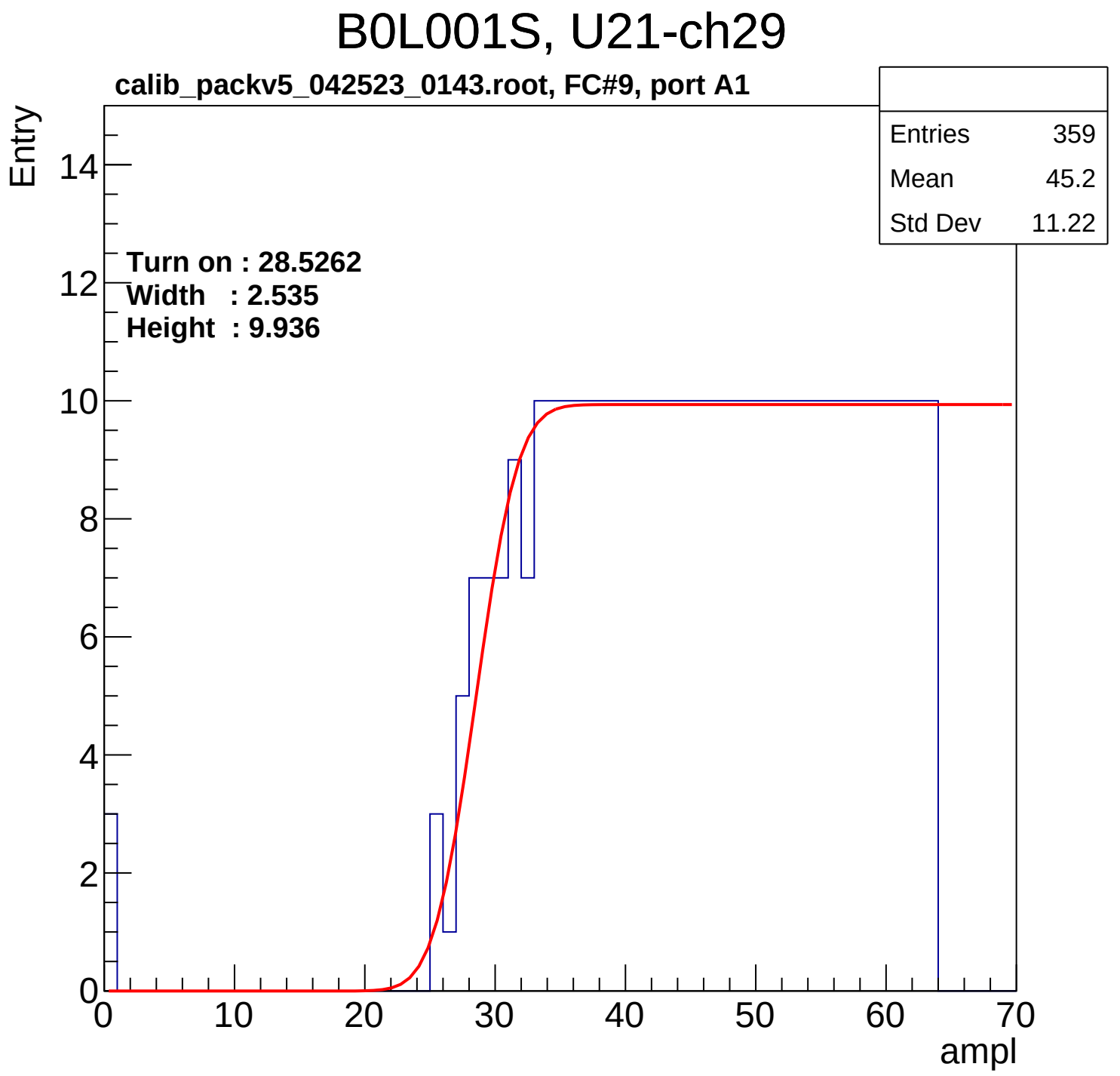
B0L001S, U21-ch29
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 45.2
Std Dev 11.22
Turn on : 28.5262
Width : 2.535
Height : 9.936
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ampl
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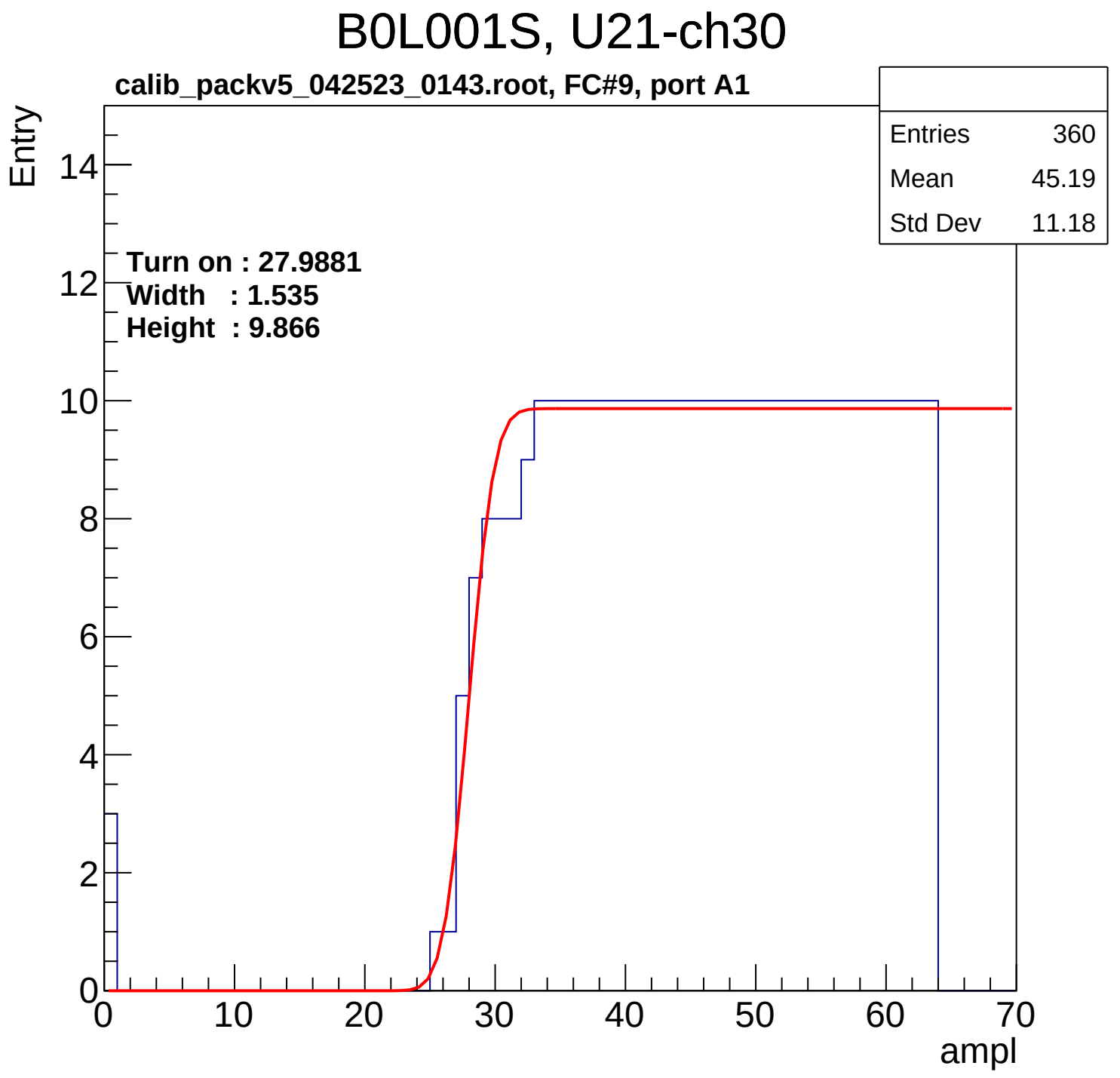
B0L001S, U21-ch30
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 45.19
Std Dev 11.18
Turn on : 27.9881
Width : 1.535
Height : 9.866
Entry
ampl
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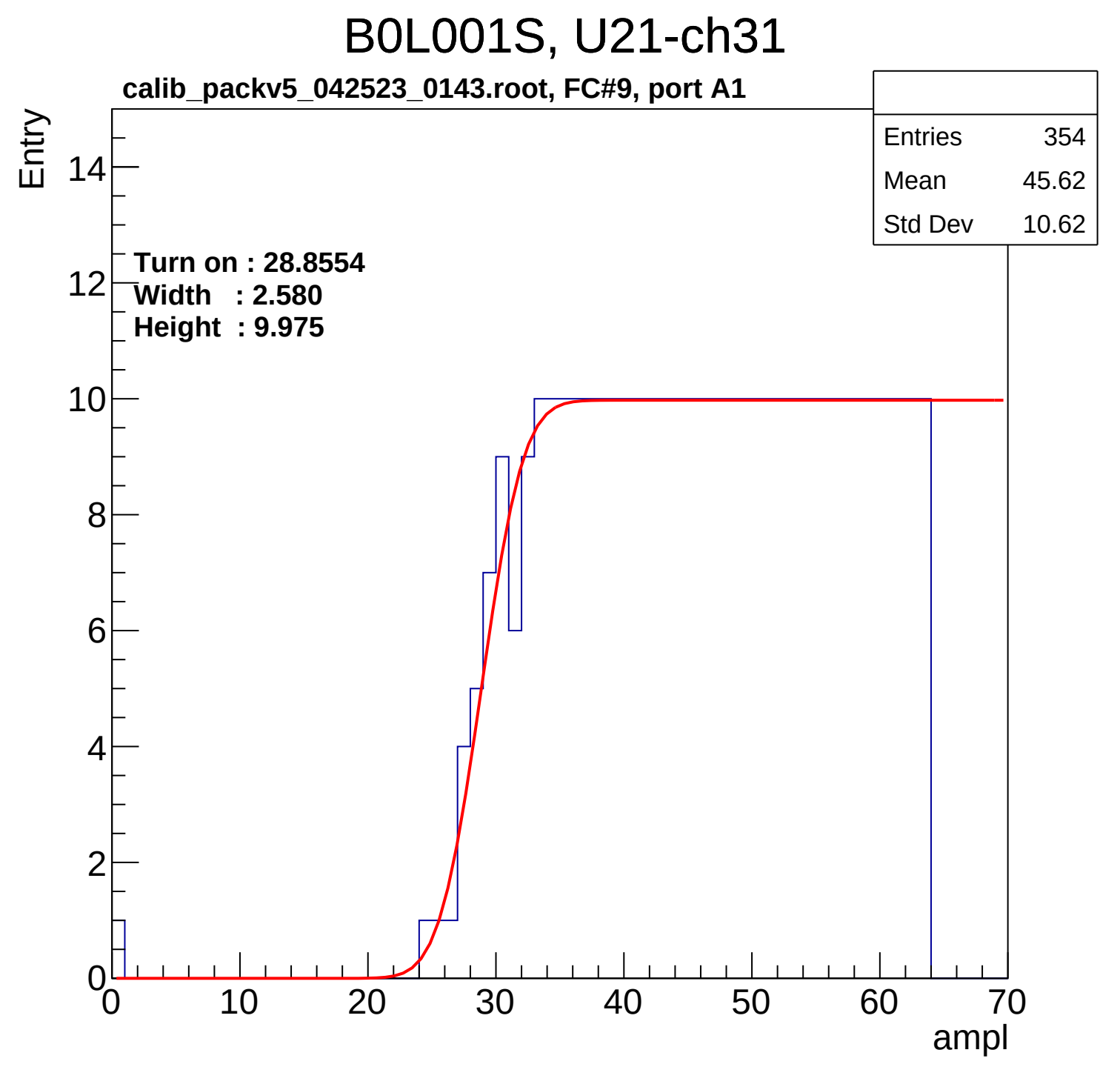
B0L001S, U21-ch31
calib_packv5_042523_0143.root, FC#9, port A1
Entries 354
Mean 45.62
Std Dev 10.62
Turn on : 28.8554
Width : 2.580
Height : 9.975
Entry
ampl
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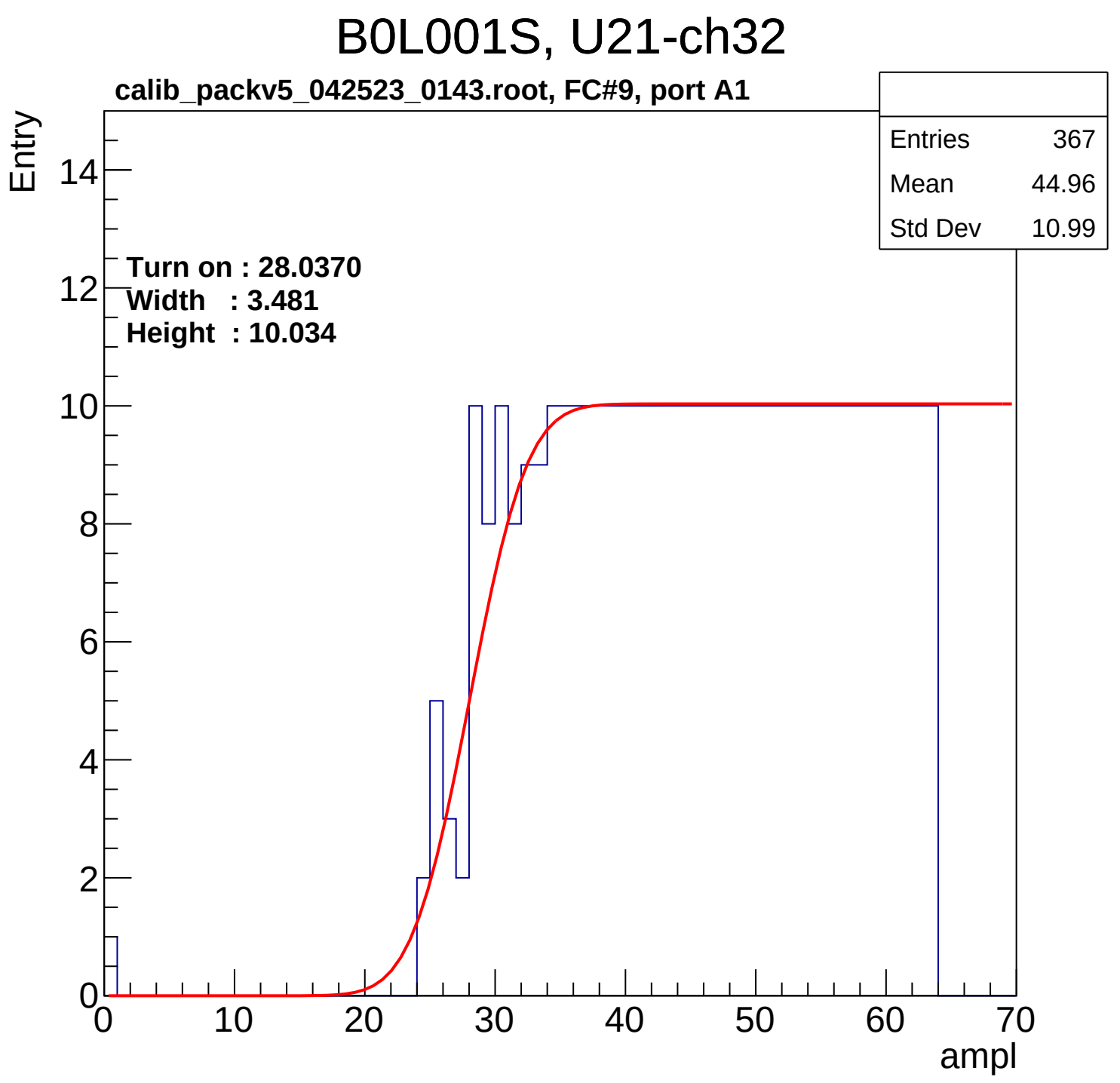
B0L001S, U21-ch32
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.96
Std Dev 10.99
Turn on : 28.0370
Width : 3.481
Height : 10.034
Entry
ampl
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6
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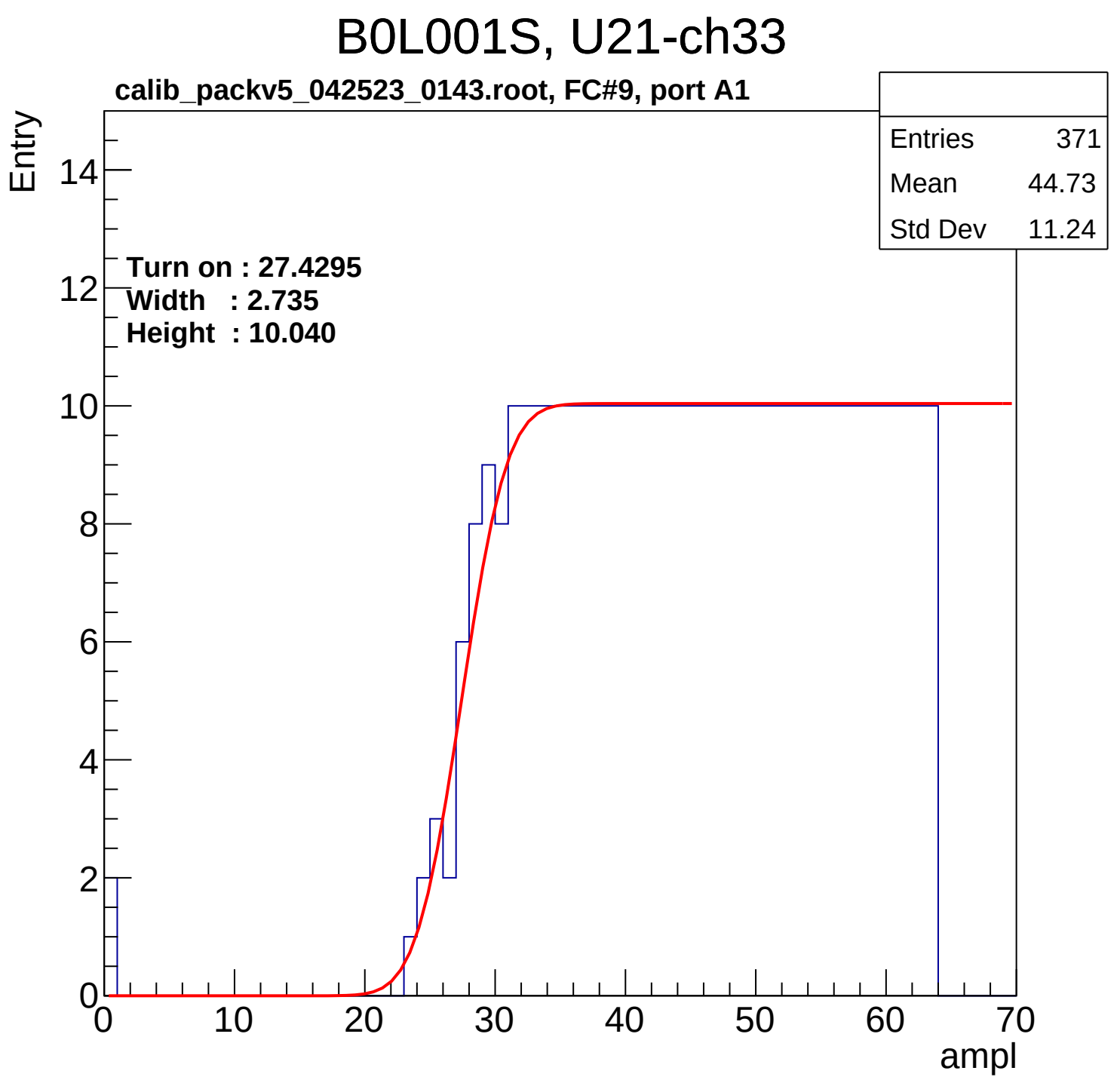
B0L001S, U21-ch33
calib_packv5_042523_0143.root, FC#9, port A1
Entries 371
Mean 44.73
Std Dev 11.24
Turn on : 27.4295
Width : 2.735
Height : 10.040
Entry
ampl
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4
6
8
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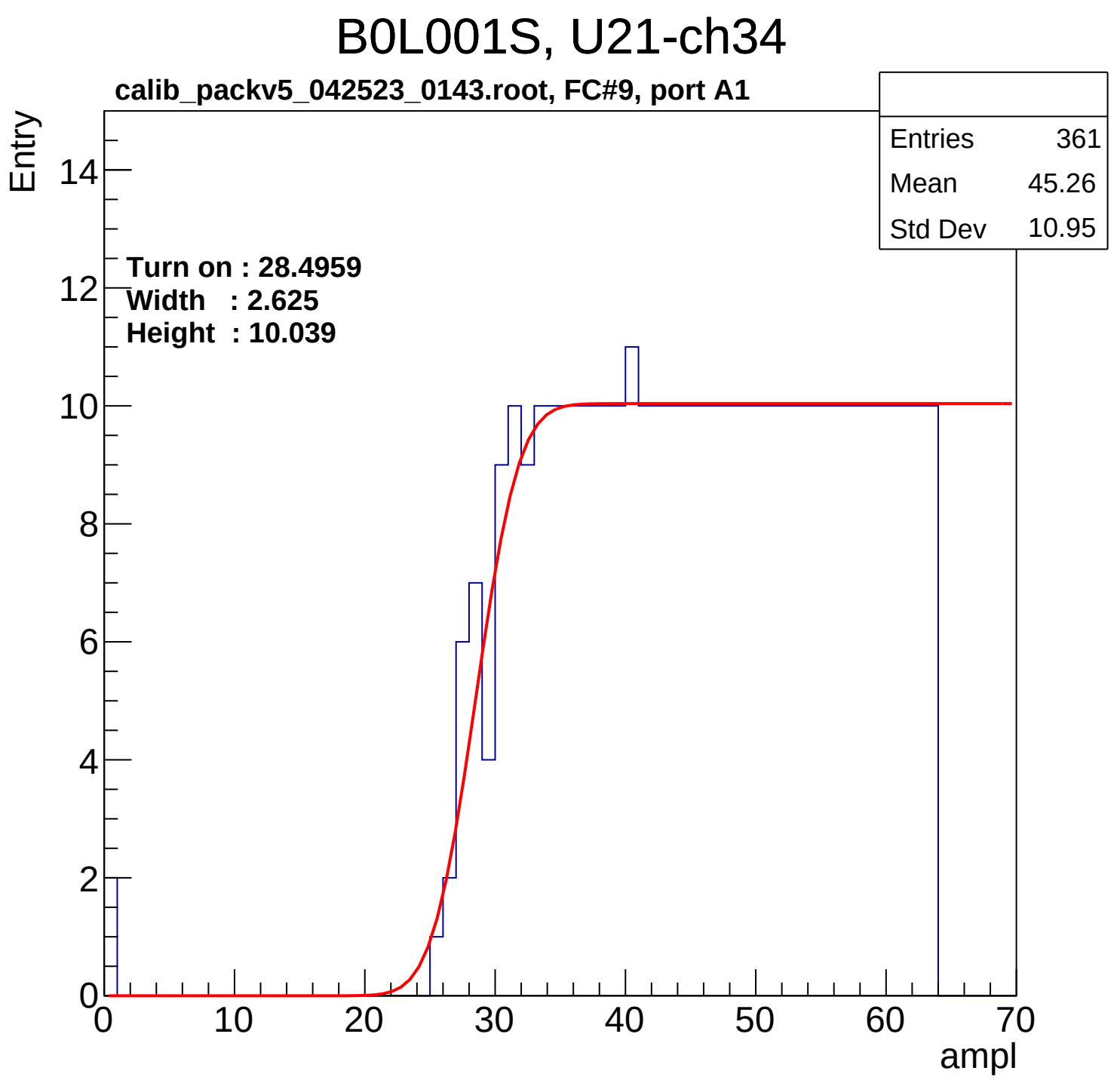
B0L001S, U21-ch34
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 45.26
Std Dev 10.95
Turn on : 28.4959
Width : 2.625
Height : 10.039
Entry
ampl
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2
4
6
8
10
12
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0
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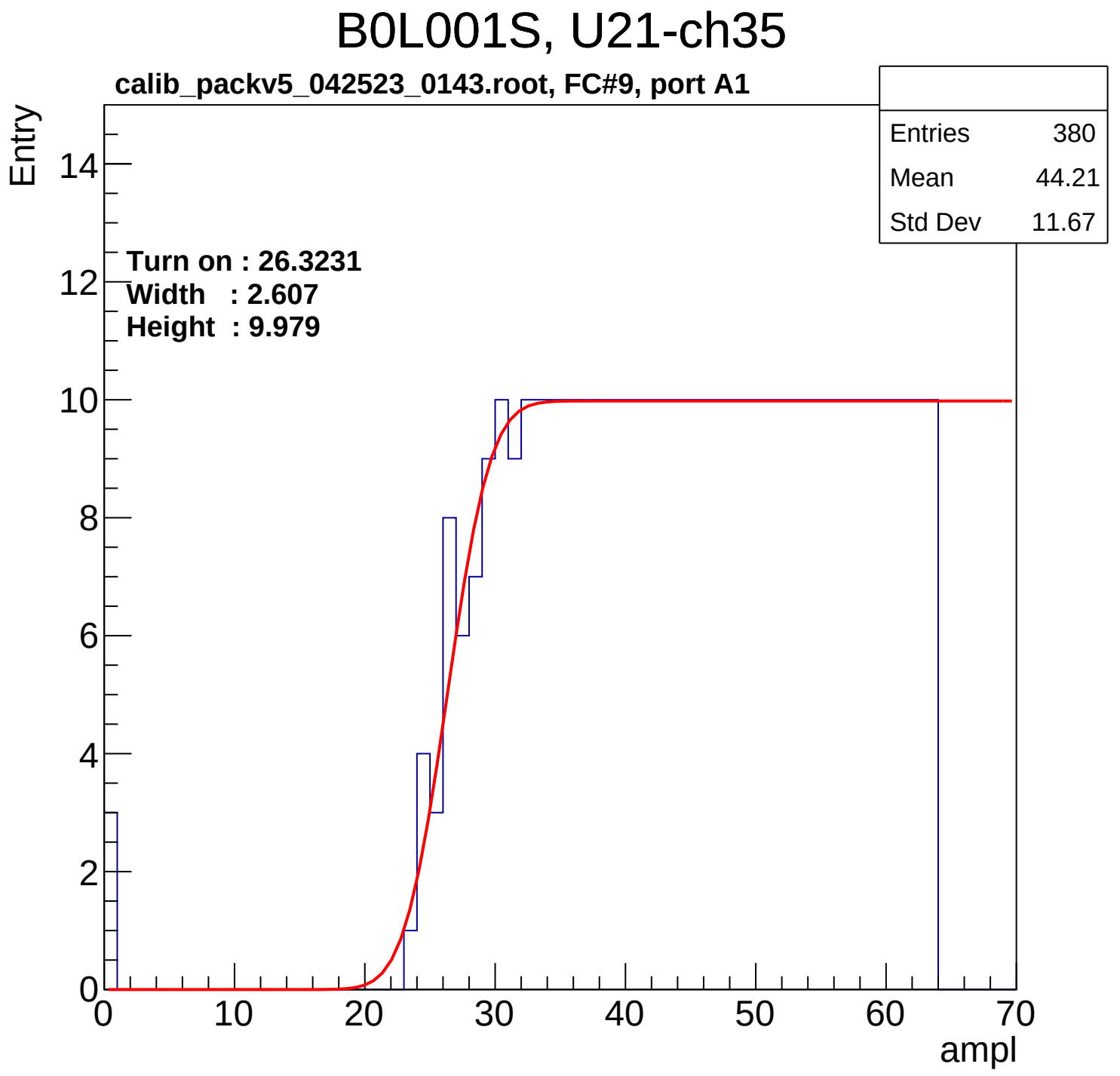
B0L001S, U21-ch35
calib_packv5_042523_0143.root, FC#9, port A1
Entries 380
Mean 44.21
Std Dev 11.67
Turn on : 26.3231
Width : 2.607
Height : 9.979
Entry
ampl
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2
4
6
8
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12
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0
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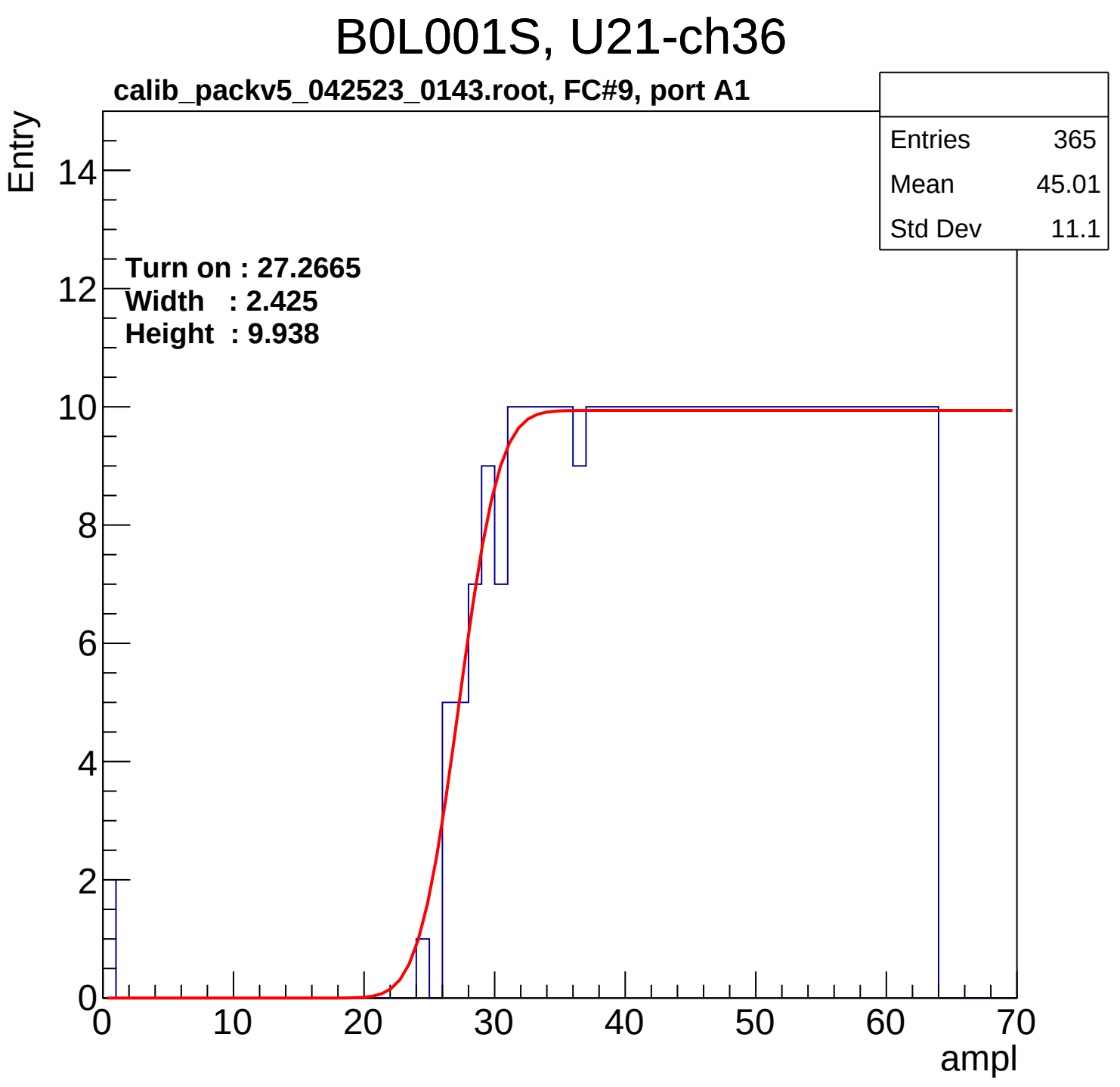
B0L001S, U21-ch36
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 45.01
Std Dev 11.1
Turn on : 27.2665
Width : 2.425
Height : 9.938
Entry
ampl
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2
4
6
8
10
12
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0
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20
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40
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60
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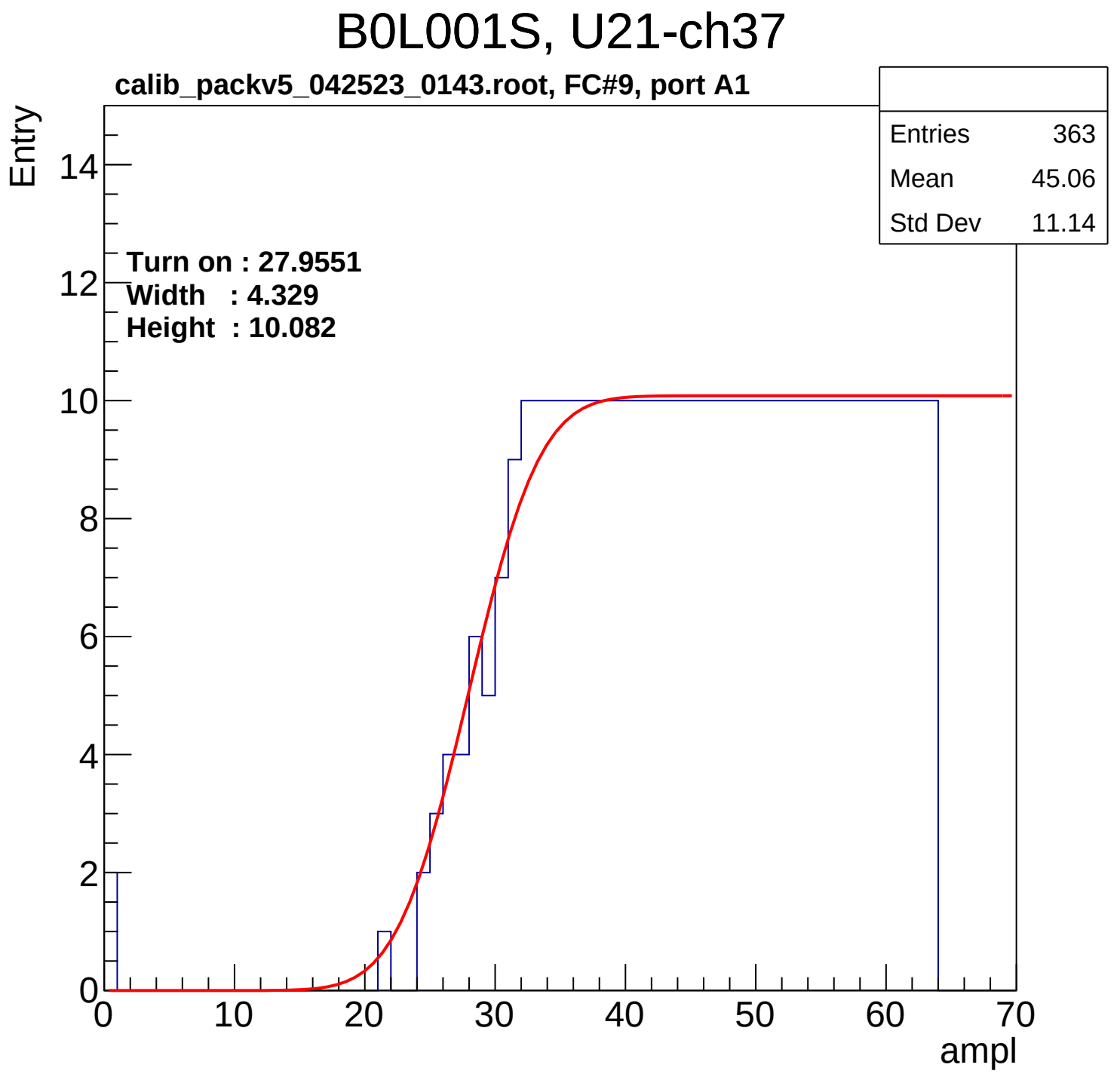
B0L001S, U21-ch37
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 45.06
Std Dev 11.14
Turn on : 27.9551
Width : 4.329
Height : 10.082
Entry
ampl
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2
4
6
8
10
12
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0
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60
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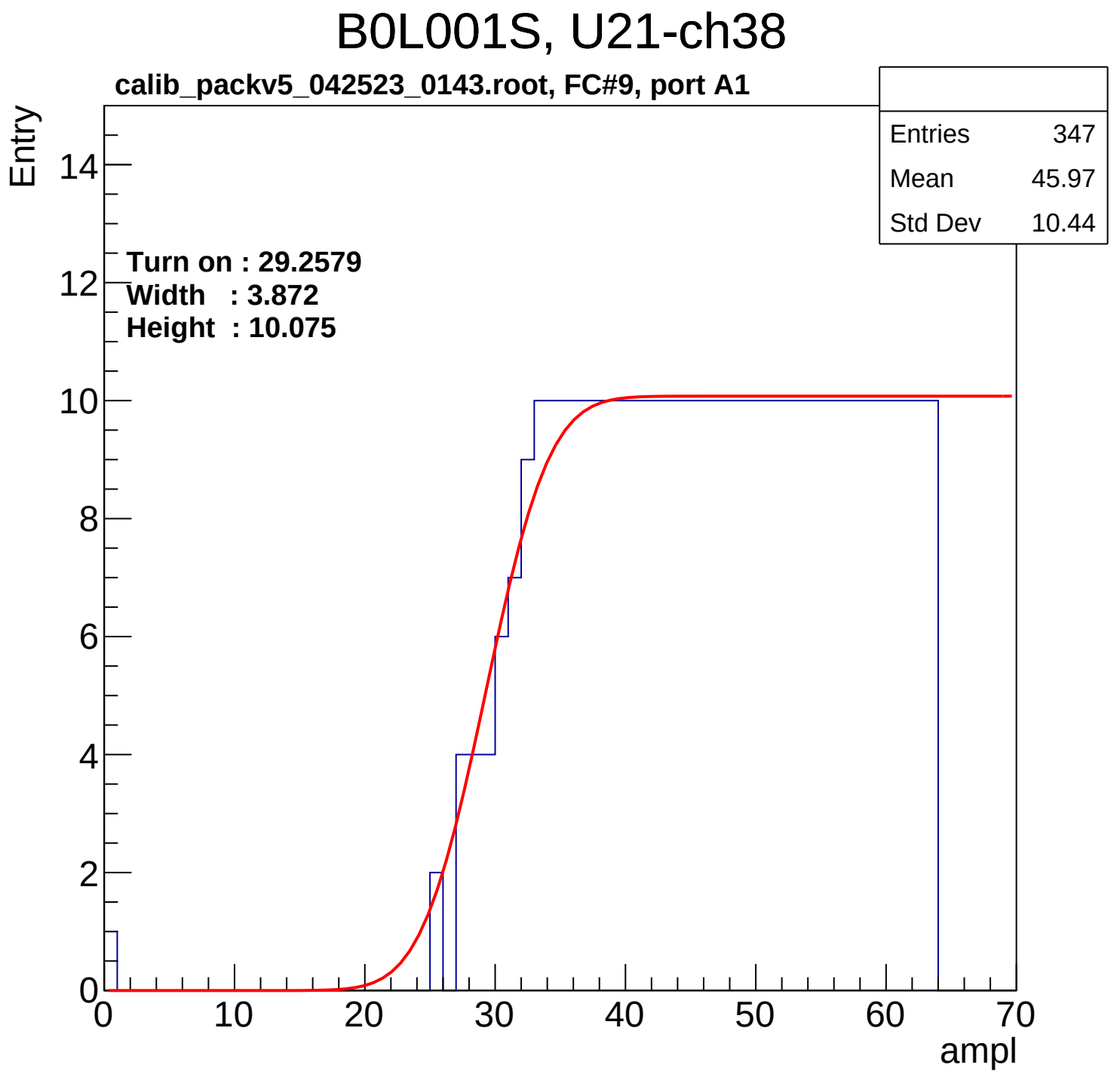
B0L001S, U21-ch38
calib_packv5_042523_0143.root, FC#9, port A1
Entries 347
Mean 45.97
Std Dev 10.44
Turn on : 29.2579
Width : 3.872
Height : 10.075
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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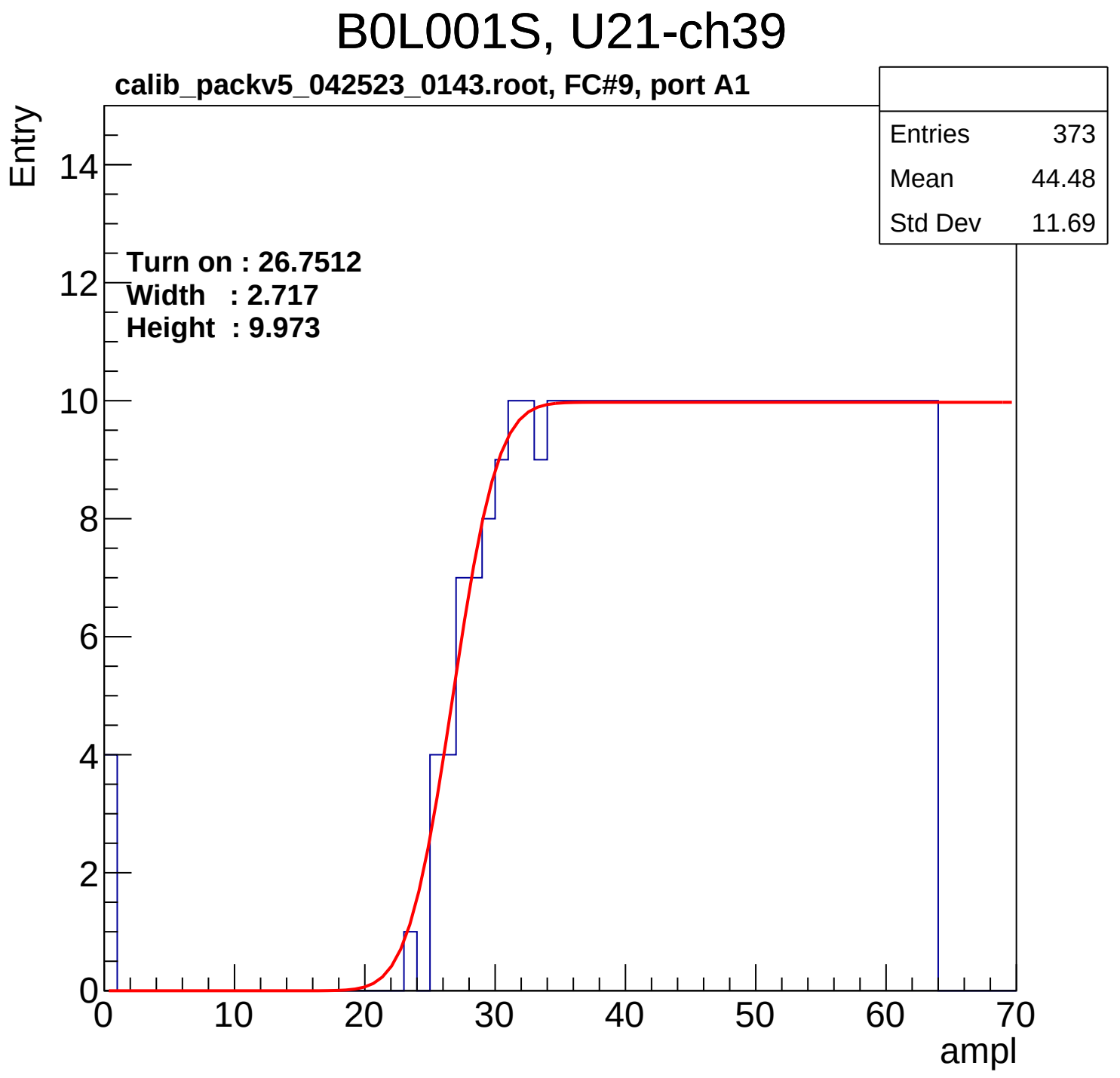
B0L001S, U21-ch39
calib_packv5_042523_0143.root, FC#9, port A1
Entries 373
Mean 44.48
Std Dev 11.69
Turn on : 26.7512
Width : 2.717
Height : 9.973
Entry
ampl
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4
6
8
10
12
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0
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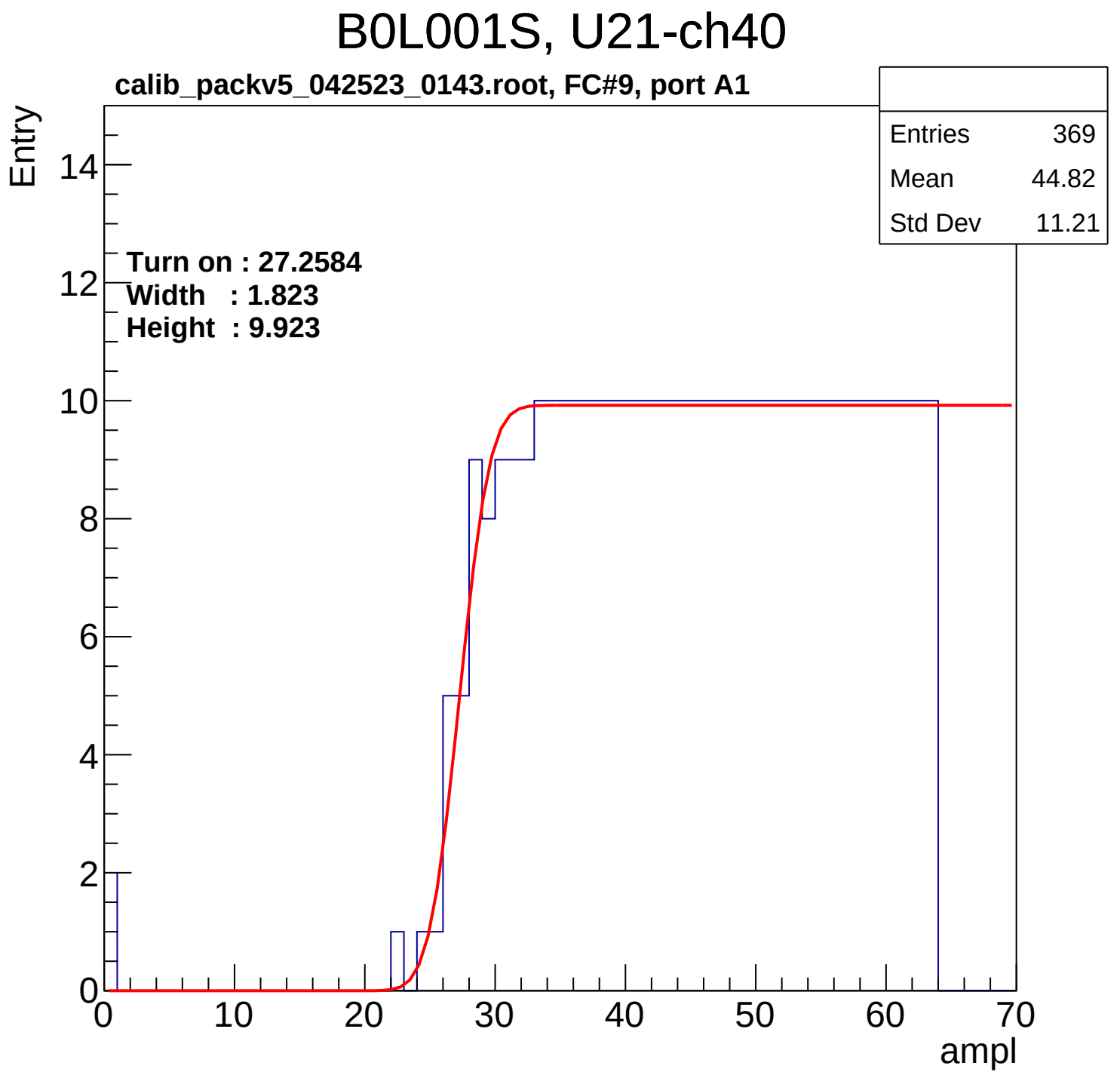
B0L001S, U21-ch40
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.82
Std Dev 11.21
Turn on : 27.2584
Width : 1.823
Height : 9.923
Entry
ampl
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4
6
8
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0
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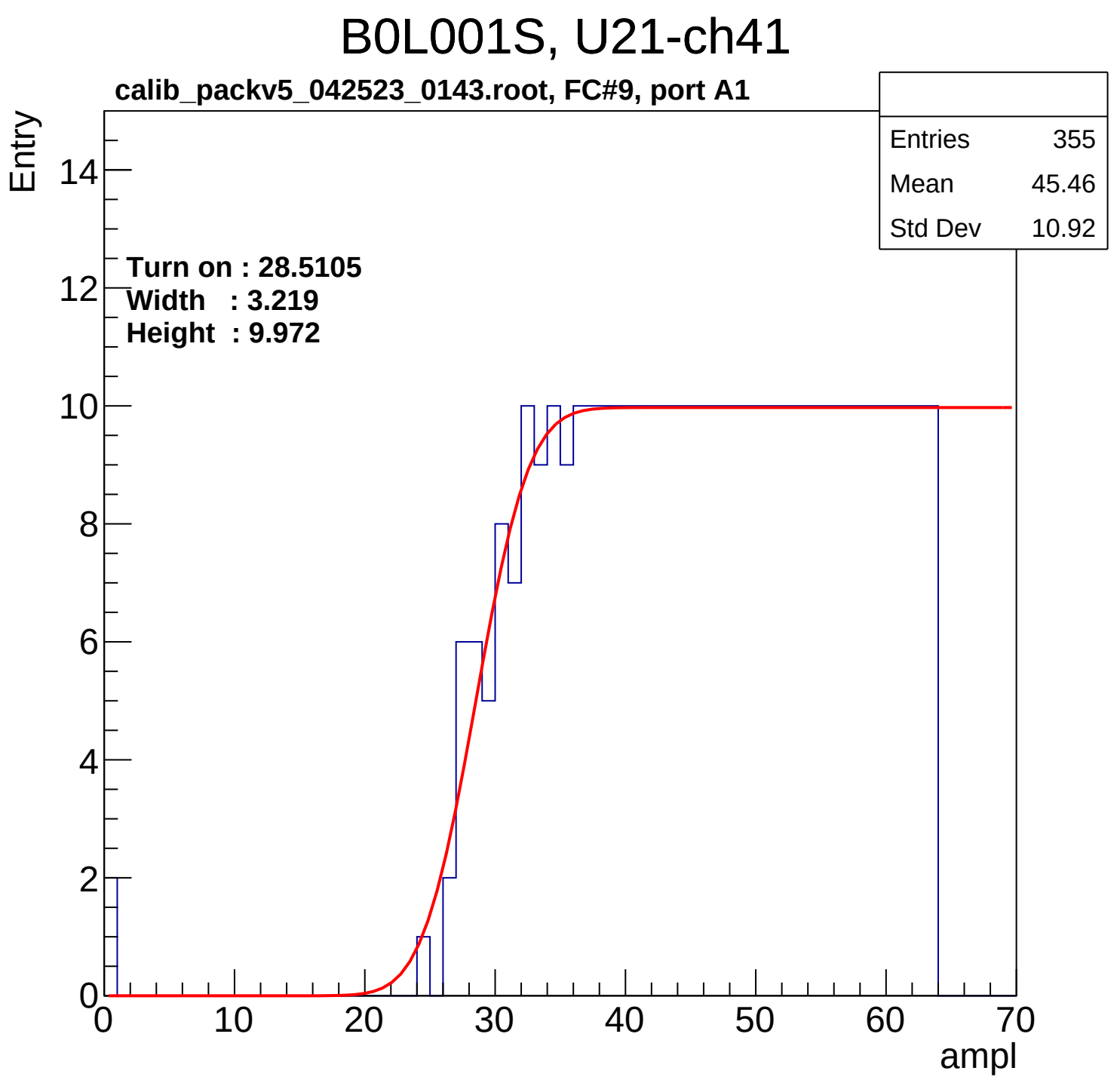
B0L001S, U21-ch41
calib_packv5_042523_0143.root, FC#9, port A1
Entries 355
Mean 45.46
Std Dev 10.92
Turn on : 28.5105
Width : 3.219
Height : 9.972
Entry
ampl
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6
8
10
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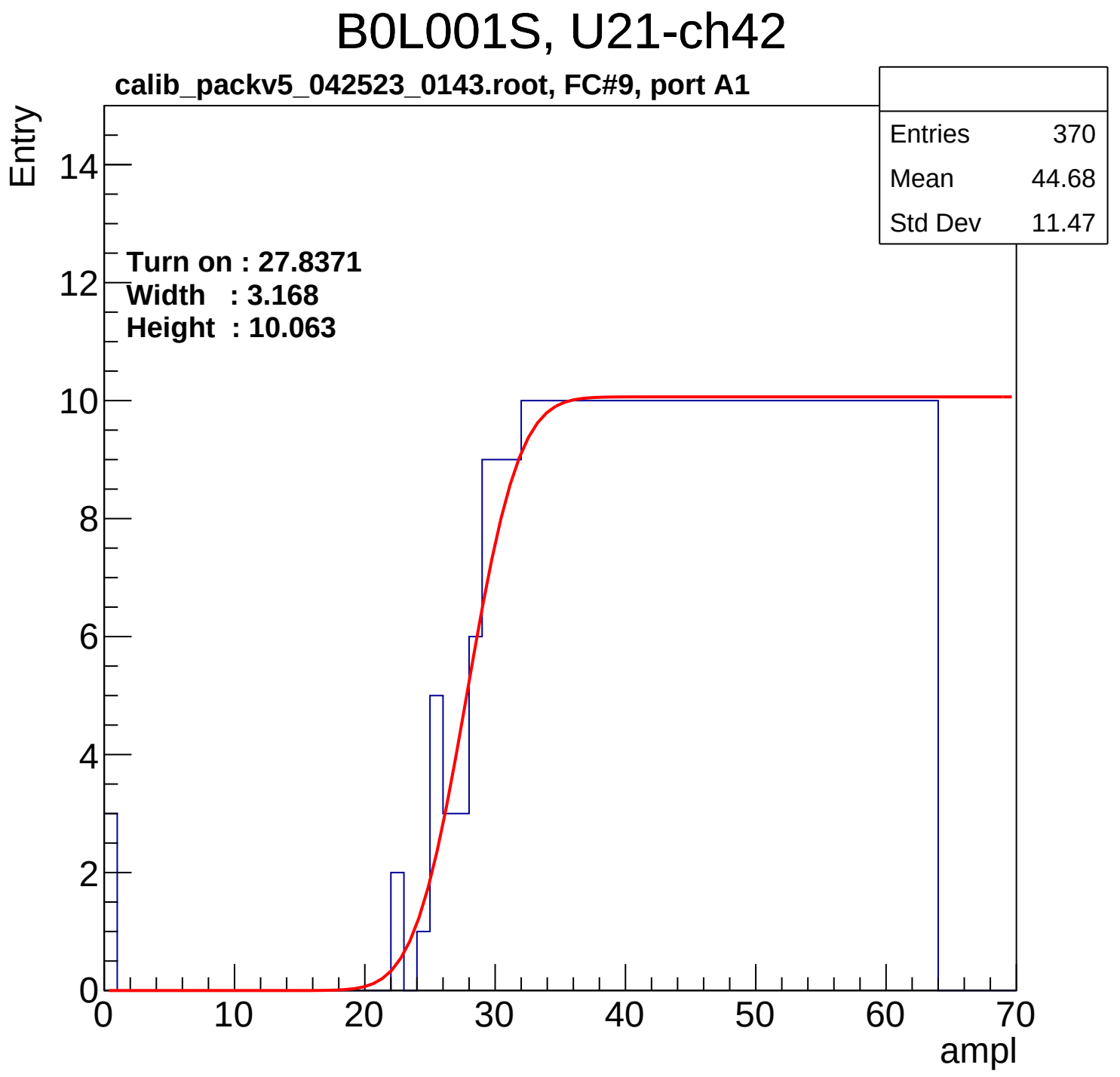
B0L001S, U21-ch42
calib_packv5_042523_0143.root, FC#9, port A1
Entries 370
Mean 44.68
Std Dev 11.47
Turn on : 27.8371
Width : 3.168
Height : 10.063
Entry
ampl
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2
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6
8
10
12
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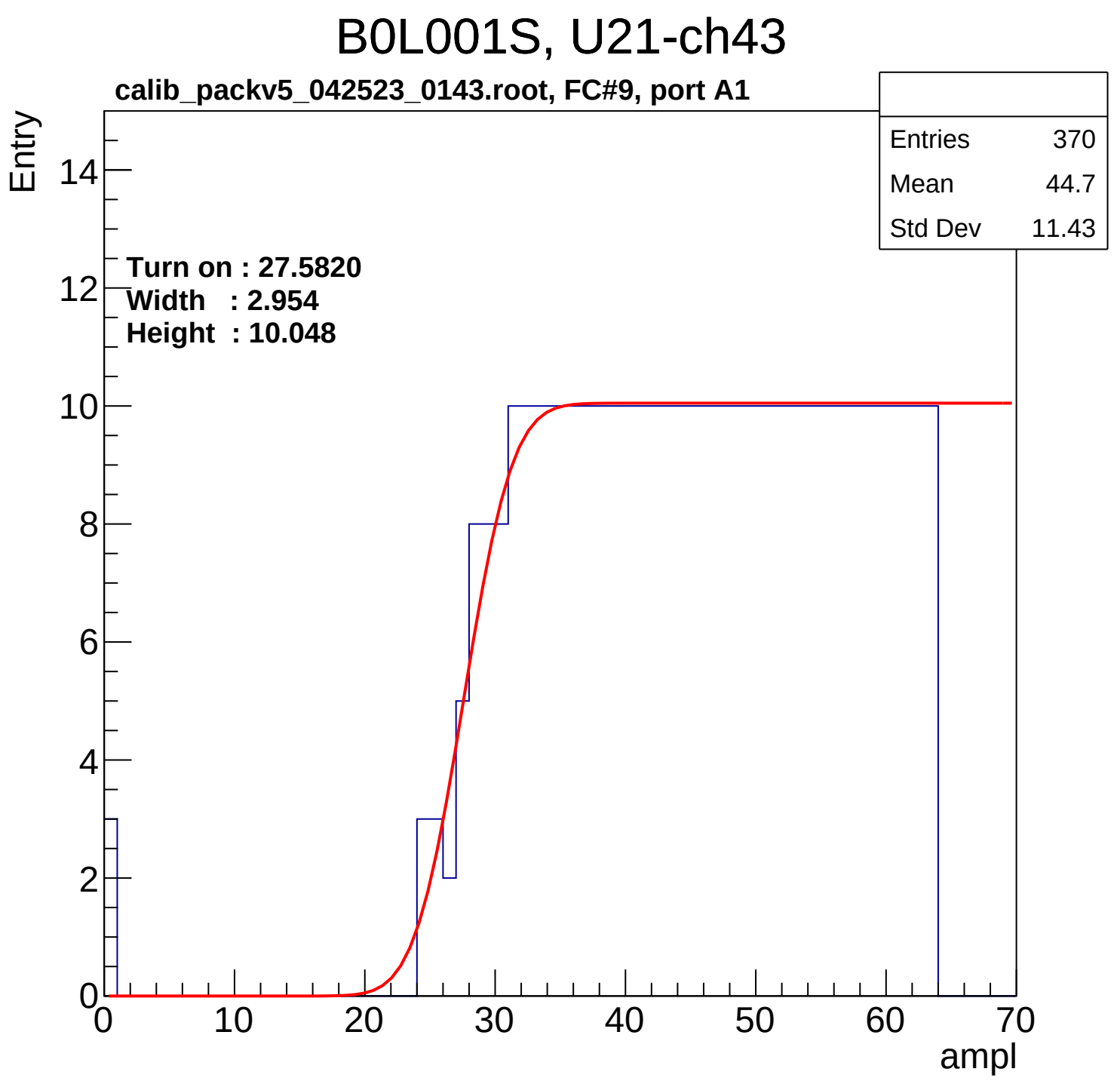
B0L001S, U21-ch43
calib_packv5_042523_0143.root, FC#9, port A1
Entries 370
Mean 44.7
Std Dev 11.43
Turn on : 27.5820
Width : 2.954
Height : 10.048
Entry
ampl
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6
8
10
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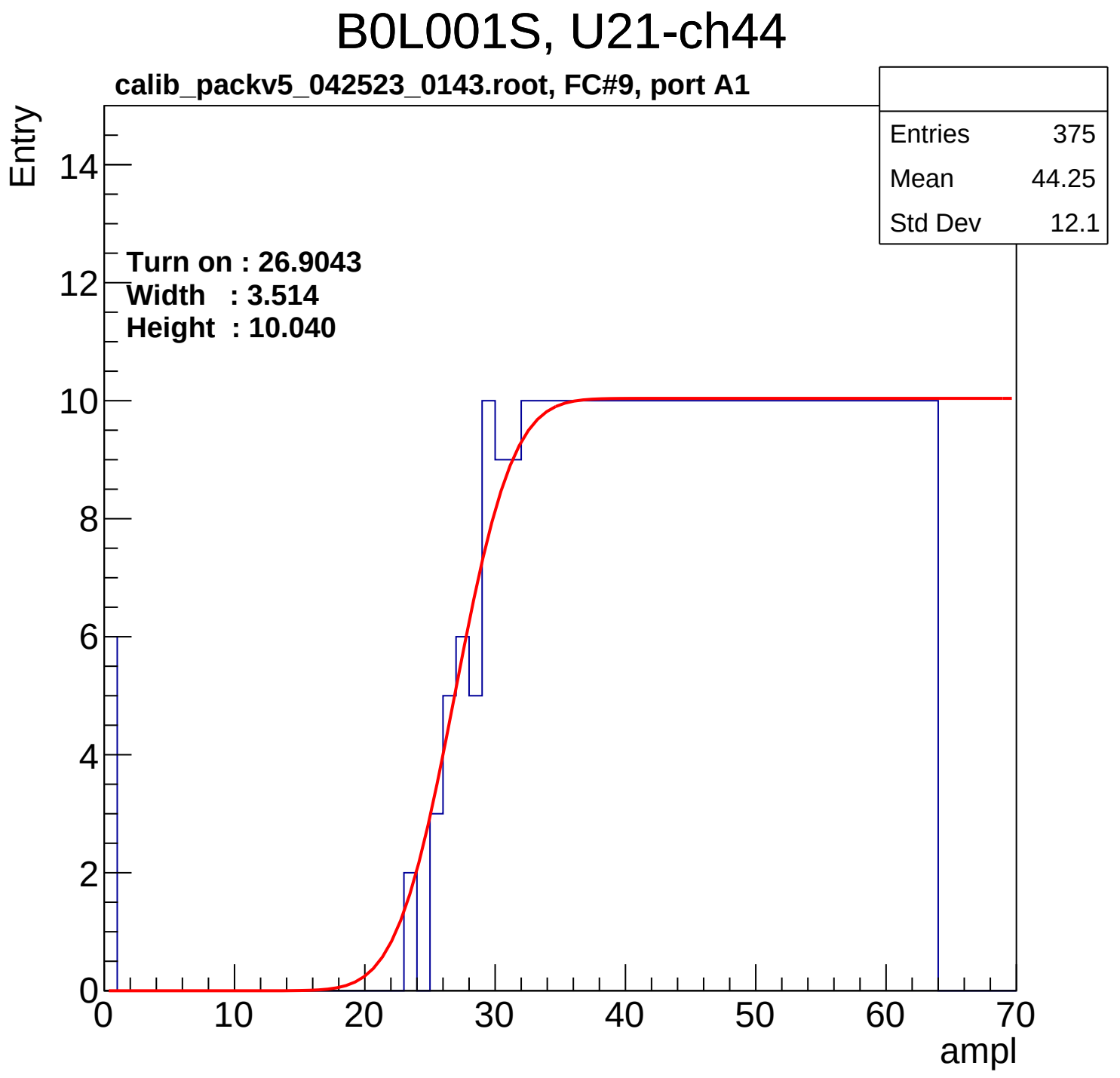
B0L001S, U21-ch44
calib_packv5_042523_0143.root, FC#9, port A1
Entries 375
Mean 44.25
Std Dev 12.1
Turn on : 26.9043
Width : 3.514
Height : 10.040
Entry
ampl
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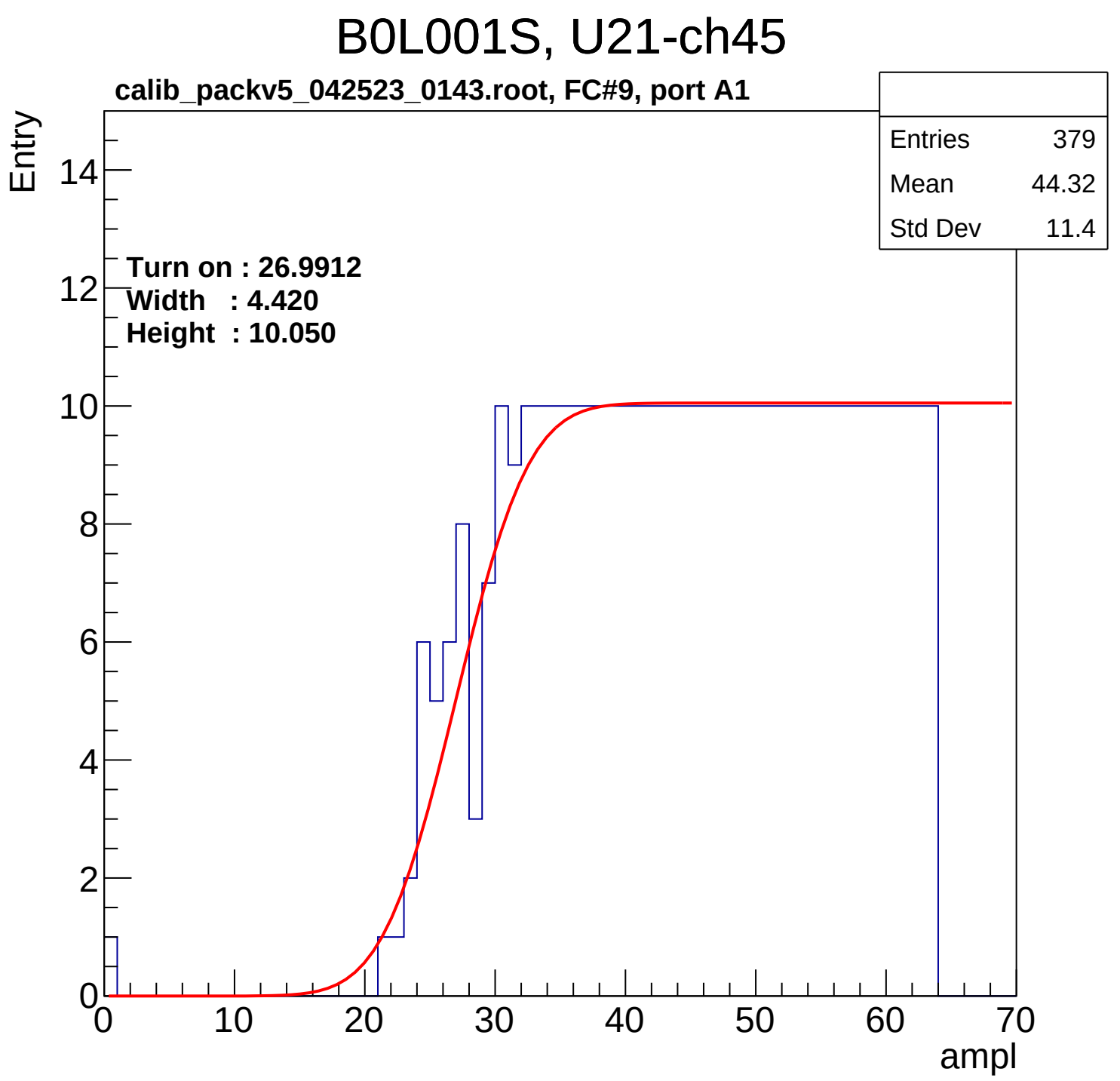
B0L001S, U21-ch45
calib_packv5_042523_0143.root, FC#9, port A1
Entries 379
Mean 44.32
Std Dev 11.4
Turn on : 26.9912
Width : 4.420
Height : 10.050
Entry
ampl
0
2
4
6
8
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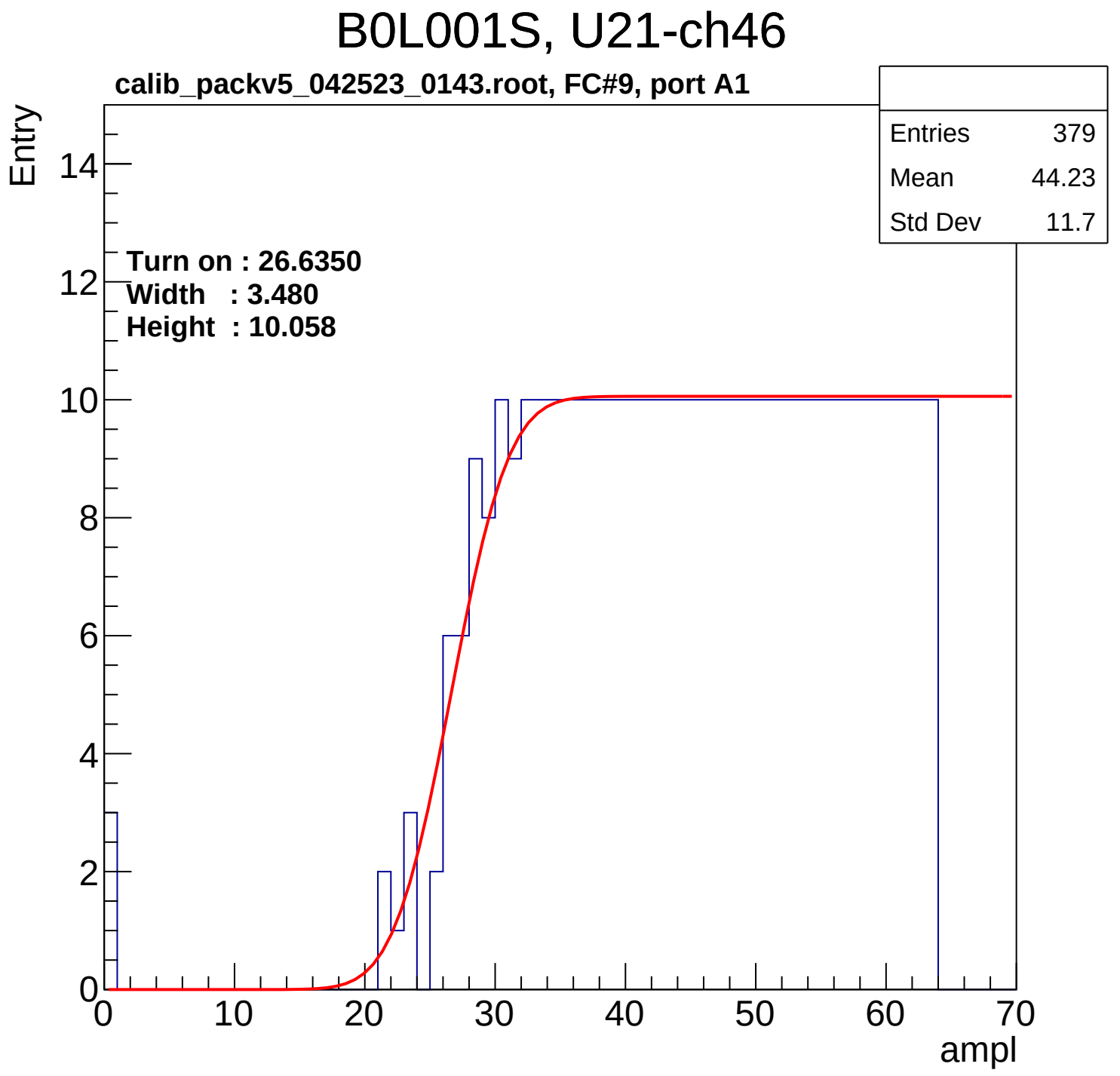
B0L001S, U21-ch46
calib_packv5_042523_0143.root, FC#9, port A1
Entries 379
Mean 44.23
Std Dev 11.7
Turn on : 26.6350
Width : 3.480
Height : 10.058
Entry
ampl
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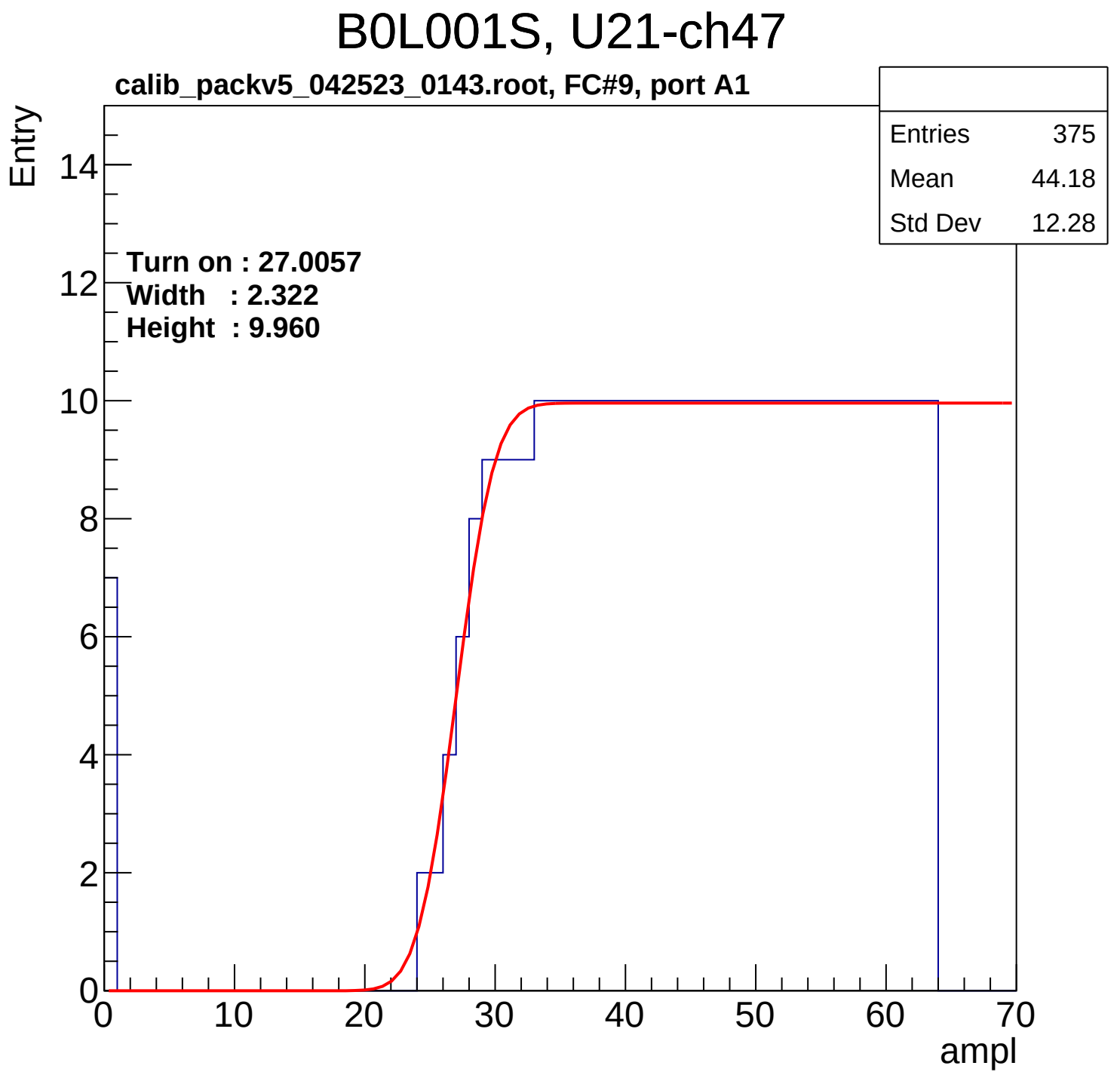
B0L001S, U21-ch47
calib_packv5_042523_0143.root, FC#9, port A1
Entries 375
Mean 44.18
Std Dev 12.28
Turn on : 27.0057
Width : 2.322
Height : 9.960
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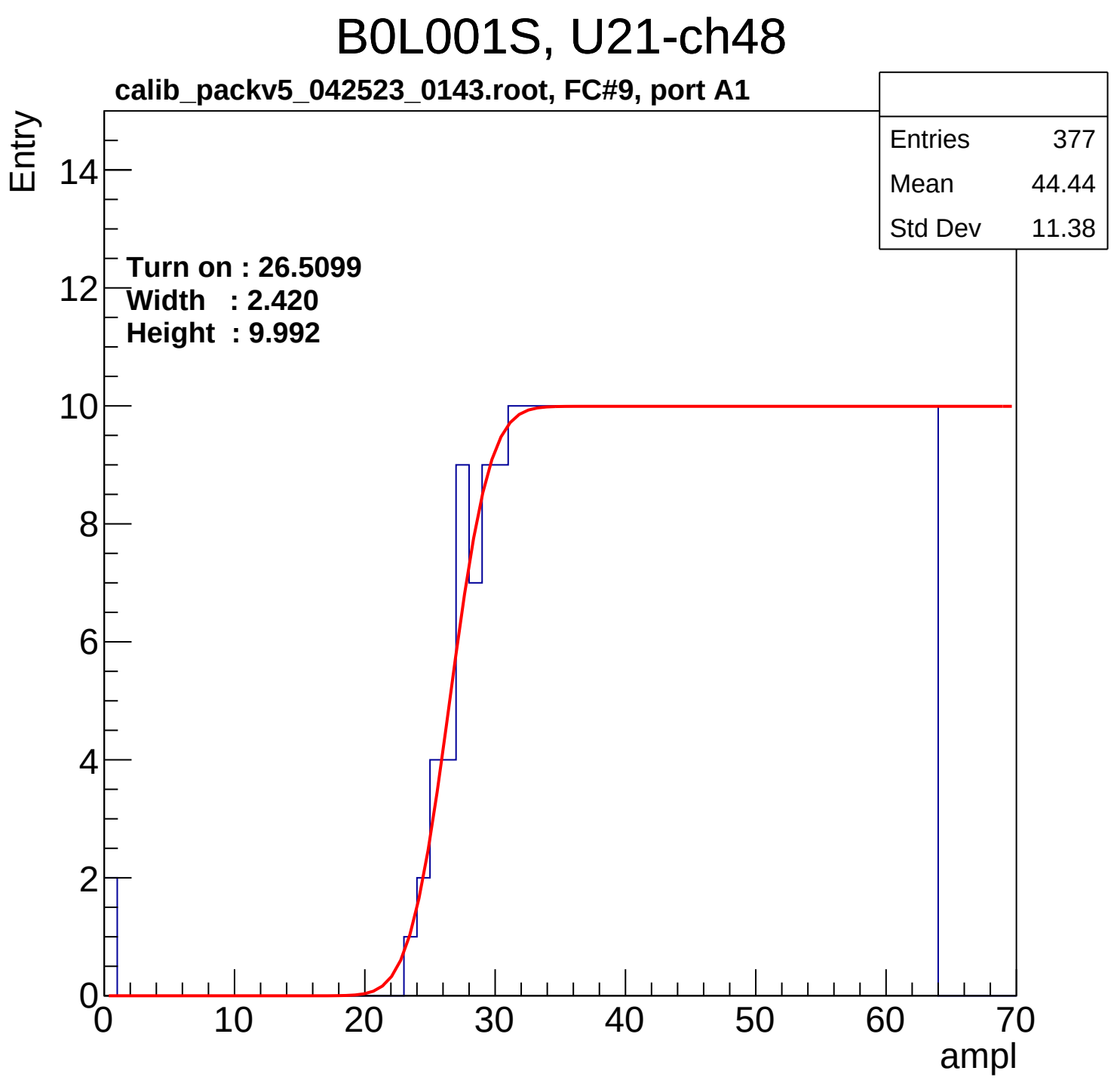
B0L001S, U21-ch48
calib_packv5_042523_0143.root, FC#9, port A1
Entries 377
Mean 44.44
Std Dev 11.38
Turn on : 26.5099
Width : 2.420
Height : 9.992
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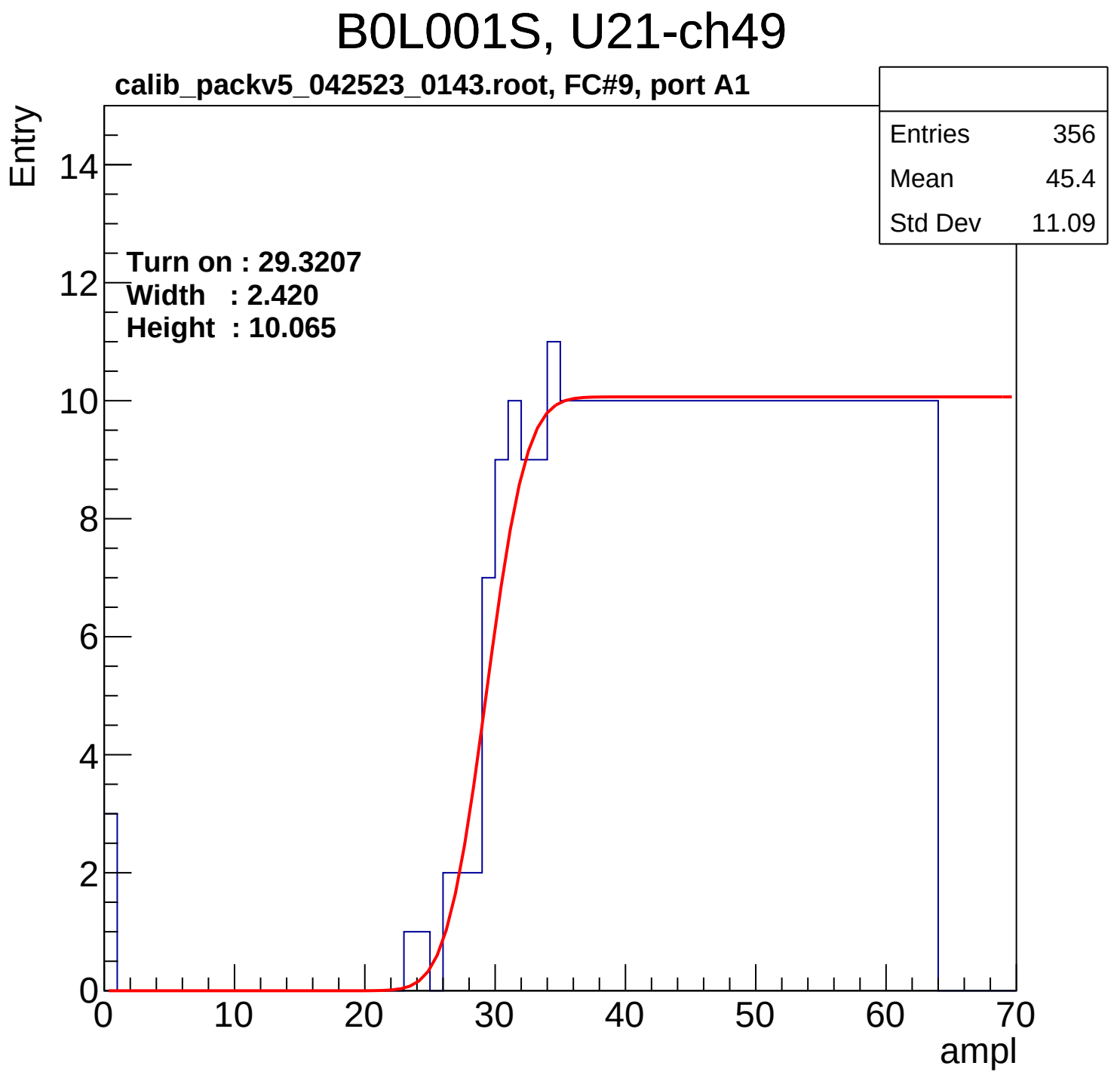
B0L001S, U21-ch49
calib_packv5_042523_0143.root, FC#9, port A1
Entries 356
Mean 45.4
Std Dev 11.09
Turn on : 29.3207
Width : 2.420
Height : 10.065
Entry
ampl
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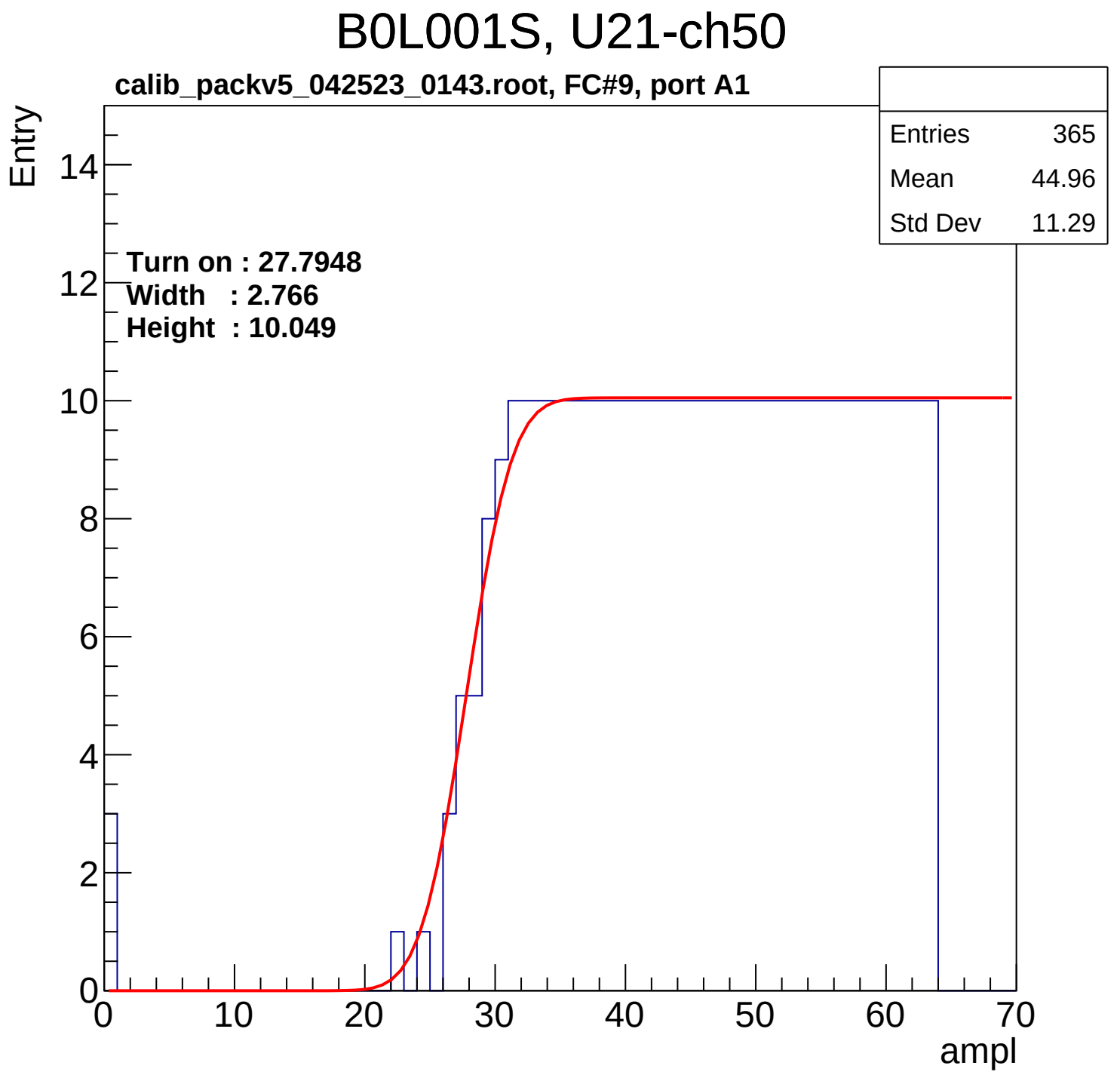
B0L001S, U21-ch50
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 44.96
Std Dev 11.29
Turn on : 27.7948
Width : 2.766
Height : 10.049
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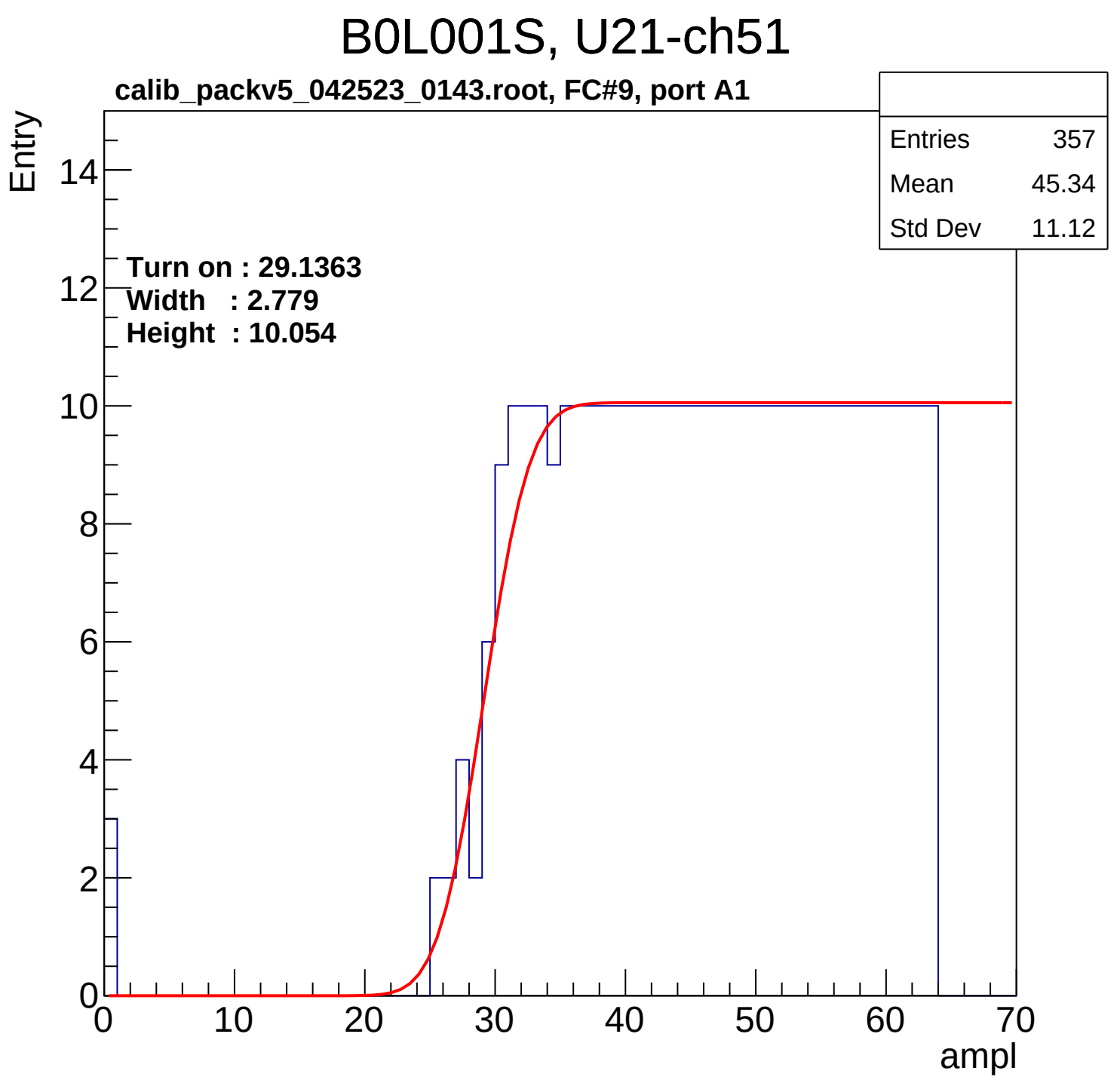
B0L001S, U21-ch51
calib_packv5_042523_0143.root, FC#9, port A1
Entries 357
Mean 45.34
Std Dev 11.12
Turn on : 29.1363
Width : 2.779
Height : 10.054
Entry
ampl
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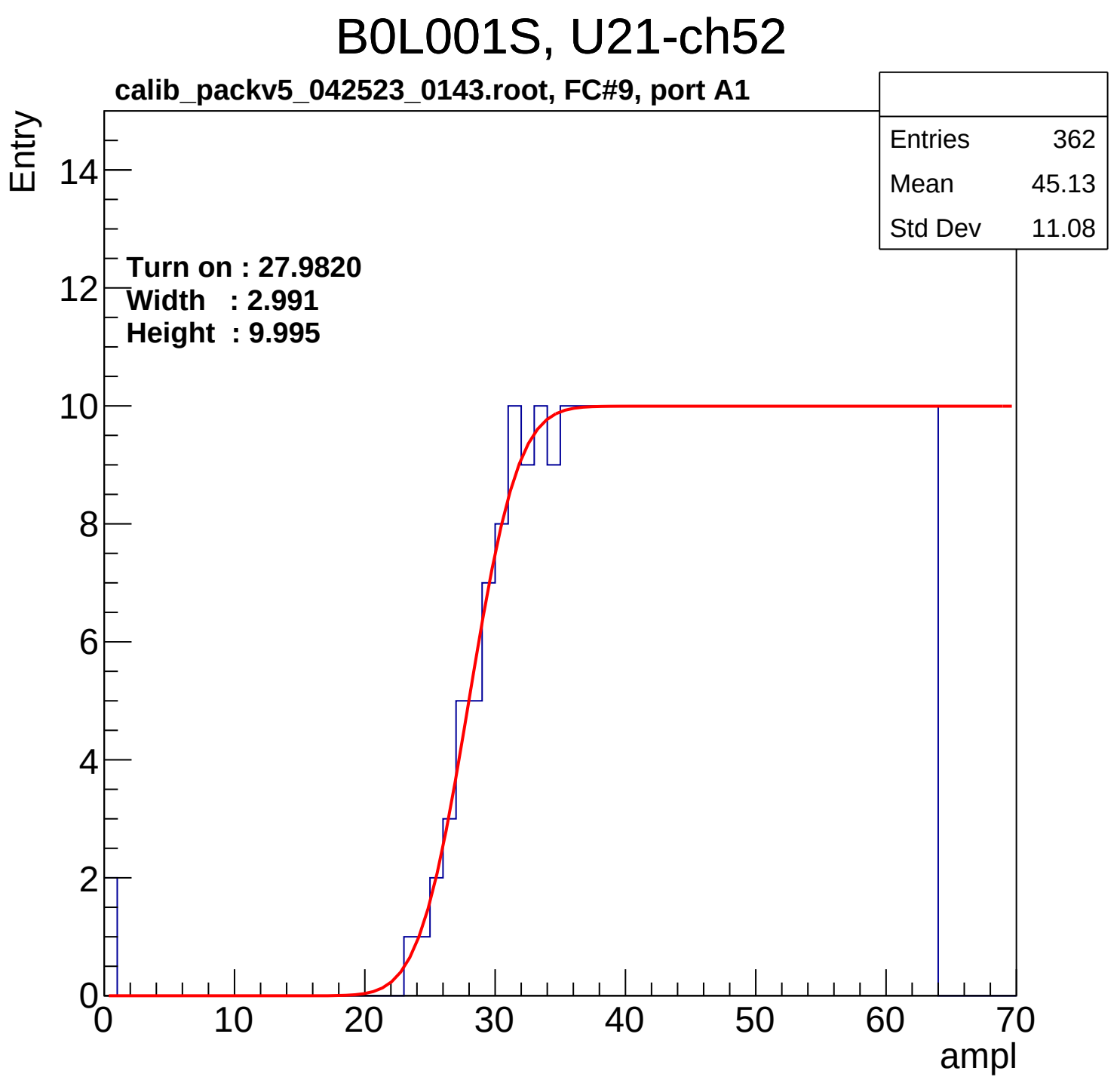
B0L001S, U21-ch52
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 45.13
Std Dev 11.08
Turn on : 27.9820
Width : 2.991
Height : 9.995
Entry
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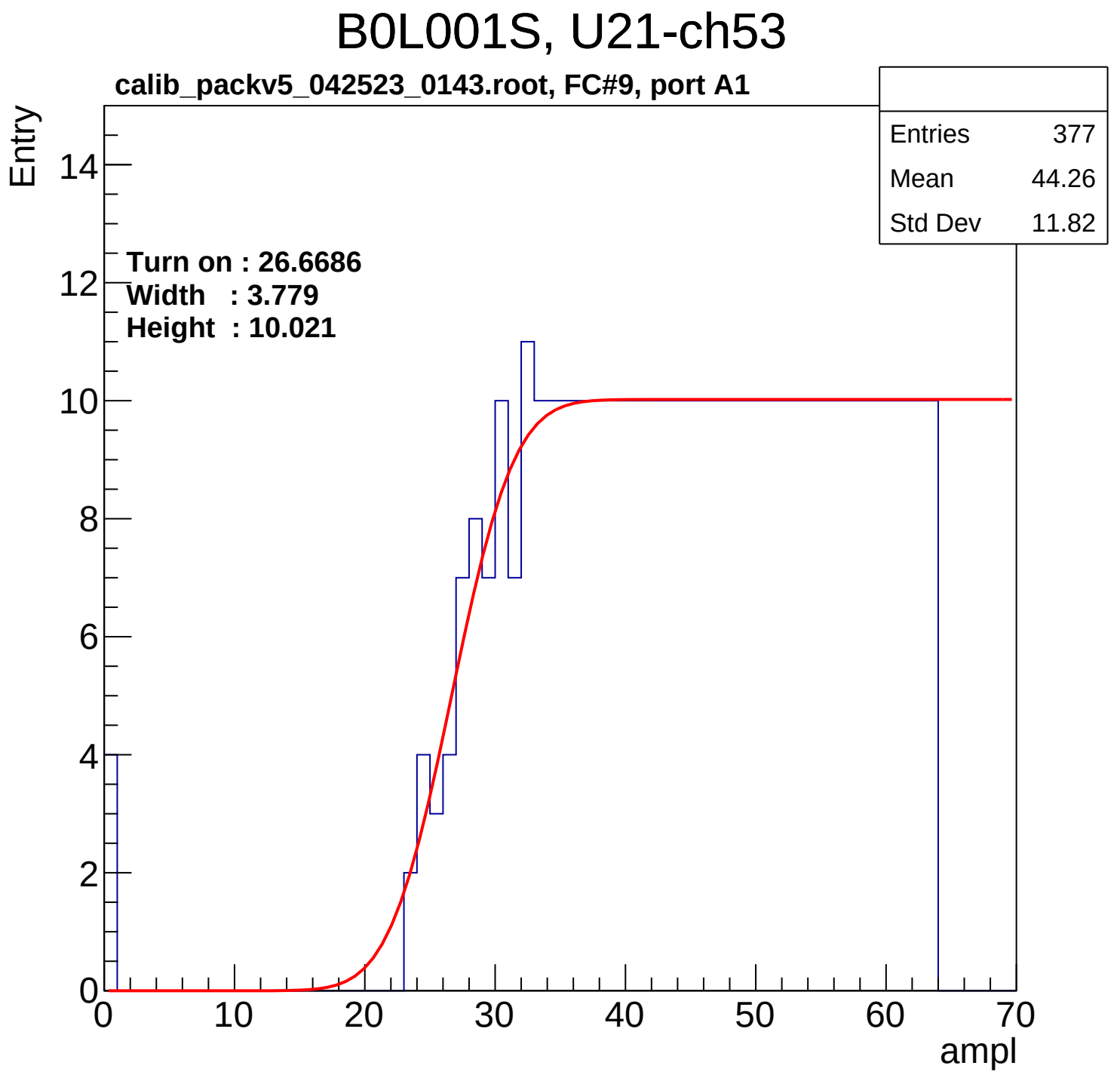
B0L001S, U21-ch53
calib_packv5_042523_0143.root, FC#9, port A1
Entries 377
Mean 44.26
Std Dev 11.82
Turn on : 26.6686
Width : 3.779
Height : 10.021
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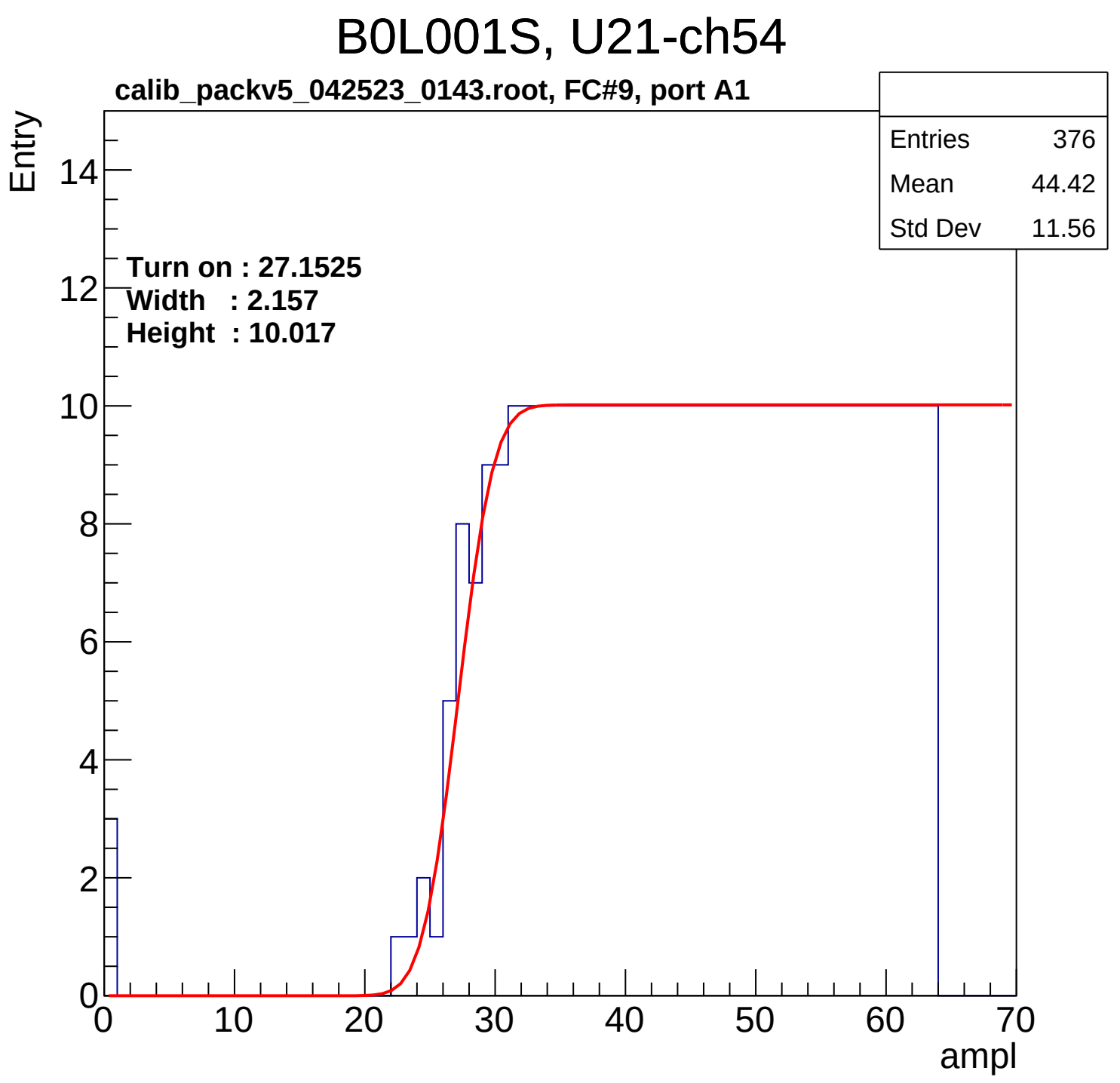
B0L001S, U21-ch54
calib_packv5_042523_0143.root, FC#9, port A1
Entries 376
Mean 44.42
Std Dev 11.56
Turn on : 27.1525
Width : 2.157
Height : 10.017
Entry
ampl
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6
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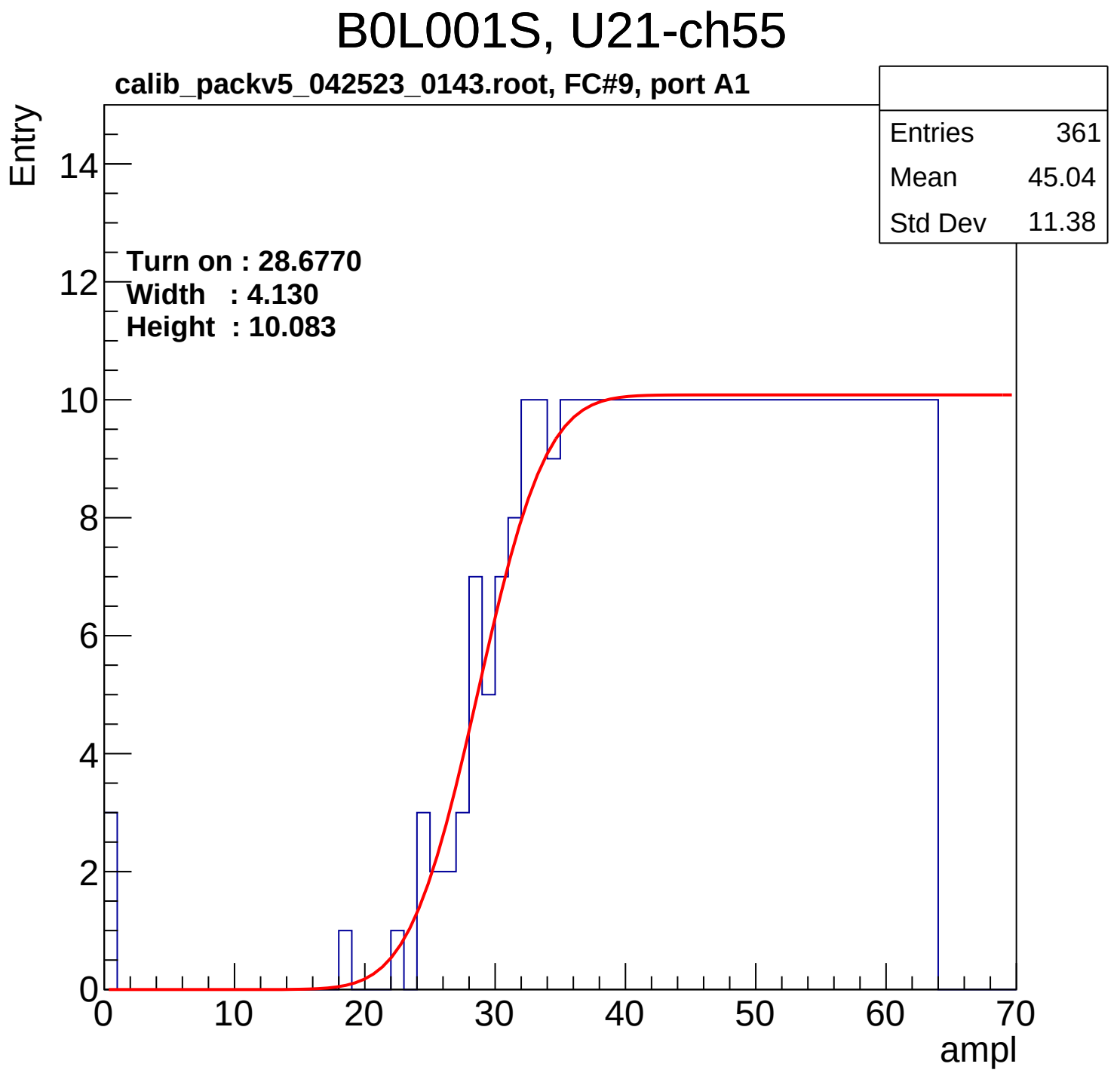
B0L001S, U21-ch55
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 45.04
Std Dev 11.38
Turn on : 28.6770
Width : 4.130
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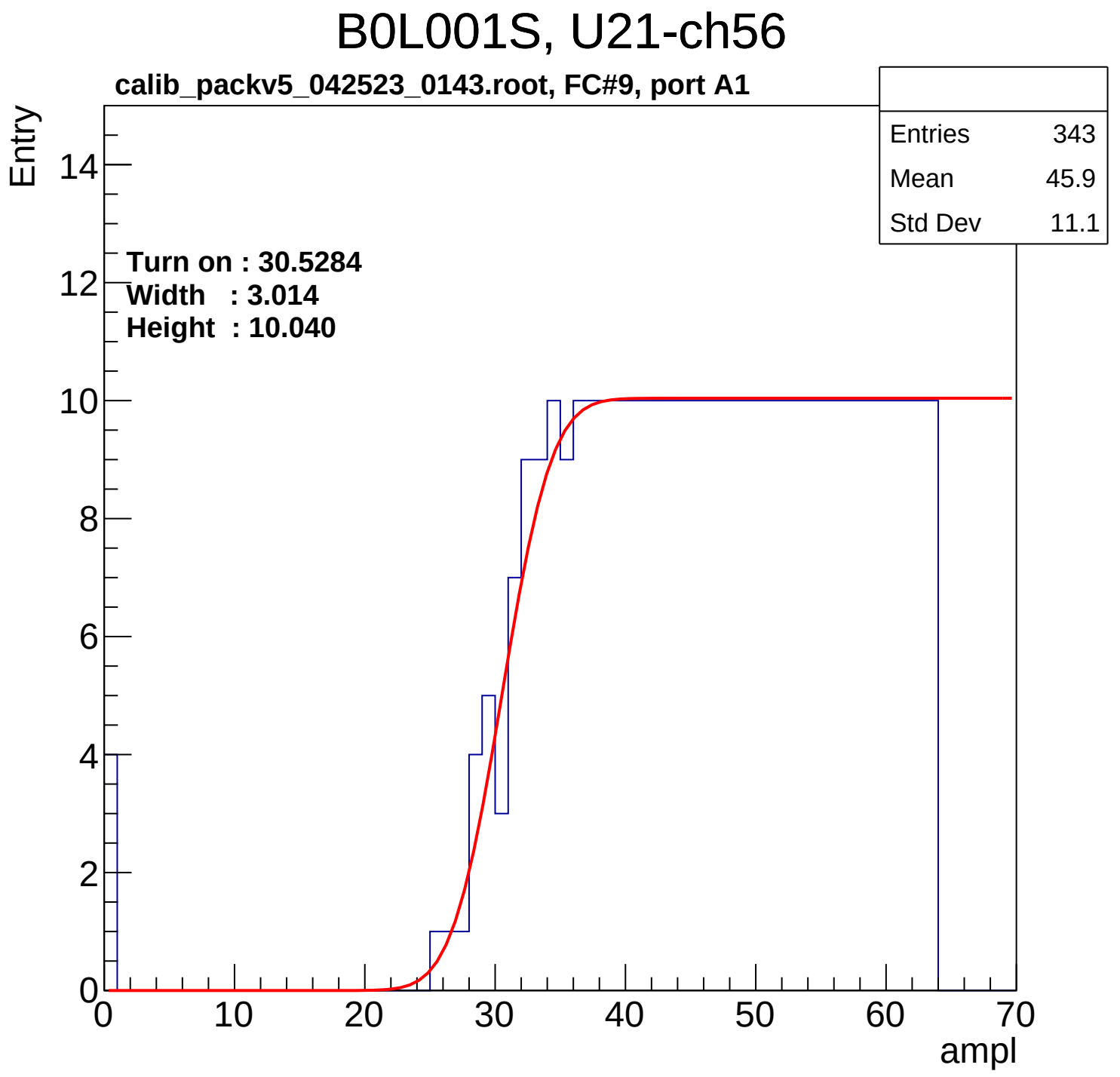
B0L001S, U21-ch56
calib_packv5_042523_0143.root, FC#9, port A1
Entries 343
Mean 45.9
Std Dev 11.1
Turn on : 30.5284
Width : 3.014
Height : 10.040
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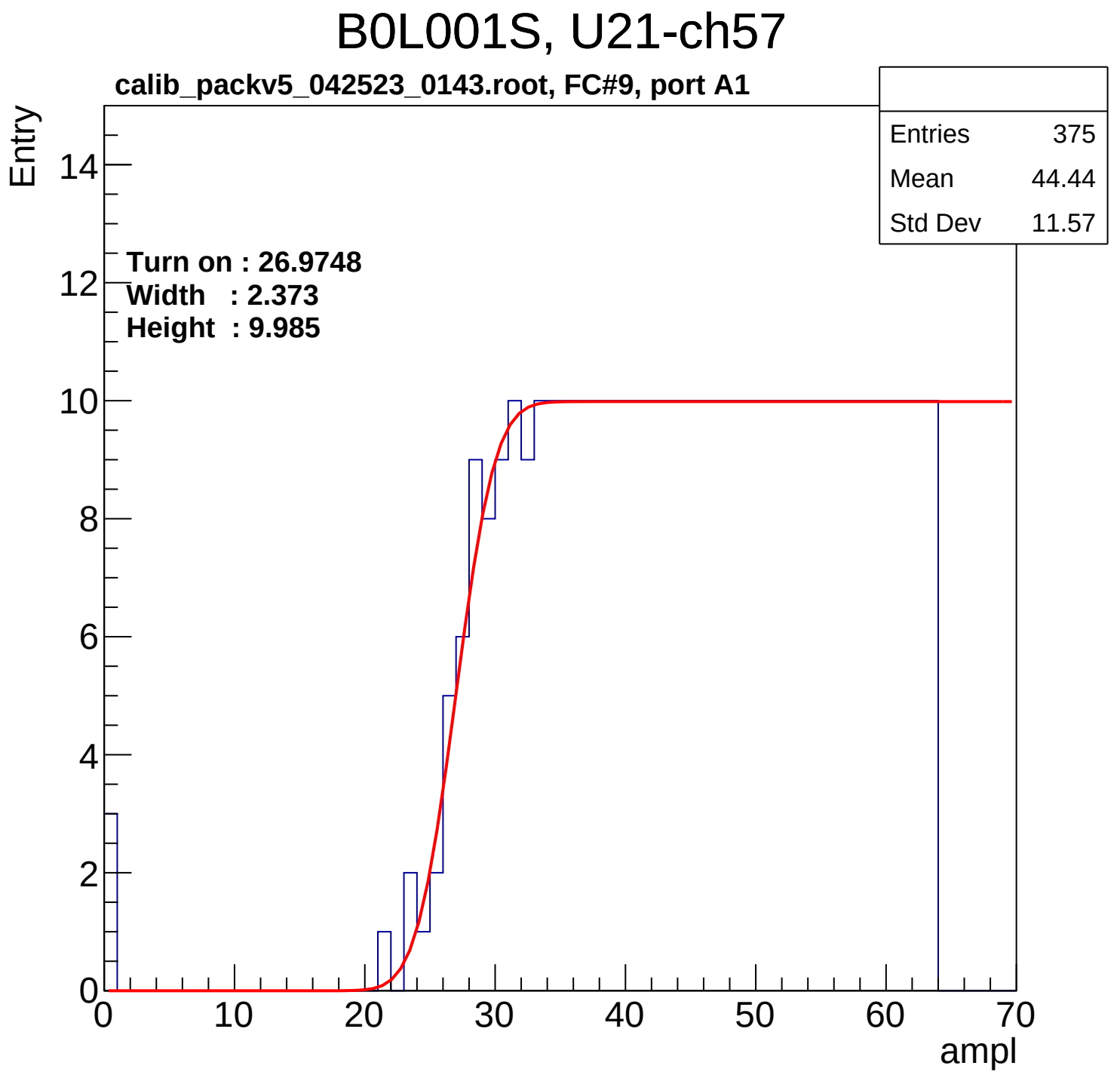
B0L001S, U21-ch57
calib_packv5_042523_0143.root, FC#9, port A1
Entries 375
Mean 44.44
Std Dev 11.57
Turn on : 26.9748
Width : 2.373
Height : 9.985
Entry
ampl
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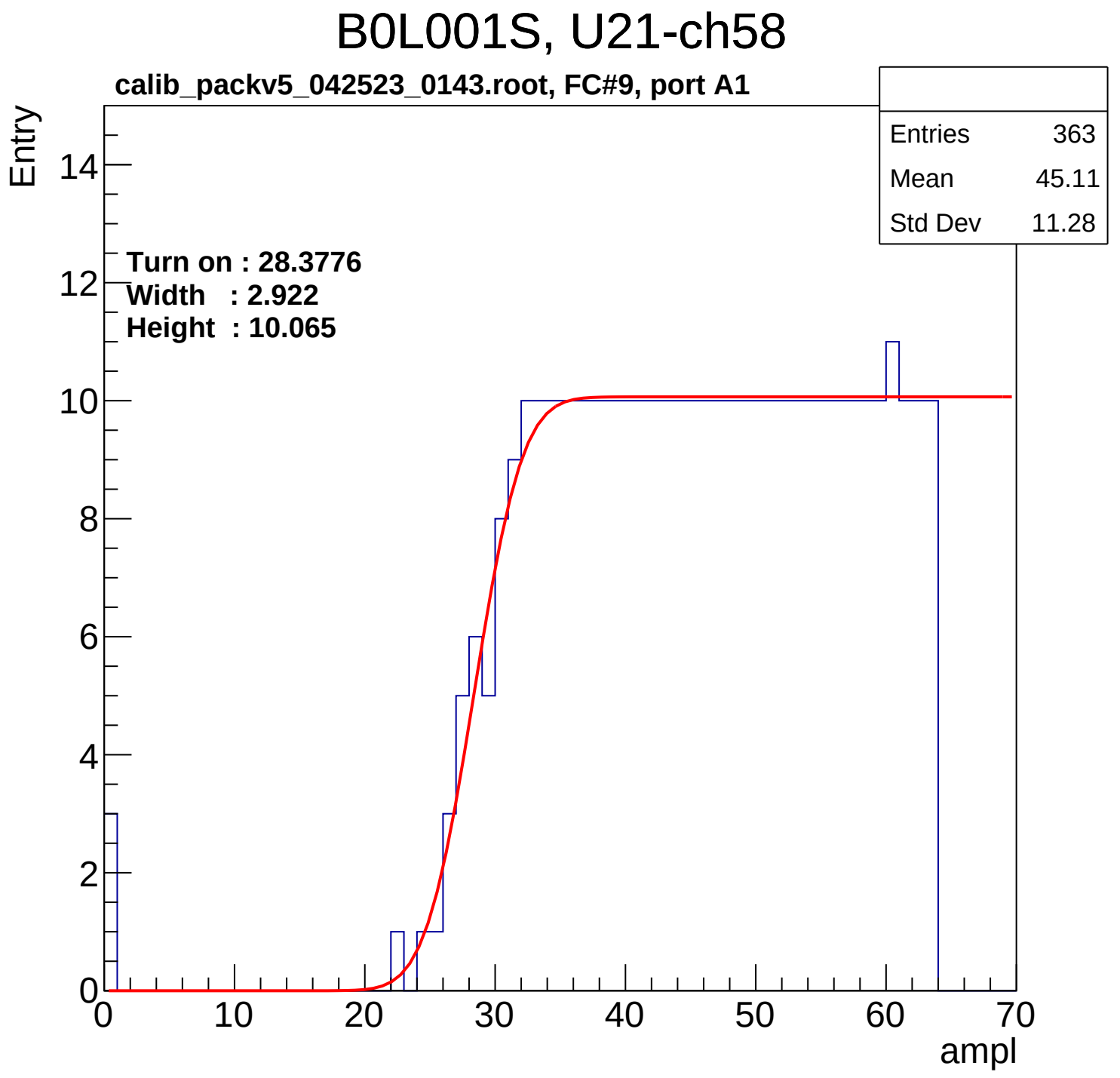
B0L001S, U21-ch58
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 45.11
Std Dev 11.28
Turn on : 28.3776
Width : 2.922
Height : 10.065
Entry
ampl
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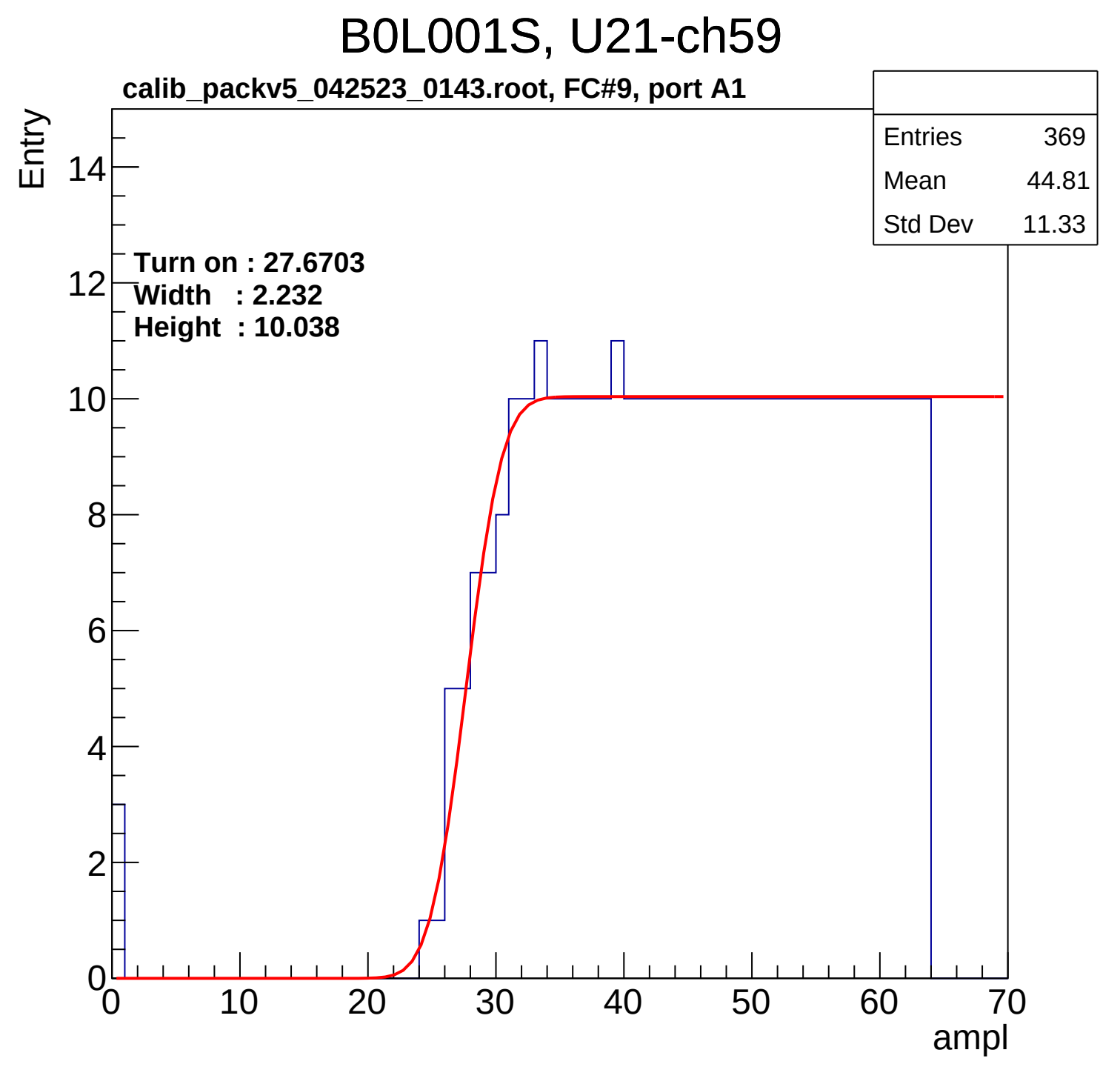
B0L001S, U21-ch59
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.81
Std Dev 11.33
Turn on : 27.6703
Width : 2.232
Height : 10.038
Entry
ampl
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2
4
6
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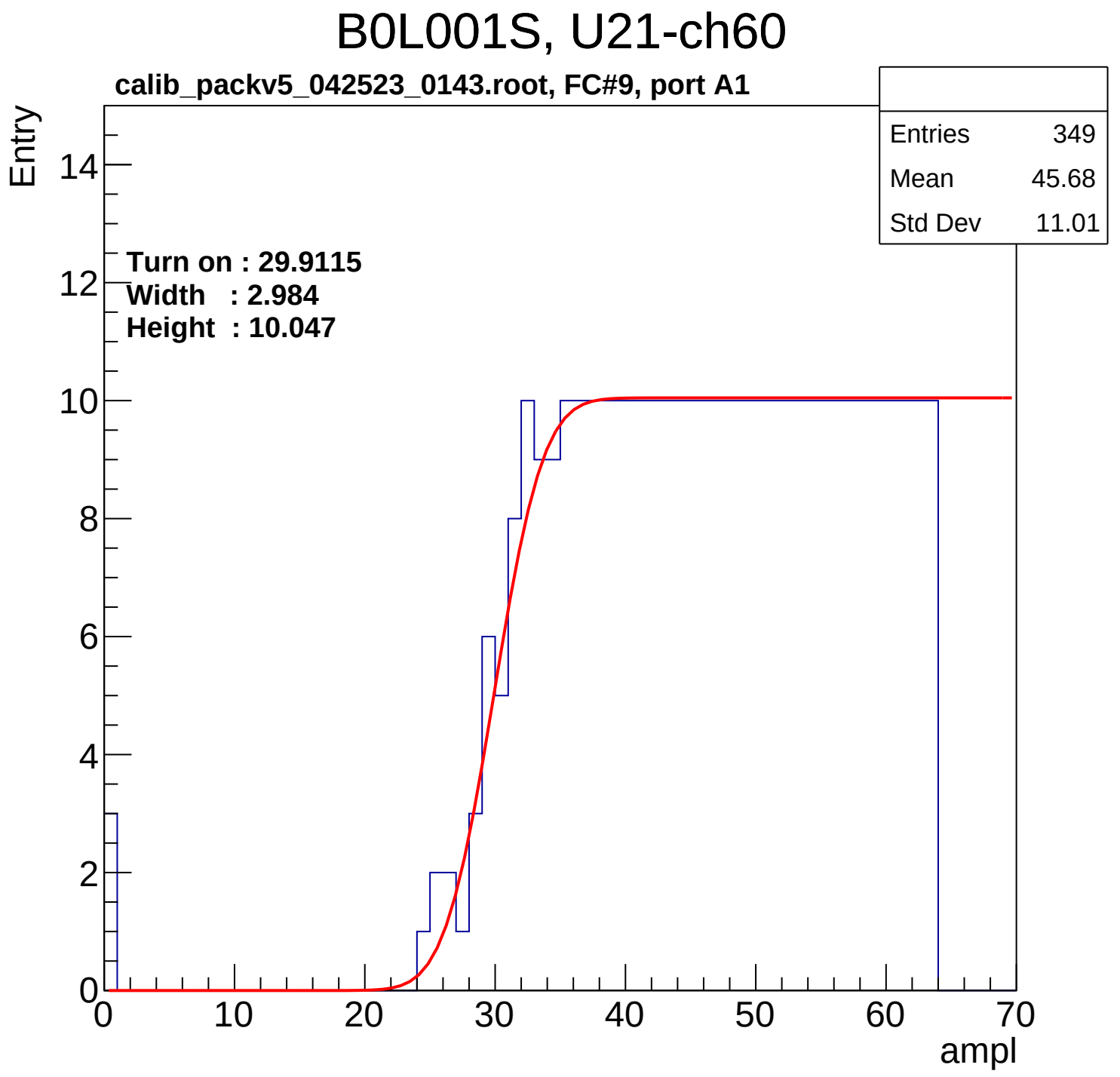
B0L001S, U21-ch60
calib_packv5_042523_0143.root, FC#9, port A1
Entries 349
Mean 45.68
Std Dev 11.01
Turn on : 29.9115
Width : 2.984
Height : 10.047
Entry
ampl
0
2
4
6
8
10
12
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0
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40
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60
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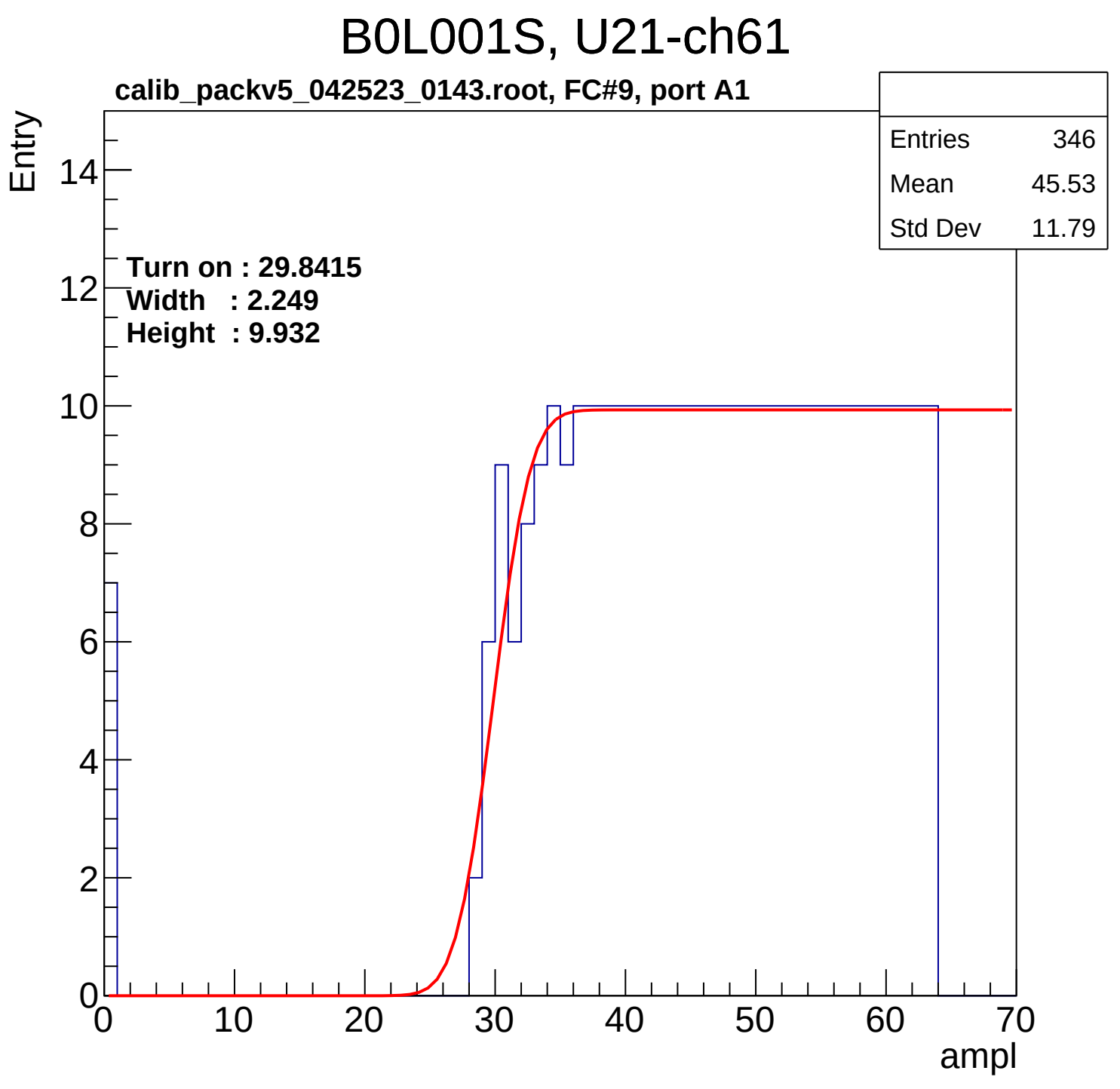
B0L001S, U21-ch61
calib_packv5_042523_0143.root, FC#9, port A1
Entries 346
Mean 45.53
Std Dev 11.79
Turn on : 29.8415
Width : 2.249
Height : 9.932
Entry
ampl
0
2
4
6
8
10
12
14
0
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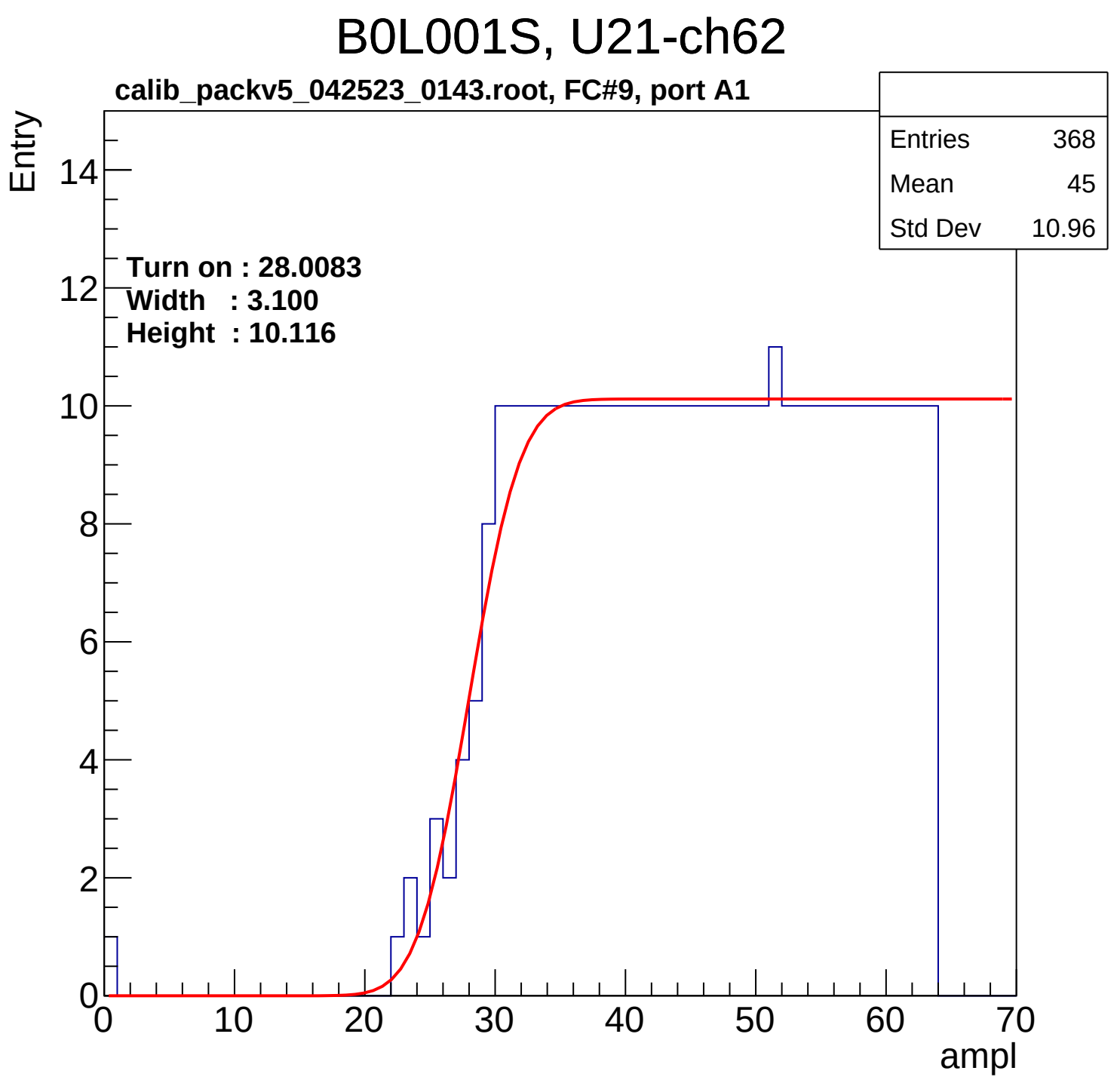
B0L001S, U21-ch62
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 45
Std Dev 10.96
Turn on : 28.0083
Width : 3.100
Height : 10.116
Entry
ampl
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2
4
6
8
10
12
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0
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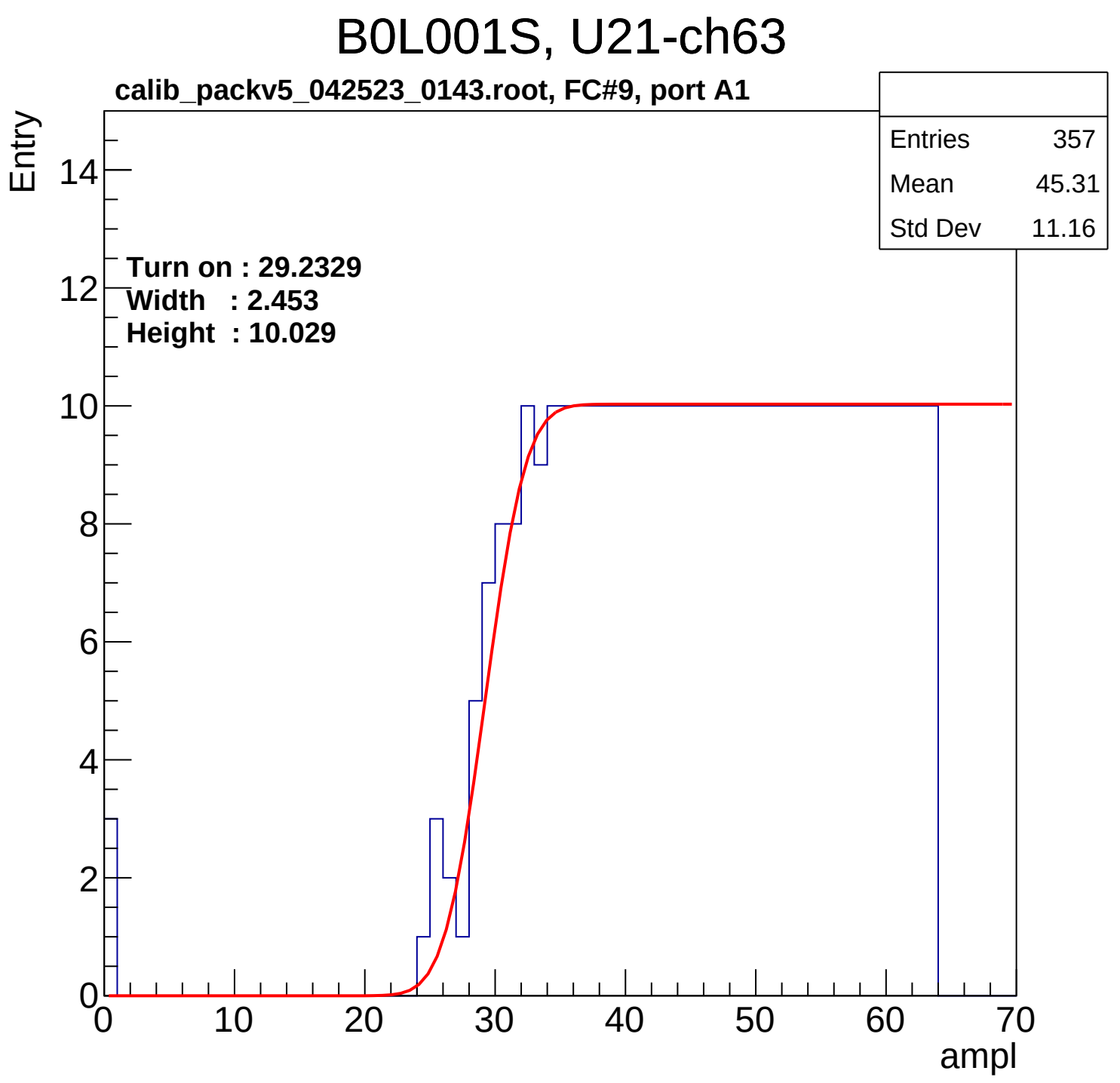
B0L001S, U21-ch63
calib_packv5_042523_0143.root, FC#9, port A1
Entries 357
Mean 45.31
Std Dev 11.16
Turn on : 29.2329
Width : 2.453
Height : 10.029
Entry
ampl
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2
4
6
8
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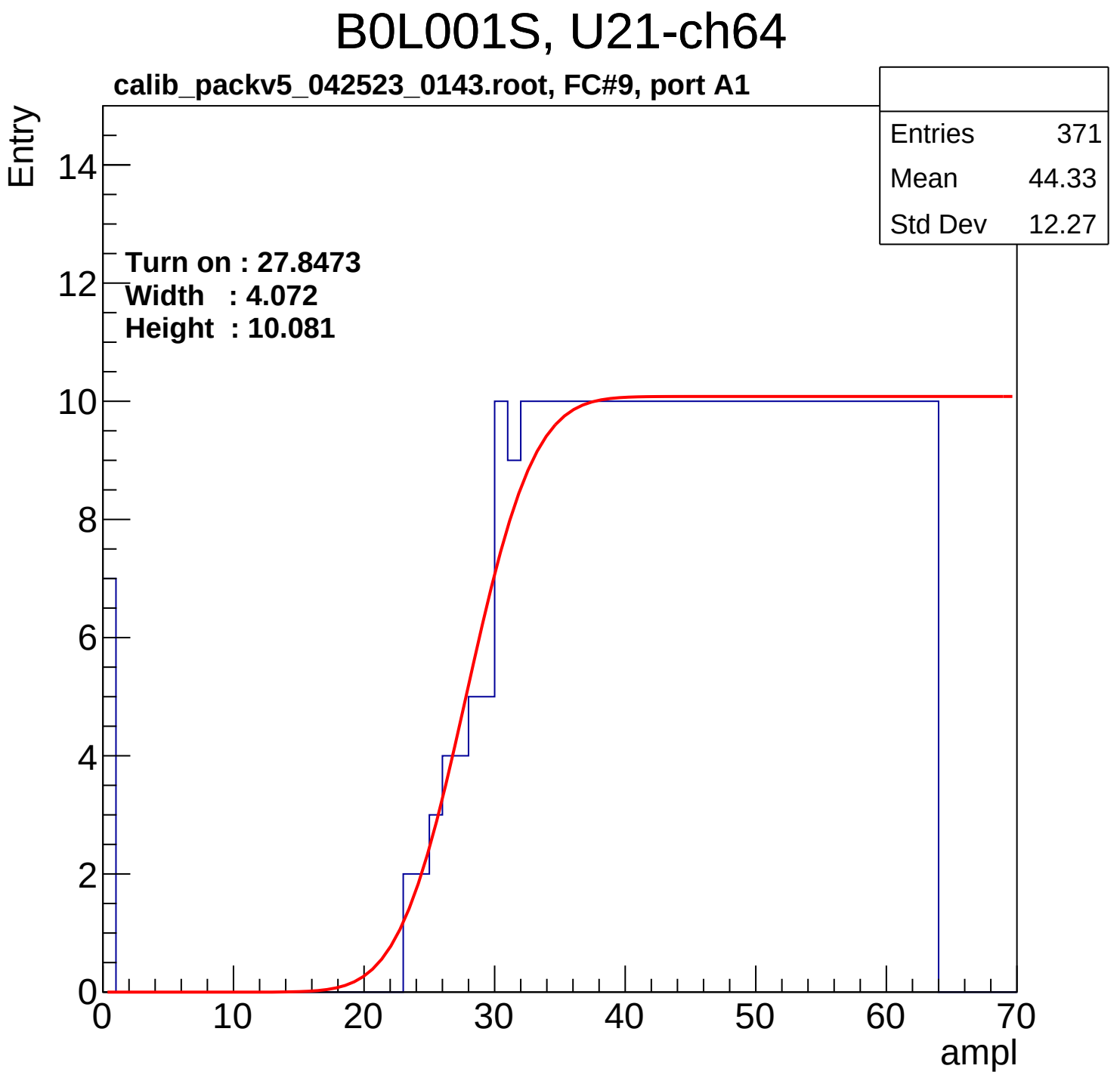
B0L001S, U21-ch64
calib_packv5_042523_0143.root, FC#9, port A1
Entries 371
Mean 44.33
Std Dev 12.27
Turn on : 27.8473
Width : 4.072
Height : 10.081
Entry
ampl
0
2
4
6
8
10
12
14
0
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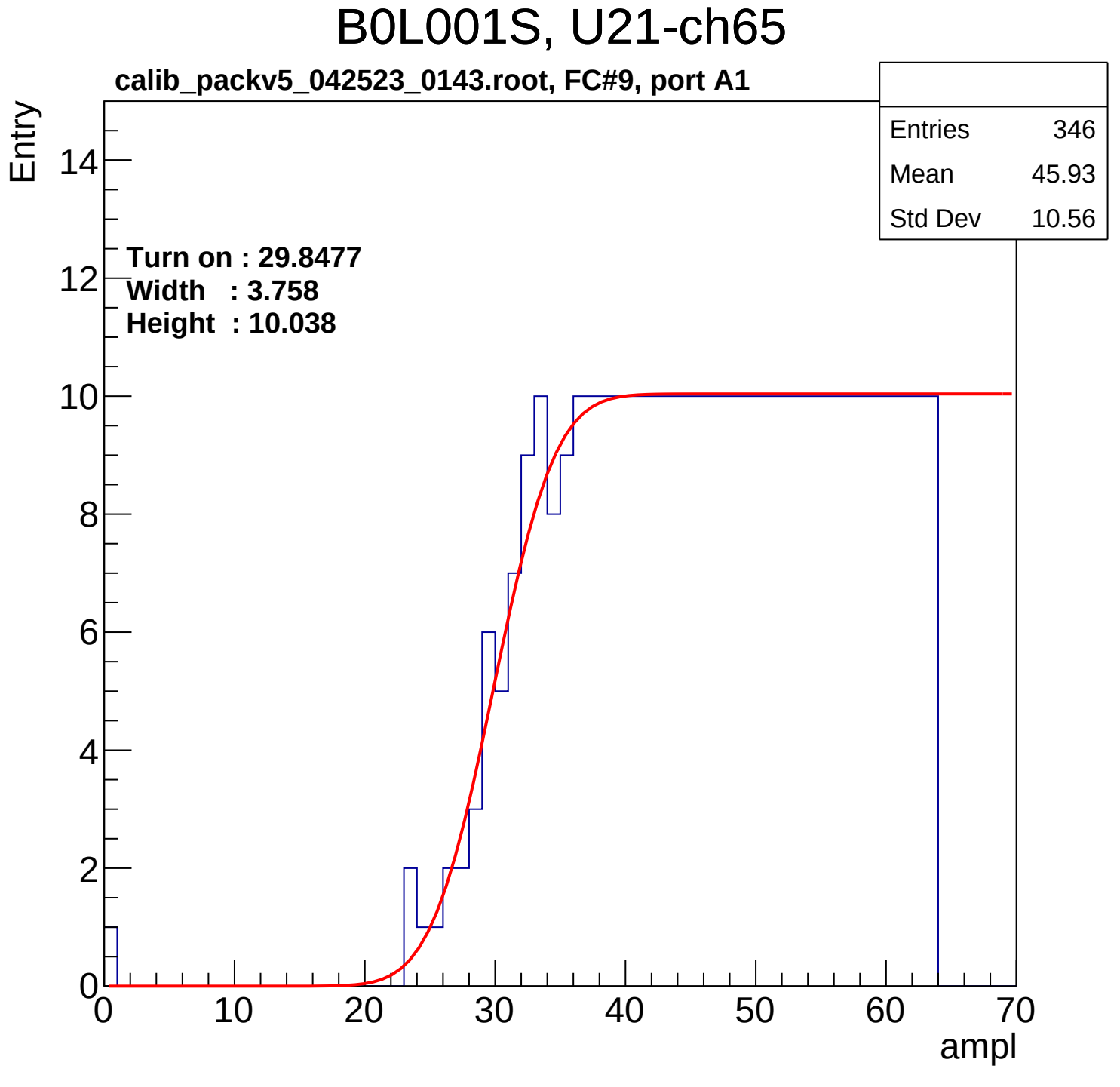
B0L001S, U21-ch65
calib_packv5_042523_0143.root, FC#9, port A1
Entries 346
Mean 45.93
Std Dev 10.56
Turn on : 29.8477
Width : 3.758
Height : 10.038
Entry
ampl
0
2
4
6
8
10
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14
0
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20
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40
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60
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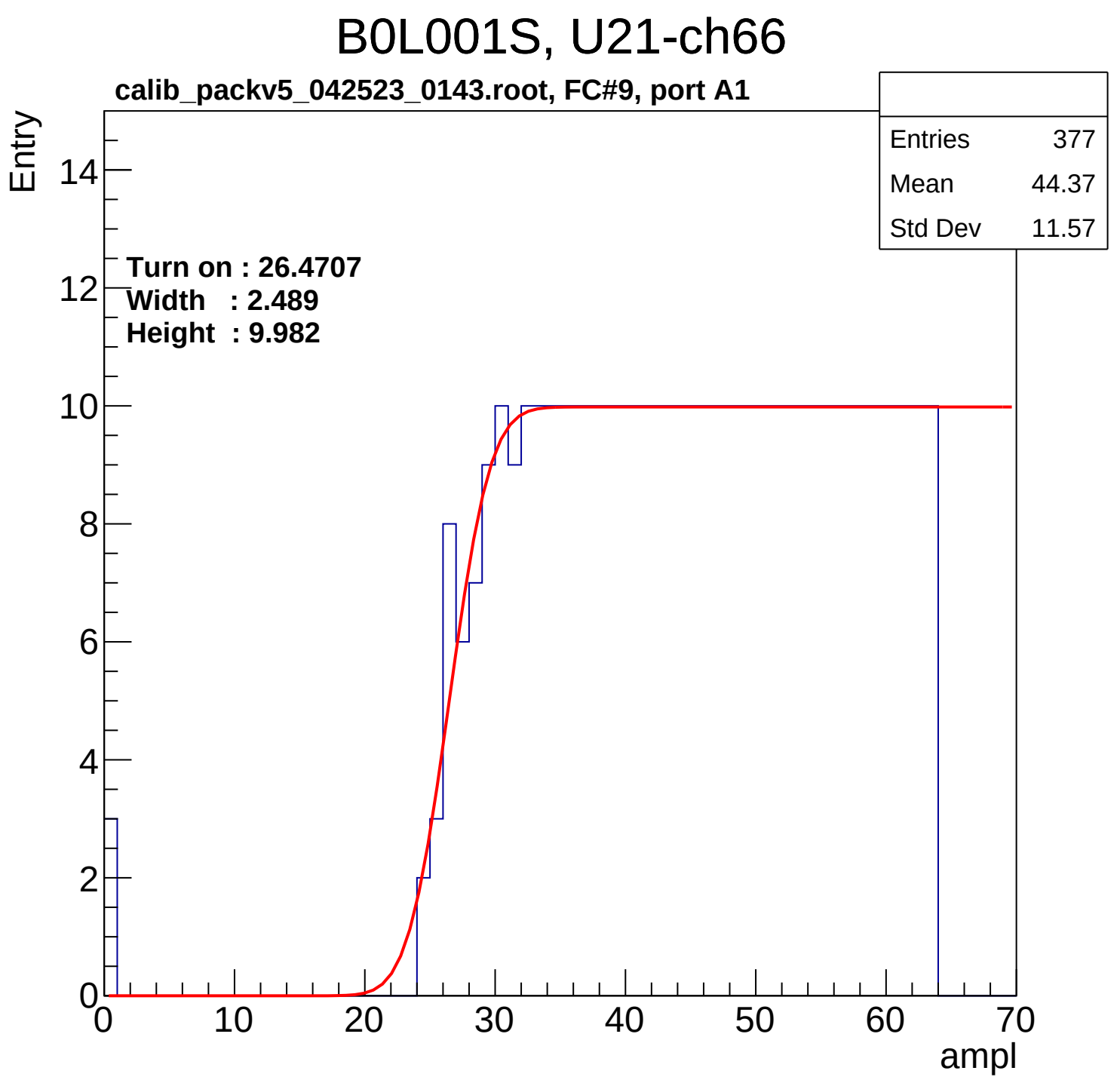
B0L001S, U21-ch66
calib_packv5_042523_0143.root, FC#9, port A1
Entries 377
Mean 44.37
Std Dev 11.57
Turn on : 26.4707
Width : 2.489
Height : 9.982
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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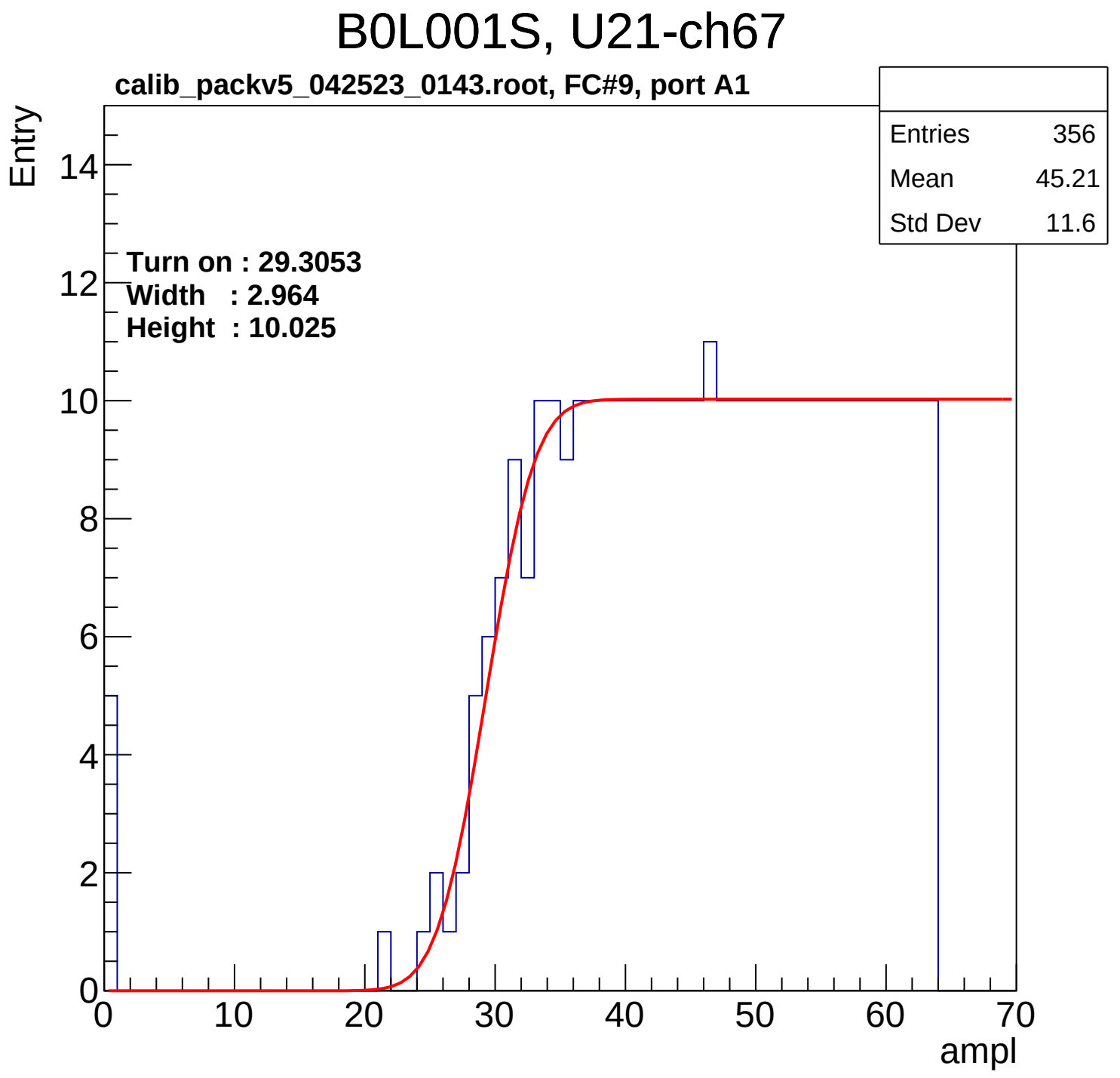
B0L001S, U21-ch67
calib_packv5_042523_0143.root, FC#9, port A1
Entries 356
Mean 45.21
Std Dev 11.6
Turn on : 29.3053
Width : 2.964
Height : 10.025
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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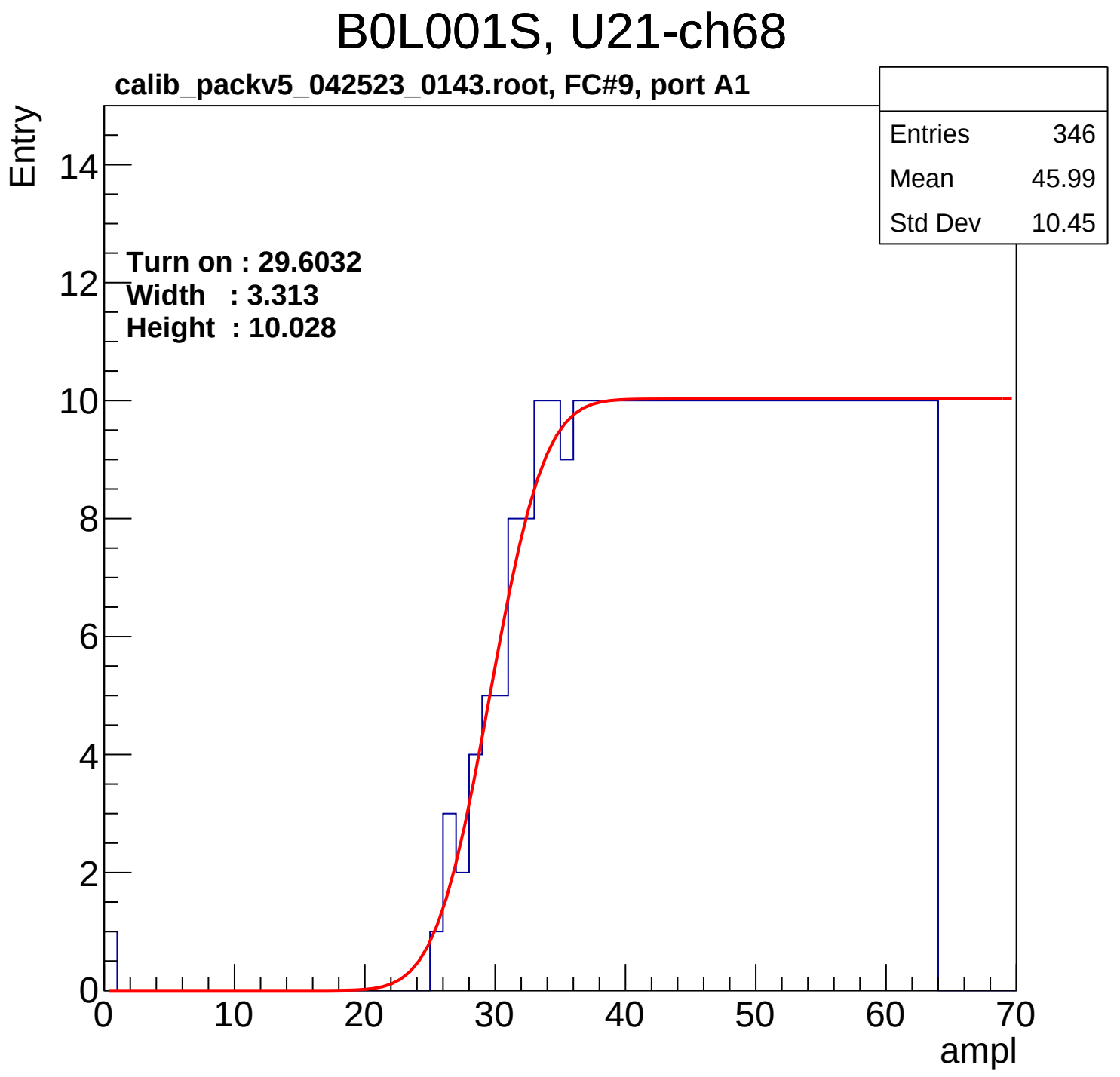
B0L001S, U21-ch68
calib_packv5_042523_0143.root, FC#9, port A1
Entries 346
Mean 45.99
Std Dev 10.45
Turn on : 29.6032
Width : 3.313
Height : 10.028
Entry
ampl
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4
6
8
10
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0
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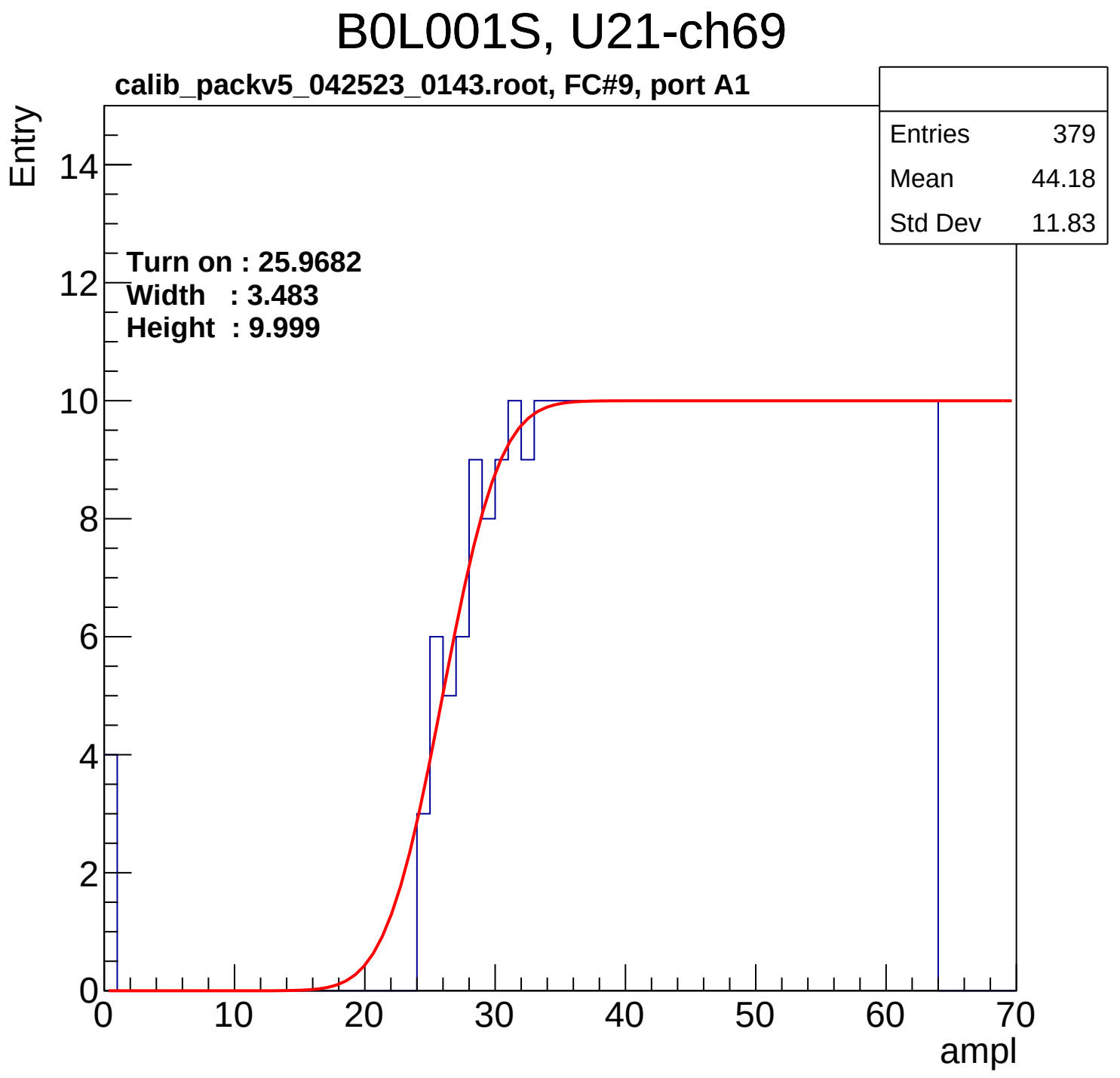
B0L001S, U21-ch69
calib_packv5_042523_0143.root, FC#9, port A1
Entries 379
Mean 44.18
Std Dev 11.83
Turn on : 25.9682
Width : 3.483
Height : 9.999
Entry
ampl
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2
4
6
8
10
12
14
0
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20
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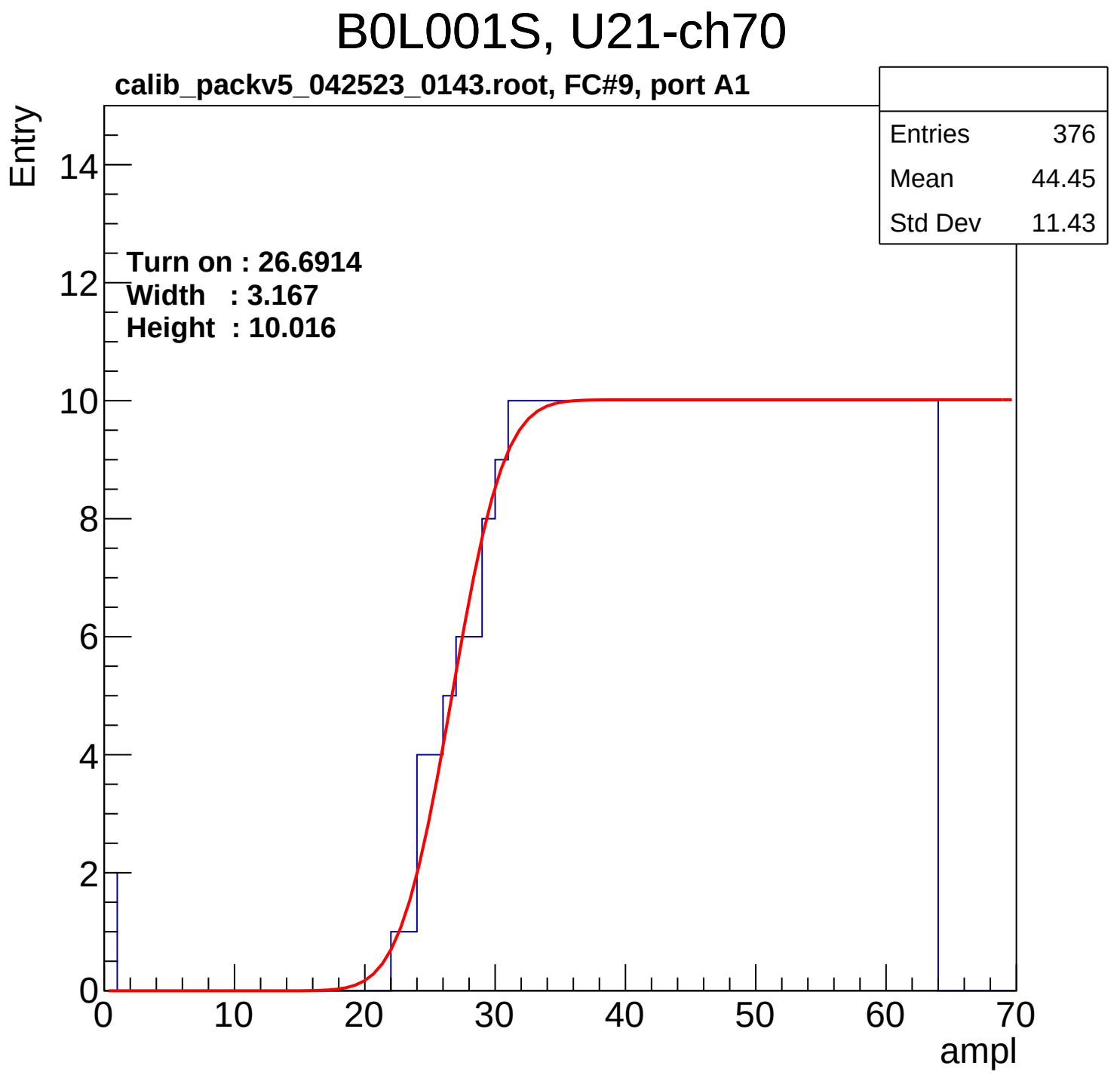
B0L001S, U21-ch70
calib_packv5_042523_0143.root, FC#9, port A1
Entries 376
Mean 44.45
Std Dev 11.43
Turn on : 26.6914
Width : 3.167
Height : 10.016
Entry
ampl
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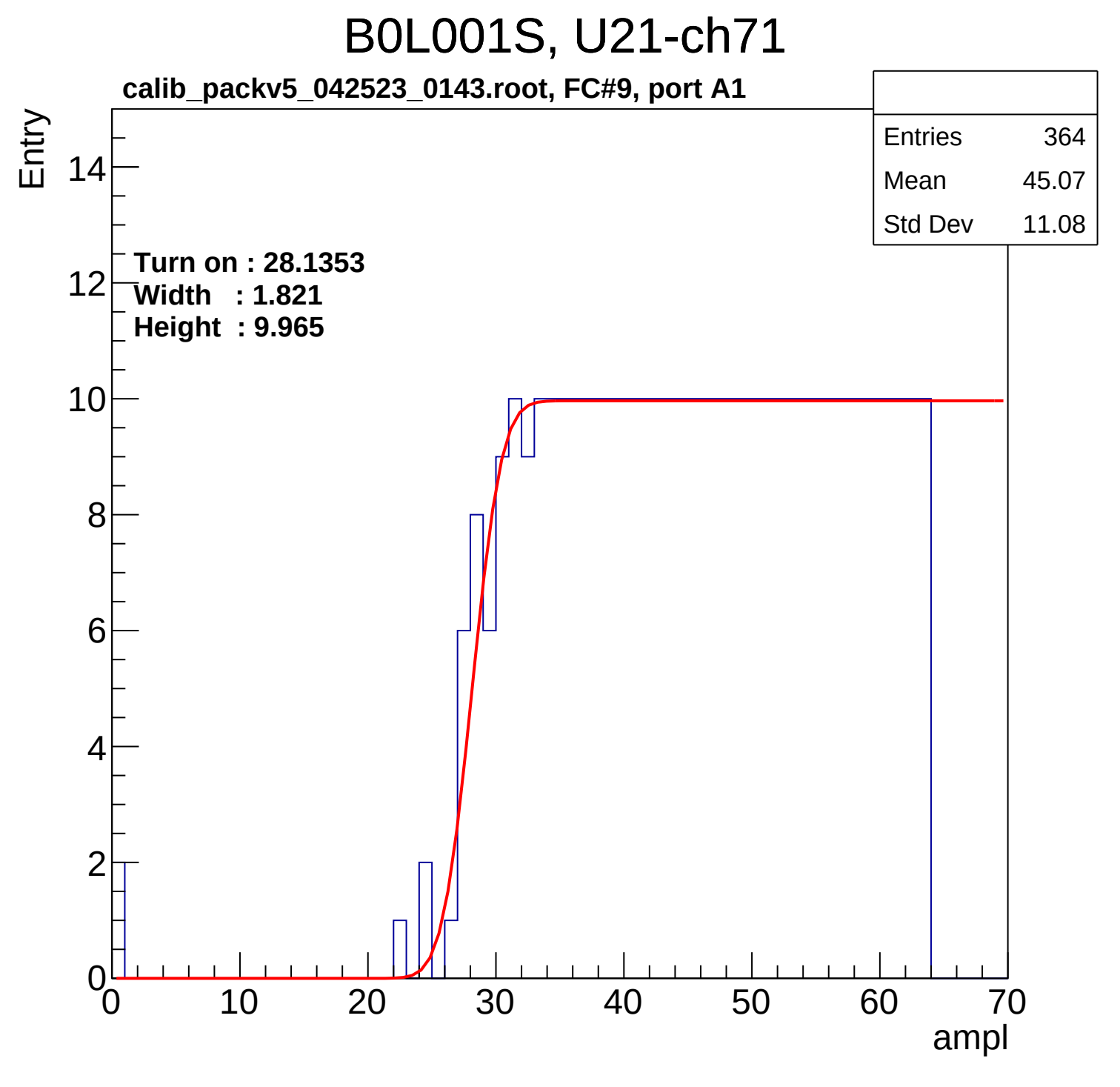
B0L001S, U21-ch71
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 45.07
Std Dev 11.08
Turn on : 28.1353
Width : 1.821
Height : 9.965
Entry
ampl
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2
4
6
8
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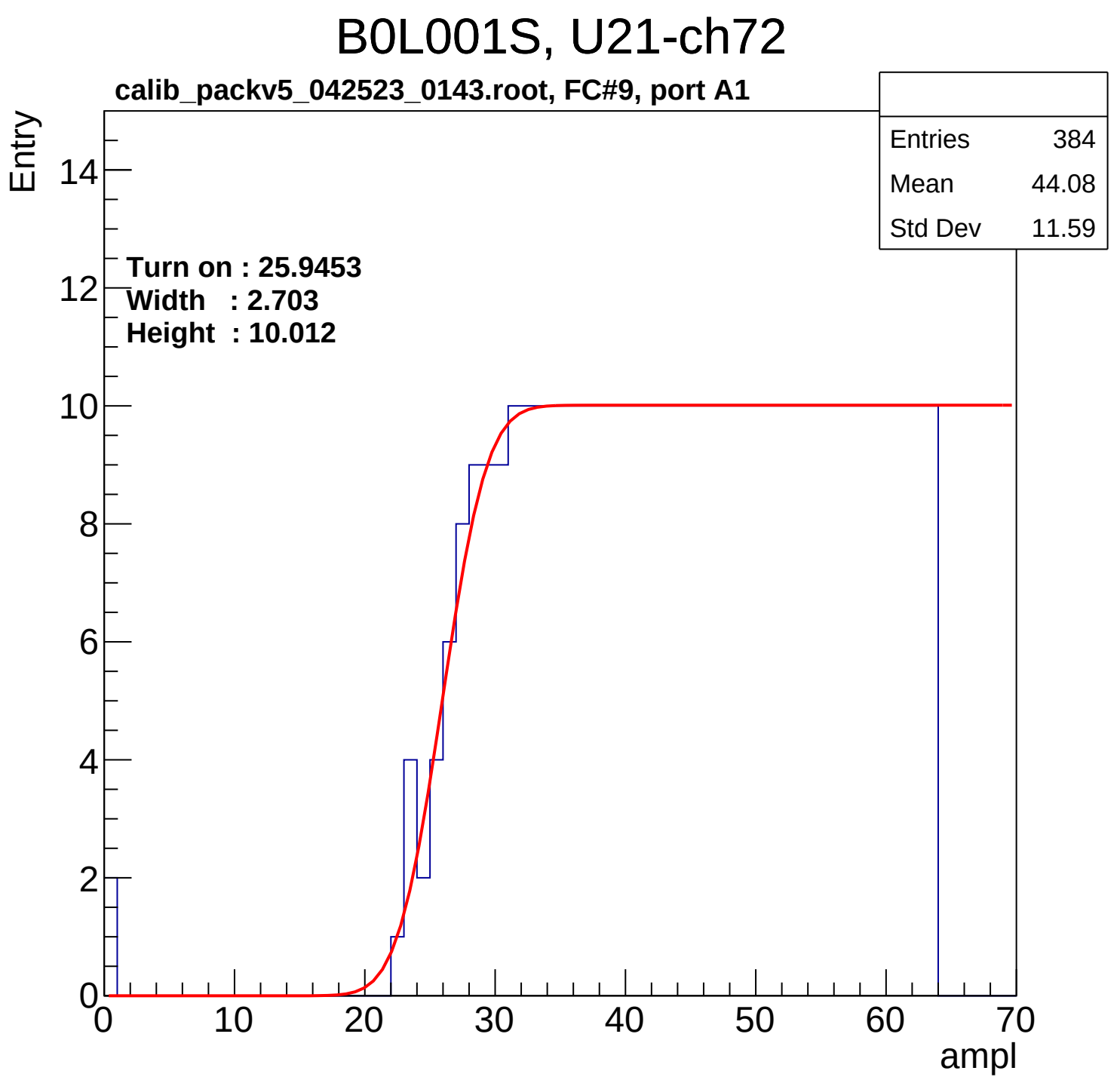
B0L001S, U21-ch72
calib_packv5_042523_0143.root, FC#9, port A1
Entries 384
Mean 44.08
Std Dev 11.59
Turn on : 25.9453
Width : 2.703
Height : 10.012
Entry
ampl
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6
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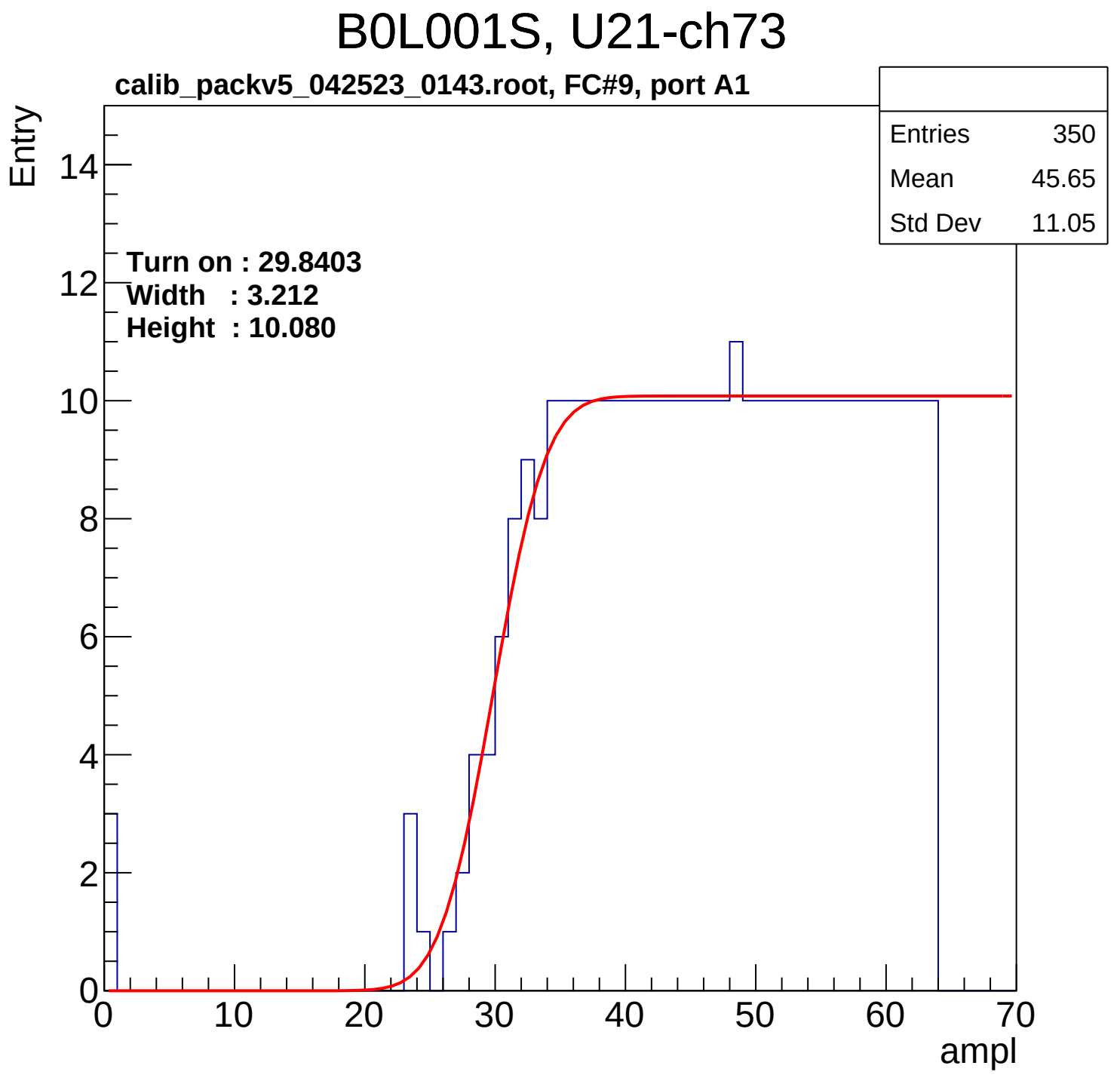
B0L001S, U21-ch73
calib_packv5_042523_0143.root, FC#9, port A1
Entries 350
Mean 45.65
Std Dev 11.05
Turn on : 29.8403
Width : 3.212
Height : 10.080
Entry
ampl
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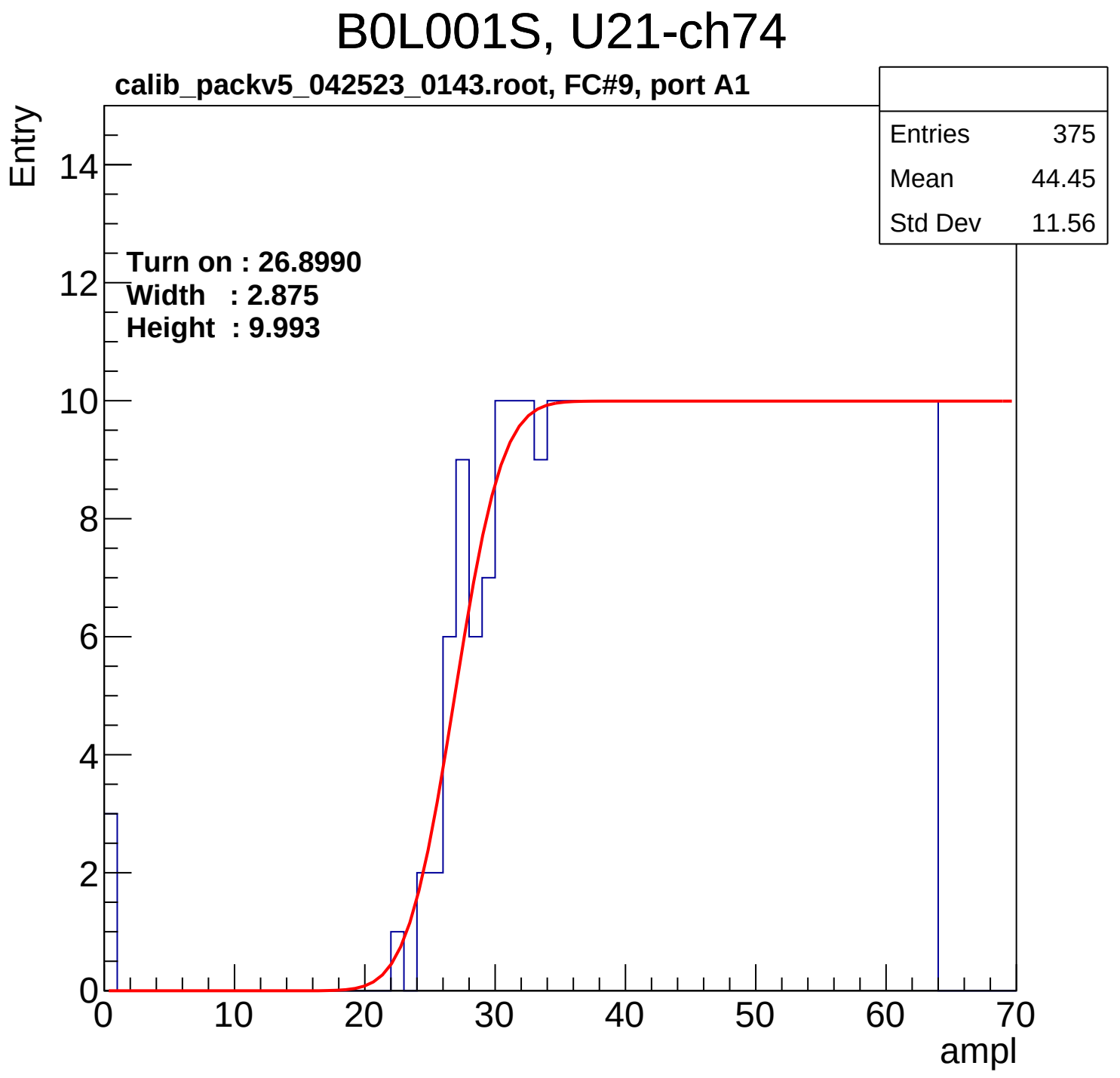
B0L001S, U21-ch74
calib_packv5_042523_0143.root, FC#9, port A1
Entries 375
Mean 44.45
Std Dev 11.56
Turn on : 26.8990
Width : 2.875
Height : 9.993
Entry
ampl
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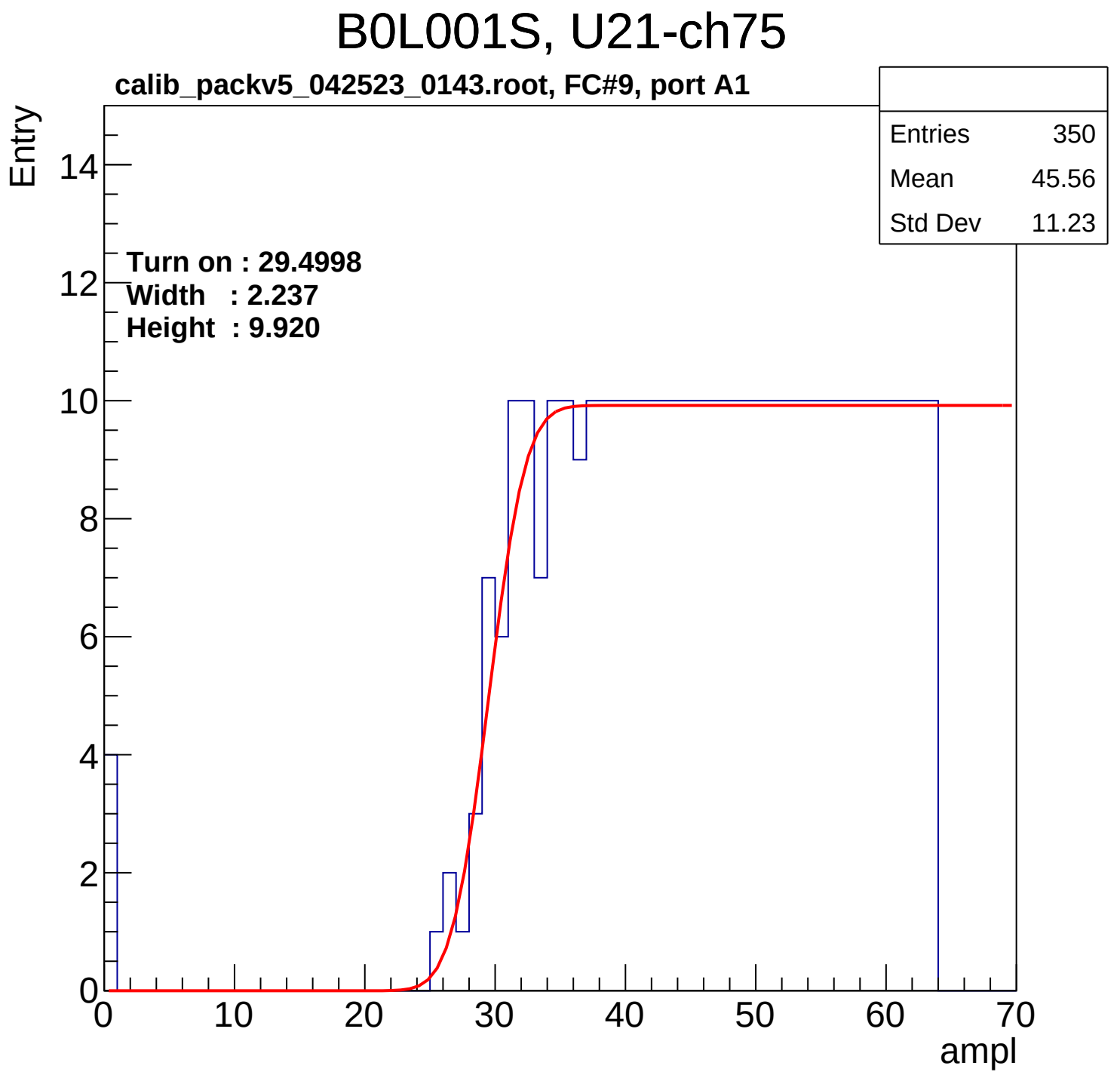
B0L001S, U21-ch75
calib_packv5_042523_0143.root, FC#9, port A1
Entries 350
Mean 45.56
Std Dev 11.23
Turn on : 29.4998
Width : 2.237
Height : 9.920
Entry
ampl
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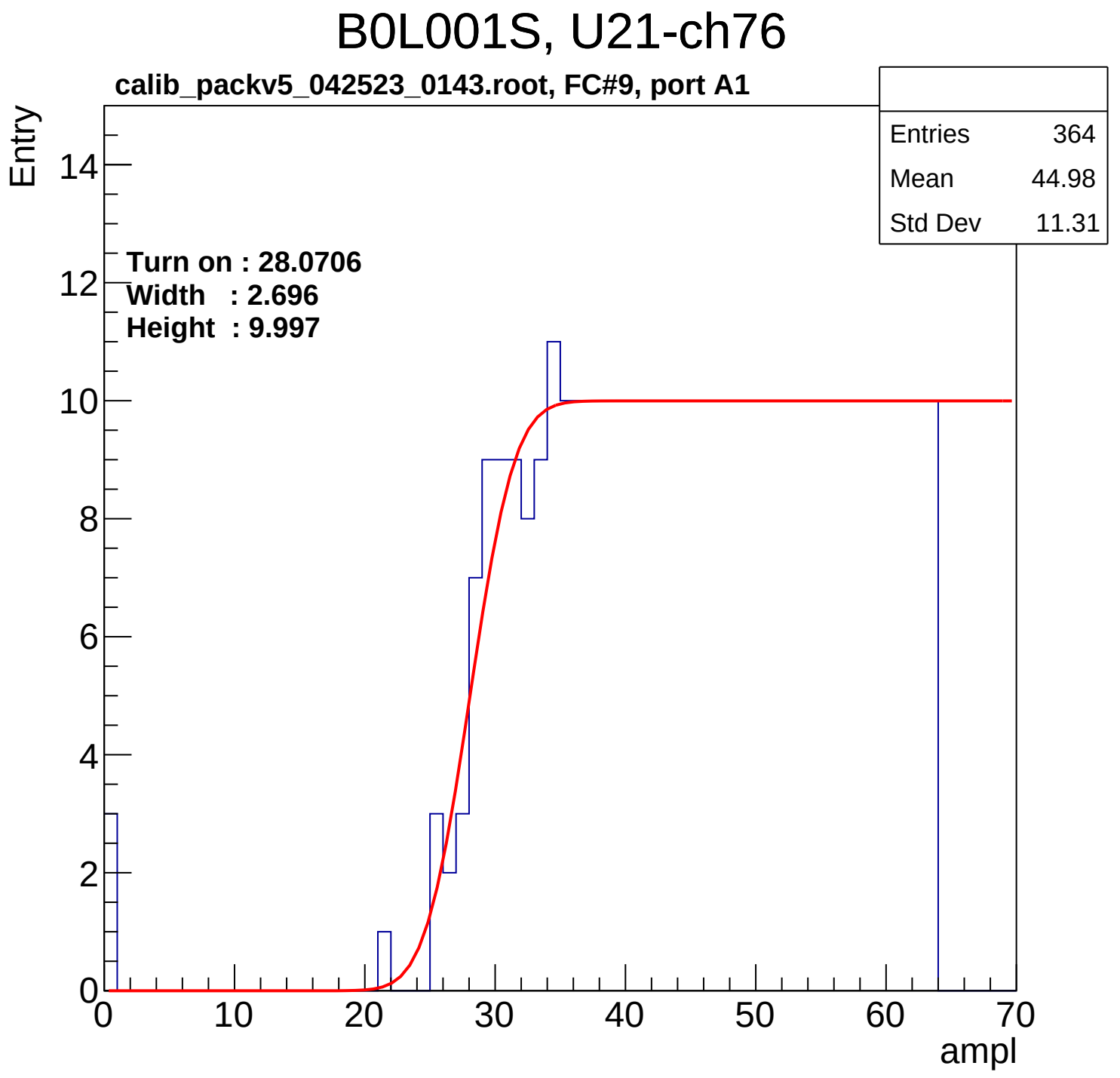
B0L001S, U21-ch76
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 44.98
Std Dev 11.31
Turn on : 28.0706
Width : 2.696
Height : 9.997
Entry
ampl
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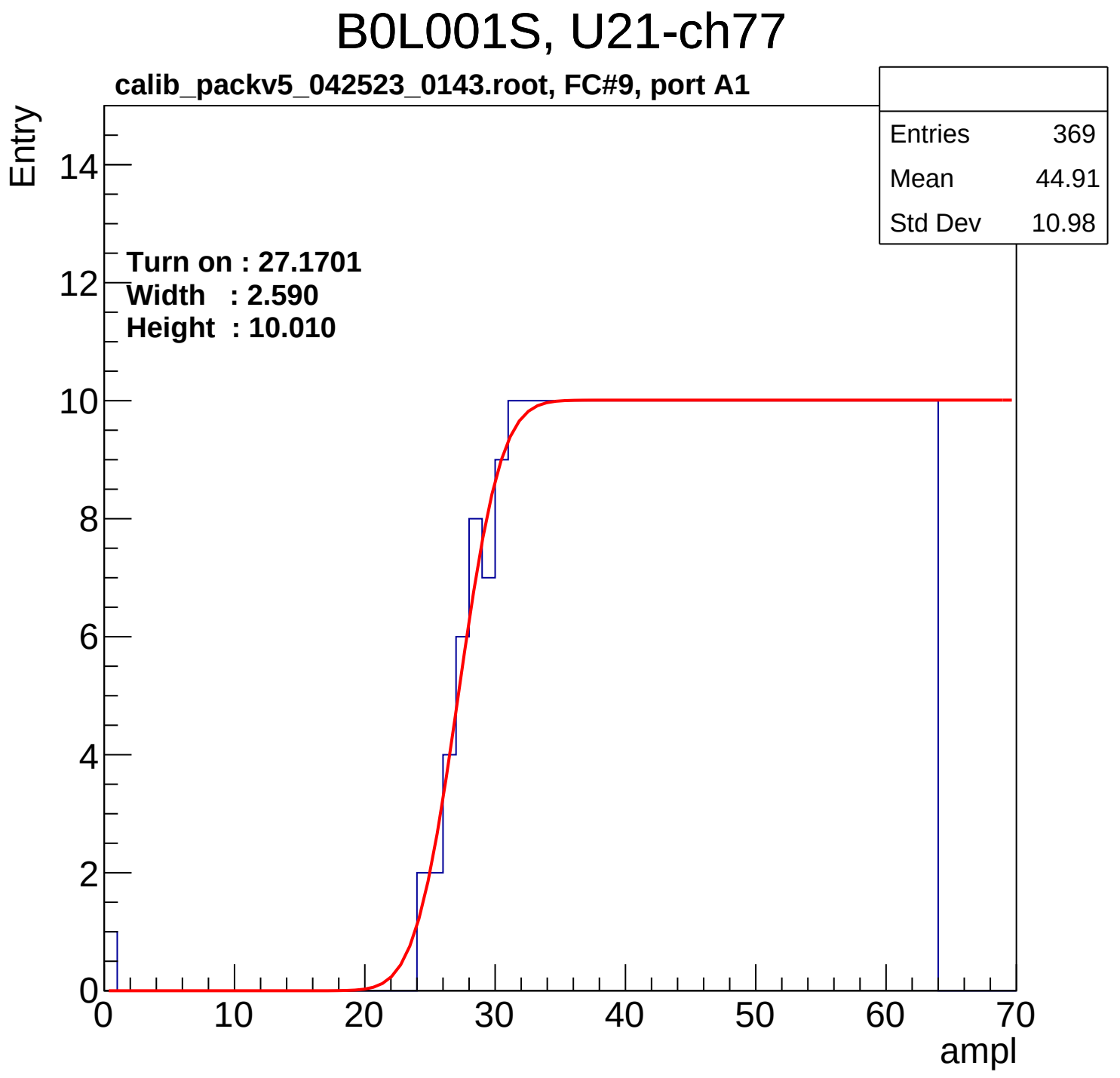
B0L001S, U21-ch77
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.91
Std Dev 10.98
Turn on : 27.1701
Width : 2.590
Height : 10.010
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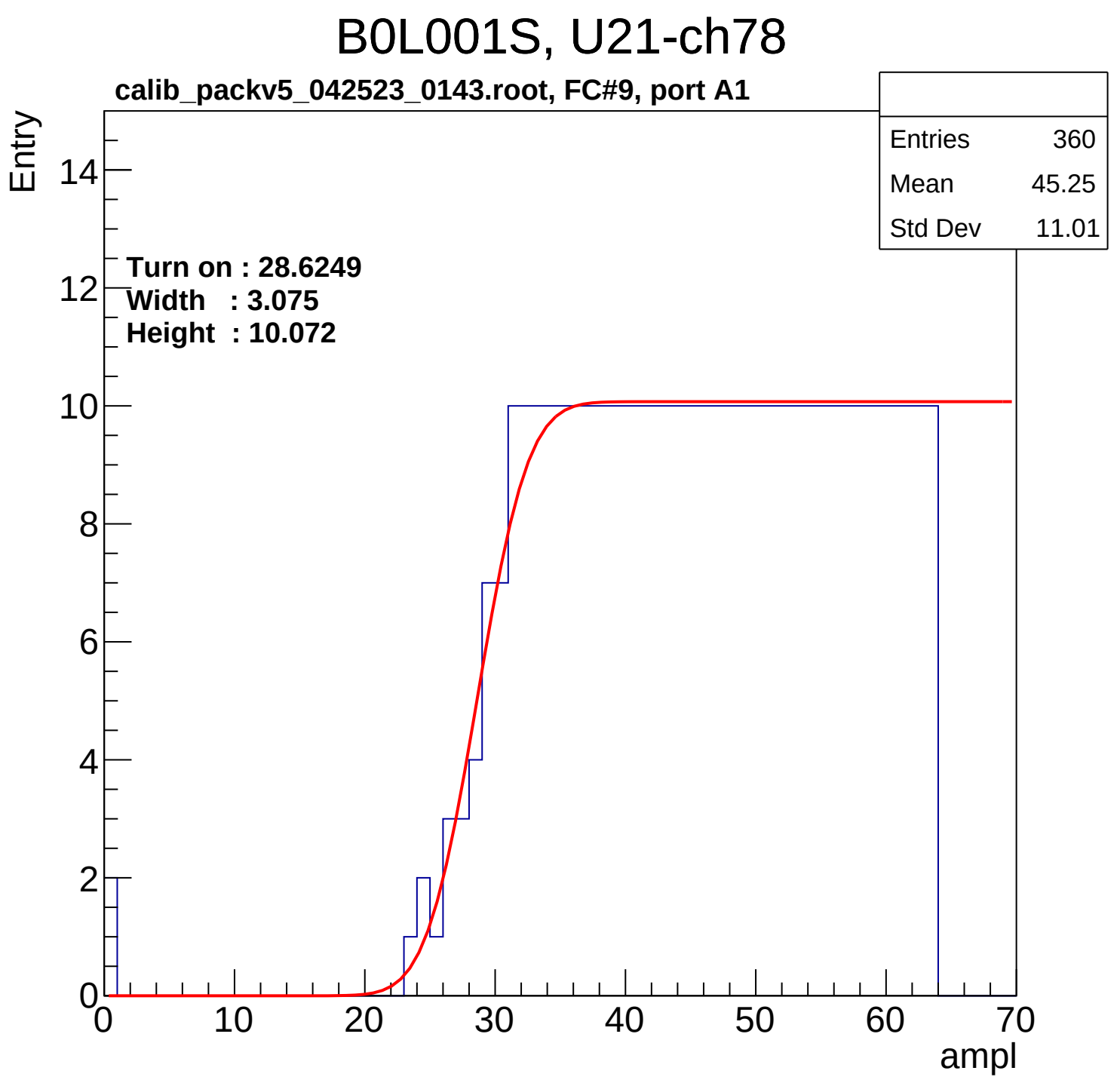
B0L001S, U21-ch78
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 45.25
Std Dev 11.01
Turn on : 28.6249
Width : 3.075
Height : 10.072
Entry
ampl
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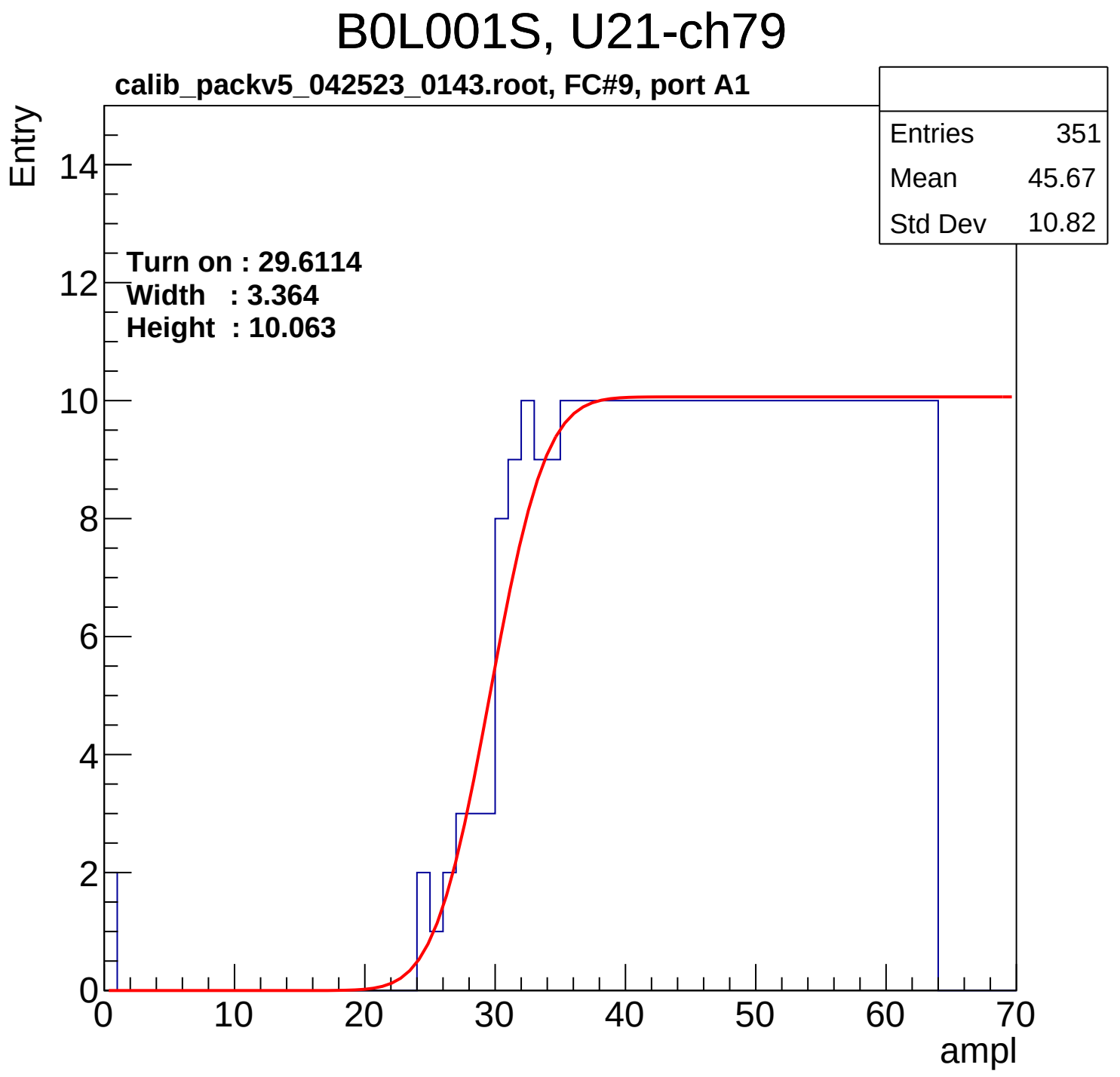
B0L001S, U21-ch79
calib_packv5_042523_0143.root, FC#9, port A1
Entries 351
Mean 45.67
Std Dev 10.82
Turn on : 29.6114
Width : 3.364
Height : 10.063
Entry
ampl
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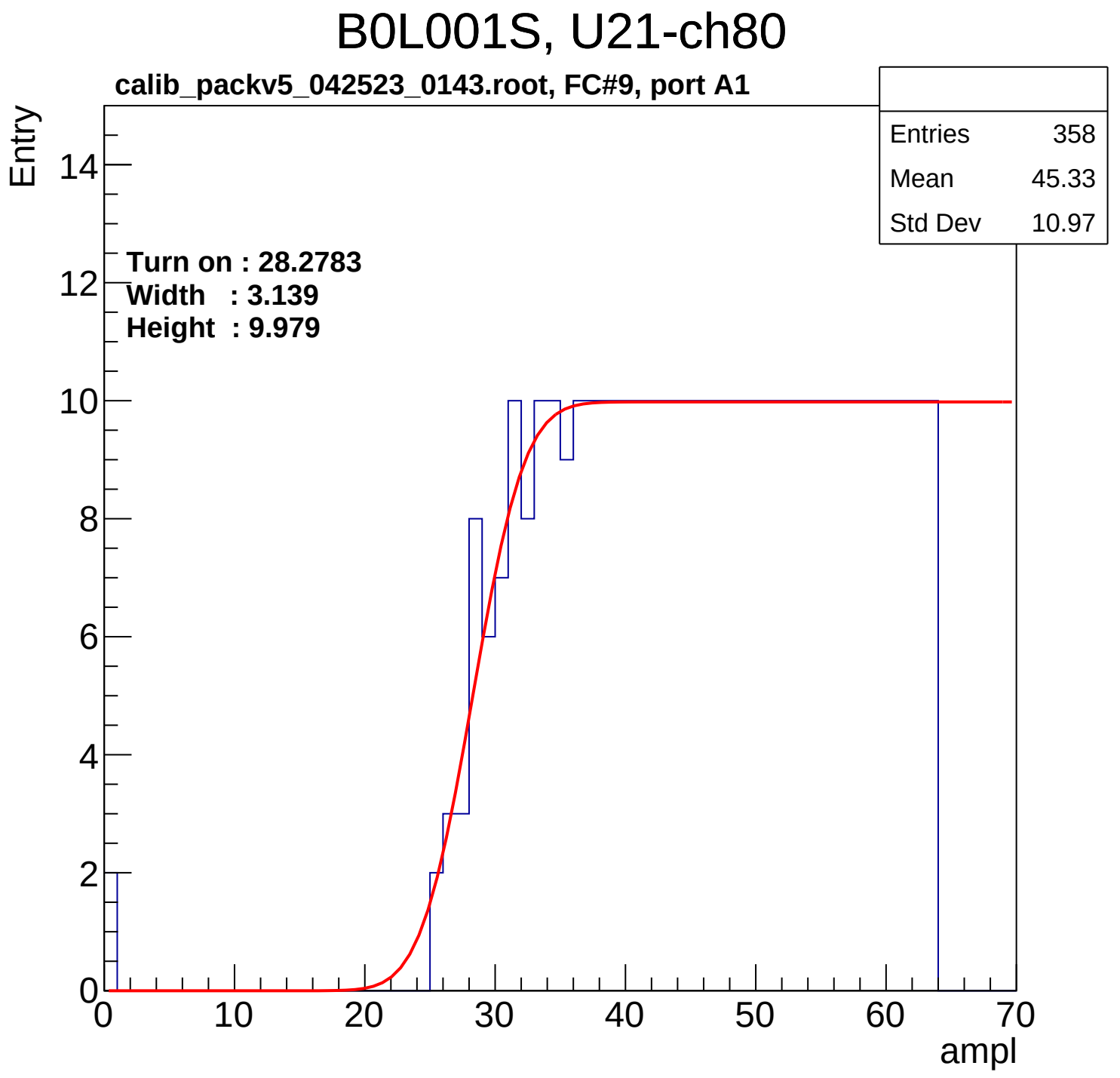
B0L001S, U21-ch80
calib_packv5_042523_0143.root, FC#9, port A1
Entries 358
Mean 45.33
Std Dev 10.97
Turn on : 28.2783
Width : 3.139
Height : 9.979
Entry
ampl
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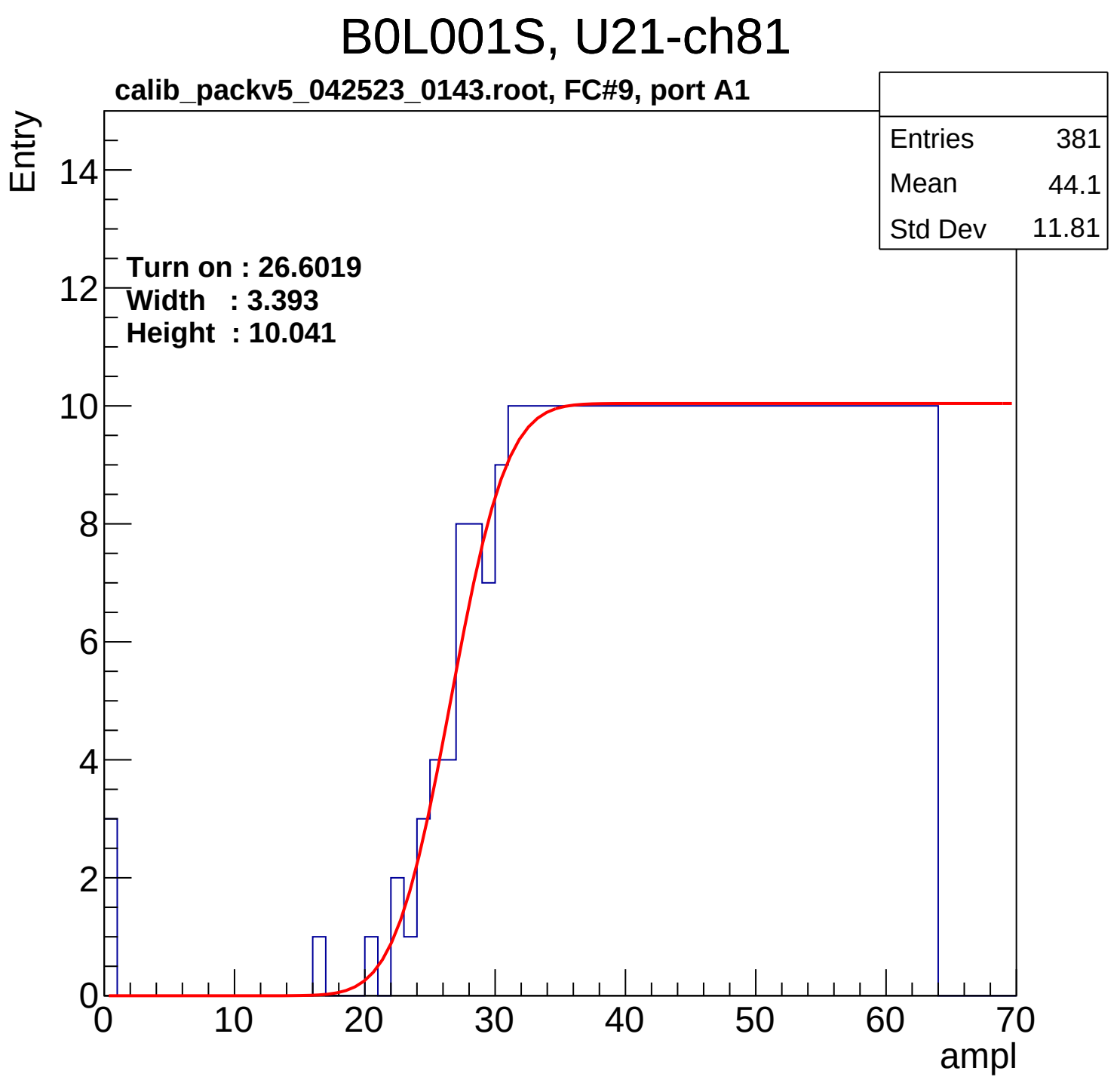
B0L001S, U21-ch81
calib_packv5_042523_0143.root, FC#9, port A1
Entries 381
Mean 44.1
Std Dev 11.81
Turn on : 26.6019
Width : 3.393
Height : 10.041
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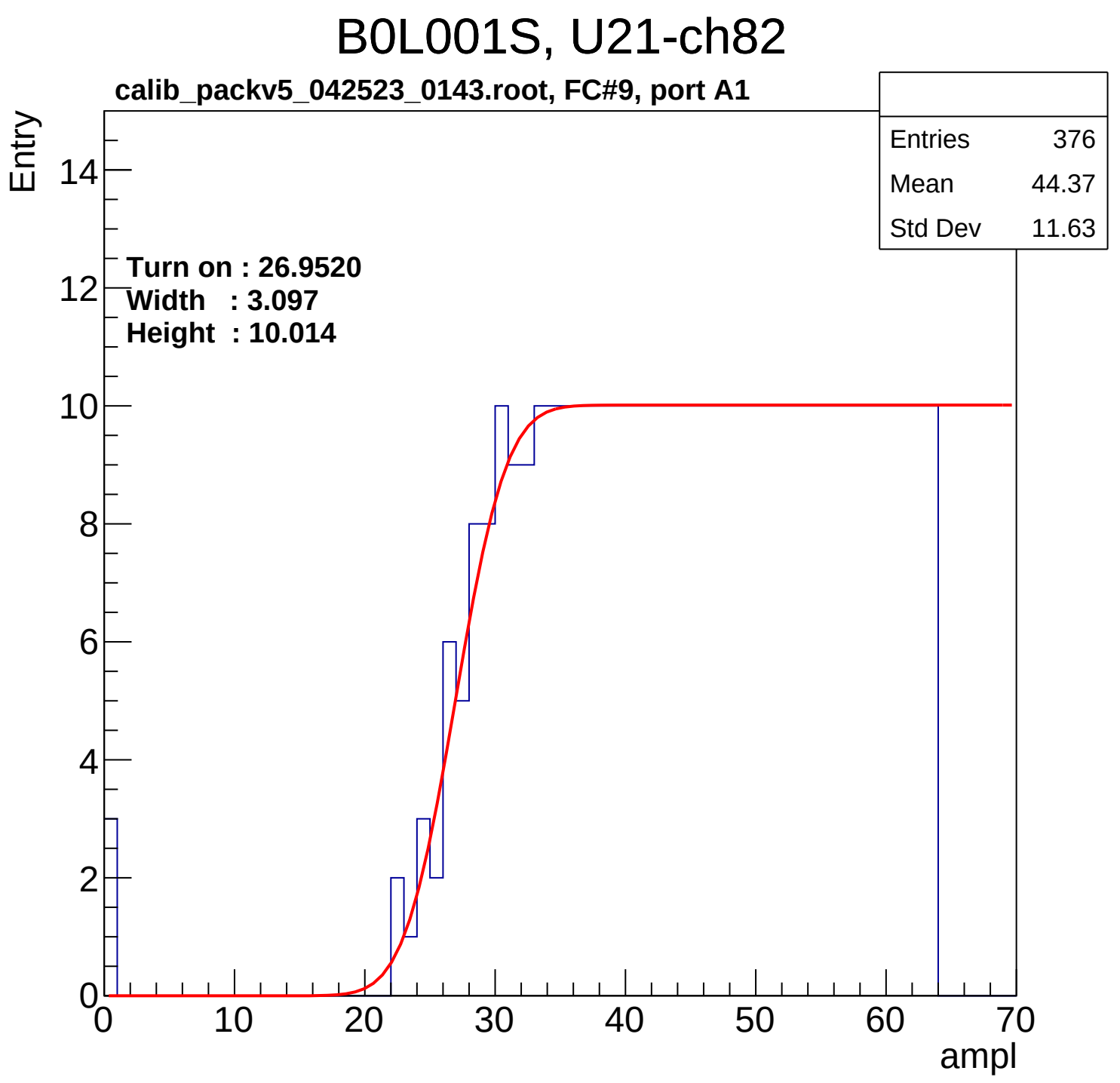
B0L001S, U21-ch82
calib_packv5_042523_0143.root, FC#9, port A1
Entries 376
Mean 44.37
Std Dev 11.63
Turn on : 26.9520
Width : 3.097
Height : 10.014
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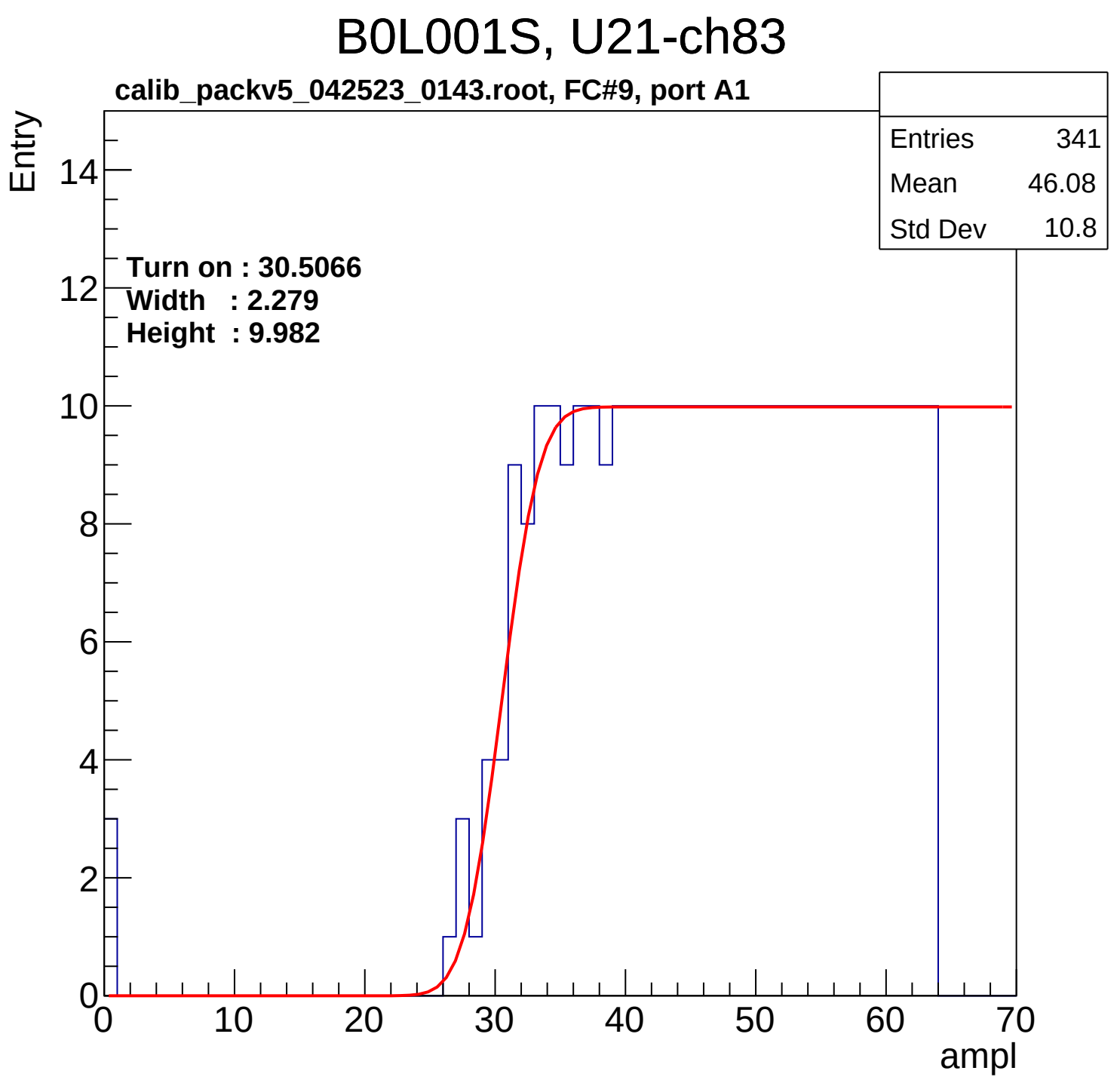
B0L001S, U21-ch83
calib_packv5_042523_0143.root, FC#9, port A1
Entries 341
Mean 46.08
Std Dev 10.8
Turn on : 30.5066
Width : 2.279
Height : 9.982
Entry
ampl
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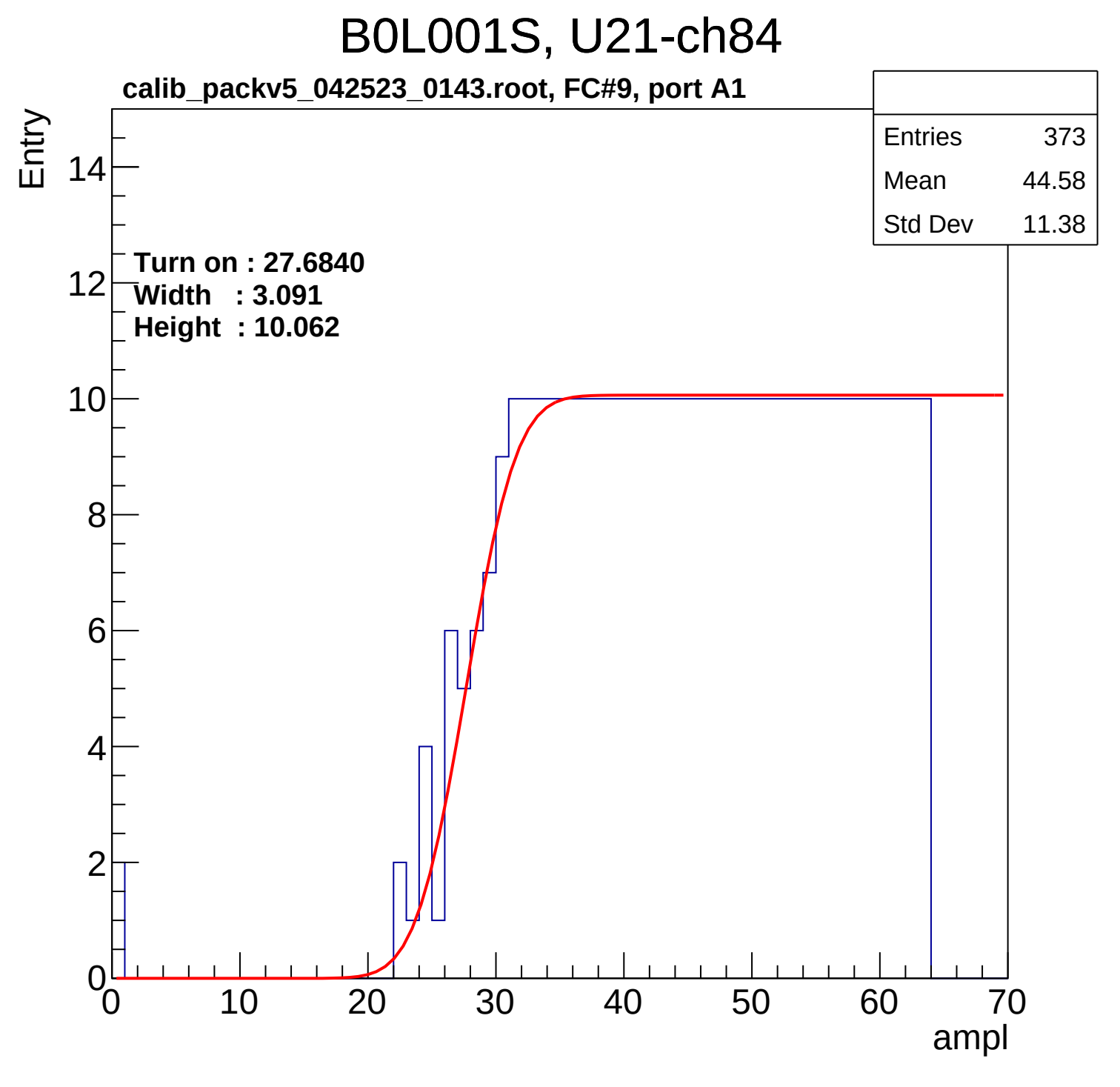
B0L001S, U21-ch84
calib_packv5_042523_0143.root, FC#9, port A1
Entries 373
Mean 44.58
Std Dev 11.38
Turn on : 27.6840
Width : 3.091
Height : 10.062
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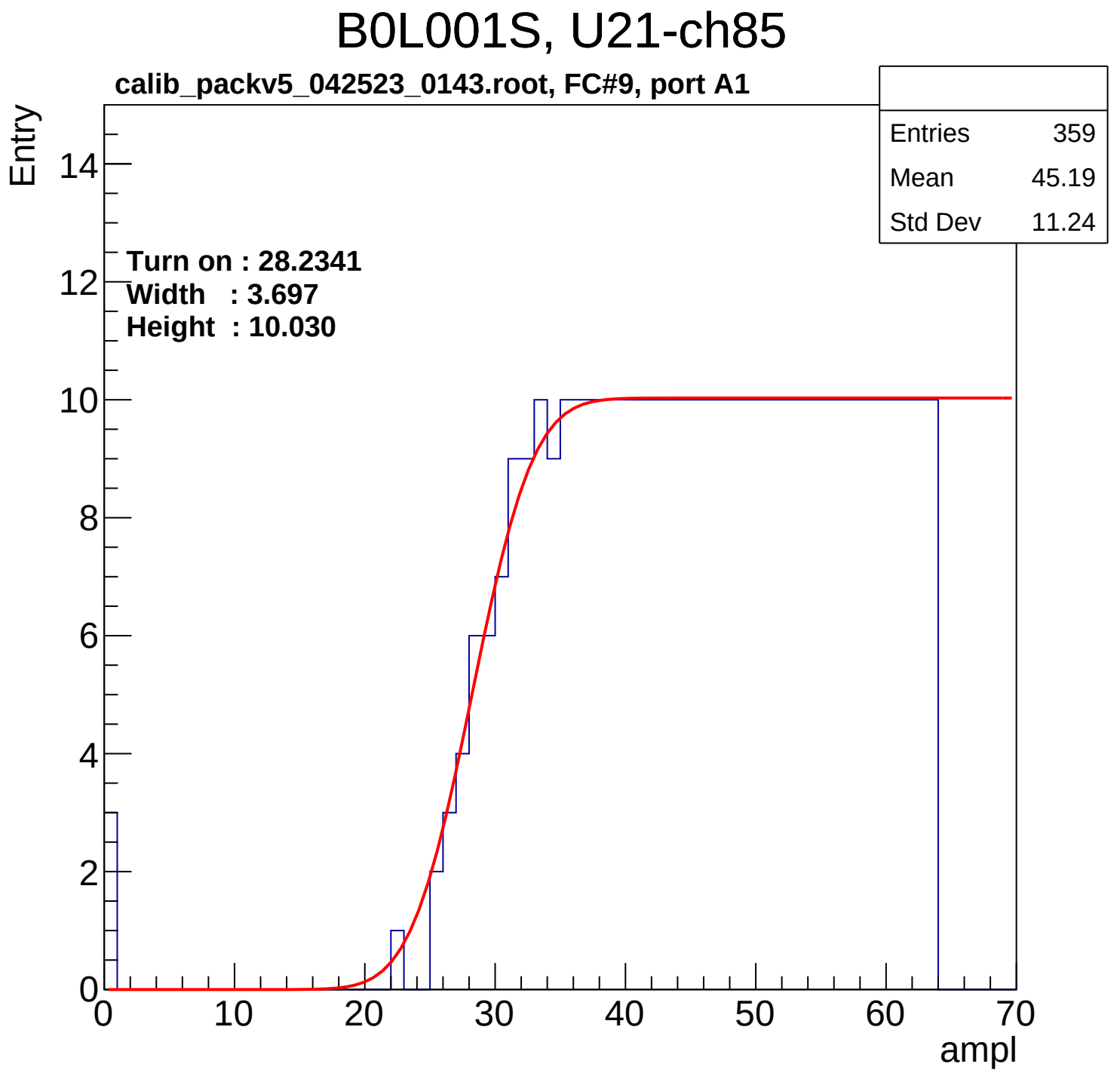
B0L001S, U21-ch85
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 45.19
Std Dev 11.24
Turn on : 28.2341
Width : 3.697
Height : 10.030
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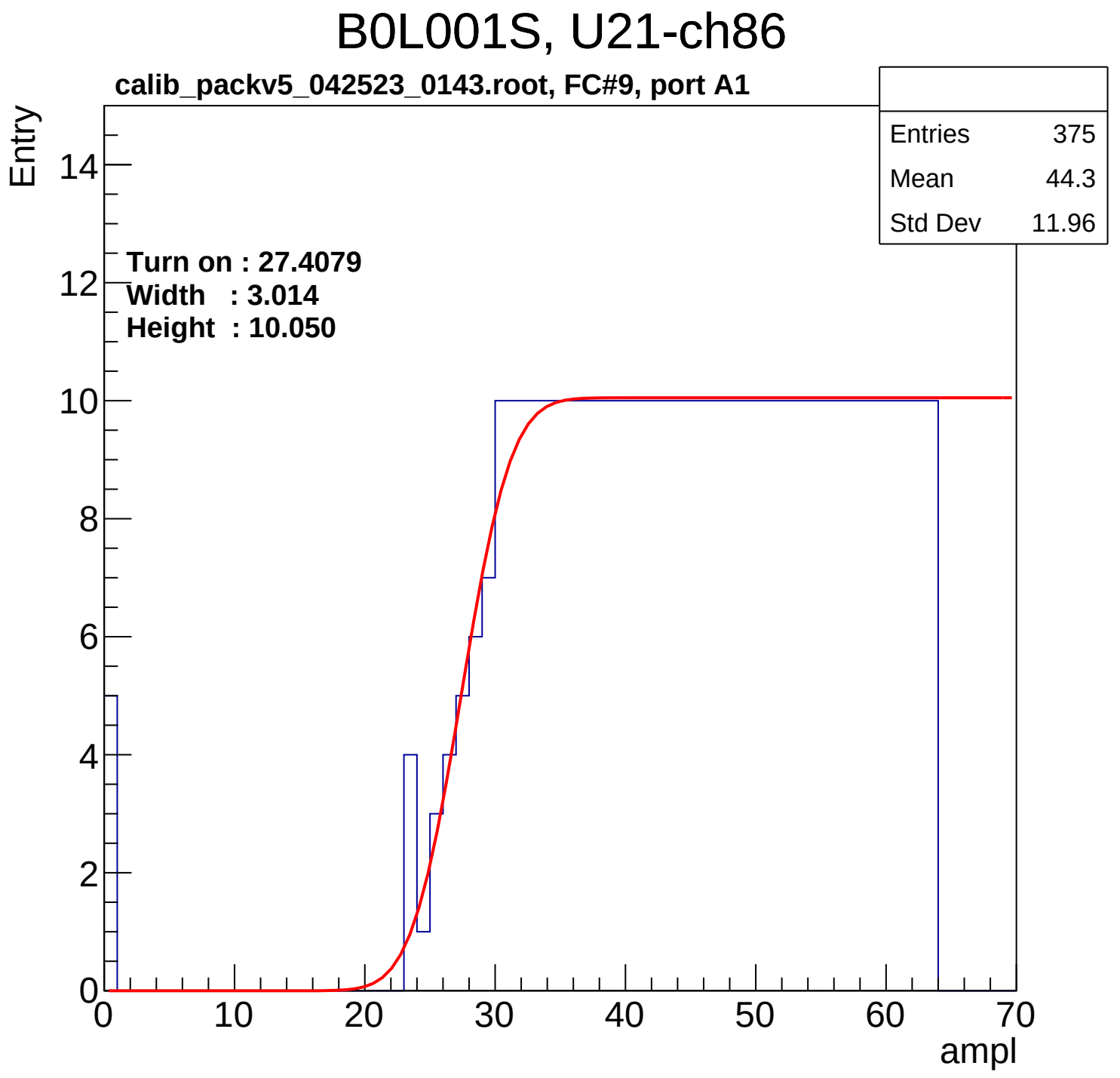
B0L001S, U21-ch86
calib_packv5_042523_0143.root, FC#9, port A1
Entries 375
Mean 44.3
Std Dev 11.96
Turn on : 27.4079
Width : 3.014
Height : 10.050
Entry
ampl
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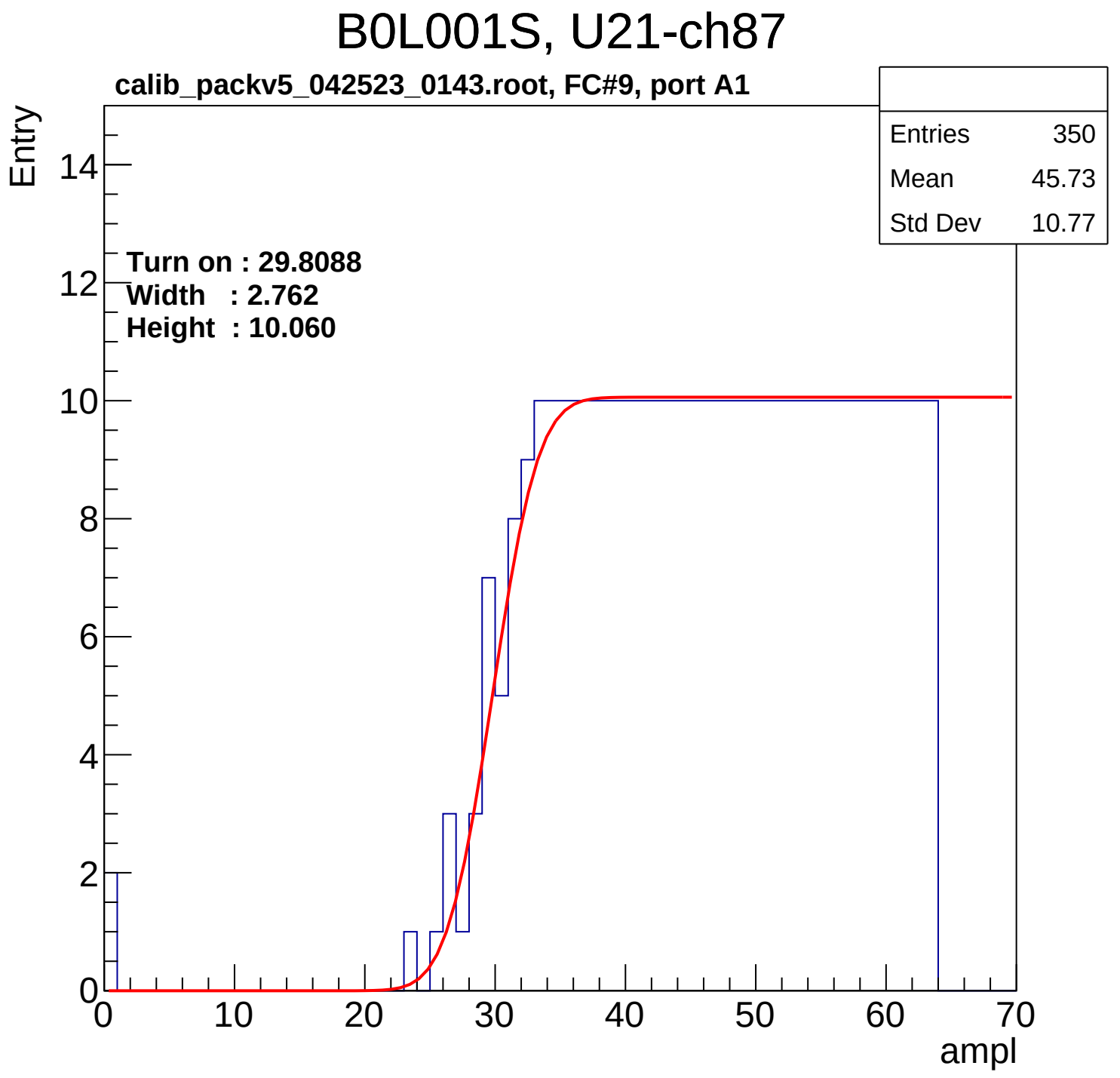
B0L001S, U21-ch87
calib_packv5_042523_0143.root, FC#9, port A1
Entries 350
Mean 45.73
Std Dev 10.77
Turn on : 29.8088
Width : 2.762
Height : 10.060
Entry
ampl
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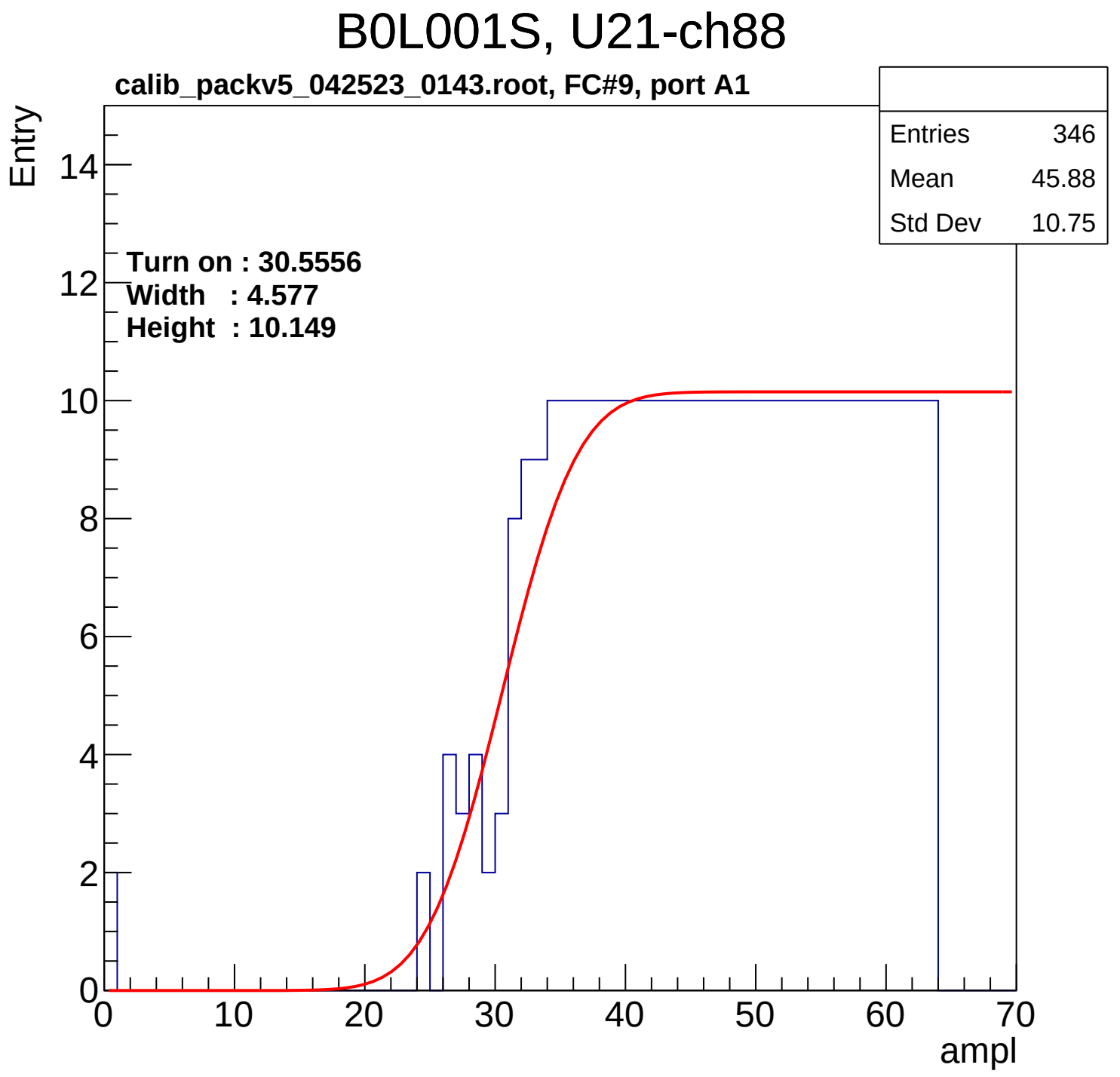
B0L001S, U21-ch88
calib_packv5_042523_0143.root, FC#9, port A1
Entries 346
Mean 45.88
Std Dev 10.75
Turn on : 30.5556
Width : 4.577
Height : 10.149
Entry
ampl
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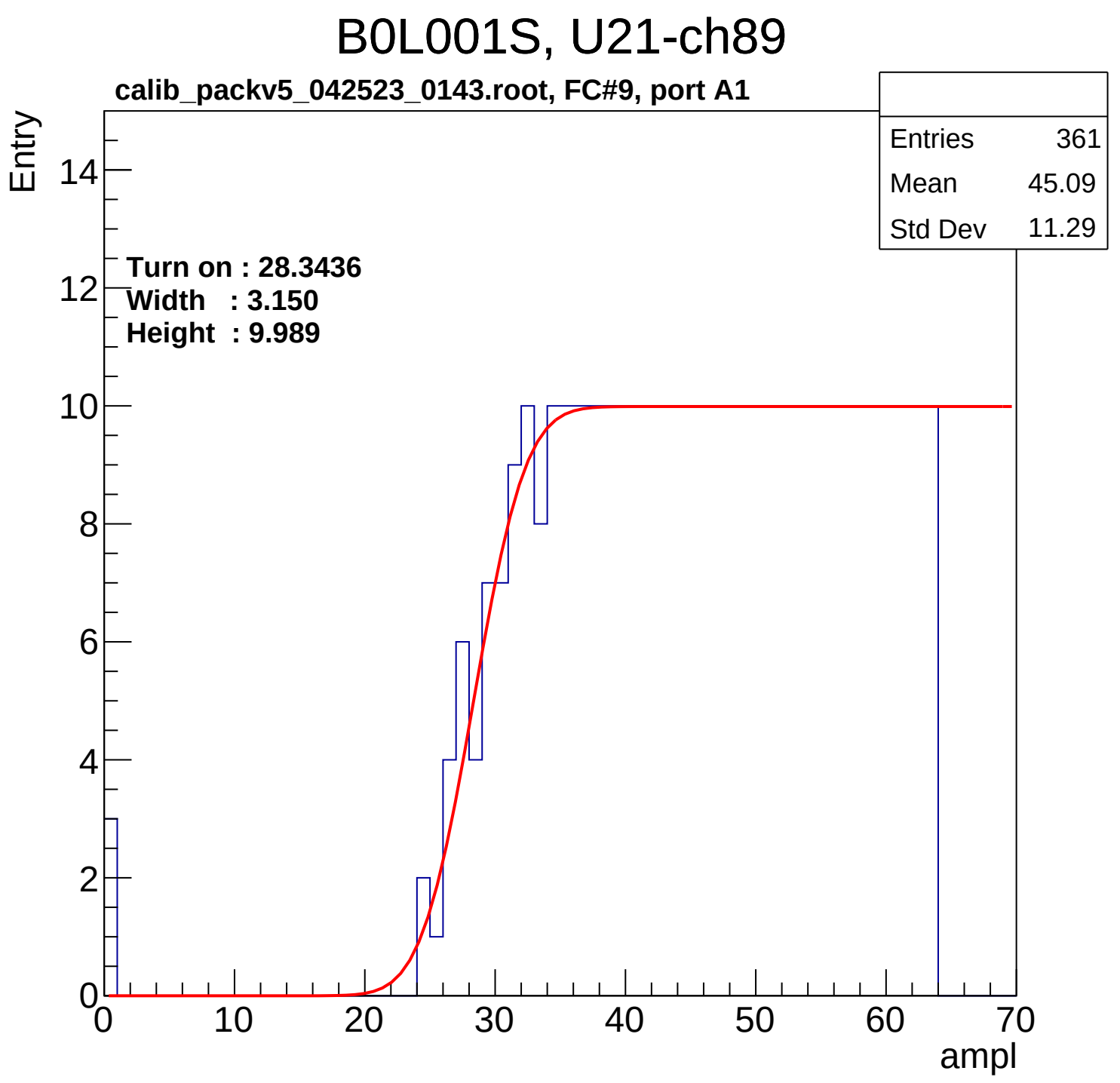
B0L001S, U21-ch89
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 45.09
Std Dev 11.29
Turn on : 28.3436
Width : 3.150
Height : 9.989
Entry
ampl
0
2
4
6
8
10
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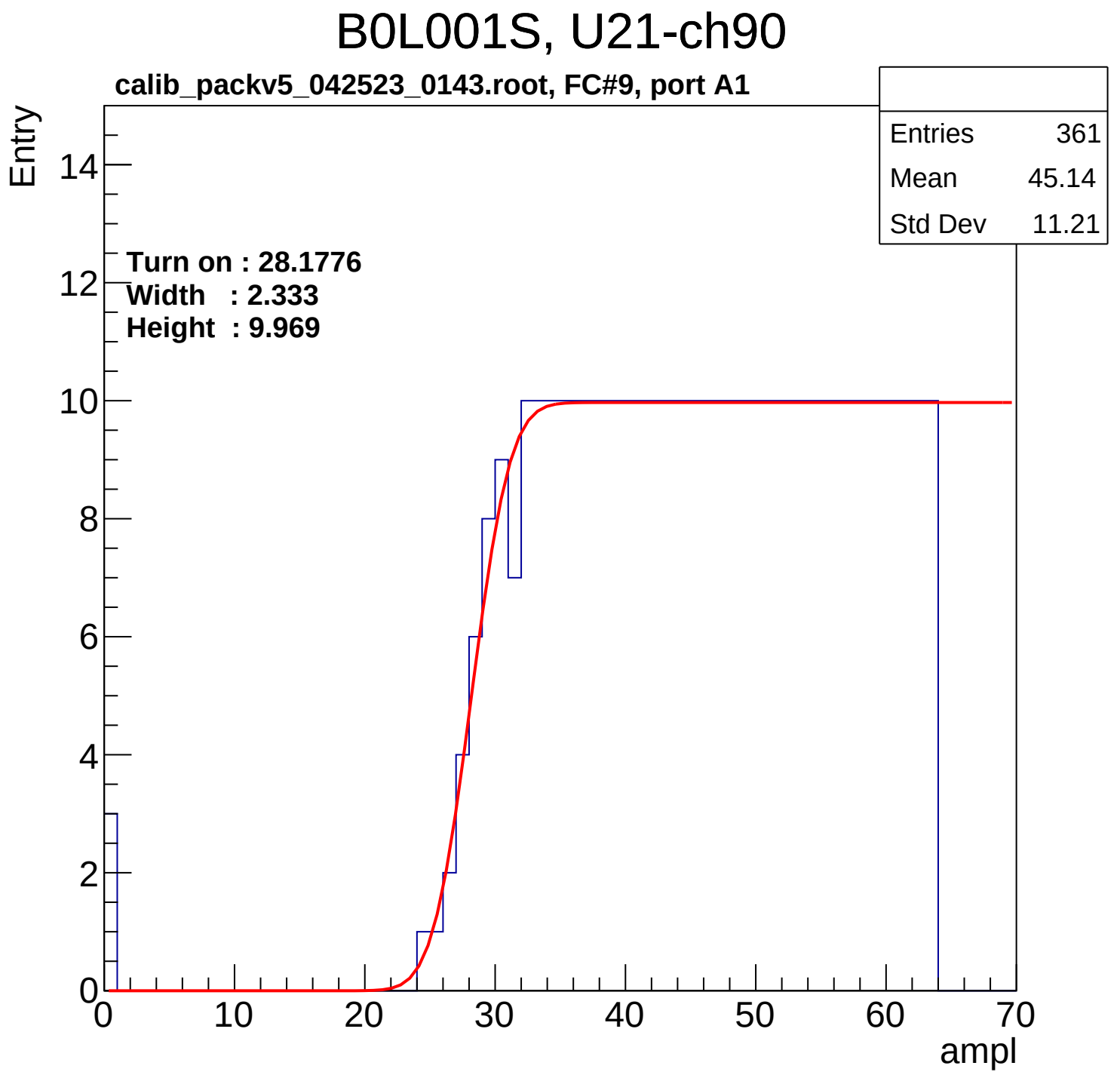
B0L001S, U21-ch90
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 45.14
Std Dev 11.21
Turn on : 28.1776
Width : 2.333
Height : 9.969
Entry
ampl
0
2
4
6
8
10
12
14
0
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60
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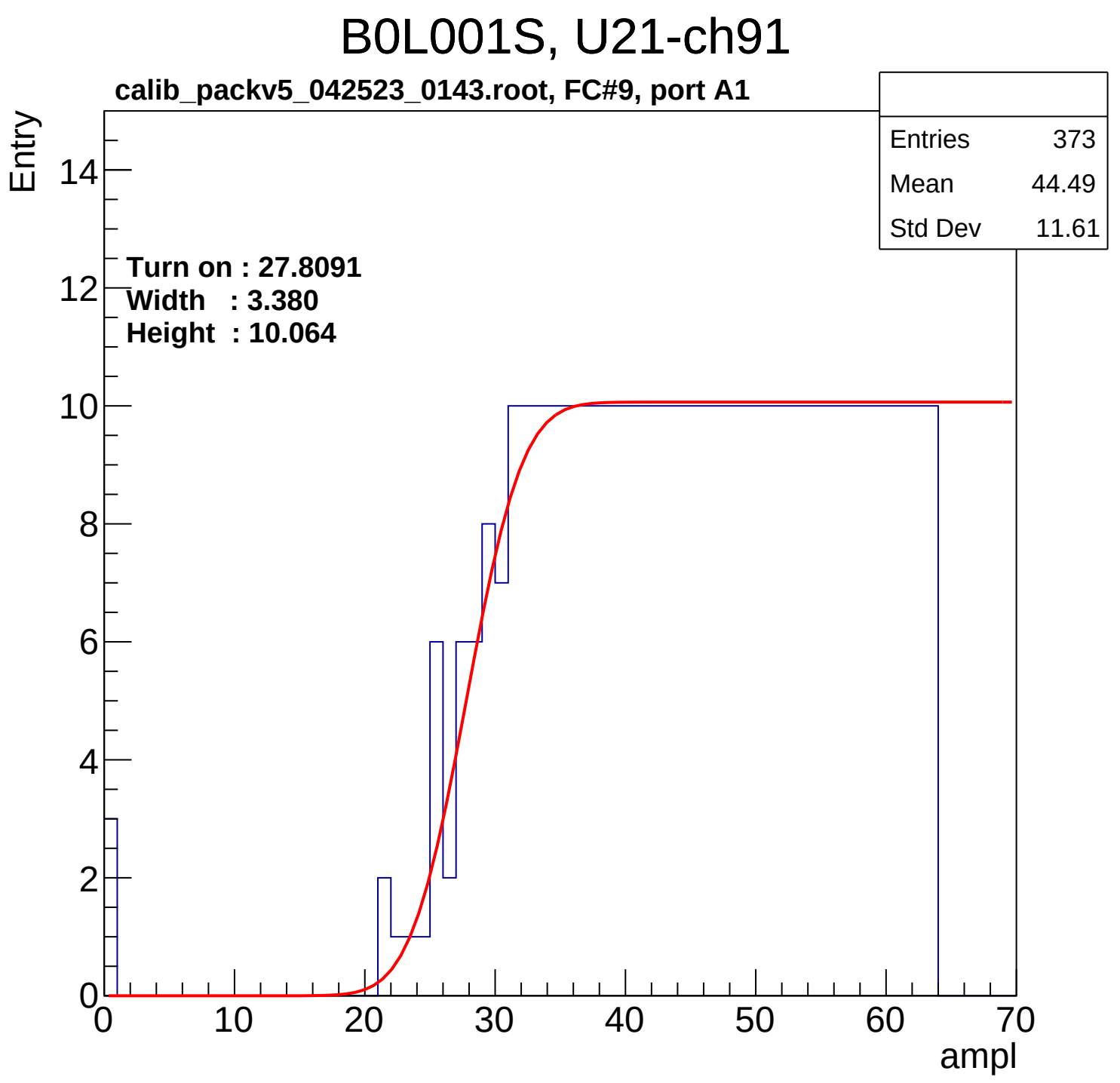
B0L001S, U21-ch91
calib_packv5_042523_0143.root, FC#9, port A1
Entries 373
Mean 44.49
Std Dev 11.61
Turn on : 27.8091
Width : 3.380
Height : 10.064
Entry
ampl
0
2
4
6
8
10
12
14
0
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60
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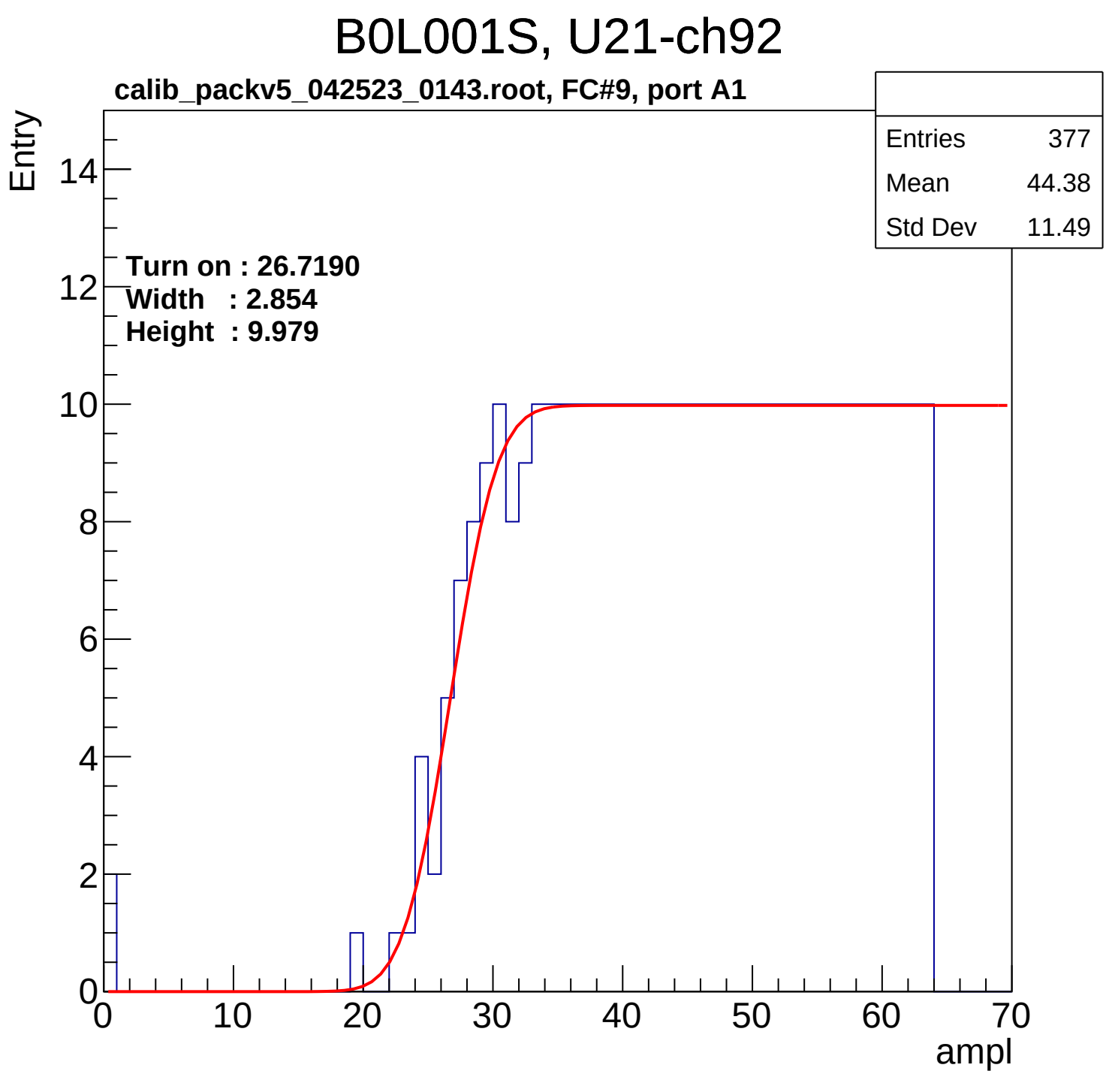
B0L001S, U21-ch92
calib_packv5_042523_0143.root, FC#9, port A1
Entries 377
Mean 44.38
Std Dev 11.49
Turn on : 26.7190
Width : 2.854
Height : 9.979
Entry
ampl
0
2
4
6
8
10
12
14
0
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60
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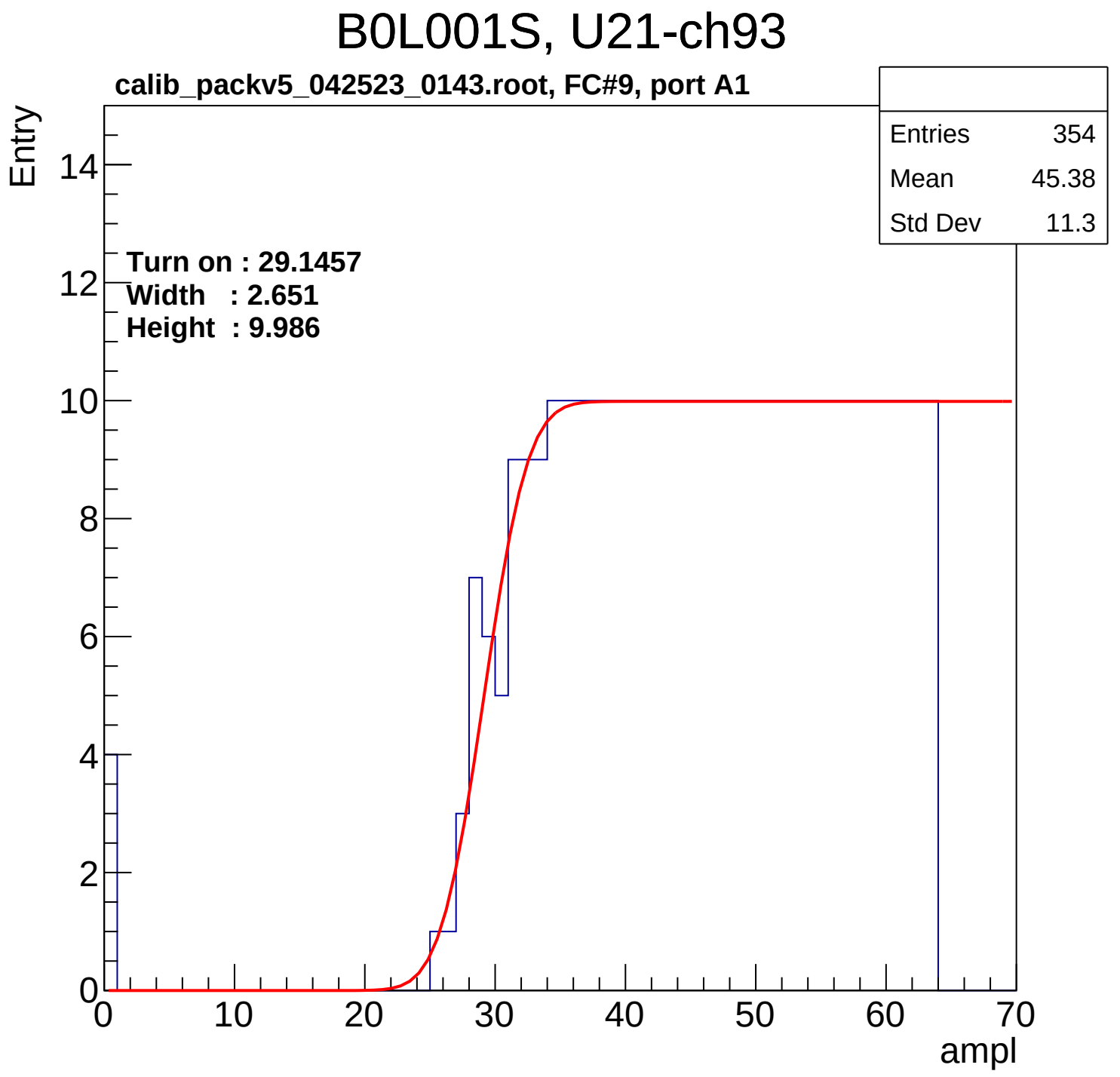
B0L001S, U21-ch93
calib_packv5_042523_0143.root, FC#9, port A1
Entries 354
Mean 45.38
Std Dev 11.3
Turn on : 29.1457
Width : 2.651
Height : 9.986
Entry
ampl
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2
4
6
8
10
12
14
0
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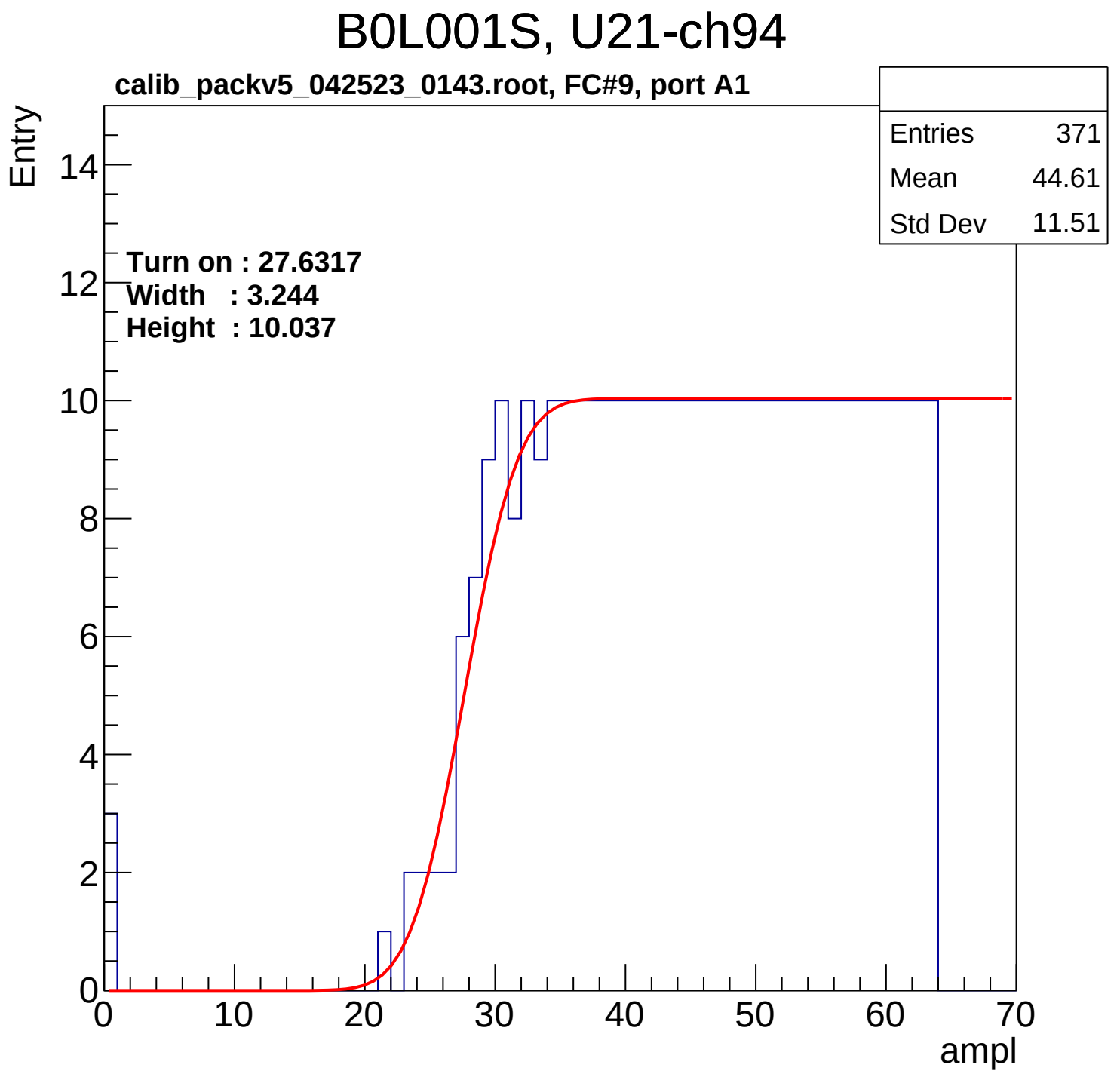
B0L001S, U21-ch94
calib_packv5_042523_0143.root, FC#9, port A1
Entries 371
Mean 44.61
Std Dev 11.51
Turn on : 27.6317
Width : 3.244
Height : 10.037
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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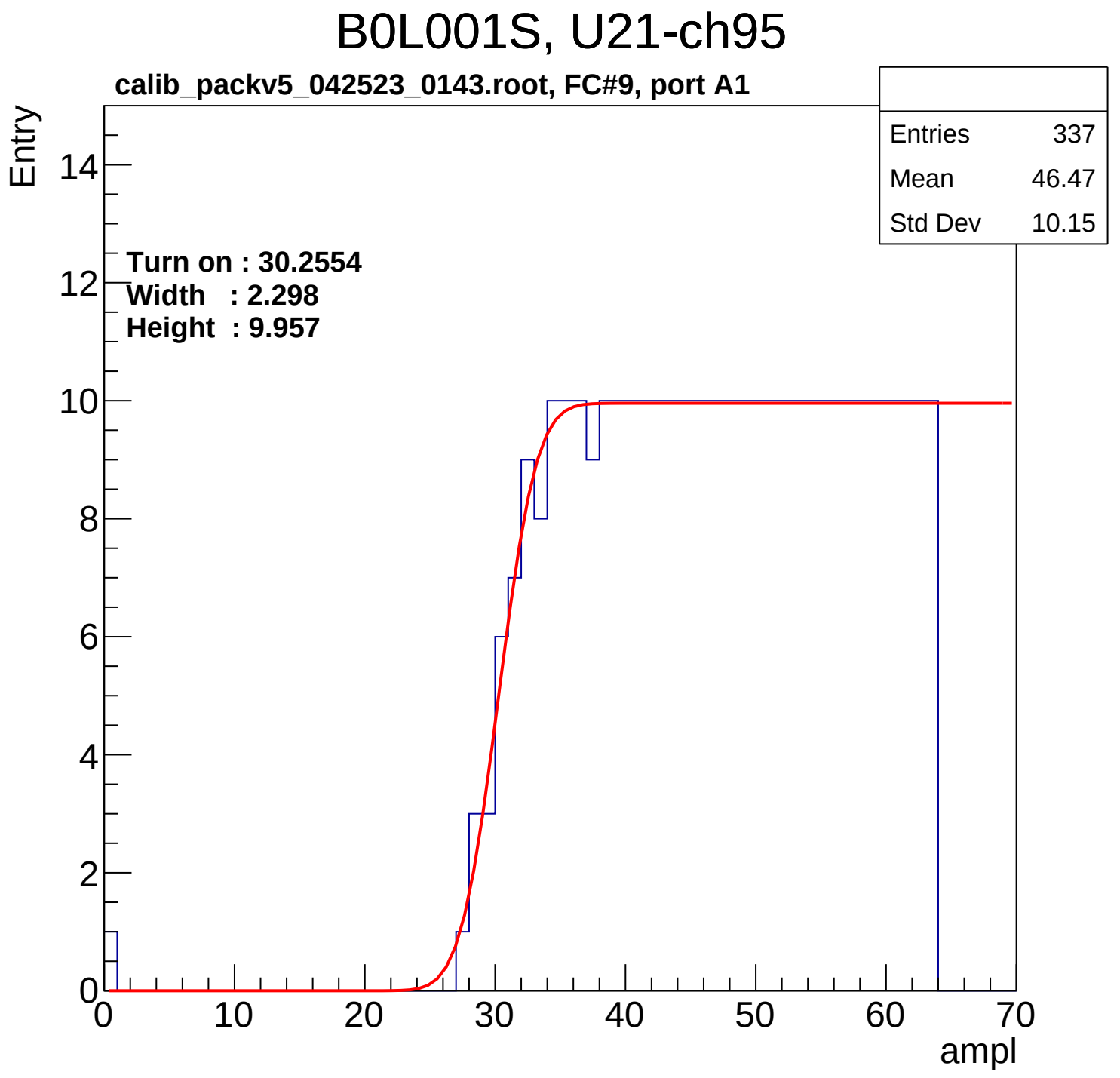
40
50
60
70


B0L001S, U21-ch95
calib_packv5_042523_0143.root, FC#9, port A1
Entries 337
Mean 46.47
Std Dev 10.15
Turn on : 30.2554
Width : 2.298
Height : 9.957
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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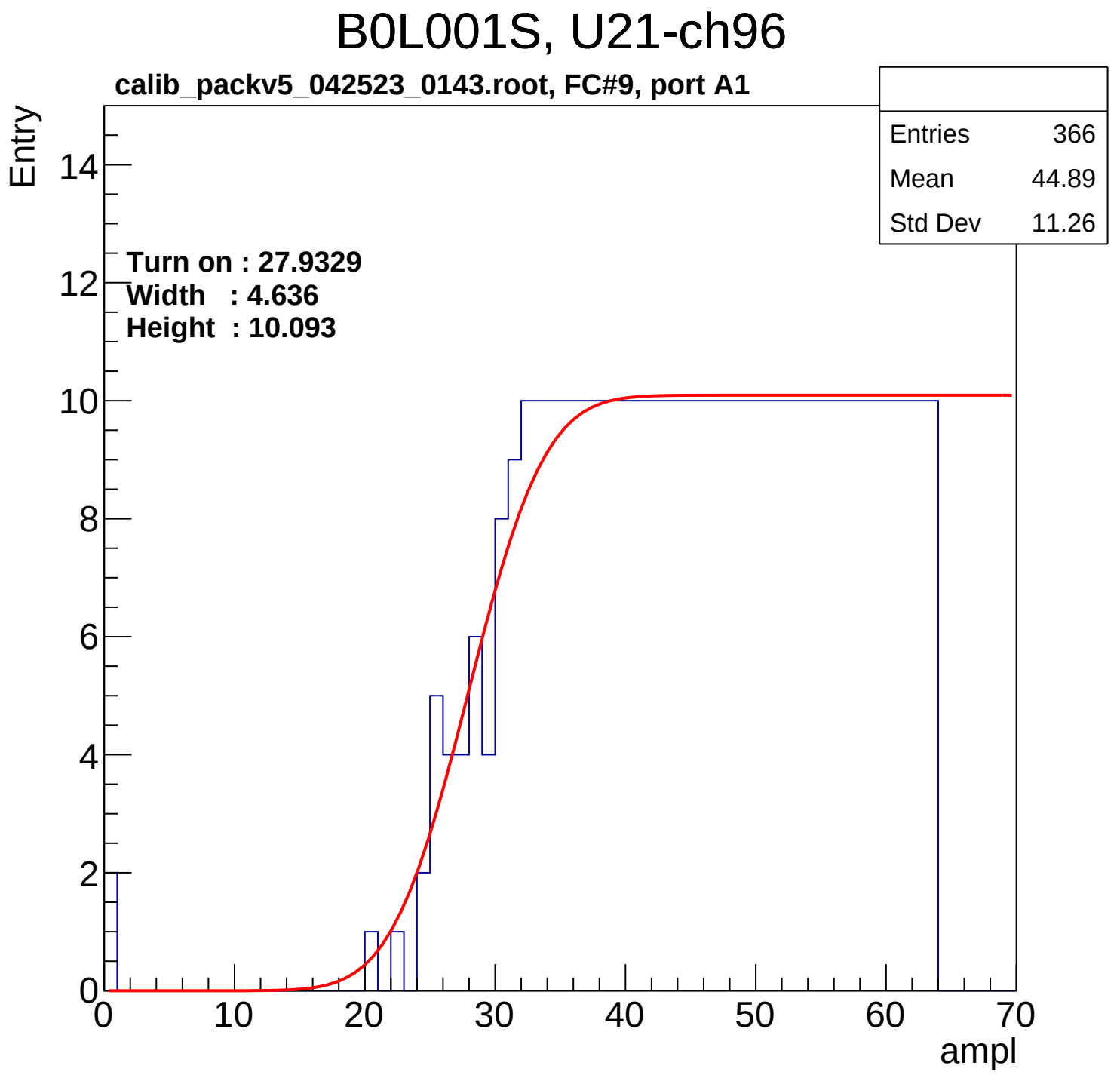
B0L001S, U21-ch96
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.89
Std Dev 11.26
Turn on : 27.9329
Width : 4.636
Height : 10.093
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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40
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60
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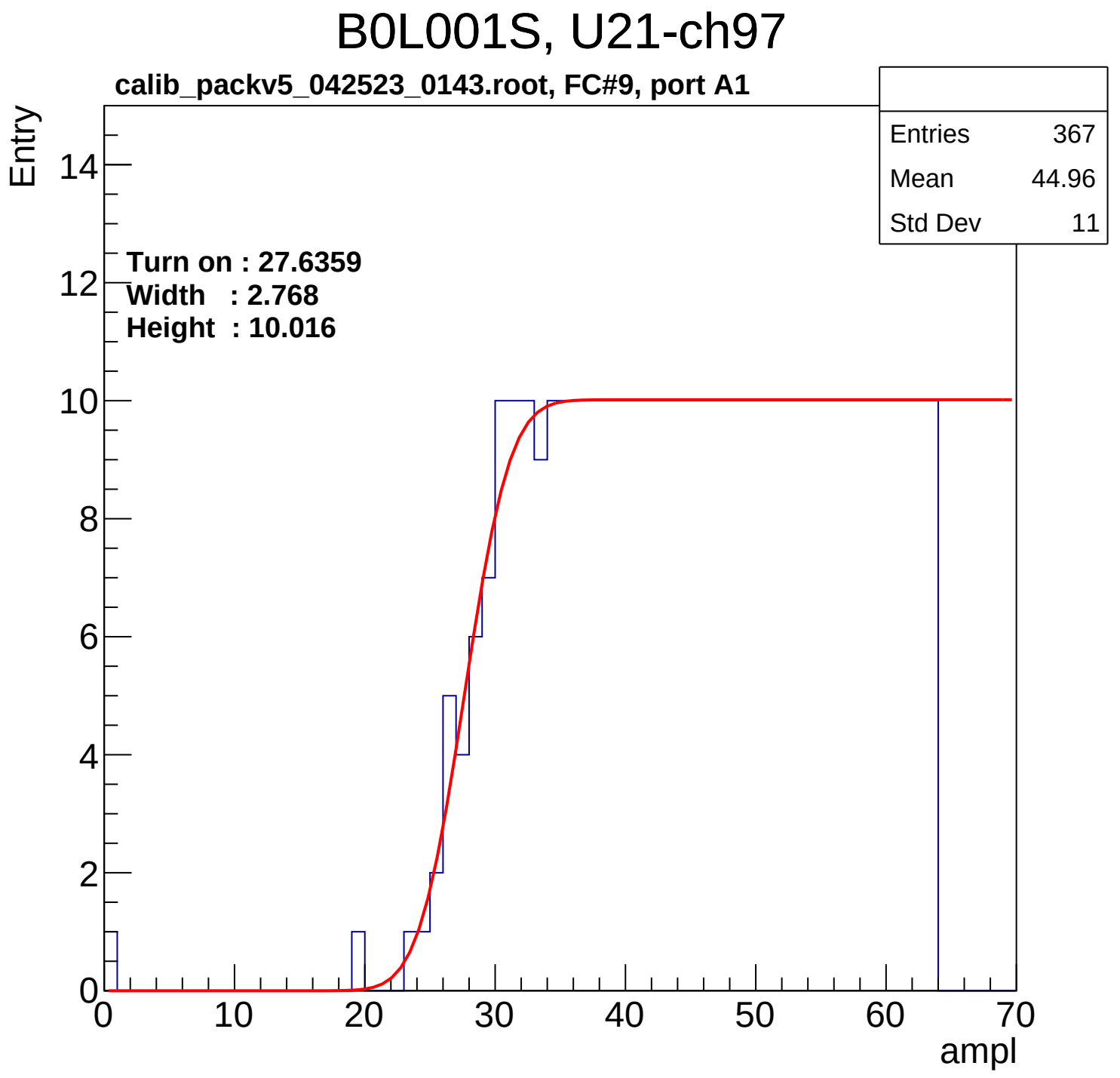
B0L001S, U21-ch97
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.96
Std Dev 11
Turn on : 27.6359
Width : 2.768
Height : 10.016
Entry
ampl
0
2
4
6
8
10
12
14
0
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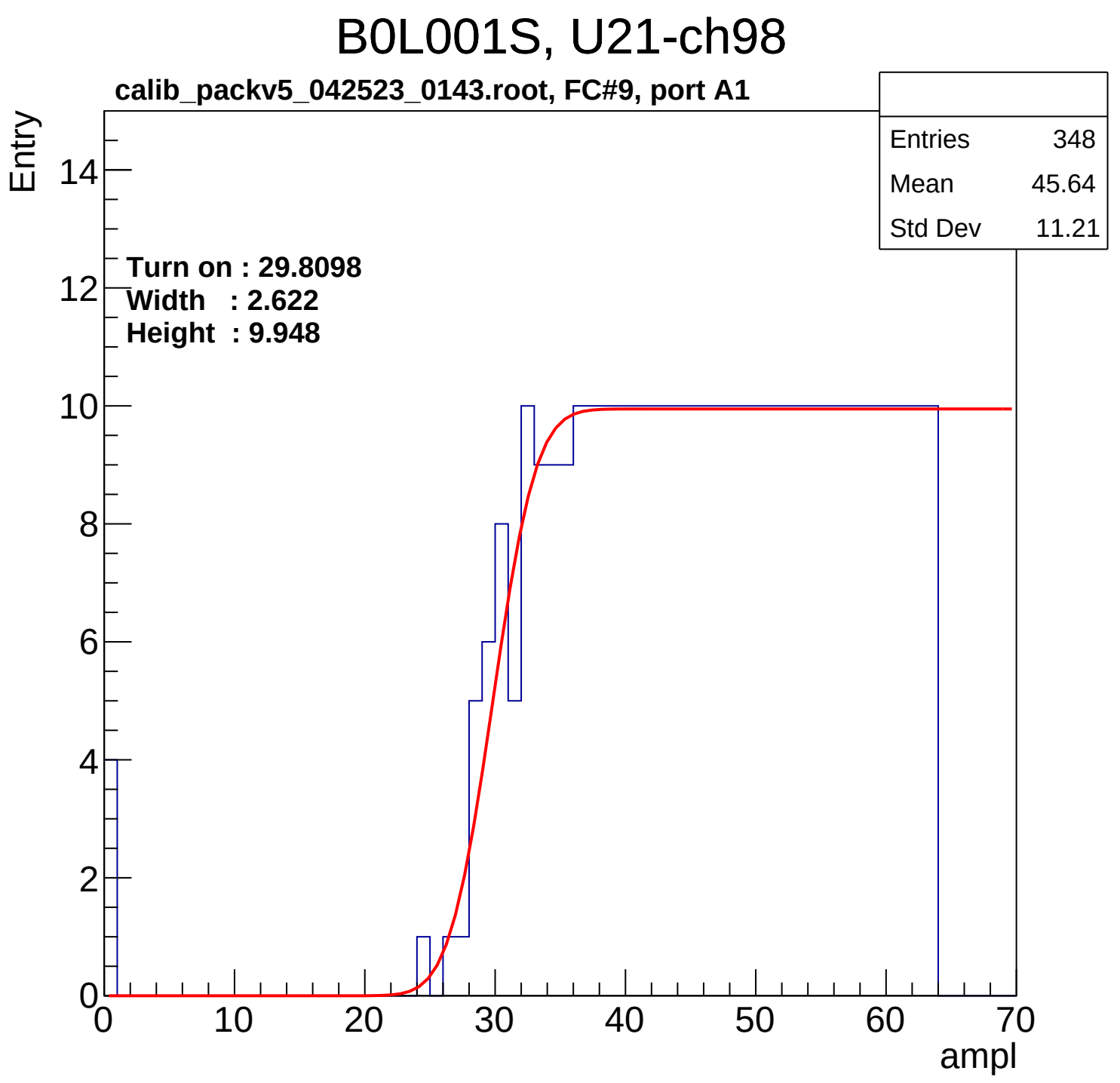
B0L001S, U21-ch98
calib_packv5_042523_0143.root, FC#9, port A1
Entries 348
Mean 45.64
Std Dev 11.21
Turn on : 29.8098
Width : 2.622
Height : 9.948
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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60
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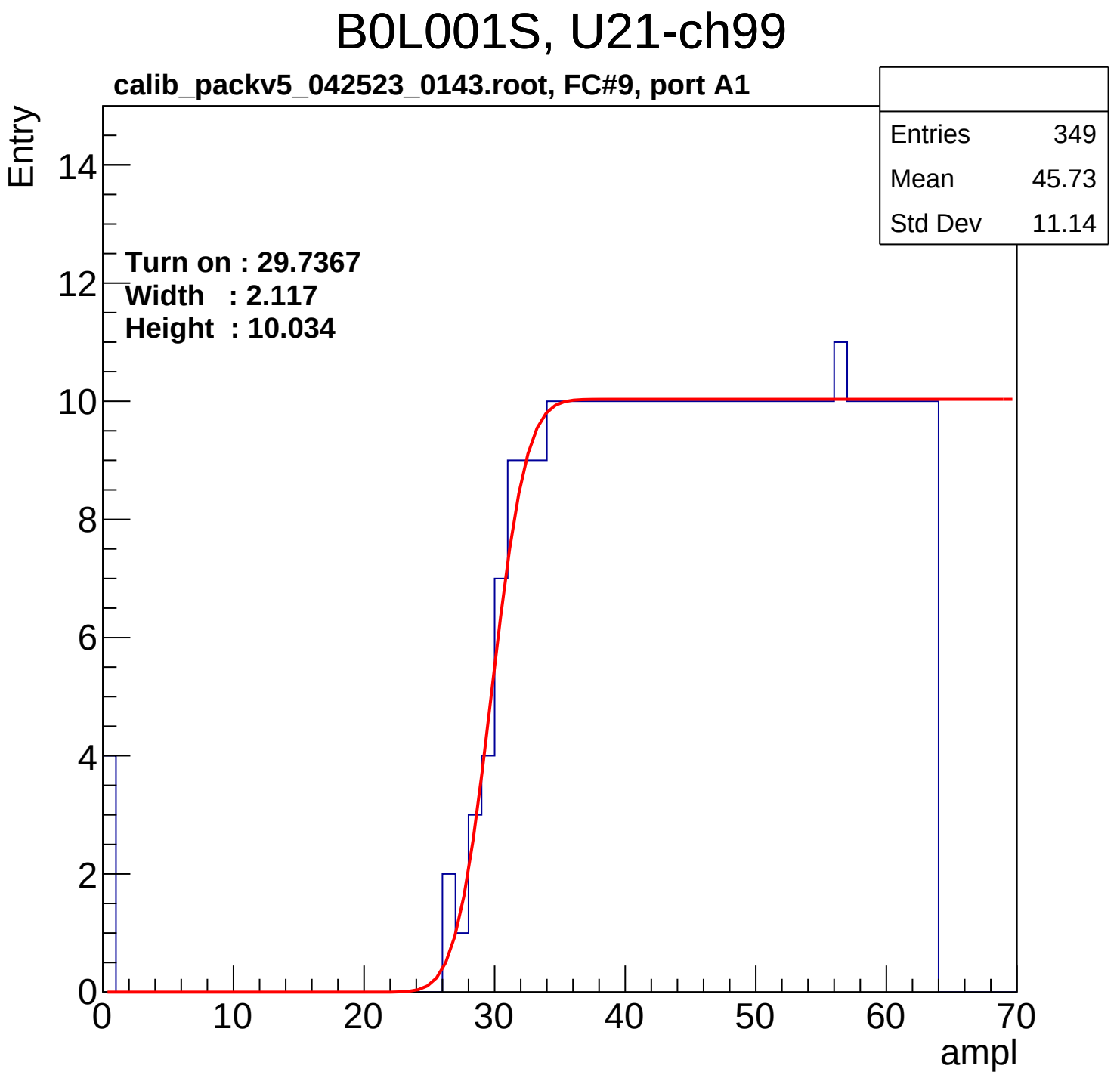
B0L001S, U21-ch99
calib_packv5_042523_0143.root, FC#9, port A1
Entries 349
Mean 45.73
Std Dev 11.14
Turn on : 29.7367
Width : 2.117
Height : 10.034
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
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60
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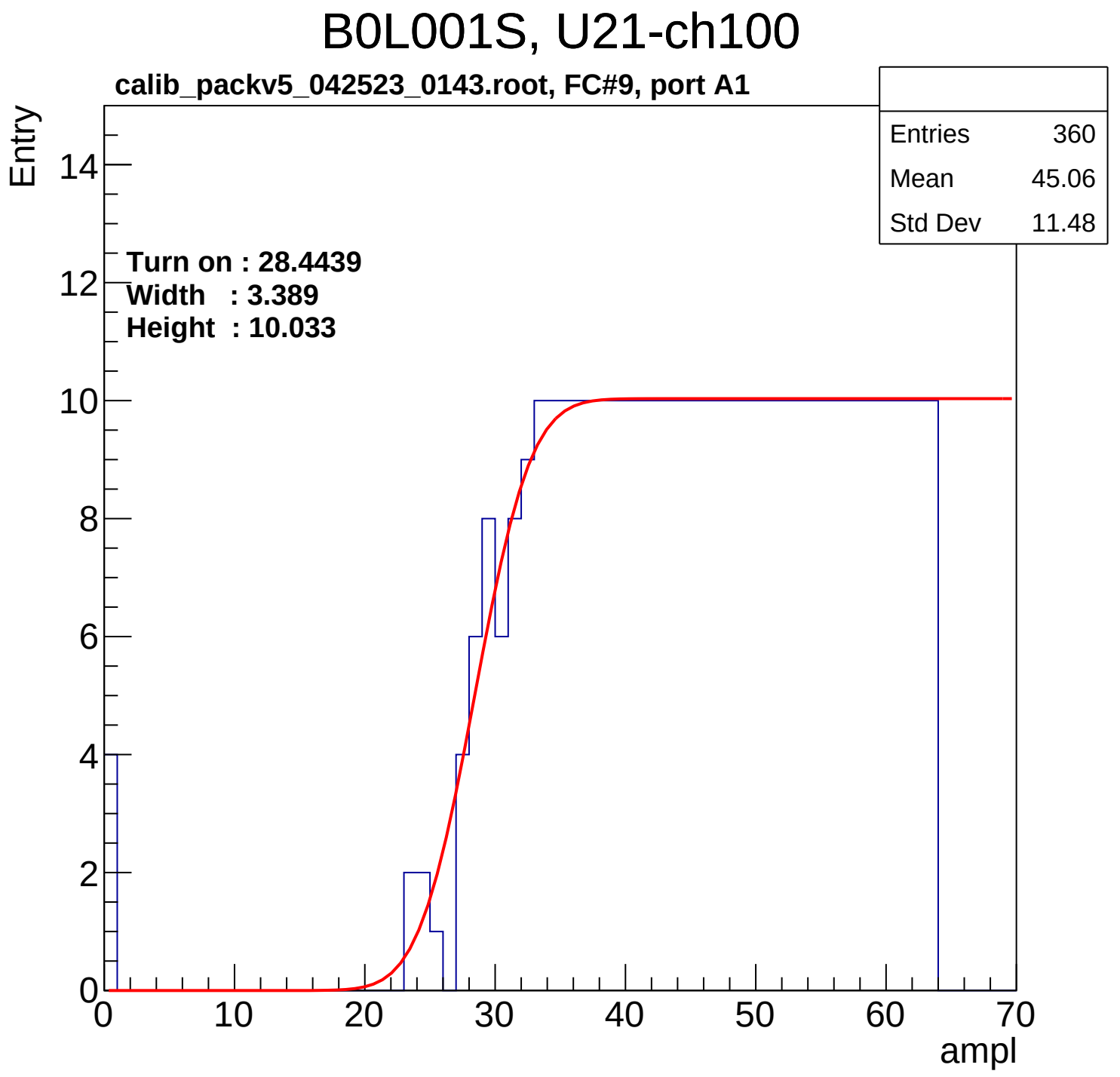
B0L001S, U21-ch100
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 45.06
Std Dev 11.48
Turn on : 28.4439
Width : 3.389
Height : 10.033
Entry
ampl
0
2
4
6
8
10
12
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0
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20
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40
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60
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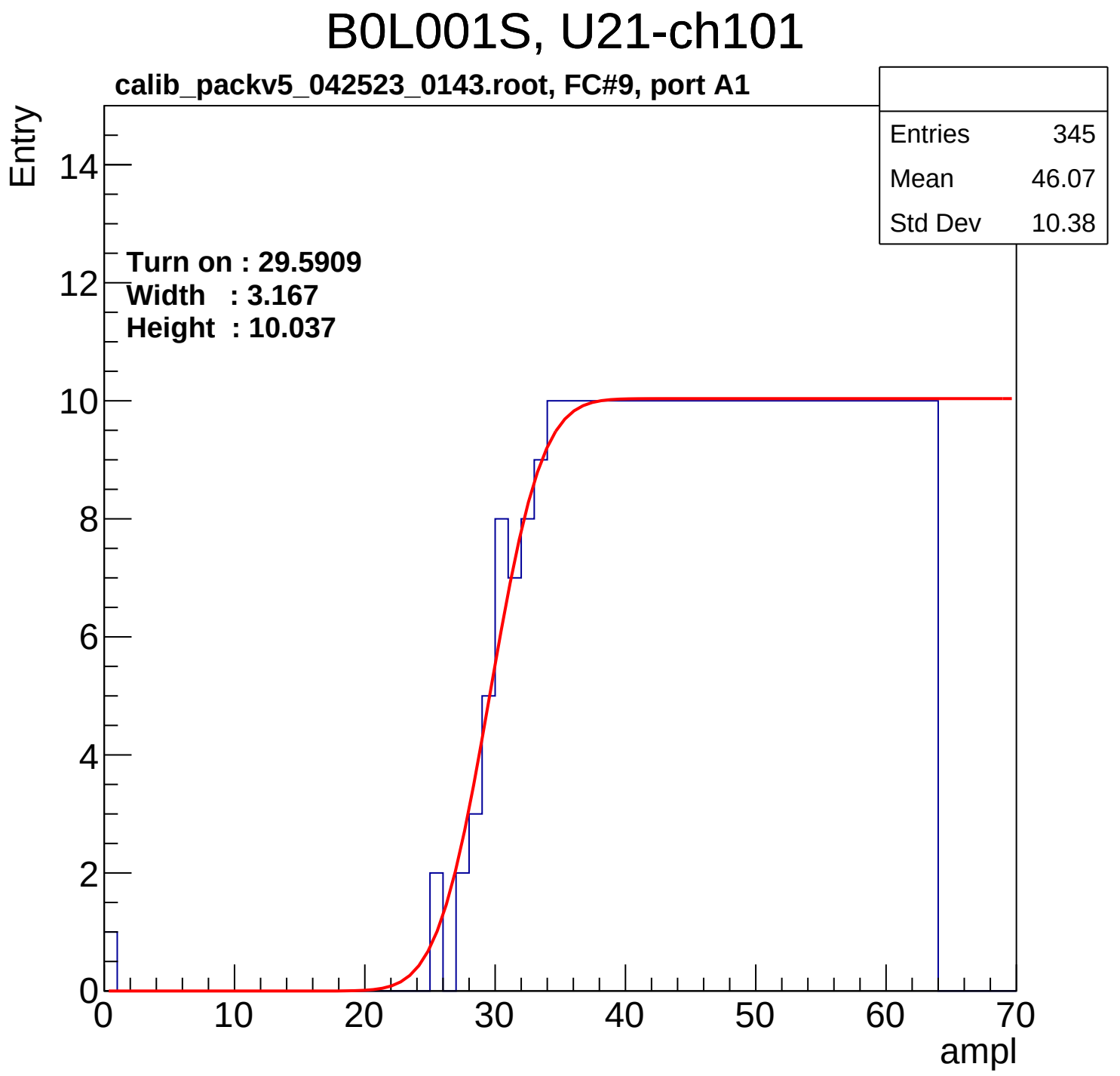
B0L001S, U21-ch101
calib_packv5_042523_0143.root, FC#9, port A1
Entries 345
Mean 46.07
Std Dev 10.38
Turn on : 29.5909
Width : 3.167
Height : 10.037
Entry
ampl
0
2
4
6
8
10
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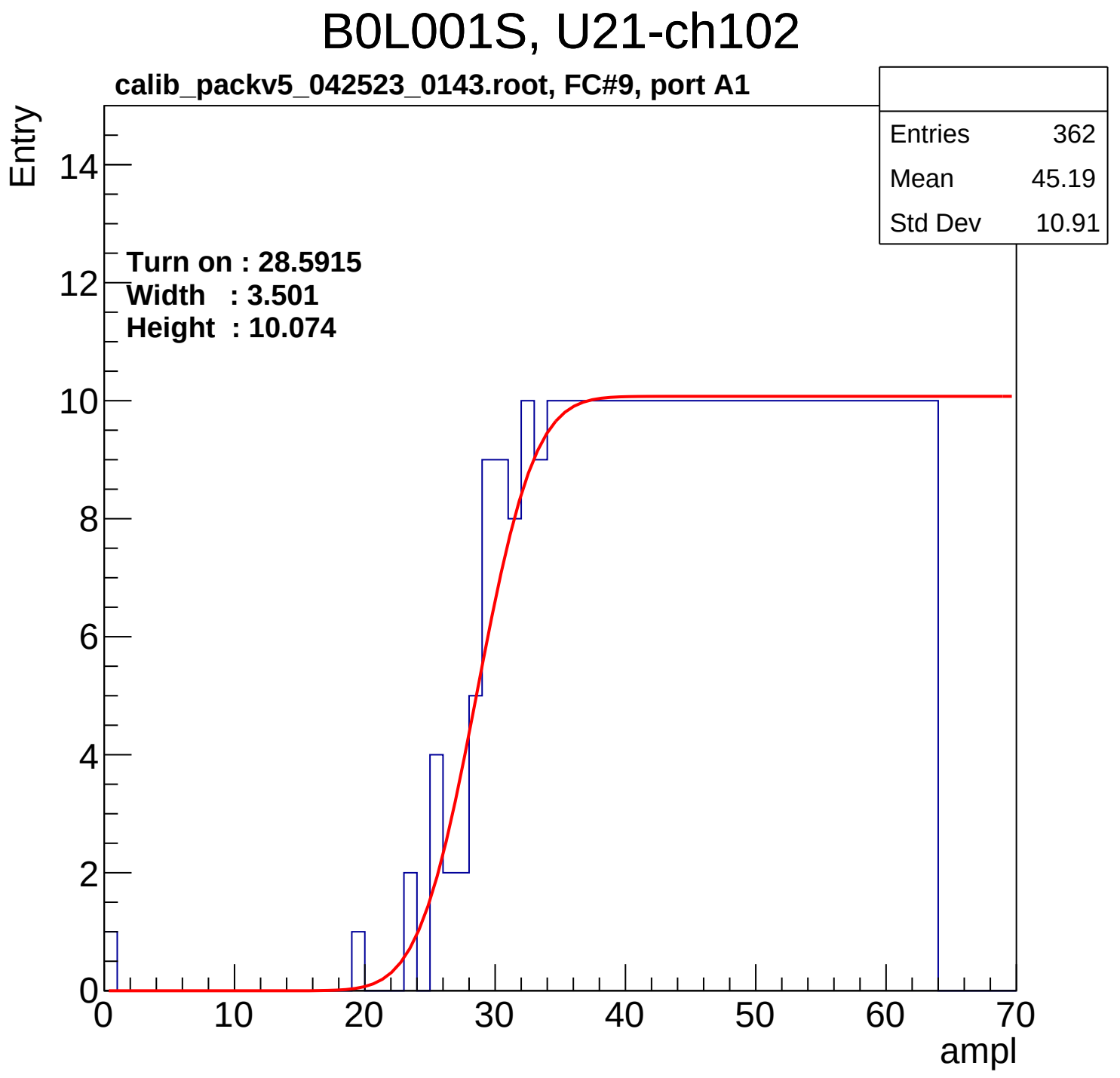
B0L001S, U21-ch102
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 45.19
Std Dev 10.91
Turn on : 28.5915
Width : 3.501
Height : 10.074
Entry
ampl
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6
8
10
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0
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60
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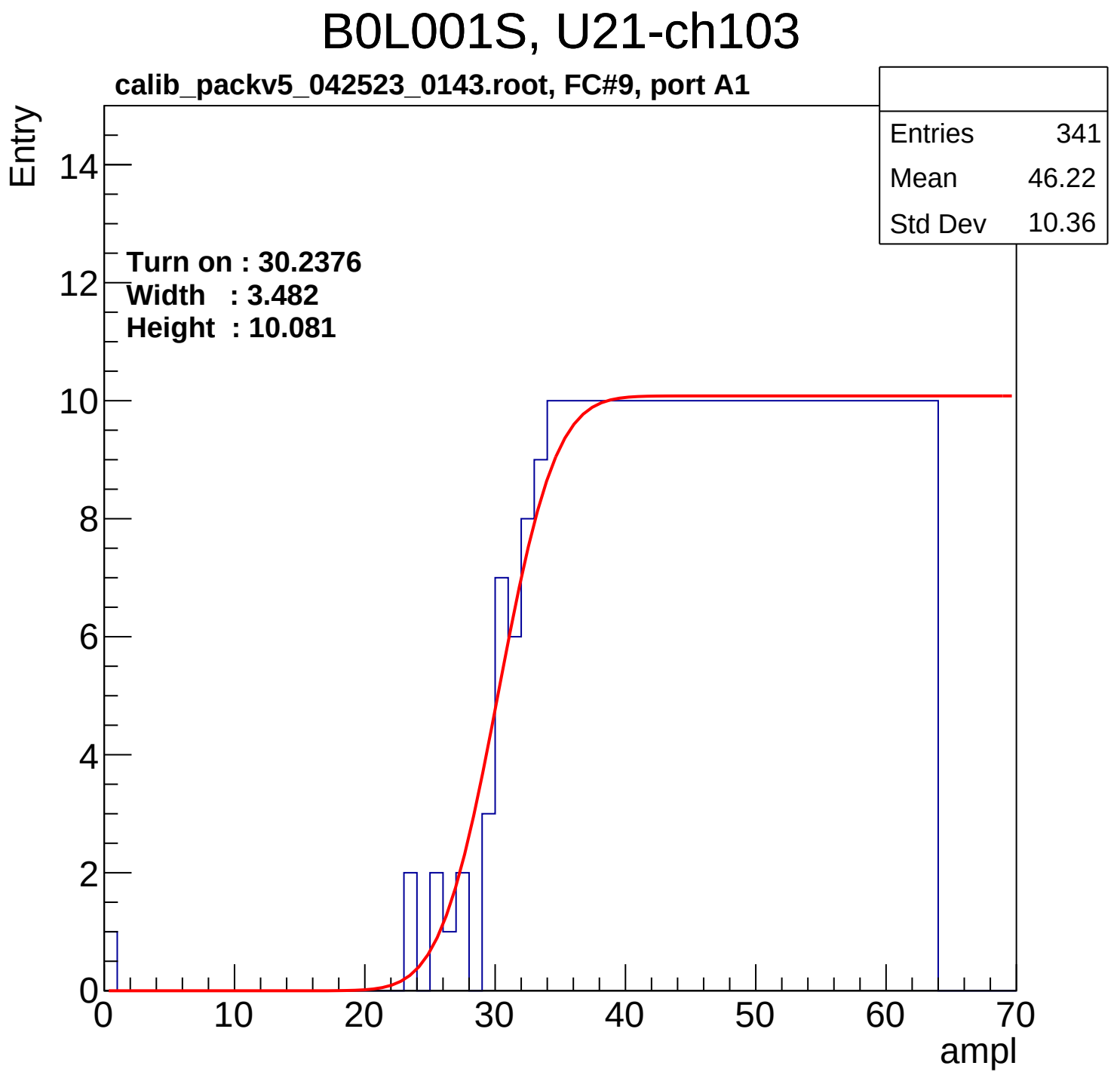
B0L001S, U21-ch103
calib_packv5_042523_0143.root, FC#9, port A1
Entries 341
Mean 46.22
Std Dev 10.36
Turn on : 30.2376
Width : 3.482
Height : 10.081
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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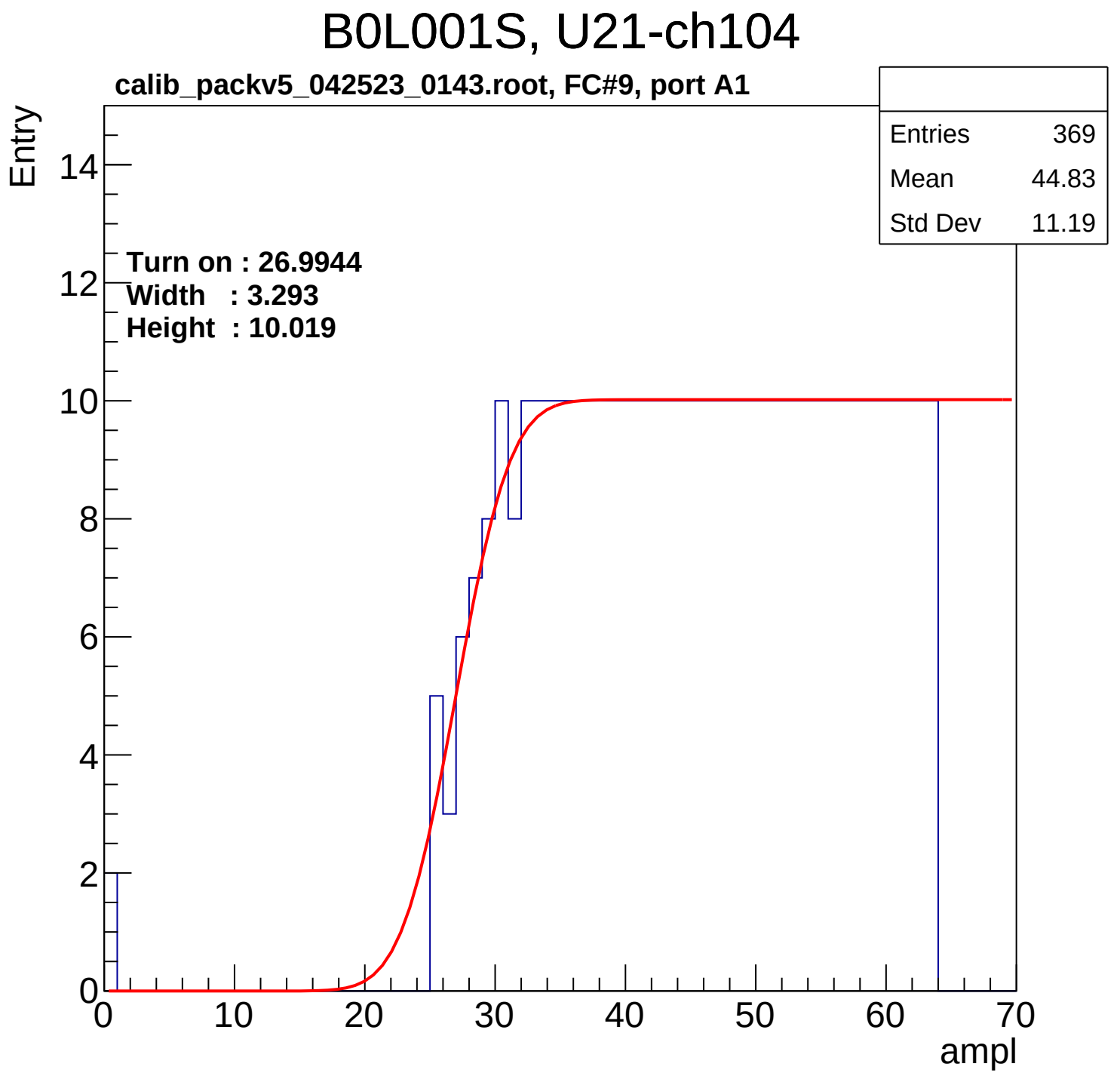
B0L001S, U21-ch104
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.83
Std Dev 11.19
Turn on : 26.9944
Width : 3.293
Height : 10.019
Entry
ampl
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6
8
10
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0
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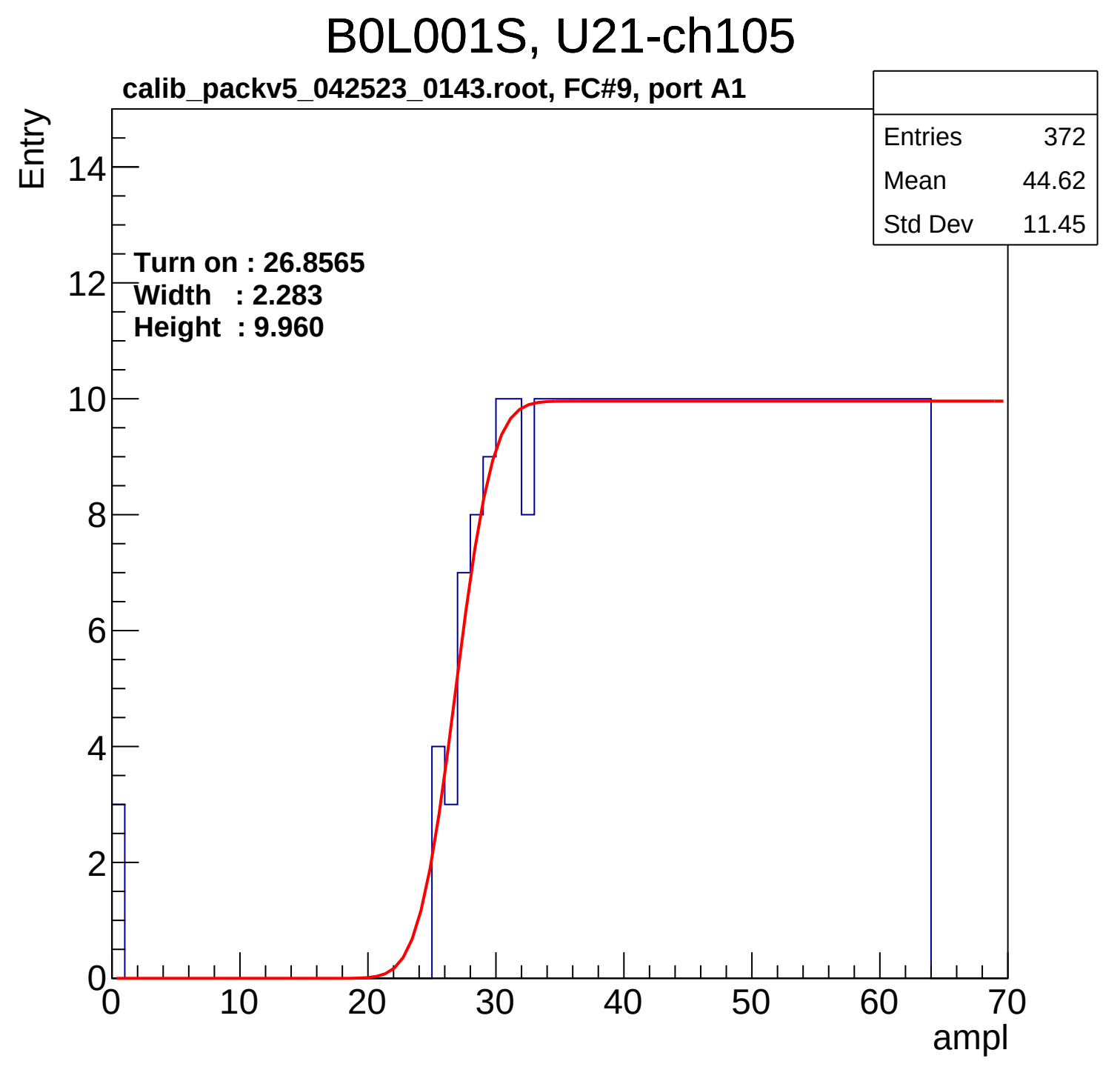
B0L001S, U21-ch105
calib_packv5_042523_0143.root, FC#9, port A1
Entries 372
Mean 44.62
Std Dev 11.45
Turn on : 26.8565
Width : 2.283
Height : 9.960
Entry
ampl
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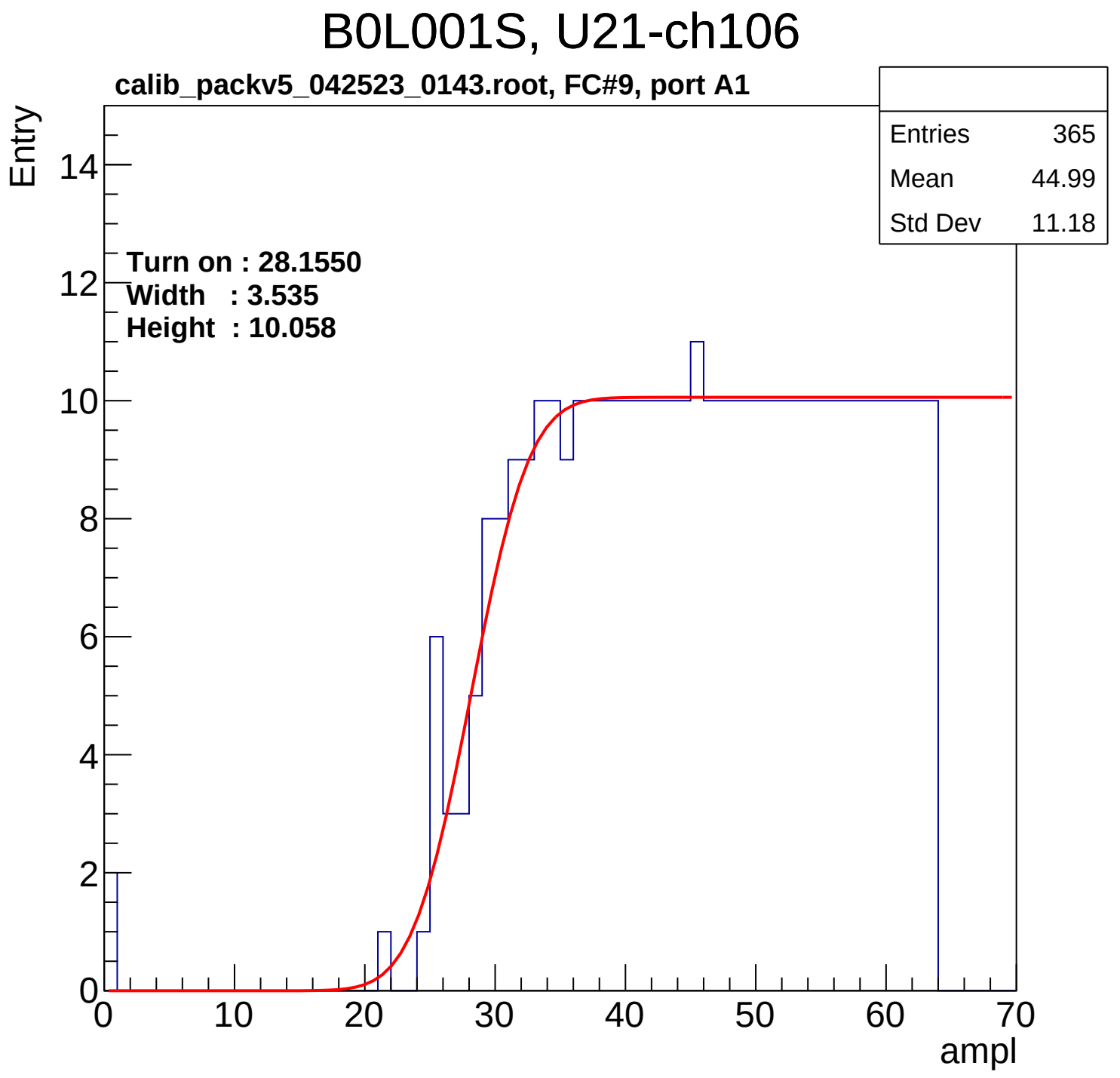
B0L001S, U21-ch106
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 44.99
Std Dev 11.18
Turn on : 28.1550
Width : 3.535
Height : 10.058
Entry
ampl
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8
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0
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60
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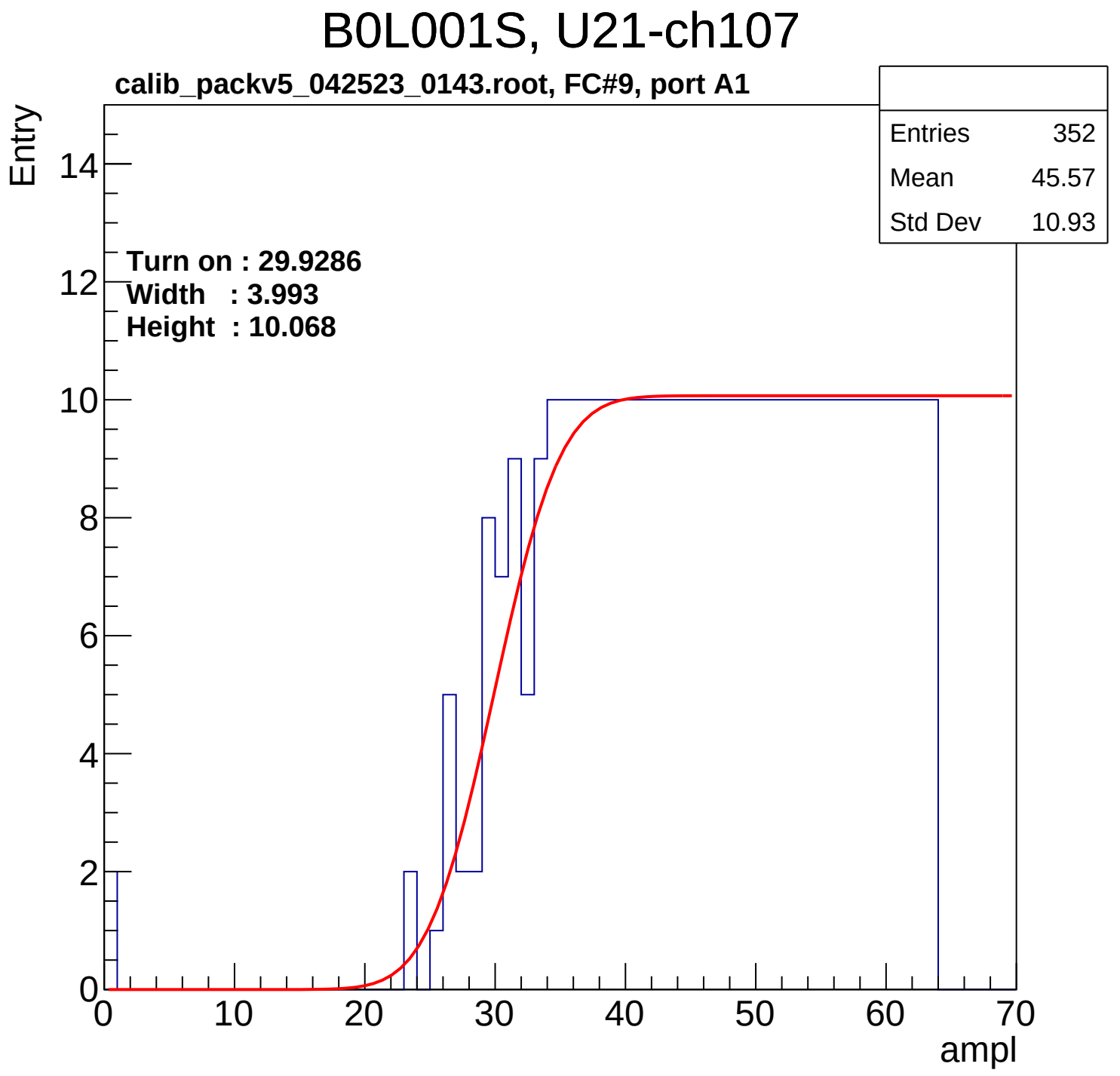
B0L001S, U21-ch107
calib_packv5_042523_0143.root, FC#9, port A1
Entries 352
Mean 45.57
Std Dev 10.93
Turn on : 29.9286
Width : 3.993
Height : 10.068
Entry
ampl
0
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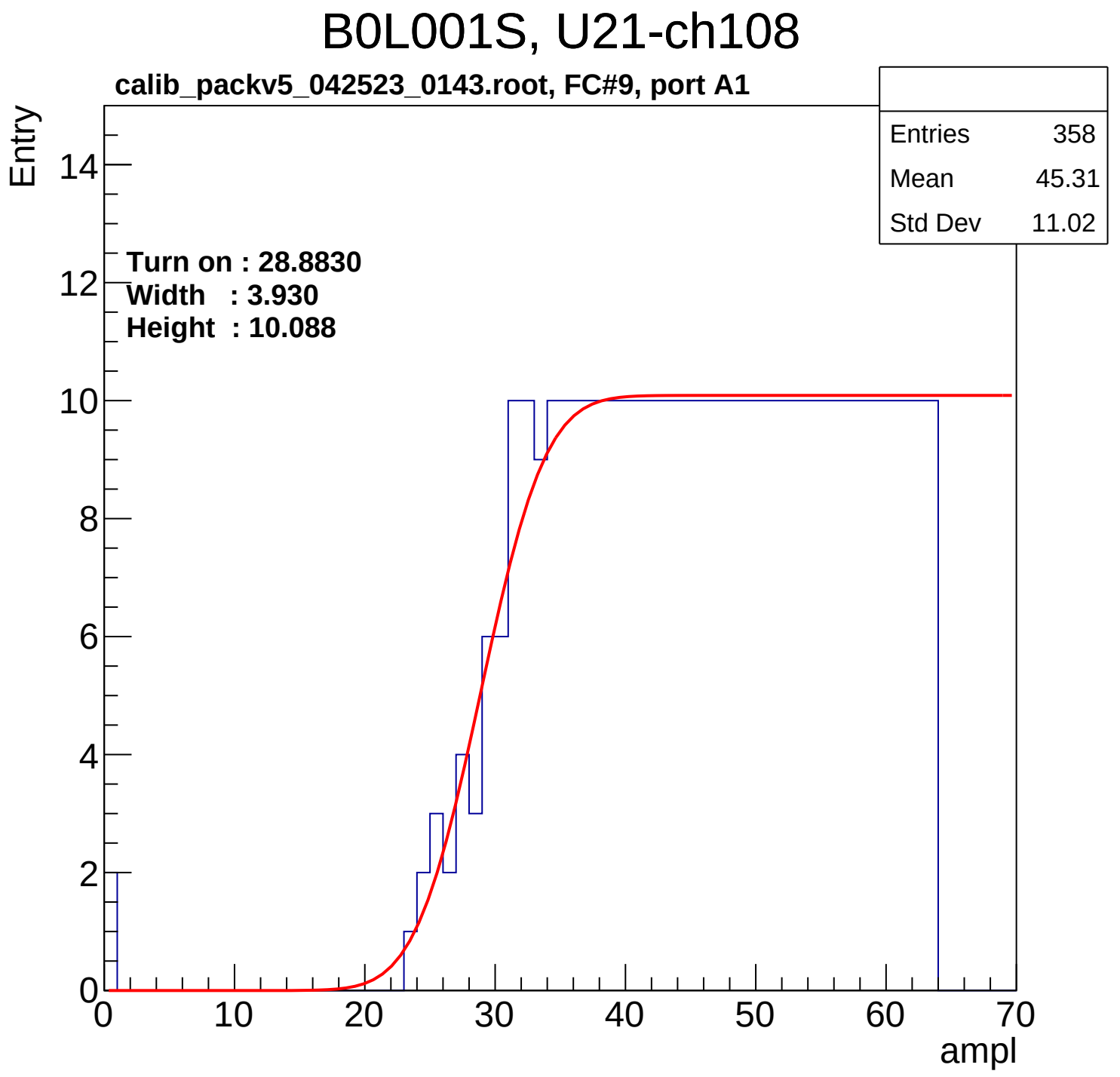
B0L001S, U21-ch108
calib_packv5_042523_0143.root, FC#9, port A1
Entries 358
Mean 45.31
Std Dev 11.02
Turn on : 28.8830
Width : 3.930
Height : 10.088
Entry
ampl
0
2
4
6
8
10
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0
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60
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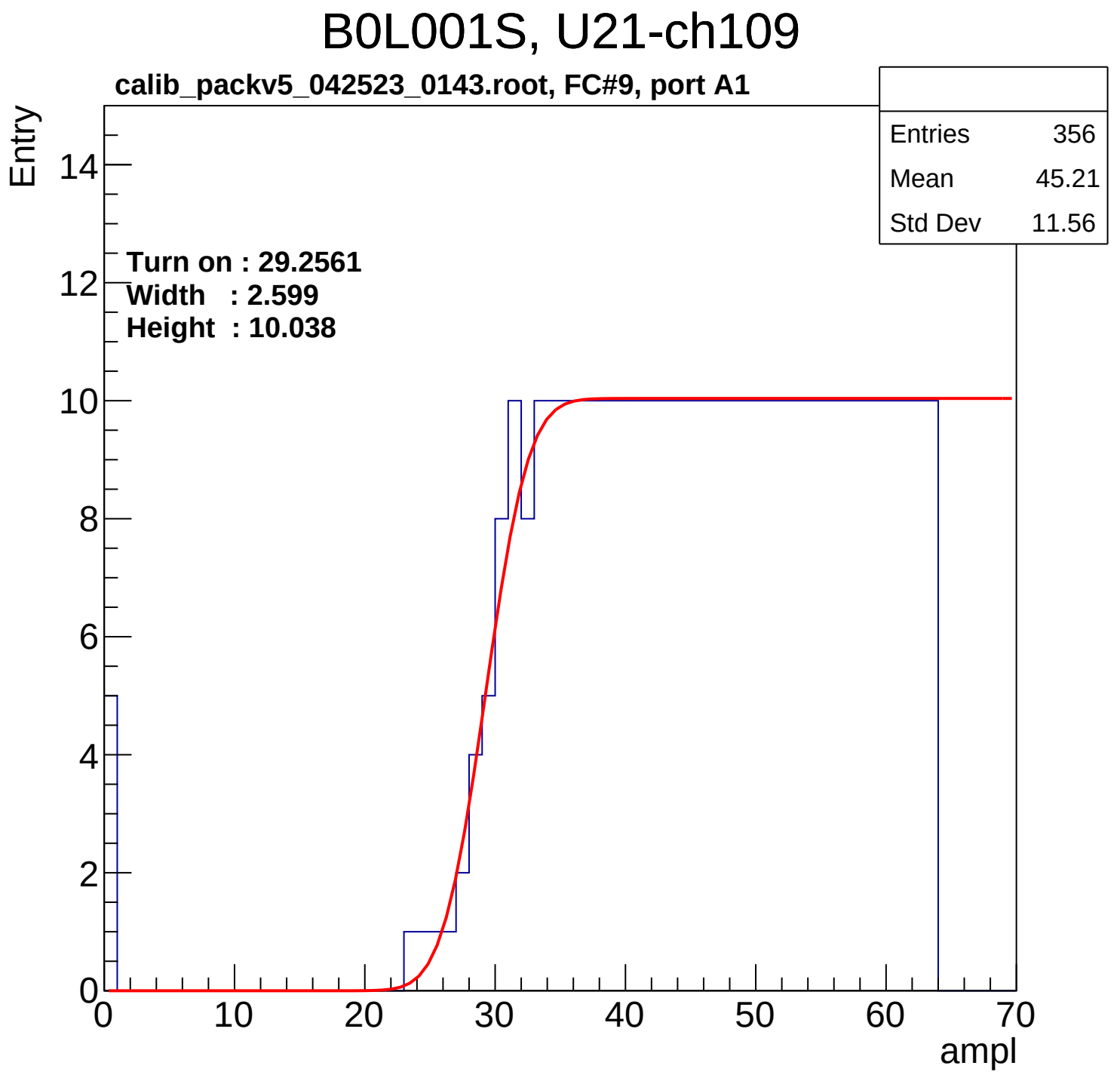
B0L001S, U21-ch109
calib_packv5_042523_0143.root, FC#9, port A1
Entries 356
Mean 45.21
Std Dev 11.56
Turn on : 29.2561
Width : 2.599
Height : 10.038
Entry
ampl
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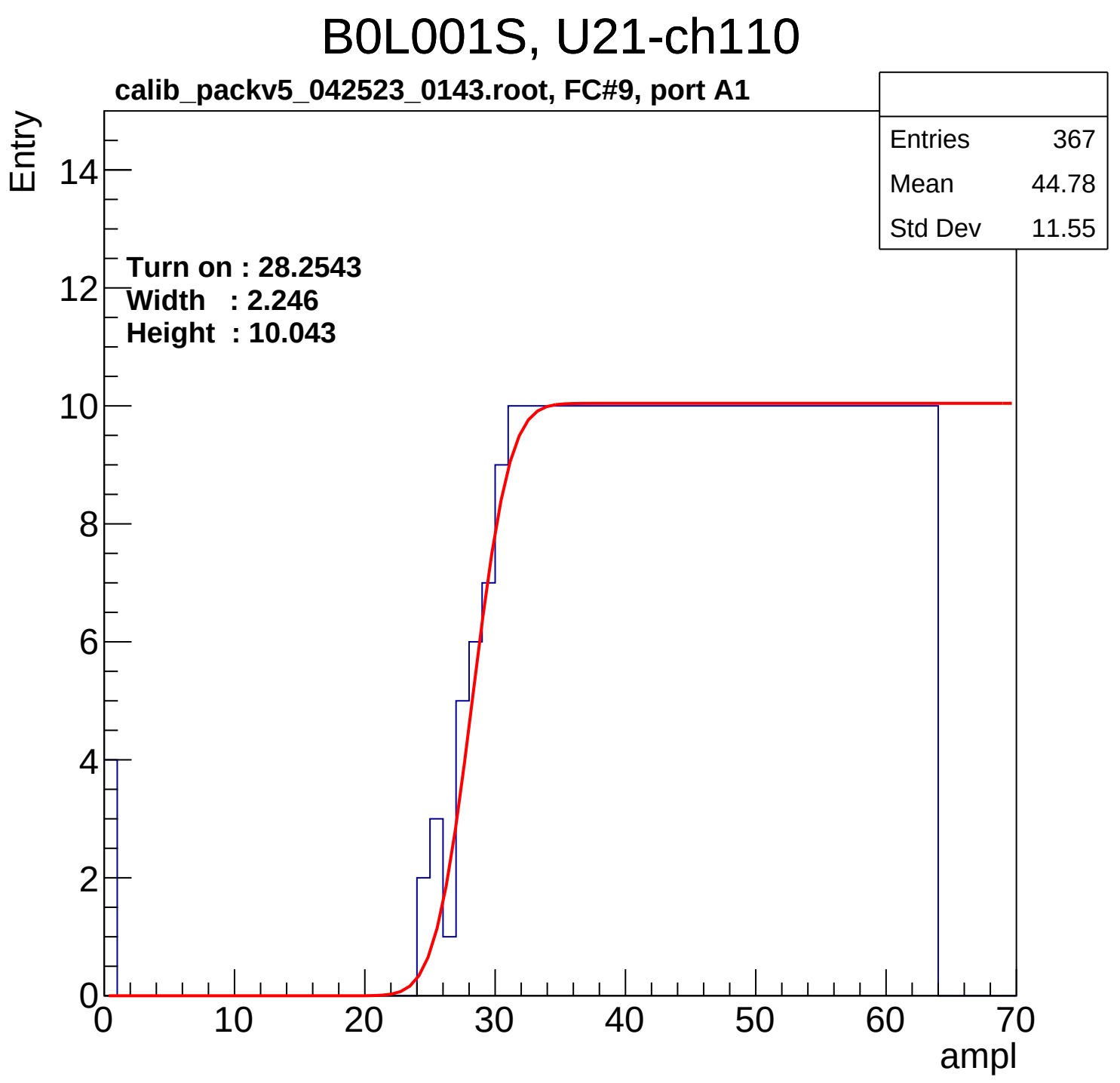
B0L001S, U21-ch110
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.78
Std Dev 11.55
Turn on : 28.2543
Width : 2.246
Height : 10.043
Entry
ampl
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2
4
6
8
10
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0
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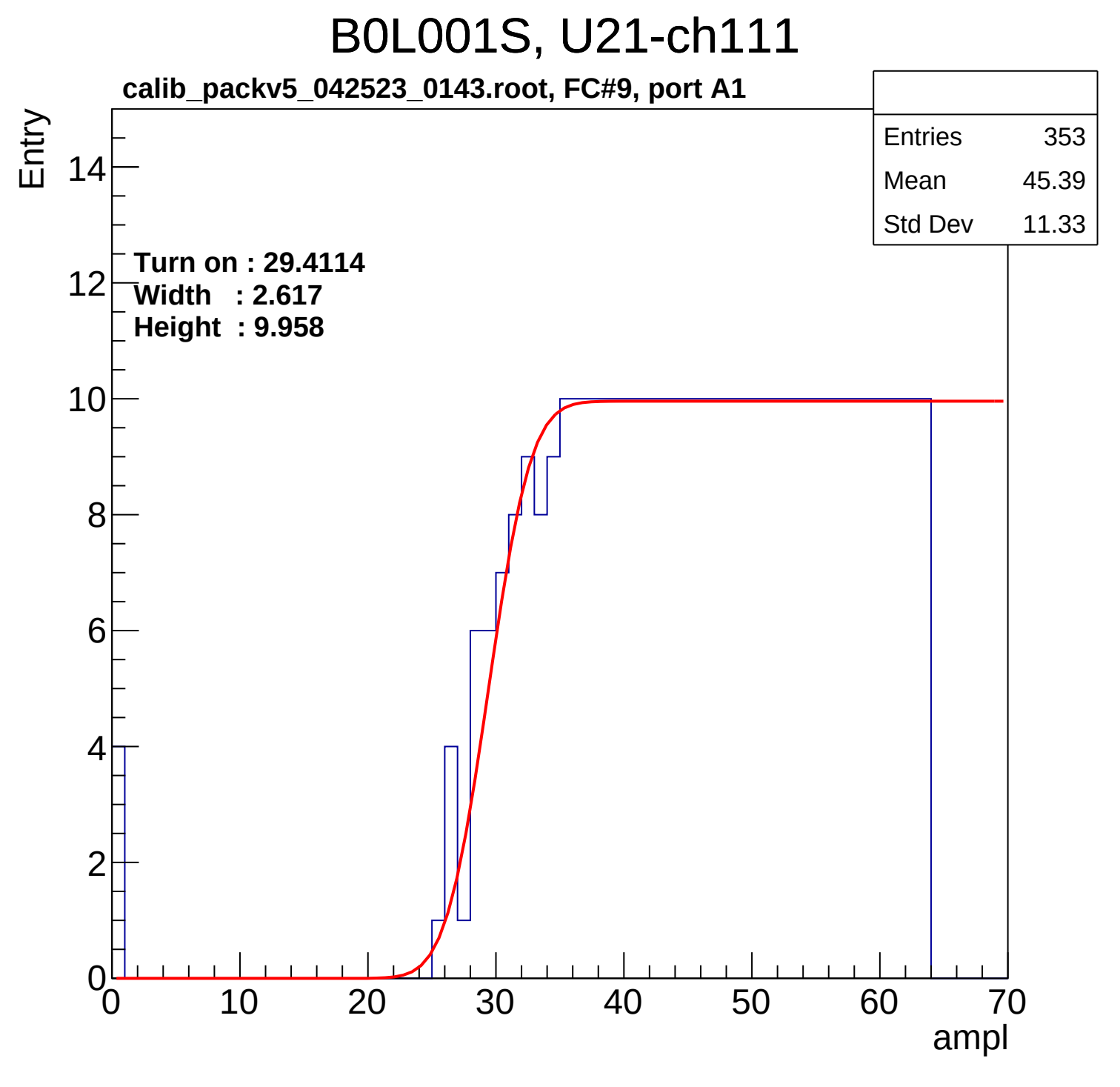
B0L001S, U21-ch111
calib_packv5_042523_0143.root, FC#9, port A1
Entries 353
Mean 45.39
Std Dev 11.33
Turn on : 29.4114
Width : 2.617
Height : 9.958
Entry
ampl
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6
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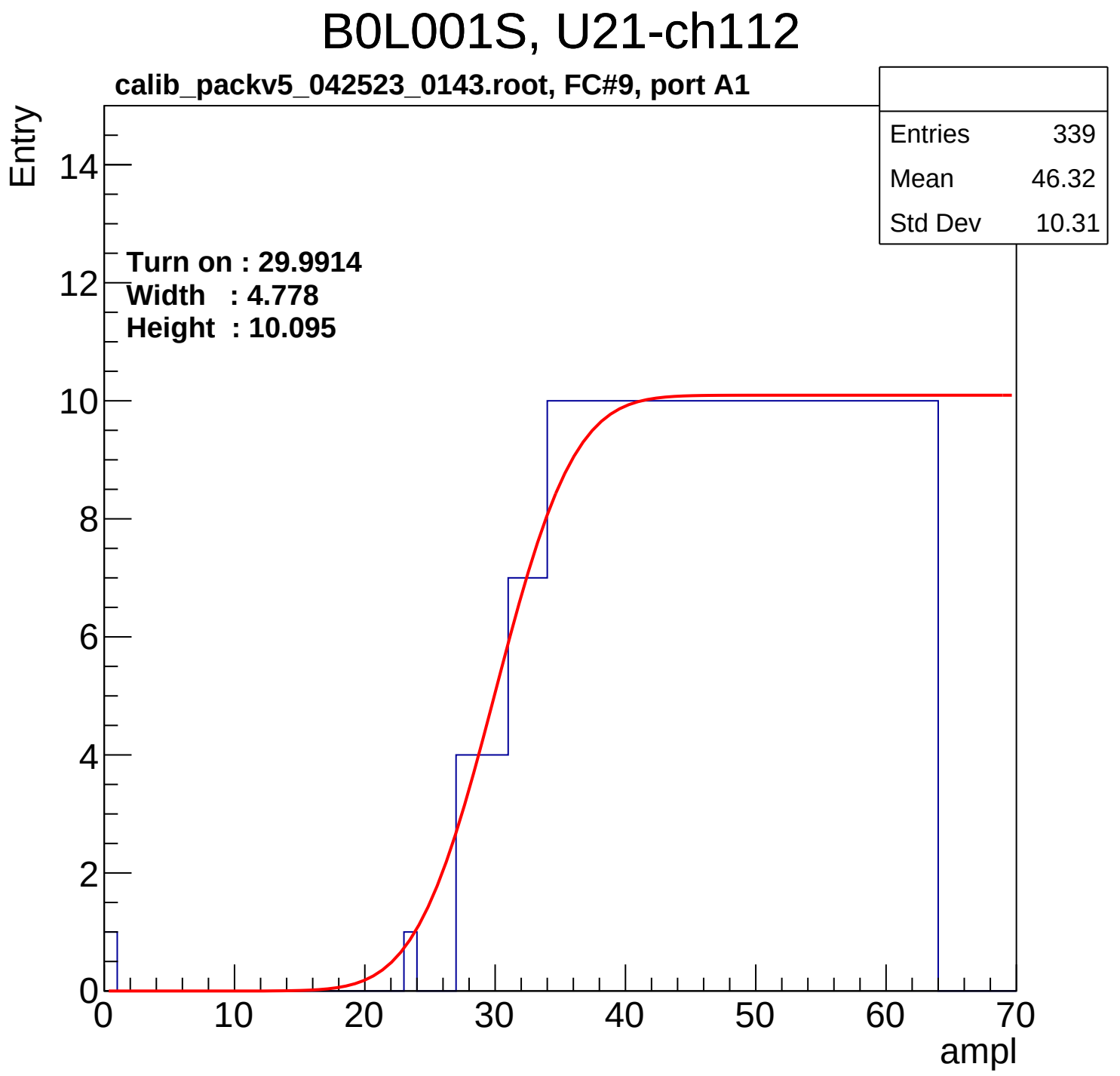
B0L001S, U21-ch112
calib_packv5_042523_0143.root, FC#9, port A1
Entries 339
Mean 46.32
Std Dev 10.31
Turn on : 29.9914
Width : 4.778
Height : 10.095
Entry
ampl
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6
8
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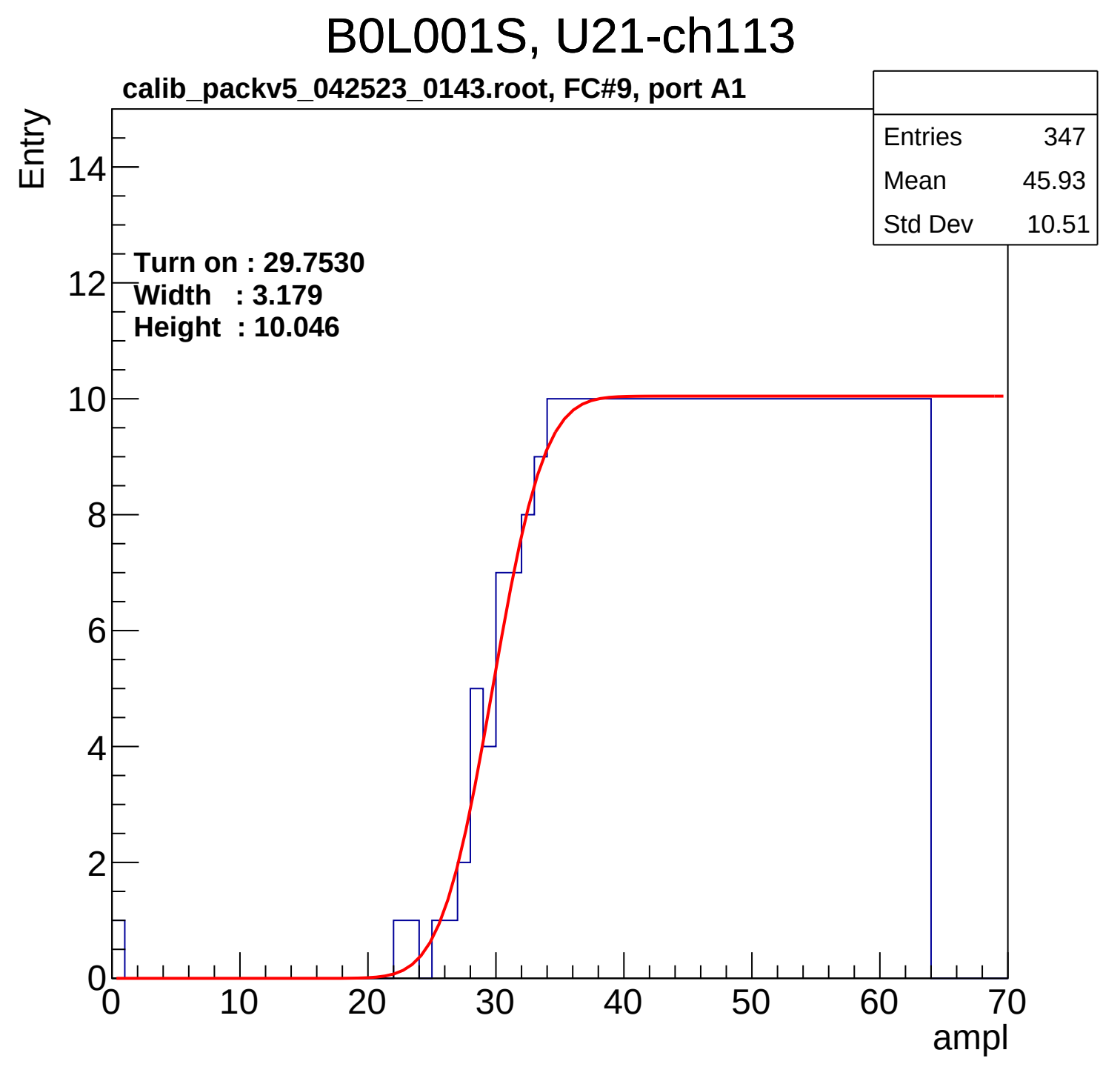
B0L001S, U21-ch113
calib_packv5_042523_0143.root, FC#9, port A1
Entries 347
Mean 45.93
Std Dev 10.51
Turn on : 29.7530
Width : 3.179
Height : 10.046
Entry
ampl
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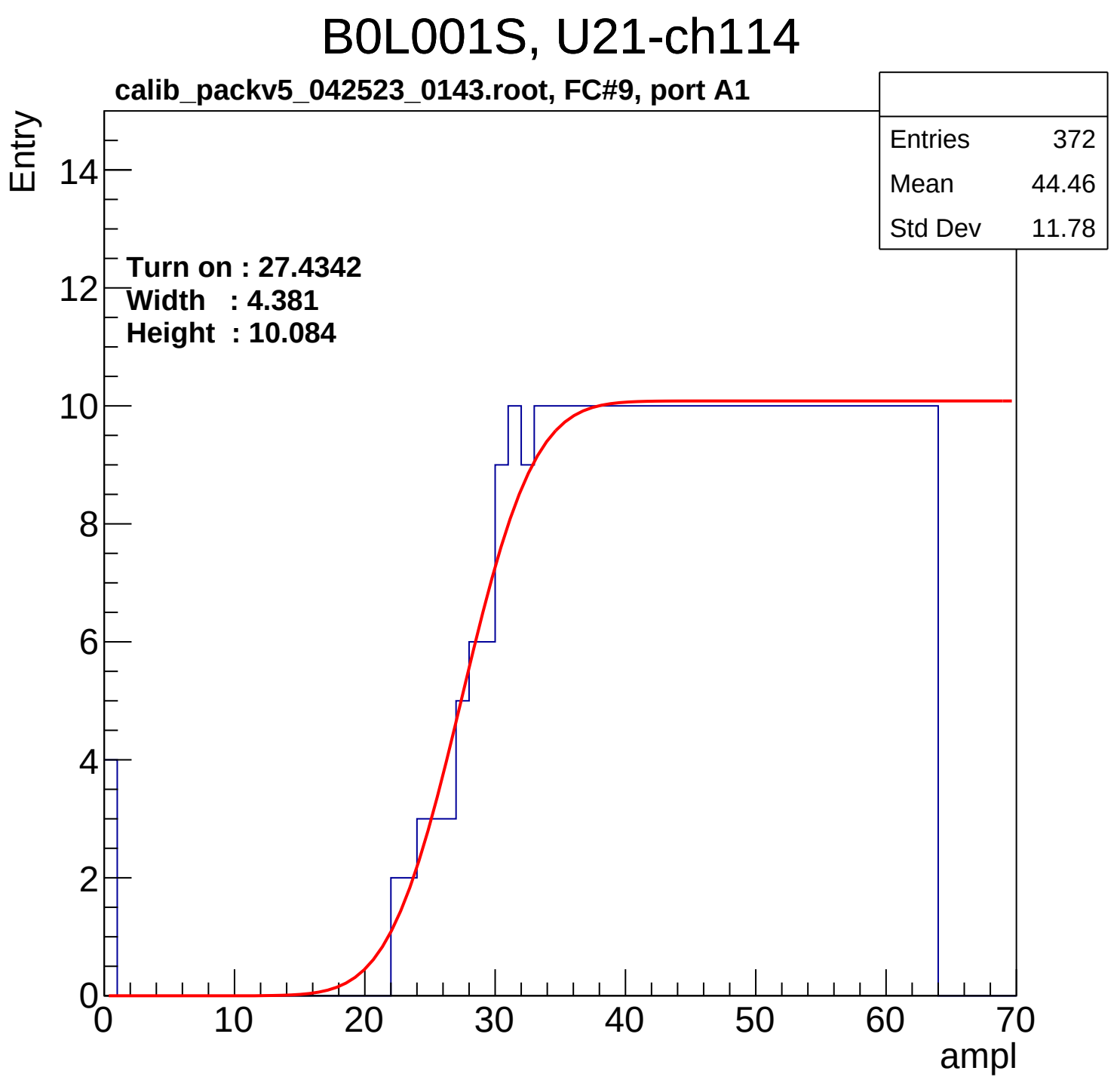
B0L001S, U21-ch114
calib_packv5_042523_0143.root, FC#9, port A1
Entries 372
Mean 44.46
Std Dev 11.78
Turn on : 27.4342
Width : 4.381
Height : 10.084
Entry
ampl
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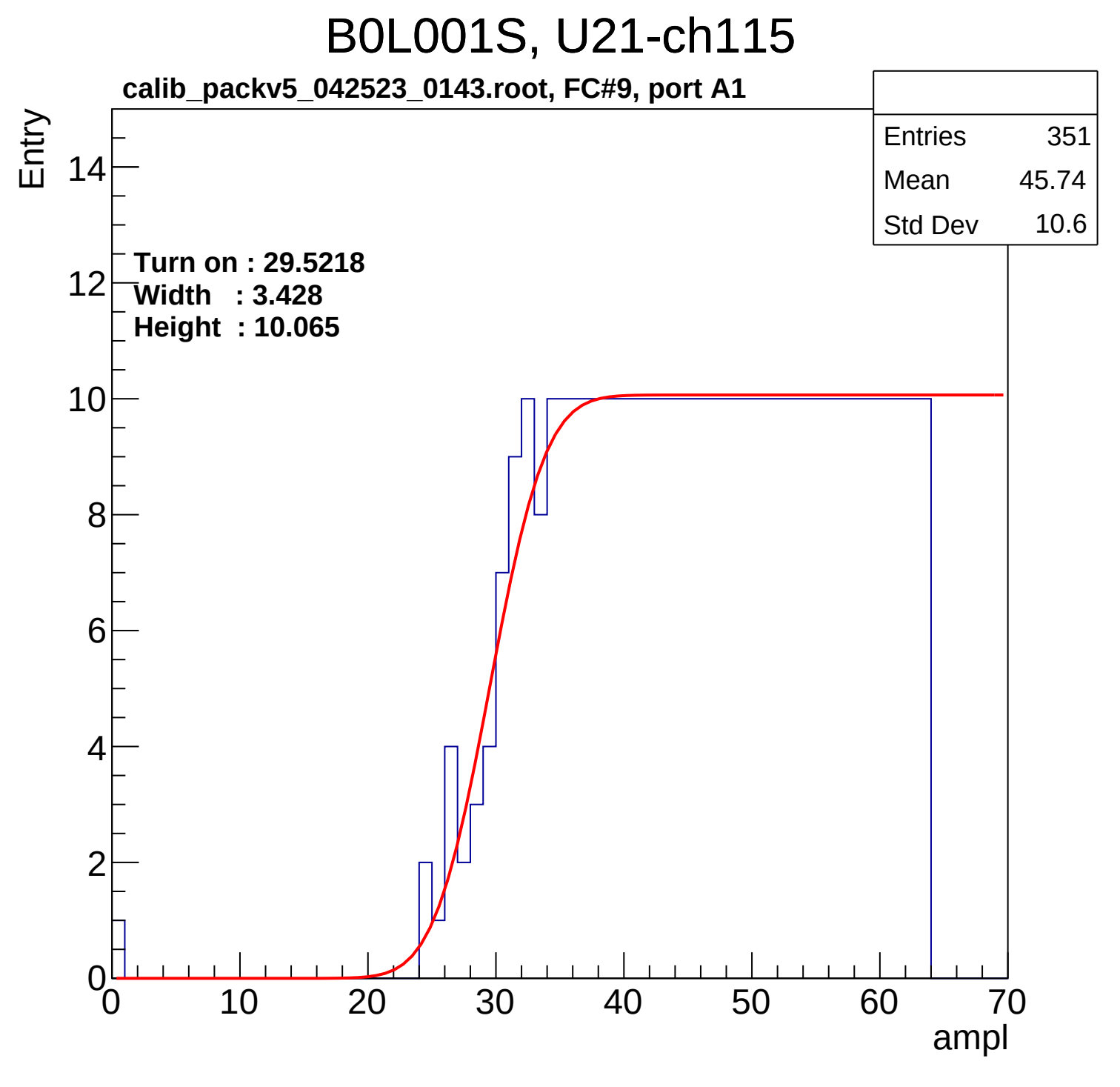
B0L001S, U21-ch115
calib_packv5_042523_0143.root, FC#9, port A1
Entries 351
Mean 45.74
Std Dev 10.6
Turn on : 29.5218
Width : 3.428
Height : 10.065
Entry
ampl
0
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4
6
8
10
12
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0
10
20
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40
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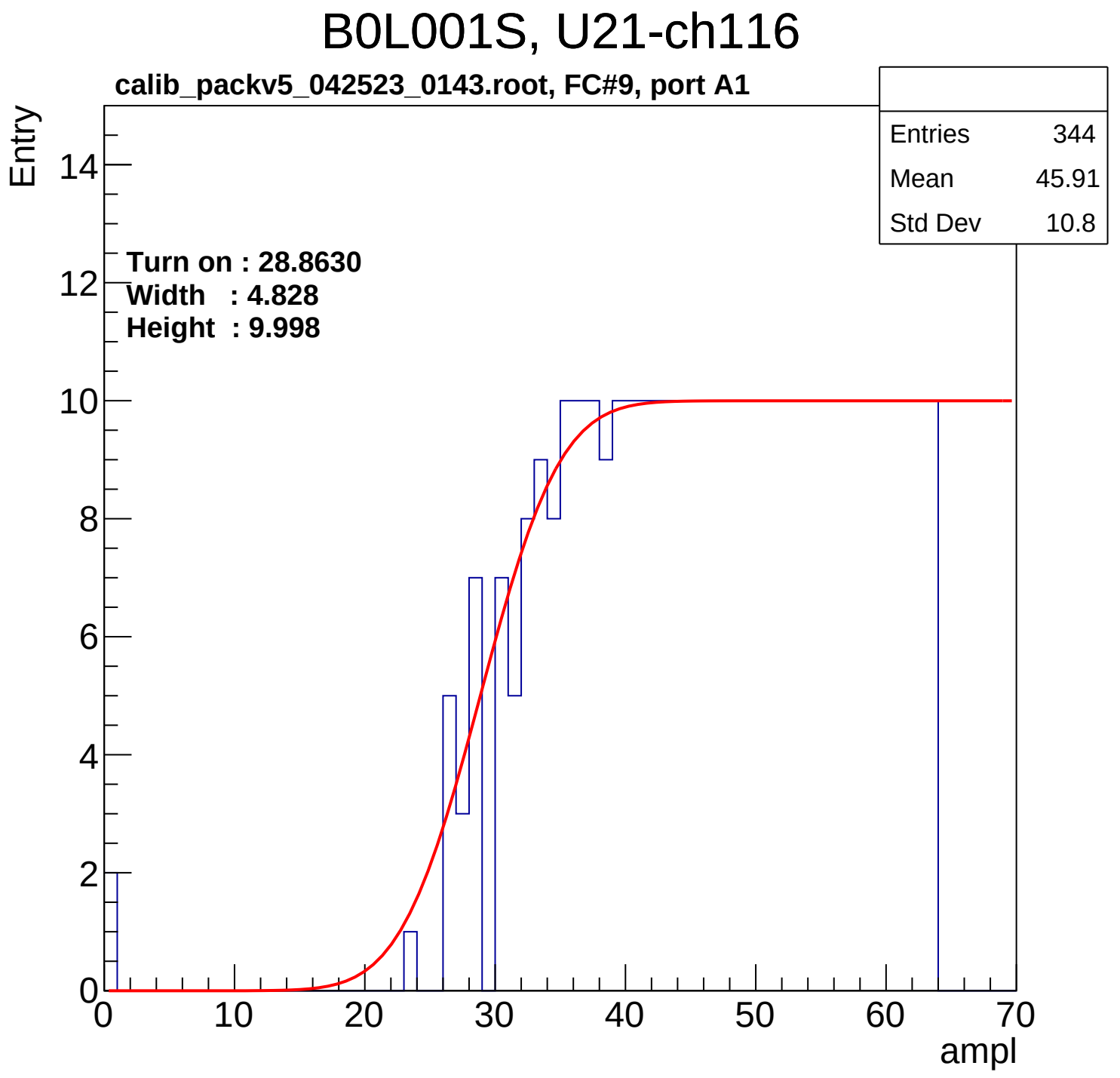
B0L001S, U21-ch116
calib_packv5_042523_0143.root, FC#9, port A1
Entries 344
Mean 45.91
Std Dev 10.8
Turn on : 28.8630
Width : 4.828
Height : 9.998
Entry
ampl
0
2
4
6
8
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0
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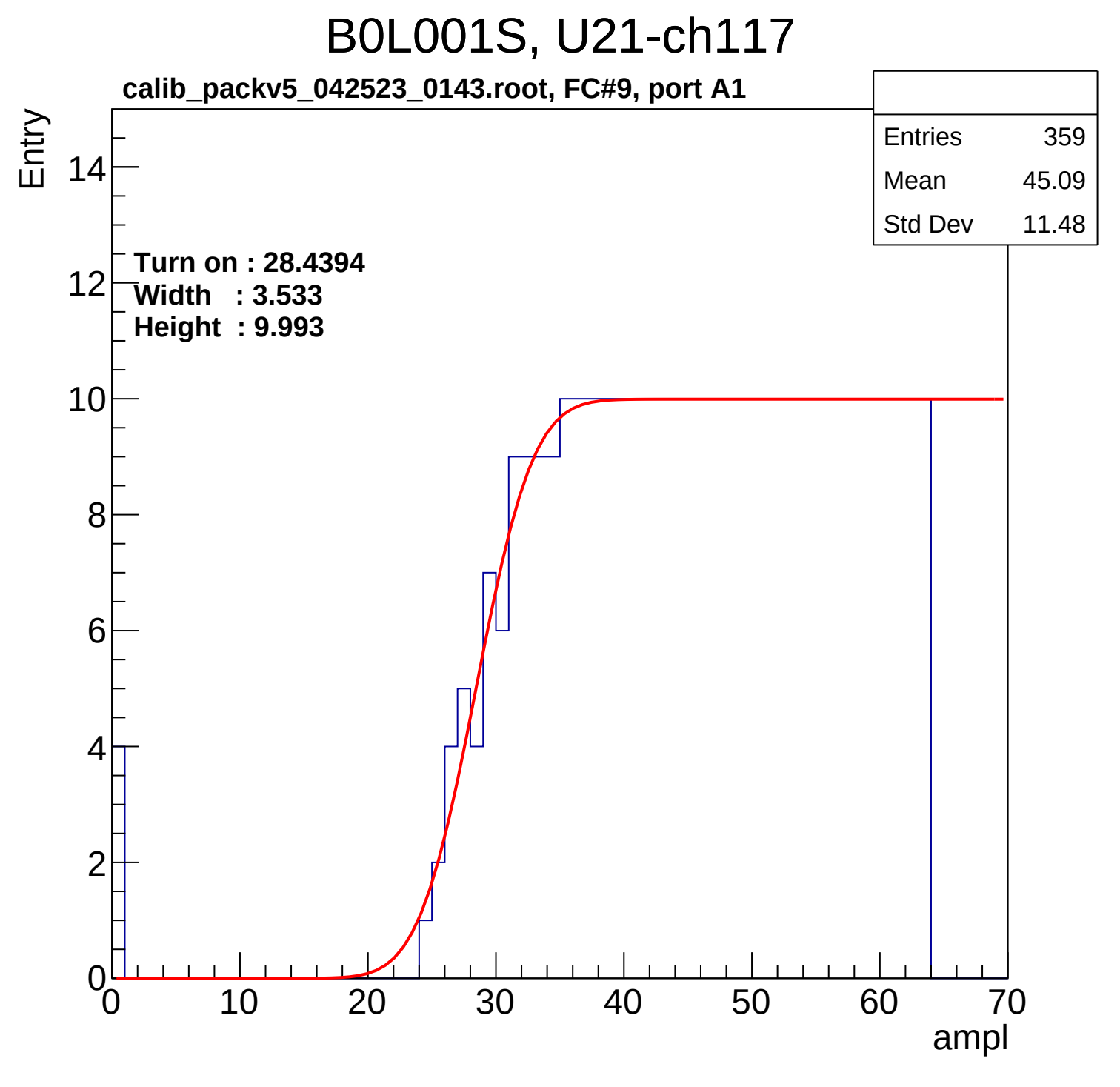
B0L001S, U21-ch117
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 45.09
Std Dev 11.48
Turn on : 28.4394
Width : 3.533
Height : 9.993
Entry
ampl
0
2
4
6
8
10
12
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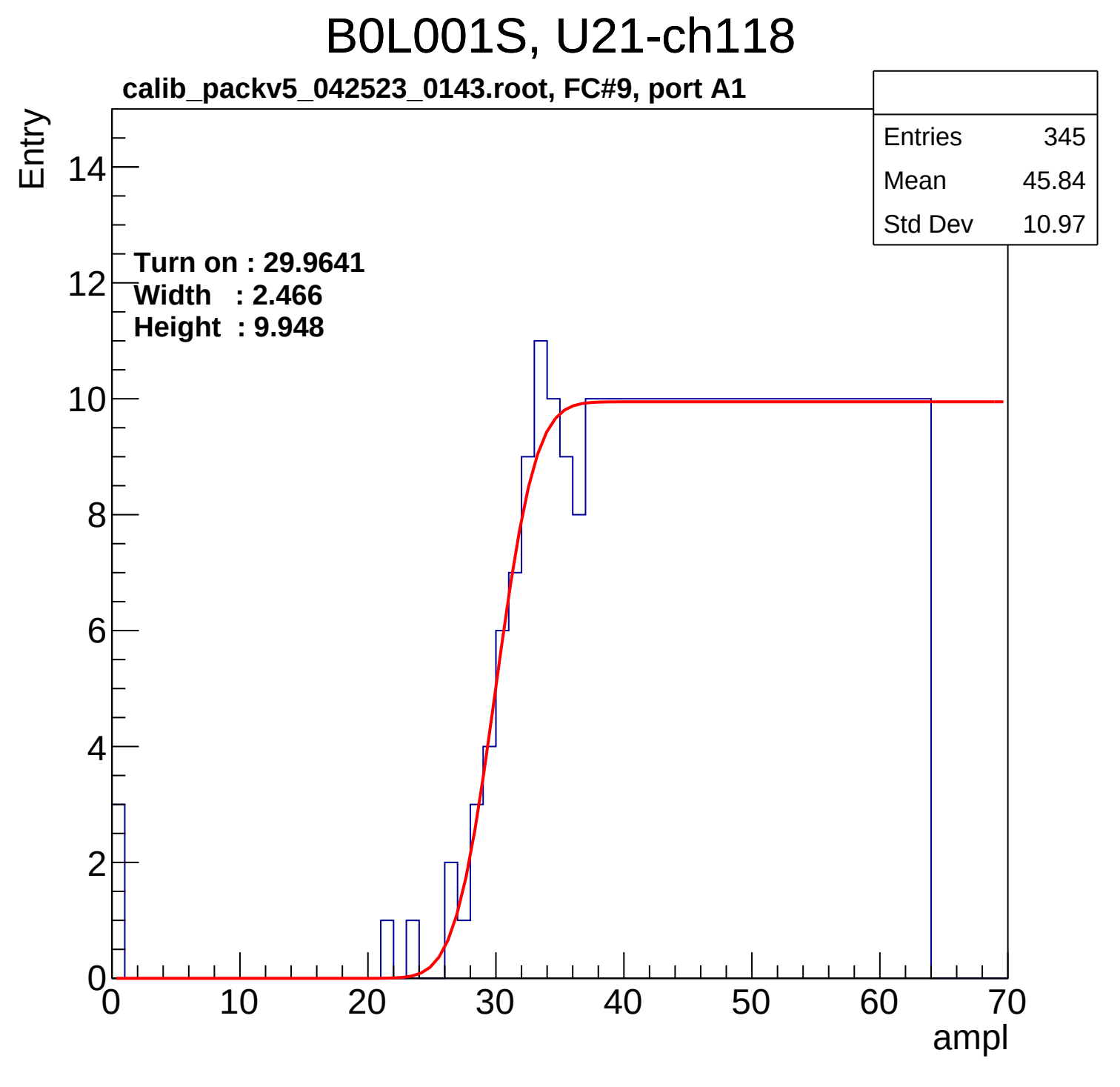
B0L001S, U21-ch118
calib_packv5_042523_0143.root, FC#9, port A1
Entries 345
Mean 45.84
Std Dev 10.97
Turn on : 29.9641
Width : 2.466
Height : 9.948
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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60
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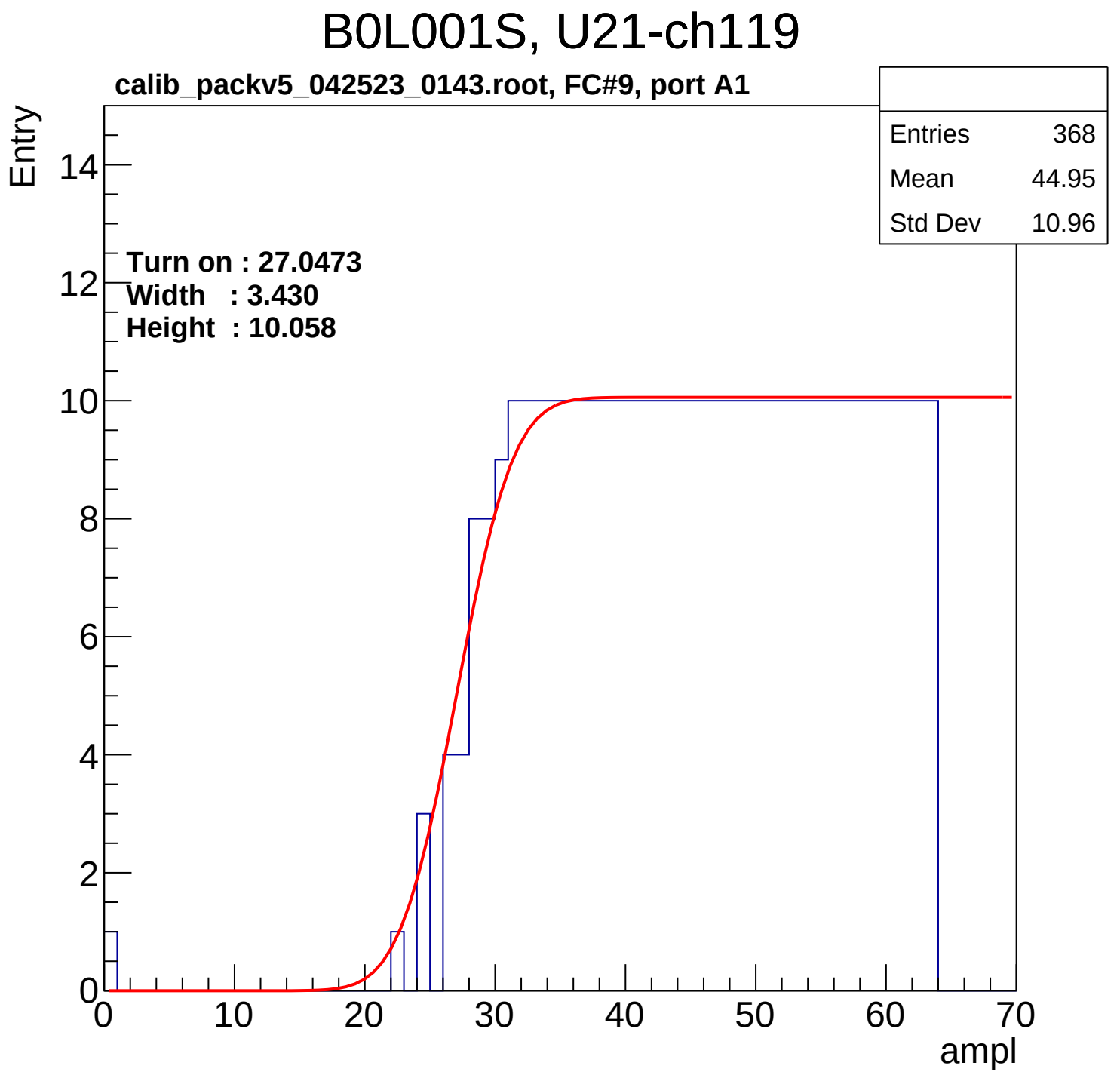
B0L001S, U21-ch119
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.95
Std Dev 10.96
Turn on : 27.0473
Width : 3.430
Height : 10.058
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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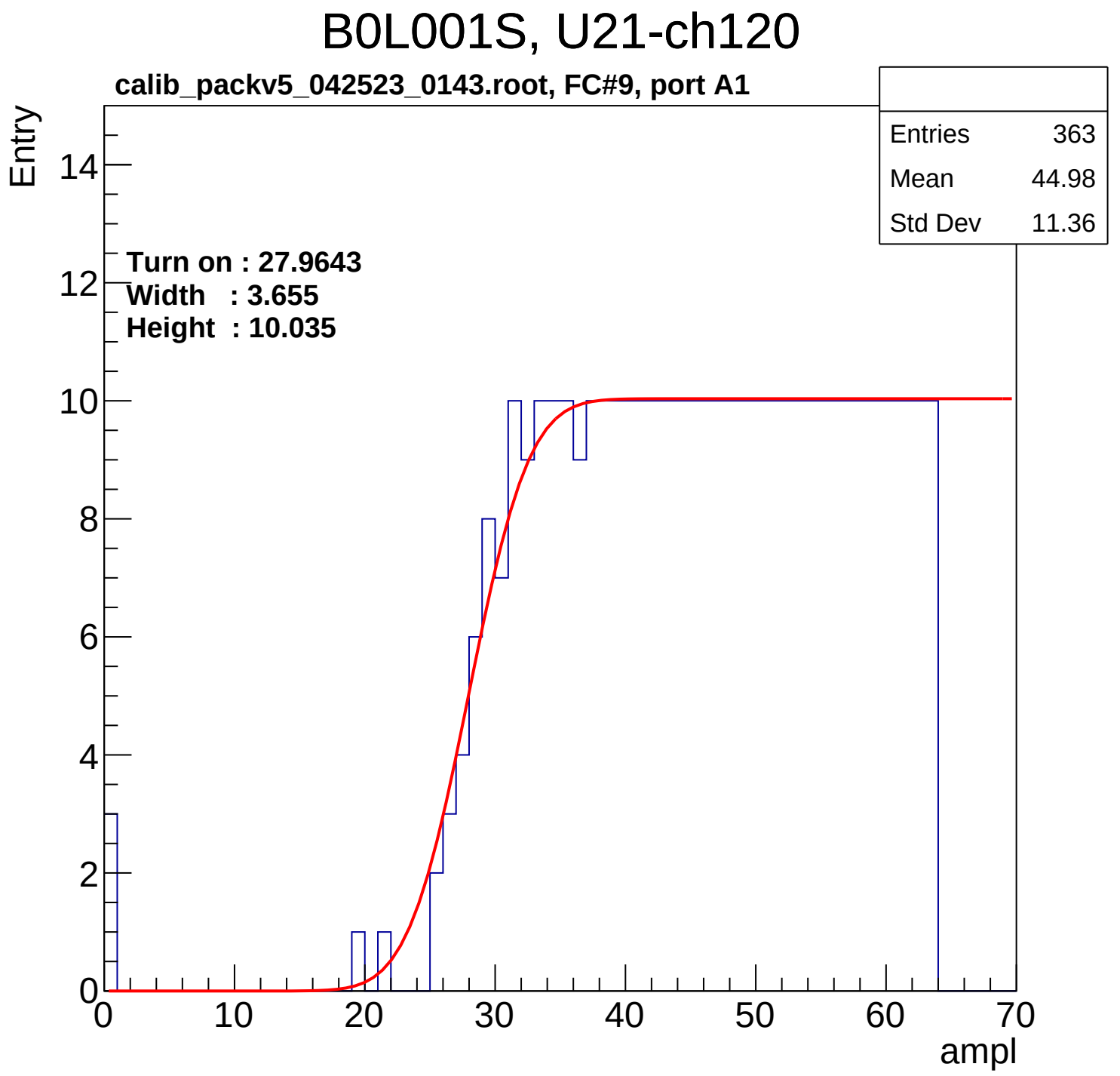
B0L001S, U21-ch120
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 44.98
Std Dev 11.36
Turn on : 27.9643
Width : 3.655
Height : 10.035
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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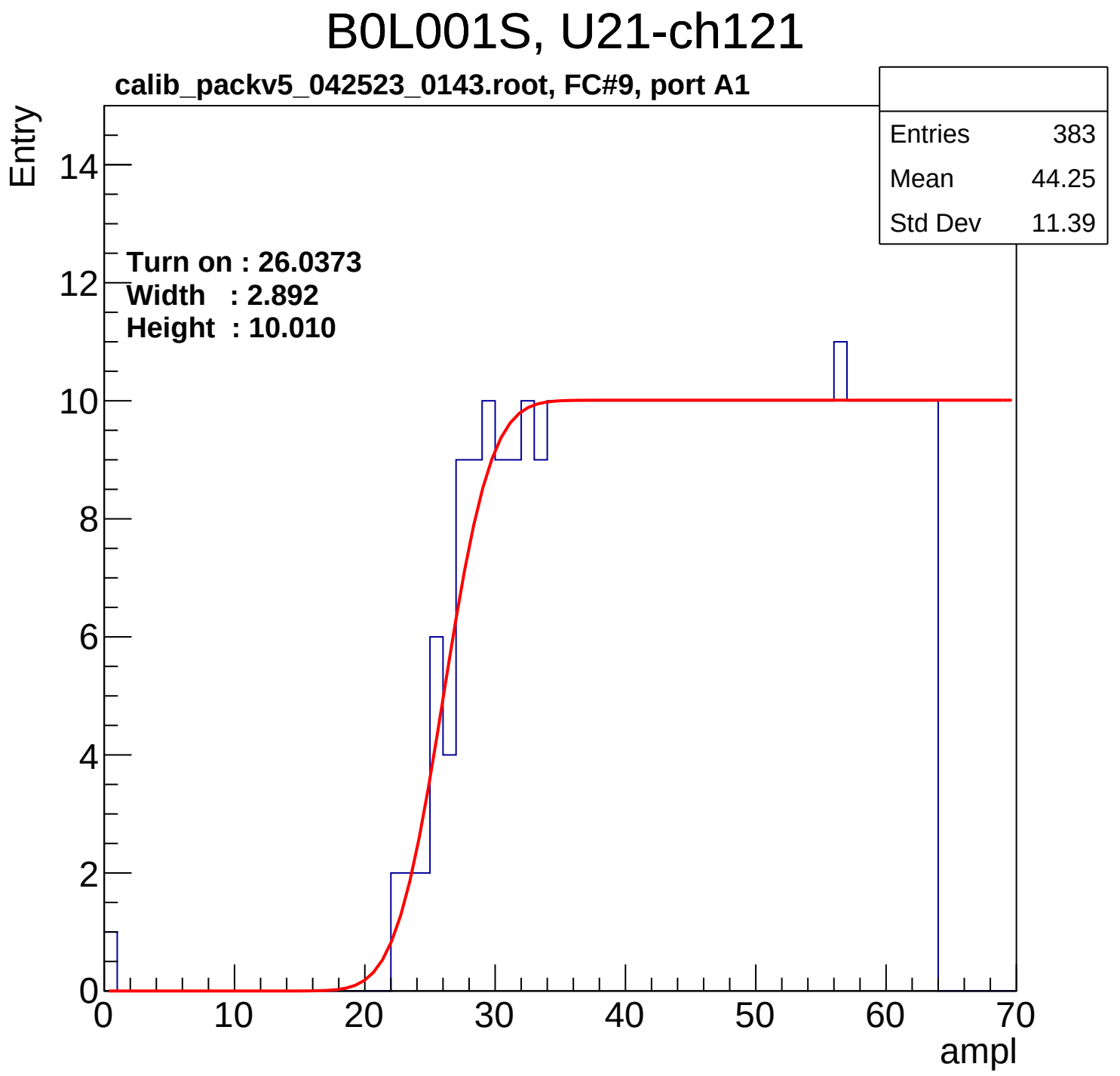
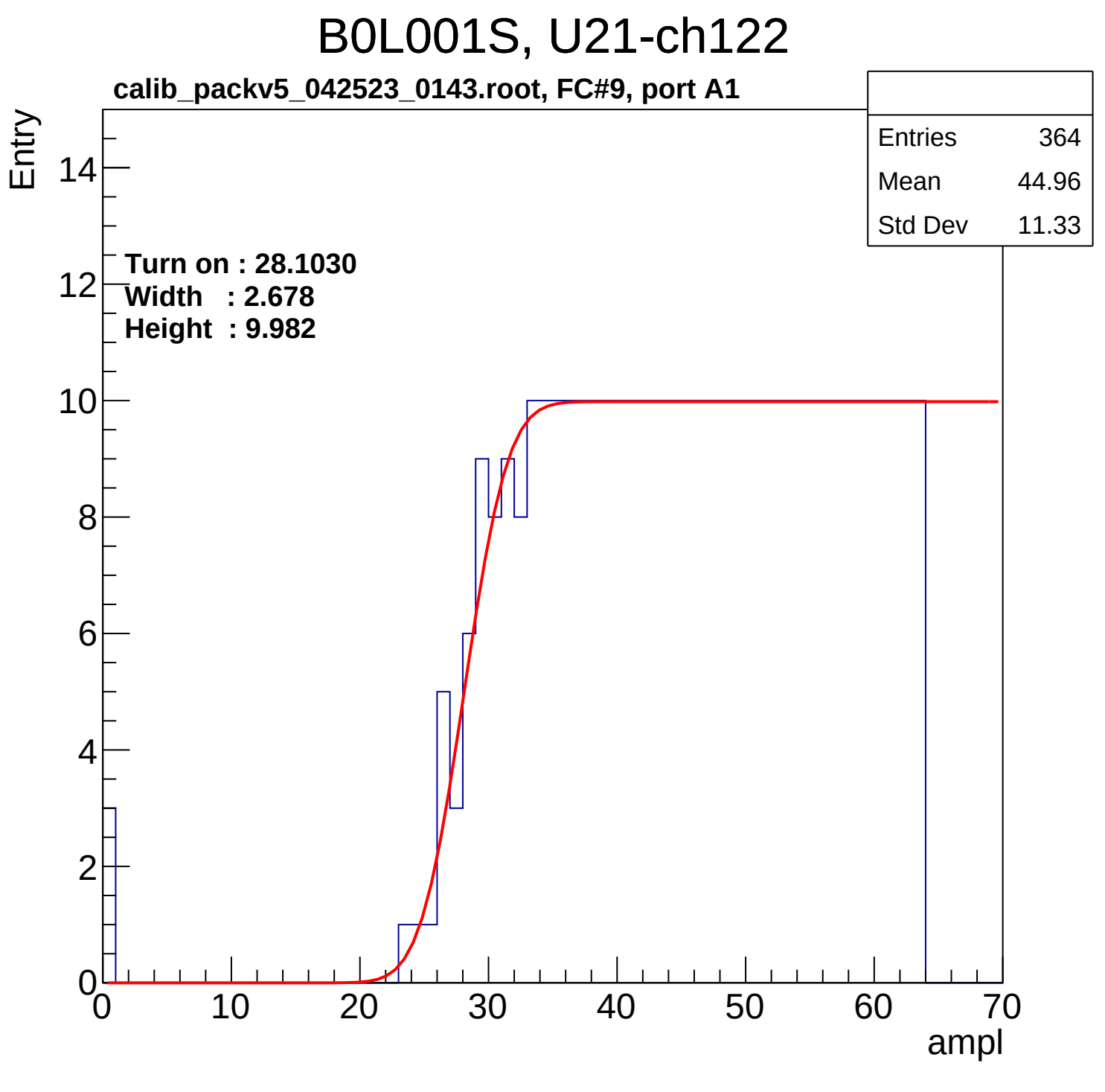
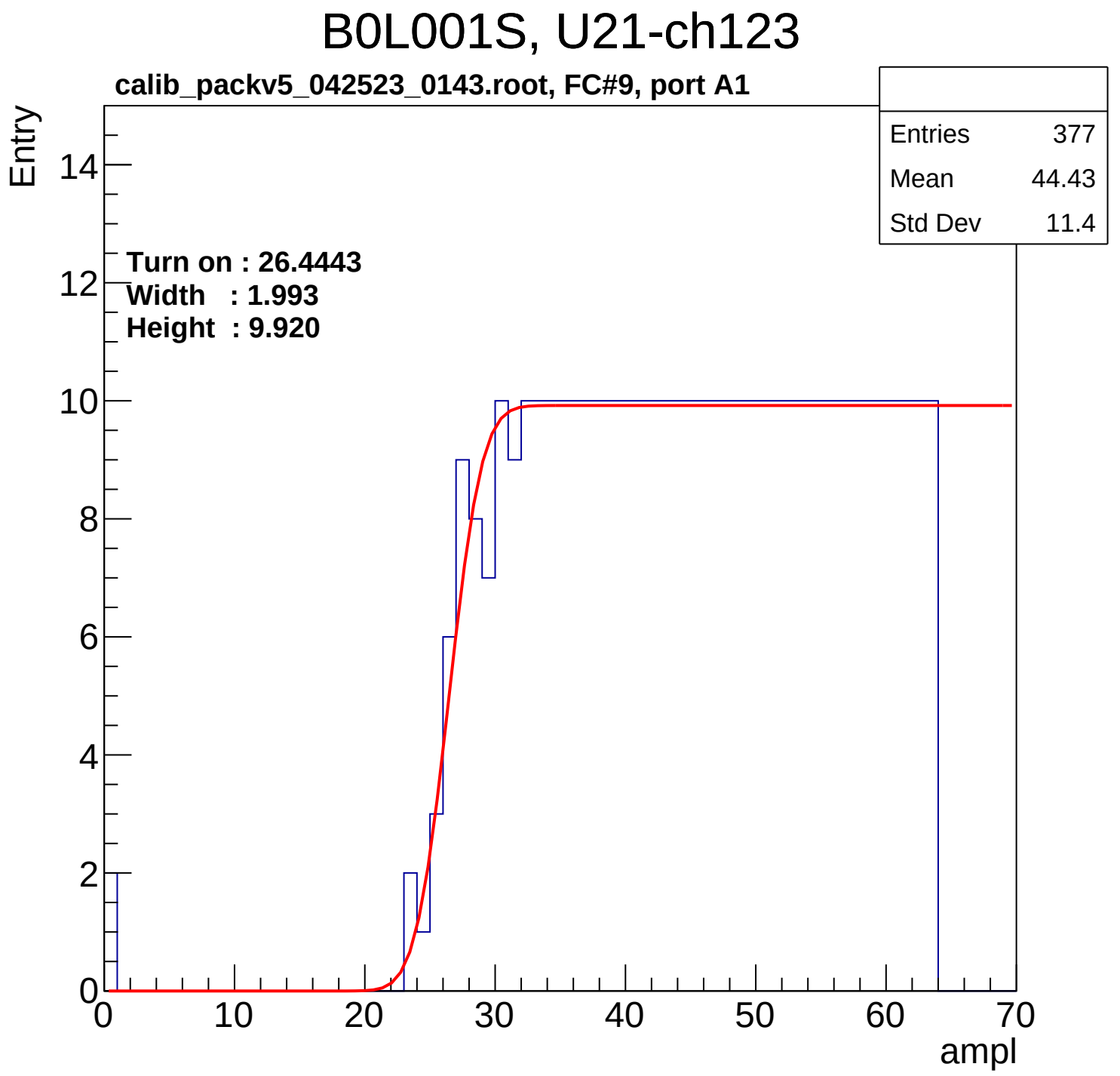
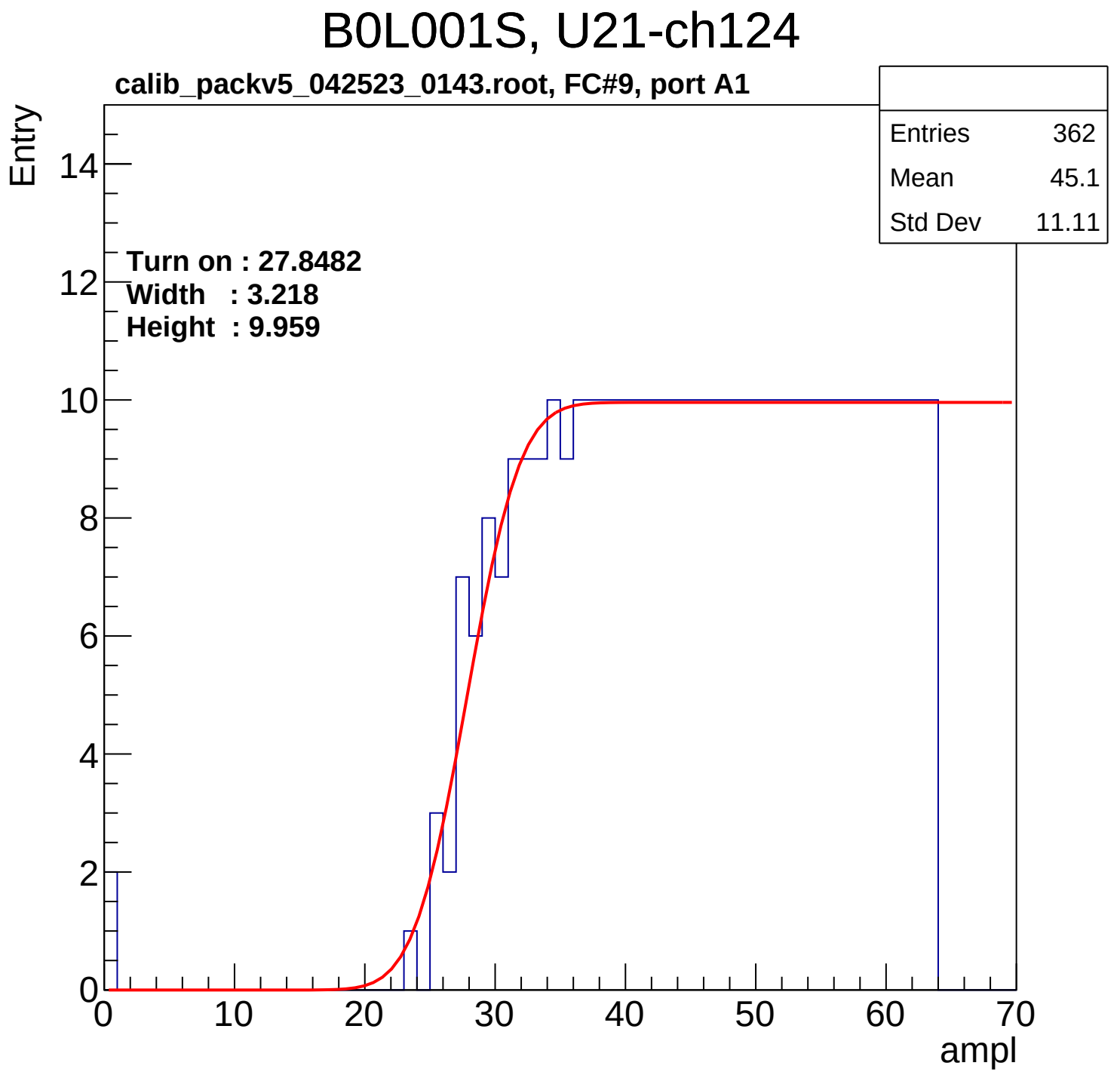
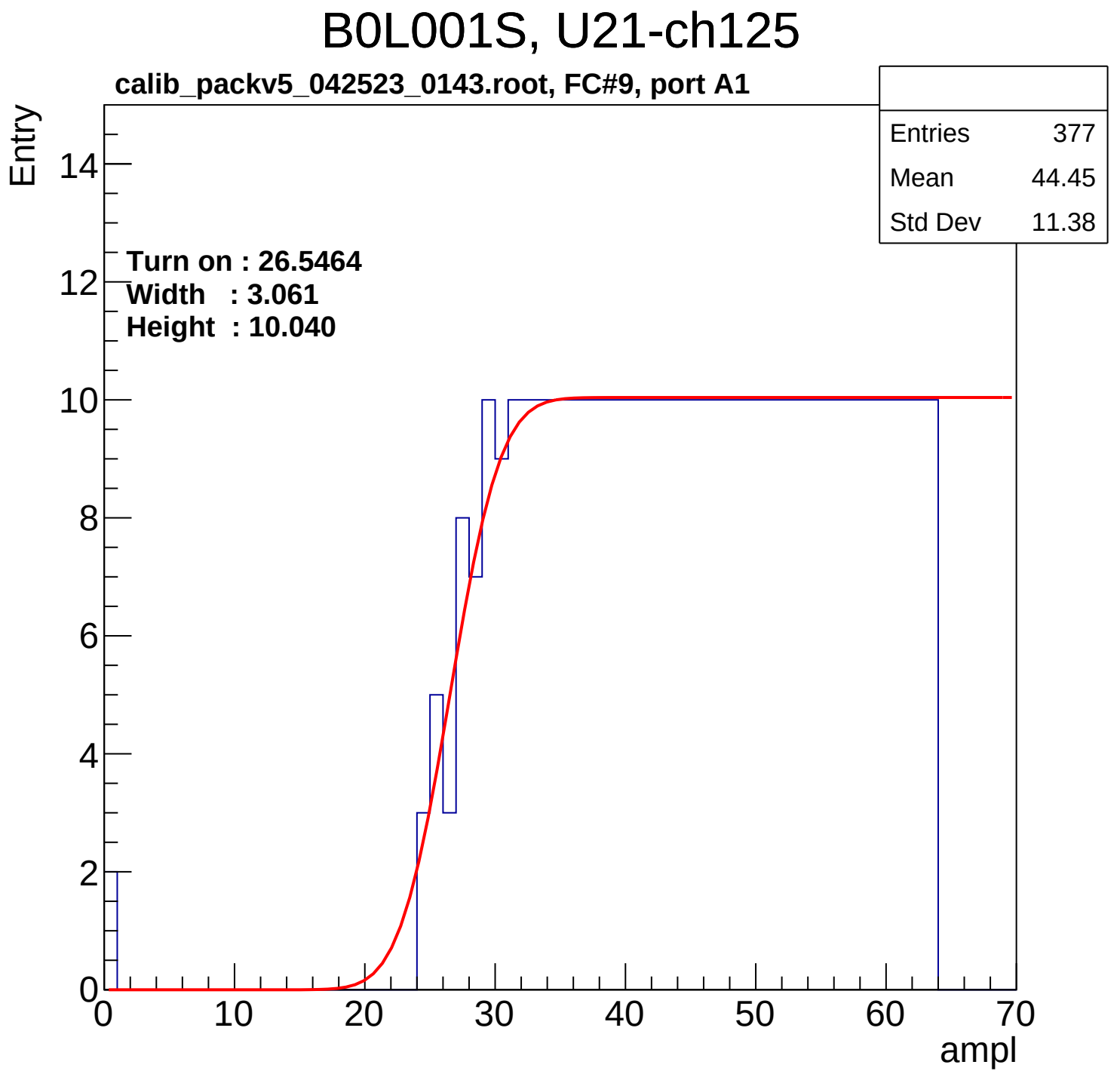
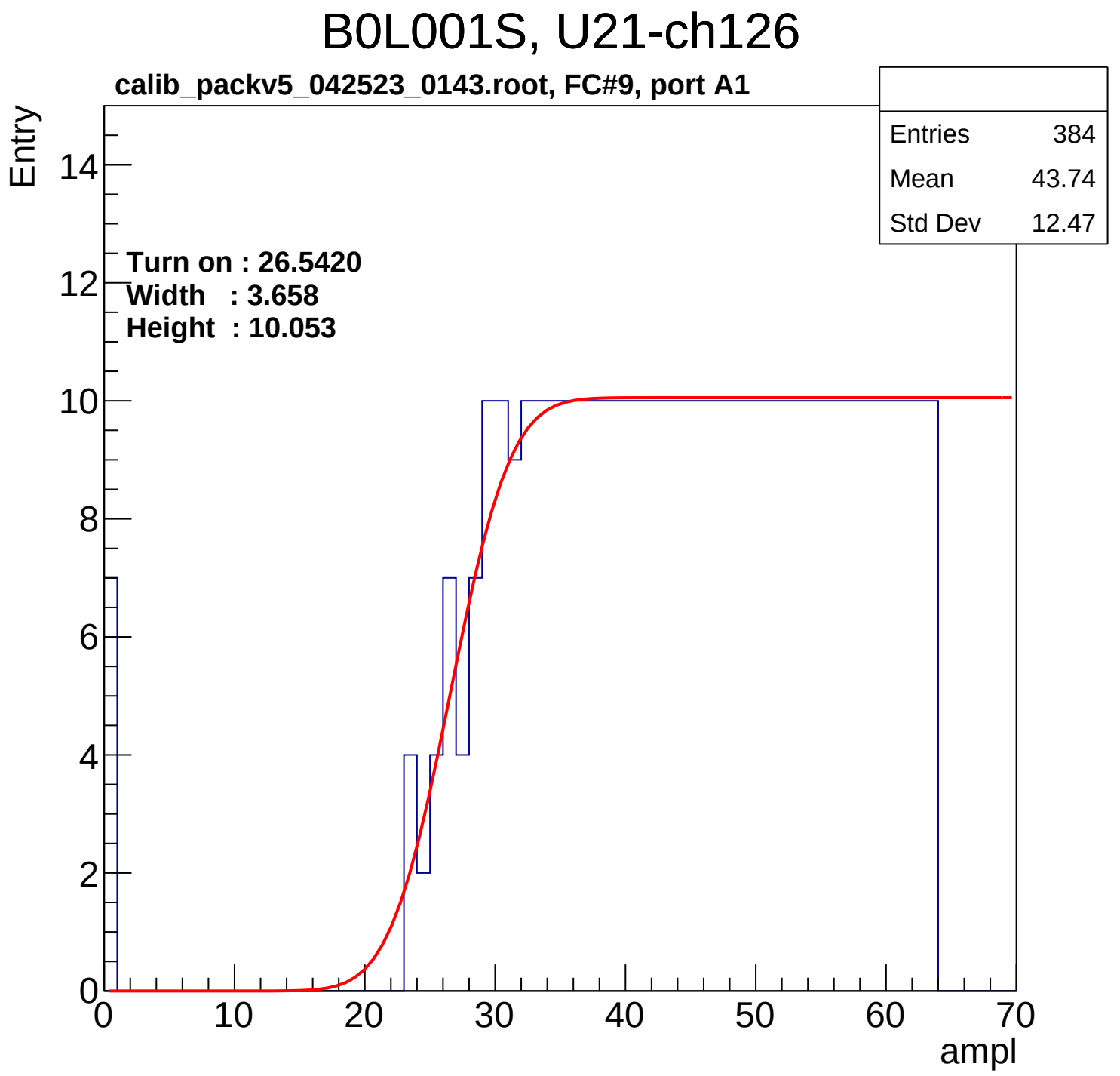

B0L001S, U21-ch121
calib_packv5_042523_0143.root, FC#9, port A1
Entries 383
Mean 44.25
Std Dev 11.39
Turn on : 26.0373
Width : 2.892
Height : 10.010
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U21-ch122
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 44.96
Std Dev 11.33
Turn on : 28.1030
Width : 2.678
Height : 9.982
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U21-ch123
calib_packv5_042523_0143.root, FC#9, port A1
Entries 377
Mean 44.43
Std Dev 11.4
Turn on : 26.4443
Width : 1.993
Height : 9.920
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U21-ch124
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 45.1
Std Dev 11.11
Turn on : 27.8482
Width : 3.218
Height : 9.959
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U21-ch125
calib_packv5_042523_0143.root, FC#9, port A1
Entries 377
Mean 44.45
Std Dev 11.38
Turn on : 26.5464
Width : 3.061
Height : 10.040
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U21-ch126
calib_packv5_042523_0143.root, FC#9, port A1
Entries 384
Mean 43.74
Std Dev 12.47
Turn on : 26.5420
Width : 3.658
Height : 10.053
Entry
ampl
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2
4
6
8
10
12
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0
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20
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60
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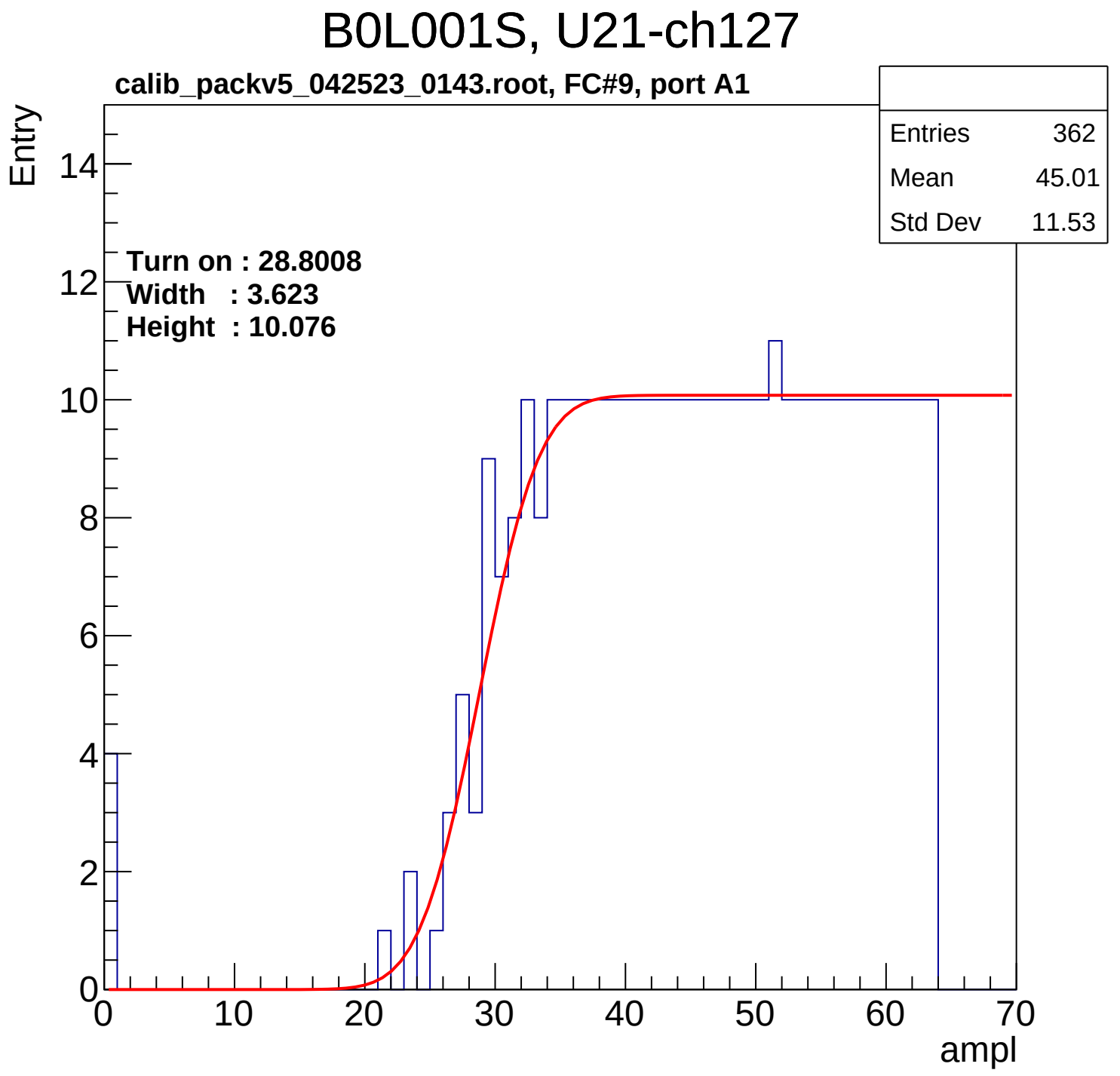
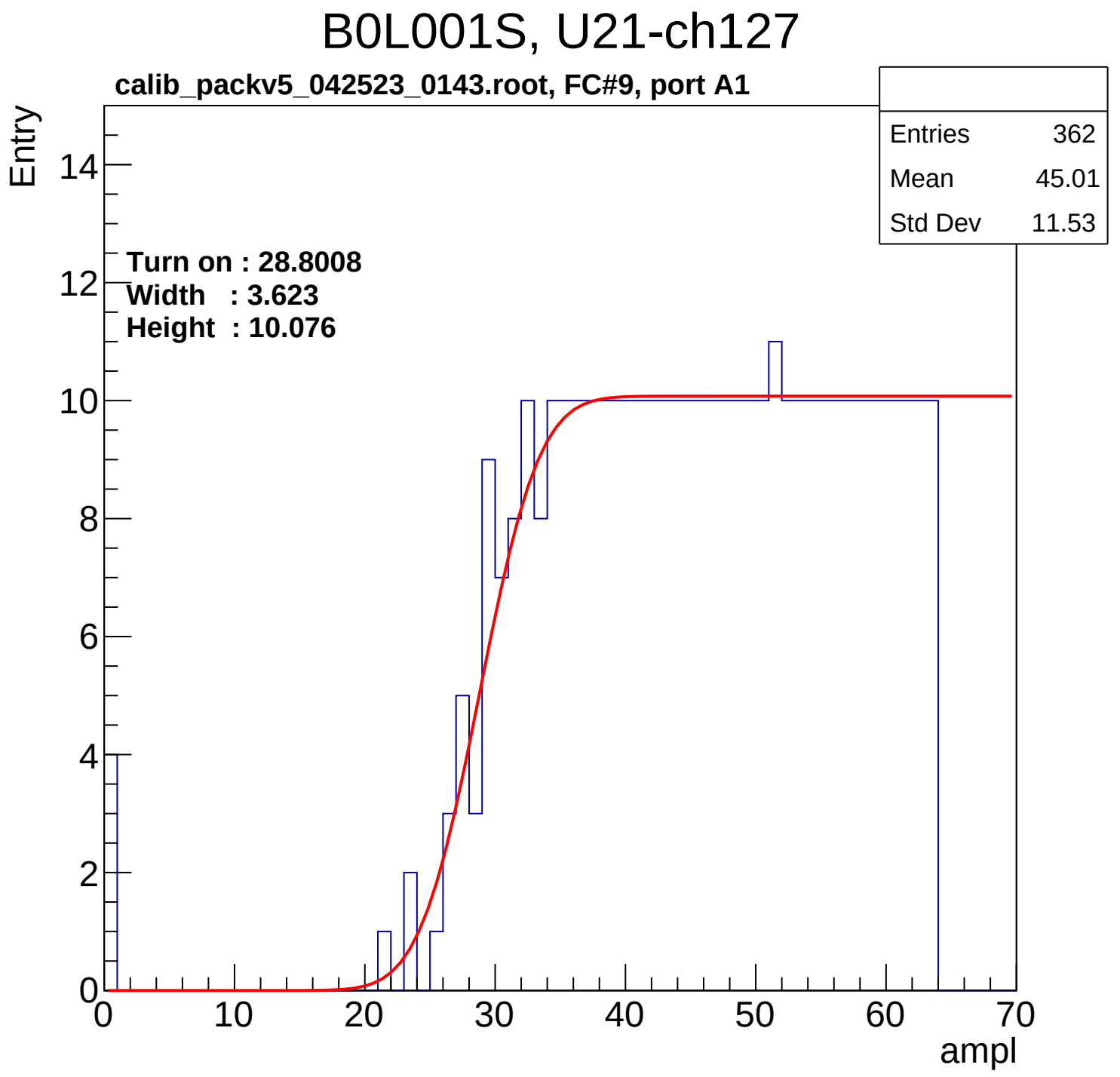

B0L001S, U21-ch127
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 45.01
Std Dev 11.53
Turn on : 28.8008
Width : 3.623
Height : 10.076
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U21-ch127
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 45.01
Std Dev 11.53
Turn on : 28.8008
Width : 3.623
Height : 10.076
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
30
40
50
60
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