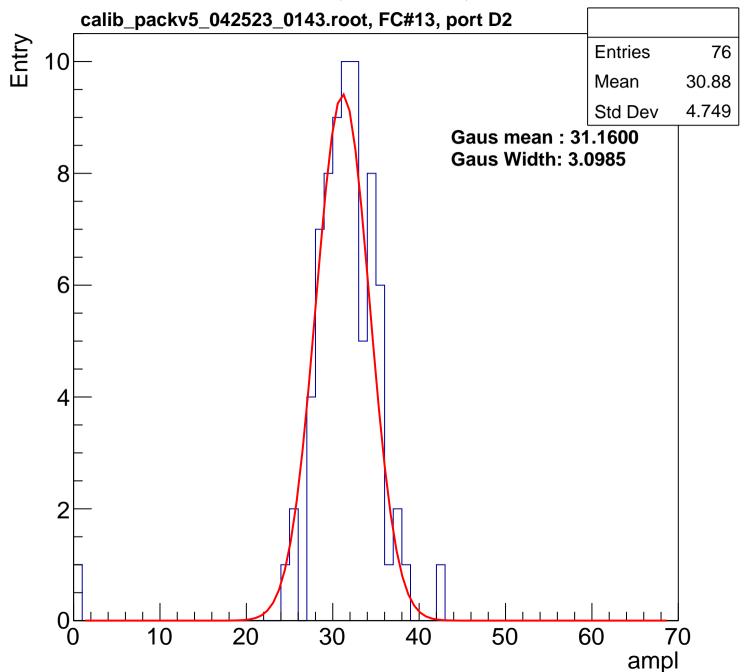
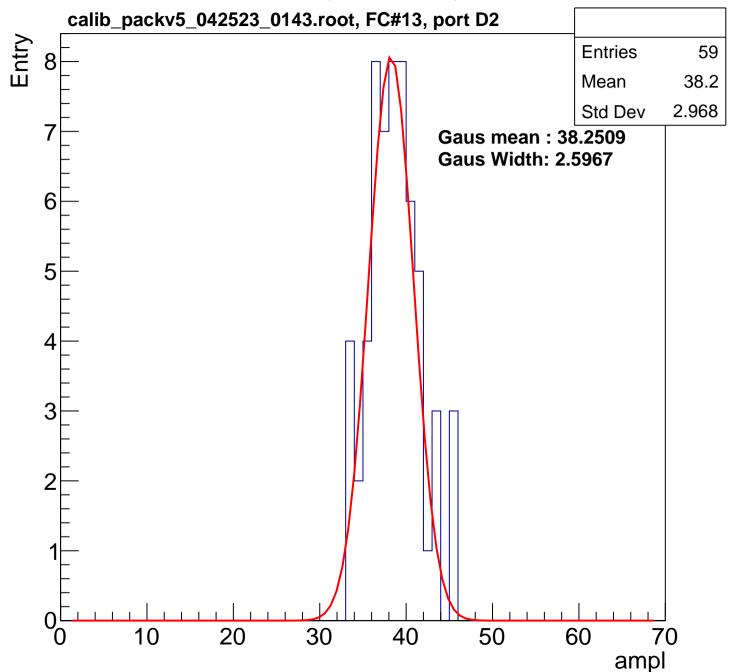
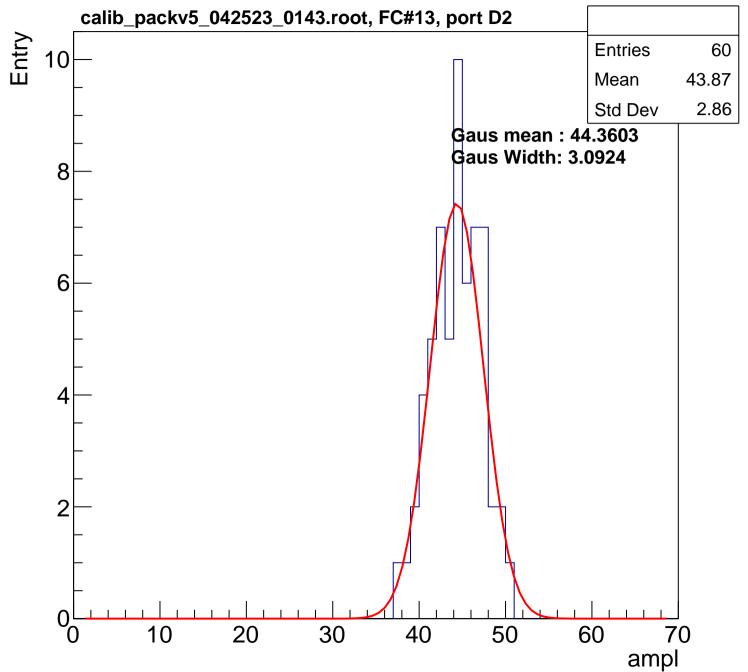
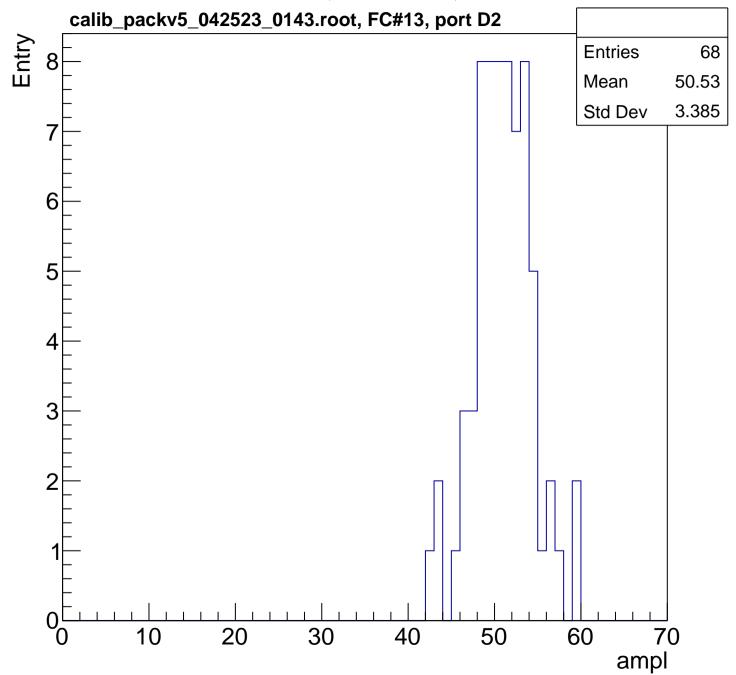


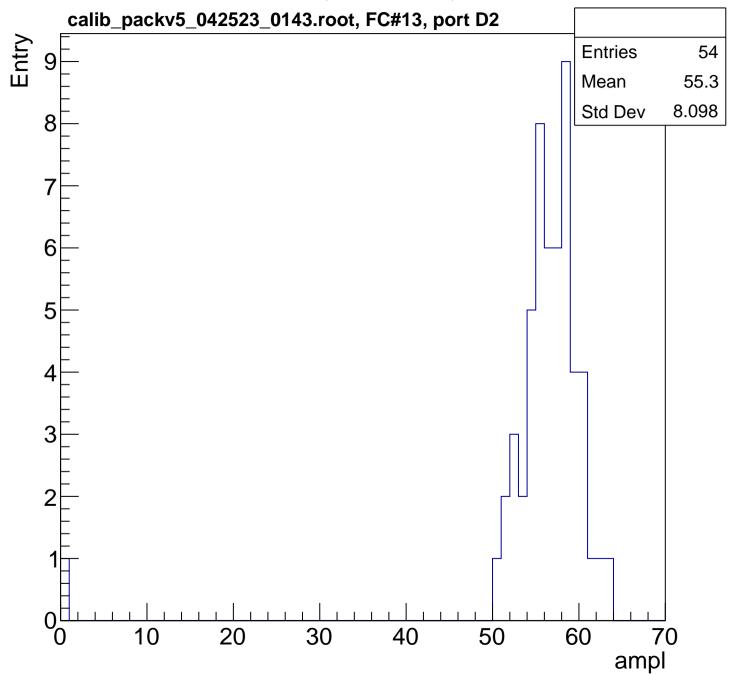
B1L003S, U8-ch1, adc7 calib\_packv5\_042523\_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

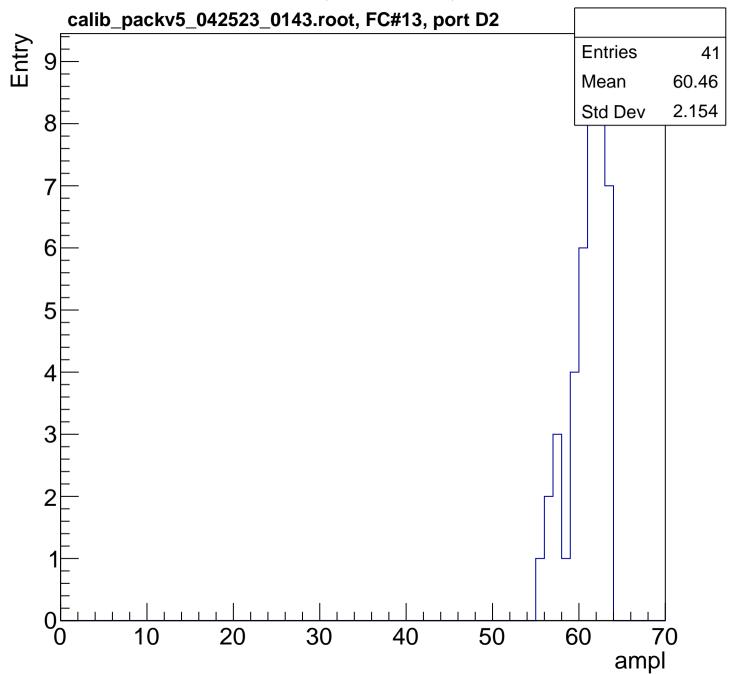


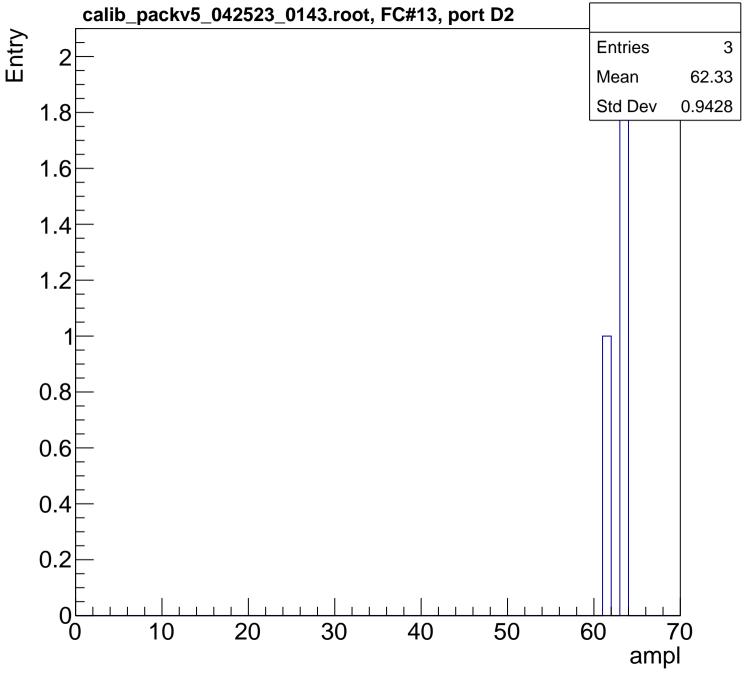


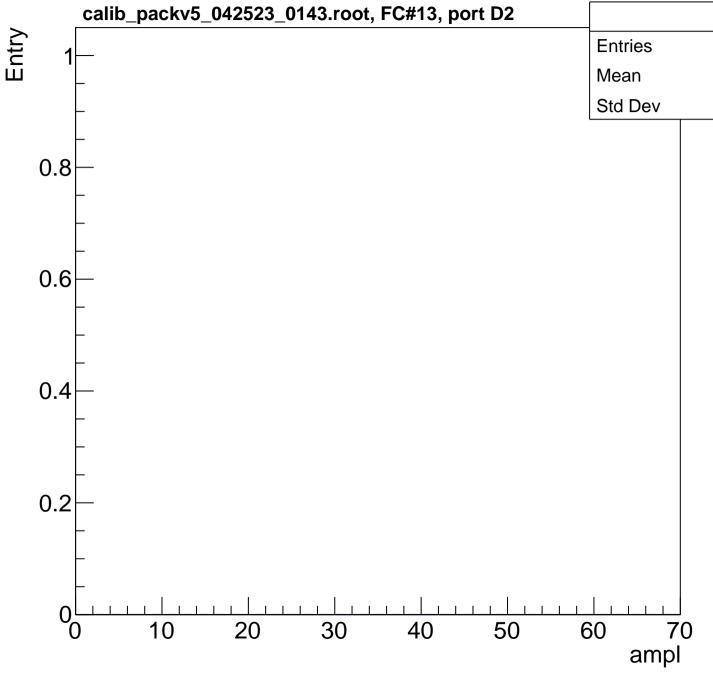


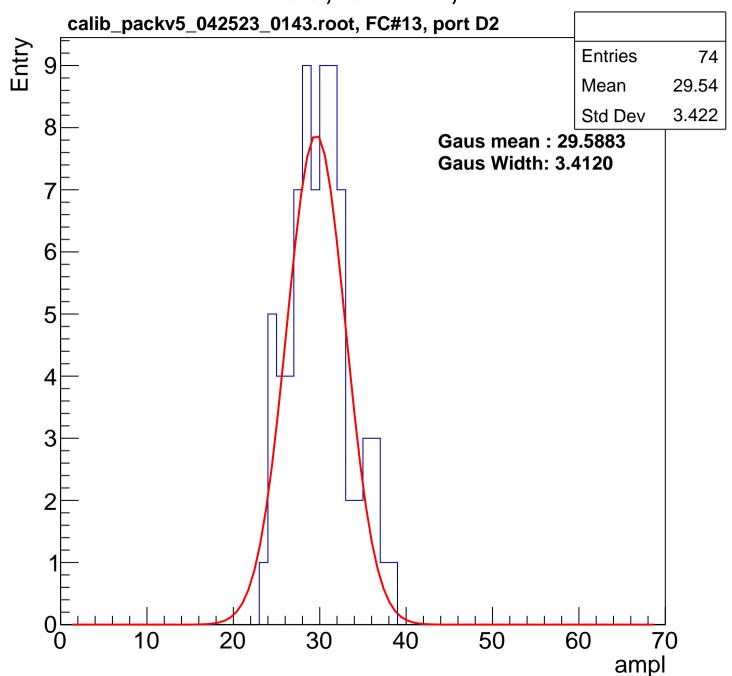


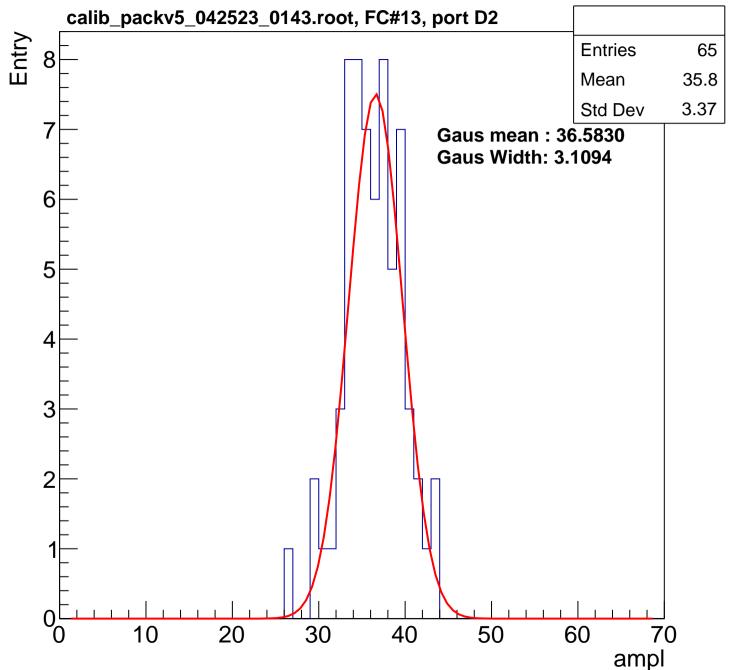


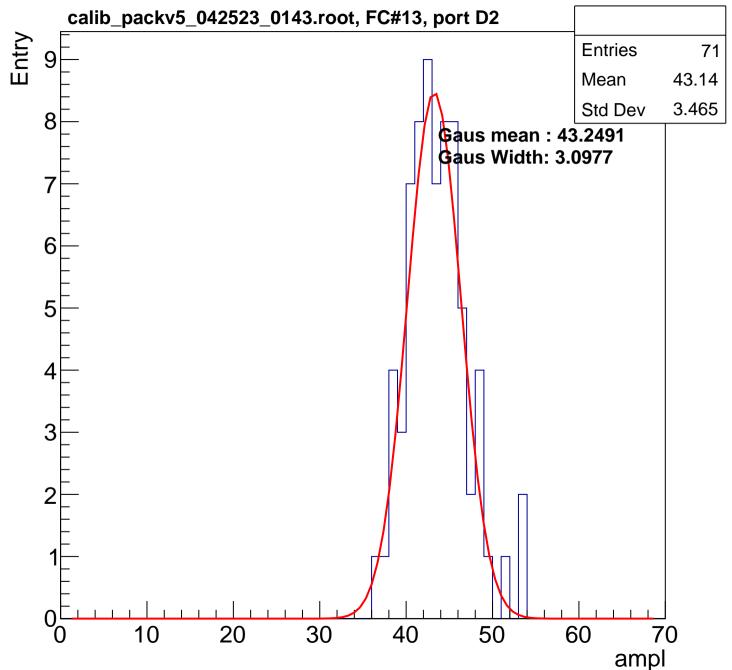


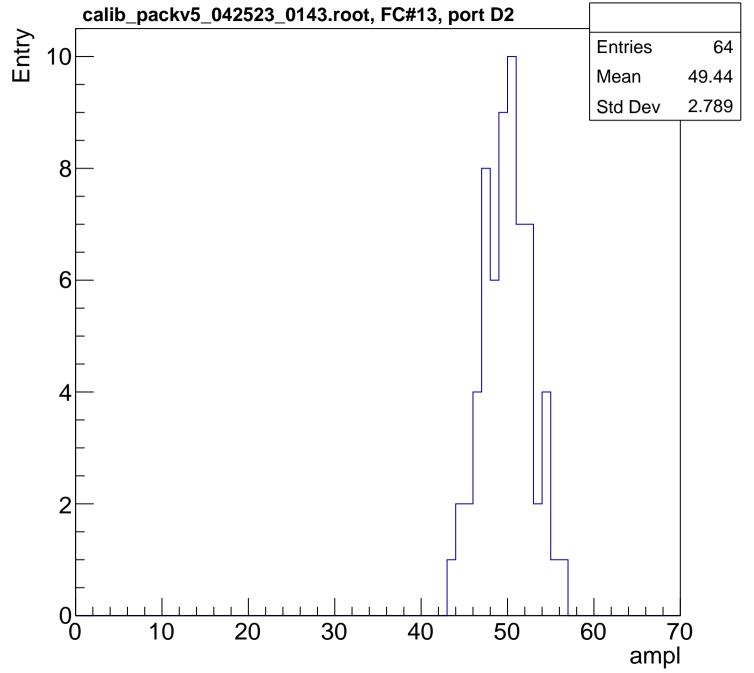


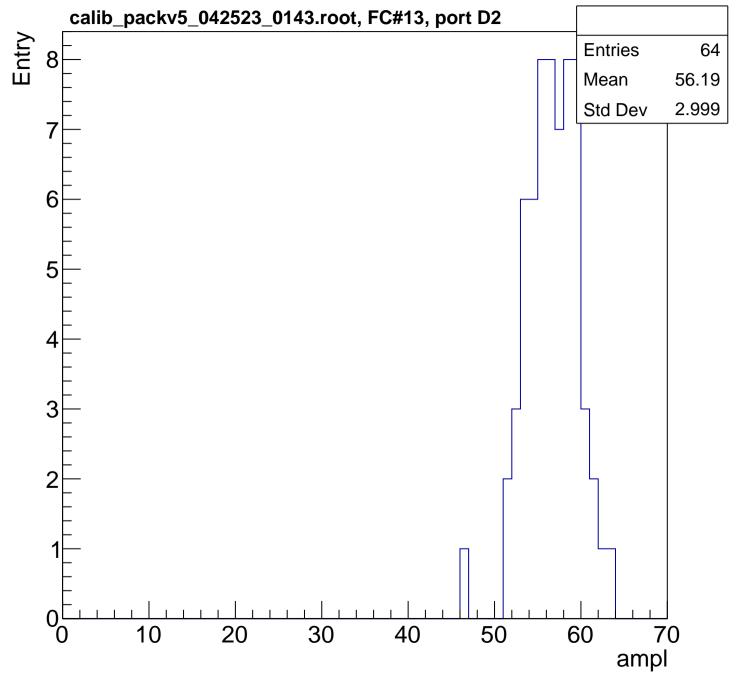


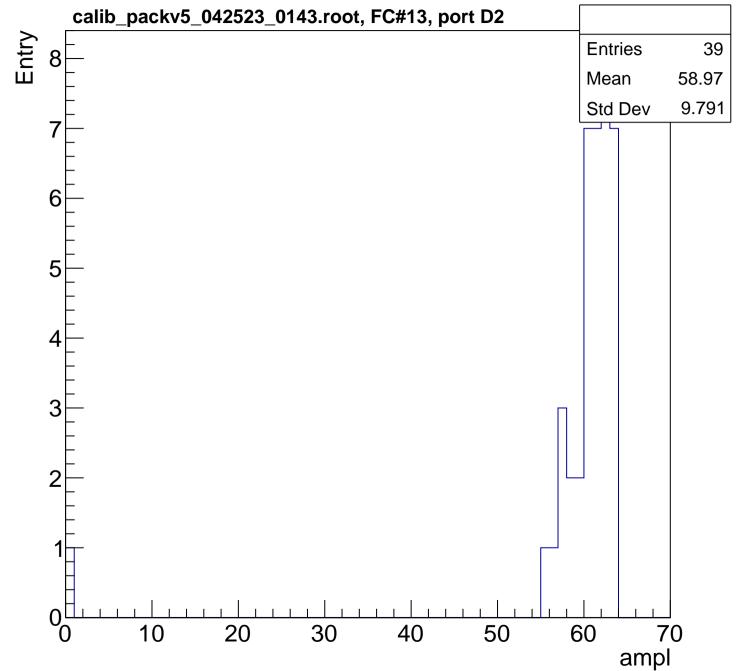


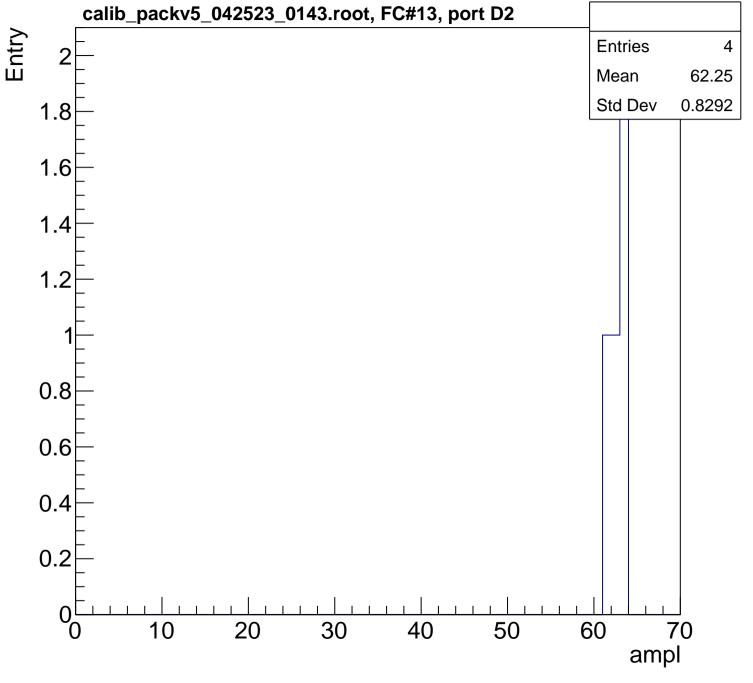




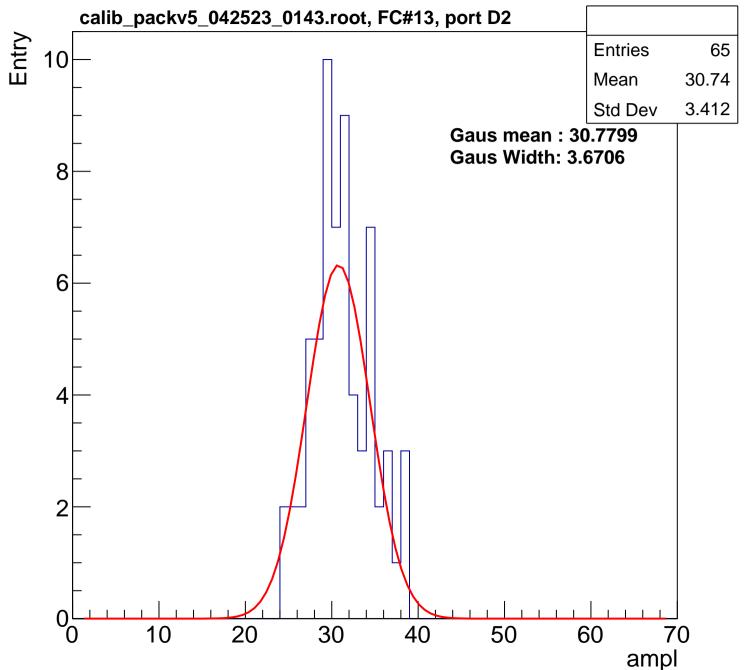


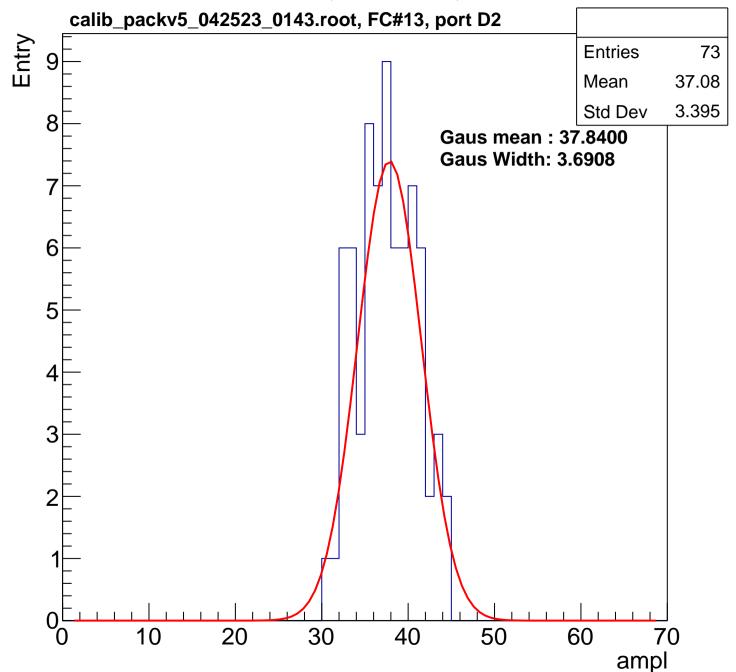


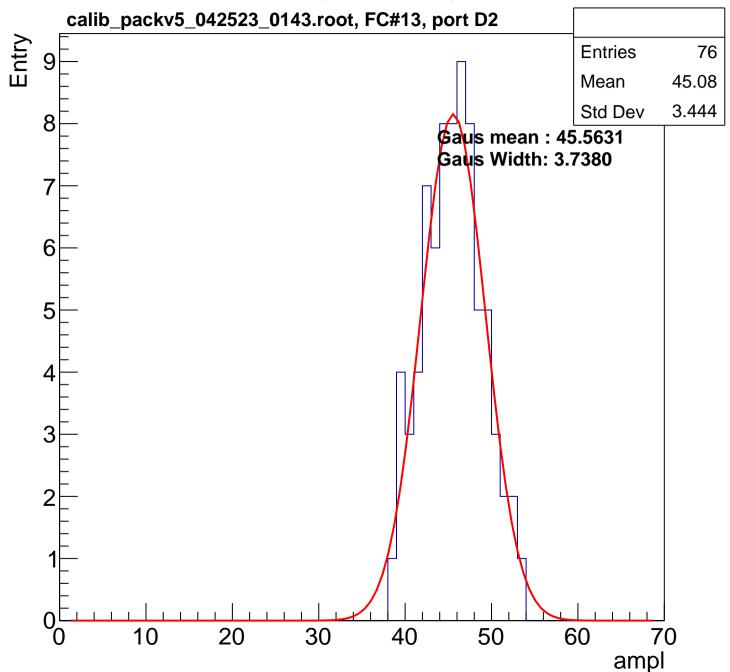


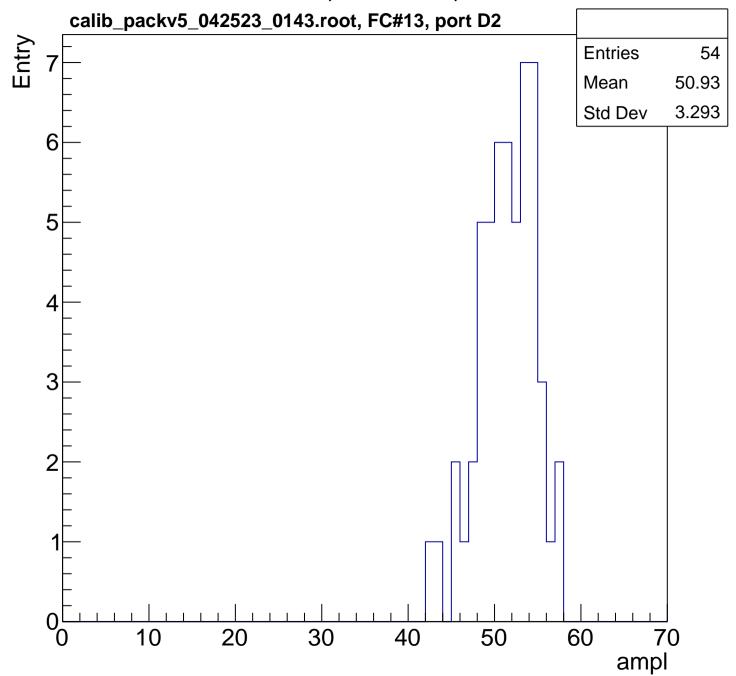


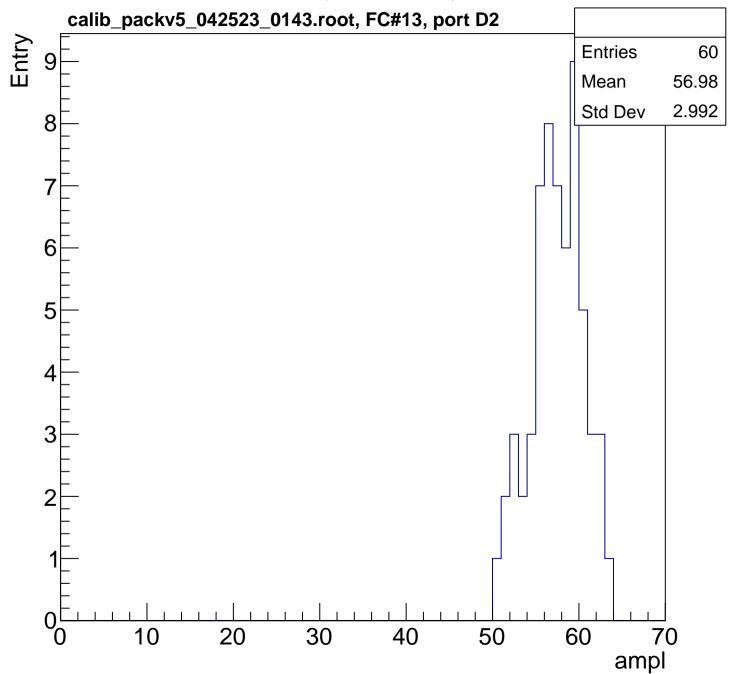


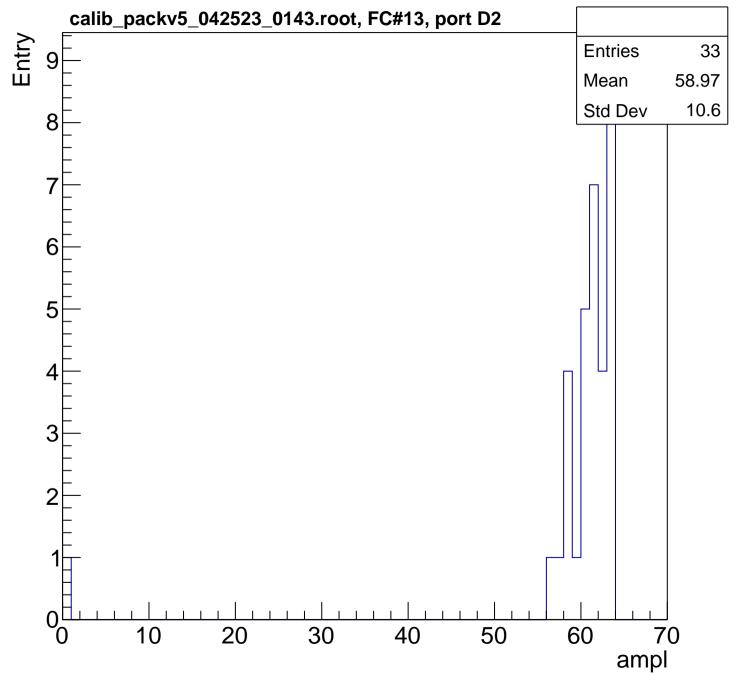


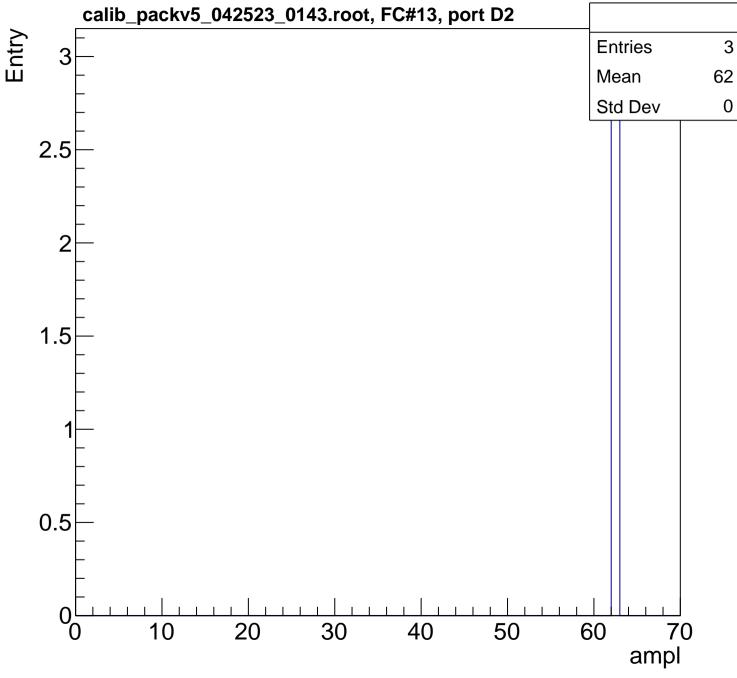


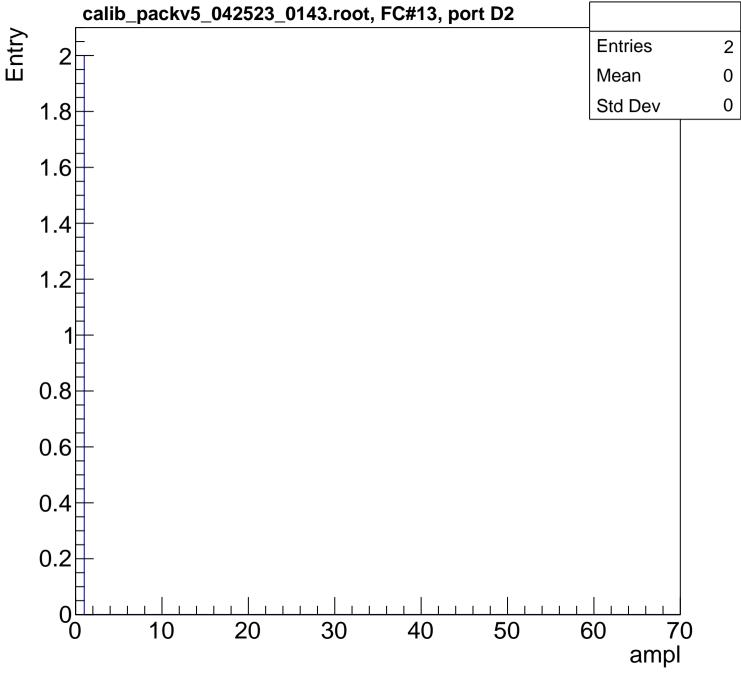


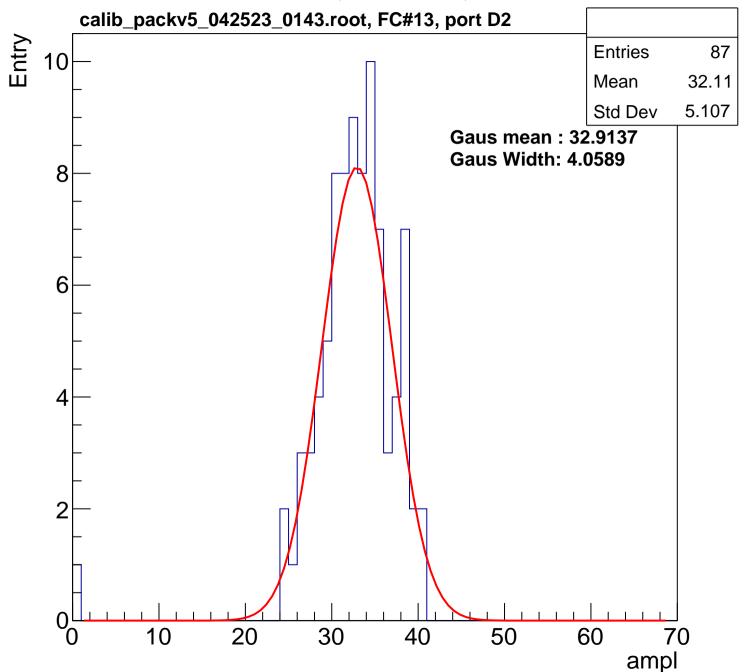


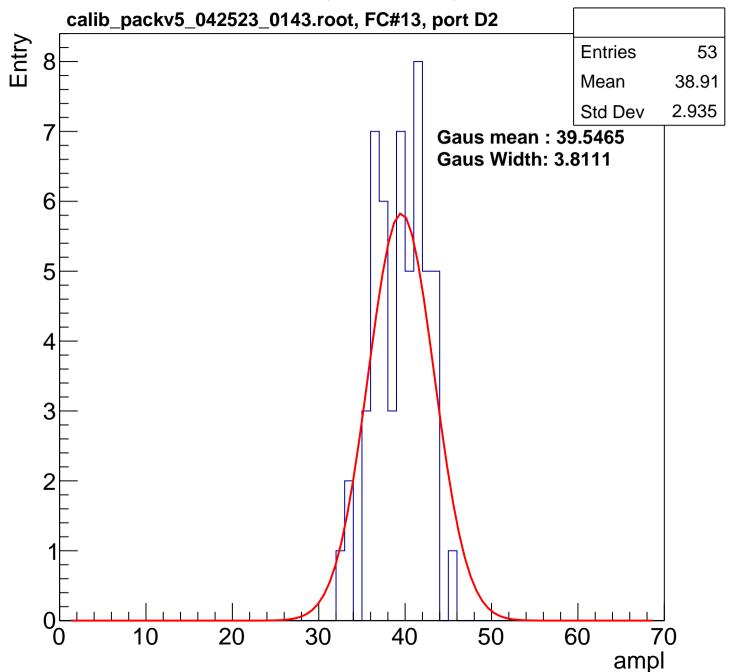


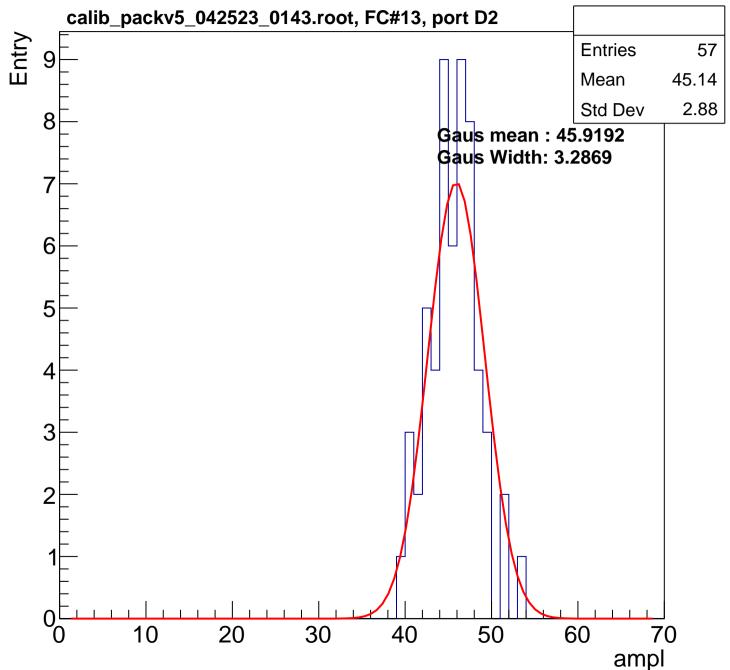


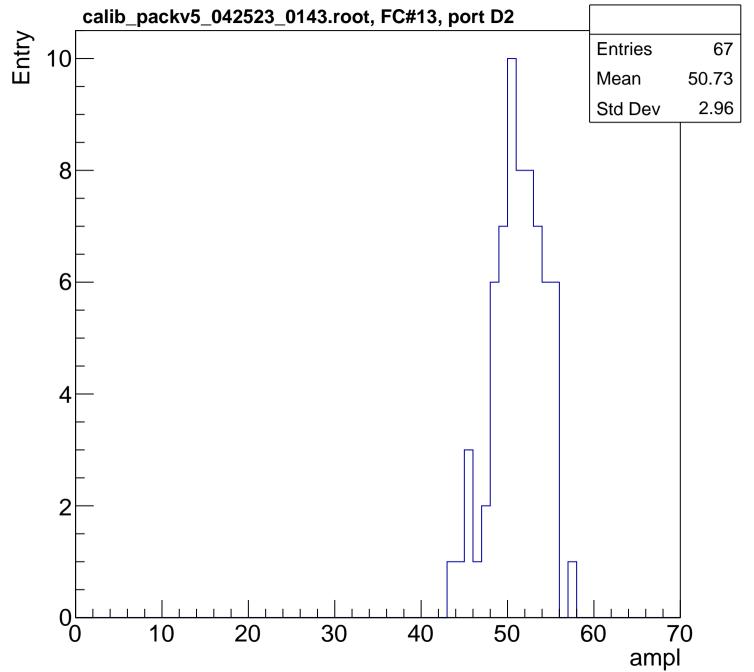


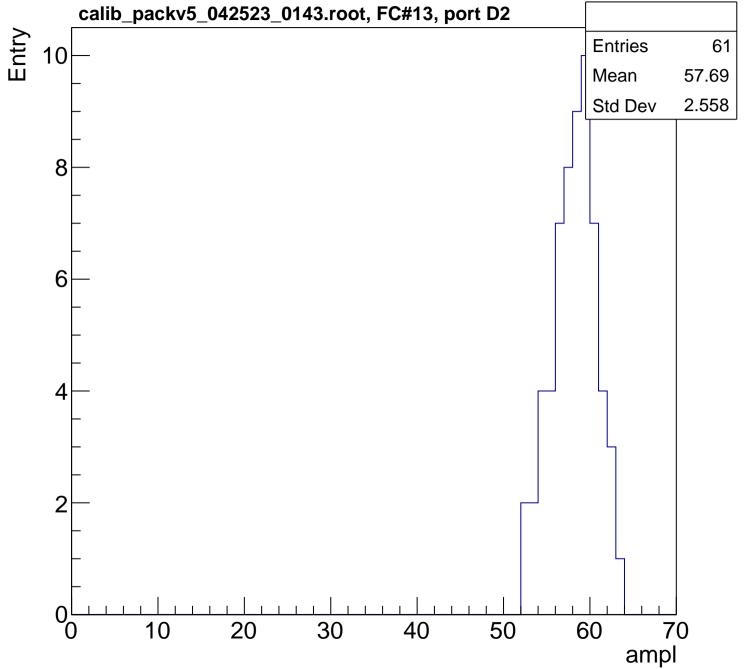


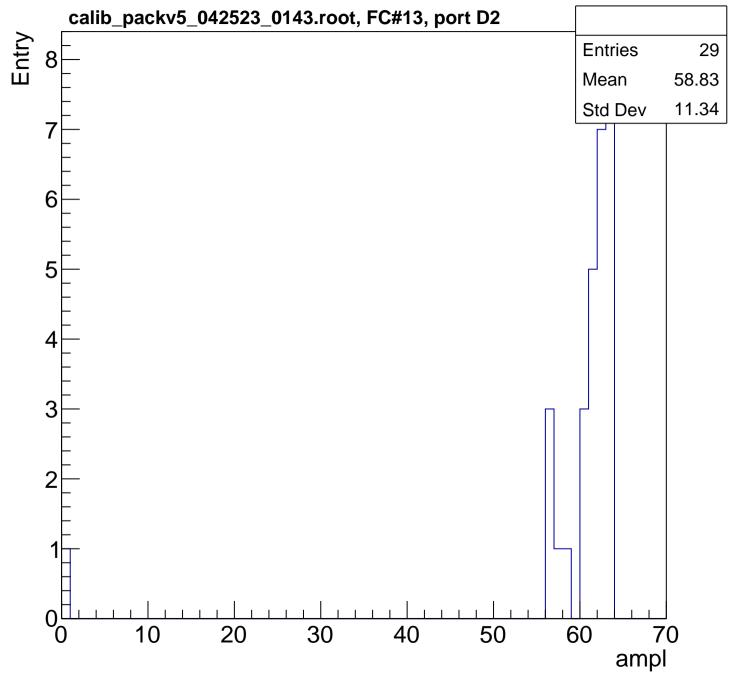


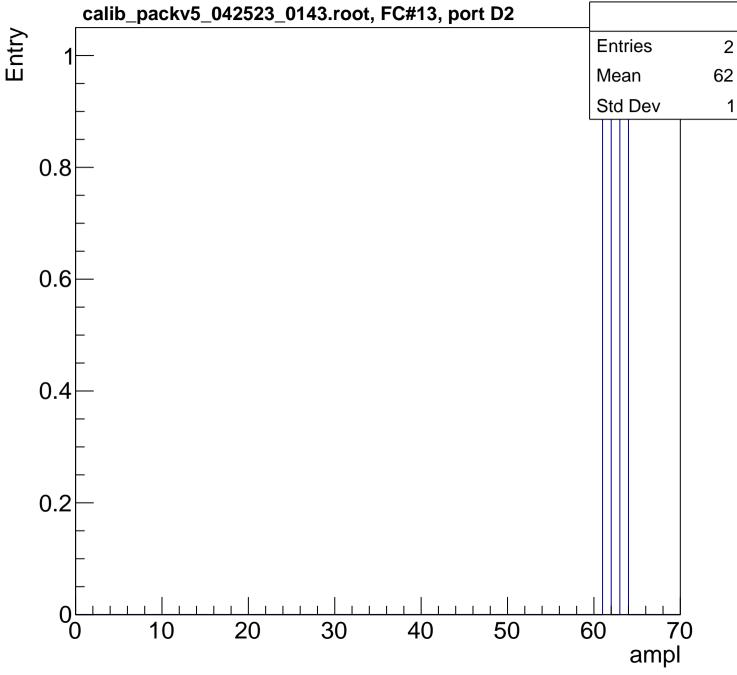




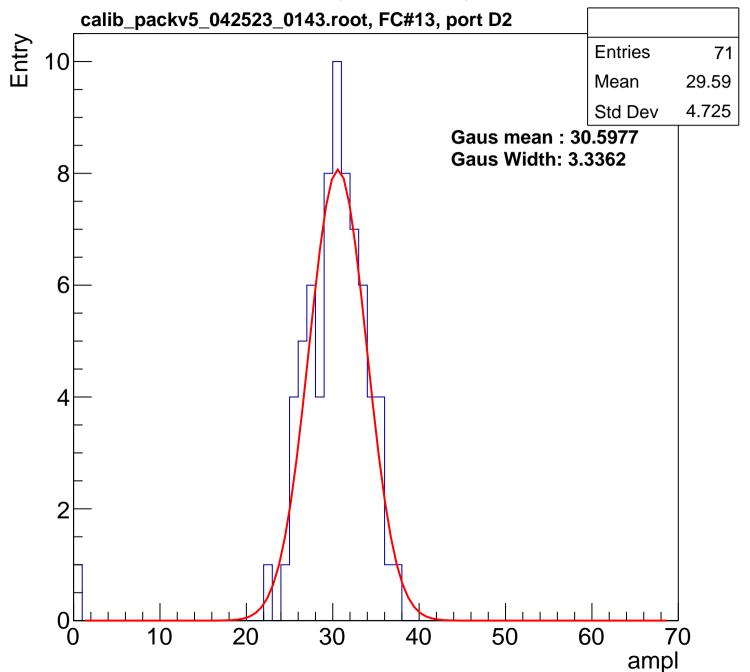


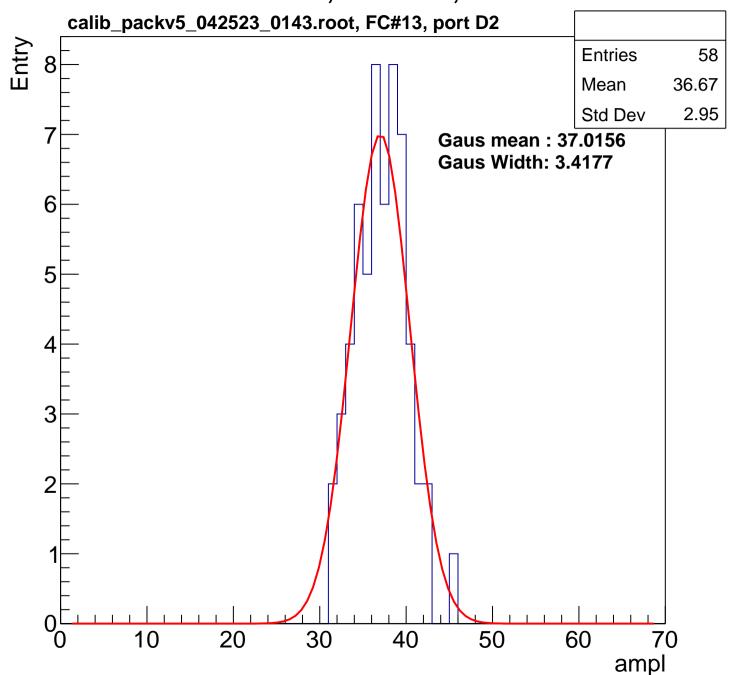


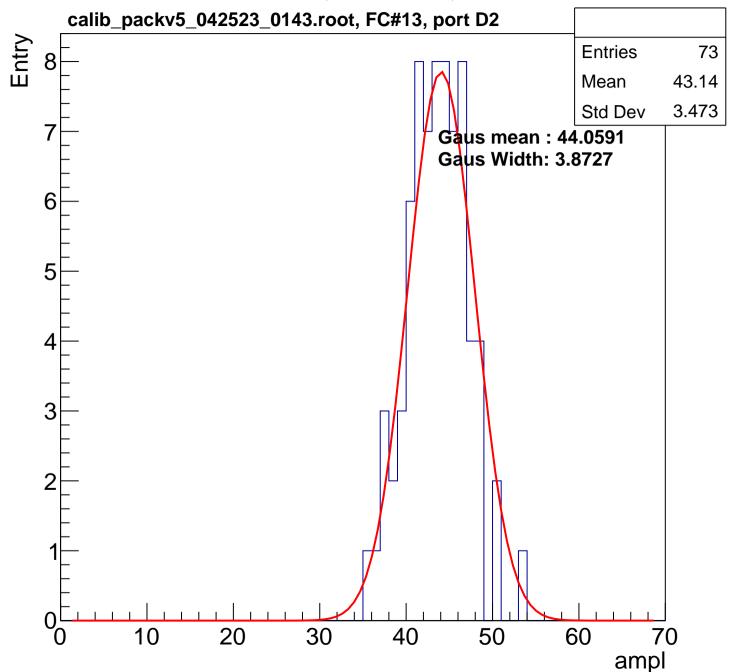


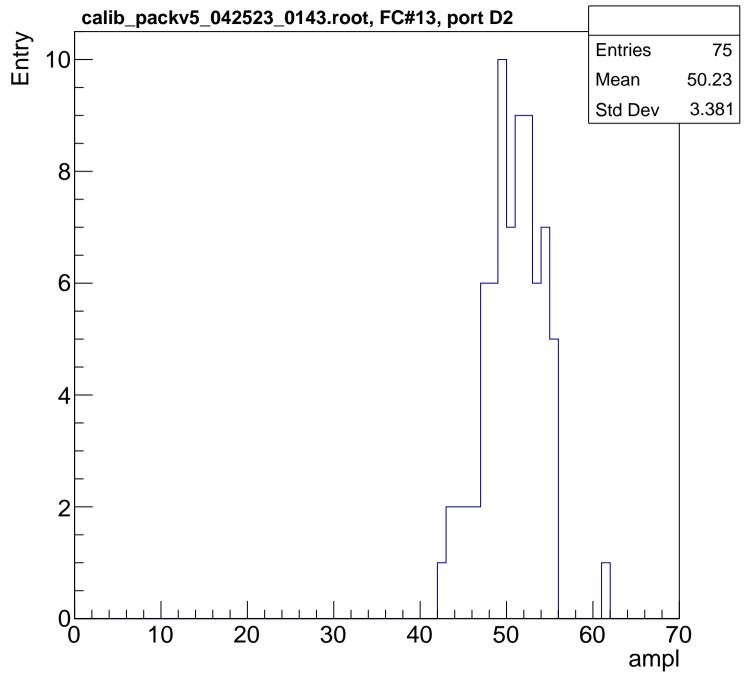


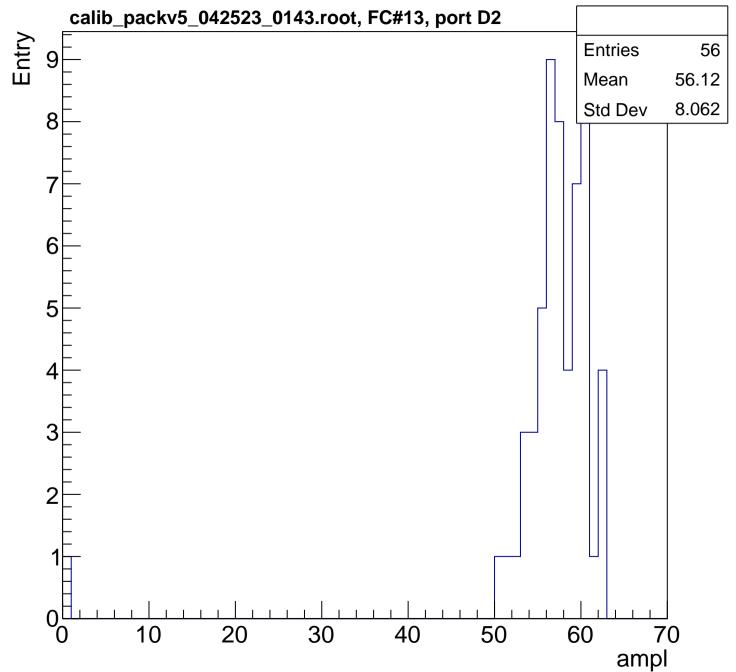
B1L003S, U8-ch5, adc7 calib\_packv5\_042523\_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

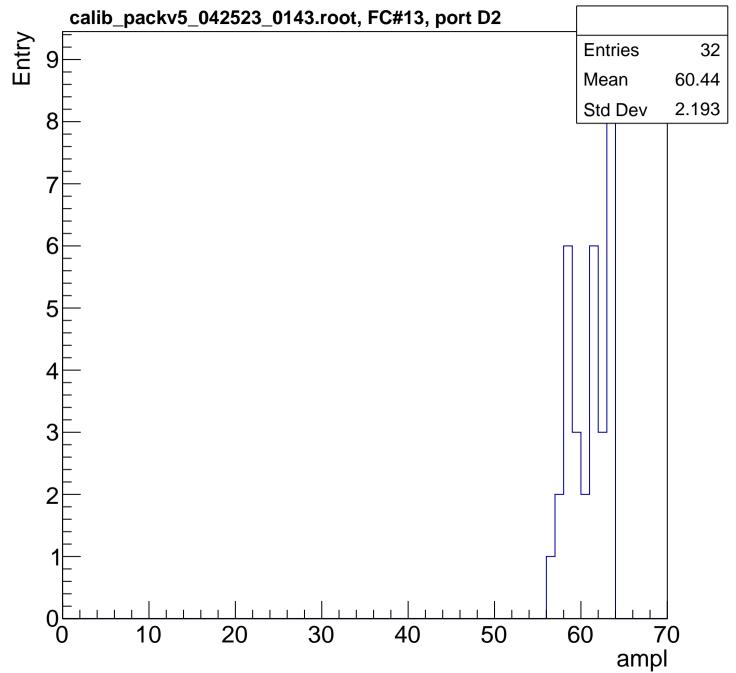


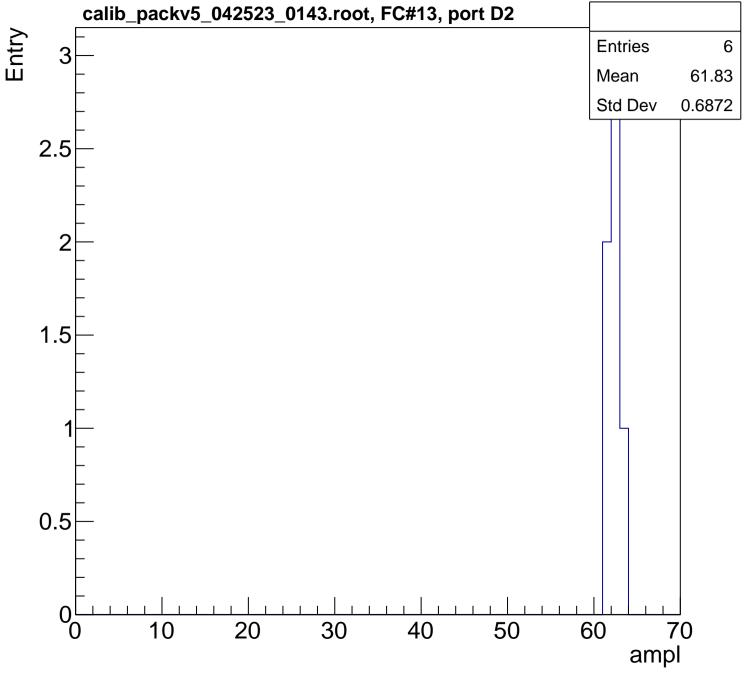


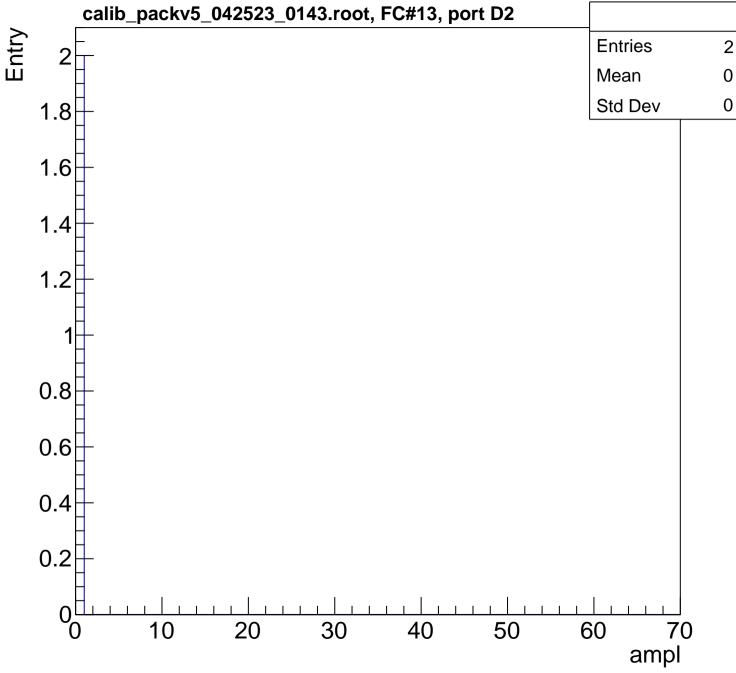


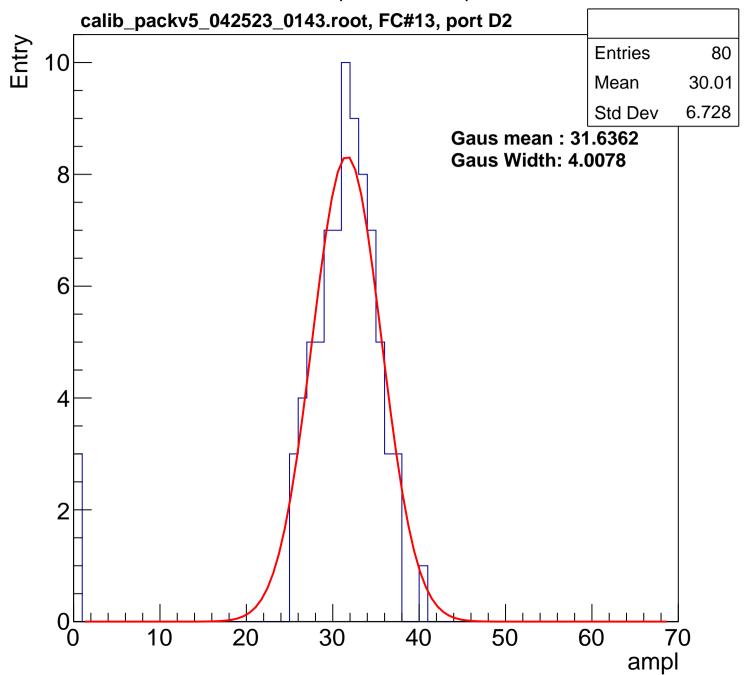


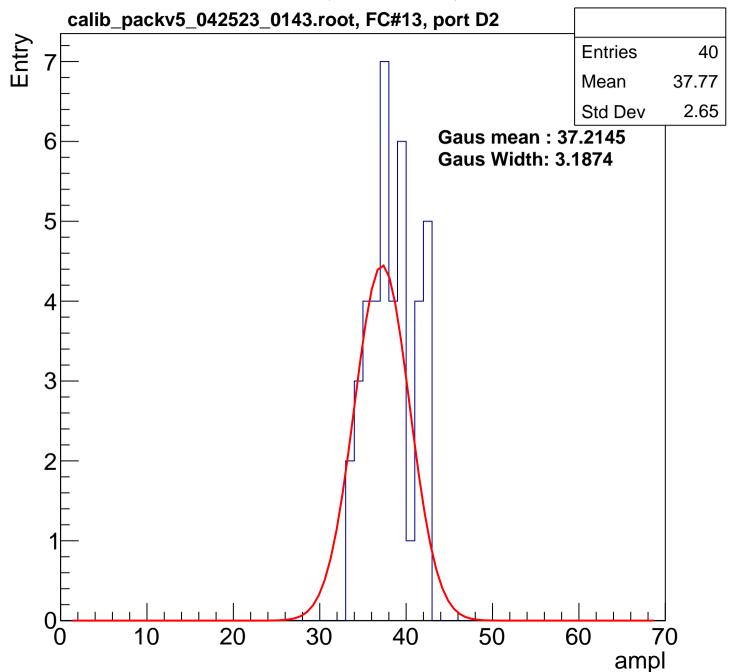


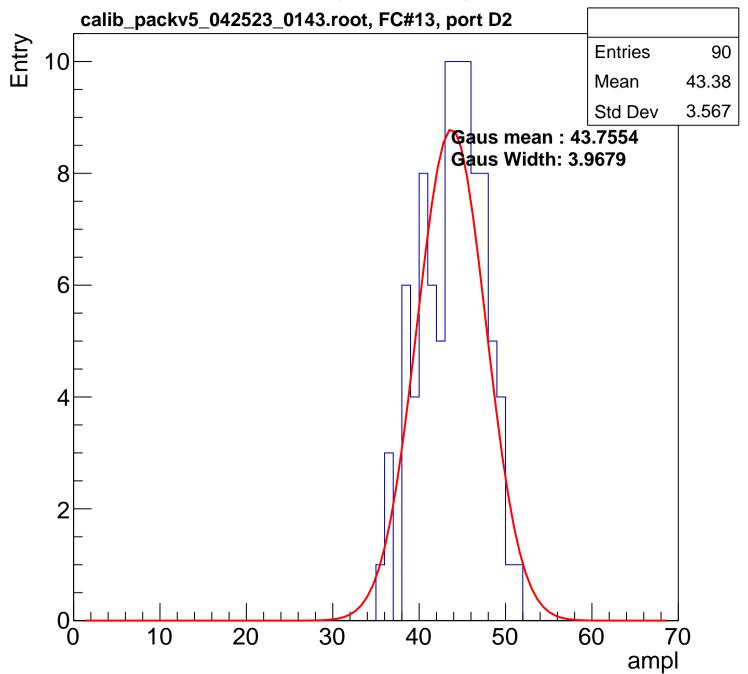


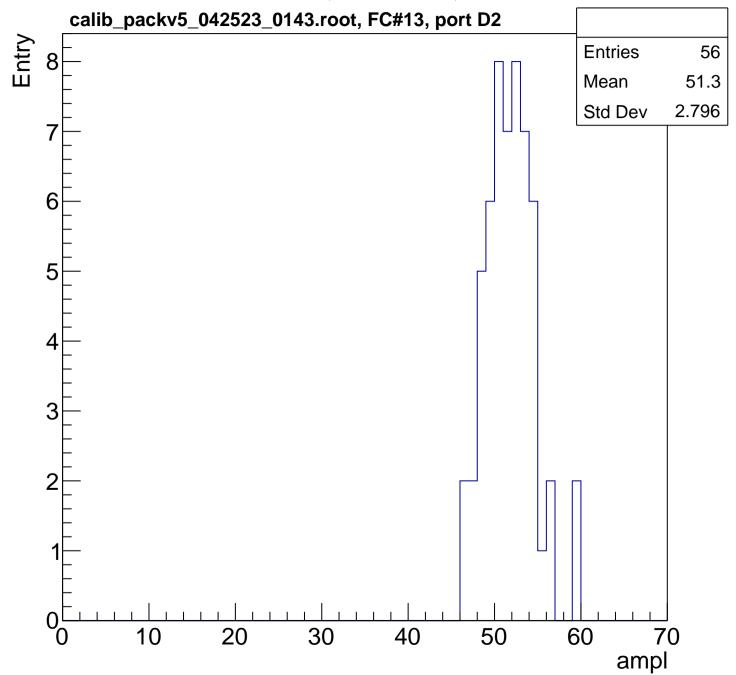


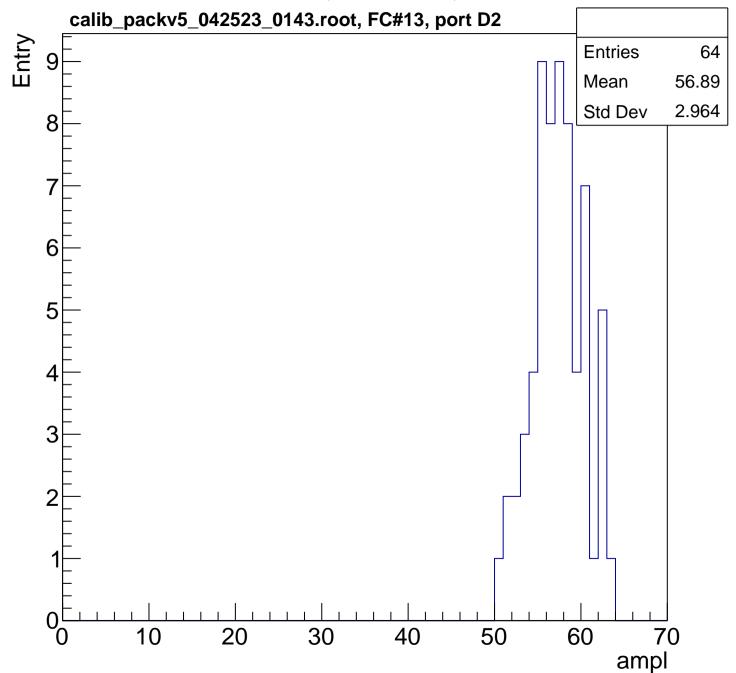


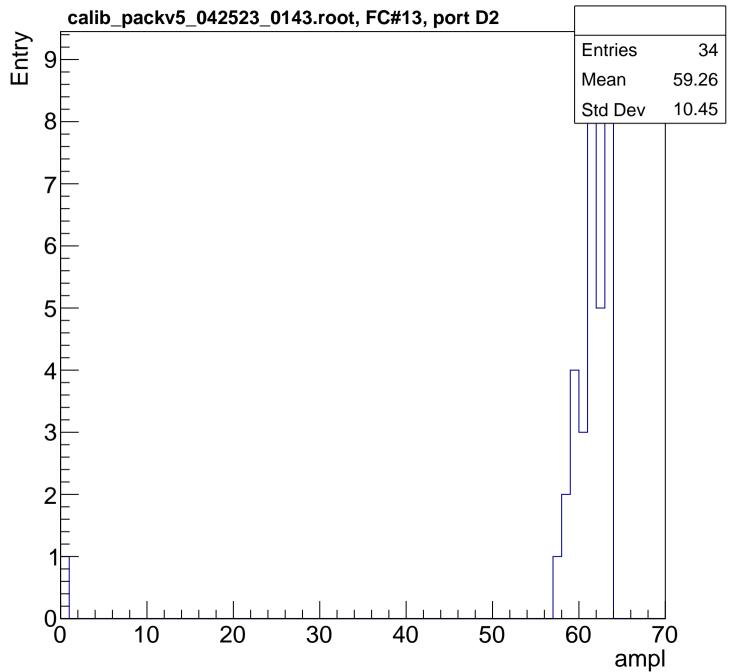


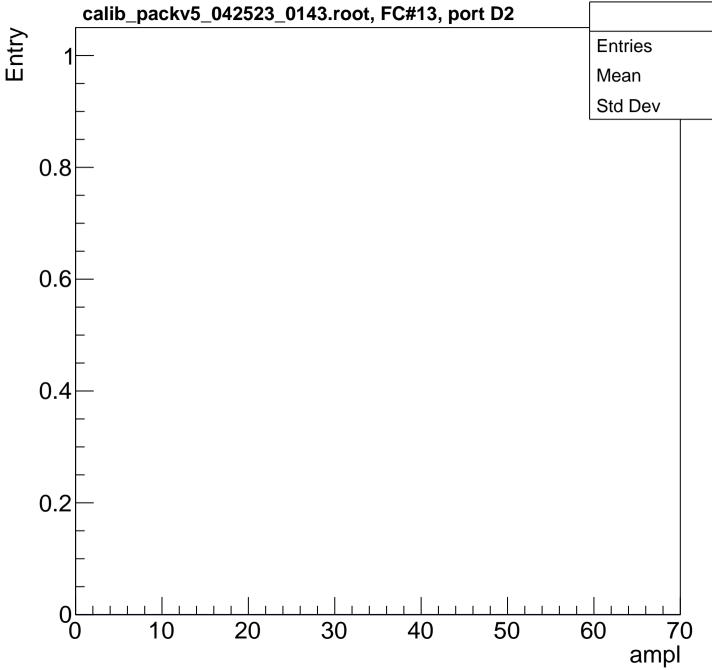


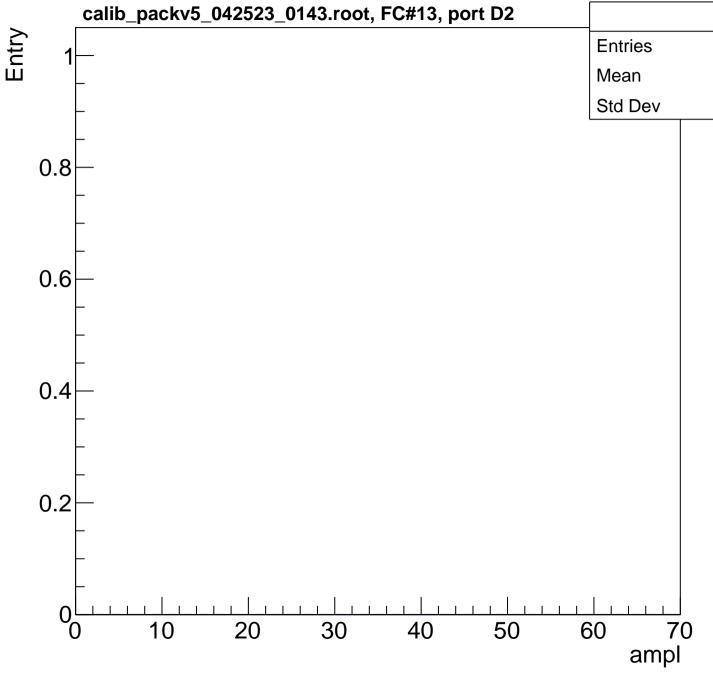


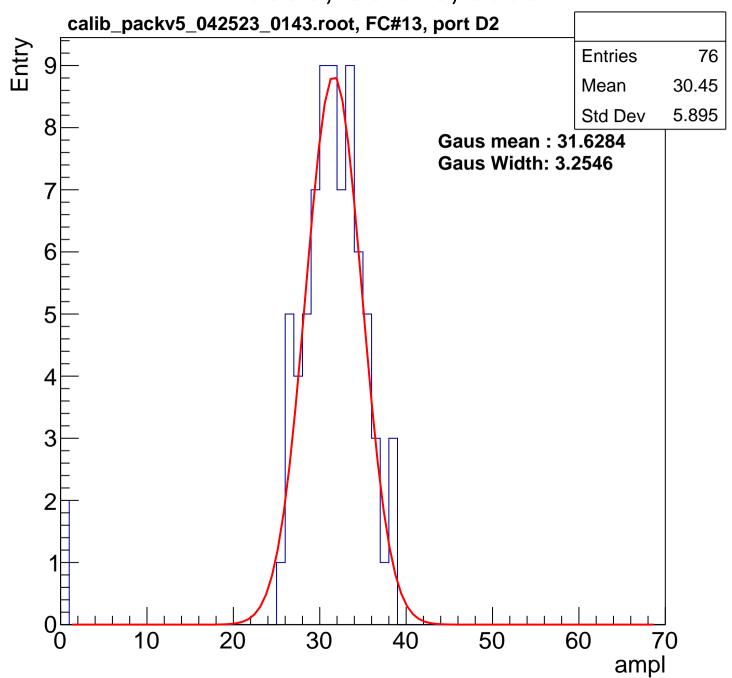


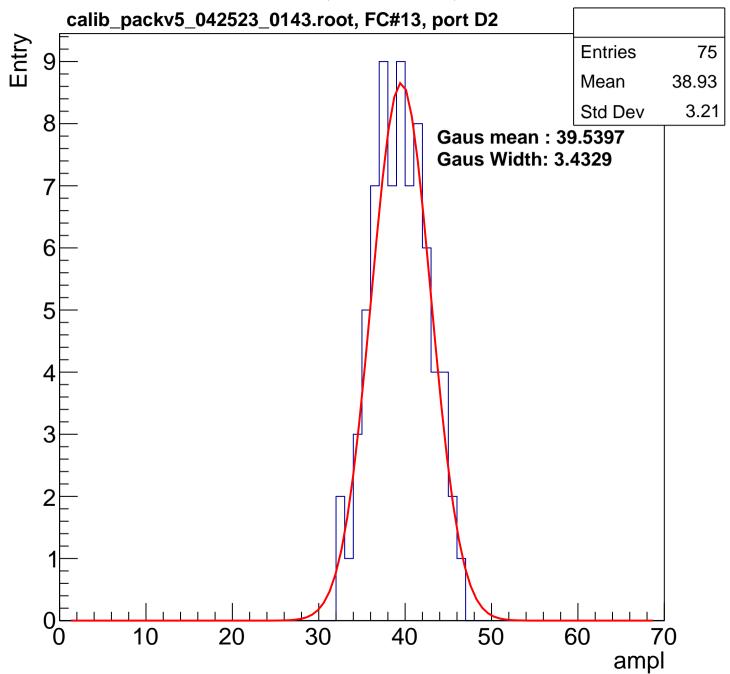


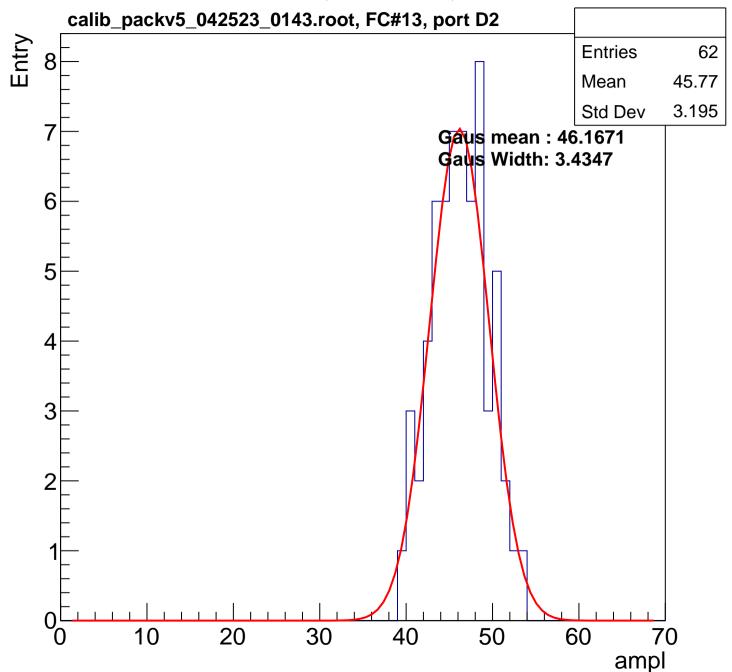


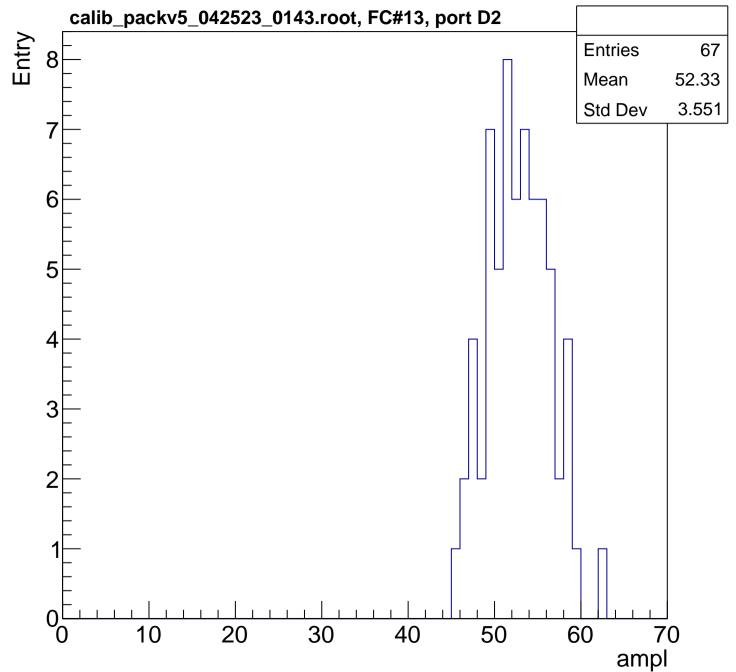


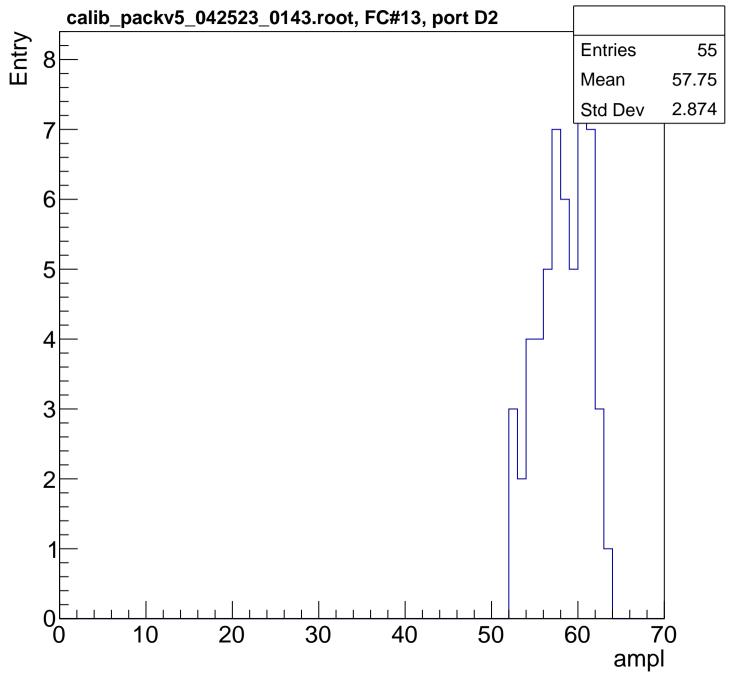


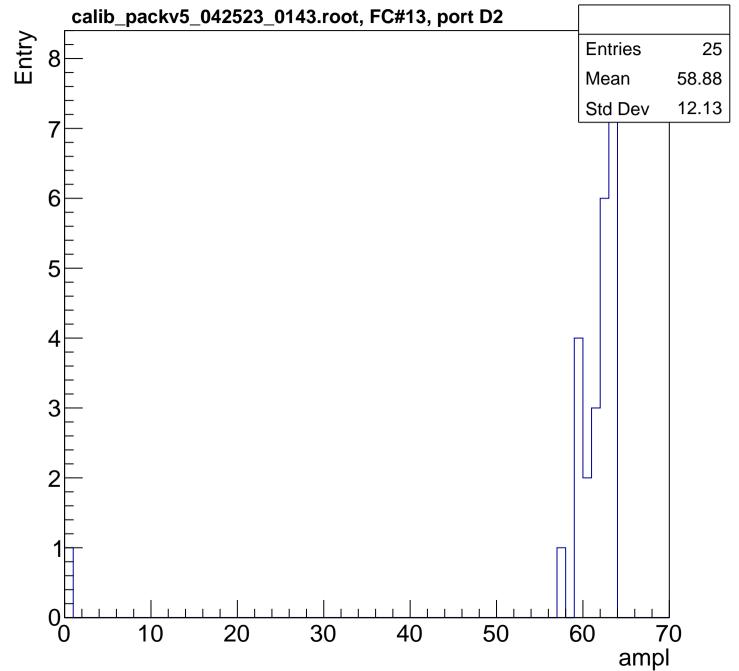


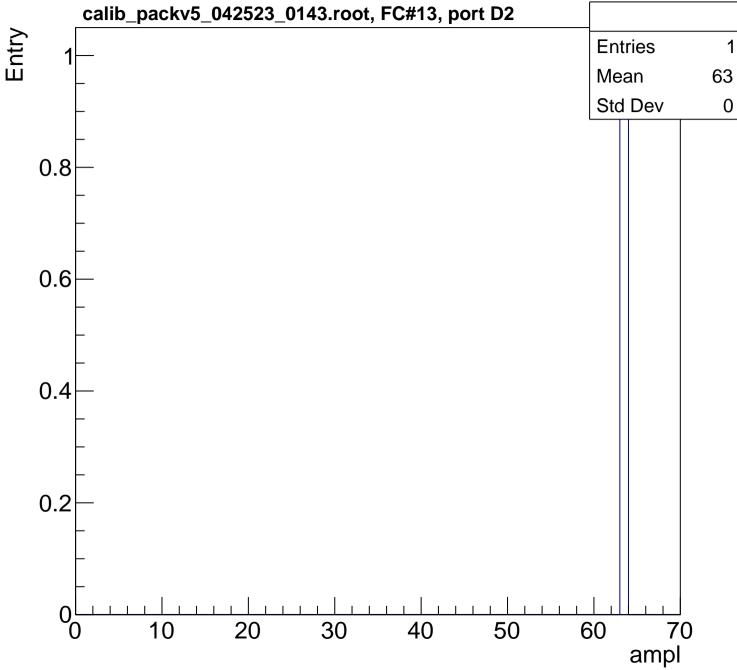


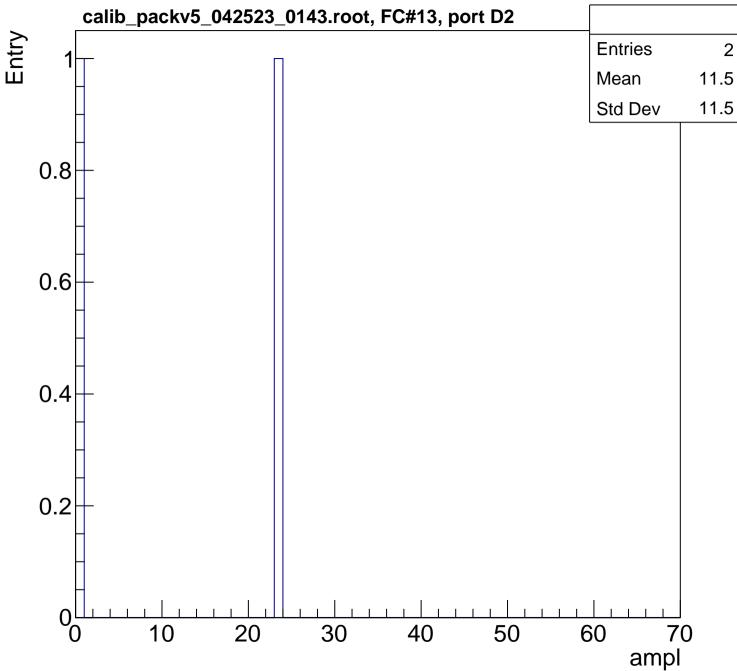


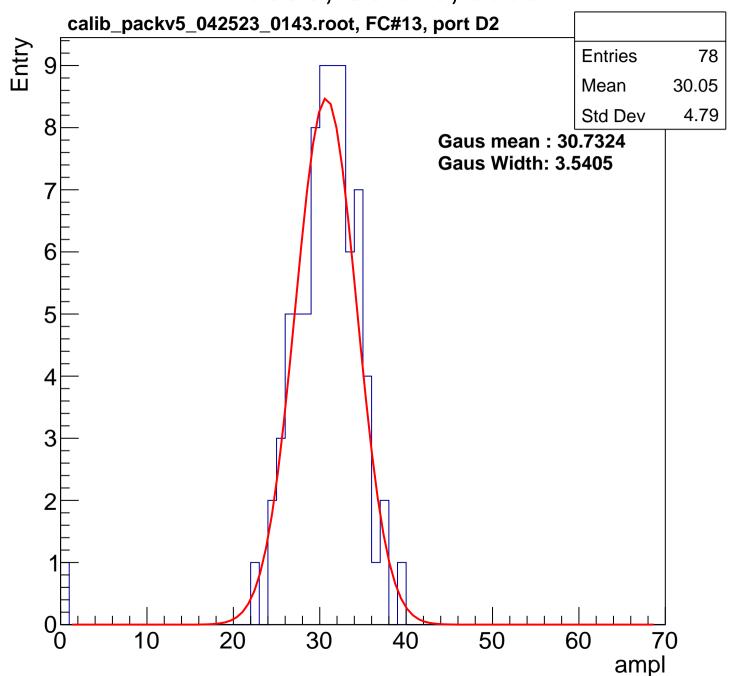


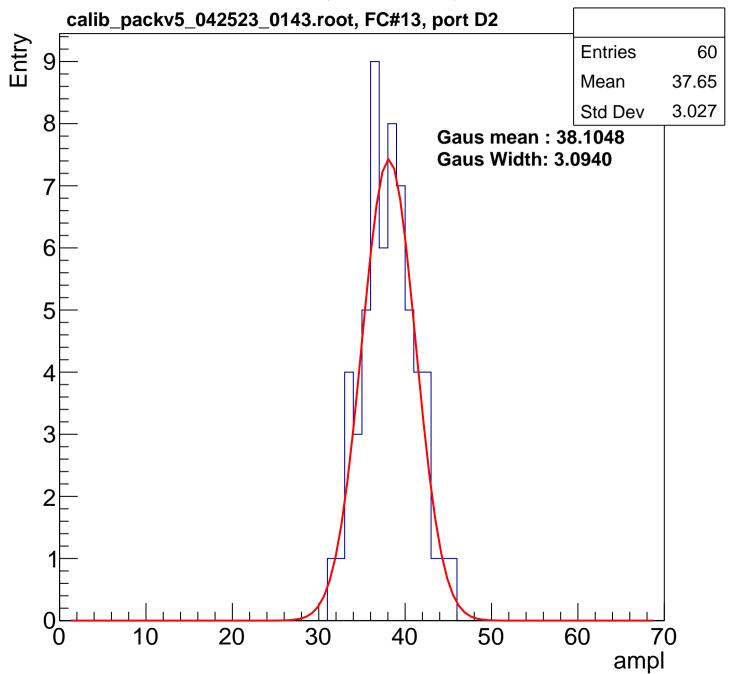


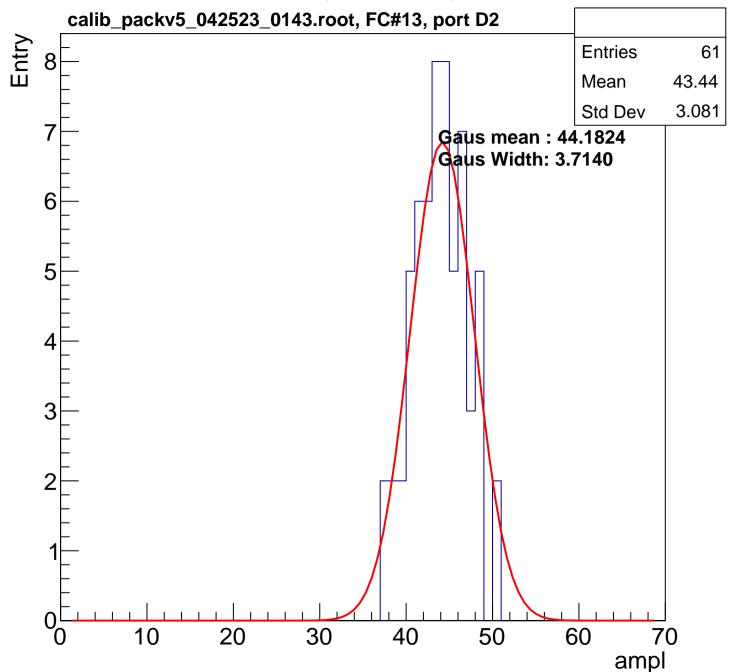


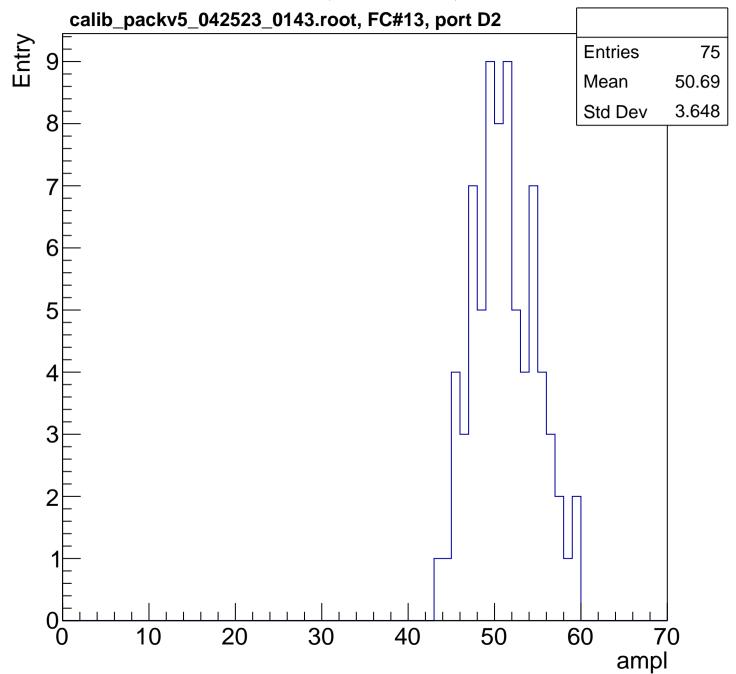


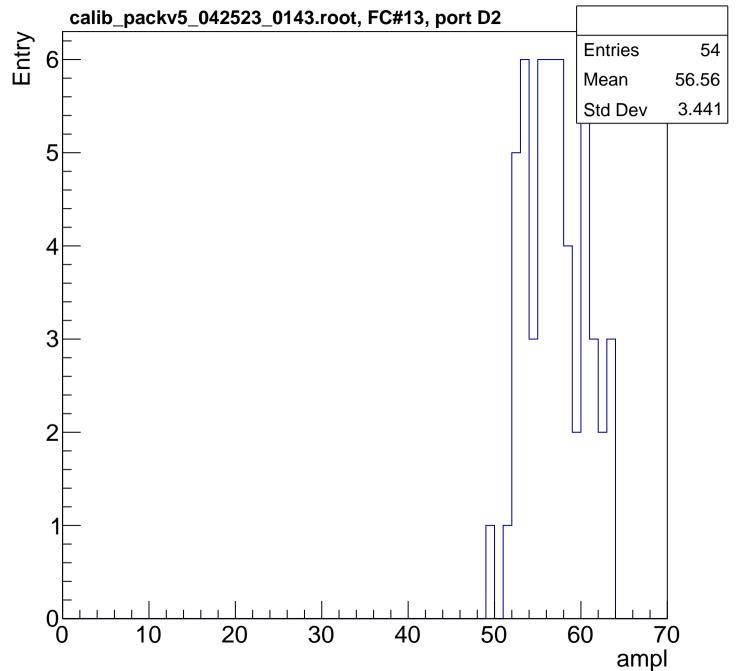


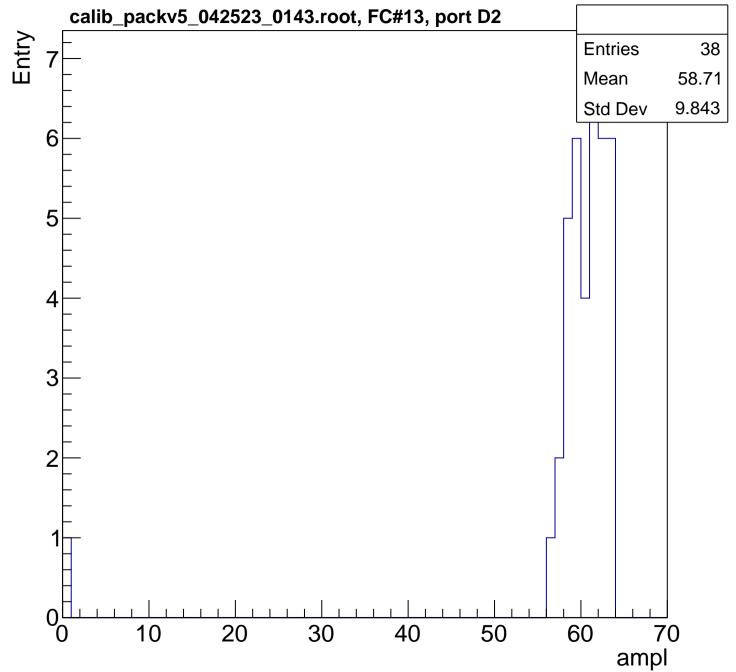


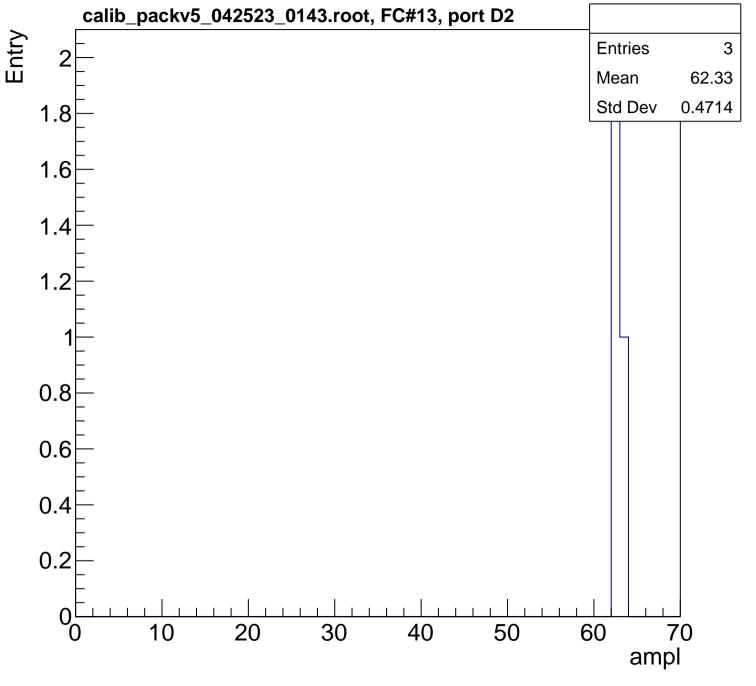


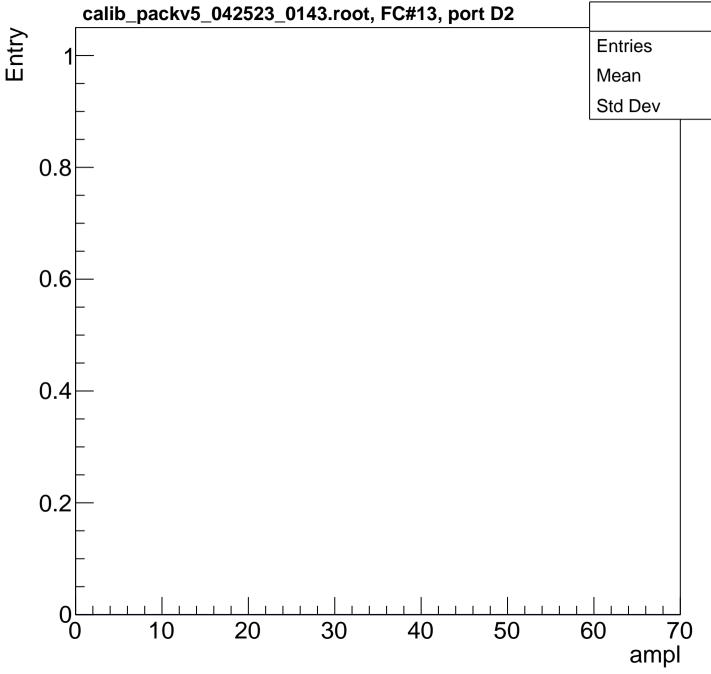


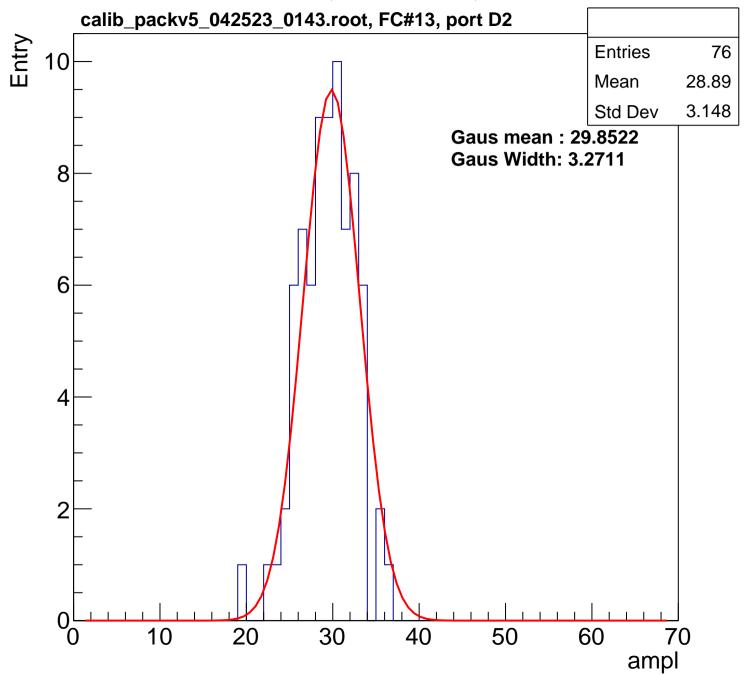


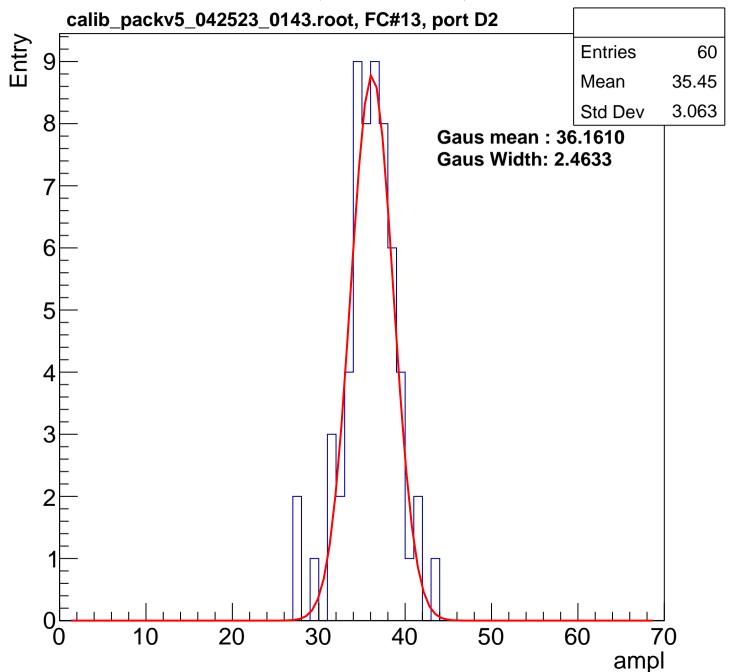


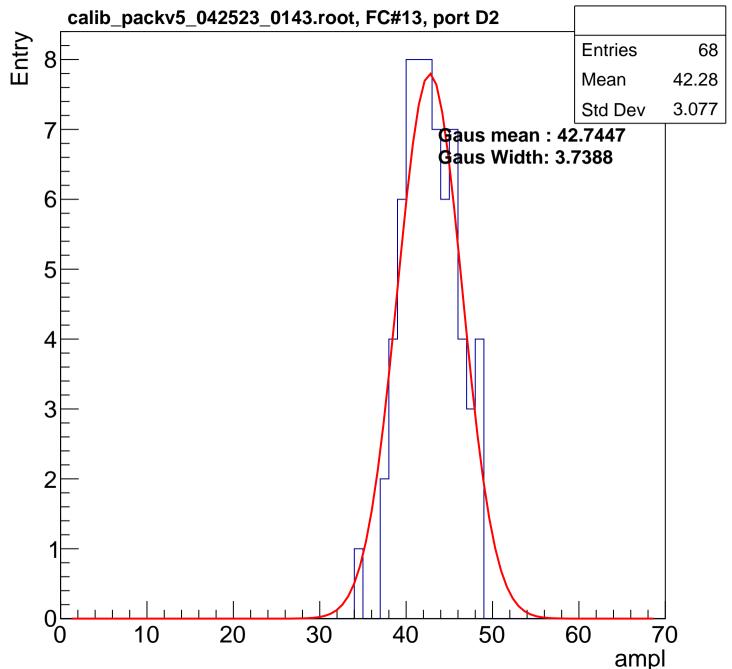


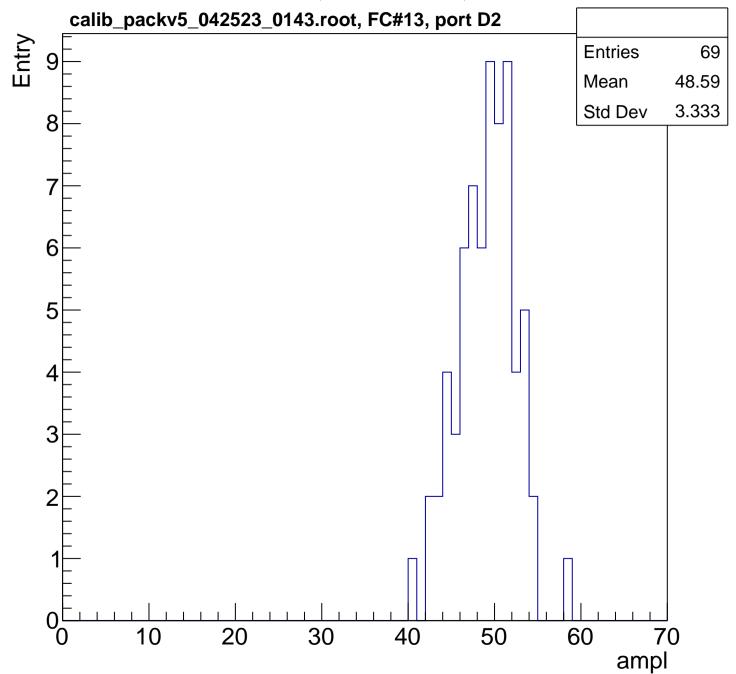


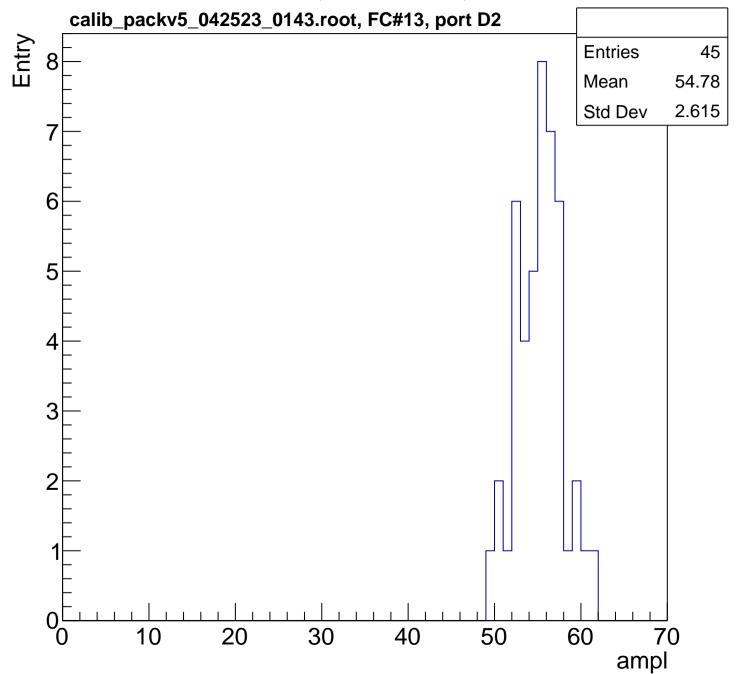


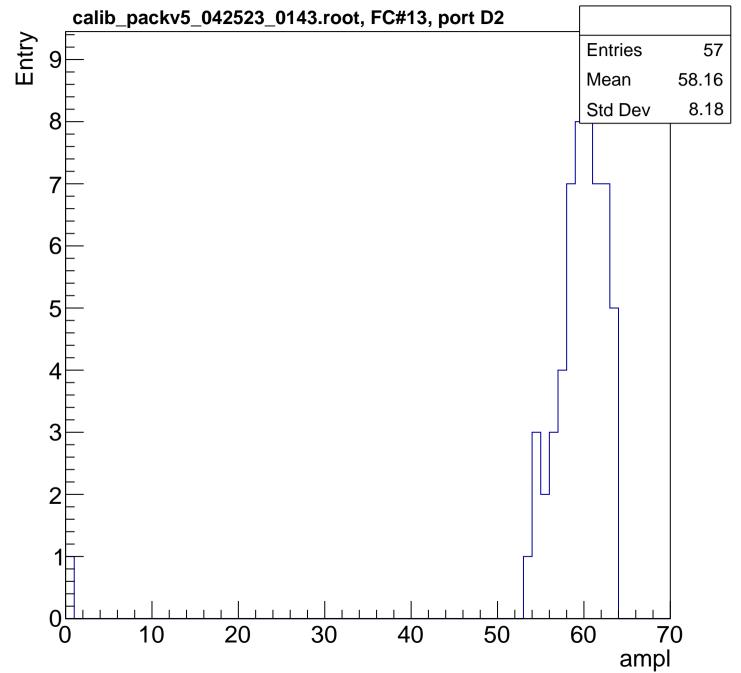


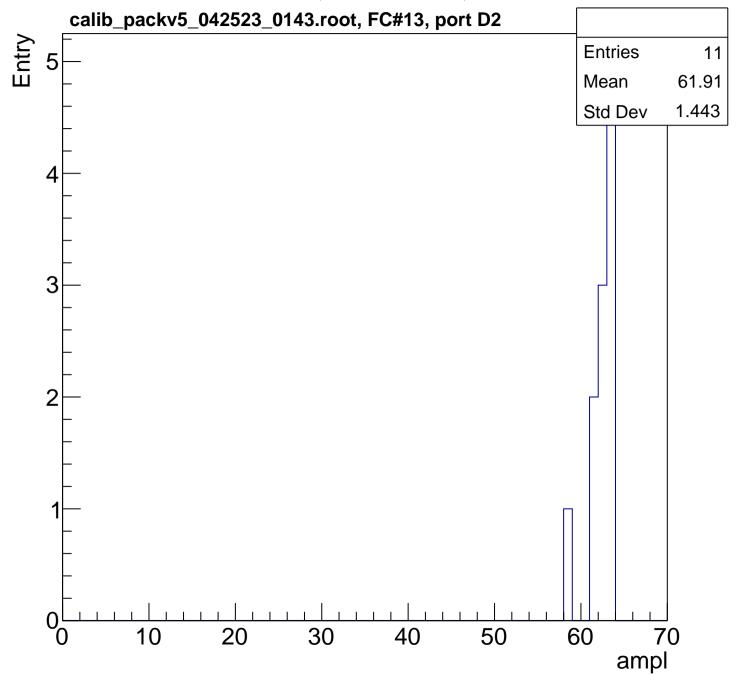


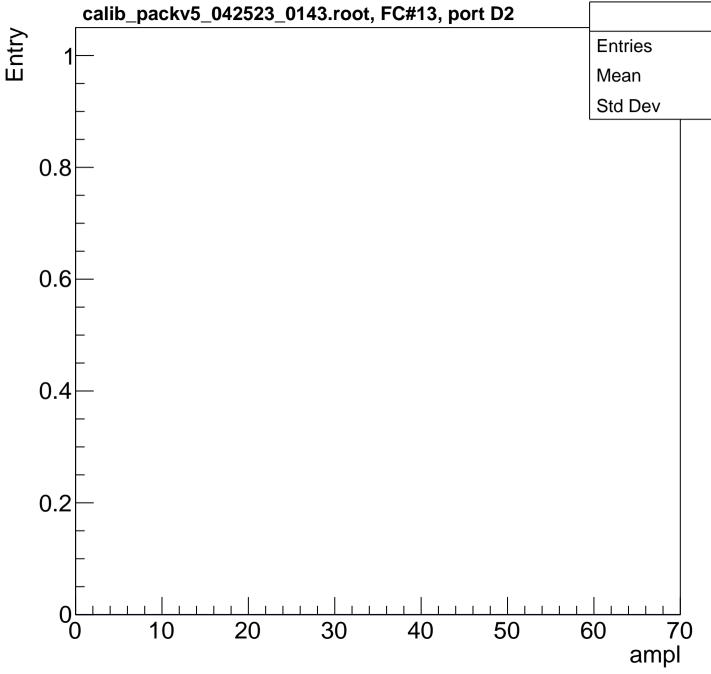


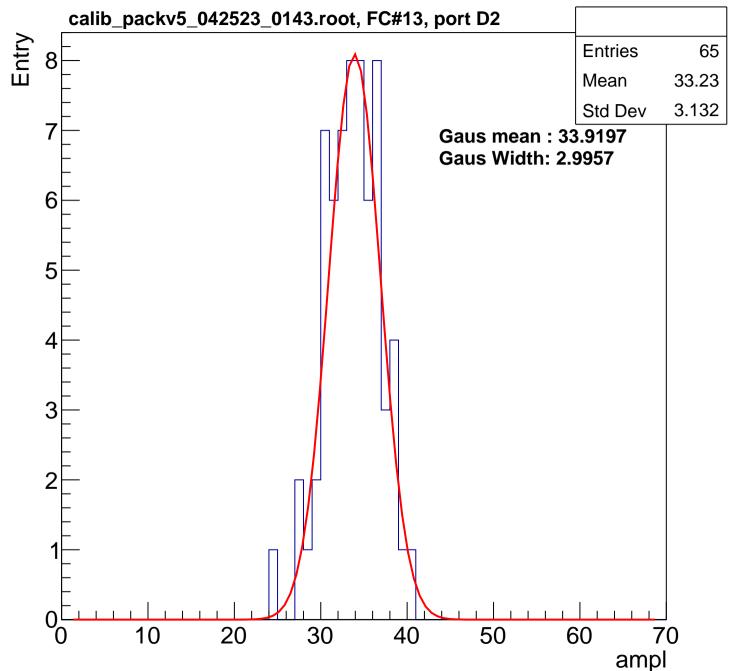


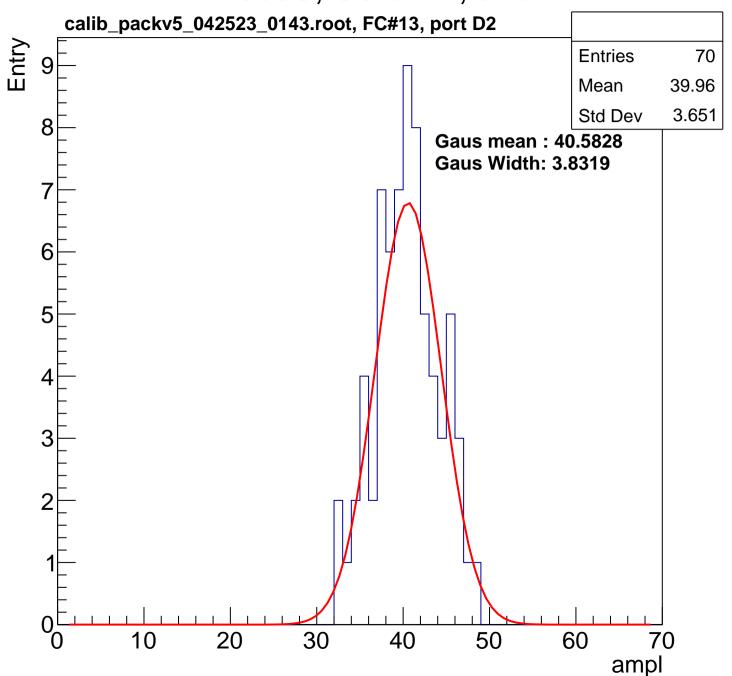


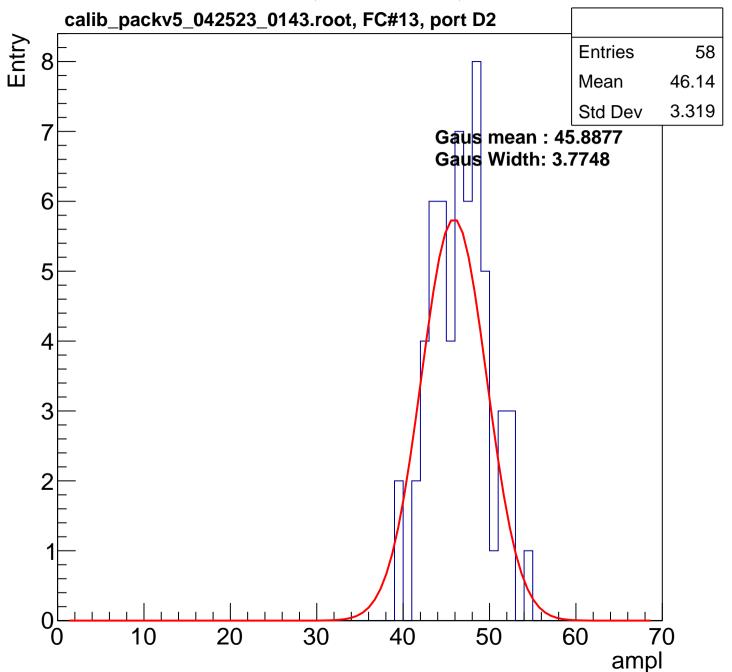


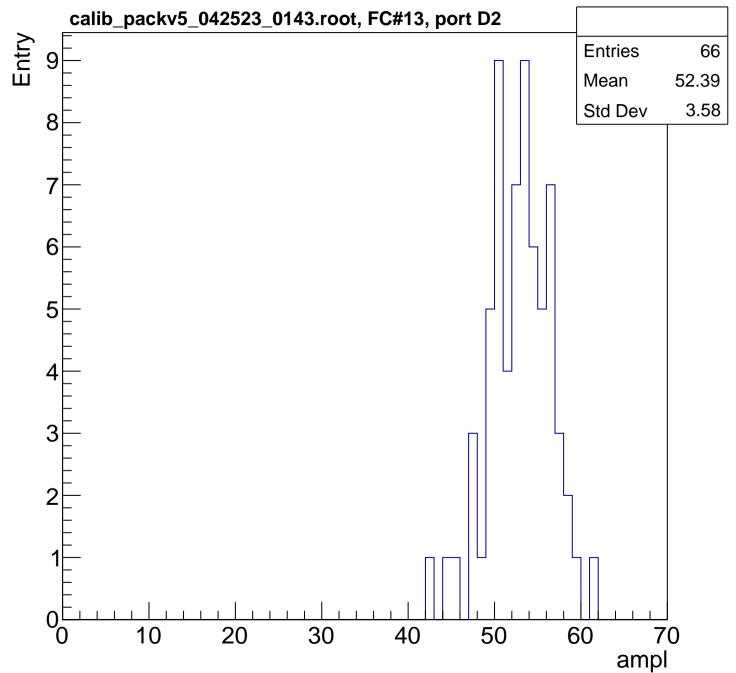


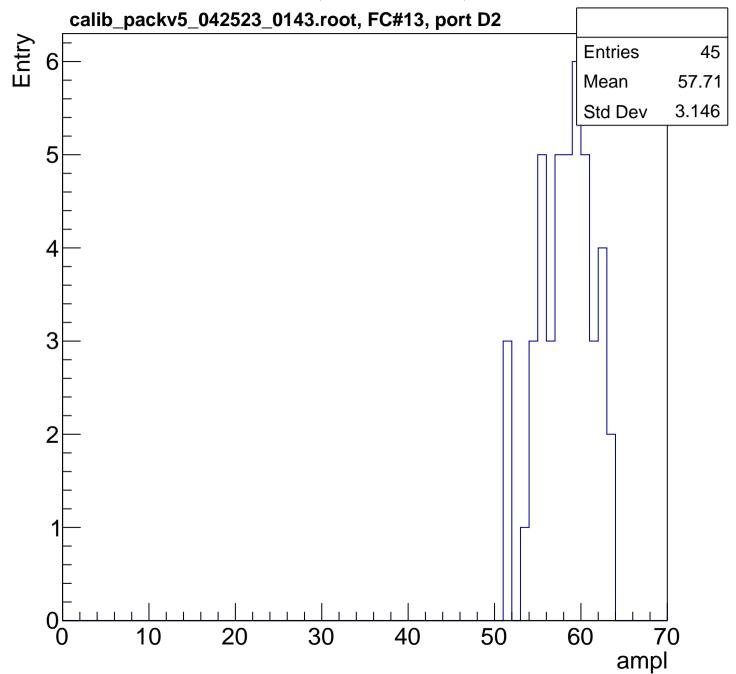


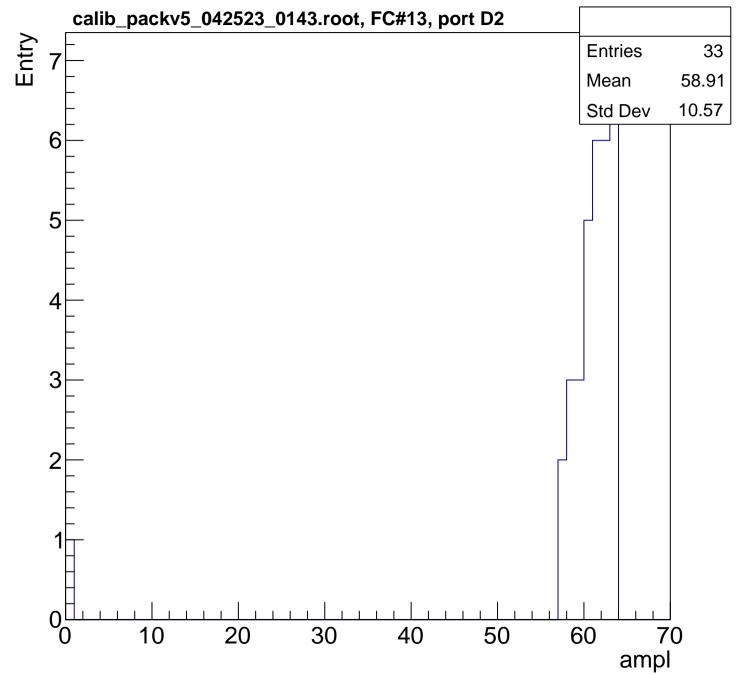


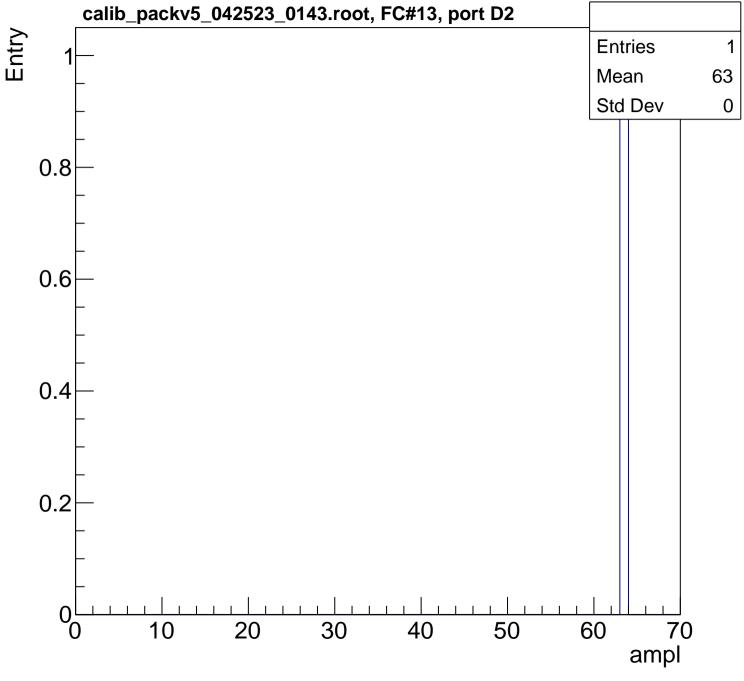




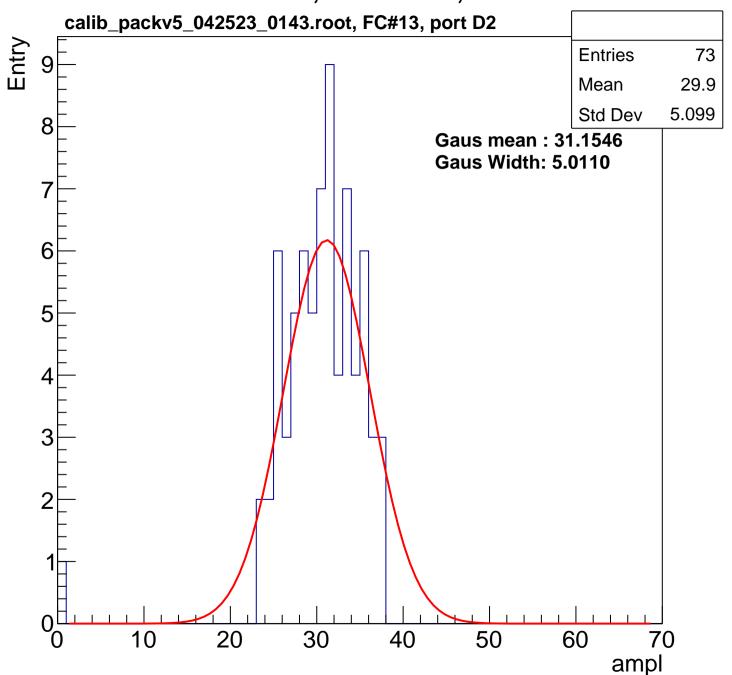


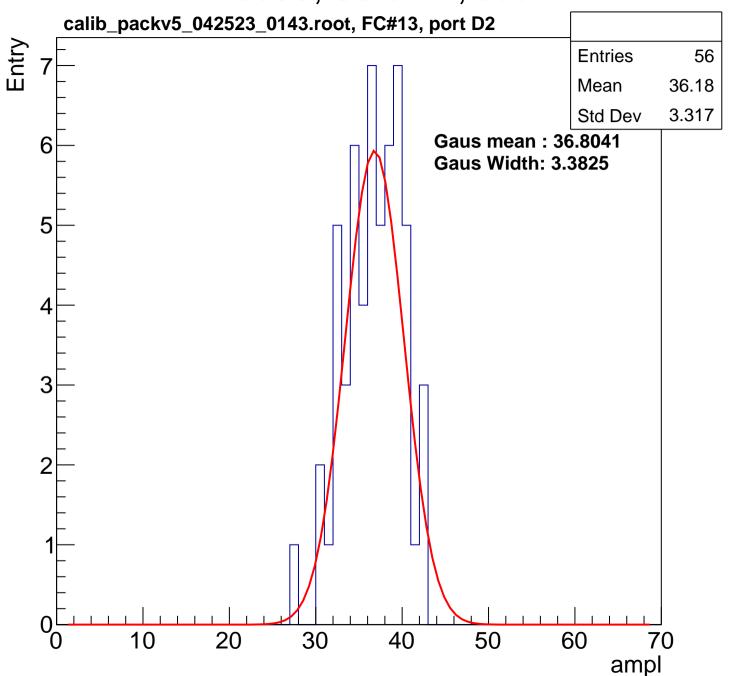


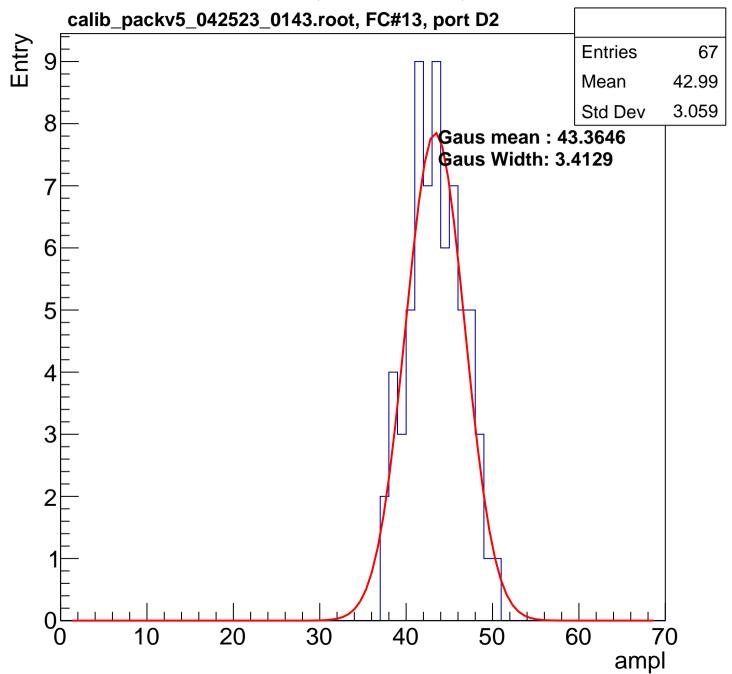


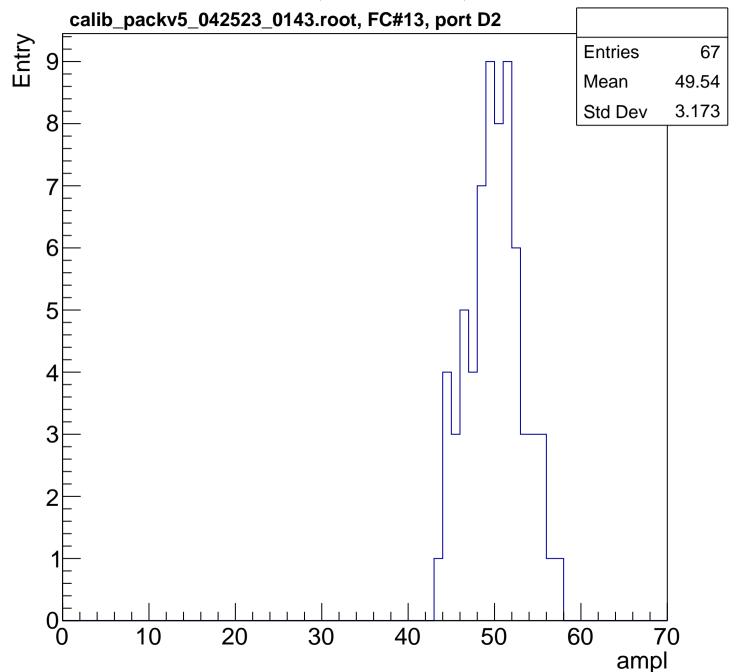


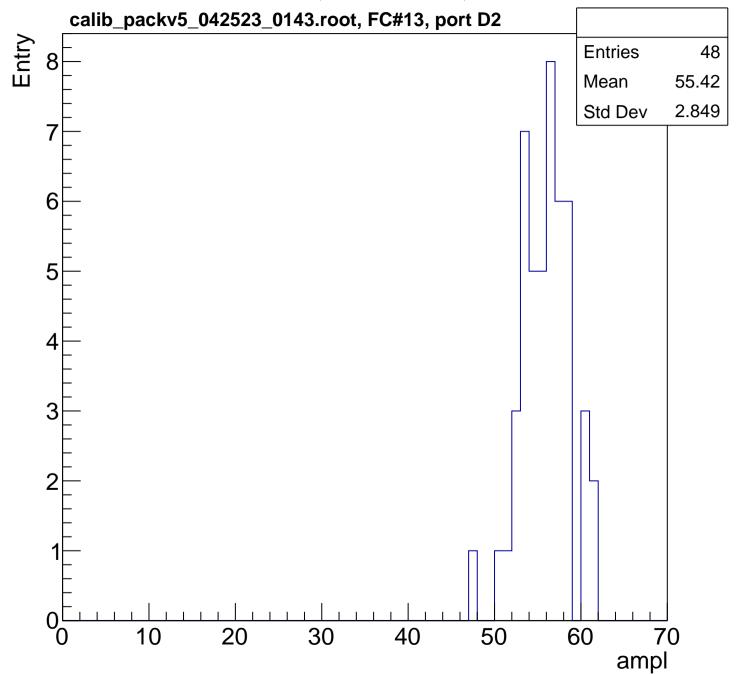


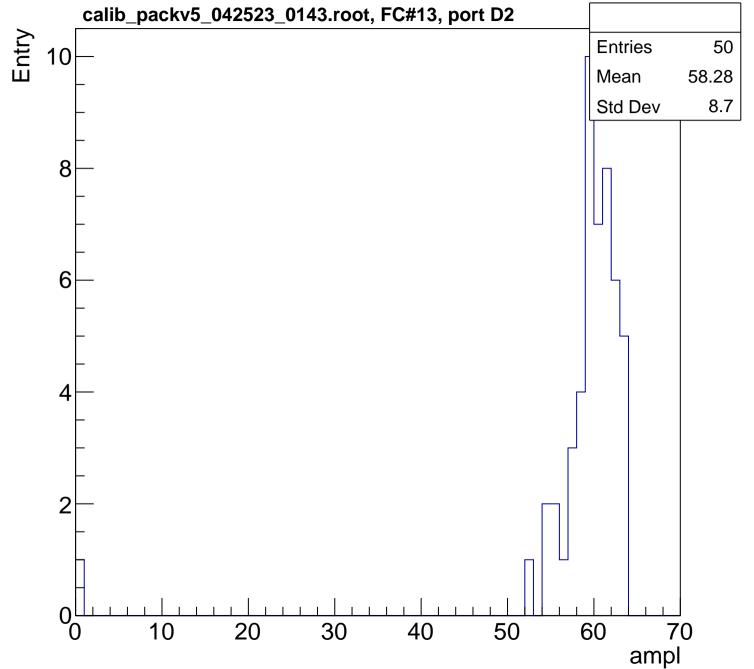


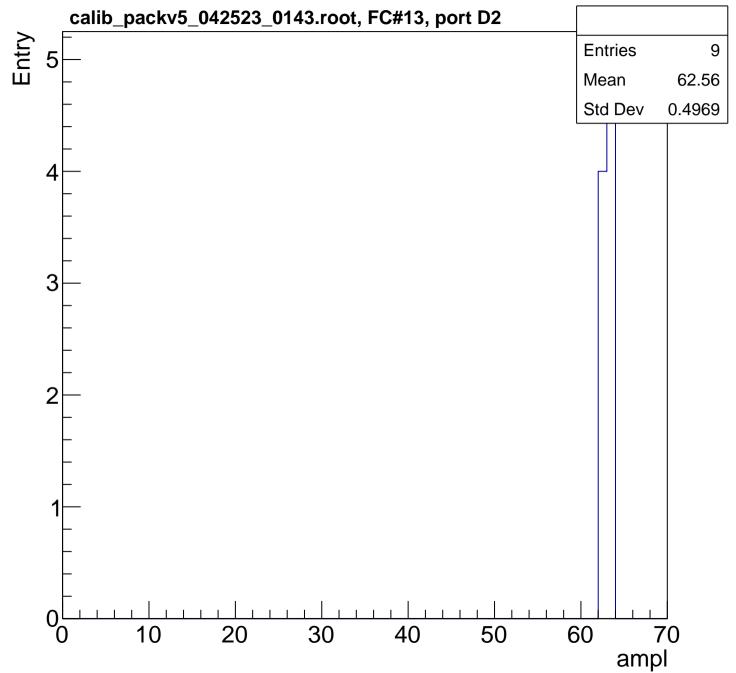




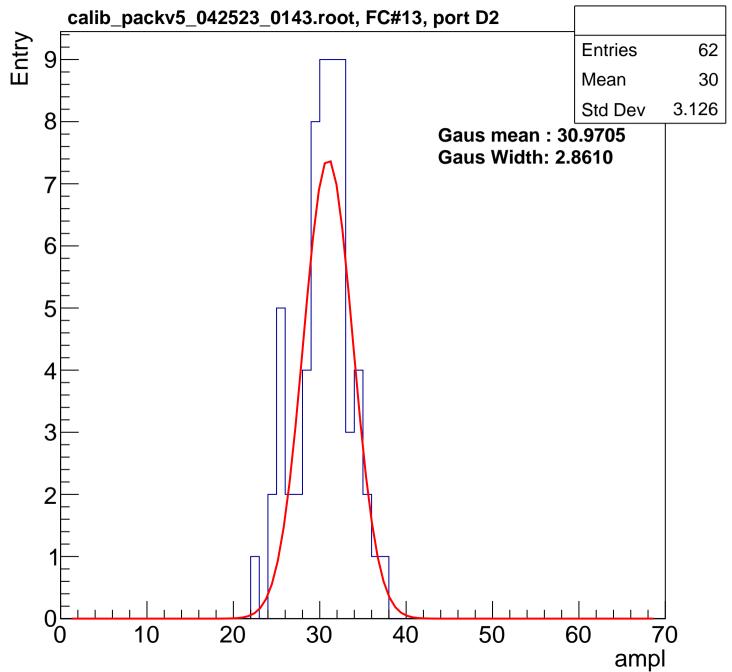


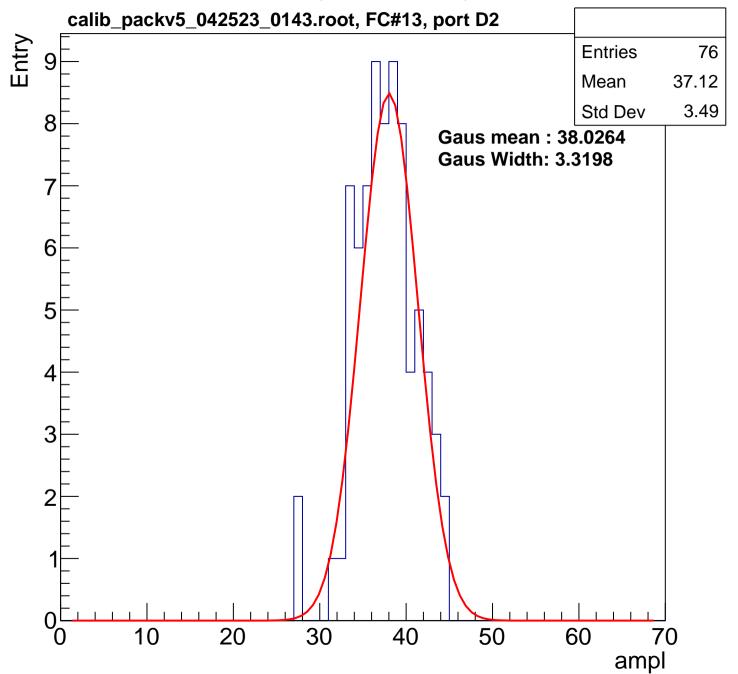


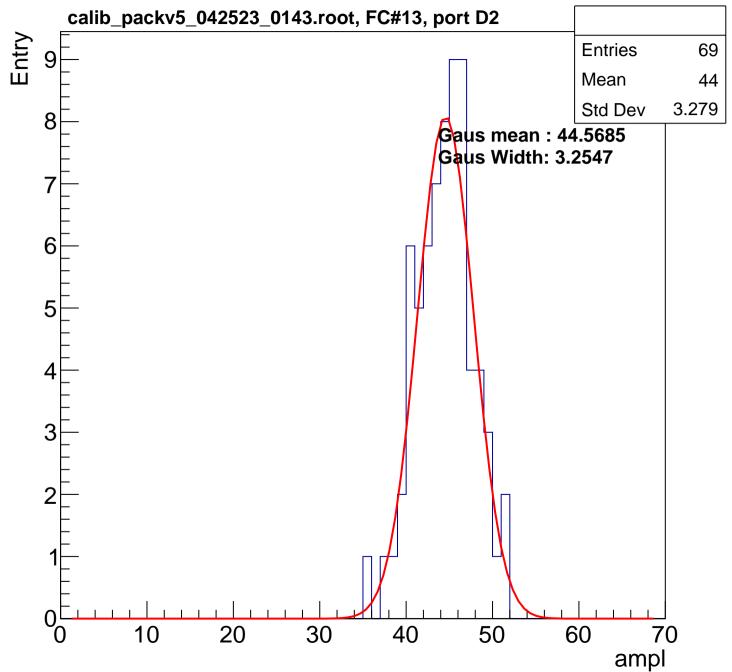


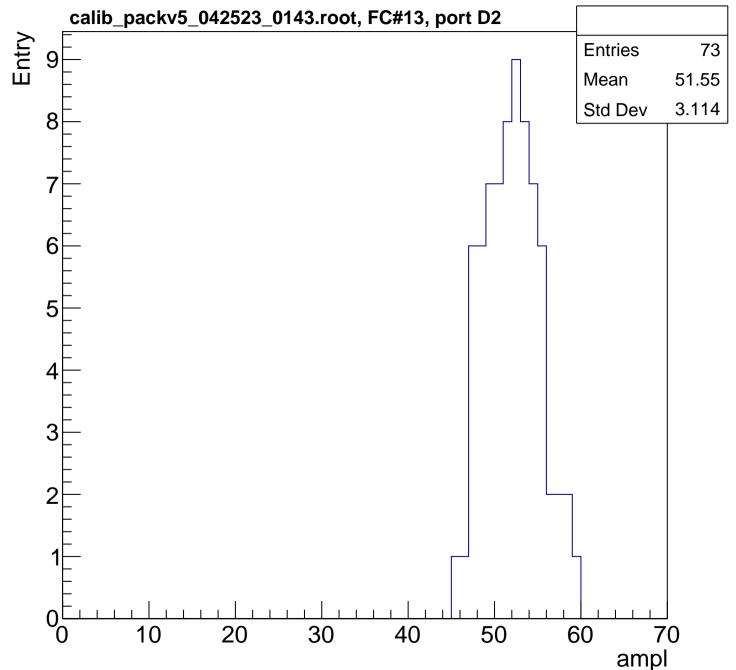


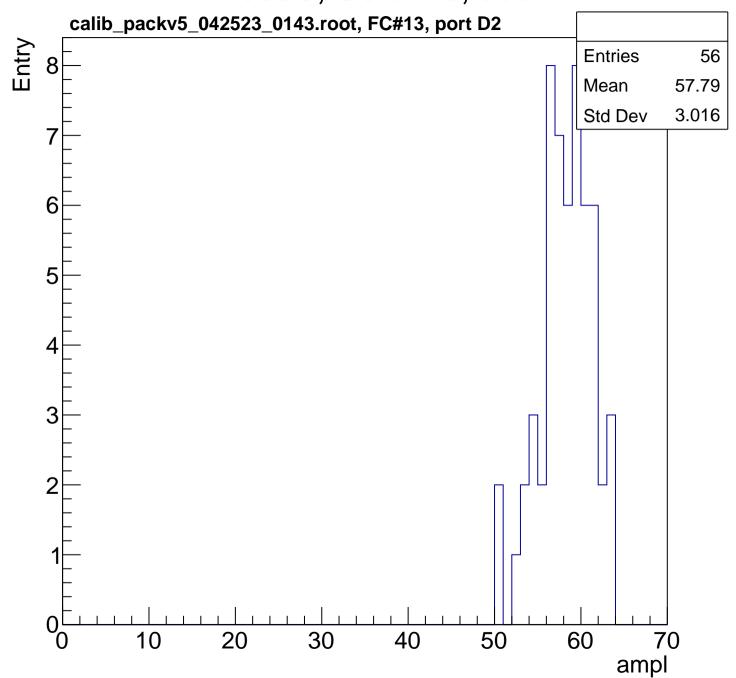
B1L003S, U8-ch12, adc7 calib\_packv5\_042523\_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

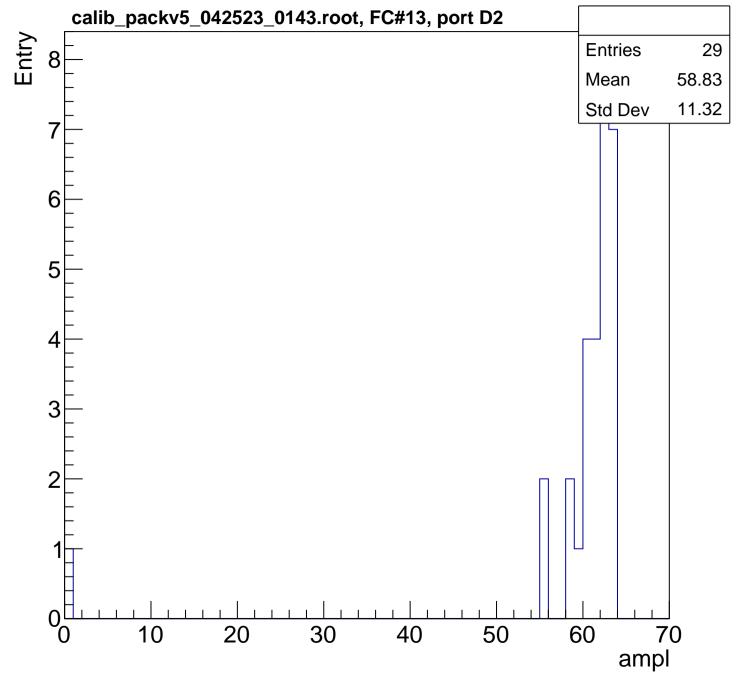


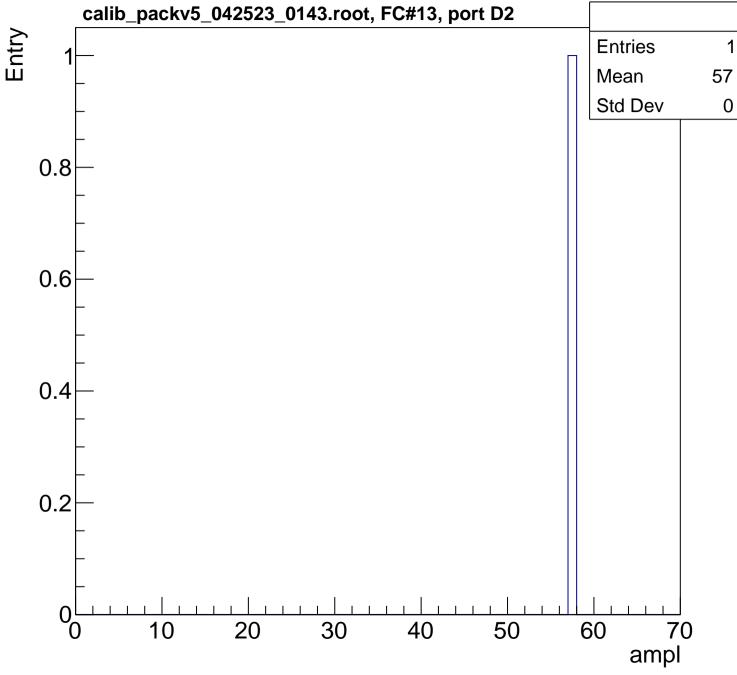


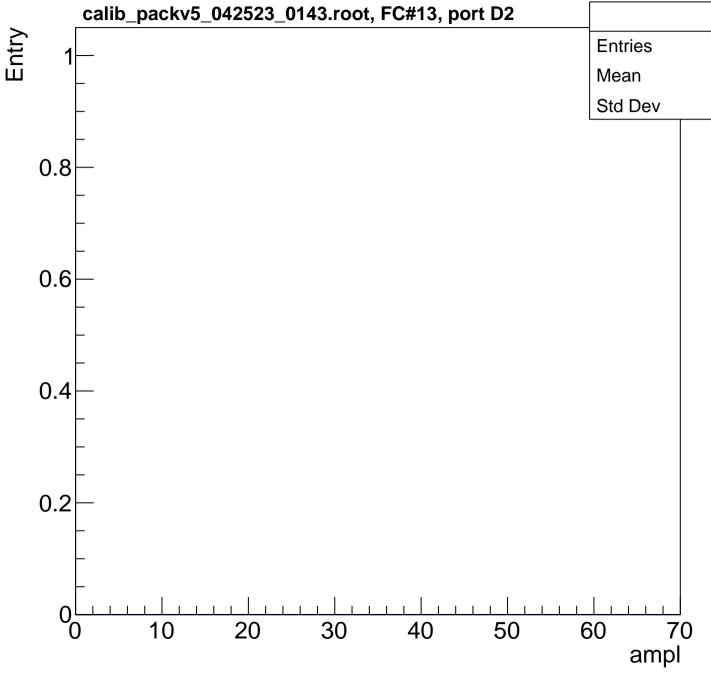


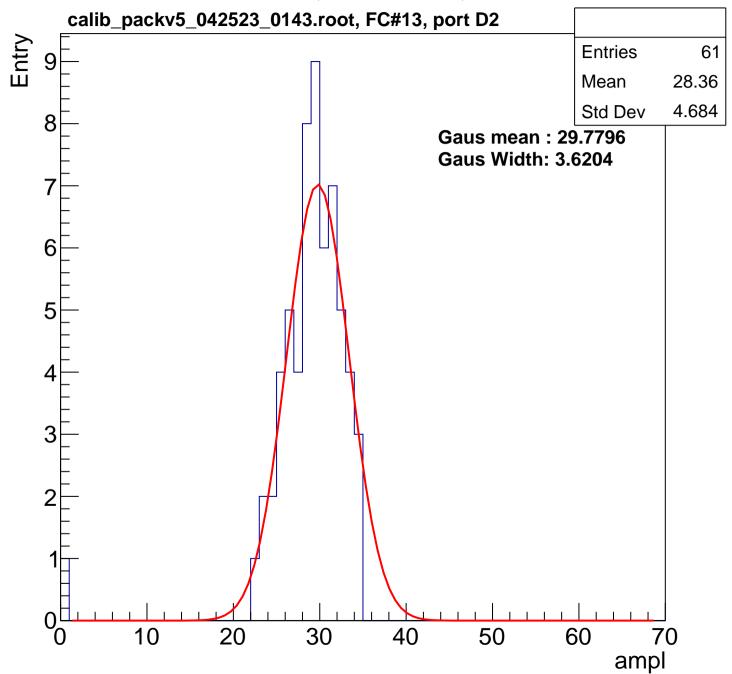


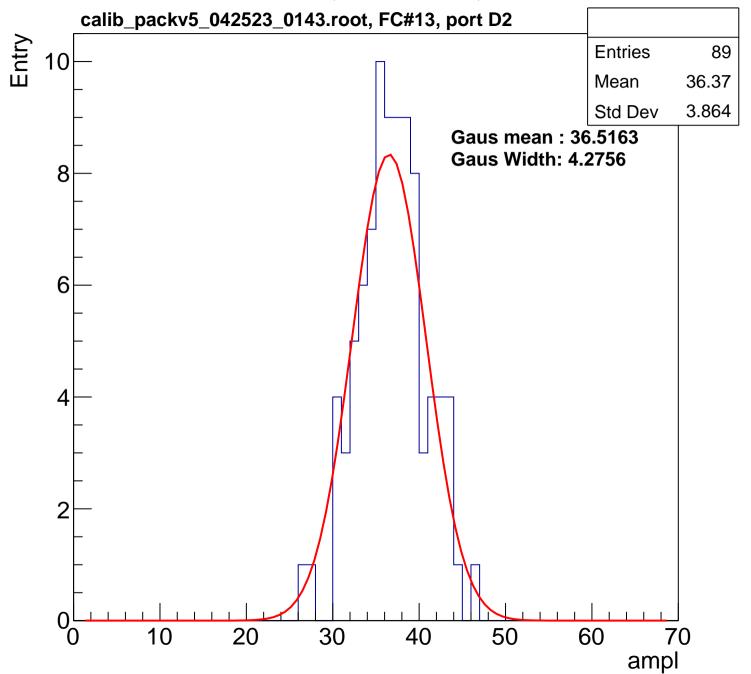


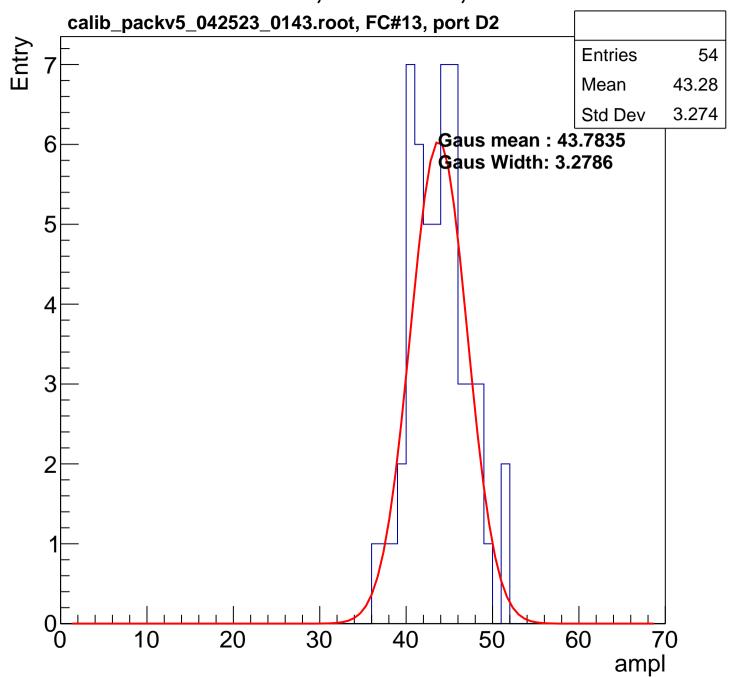


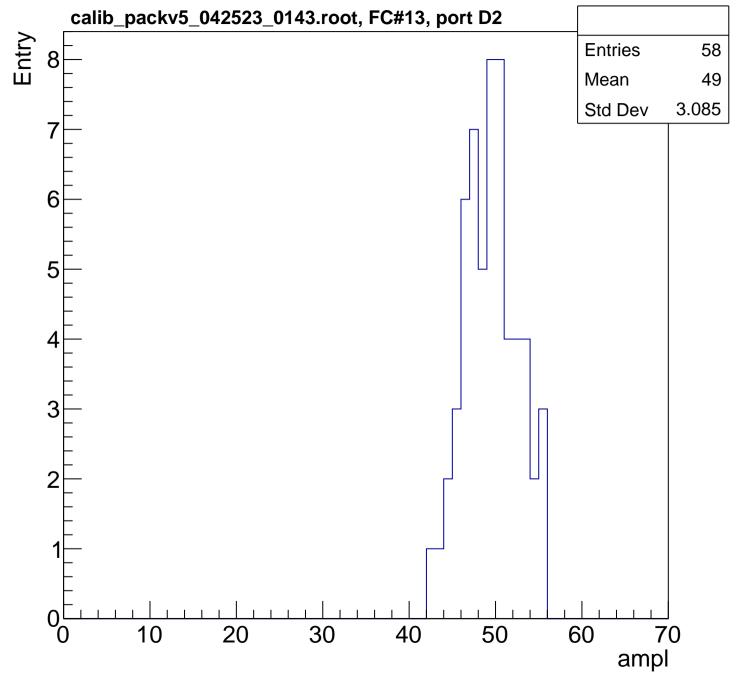


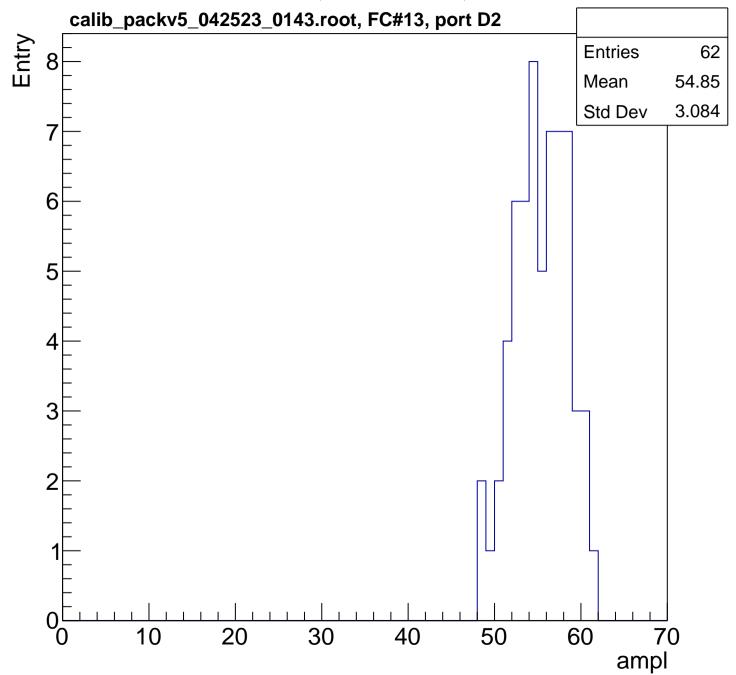


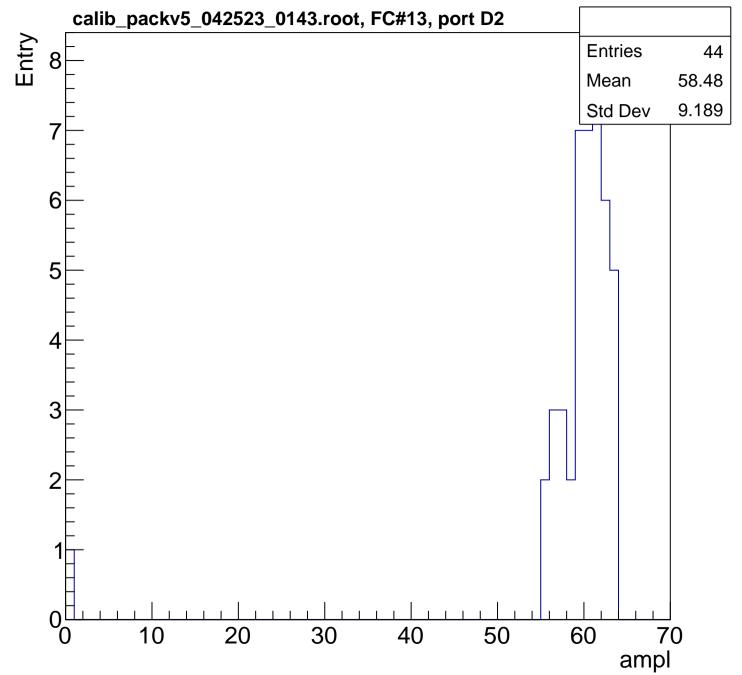


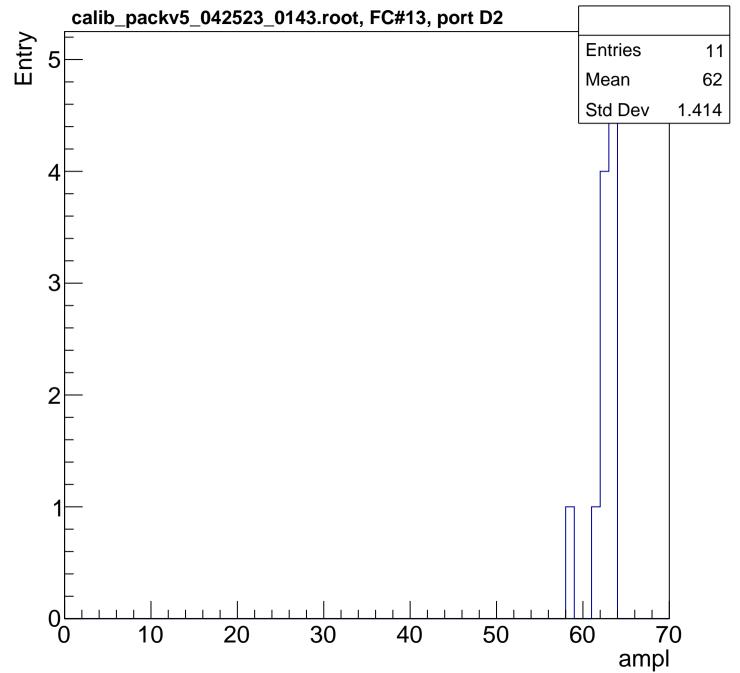




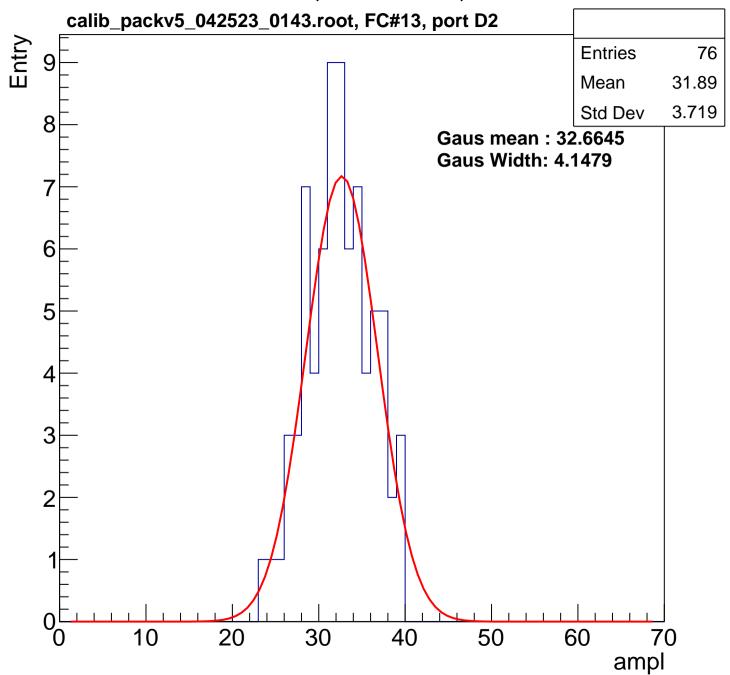


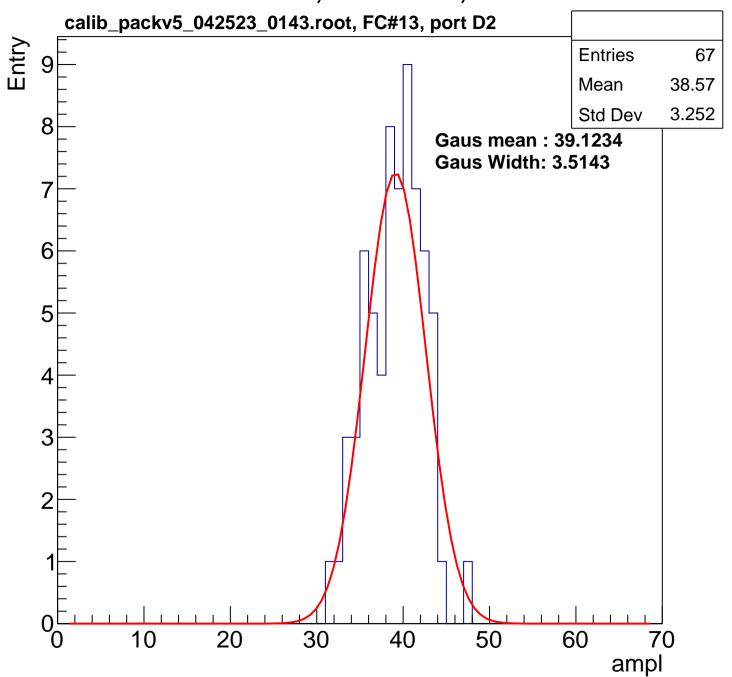


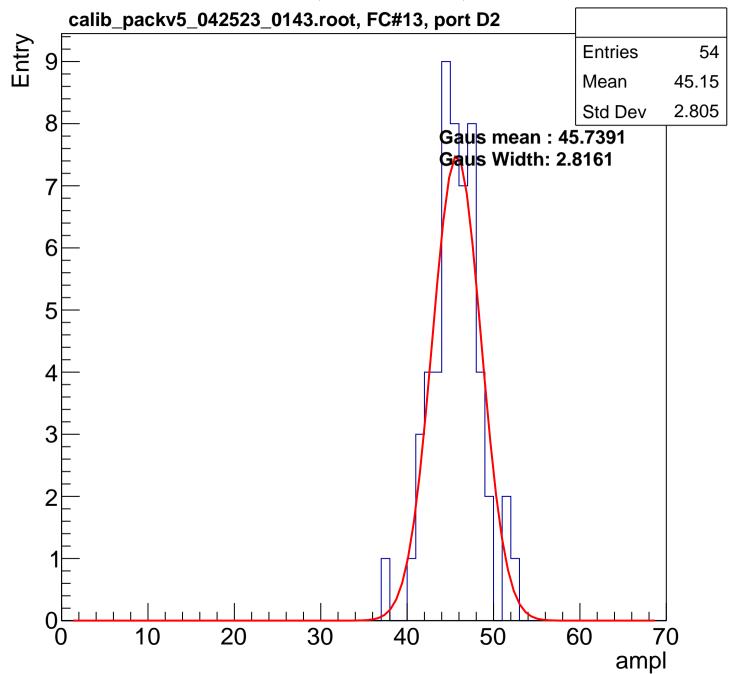


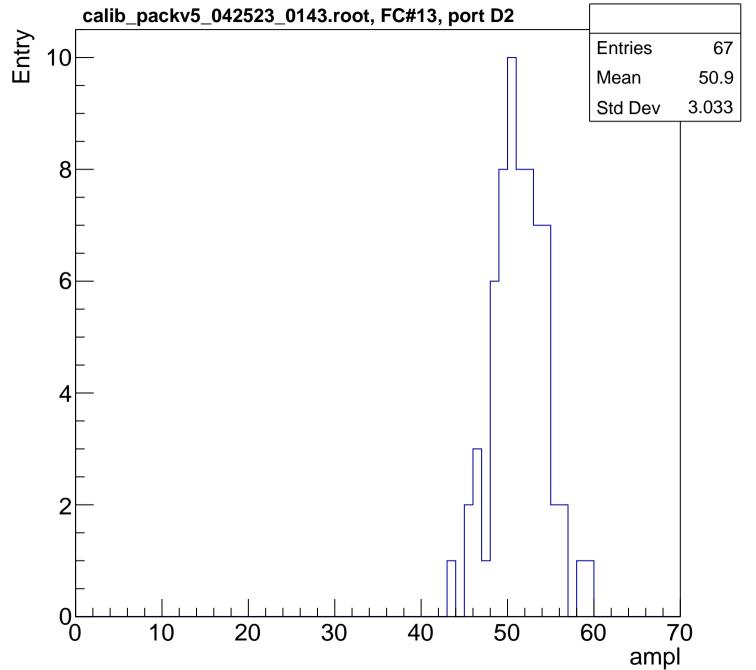


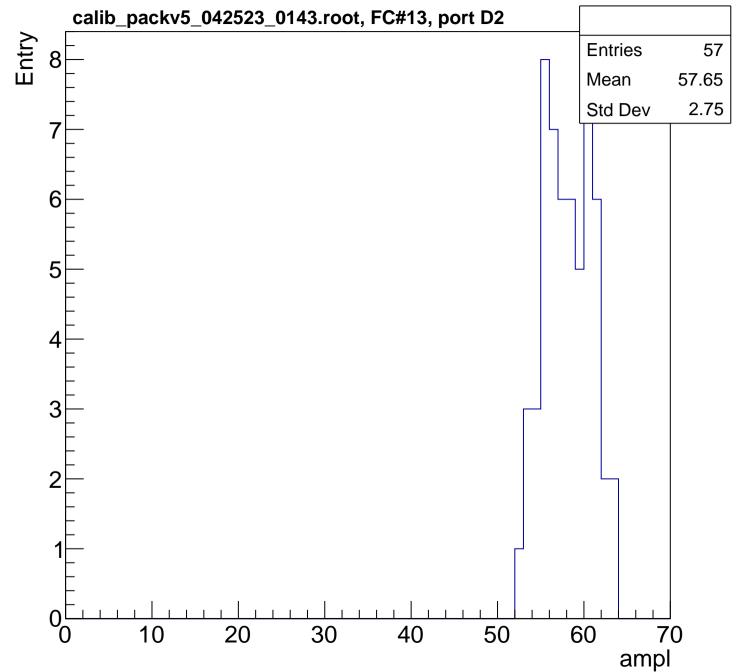


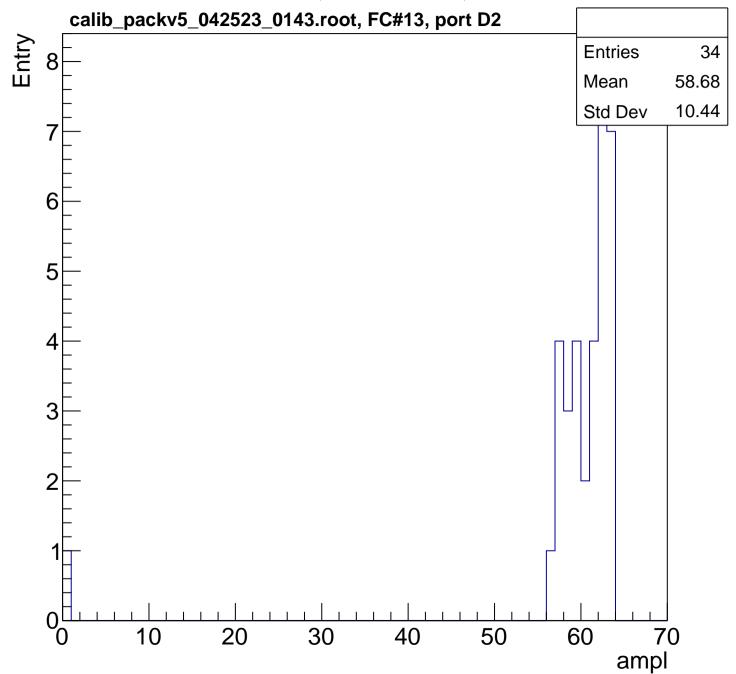


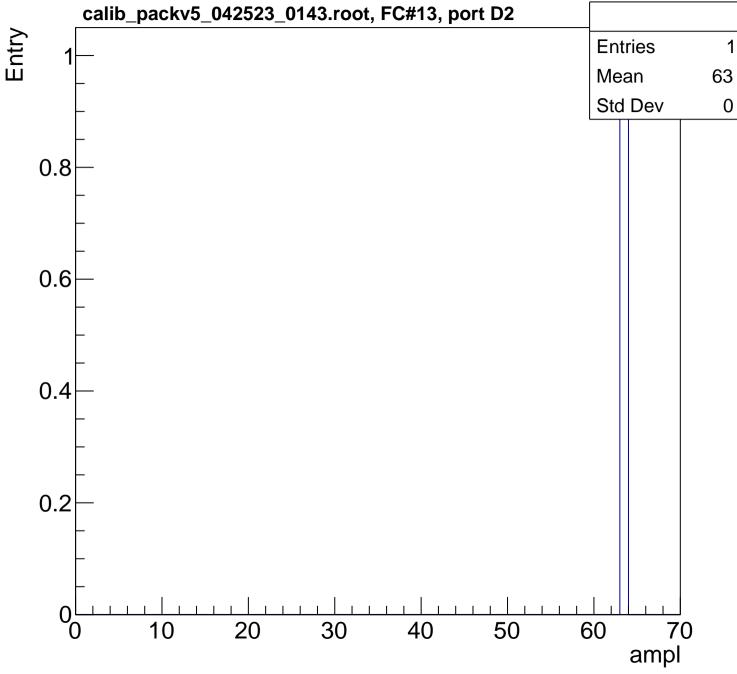


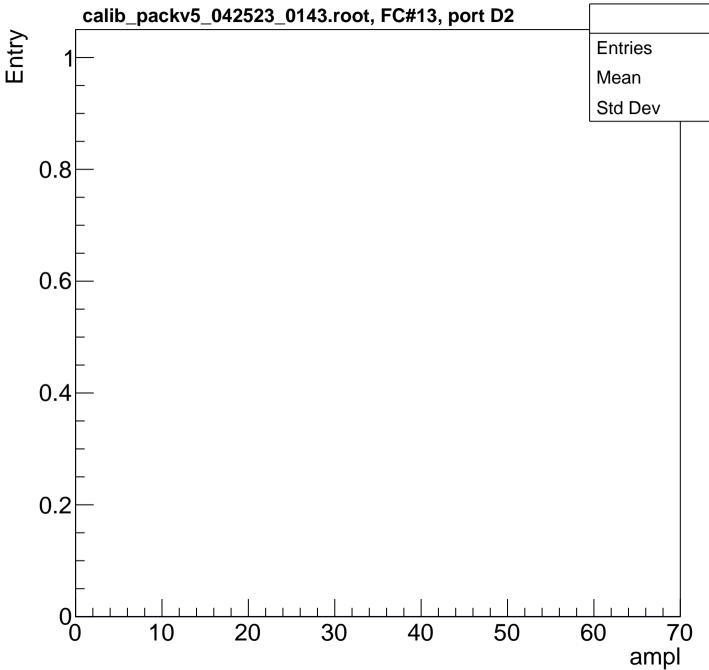


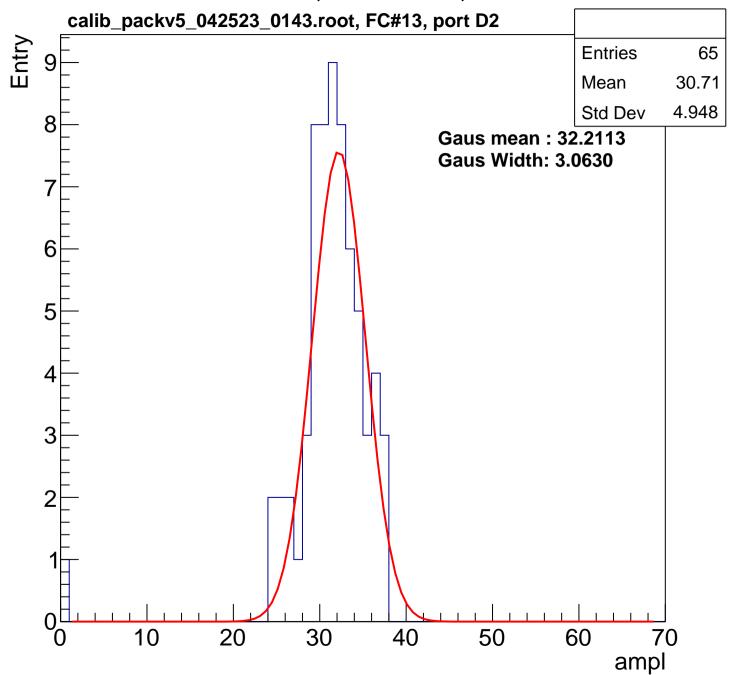


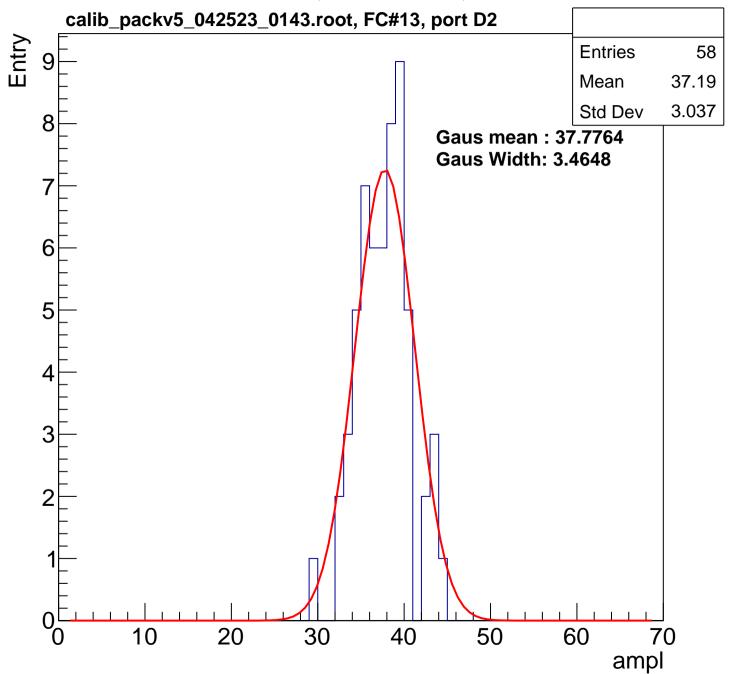


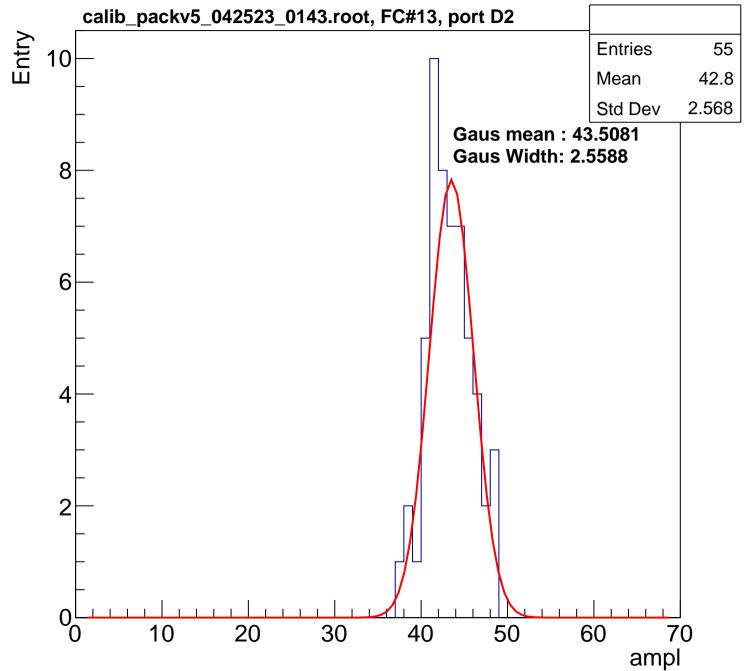


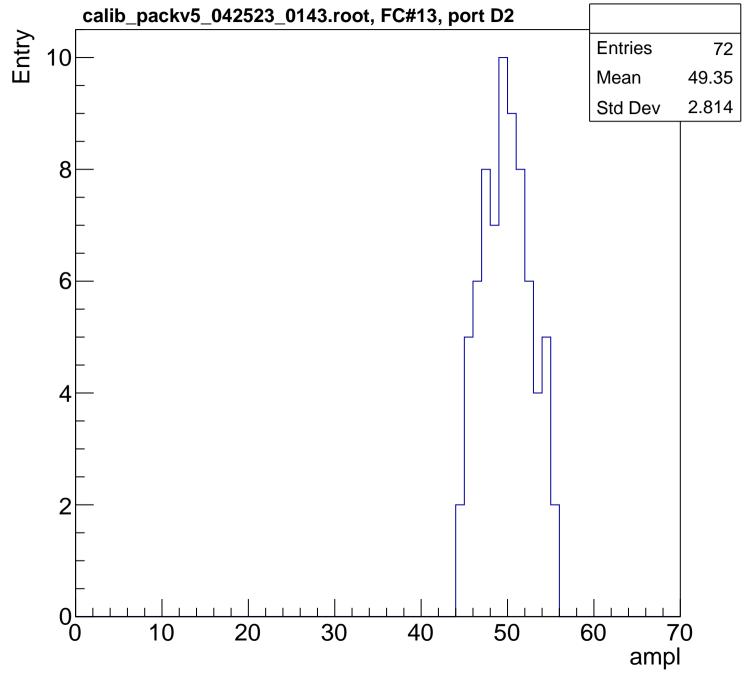


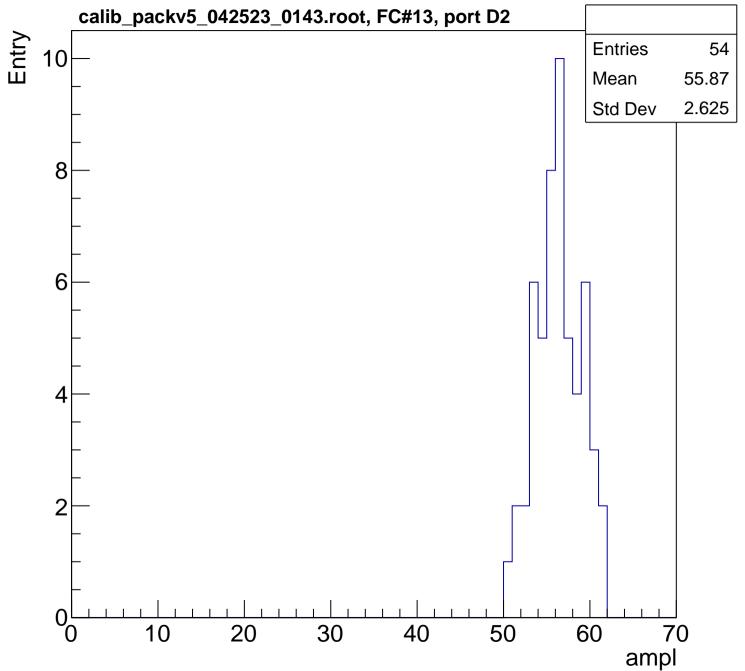


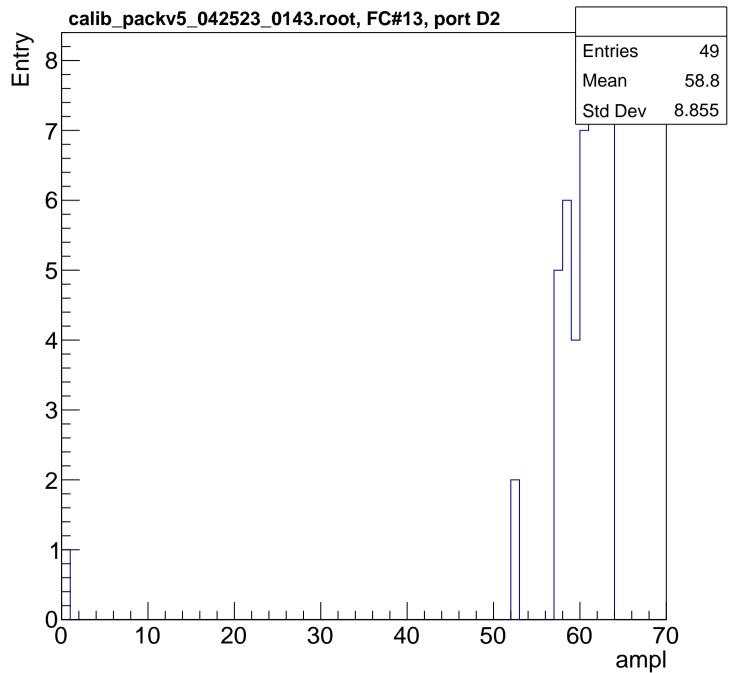


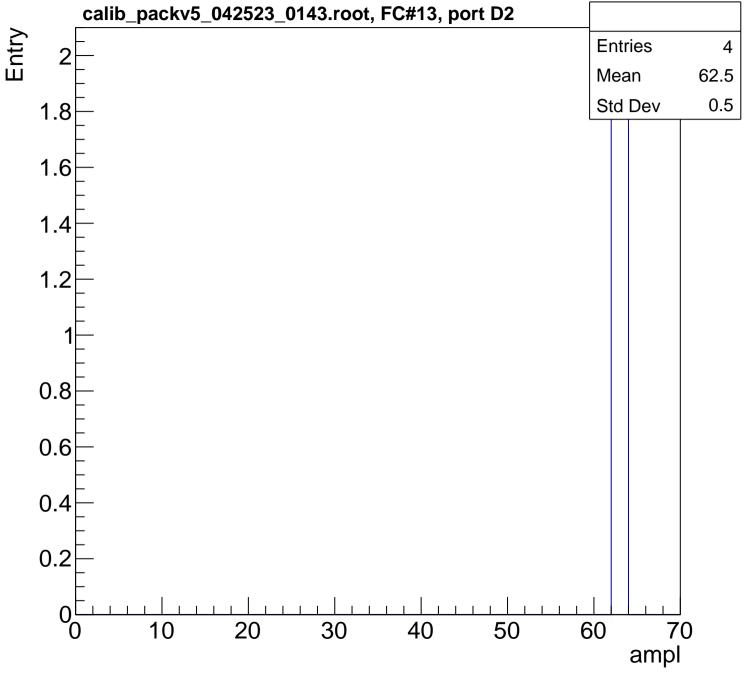




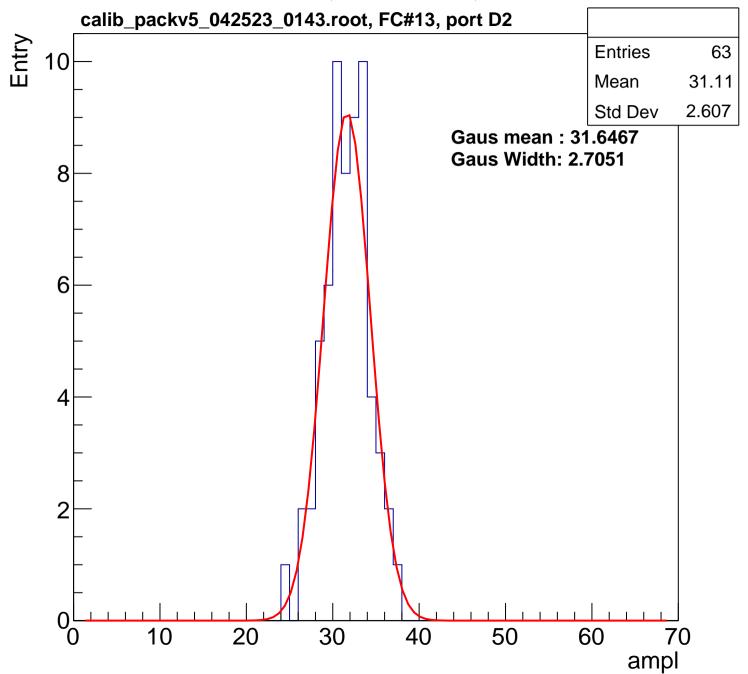


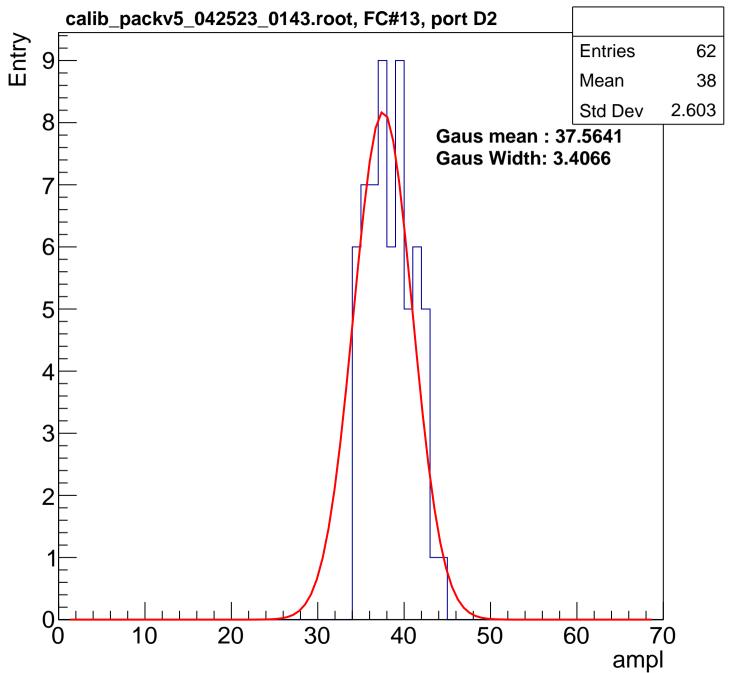


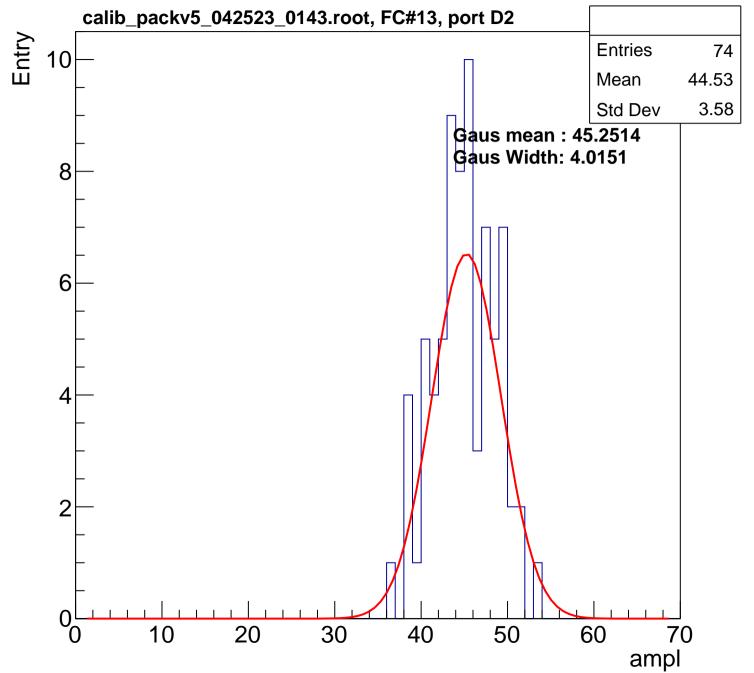


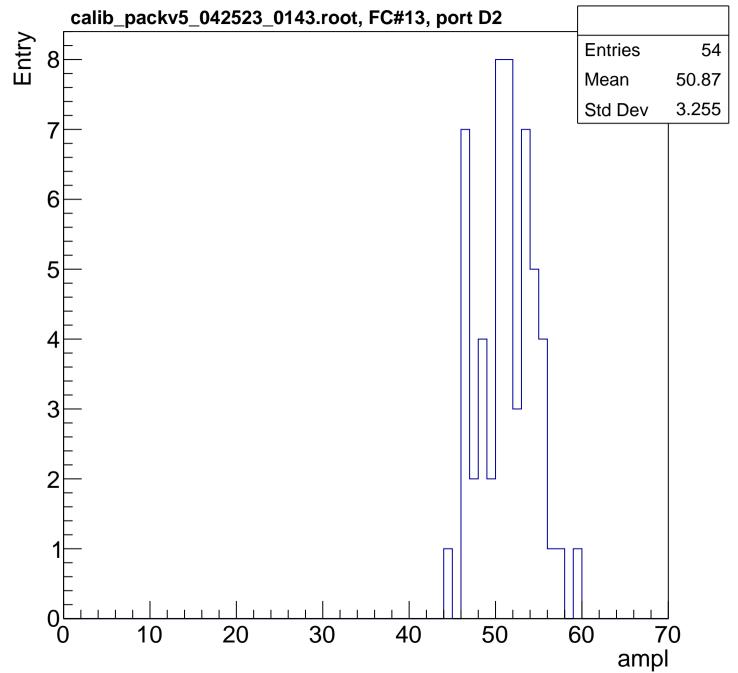


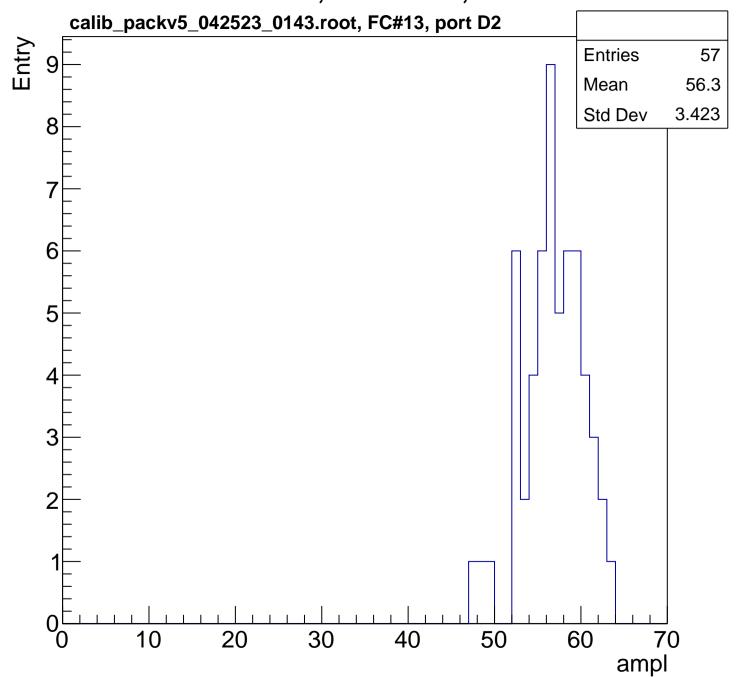
B1L003S, U8-ch16, adc7 calib\_packv5\_042523\_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

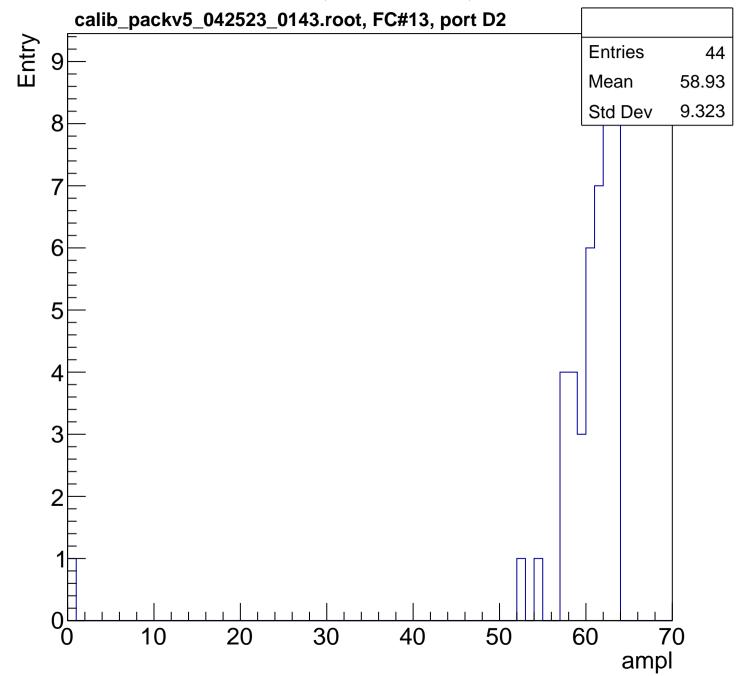


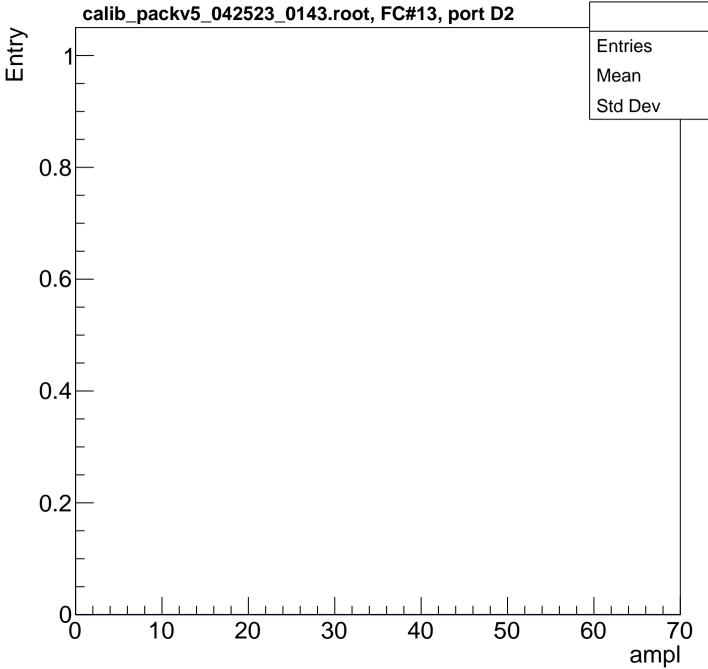




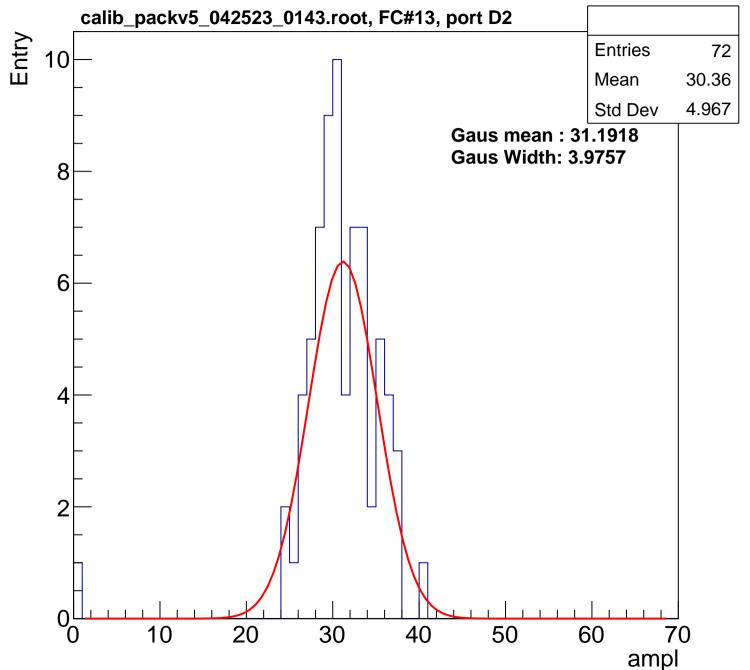


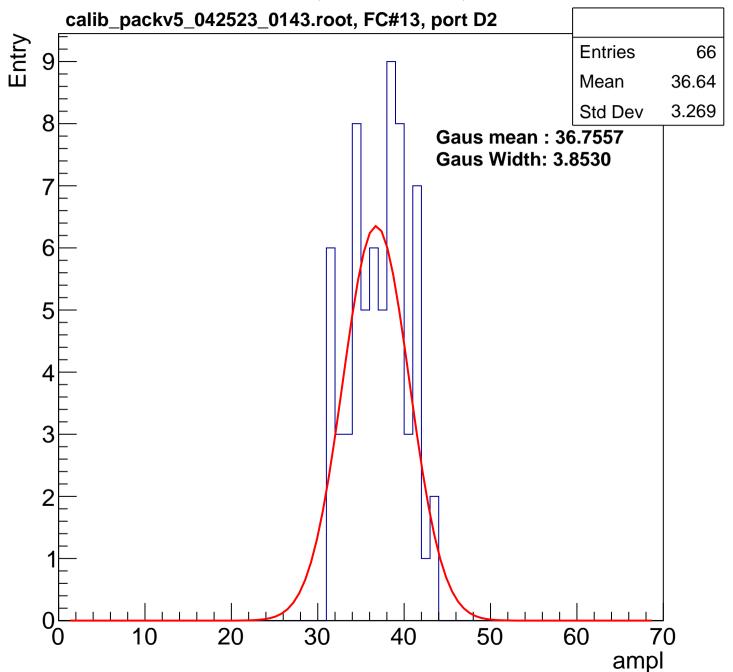


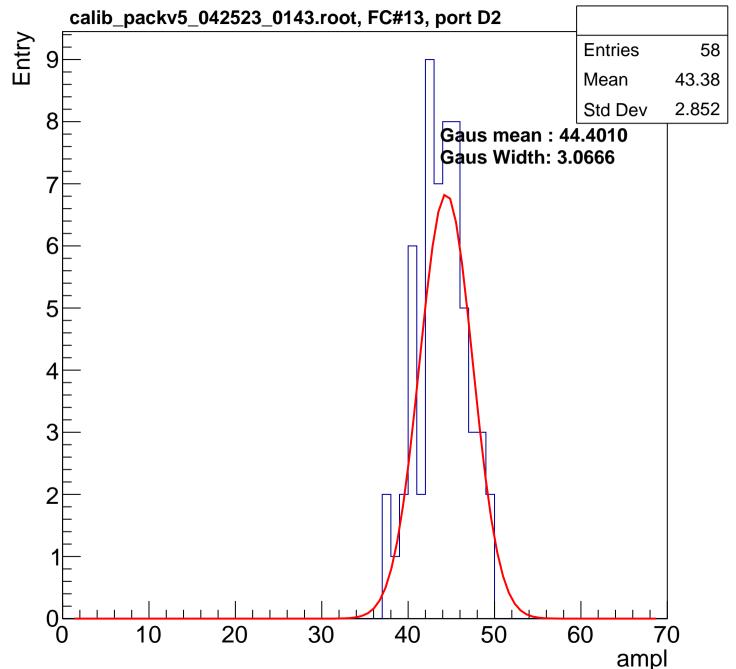


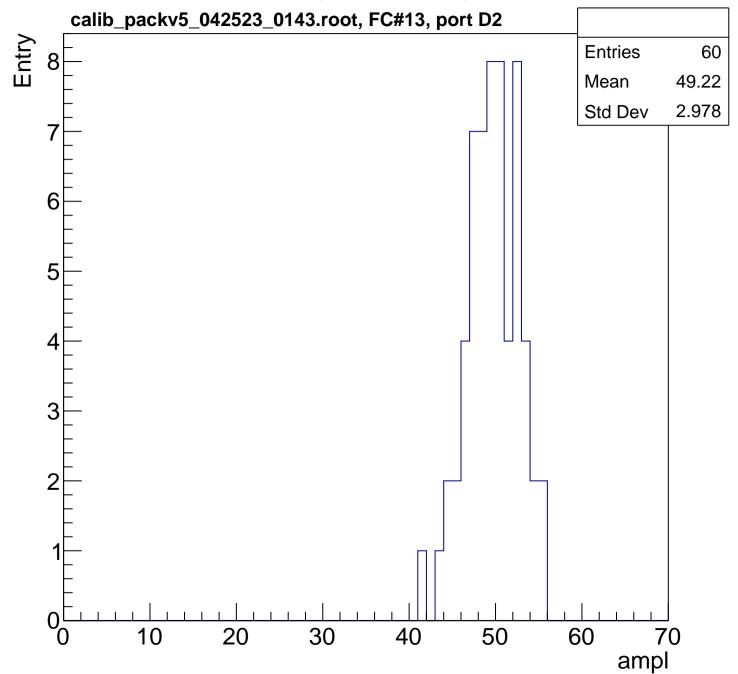


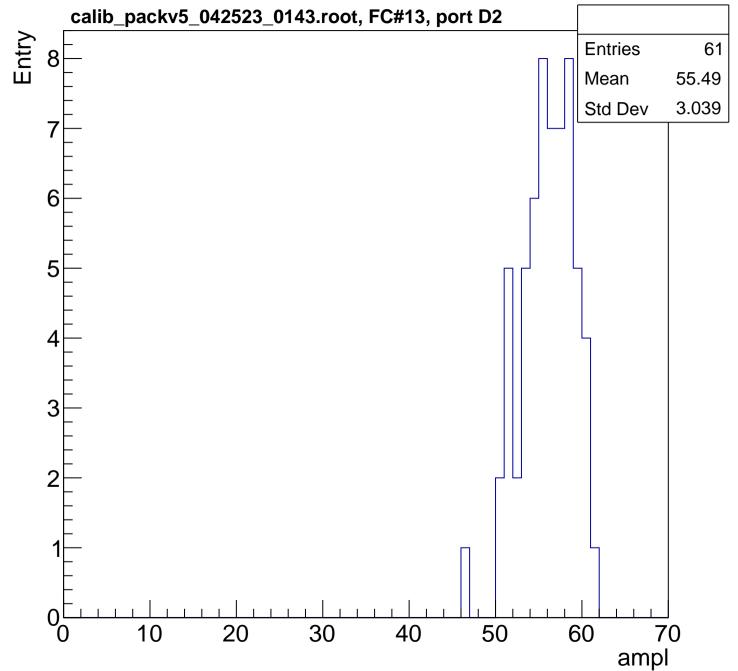


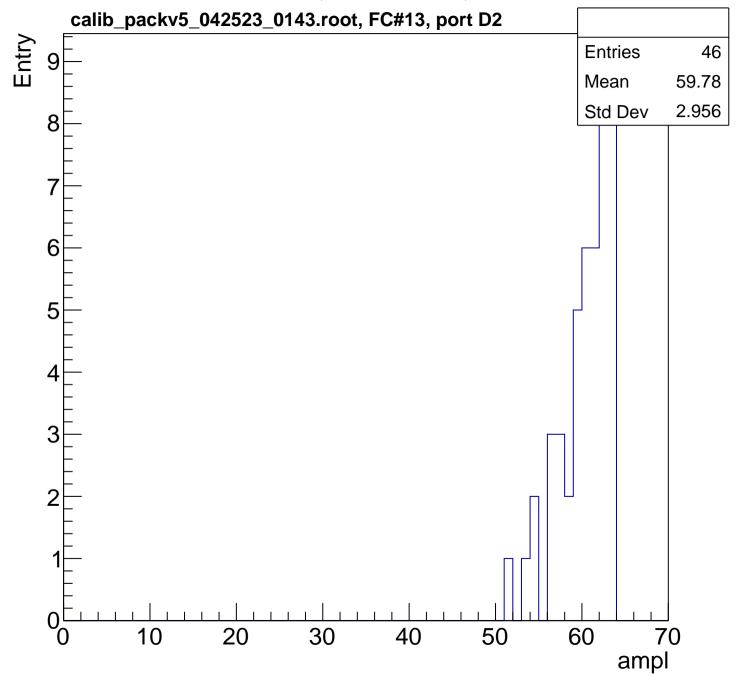


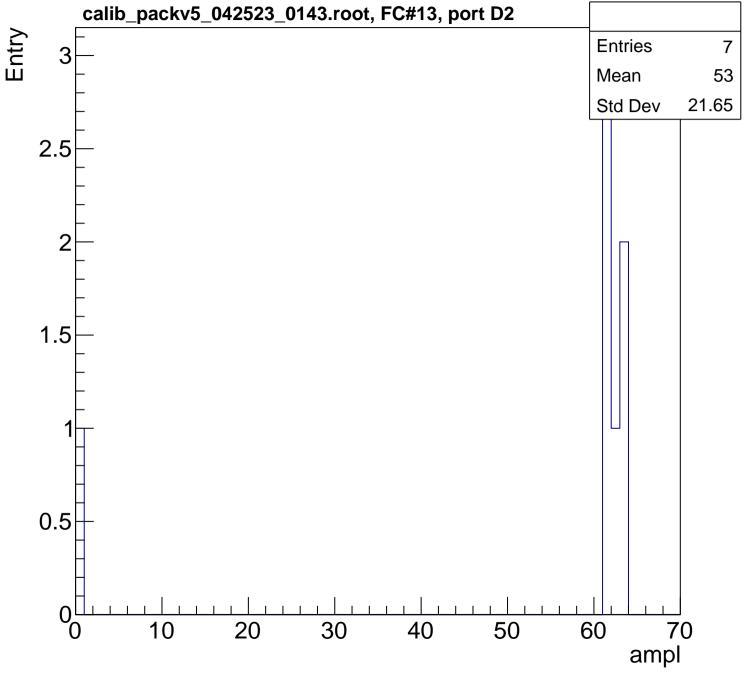




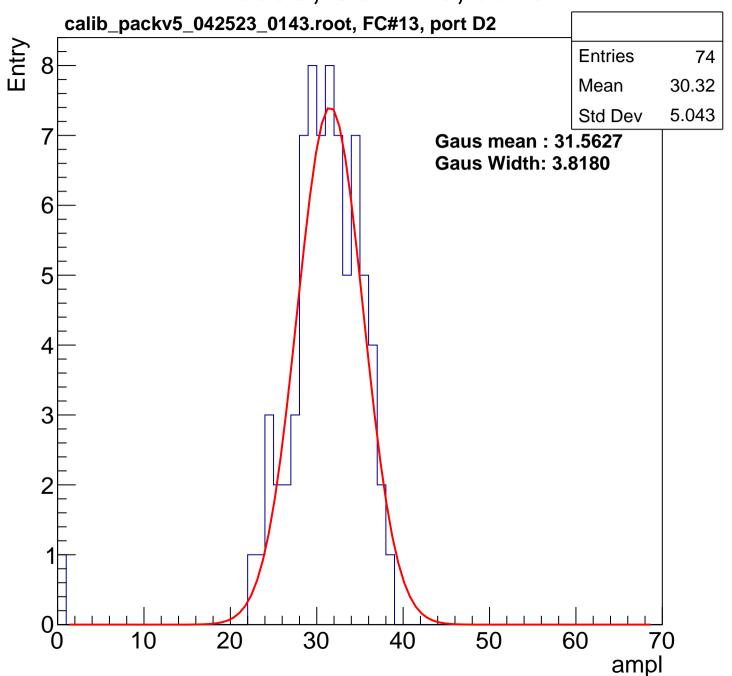


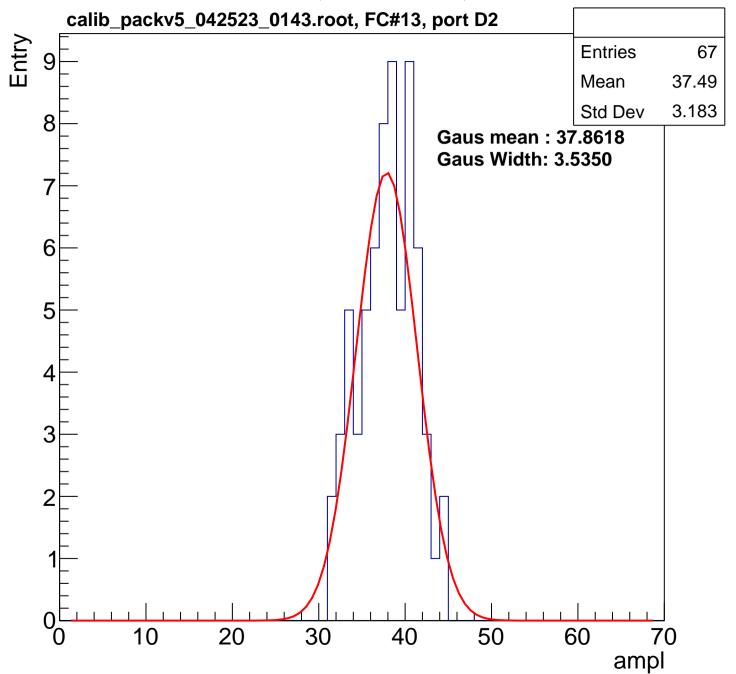


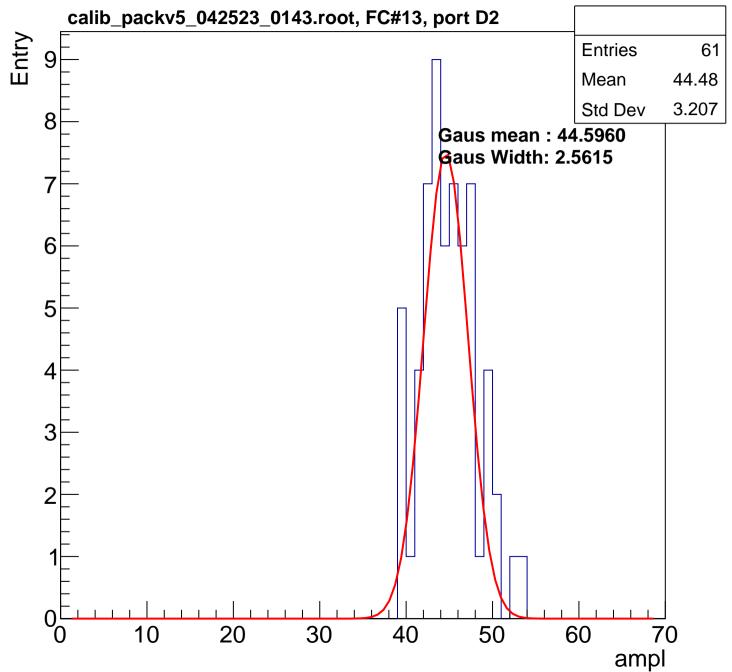


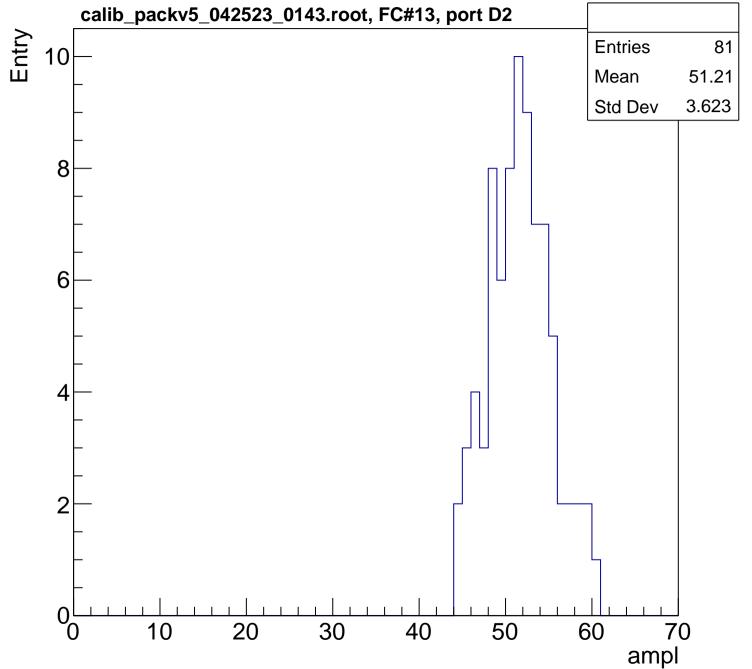


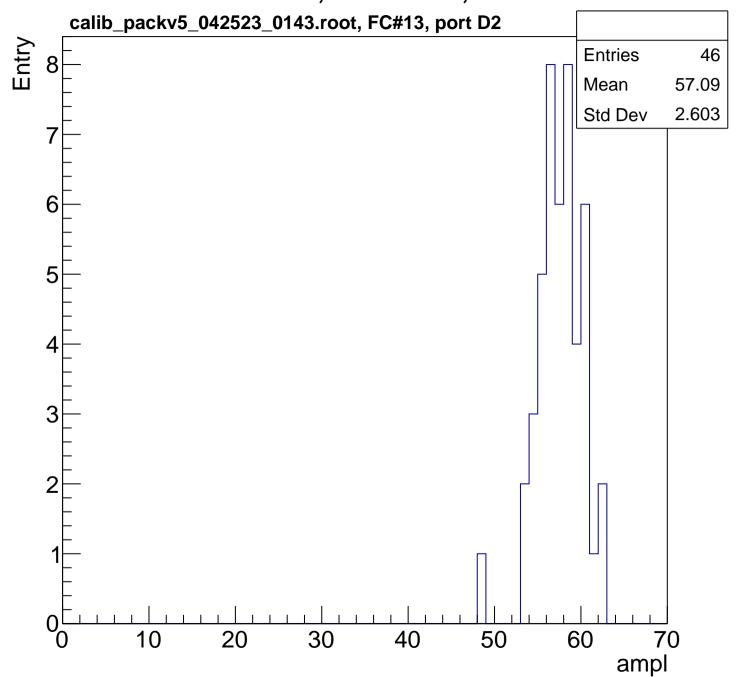
B1L003S, U8-ch18, adc7 calib\_packv5\_042523\_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

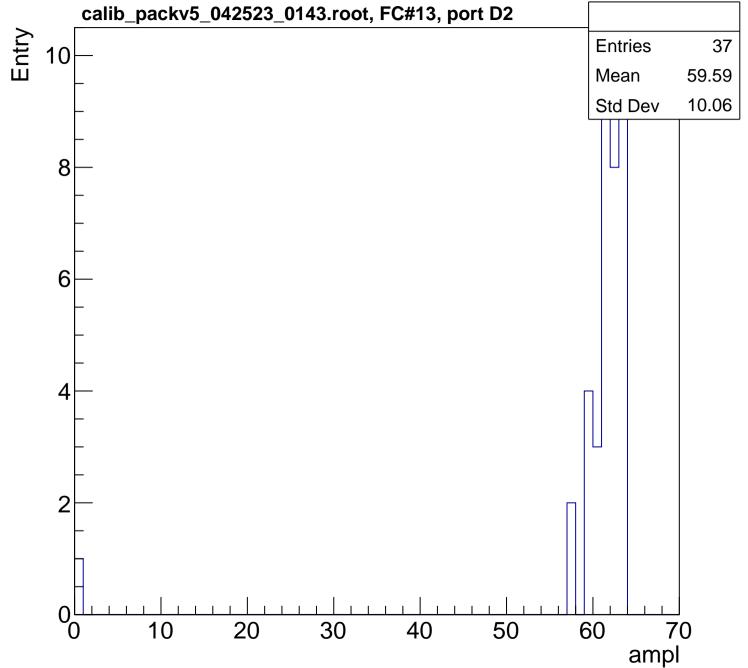


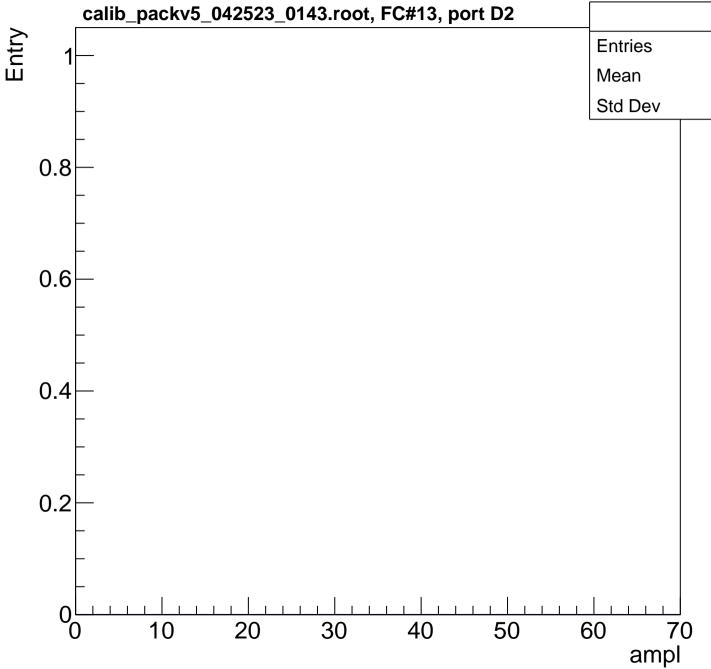




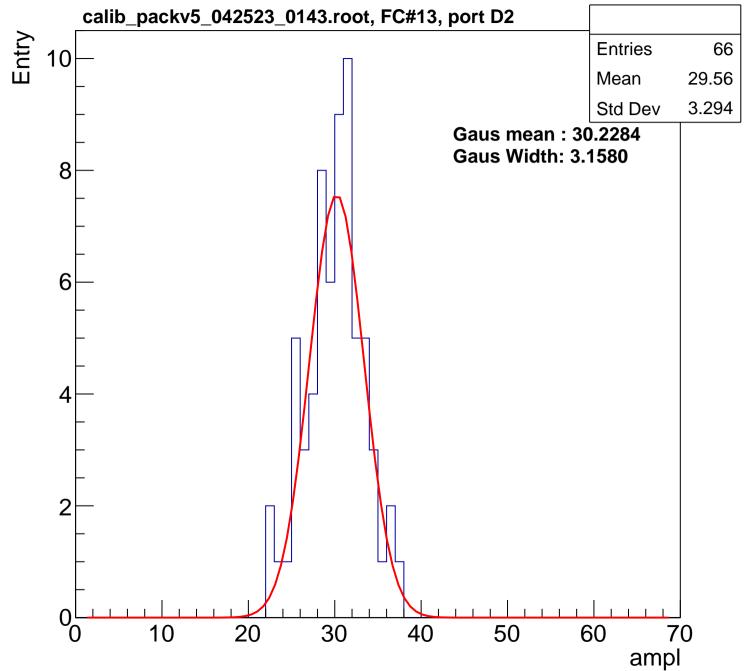


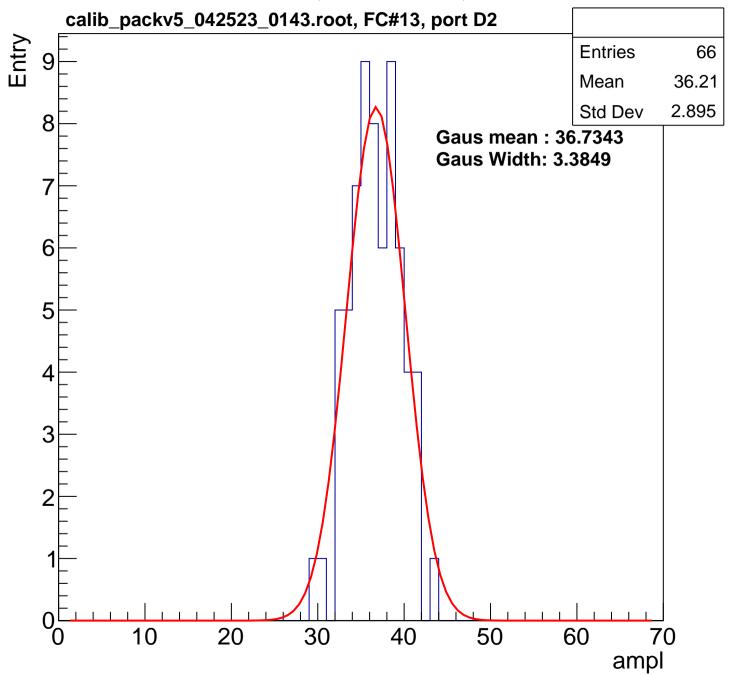


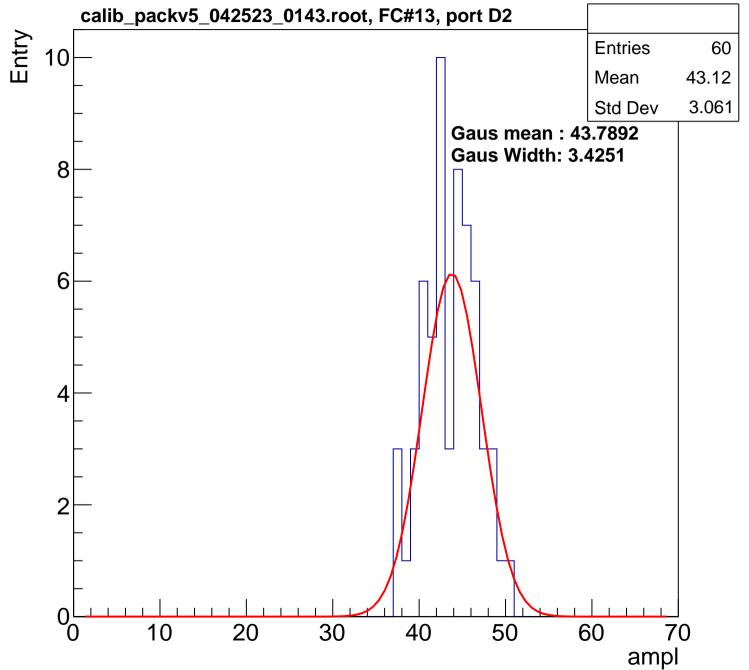


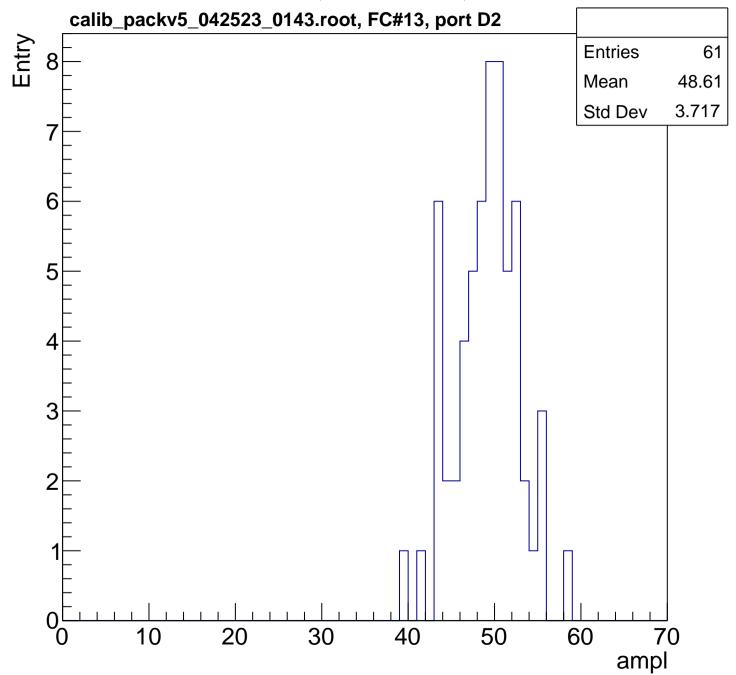


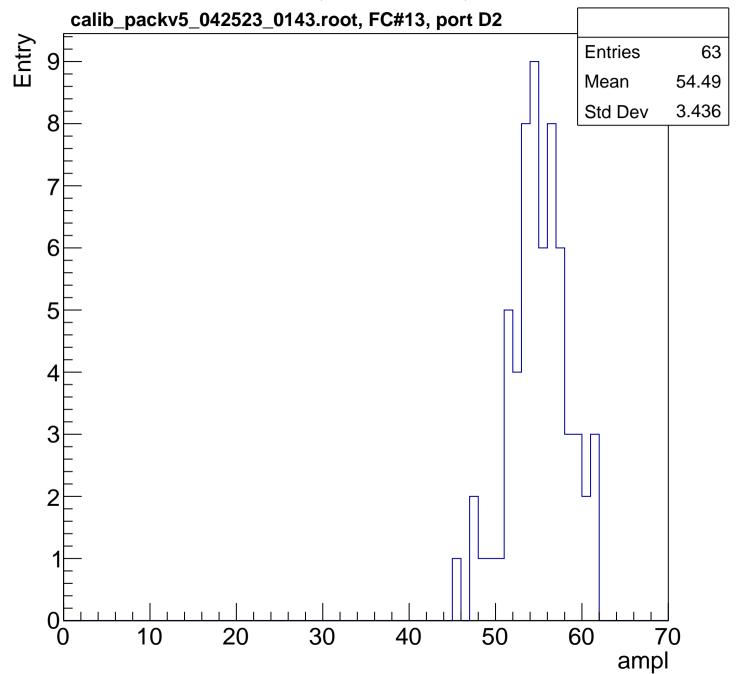


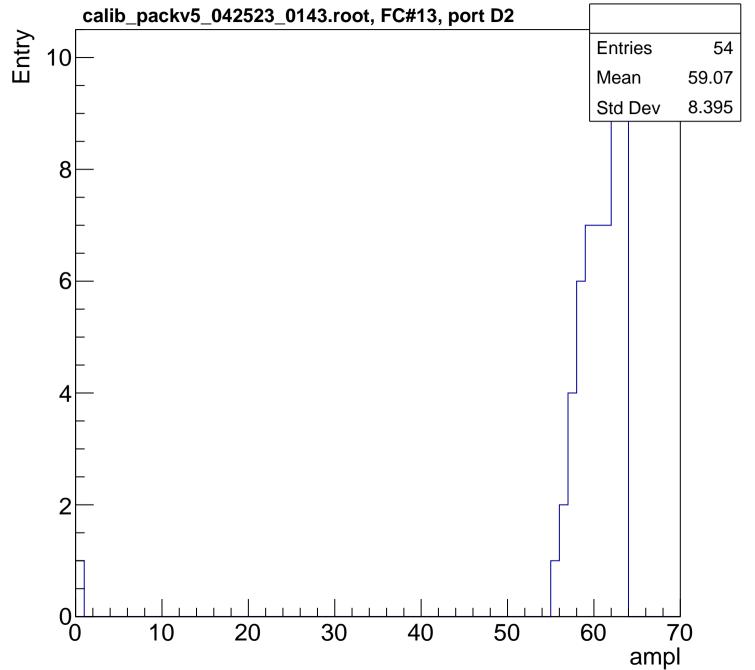


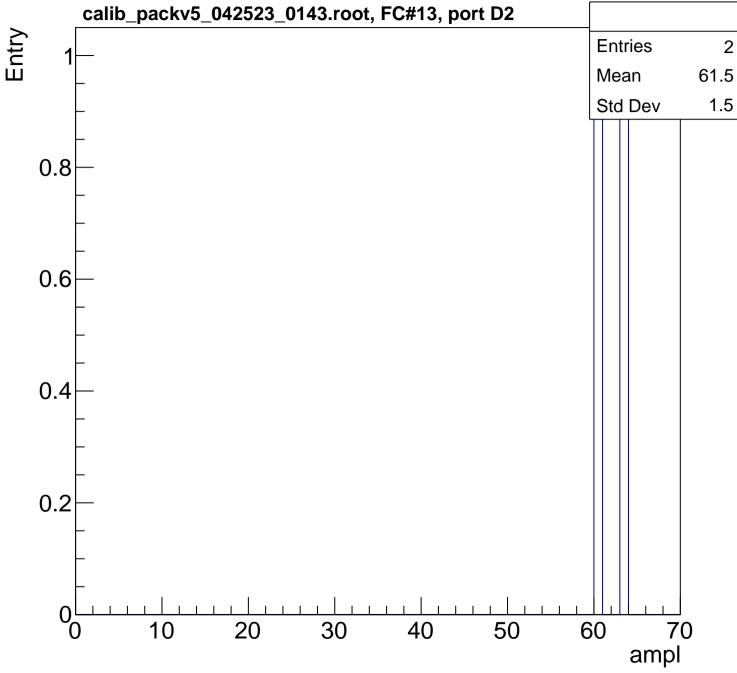




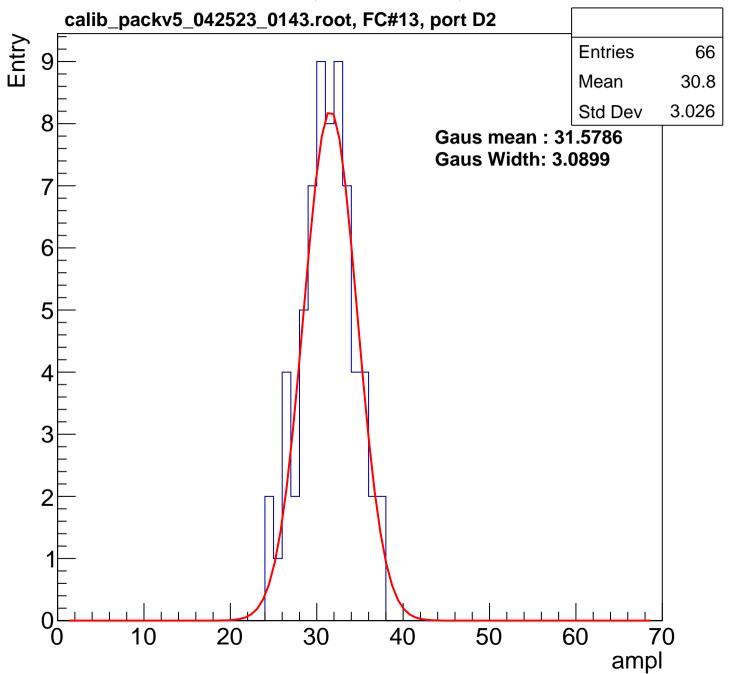


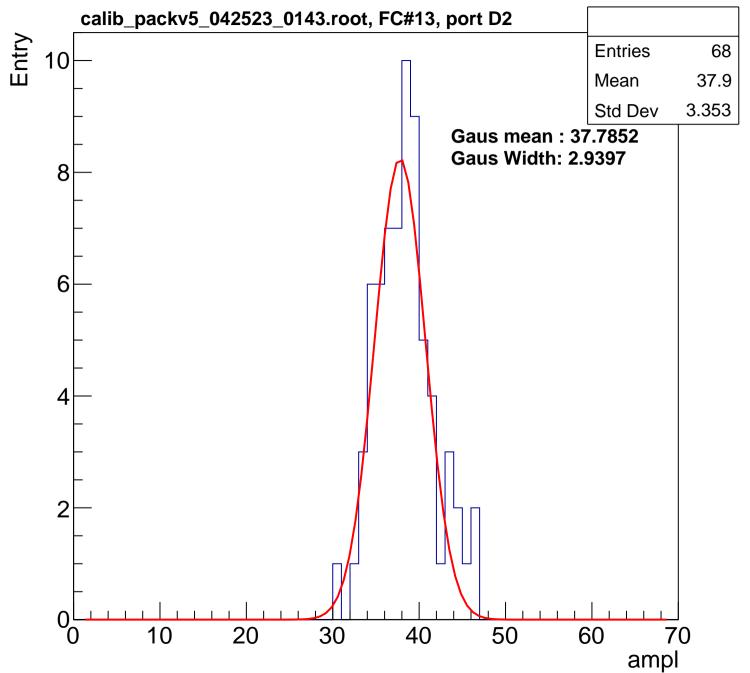


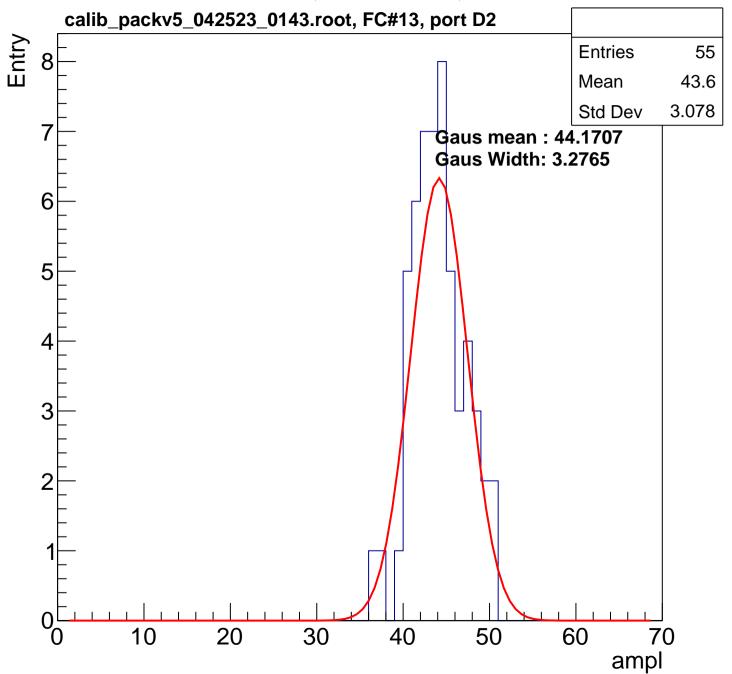


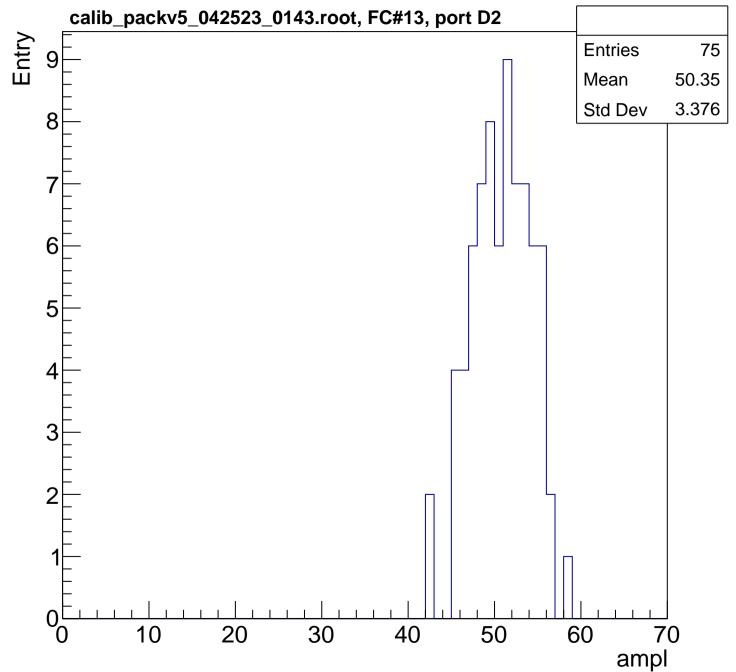


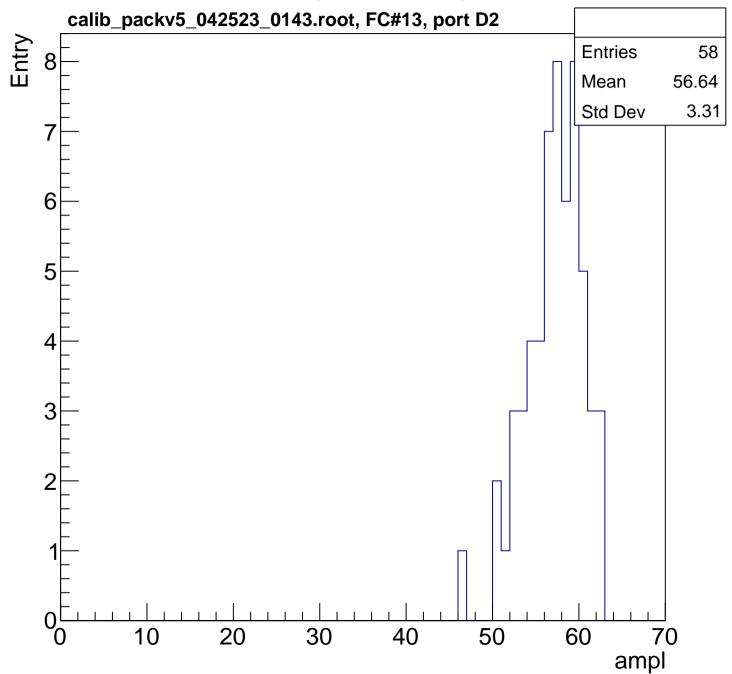
B1L003S, U8-ch20, adc7 calib\_packv5\_042523\_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

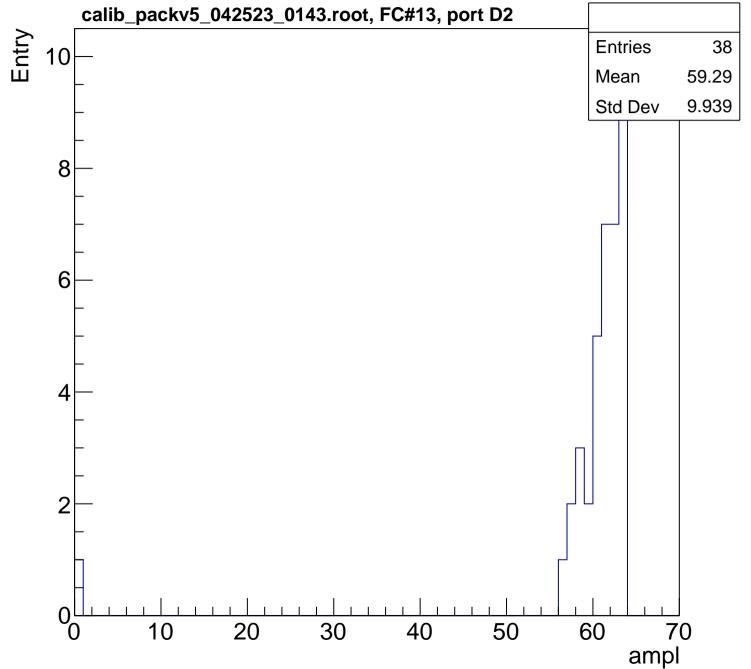




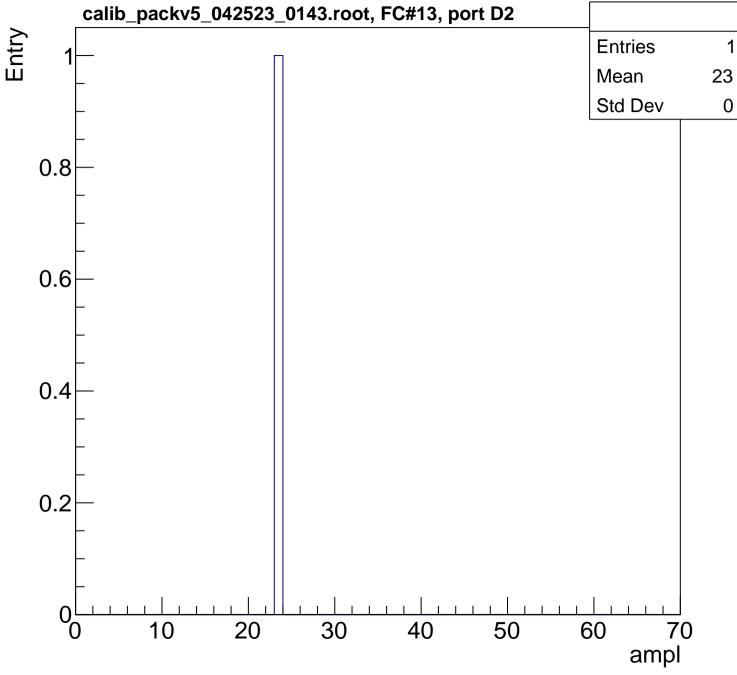


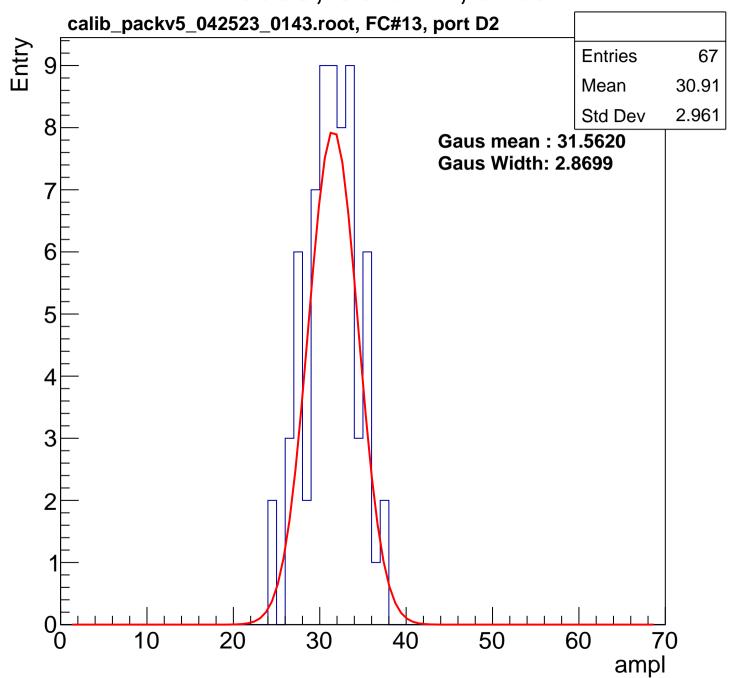


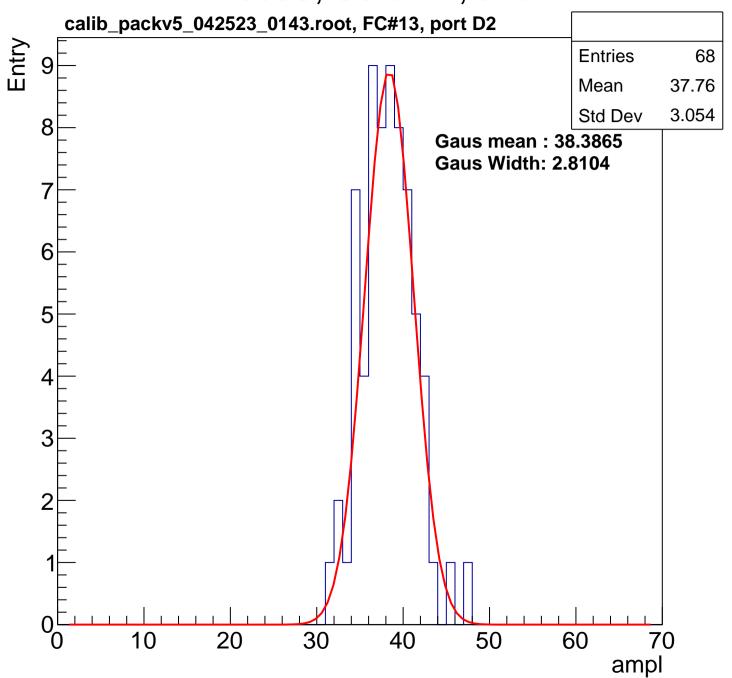


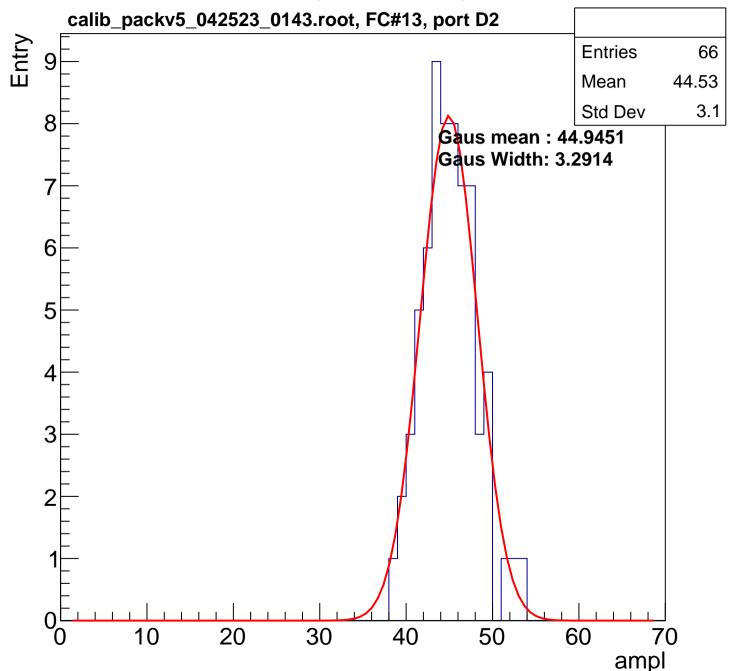


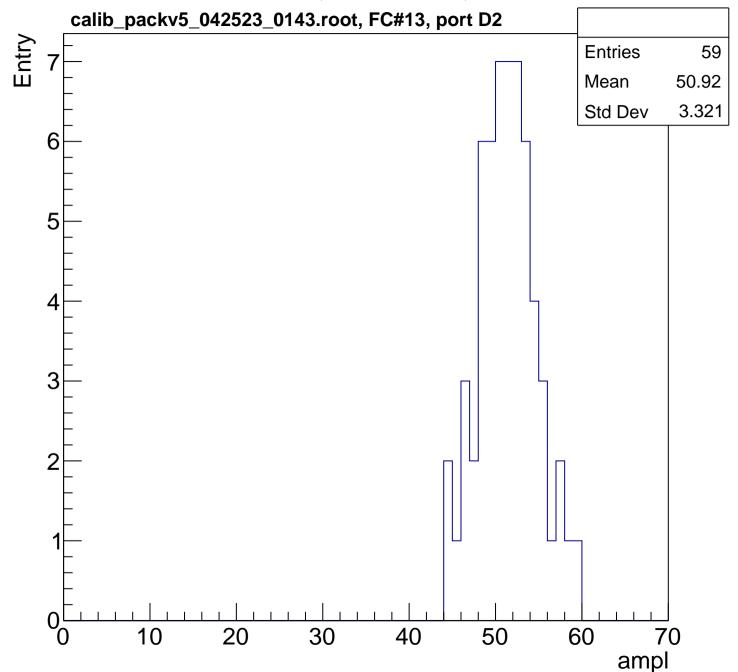


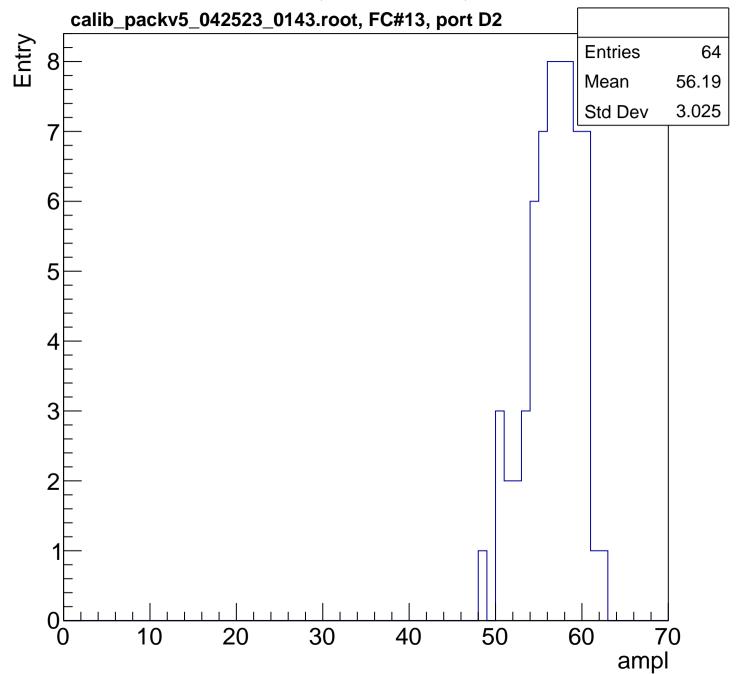


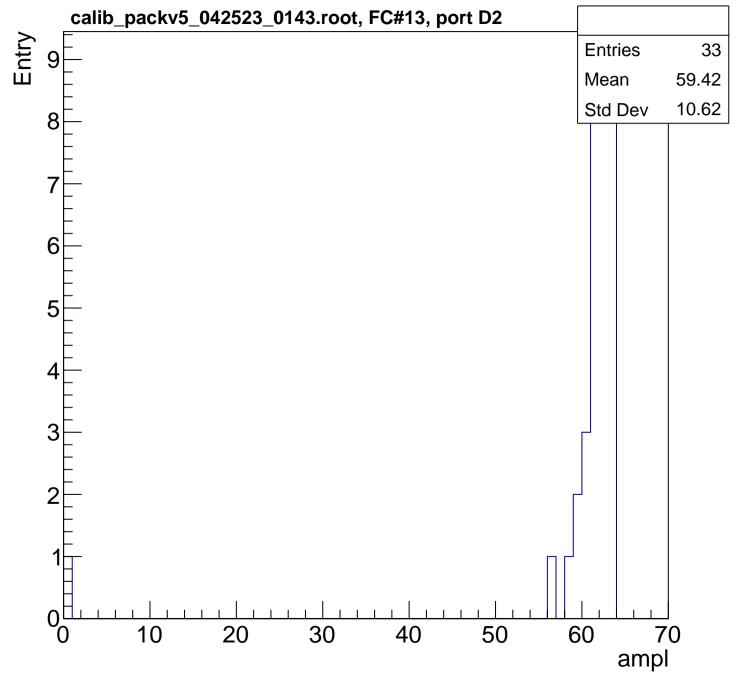


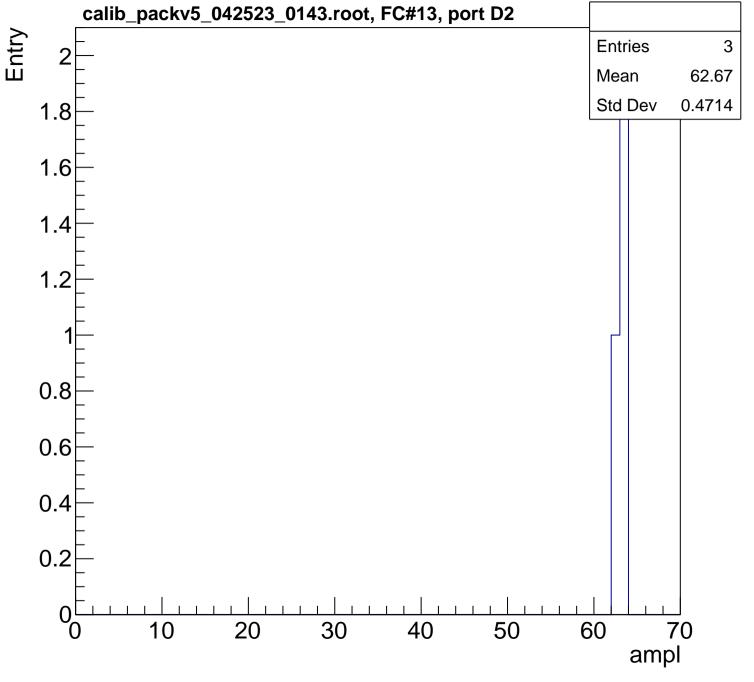




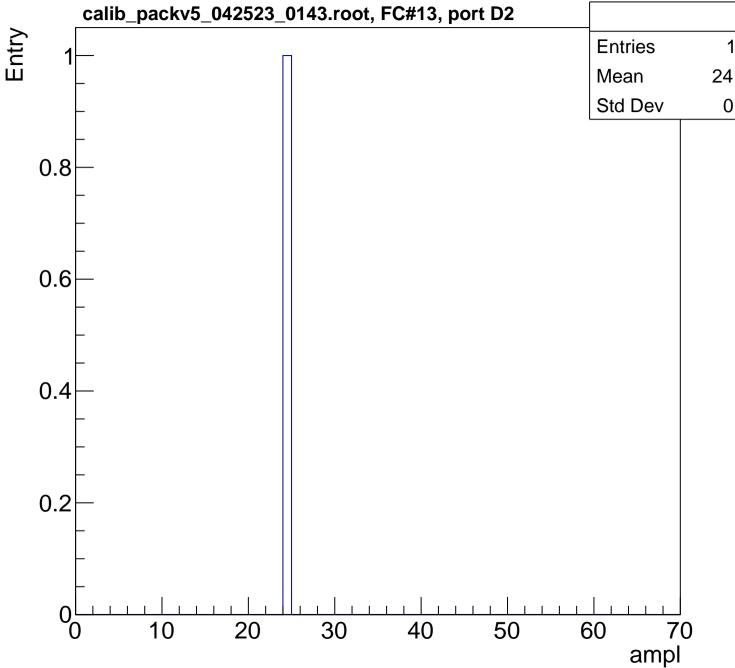


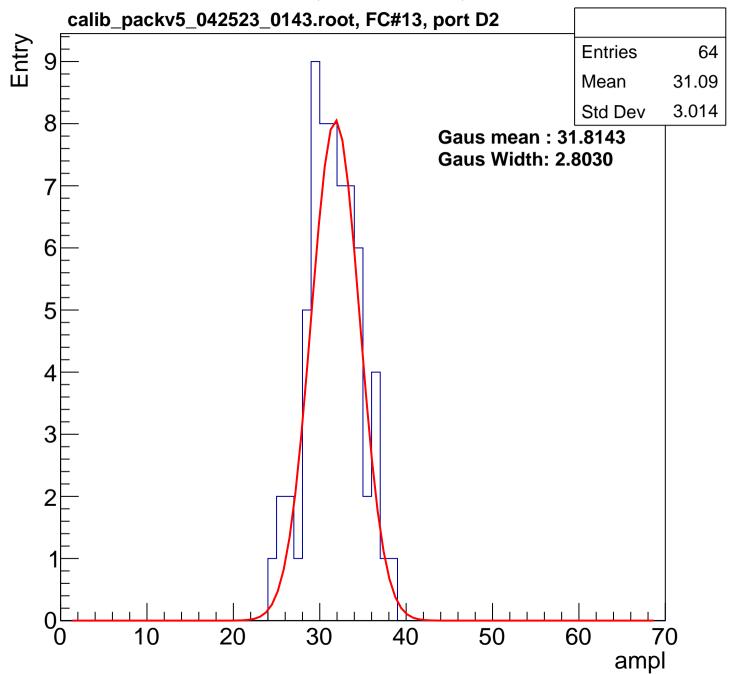


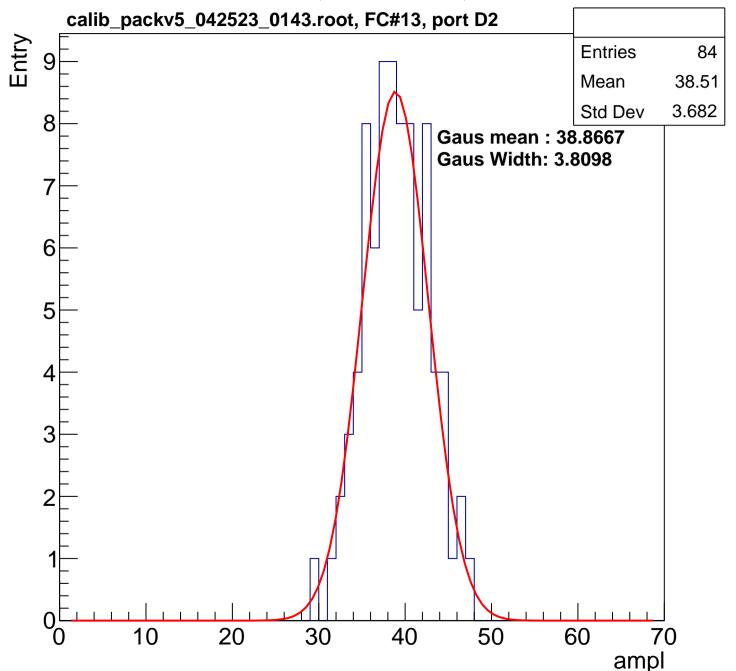


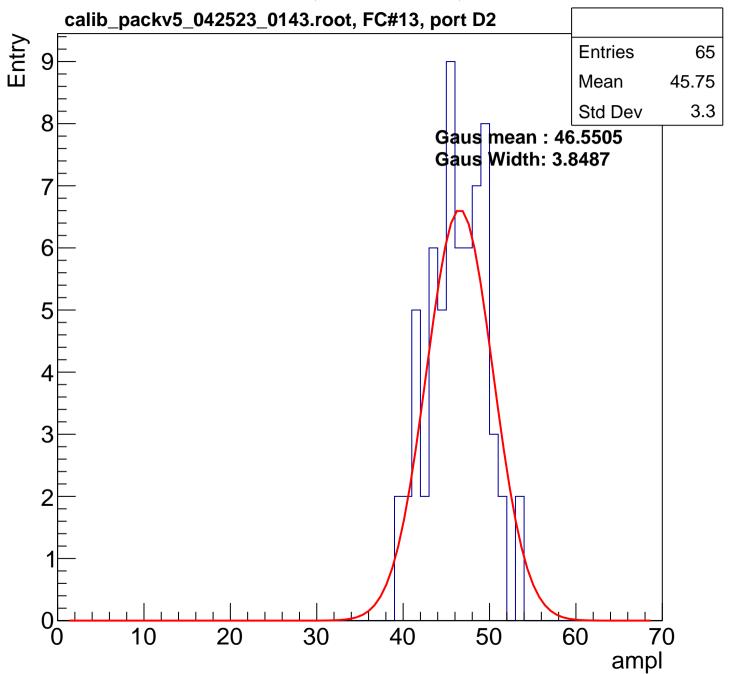


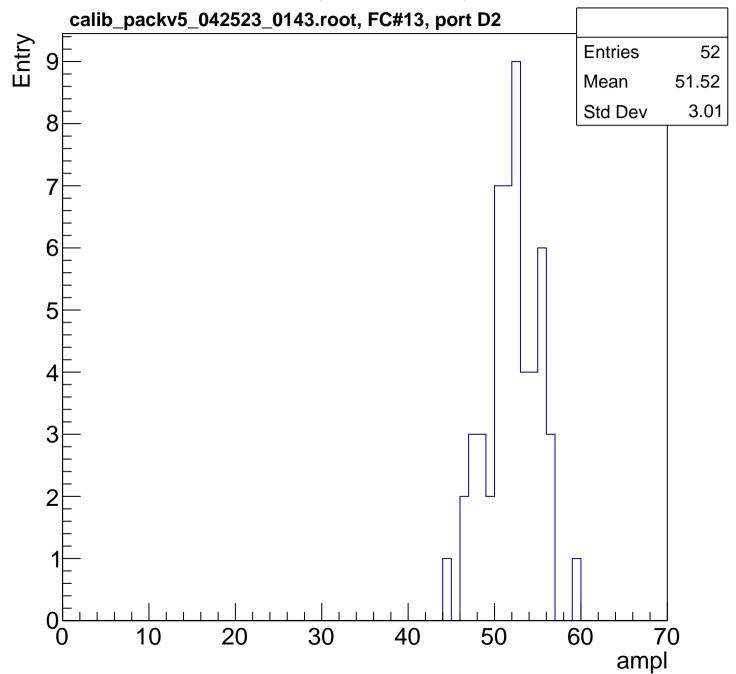
0

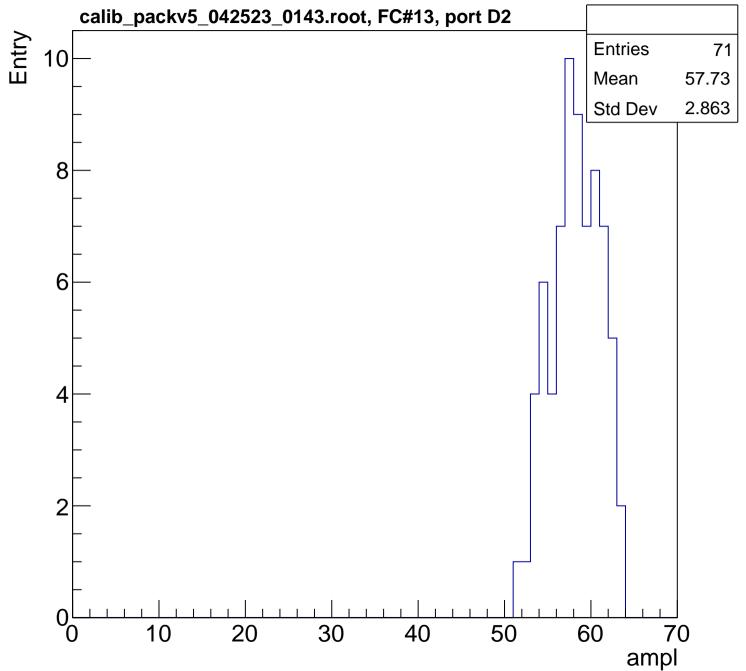


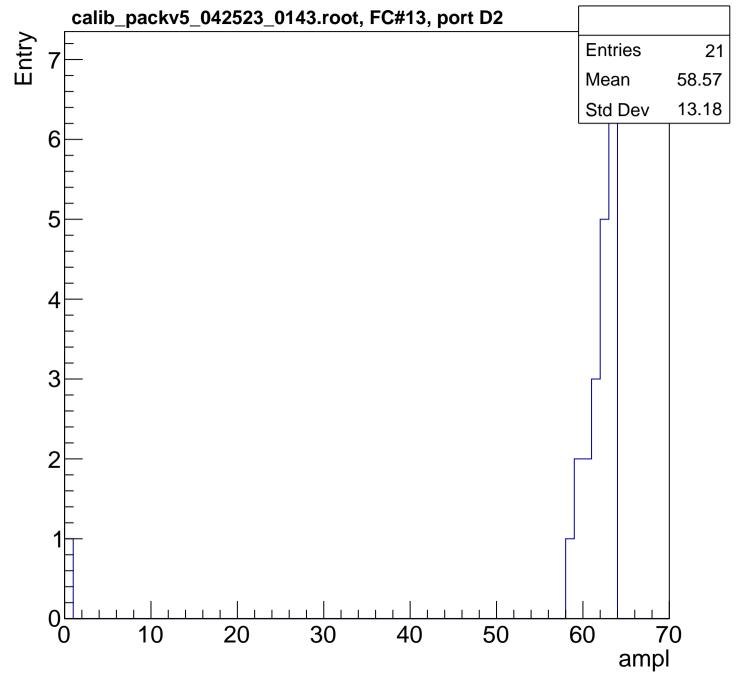


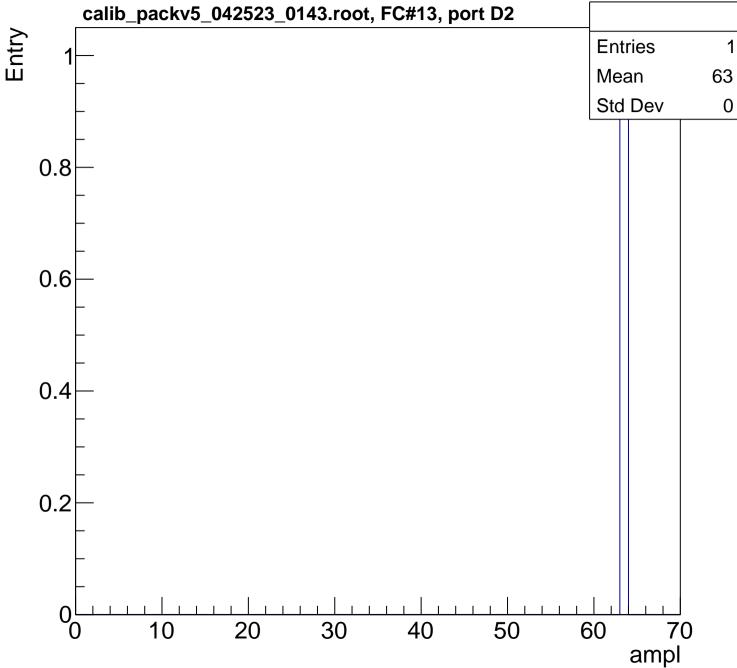




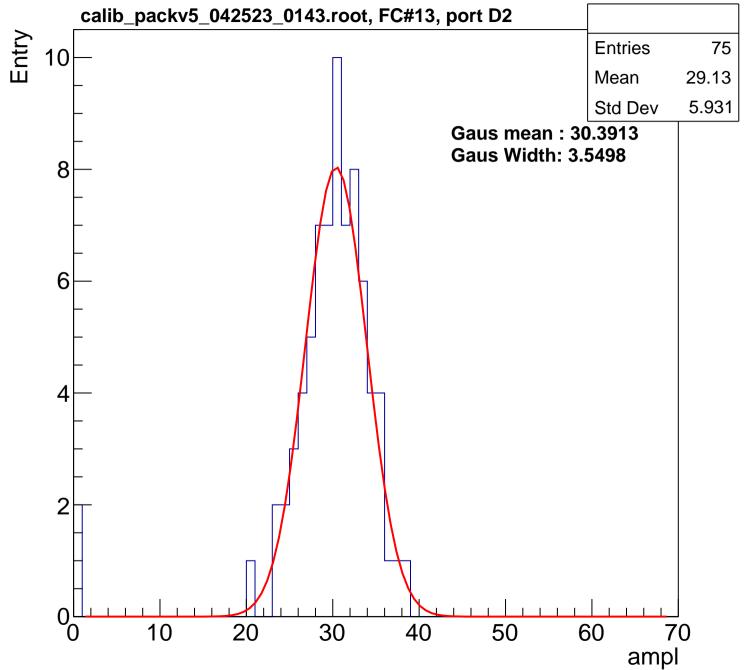


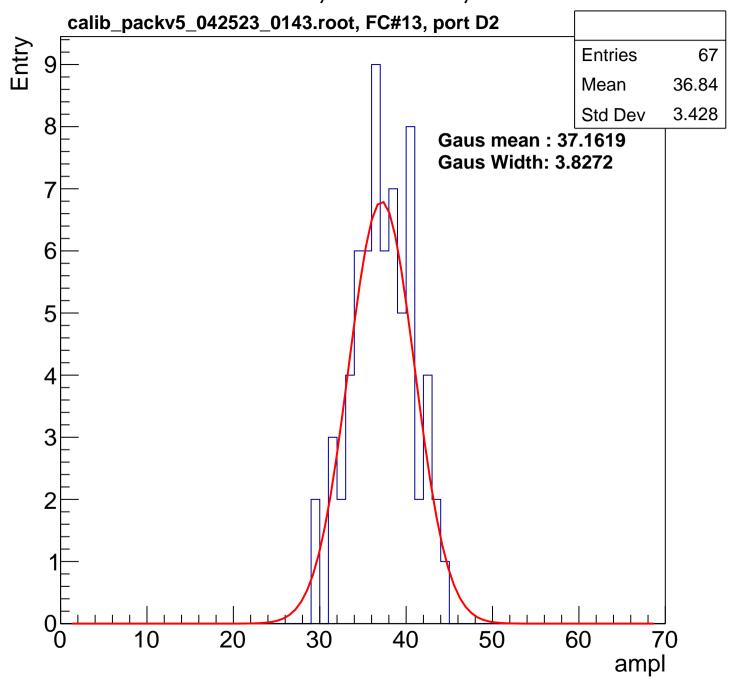


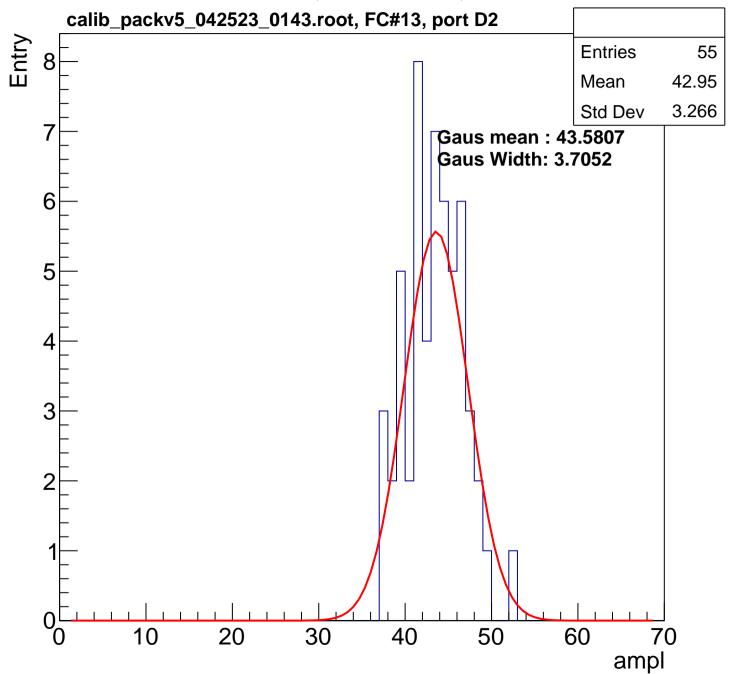


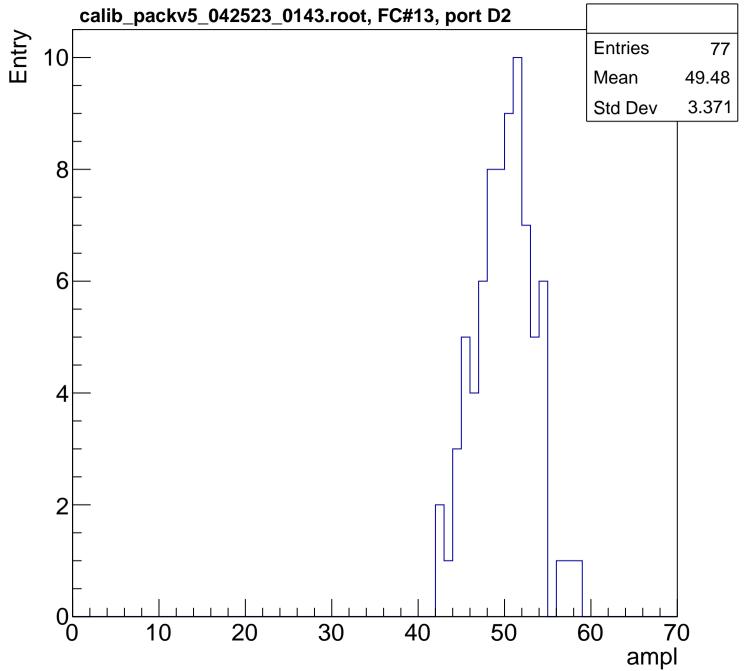


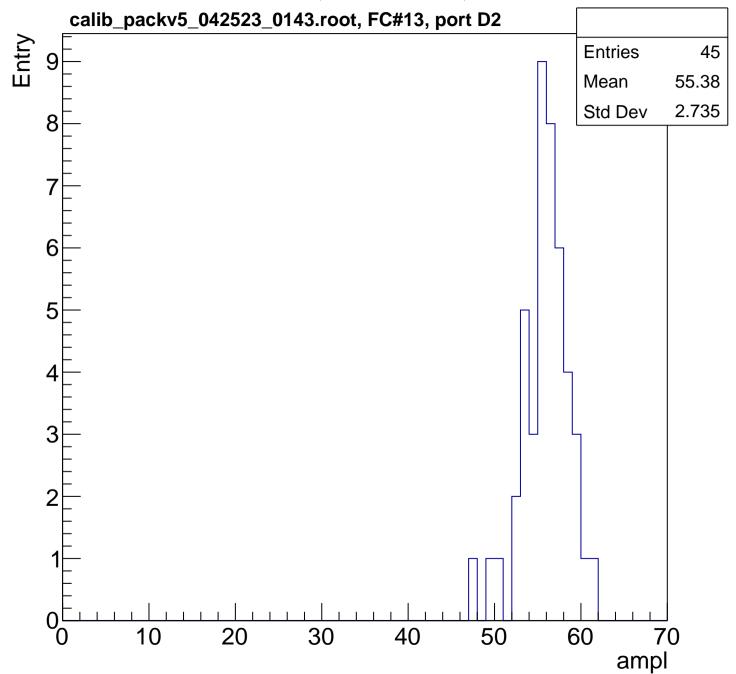


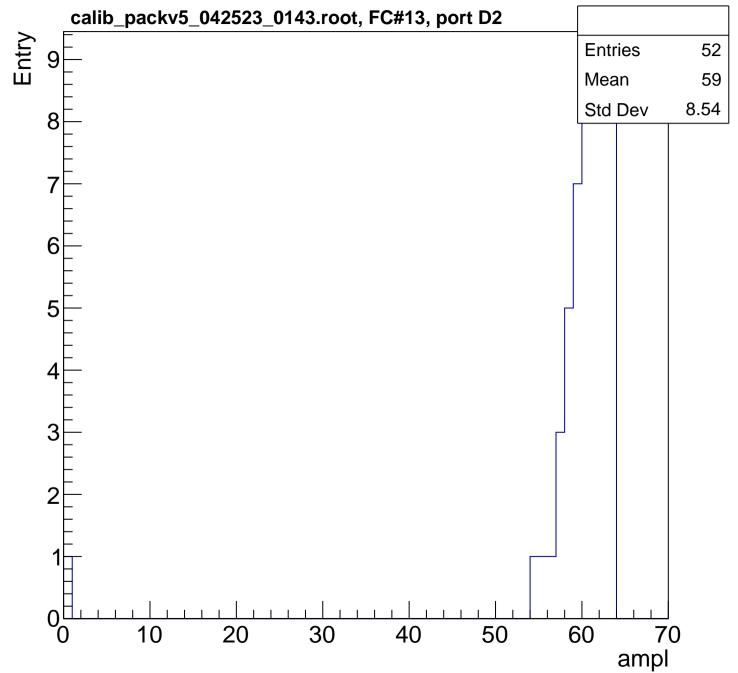


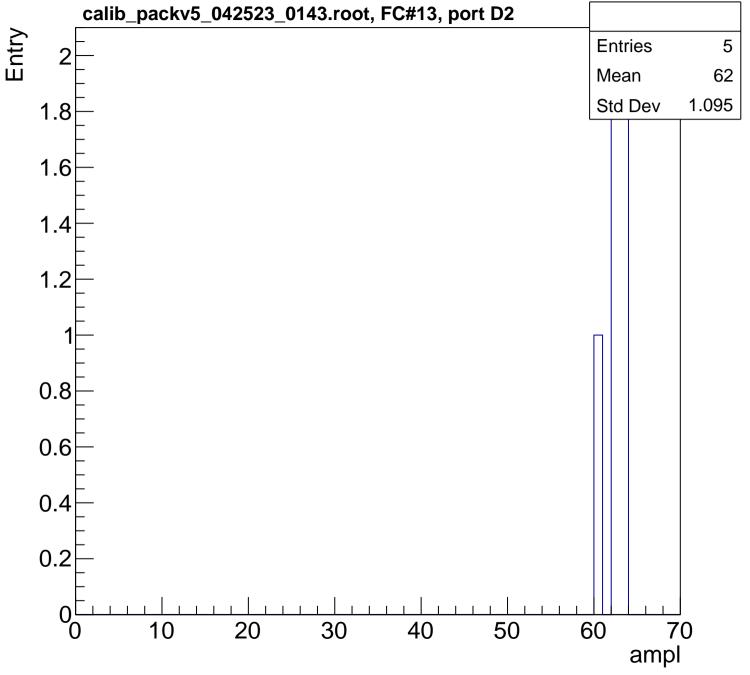




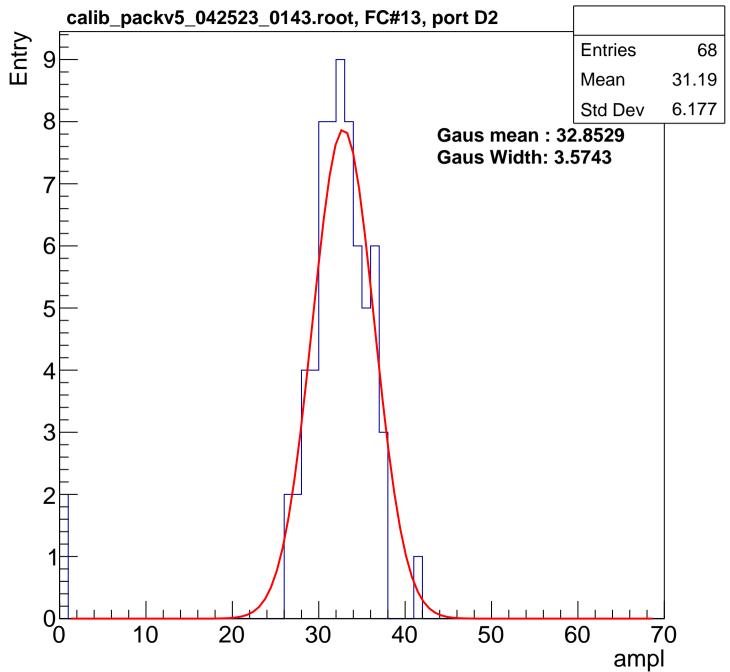


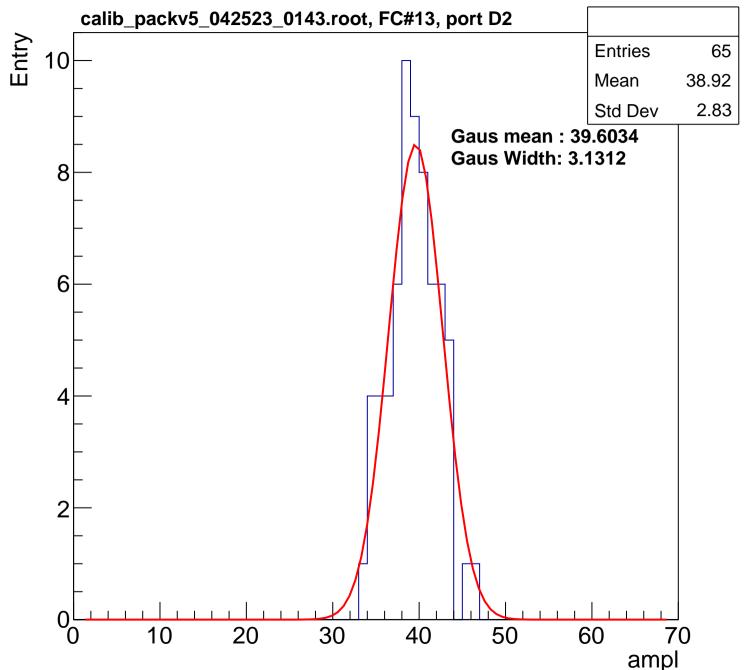


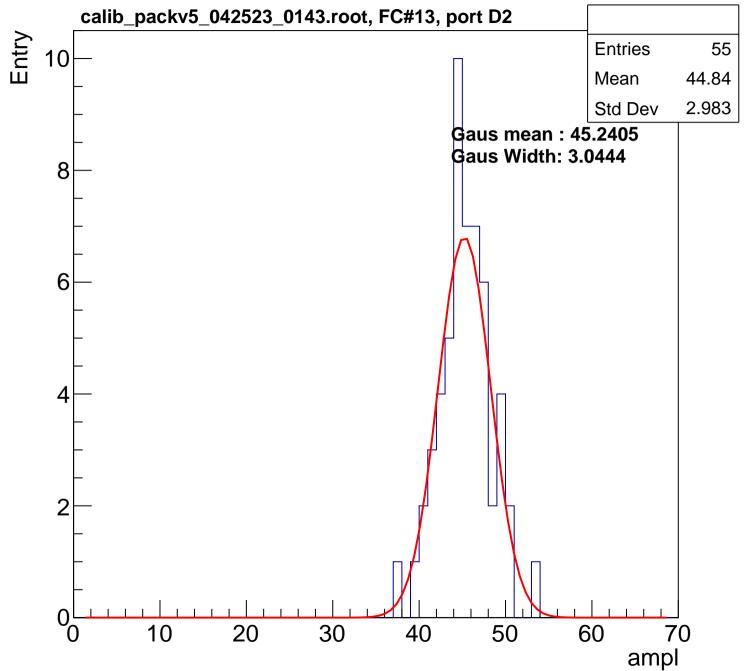


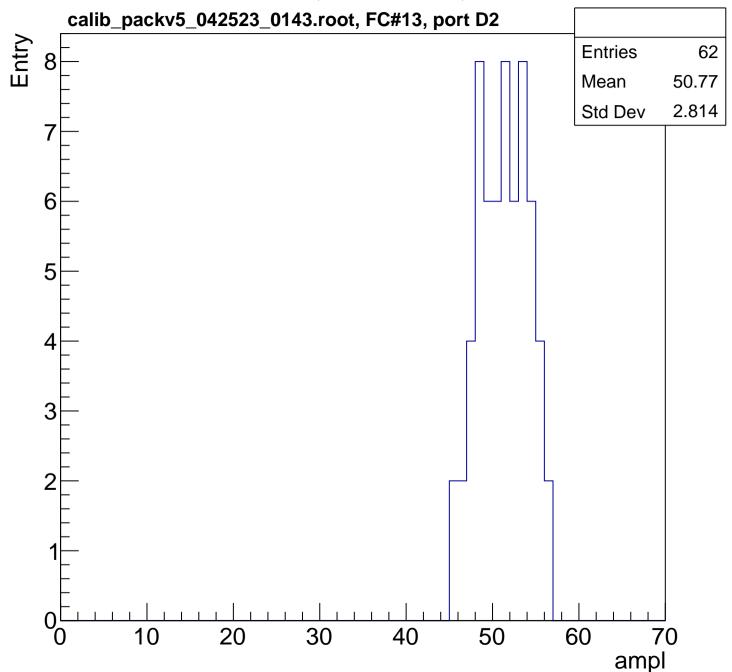


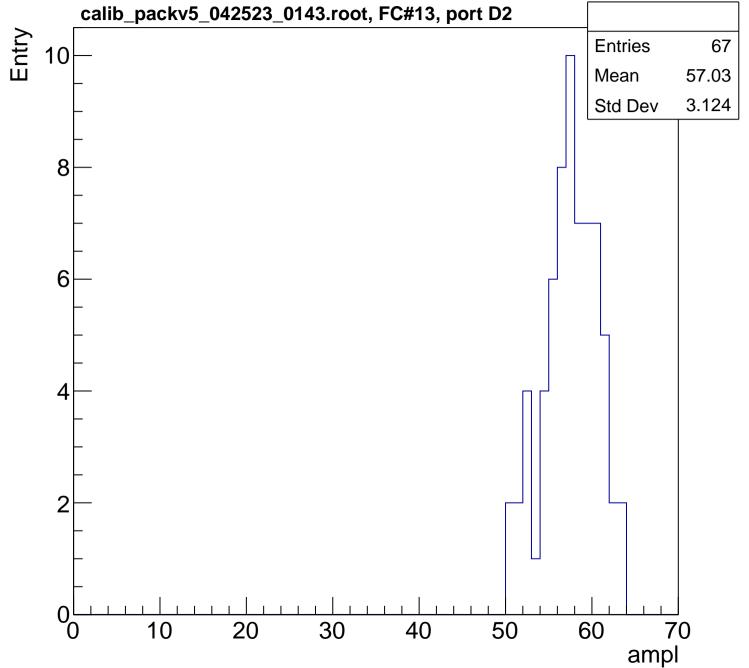
B1L003S, U8-ch24, adc7 calib\_packv5\_042523\_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

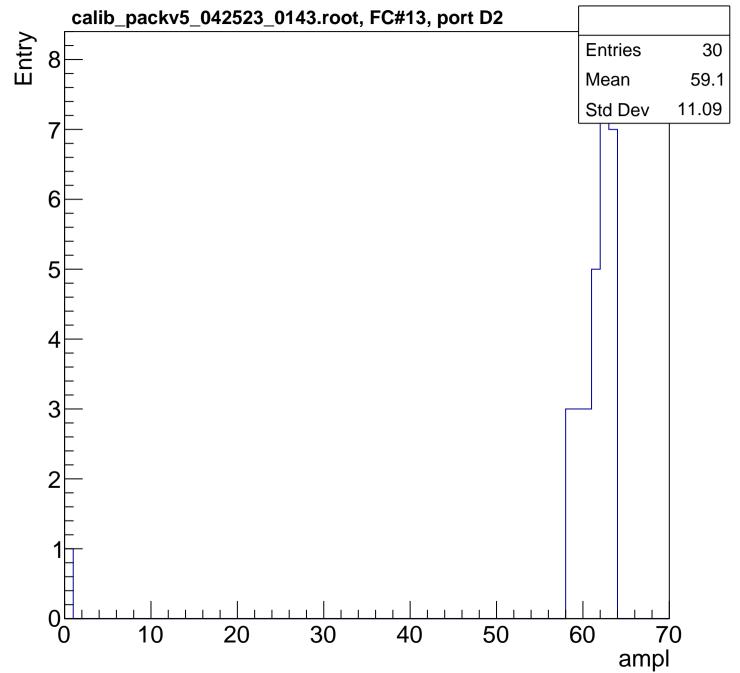


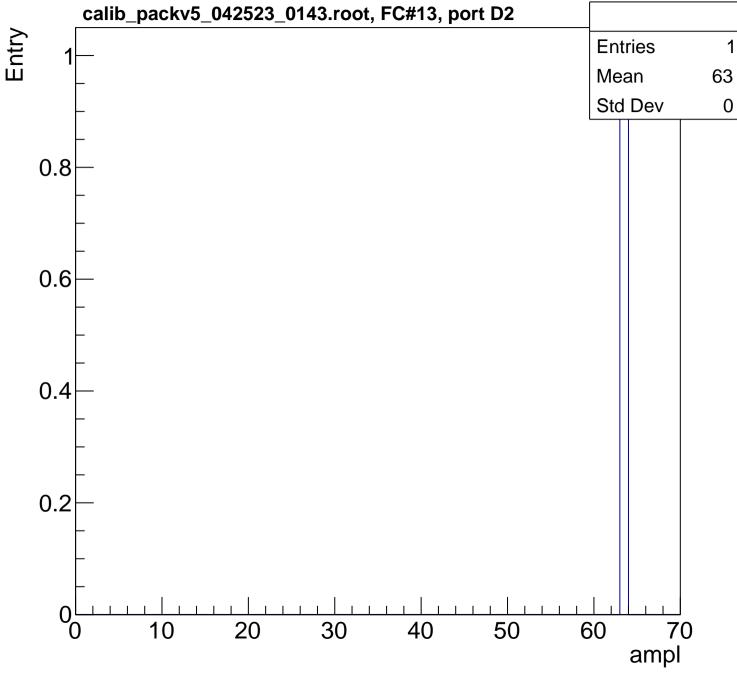


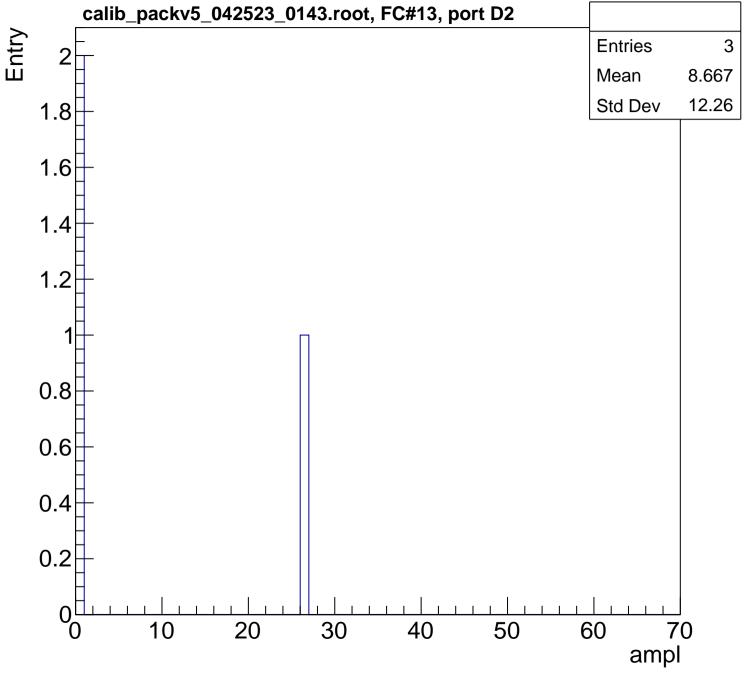


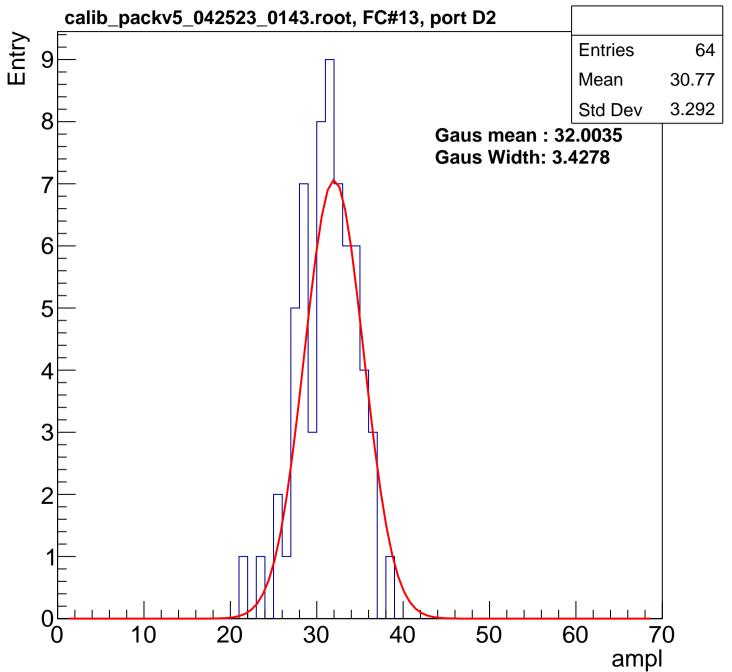


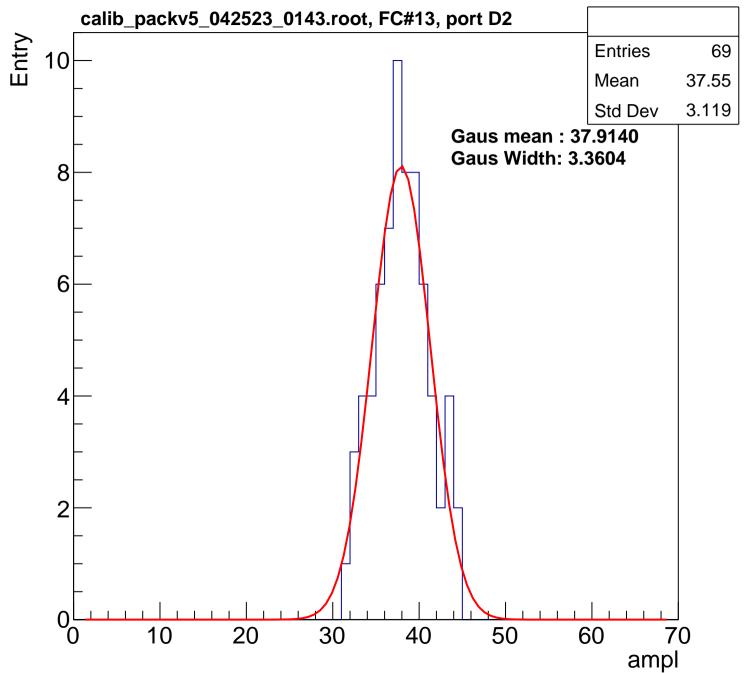


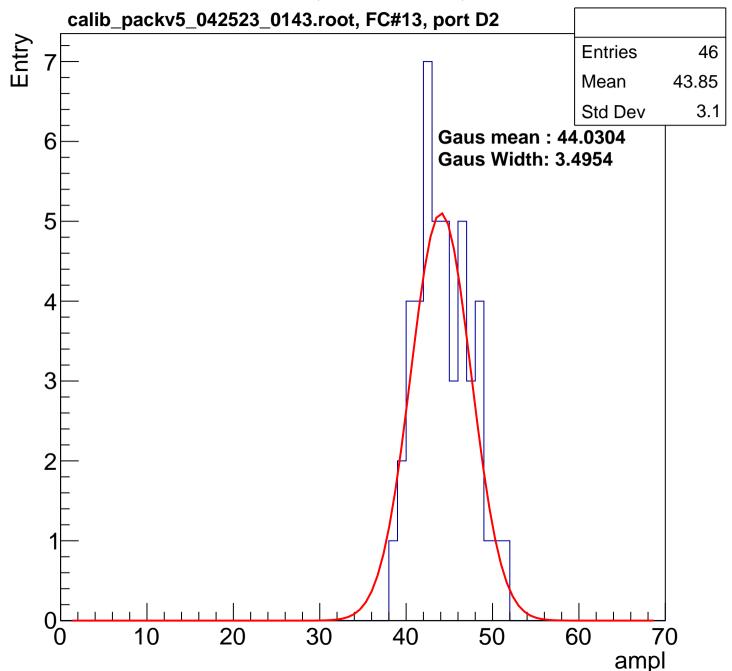


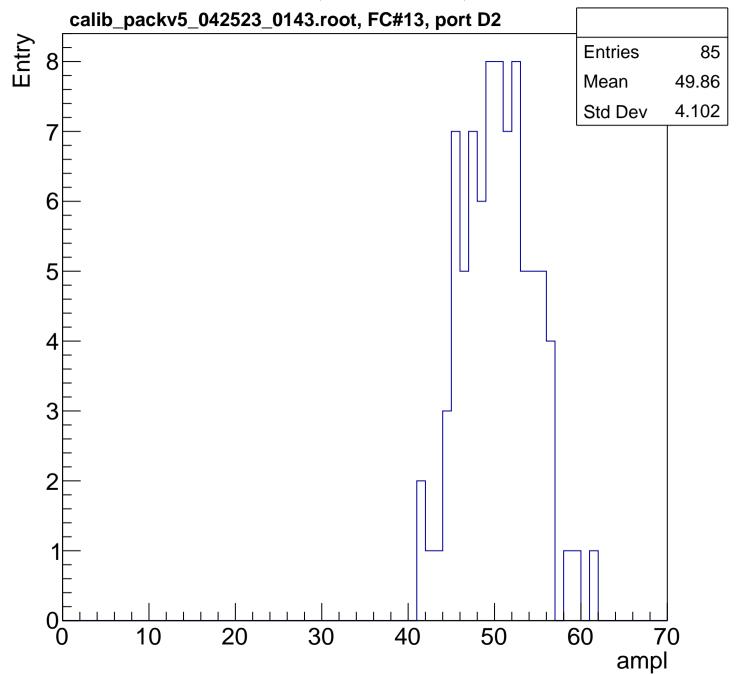


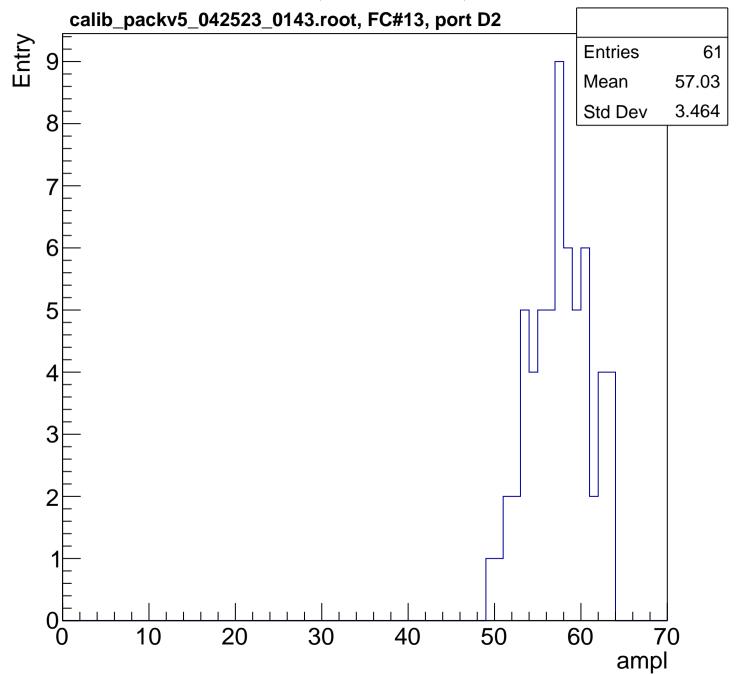


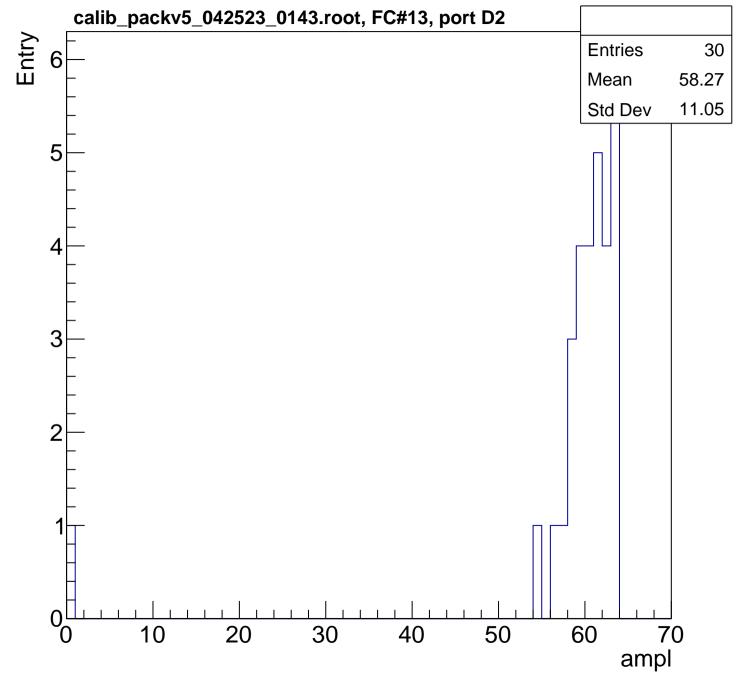


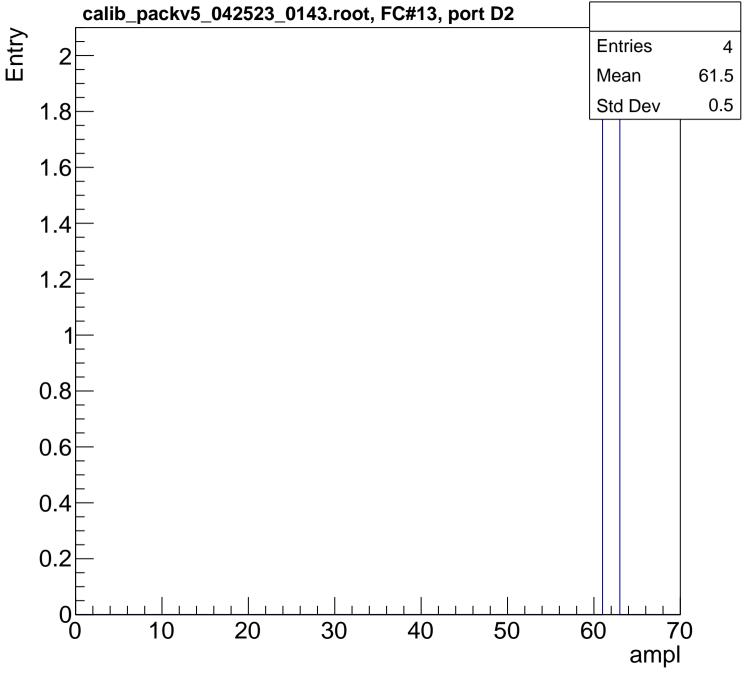


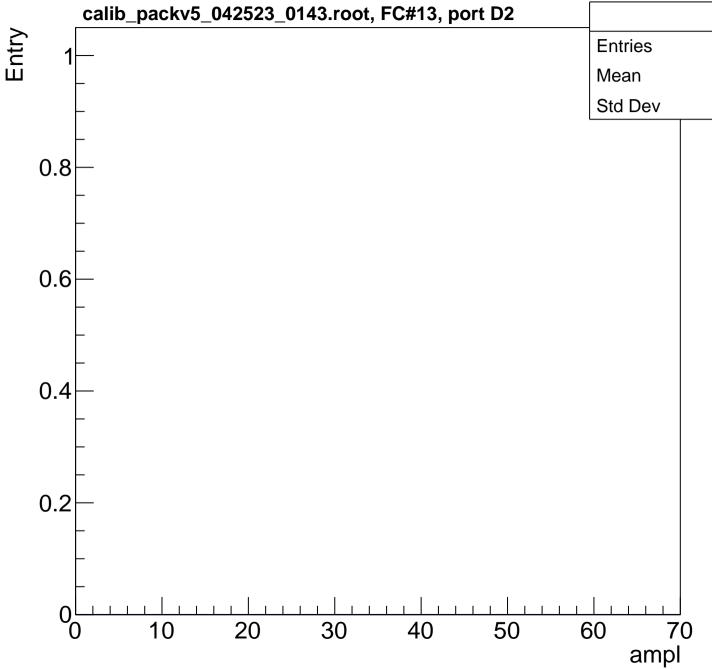


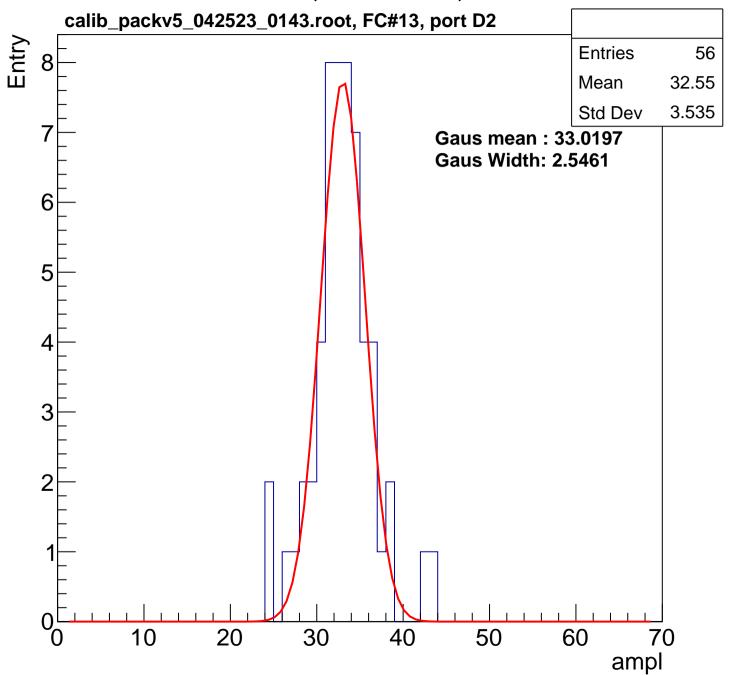


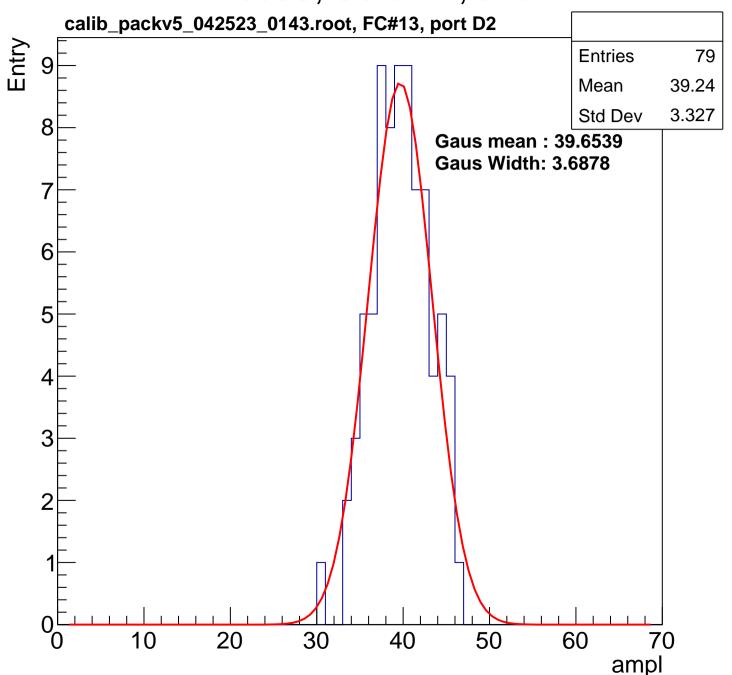


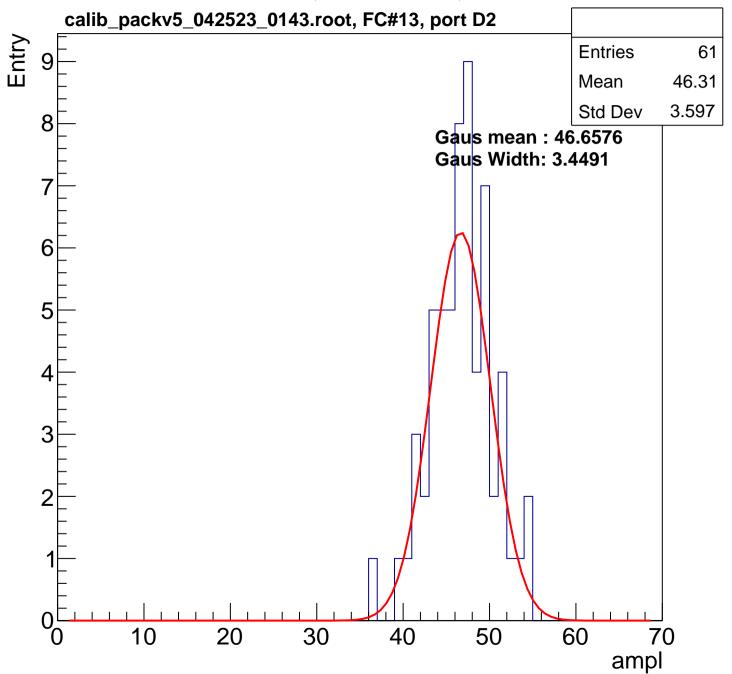


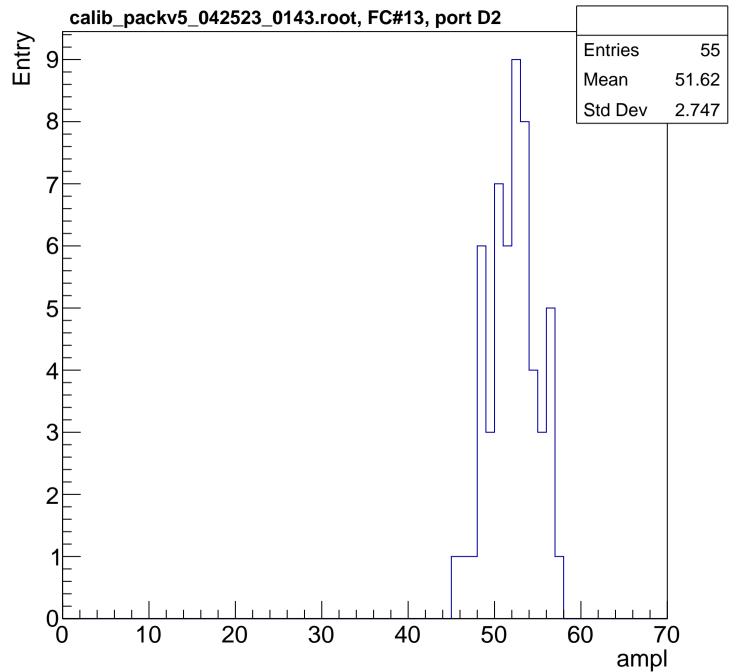


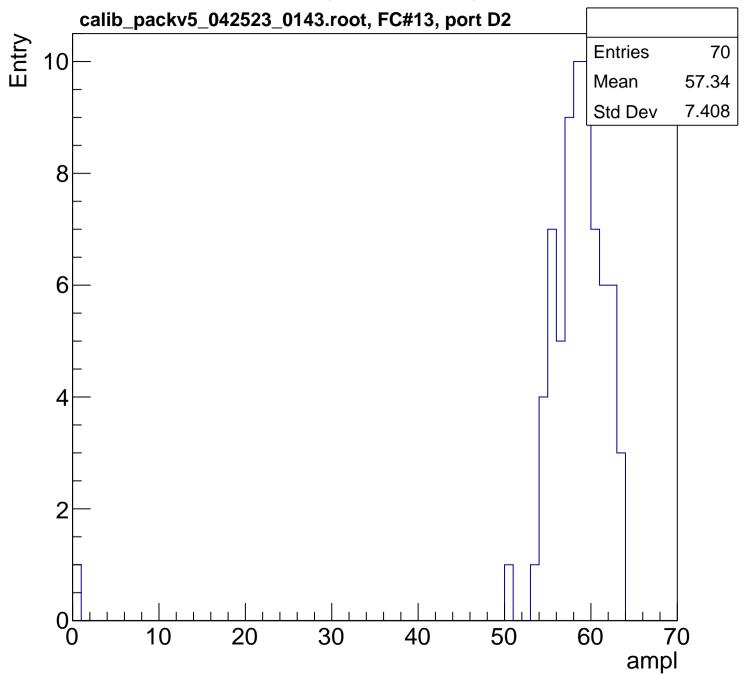


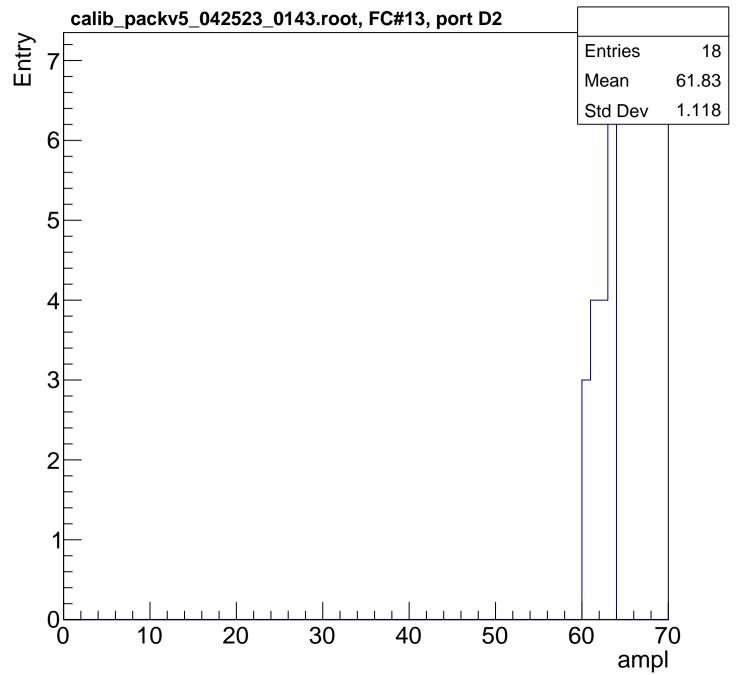


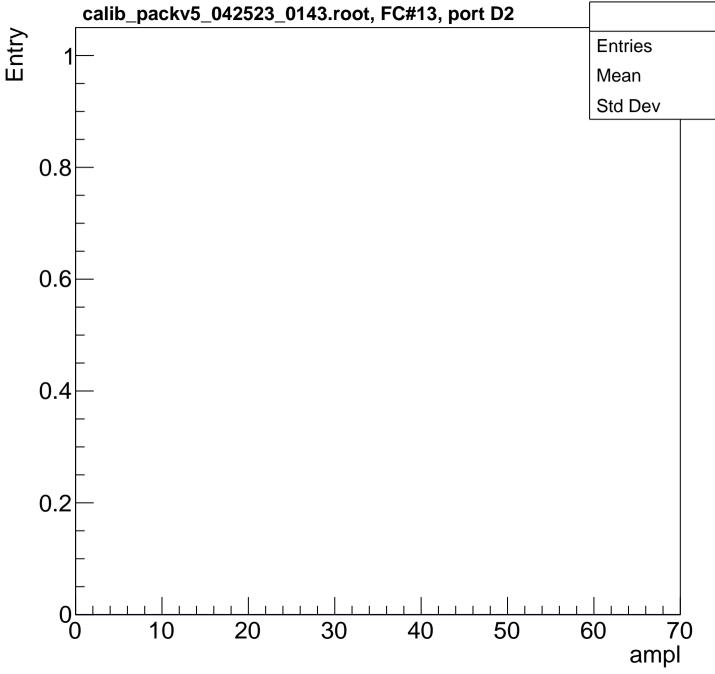




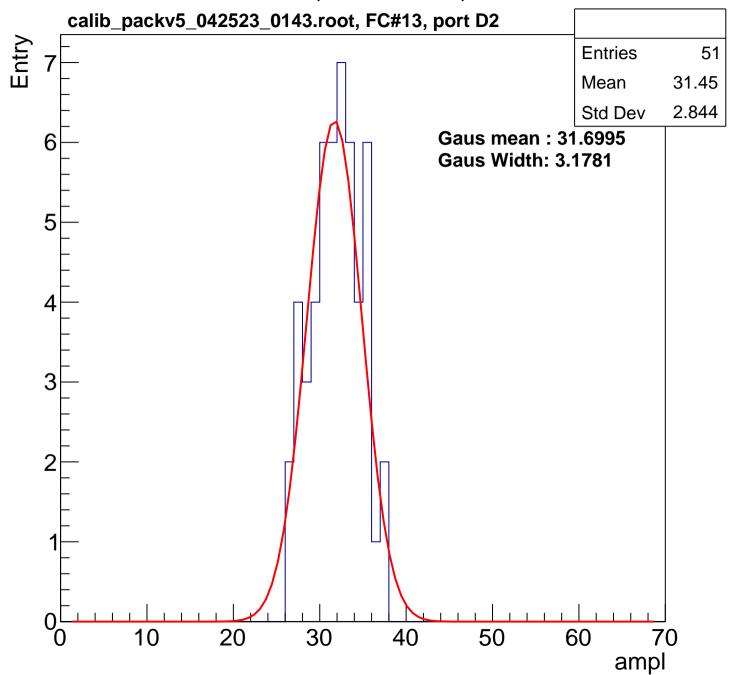


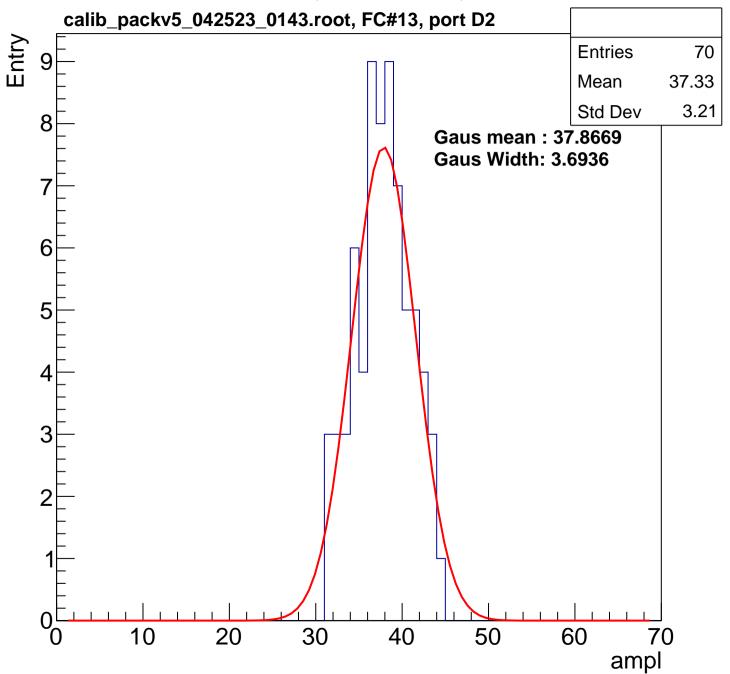


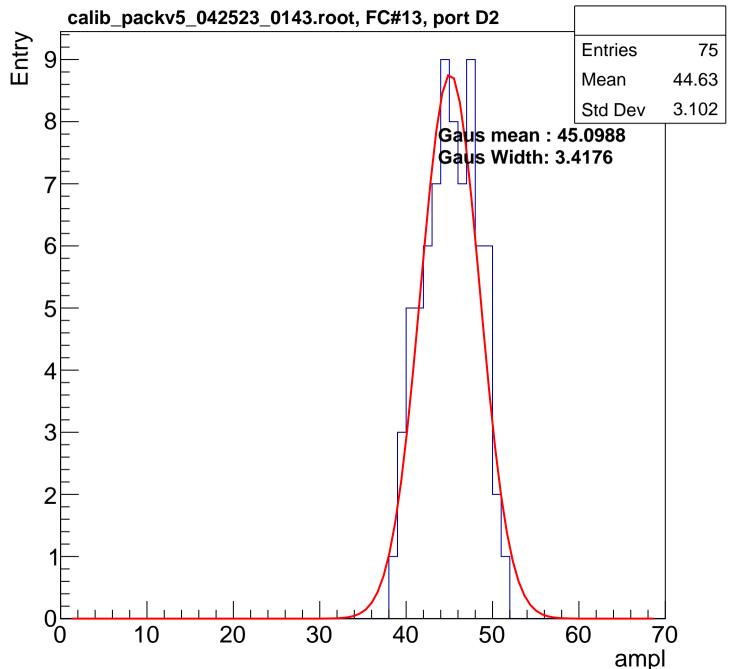


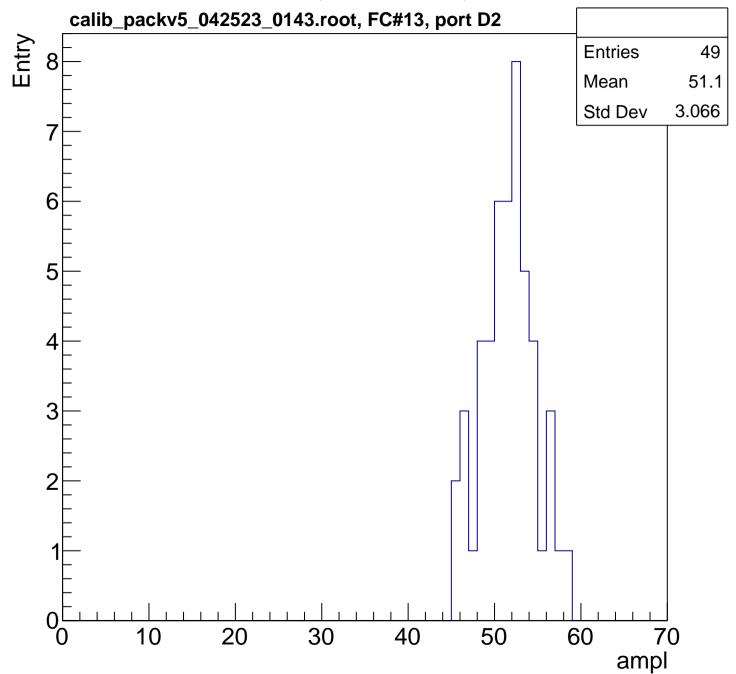


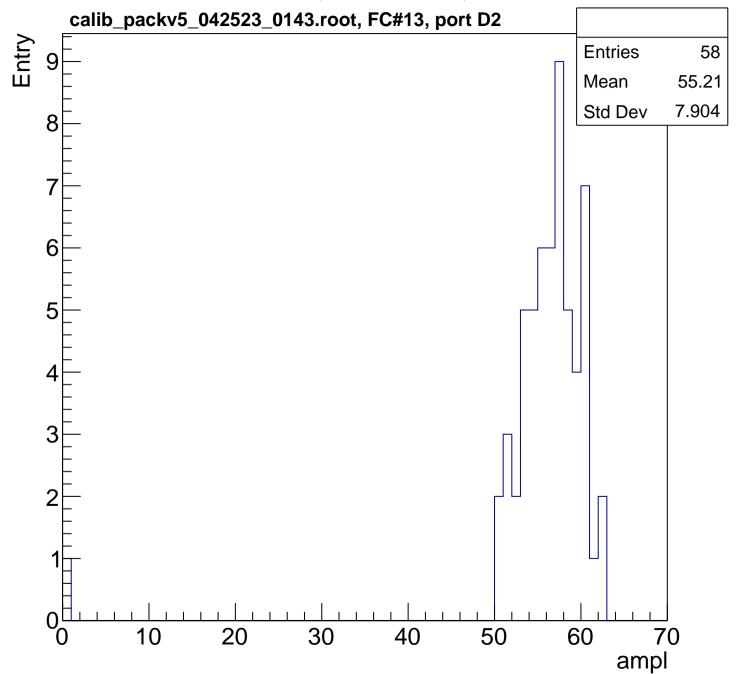
B1L003S, U8-ch27, adc7 calib\_packv5\_042523\_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

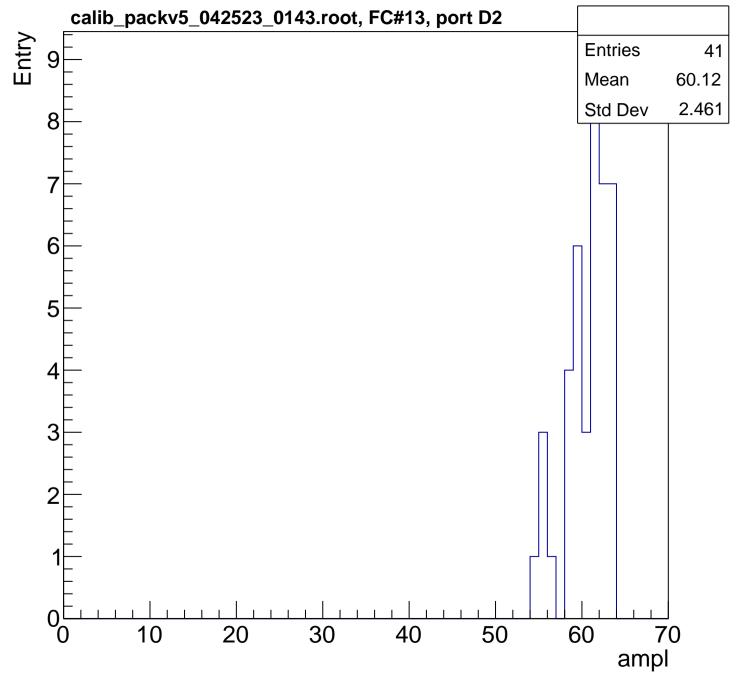


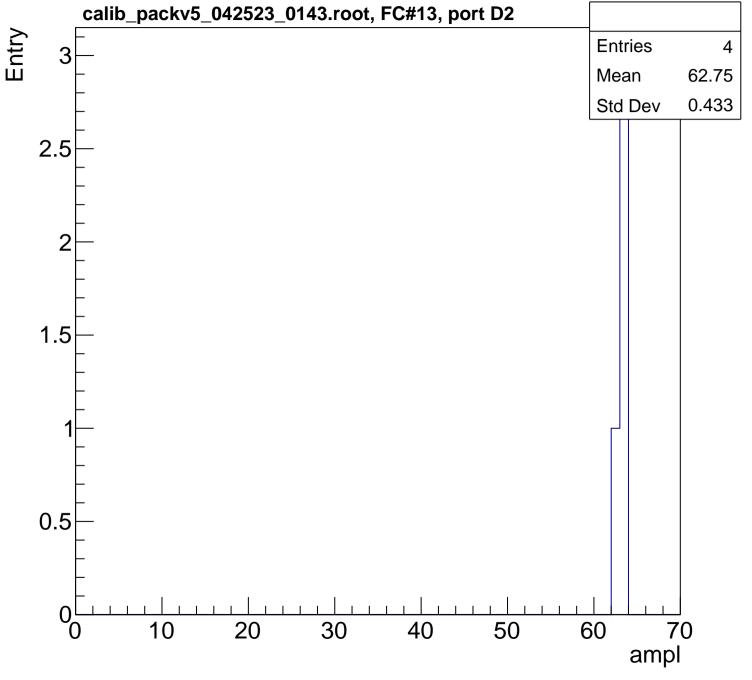


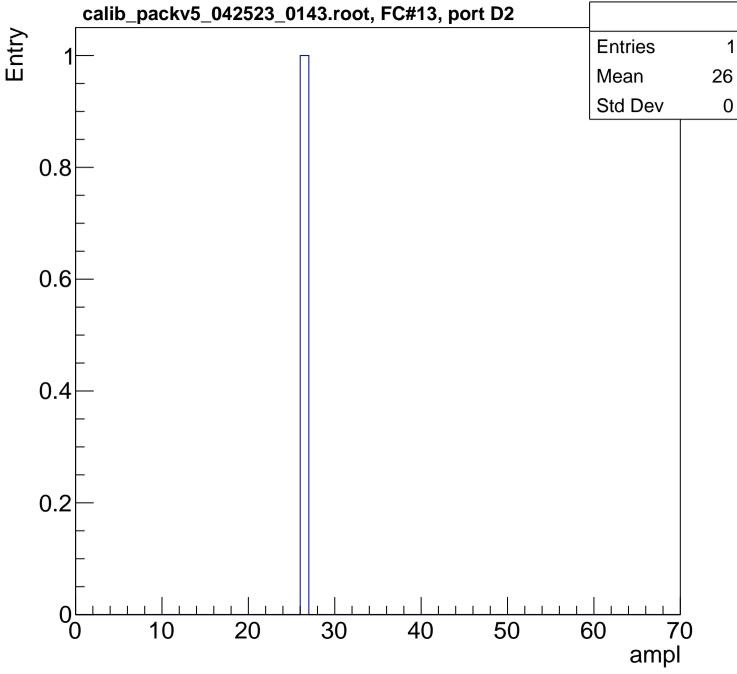


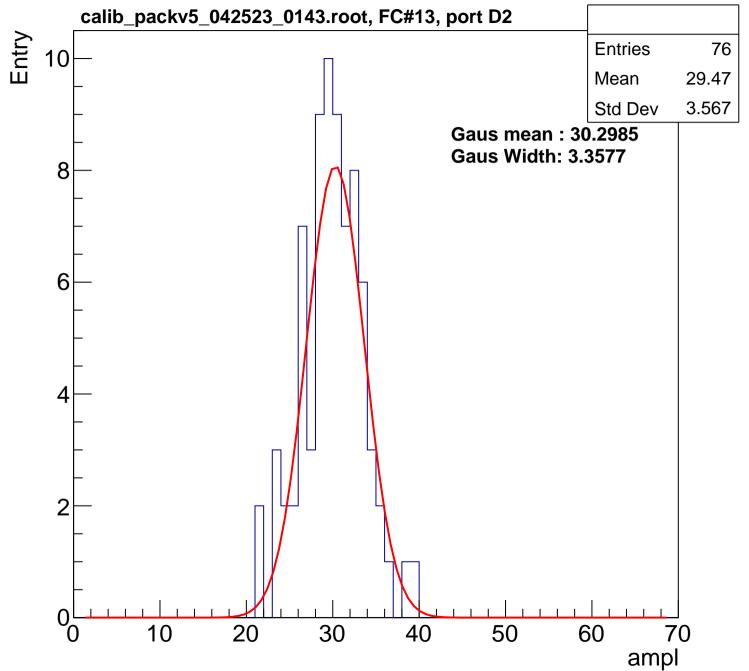


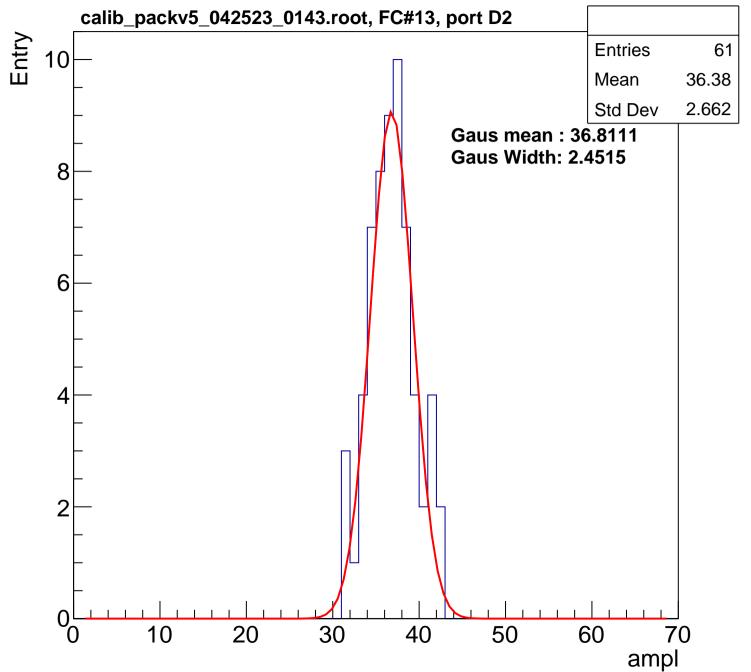


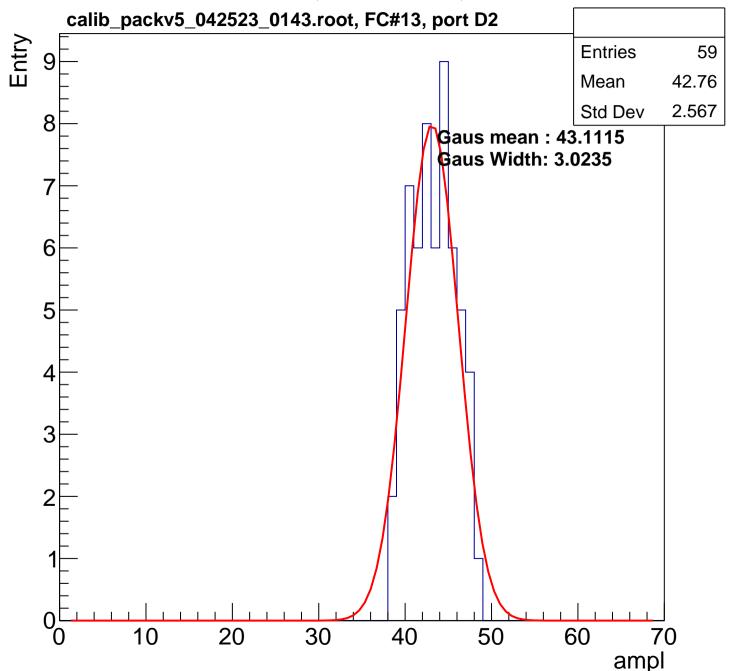


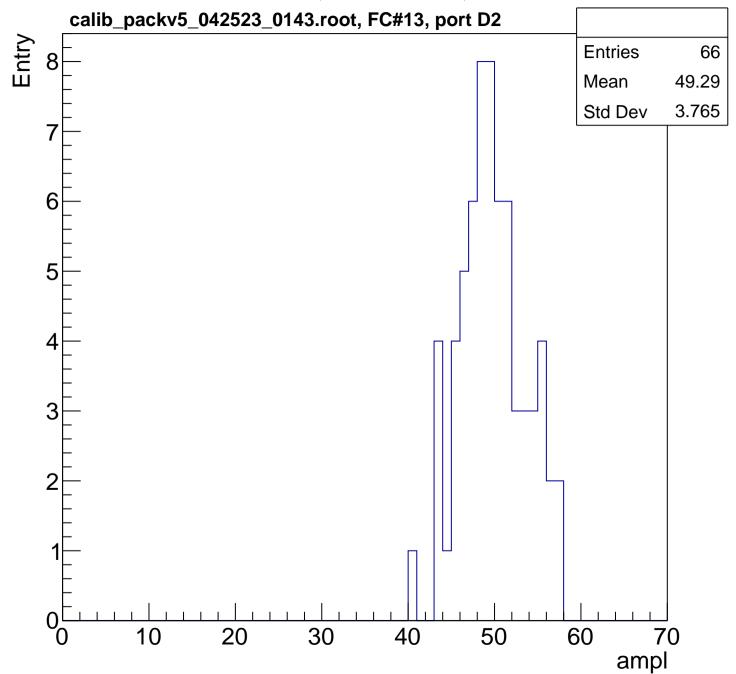


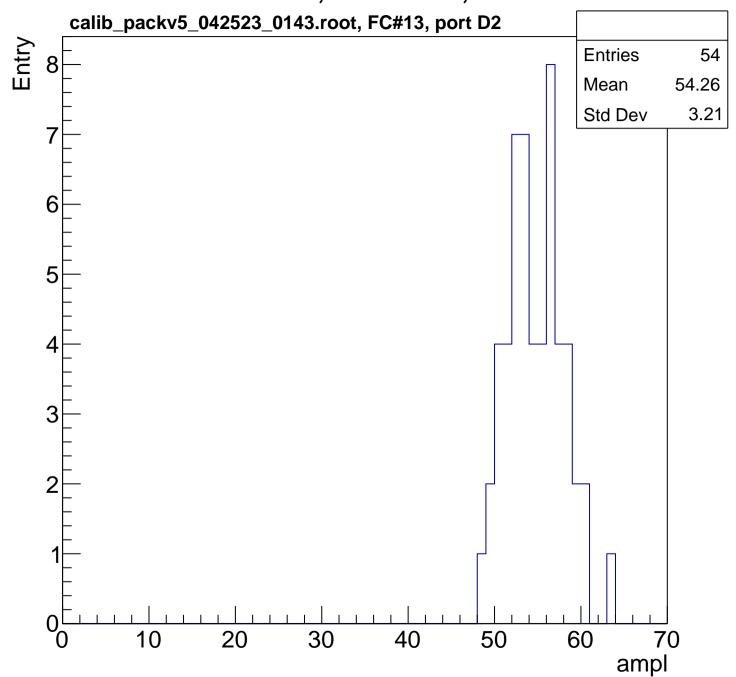


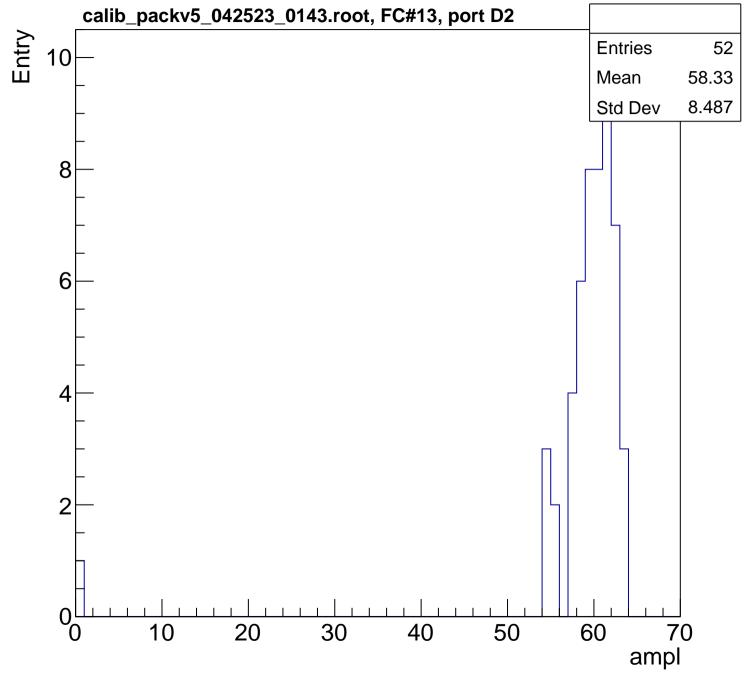


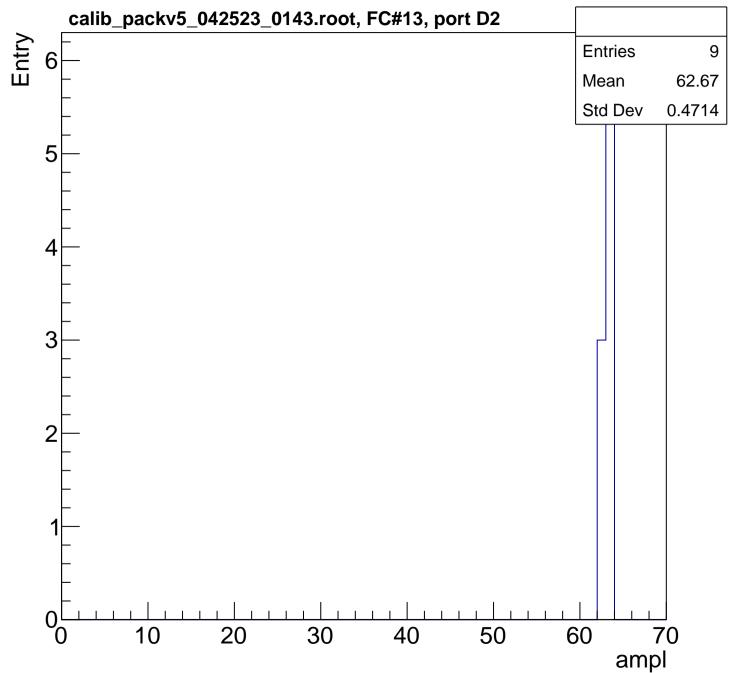




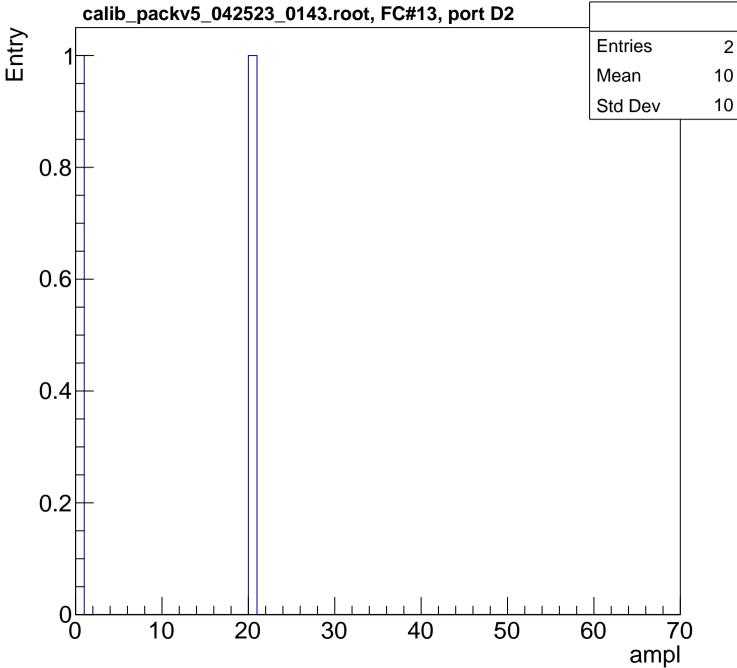


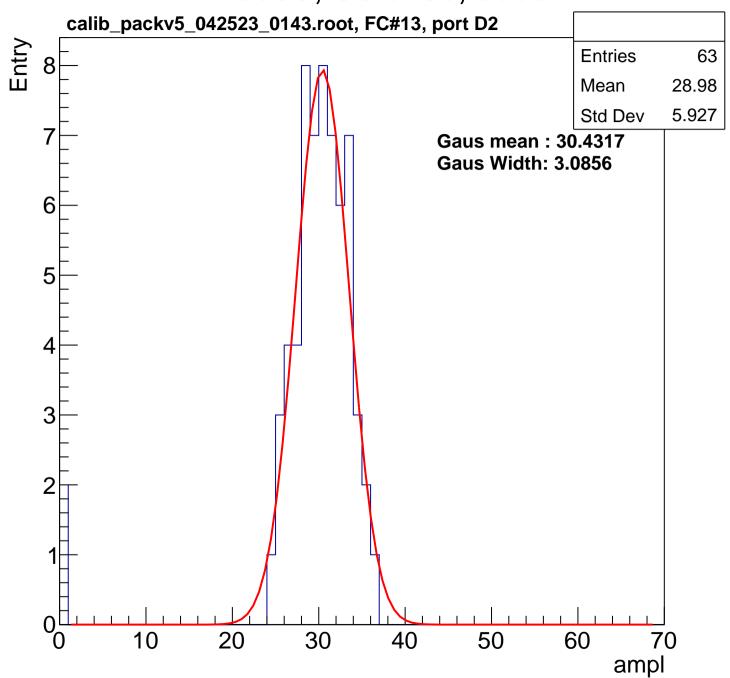


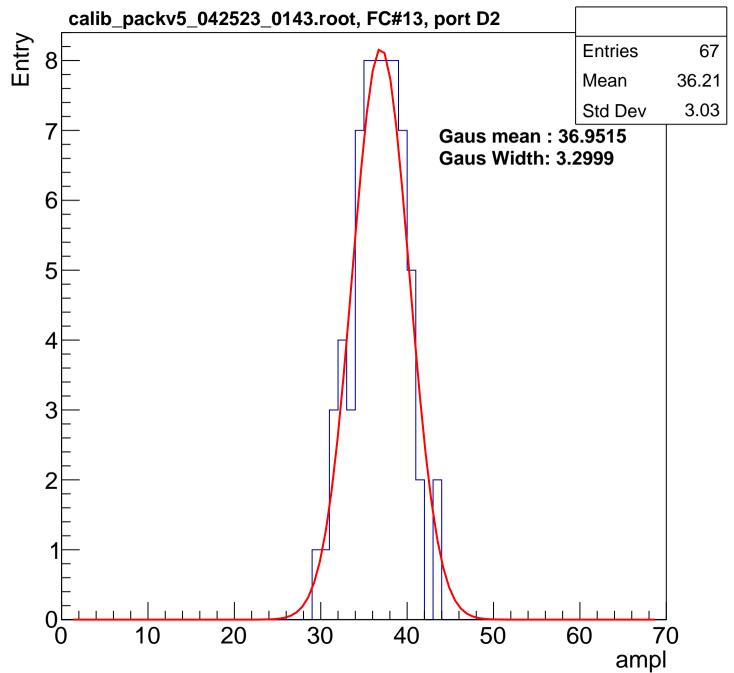


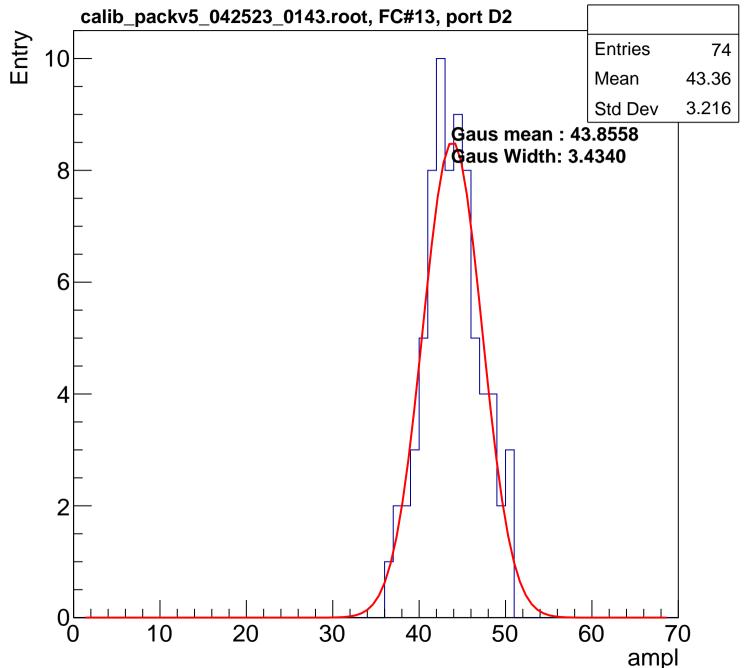


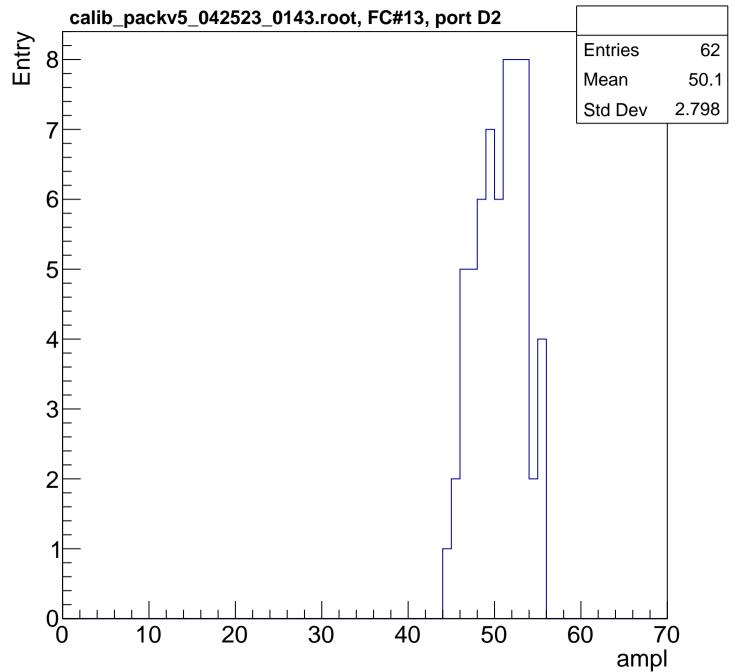
2

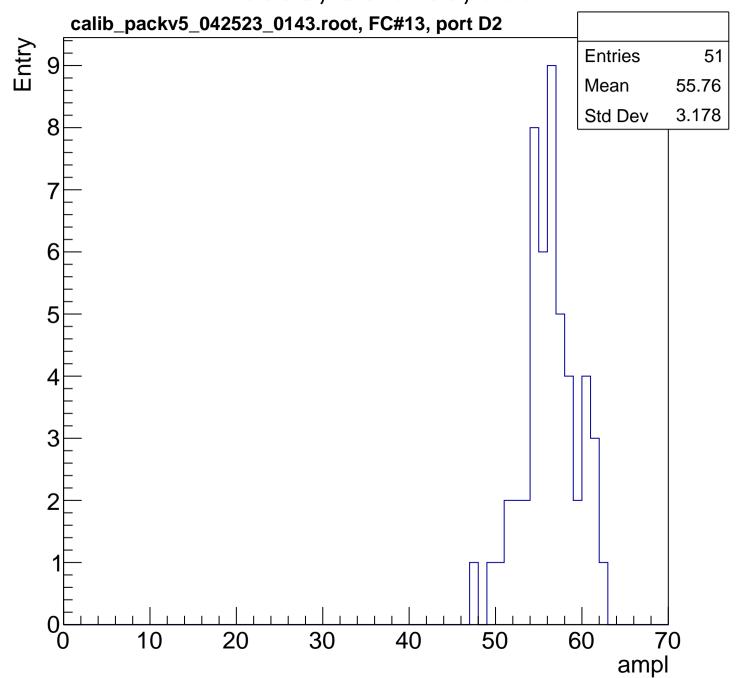


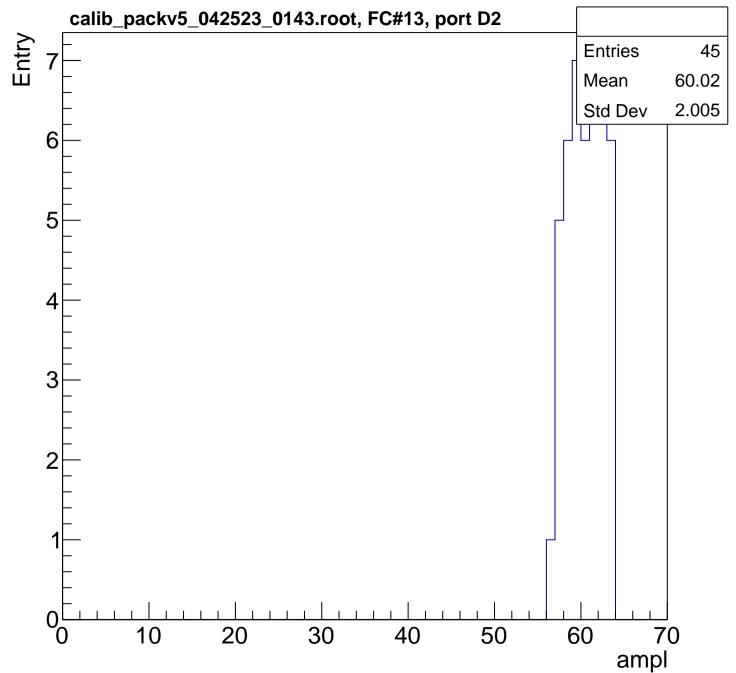


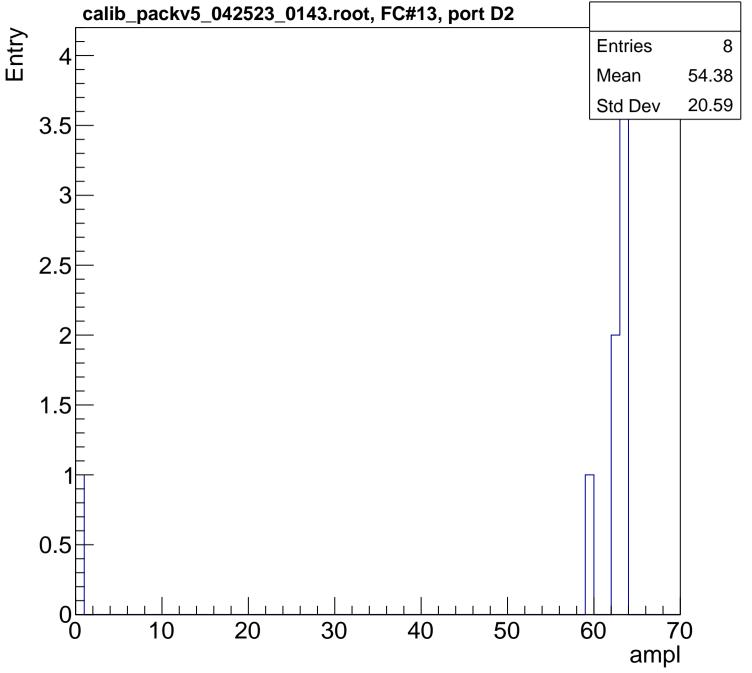


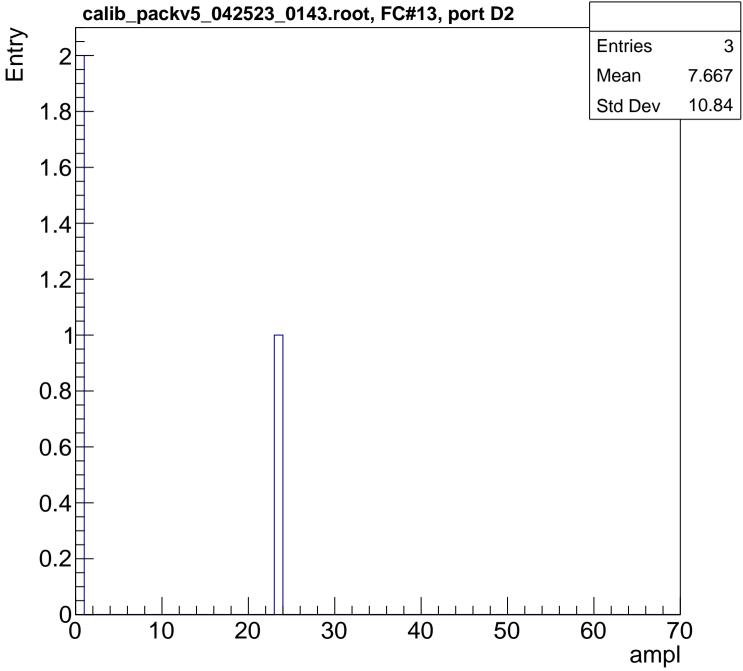


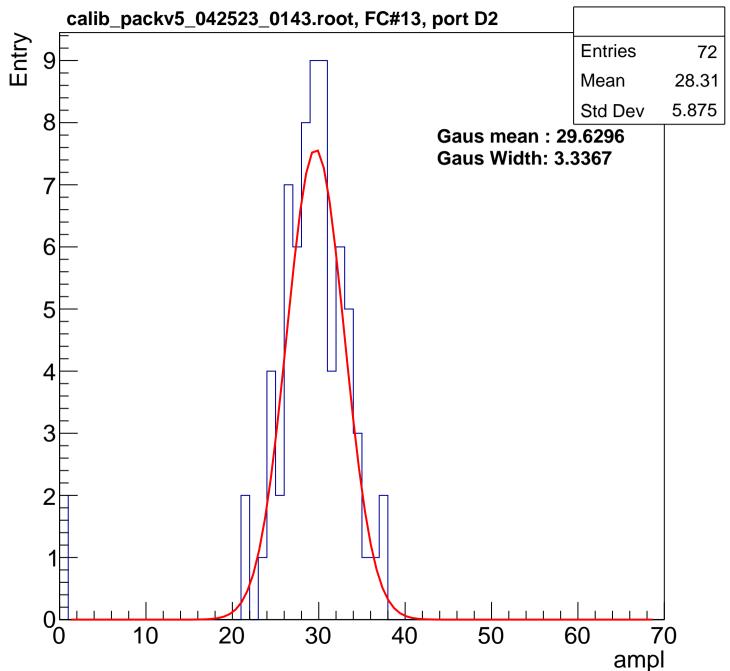


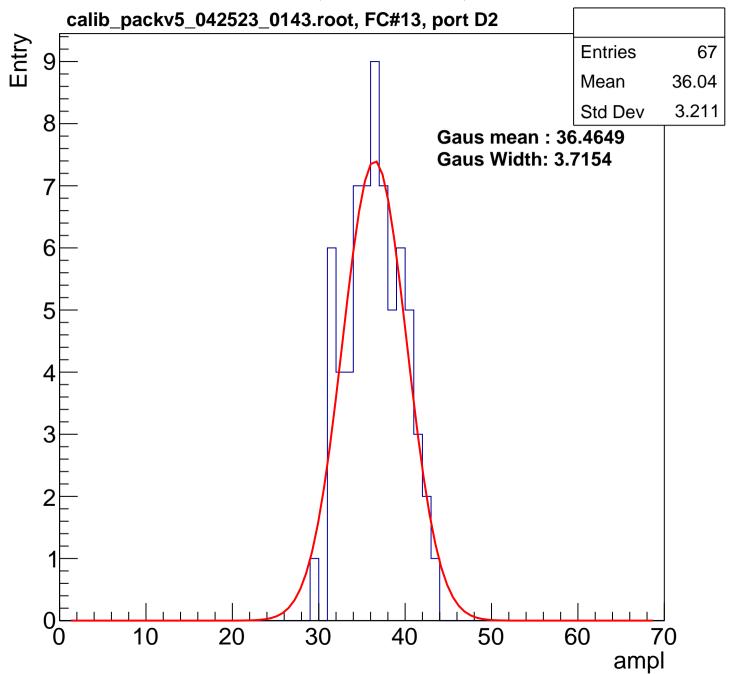


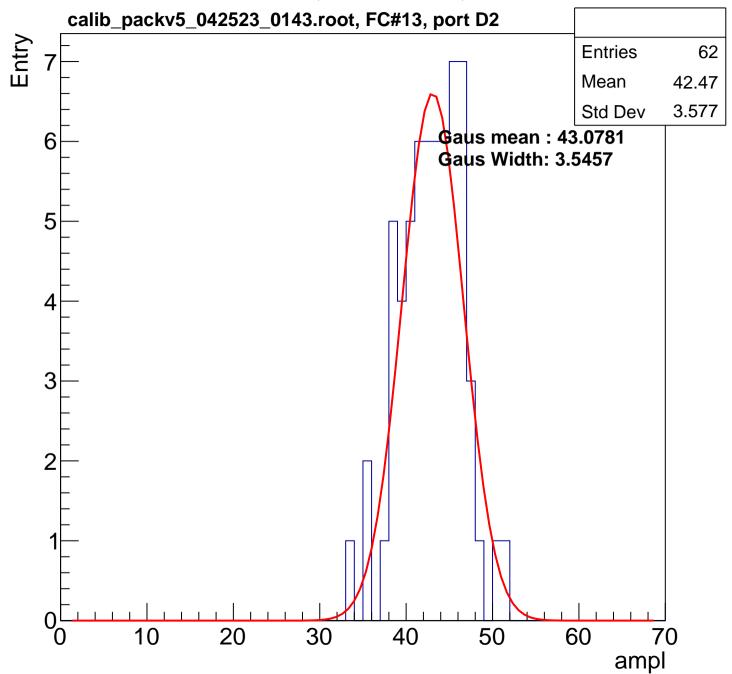


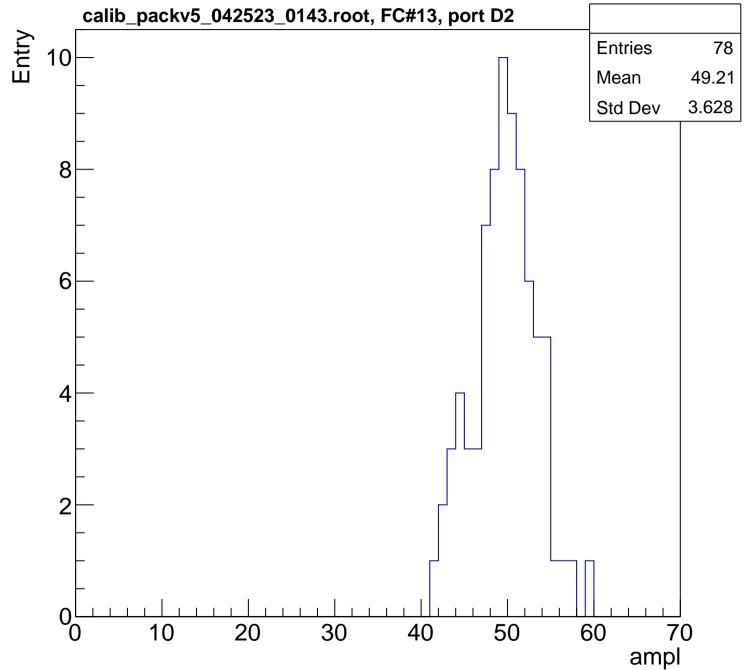


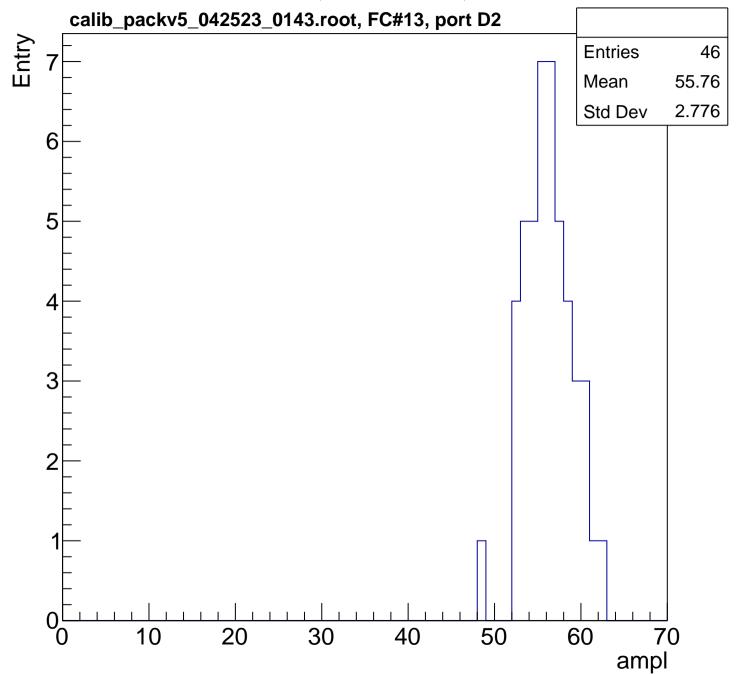


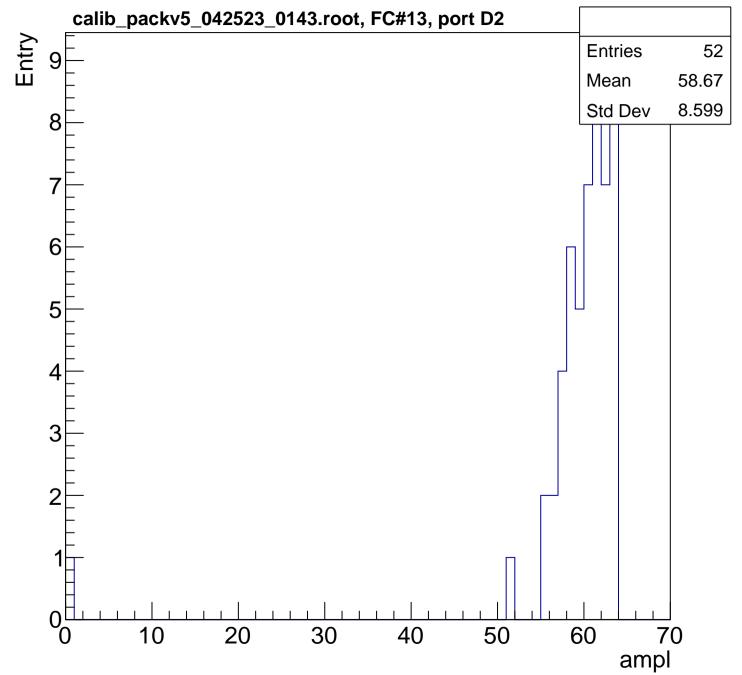


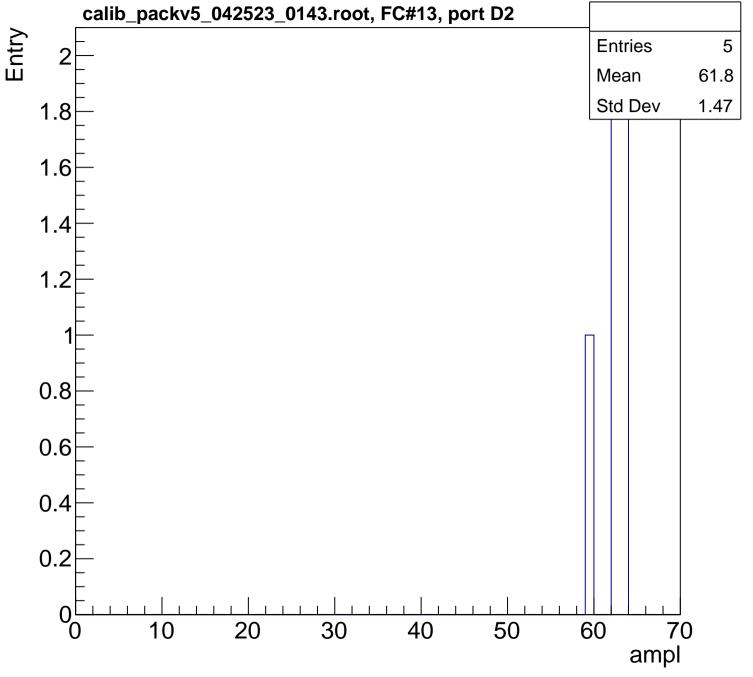




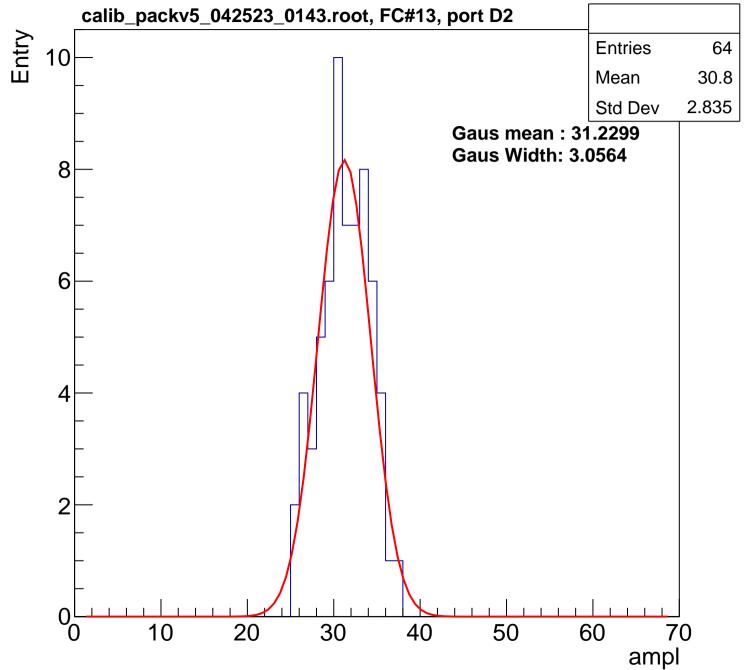


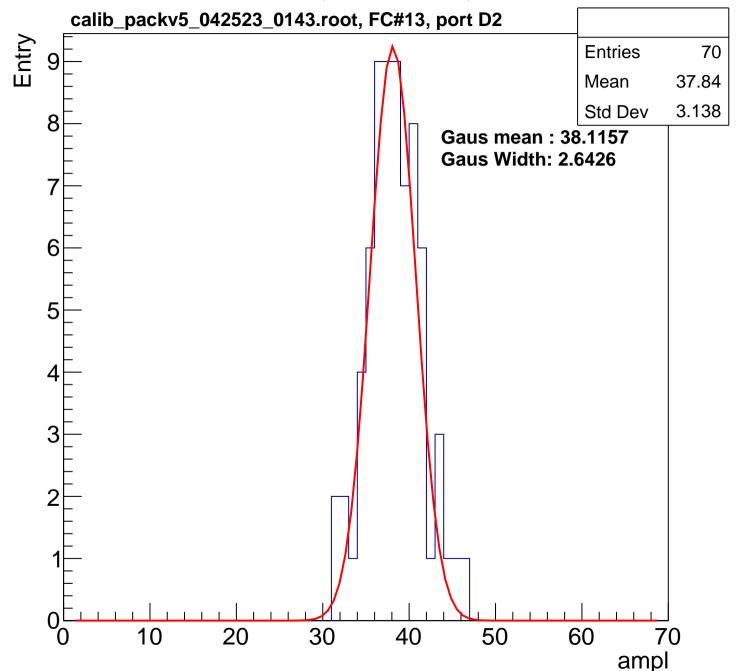


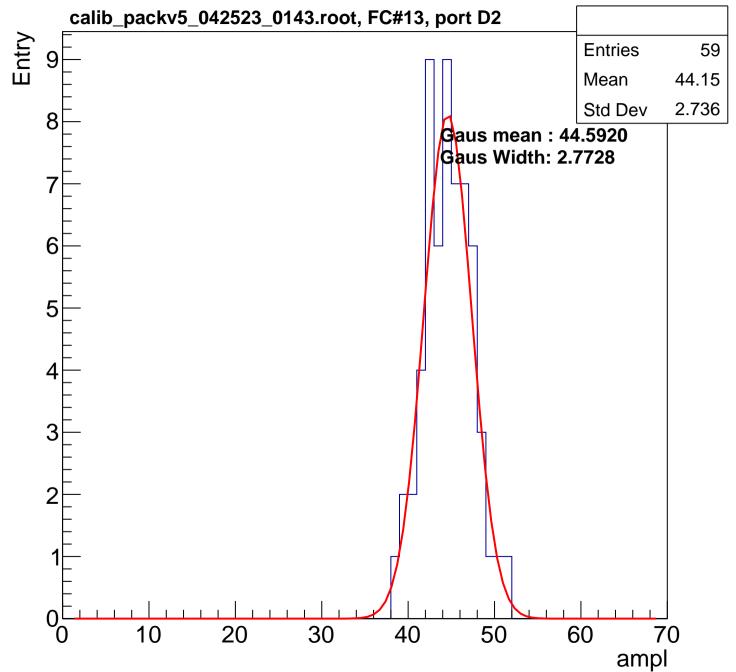


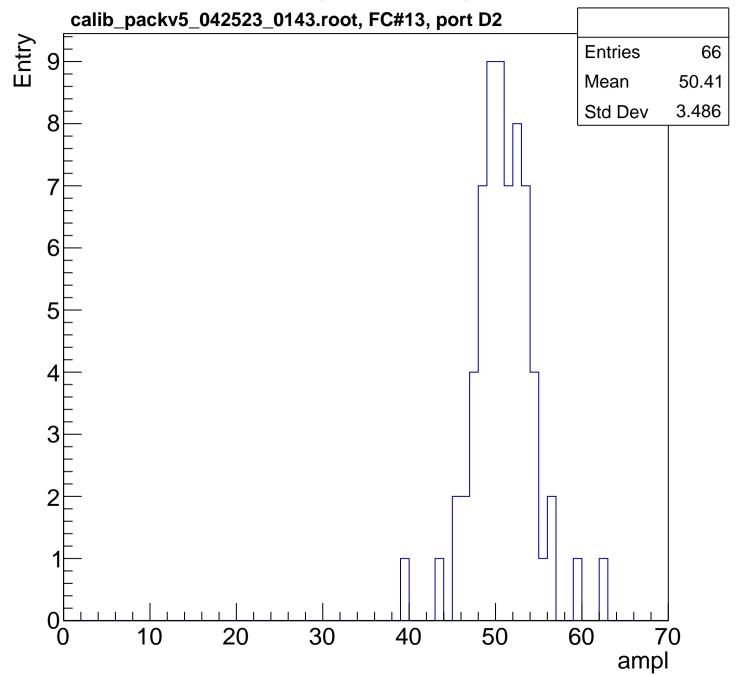


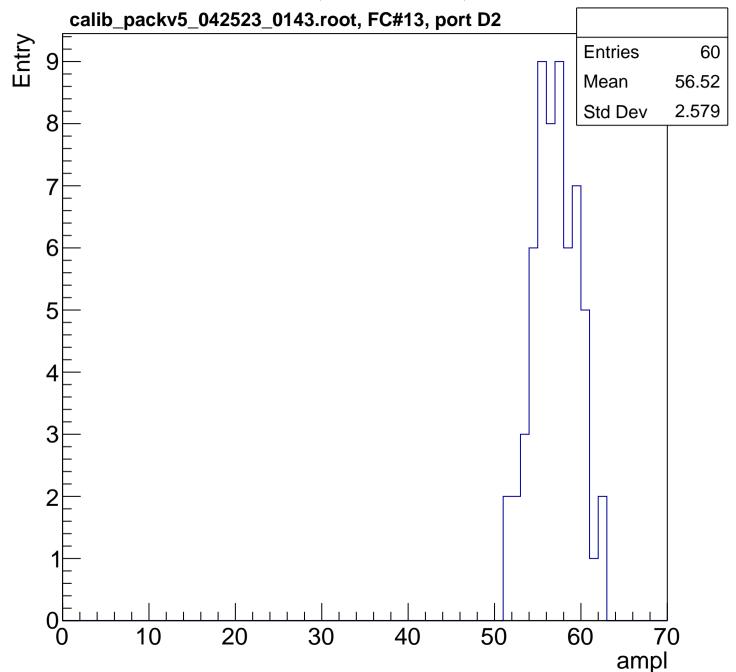


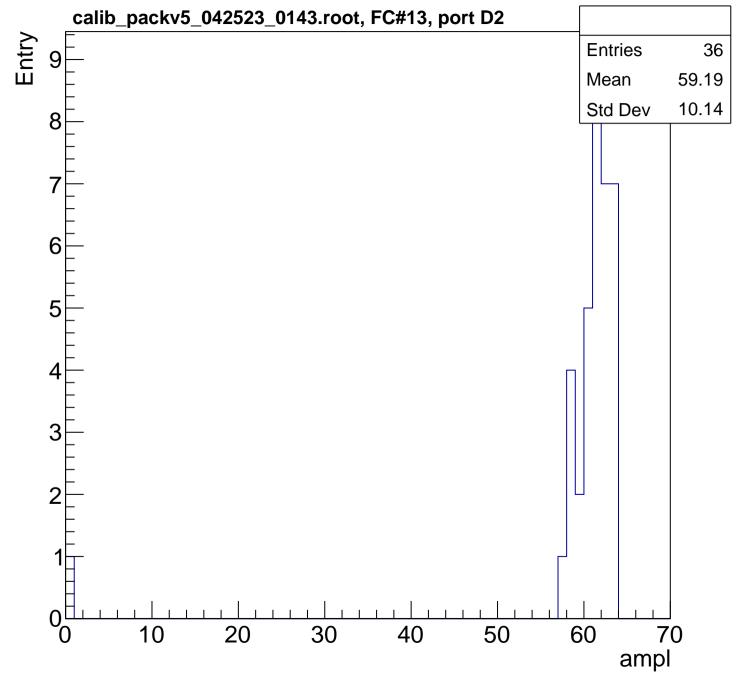


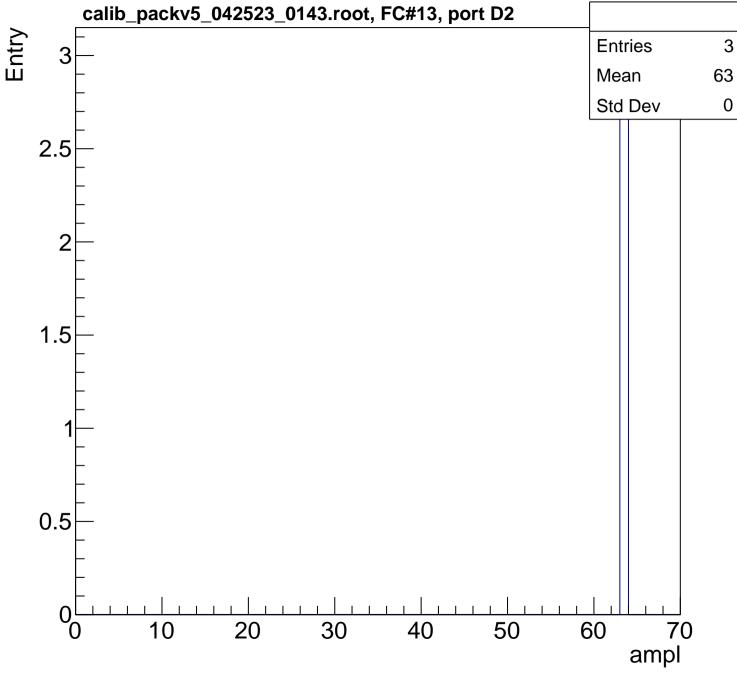




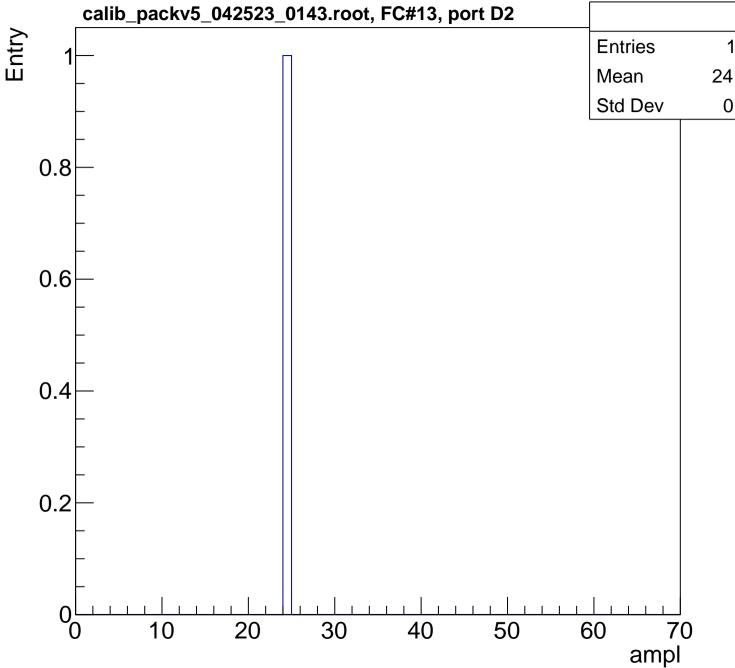


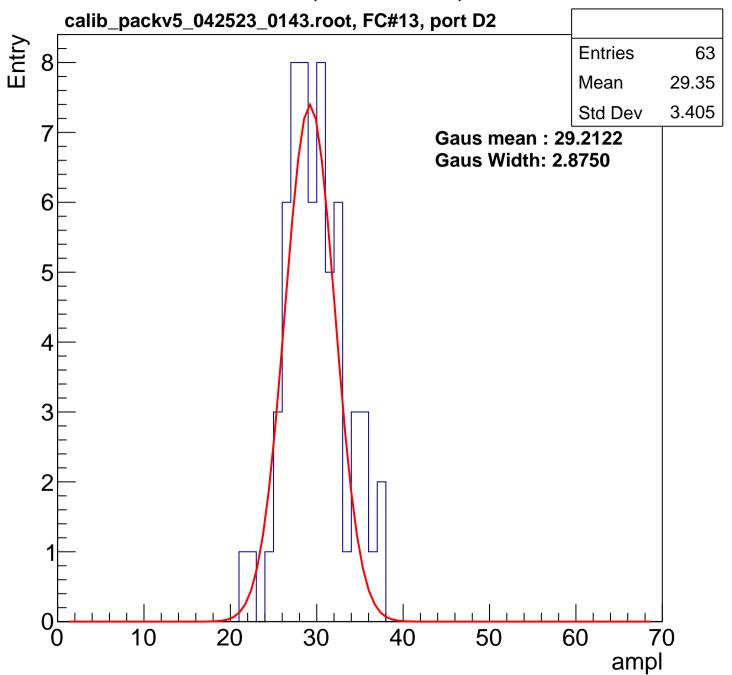


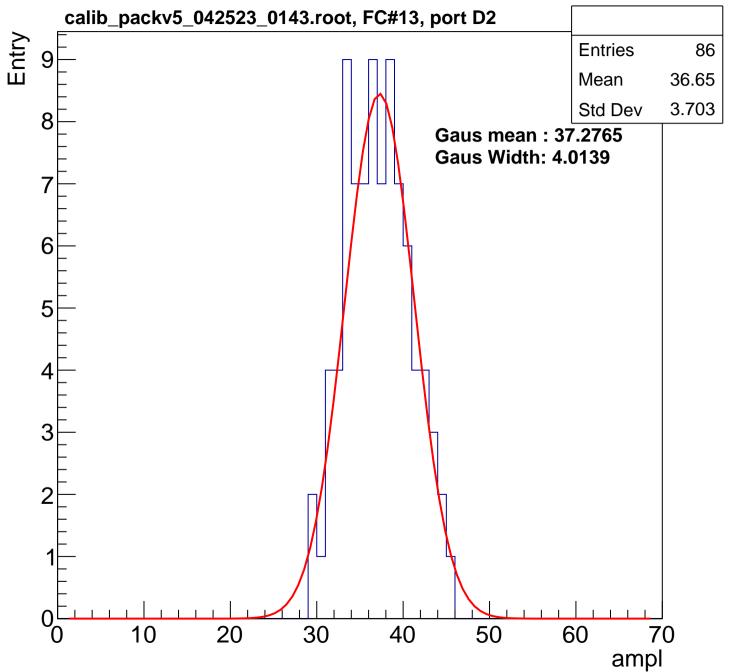


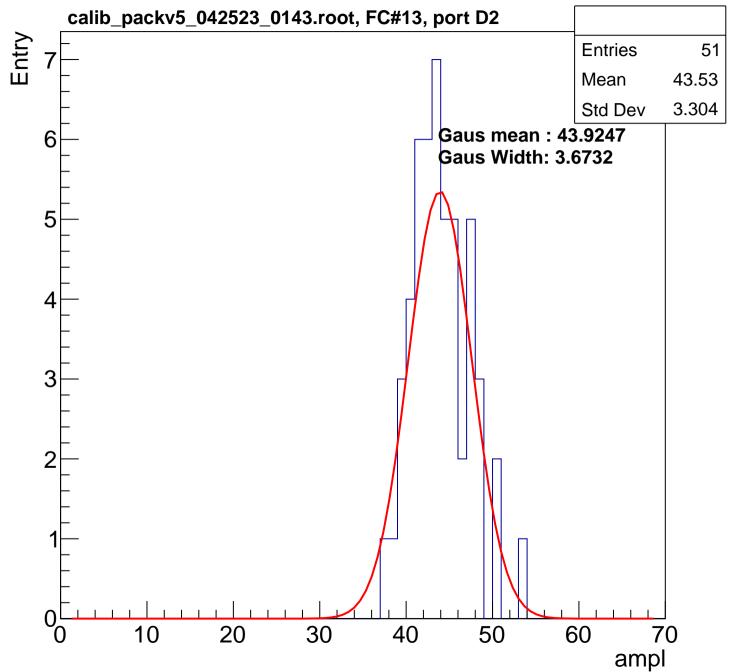


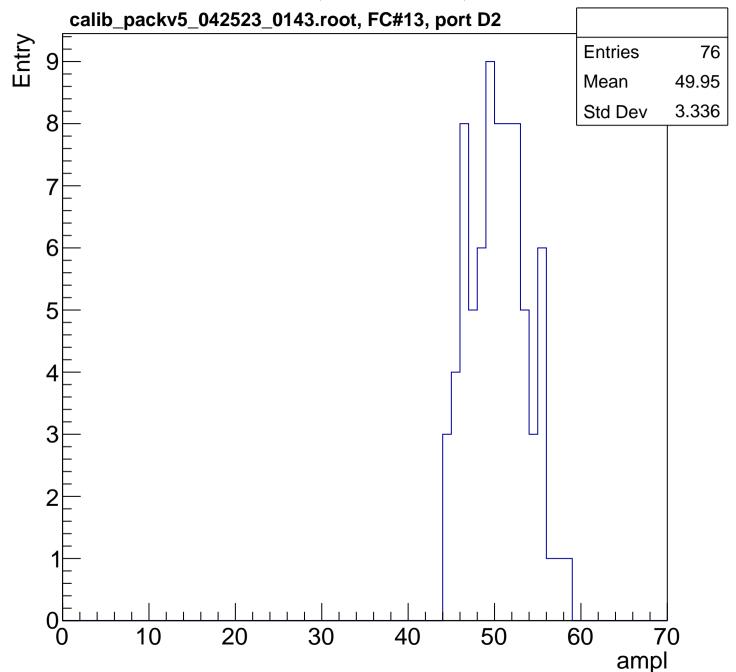
0

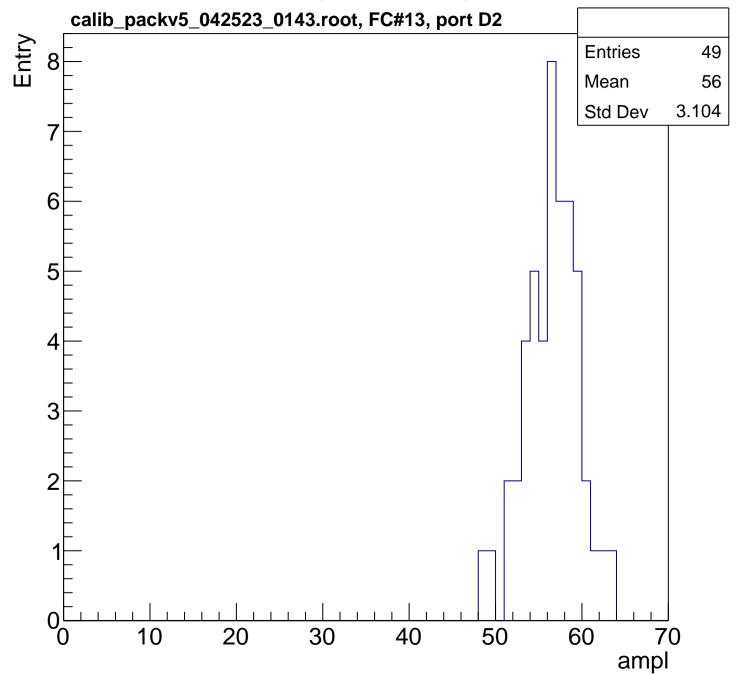


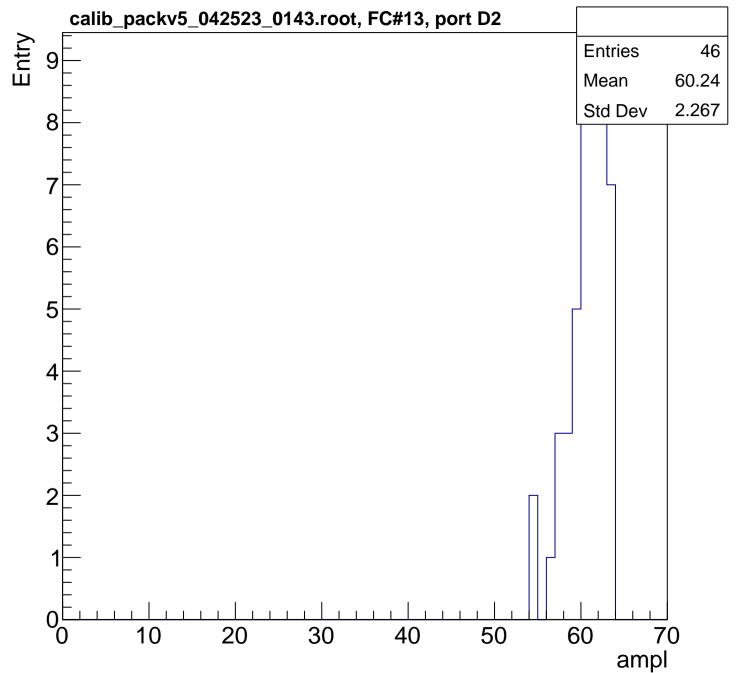


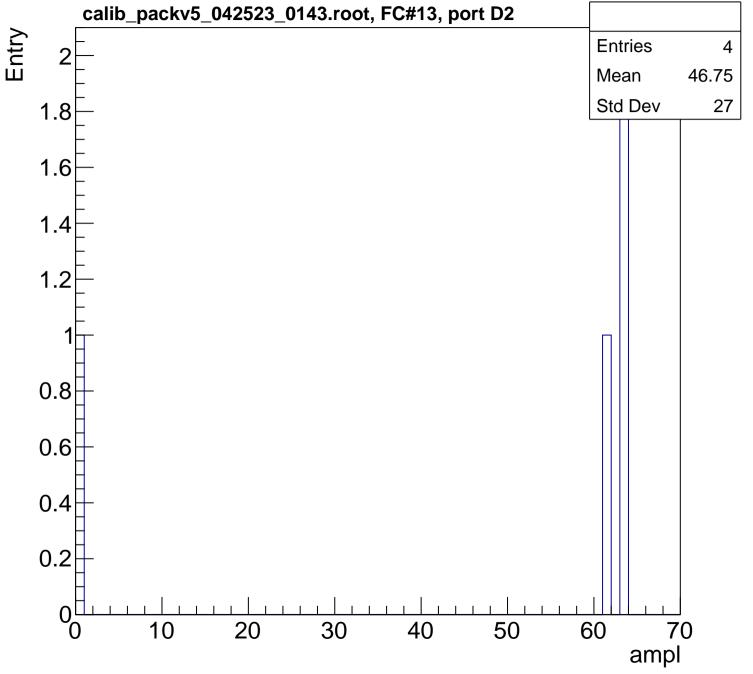




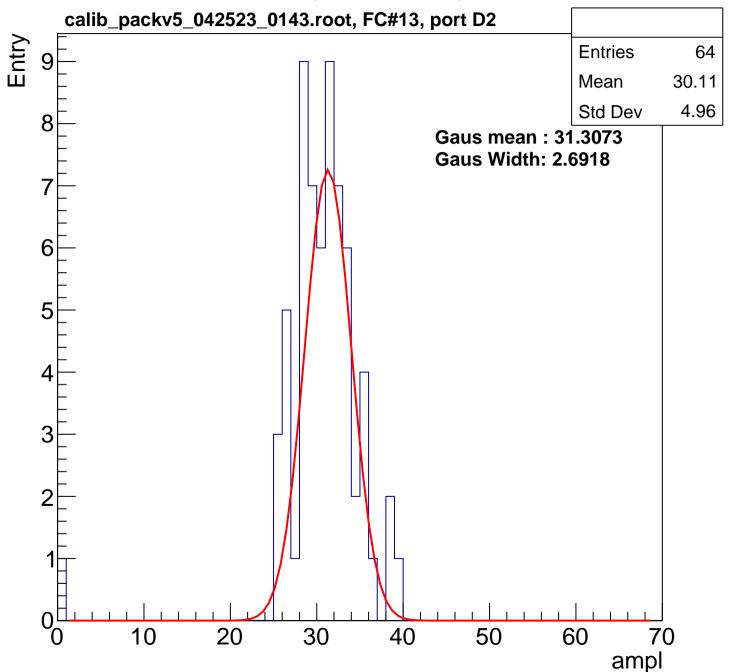


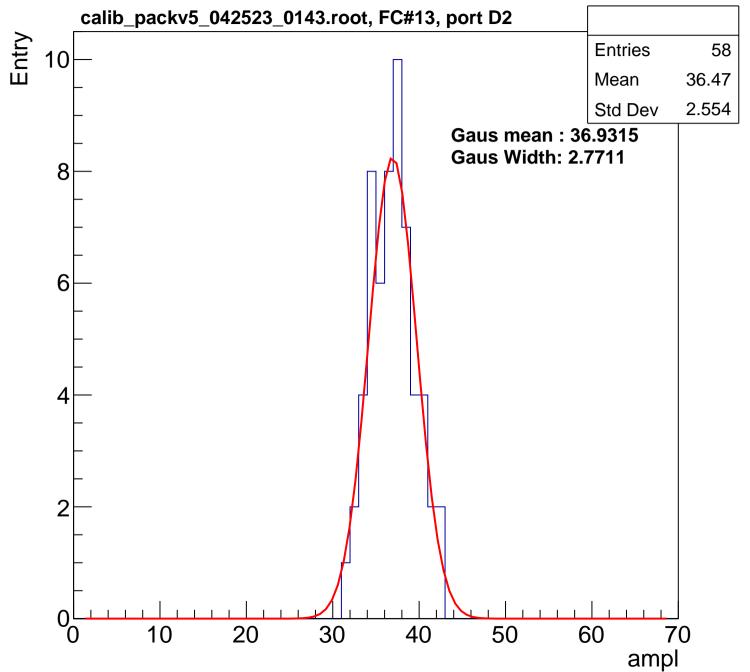


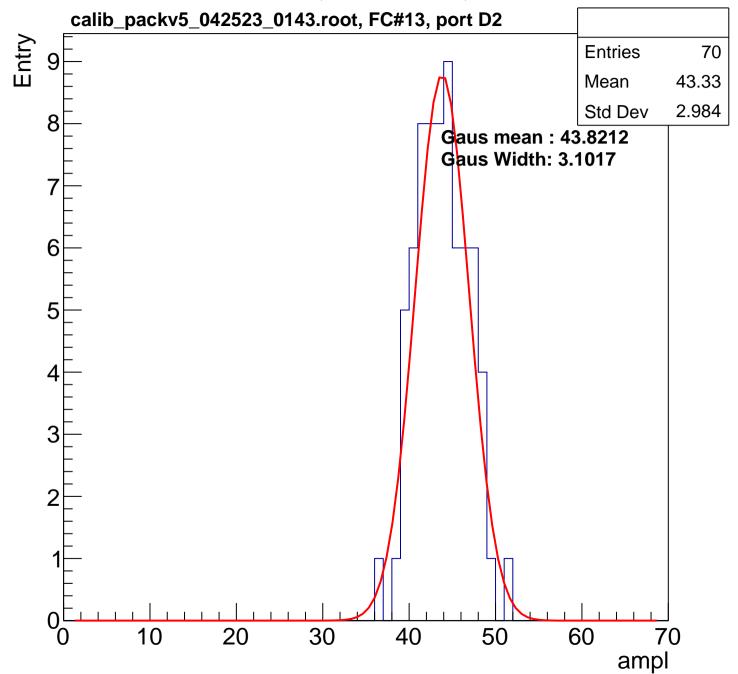


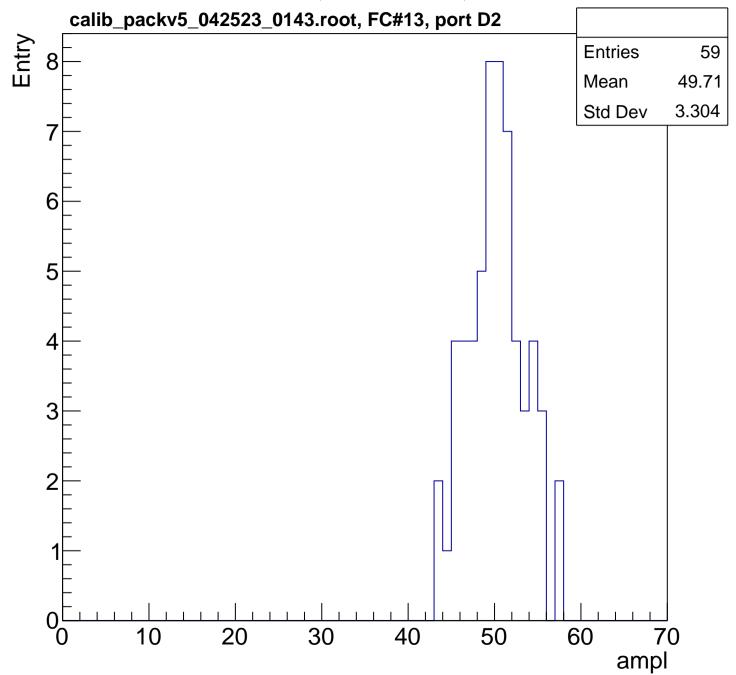


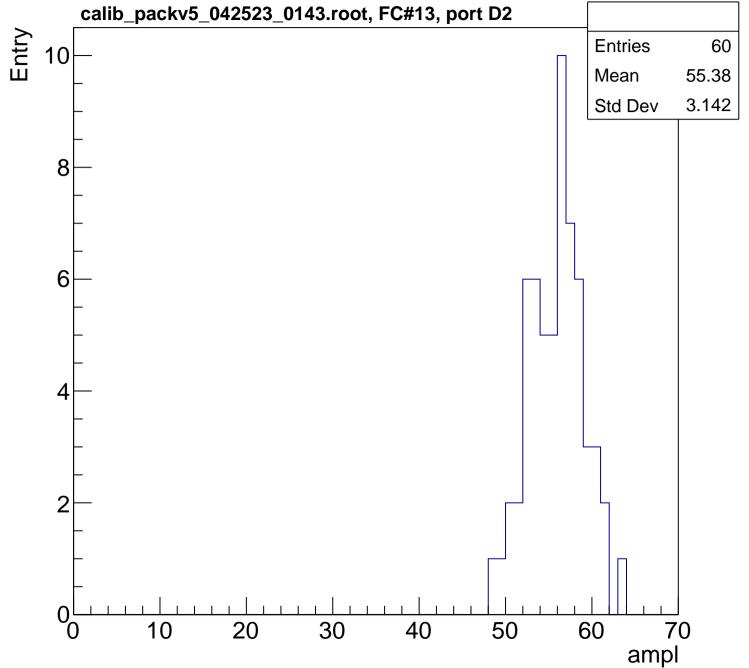


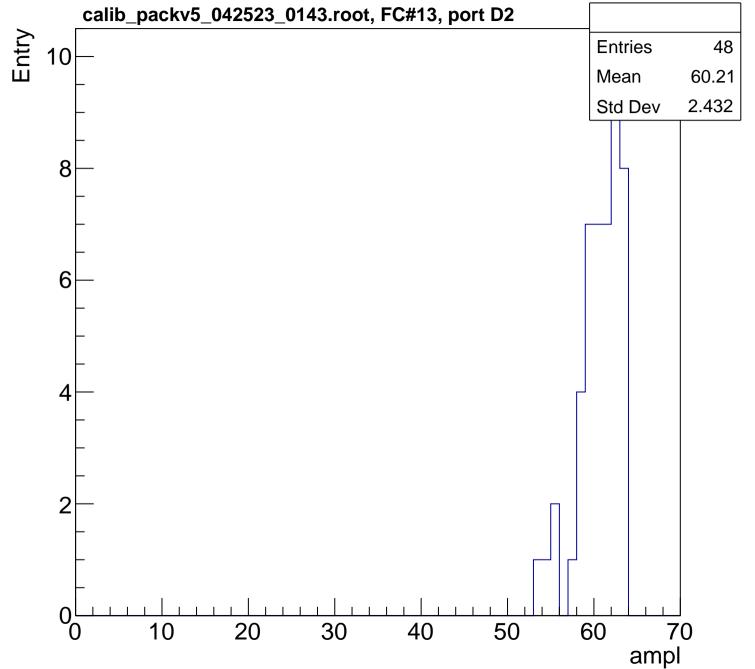


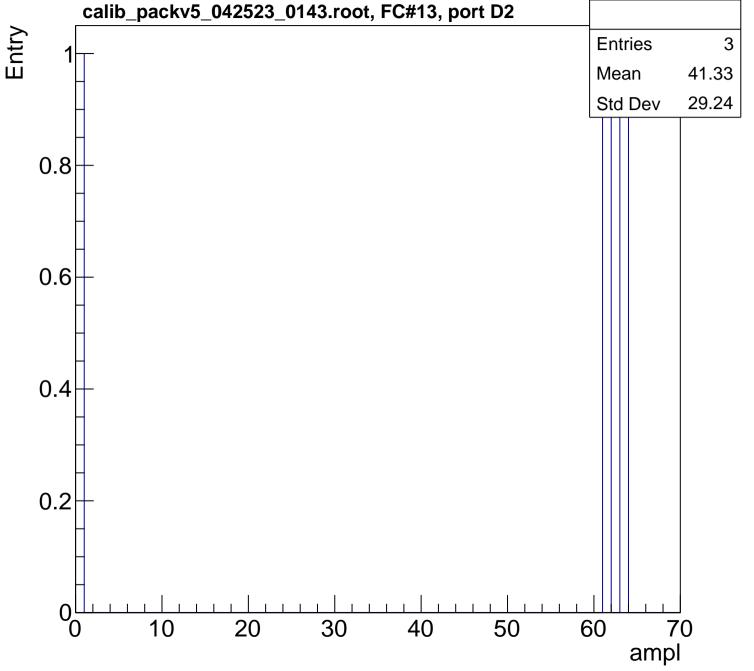


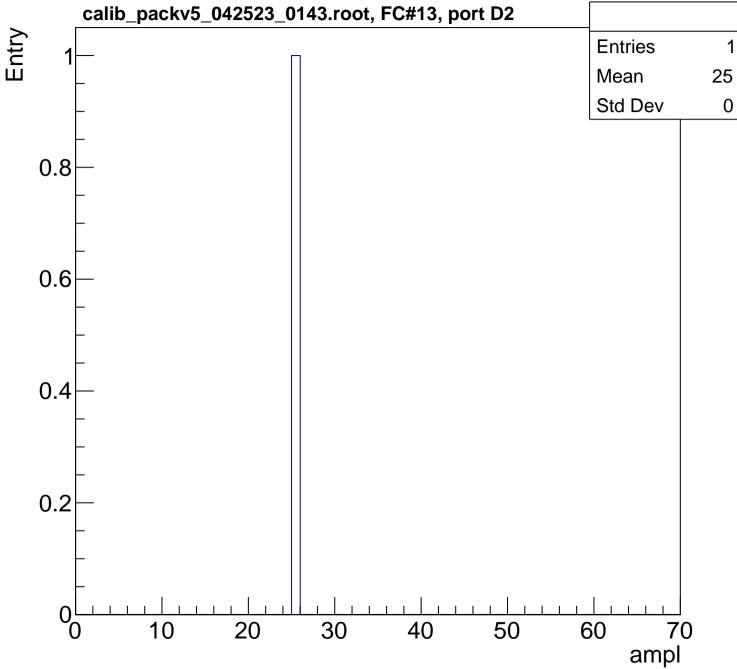


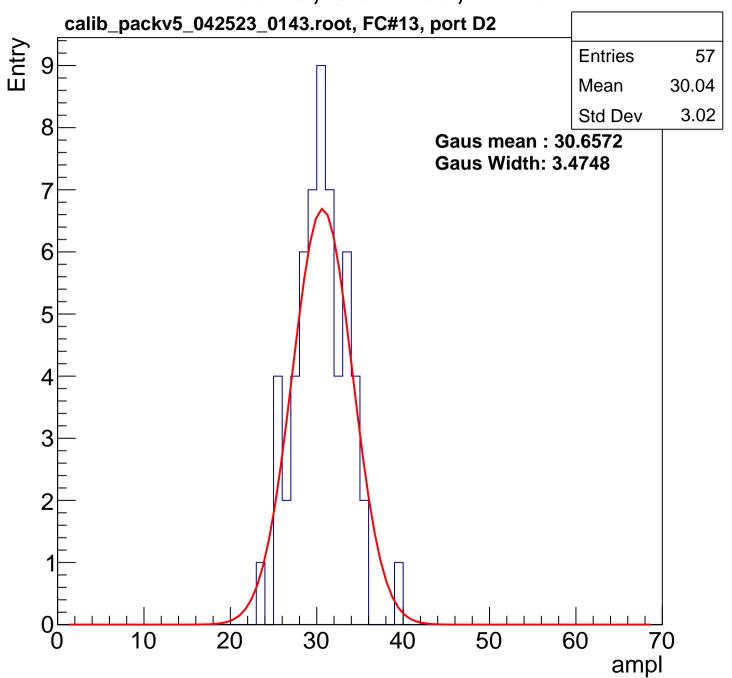


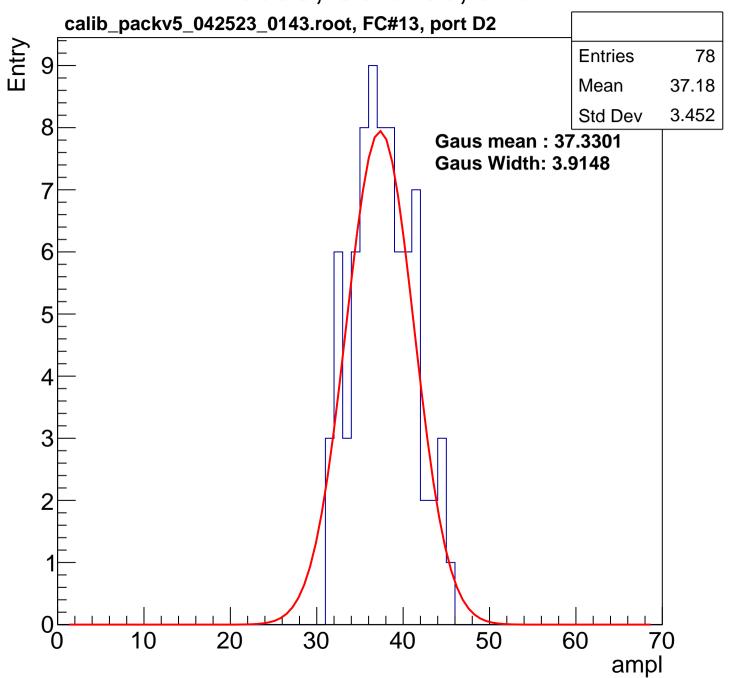


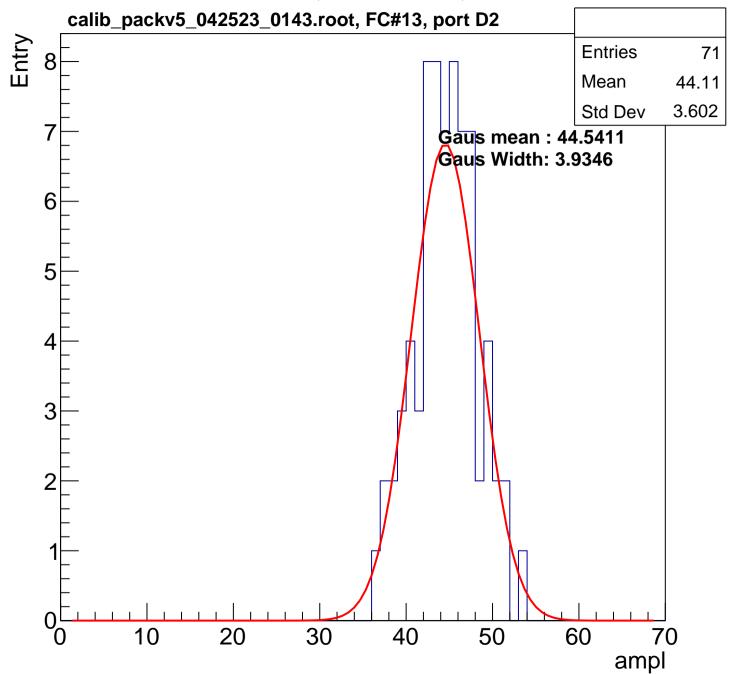


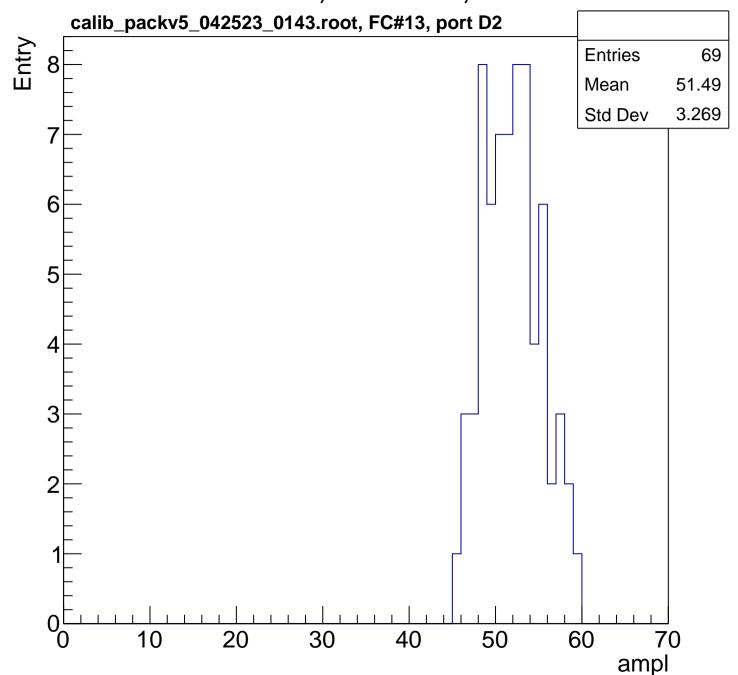


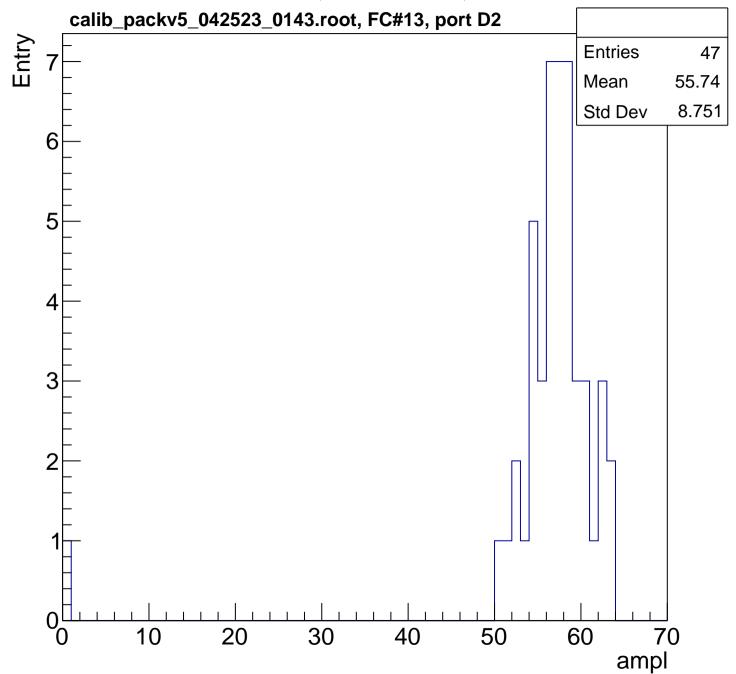


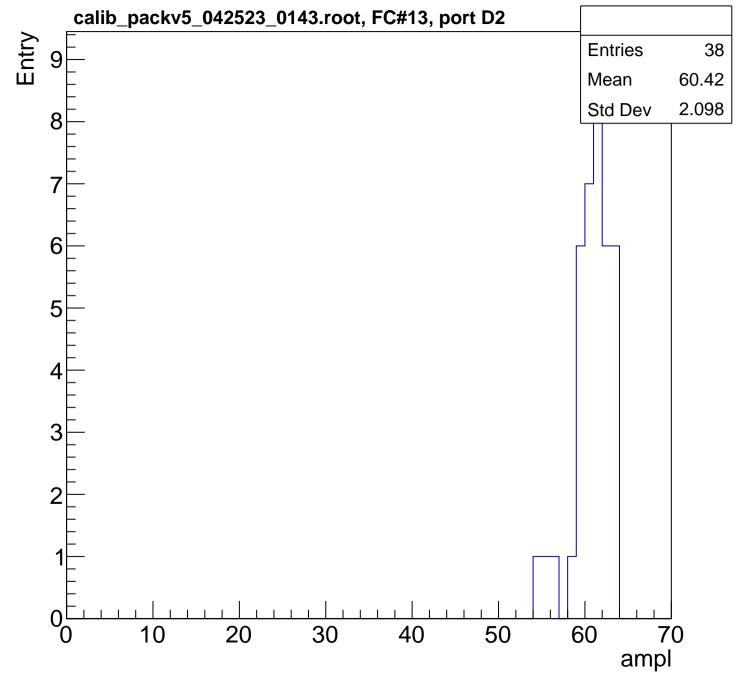


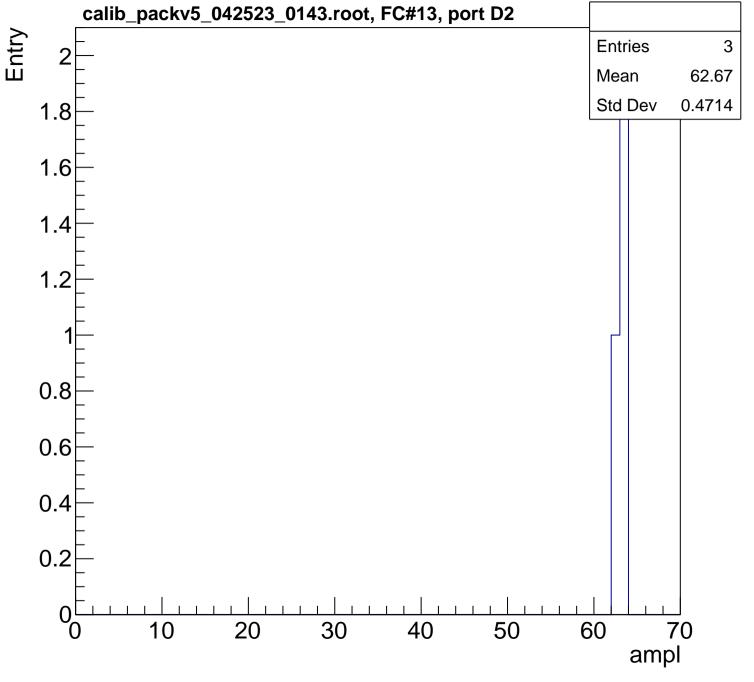




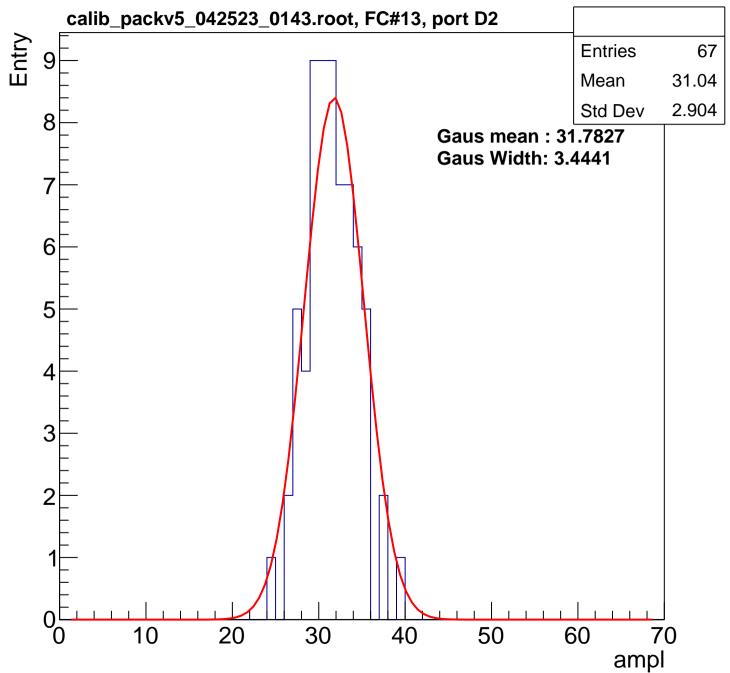


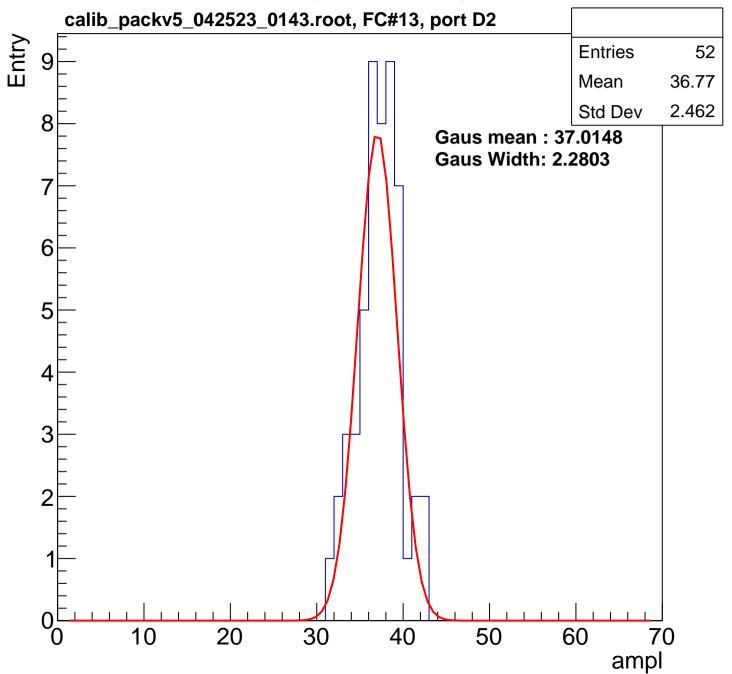


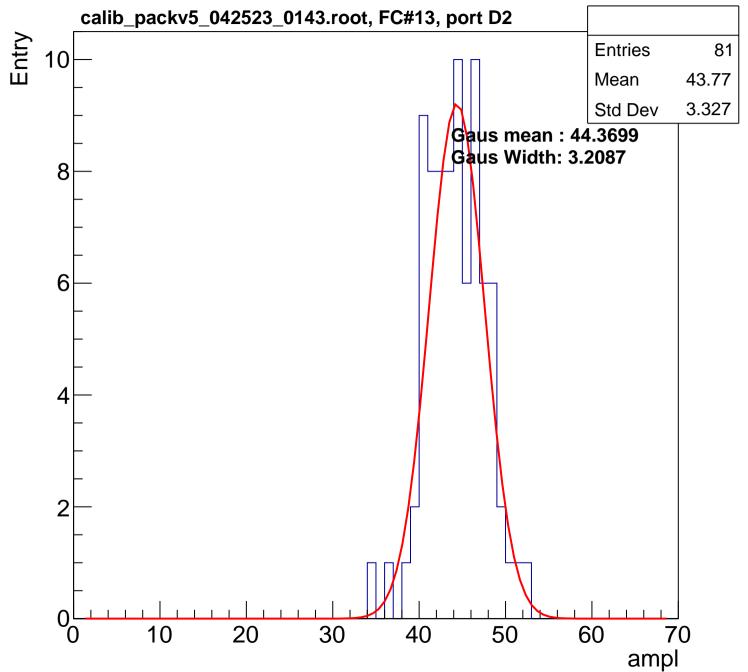


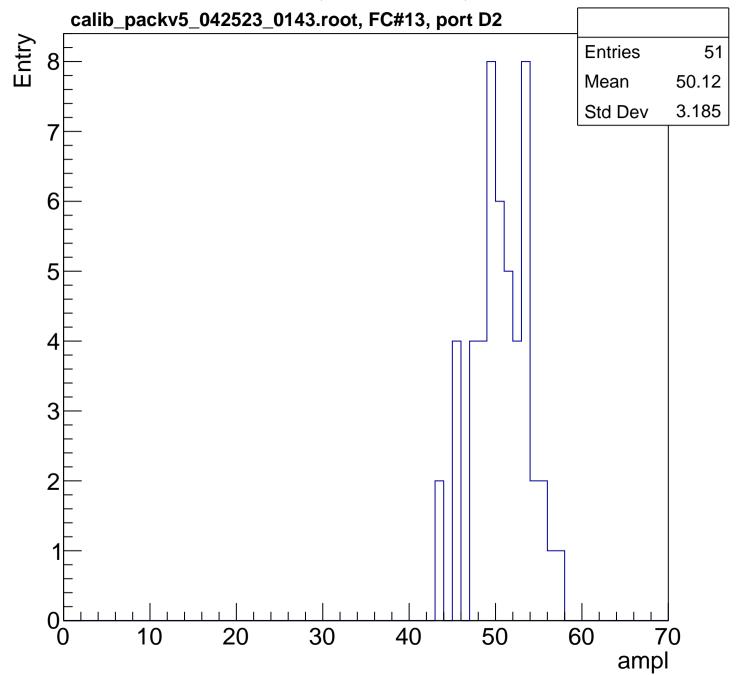


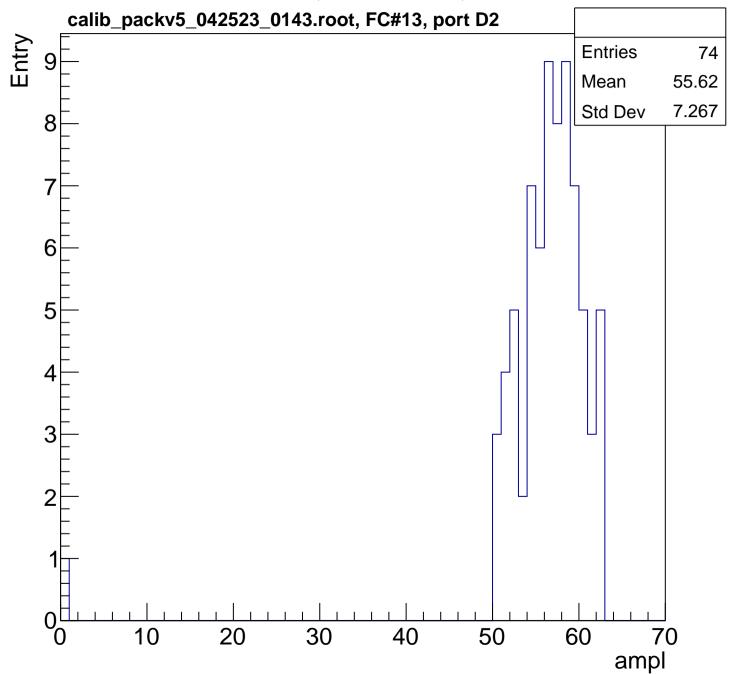


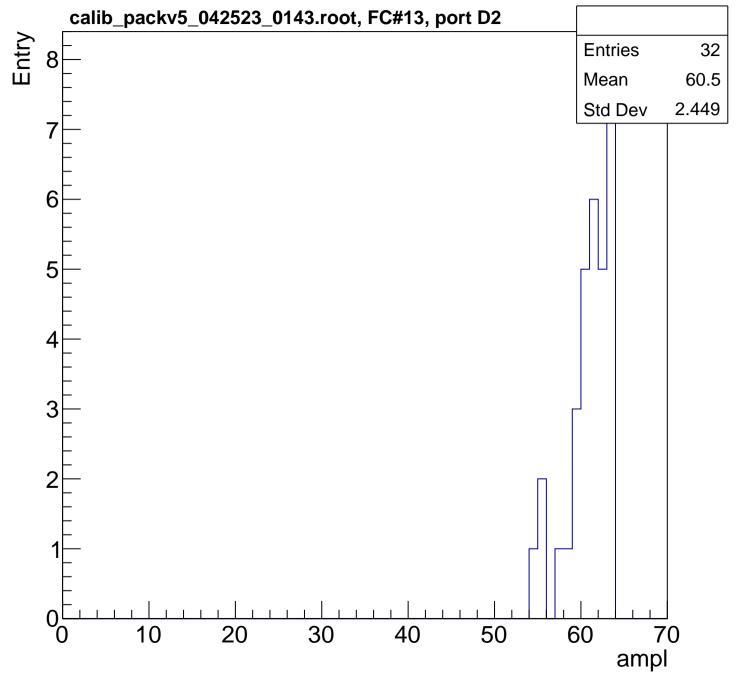


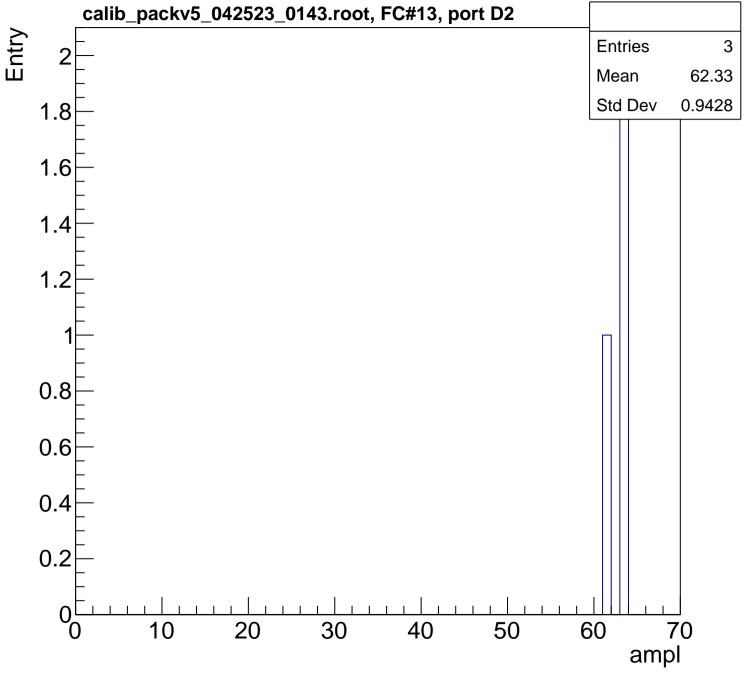




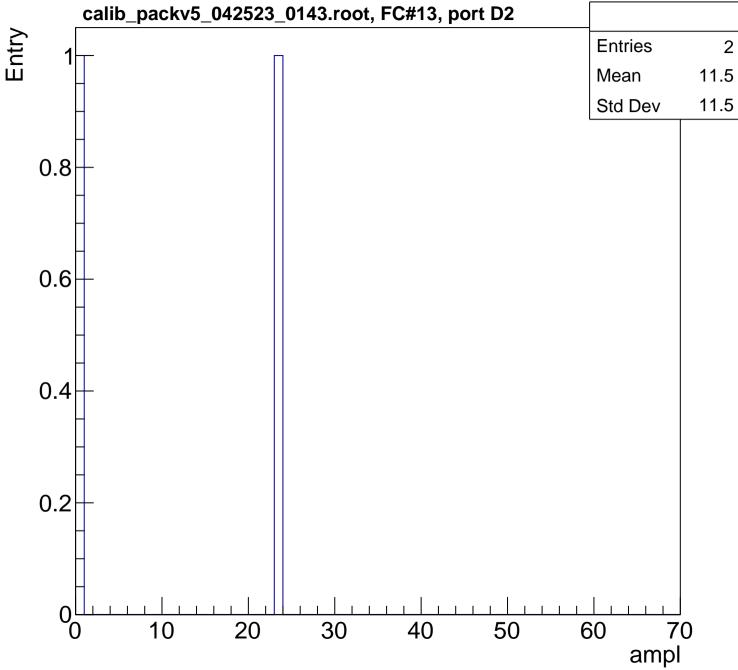


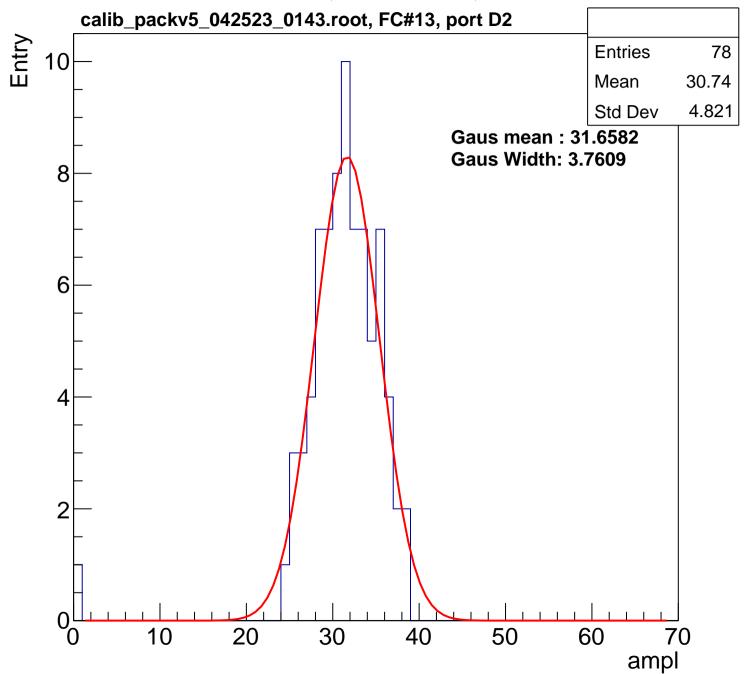


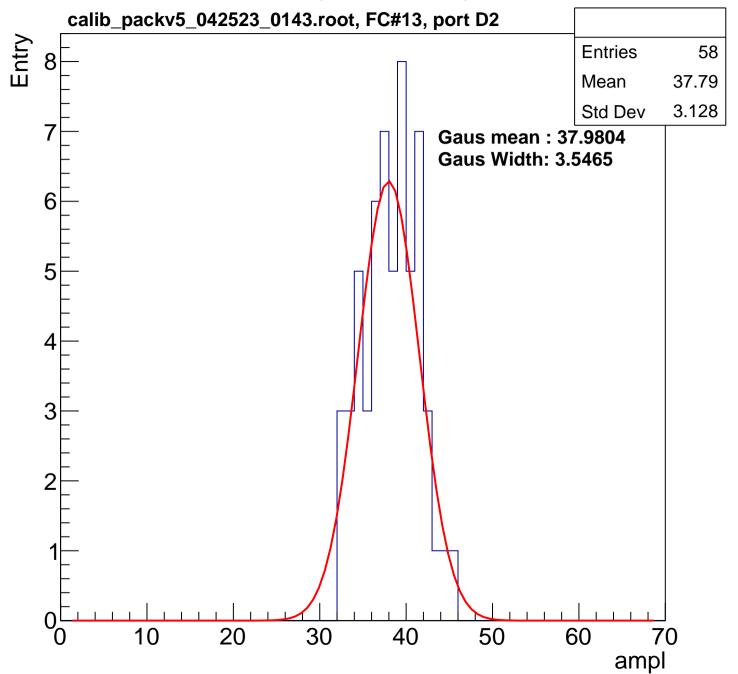


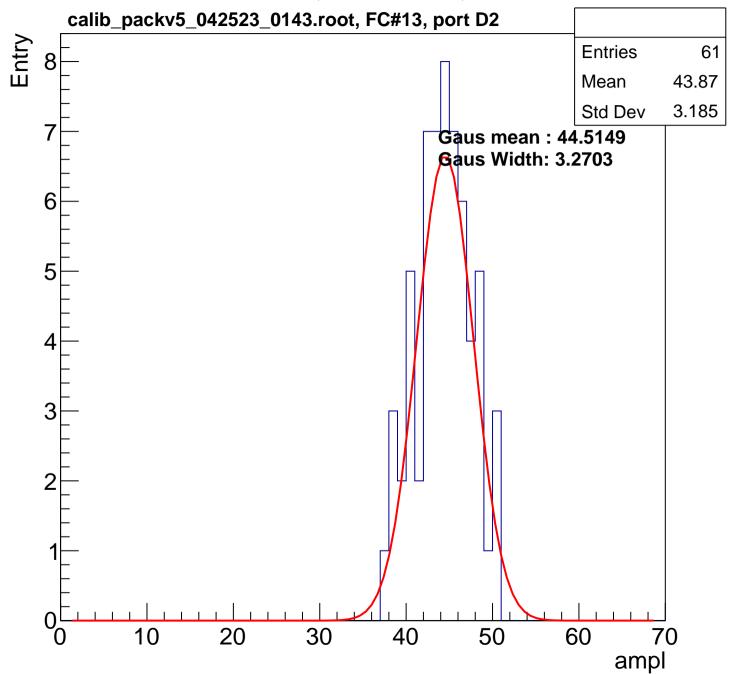


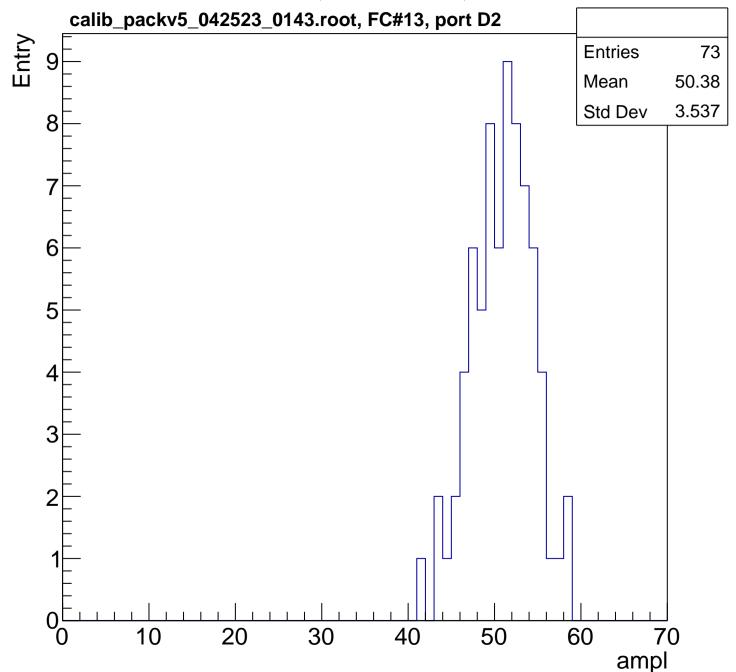
2

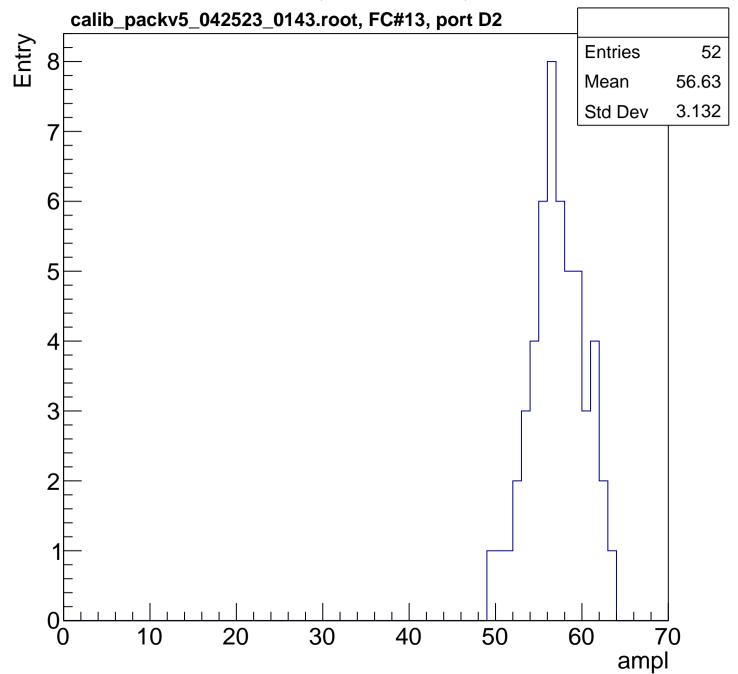


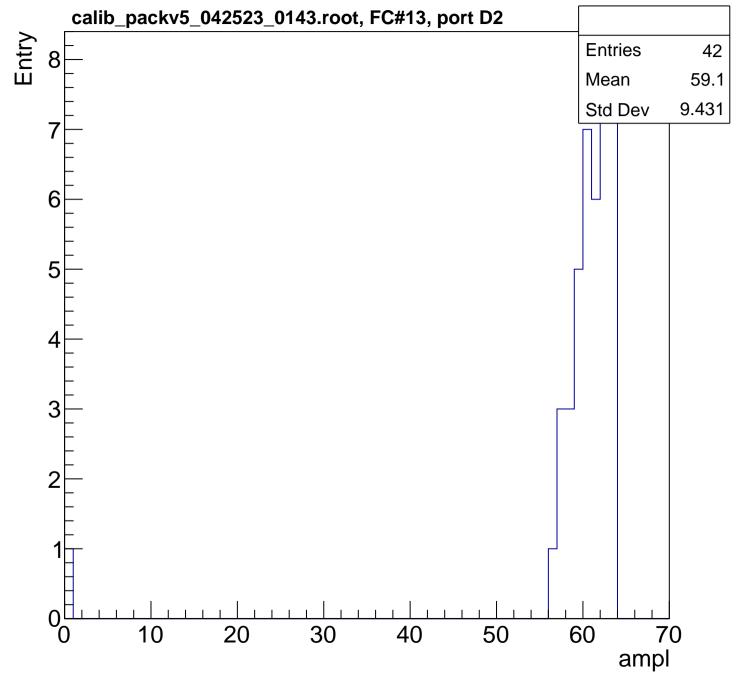


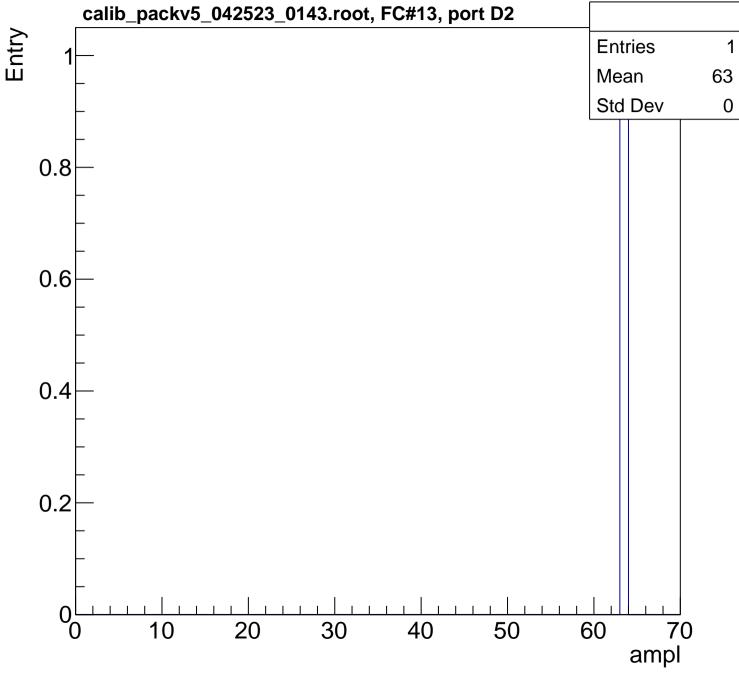




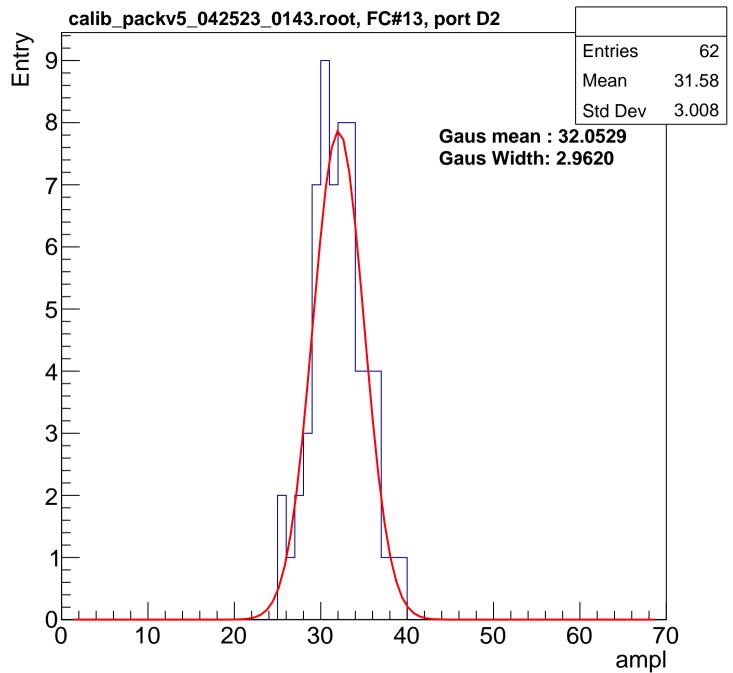


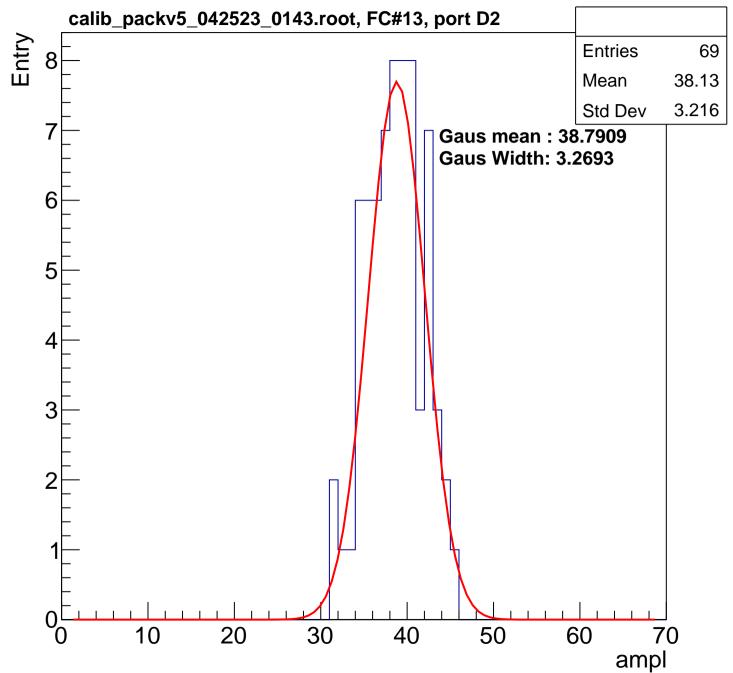


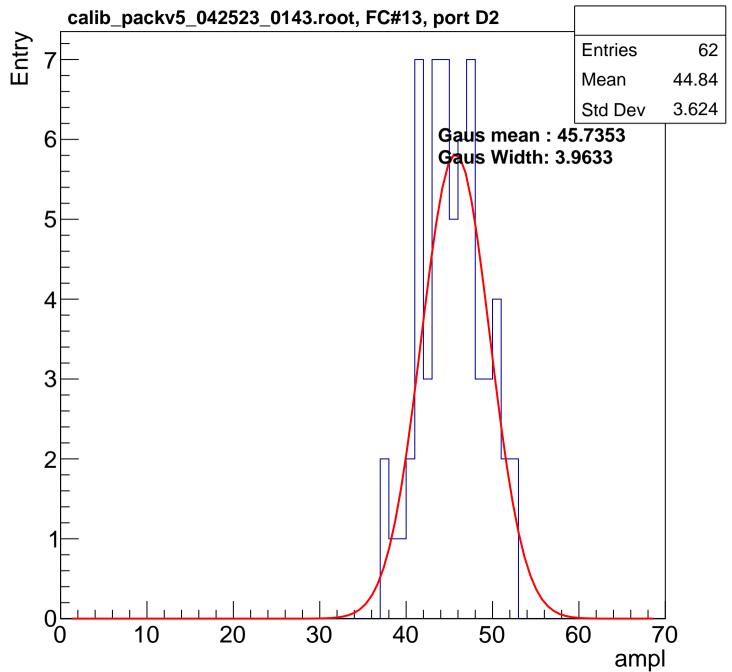


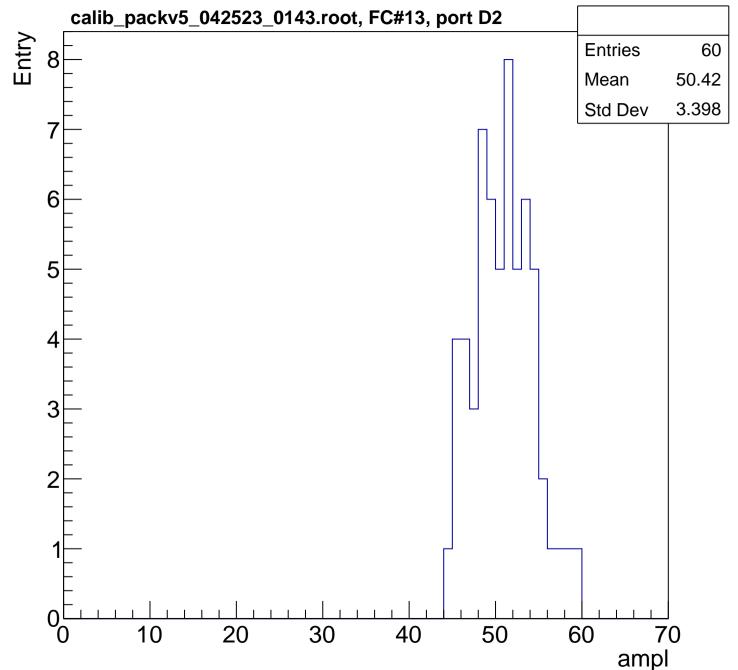


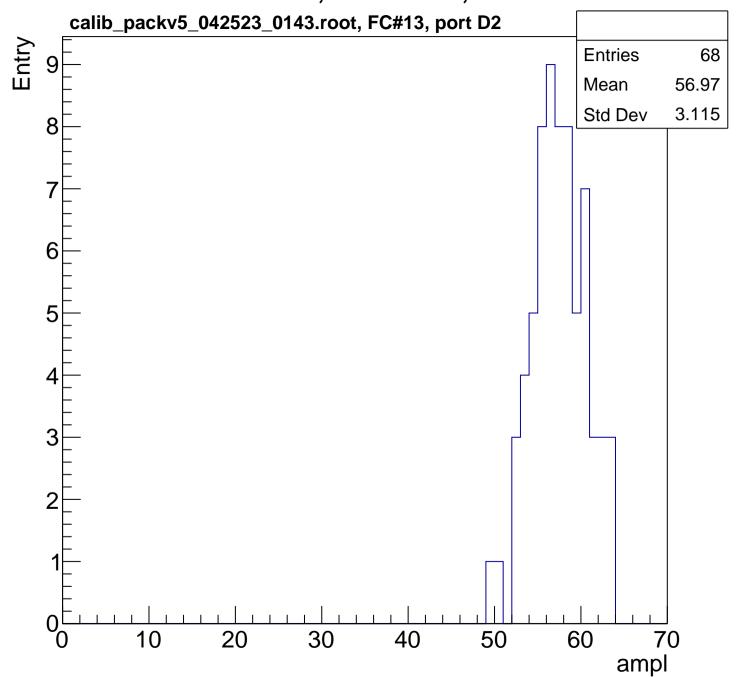
B1L003S, U8-ch37, adc7 calib\_packv5\_042523\_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

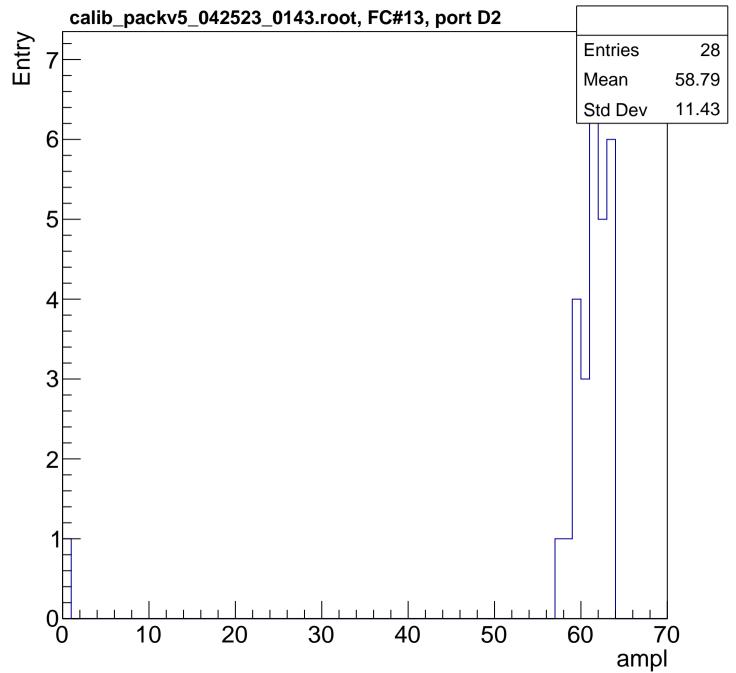


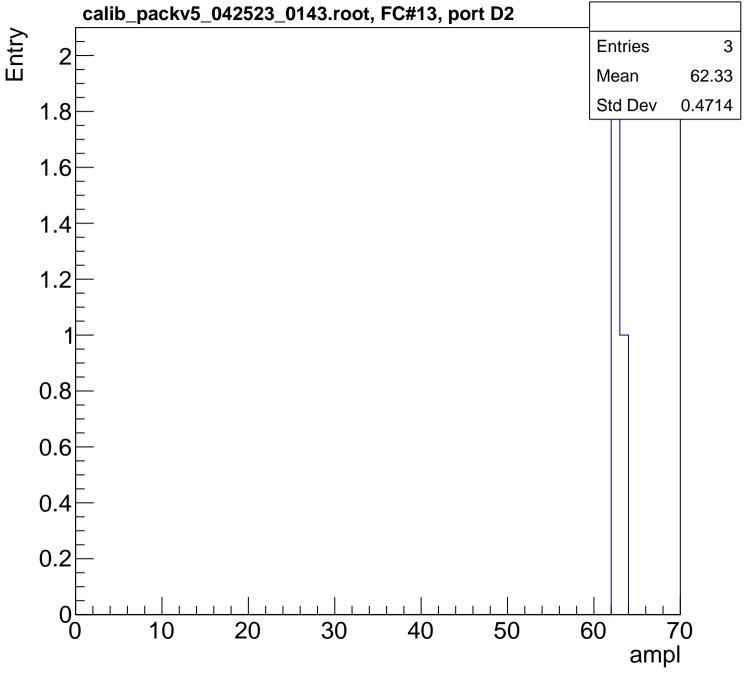


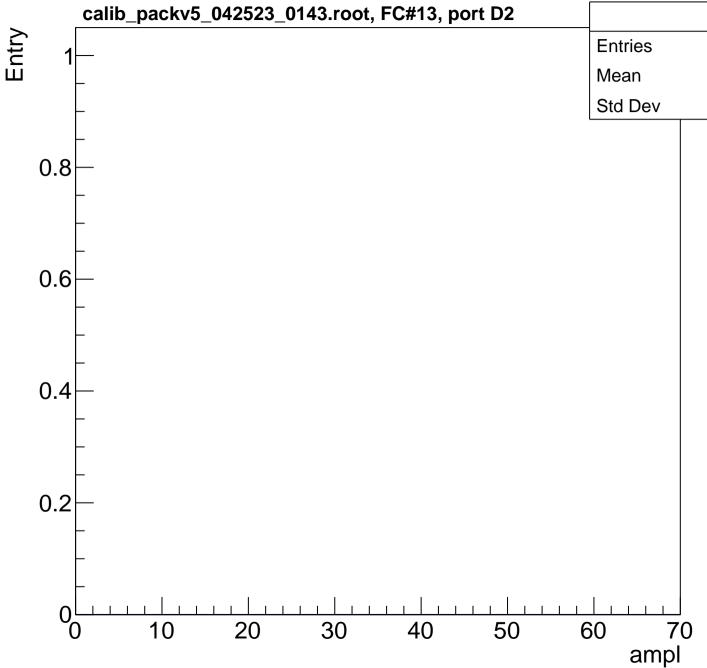


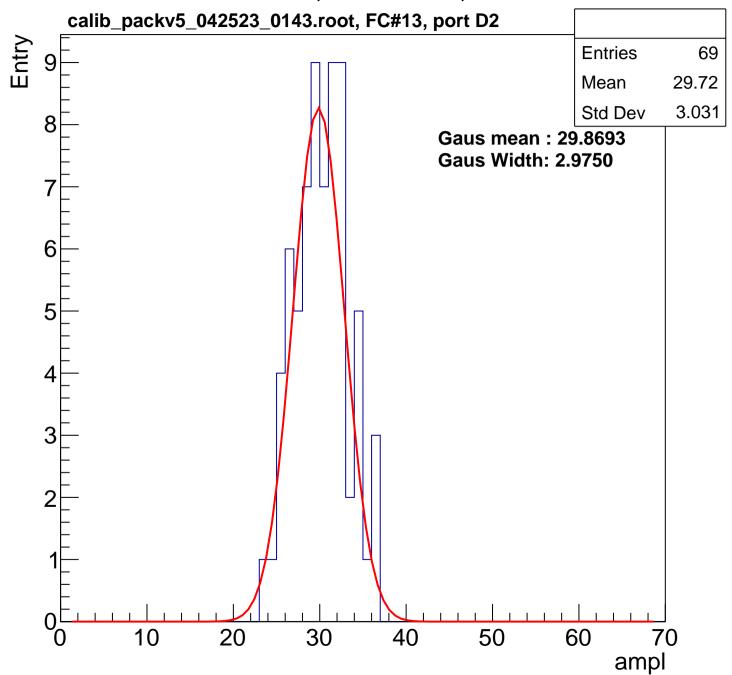


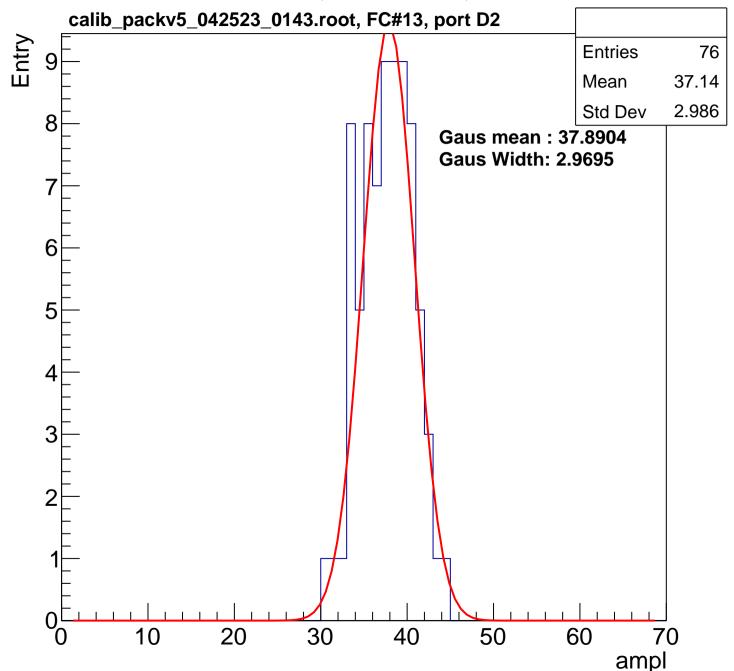


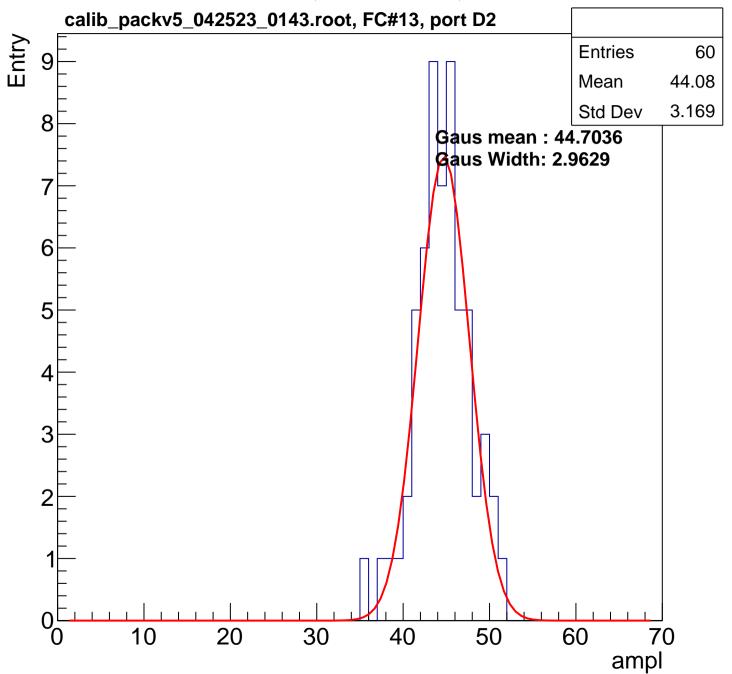


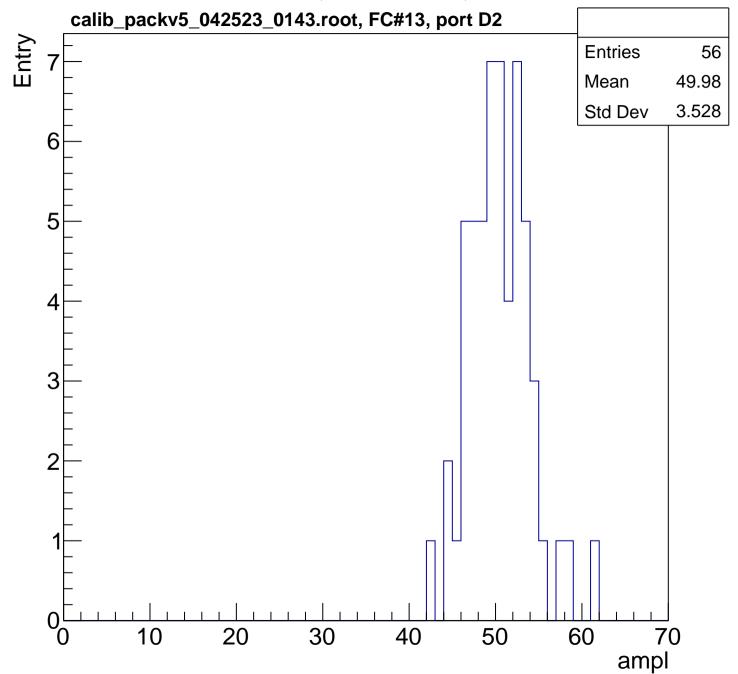


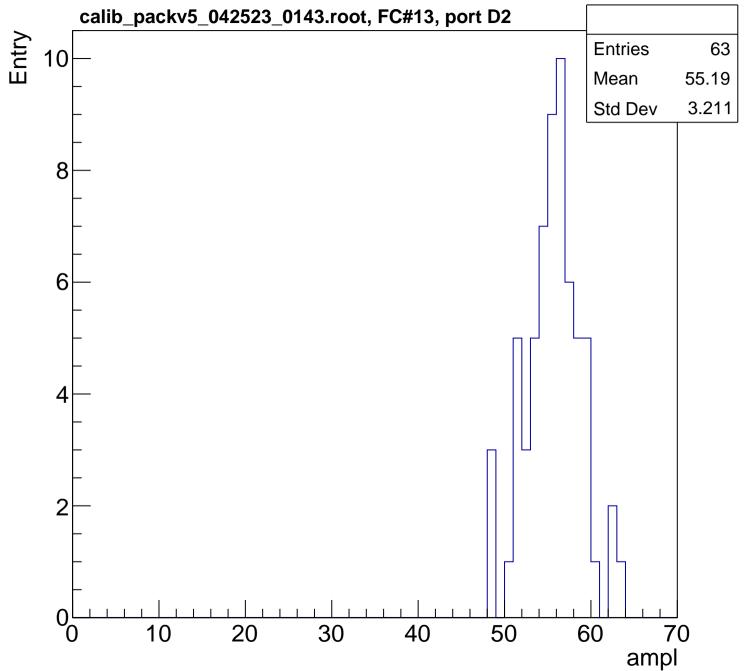


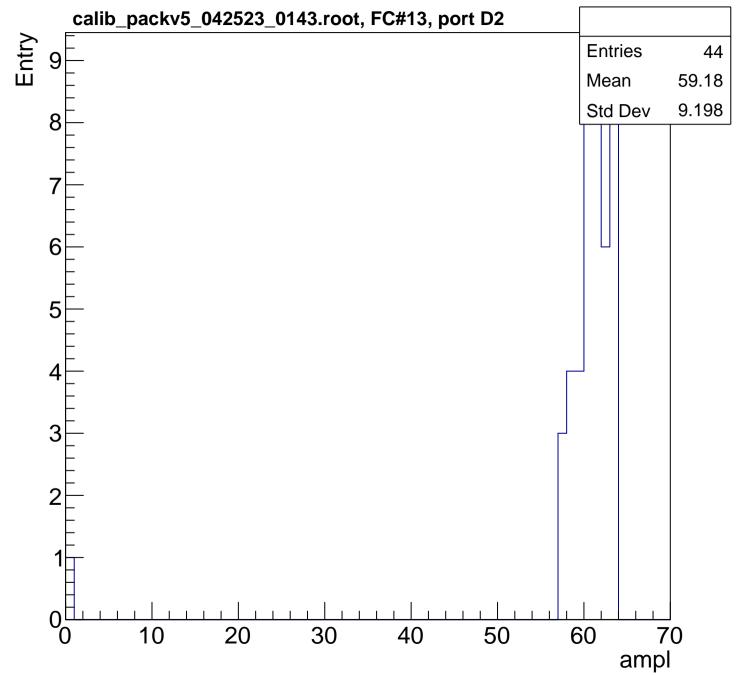


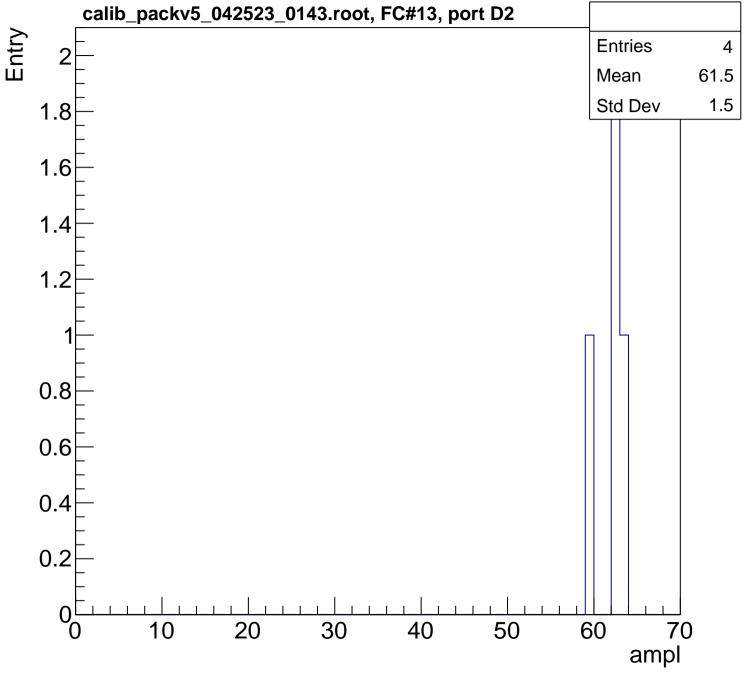


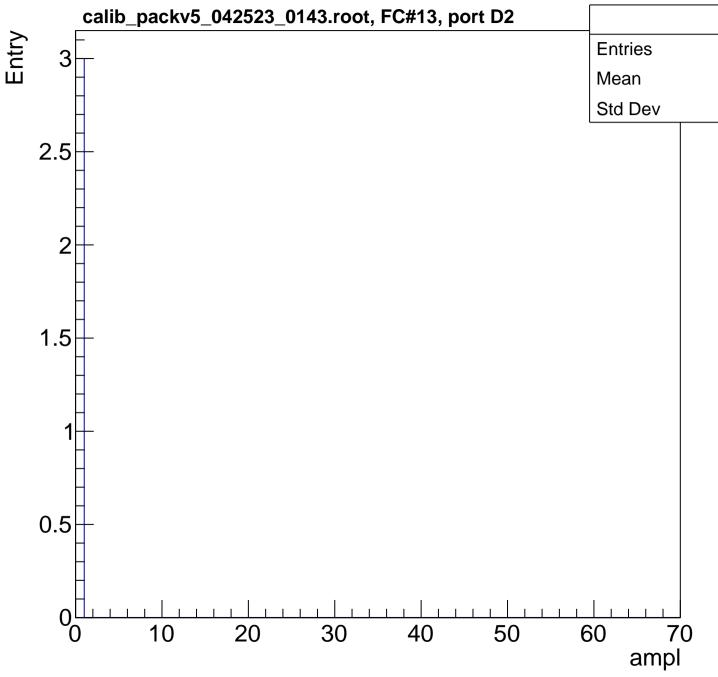


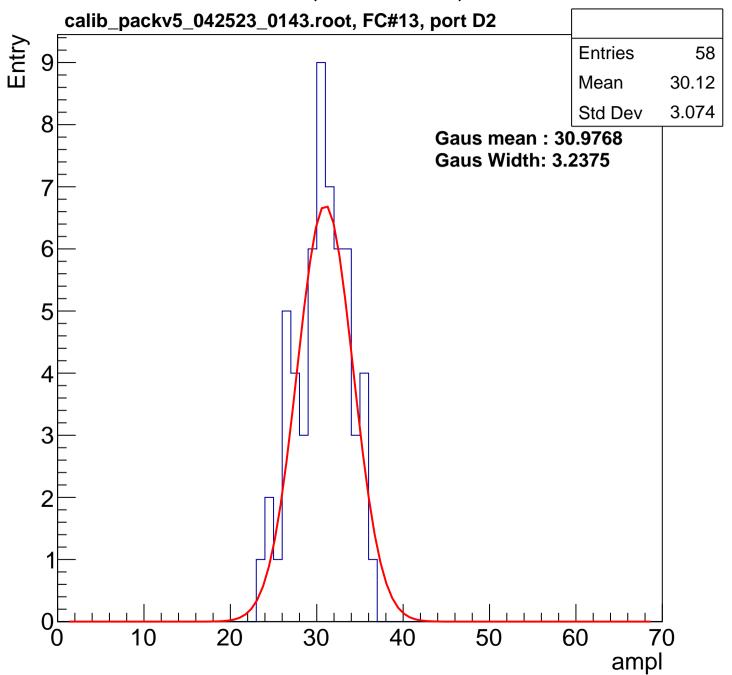


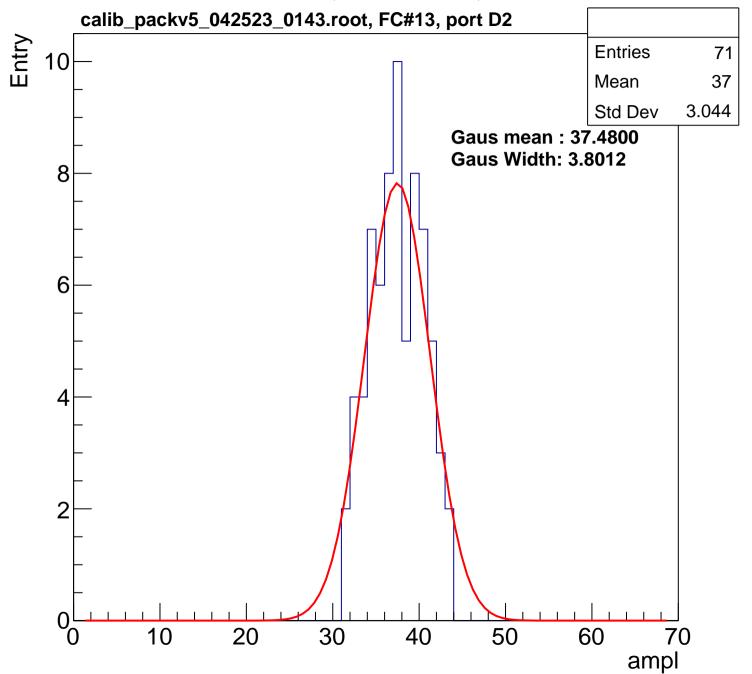


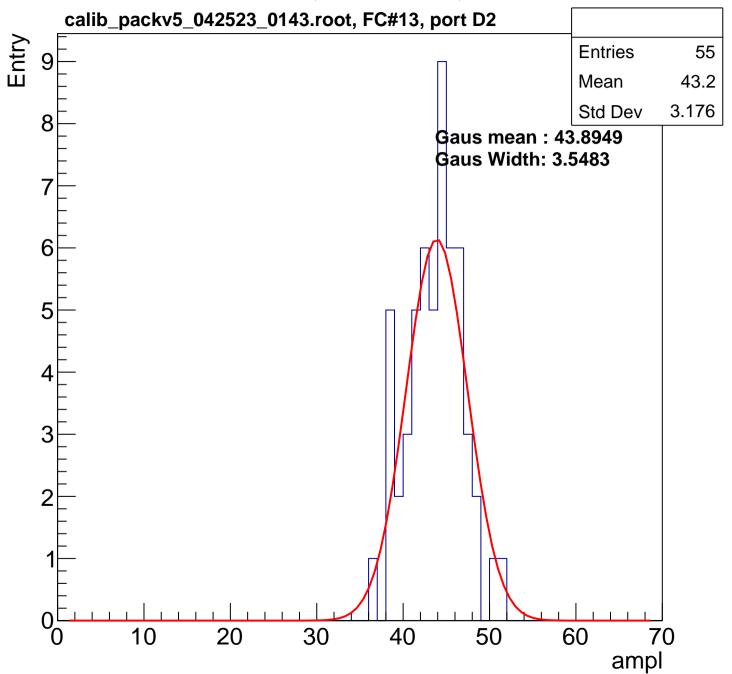


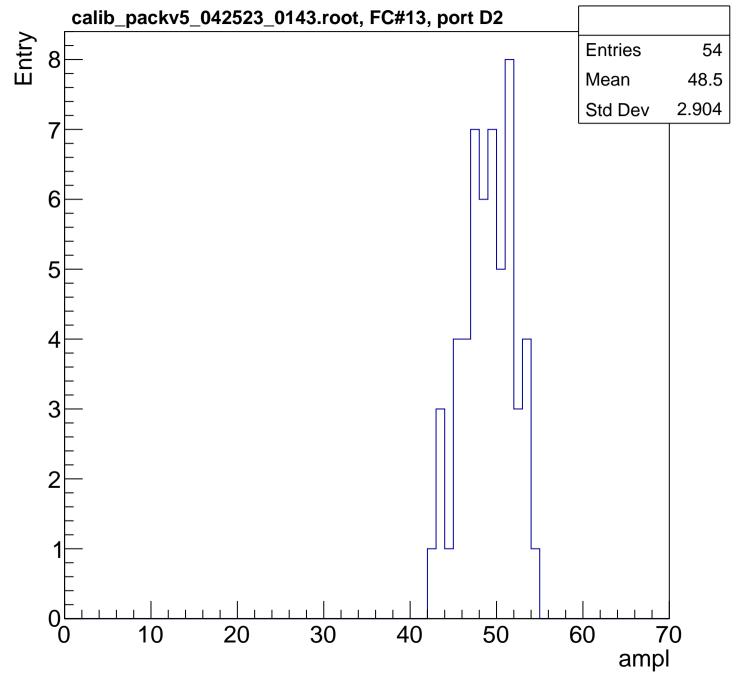


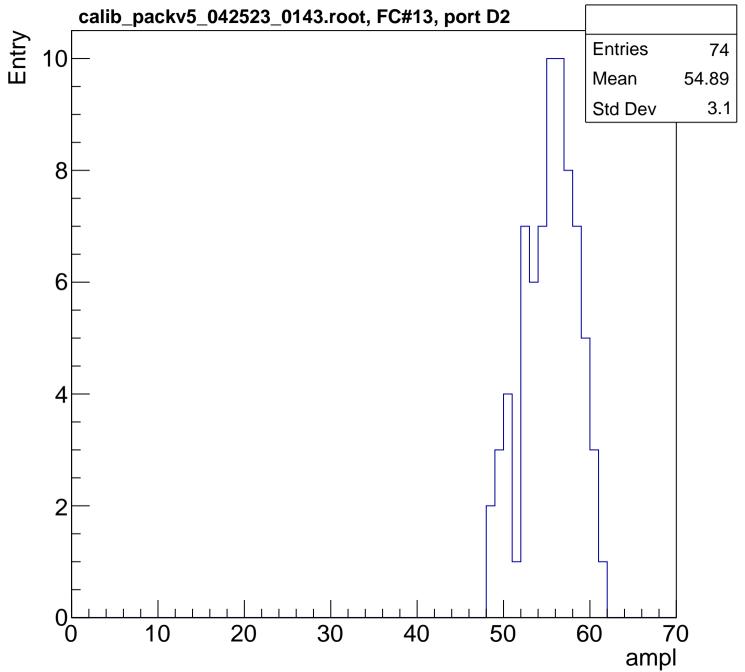


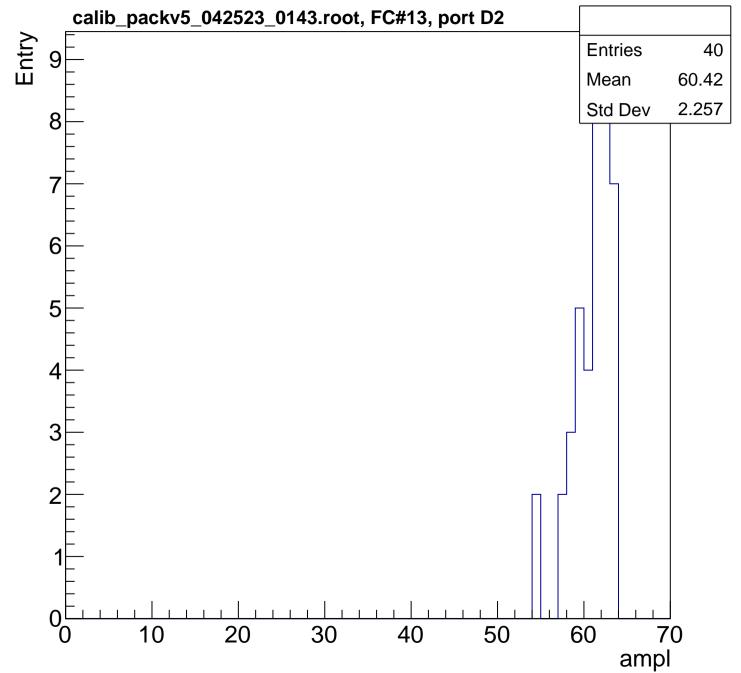


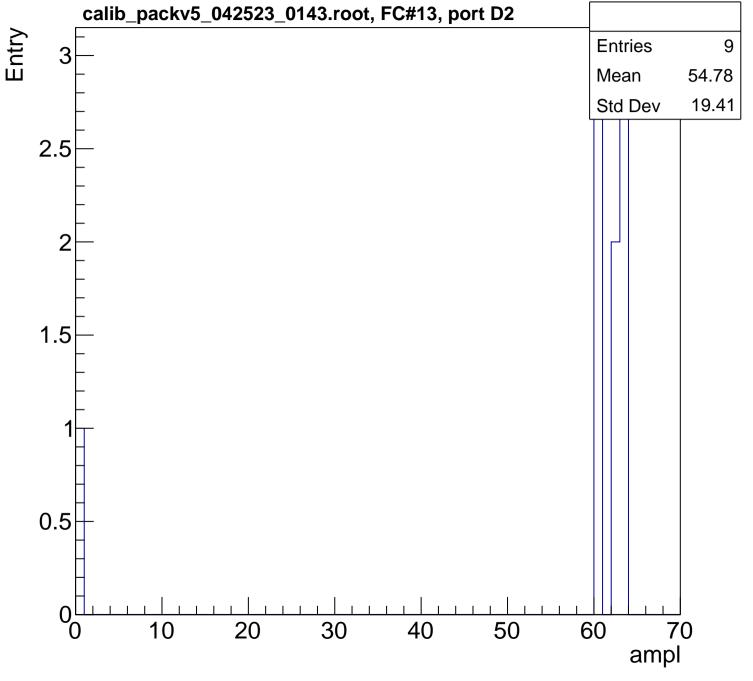




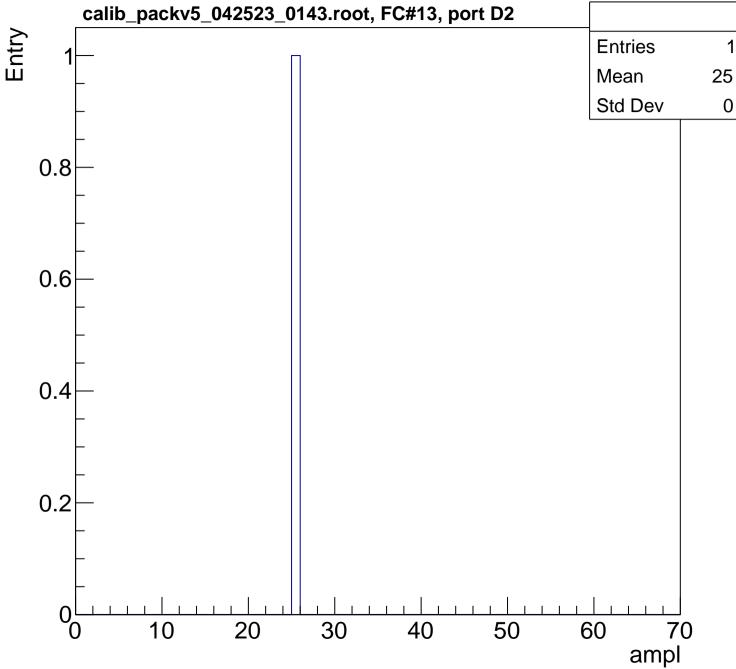


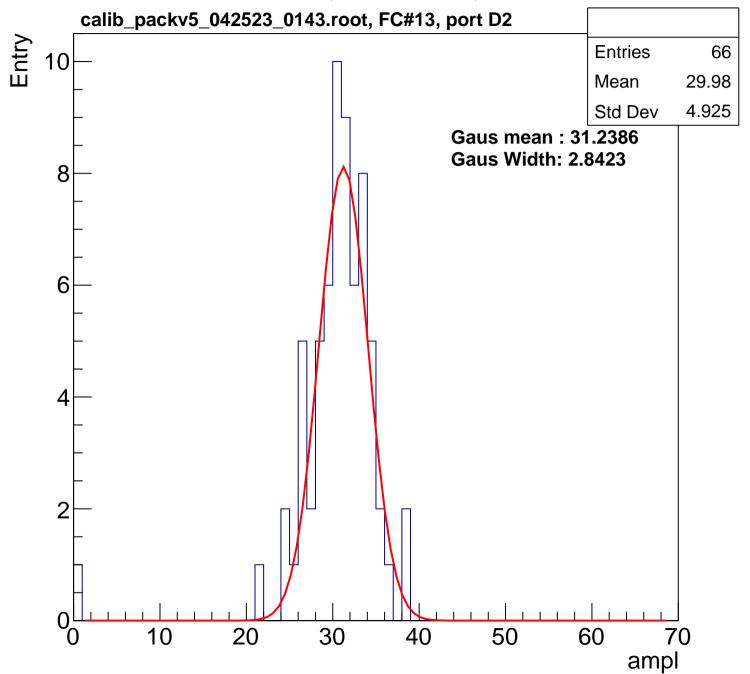


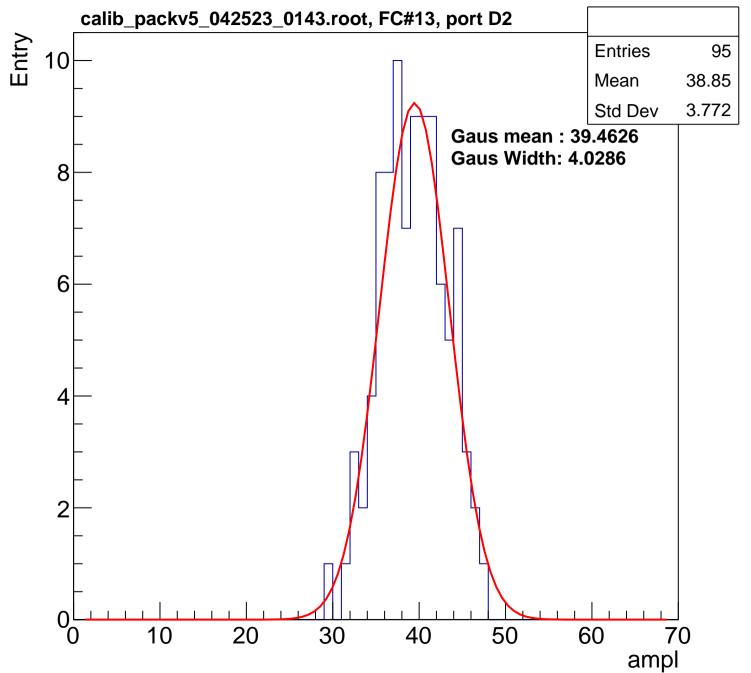


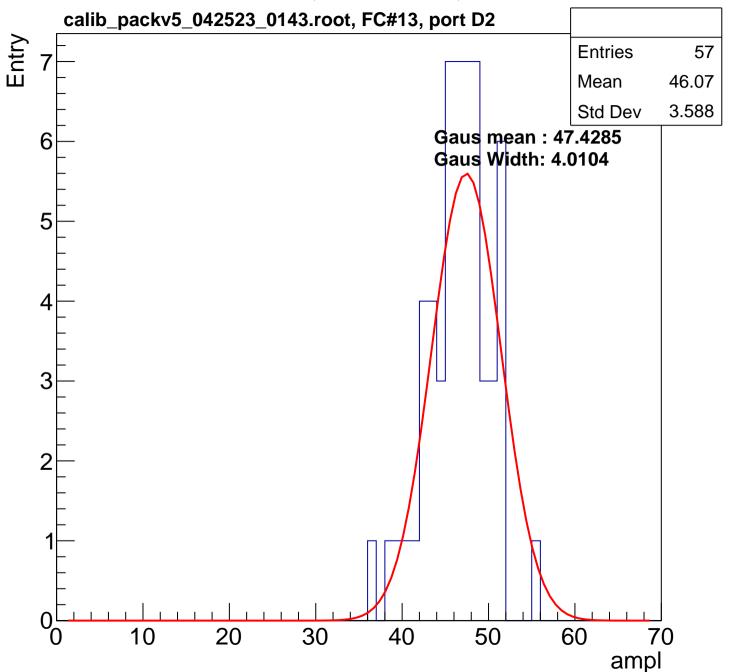


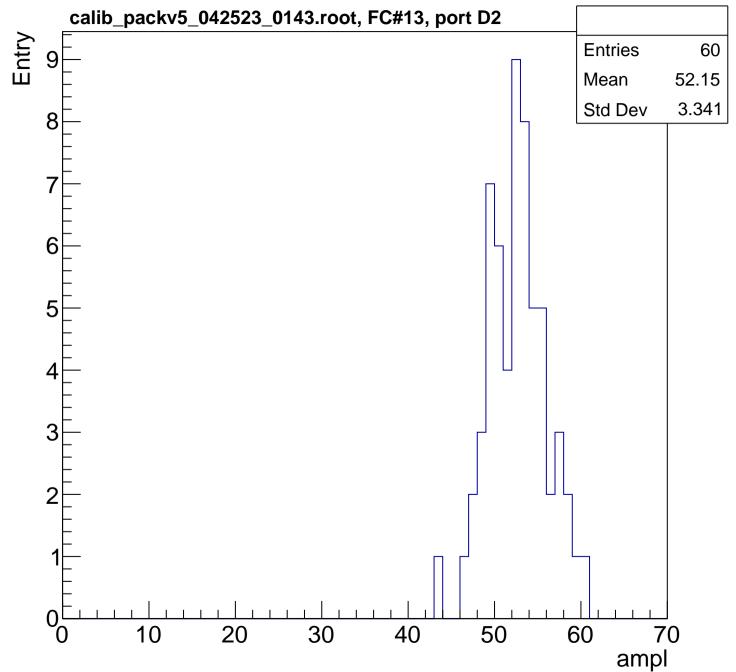
0

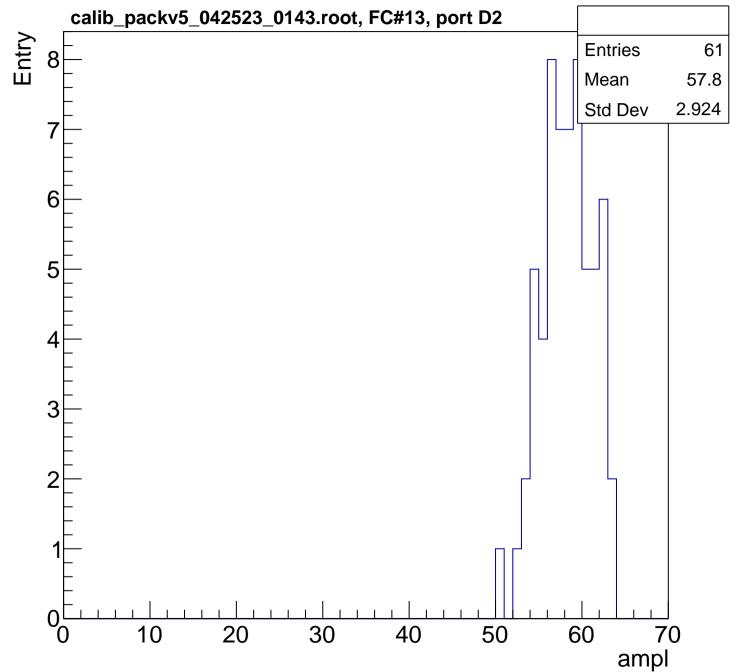


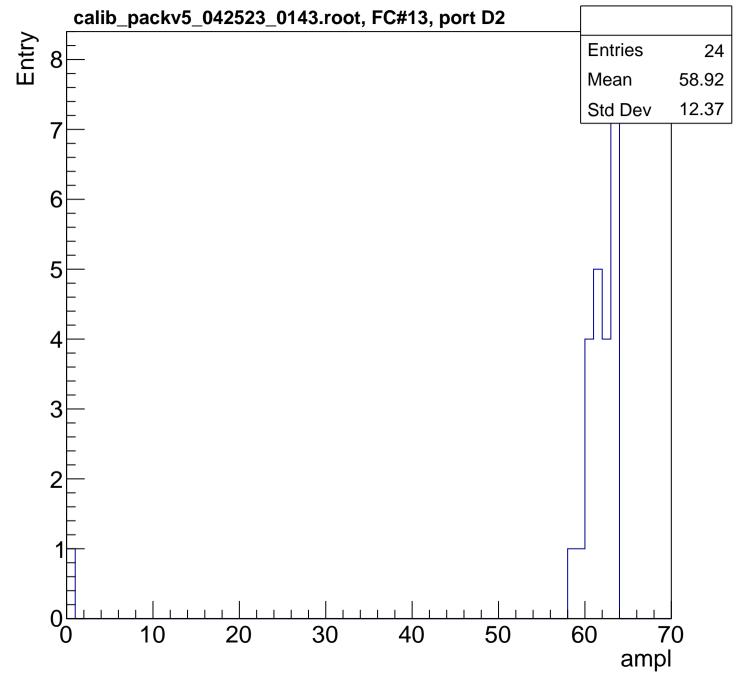


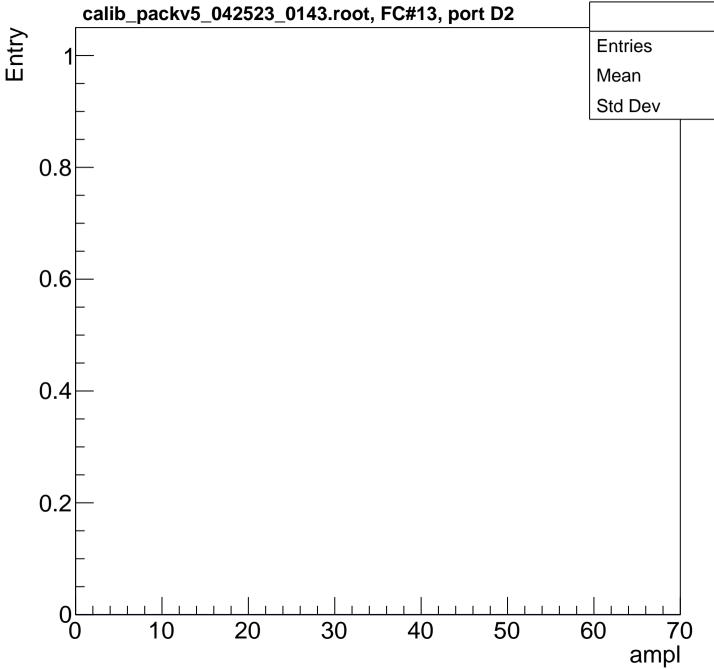


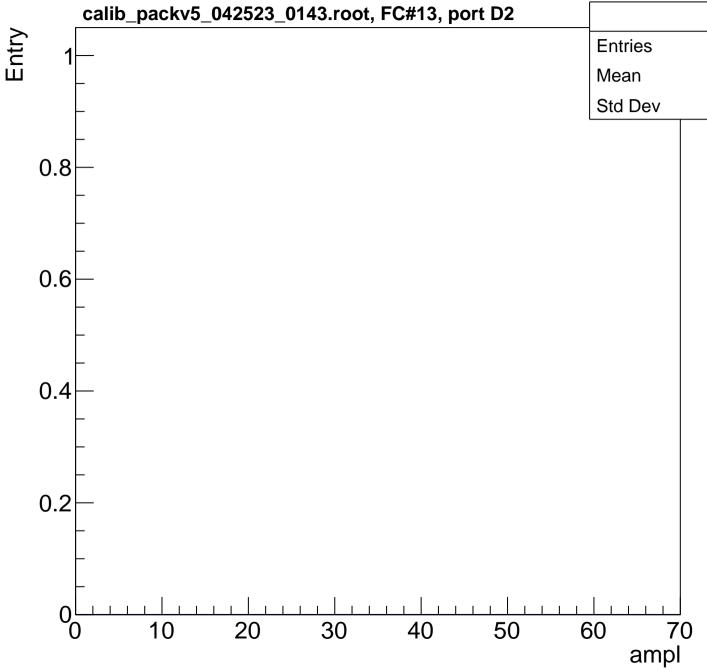


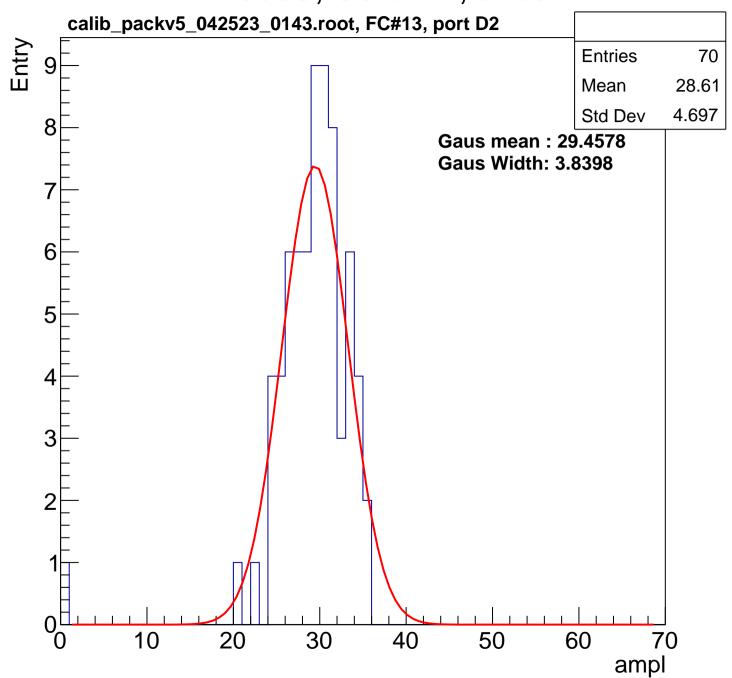


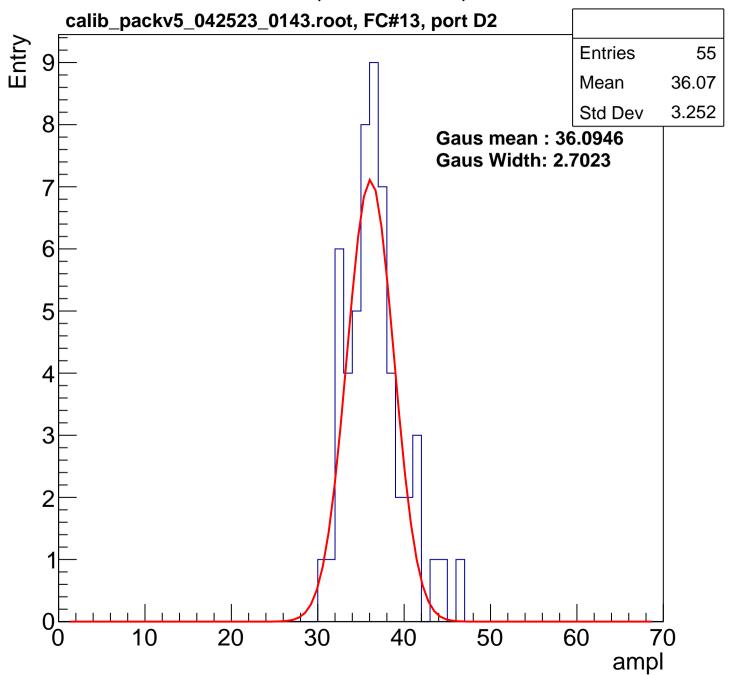


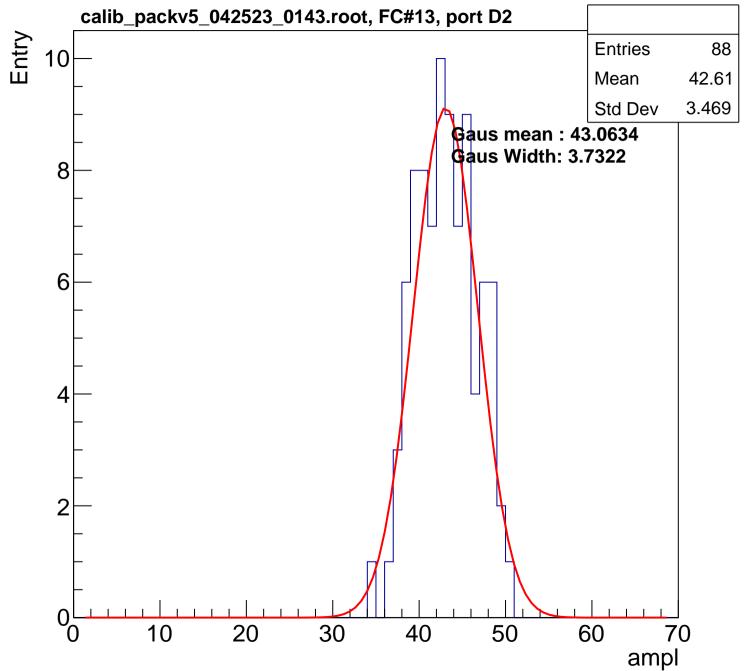


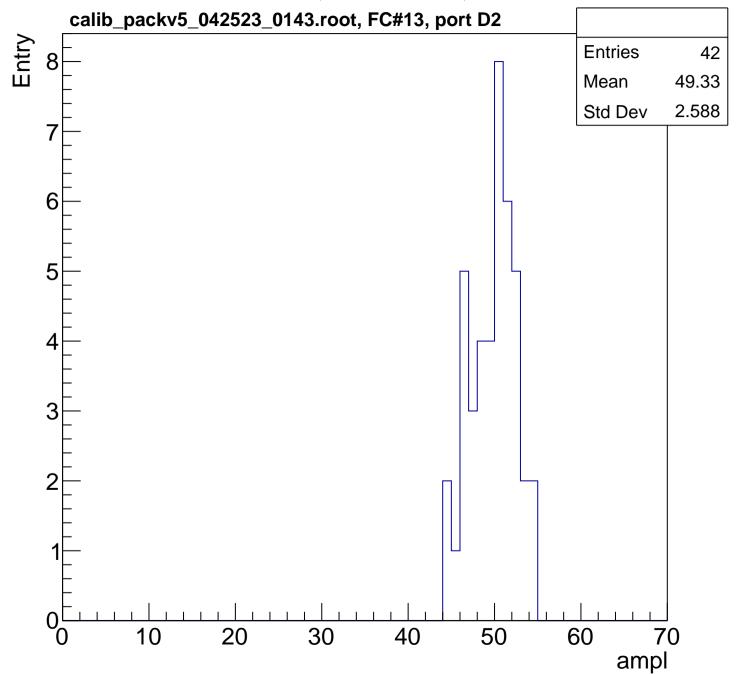


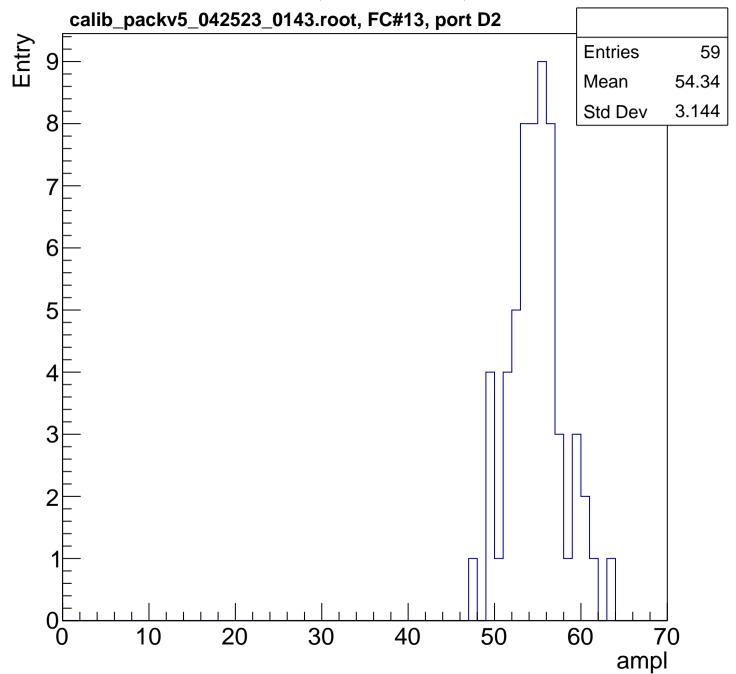


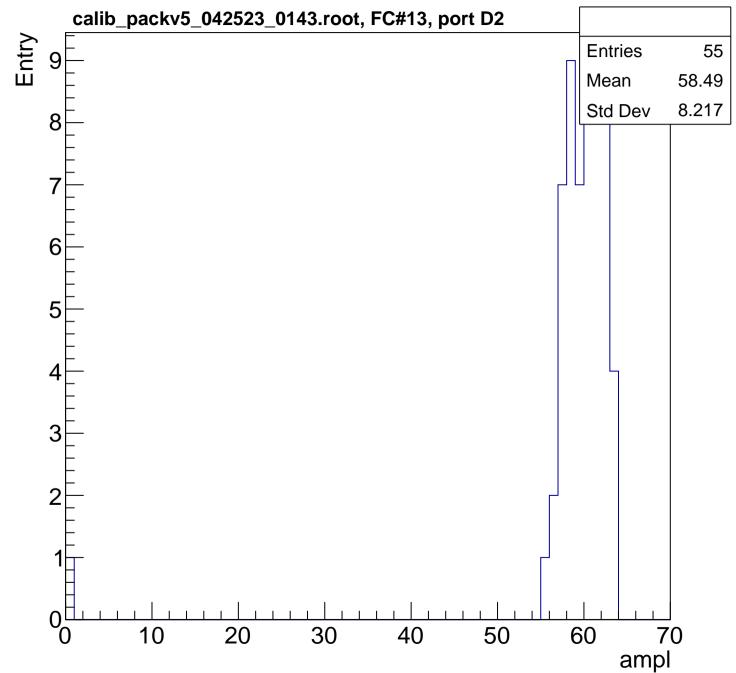


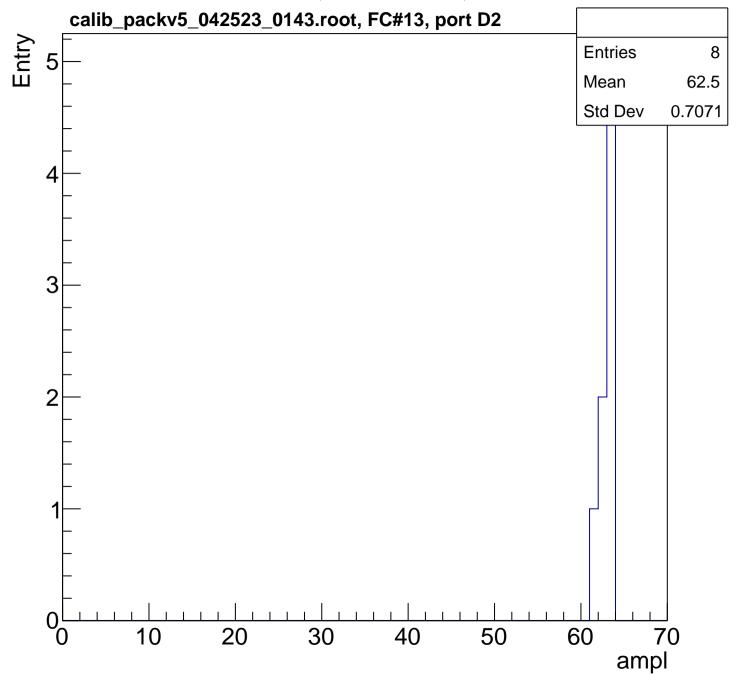




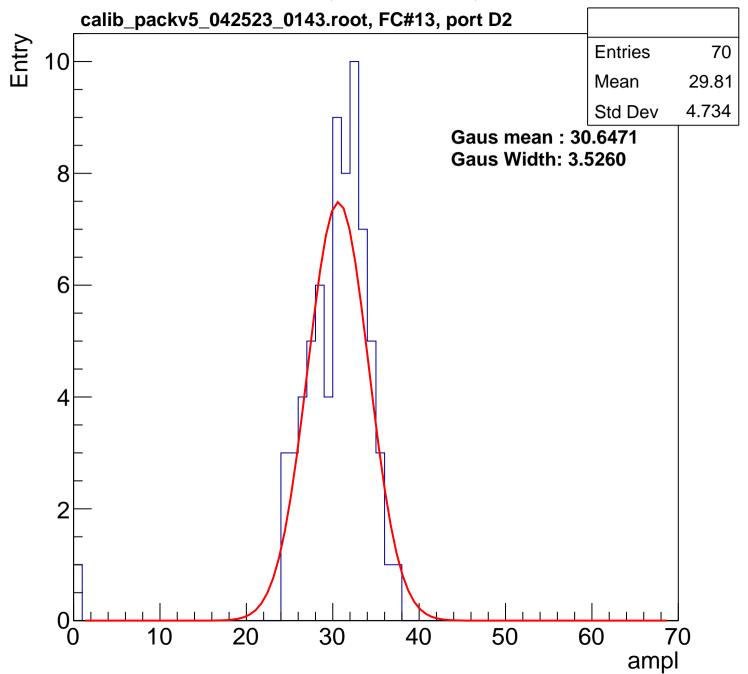


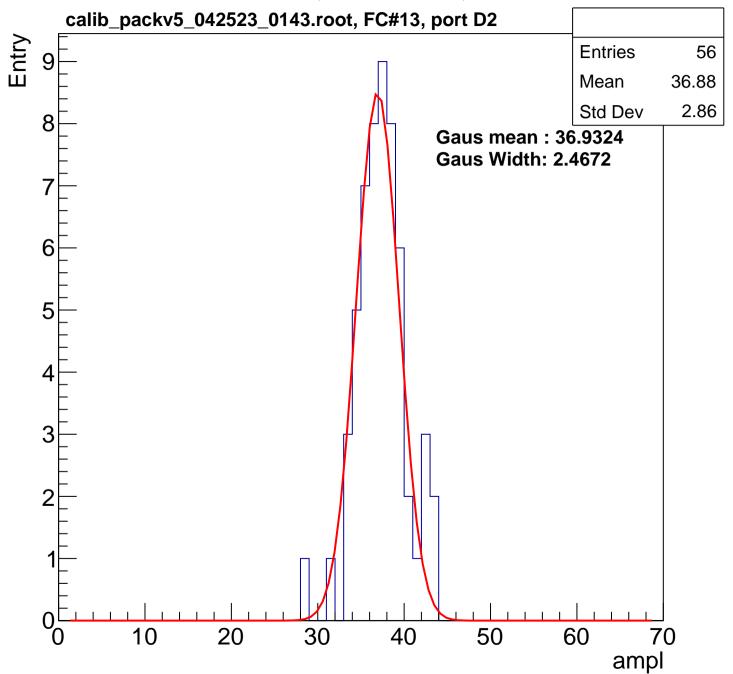


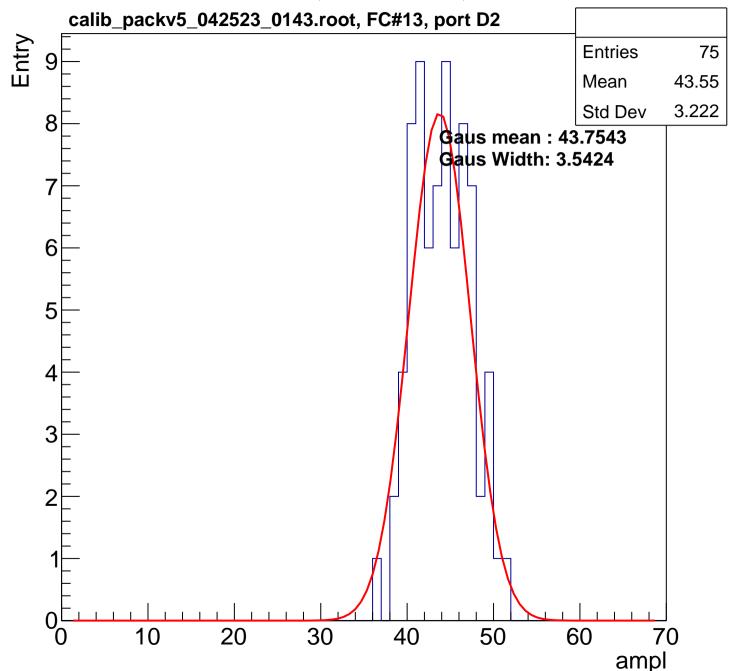


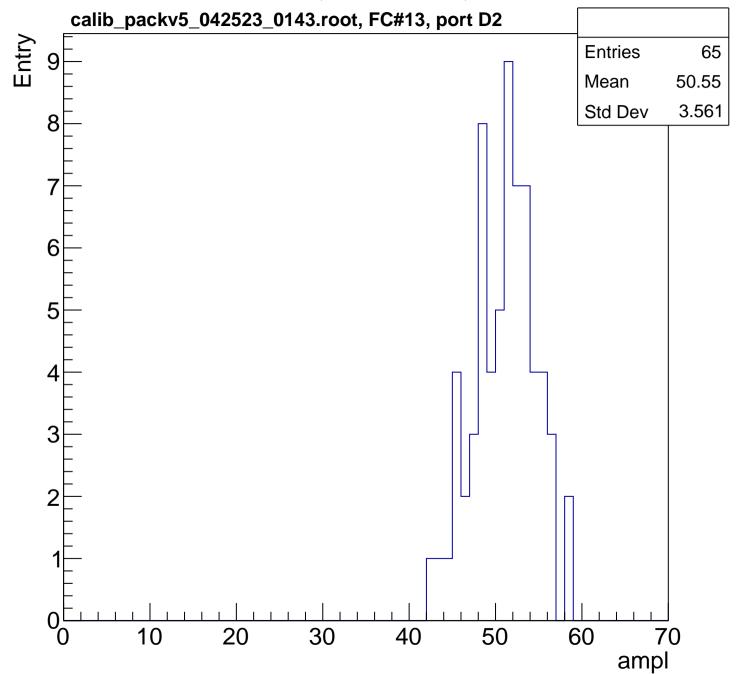


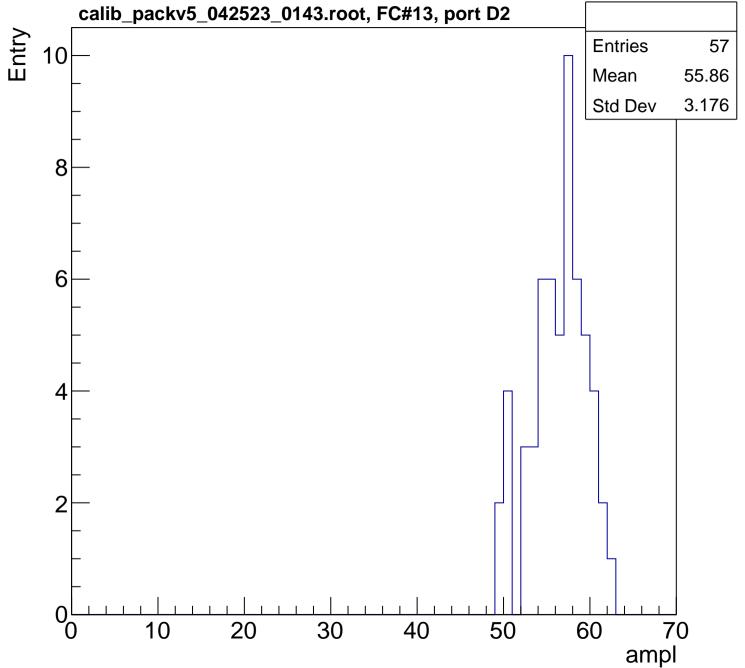
B1L003S, U8-ch42, adc7 calib\_packv5\_042523\_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

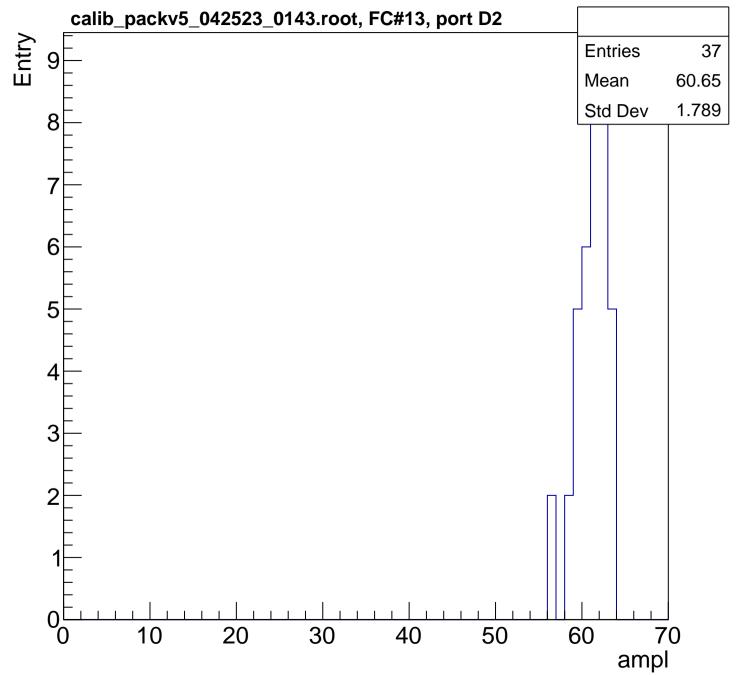


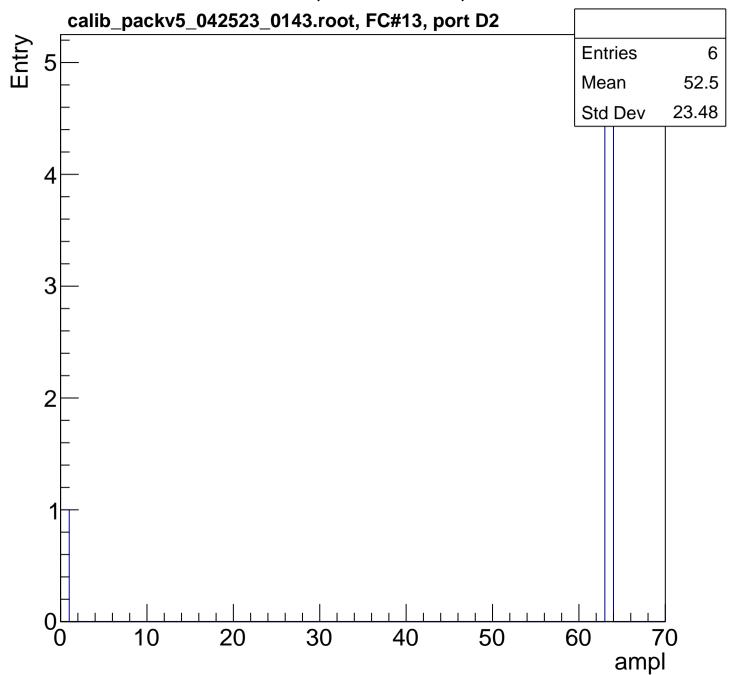












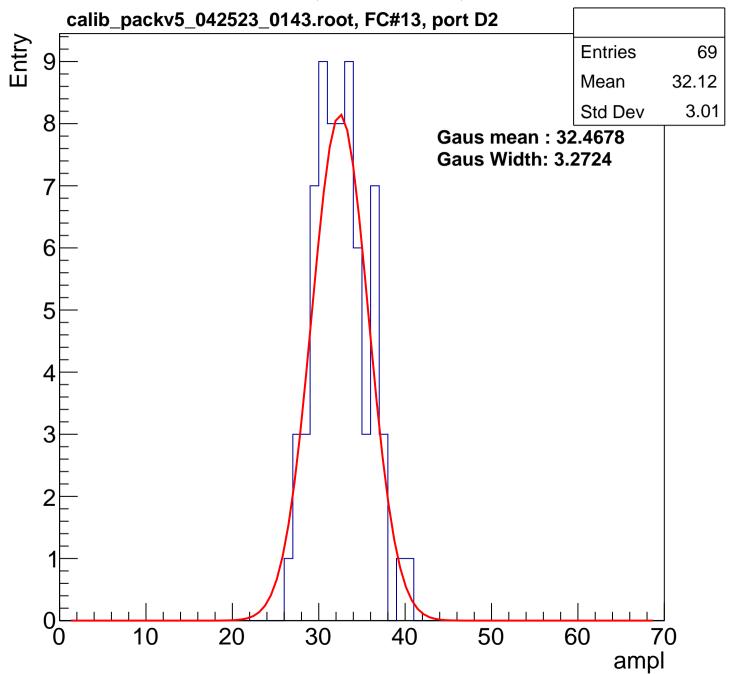
#### B1L003S, U8-ch43, adc7 5\_042523\_0143.root, FC#13, port D2

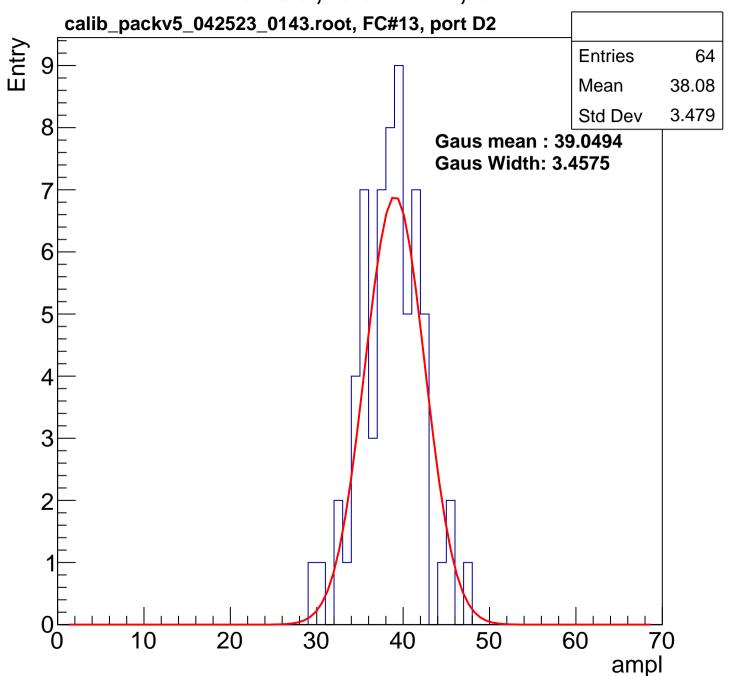
0

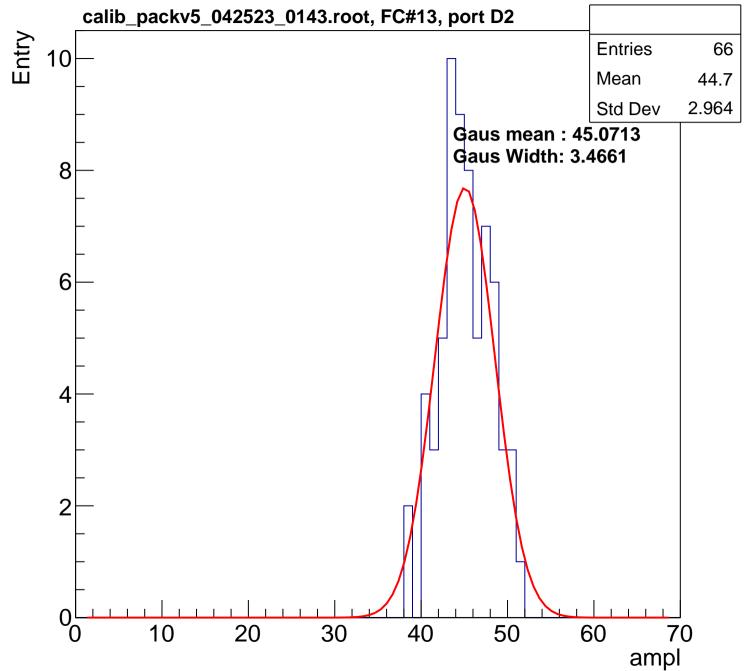
0

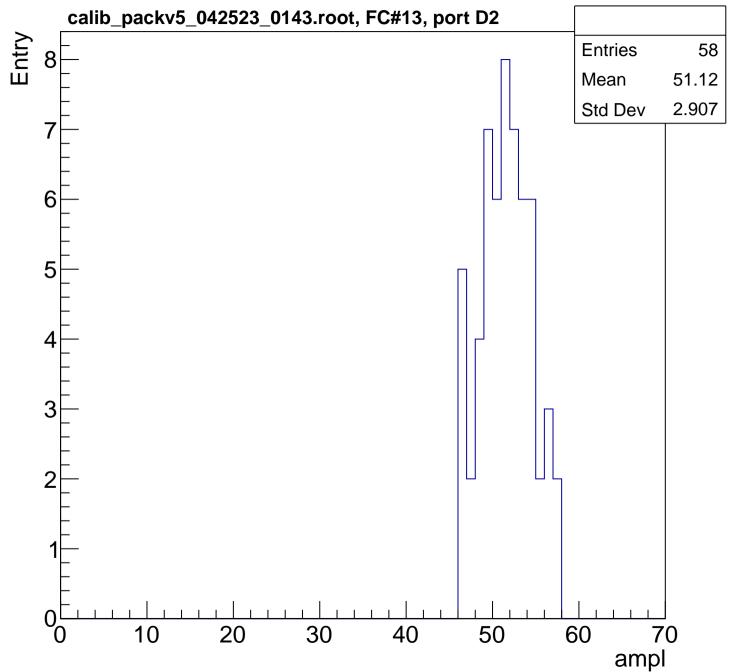
0

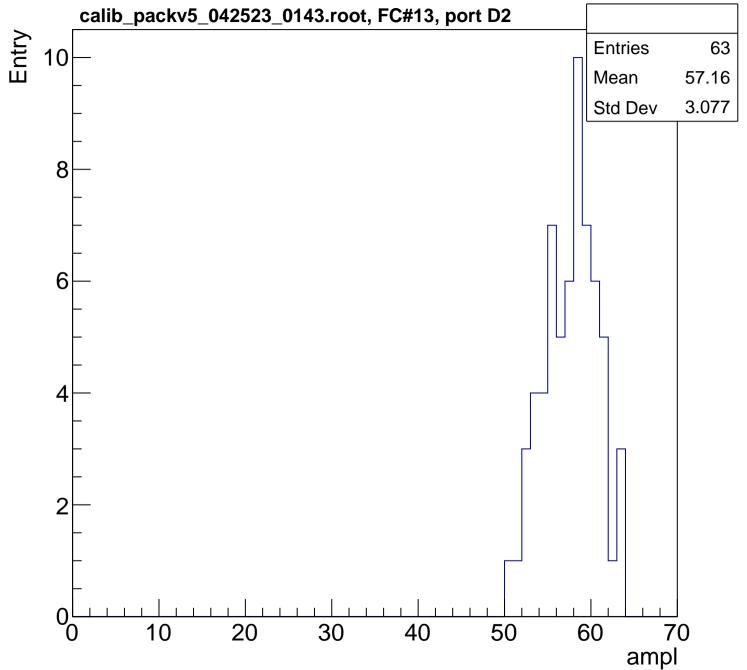


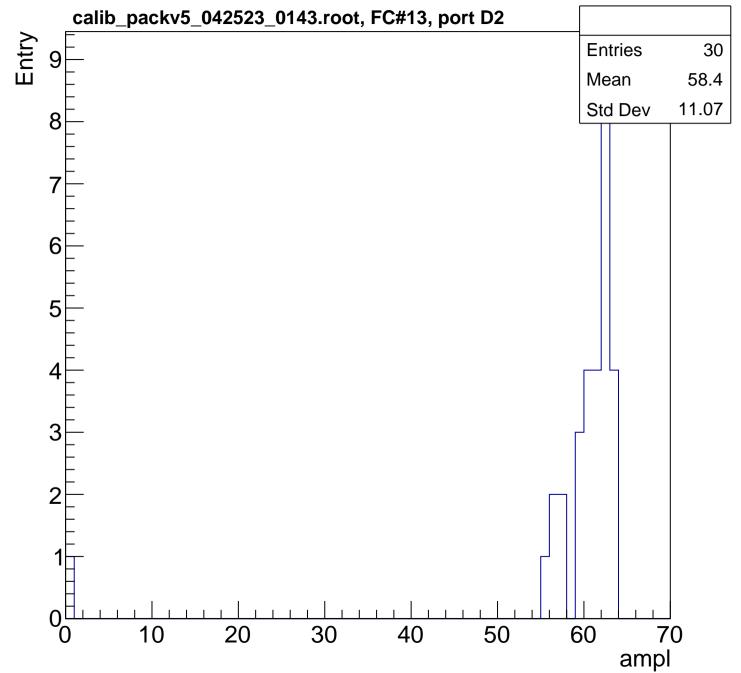


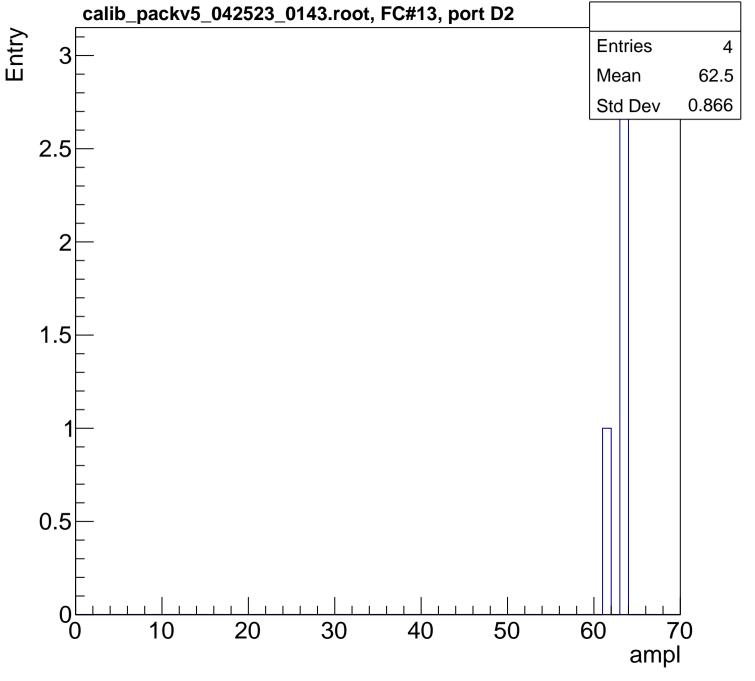


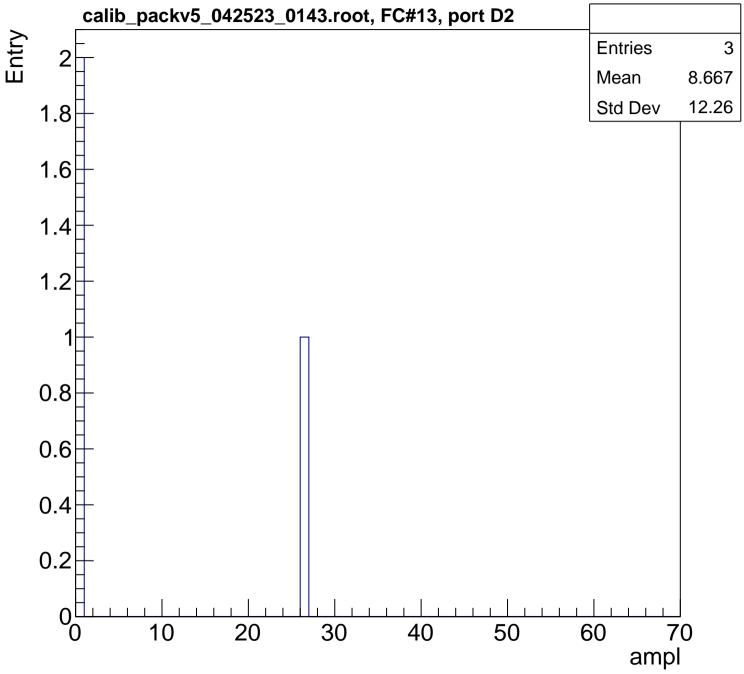


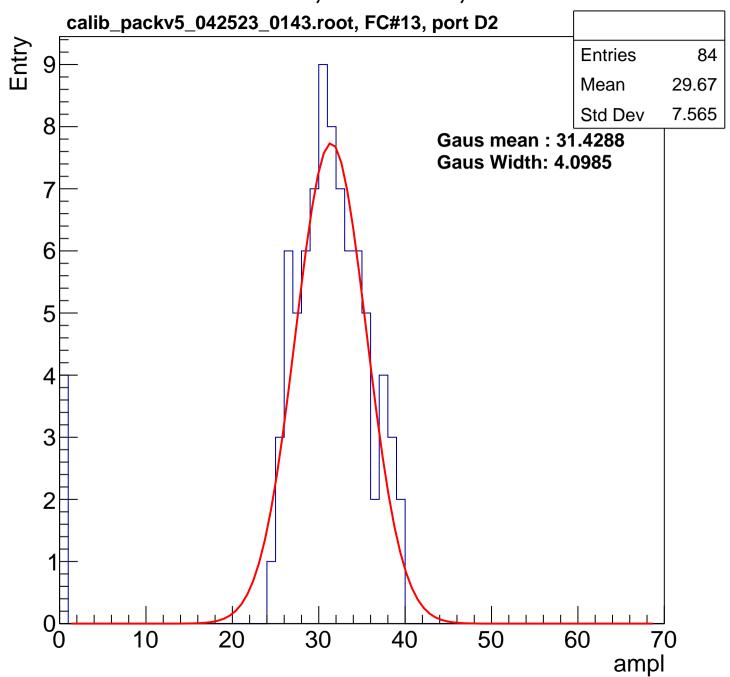


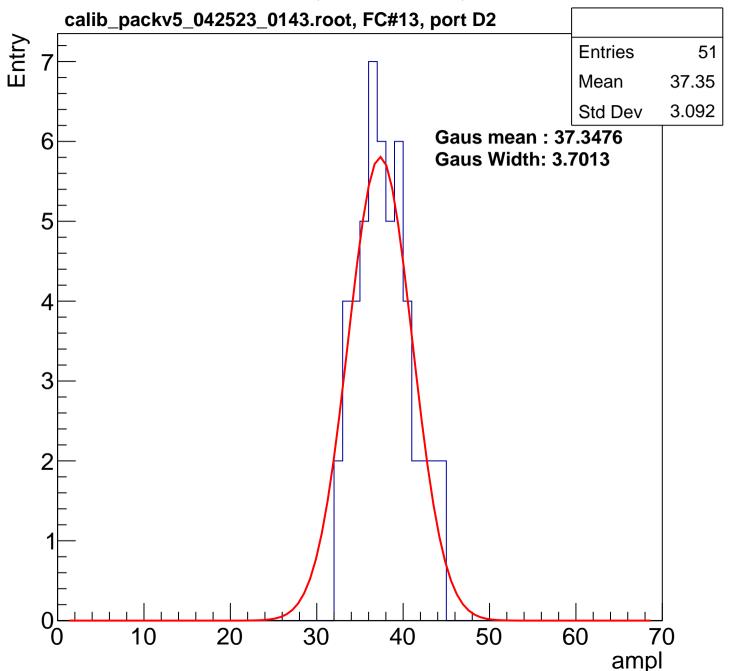


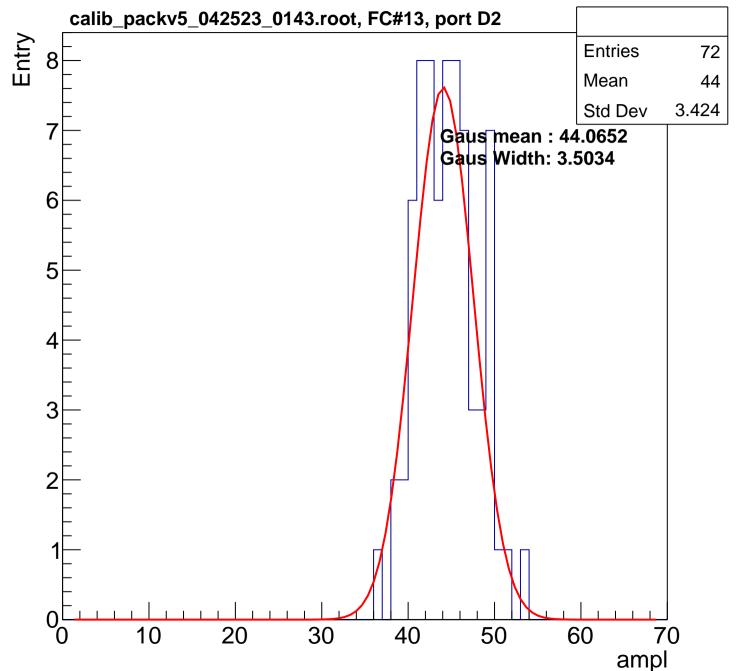


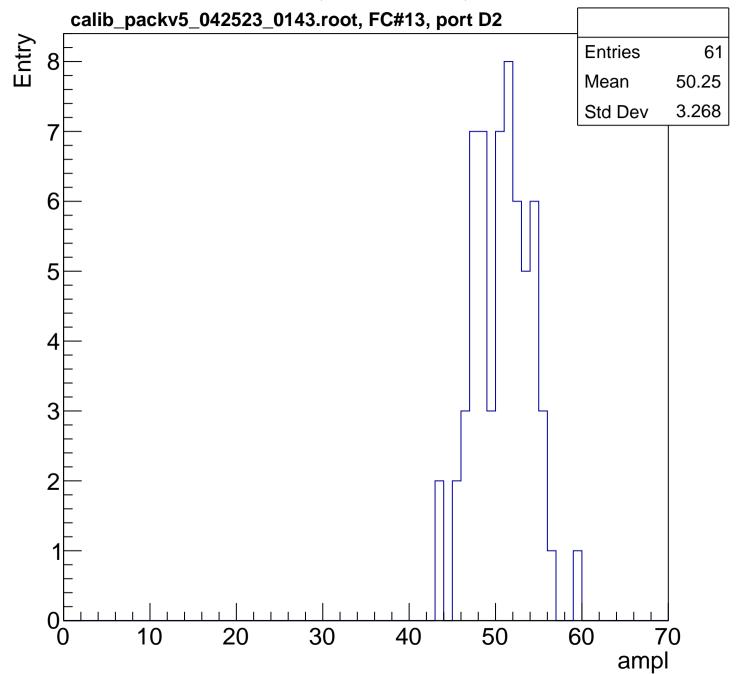


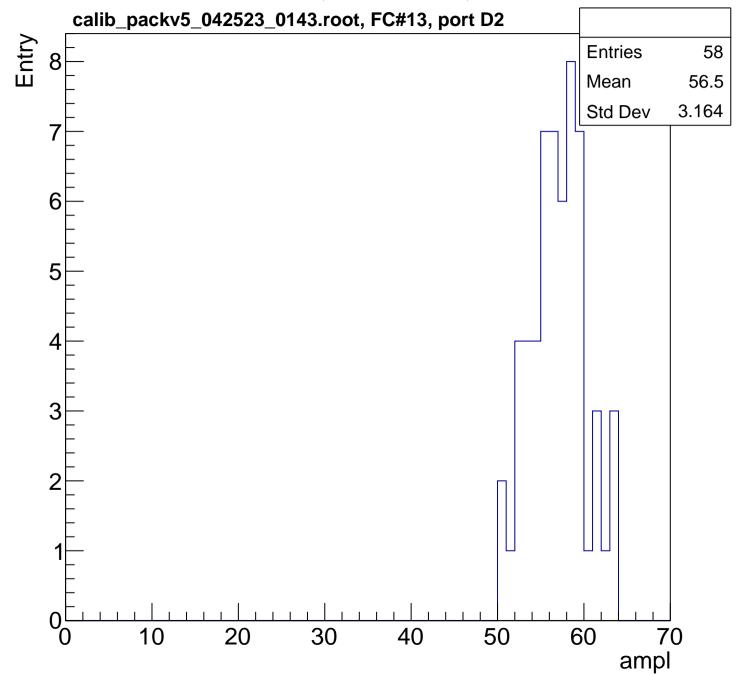


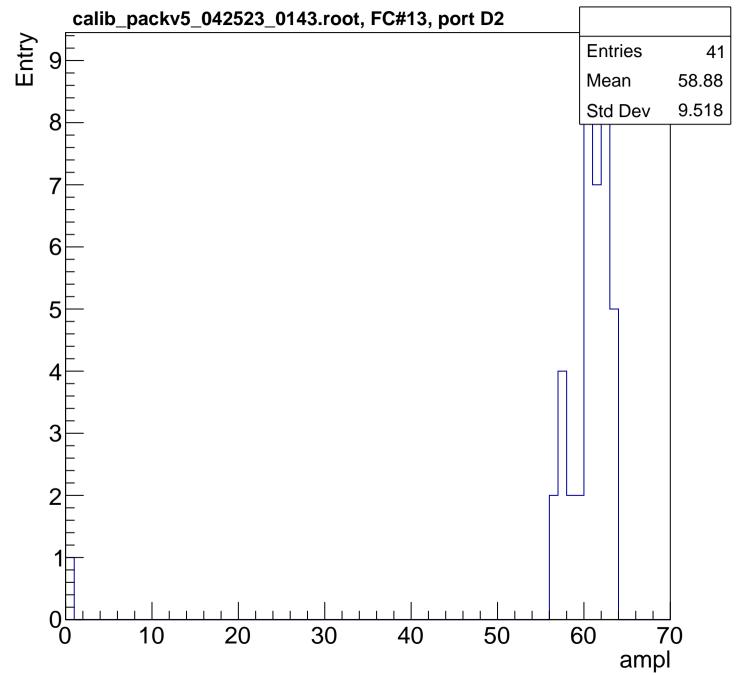


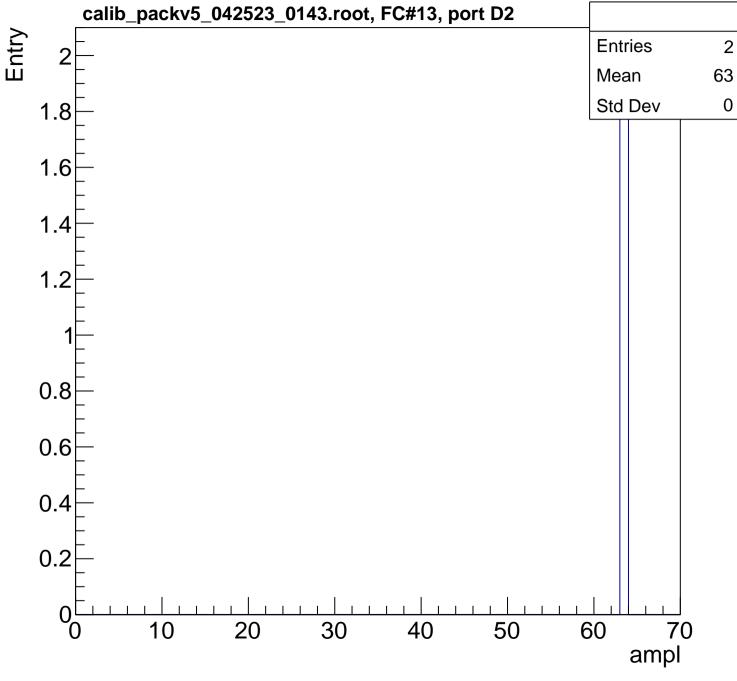


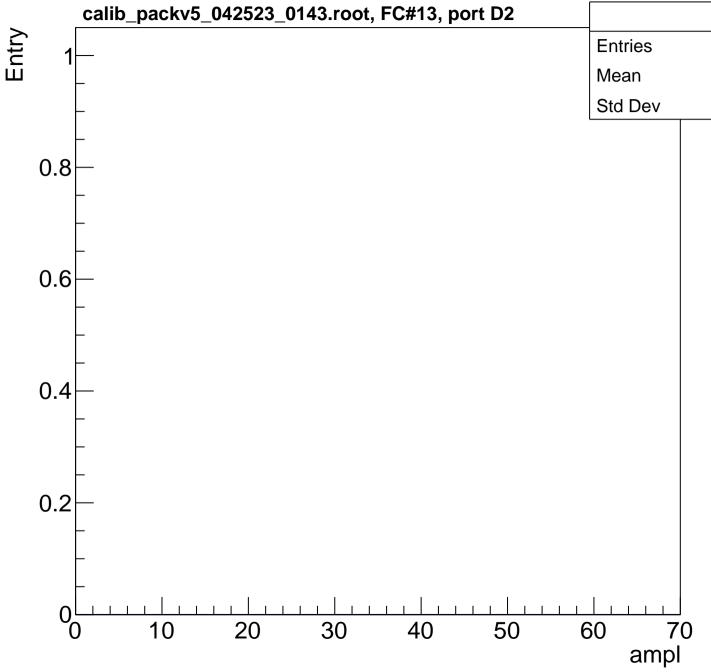


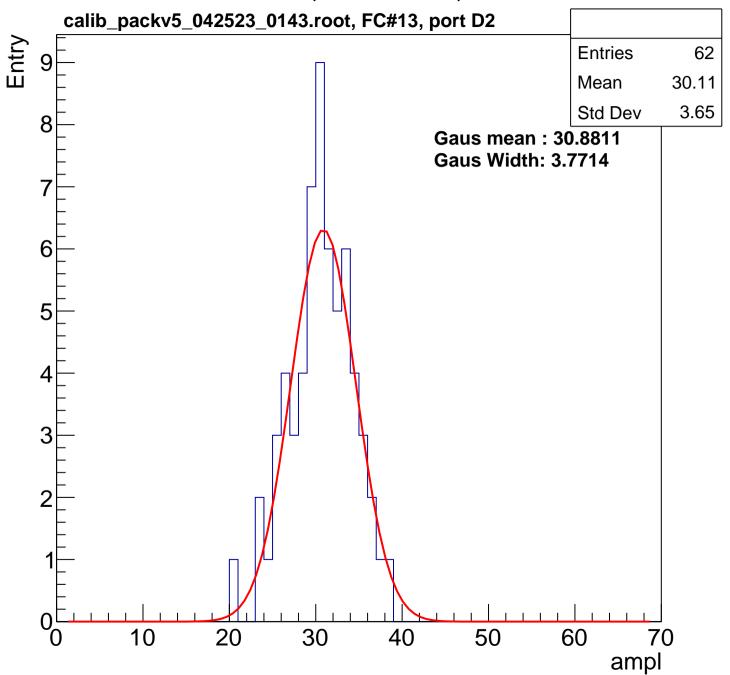


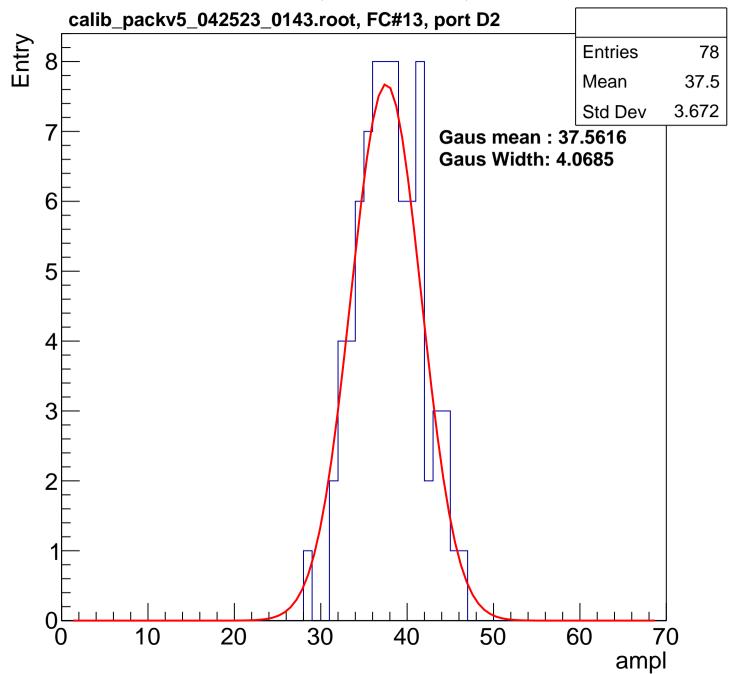


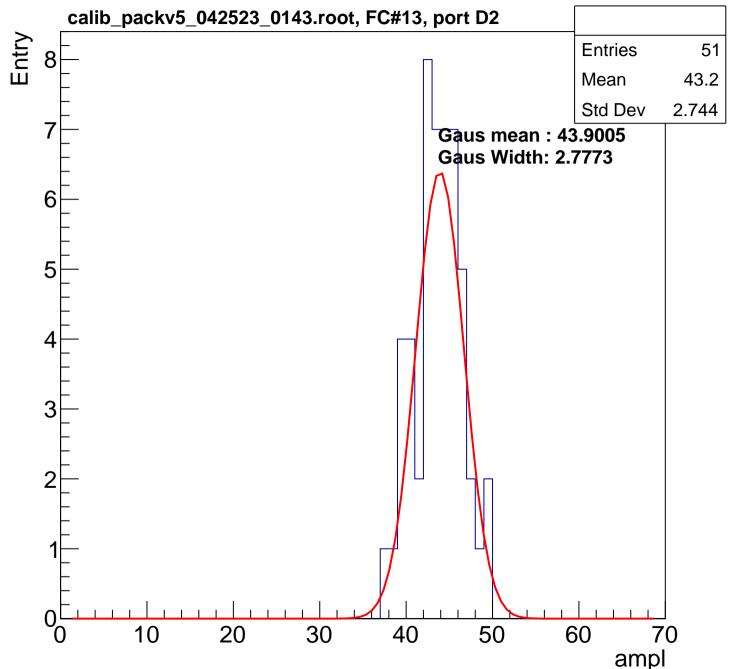


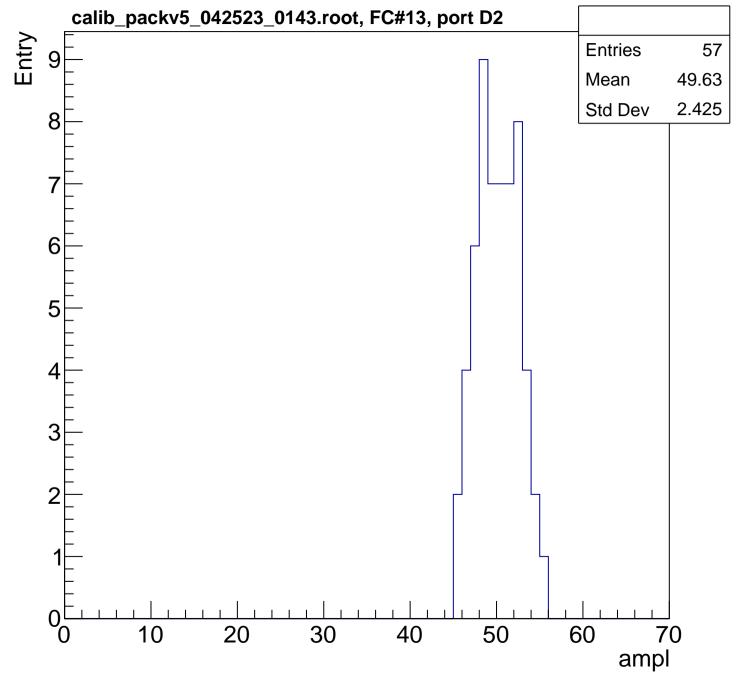


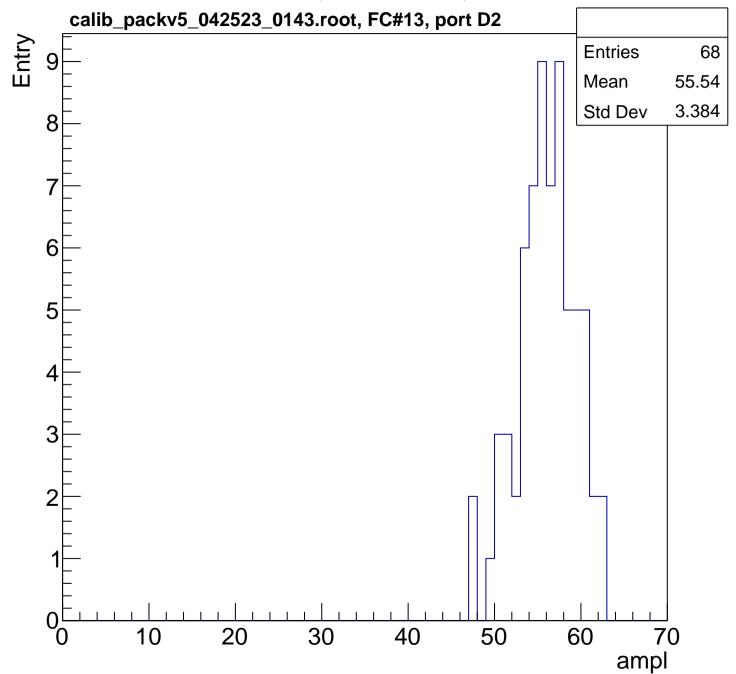


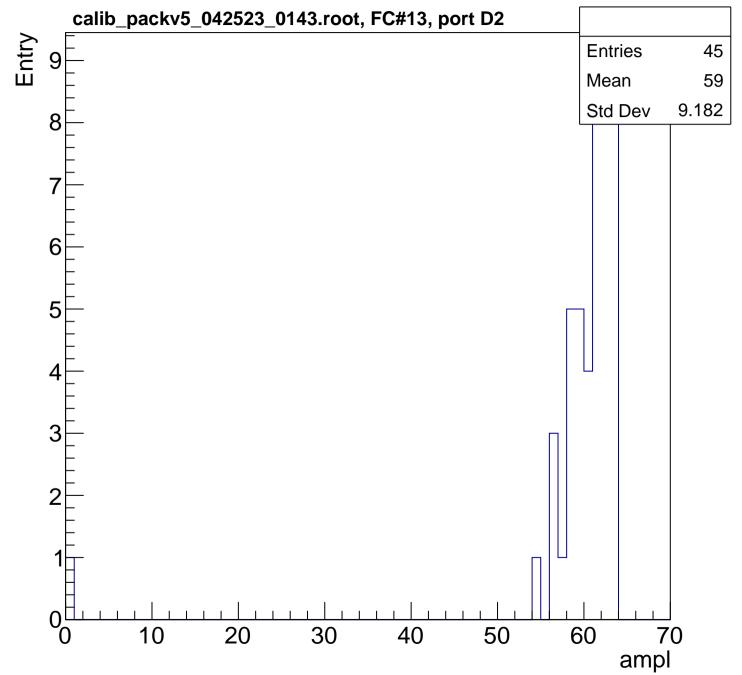


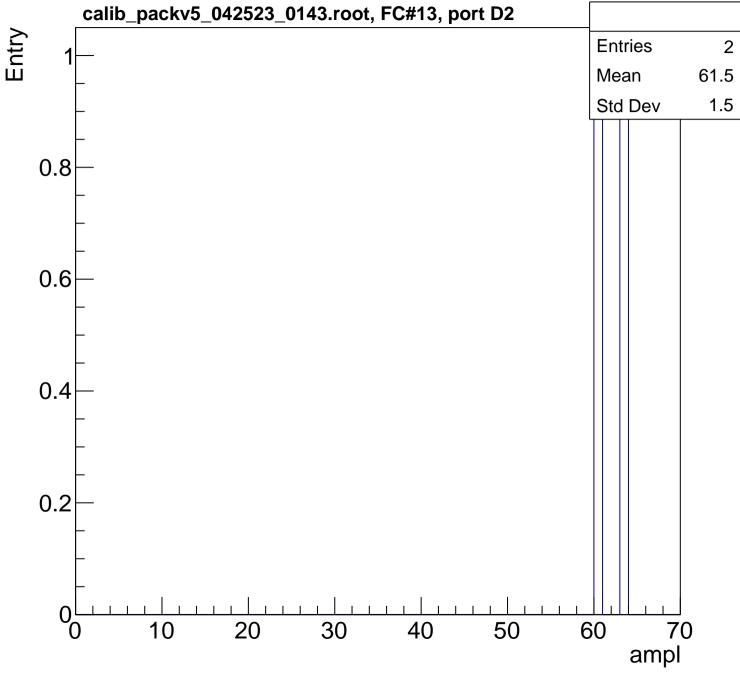




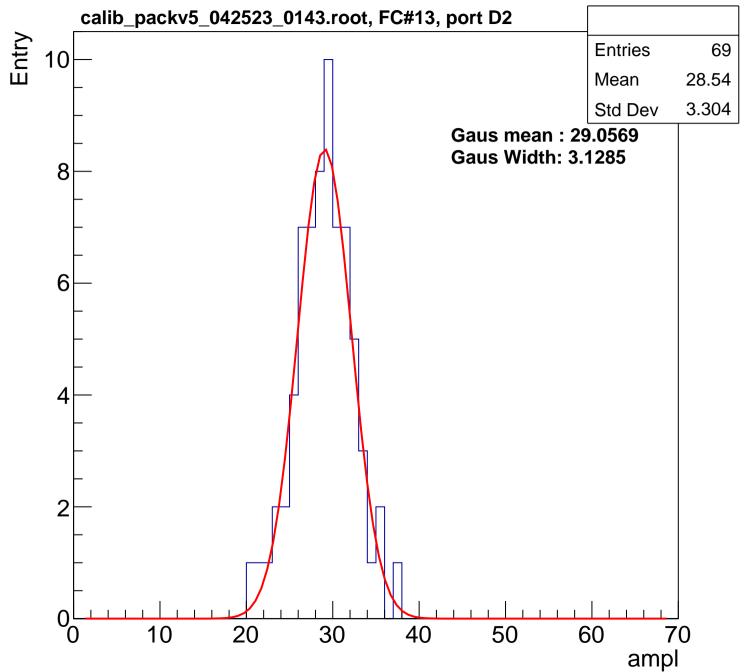


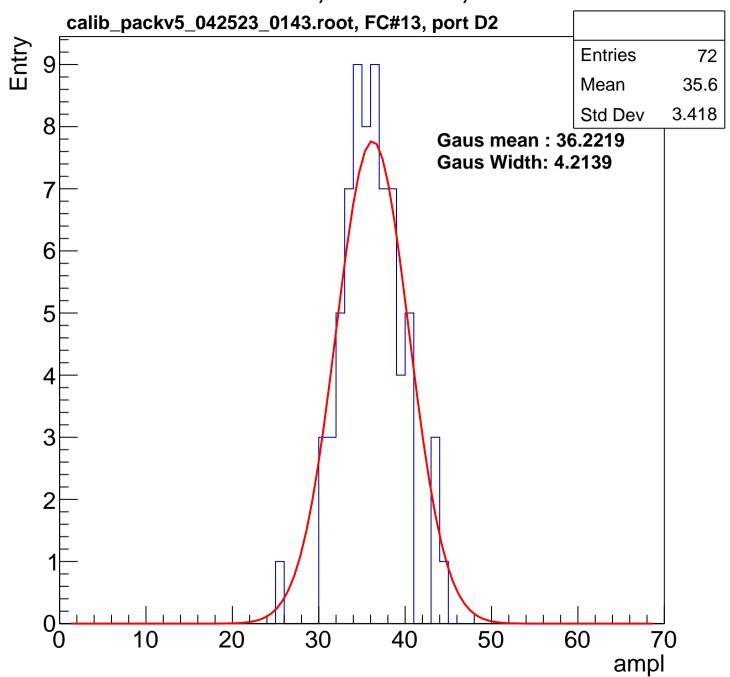


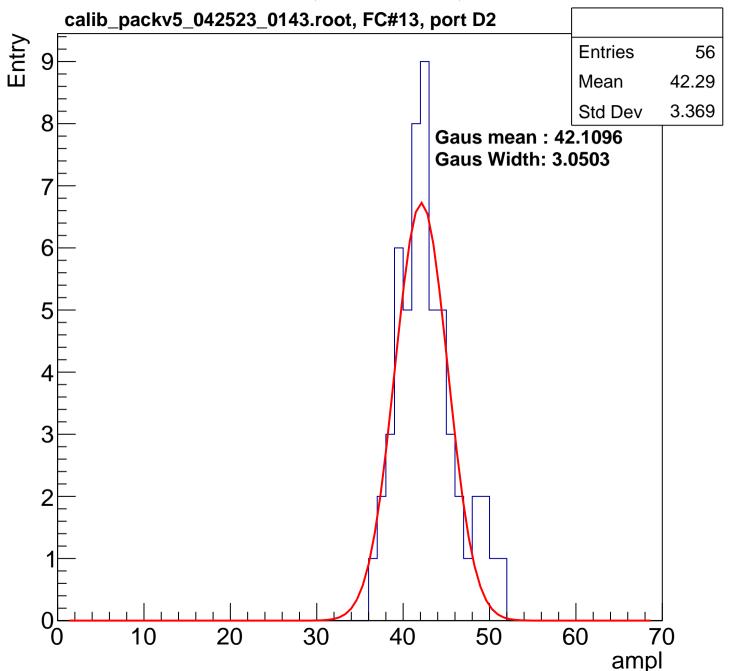


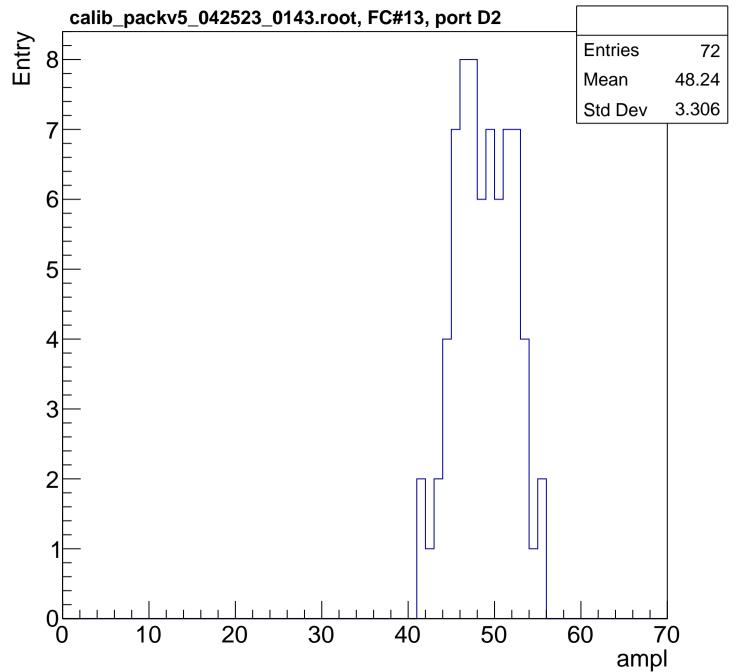


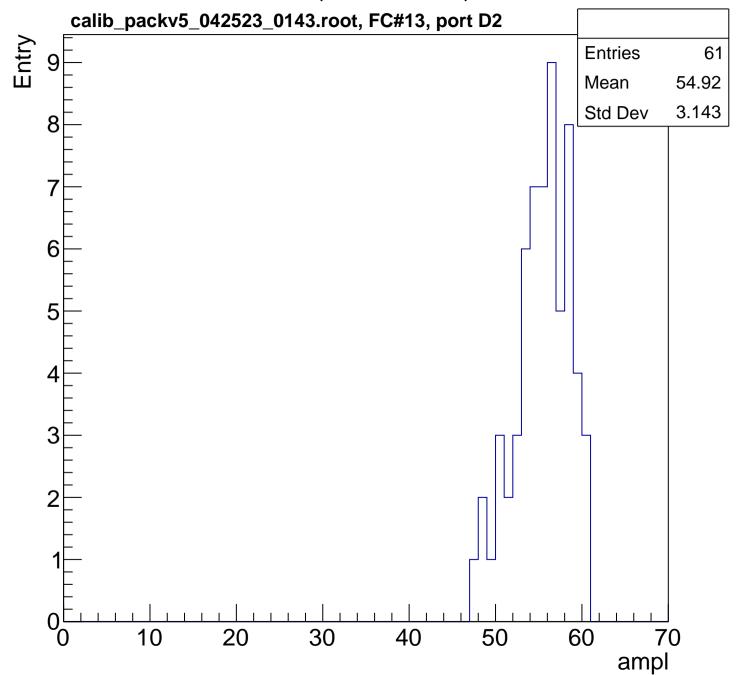
B1L003S, U8-ch46, adc7 calib\_packv5\_042523\_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

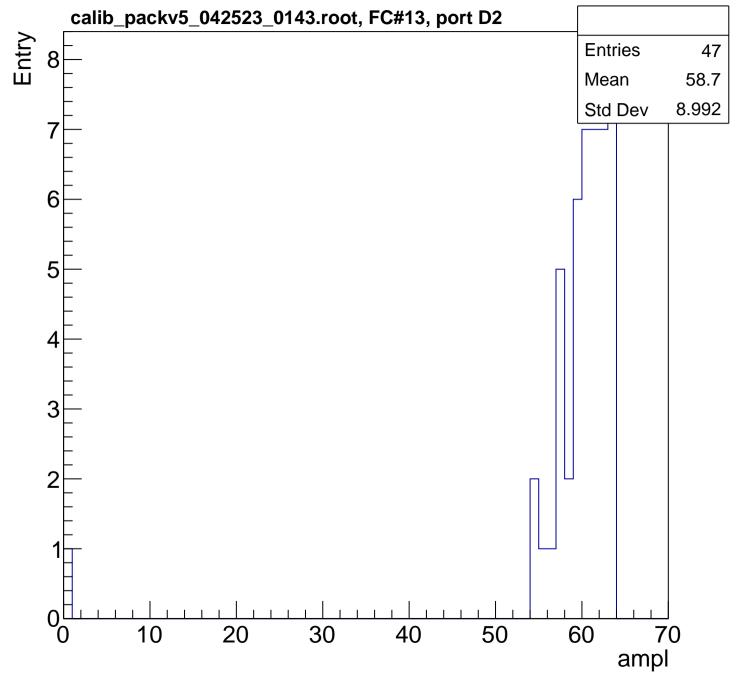


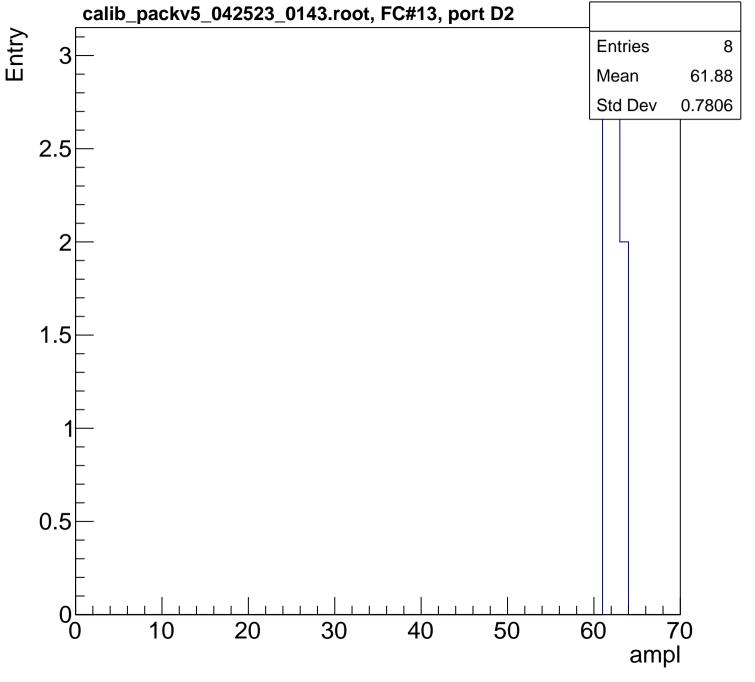


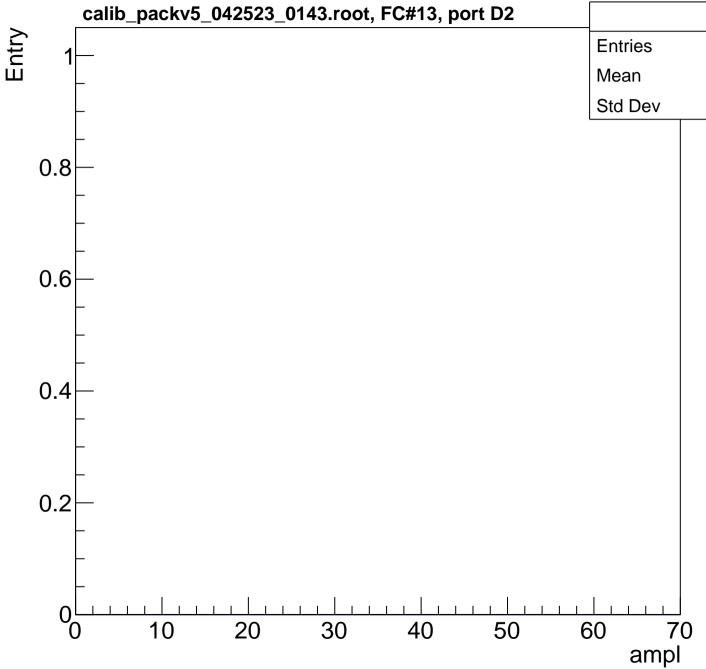


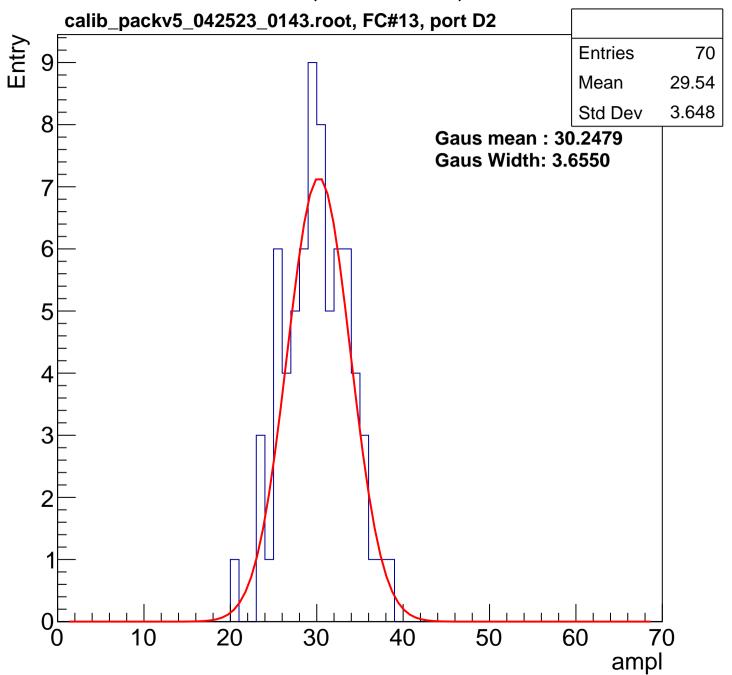


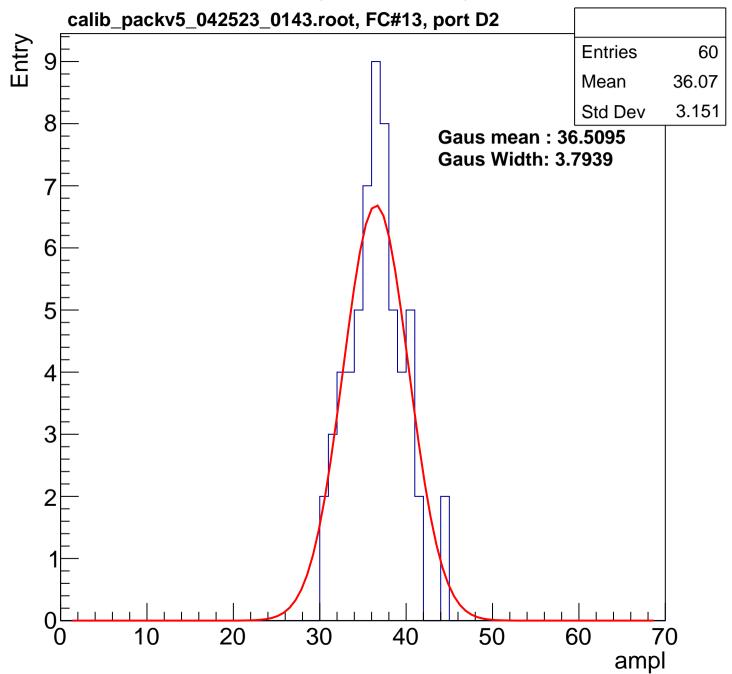


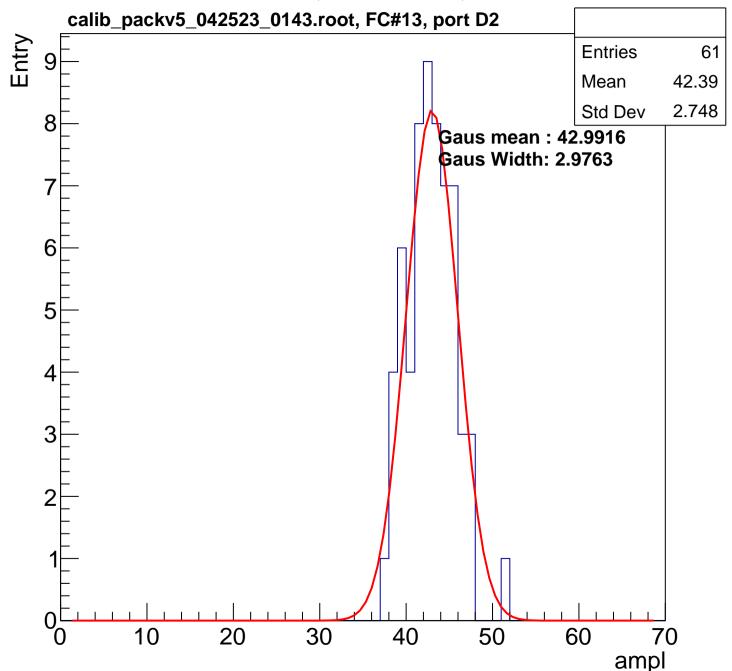


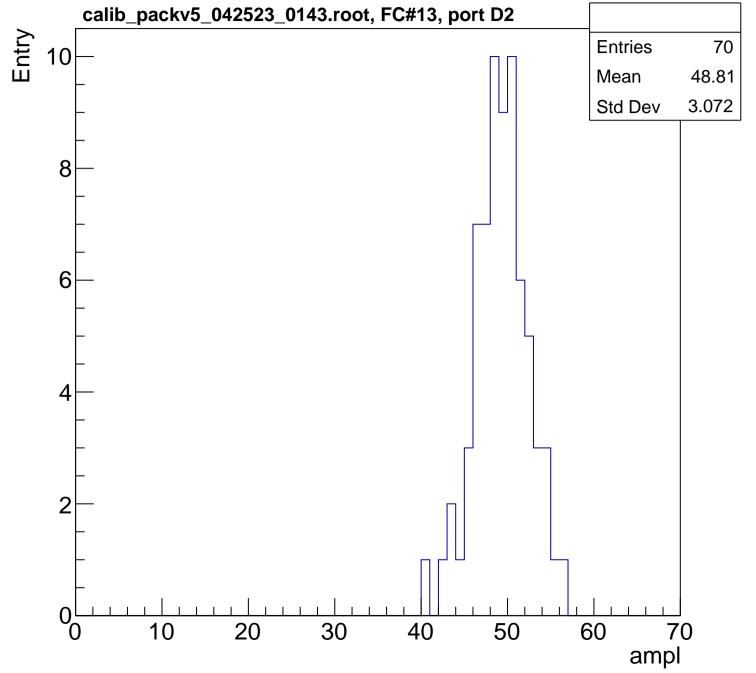


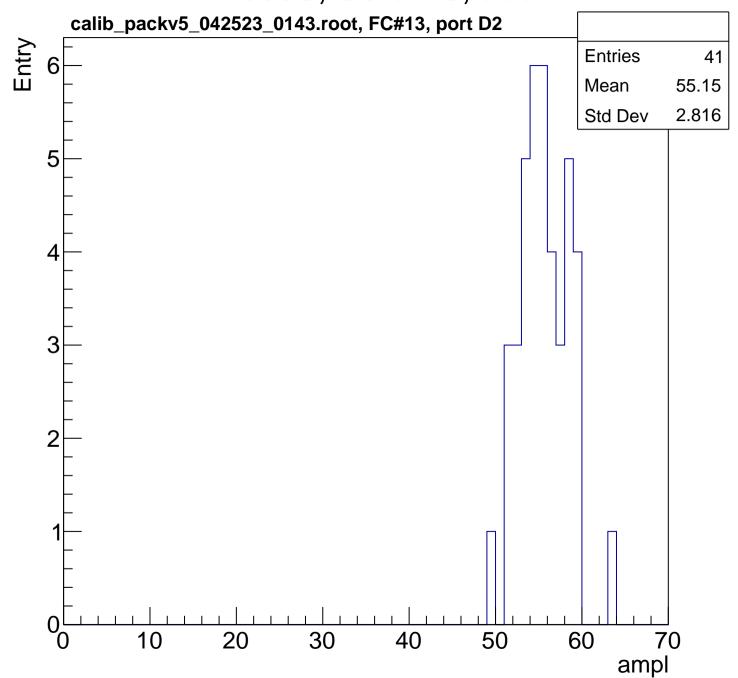


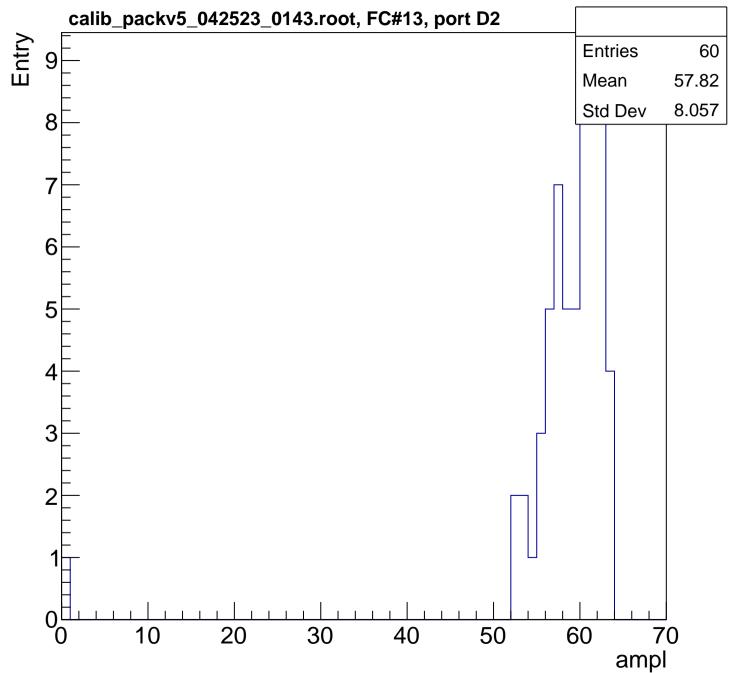


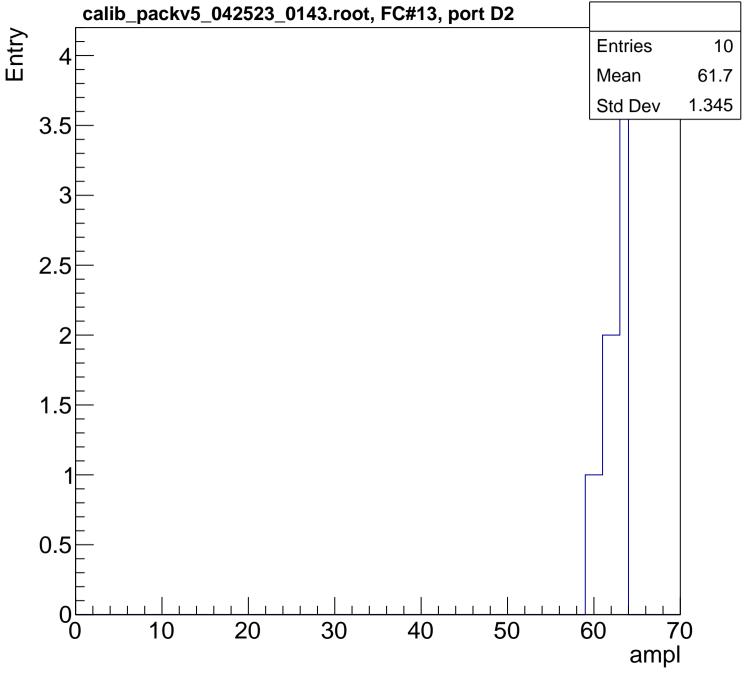


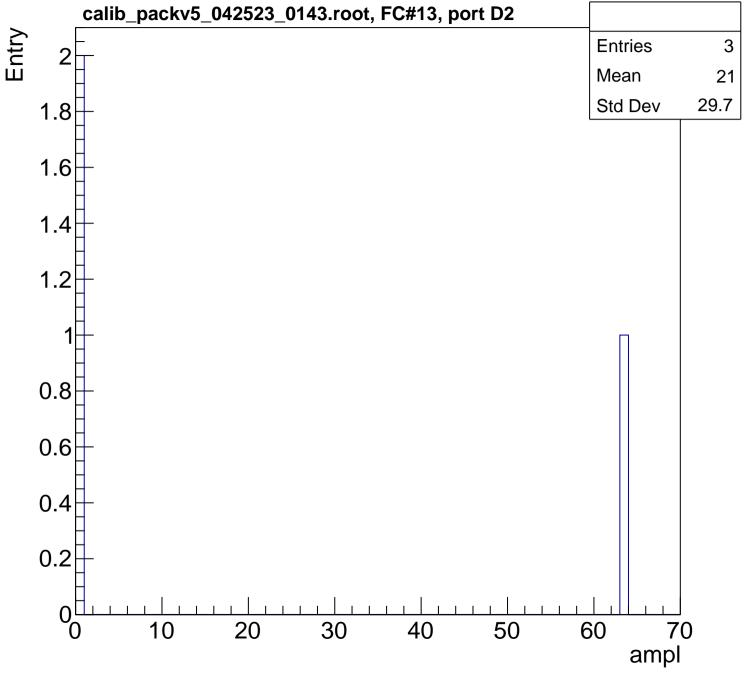


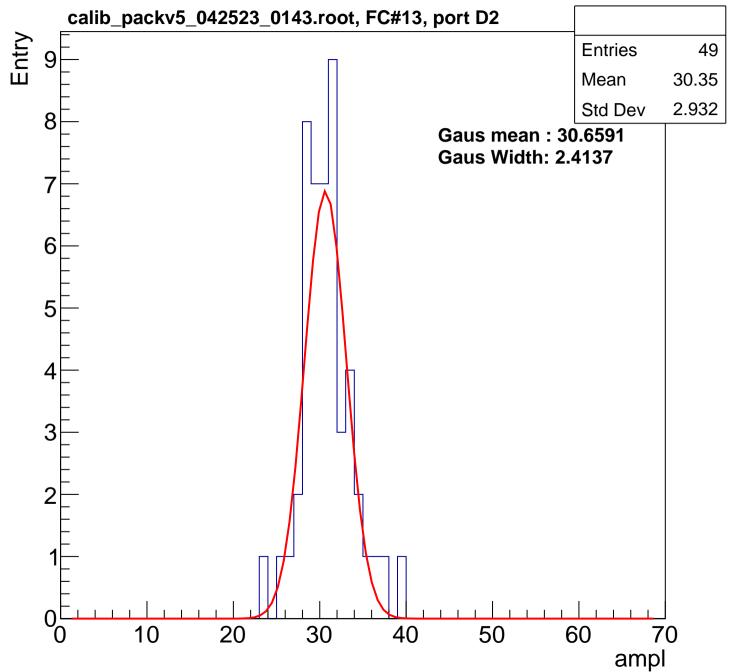


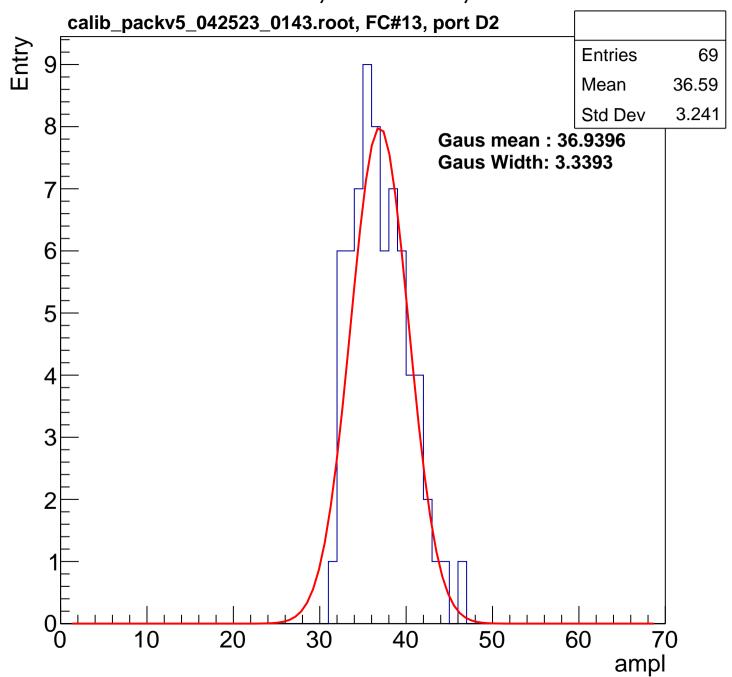


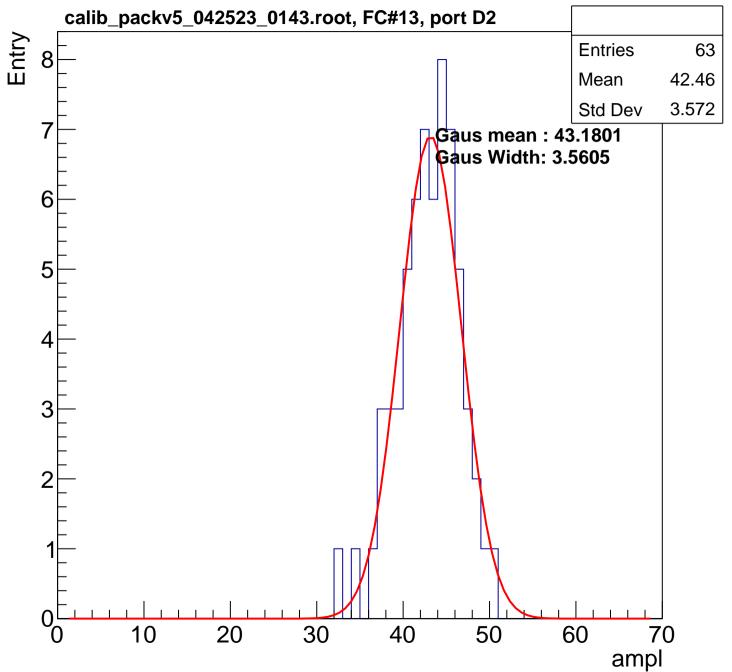


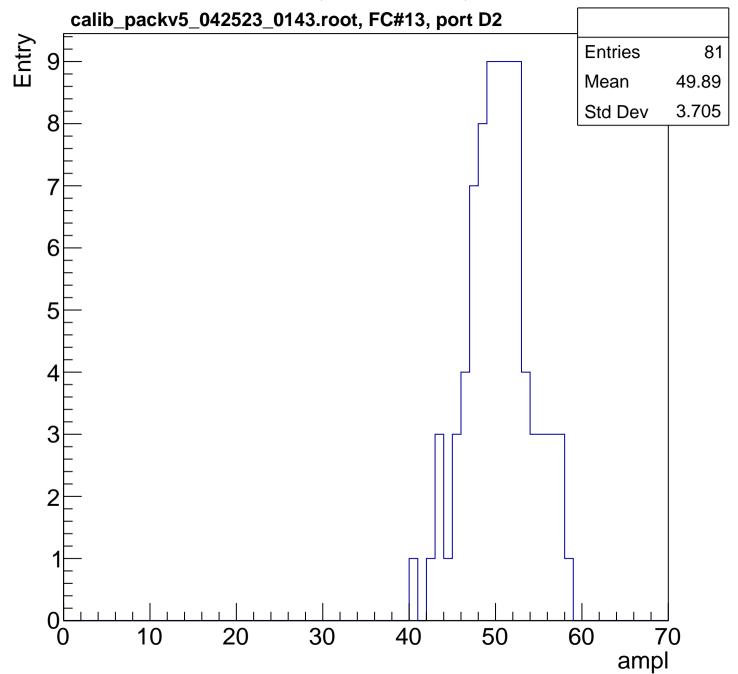


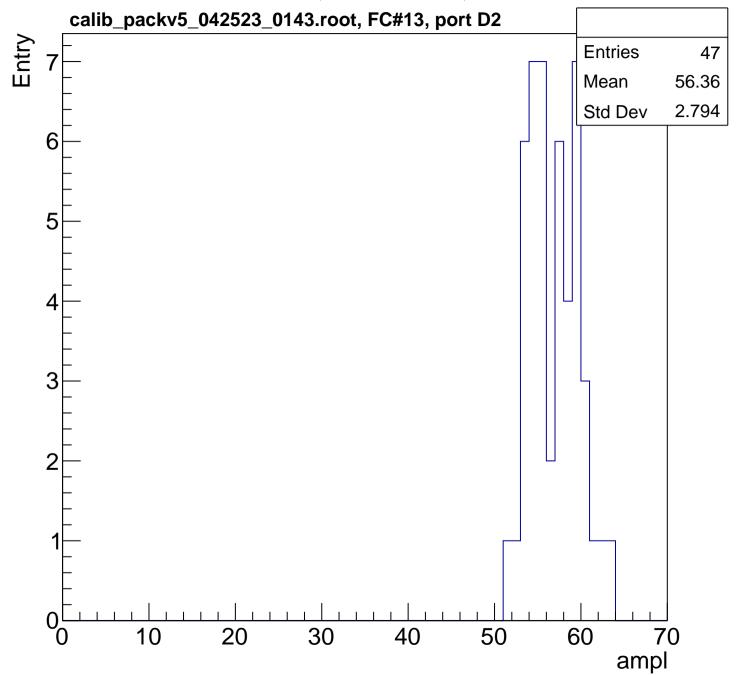


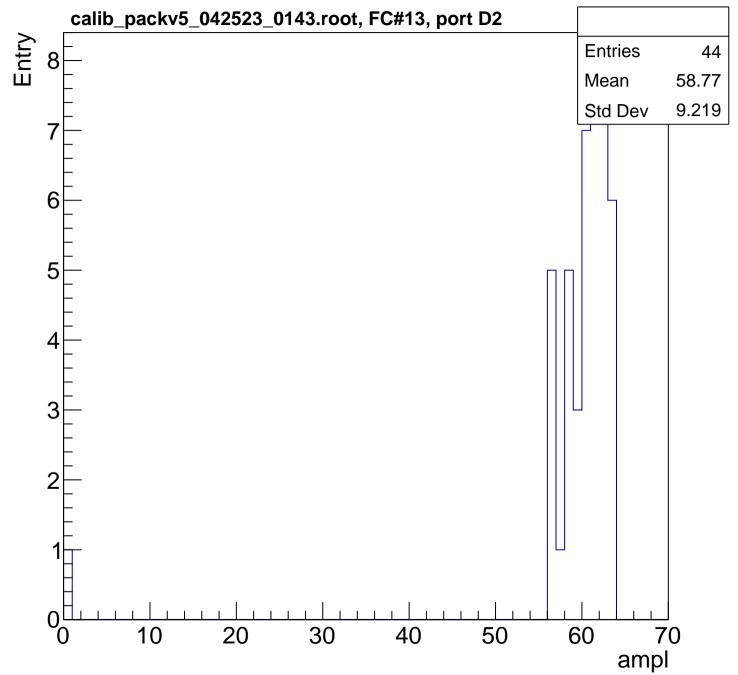


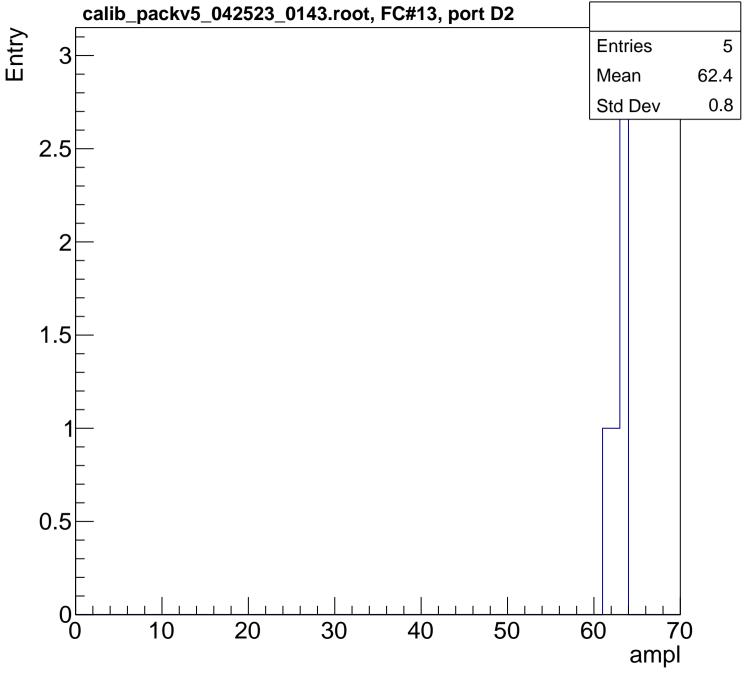




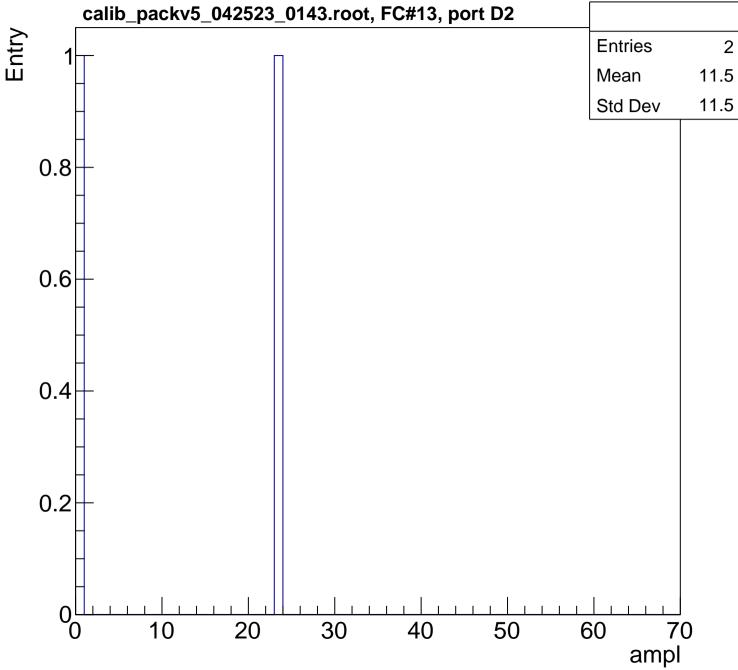


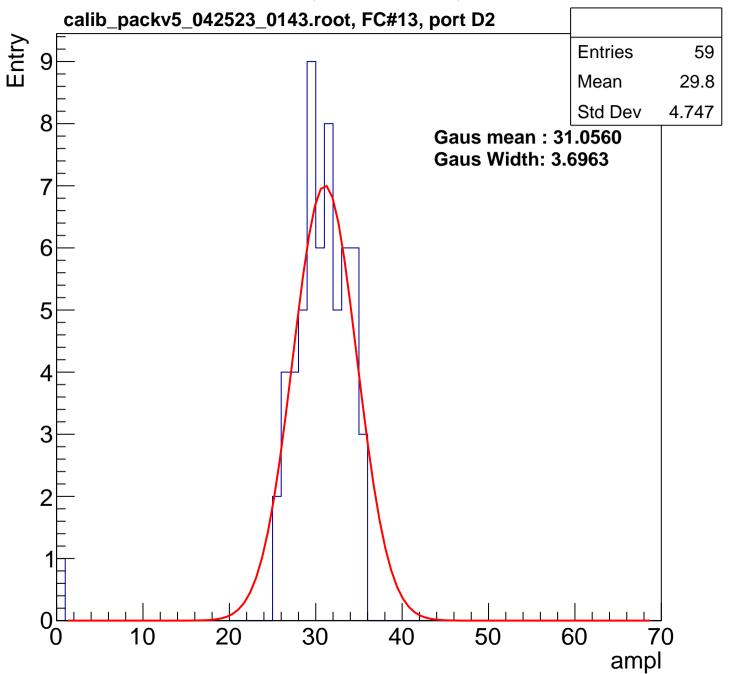


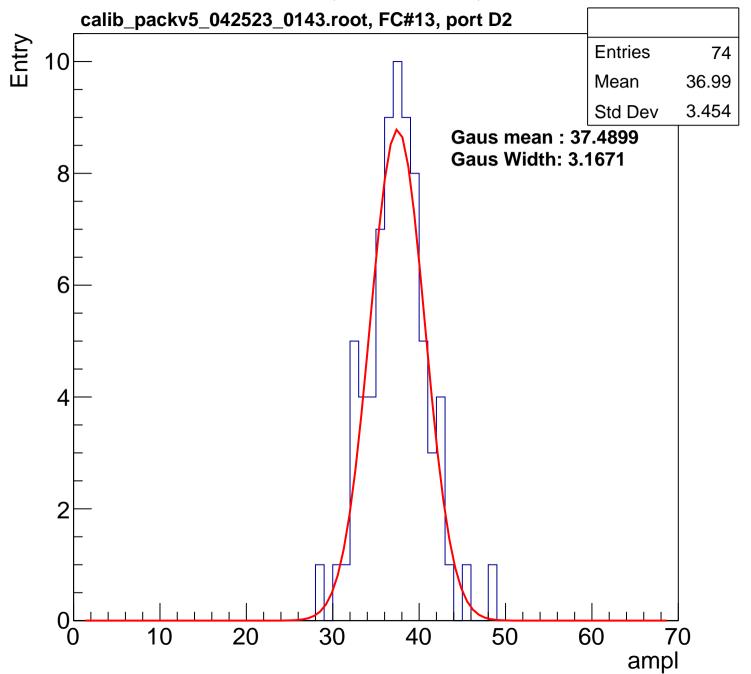


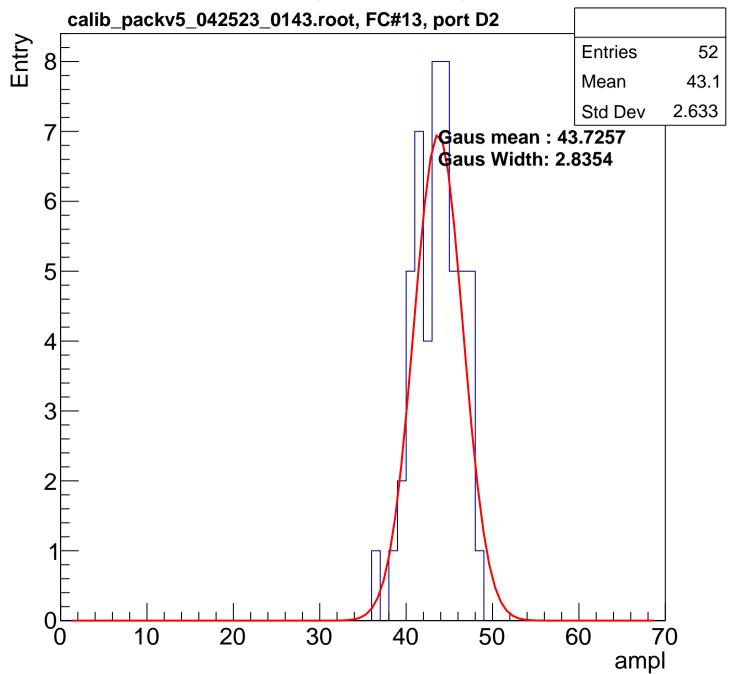


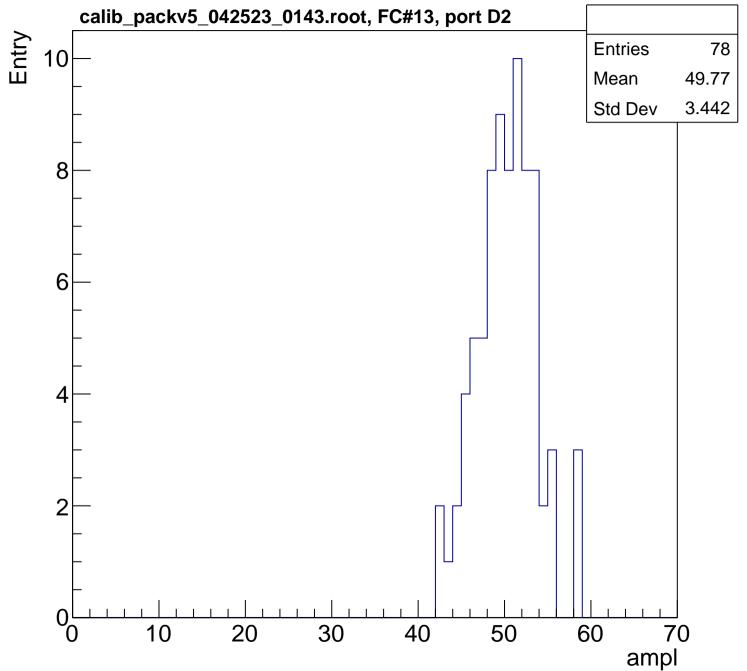
2

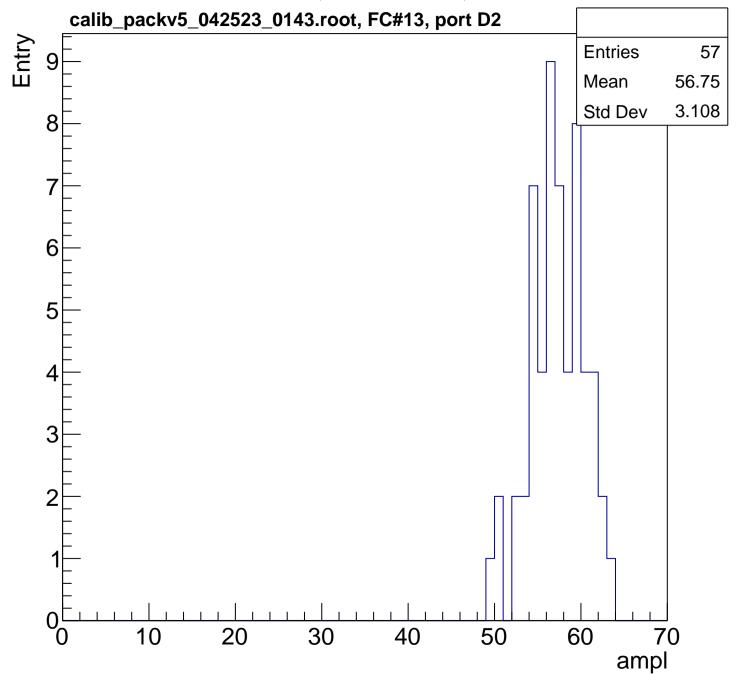


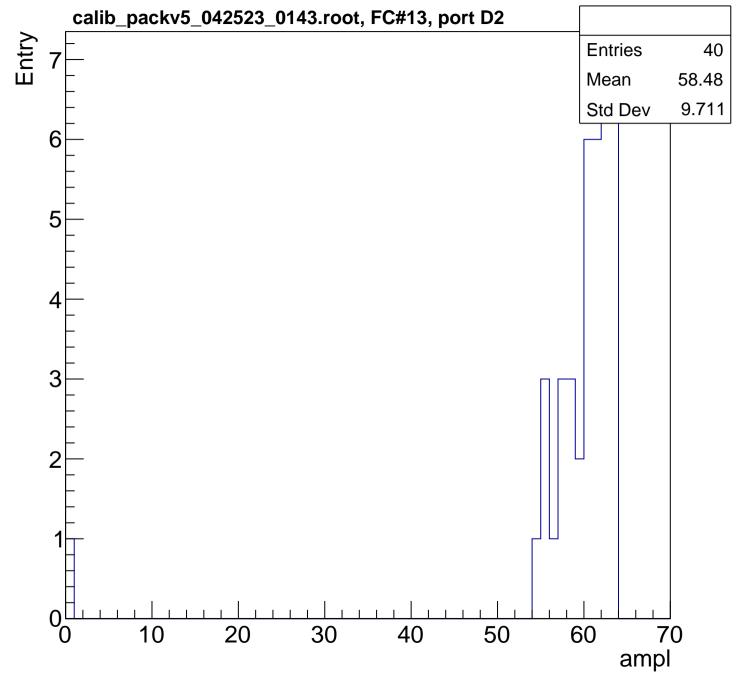


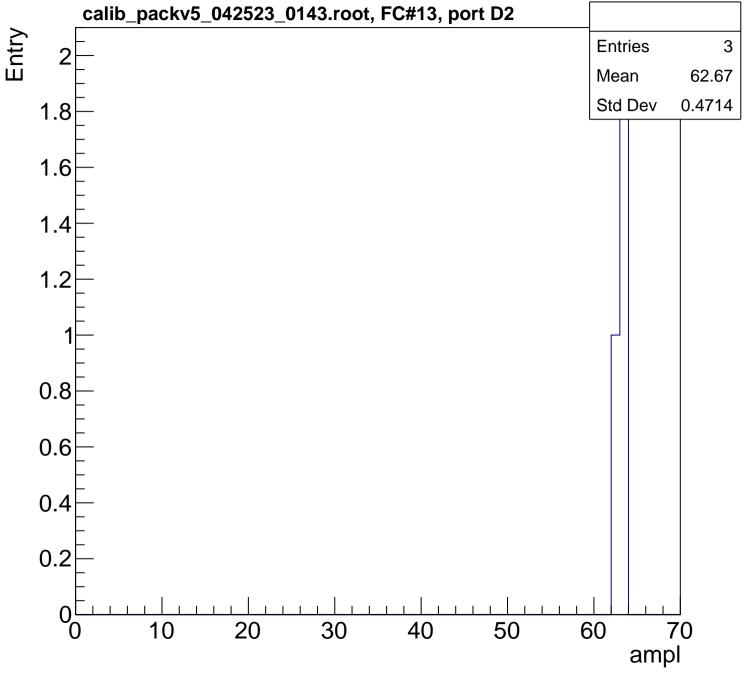


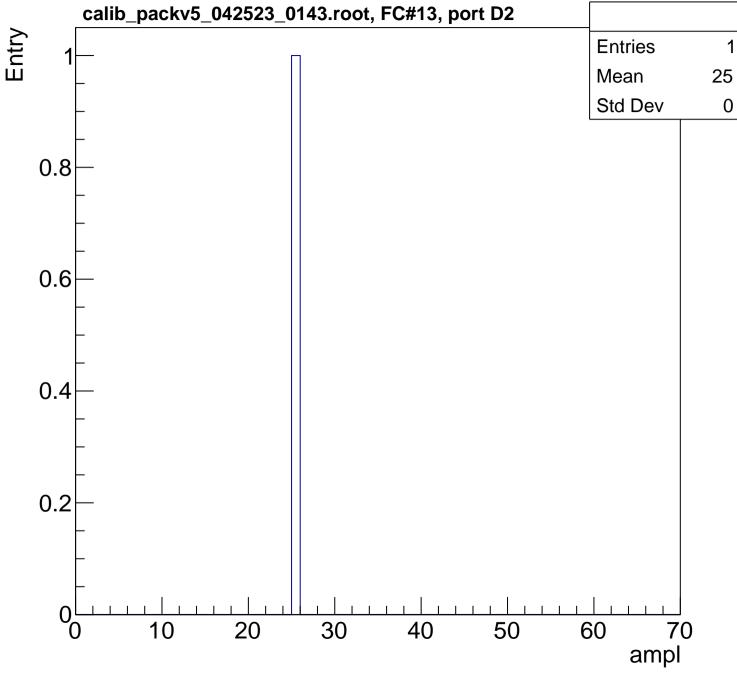


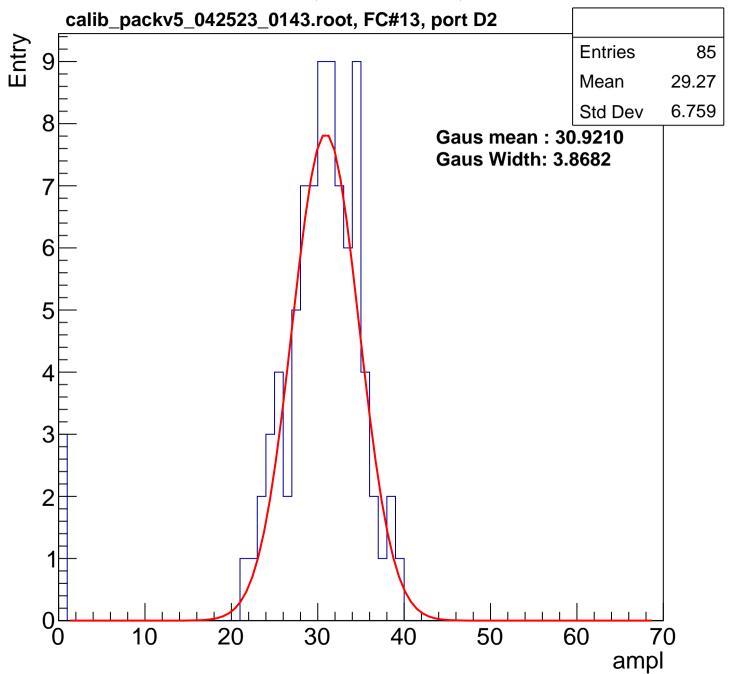


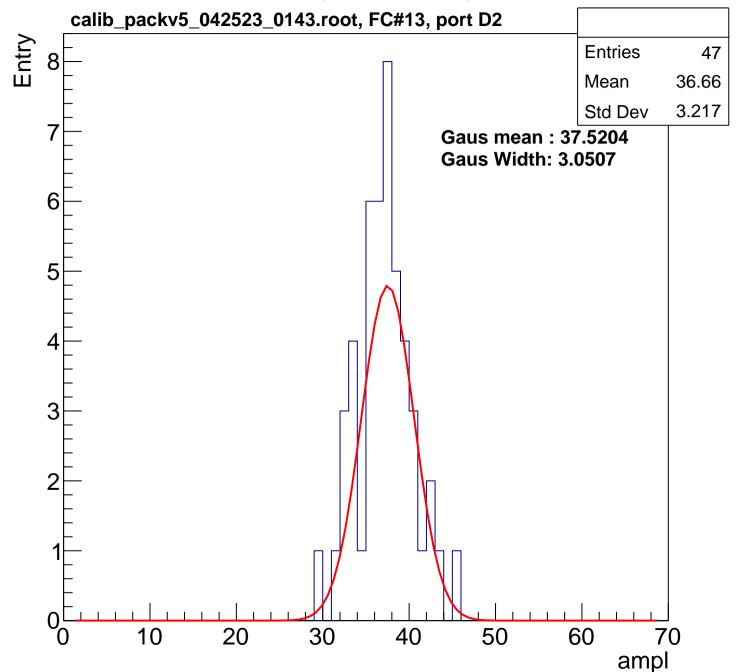


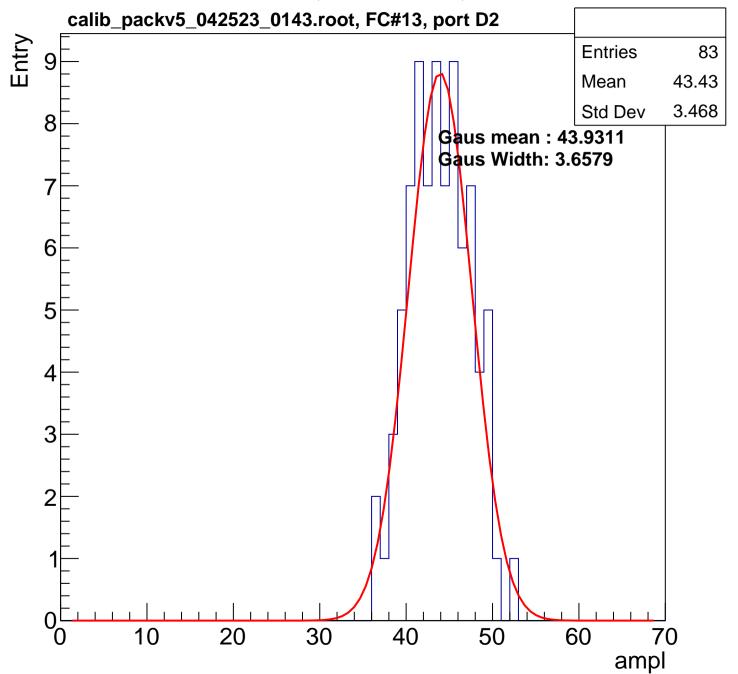


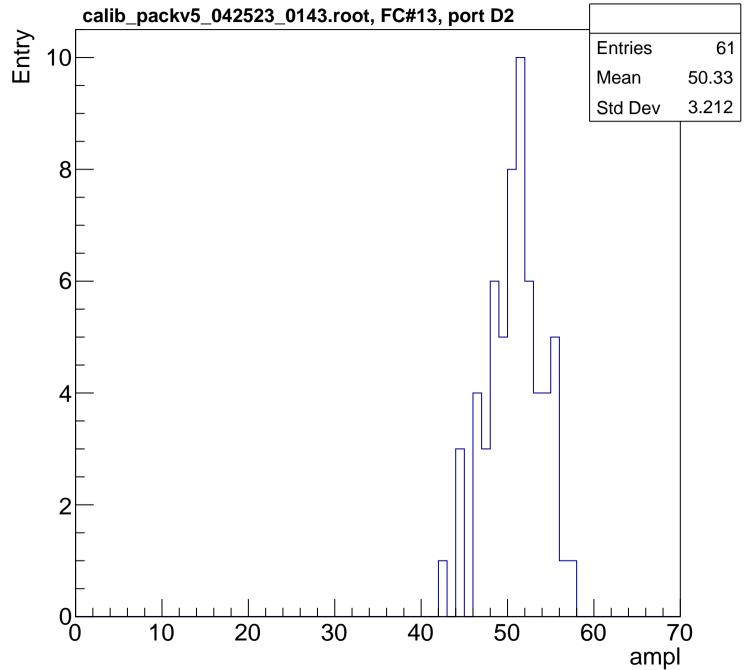


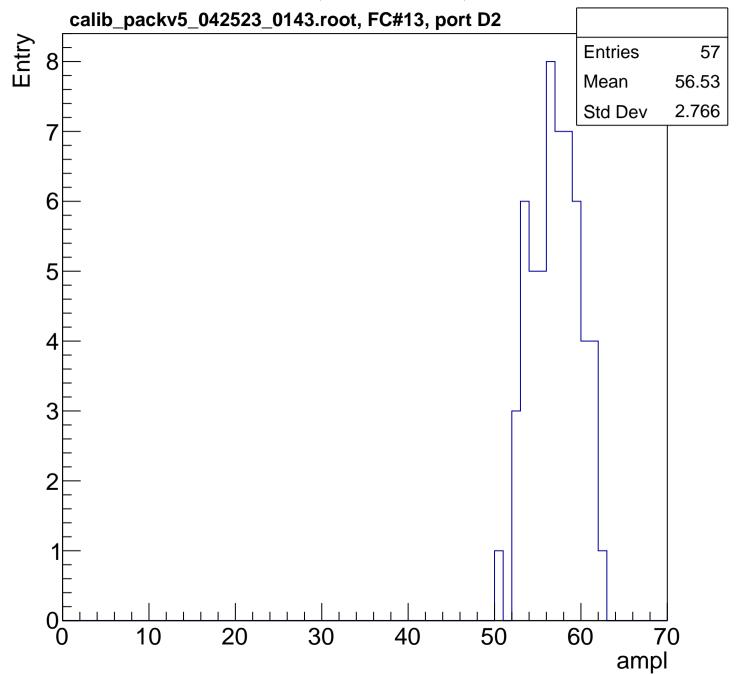


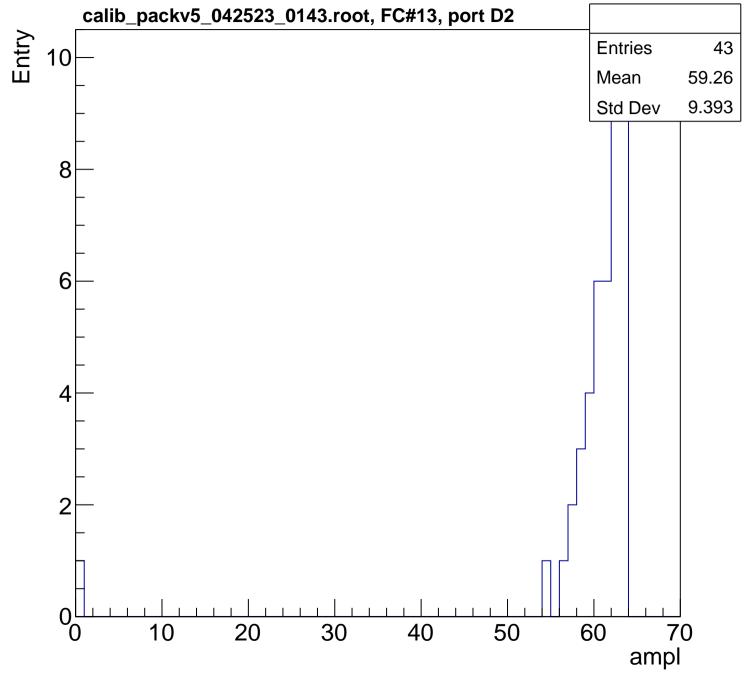






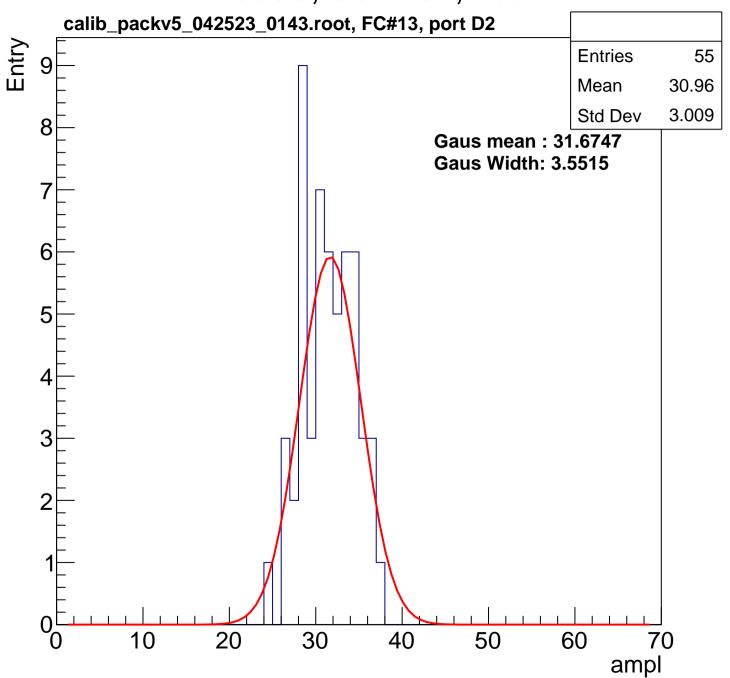


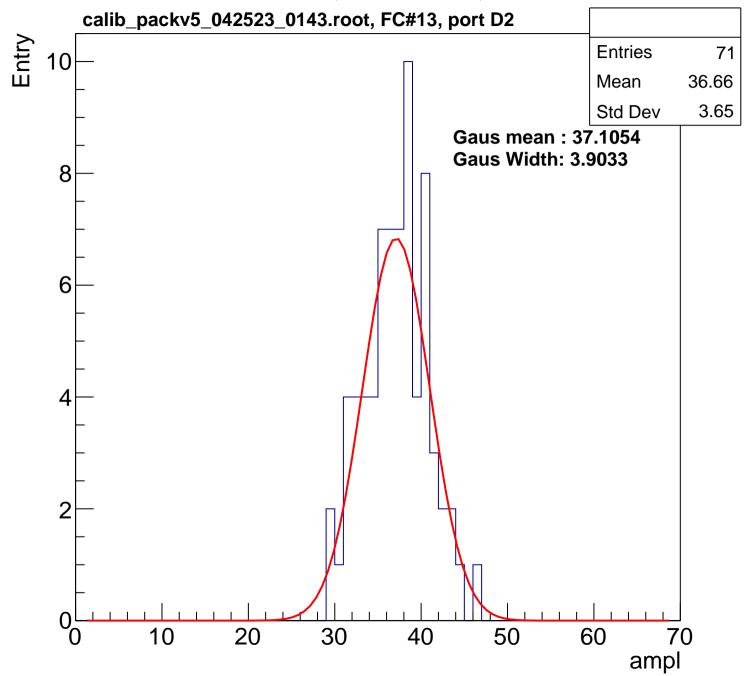


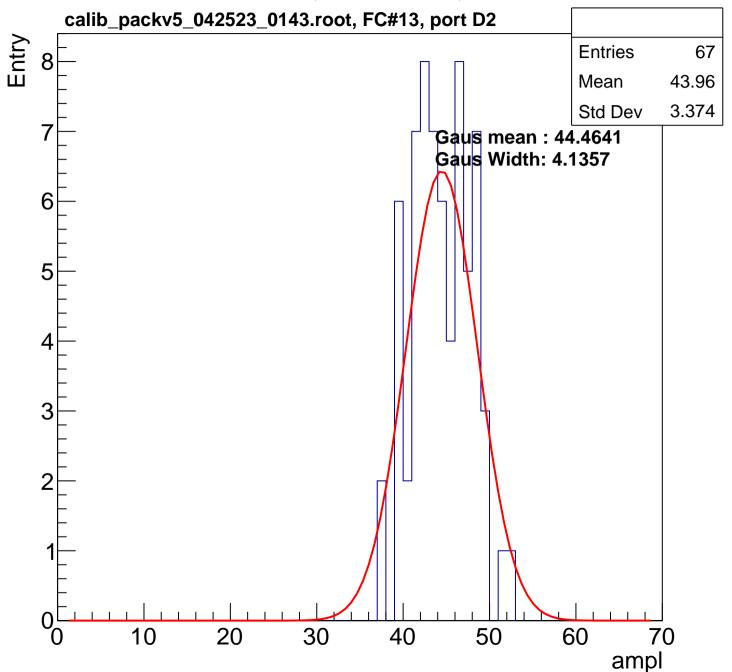


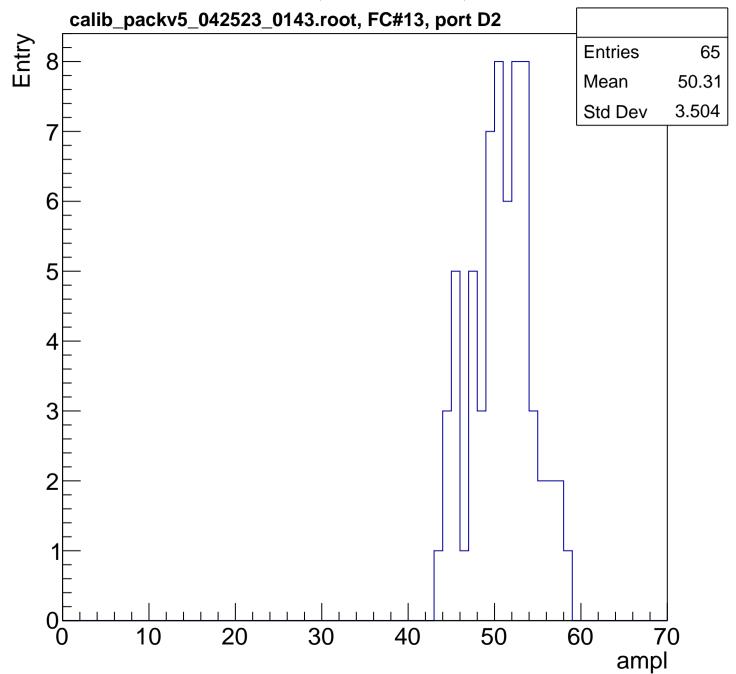


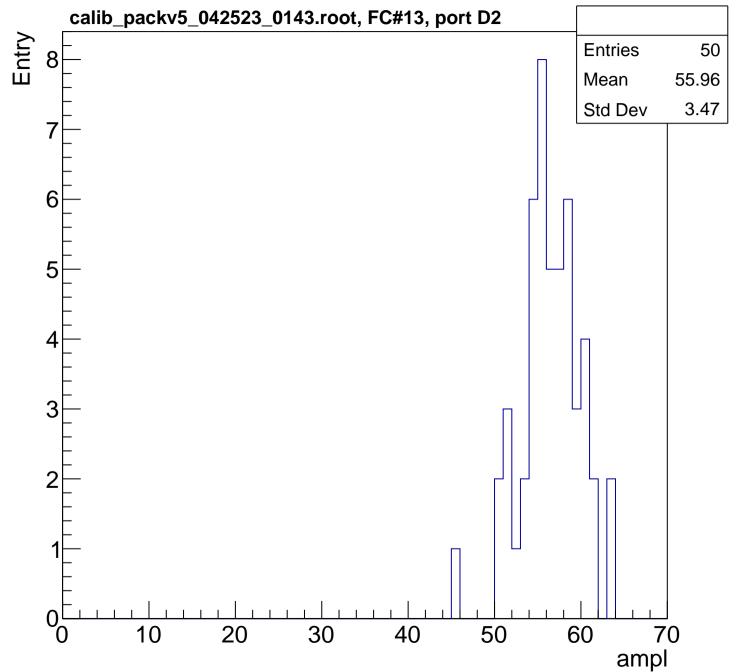
B1L003S, U8-ch51, adc7 calib\_packv5\_042523\_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

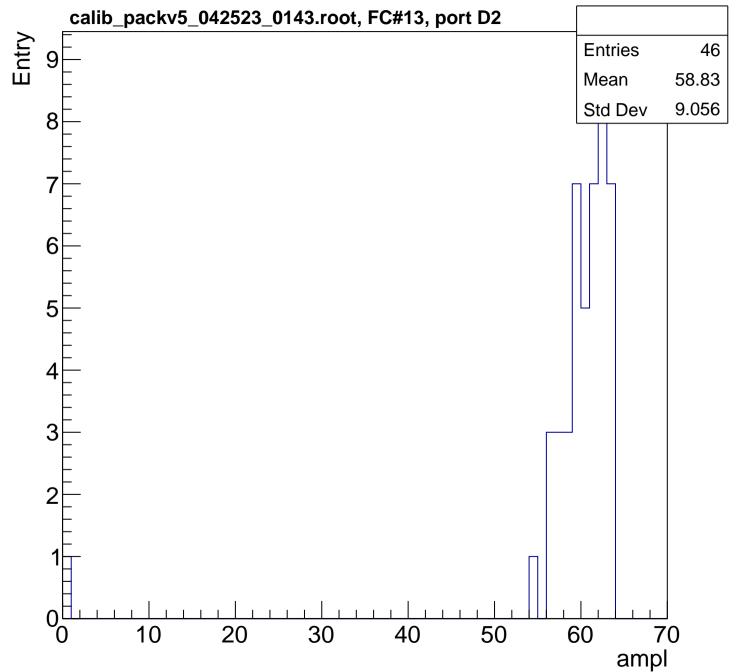


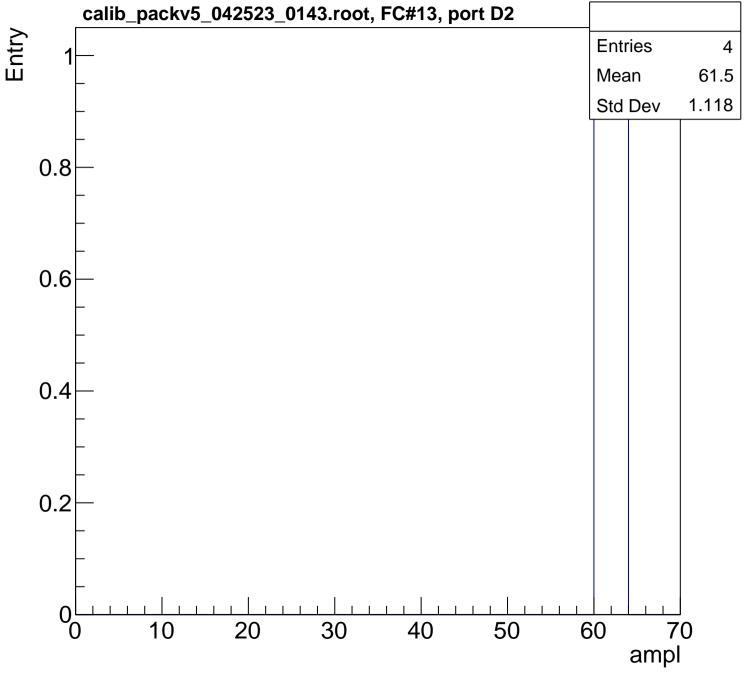




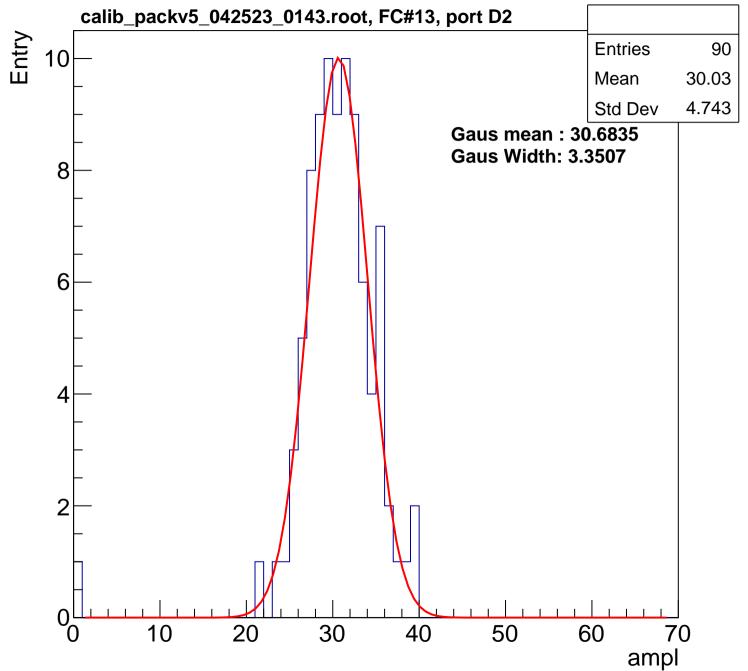


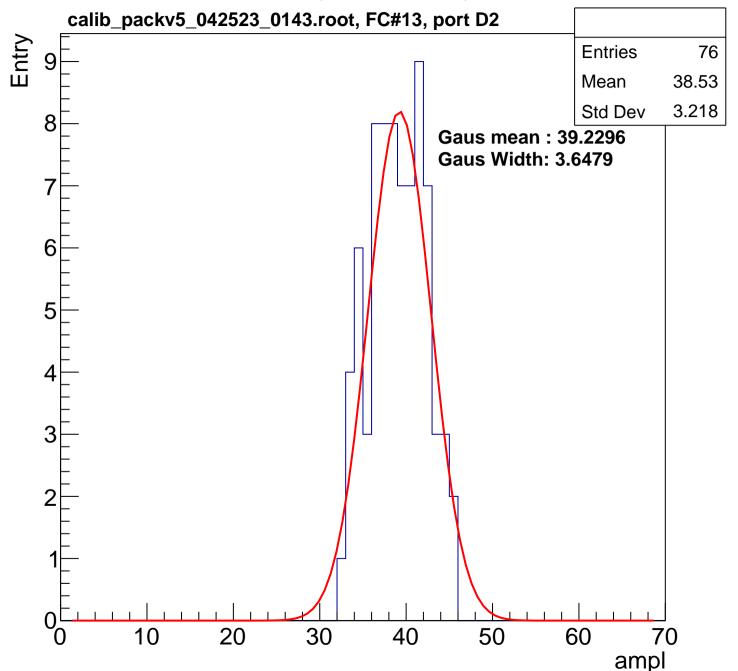


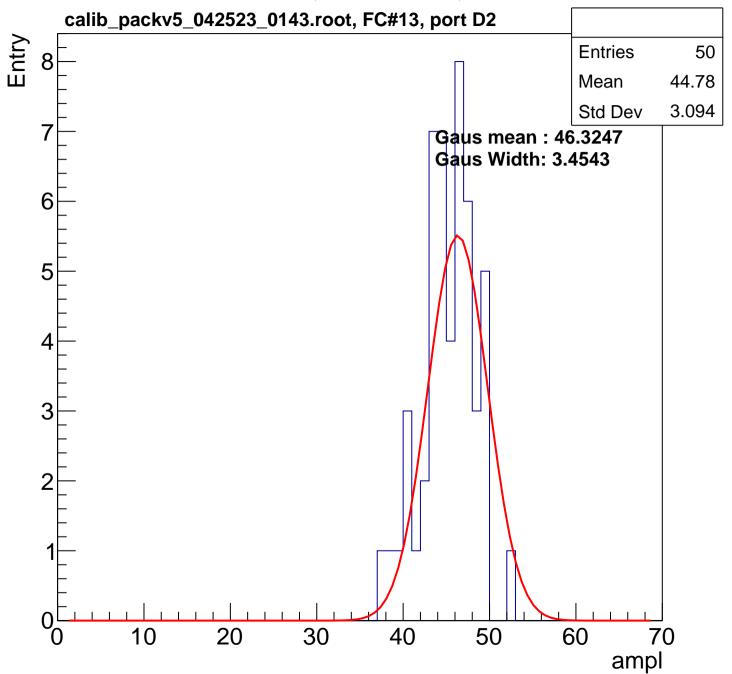


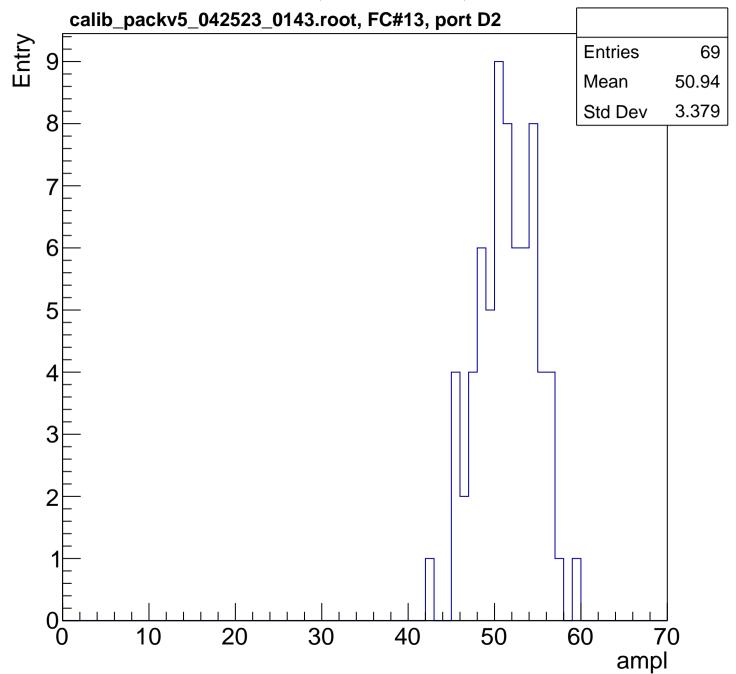


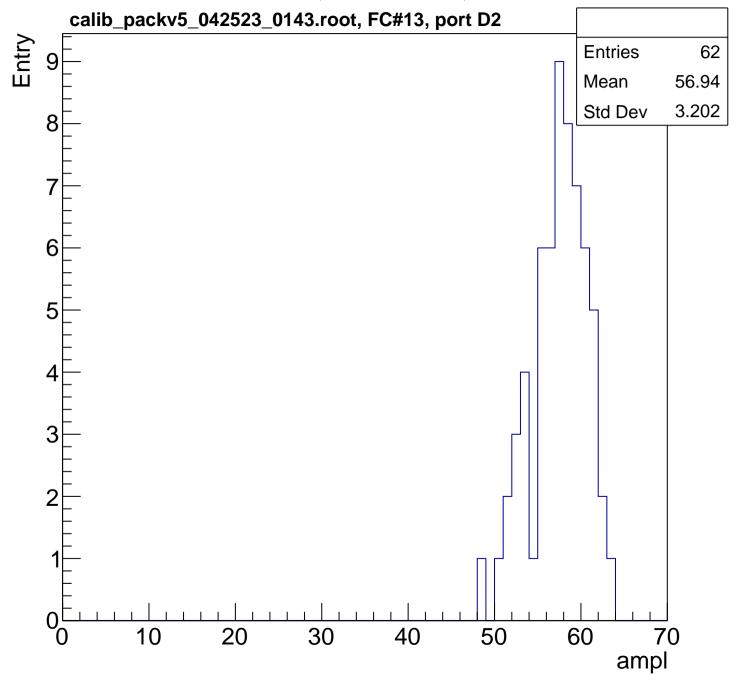


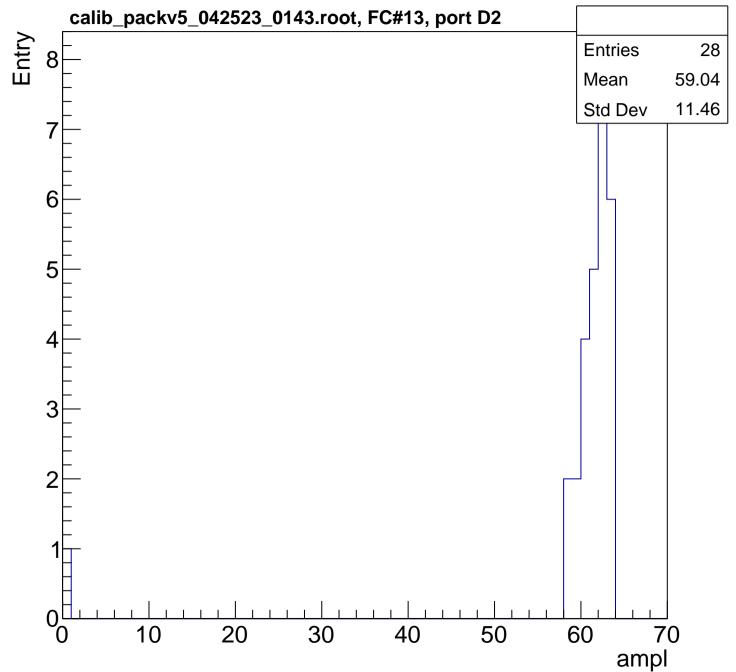


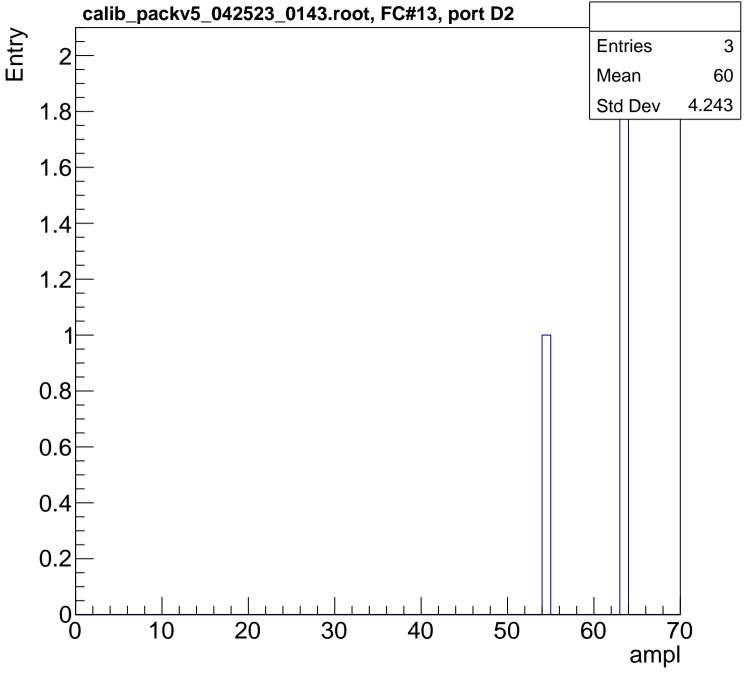


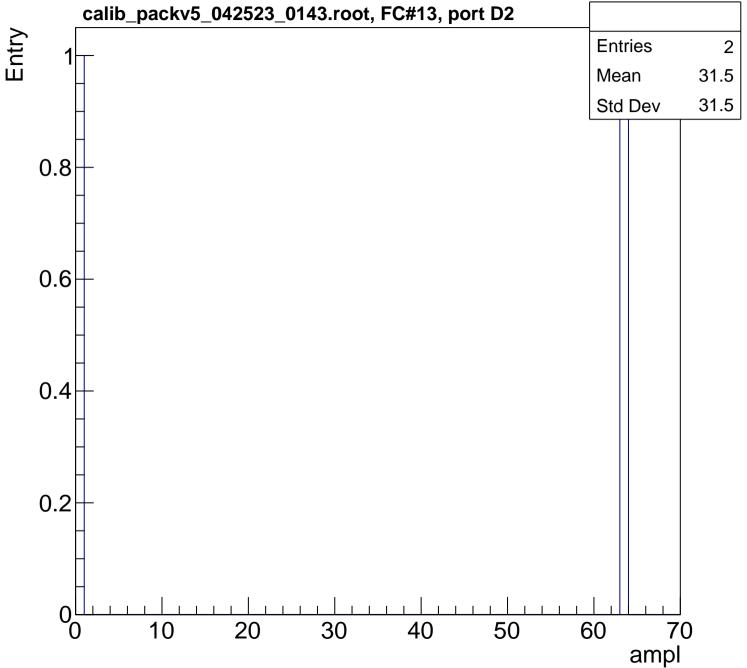


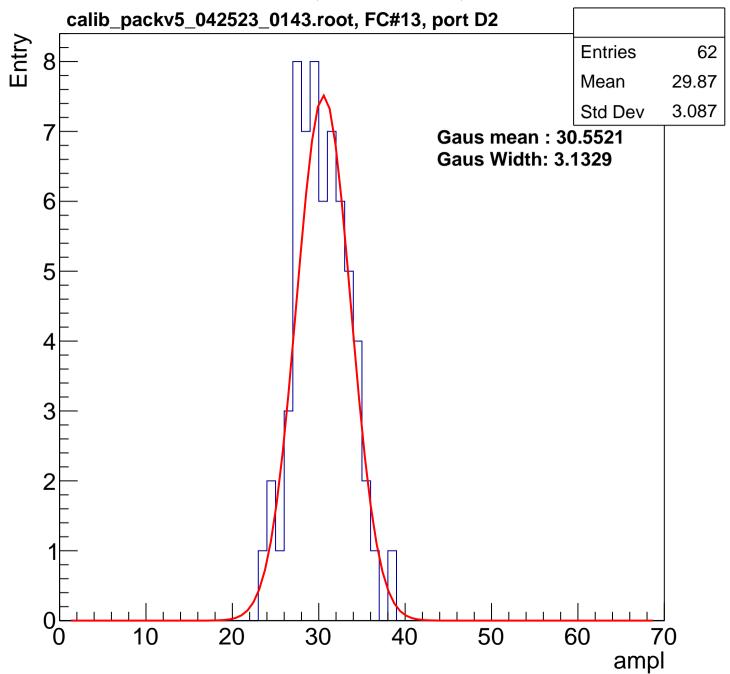


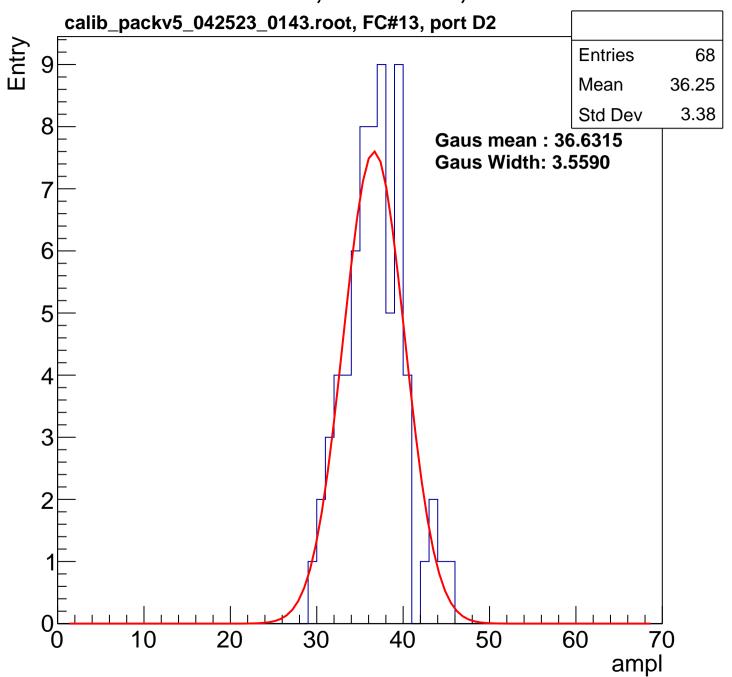


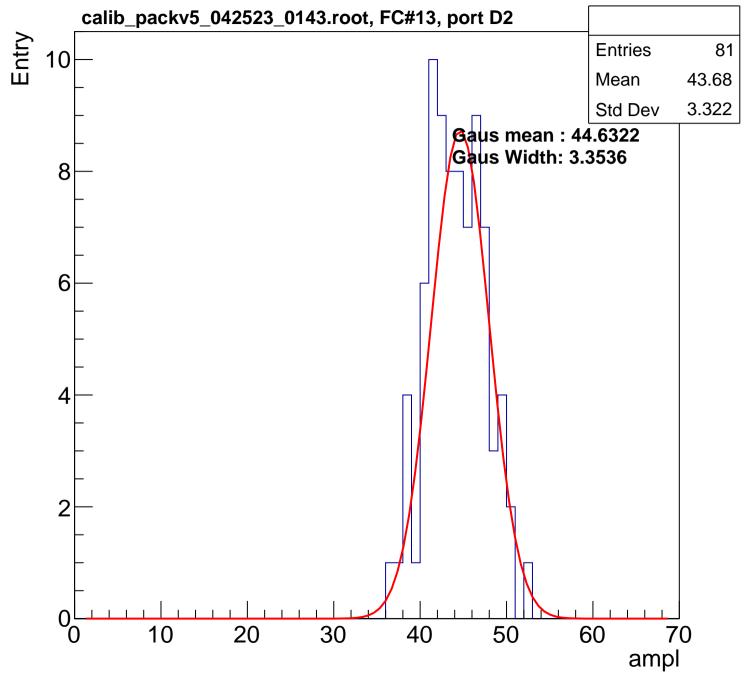


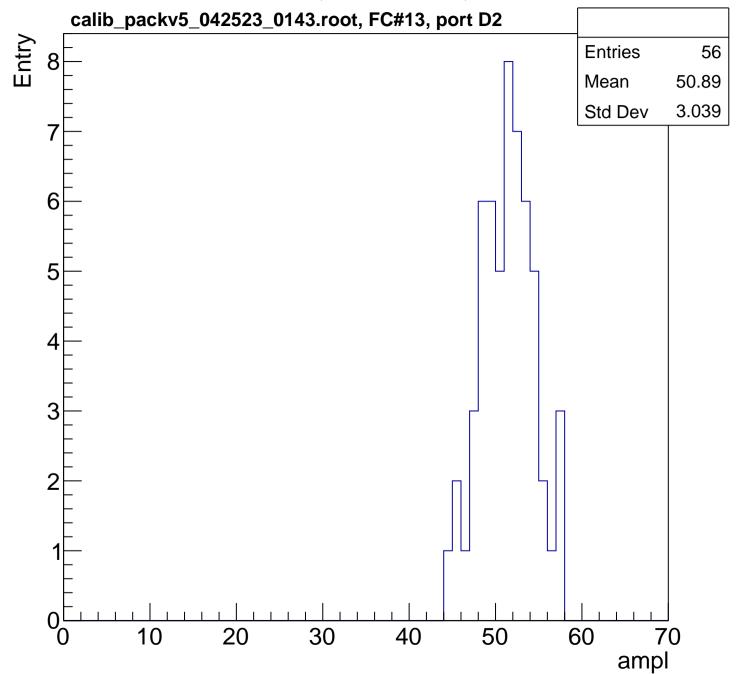


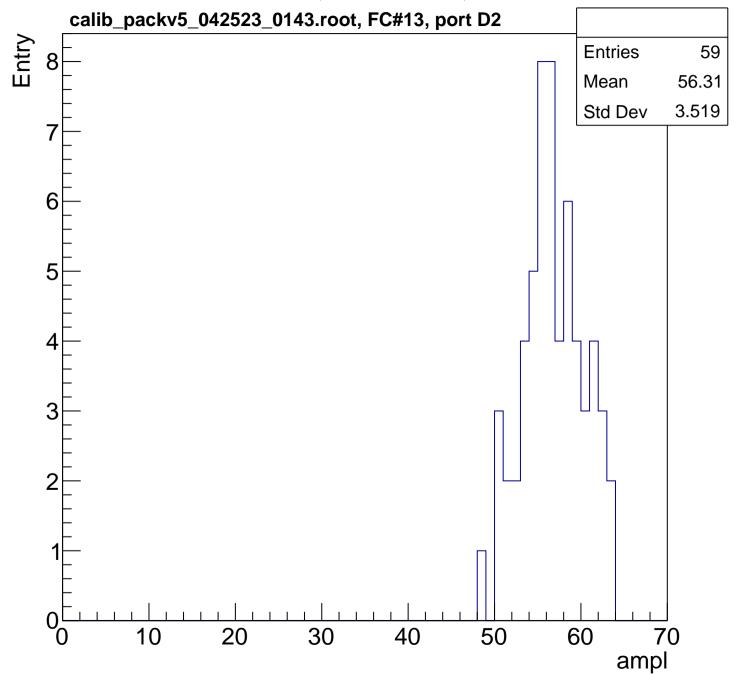


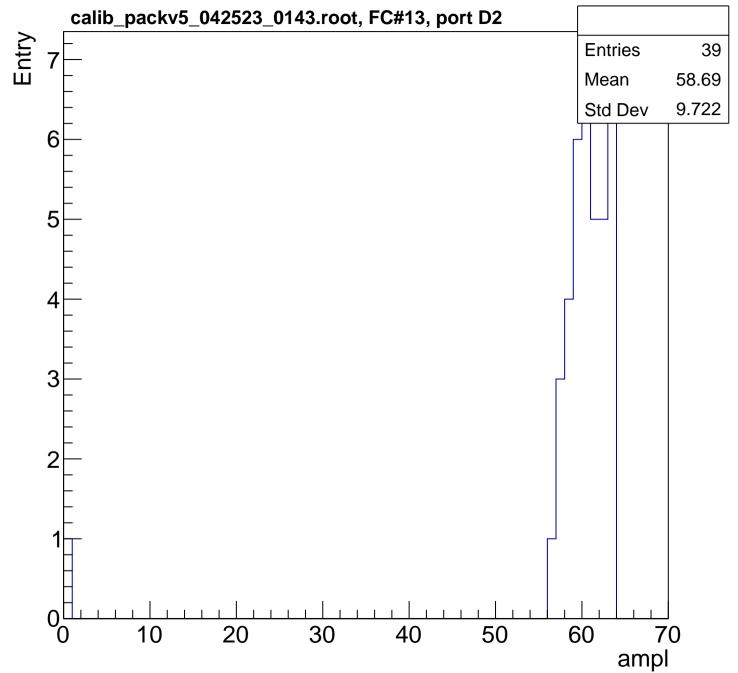


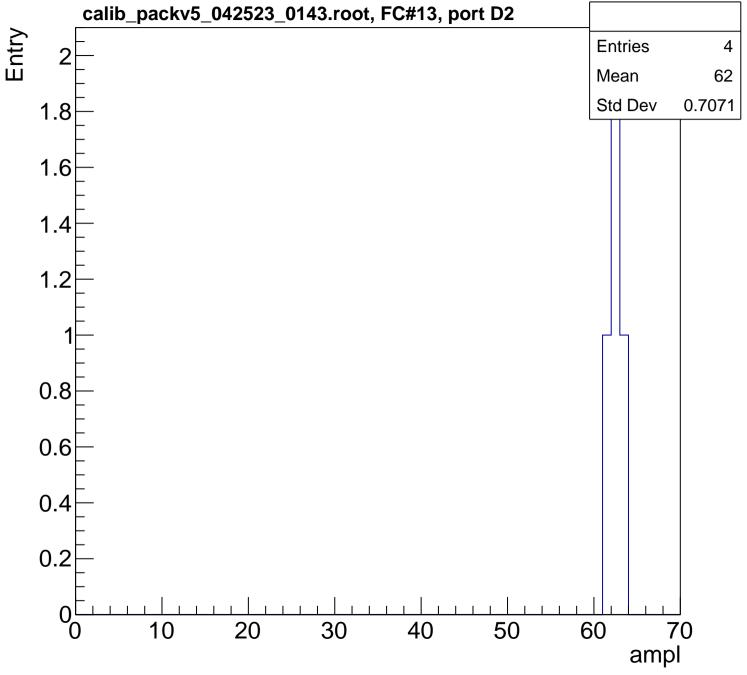




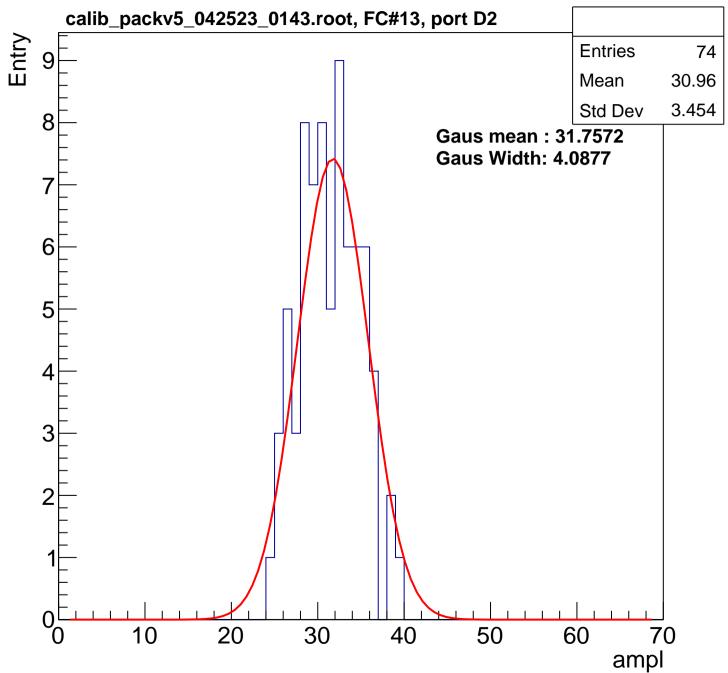


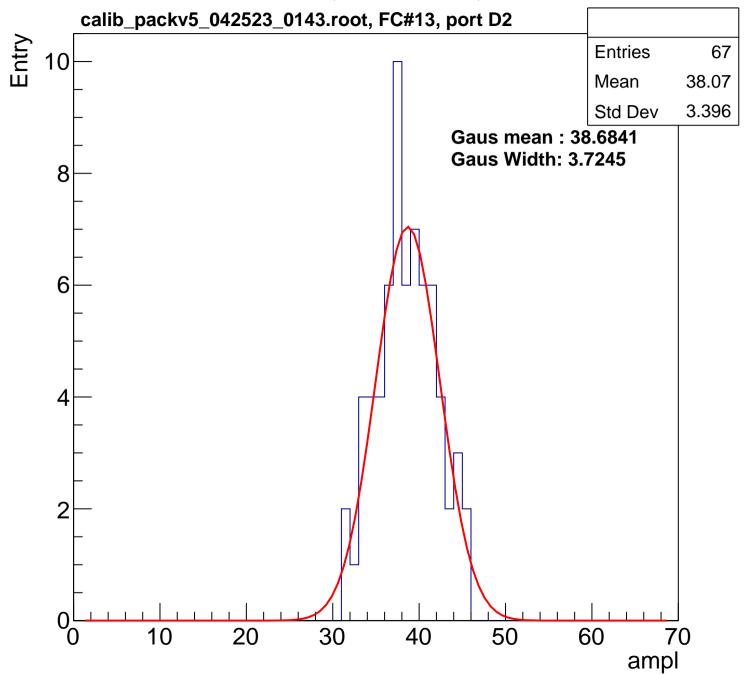


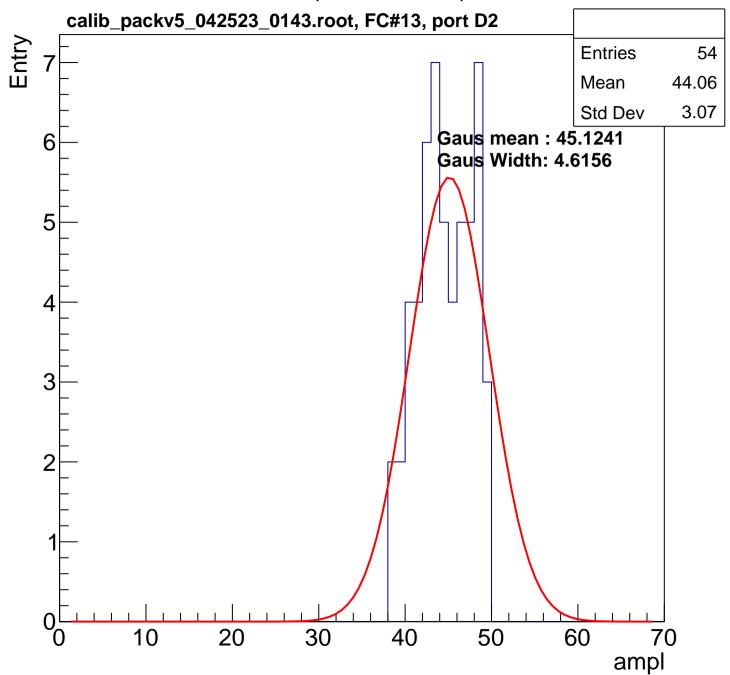


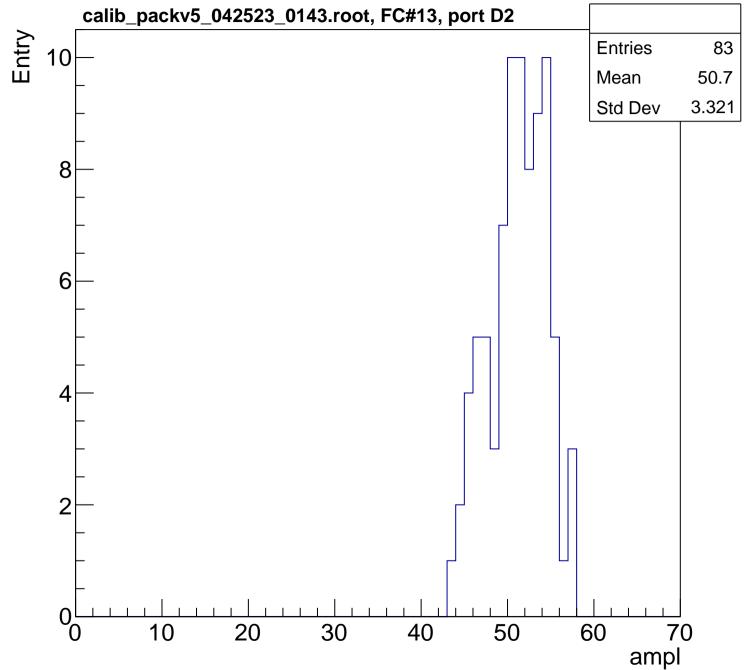


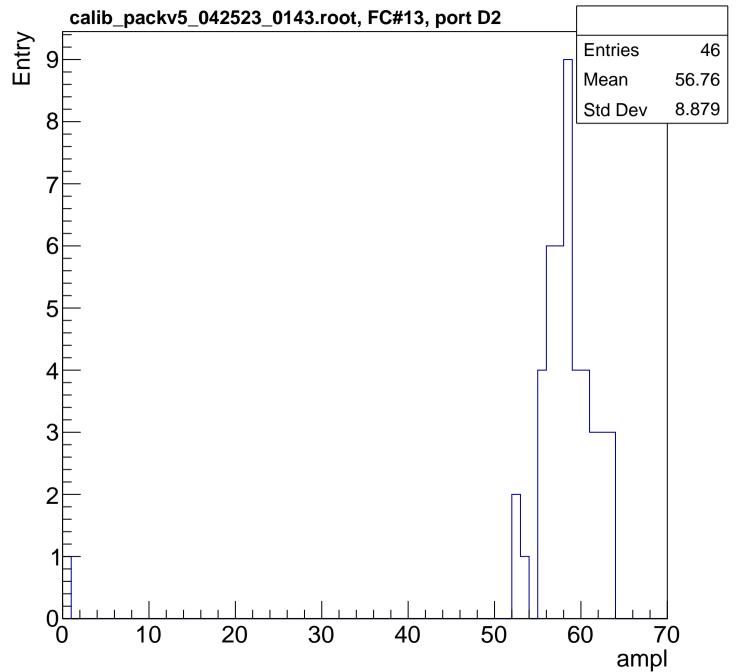
B1L003S, U8-ch54, adc7 calib\_packv5\_042523\_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

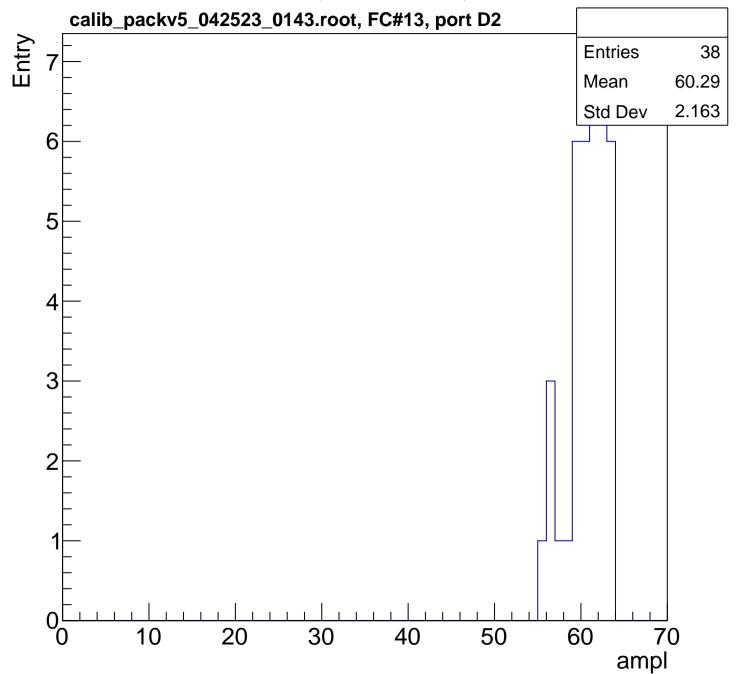


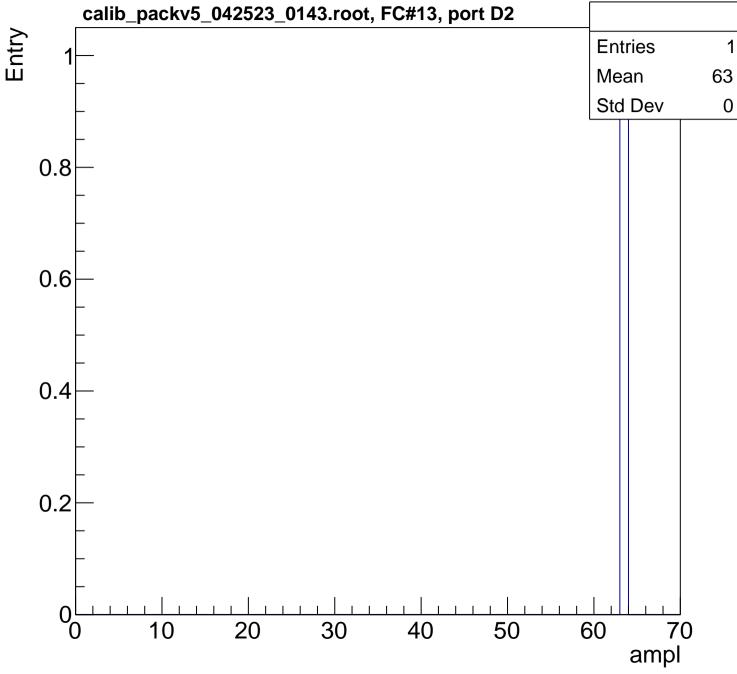




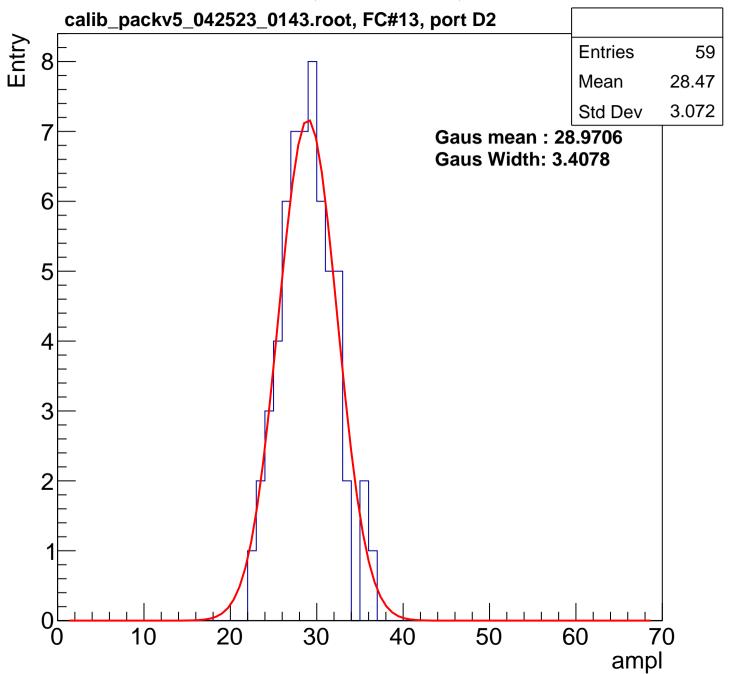


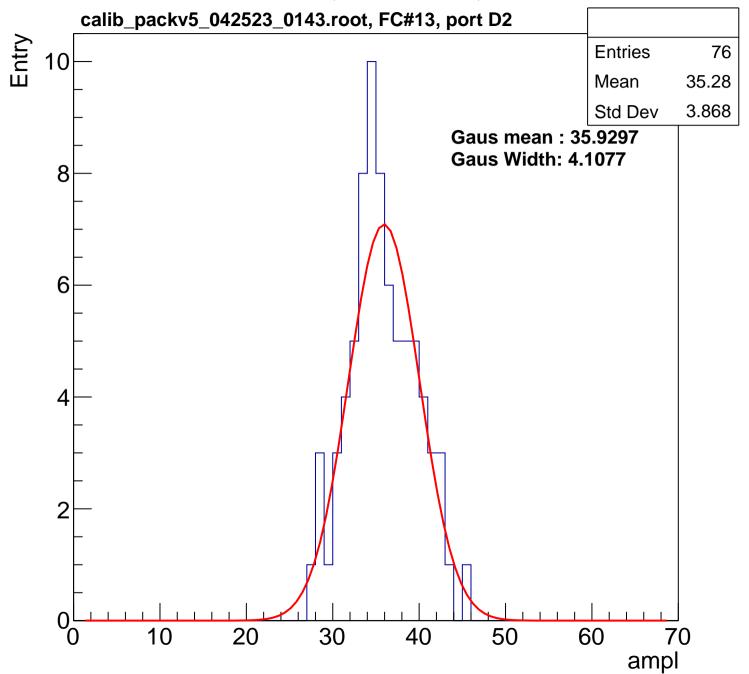


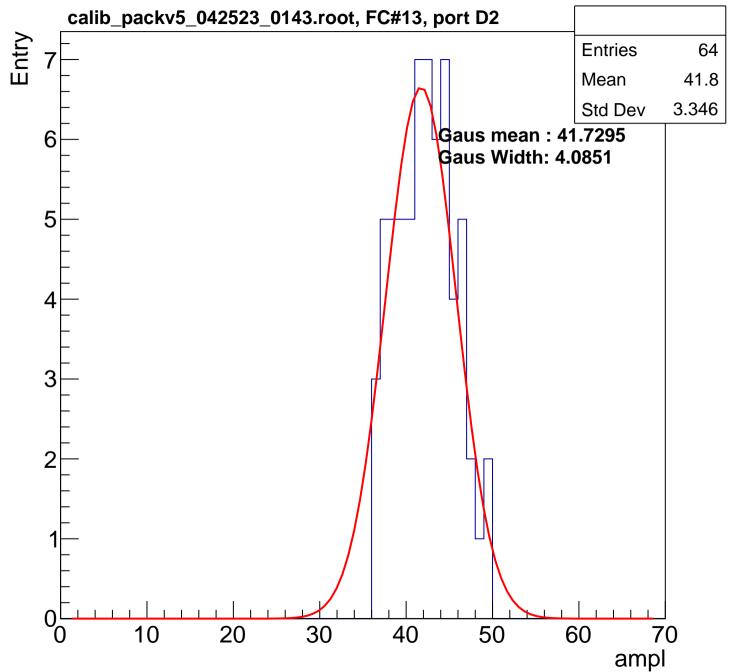


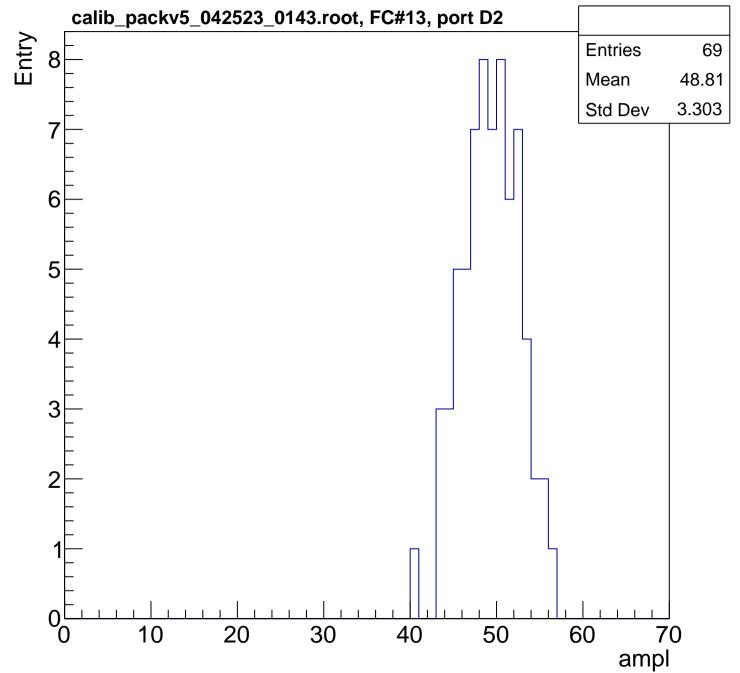


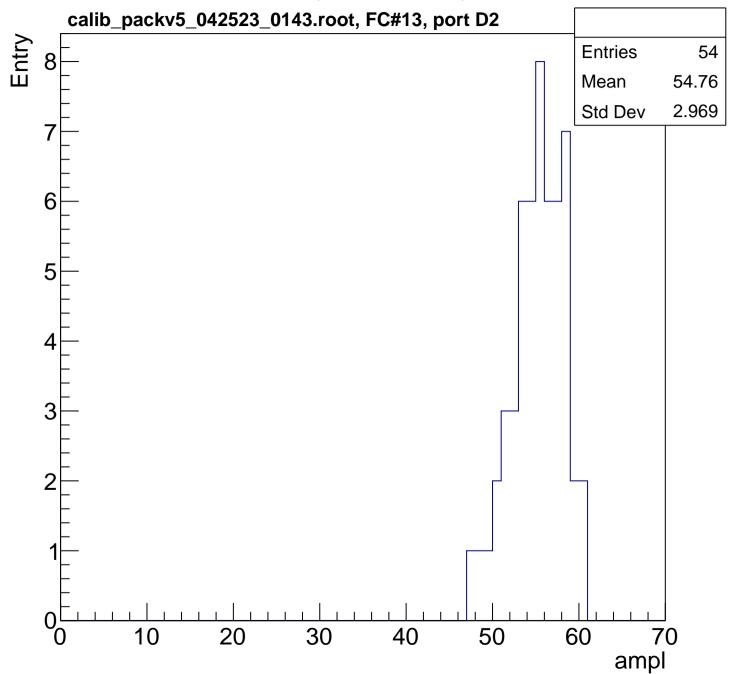
B1L003S, U8-ch55, adc7 calib\_packv5\_042523\_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

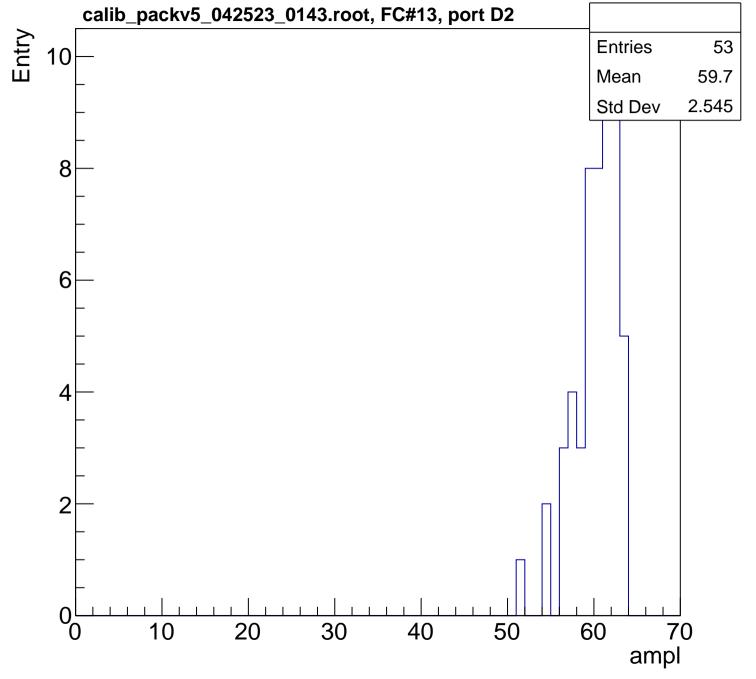


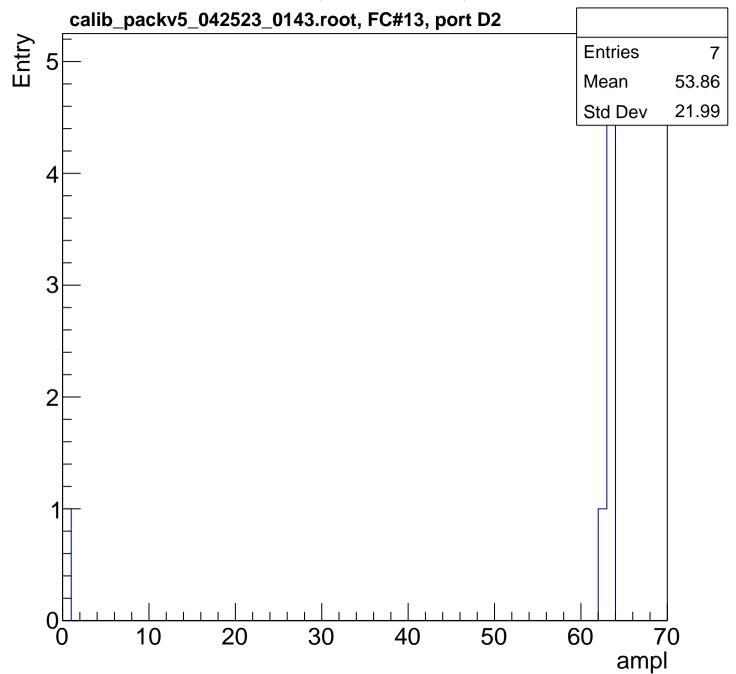




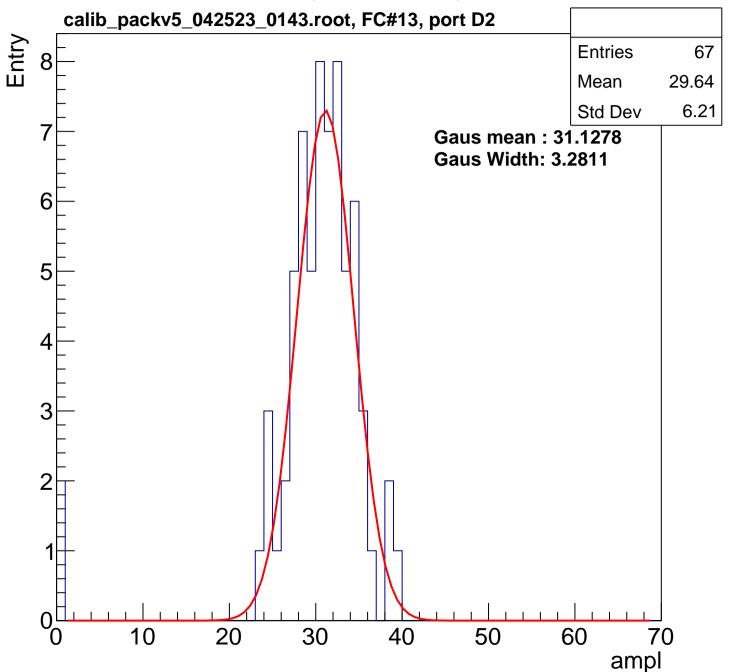


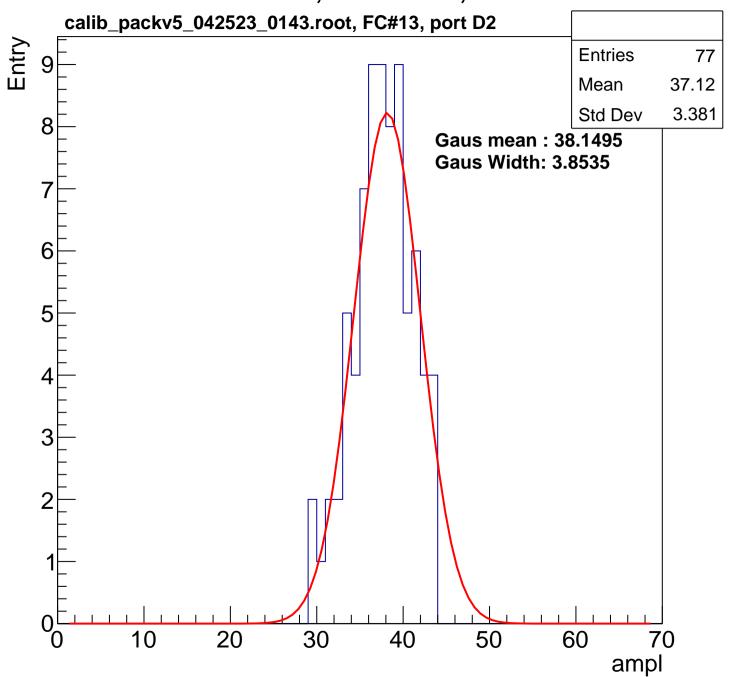


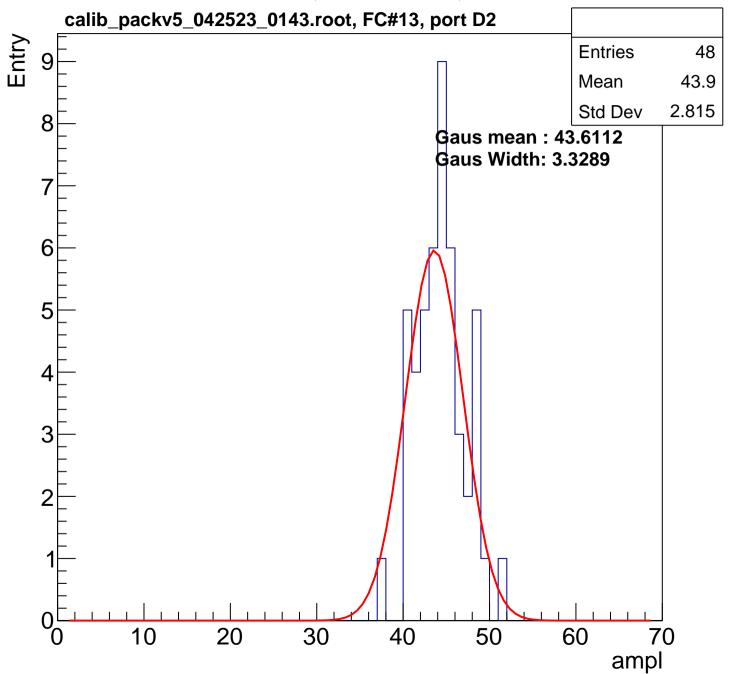


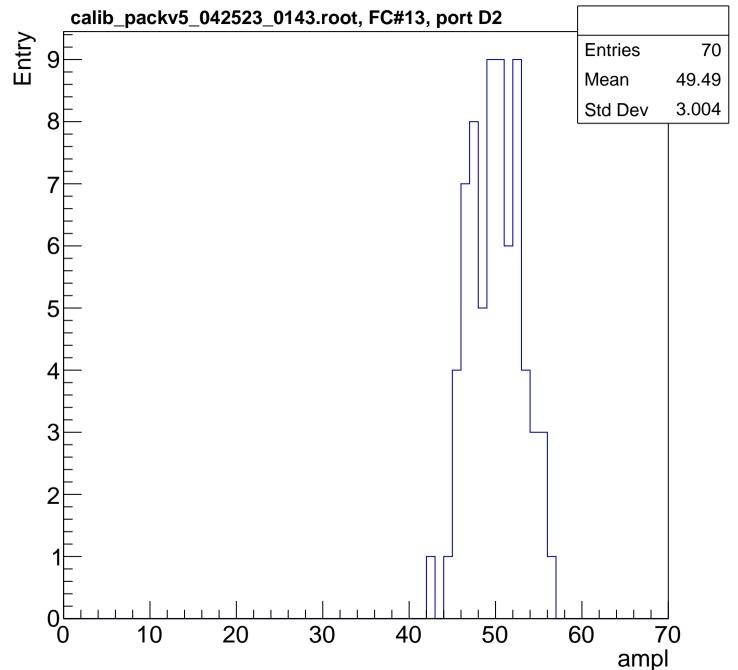


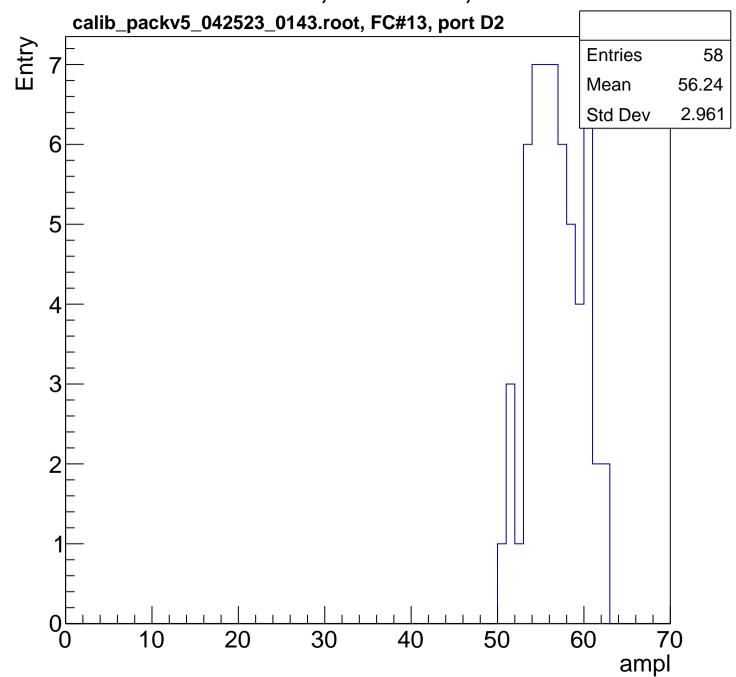


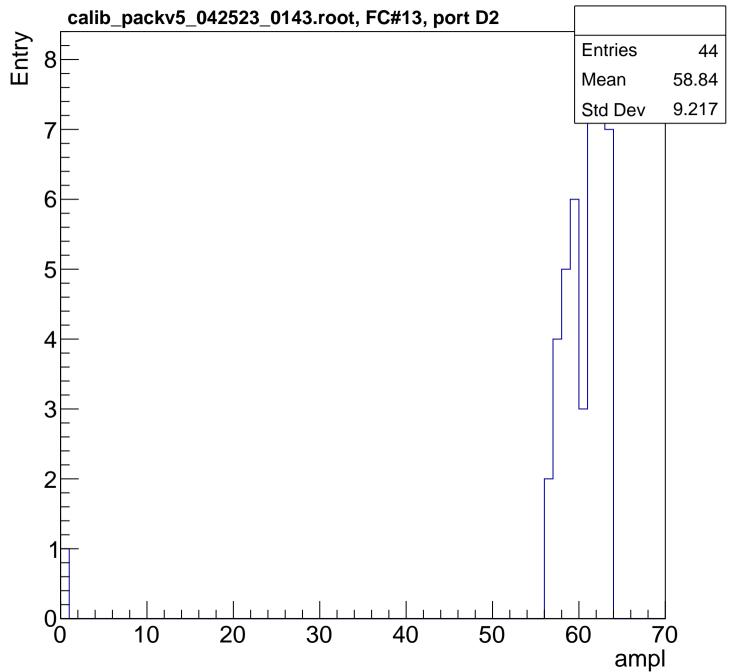


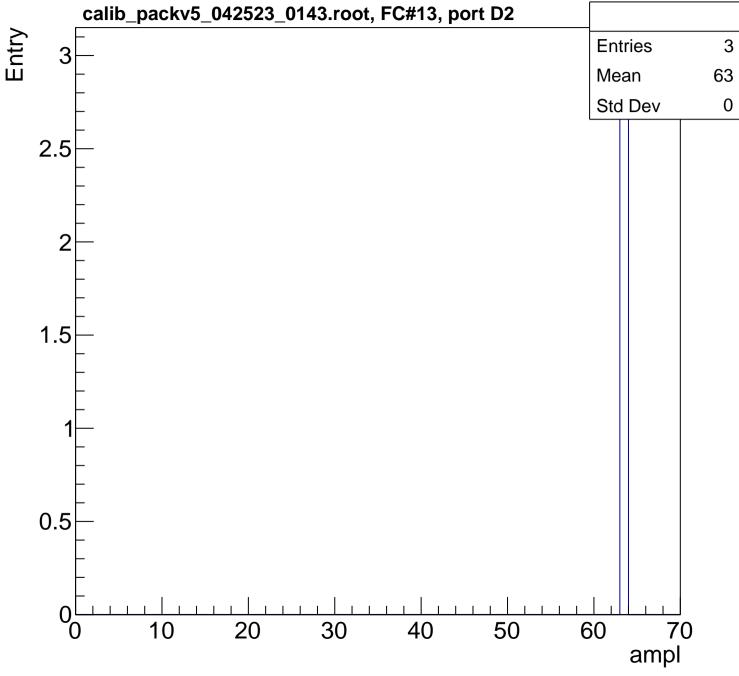


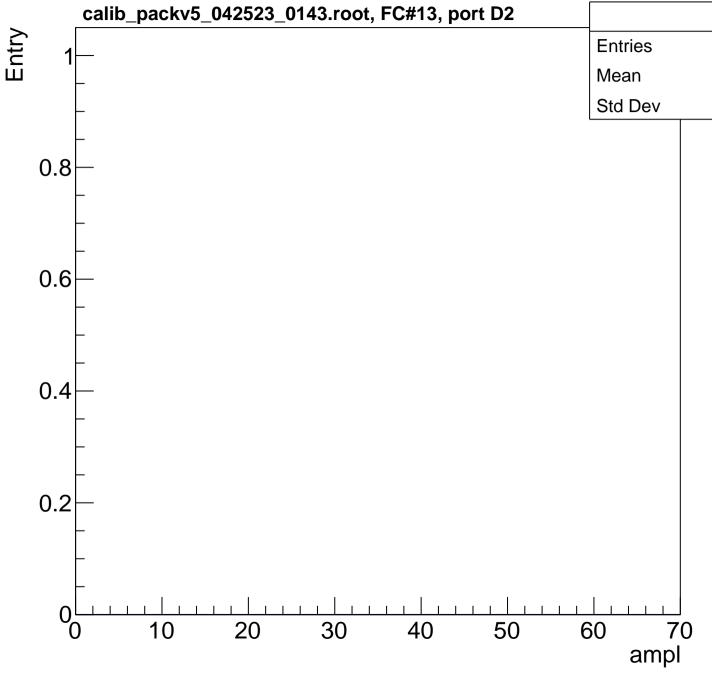


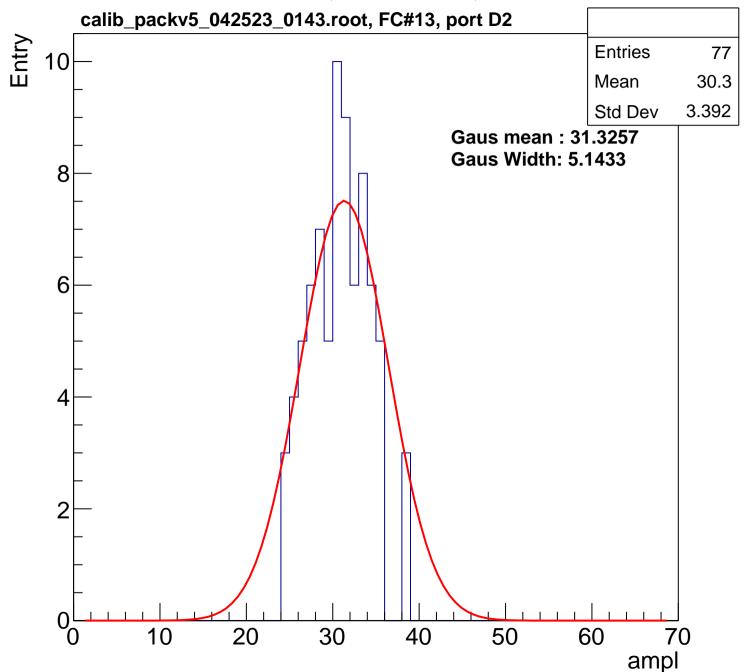


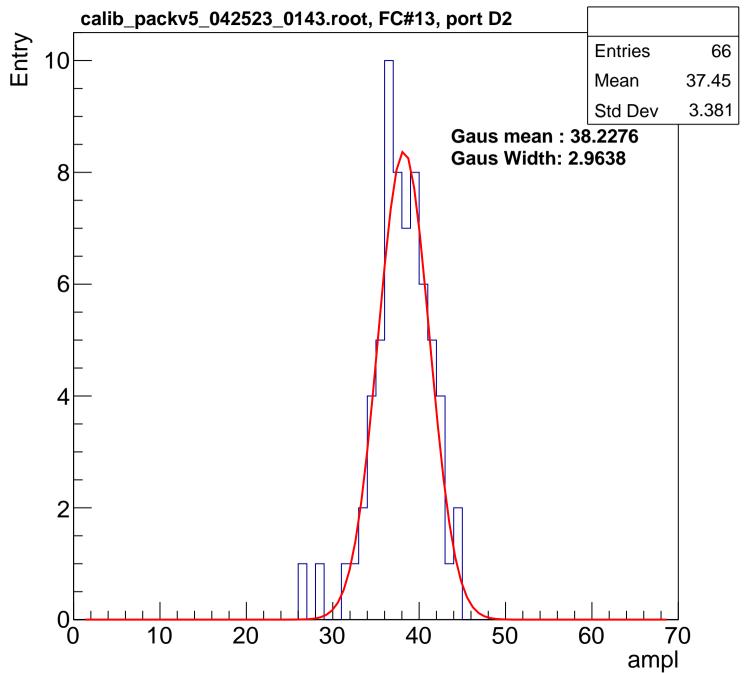


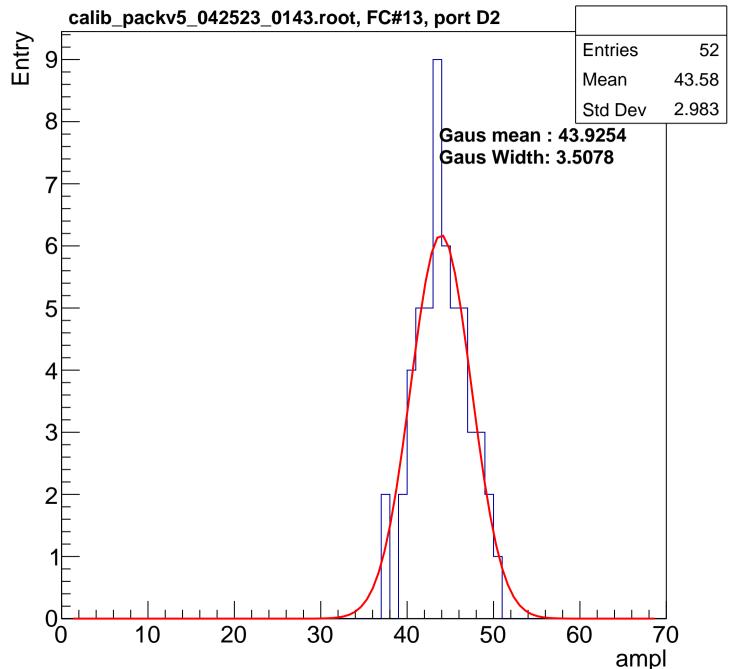


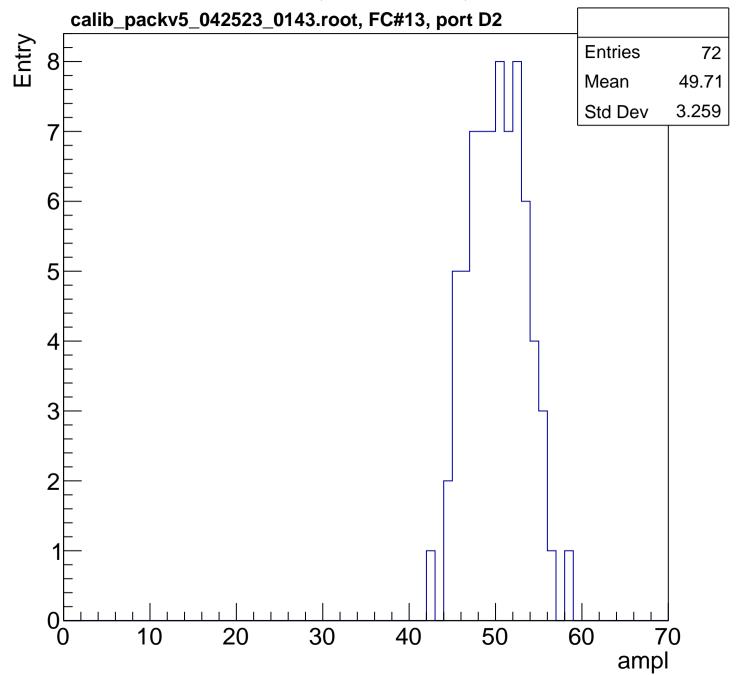


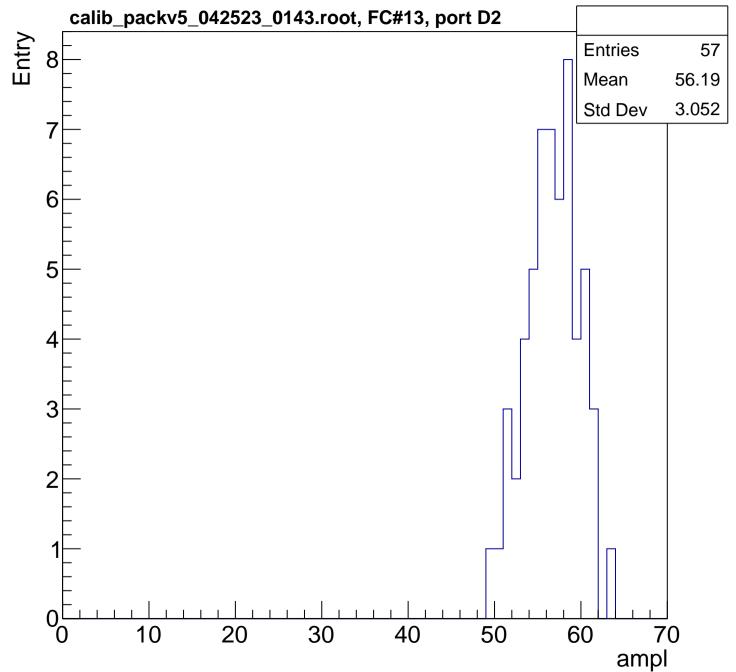


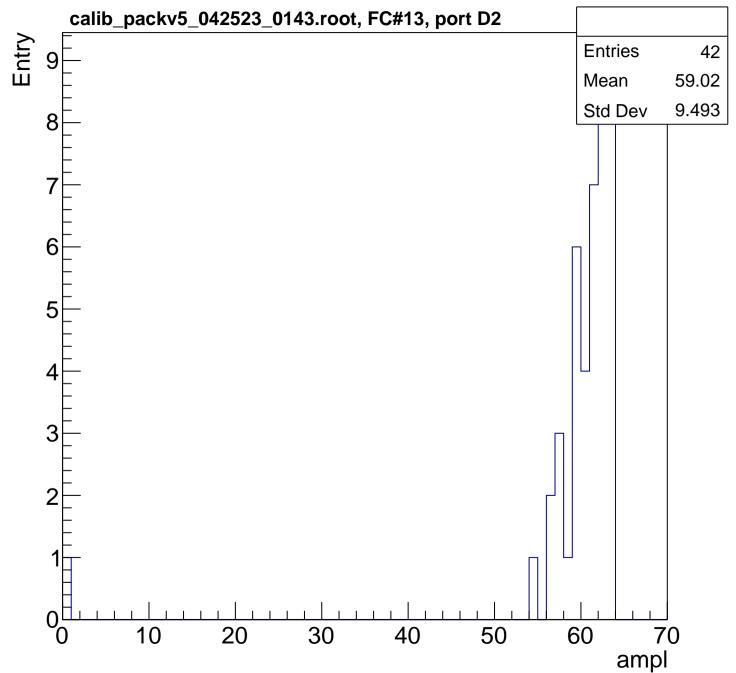


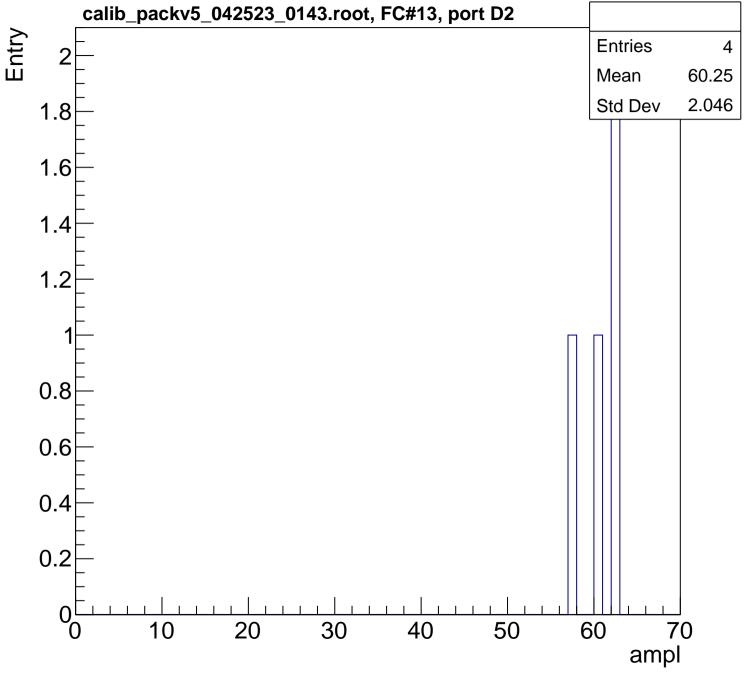




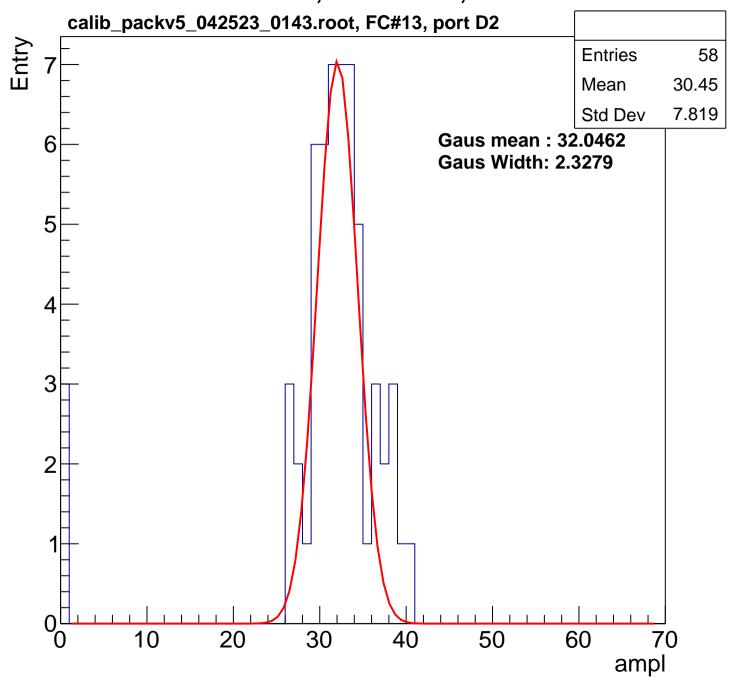


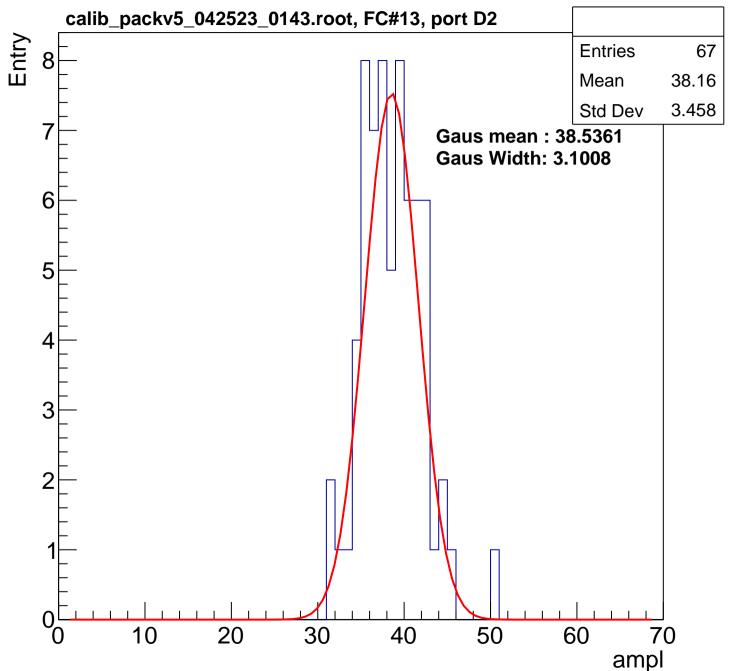


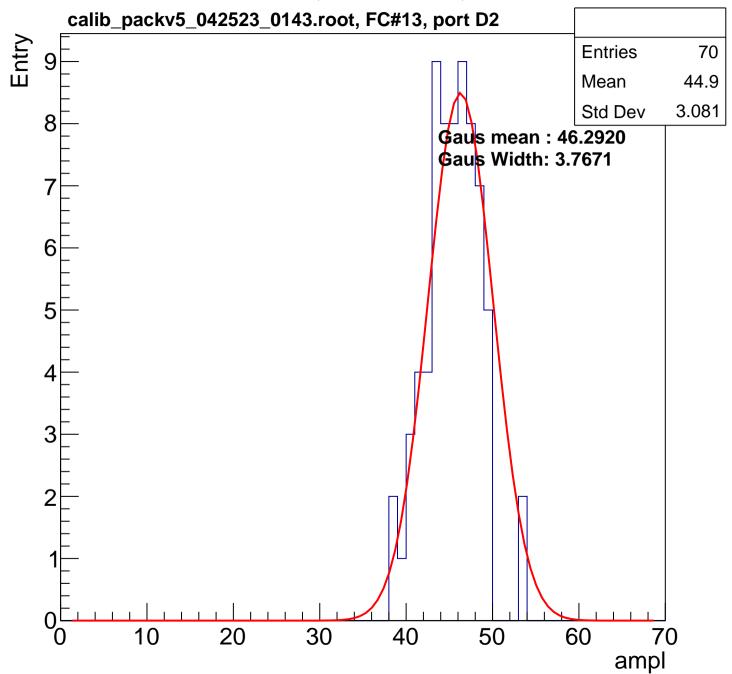


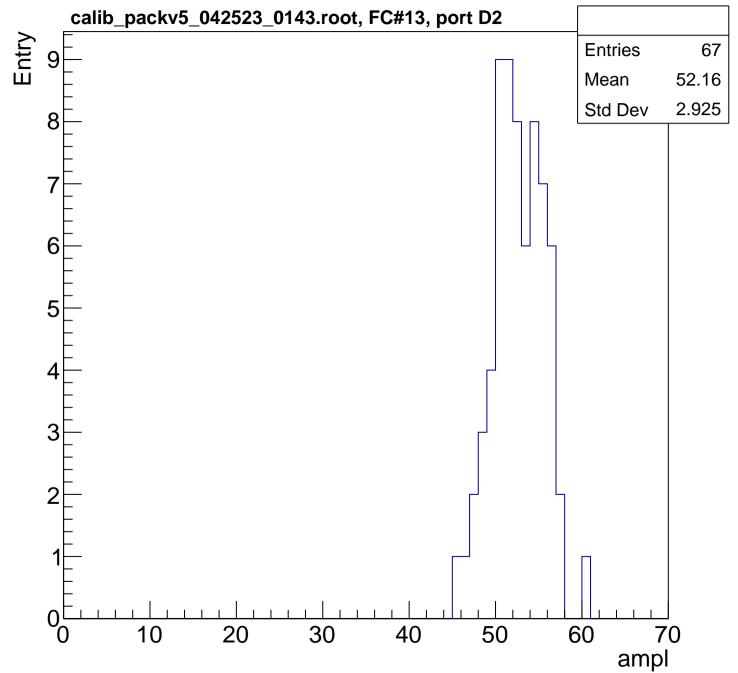


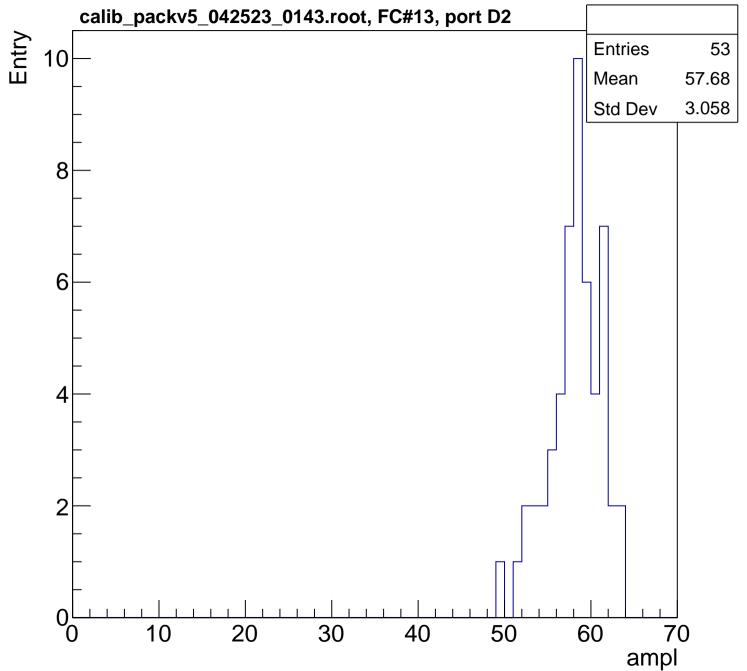
B1L003S, U8-ch58, adc7 calib\_packv5\_042523\_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

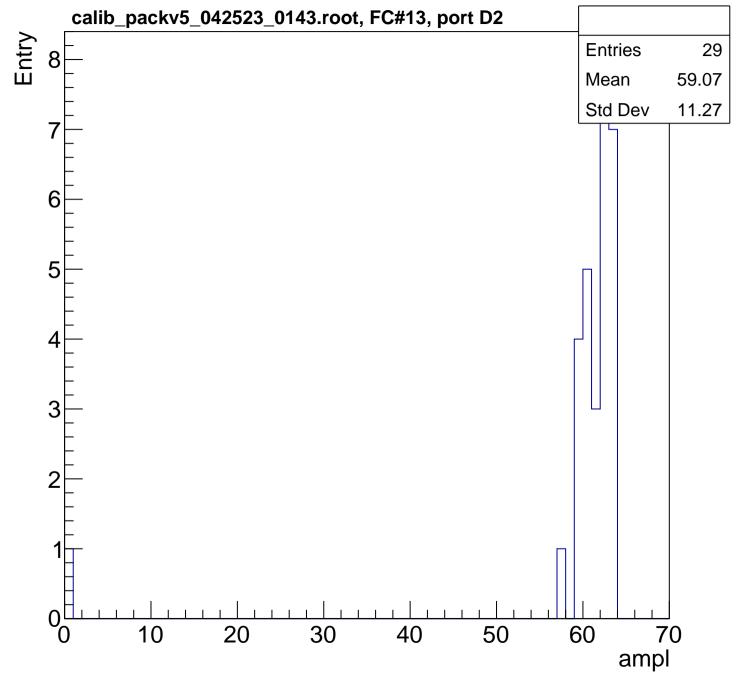


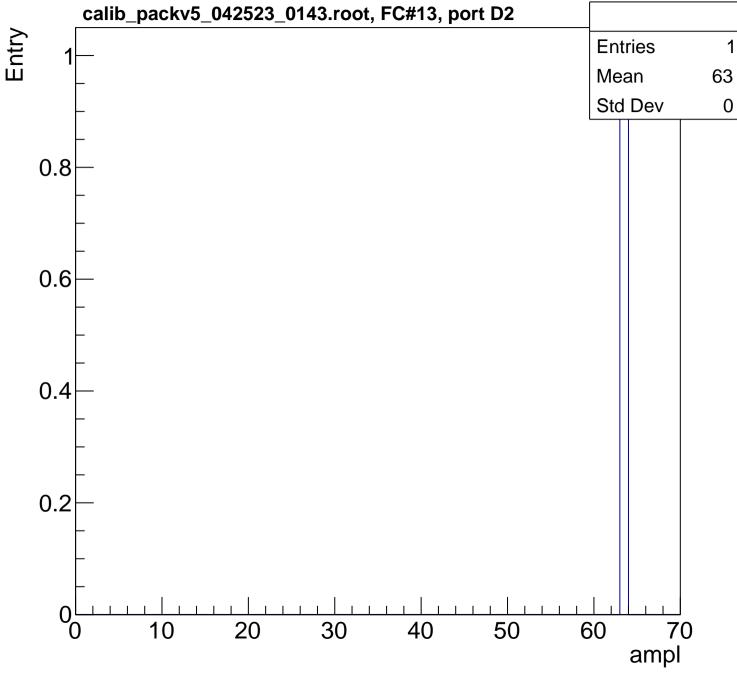




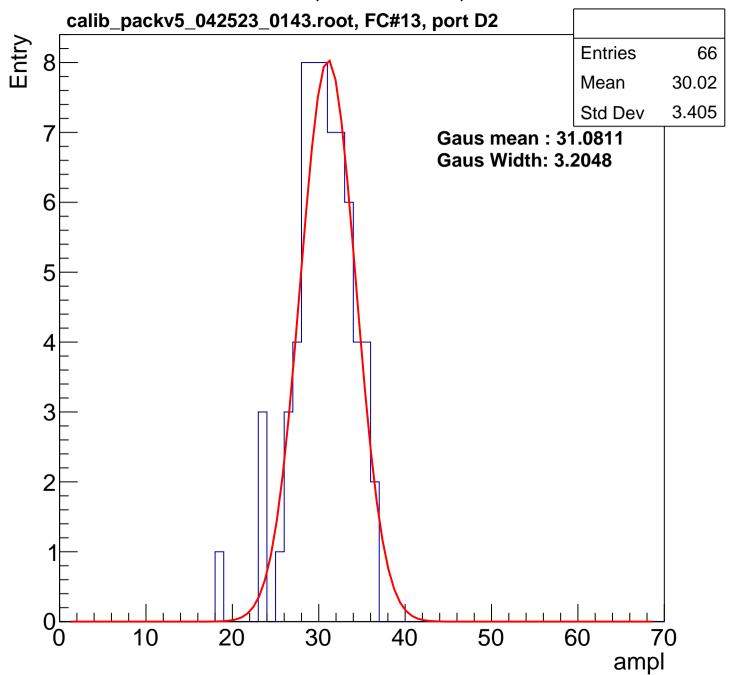


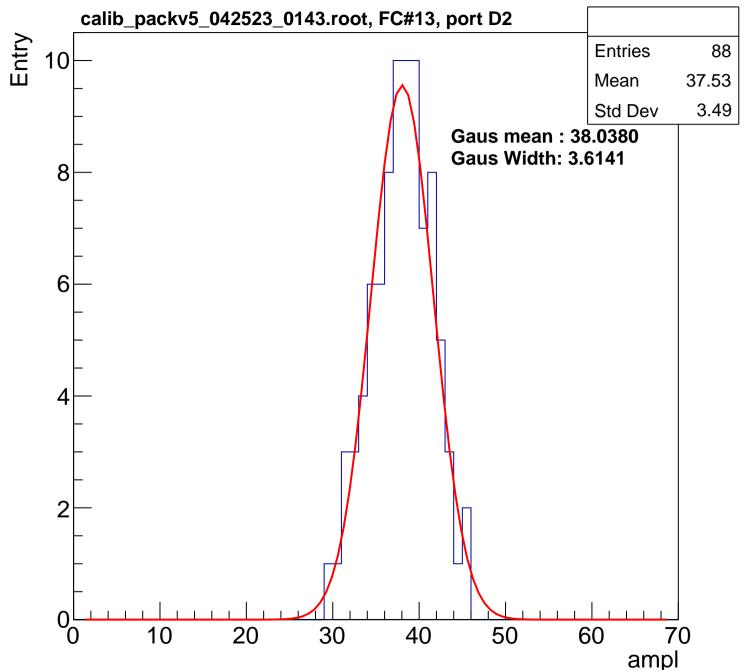


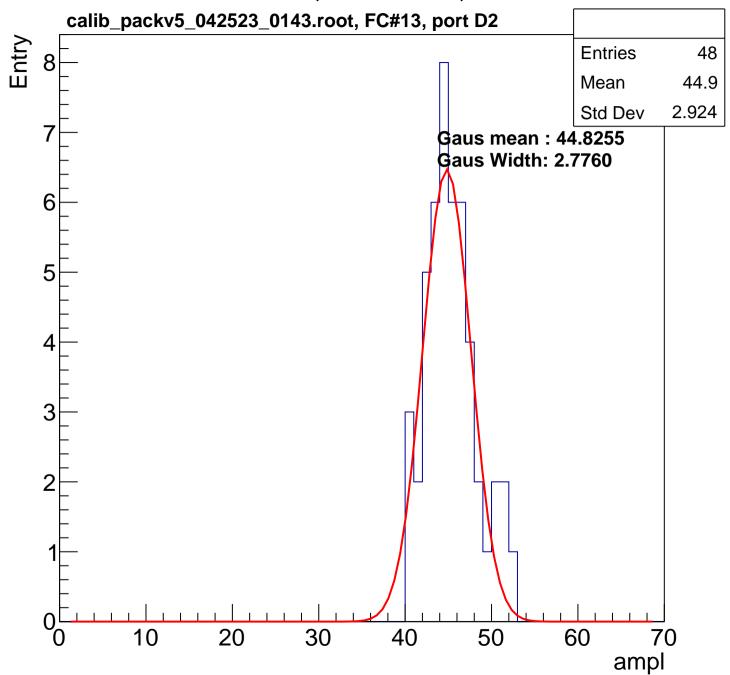


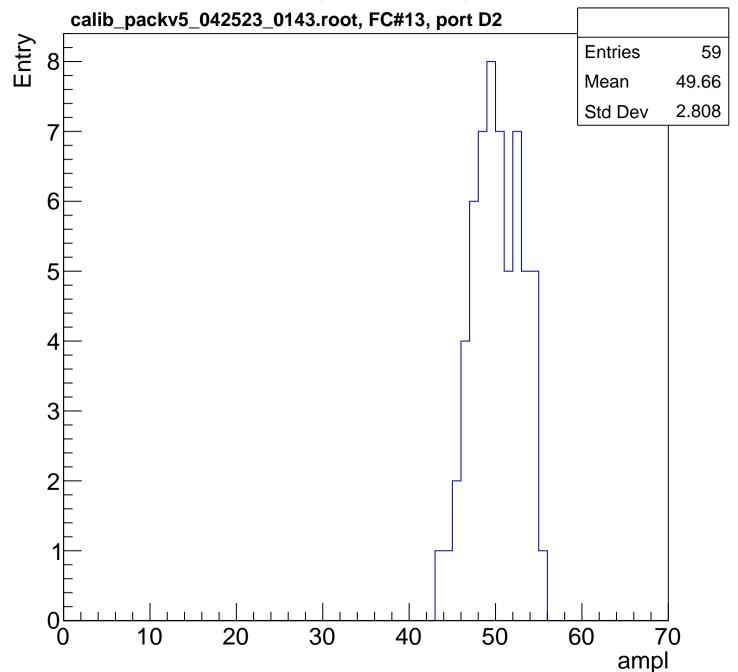


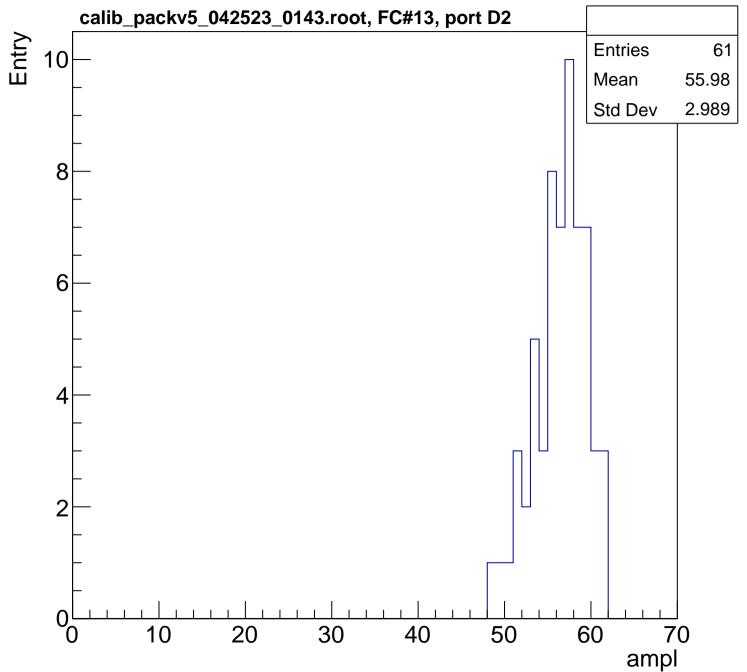


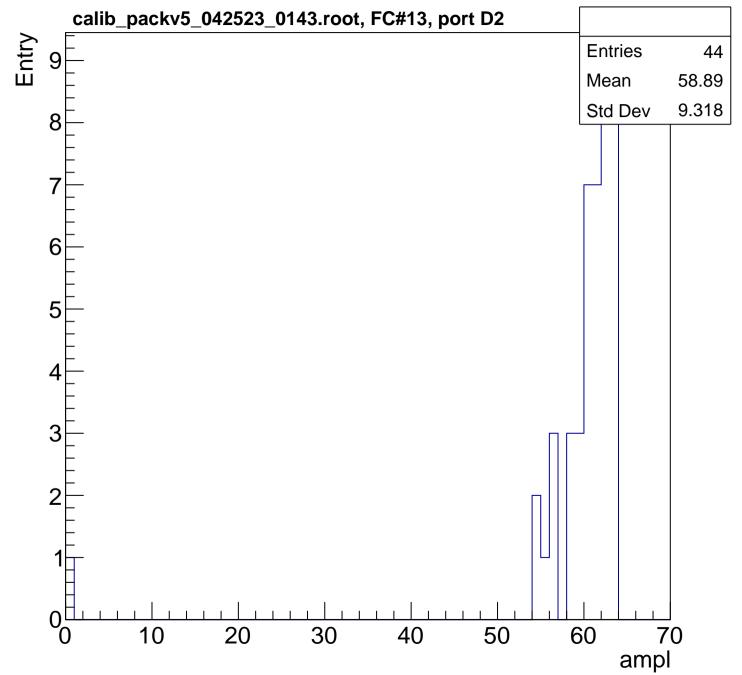


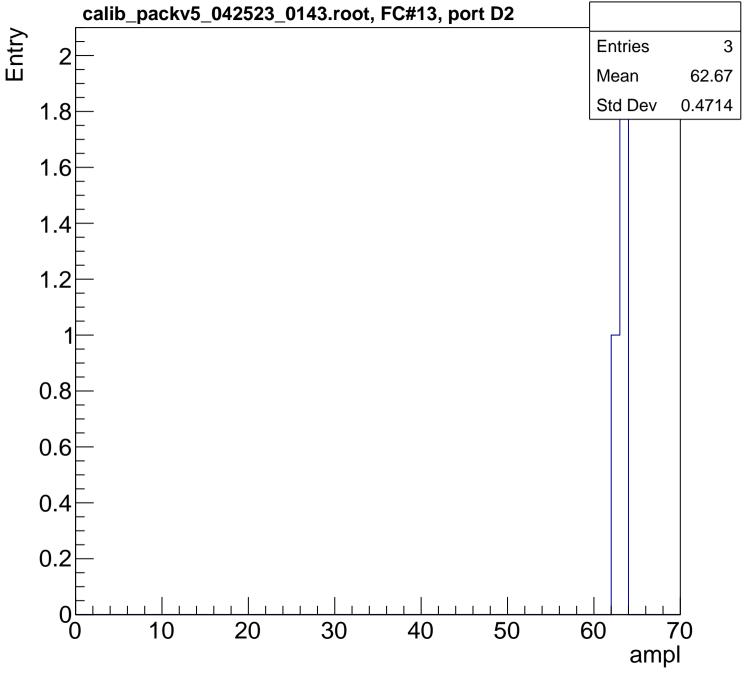


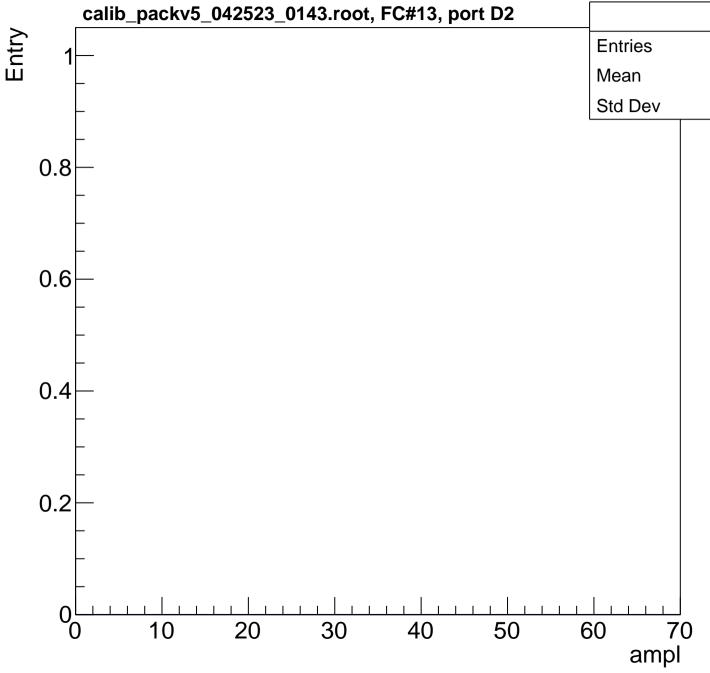


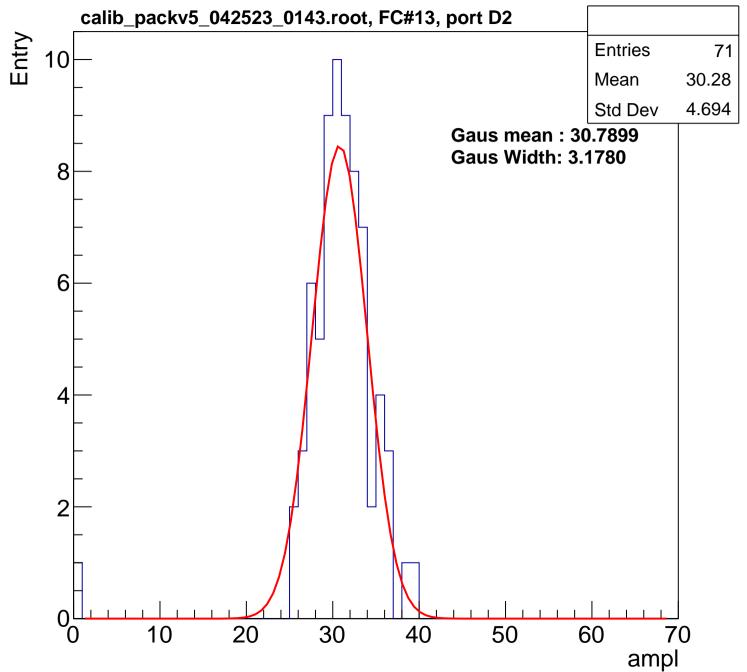


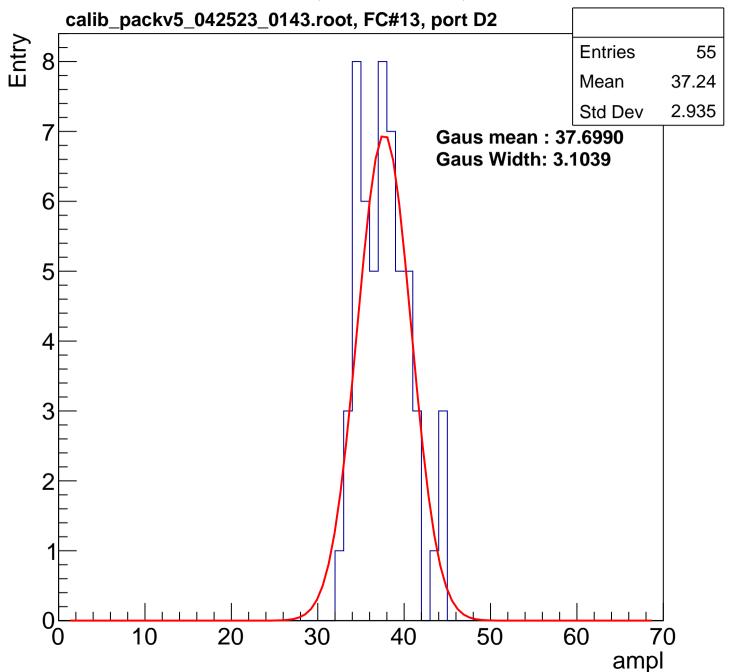


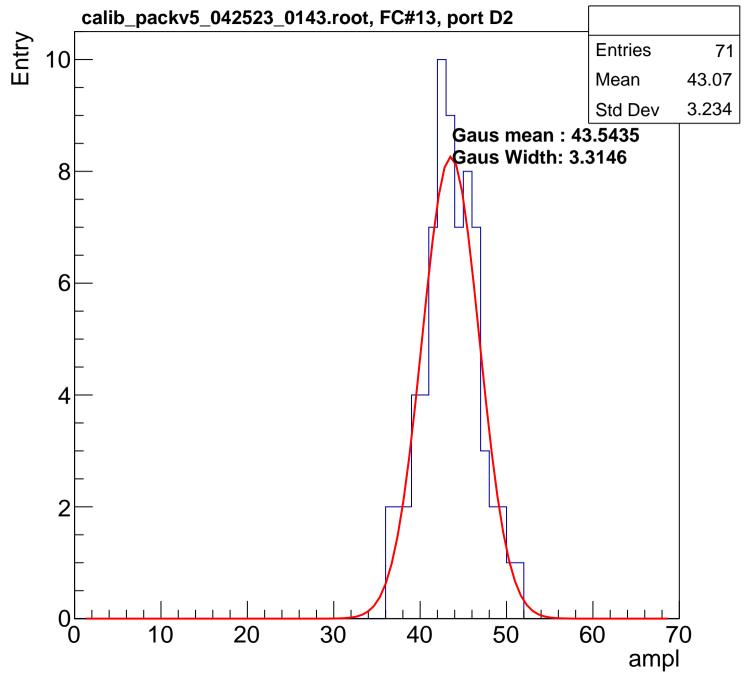


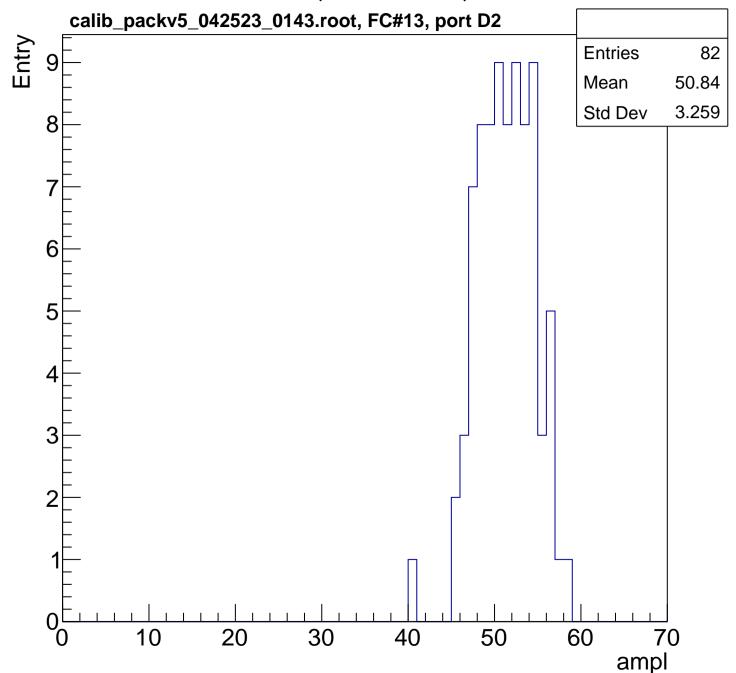


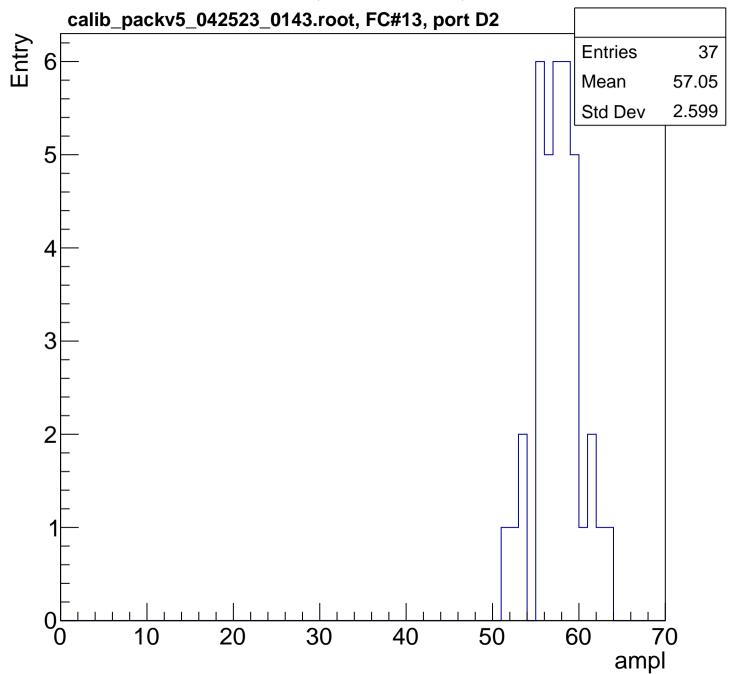


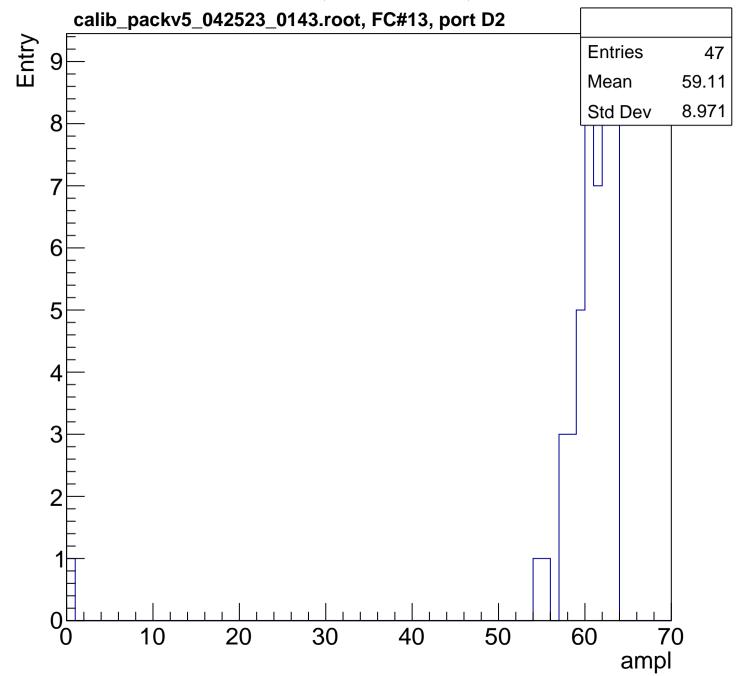


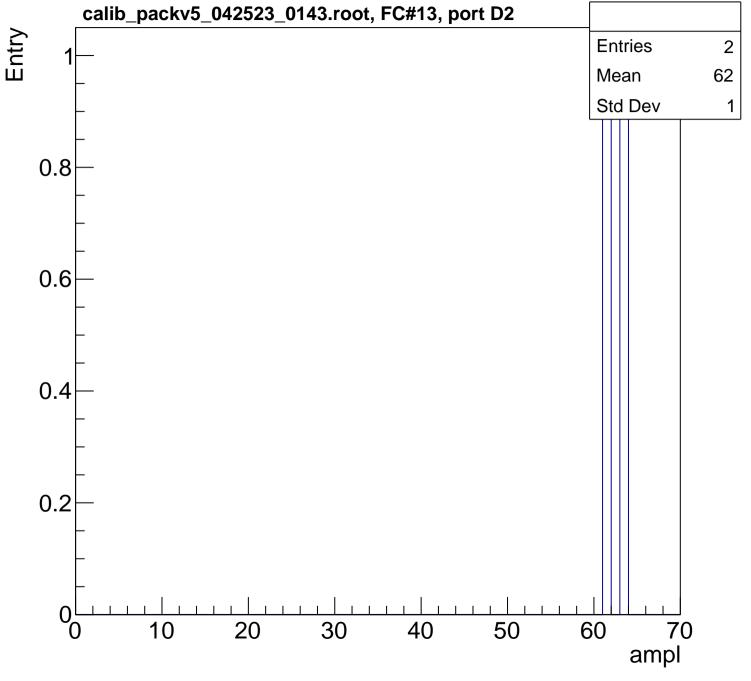




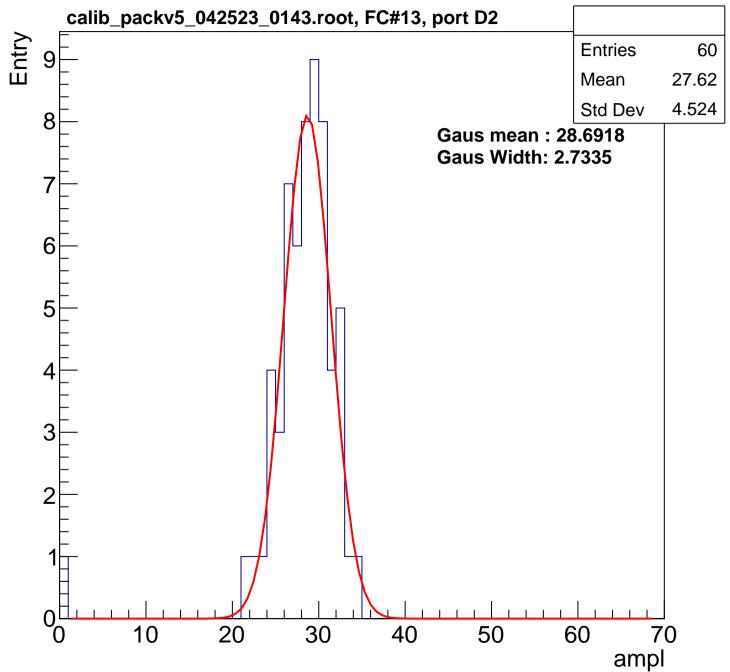


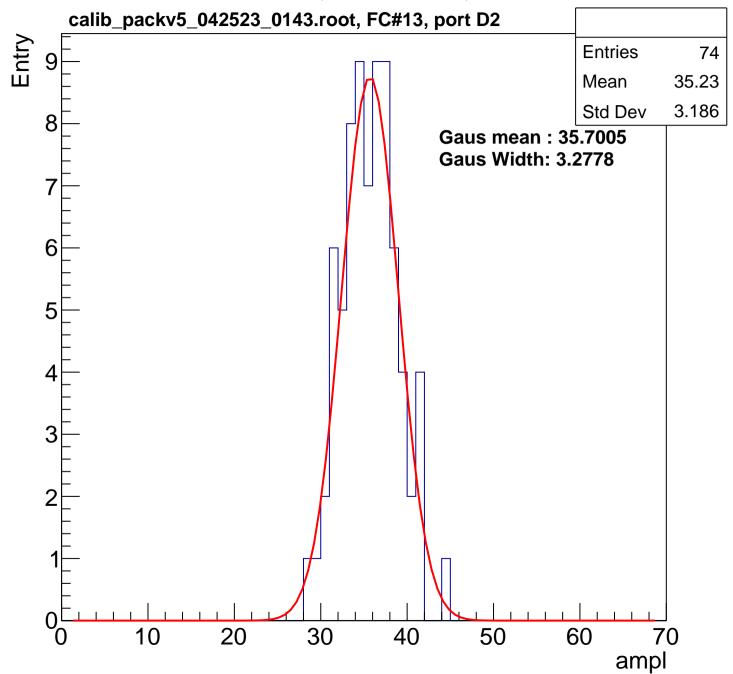


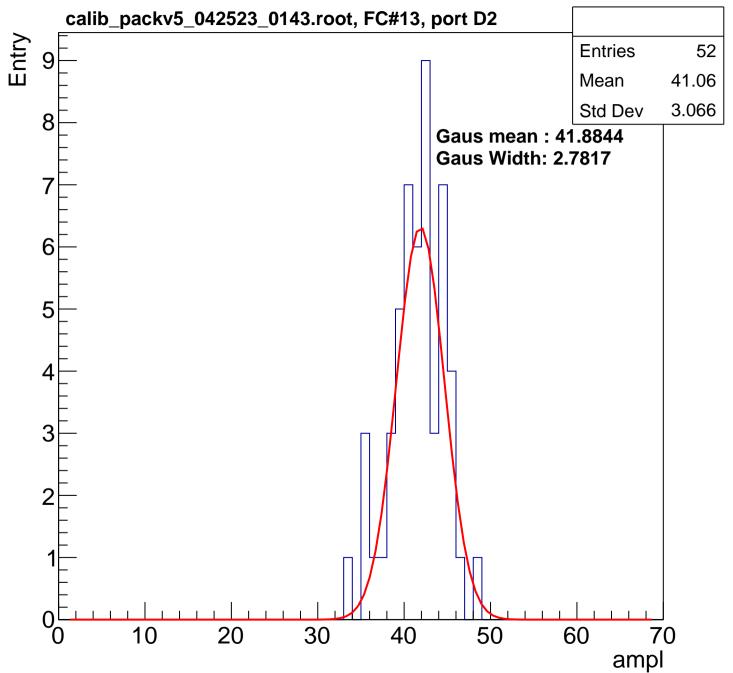


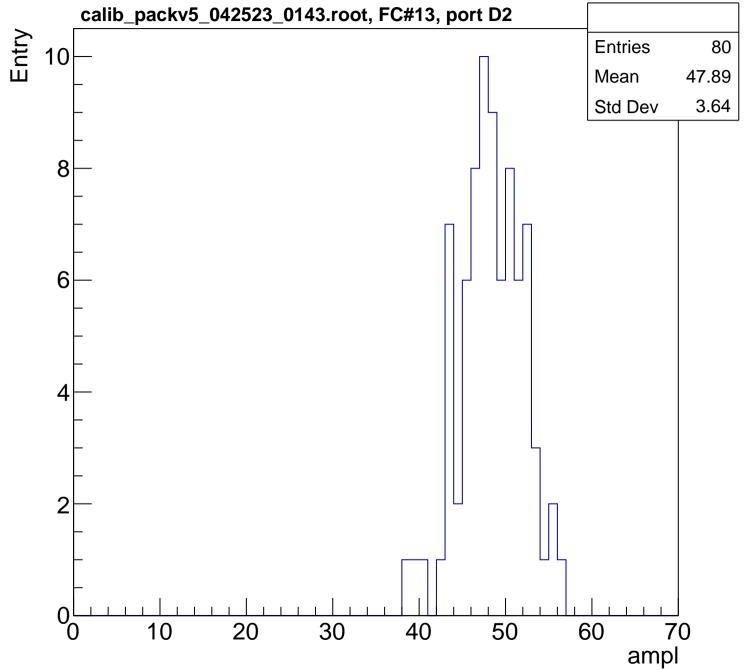


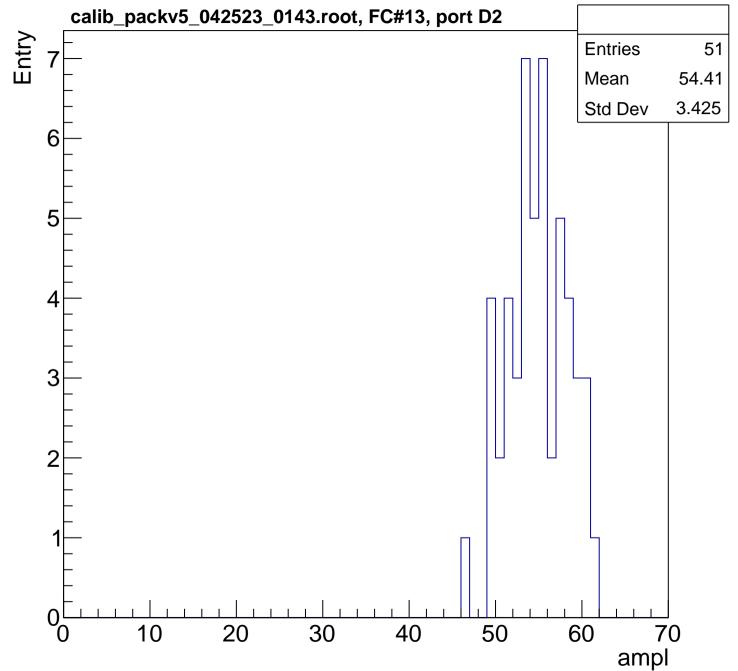


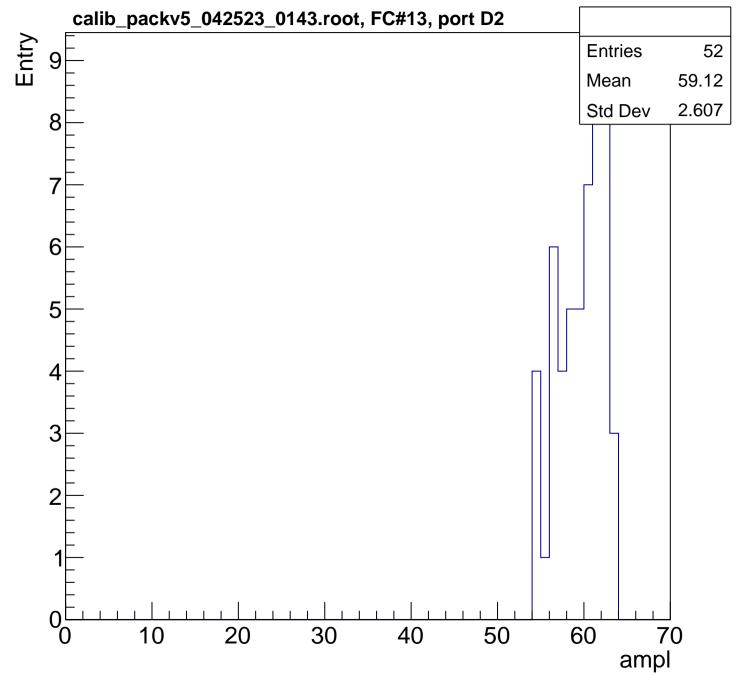


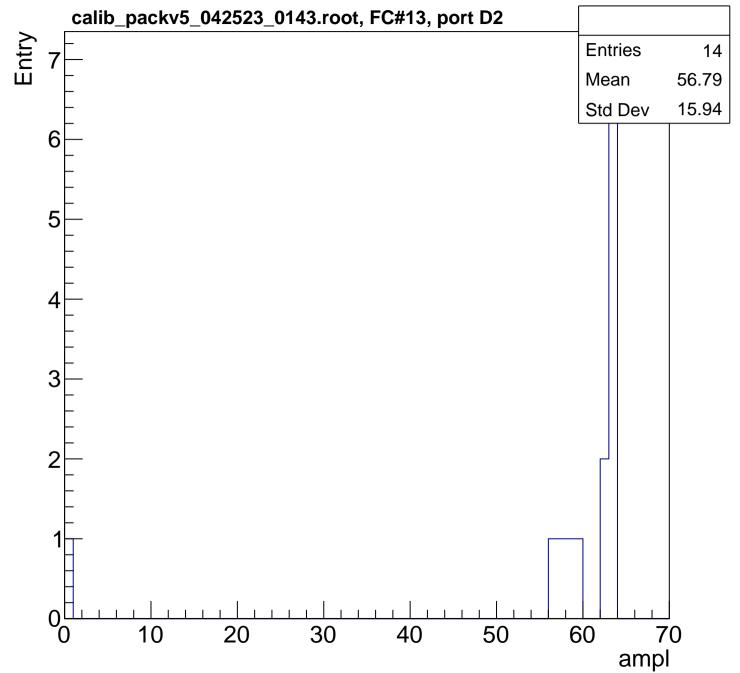


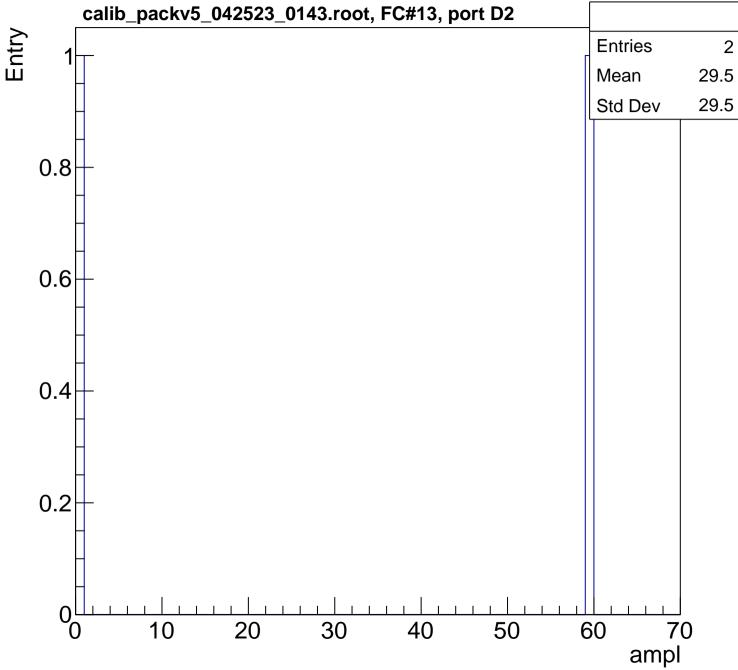


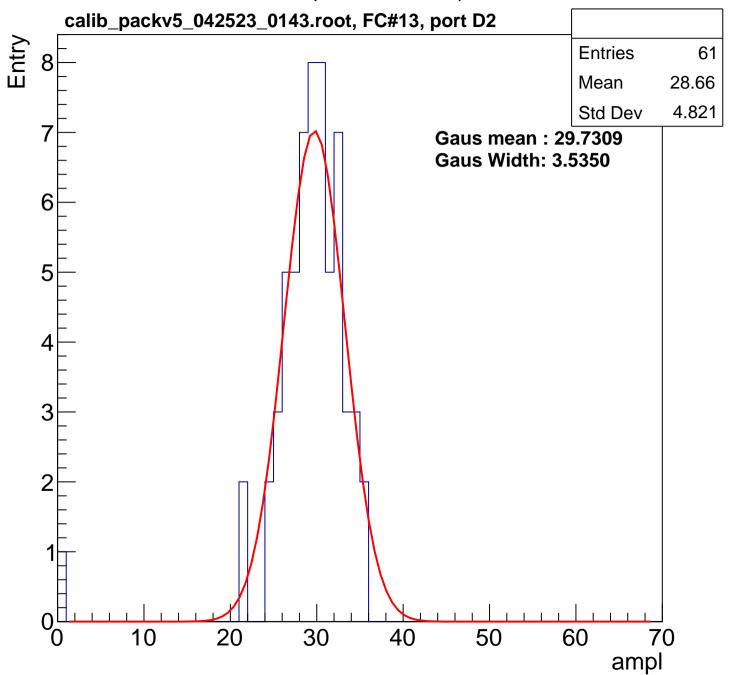


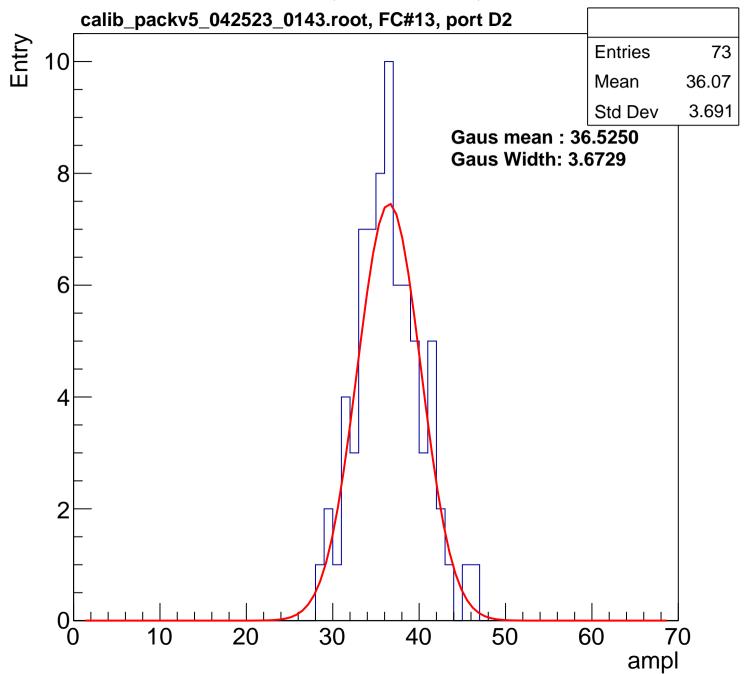


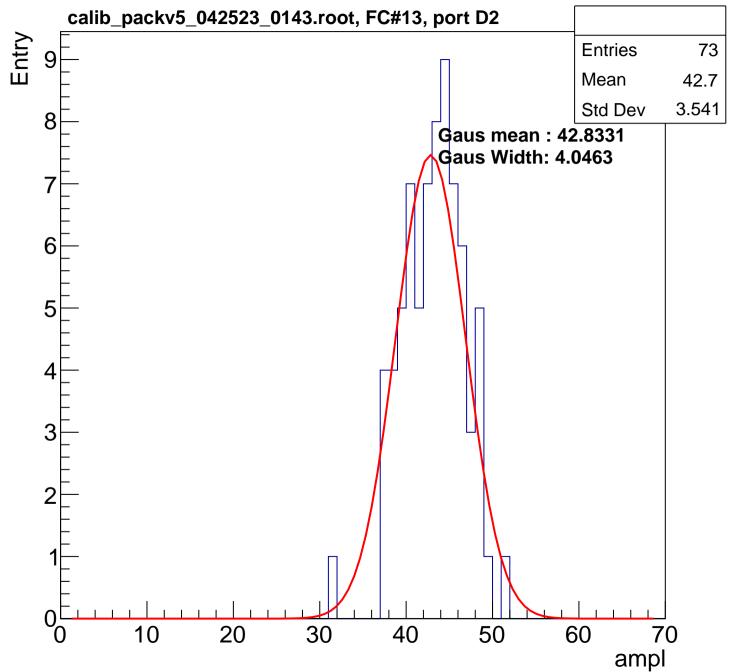


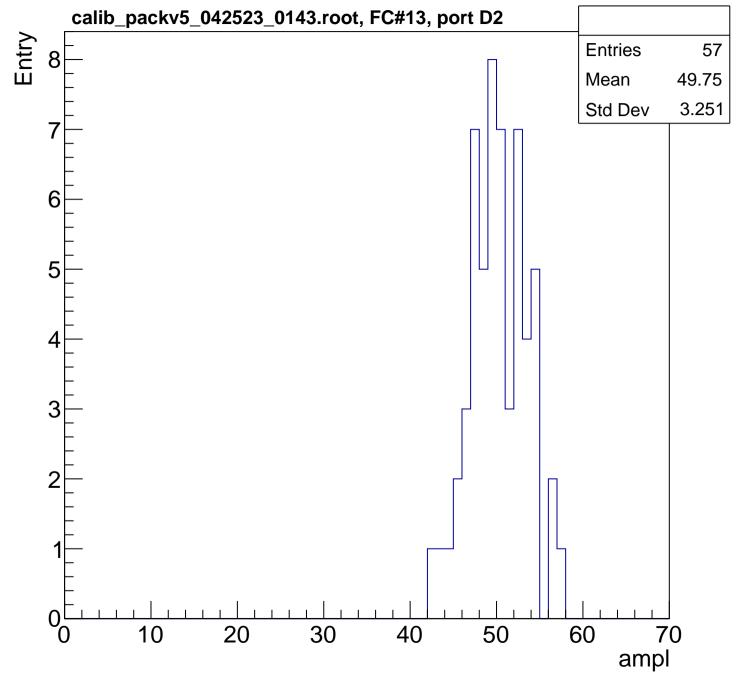


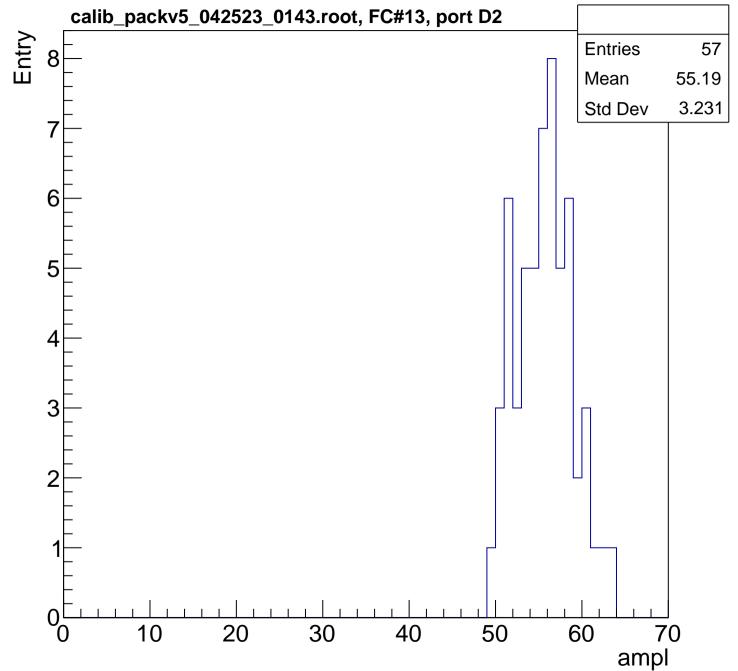


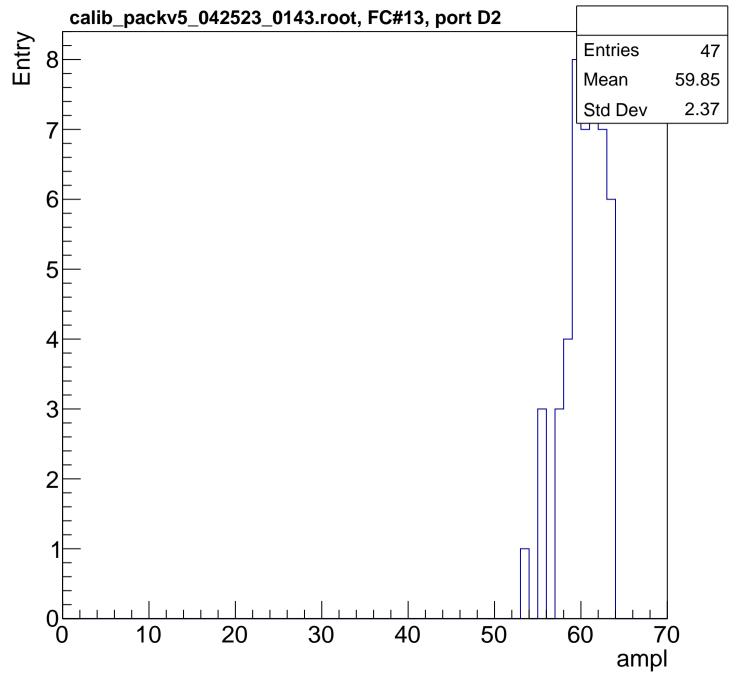


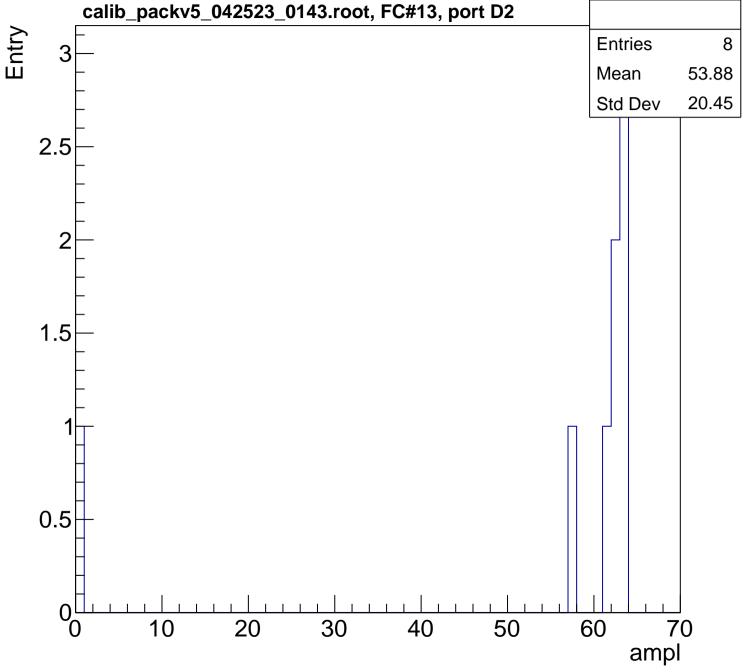




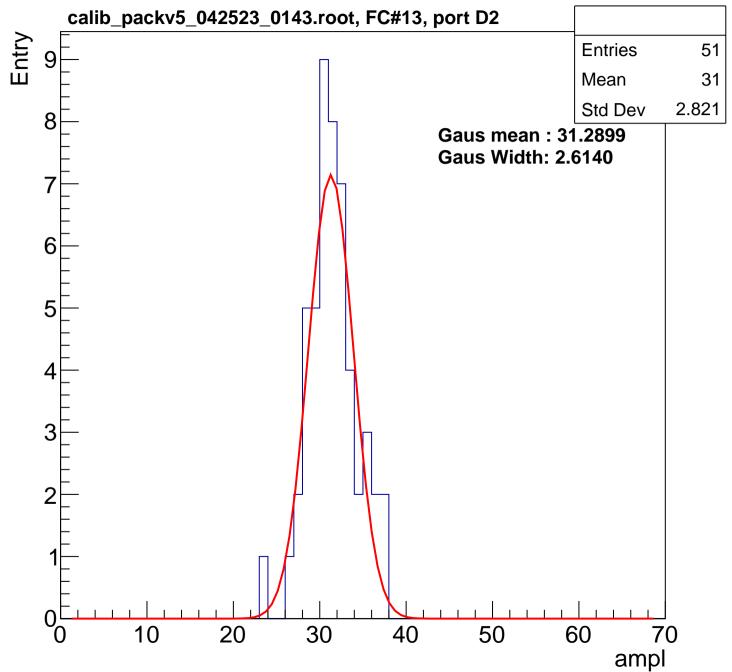


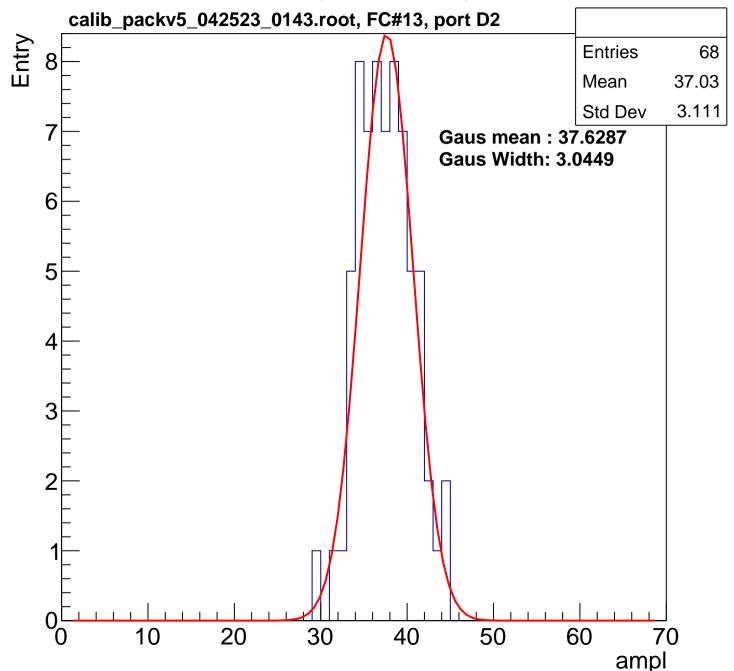


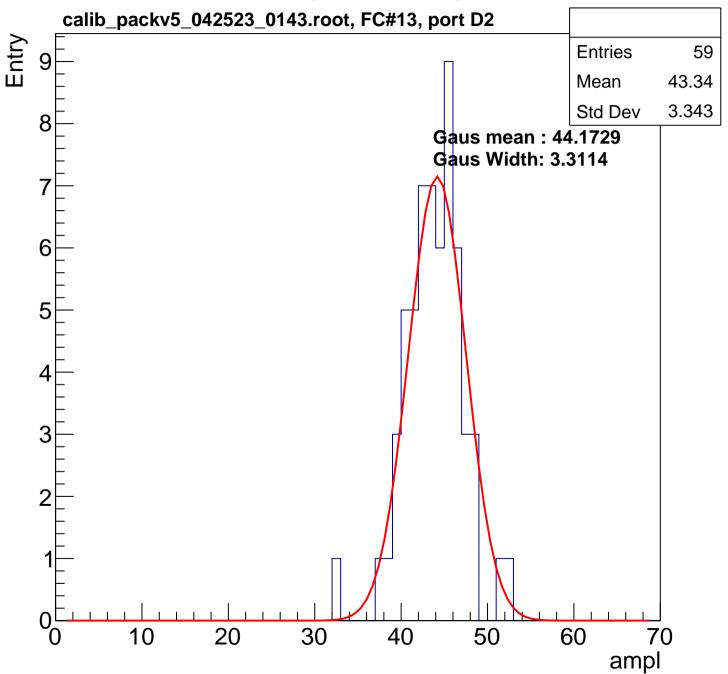


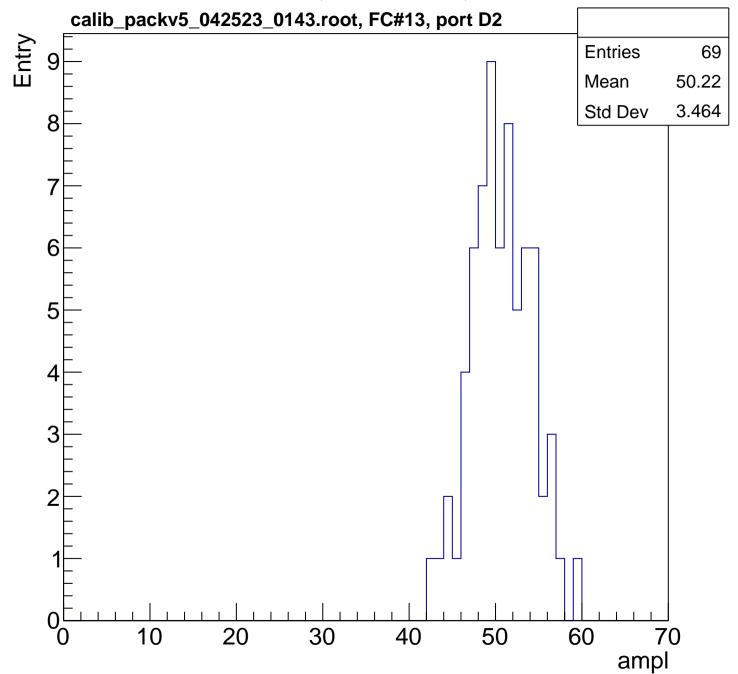


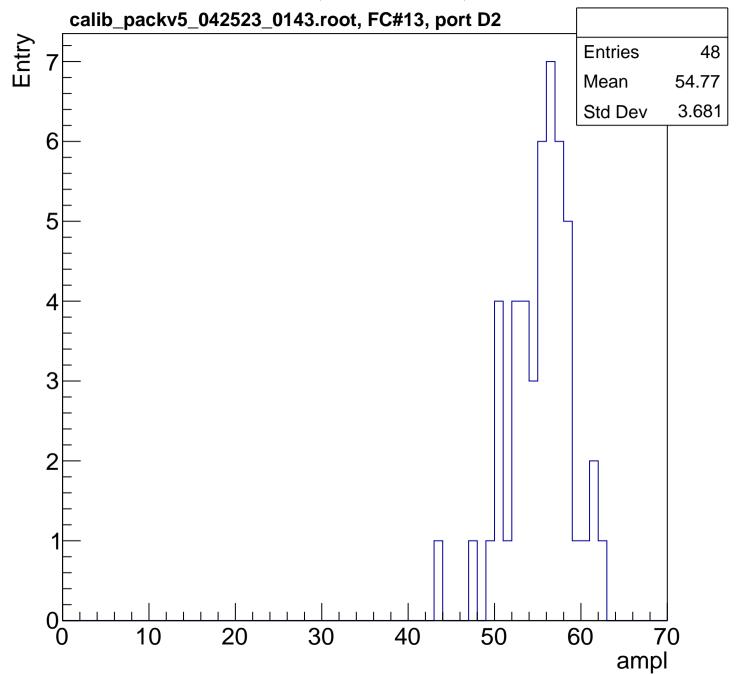
B1L003S, U8-ch63, adc7 calib\_packv5\_042523\_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

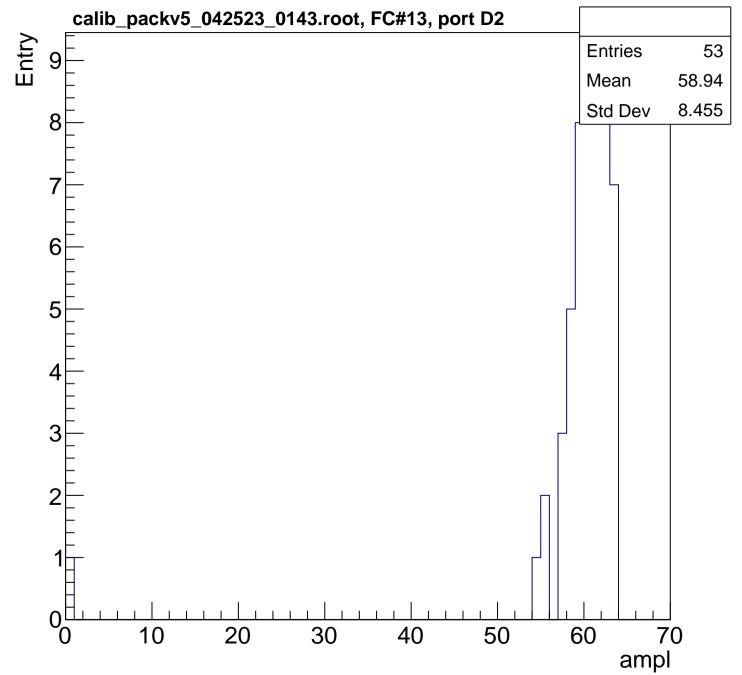


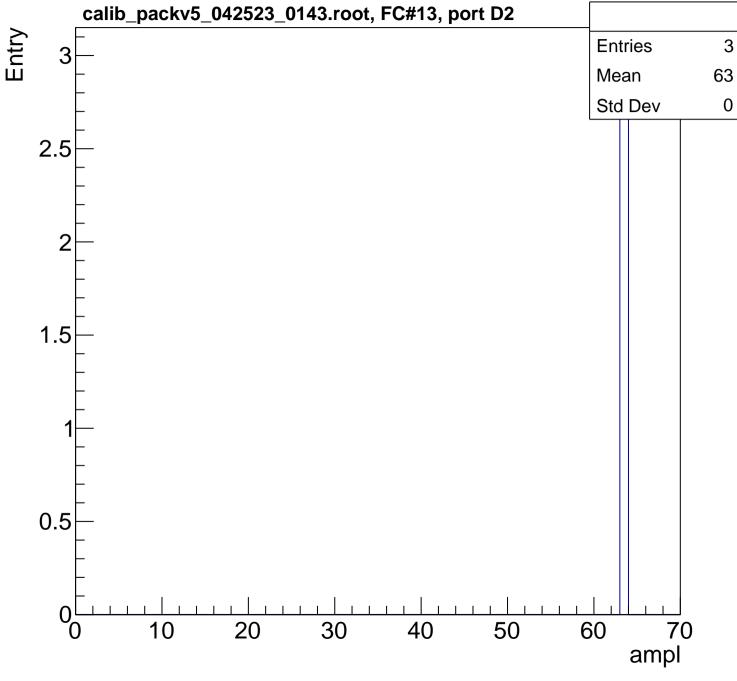




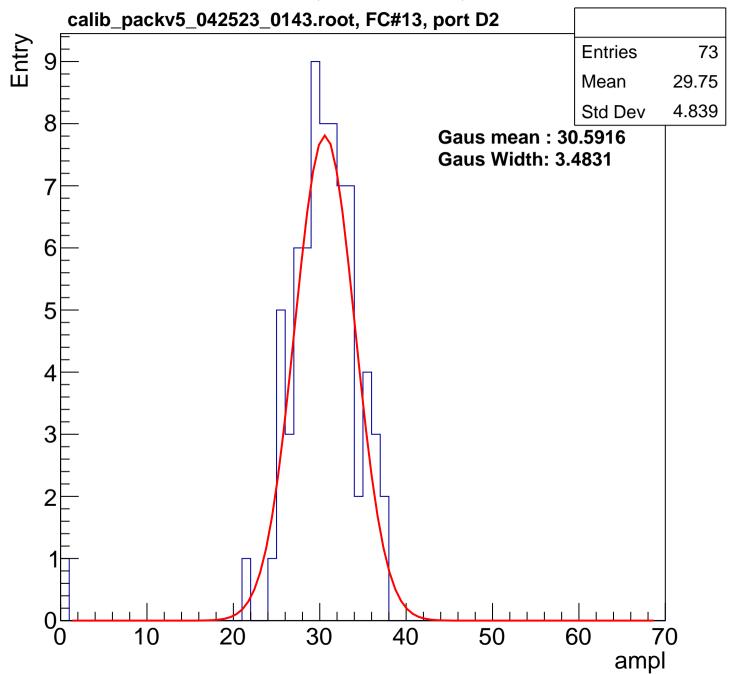


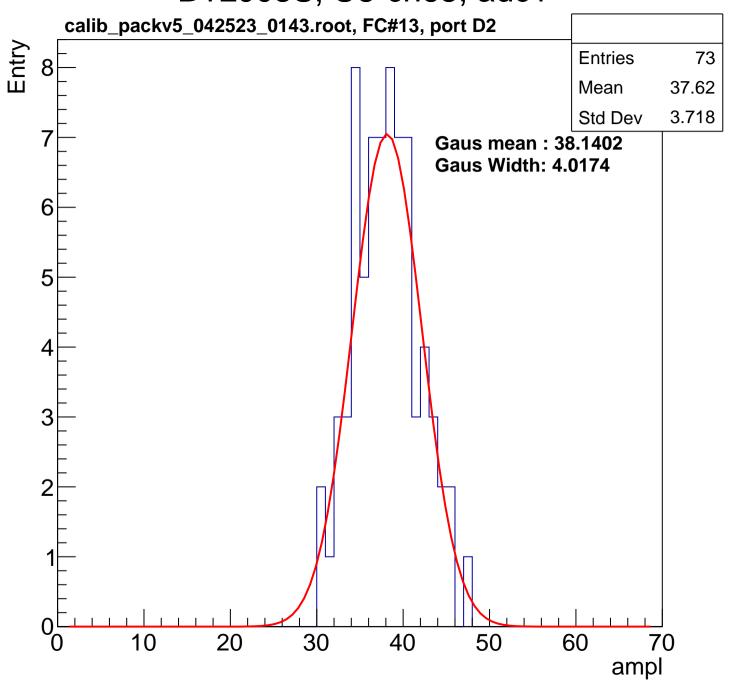


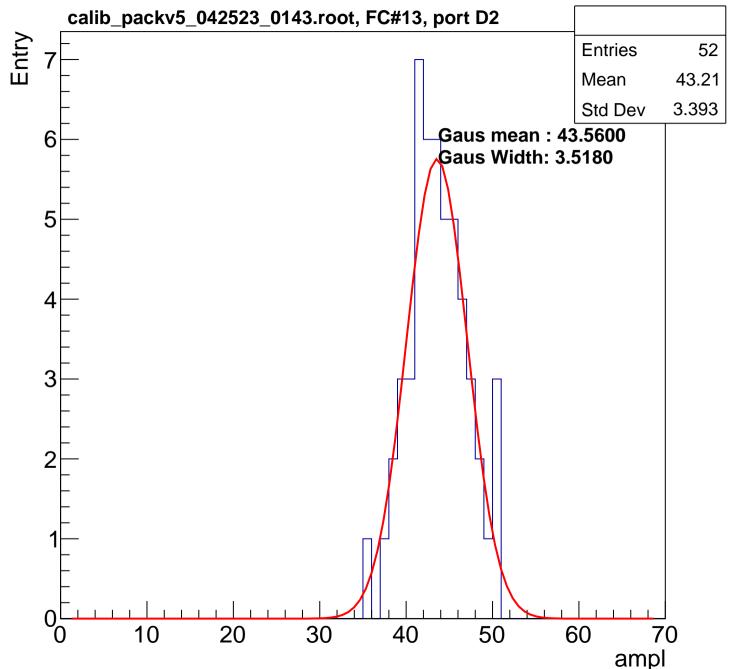


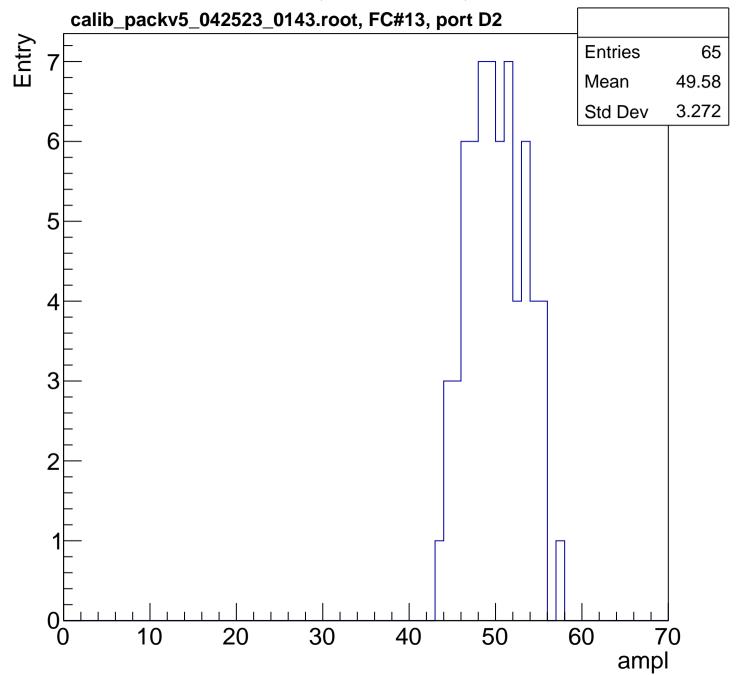


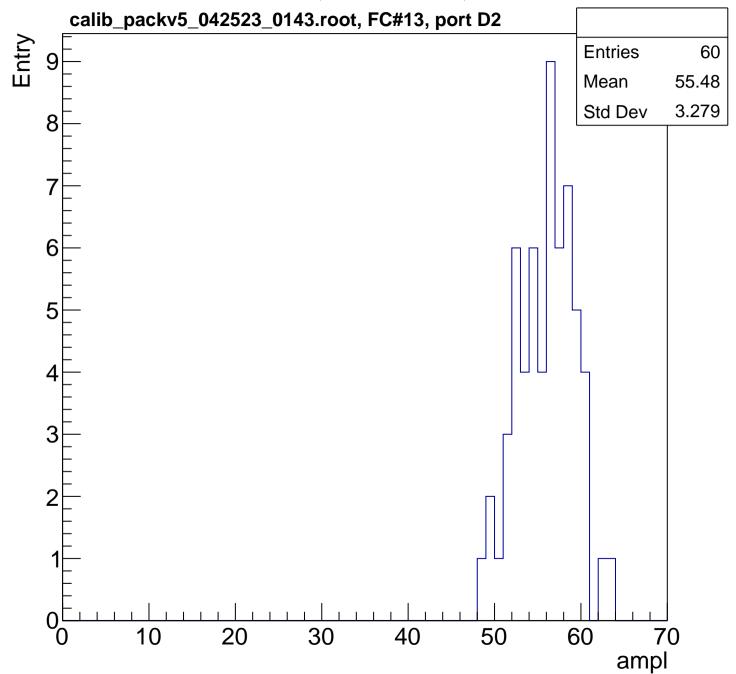


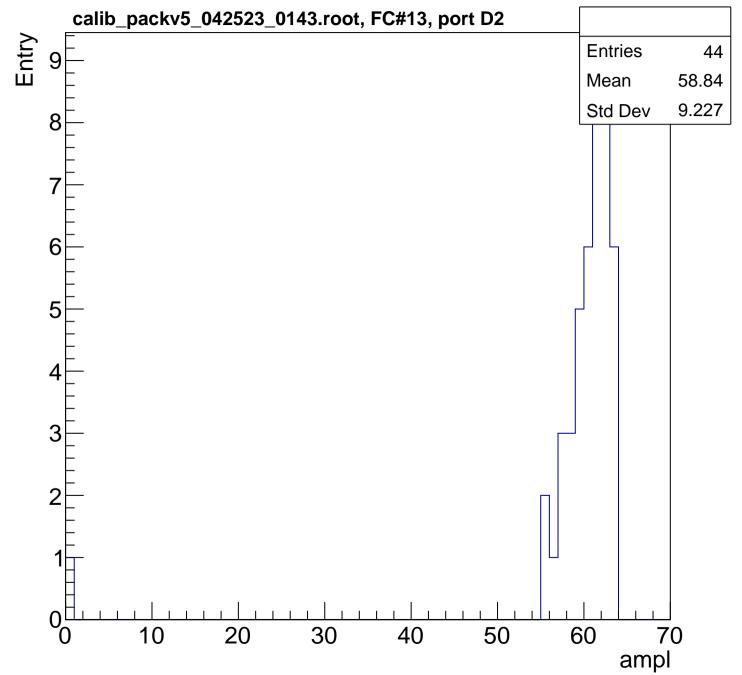


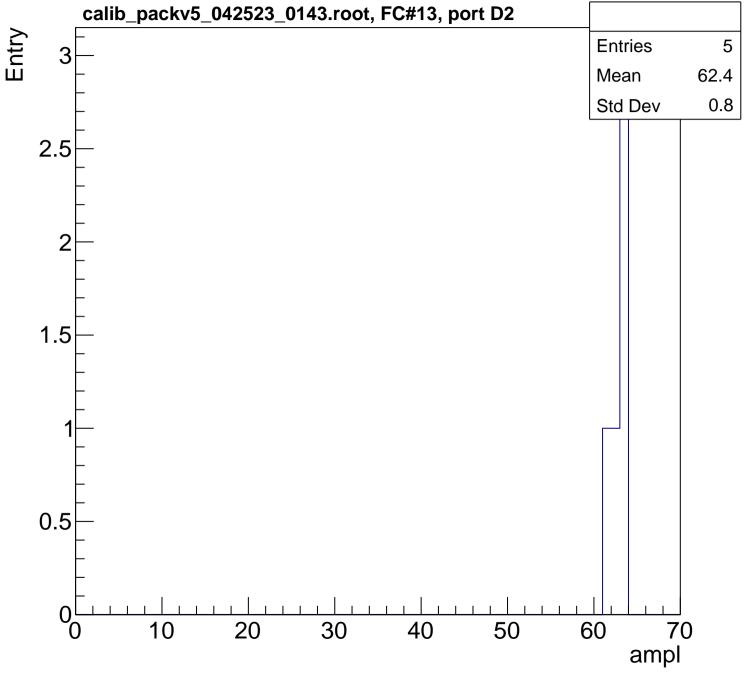




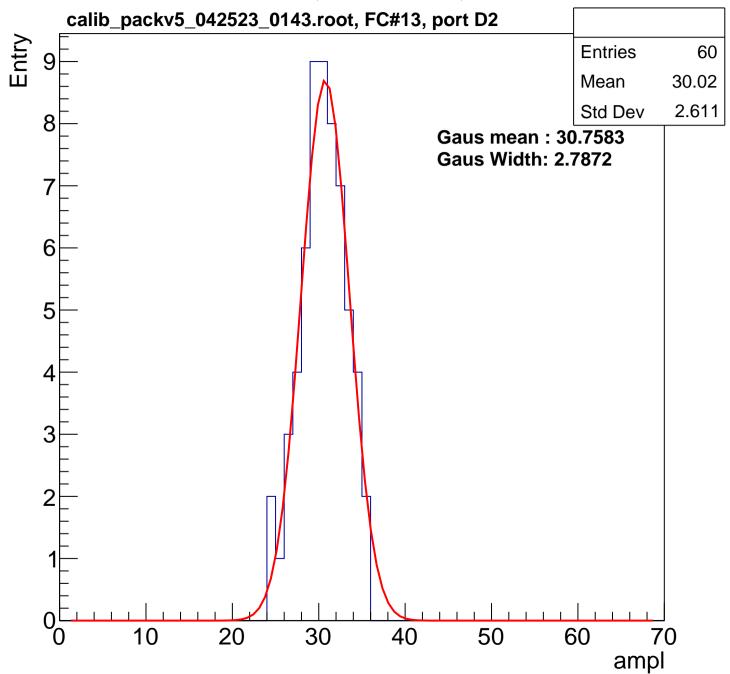


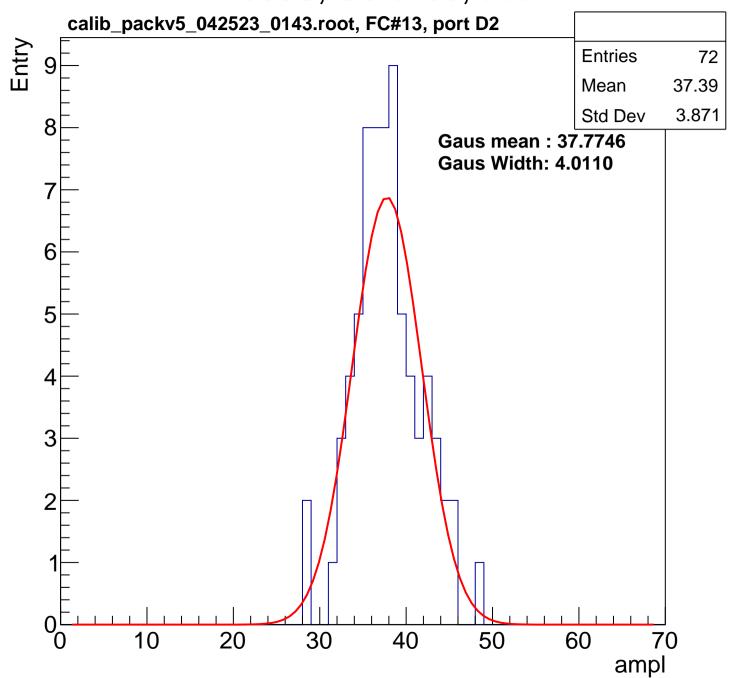


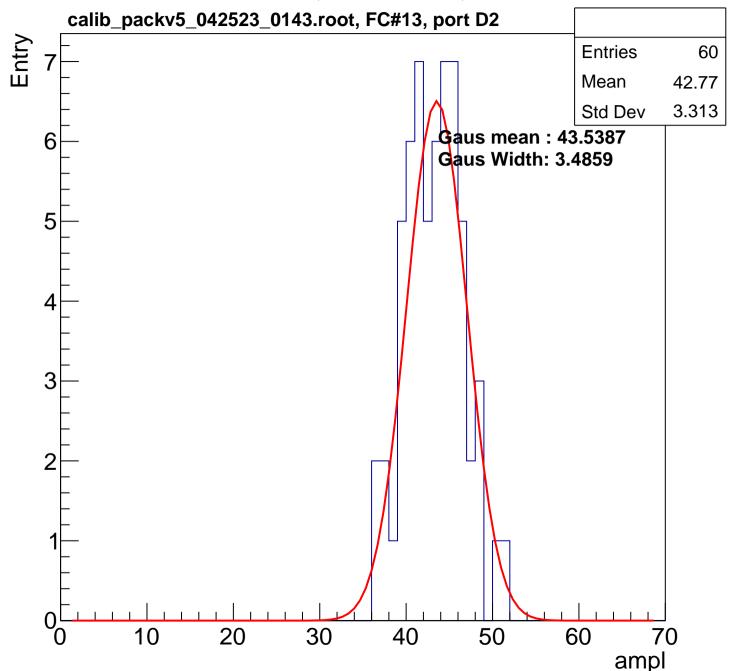


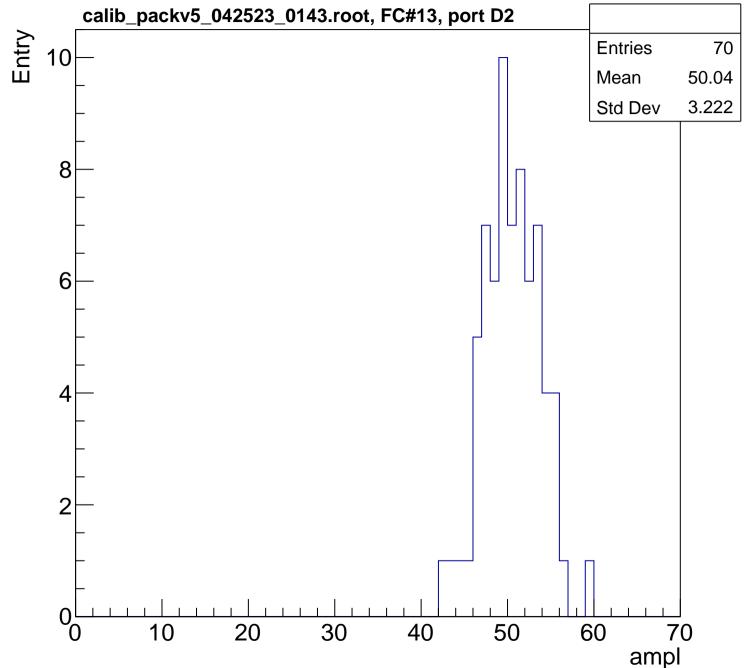


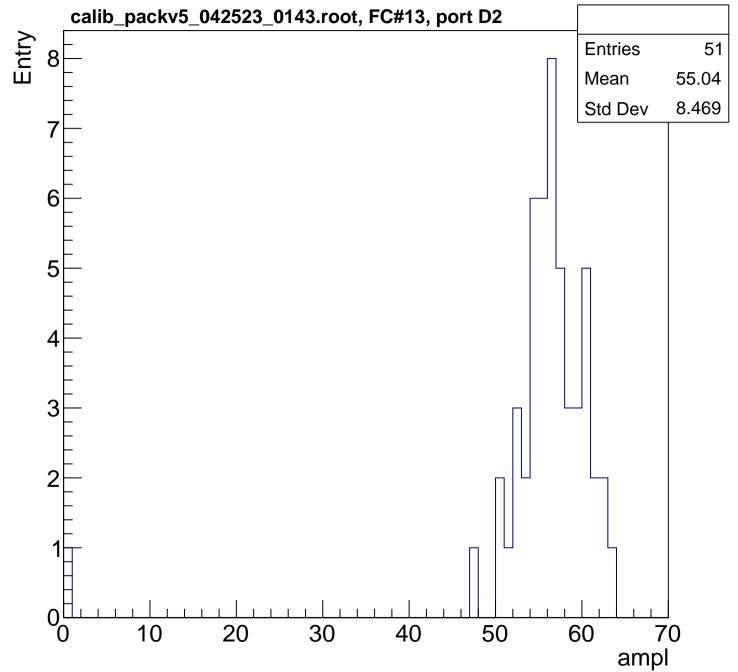
B1L003S, U8-ch65, adc7 calib\_packv5\_042523\_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

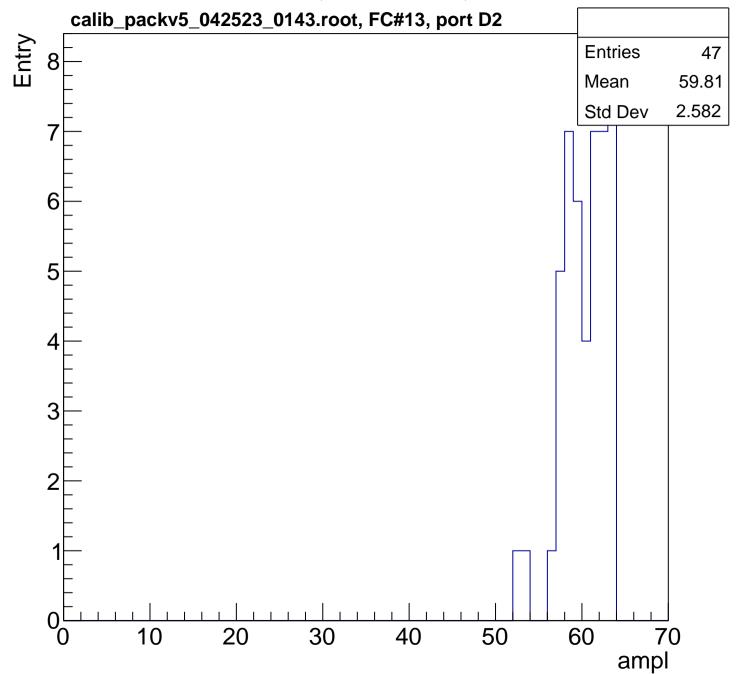


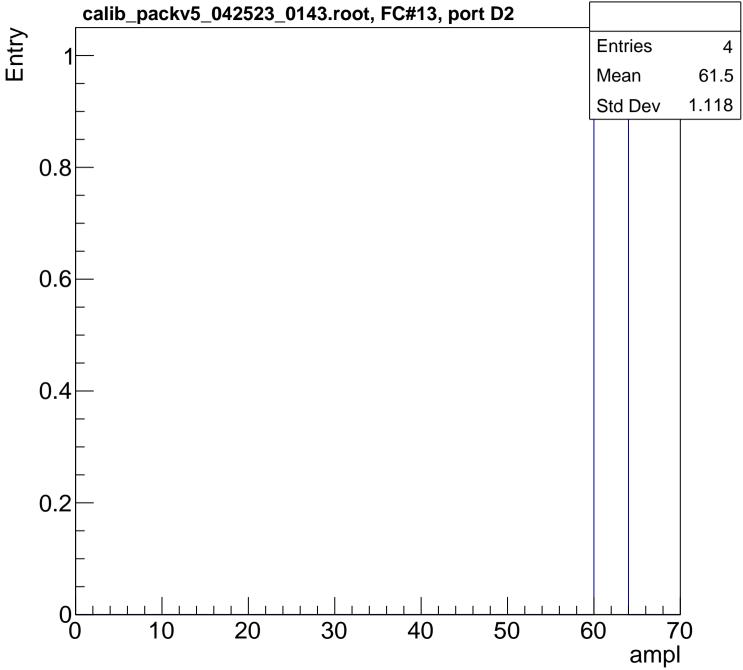




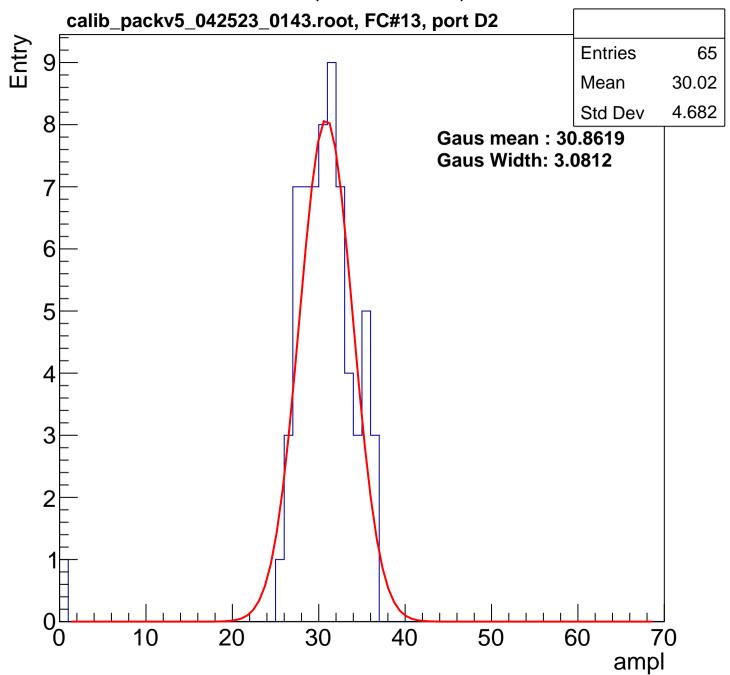


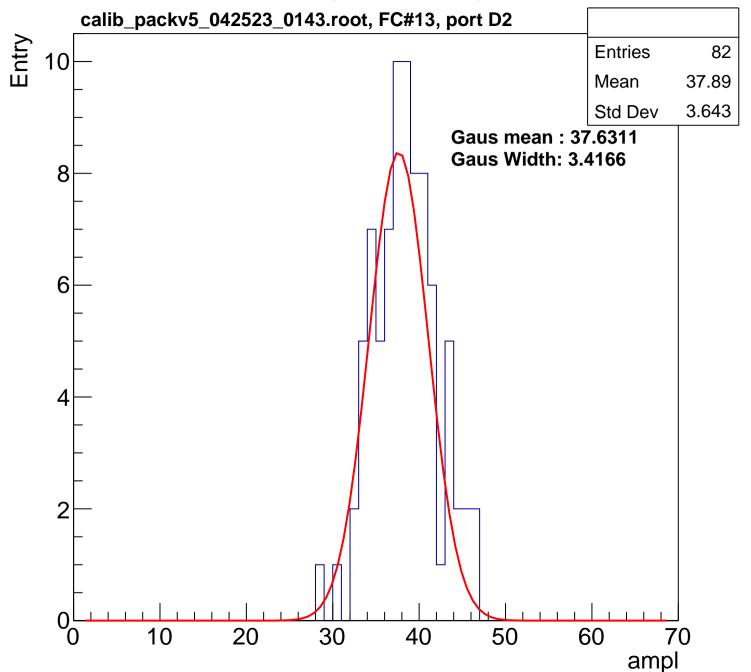


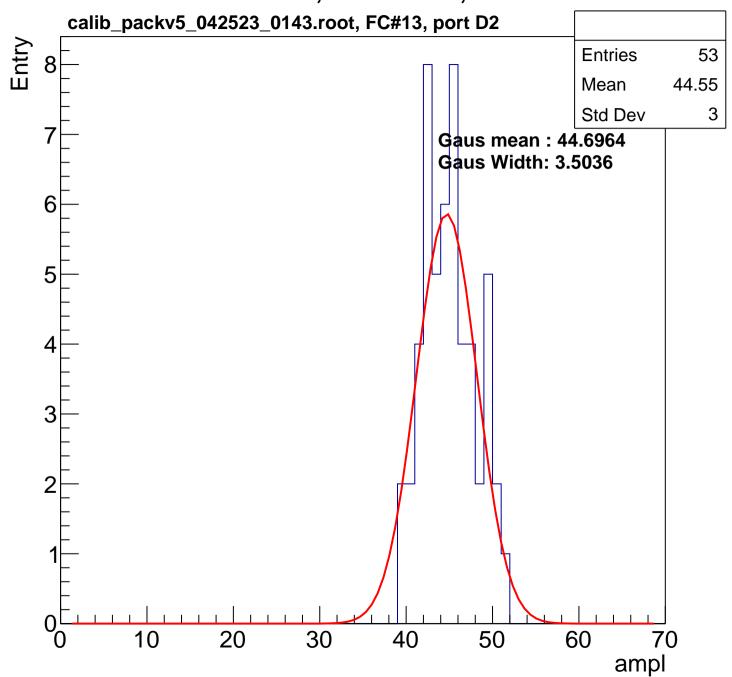


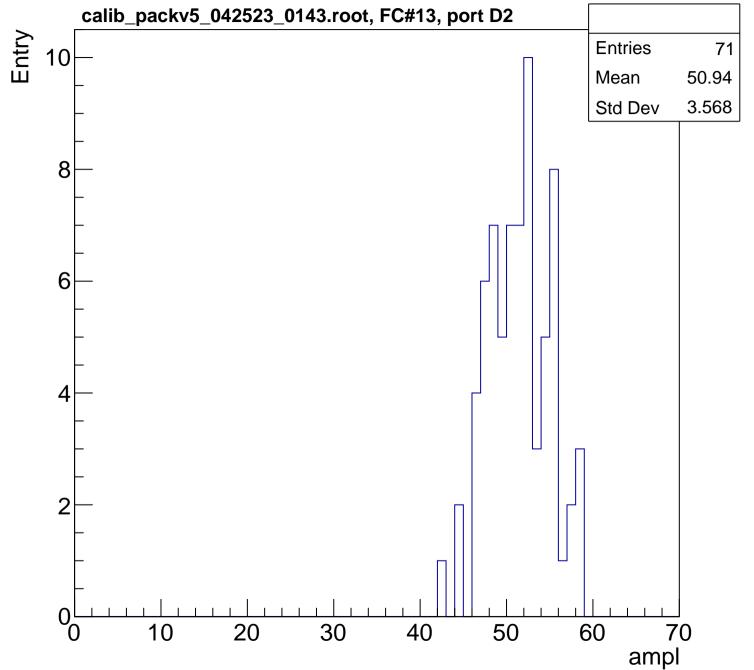


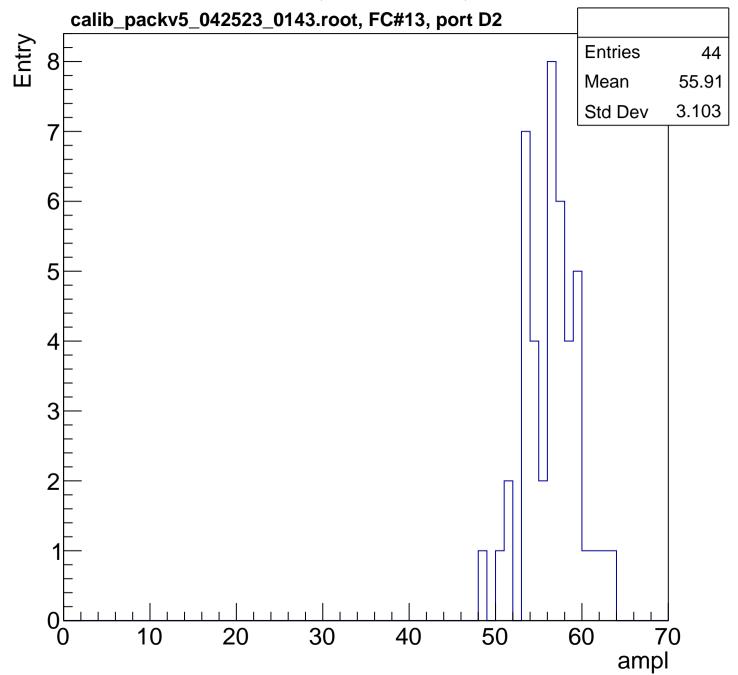


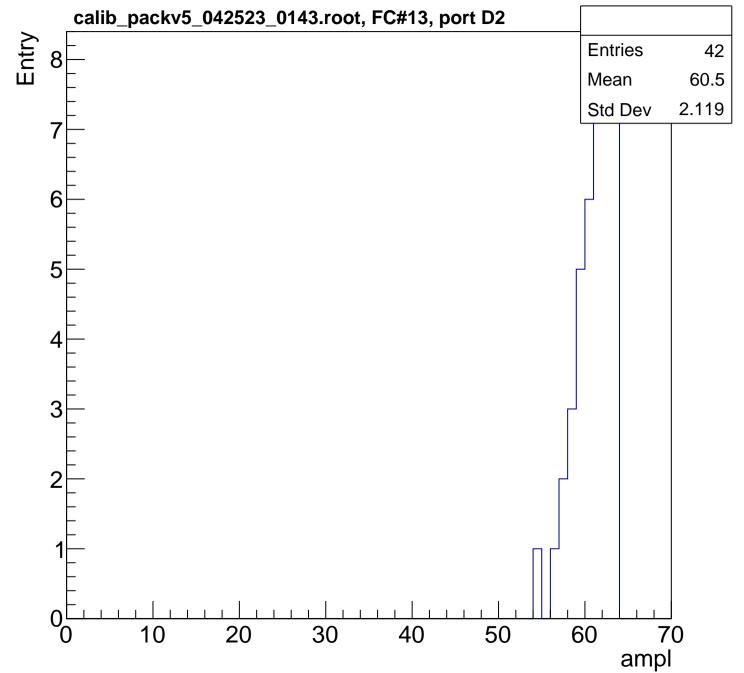


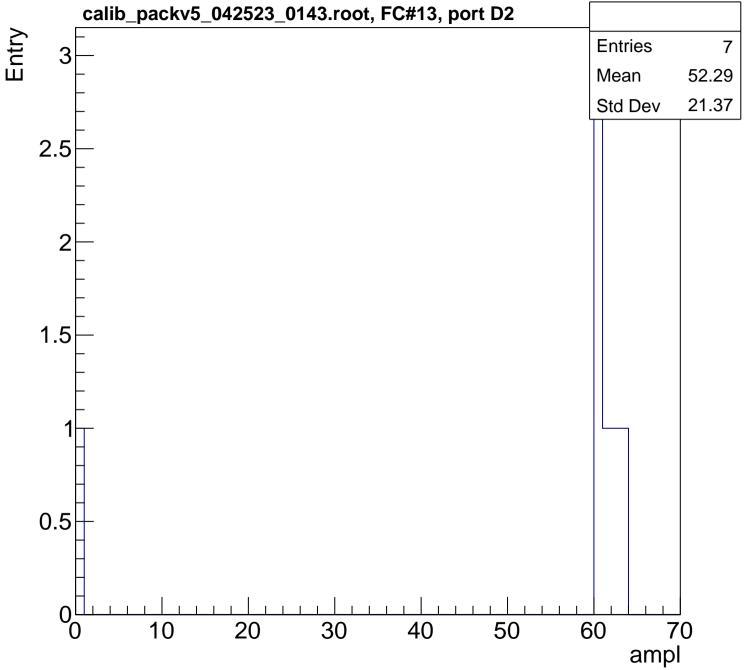


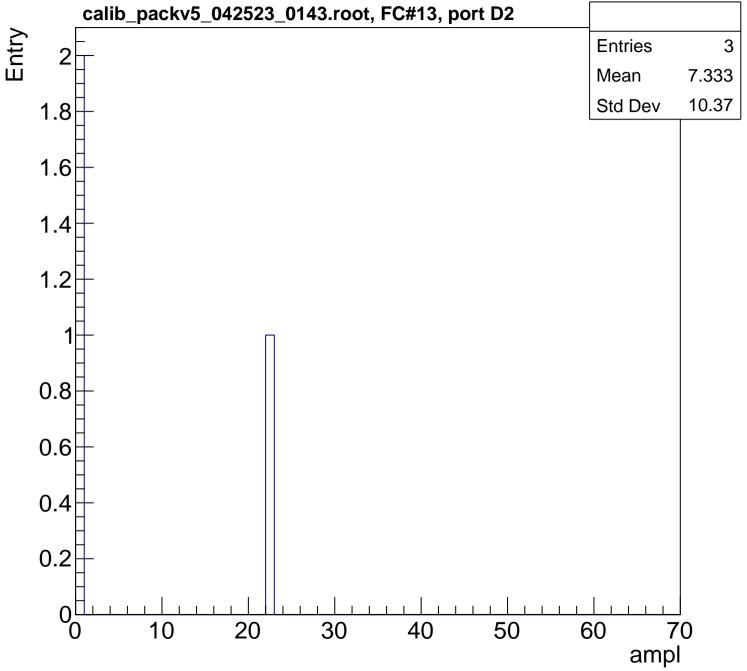


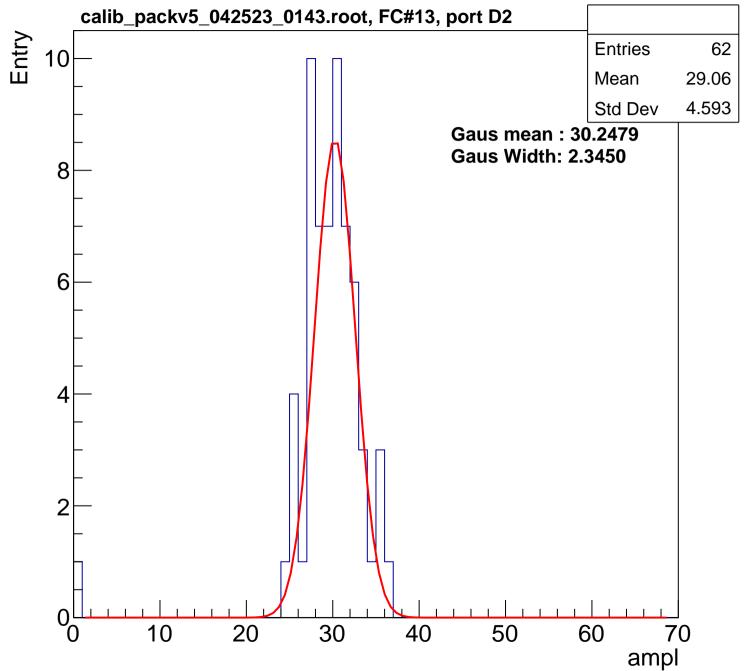


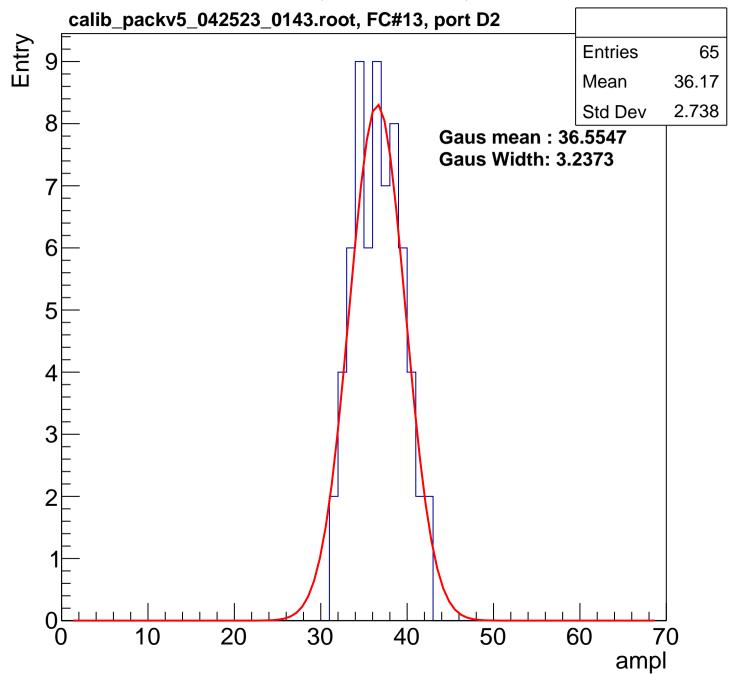


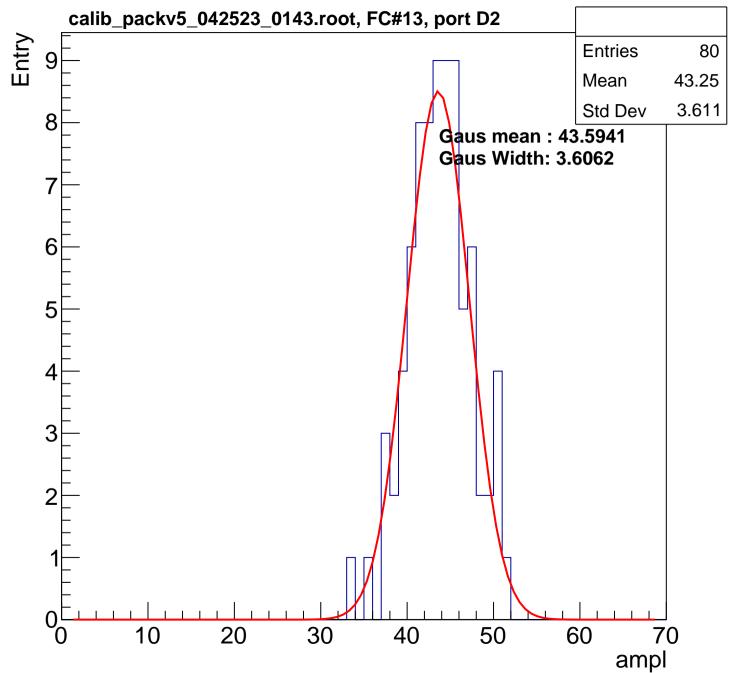


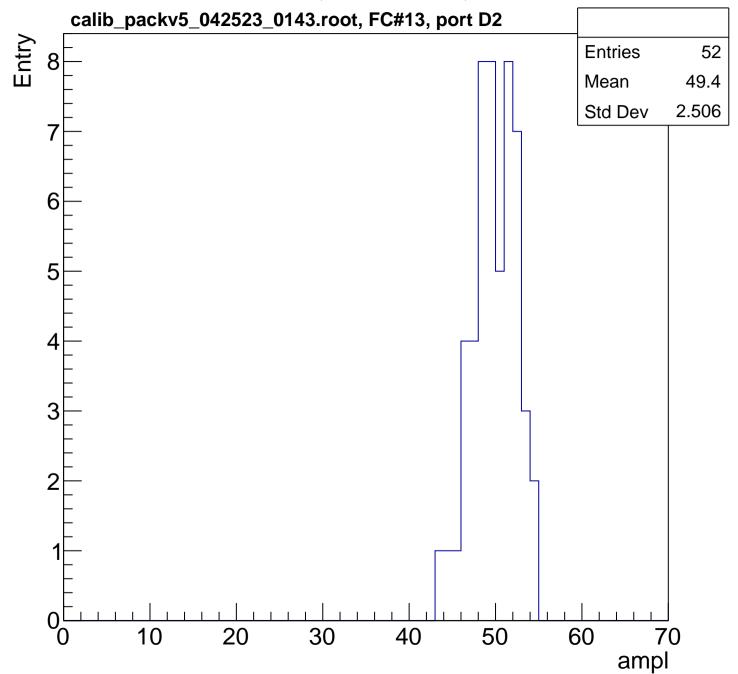


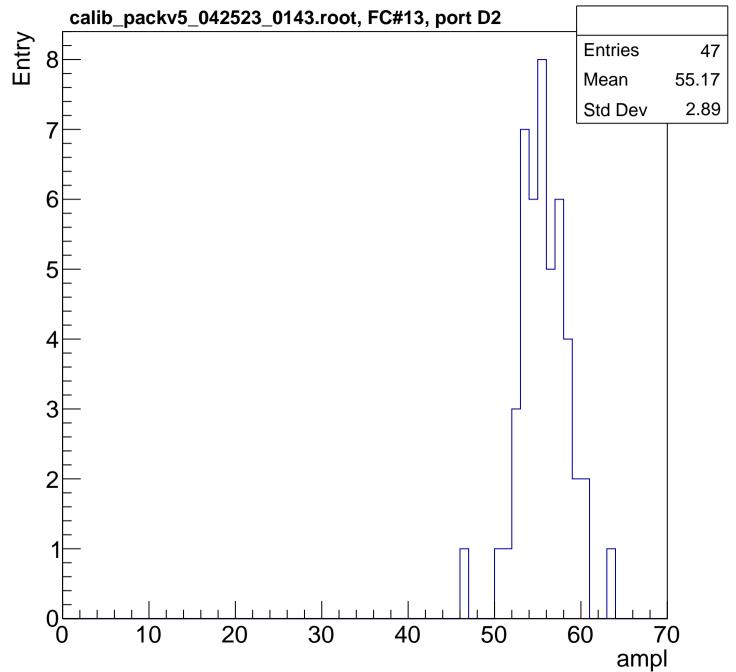


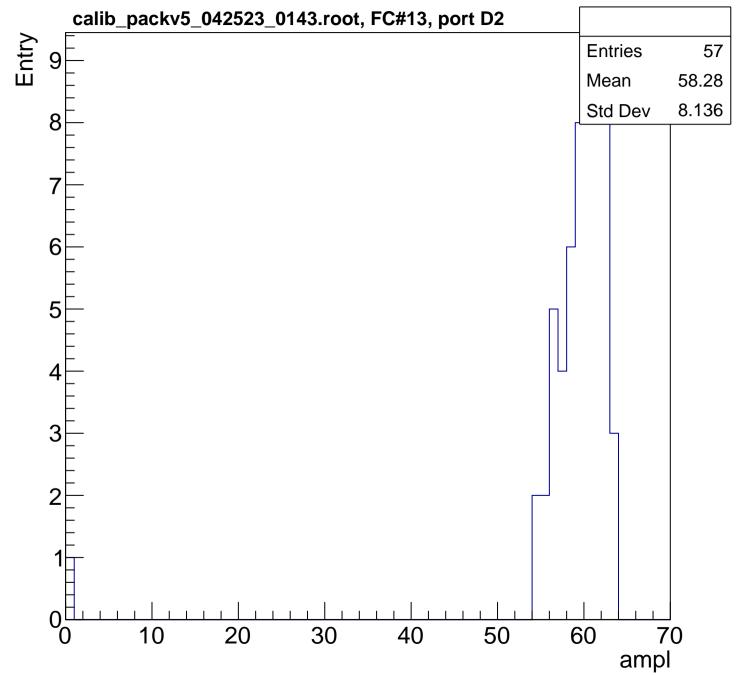


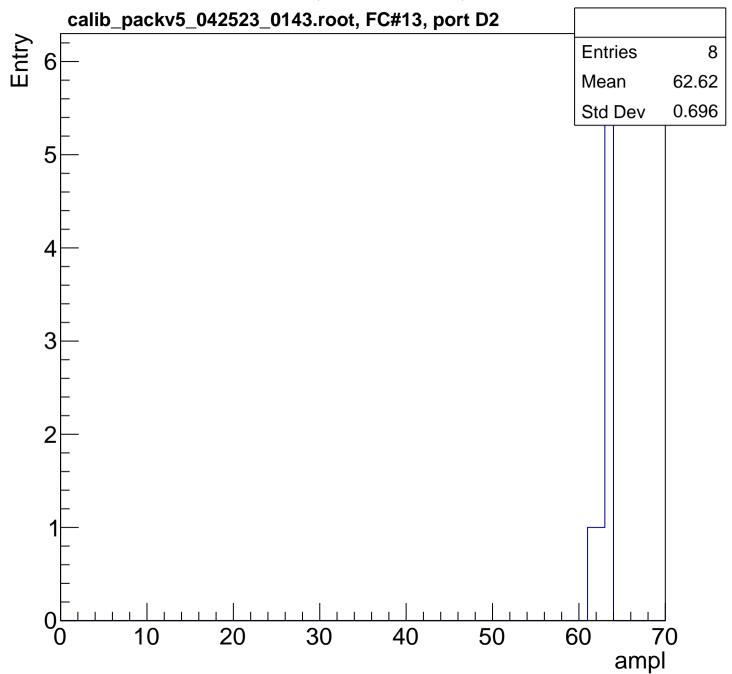




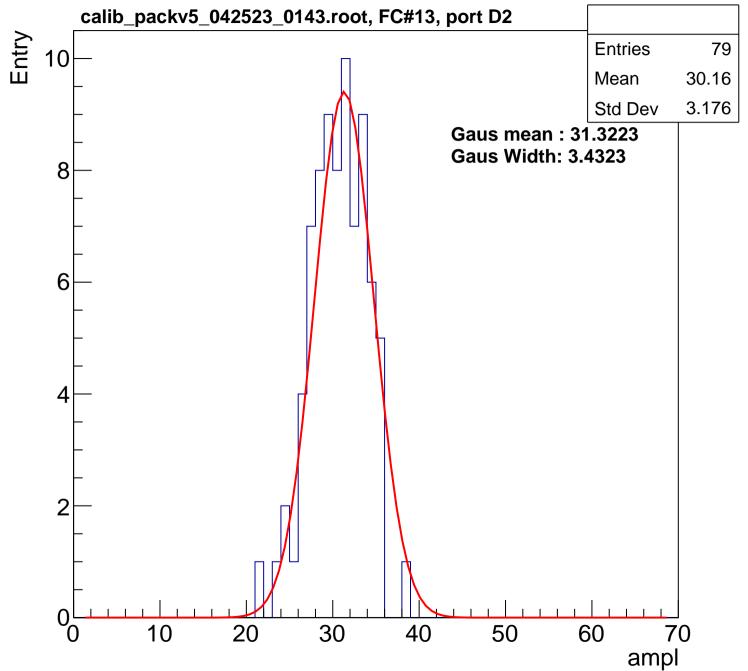


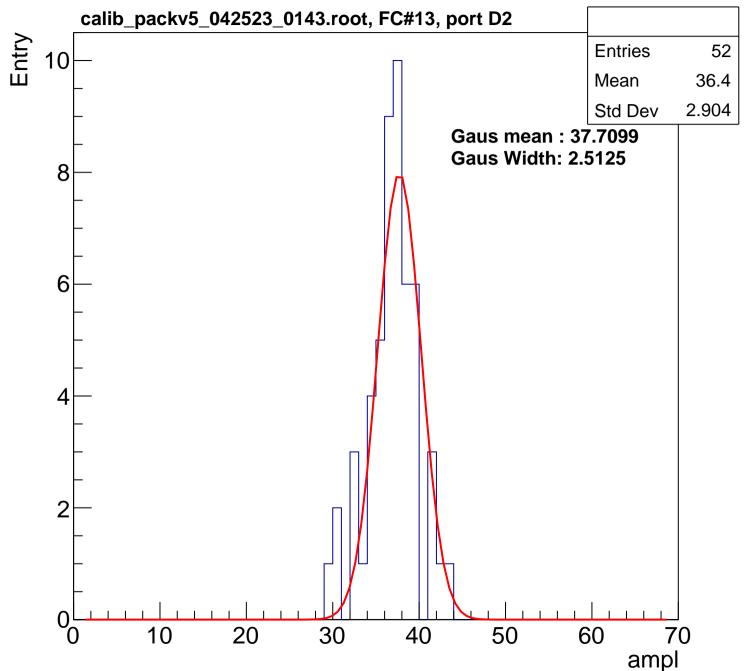


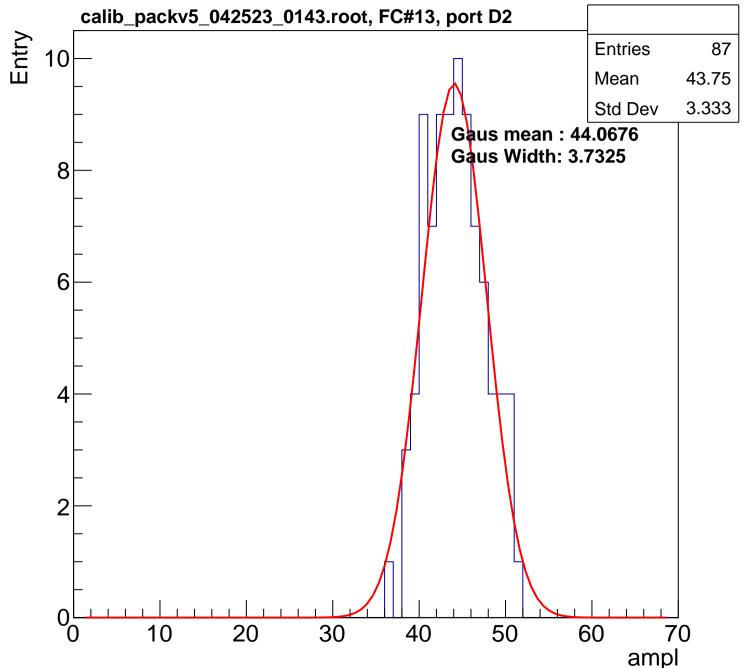


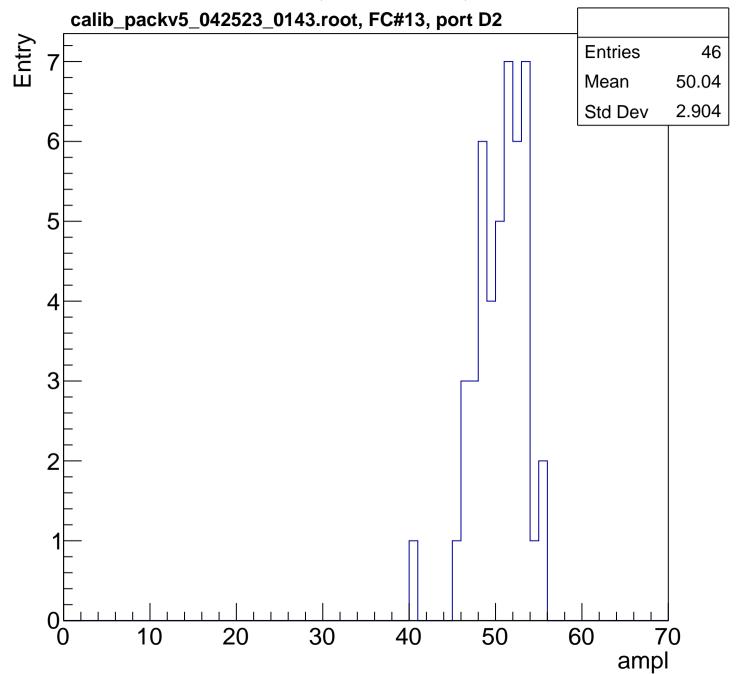


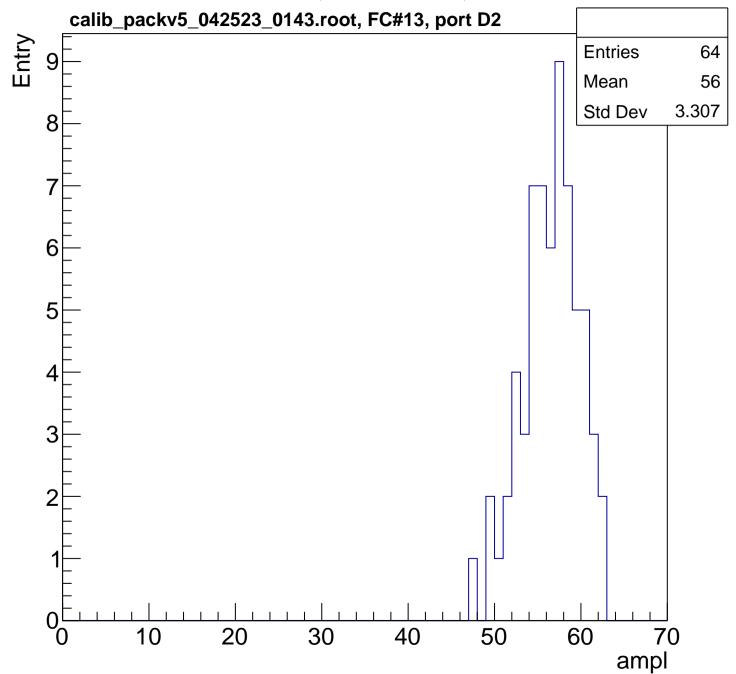


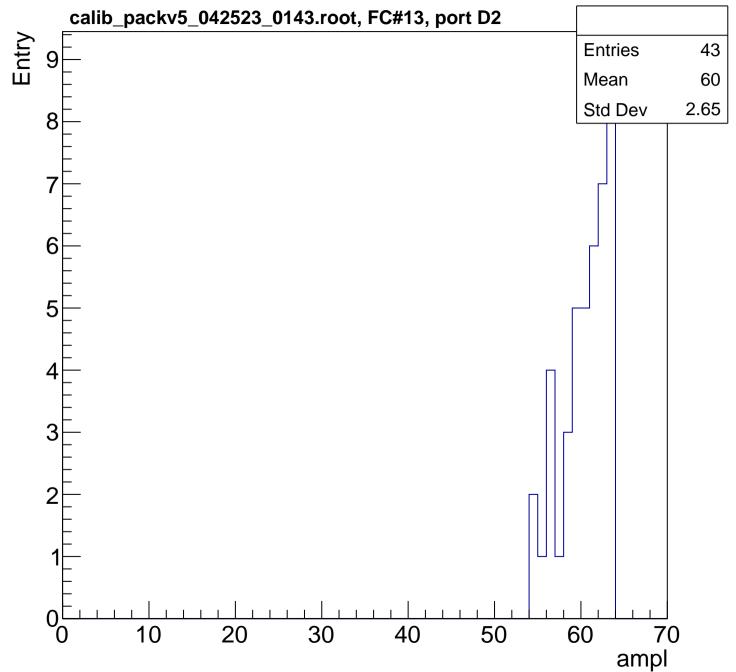


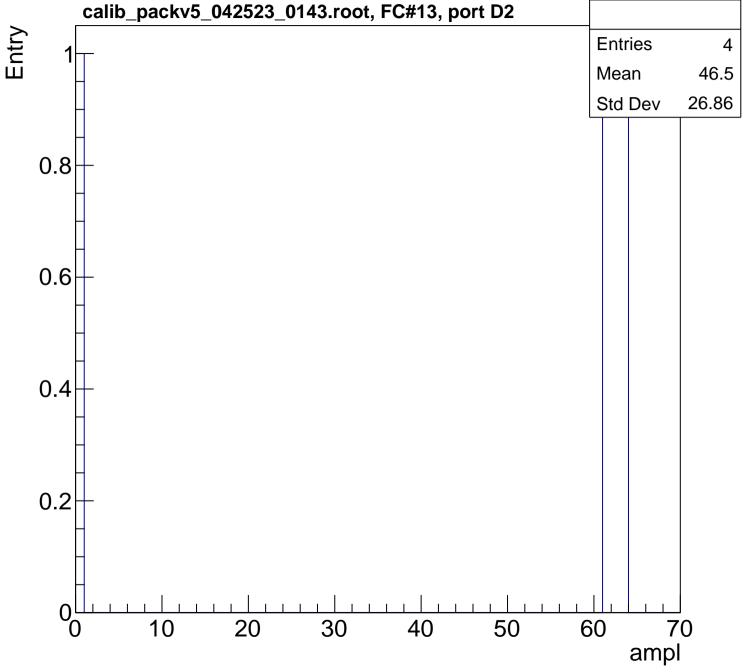




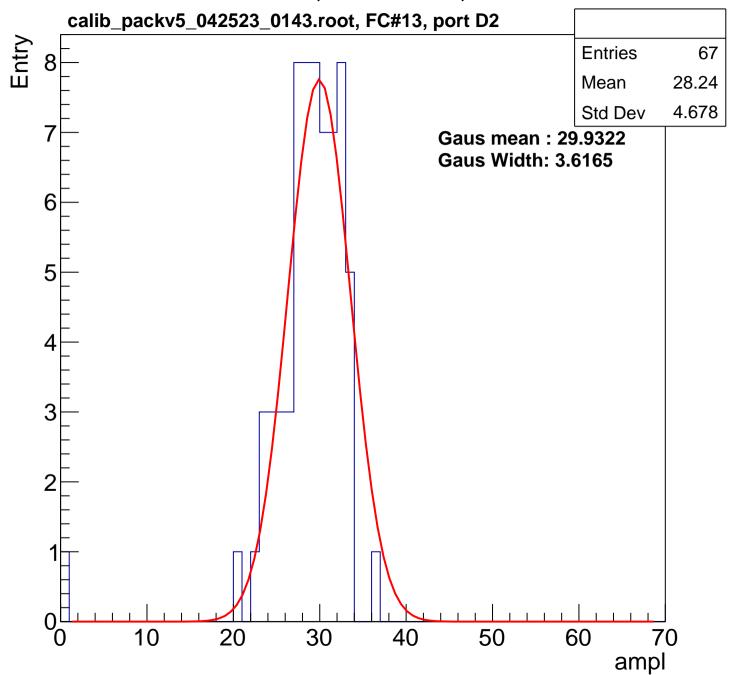


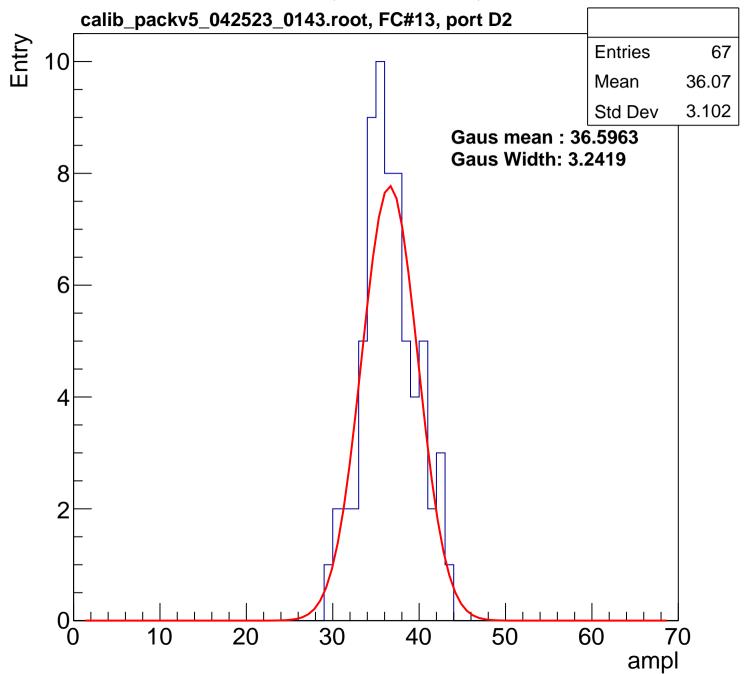


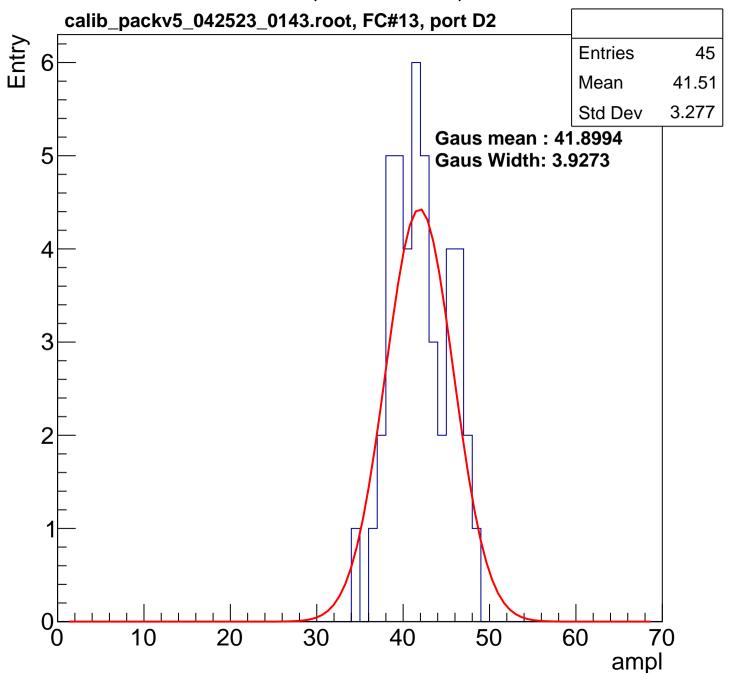


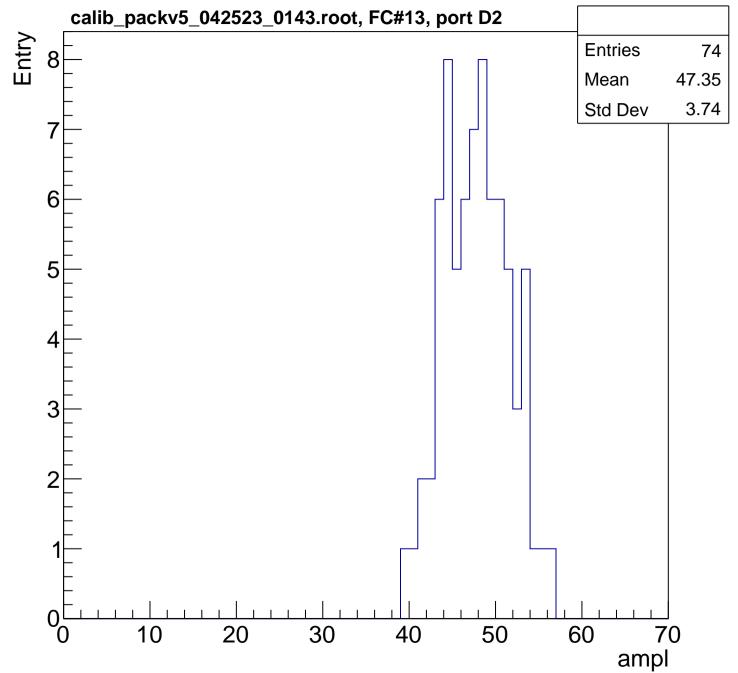


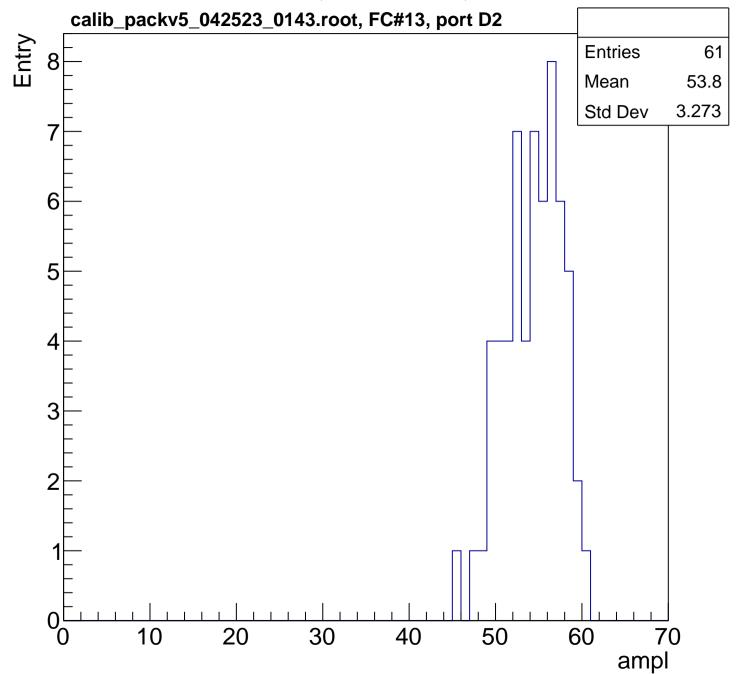
B1L003S, U8-ch69, adc7 calib\_packv5\_042523\_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

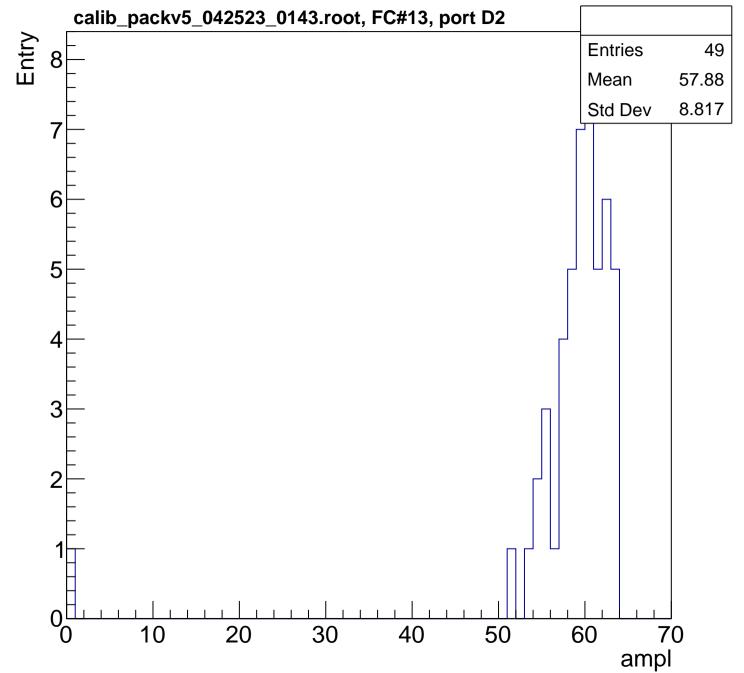


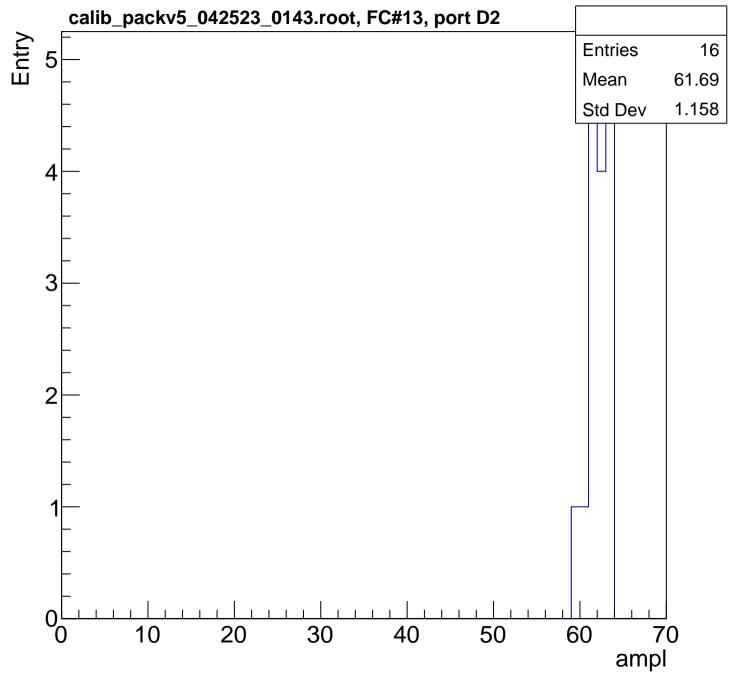




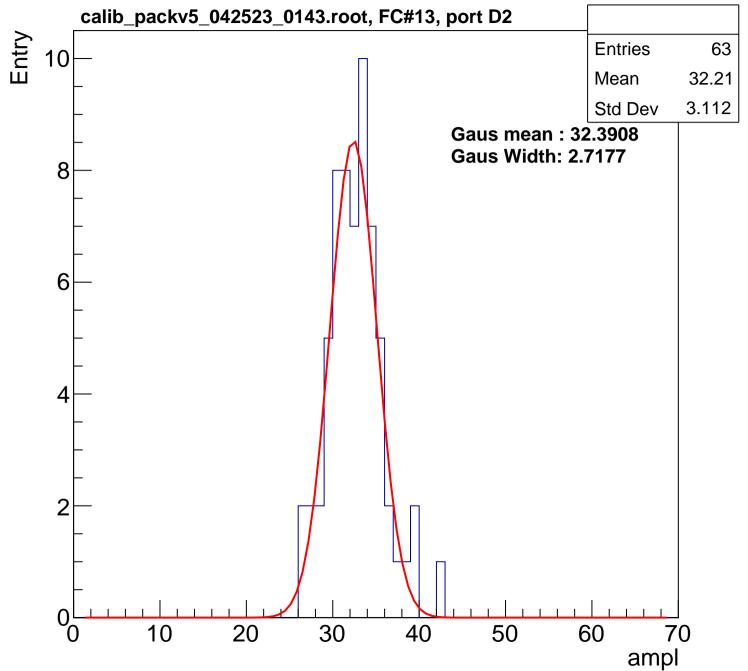


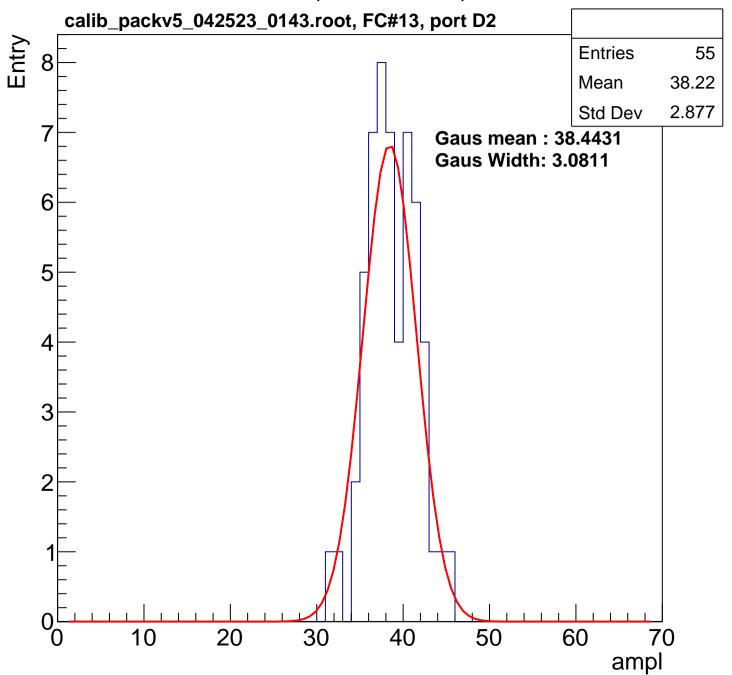


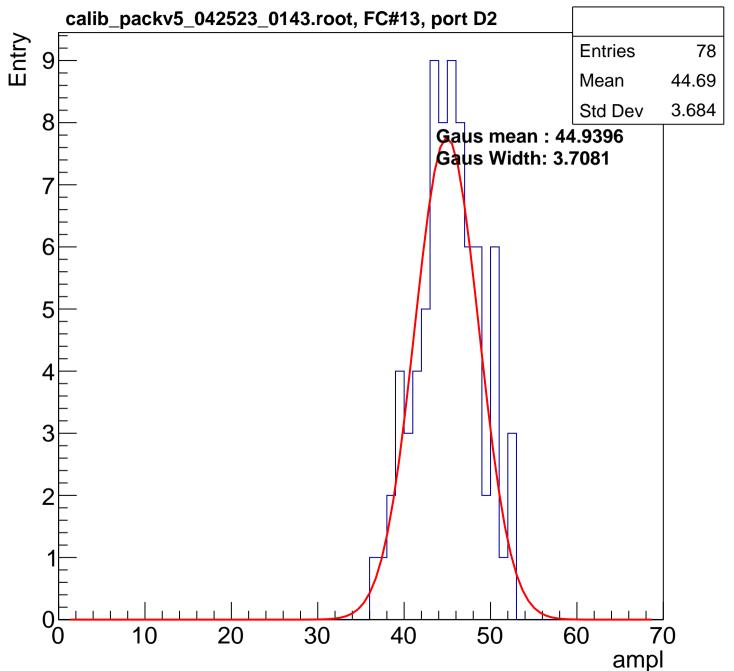


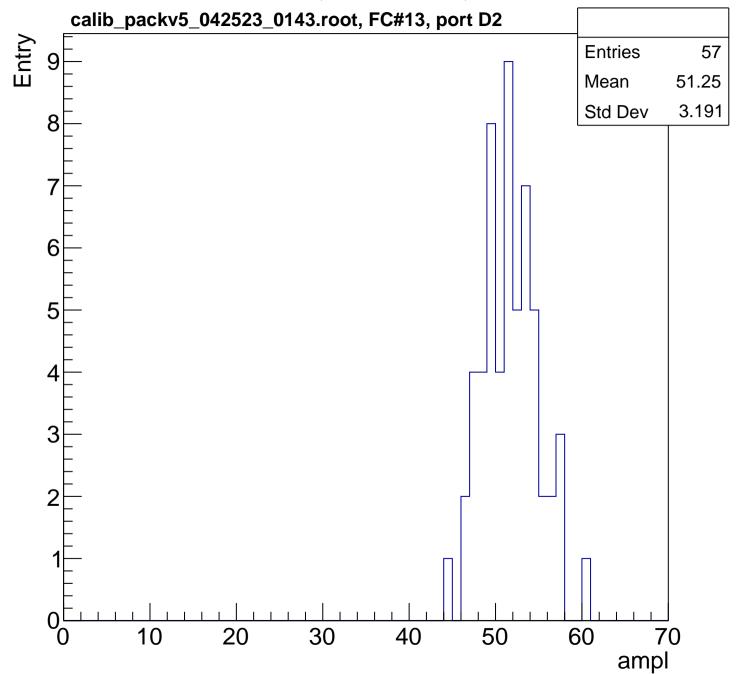


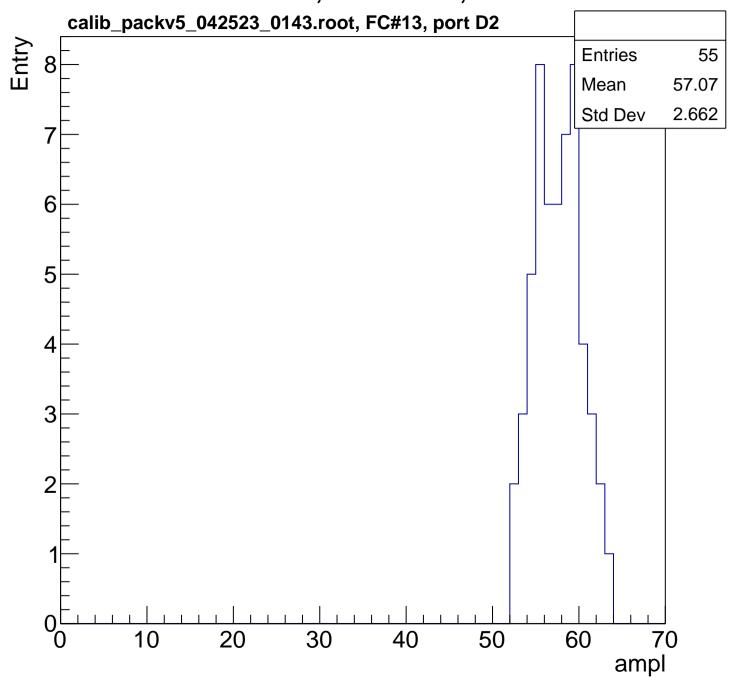
B1L003S, U8-ch70, adc7 calib\_packv5\_042523\_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

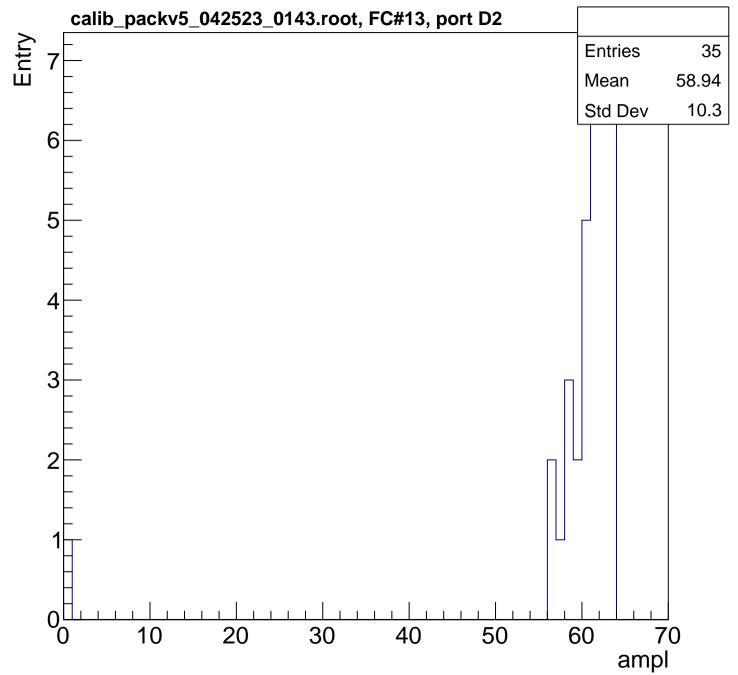


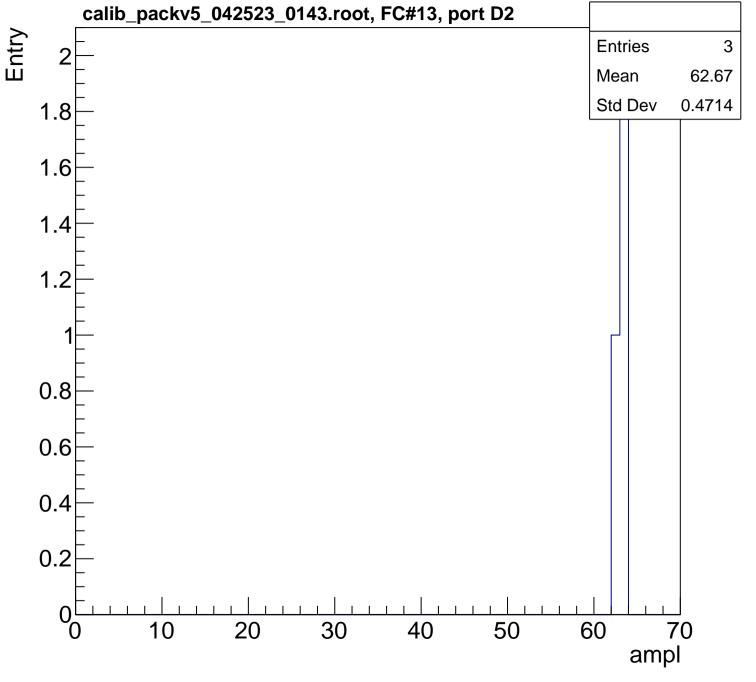




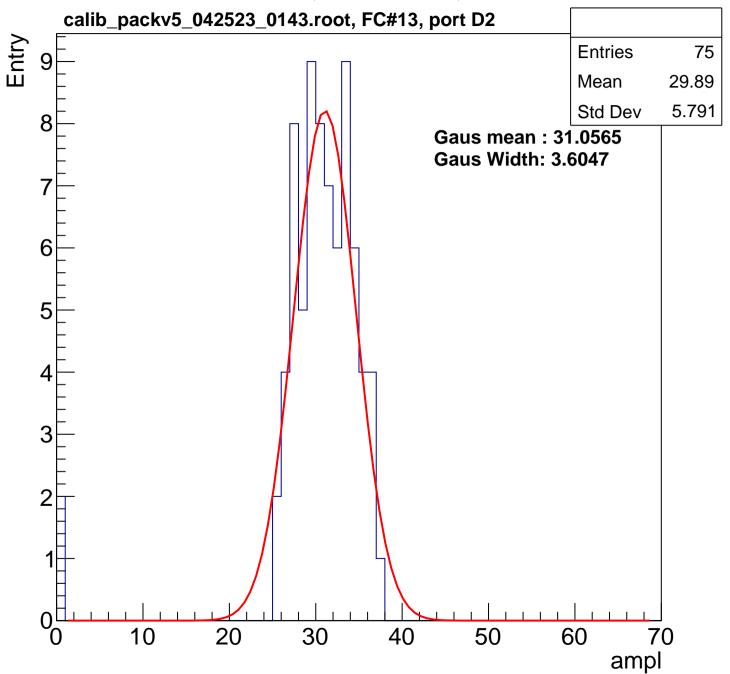


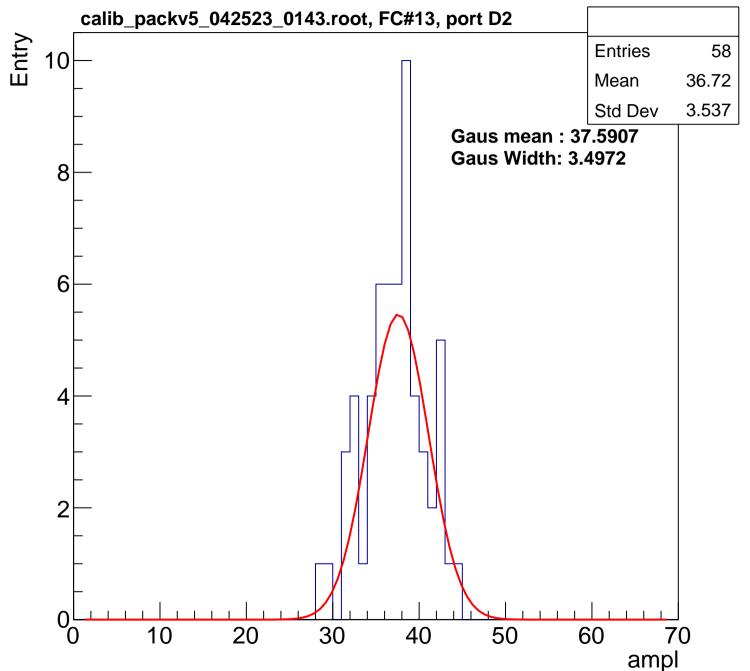


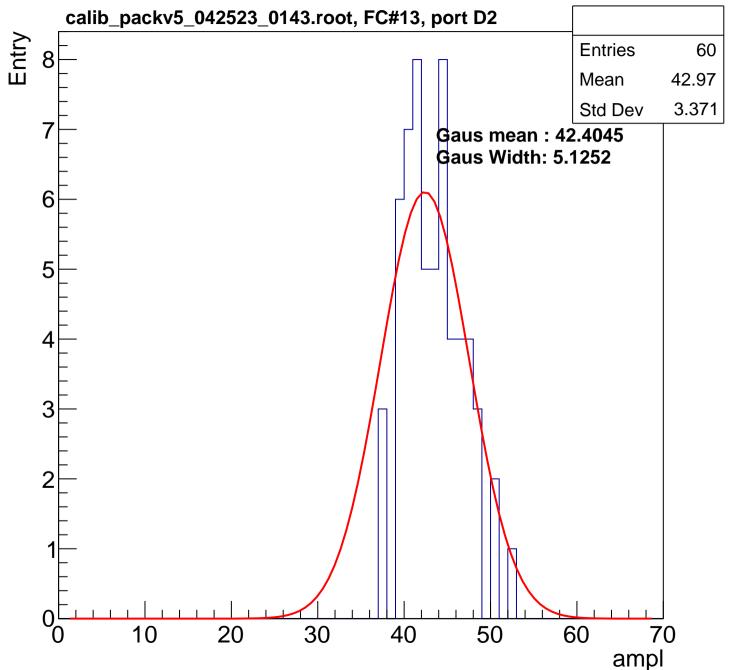


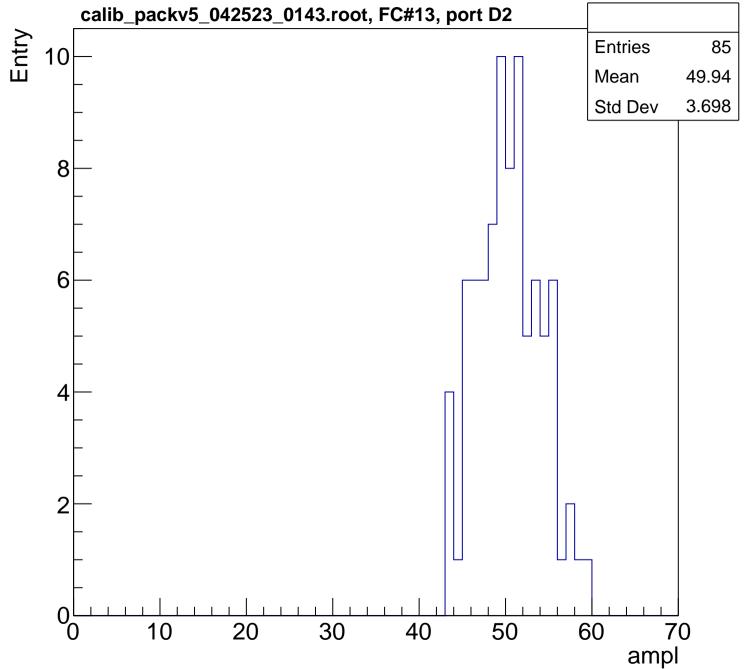


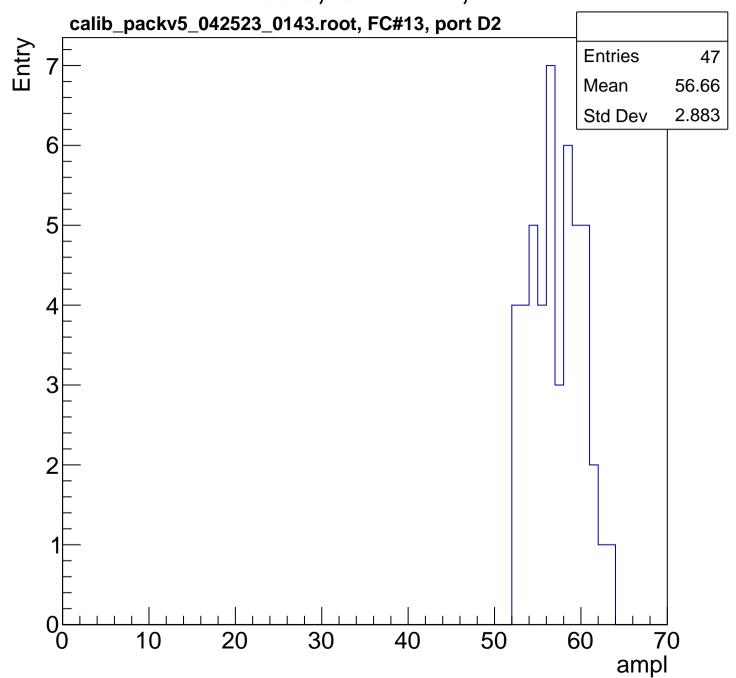
B1L003S, U8-ch71, adc7 calib\_packv5\_042523\_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

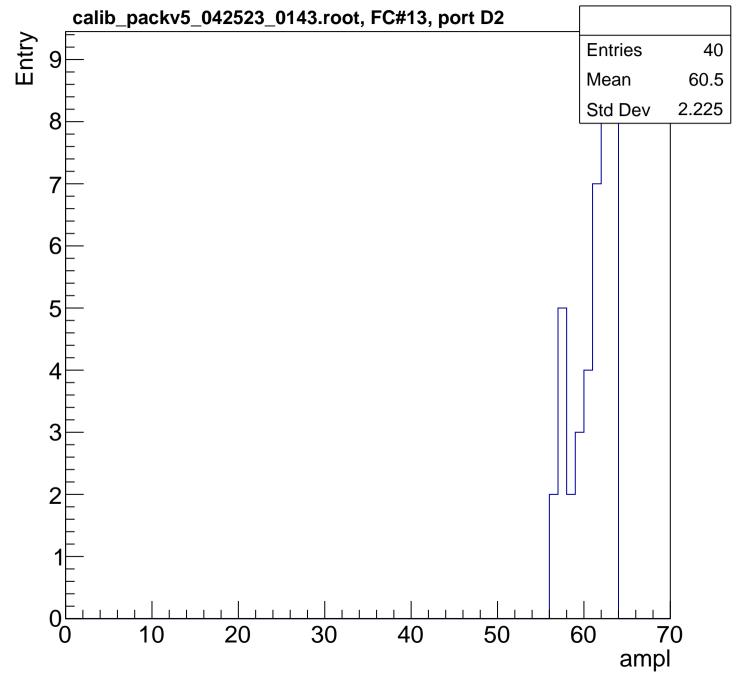


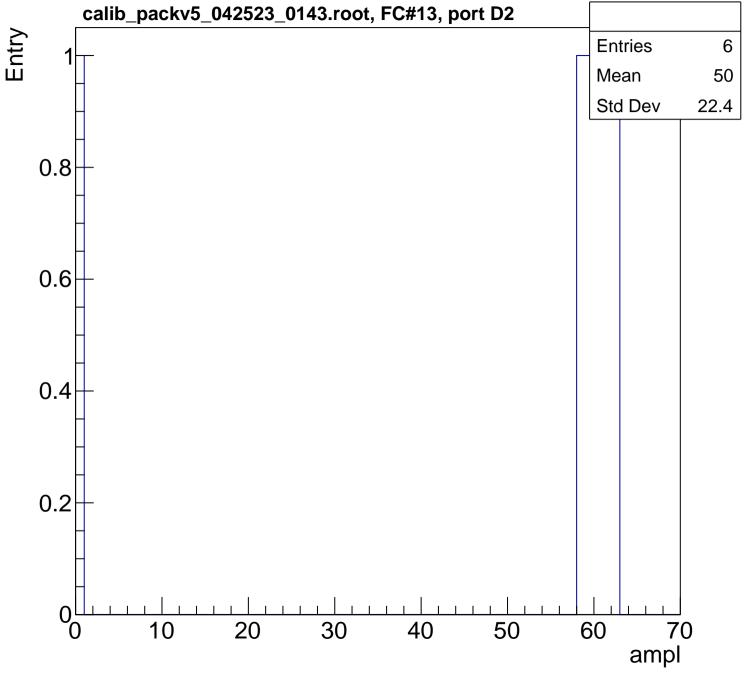


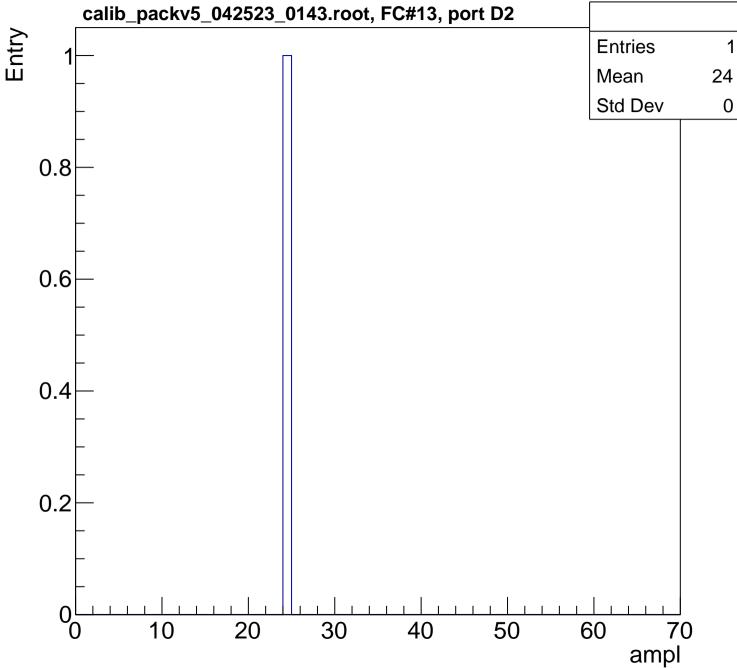


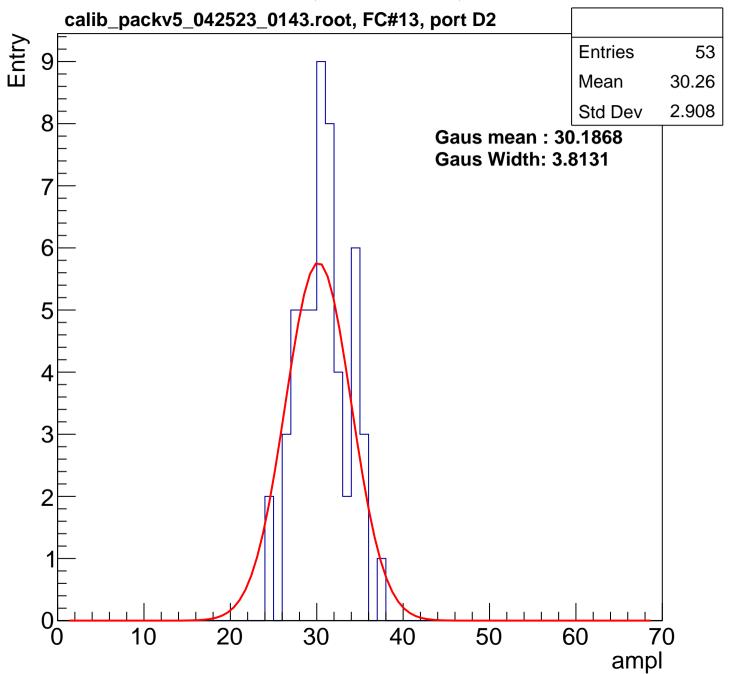


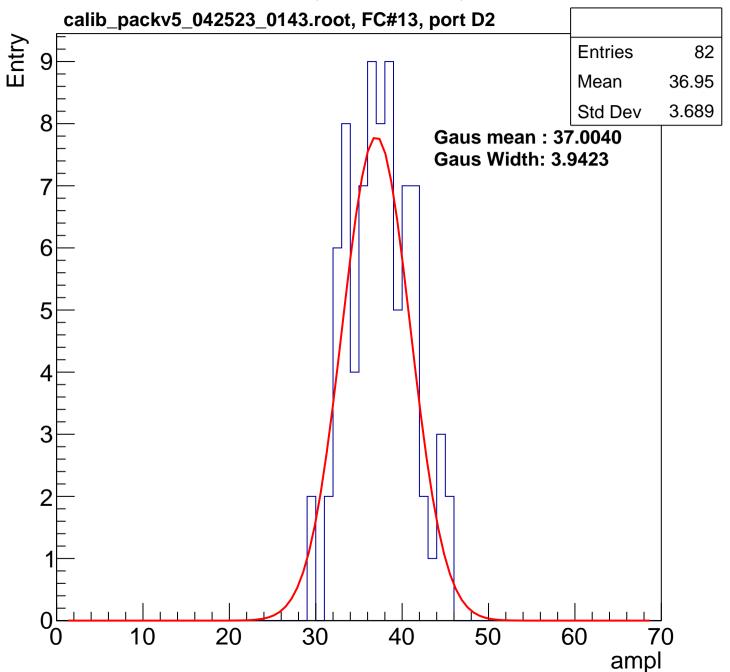


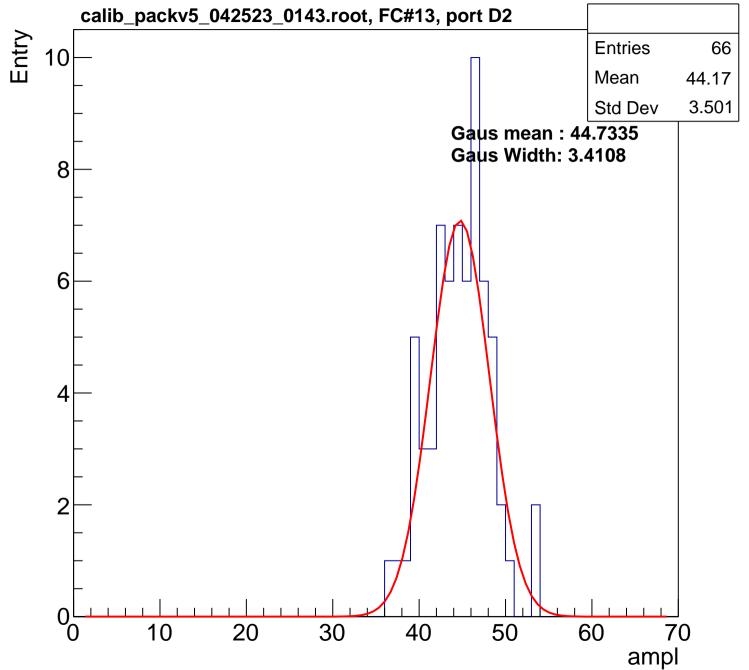


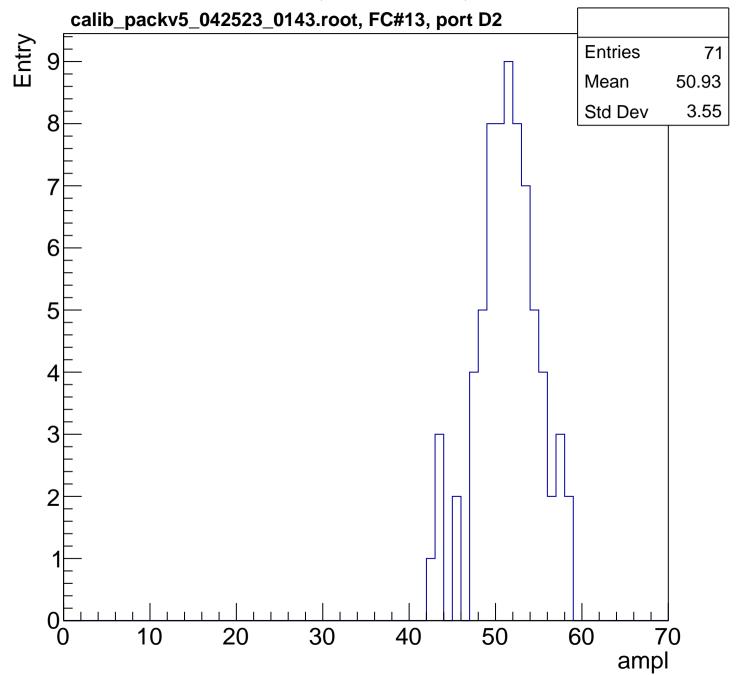


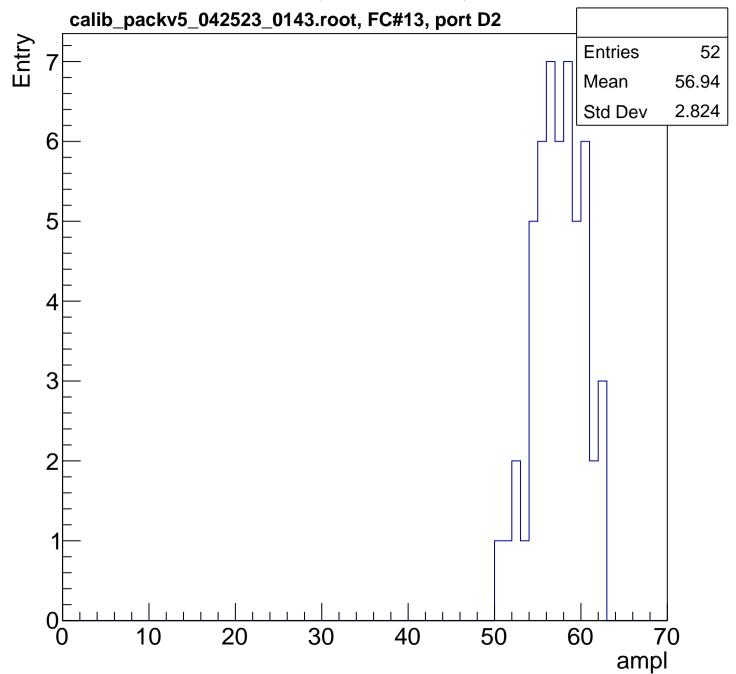


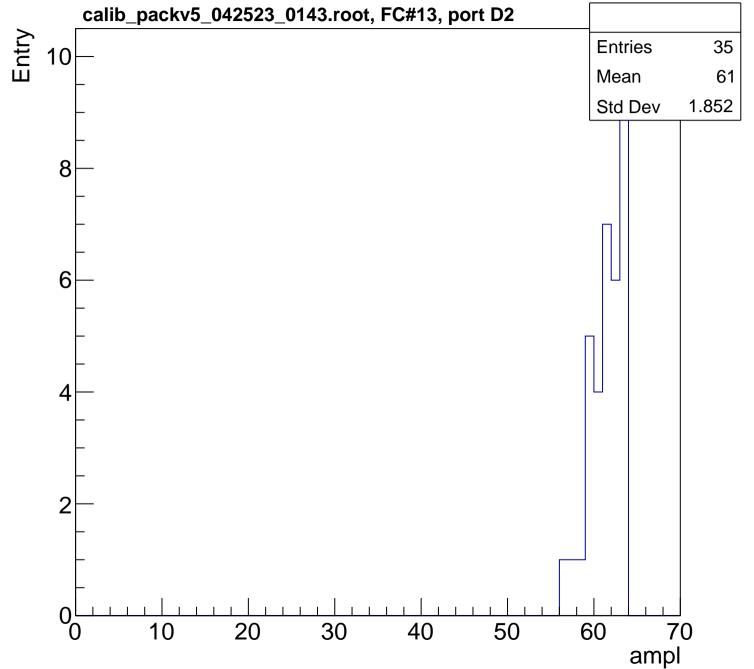


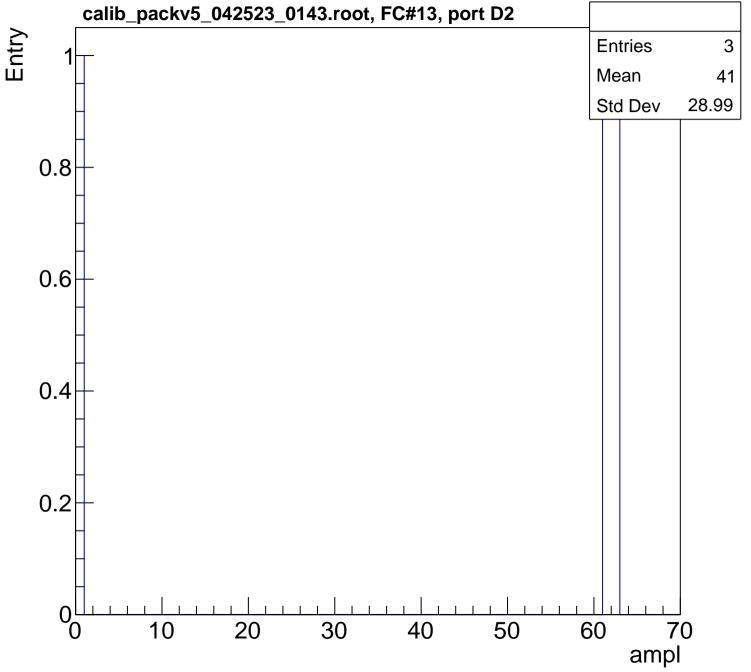




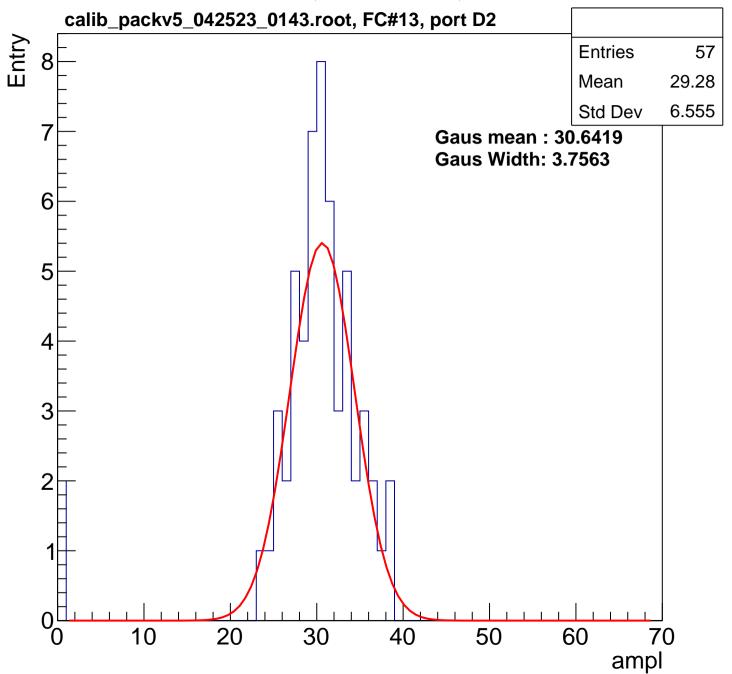


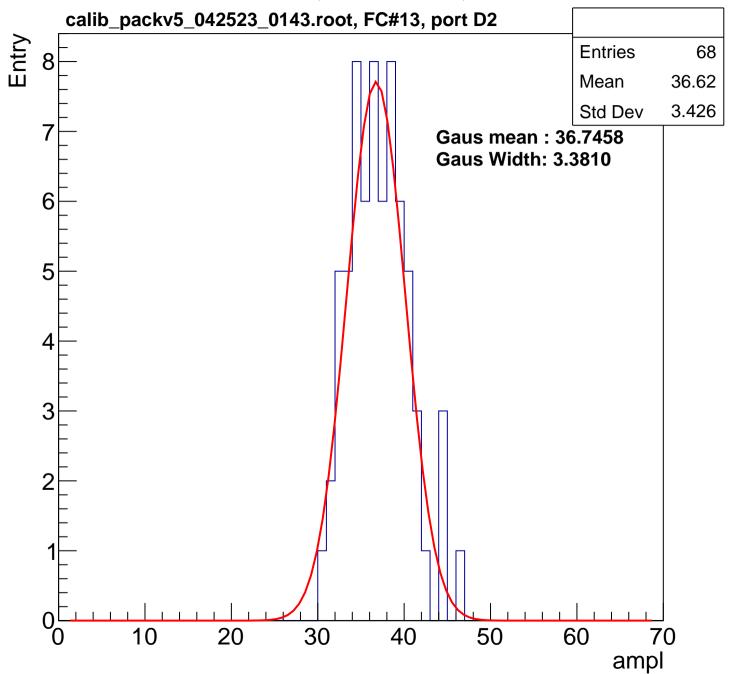


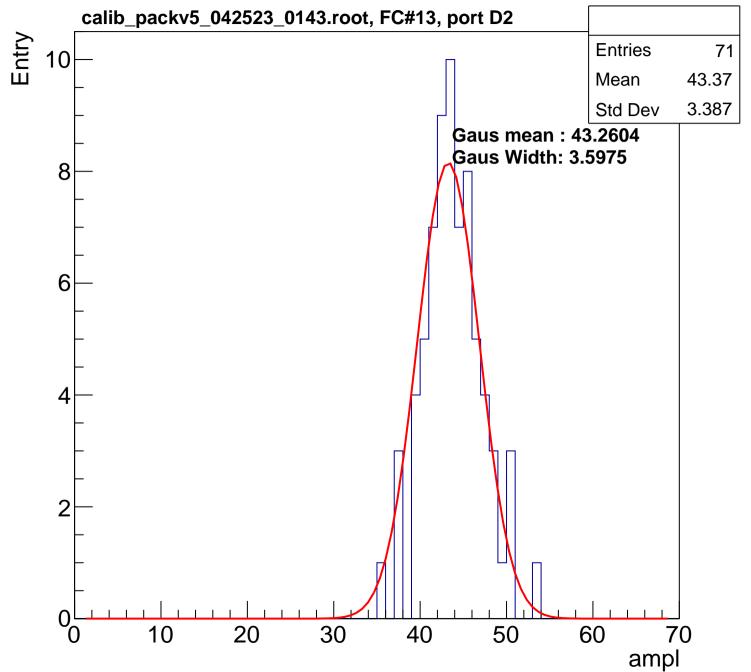


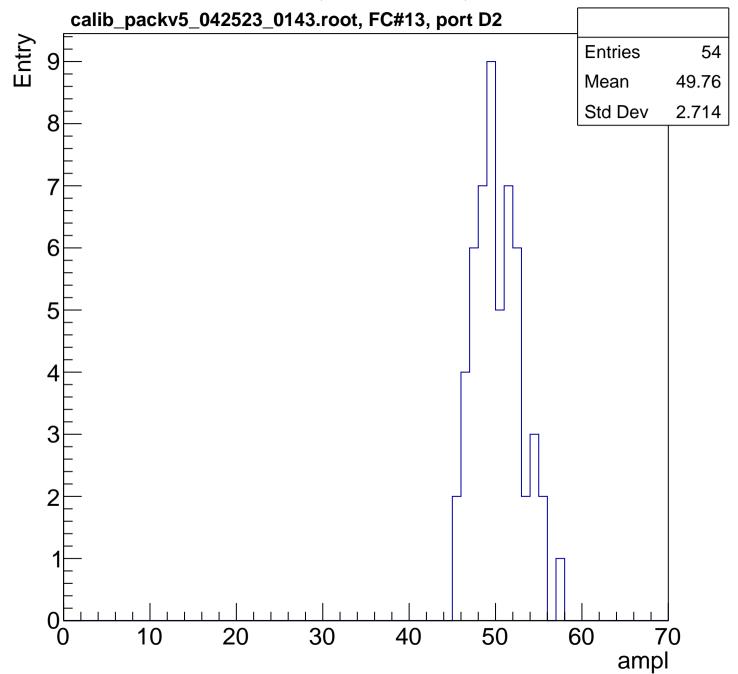


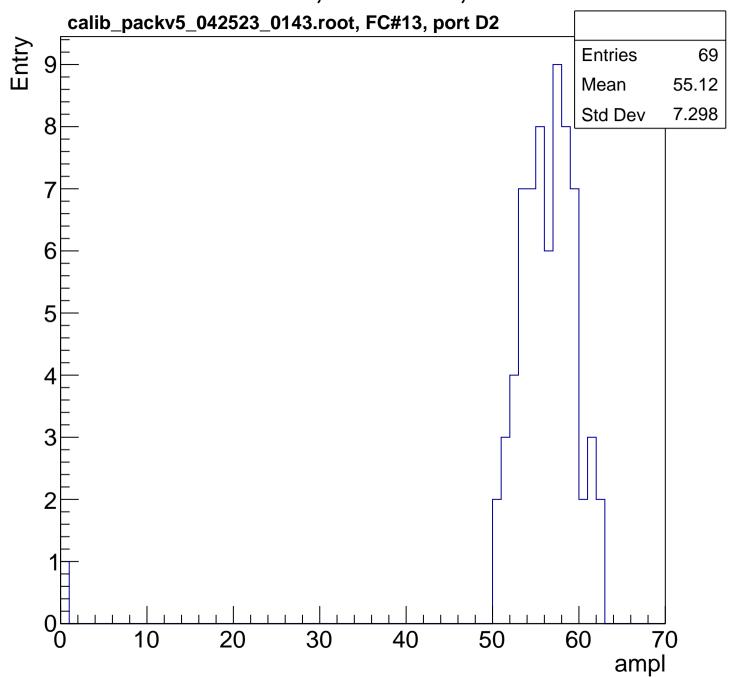
B1L003S, U8-ch73, adc7 calib\_packv5\_042523\_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

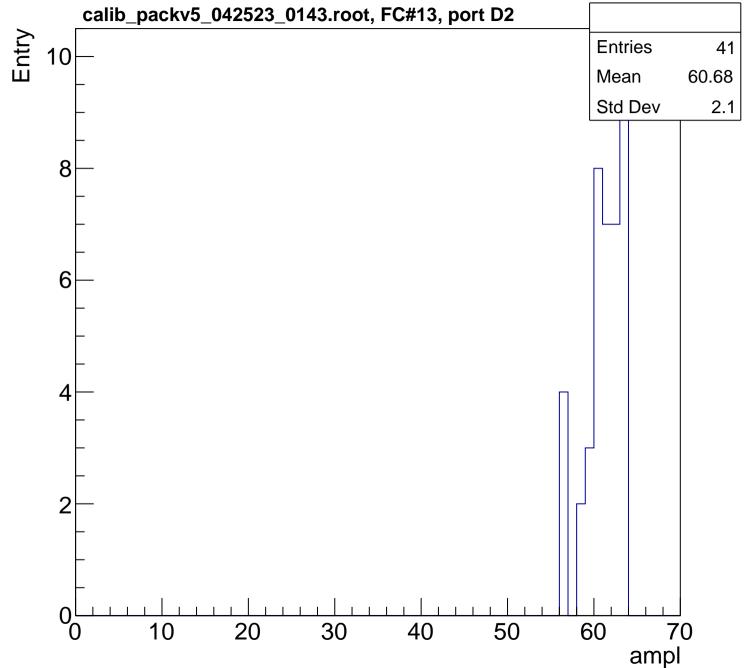


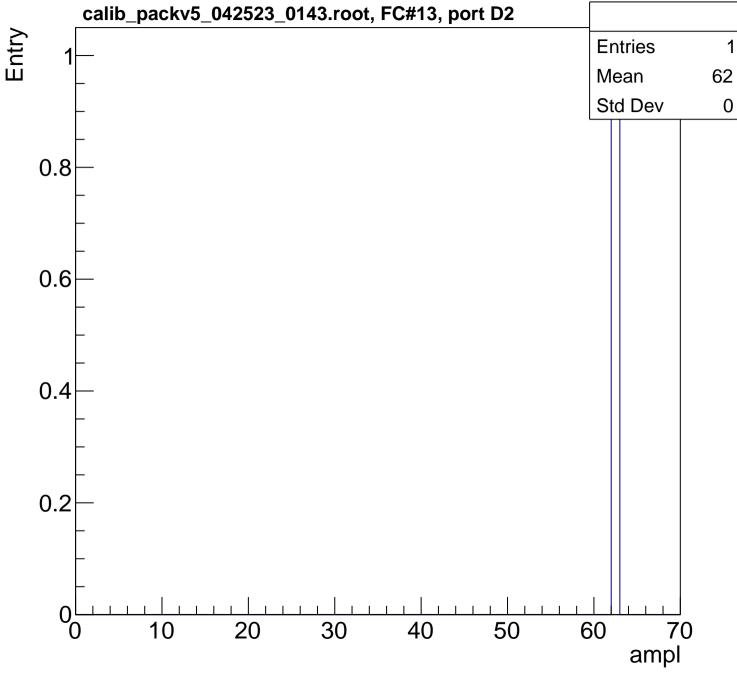


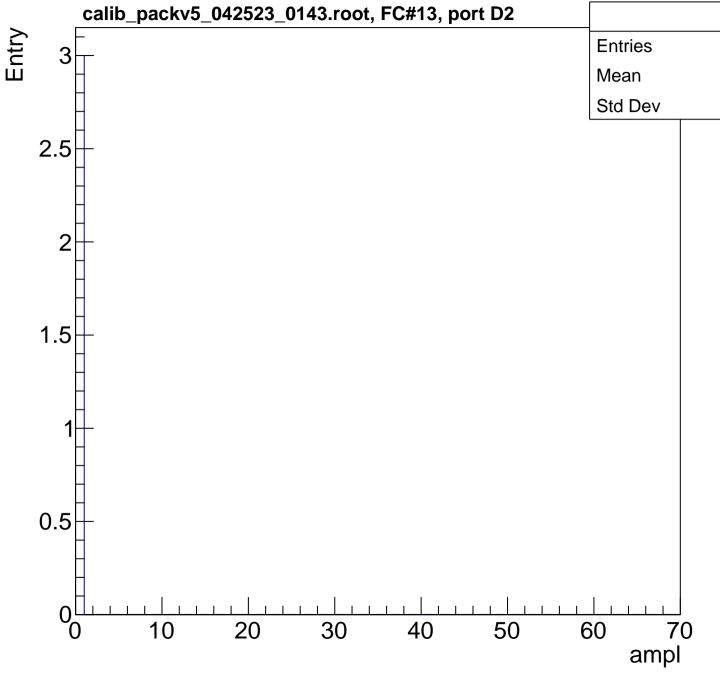


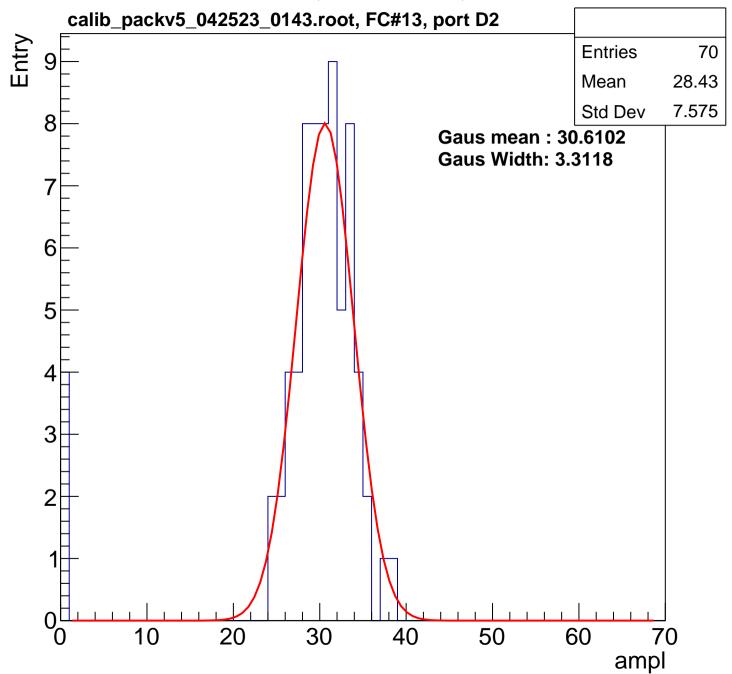


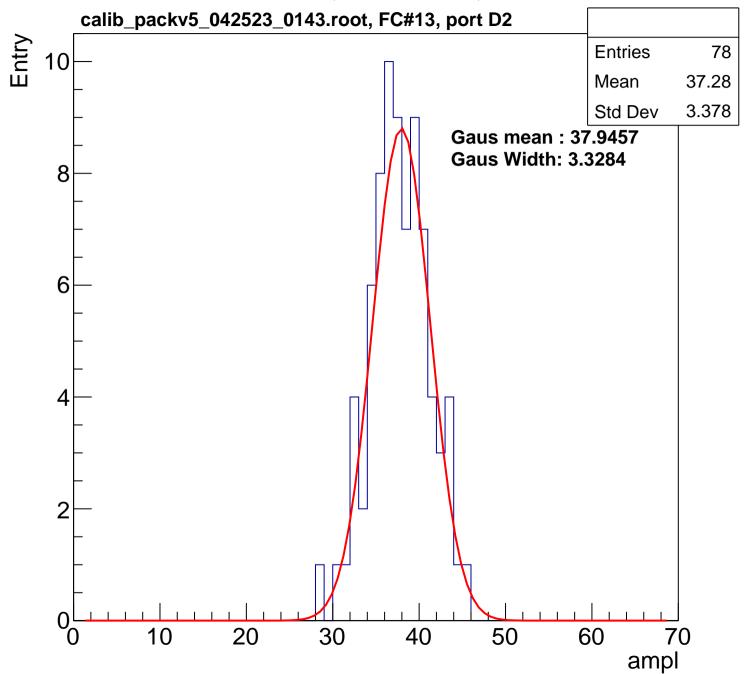


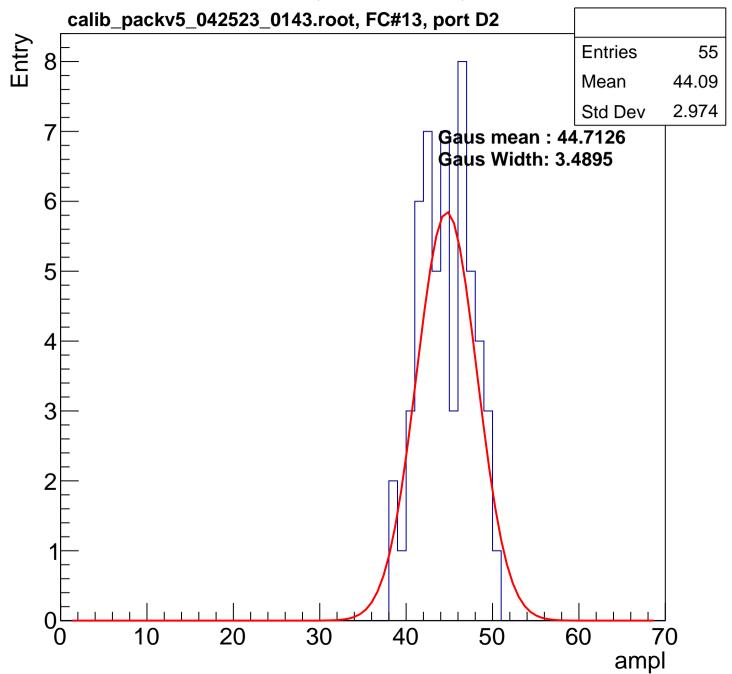


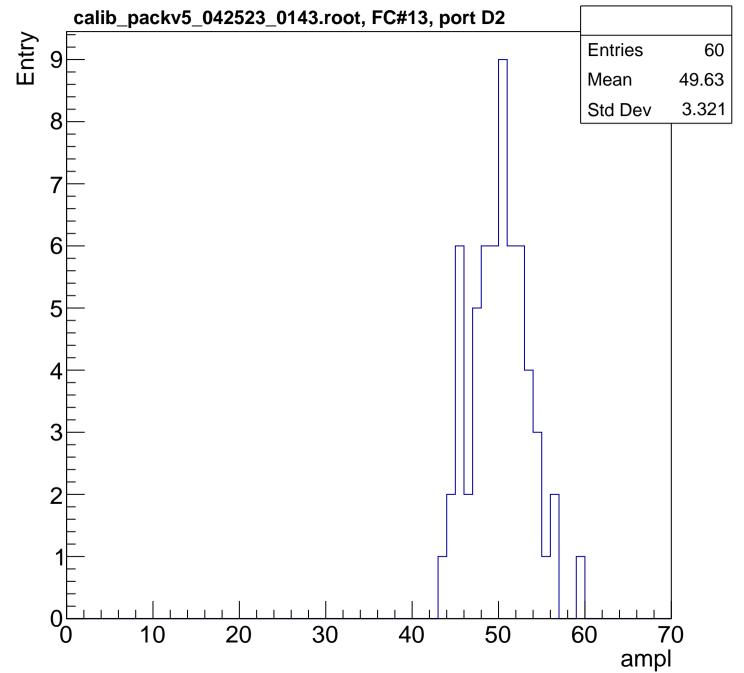


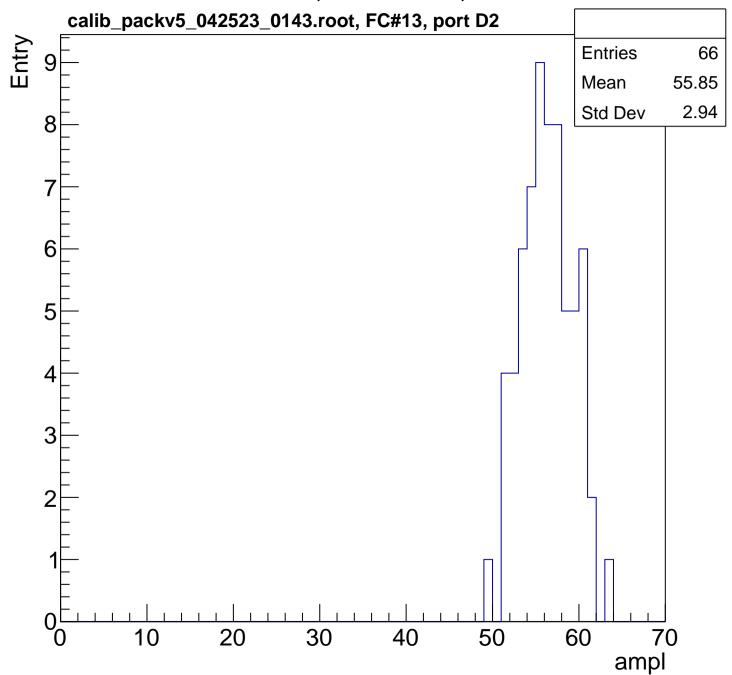


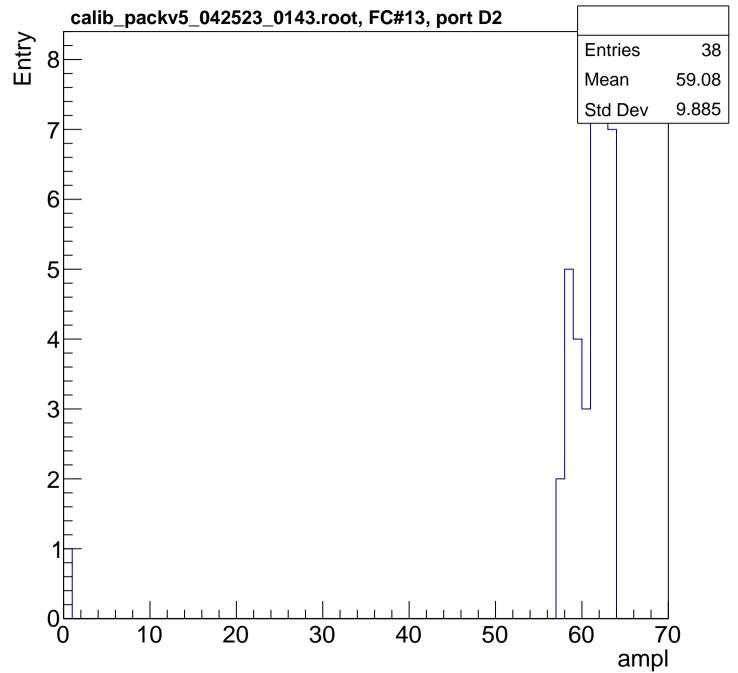


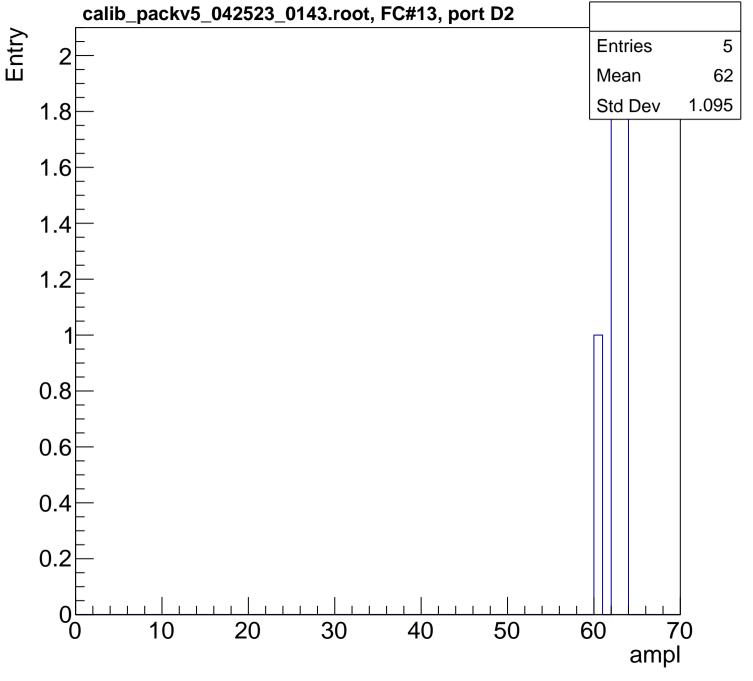


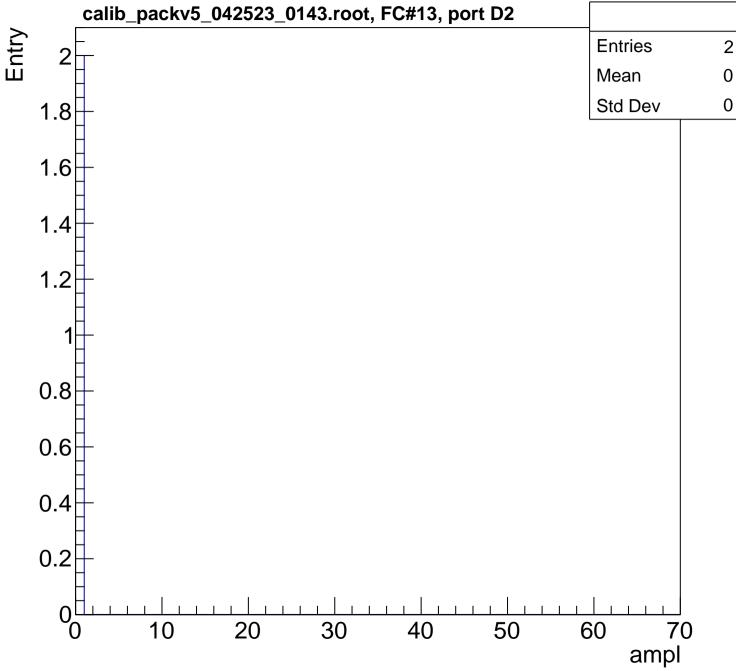


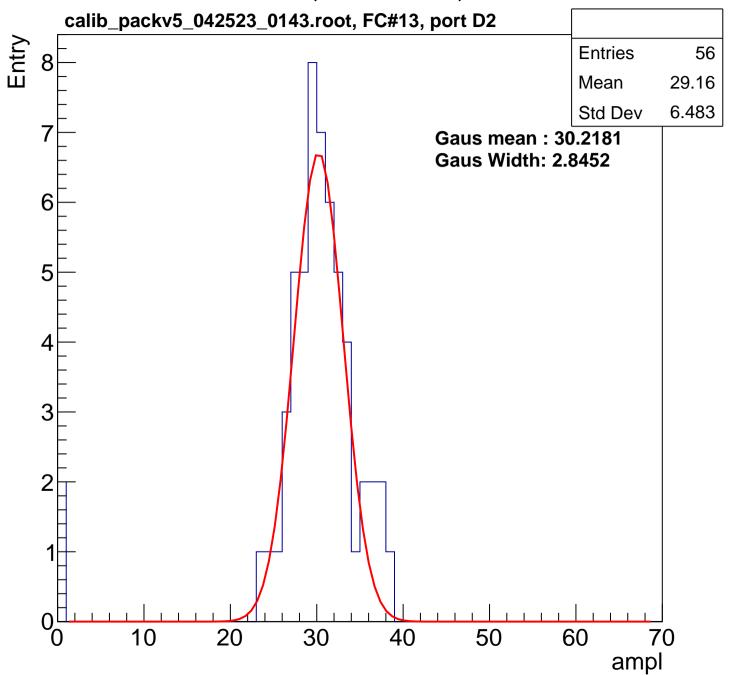


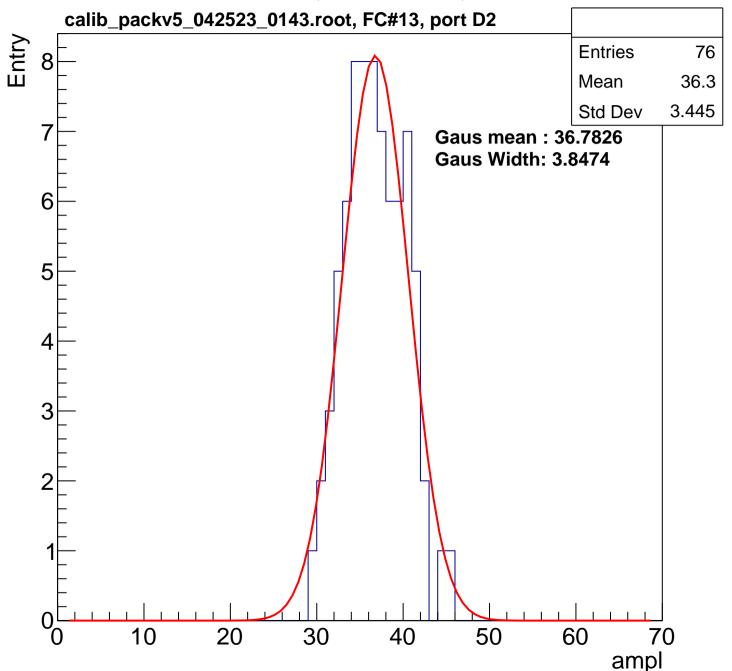


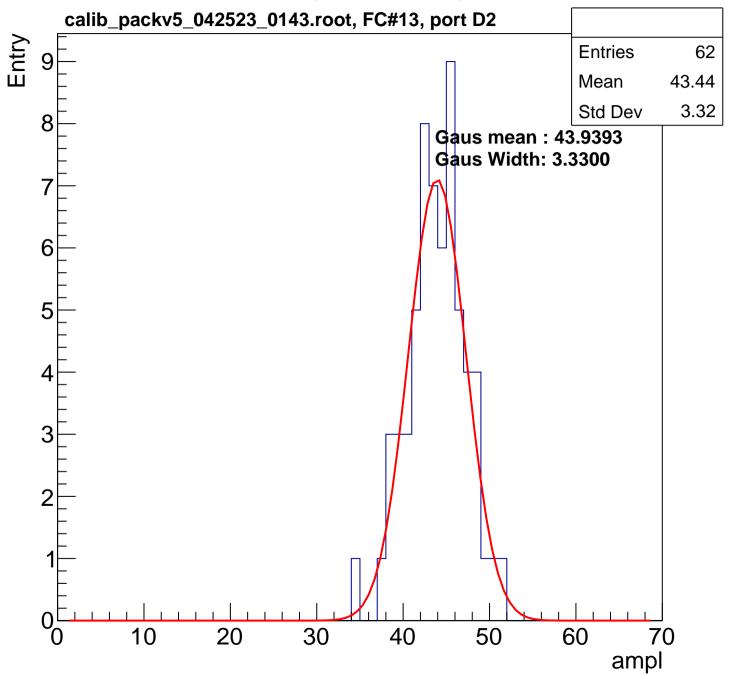


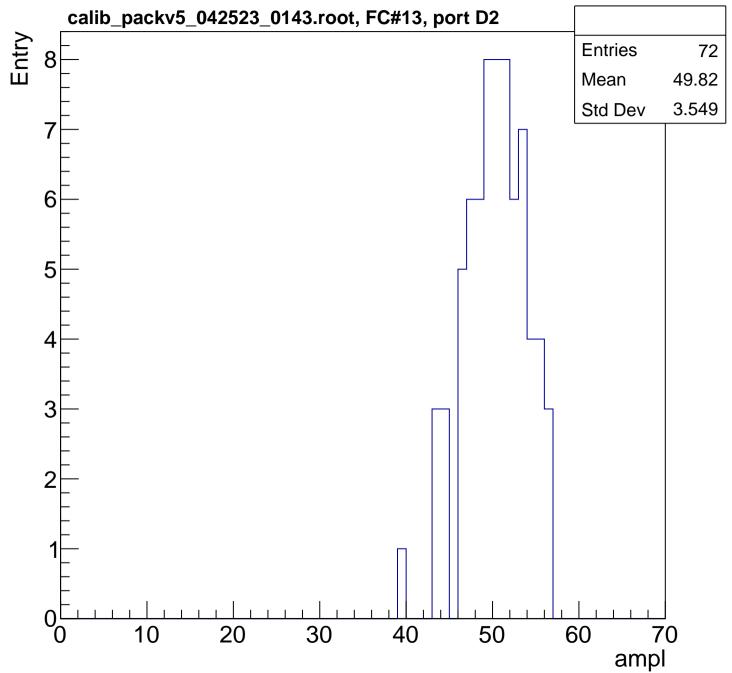


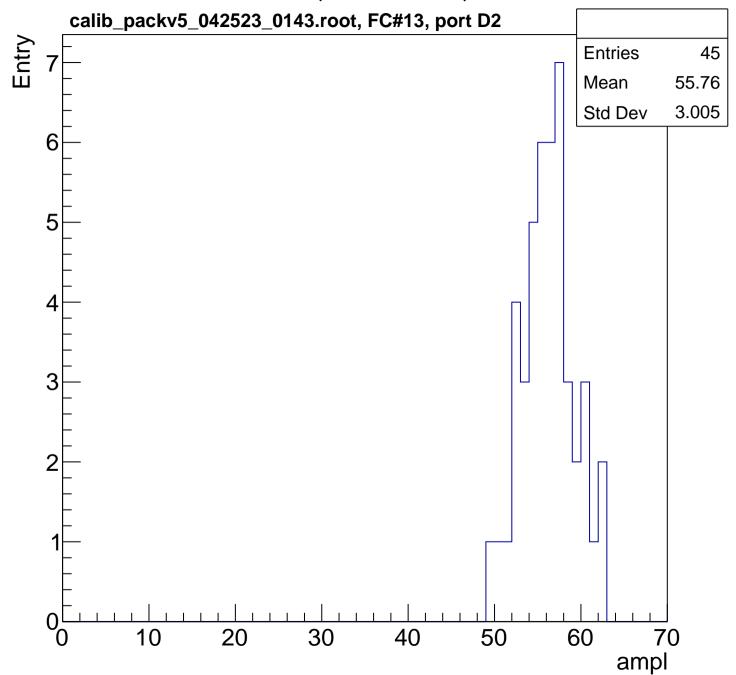


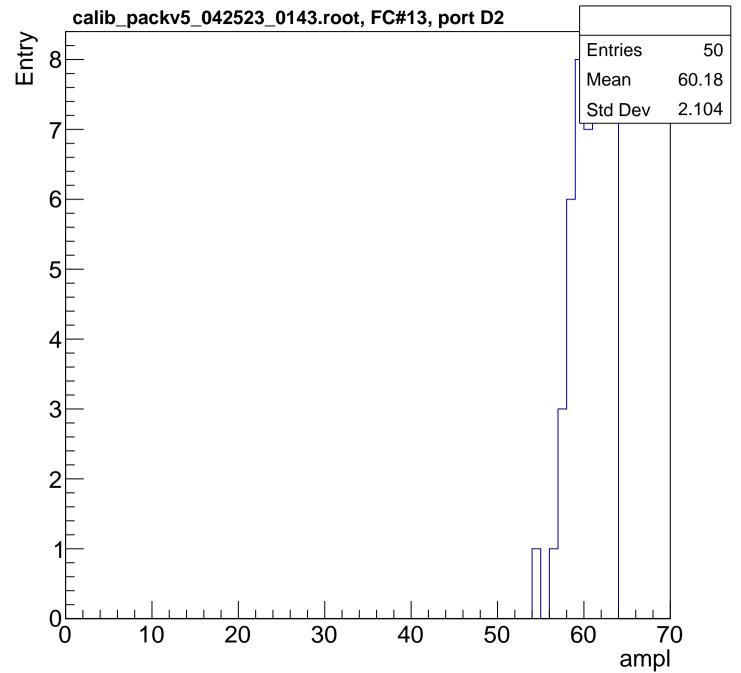


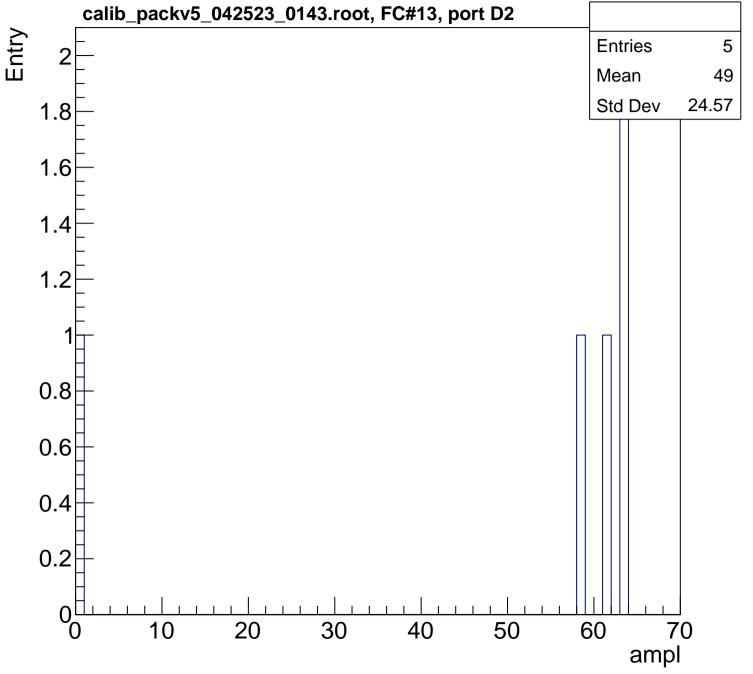




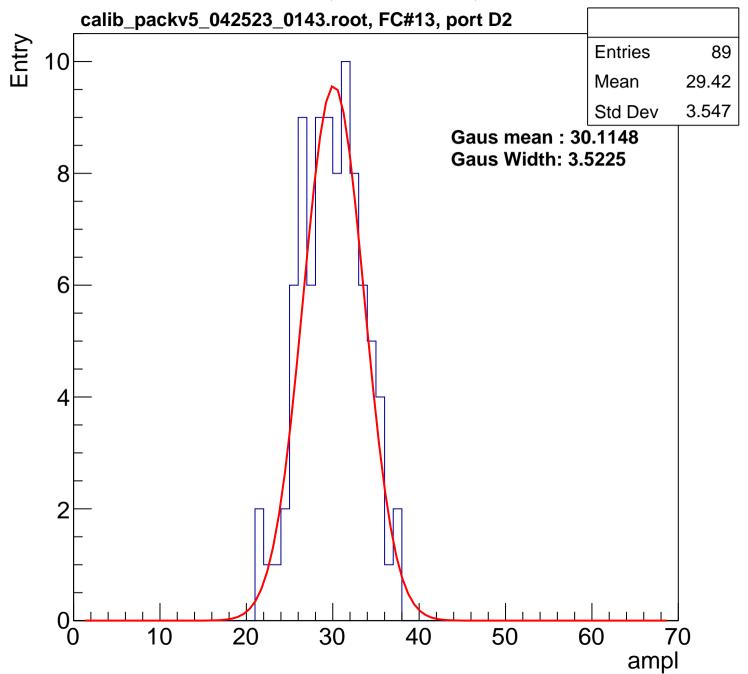


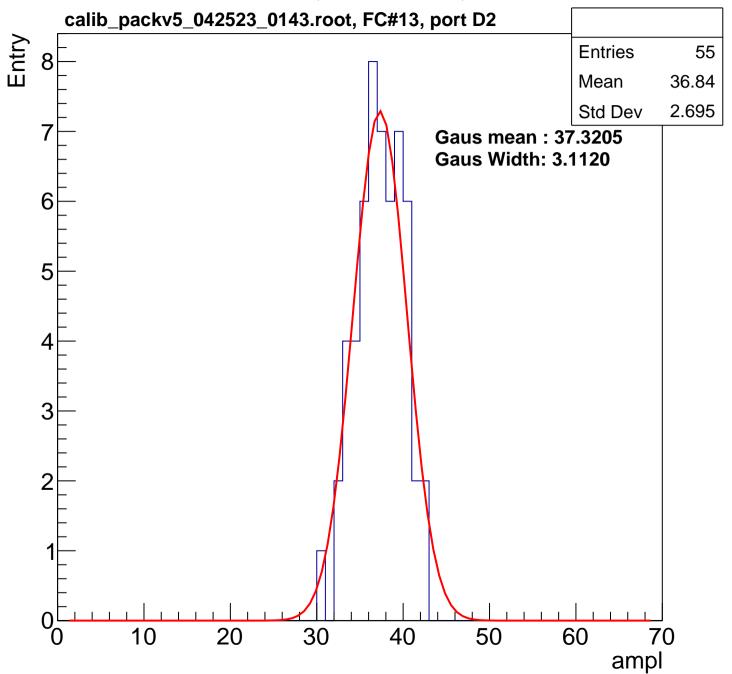


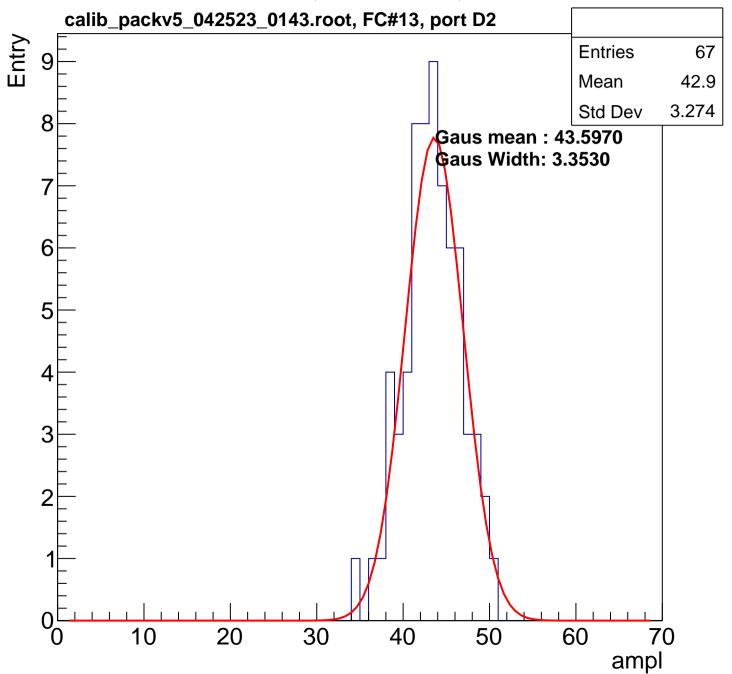


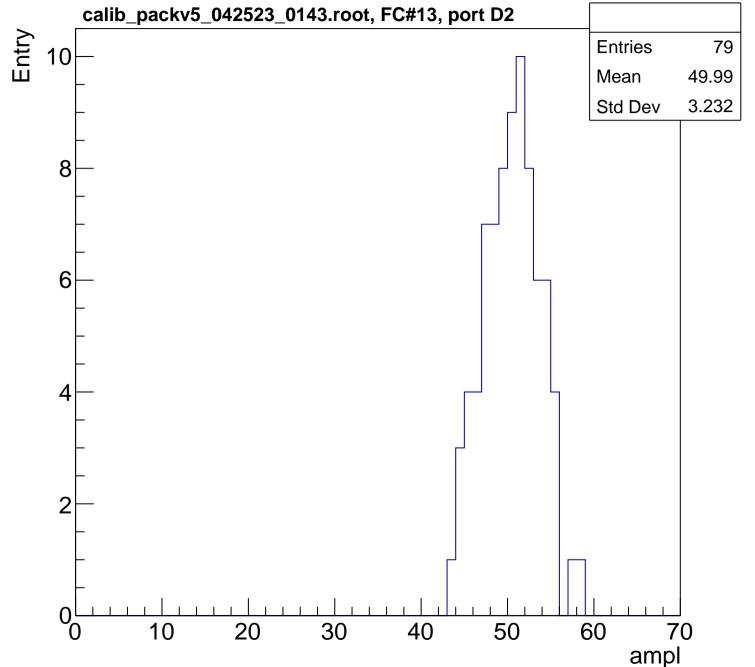


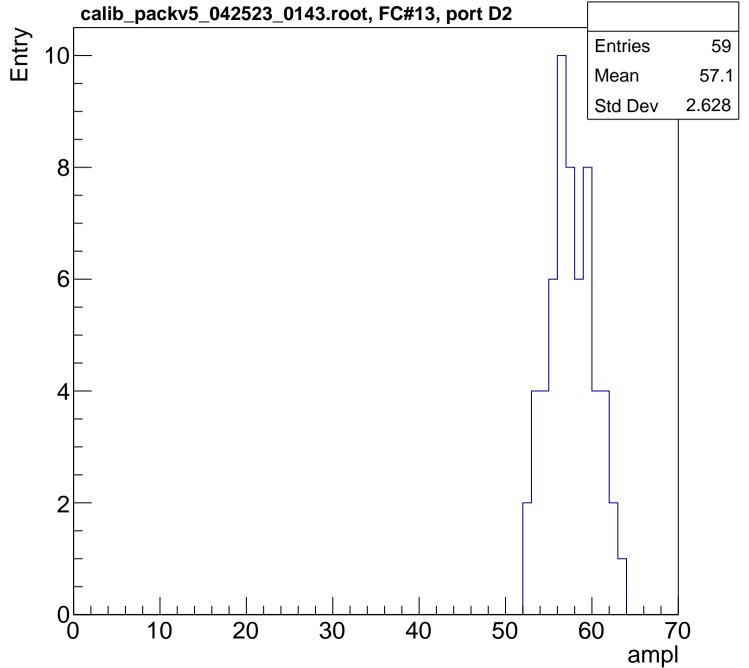


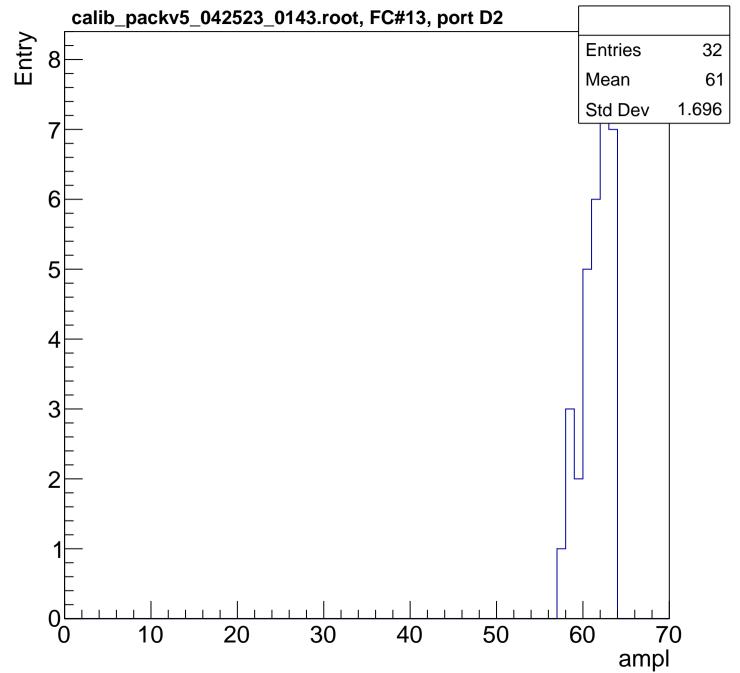


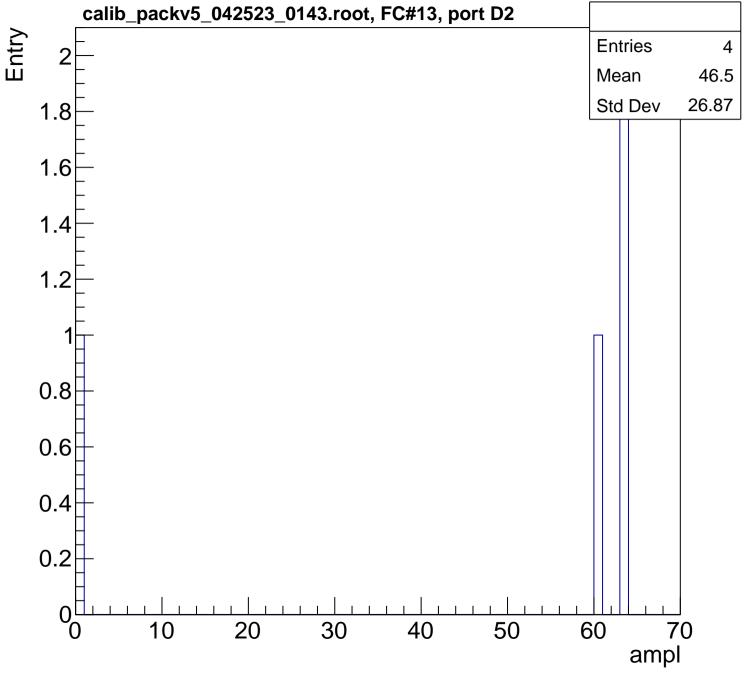




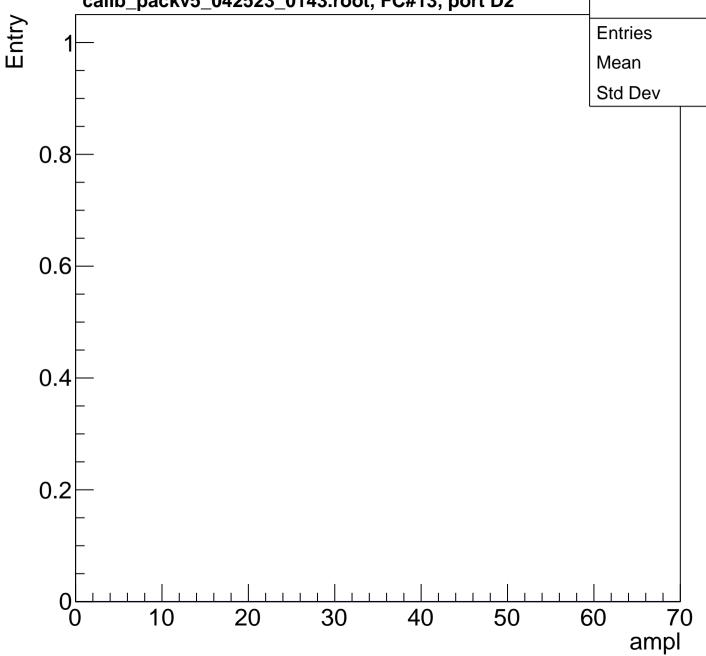


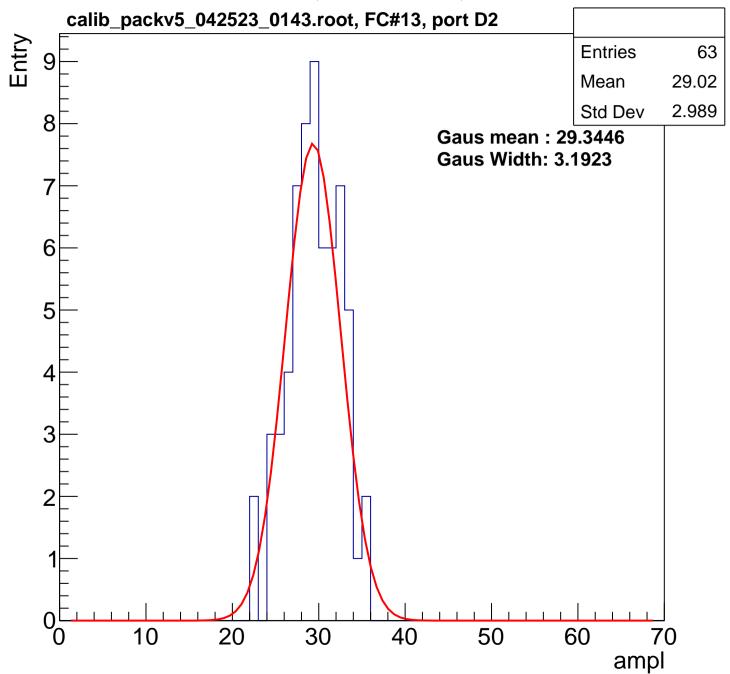


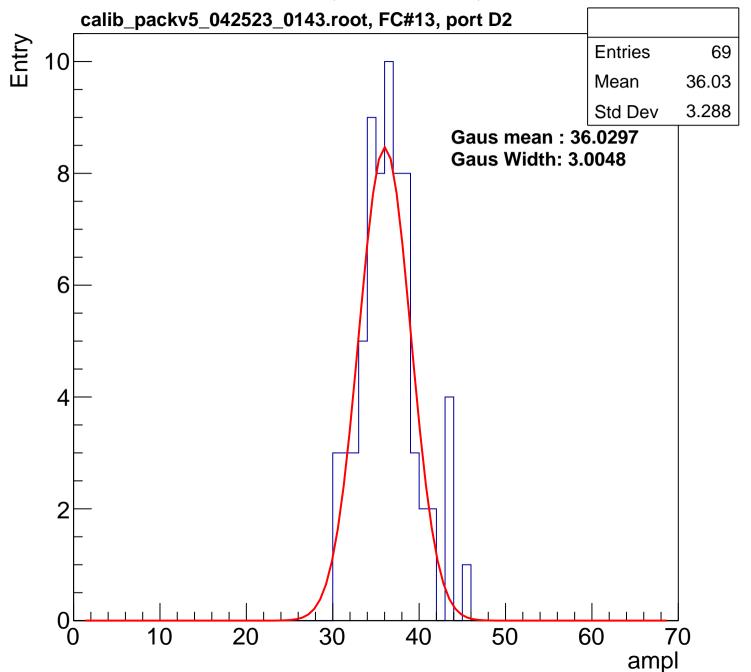


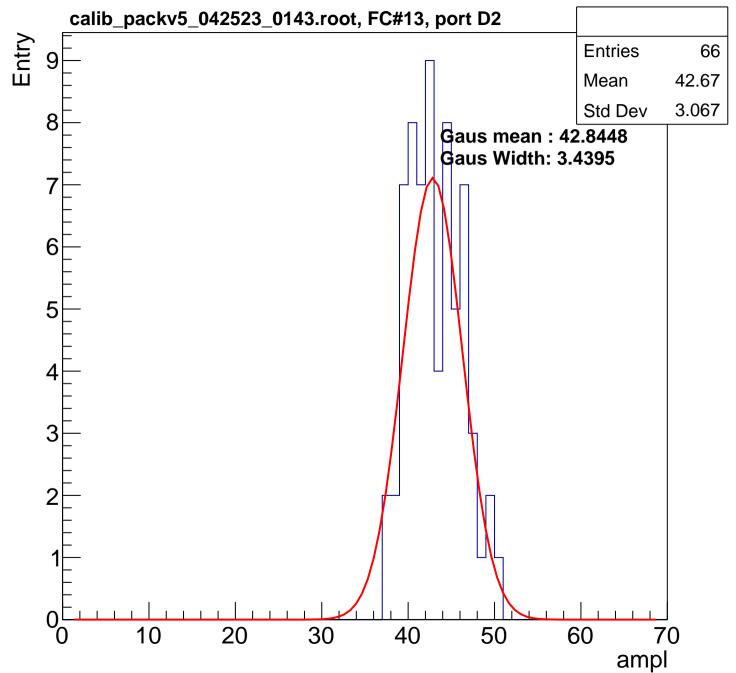


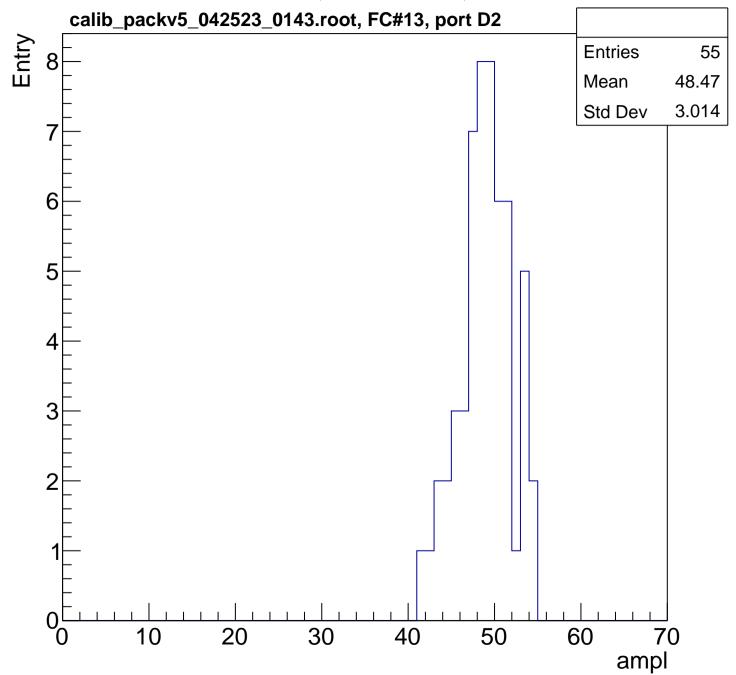
# B1L003S, U8-ch77, adc7 calib\_packv5\_042523\_0143.root, FC#13, port D2

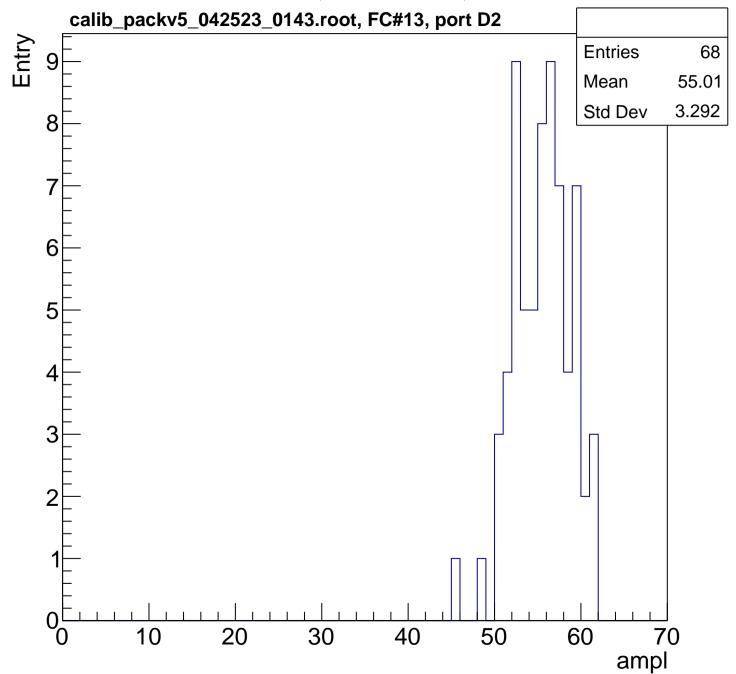


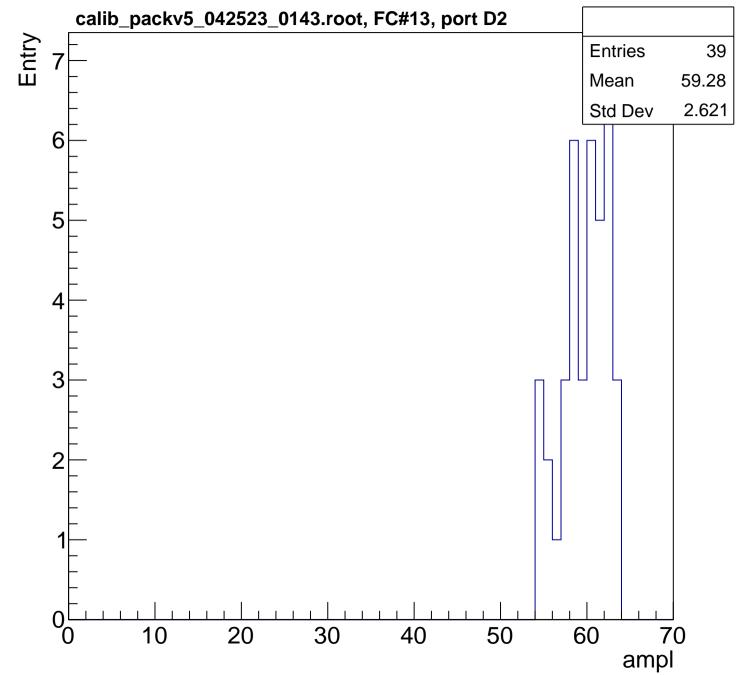


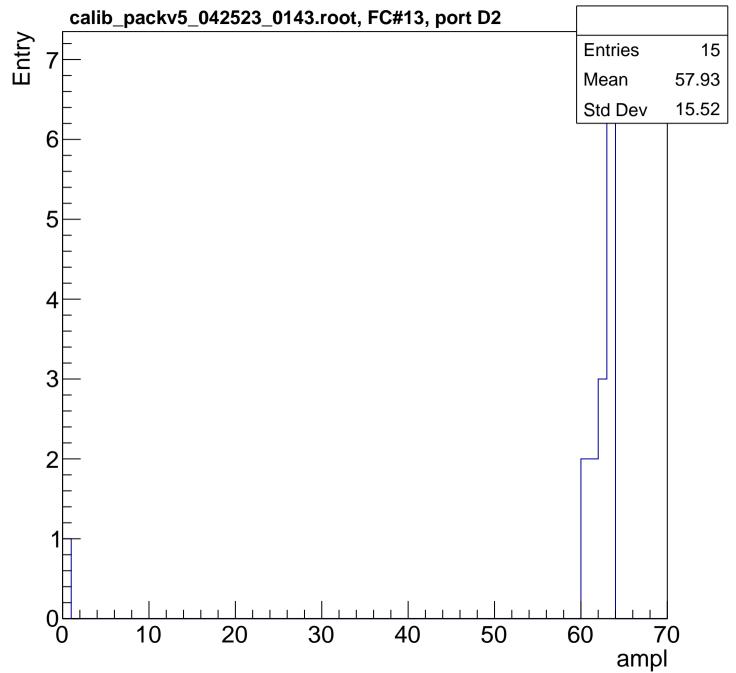


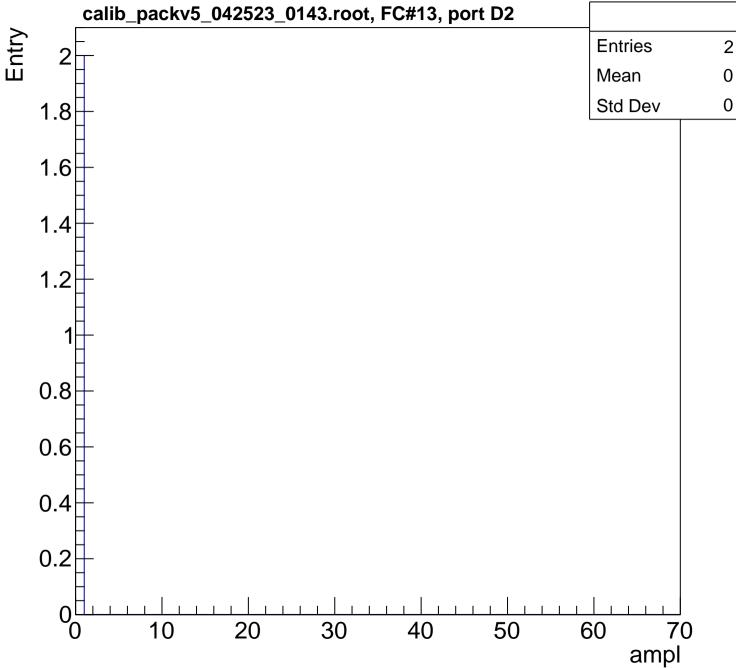


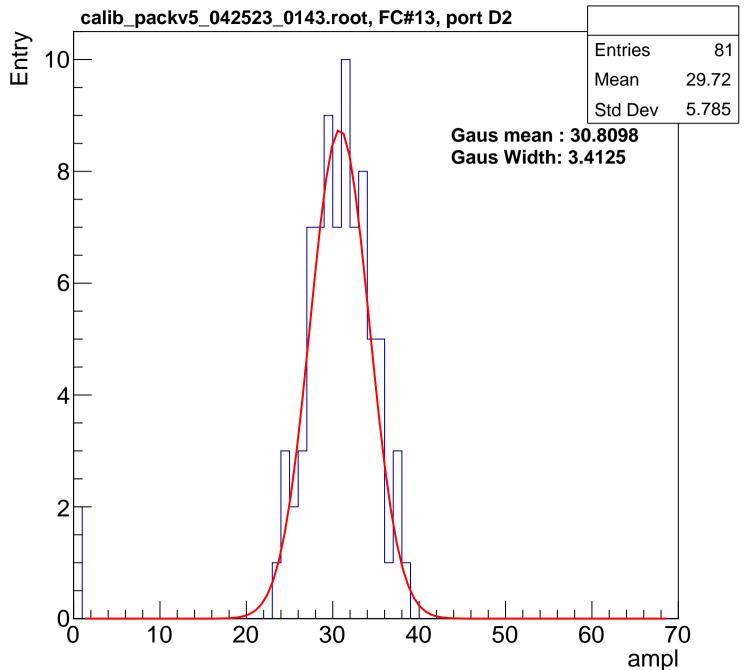


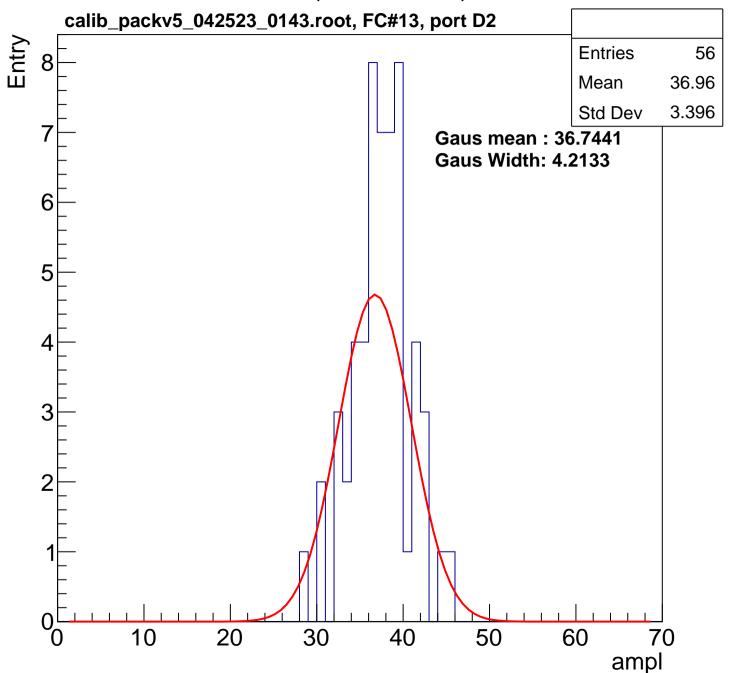


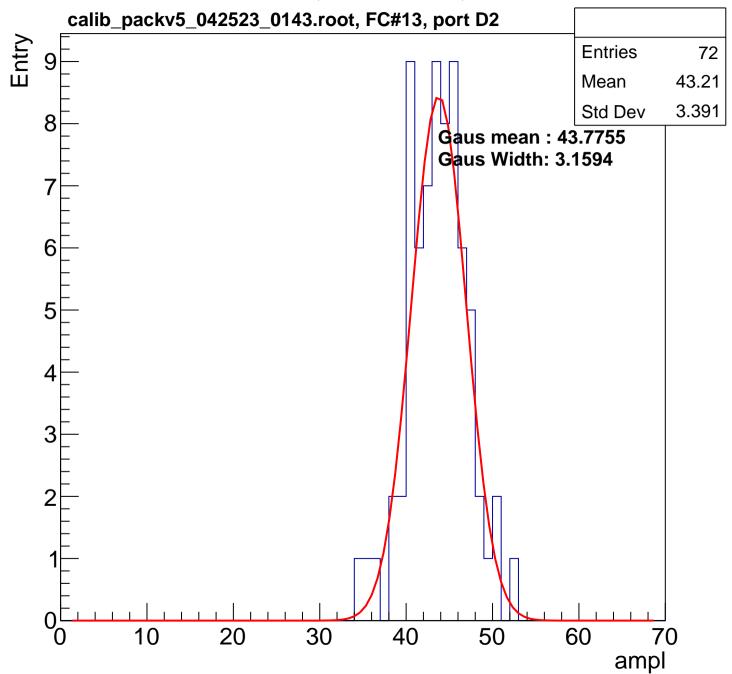


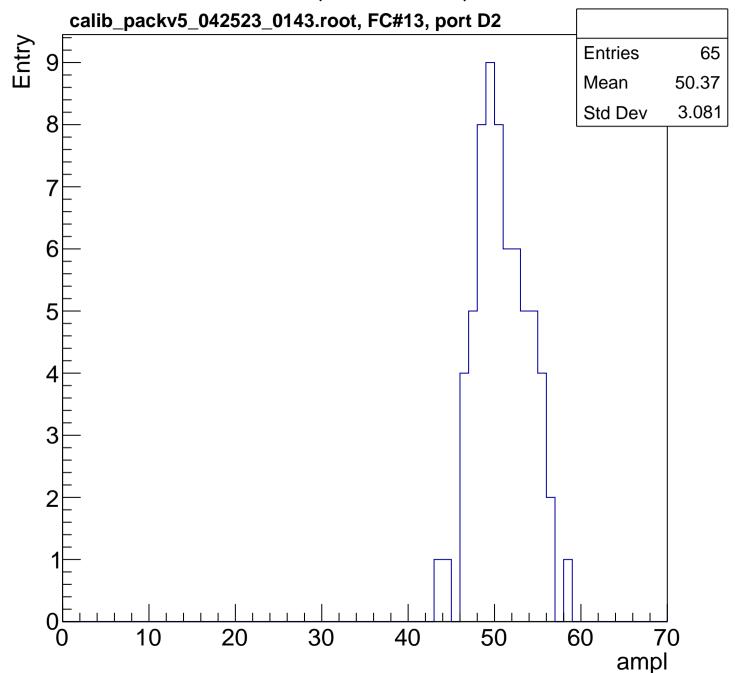


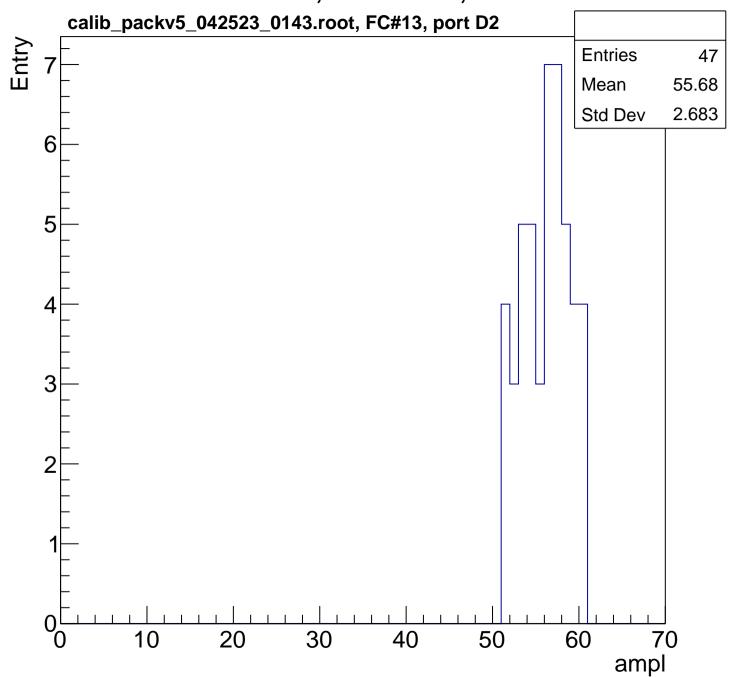


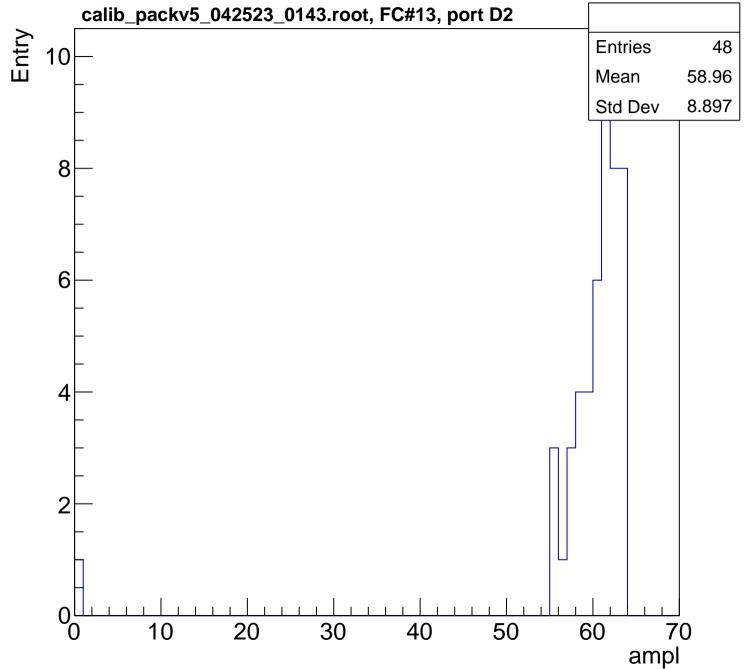


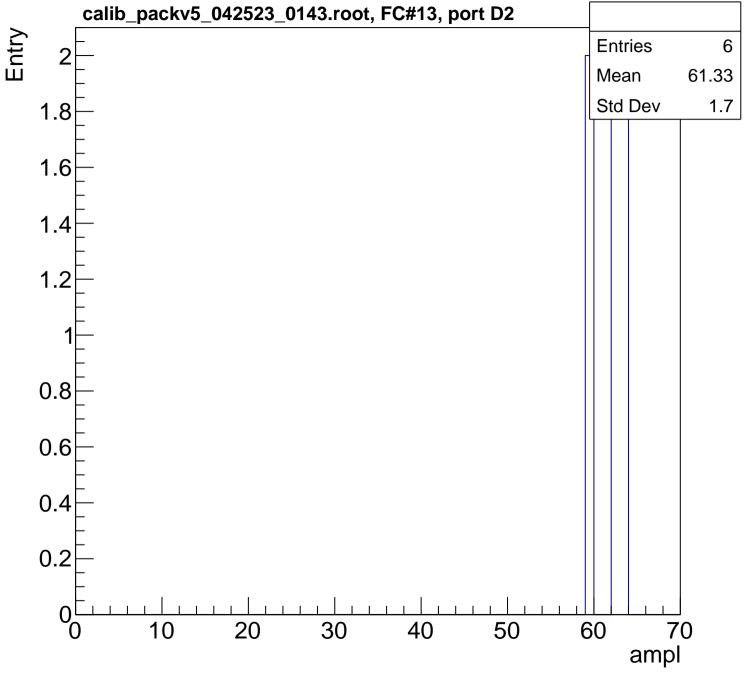




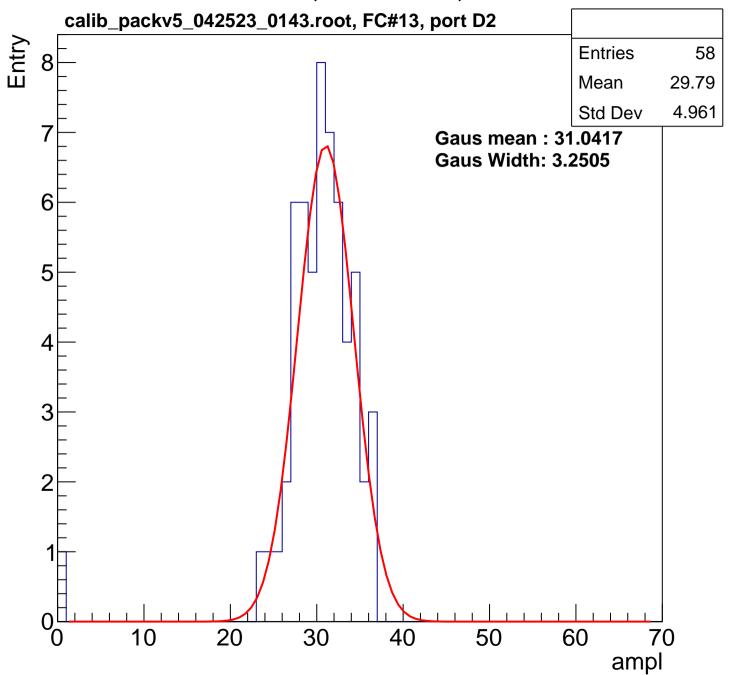


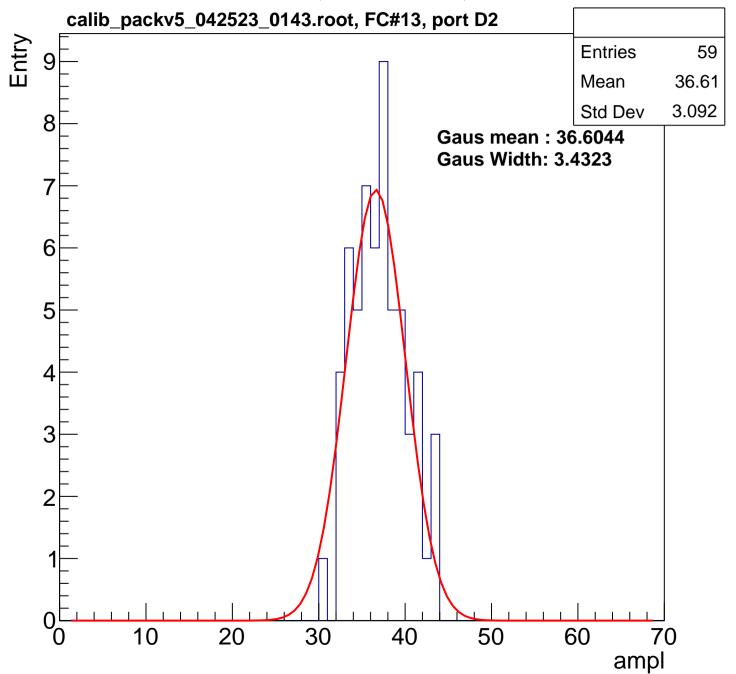


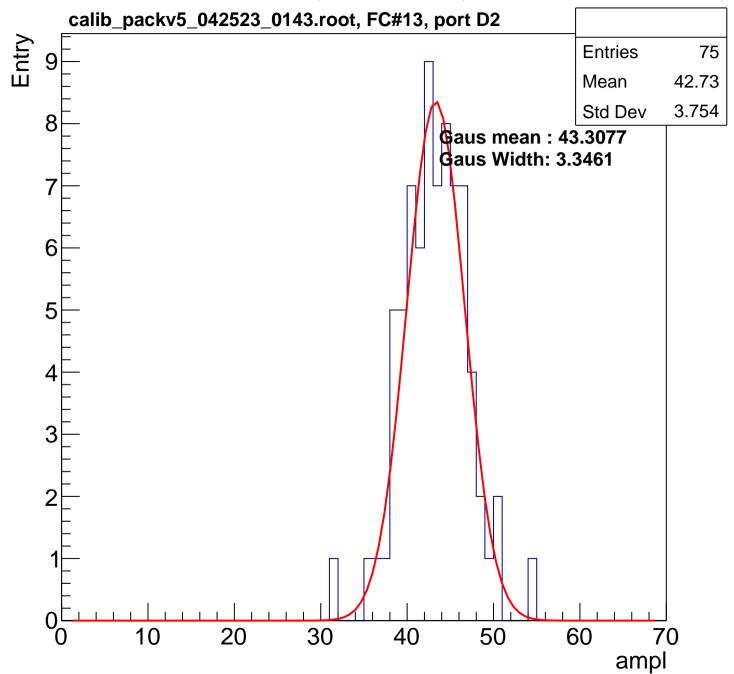


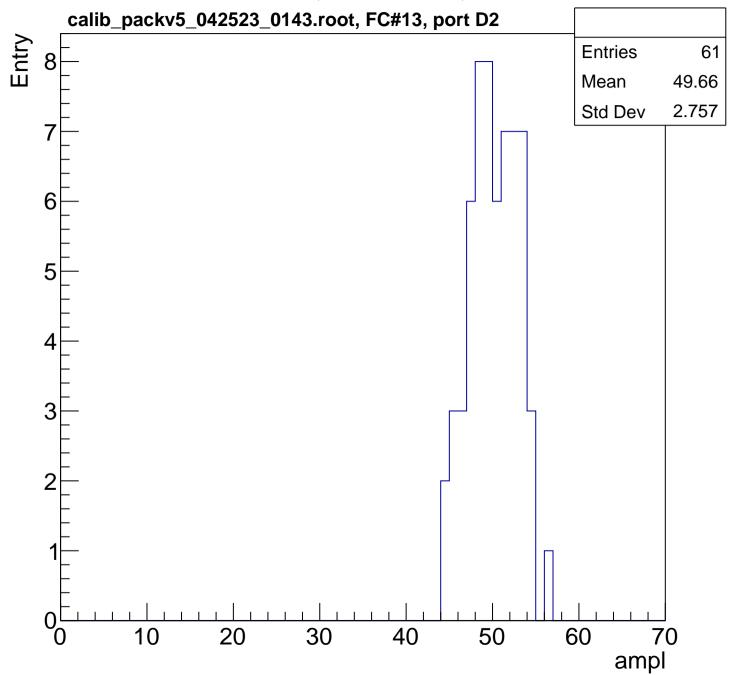


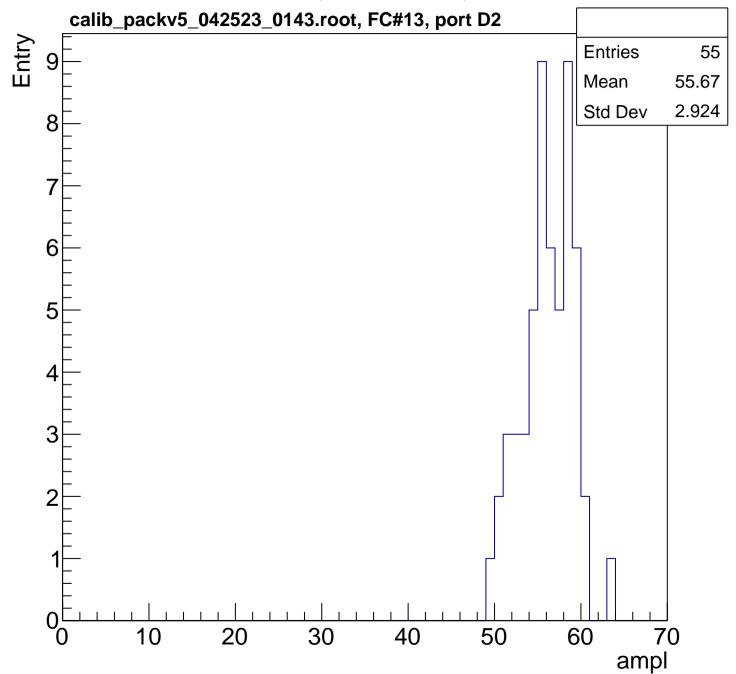


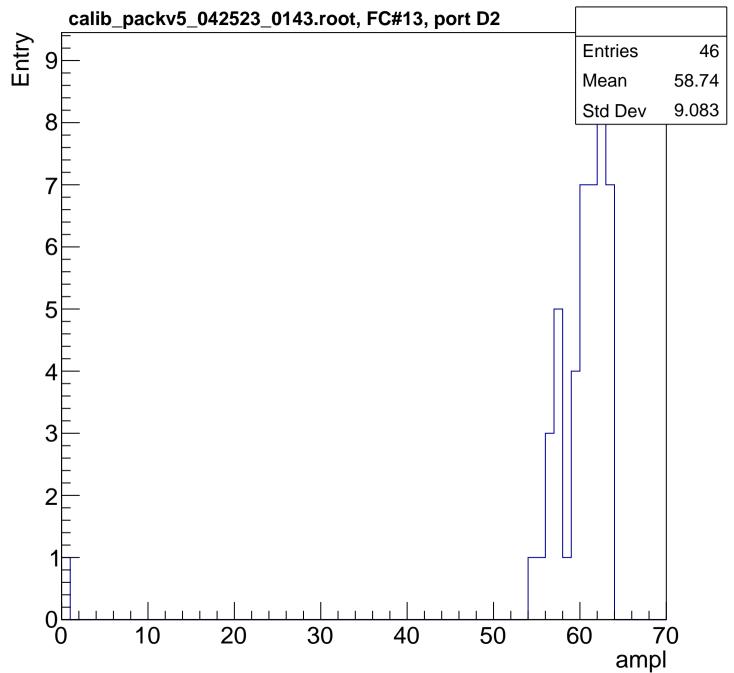


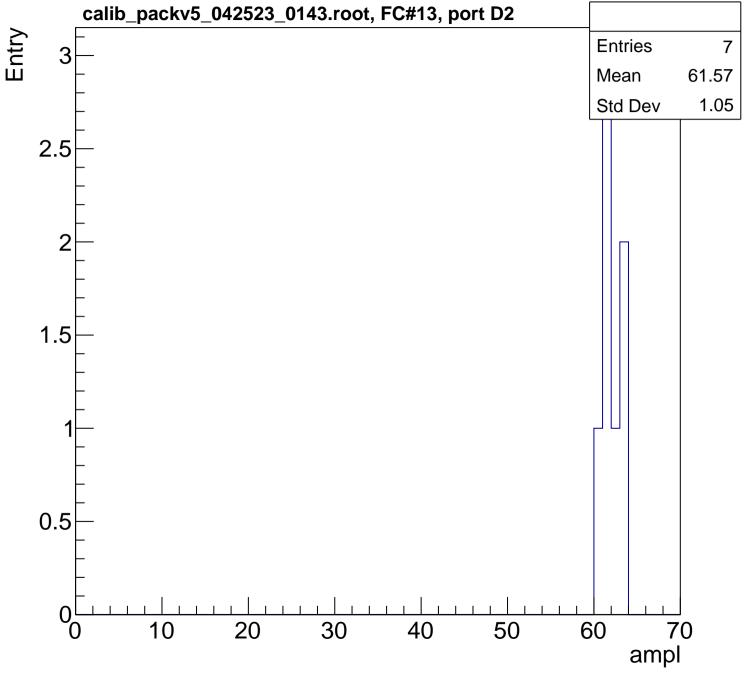




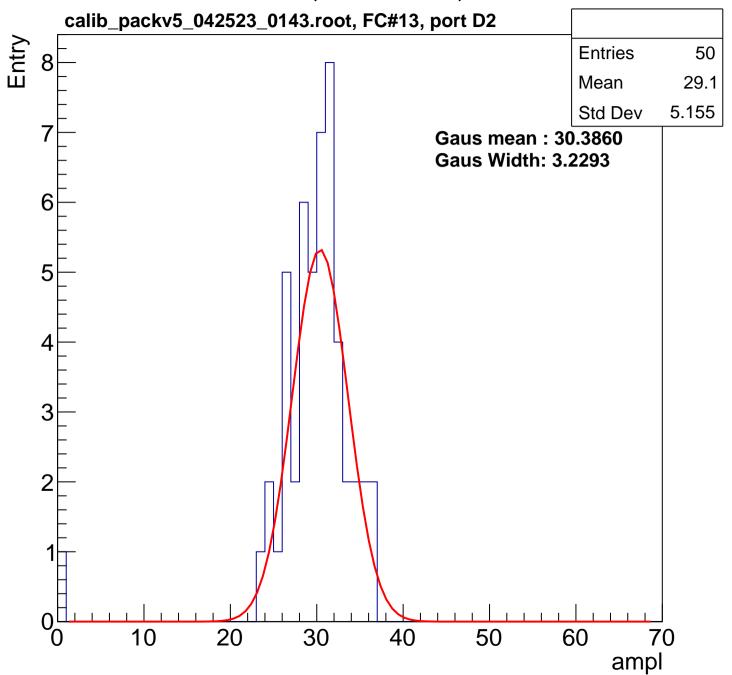


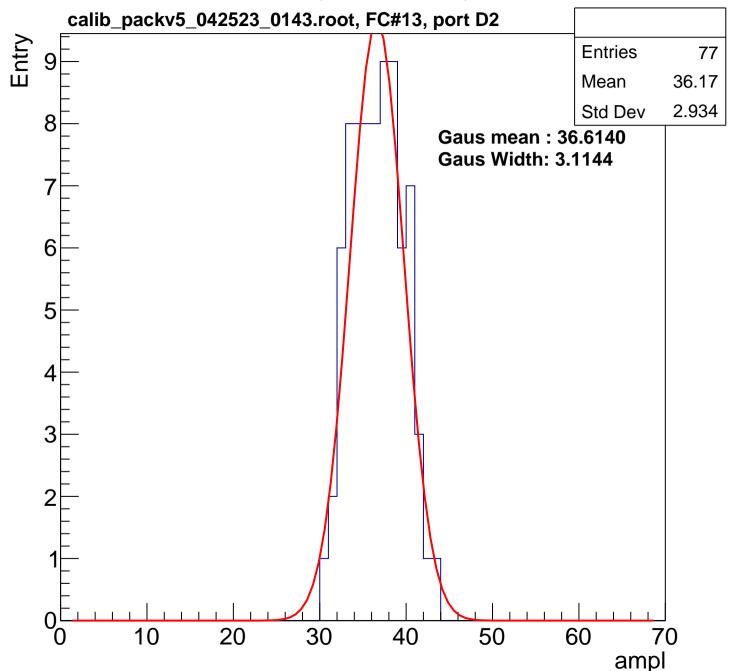


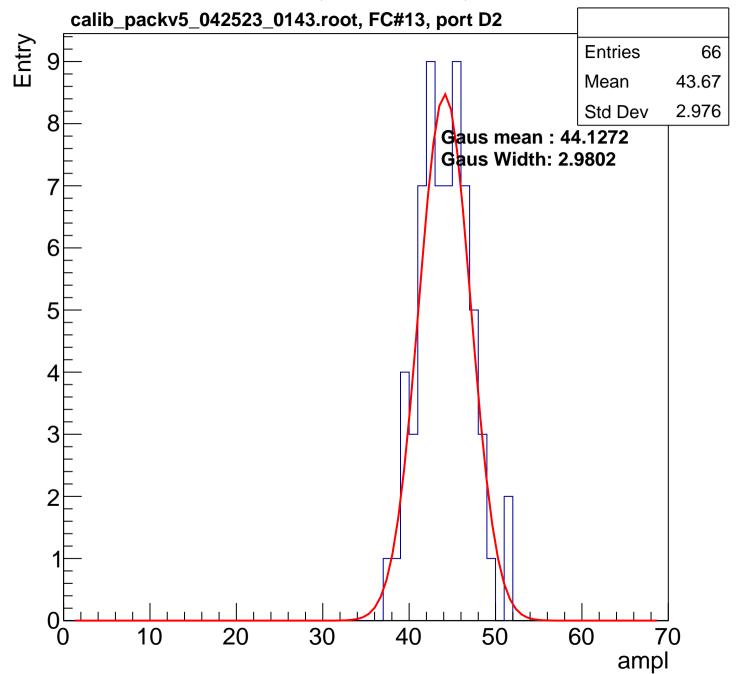


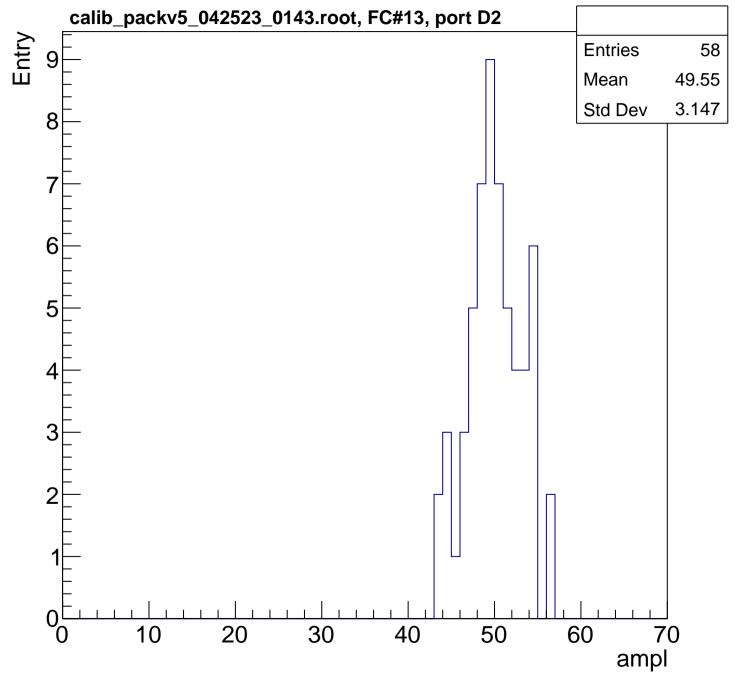


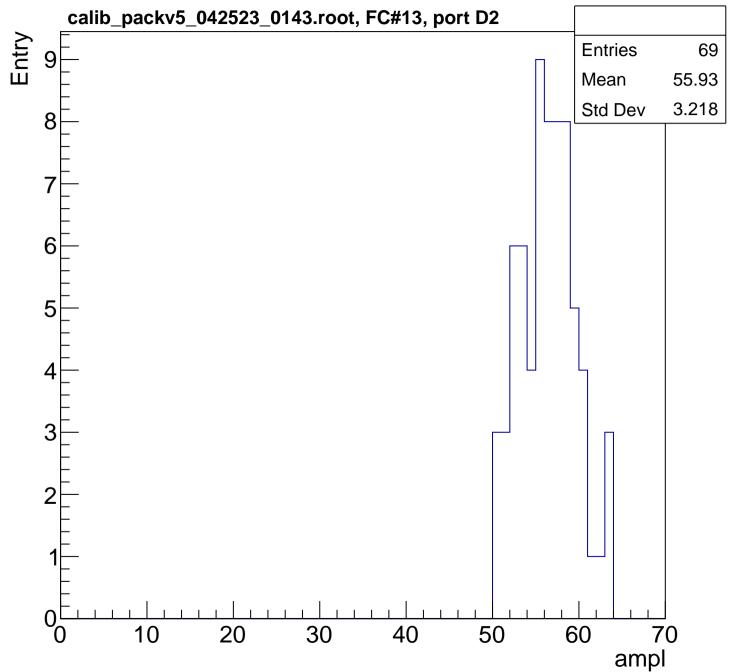
B1L003S, U8-ch80, adc7 calib\_packv5\_042523\_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

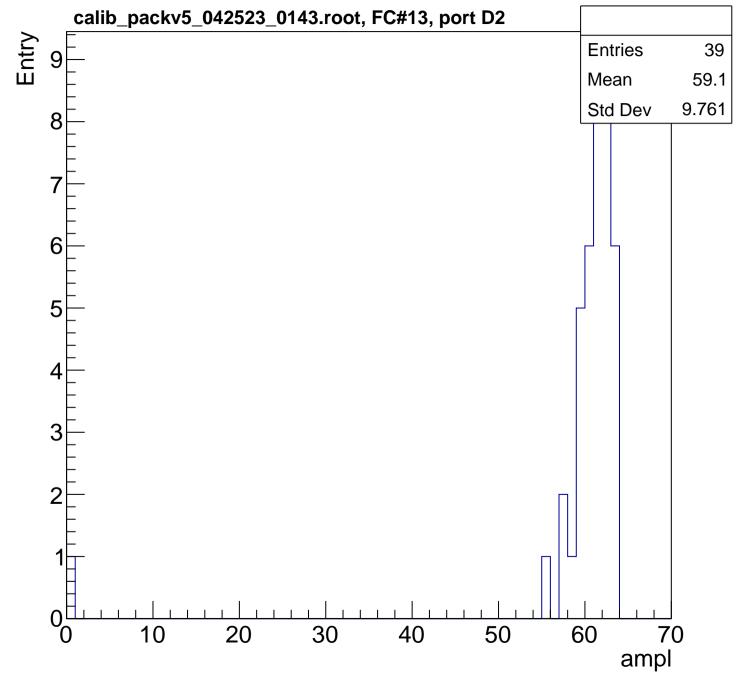


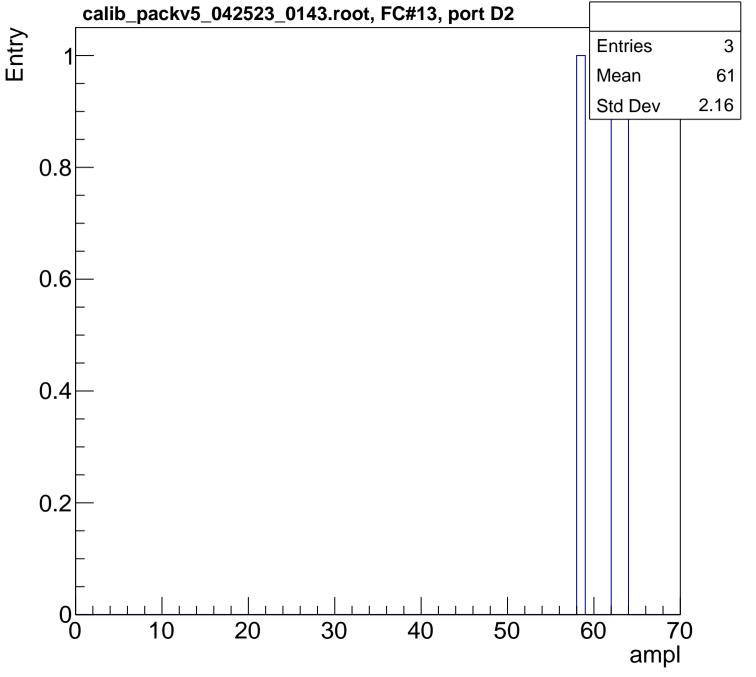




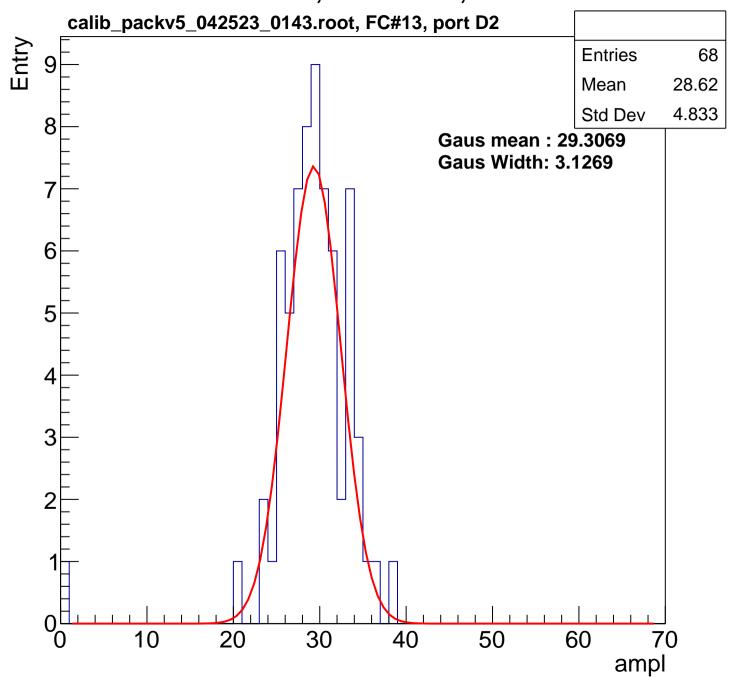


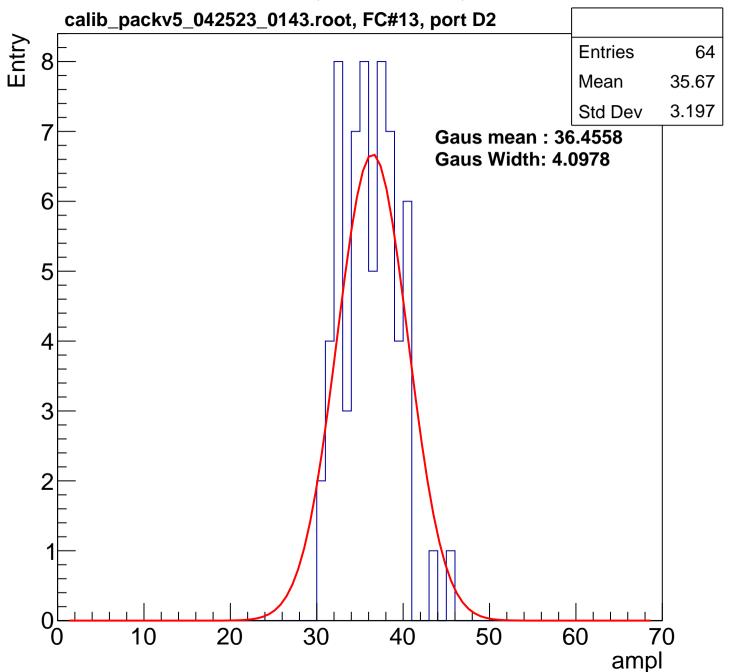


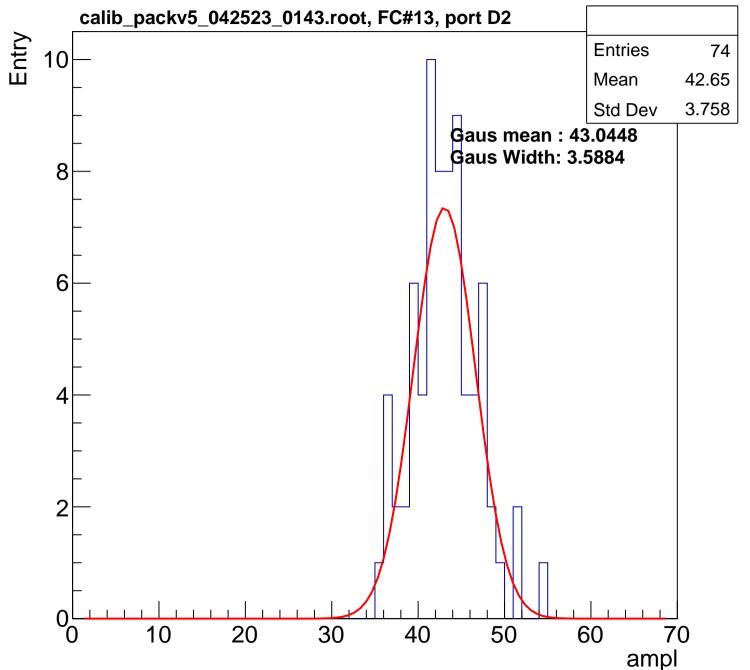


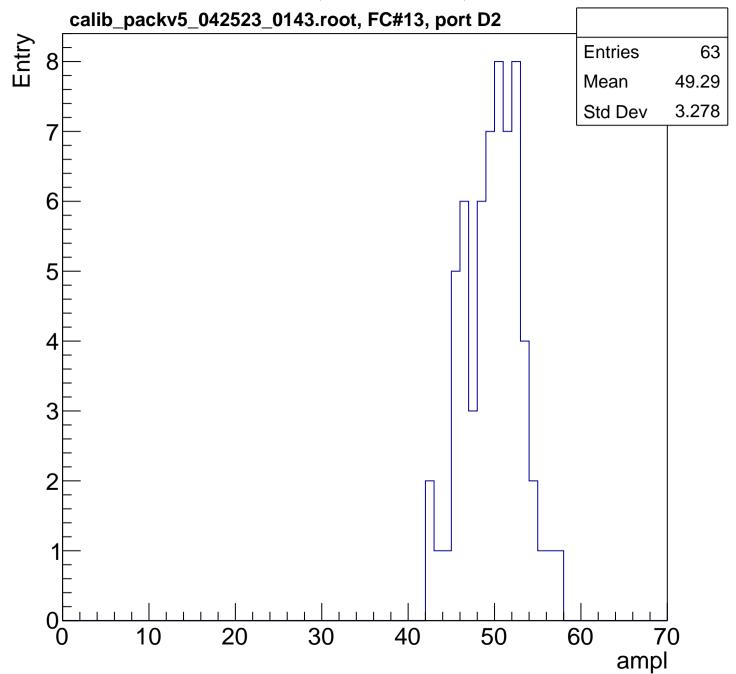


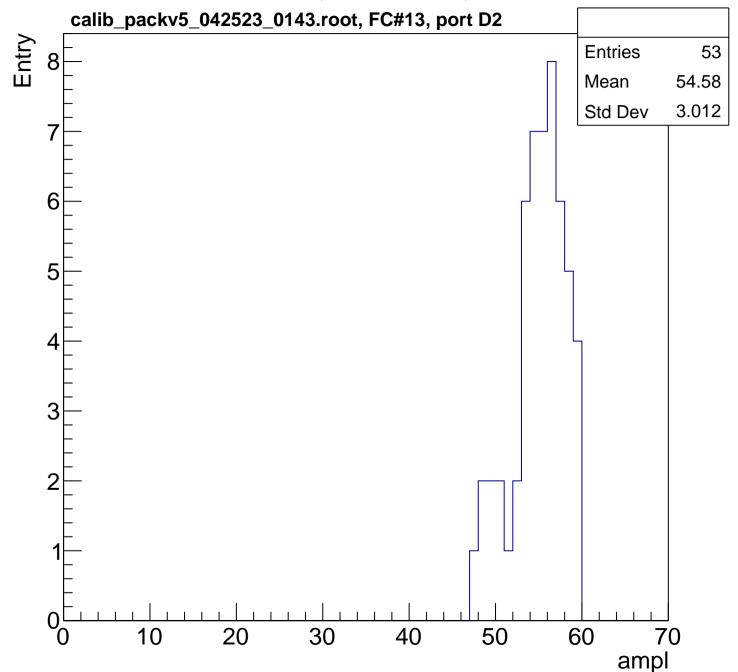


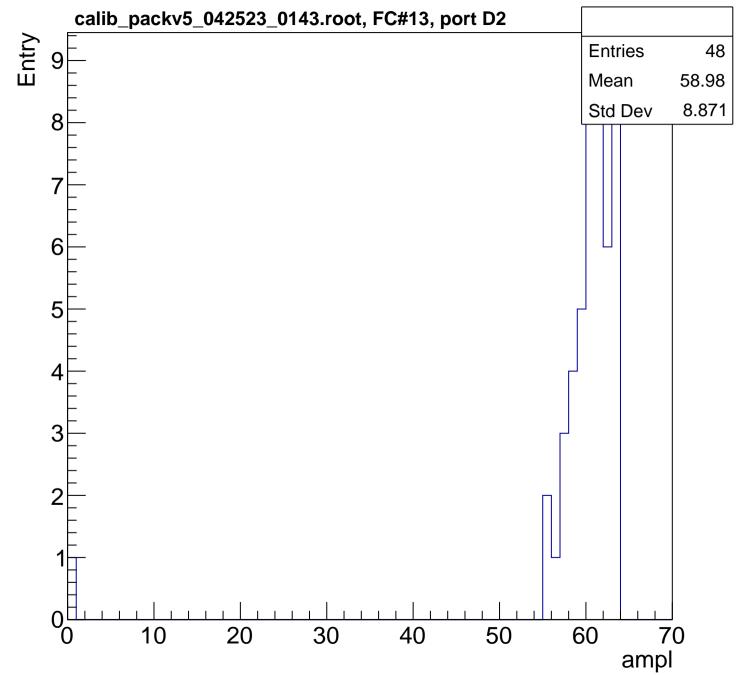


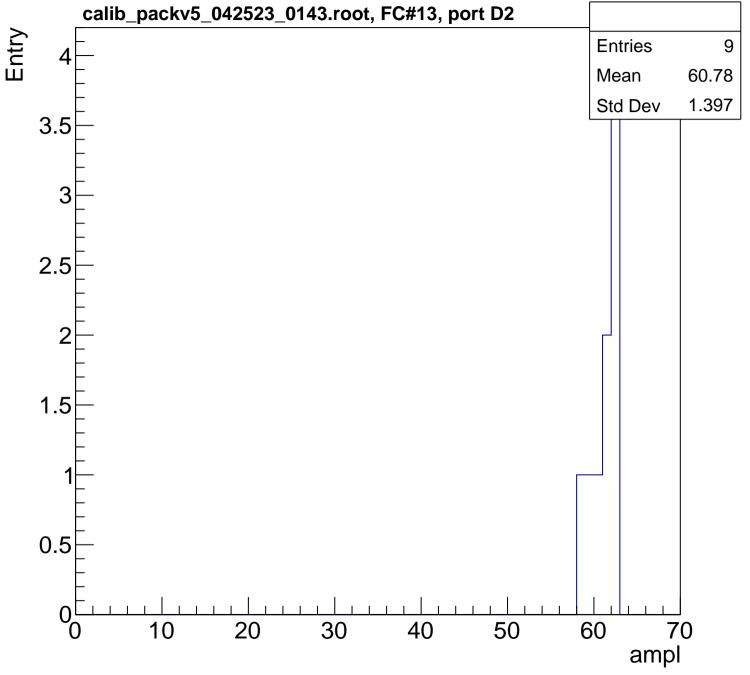


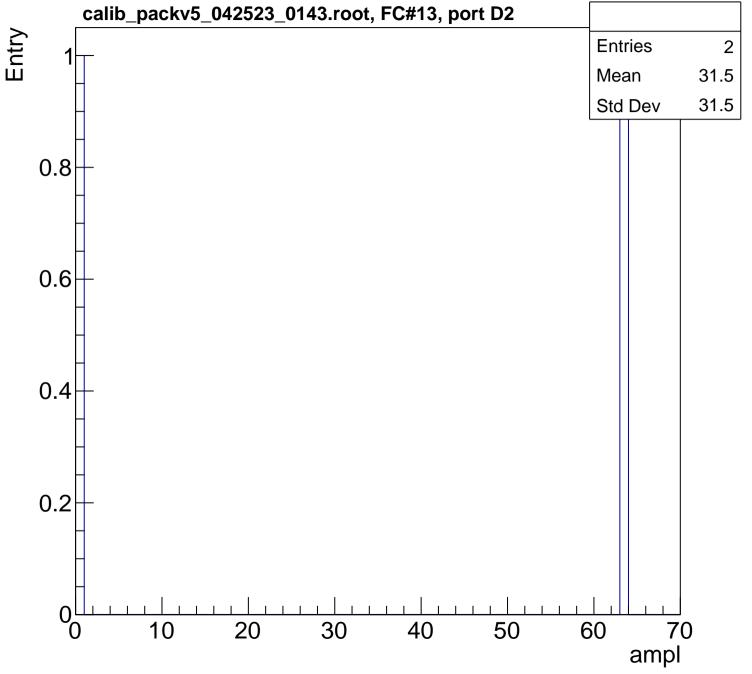


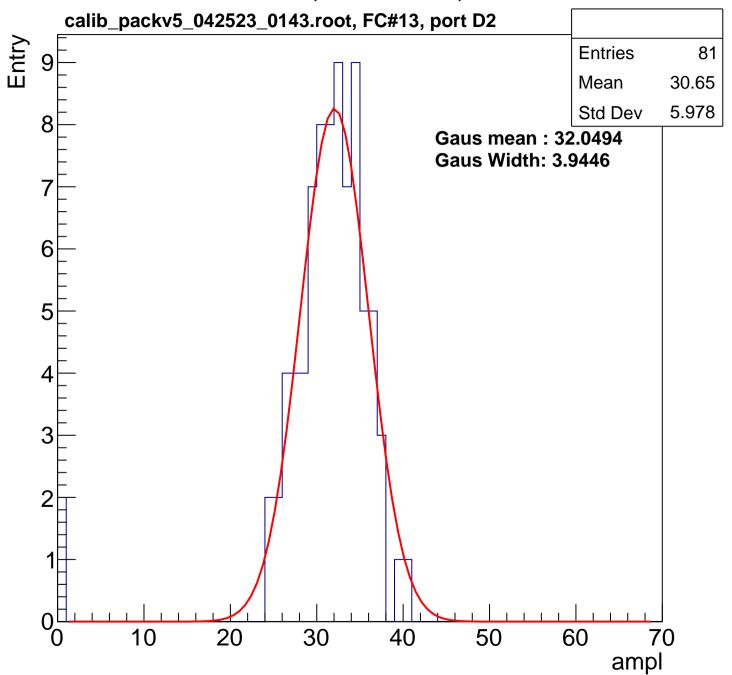


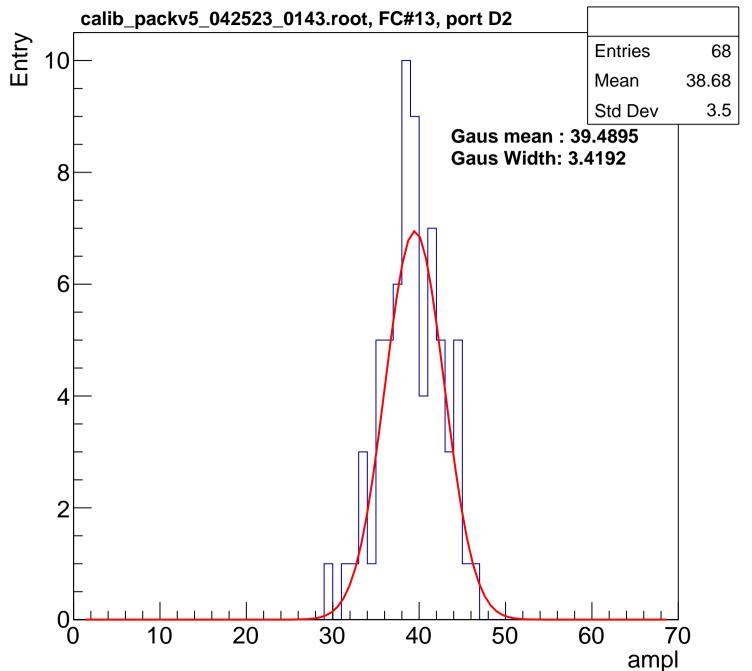


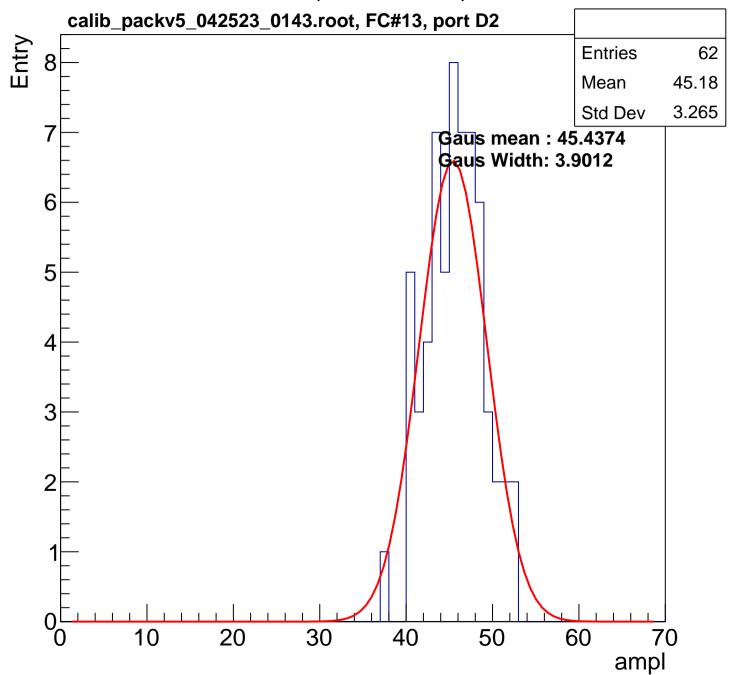


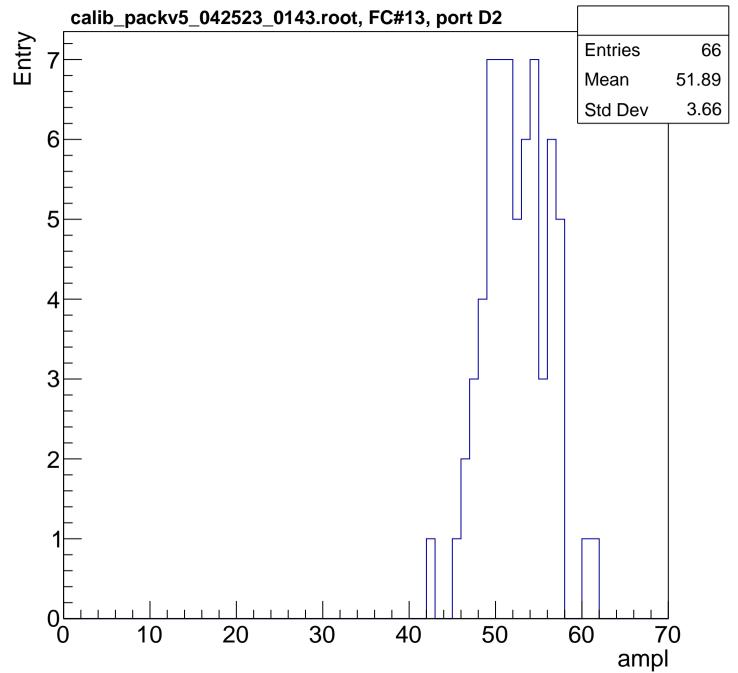


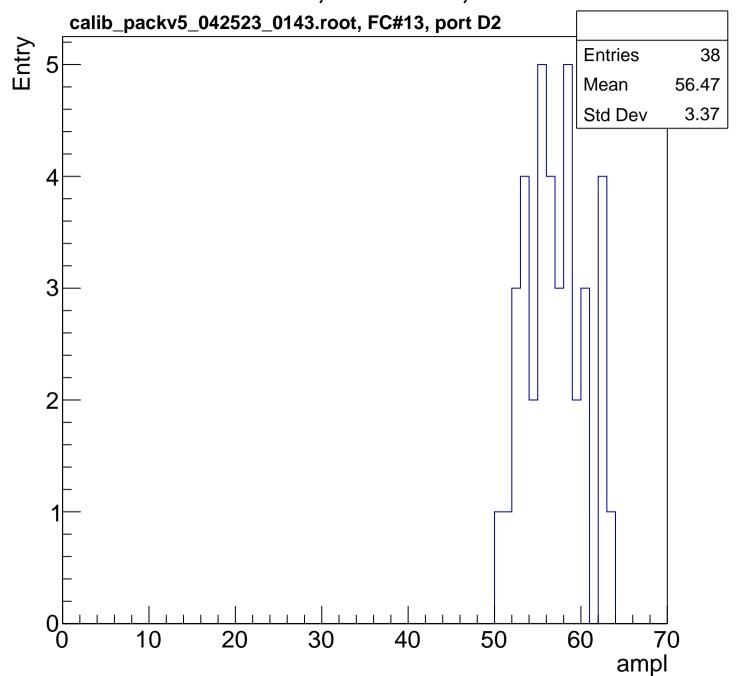


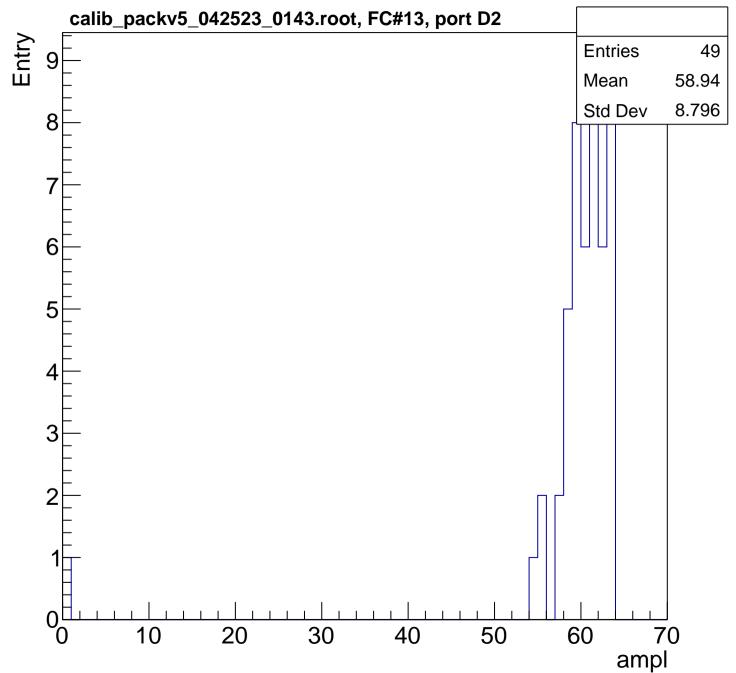






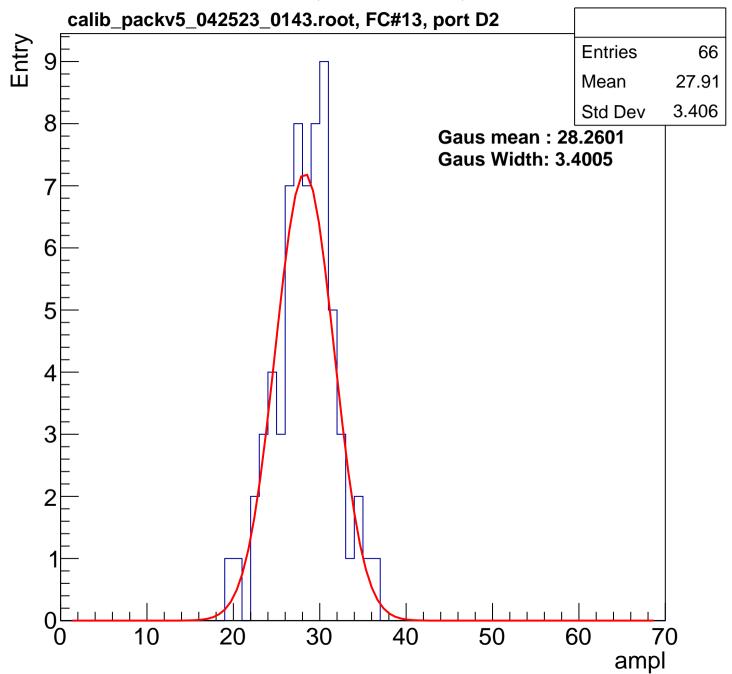


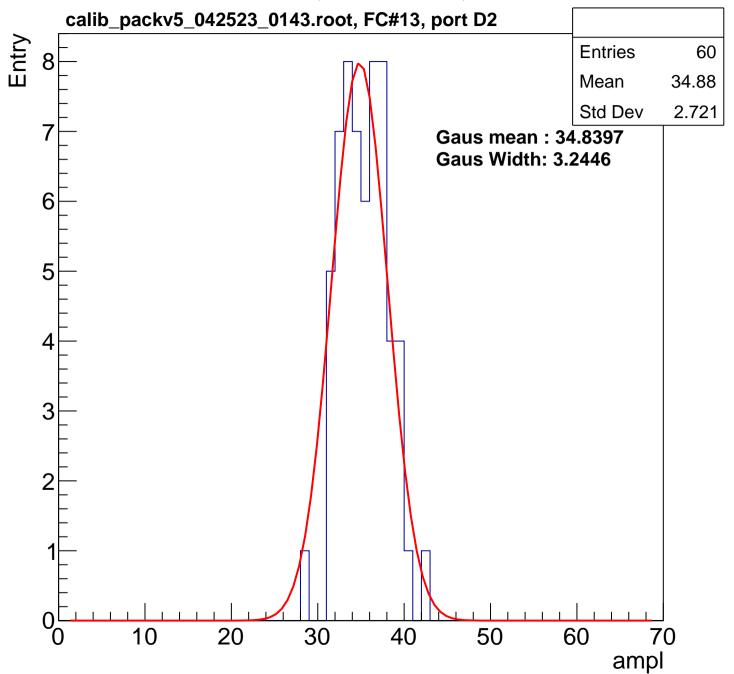


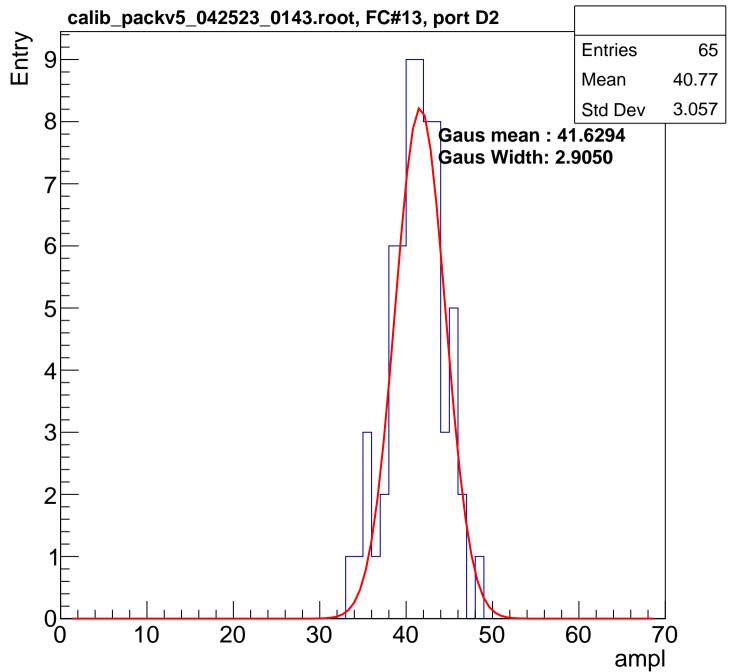


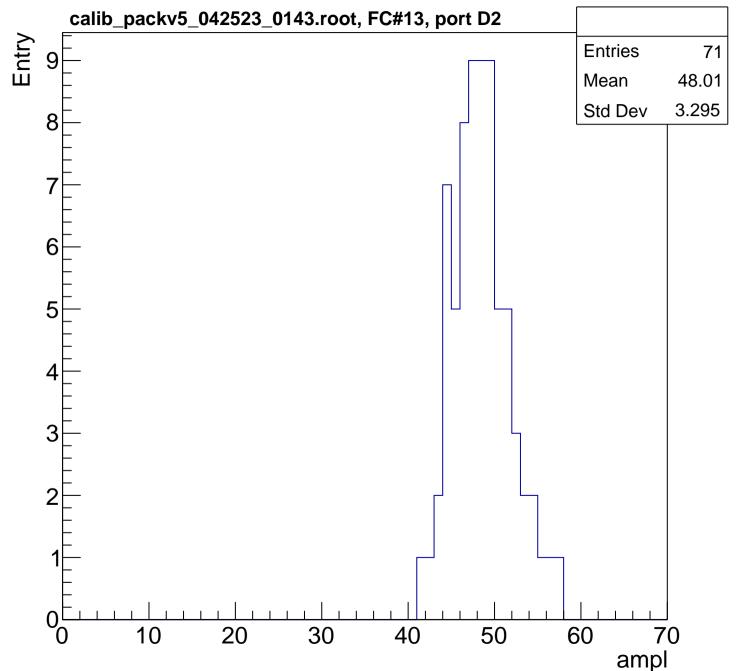


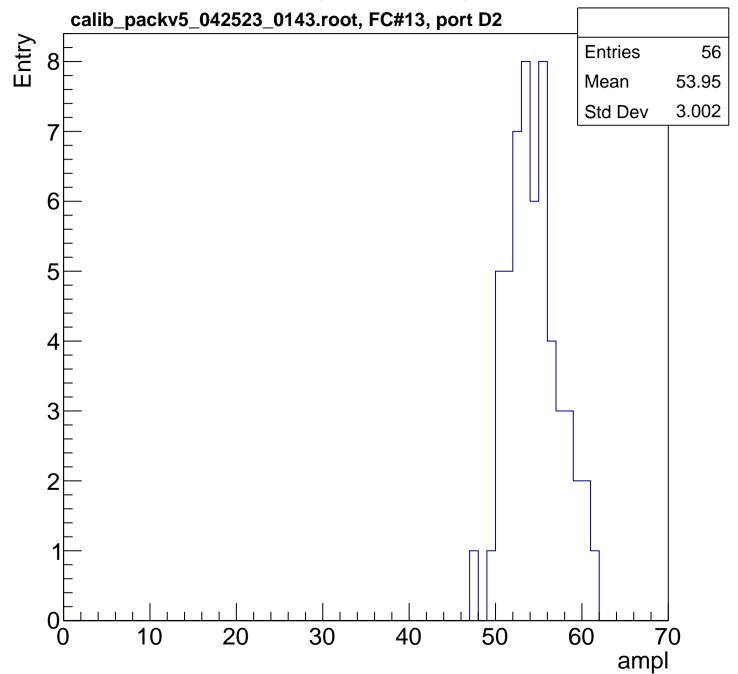


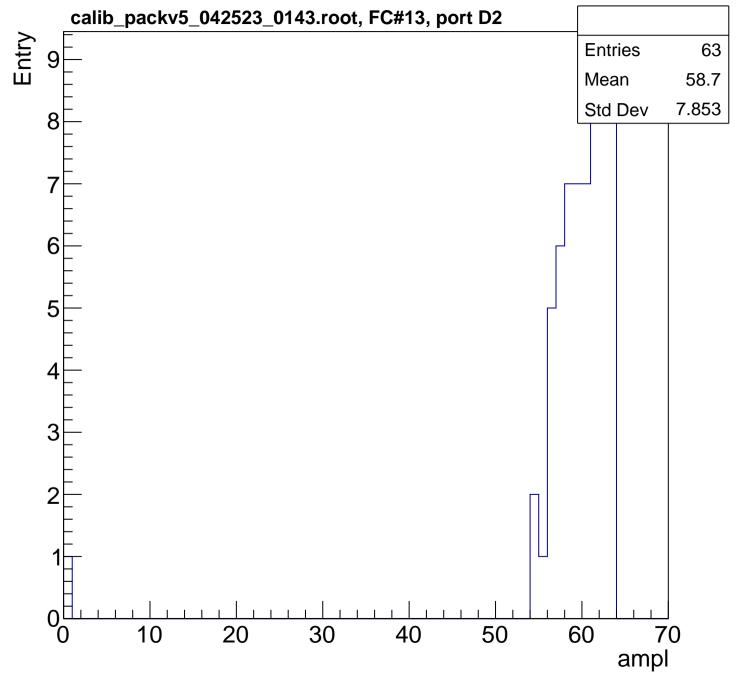


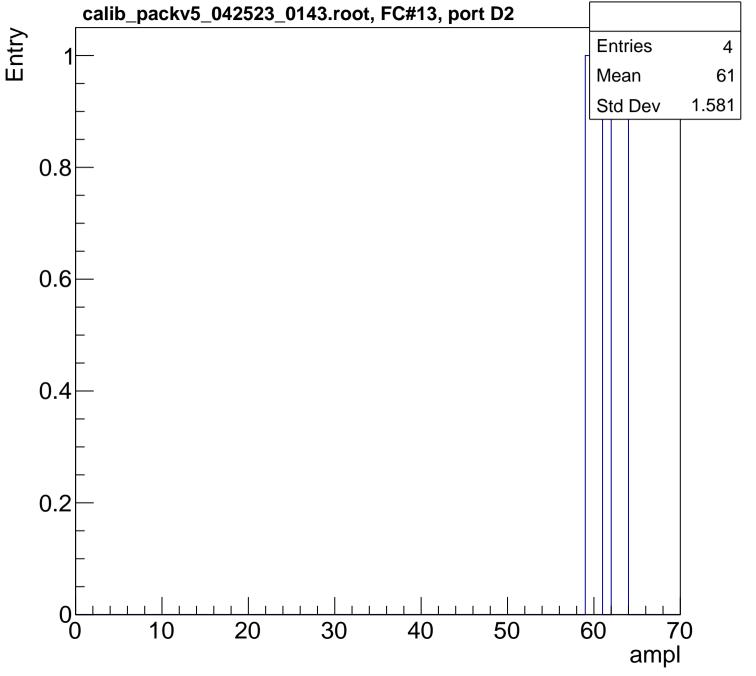




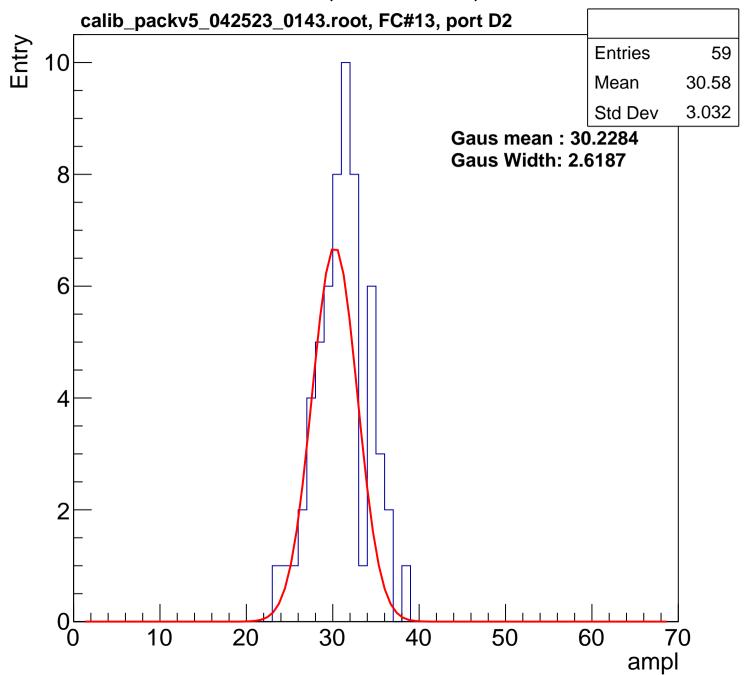


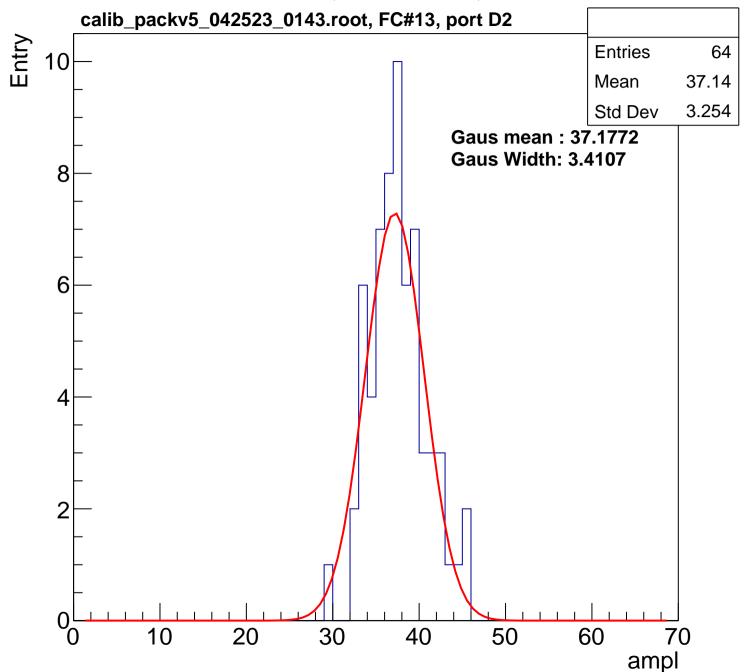


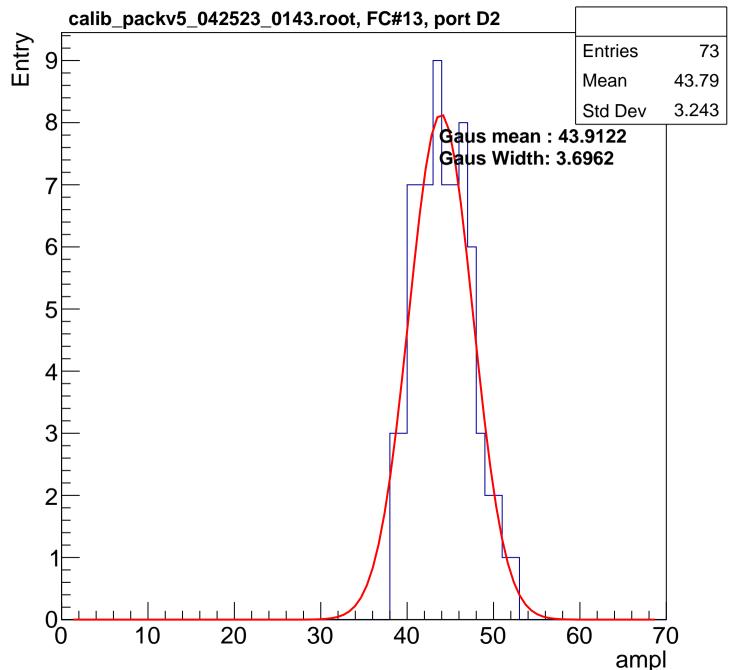


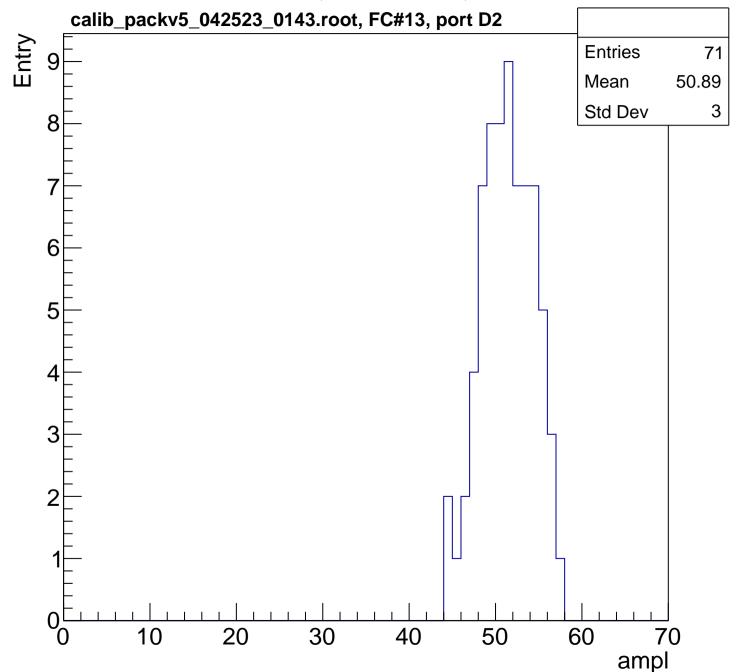


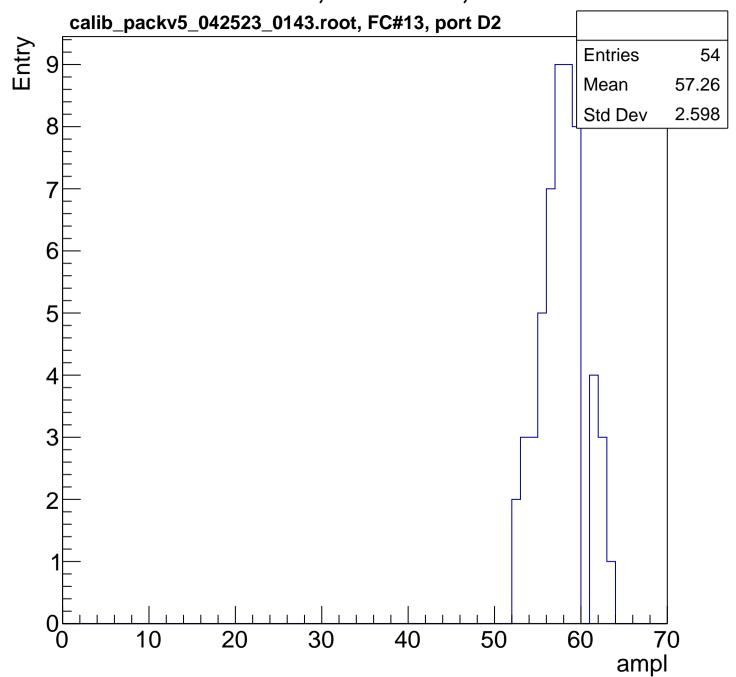


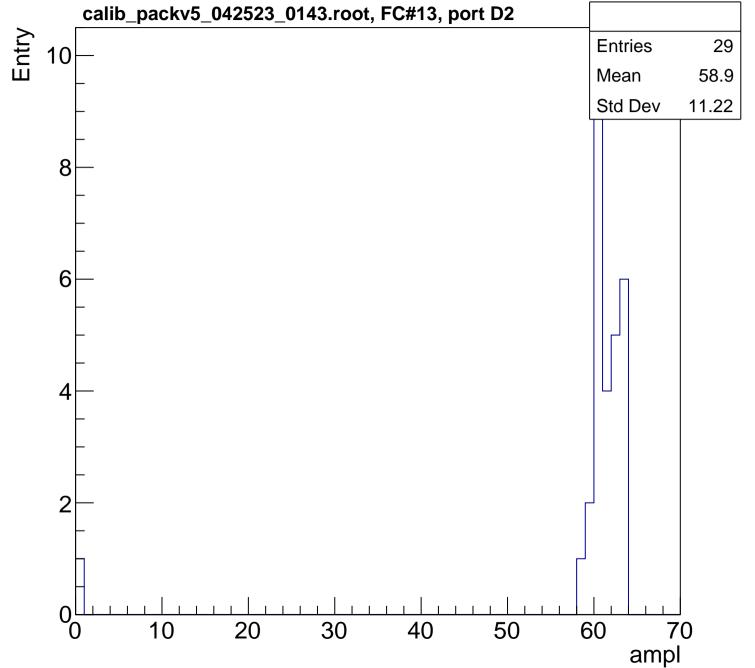


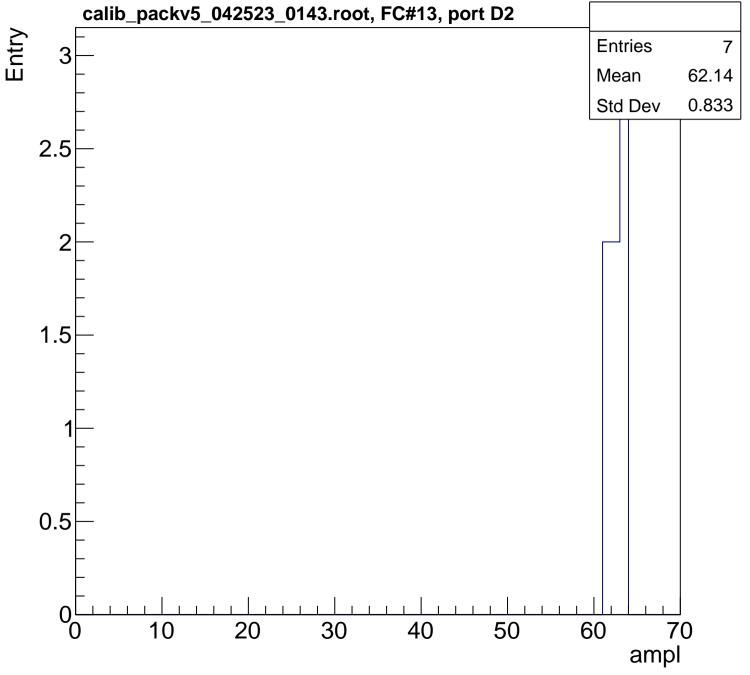


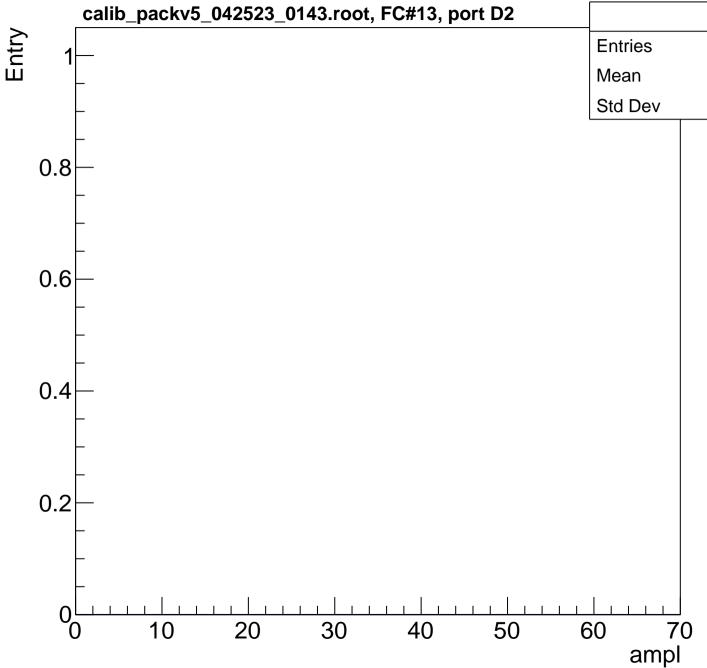


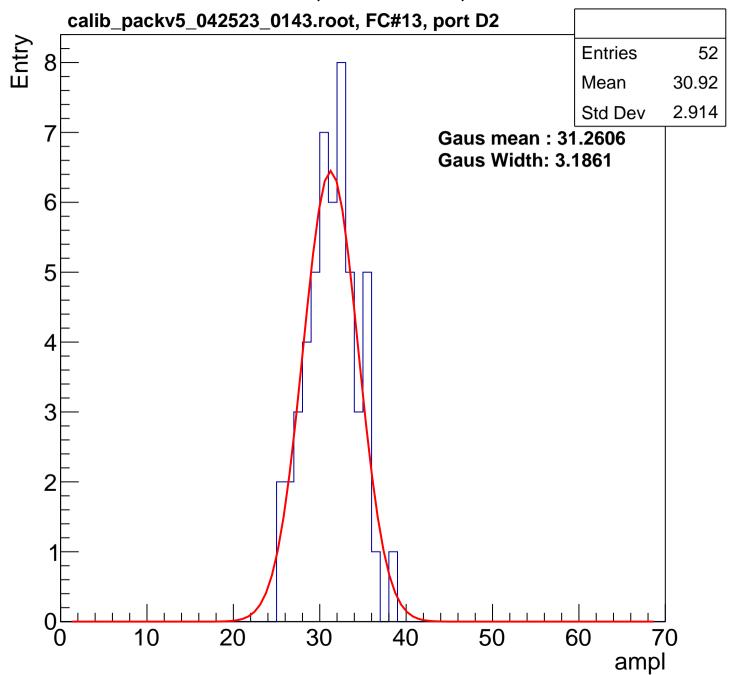


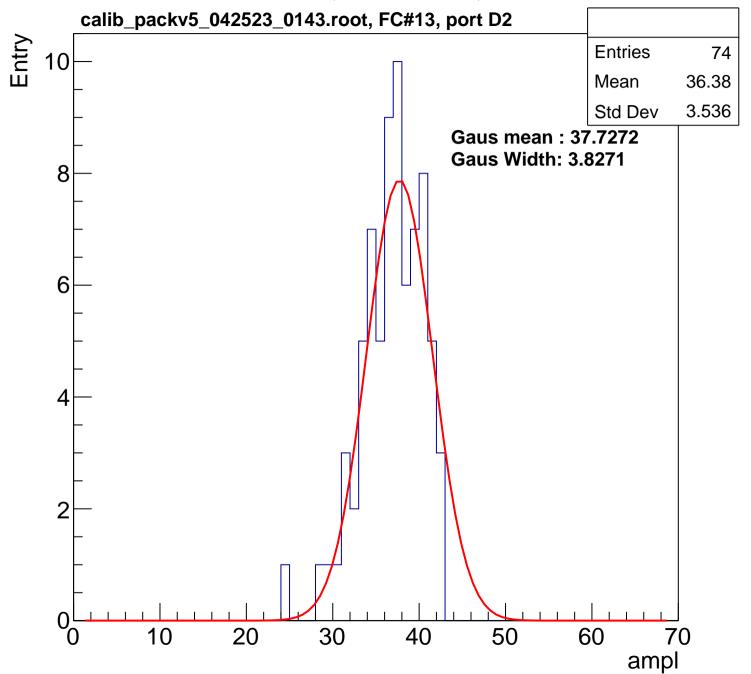


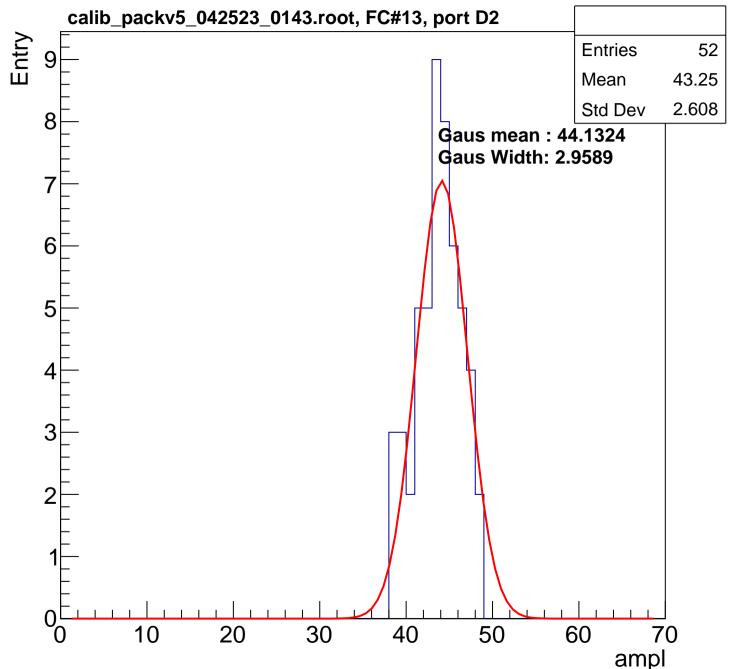


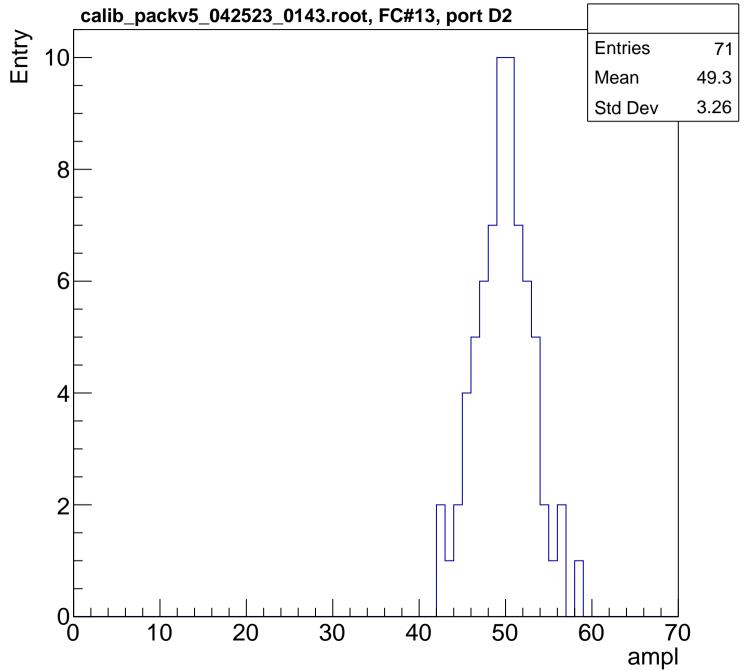


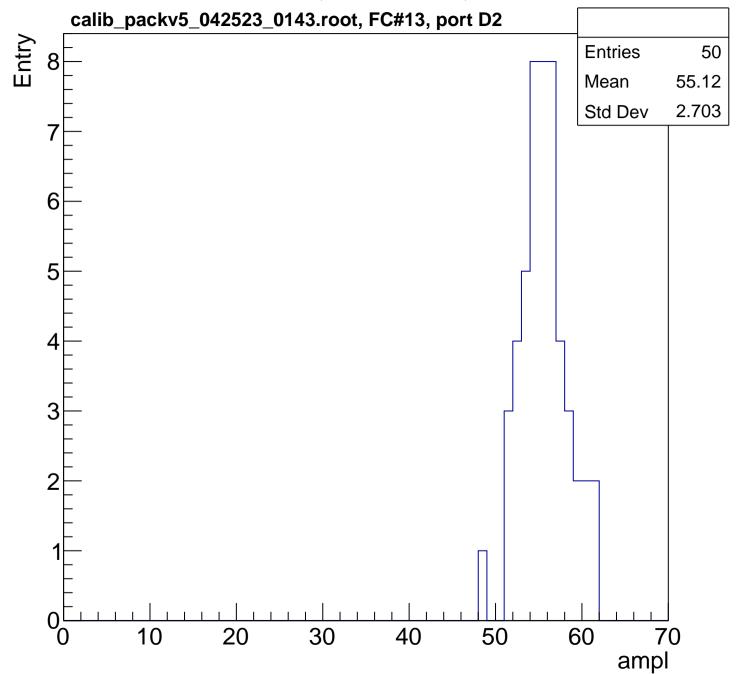


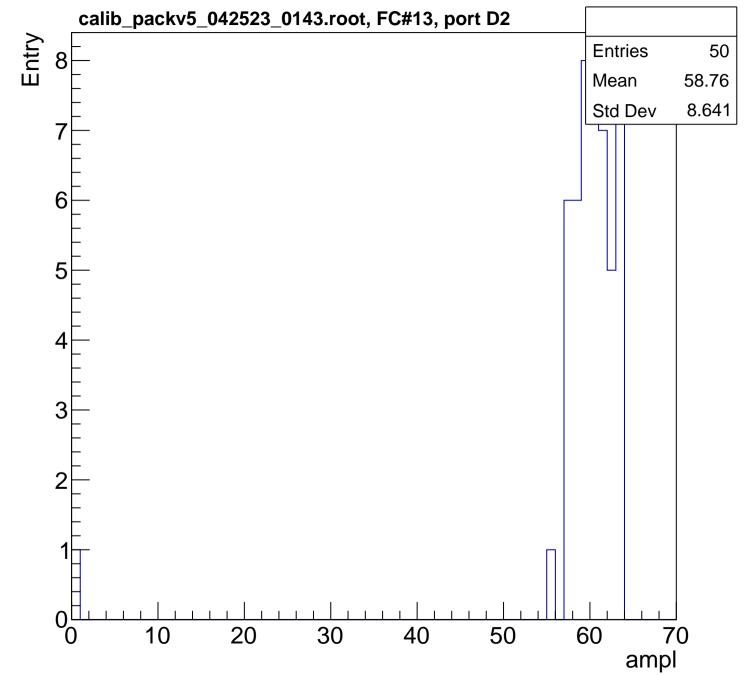


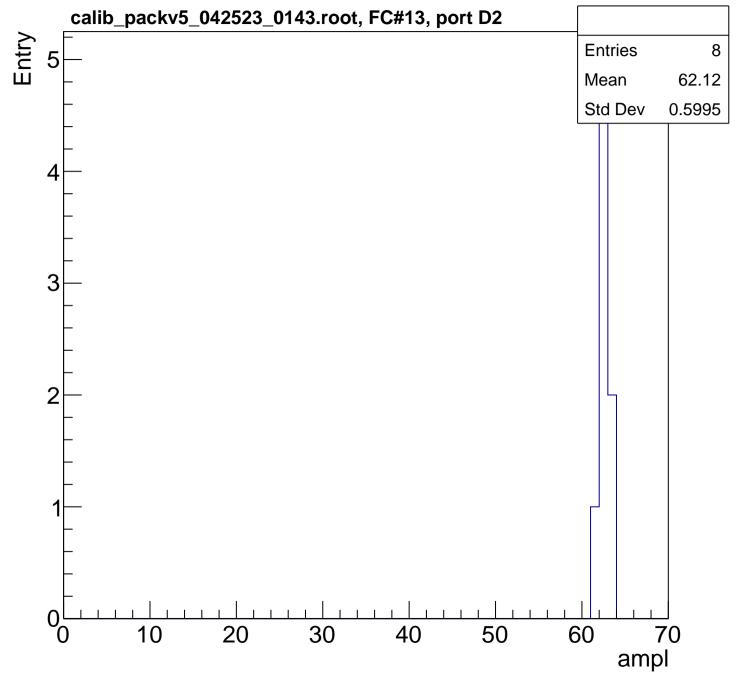


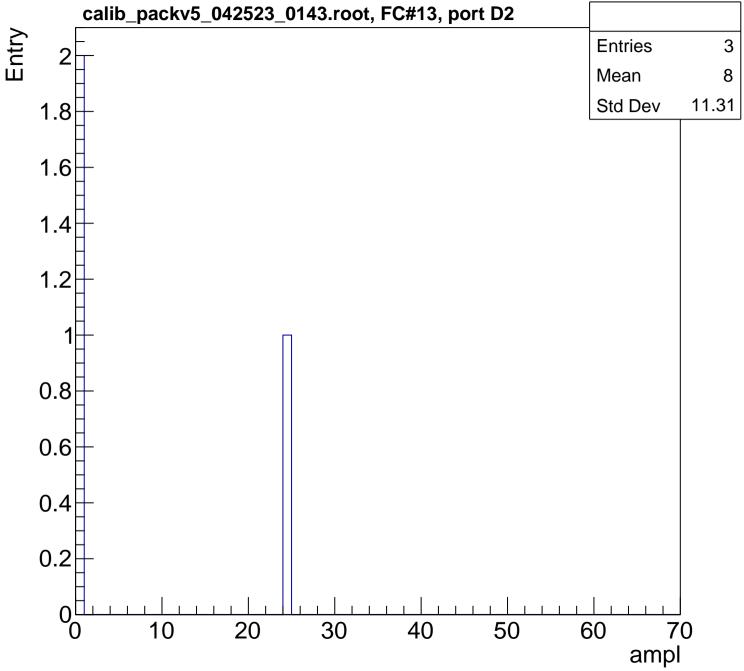


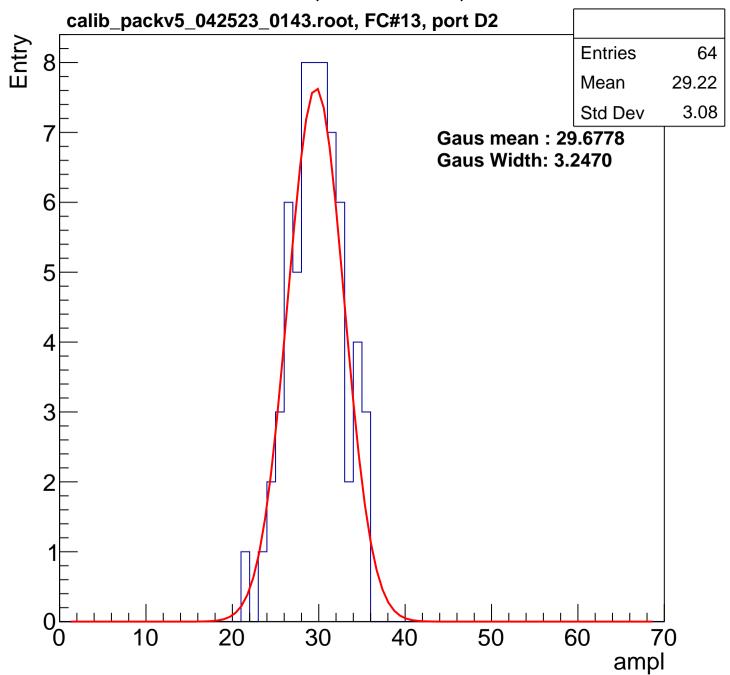


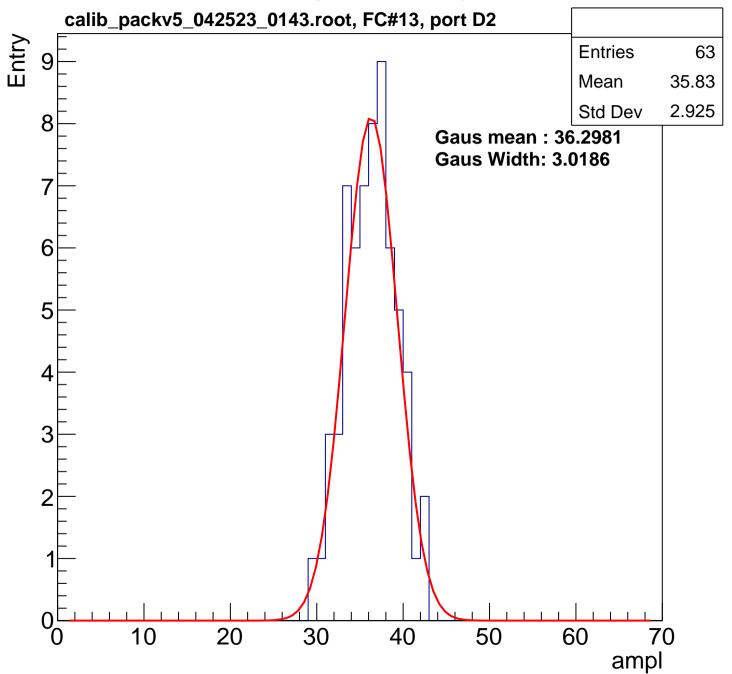


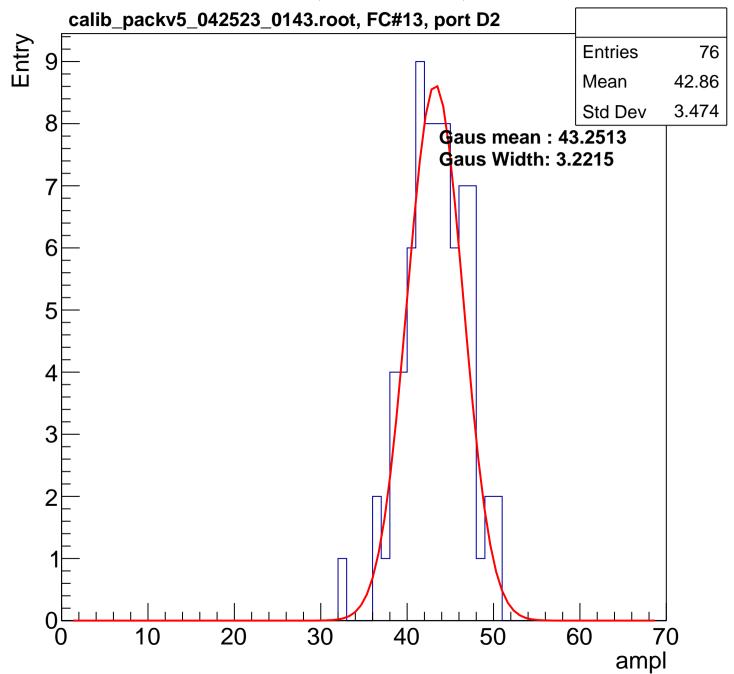


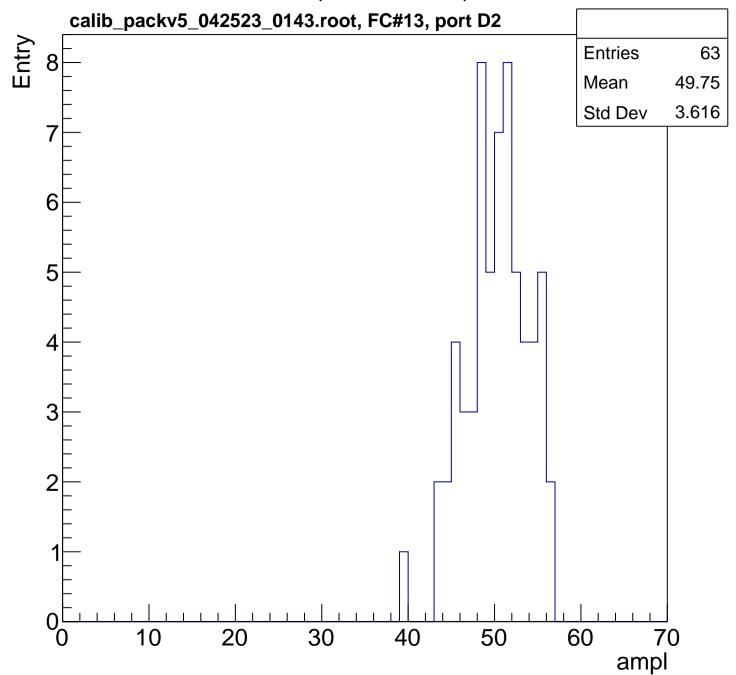


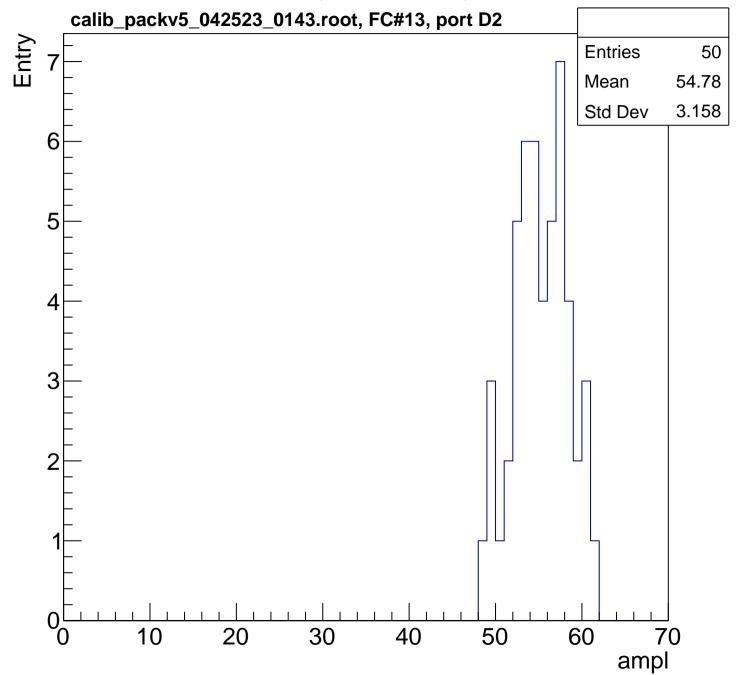


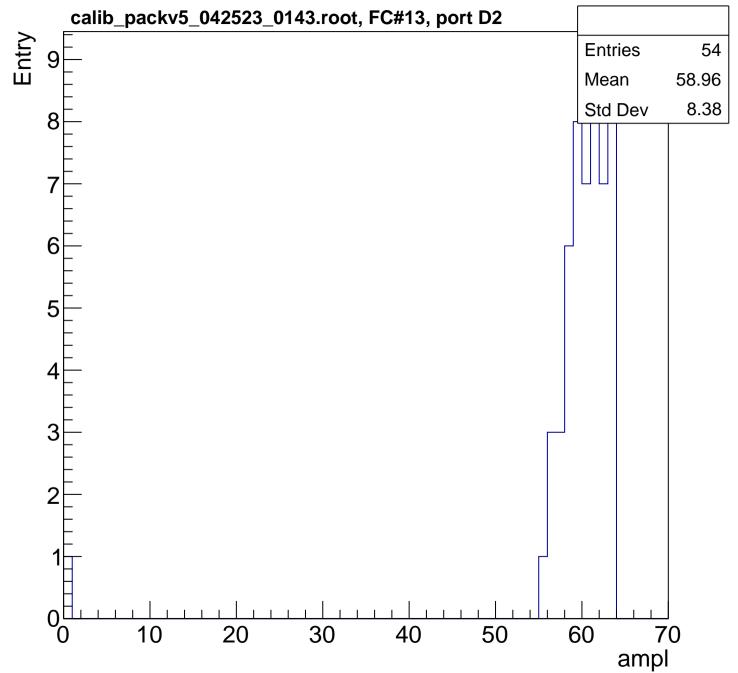


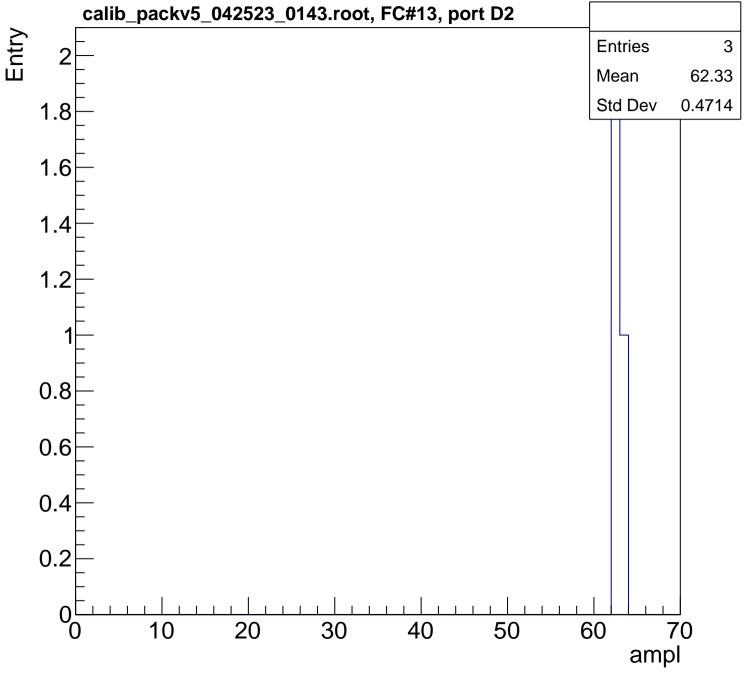




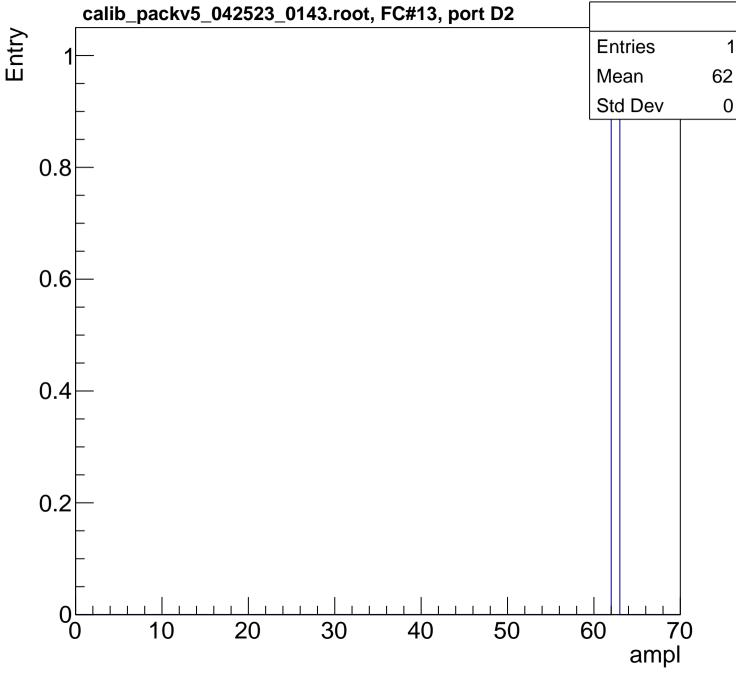


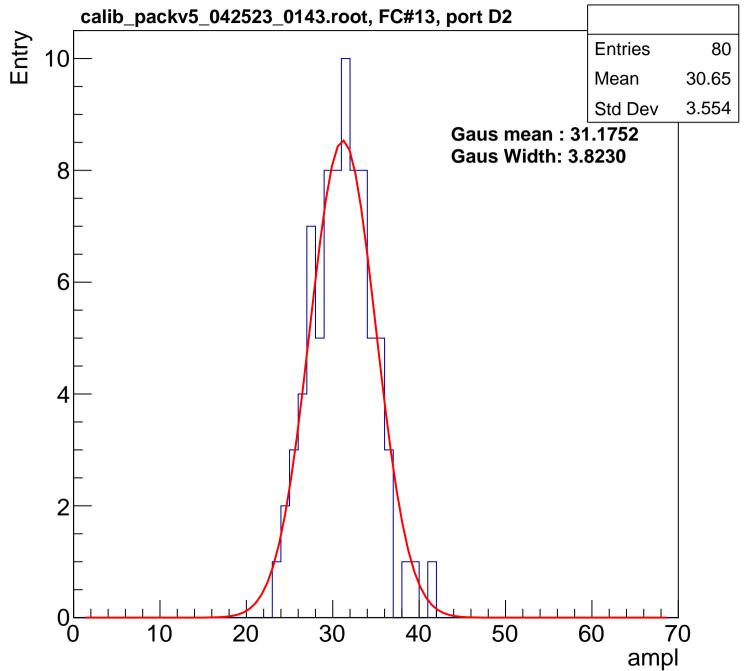


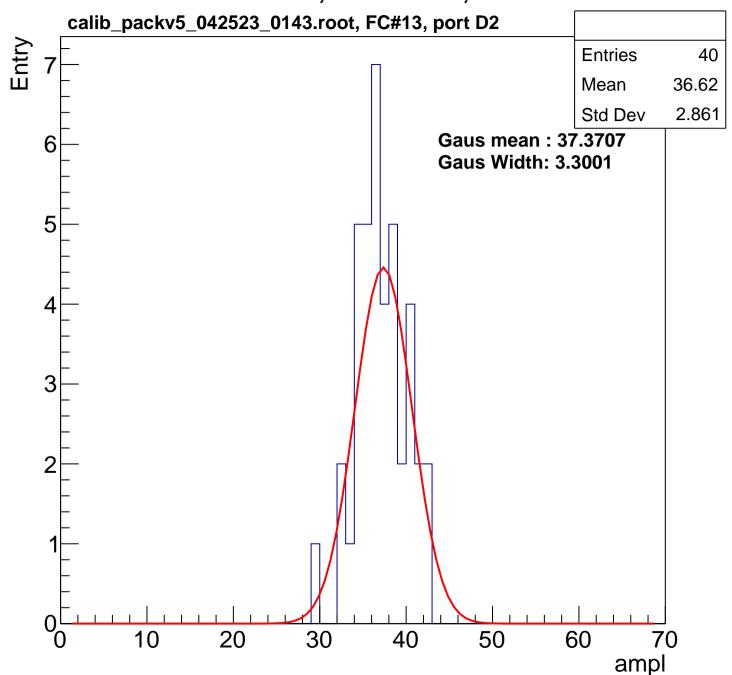


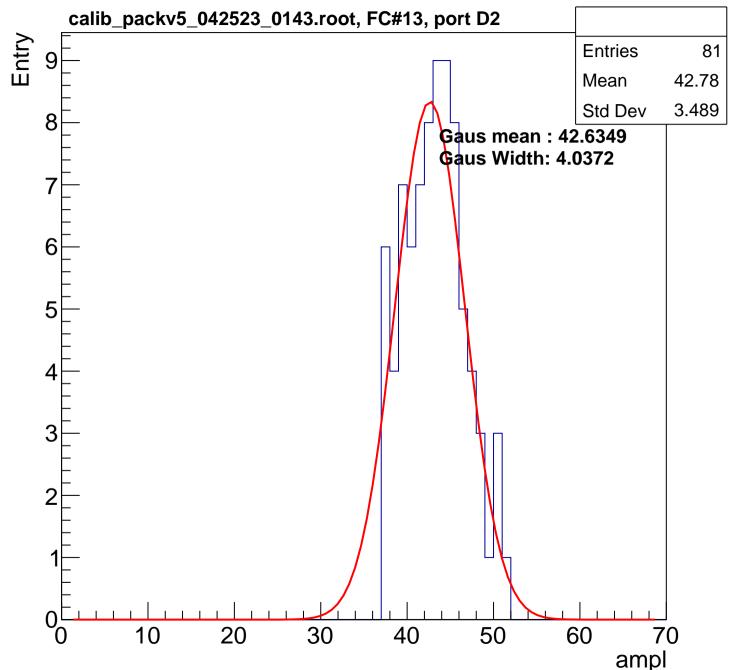


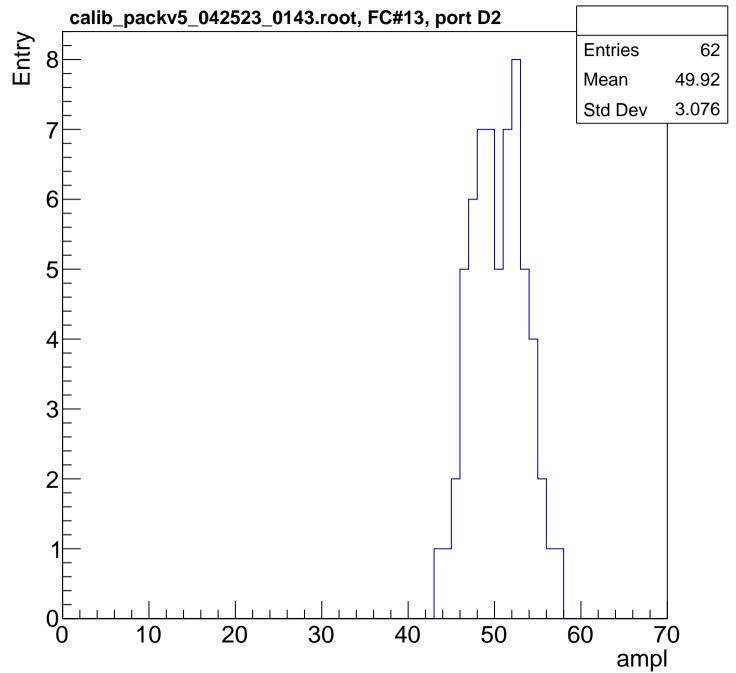
0

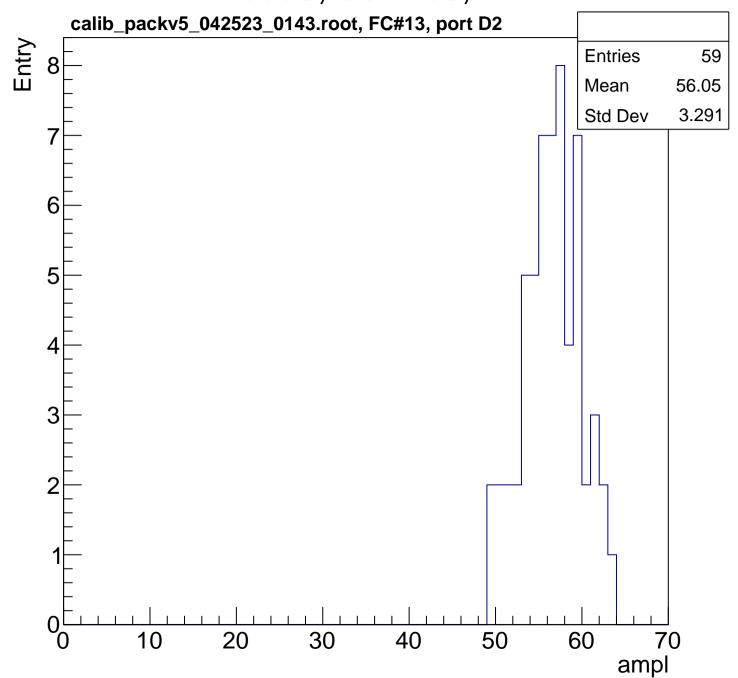


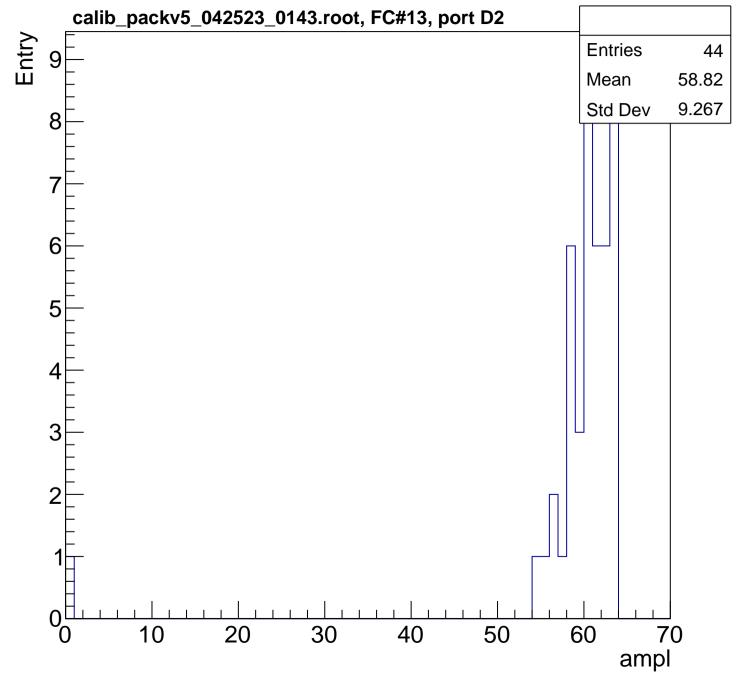


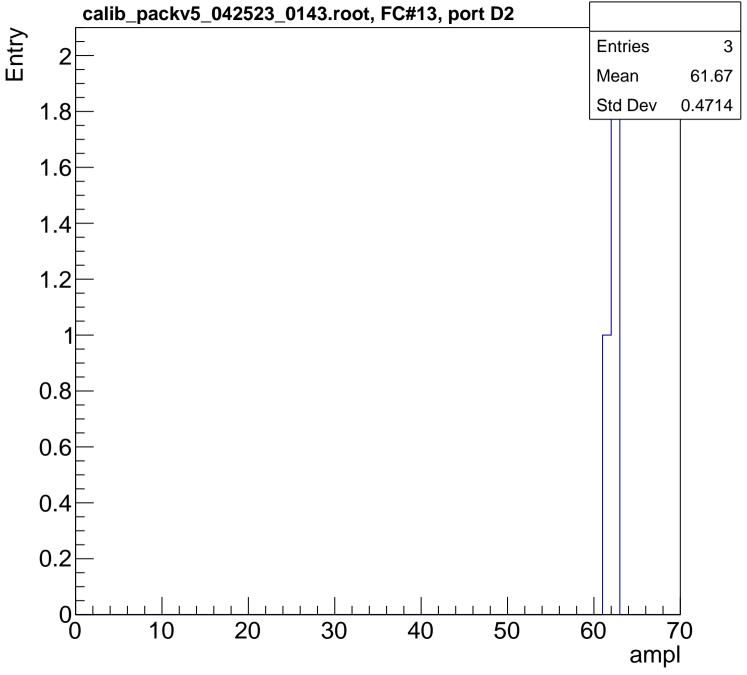




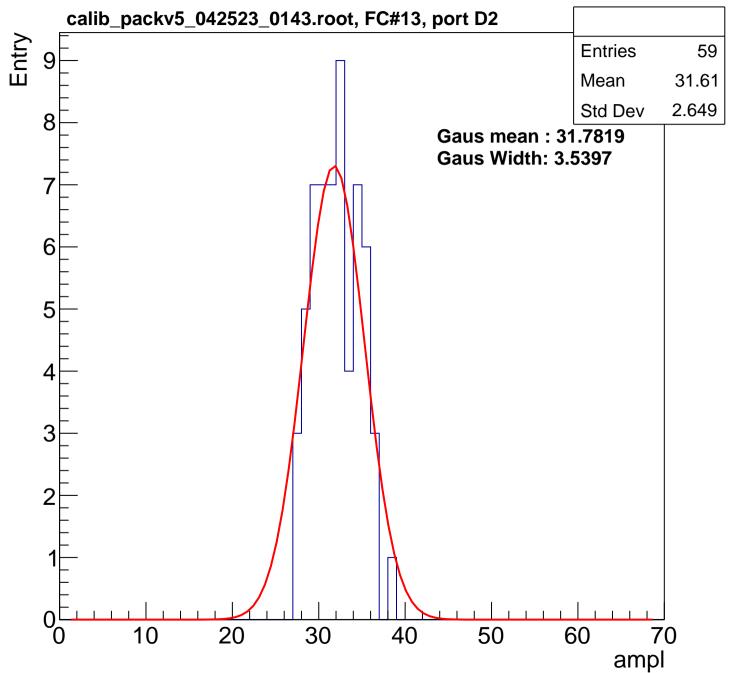


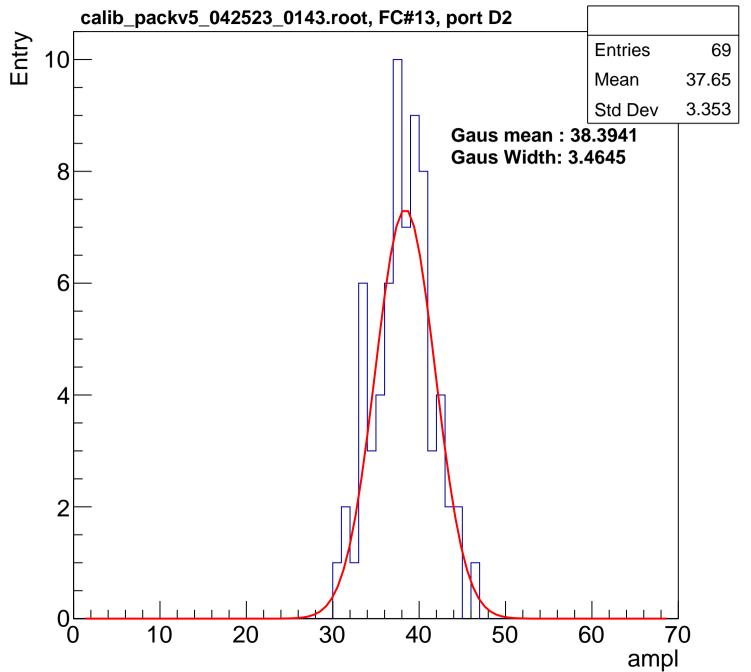


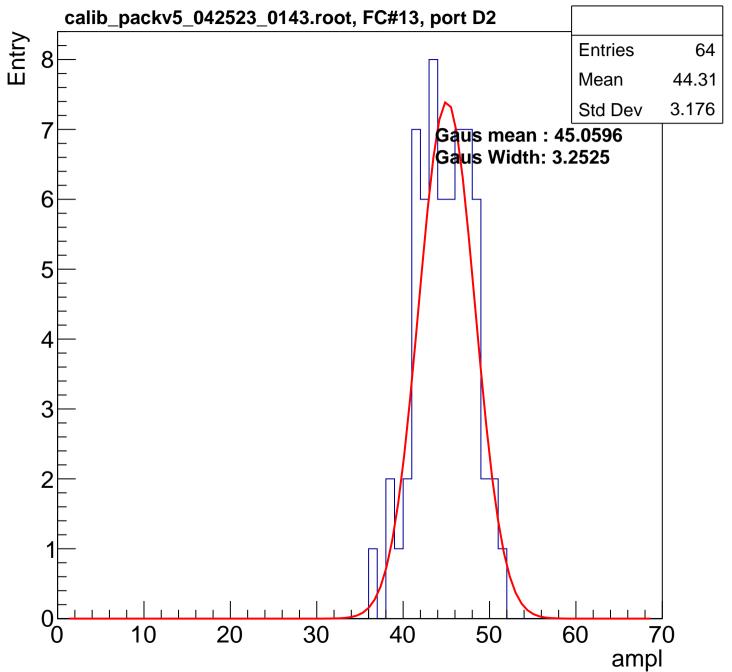


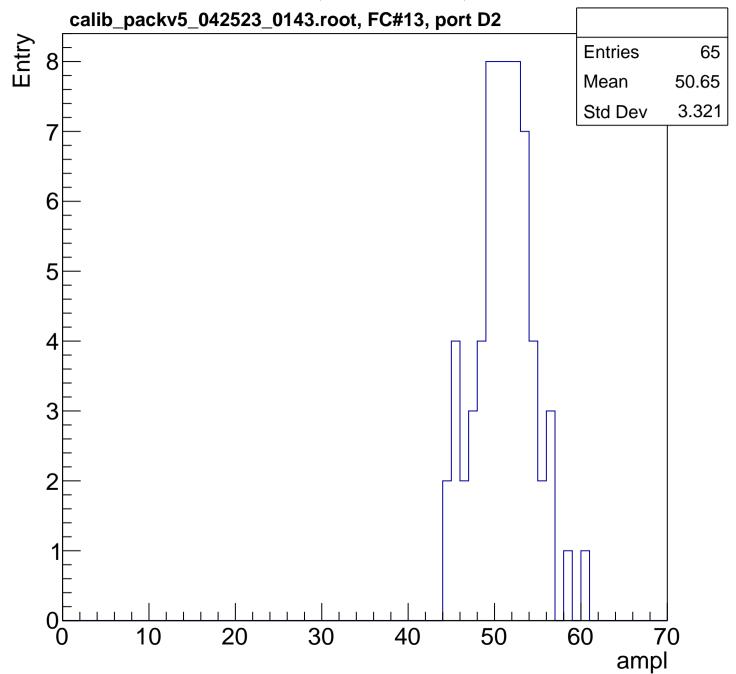


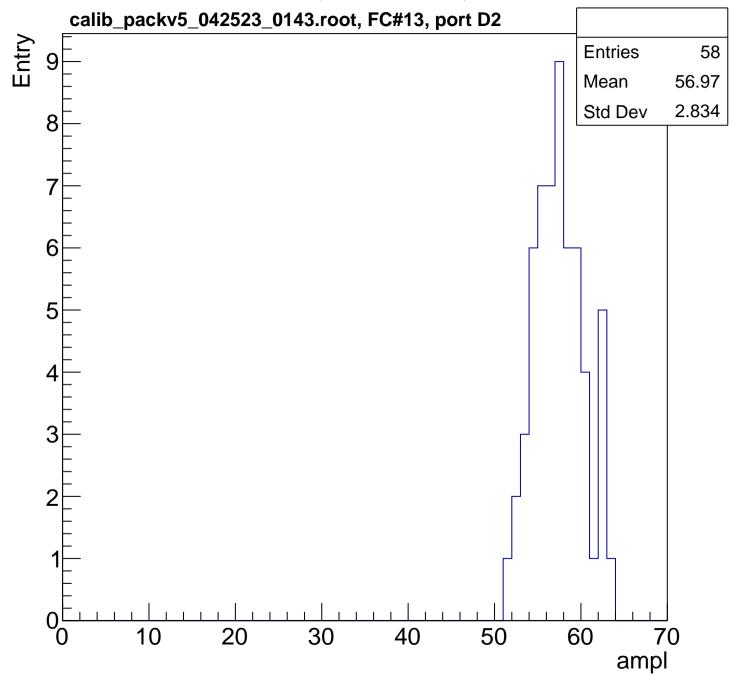
B1L003S, U8-ch88, adc7 calib\_packv5\_042523\_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

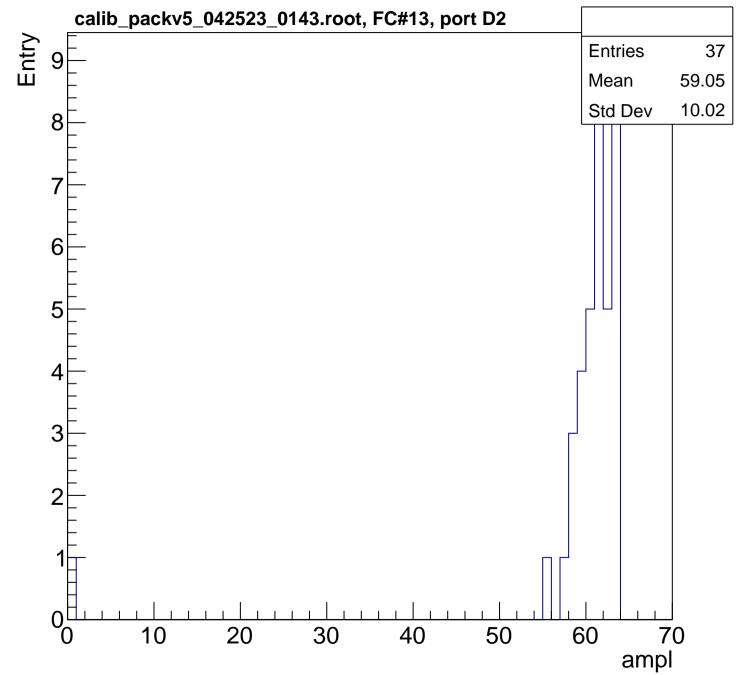


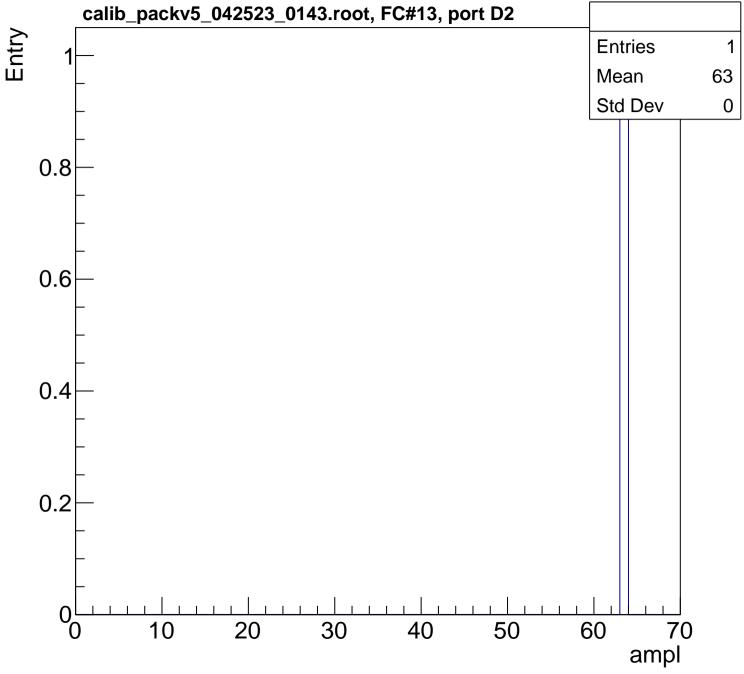


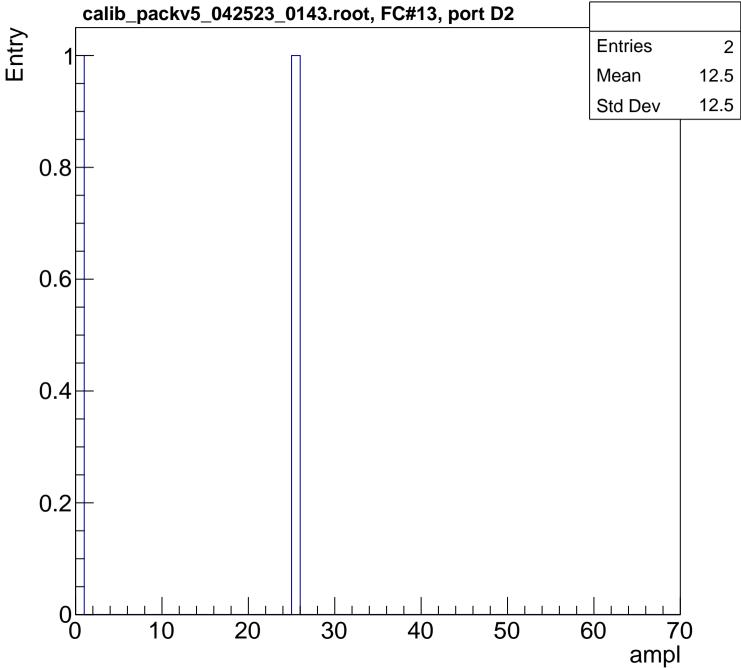


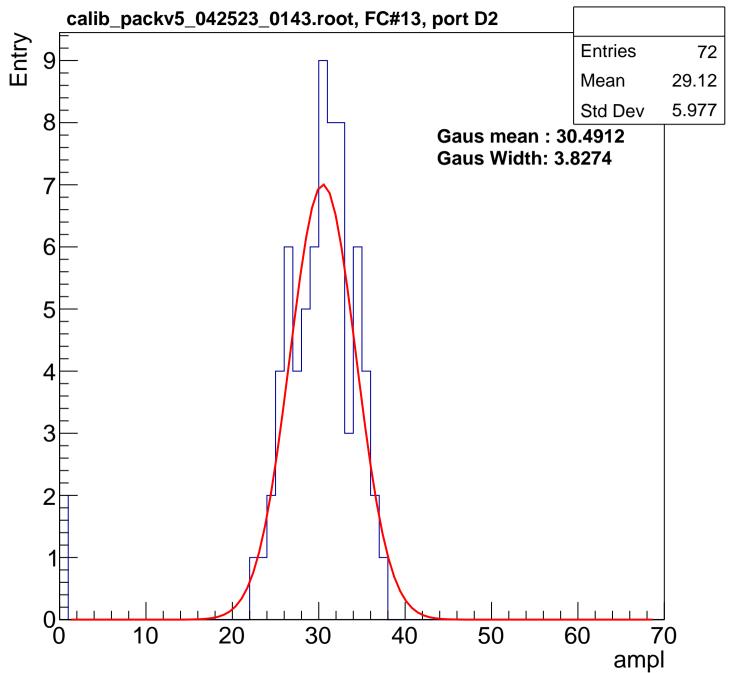


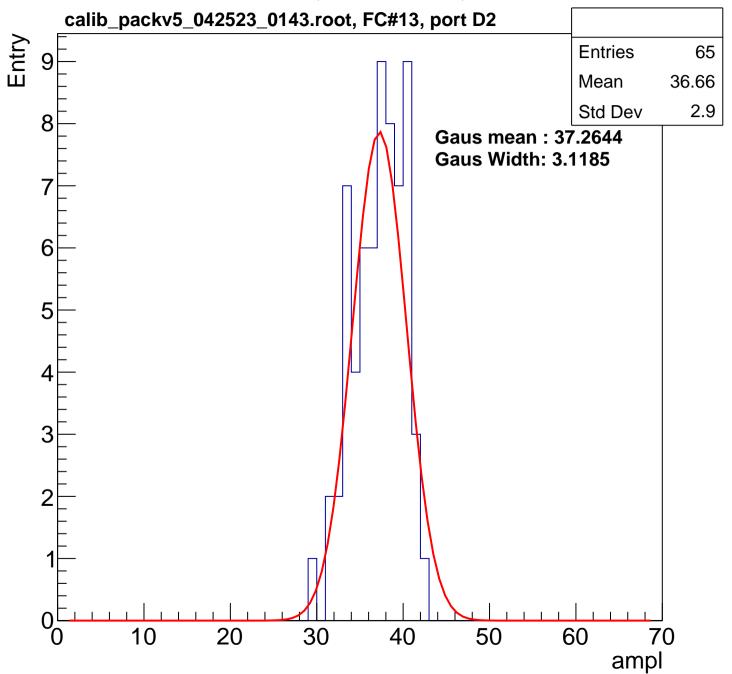


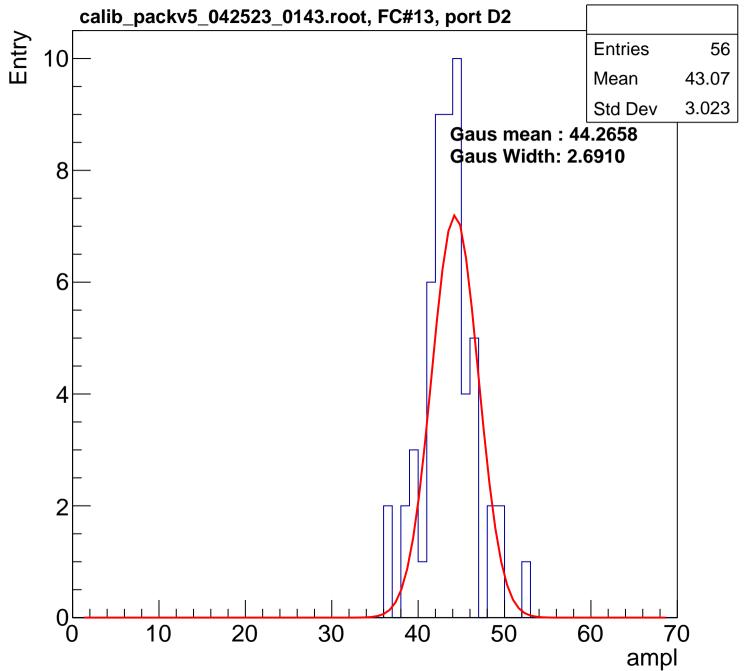


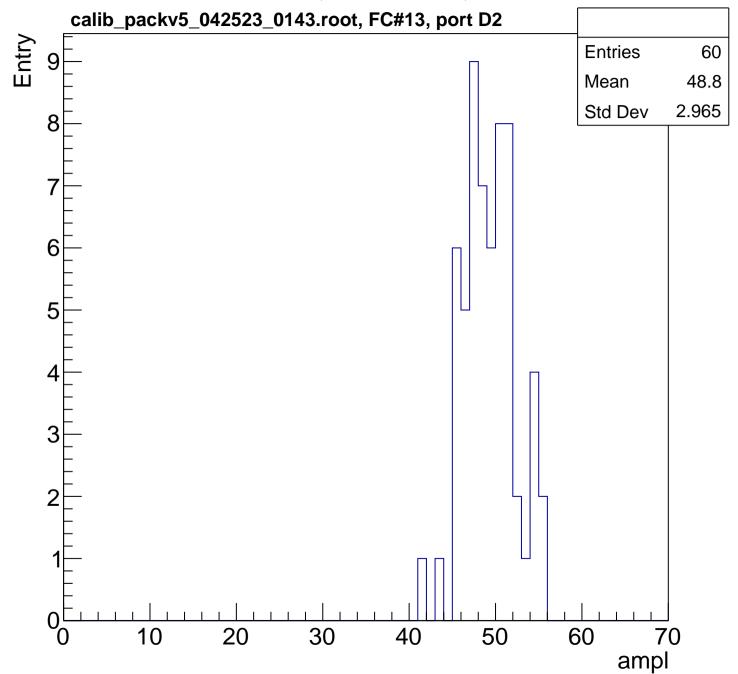


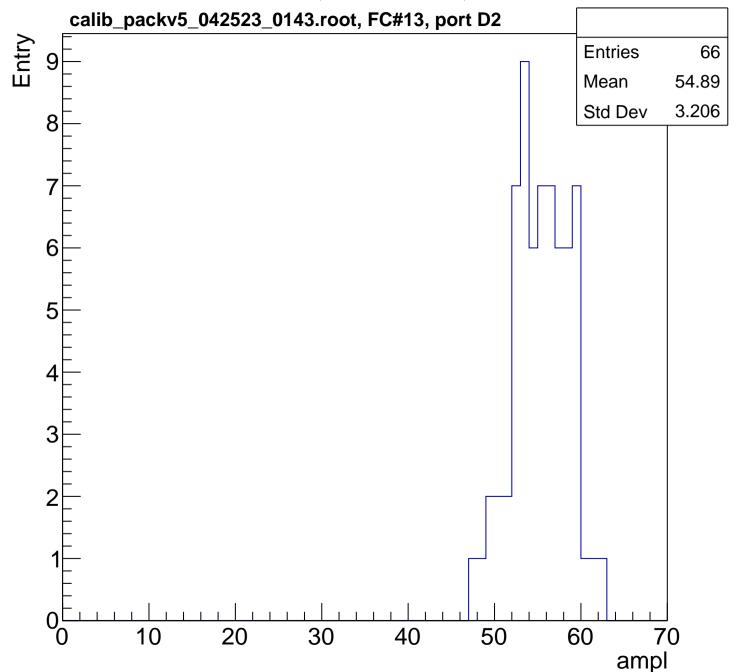


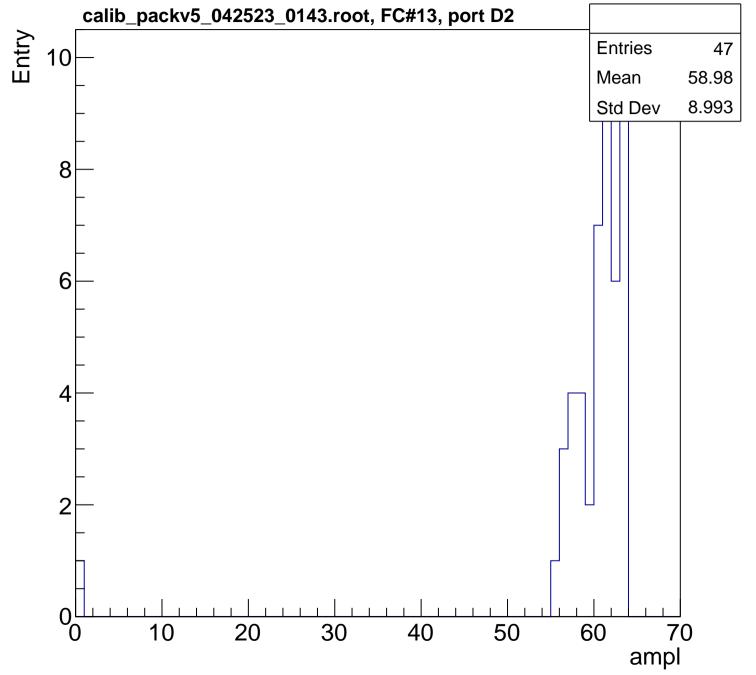


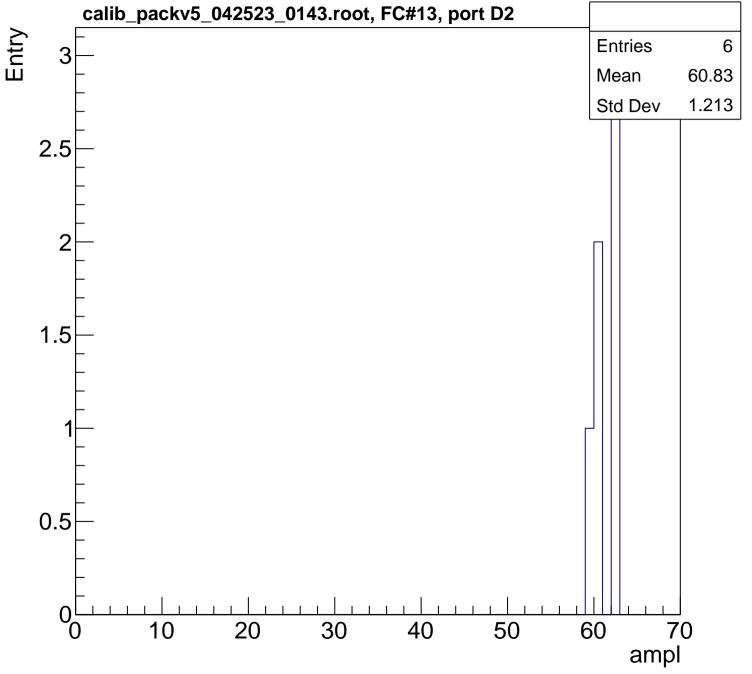




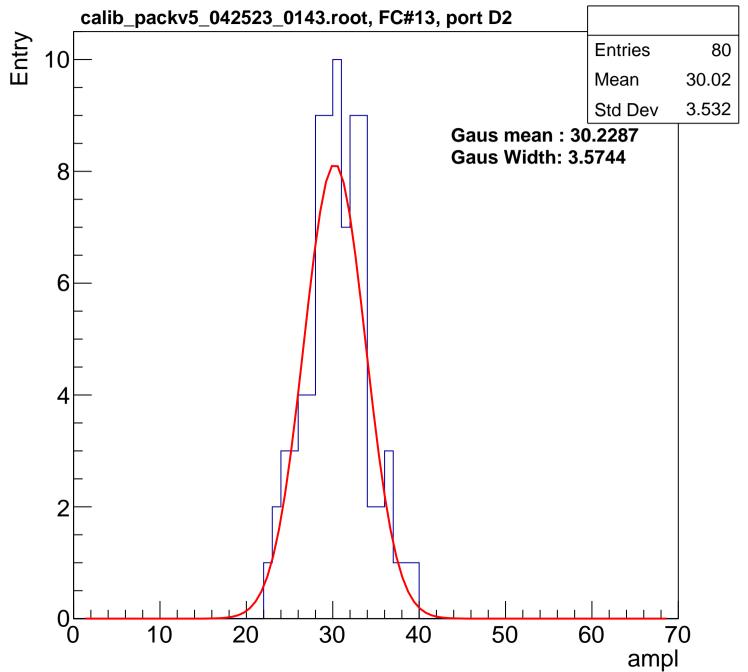


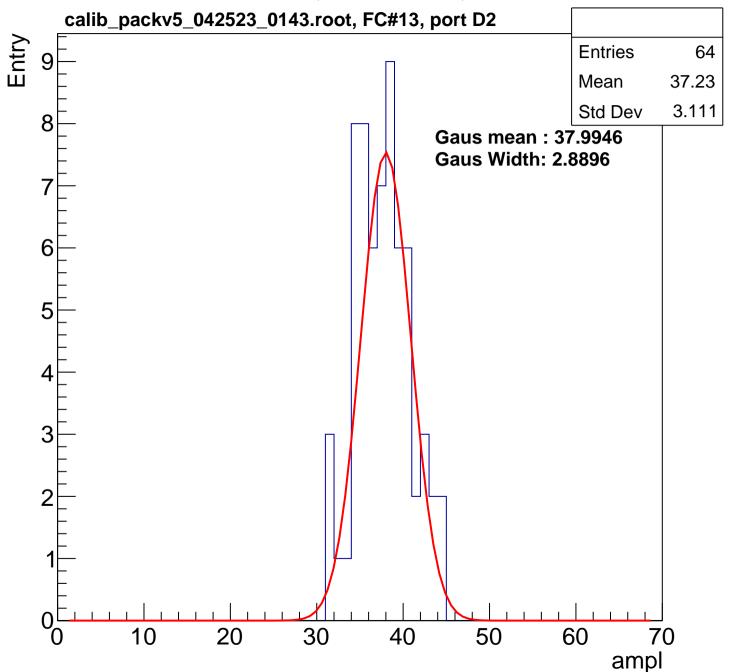


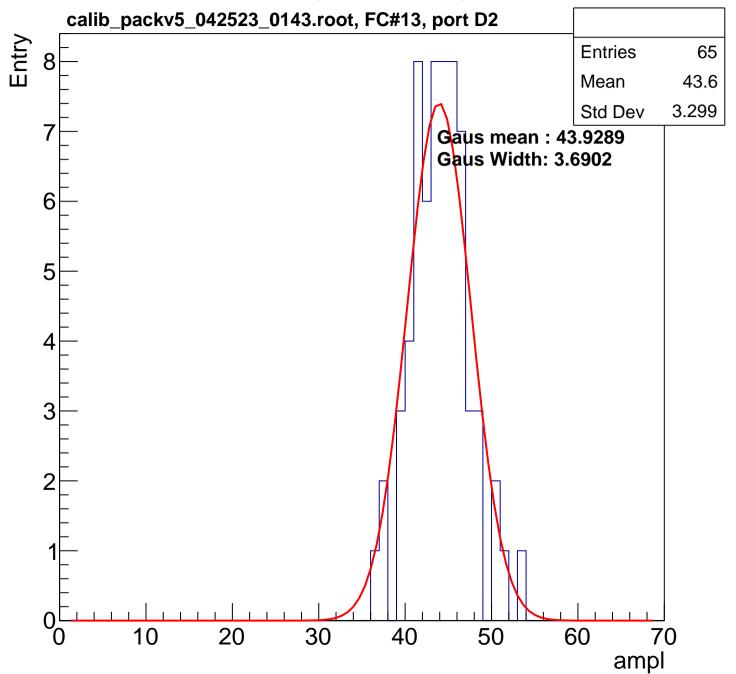


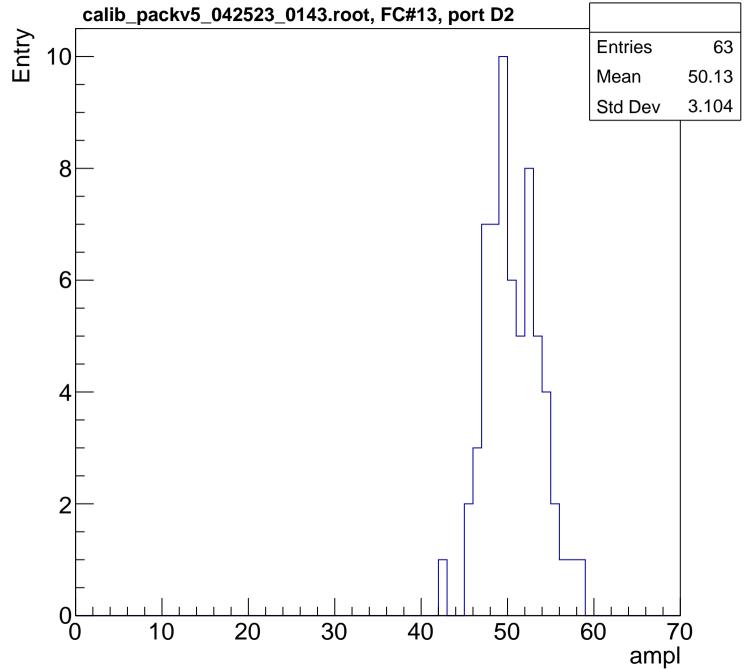


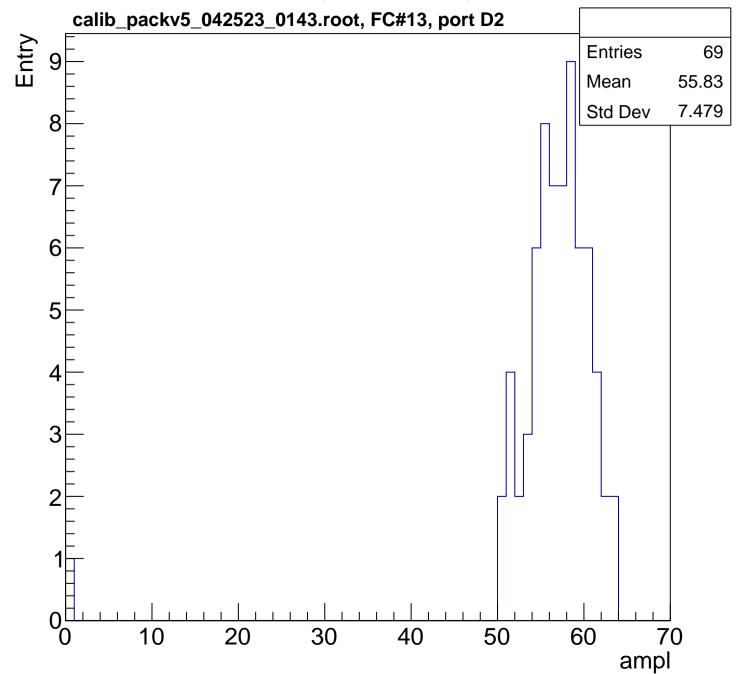
B1L003S, U8-ch90, adc7 calib\_packv5\_042523\_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

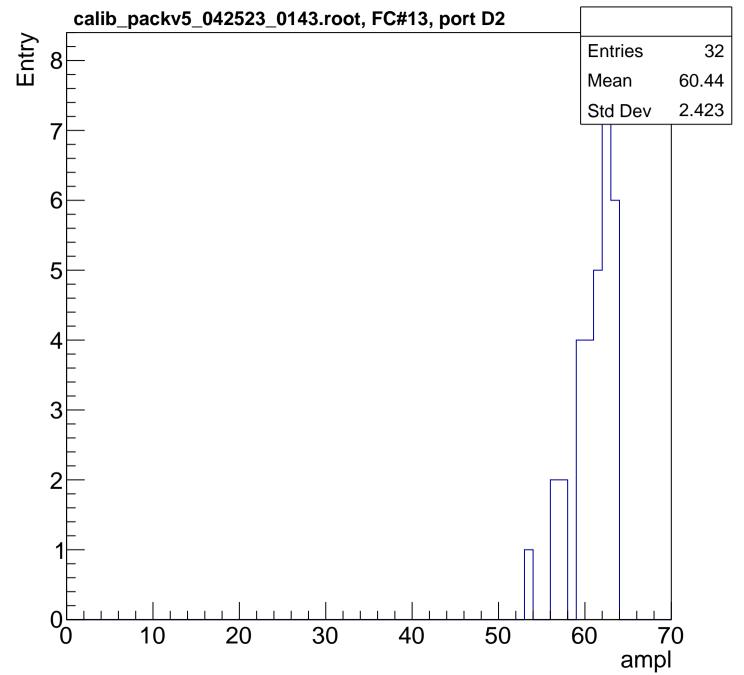


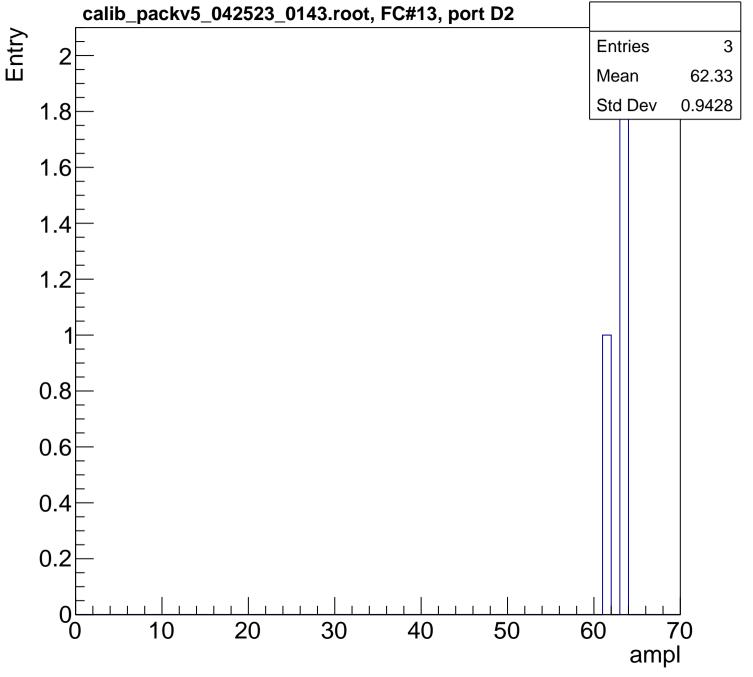




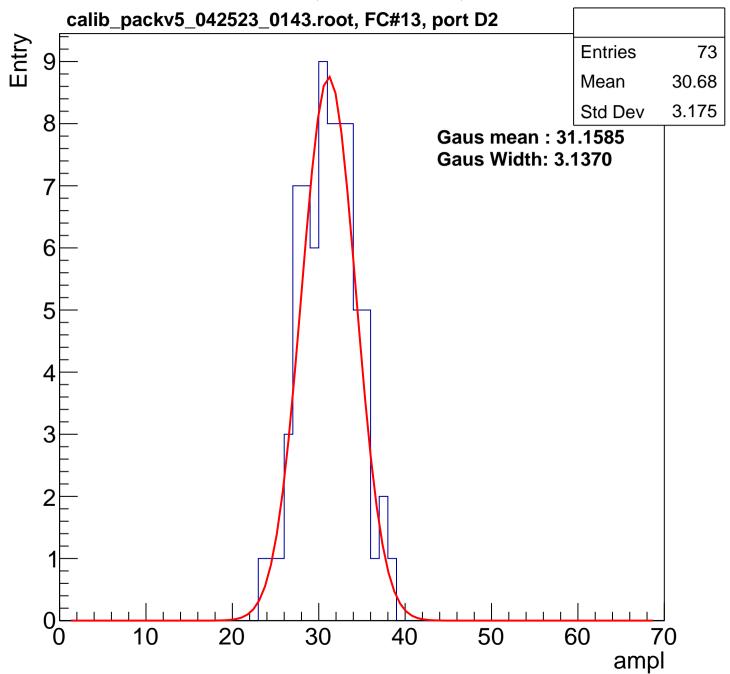


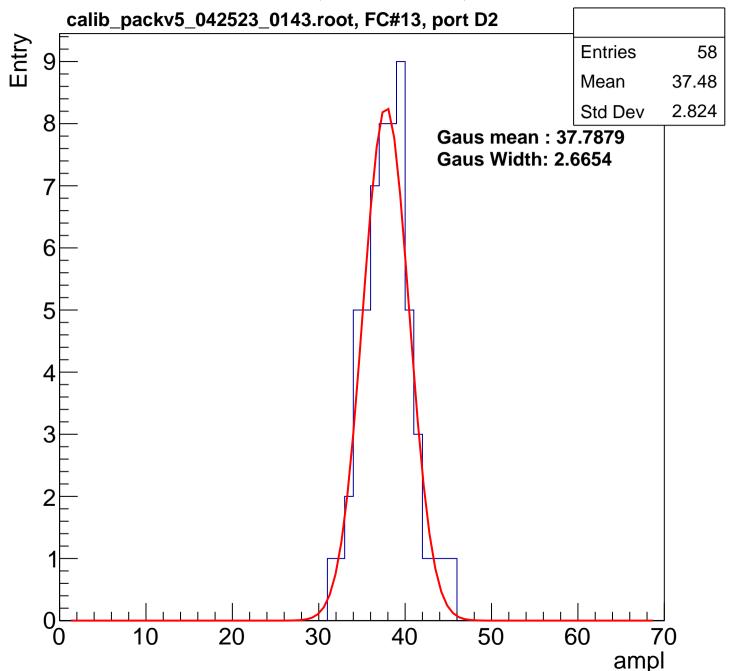


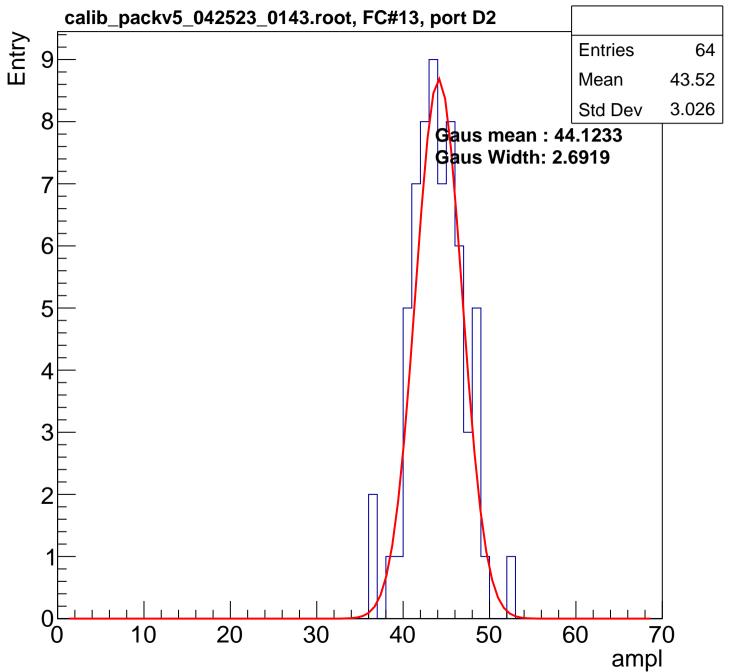


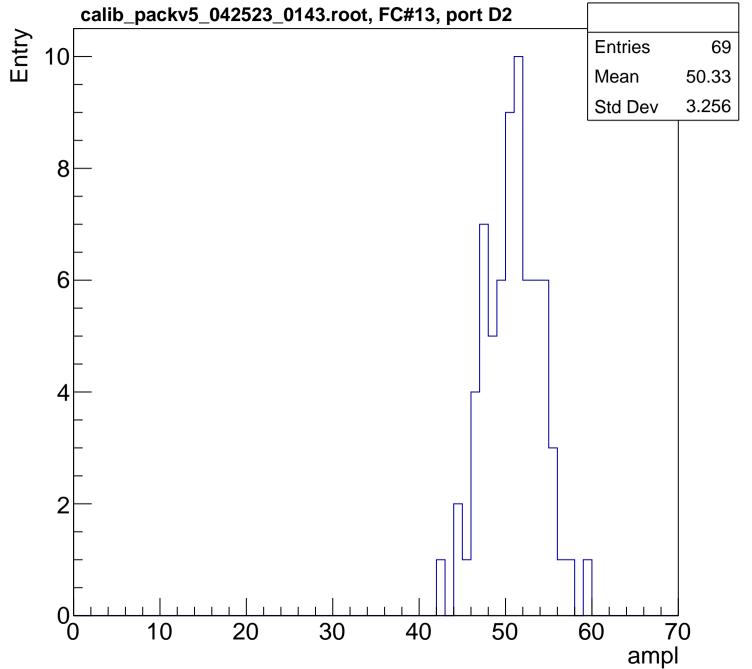


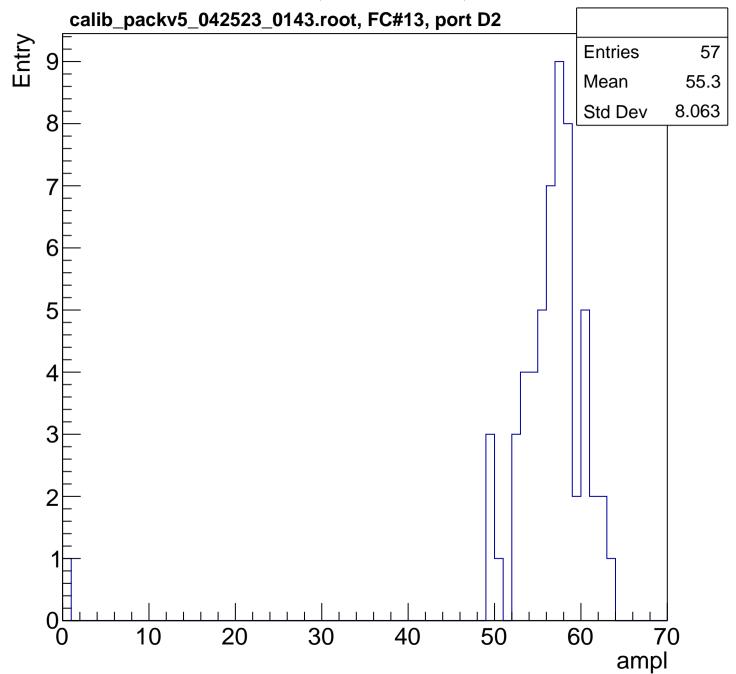
B1L003S, U8-ch91, adc7 calib\_packv5\_042523\_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

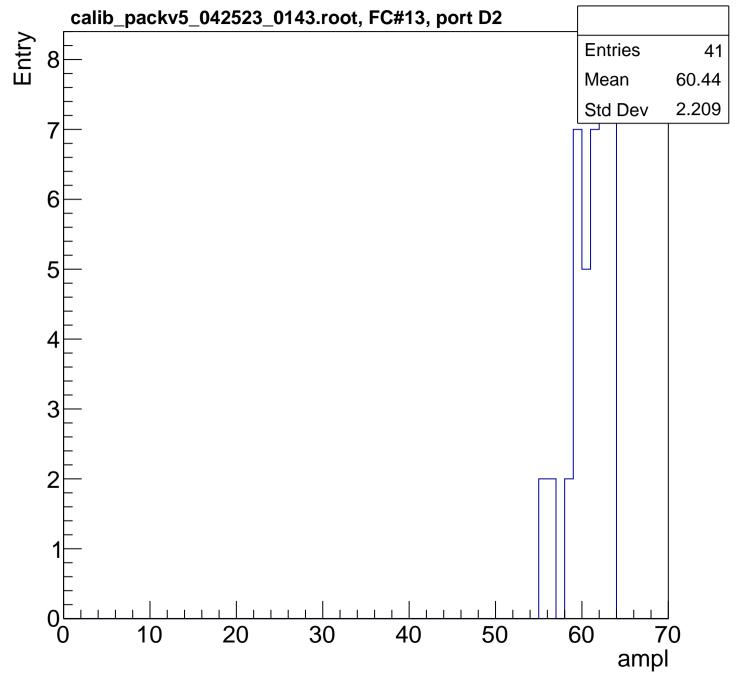


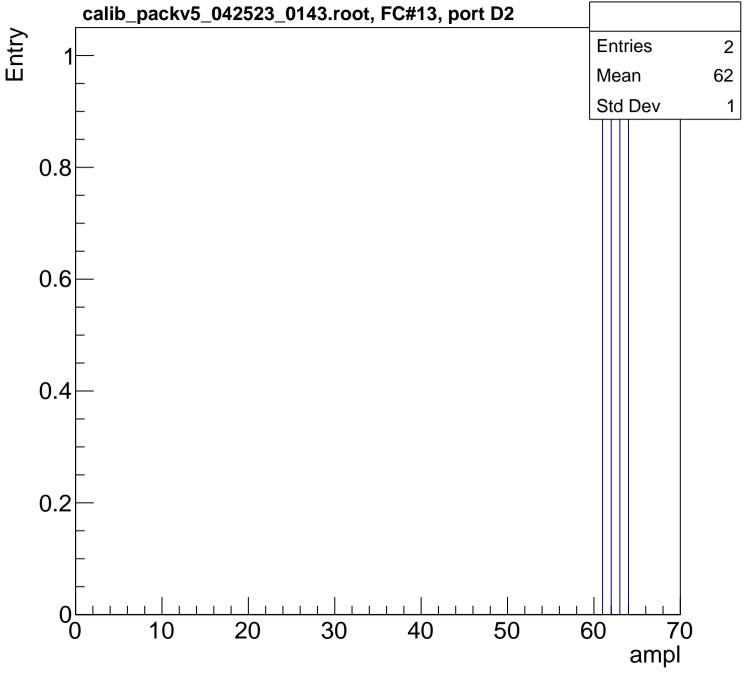




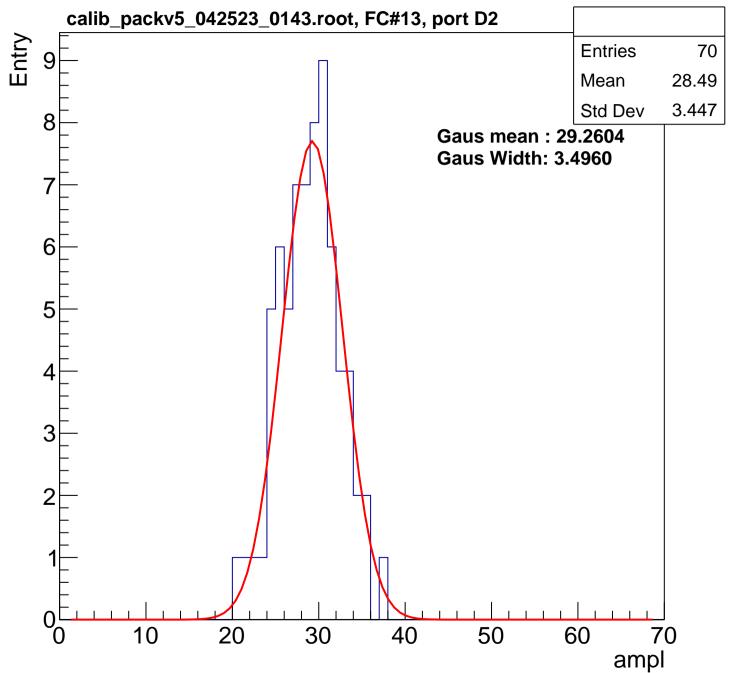


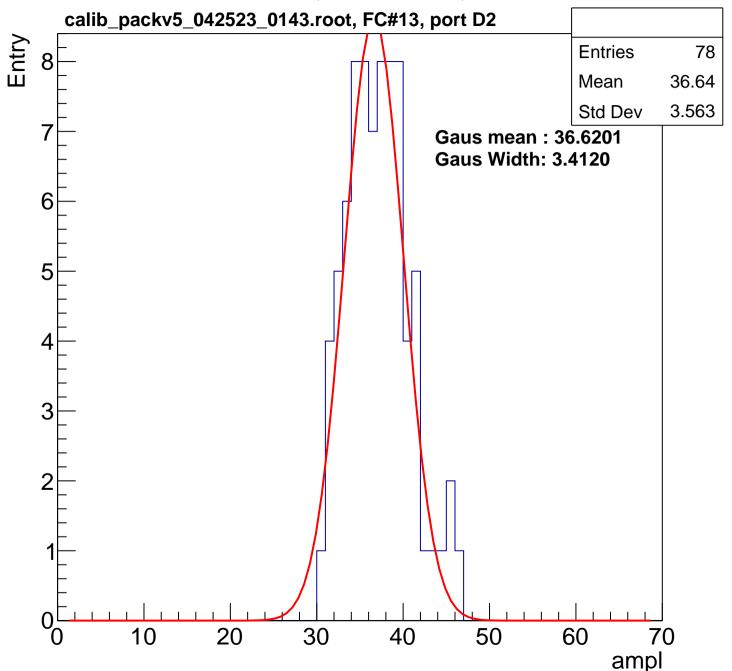


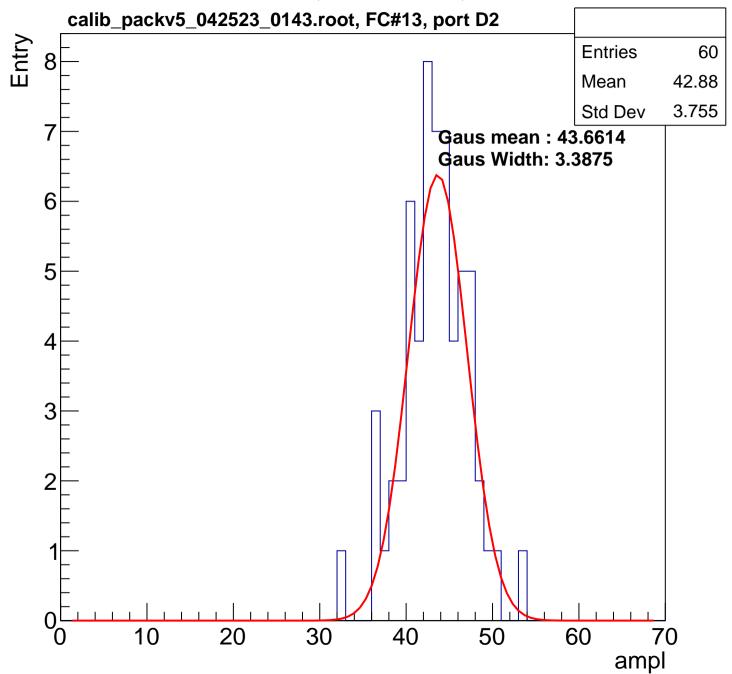


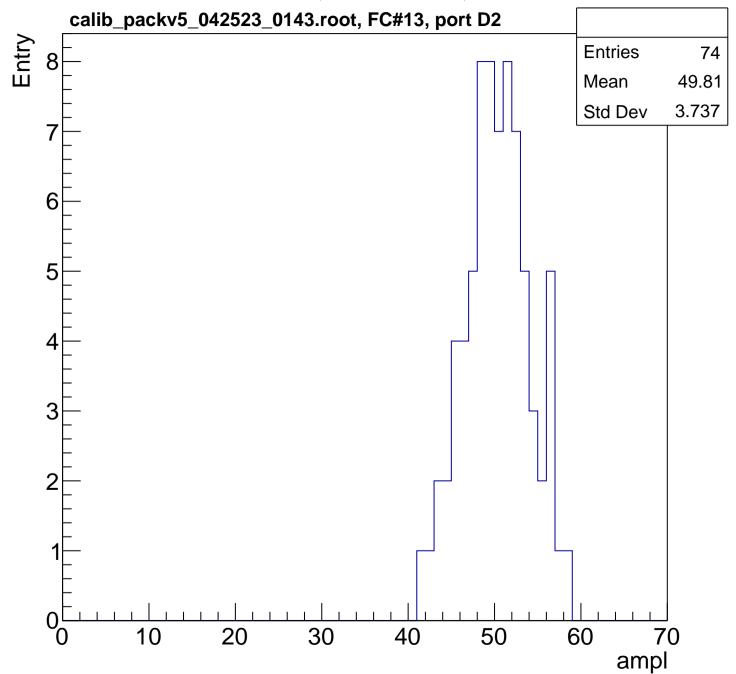


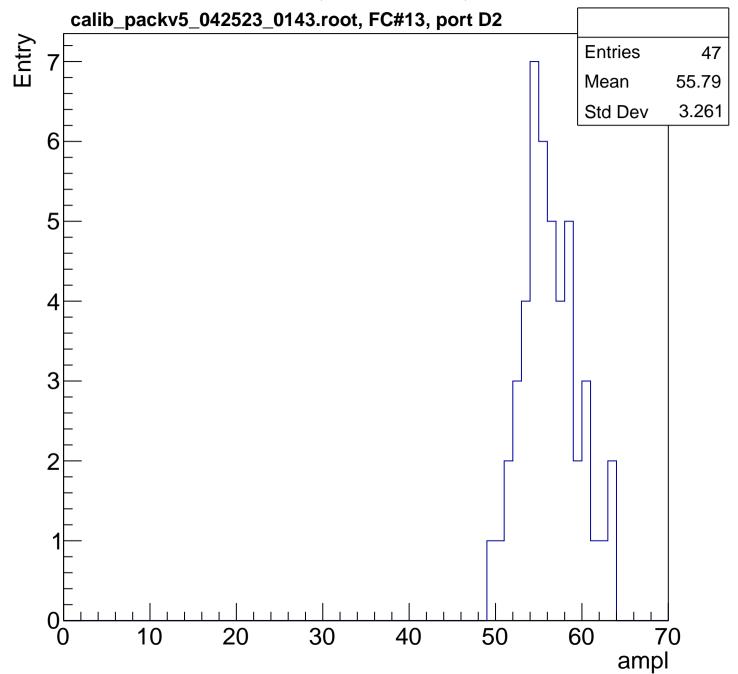


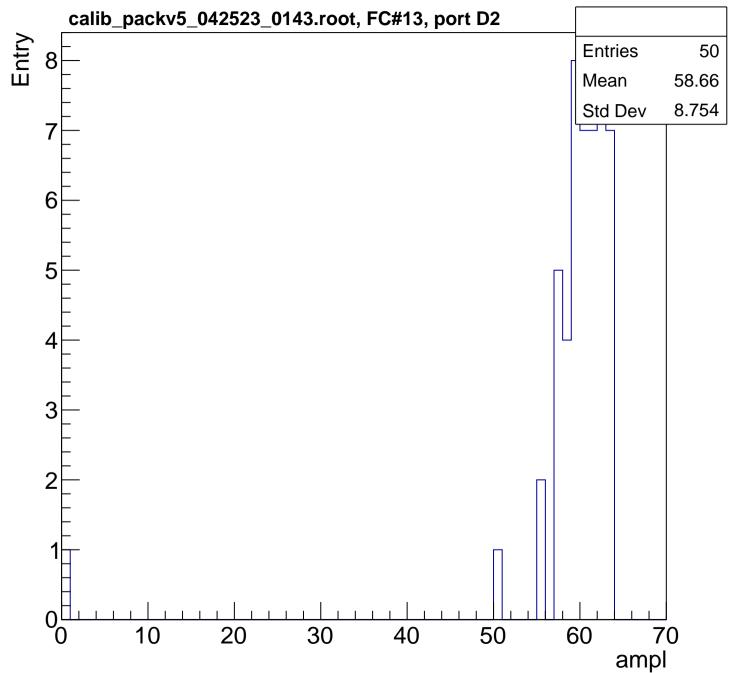


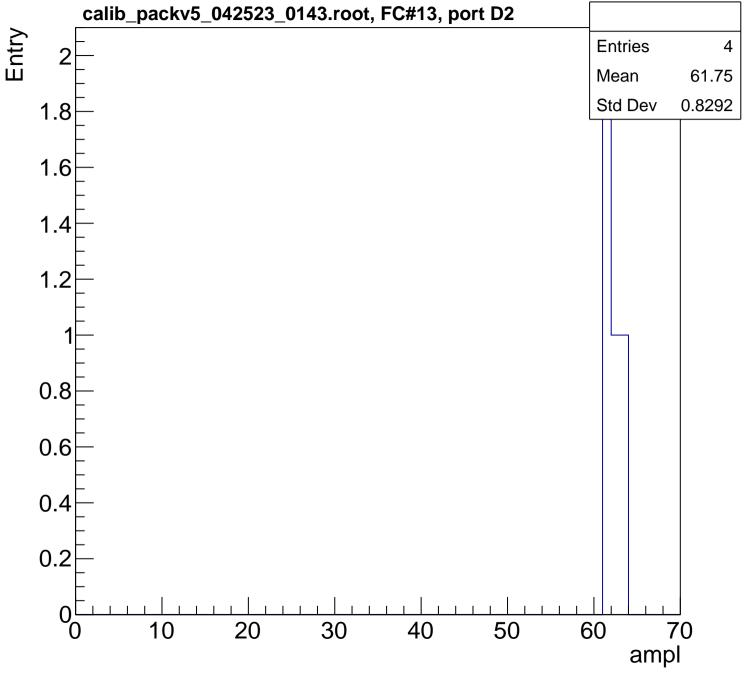




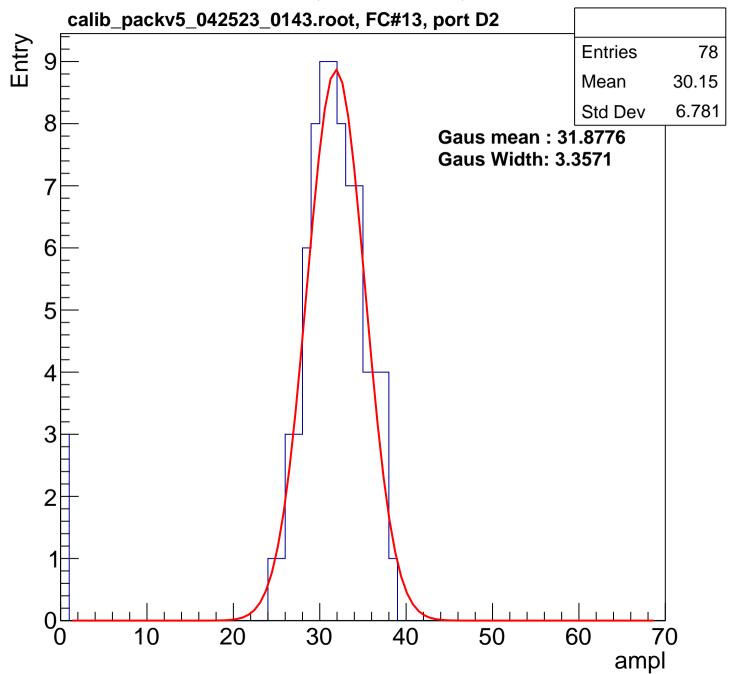


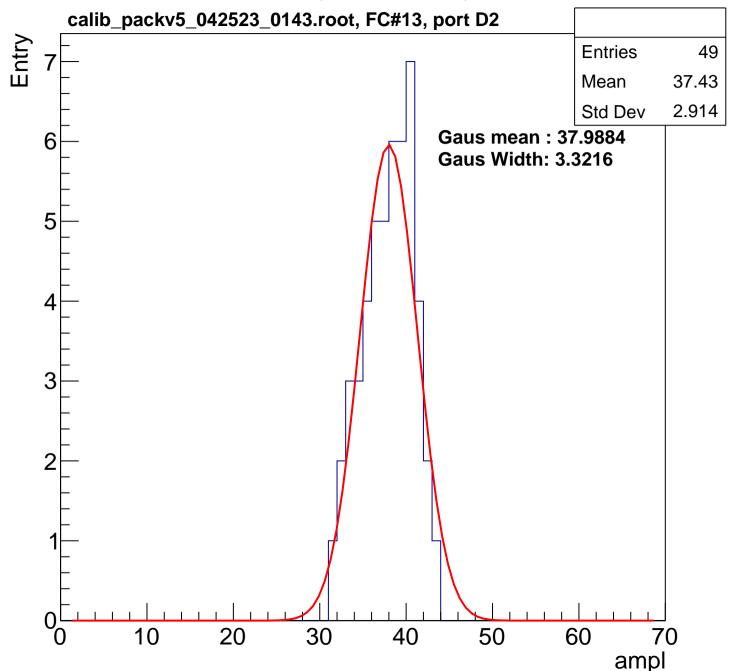


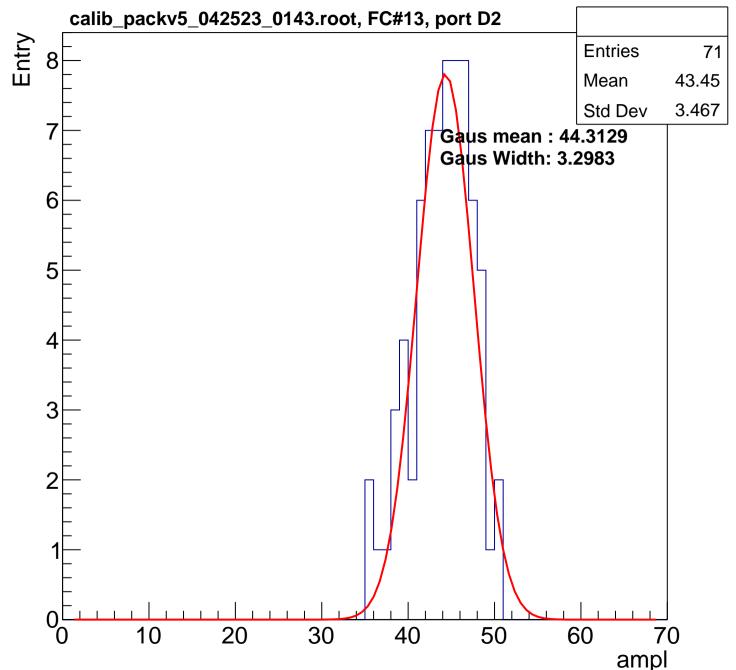


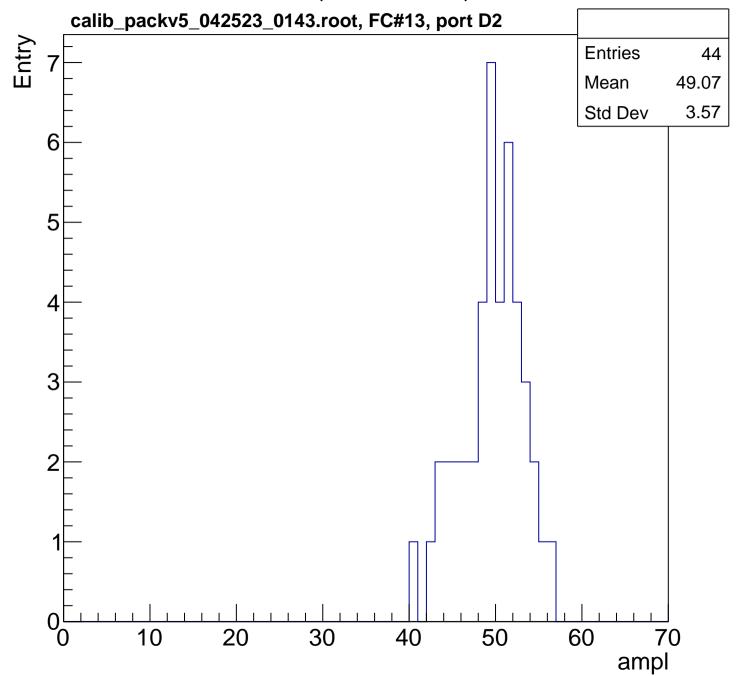


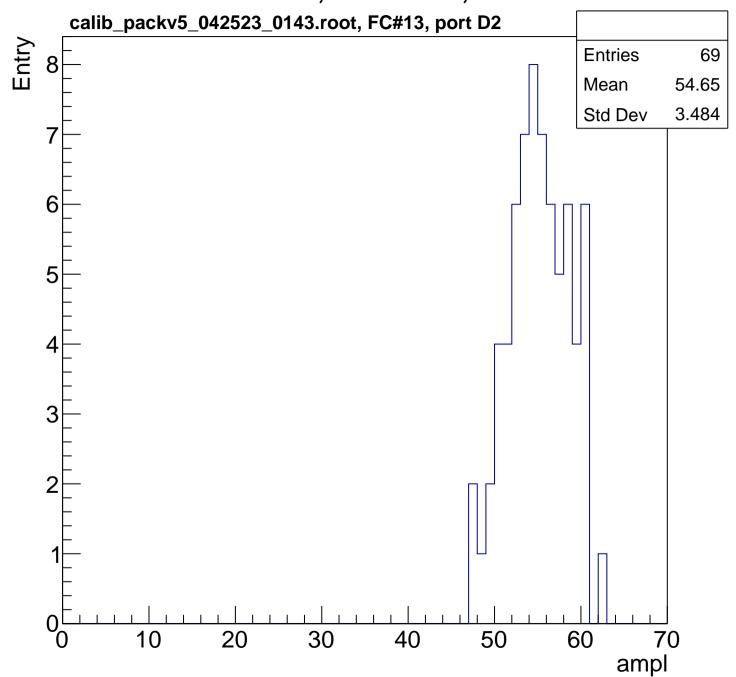
B1L003S, U8-ch93, adc7 calib\_packv5\_042523\_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

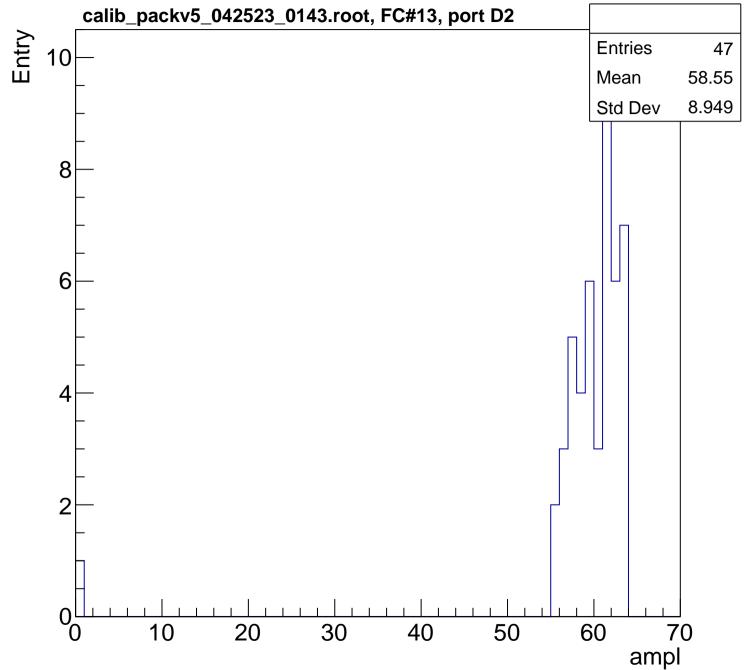


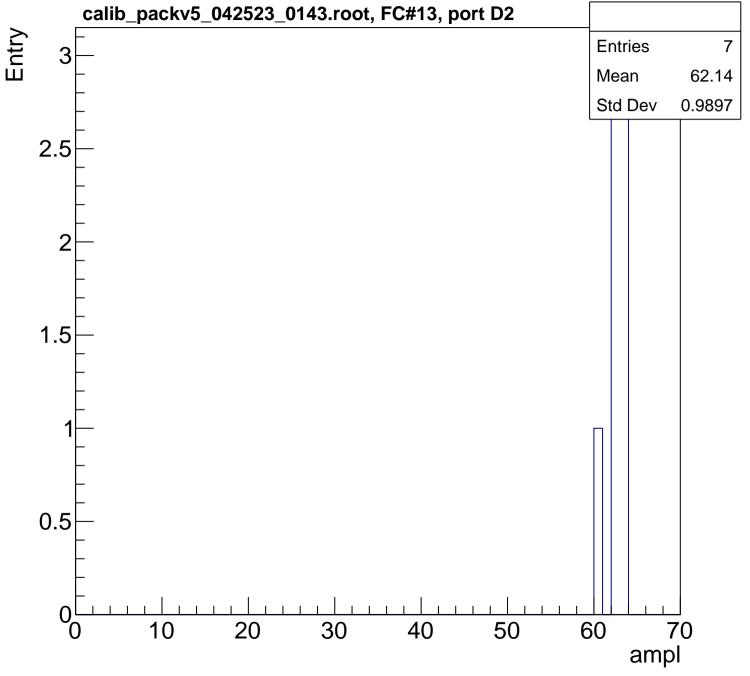


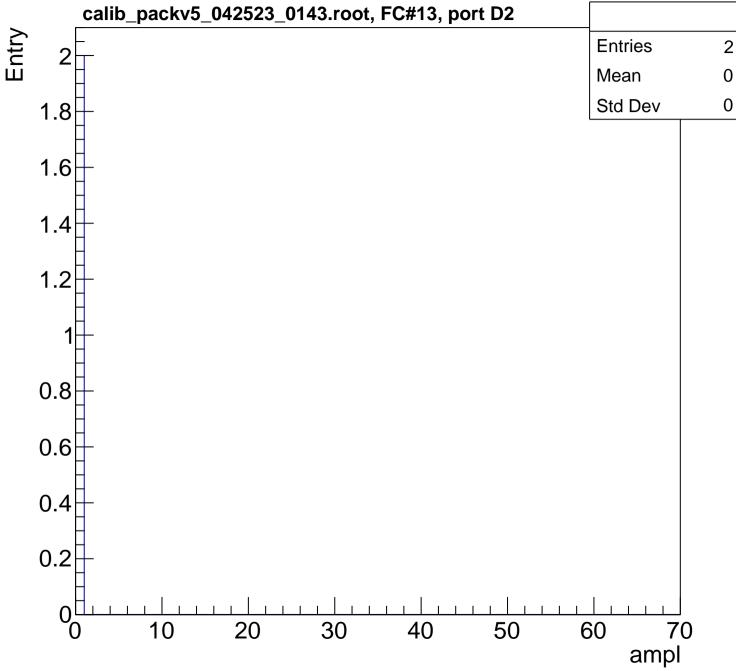


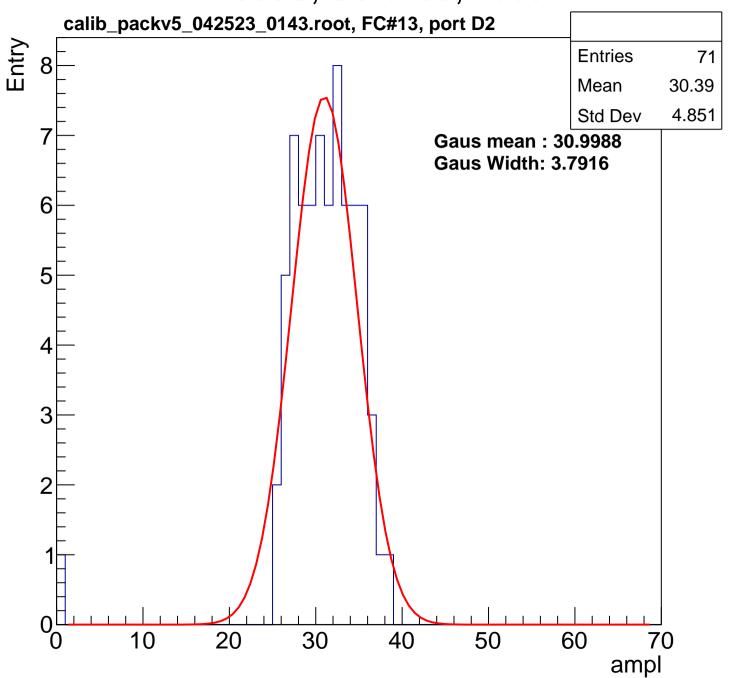


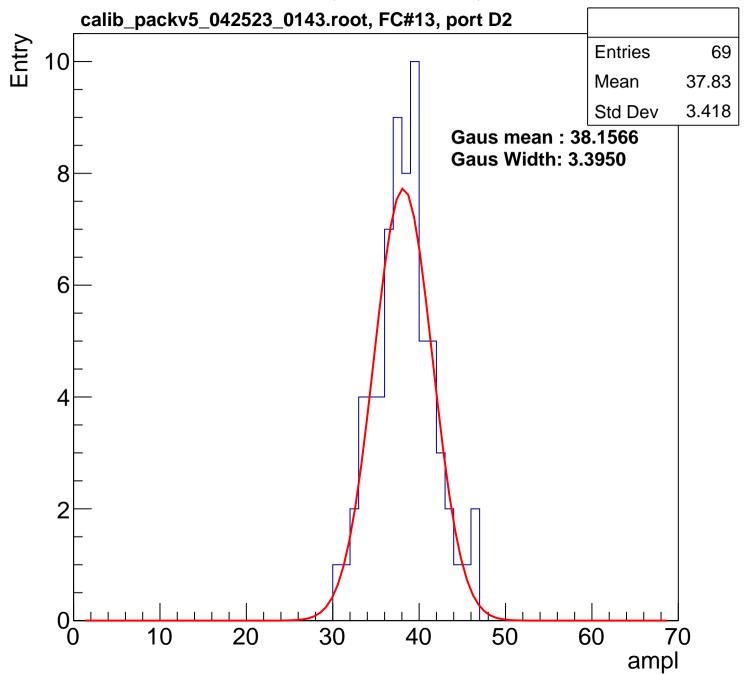


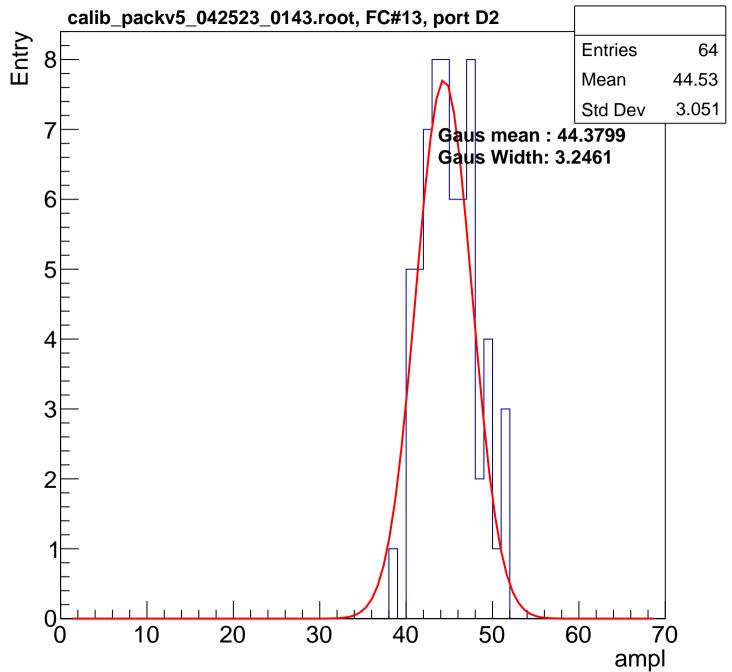


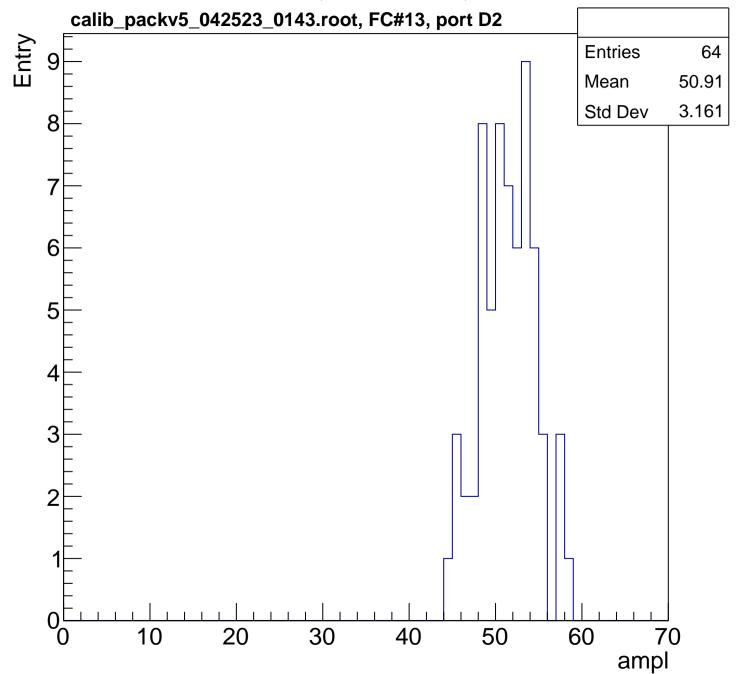


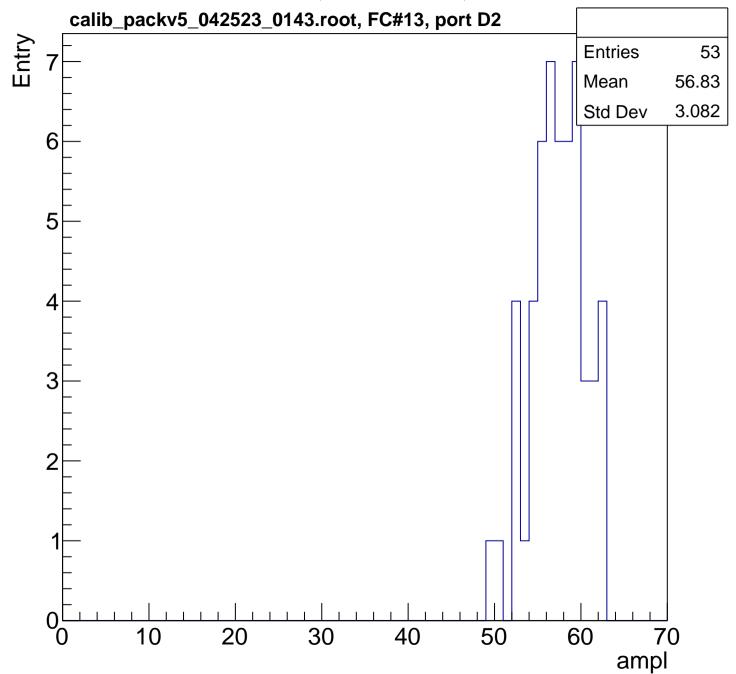


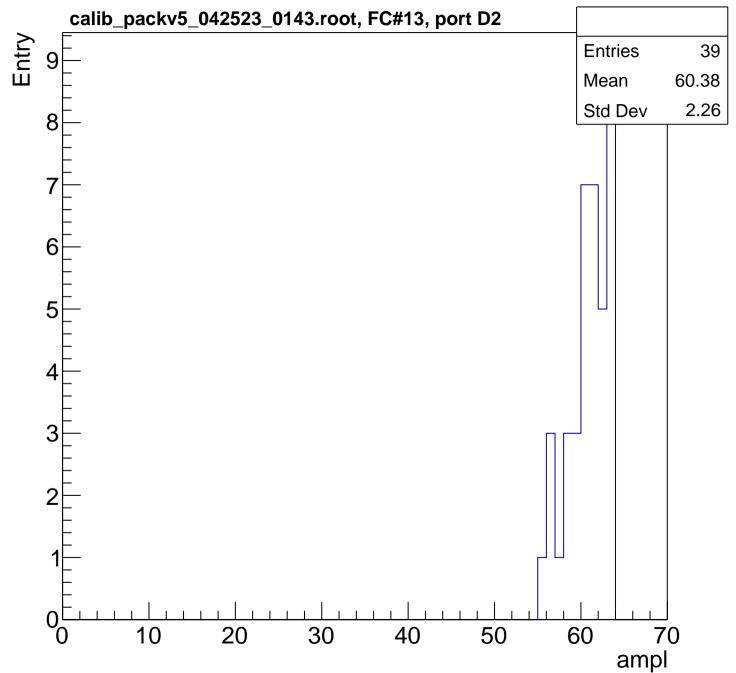


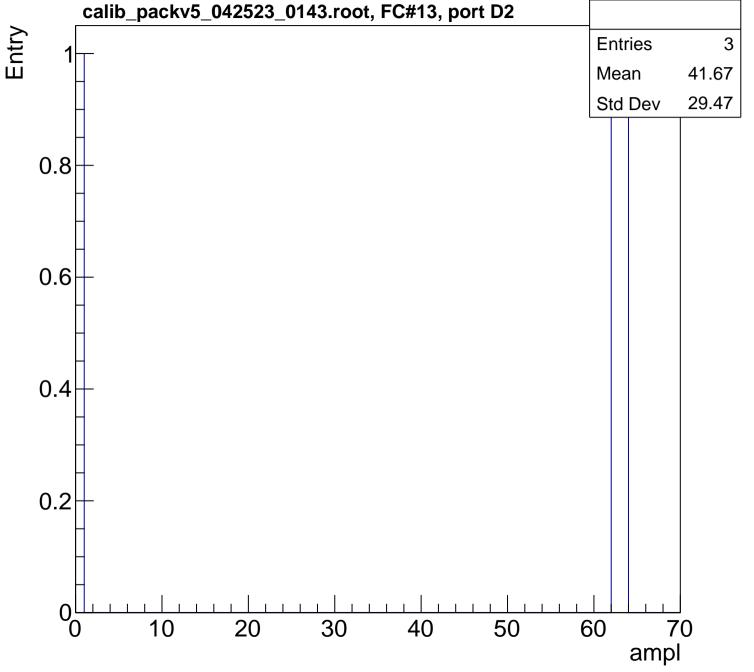




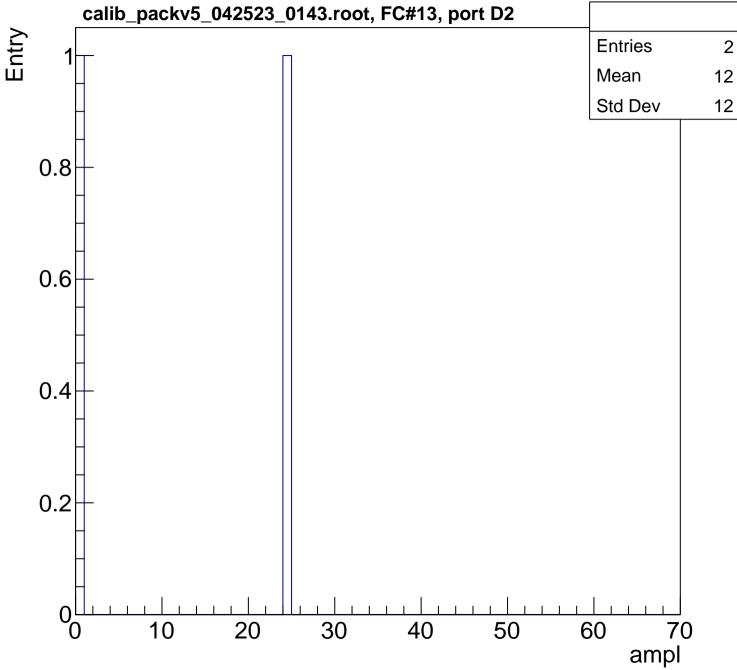


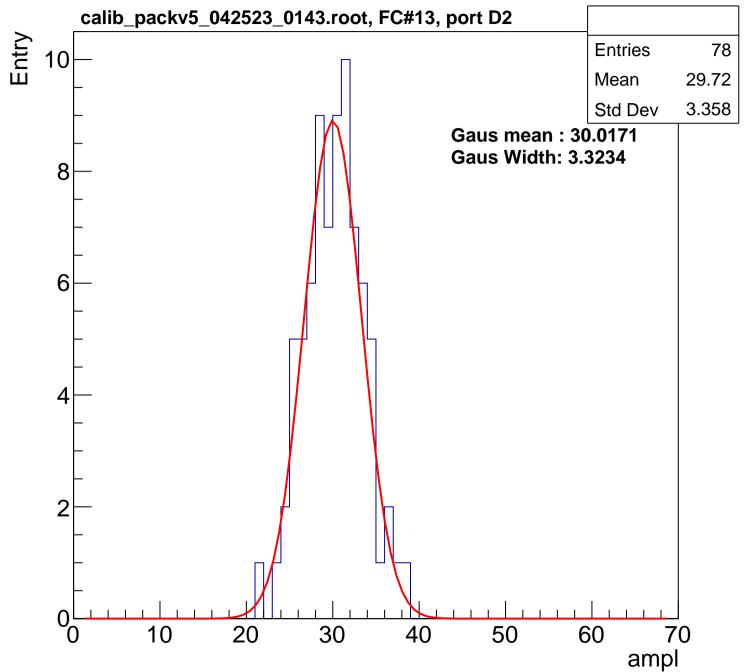


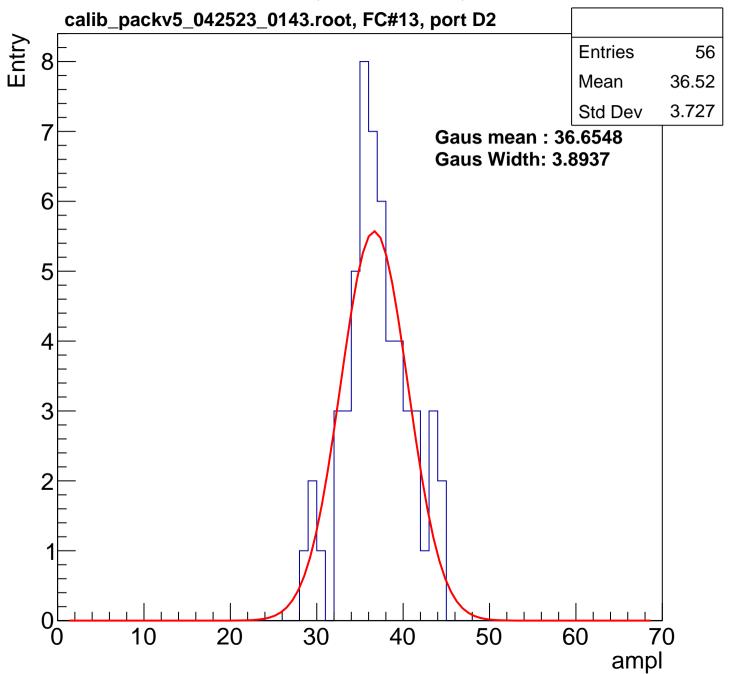


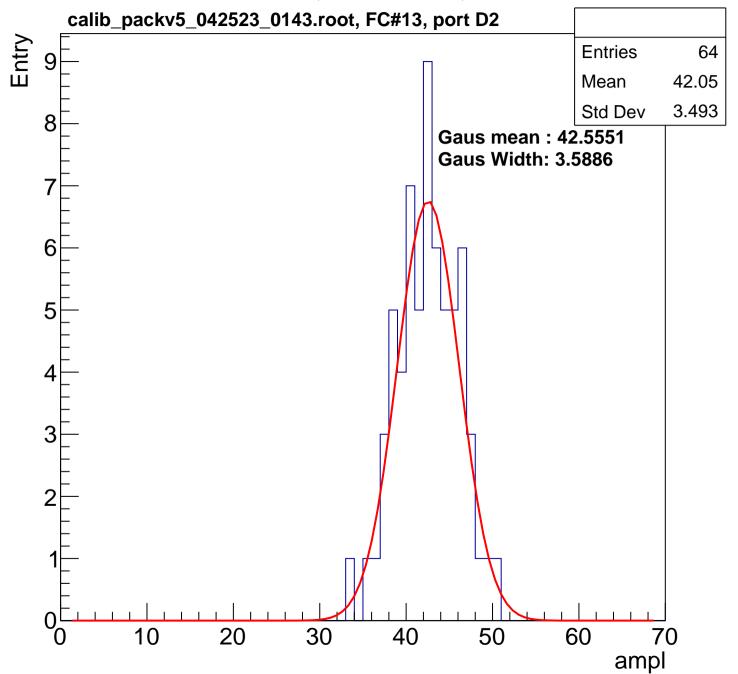


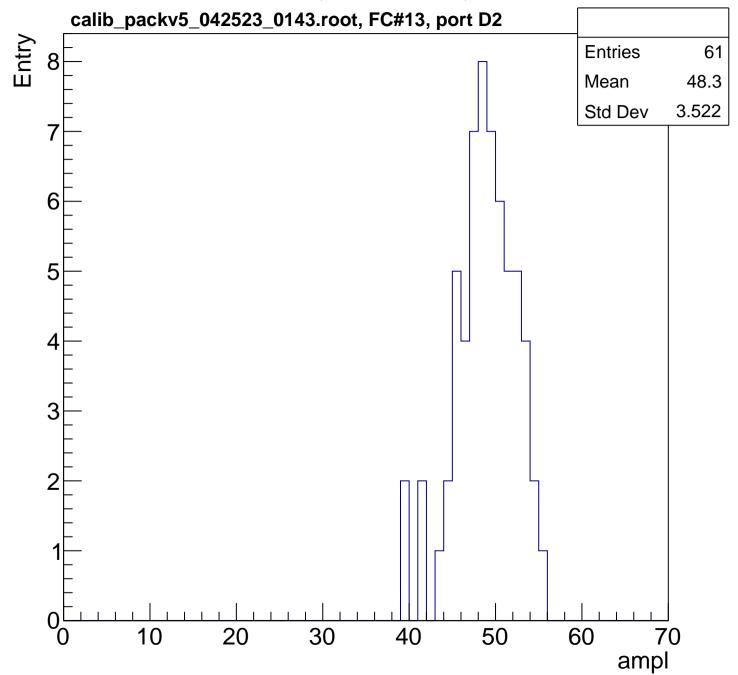
2

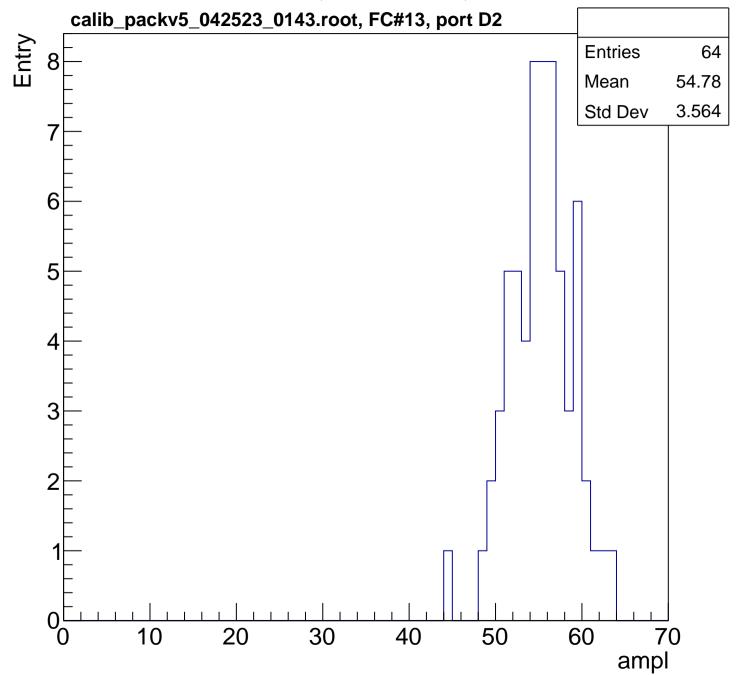


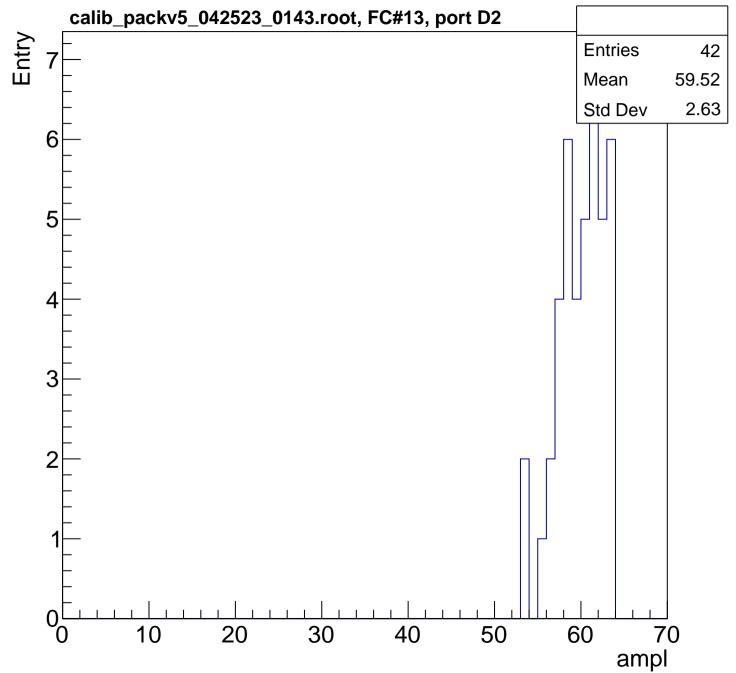


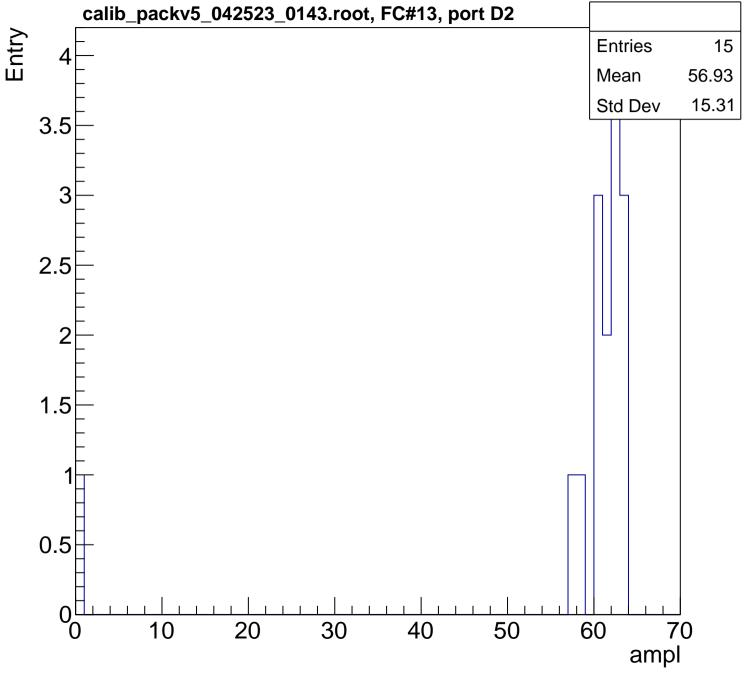




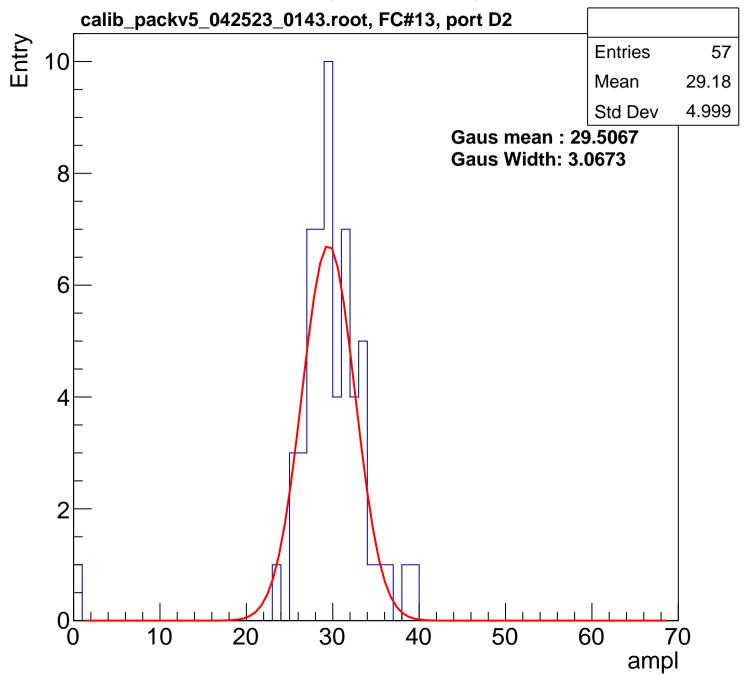


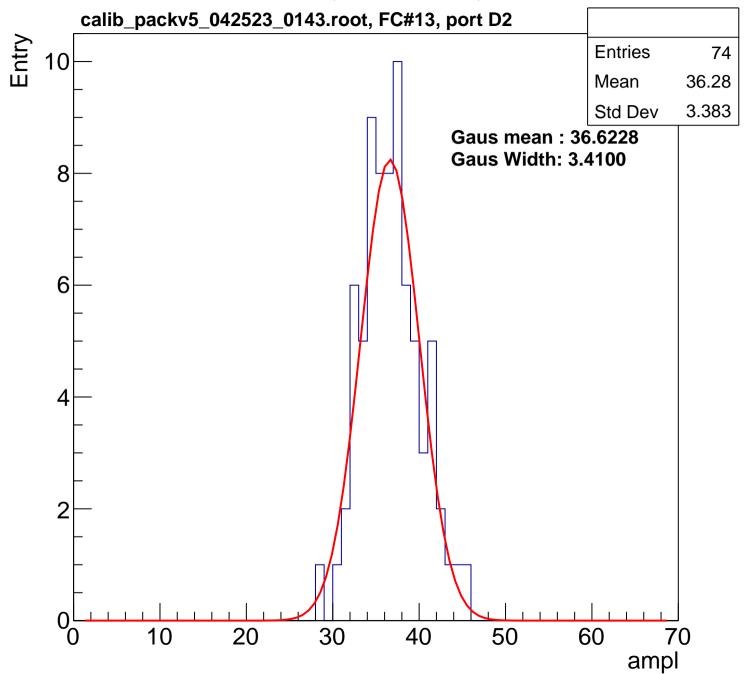


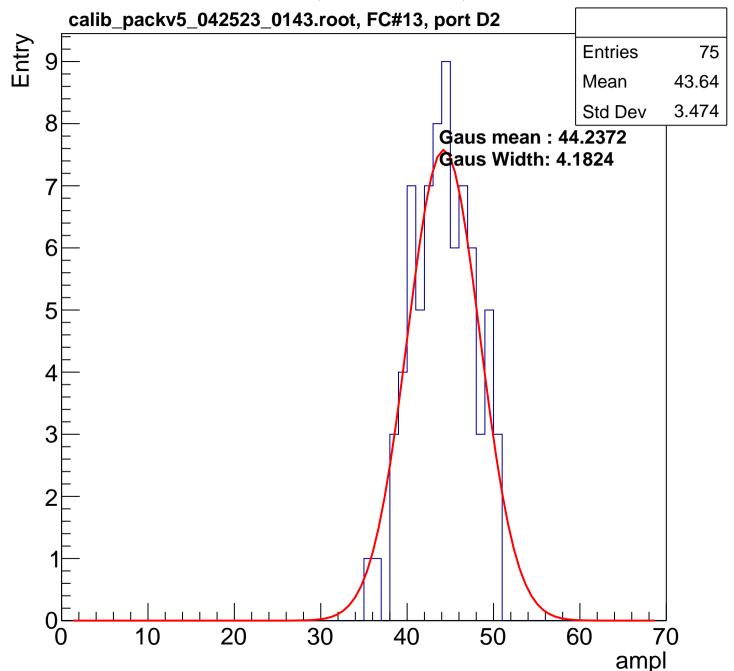


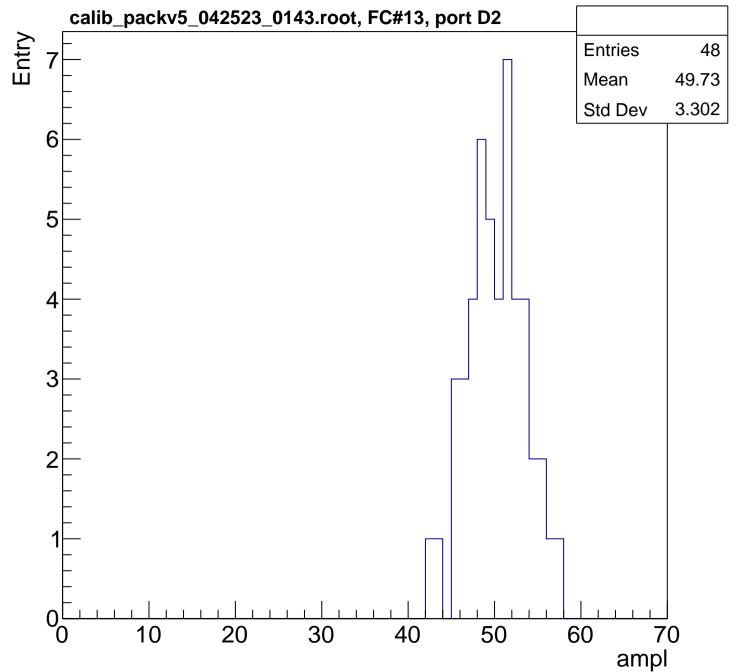


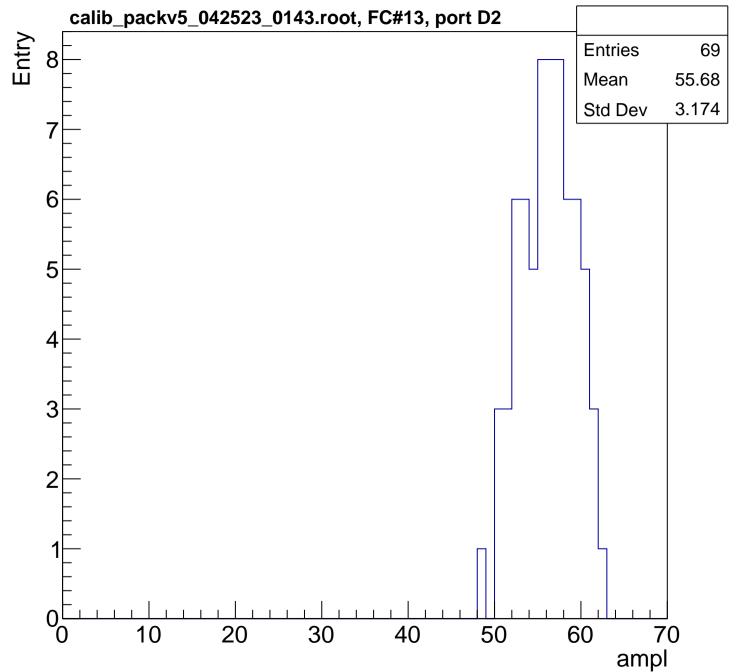
B1L003S, U8-ch96, adc7 calib\_packv5\_042523\_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

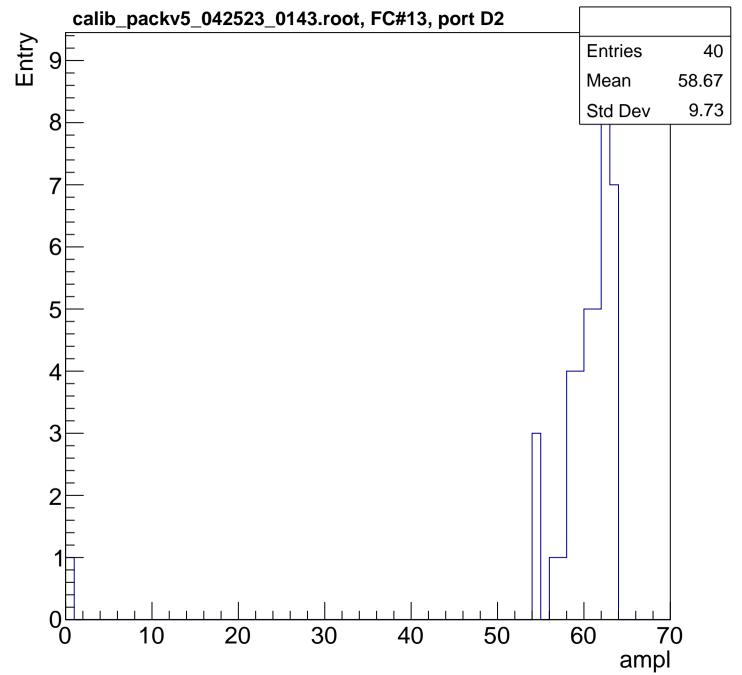


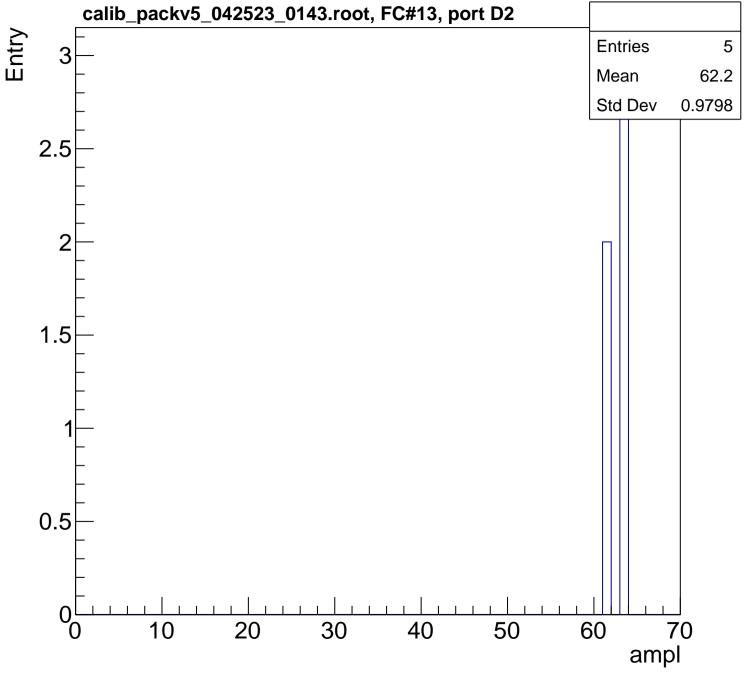




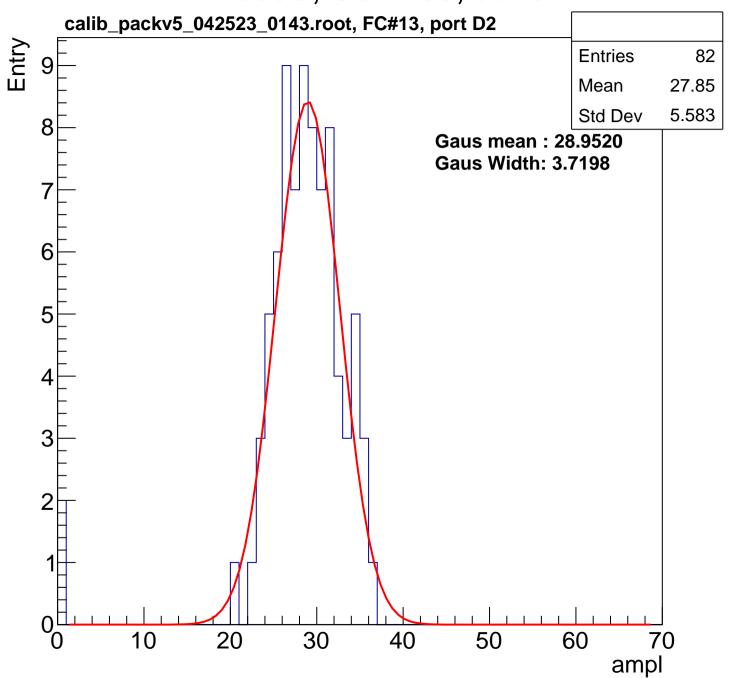


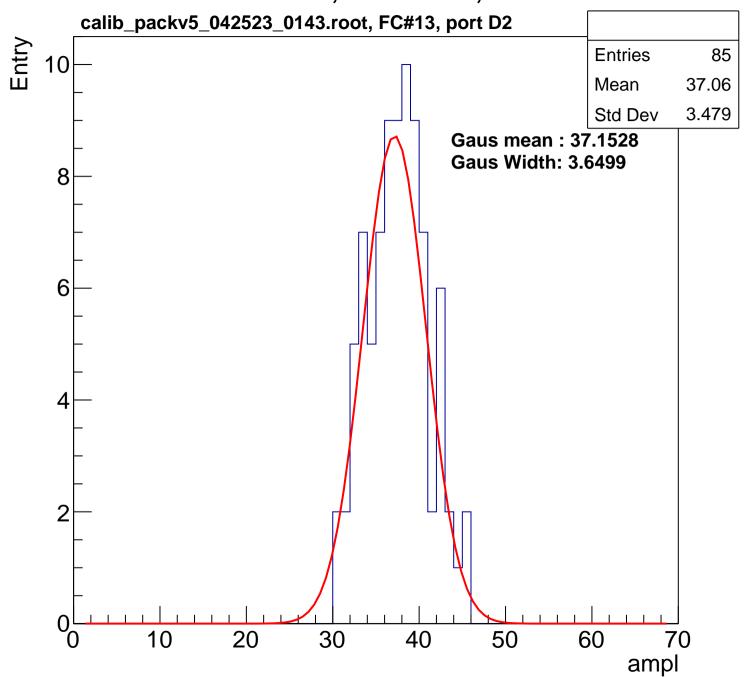


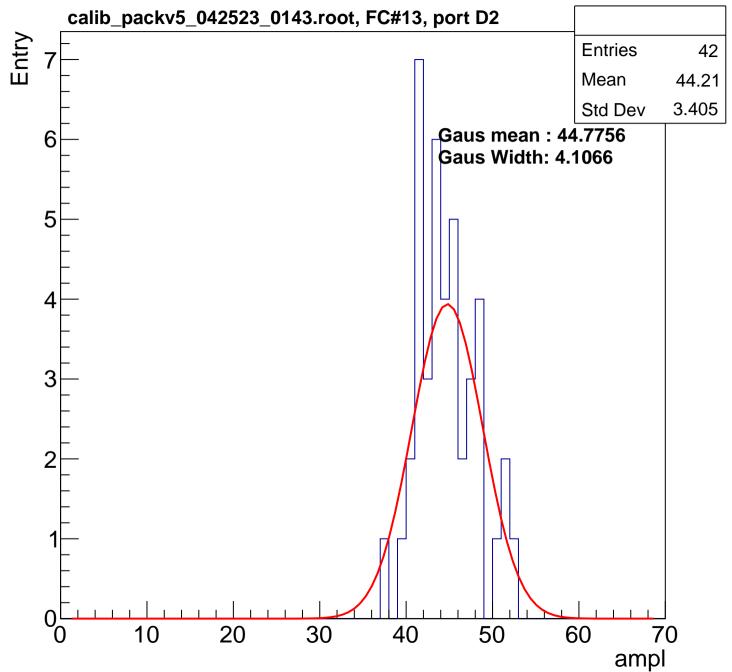


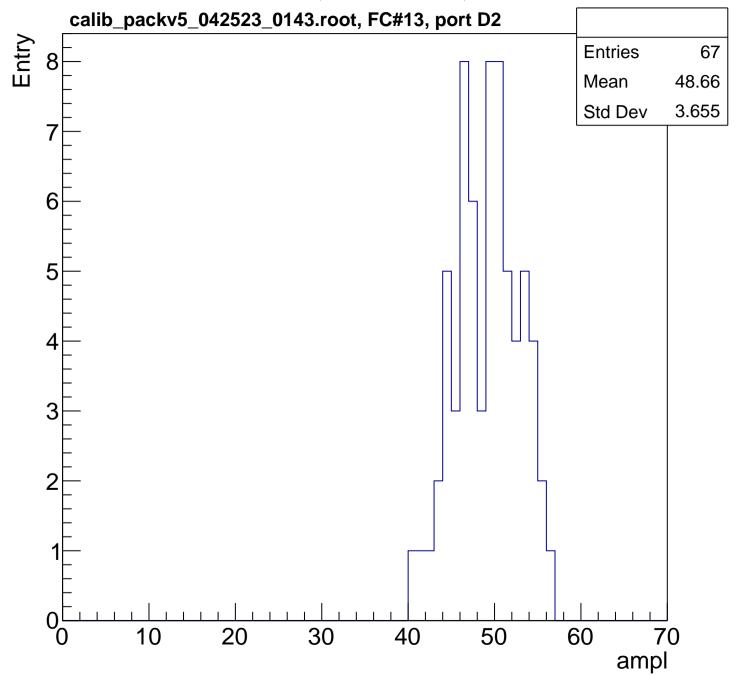


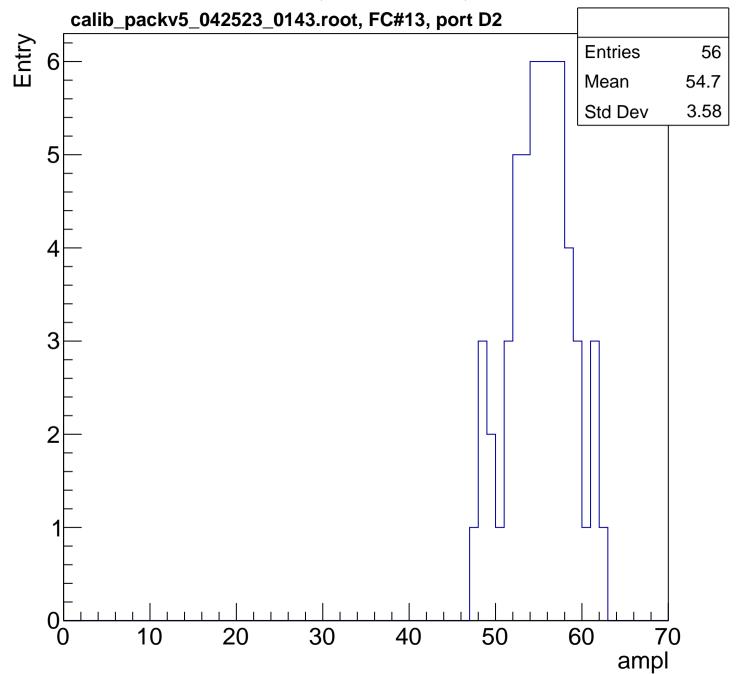
B1L003S, U8-ch97, adc7 calib\_packv5\_042523\_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

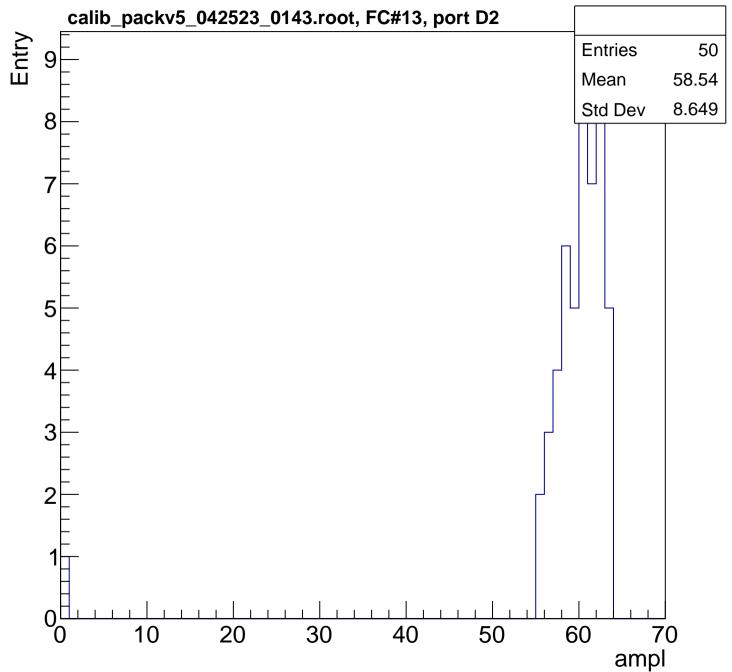


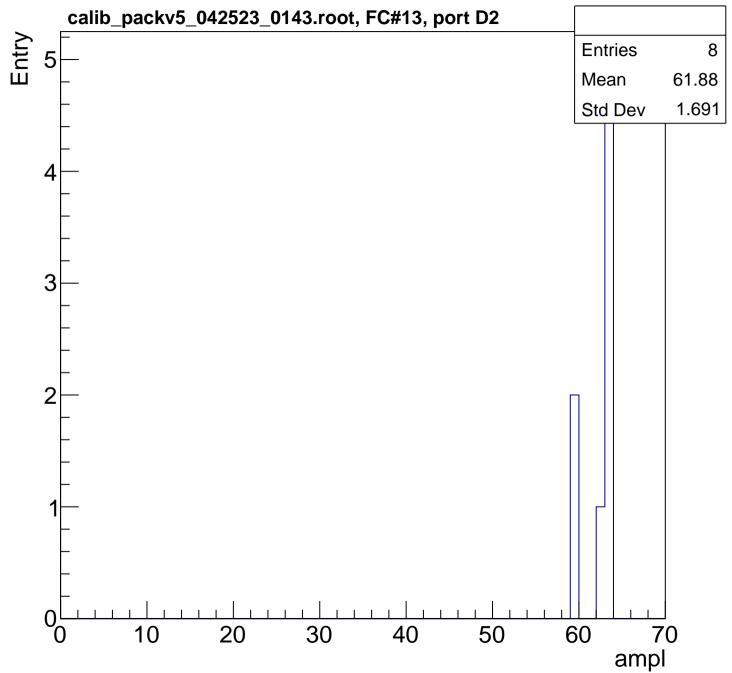


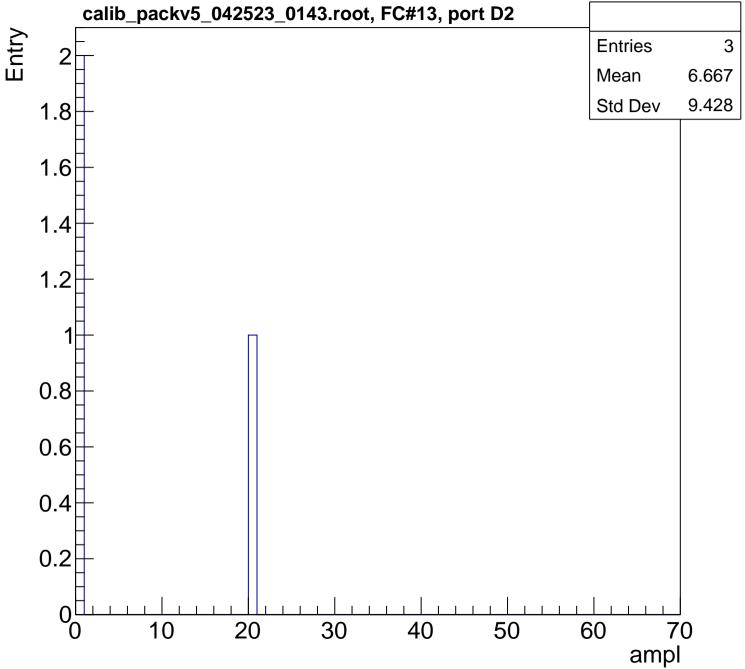


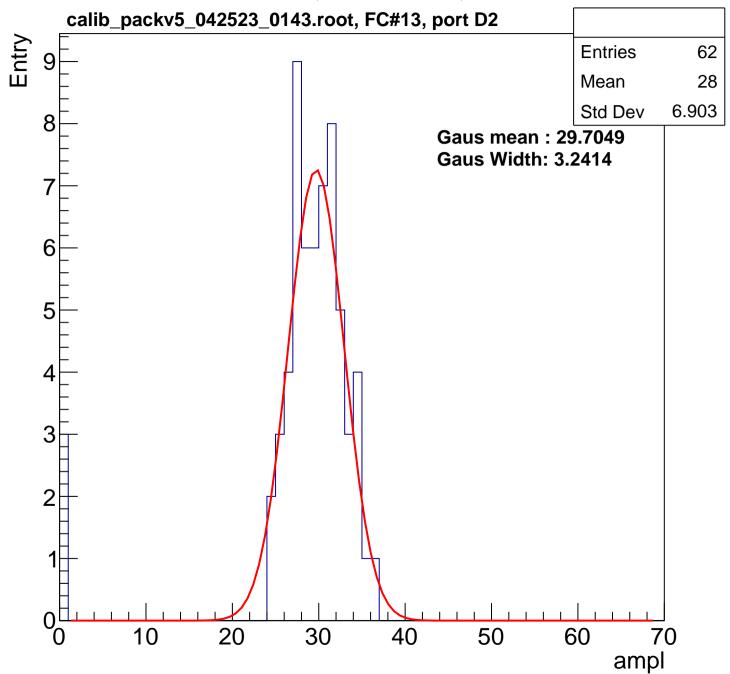


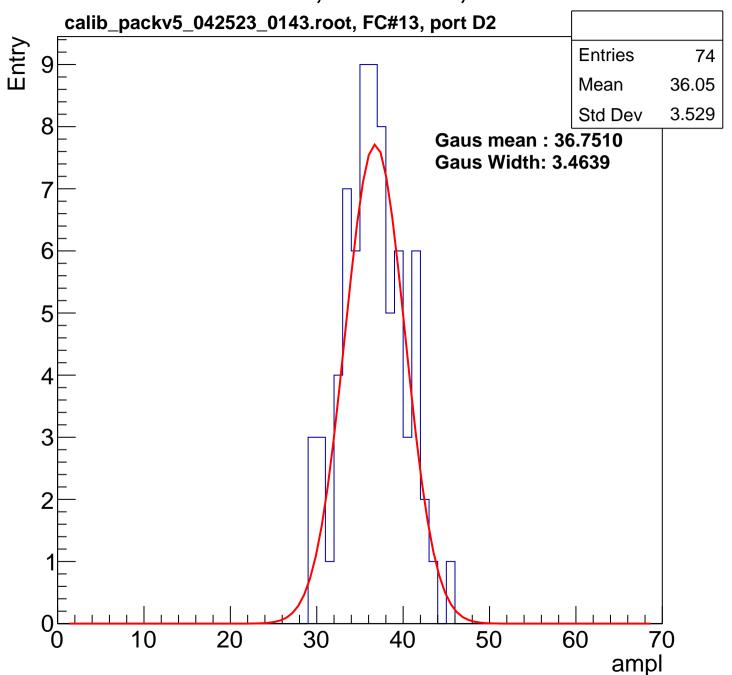


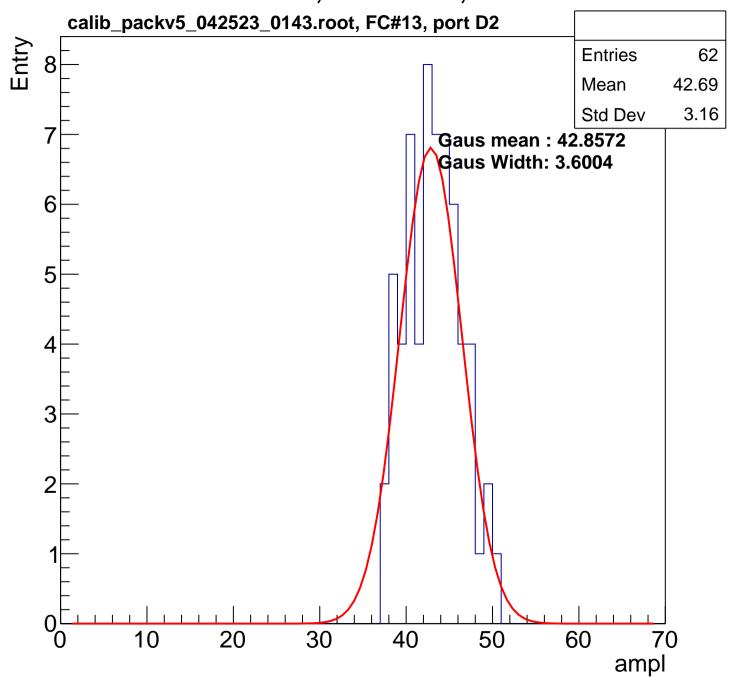


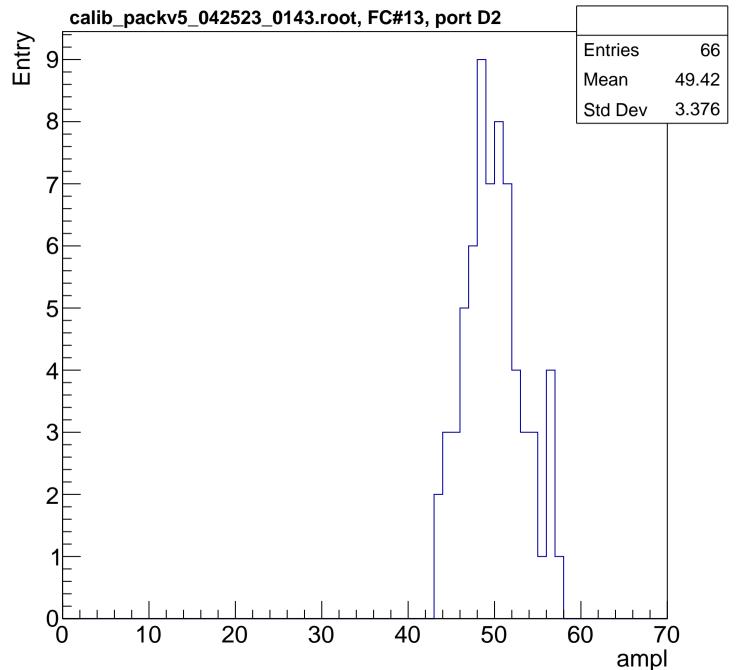


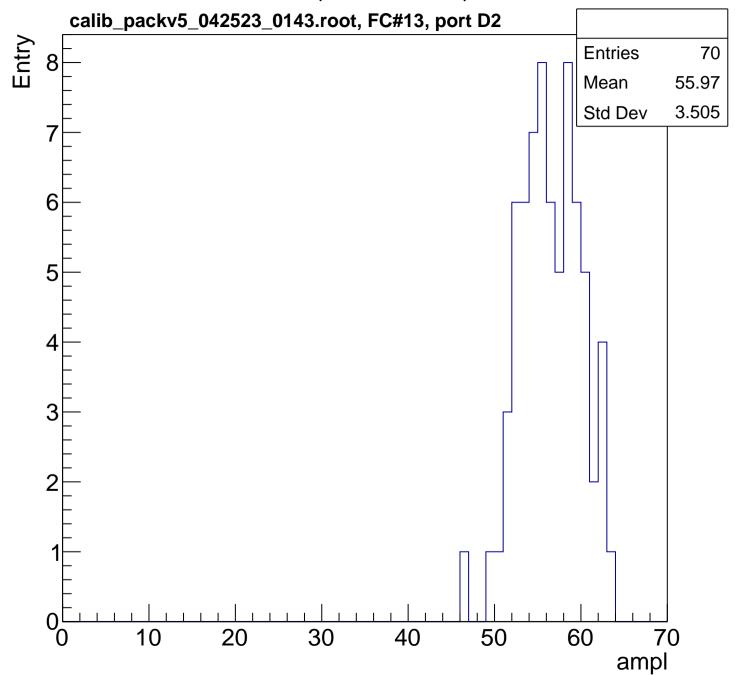


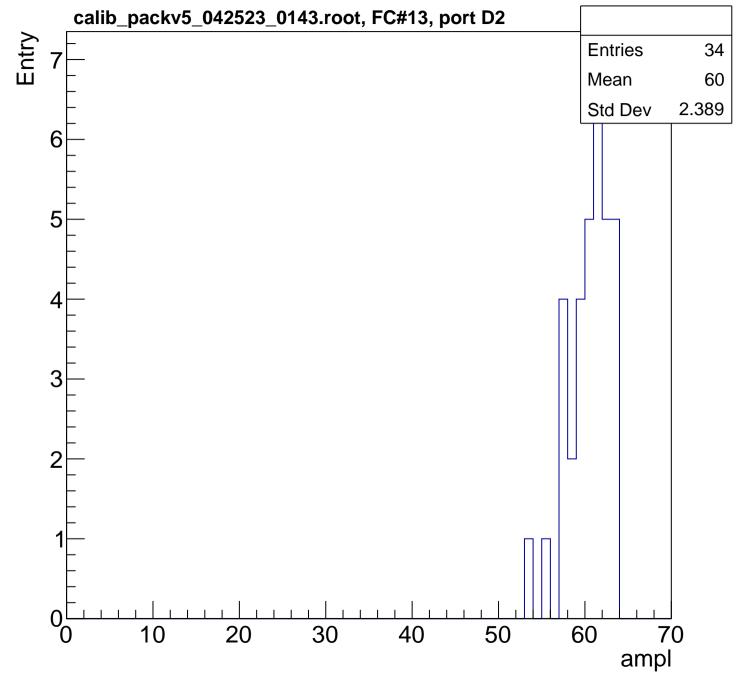


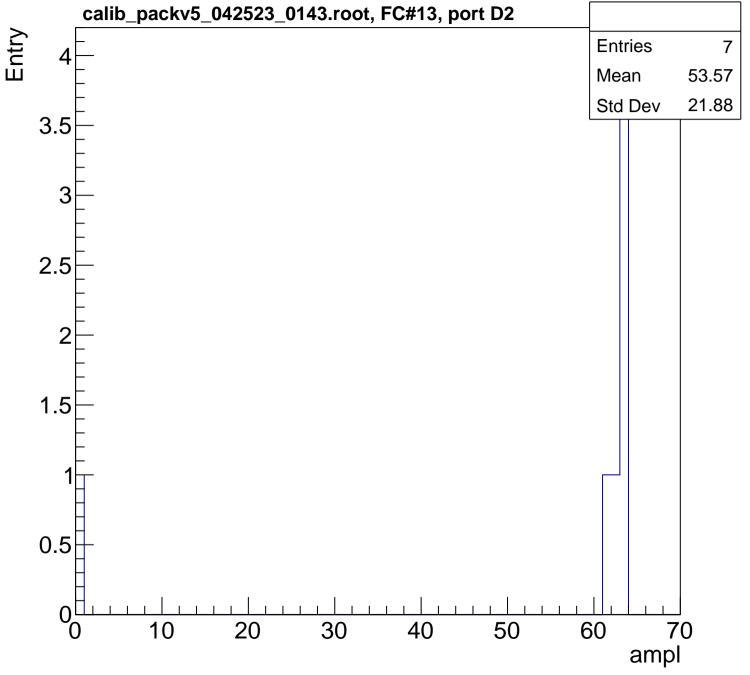












0

