



# B0L001S, U17-ch0, adc0

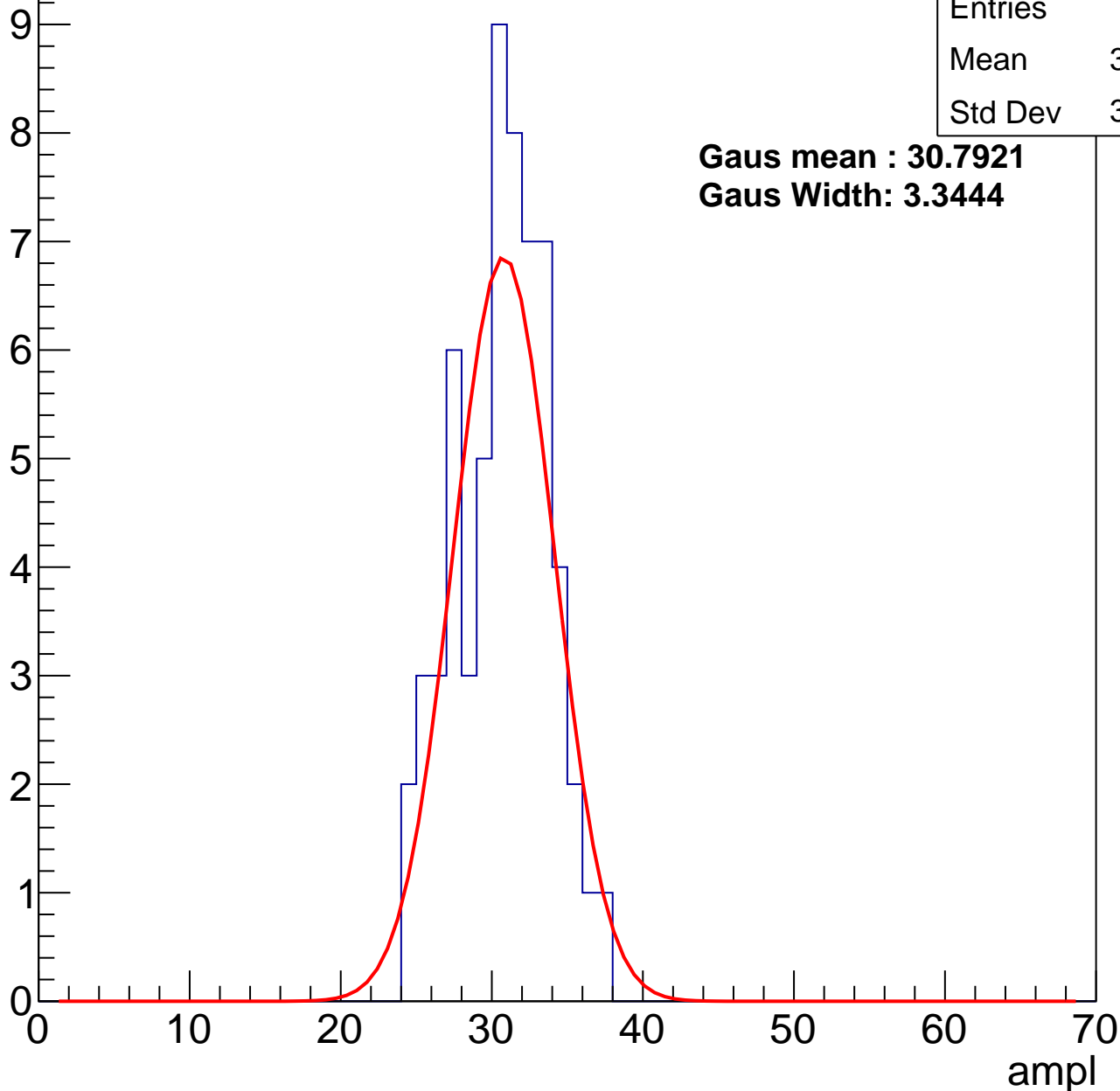
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	30.23
Std Dev	3.032

**Gaus mean : 30.7921**

**Gaus Width: 3.3444**



# B0L001S, U17-ch0, adc1

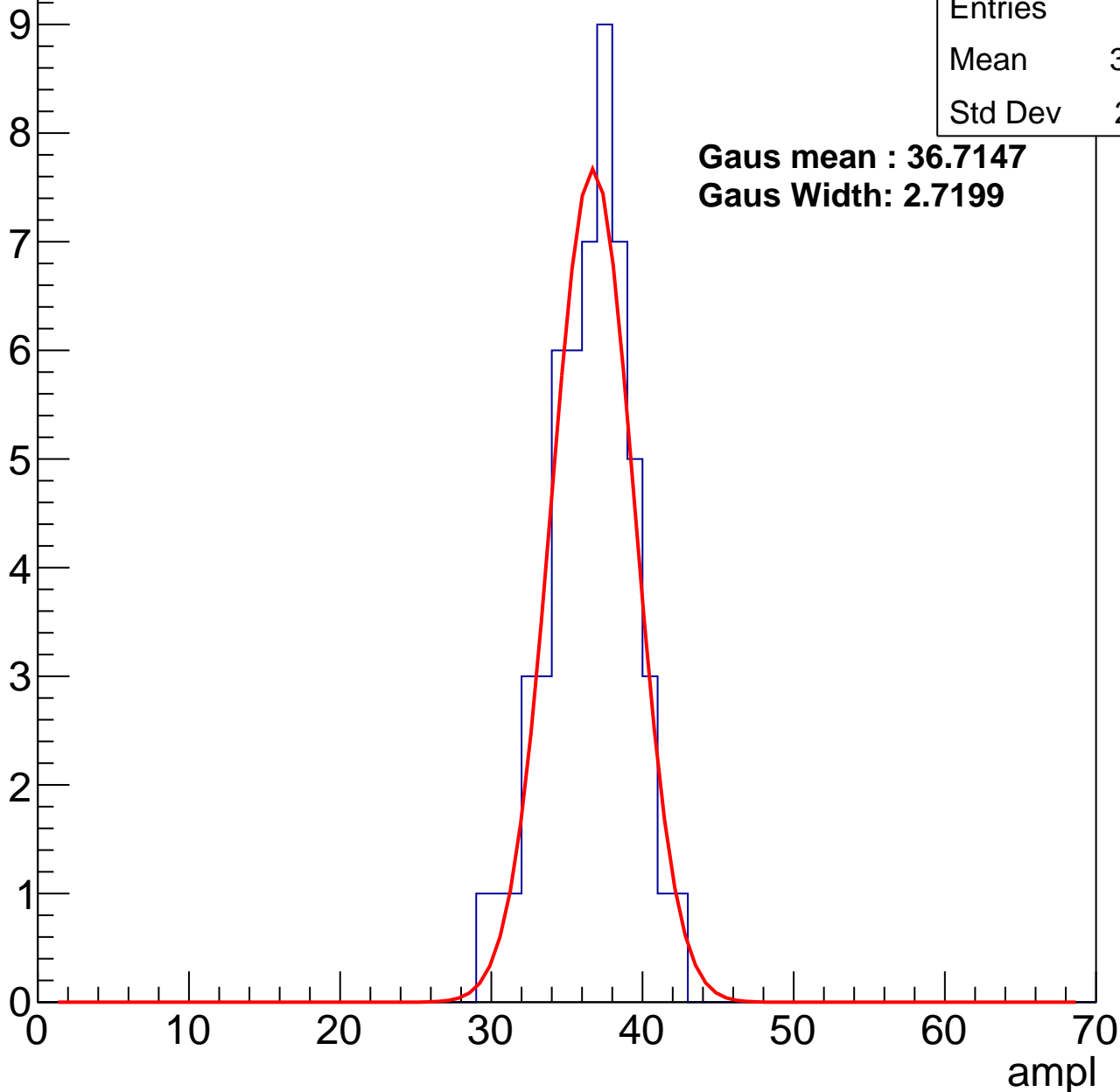
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	36.07
Std Dev	2.741

**Gaus mean : 36.7147**

**Gaus Width: 2.7199**



# B0L001S, U17-ch0, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

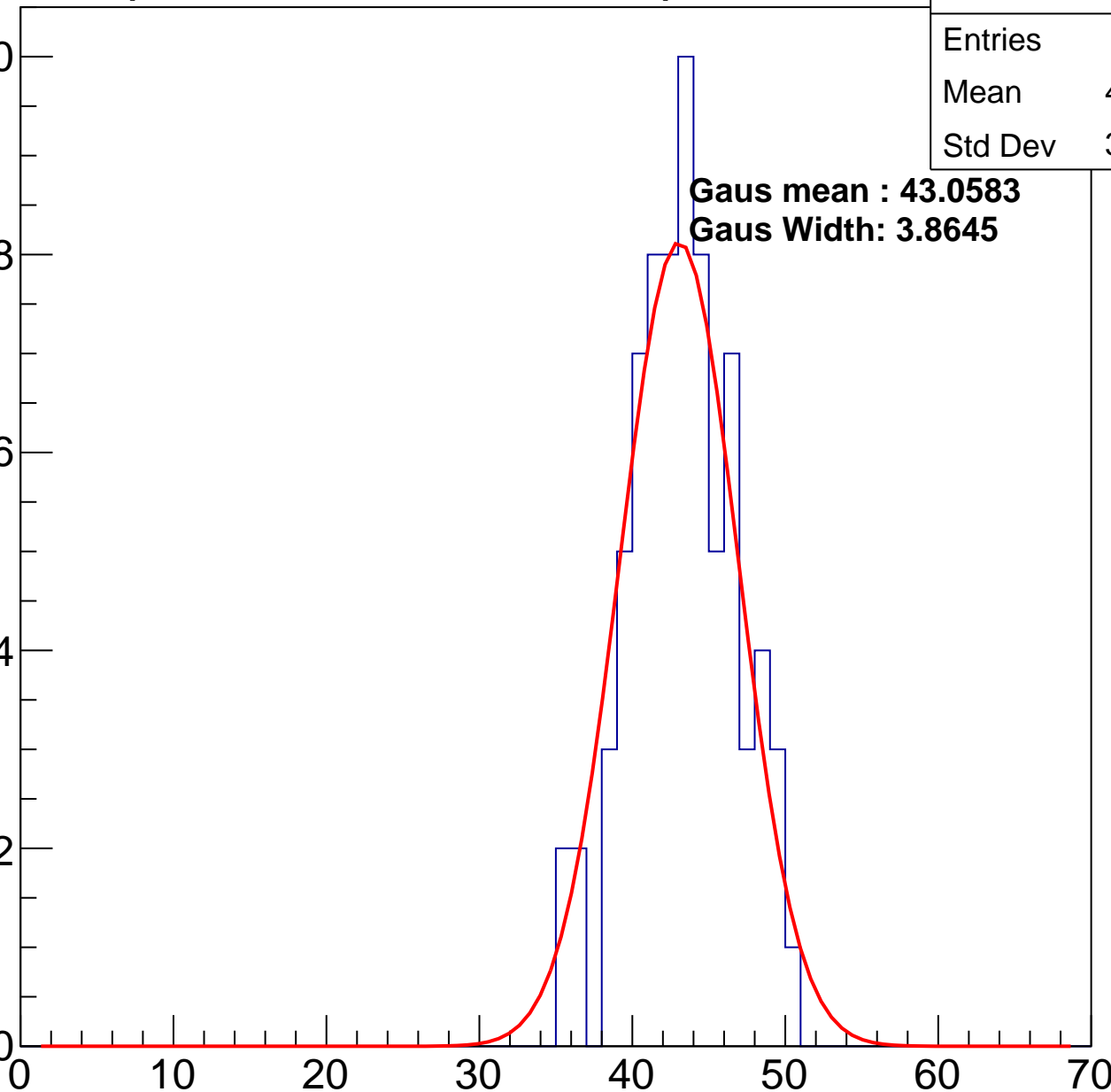
Entries	76
Mean	42.82
Std Dev	3.398

**Gaus mean : 43.0583**

**Gaus Width: 3.8645**

10  
8  
6  
4  
2  
0

ampl

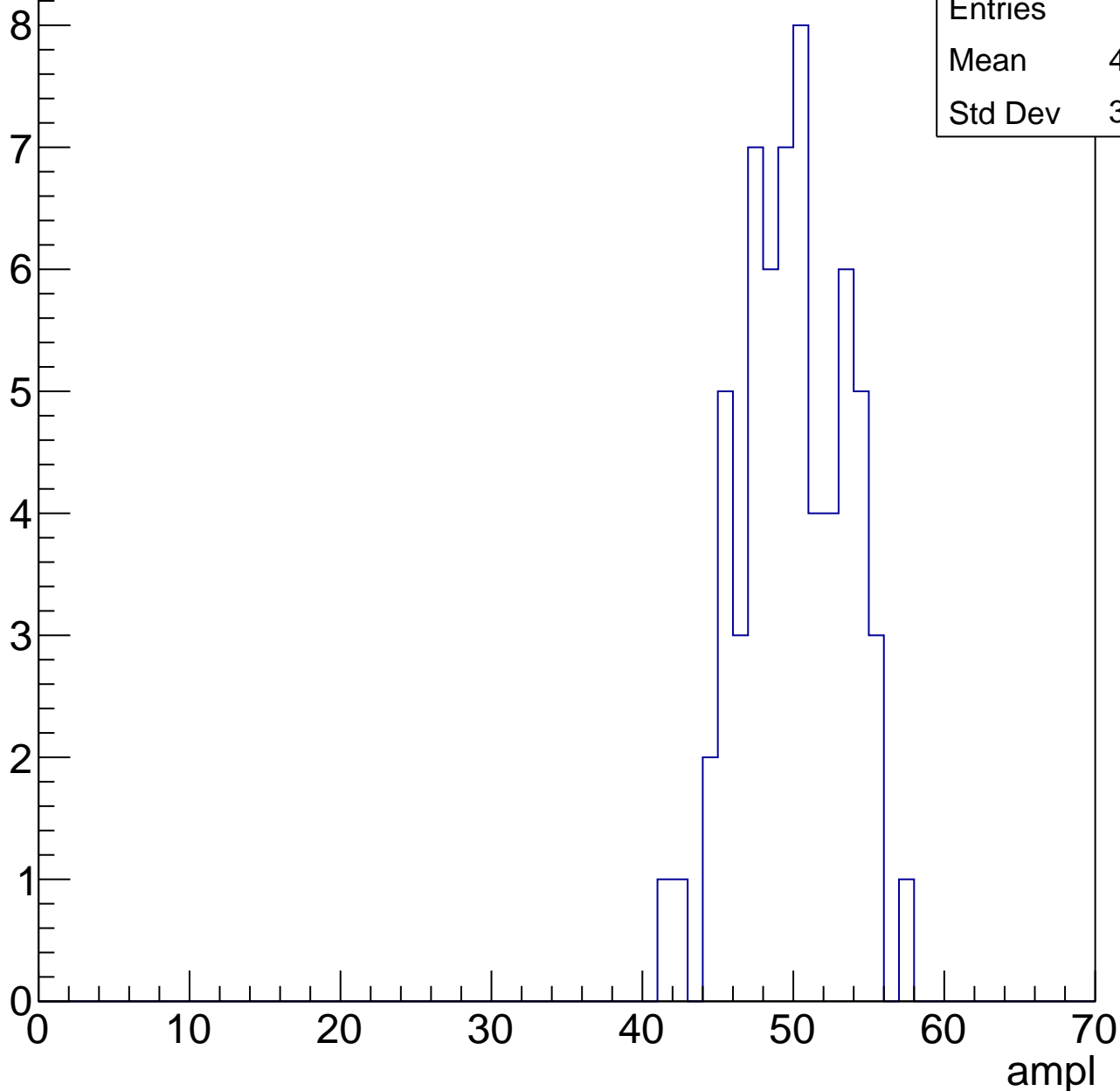


# B0L001S, U17-ch0, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	49.46
Std Dev	3.436

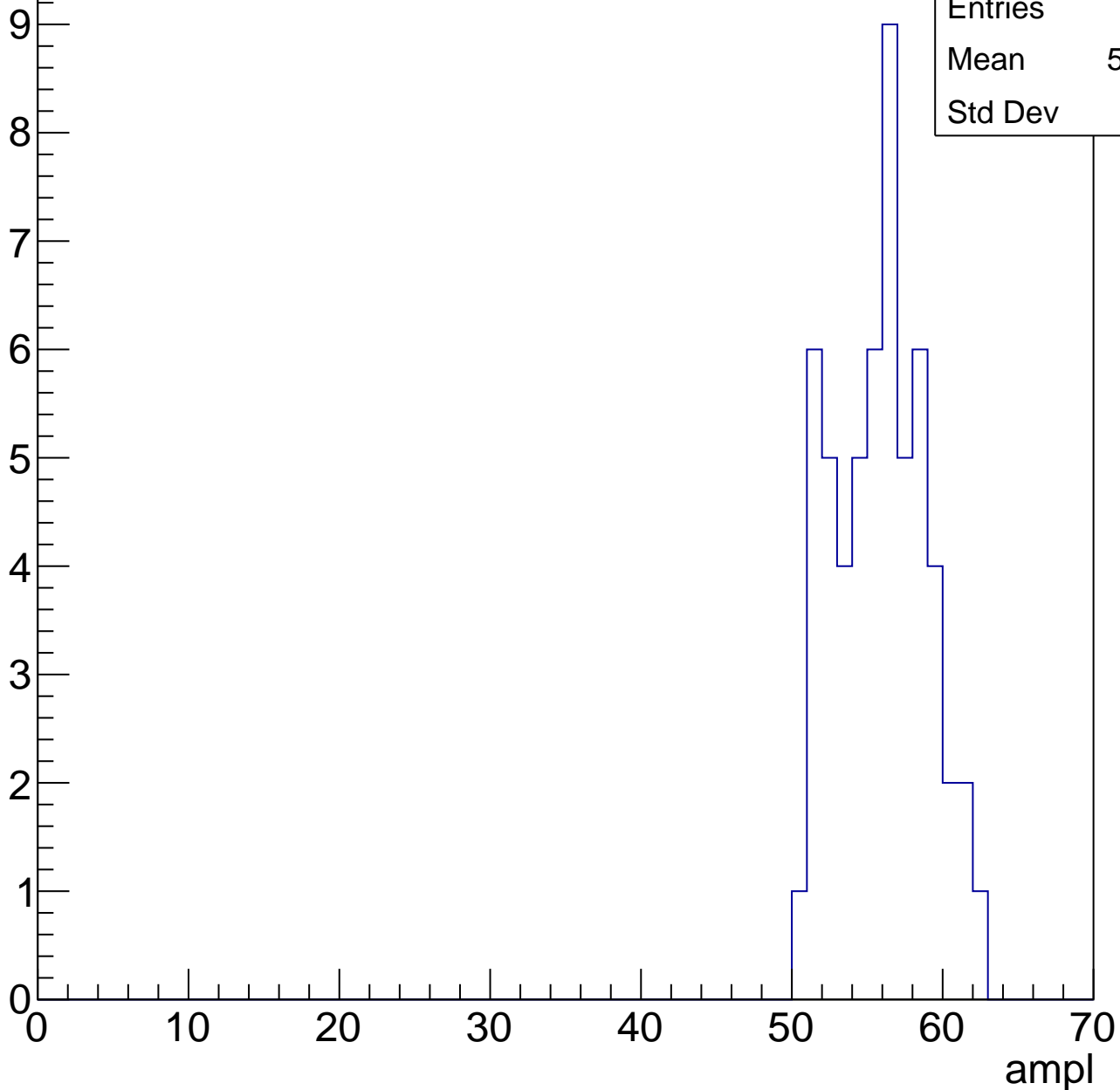


# B0L001S, U17-ch0, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	55.45
Std Dev	2.97

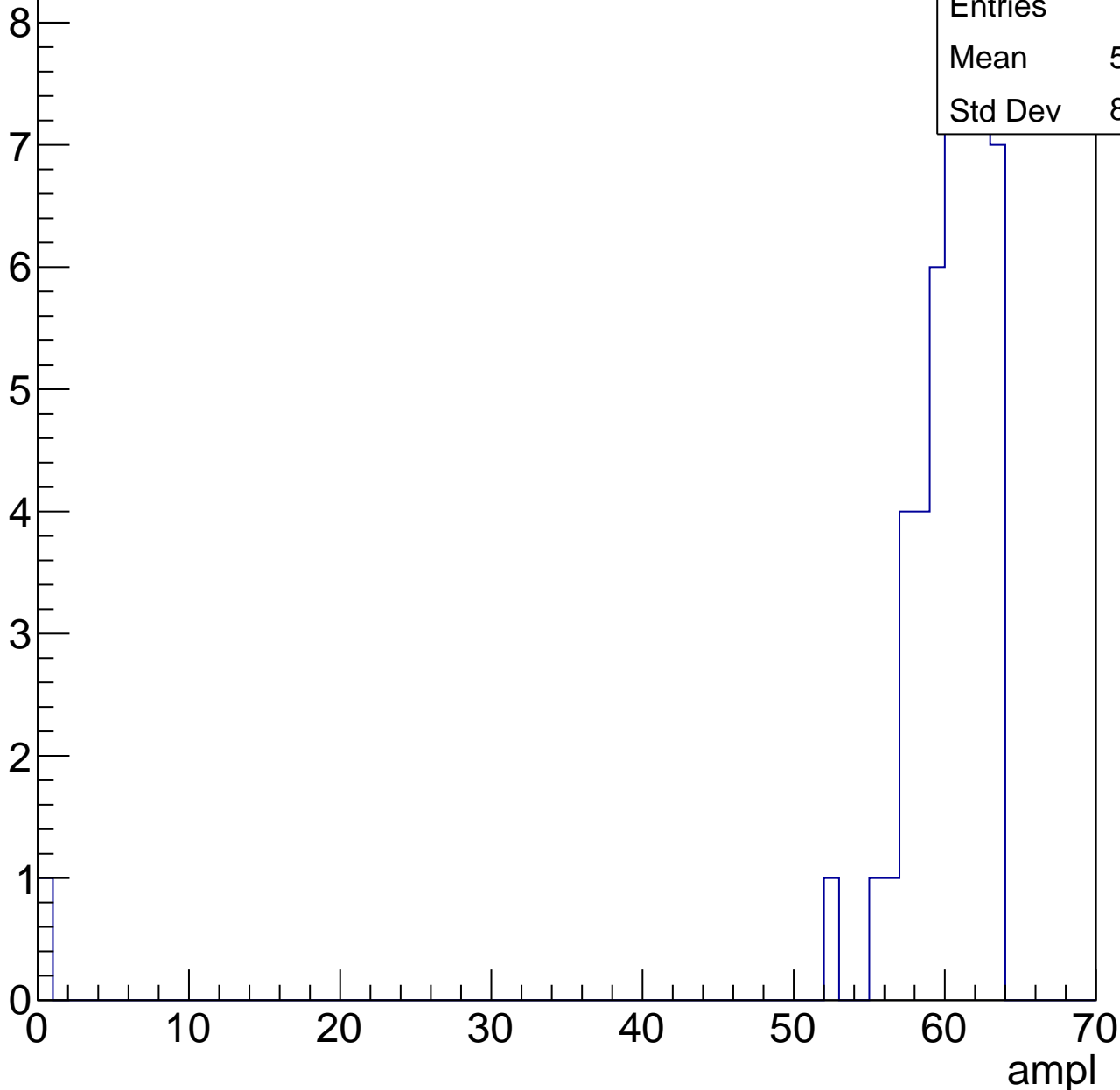


# B0L001S, U17-ch0, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

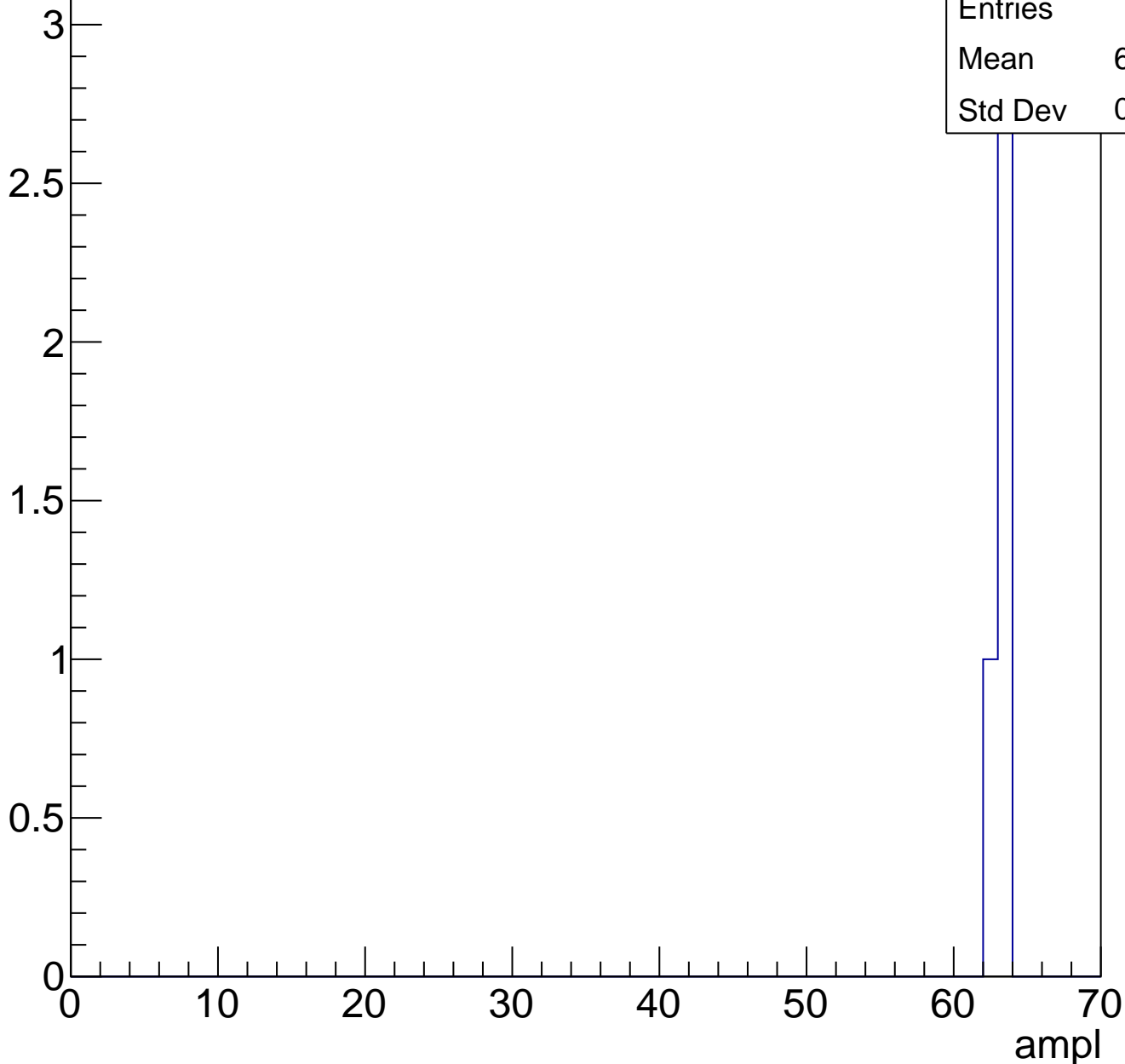
Entries	49
Mean	58.82
Std Dev	8.803



# B0L001S, U17-ch0, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

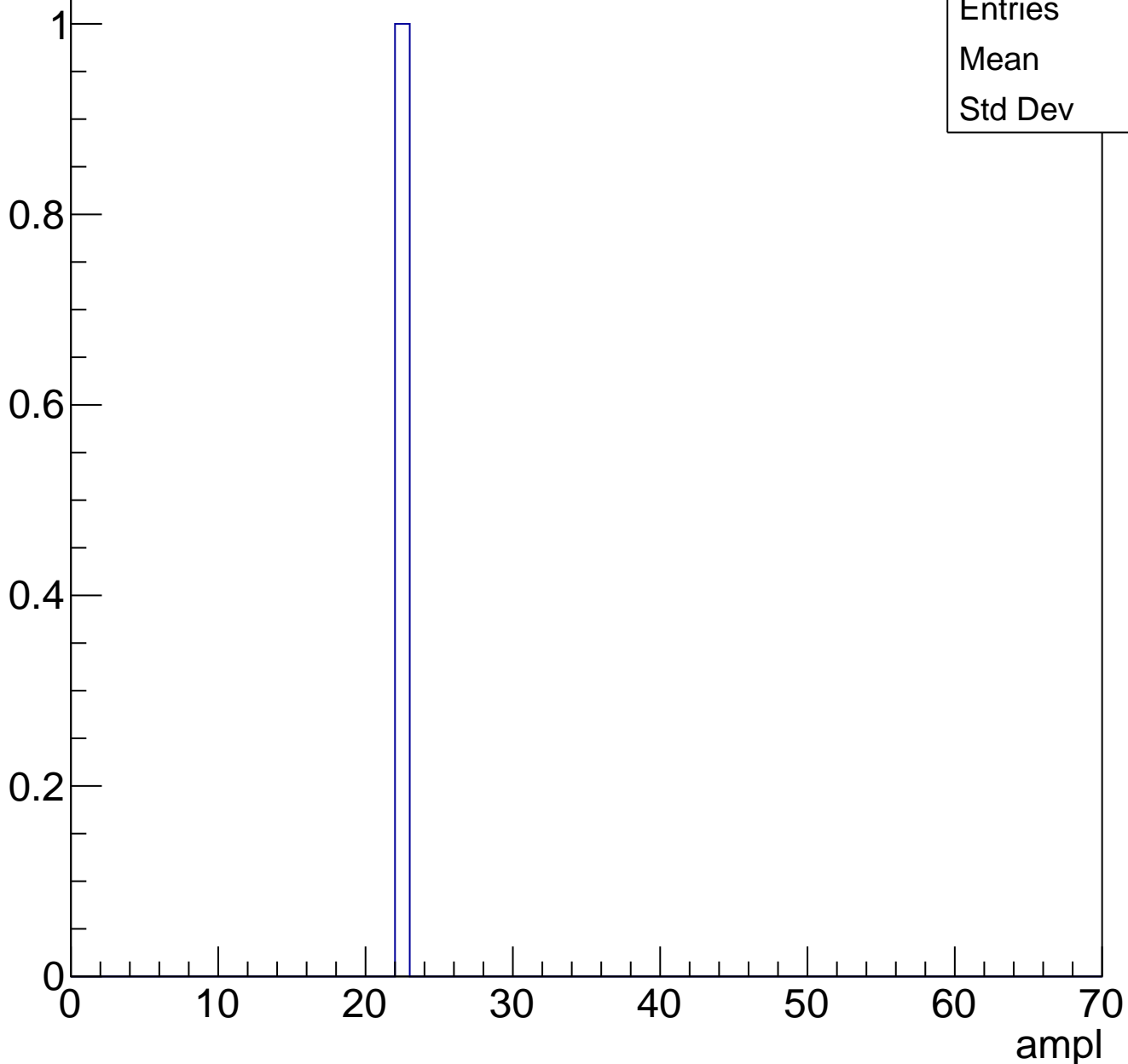




# B0L001S, U17-ch0, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	22
Std Dev	0

# B0L001S, U17-ch1, adc0

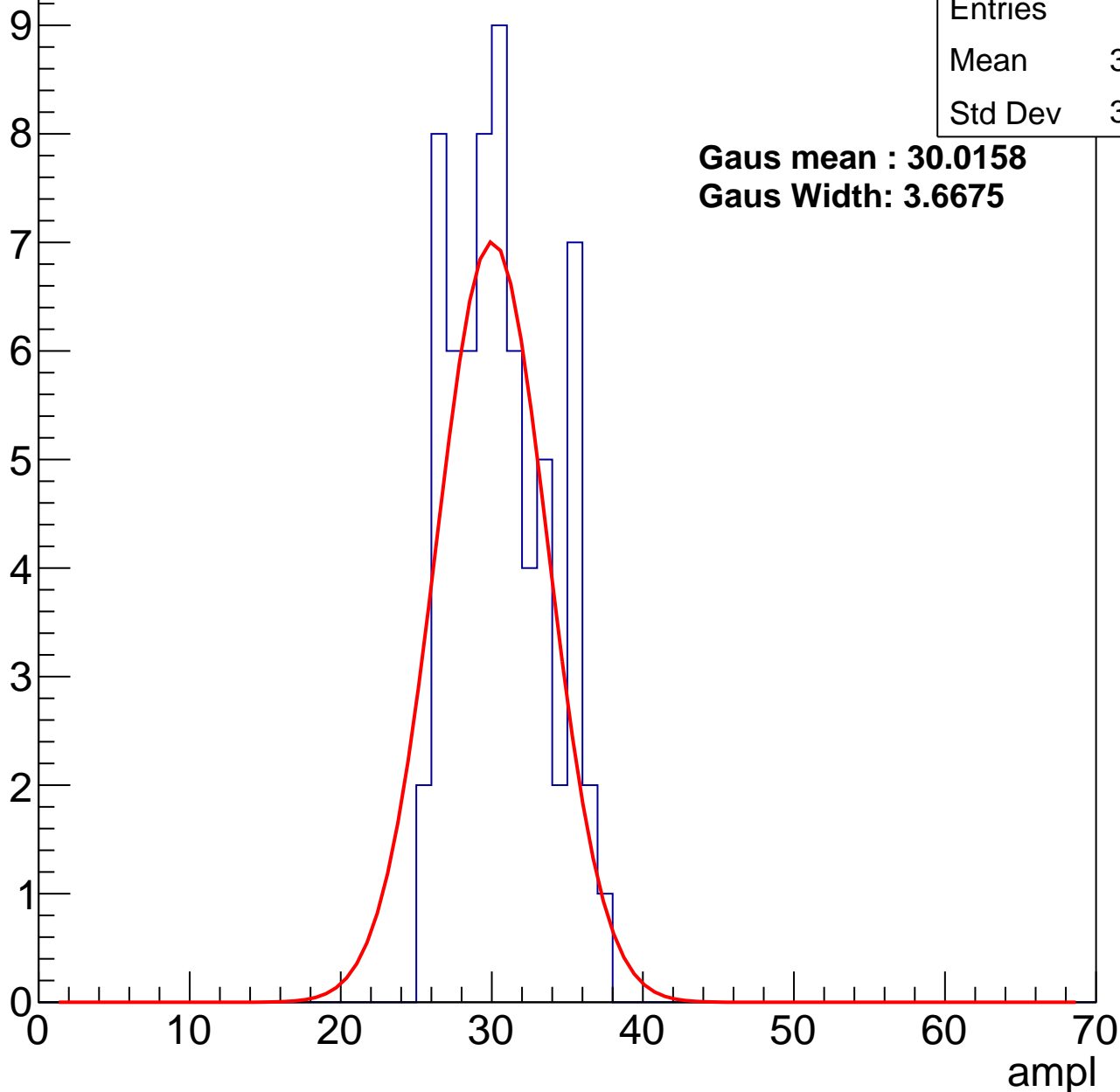
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	30.17
Std Dev	3.155

**Gaus mean : 30.0158**

**Gaus Width: 3.6675**



# B0L001S, U17-ch1, adc1

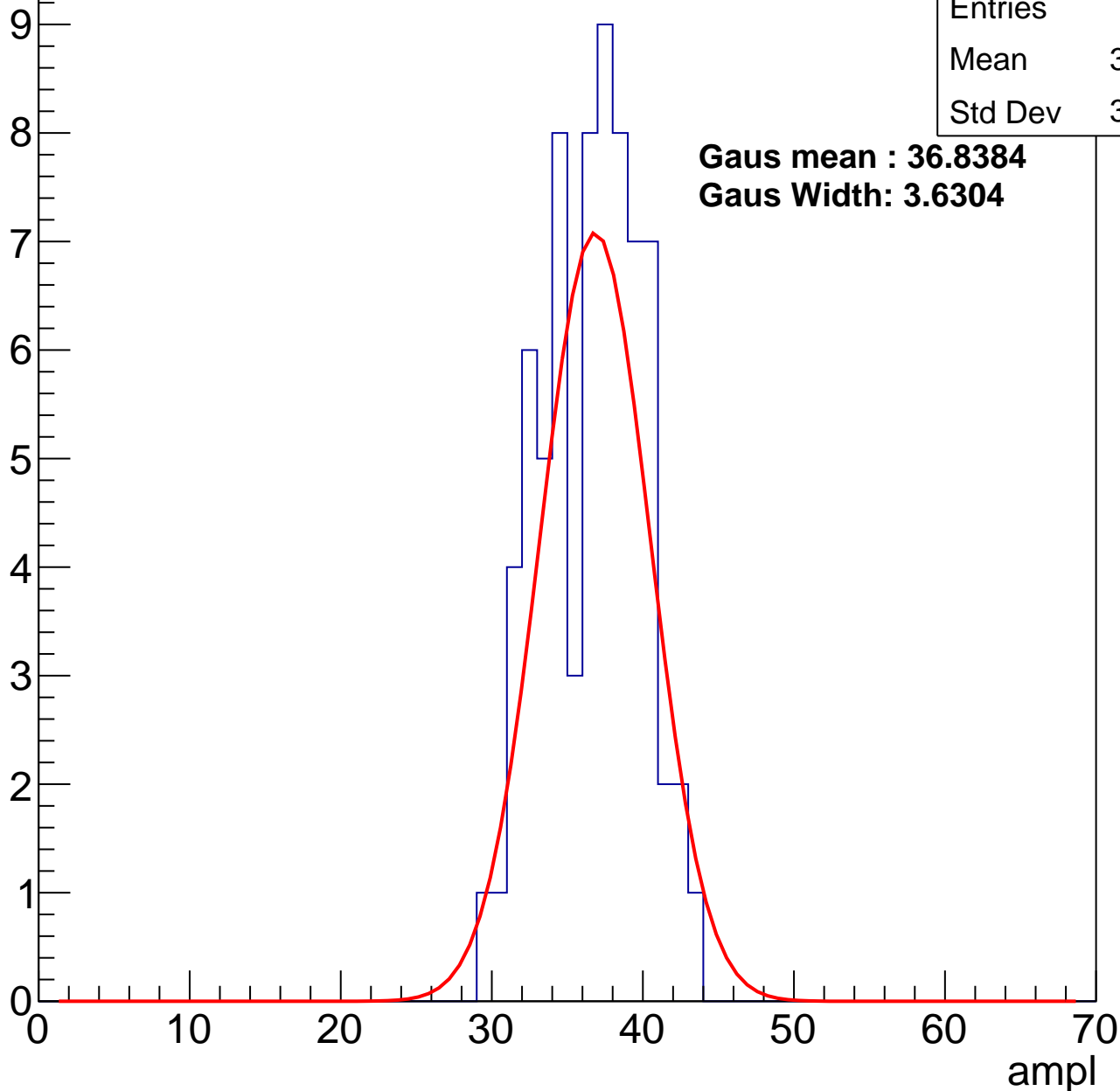
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	36.17
Std Dev	3.219

**Gaus mean : 36.8384**

**Gaus Width: 3.6304**



# B0L001S, U17-ch1, adc2

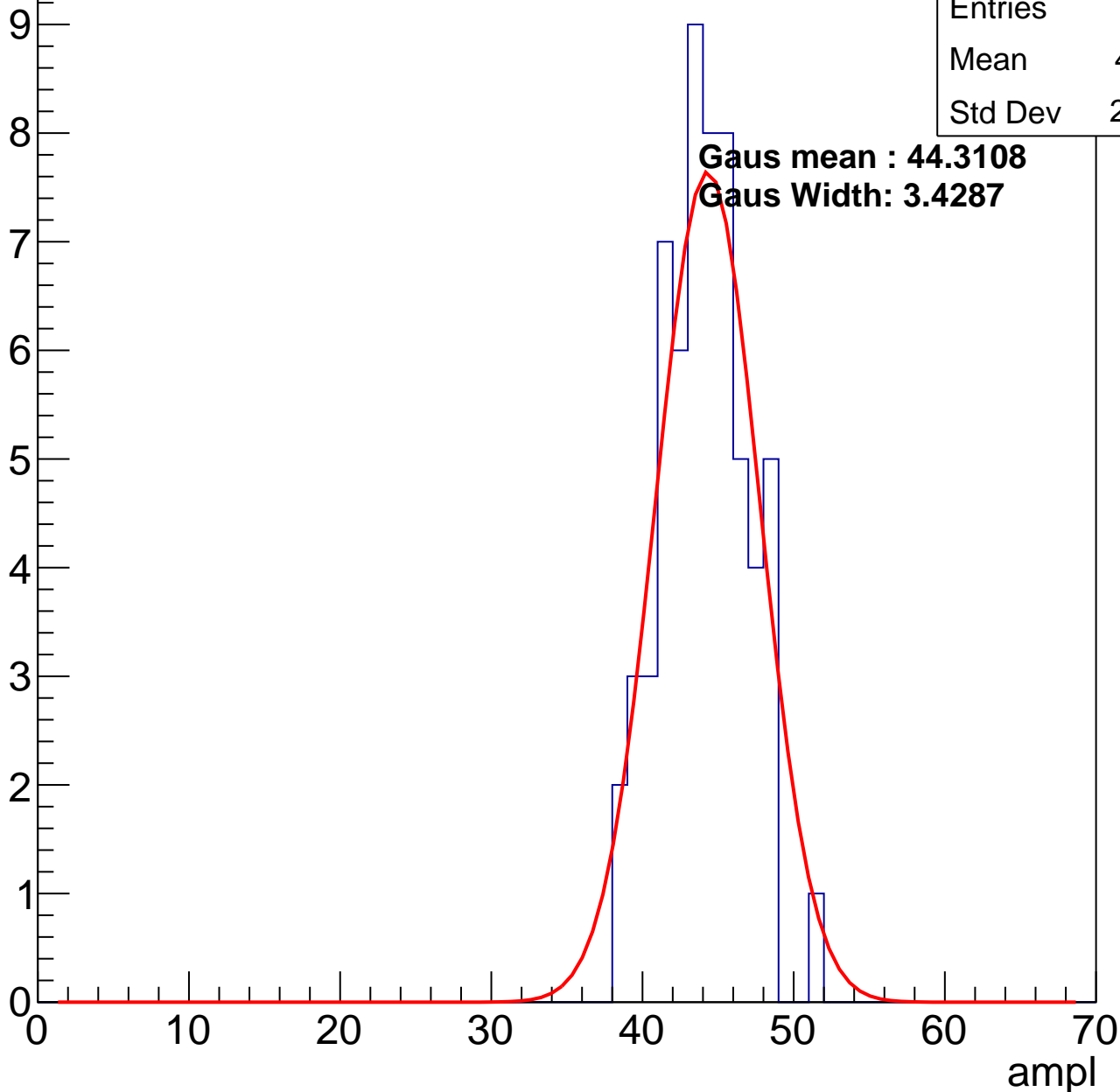
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	43.61
Std Dev	2.789

**Gaus mean : 44.3108**

**Gaus Width: 3.4287**

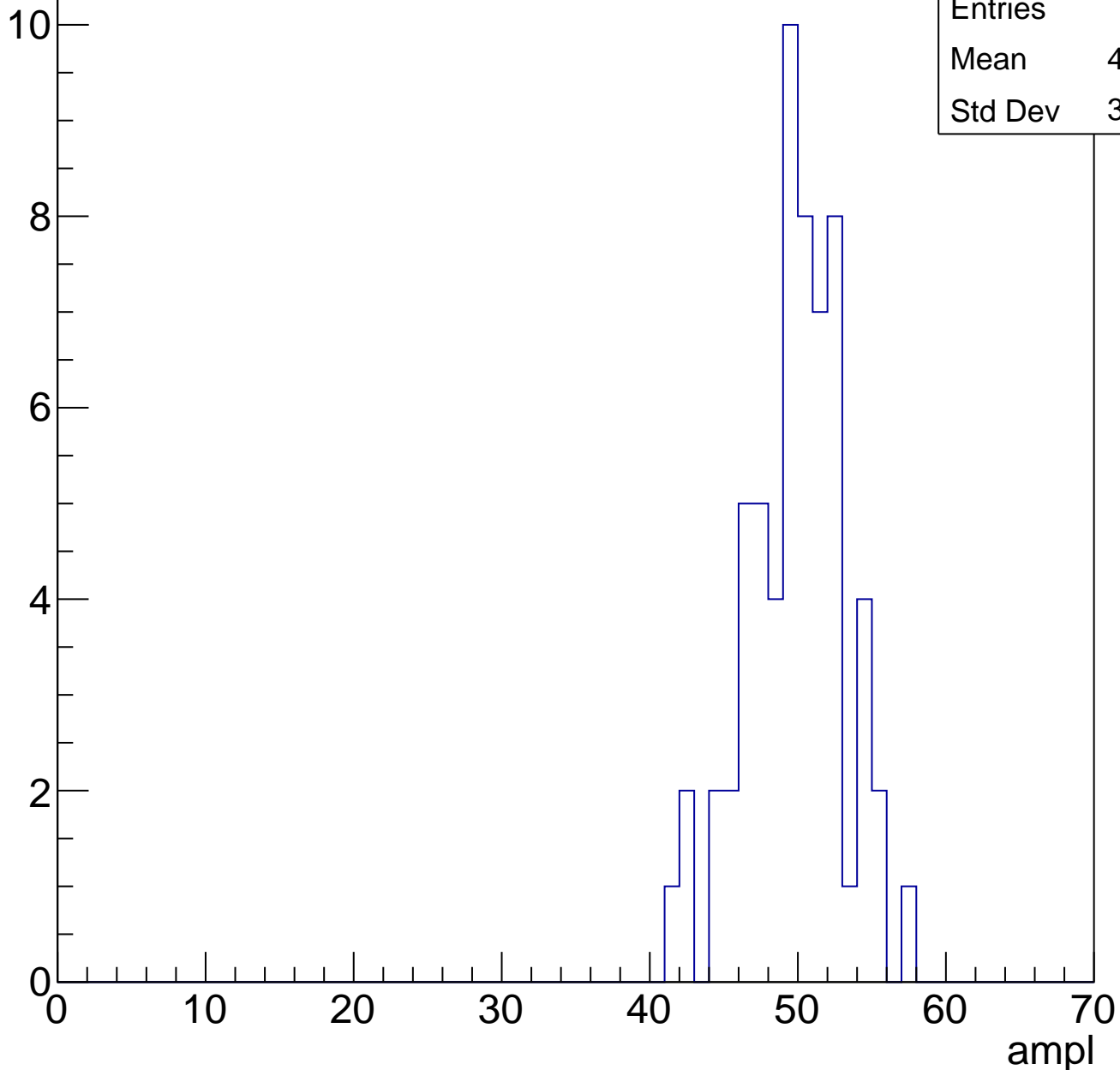


# B0L001S, U17-ch1, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	62
Mean	49.34
Std Dev	3.277

Entry

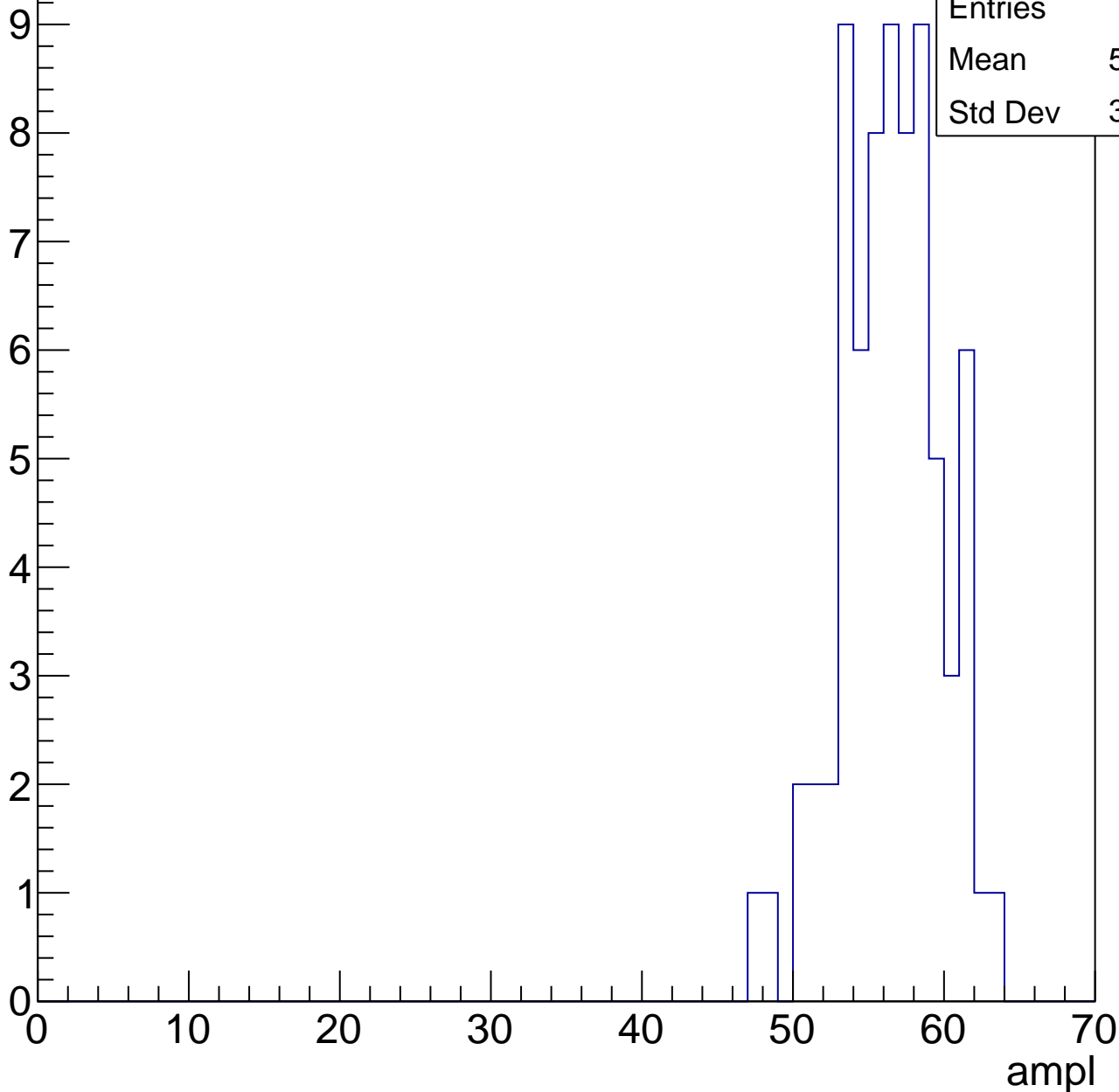


# B0L001S, U17-ch1, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	56.03
Std Dev	3.277

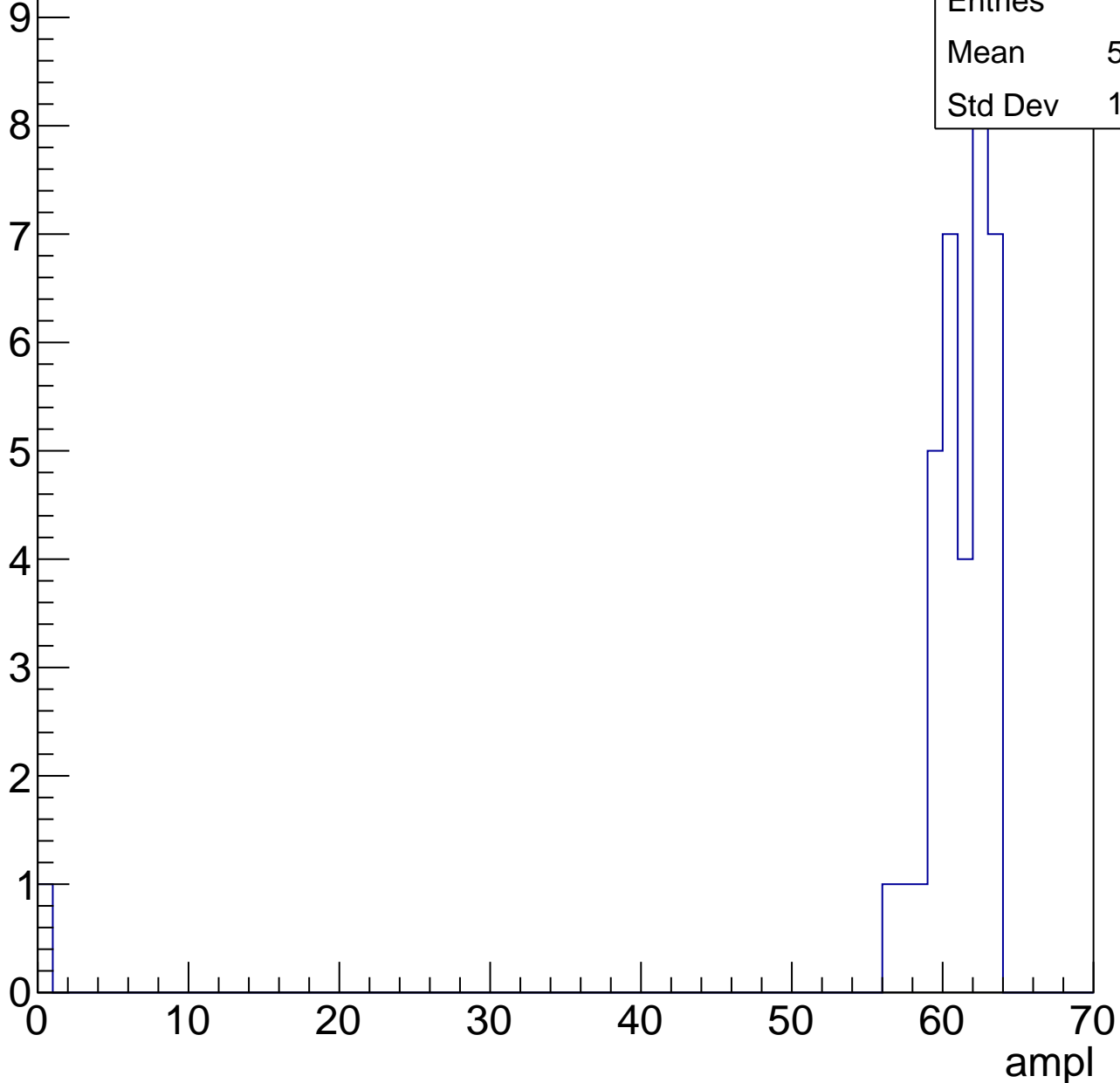


# B0L001S, U17-ch1, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	36
Mean	59.14
Std Dev	10.15



# B0L001S, U17-ch1, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch1, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U17-ch2, adc0

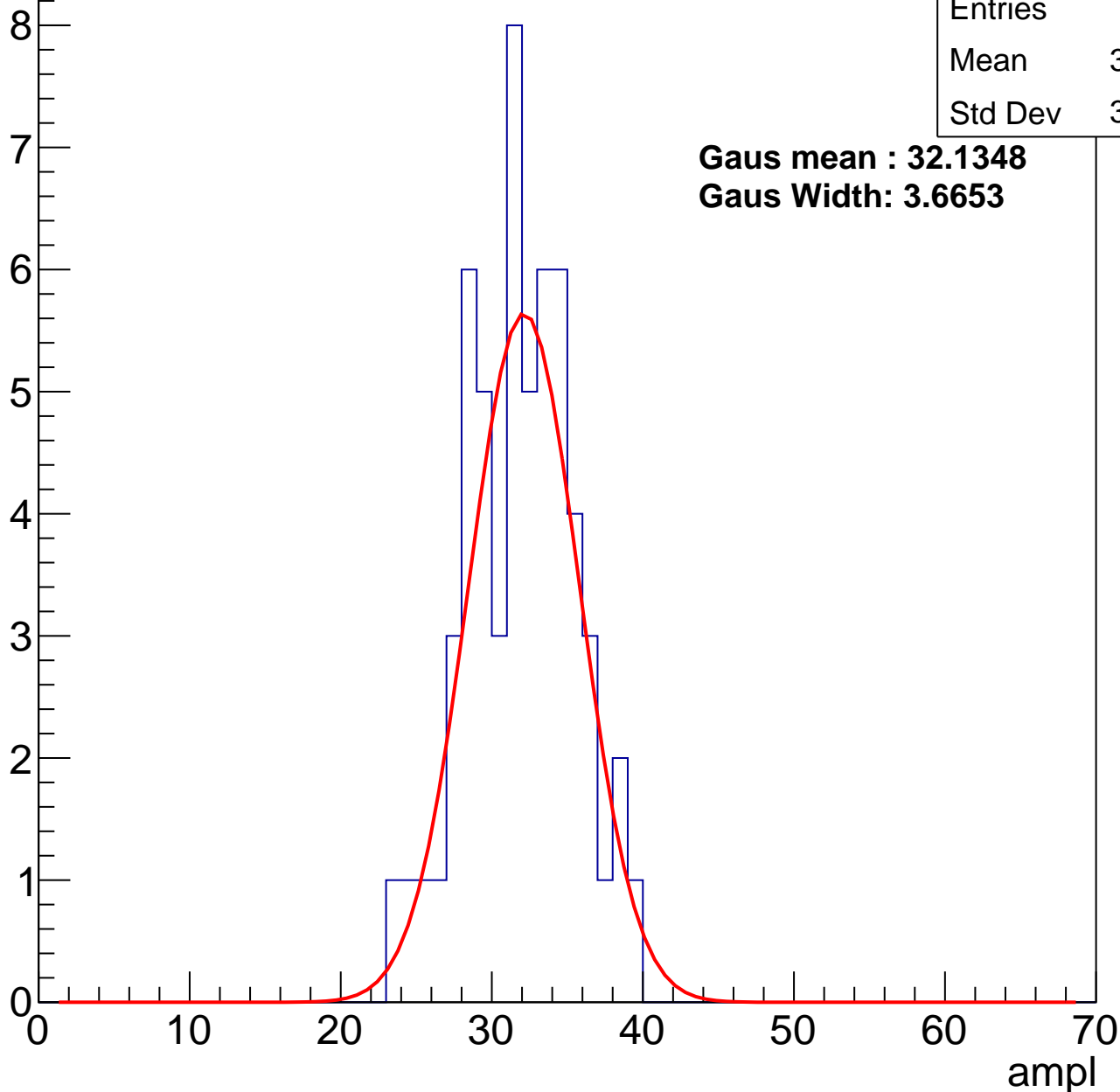
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	31.44
Std Dev	3.524

**Gaus mean : 32.1348**

**Gaus Width: 3.6653**



# B0L001S, U17-ch2, adc1

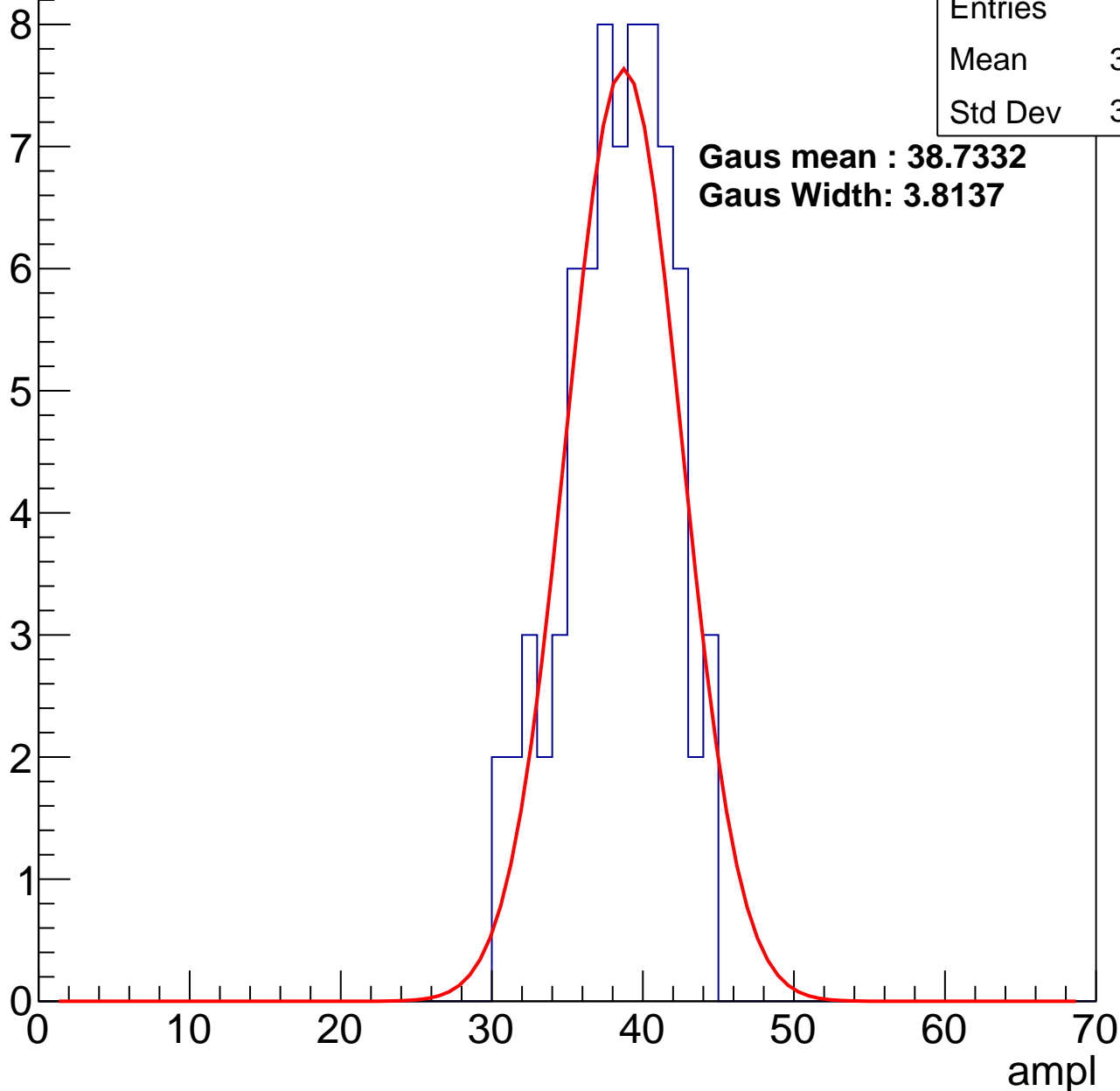
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	37.85
Std Dev	3.459

**Gaus mean : 38.7332**

**Gaus Width: 3.8137**



# B0L001S, U17-ch2, adc2

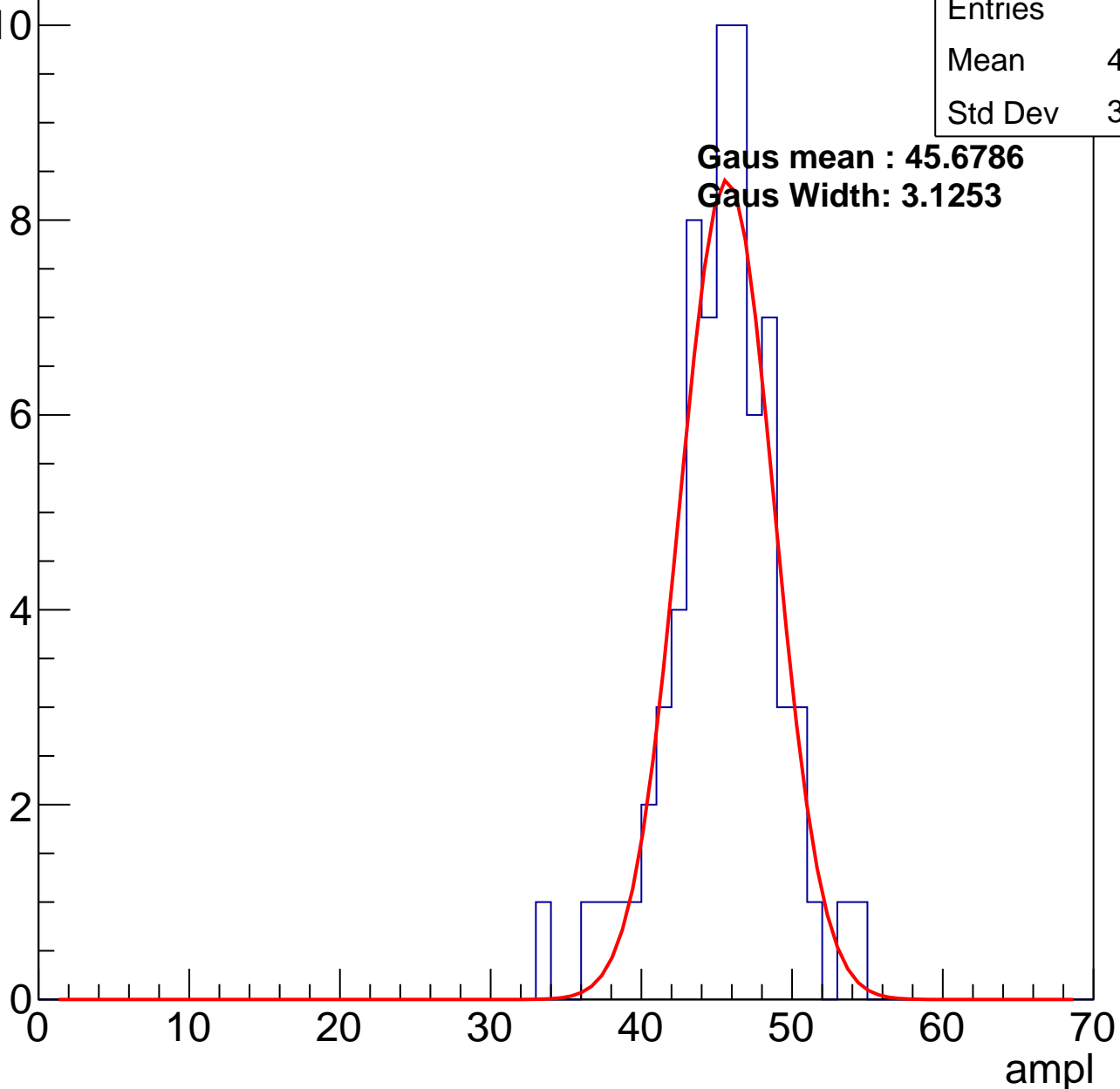
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	44.92
Std Dev	3.653

**Gaus mean : 45.6786**

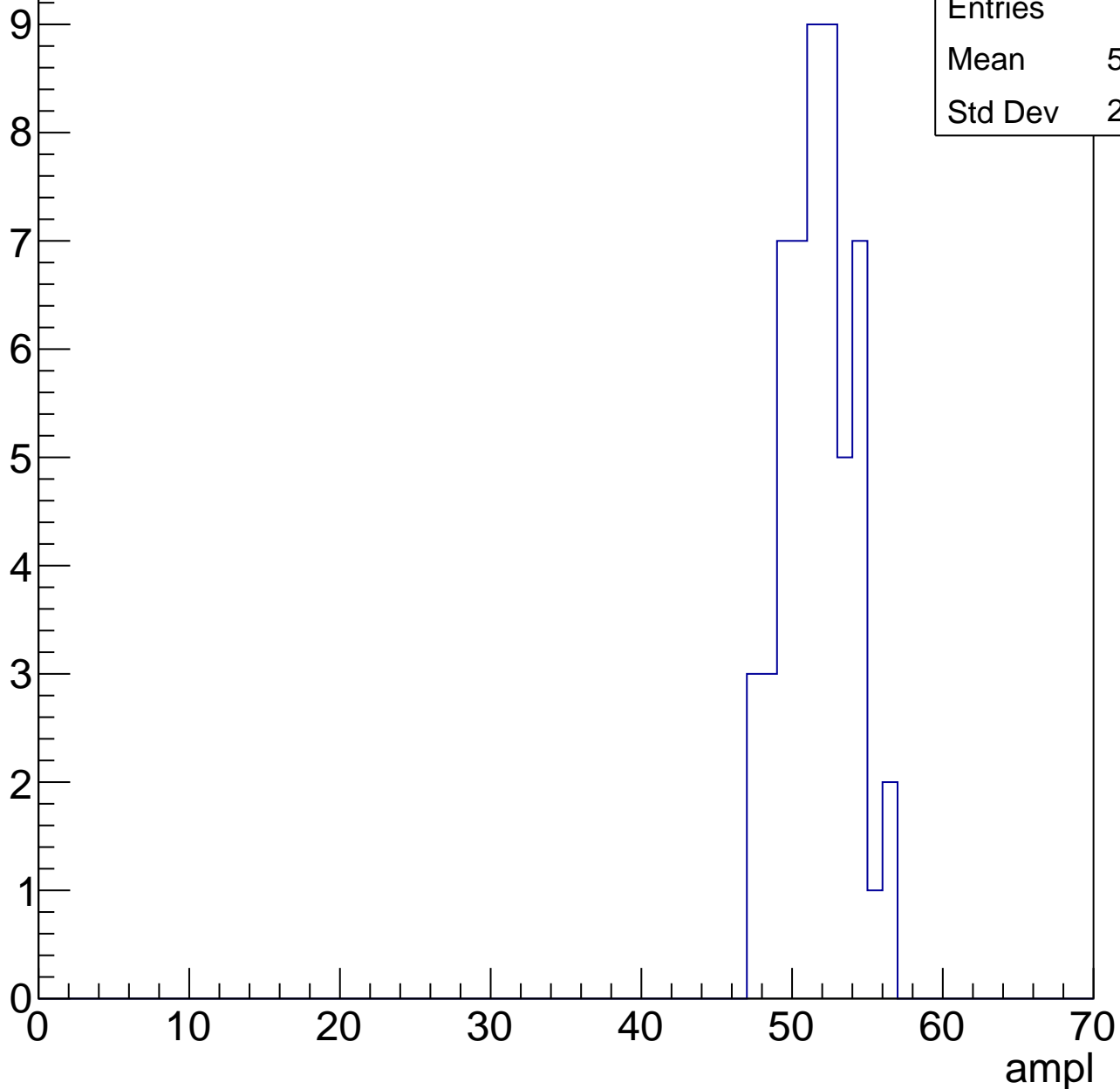
**Gaus Width: 3.1253**



# B0L001S, U17-ch2, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



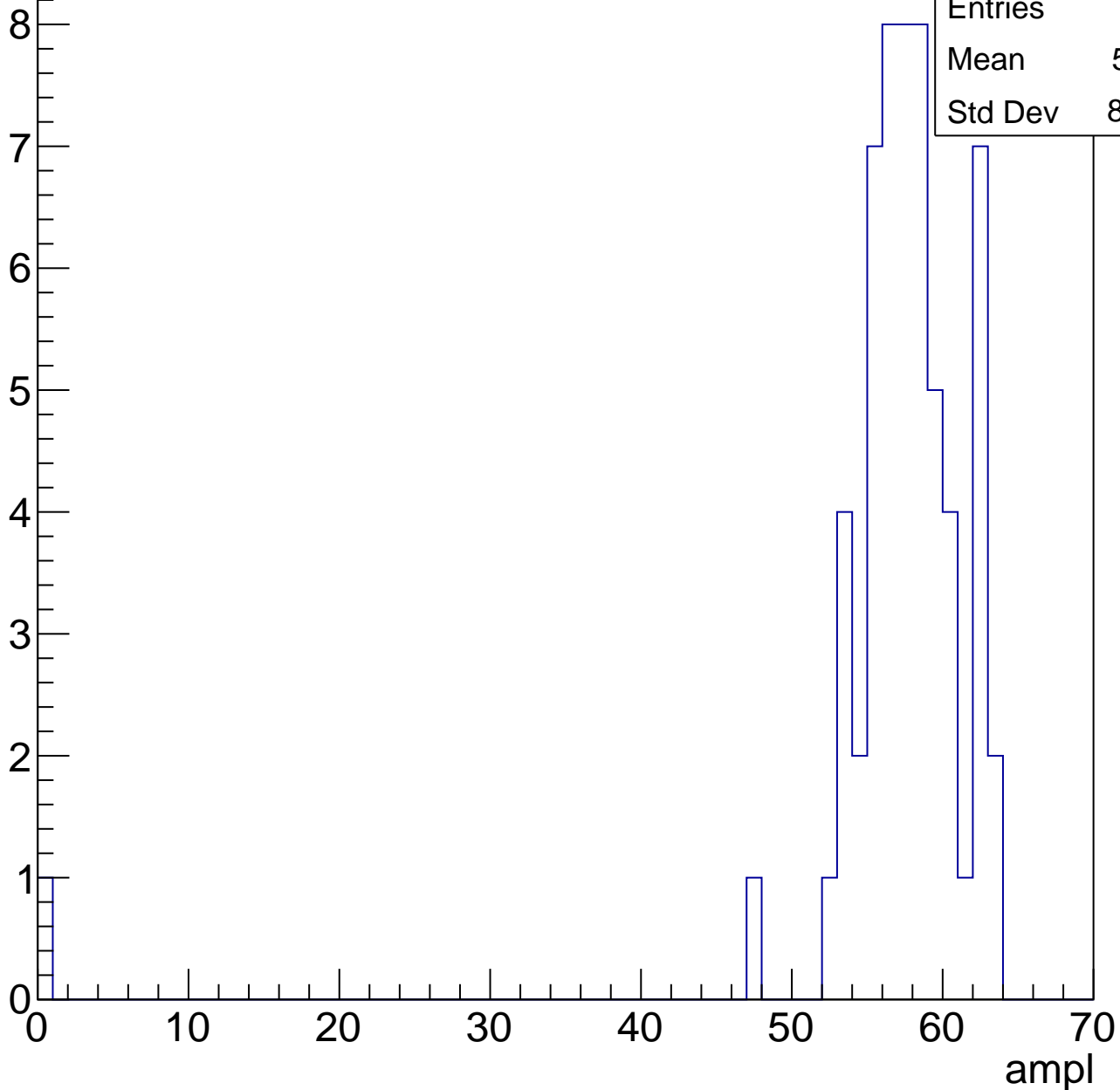
Entries	53
Mean	51.23
Std Dev	2.237

# B0L001S, U17-ch2, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

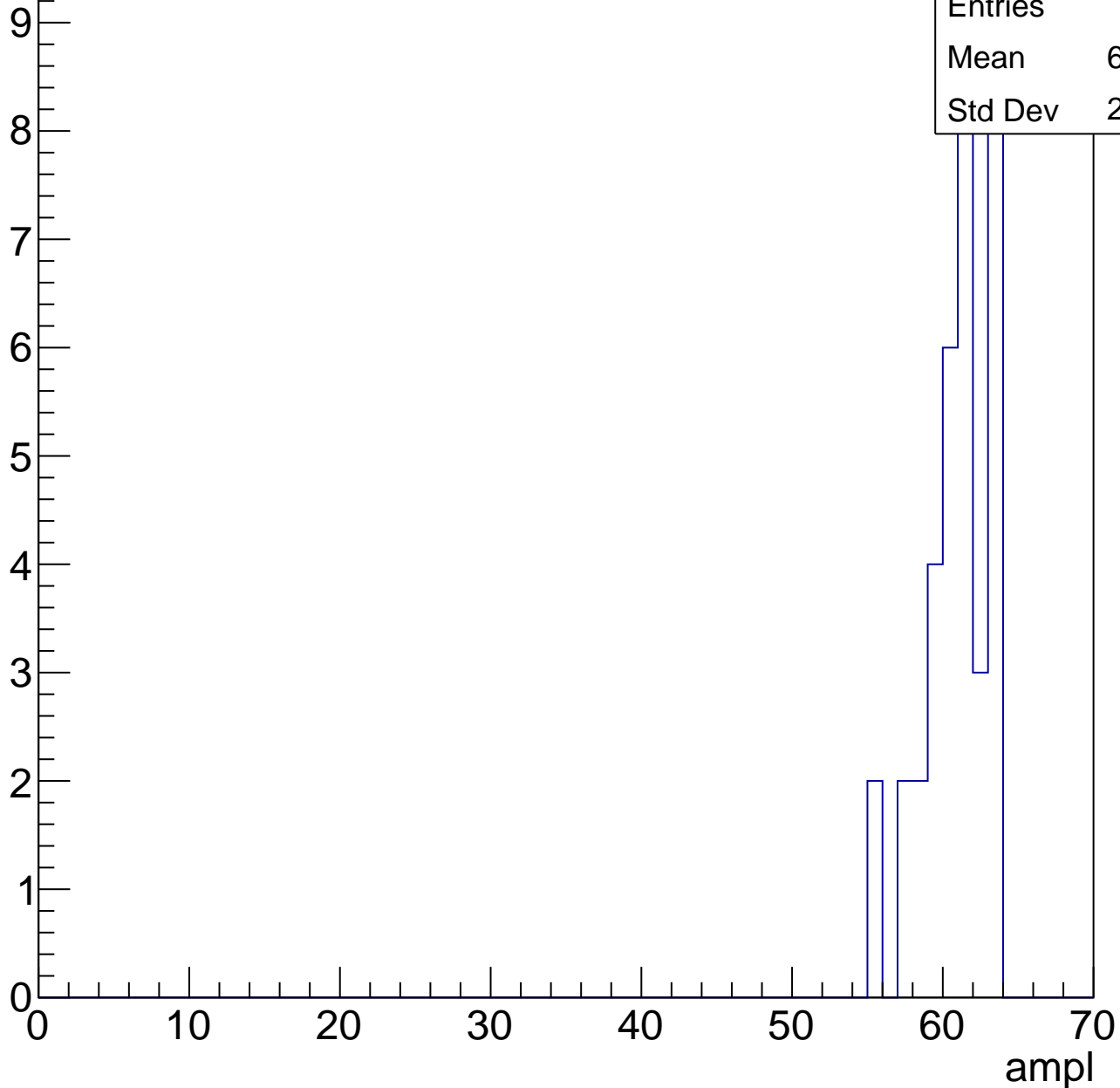
Entries	59
Mean	56.41
Std Dev	8.024



# B0L001S, U17-ch2, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

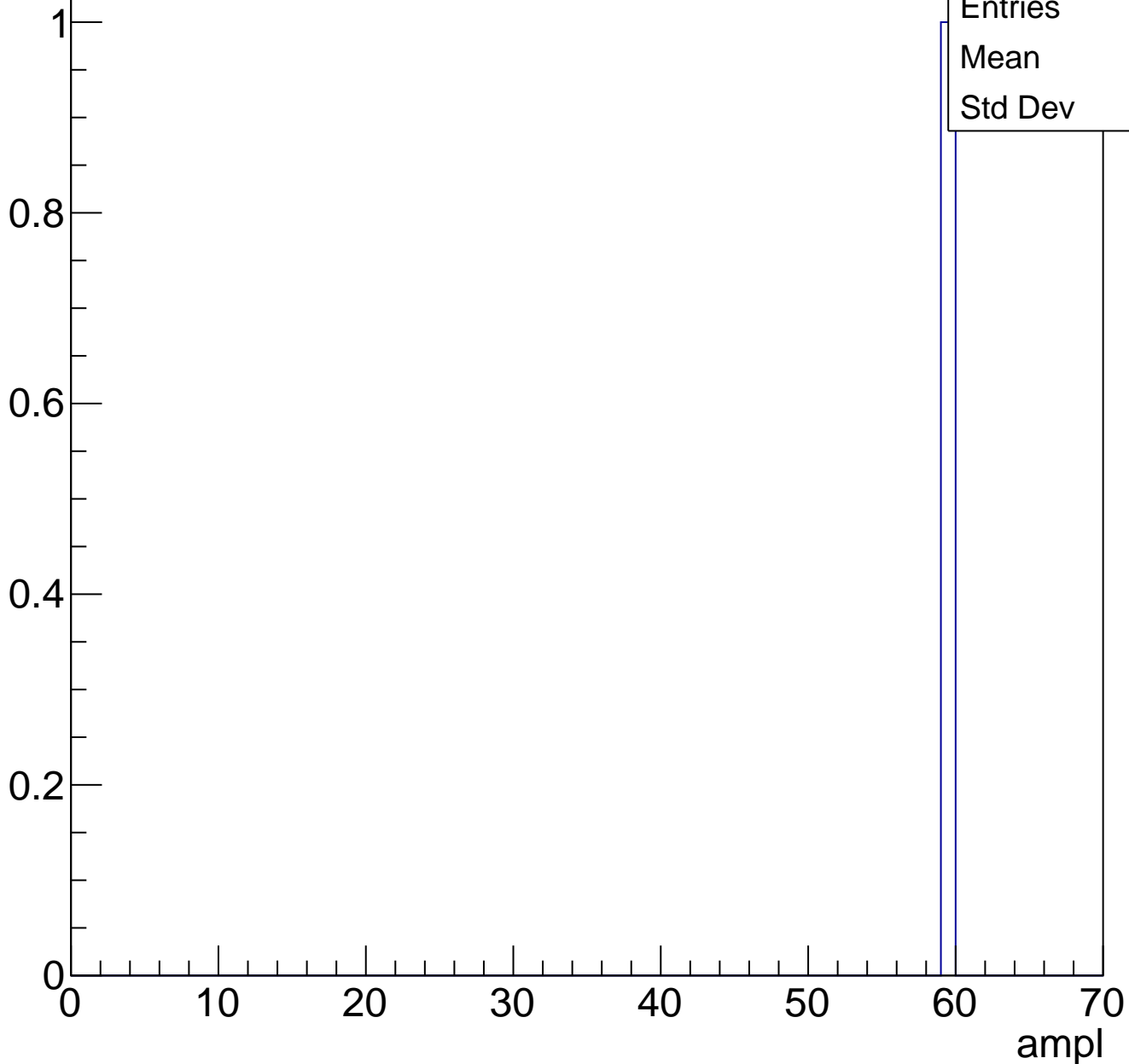
Entry



# B0L001S, U17-ch2, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch2, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U17-ch3, adc0

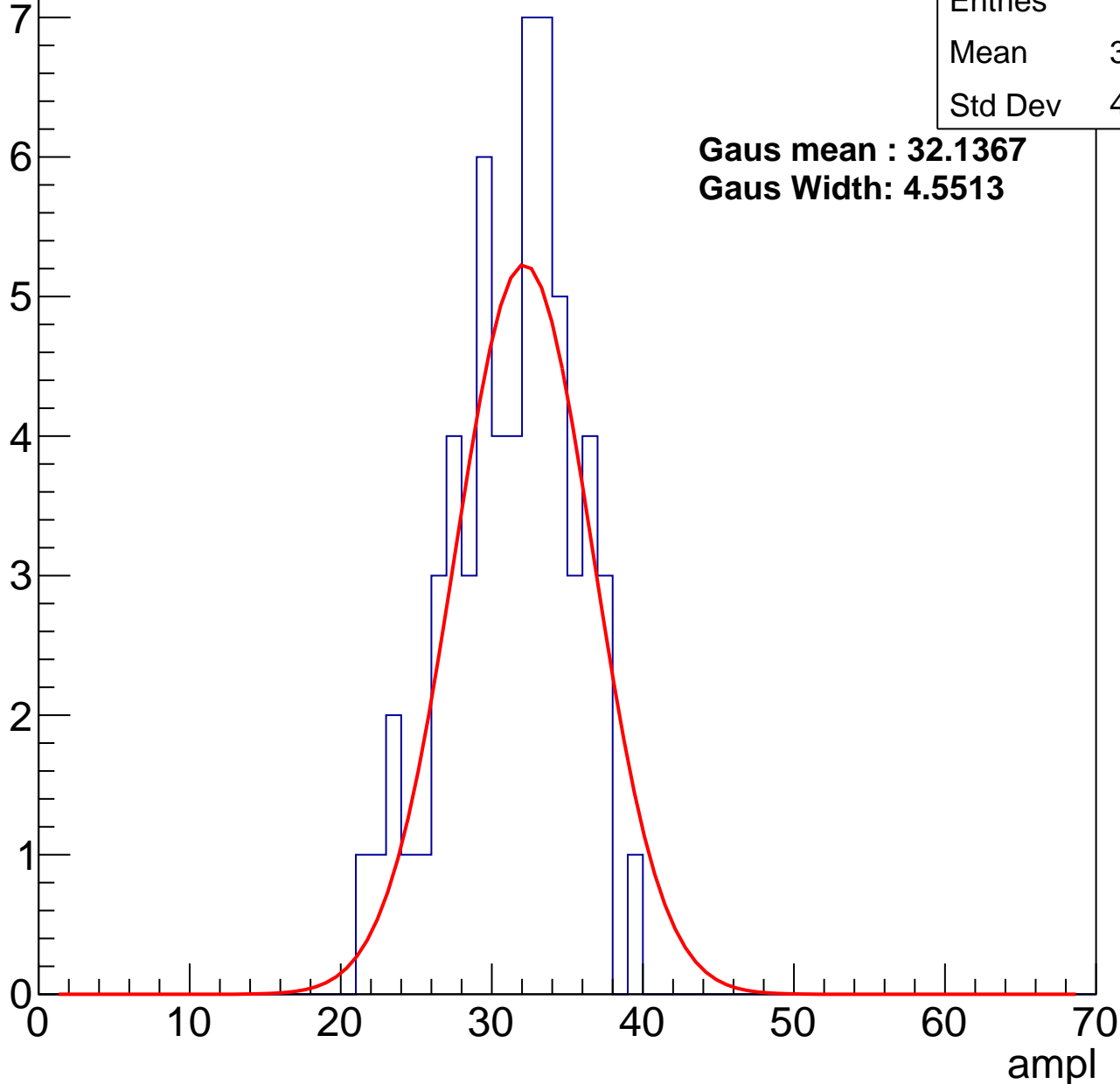
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	30.83
Std Dev	4.054

**Gaus mean : 32.1367**

**Gaus Width: 4.5513**



# B0L001S, U17-ch3, adc1

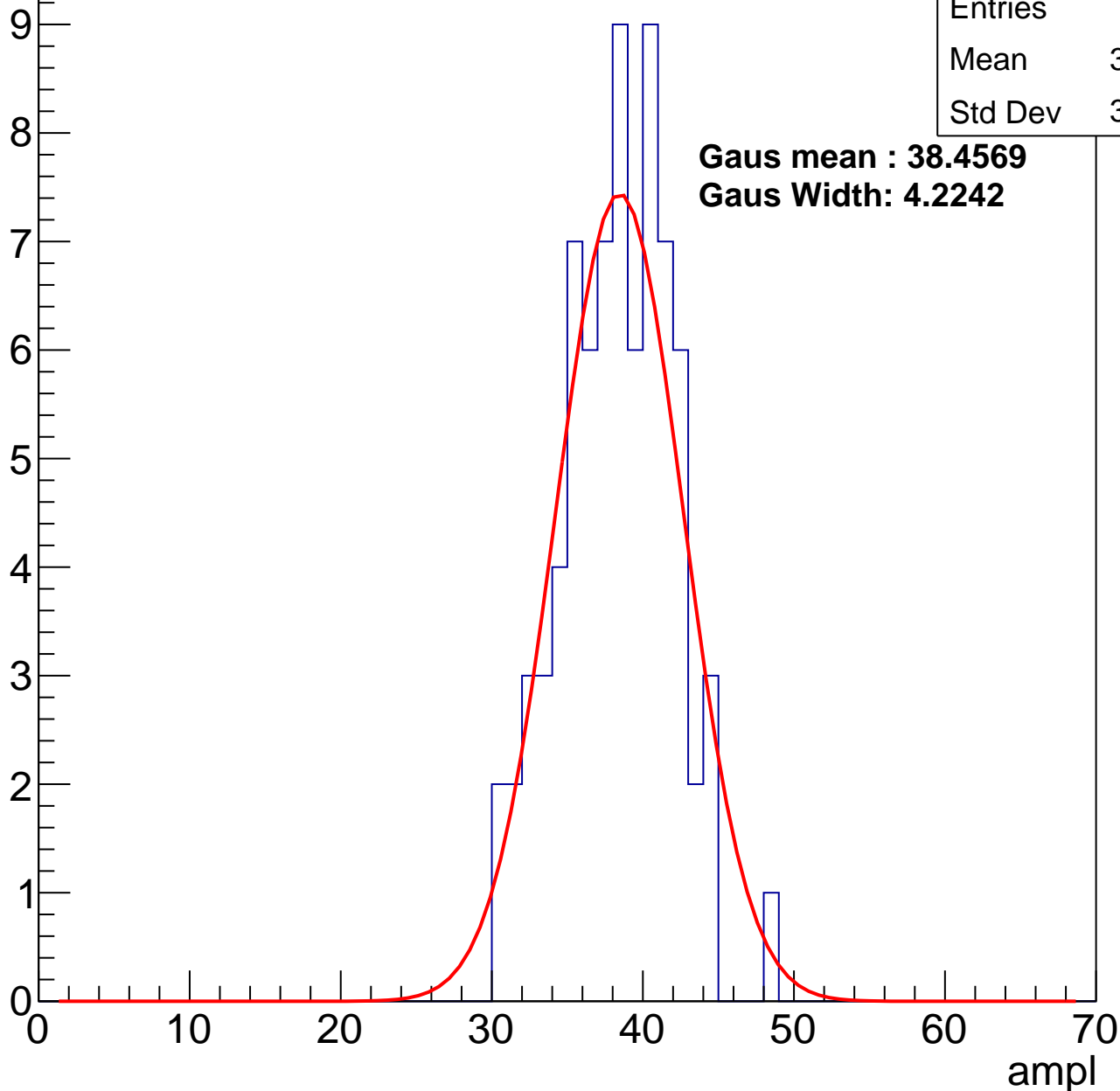
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	77
Mean	37.84
Std Dev	3.647

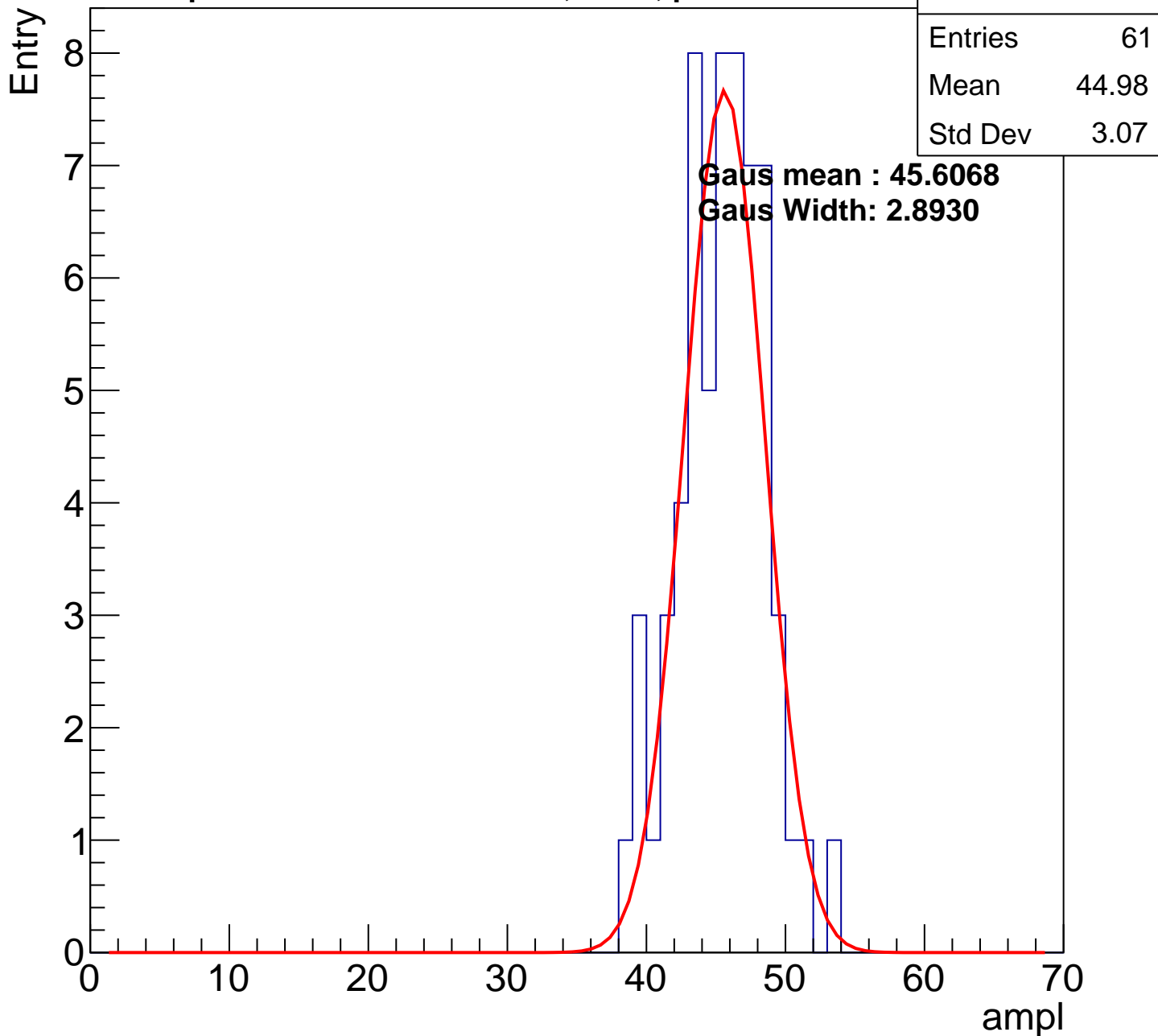
**Gaus mean : 38.4569**

**Gaus Width: 4.2242**



# B0L001S, U17-ch3, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

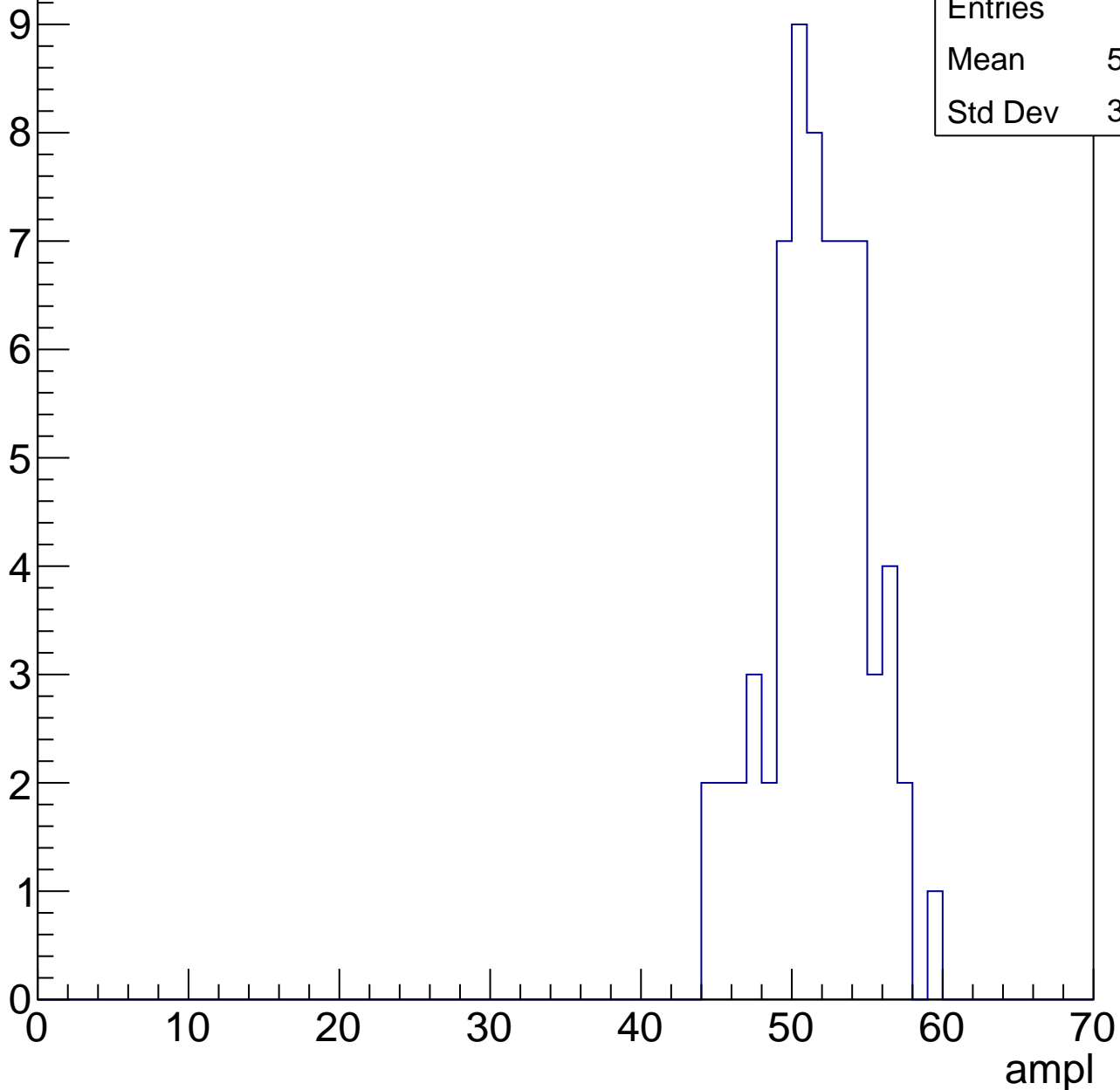


# B0L001S, U17-ch3, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	51.26
Std Dev	3.258



# B0L001S, U17-ch3, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

7  
6  
5  
4  
3  
2  
1  
0

Entries	48
Mean	56.96
Std Dev	2.915

ampl

0

10

20

30

40

50

60

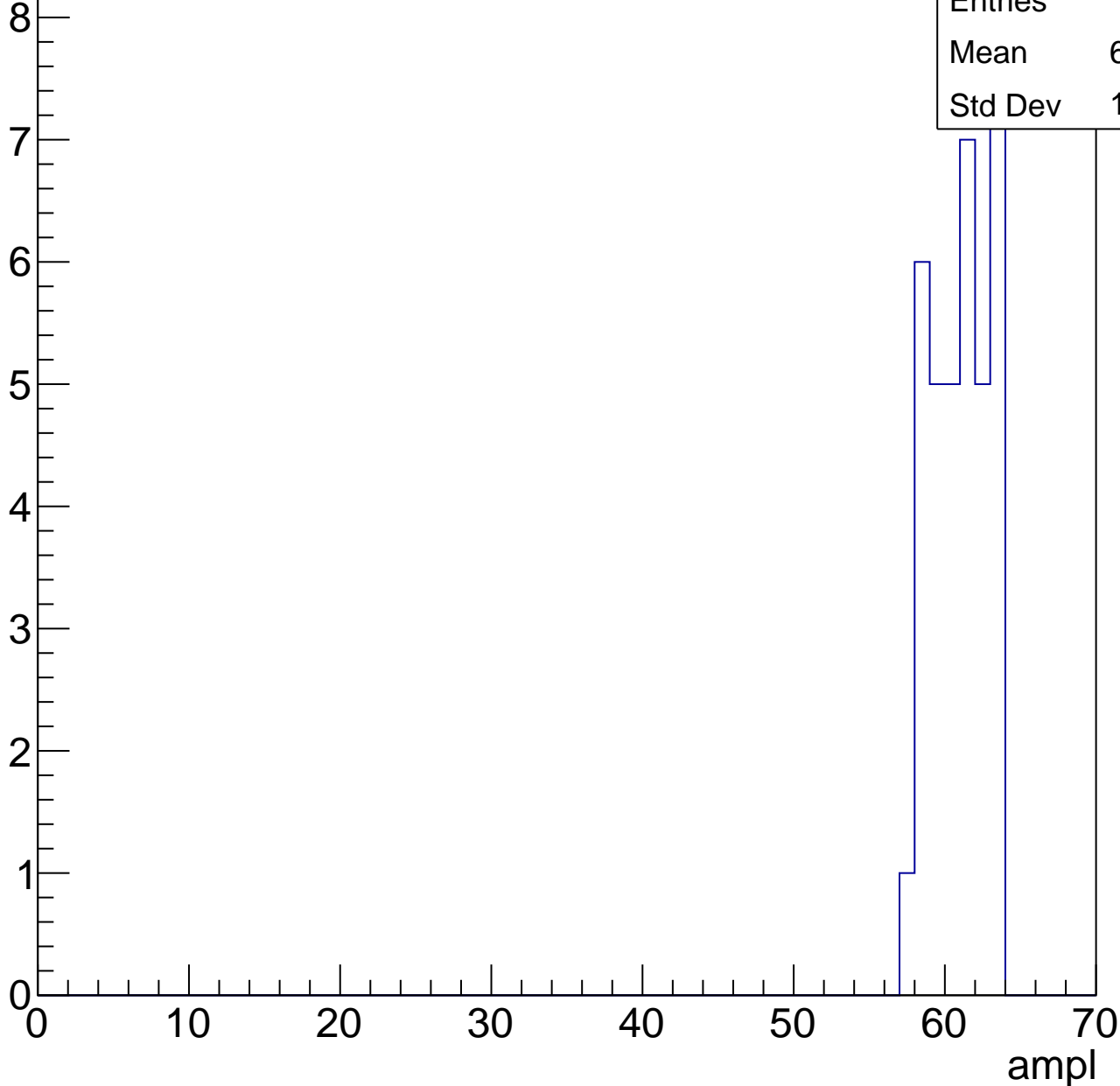
70

# B0L001S, U17-ch3, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

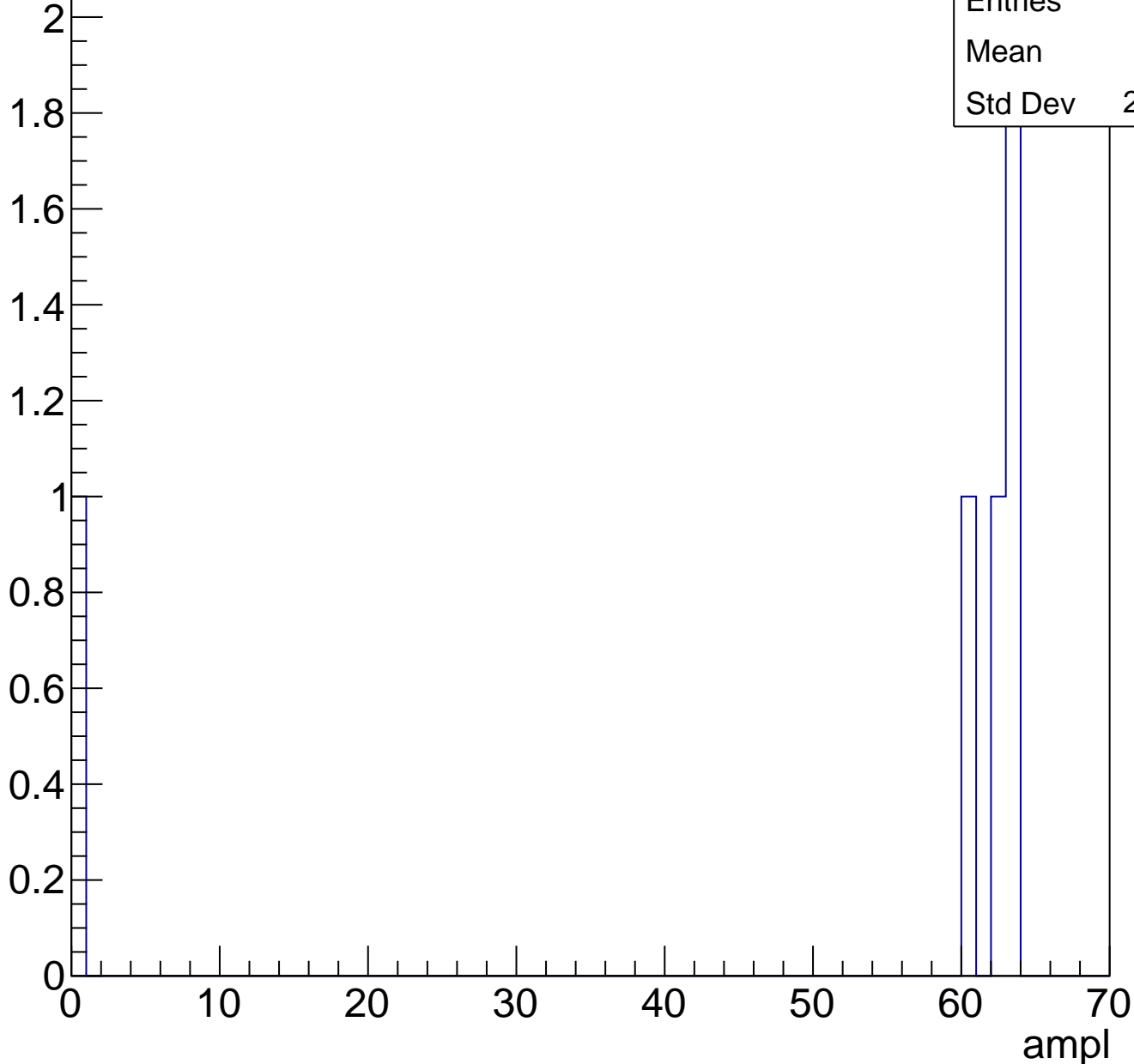
Entries	37
Mean	60.57
Std Dev	1.839



# B0L001S, U17-ch3, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch3, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U17-ch4, adc0

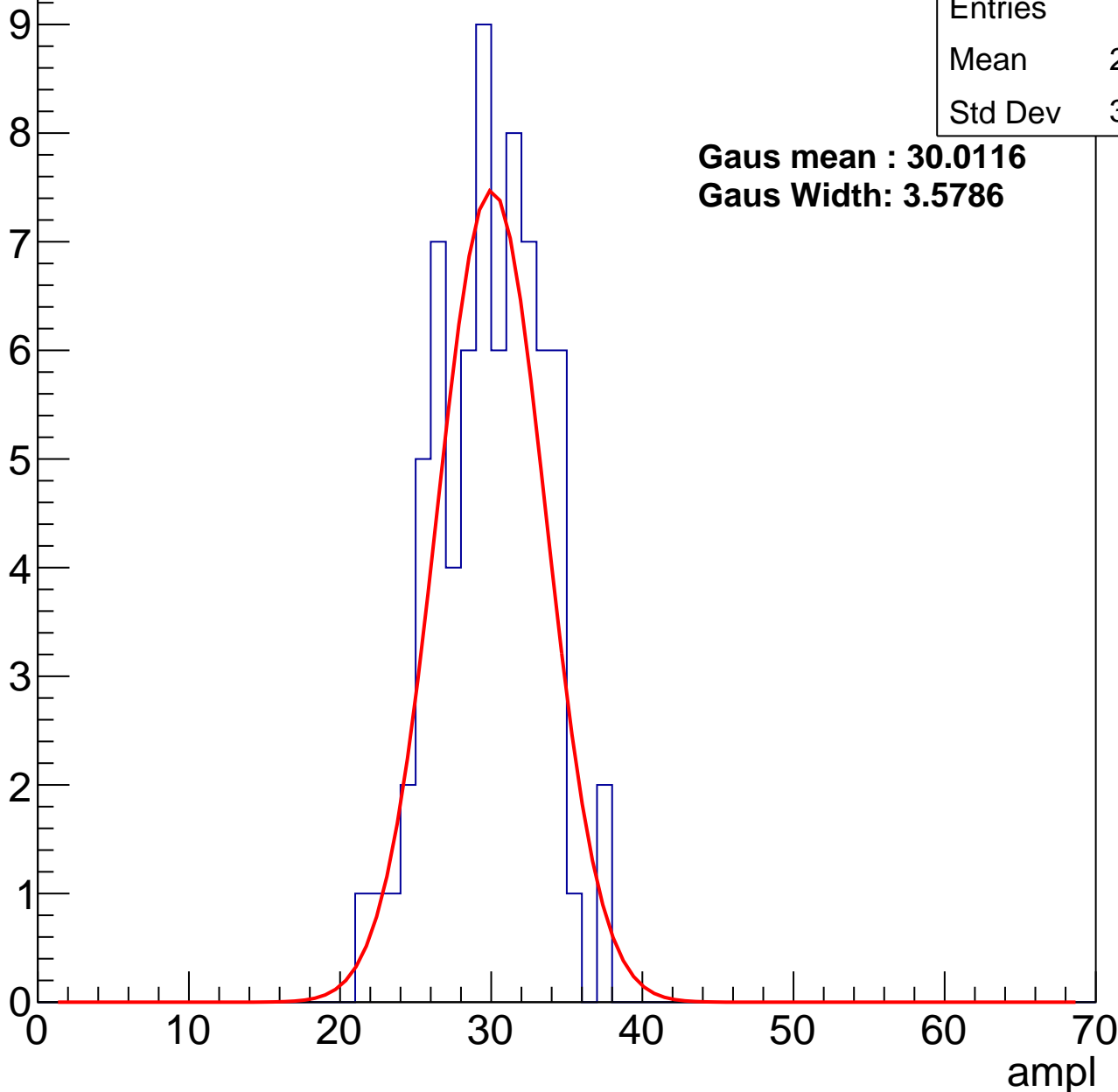
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	29.46
Std Dev	3.456

**Gaus mean : 30.0116**

**Gaus Width: 3.5786**



# B0L001S, U17-ch4, adc1

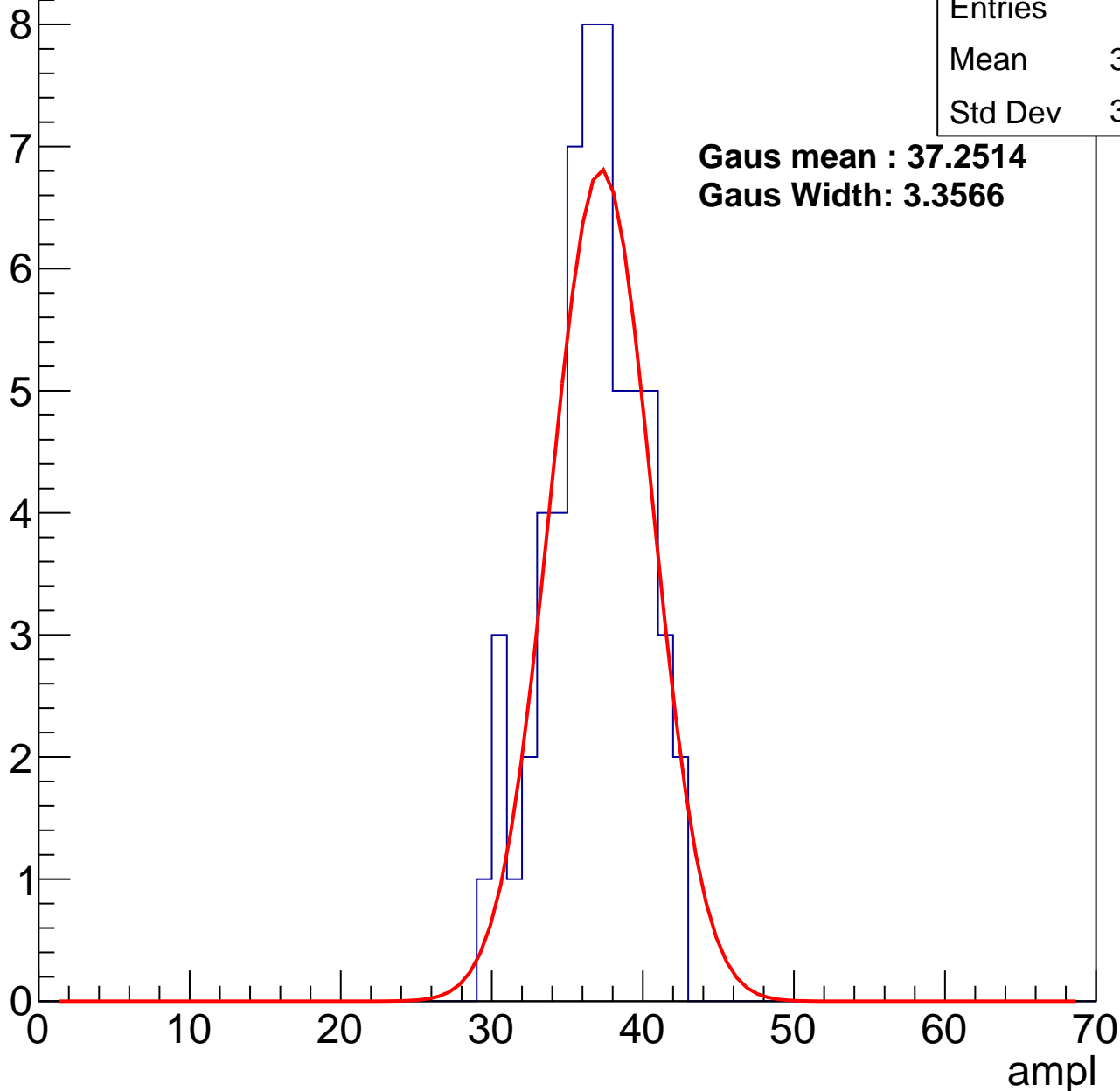
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	36.26
Std Dev	3.132

**Gaus mean : 37.2514**

**Gaus Width: 3.3566**



# B0L001S, U17-ch4, adc2

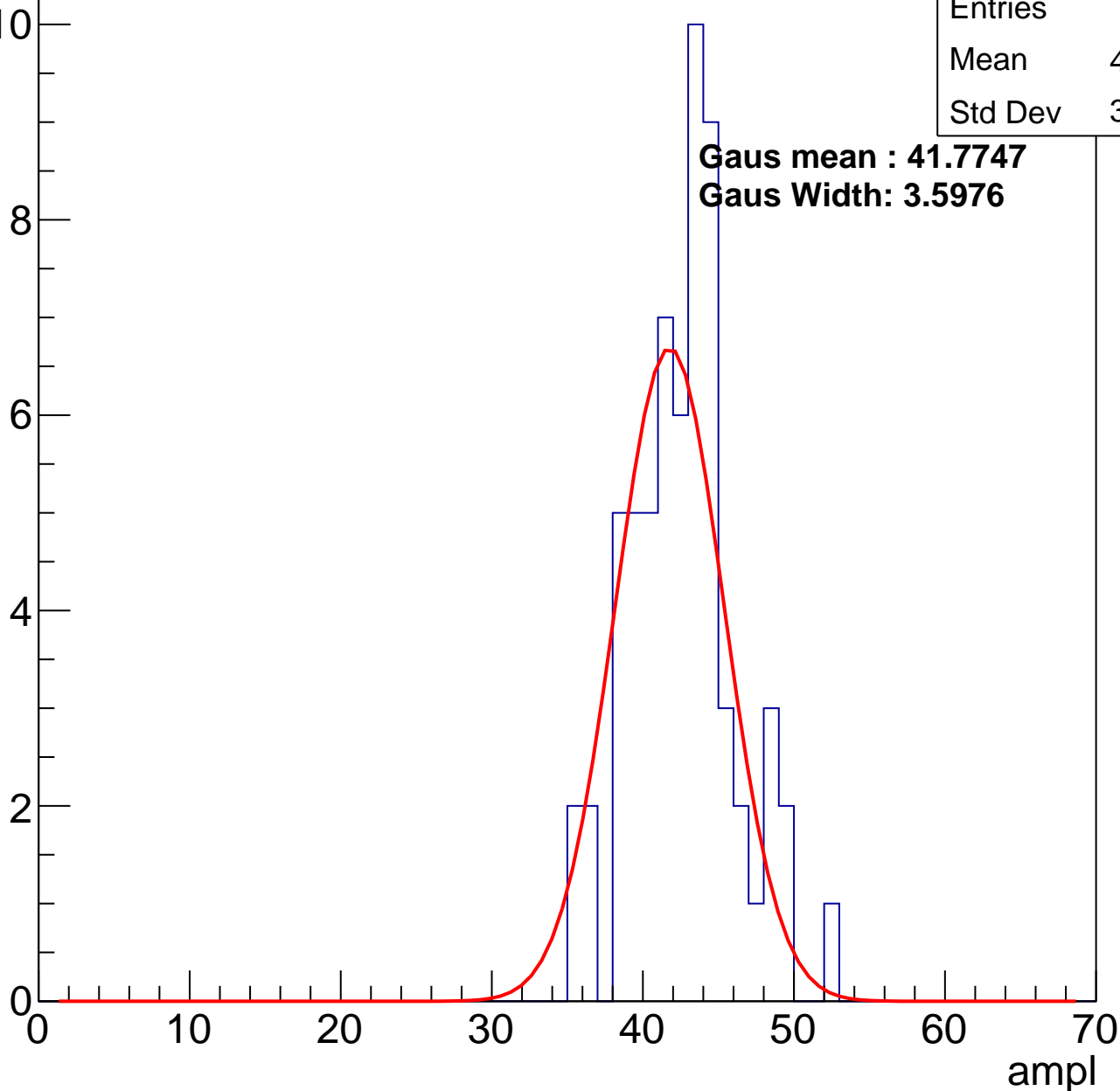
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	42.22
Std Dev	3.462

**Gaus mean : 41.7747**

**Gaus Width: 3.5976**

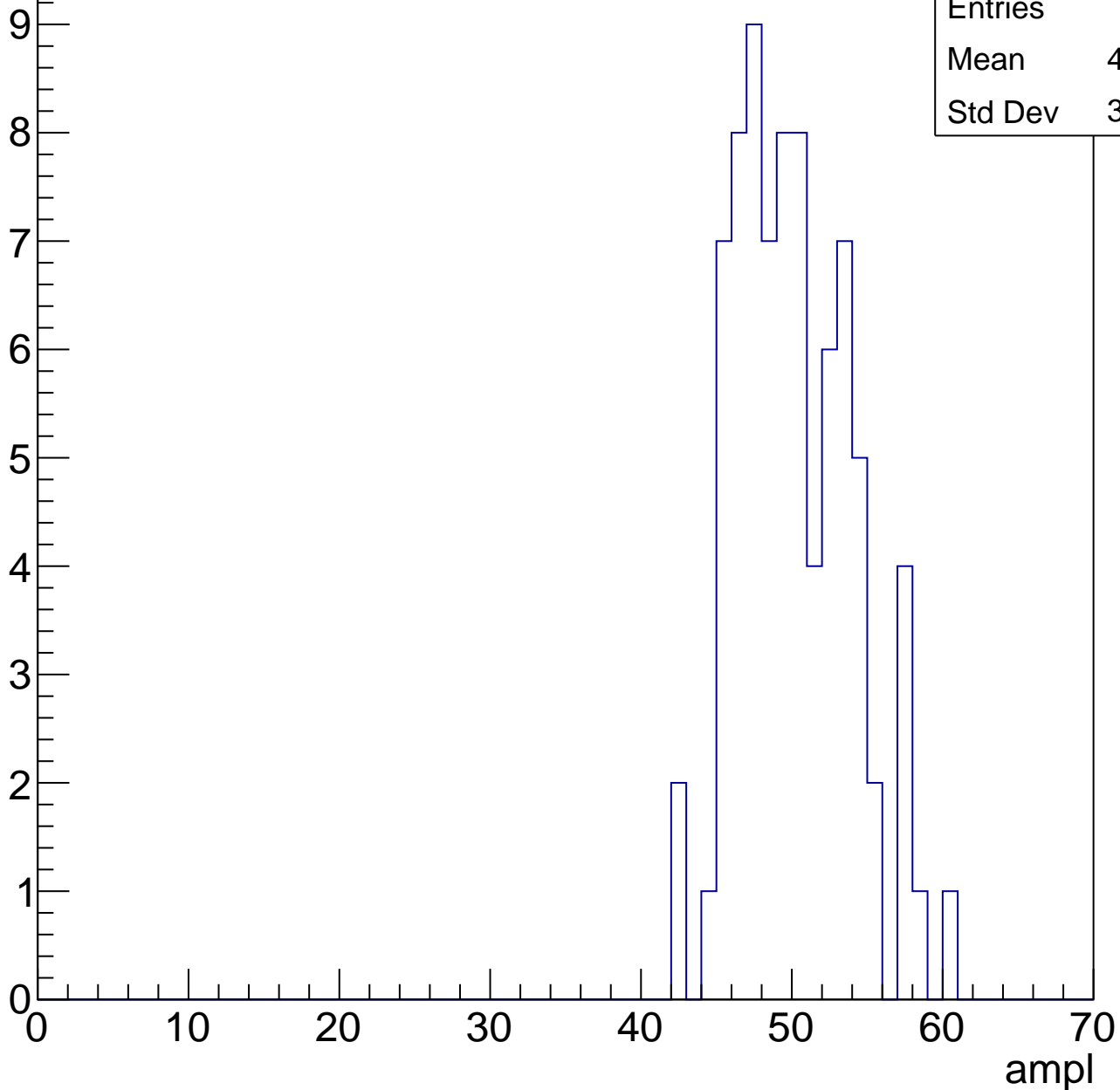


# B0L001S, U17-ch4, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

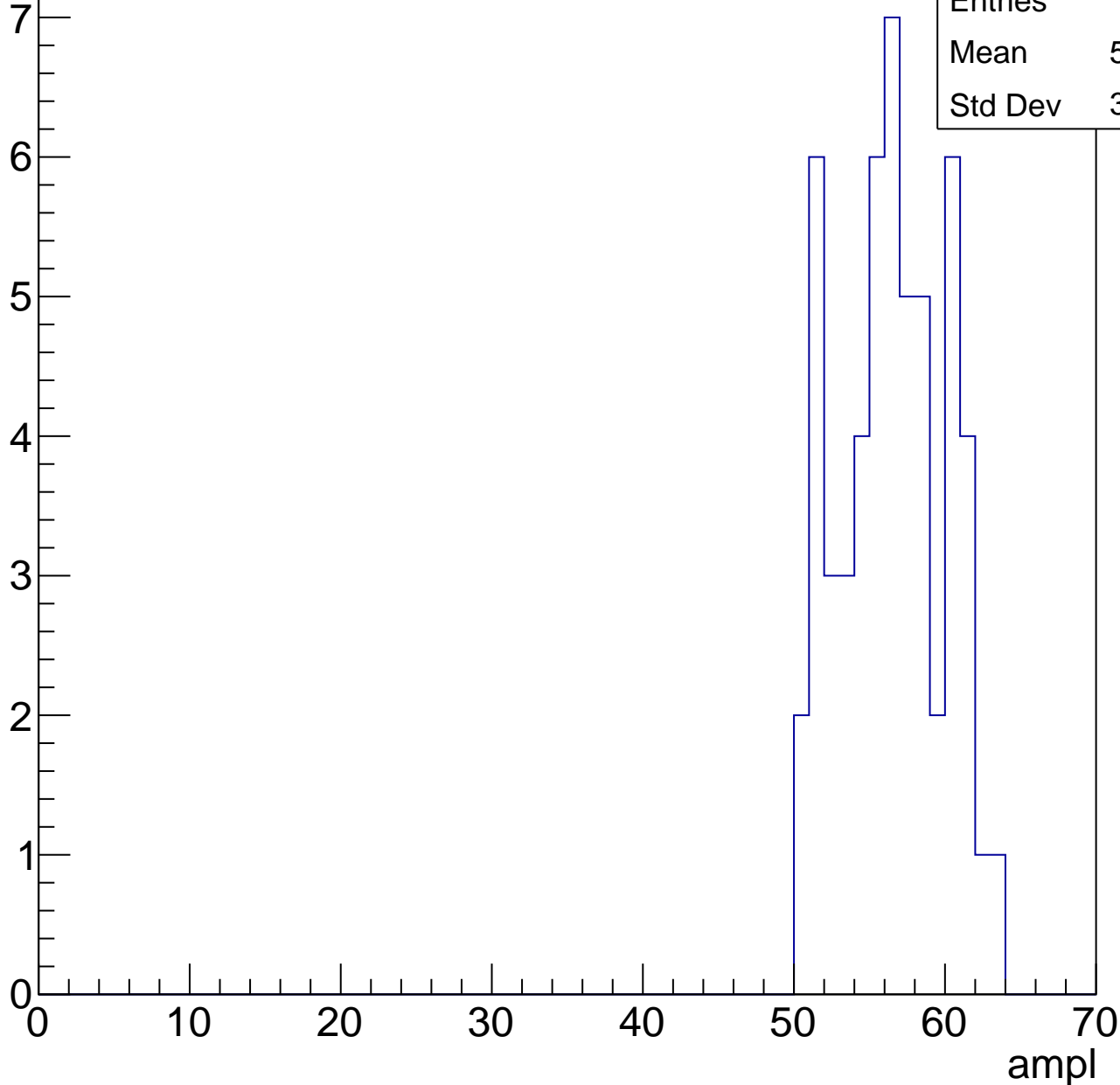
Entries	80
Mean	49.69
Std Dev	3.803



# B0L001S, U17-ch4, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

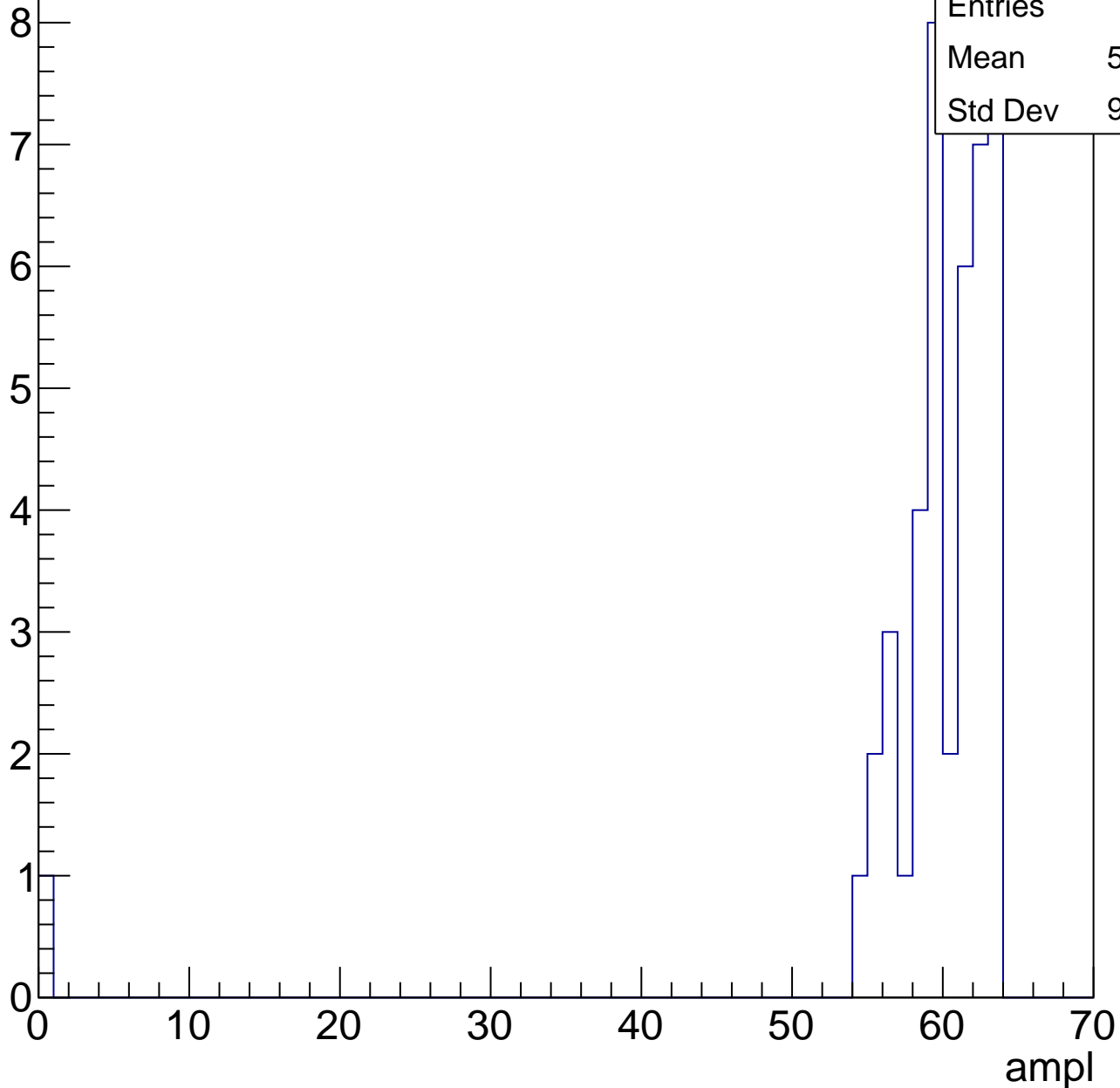


Entries	55
Mean	56.02
Std Dev	3.419

# B0L001S, U17-ch4, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U17-ch4, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

ampl

Entries

3

Mean

61.67

Std Dev

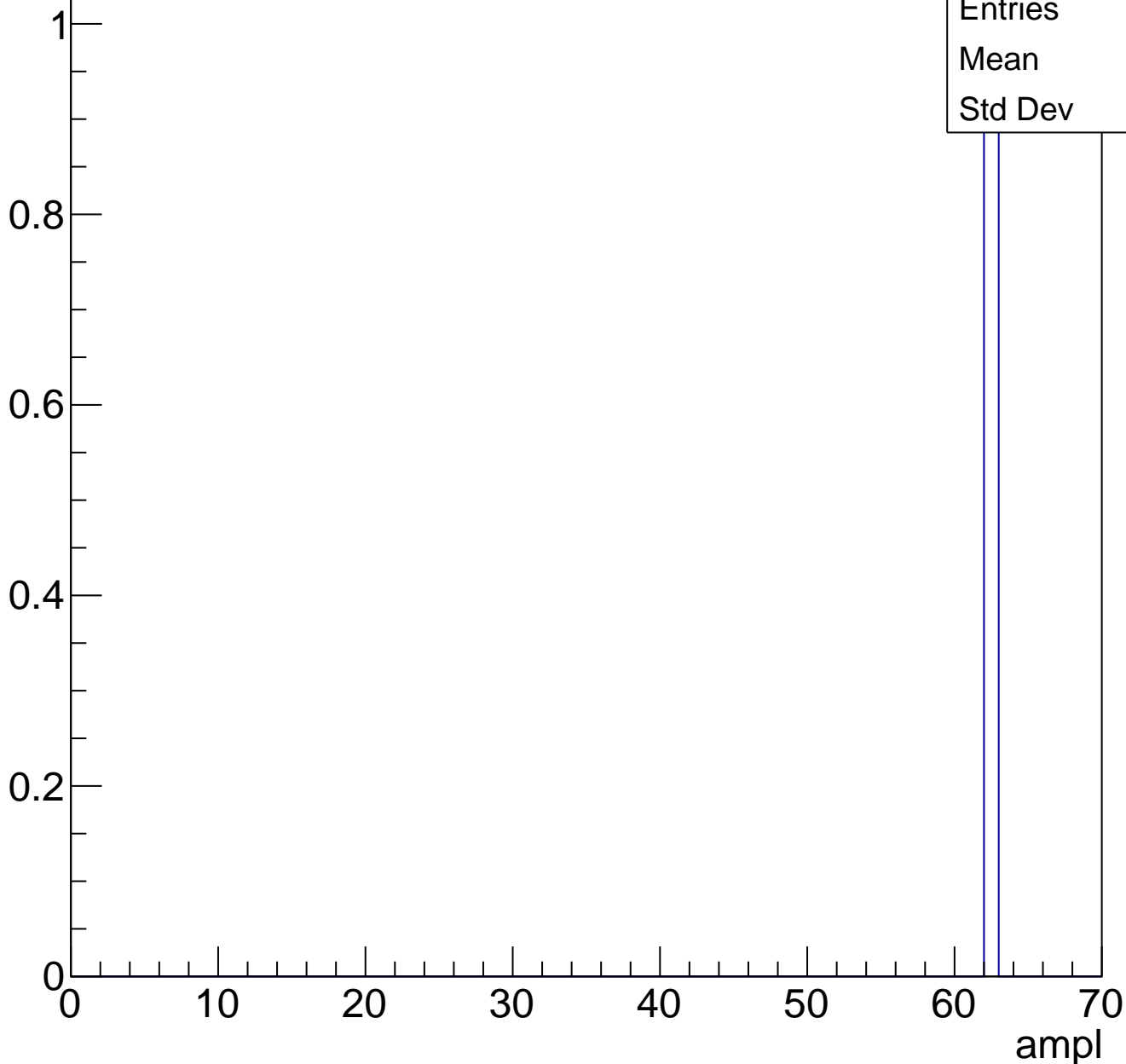
1.247



# B0L001S, U17-ch4, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U17-ch5, adc0

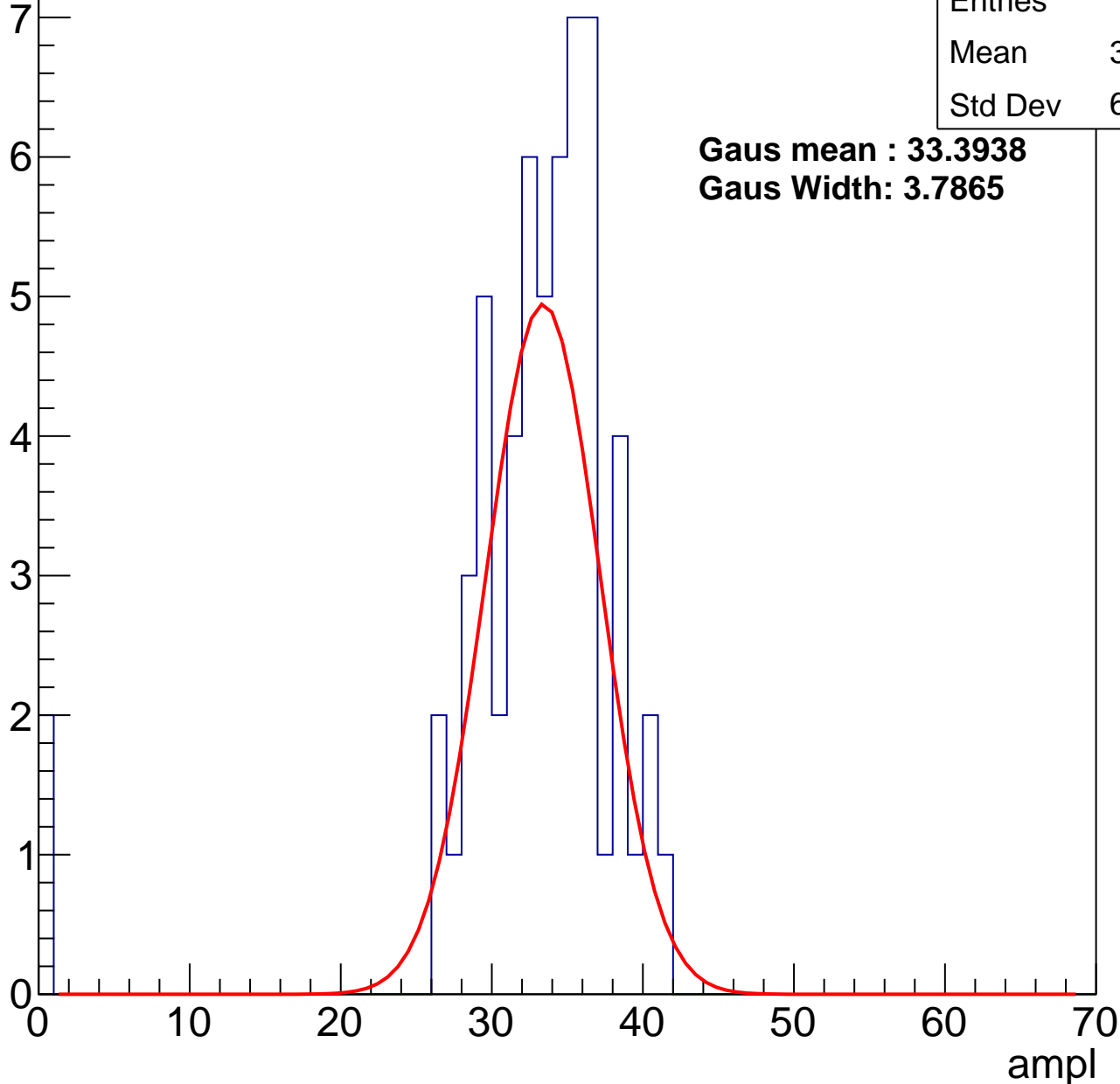
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	32.19
Std Dev	6.985

**Gaus mean : 33.3938**

**Gaus Width: 3.7865**



# B0L001S, U17-ch5, adc1

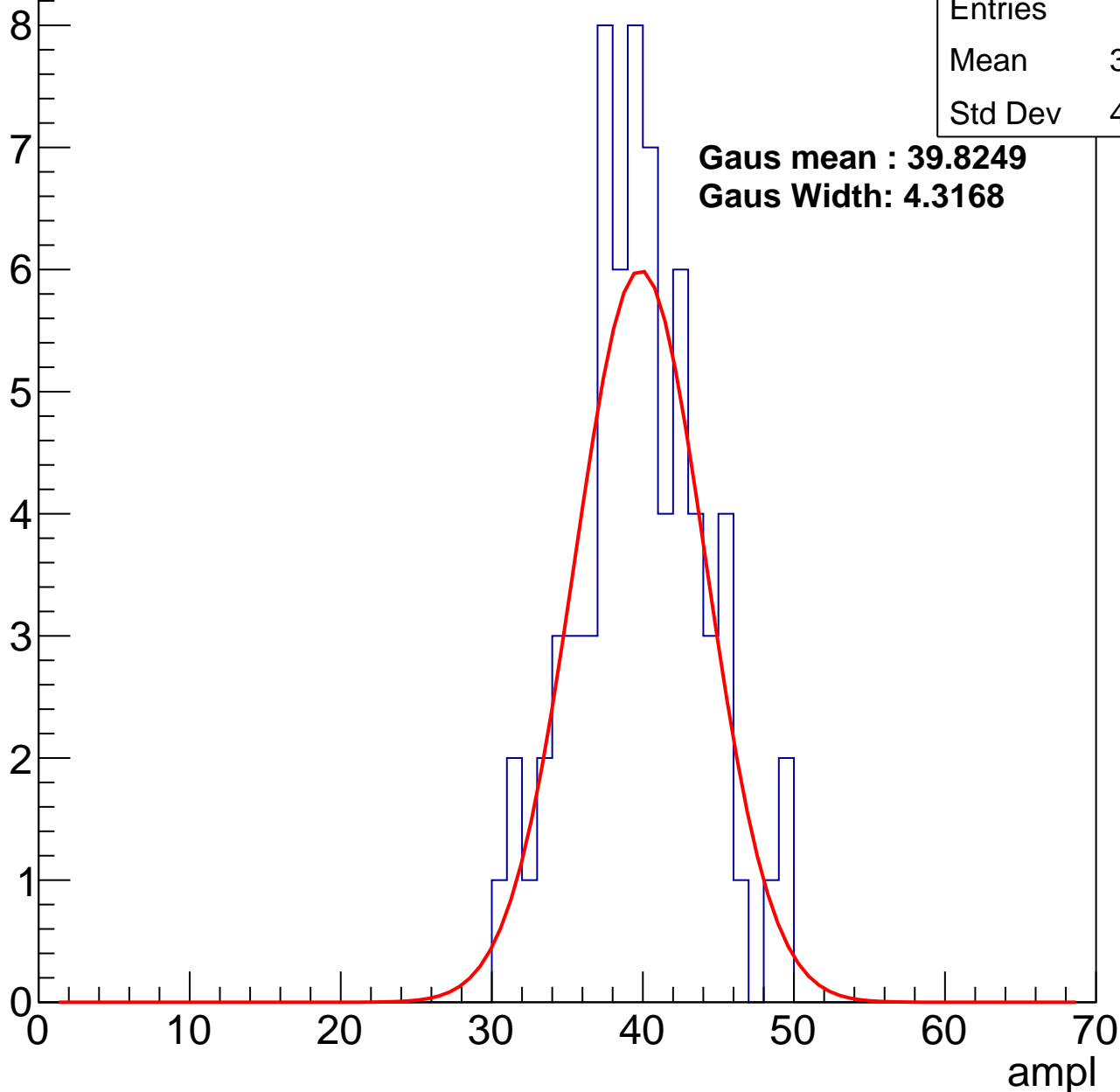
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	39.32
Std Dev	4.172

**Gaus mean : 39.8249**

**Gaus Width: 4.3168**



# B0L001S, U17-ch5, adc2

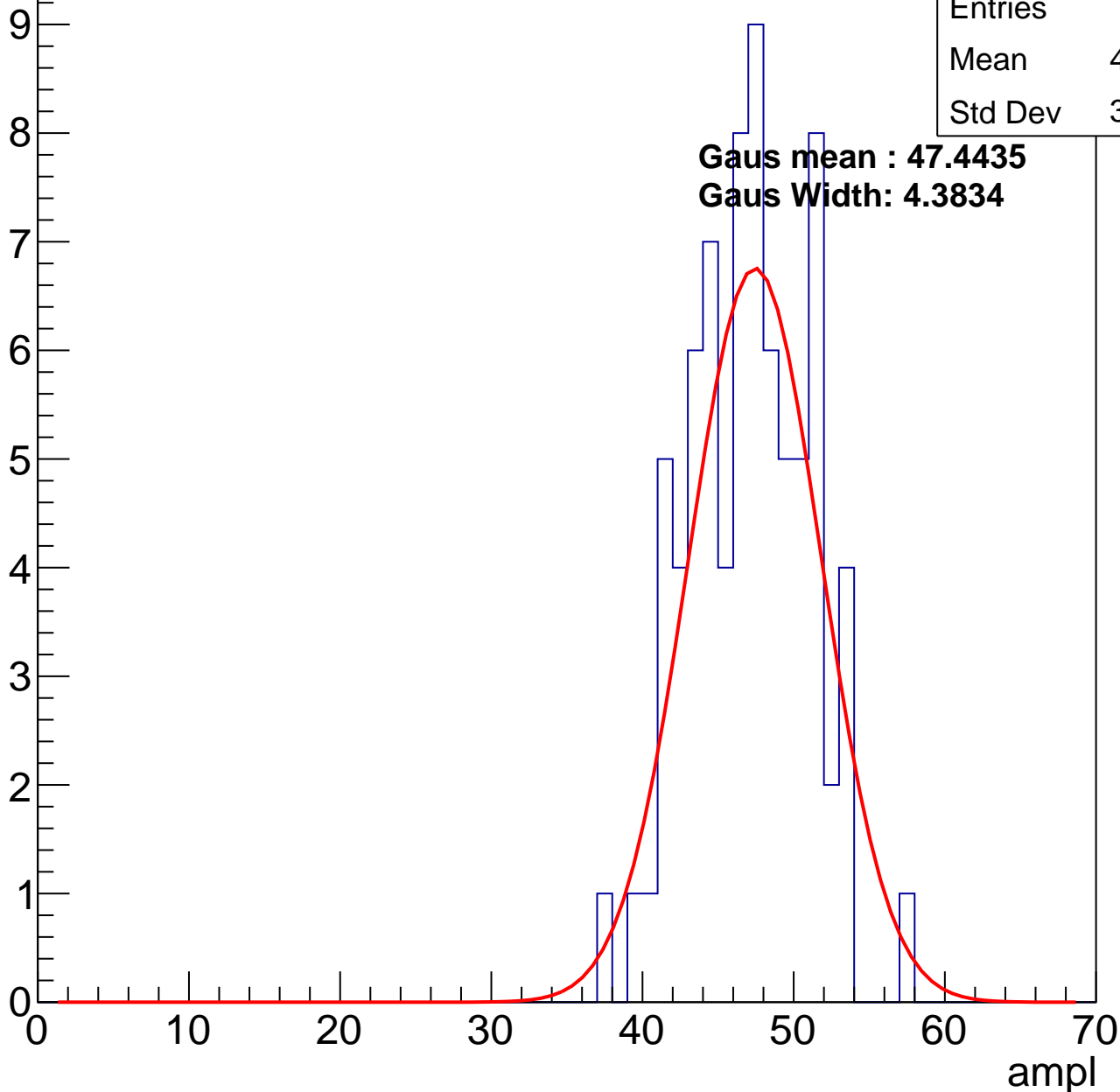
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	77
Mean	46.62
Std Dev	3.878

**Gaus mean : 47.4435**

**Gaus Width: 4.3834**

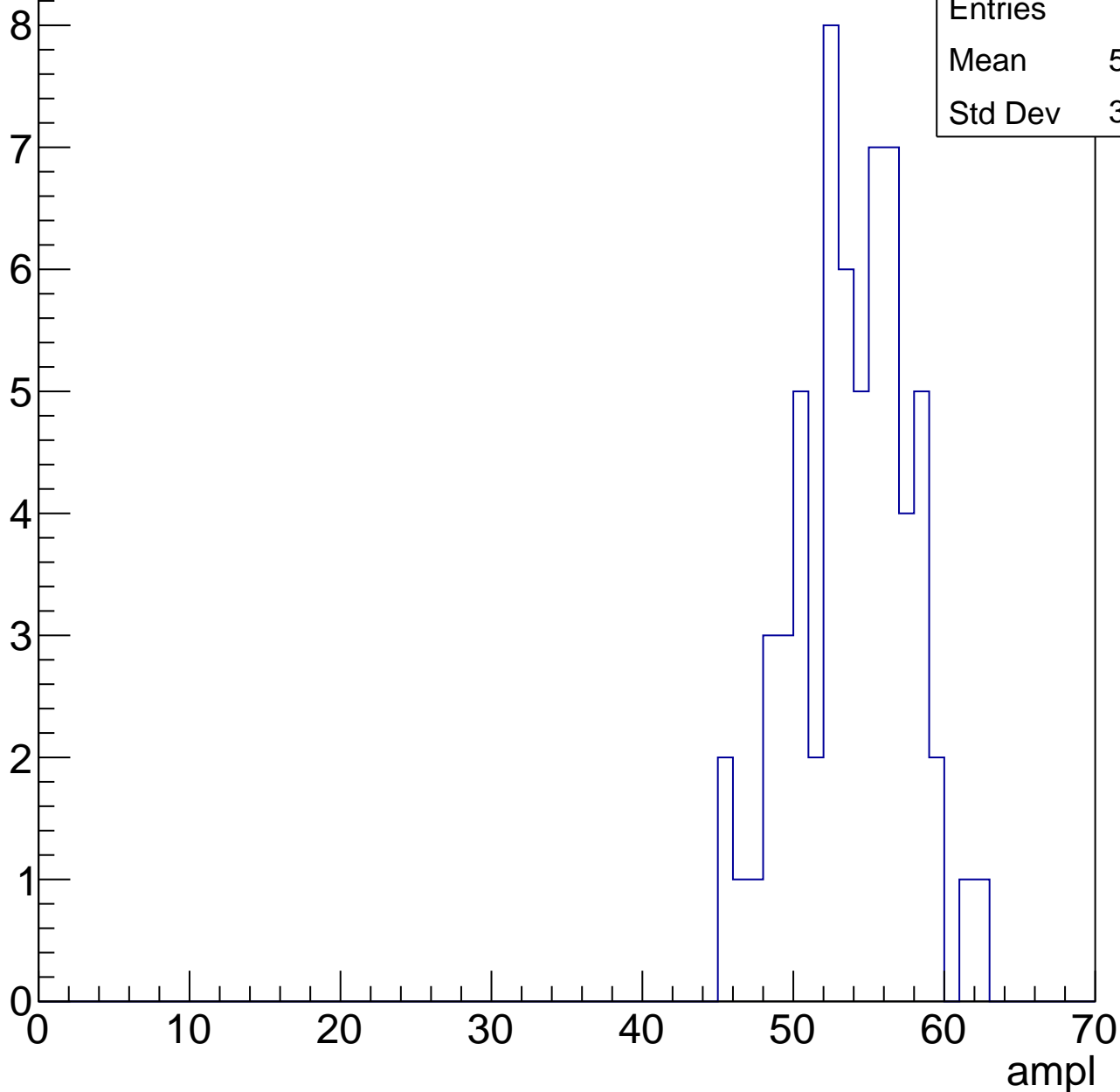


# B0L001S, U17-ch5, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	53.43
Std Dev	3.753

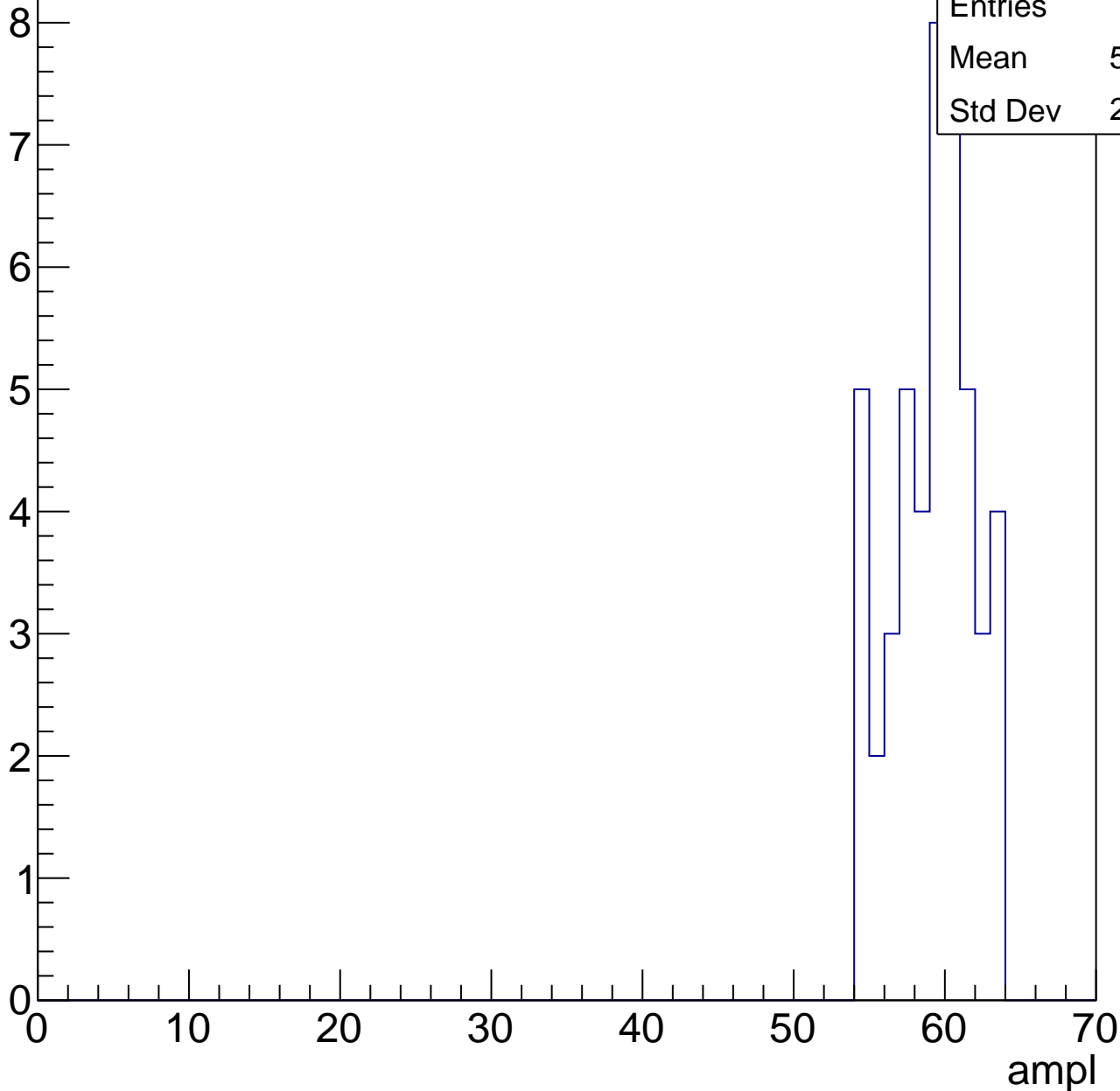


# B0L001S, U17-ch5, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	47
Mean	58.72
Std Dev	2.623

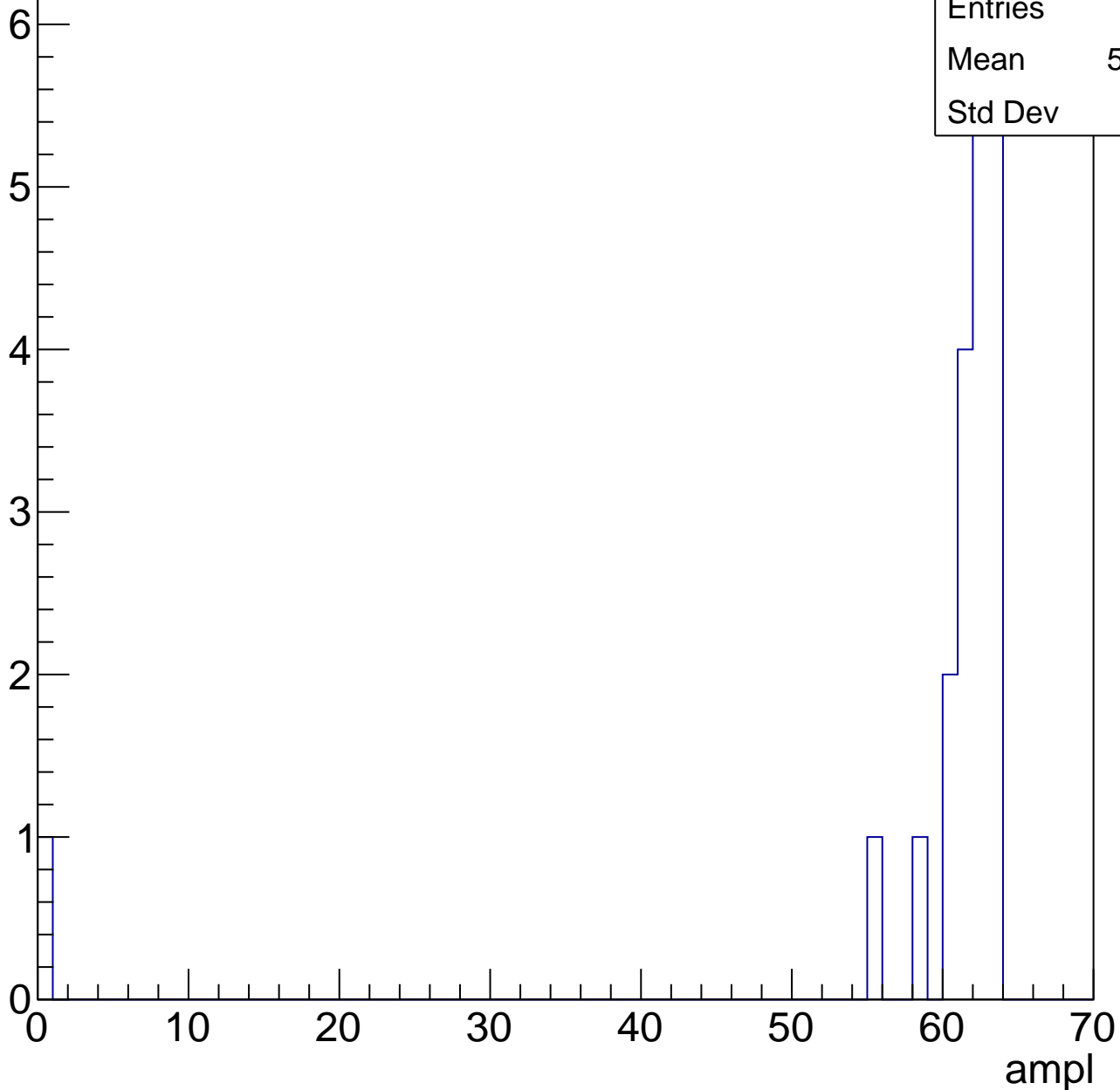


# B0L001S, U17-ch5, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	21
Mean	58.43
Std Dev	13.2



# B0L001S, U17-ch5, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U17-ch5, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	12.5
Std Dev	12.5

# B0L001S, U17-ch6, adc0

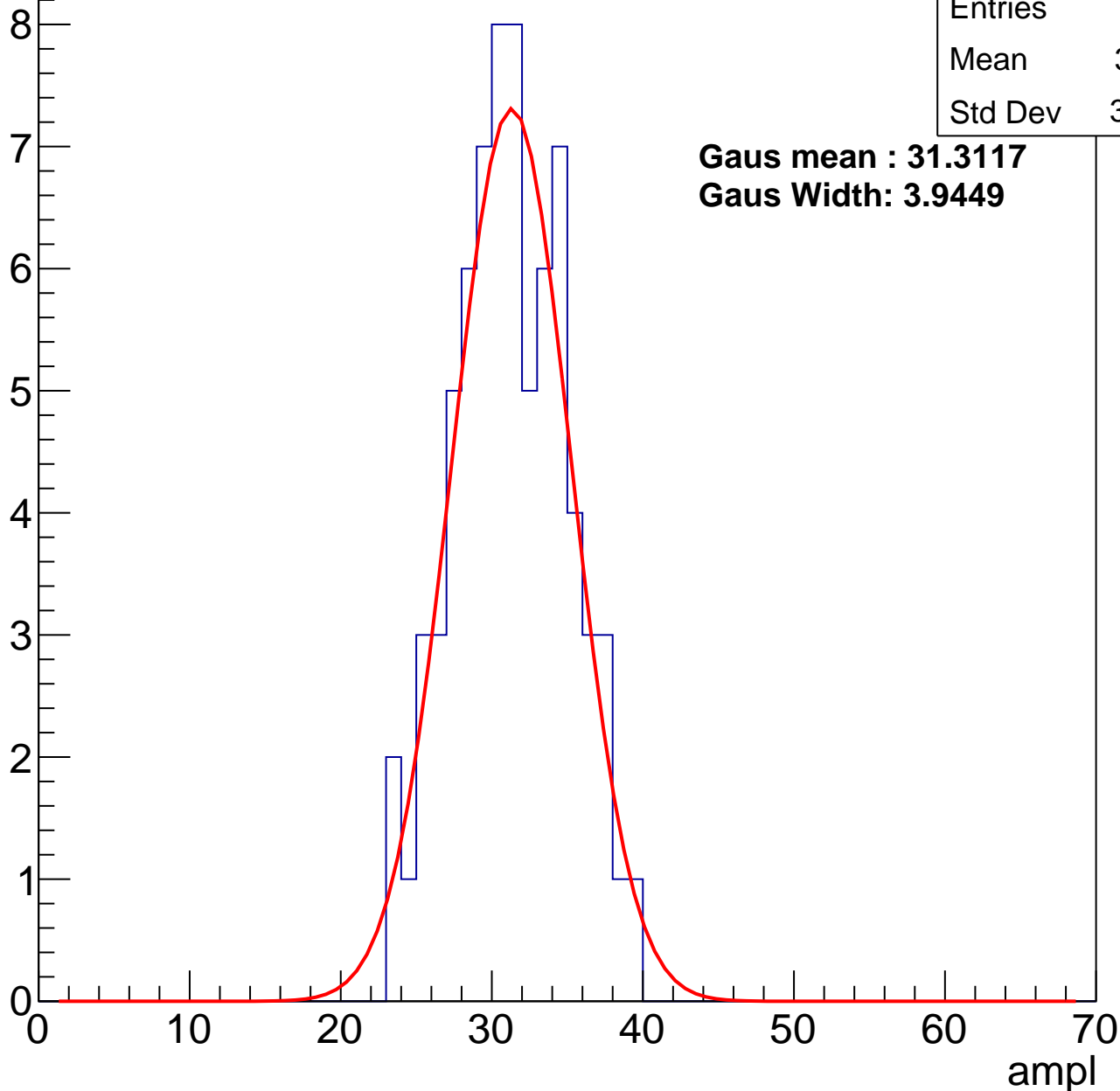
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	30.81
Std Dev	3.663

**Gaus mean : 31.3117**

**Gaus Width: 3.9449**



# B0L001S, U17-ch6, adc1

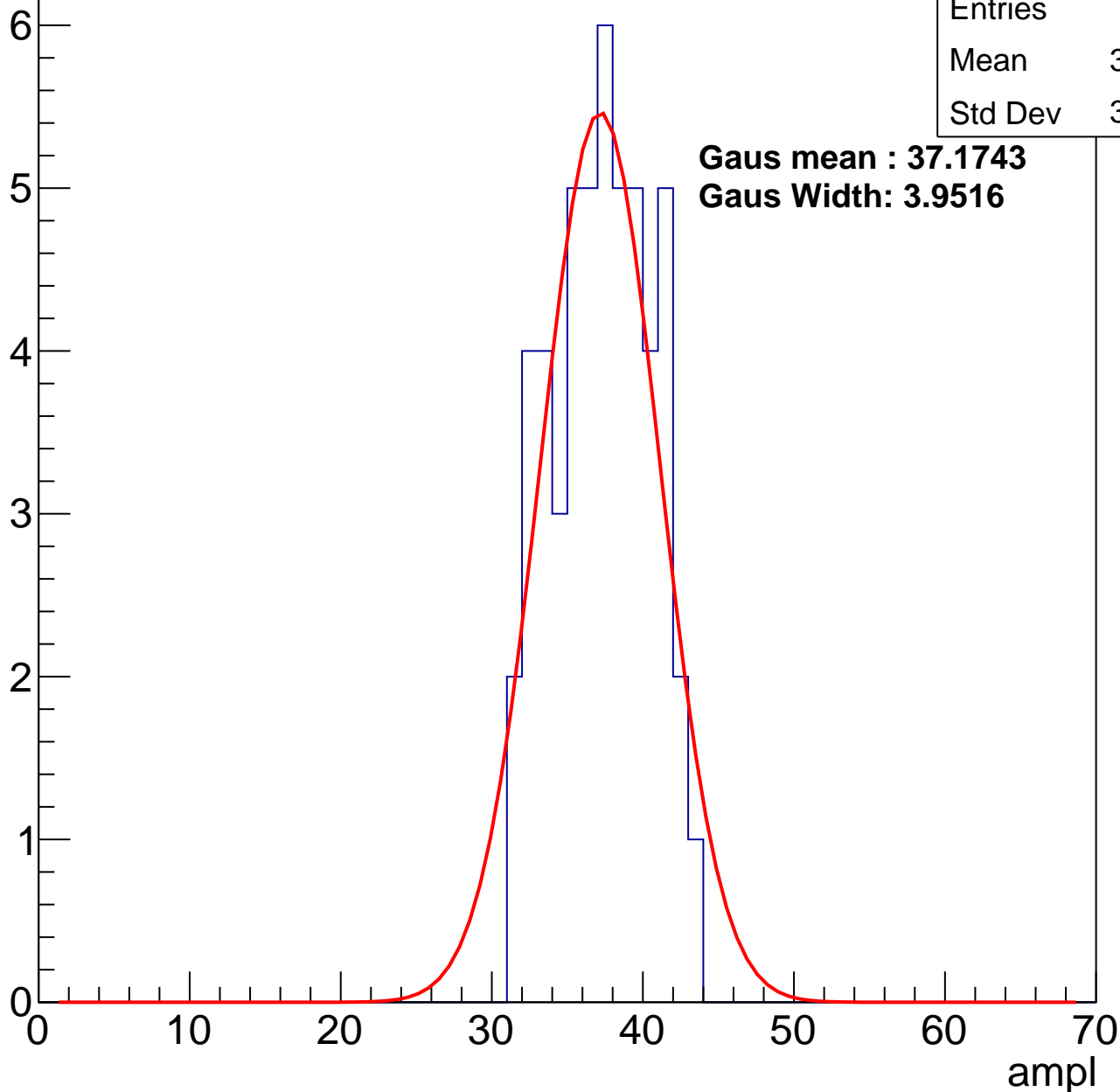
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	51
Mean	36.82
Std Dev	3.173

**Gaus mean : 37.1743**

**Gaus Width: 3.9516**



# B0L001S, U17-ch6, adc2

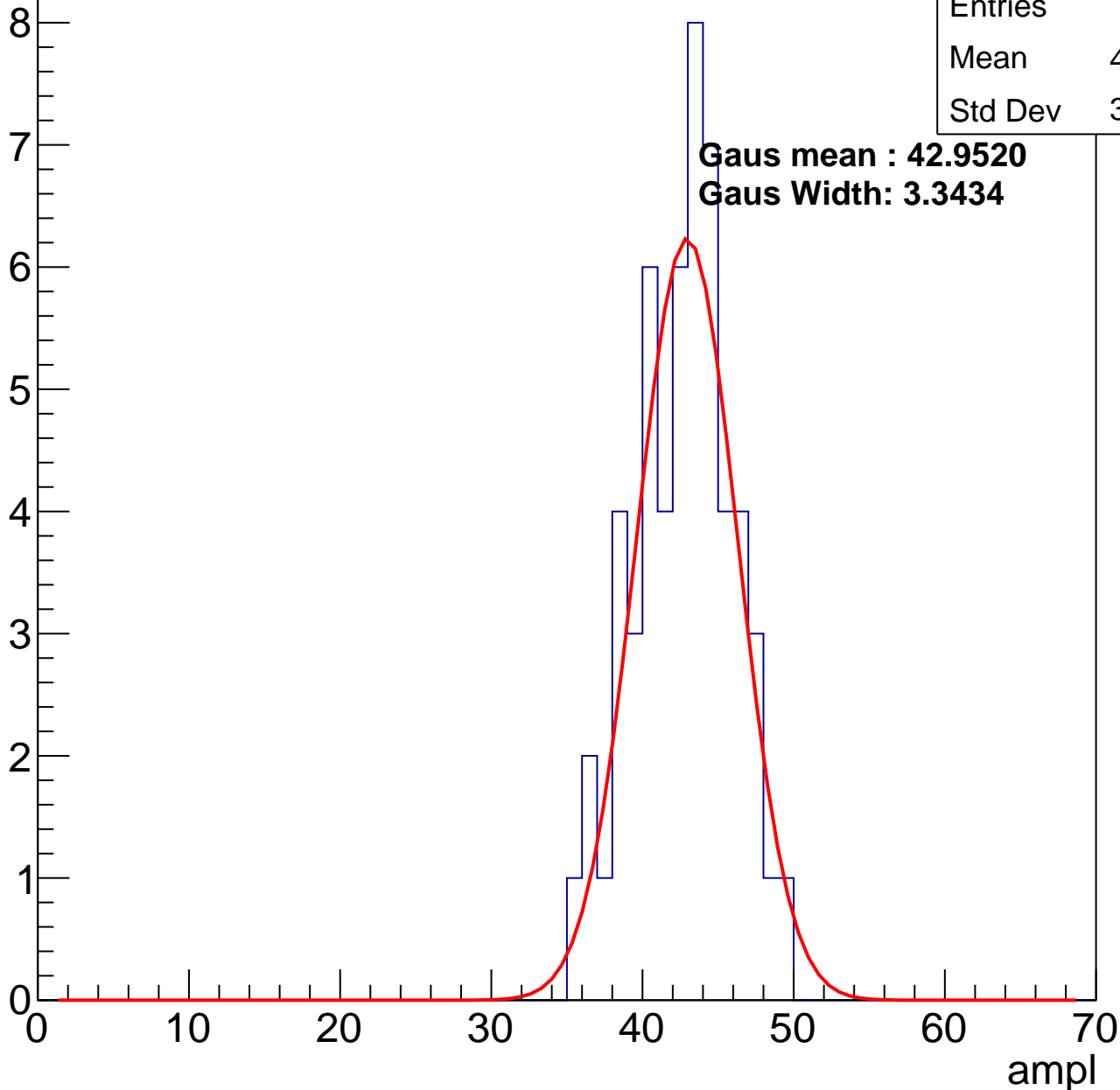
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	42.24
Std Dev	3.185

**Gaus mean : 42.9520**

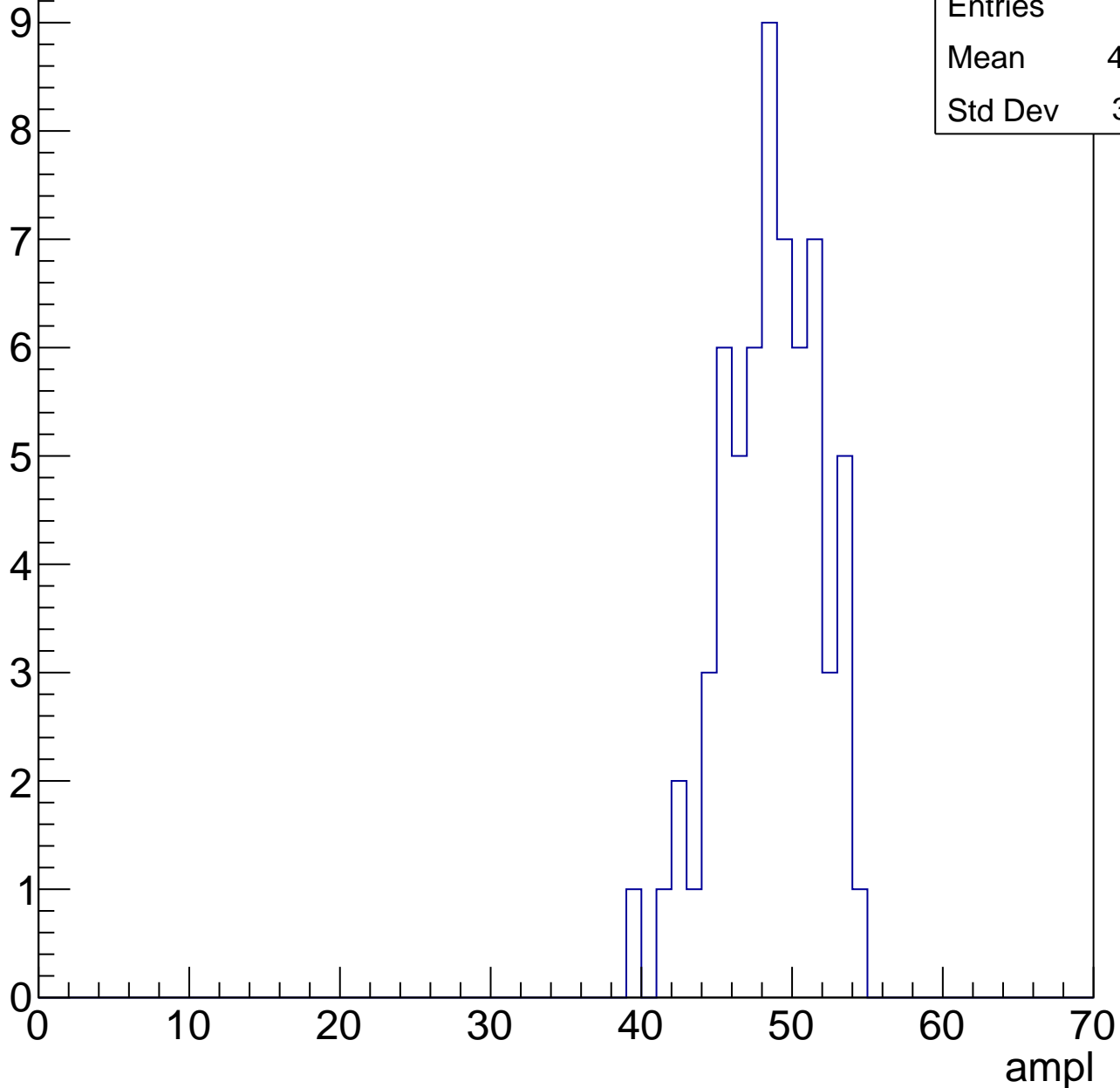
**Gaus Width: 3.3434**



# B0L001S, U17-ch6, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	63
Mean	48.06
Std Dev	3.231

# B0L001S, U17-ch6, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

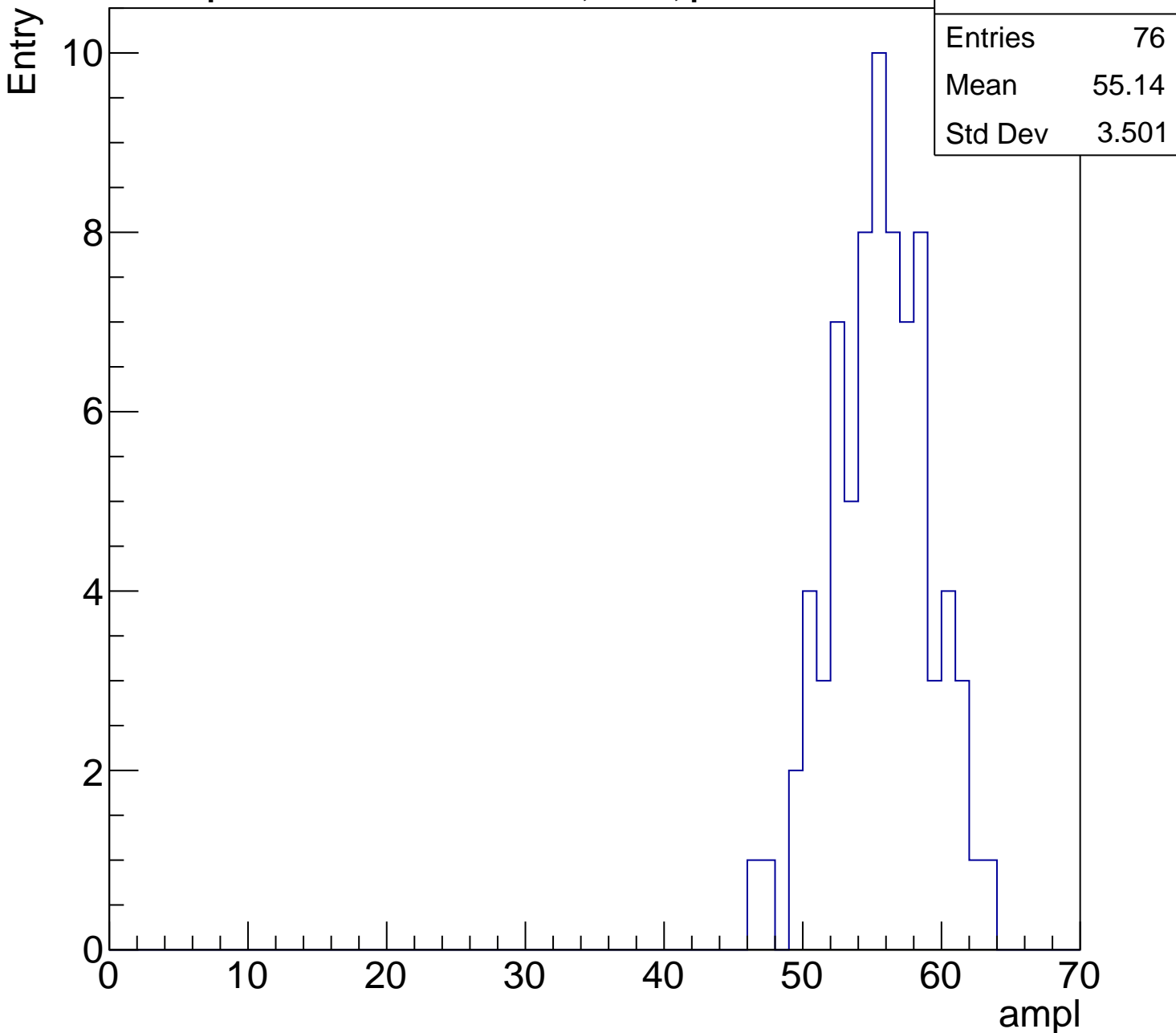
Entries	76
Mean	55.14
Std Dev	3.501

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

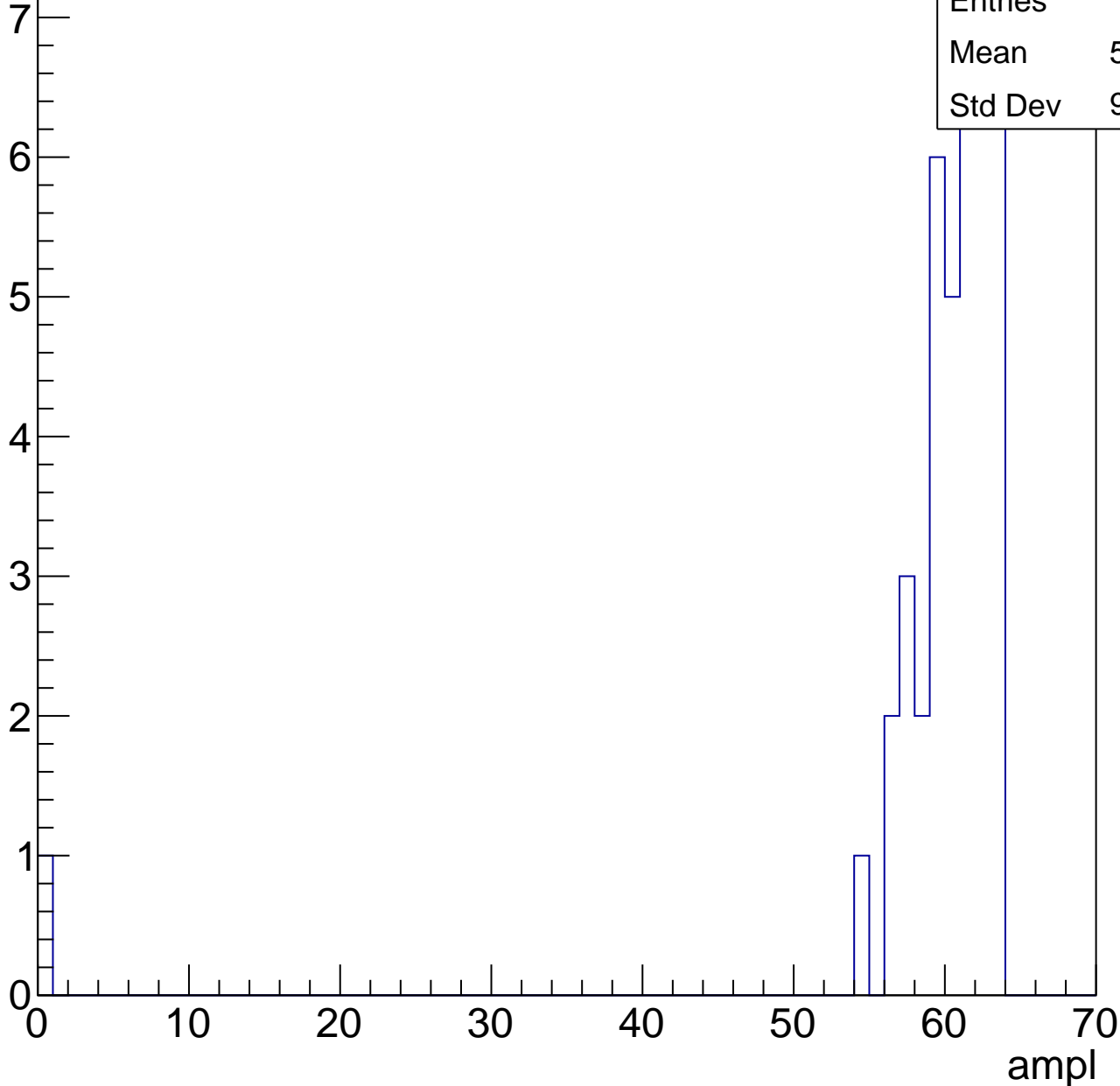


# B0L001S, U17-ch6, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	41
Mean	58.76
Std Dev	9.555



# B0L001S, U17-ch6, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

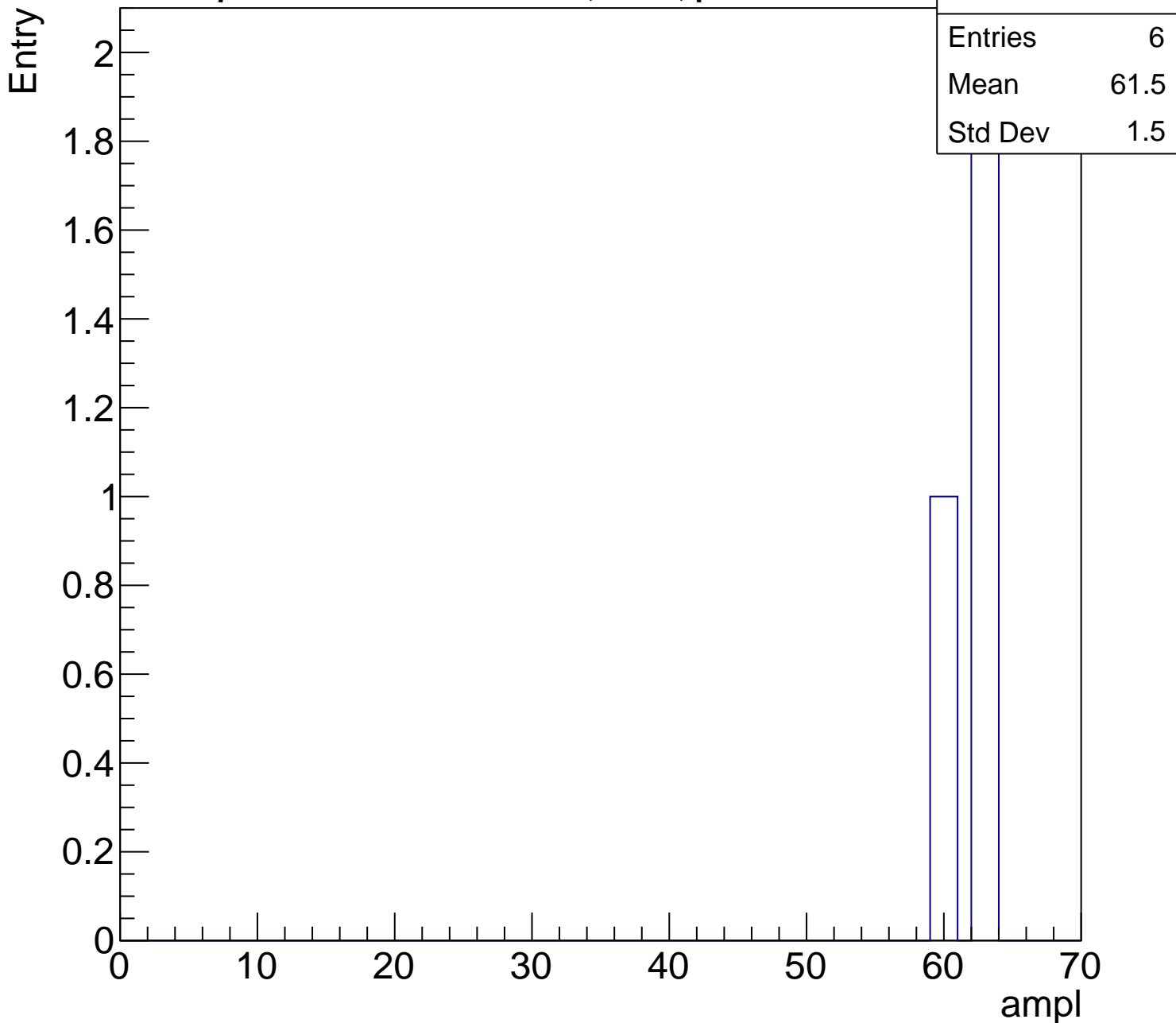
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	61.5
Std Dev	1.5

ampl

0 10 20 30 40 50 60 70





# B0L001S, U17-ch6, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U17-ch7, adc0

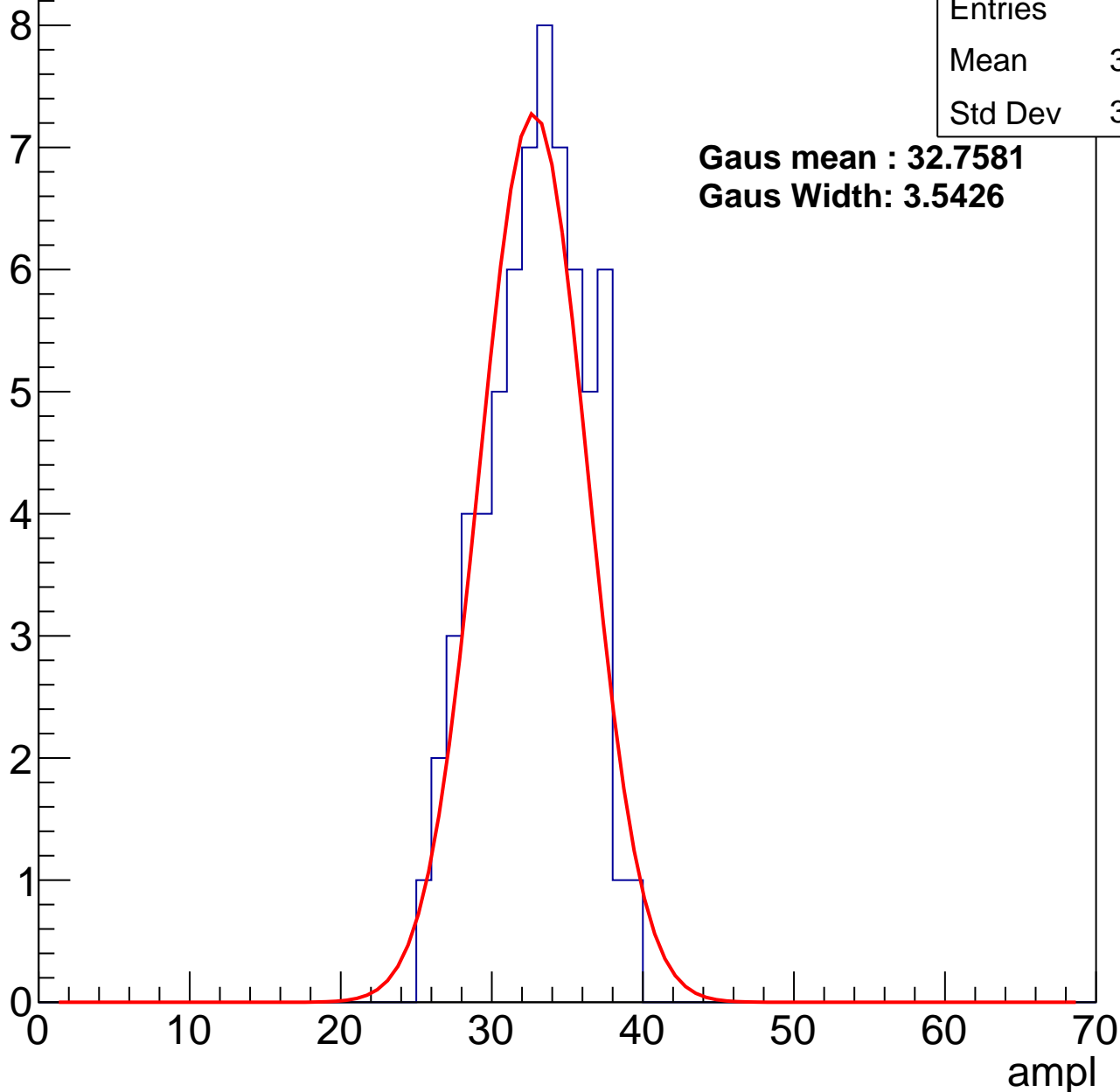
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	32.38
Std Dev	3.297

**Gaus mean : 32.7581**

**Gaus Width: 3.5426**



# B0L001S, U17-ch7, adc1

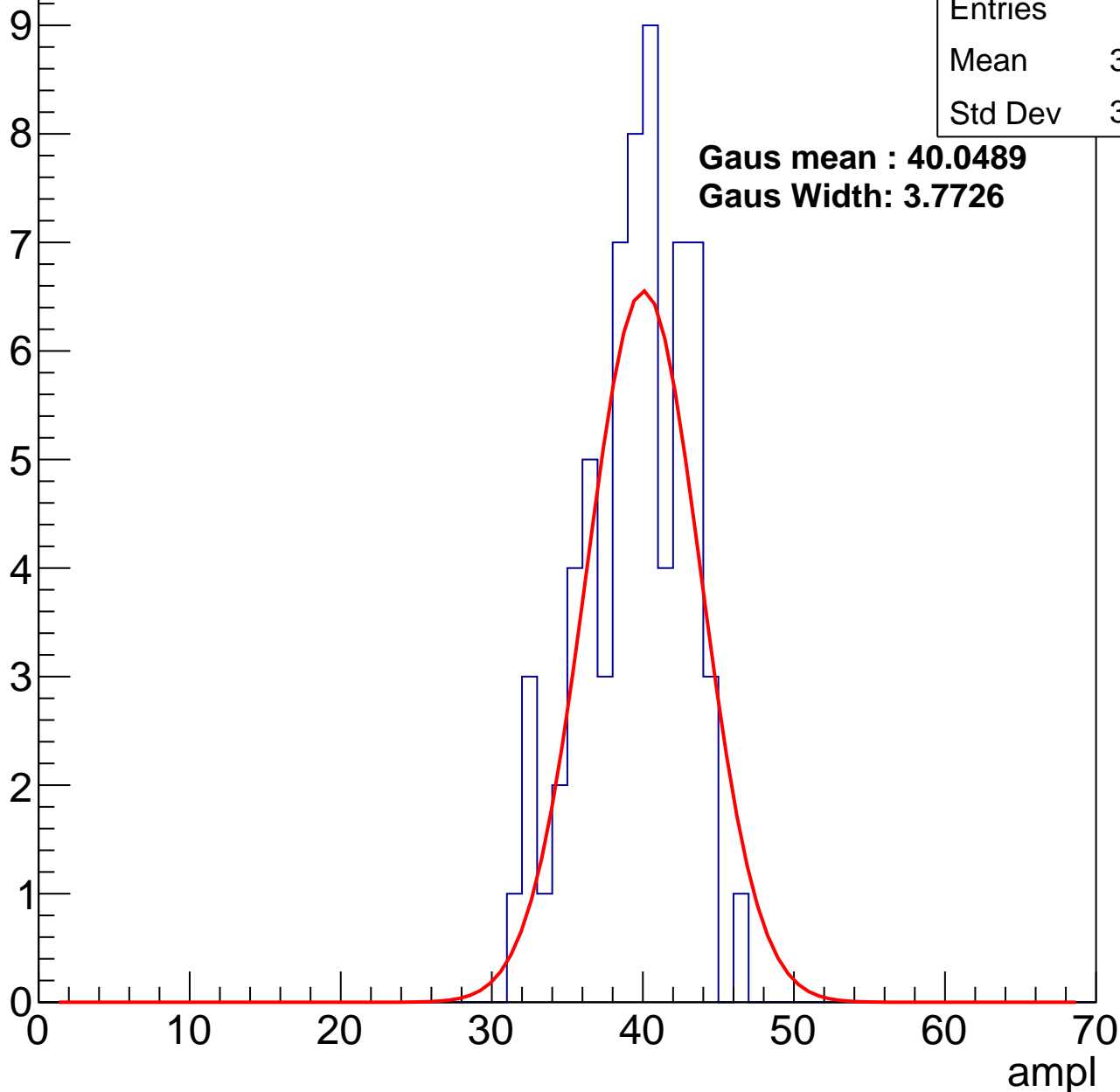
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	38.98
Std Dev	3.395

**Gaus mean : 40.0489**

**Gaus Width: 3.7726**



# B0L001S, U17-ch7, adc2

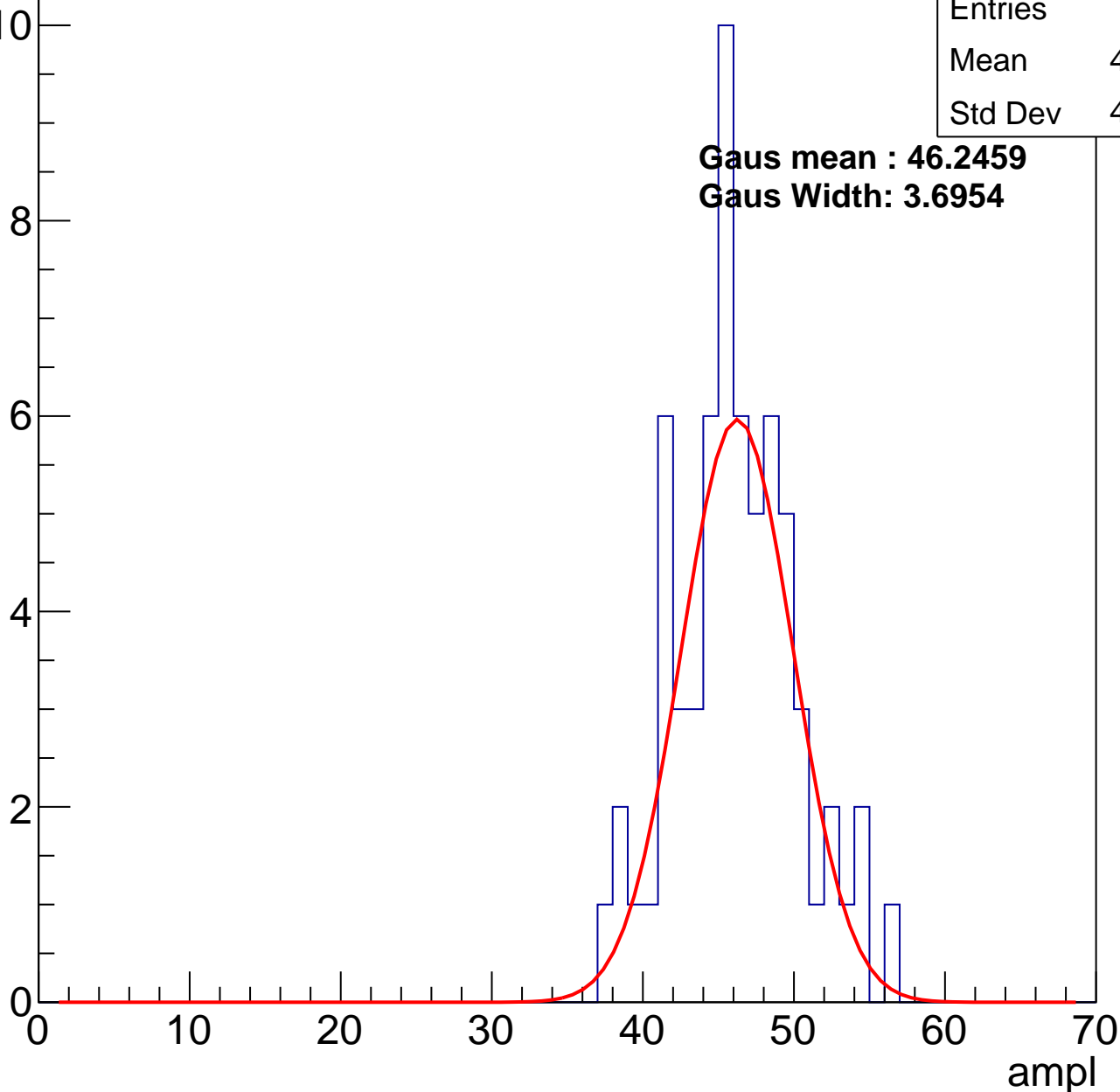
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	45.74
Std Dev	4.009

**Gaus mean : 46.2459**

**Gaus Width: 3.6954**

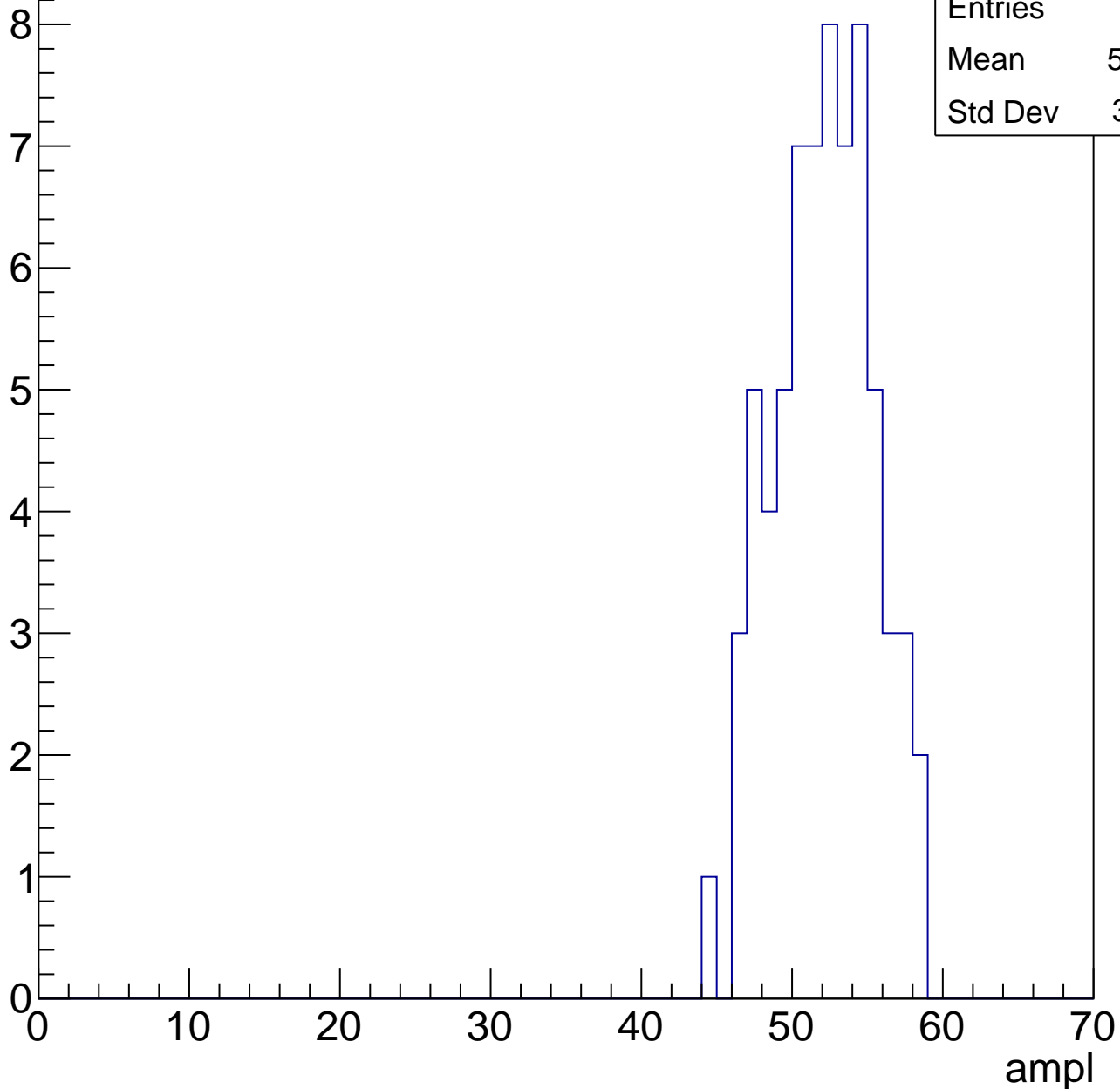


# B0L001S, U17-ch7, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	51.62
Std Dev	3.231

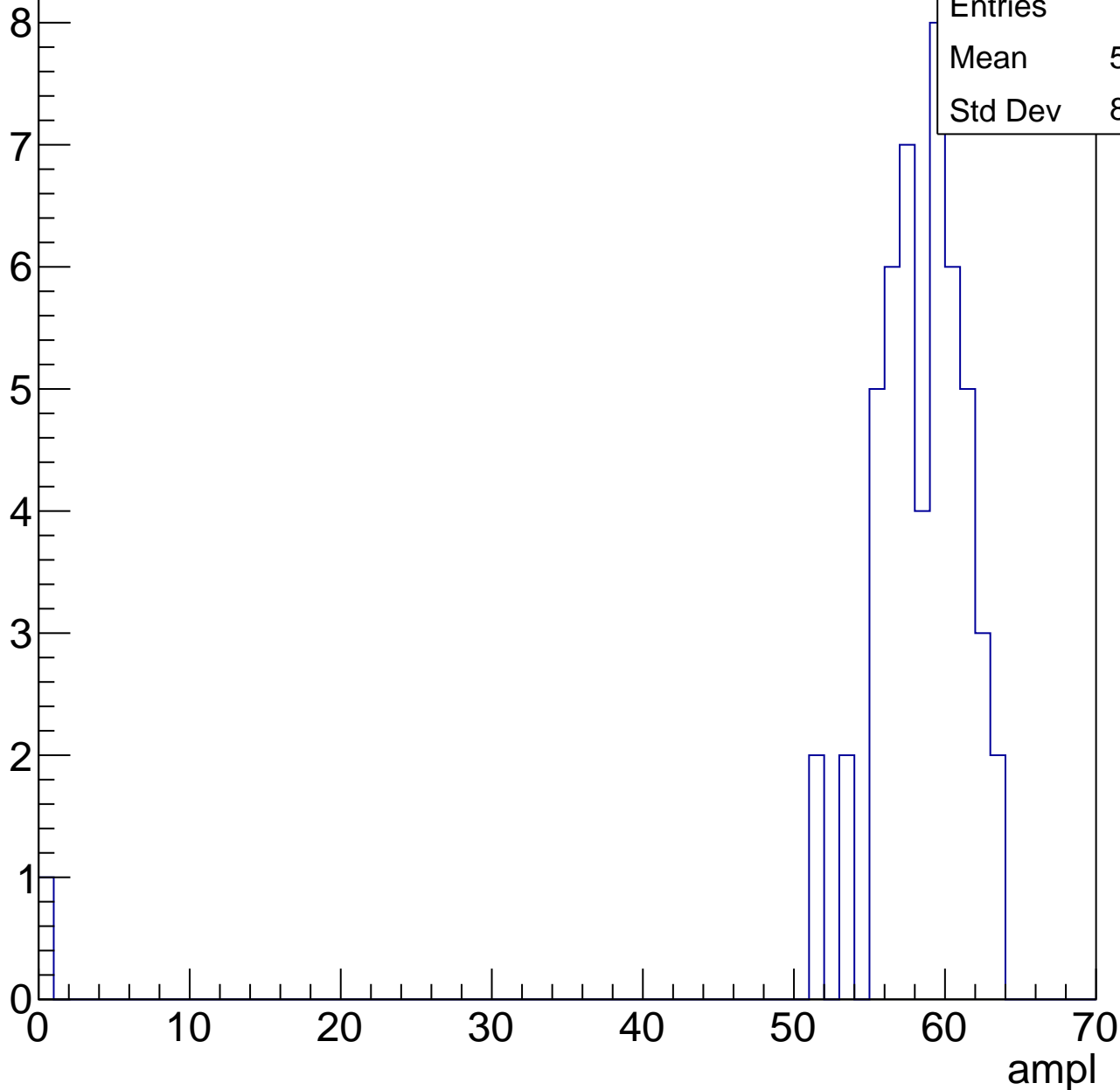


# B0L001S, U17-ch7, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	51
Mean	56.84
Std Dev	8.512

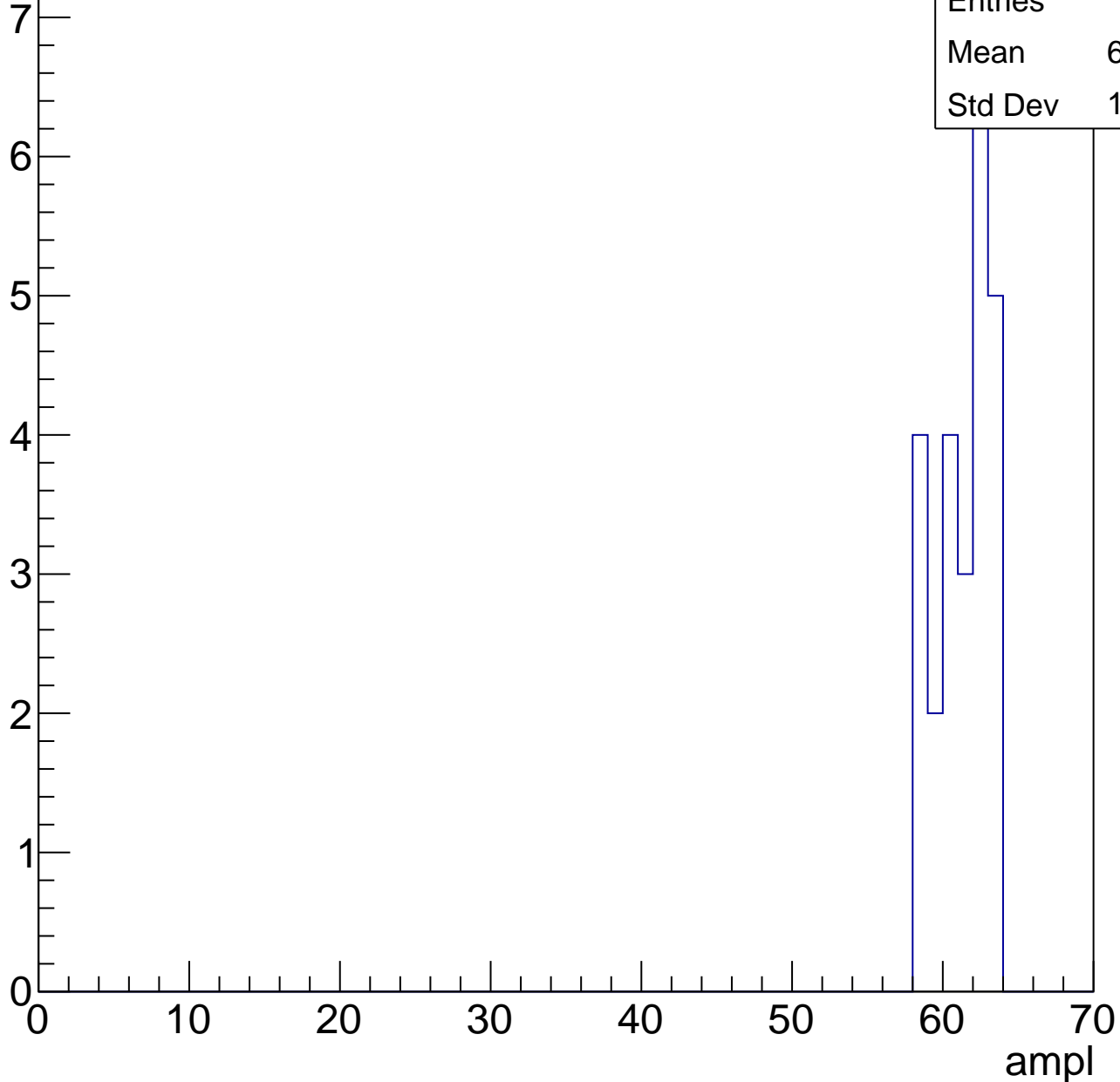


# B0L001S, U17-ch7, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	25
Mean	60.88
Std Dev	1.728



# B0L001S, U17-ch7, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch7, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U17-ch8, adc0

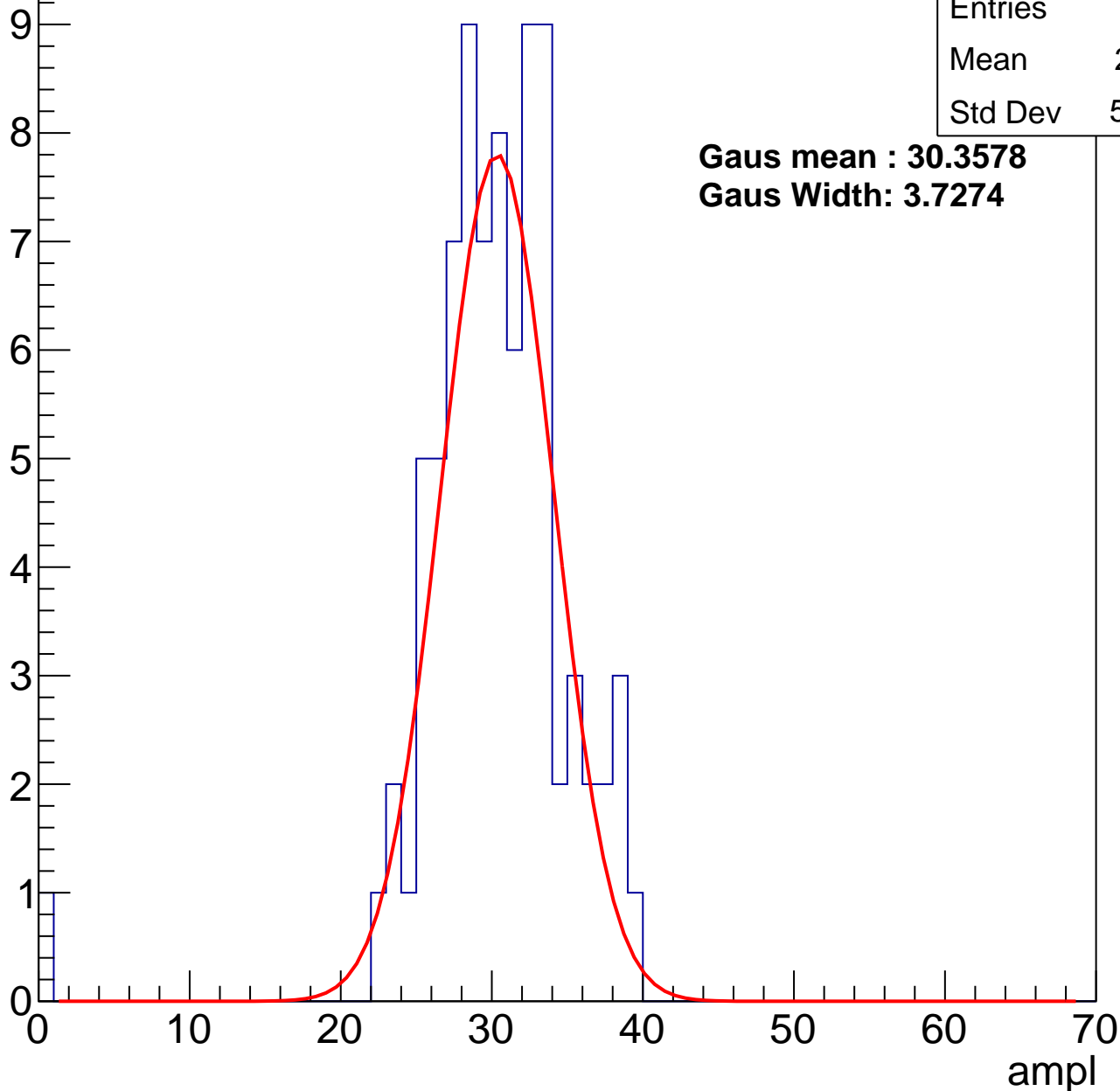
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	83
Mean	29.81
Std Dev	5.005

**Gaus mean : 30.3578**

**Gaus Width: 3.7274**



# B0L001S, U17-ch8, adc1

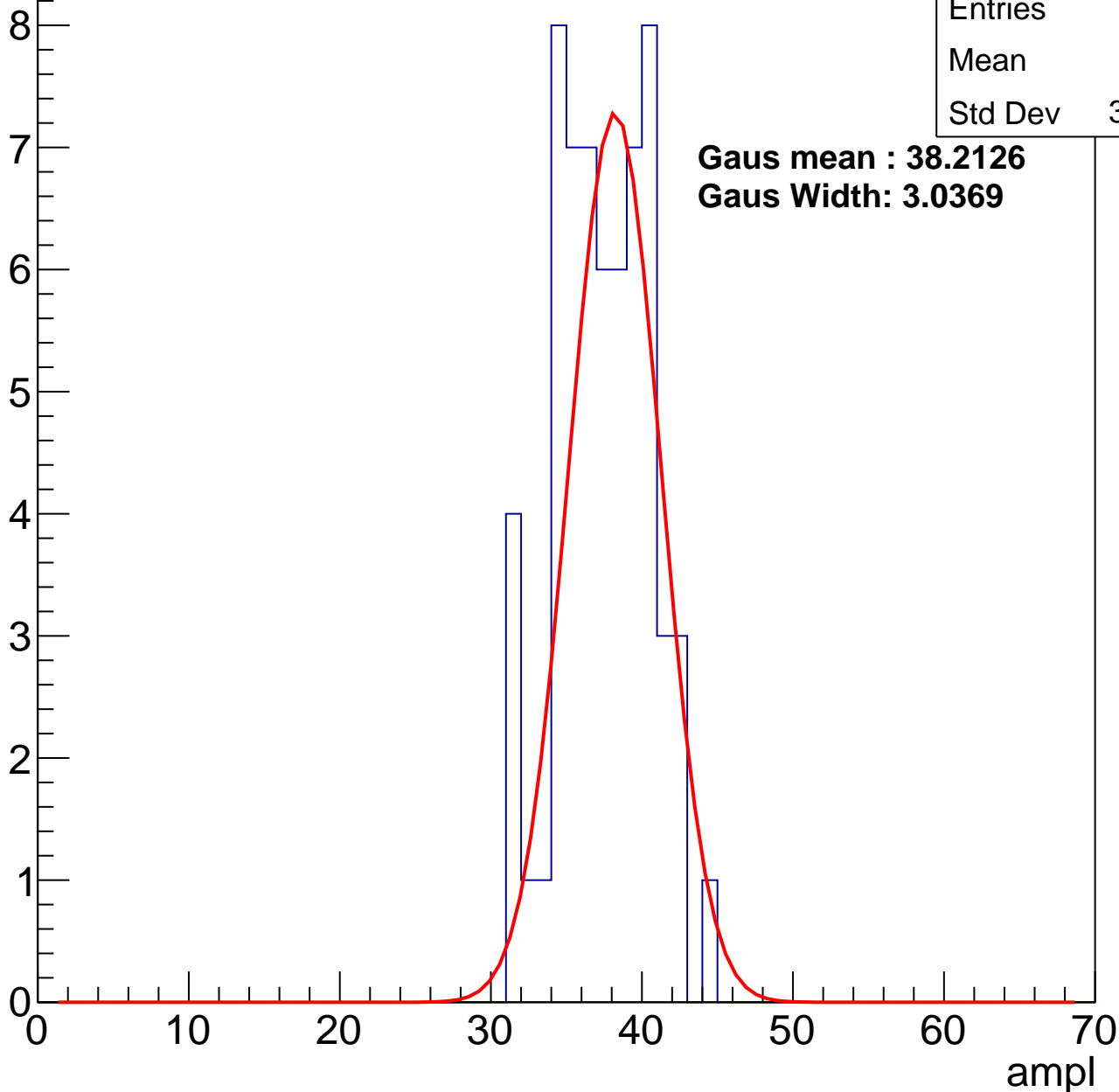
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	37
Std Dev	3.032

**Gaus mean : 38.2126**

**Gaus Width: 3.0369**



# B0L001S, U17-ch8, adc2

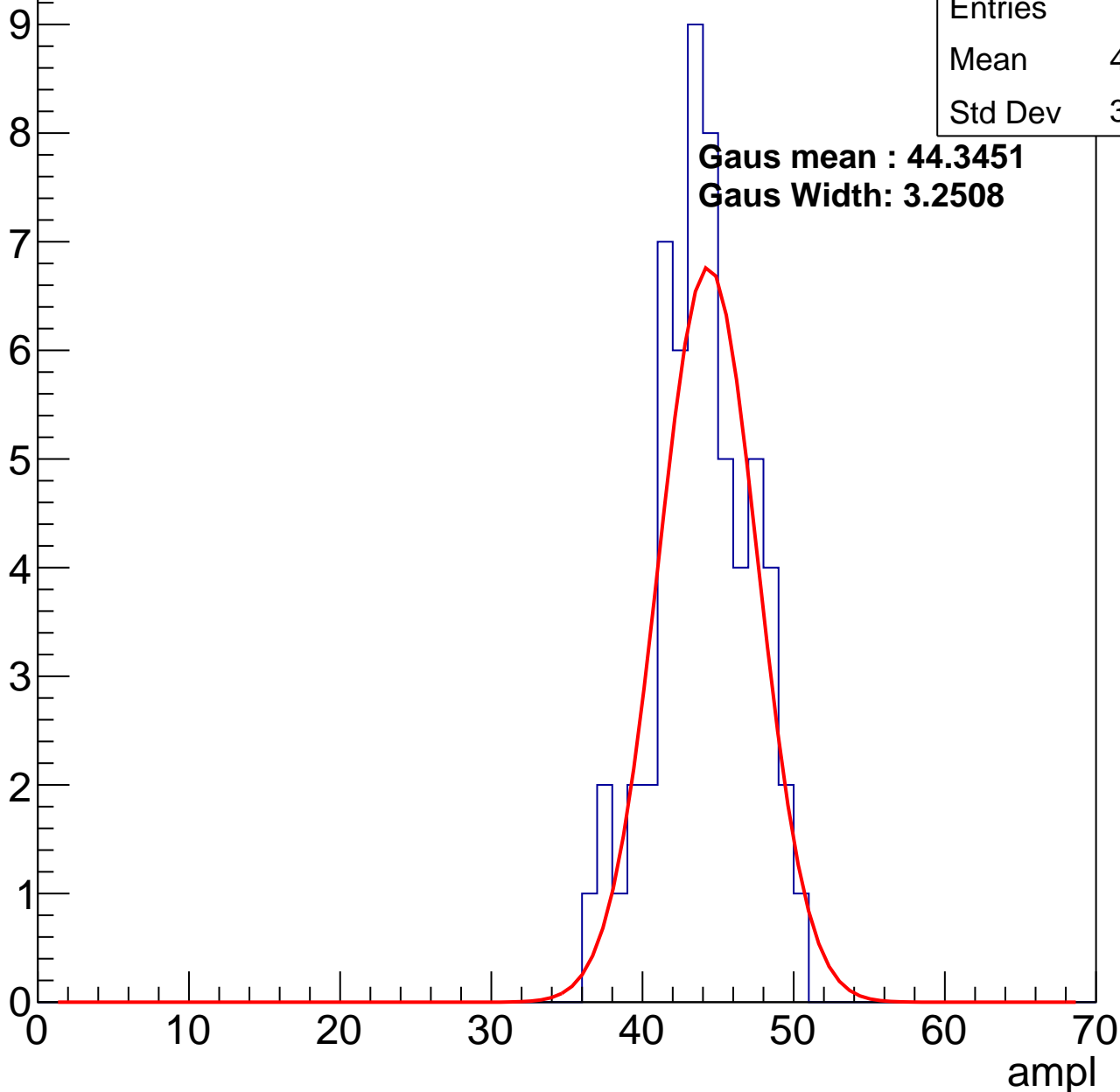
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	43.53
Std Dev	3.132

**Gaus mean : 44.3451**

**Gaus Width: 3.2508**

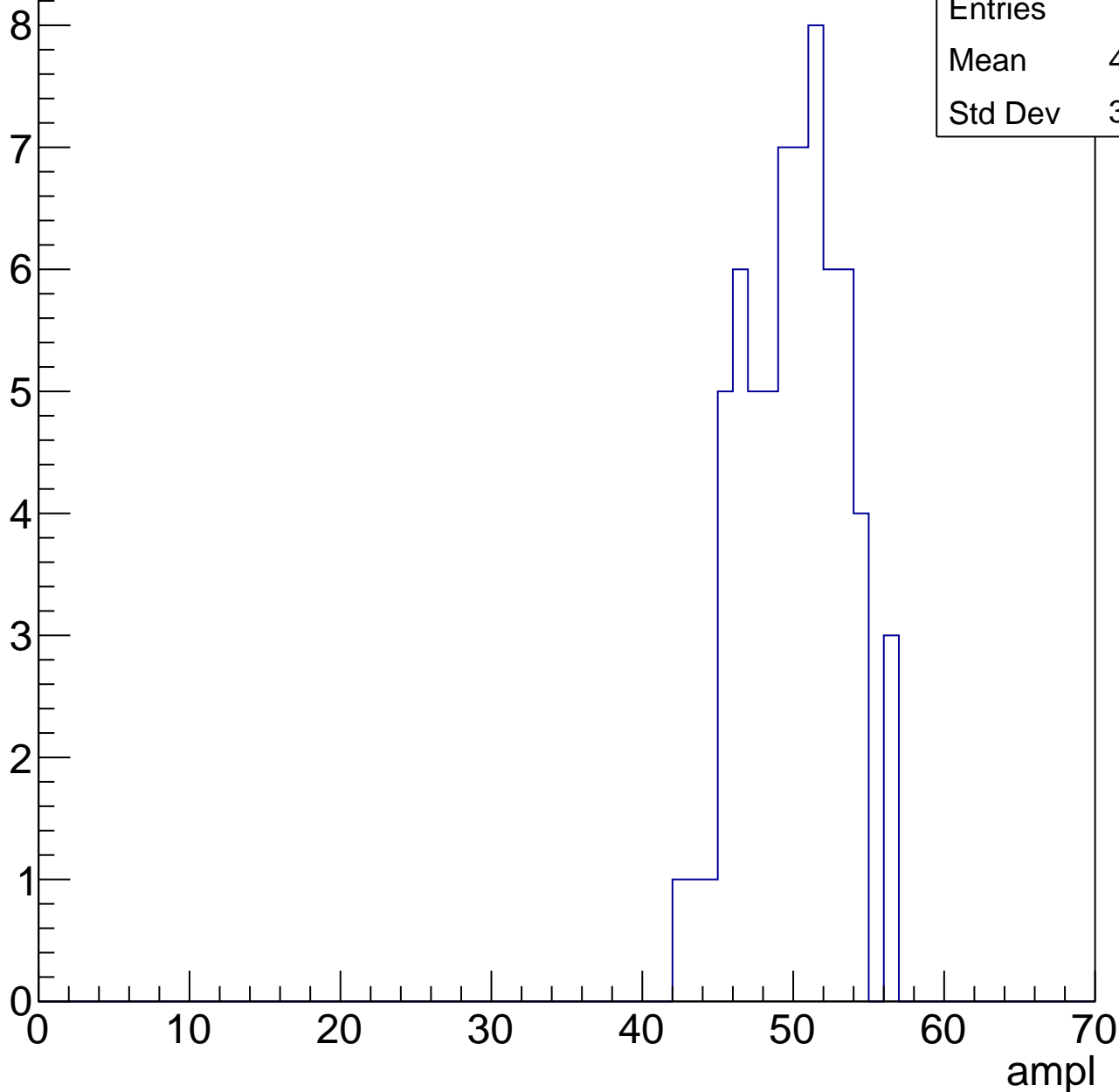


# B0L001S, U17-ch8, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

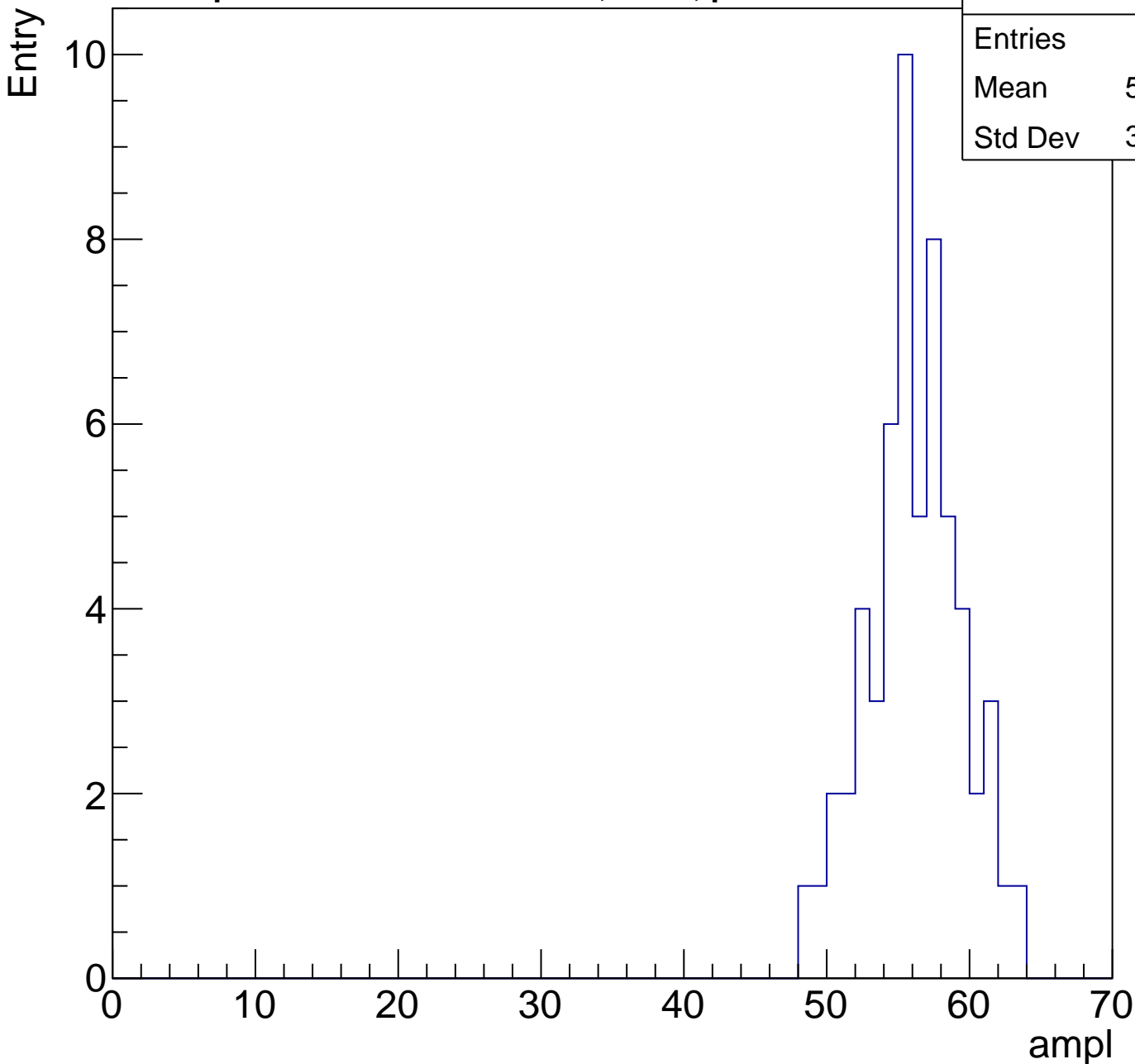
Entries	65
Mean	49.54
Std Dev	3.249



# B0L001S, U17-ch8, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	58
Mean	55.69
Std Dev	3.244

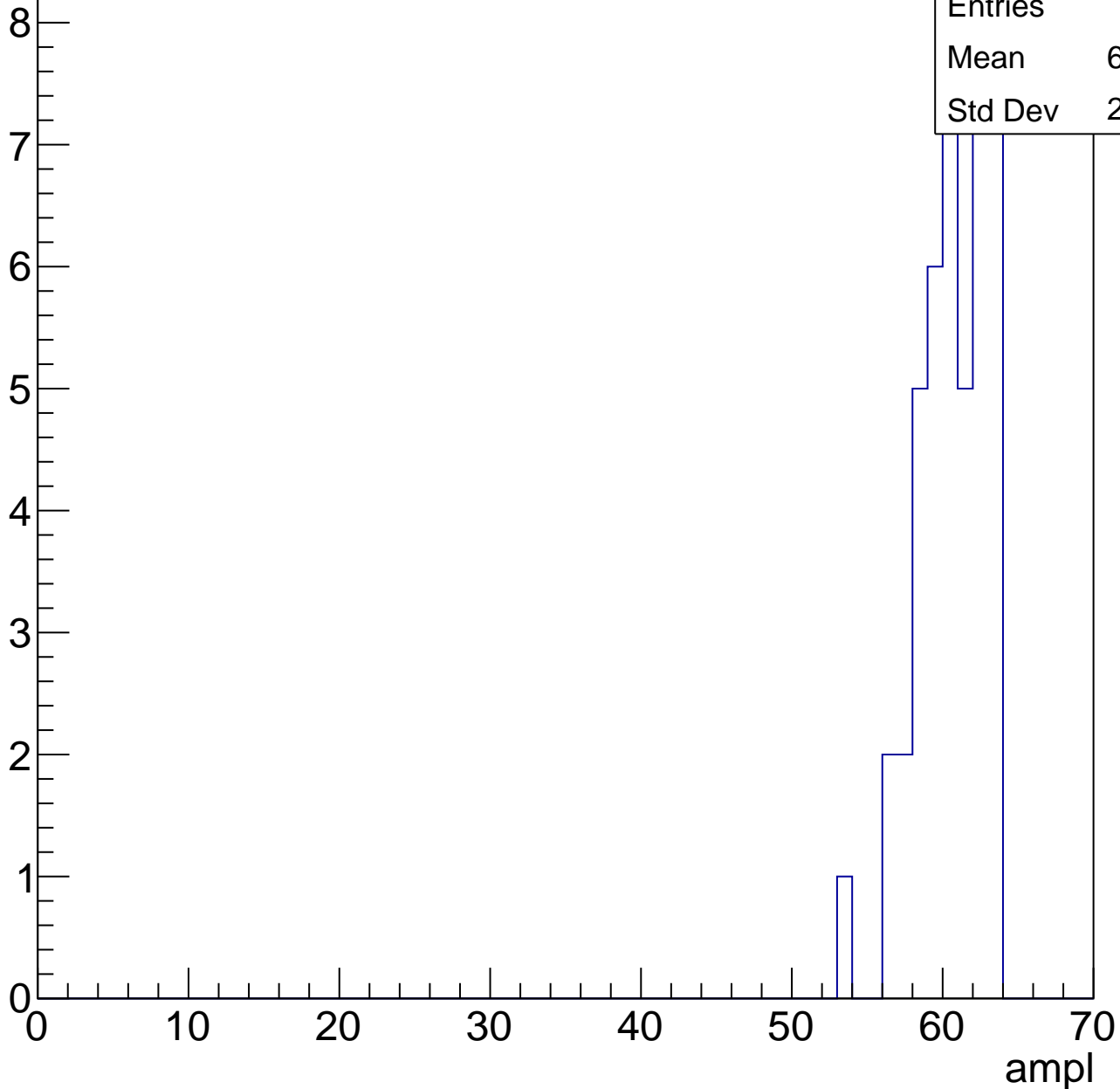


# B0L001S, U17-ch8, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

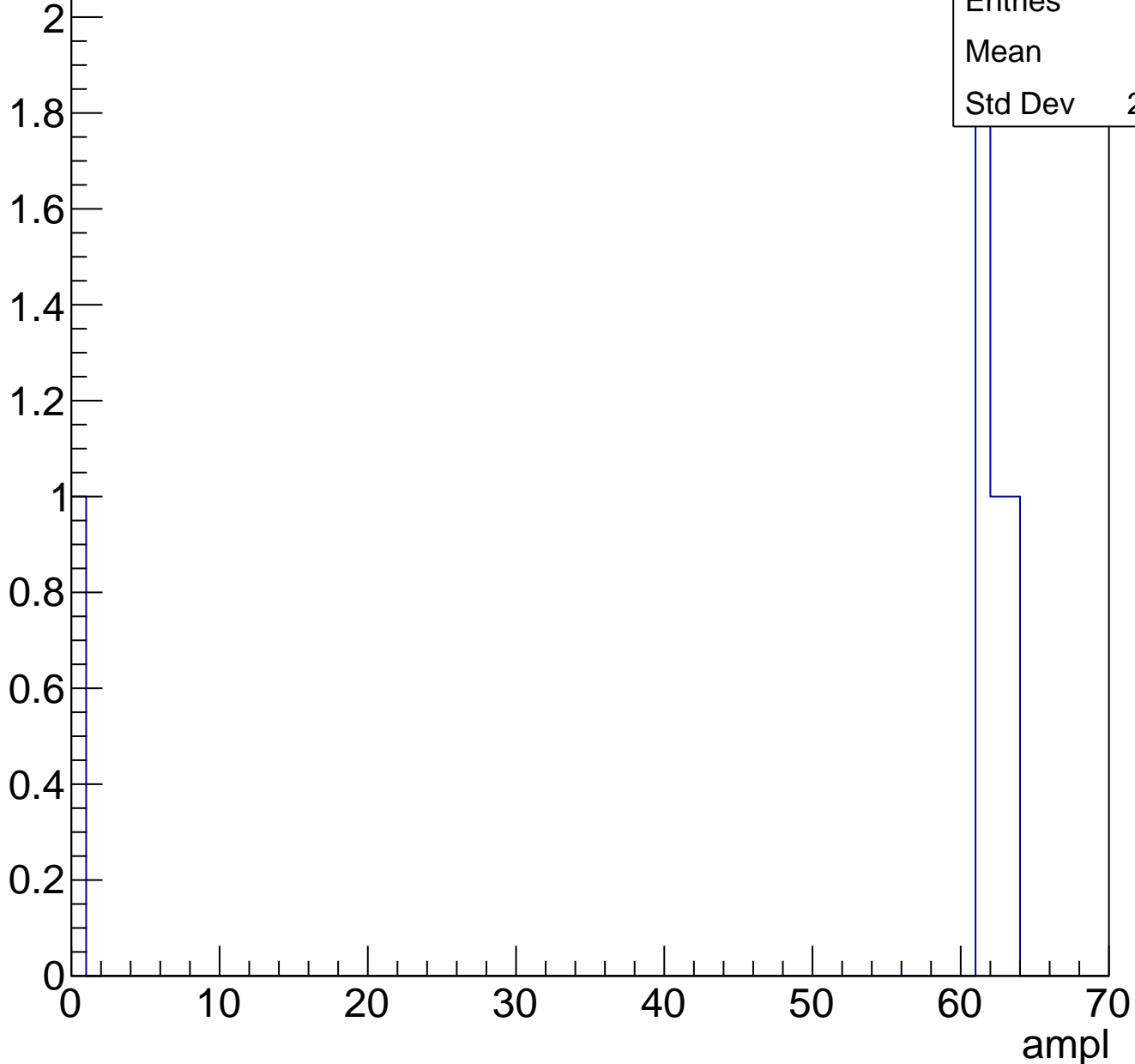
Entries	45
Mean	60.18
Std Dev	2.273



# B0L001S, U17-ch8, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	5
Mean	49.4
Std Dev	24.71



# B0L001S, U17-ch8, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U17-ch9, adc0

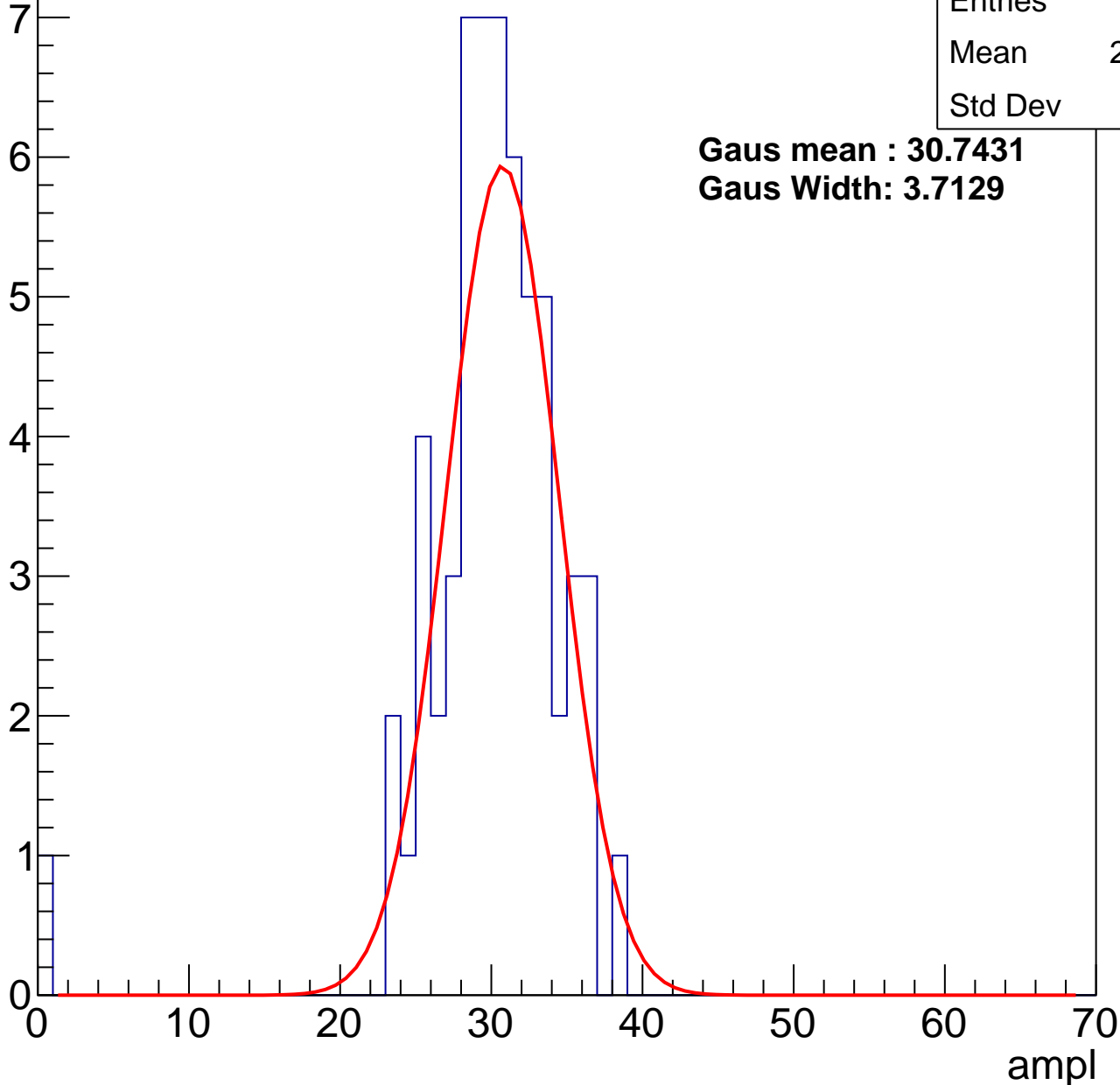
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	29.53
Std Dev	5.15

**Gaus mean : 30.7431**

**Gaus Width: 3.7129**



# B0L001S, U17-ch9, adc1

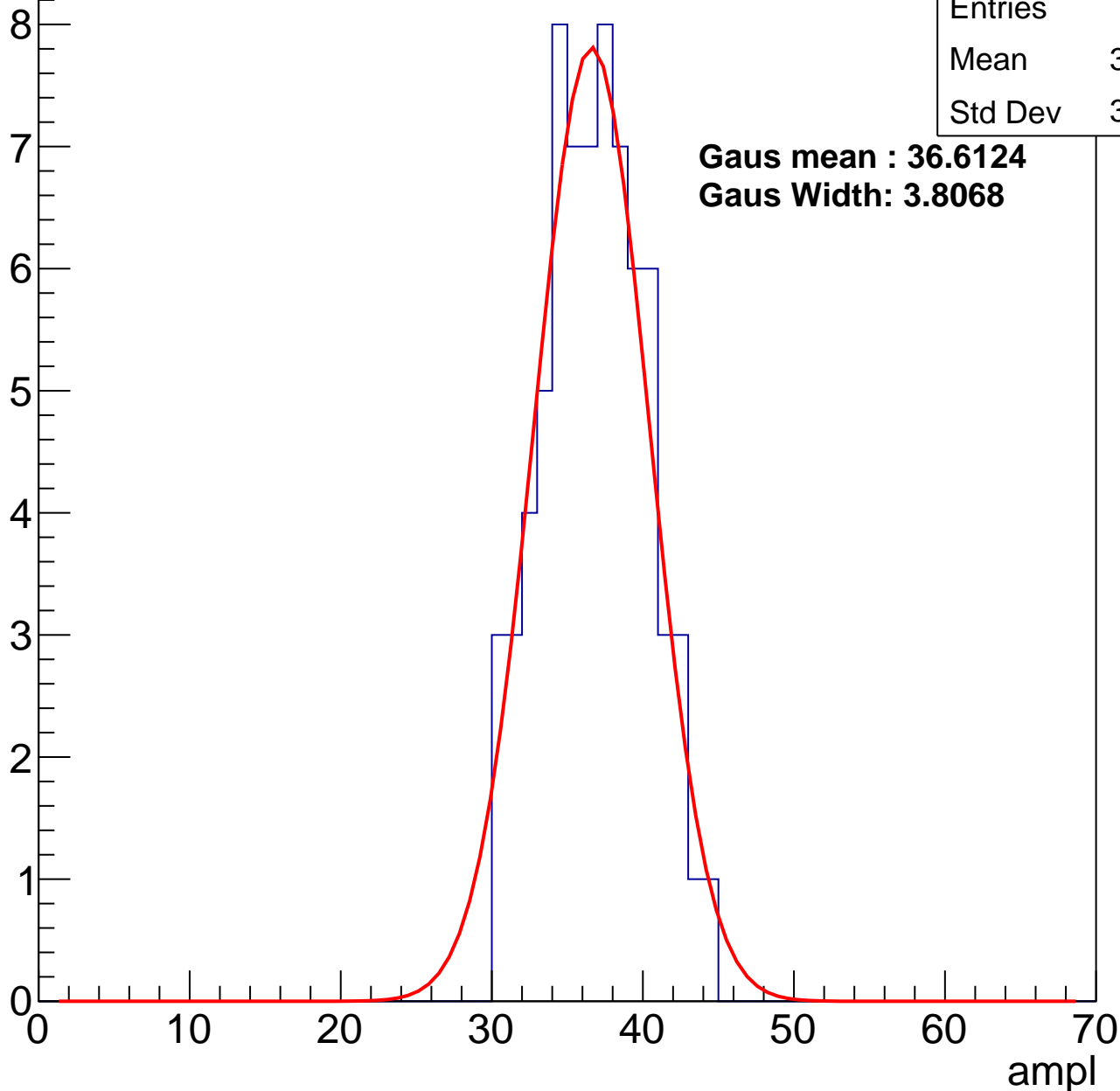
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	36.35
Std Dev	3.342

**Gaus mean : 36.6124**

**Gaus Width: 3.8068**



# B0L001S, U17-ch9, adc2

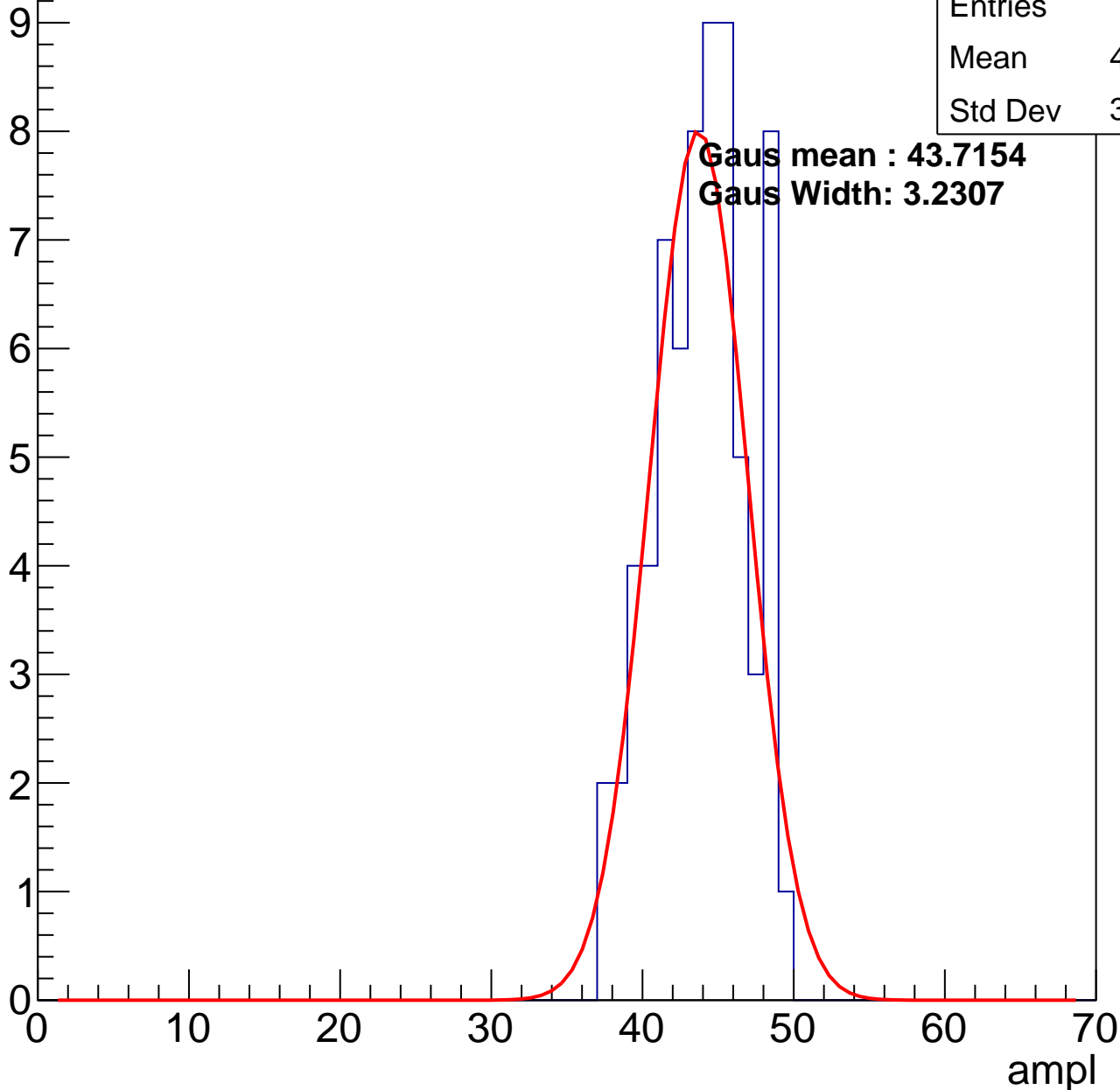
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	43.44
Std Dev	3.012

**Gaus mean : 43.7154**

**Gaus Width: 3.2307**

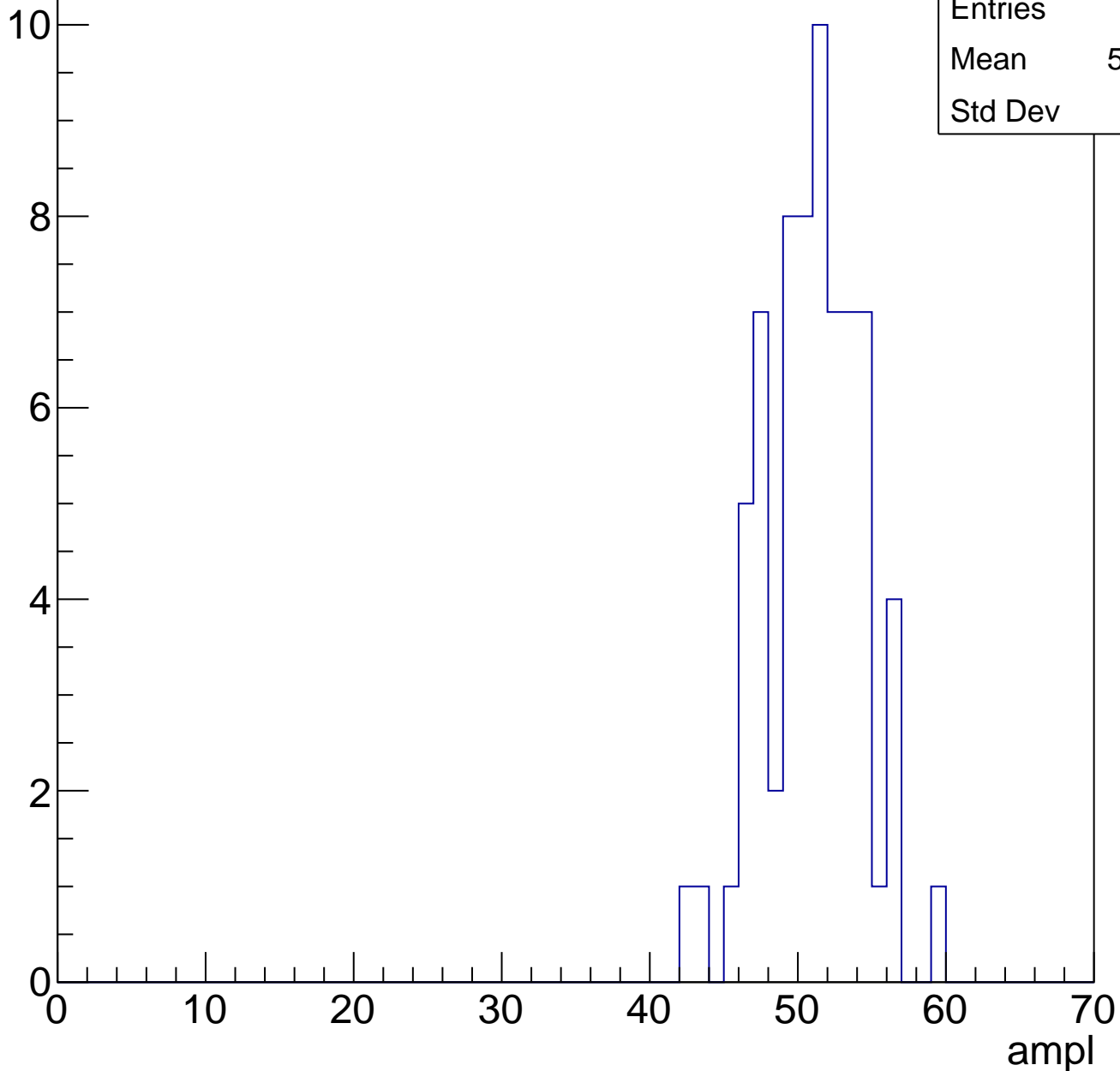


# B0L001S, U17-ch9, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	70
Mean	50.54
Std Dev	3.25

Entry

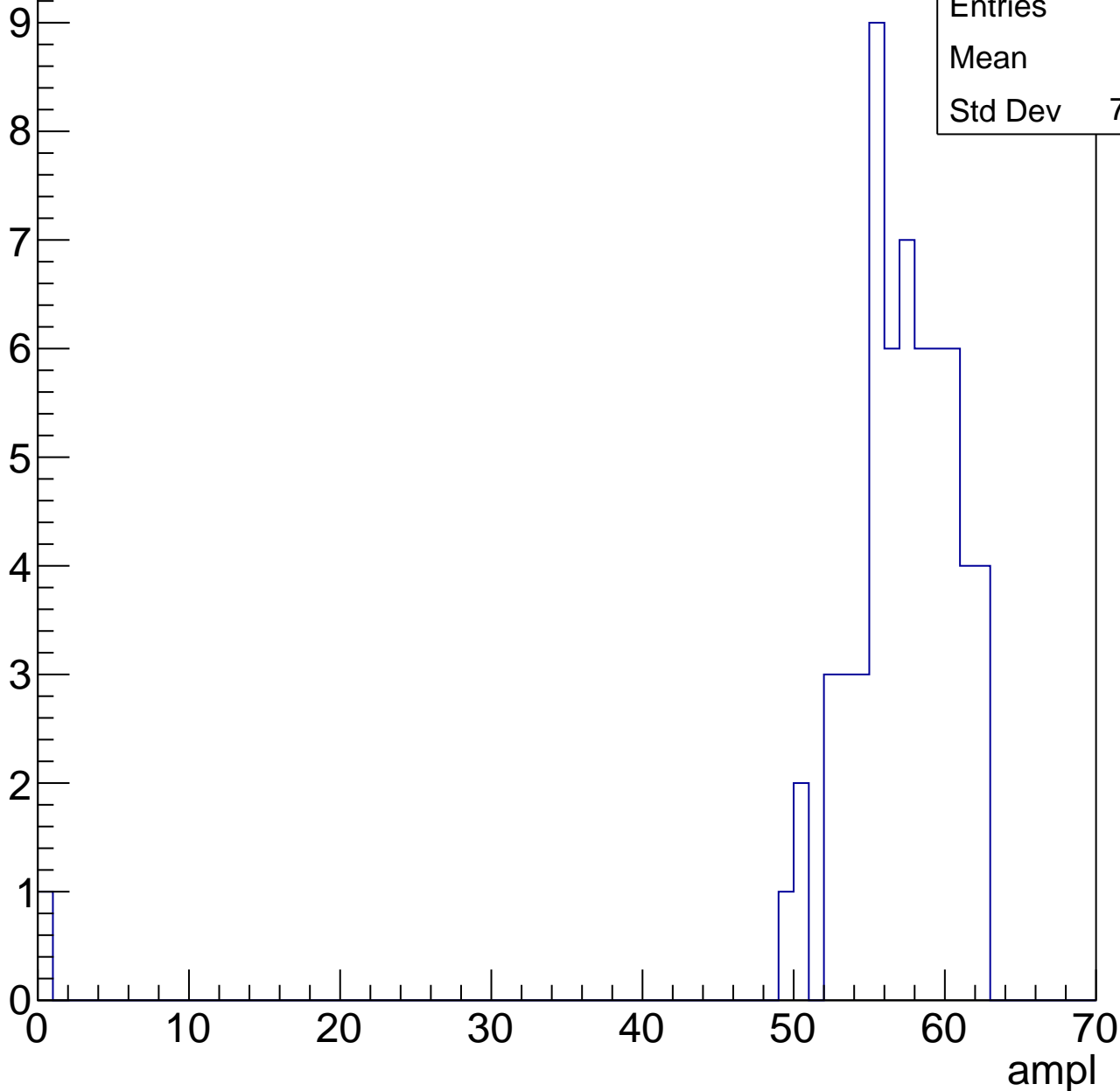


# B0L001S, U17-ch9, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	55.9
Std Dev	7.869



# B0L001S, U17-ch9, adc5

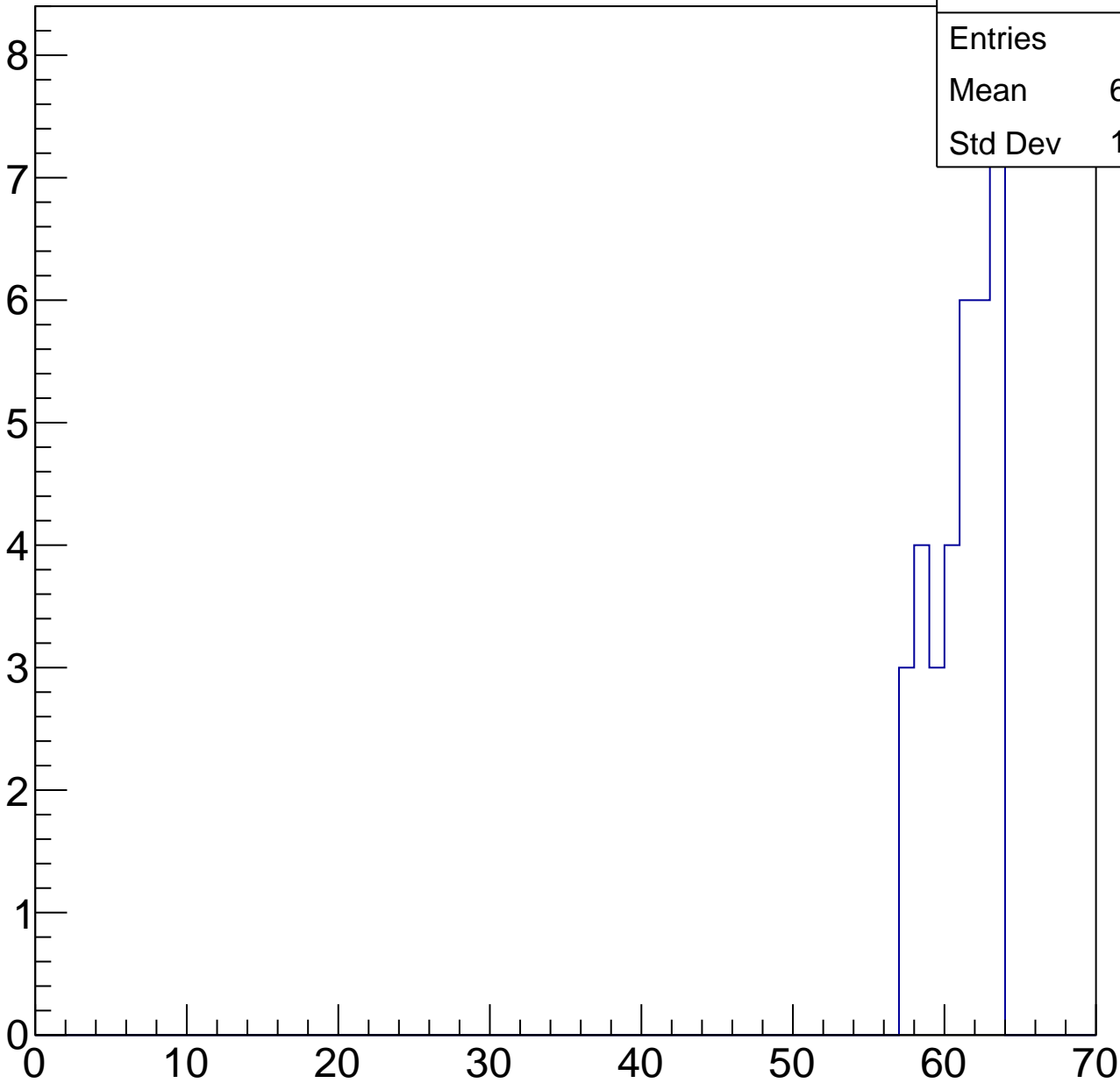
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	34
Mean	60.65
Std Dev	1.983

ampl



# B0L001S, U17-ch9, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch9, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U17-ch10, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	65
Mean	32.23
Std Dev	3.219

**Gaus mean : 32.7391**

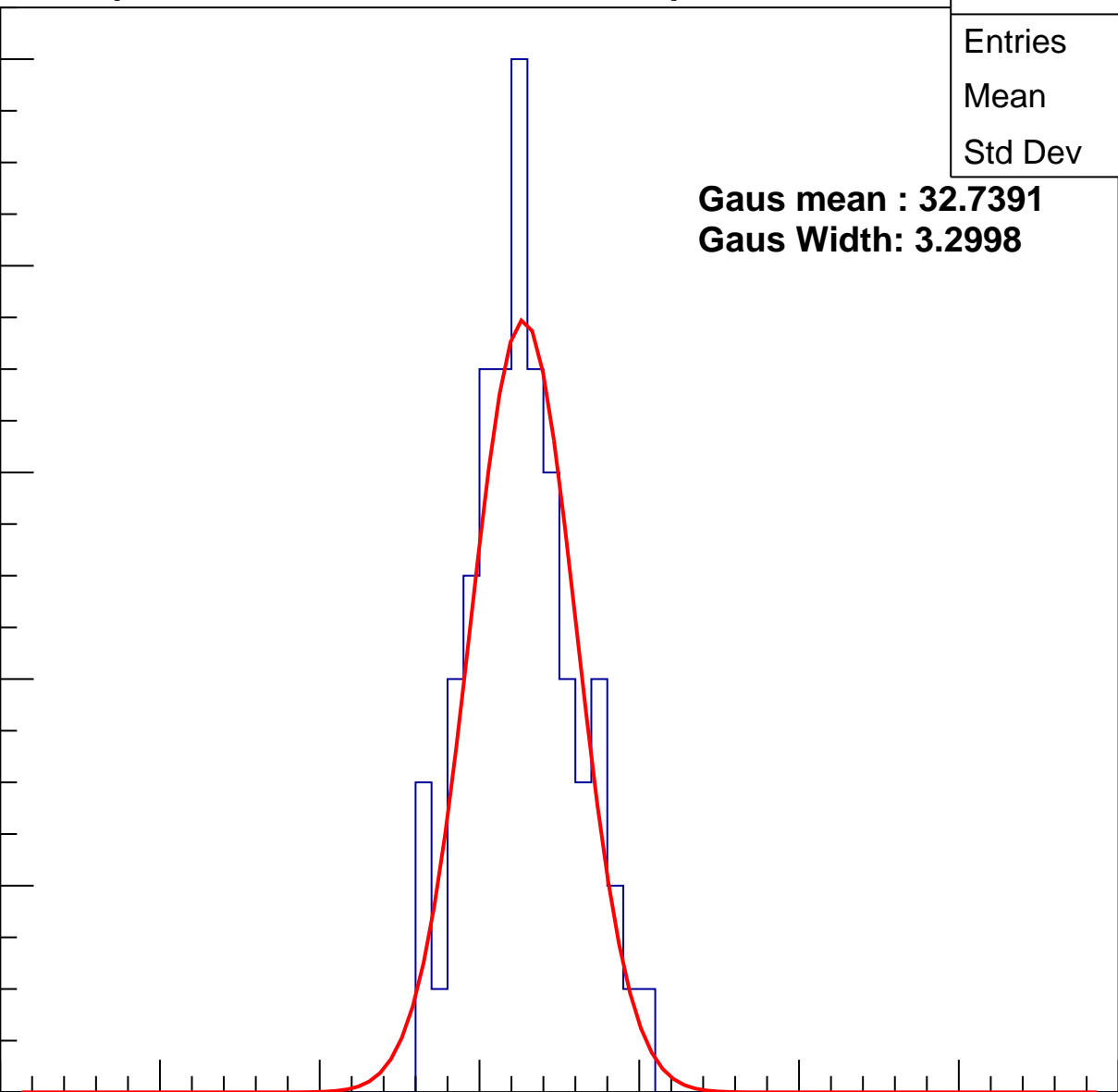
**Gaus Width: 3.2998**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U17-ch10, adc1

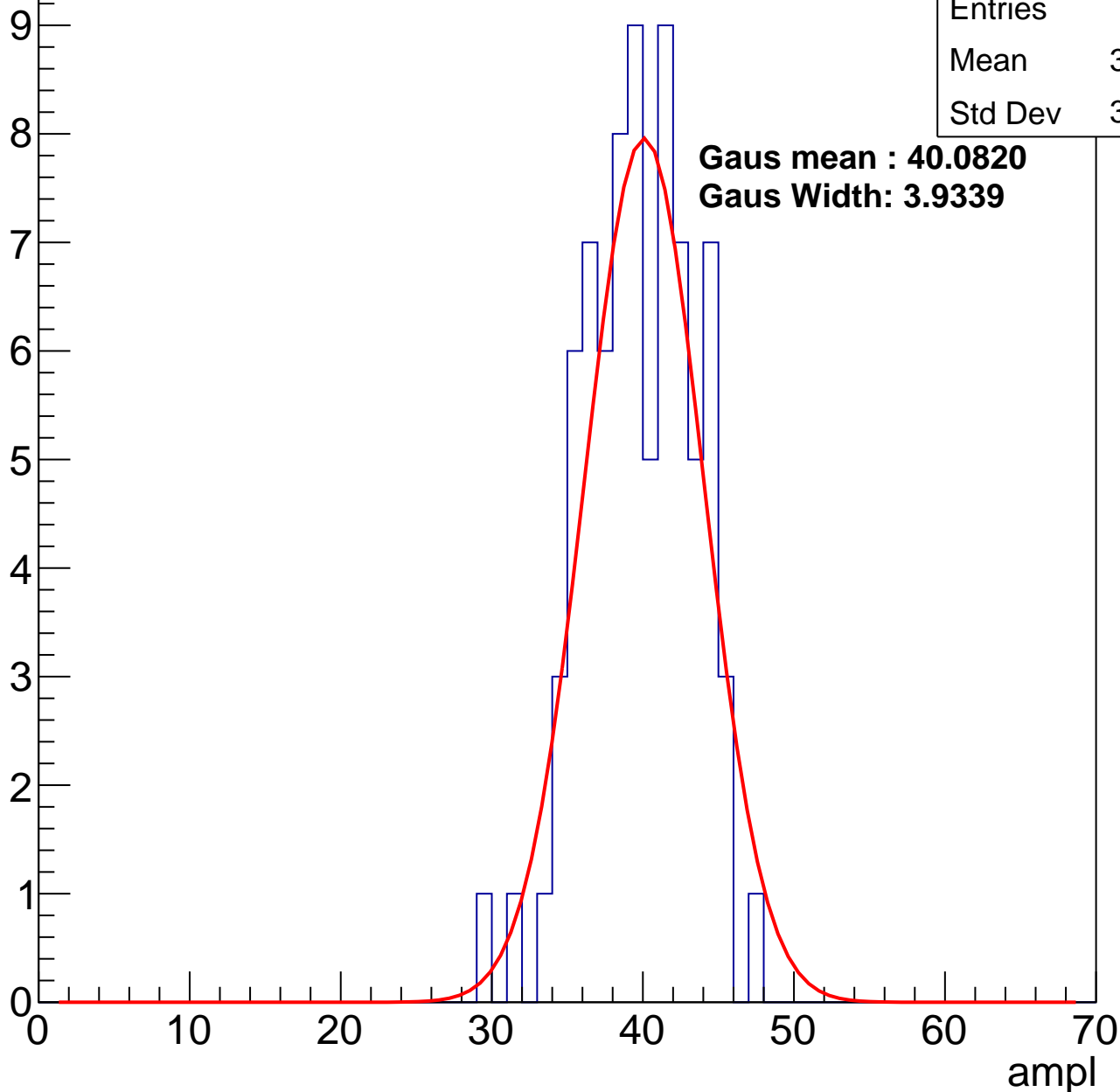
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	79
Mean	39.27
Std Dev	3.543

**Gaus mean : 40.0820**

**Gaus Width: 3.9339**



# B0L001S, U17-ch10, adc2

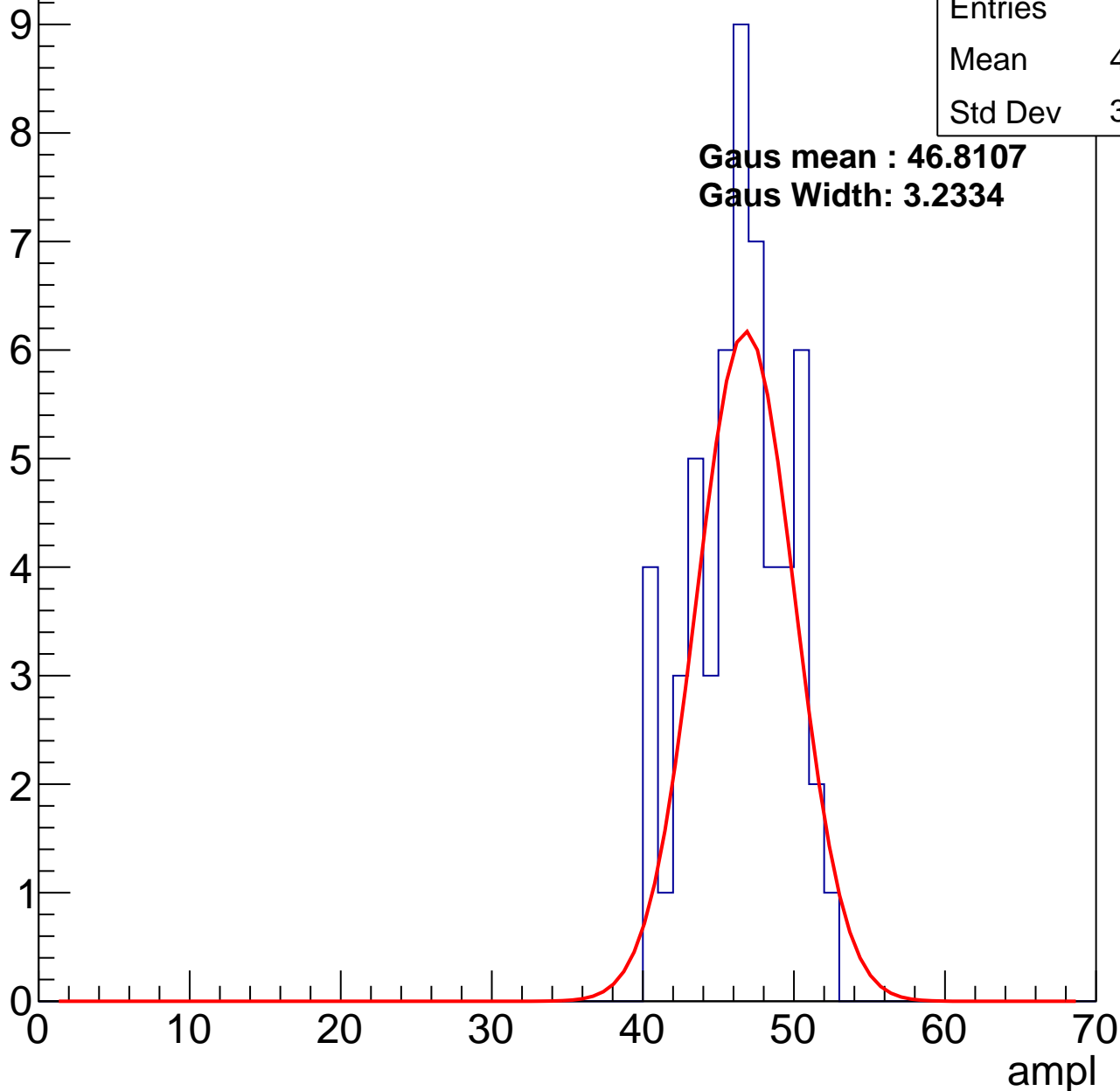
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	45.98
Std Dev	3.078

**Gaus mean : 46.8107**

**Gaus Width: 3.2334**

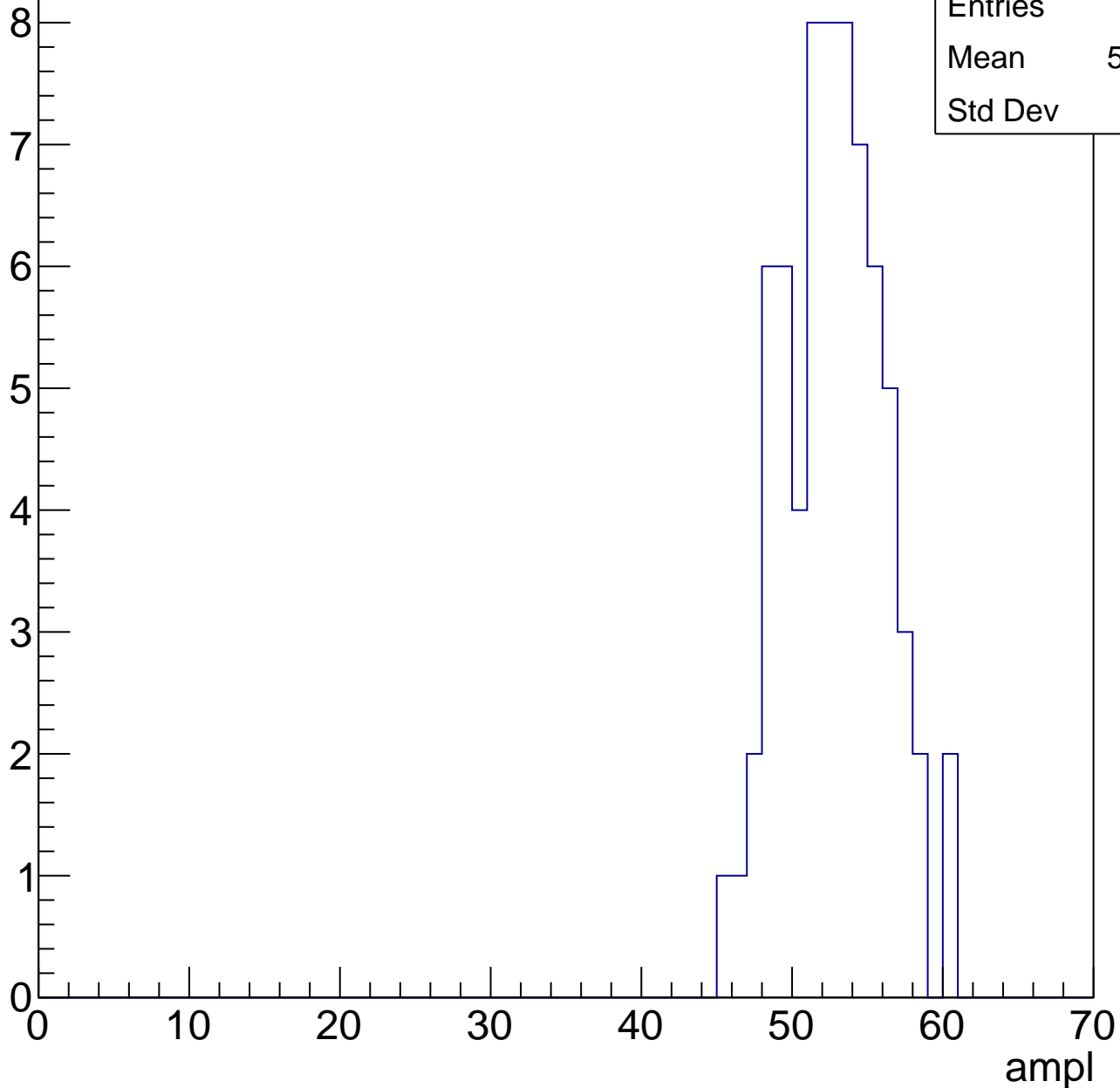


# B0L001S, U17-ch10, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	52.32
Std Dev	3.29

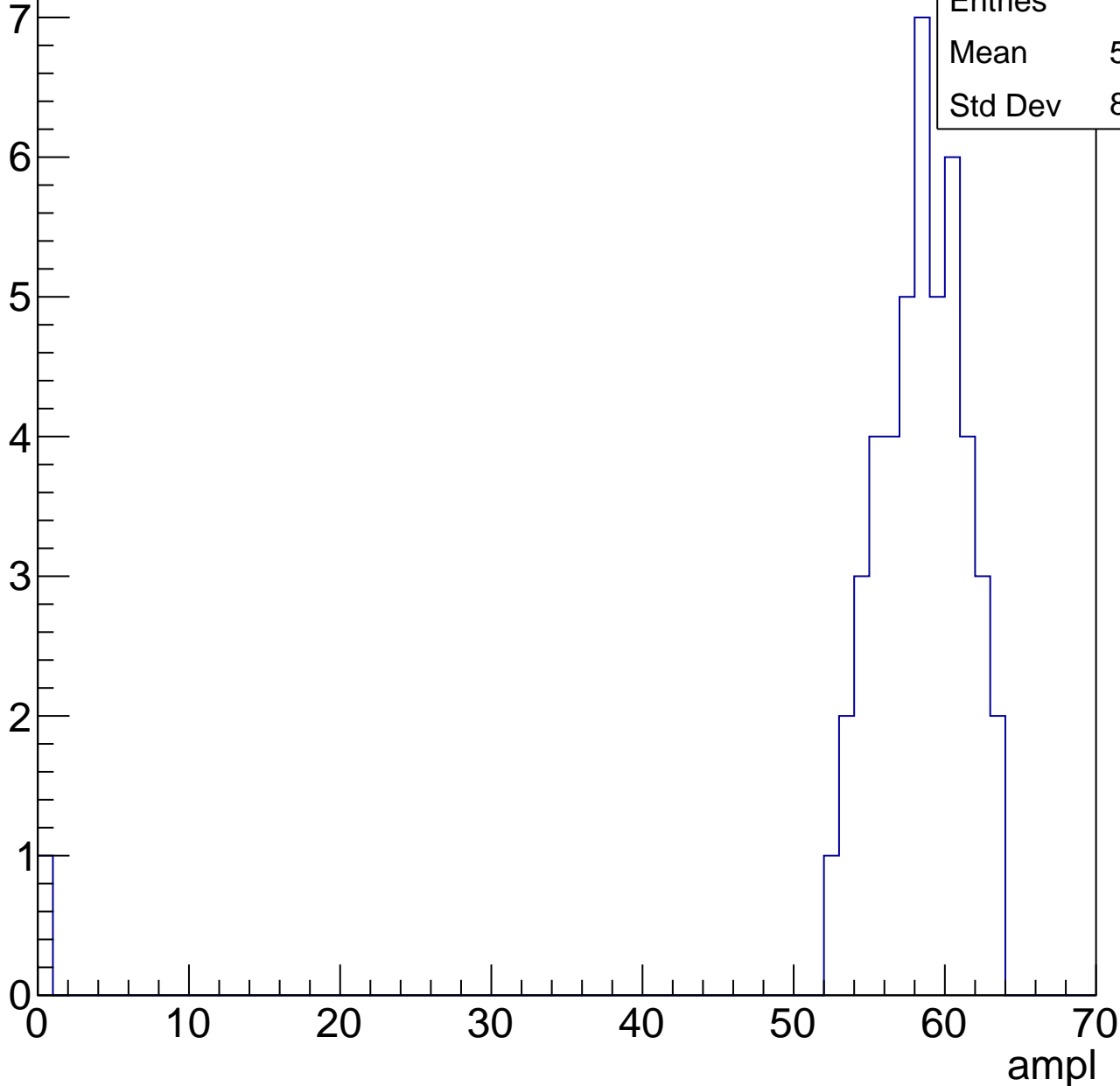


# B0L001S, U17-ch10, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	47
Mean	56.72
Std Dev	8.802

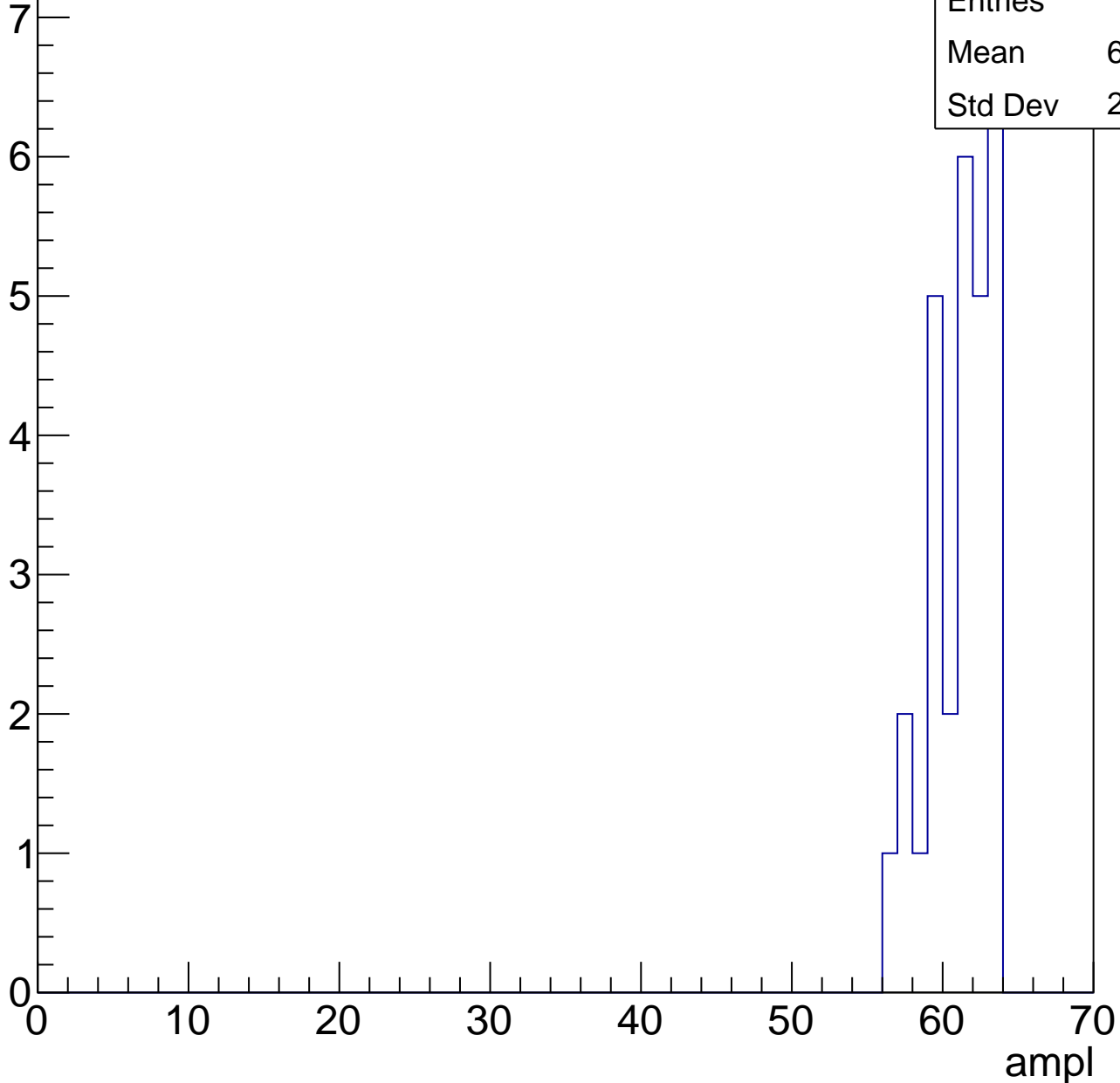


# B0L001S, U17-ch10, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	29
Mean	60.69
Std Dev	2.019



# B0L001S, U17-ch10, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.33
Std Dev	0.4714

ampl

0 10 20 30 40 50 60 70



# B0L001S, U17-ch10, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U17-ch11, adc0

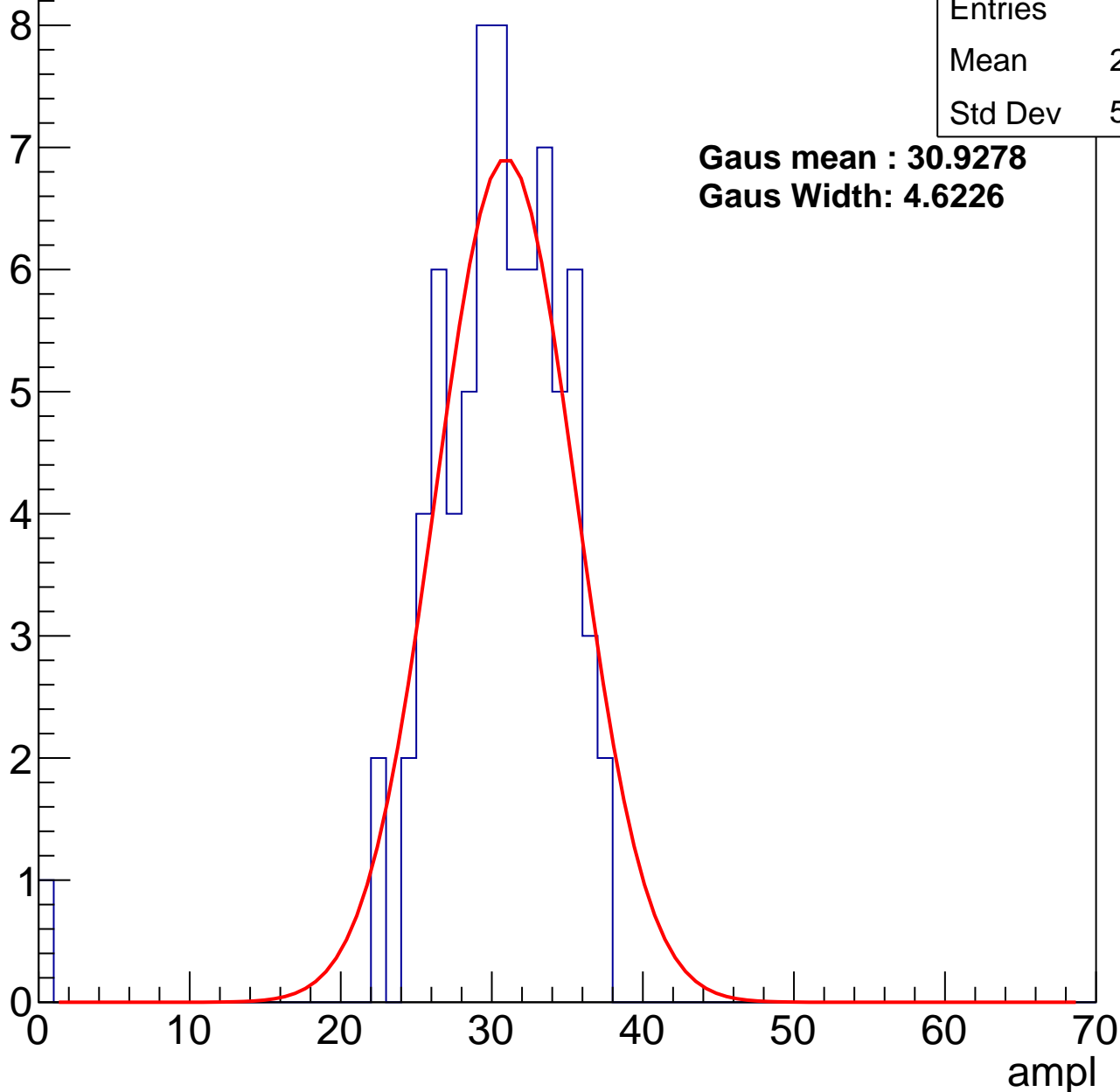
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	75
Mean	29.85
Std Dev	5.016

**Gaus mean : 30.9278**

**Gaus Width: 4.6226**



# B0L001S, U17-ch11, adc1

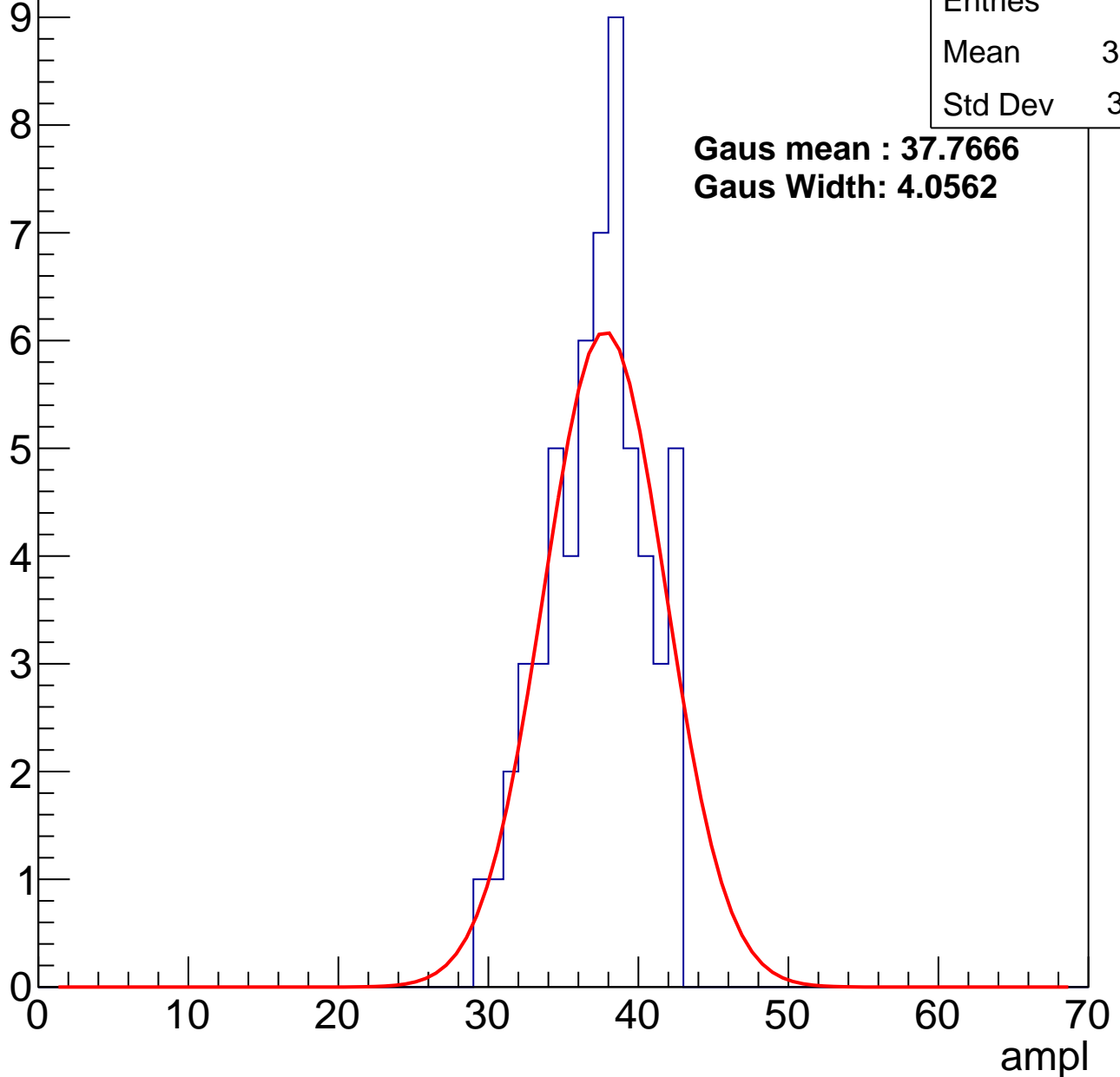
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	36.74
Std Dev	3.241

**Gaus mean : 37.7666**

**Gaus Width: 4.0562**



# B0L001S, U17-ch11, adc2

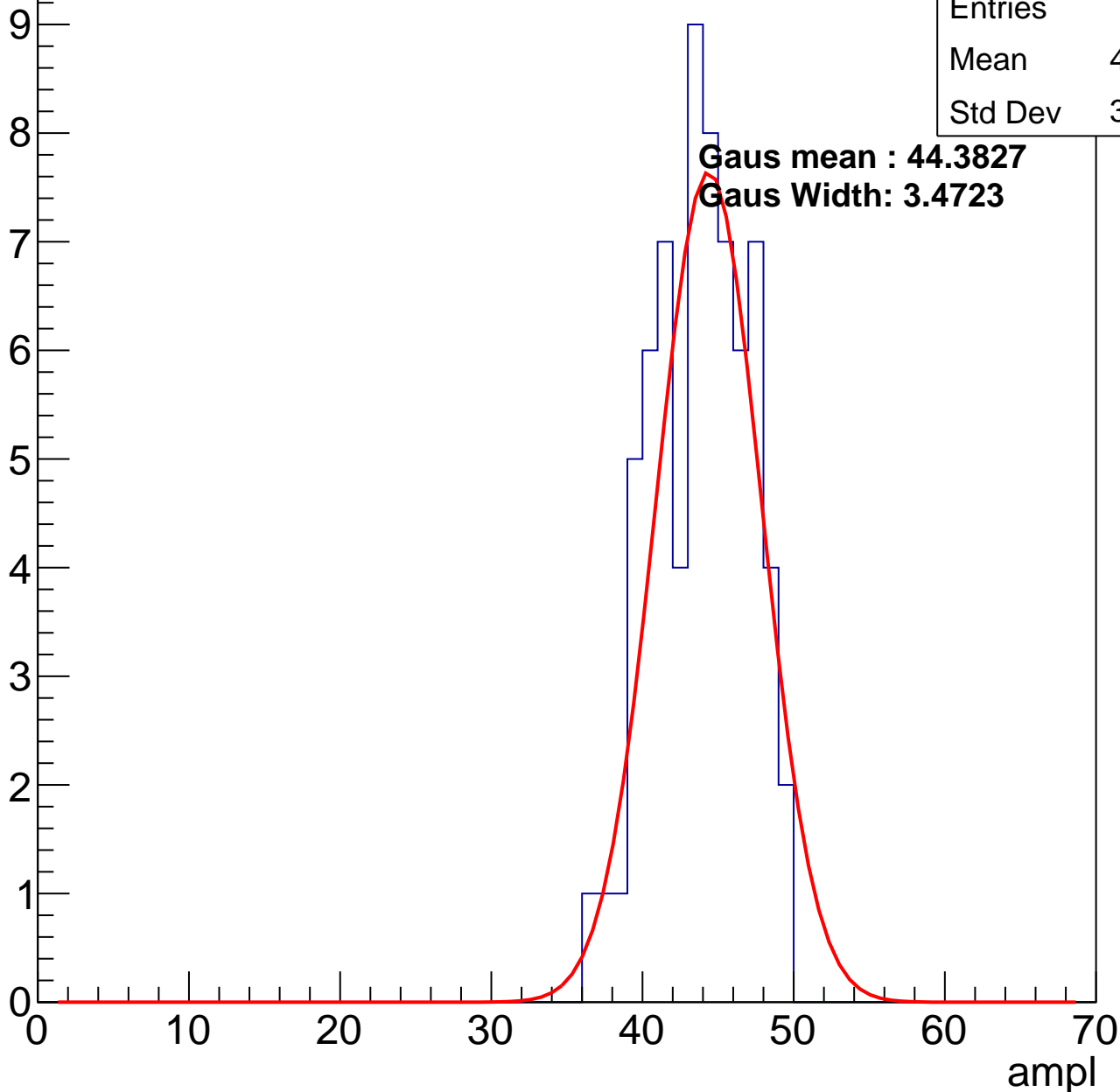
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	43.38
Std Dev	3.068

**Gaus mean : 44.3827**

**Gaus Width: 3.4723**

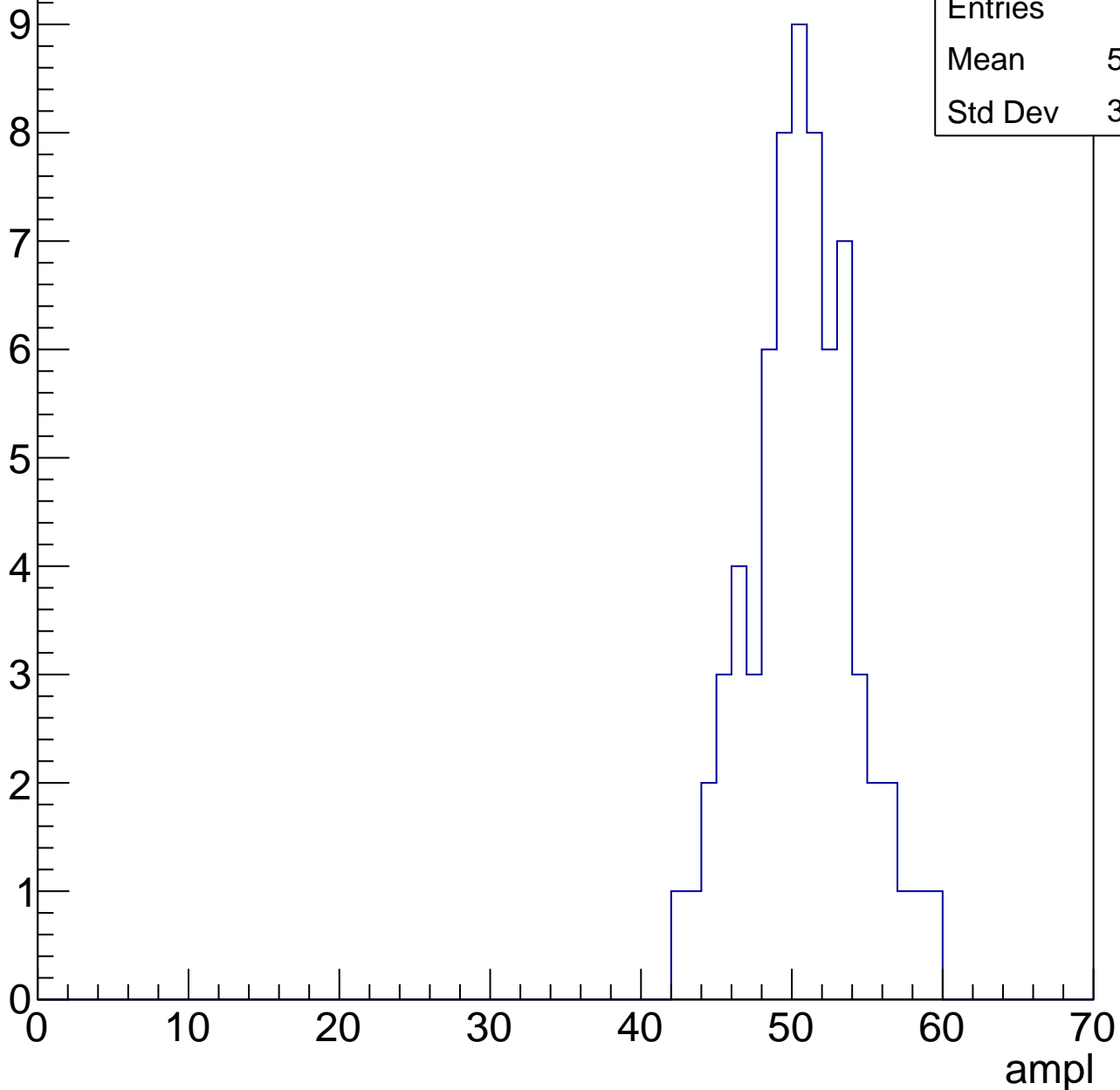


# B0L001S, U17-ch11, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	50.18
Std Dev	3.514

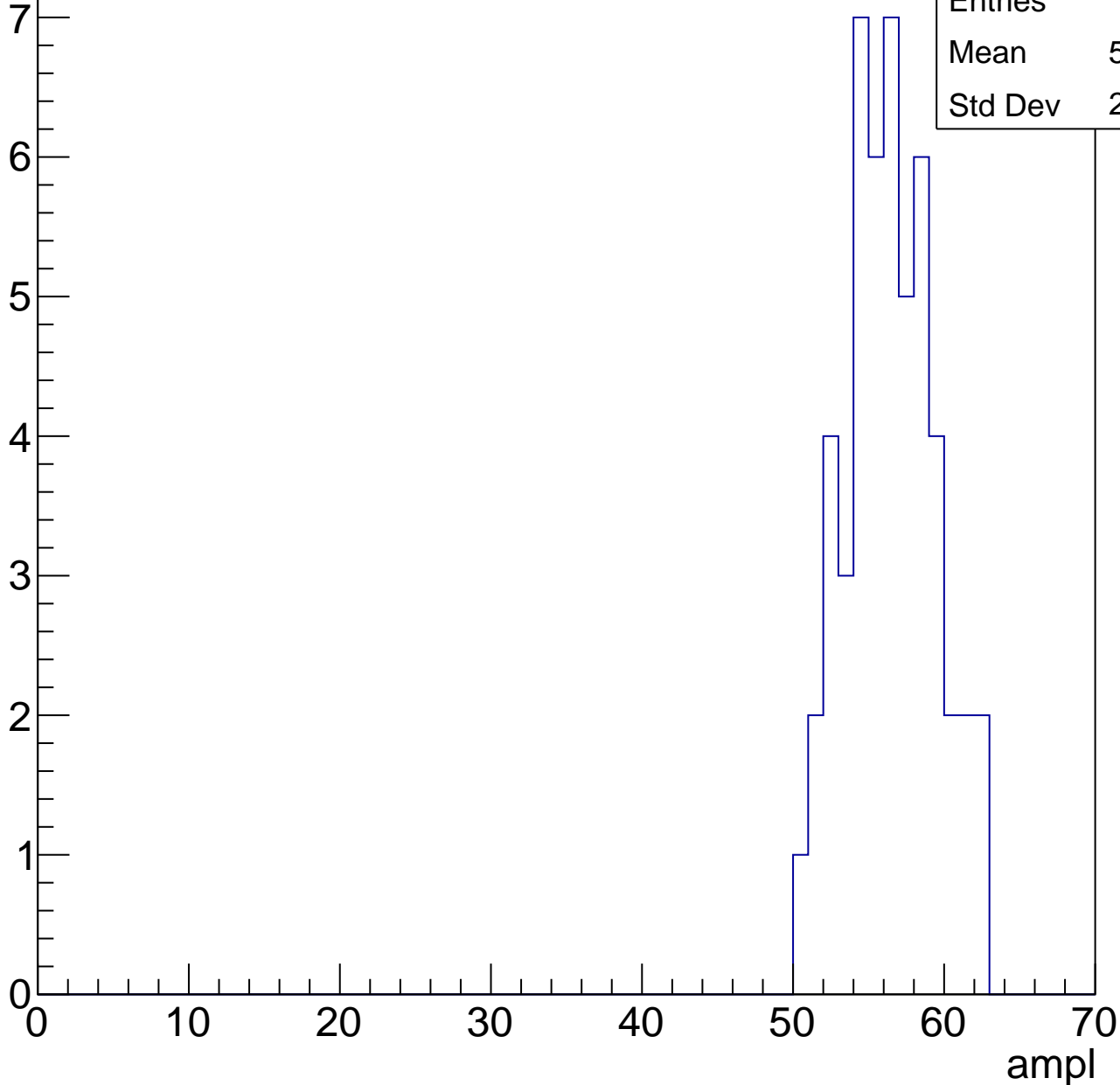


# B0L001S, U17-ch11, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	51
Mean	55.96
Std Dev	2.903

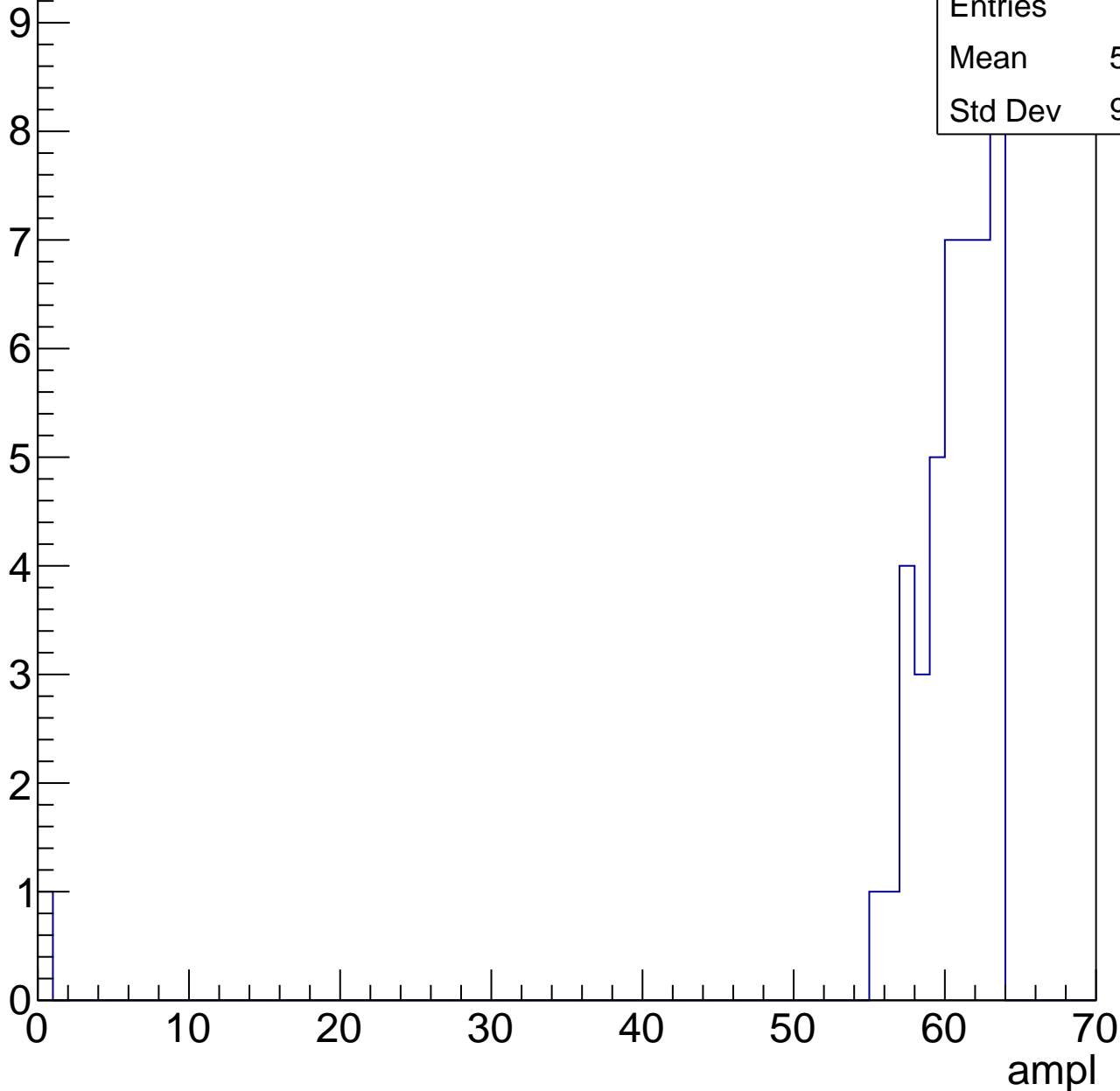


# B0L001S, U17-ch11, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	45
Mean	59.02
Std Dev	9.149



# B0L001S, U17-ch11, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	60.2
Std Dev	2.786

ampl

0 10 20 30 40 50 60 70



# B0L001S, U17-ch11, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U17-ch12, adc0

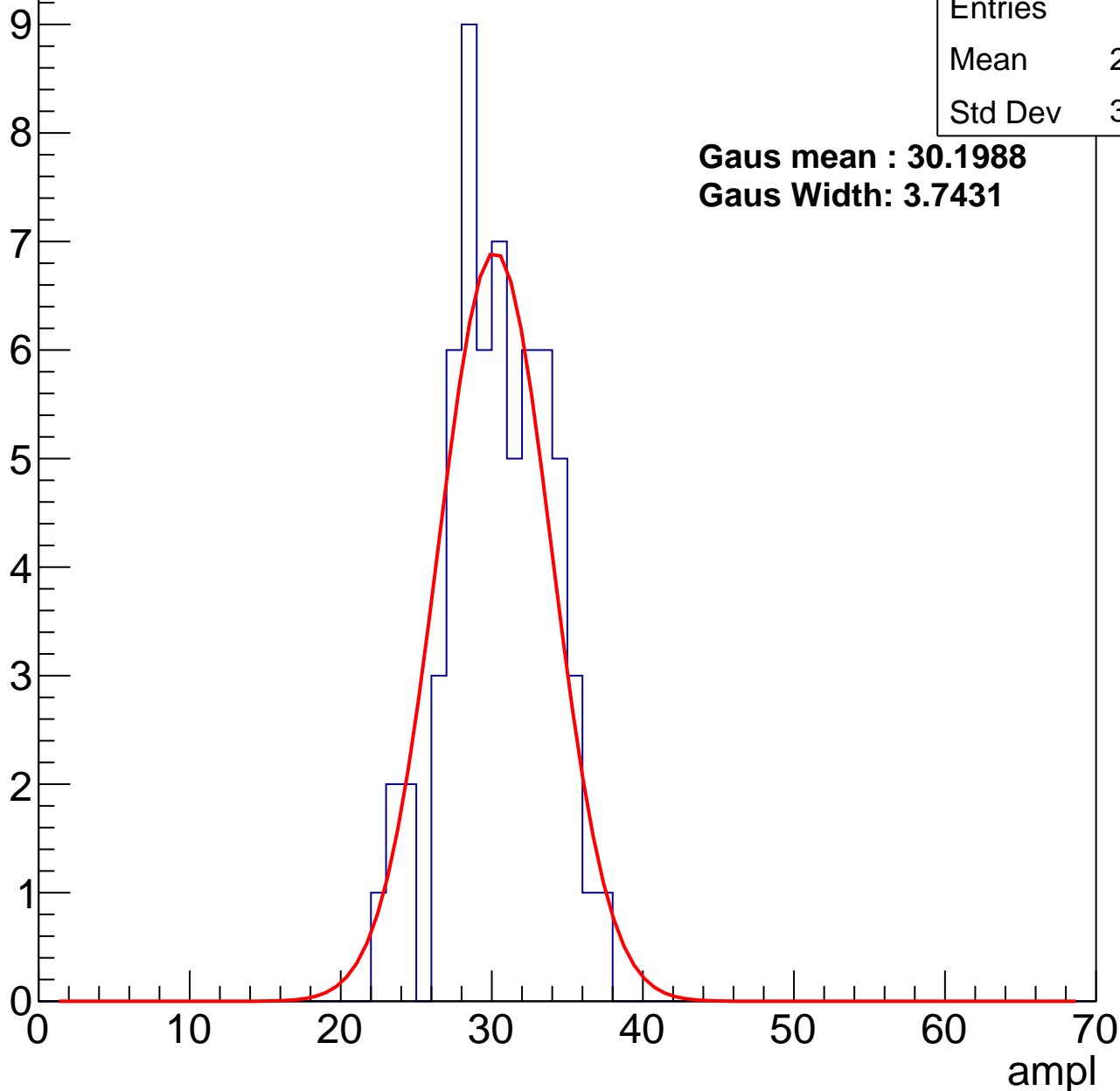
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	29.92
Std Dev	3.335

**Gaus mean : 30.1988**

**Gaus Width: 3.7431**



# B0L001S, U17-ch12, adc1

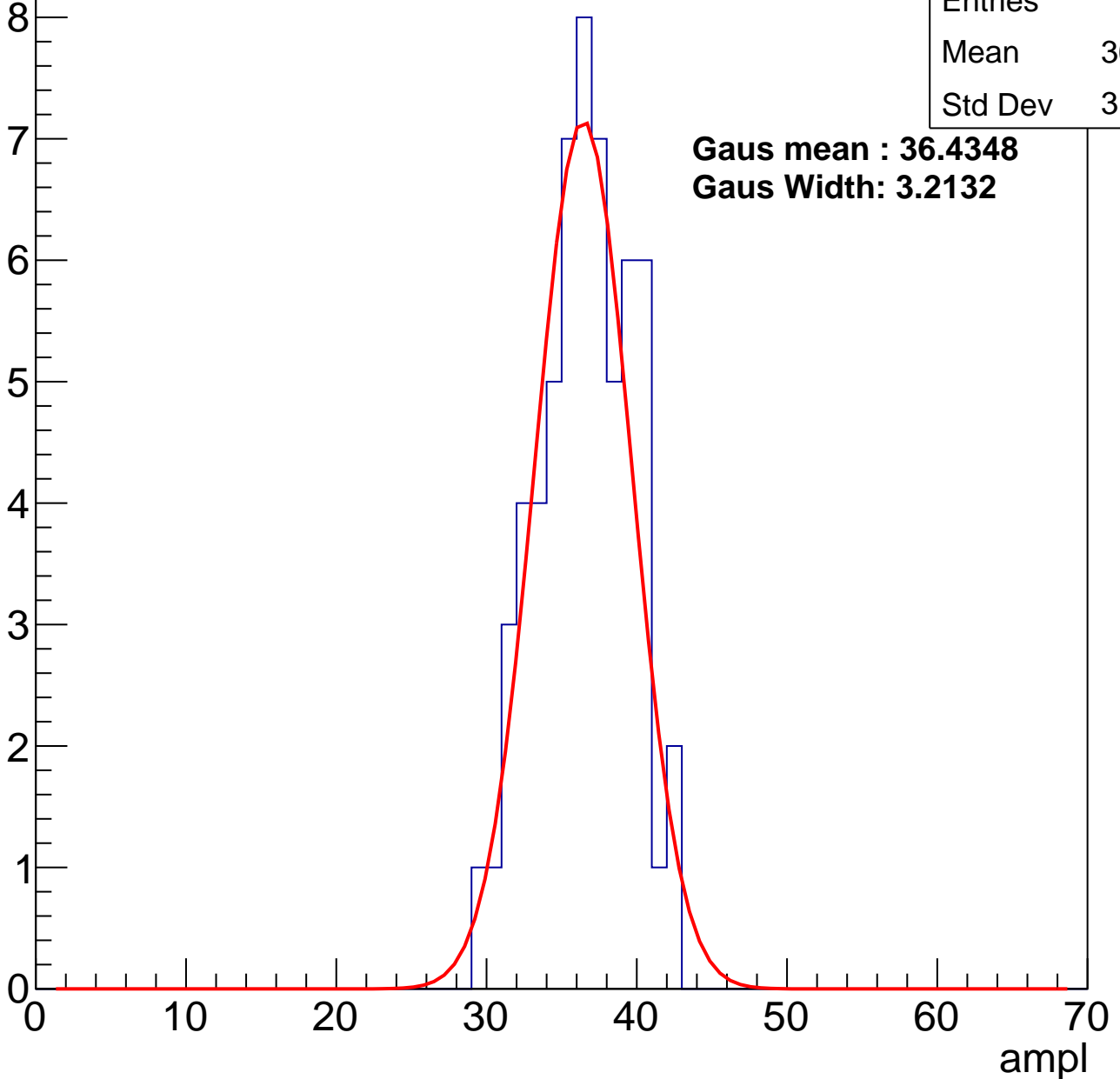
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	36.05
Std Dev	3.057

**Gaus mean : 36.4348**

**Gaus Width: 3.2132**



# B0L001S, U17-ch12, adc2

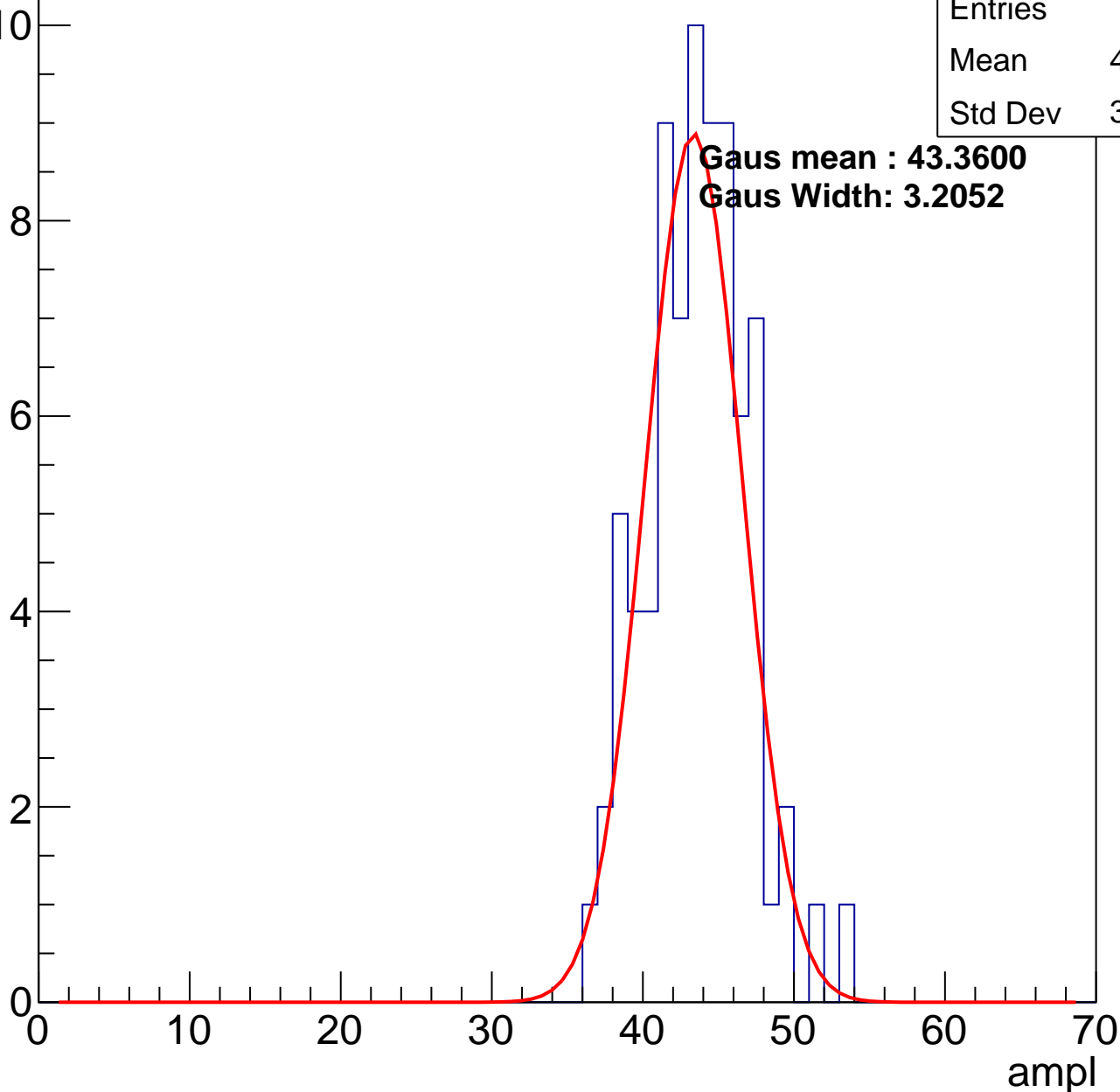
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	78
Mean	43.14
Std Dev	3.319

**Gaus mean : 43.3600**

**Gaus Width: 3.2052**

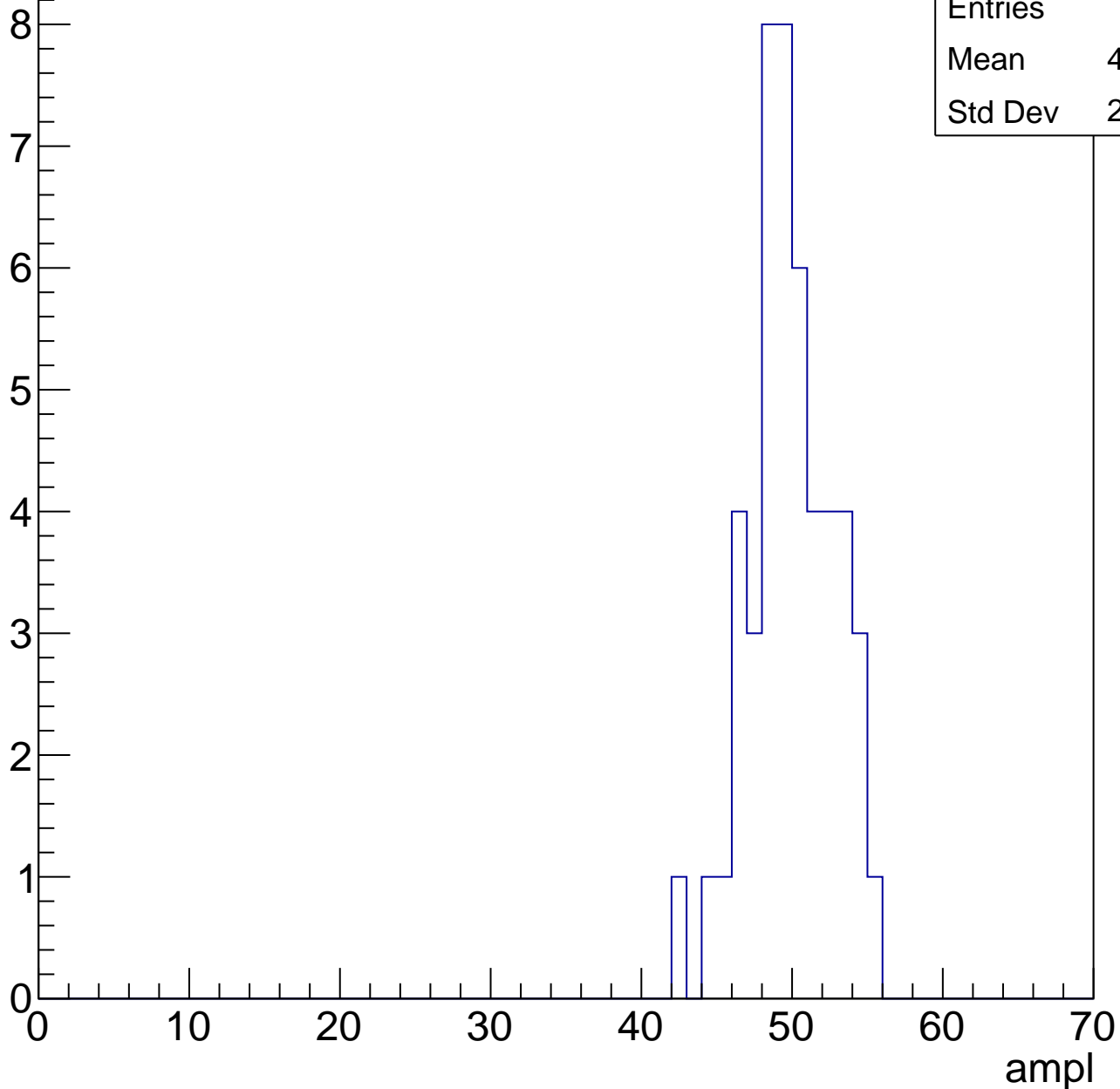


# B0L001S, U17-ch12, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	48
Mean	49.44
Std Dev	2.776

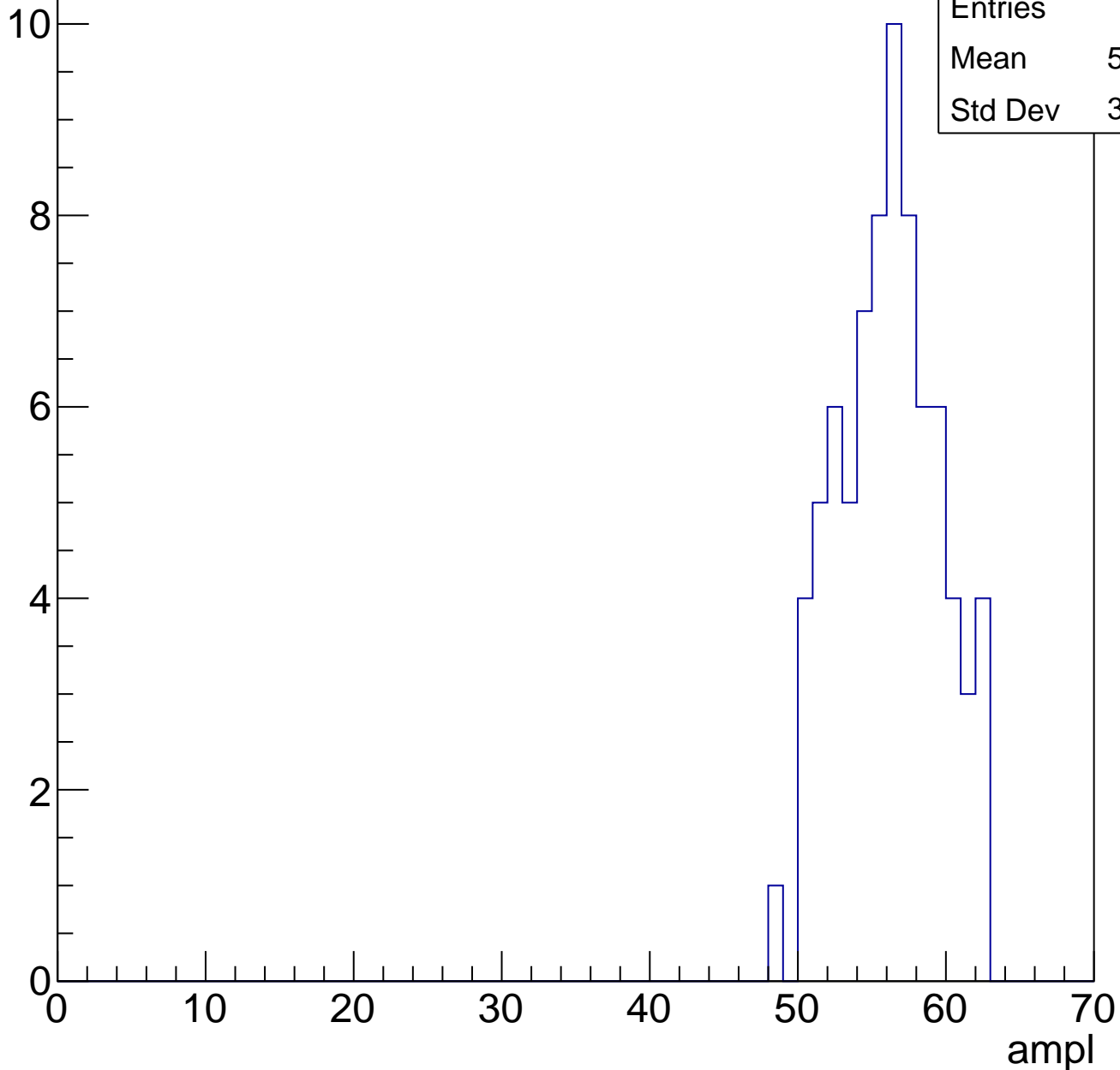


# B0L001S, U17-ch12, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	77
Mean	55.68
Std Dev	3.363

Entry

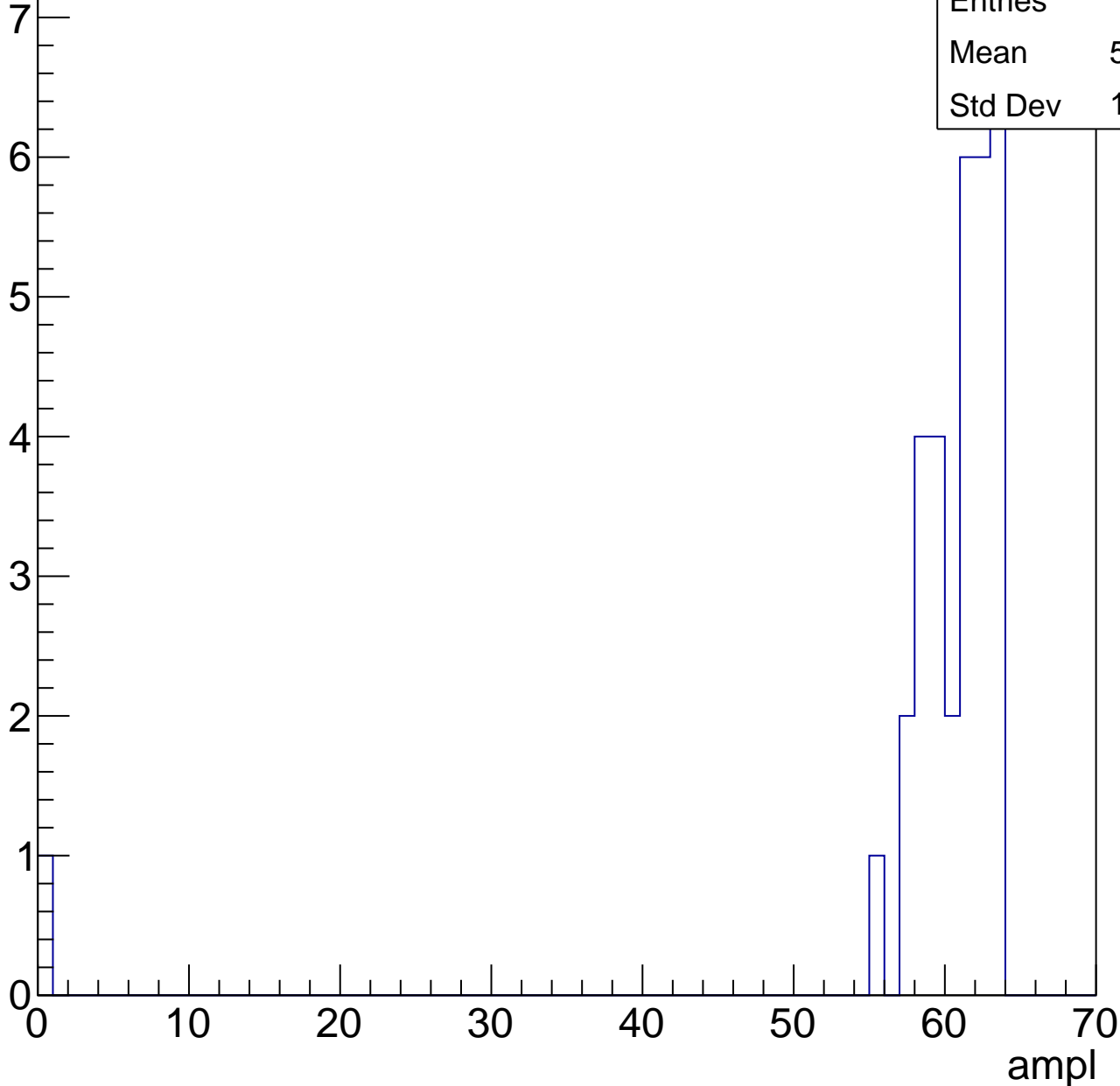


# B0L001S, U17-ch12, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

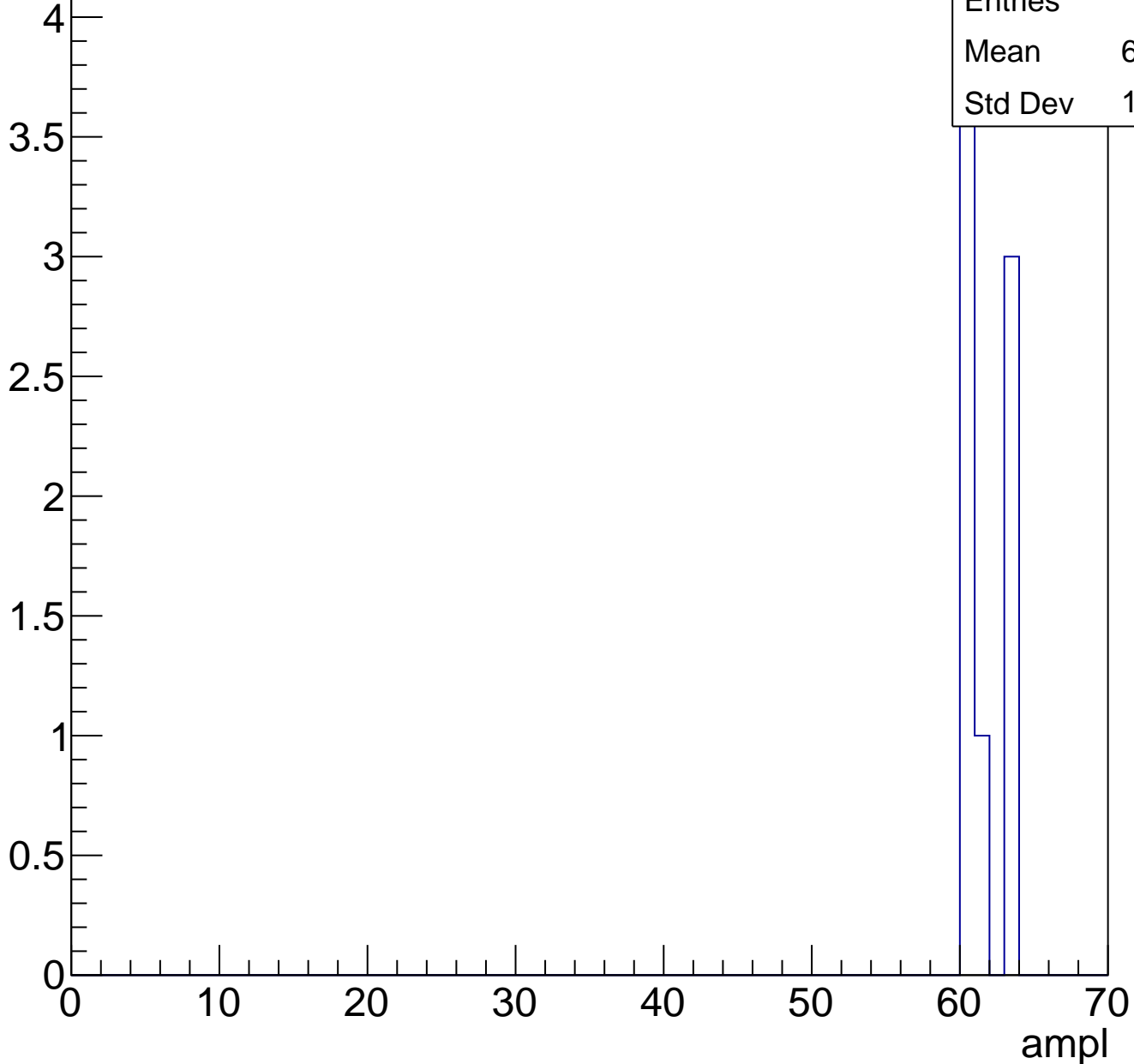
Entries	33
Mean	58.67
Std Dev	10.58



# B0L001S, U17-ch12, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch12, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U17-ch13, adc0

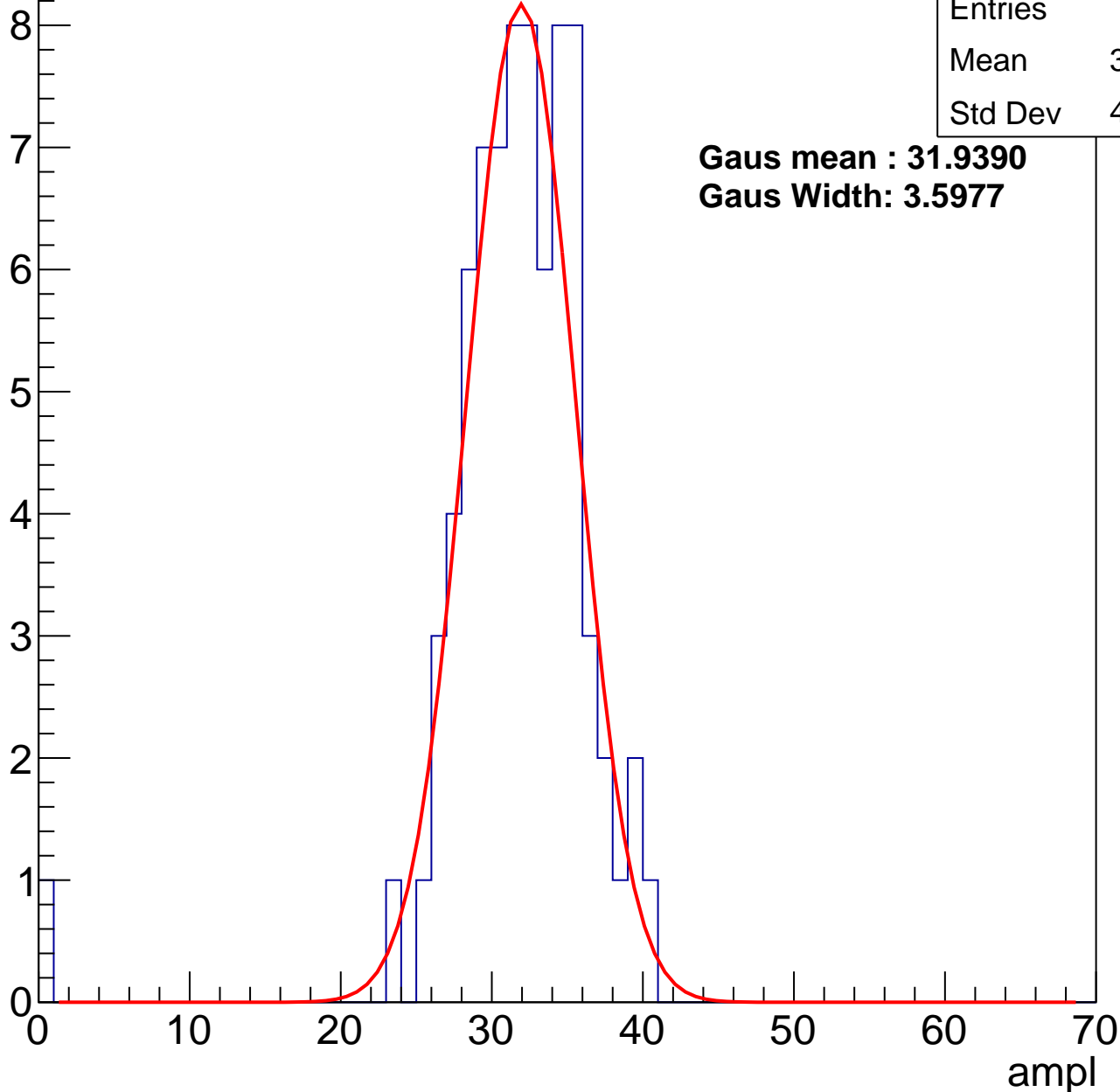
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	77
Mean	31.26
Std Dev	4.995

**Gaus mean : 31.9390**

**Gaus Width: 3.5977**



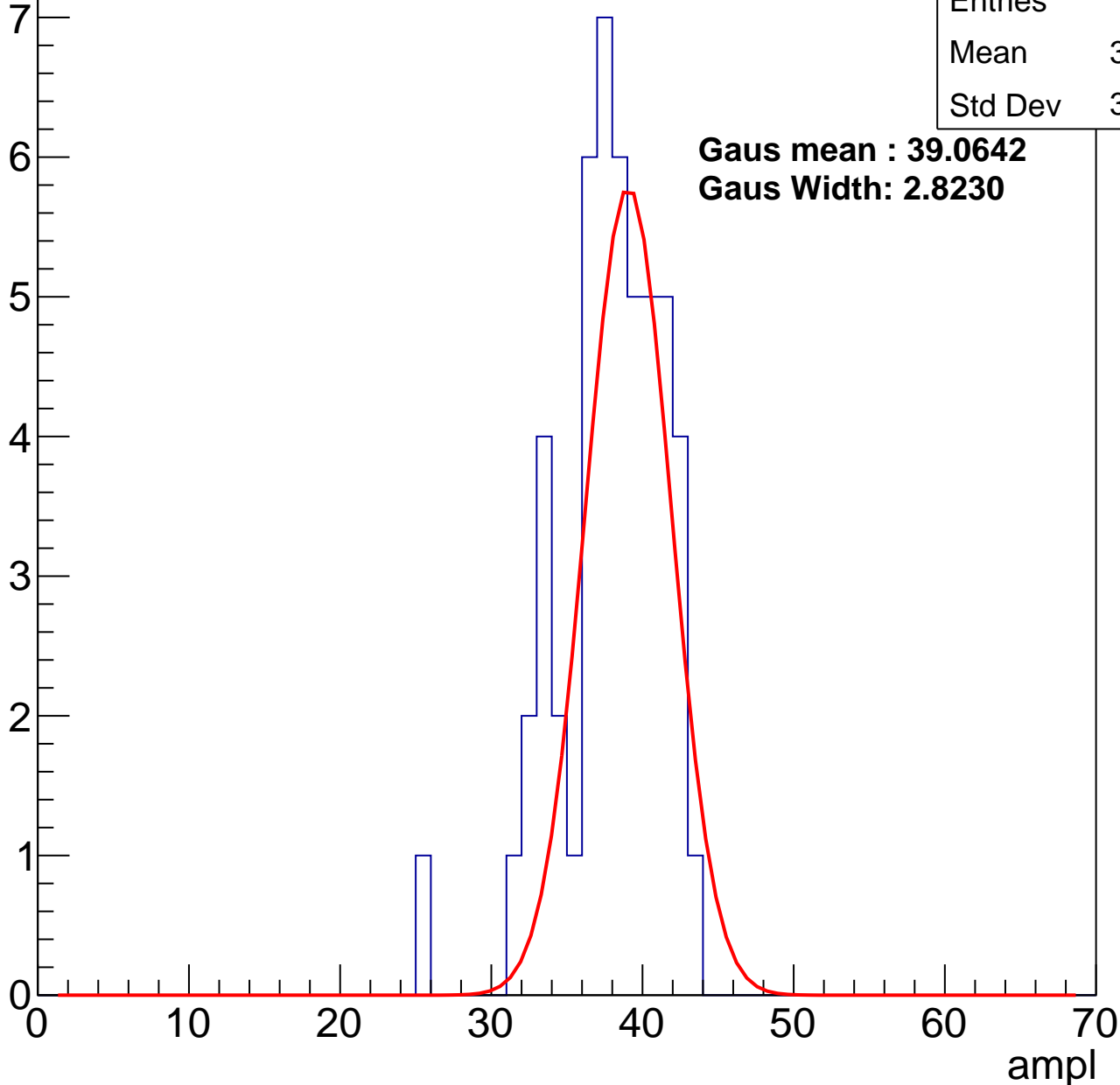
# B0L001S, U17-ch13, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	50
Mean	37.38
Std Dev	3.469

**Gaus mean : 39.0642**  
**Gaus Width: 2.8230**



# B0L001S, U17-ch13, adc2

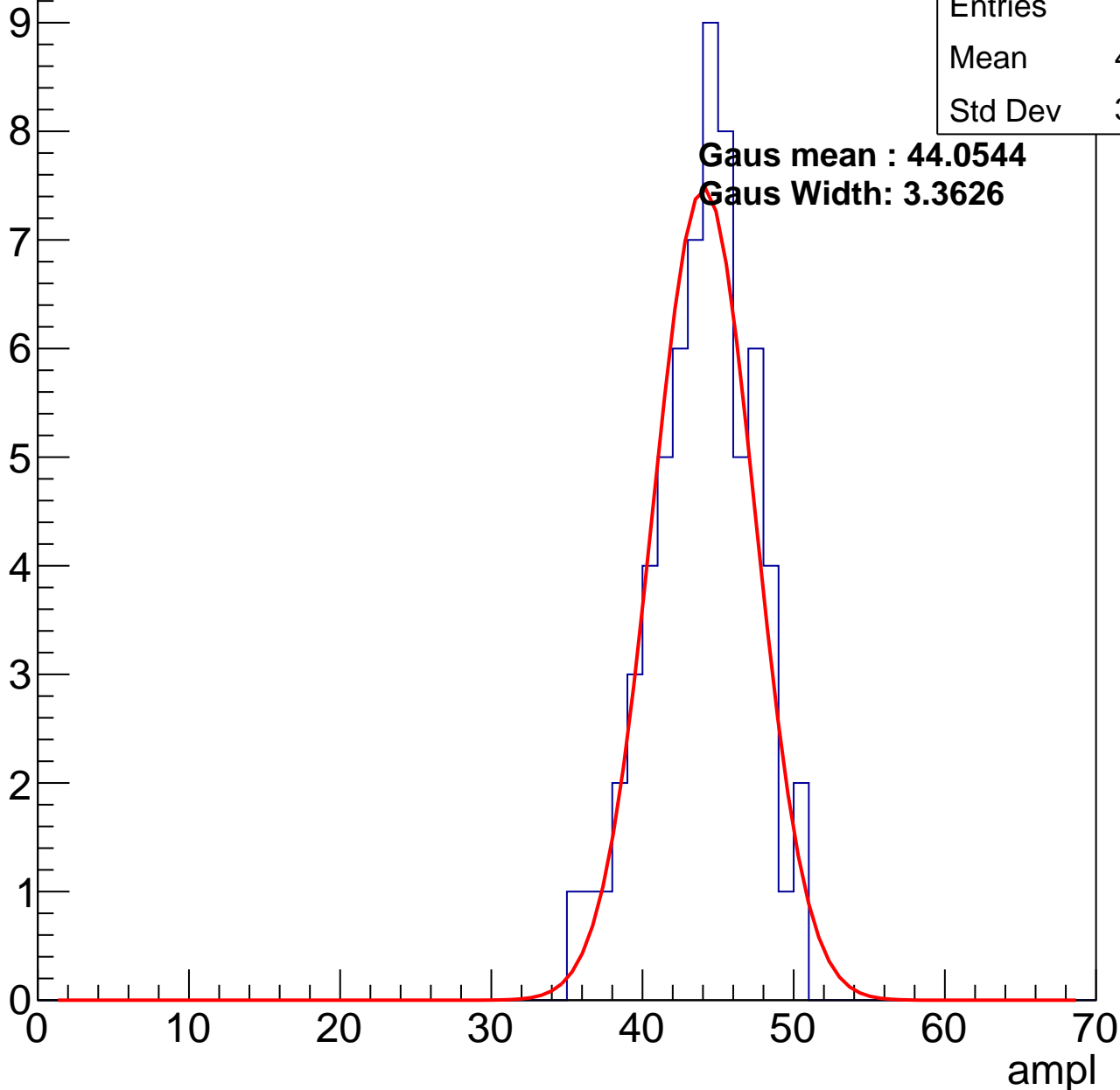
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	43.51
Std Dev	3.301

**Gaus mean : 44.0544**

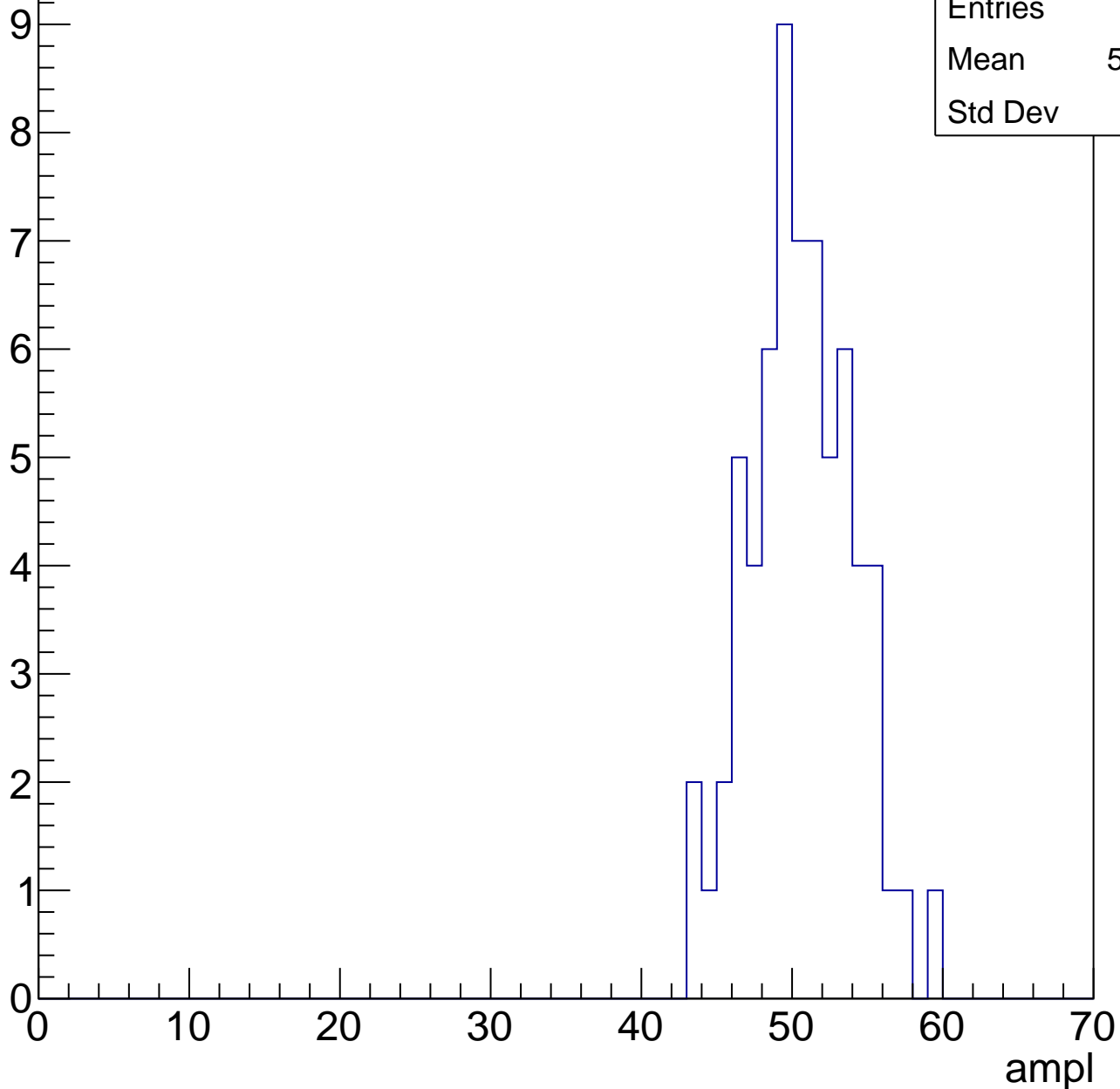
**Gaus Width: 3.3626**



# B0L001S, U17-ch13, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

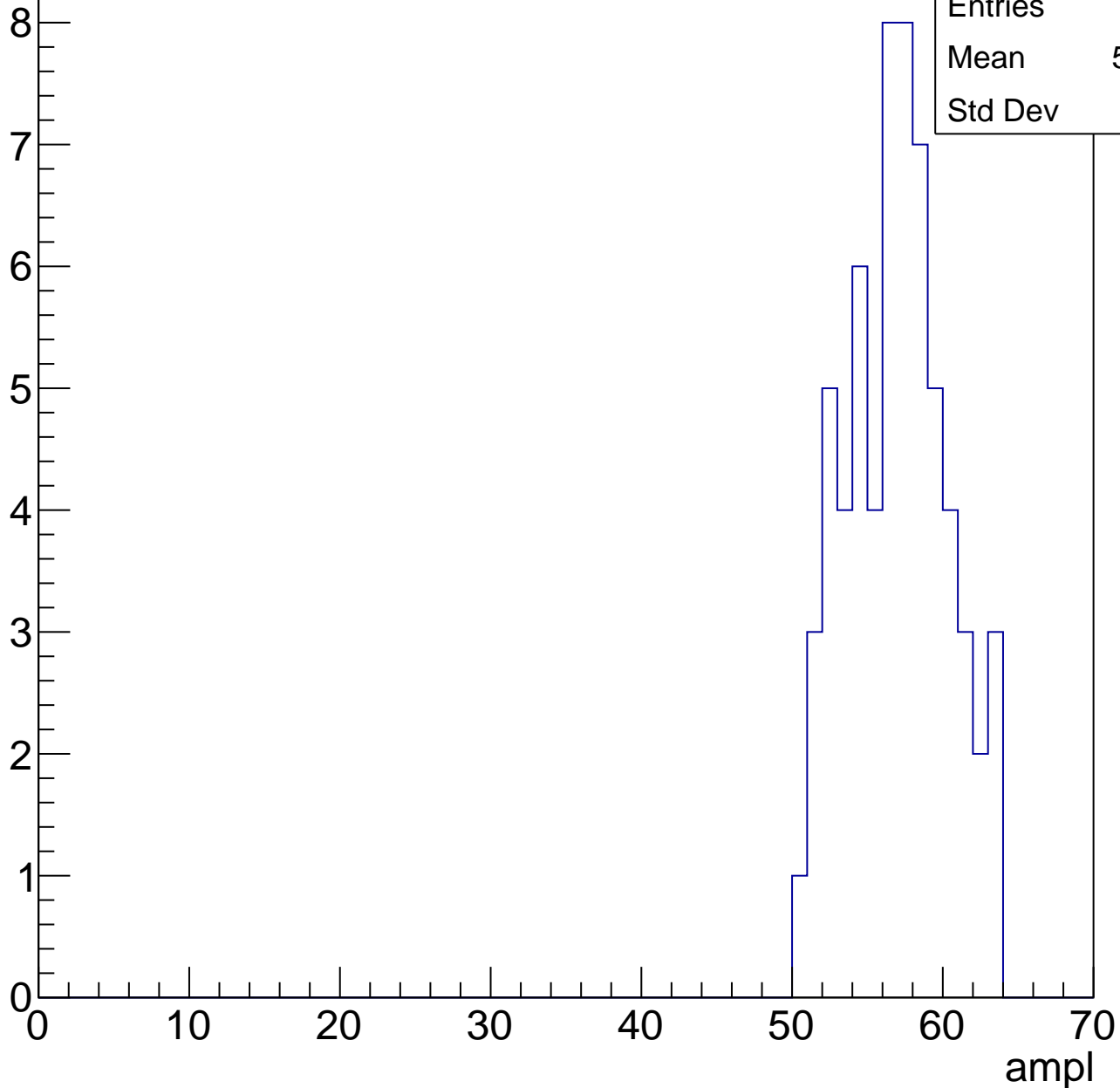


# B0L001S, U17-ch13, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

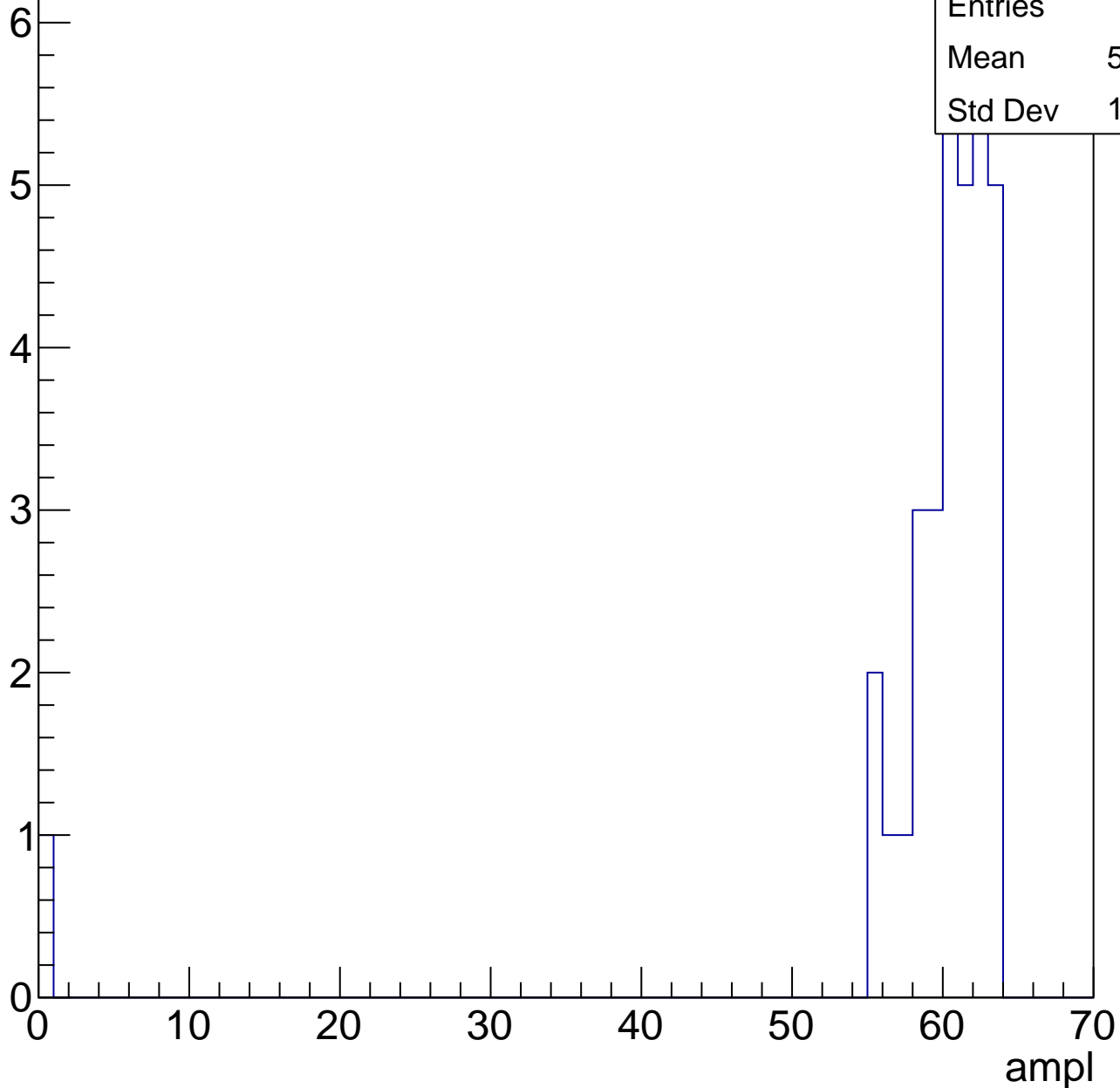
Entries	63
Mean	56.51
Std Dev	3.28



# B0L001S, U17-ch13, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

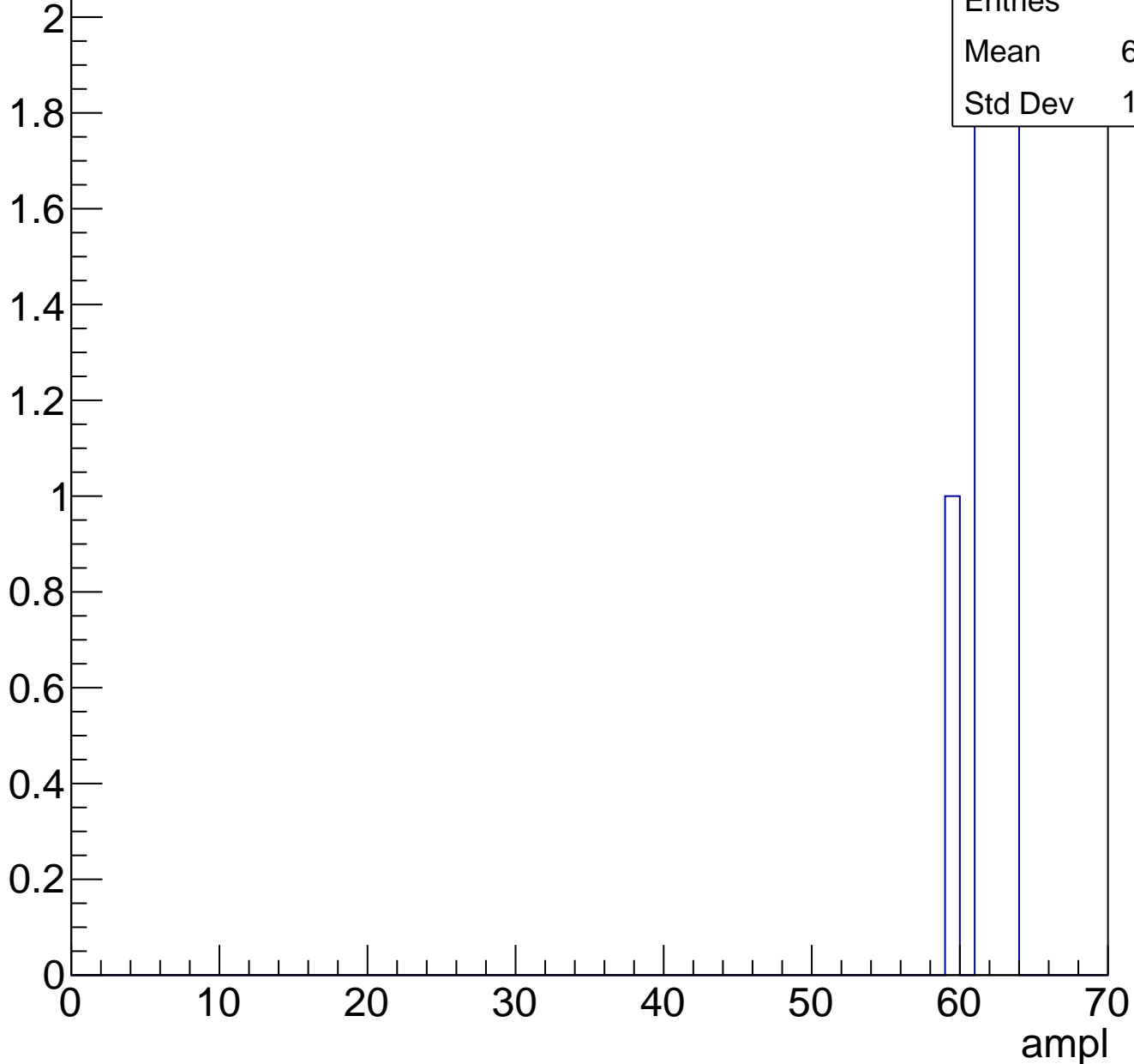
Entry



# B0L001S, U17-ch13, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch13, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	22
Std Dev	0

# B0L001S, U17-ch14, adc0

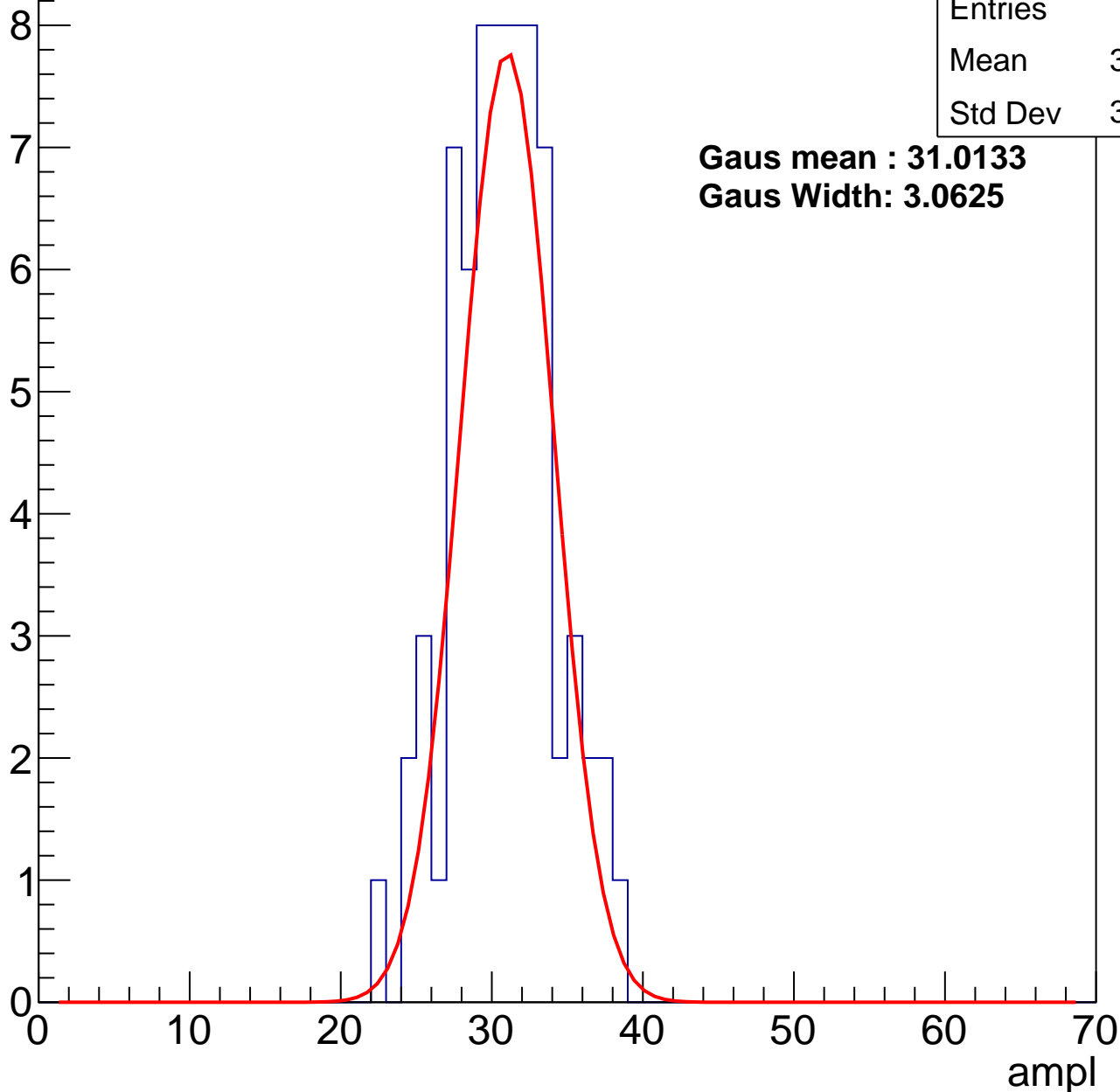
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	30.32
Std Dev	3.317

**Gaus mean : 31.0133**

**Gaus Width: 3.0625**



# B0L001S, U17-ch14, adc1

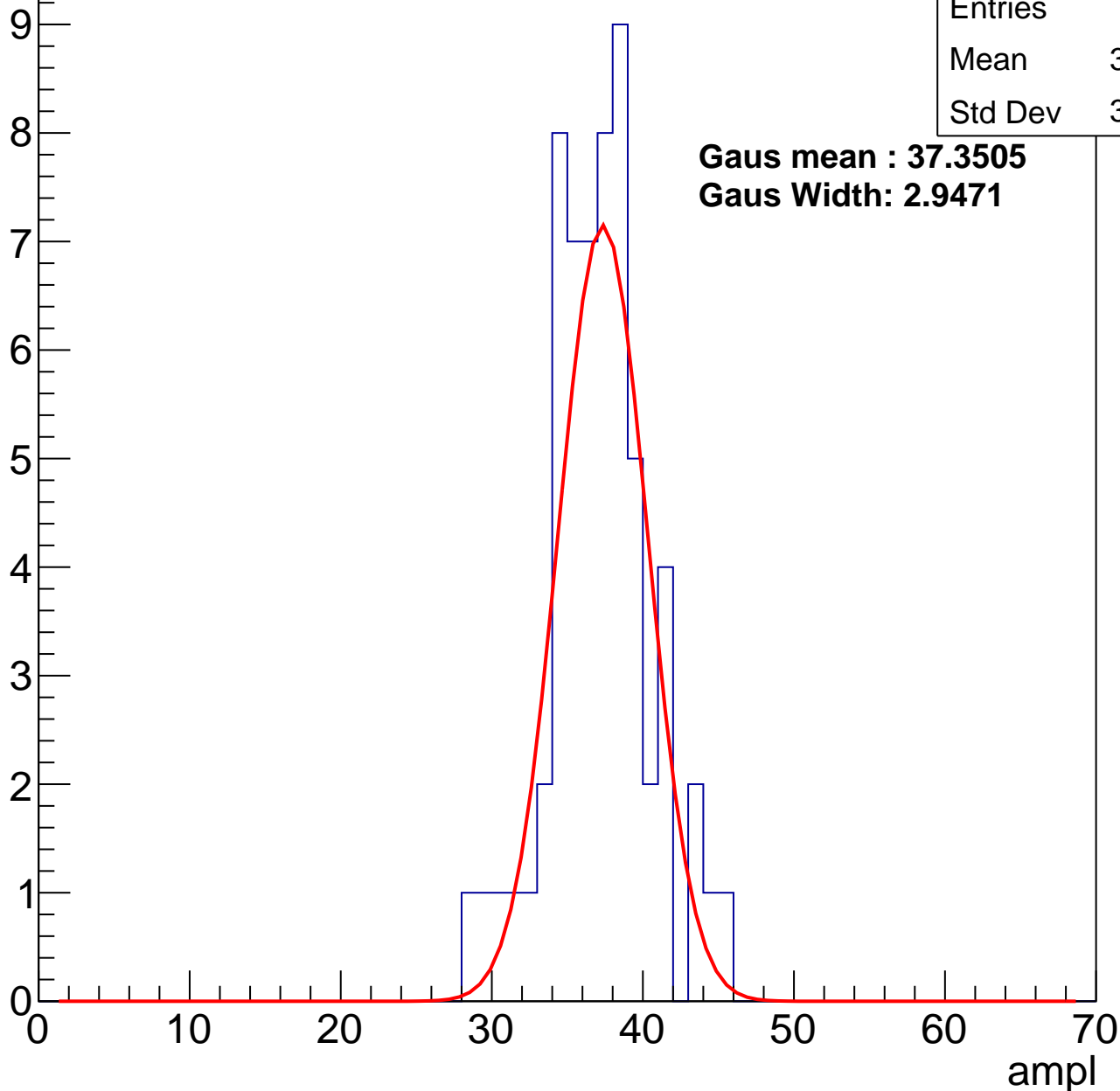
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	36.67
Std Dev	3.347

**Gaus mean : 37.3505**

**Gaus Width: 2.9471**



# B0L001S, U17-ch14, adc2

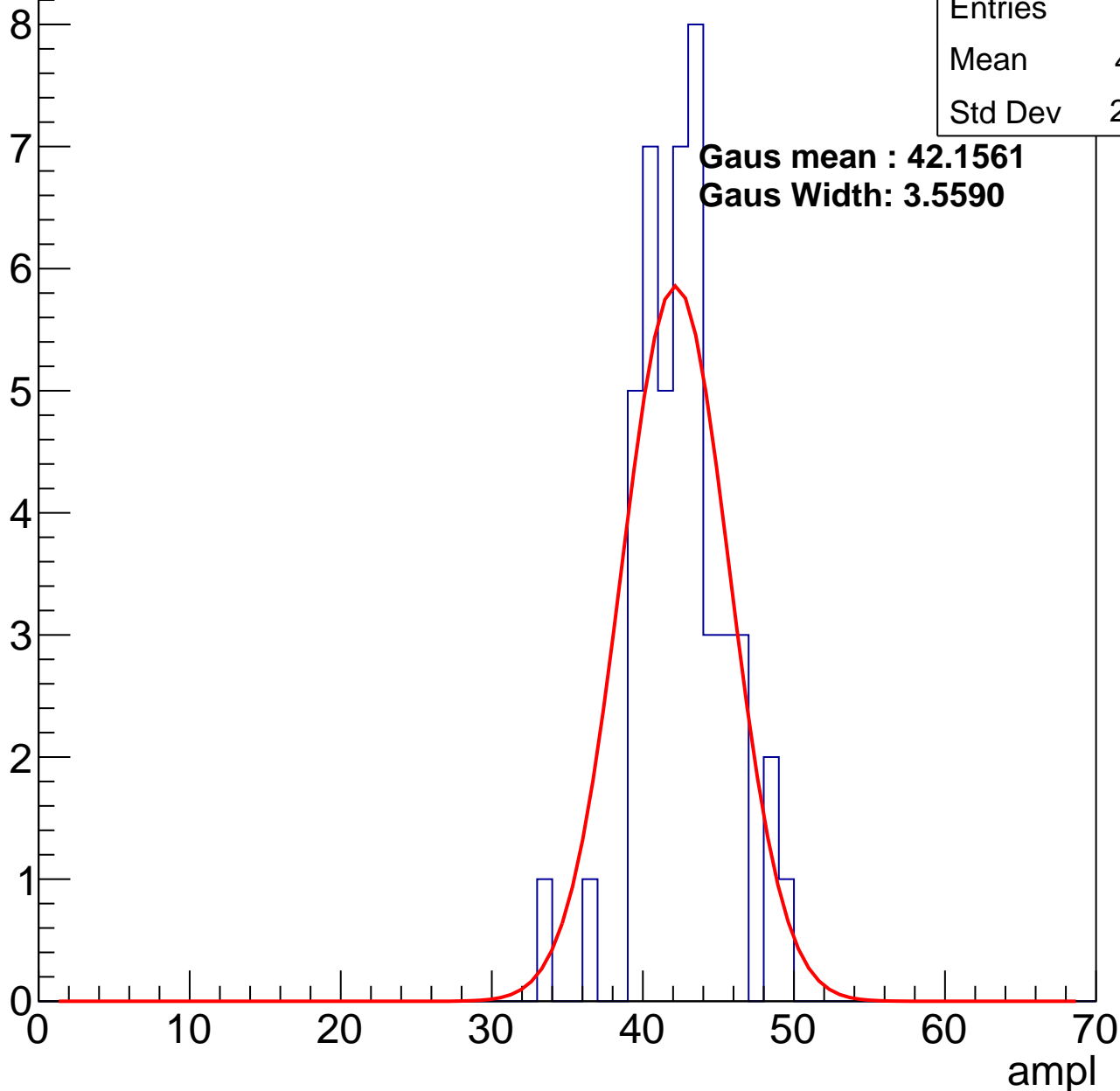
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	46
Mean	42.11
Std Dev	2.987

**Gaus mean : 42.1561**

**Gaus Width: 3.5590**

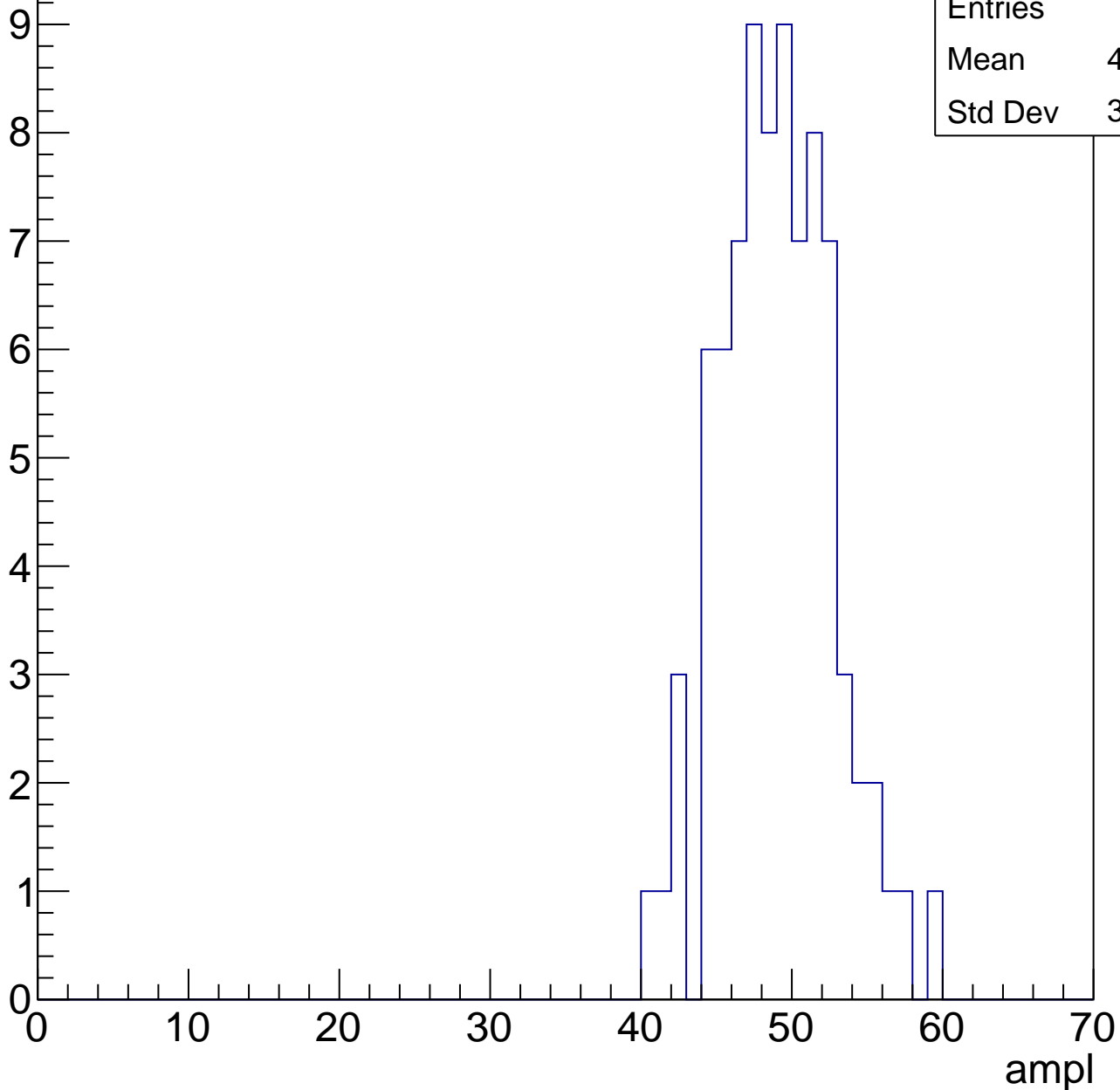


# B0L001S, U17-ch14, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	82
Mean	48.56
Std Dev	3.686

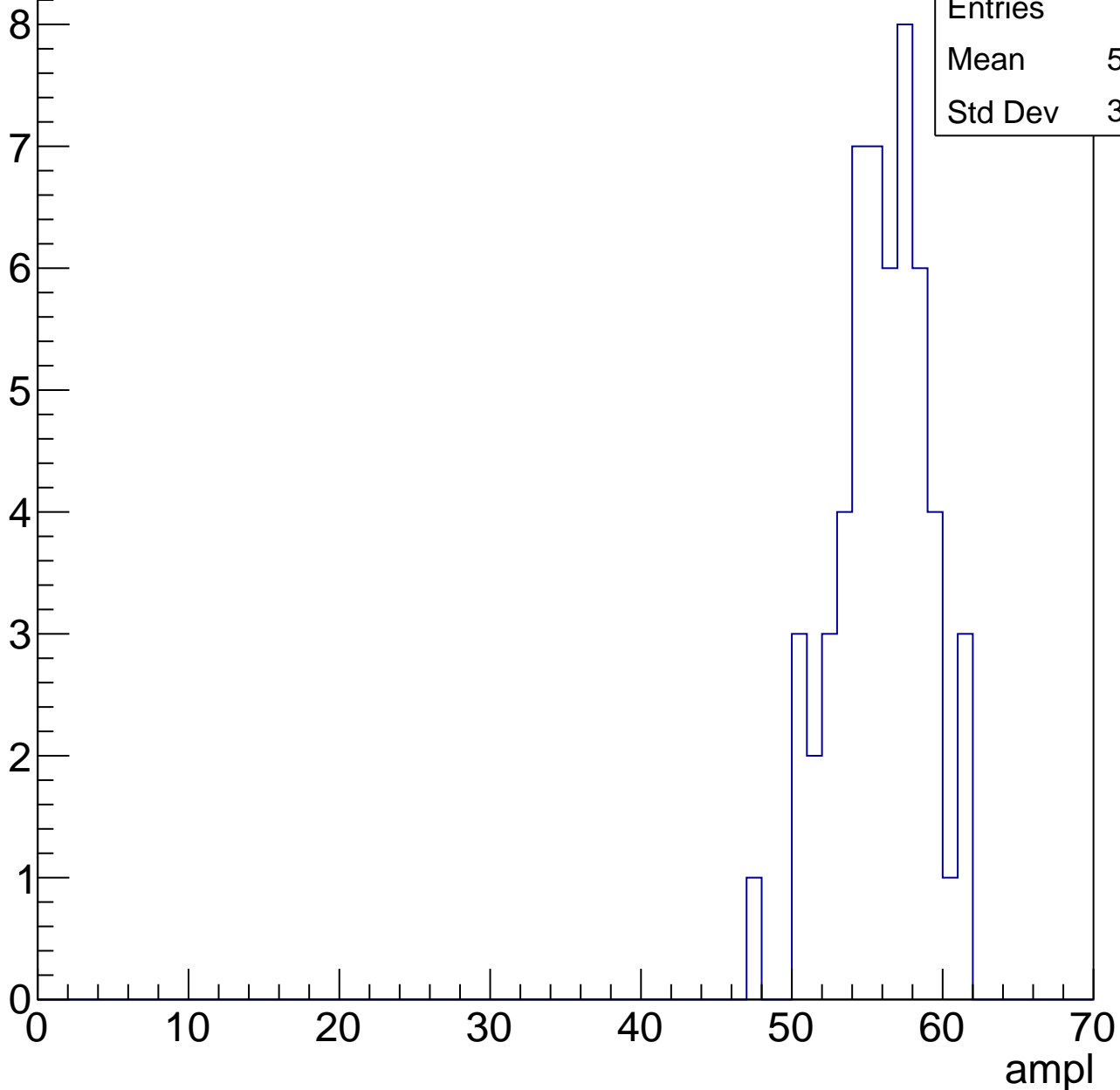


# B0L001S, U17-ch14, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

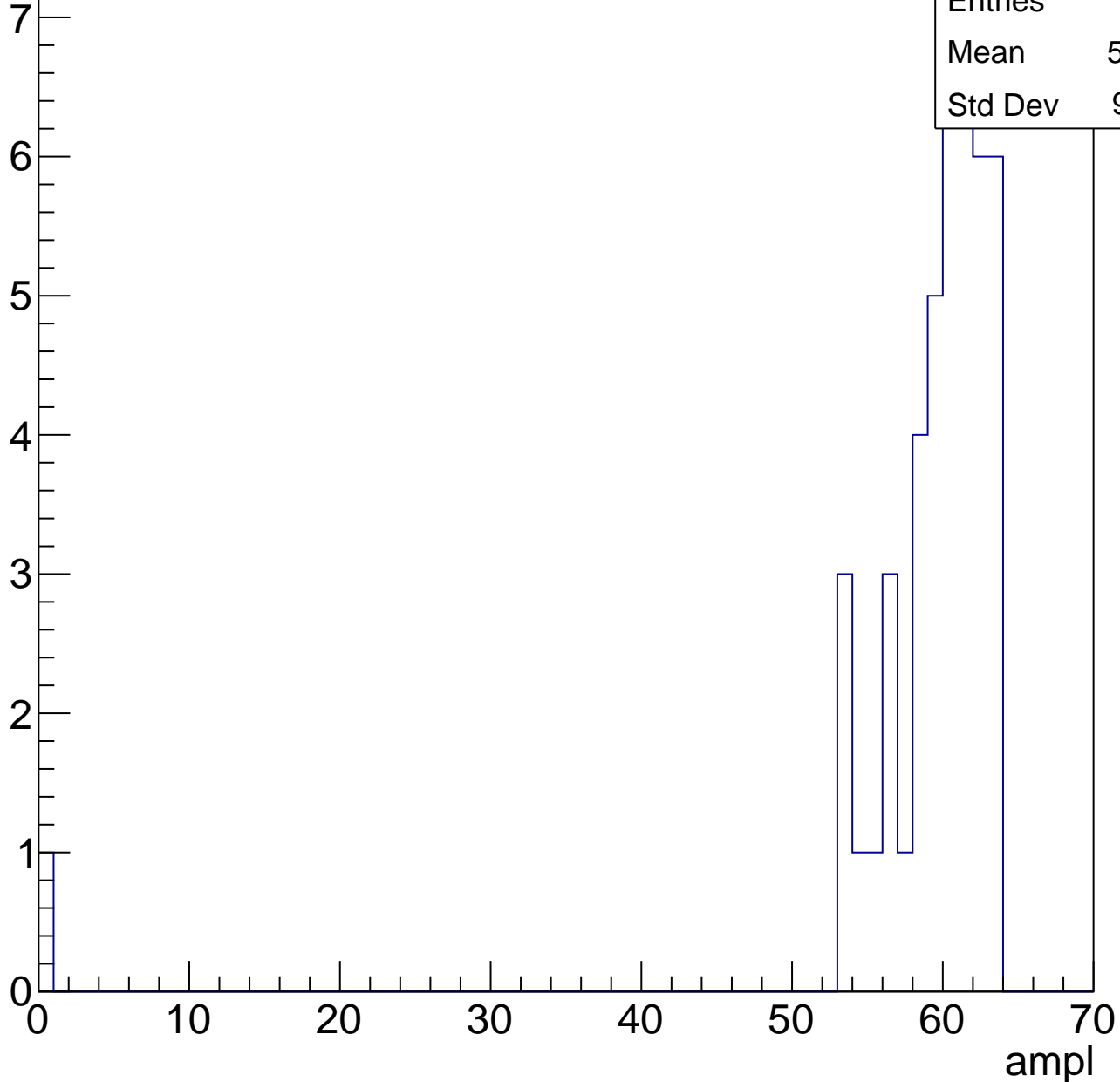
Entries	55
Mean	55.44
Std Dev	3.014



# B0L001S, U17-ch14, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

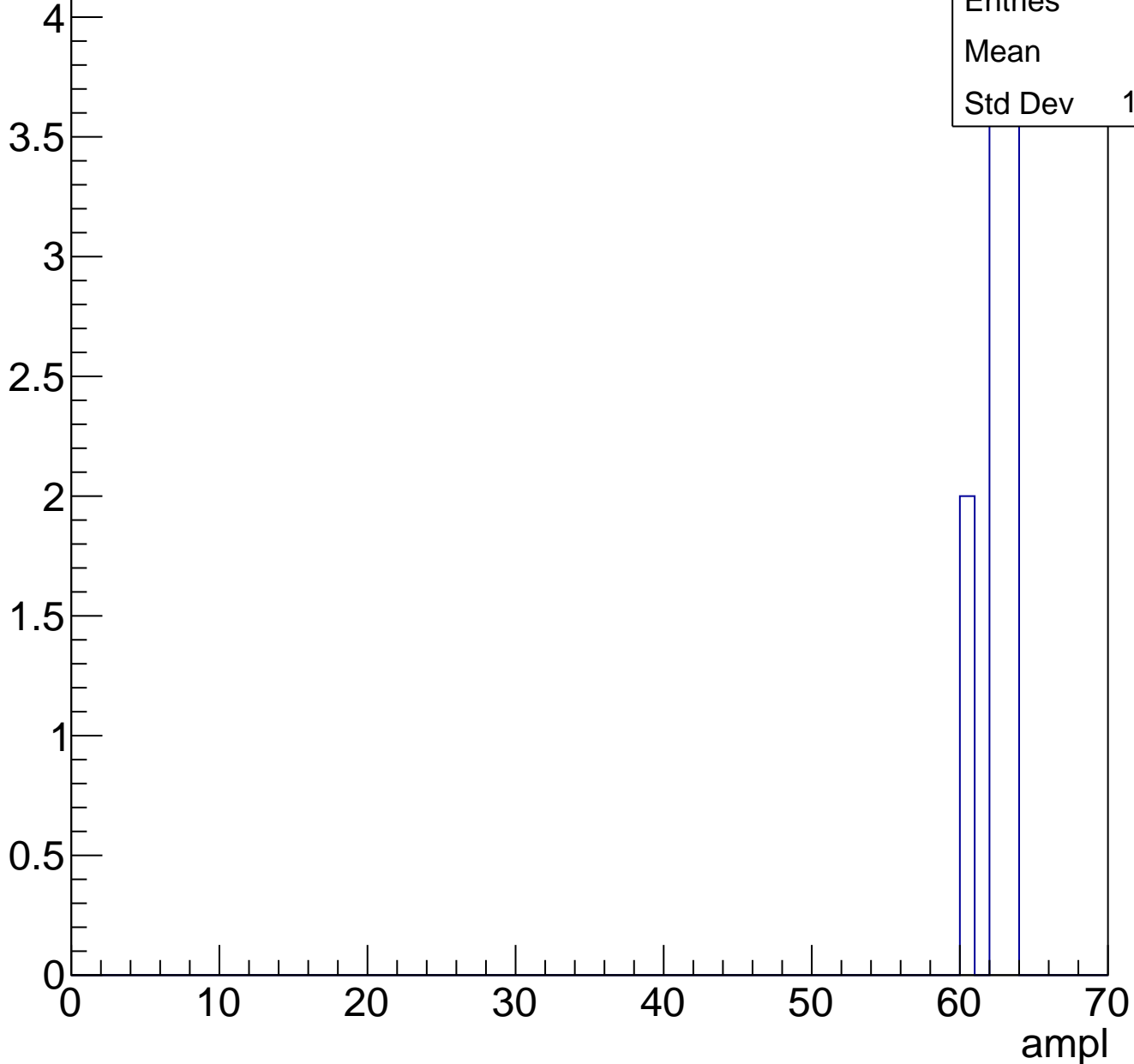


Entries	45
Mean	58.16
Std Dev	9.211

# B0L001S, U17-ch14, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch14, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U17-ch15, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	67
Mean	28.48
Std Dev	6.899

**Gaus mean : 29.8375**

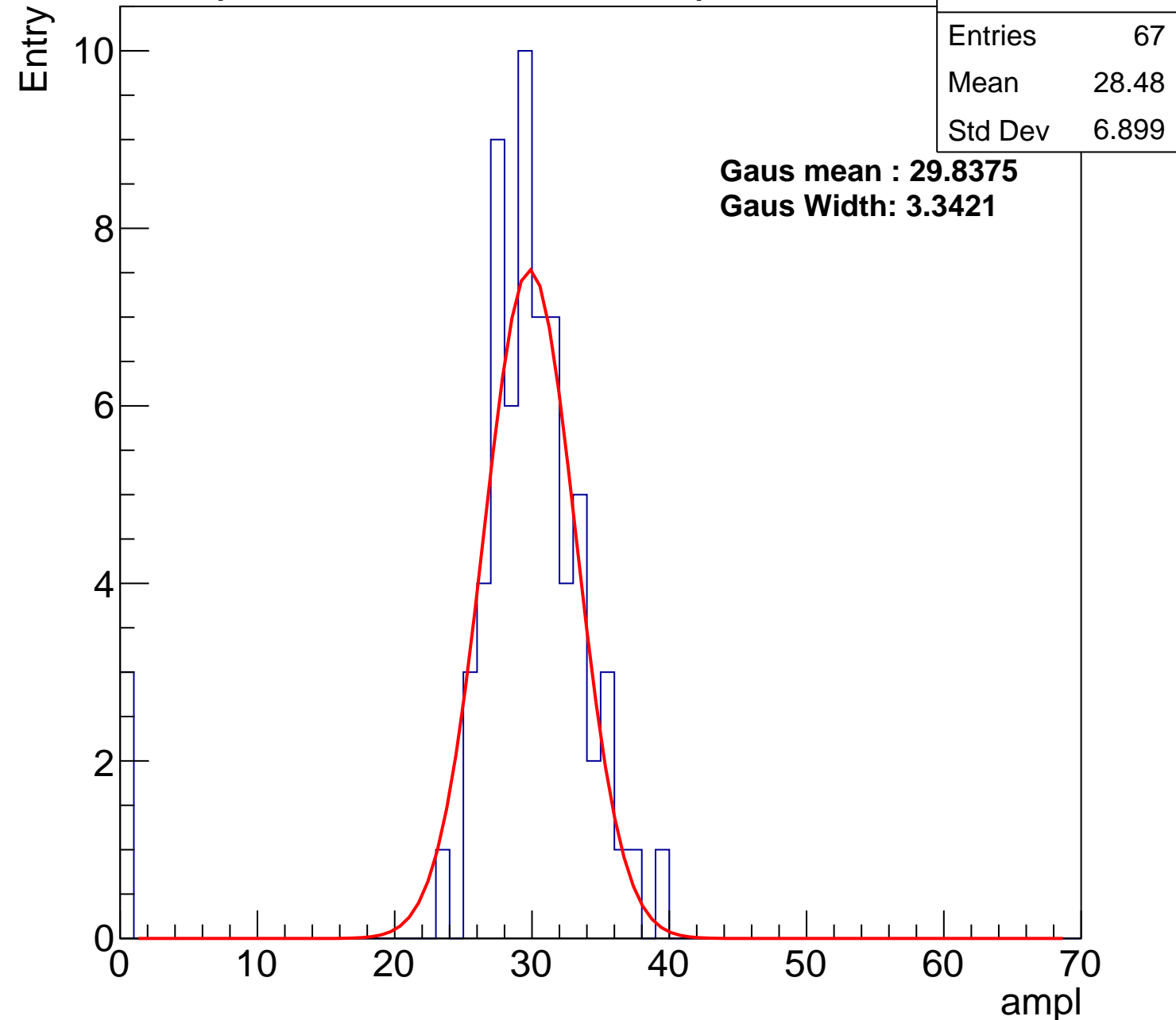
**Gaus Width: 3.3421**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



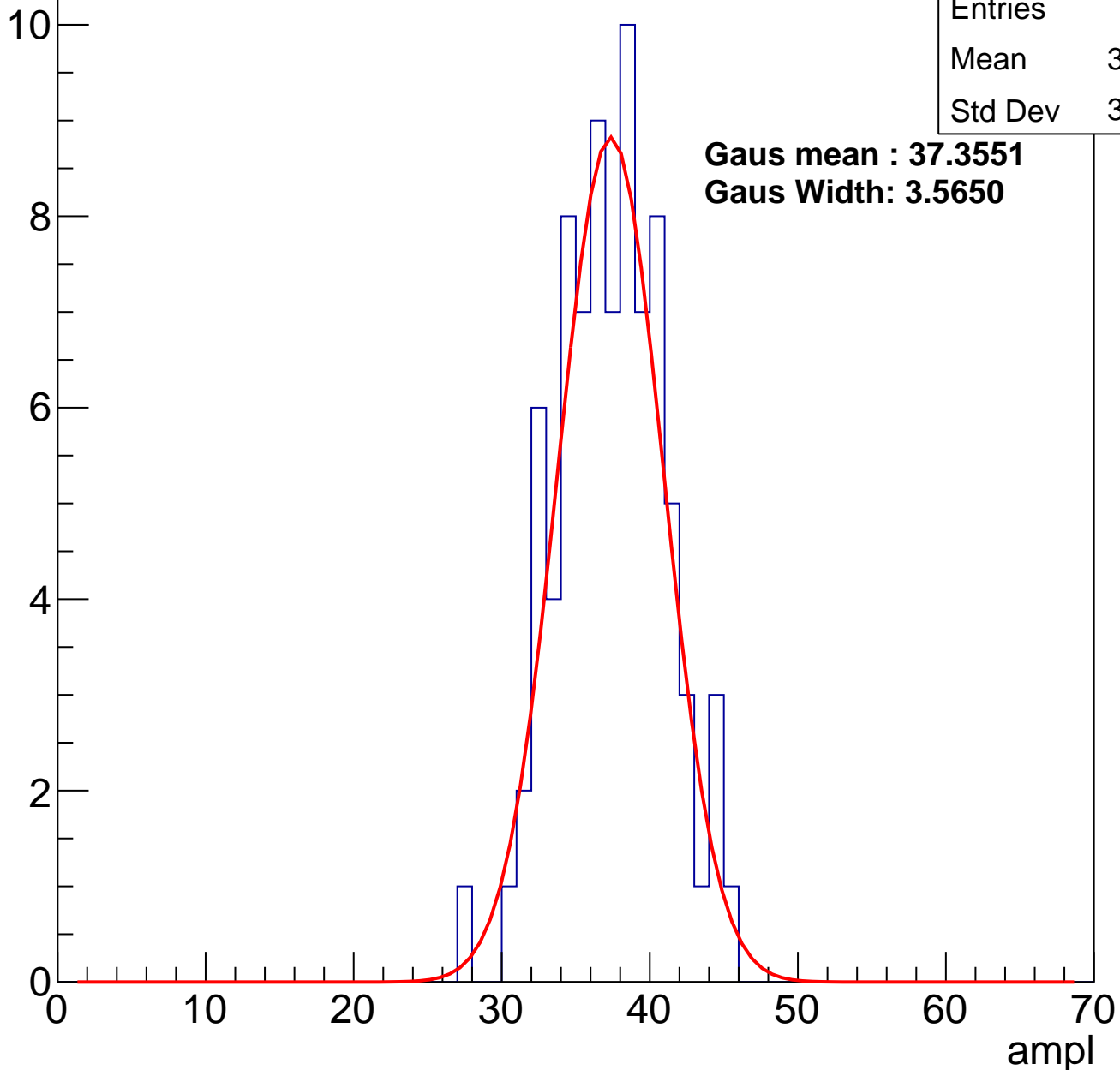
# B0L001S, U17-ch15, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	83
Mean	36.95
Std Dev	3.567

**Gaus mean : 37.3551**  
**Gaus Width: 3.5650**

Entry



# B0L001S, U17-ch15, adc2

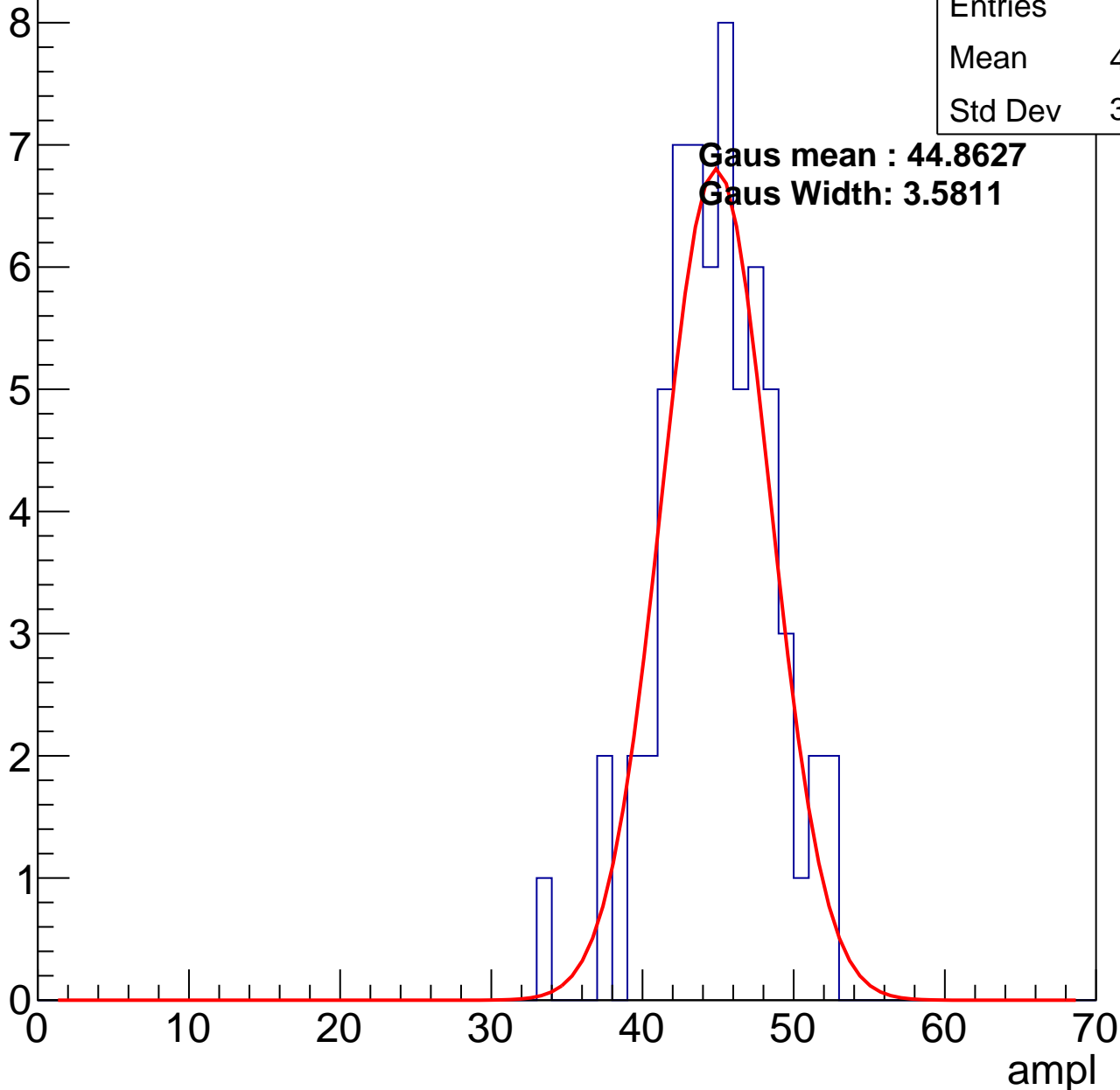
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	44.44
Std Dev	3.682

**Gaus mean : 44.8627**

**Gaus Width: 3.5811**

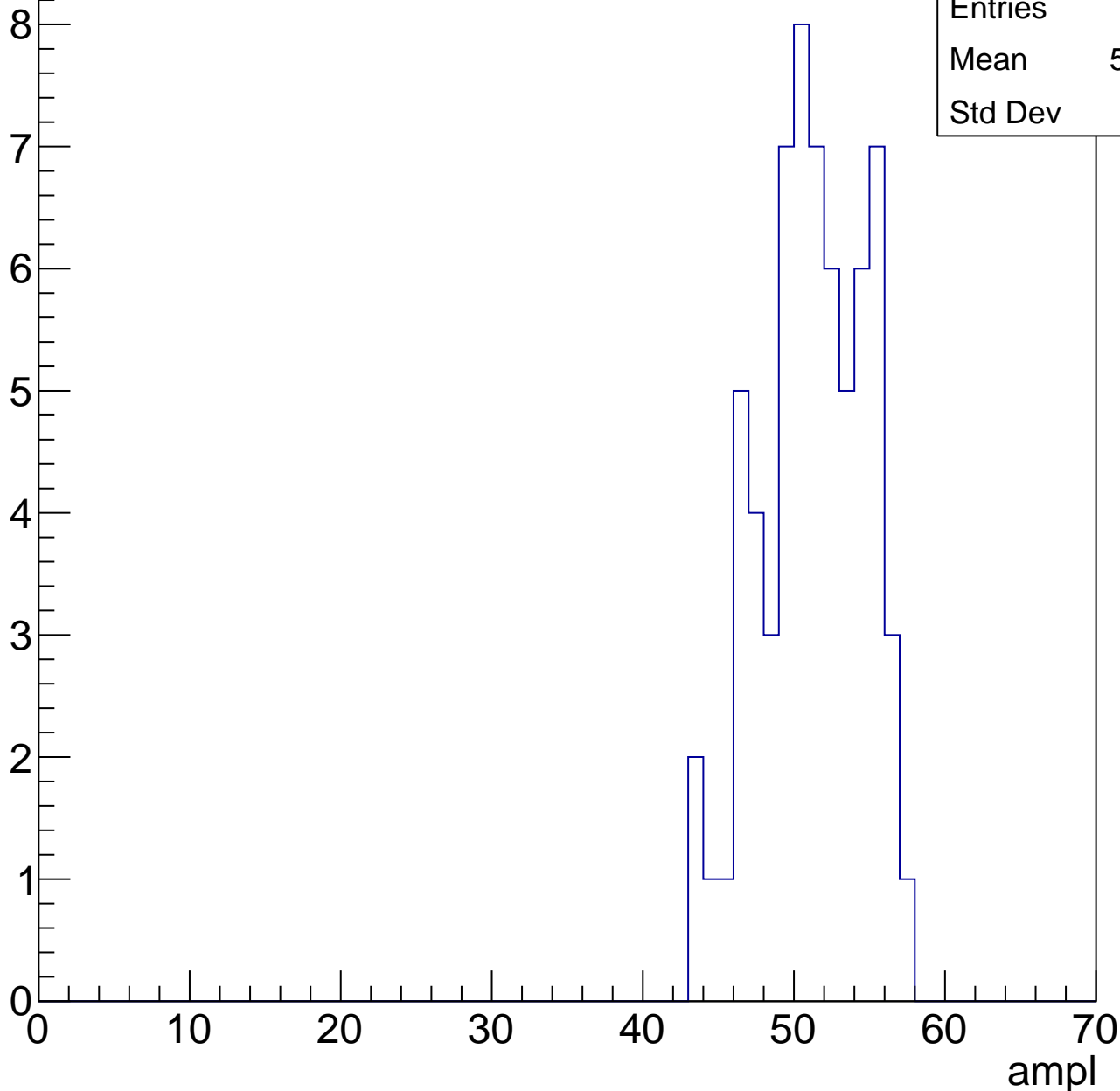


# B0L001S, U17-ch15, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	50.73
Std Dev	3.4

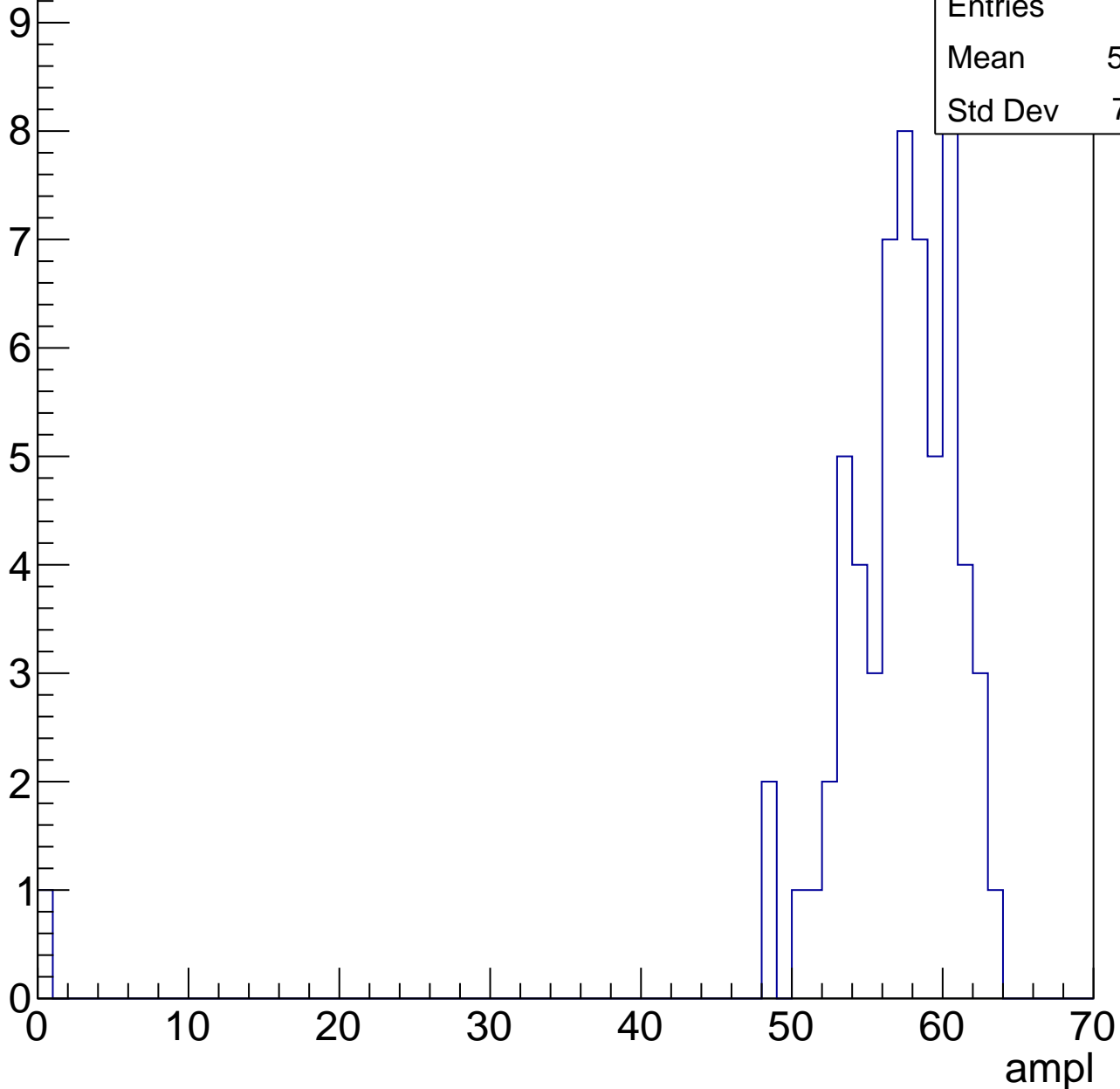


# B0L001S, U17-ch15, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	56.02
Std Dev	7.871

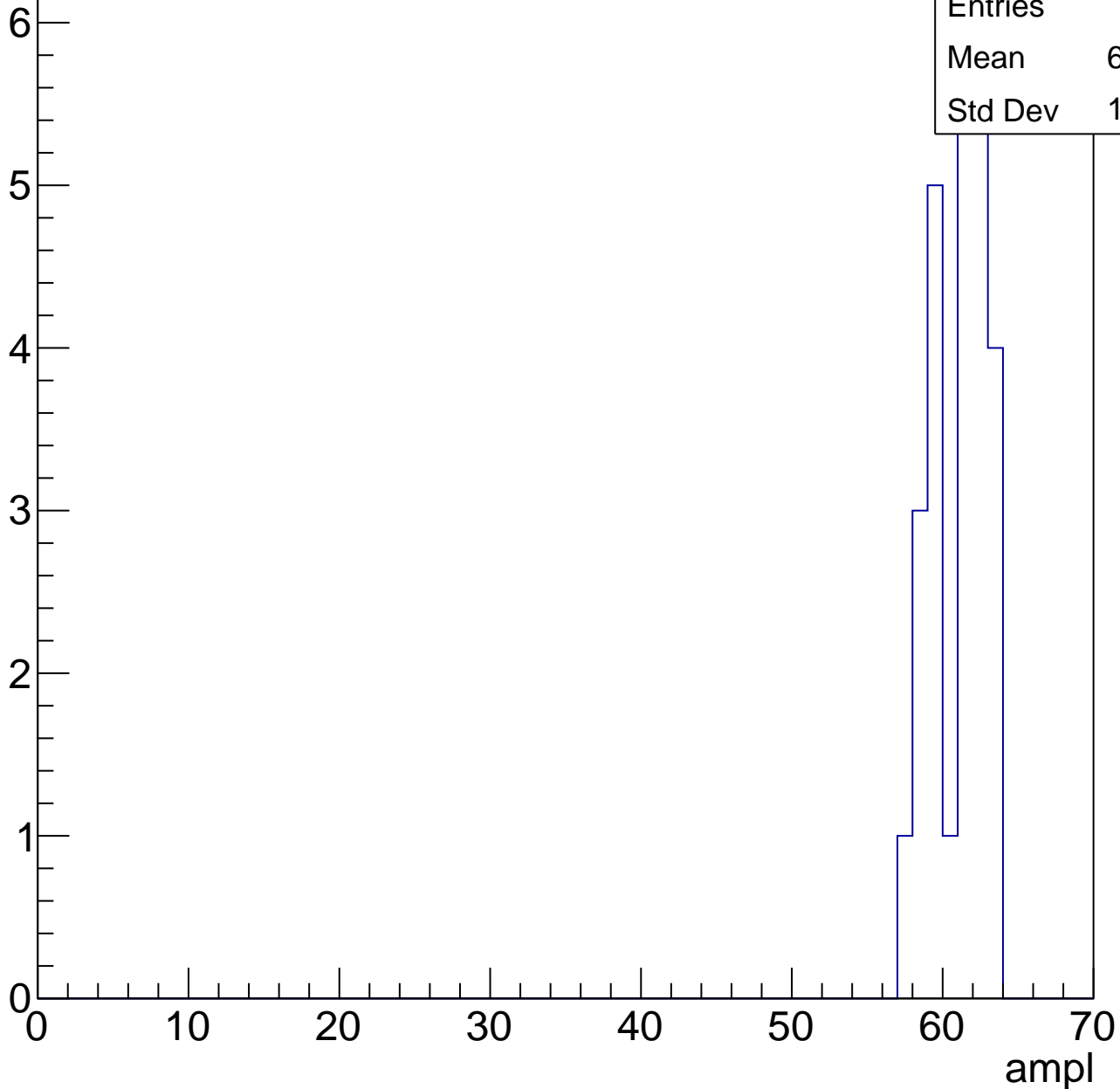


# B0L001S, U17-ch15, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	26
Mean	60.62
Std Dev	1.778

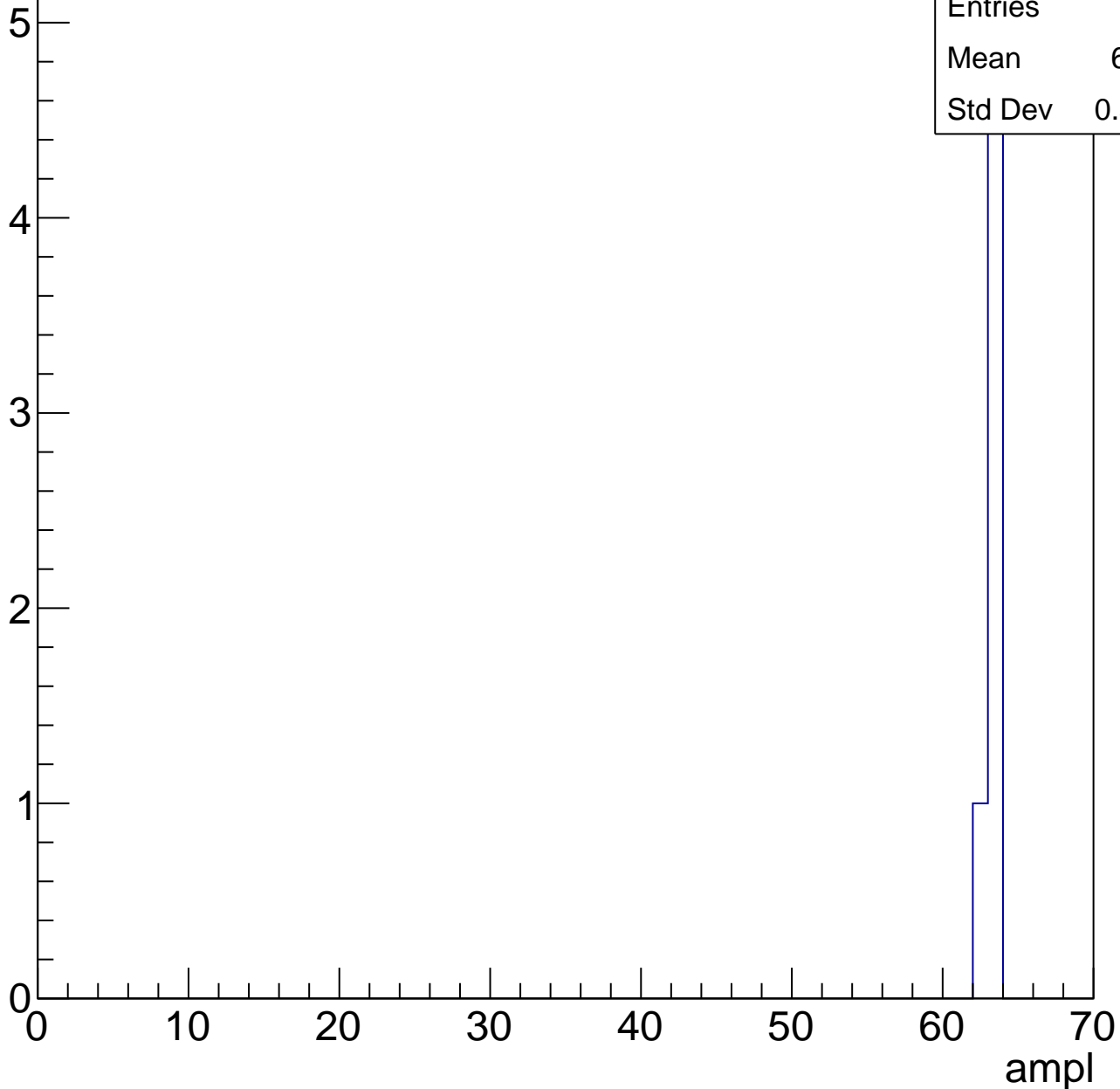


# B0L001S, U17-ch15, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	6
Mean	62.83
Std Dev	0.3727





# B0L001S, U17-ch15, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U17-ch16, adc0

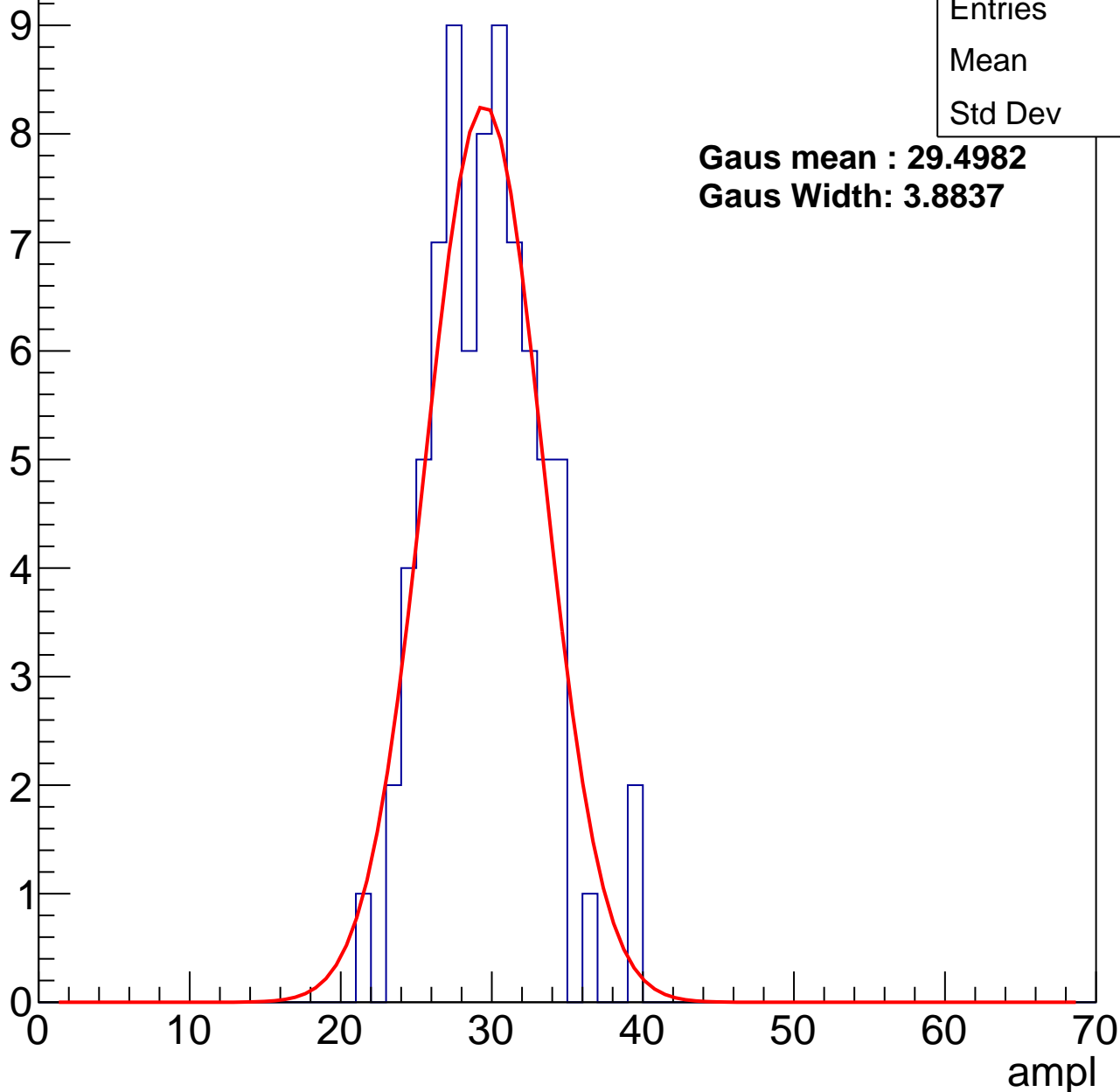
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	77
Mean	29.1
Std Dev	3.54

**Gaus mean : 29.4982**

**Gaus Width: 3.8837**



# B0L001S, U17-ch16, adc1

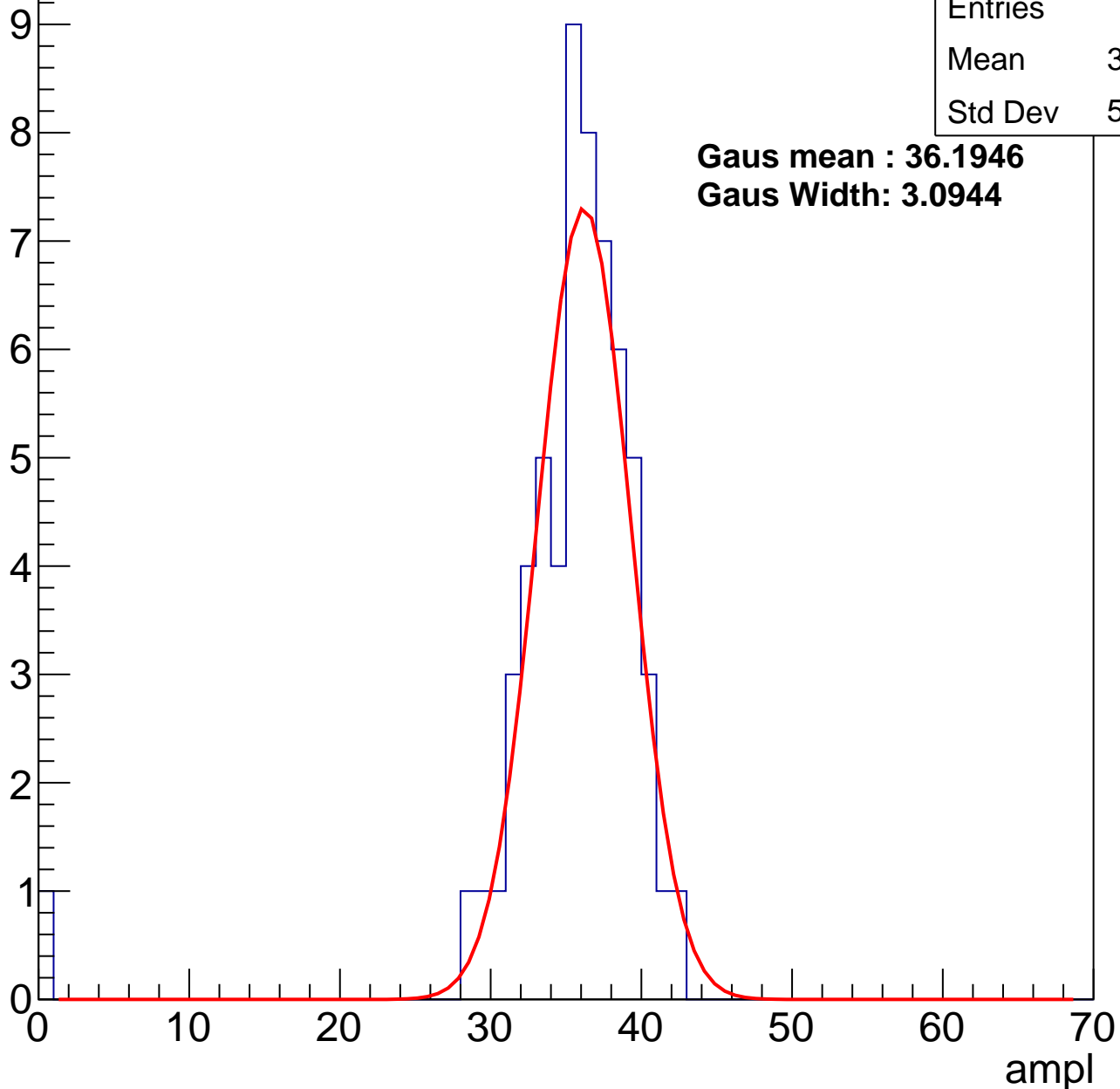
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	34.95
Std Dev	5.436

**Gaus mean : 36.1946**

**Gaus Width: 3.0944**



# B0L001S, U17-ch16, adc2

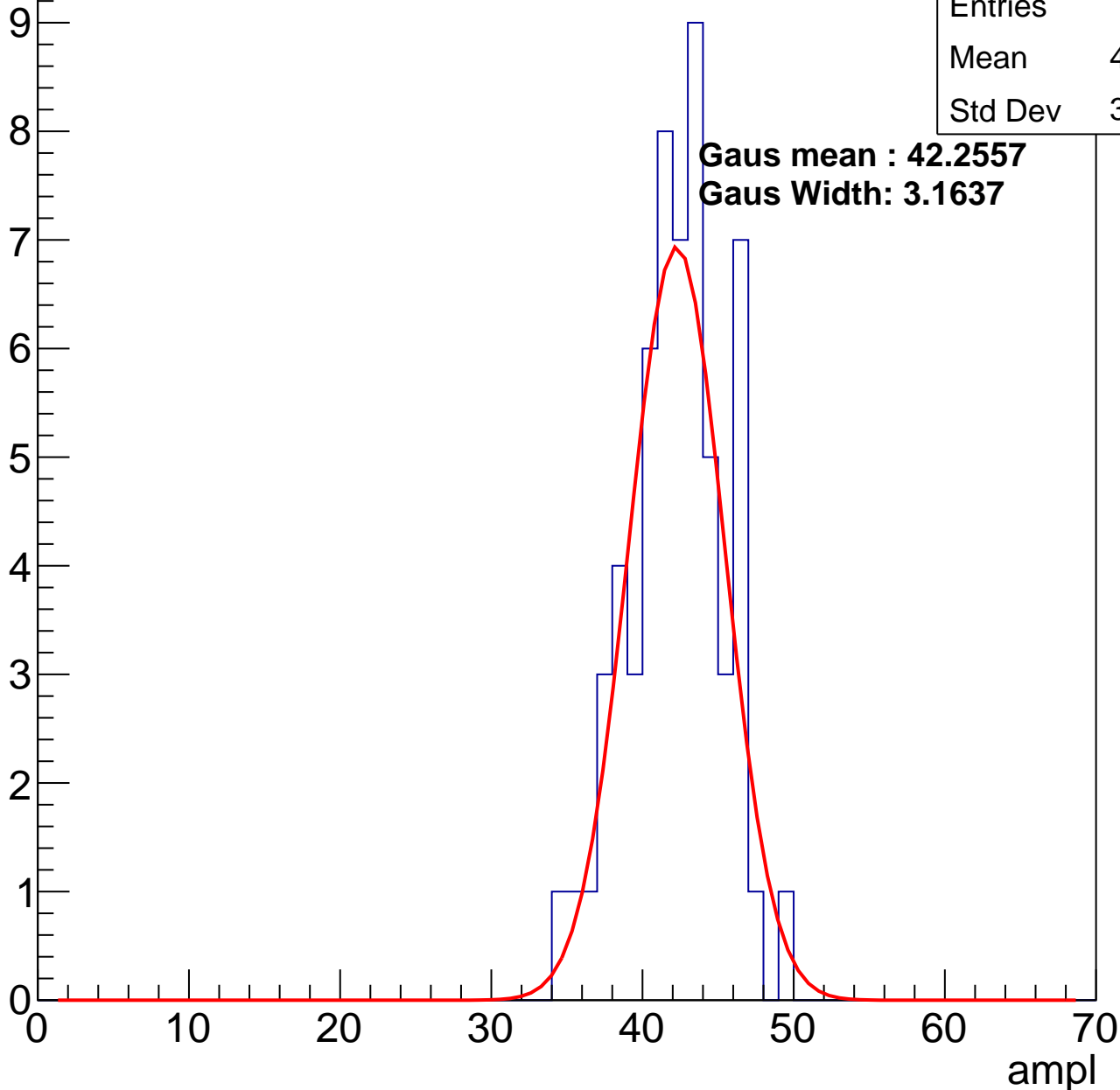
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	41.78
Std Dev	3.126

**Gaus mean : 42.2557**

**Gaus Width: 3.1637**



# B0L001S, U17-ch16, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

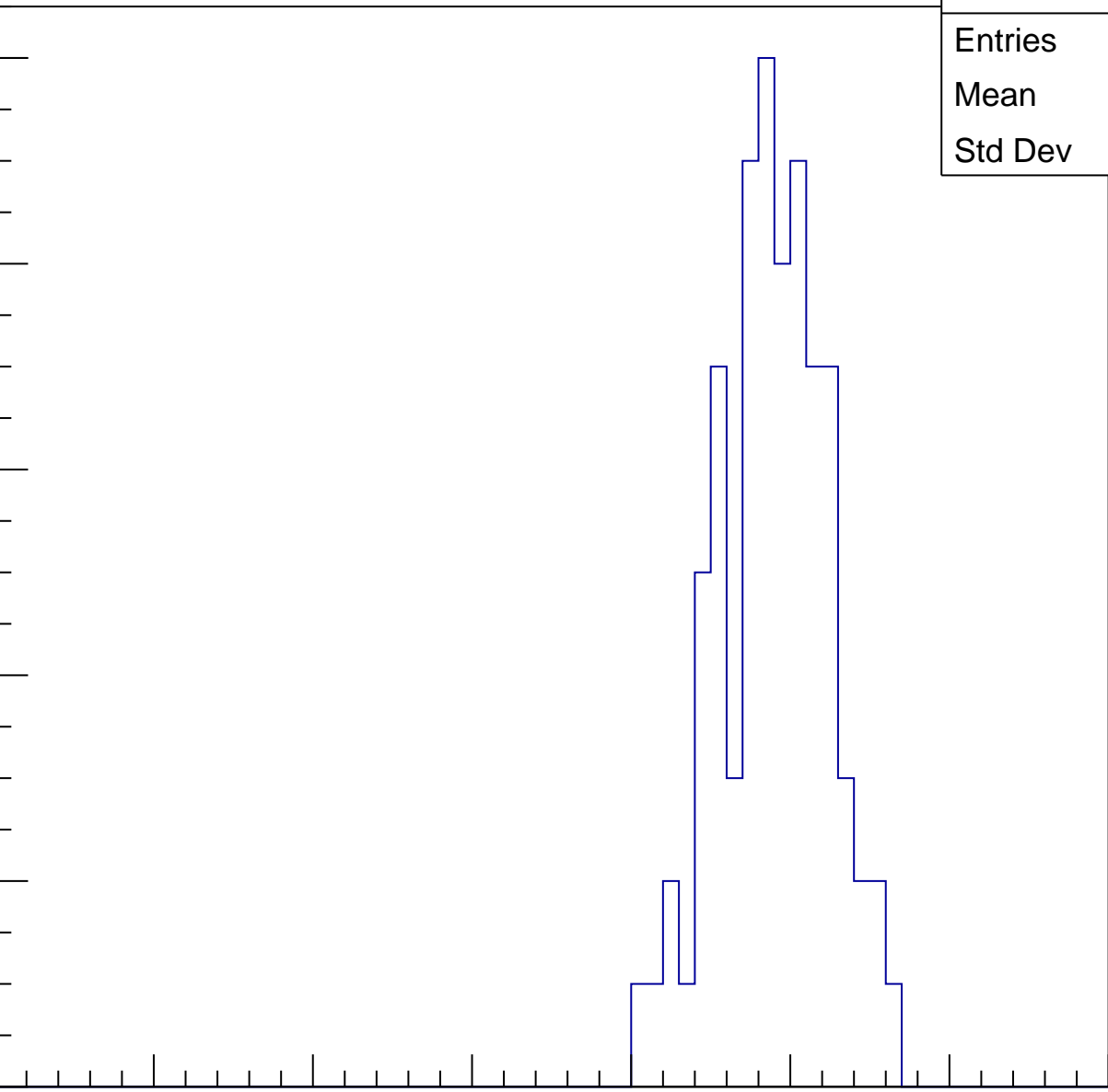
Entries	78
Mean	48.46
Std Dev	3.369

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

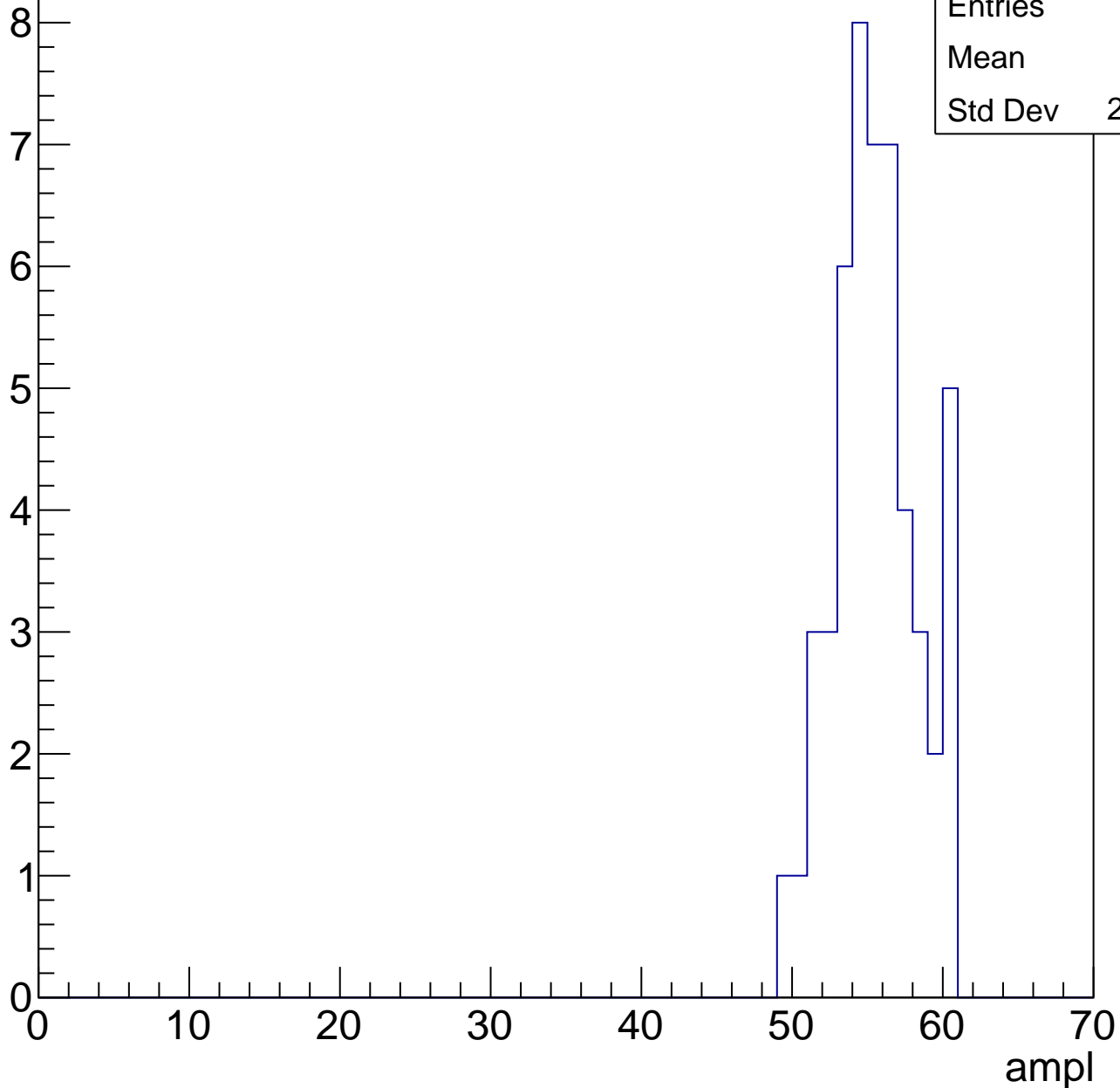


# B0L001S, U17-ch16, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	50
Mean	55.1
Std Dev	2.737

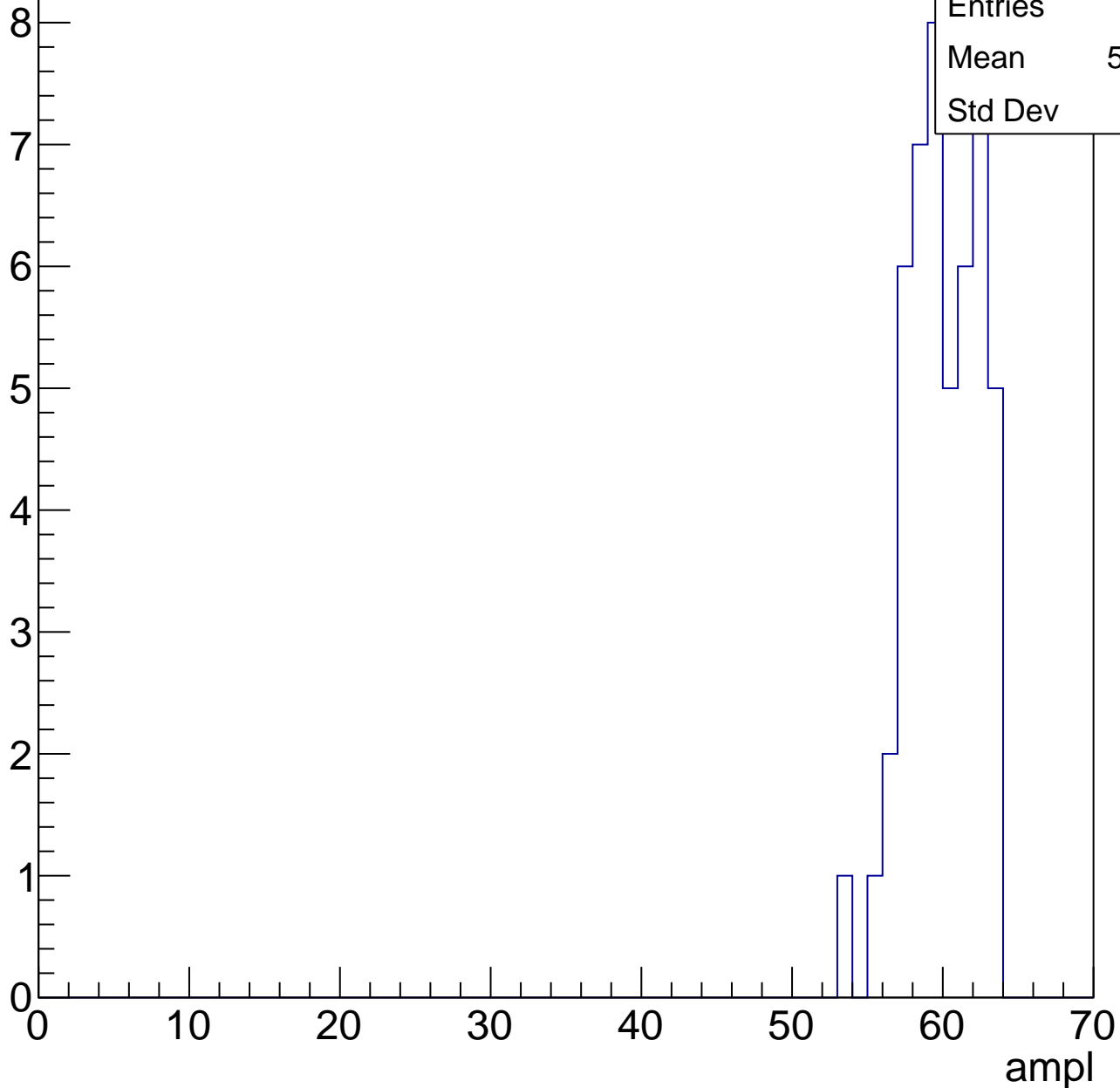


# B0L001S, U17-ch16, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

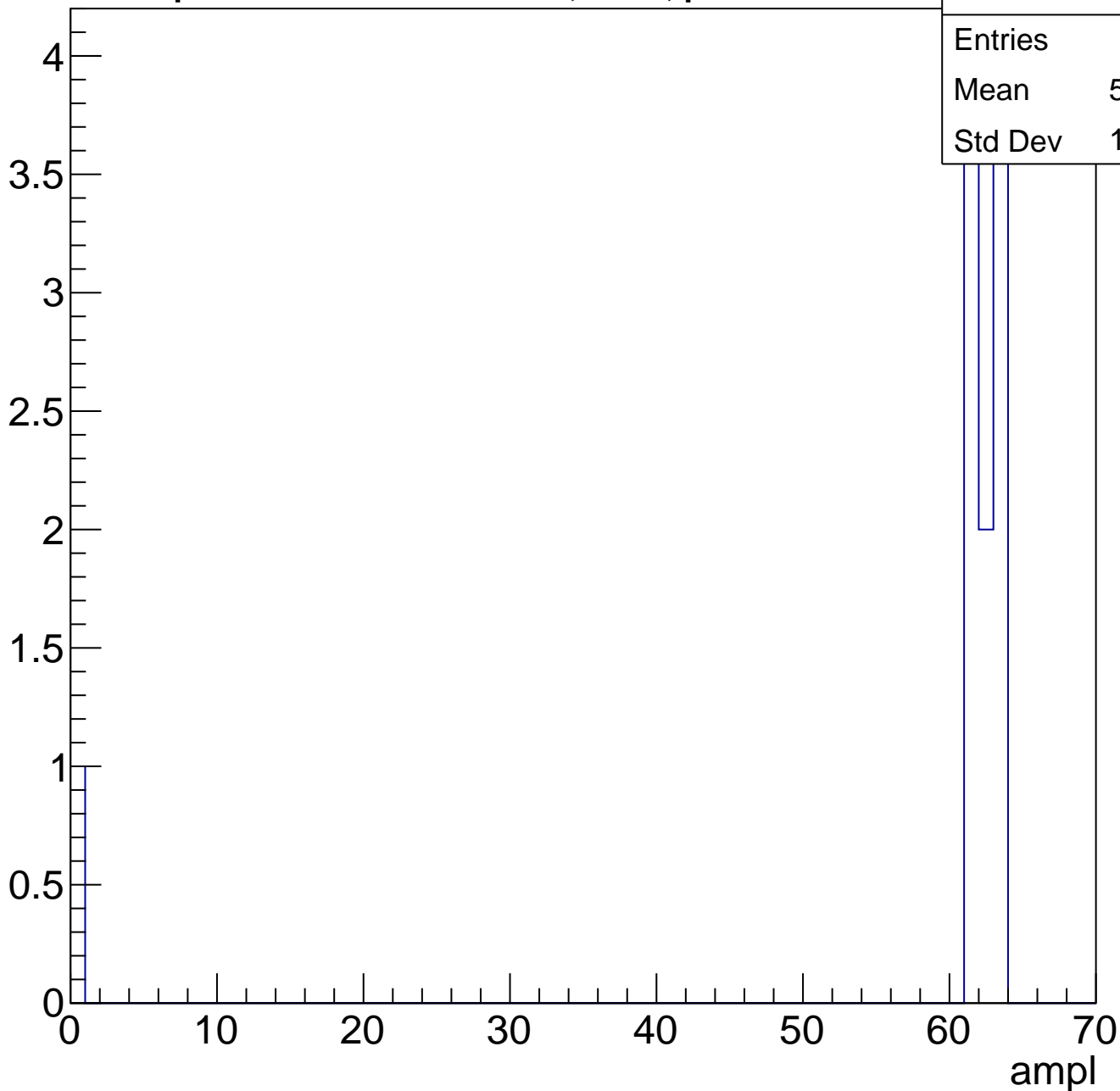
Entries	49
Mean	59.53
Std Dev	2.34



# B0L001S, U17-ch16, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch16, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U17-ch17, adc0

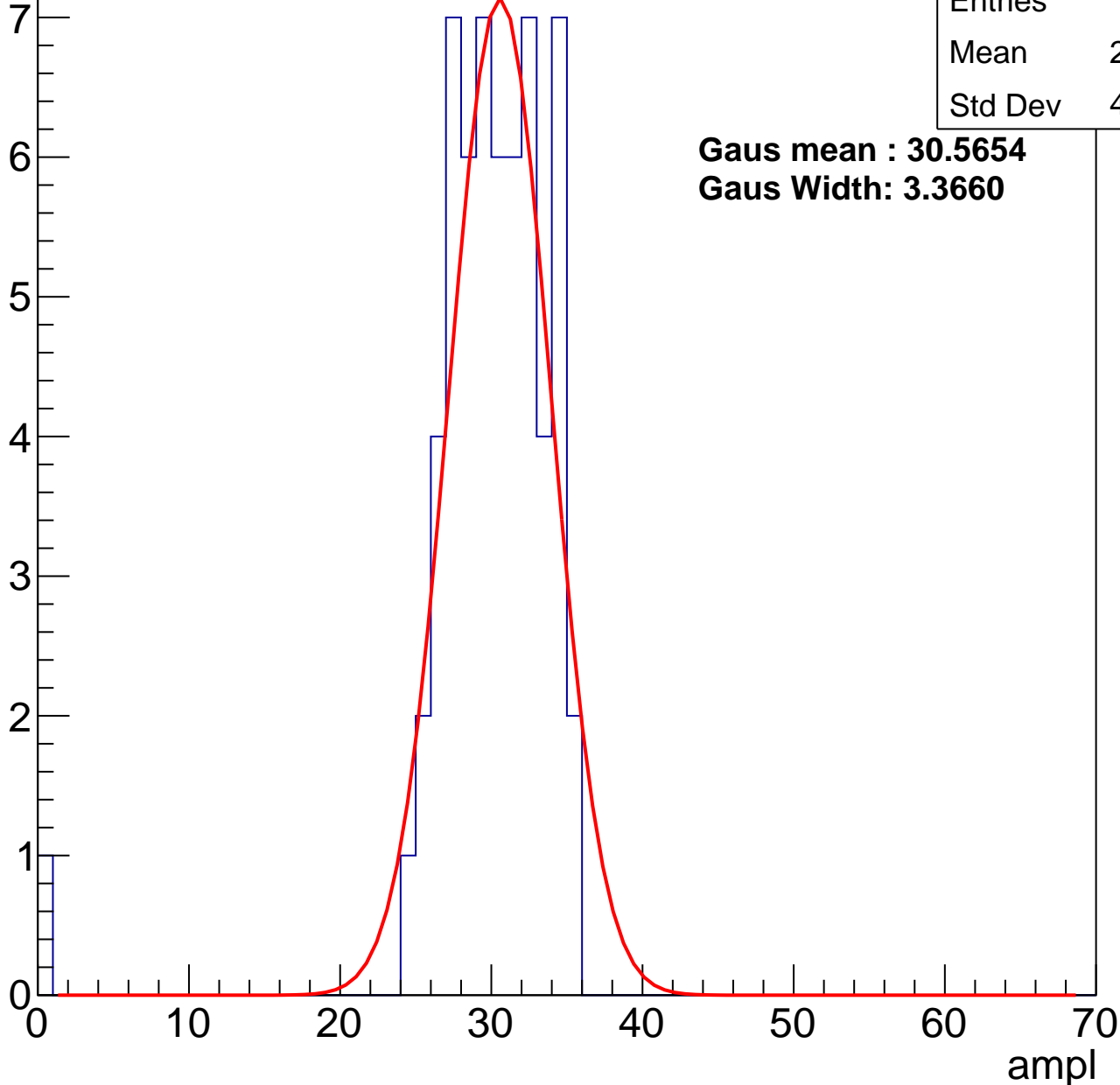
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	29.47
Std Dev	4.759

**Gaus mean : 30.5654**

**Gaus Width: 3.3660**



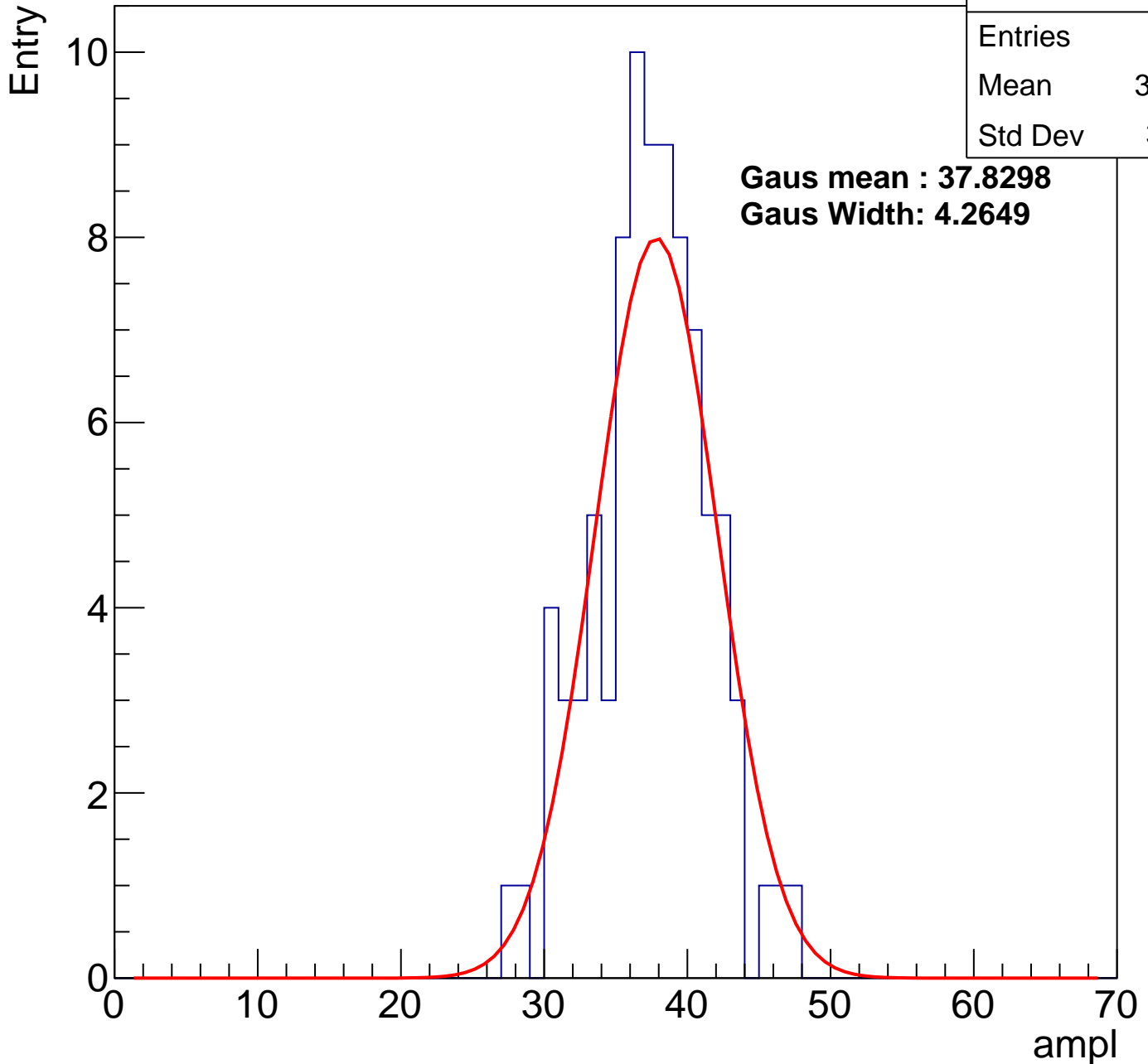
# B0L001S, U17-ch17, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	87
Mean	37.01
Std Dev	3.97

**Gaus mean : 37.8298**

**Gaus Width: 4.2649**

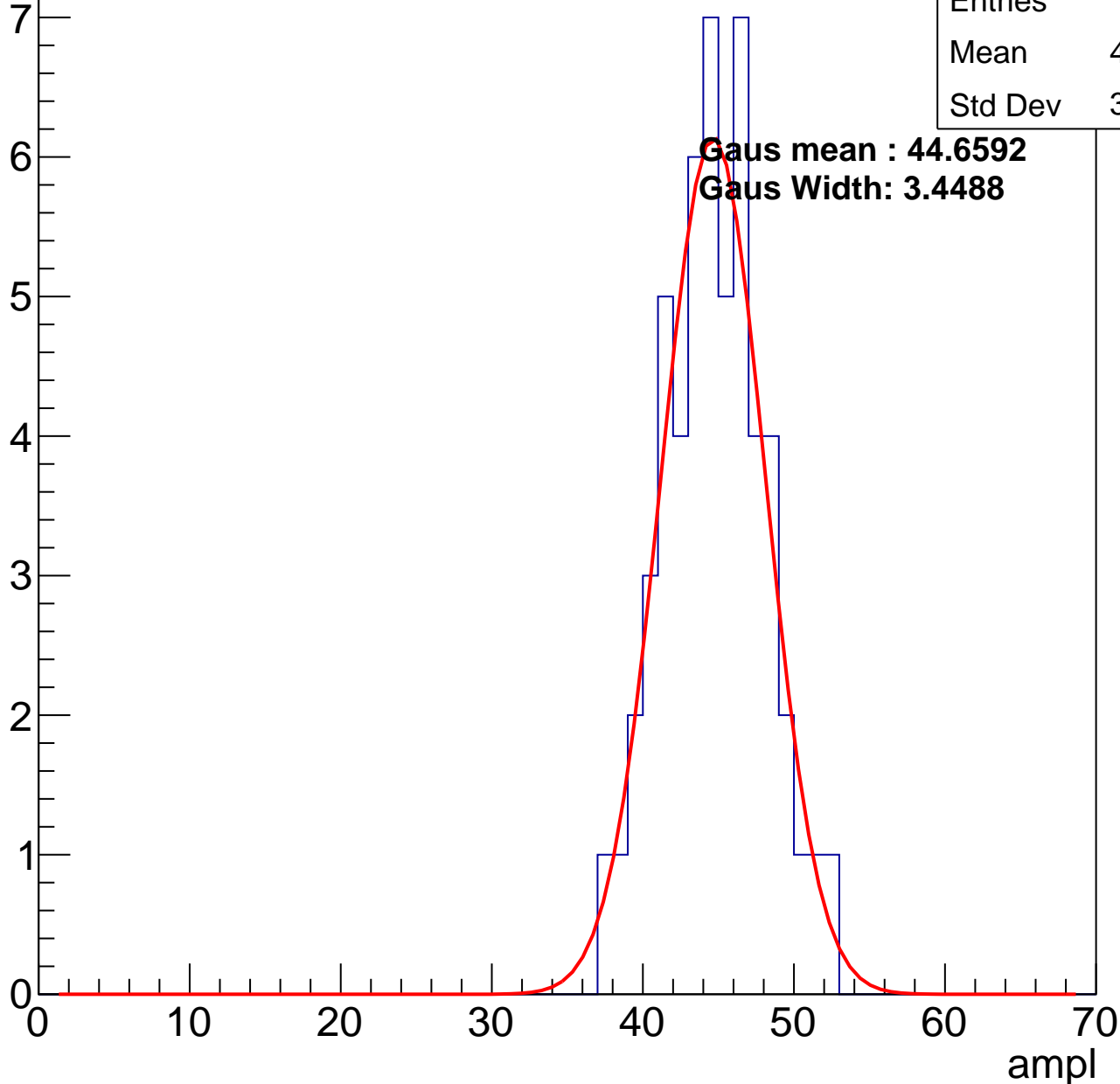


# B0L001S, U17-ch17, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	44.26
Std Dev	3.273

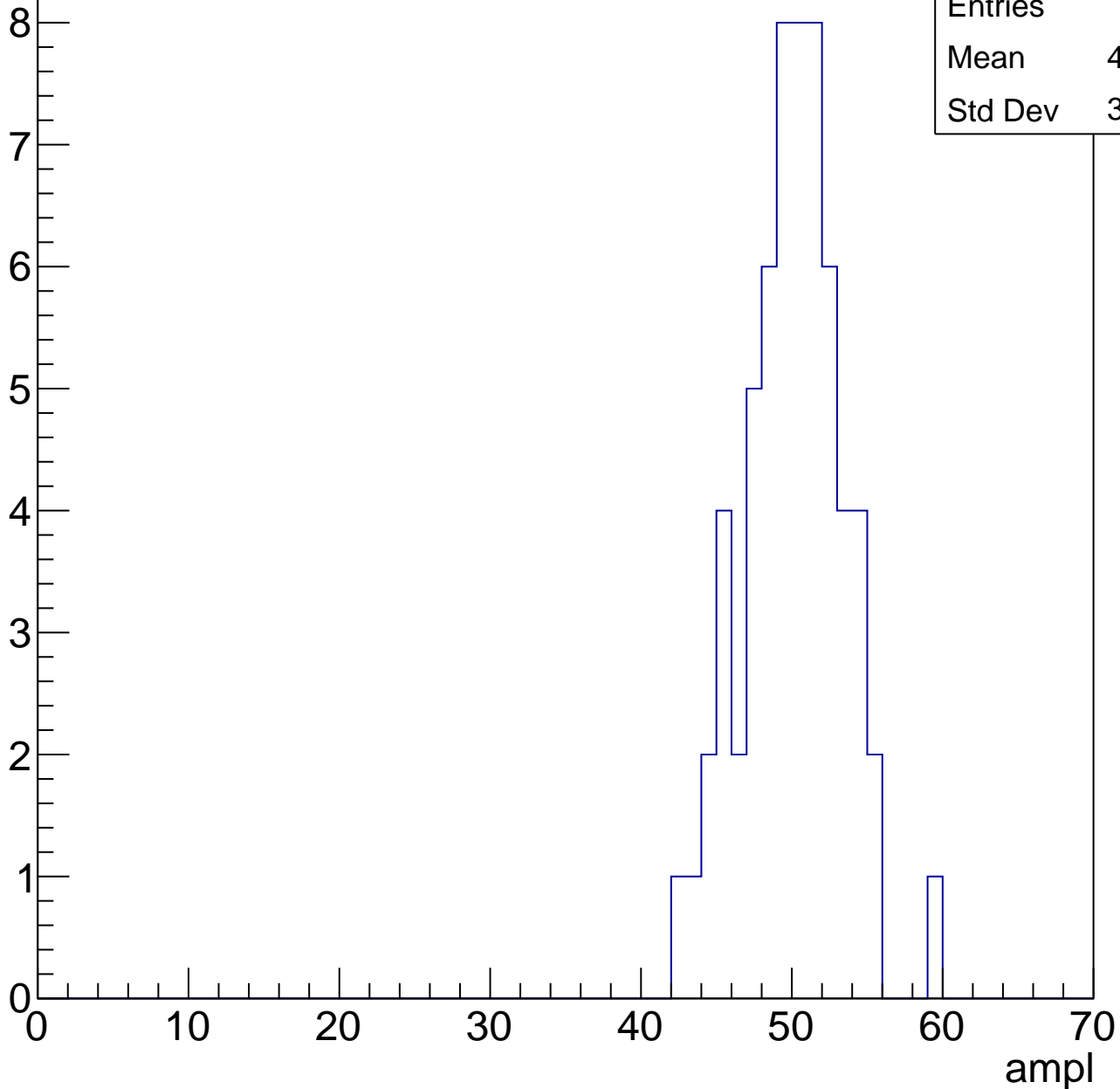


# B0L001S, U17-ch17, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	49.63
Std Dev	3.234

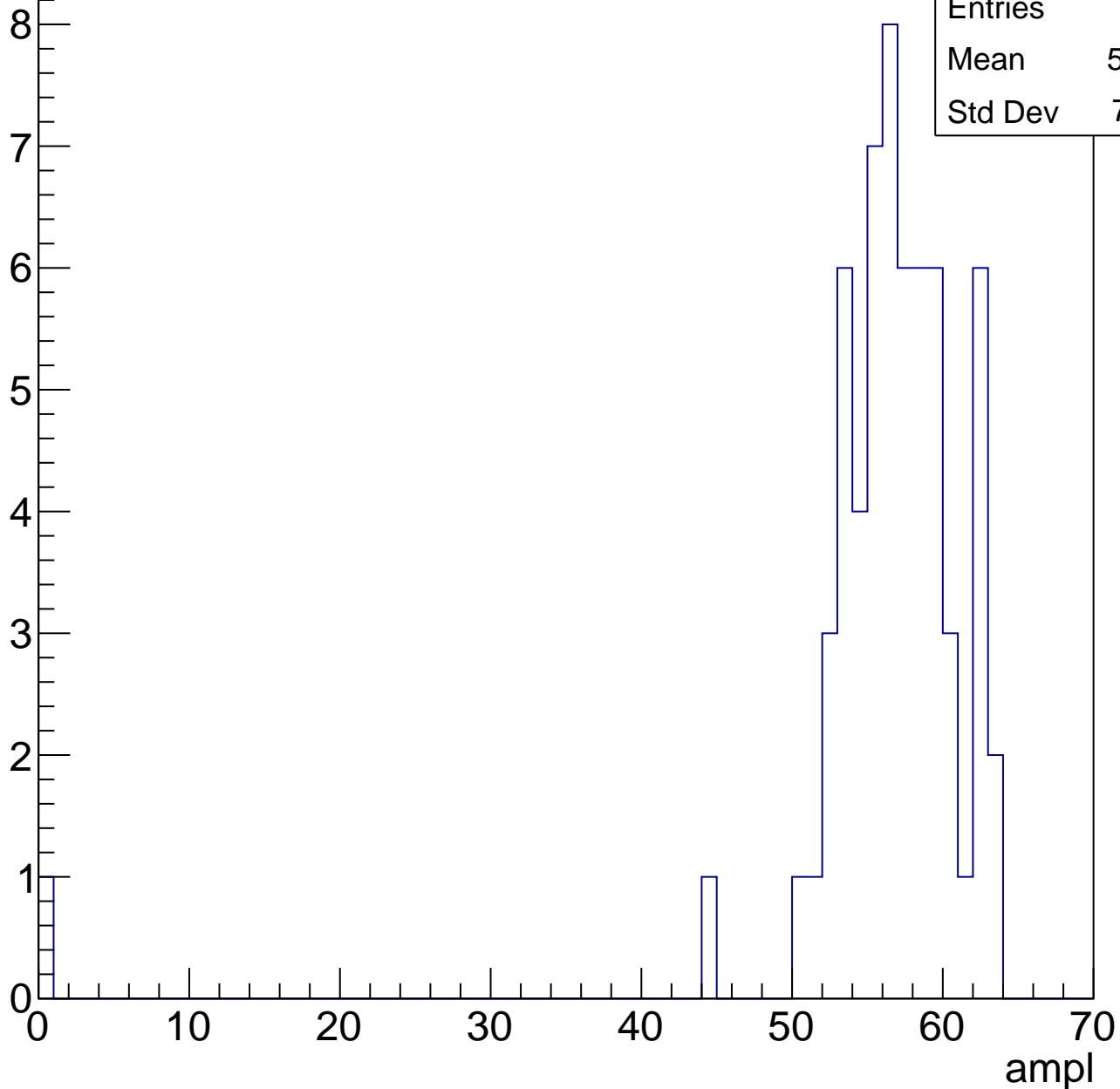


# B0L001S, U17-ch17, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	55.66
Std Dev	7.961

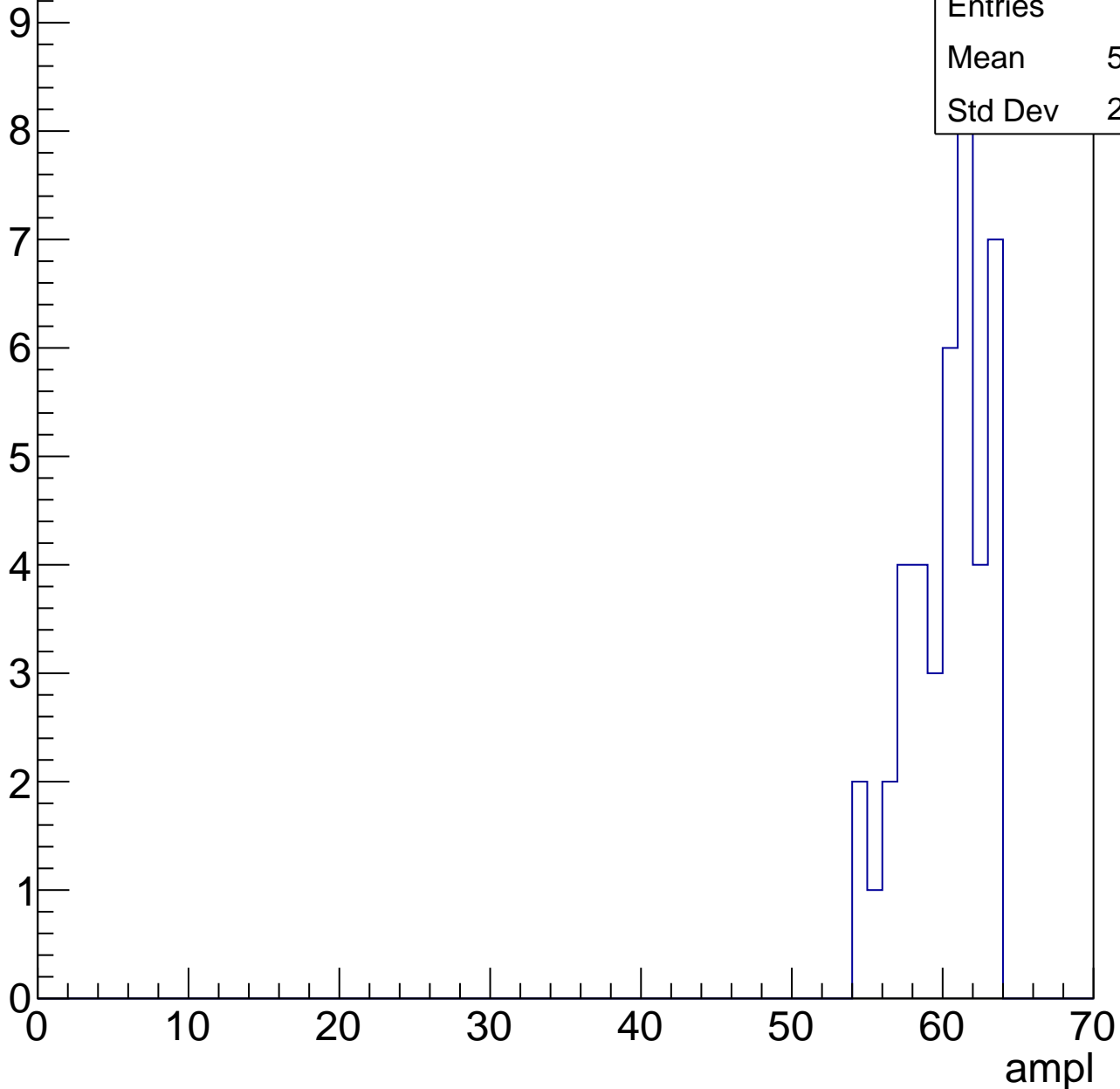


# B0L001S, U17-ch17, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	42
Mean	59.76
Std Dev	2.534



# B0L001S, U17-ch17, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch17, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U17-ch18, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	66
Mean	29.24
Std Dev	5.096

**Gaus mean : 30.9633**

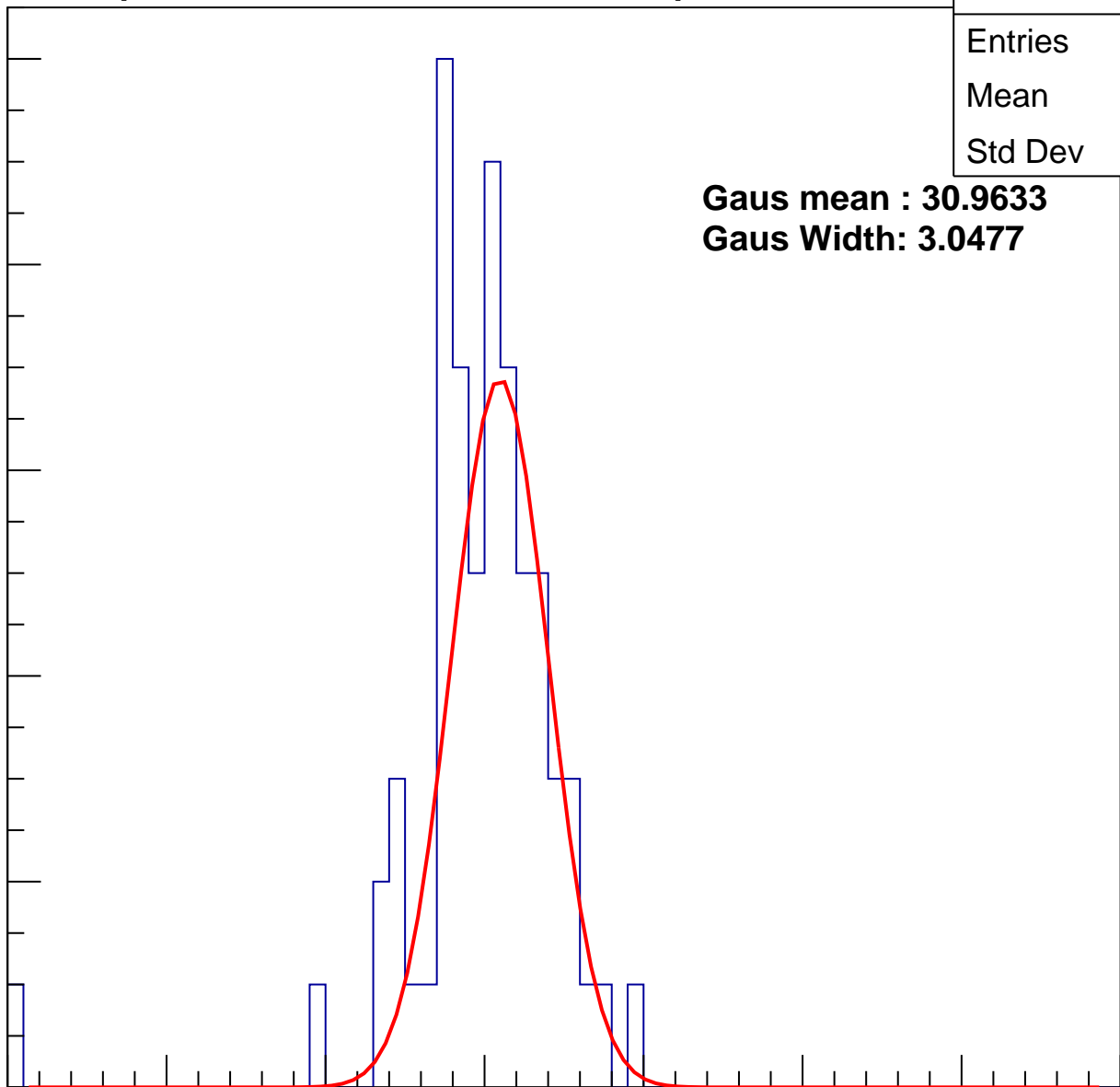
**Gaus Width: 3.0477**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



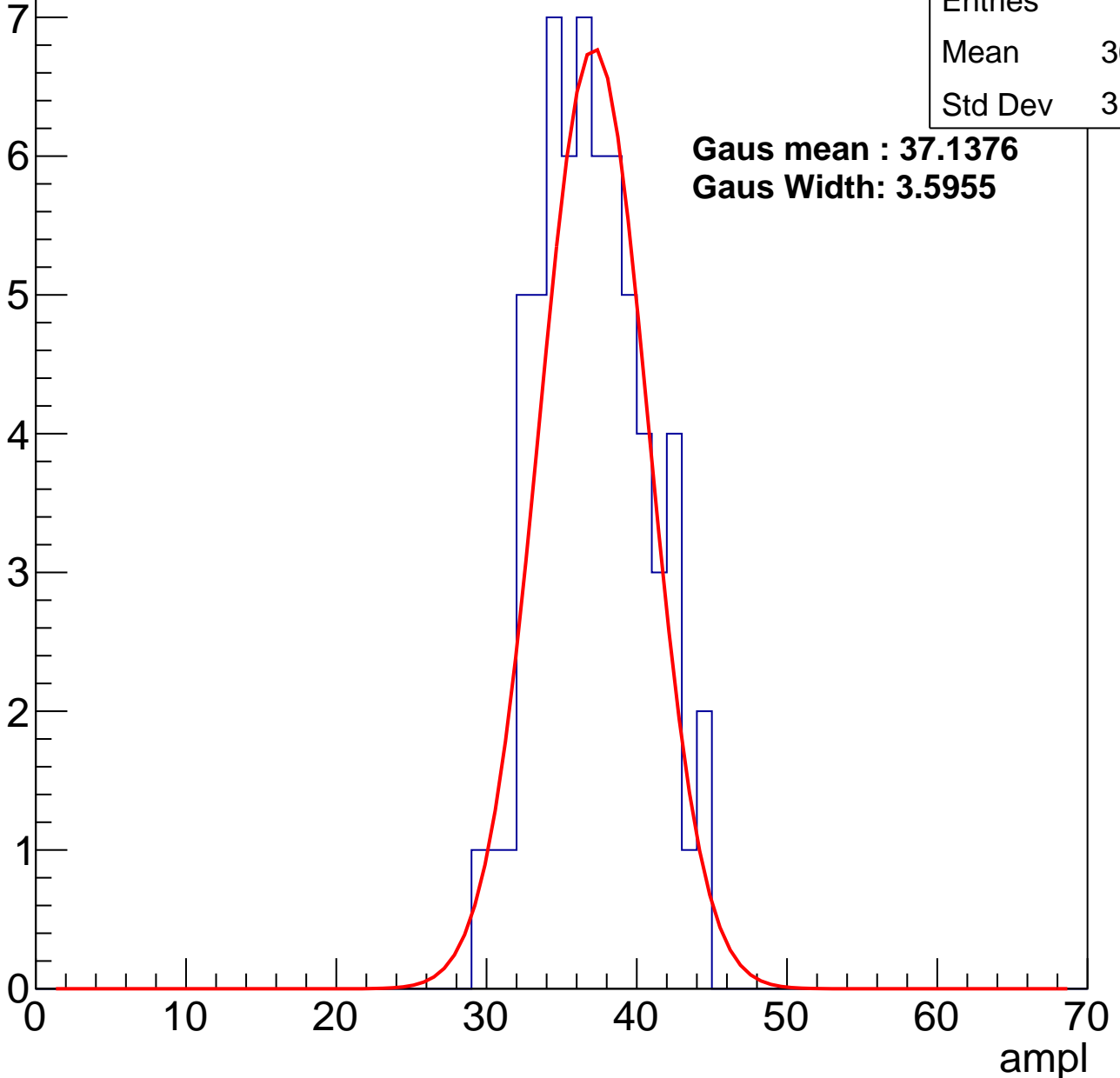
# B0L001S, U17-ch18, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	36.59
Std Dev	3.494

**Gaus mean : 37.1376**  
**Gaus Width: 3.5955**



# B0L001S, U17-ch18, adc2

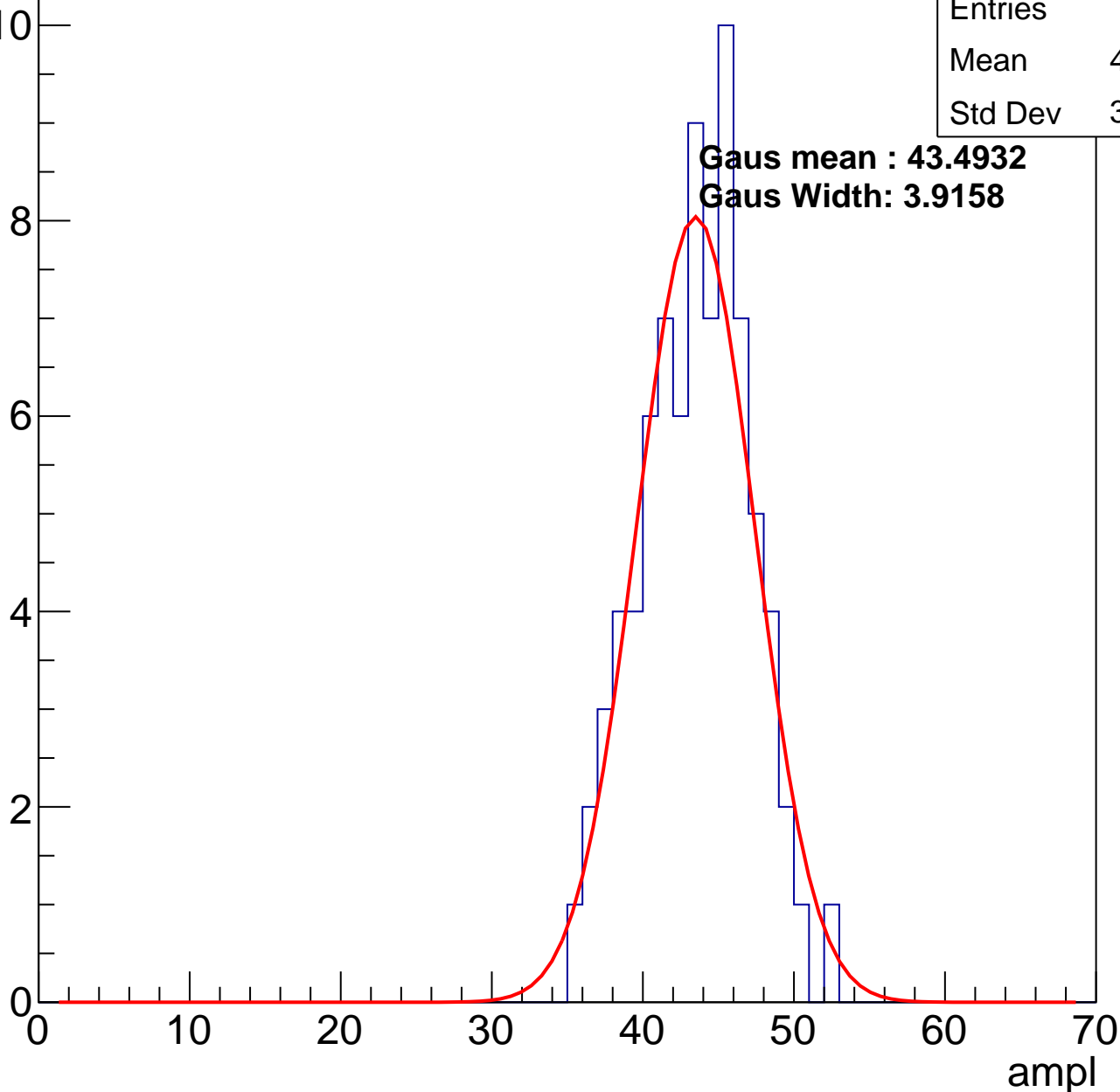
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	79
Mean	43.03
Std Dev	3.583

**Gaus mean : 43.4932**

**Gaus Width: 3.9158**

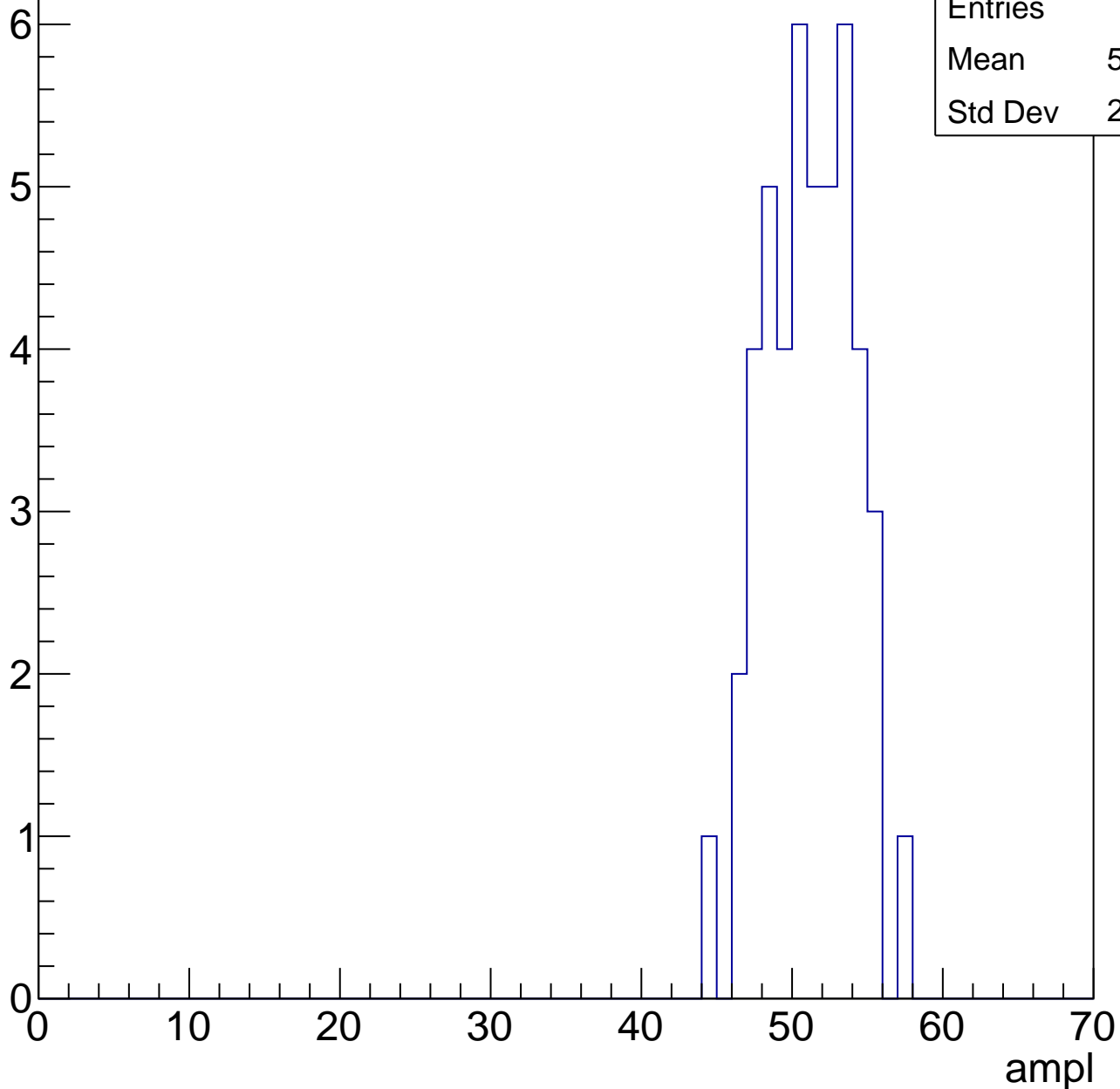


# B0L001S, U17-ch18, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	46
Mean	50.67
Std Dev	2.852

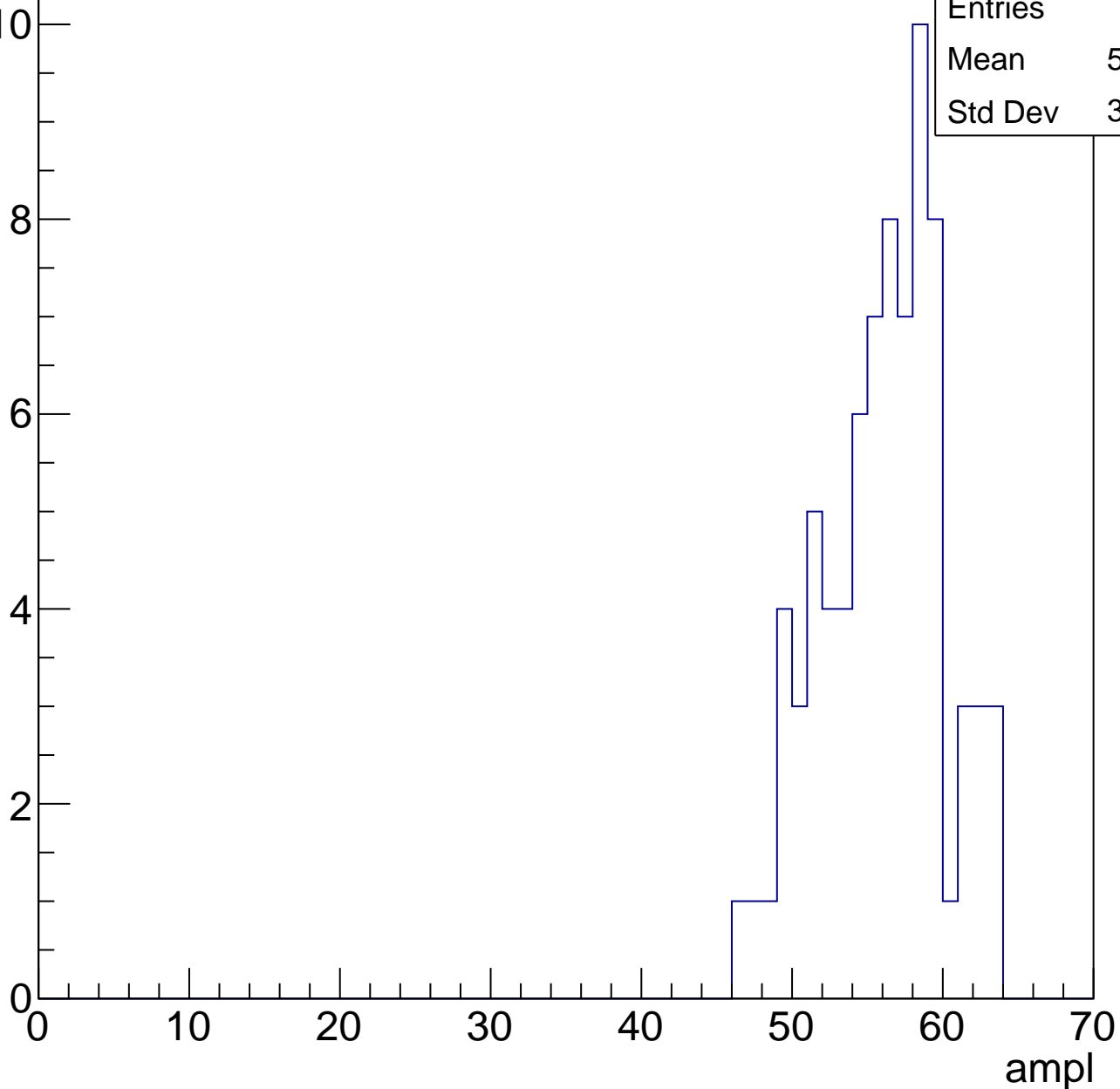


# B0L001S, U17-ch18, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

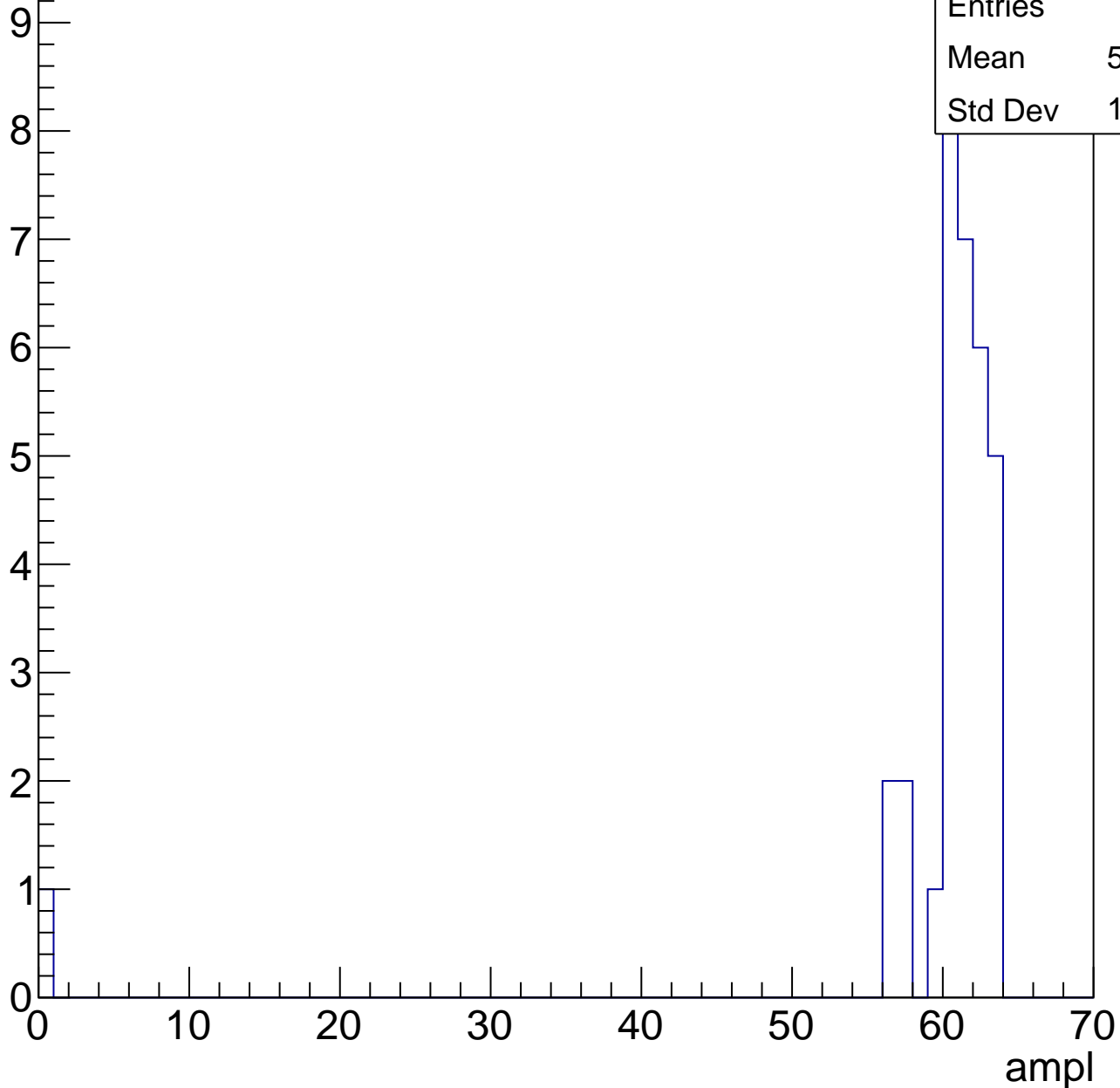
Entries	79
Mean	55.54
Std Dev	3.984



# B0L001S, U17-ch18, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

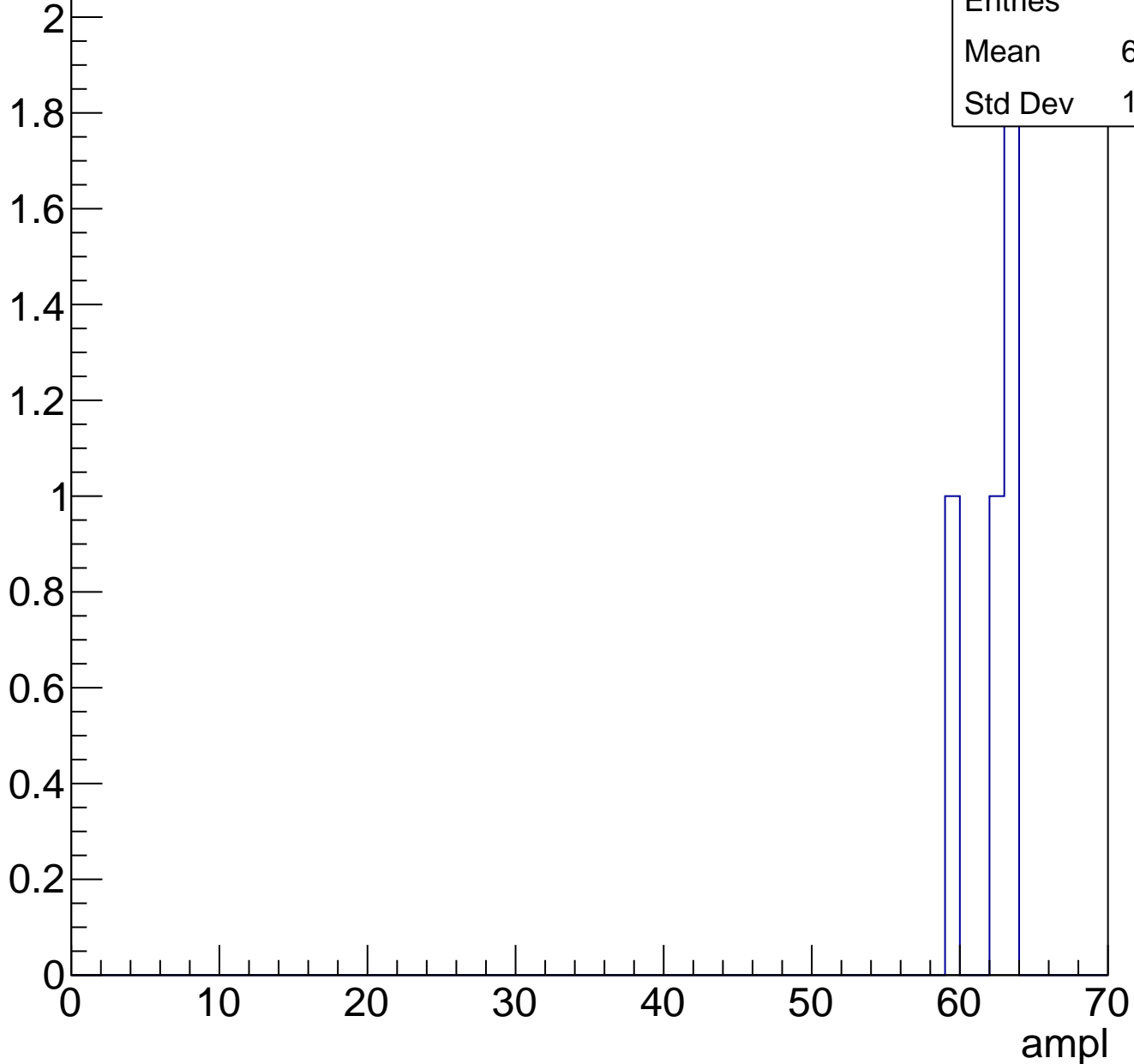
Entry



# B0L001S, U17-ch18, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch18, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U17-ch19, adc0

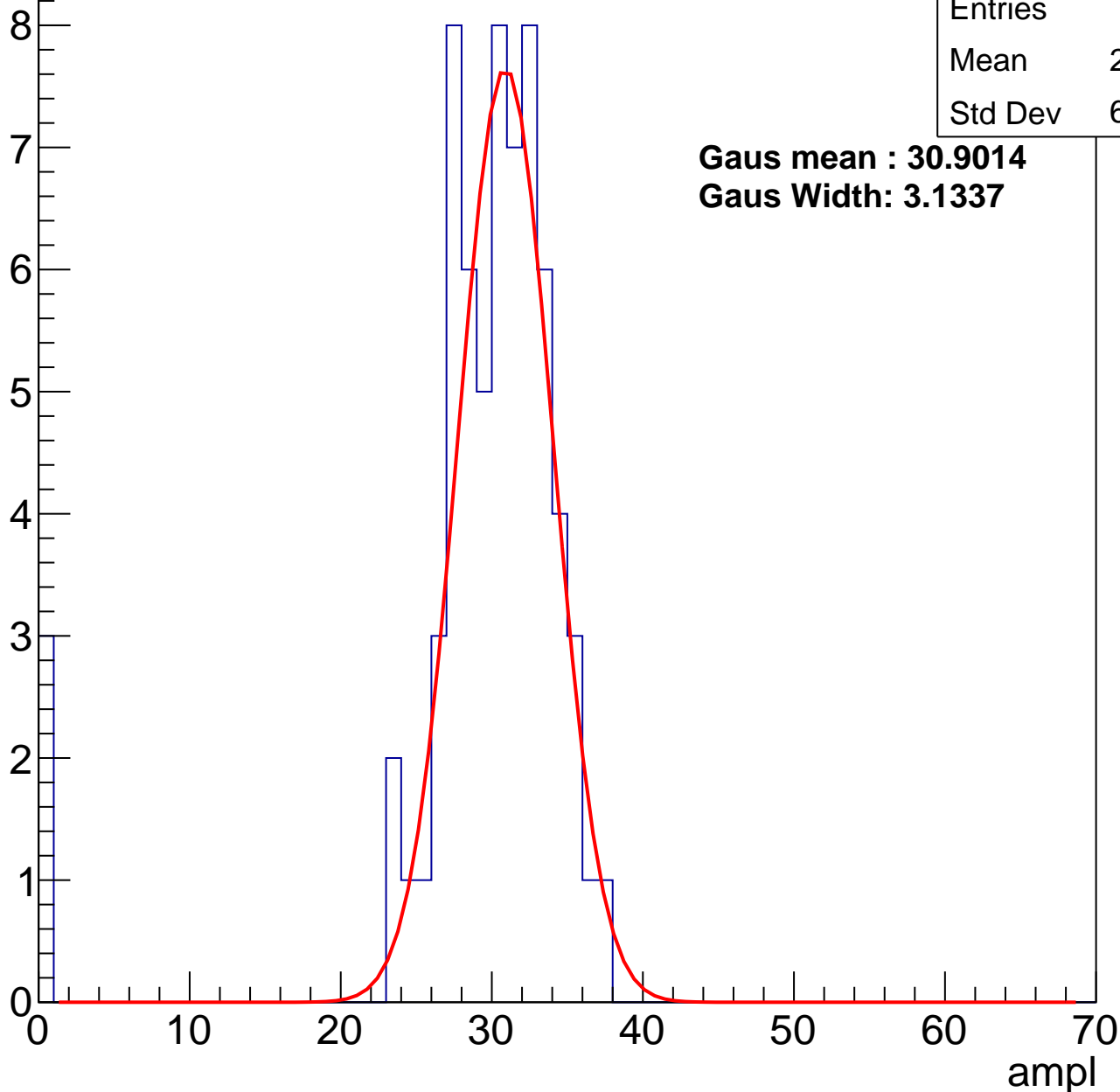
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	28.76
Std Dev	6.935

**Gaus mean : 30.9014**

**Gaus Width: 3.1337**



# B0L001S, U17-ch19, adc1

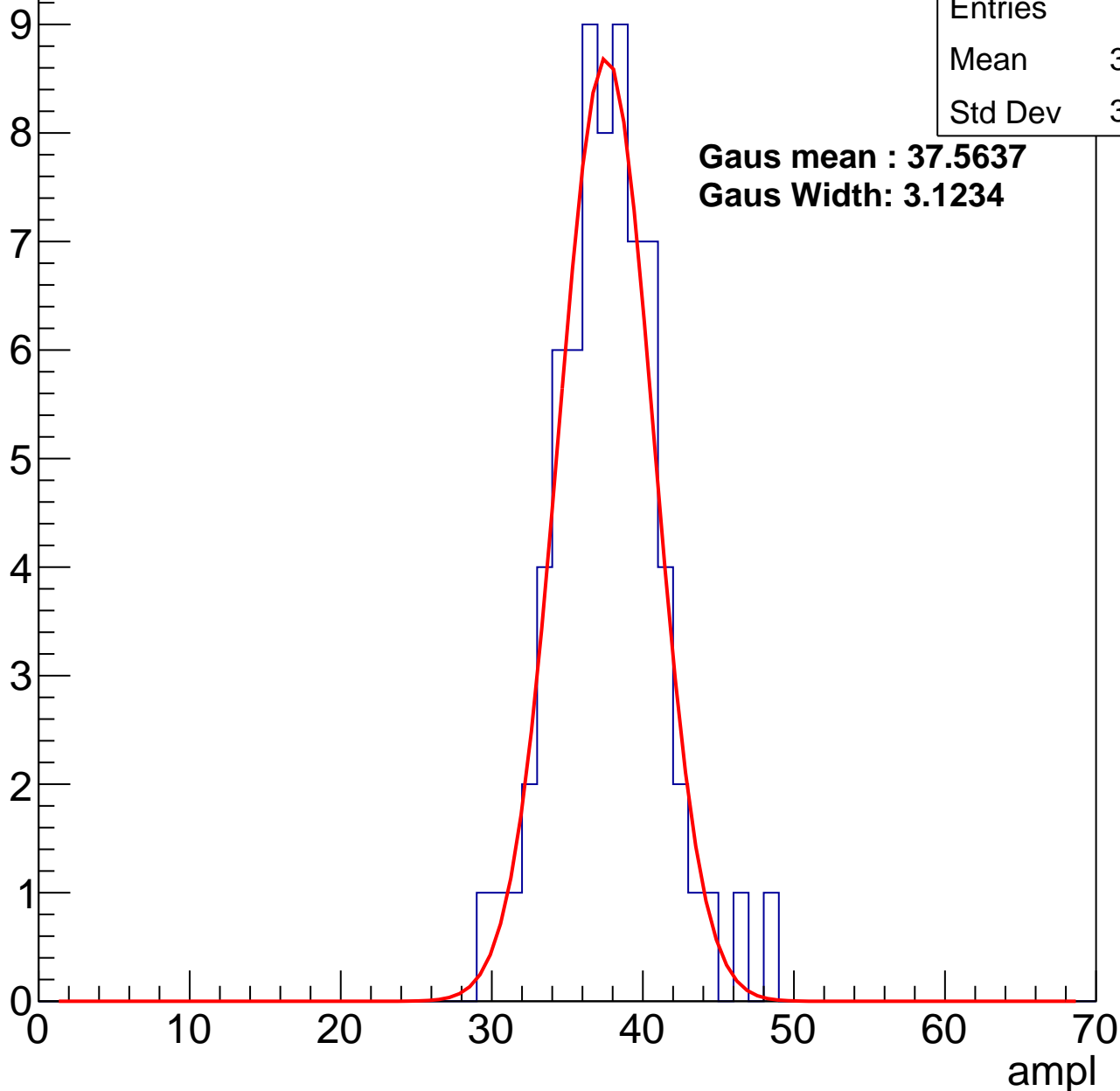
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	37.24
Std Dev	3.454

**Gaus mean : 37.5637**

**Gaus Width: 3.1234**



# B0L001S, U17-ch19, adc2

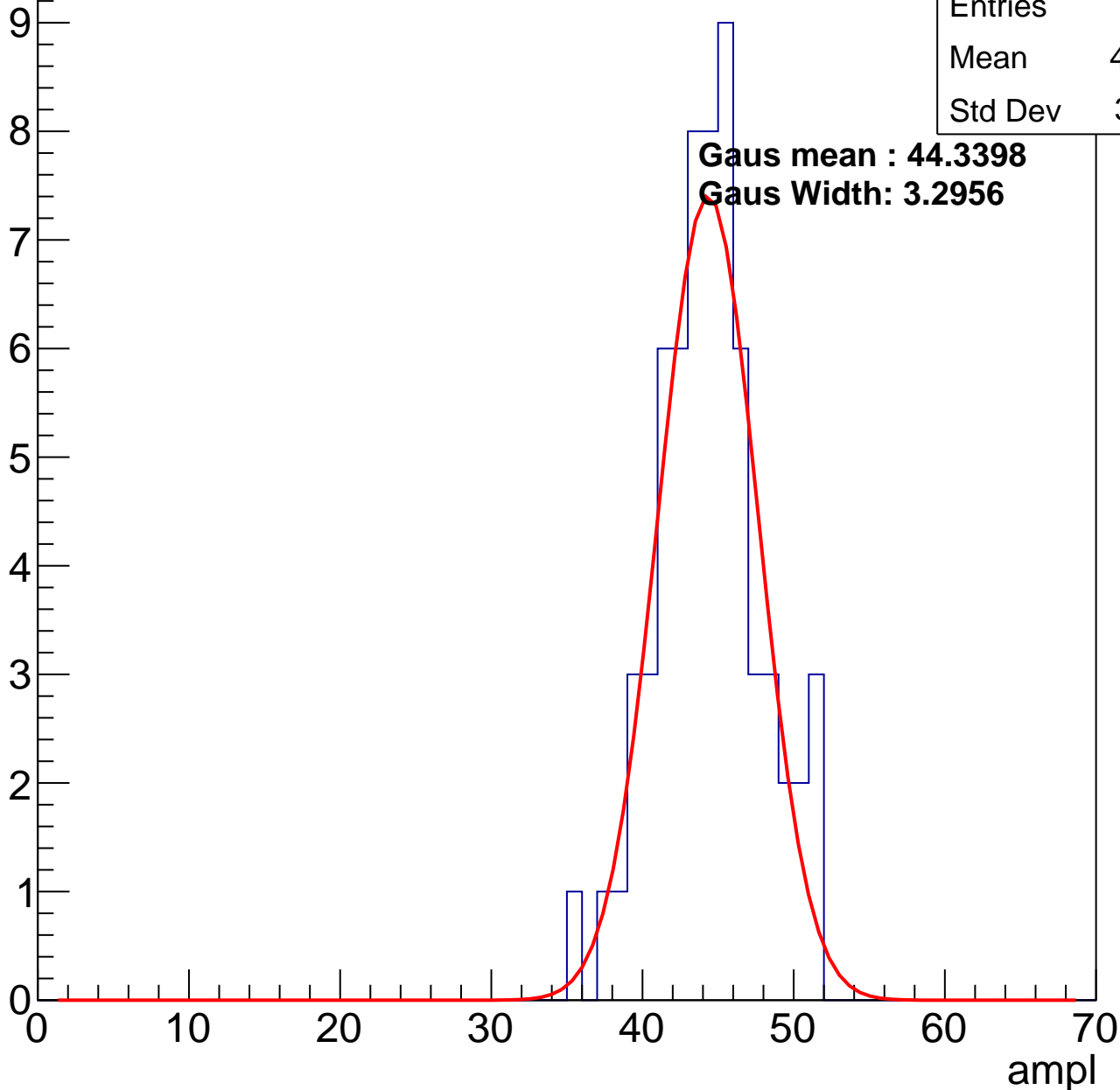
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	43.97
Std Dev	3.401

**Gaus mean : 44.3398**

**Gaus Width: 3.2956**

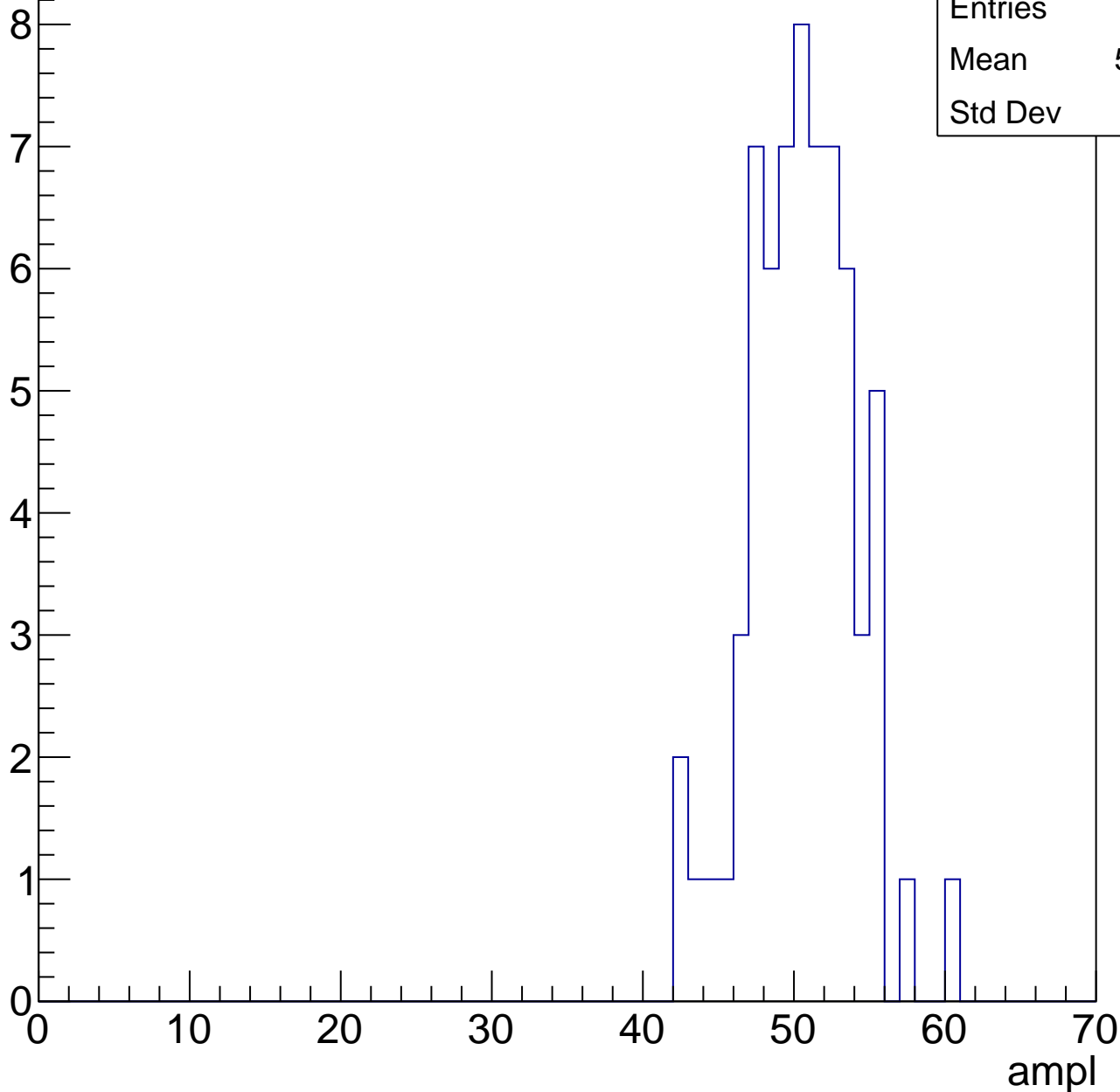


# B0L001S, U17-ch19, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	50.11
Std Dev	3.46



# B0L001S, U17-ch19, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	59
Mean	56.58
Std Dev	2.775

Entry

10

8

6

4

2

0

0

10

20

30

40

50

ampl

60

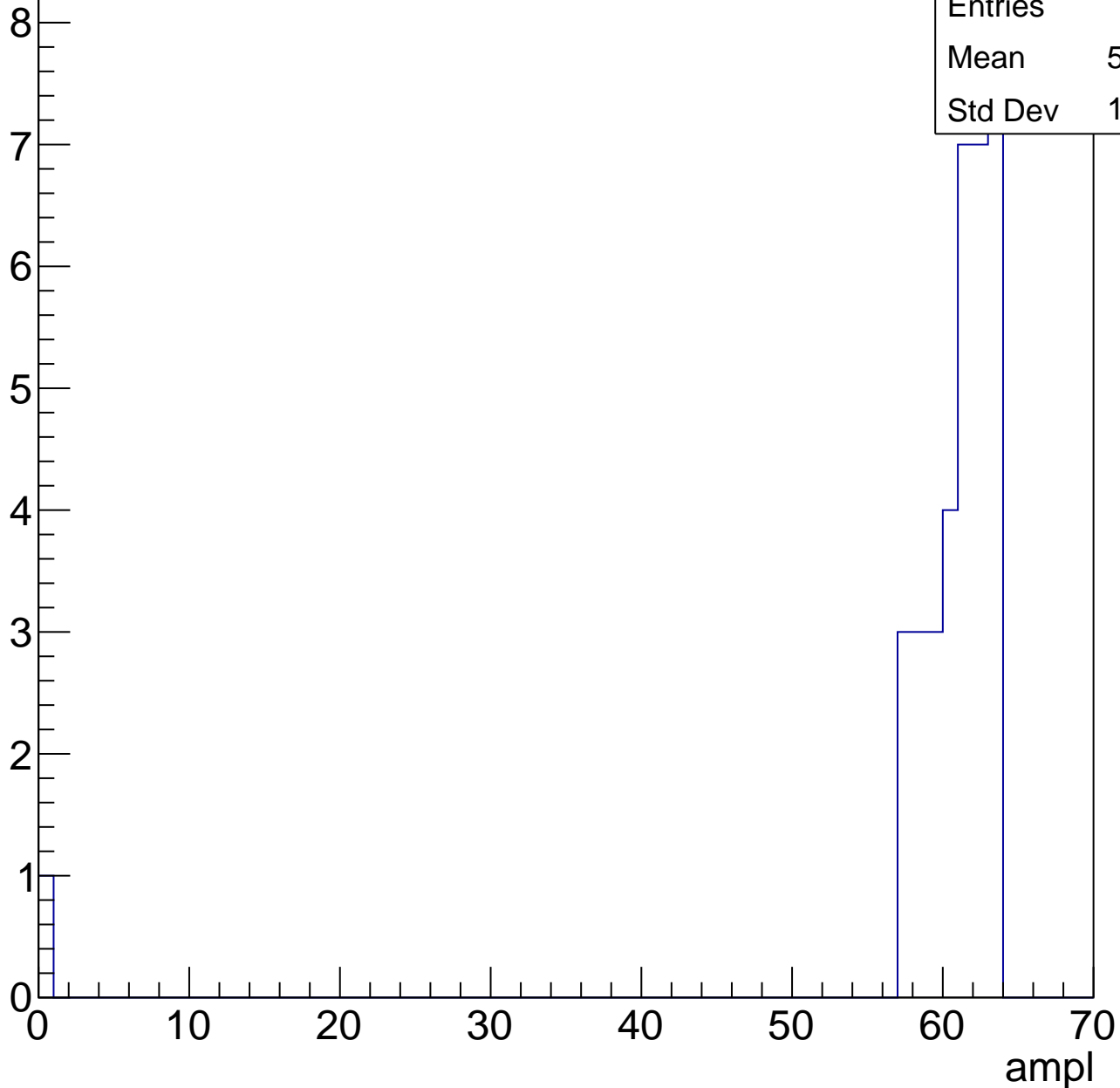
70

# B0L001S, U17-ch19, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	36
Mean	59.08
Std Dev	10.16



# B0L001S, U17-ch19, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch19, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L001S, U17-ch20, adc0

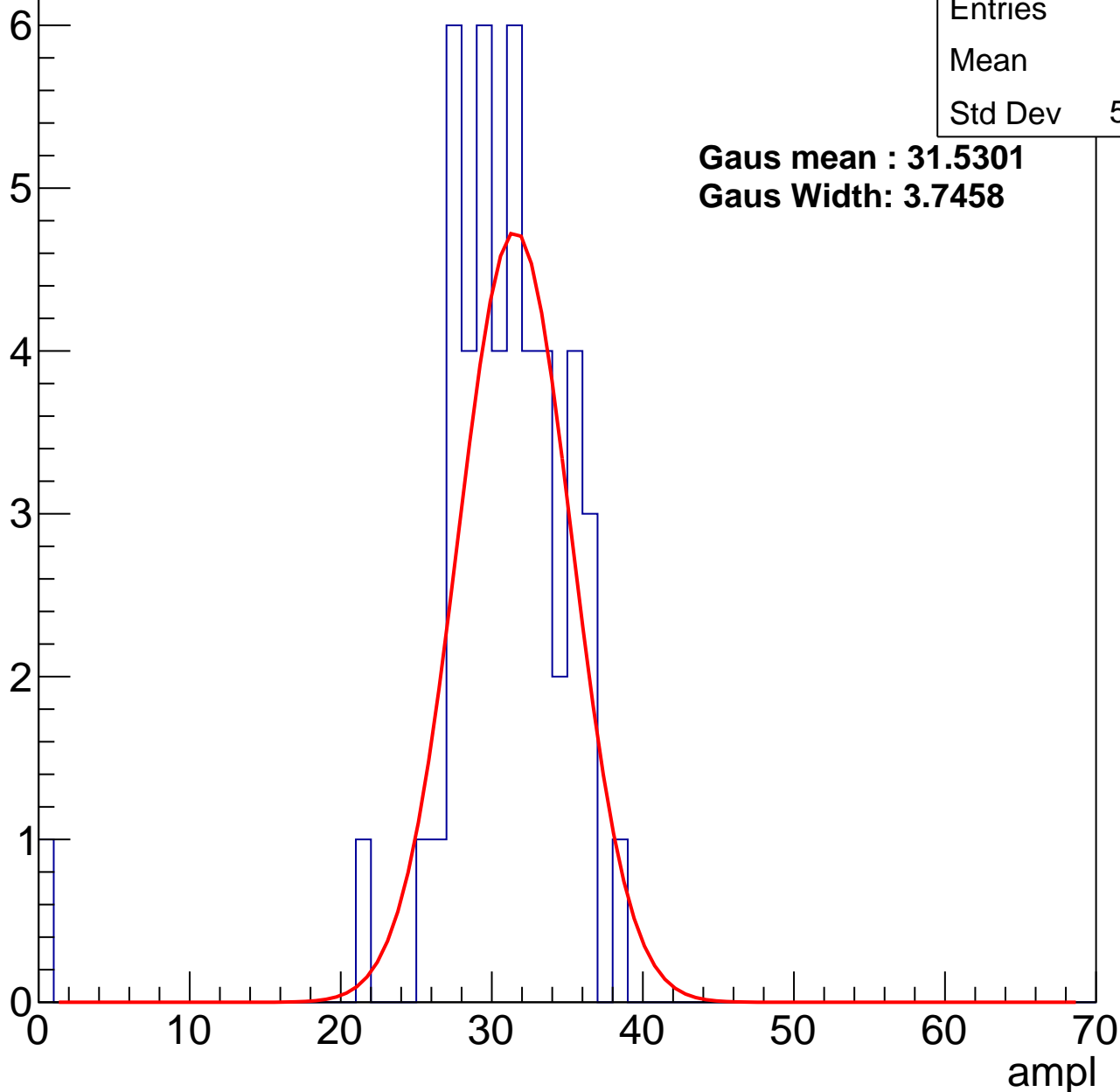
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	48
Mean	30
Std Dev	5.515

**Gaus mean : 31.5301**

**Gaus Width: 3.7458**



# B0L001S, U17-ch20, adc1

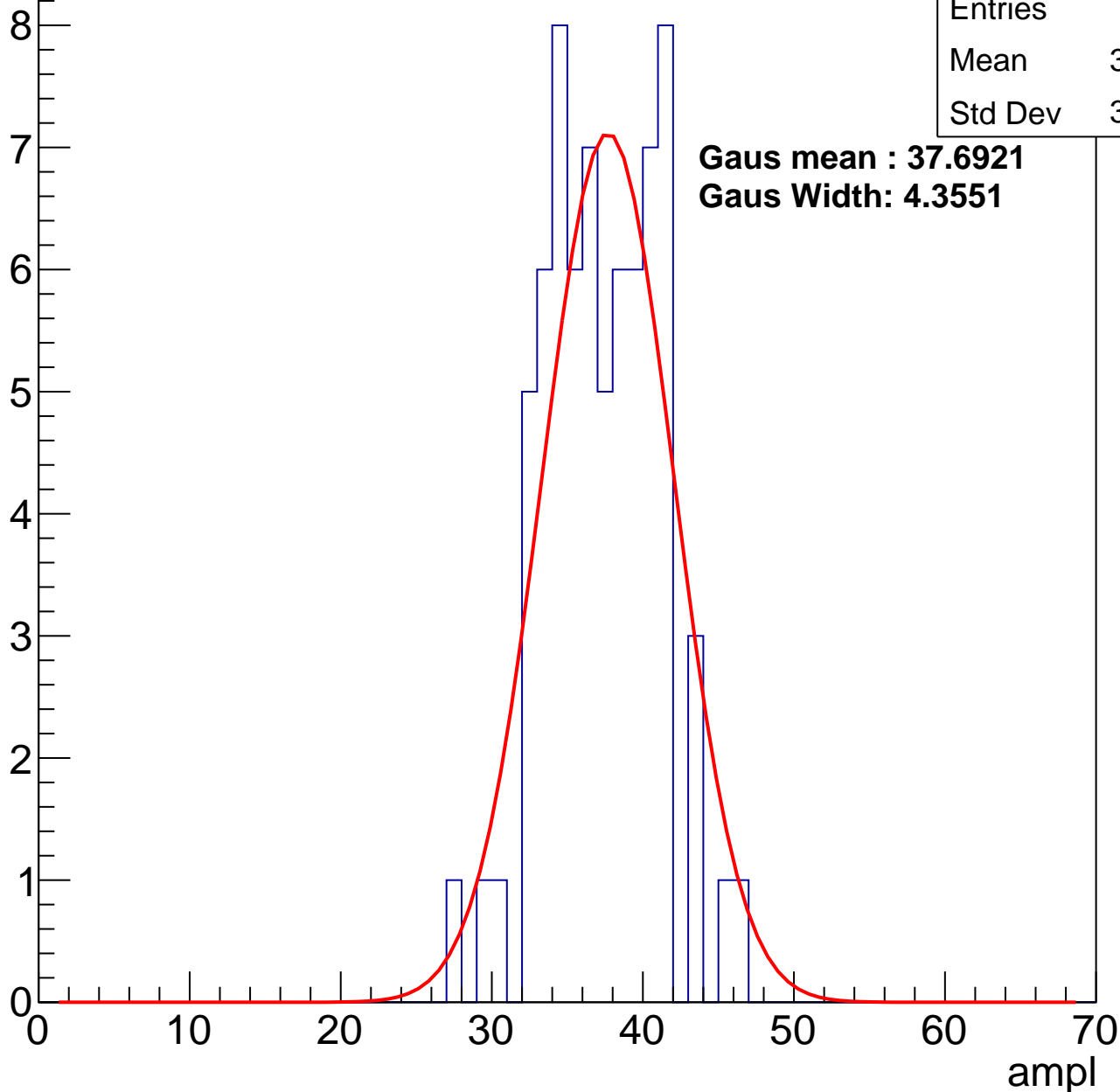
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	36.85
Std Dev	3.744

**Gaus mean : 37.6921**

**Gaus Width: 4.3551**



# B0L001S, U17-ch20, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	65
Mean	43.15
Std Dev	3.315

**Gaus mean : 44.4584**

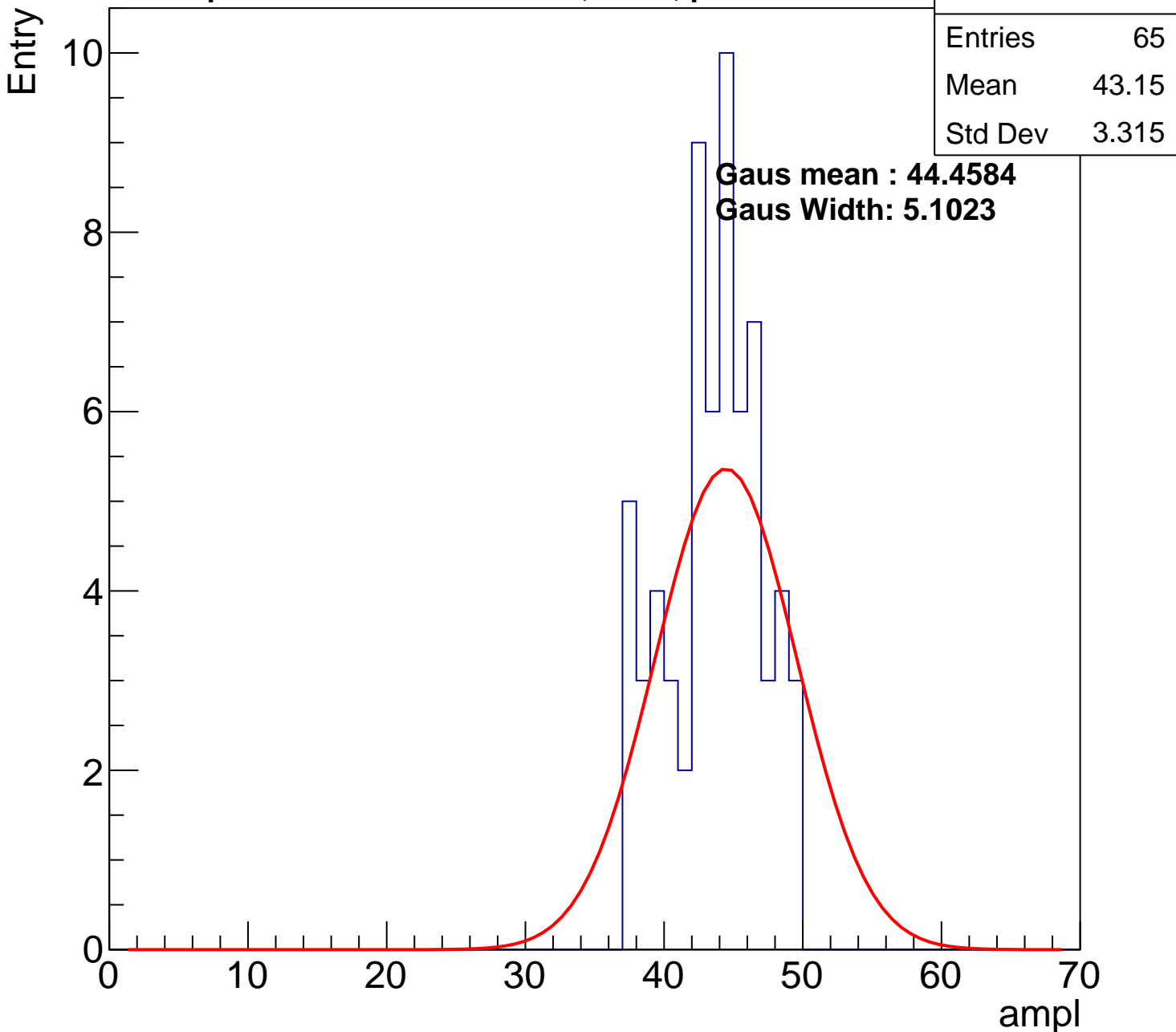
**Gaus Width: 5.1023**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

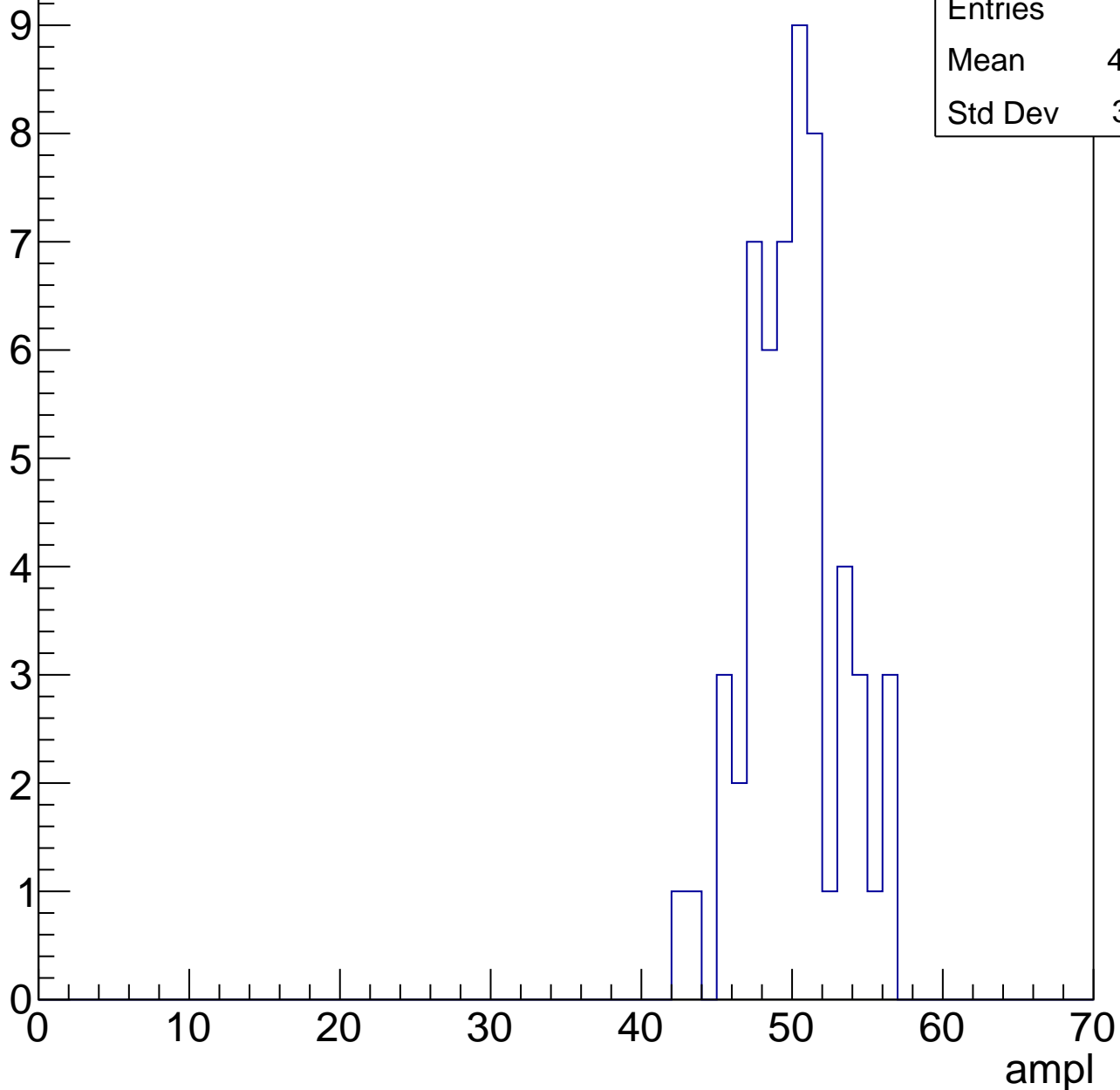


# B0L001S, U17-ch20, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	49.62
Std Dev	3.091

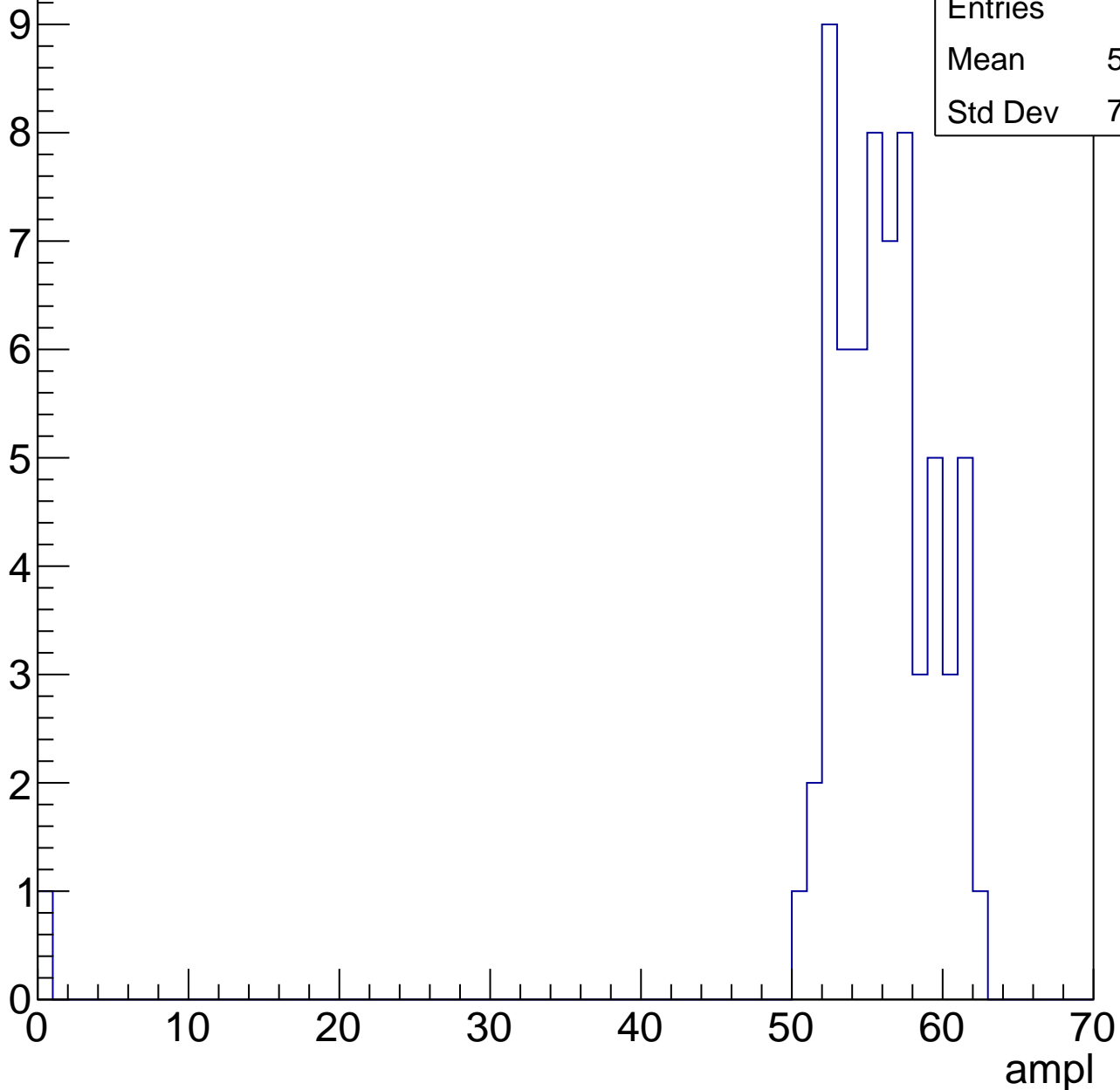


# B0L001S, U17-ch20, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	54.86
Std Dev	7.485

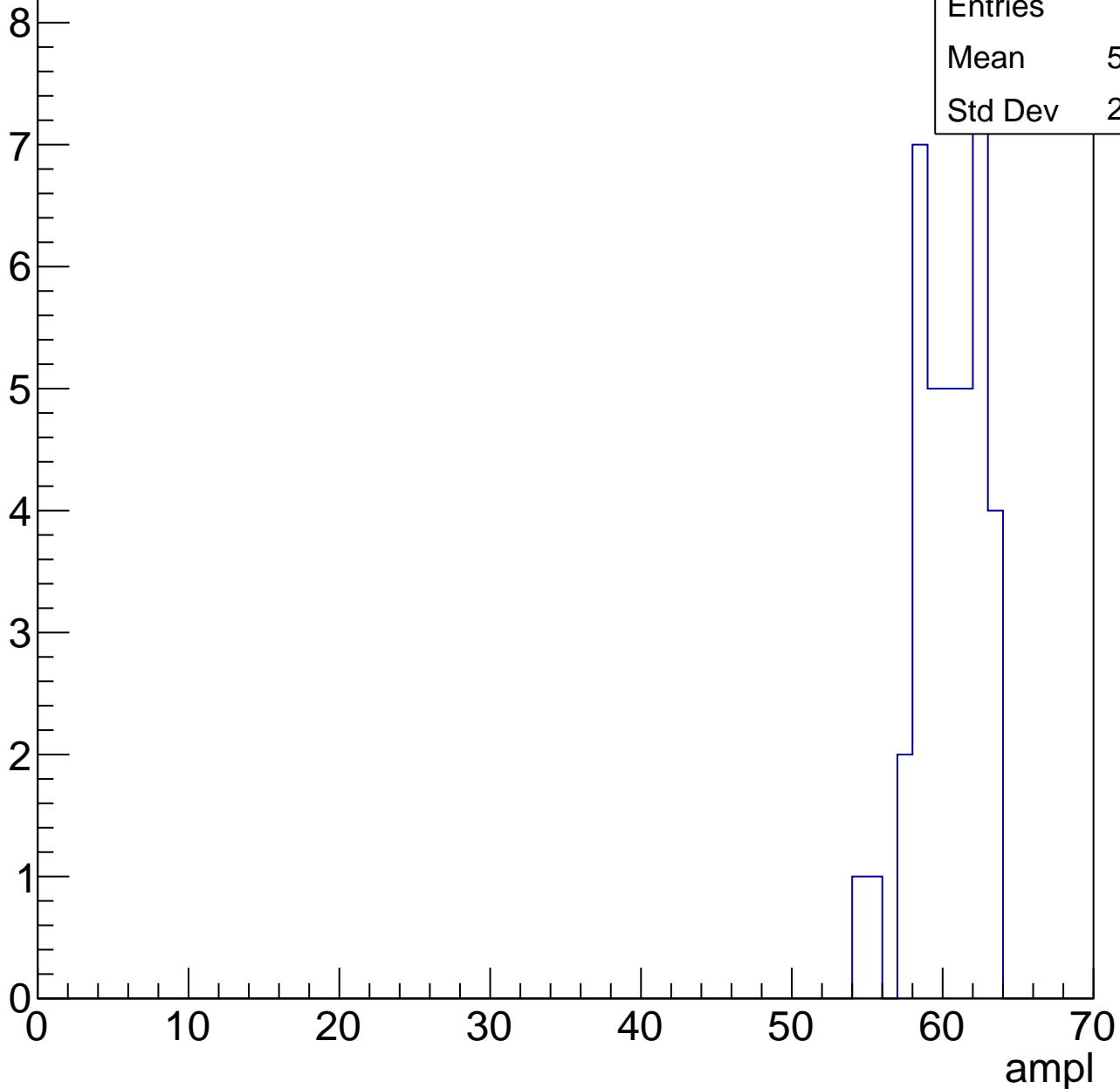


# B0L001S, U17-ch20, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	38
Mean	59.92
Std Dev	2.205

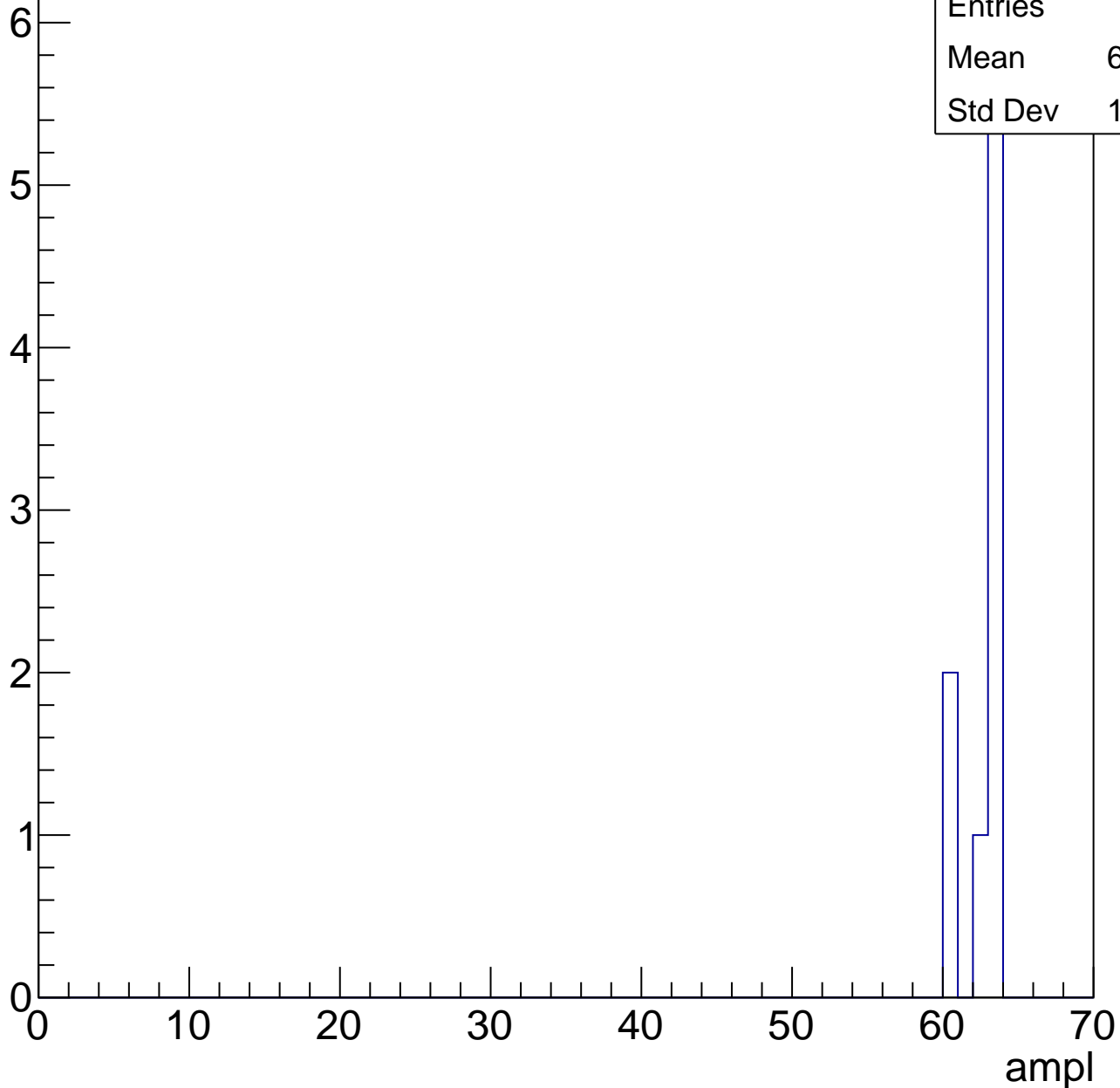


# B0L001S, U17-ch20, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	9
Mean	62.22
Std Dev	1.227





# B0L001S, U17-ch20, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U17-ch21, adc0

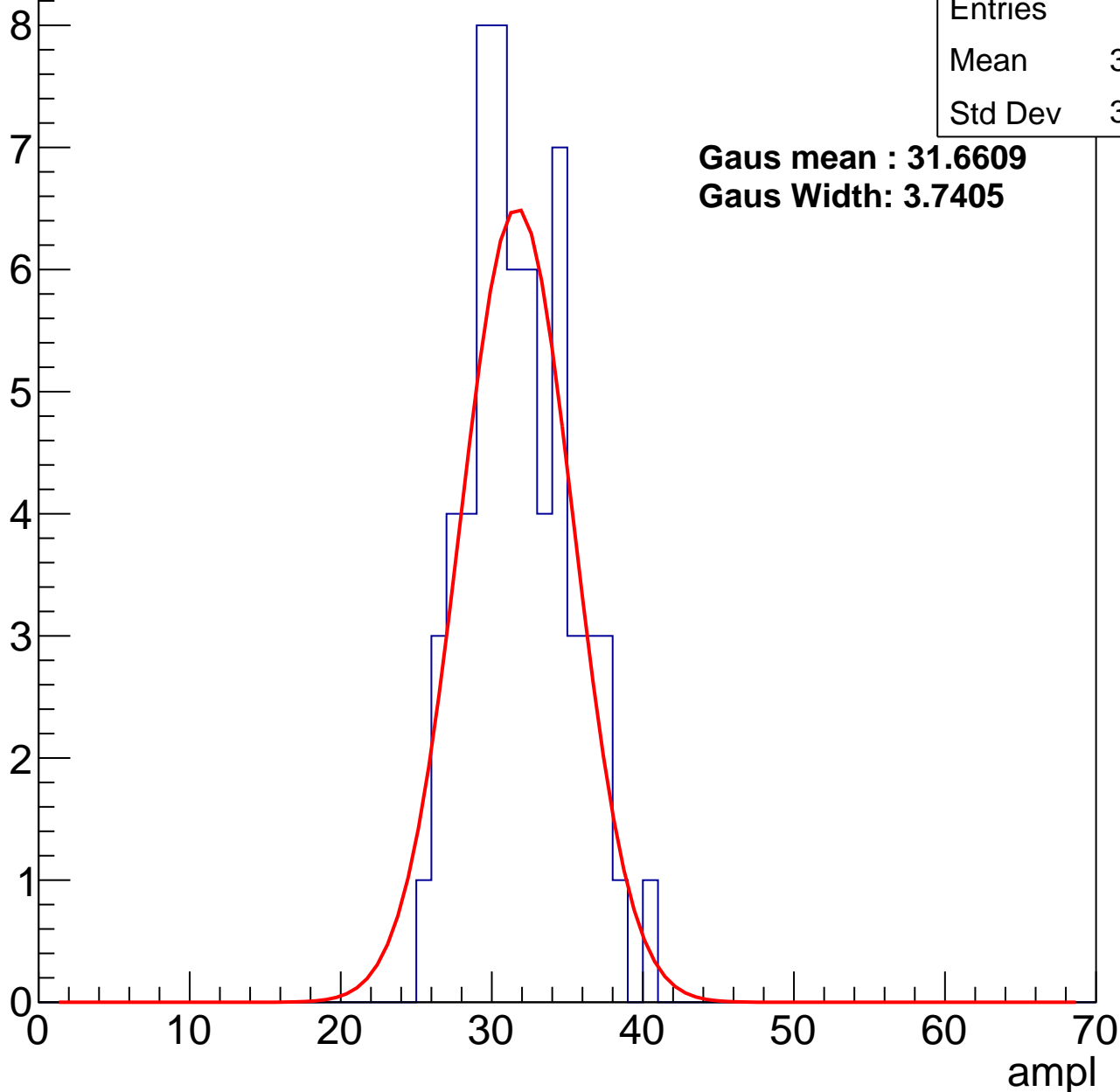
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	31.37
Std Dev	3.332

**Gaus mean : 31.6609**

**Gaus Width: 3.7405**



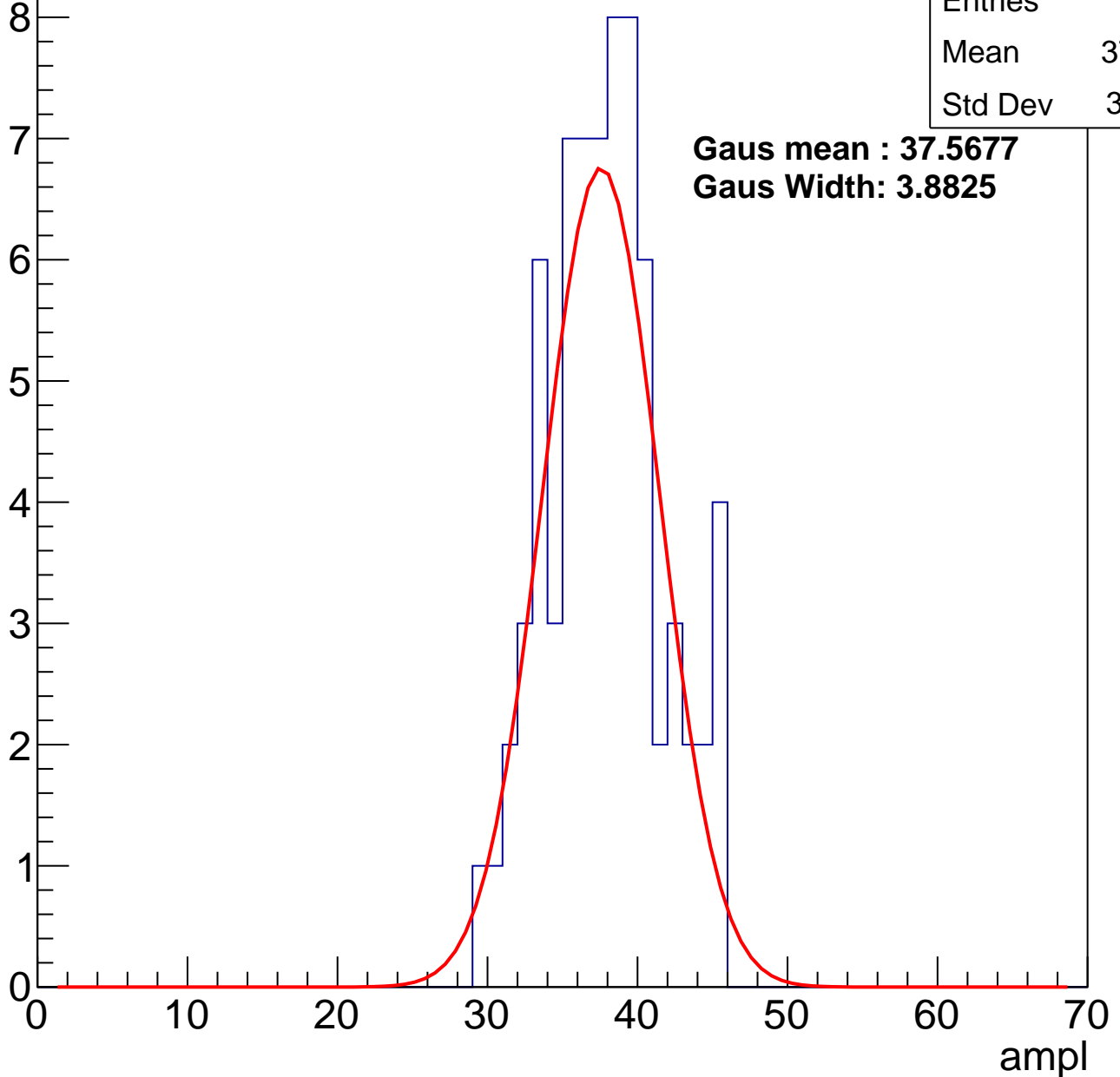
# B0L001S, U17-ch21, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	37.38
Std Dev	3.791

**Gaus mean : 37.5677**  
**Gaus Width: 3.8825**



# B0L001S, U17-ch21, adc2

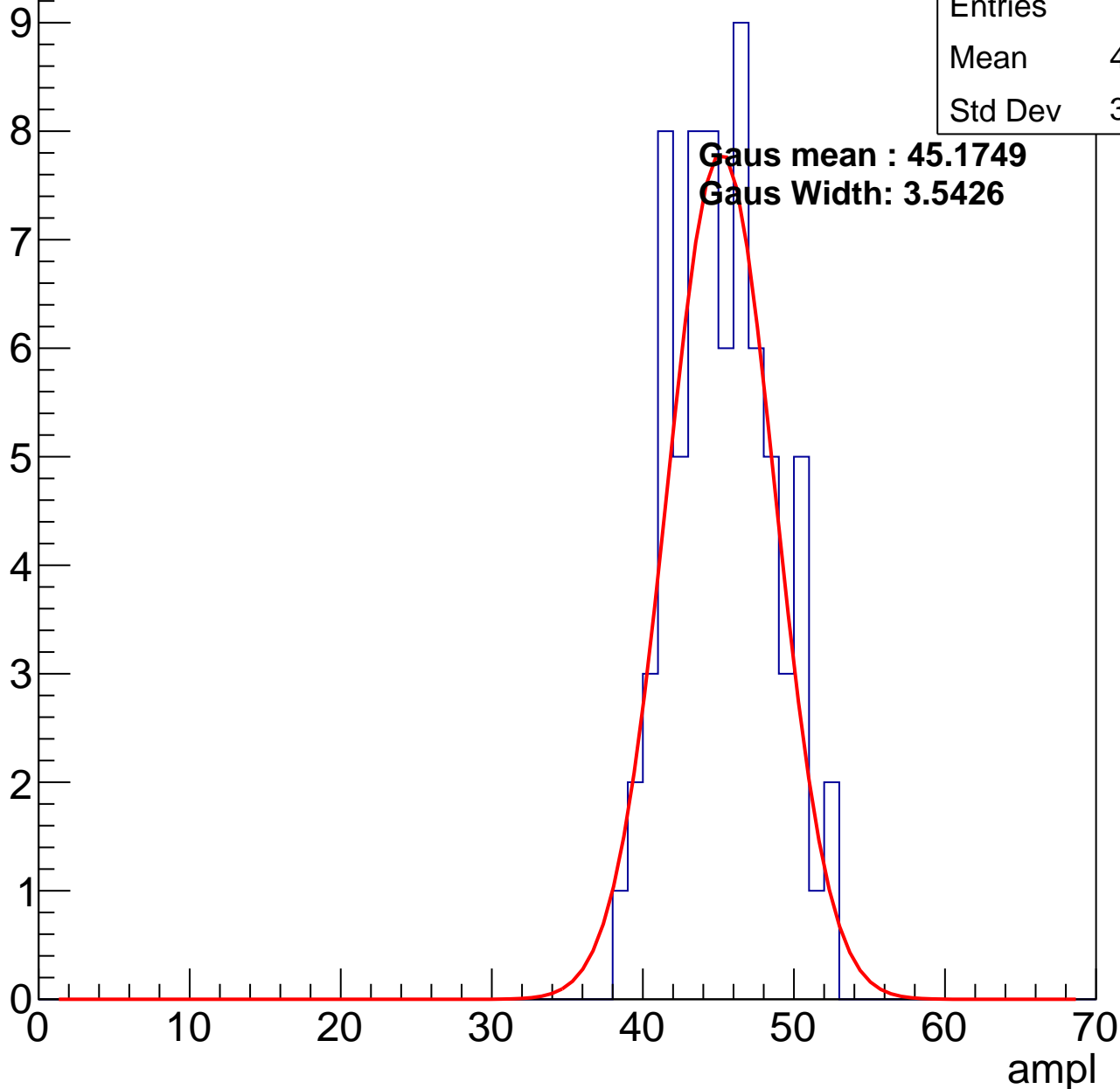
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	44.83
Std Dev	3.317

**Gaus mean : 45.1749**

**Gaus Width: 3.5426**

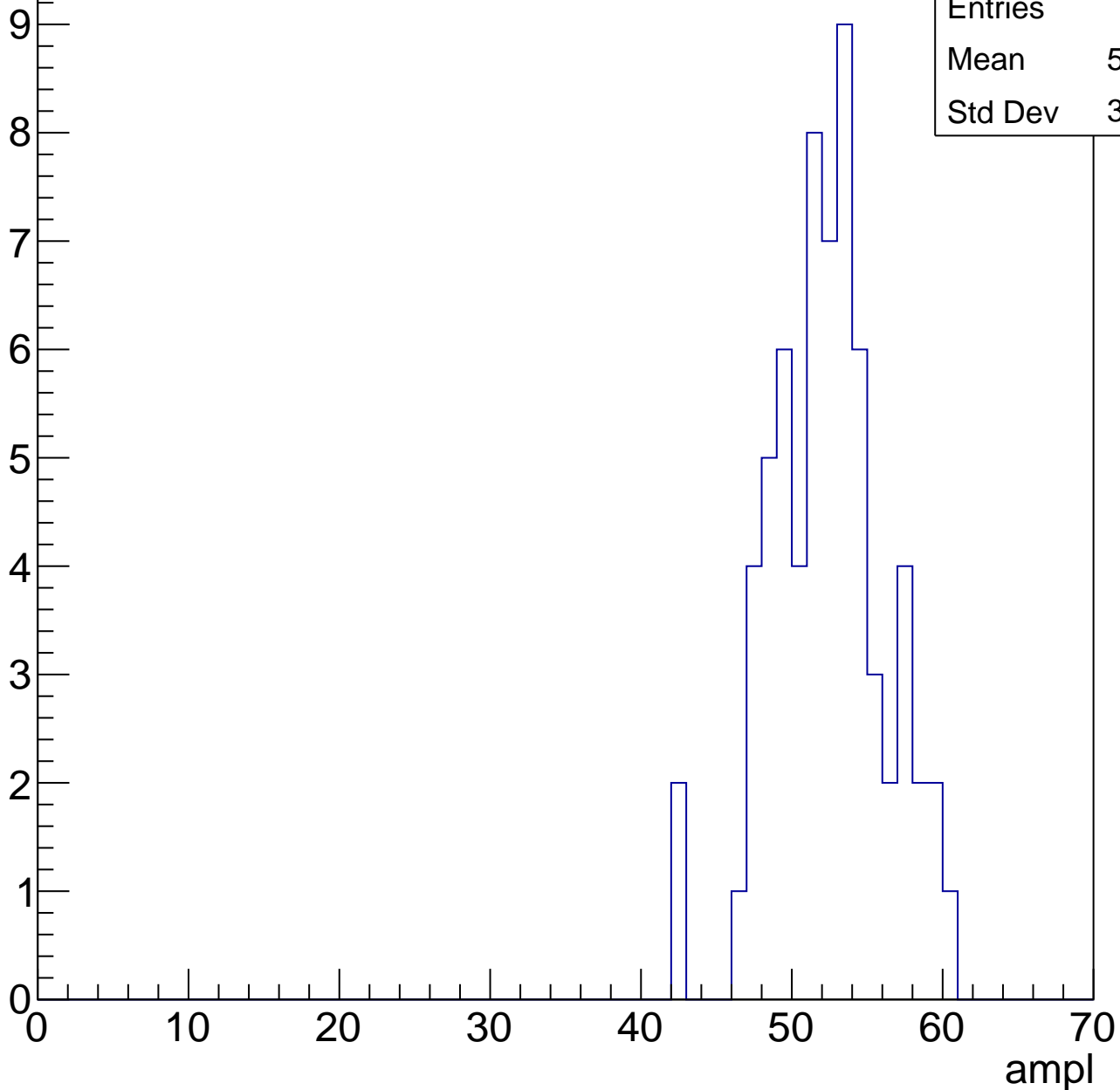


# B0L001S, U17-ch21, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

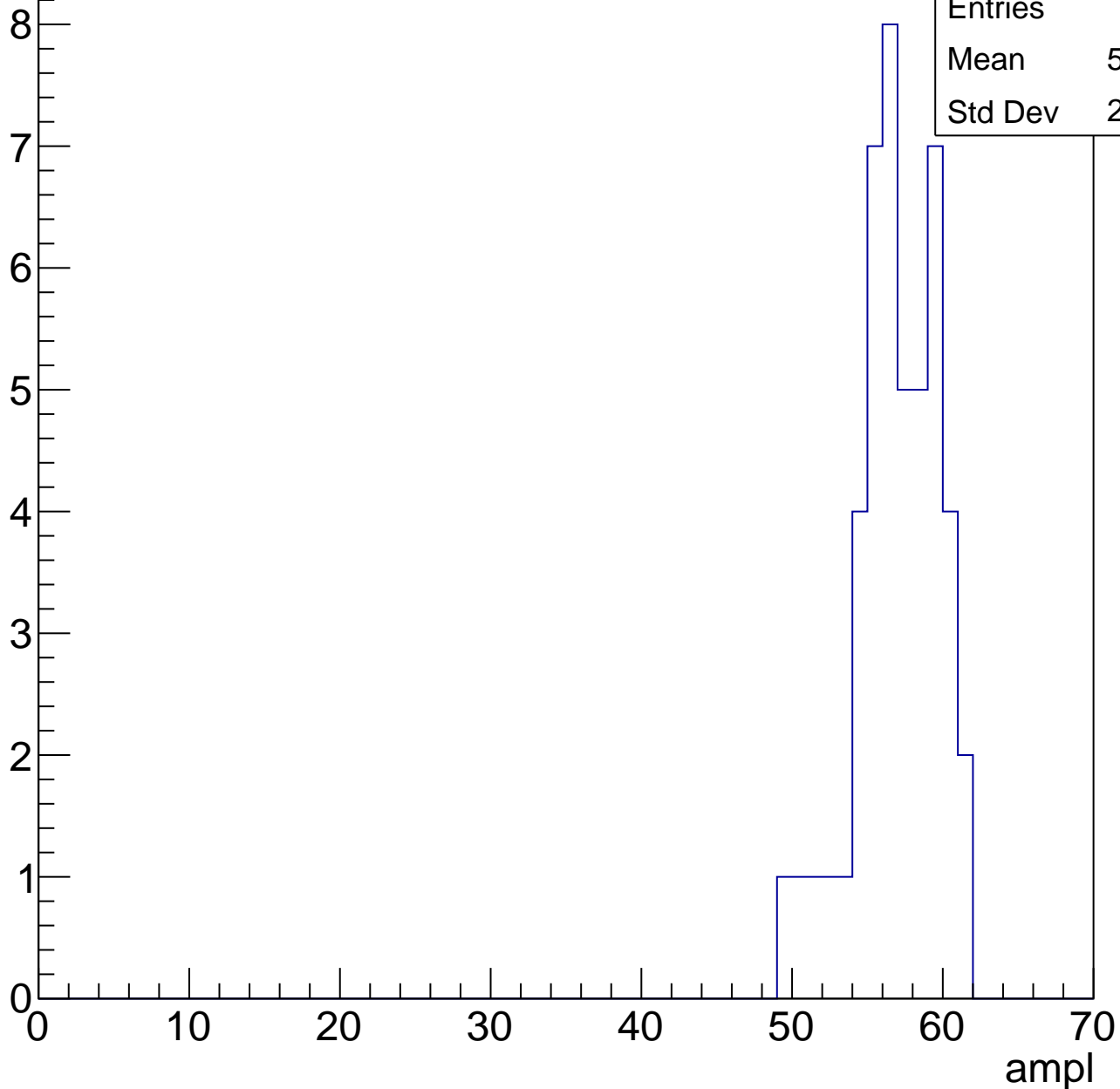
Entries	66
Mean	51.88
Std Dev	3.732



# B0L001S, U17-ch21, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

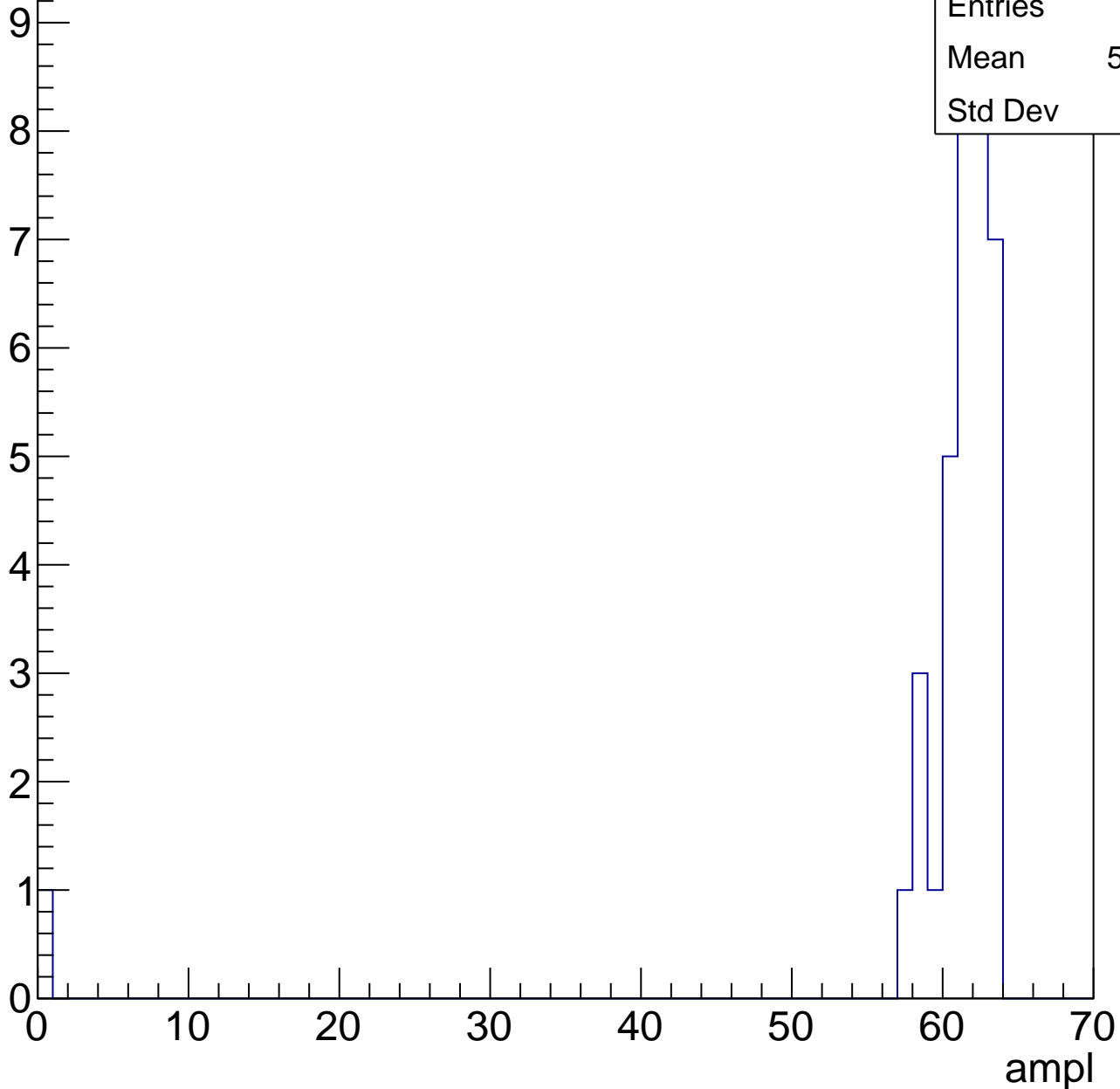


# B0L001S, U17-ch21, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	35
Mean	59.34
Std Dev	10.3



# B0L001S, U17-ch21, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch21, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	10
Std Dev	10

# B0L001S, U17-ch22, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	79
Mean	29.37
Std Dev	3.269

**Gaus mean : 30.1071**

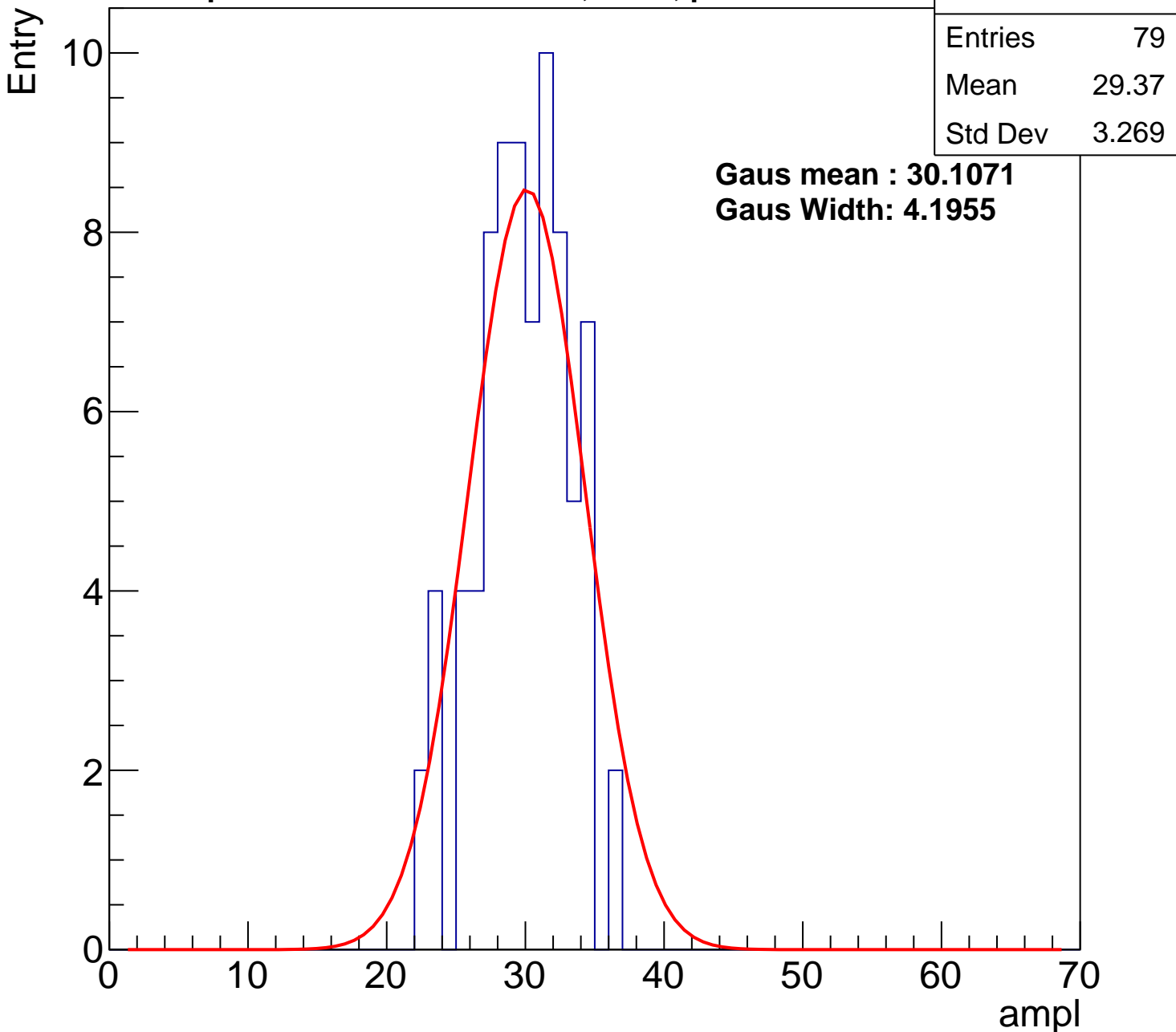
**Gaus Width: 4.1955**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U17-ch22, adc1

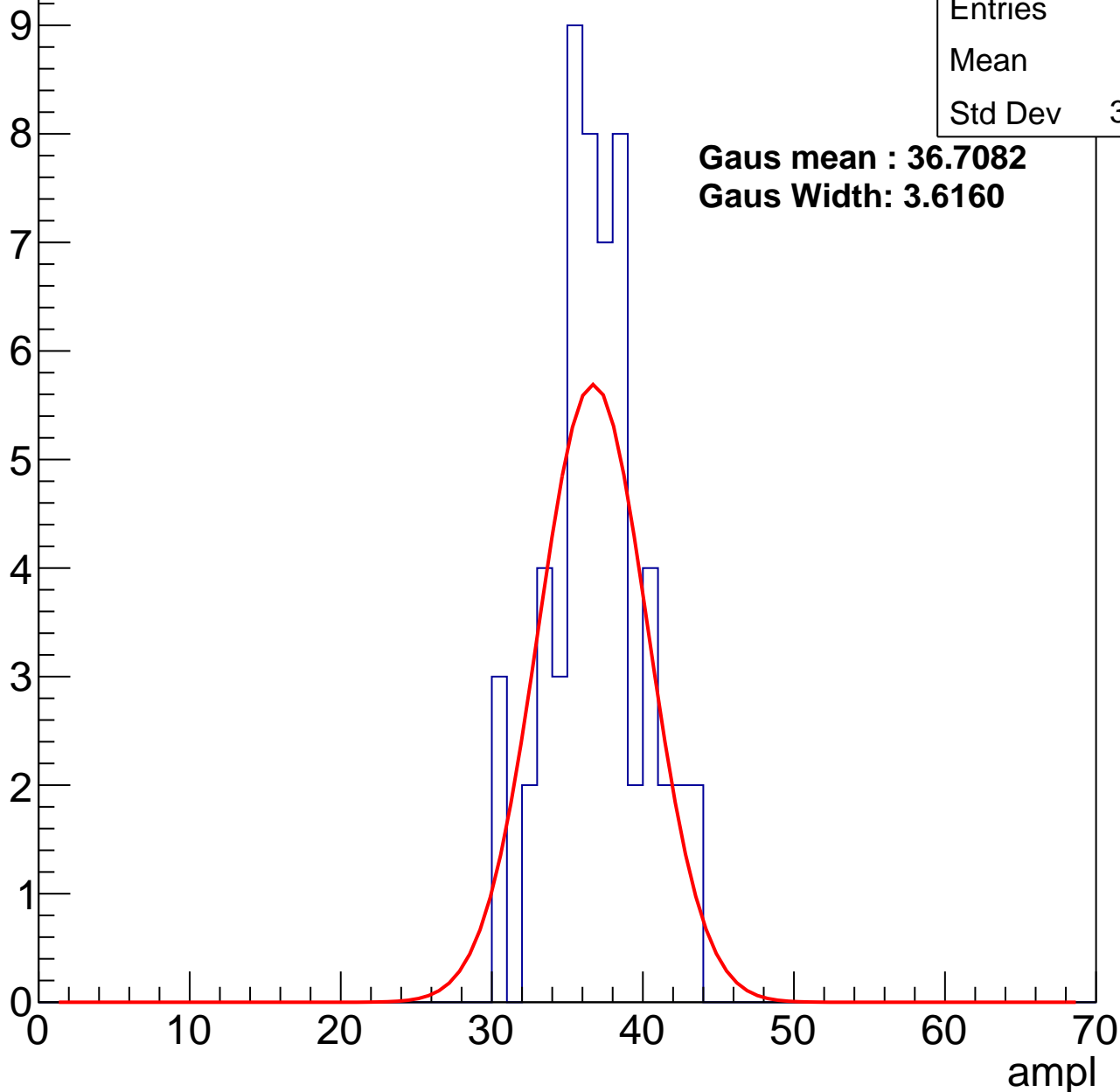
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	36.5
Std Dev	3.059

**Gaus mean : 36.7082**

**Gaus Width: 3.6160**



# B0L001S, U17-ch22, adc2

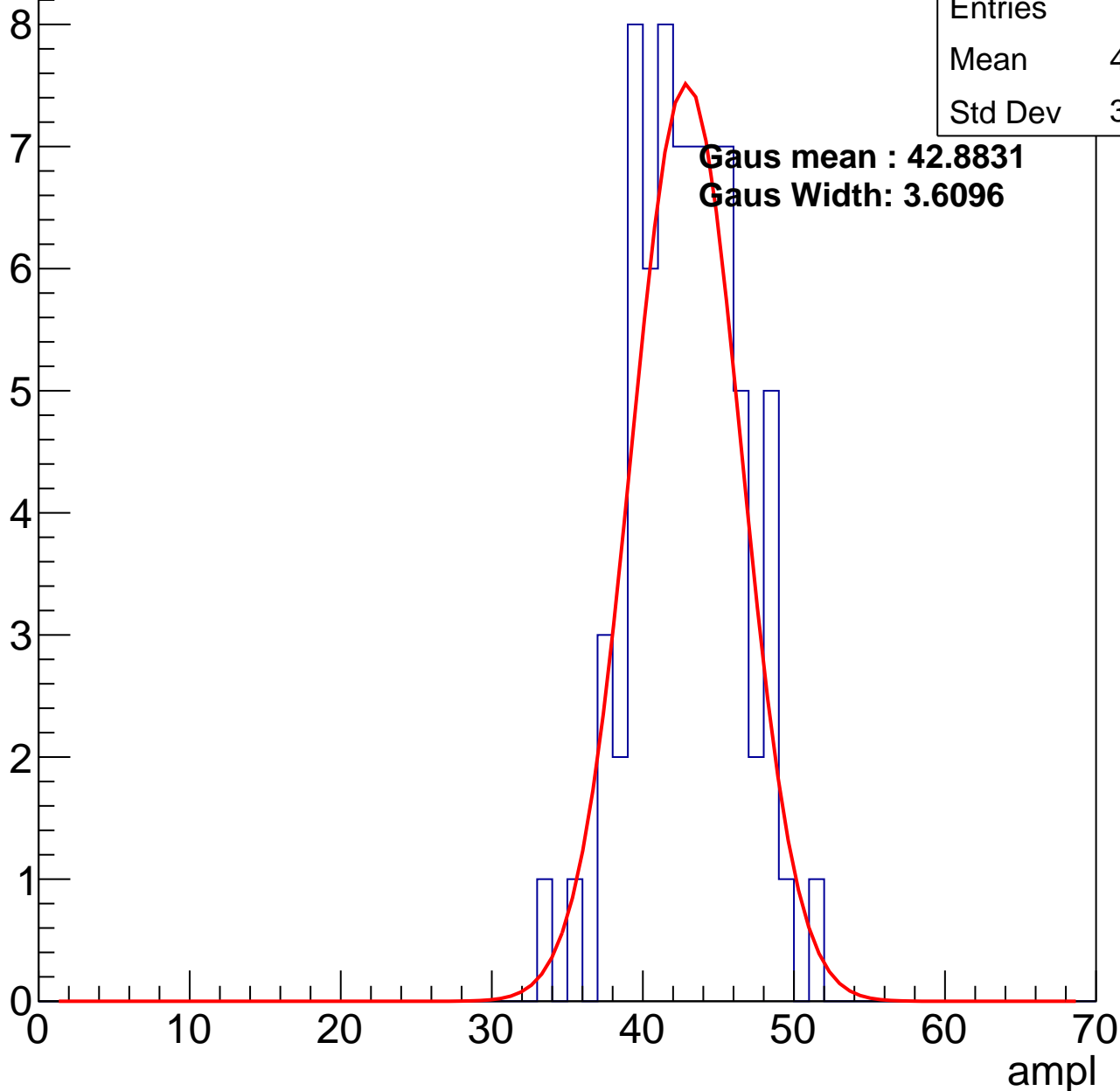
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	42.49
Std Dev	3.484

**Gaus mean : 42.8831**

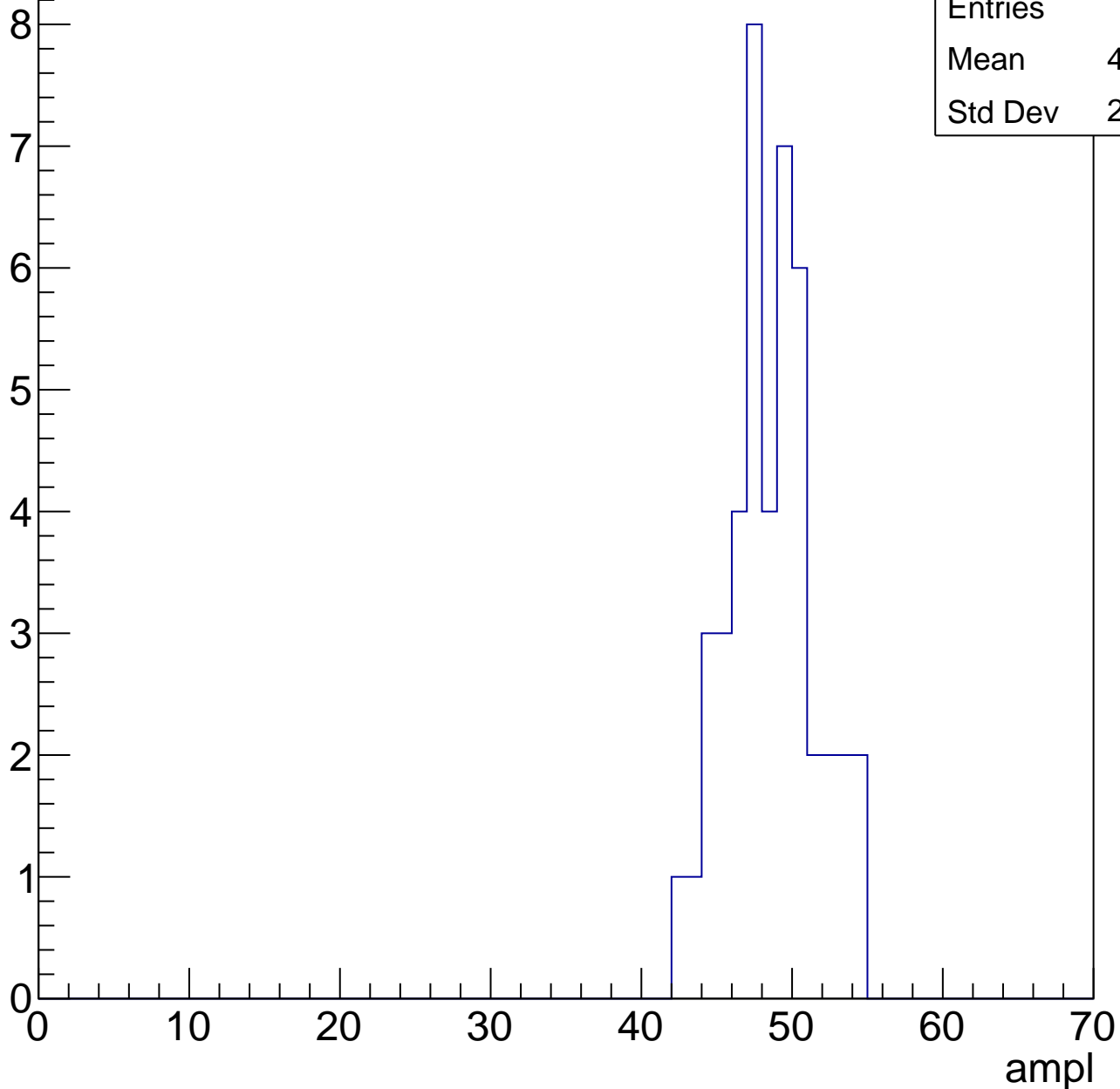
**Gaus Width: 3.6096**



# B0L001S, U17-ch22, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



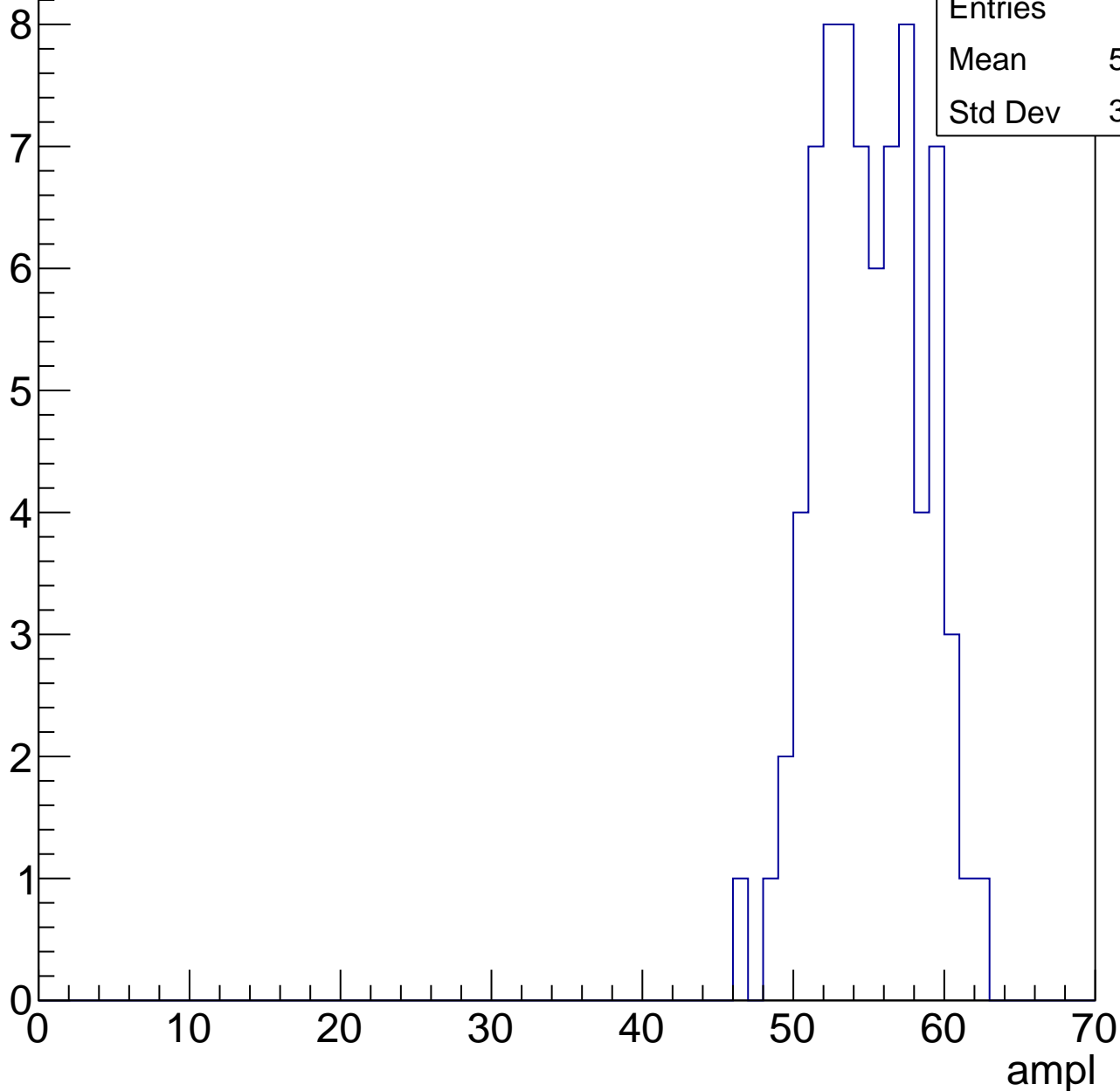
Entries	45
Mean	48.16
Std Dev	2.836

# B0L001S, U17-ch22, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	75
Mean	54.57
Std Dev	3.383

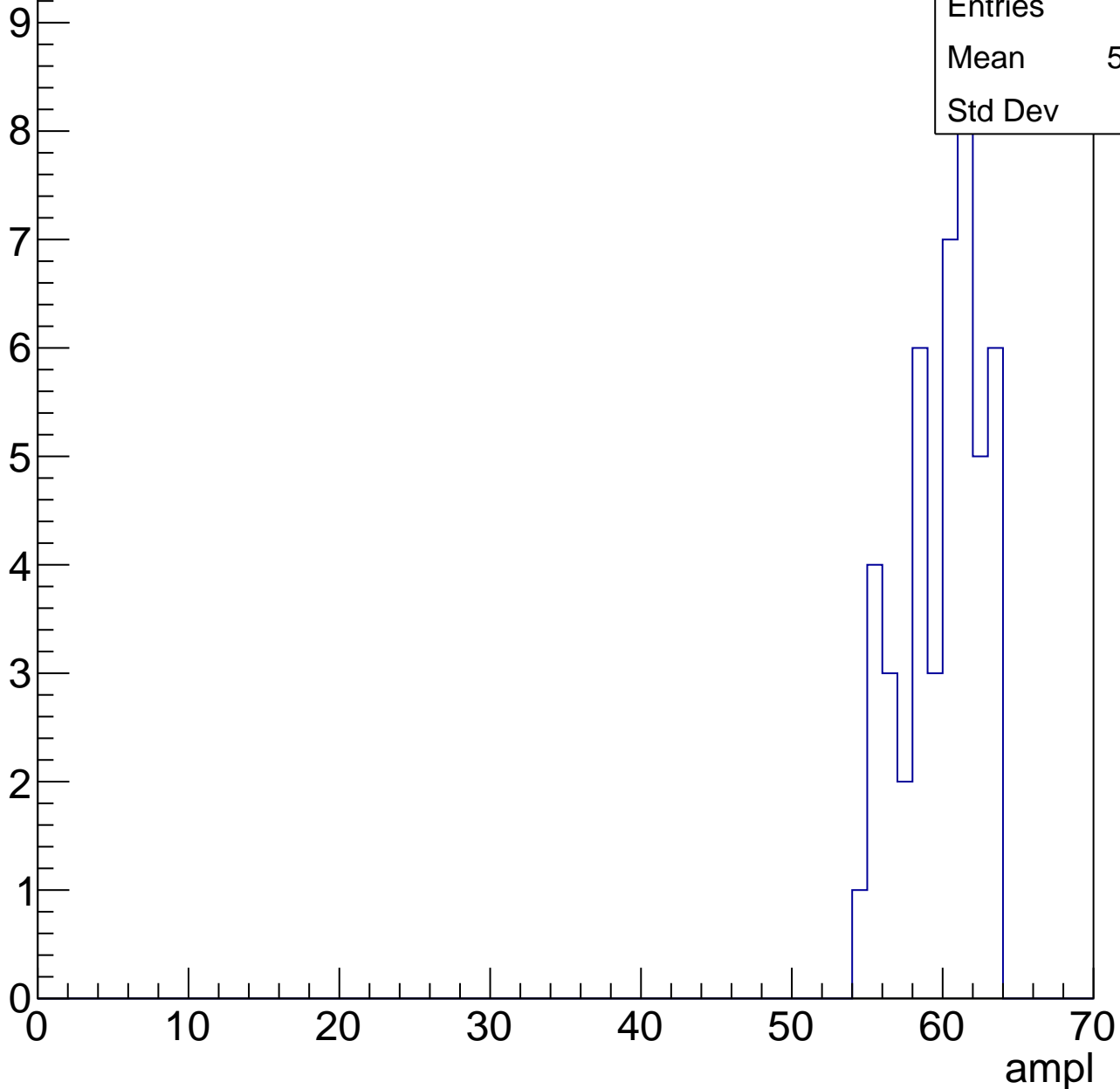


# B0L001S, U17-ch22, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

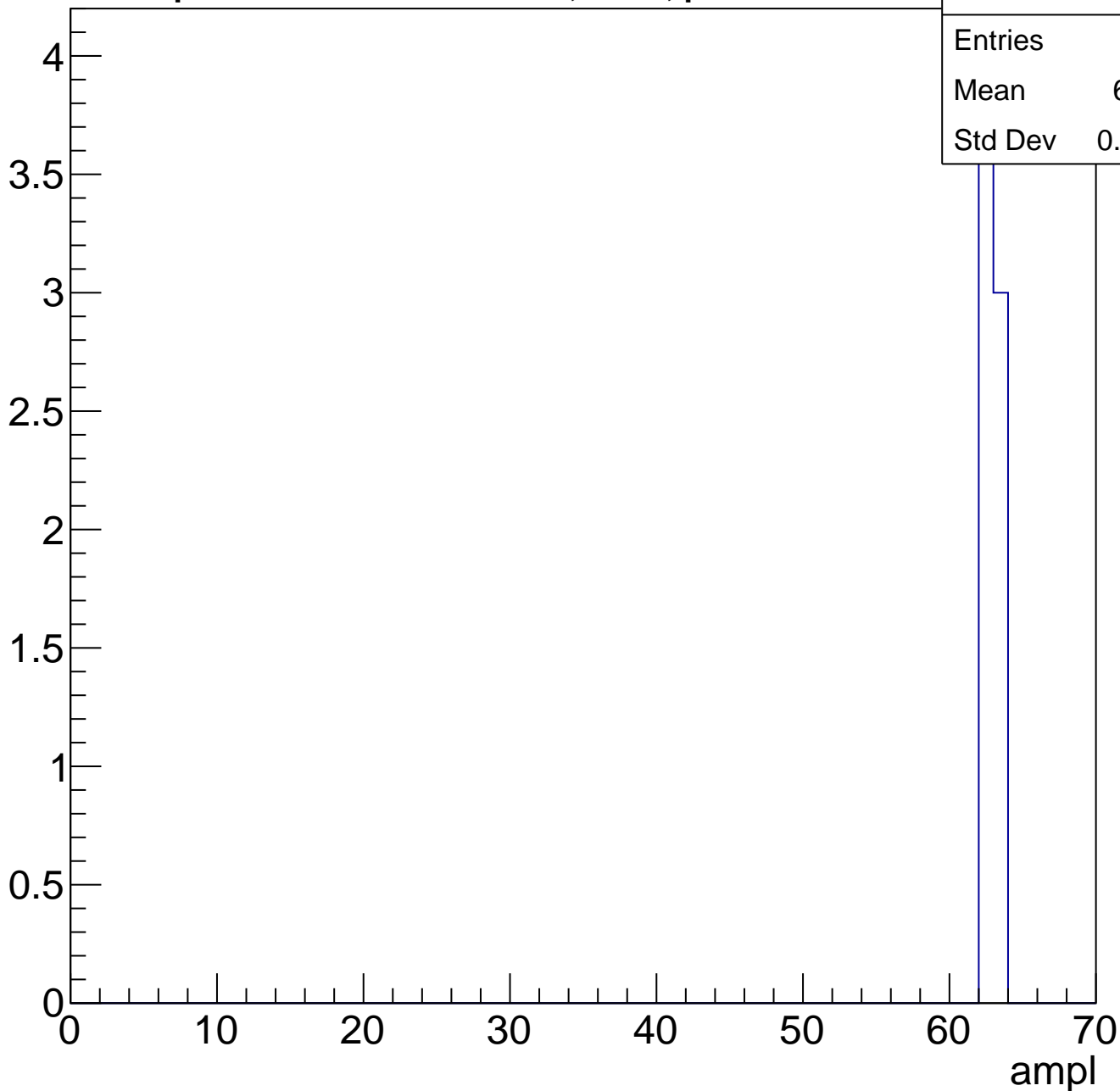
Entries	46
Mean	59.52
Std Dev	2.56



# B0L001S, U17-ch22, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

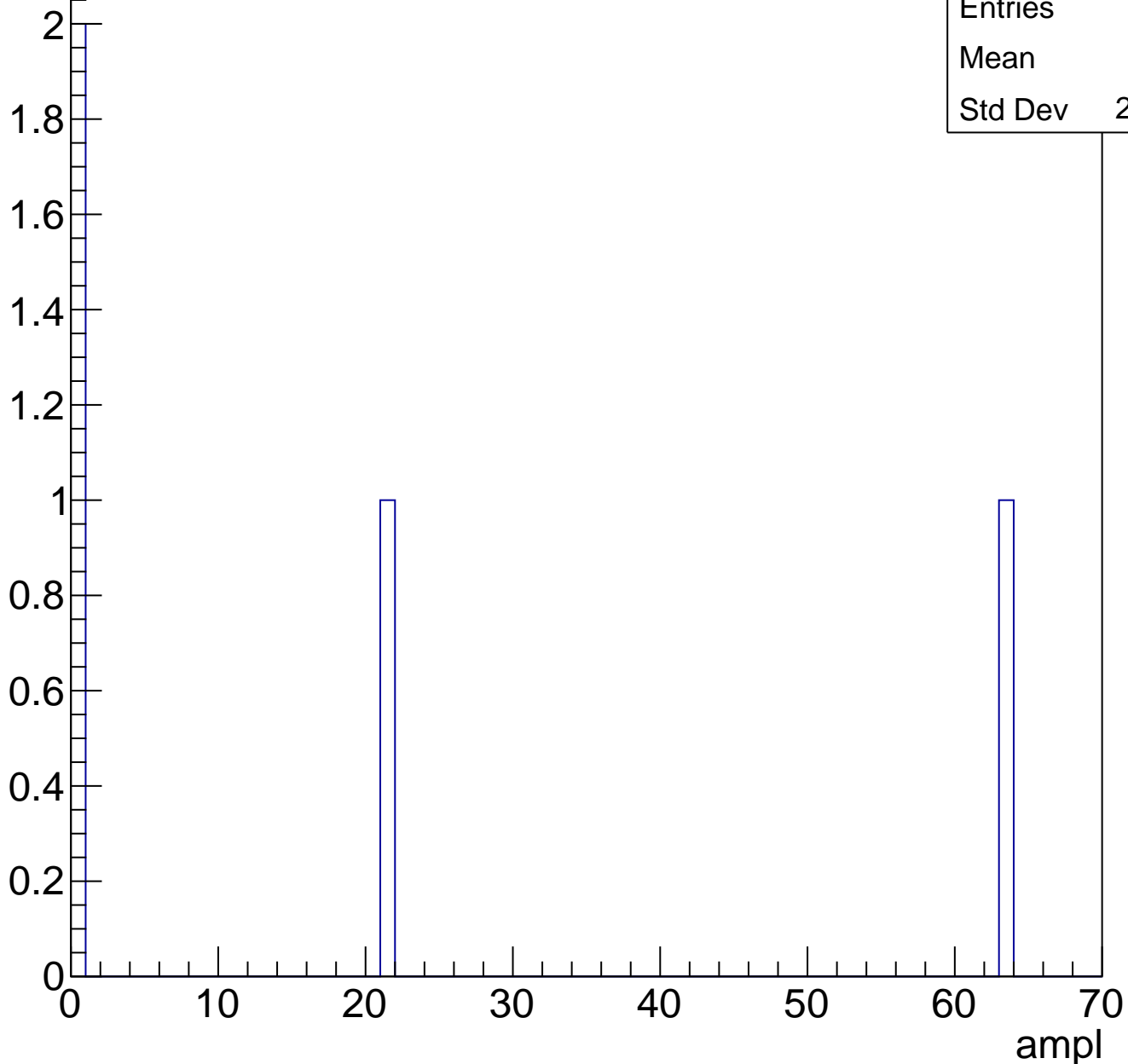




# B0L001S, U17-ch22, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	4
Mean	21
Std Dev	25.72

# B0L001S, U17-ch23, adc0

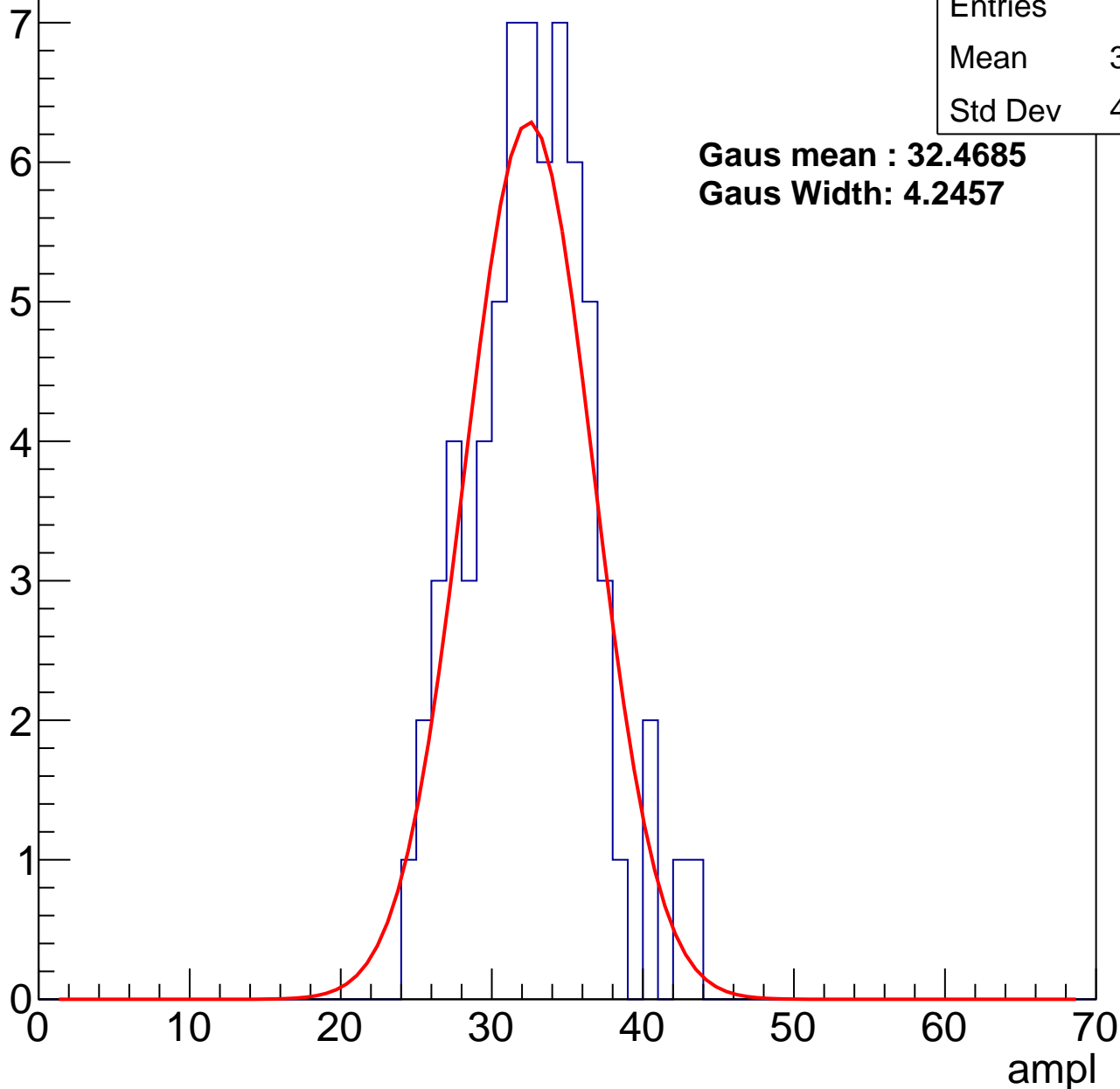
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	32.22
Std Dev	4.032

**Gaus mean : 32.4685**

**Gaus Width: 4.2457**



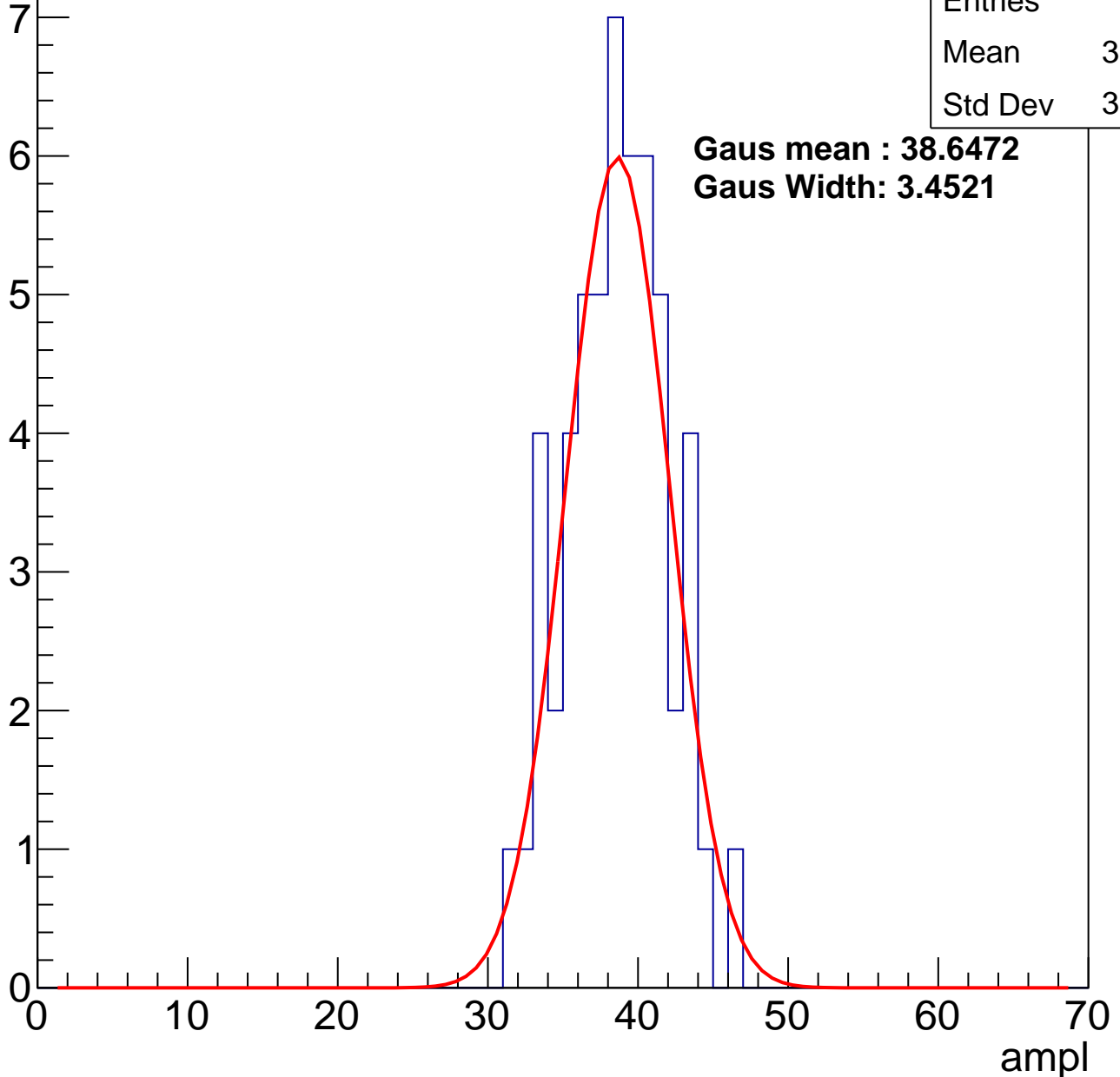
# B0L001S, U17-ch23, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	38.13
Std Dev	3.289

**Gaus mean : 38.6472**  
**Gaus Width: 3.4521**



# B0L001S, U17-ch23, adc2

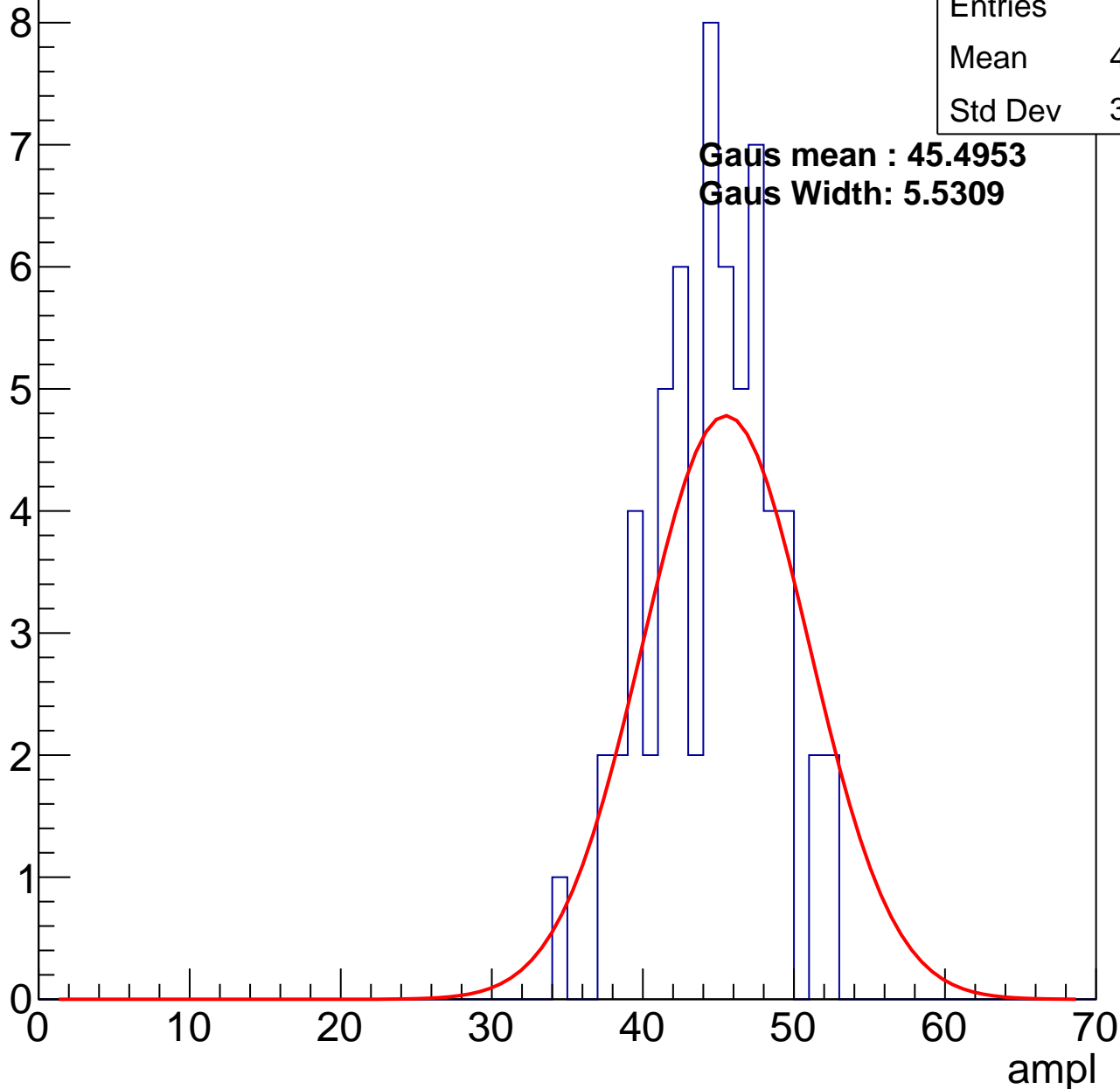
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	44.16
Std Dev	3.915

**Gaus mean : 45.4953**

**Gaus Width: 5.5309**

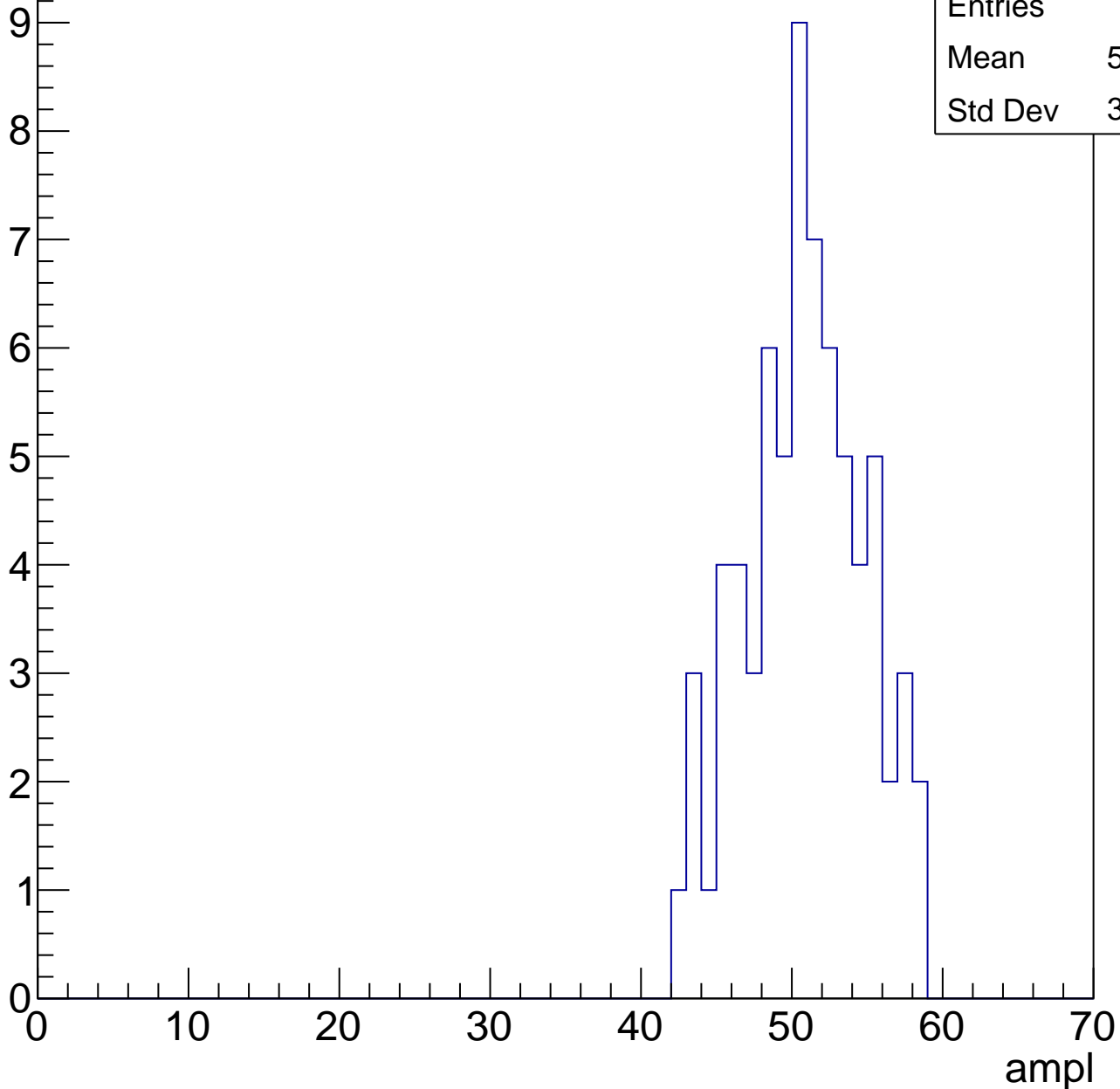


# B0L001S, U17-ch23, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

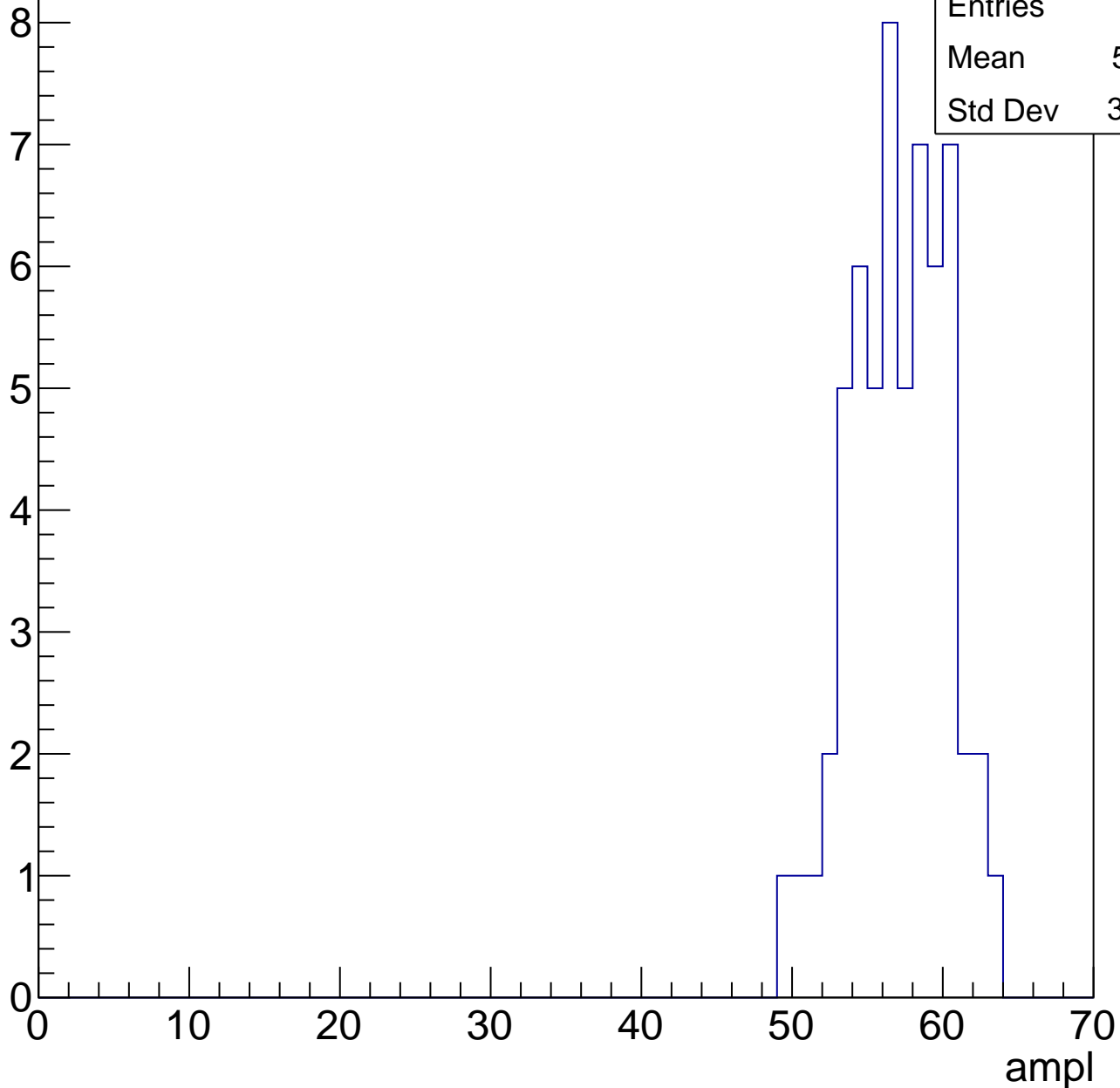
Entries	70
Mean	50.39
Std Dev	3.907



# B0L001S, U17-ch23, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



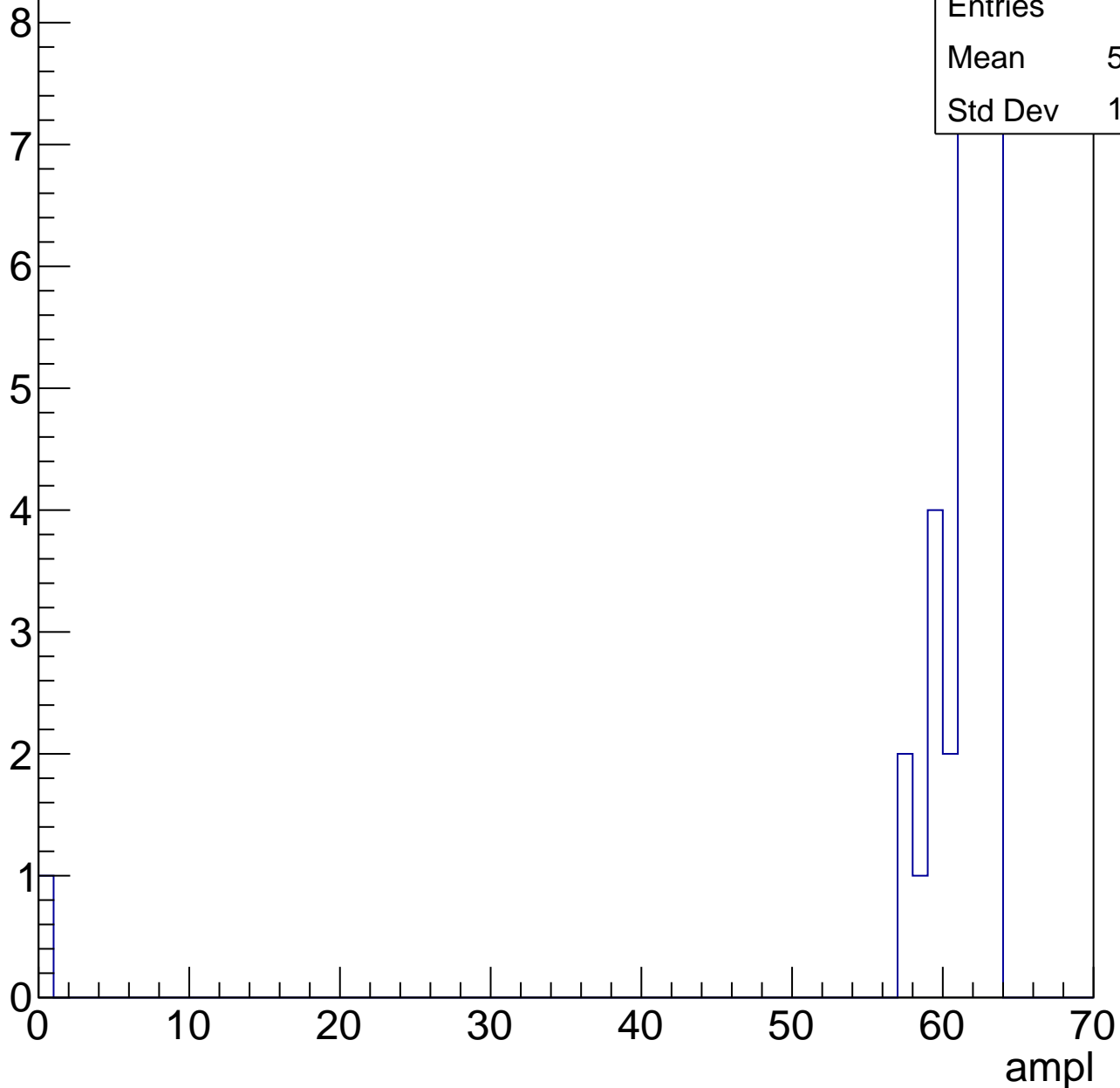
Entries	59
Mean	56.61
Std Dev	3.092

# B0L001S, U17-ch23, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	34
Mean	59.29
Std Dev	10.46



# B0L001S, U17-ch23, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch23, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U17-ch24, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	67
Mean	30.61
Std Dev	3.407

**Gaus mean : 30.8453**

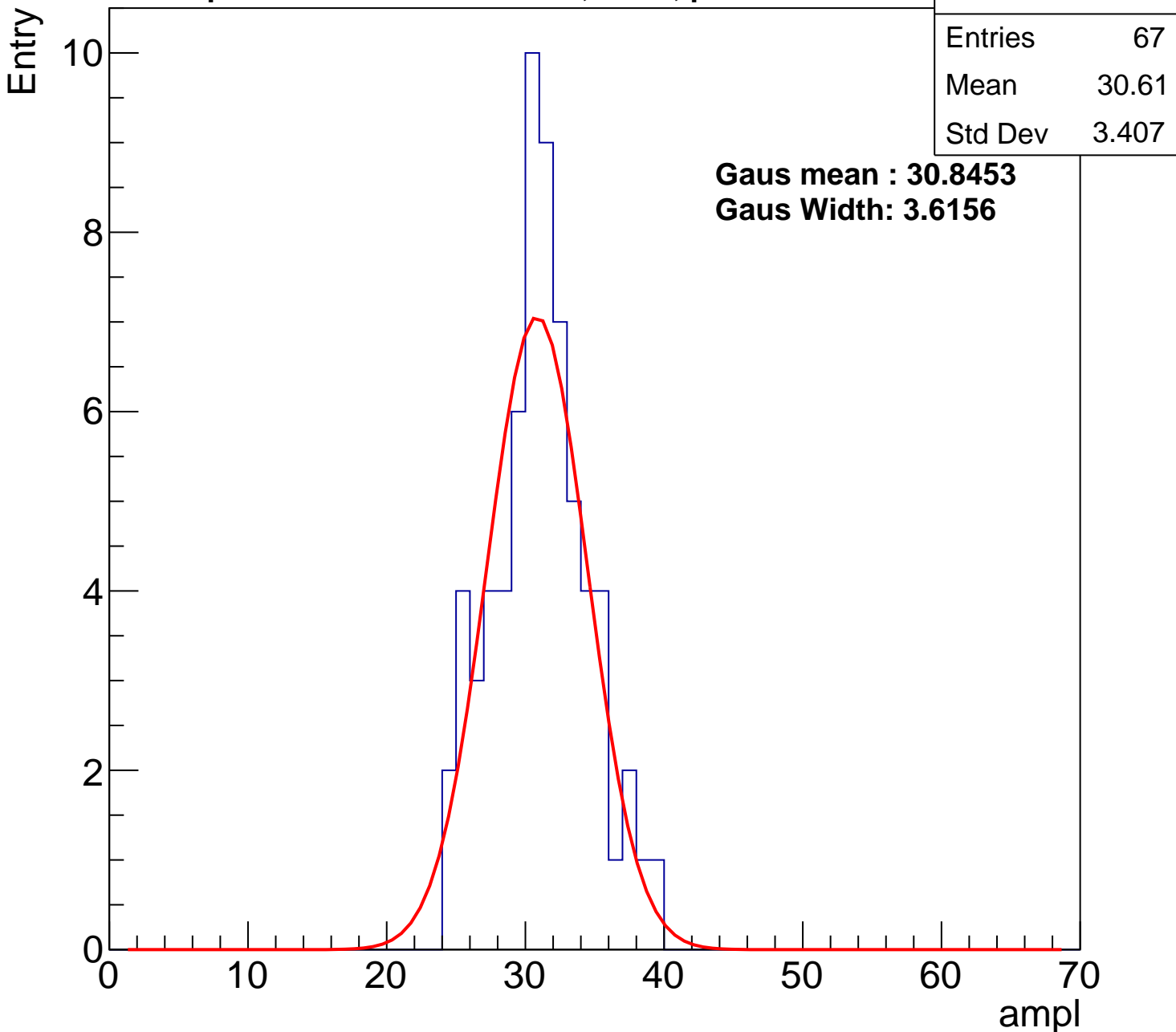
**Gaus Width: 3.6156**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U17-ch24, adc1

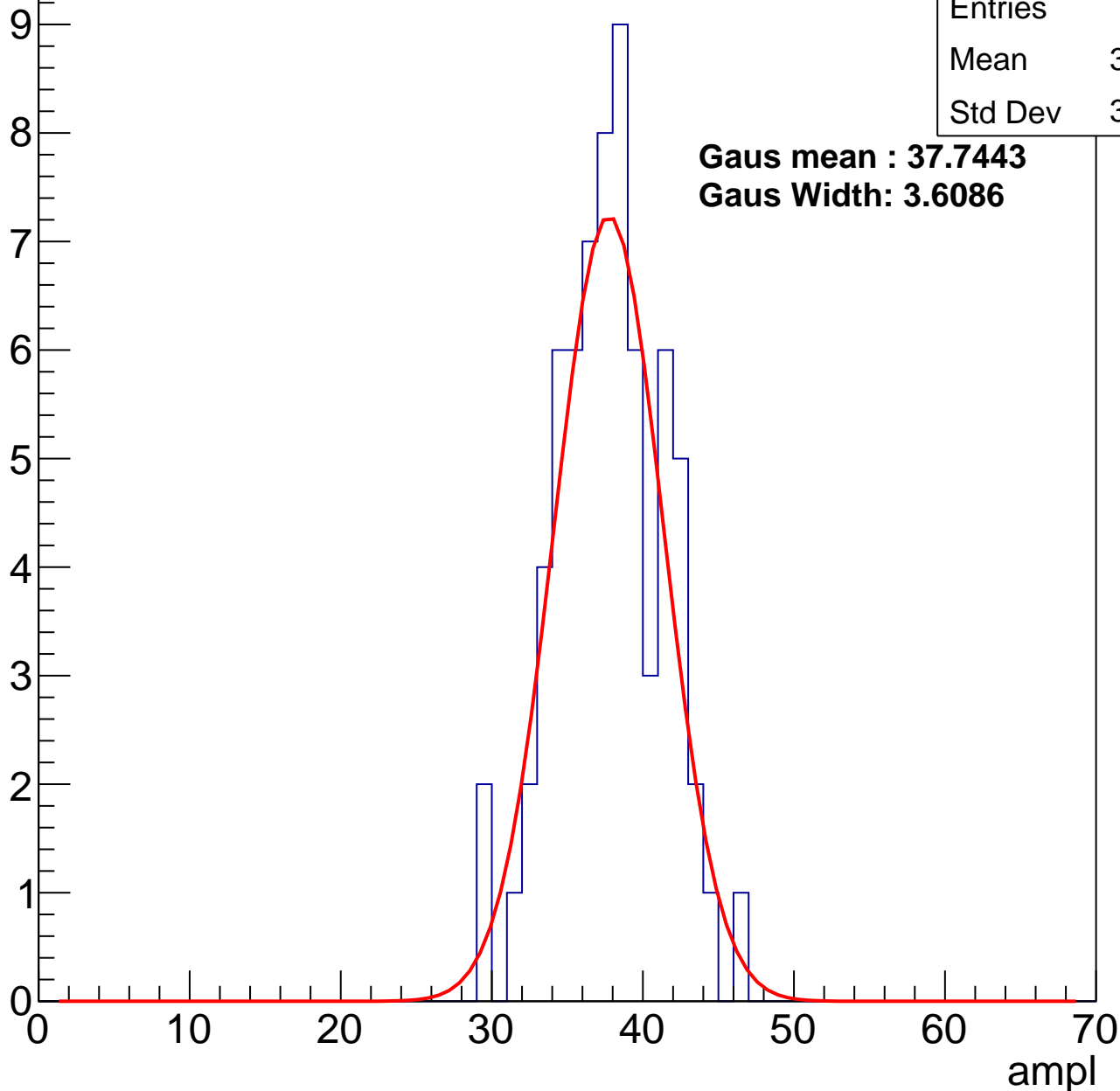
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	37.32
Std Dev	3.487

**Gaus mean : 37.7443**

**Gaus Width: 3.6086**



# B0L001S, U17-ch24, adc2

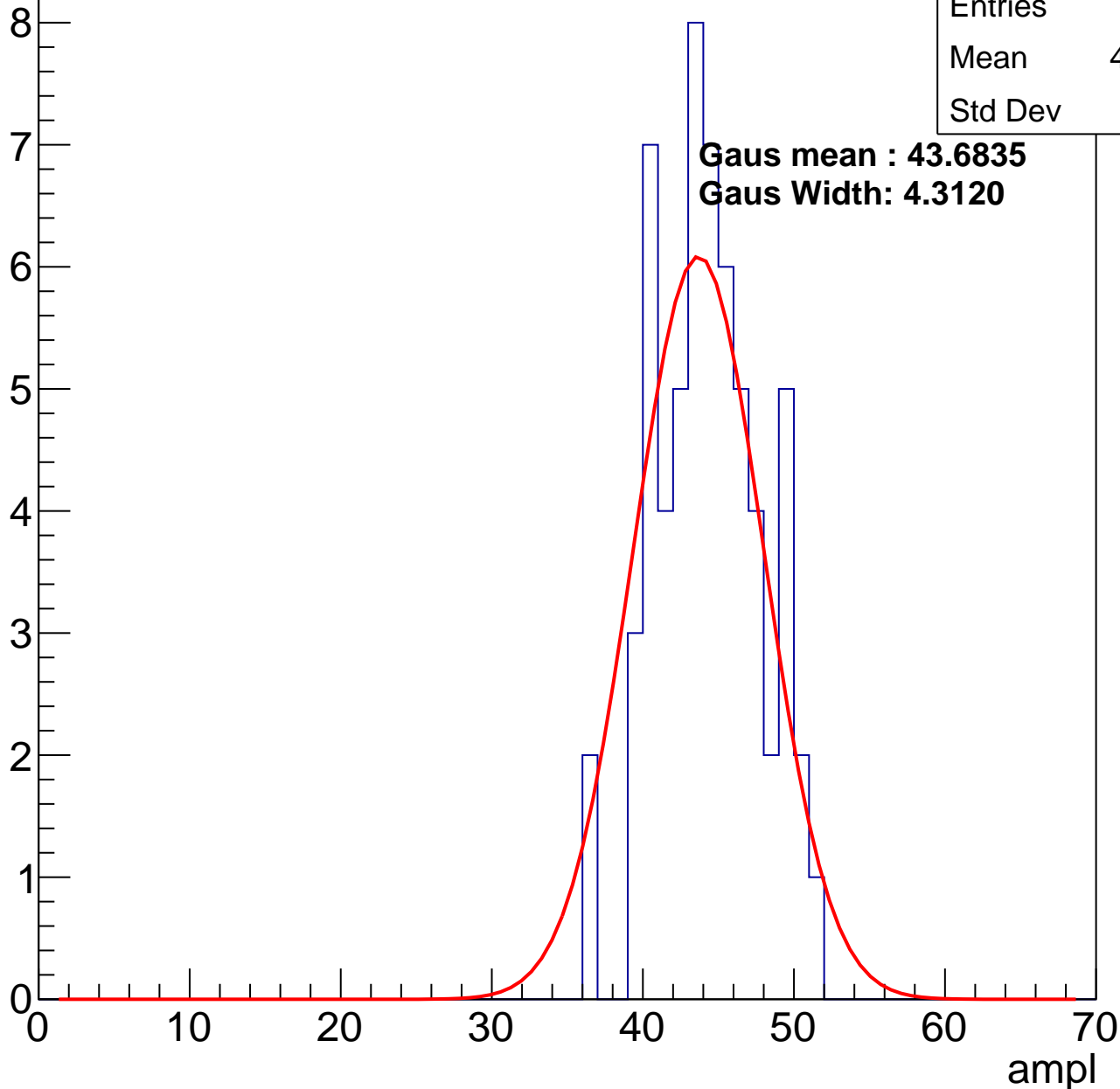
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	43.85
Std Dev	3.43

**Gaus mean : 43.6835**

**Gaus Width: 4.3120**

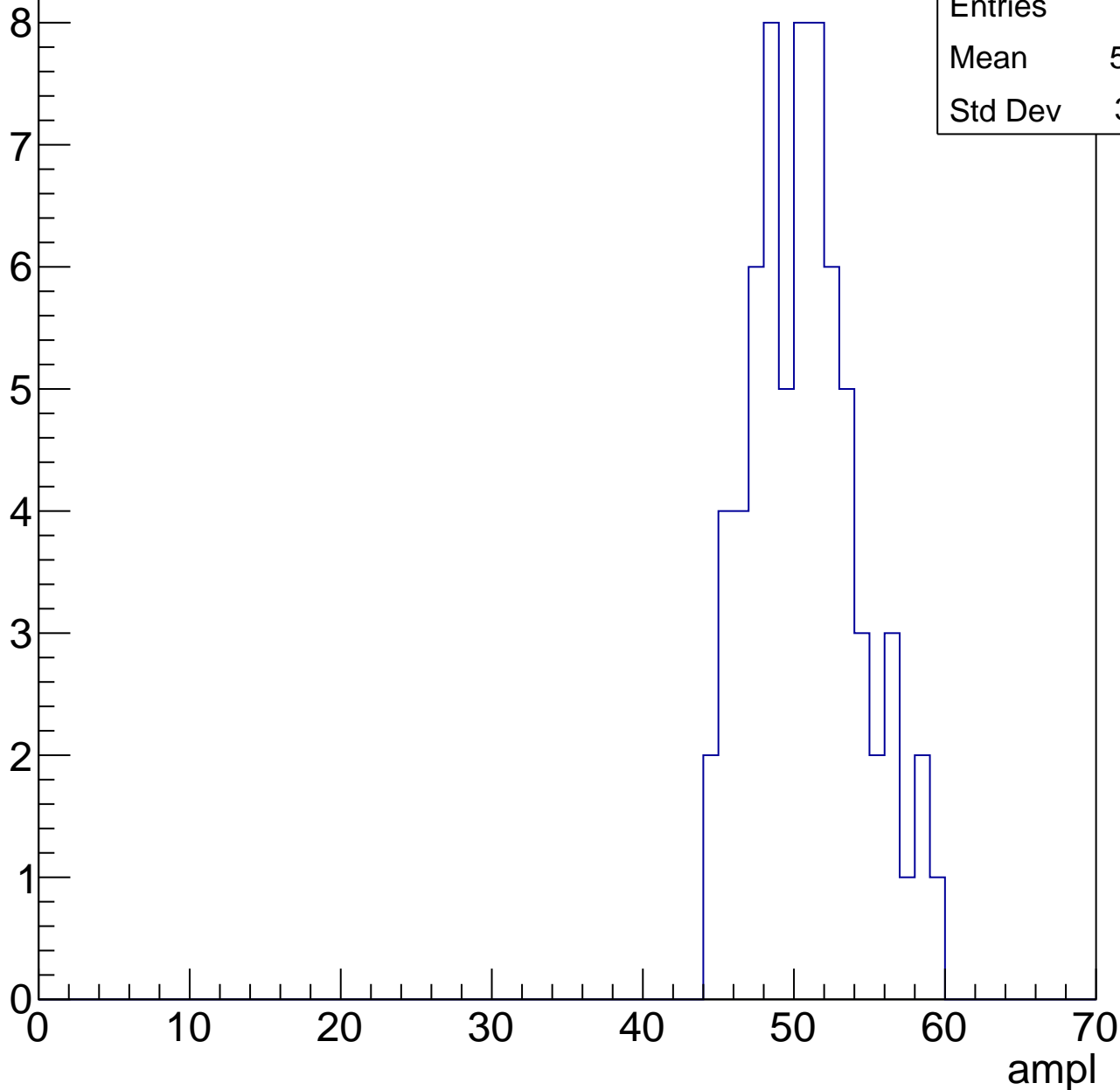


# B0L001S, U17-ch24, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

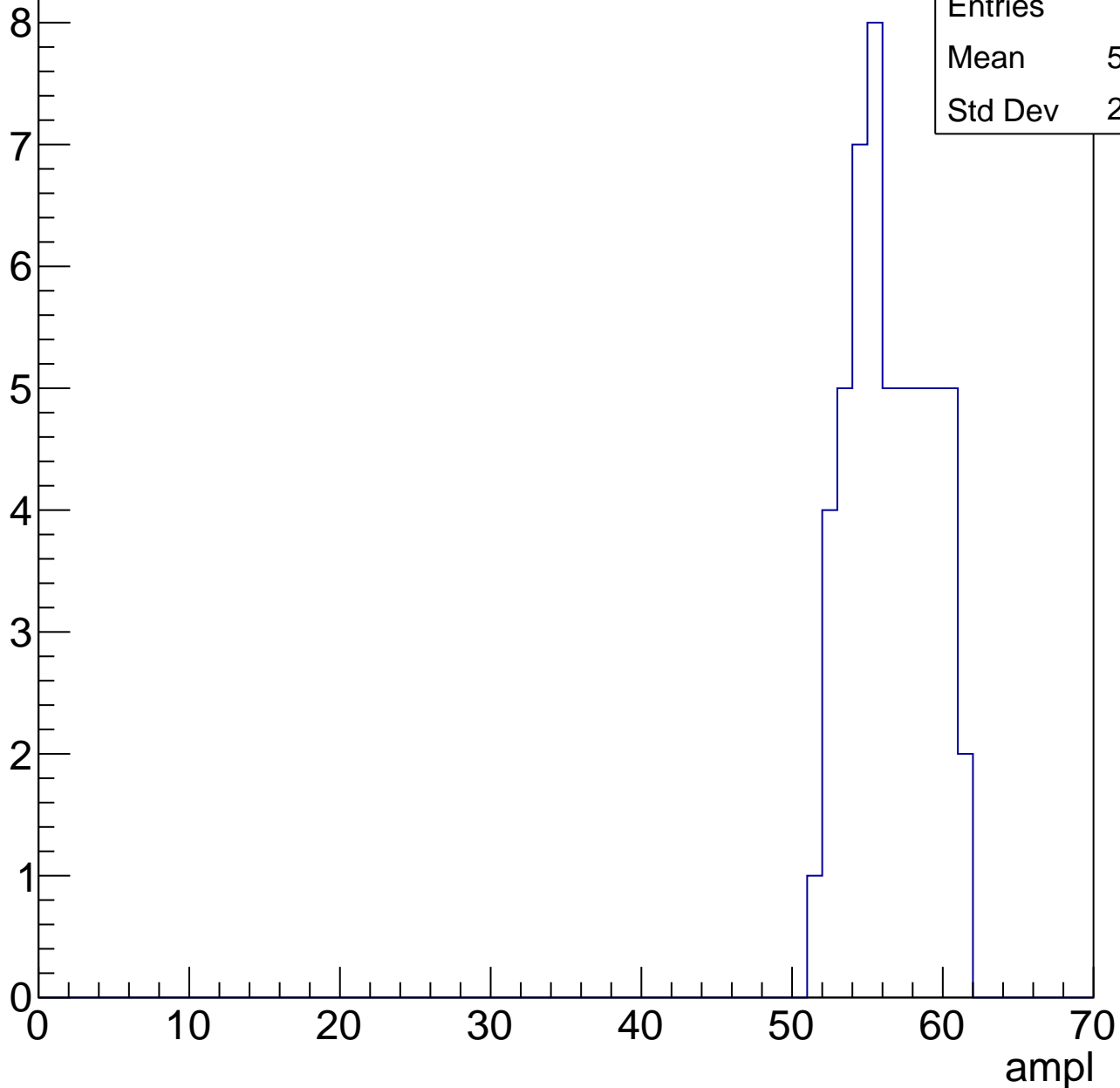
Entries	68
Mean	50.29
Std Dev	3.561



# B0L001S, U17-ch24, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



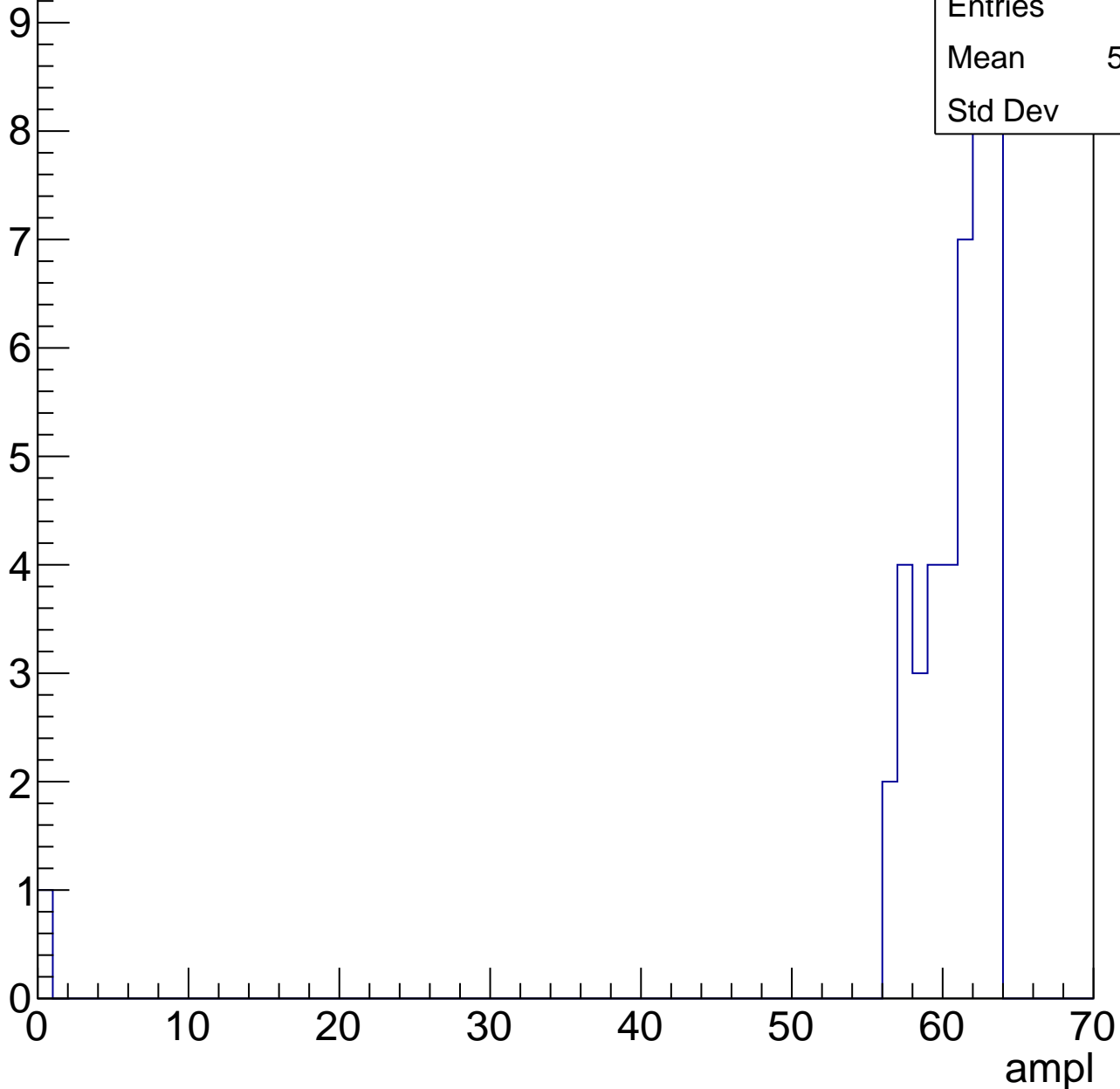
Entries	52
Mean	56.04
Std Dev	2.667

# B0L001S, U17-ch24, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	42
Mean	59.02
Std Dev	9.46



# B0L001S, U17-ch24, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

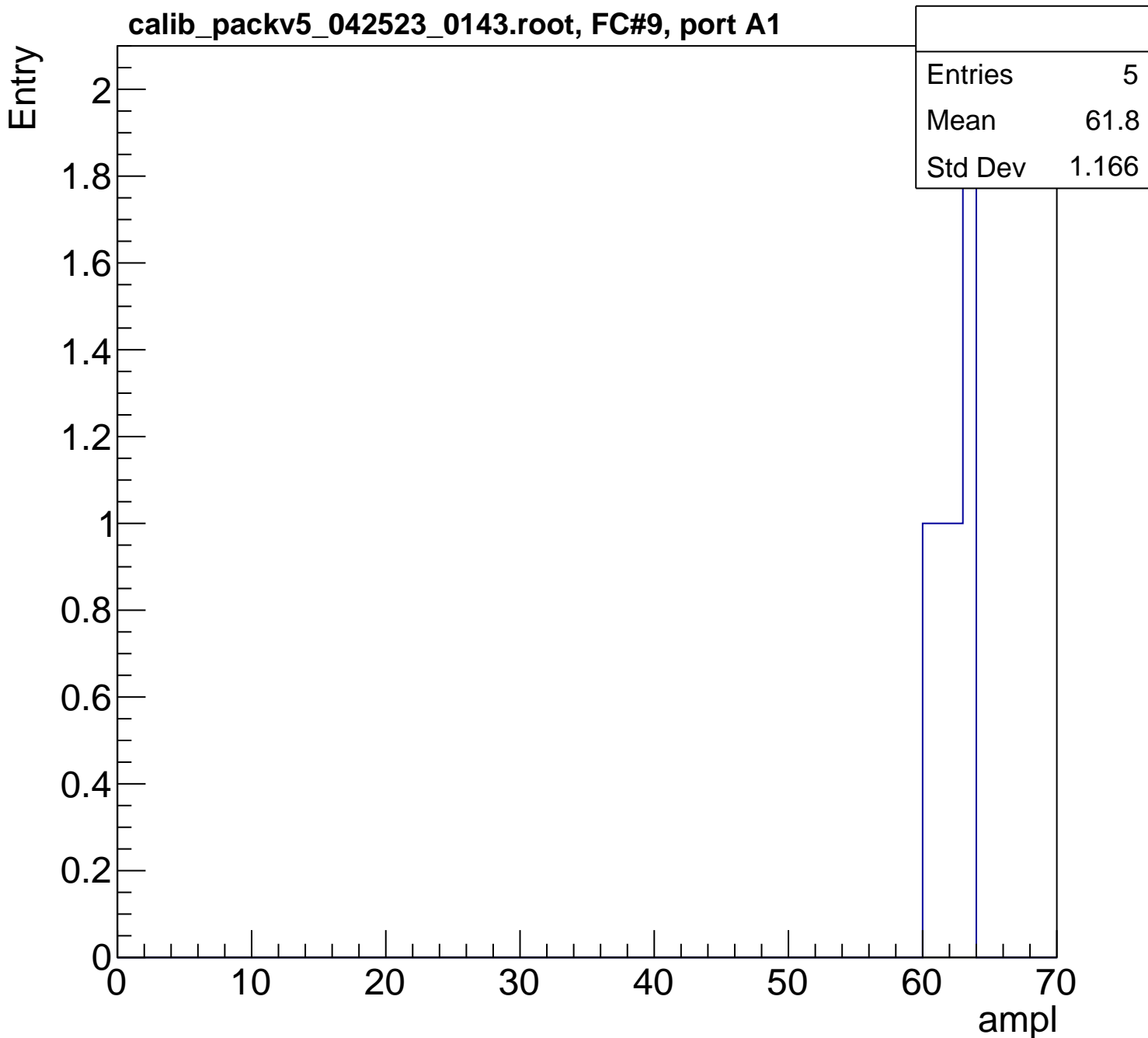
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	61.8
Std Dev	1.166

ampl

0 10 20 30 40 50 60 70





# B0L001S, U17-ch24, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U17-ch25, adc0

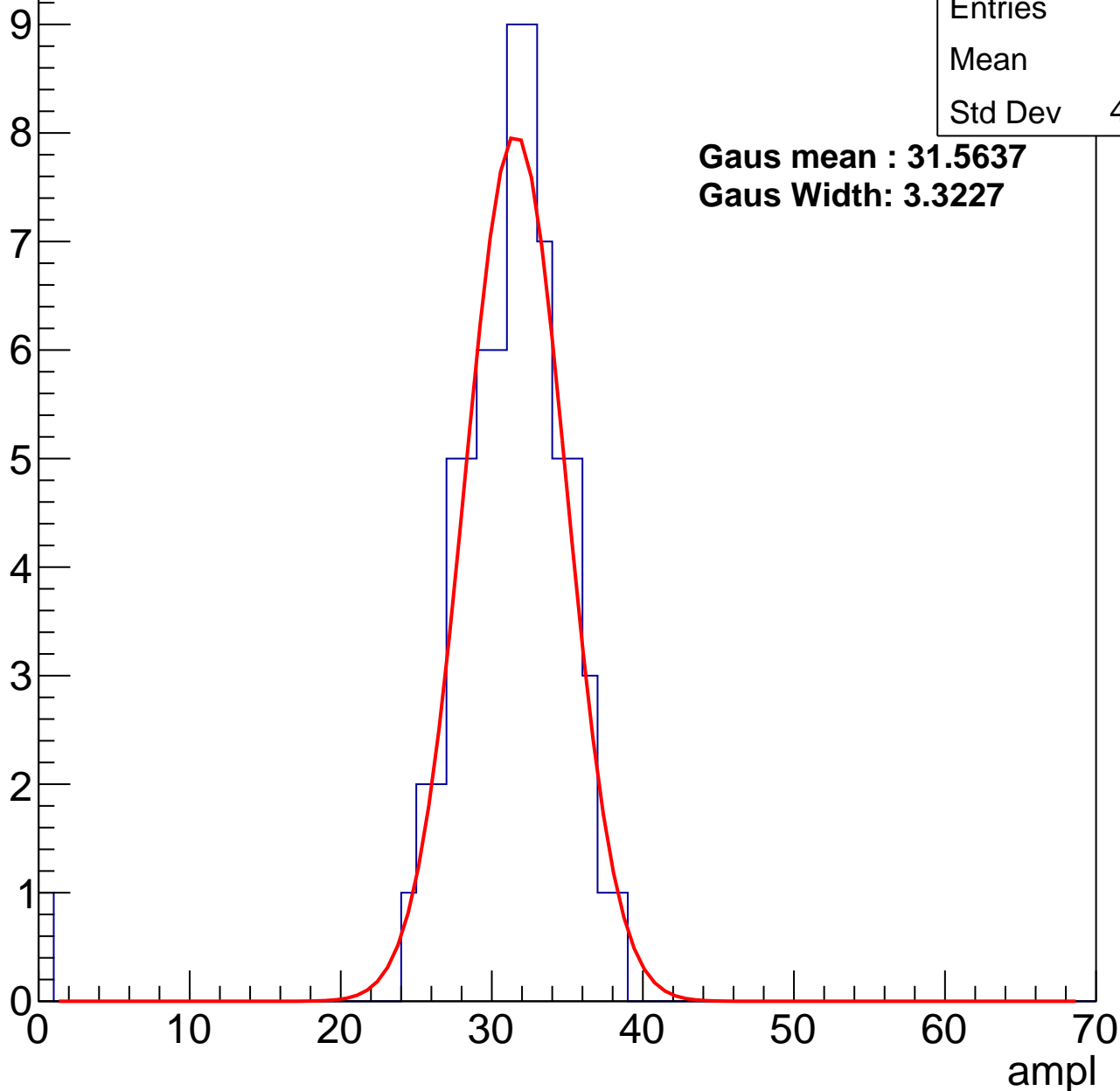
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	30.6
Std Dev	4.848

**Gaus mean : 31.5637**

**Gaus Width: 3.3227**



# B0L001S, U17-ch25, adc1

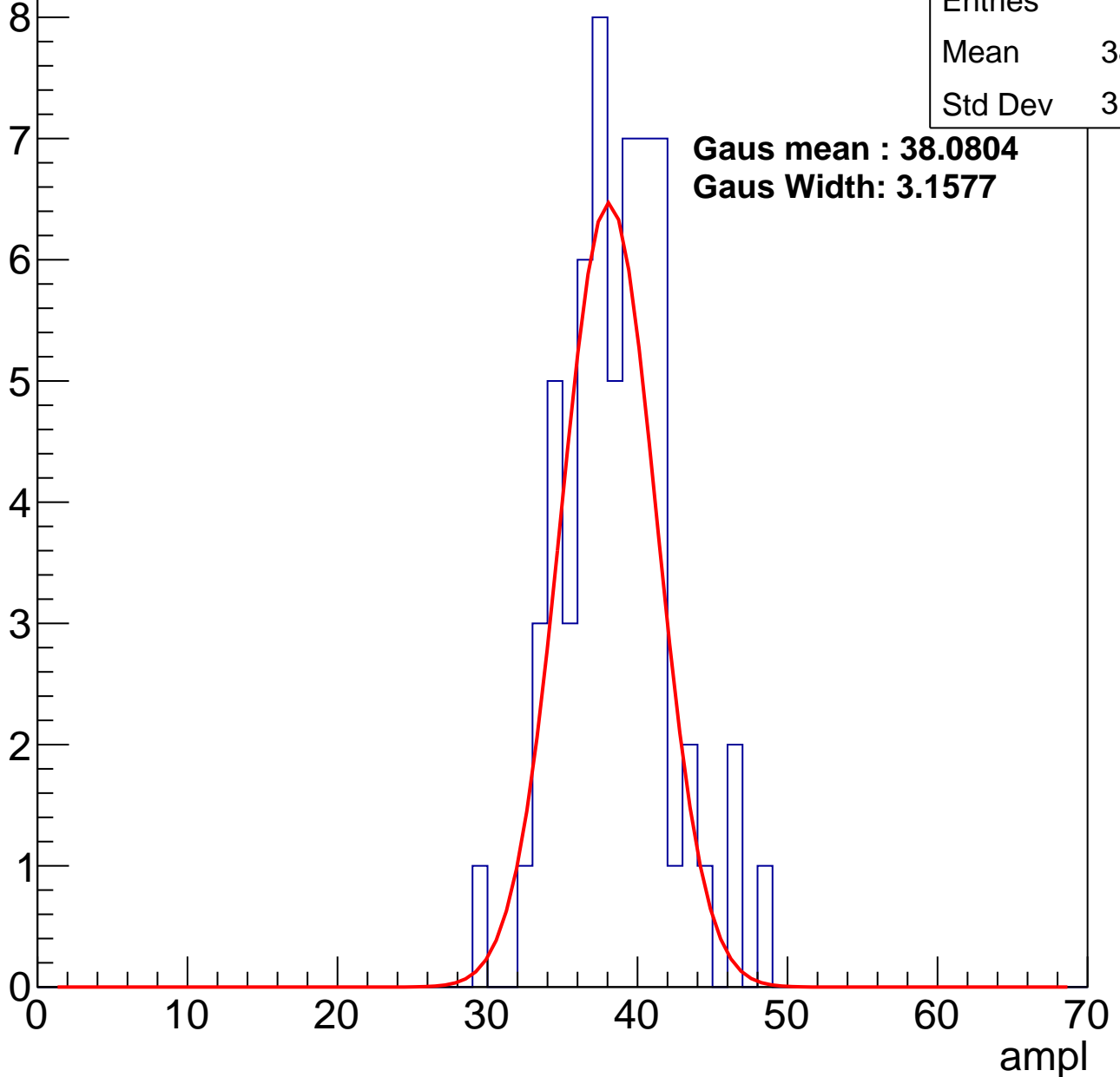
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	38.15
Std Dev	3.554

**Gaus mean : 38.0804**

**Gaus Width: 3.1577**



# B0L001S, U17-ch25, adc2

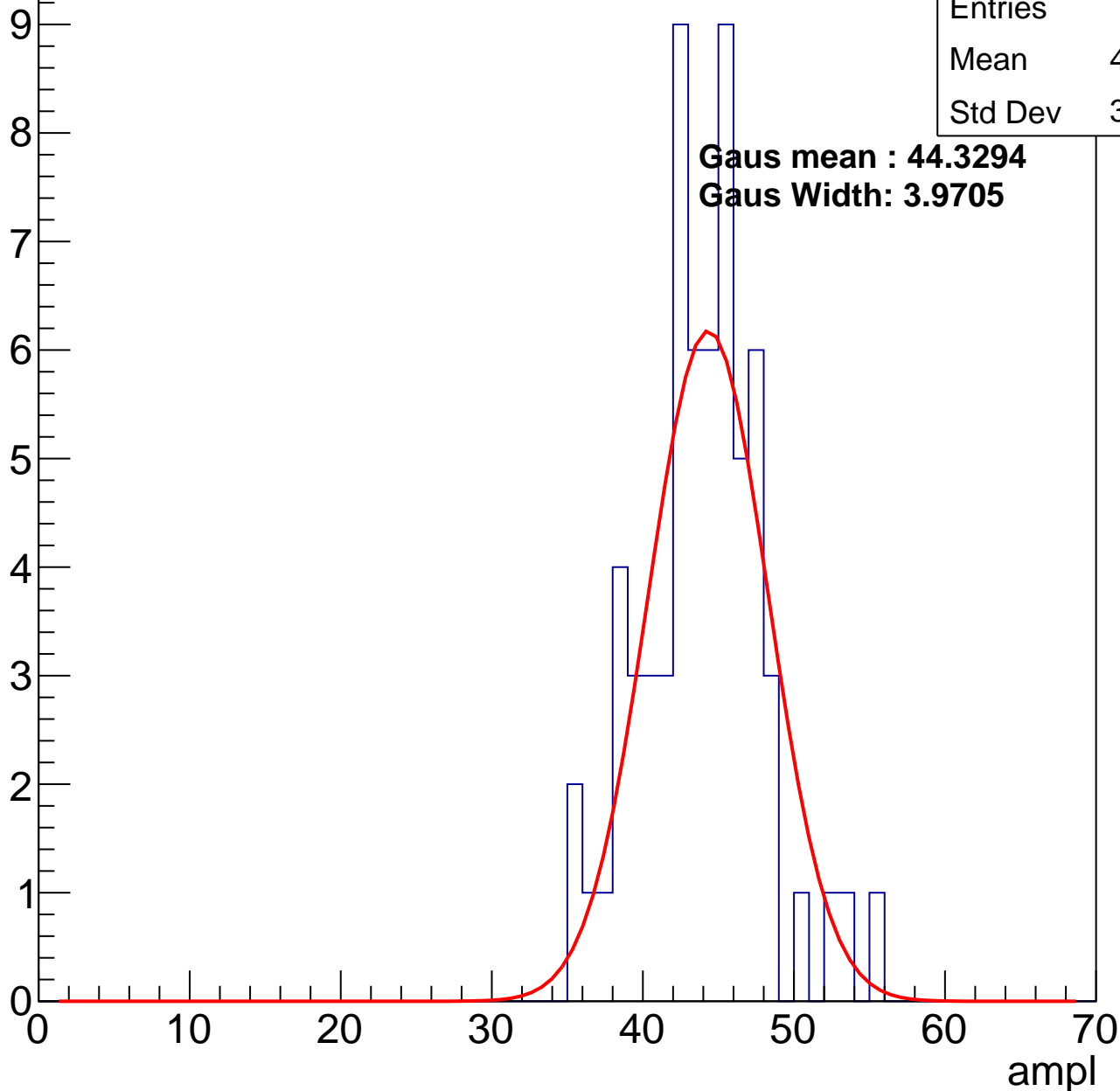
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	43.48
Std Dev	3.973

**Gaus mean : 44.3294**

**Gaus Width: 3.9705**



# B0L001S, U17-ch25, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

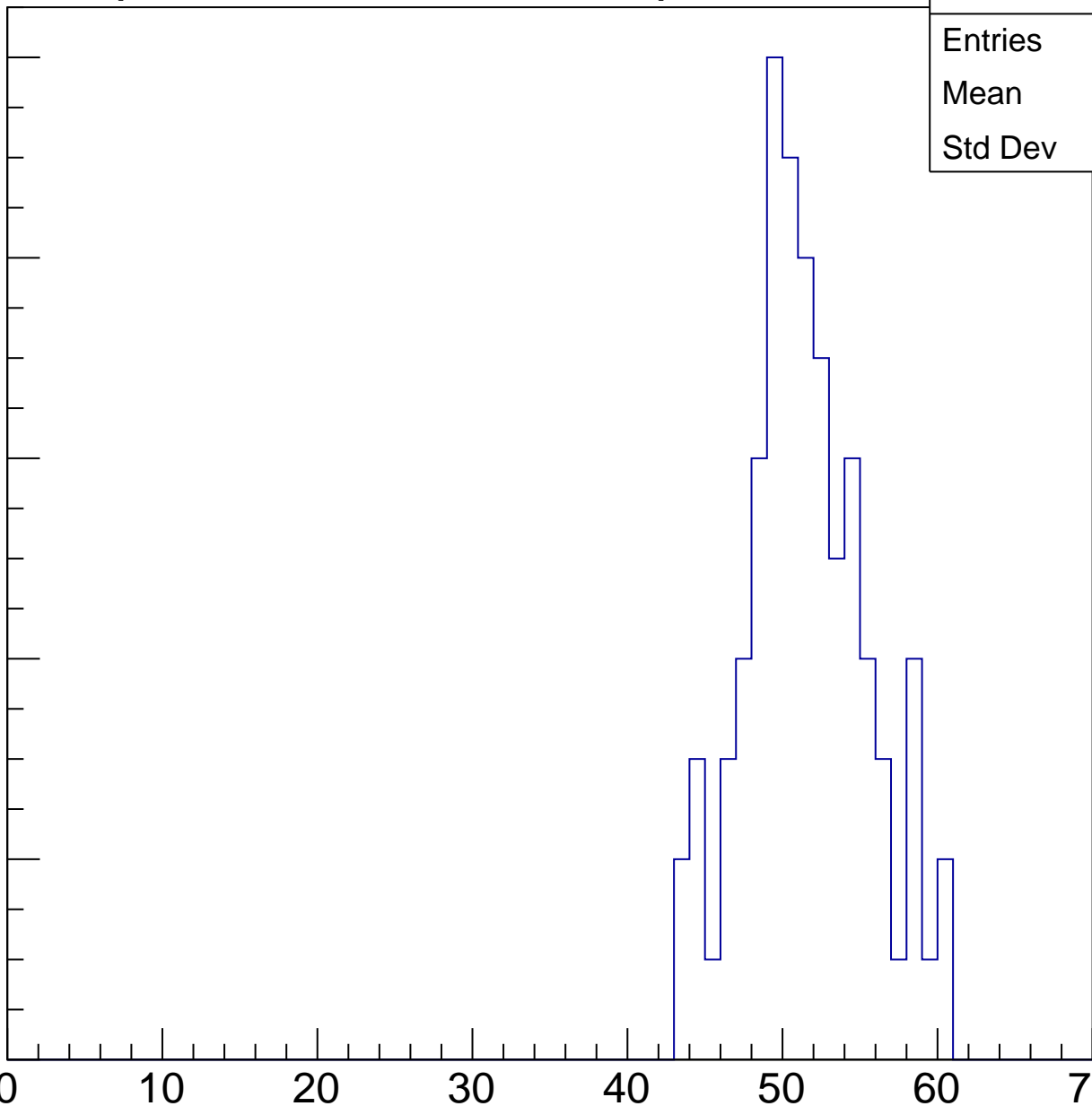
Entries	79
Mean	51.06
Std Dev	3.947

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

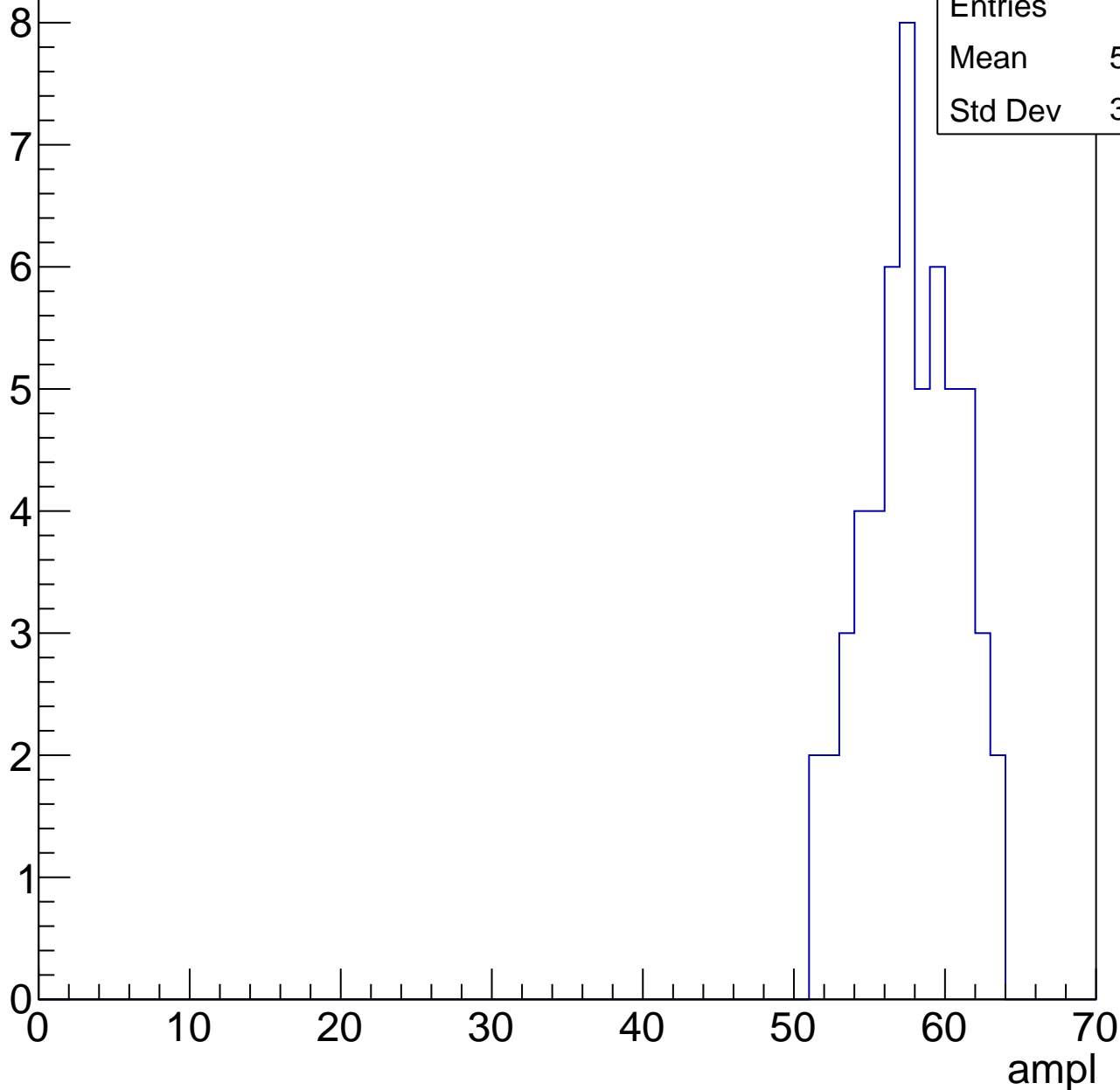


# B0L001S, U17-ch25, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	57.35
Std Dev	3.082

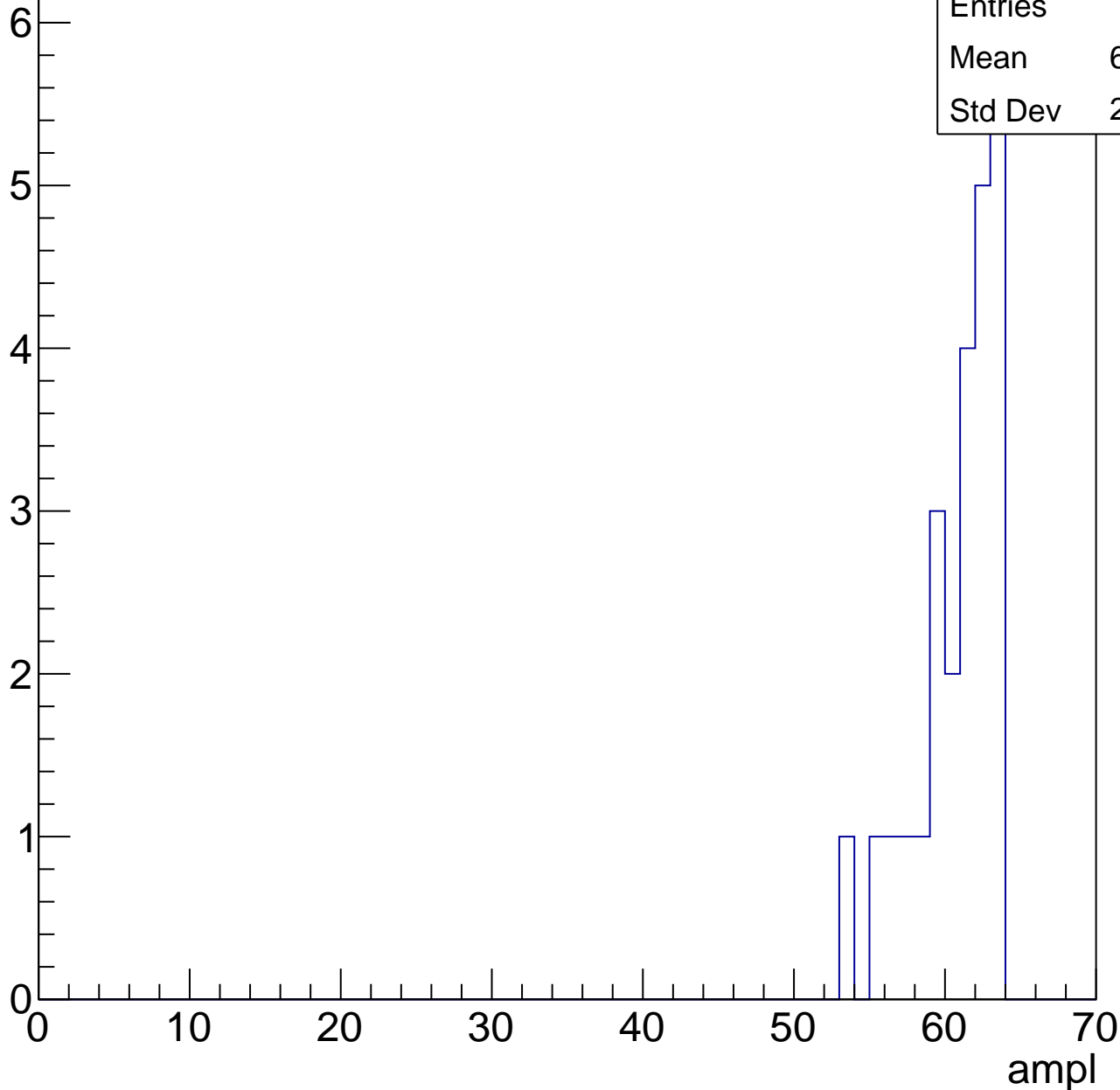


# B0L001S, U17-ch25, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

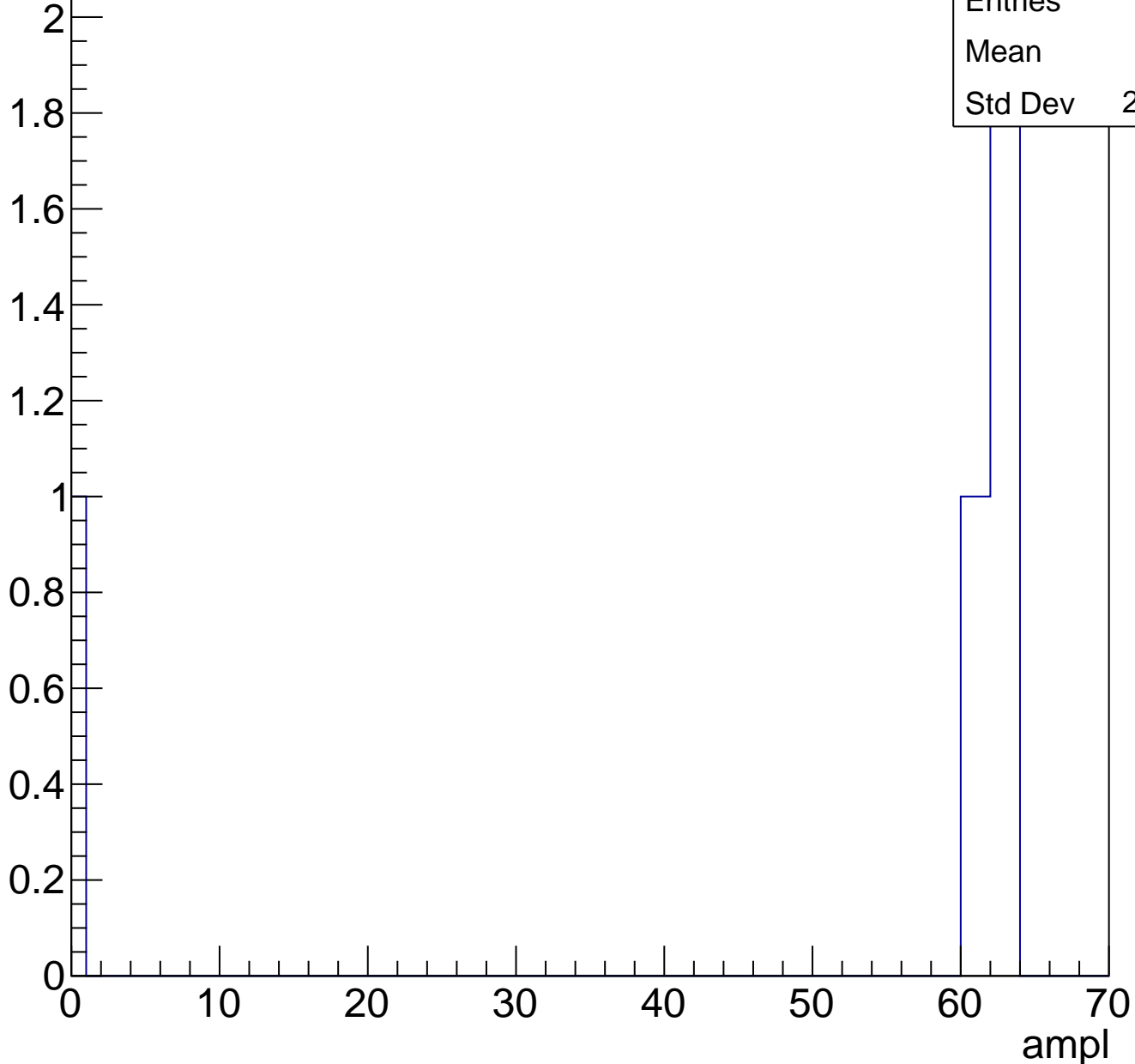
Entries	25
Mean	60.32
Std Dev	2.694



# B0L001S, U17-ch25, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

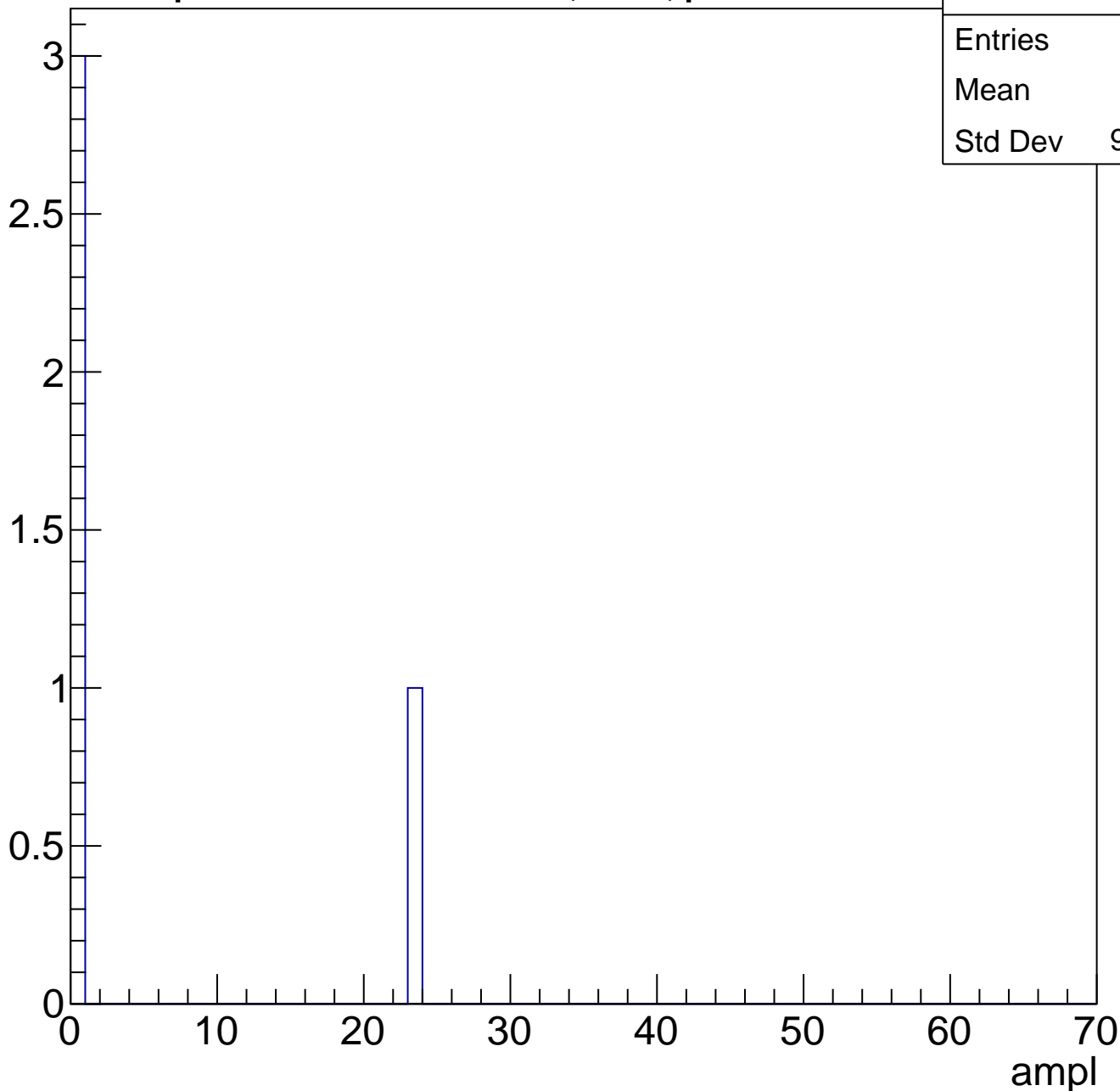




# B0L001S, U17-ch25, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	4
Mean	5.75
Std Dev	9.959

# B0L001S, U17-ch26, adc0

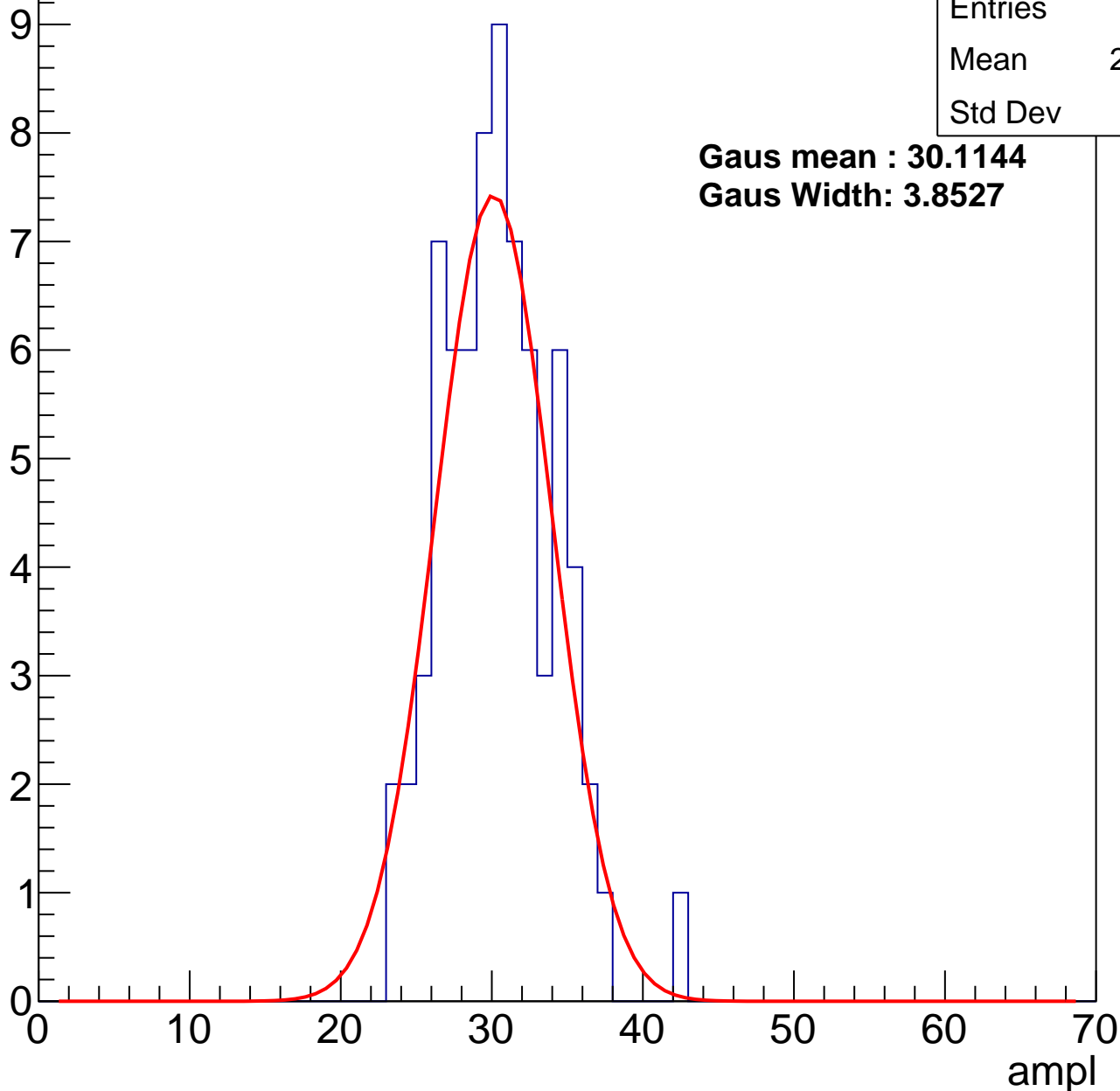
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	29.95
Std Dev	3.63

**Gaus mean : 30.1144**

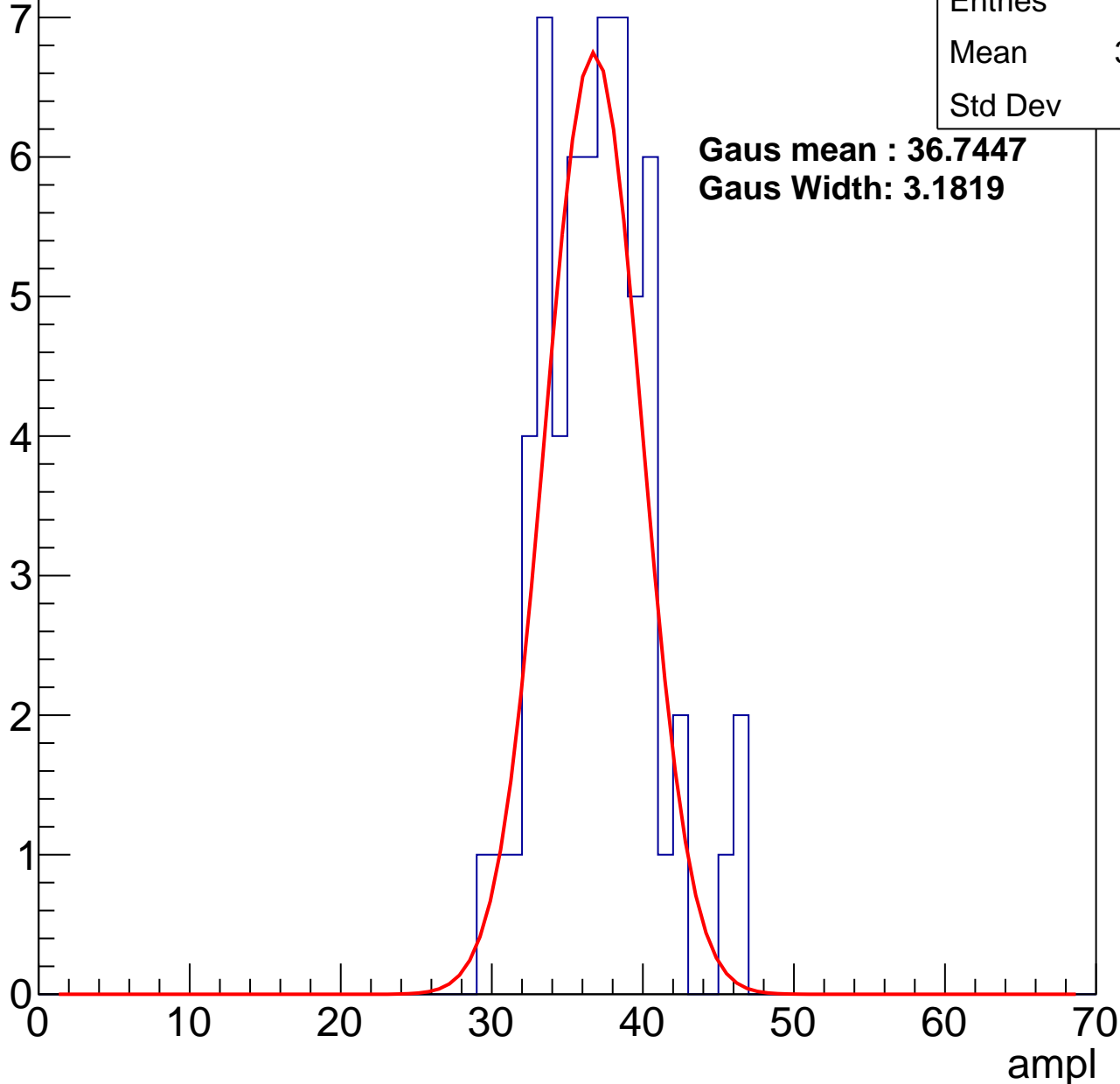
**Gaus Width: 3.8527**



# B0L001S, U17-ch26, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U17-ch26, adc2

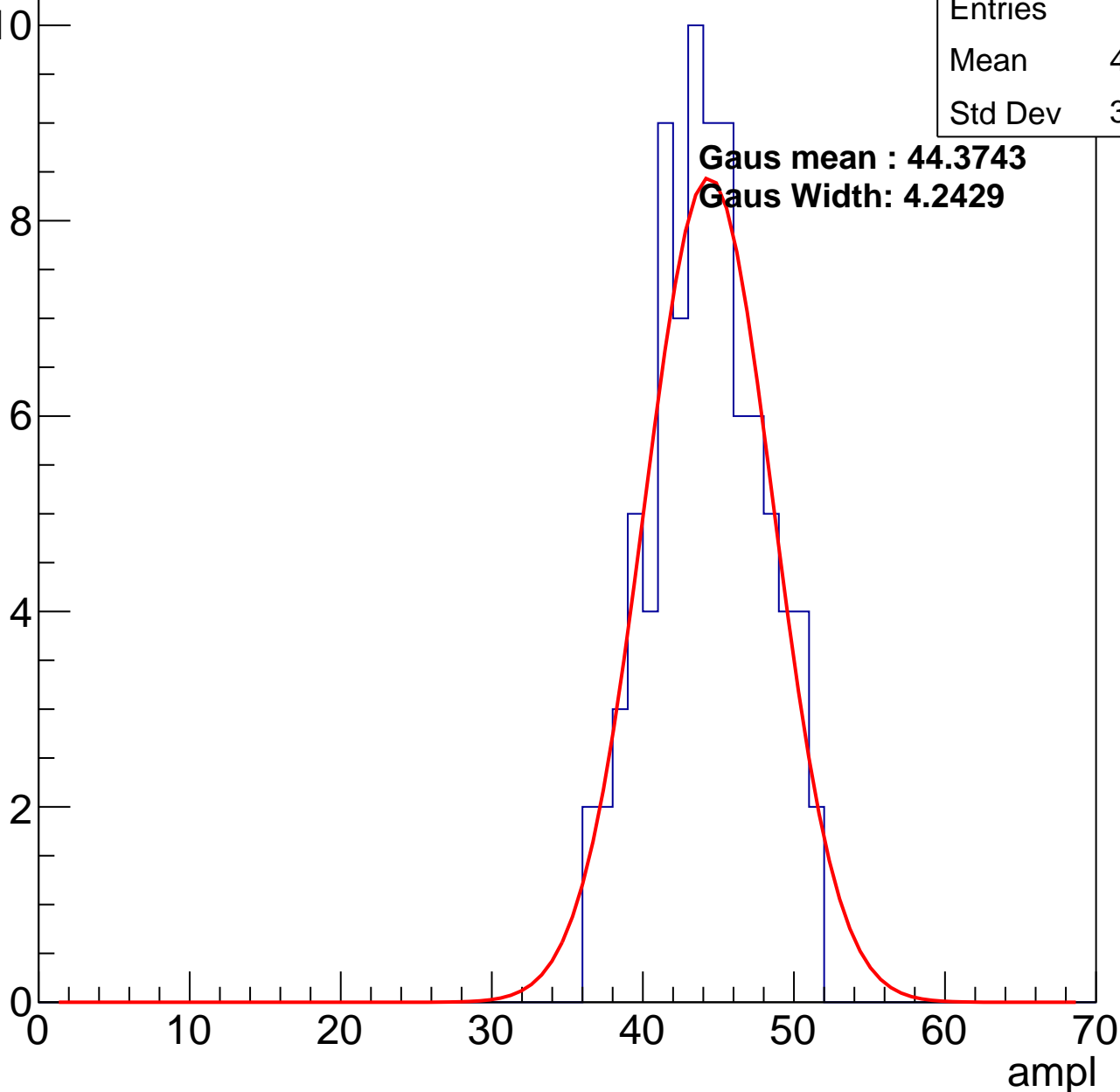
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	87
Mean	43.74
Std Dev	3.628

**Gaus mean : 44.3743**

**Gaus Width: 4.2429**

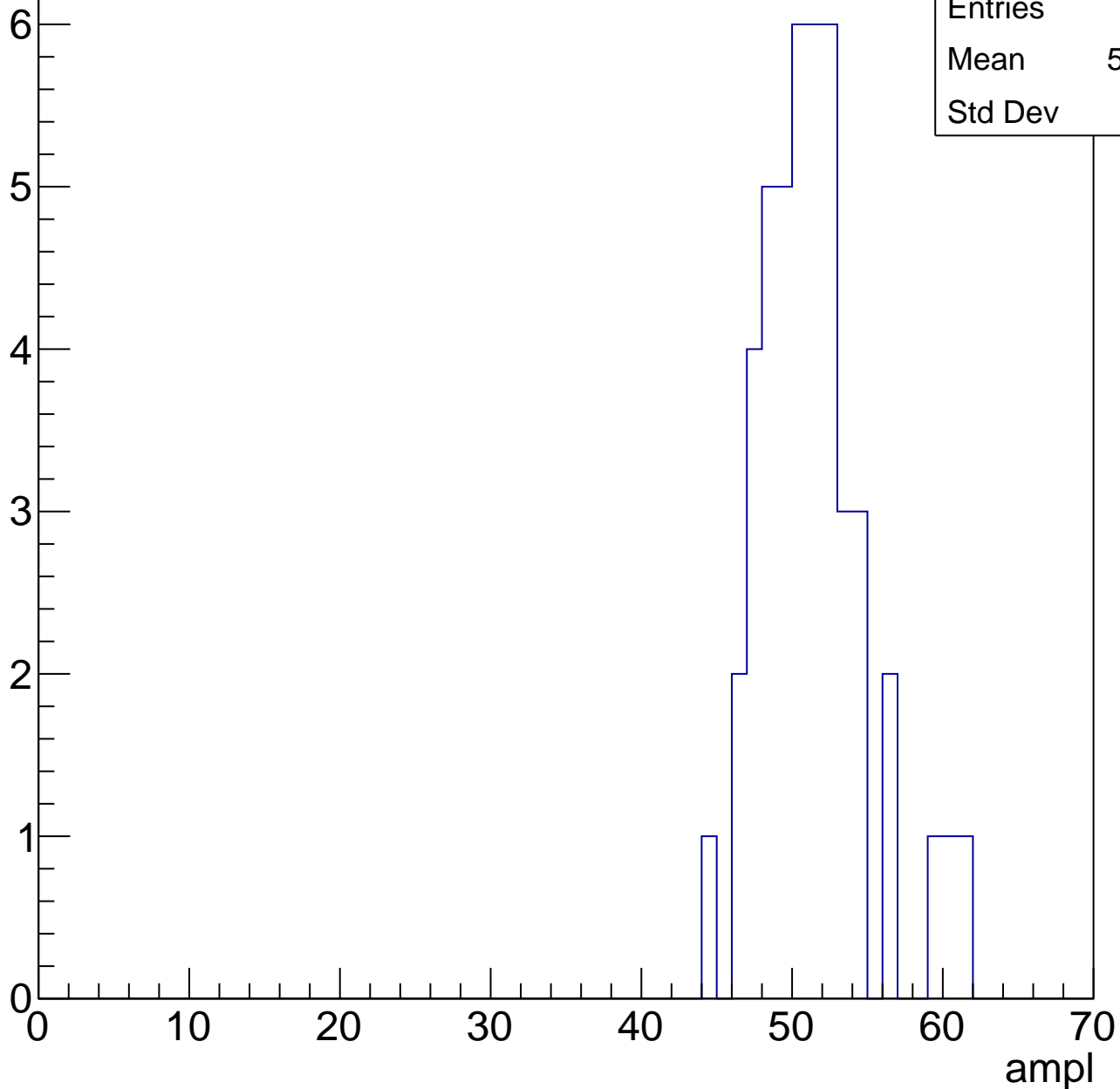


# B0L001S, U17-ch26, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	46
Mean	50.87
Std Dev	3.53

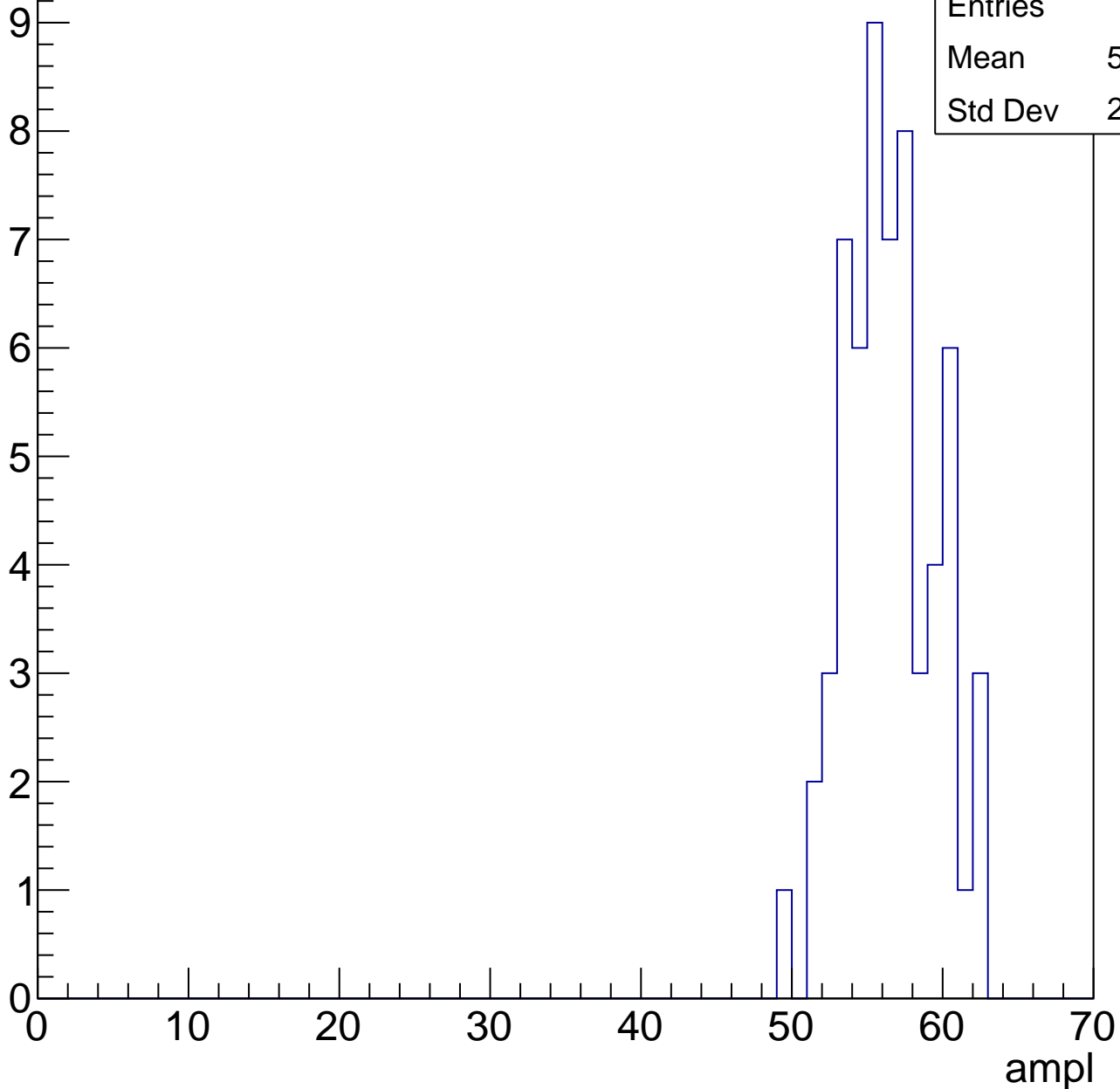


# B0L001S, U17-ch26, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	56.03
Std Dev	2.966

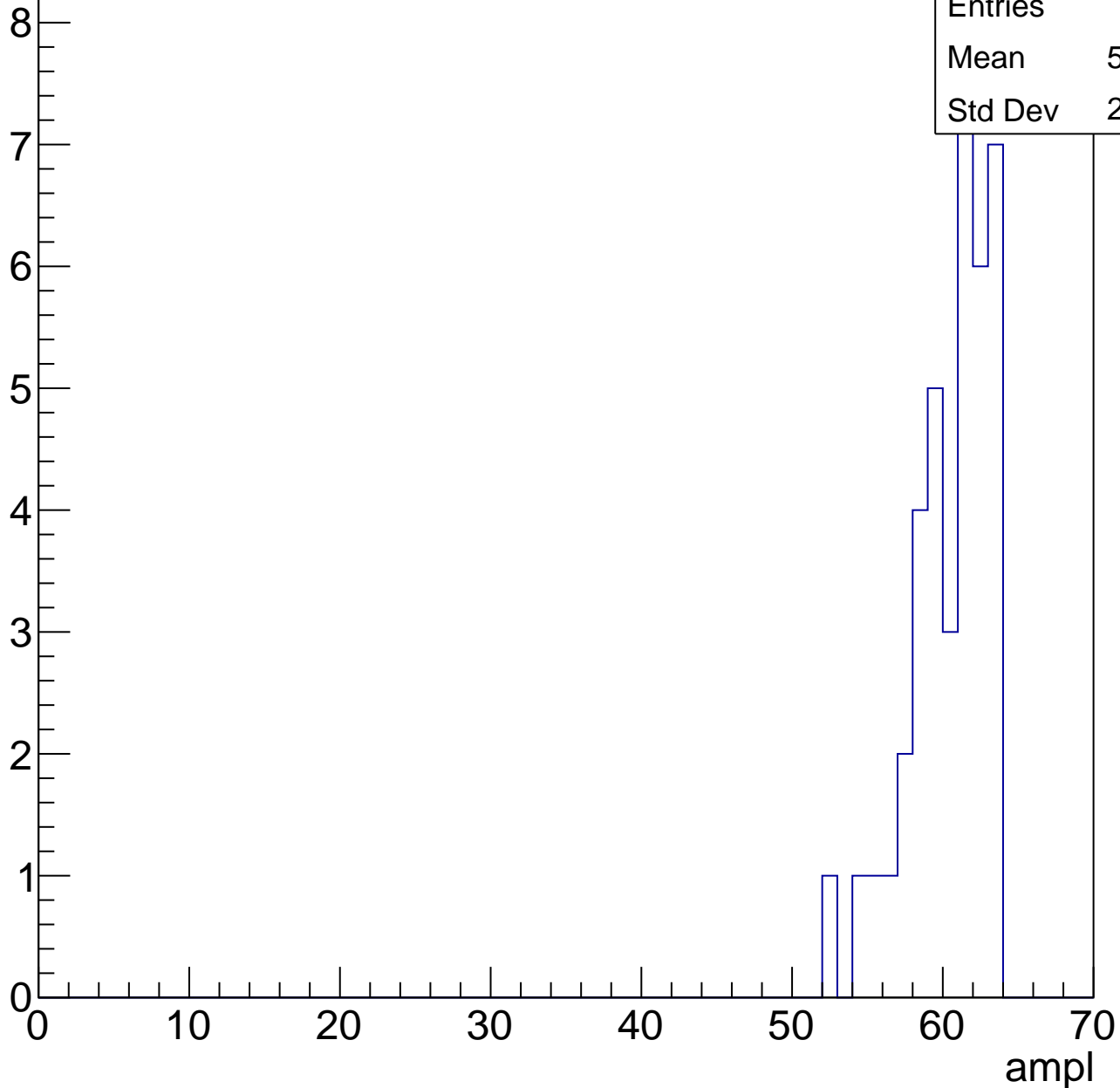


# B0L001S, U17-ch26, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	39
Mean	59.97
Std Dev	2.655



# B0L001S, U17-ch26, adc6

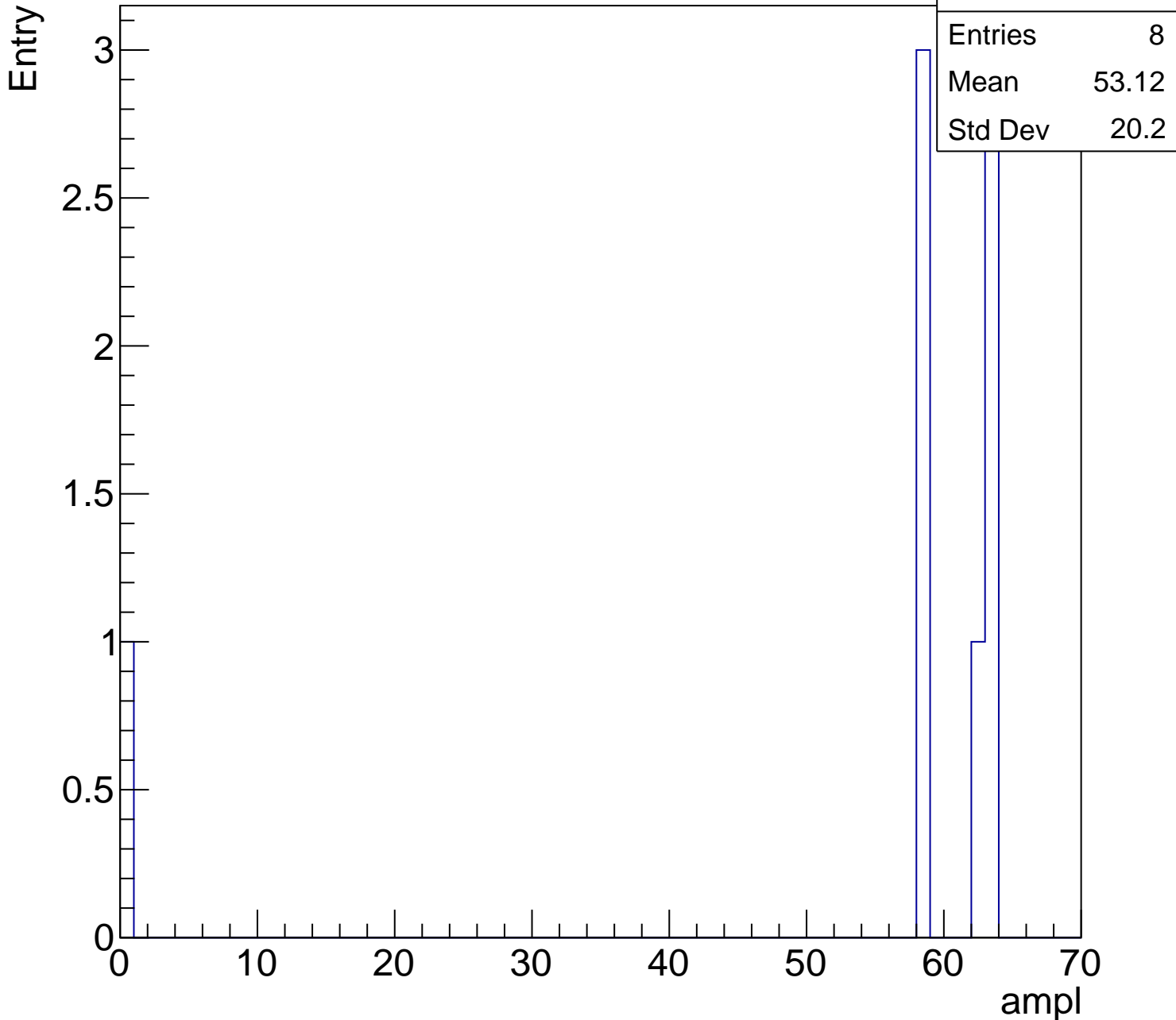
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

3  
2.5  
2  
1.5  
1  
0.5  
0

Entries	8
Mean	53.12
Std Dev	20.2

ampl





# B0L001S, U17-ch26, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	3
Mean	0
Std Dev	0

# B0L001S, U17-ch27, adc0

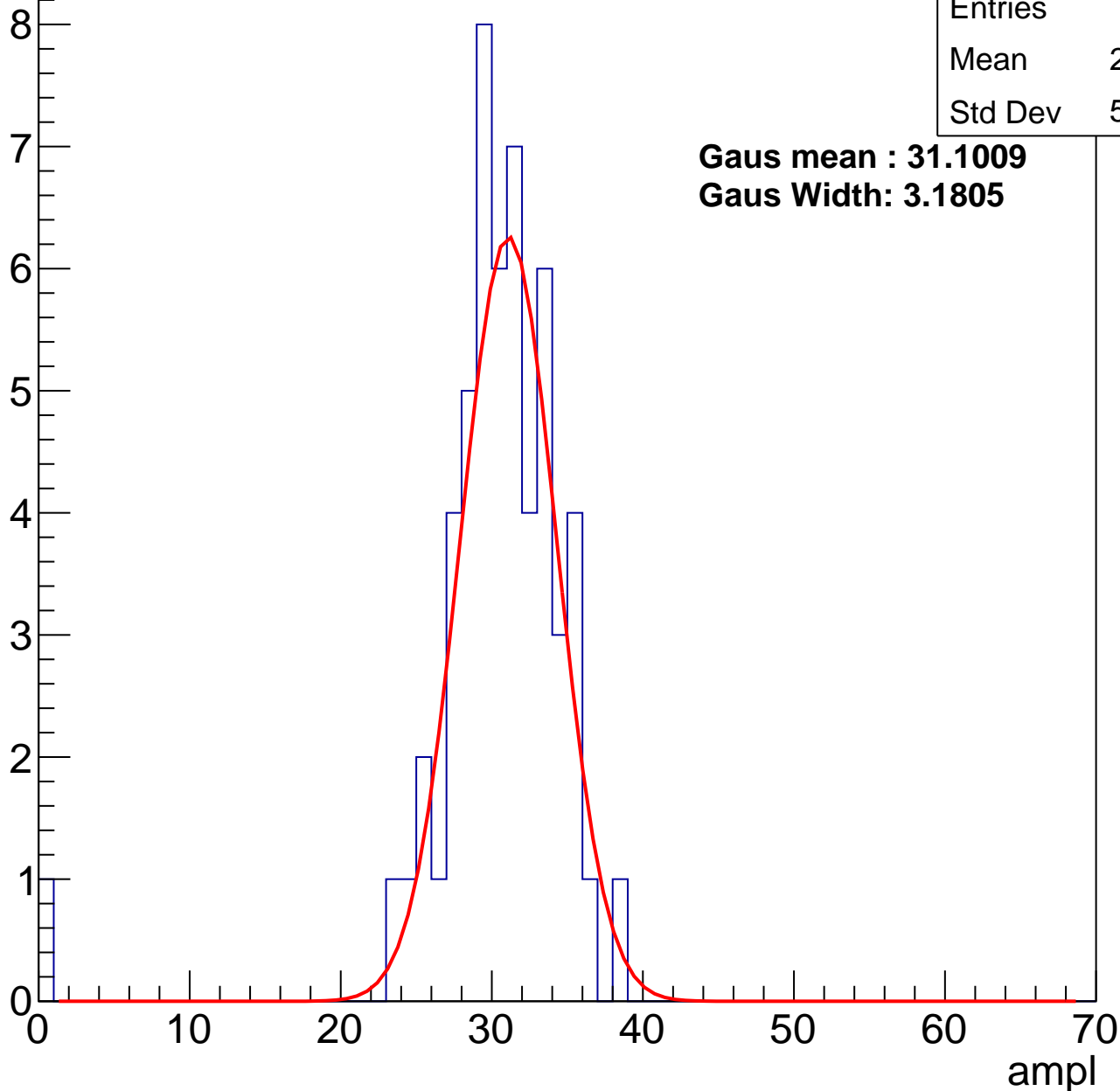
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	29.85
Std Dev	5.115

**Gaus mean : 31.1009**

**Gaus Width: 3.1805**



# B0L001S, U17-ch27, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	79
Mean	36.39
Std Dev	4.141

**Gaus mean : 37.4782**

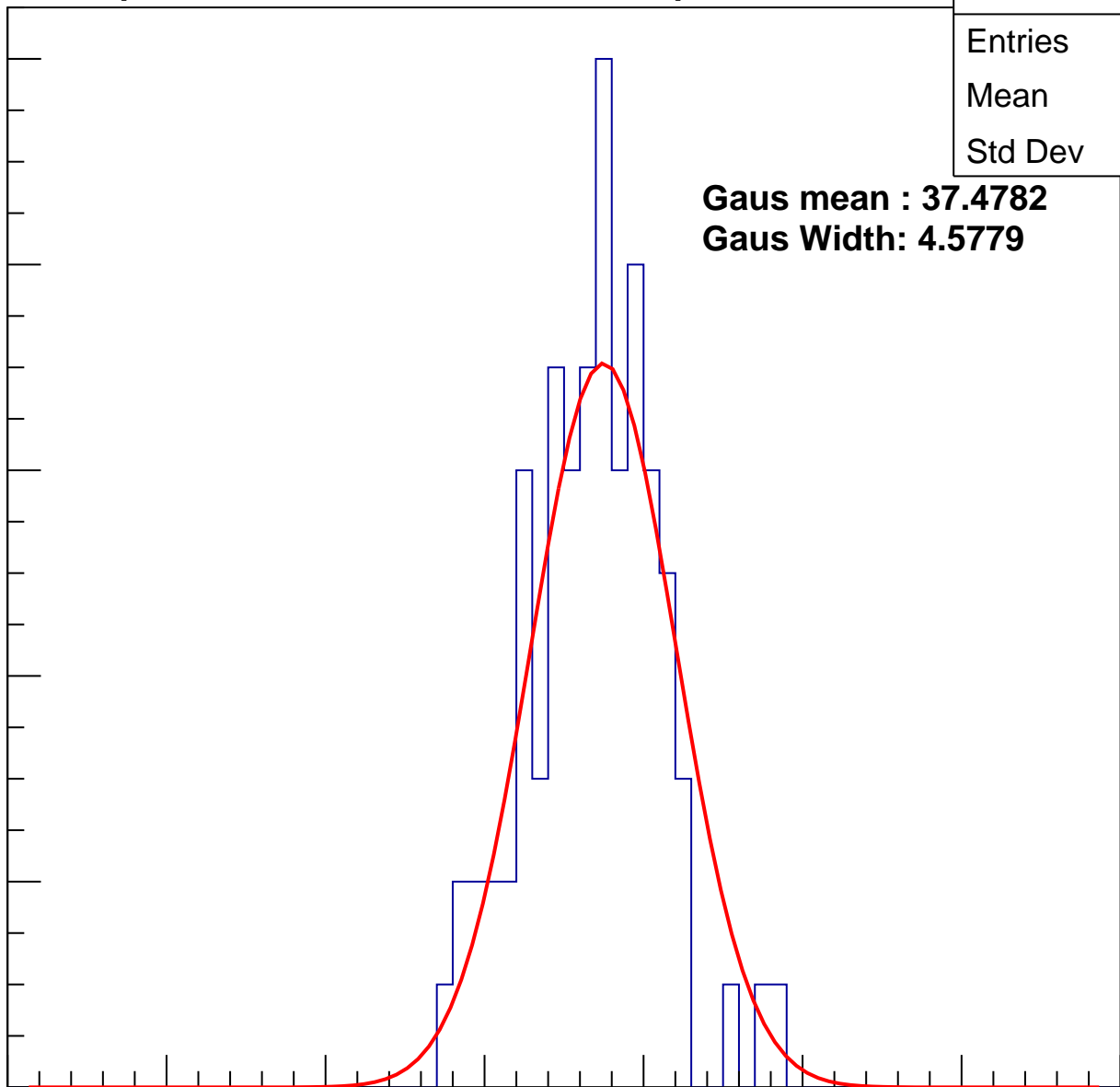
**Gaus Width: 4.5779**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B0L001S, U17-ch27, adc2

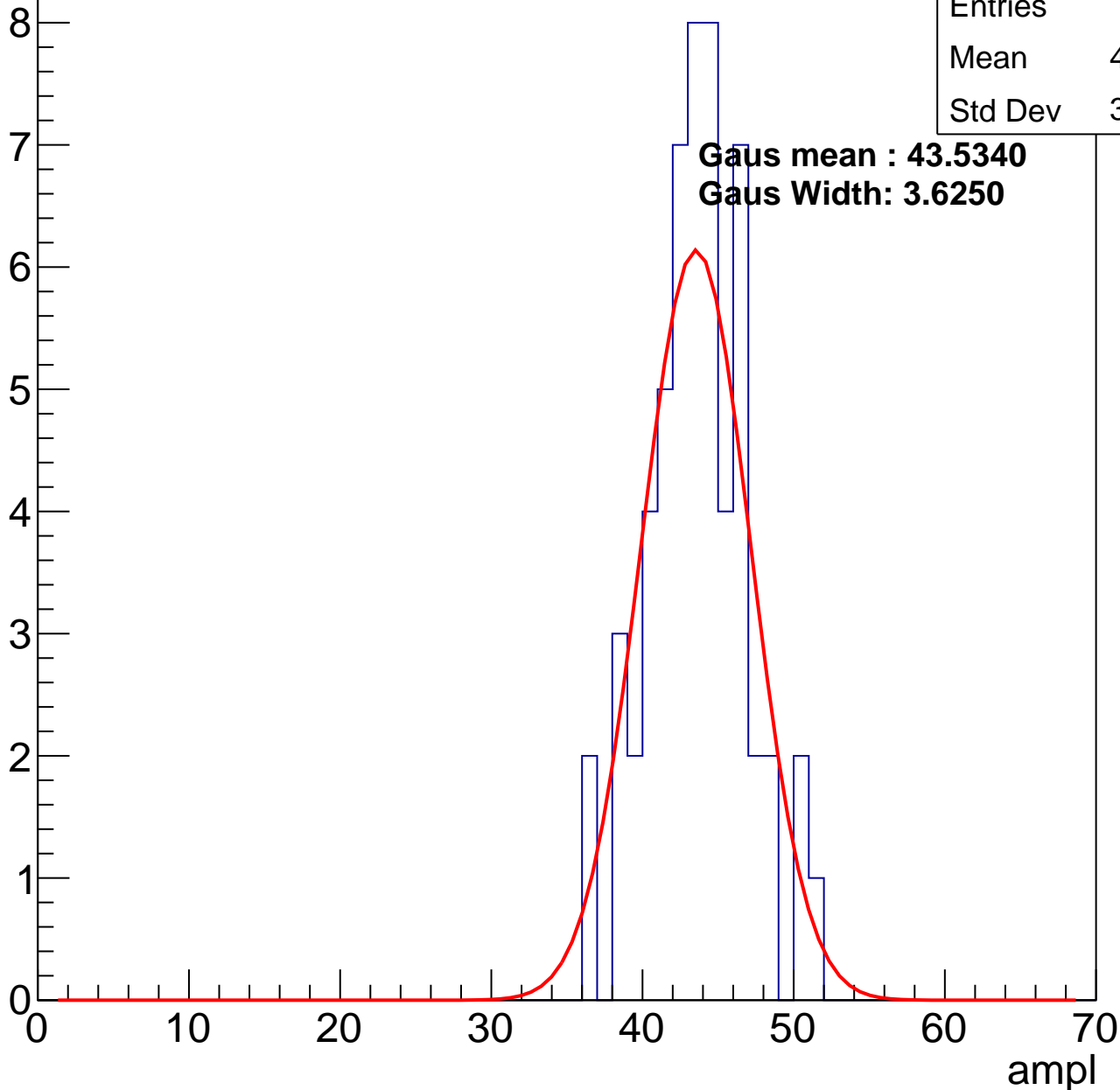
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	43.19
Std Dev	3.236

**Gaus mean : 43.5340**

**Gaus Width: 3.6250**



# B0L001S, U17-ch27, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

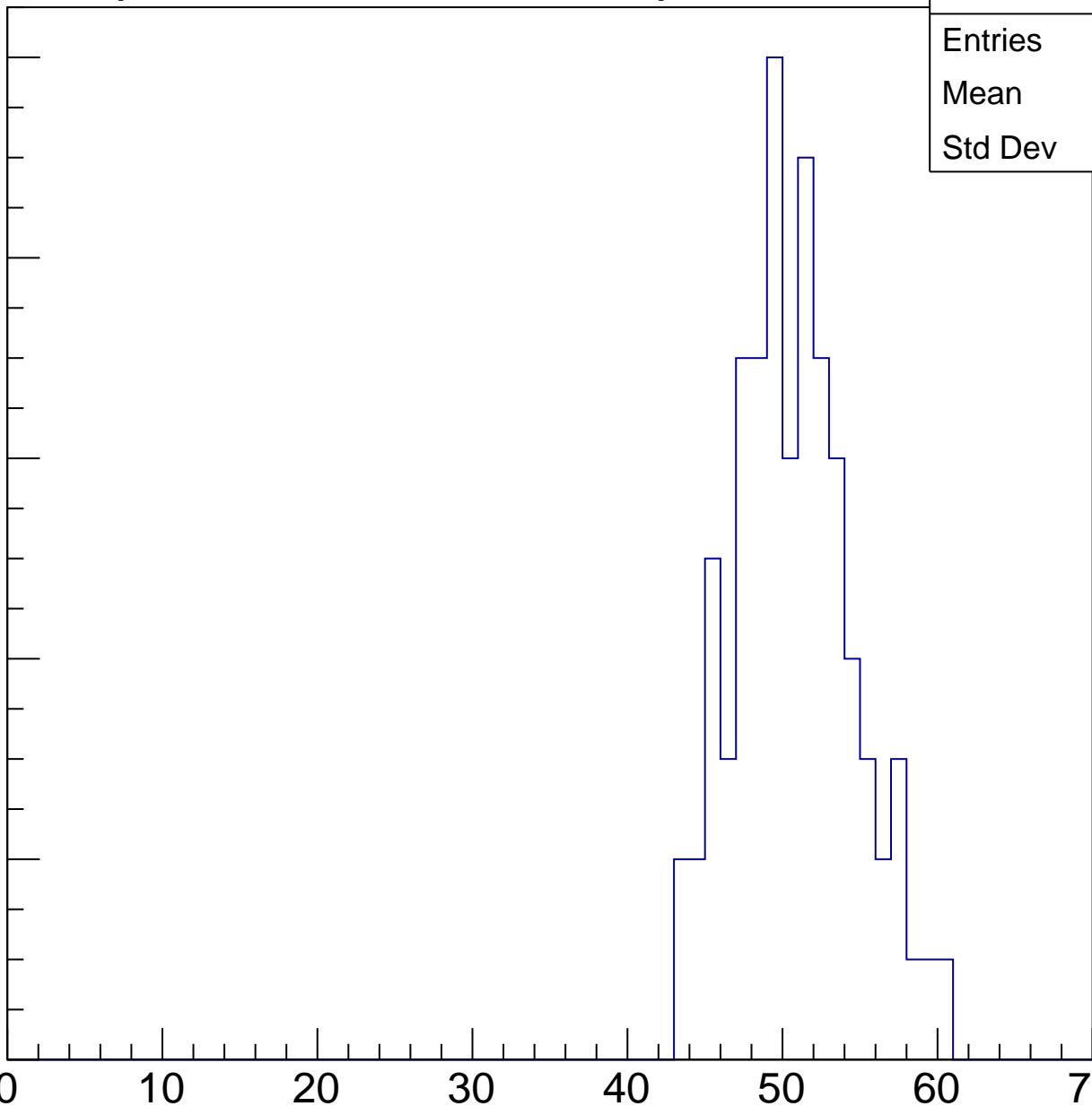
Entries	79
Mean	50.3
Std Dev	3.783

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

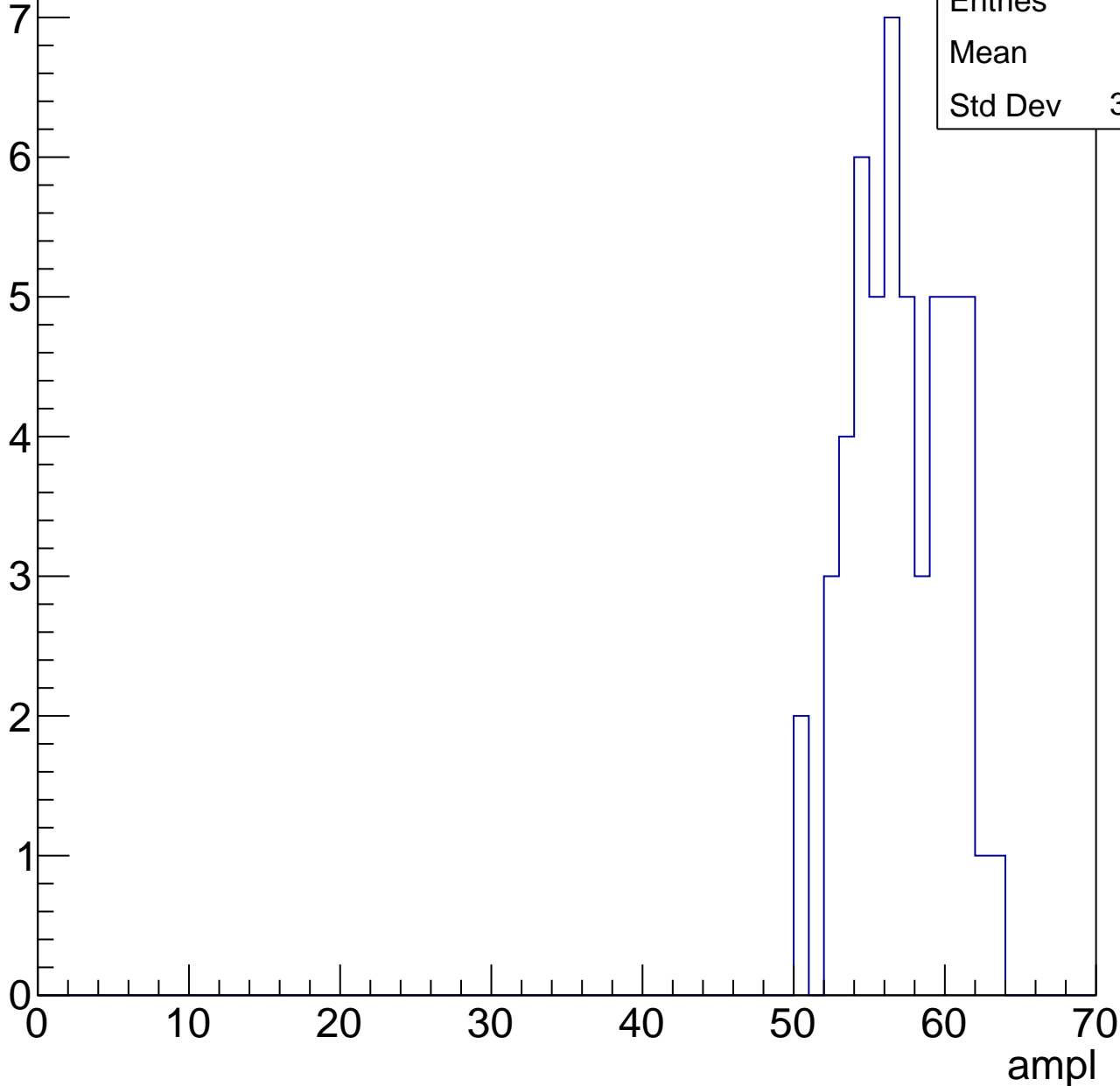


# B0L001S, U17-ch27, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	56.6
Std Dev	3.158

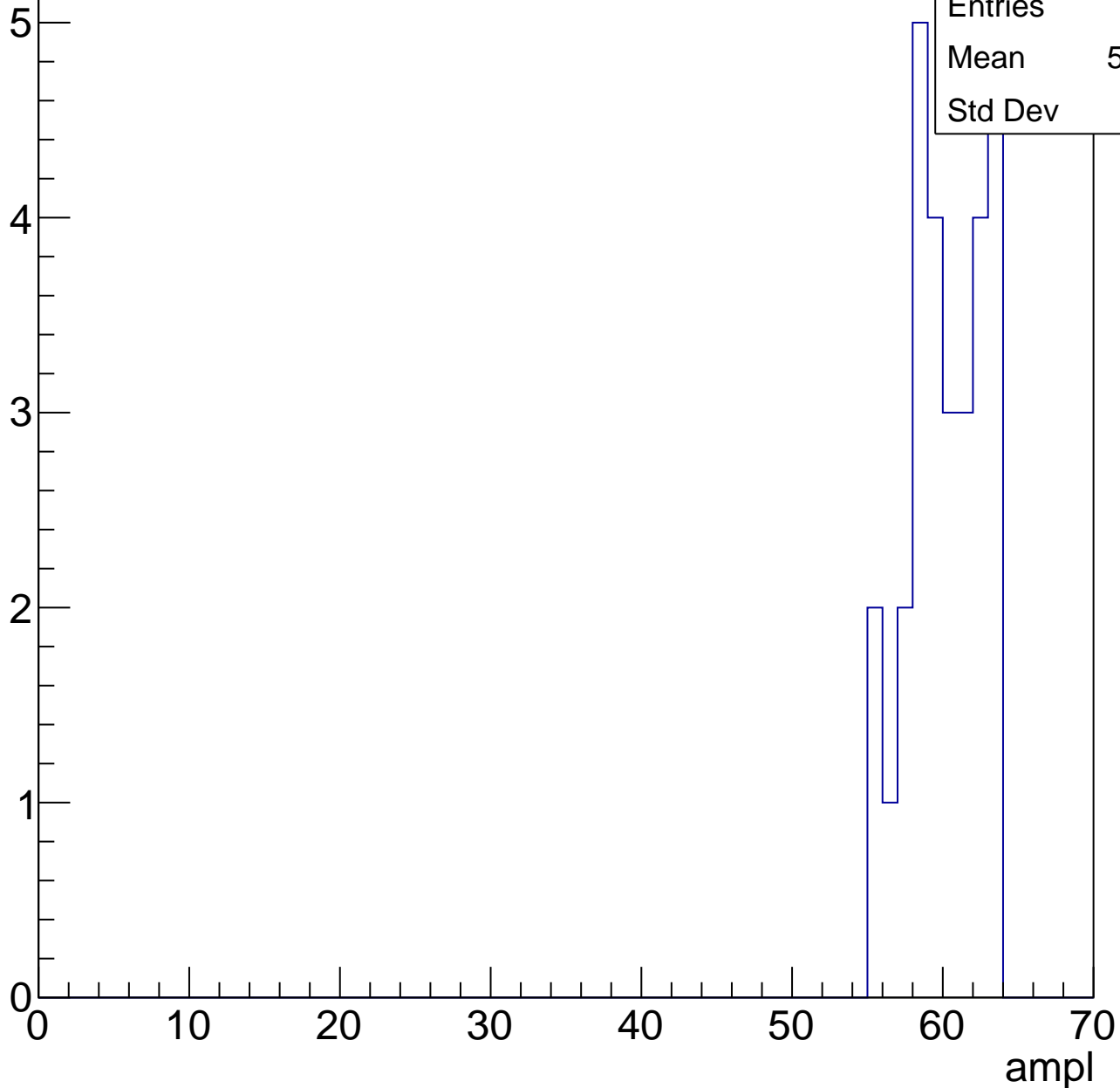


# B0L001S, U17-ch27, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	29
Mean	59.72
Std Dev	2.42

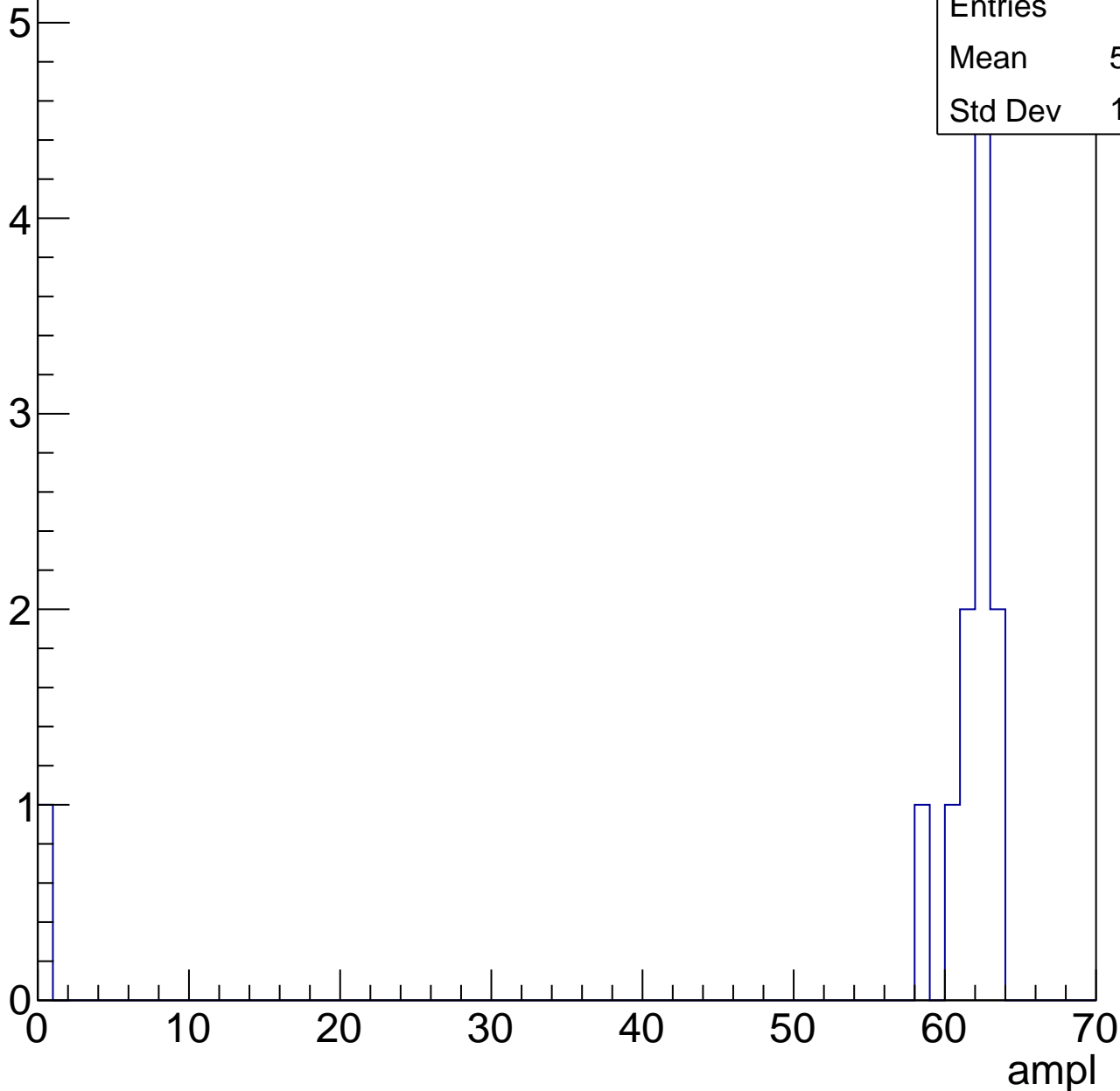


# B0L001S, U17-ch27, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	12
Mean	56.33
Std Dev	17.04





# B0L001S, U17-ch27, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U17-ch28, adc0

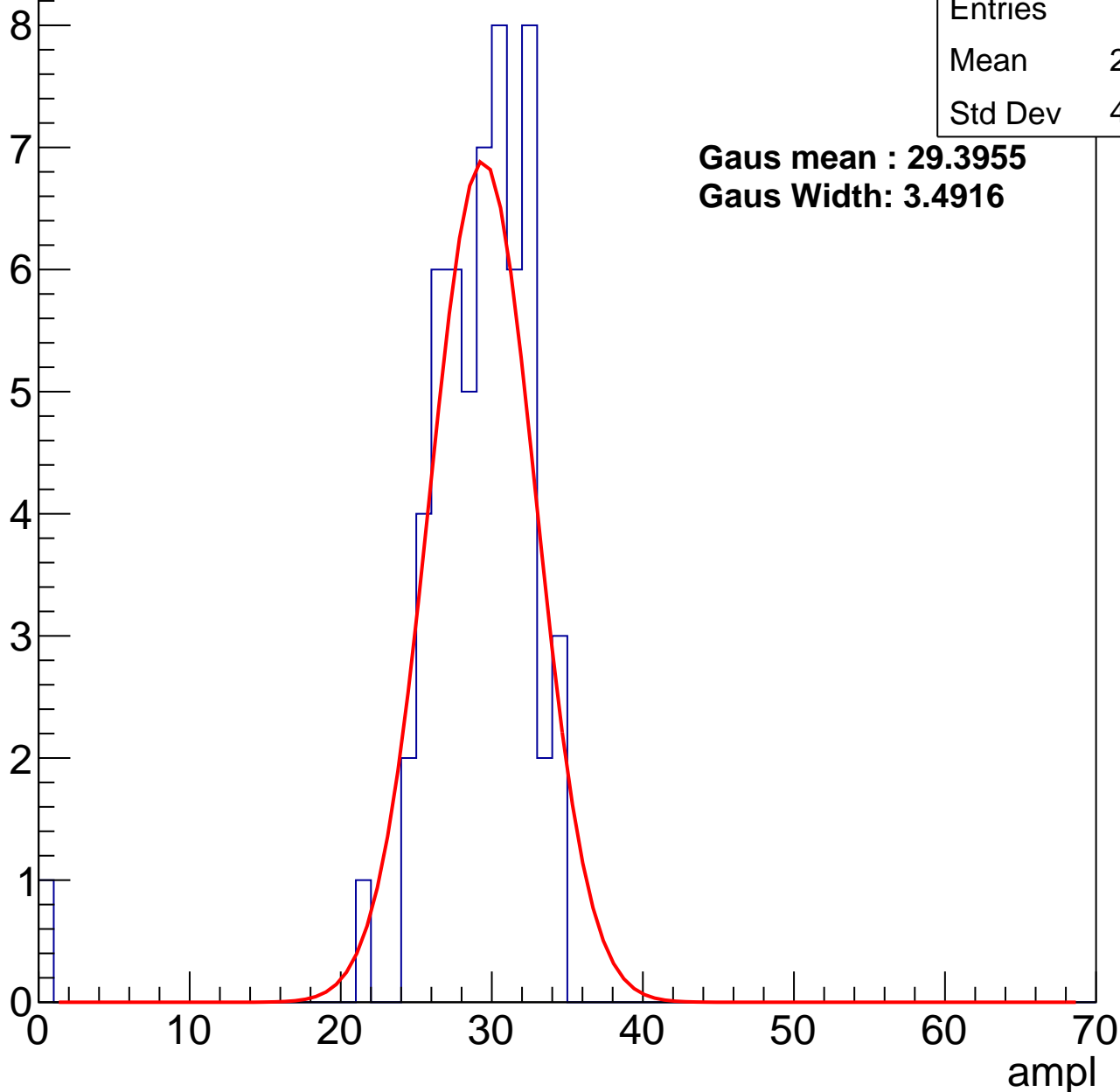
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	28.47
Std Dev	4.688

**Gaus mean : 29.3955**

**Gaus Width: 3.4916**



# B0L001S, U17-ch28, adc1

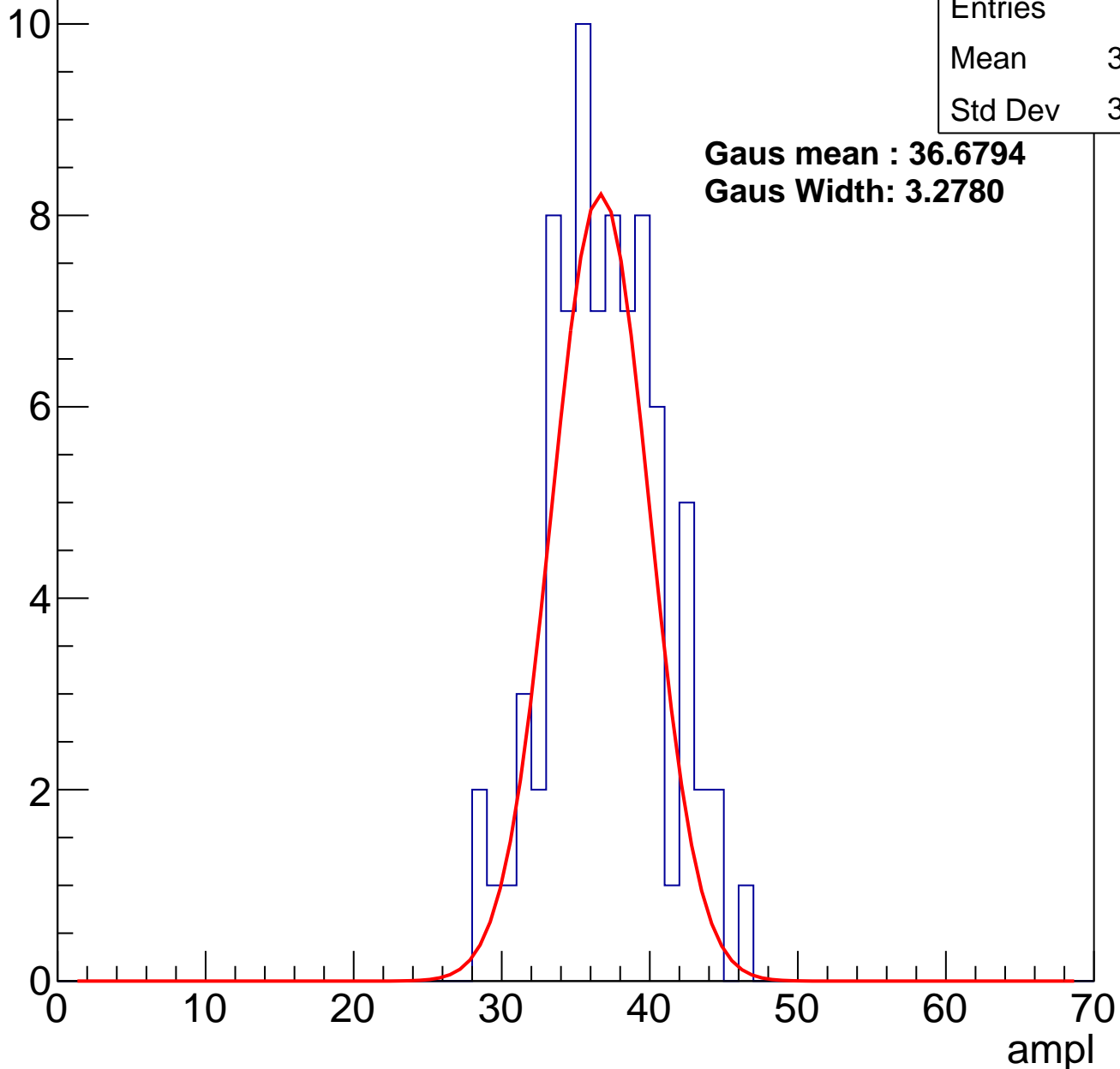
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	81
Mean	36.56
Std Dev	3.752

**Gaus mean : 36.6794**

**Gaus Width: 3.2780**

Entry



# B0L001S, U17-ch28, adc2

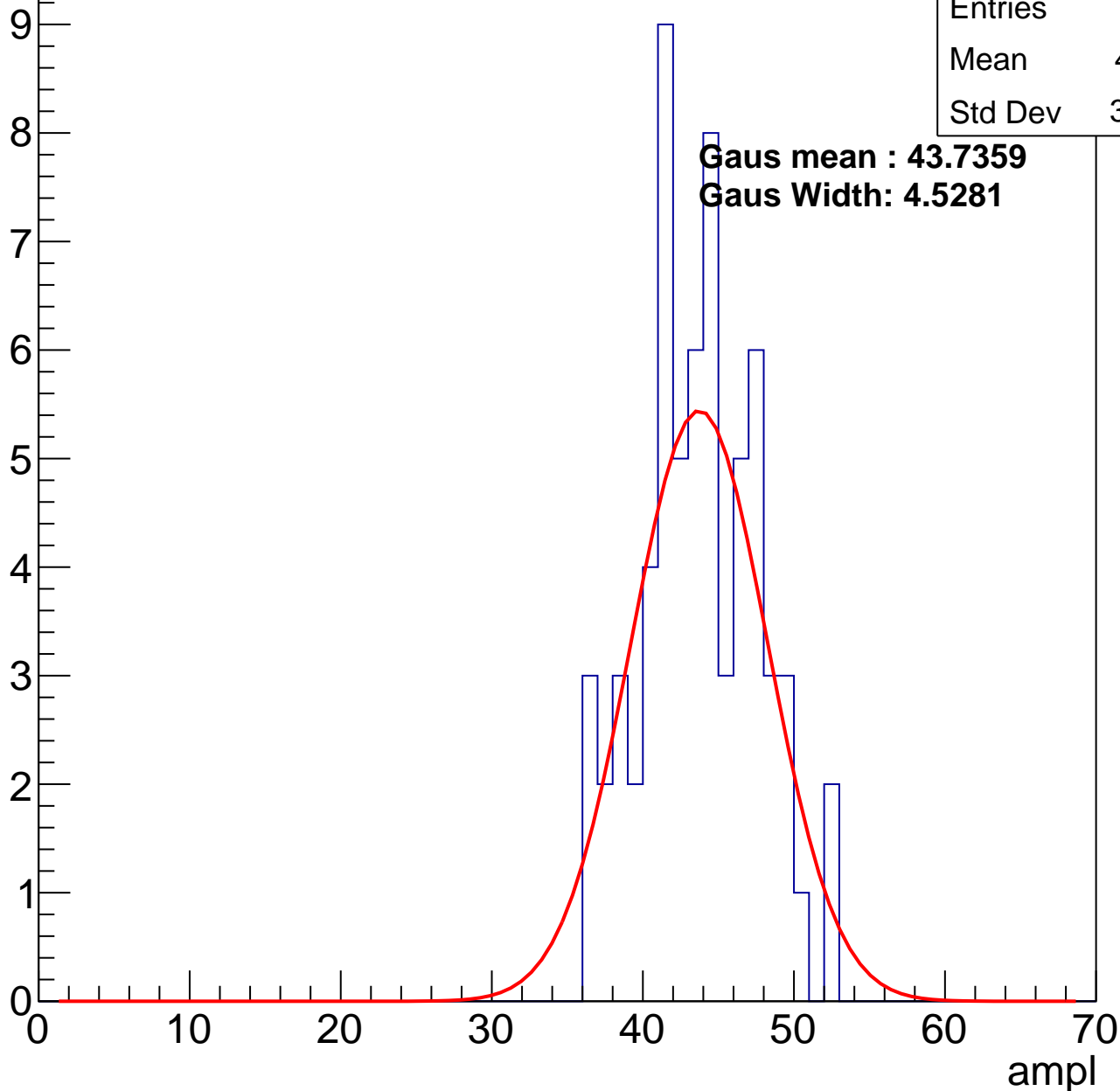
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	43.31
Std Dev	3.827

**Gaus mean : 43.7359**

**Gaus Width: 4.5281**

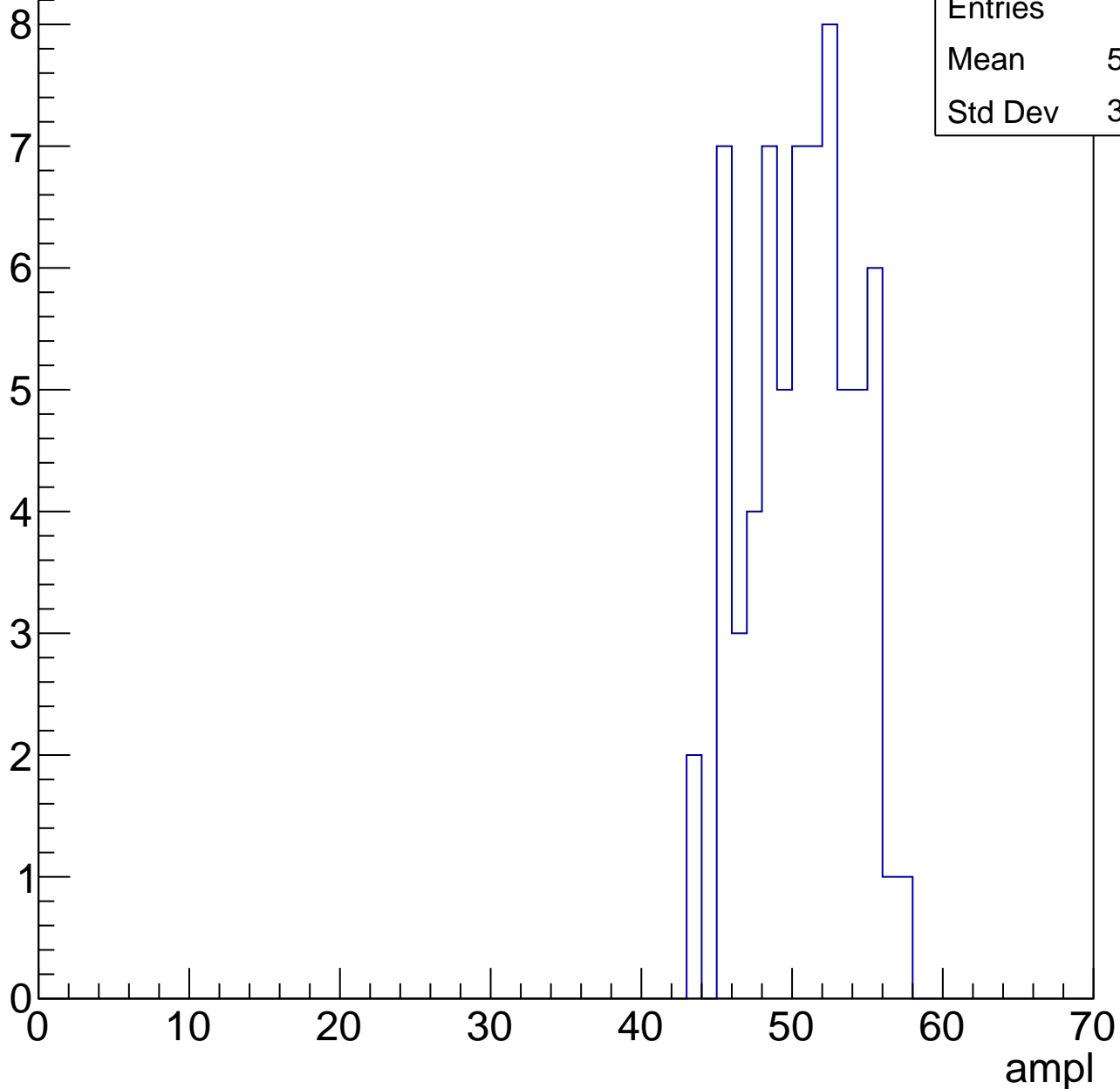


# B0L001S, U17-ch28, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	50.13
Std Dev	3.404

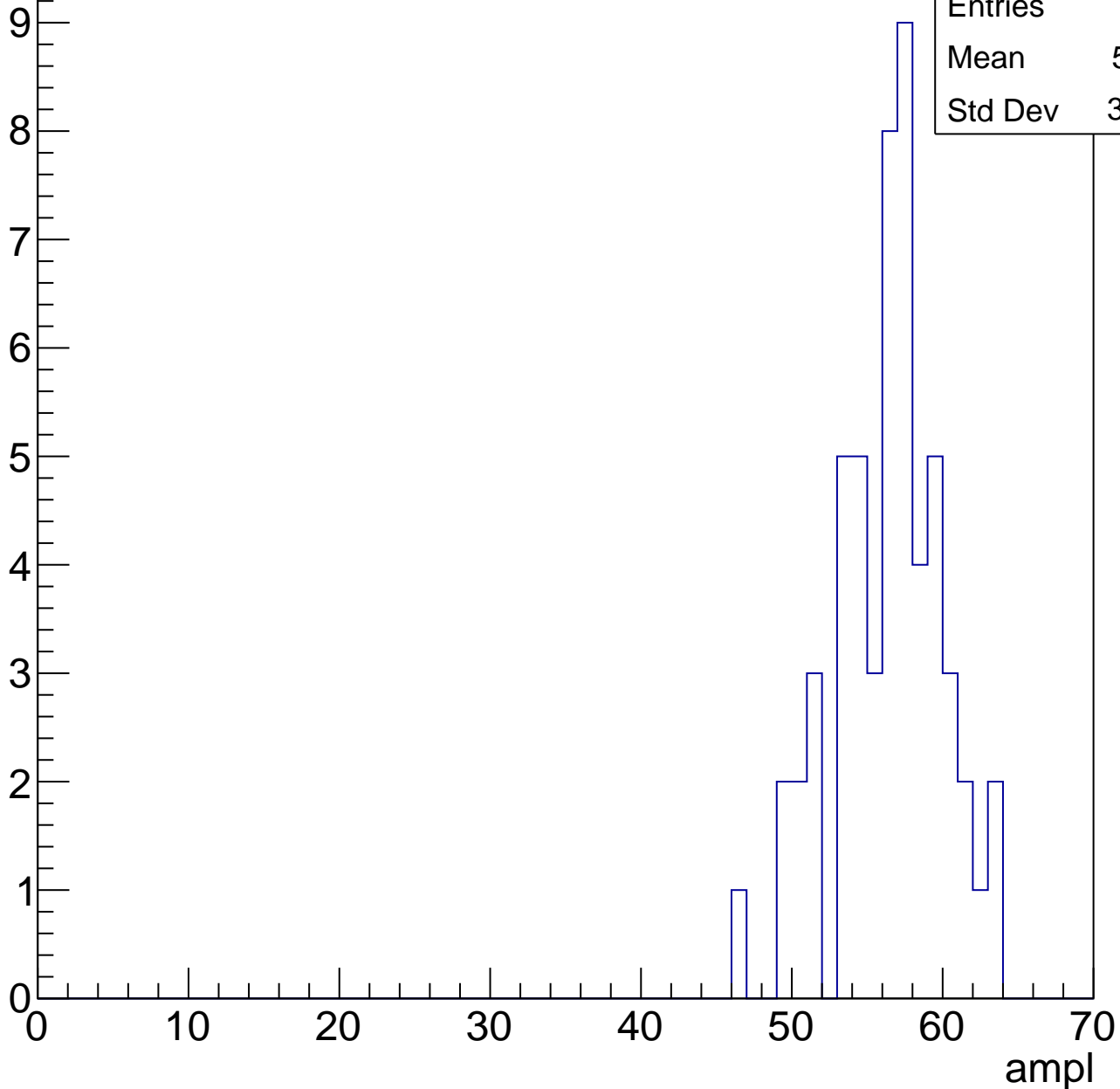


# B0L001S, U17-ch28, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	55.91
Std Dev	3.604

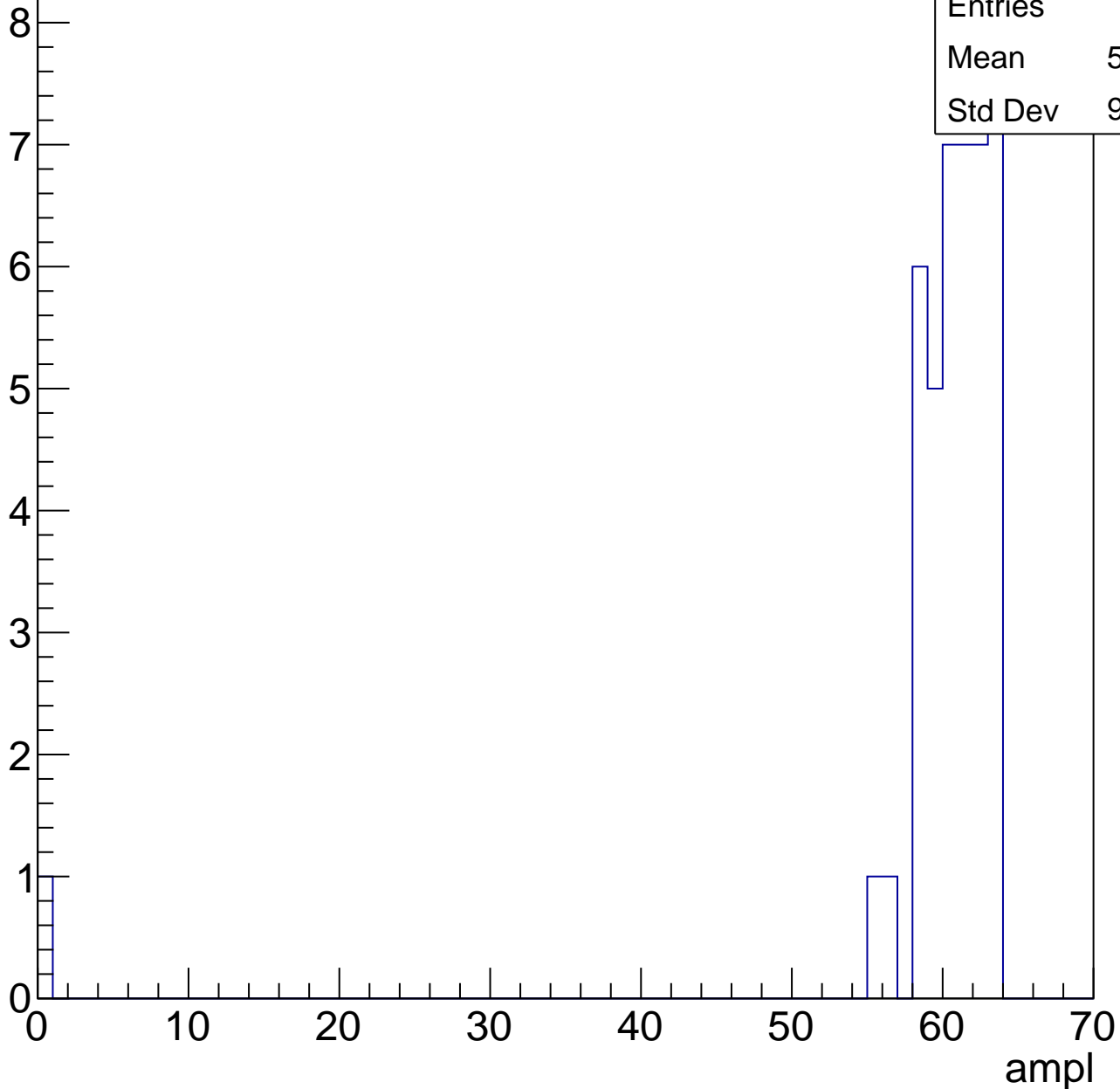


# B0L001S, U17-ch28, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	43
Mean	59.05
Std Dev	9.324



# B0L001S, U17-ch28, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	61.67
Std Dev	0.4714

ampl

0 10 20 30 40 50 60 70



# B0L001S, U17-ch28, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U17-ch29, adc0

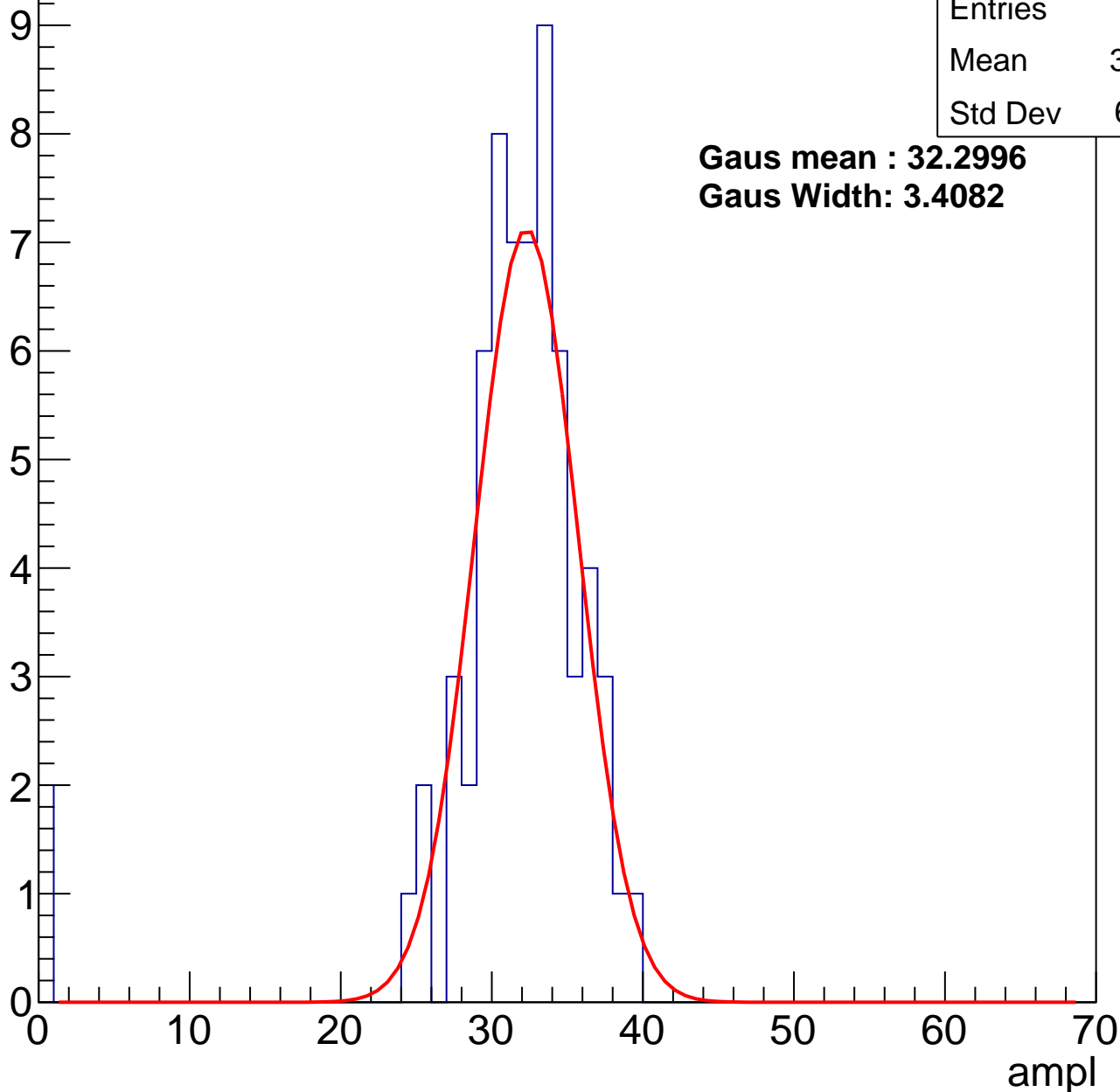
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	30.83
Std Dev	6.331

**Gaus mean : 32.2996**

**Gaus Width: 3.4082**



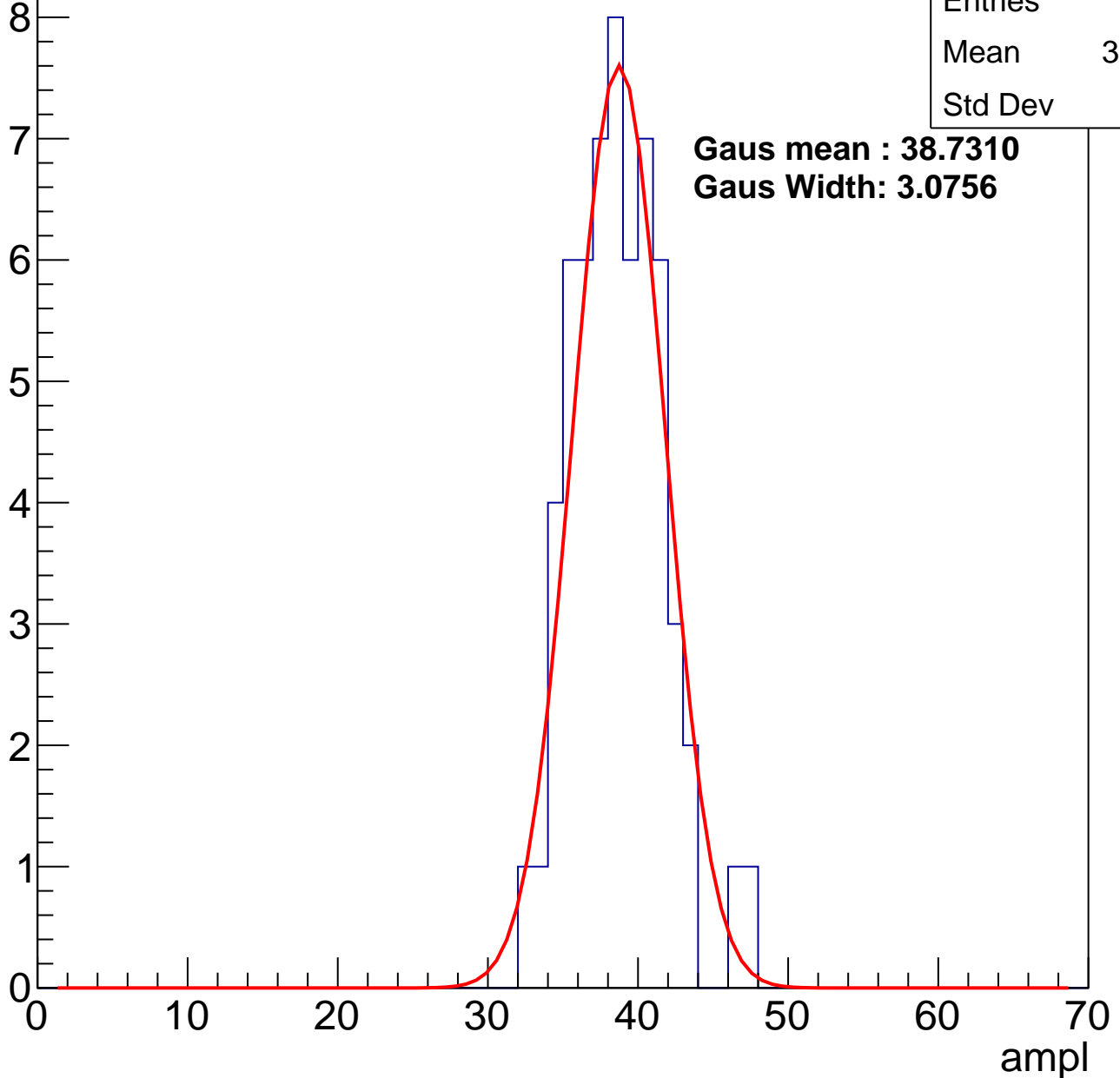
# B0L001S, U17-ch29, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	38.22
Std Dev	3.02

**Gaus mean : 38.7310**  
**Gaus Width: 3.0756**



# B0L001S, U17-ch29, adc2

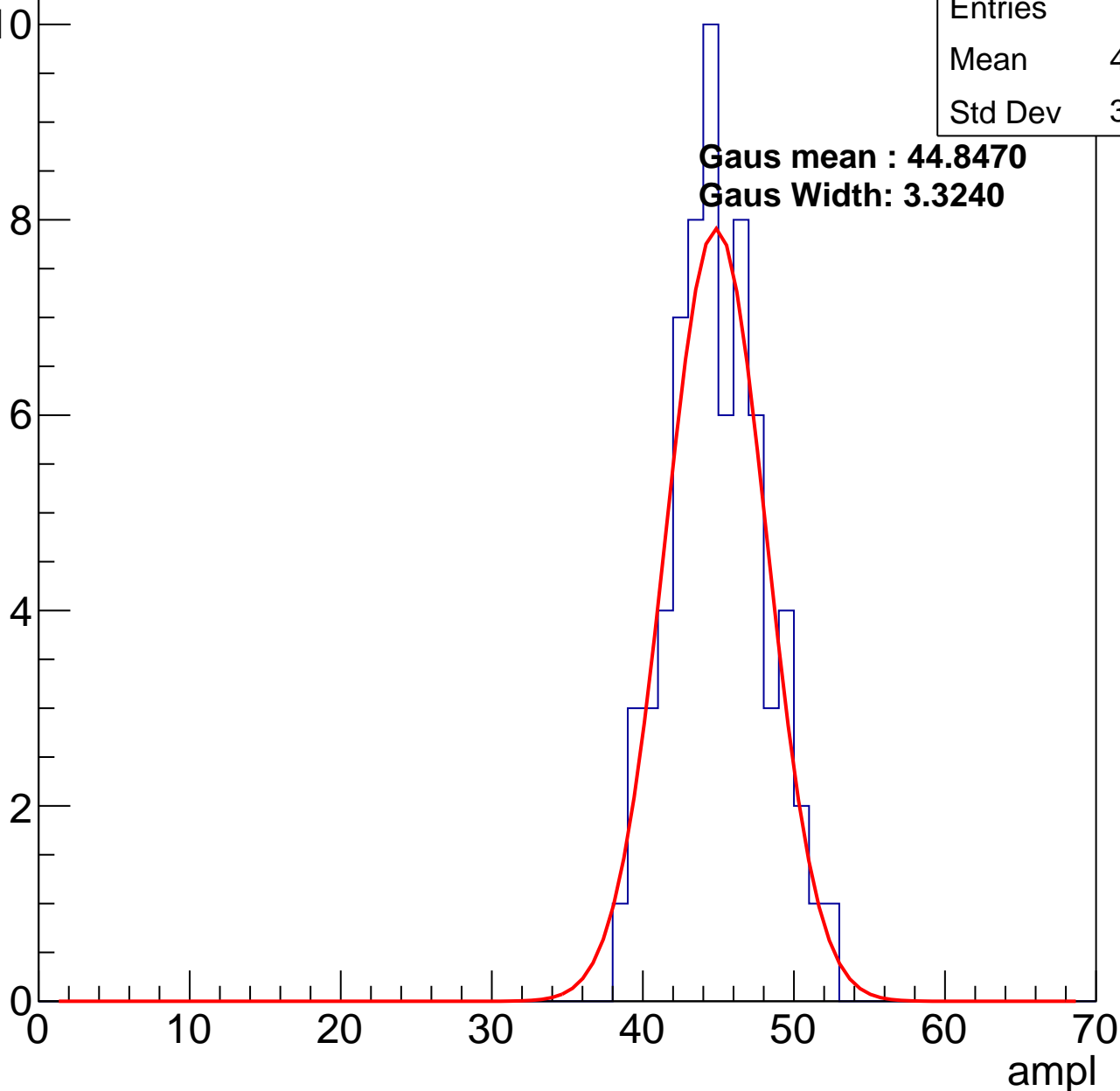
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	44.48
Std Dev	3.092

**Gaus mean : 44.8470**

**Gaus Width: 3.3240**

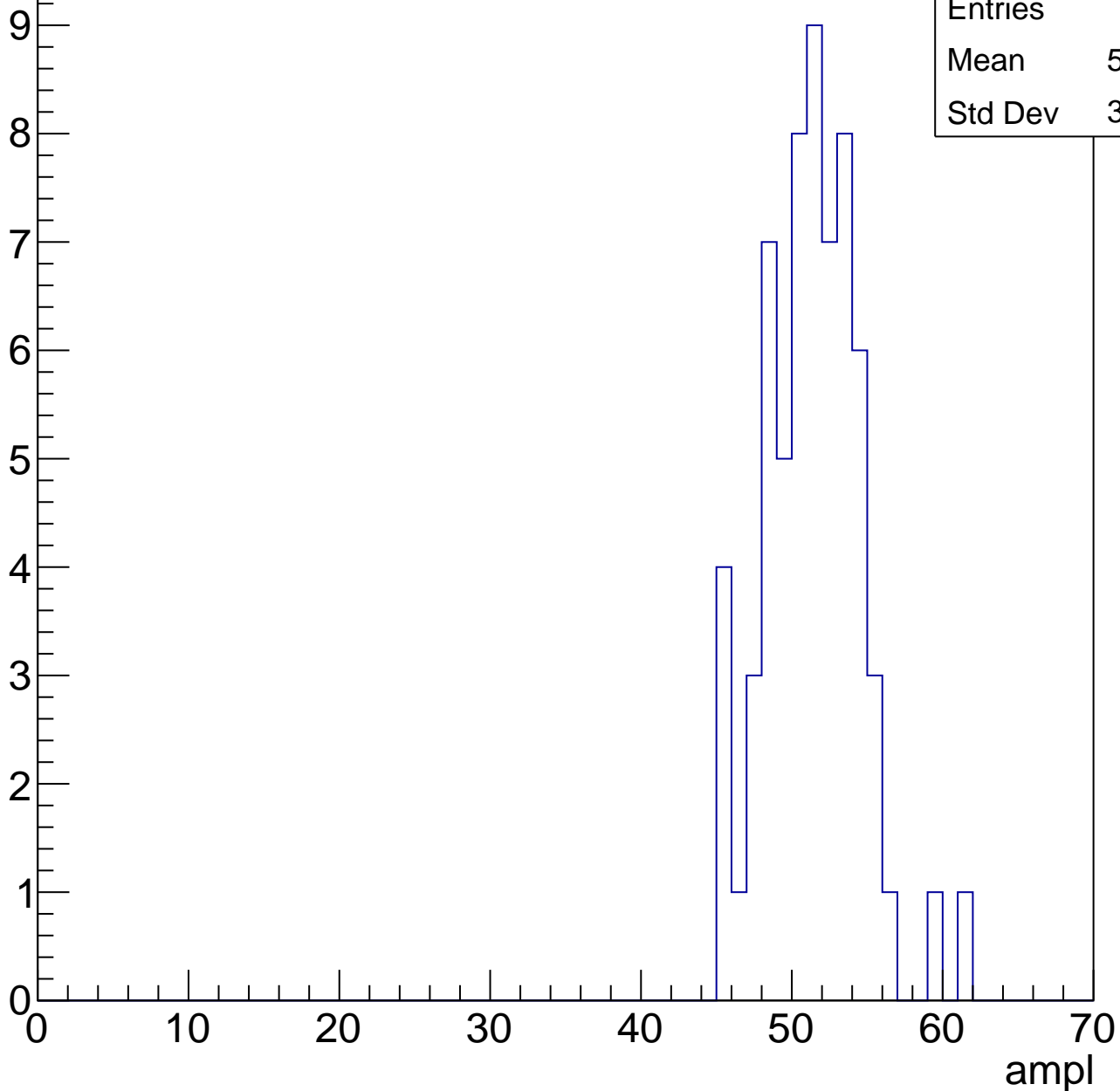


# B0L001S, U17-ch29, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

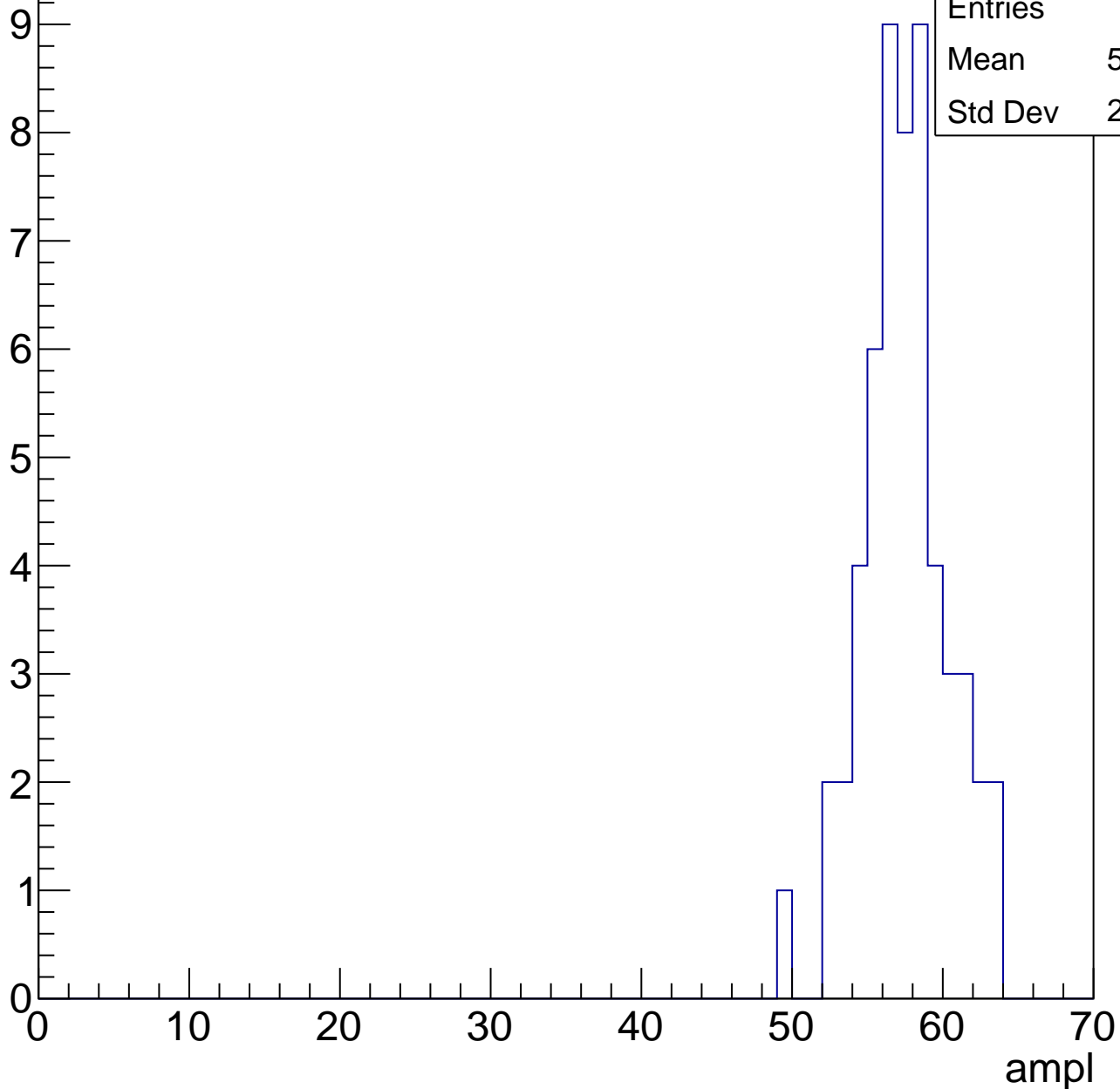
Entries	64
Mean	50.94
Std Dev	3.157



# B0L001S, U17-ch29, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

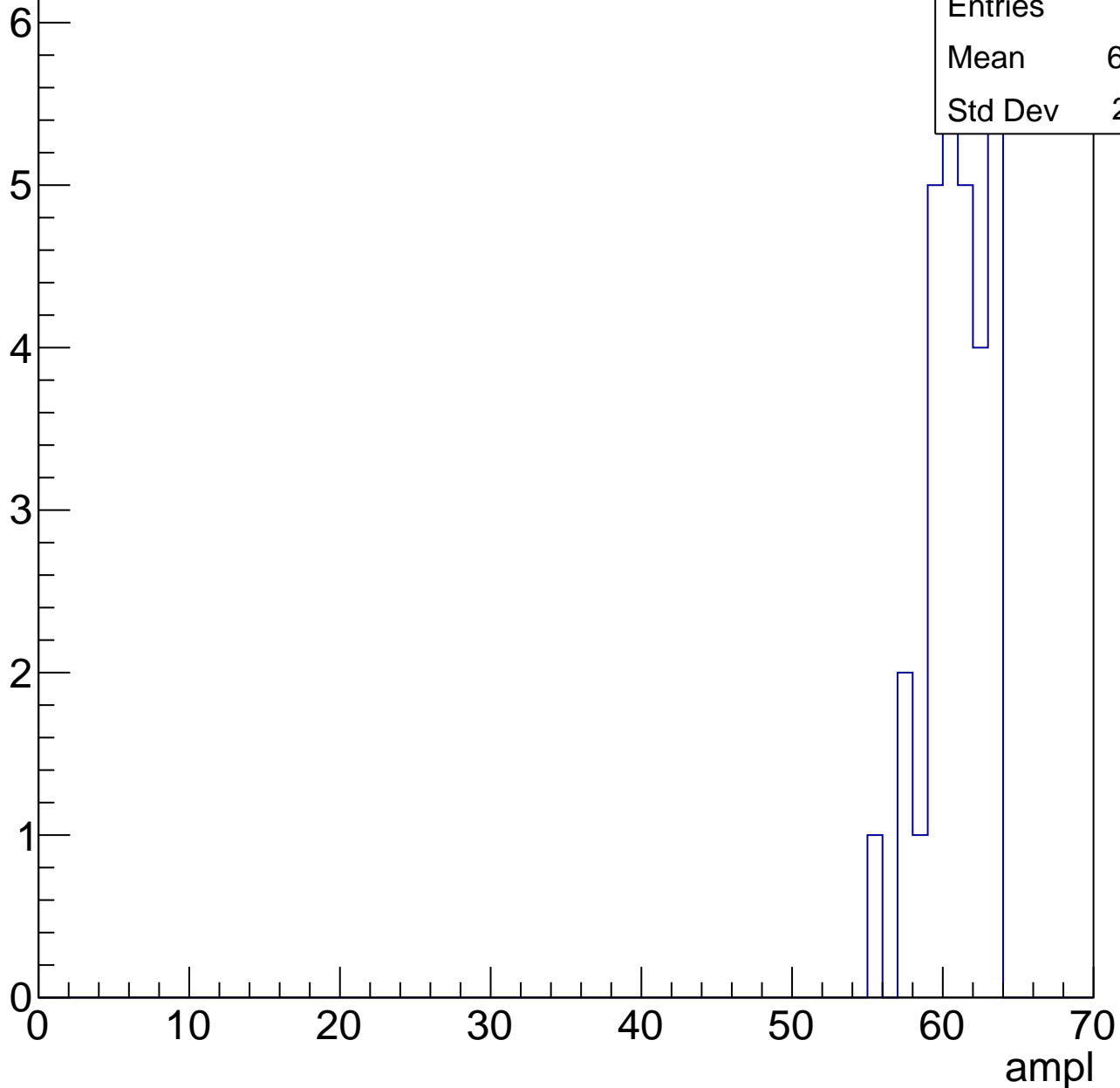


Entries	55
Mean	57.02
Std Dev	2.819

# B0L001S, U17-ch29, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

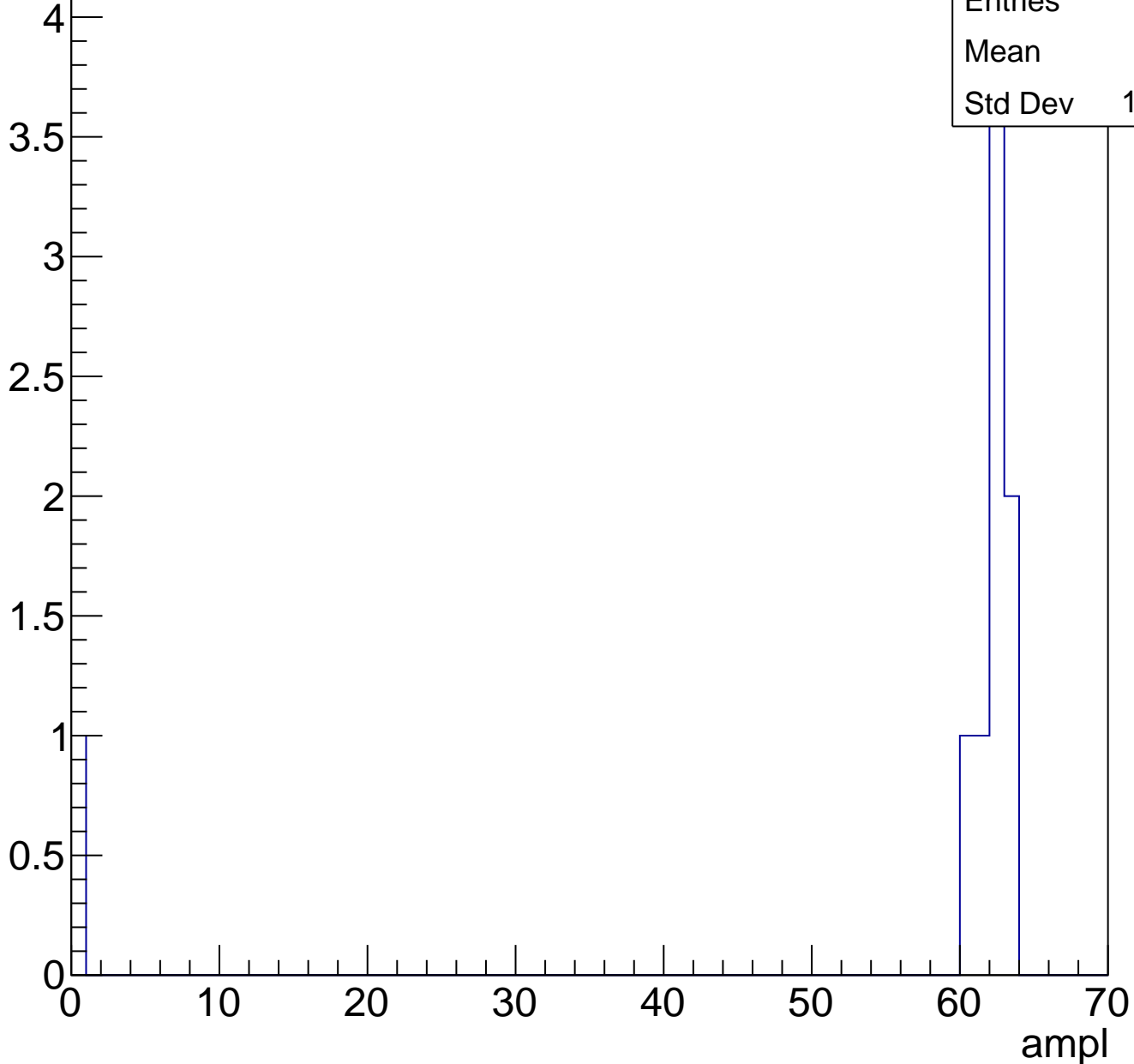
Entry



# B0L001S, U17-ch29, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	9
Mean	55
Std Dev	19.47



# B0L001S, U17-ch29, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U17-ch30, adc0

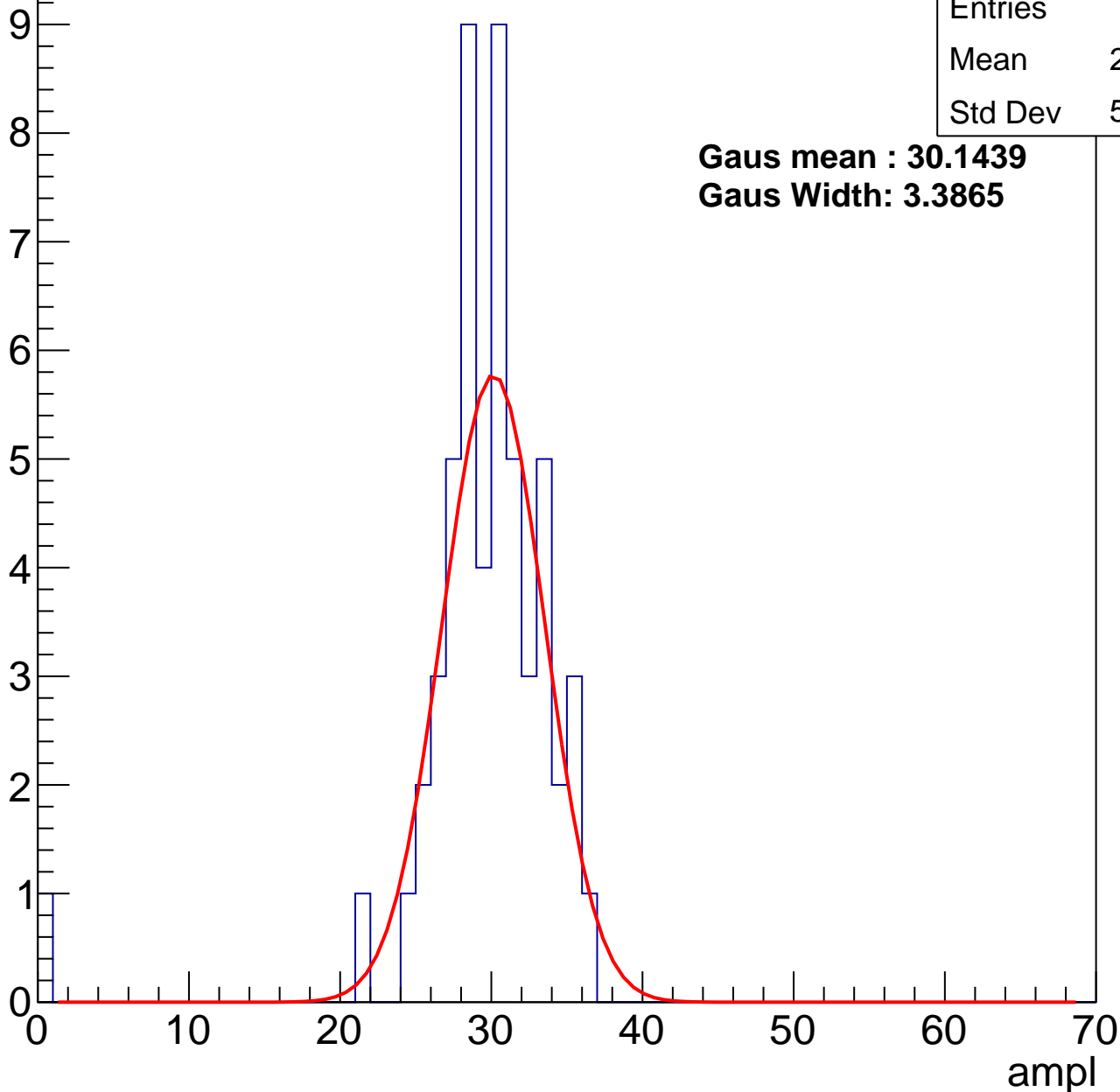
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	29.09
Std Dev	5.019

**Gaus mean : 30.1439**

**Gaus Width: 3.3865**



# B0L001S, U17-ch30, adc1

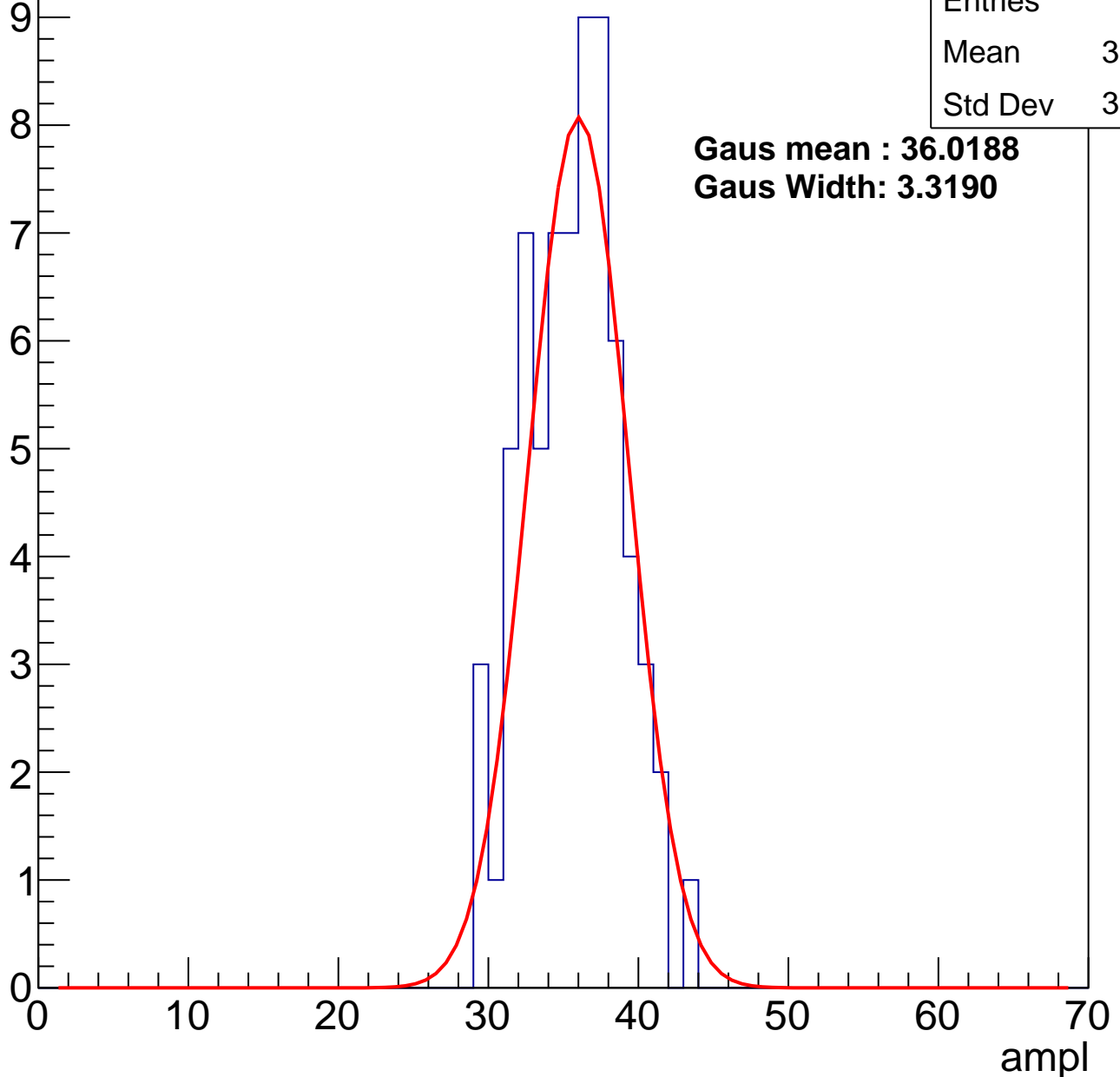
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	35.22
Std Dev	3.125

**Gaus mean : 36.0188**

**Gaus Width: 3.3190**



# B0L001S, U17-ch30, adc2

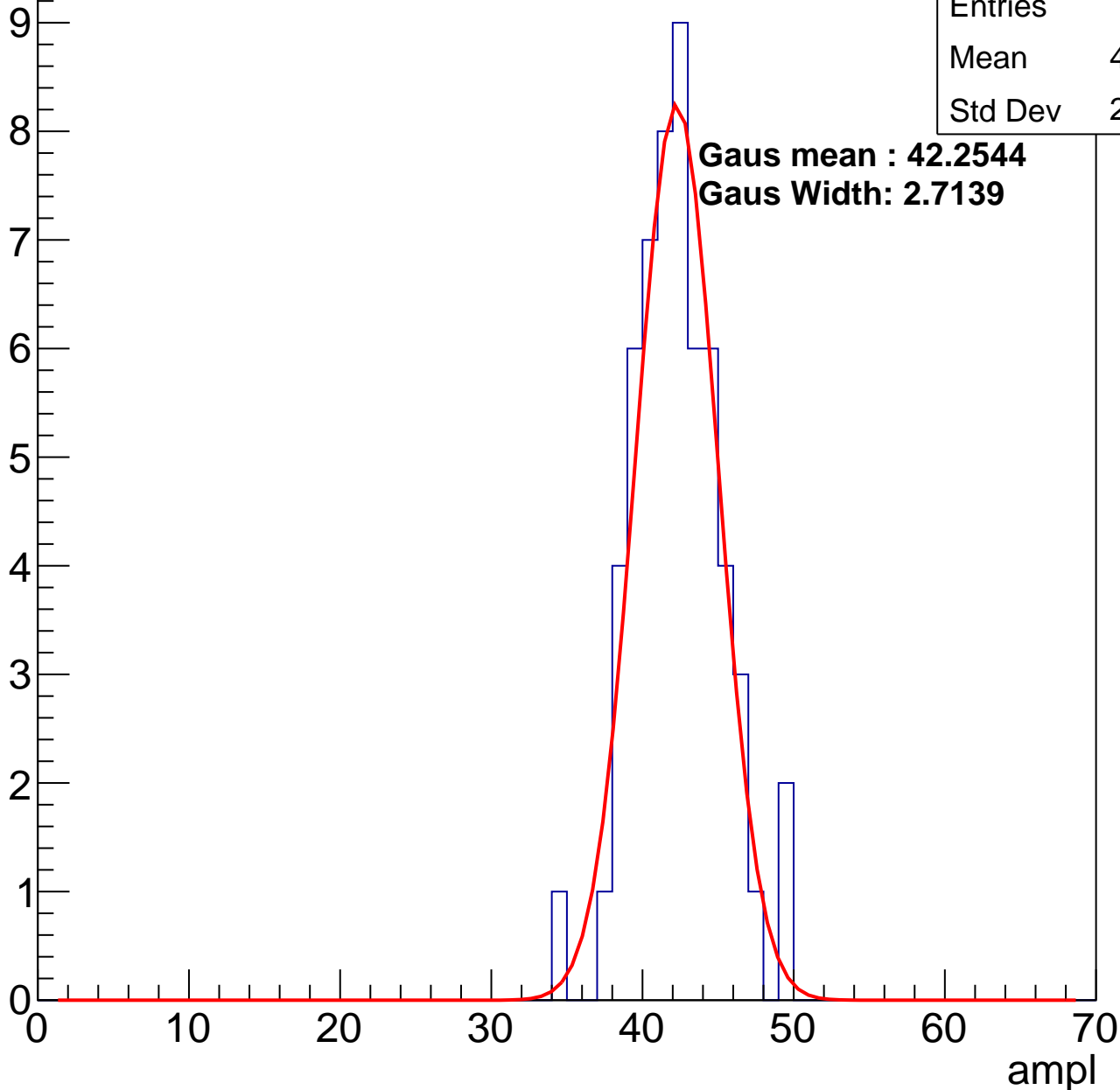
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	41.86
Std Dev	2.873

**Gaus mean : 42.2544**

**Gaus Width: 2.7139**

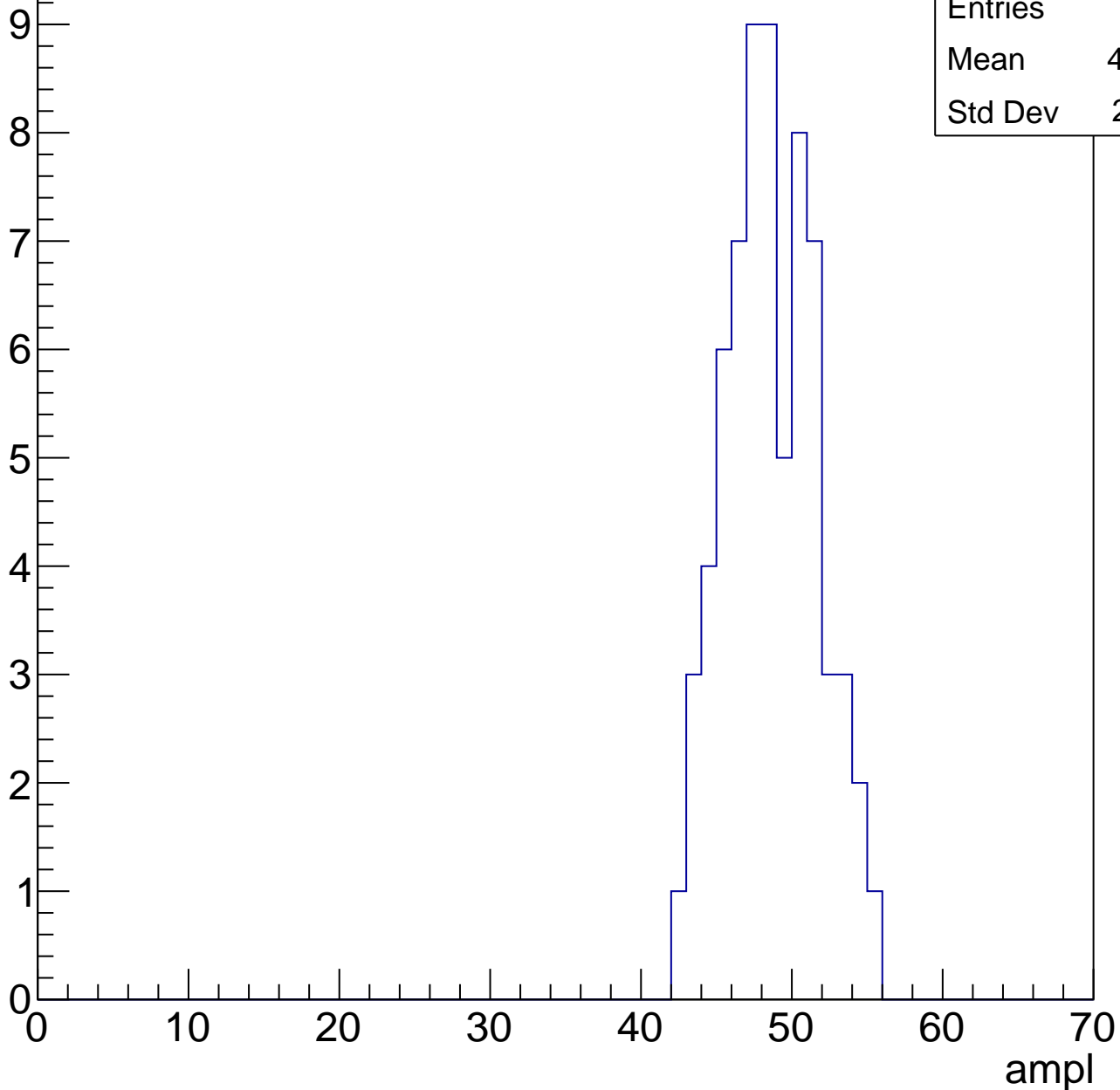


# B0L001S, U17-ch30, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	48.15
Std Dev	2.991

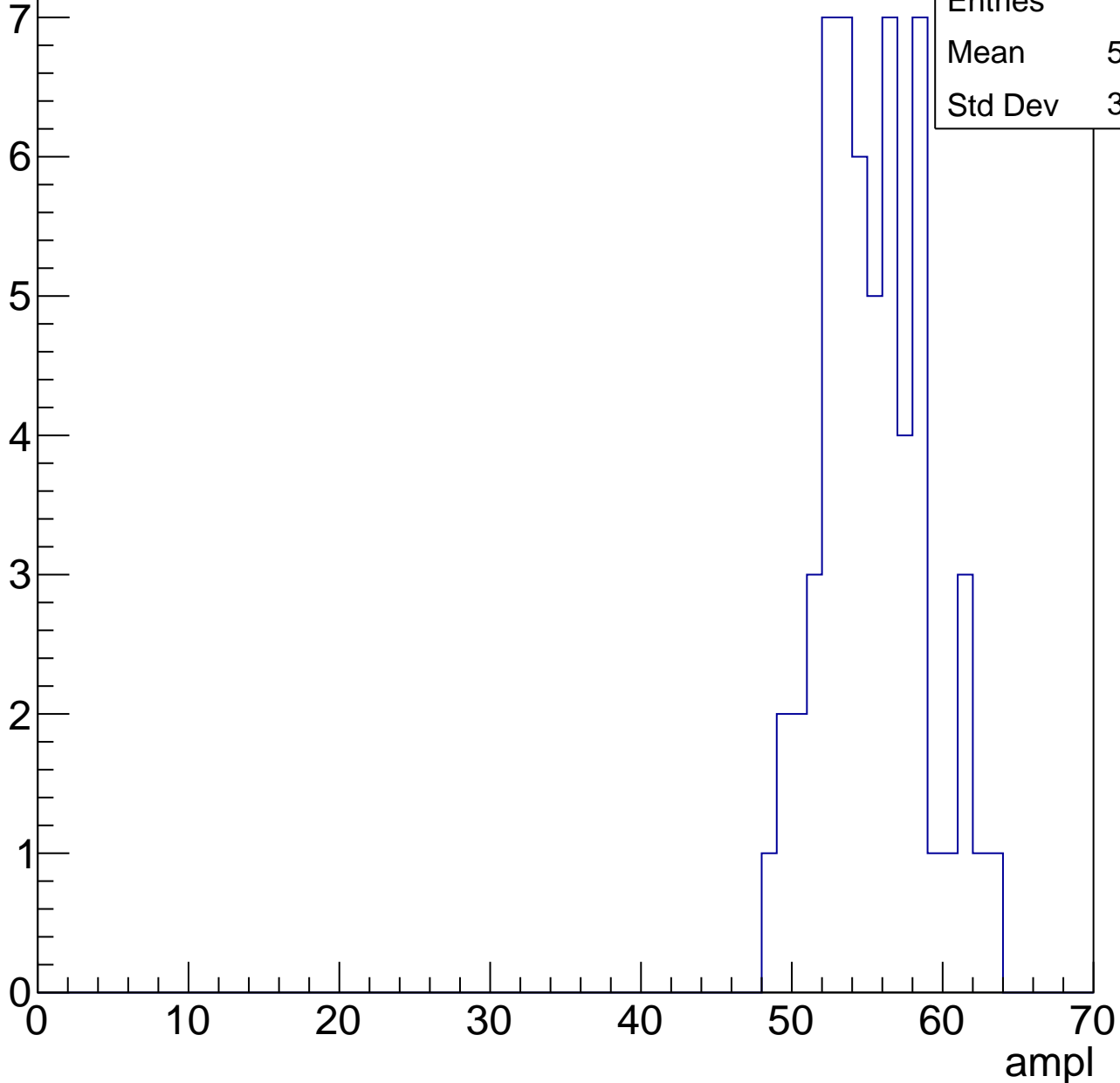


# B0L001S, U17-ch30, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	54.93
Std Dev	3.383

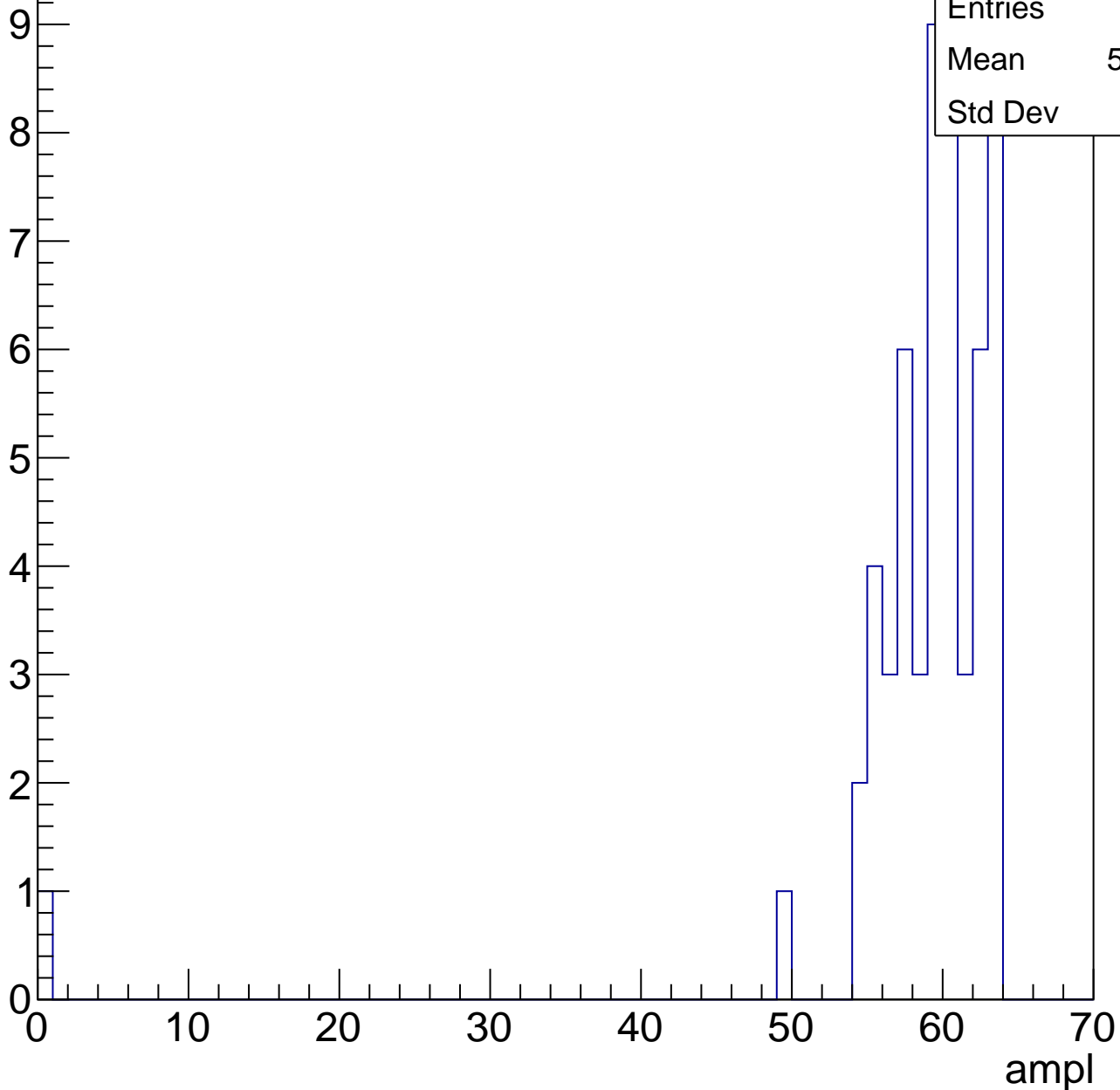


# B0L001S, U17-ch30, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

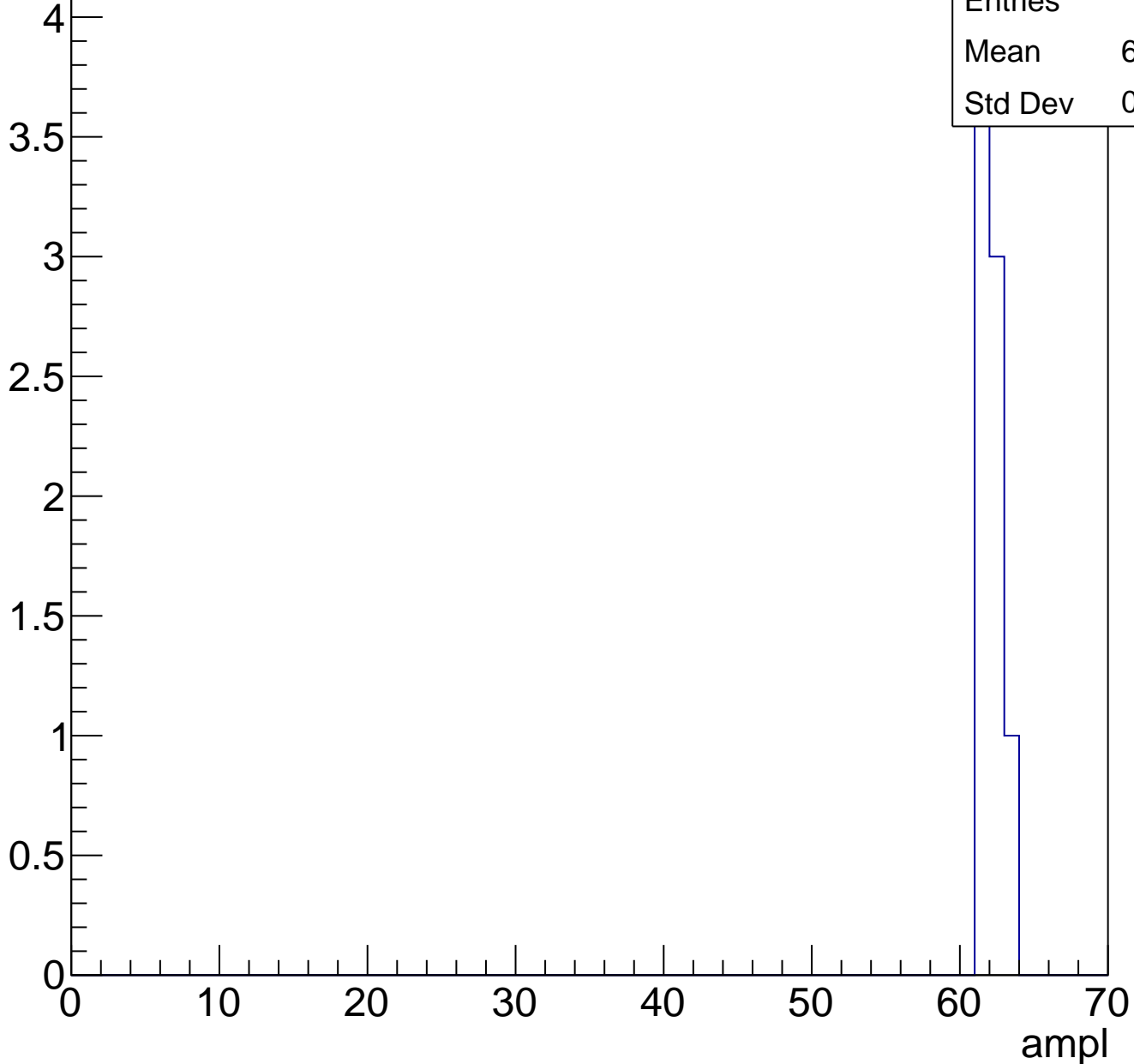
Entries	55
Mean	58.02
Std Dev	8.42



# B0L001S, U17-ch30, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch30, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U17-ch31, adc0

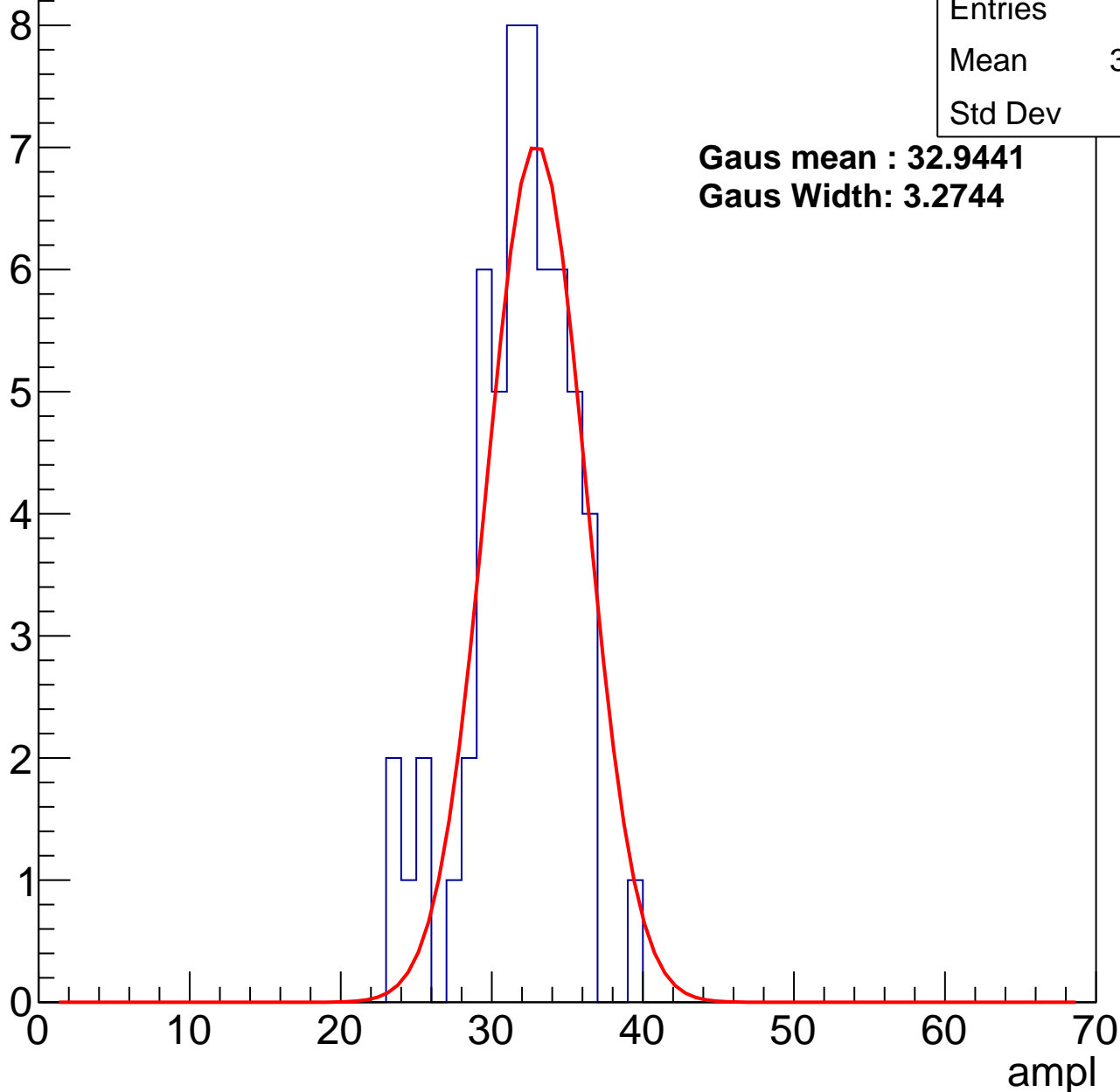
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	31.42
Std Dev	3.33

**Gaus mean : 32.9441**

**Gaus Width: 3.2744**



# B0L001S, U17-ch31, adc1

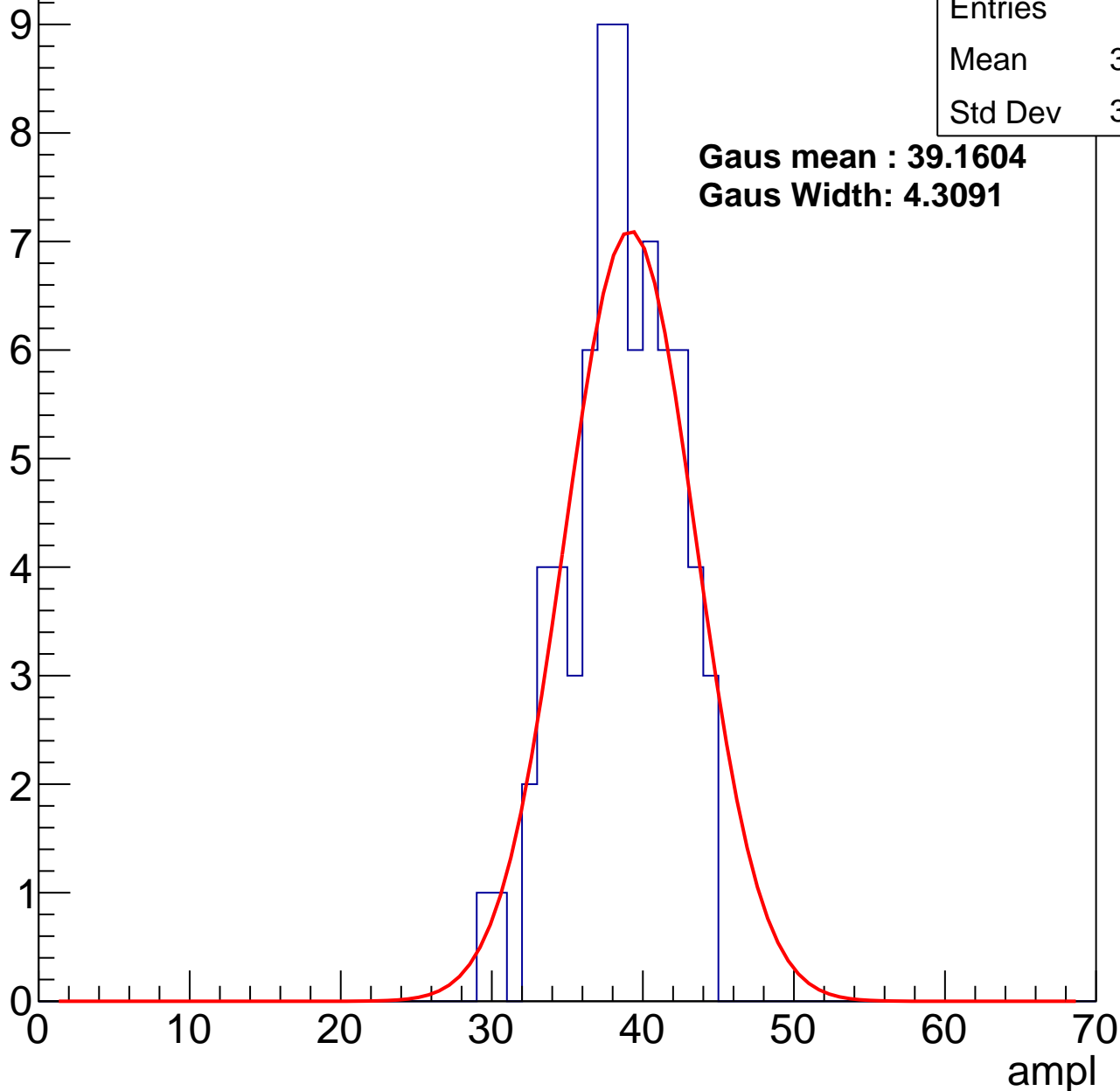
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	38.07
Std Dev	3.425

**Gaus mean : 39.1604**

**Gaus Width: 4.3091**



# B0L001S, U17-ch31, adc2

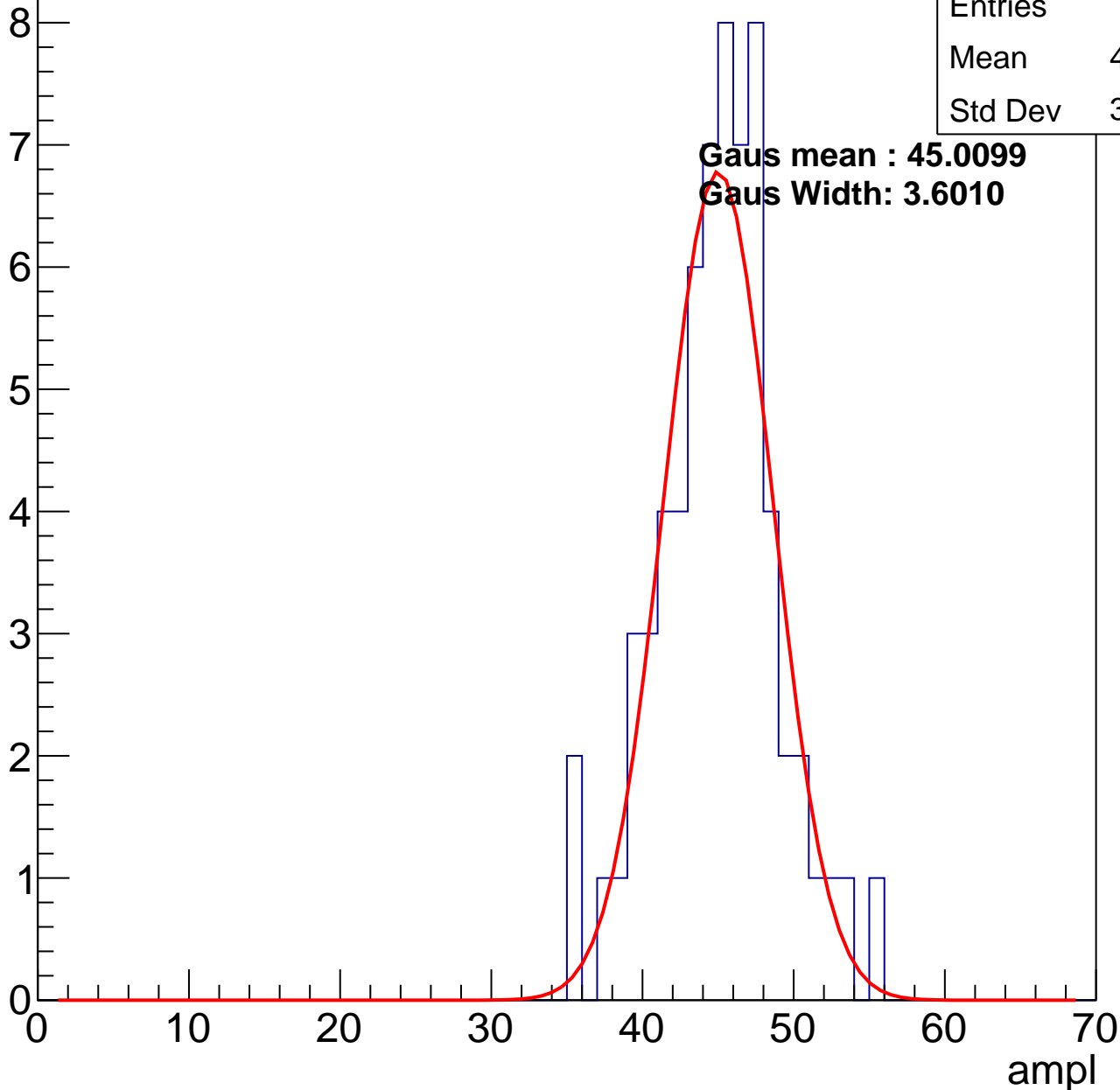
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	44.53
Std Dev	3.928

**Gaus mean : 45.0099**

**Gaus Width: 3.6010**

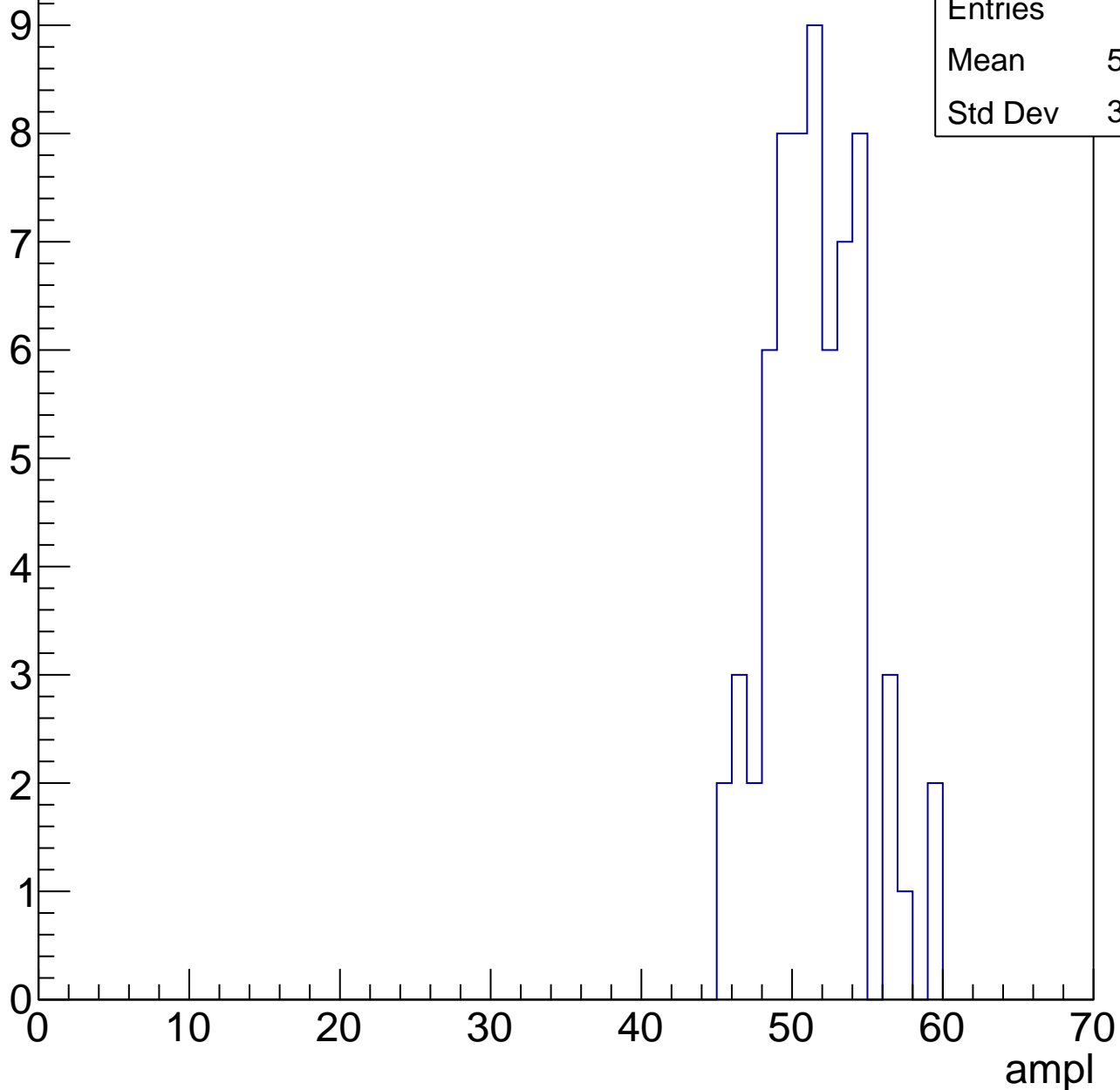


# B0L001S, U17-ch31, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	51.06
Std Dev	3.083

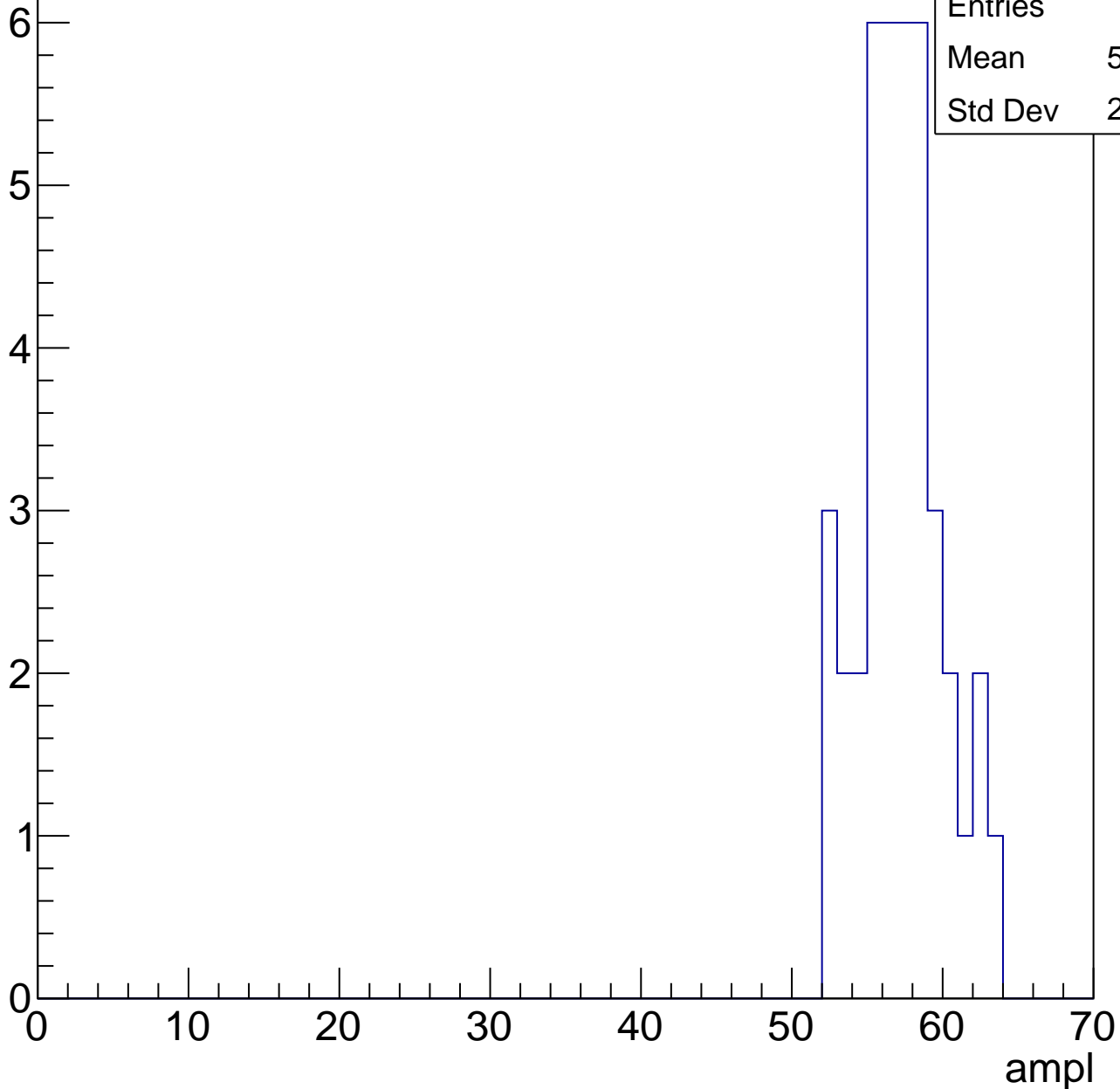


# B0L001S, U17-ch31, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

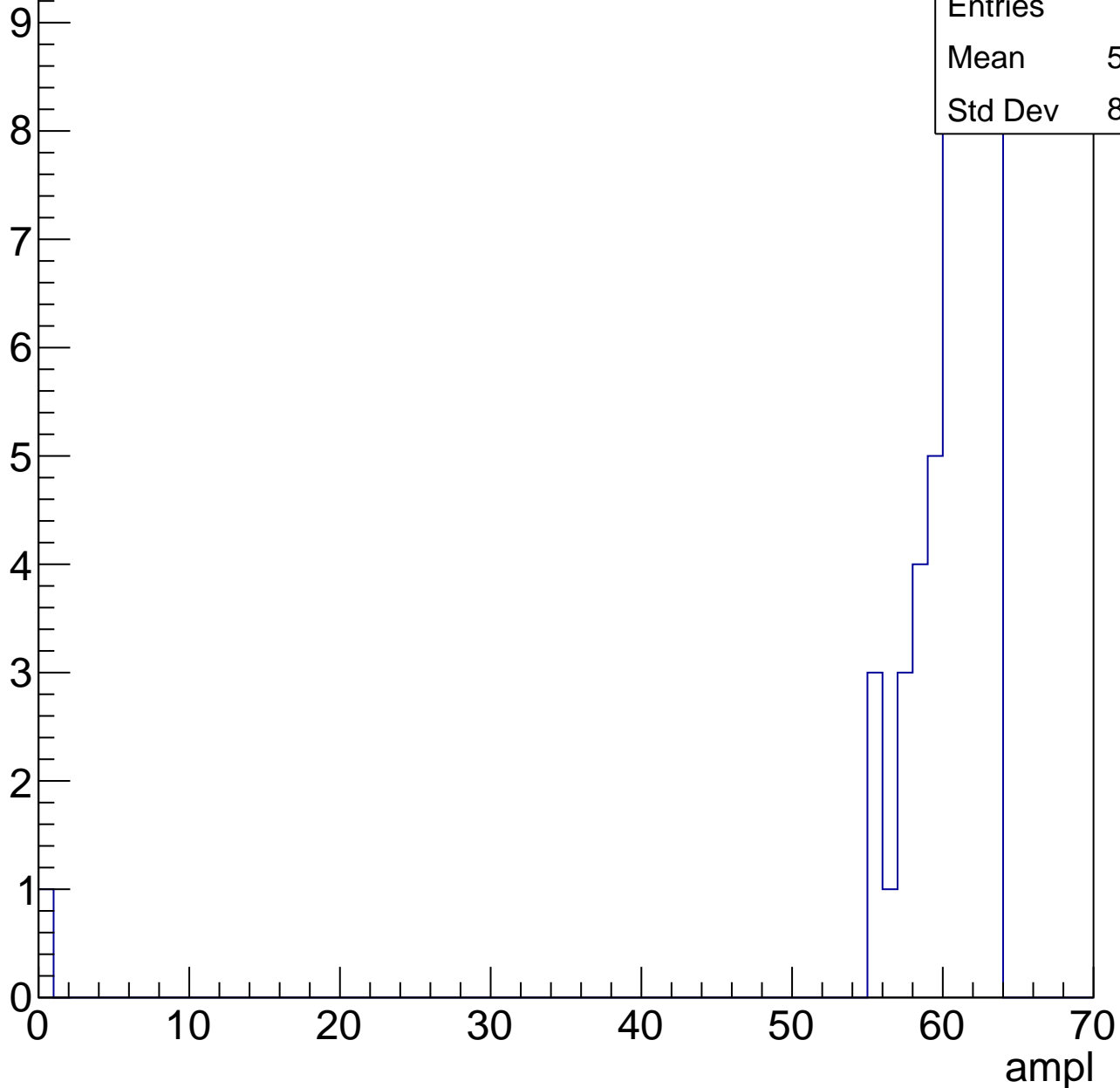
Entries	40
Mean	56.77
Std Dev	2.697



# B0L001S, U17-ch31, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U17-ch31, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch31, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U17-ch32, adc0

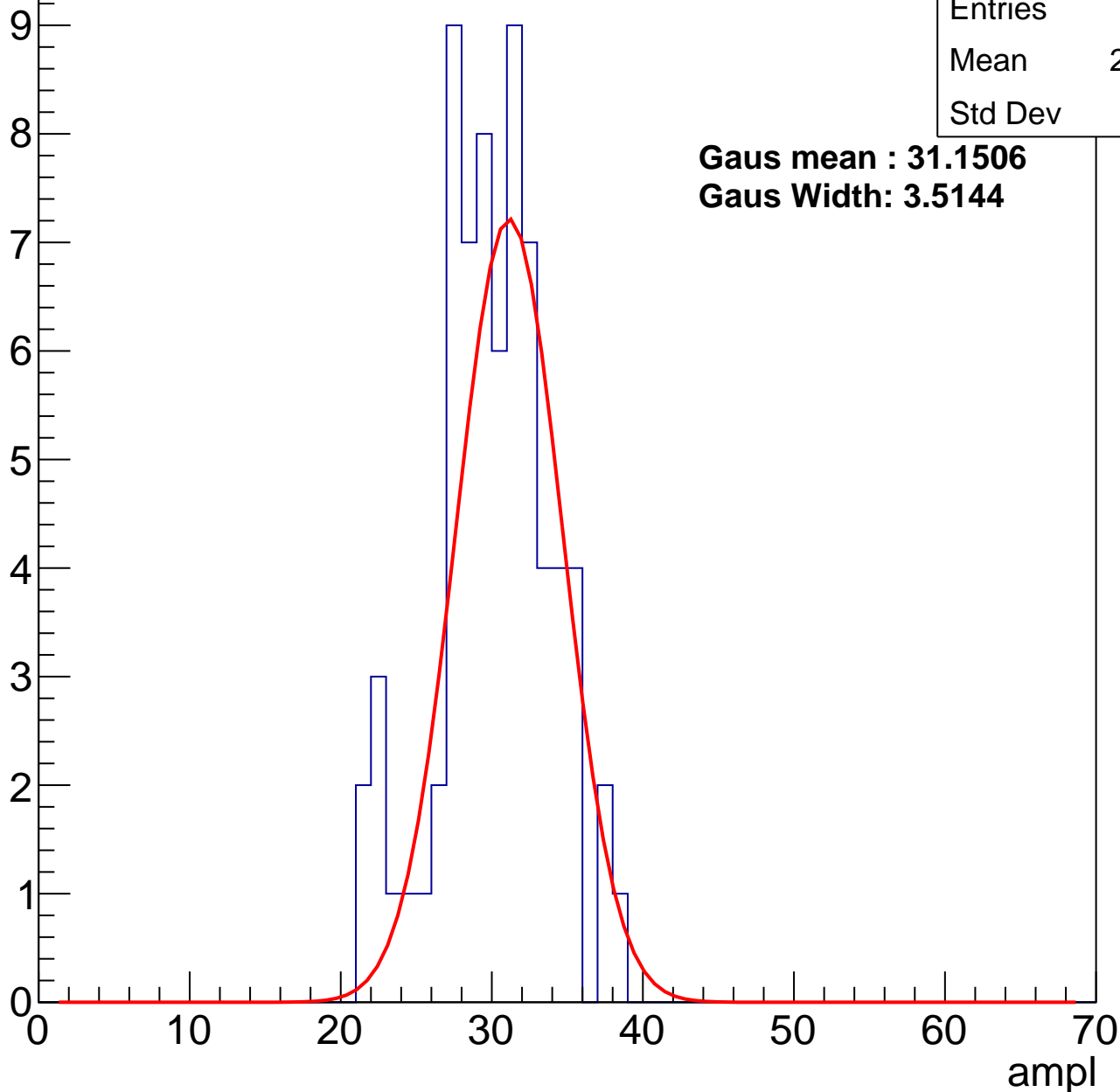
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	29.66
Std Dev	3.76

**Gaus mean : 31.1506**

**Gaus Width: 3.5144**



# B0L001S, U17-ch32, adc1

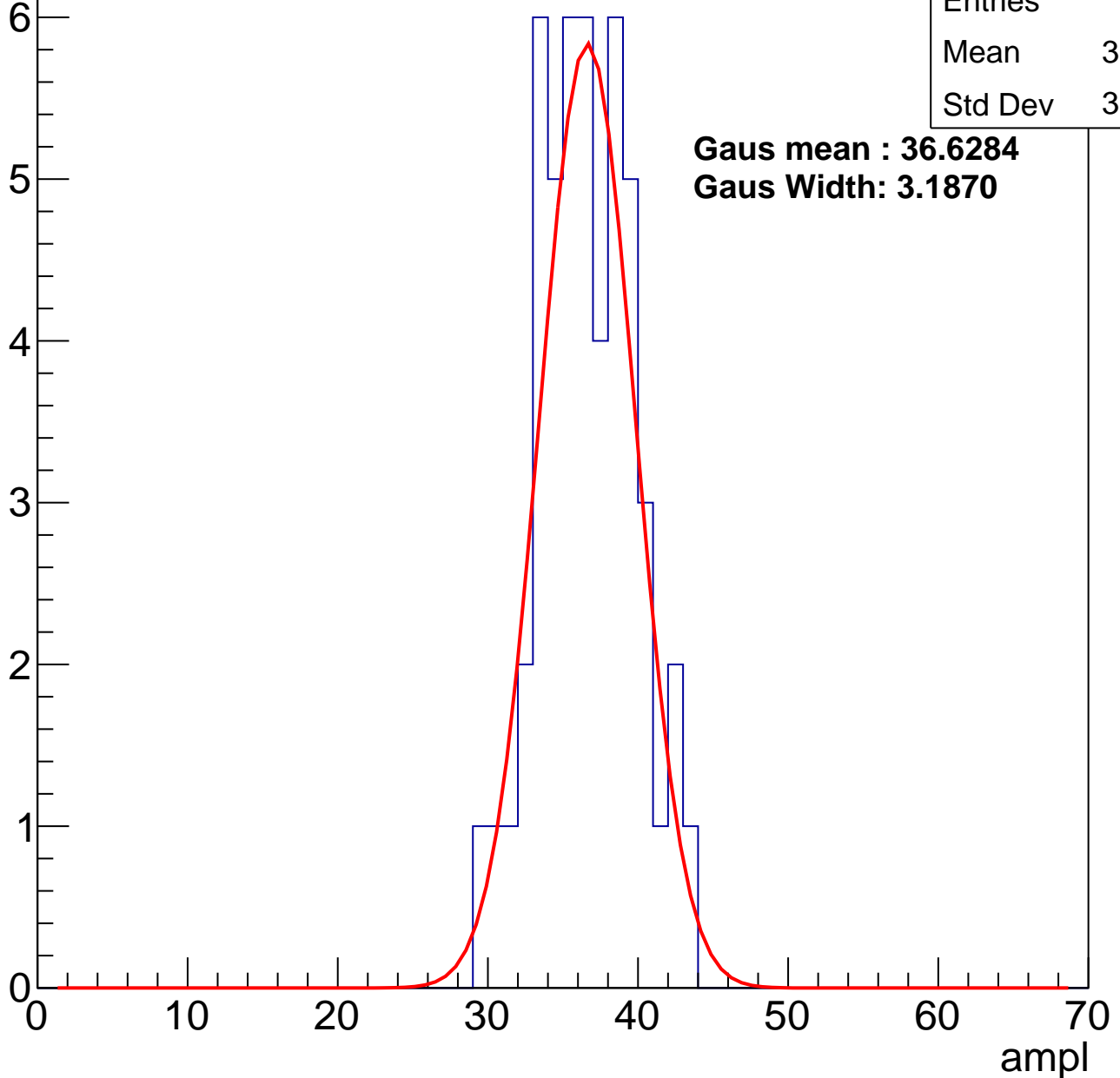
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	50
Mean	36.14
Std Dev	3.124

**Gaus mean : 36.6284**

**Gaus Width: 3.1870**



# B0L001S, U17-ch32, adc2

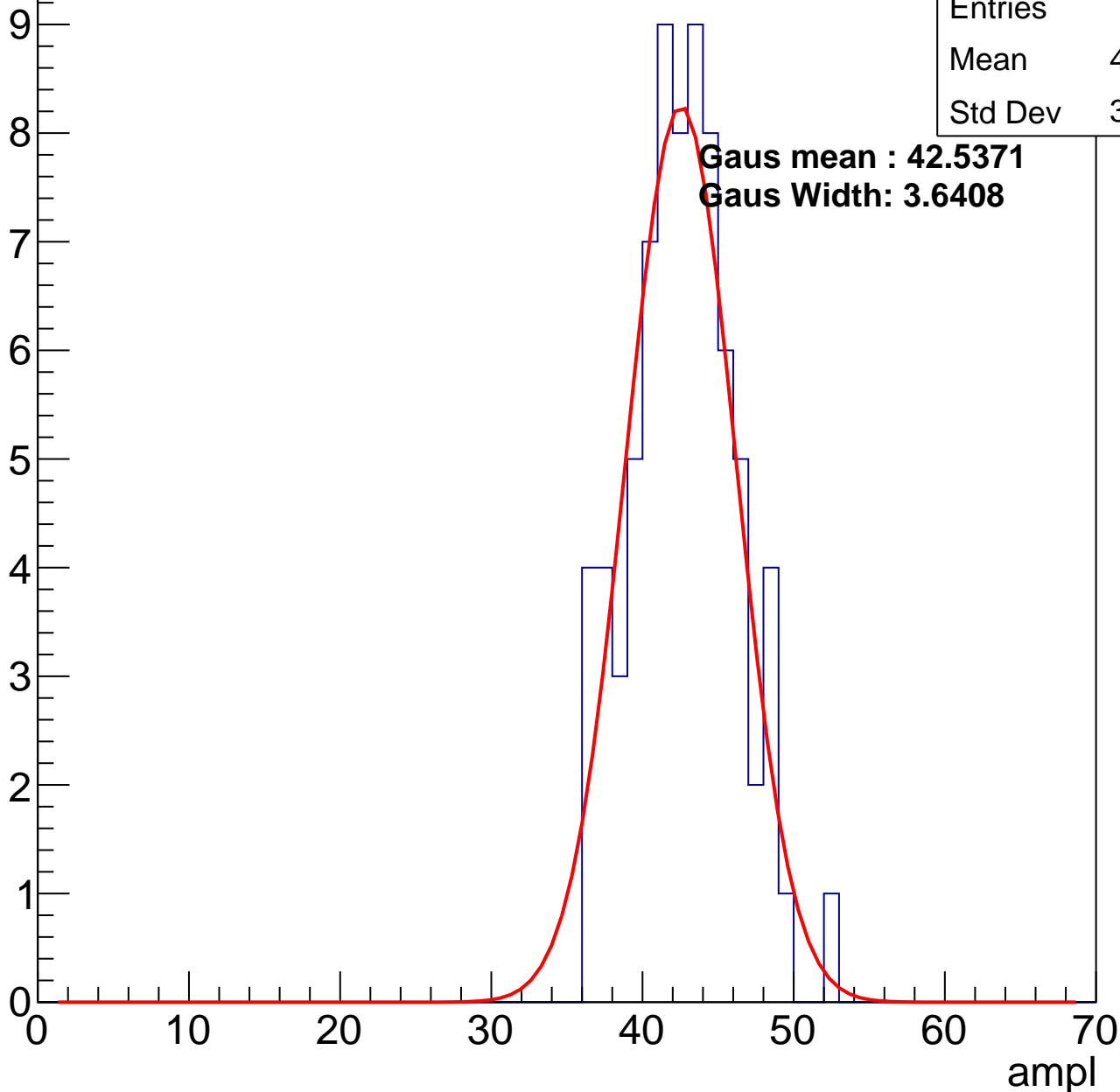
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	76
Mean	42.26
Std Dev	3.416

**Gaus mean : 42.5371**

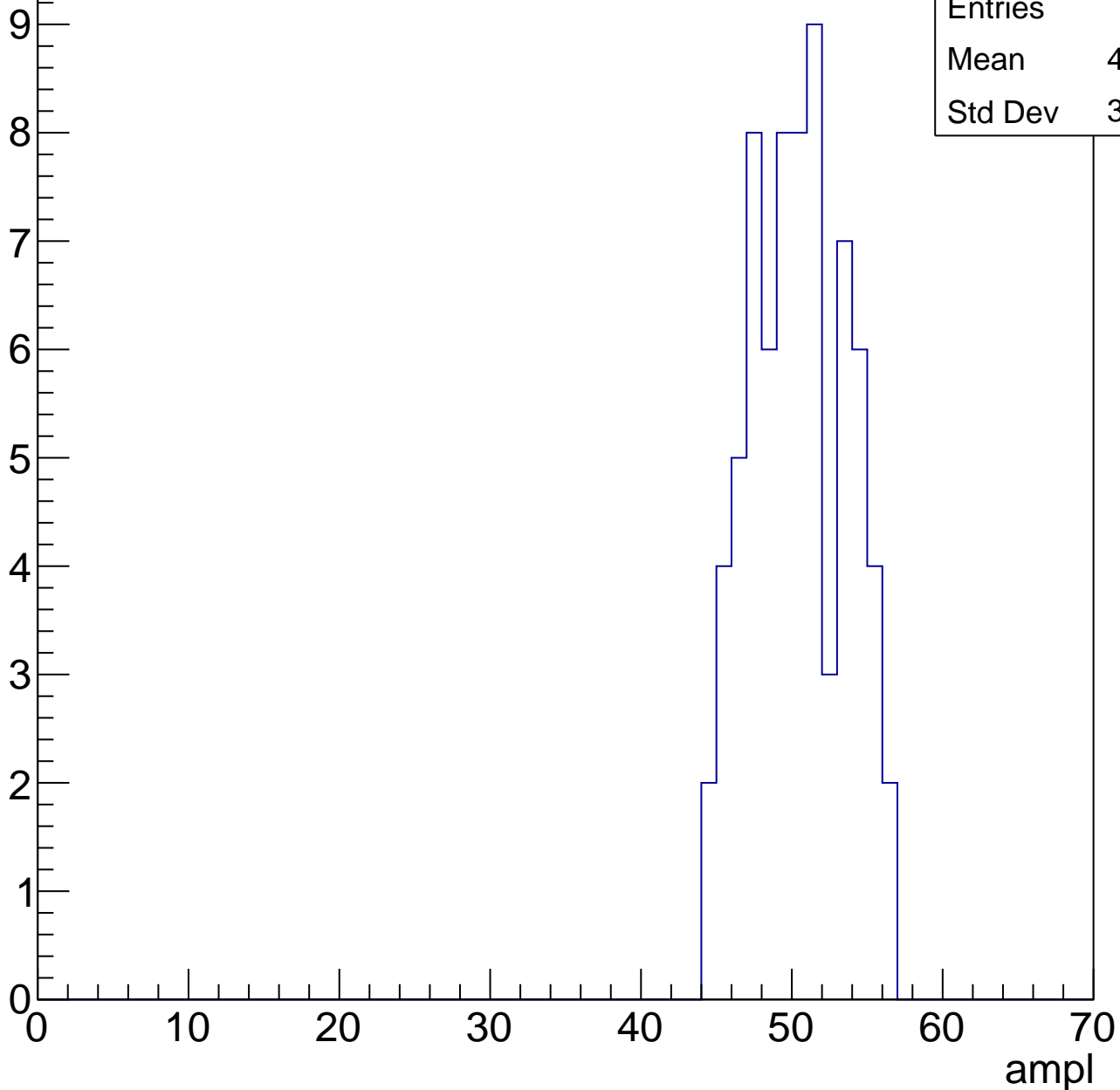
**Gaus Width: 3.6408**



# B0L001S, U17-ch32, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



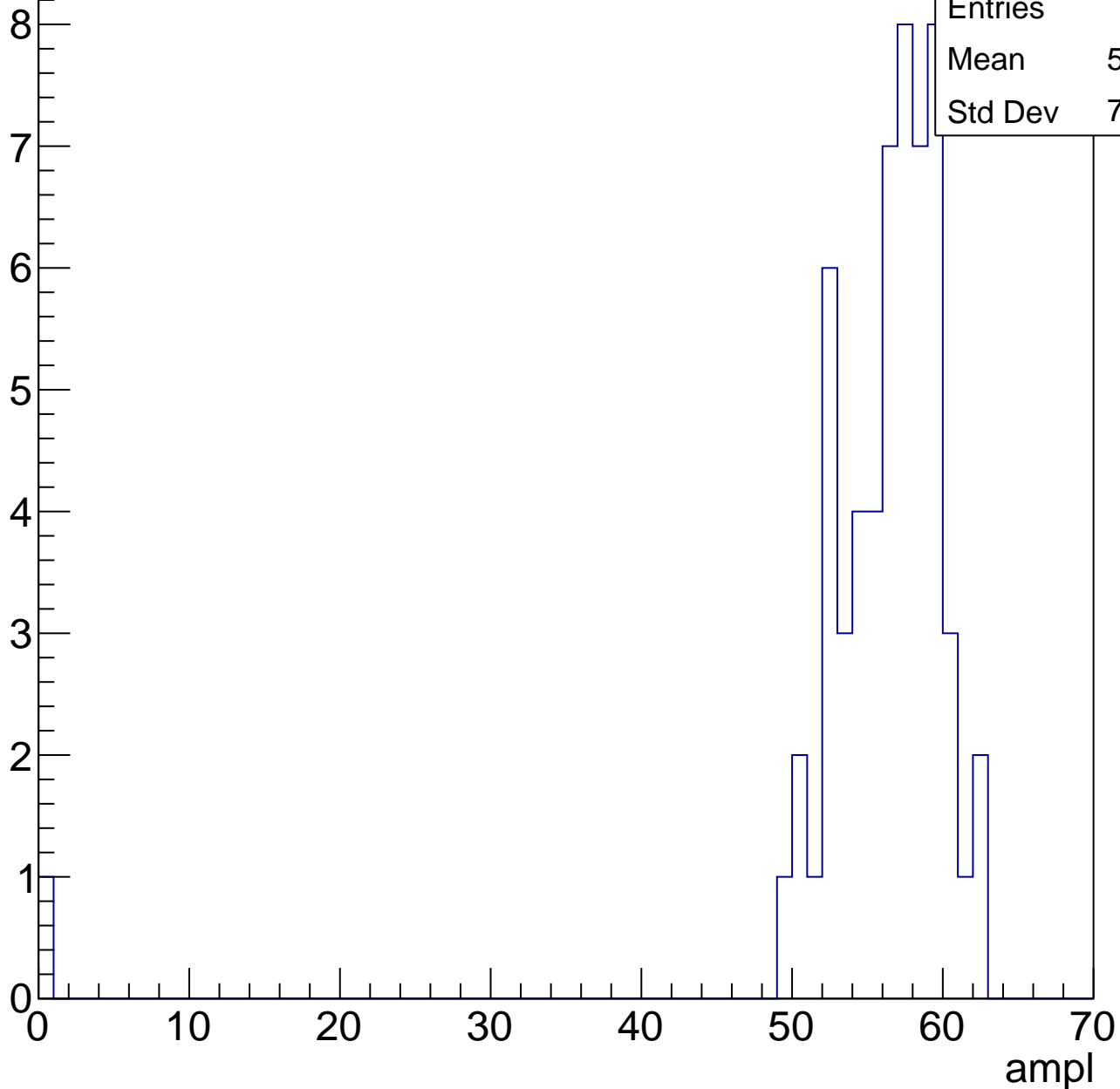
Entries	72
Mean	49.94
Std Dev	3.135

# B0L001S, U17-ch32, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

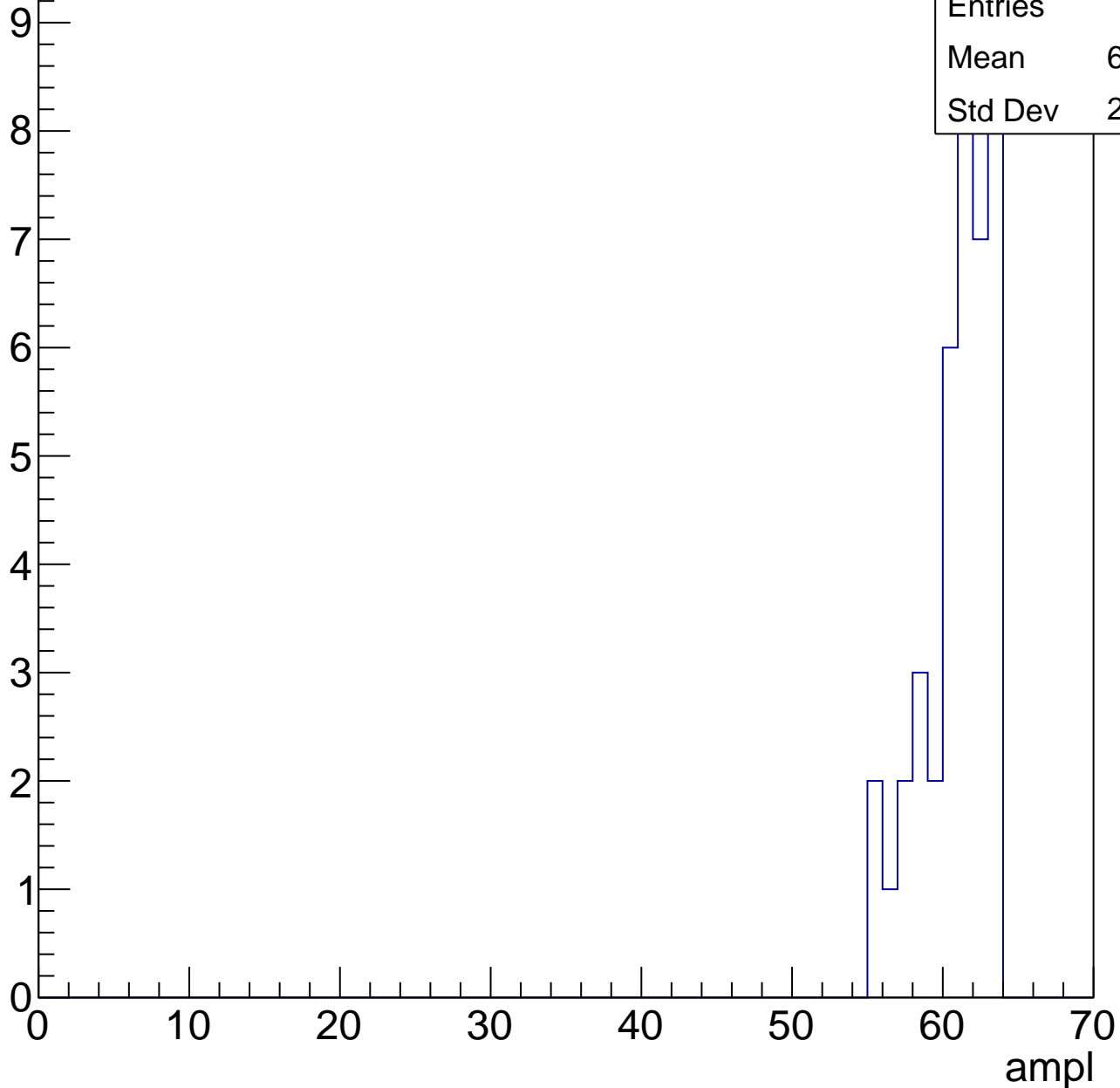
Entries	58
Mean	55.14
Std Dev	7.916



# B0L001S, U17-ch32, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	41
Mean	60.54
Std Dev	2.232

# B0L001S, U17-ch32, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch32, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U17-ch33, adc0

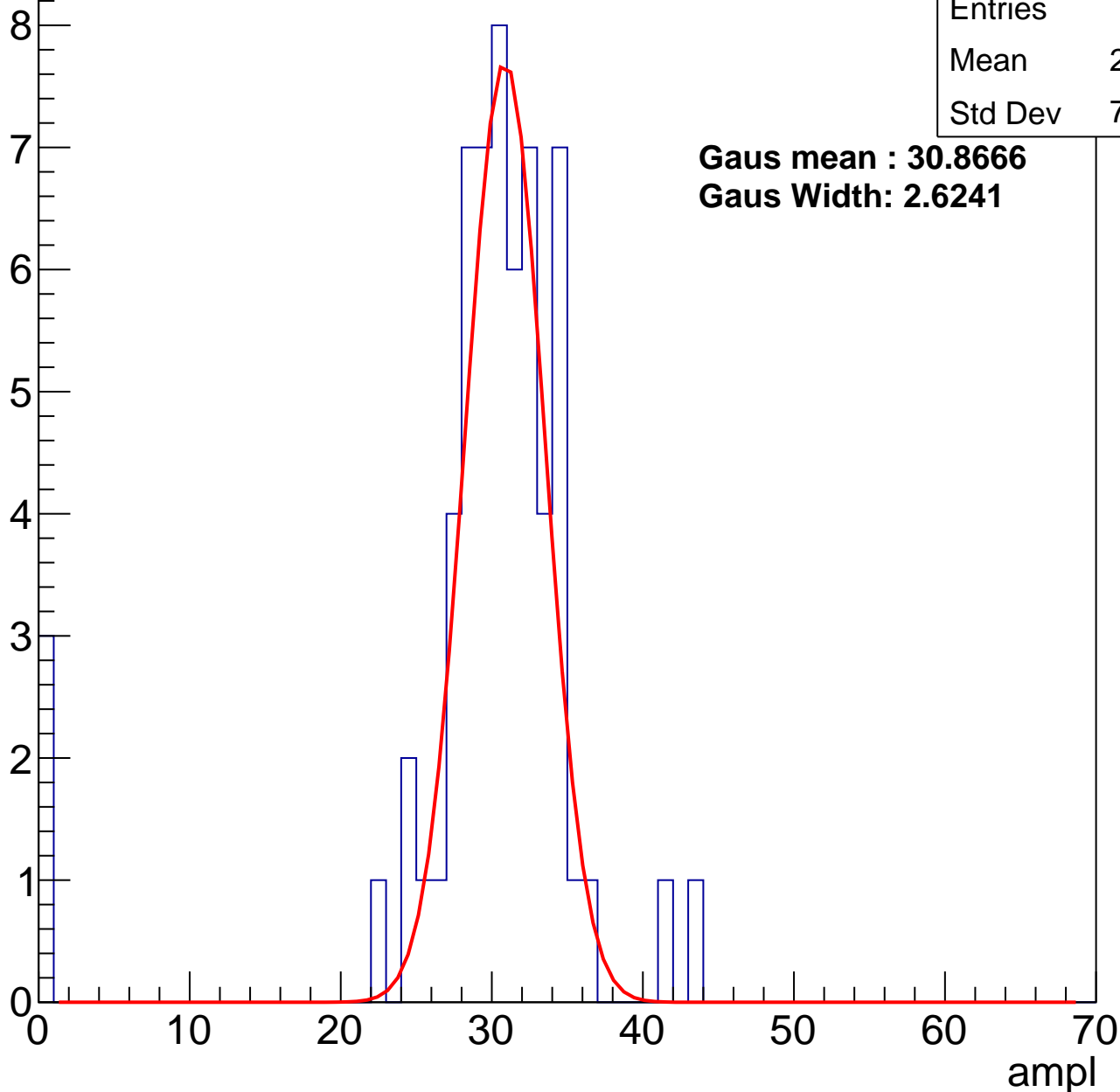
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	29.08
Std Dev	7.436

**Gaus mean : 30.8666**

**Gaus Width: 2.6241**

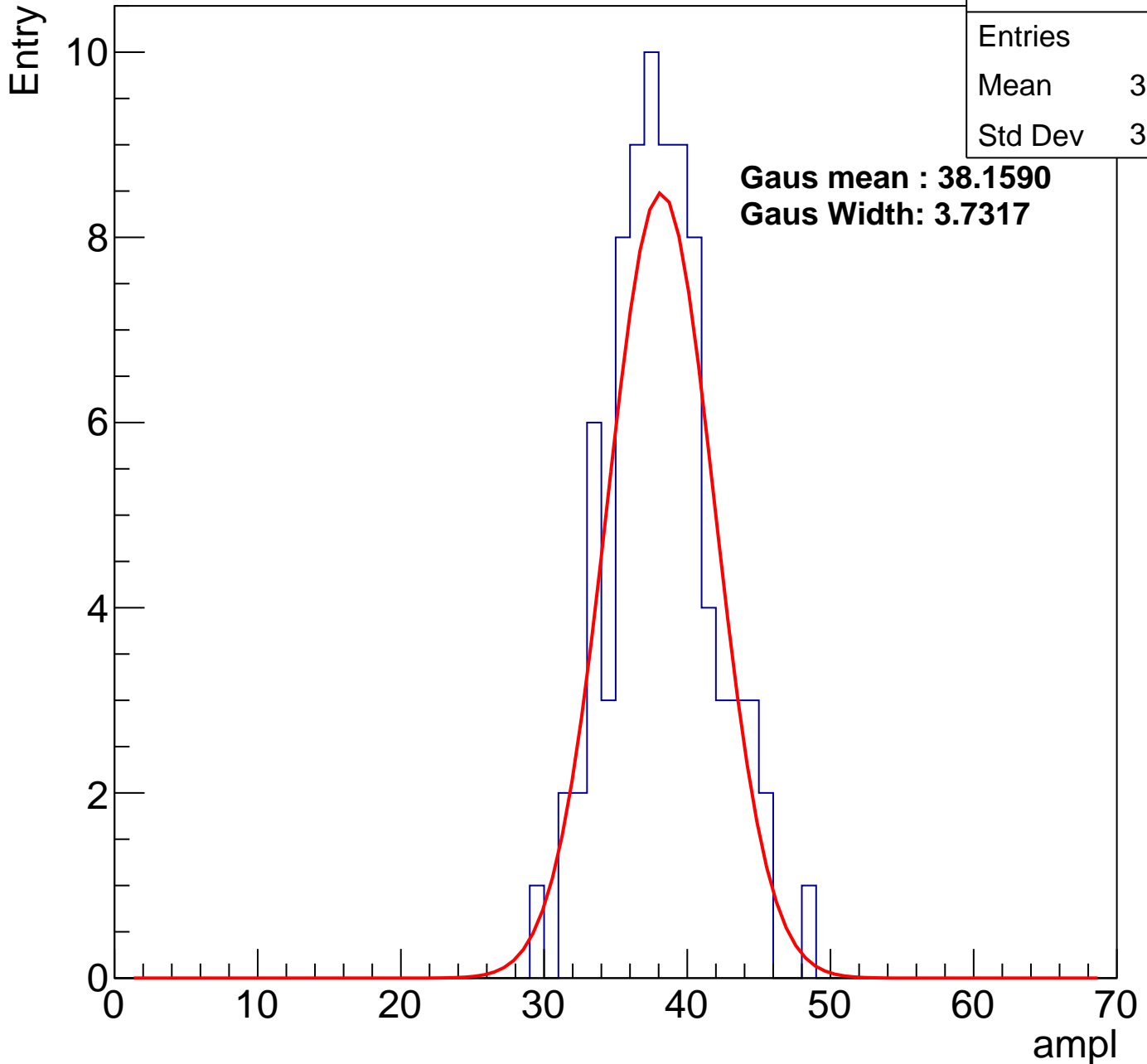


# B0L001S, U17-ch33, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	83
Mean	37.72
Std Dev	3.585

**Gaus mean : 38.1590**  
**Gaus Width: 3.7317**



# B0L001S, U17-ch33, adc2

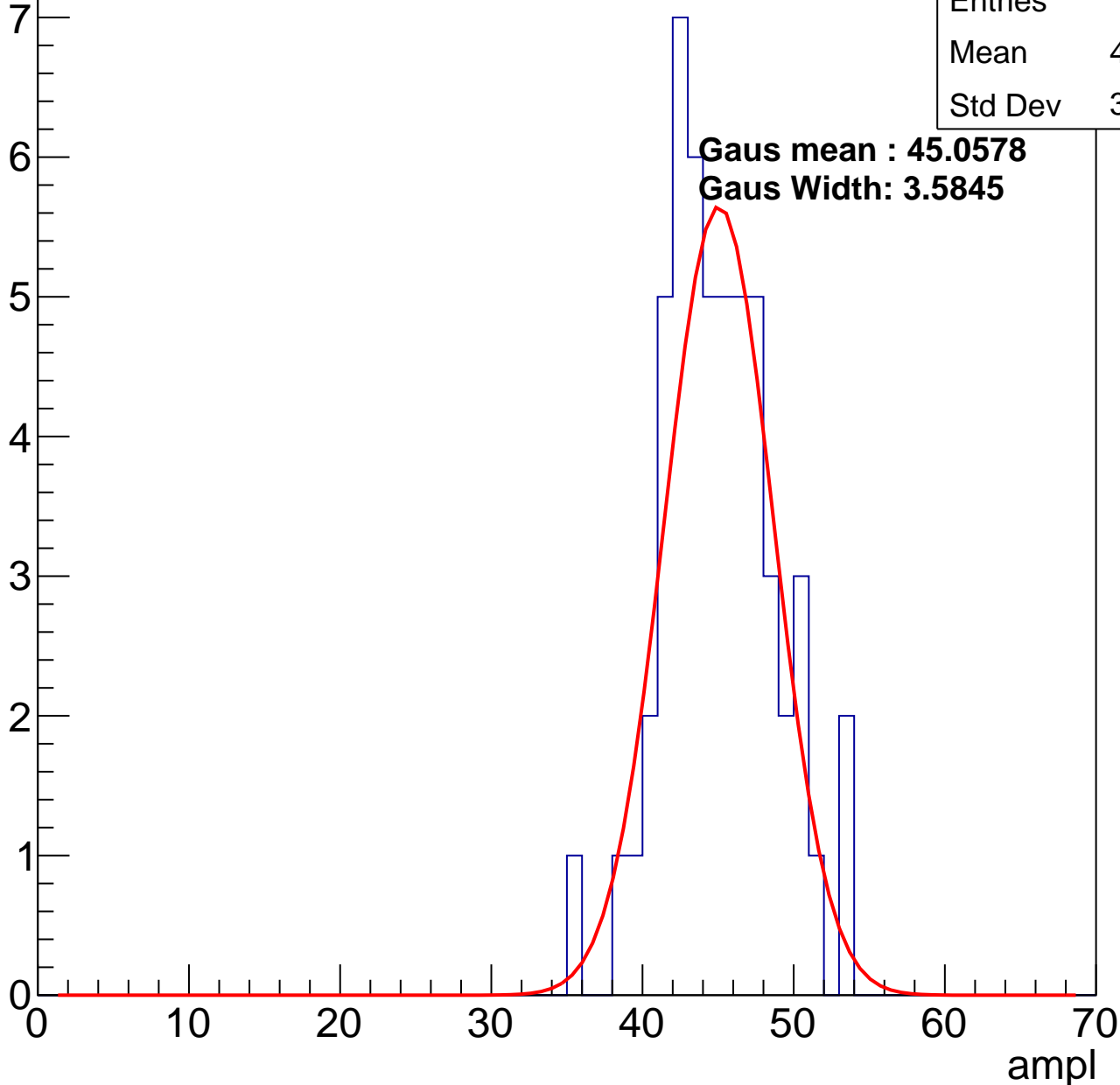
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	44.59
Std Dev	3.654

**Gaus mean : 45.0578**

**Gaus Width: 3.5845**

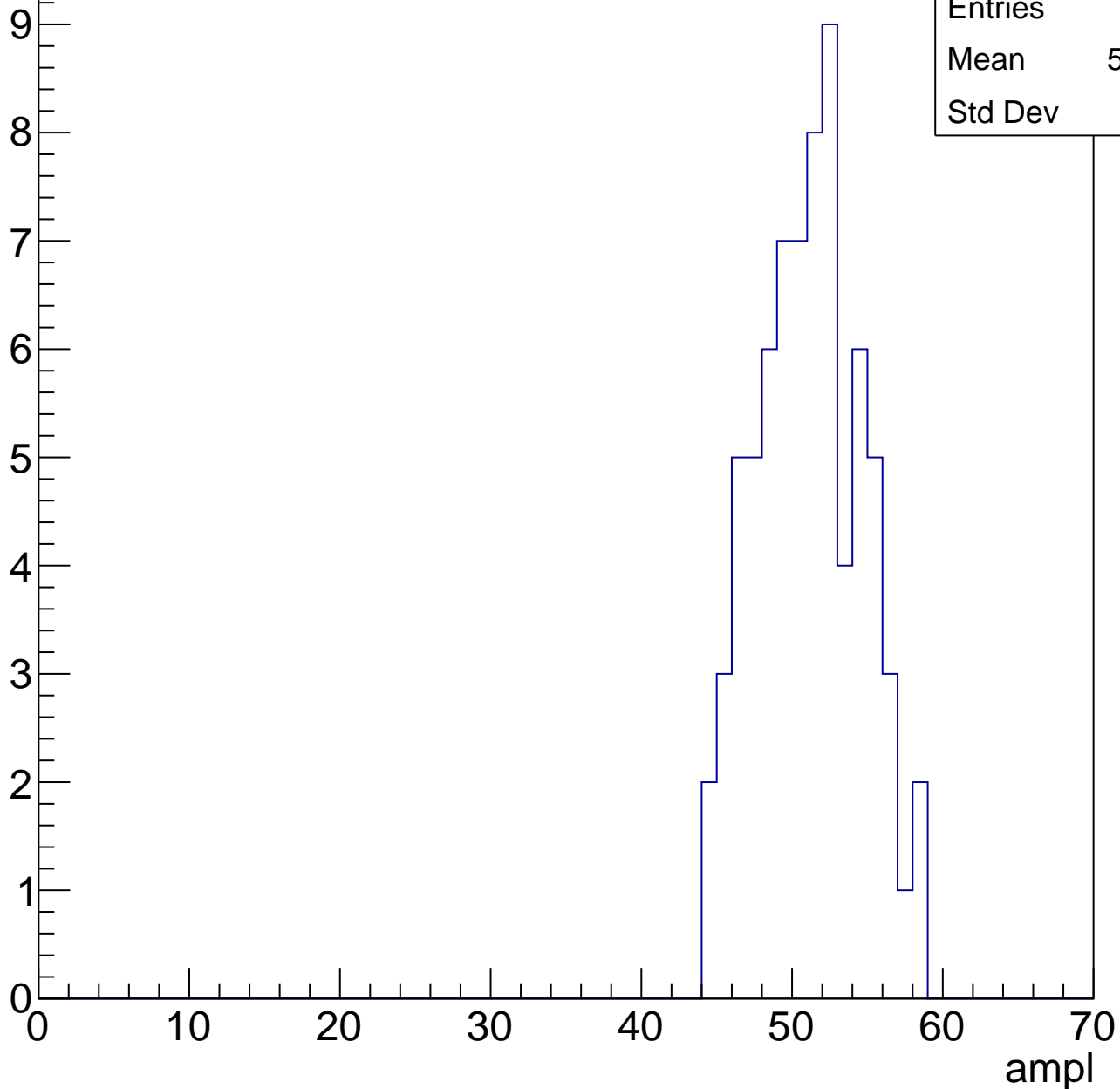


# B0L001S, U17-ch33, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	50.64
Std Dev	3.43

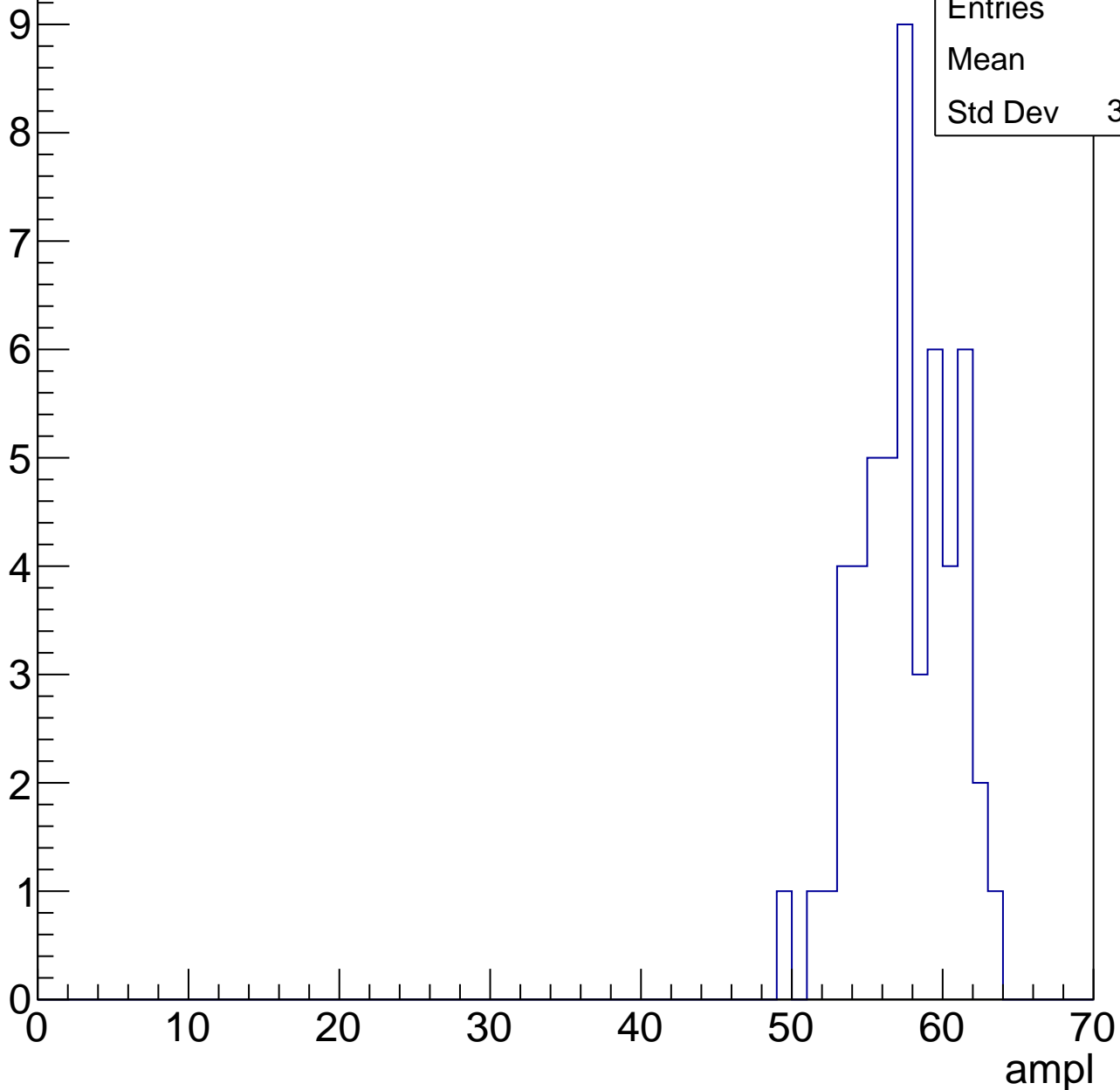


# B0L001S, U17-ch33, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	57.1
Std Dev	3.084

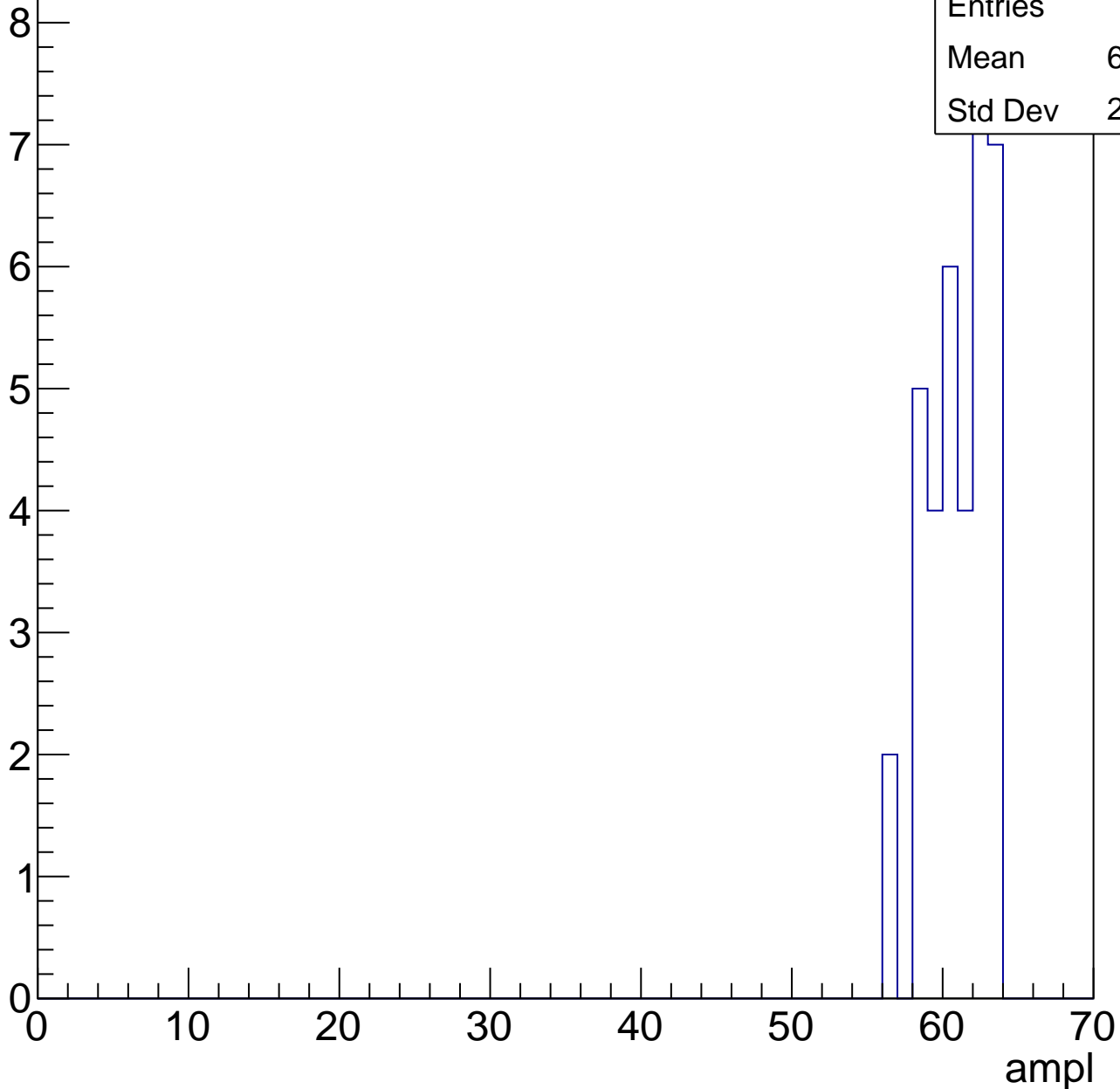


# B0L001S, U17-ch33, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	36
Mean	60.53
Std Dev	2.007



# B0L001S, U17-ch33, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch33, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U17-ch34, adc0

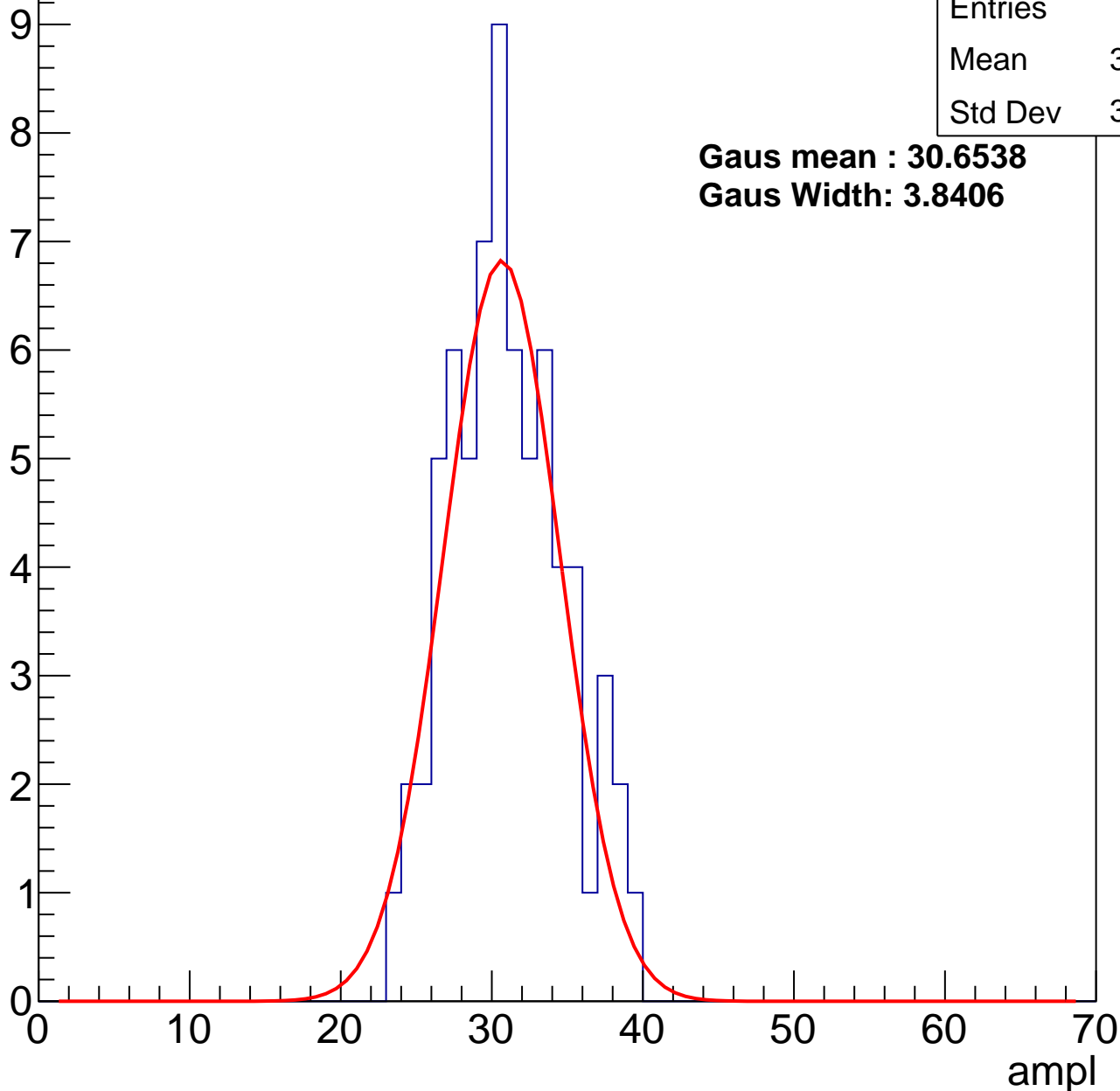
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	30.55
Std Dev	3.705

**Gaus mean : 30.6538**

**Gaus Width: 3.8406**



# B0L001S, U17-ch34, adc1

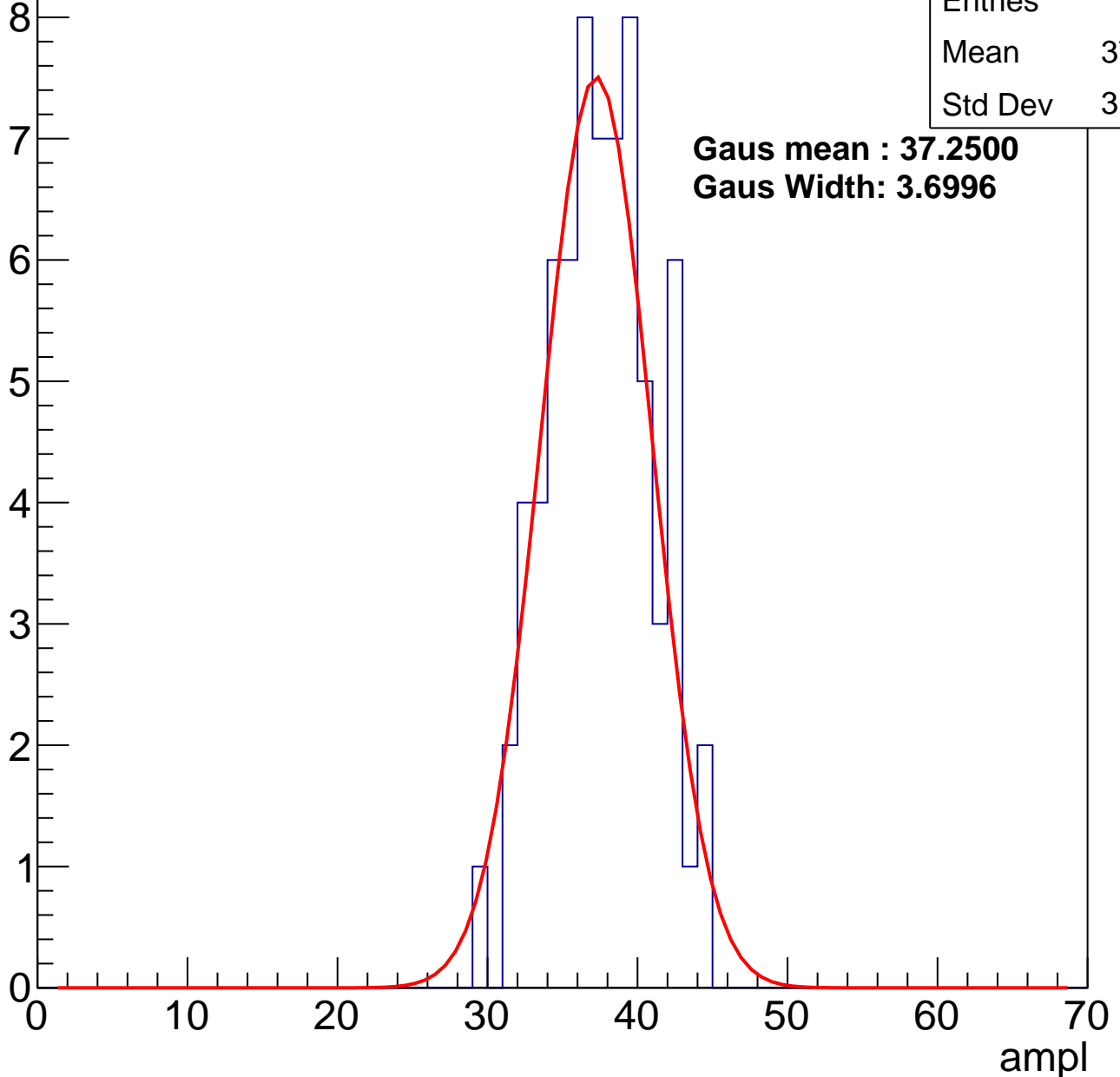
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	37.09
Std Dev	3.384

**Gaus mean : 37.2500**

**Gaus Width: 3.6996**



# B0L001S, U17-ch34, adc2

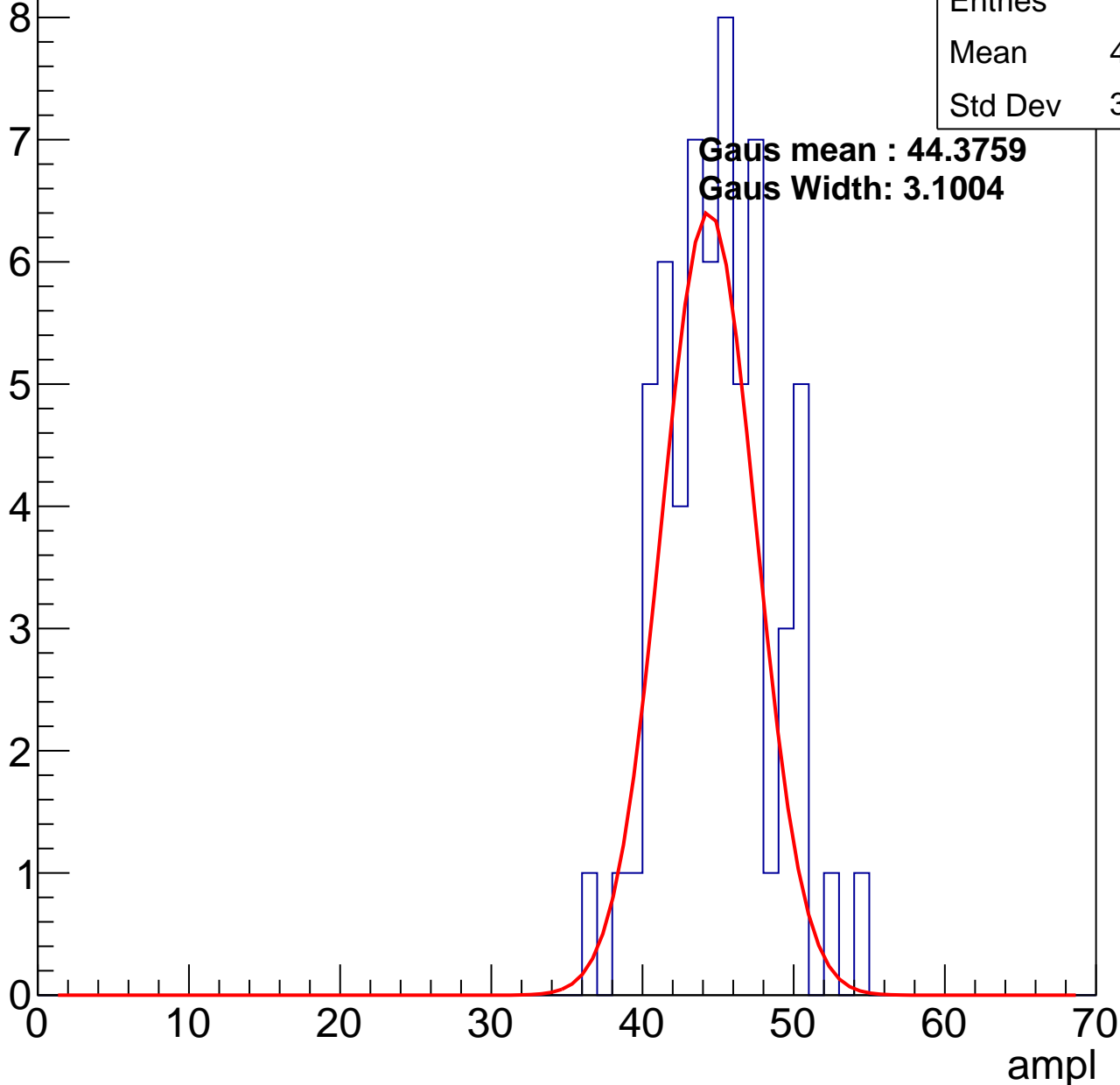
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	44.55
Std Dev	3.568

**Gaus mean : 44.3759**

**Gaus Width: 3.1004**

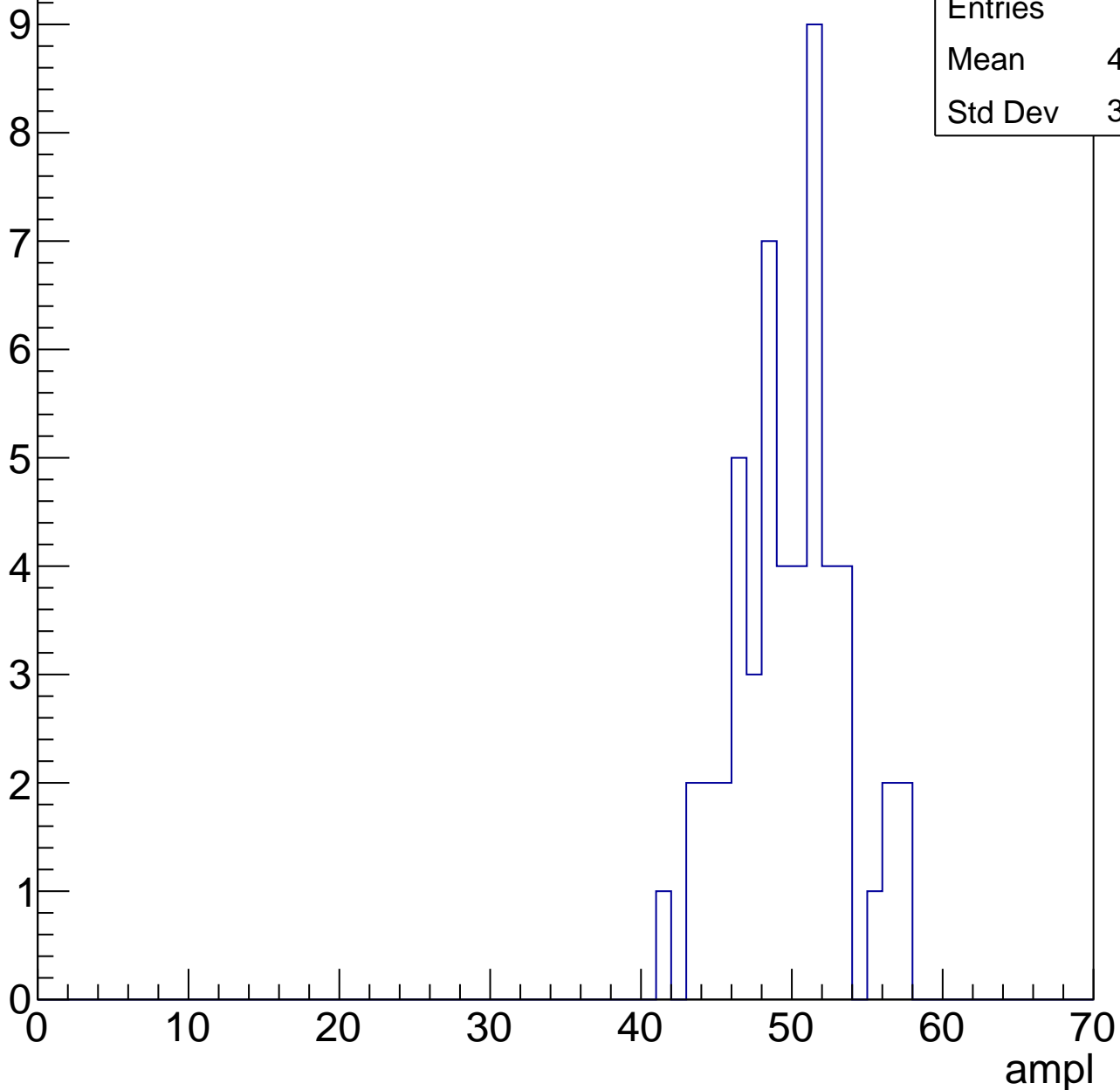


# B0L001S, U17-ch34, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	49.38
Std Dev	3.606

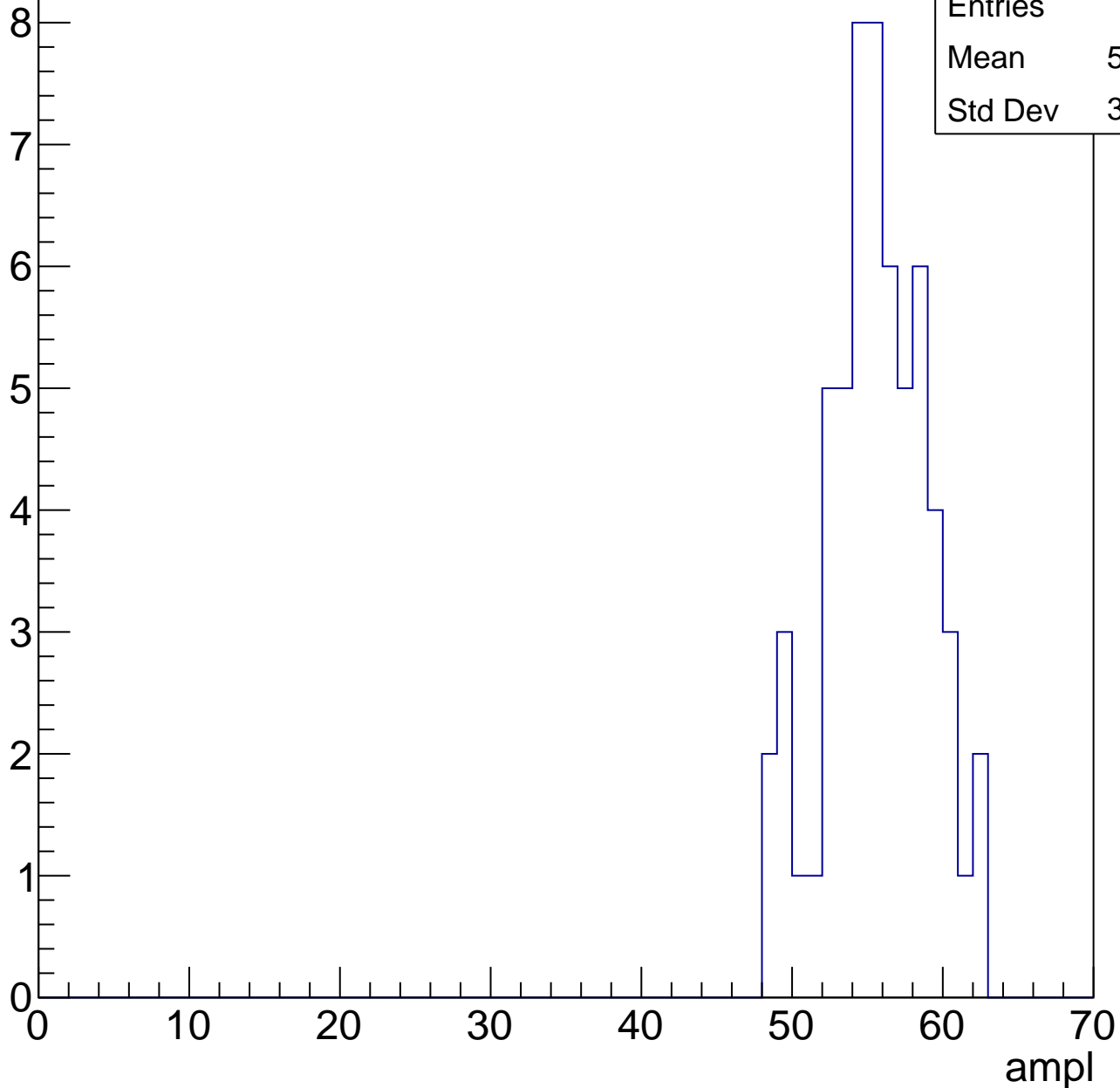


# B0L001S, U17-ch34, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	55.18
Std Dev	3.344

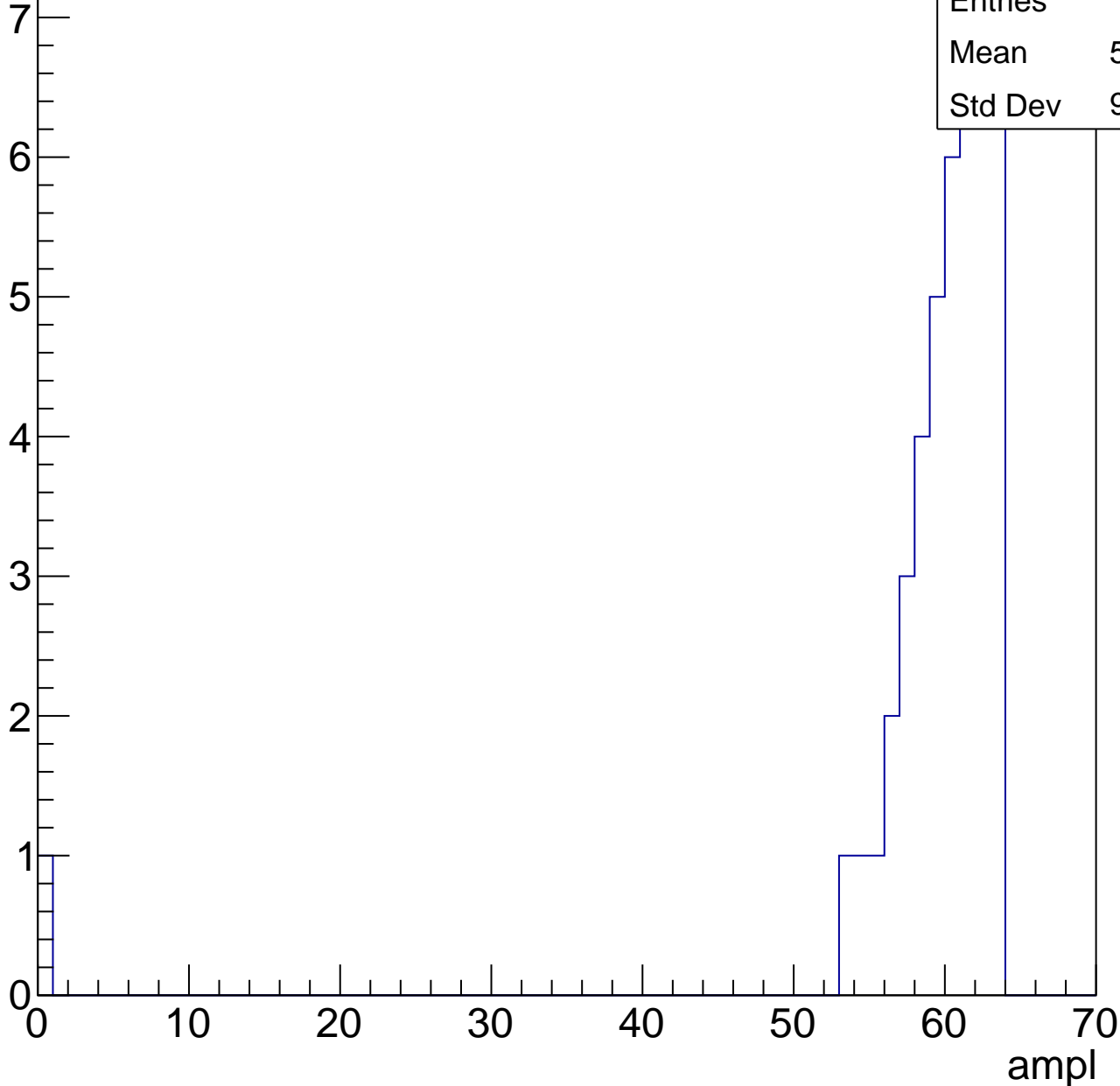


# B0L001S, U17-ch34, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	45
Mean	58.53
Std Dev	9.179



# B0L001S, U17-ch34, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries

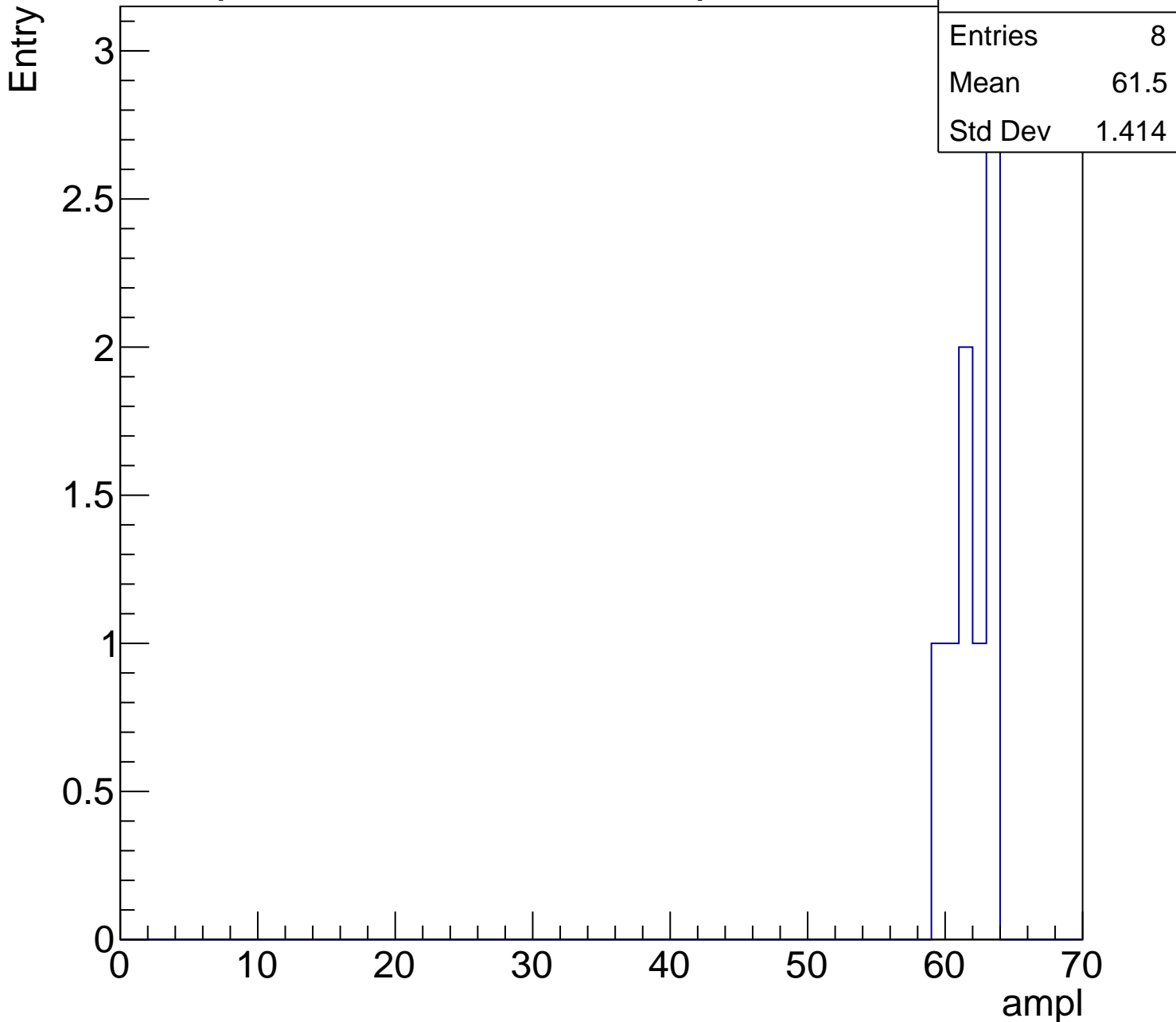
8

Mean

61.5

Std Dev

1.414





# B0L001S, U17-ch34, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U17-ch35, adc0

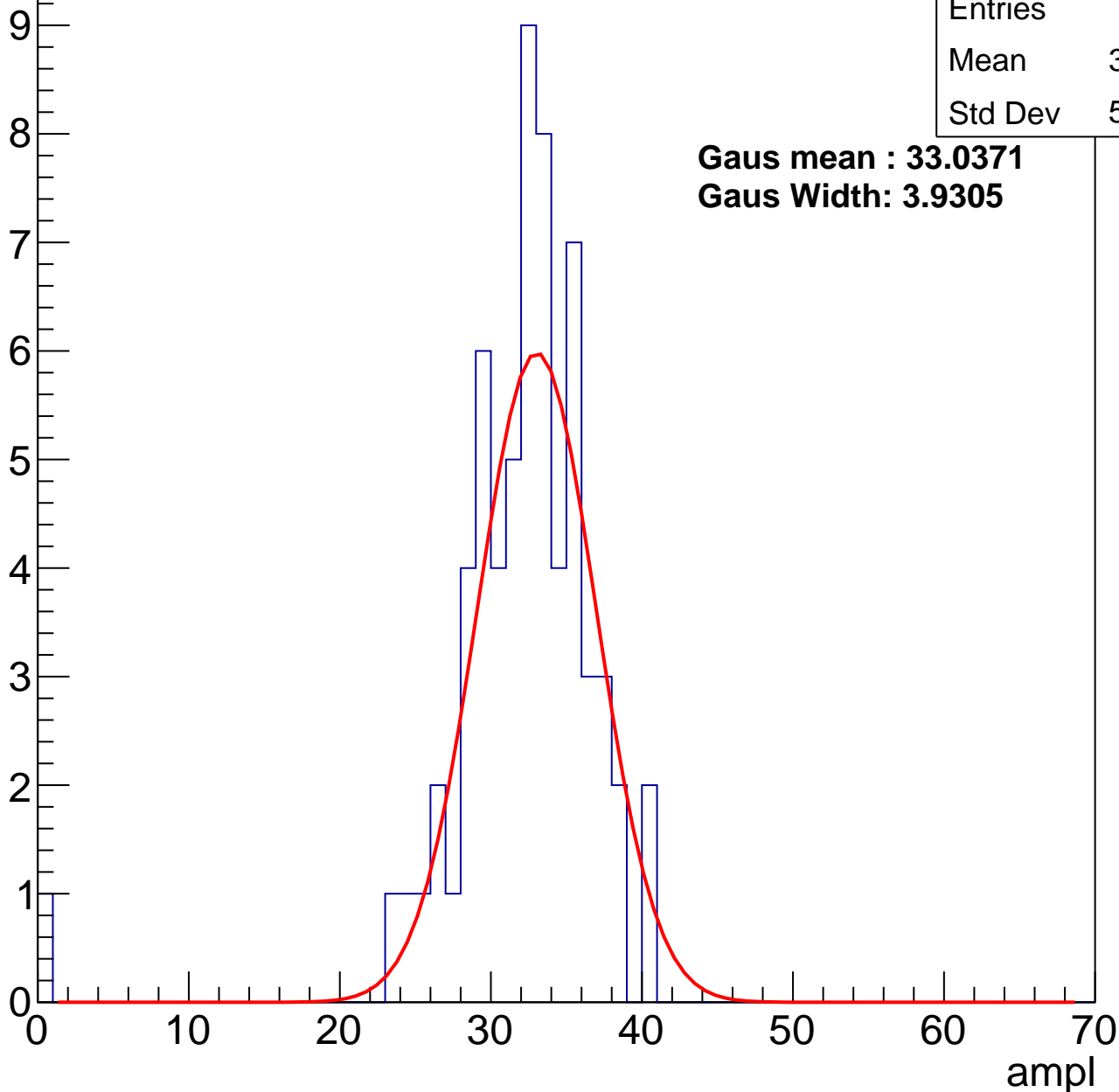
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	31.56
Std Dev	5.379

**Gaus mean : 33.0371**

**Gaus Width: 3.9305**



# B0L001S, U17-ch35, adc1

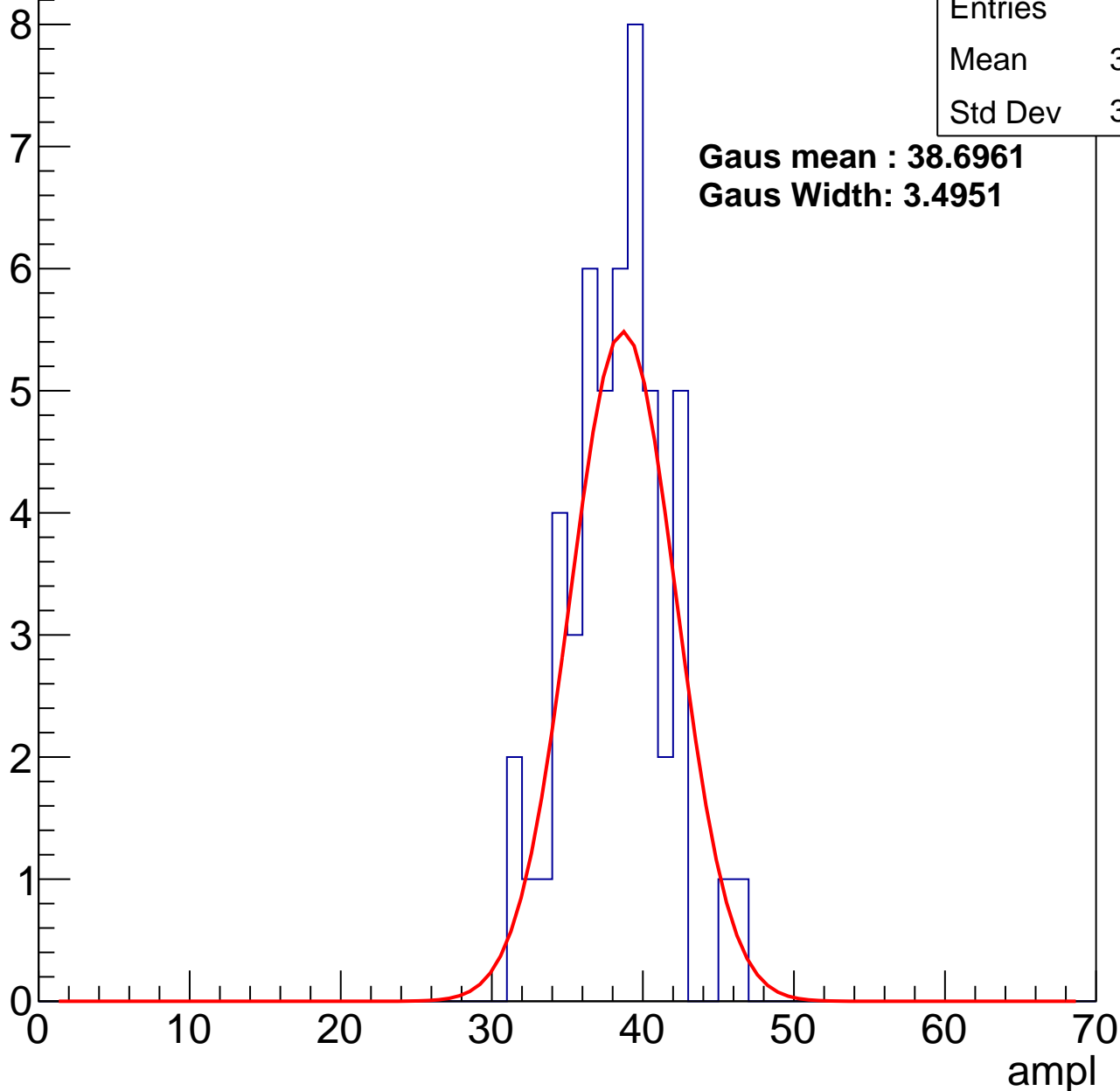
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	50
Mean	37.84
Std Dev	3.215

**Gaus mean : 38.6961**

**Gaus Width: 3.4951**



# B0L001S, U17-ch35, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	73
Mean	43.64
Std Dev	3.772

**Gaus mean : 44.2679**

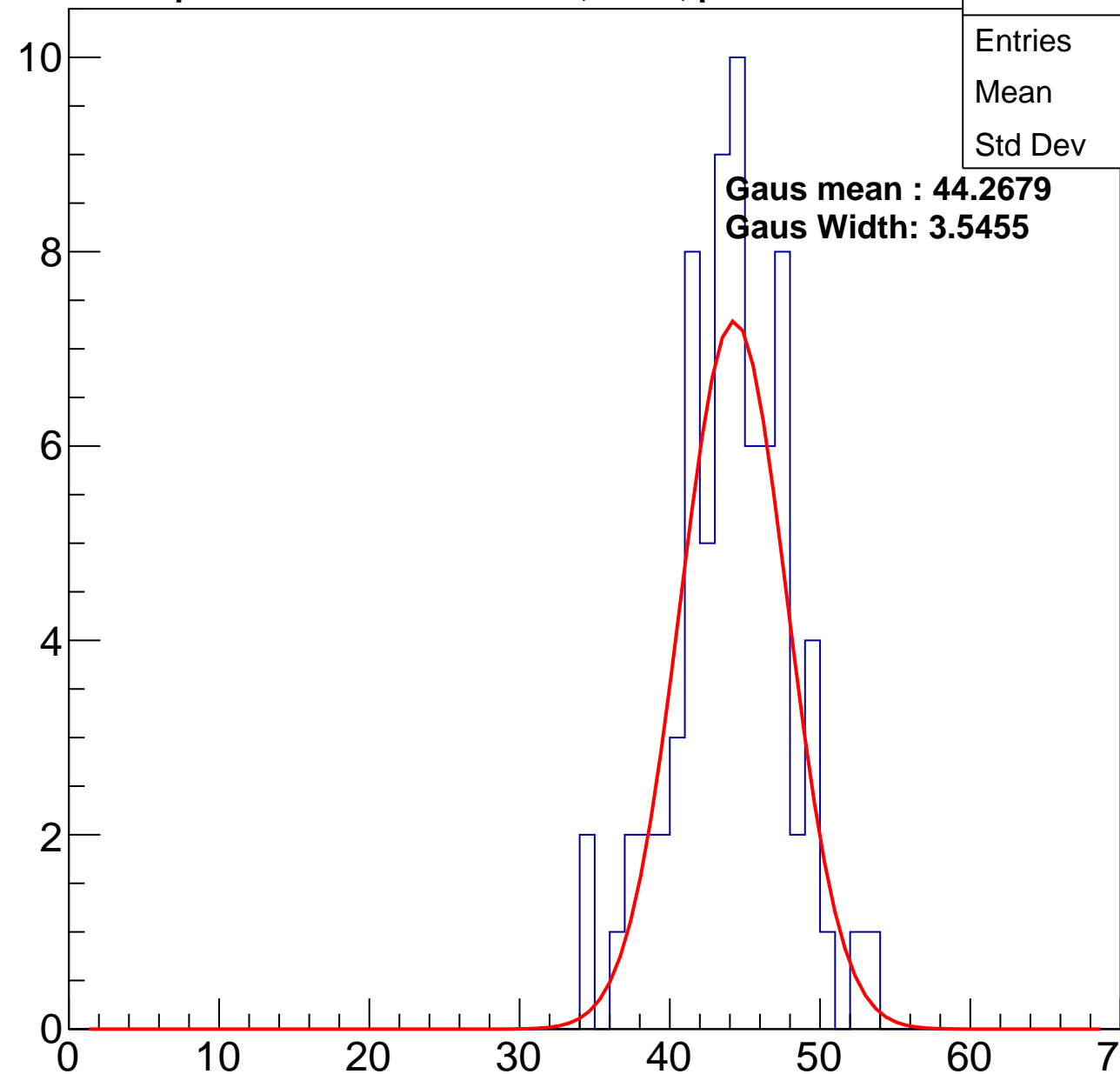
**Gaus Width: 3.5455**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U17-ch35, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

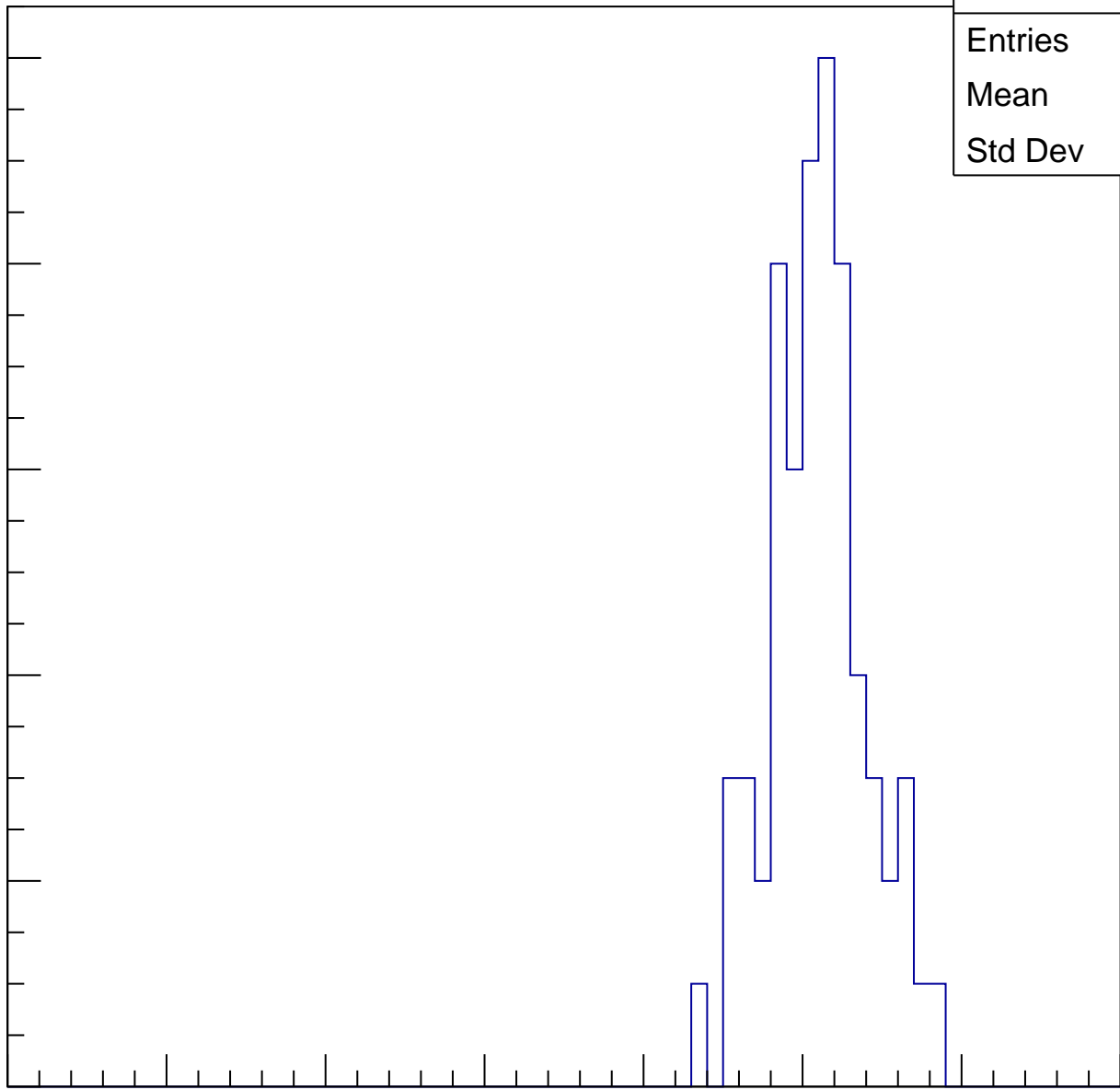
Entries	64
Mean	50.48
Std Dev	3.087

Entry

10  
8  
6  
4  
2  
0

ampl

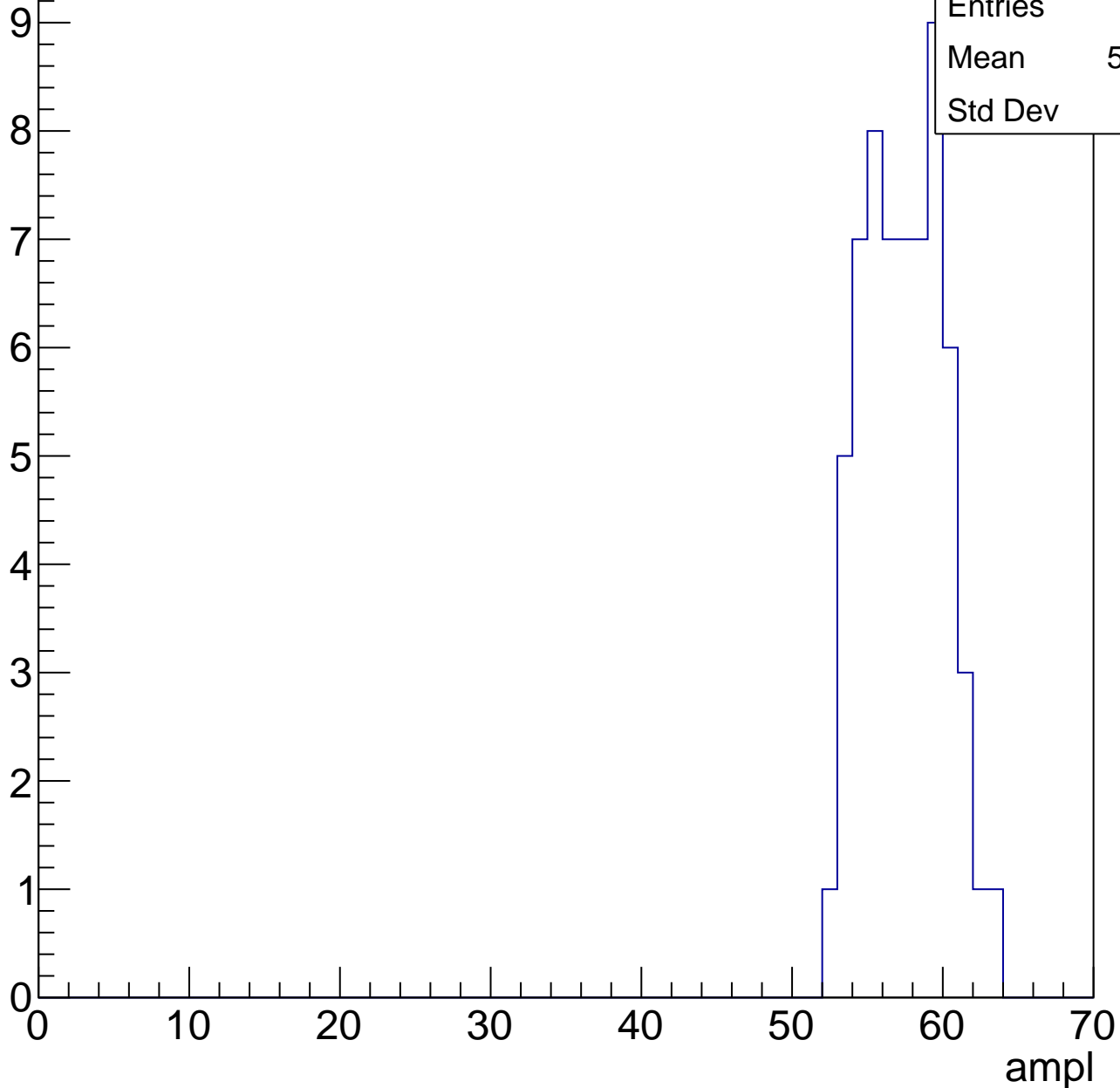
0 10 20 30 40 50 60 70



# B0L001S, U17-ch35, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

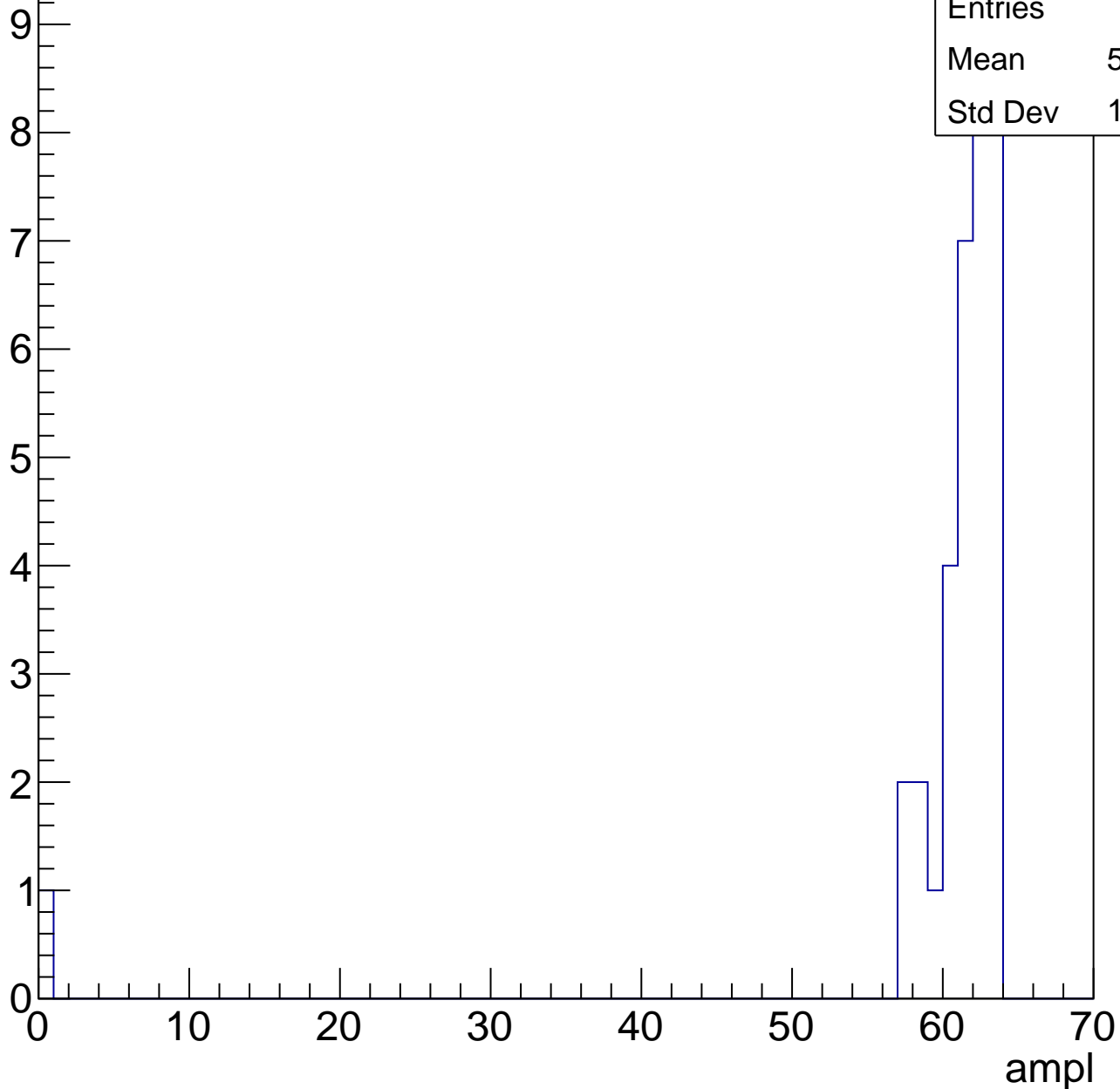


# B0L001S, U17-ch35, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	34
Mean	59.35
Std Dev	10.47



# B0L001S, U17-ch35, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch35, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U17-ch36, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	75
Mean	29.48
Std Dev	3.336

**Gaus mean : 30.0534**

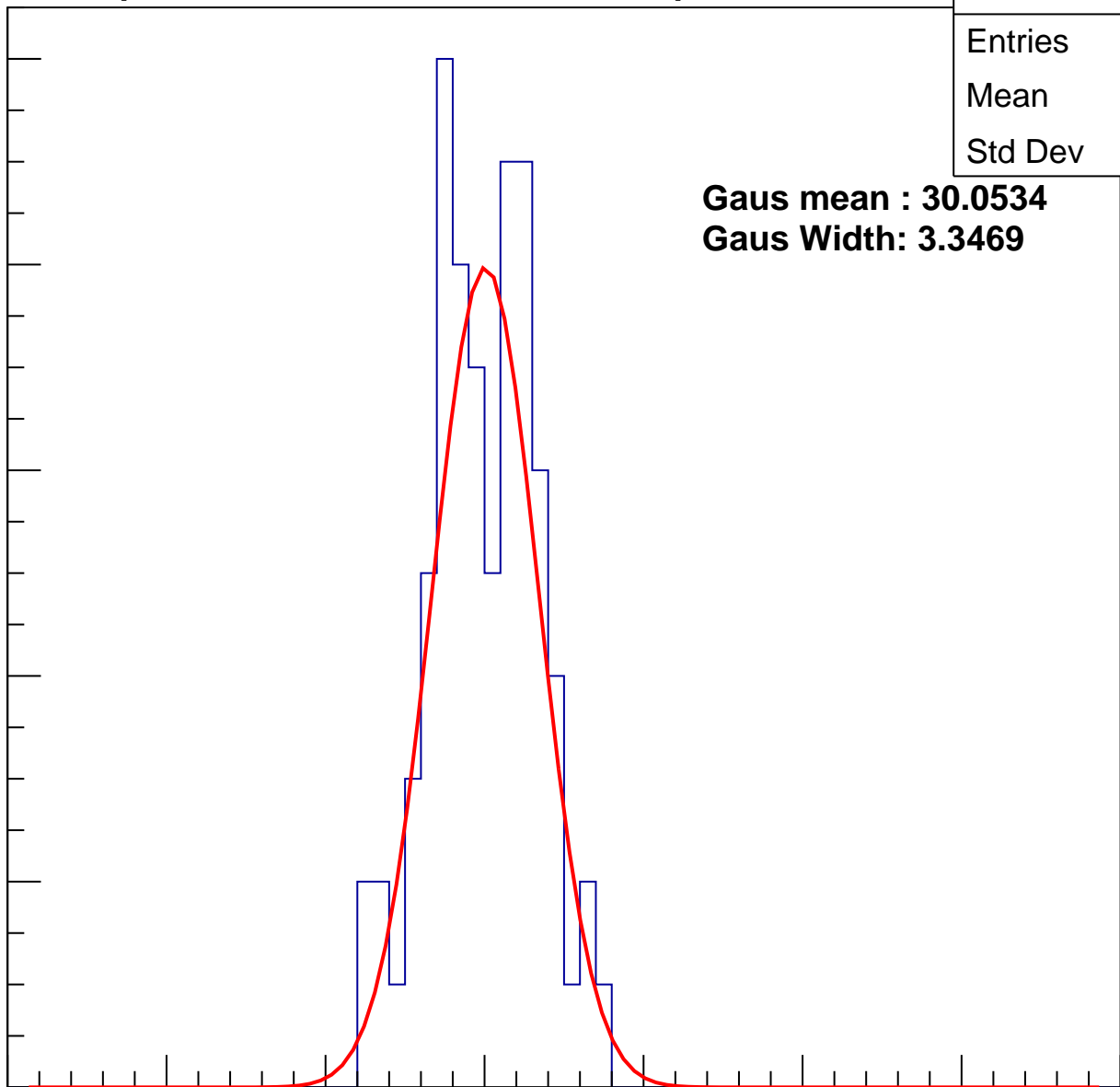
**Gaus Width: 3.3469**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U17-ch36, adc1

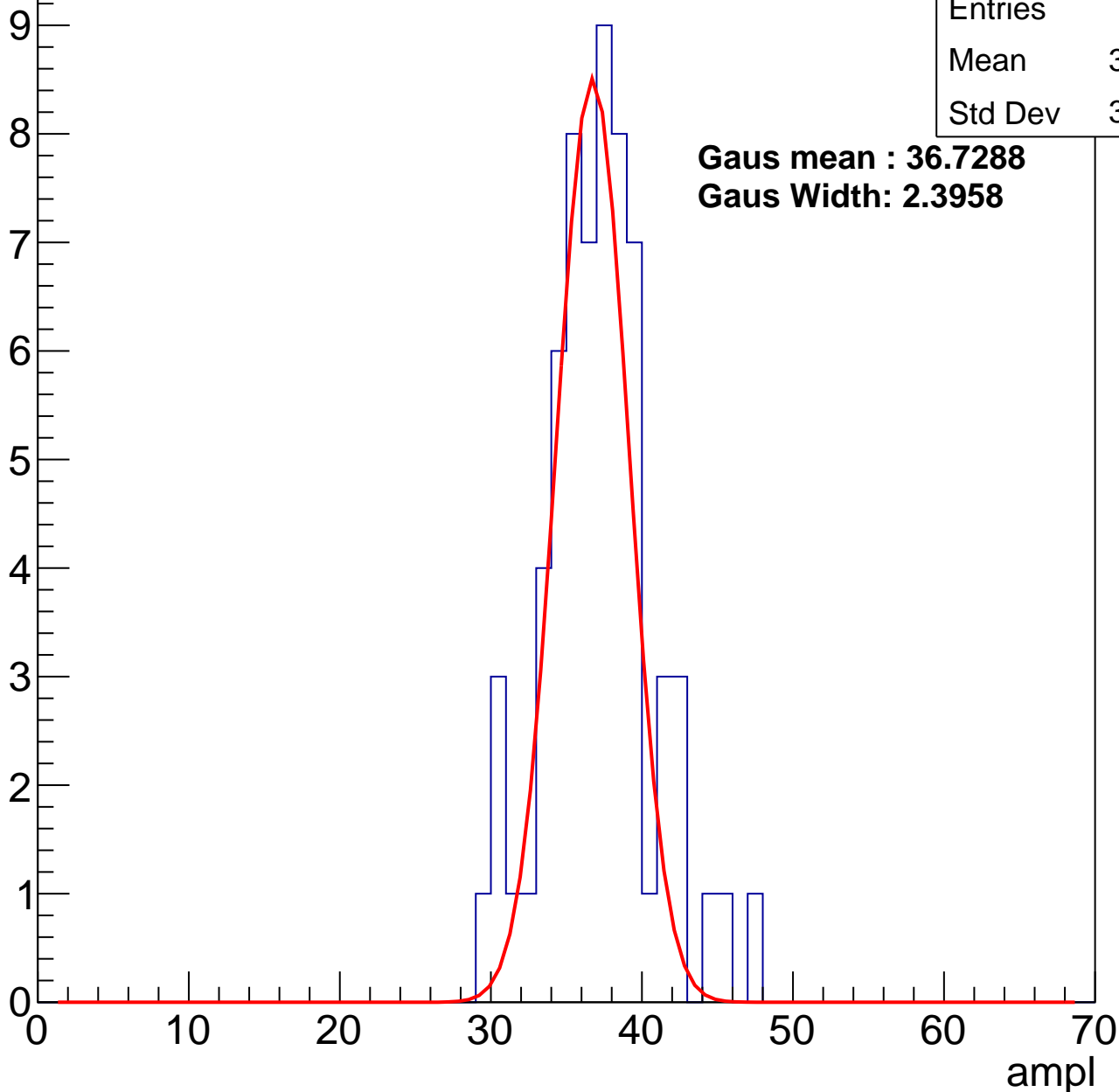
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	36.69
Std Dev	3.517

**Gaus mean : 36.7288**

**Gaus Width: 2.3958**



# B0L001S, U17-ch36, adc2

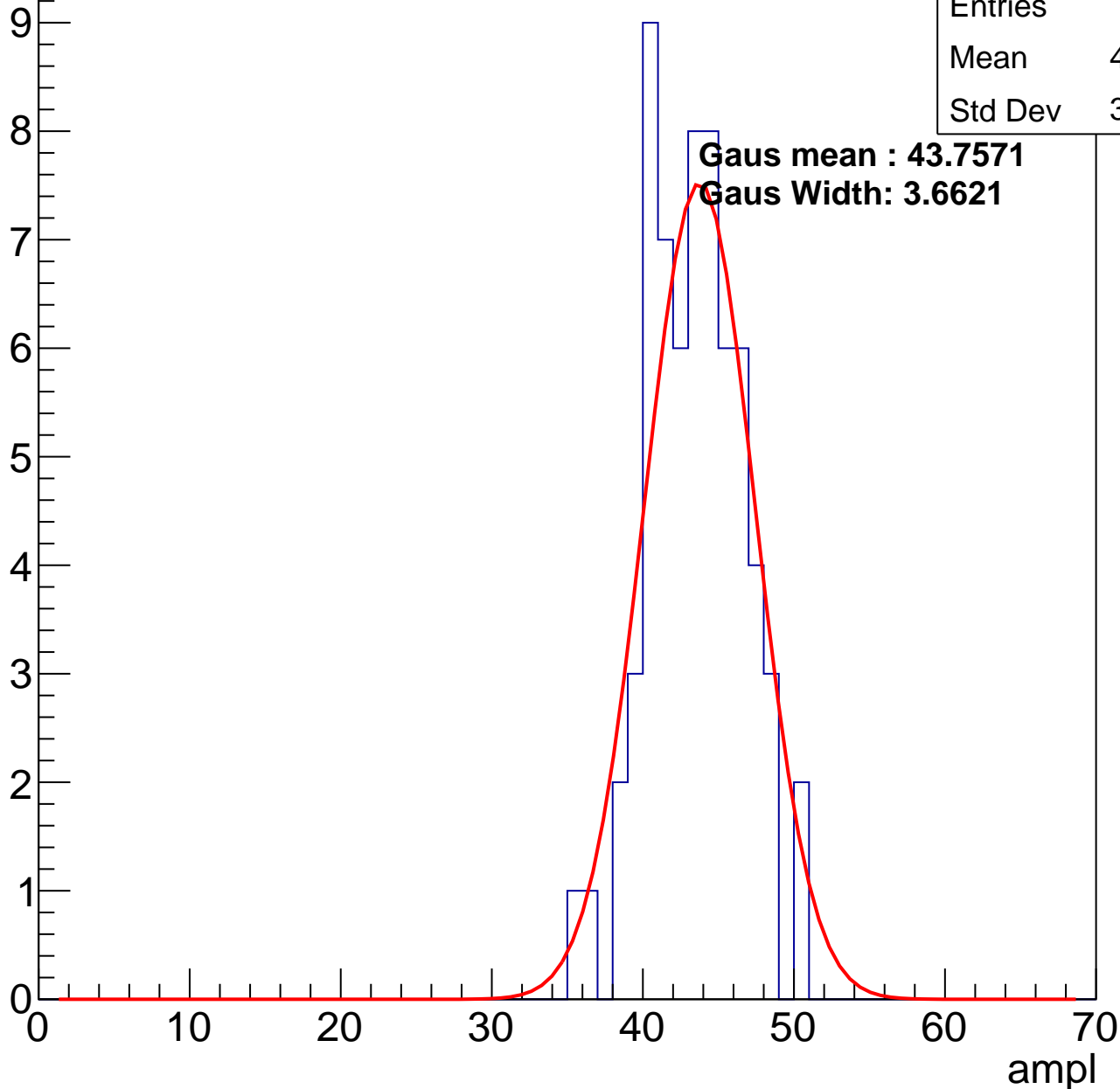
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	42.98
Std Dev	3.136

**Gaus mean : 43.7571**

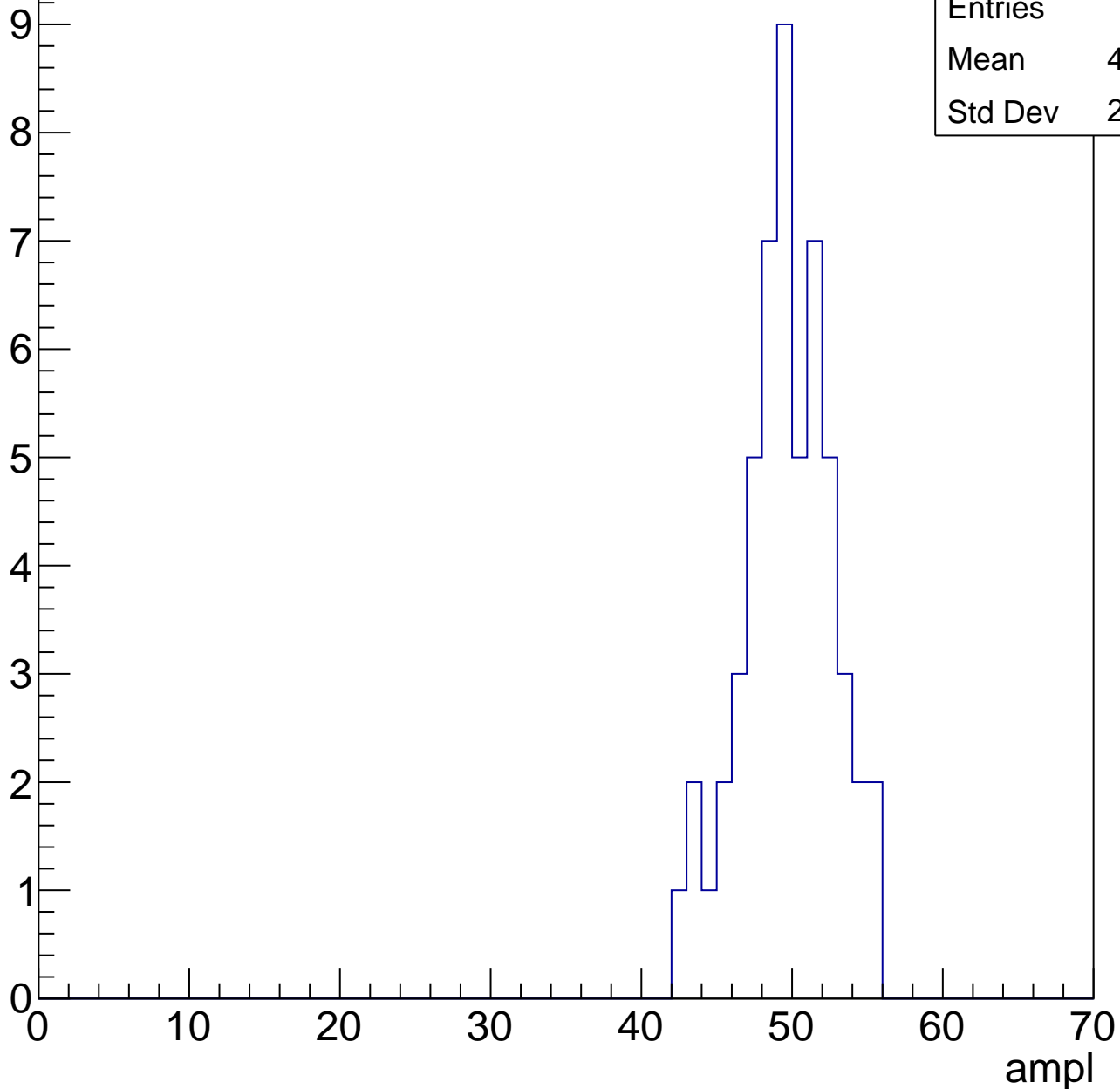
**Gaus Width: 3.6621**



# B0L001S, U17-ch36, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



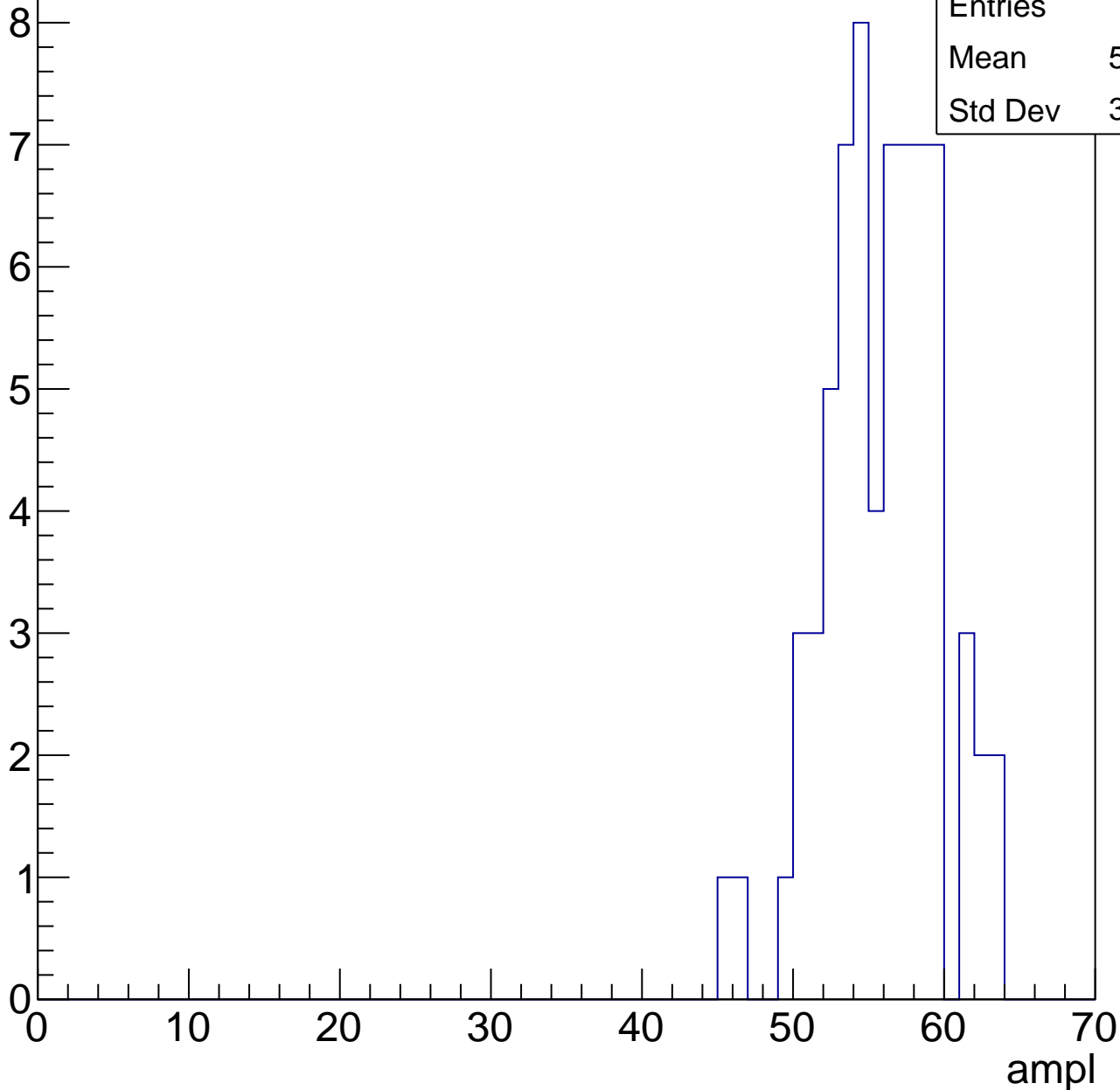
Entries	54
Mean	49.19
Std Dev	2.976

# B0L001S, U17-ch36, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	55.43
Std Dev	3.743



# B0L001S, U17-ch36, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	48
Mean	58.6
Std Dev	8.895

Entry

10

8

6

4

2

0

0

10

20

30

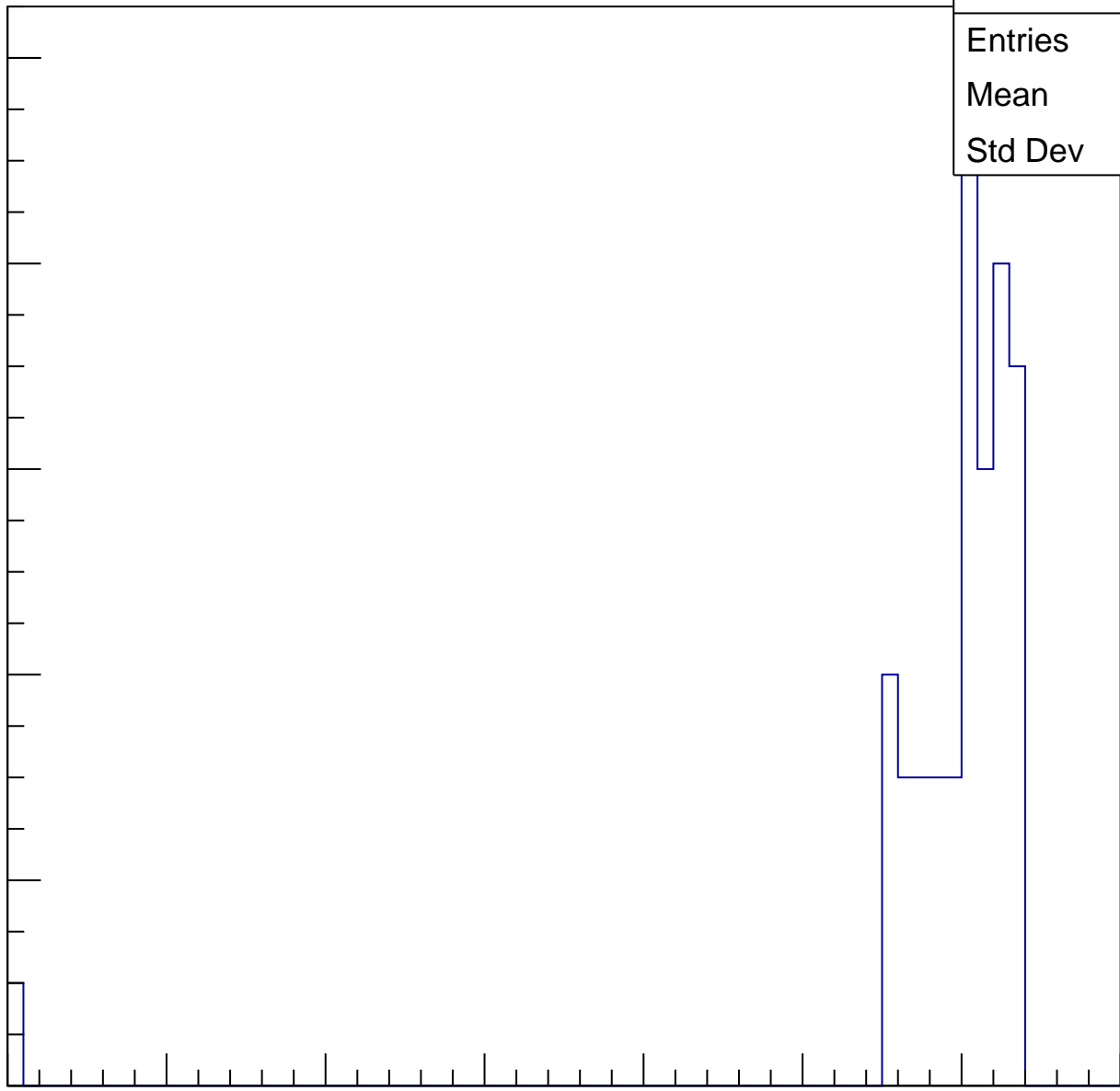
40

50

60

70

ampl



# B0L001S, U17-ch36, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch36, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U17-ch37, adc0

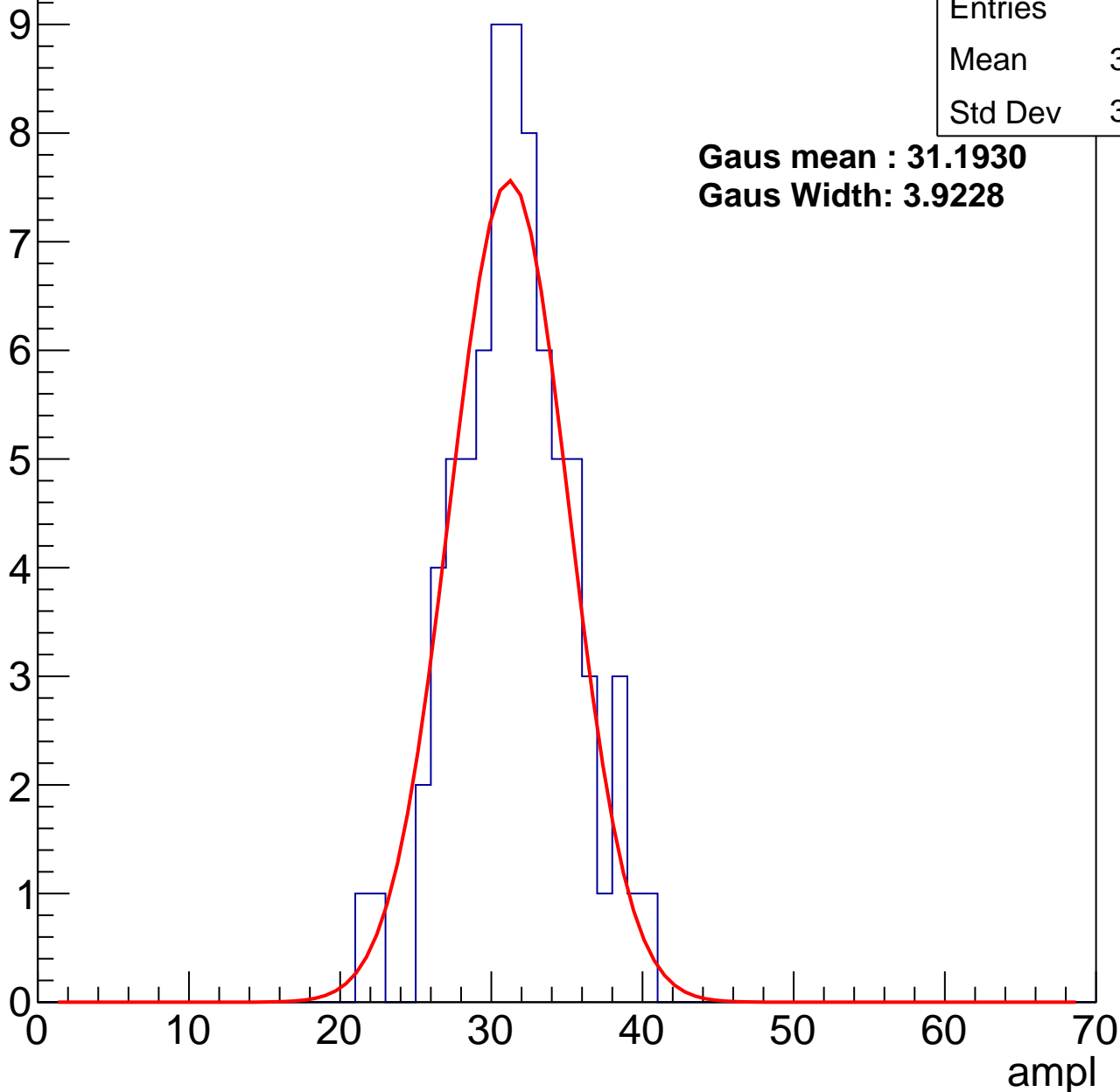
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	75
Mean	31.09
Std Dev	3.778

**Gaus mean : 31.1930**

**Gaus Width: 3.9228**



# B0L001S, U17-ch37, adc1

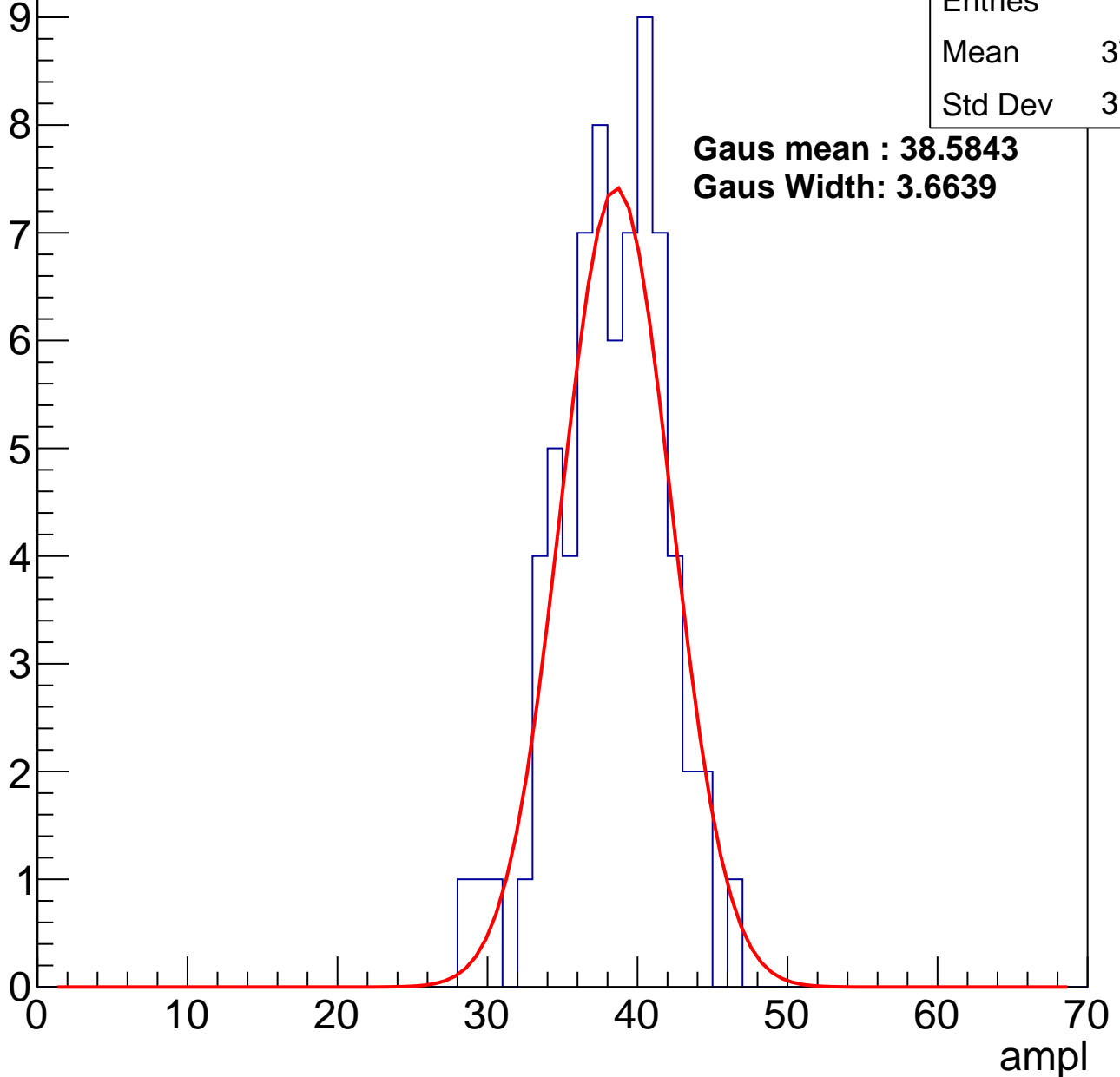
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	37.79
Std Dev	3.557

**Gaus mean : 38.5843**

**Gaus Width: 3.6639**



# B0L001S, U17-ch37, adc2

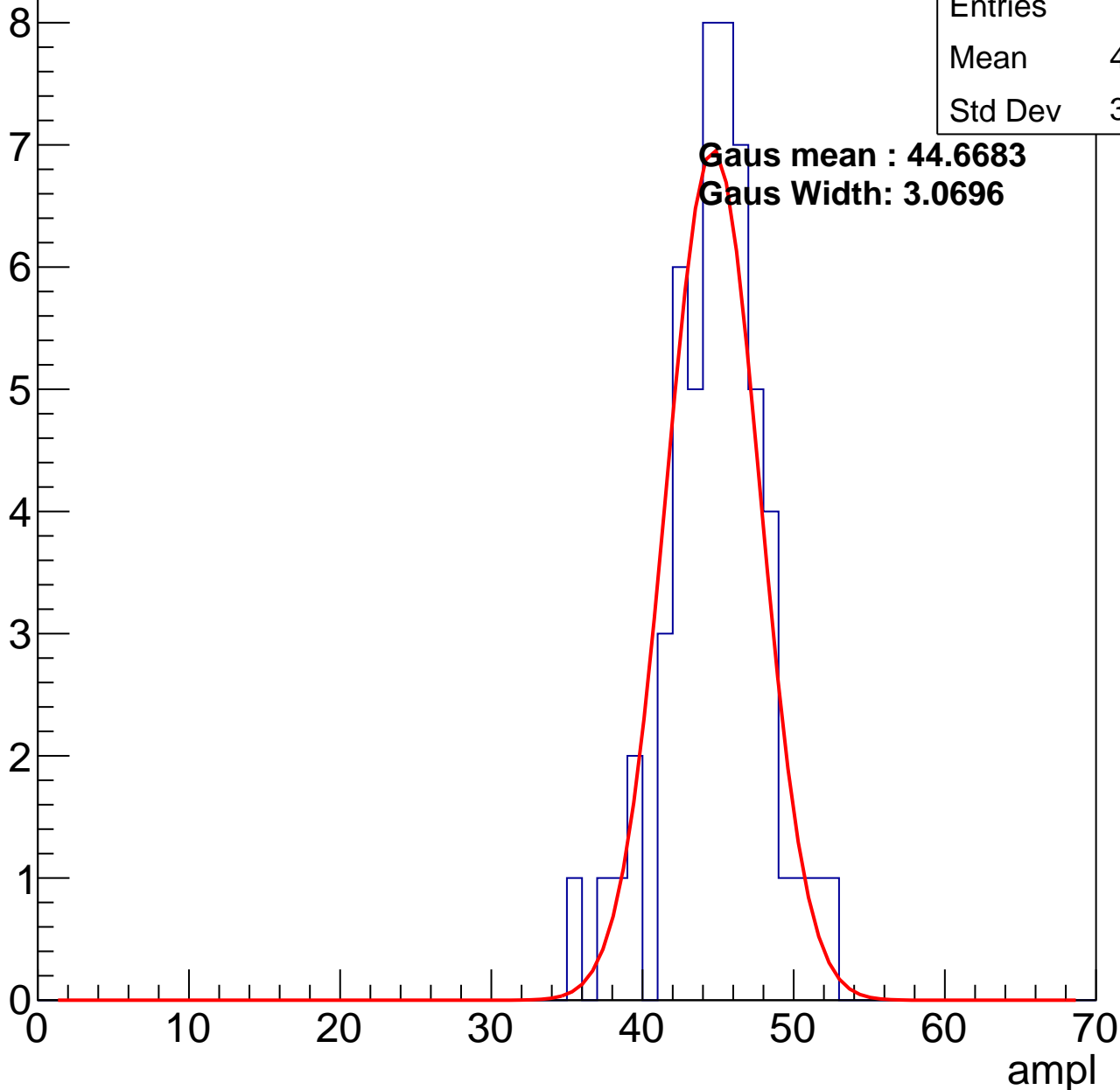
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	44.38
Std Dev	3.256

**Gaus mean : 44.6683**

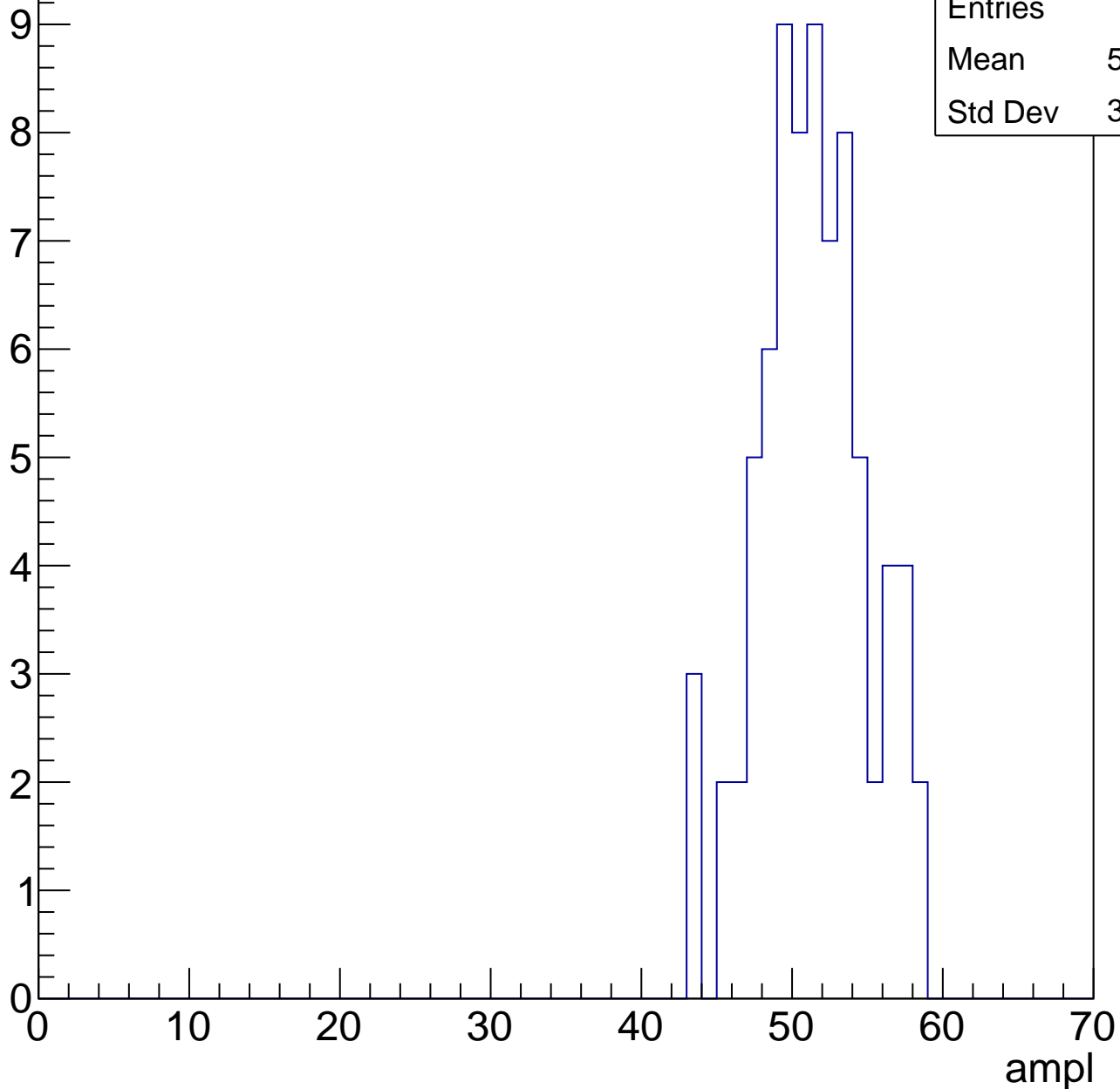
**Gaus Width: 3.0696**



# B0L001S, U17-ch37, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

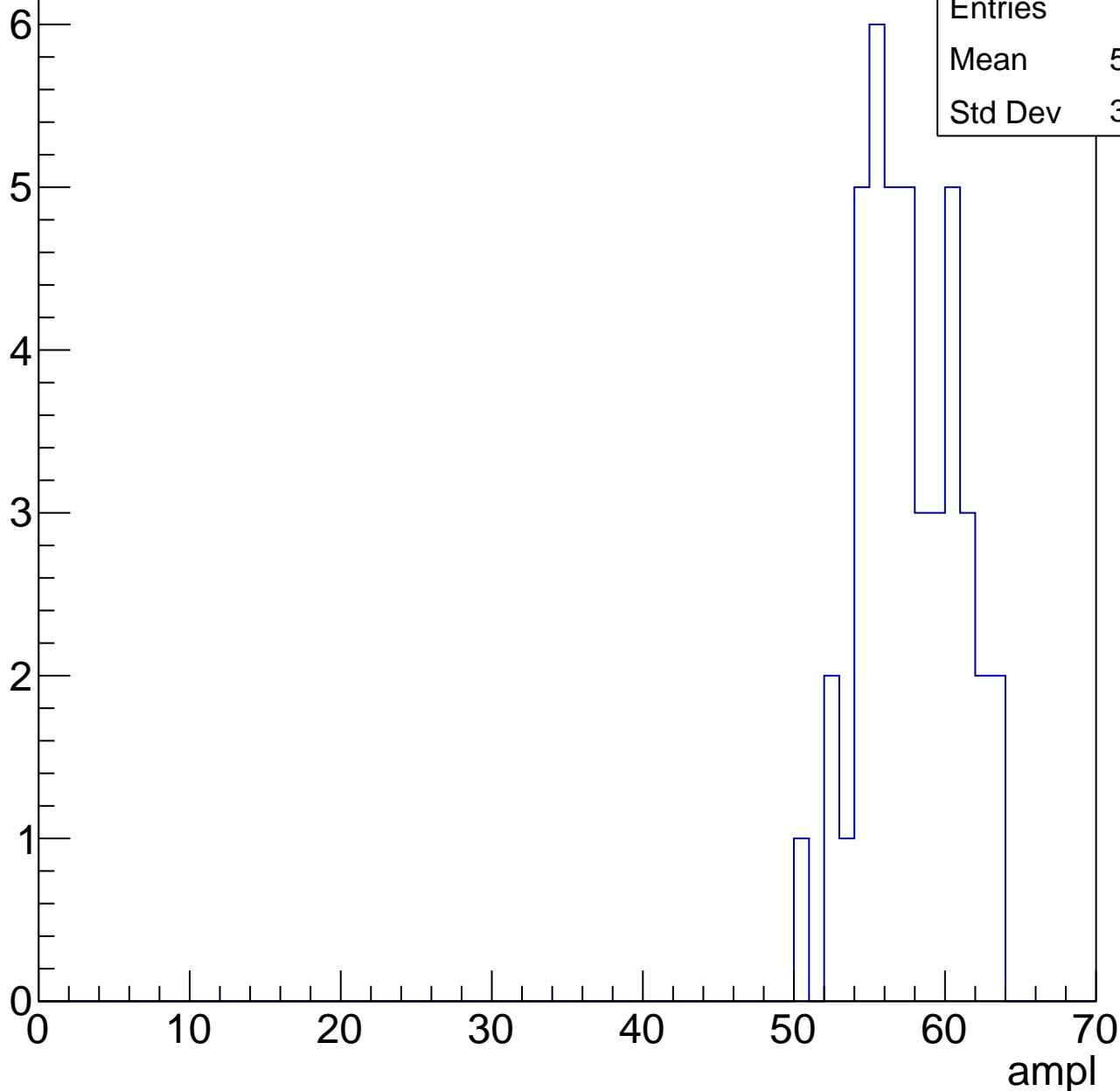


# B0L001S, U17-ch37, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	43
Mean	57.12
Std Dev	3.119

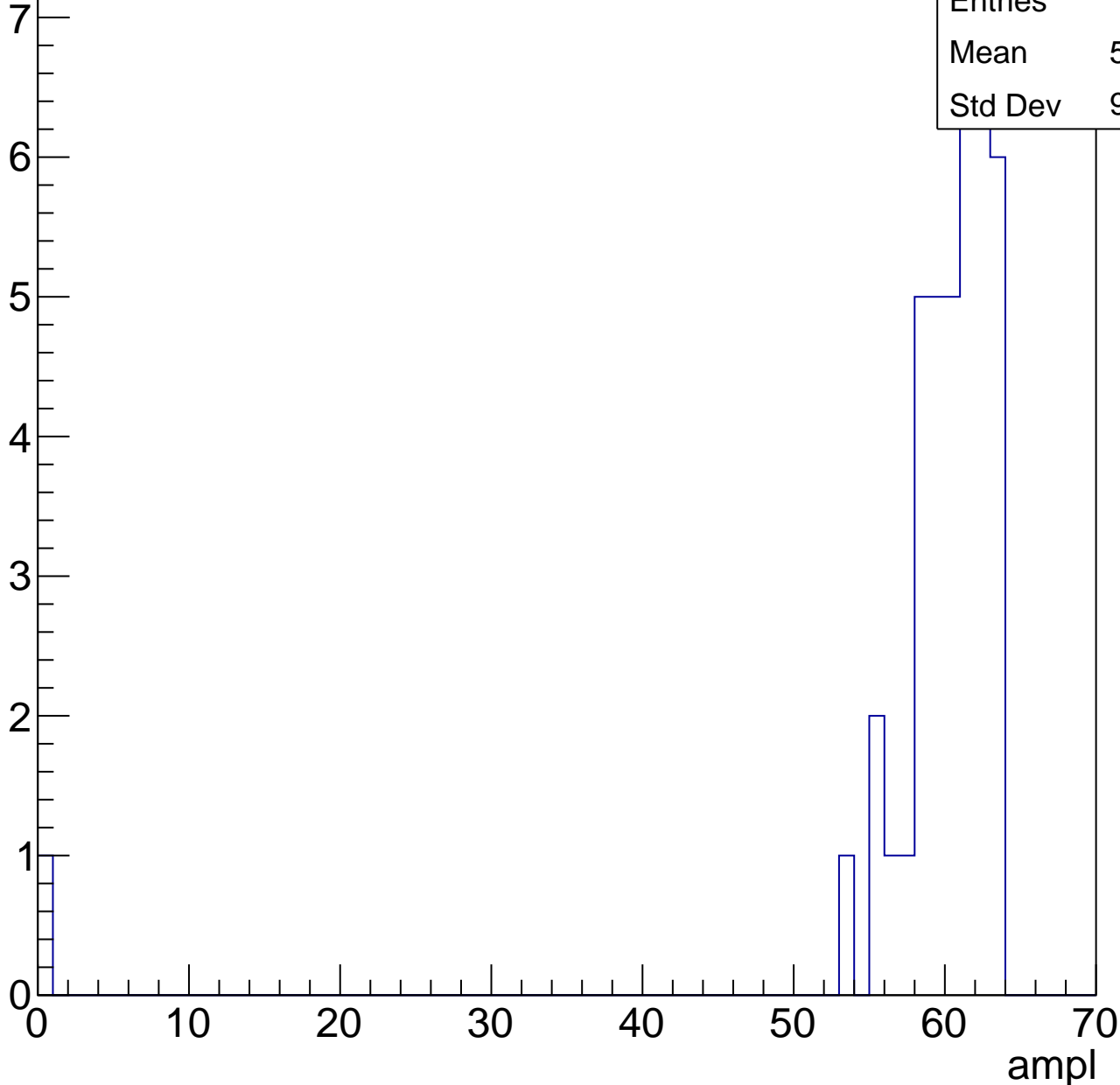


# B0L001S, U17-ch37, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	41
Mean	58.54
Std Dev	9.564



# B0L001S, U17-ch37, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

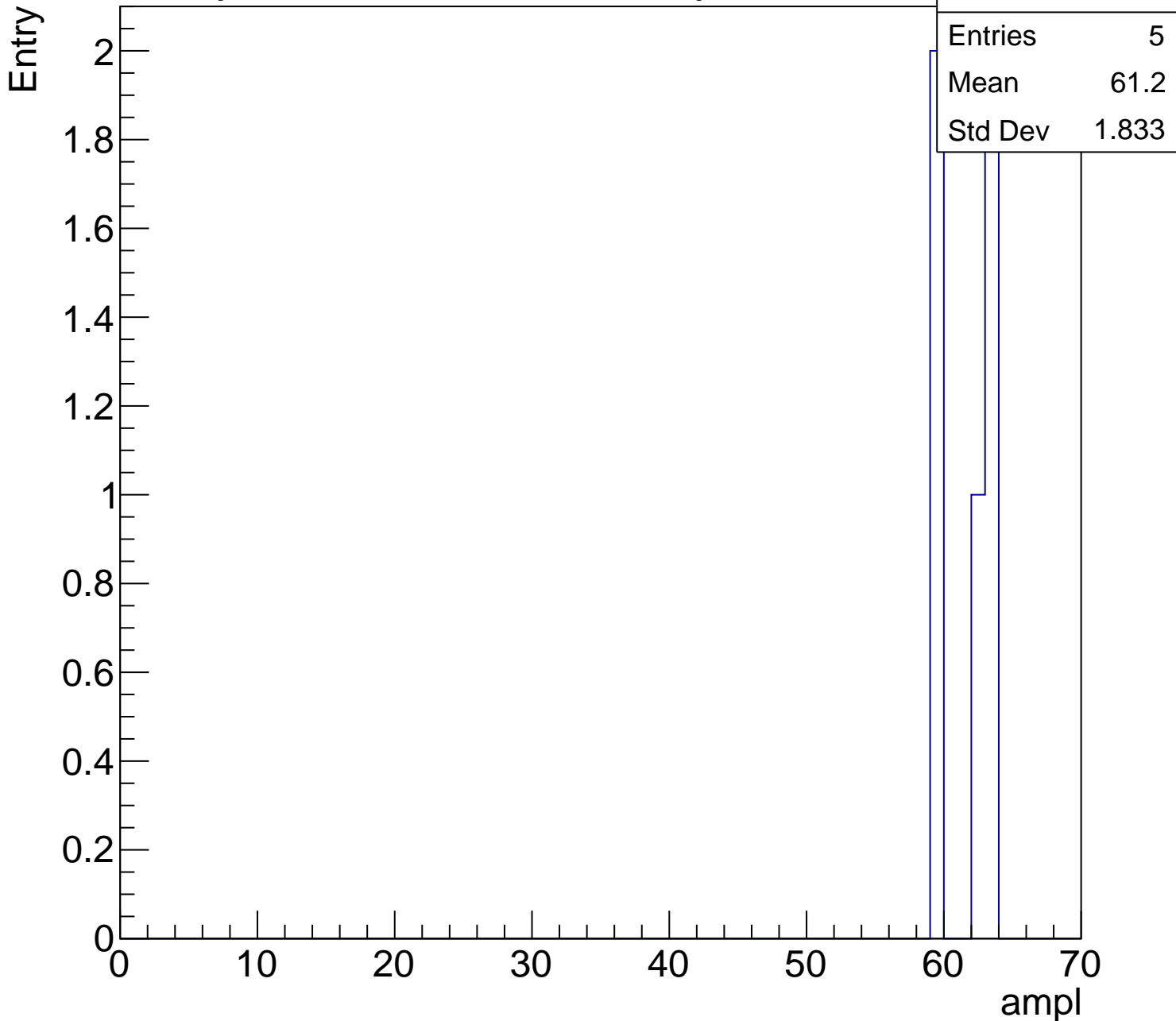
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	61.2
Std Dev	1.833

0 10 20 30 40 50 60 70

ampl





# B0L001S, U17-ch37, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U17-ch38, adc0

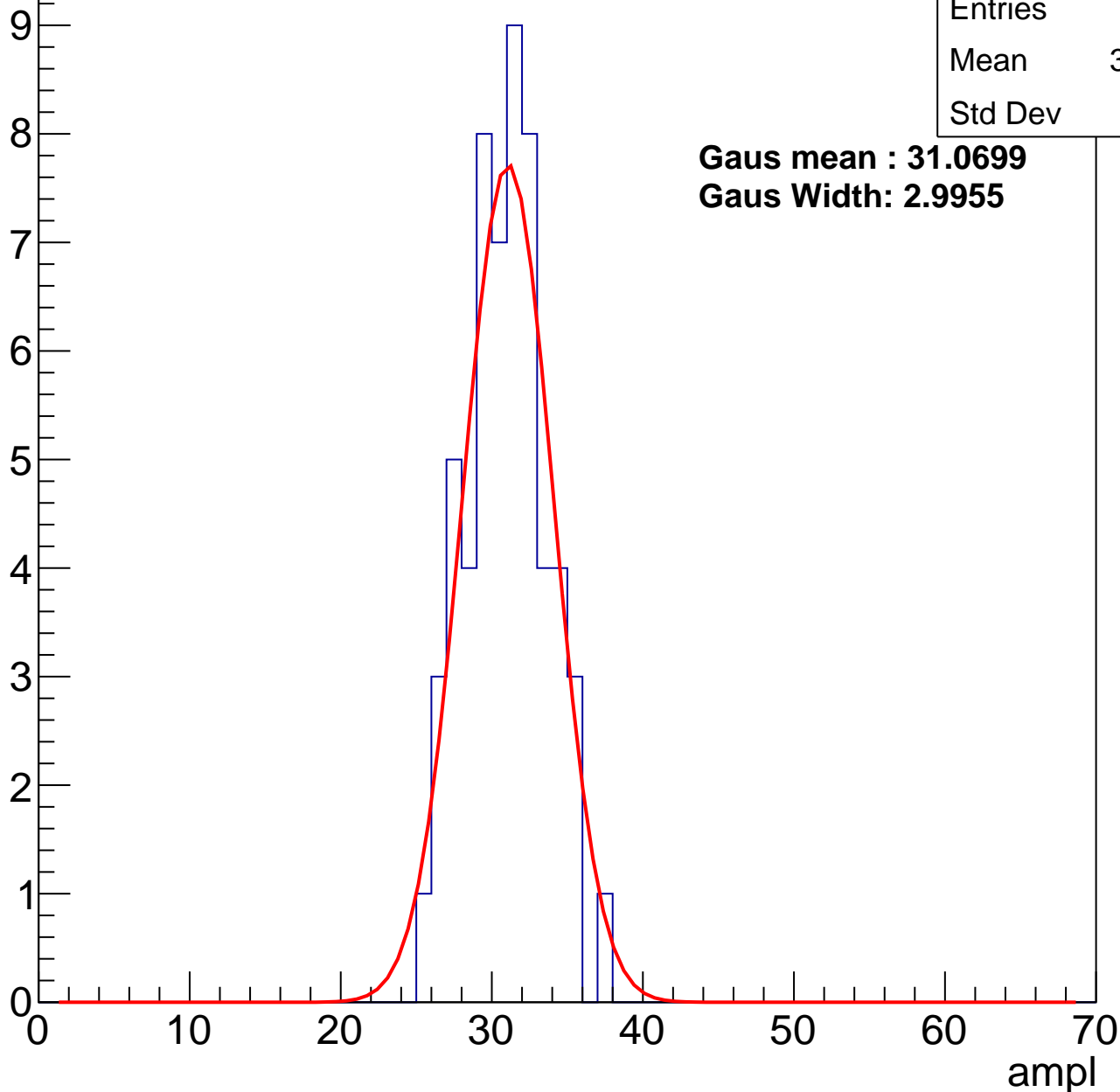
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	30.47
Std Dev	2.63

**Gaus mean : 31.0699**

**Gaus Width: 2.9955**



# B0L001S, U17-ch38, adc1

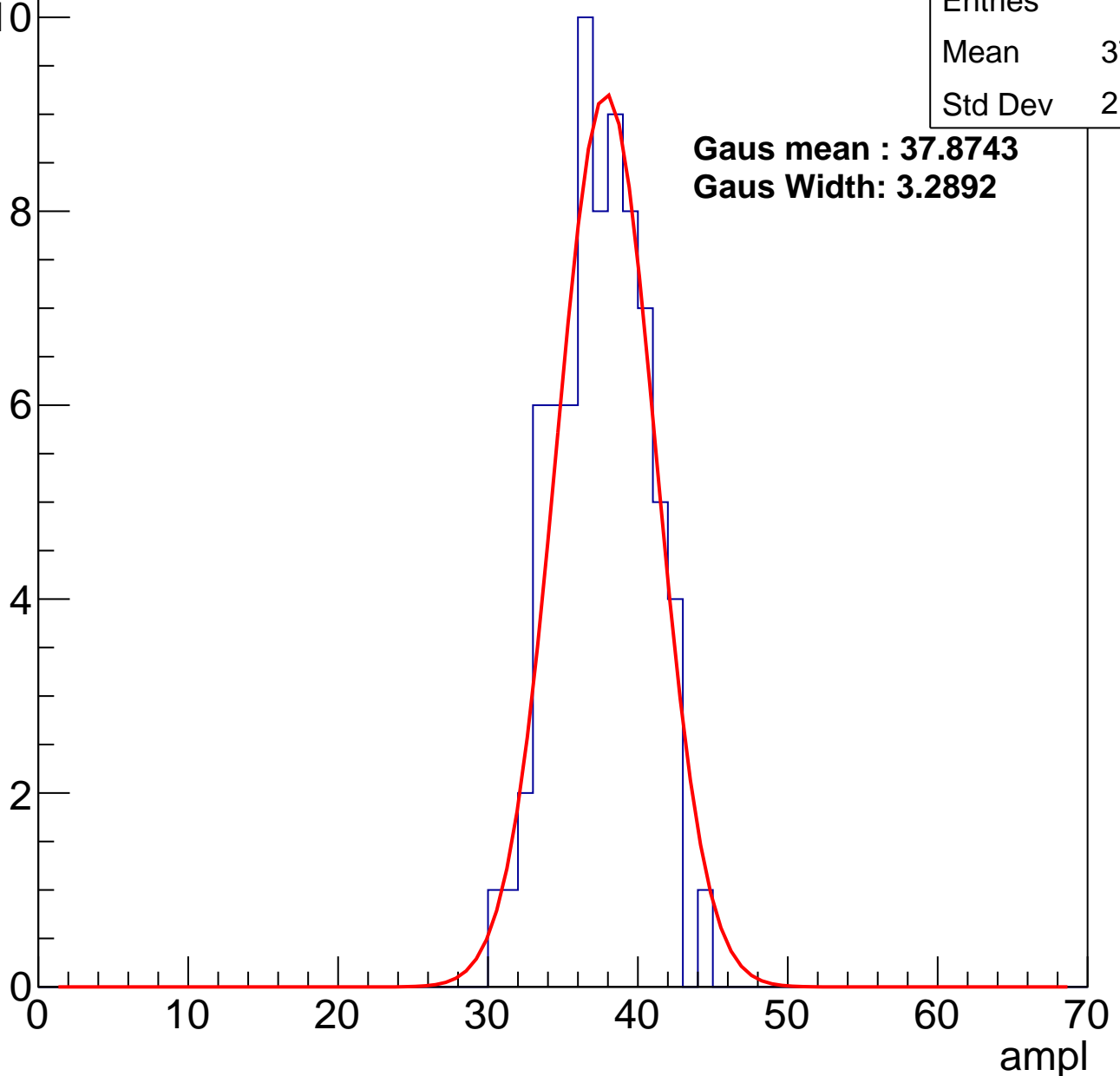
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	37.08
Std Dev	2.967

**Gaus mean : 37.8743**

**Gaus Width: 3.2892**



# B0L001S, U17-ch38, adc2

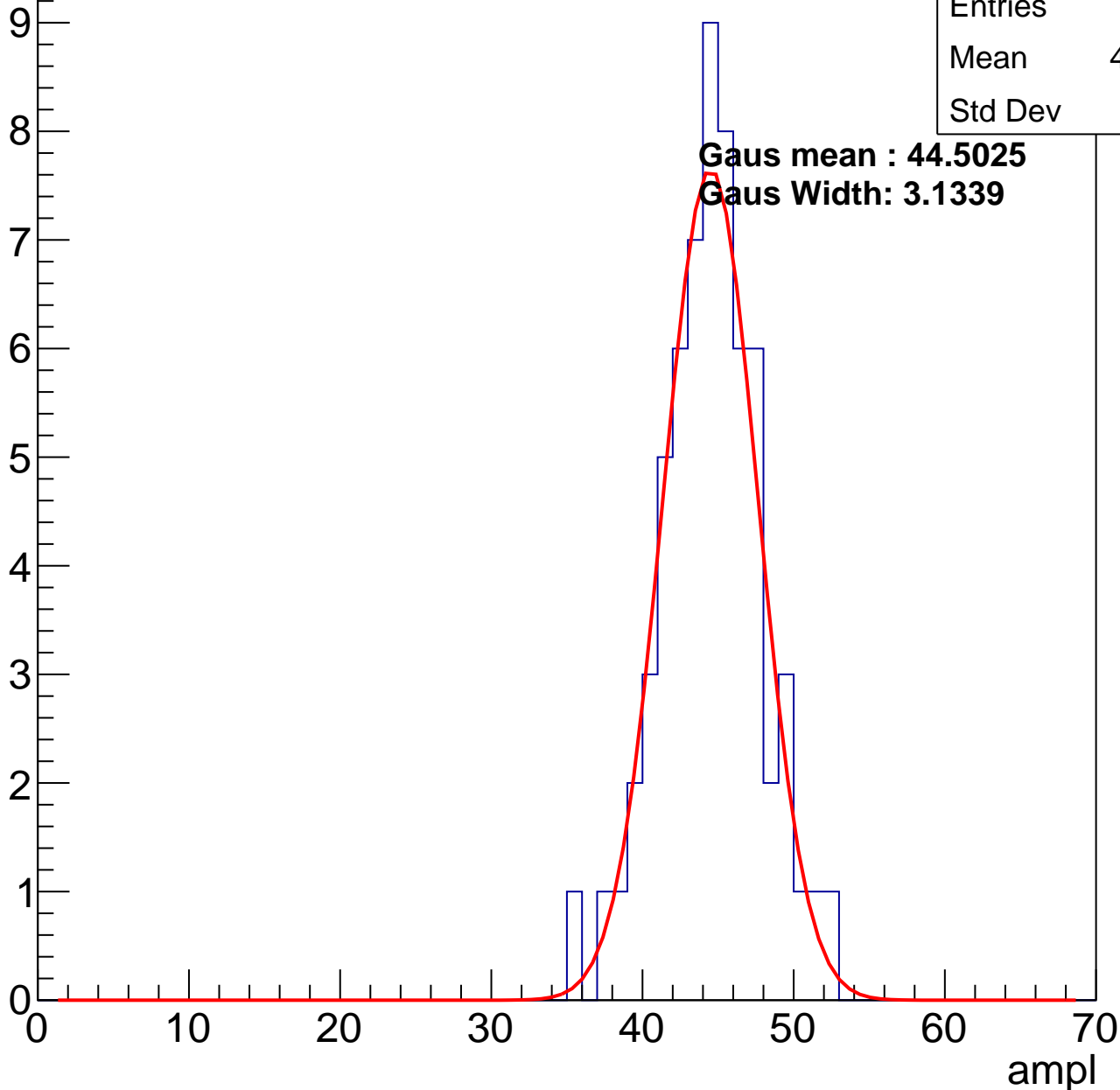
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	44.06
Std Dev	3.29

**Gaus mean : 44.5025**

**Gaus Width: 3.1339**

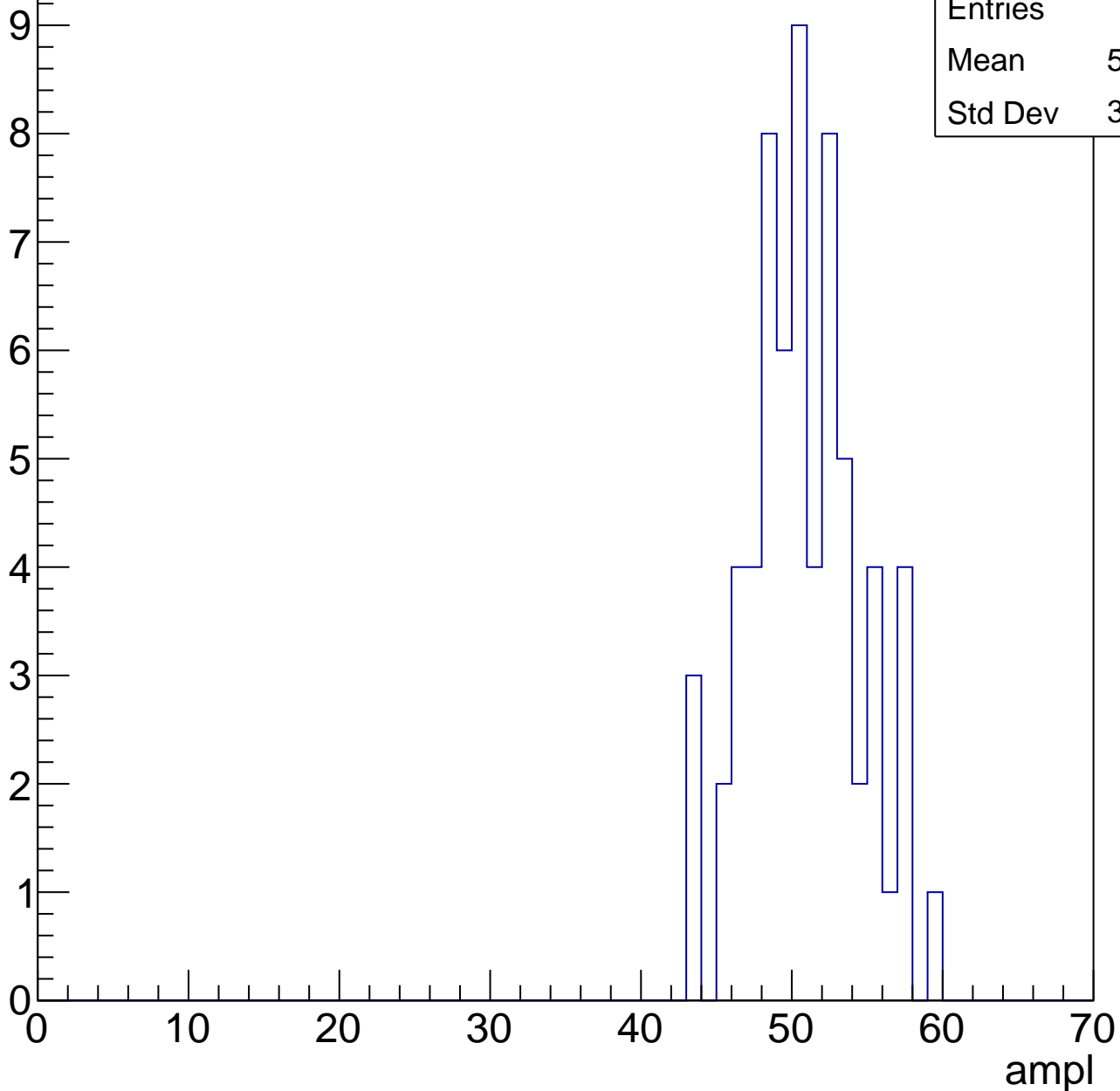


# B0L001S, U17-ch38, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	50.38
Std Dev	3.619

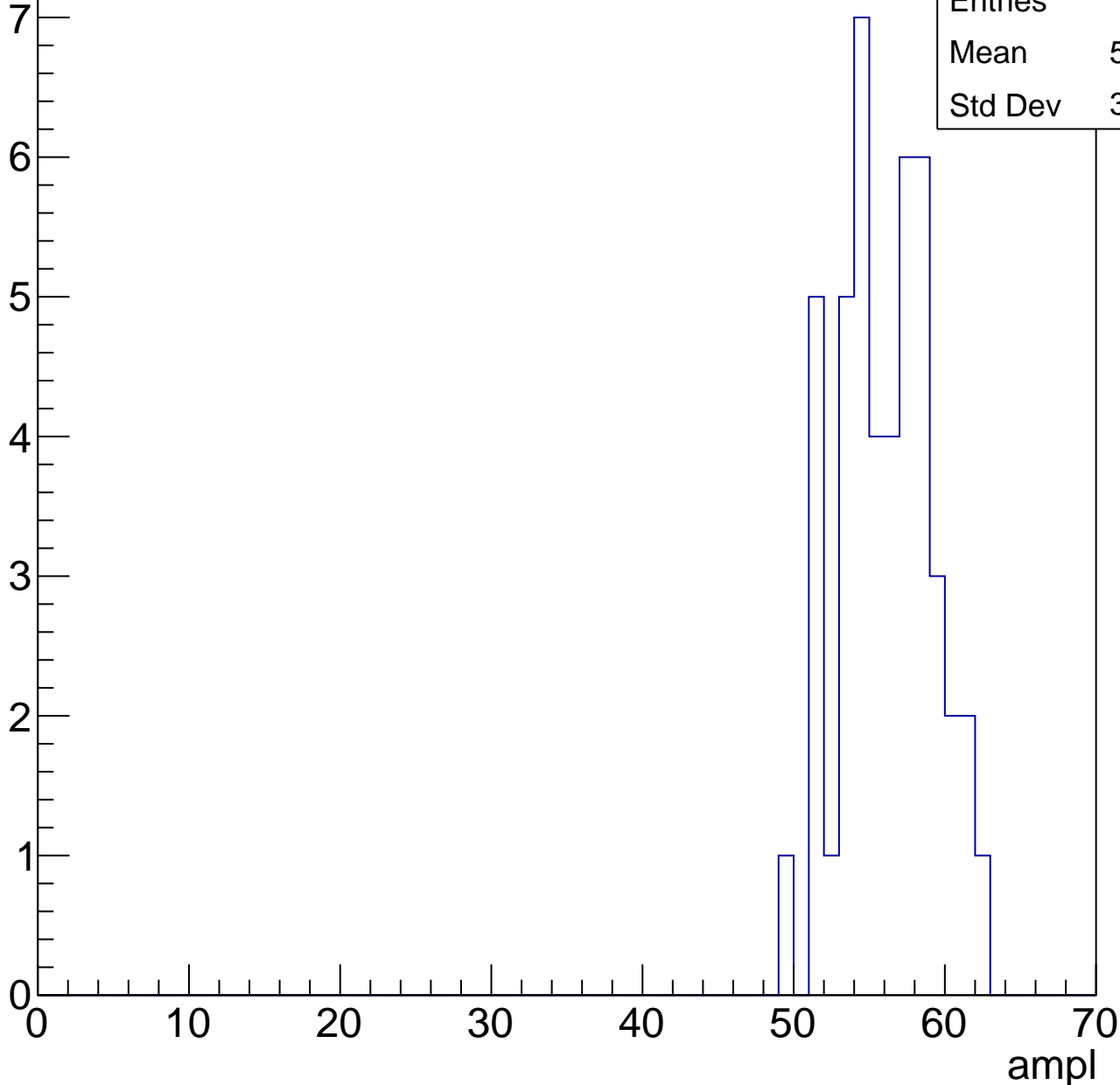


# B0L001S, U17-ch38, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	47
Mean	55.62
Std Dev	3.043



# B0L001S, U17-ch38, adc5

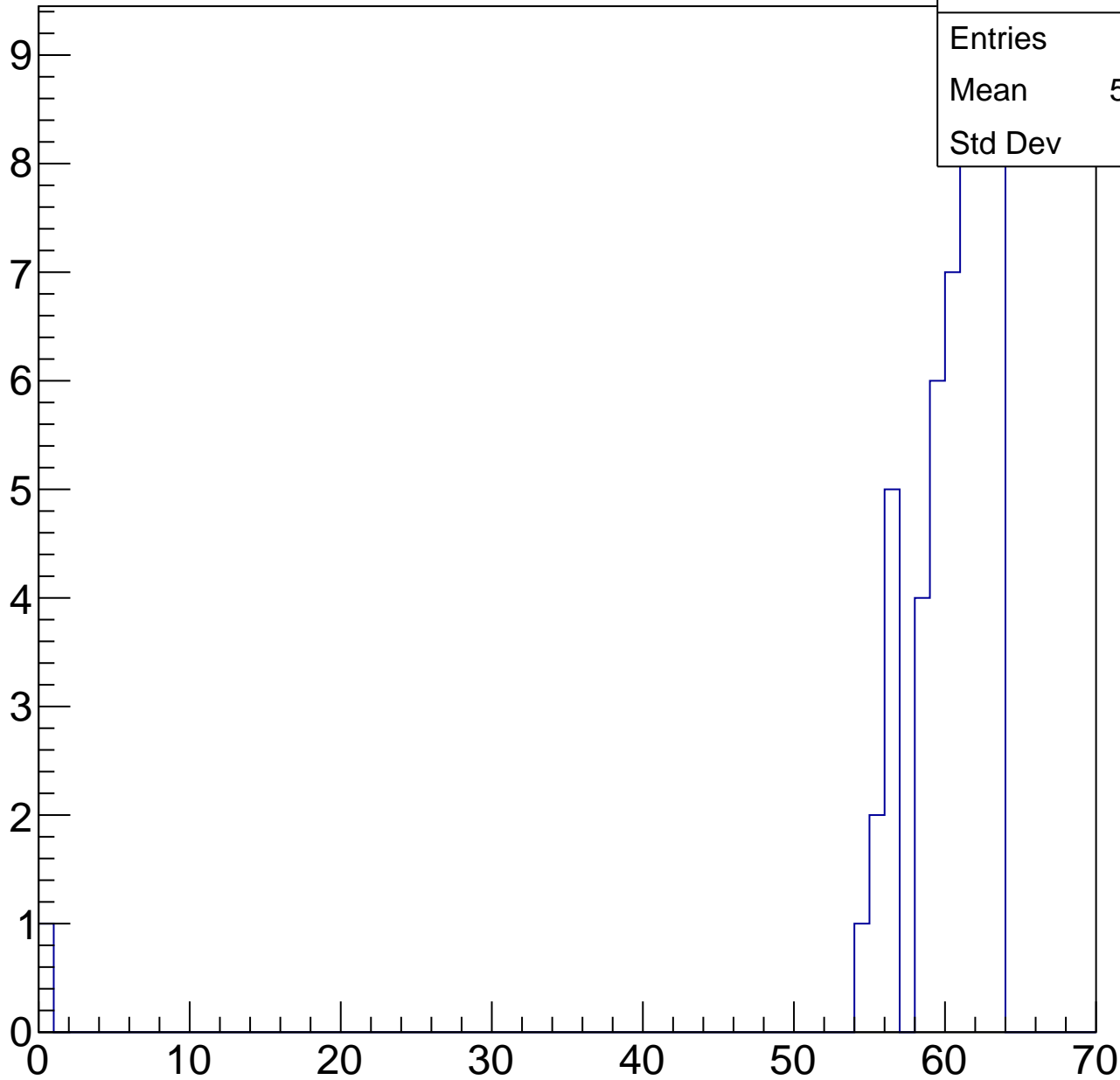
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	51
Mean	58.82
Std Dev	8.67

ampl



# B0L001S, U17-ch38, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch38, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U17-ch39, adc0

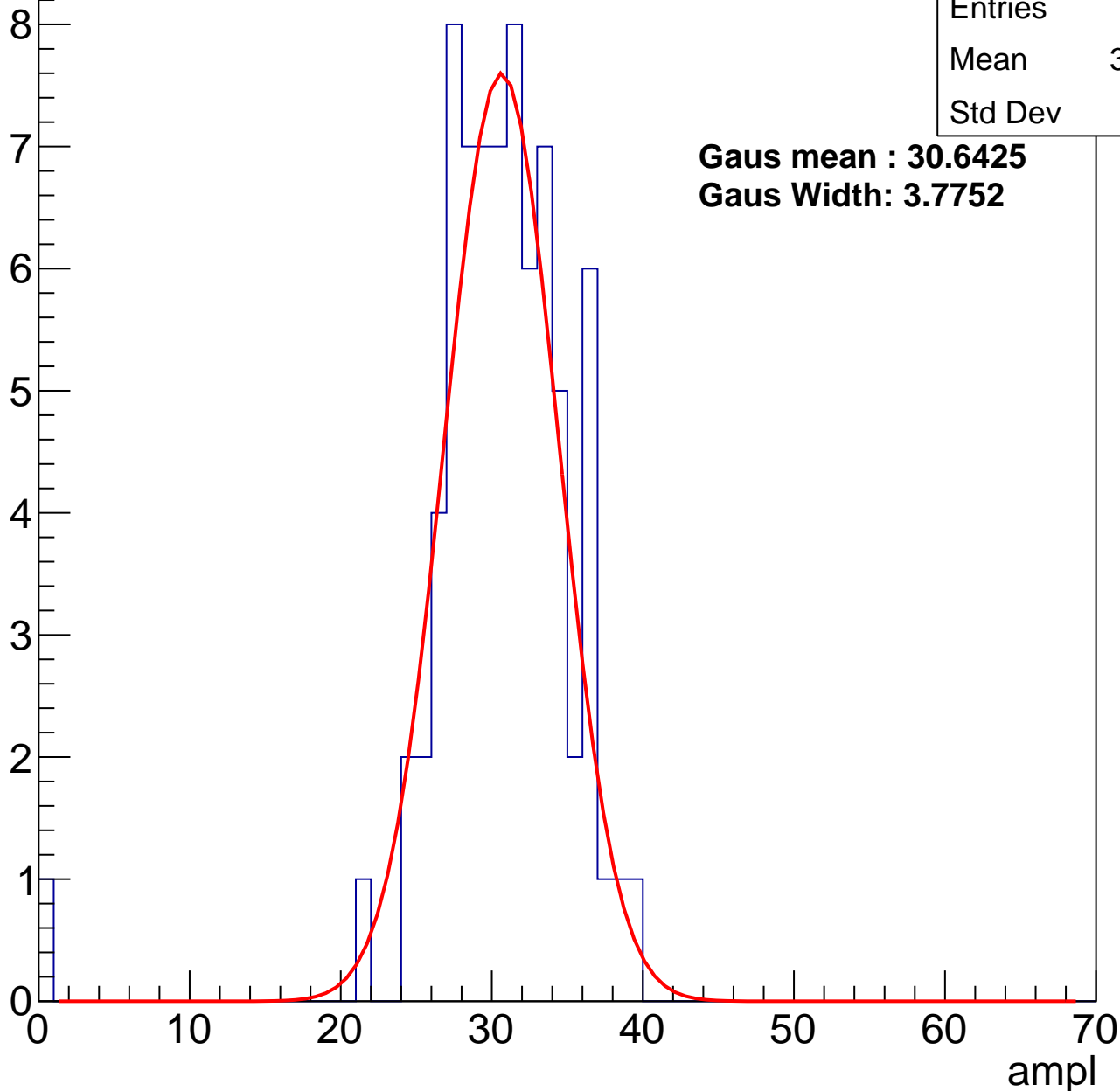
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	76
Mean	30.12
Std Dev	5.01

**Gaus mean : 30.6425**

**Gaus Width: 3.7752**



# B0L001S, U17-ch39, adc1

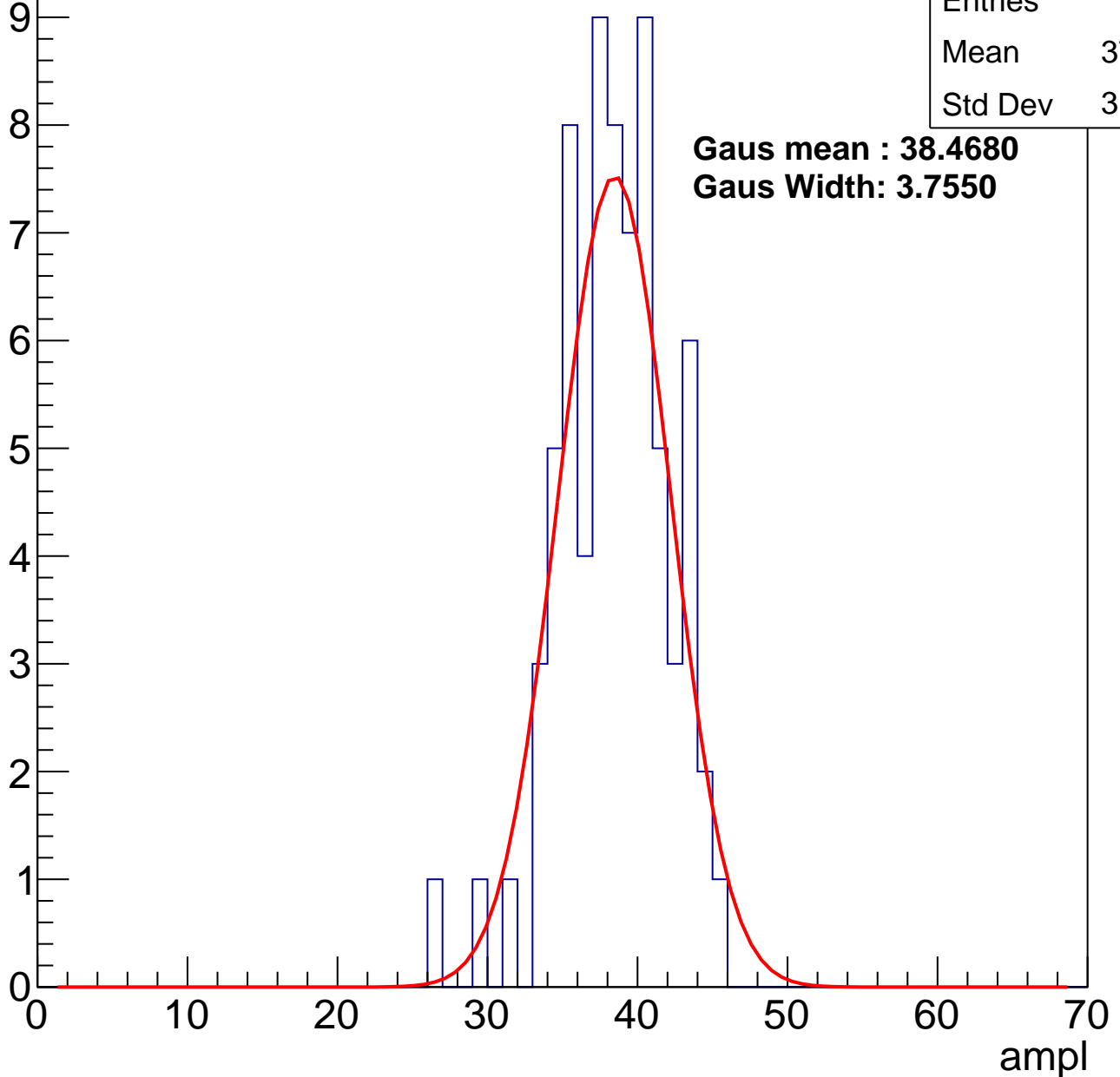
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	37.96
Std Dev	3.575

**Gaus mean : 38.4680**

**Gaus Width: 3.7550**



# B0L001S, U17-ch39, adc2

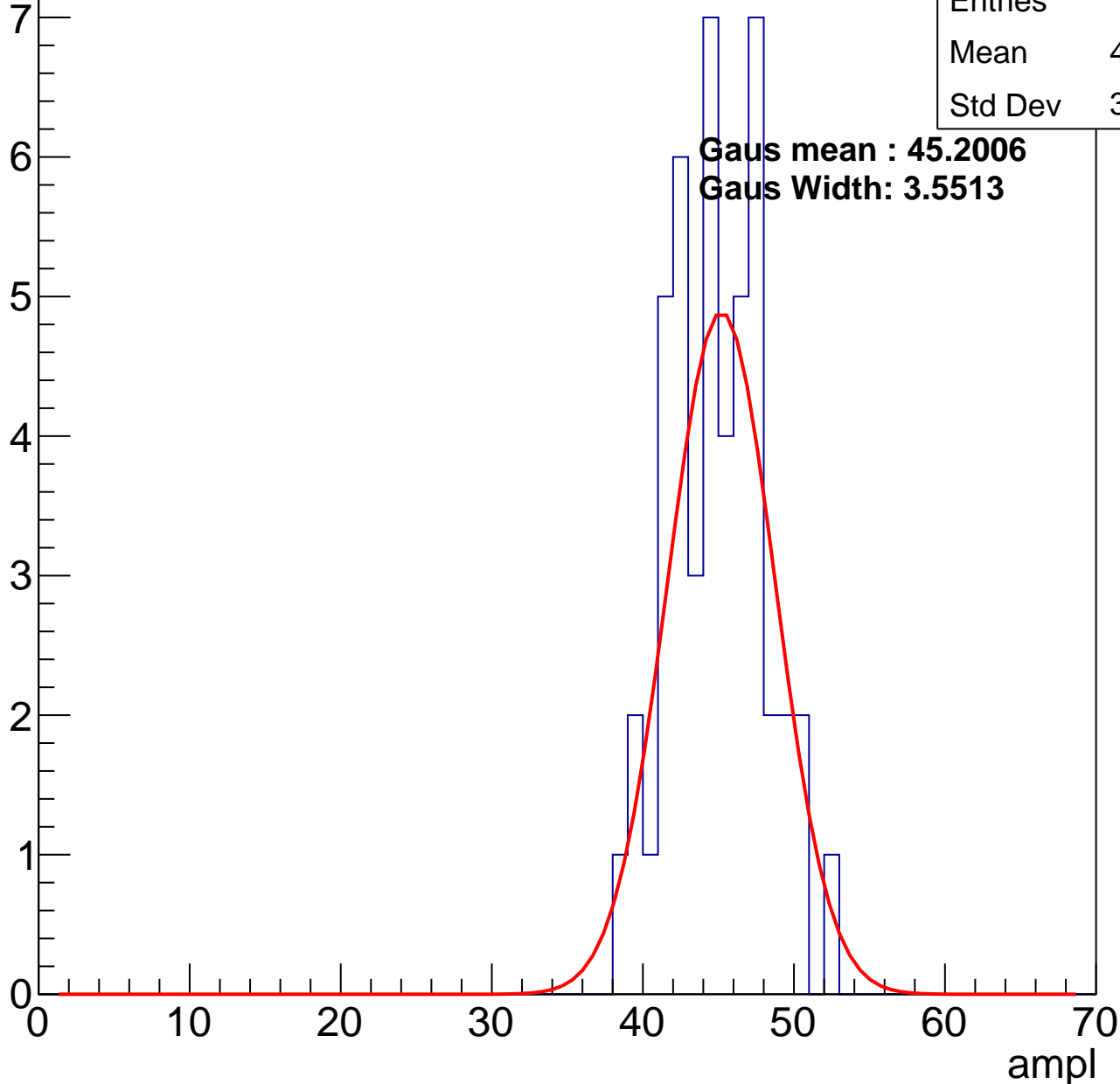
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	48
Mean	44.48
Std Dev	3.122

**Gaus mean : 45.2006**

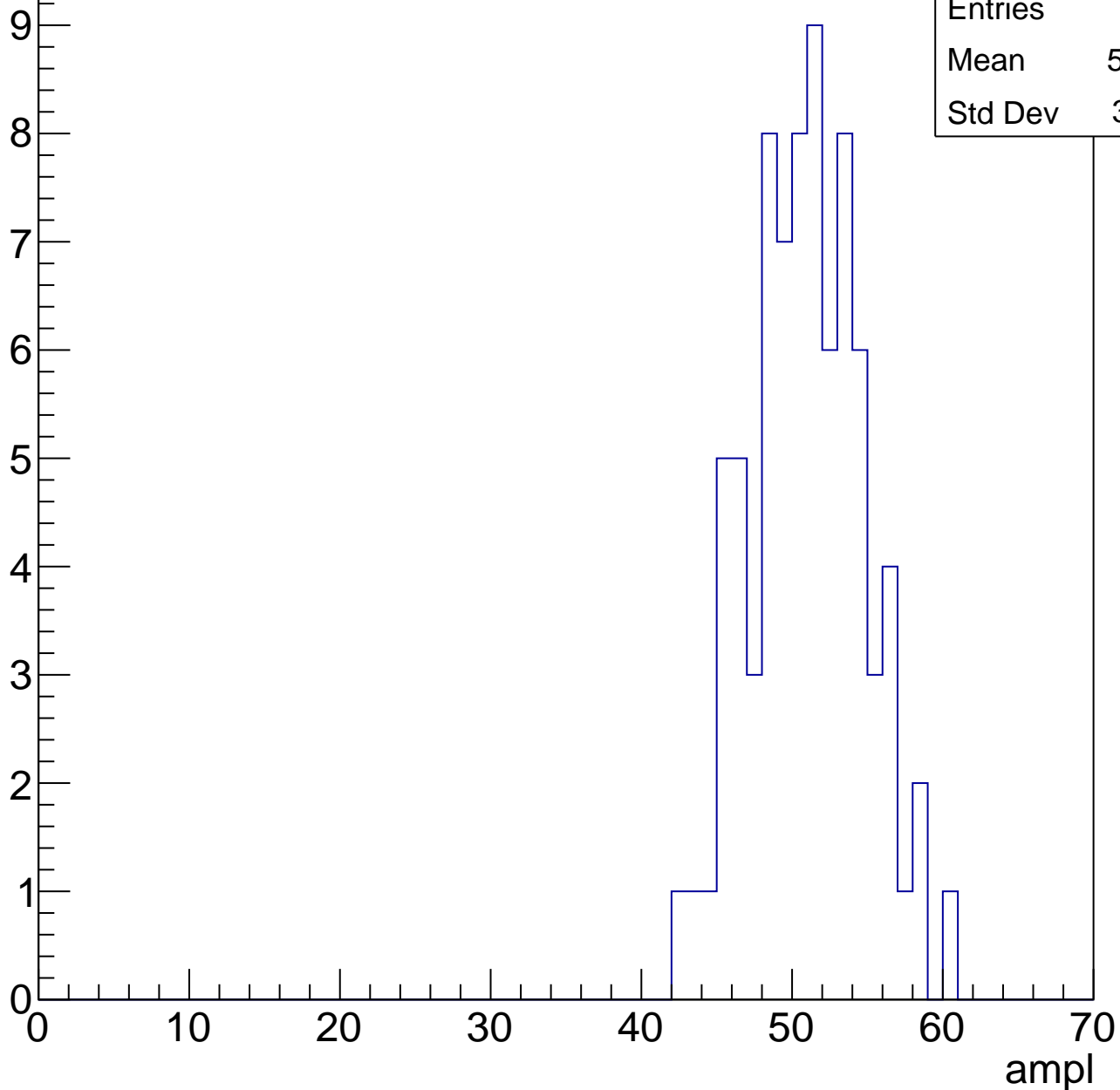
**Gaus Width: 3.5513**



# B0L001S, U17-ch39, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

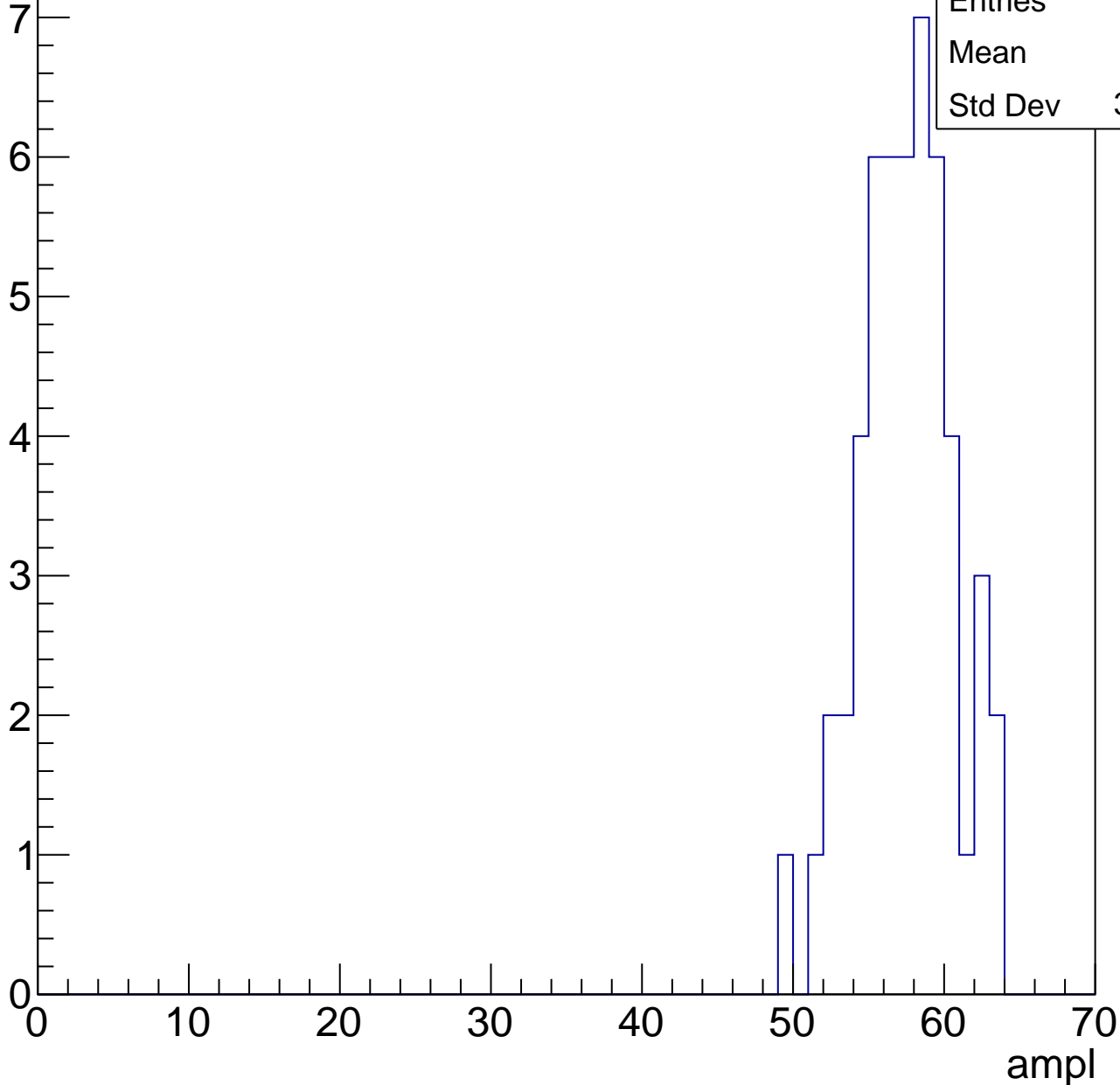


# B0L001S, U17-ch39, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	51
Mean	57
Std Dev	3.061

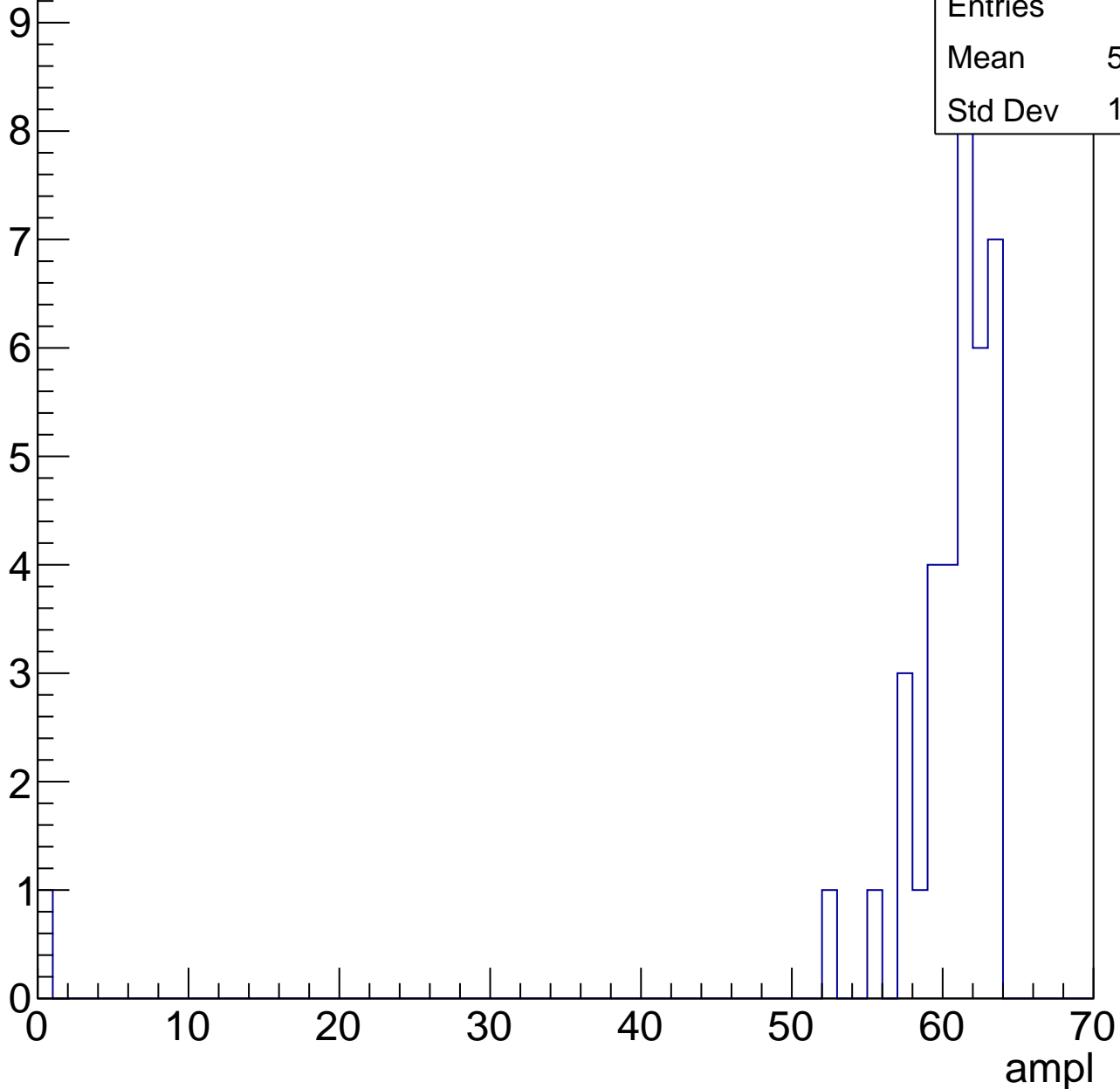


# B0L001S, U17-ch39, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

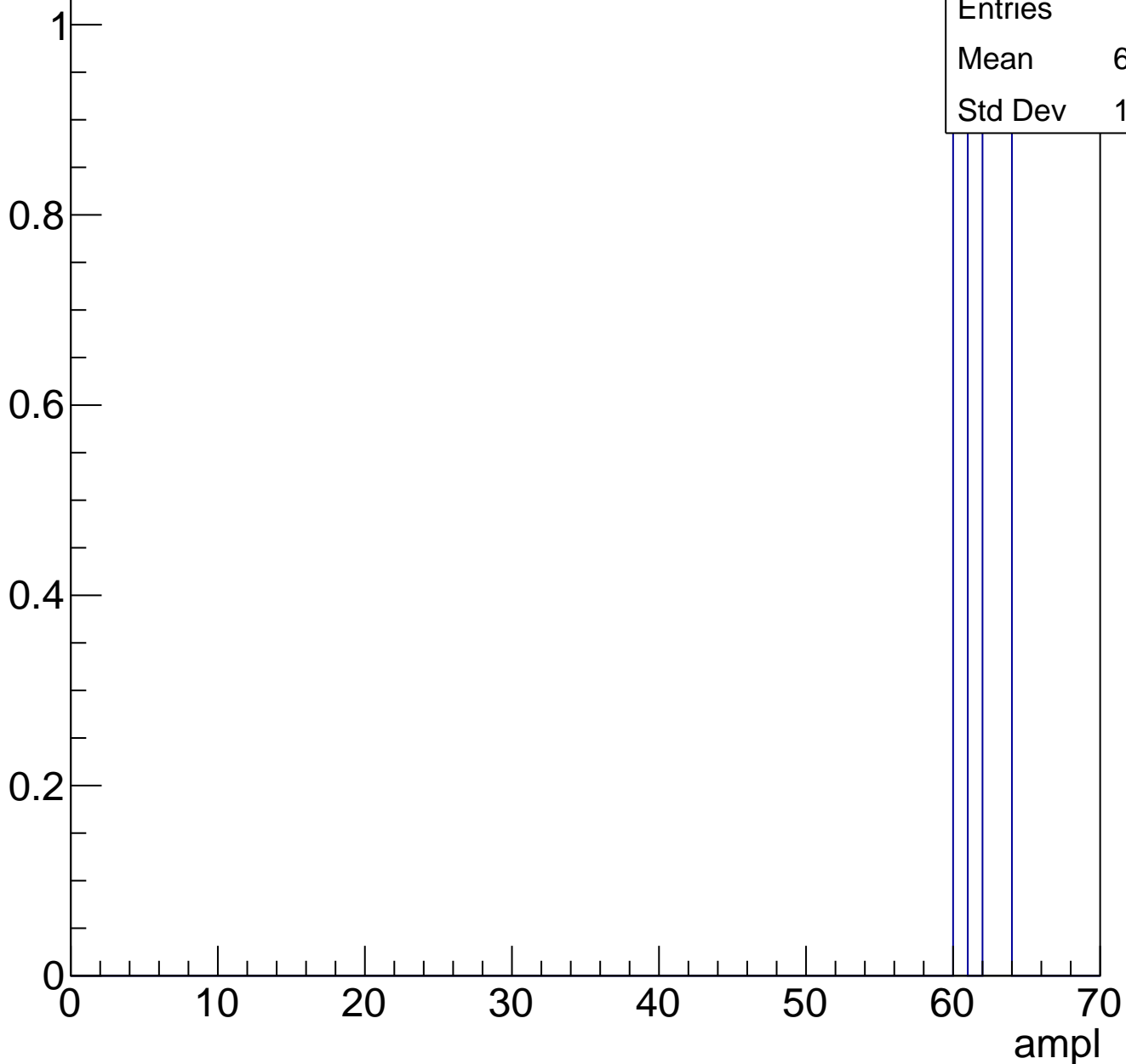
Entries	37
Mean	58.76
Std Dev	10.08



# B0L001S, U17-ch39, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch39, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L001S, U17-ch40, adc0

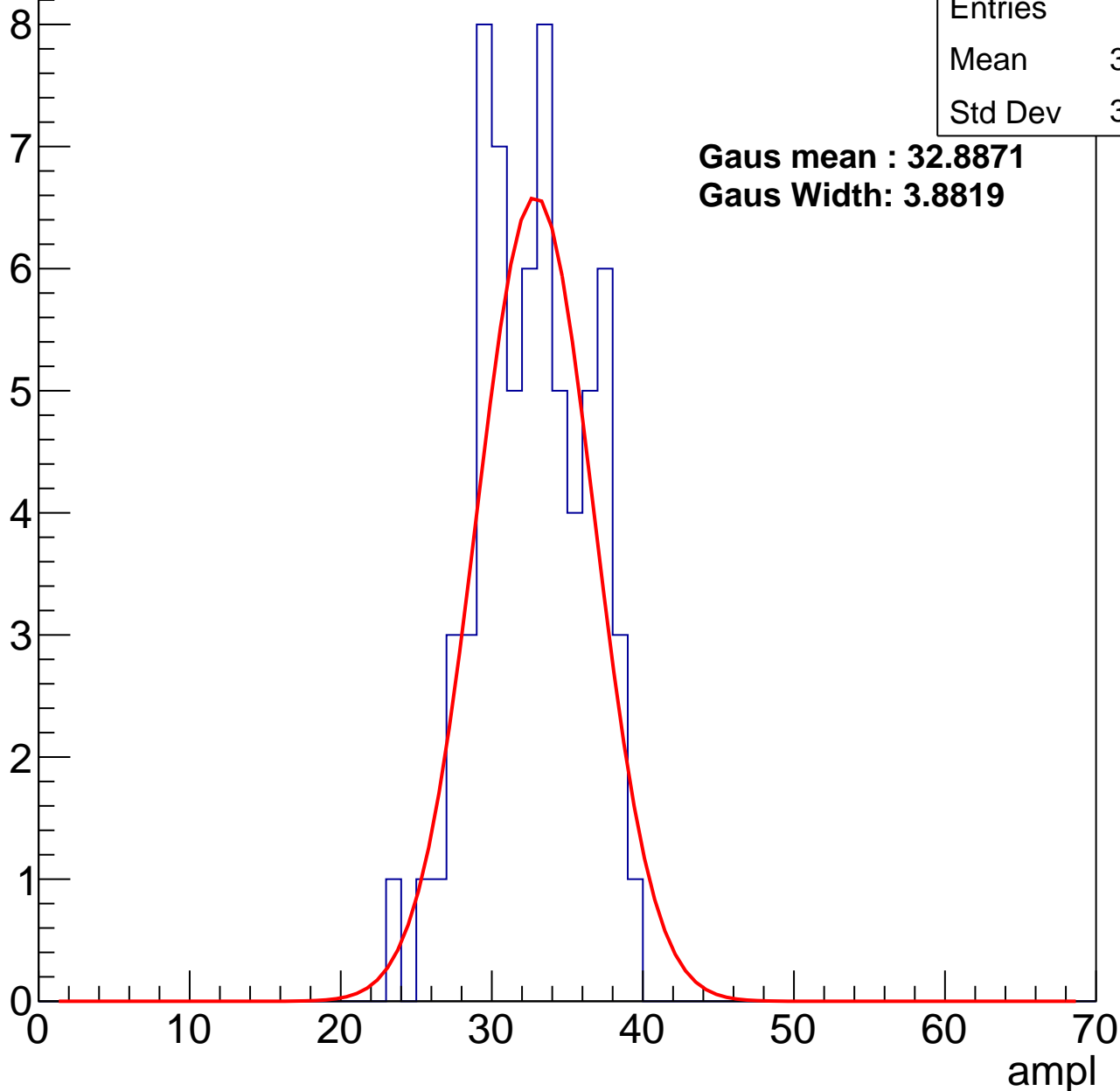
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	32.19
Std Dev	3.546

**Gaus mean : 32.8871**

**Gaus Width: 3.8819**



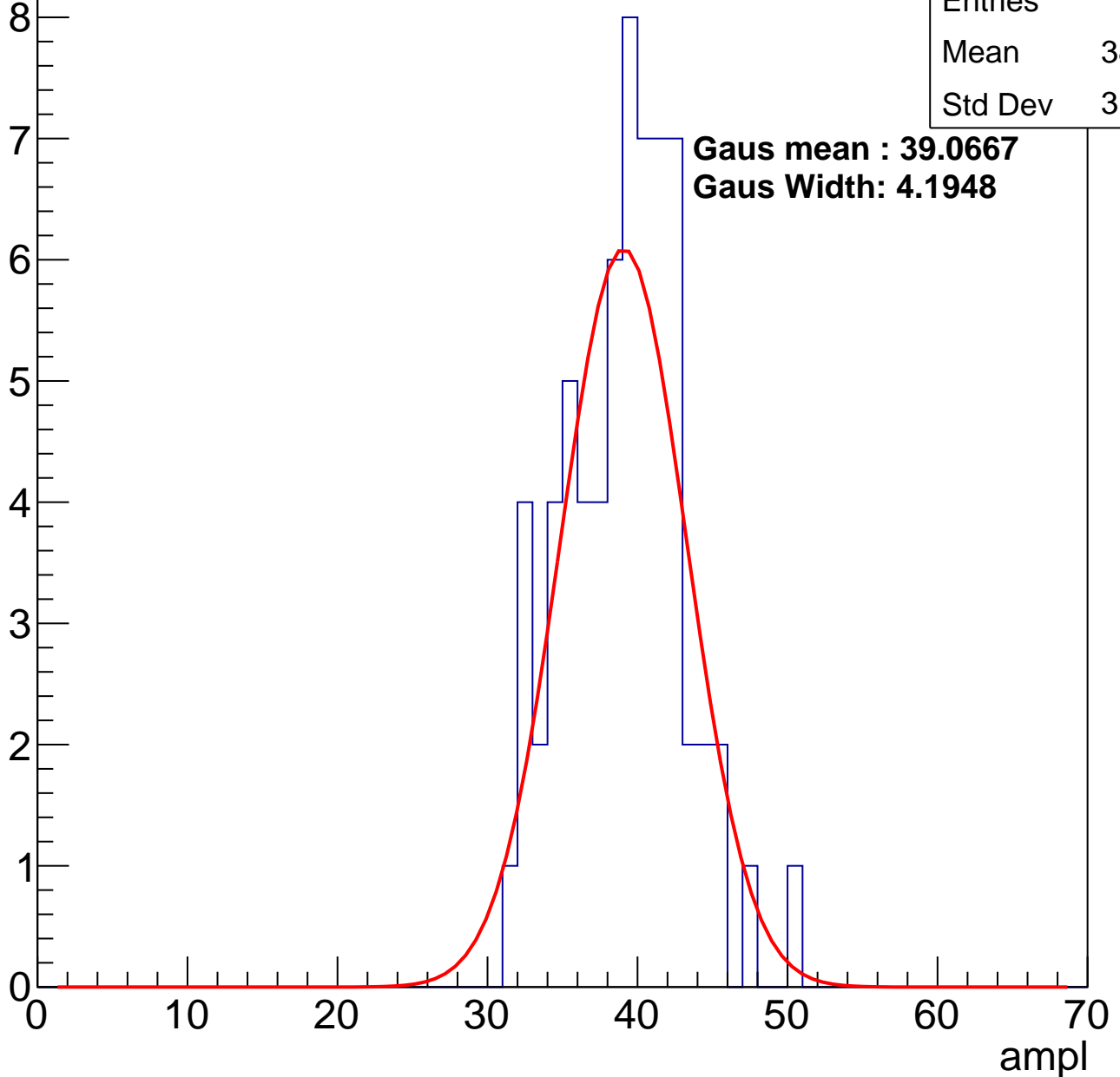
# B0L001S, U17-ch40, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	38.66
Std Dev	3.862

**Gaus mean : 39.0667**  
**Gaus Width: 4.1948**



# B0L001S, U17-ch40, adc2

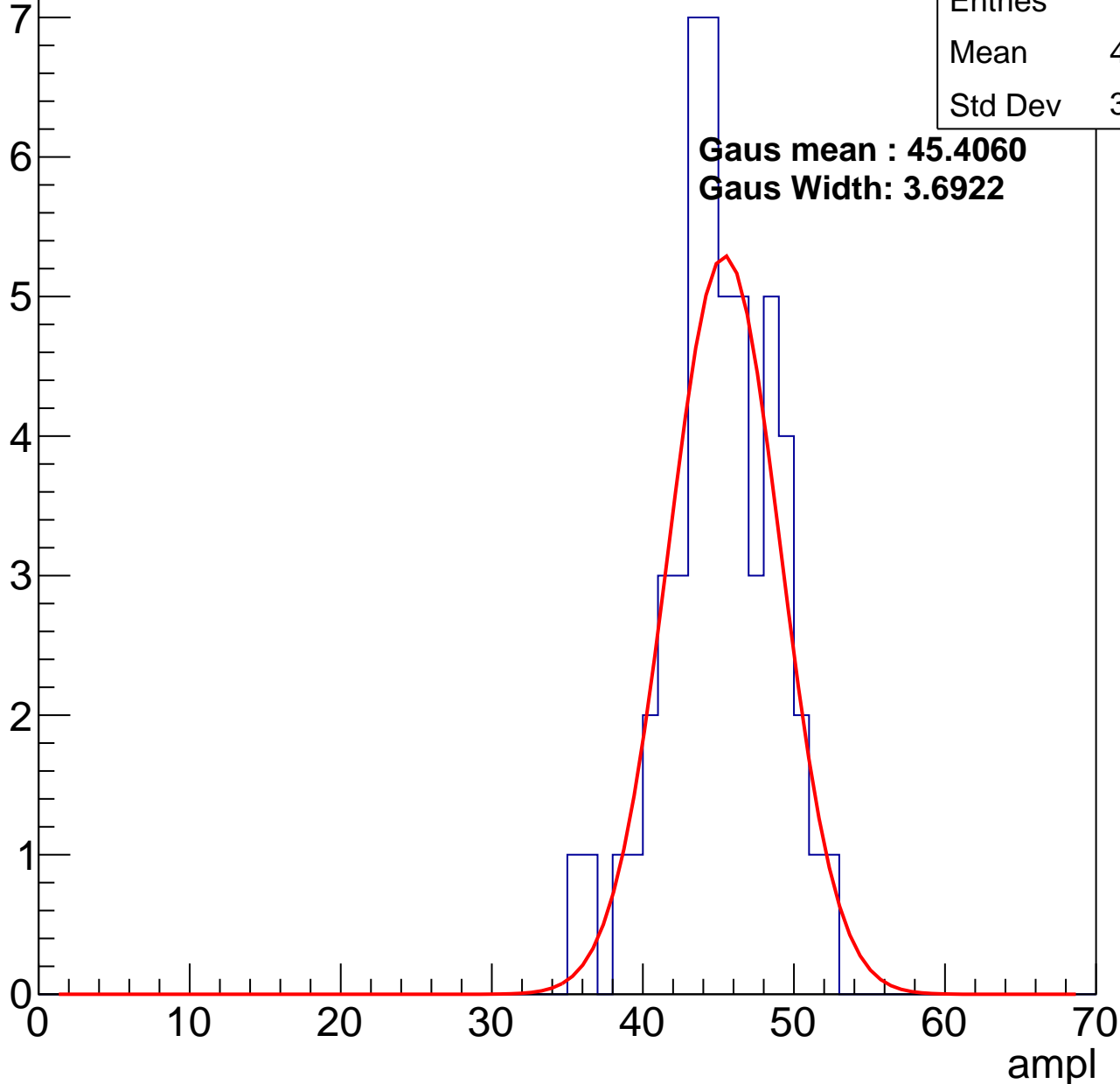
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	44.63
Std Dev	3.616

**Gaus mean : 45.4060**

**Gaus Width: 3.6922**

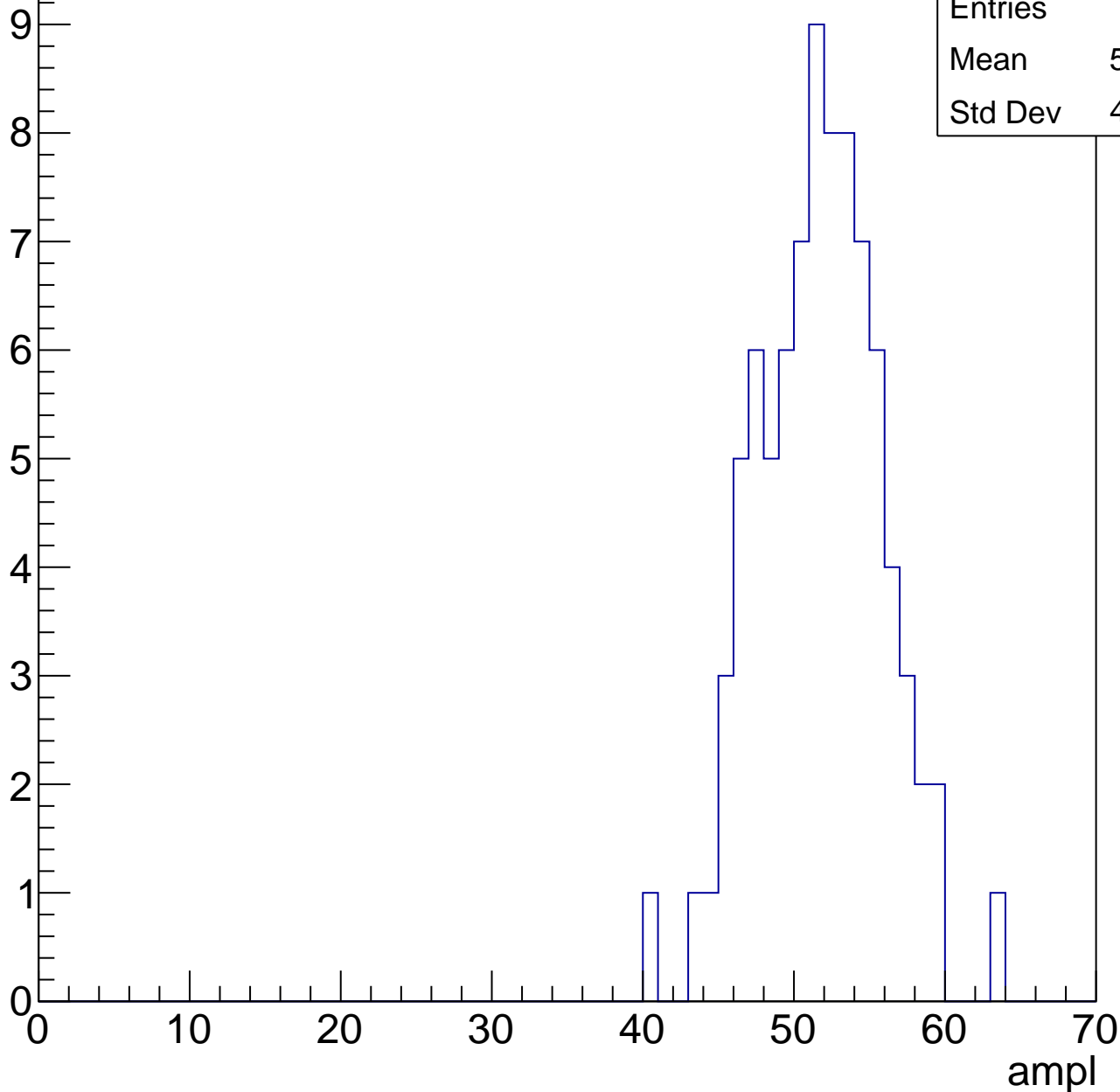


# B0L001S, U17-ch40, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	85
Mean	51.26
Std Dev	4.073

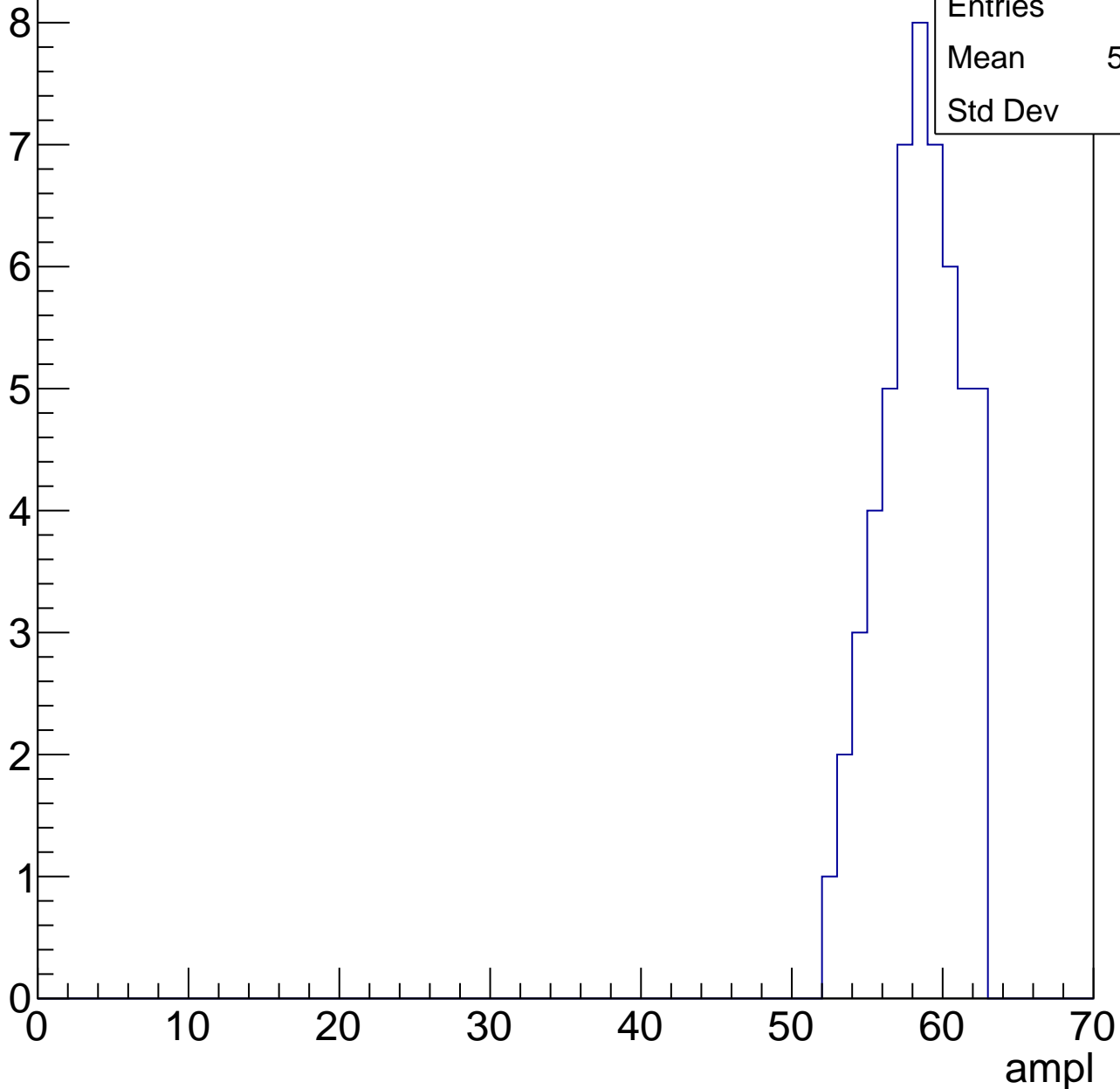


# B0L001S, U17-ch40, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	57.94
Std Dev	2.58

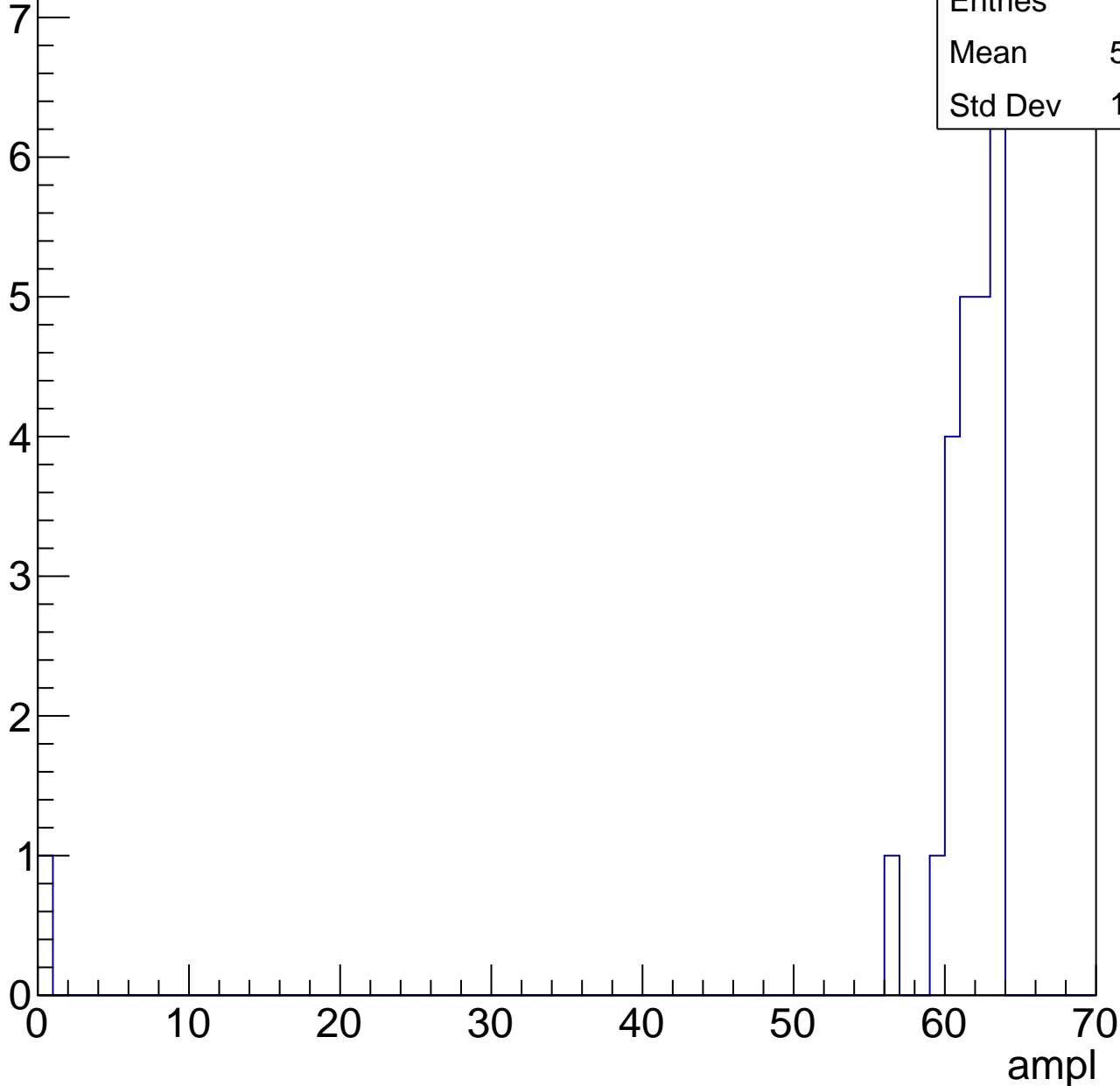


# B0L001S, U17-ch40, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	24
Mean	58.79
Std Dev	12.37



# B0L001S, U17-ch40, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	63
Std Dev	0

0 10 20 30 40 50 60 70

ampl



# B0L001S, U17-ch40, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U17-ch41, adc0

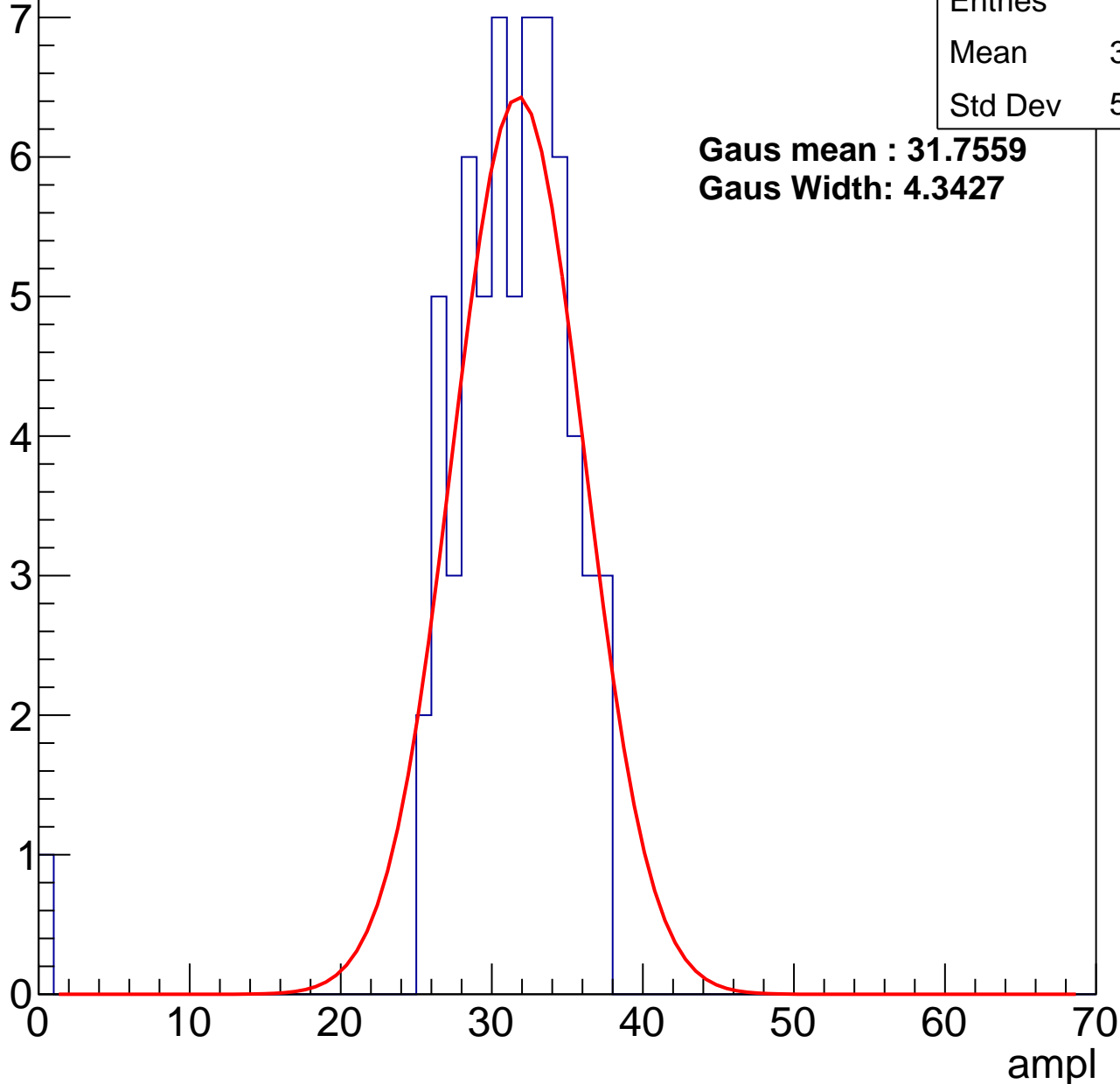
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	30.58
Std Dev	5.018

**Gaus mean : 31.7559**

**Gaus Width: 4.3427**

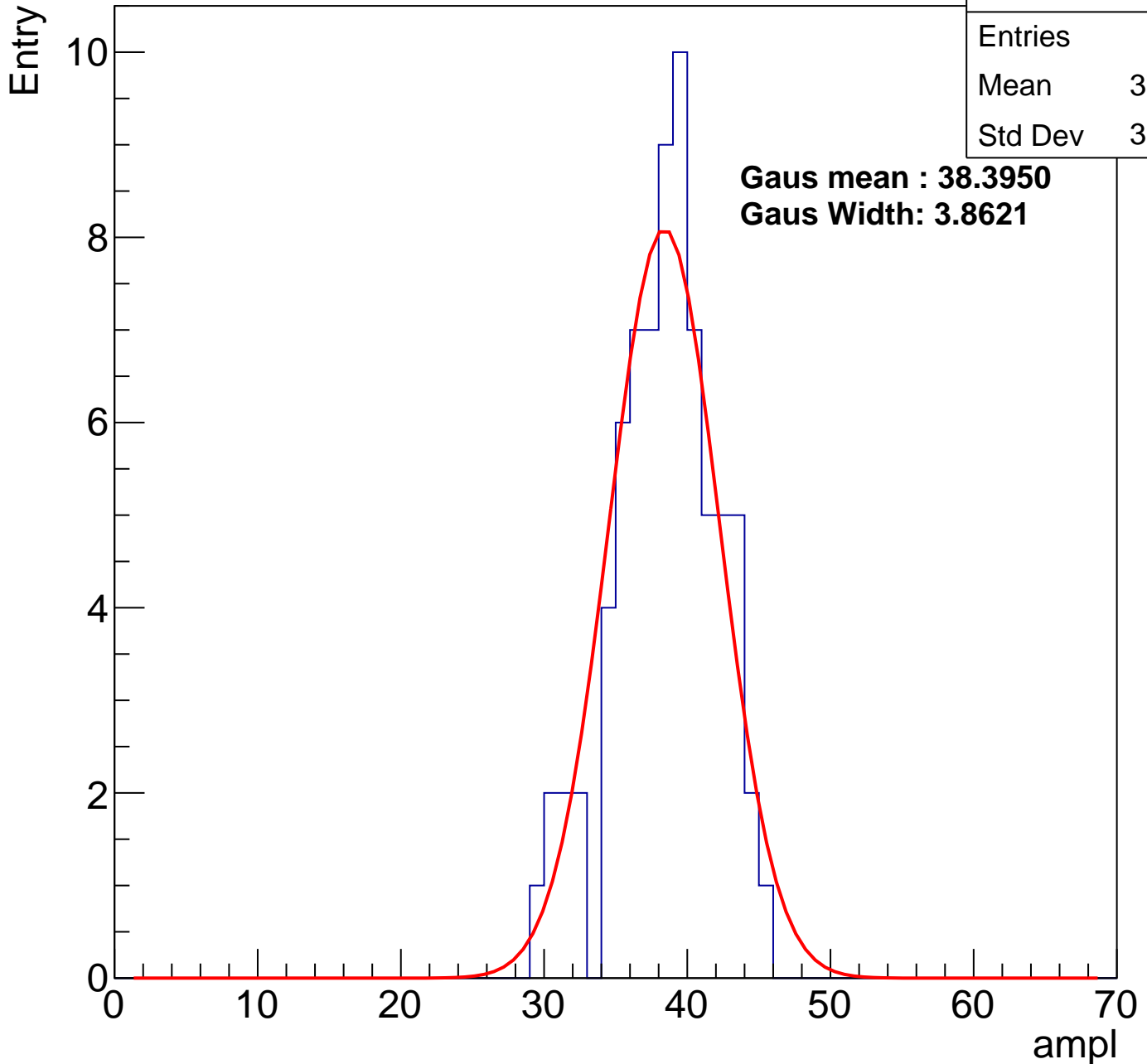


# B0L001S, U17-ch41, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	75
Mean	37.96
Std Dev	3.542

**Gaus mean : 38.3950**  
**Gaus Width: 3.8621**



# B0L001S, U17-ch41, adc2

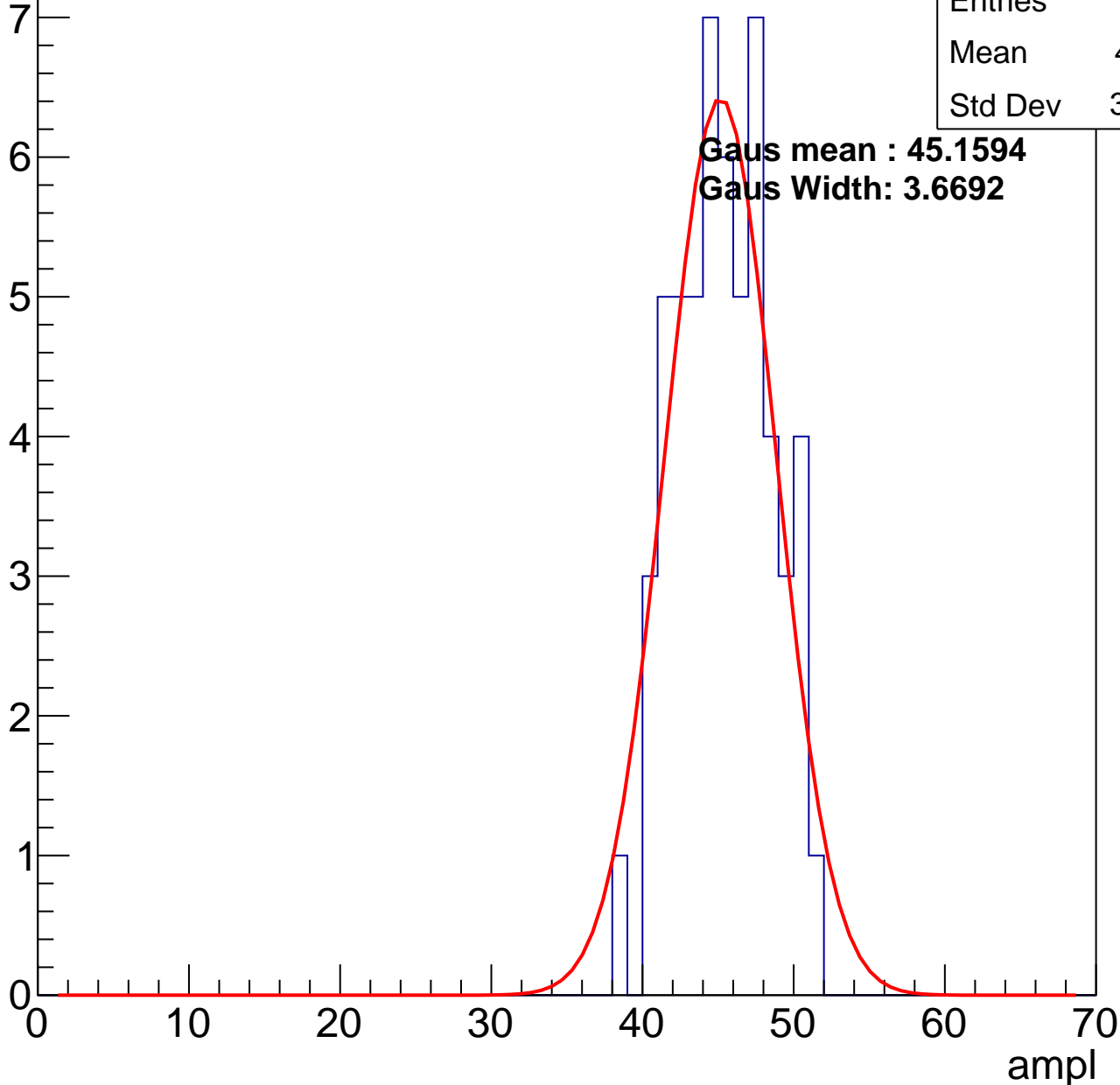
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	44.91
Std Dev	3.072

**Gaus mean : 45.1594**

**Gaus Width: 3.6692**

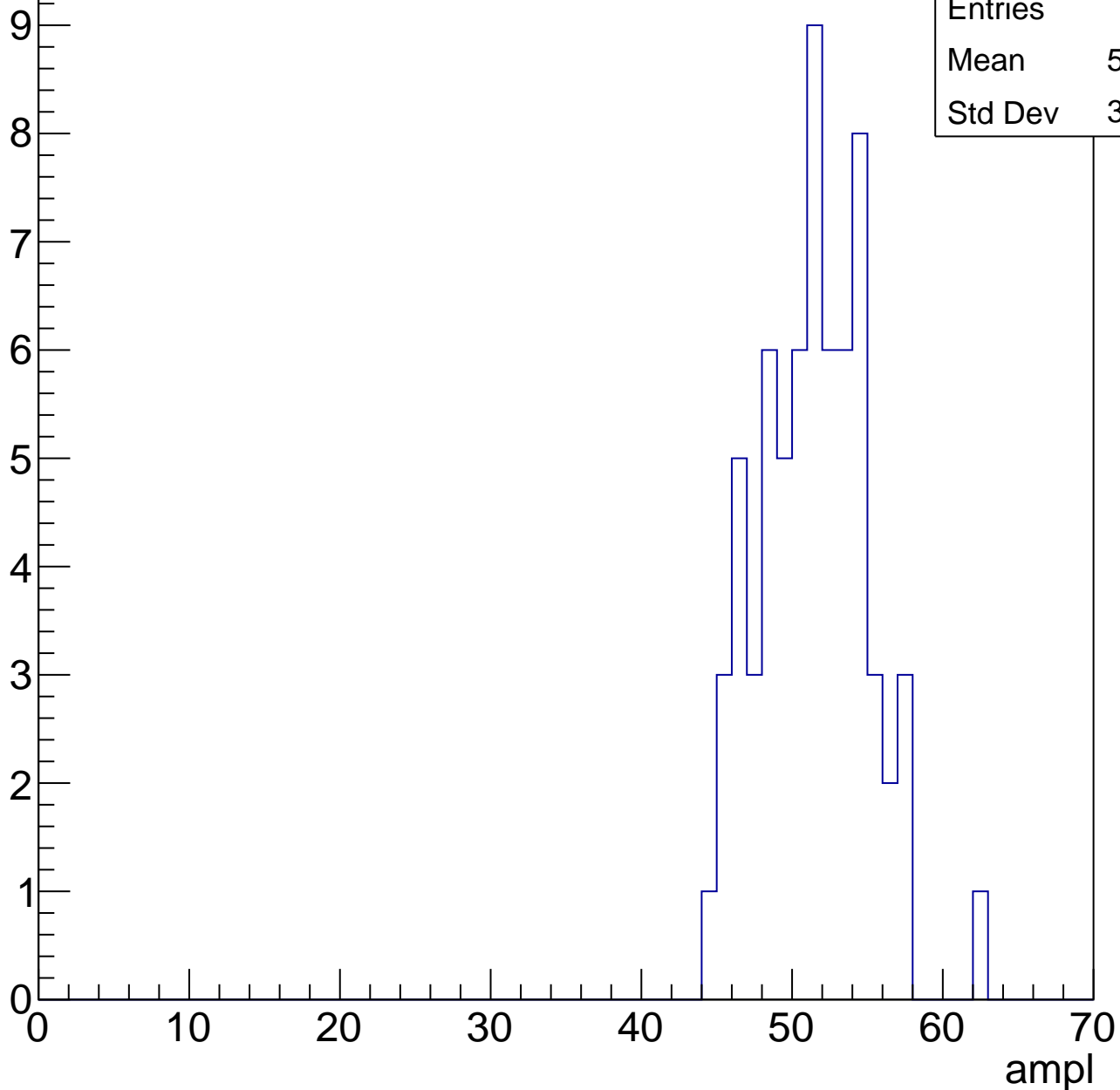


# B0L001S, U17-ch41, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	50.96
Std Dev	3.538

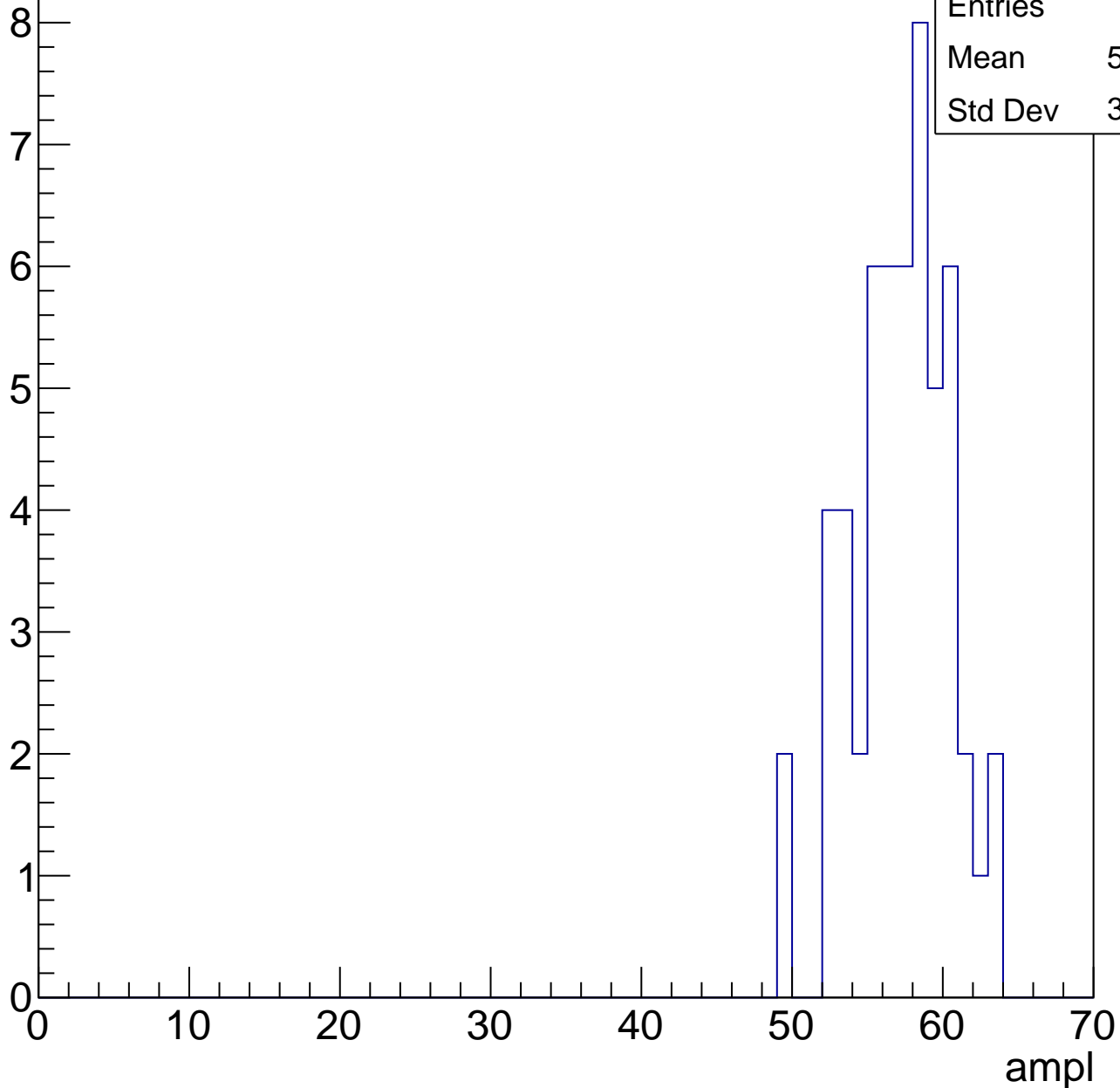


# B0L001S, U17-ch41, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	56.72
Std Dev	3.182

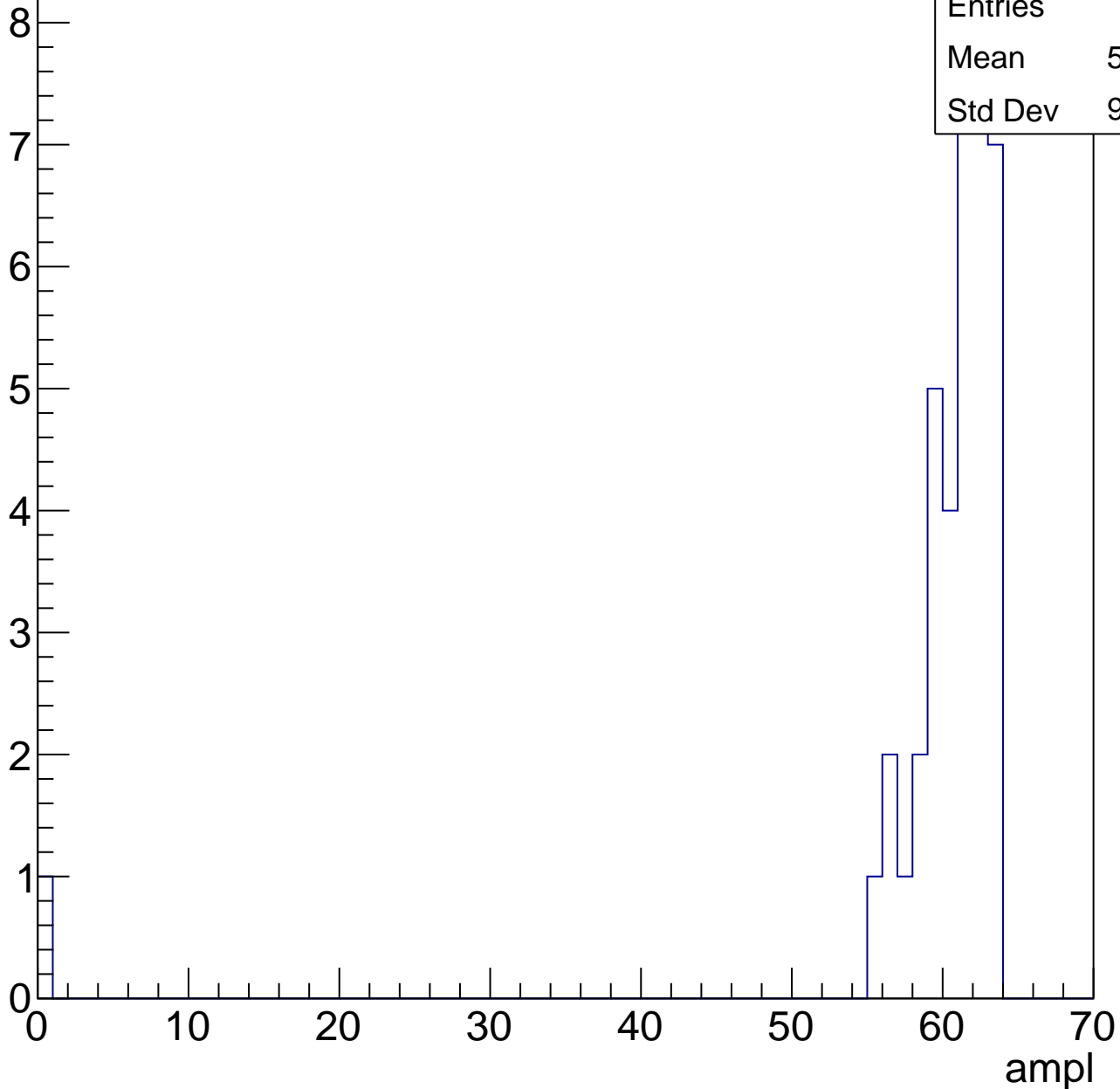


# B0L001S, U17-ch41, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	39
Mean	58.97
Std Dev	9.794



# B0L001S, U17-ch41, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	63
Std Dev	0



# B0L001S, U17-ch41, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U17-ch42, adc0

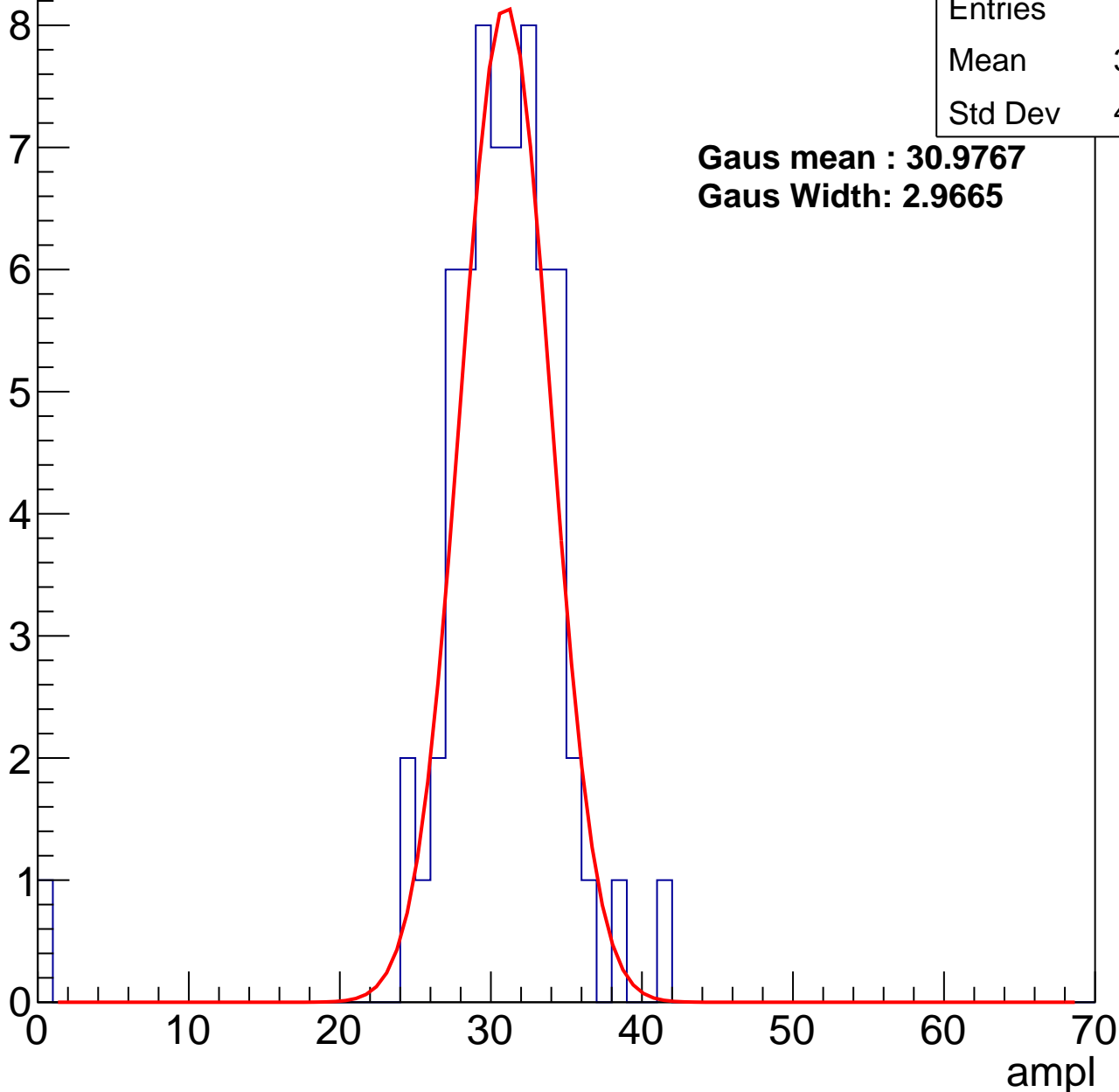
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	30.11
Std Dev	4.921

**Gaus mean : 30.9767**

**Gaus Width: 2.9665**



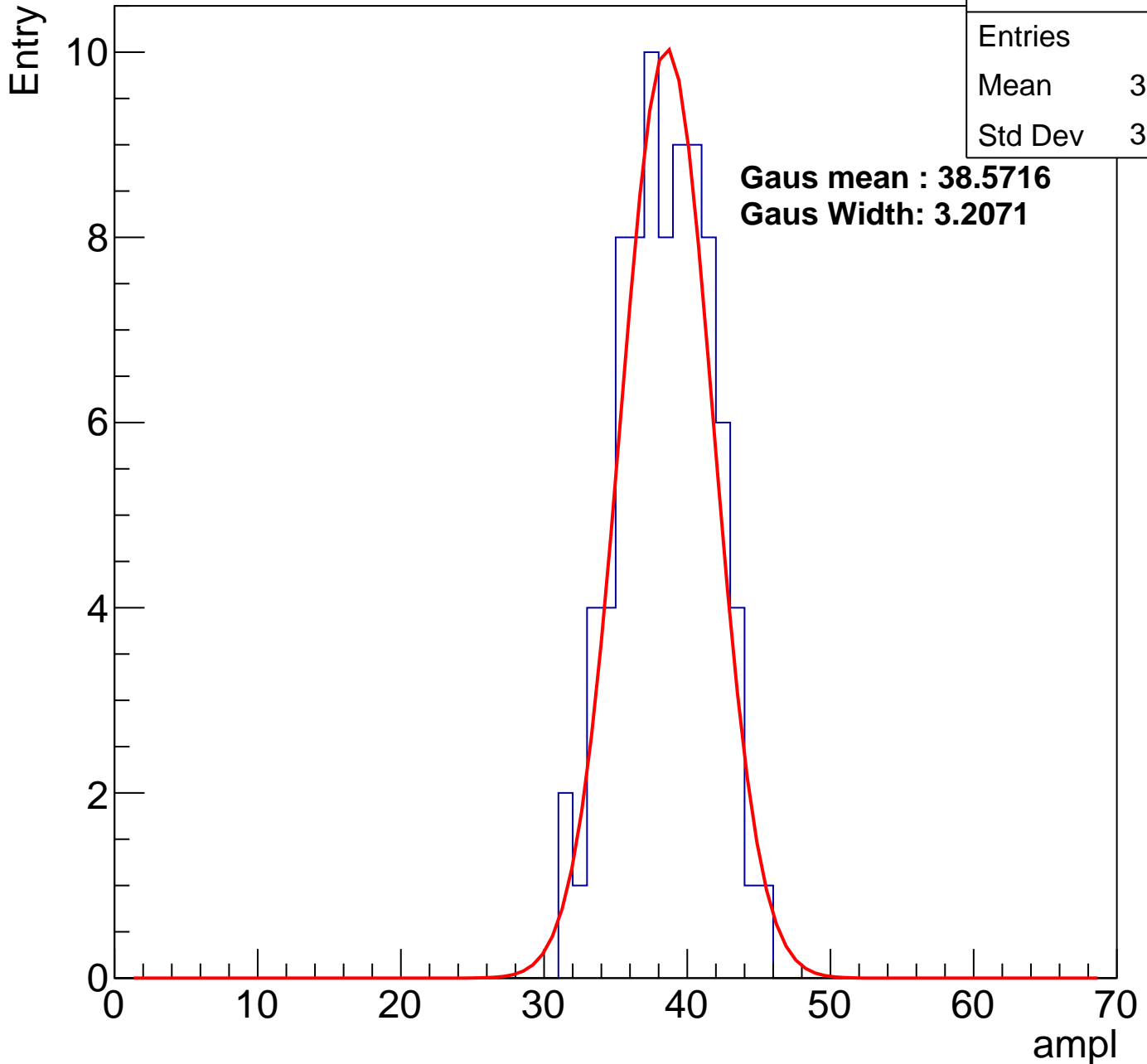
# B0L001S, U17-ch42, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	83
Mean	38.02
Std Dev	3.124

**Gaus mean : 38.5716**

**Gaus Width: 3.2071**



# B0L001S, U17-ch42, adc2

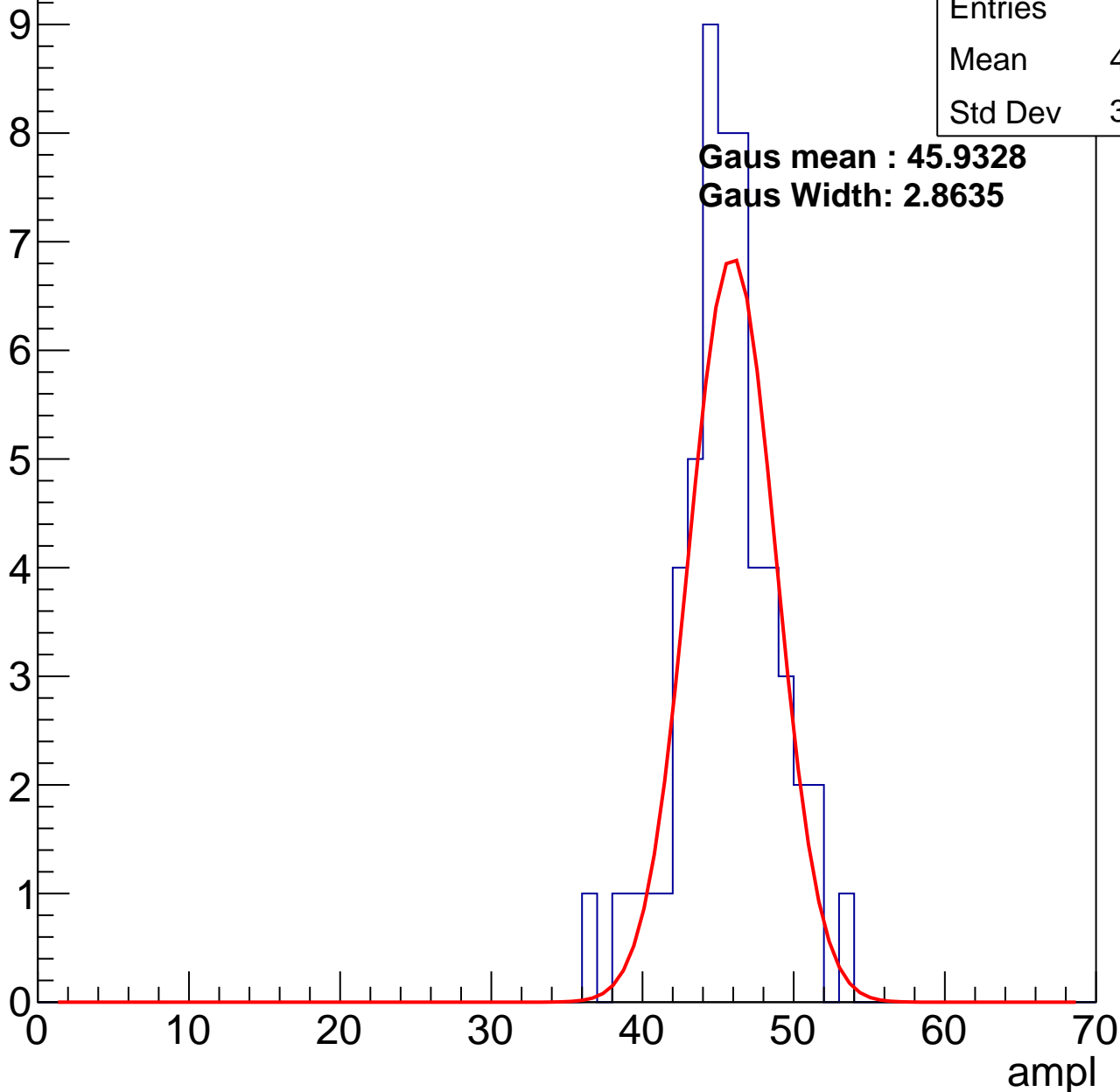
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	45.15
Std Dev	3.205

**Gaus mean : 45.9328**

**Gaus Width: 2.8635**

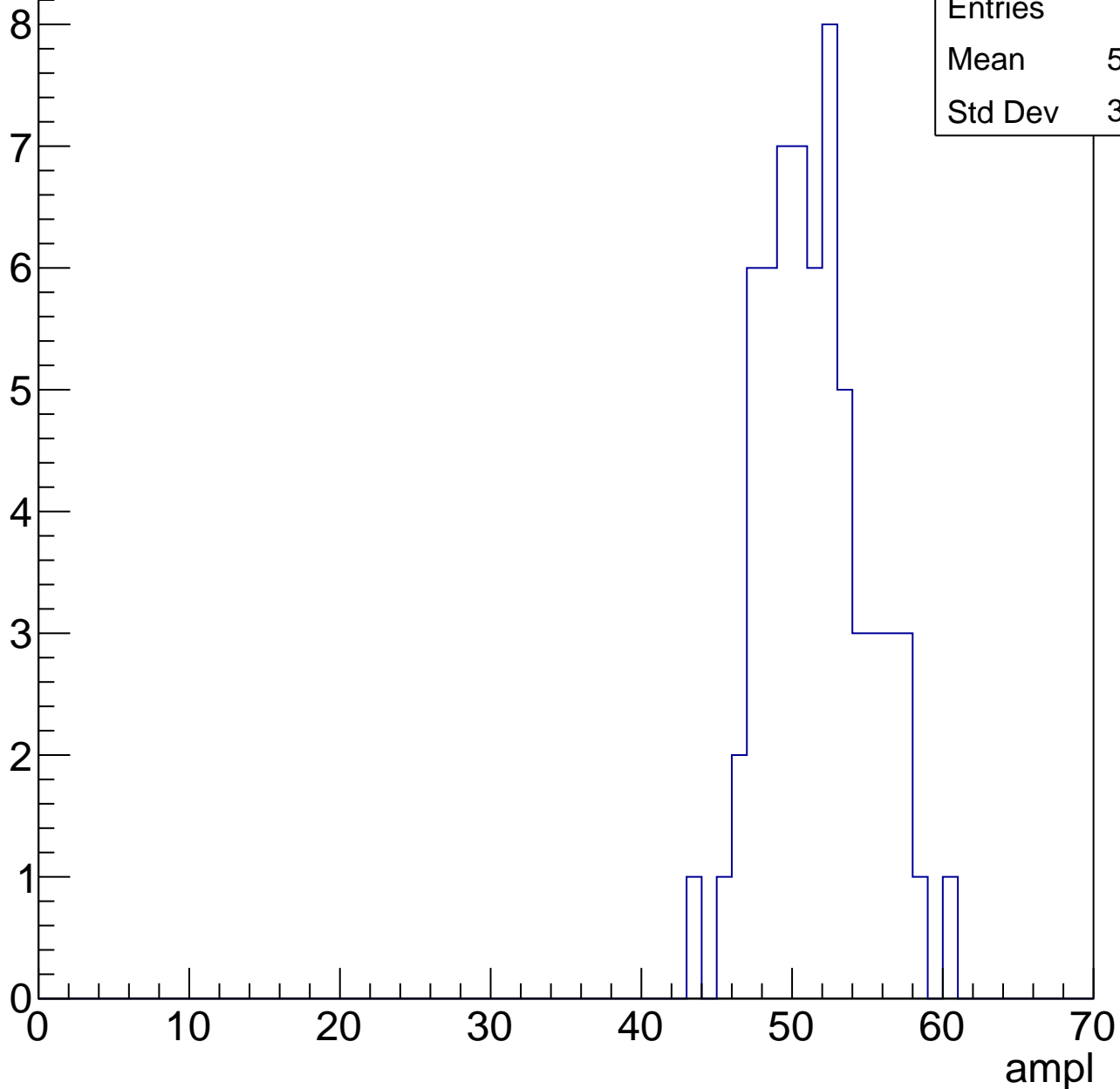


# B0L001S, U17-ch42, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	51.02
Std Dev	3.453

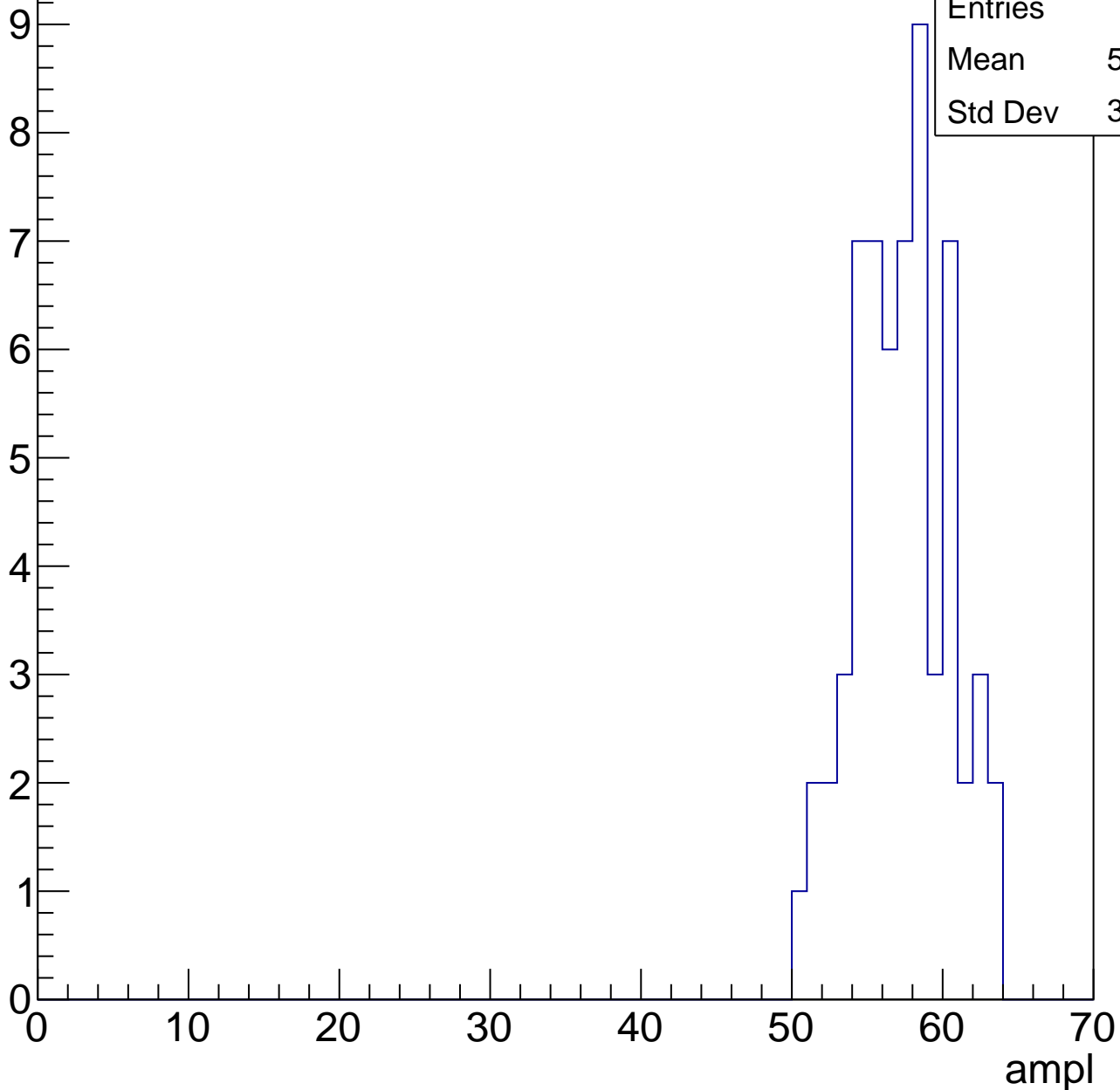


# B0L001S, U17-ch42, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	56.82
Std Dev	3.076

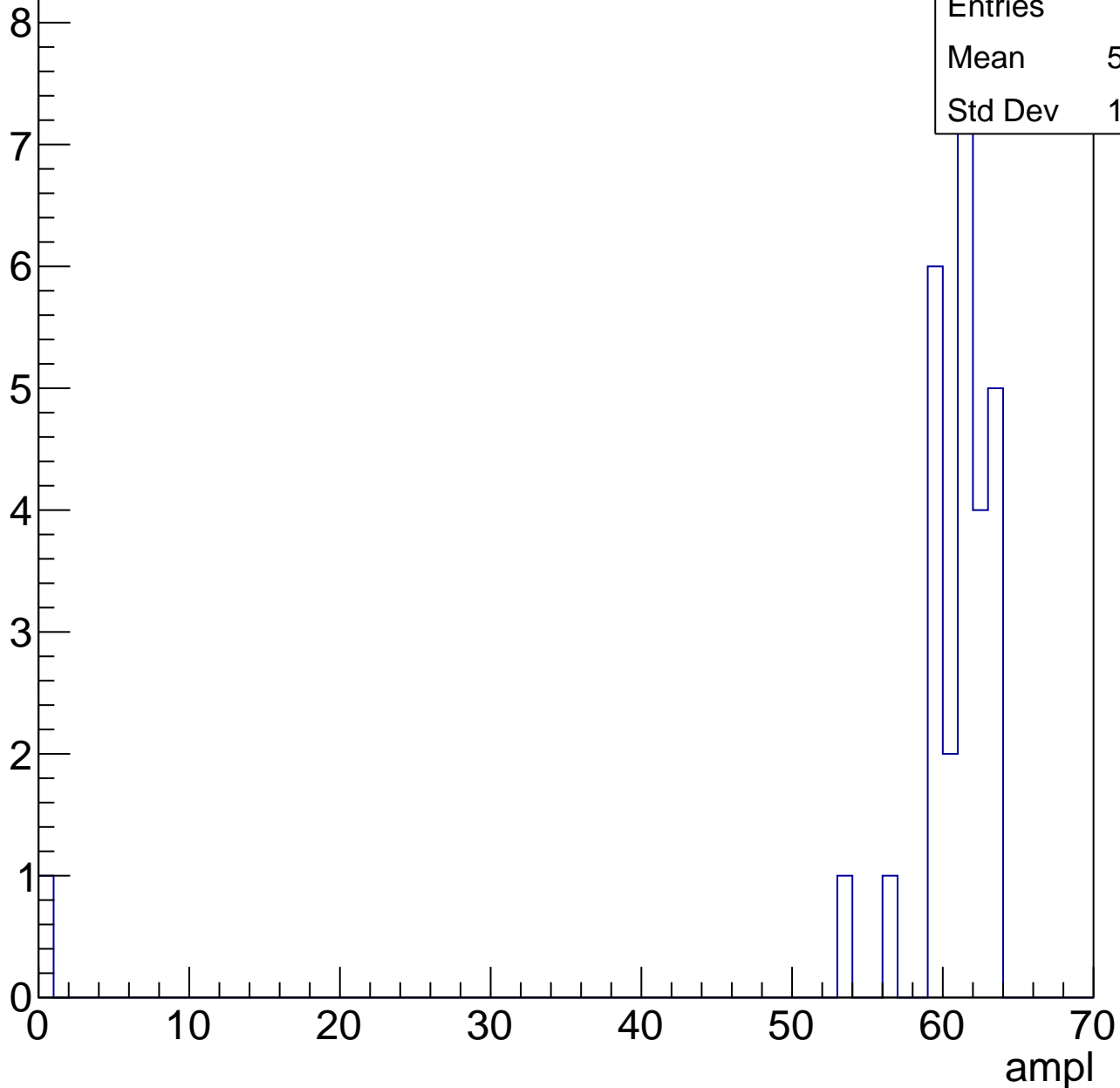


# B0L001S, U17-ch42, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

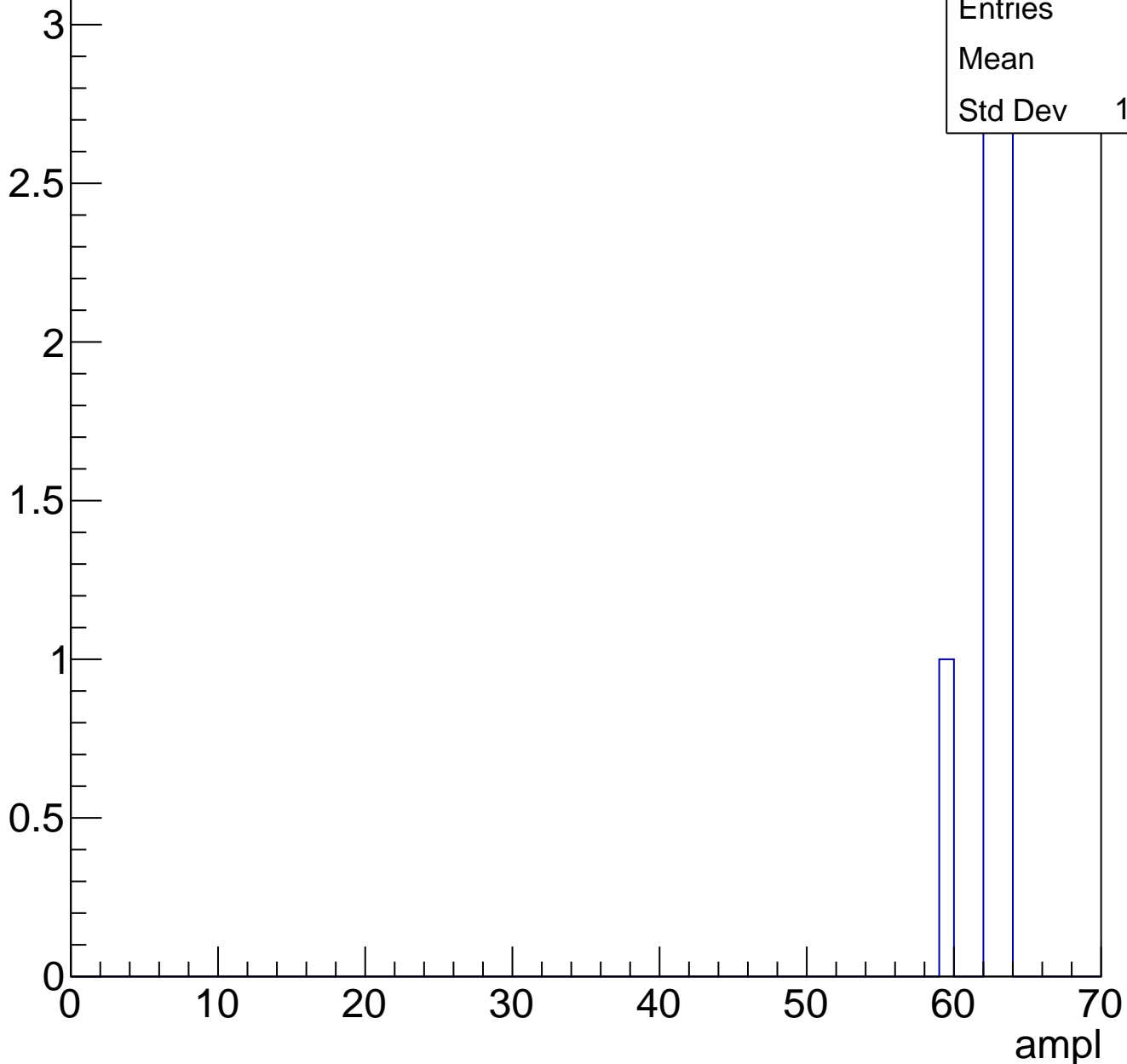
Entries	28
Mean	58.36
Std Dev	11.44



# B0L001S, U17-ch42, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch42, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U17-ch43, adc0

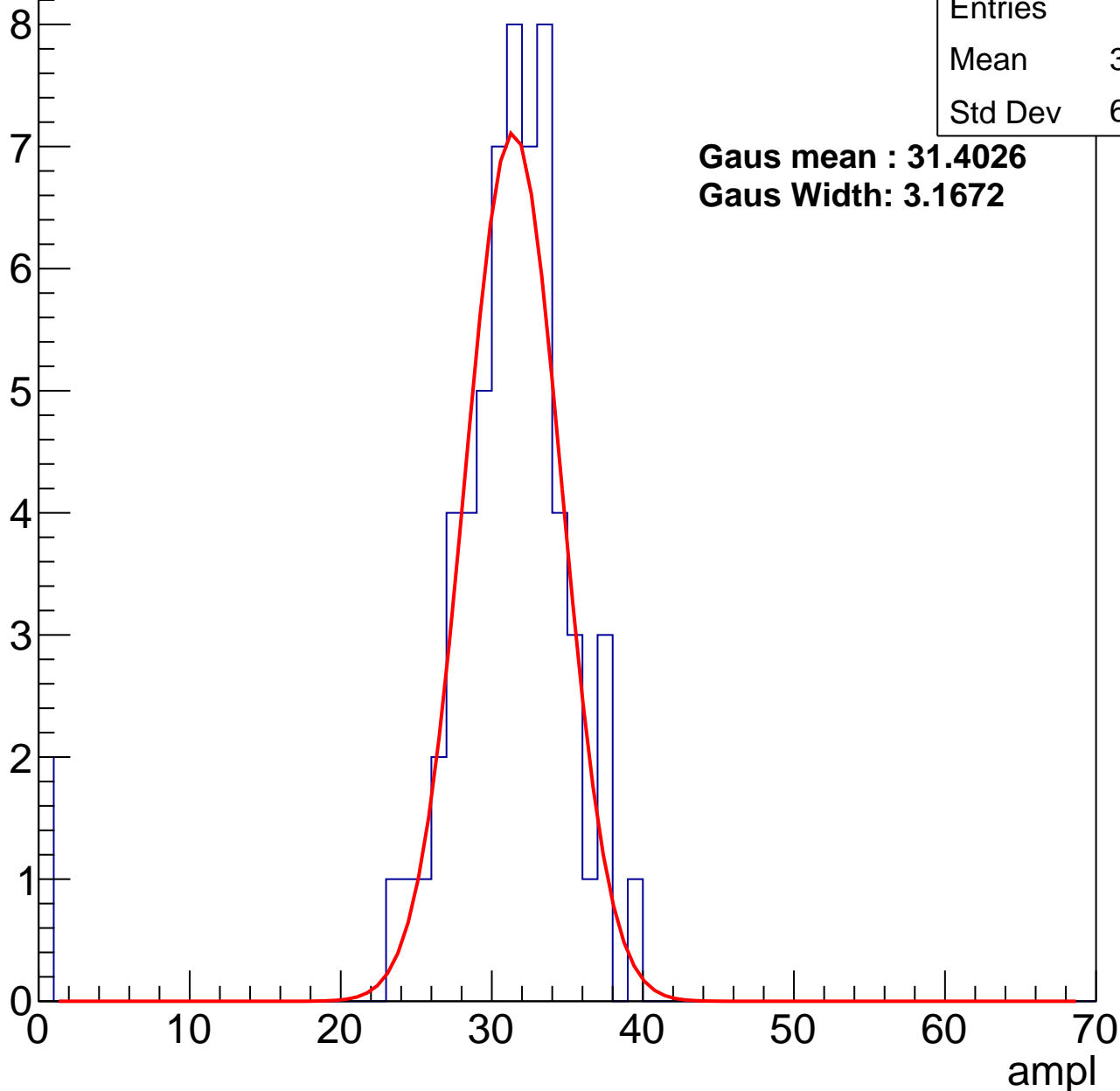
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	30.03
Std Dev	6.363

**Gaus mean : 31.4026**

**Gaus Width: 3.1672**



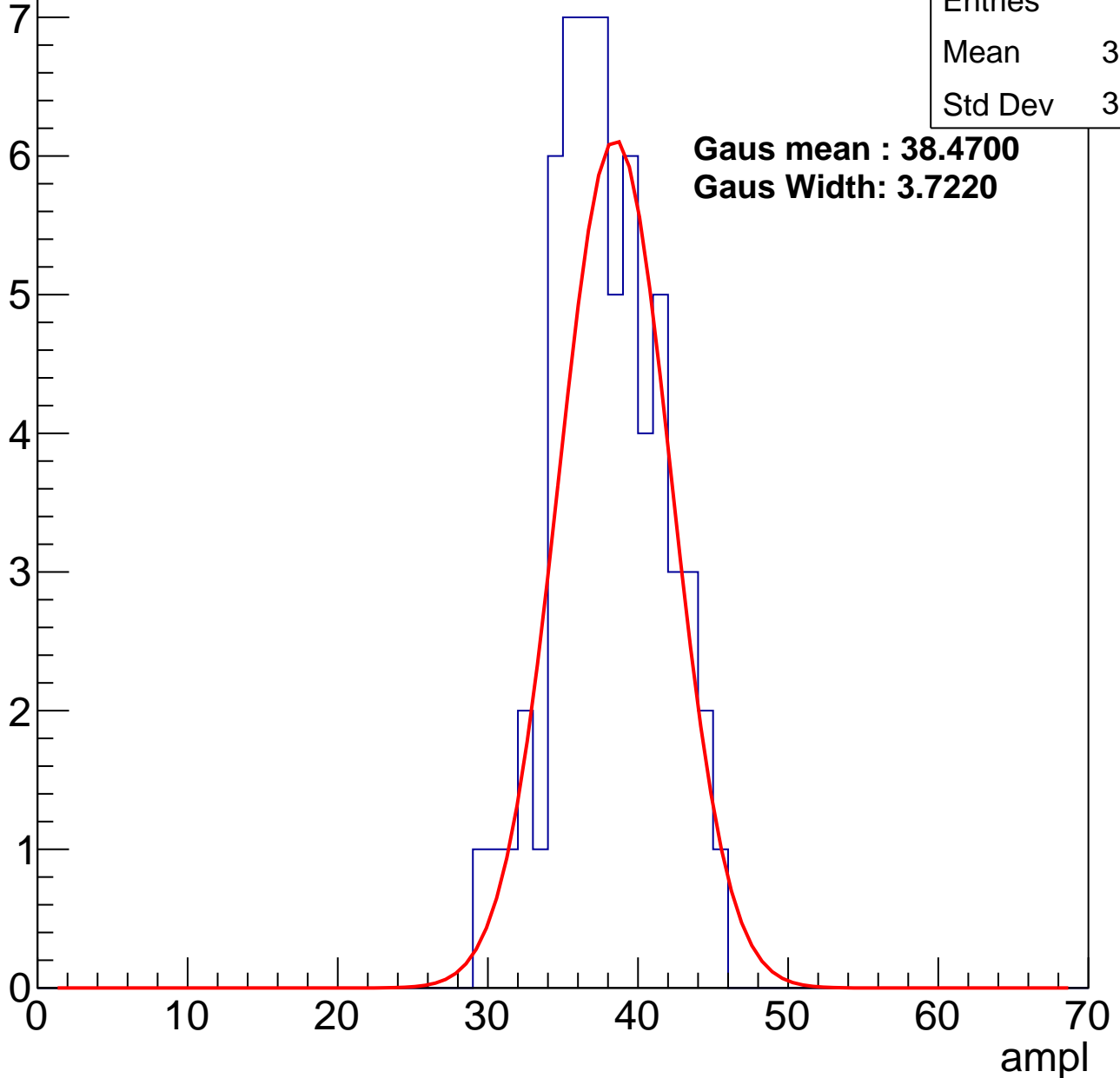
# B0L001S, U17-ch43, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	37.48
Std Dev	3.546

**Gaus mean : 38.4700**  
**Gaus Width: 3.7220**



# B0L001S, U17-ch43, adc2

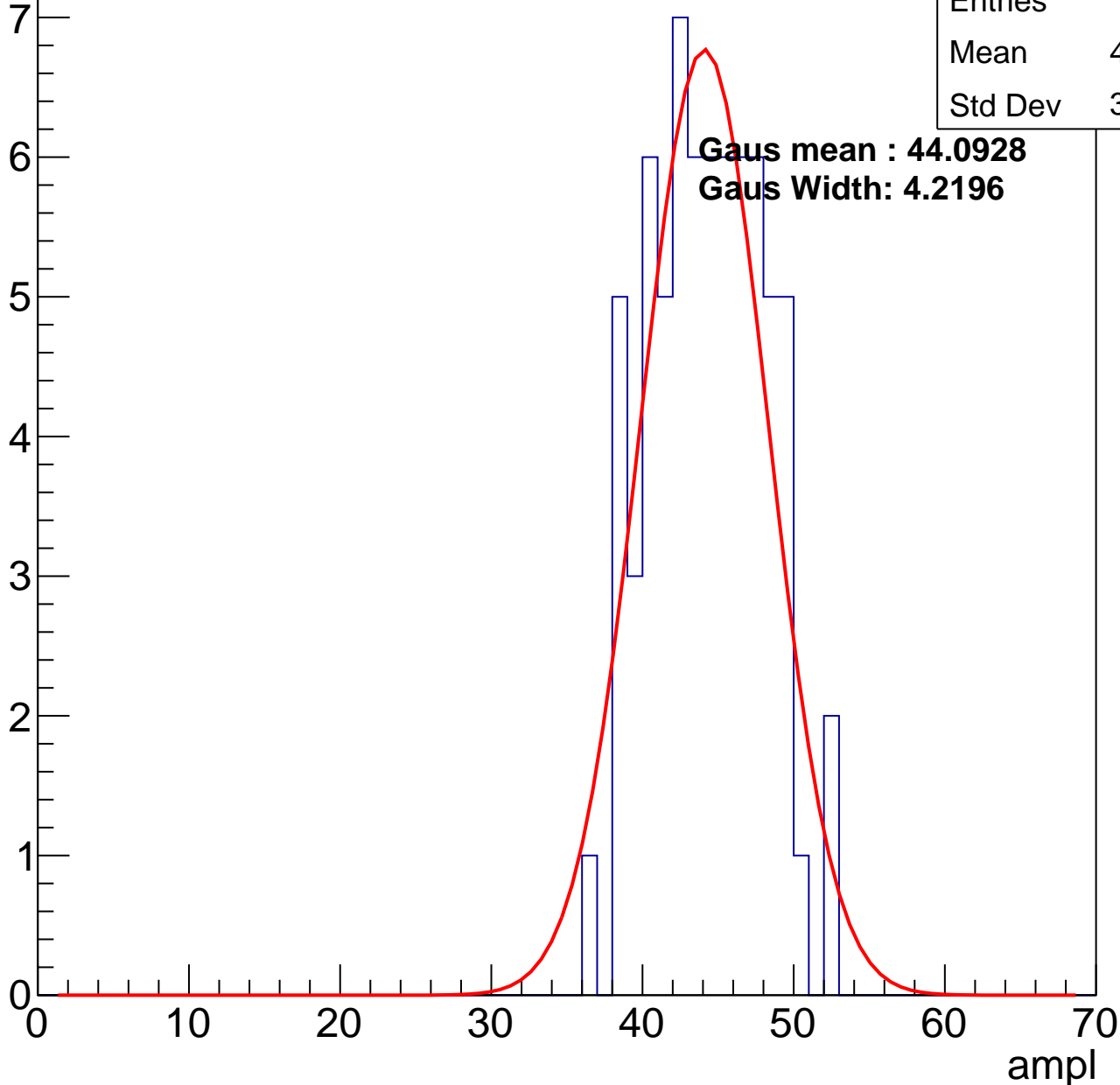
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	43.87
Std Dev	3.676

**Gaus mean : 44.0928**

**Gaus Width: 4.2196**

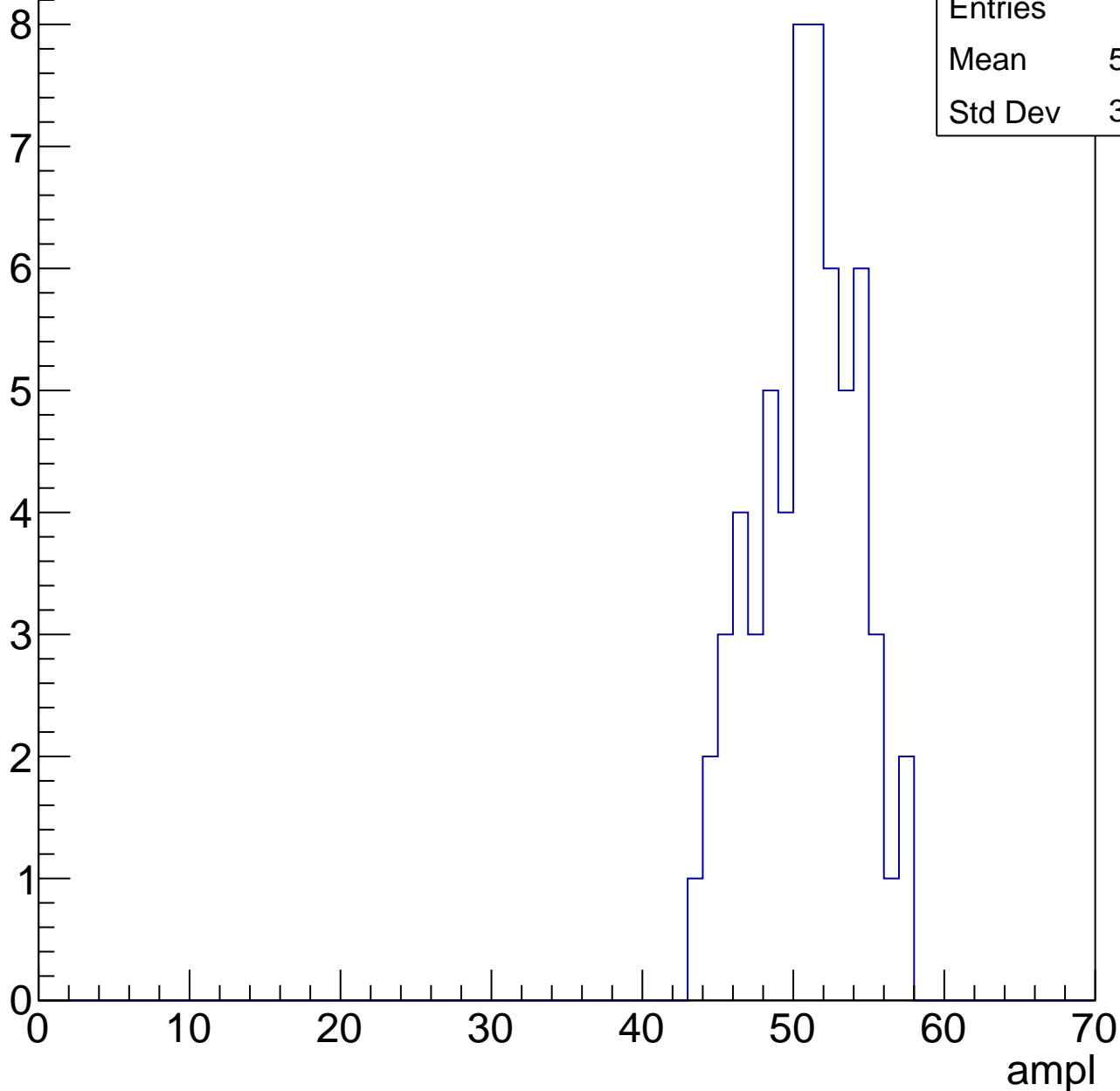


# B0L001S, U17-ch43, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	50.34
Std Dev	3.353

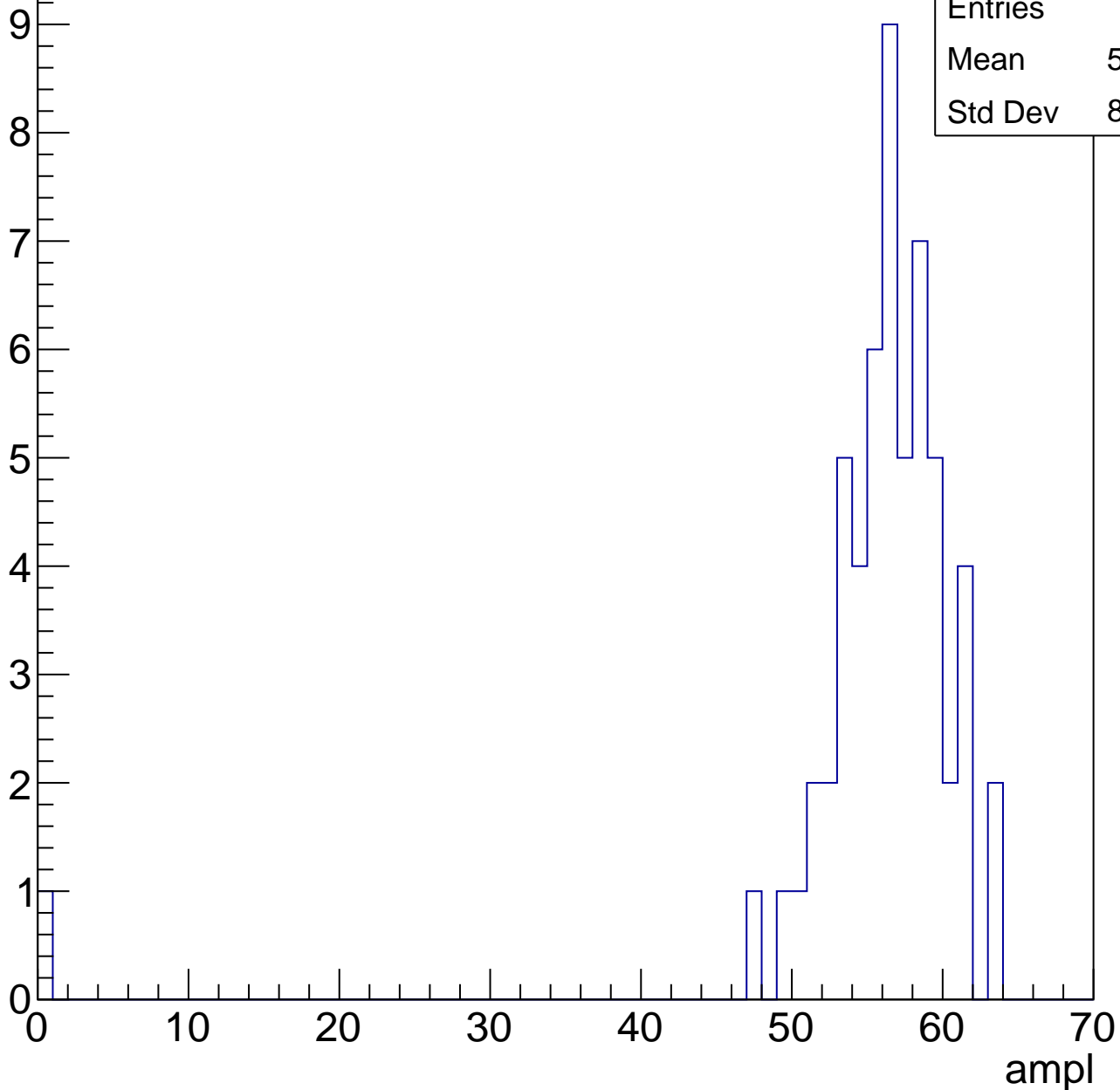


# B0L001S, U17-ch43, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	55.14
Std Dev	8.075

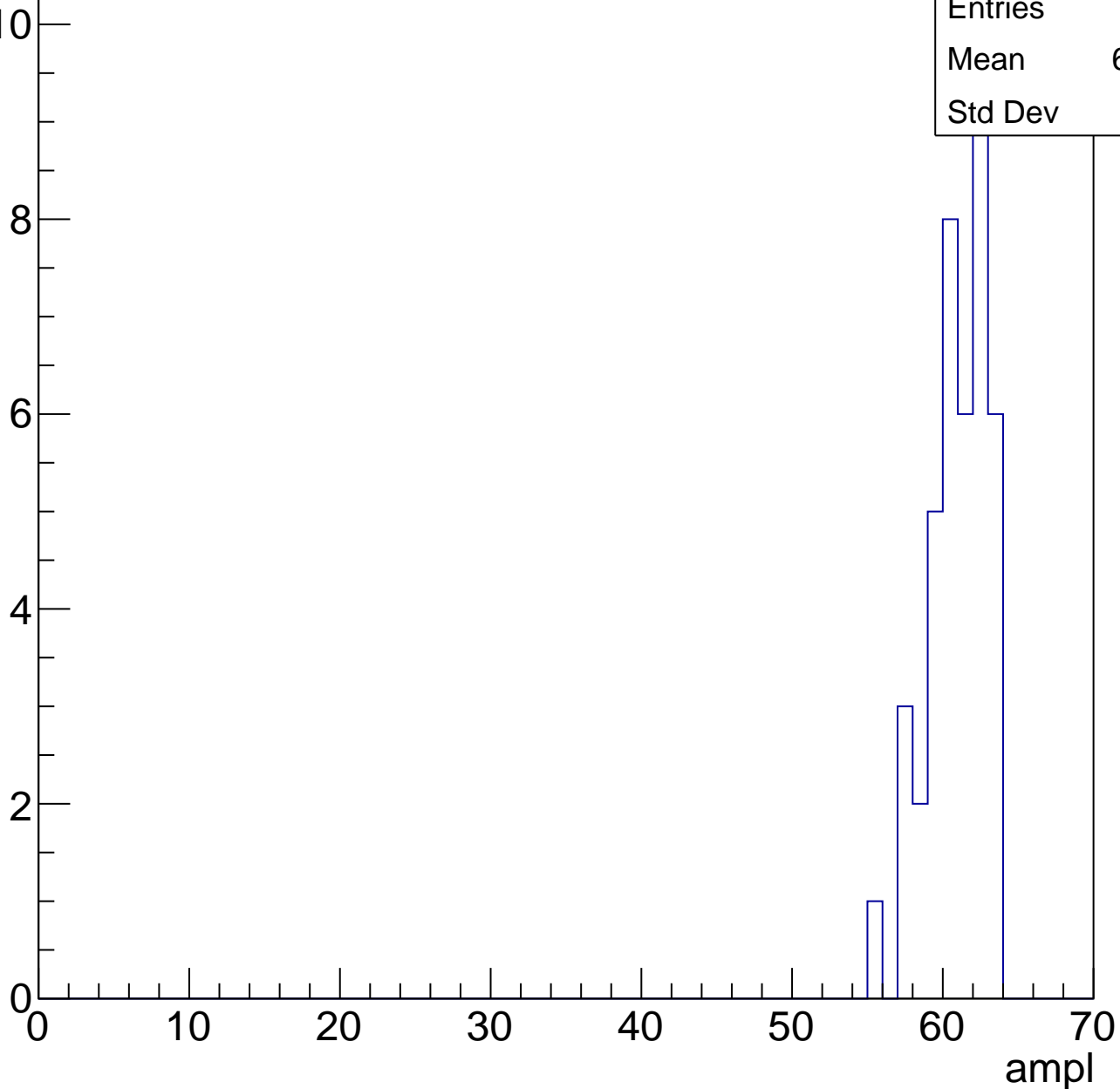


# B0L001S, U17-ch43, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

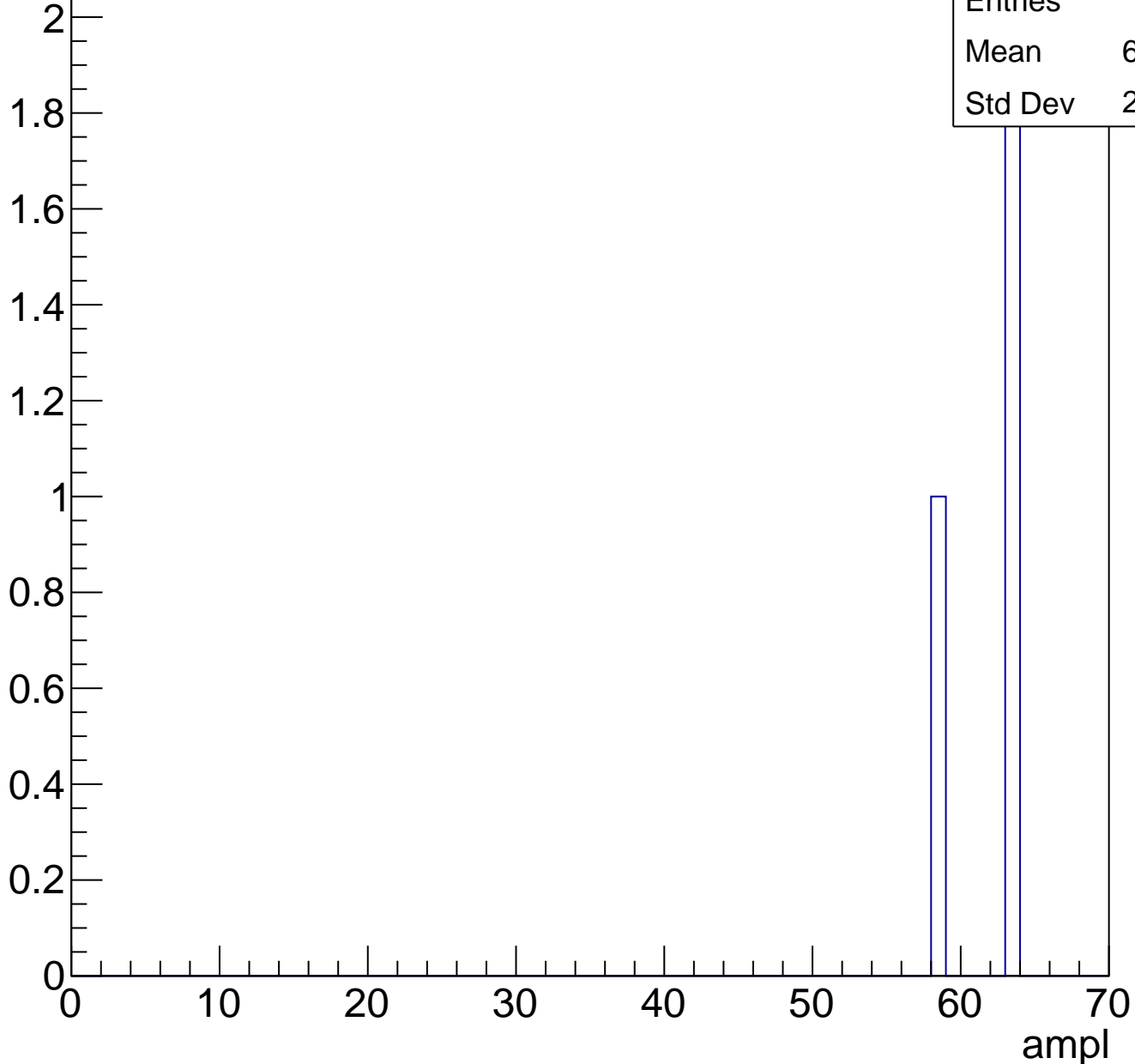
Entries	41
Mean	60.51
Std Dev	1.94



# B0L001S, U17-ch43, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	3
Mean	61.33
Std Dev	2.357



# B0L001S, U17-ch43, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U17-ch44, adc0

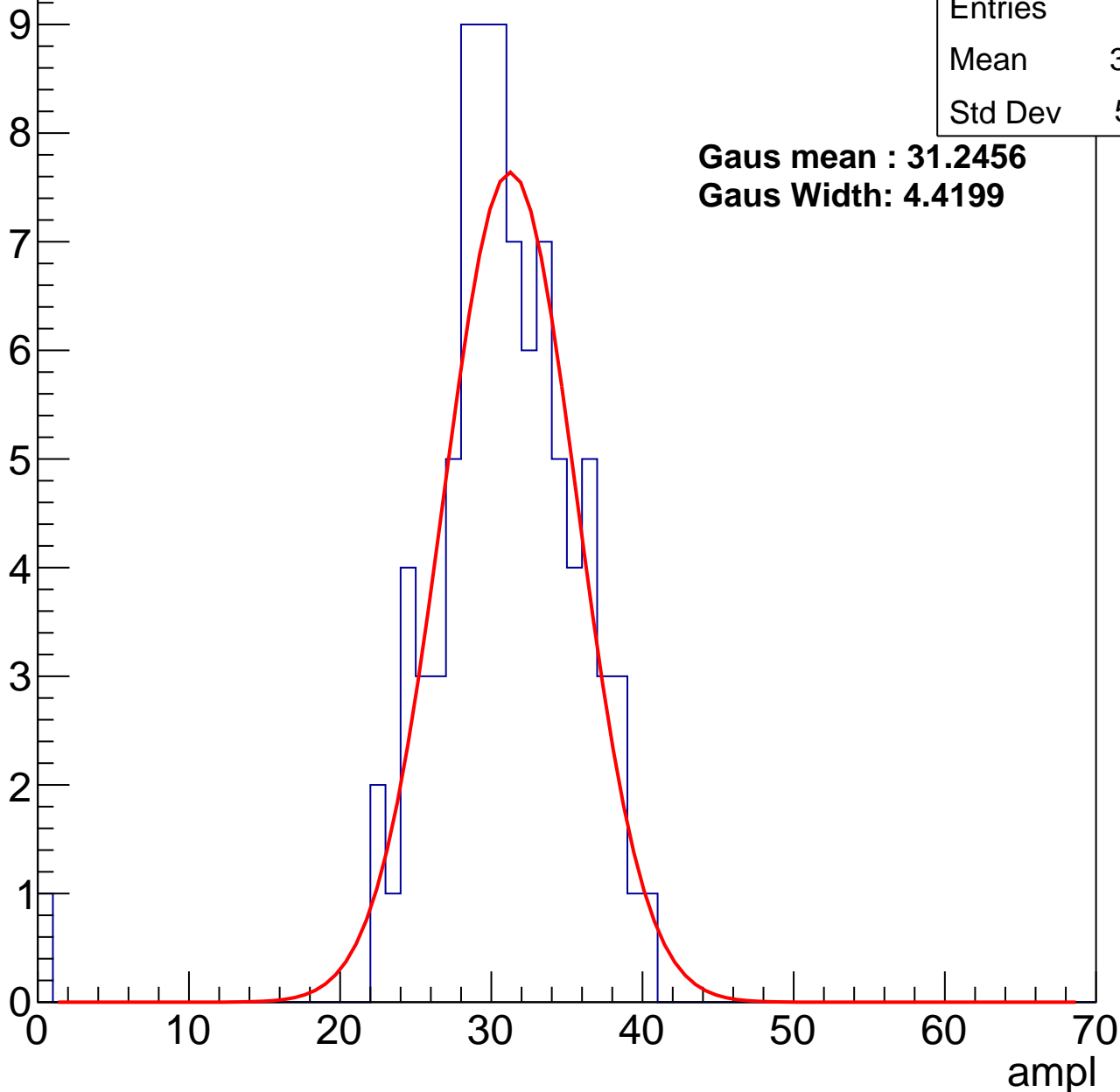
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	88
Mean	30.32
Std Dev	5.221

**Gaus mean : 31.2456**

**Gaus Width: 4.4199**



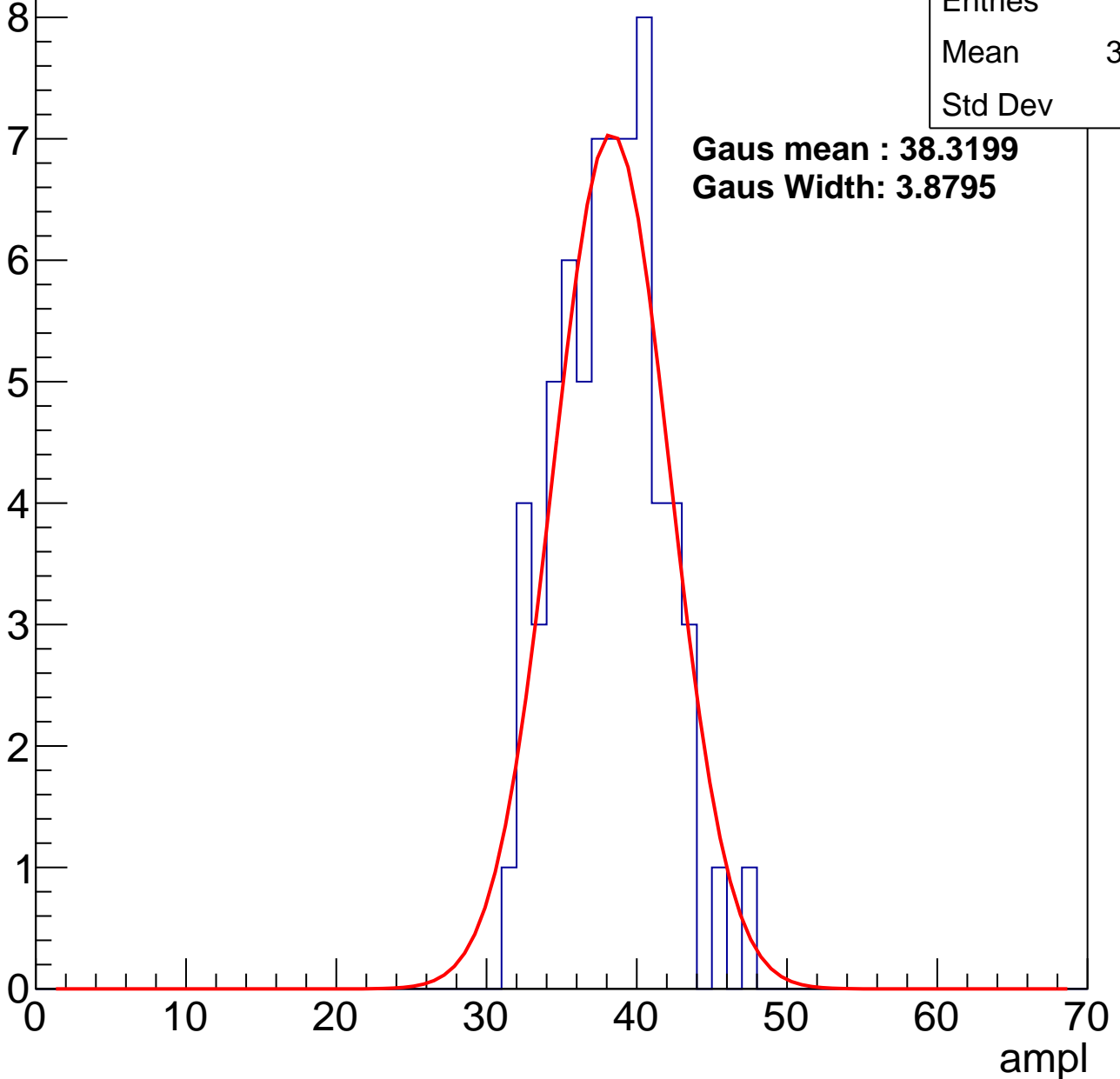
# B0L001S, U17-ch44, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	37.71
Std Dev	3.41

**Gaus mean : 38.3199**  
**Gaus Width: 3.8795**



# B0L001S, U17-ch44, adc2

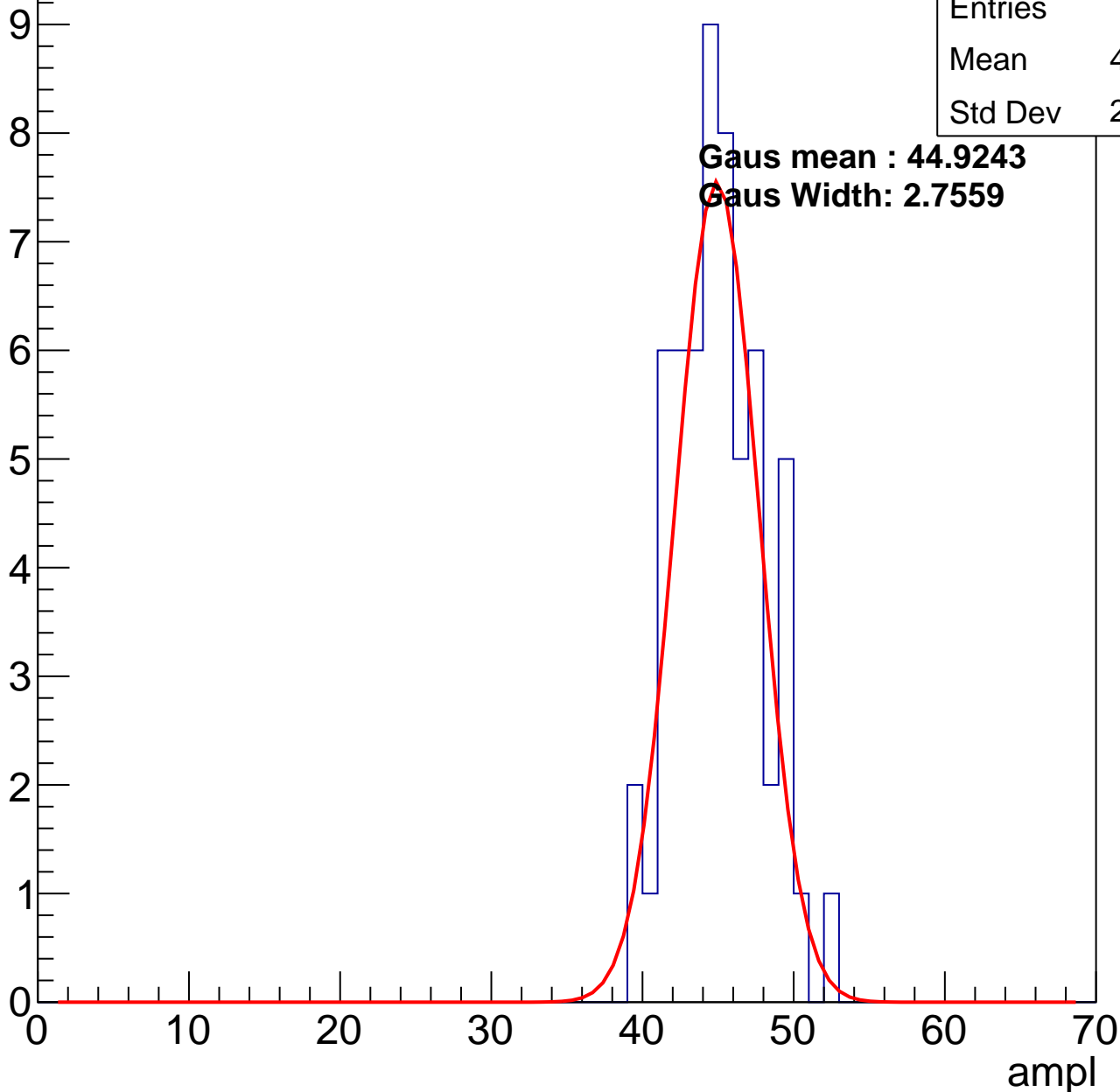
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	44.57
Std Dev	2.847

**Gaus mean : 44.9243**

**Gaus Width: 2.7559**

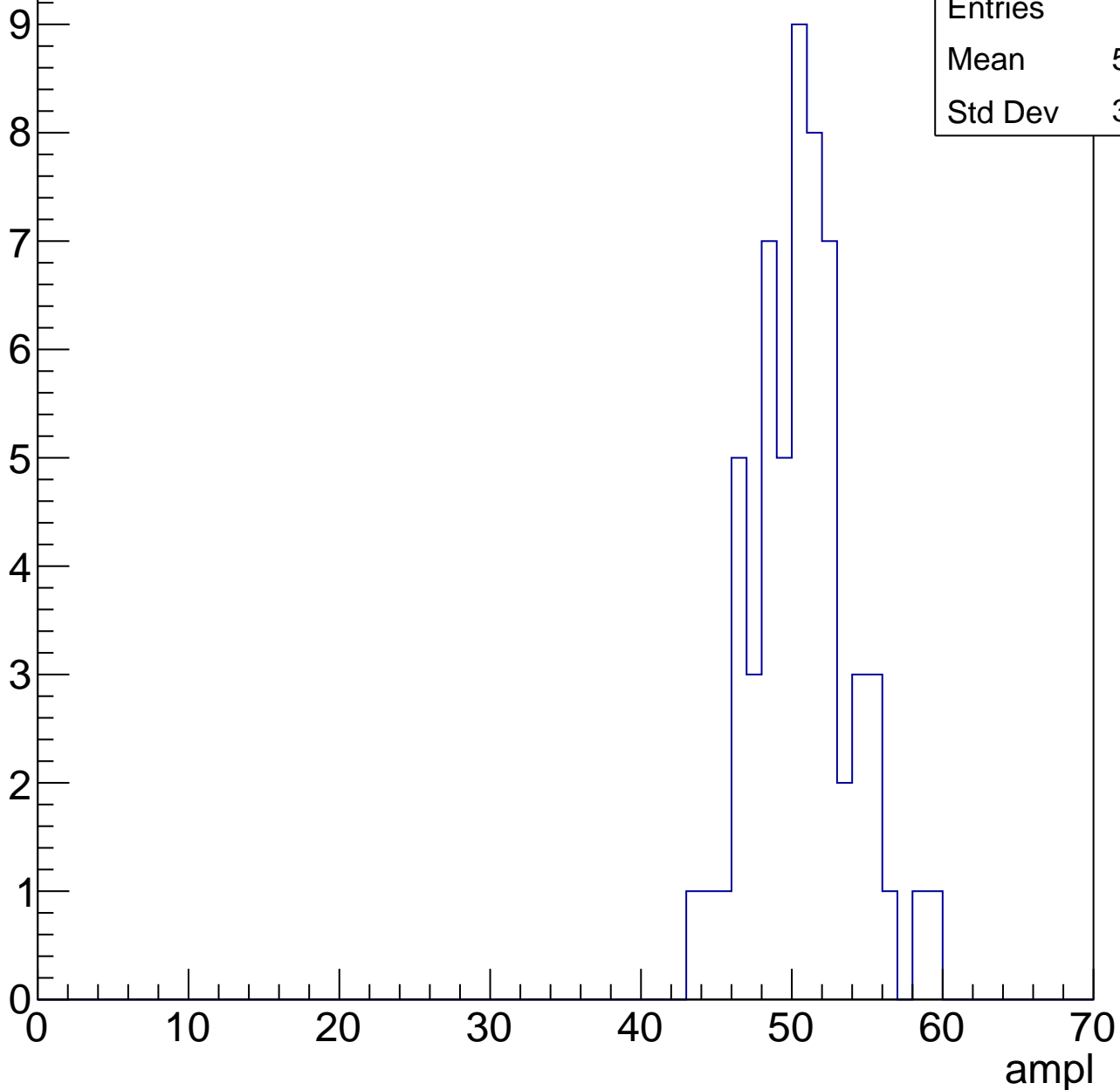


# B0L001S, U17-ch44, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	50.21
Std Dev	3.231

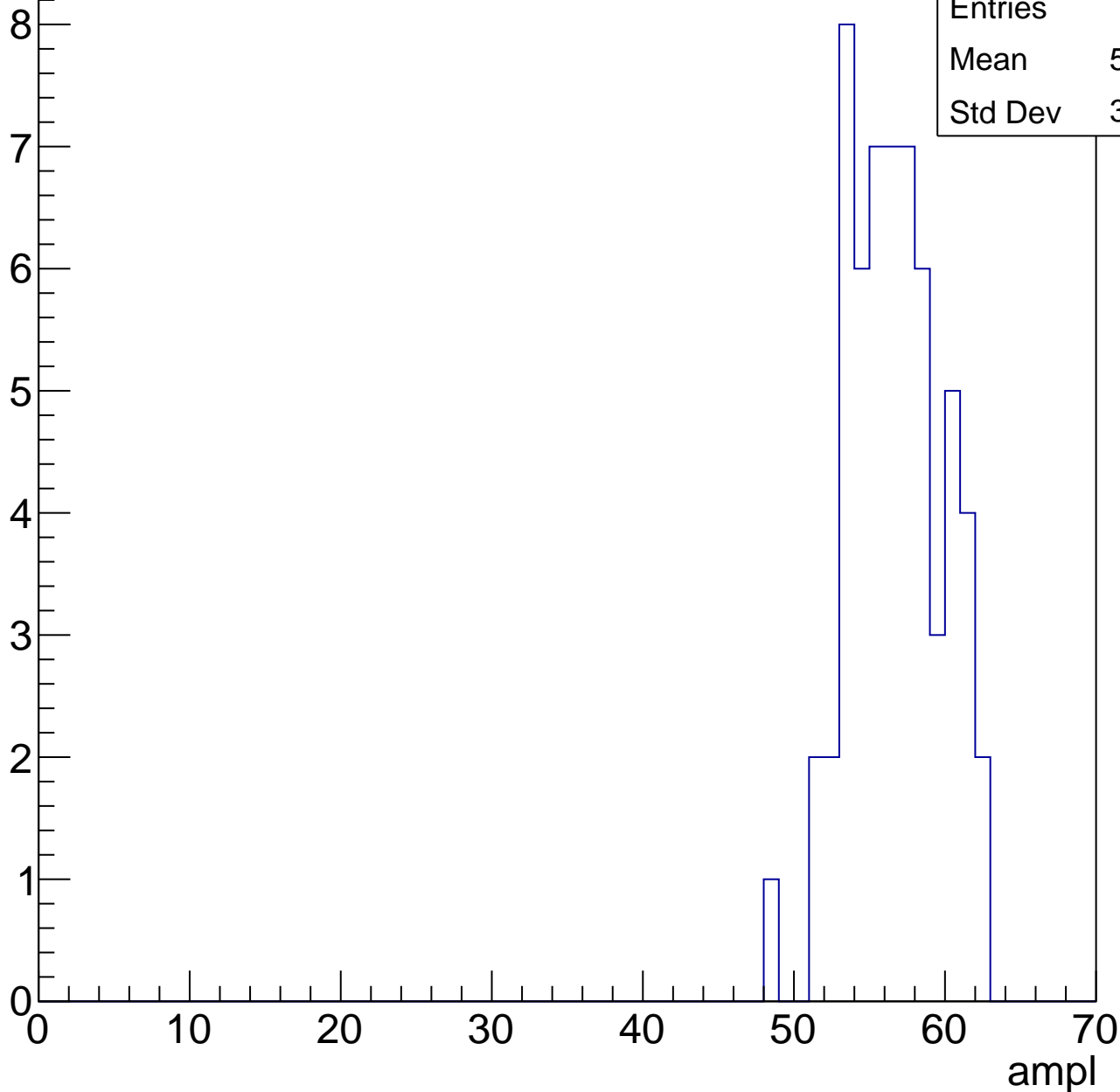


# B0L001S, U17-ch44, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	56.18
Std Dev	3.047

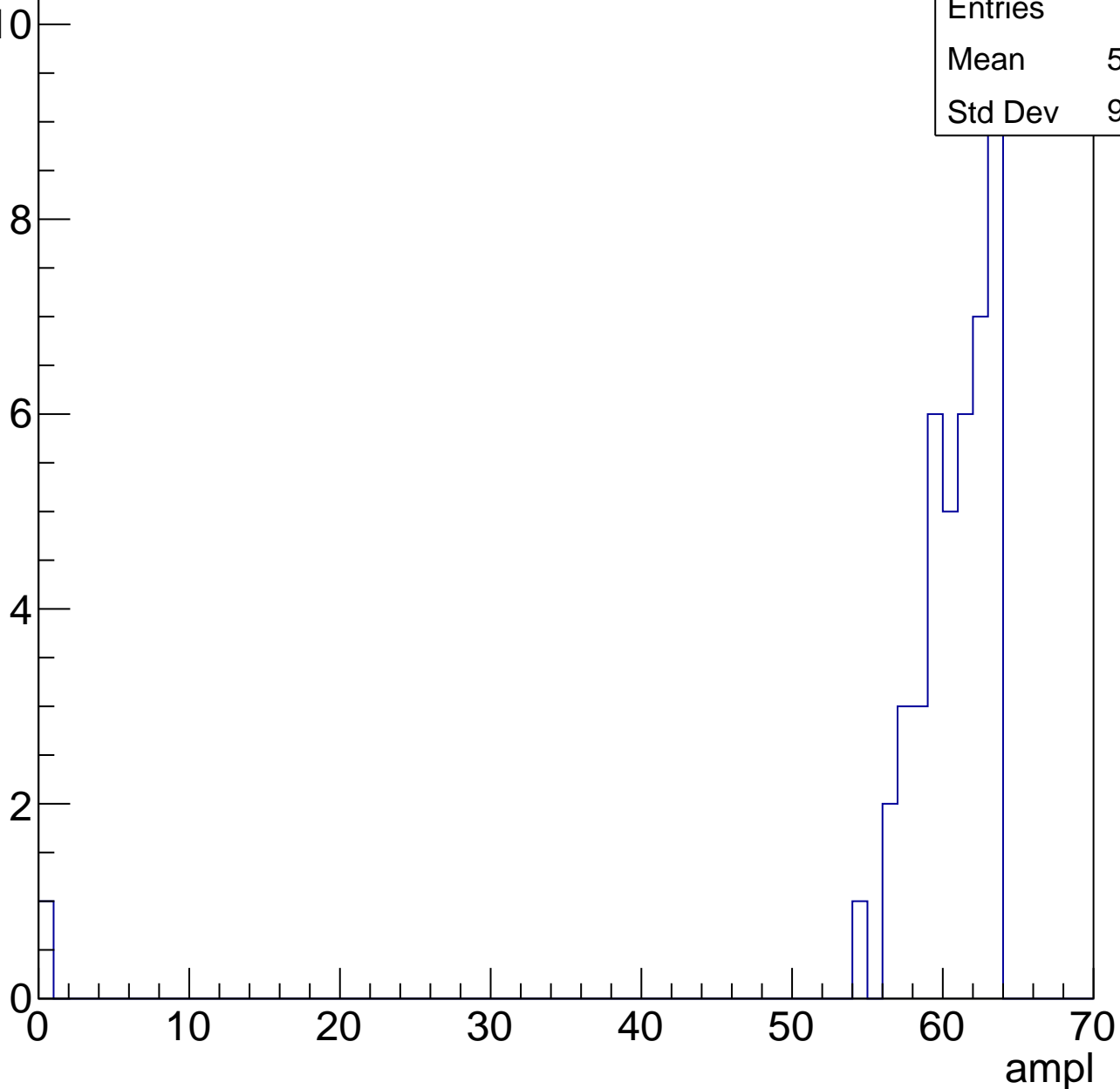


# B0L001S, U17-ch44, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	44
Mean	58.98
Std Dev	9.282



# B0L001S, U17-ch44, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch44, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U17-ch45, adc0

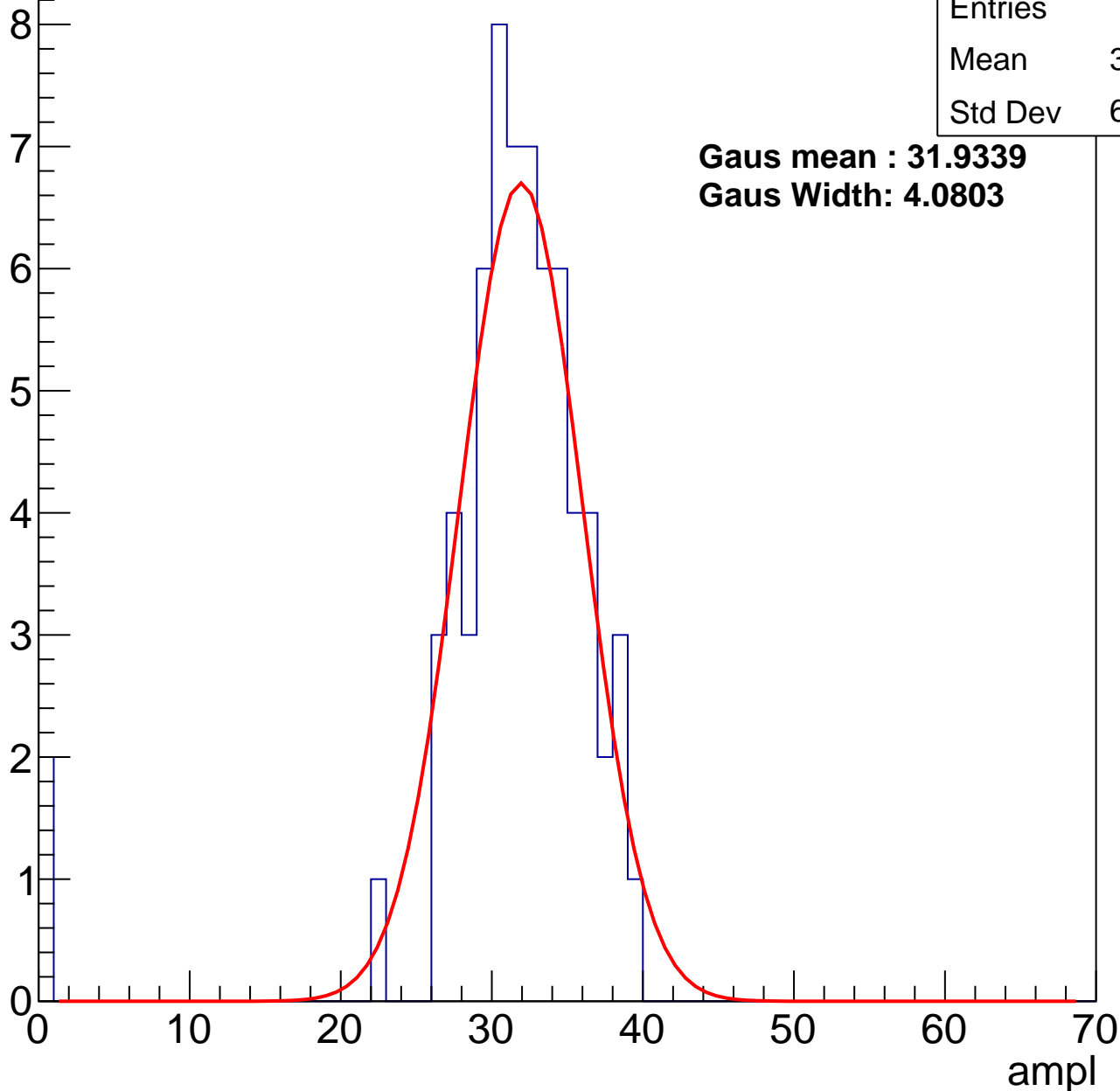
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	30.75
Std Dev	6.382

**Gaus mean : 31.9339**

**Gaus Width: 4.0803**



# B0L001S, U17-ch45, adc1

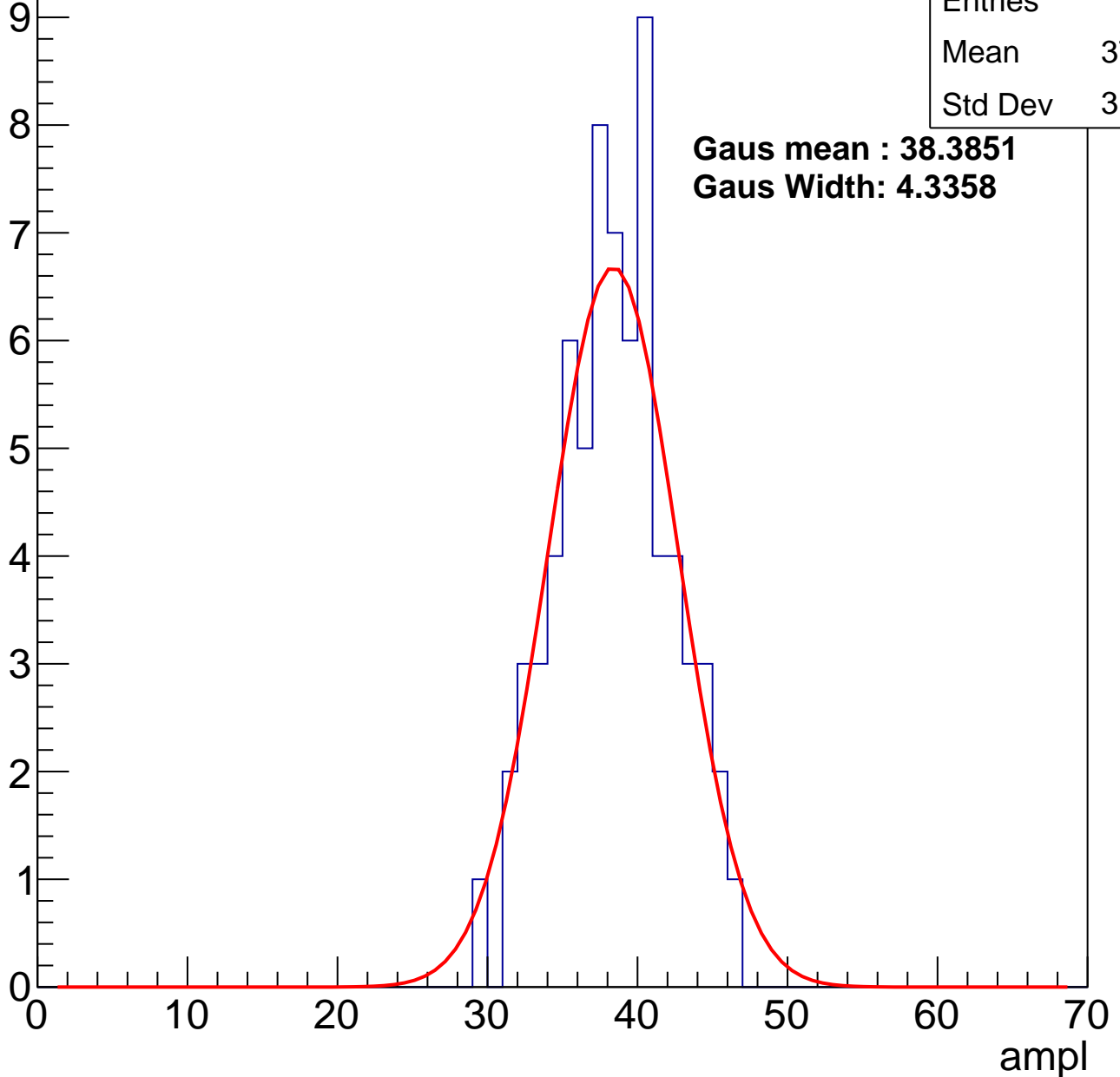
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	37.99
Std Dev	3.744

**Gaus mean : 38.3851**

**Gaus Width: 4.3358**

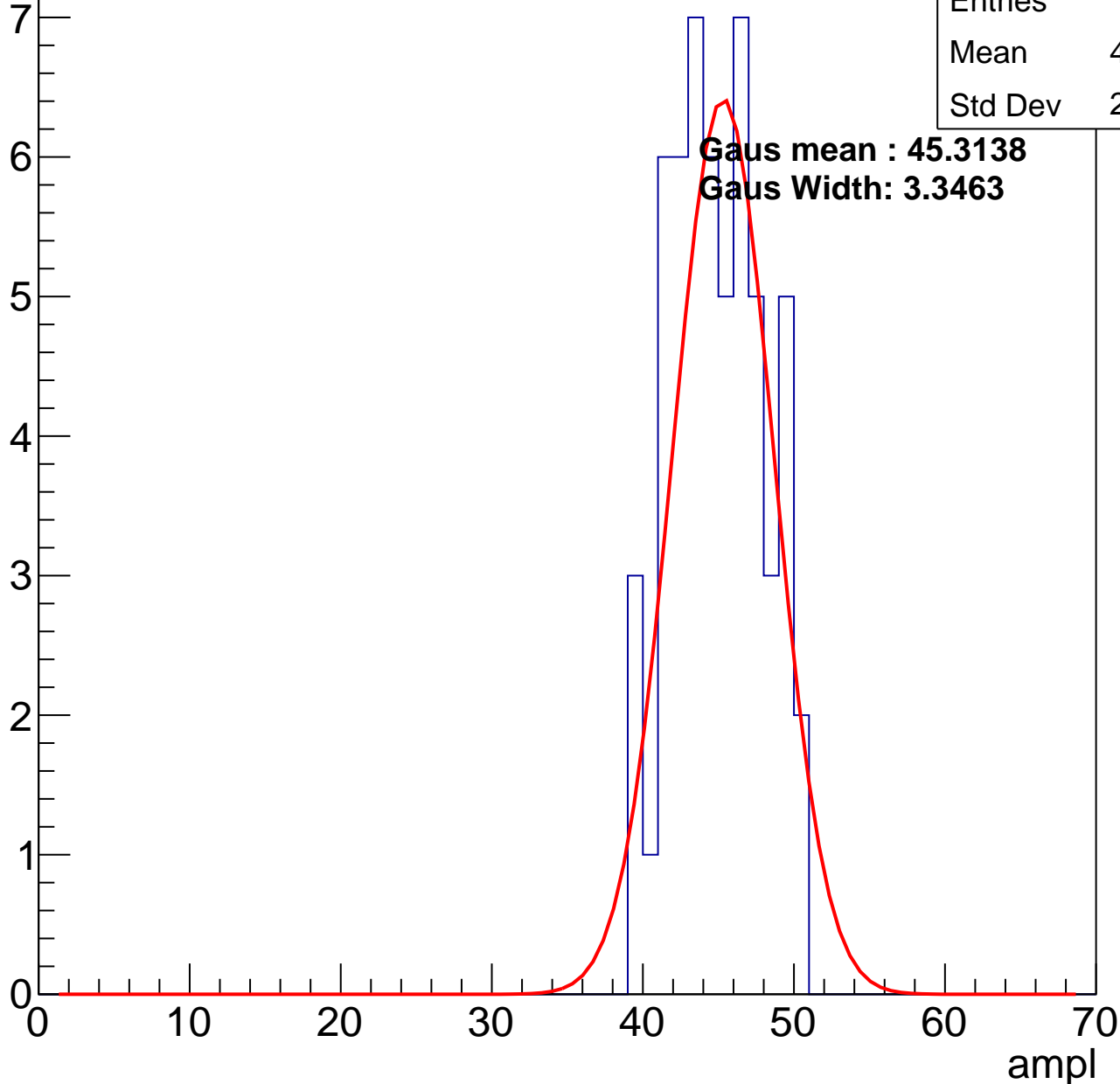


# B0L001S, U17-ch45, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	44.48
Std Dev	2.946

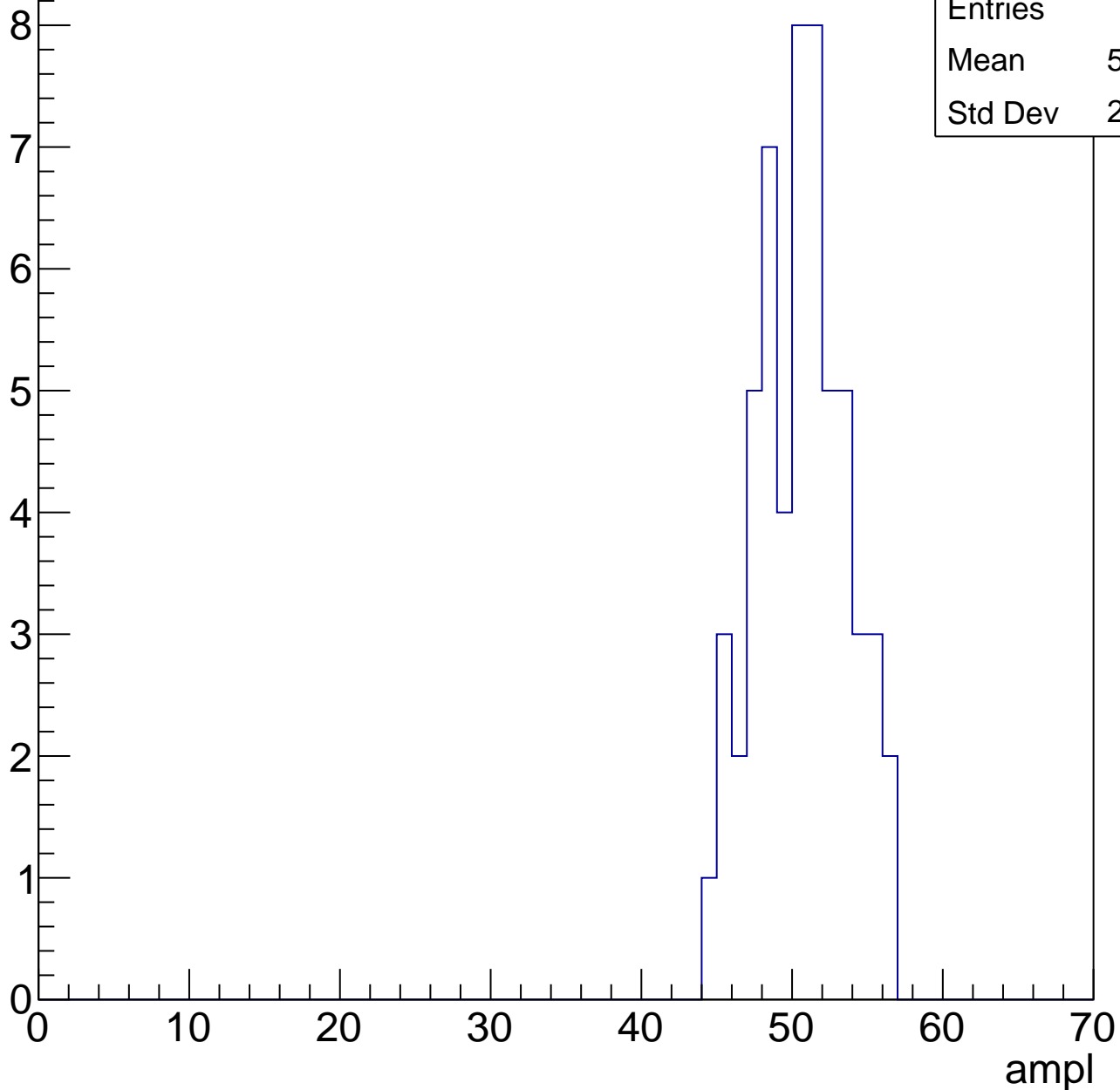


# B0L001S, U17-ch45, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	50.18
Std Dev	2.947

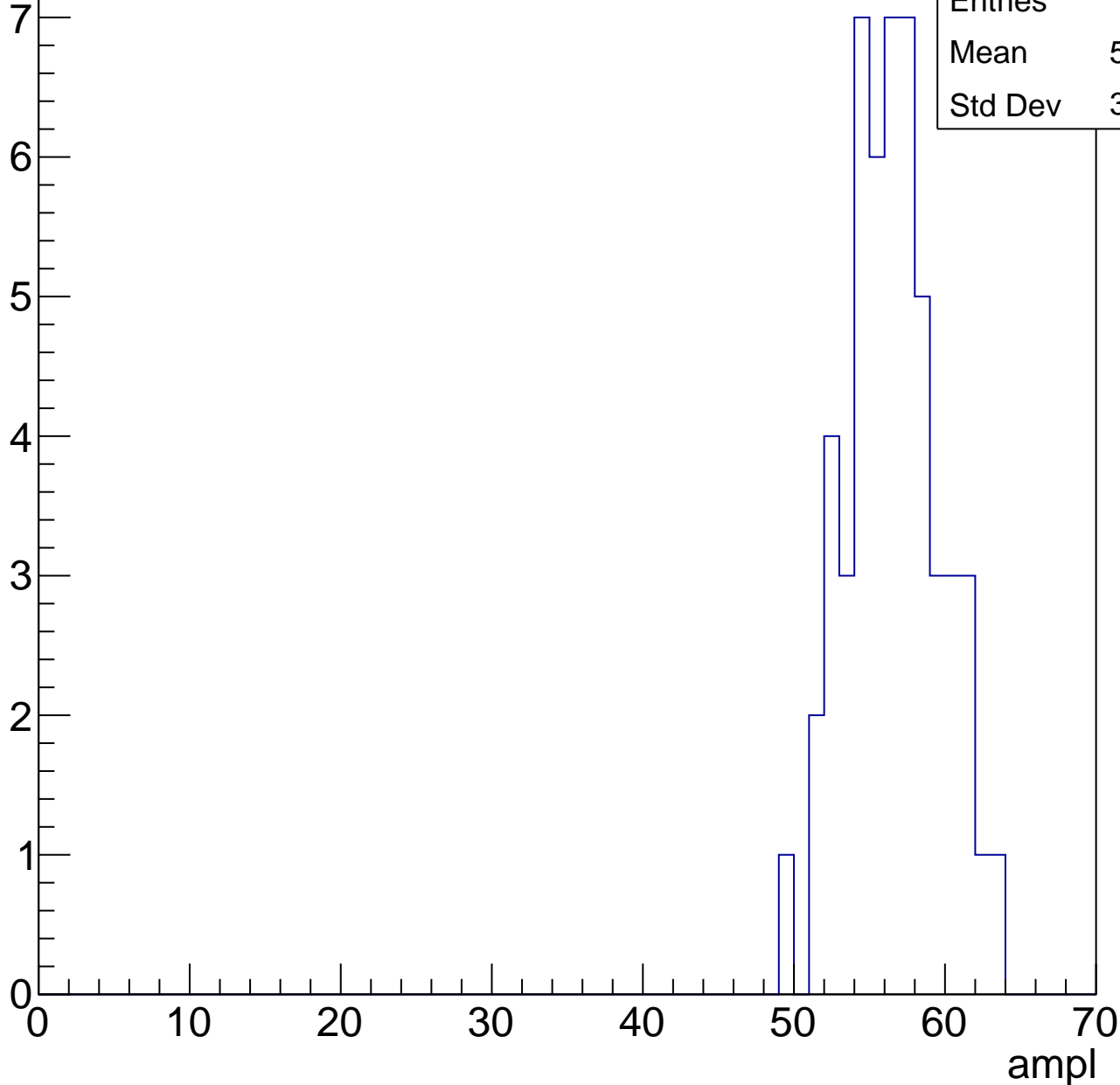


# B0L001S, U17-ch45, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	56.08
Std Dev	3.027

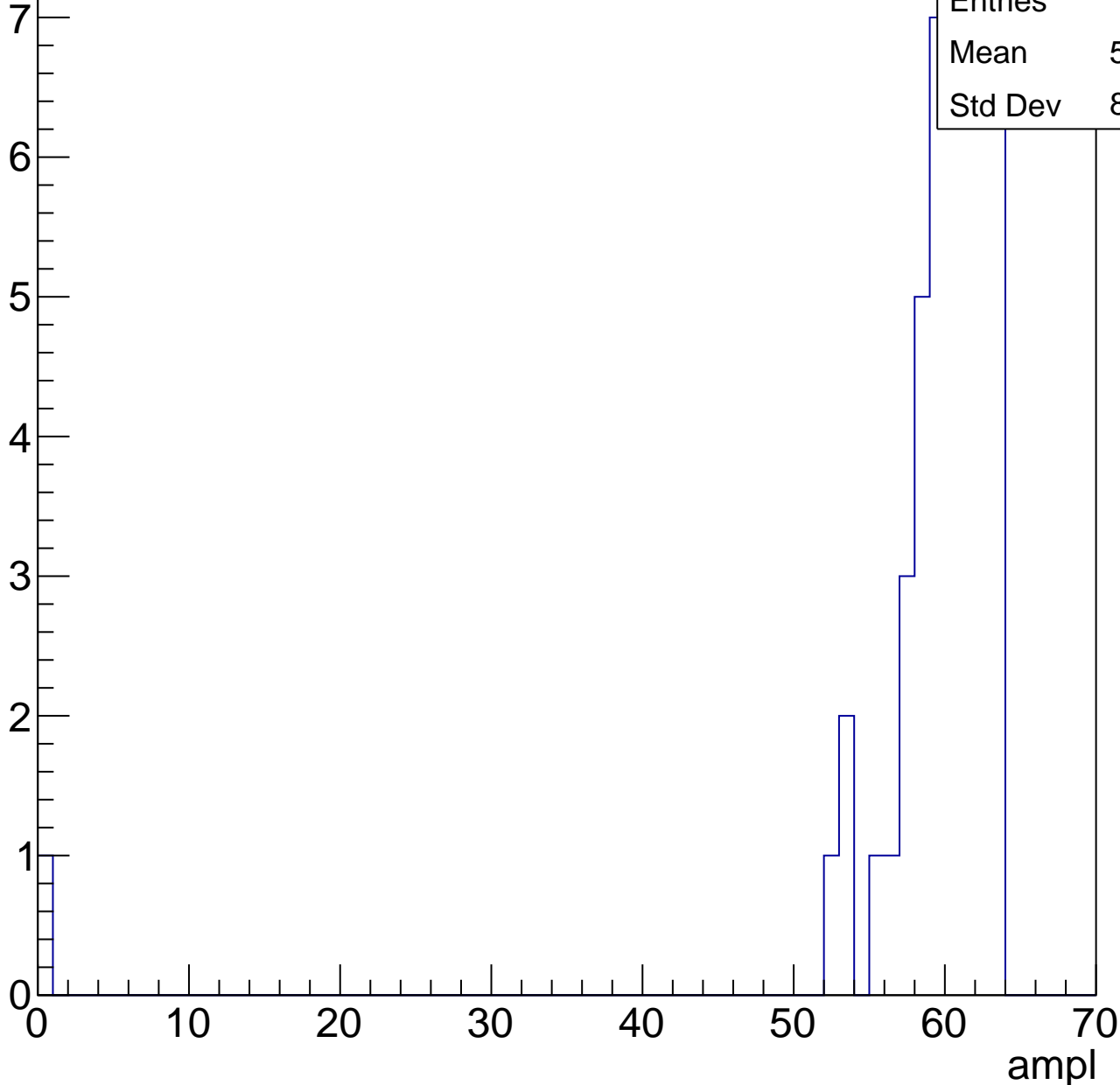


# B0L001S, U17-ch45, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	49
Mean	58.47
Std Dev	8.853



# B0L001S, U17-ch45, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch45, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U17-ch46, adc0

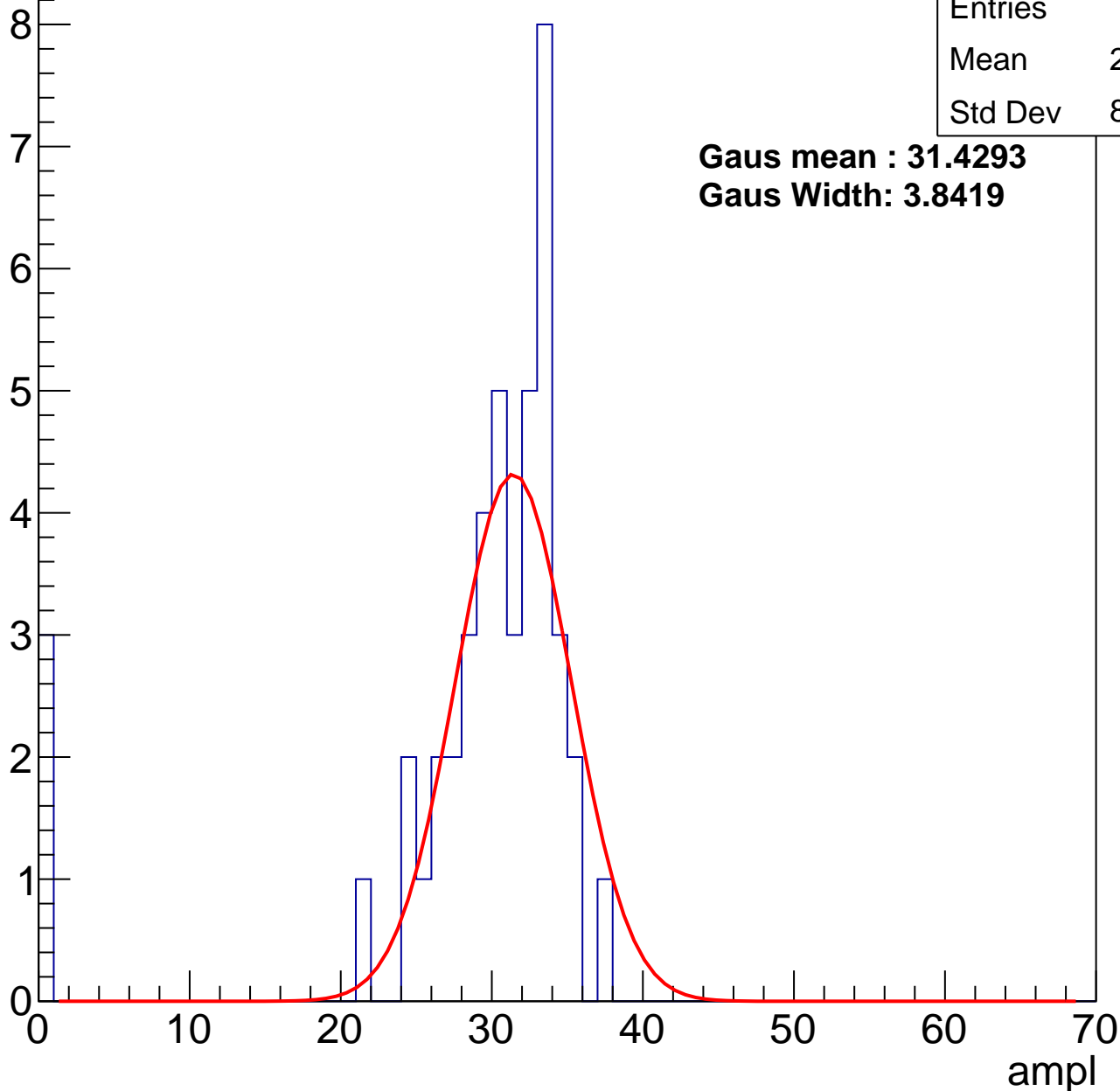
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	45
Mean	28.36
Std Dev	8.252

**Gaus mean : 31.4293**

**Gaus Width: 3.8419**

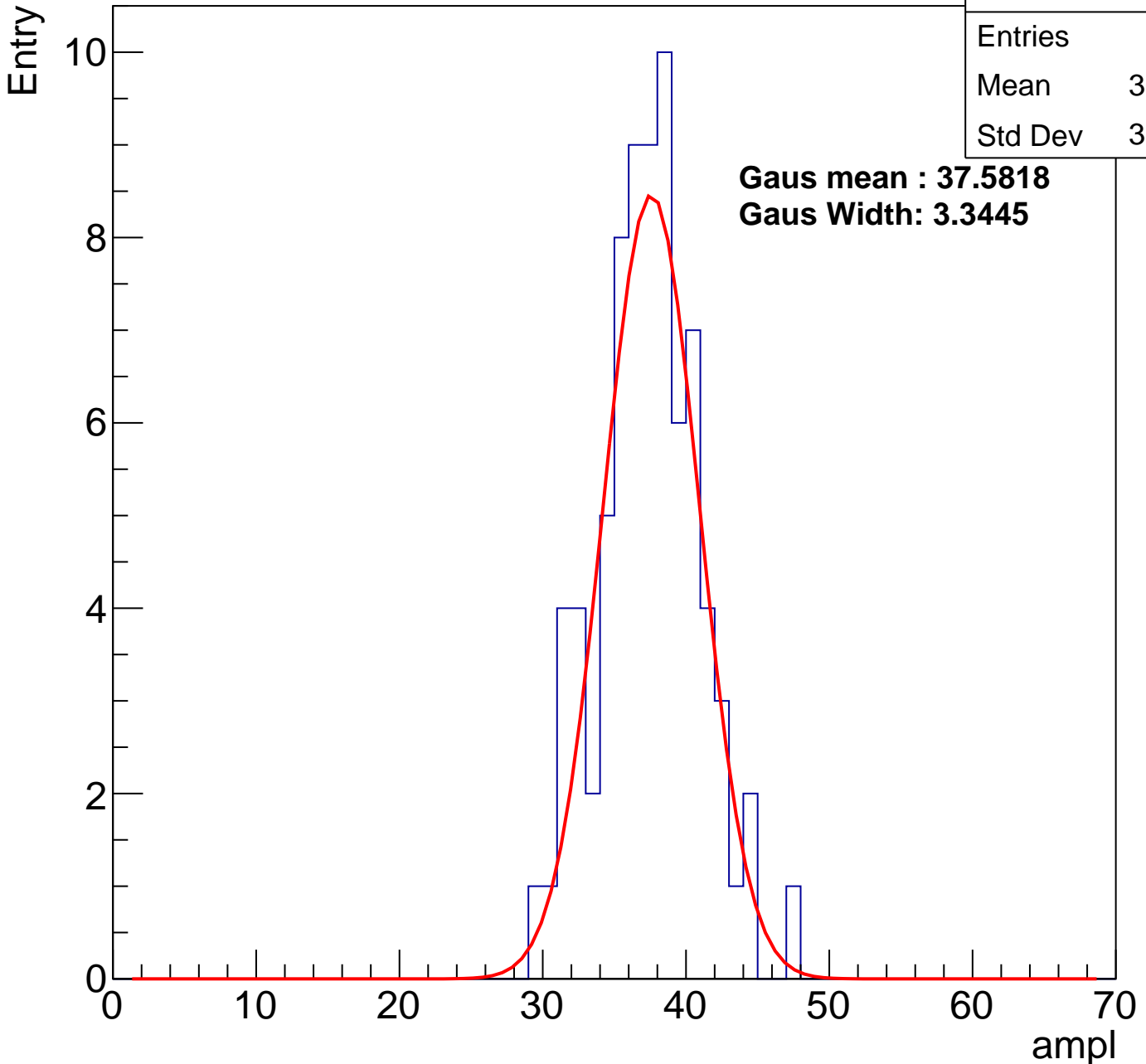


# B0L001S, U17-ch46, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	77
Mean	36.96
Std Dev	3.503

**Gaus mean : 37.5818**  
**Gaus Width: 3.3445**



# B0L001S, U17-ch46, adc2

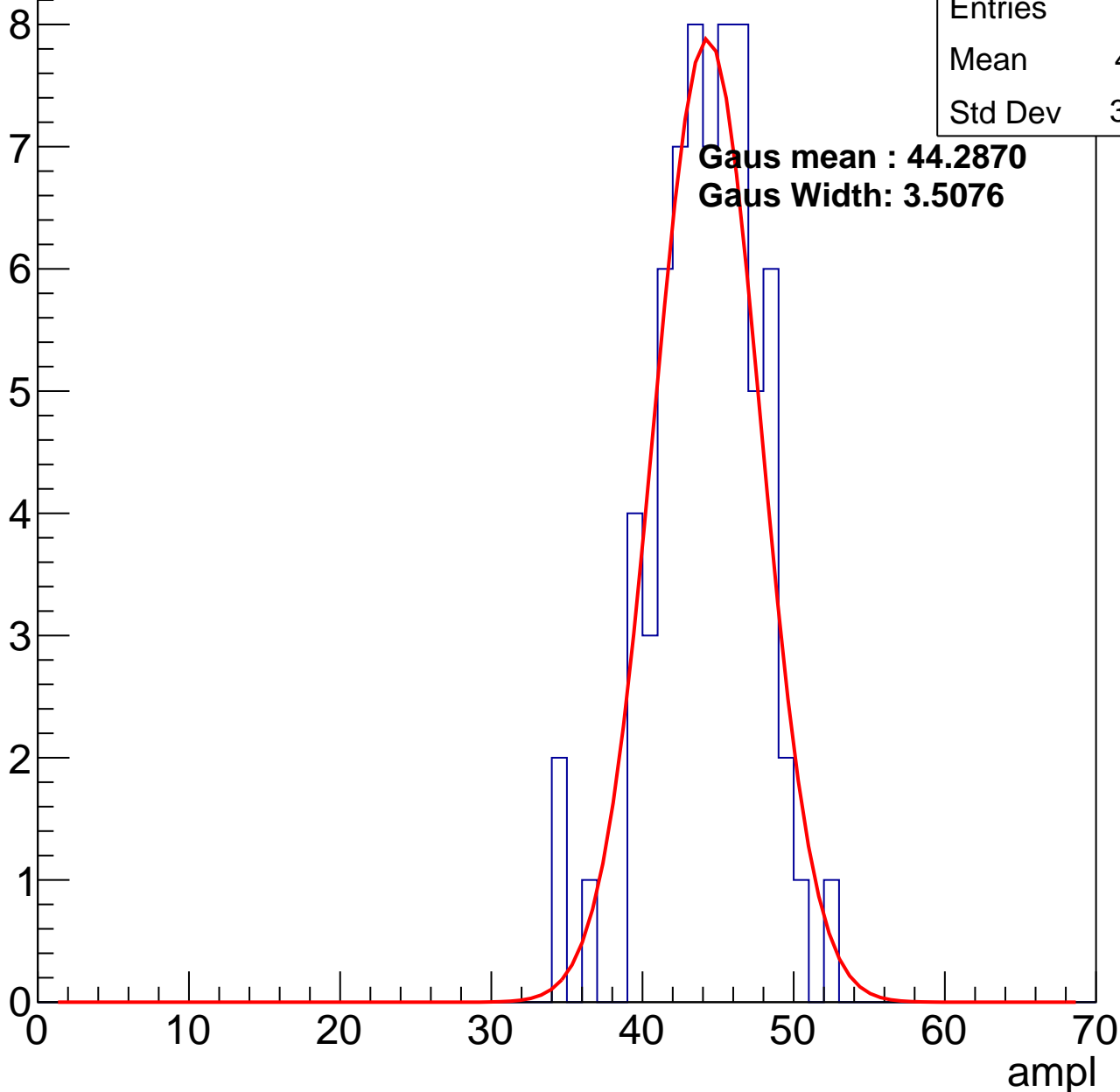
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	43.81
Std Dev	3.469

**Gaus mean : 44.2870**

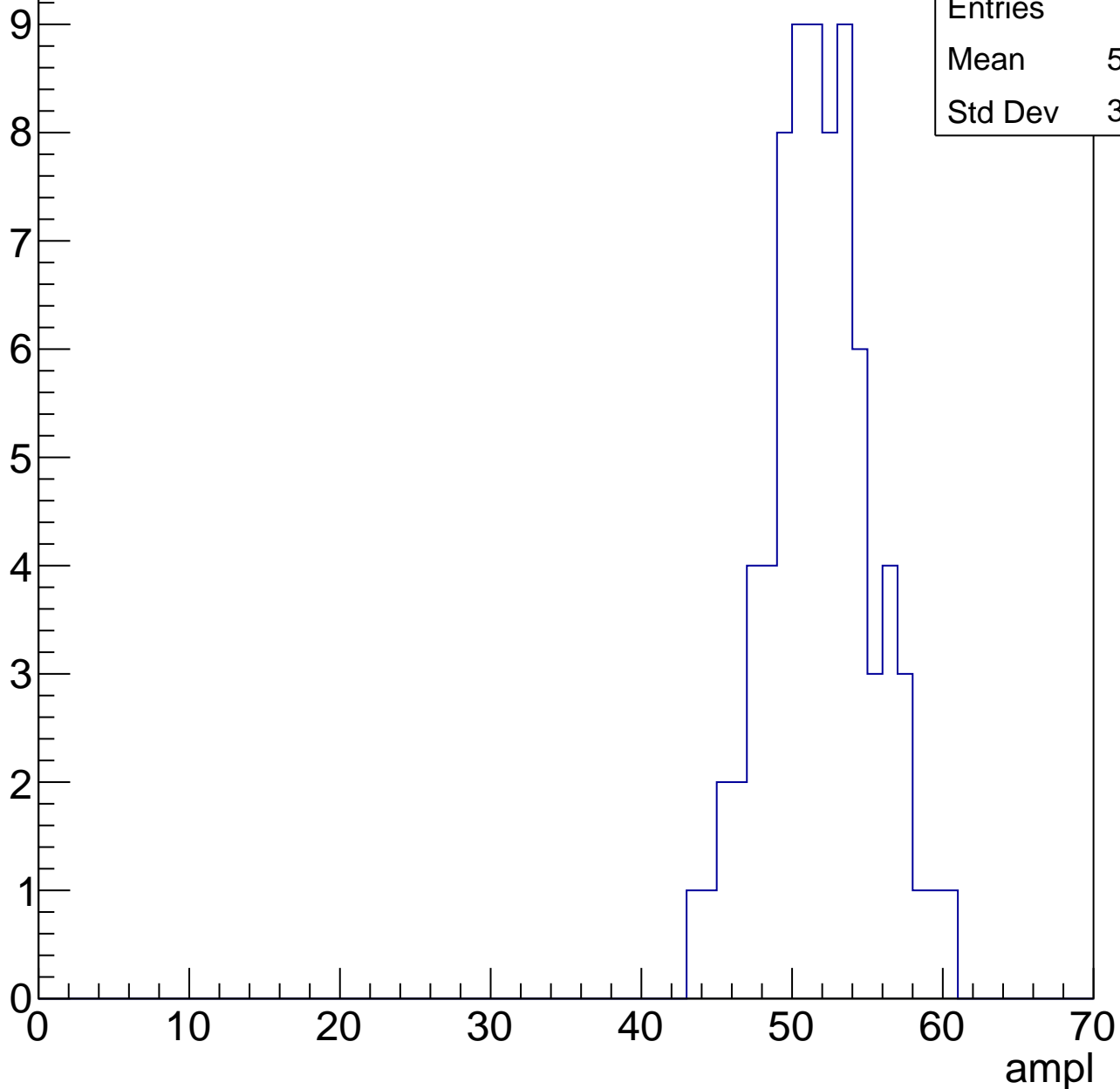
**Gaus Width: 3.5076**



# B0L001S, U17-ch46, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

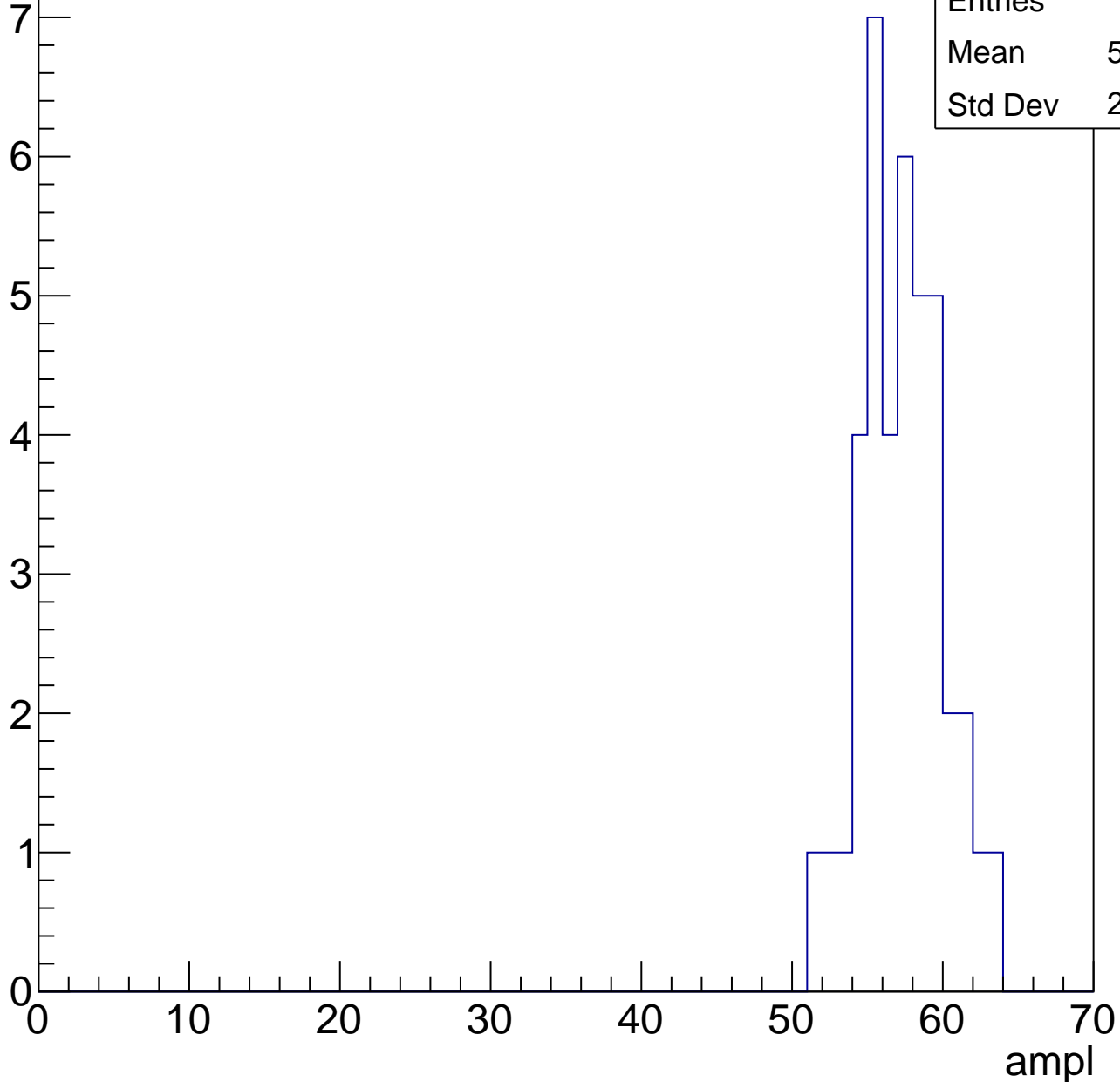


Entries	76
Mean	51.37
Std Dev	3.467

# B0L001S, U17-ch46, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



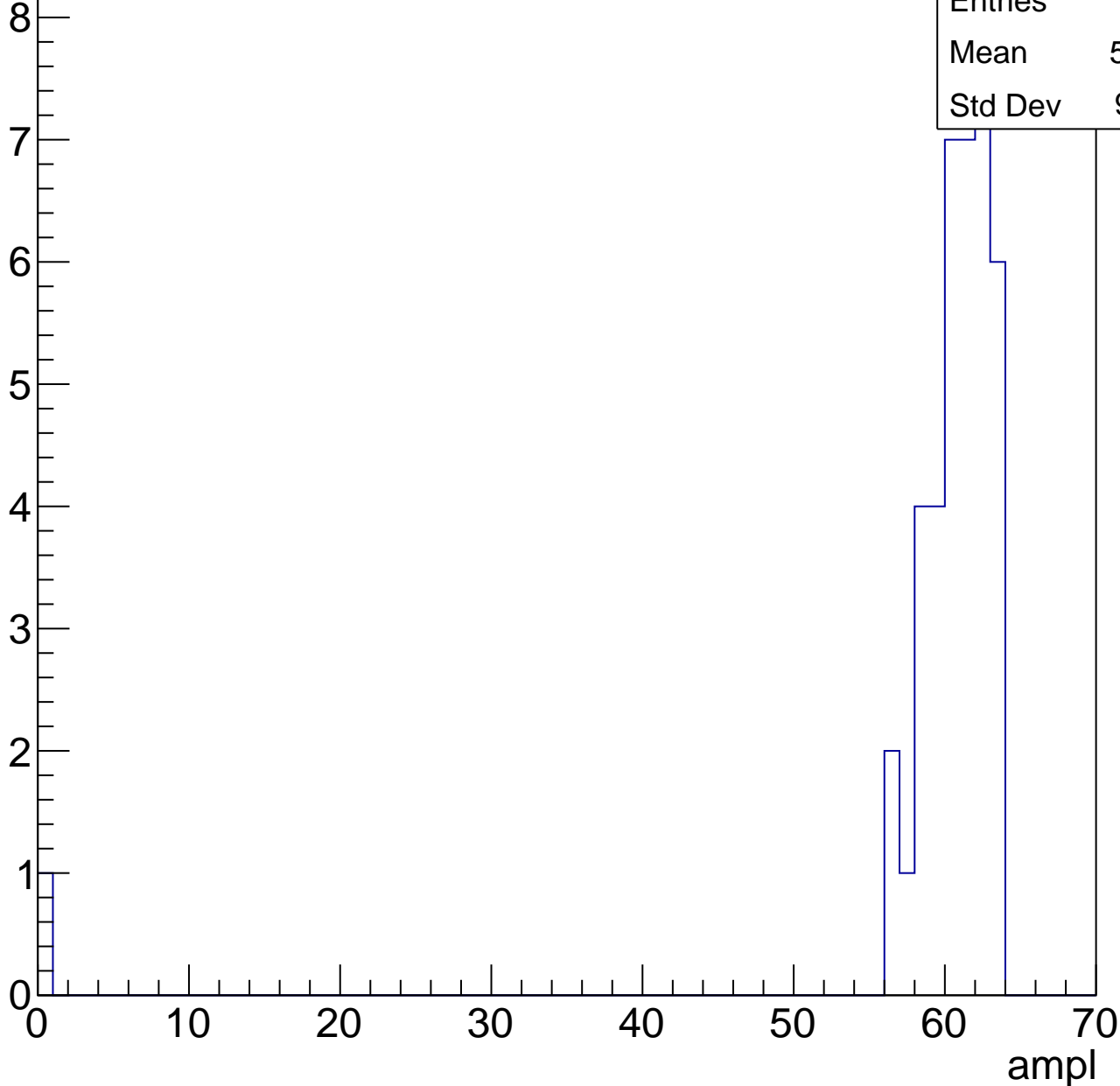
Entries	40
Mean	56.88
Std Dev	2.648

# B0L001S, U17-ch46, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	40
Mean	58.95
Std Dev	9.631



# B0L001S, U17-ch46, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch46, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U17-ch47, adc0

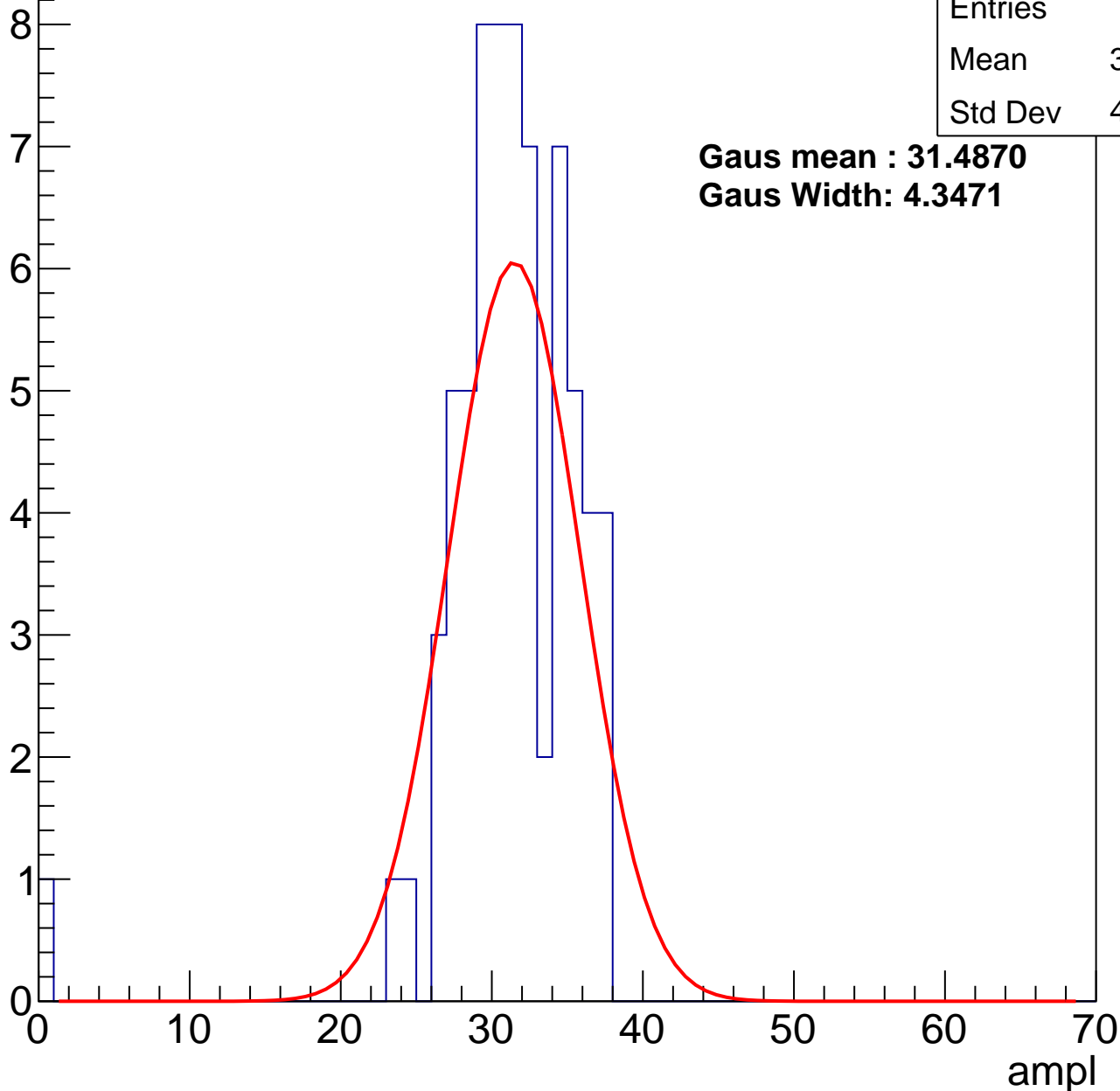
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	30.65
Std Dev	4.975

**Gaus mean : 31.4870**

**Gaus Width: 4.3471**



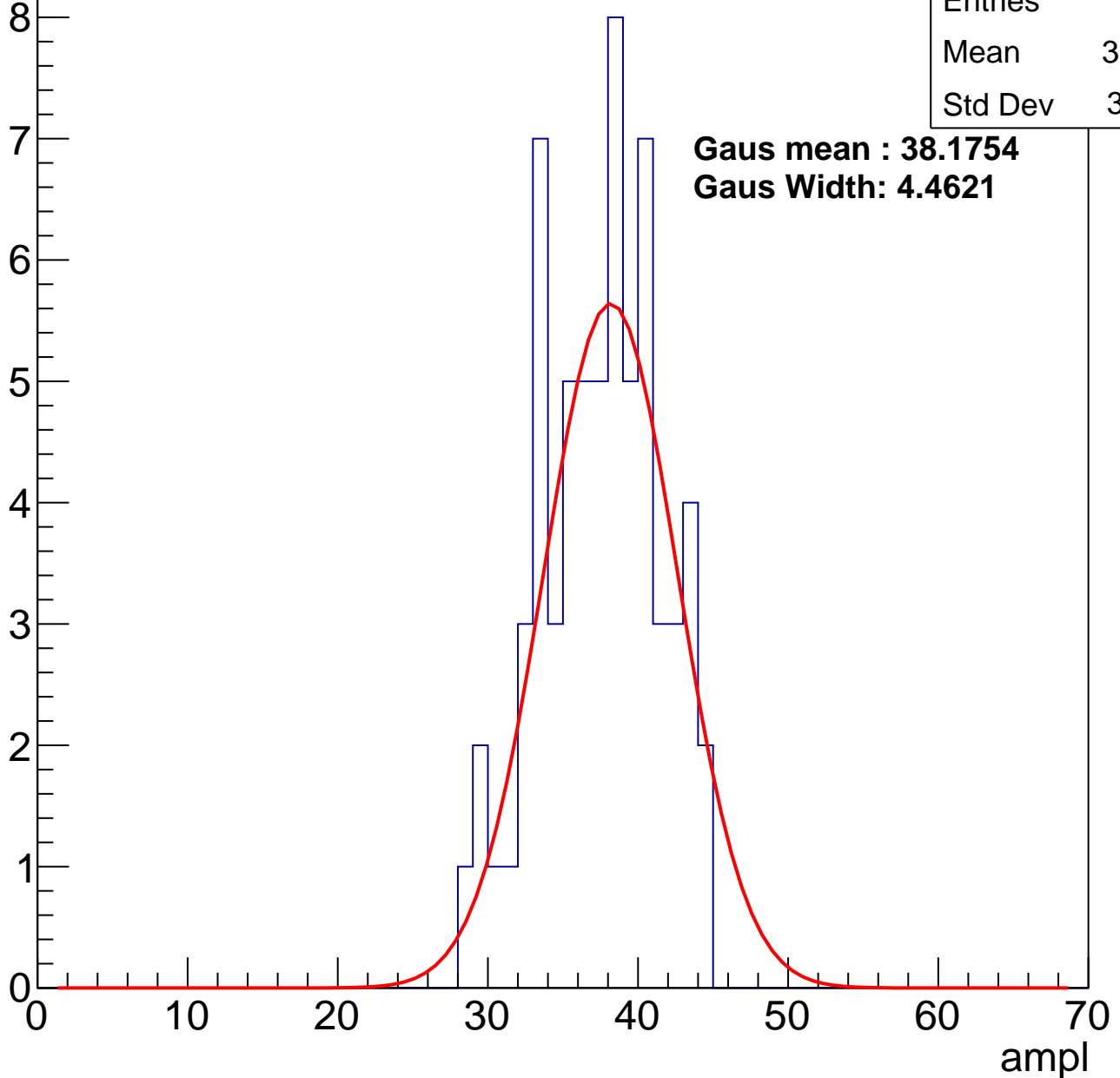
# B0L001S, U17-ch47, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	36.98
Std Dev	3.901

**Gaus mean : 38.1754**  
**Gaus Width: 4.4621**



# B0L001S, U17-ch47, adc2

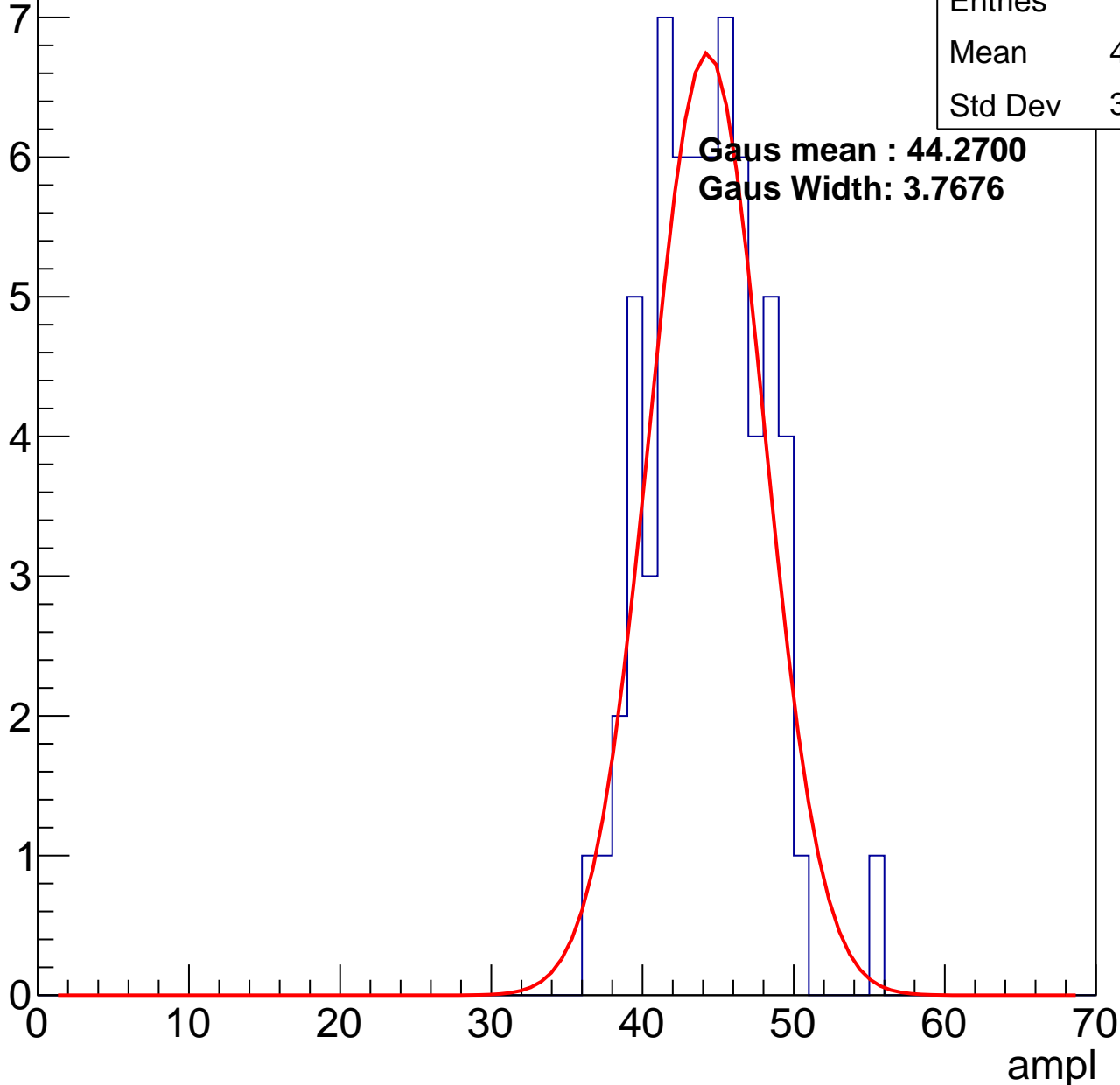
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	43.77
Std Dev	3.619

**Gaus mean : 44.2700**

**Gaus Width: 3.7676**

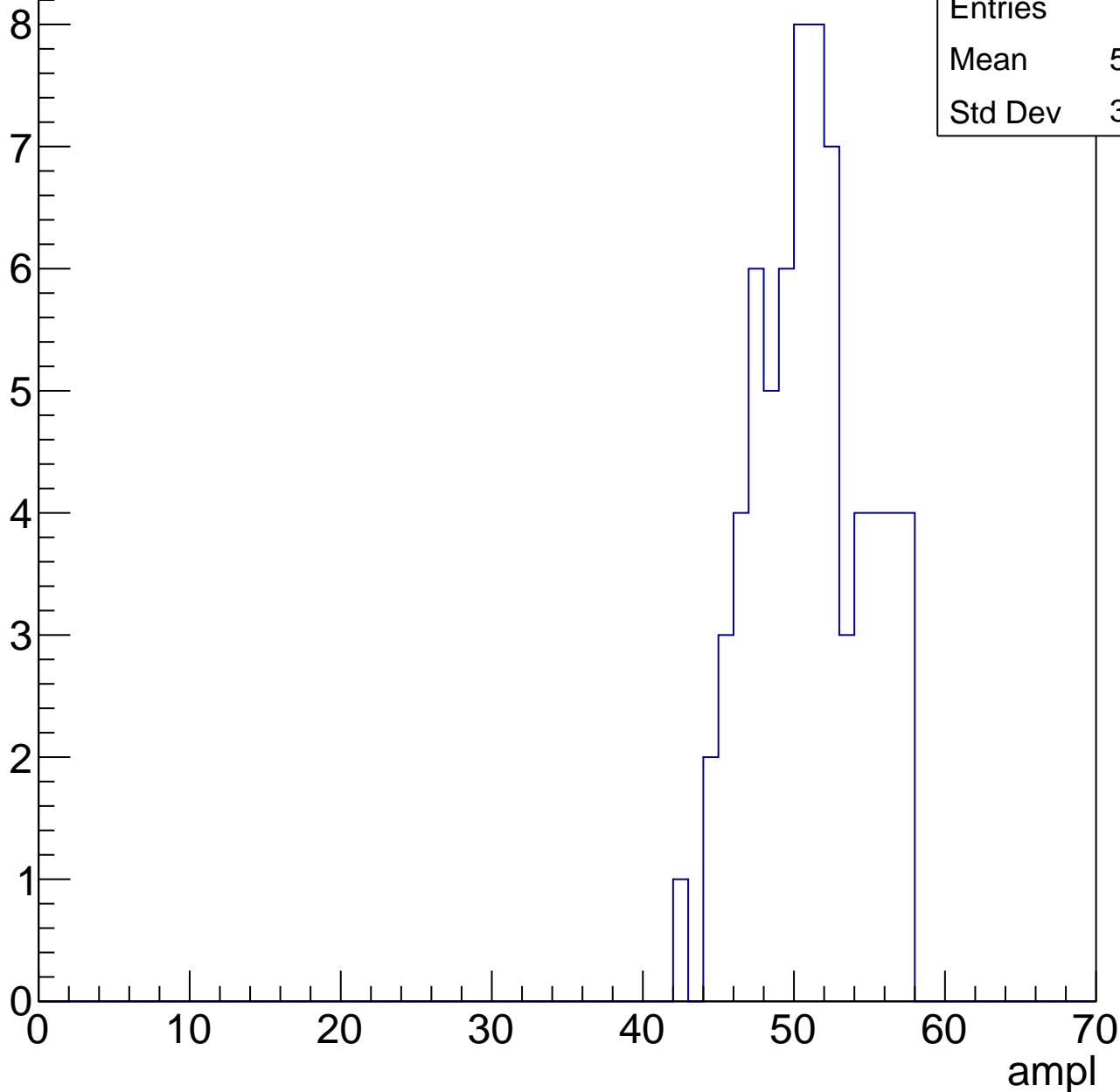


# B0L001S, U17-ch47, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	50.49
Std Dev	3.622

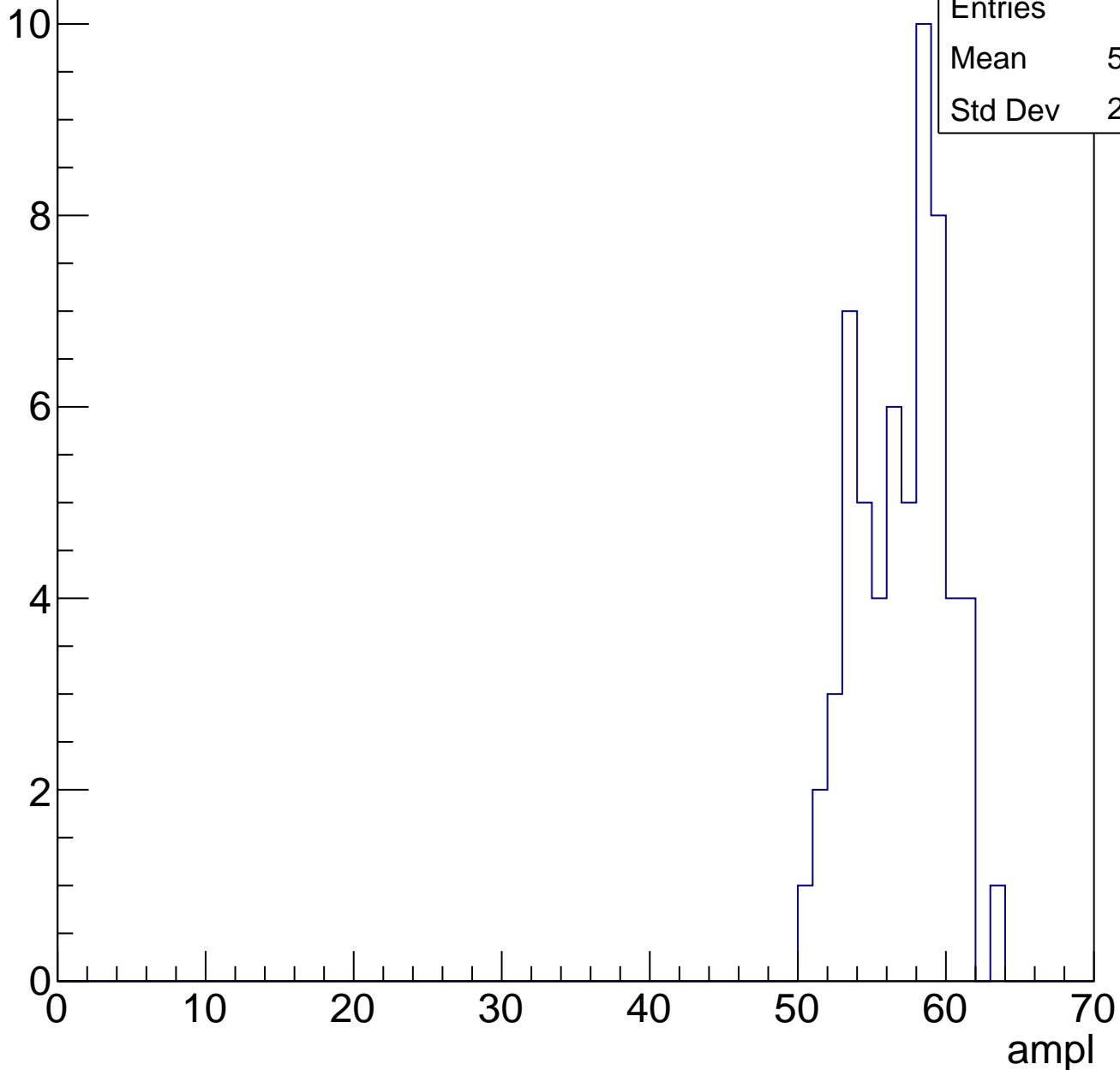


# B0L001S, U17-ch47, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	60
Mean	56.48
Std Dev	2.992

Entry

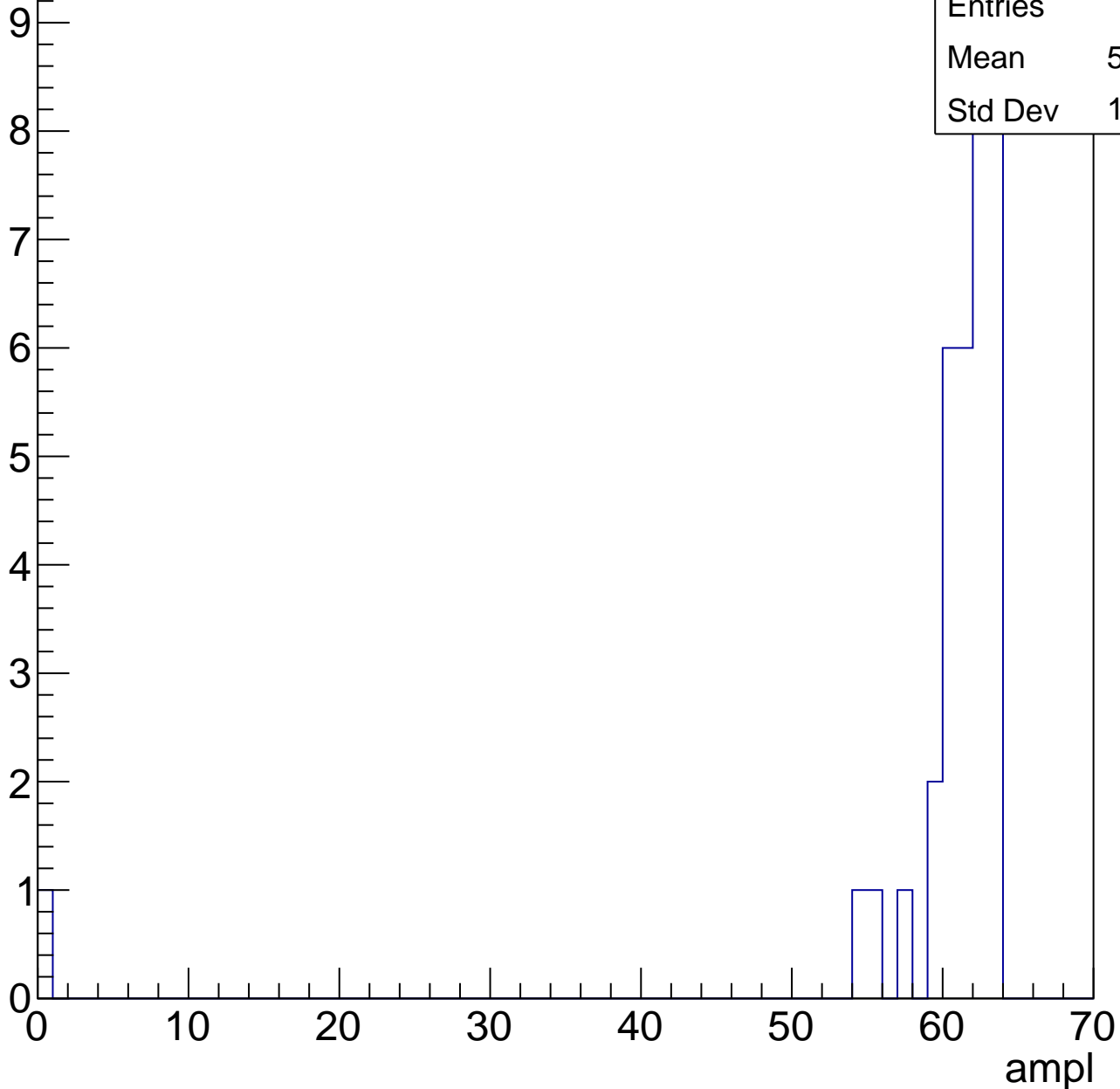


# B0L001S, U17-ch47, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	35
Mean	59.23
Std Dev	10.38



# B0L001S, U17-ch47, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch47, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U17-ch48, adc0

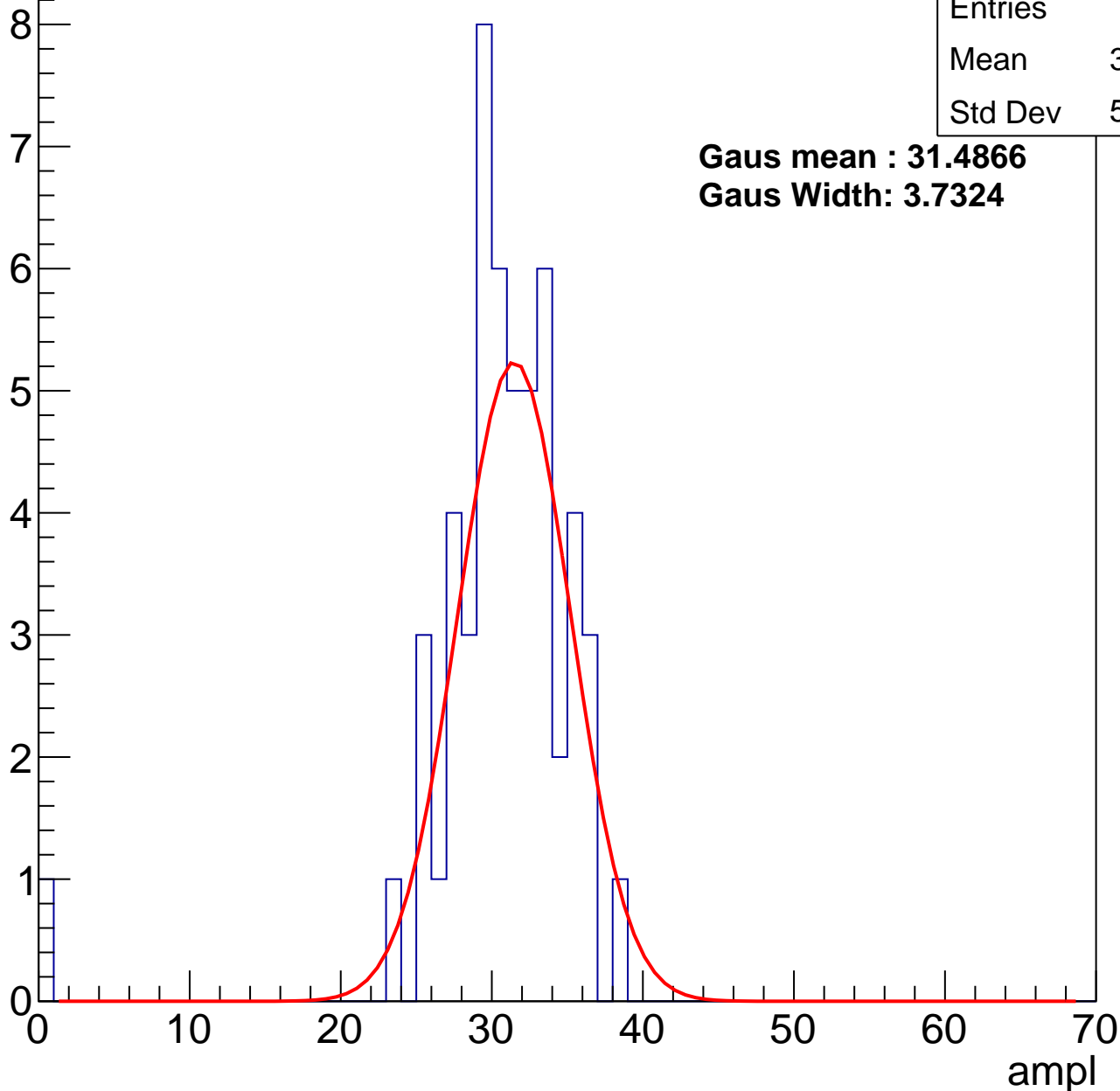
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	30.09
Std Dev	5.282

**Gaus mean : 31.4866**

**Gaus Width: 3.7324**



# B0L001S, U17-ch48, adc1

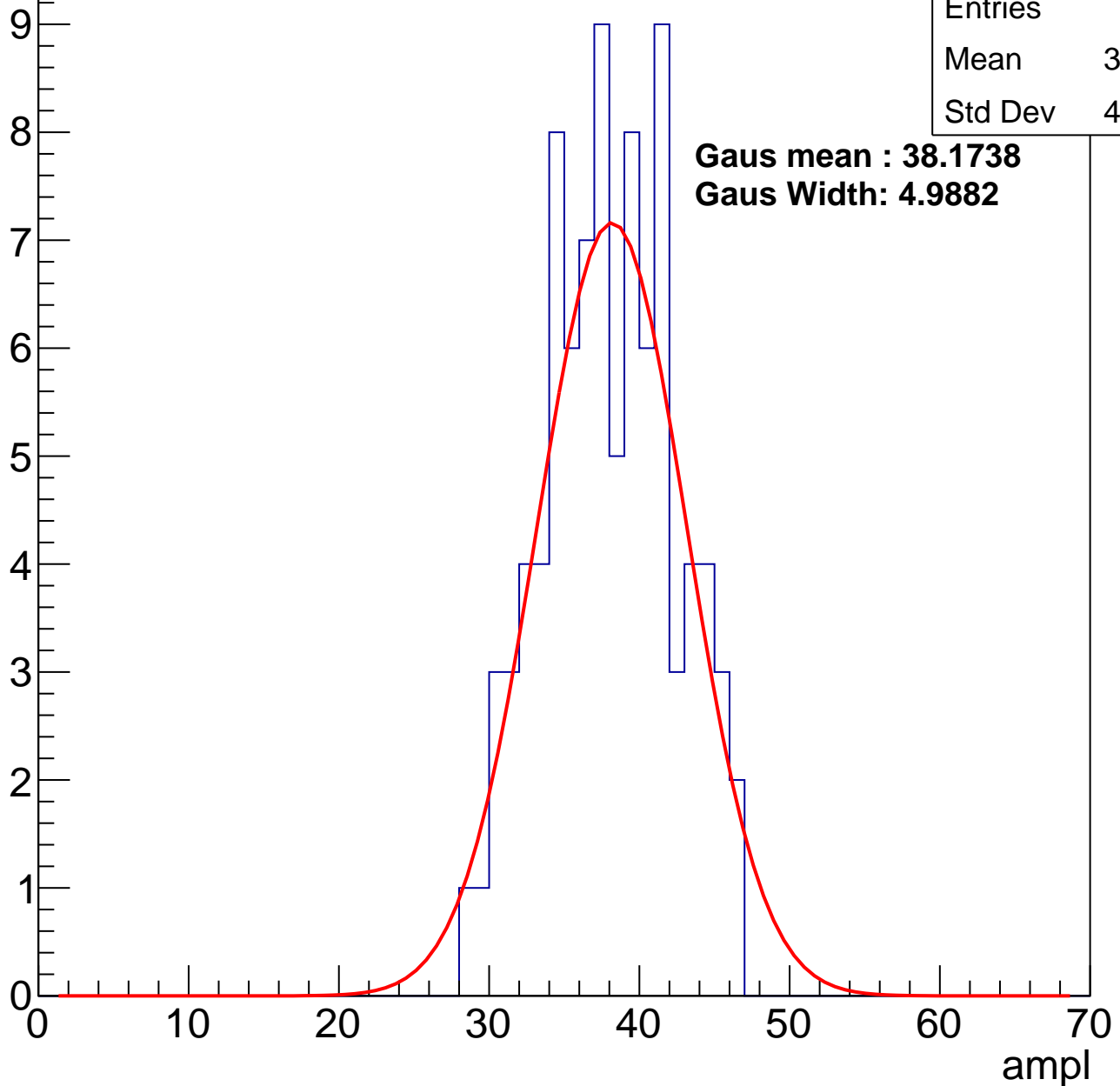
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	90
Mean	37.54
Std Dev	4.274

**Gaus mean : 38.1738**

**Gaus Width: 4.9882**



# B0L001S, U17-ch48, adc2

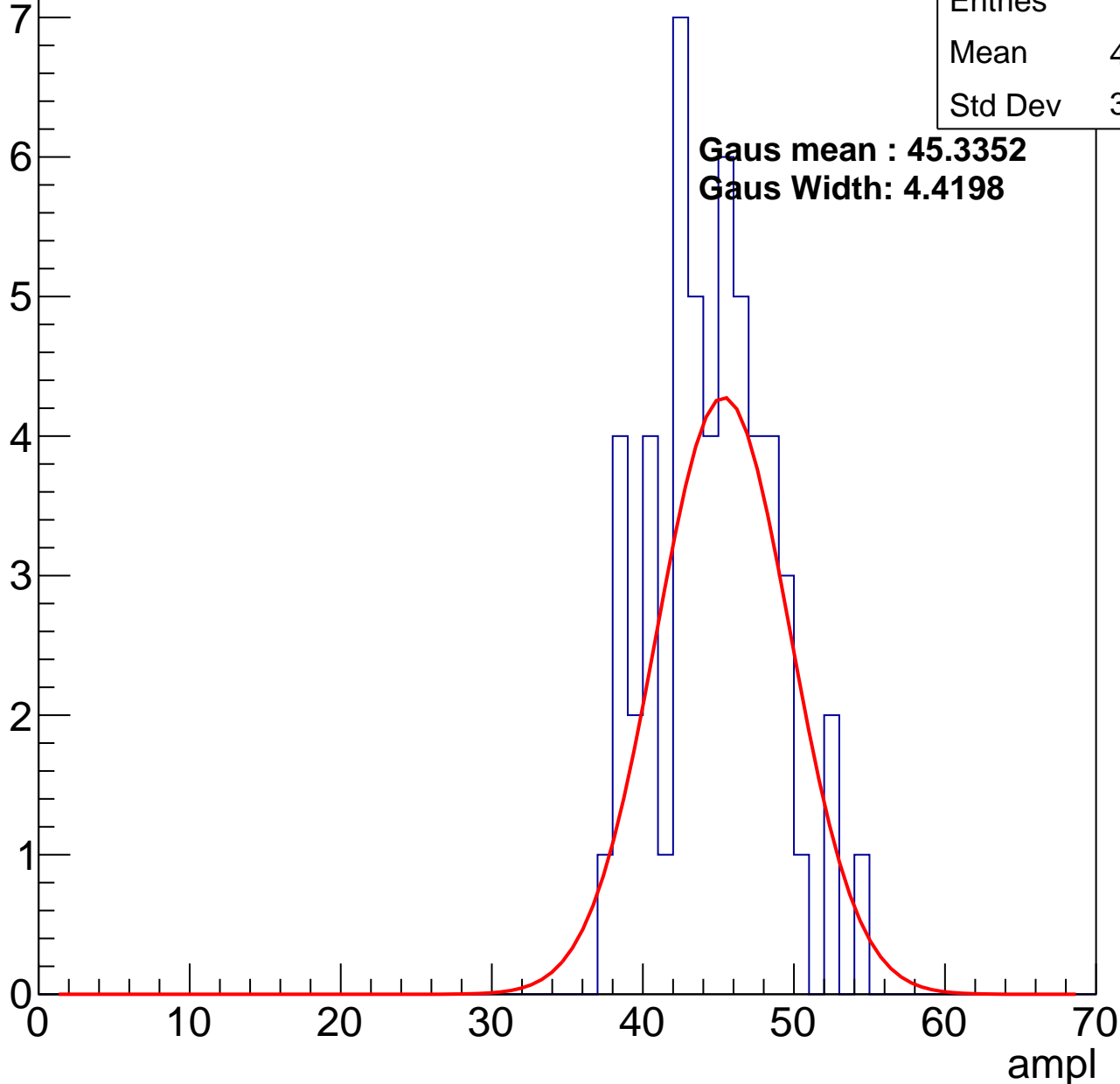
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	44.22
Std Dev	3.876

**Gaus mean : 45.3352**

**Gaus Width: 4.4198**

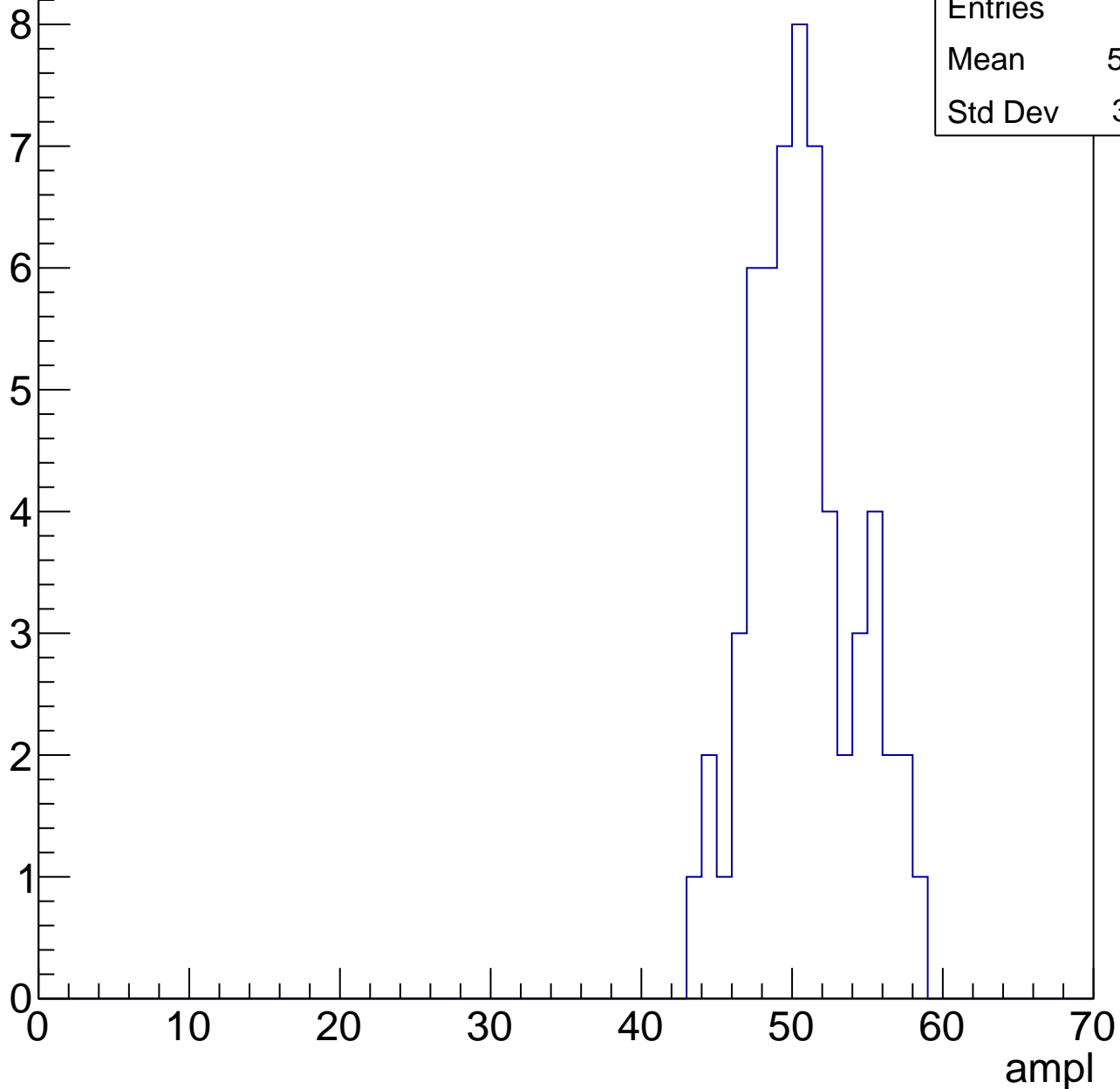


# B0L001S, U17-ch48, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	50.24
Std Dev	3.441

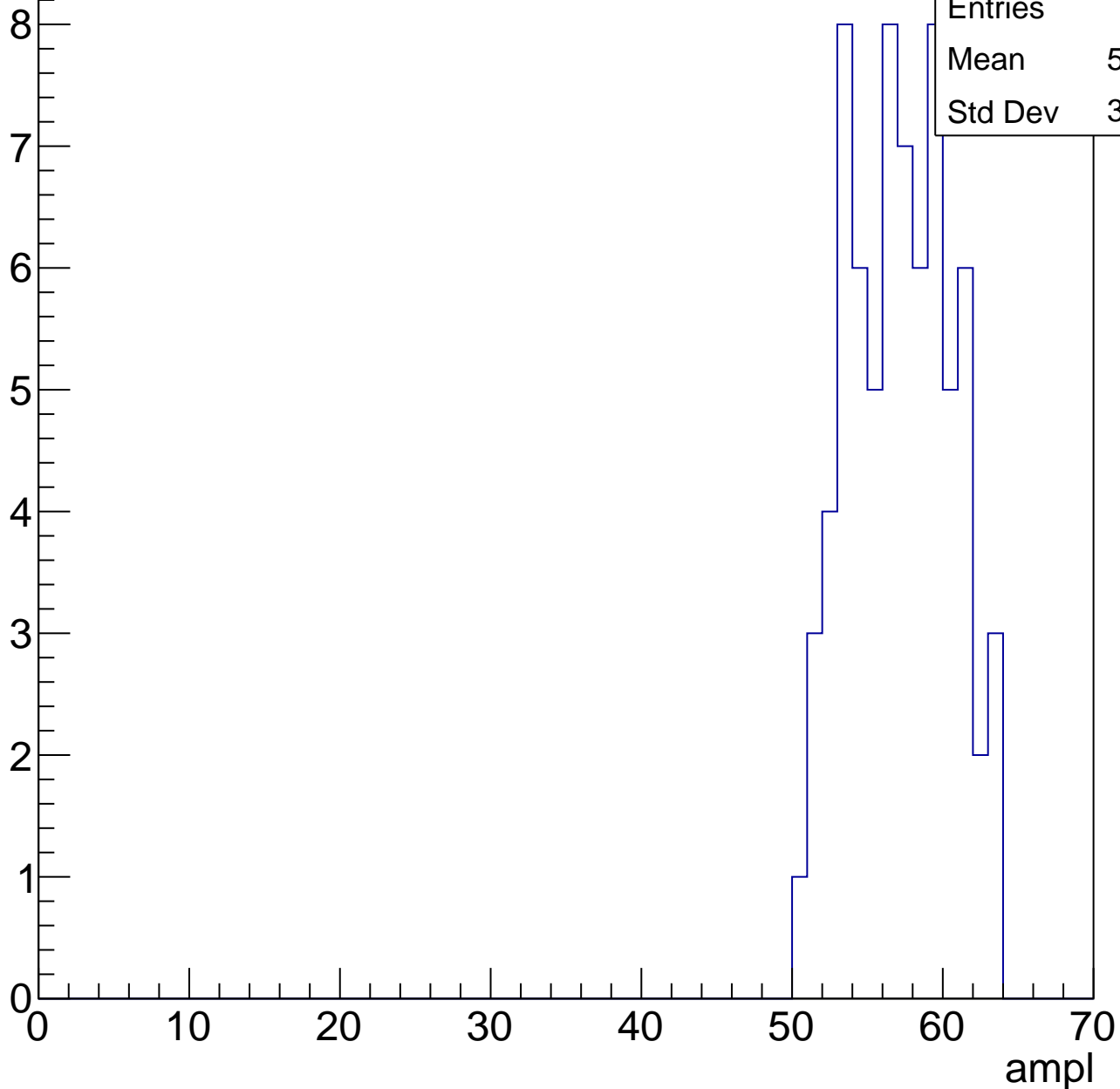


# B0L001S, U17-ch48, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	56.67
Std Dev	3.325

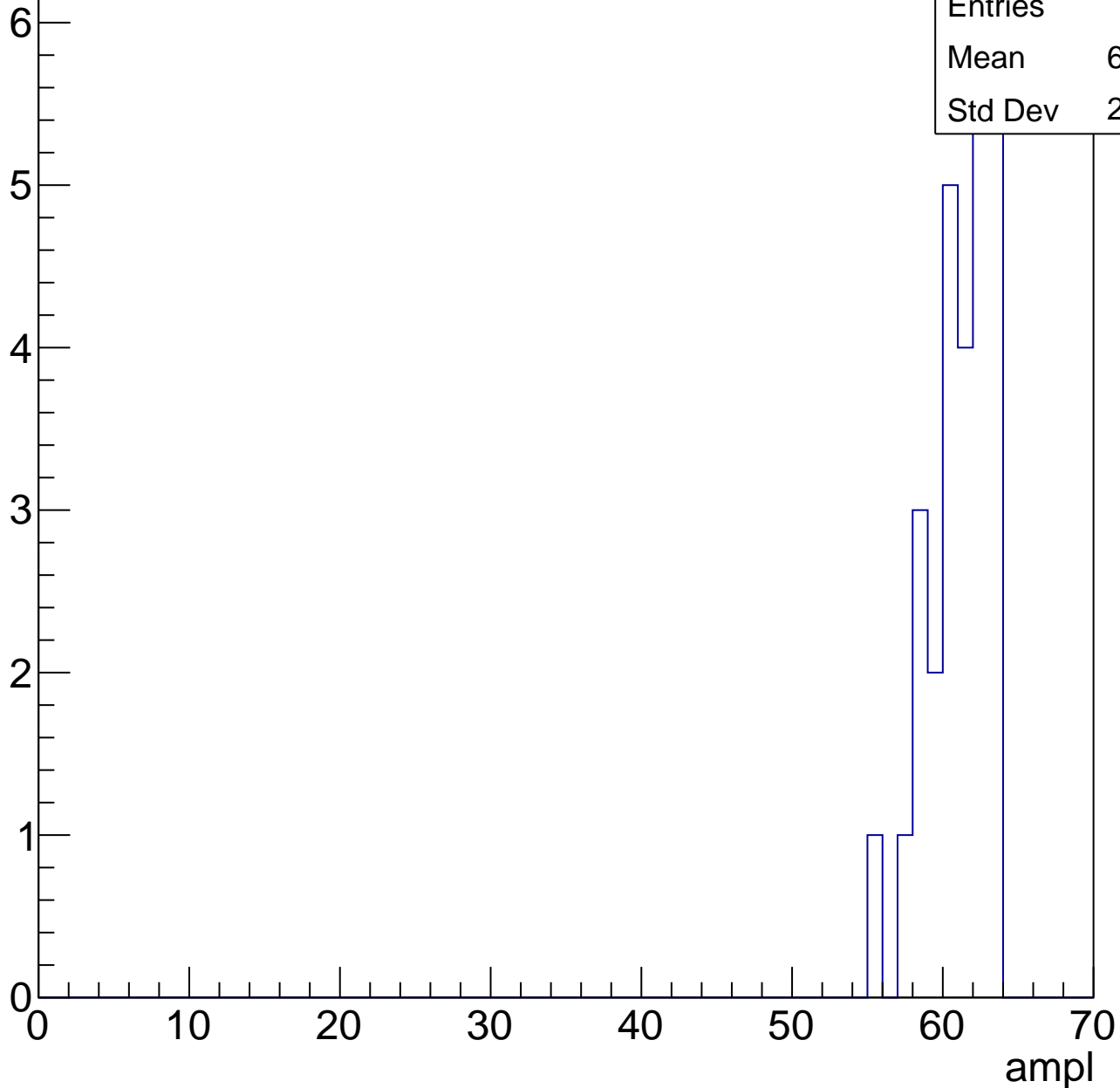


# B0L001S, U17-ch48, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	28
Mean	60.64
Std Dev	2.057



# B0L001S, U17-ch48, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	46.75
Std Dev	26.99

ampl



# B0L001S, U17-ch48, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U17-ch49, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	94
Mean	29.7
Std Dev	8.075

**Gaus mean : 31.8593**

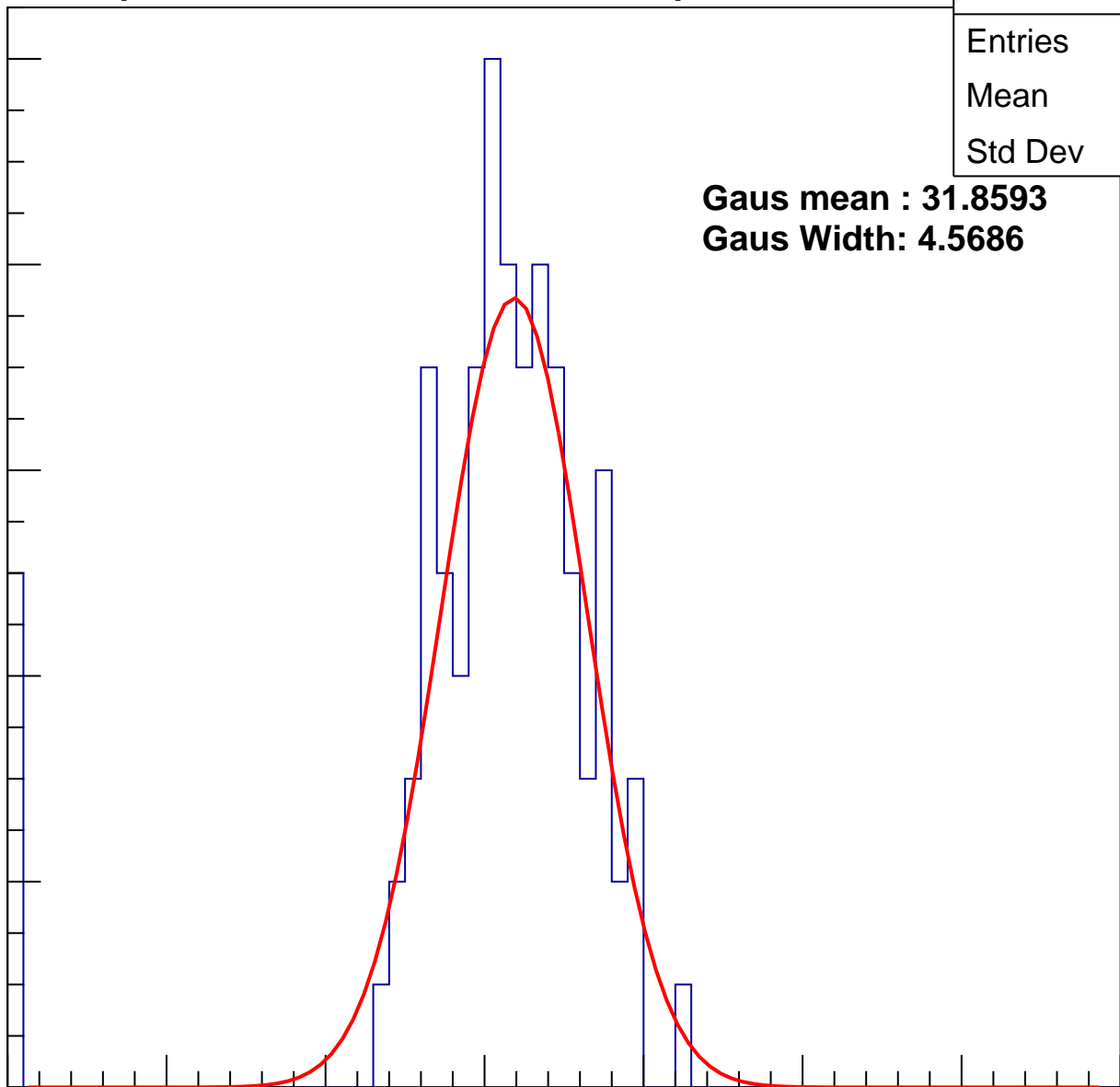
**Gaus Width: 4.5686**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U17-ch49, adc1

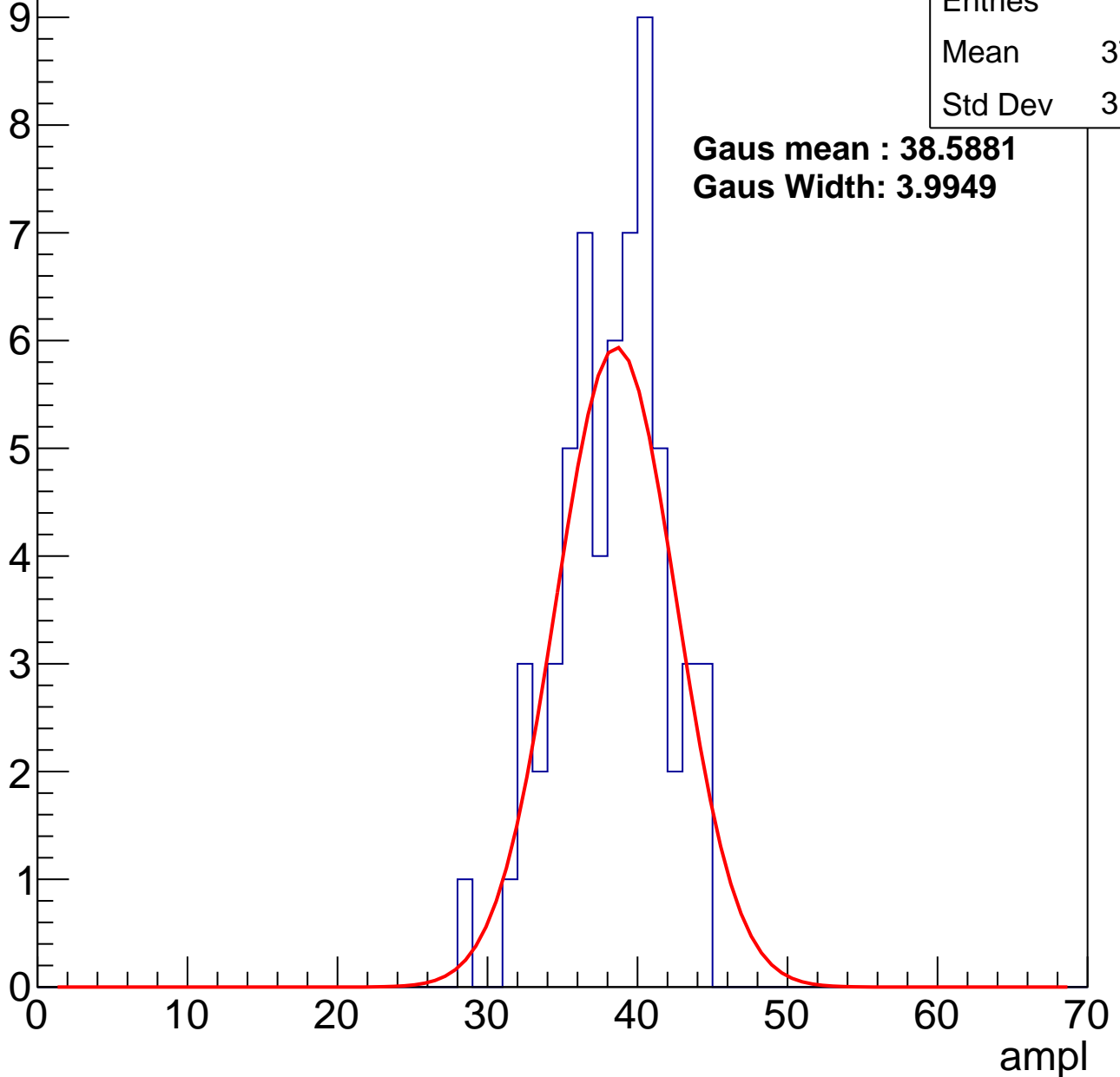
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	37.85
Std Dev	3.468

**Gaus mean : 38.5881**

**Gaus Width: 3.9949**



# B0L001S, U17-ch49, adc2

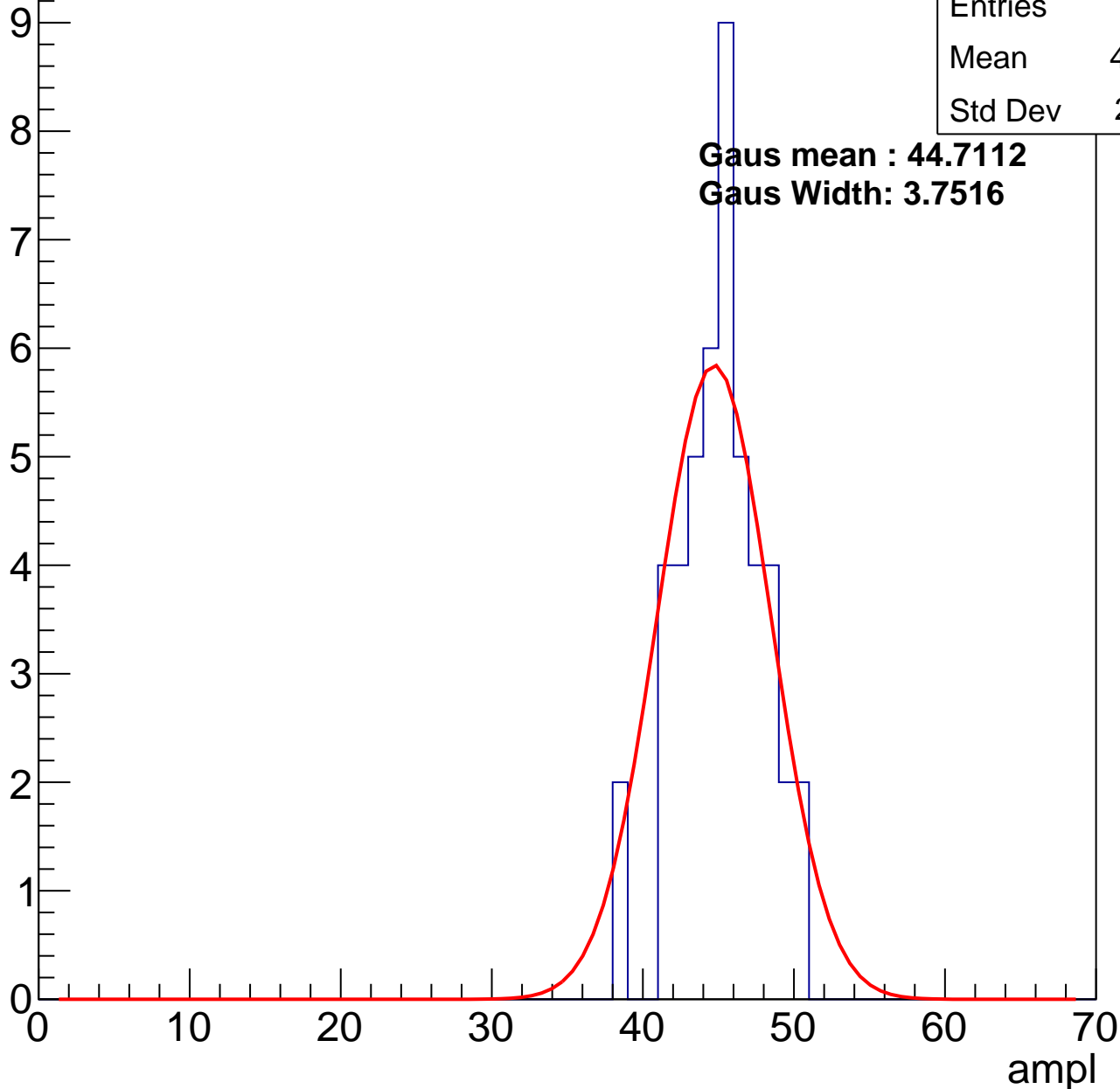
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	47
Mean	44.68
Std Dev	2.761

**Gaus mean : 44.7112**

**Gaus Width: 3.7516**

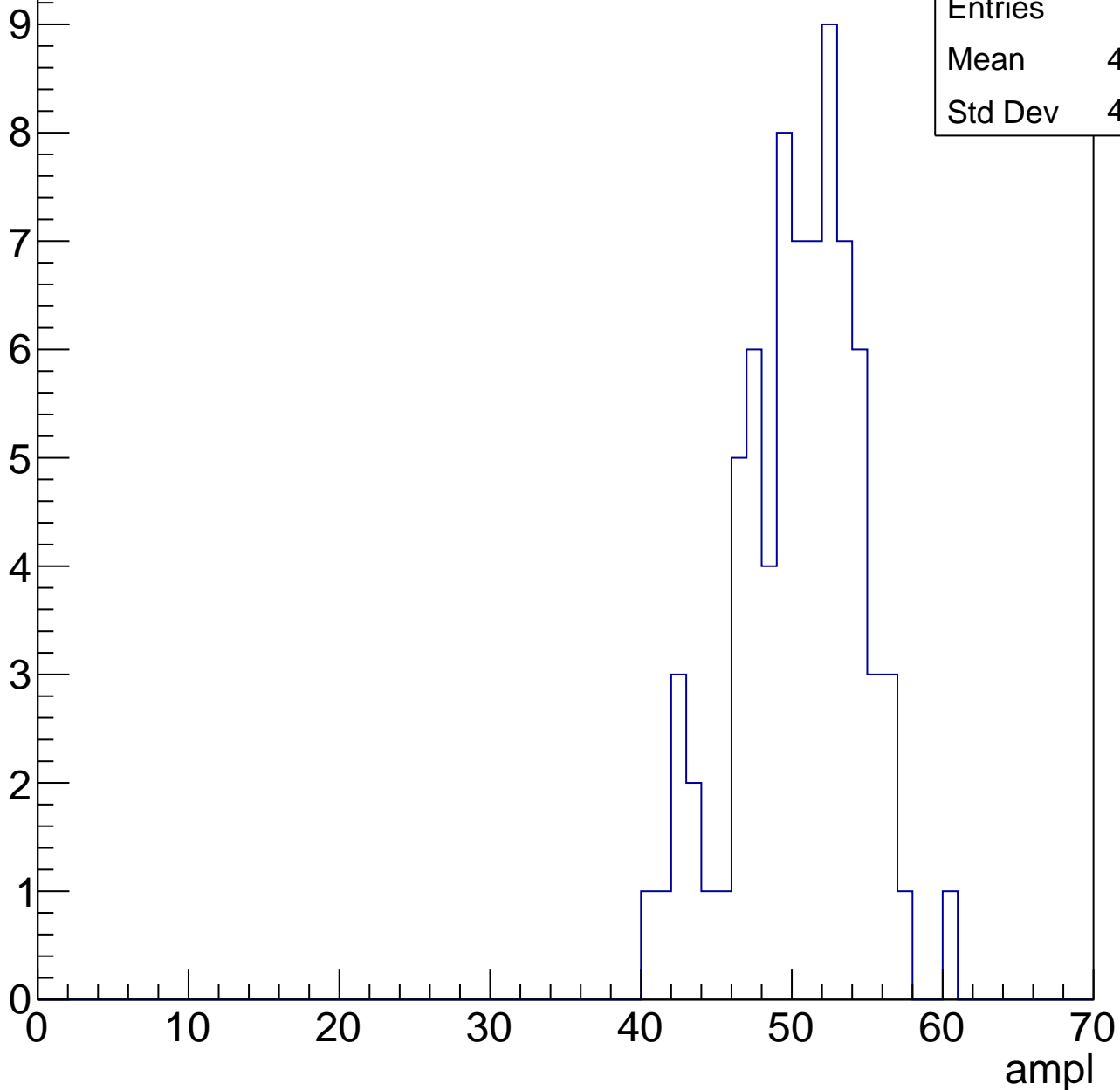


# B0L001S, U17-ch49, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	76
Mean	49.97
Std Dev	4.013

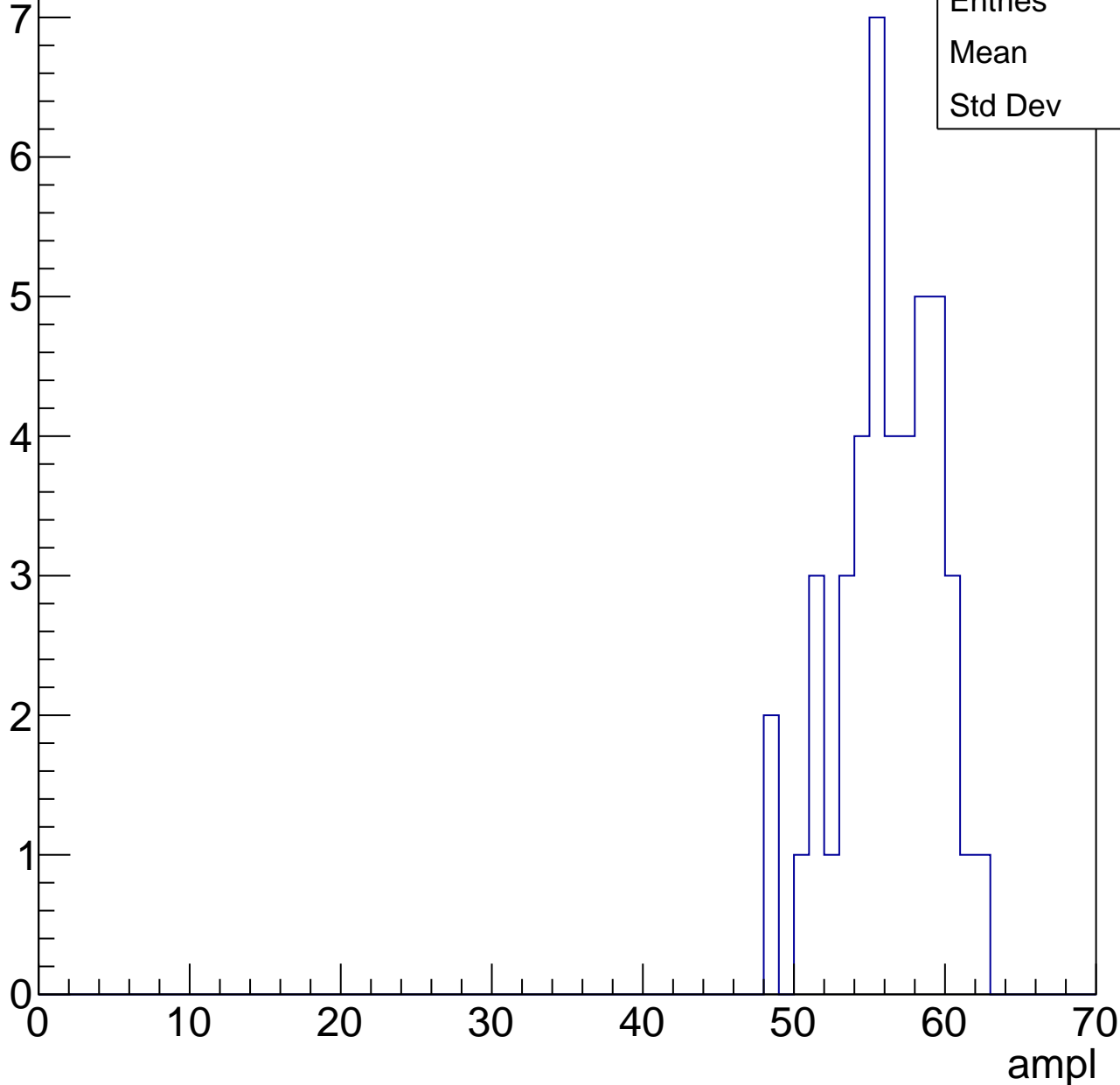


# B0L001S, U17-ch49, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

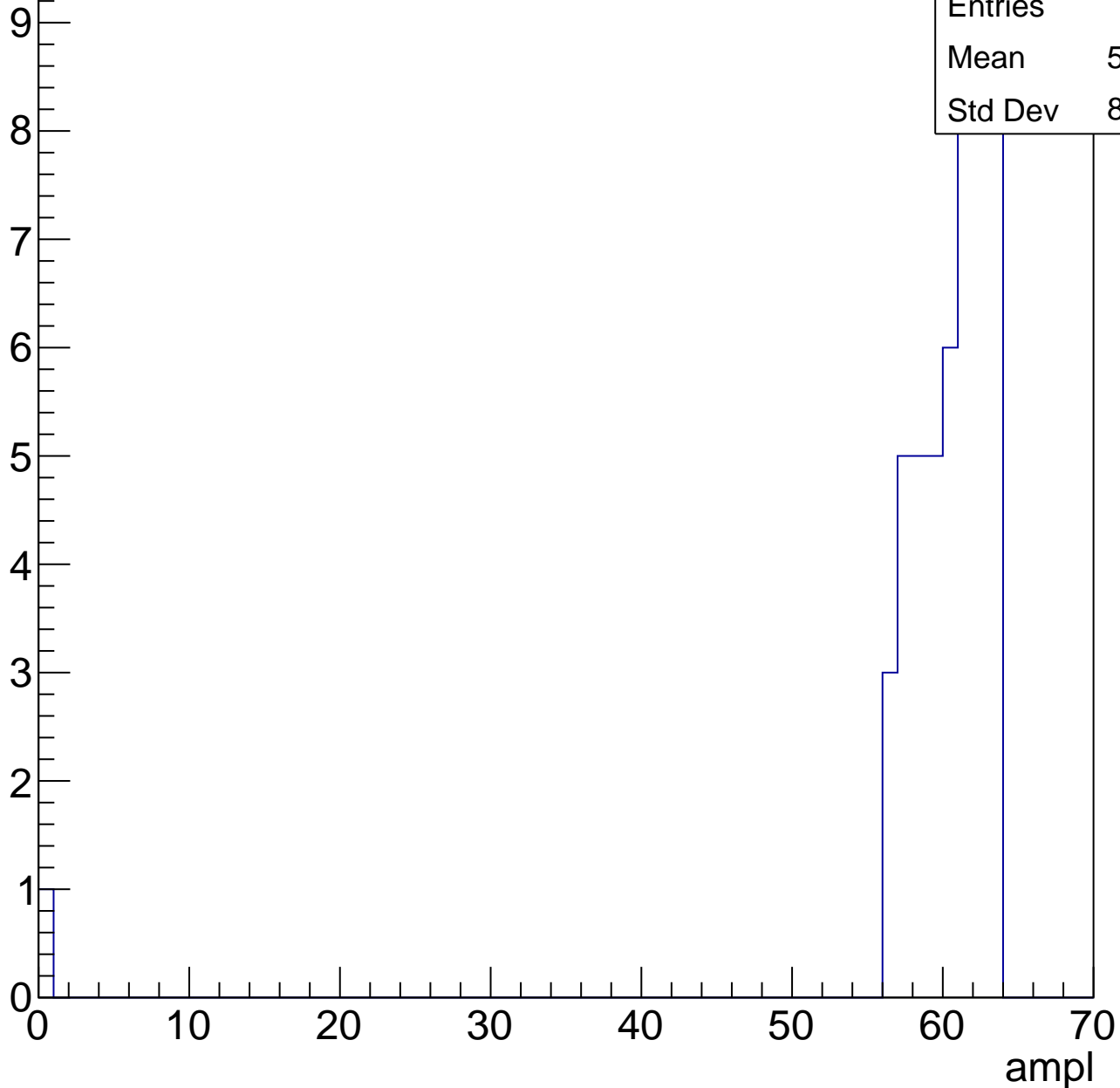
Entries	44
Mean	55.7
Std Dev	3.3



# B0L001S, U17-ch49, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U17-ch49, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch49, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U17-ch50, adc0

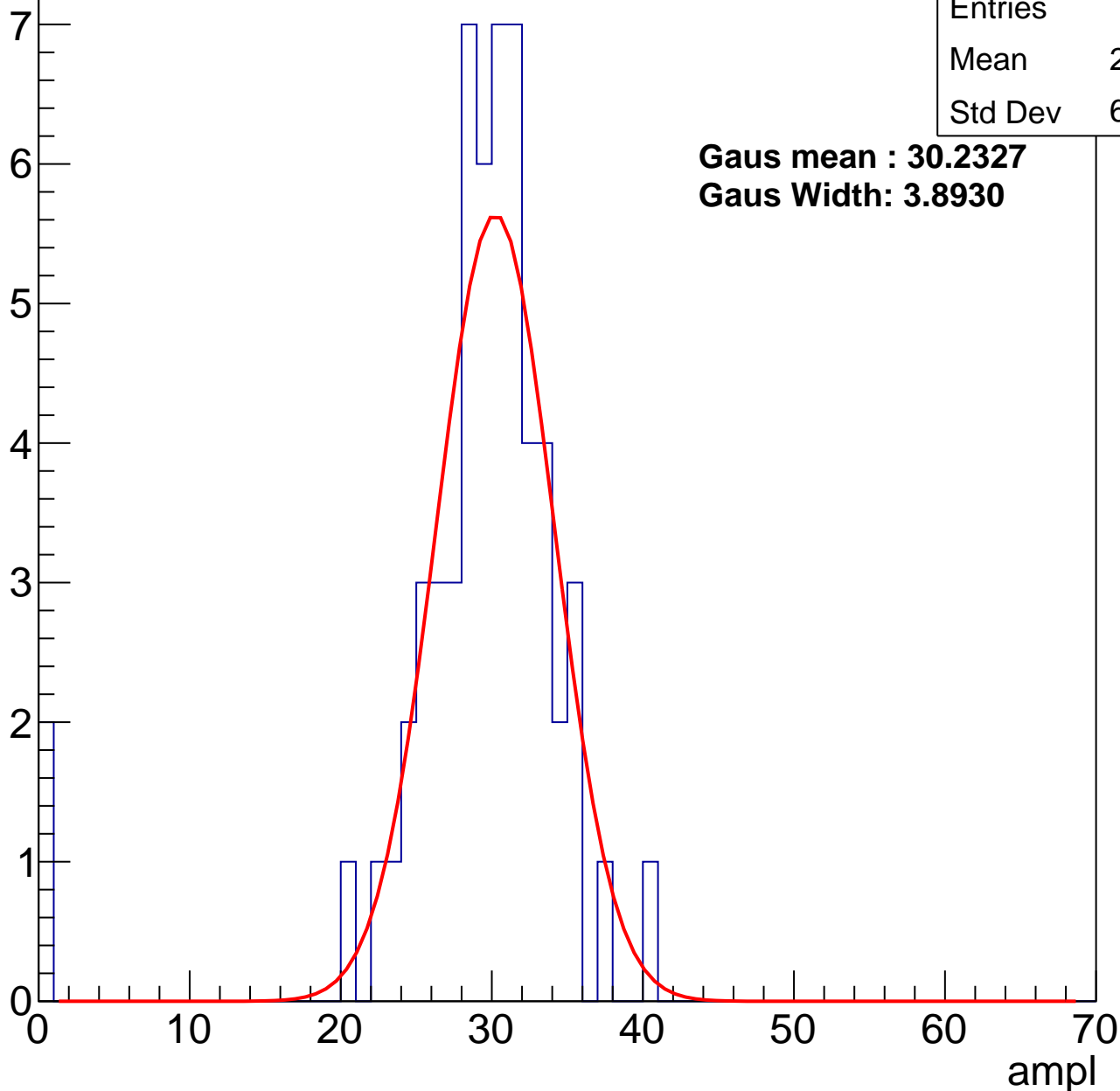
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	28.52
Std Dev	6.508

**Gaus mean : 30.2327**

**Gaus Width: 3.8930**



# B0L001S, U17-ch50, adc1

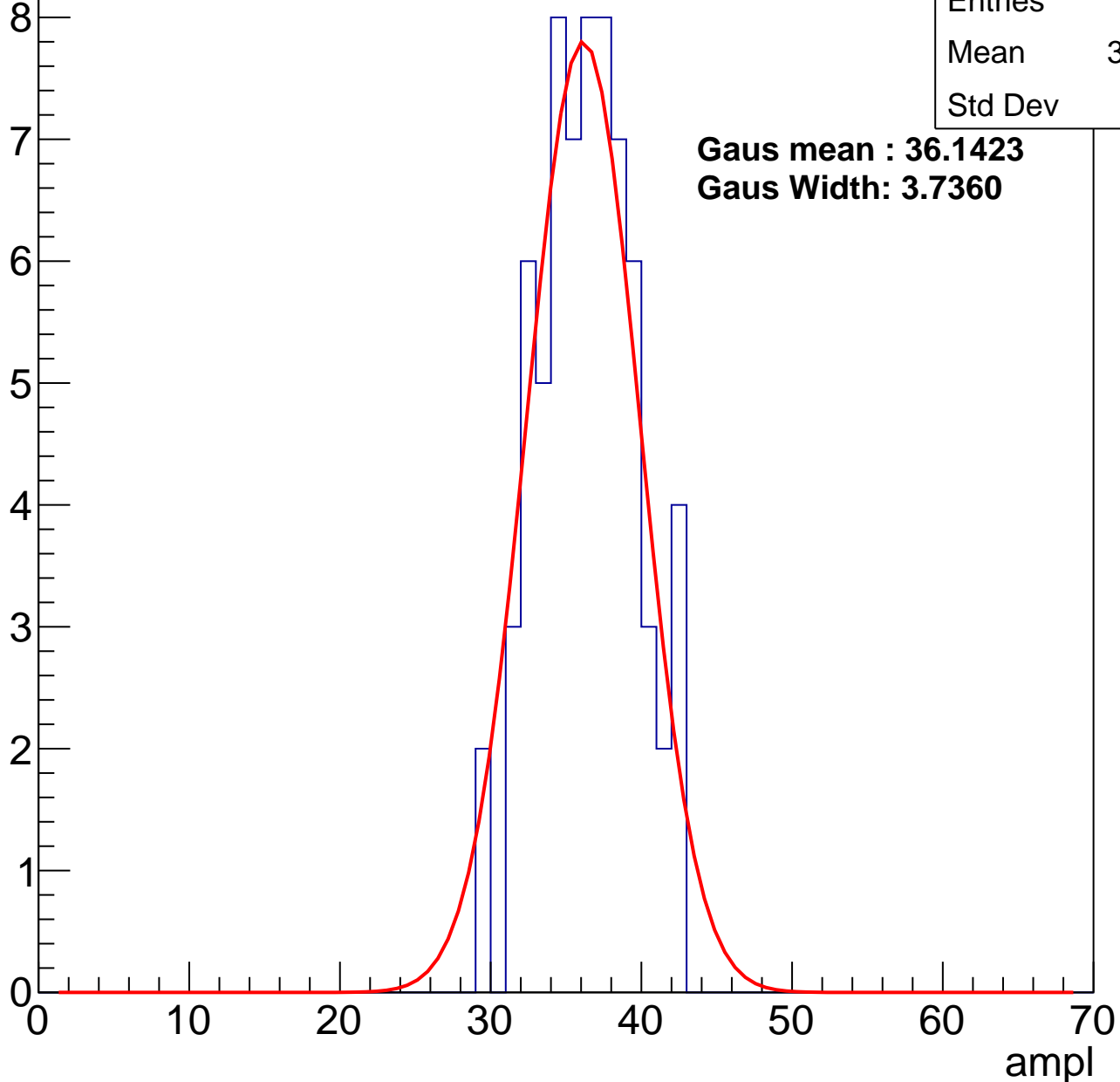
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	35.93
Std Dev	3.15

**Gaus mean : 36.1423**

**Gaus Width: 3.7360**



# B0L001S, U17-ch50, adc2

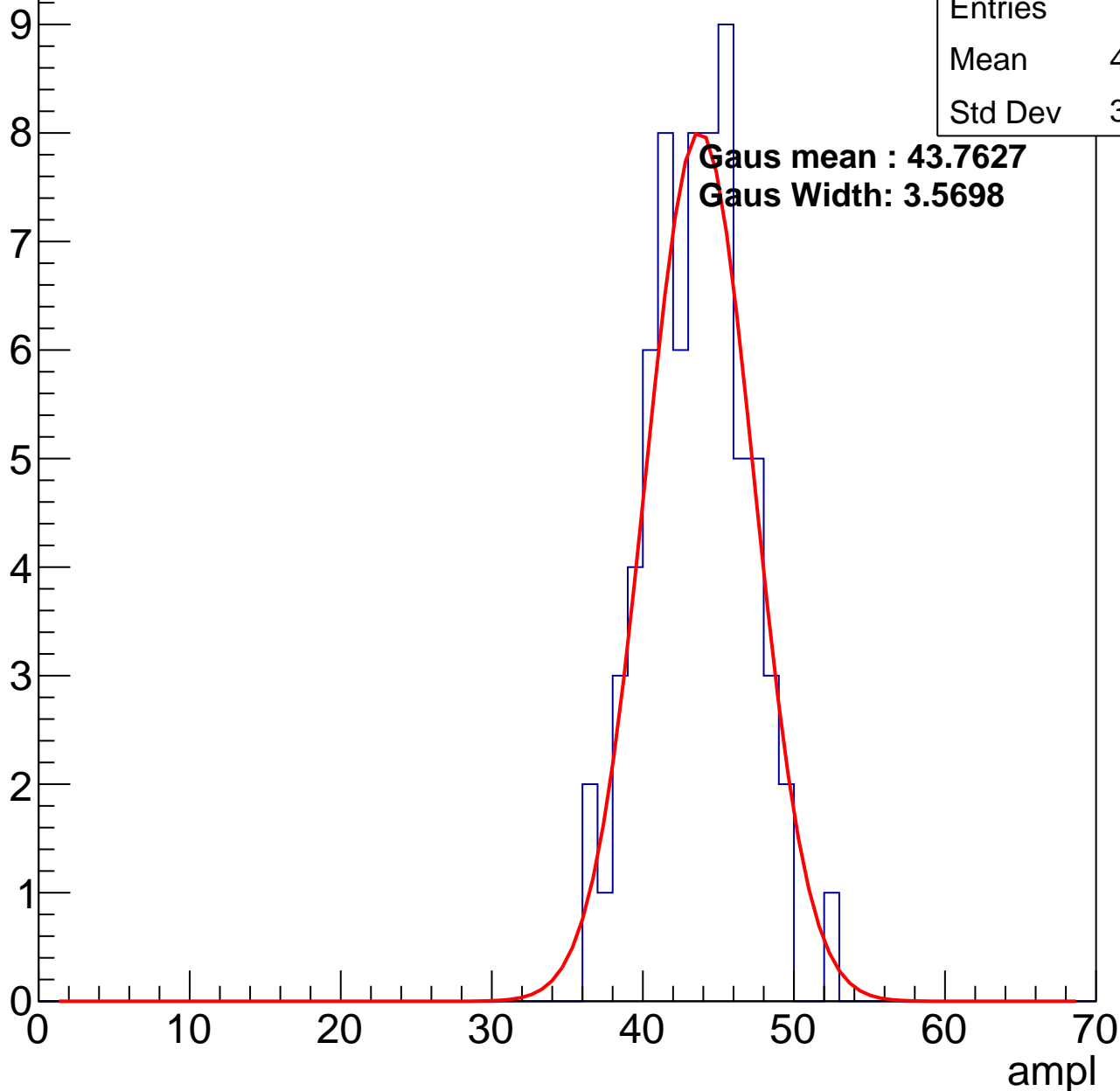
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	43.08
Std Dev	3.275

**Gaus mean : 43.7627**

**Gaus Width: 3.5698**

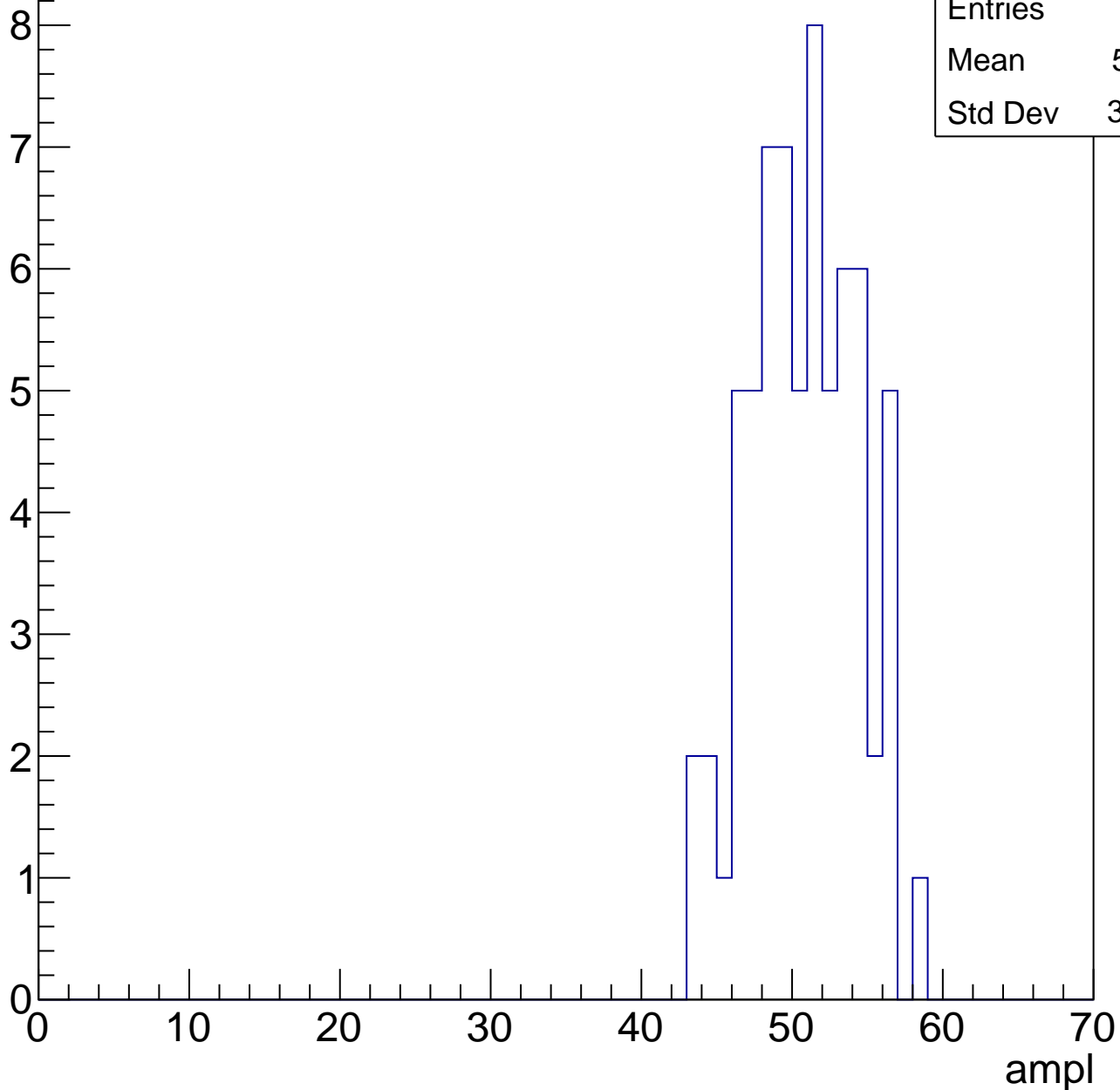


# B0L001S, U17-ch50, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	50.31
Std Dev	3.499

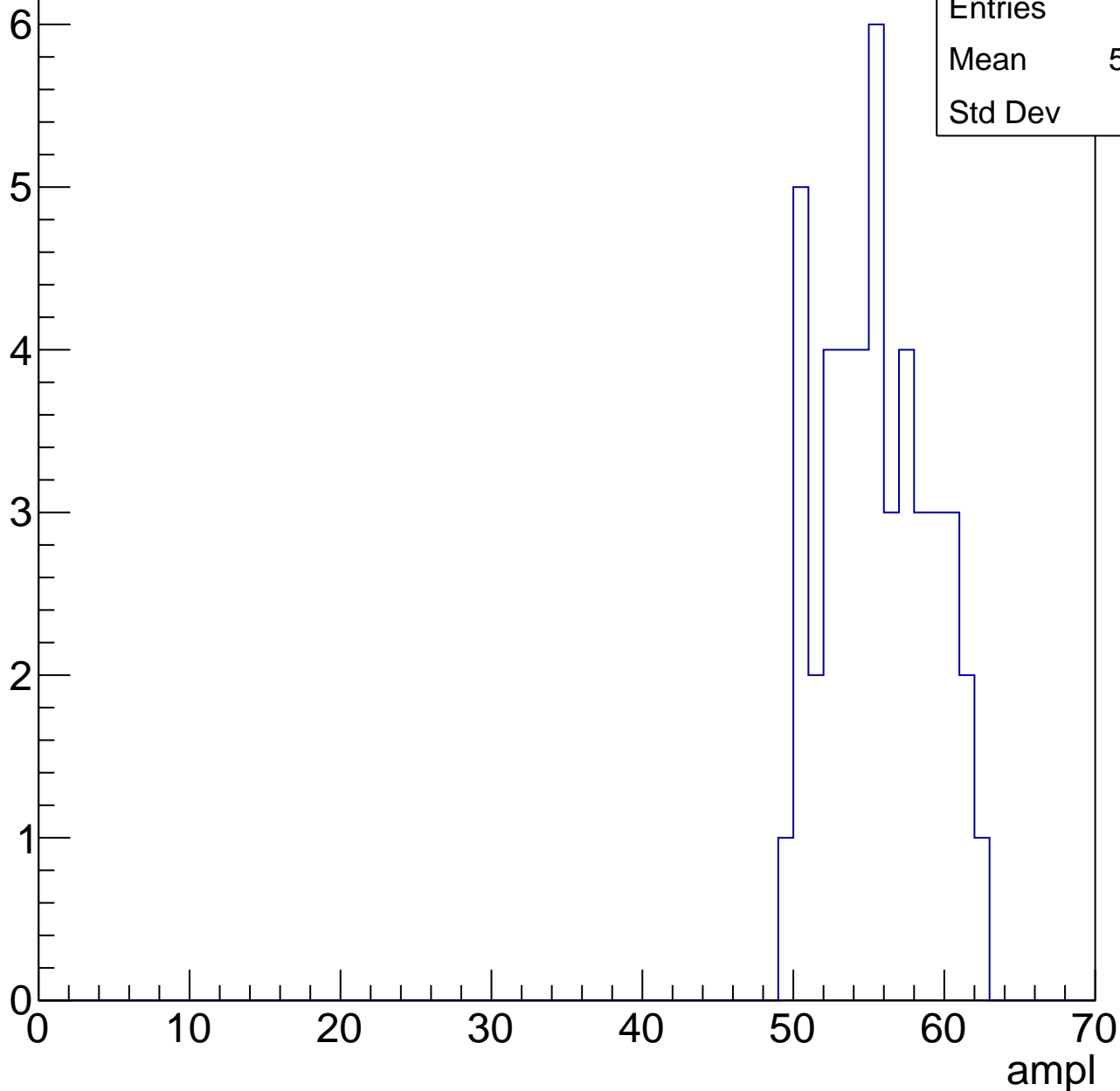


# B0L001S, U17-ch50, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	45
Mean	55.07
Std Dev	3.46

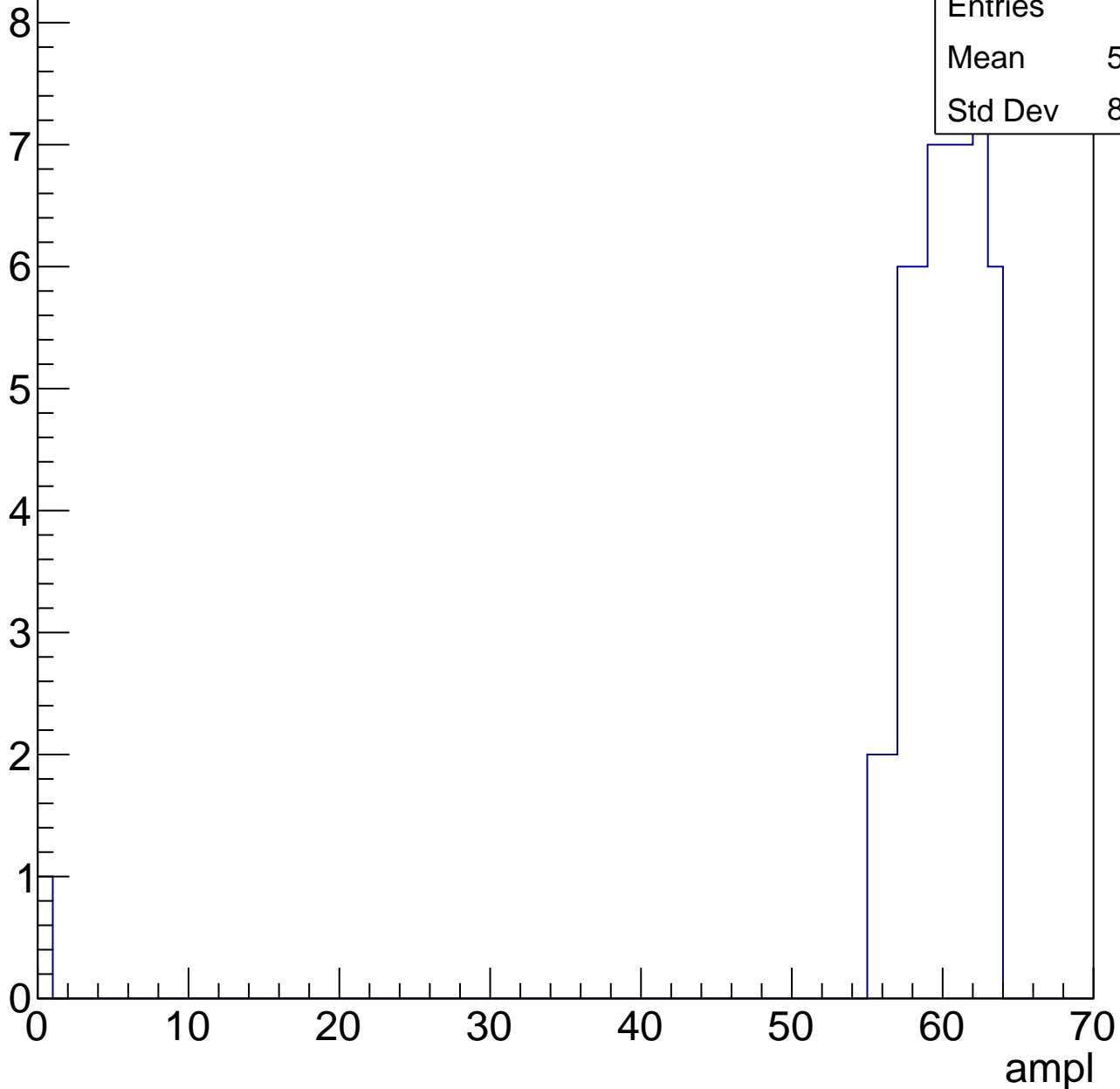


# B0L001S, U17-ch50, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	58.58
Std Dev	8.497



# B0L001S, U17-ch50, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	6
Mean	62.5
Std Dev	0.7638



# B0L001S, U17-ch50, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U17-ch51, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	65
Mean	30.08
Std Dev	6.202

**Gaus mean : 31.4616**

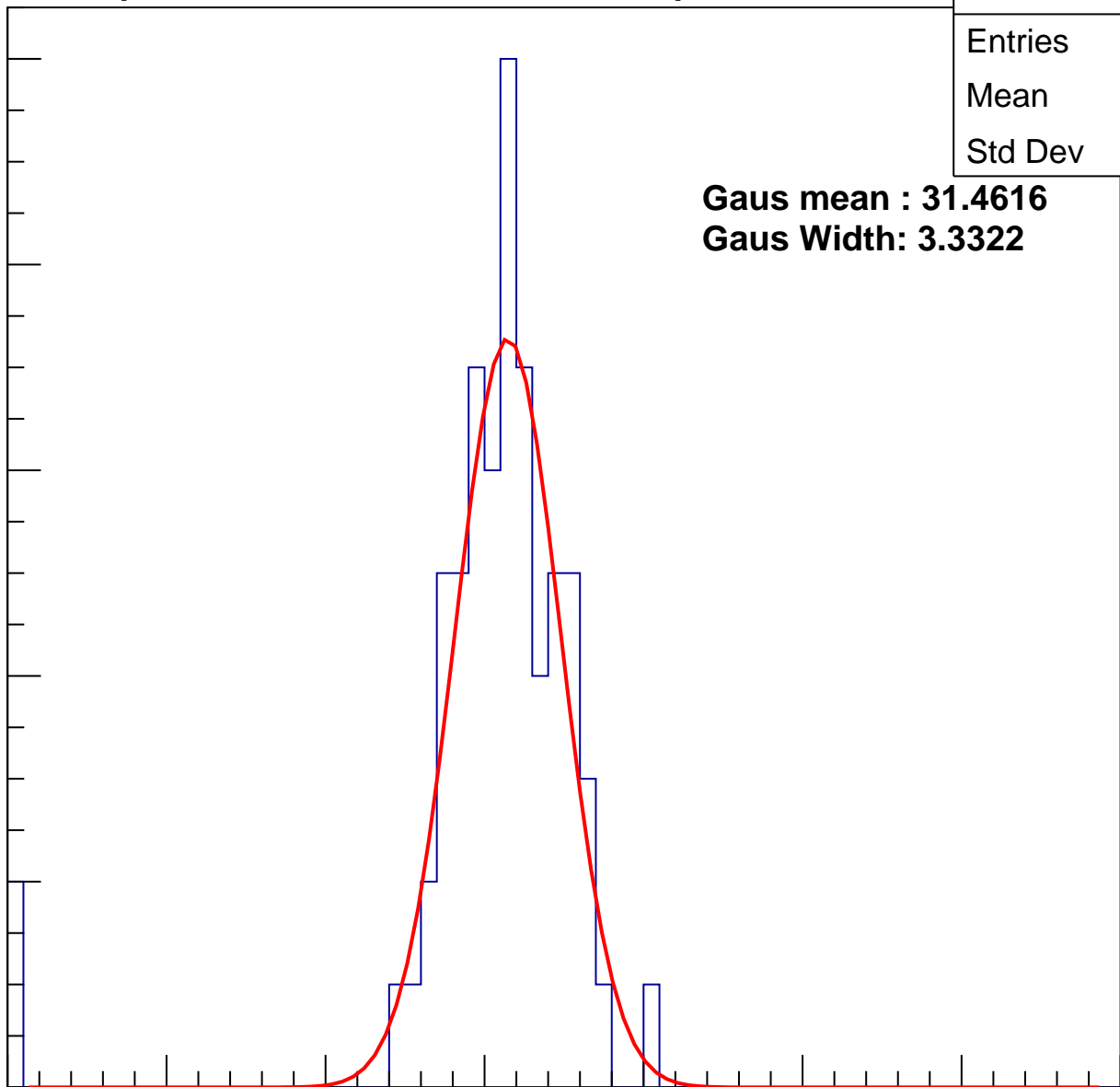
**Gaus Width: 3.3322**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U17-ch51, adc1

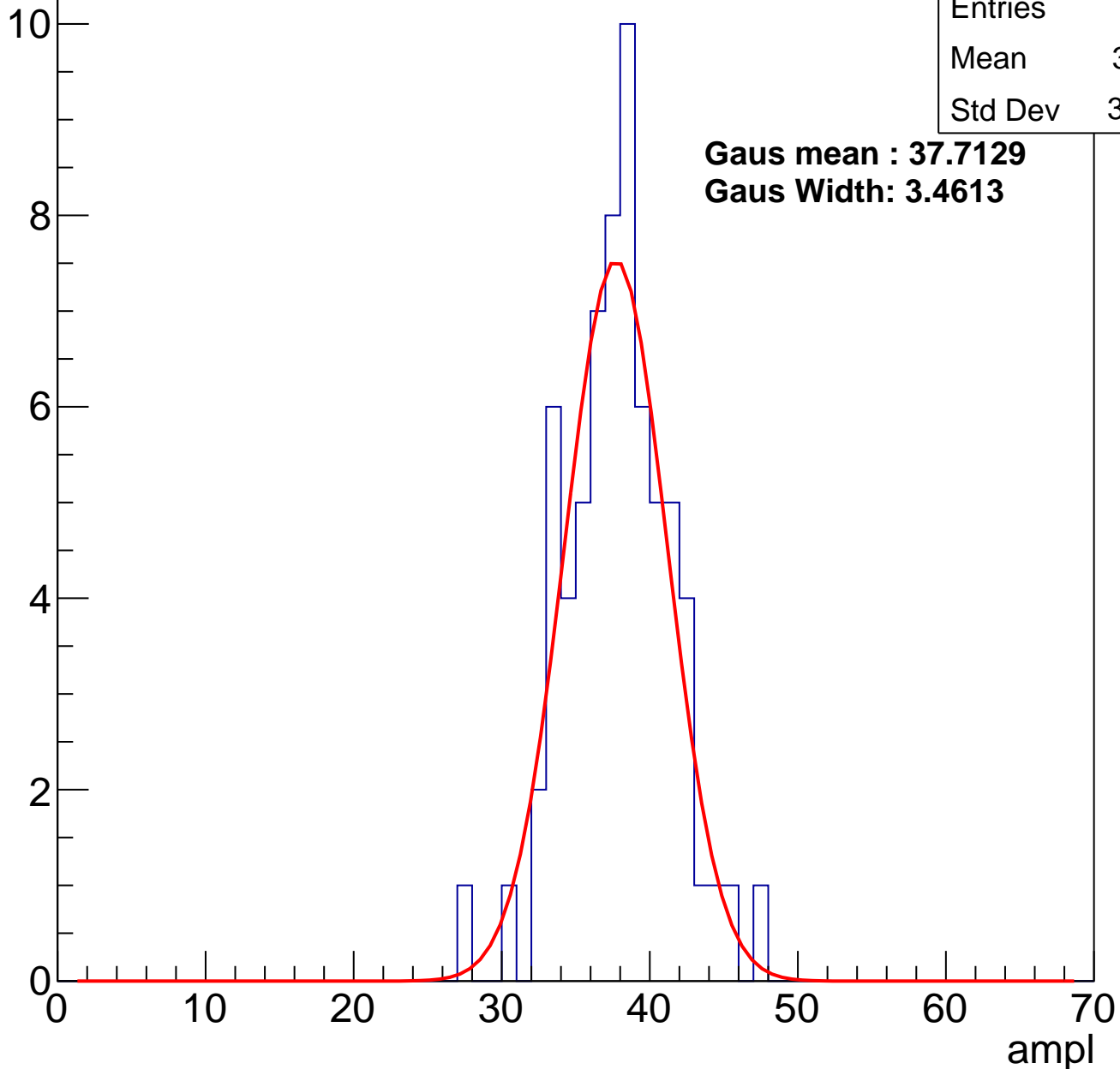
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	68
Mean	37.41
Std Dev	3.545

**Gaus mean : 37.7129**

**Gaus Width: 3.4613**

Entry



# B0L001S, U17-ch51, adc2

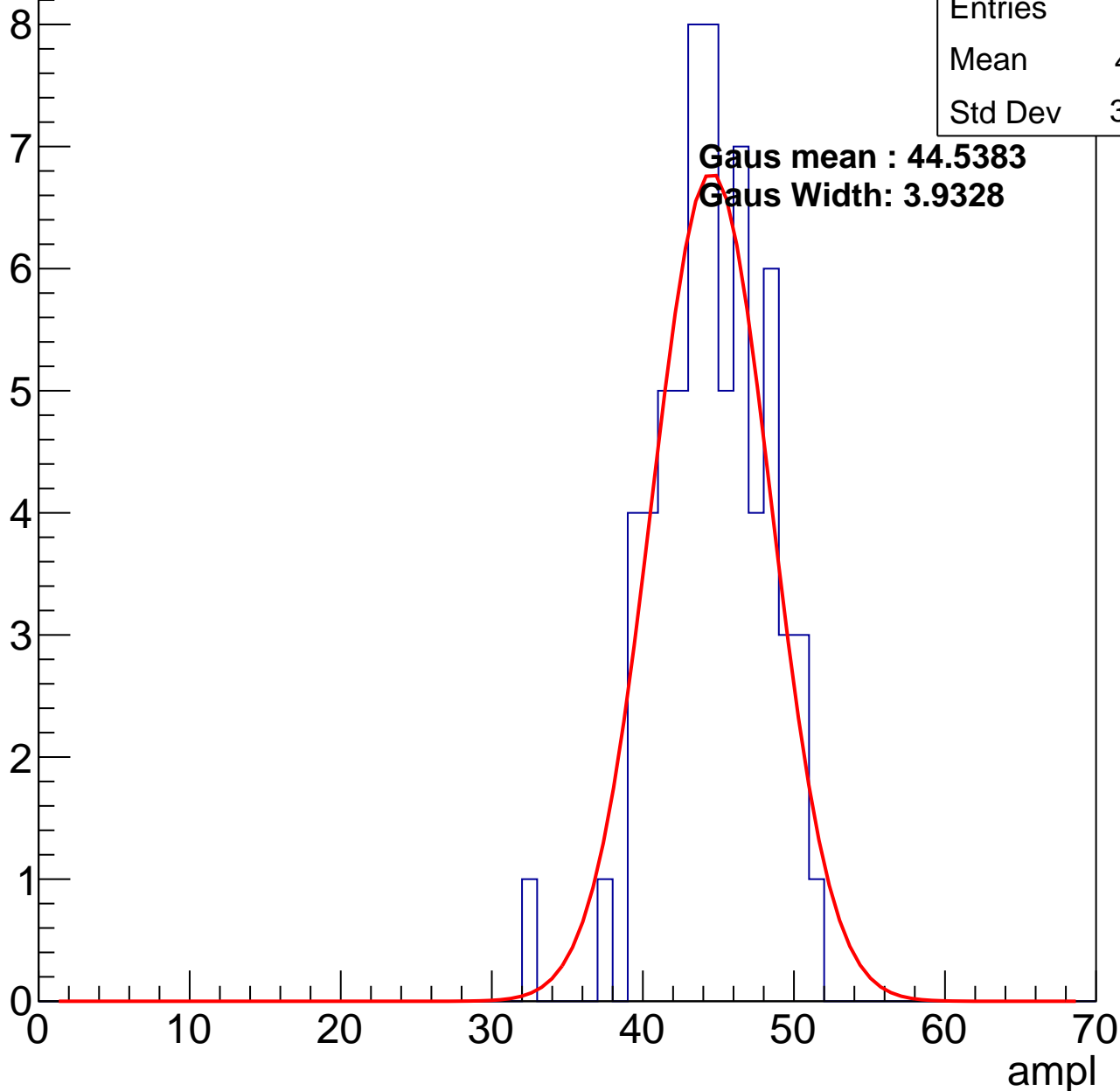
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	44.11
Std Dev	3.565

**Gaus mean : 44.5383**

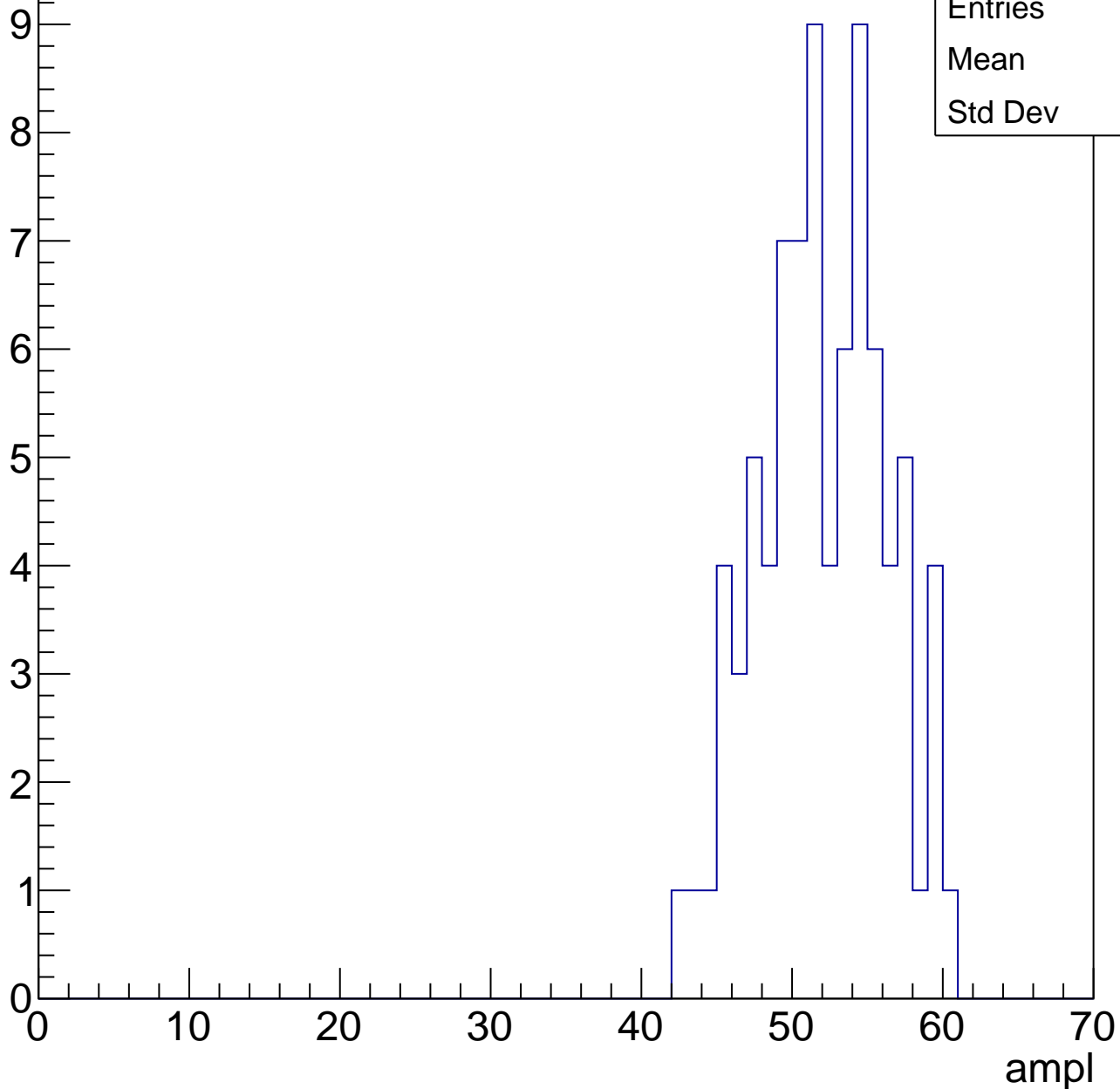
**Gaus Width: 3.9328**



# B0L001S, U17-ch51, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



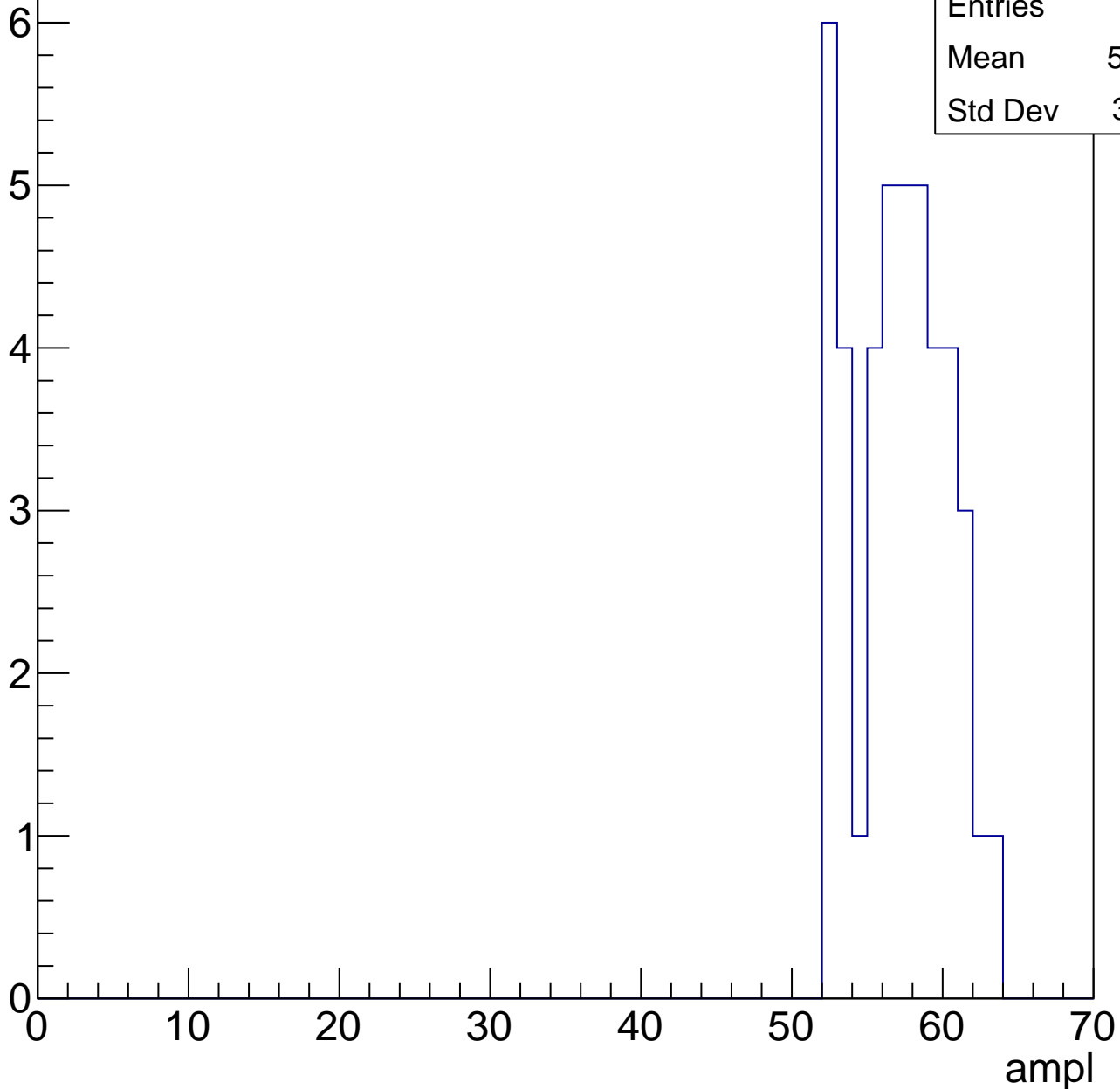
Entries	82
Mean	51.6
Std Dev	4.14

# B0L001S, U17-ch51, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	43
Mean	56.67
Std Dev	3.071

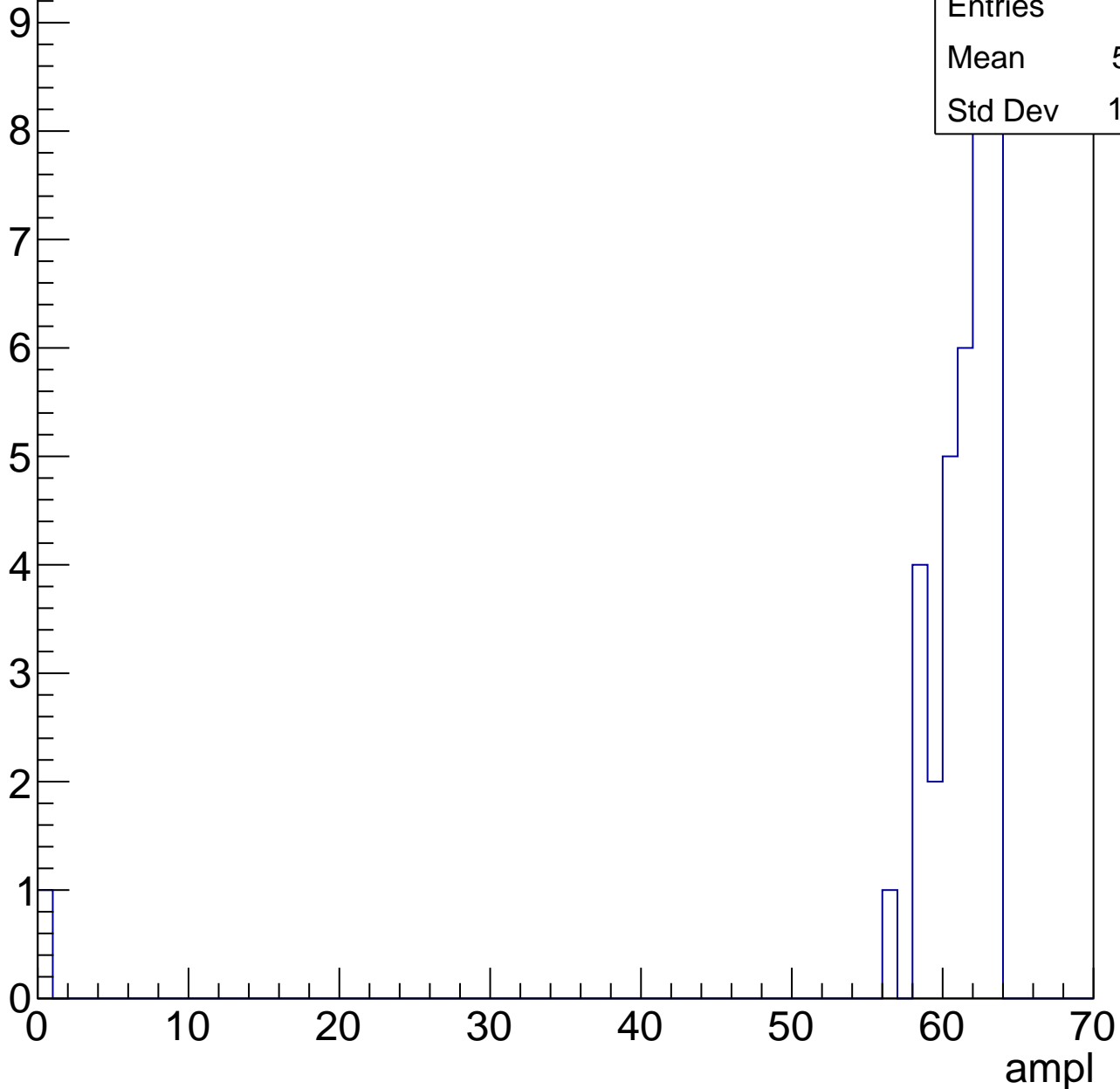


# B0L001S, U17-ch51, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	36
Mean	59.31
Std Dev	10.19



# B0L001S, U17-ch51, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

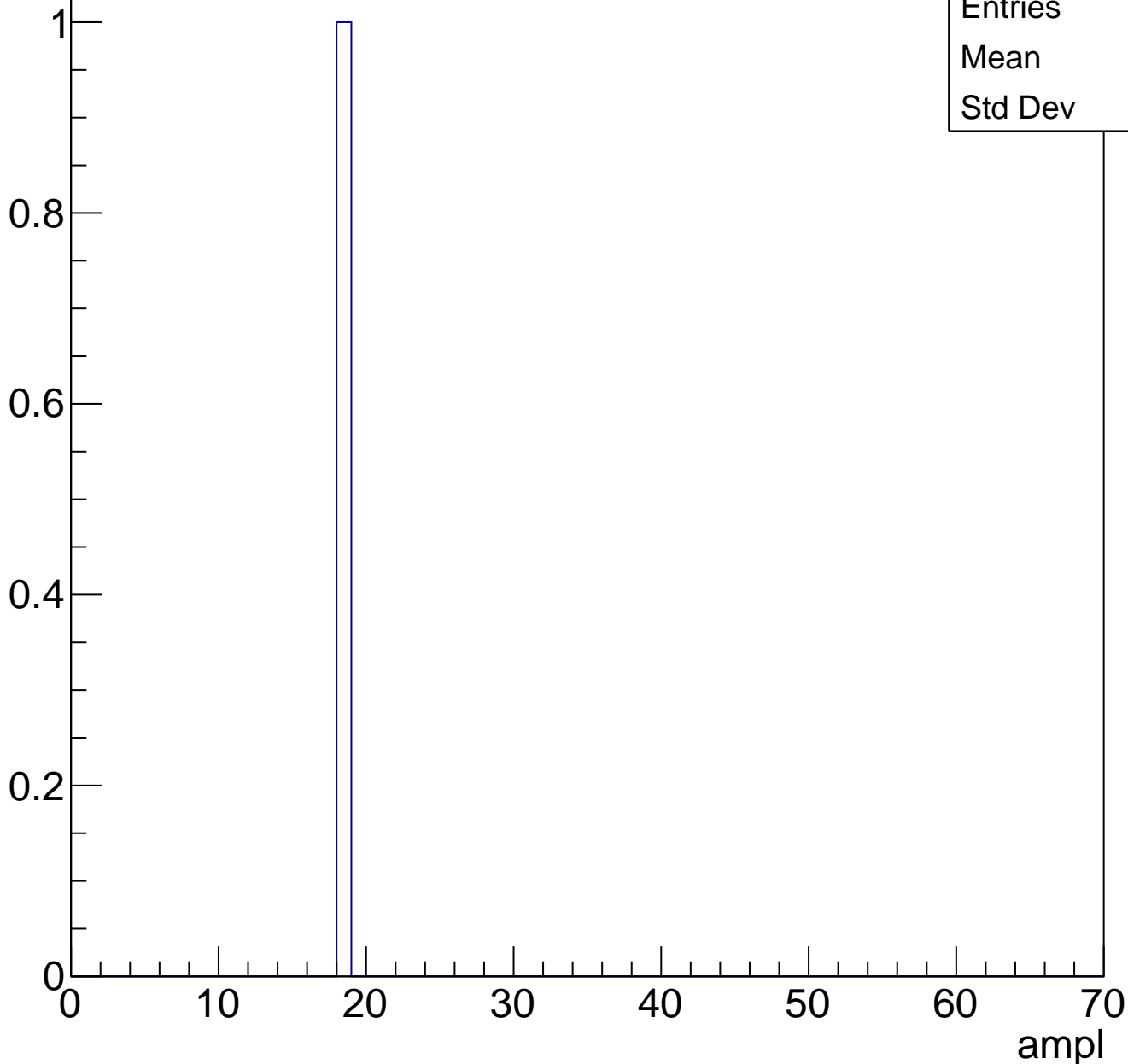




# B0L001S, U17-ch51, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U17-ch52, adc0

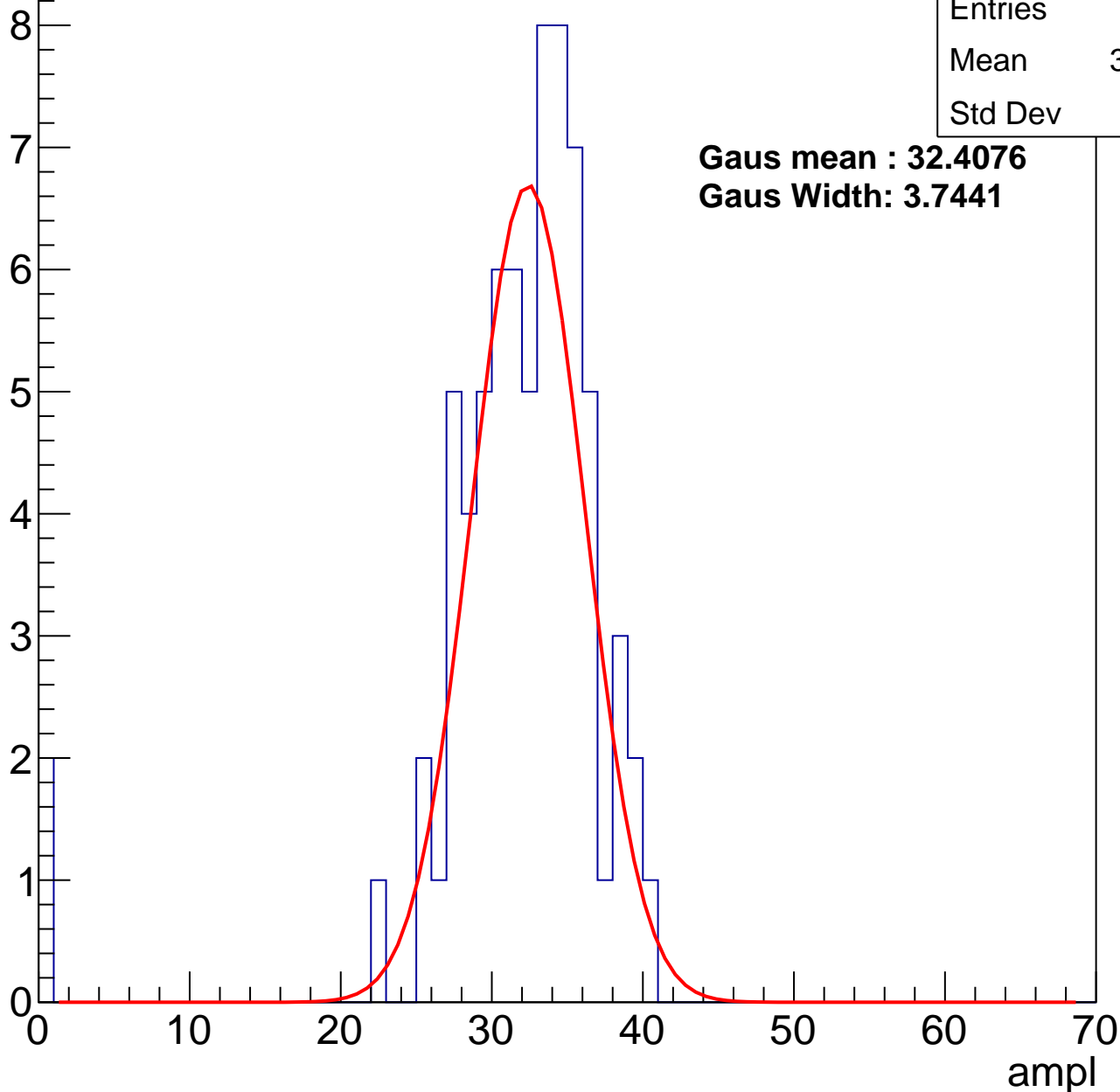
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	31.19
Std Dev	6.43

**Gaus mean : 32.4076**

**Gaus Width: 3.7441**



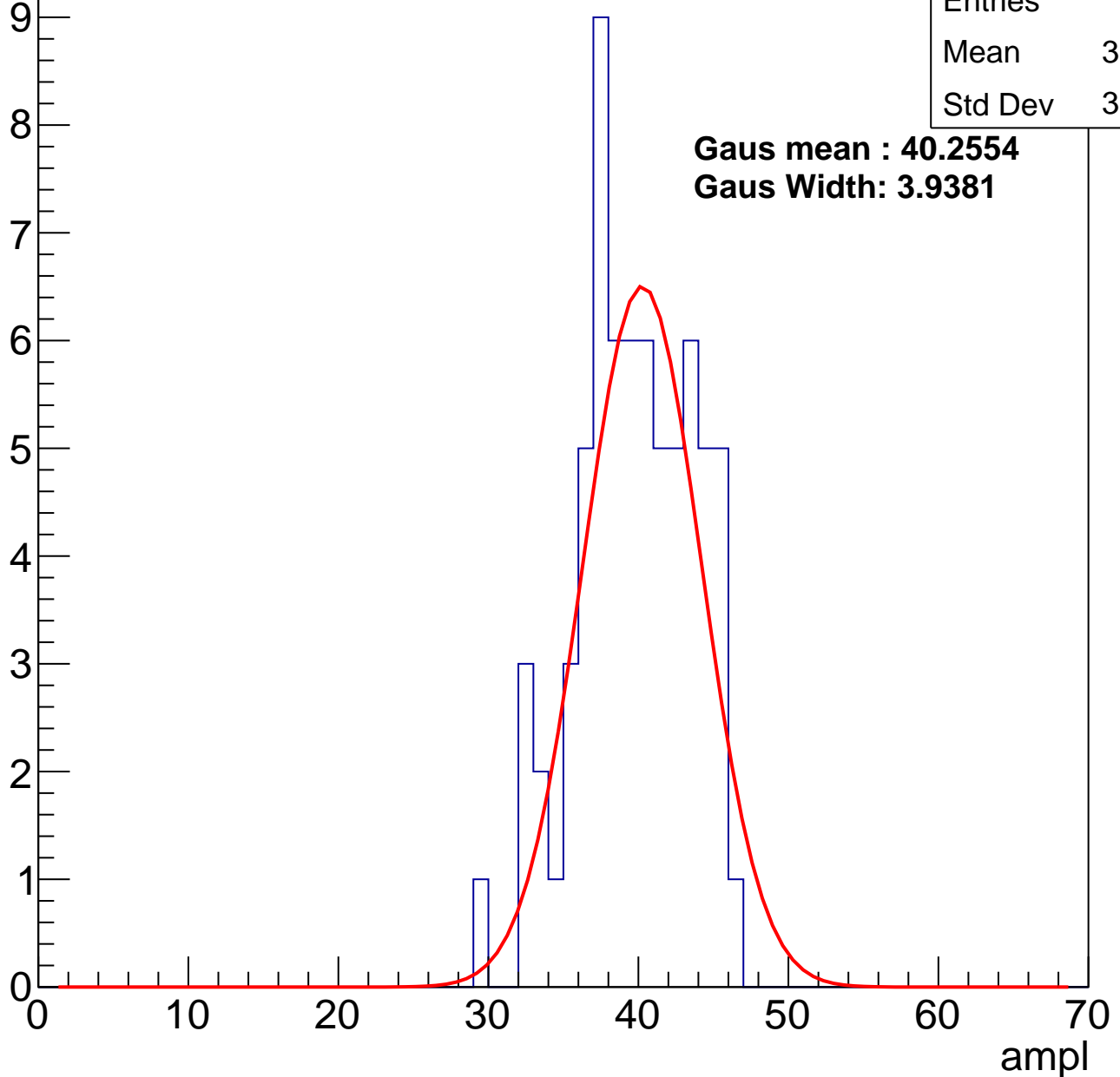
# B0L001S, U17-ch52, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	39.26
Std Dev	3.798

**Gaus mean : 40.2554**  
**Gaus Width: 3.9381**



# B0L001S, U17-ch52, adc2

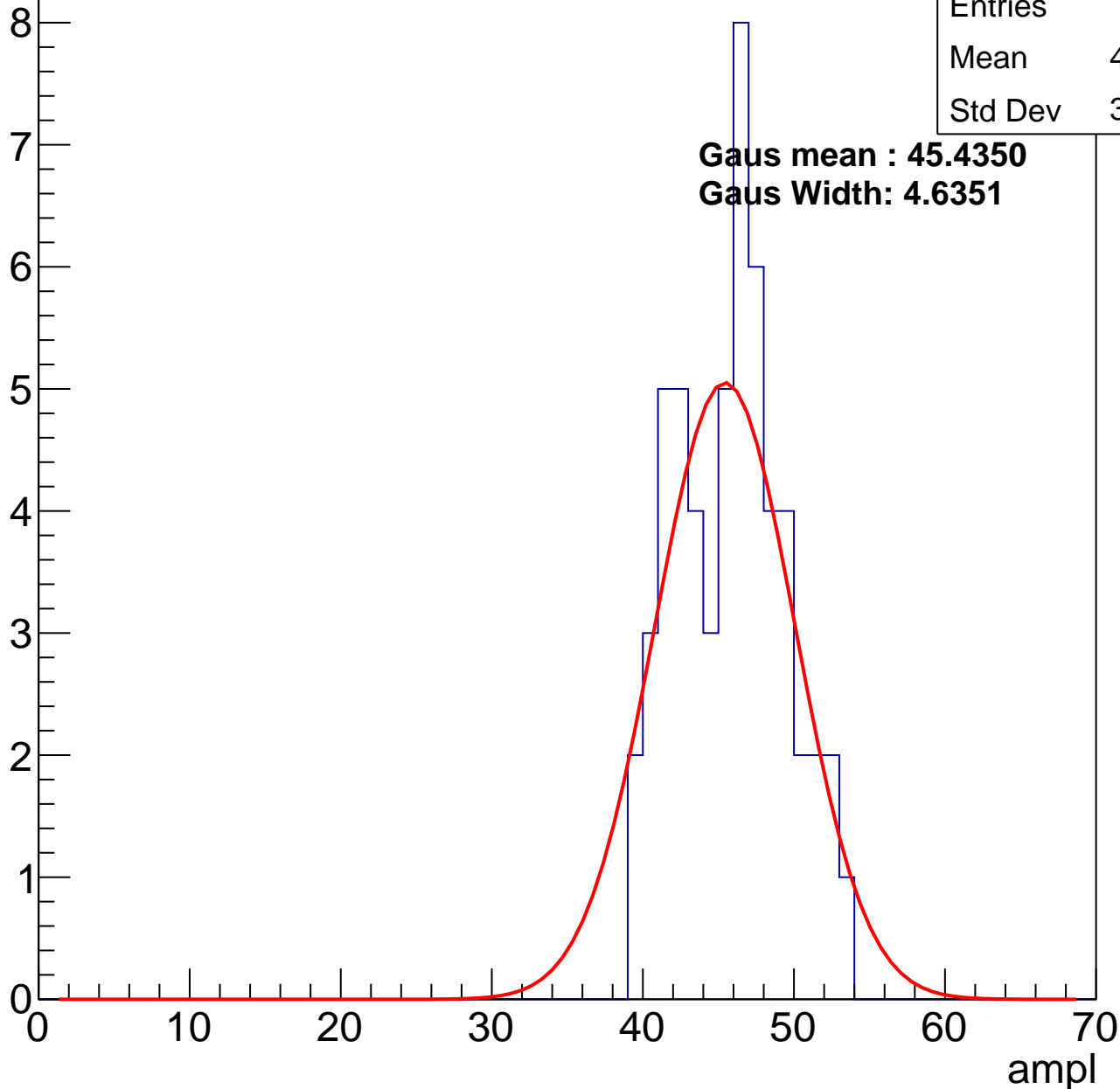
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	45.34
Std Dev	3.537

**Gaus mean : 45.4350**

**Gaus Width: 4.6351**

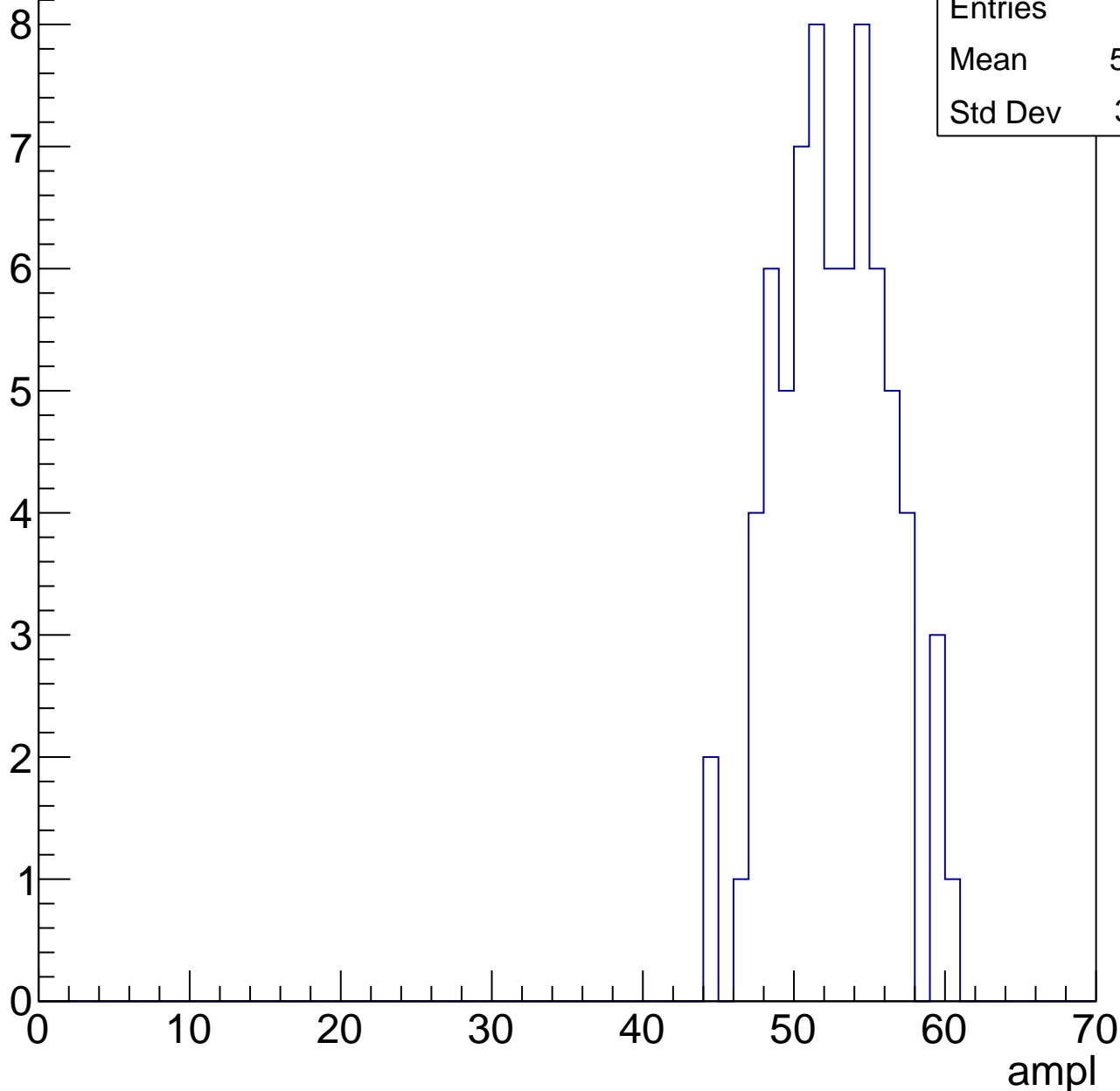


# B0L001S, U17-ch52, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	52.08
Std Dev	3.581

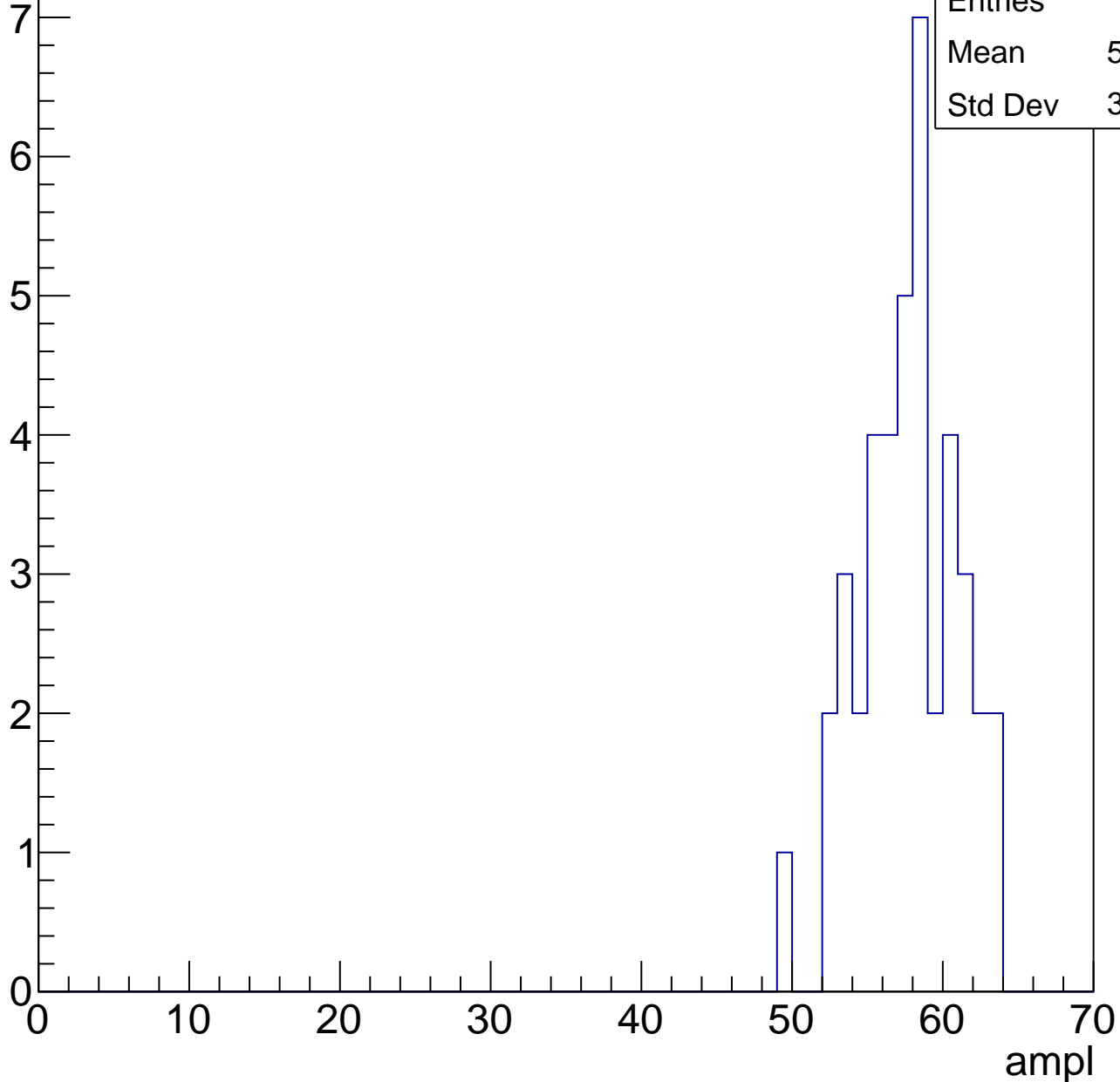


# B0L001S, U17-ch52, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	41
Mean	57.22
Std Dev	3.197

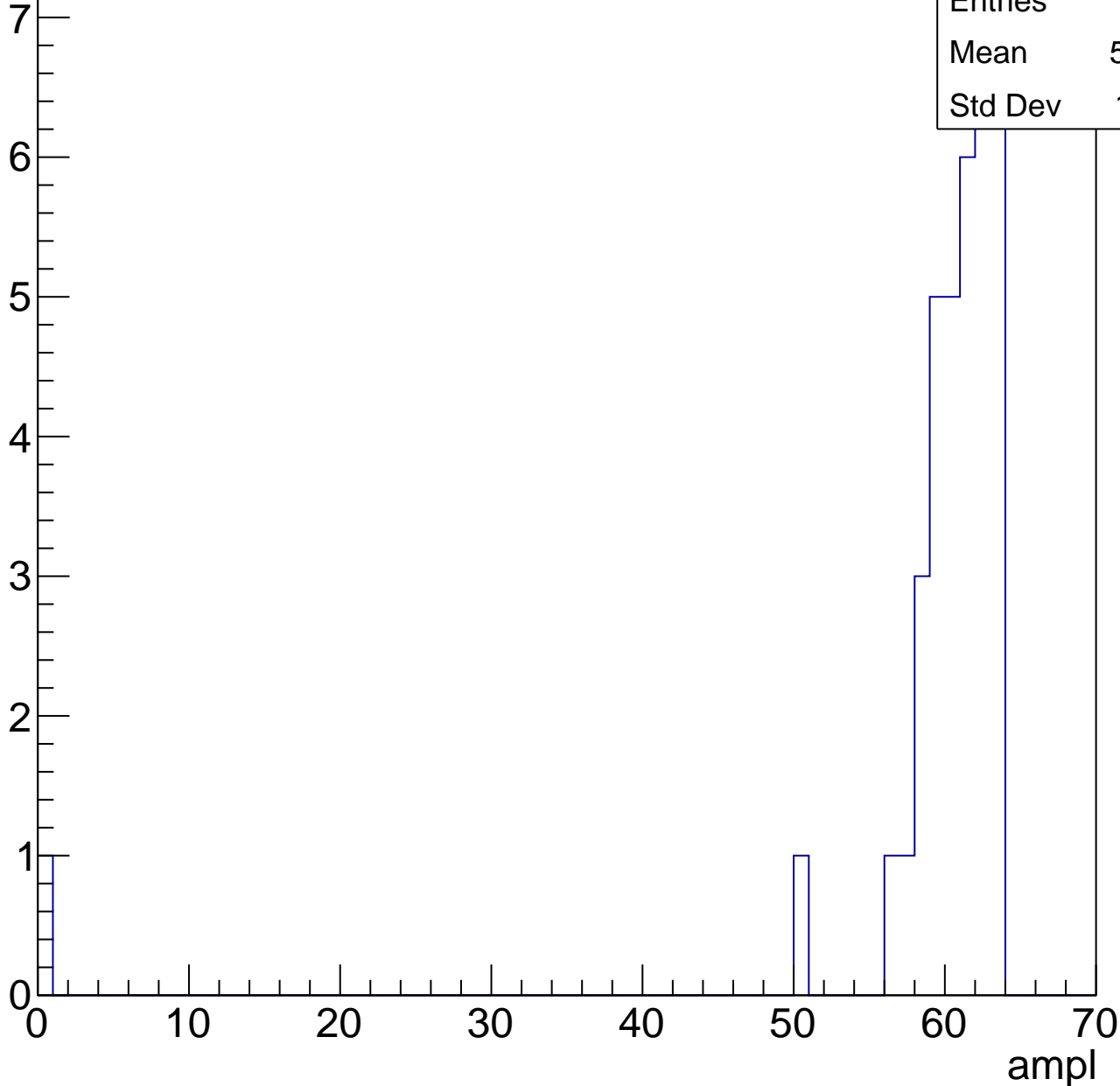


# B0L001S, U17-ch52, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	37
Mean	58.73
Std Dev	10.11



# B0L001S, U17-ch52, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch52, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U17-ch53, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	77
Mean	31.86
Std Dev	5.016

**Gaus mean : 32.9068**

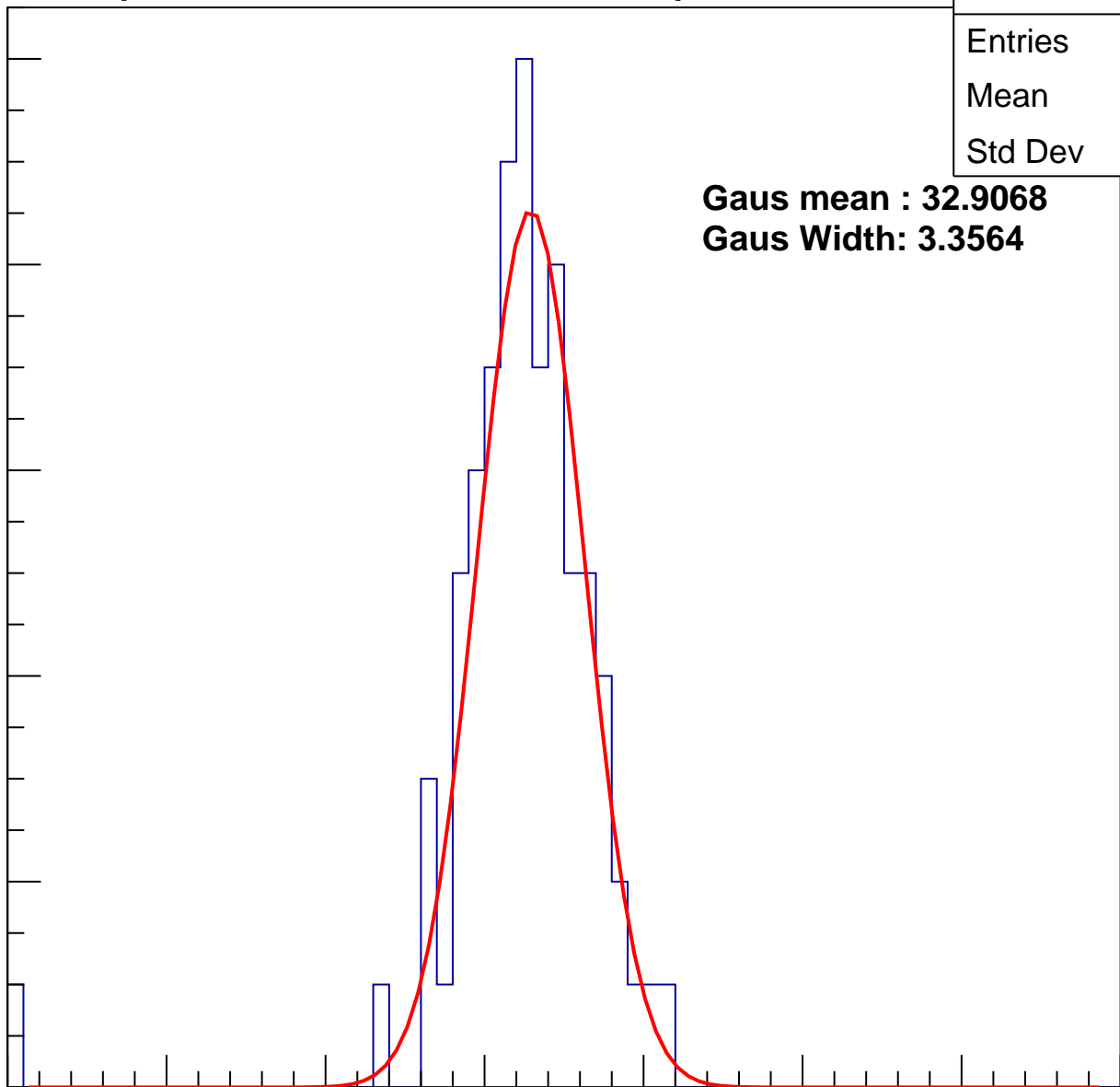
**Gaus Width: 3.3564**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U17-ch53, adc1

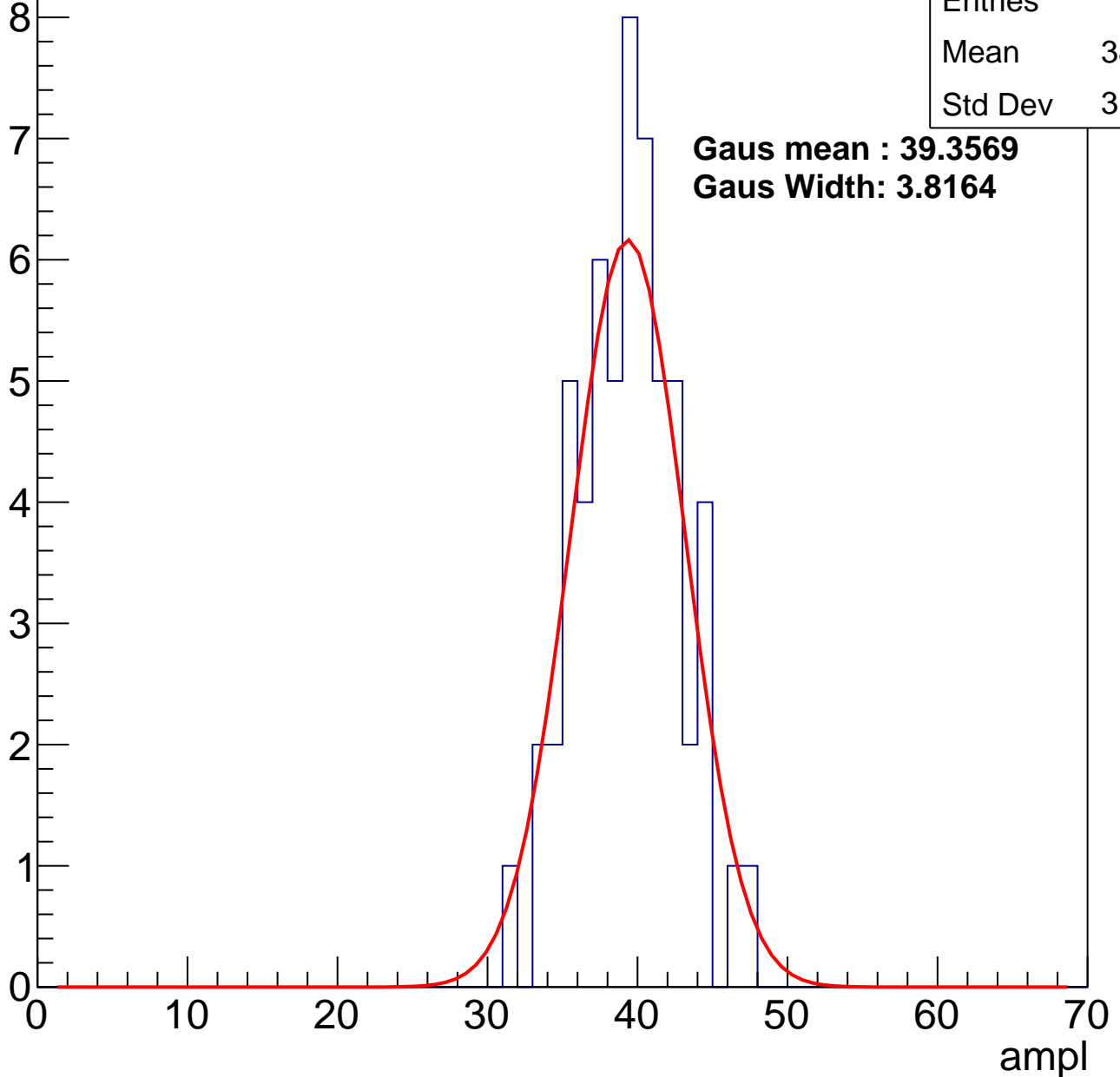
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	38.93
Std Dev	3.342

**Gaus mean : 39.3569**

**Gaus Width: 3.8164**



# B0L001S, U17-ch53, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	77
Mean	45.35
Std Dev	3.329

**Gaus mean : 46.1756**

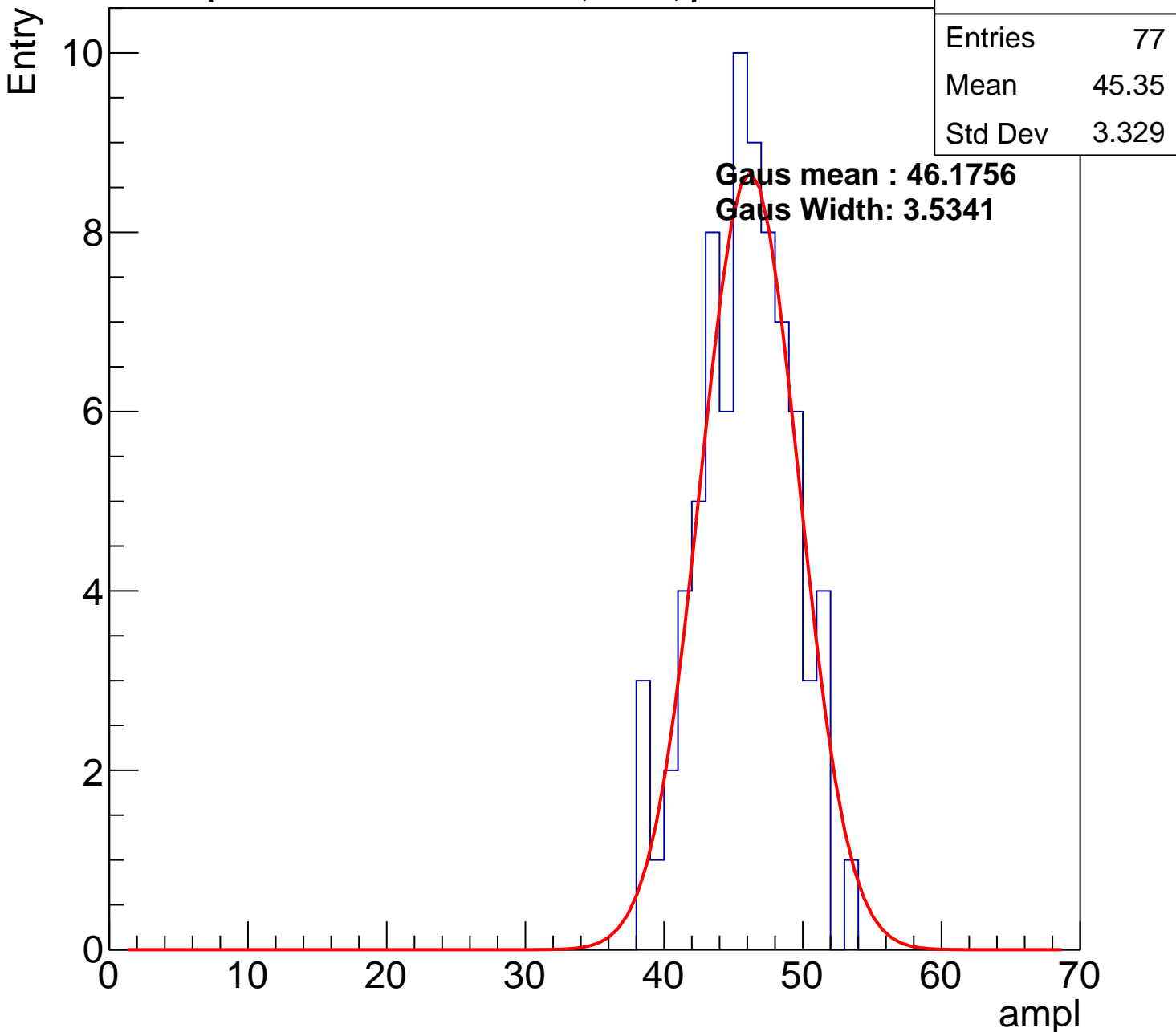
**Gaus Width: 3.5341**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

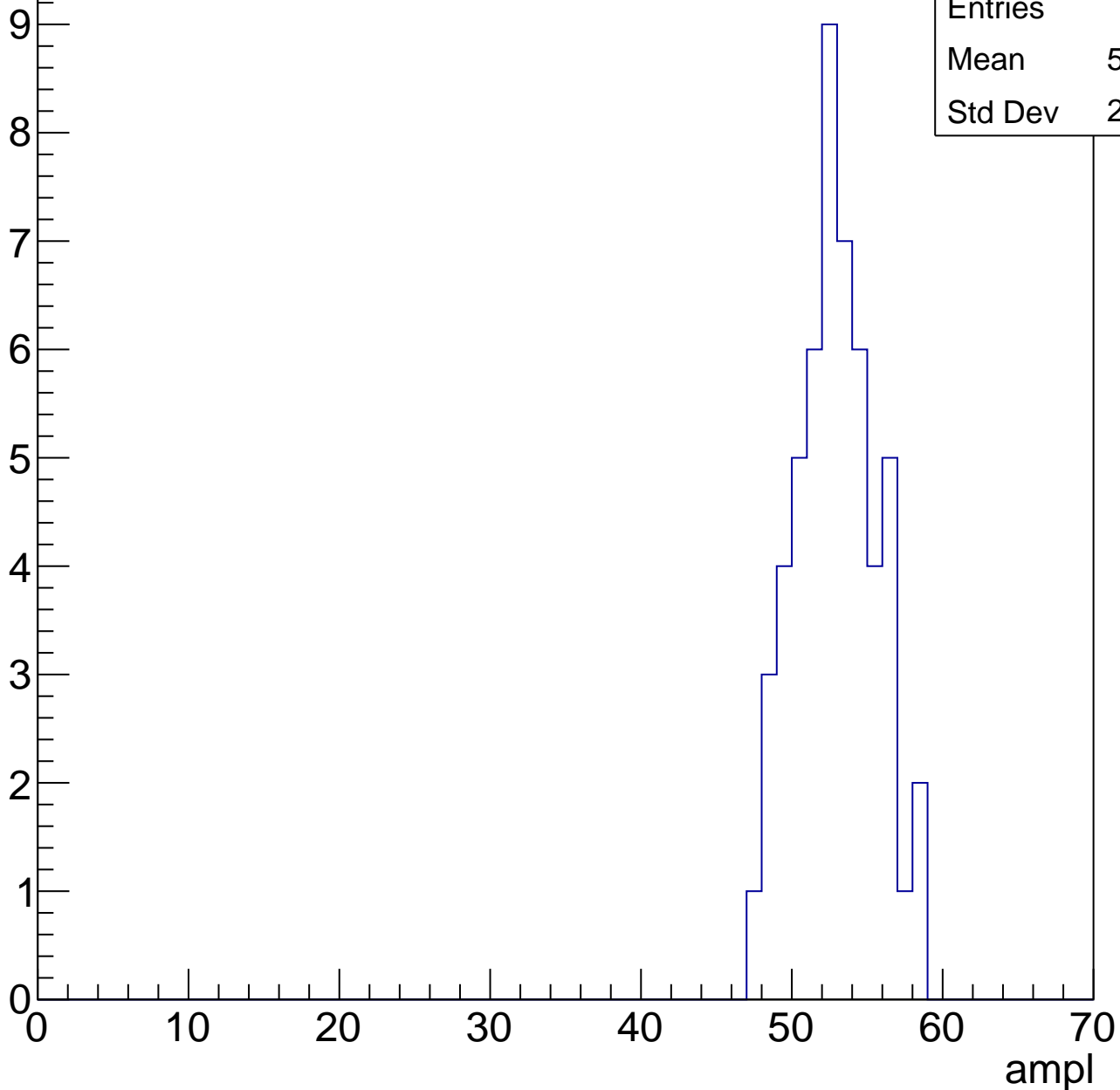


# B0L001S, U17-ch53, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

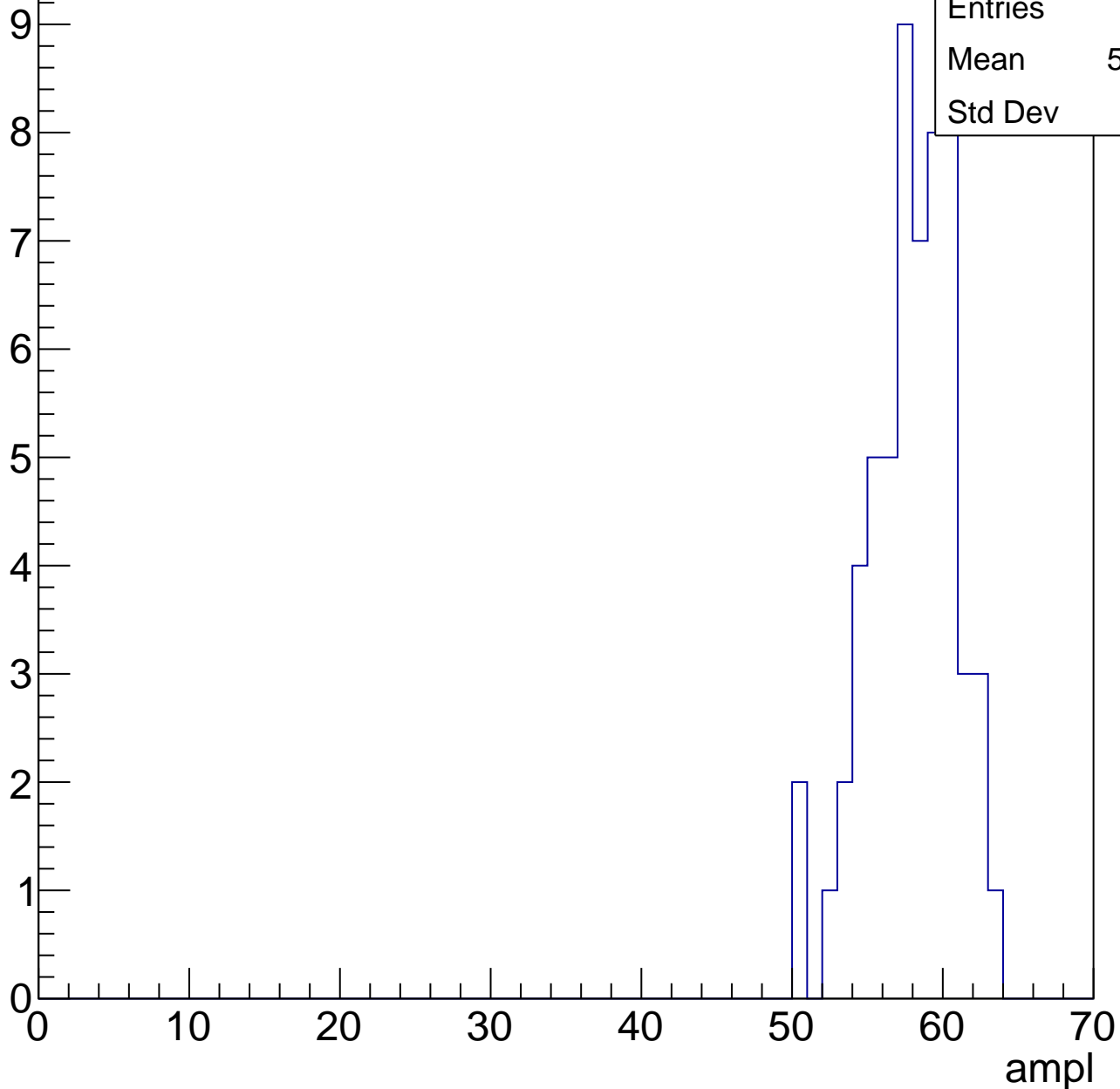
Entries	53
Mean	52.43
Std Dev	2.639



# B0L001S, U17-ch53, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



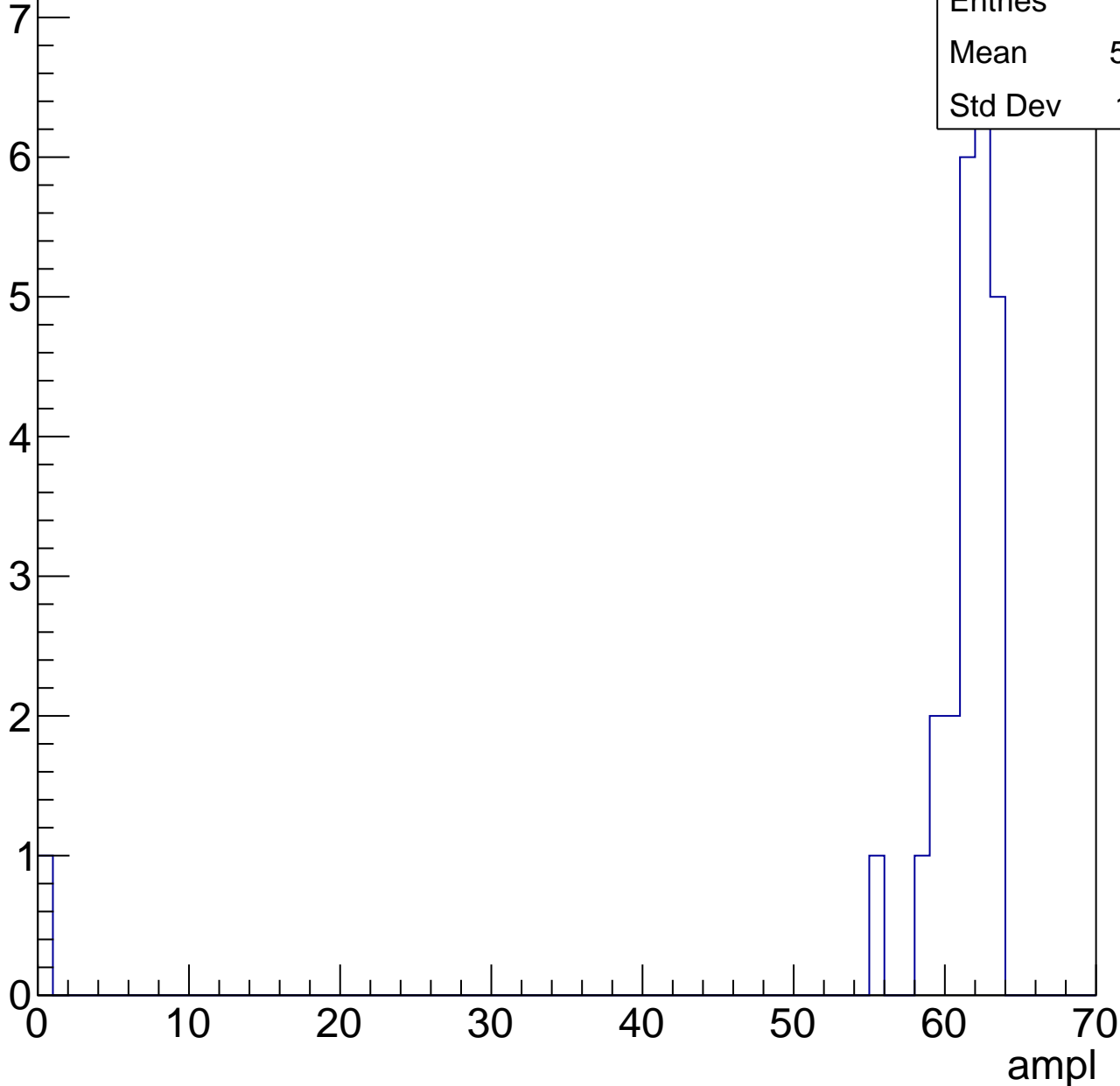
Entries	58
Mean	57.45
Std Dev	2.86

# B0L001S, U17-ch53, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

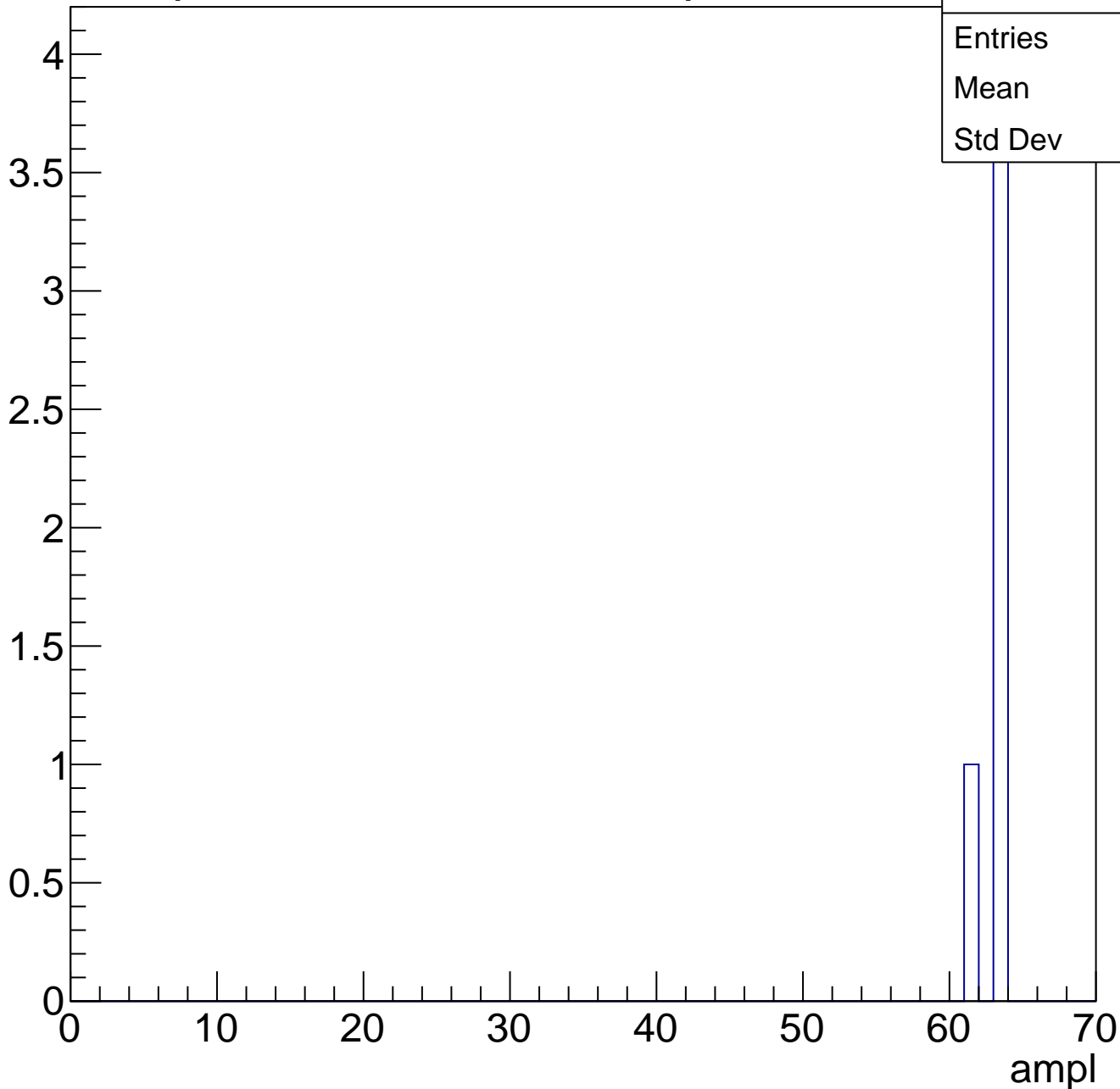
Entries	25
Mean	58.64
Std Dev	12.11



# B0L001S, U17-ch53, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch53, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	10
Std Dev	10

# B0L001S, U17-ch54, adc0

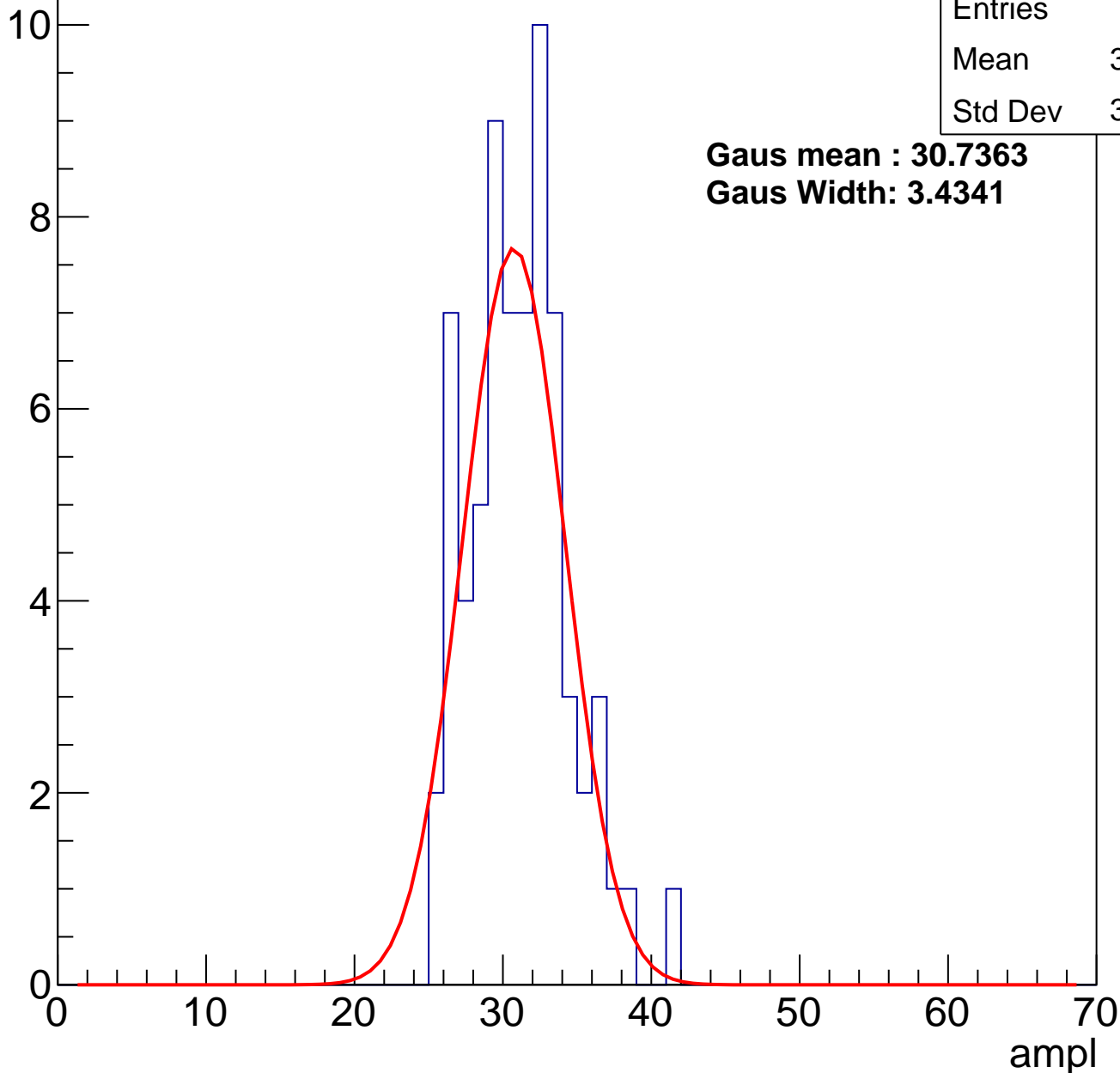
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	69
Mean	30.65
Std Dev	3.292

**Gaus mean : 30.7363**

**Gaus Width: 3.4341**

Entry



# B0L001S, U17-ch54, adc1

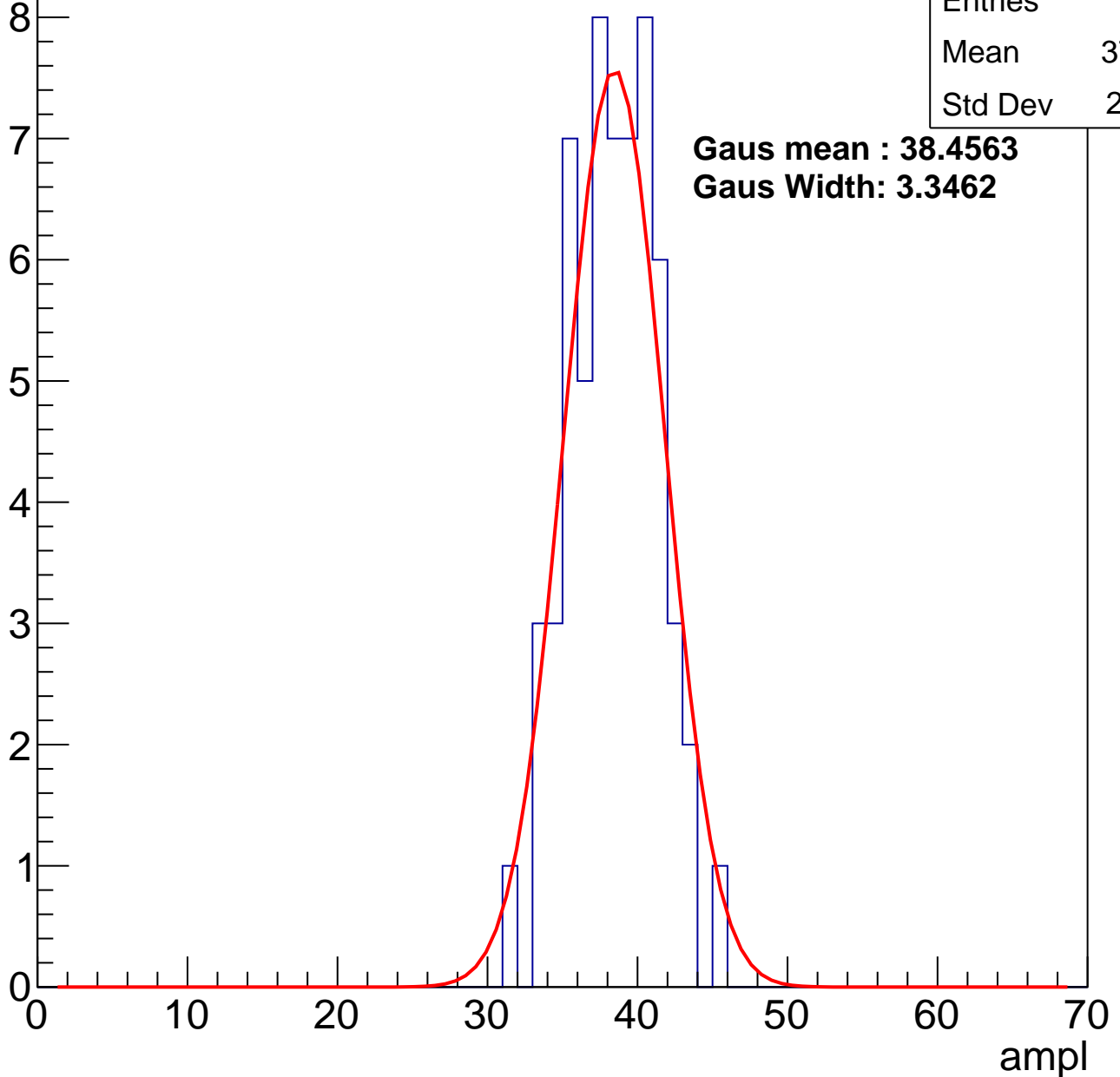
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	37.95
Std Dev	2.871

**Gaus mean : 38.4563**

**Gaus Width: 3.3462**



# B0L001S, U17-ch54, adc2

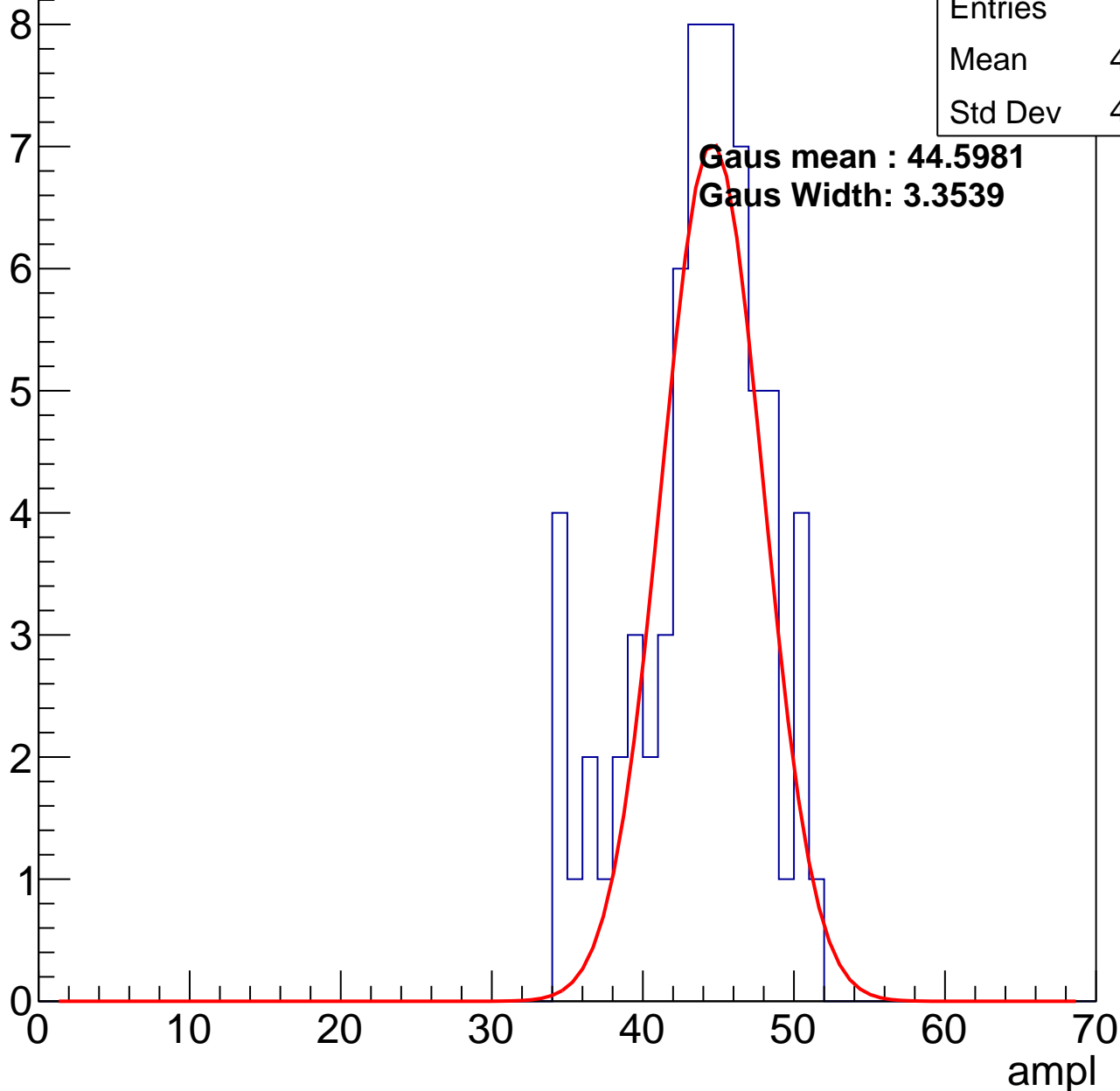
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	43.39
Std Dev	4.194

**Gaus mean : 44.5981**

**Gaus Width: 3.3539**

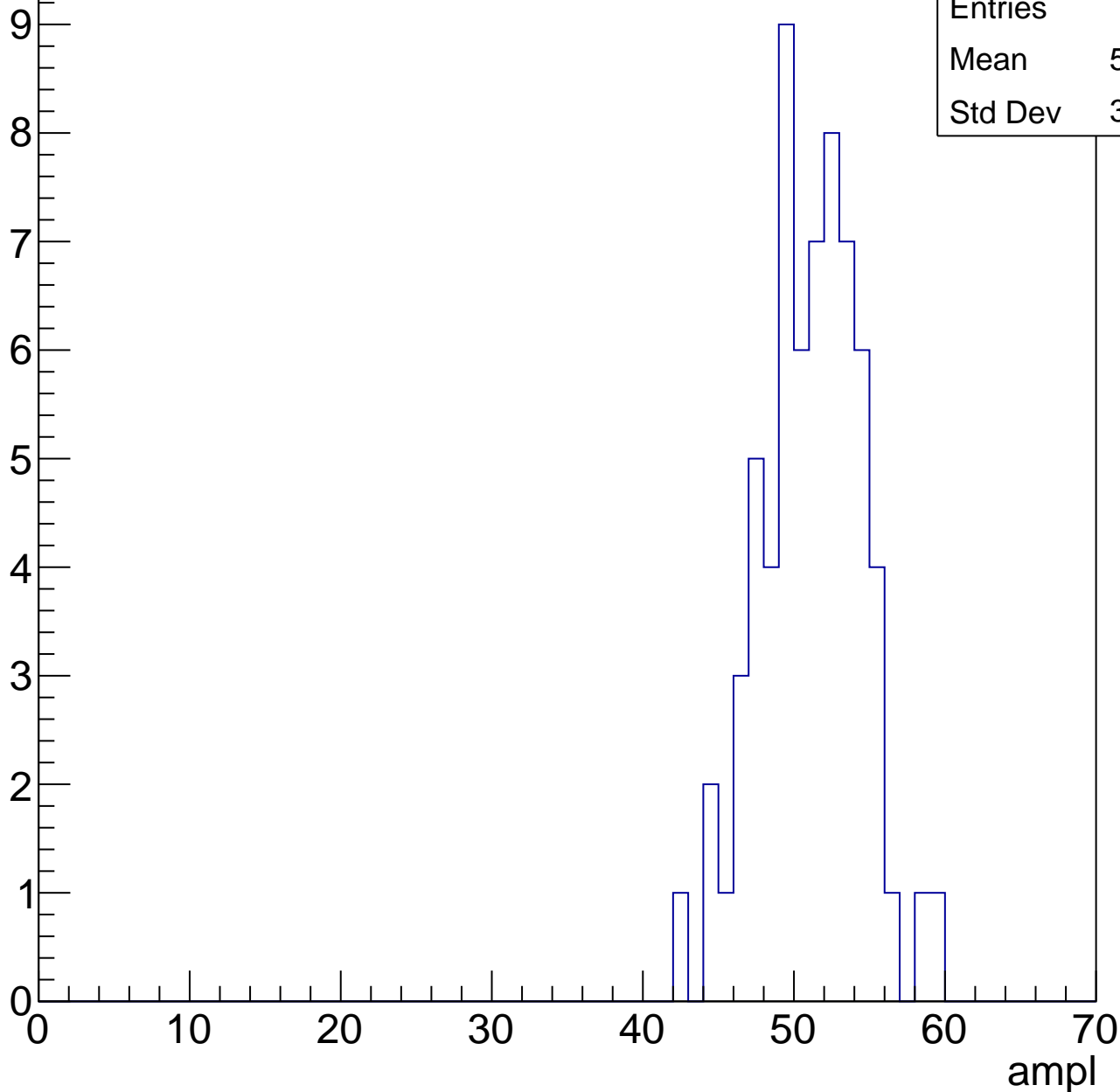


# B0L001S, U17-ch54, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	50.64
Std Dev	3.329

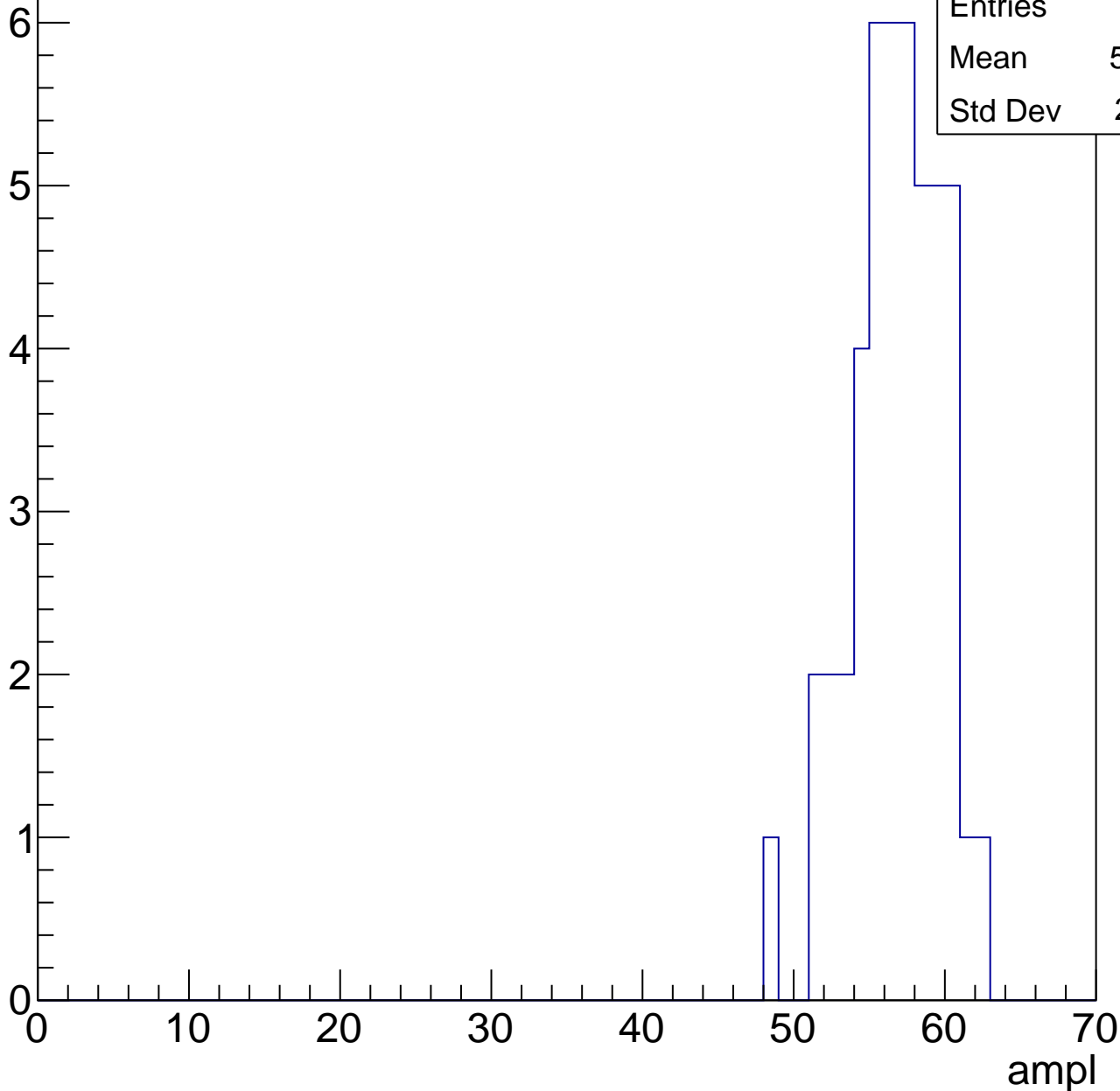


# B0L001S, U17-ch54, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	46
Mean	56.35
Std Dev	2.921

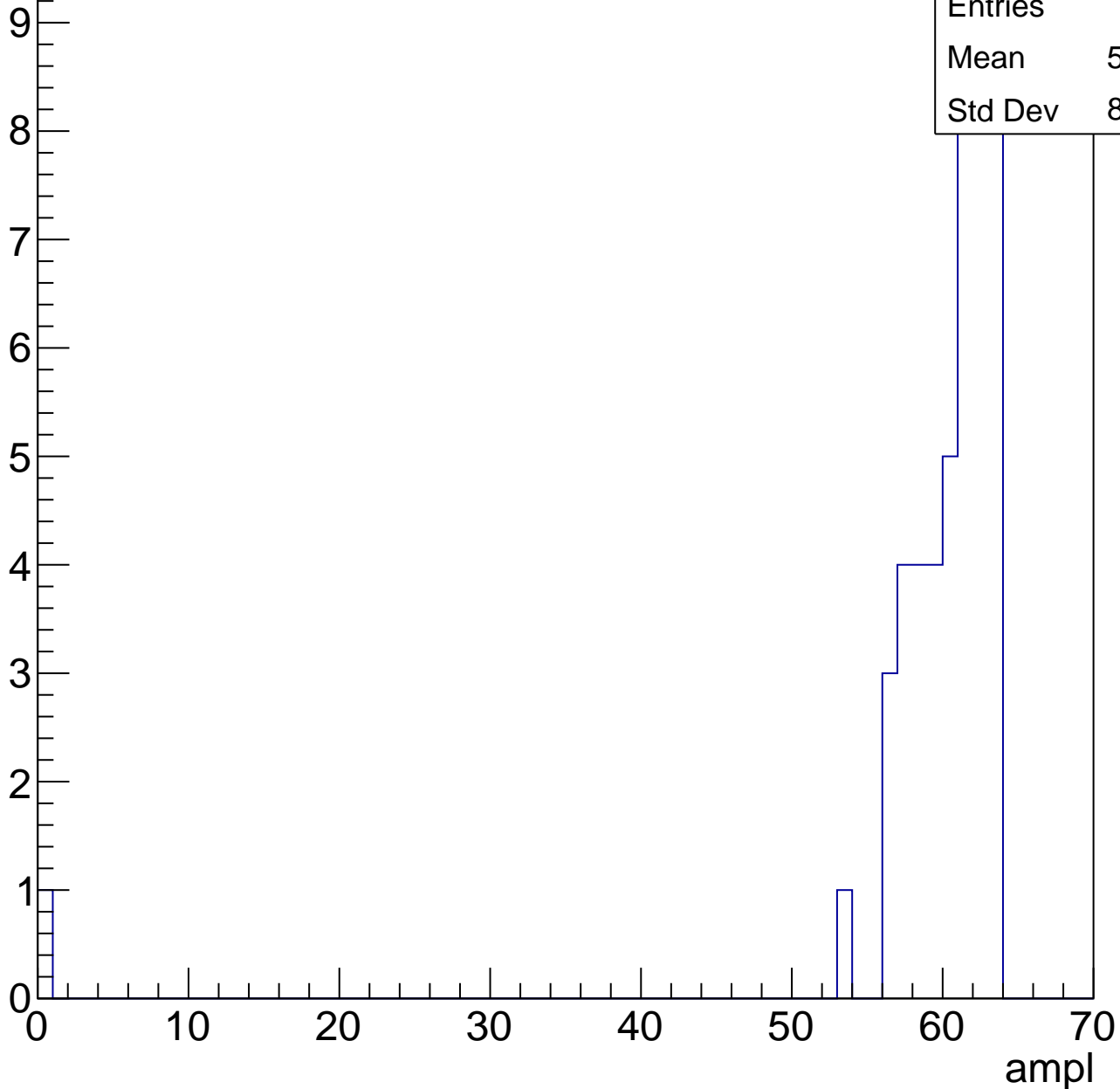


# B0L001S, U17-ch54, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	48
Mean	58.94
Std Dev	8.922



# B0L001S, U17-ch54, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch54, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U17-ch55, adc0

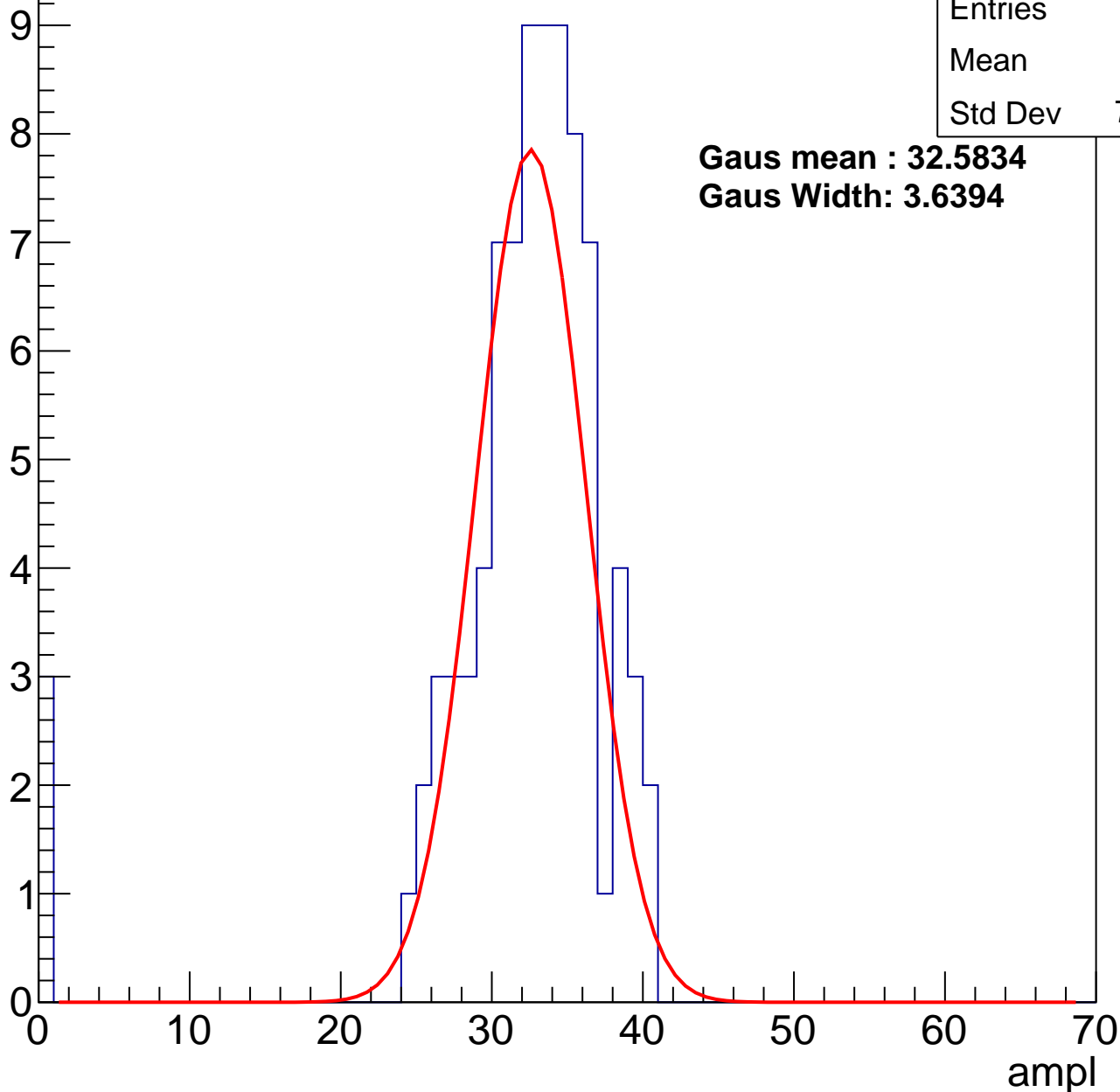
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	85
Mean	31.4
Std Dev	7.011

**Gaus mean : 32.5834**

**Gaus Width: 3.6394**



# B0L001S, U17-ch55, adc1

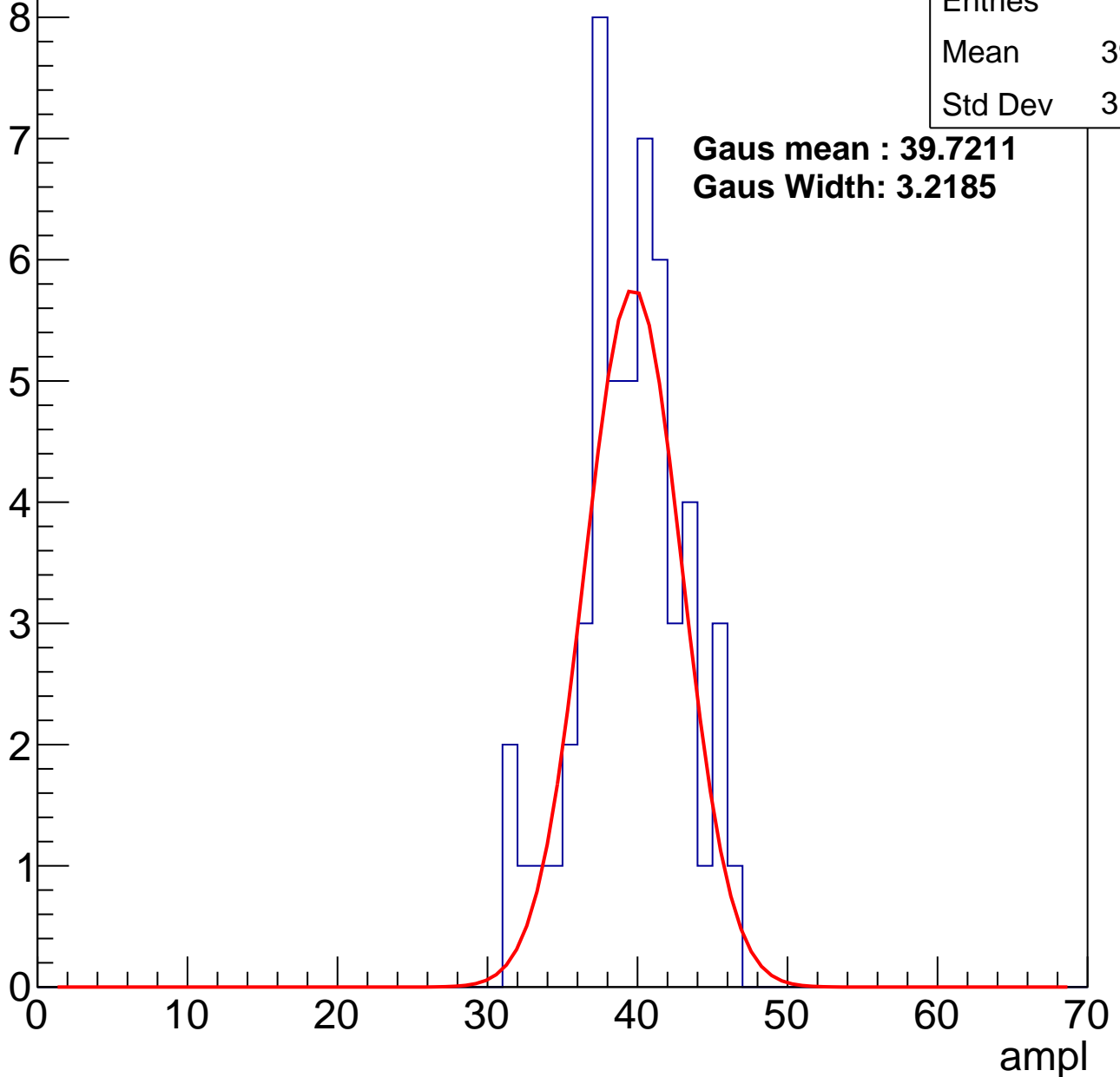
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	39.04
Std Dev	3.469

**Gaus mean : 39.7211**

**Gaus Width: 3.2185**



# B0L001S, U17-ch55, adc2

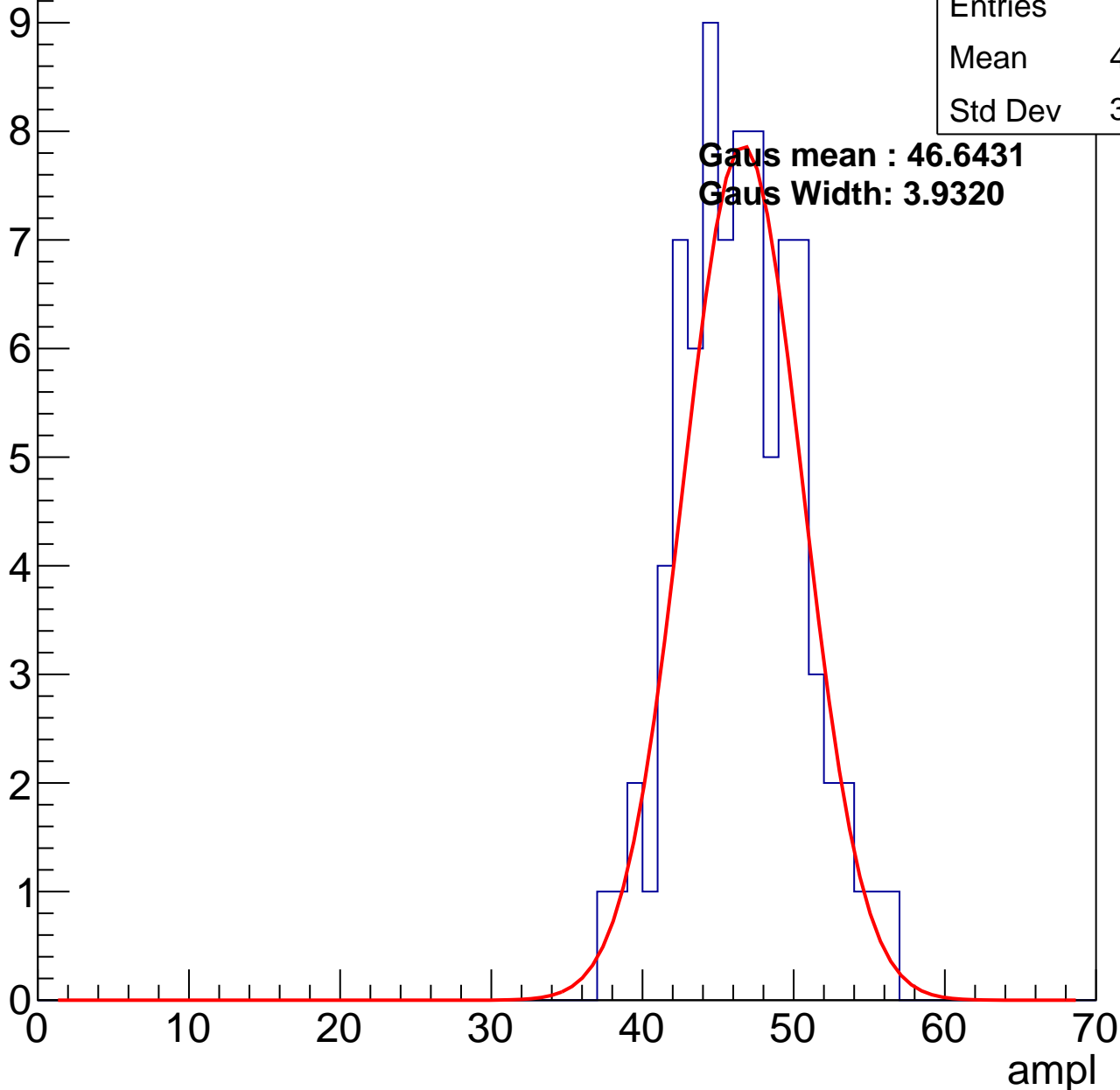
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	83
Mean	46.08
Std Dev	3.928

**Gaus mean : 46.6431**

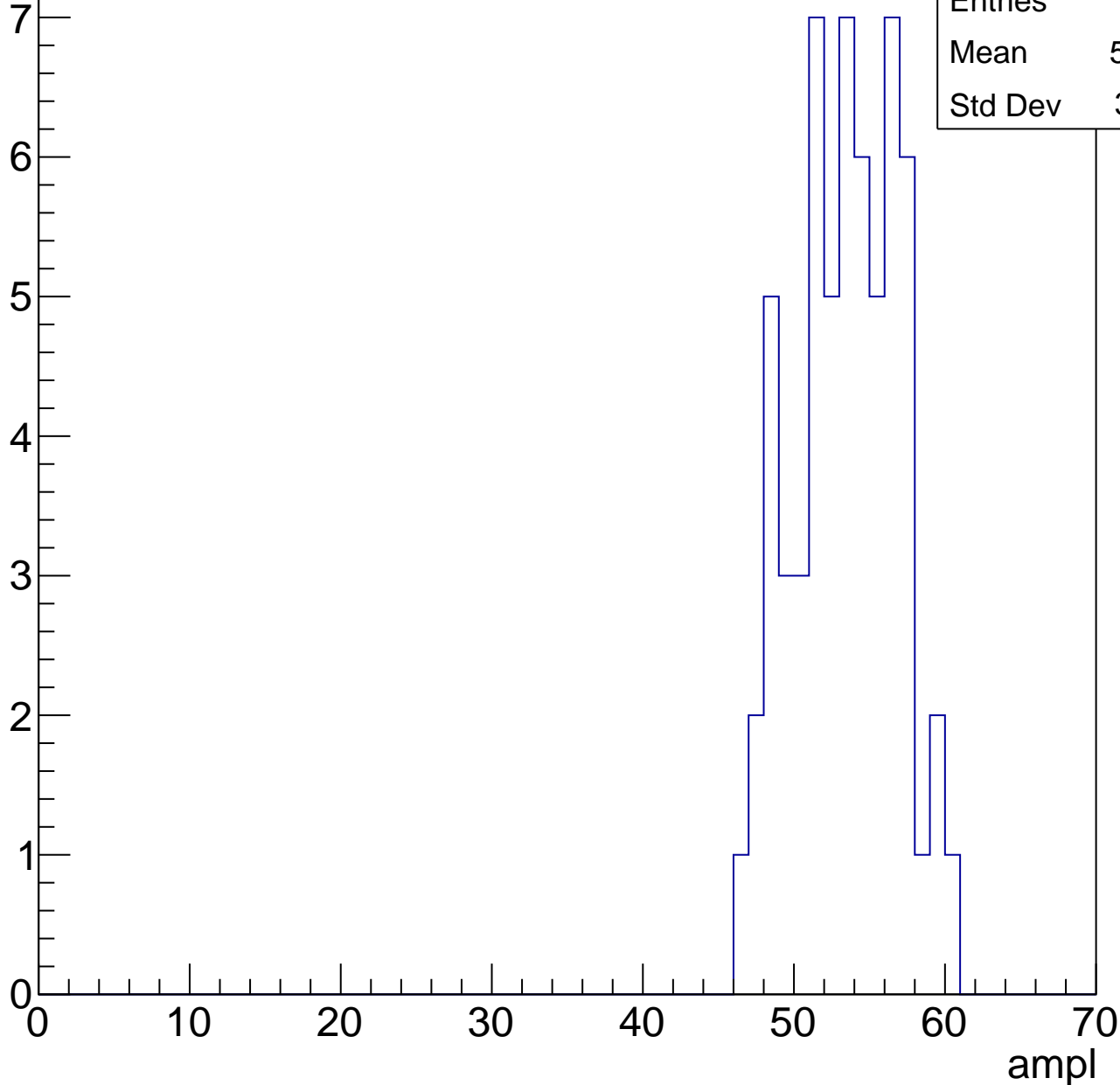
**Gaus Width: 3.9320**



# B0L001S, U17-ch55, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



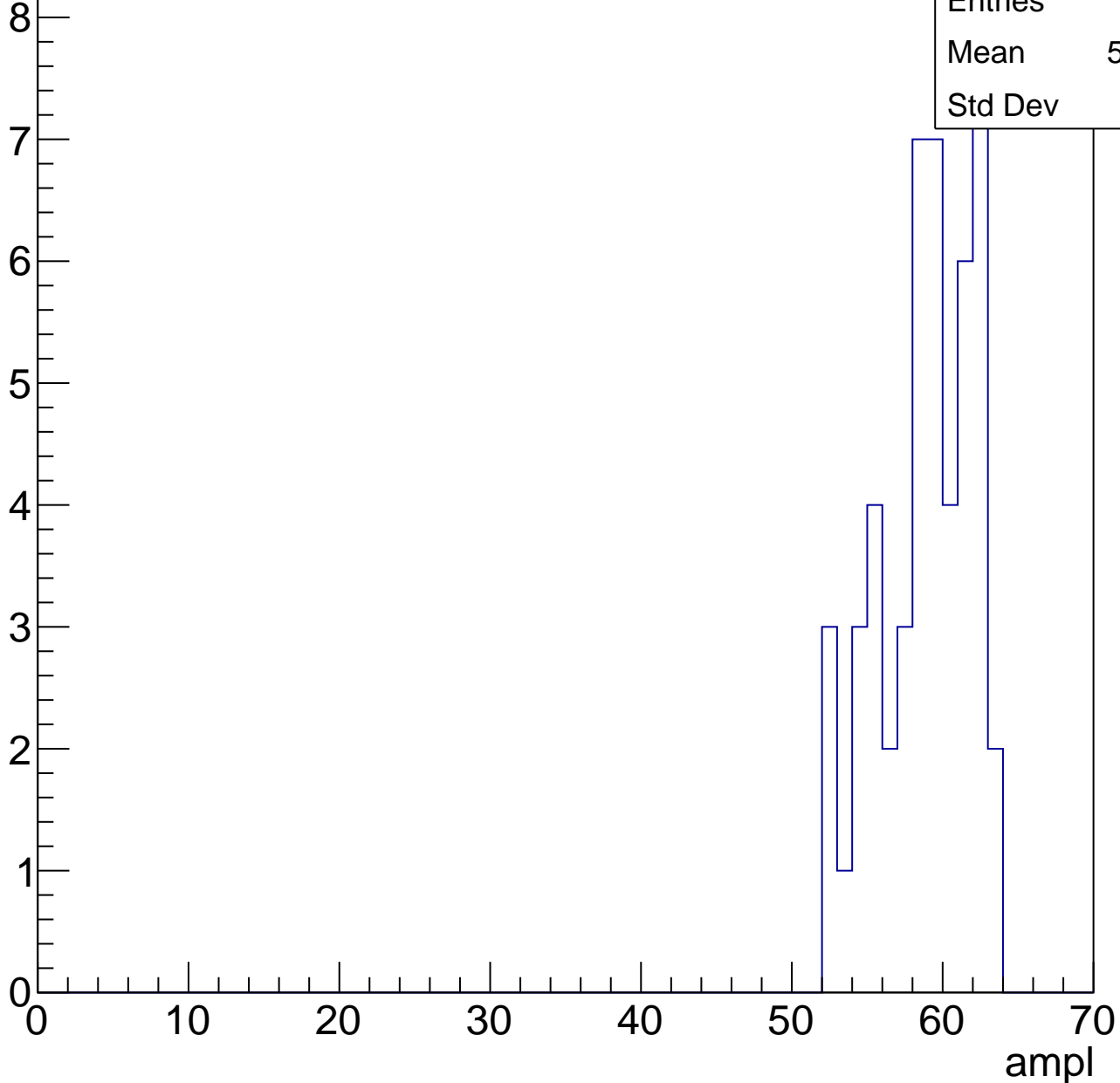
Entries	61
Mean	53.02
Std Dev	3.351

# B0L001S, U17-ch55, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	50
Mean	58.42
Std Dev	3.08

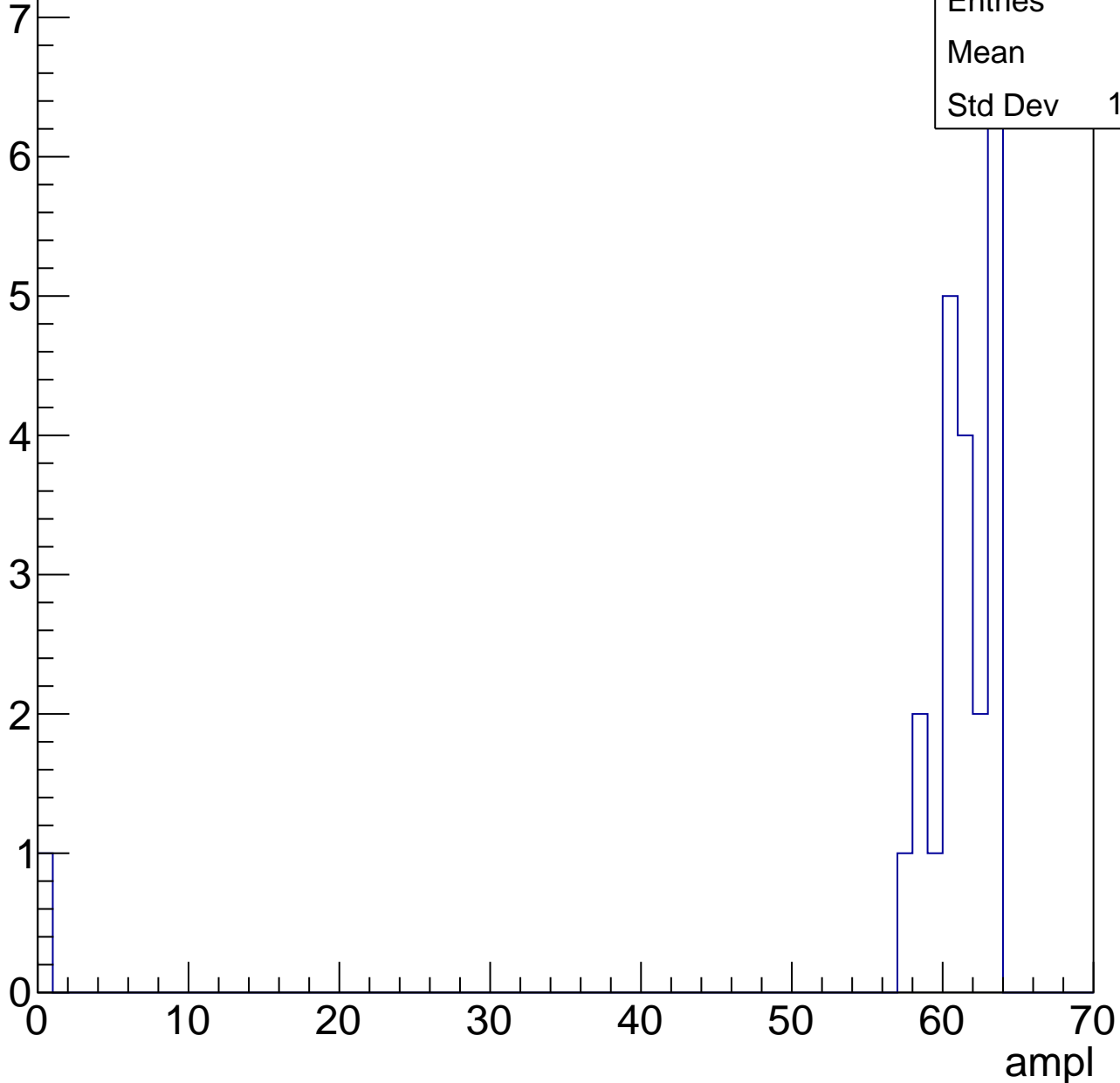


# B0L001S, U17-ch55, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	23
Mean	58.3
Std Dev	12.56



# B0L001S, U17-ch55, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch55, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U17-ch56, adc0

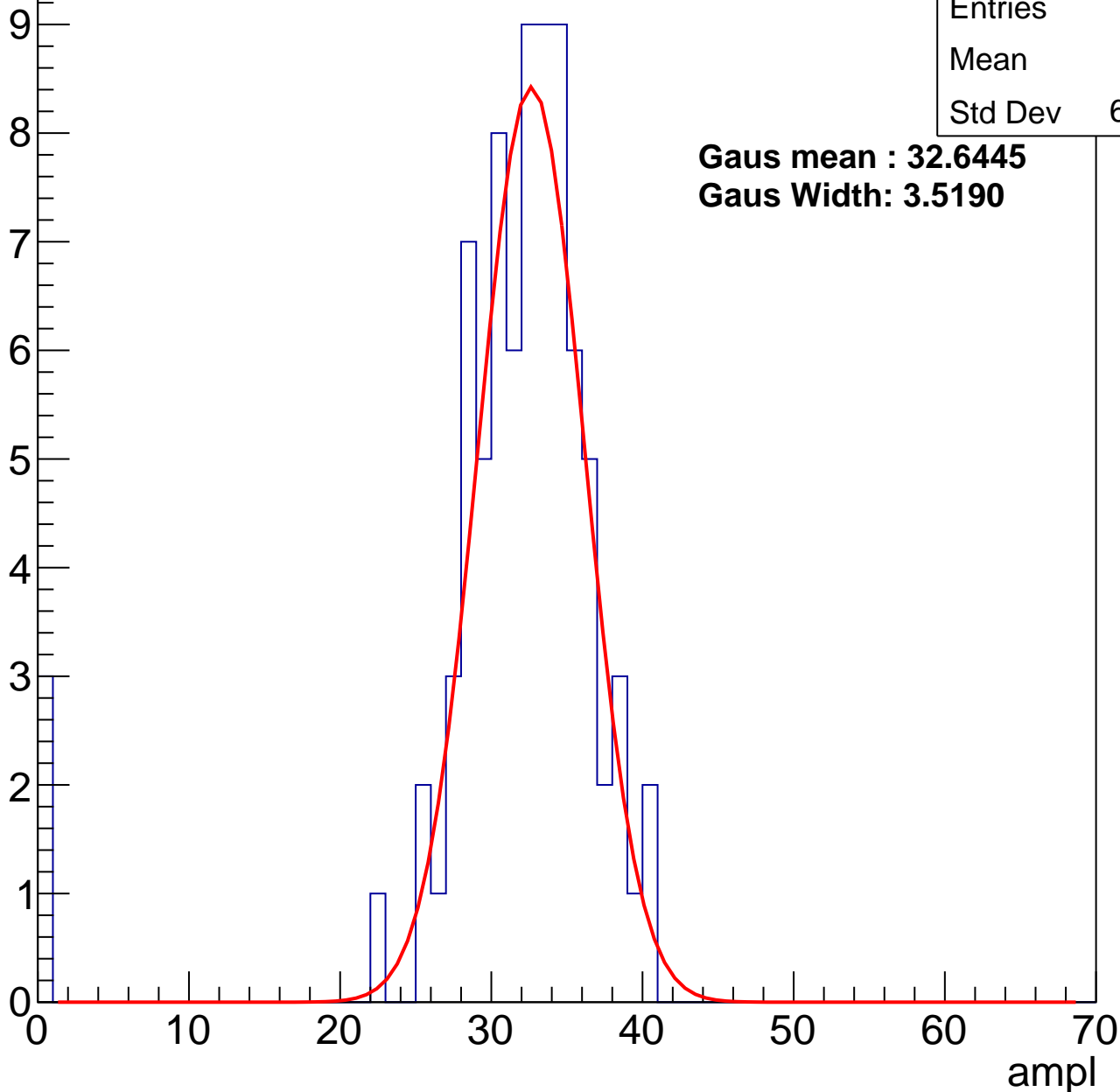
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	82
Mean	30.9
Std Dev	6.977

**Gaus mean : 32.6445**

**Gaus Width: 3.5190**



# B0L001S, U17-ch56, adc1

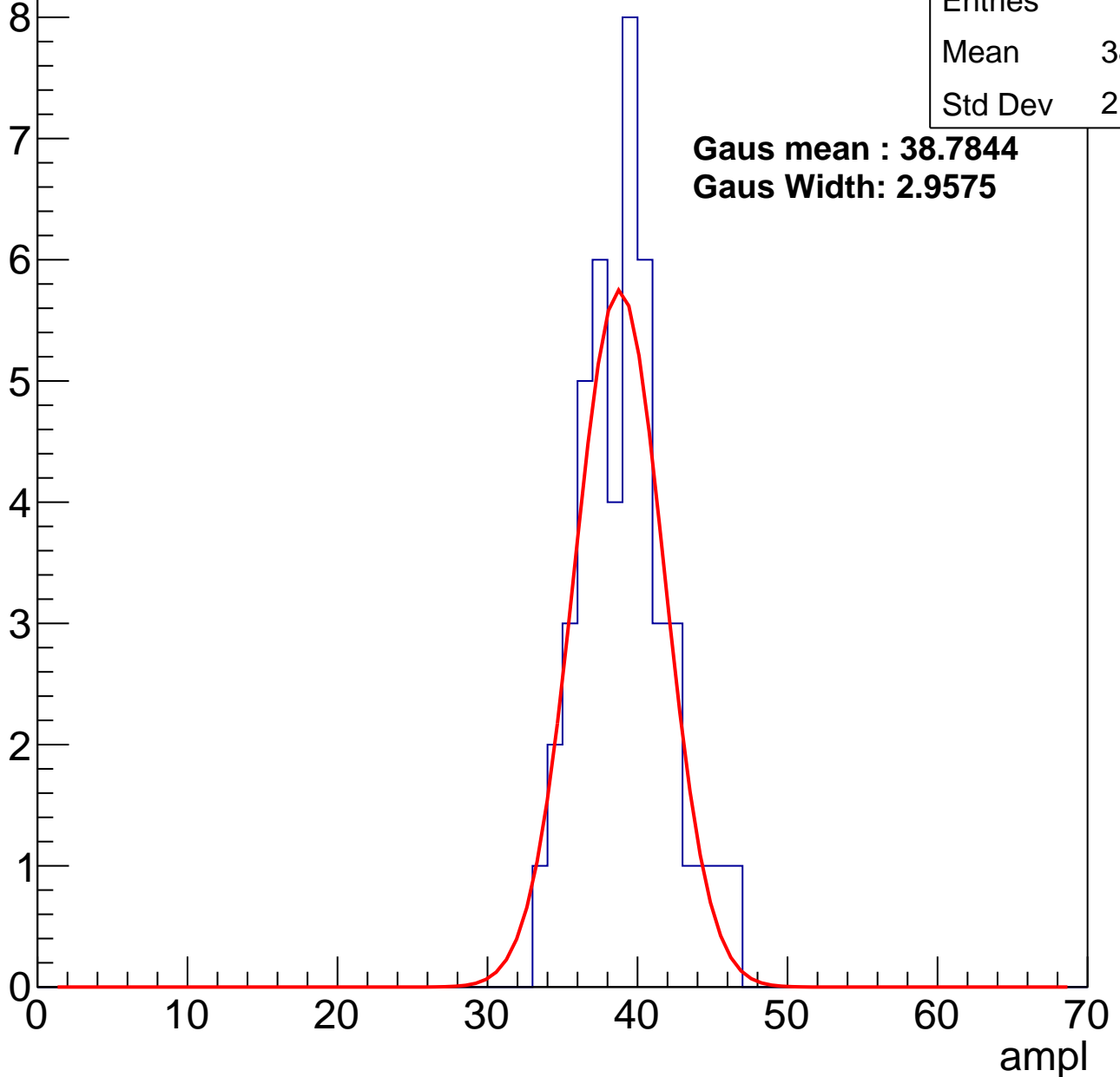
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	45
Mean	38.64
Std Dev	2.876

**Gaus mean : 38.7844**

**Gaus Width: 2.9575**



# B0L001S, U17-ch56, adc2

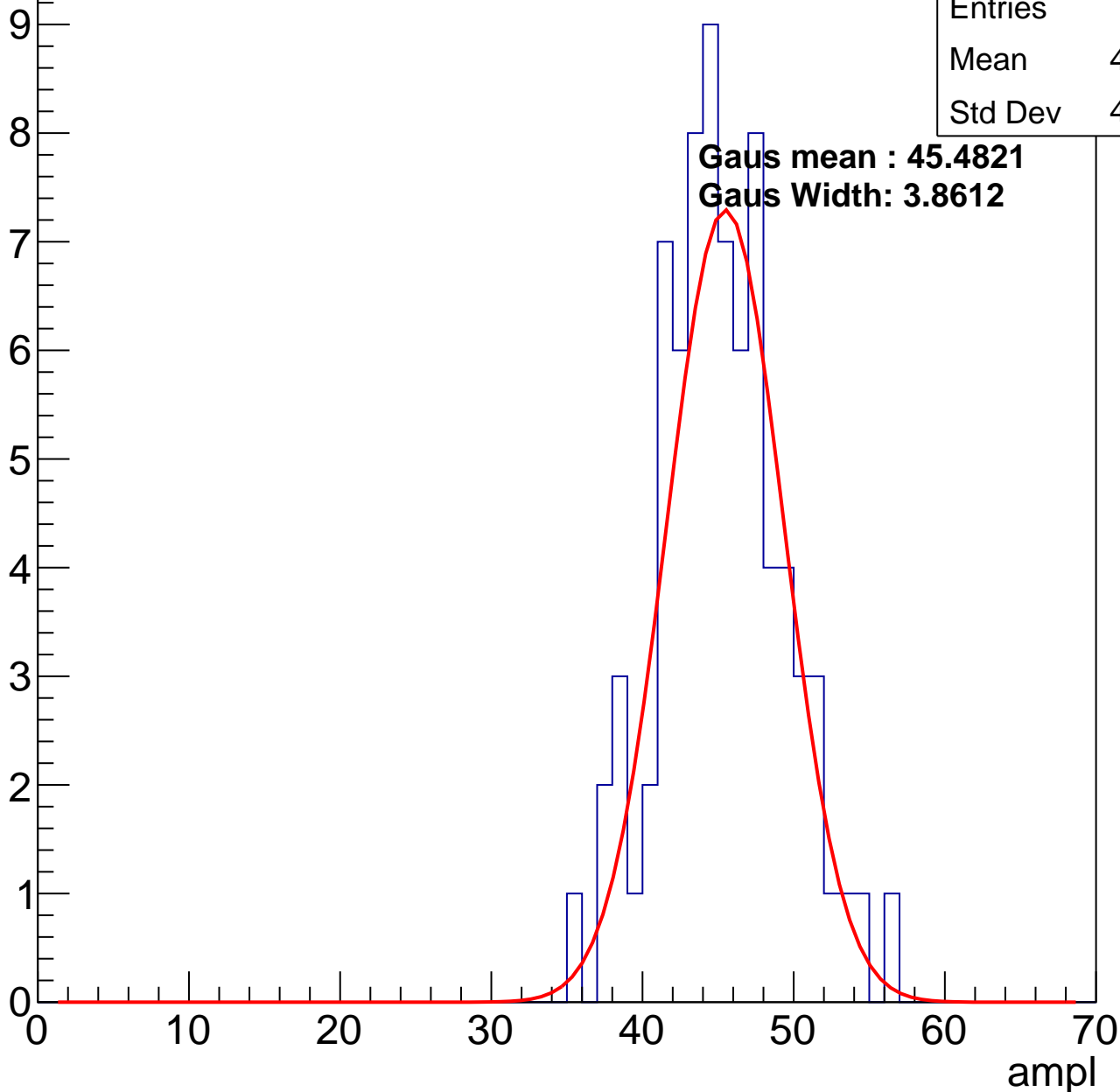
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	78
Mean	44.79
Std Dev	4.084

**Gaus mean : 45.4821**

**Gaus Width: 3.8612**

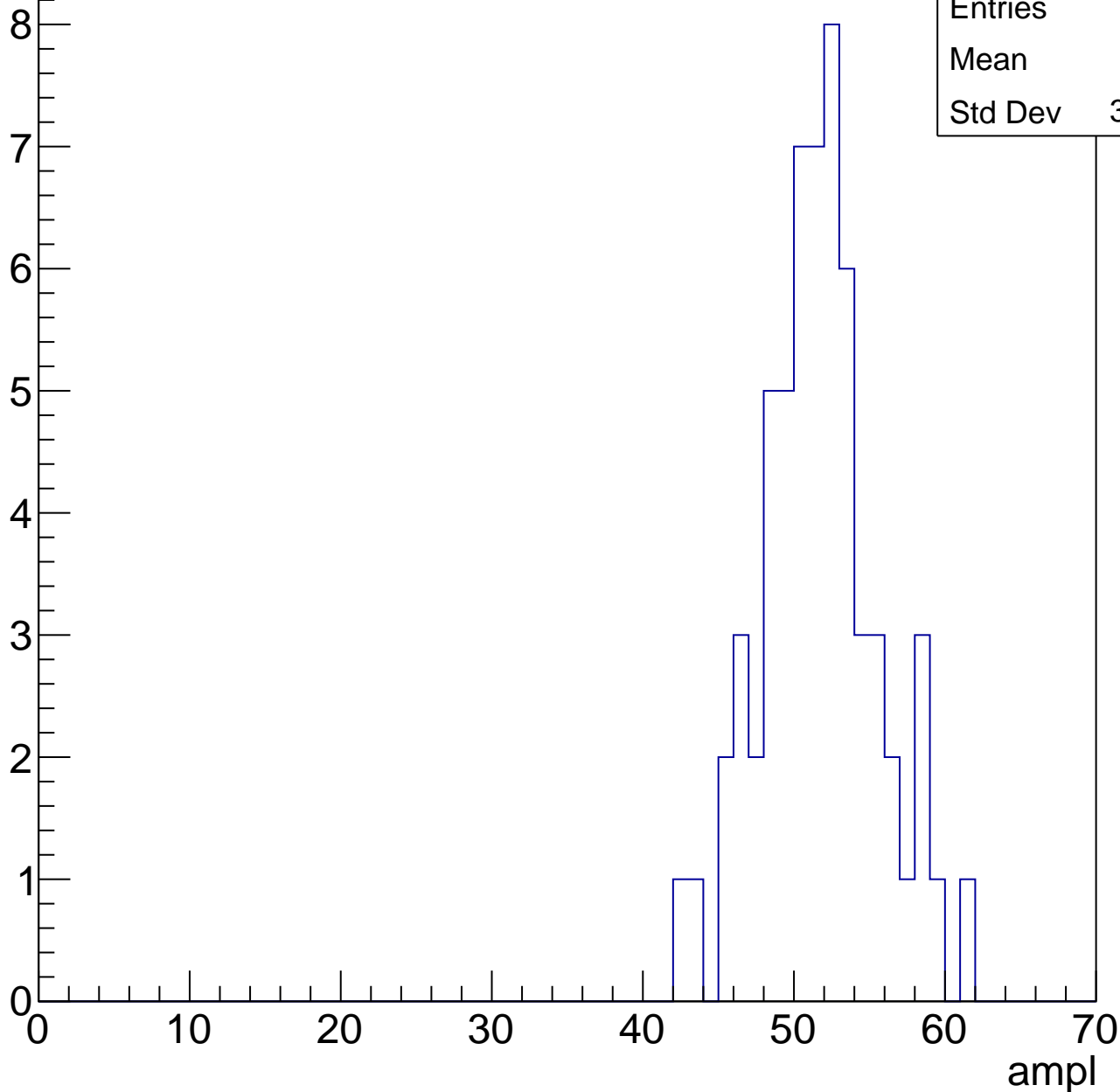


# B0L001S, U17-ch56, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	51.2
Std Dev	3.836

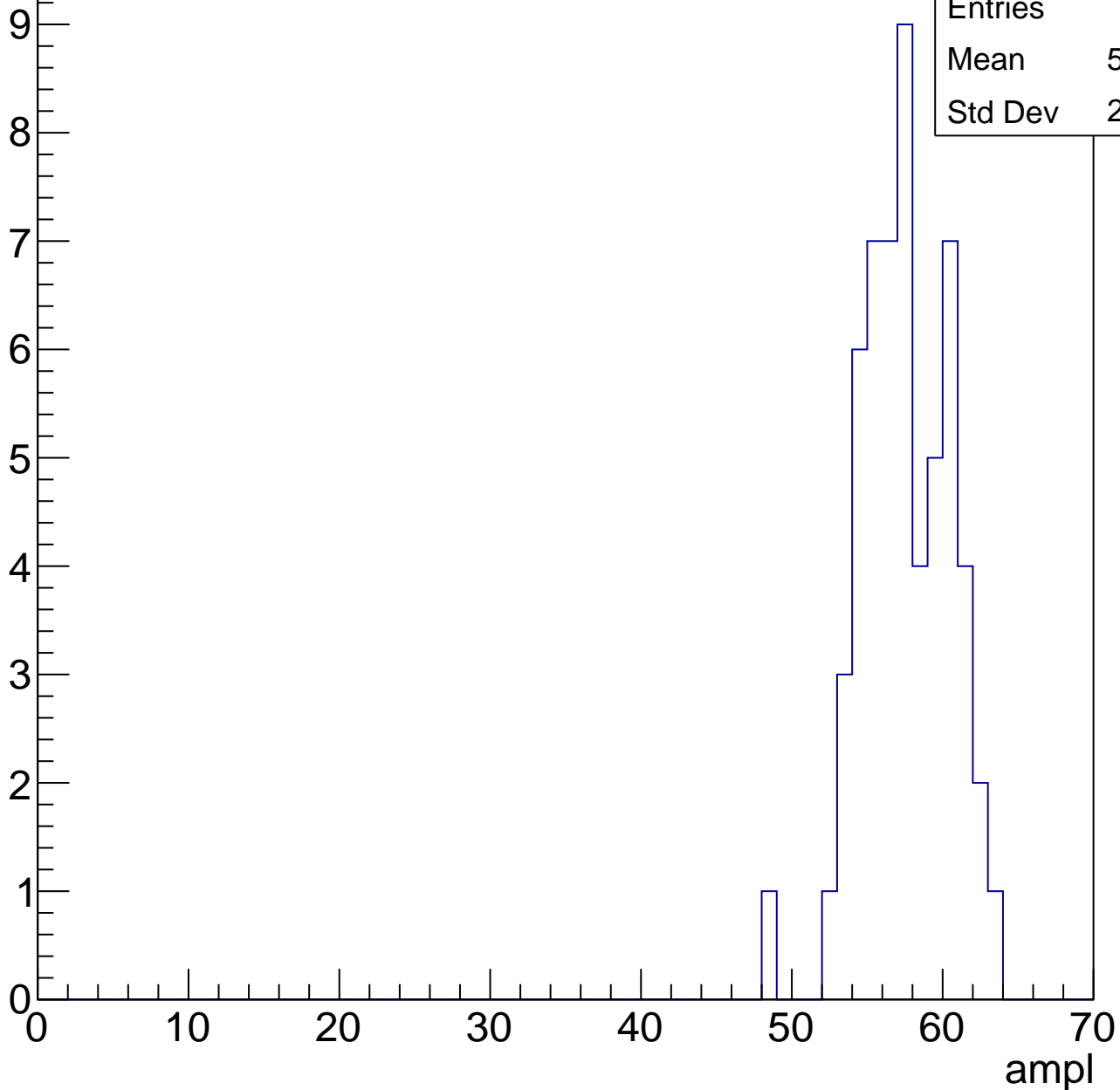


# B0L001S, U17-ch56, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	57.04
Std Dev	2.902

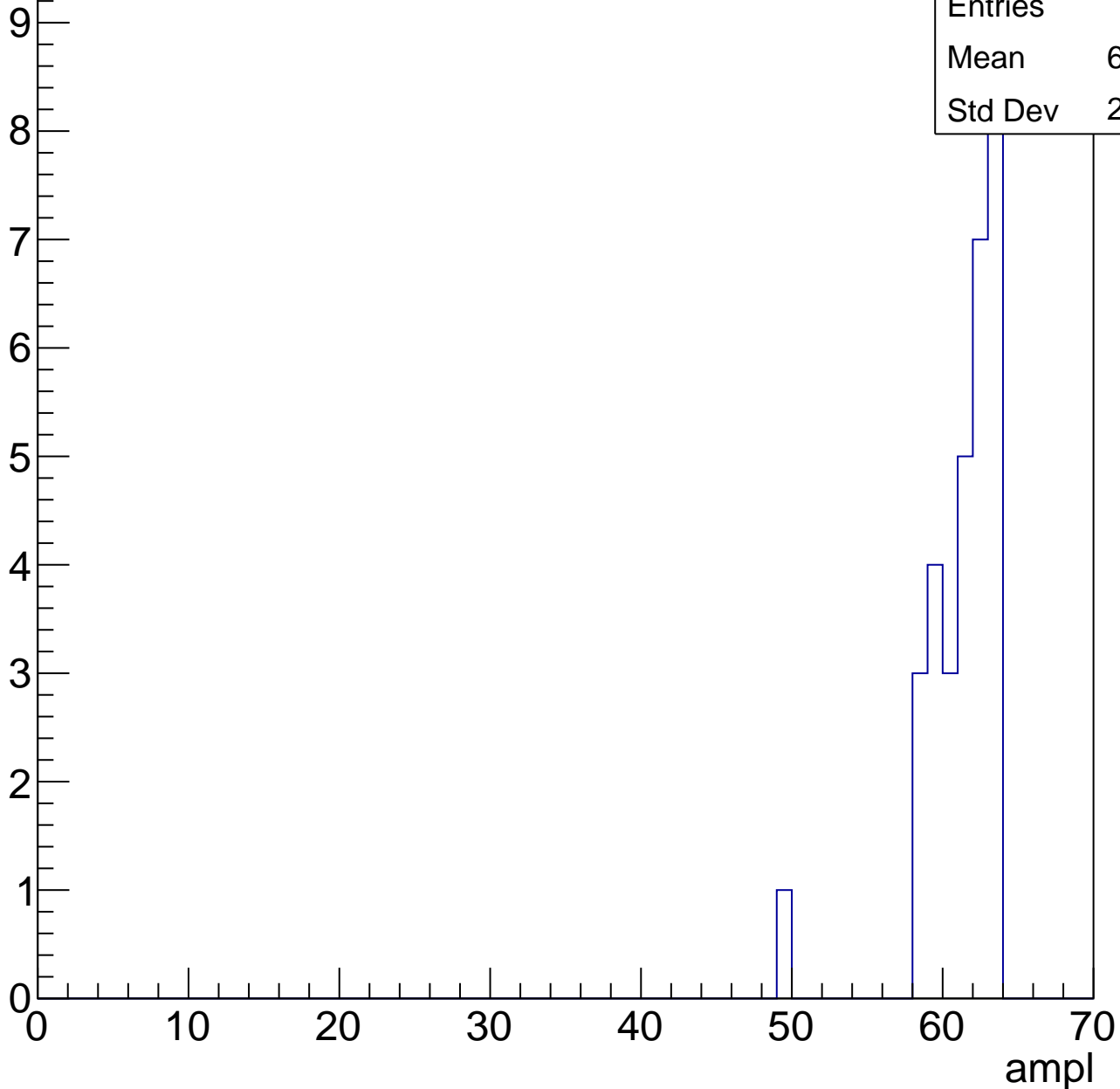


# B0L001S, U17-ch56, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	32
Mean	60.78
Std Dev	2.689



# B0L001S, U17-ch56, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch56, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U17-ch57, adc0

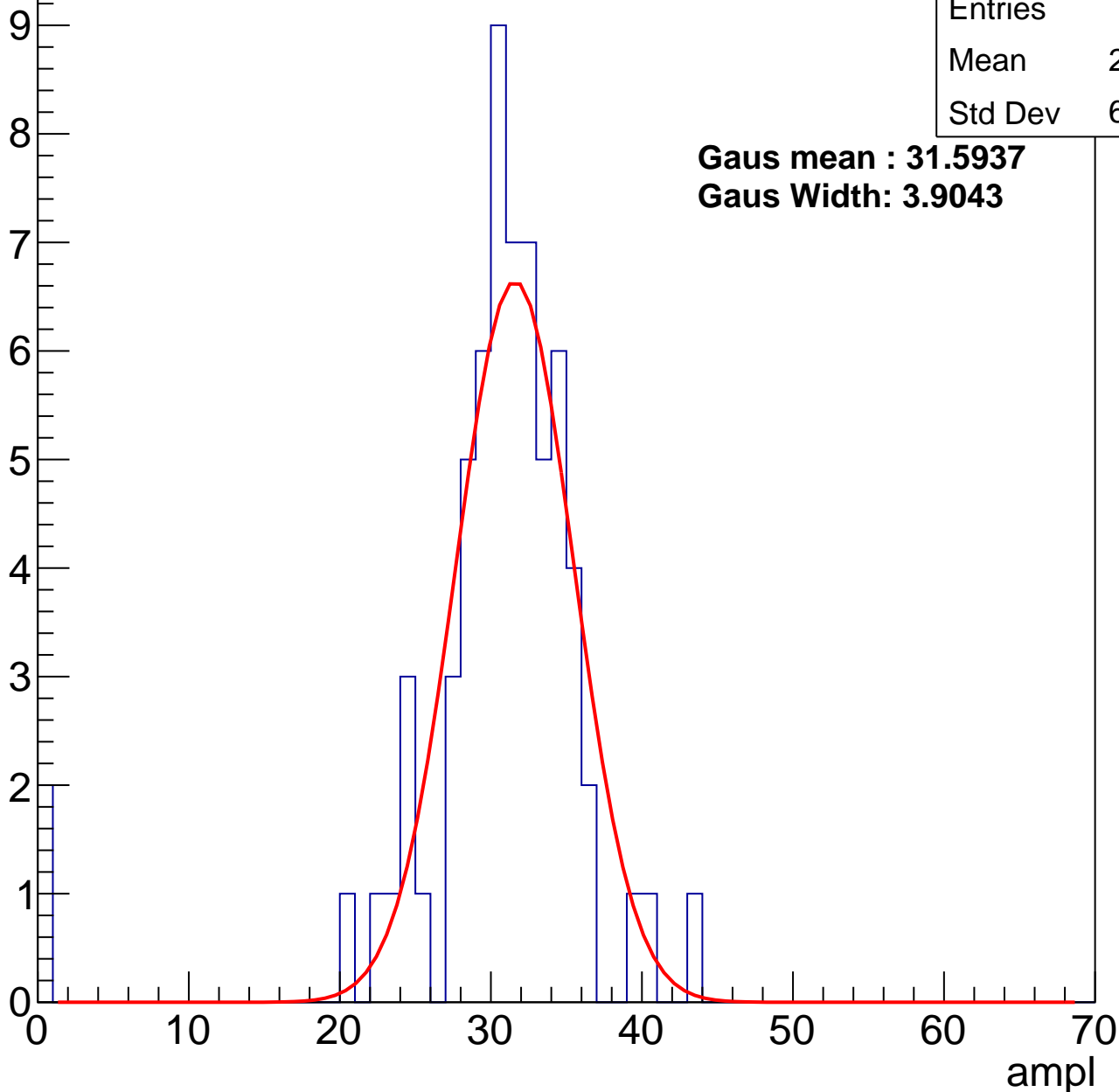
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	29.86
Std Dev	6.624

**Gaus mean : 31.5937**

**Gaus Width: 3.9043**



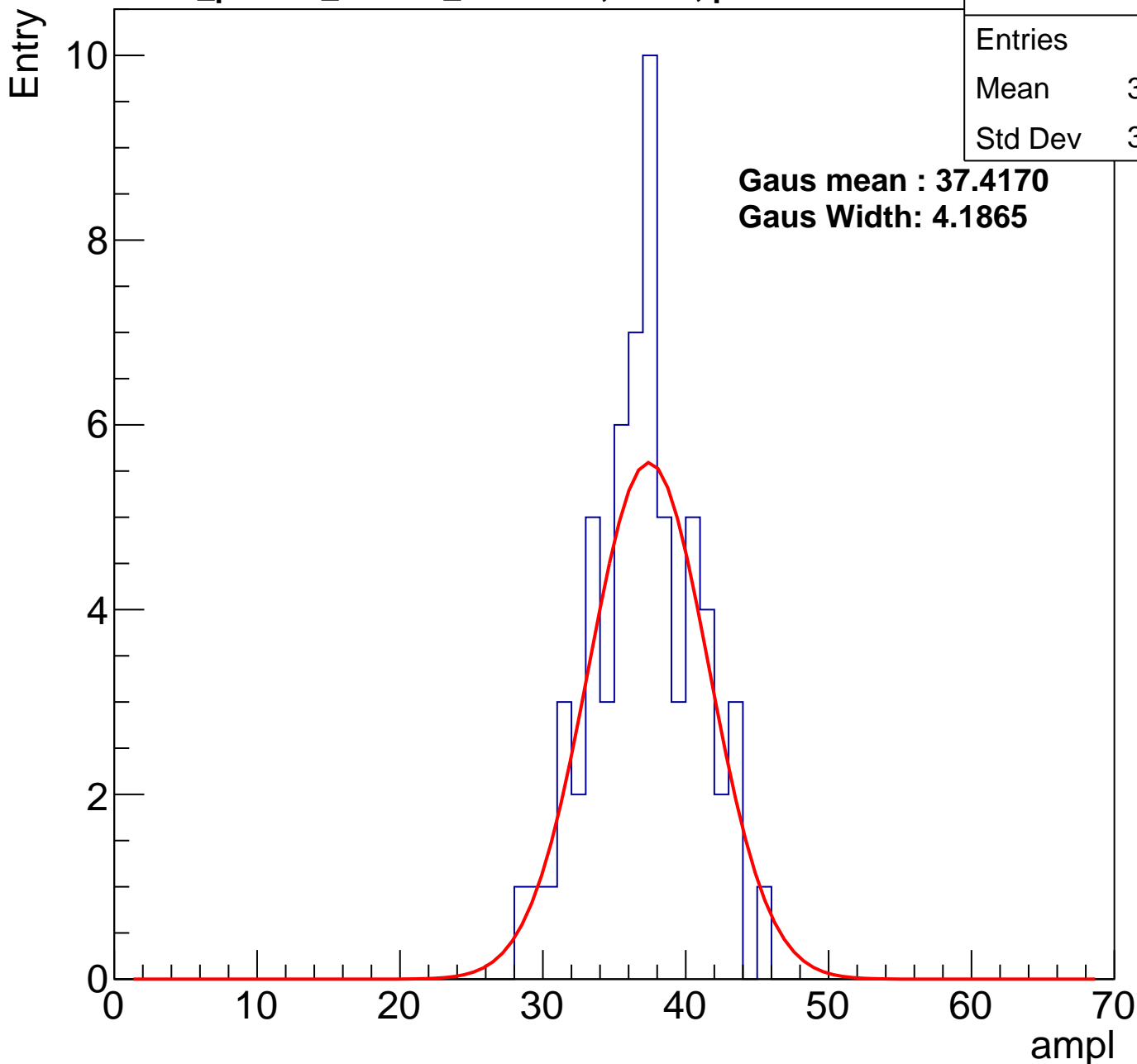
# B0L001S, U17-ch57, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	62
Mean	36.65
Std Dev	3.659

**Gaus mean : 37.4170**

**Gaus Width: 4.1865**



# B0L001S, U17-ch57, adc2

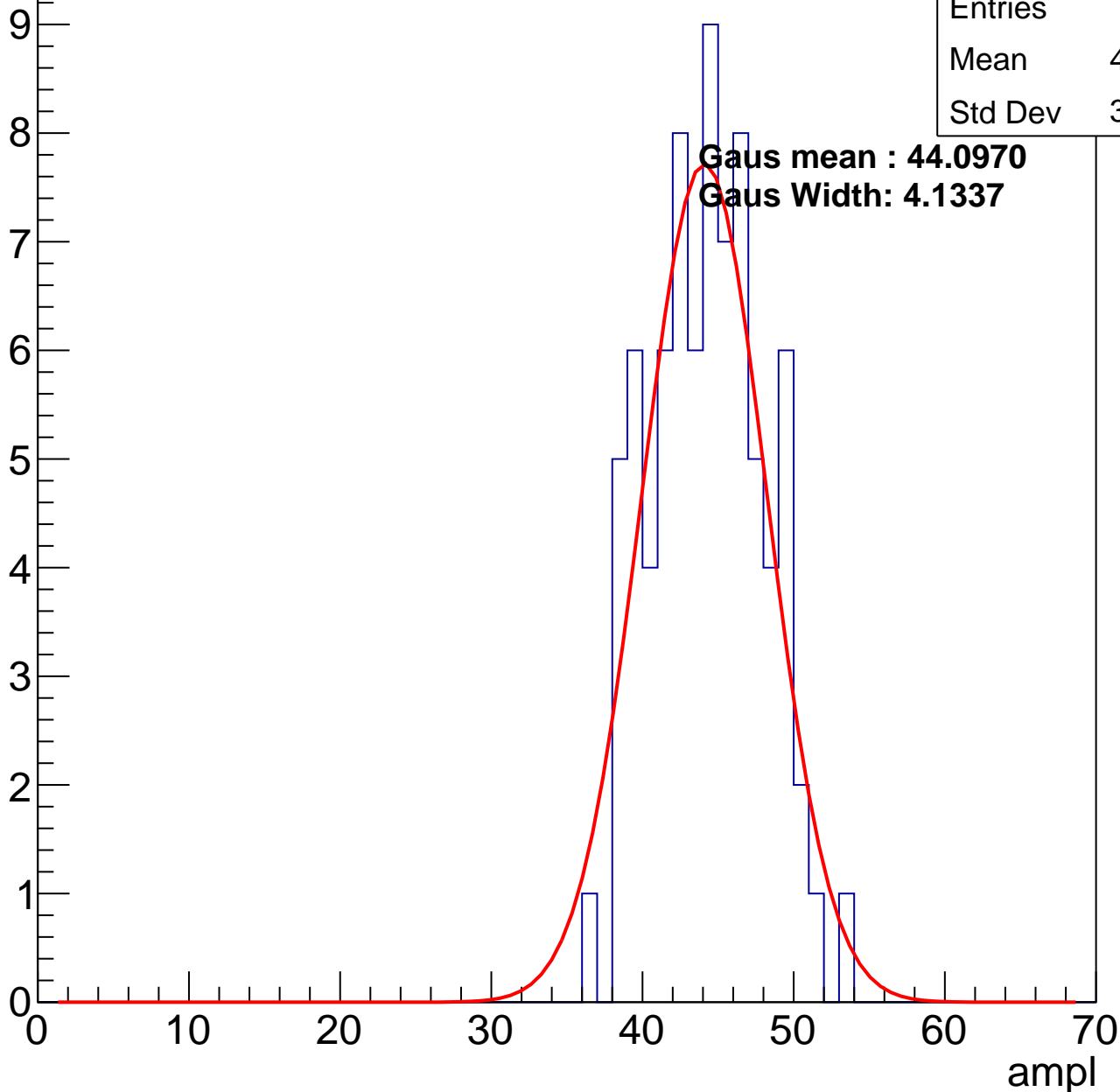
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	79
Mean	43.85
Std Dev	3.643

**Gaus mean : 44.0970**

**Gaus Width: 4.1337**

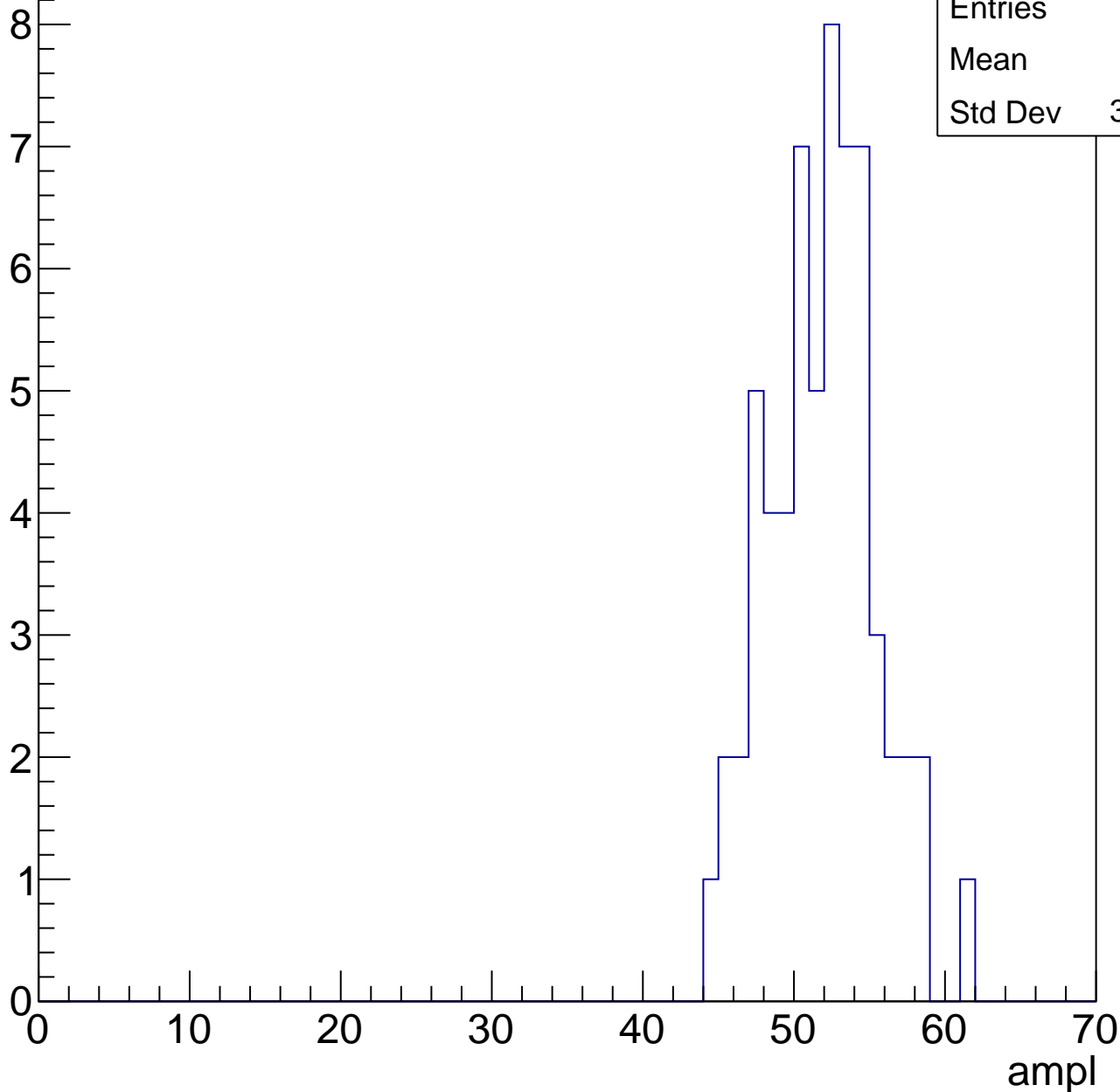


# B0L001S, U17-ch57, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

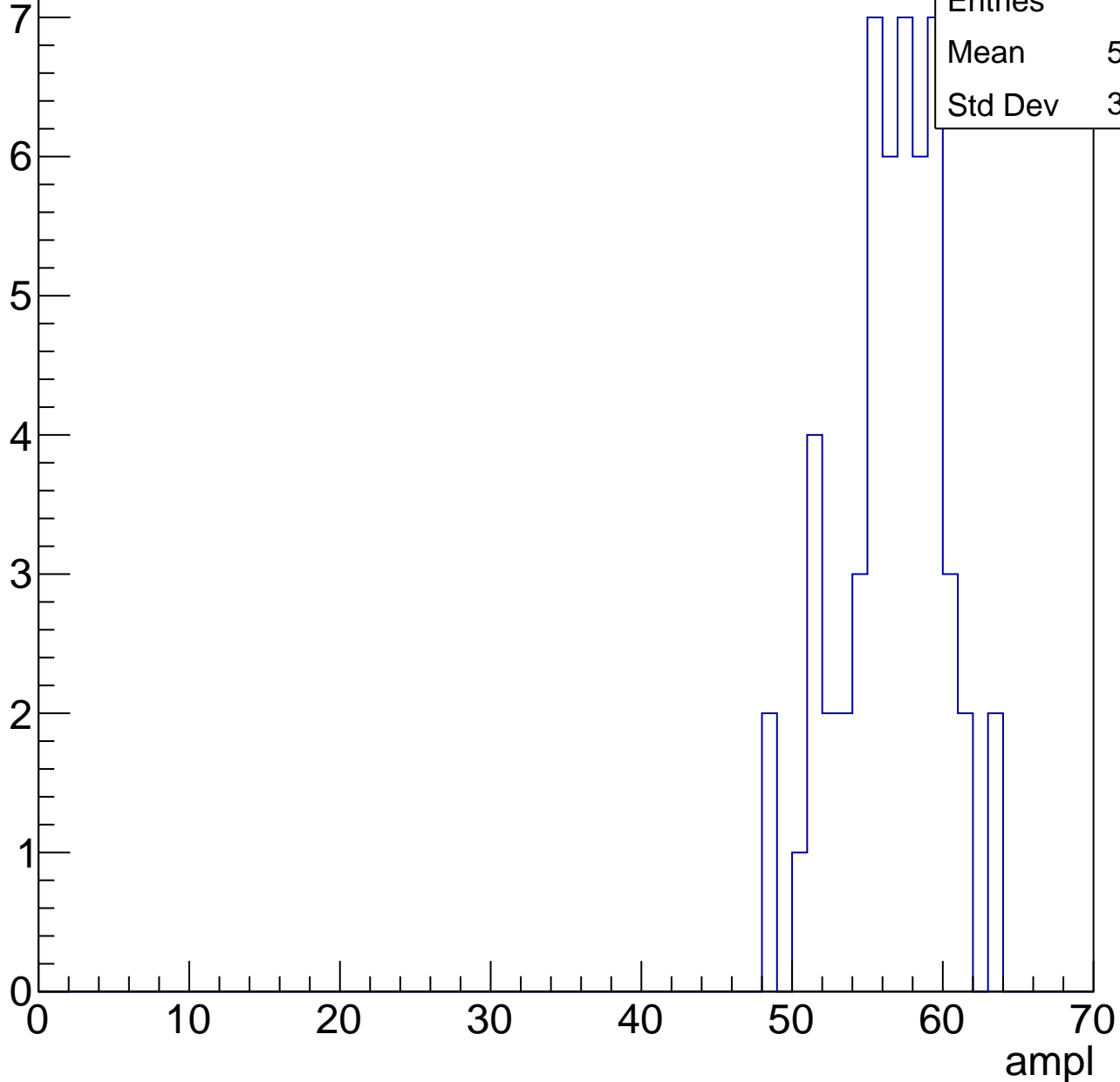
Entries	62
Mean	51.4
Std Dev	3.517



# B0L001S, U17-ch57, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



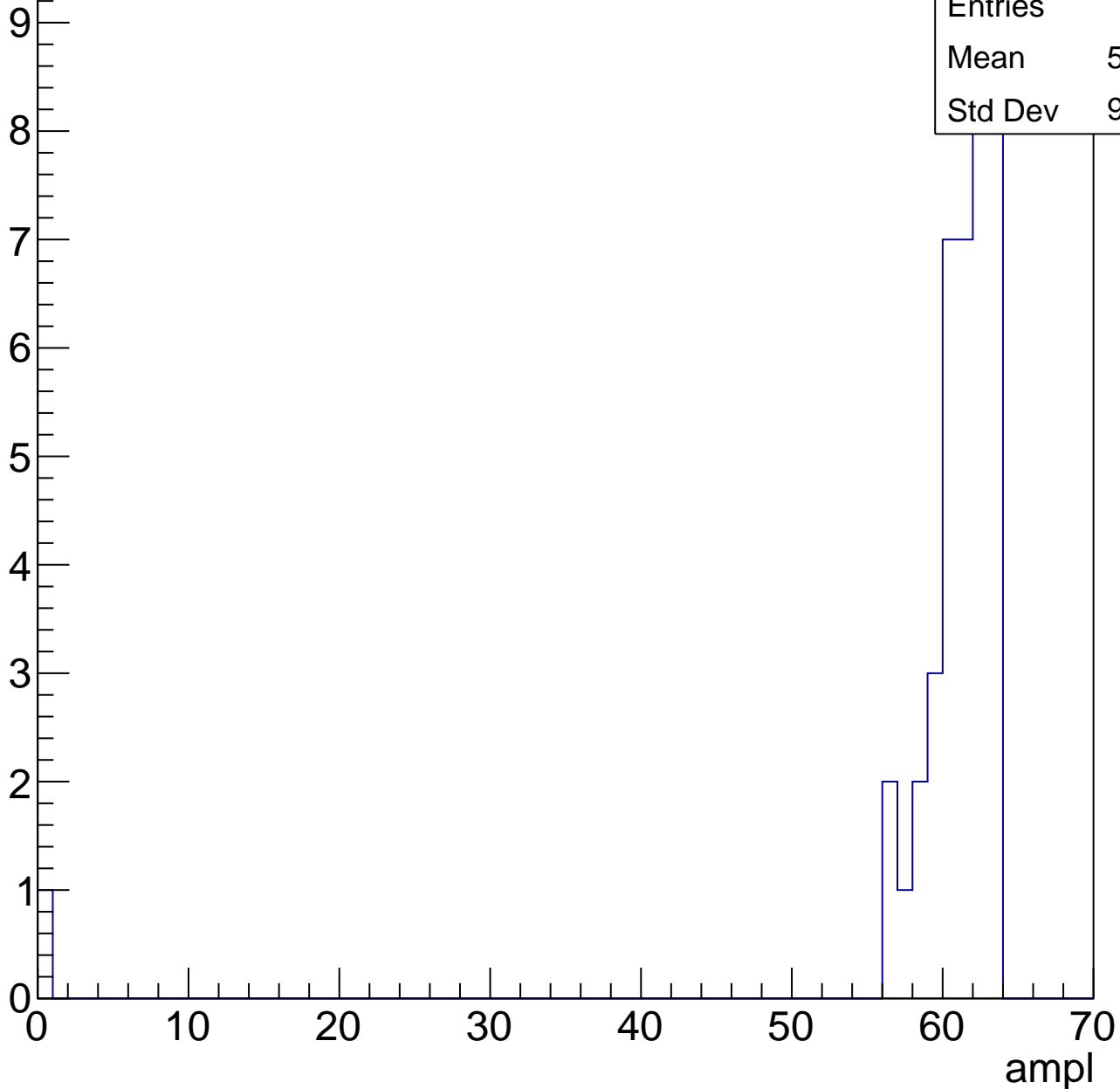
Entries	54
Mean	56.13
Std Dev	3.394

# B0L001S, U17-ch57, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	40
Mean	59.27
Std Dev	9.677



# B0L001S, U17-ch57, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	62
Std Dev	0



# B0L001S, U17-ch57, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U17-ch58, adc0

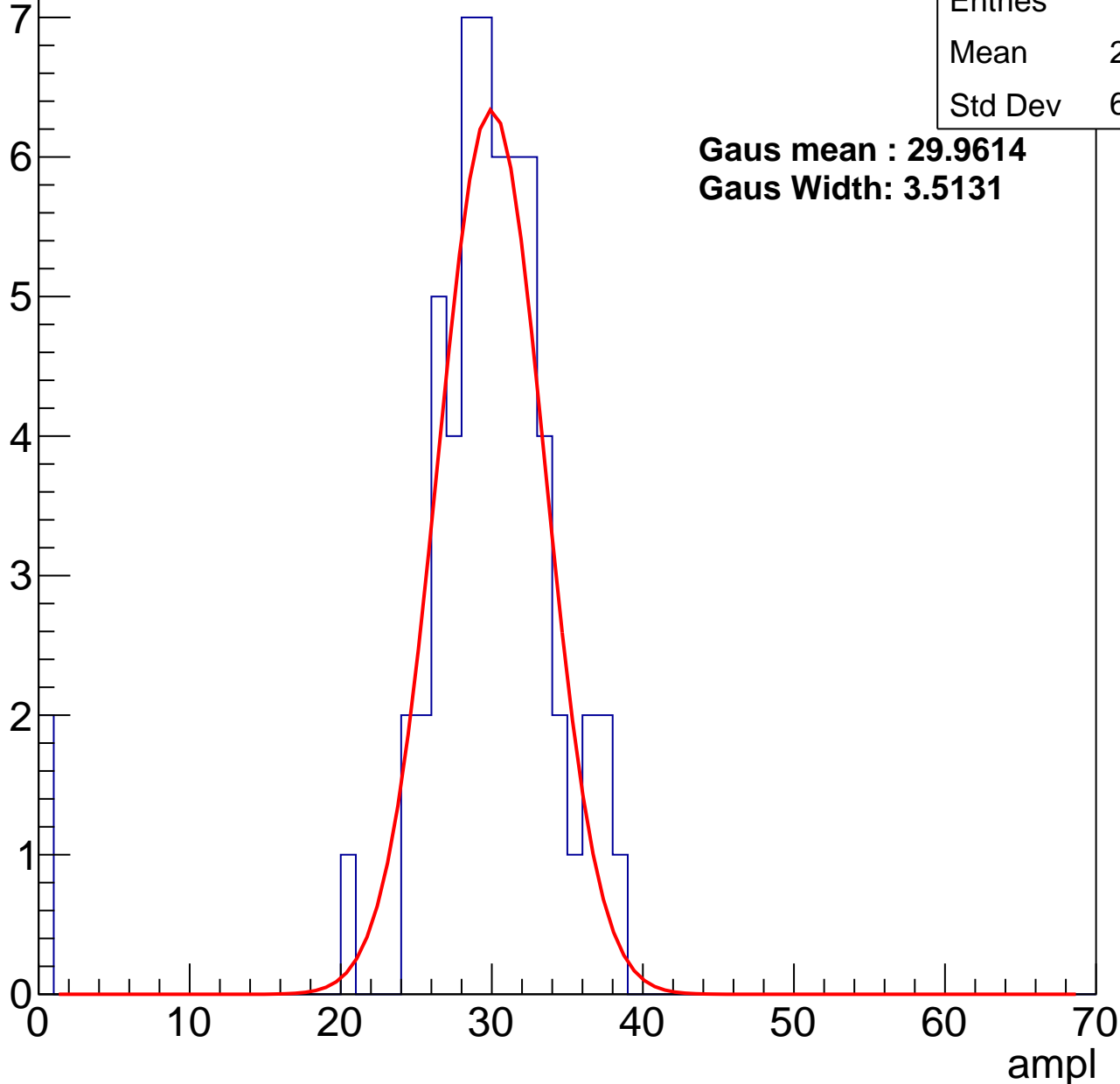
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	28.87
Std Dev	6.394

**Gaus mean : 29.9614**

**Gaus Width: 3.5131**



# B0L001S, U17-ch58, adc1

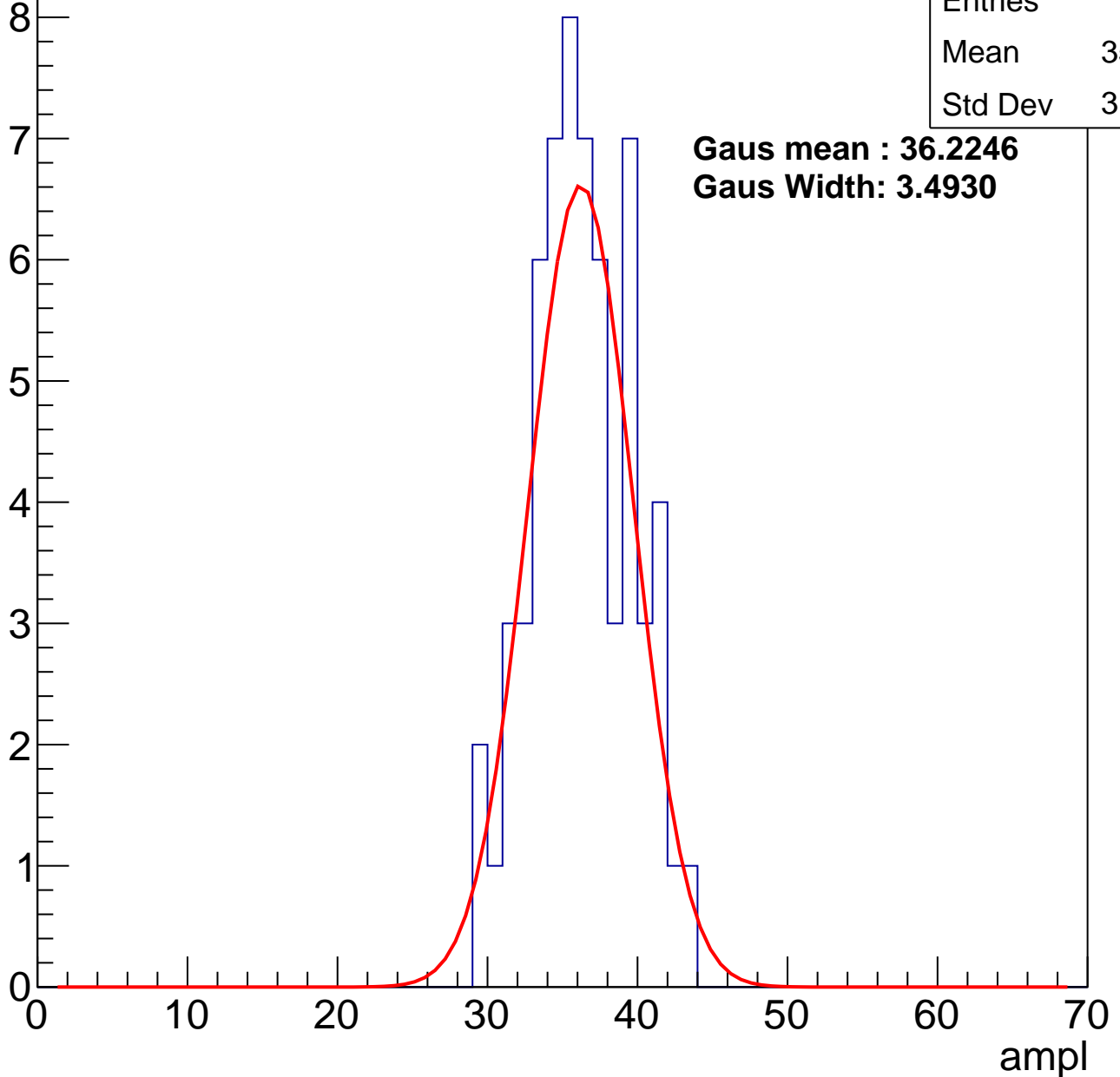
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	35.85
Std Dev	3.262

**Gaus mean : 36.2246**

**Gaus Width: 3.4930**



# B0L001S, U17-ch58, adc2

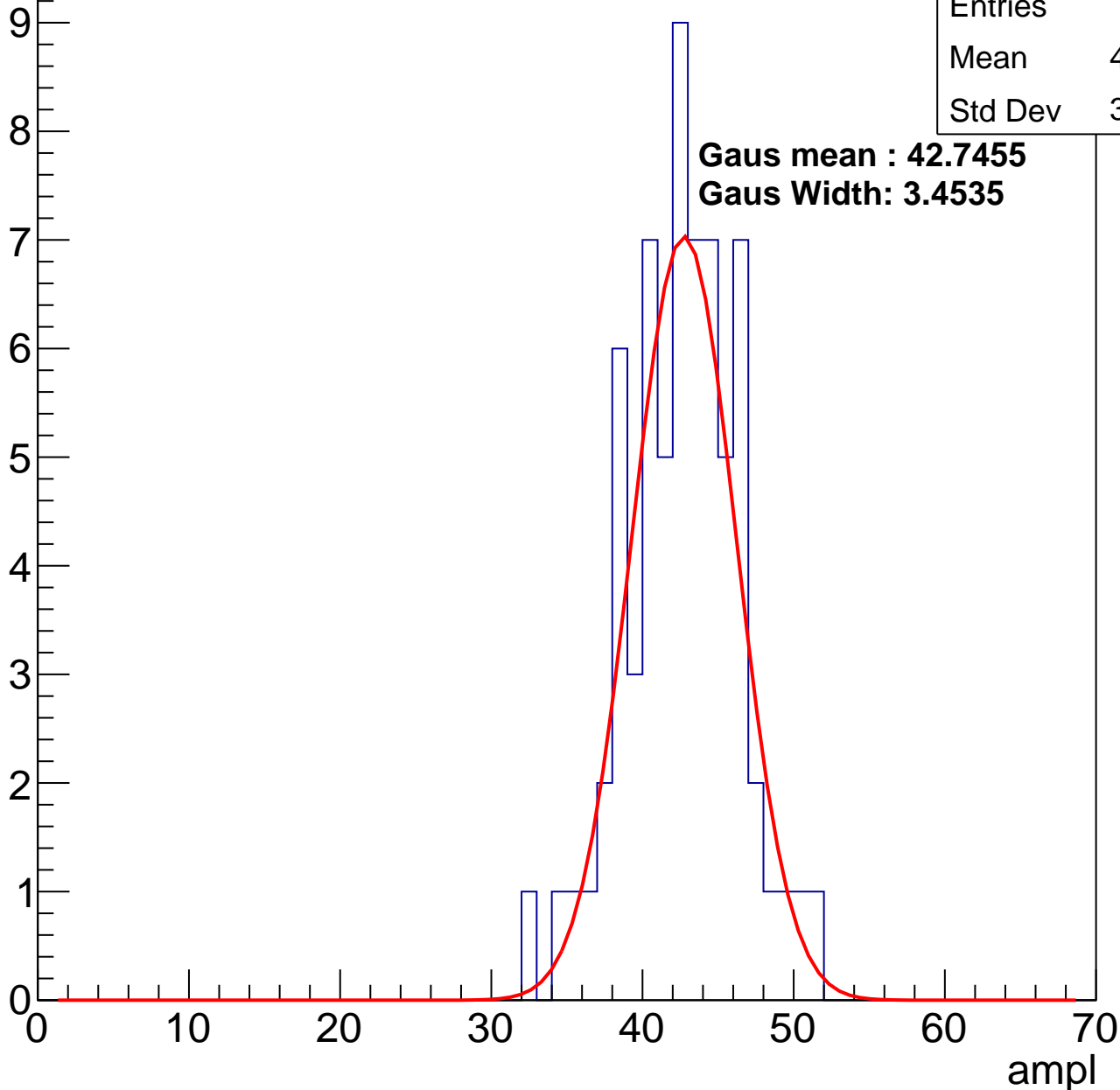
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	42.16
Std Dev	3.689

**Gaus mean : 42.7455**

**Gaus Width: 3.4535**

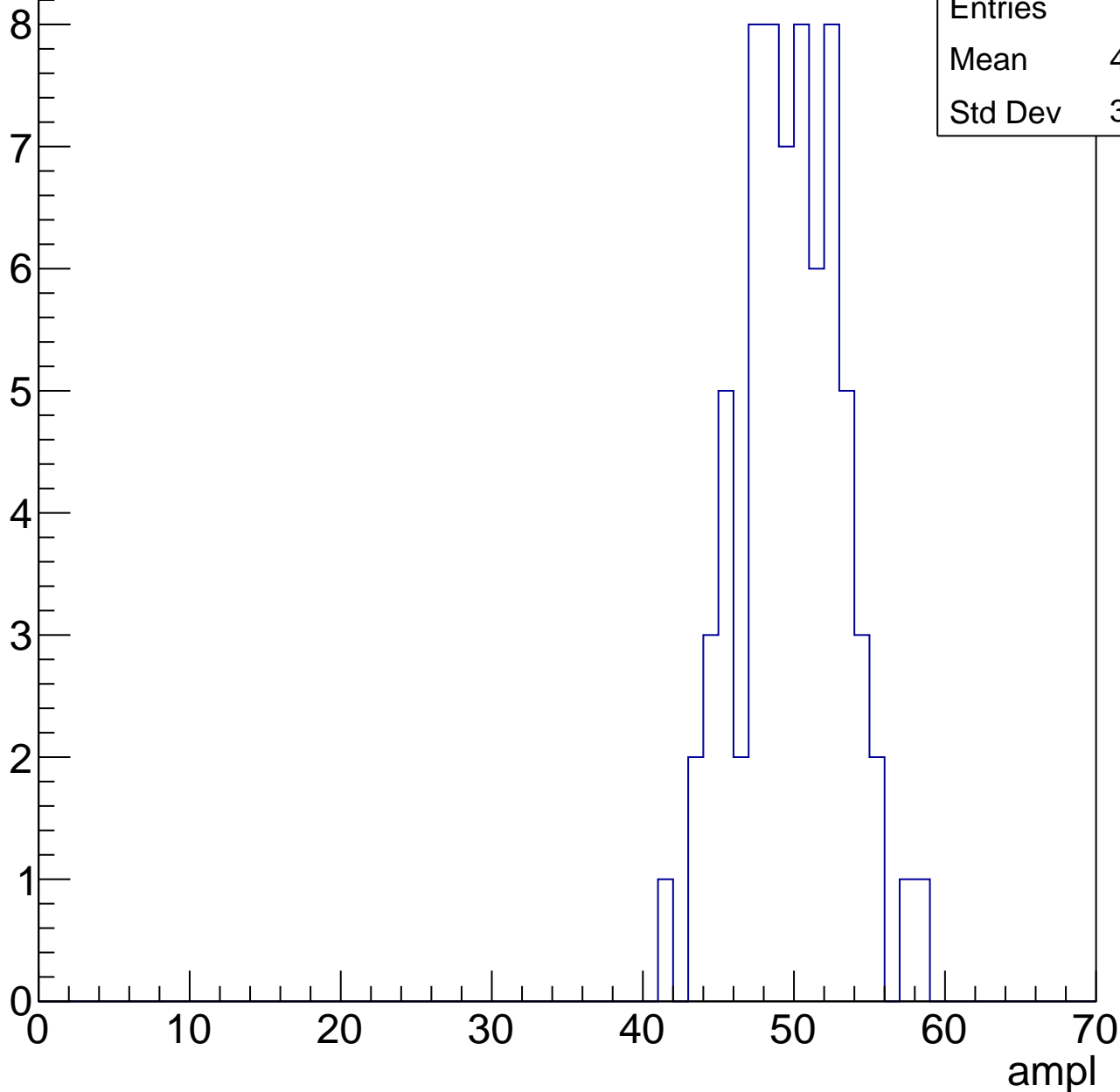


# B0L001S, U17-ch58, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	49.33
Std Dev	3.417

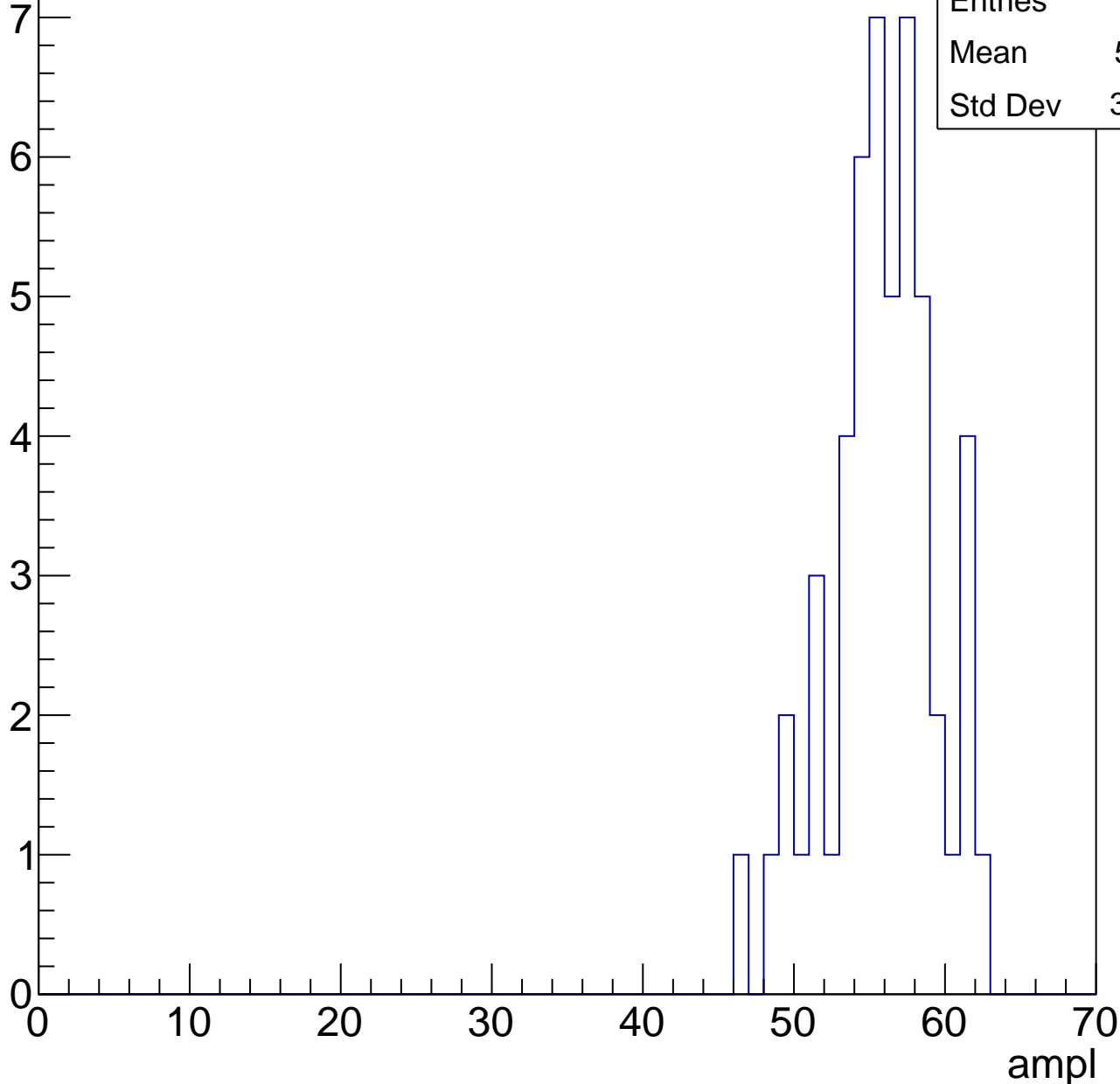


# B0L001S, U17-ch58, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

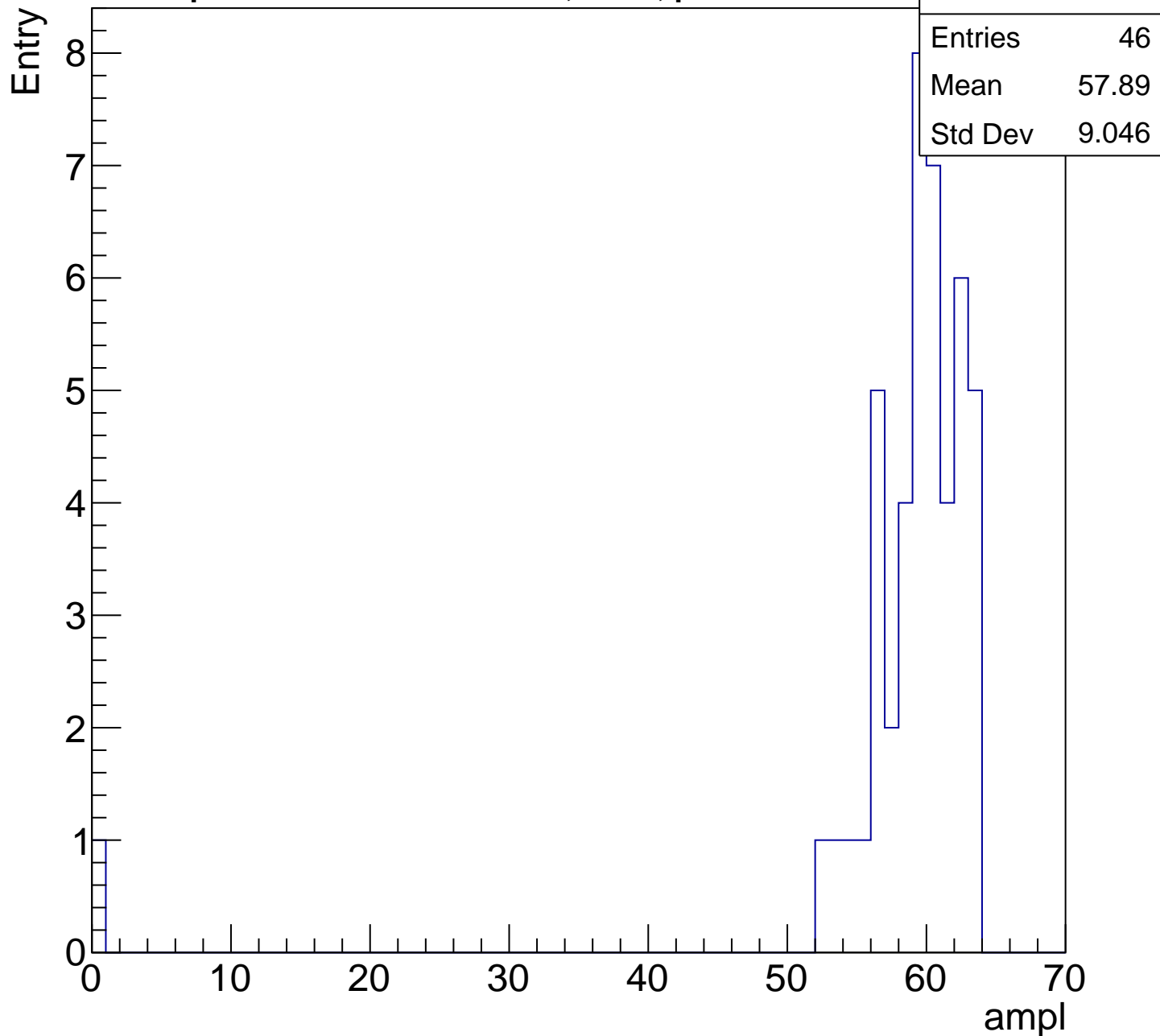
Entry

Entries	51
Mean	55.31
Std Dev	3.512



# B0L001S, U17-ch58, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

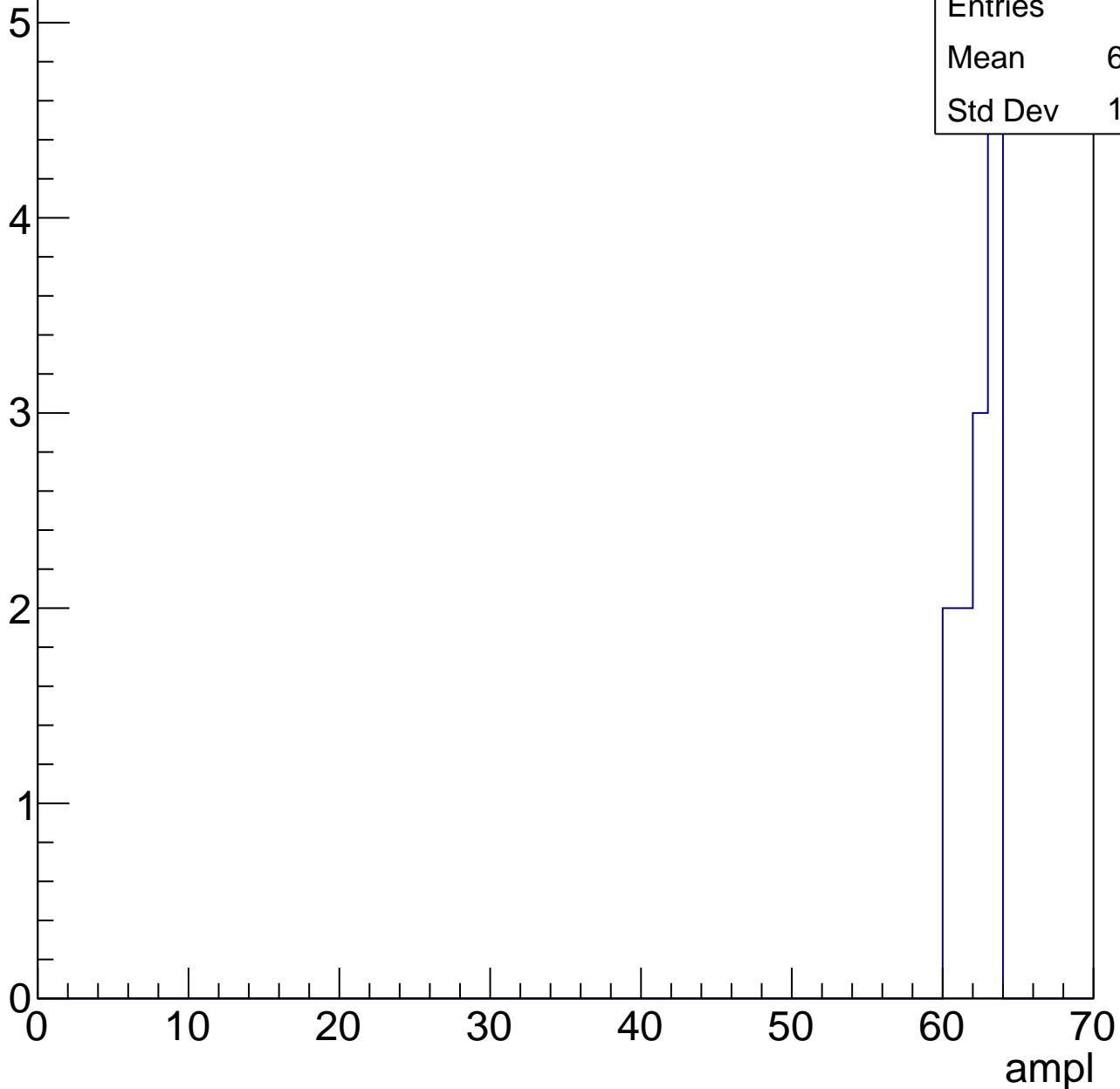


# B0L001S, U17-ch58, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	12
Mean	61.92
Std Dev	1.115





# B0L001S, U17-ch58, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U17-ch59, adc0

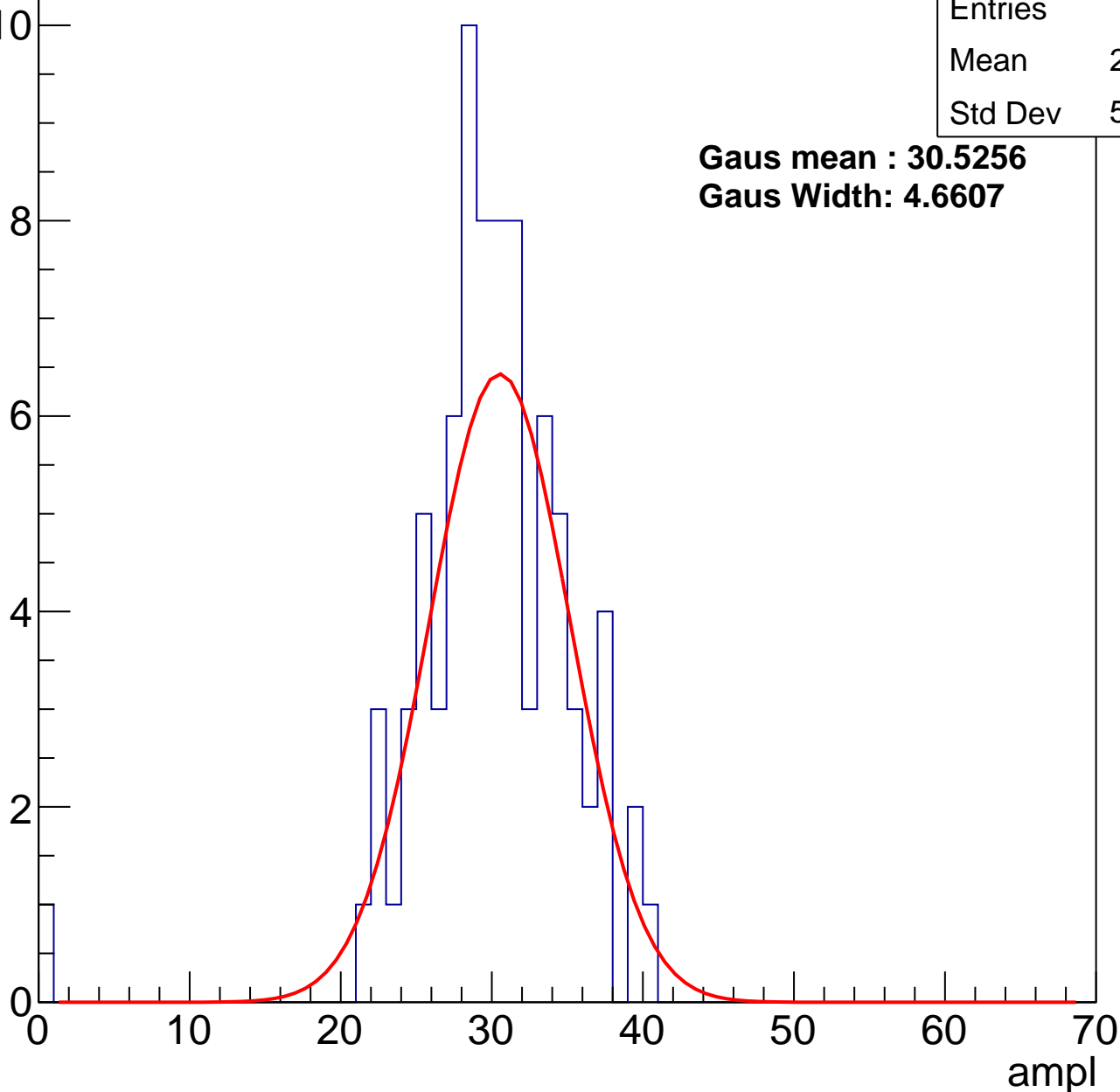
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	83
Mean	29.57
Std Dev	5.319

**Gaus mean : 30.5256**

**Gaus Width: 4.6607**



# B0L001S, U17-ch59, adc1

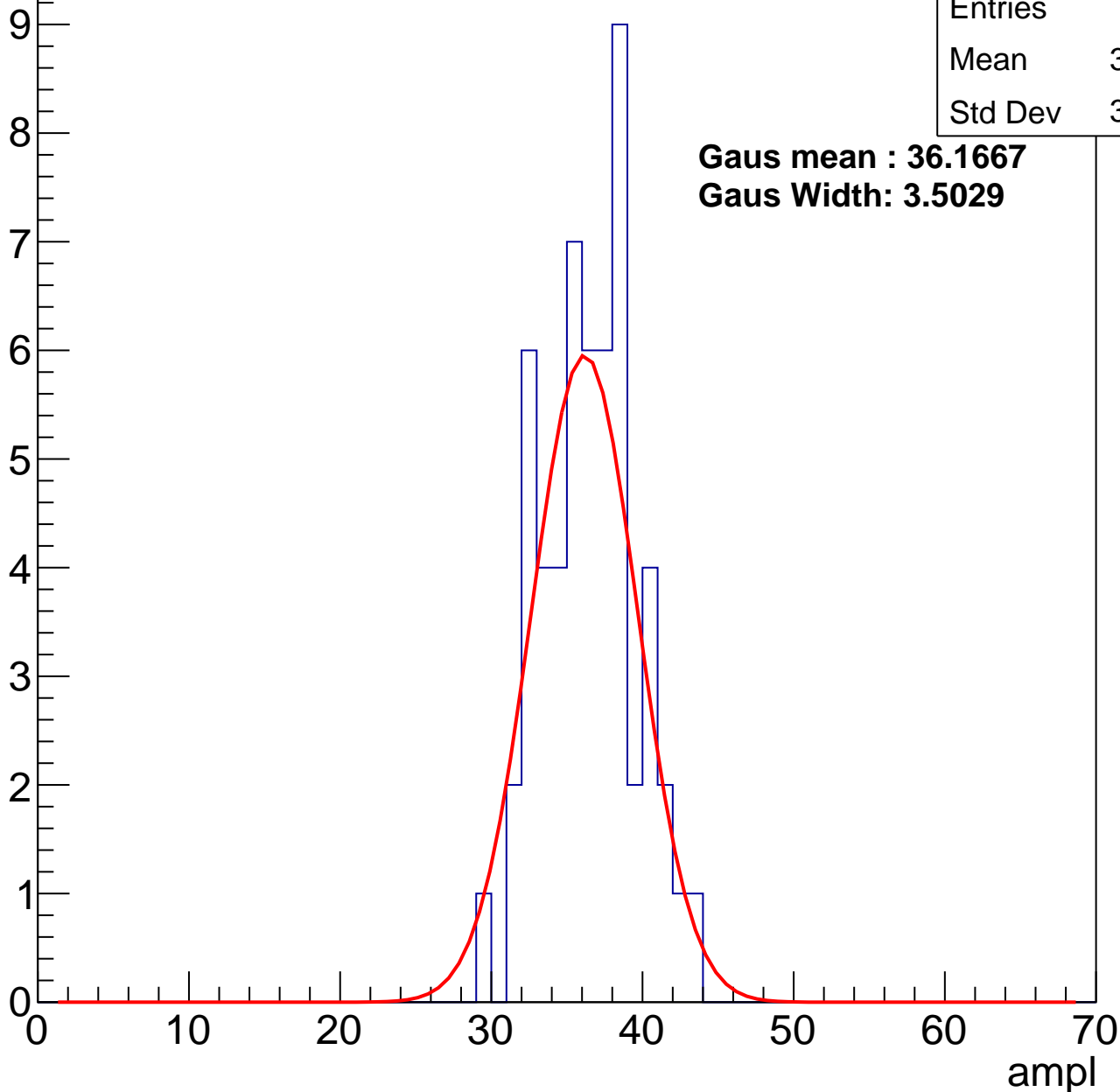
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	36.02
Std Dev	3.054

**Gaus mean : 36.1667**

**Gaus Width: 3.5029**



# B0L001S, U17-ch59, adc2

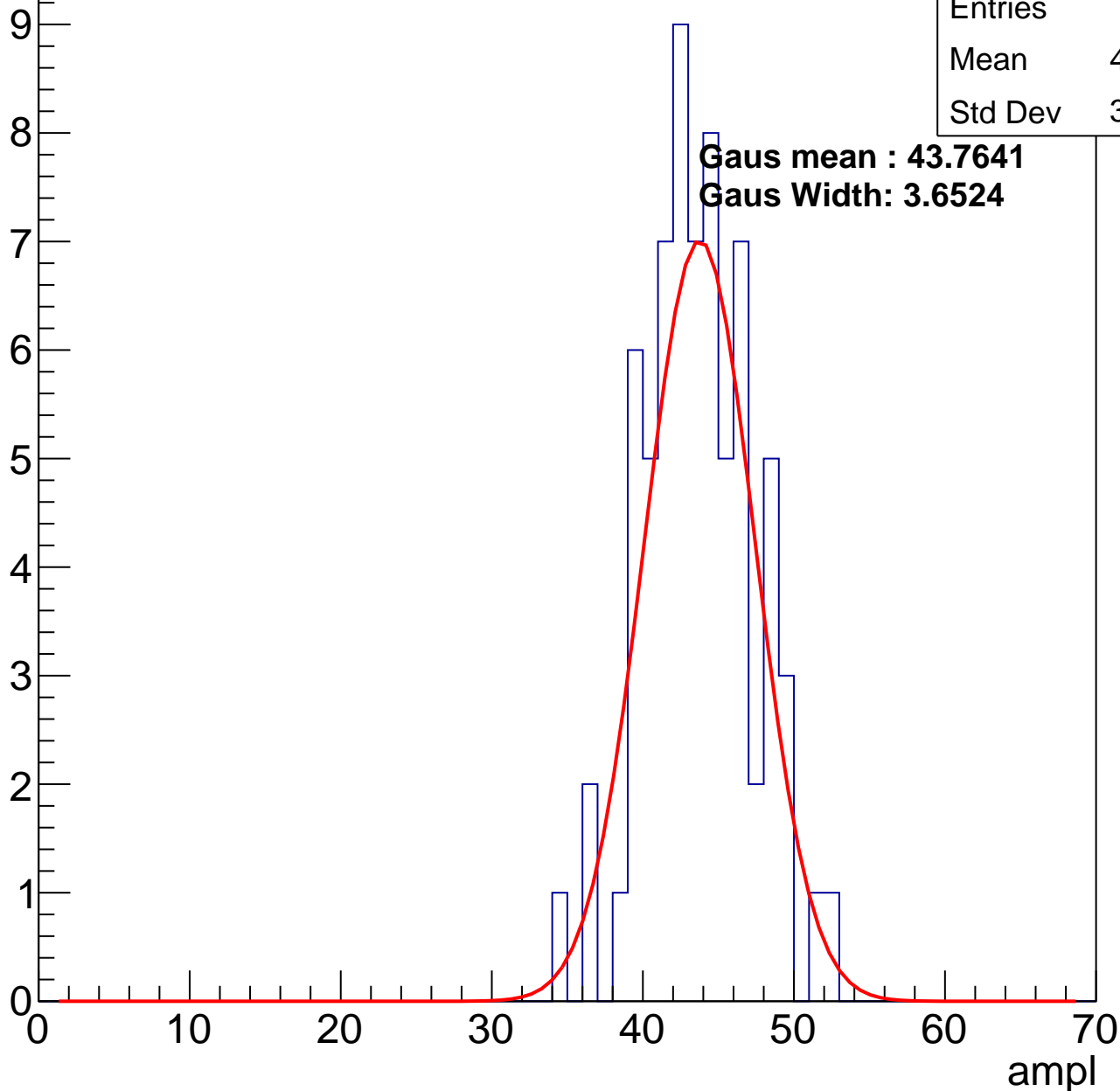
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	43.24
Std Dev	3.543

**Gaus mean : 43.7641**

**Gaus Width: 3.6524**

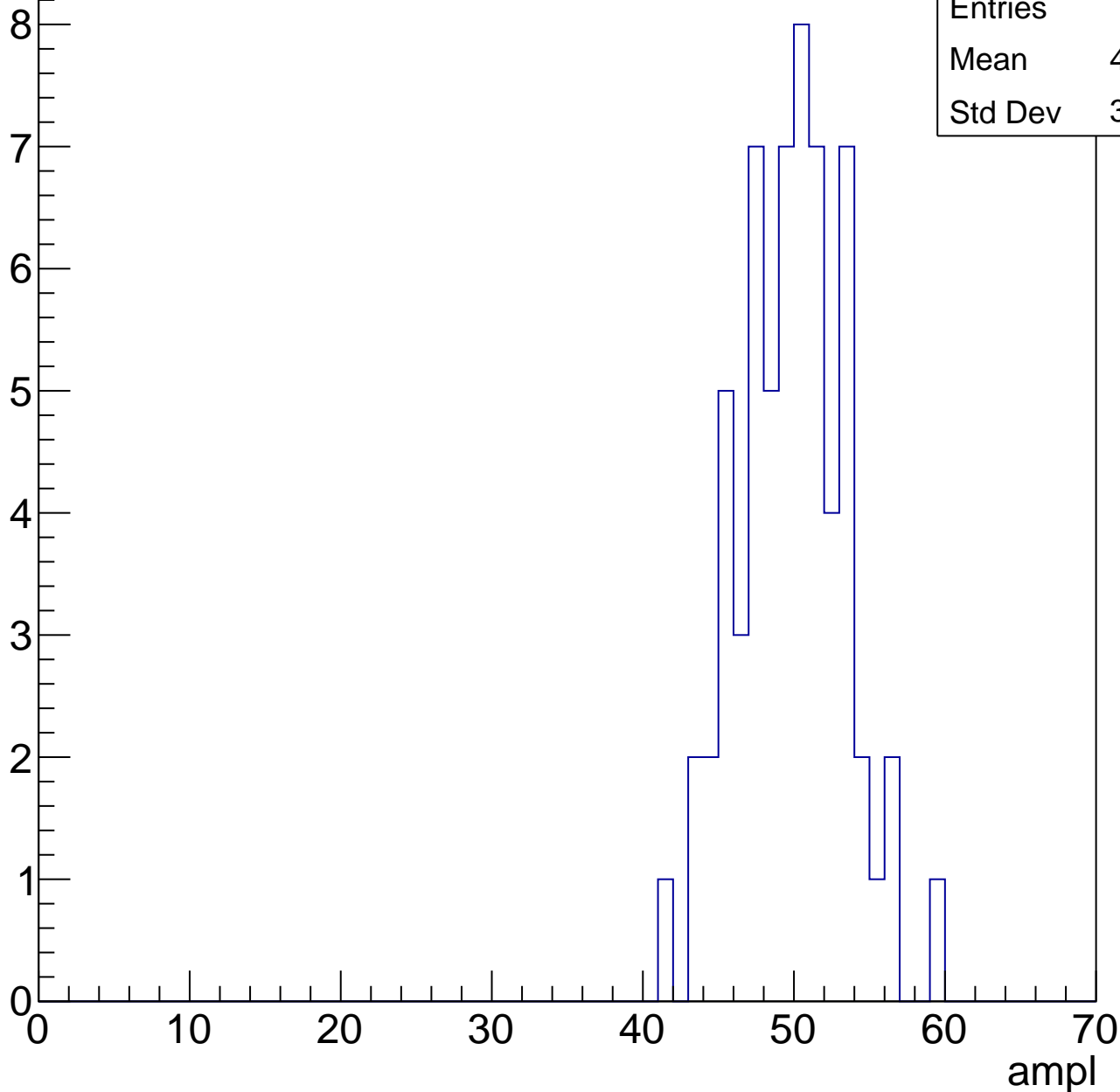


# B0L001S, U17-ch59, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	49.38
Std Dev	3.502

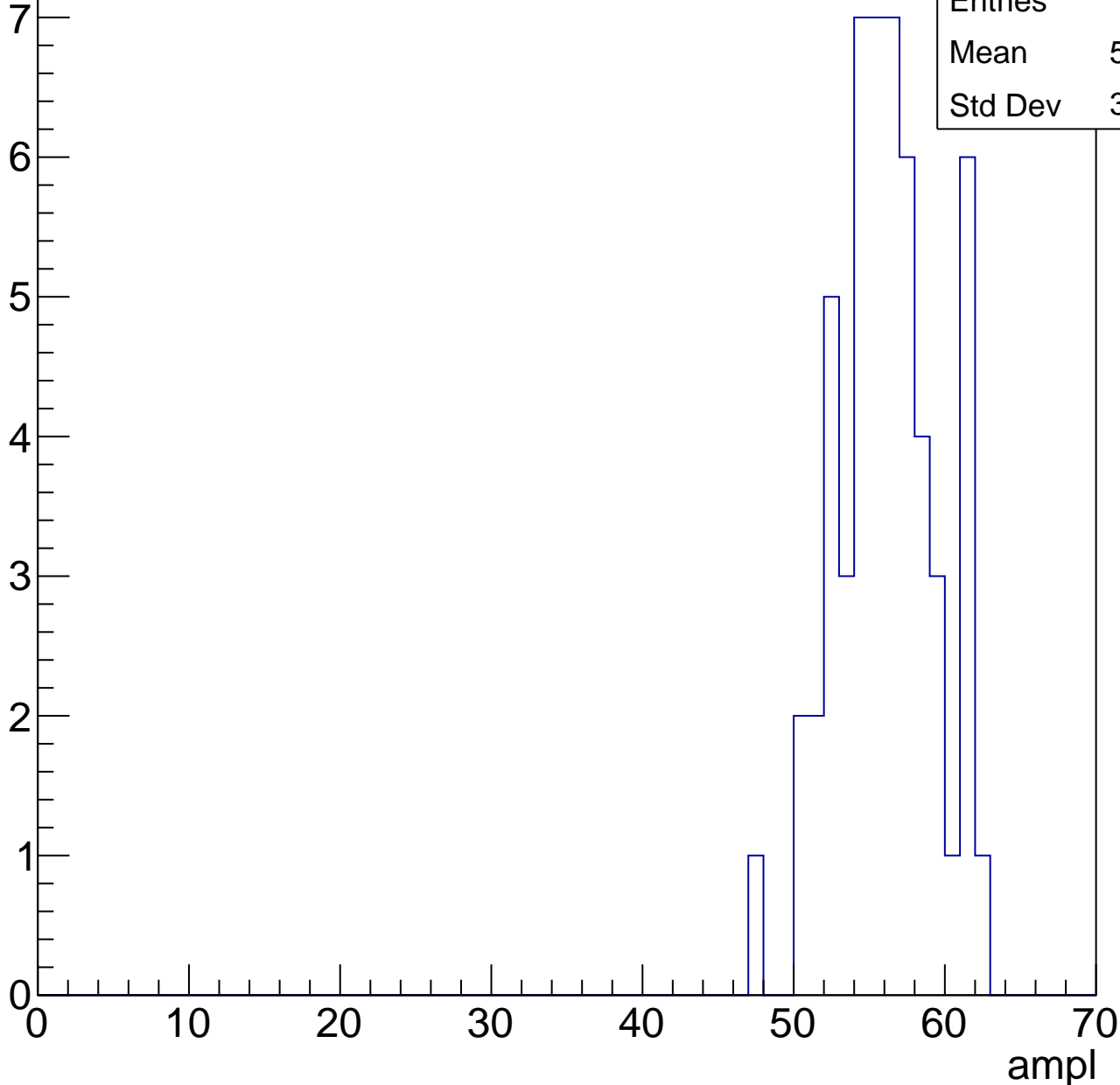


# B0L001S, U17-ch59, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	55.67
Std Dev	3.276



# B0L001S, U17-ch59, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

7

6

5

4

3

2

1

0

Entries

46

Mean

58.46

Std Dev

9.033

ampl

0

10

20

30

40

50

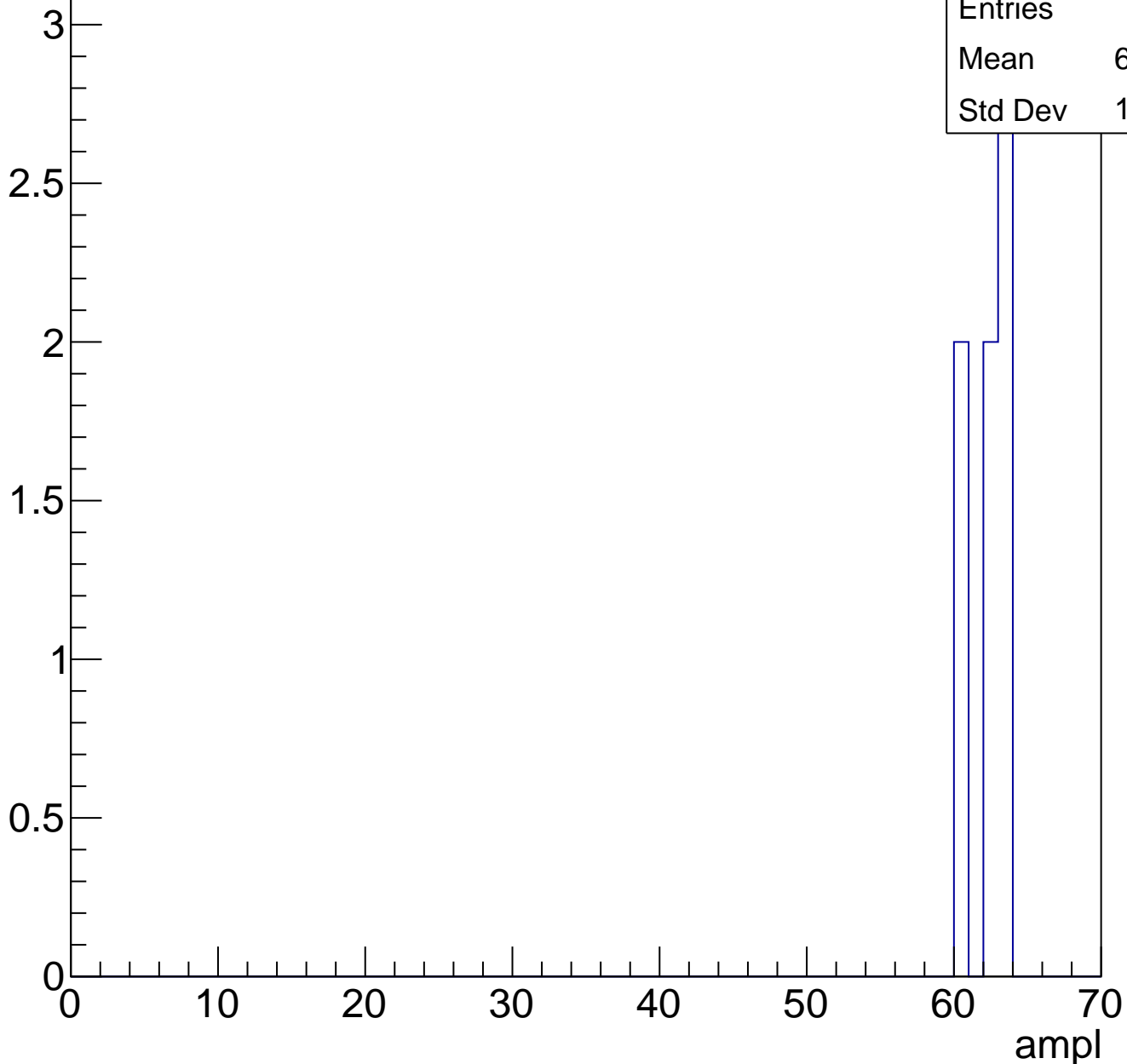
60

70

# B0L001S, U17-ch59, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch59, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U17-ch60, adc0

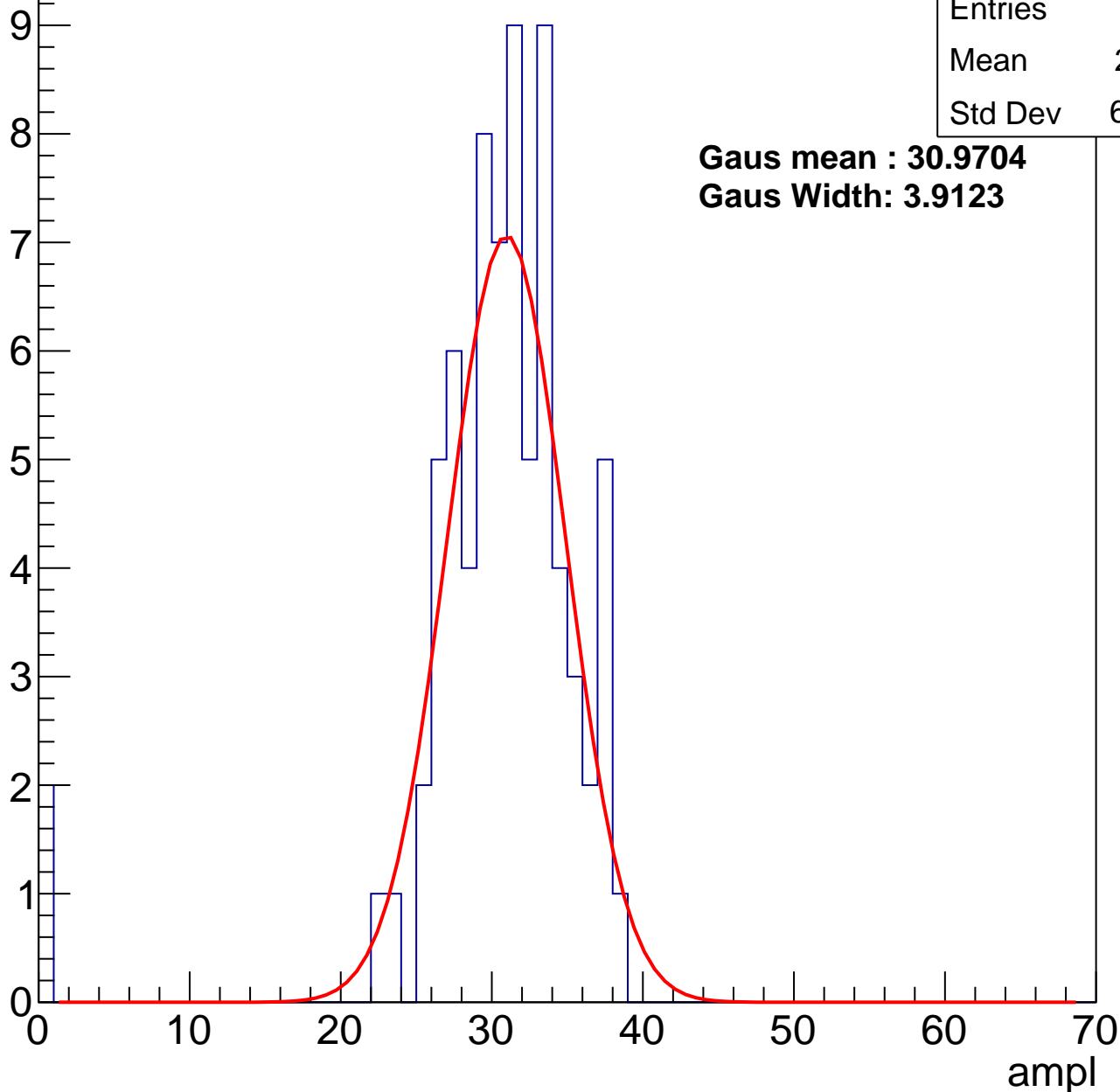
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	29.91
Std Dev	6.096

**Gaus mean : 30.9704**

**Gaus Width: 3.9123**



# B0L001S, U17-ch60, adc1

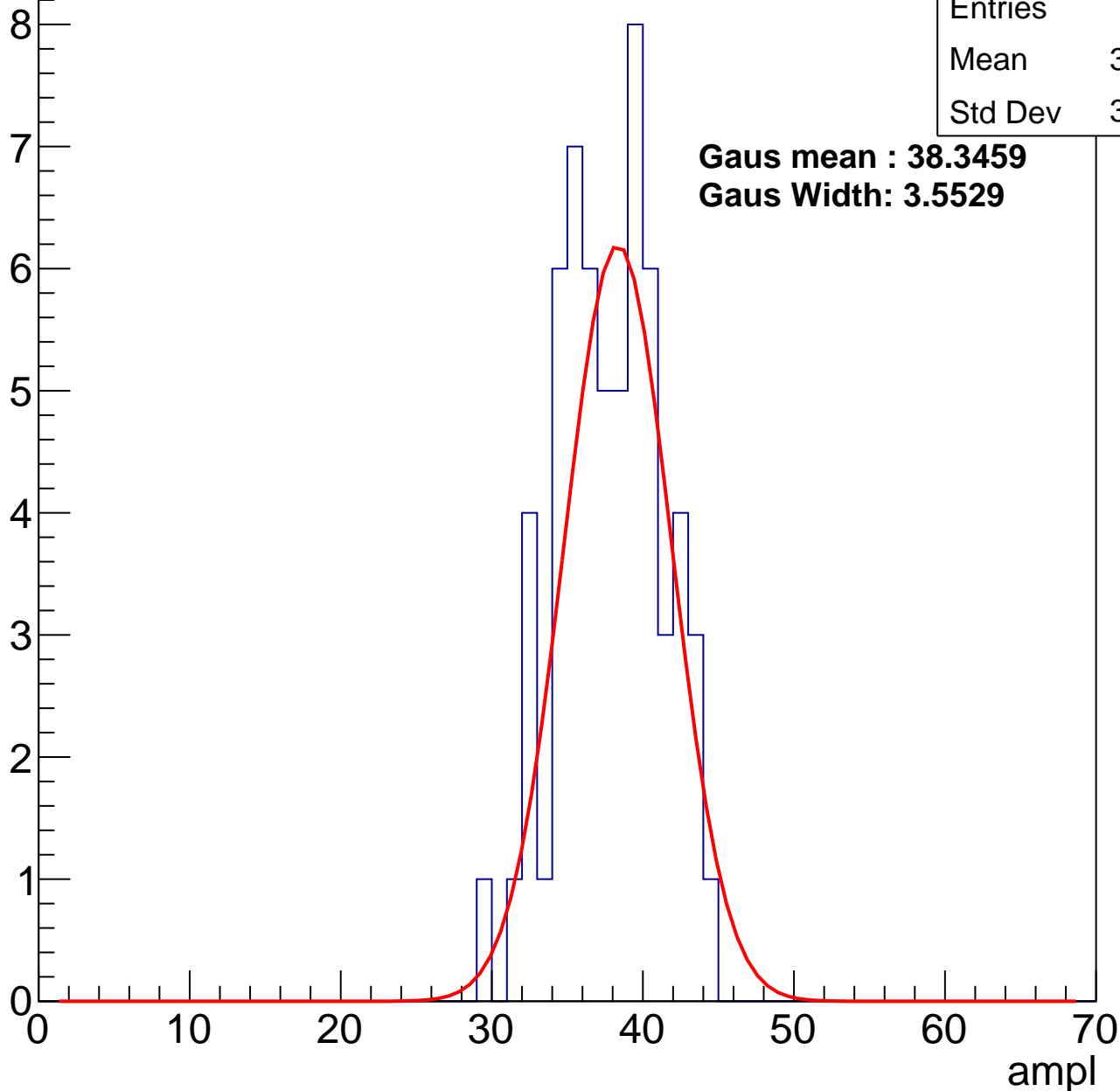
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	37.33
Std Dev	3.372

**Gaus mean : 38.3459**

**Gaus Width: 3.5529**



# B0L001S, U17-ch60, adc2

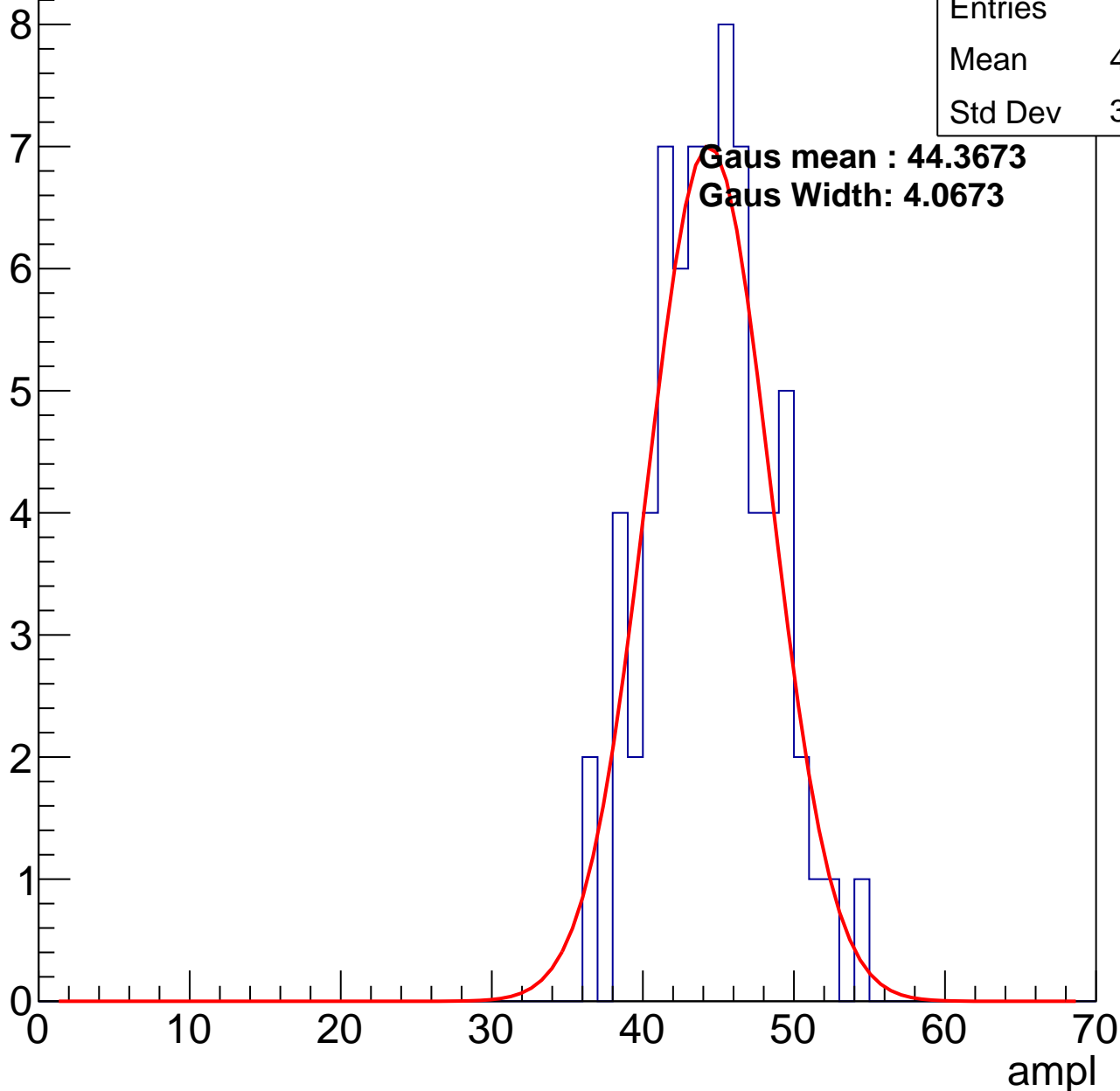
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	44.08
Std Dev	3.774

**Gaus mean : 44.3673**

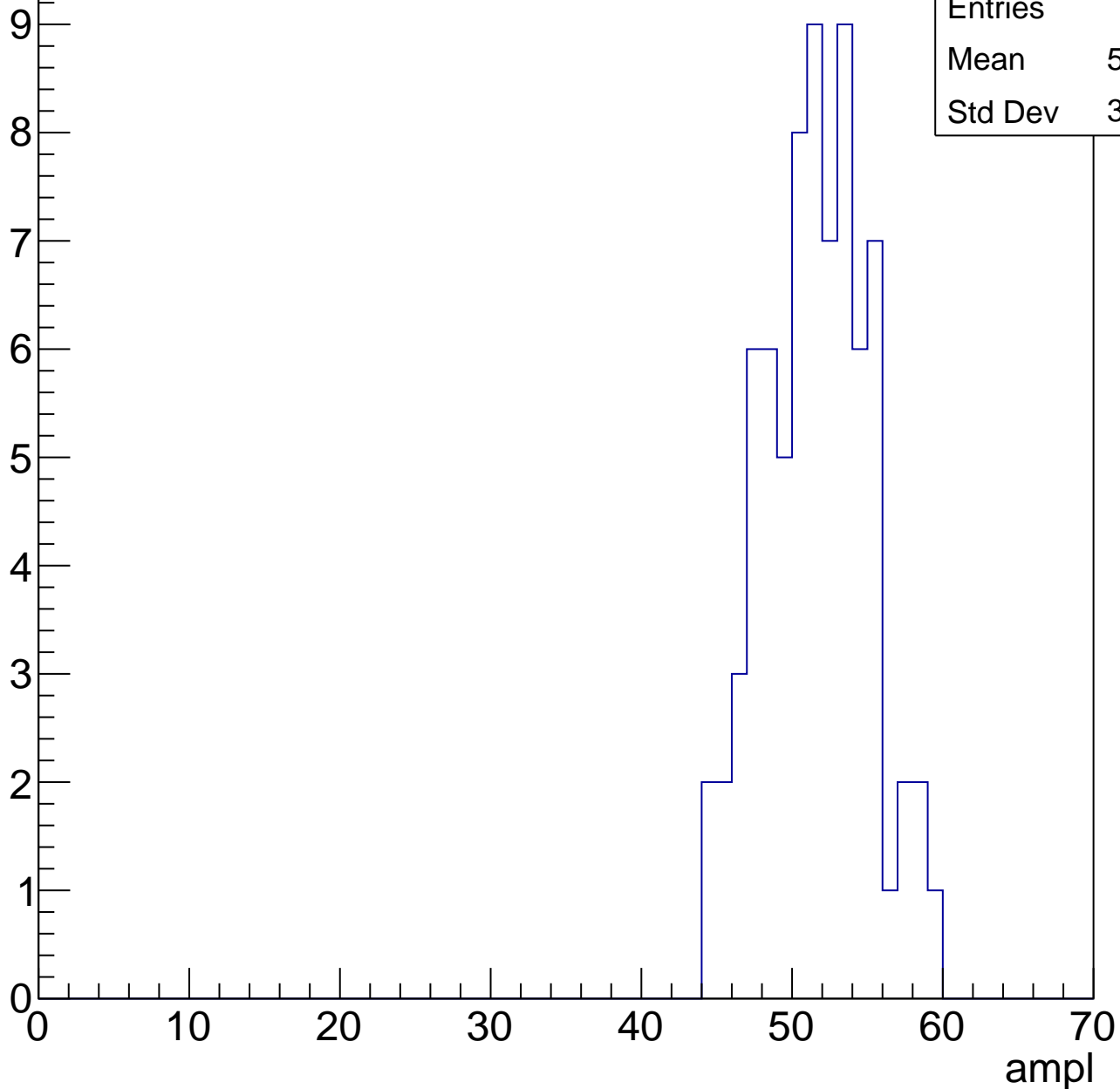
**Gaus Width: 4.0673**



# B0L001S, U17-ch60, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



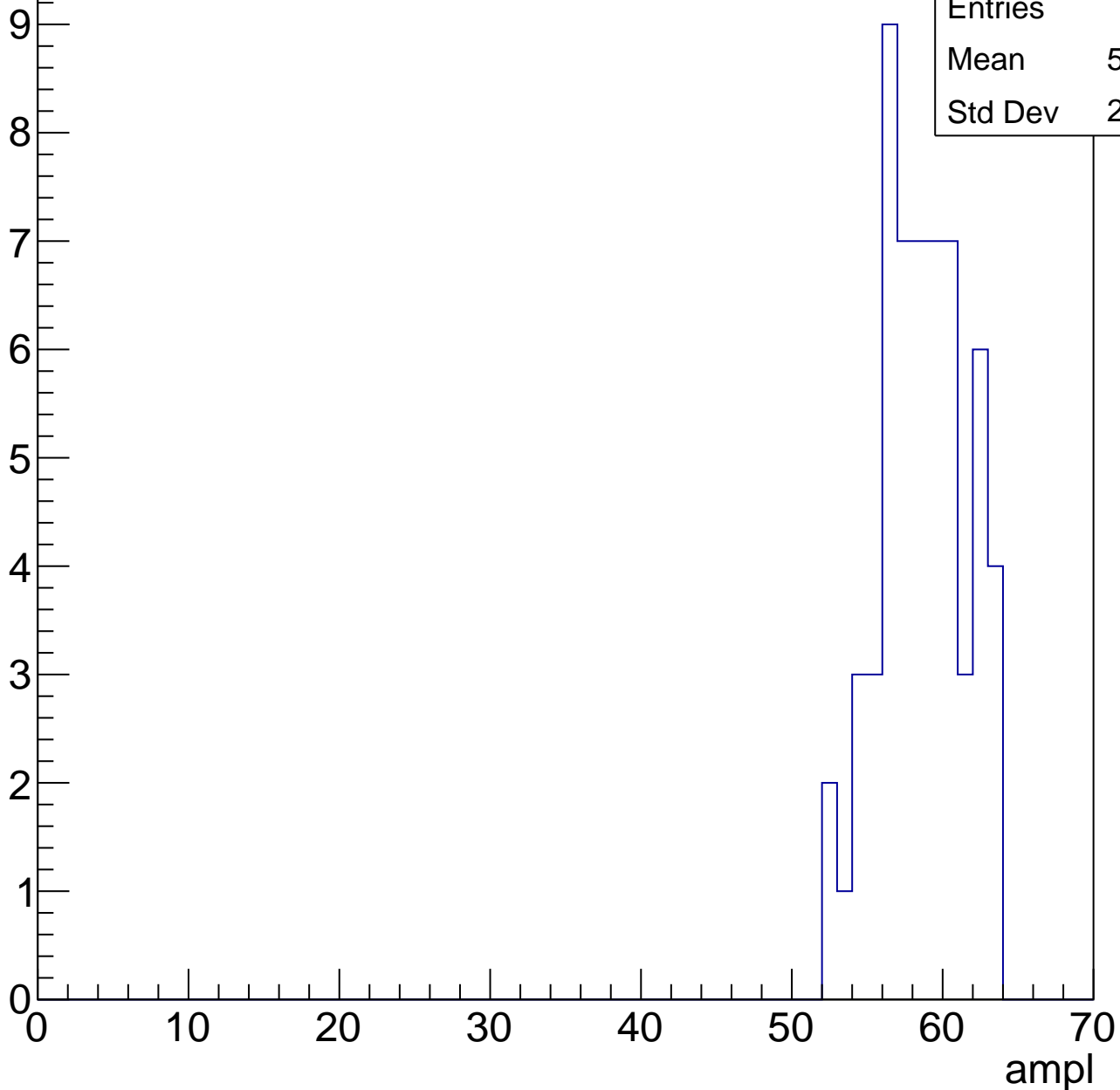
Entries	76
Mean	51.12
Std Dev	3.422

# B0L001S, U17-ch60, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	58.19
Std Dev	2.825

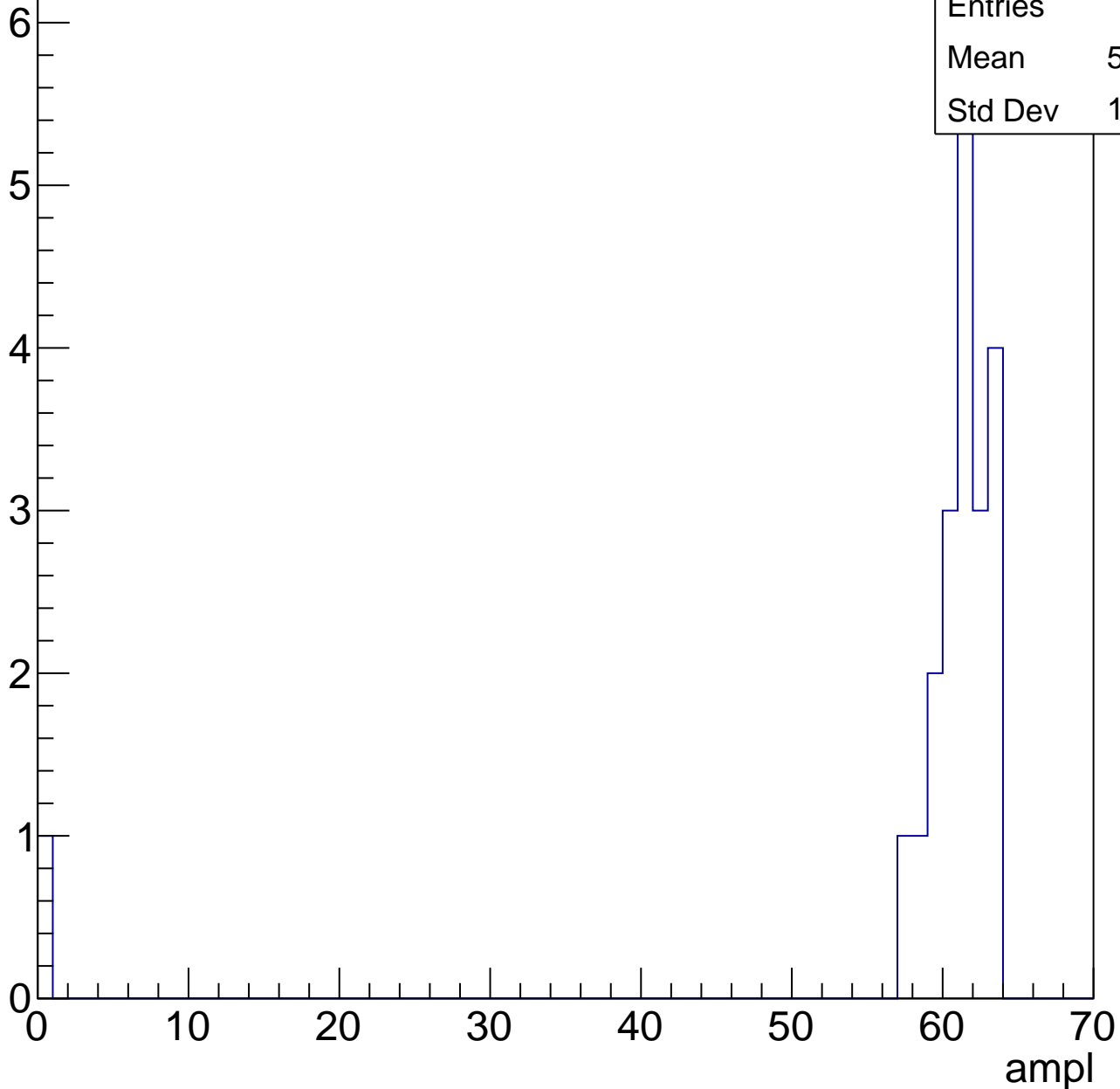


# B0L001S, U17-ch60, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	21
Mean	57.95
Std Dev	13.06



# B0L001S, U17-ch60, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch60, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U17-ch61, adc0

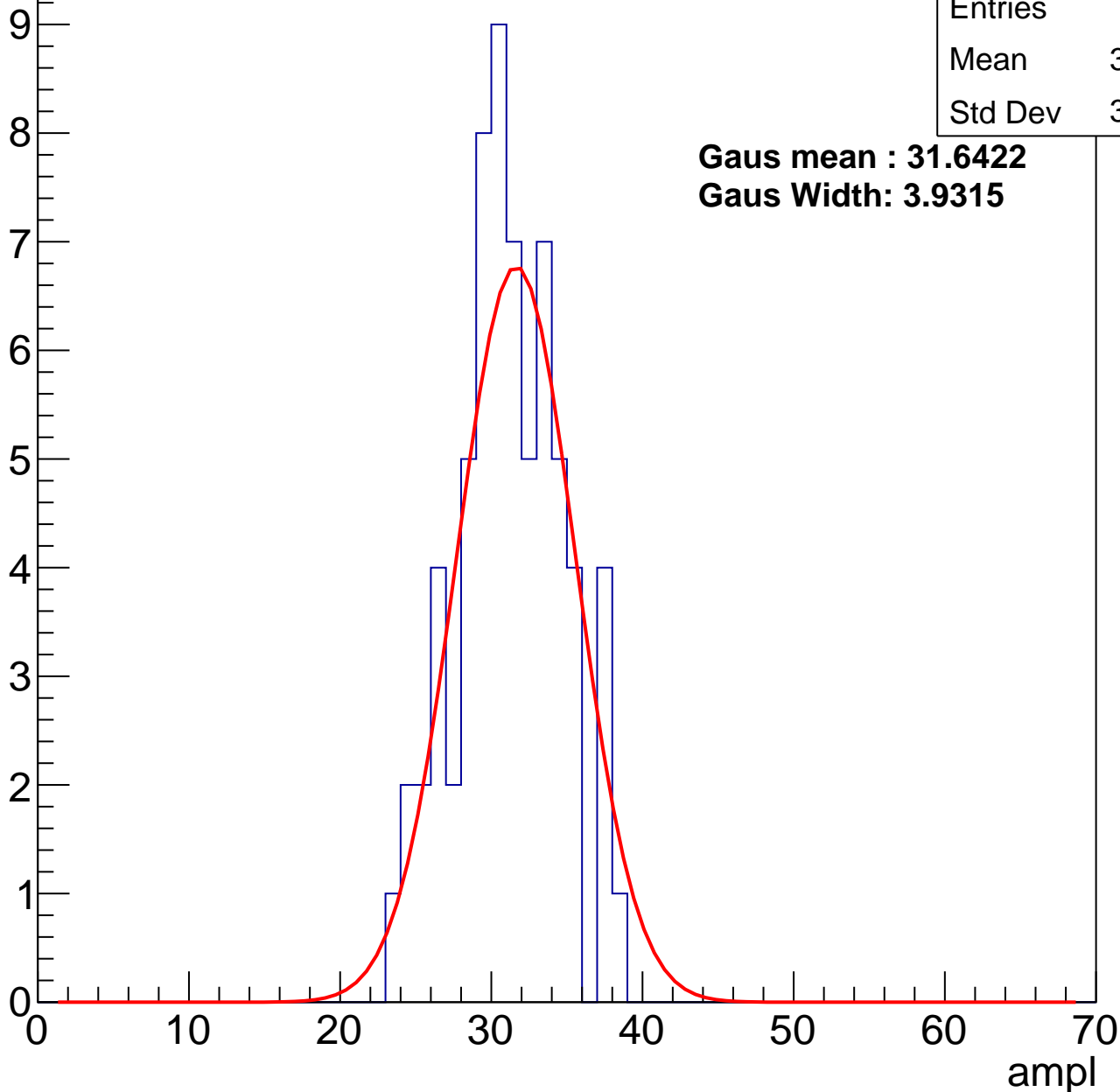
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	30.68
Std Dev	3.438

**Gaus mean : 31.6422**

**Gaus Width: 3.9315**



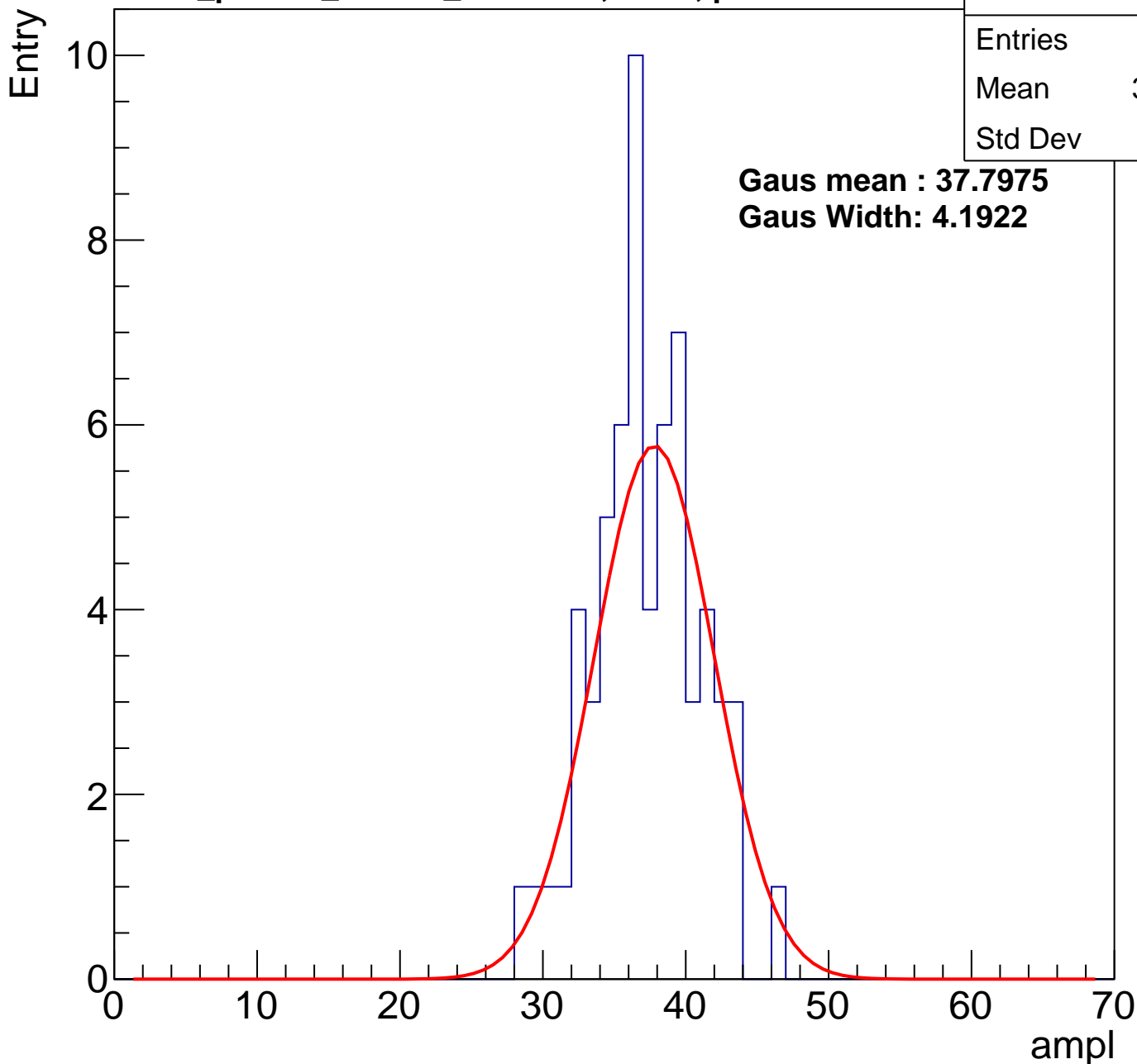
# B0L001S, U17-ch61, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	63
Mean	36.81
Std Dev	3.66

**Gaus mean : 37.7975**

**Gaus Width: 4.1922**



# B0L001S, U17-ch61, adc2

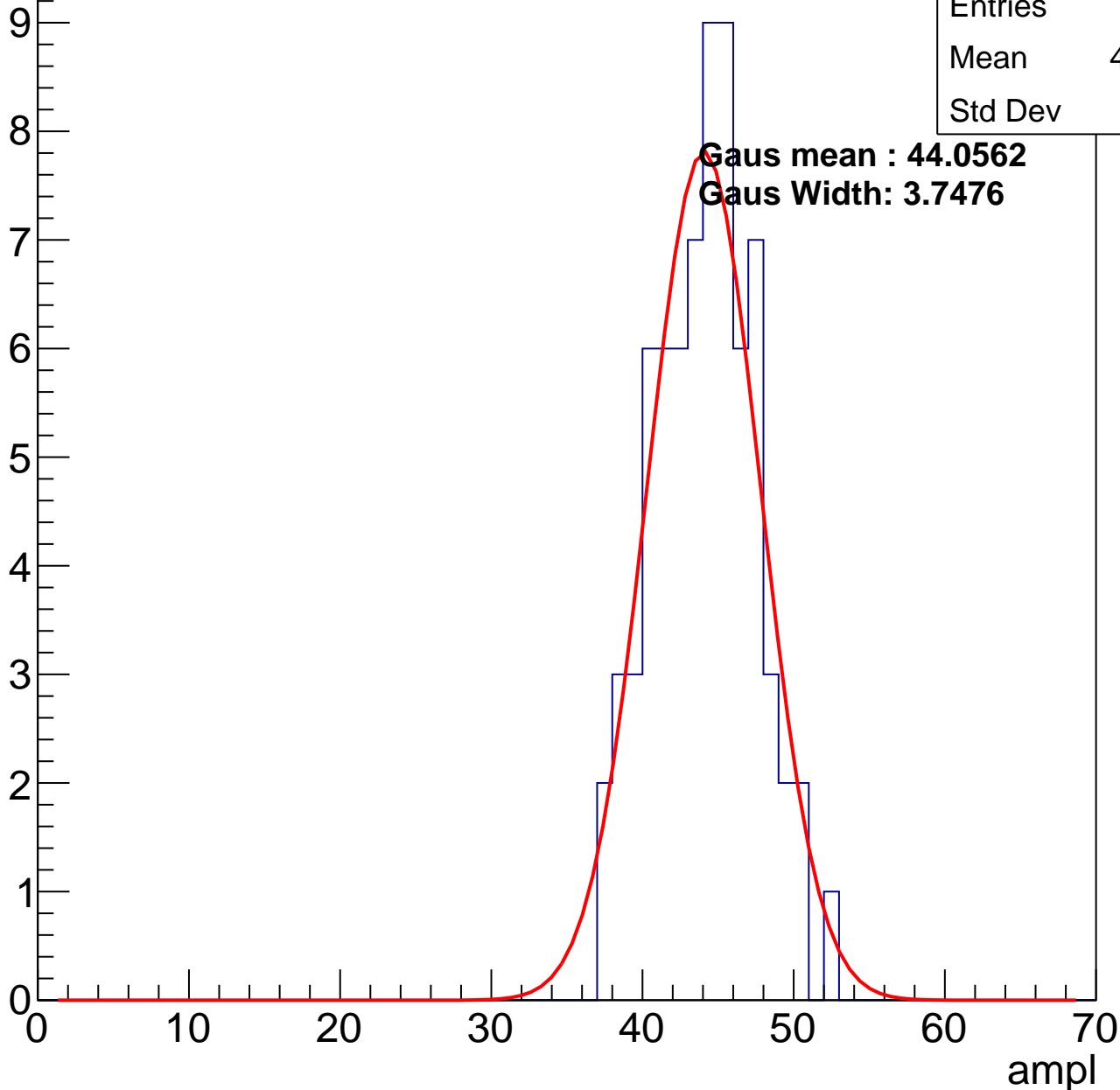
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	43.67
Std Dev	3.3

**Gaus mean : 44.0562**

**Gaus Width: 3.7476**

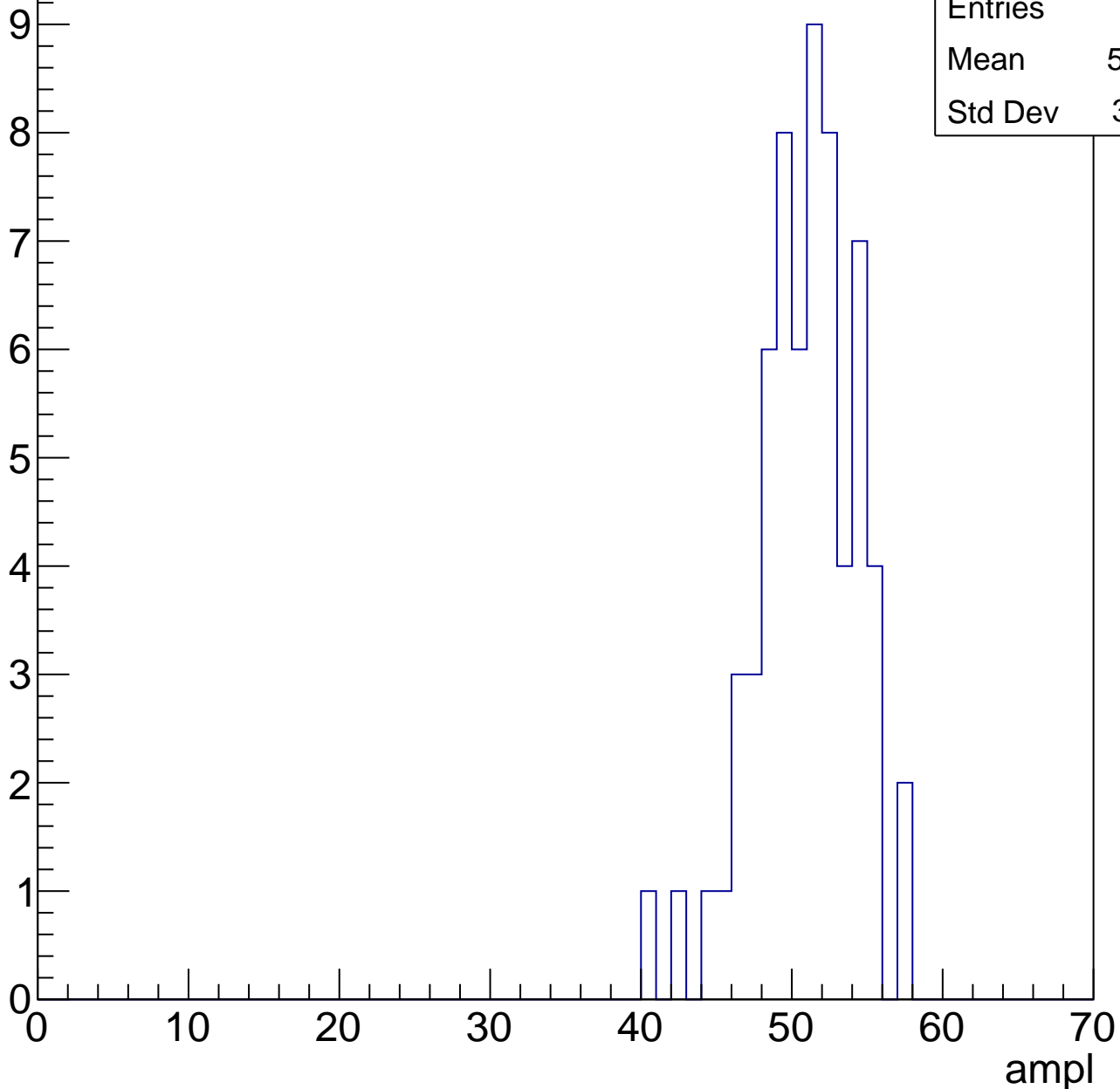


# B0L001S, U17-ch61, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	50.45
Std Dev	3.321

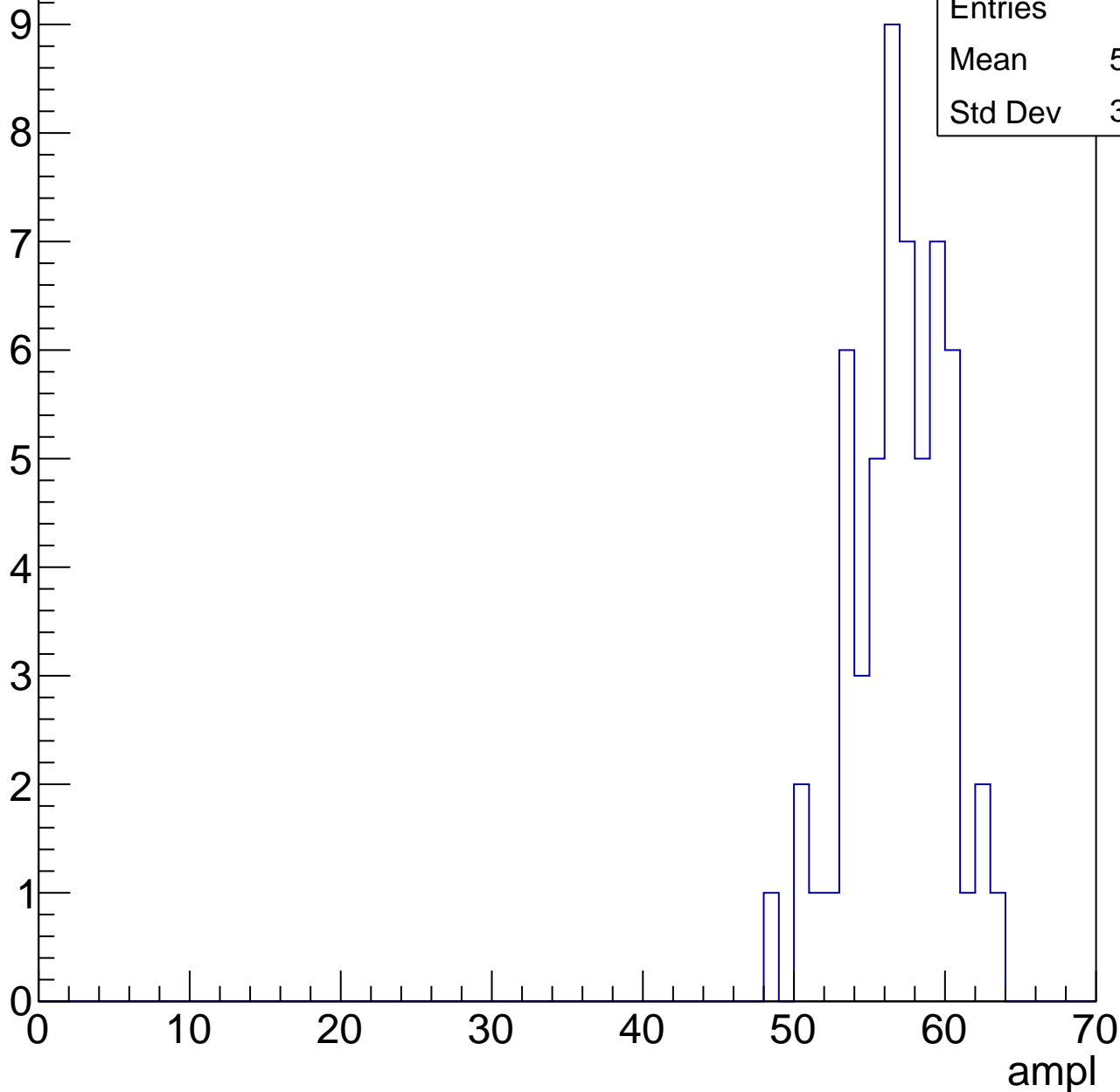


# B0L001S, U17-ch61, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	56.49
Std Dev	3.152

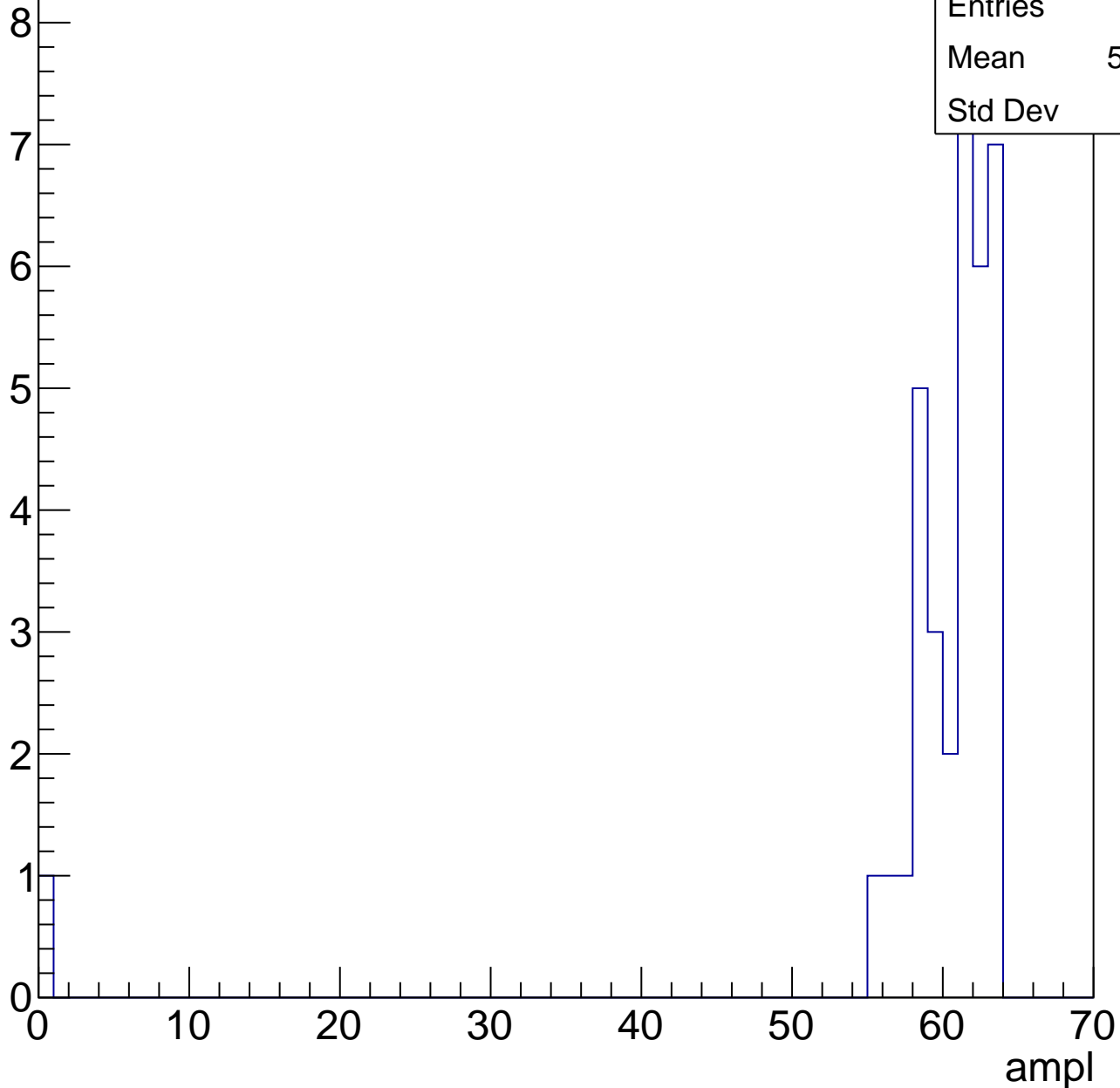


# B0L001S, U17-ch61, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	35
Mean	58.74
Std Dev	10.3



# B0L001S, U17-ch61, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

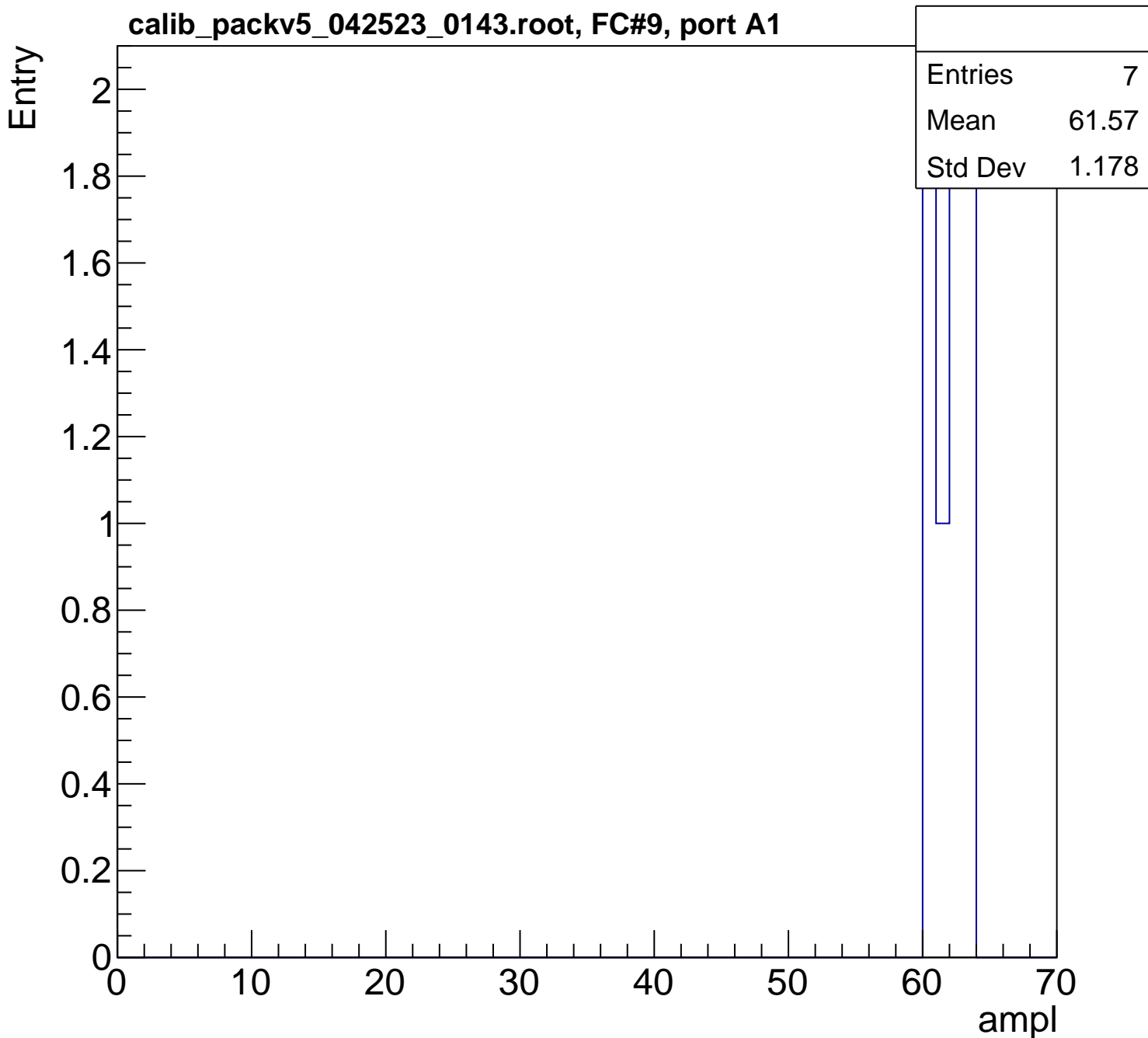
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	7
Mean	61.57
Std Dev	1.178

0 10 20 30 40 50 60 70

ampl





# B0L001S, U17-ch61, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U17-ch62, adc0

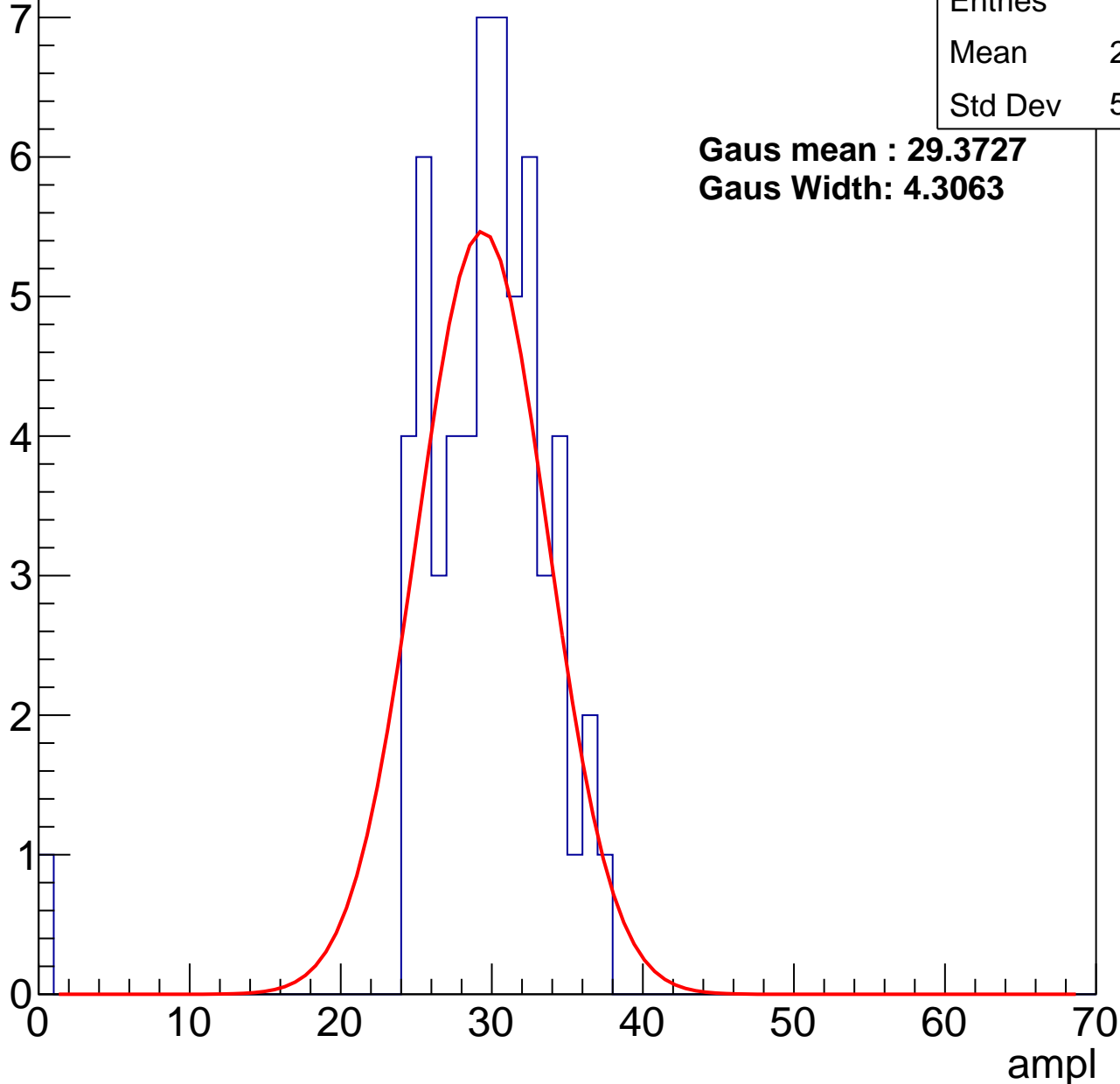
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	29.02
Std Dev	5.104

**Gaus mean : 29.3727**

**Gaus Width: 4.3063**



# B0L001S, U17-ch62, adc1

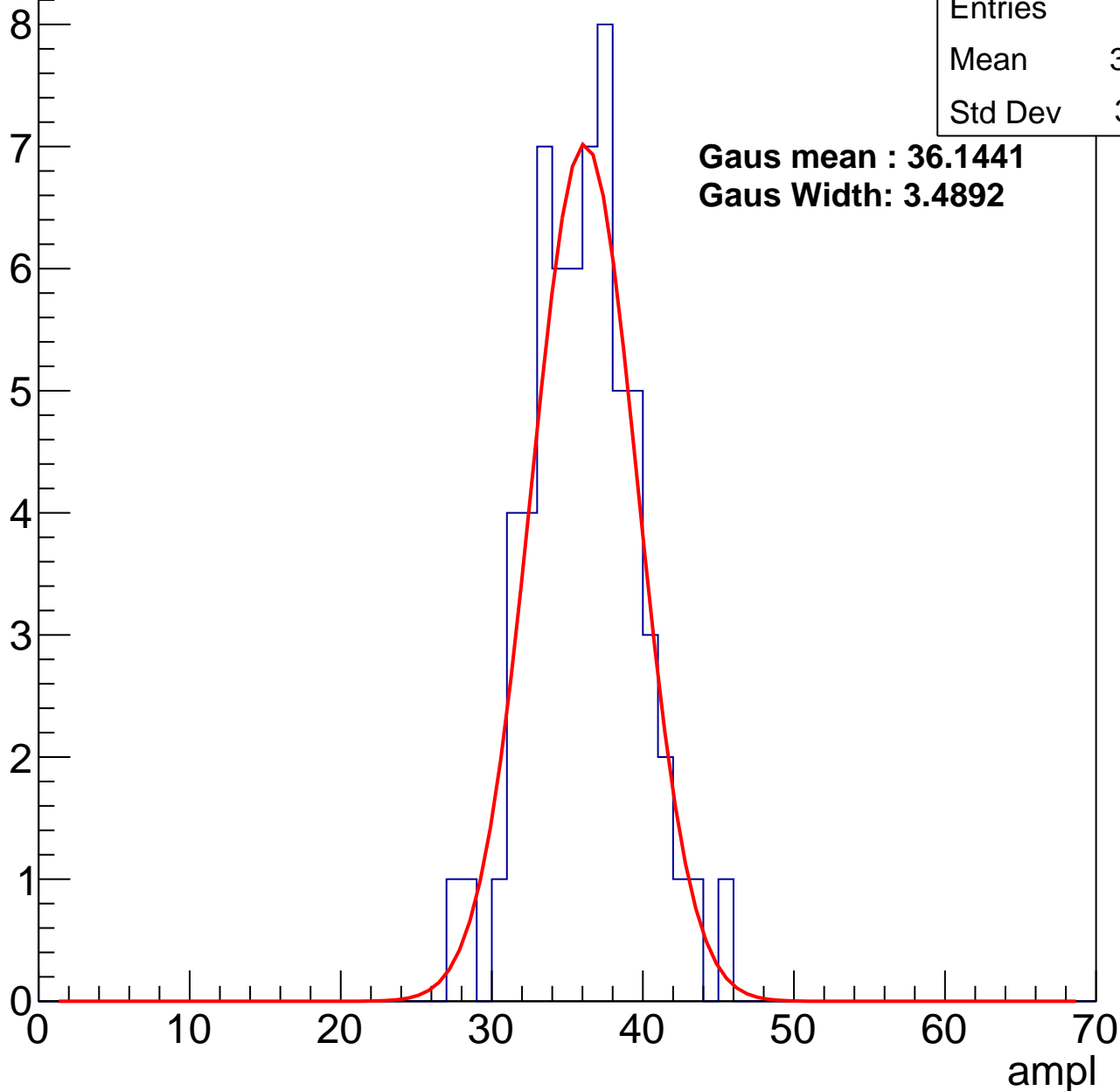
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	35.67
Std Dev	3.491

**Gaus mean : 36.1441**

**Gaus Width: 3.4892**



# B0L001S, U17-ch62, adc2

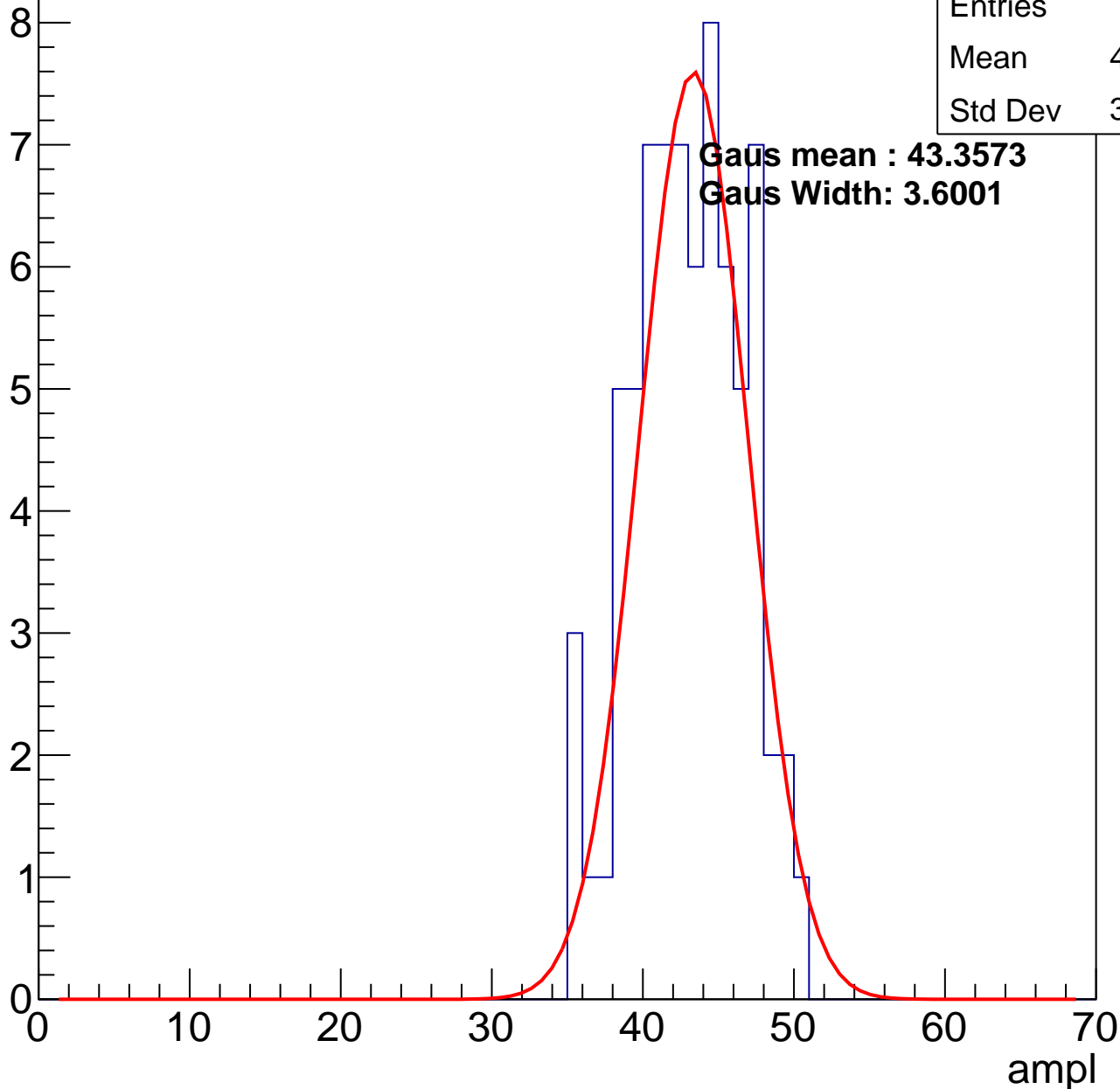
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	42.56
Std Dev	3.562

**Gaus mean : 43.3573**

**Gaus Width: 3.6001**

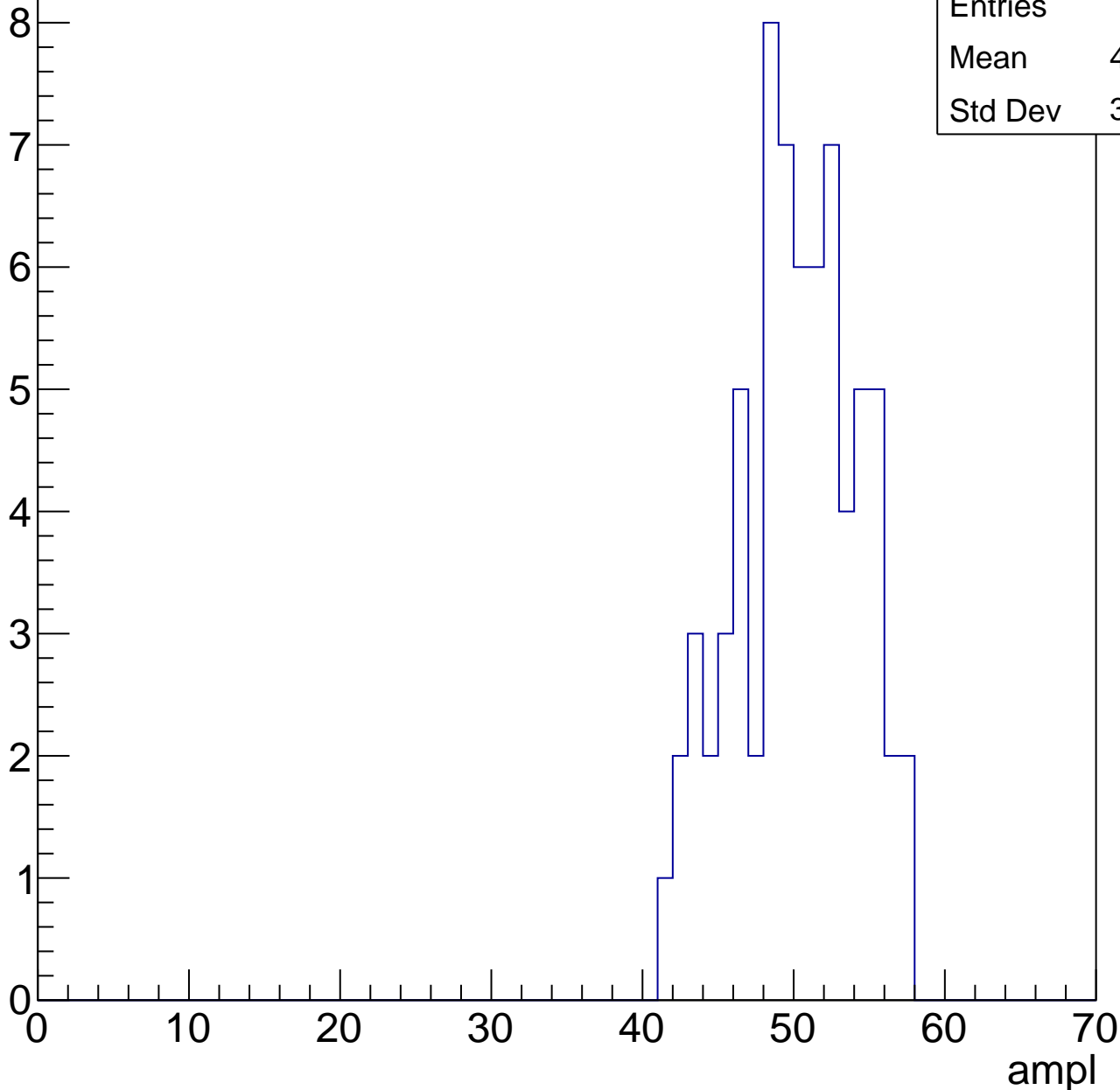


# B0L001S, U17-ch62, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	49.73
Std Dev	3.928

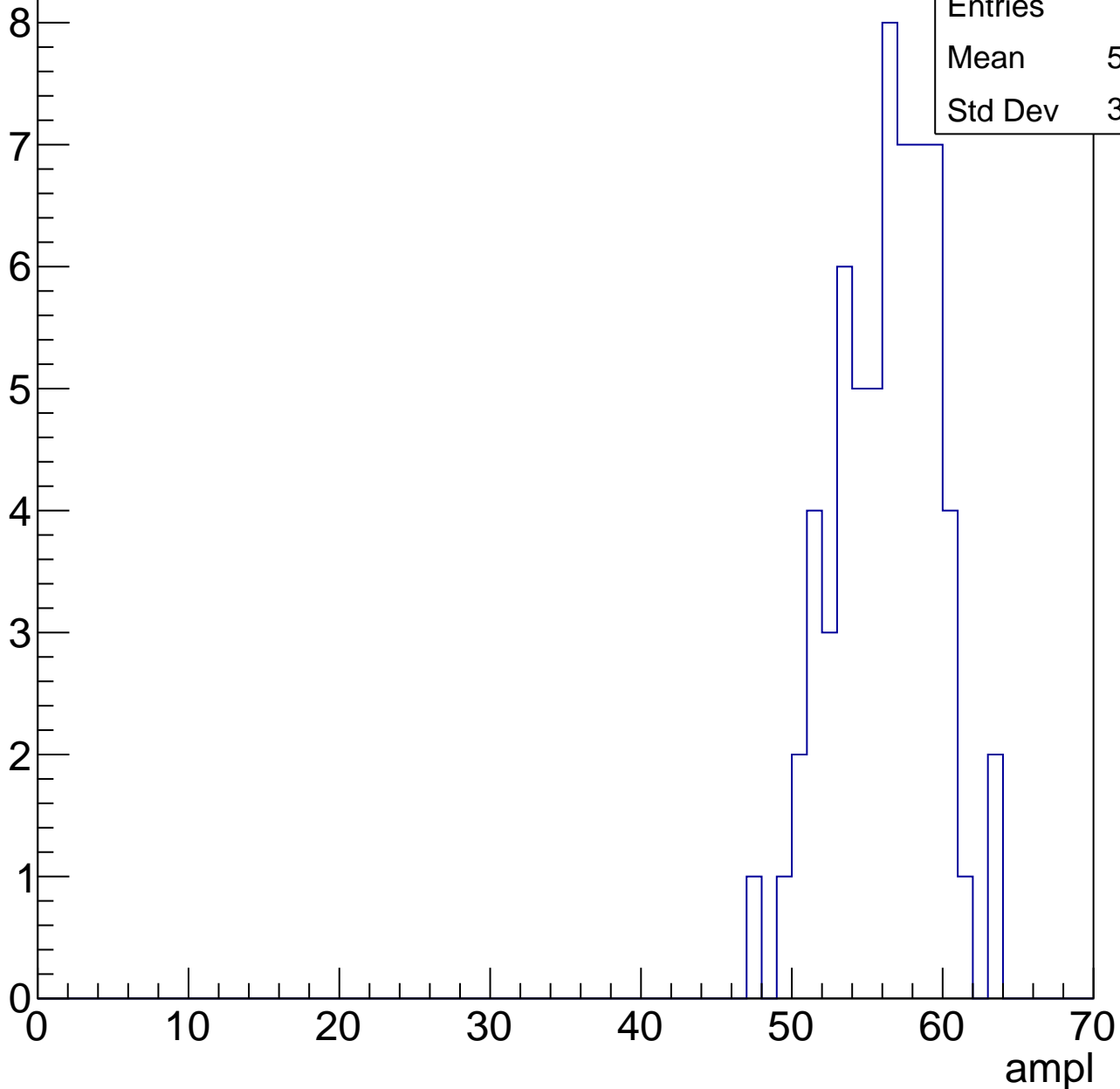


# B0L001S, U17-ch62, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	55.75
Std Dev	3.357

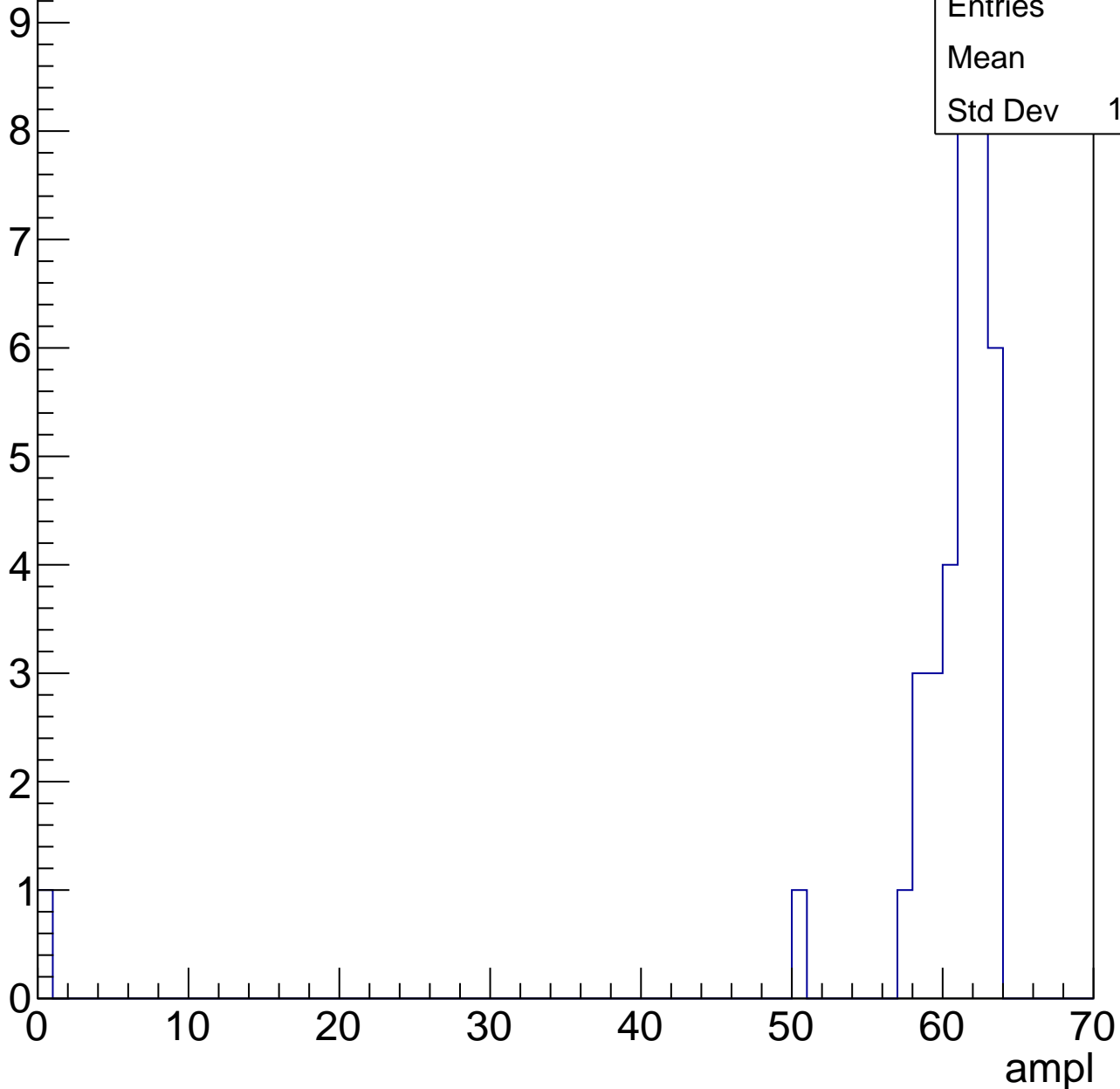


# B0L001S, U17-ch62, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	37
Mean	59
Std Dev	10.12



# B0L001S, U17-ch62, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	61.6
Std Dev	1.356

ampl

0 10 20 30 40 50 60 70



# B0L001S, U17-ch62, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U17-ch63, adc0

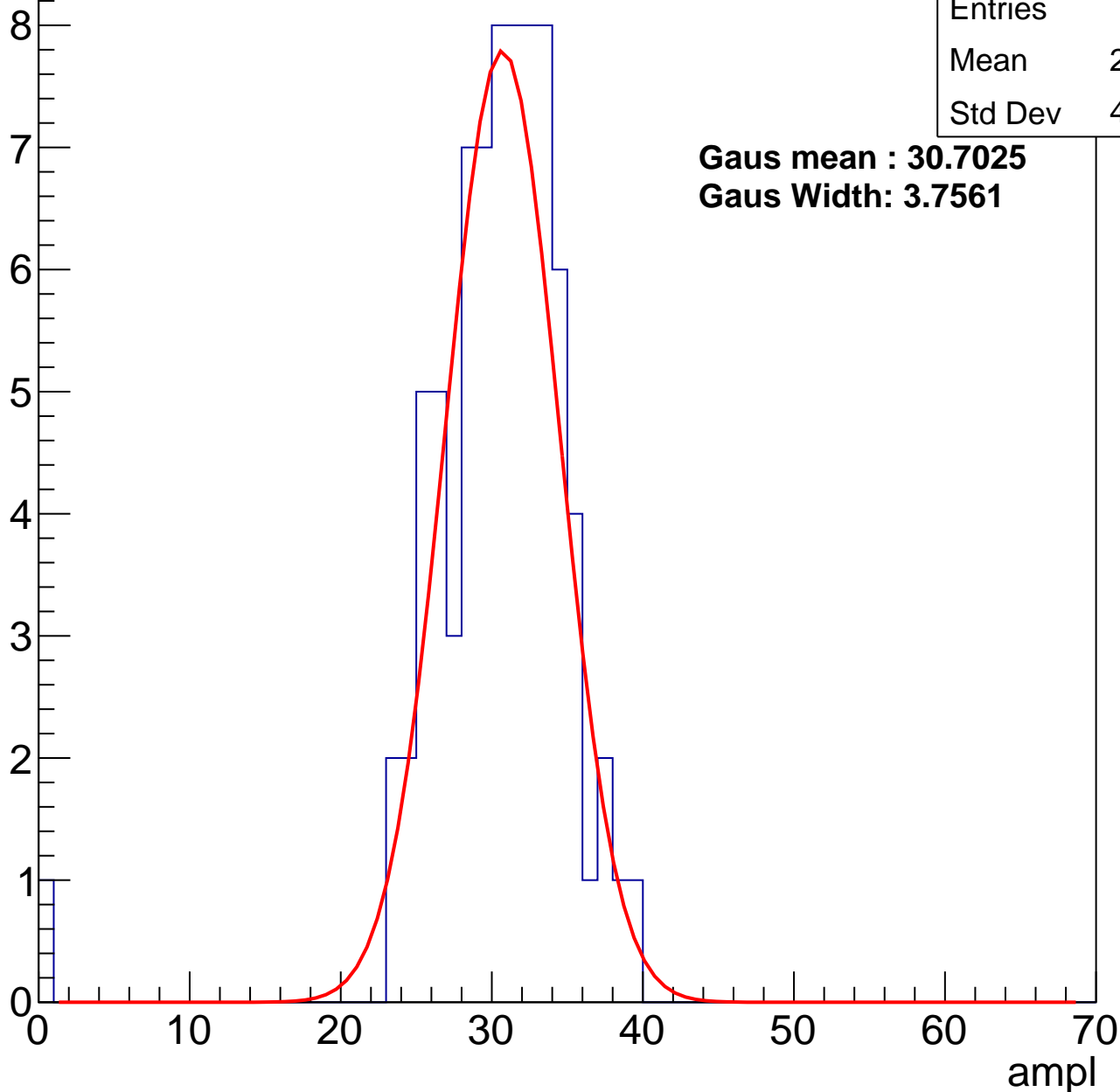
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	79
Mean	29.97
Std Dev	4.935

**Gaus mean : 30.7025**

**Gaus Width: 3.7561**



# B0L001S, U17-ch63, adc1

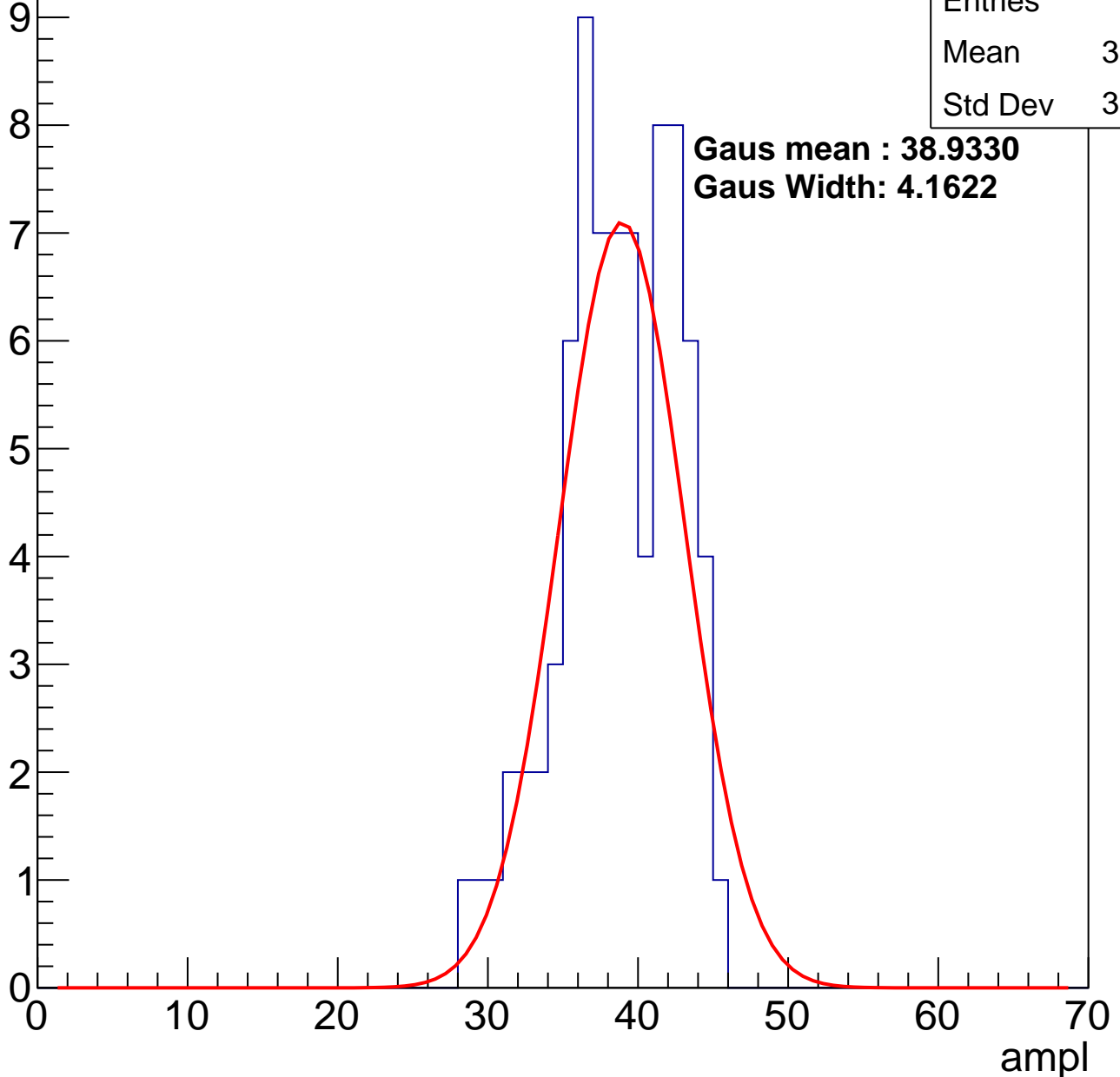
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	79
Mean	38.18
Std Dev	3.854

**Gaus mean : 38.9330**

**Gaus Width: 4.1622**



# B0L001S, U17-ch63, adc2

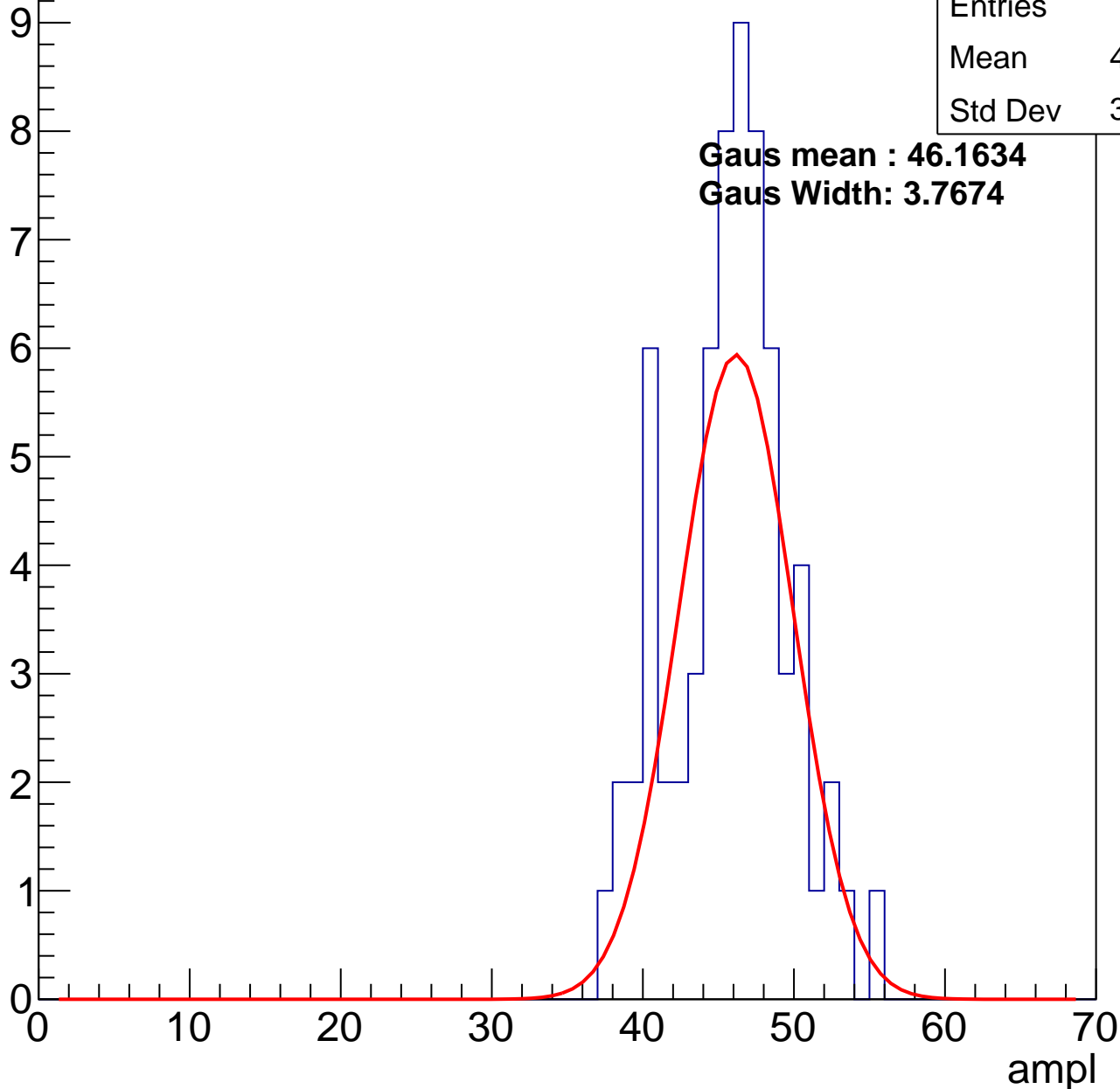
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	45.34
Std Dev	3.834

**Gaus mean : 46.1634**

**Gaus Width: 3.7674**

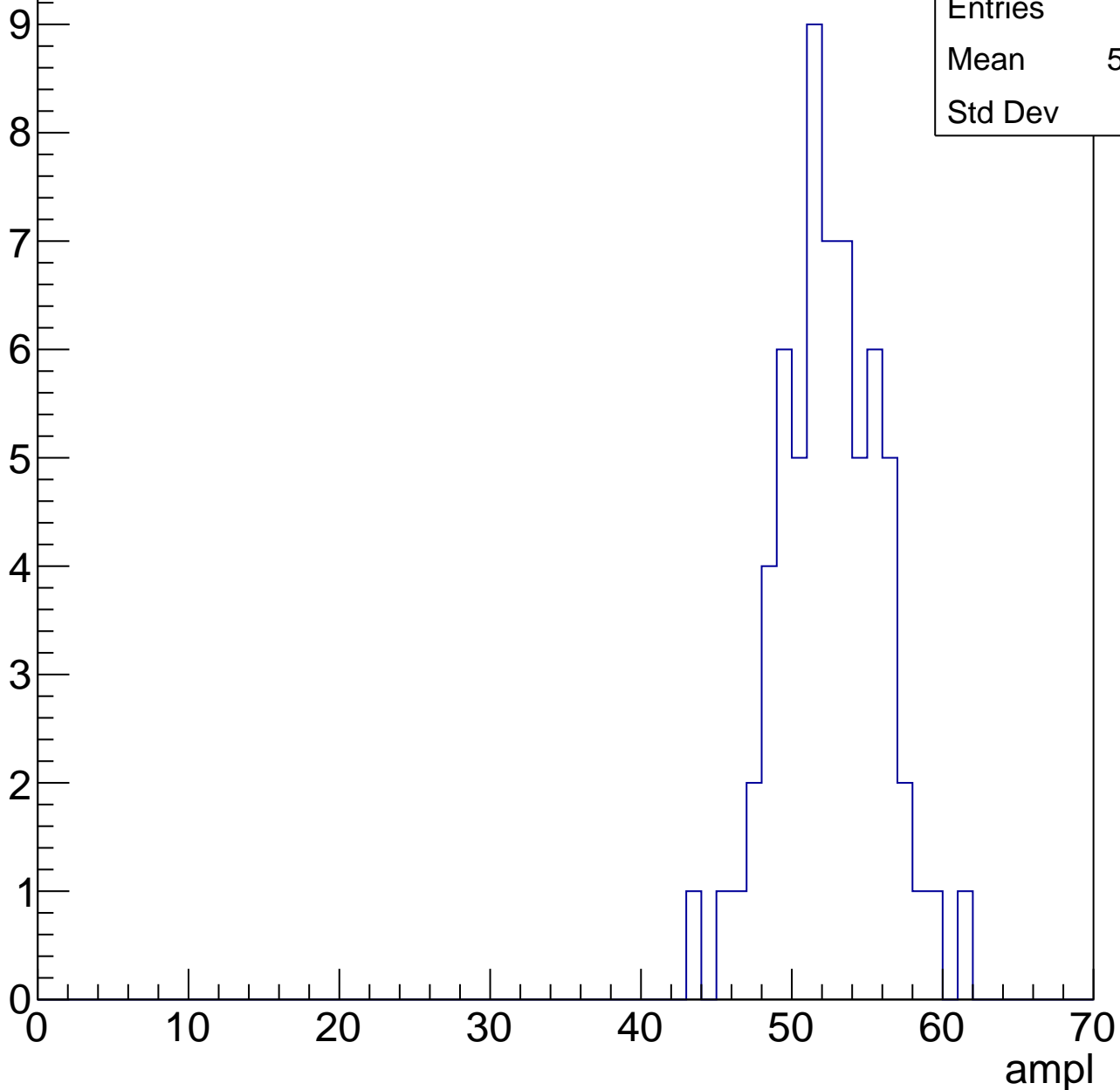


# B0L001S, U17-ch63, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	52.03
Std Dev	3.4

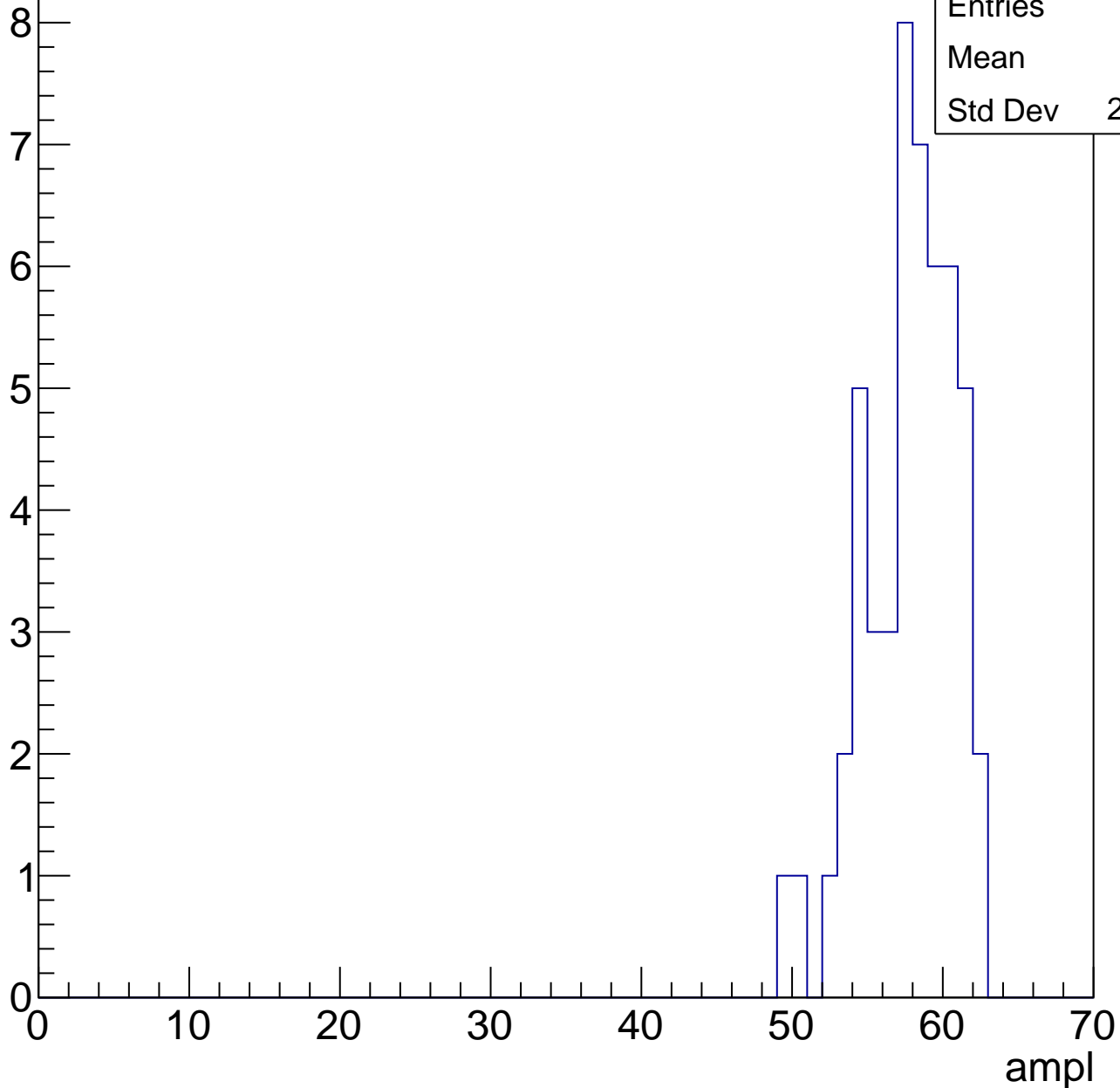


# B0L001S, U17-ch63, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	50
Mean	57.3
Std Dev	2.968

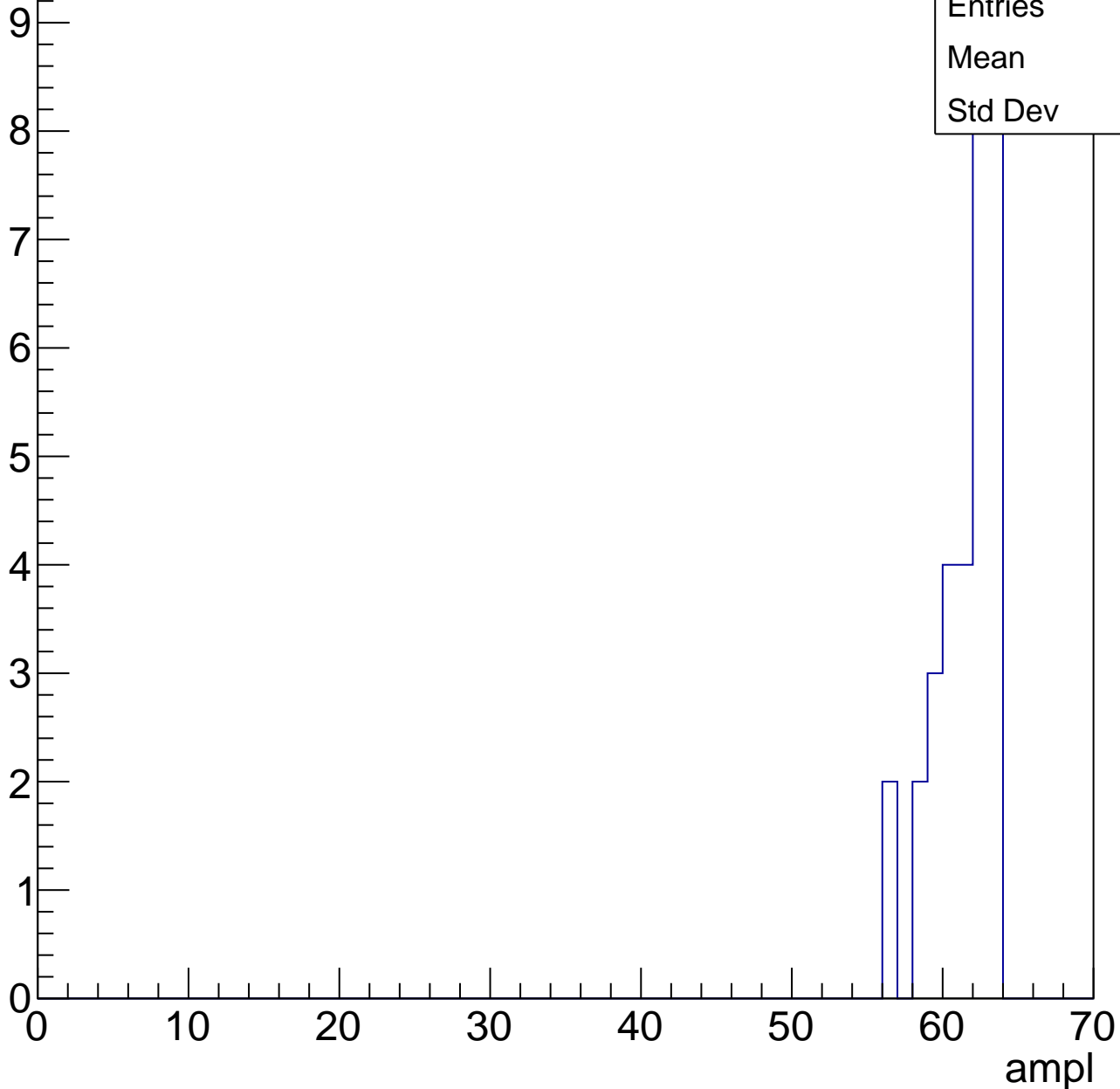


# B0L001S, U17-ch63, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	32
Mean	61
Std Dev	2



# B0L001S, U17-ch63, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch63, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U17-ch64, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	75
Mean	28.75
Std Dev	6.04

**Gaus mean : 30.5455**

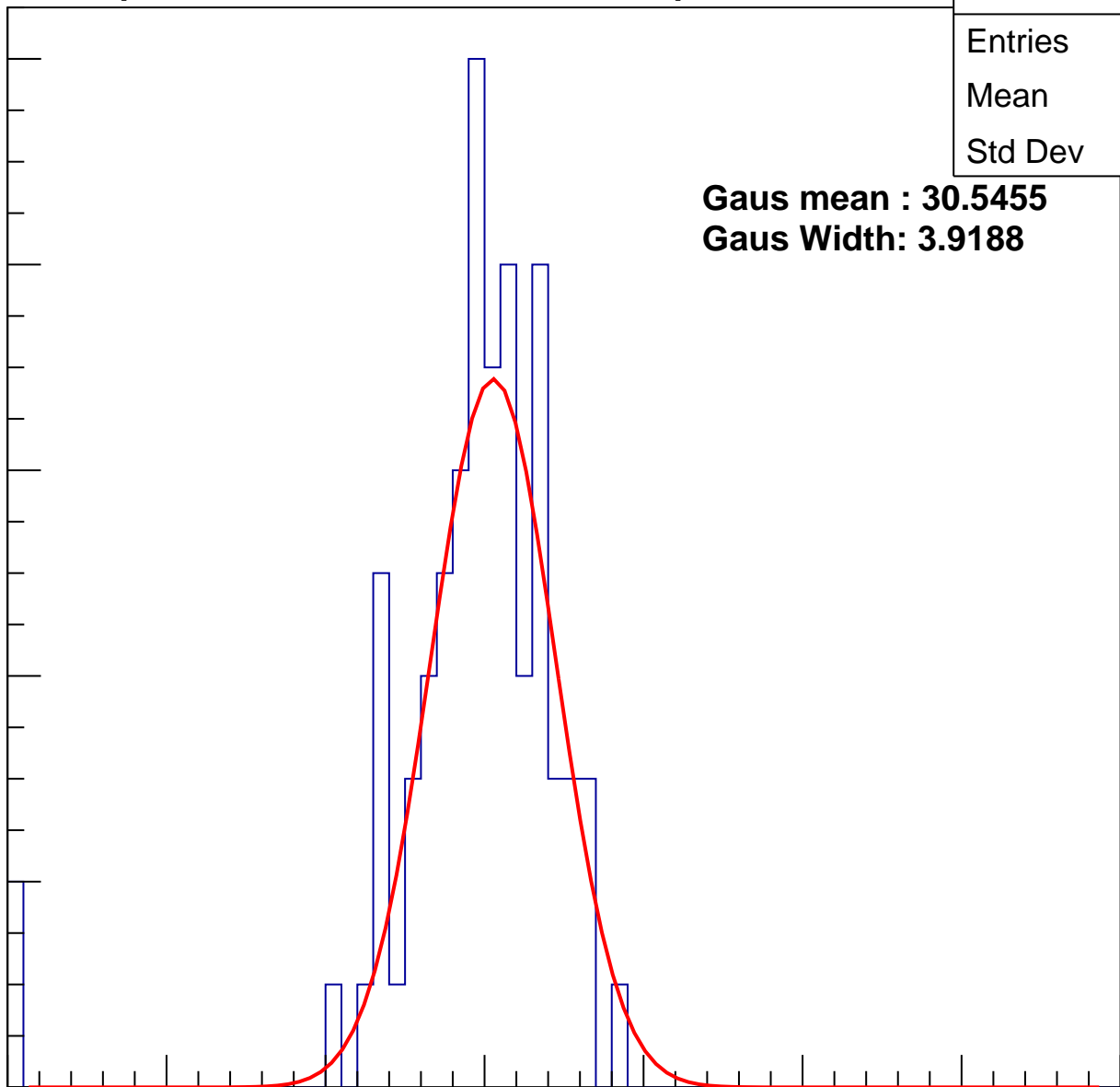
**Gaus Width: 3.9188**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U17-ch64, adc1

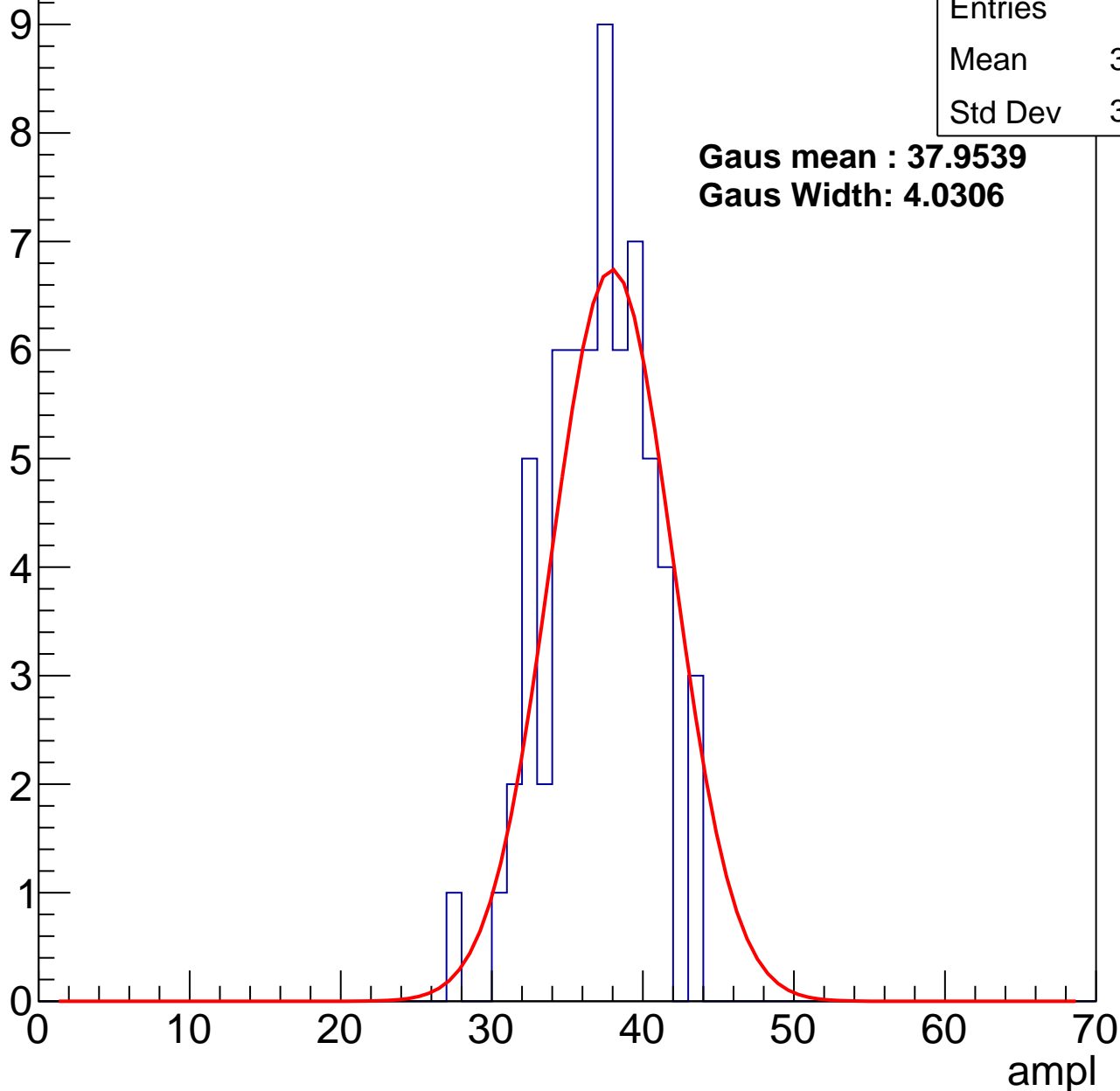
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	36.54
Std Dev	3.333

**Gaus mean : 37.9539**

**Gaus Width: 4.0306**



# B0L001S, U17-ch64, adc2

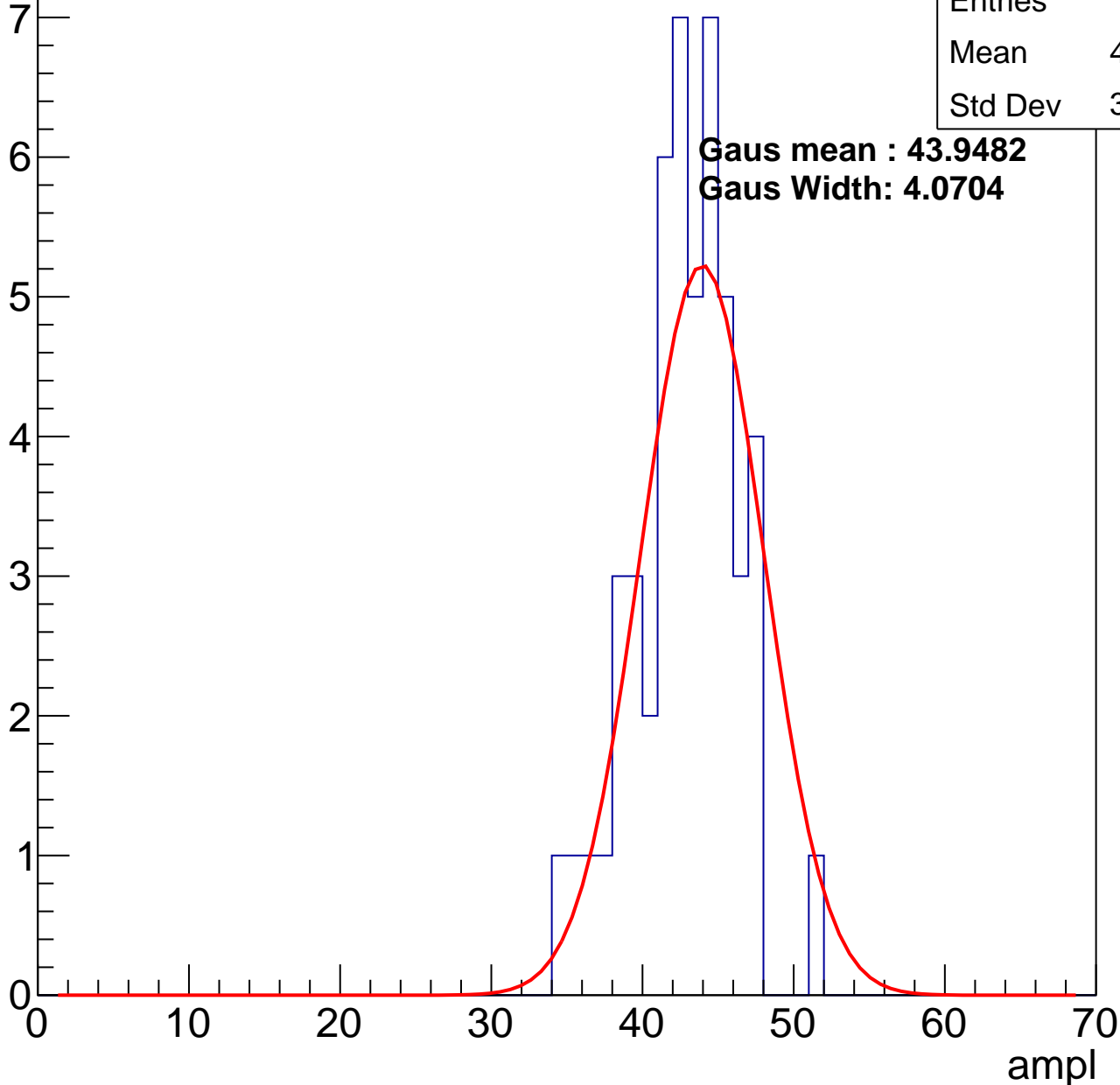
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	50
Mean	42.36
Std Dev	3.357

**Gaus mean : 43.9482**

**Gaus Width: 4.0704**

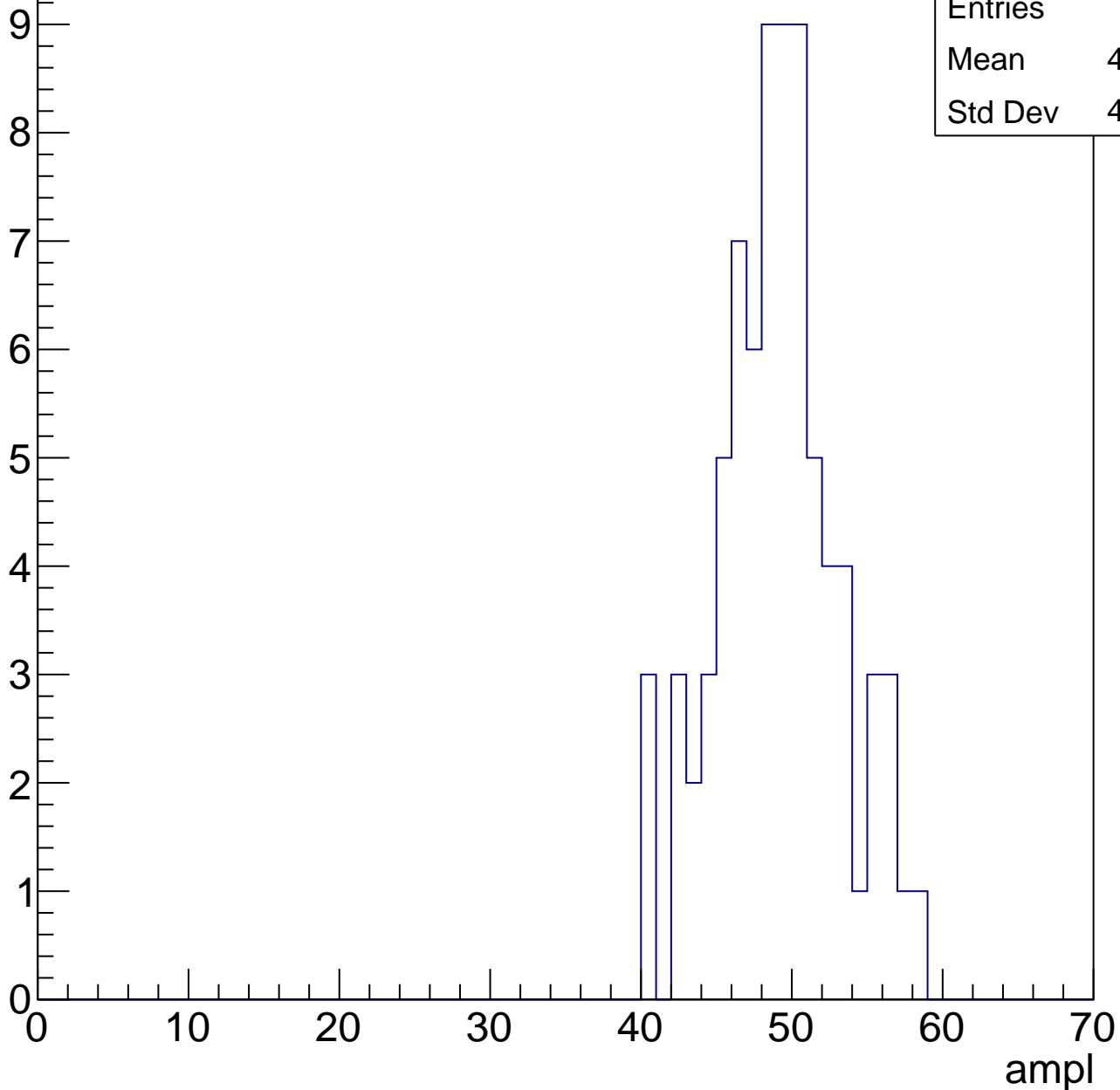


# B0L001S, U17-ch64, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

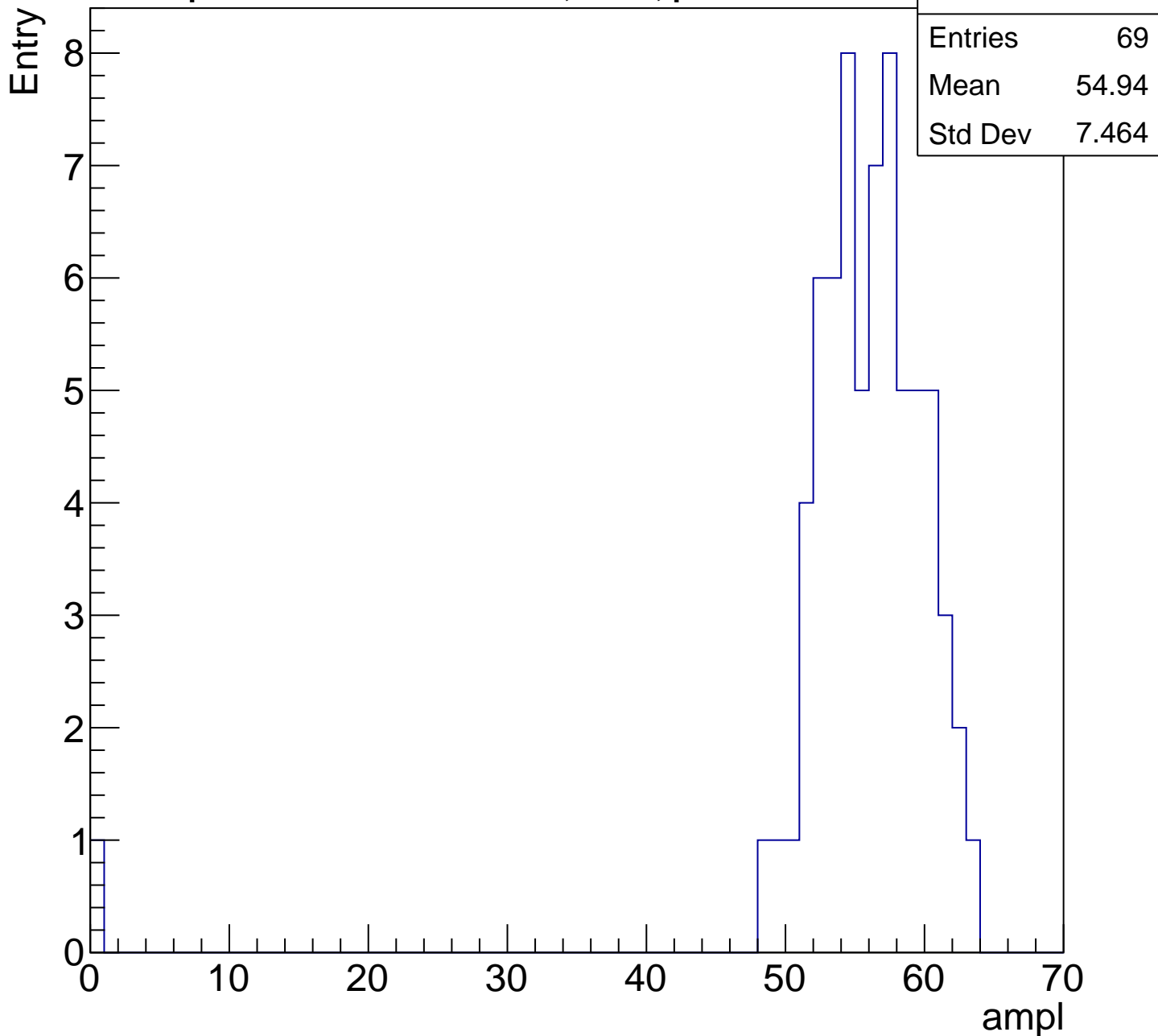
Entry

Entries	78
Mean	48.63
Std Dev	4.013



# B0L001S, U17-ch64, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

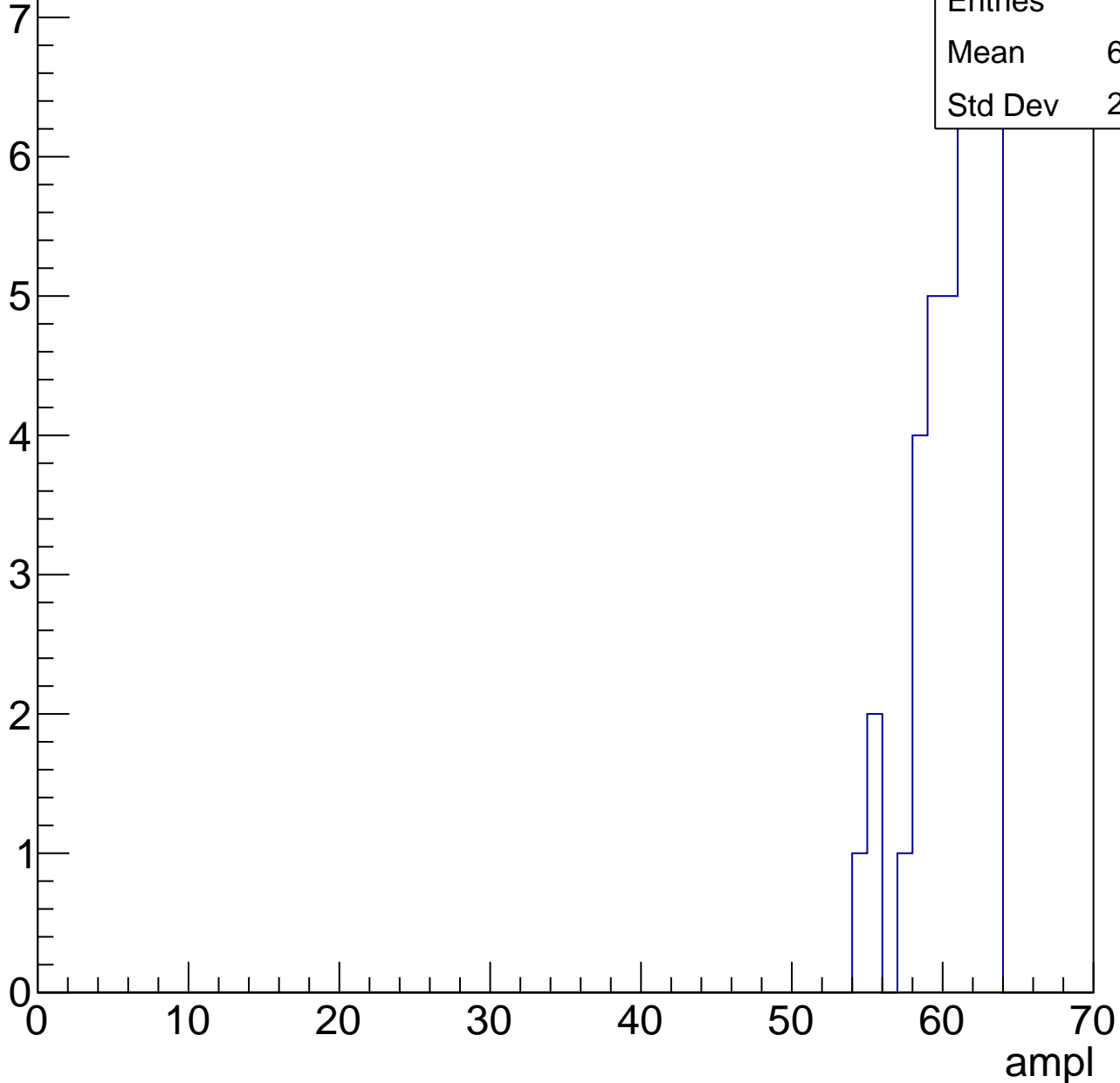


# B0L001S, U17-ch64, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	39
Mean	60.26
Std Dev	2.328



# B0L001S, U17-ch64, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch64, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U17-ch65, adc0

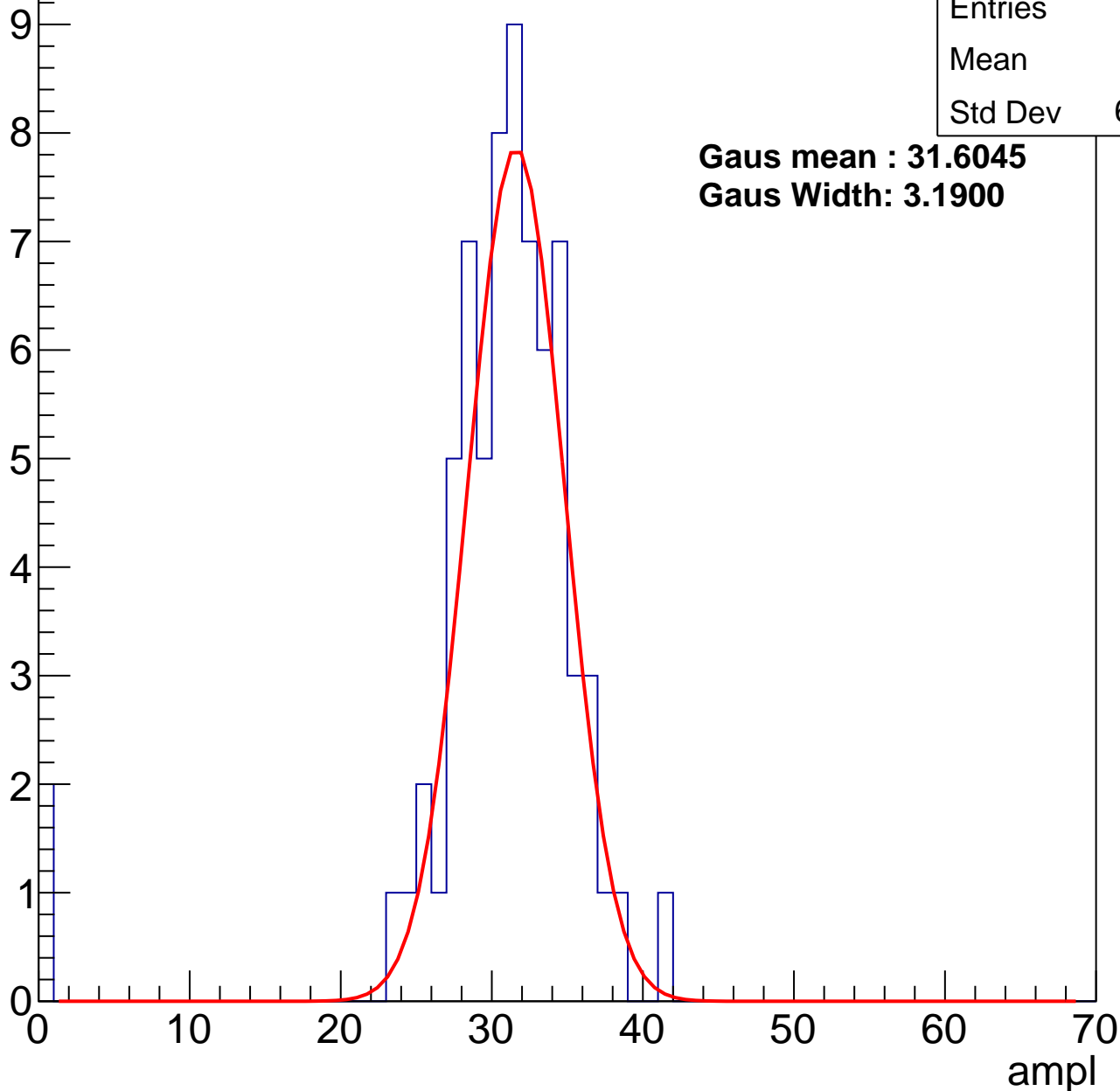
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	30.1
Std Dev	6.151

**Gaus mean : 31.6045**

**Gaus Width: 3.1900**



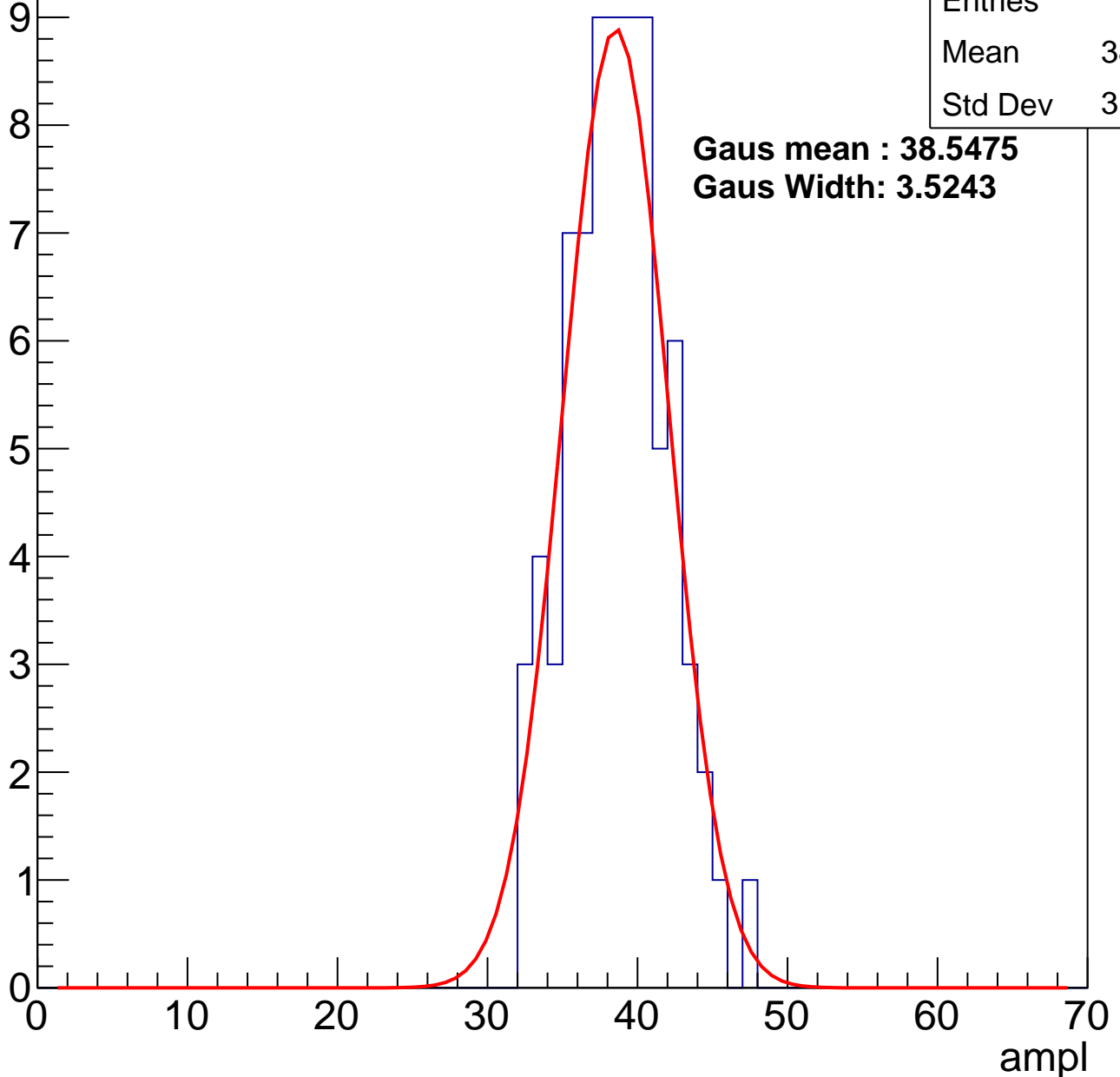
# B0L001S, U17-ch65, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	78
Mean	38.19
Std Dev	3.235

**Gaus mean : 38.5475**  
**Gaus Width: 3.5243**



# B0L001S, U17-ch65, adc2

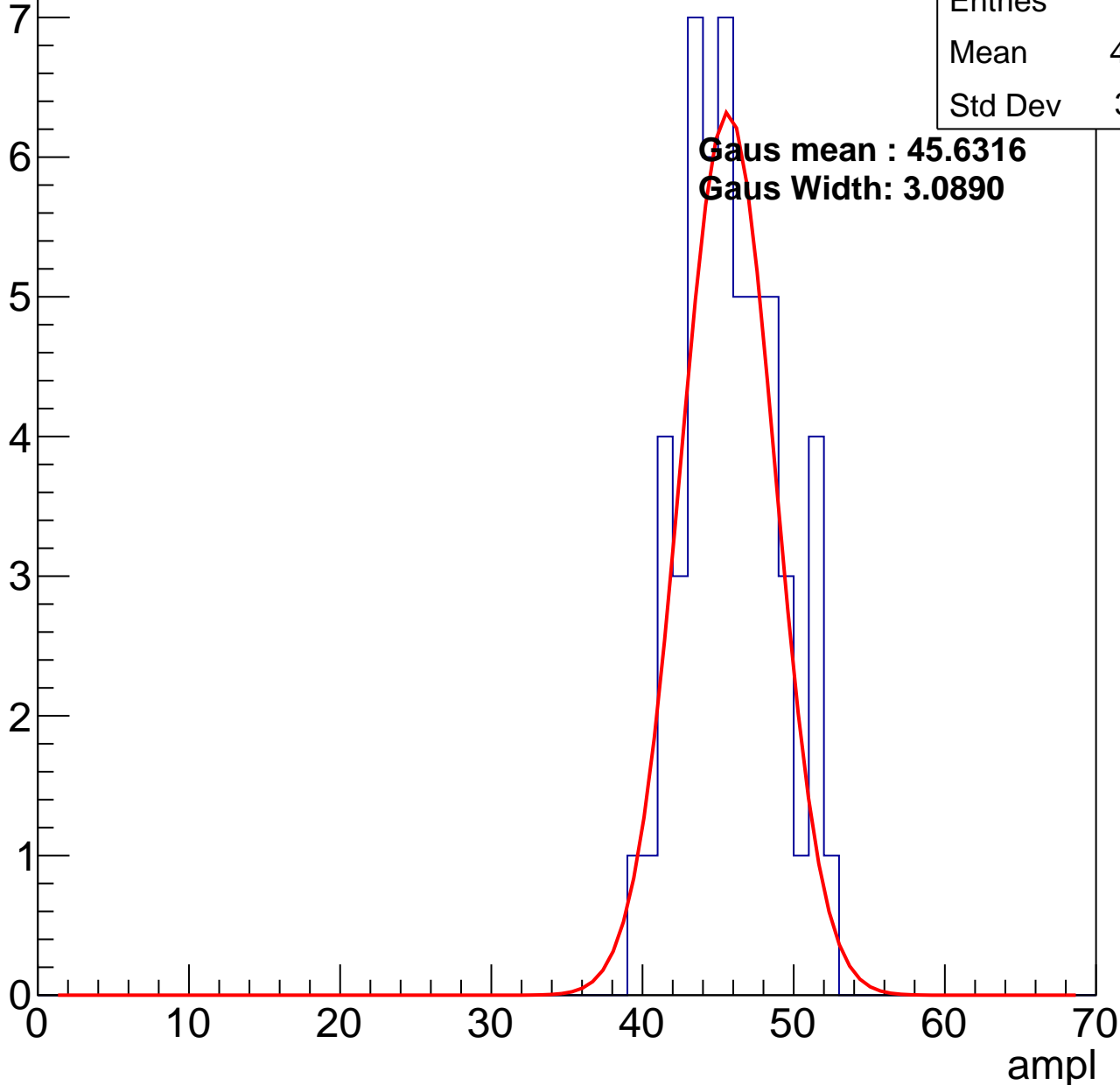
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	45.42
Std Dev	3.111

**Gaus mean : 45.6316**

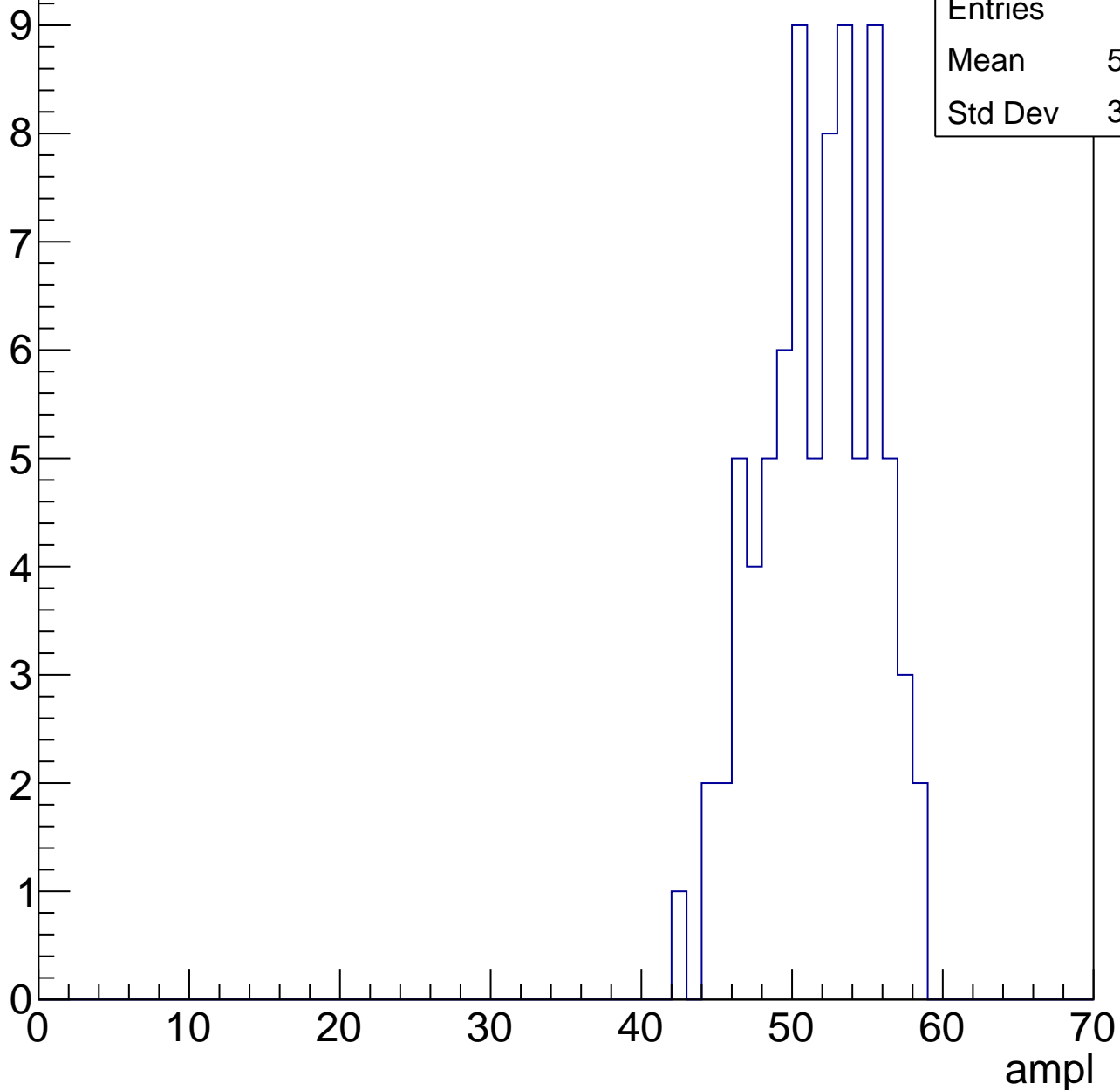
**Gaus Width: 3.0890**



# B0L001S, U17-ch65, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

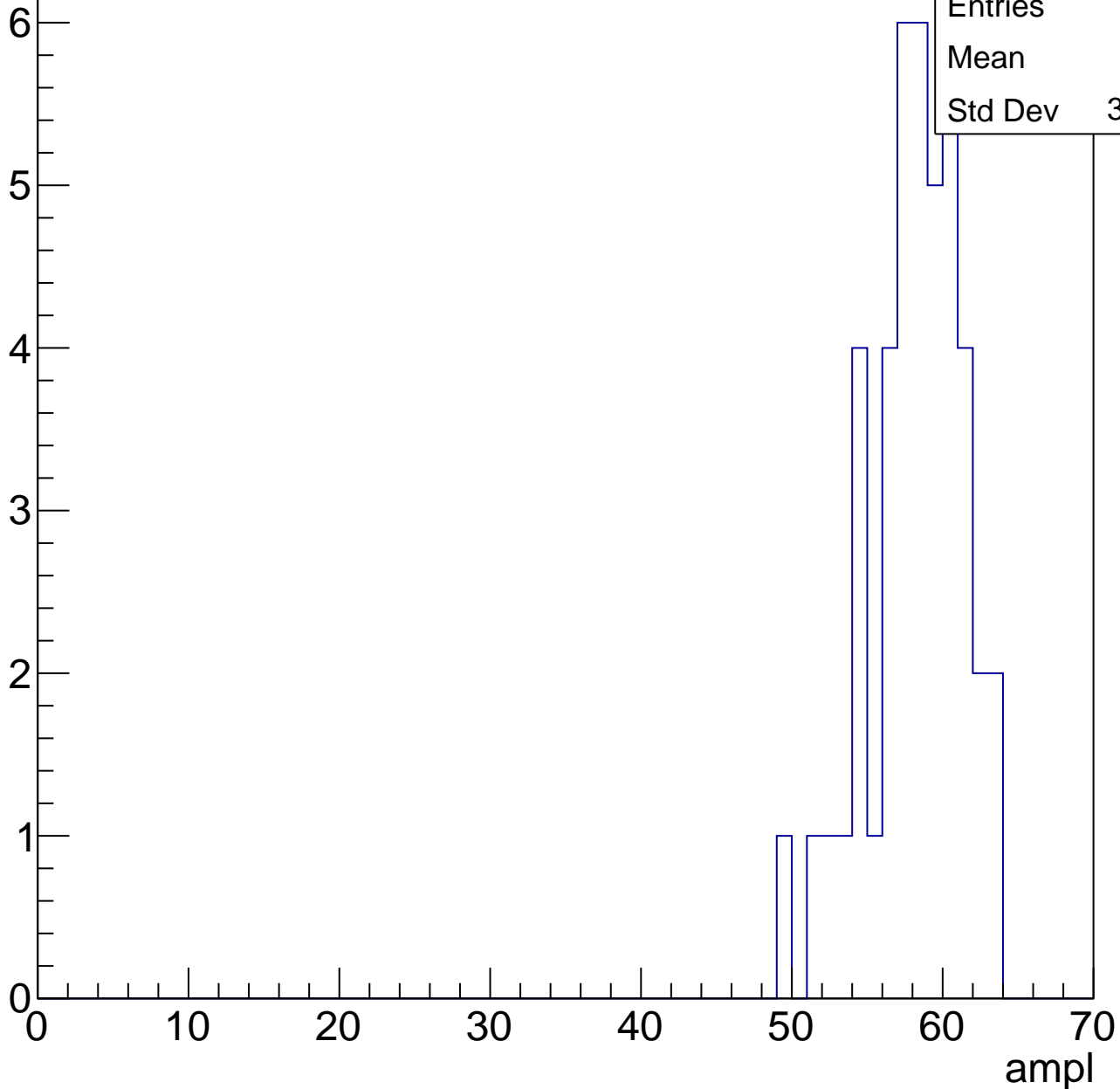


# B0L001S, U17-ch65, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	44
Mean	57.7
Std Dev	3.123

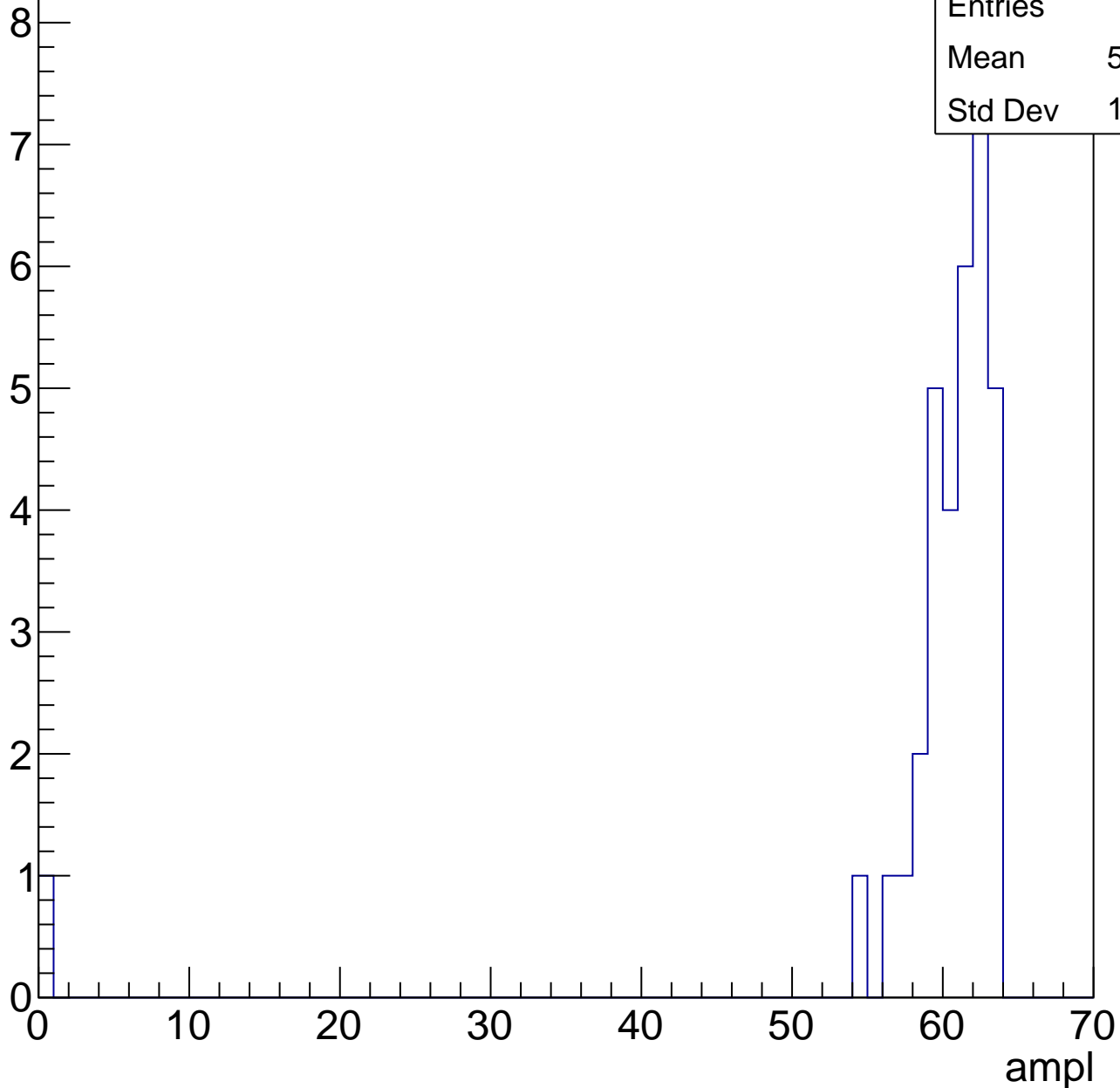


# B0L001S, U17-ch65, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	34
Mean	58.68
Std Dev	10.43



# B0L001S, U17-ch65, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

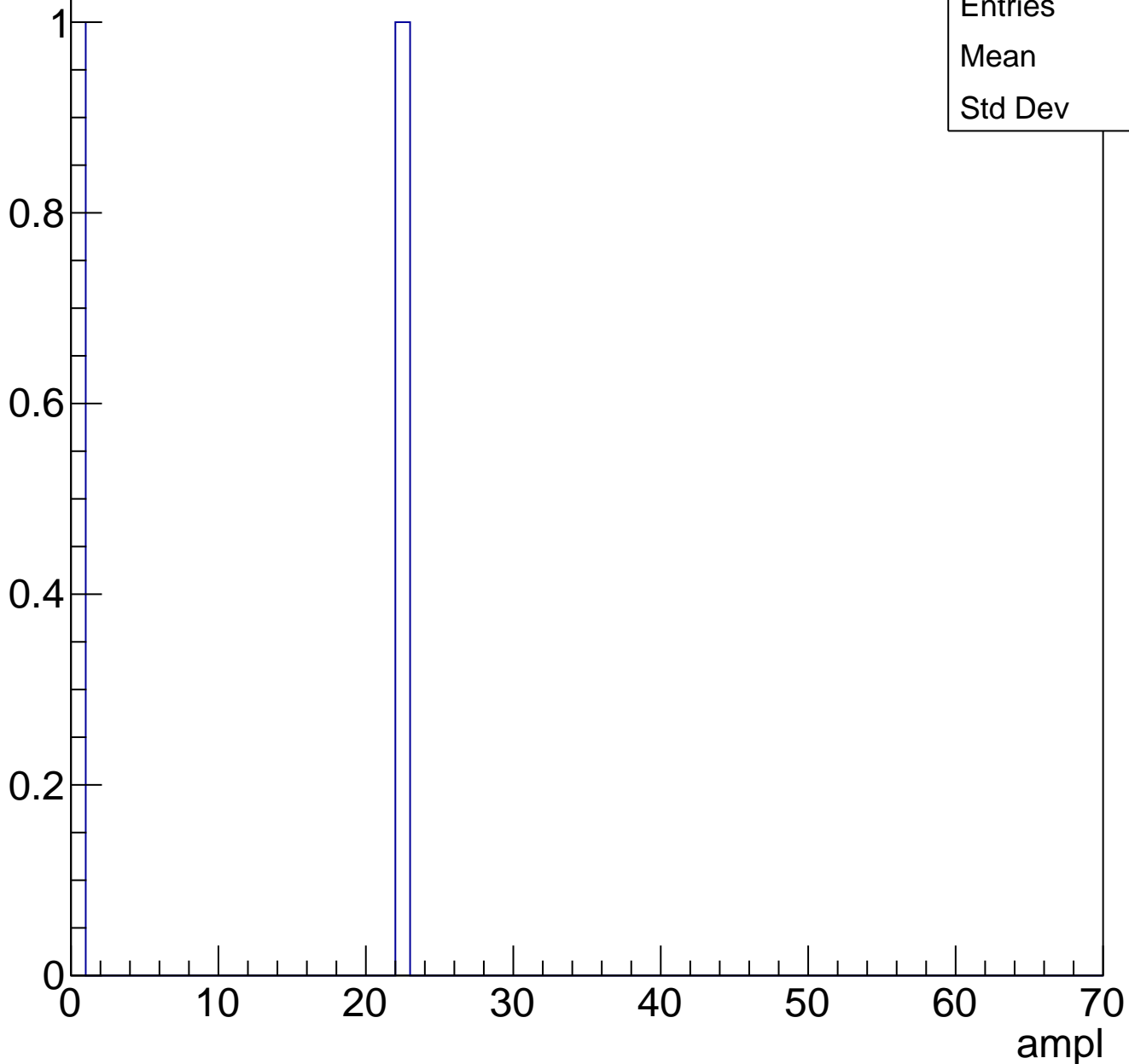




# B0L001S, U17-ch65, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	11
Std Dev	11

# B0L001S, U17-ch66, adc0

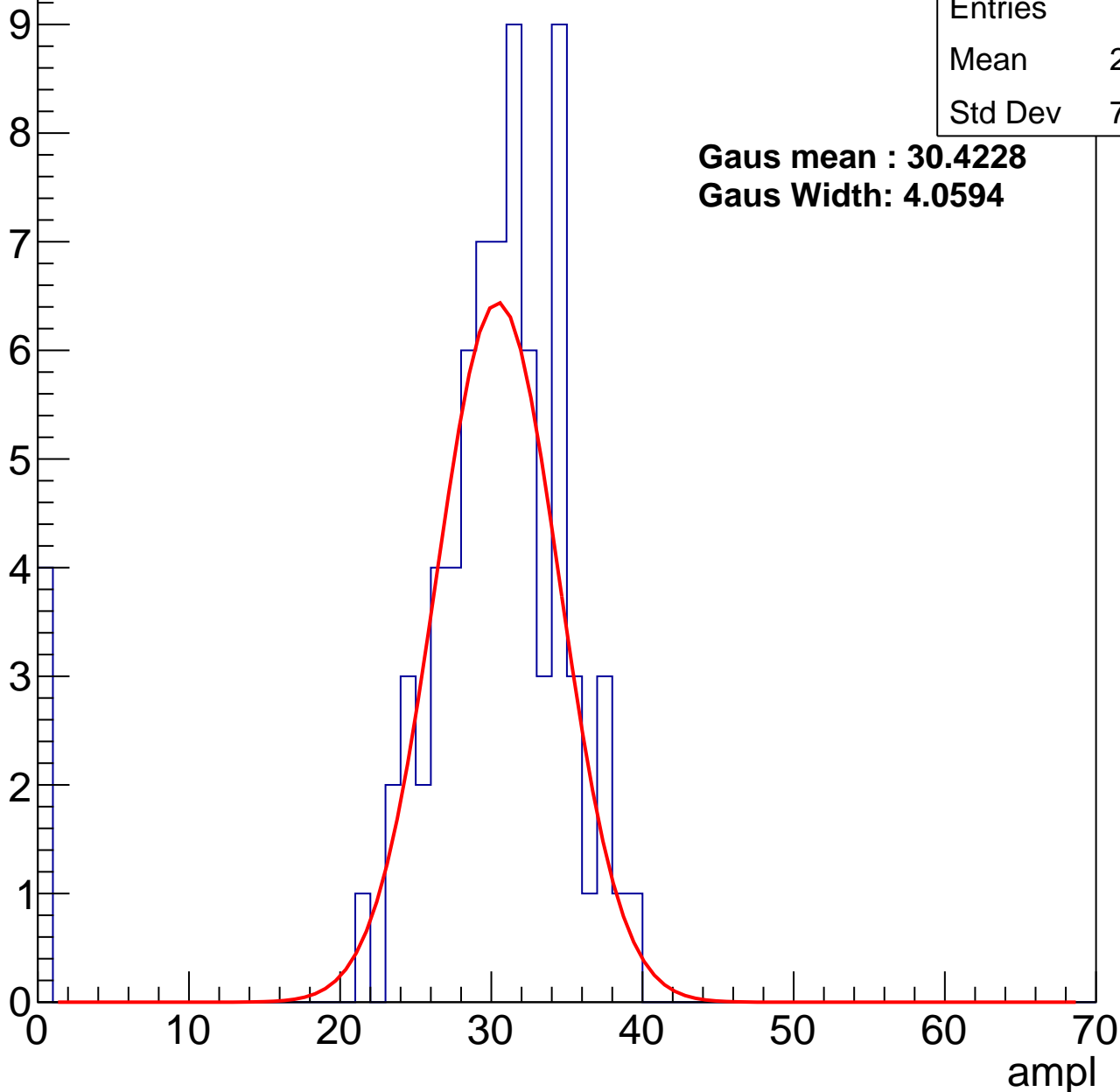
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	76
Mean	28.78
Std Dev	7.747

**Gaus mean : 30.4228**

**Gaus Width: 4.0594**



# B0L001S, U17-ch66, adc1

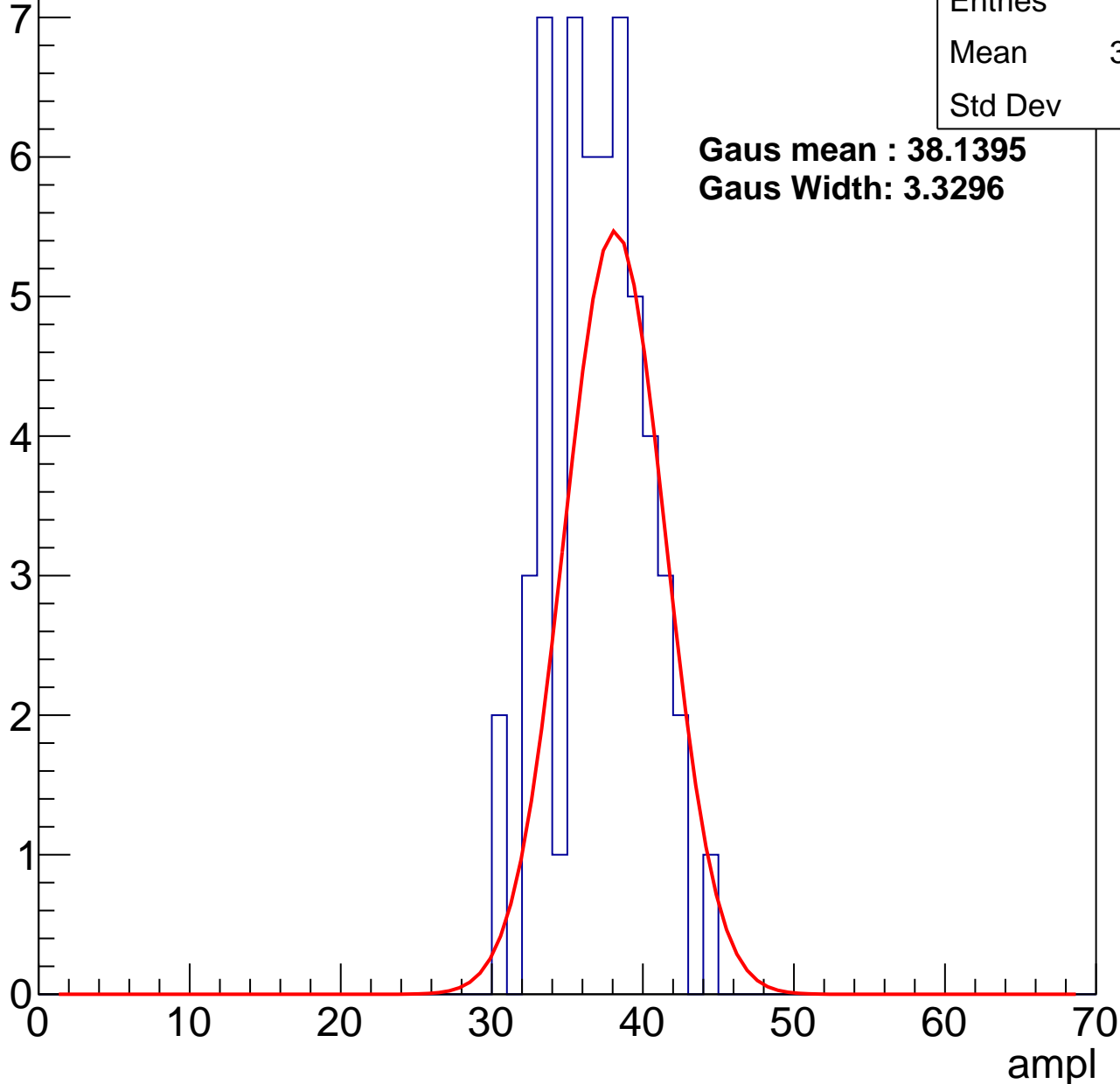
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	36.59
Std Dev	3.13

**Gaus mean : 38.1395**

**Gaus Width: 3.3296**



# B0L001S, U17-ch66, adc2

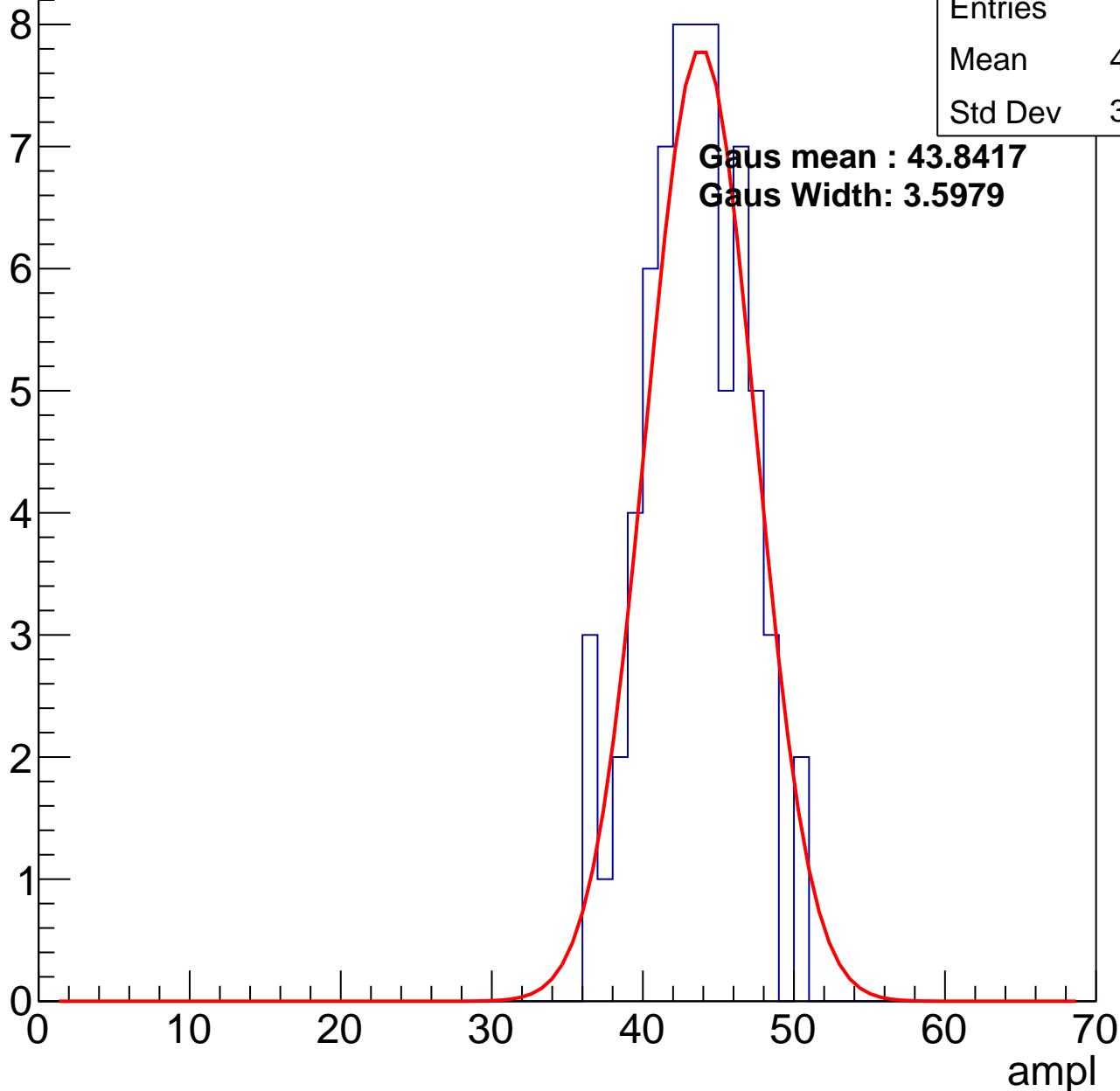
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	42.93
Std Dev	3.254

**Gaus mean : 43.8417**

**Gaus Width: 3.5979**

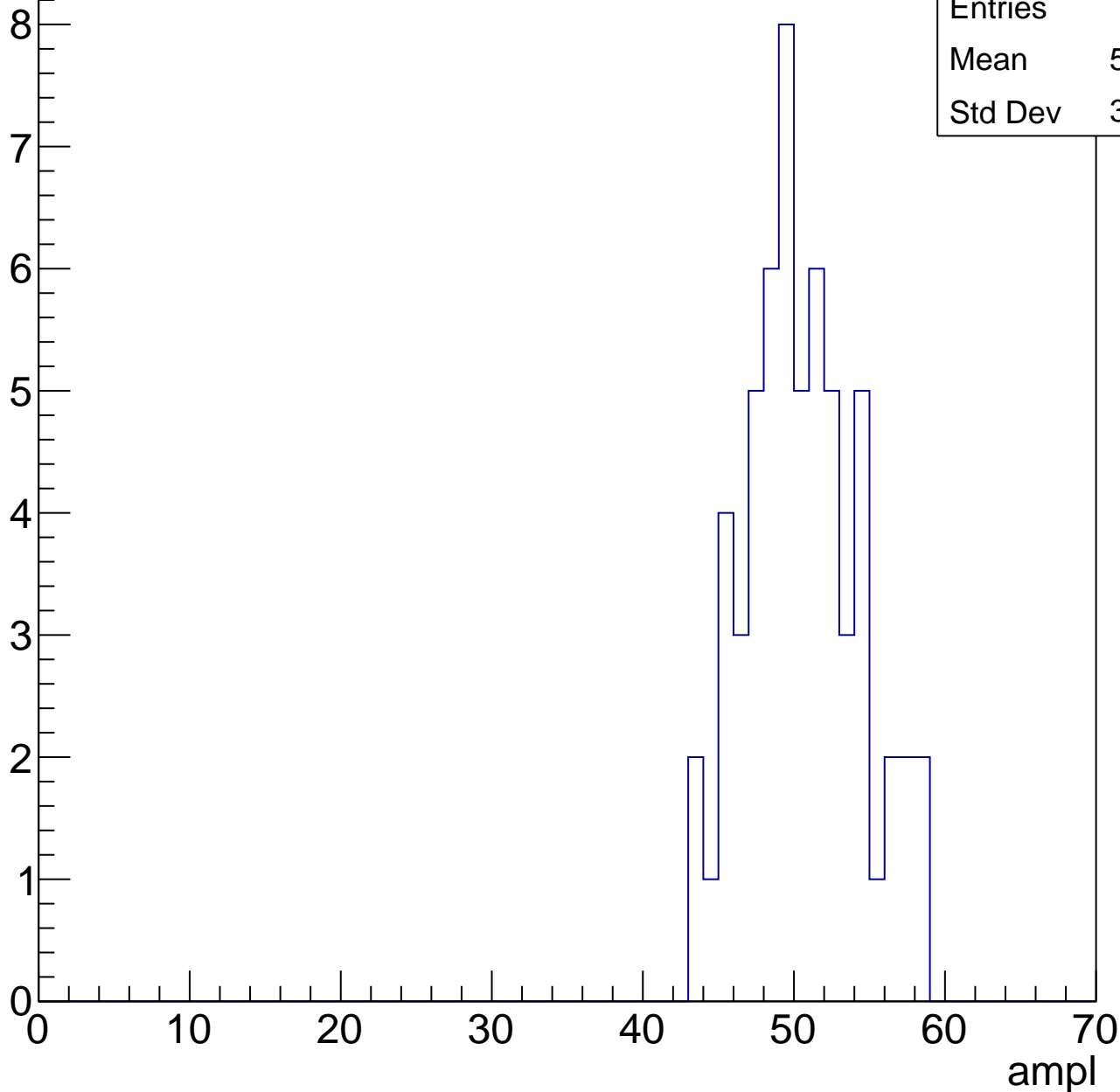


# B0L001S, U17-ch66, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	50.08
Std Dev	3.685

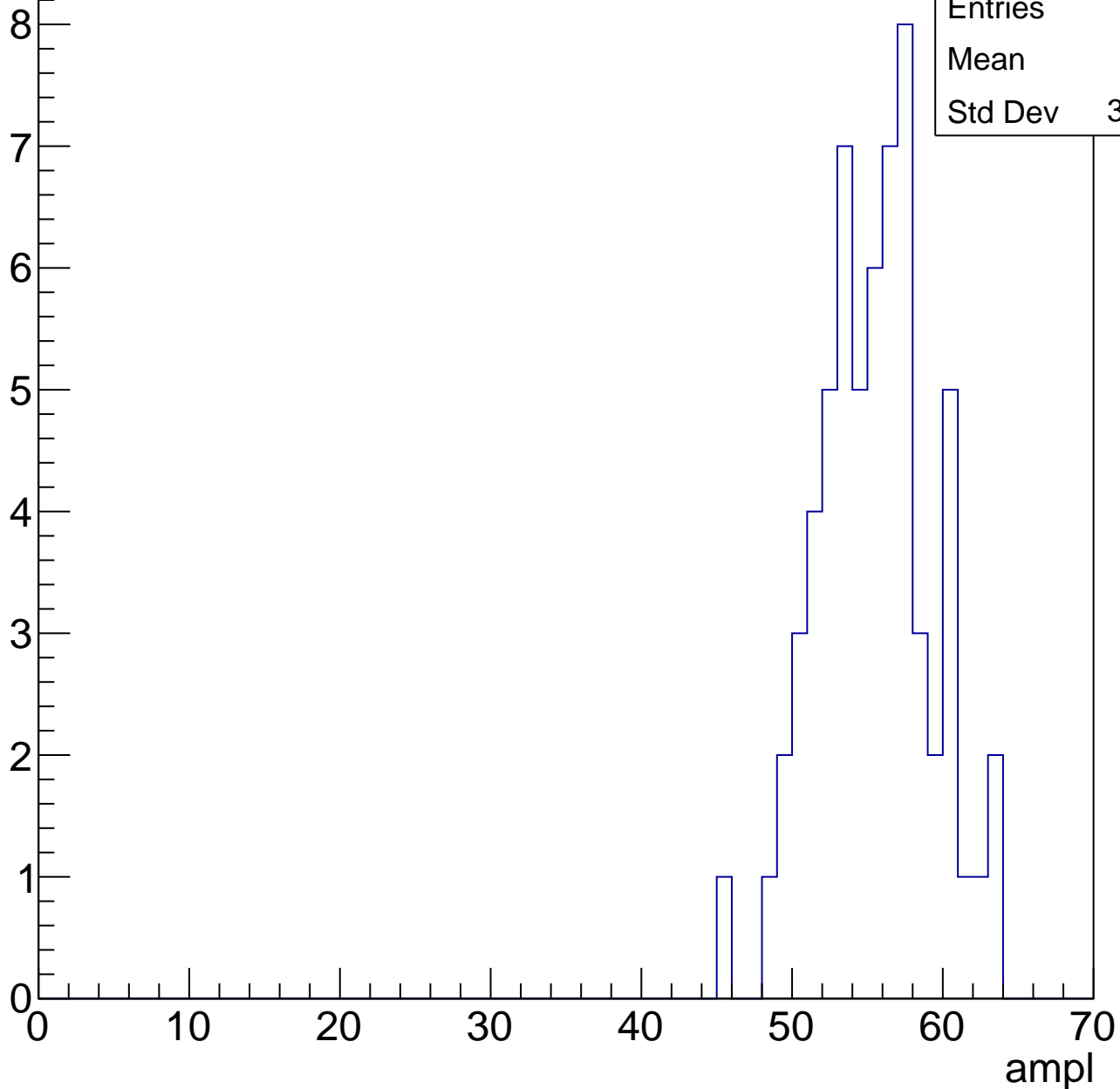


# B0L001S, U17-ch66, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	55
Std Dev	3.725

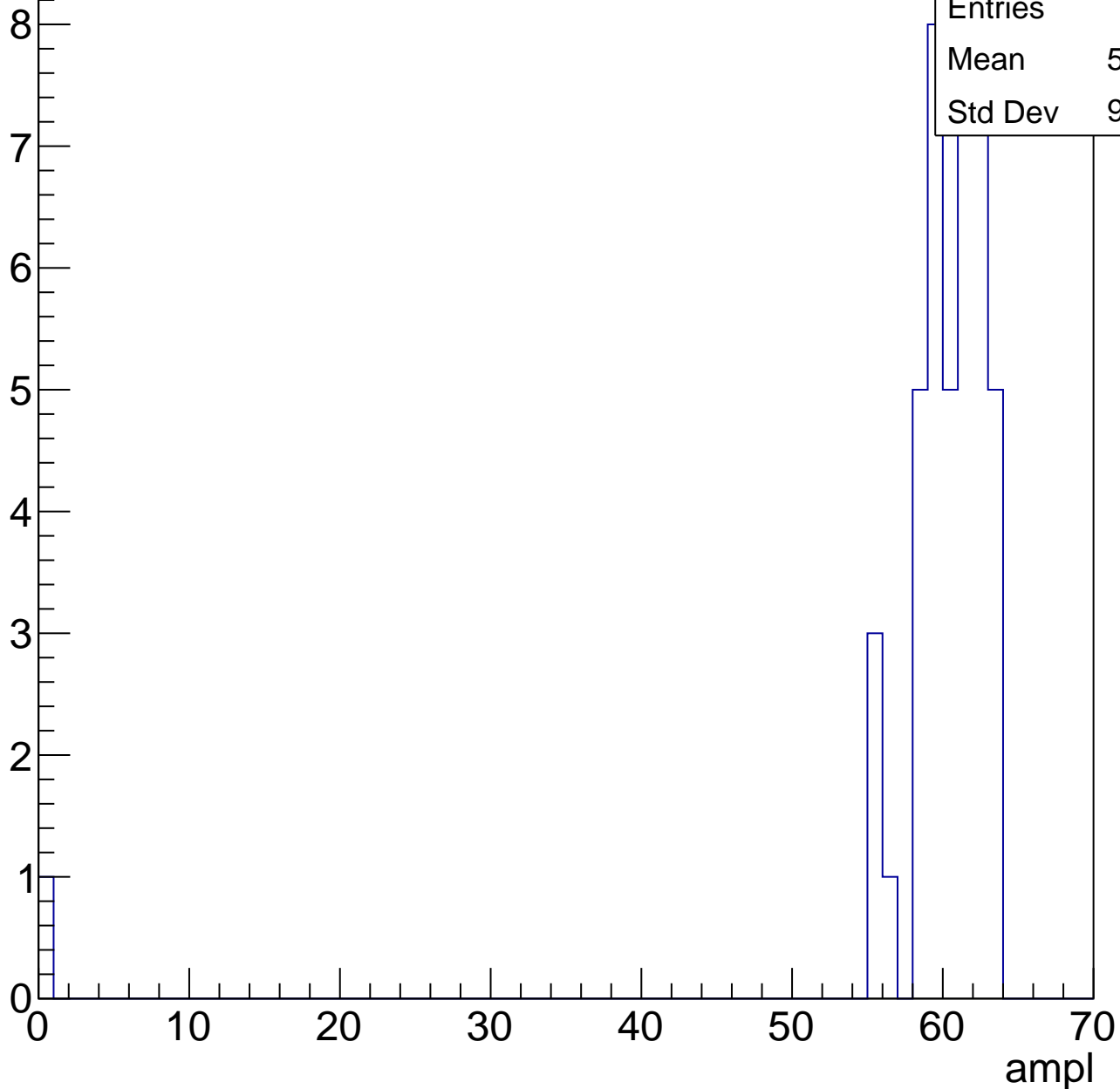


# B0L001S, U17-ch66, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	44
Mean	58.68
Std Dev	9.204



# B0L001S, U17-ch66, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch66, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U17-ch67, adc0

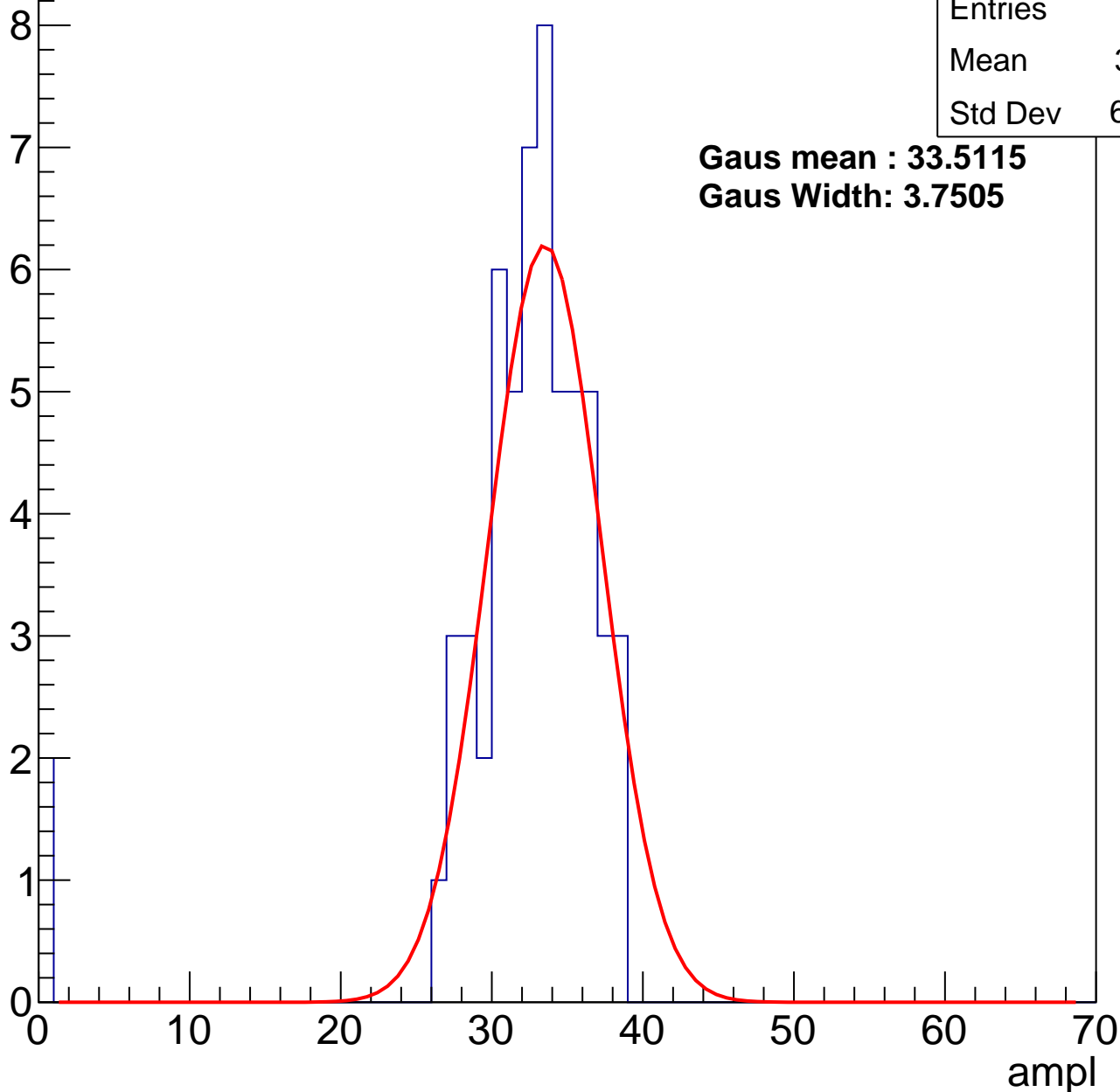
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	31.41
Std Dev	6.657

**Gaus mean : 33.5115**

**Gaus Width: 3.7505**



# B0L001S, U17-ch67, adc1

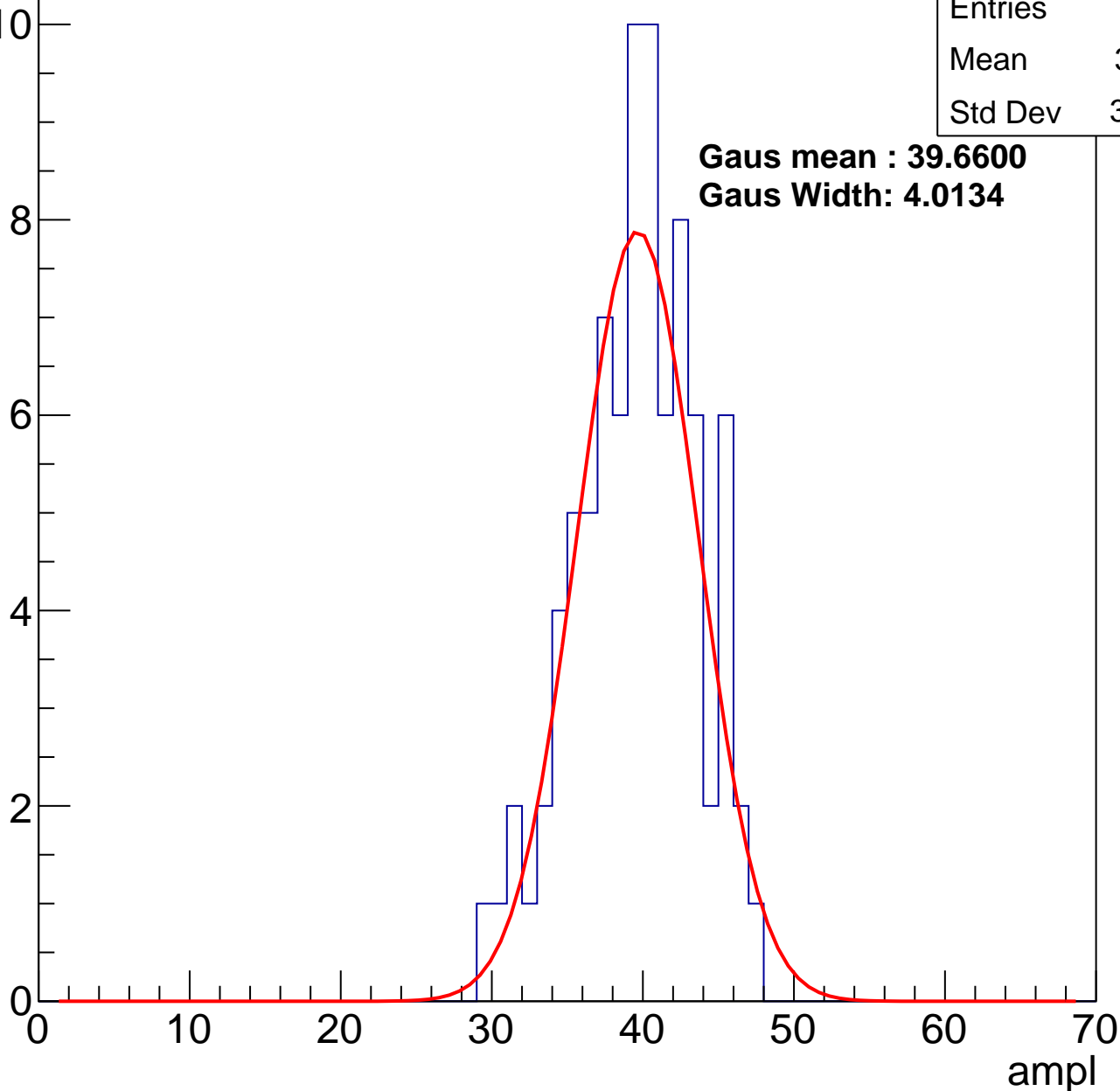
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	85
Mean	39.11
Std Dev	3.938

**Gaus mean : 39.6600**

**Gaus Width: 4.0134**



# B0L001S, U17-ch67, adc2

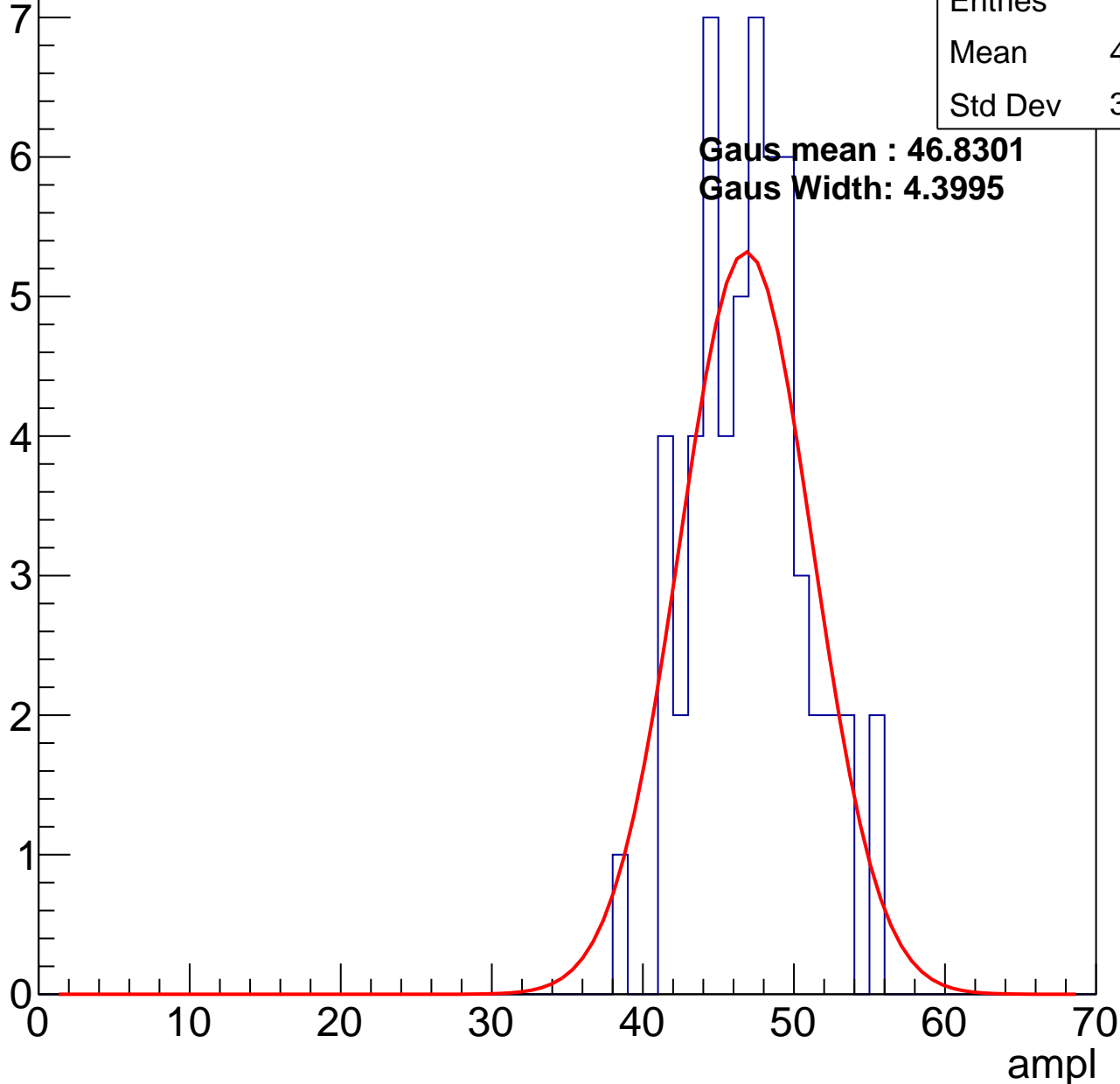
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	46.65
Std Dev	3.639

**Gaus mean : 46.8301**

**Gaus Width: 4.3995**

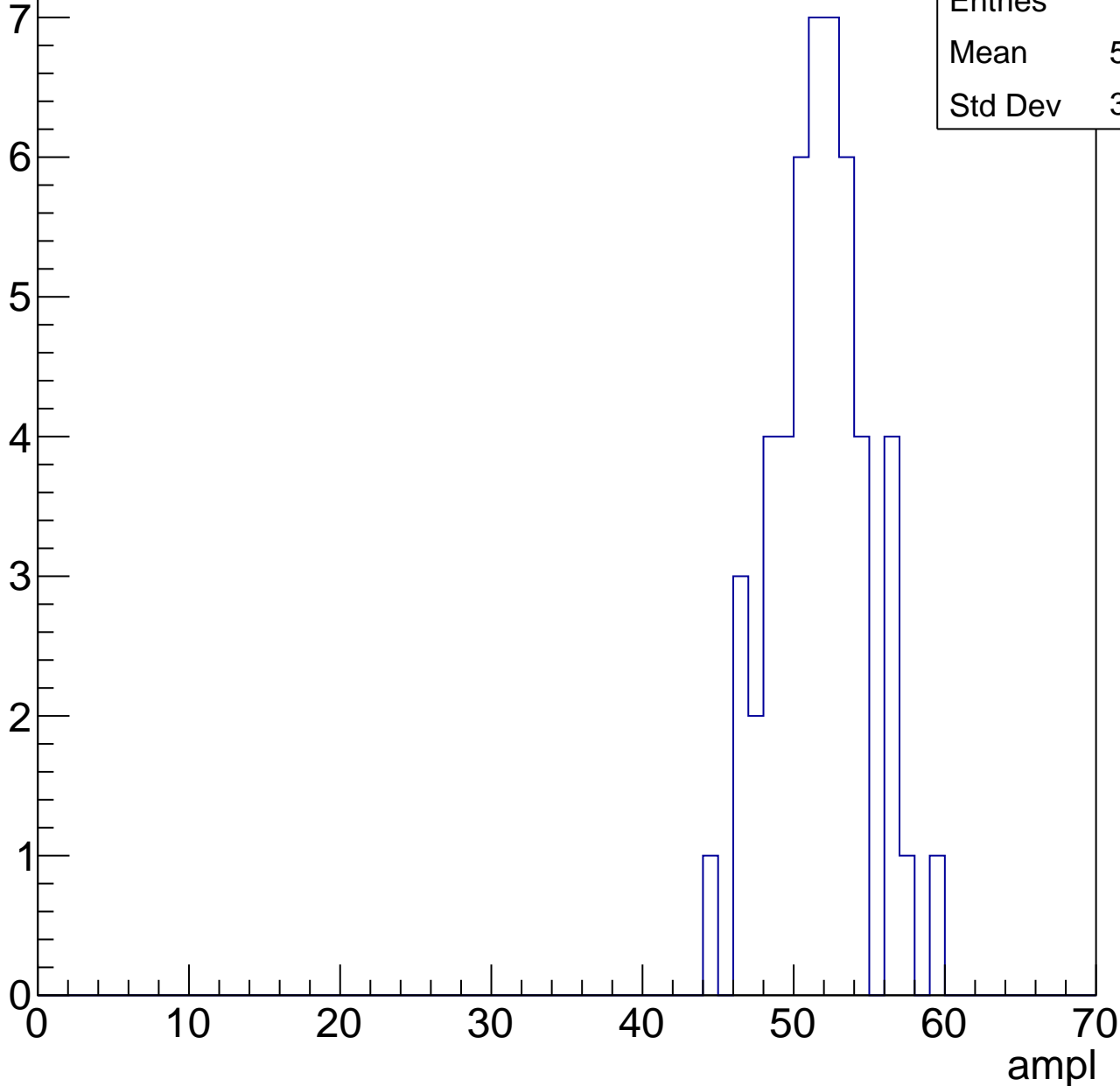


# B0L001S, U17-ch67, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	50
Mean	51.18
Std Dev	3.096

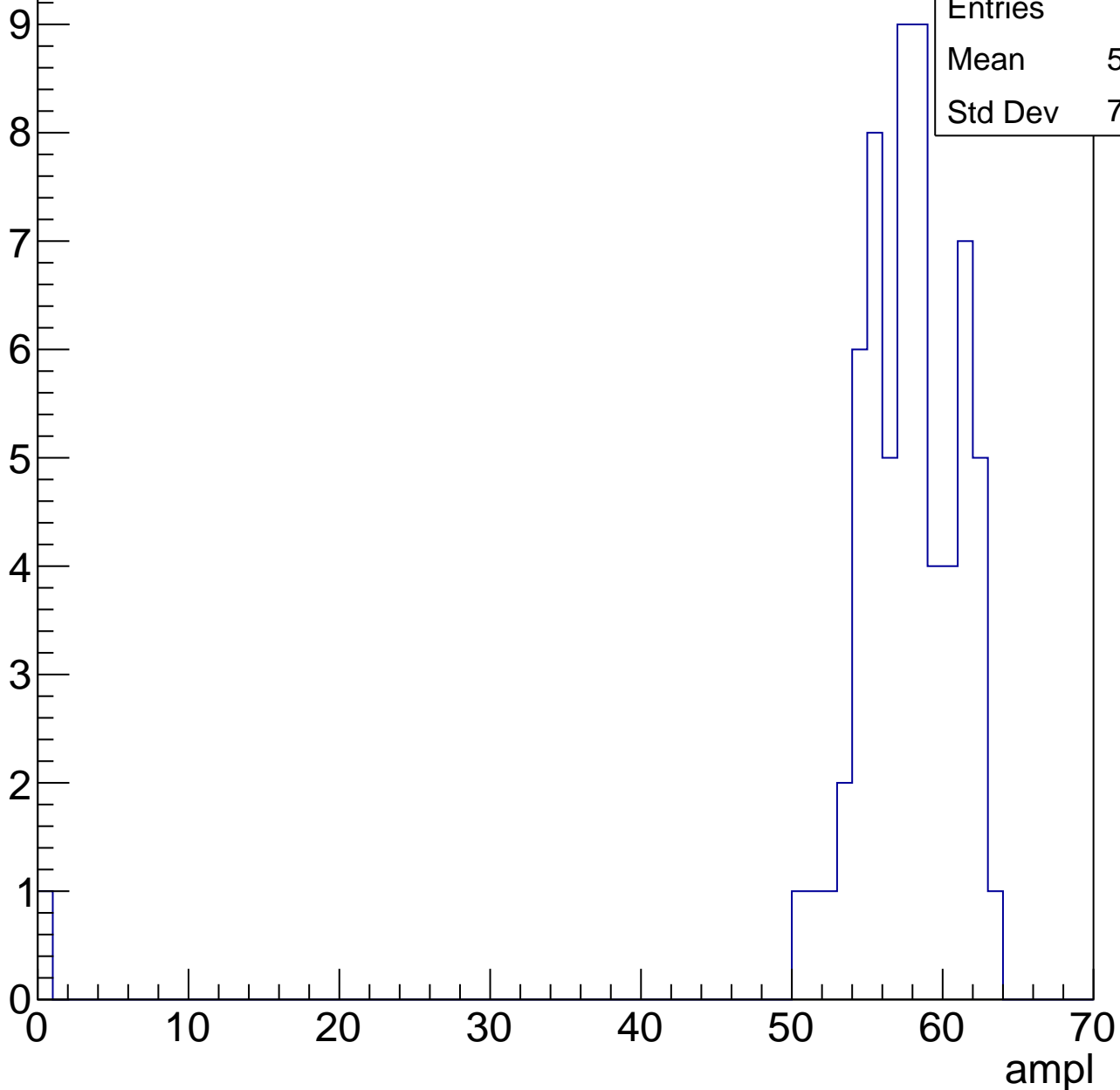


# B0L001S, U17-ch67, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	56.47
Std Dev	7.703

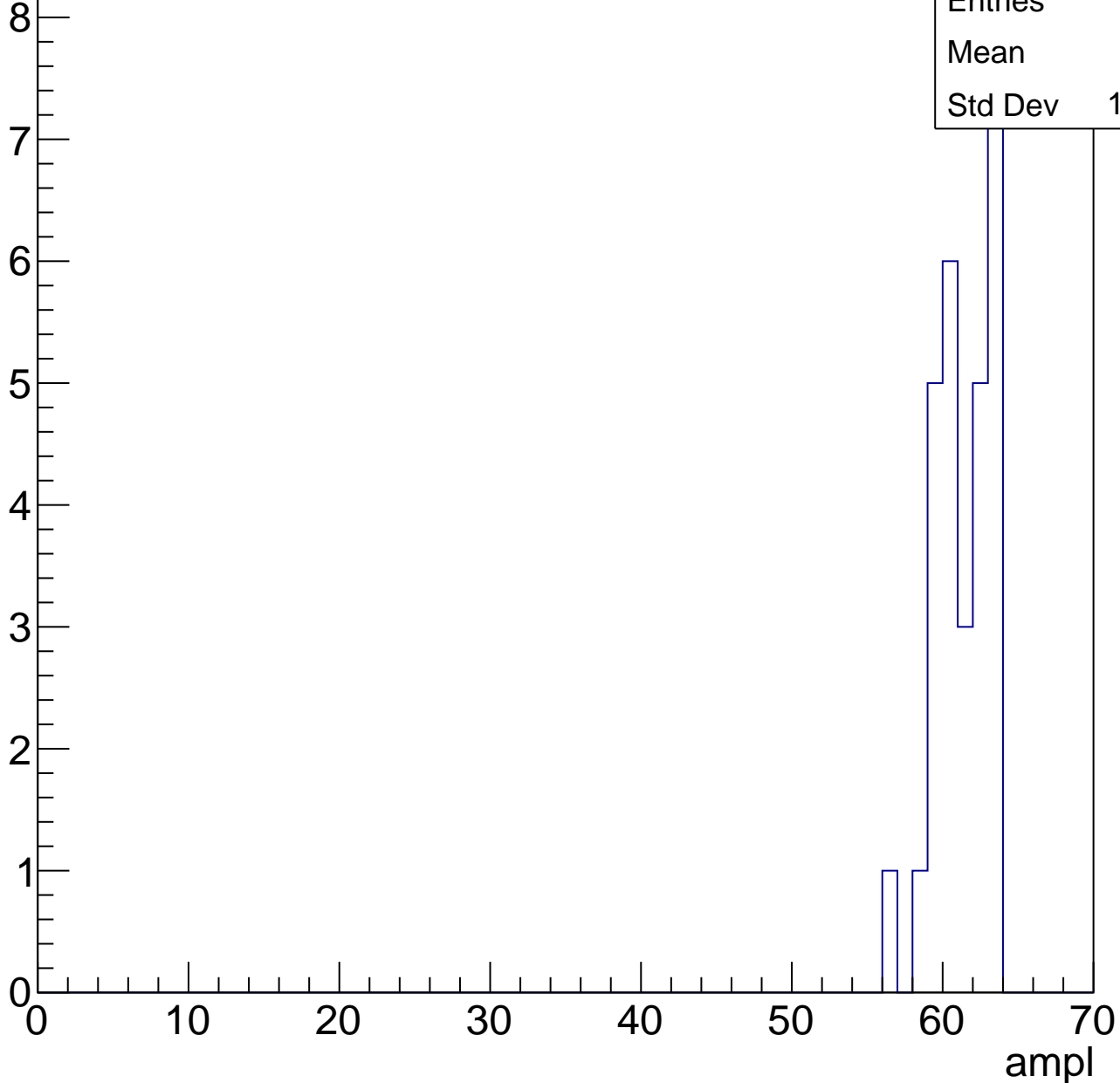


# B0L001S, U17-ch67, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	29
Mean	60.9
Std Dev	1.826



# B0L001S, U17-ch67, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch67, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U17-ch68, adc0

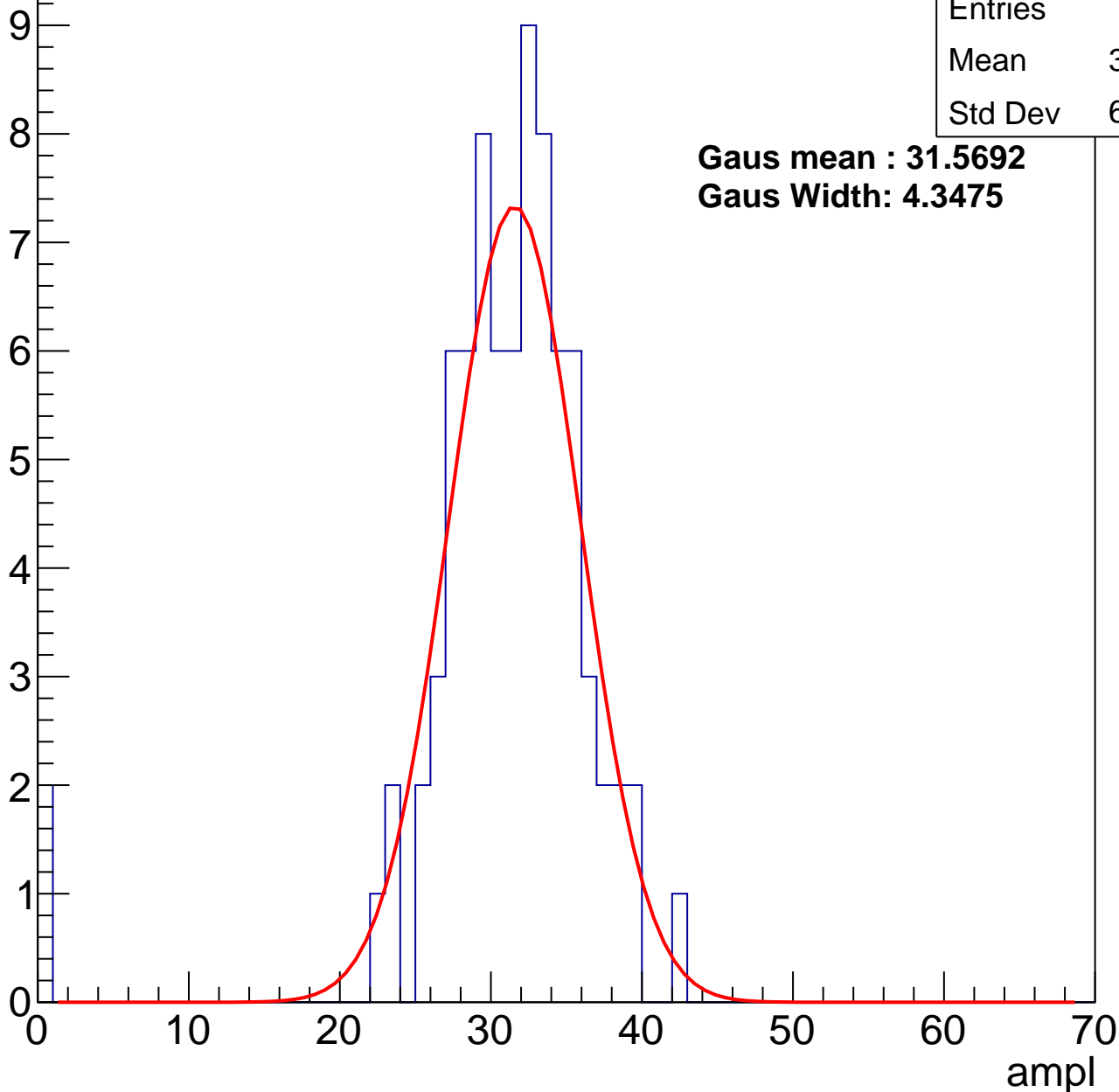
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	81
Mean	30.47
Std Dev	6.214

**Gaus mean : 31.5692**

**Gaus Width: 4.3475**



# B0L001S, U17-ch68, adc1

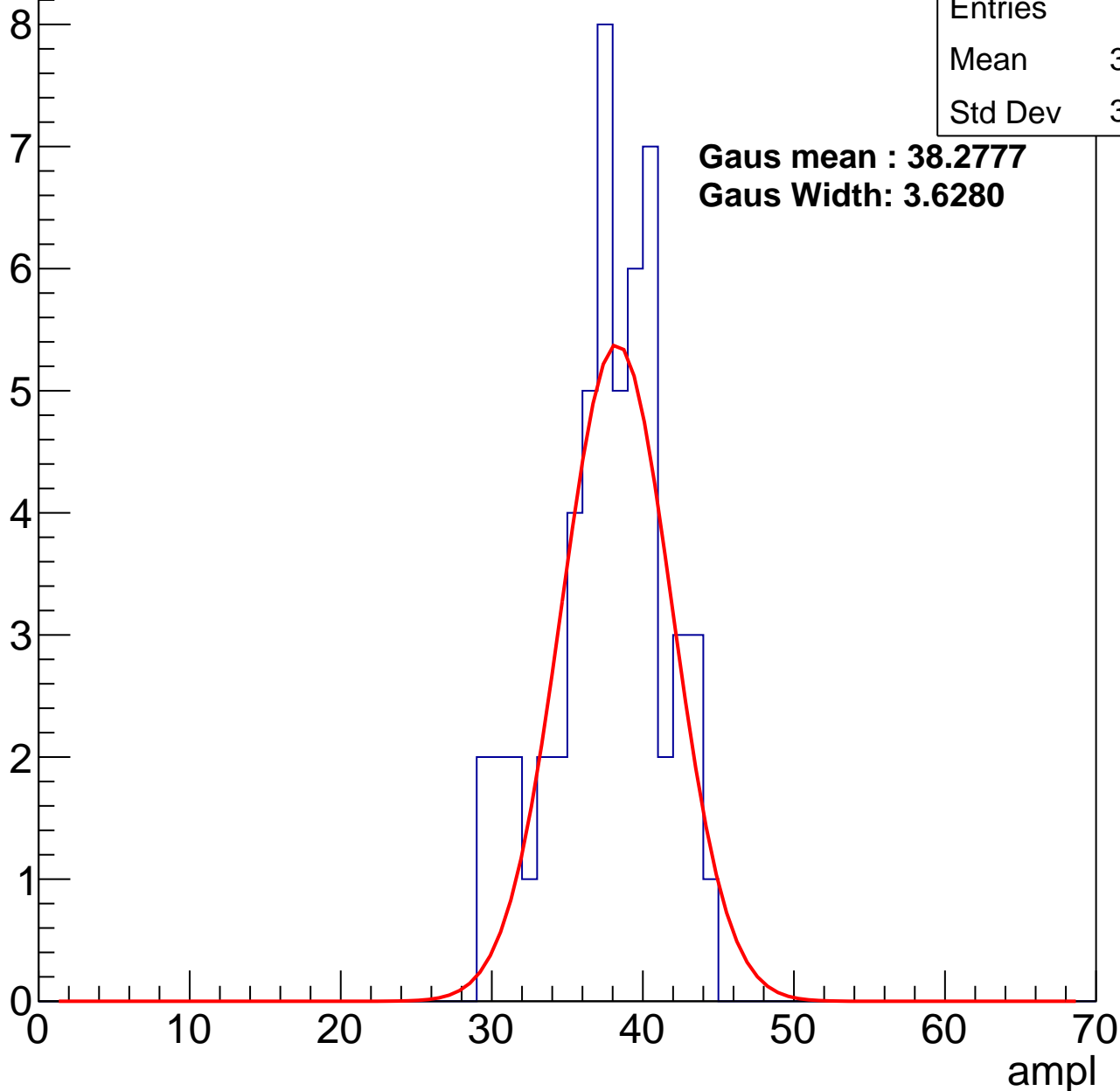
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	37.22
Std Dev	3.686

**Gaus mean : 38.2777**

**Gaus Width: 3.6280**



# B0L001S, U17-ch68, adc2

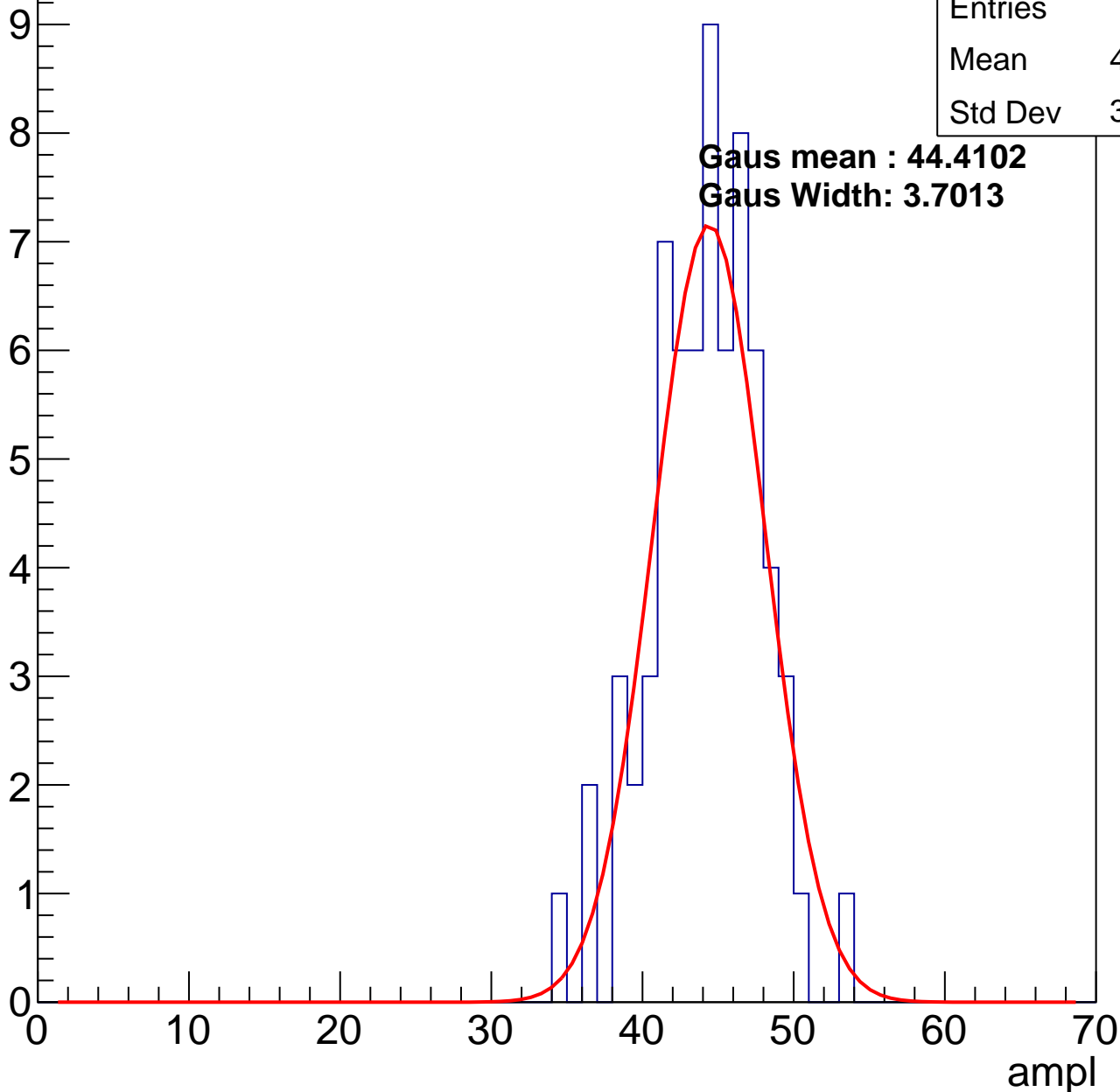
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	43.72
Std Dev	3.576

**Gaus mean : 44.4102**

**Gaus Width: 3.7013**

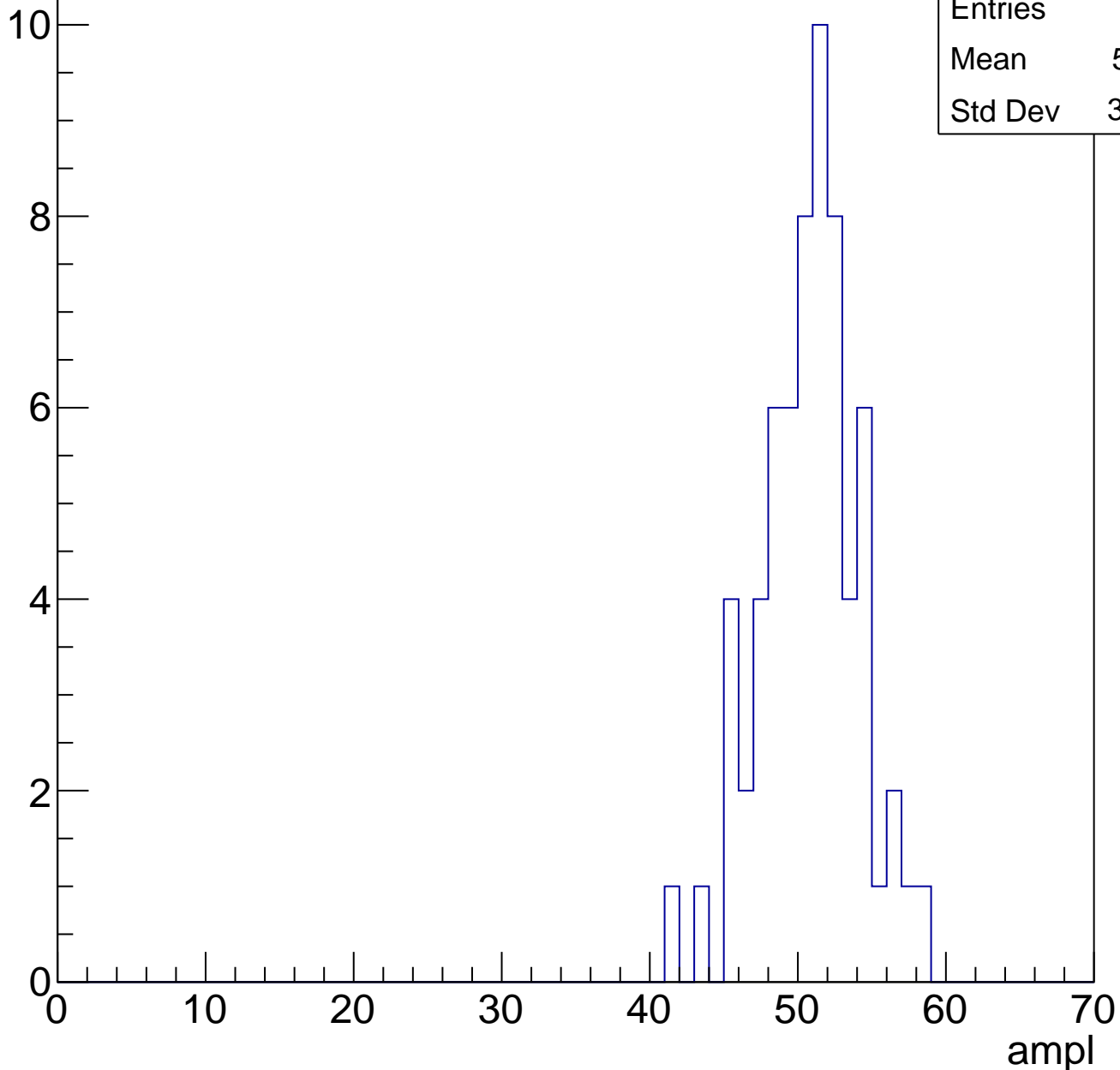


# B0L001S, U17-ch68, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	65
Mean	50.31
Std Dev	3.295

Entry

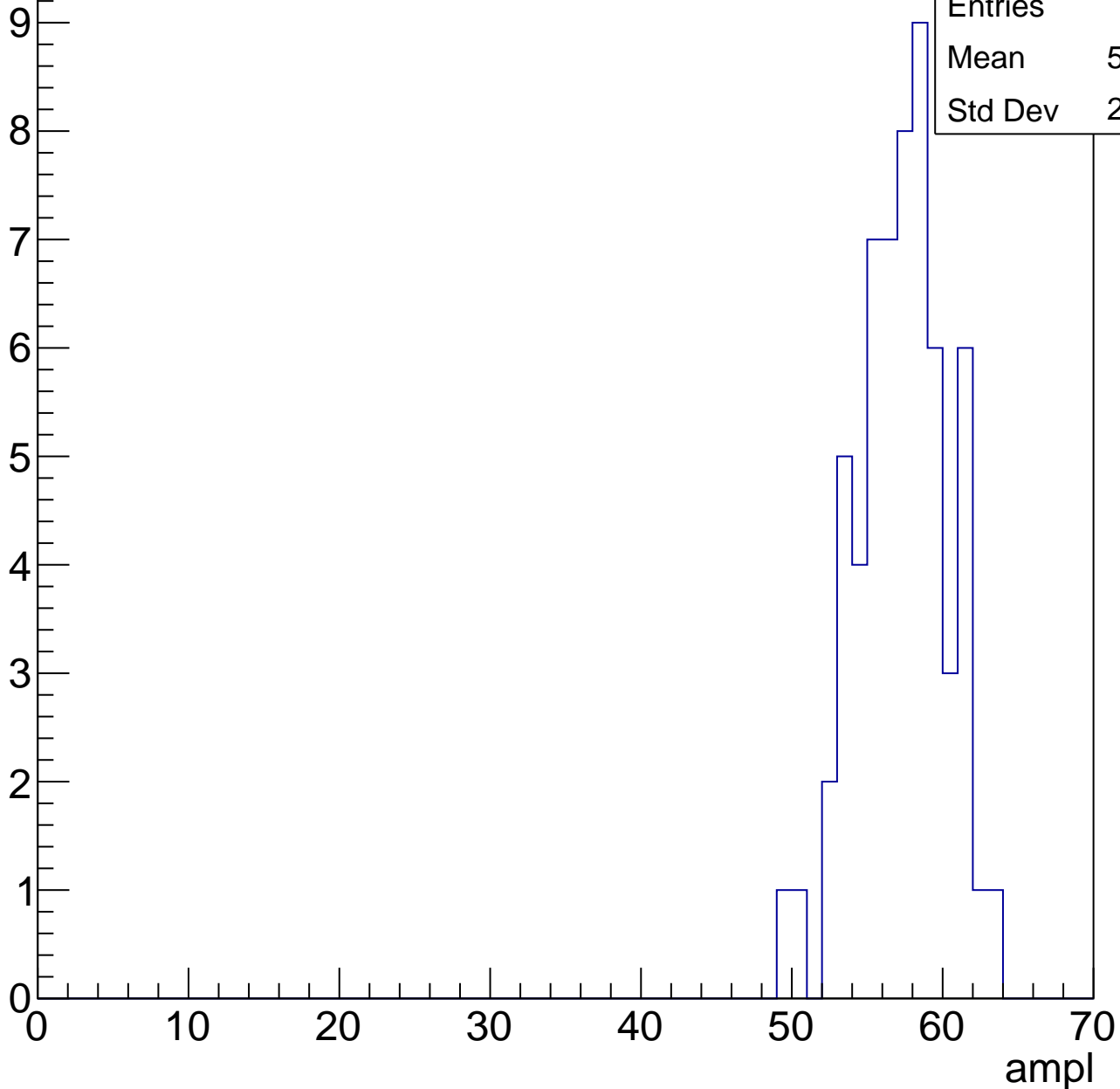


# B0L001S, U17-ch68, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

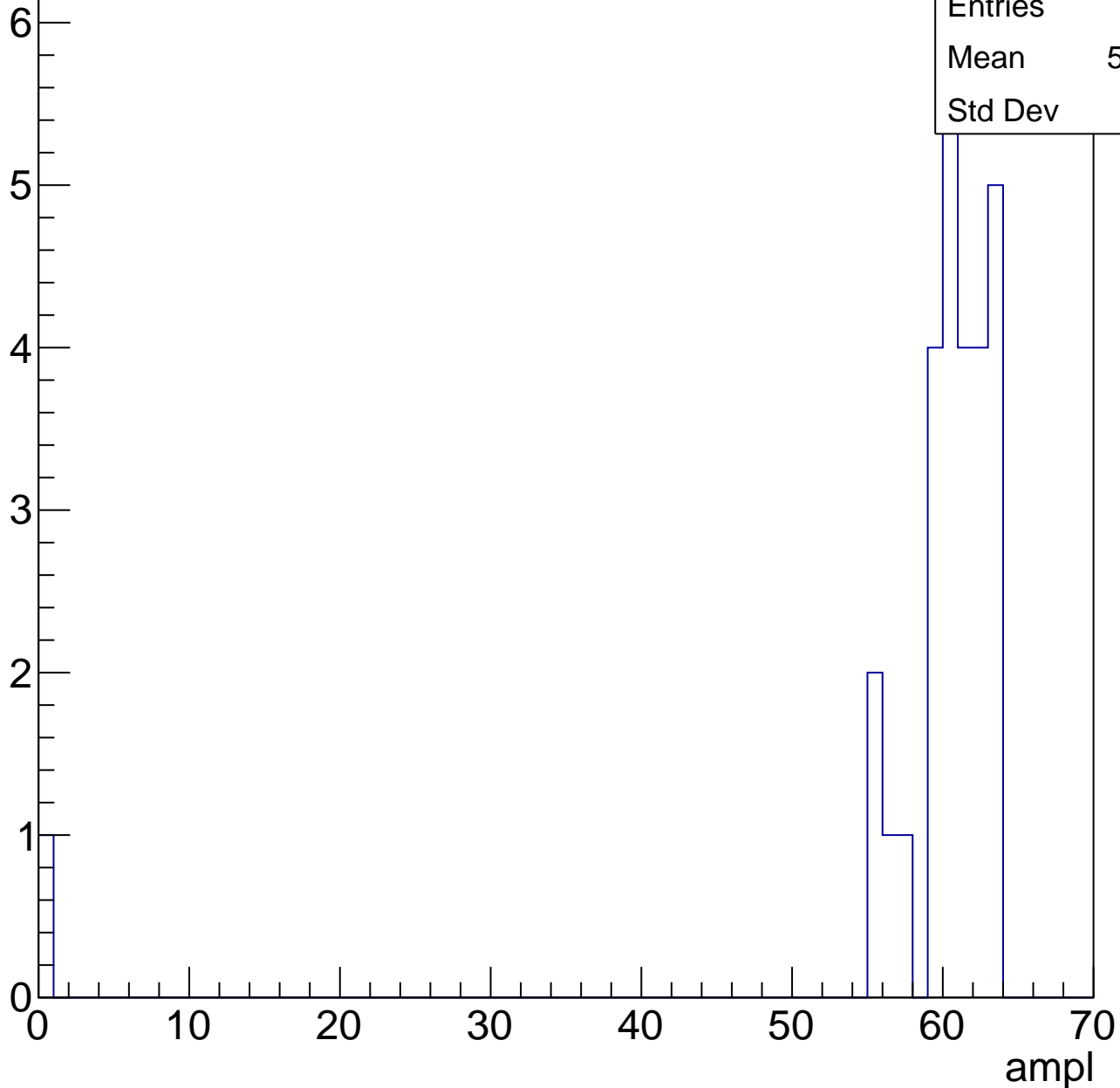
Entries	61
Mean	56.79
Std Dev	2.943



# B0L001S, U17-ch68, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

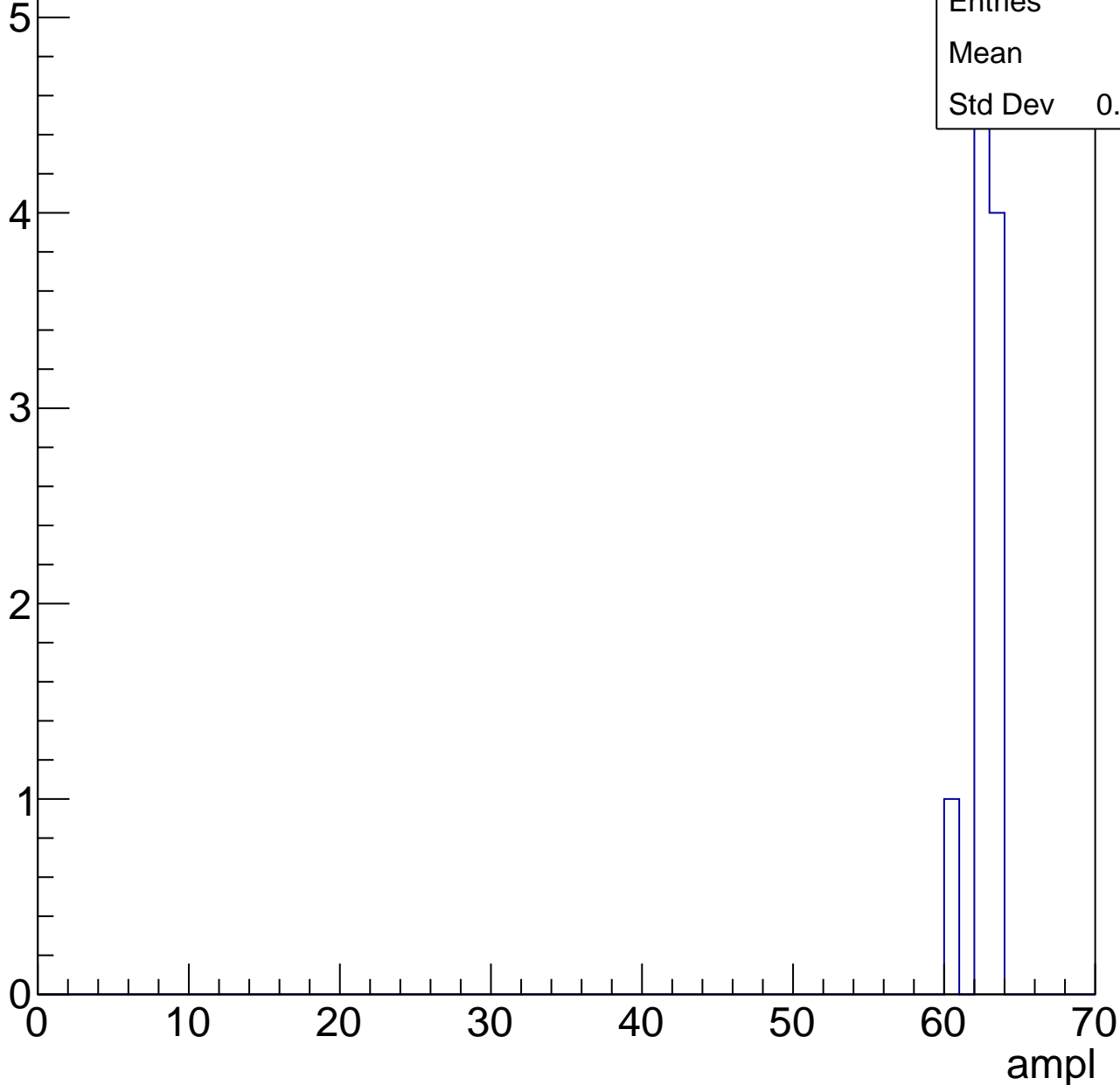


# B0L001S, U17-ch68, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	10
Mean	62.2
Std Dev	0.8718





# B0L001S, U17-ch68, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U17-ch69, adc0

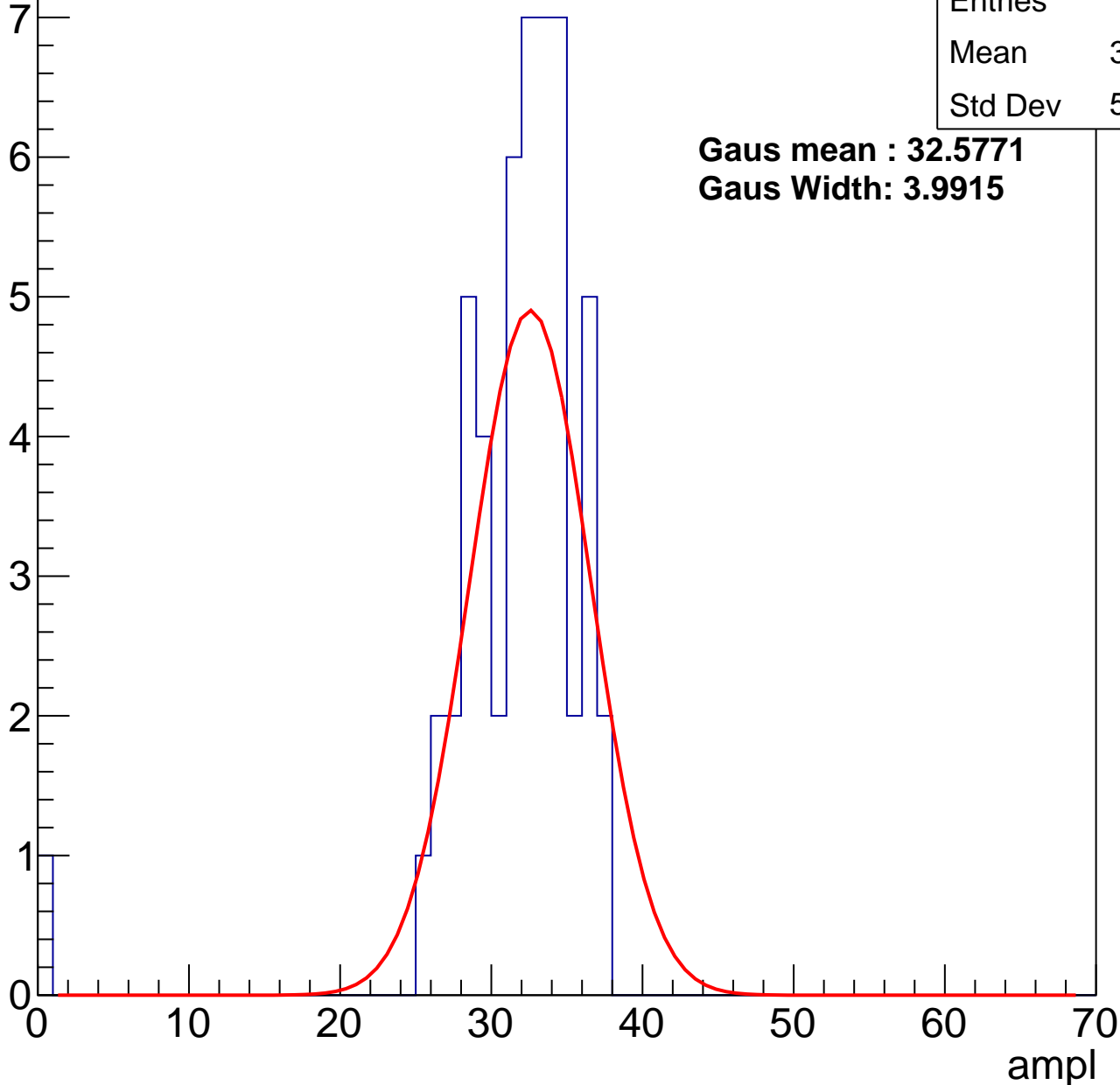
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	31.13
Std Dev	5.263

**Gaus mean : 32.5771**

**Gaus Width: 3.9915**



# B0L001S, U17-ch69, adc1

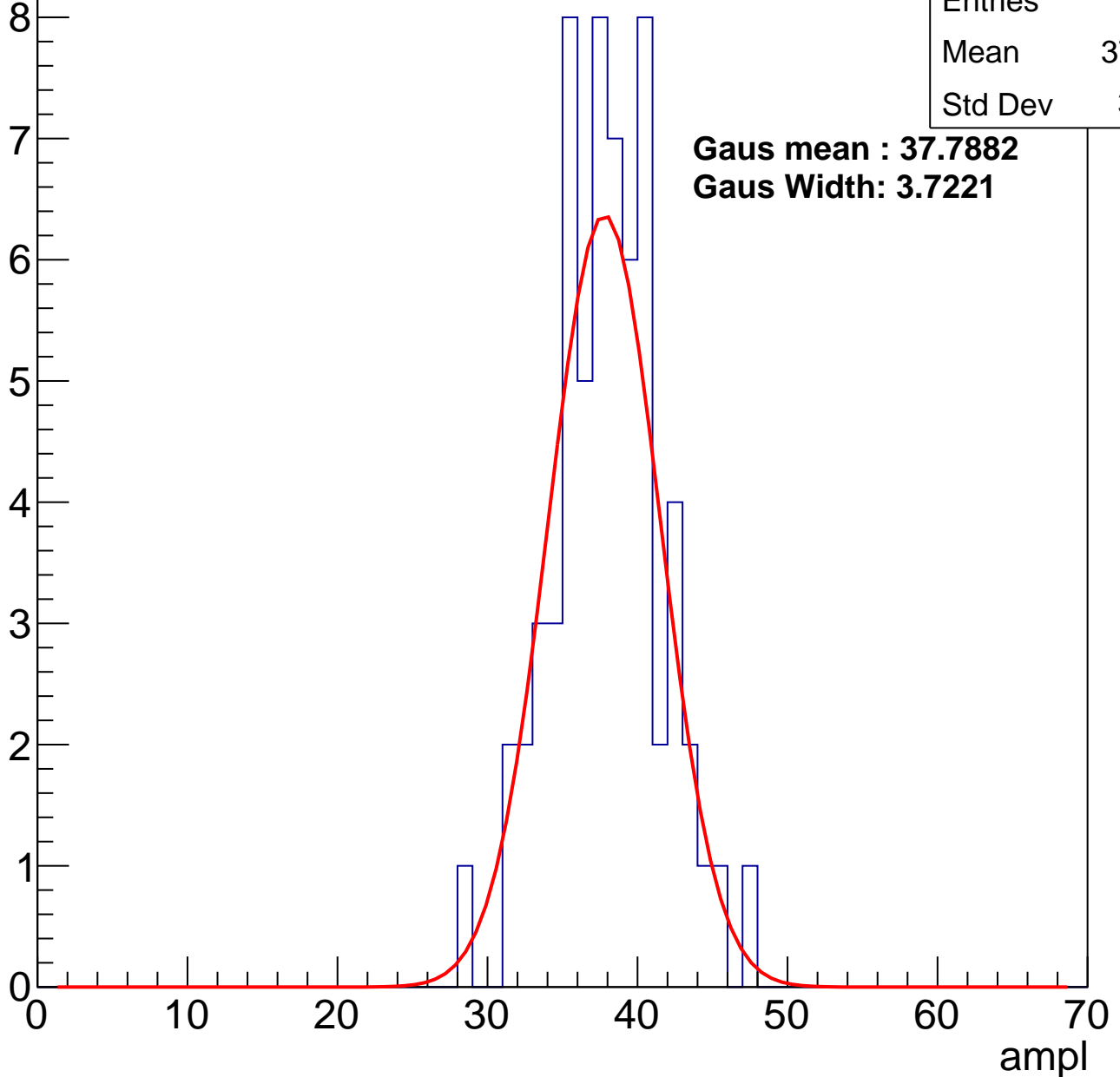
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	37.55
Std Dev	3.57

**Gaus mean : 37.7882**

**Gaus Width: 3.7221**



# B0L001S, U17-ch69, adc2

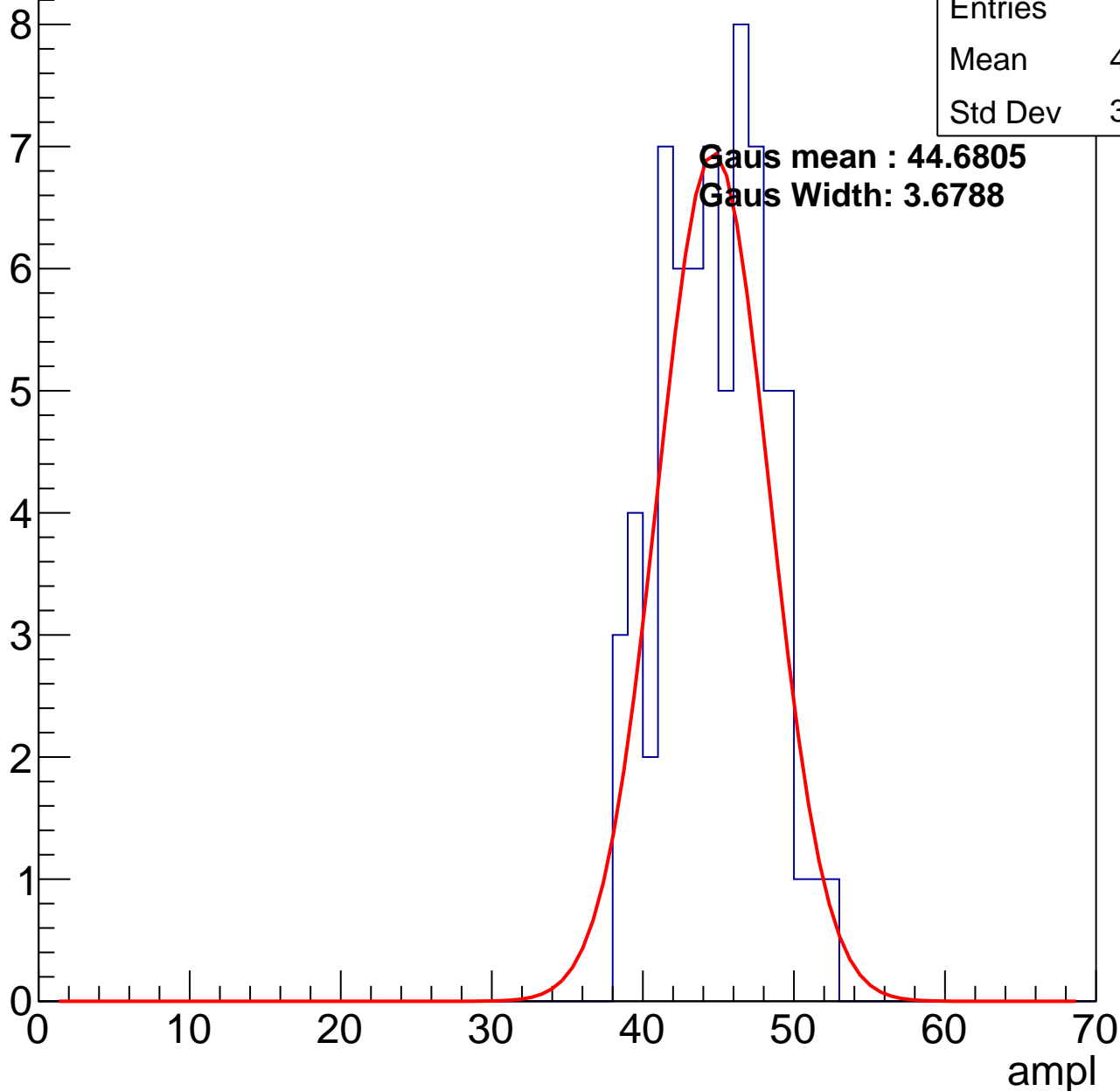
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	44.34
Std Dev	3.385

Gaus mean : 44.6805

Gaus Width: 3.6788

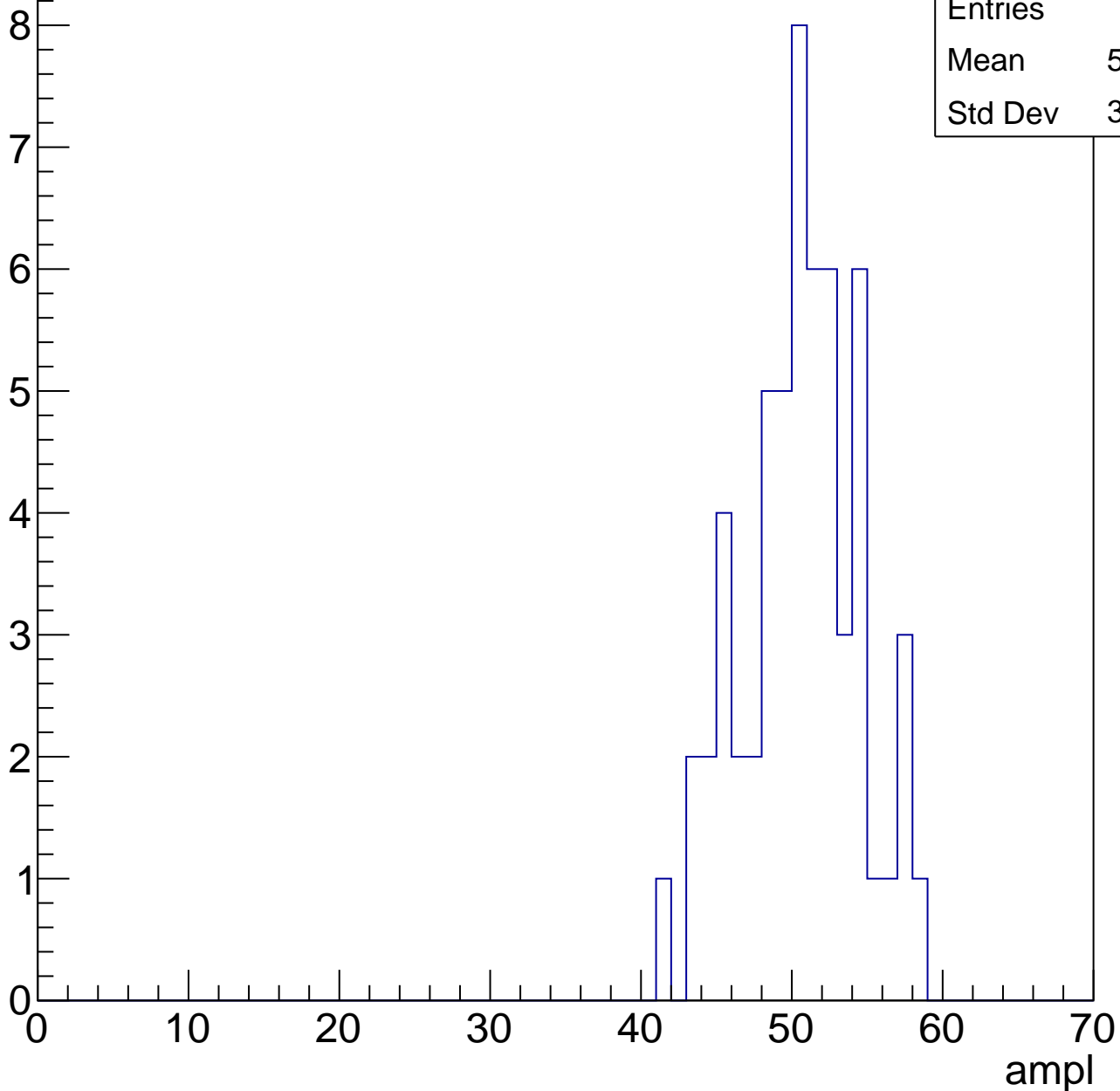


# B0L001S, U17-ch69, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	50.12
Std Dev	3.829

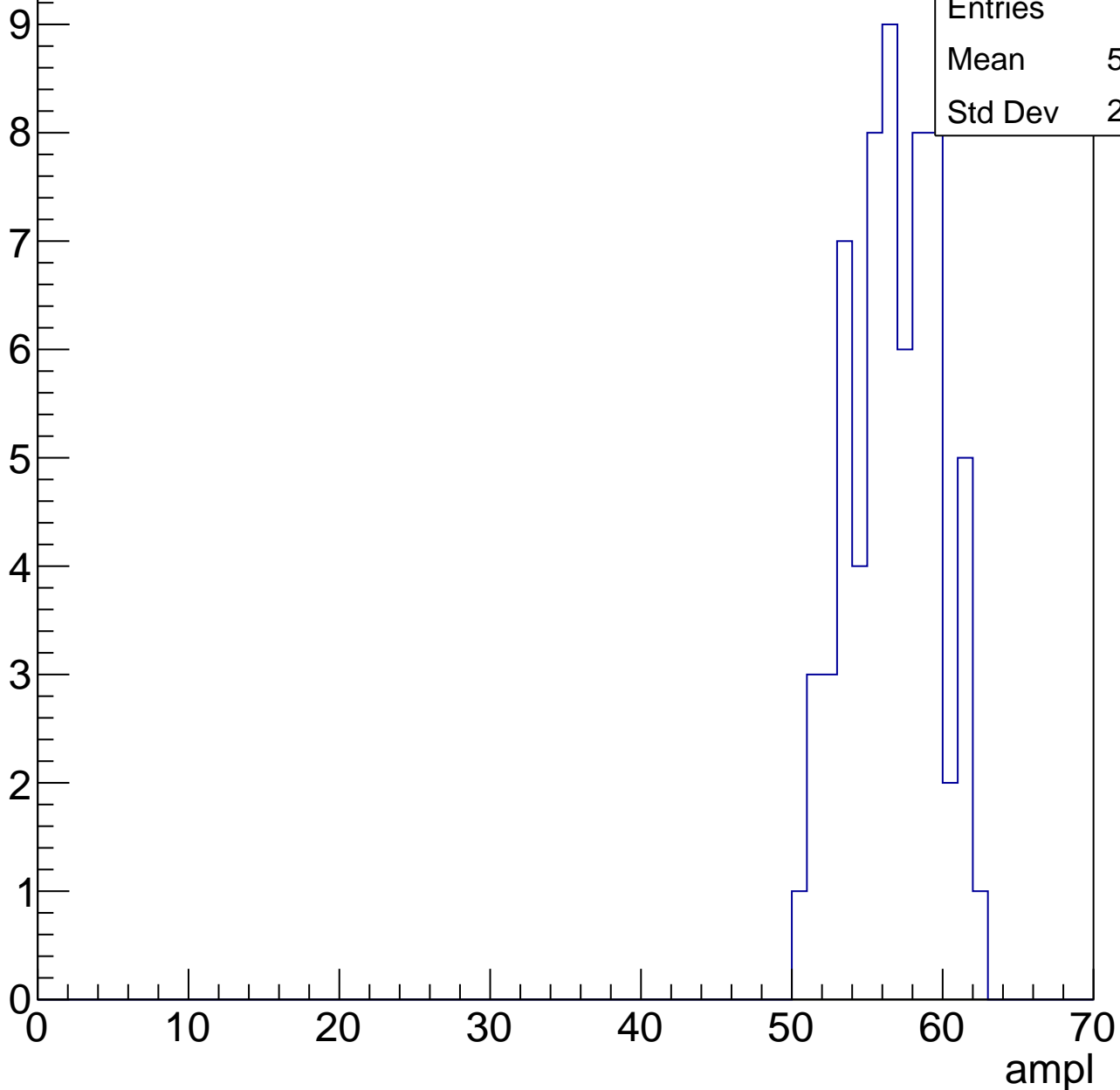


# B0L001S, U17-ch69, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	56.23
Std Dev	2.897

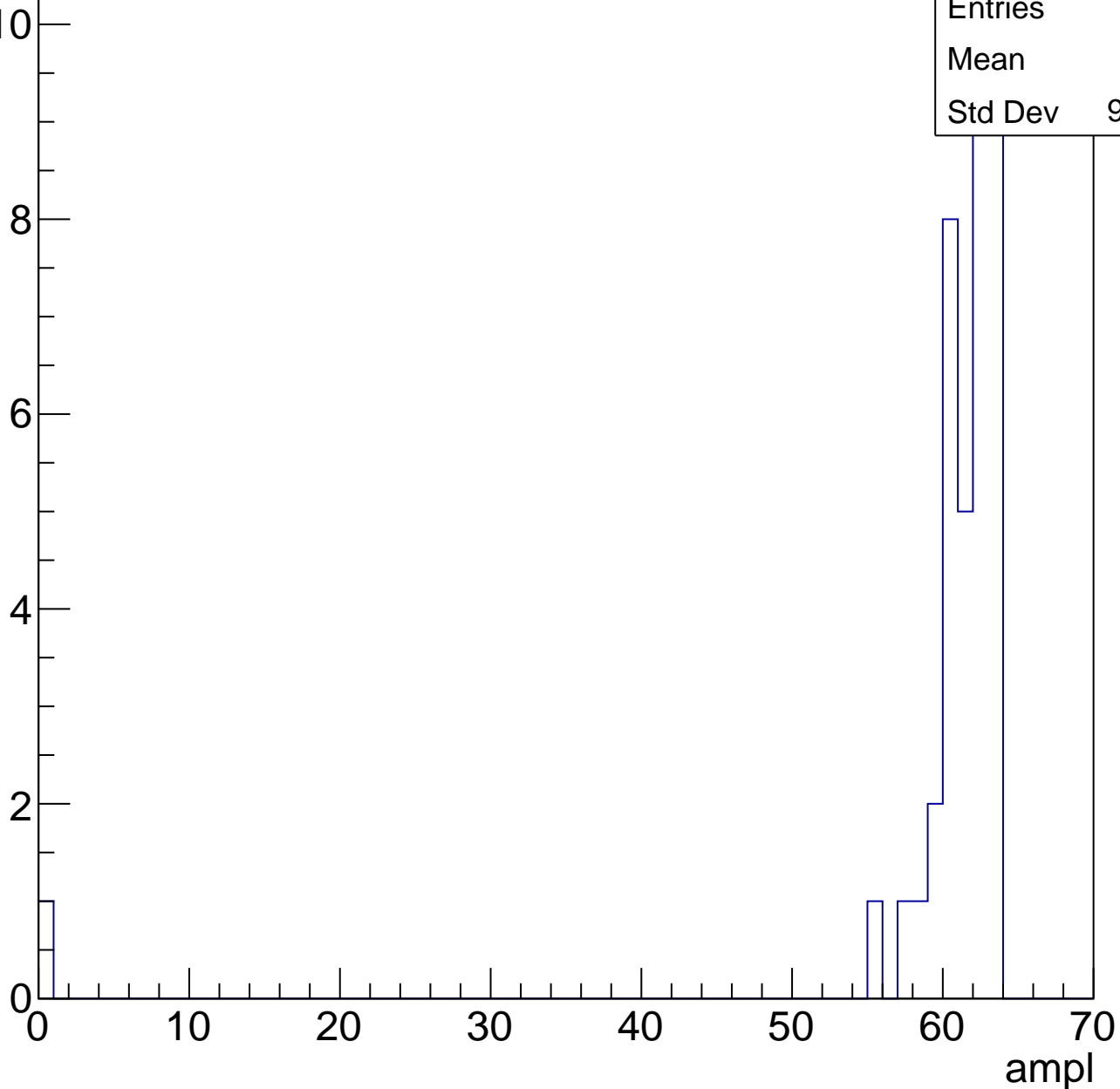


# B0L001S, U17-ch69, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	38
Mean	59.5
Std Dev	9.949



# B0L001S, U17-ch69, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U17-ch69, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U17-ch70, adc0

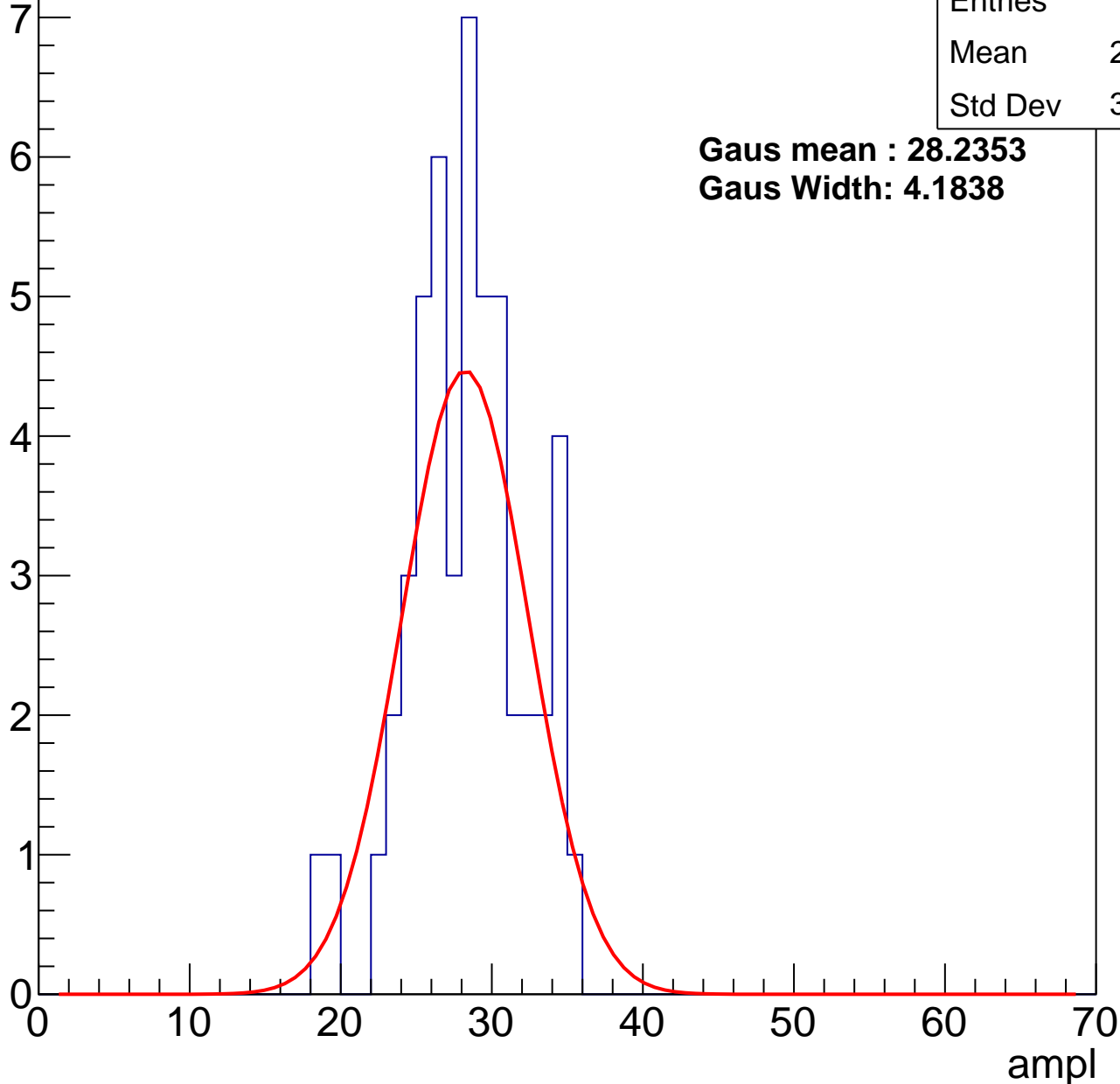
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	50
Mean	27.86
Std Dev	3.752

**Gaus mean : 28.2353**

**Gaus Width: 4.1838**



# B0L001S, U17-ch70, adc1

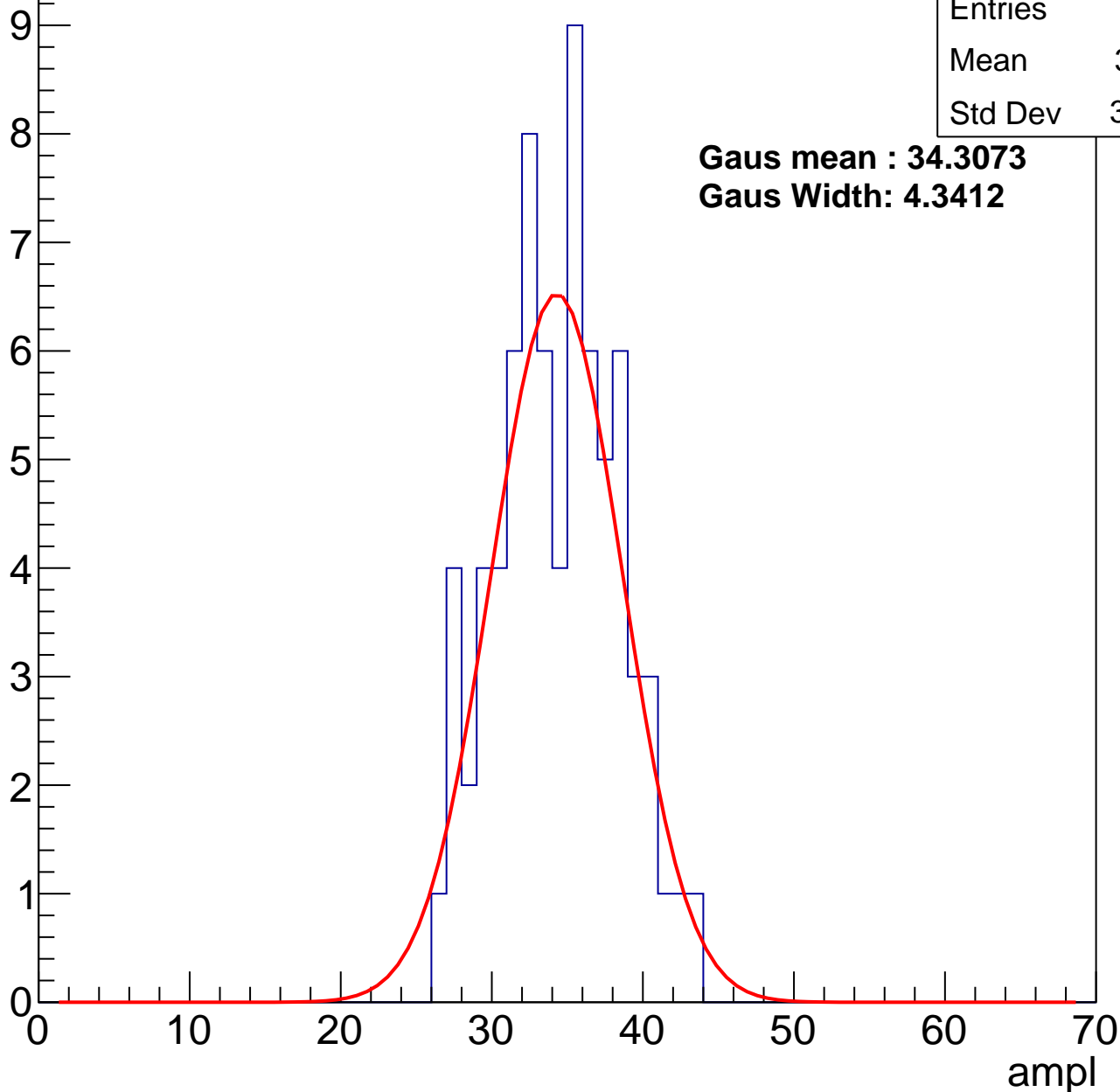
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	33.91
Std Dev	3.922

**Gaus mean : 34.3073**

**Gaus Width: 4.3412**



# B0L001S, U17-ch70, adc2

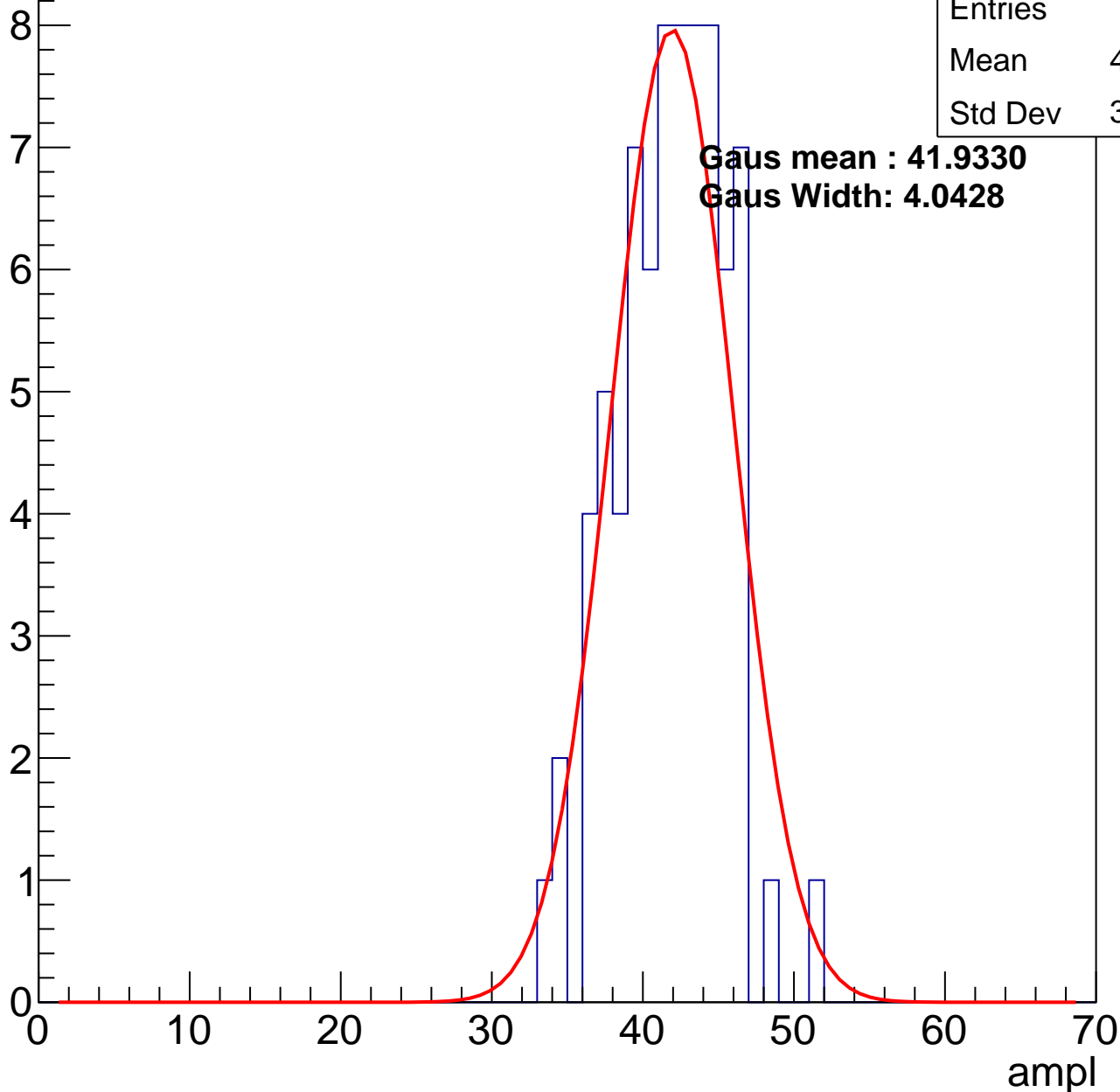
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	76
Mean	41.39
Std Dev	3.502

**Gaus mean : 41.9330**

**Gaus Width: 4.0428**



# B0L001S, U17-ch70, adc3

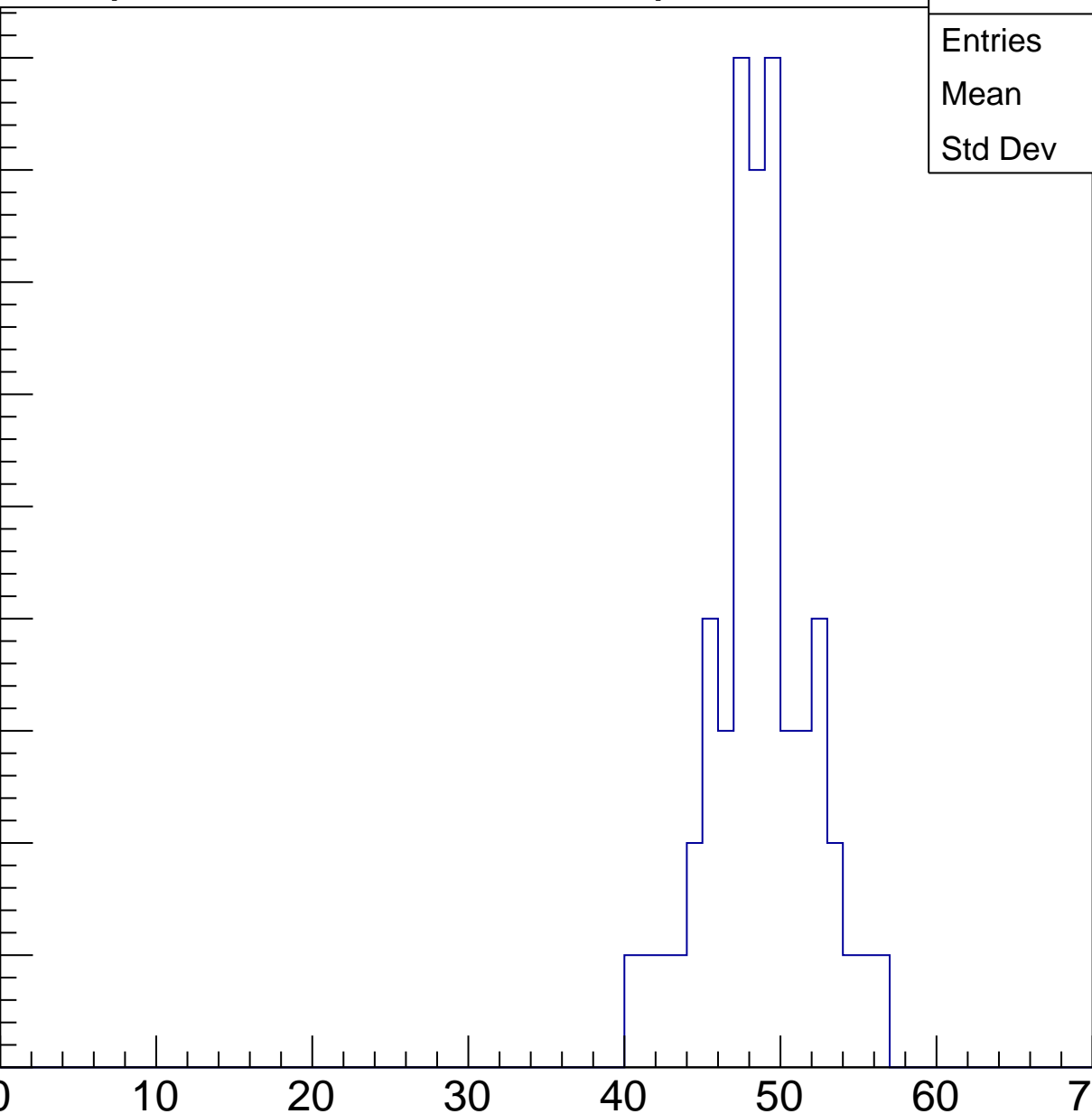
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	54
Mean	48.19
Std Dev	3.255

ampl

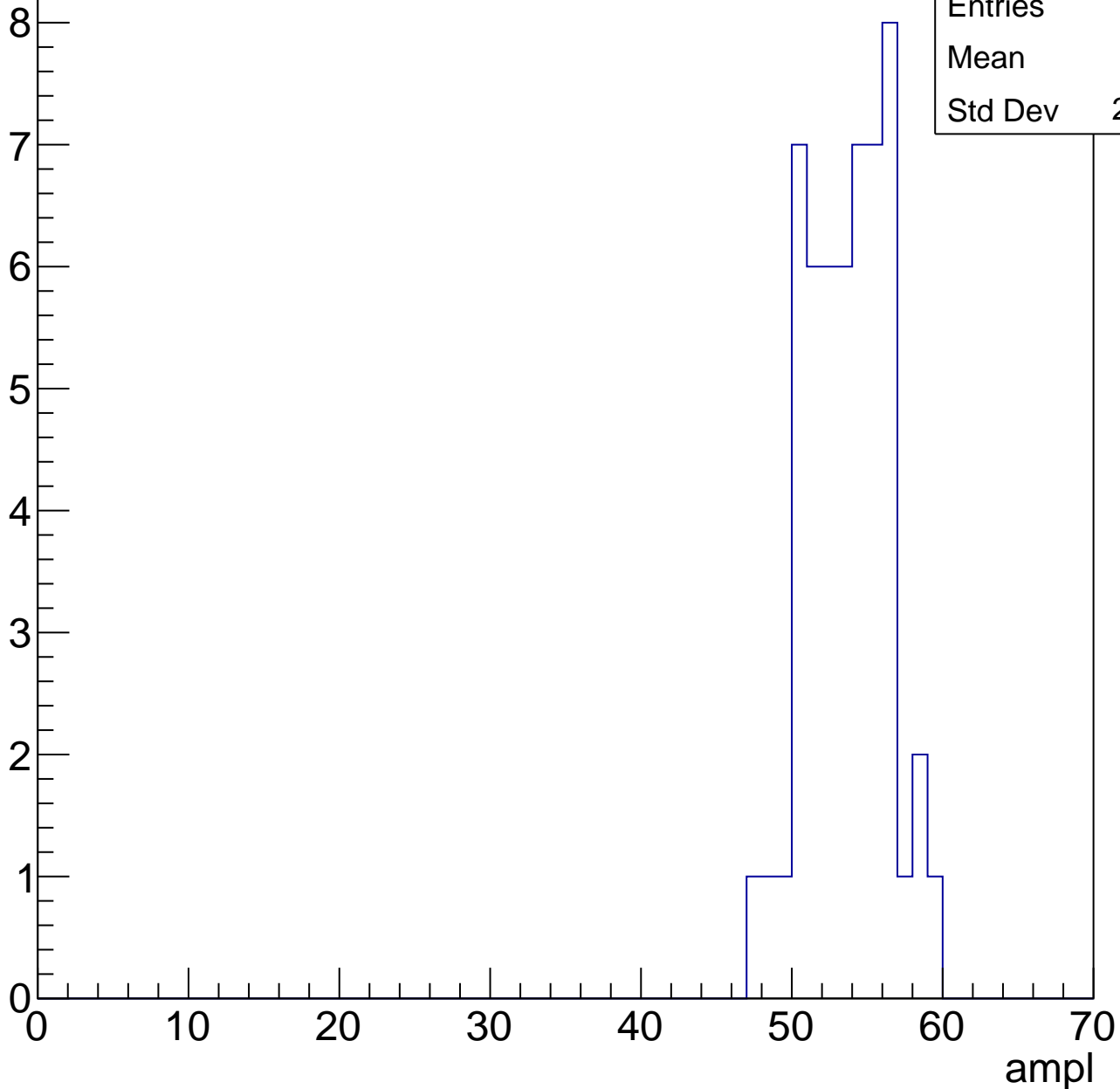


# B0L001S, U17-ch70, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

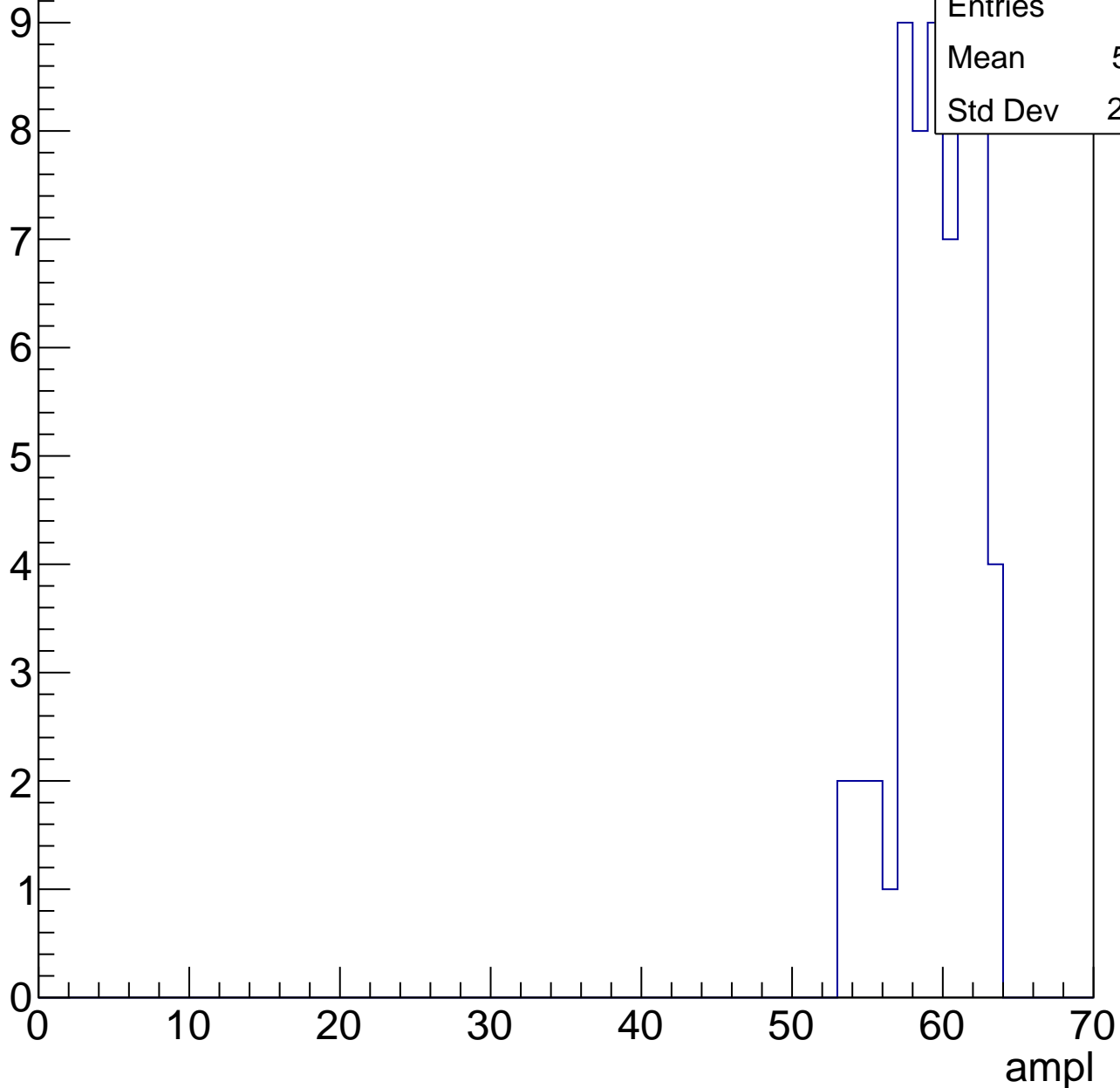
Entries	54
Mean	53.2
Std Dev	2.641



# B0L001S, U17-ch70, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

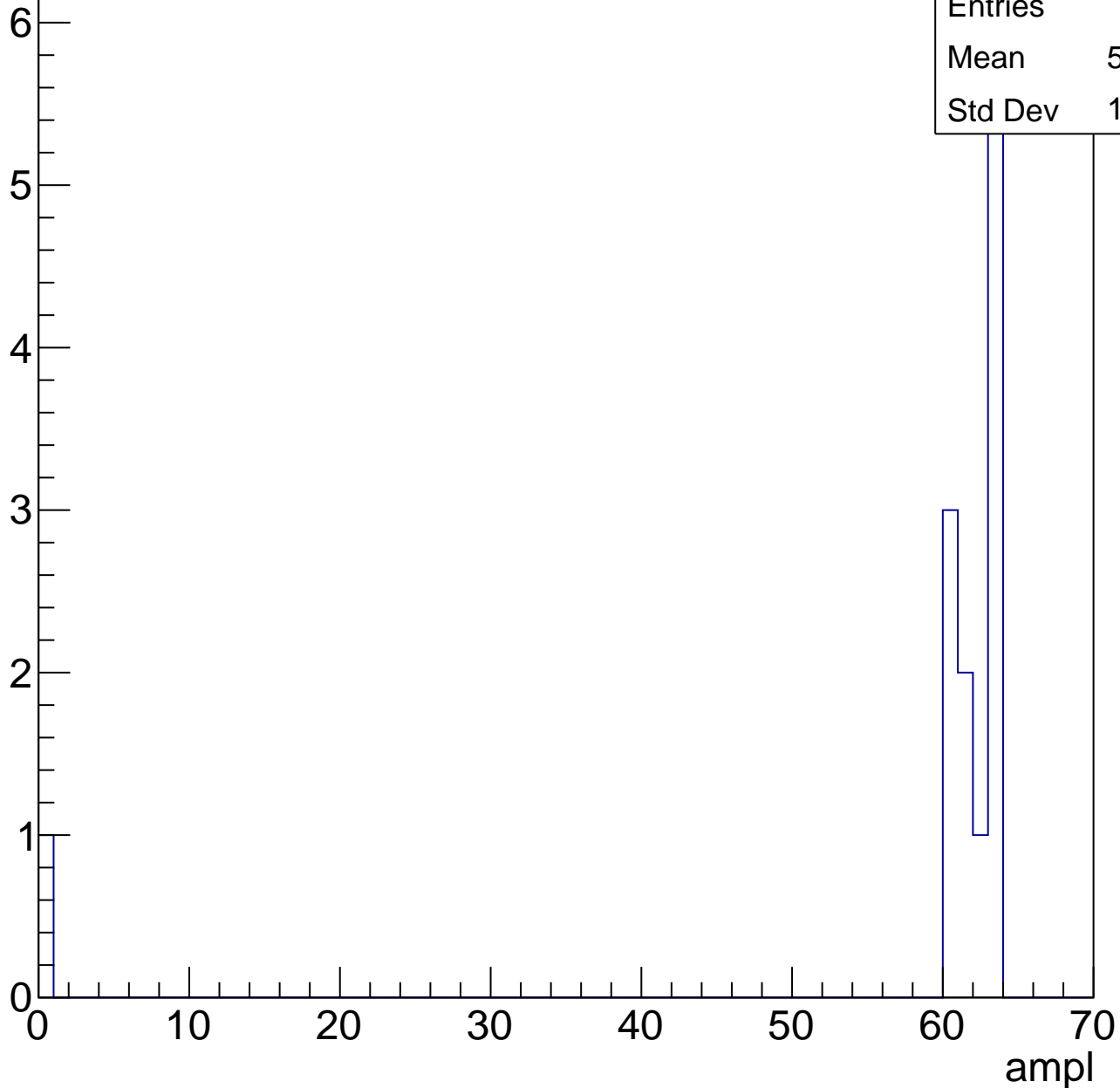


# B0L001S, U17-ch70, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	13
Mean	57.08
Std Dev	16.52





# B0L001S, U17-ch70, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U17-ch71, adc0

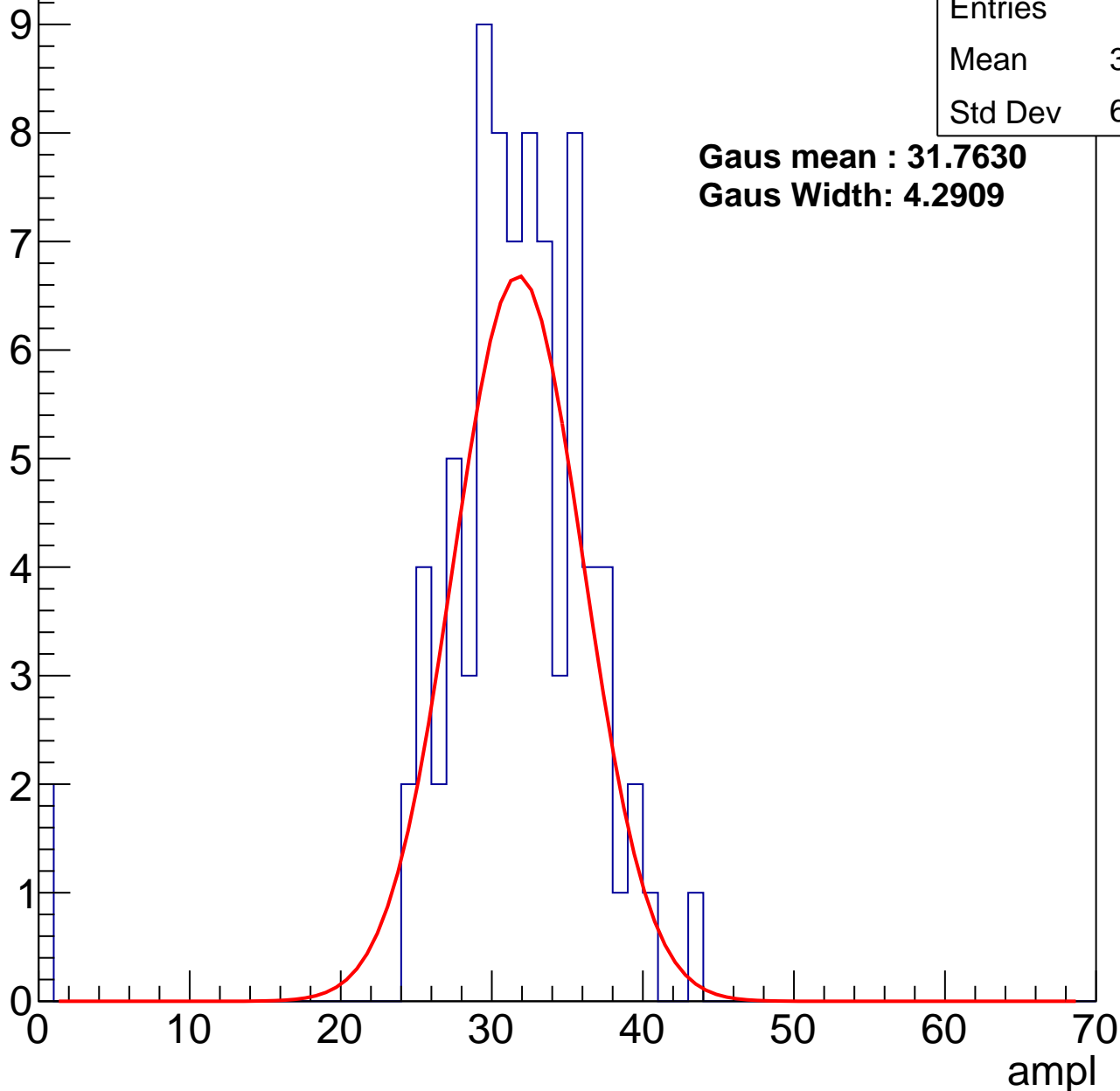
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	81
Mean	30.83
Std Dev	6.285

**Gaus mean : 31.7630**

**Gaus Width: 4.2909**



# B0L001S, U17-ch71, adc1

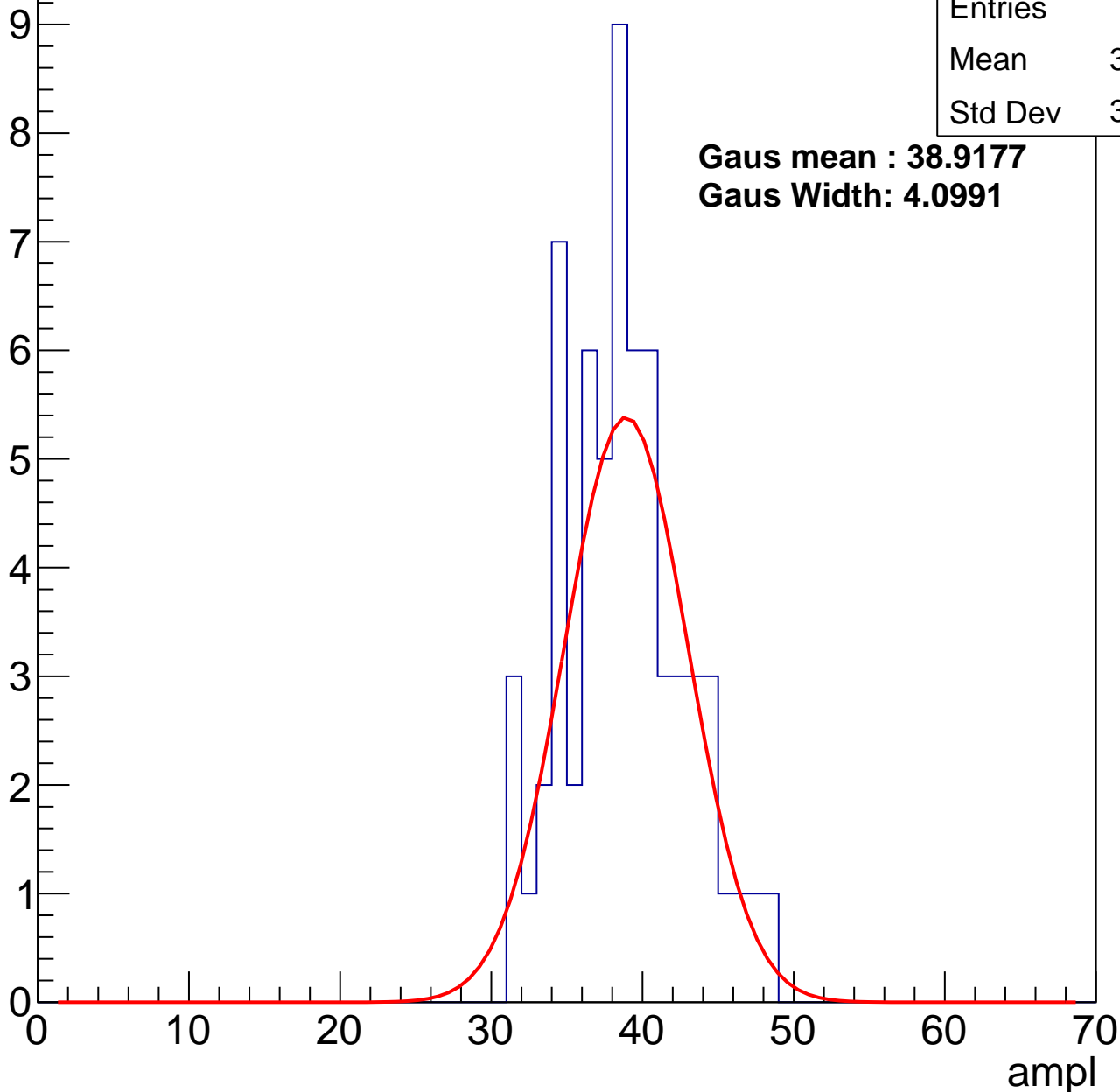
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	38.29
Std Dev	3.922

**Gaus mean : 38.9177**

**Gaus Width: 4.0991**



# B0L001S, U17-ch71, adc2

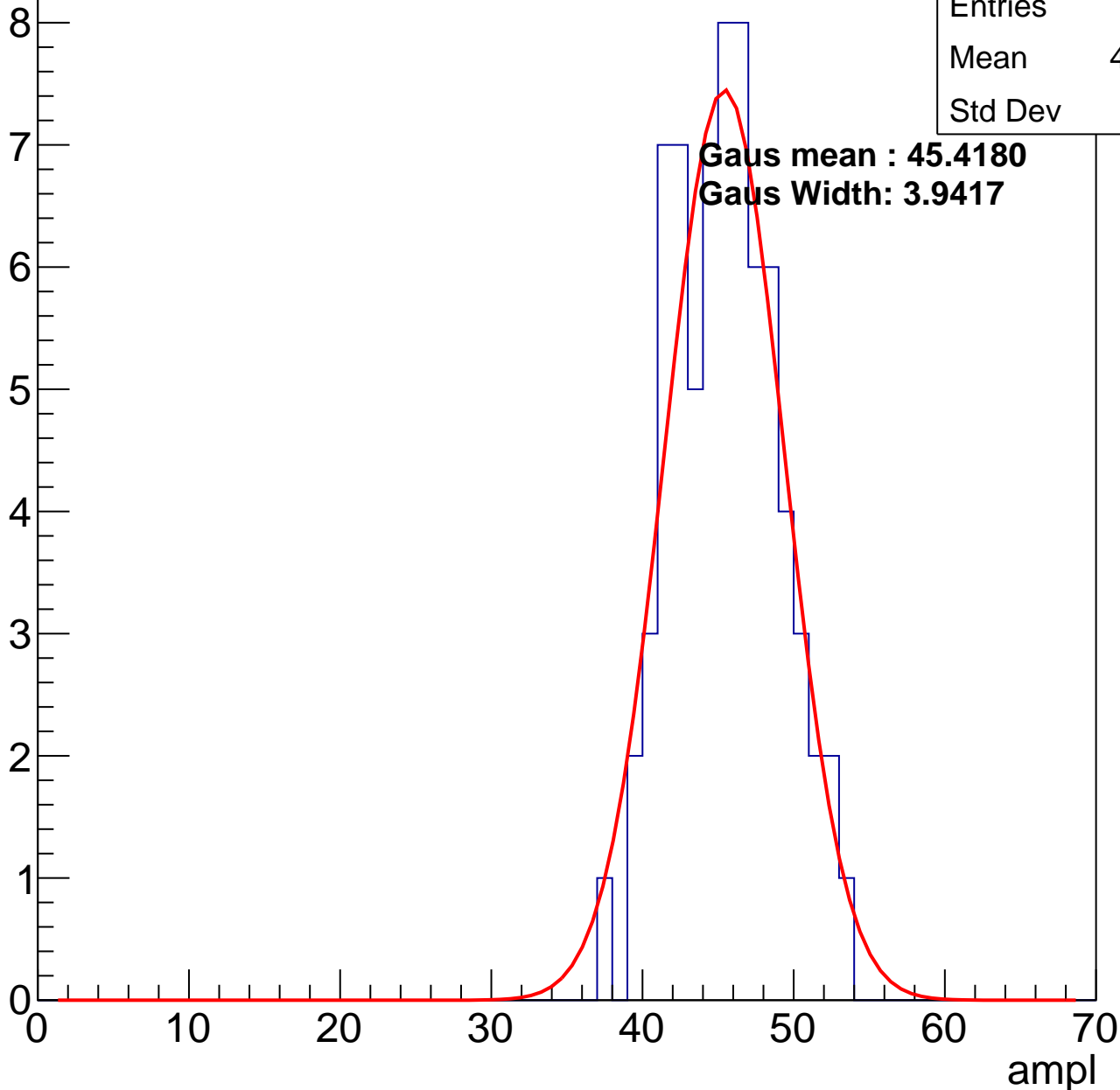
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	45.03
Std Dev	3.48

**Gaus mean : 45.4180**

**Gaus Width: 3.9417**

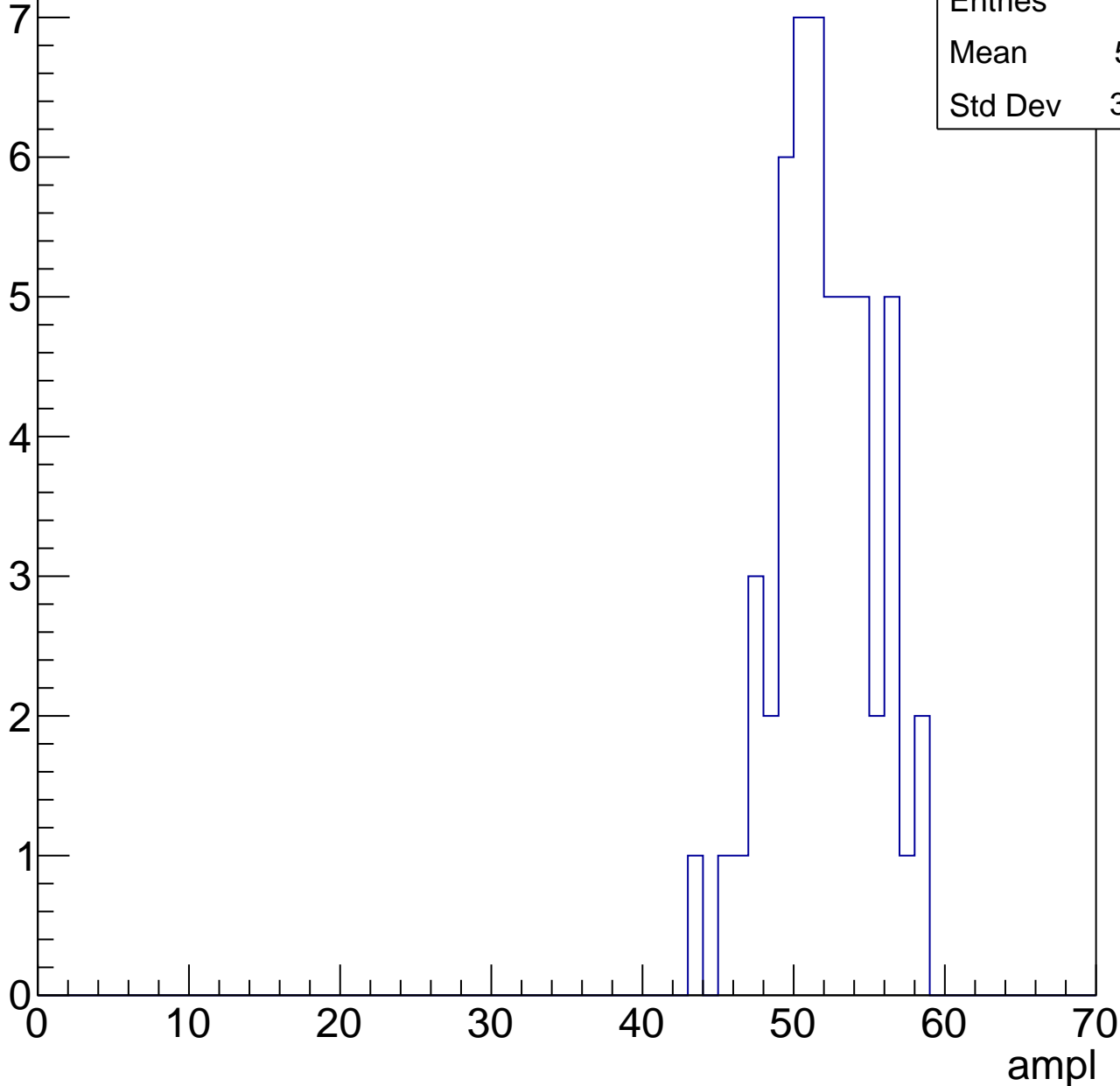


# B0L001S, U17-ch71, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	51.51
Std Dev	3.277

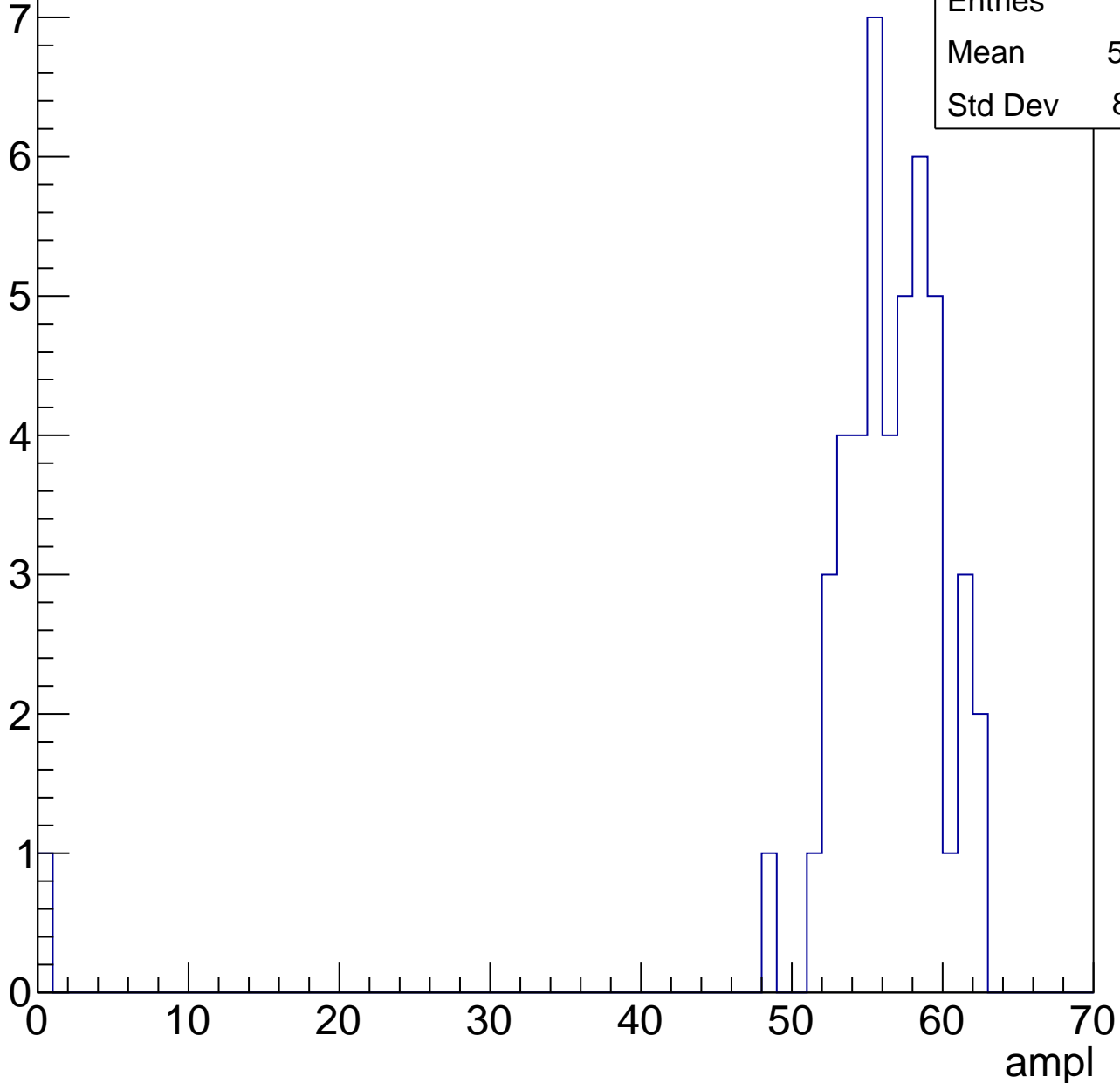


# B0L001S, U17-ch71, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

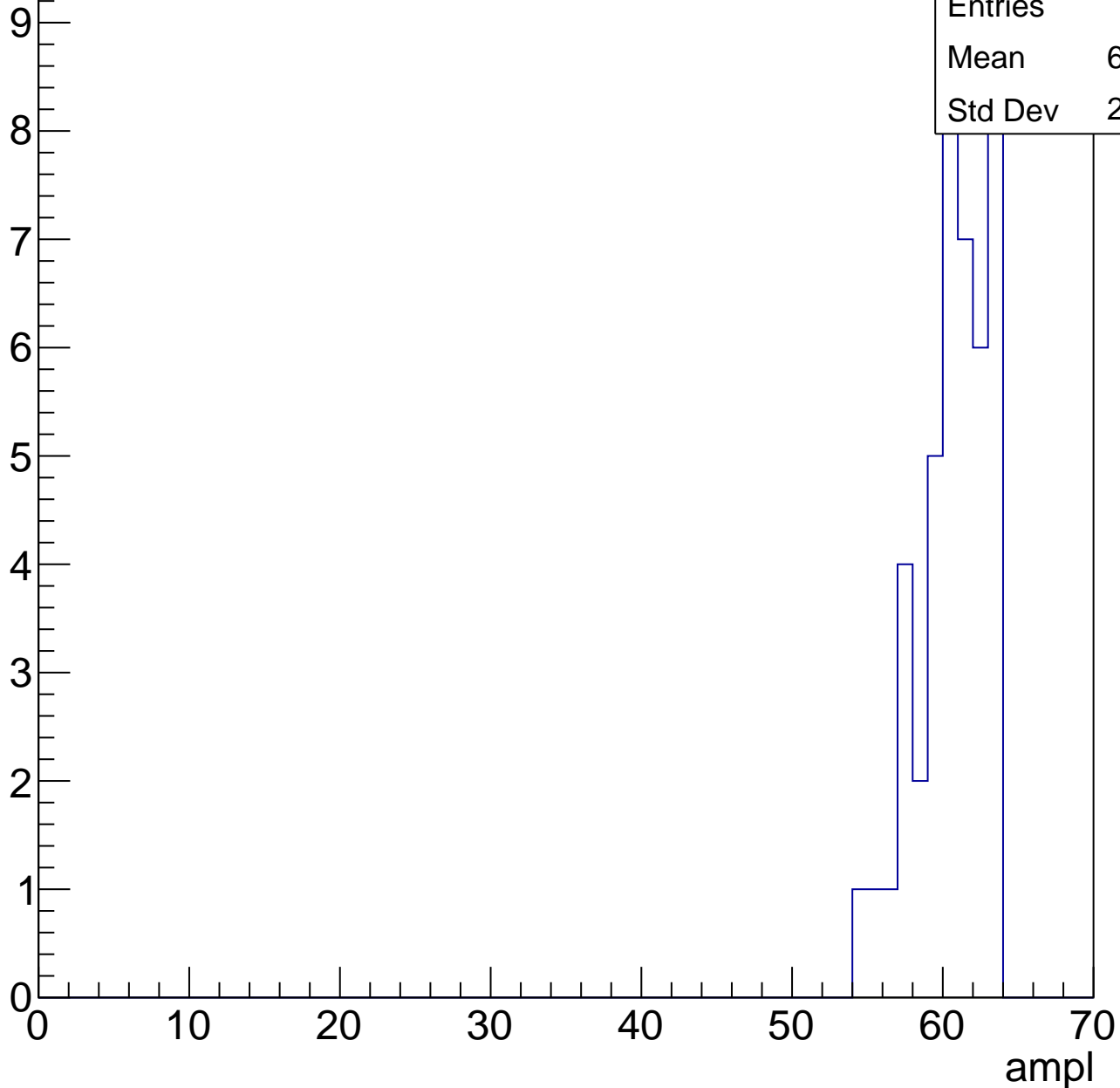
Entries	47
Mean	55.04
Std Dev	8.661



# B0L001S, U17-ch71, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U17-ch71, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch71, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	24
Std Dev	0

ampl

0 10 20 30 40 50 60 70

# B0L001S, U17-ch72, adc0

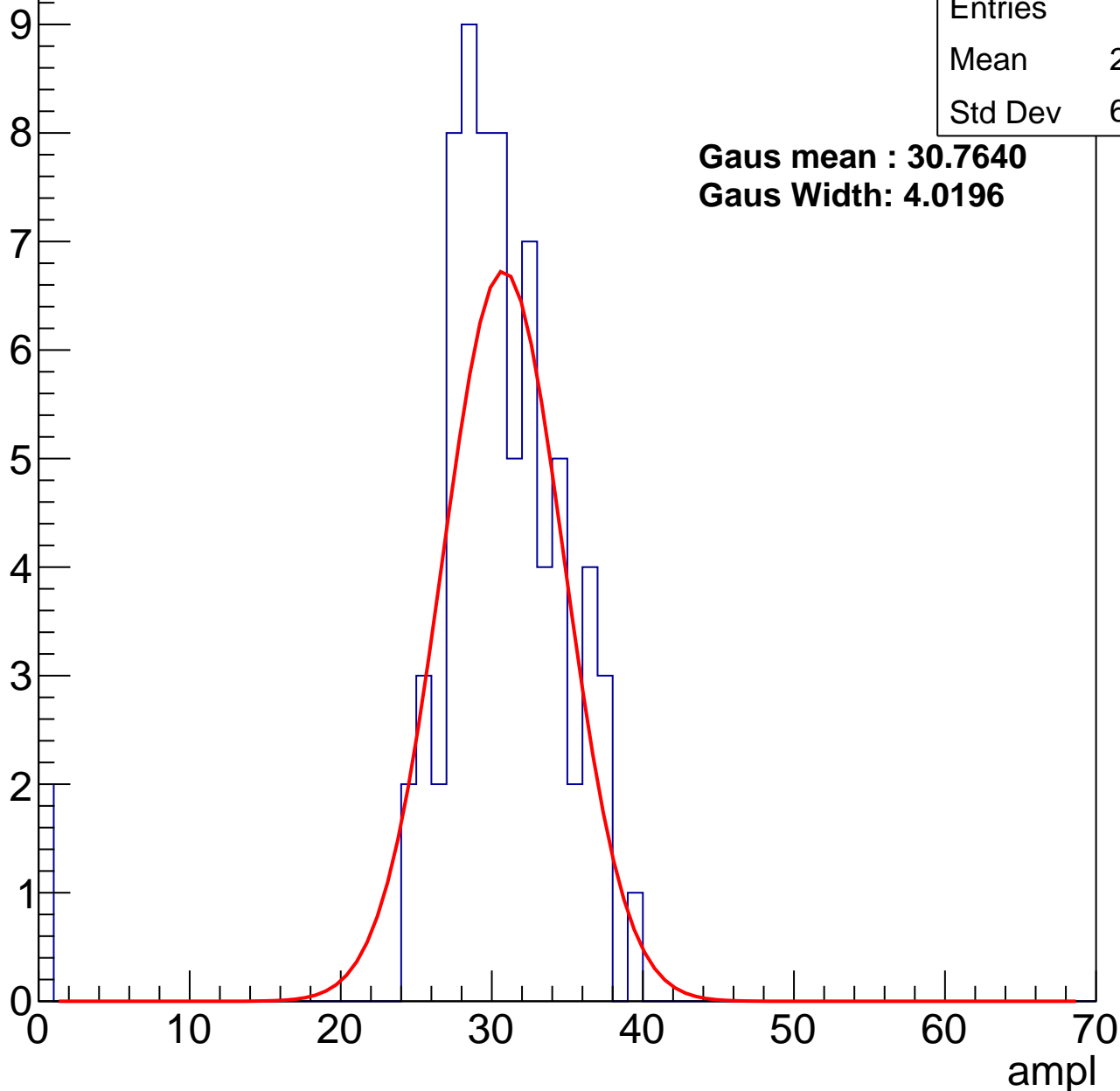
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	29.59
Std Dev	6.029

**Gaus mean : 30.7640**

**Gaus Width: 4.0196**



# B0L001S, U17-ch72, adc1

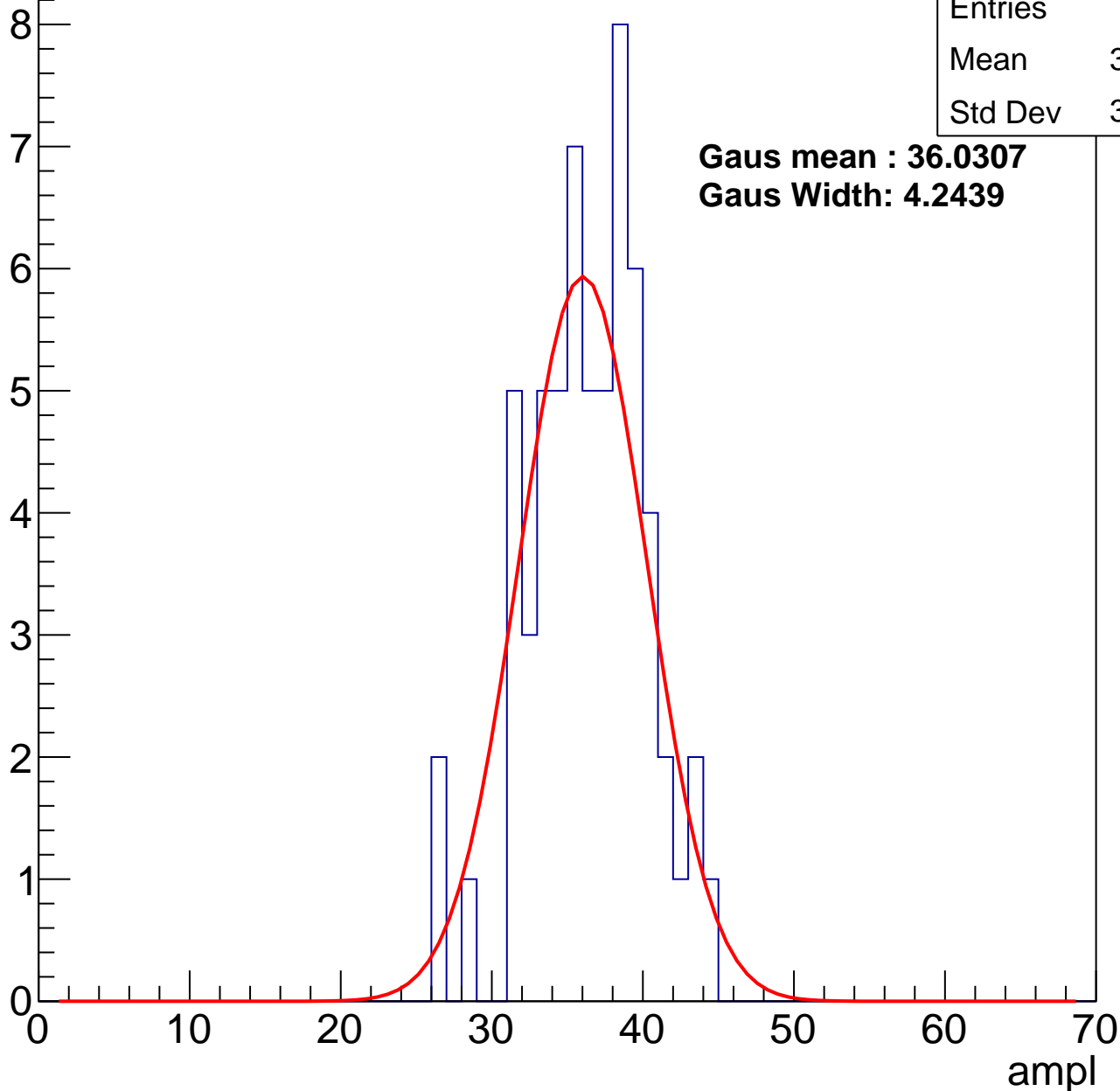
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	35.94
Std Dev	3.835

**Gaus mean : 36.0307**

**Gaus Width: 4.2439**



# B0L001S, U17-ch72, adc2

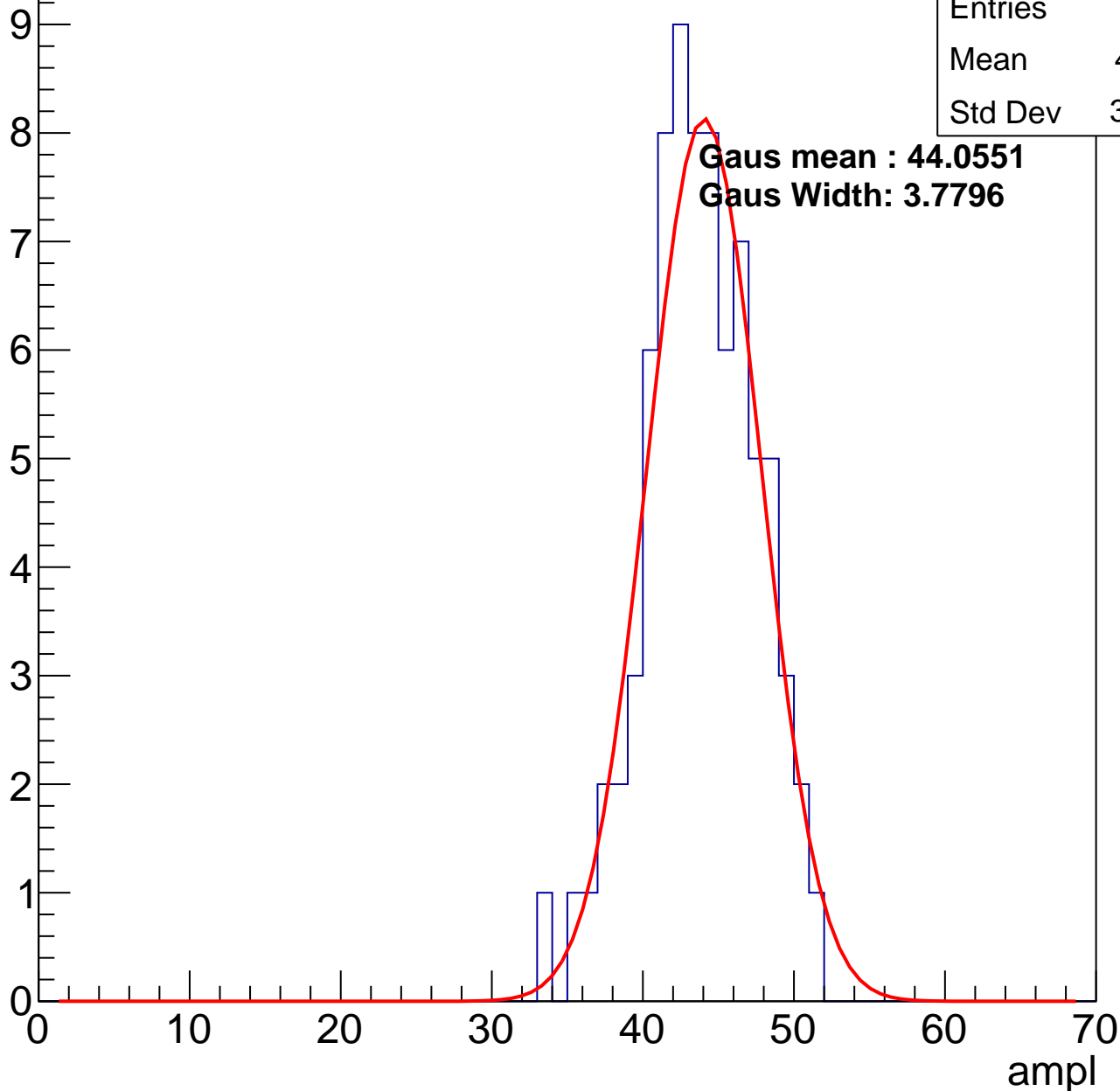
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	78
Mean	43.31
Std Dev	3.653

**Gaus mean : 44.0551**

**Gaus Width: 3.7796**

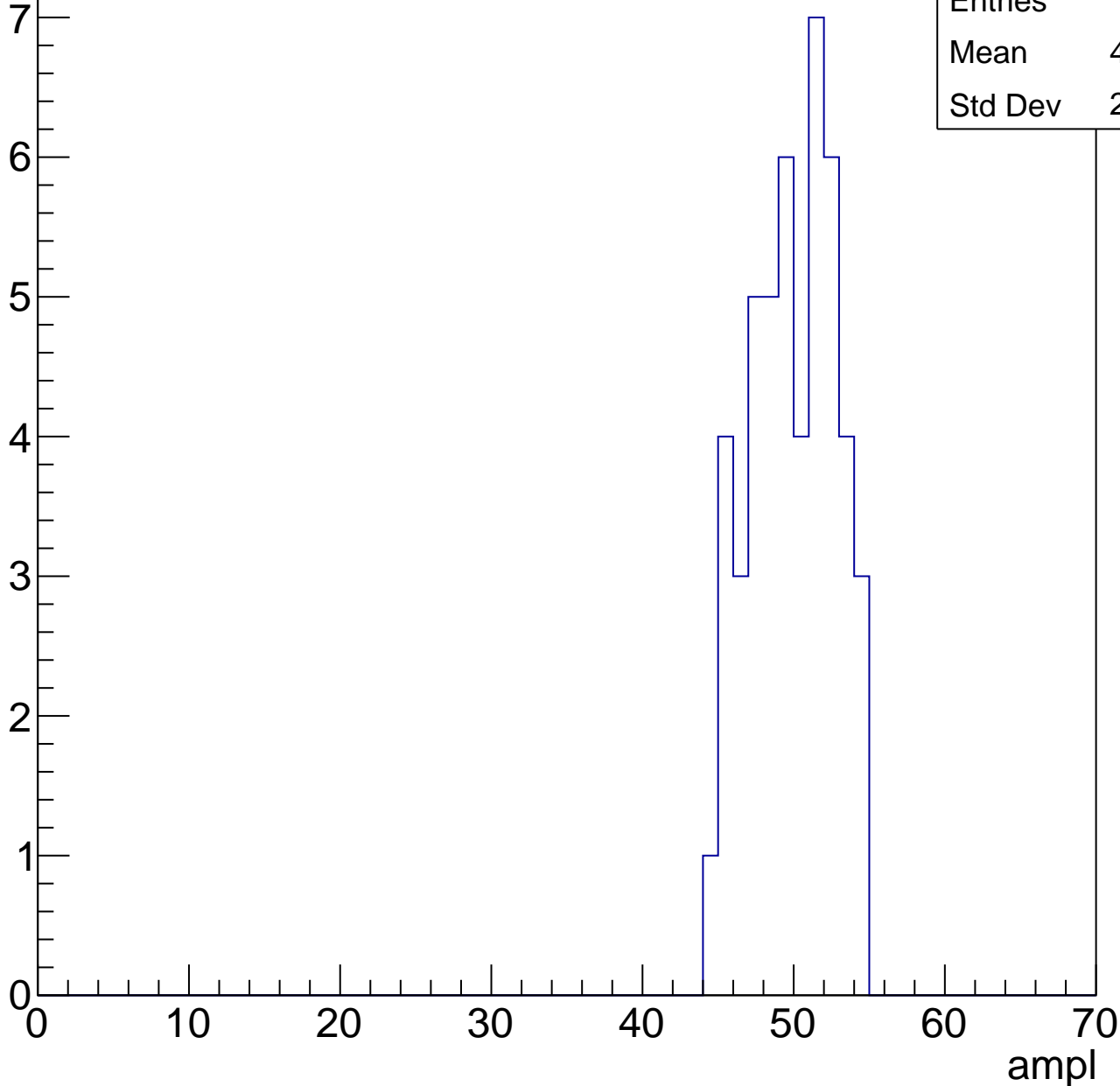


# B0L001S, U17-ch72, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	48
Mean	49.46
Std Dev	2.723

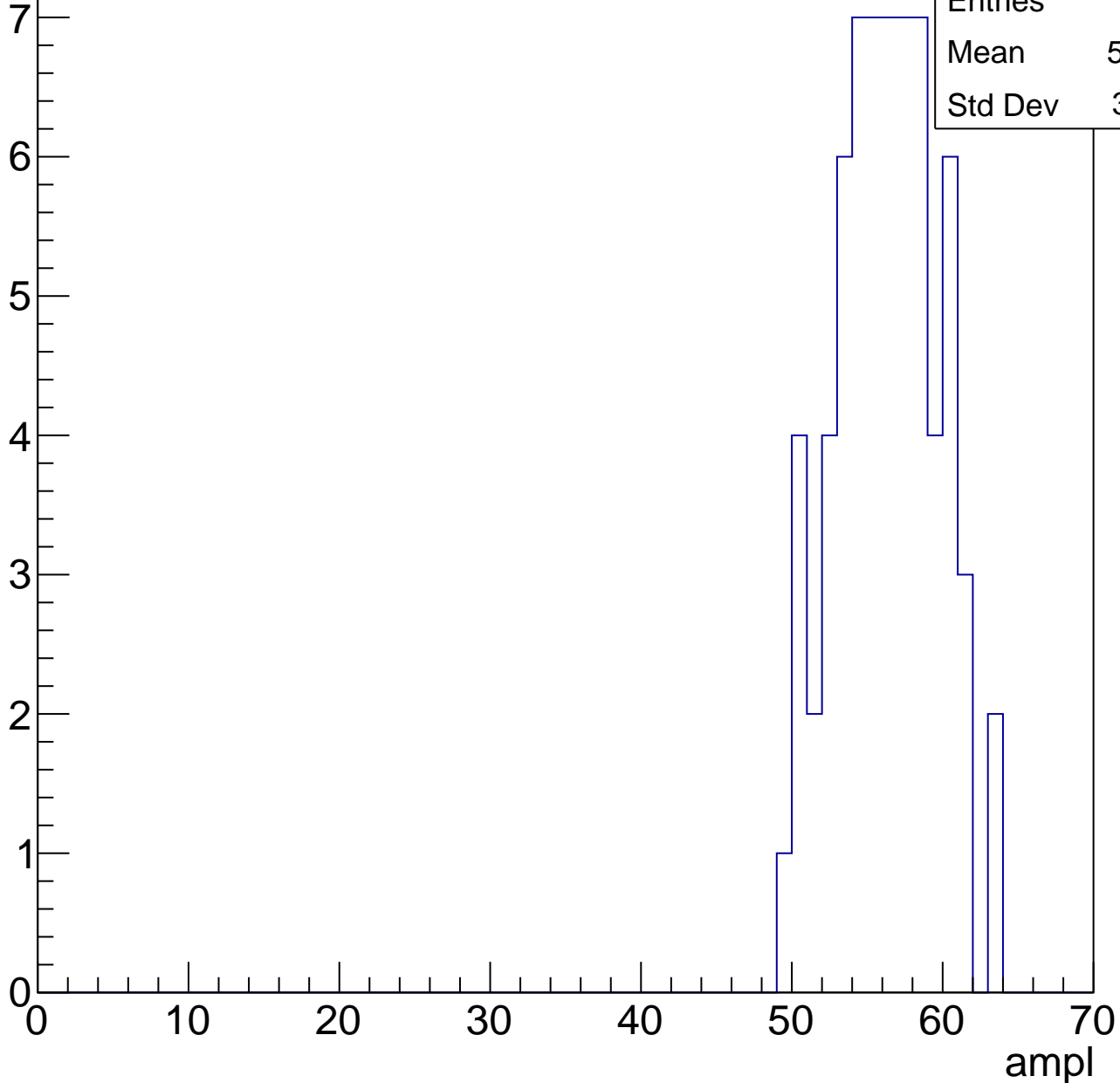


# B0L001S, U17-ch72, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	55.85
Std Dev	3.311

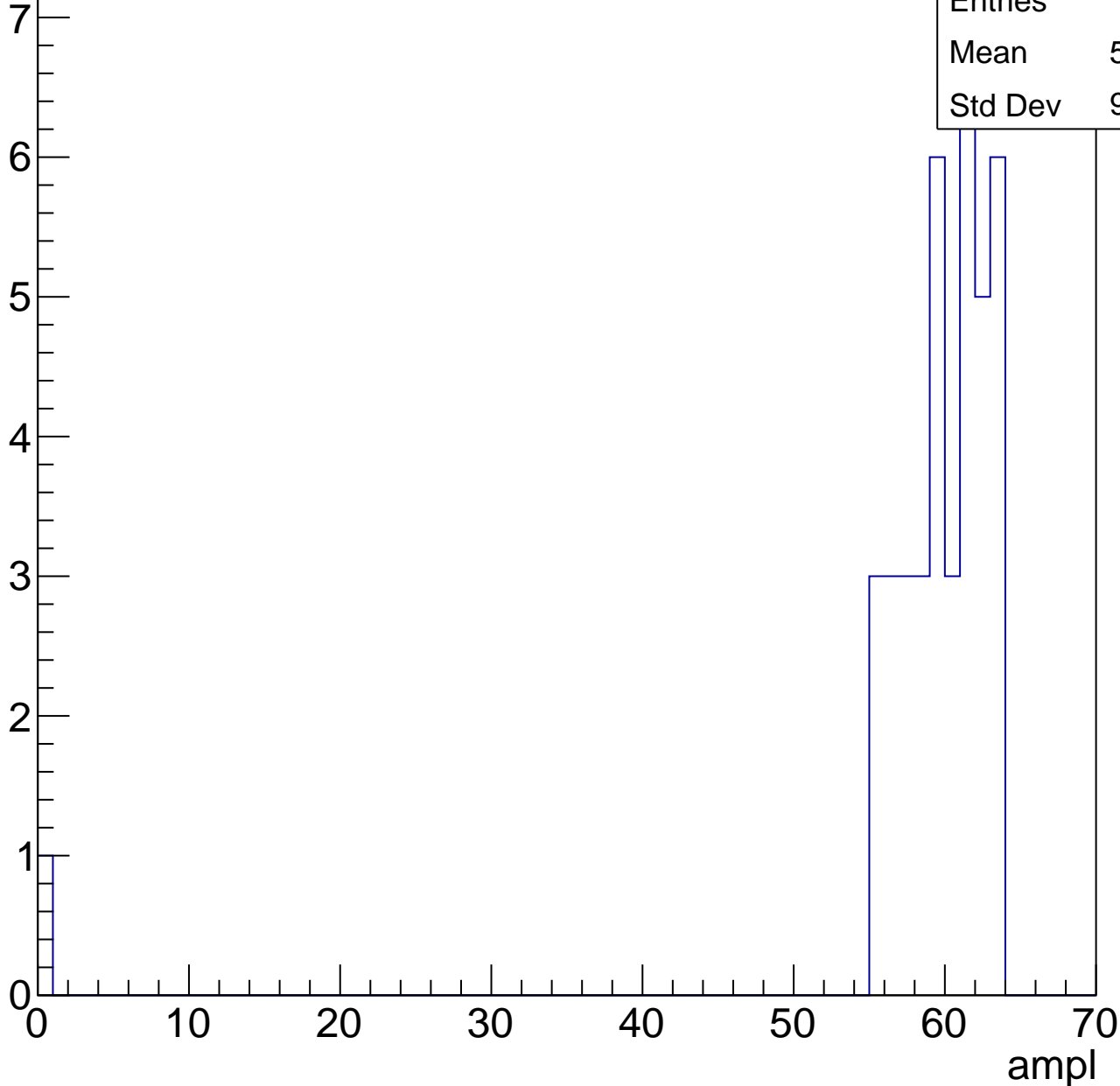


# B0L001S, U17-ch72, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	40
Mean	58.17
Std Dev	9.638

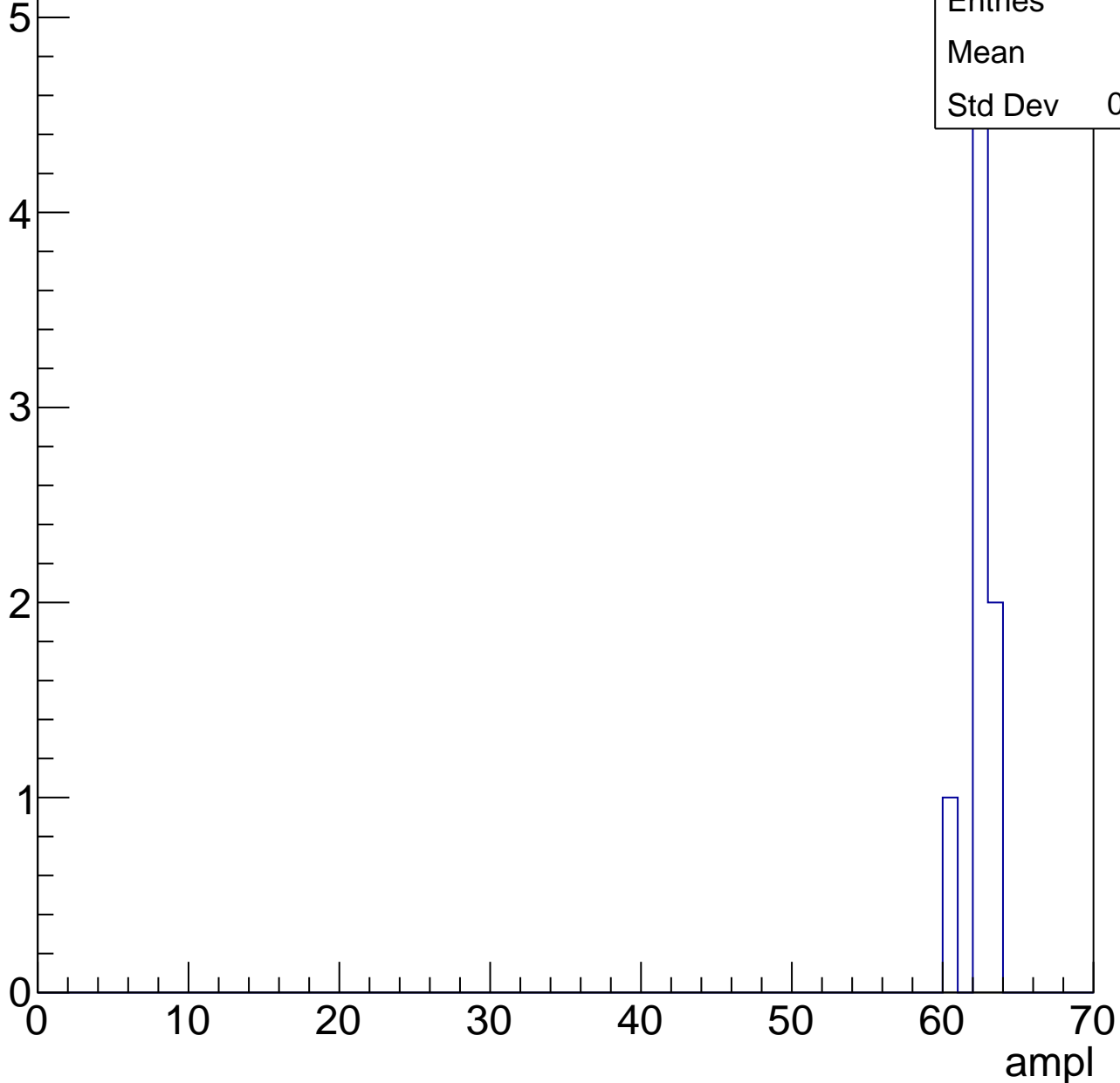


# B0L001S, U17-ch72, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	8
Mean	62
Std Dev	0.866





# B0L001S, U17-ch72, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



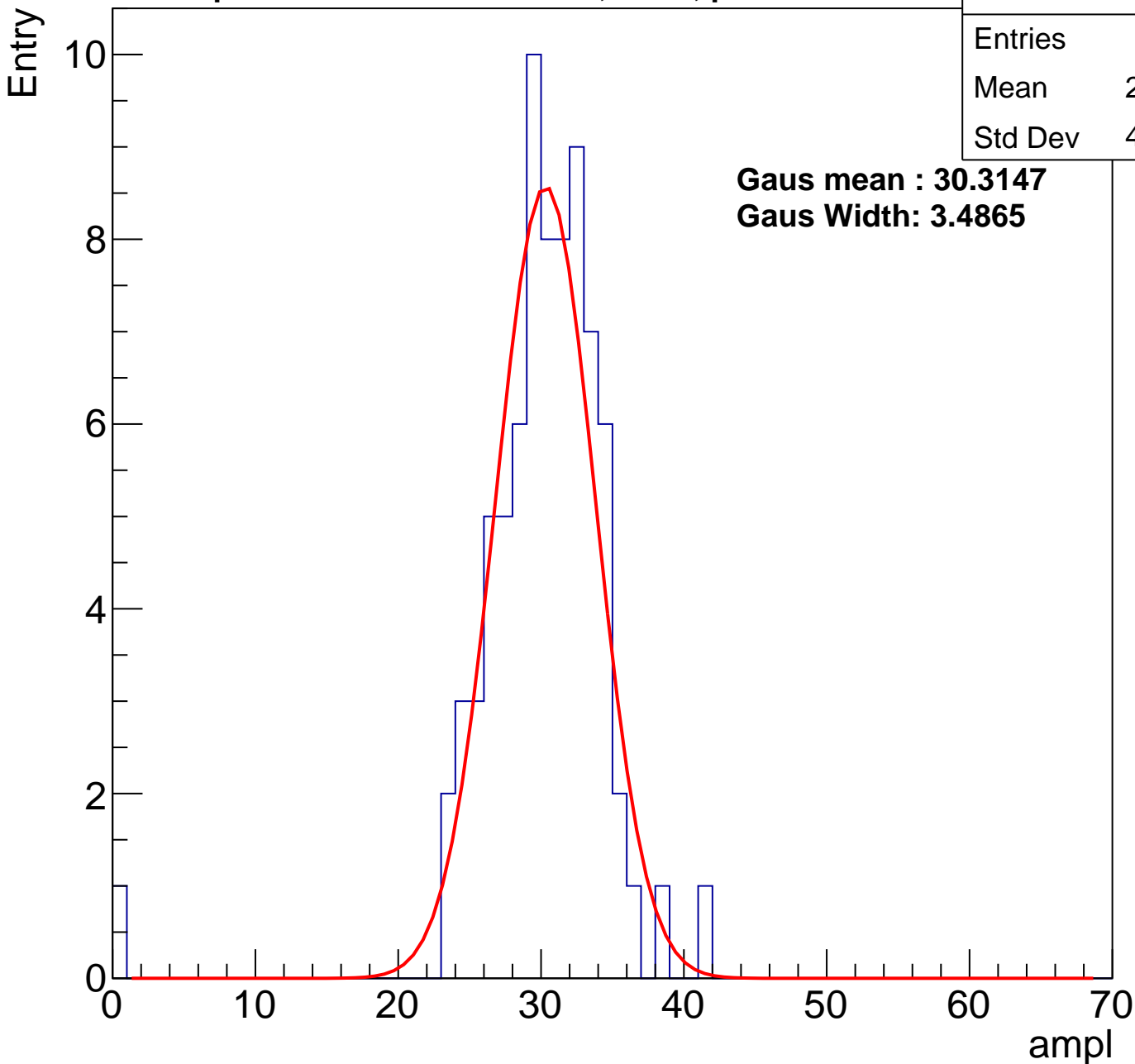
Entries	1
Mean	0
Std Dev	0

# B0L001S, U17-ch73, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	78
Mean	29.64
Std Dev	4.809

**Gaus mean : 30.3147**  
**Gaus Width: 3.4865**



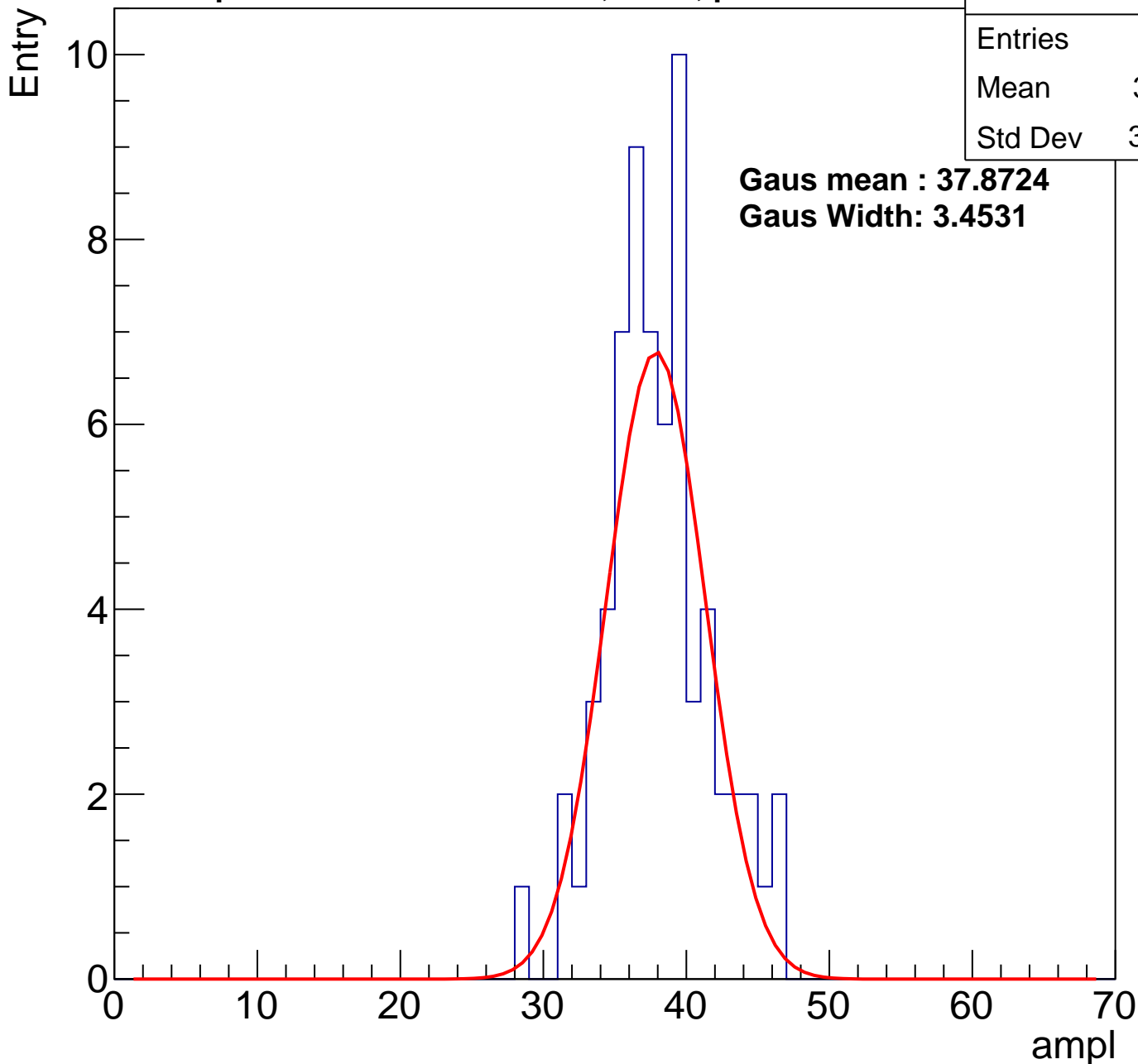
# B0L001S, U17-ch73, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	66
Mean	37.61
Std Dev	3.605

**Gaus mean : 37.8724**

**Gaus Width: 3.4531**



# B0L001S, U17-ch73, adc2

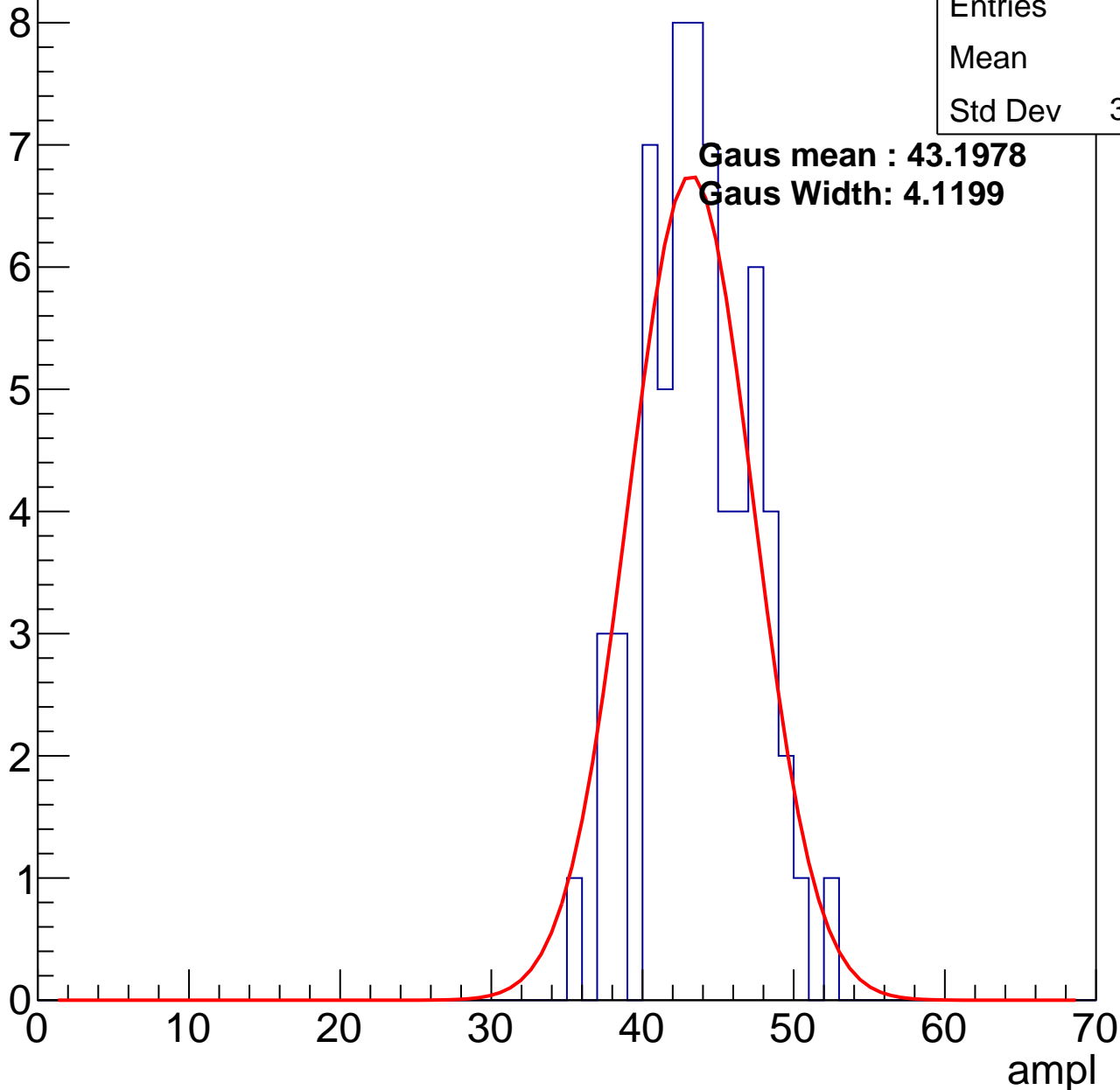
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	43.3
Std Dev	3.512

**Gaus mean : 43.1978**

**Gaus Width: 4.1199**

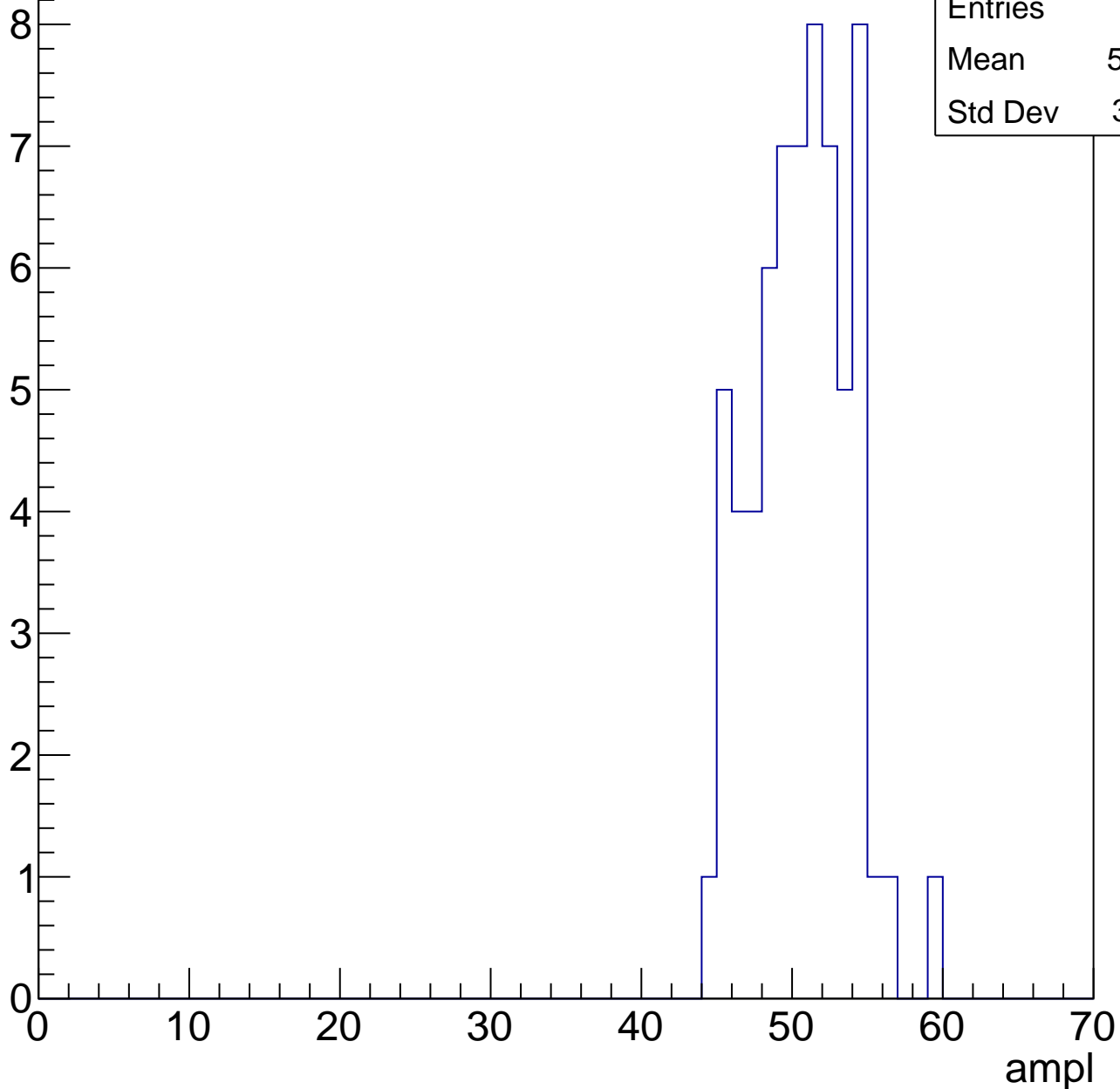


# B0L001S, U17-ch73, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	50.17
Std Dev	3.141

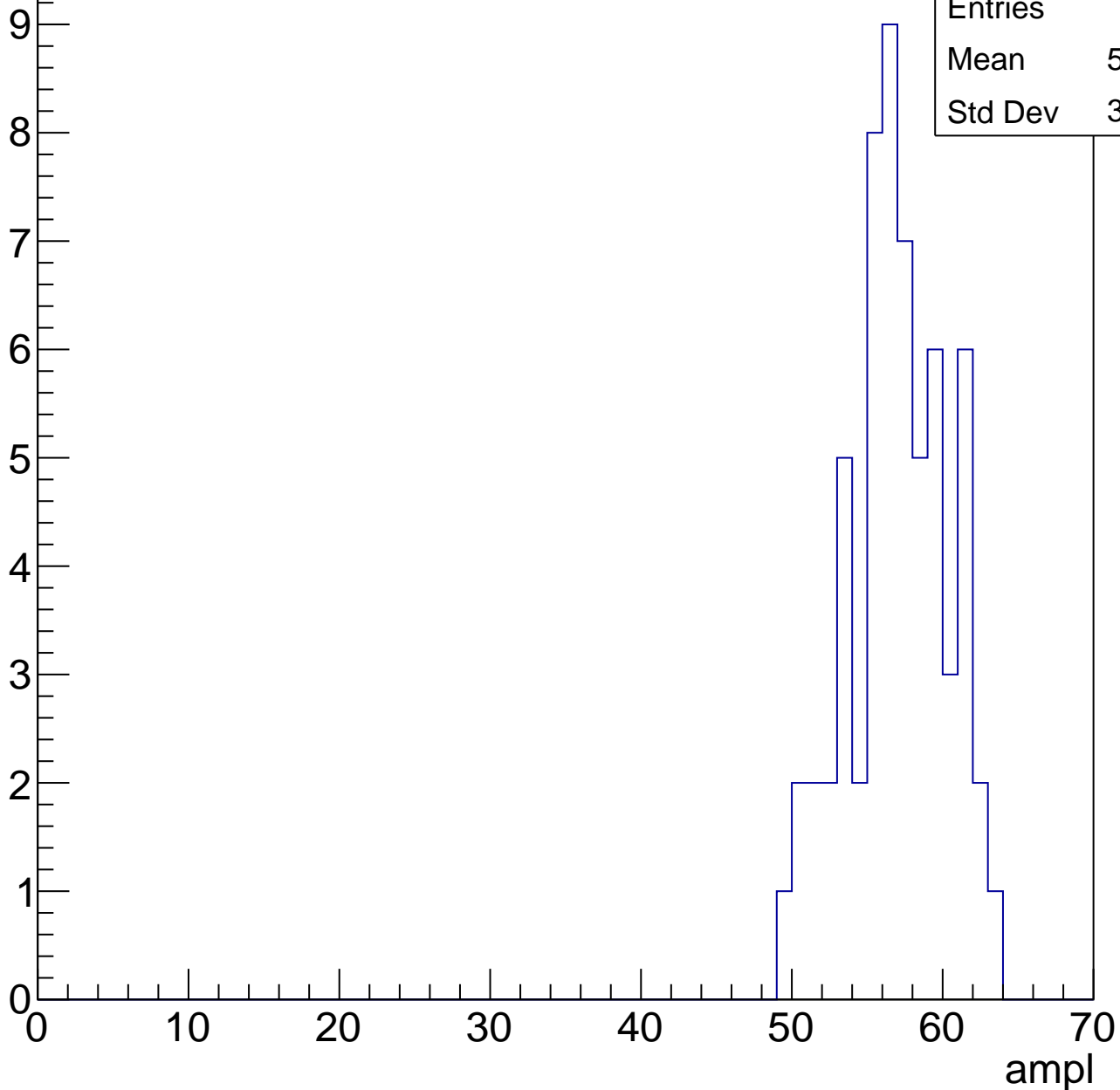


# B0L001S, U17-ch73, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	56.52
Std Dev	3.257

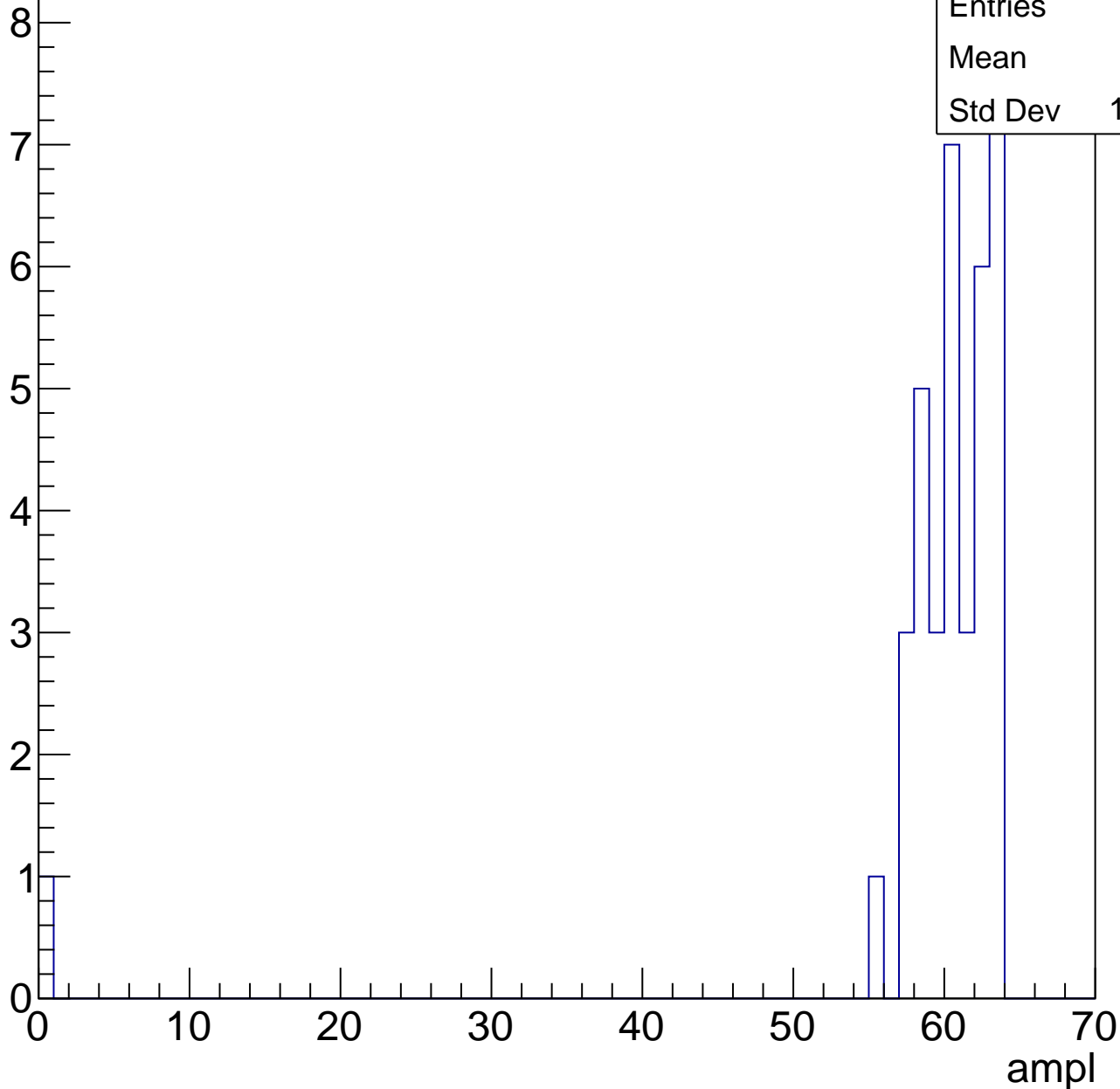


# B0L001S, U17-ch73, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	37
Mean	58.7
Std Dev	10.02



# B0L001S, U17-ch73, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



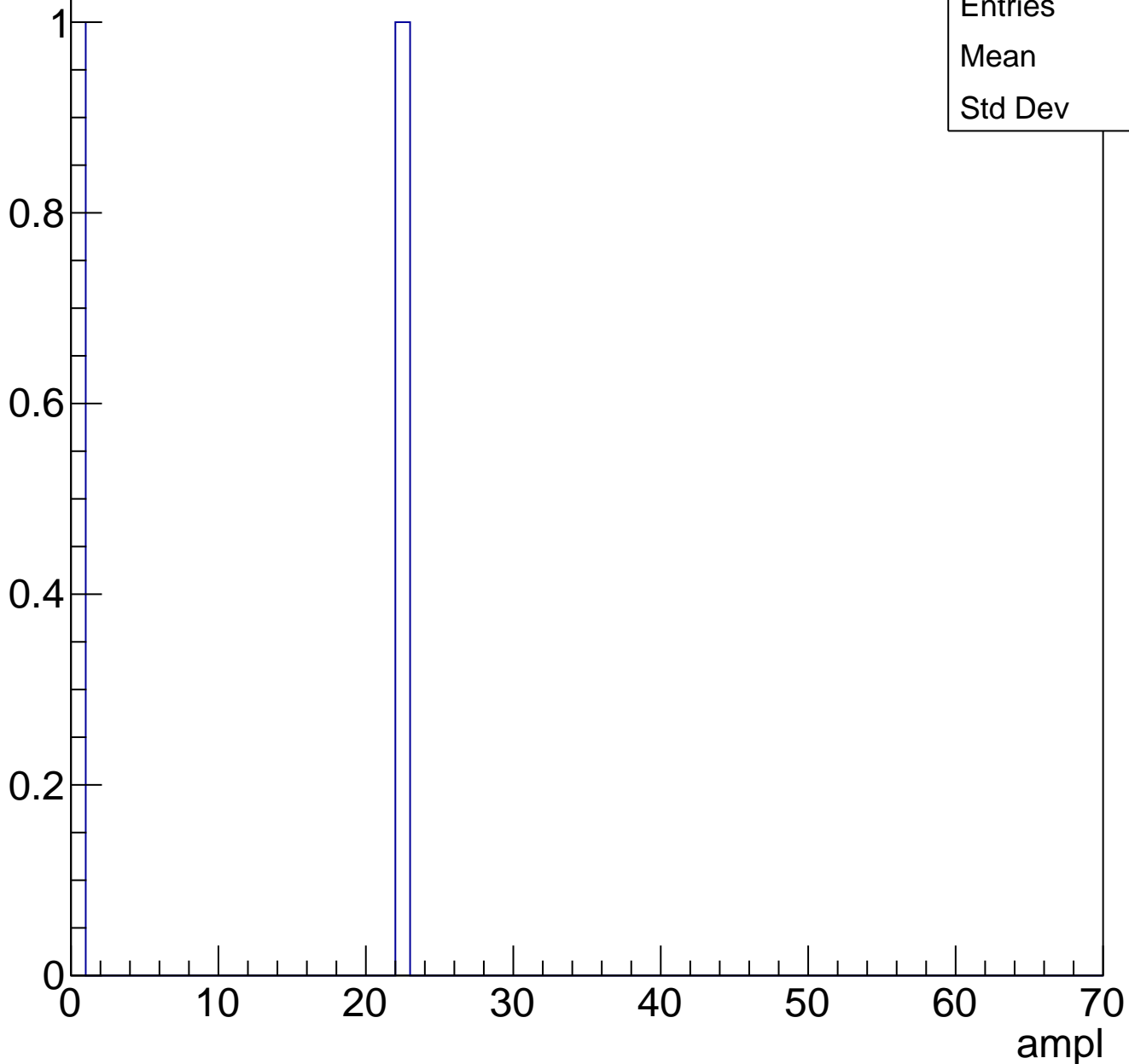
Entries	4
Mean	62
Std Dev	0.7071



# B0L001S, U17-ch73, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	11
Std Dev	11

# B0L001S, U17-ch74, adc0

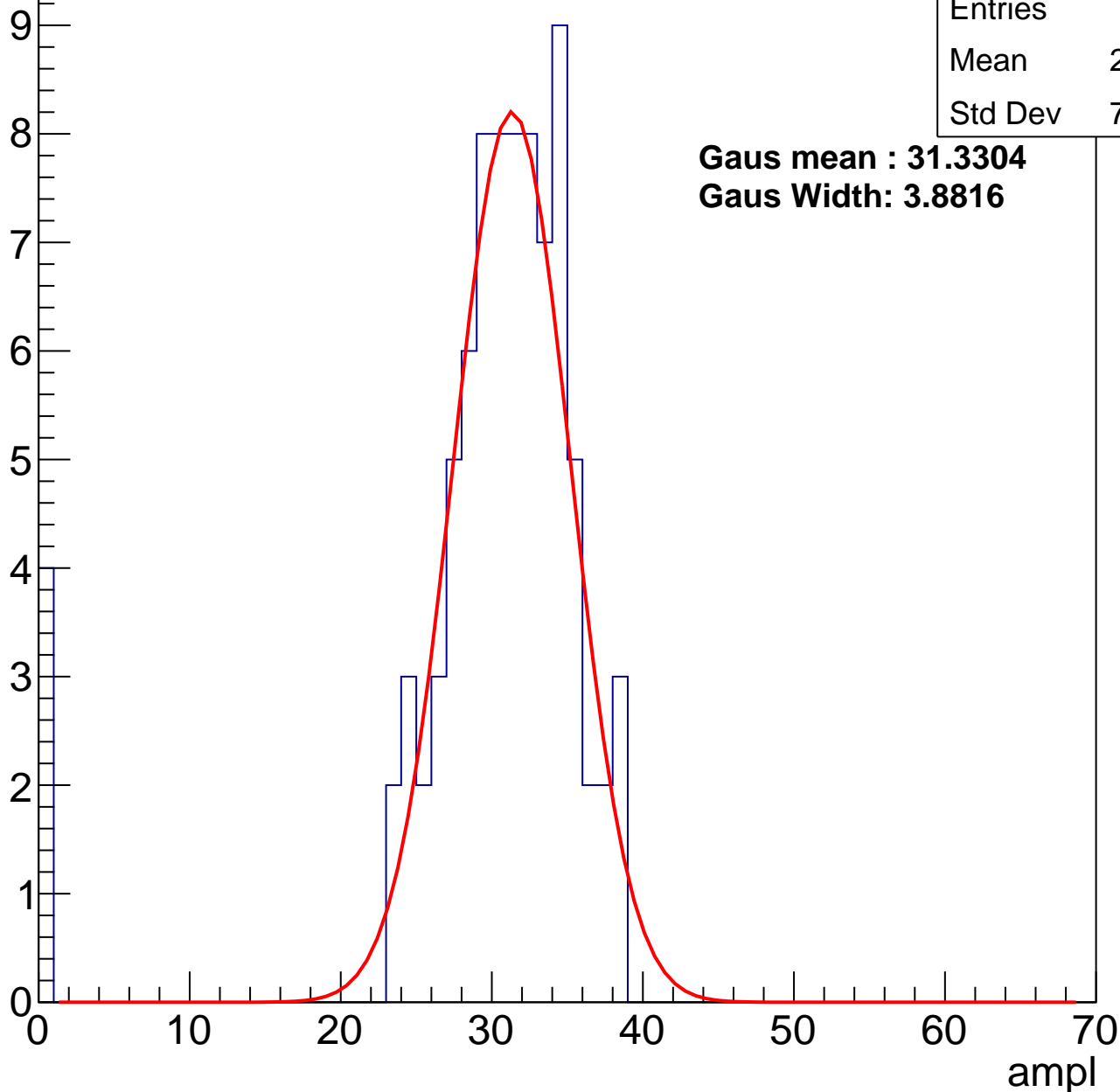
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	85
Mean	29.38
Std Dev	7.422

**Gaus mean : 31.3304**

**Gaus Width: 3.8816**



# B0L001S, U17-ch74, adc1

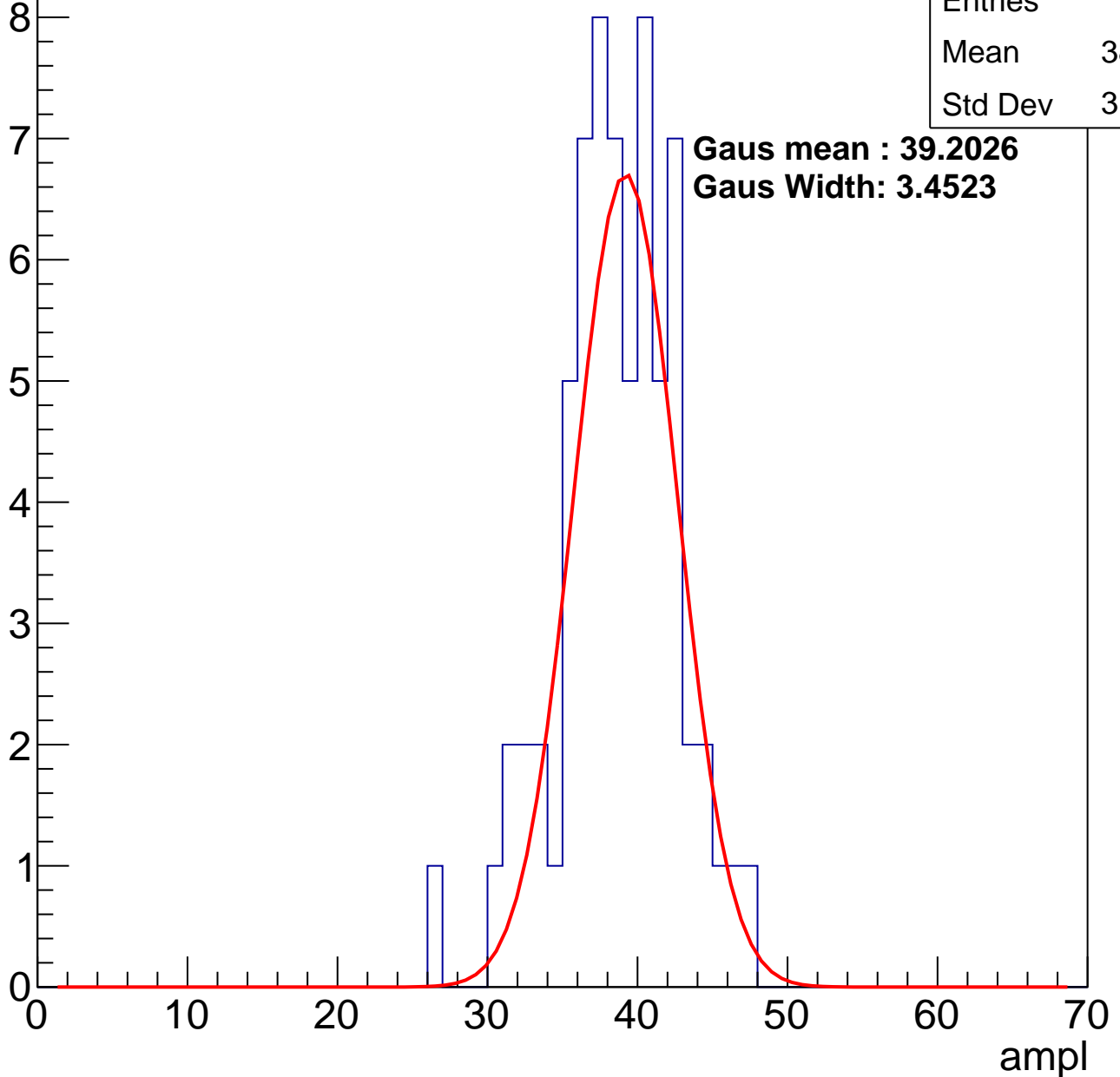
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	38.19
Std Dev	3.897

**Gaus mean : 39.2026**

**Gaus Width: 3.4523**



# B0L001S, U17-ch74, adc2

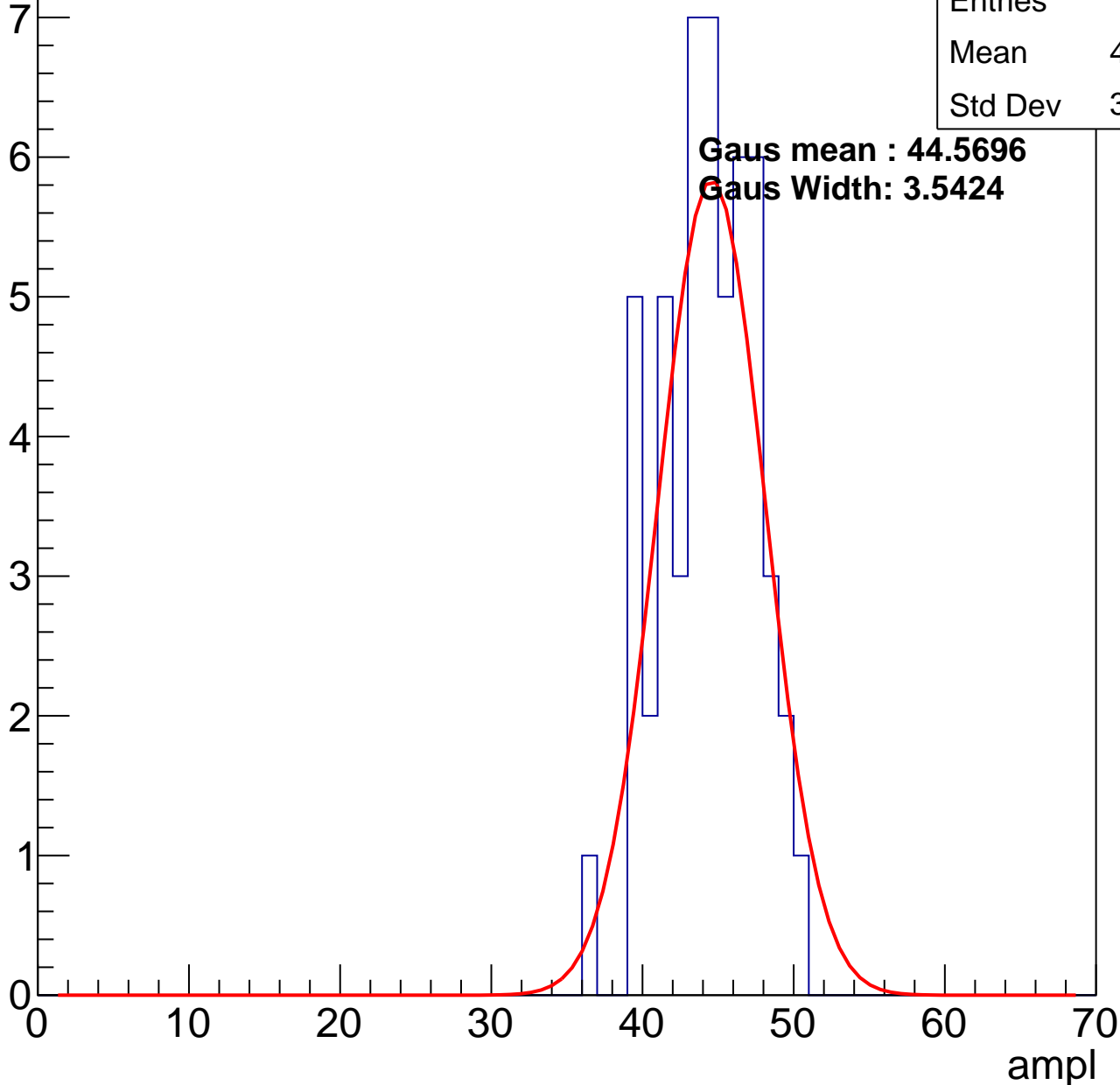
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	43.89
Std Dev	3.076

Gaus mean : 44.5696

Gaus Width: 3.5424

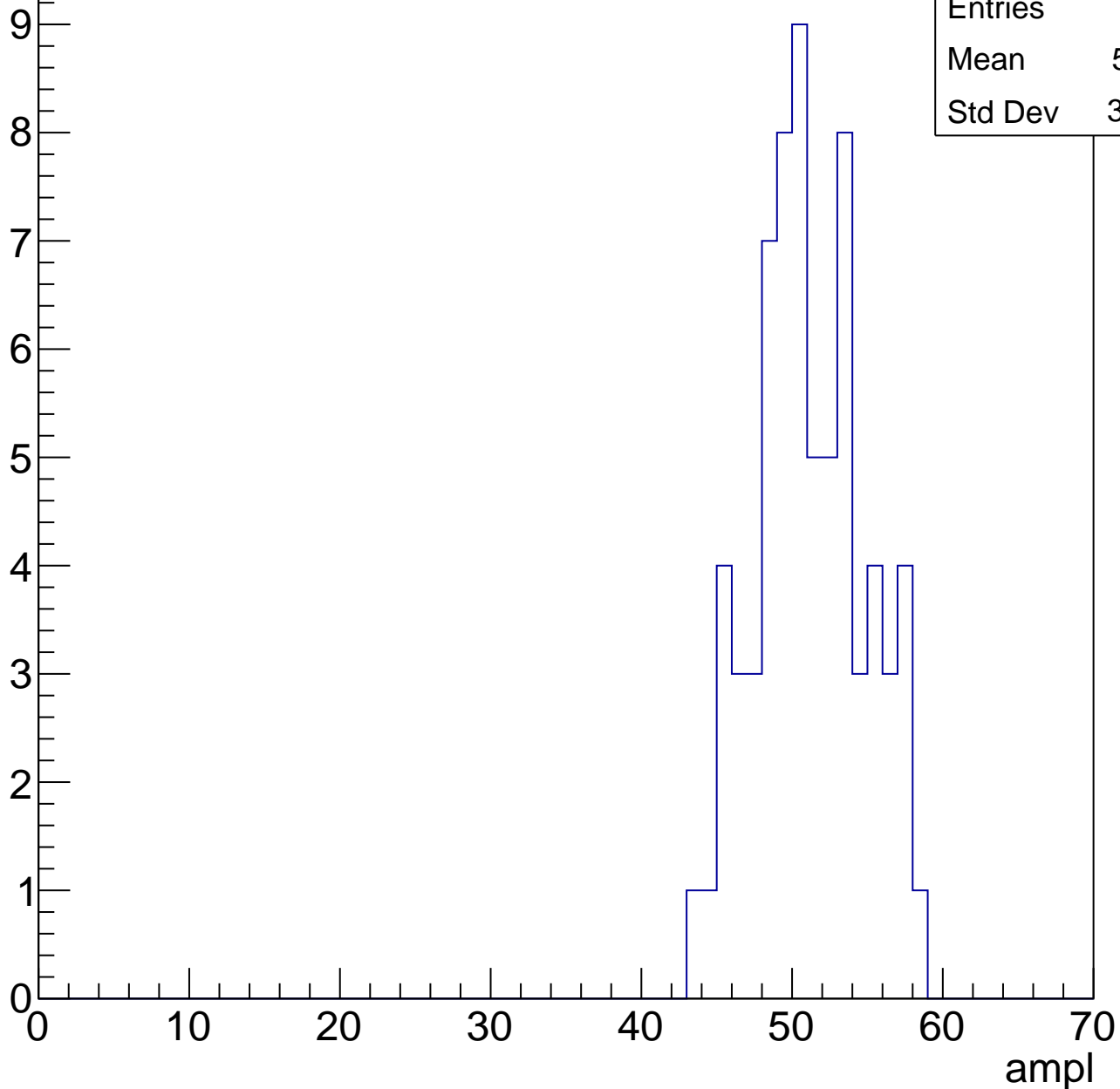


# B0L001S, U17-ch74, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	50.71
Std Dev	3.559

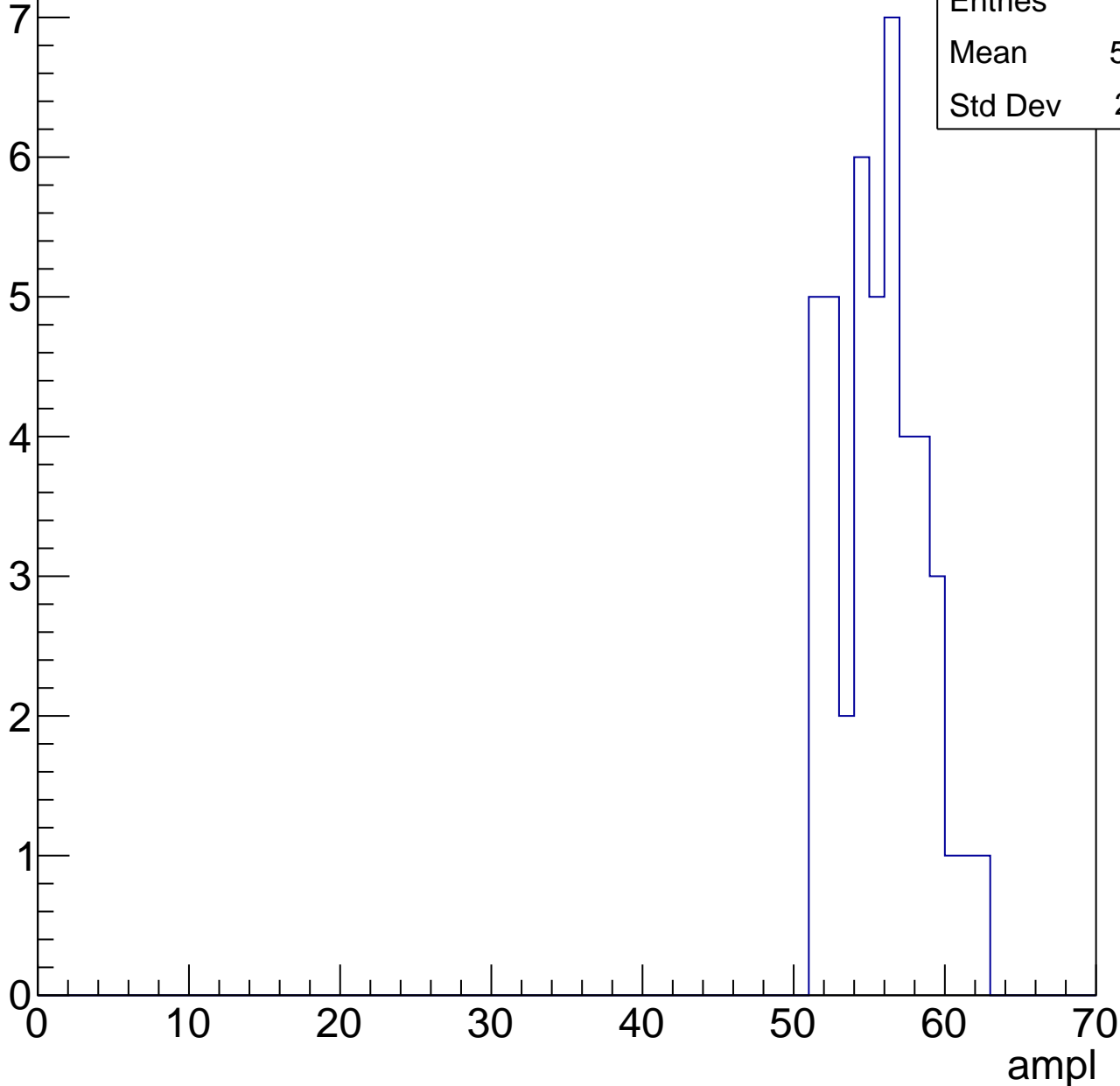


# B0L001S, U17-ch74, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	44
Mean	55.27
Std Dev	2.831

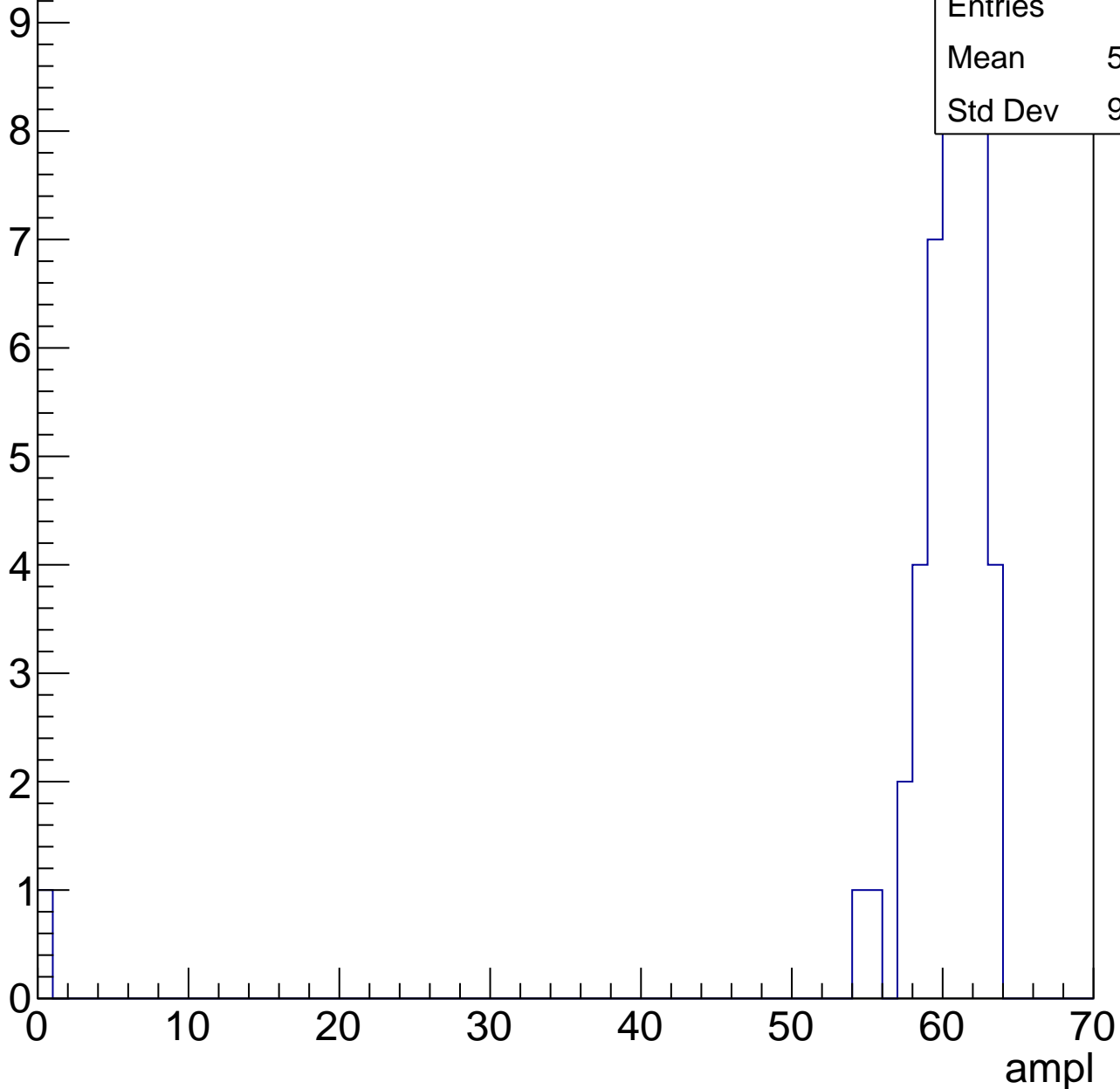


# B0L001S, U17-ch74, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	45
Mean	58.78
Std Dev	9.082

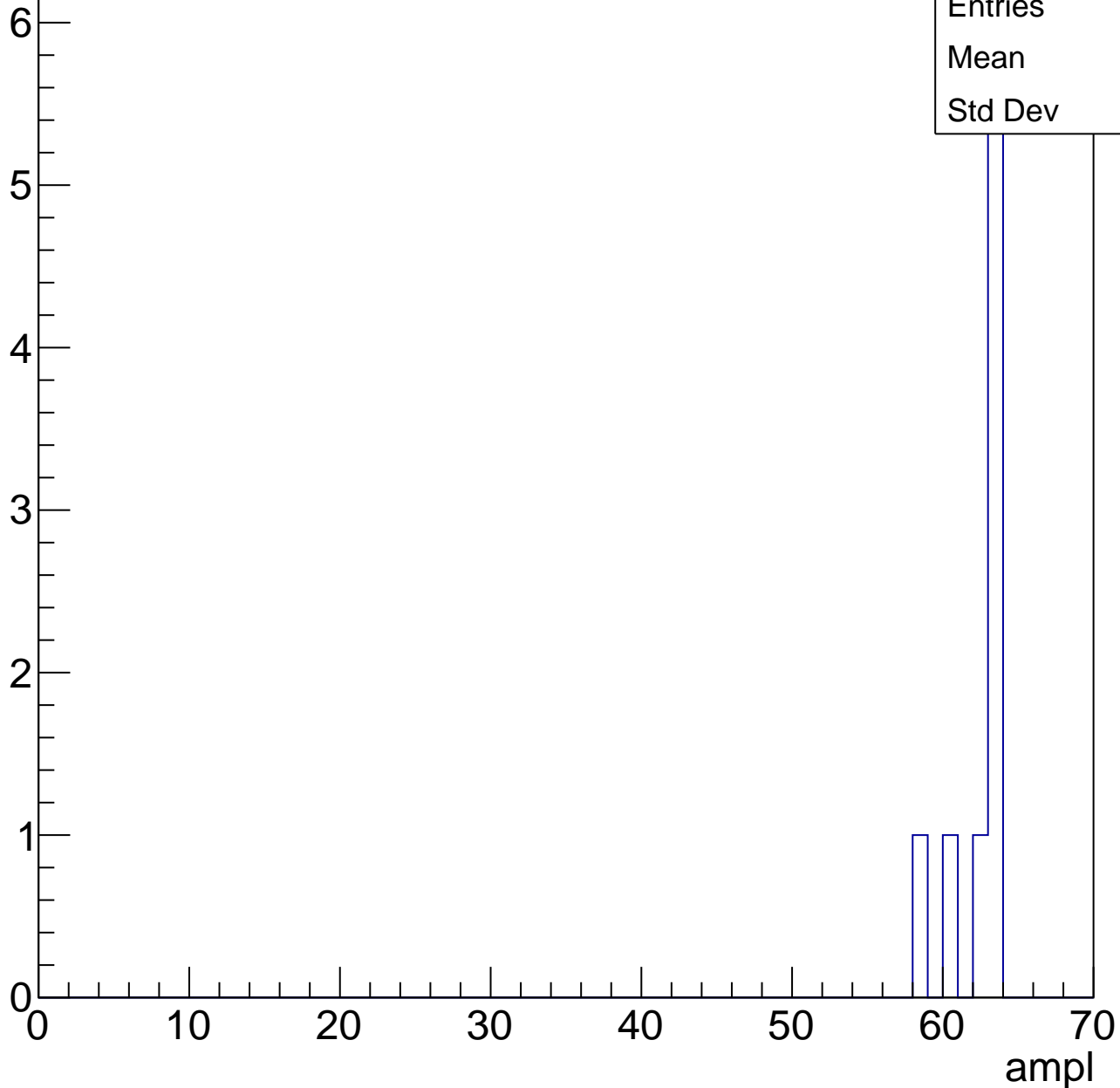


# B0L001S, U17-ch74, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	9
Mean	62
Std Dev	1.7





# B0L001S, U17-ch74, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U17-ch75, adc0

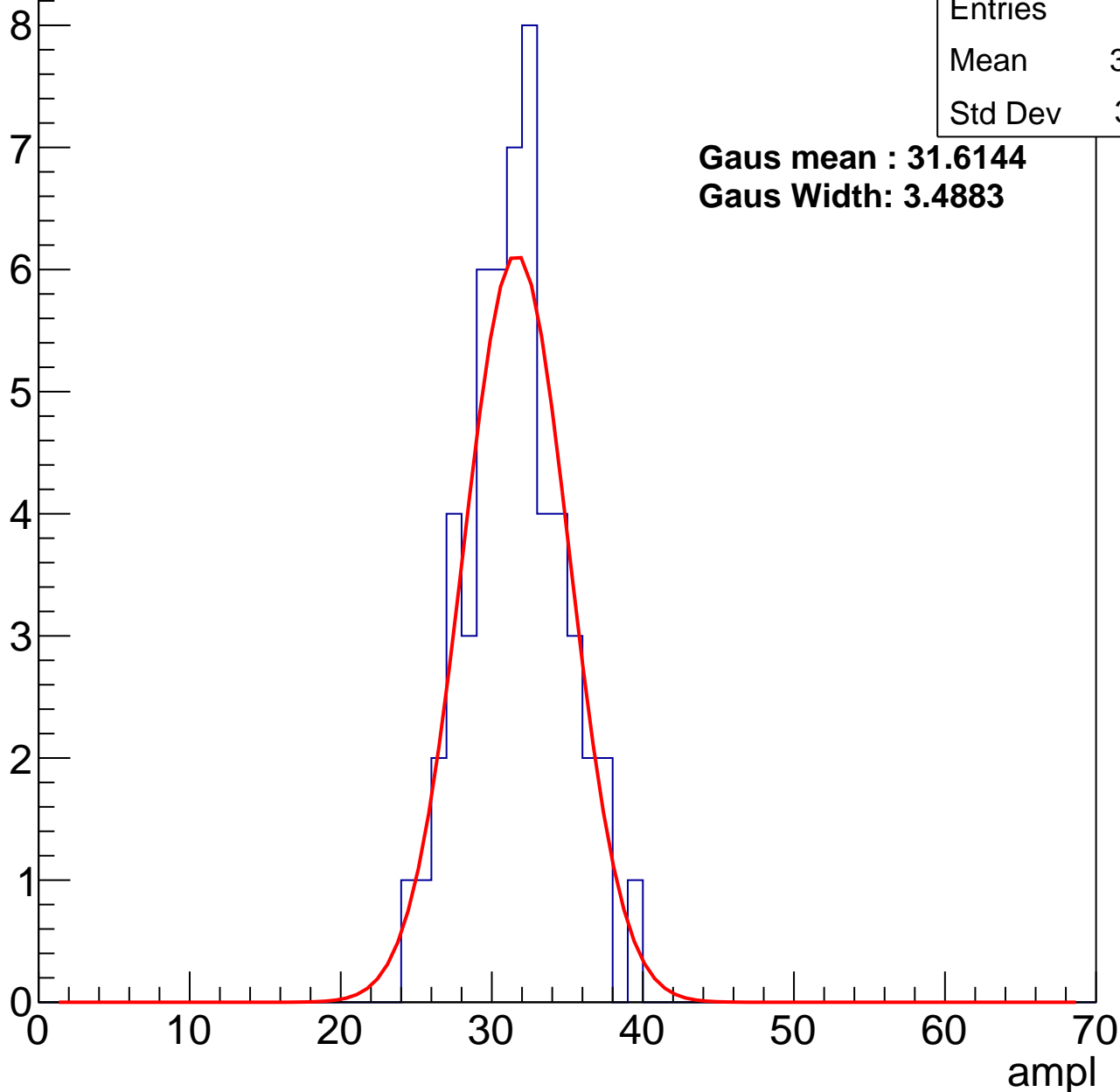
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	31.07
Std Dev	3.191

**Gaus mean : 31.6144**

**Gaus Width: 3.4883**



# B0L001S, U17-ch75, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	83
Mean	37.54
Std Dev	4.075

**Gaus mean : 38.4787**

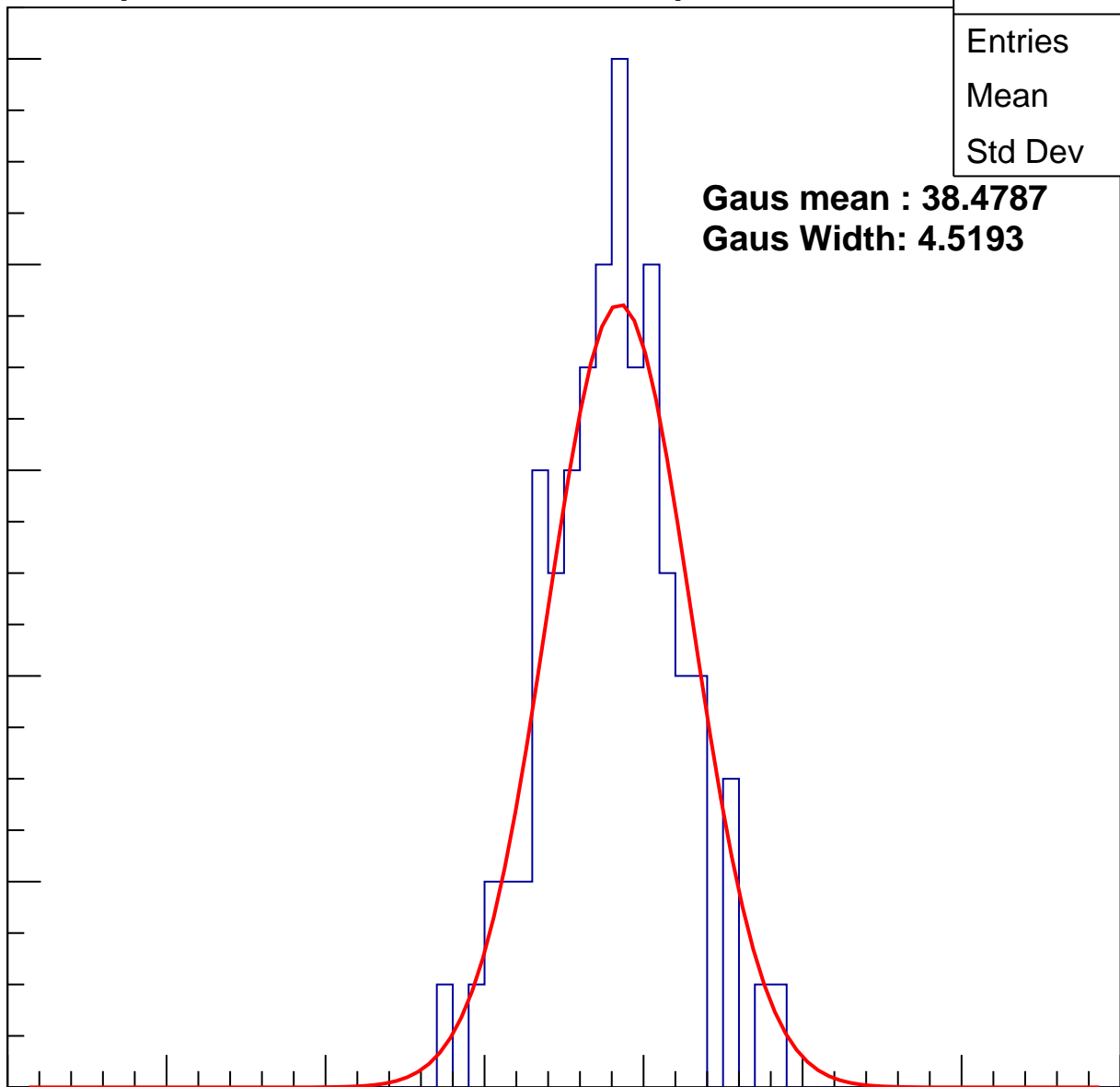
**Gaus Width: 4.5193**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U17-ch75, adc2

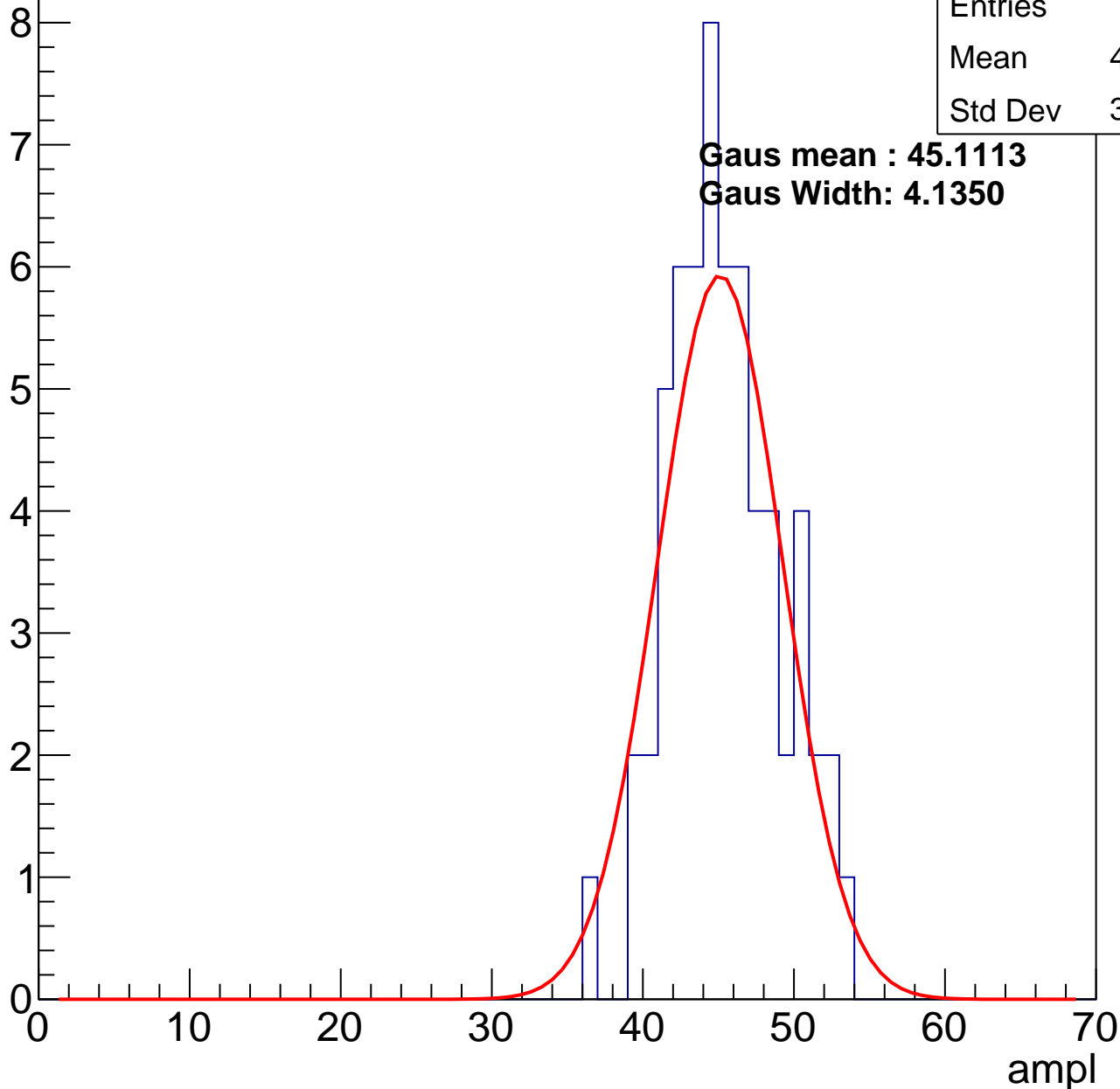
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	44.98
Std Dev	3.606

**Gaus mean : 45.1113**

**Gaus Width: 4.1350**

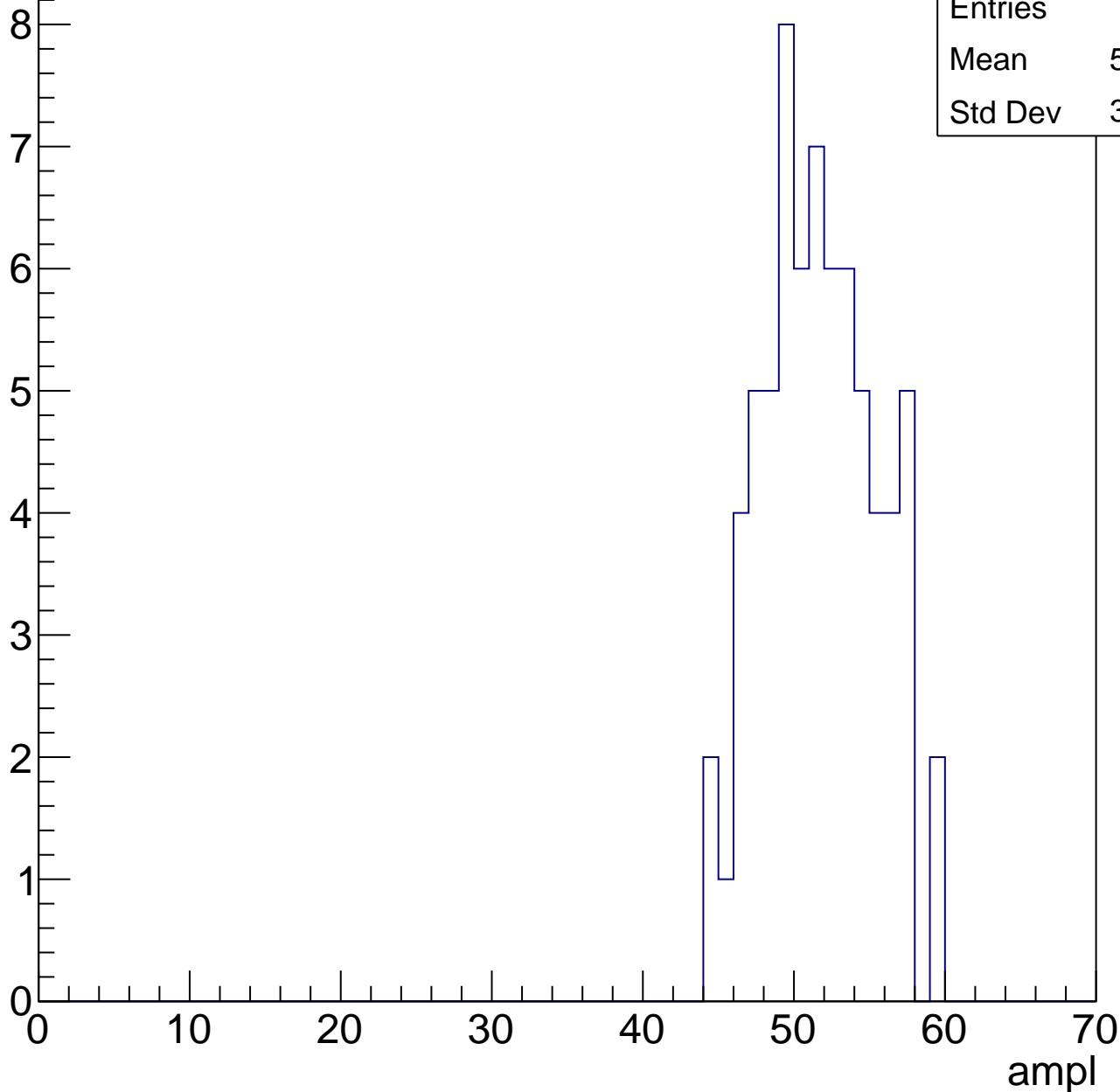


# B0L001S, U17-ch75, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	51.26
Std Dev	3.663

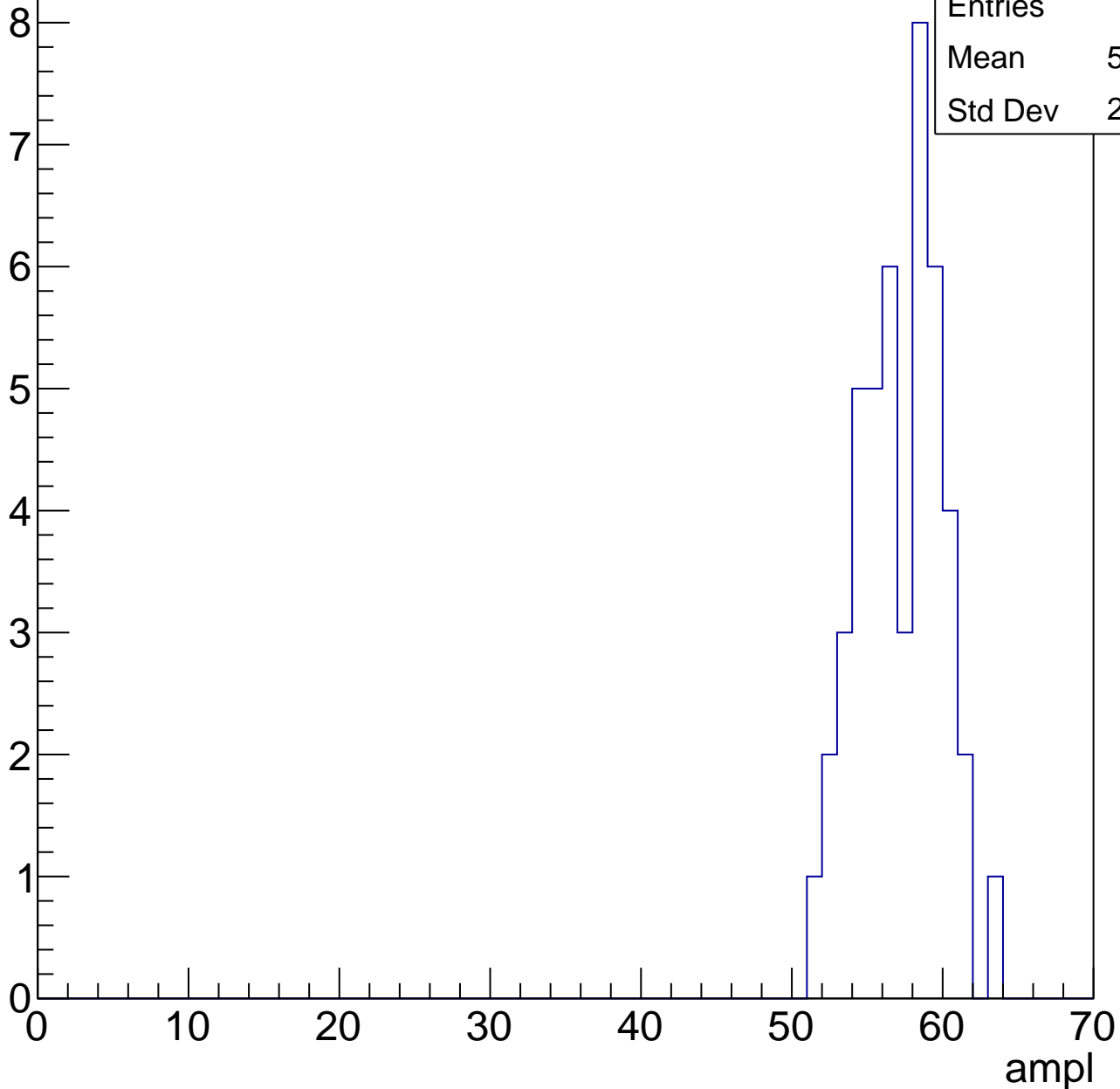


# B0L001S, U17-ch75, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	46
Mean	56.72
Std Dev	2.708



# B0L001S, U17-ch75, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	40
Mean	59.38
Std Dev	9.692

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

ampl

0

2

4

6

8

10

# B0L001S, U17-ch75, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch75, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U17-ch76, adc0

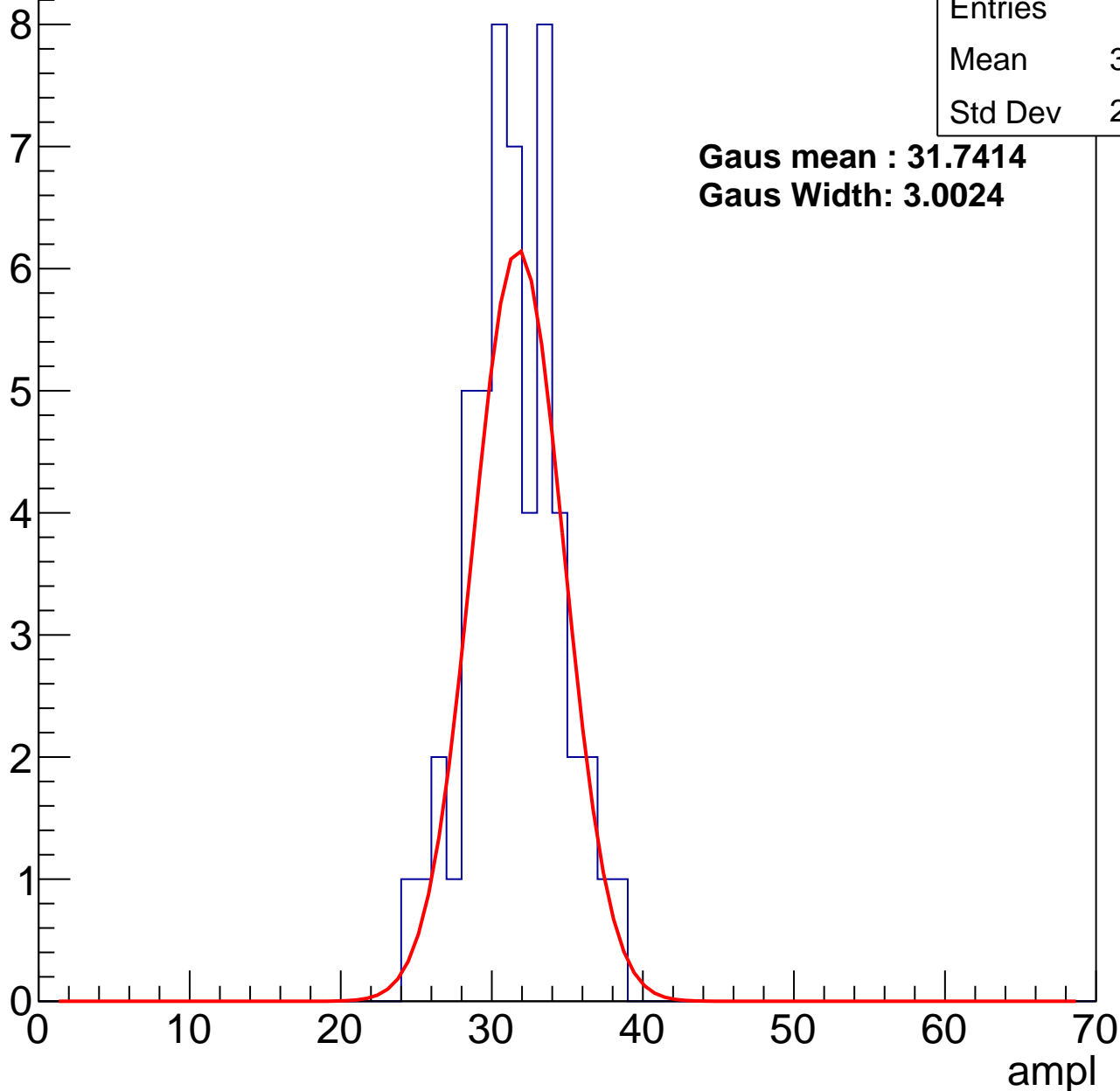
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	31.06
Std Dev	2.983

**Gaus mean : 31.7414**

**Gaus Width: 3.0024**



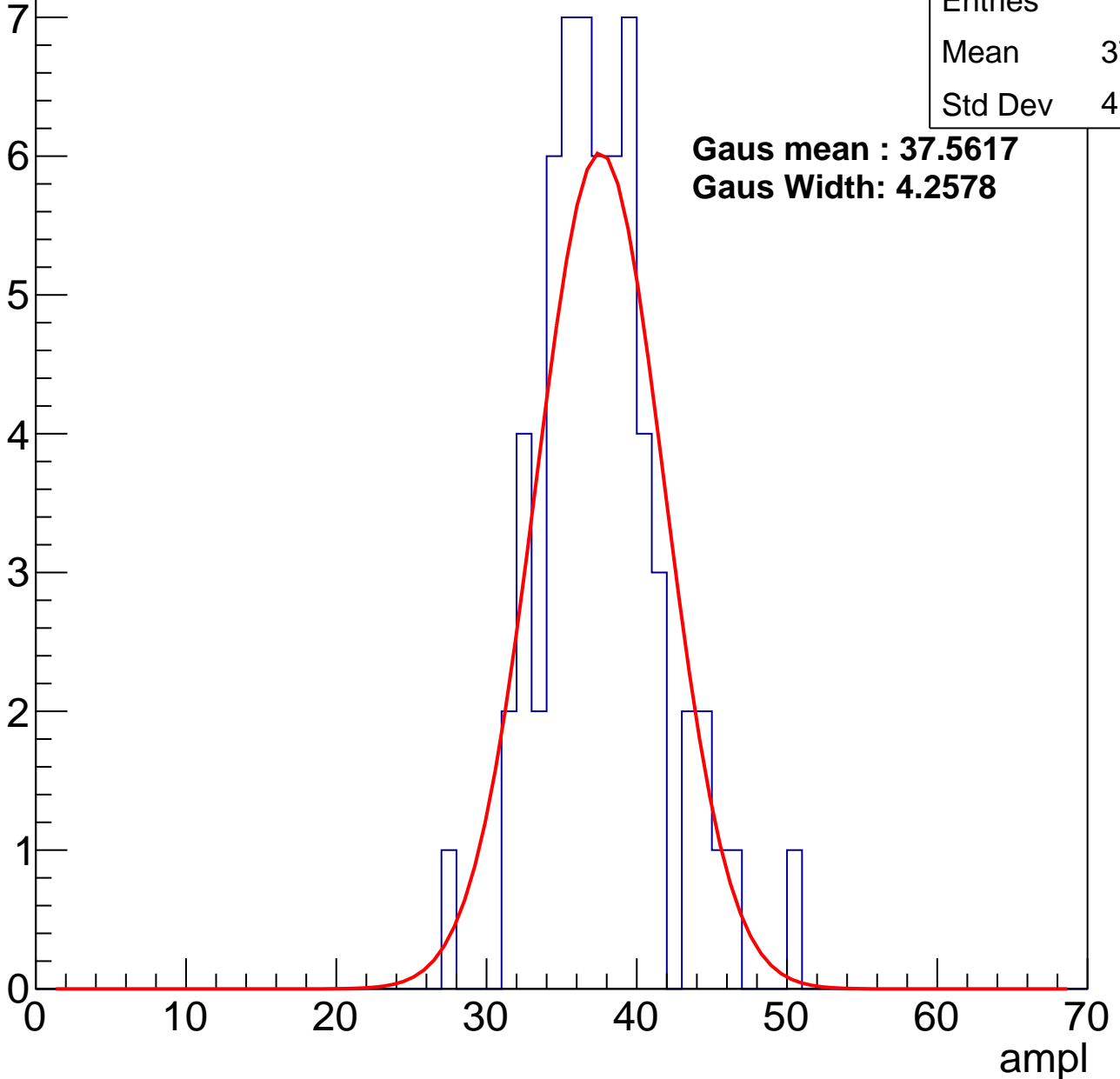
# B0L001S, U17-ch76, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	37.18
Std Dev	4.002

**Gaus mean : 37.5617**  
**Gaus Width: 4.2578**



# B0L001S, U17-ch76, adc2

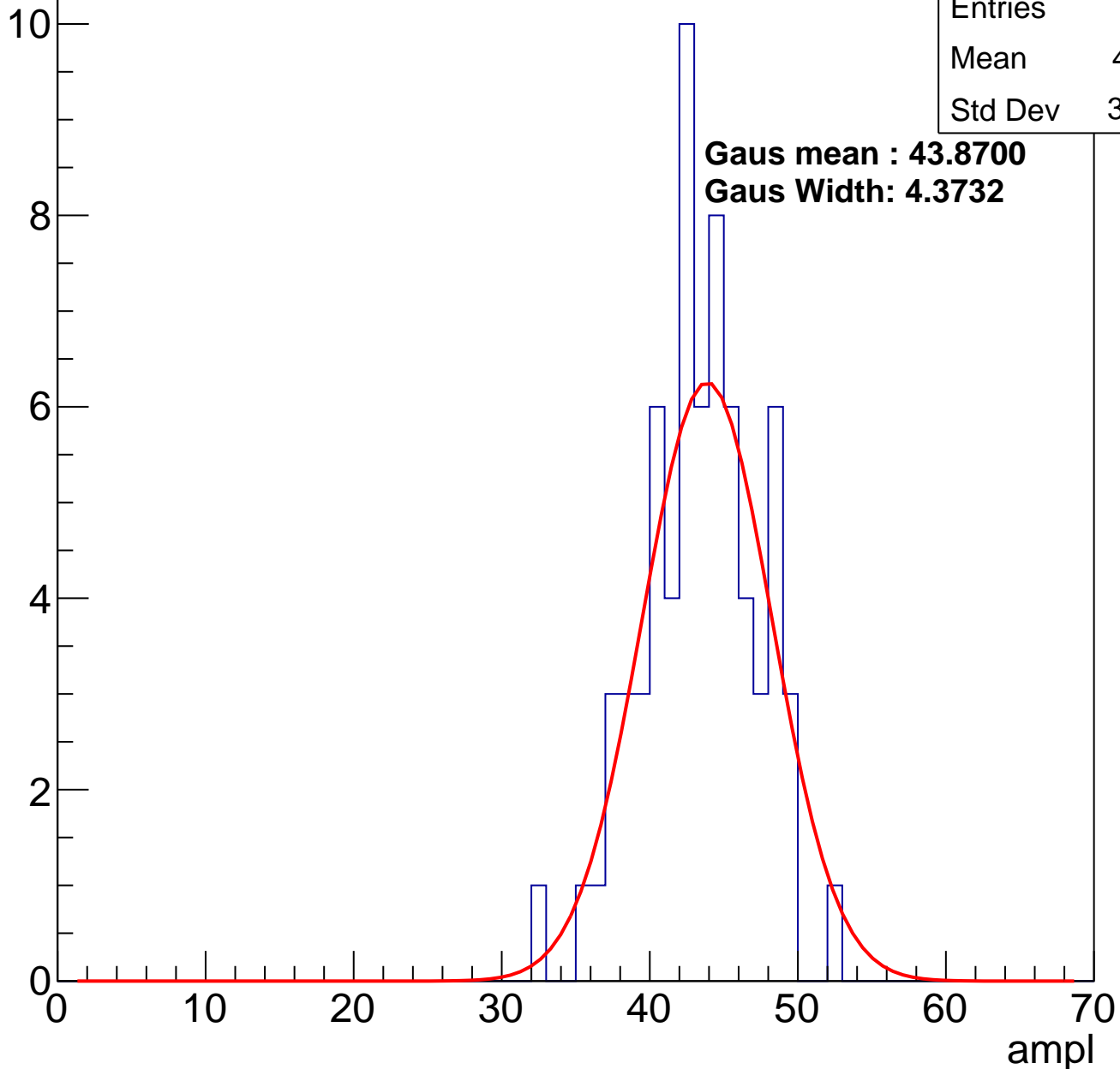
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	69
Mean	42.91
Std Dev	3.806

**Gaus mean : 43.8700**

**Gaus Width: 4.3732**

Entry

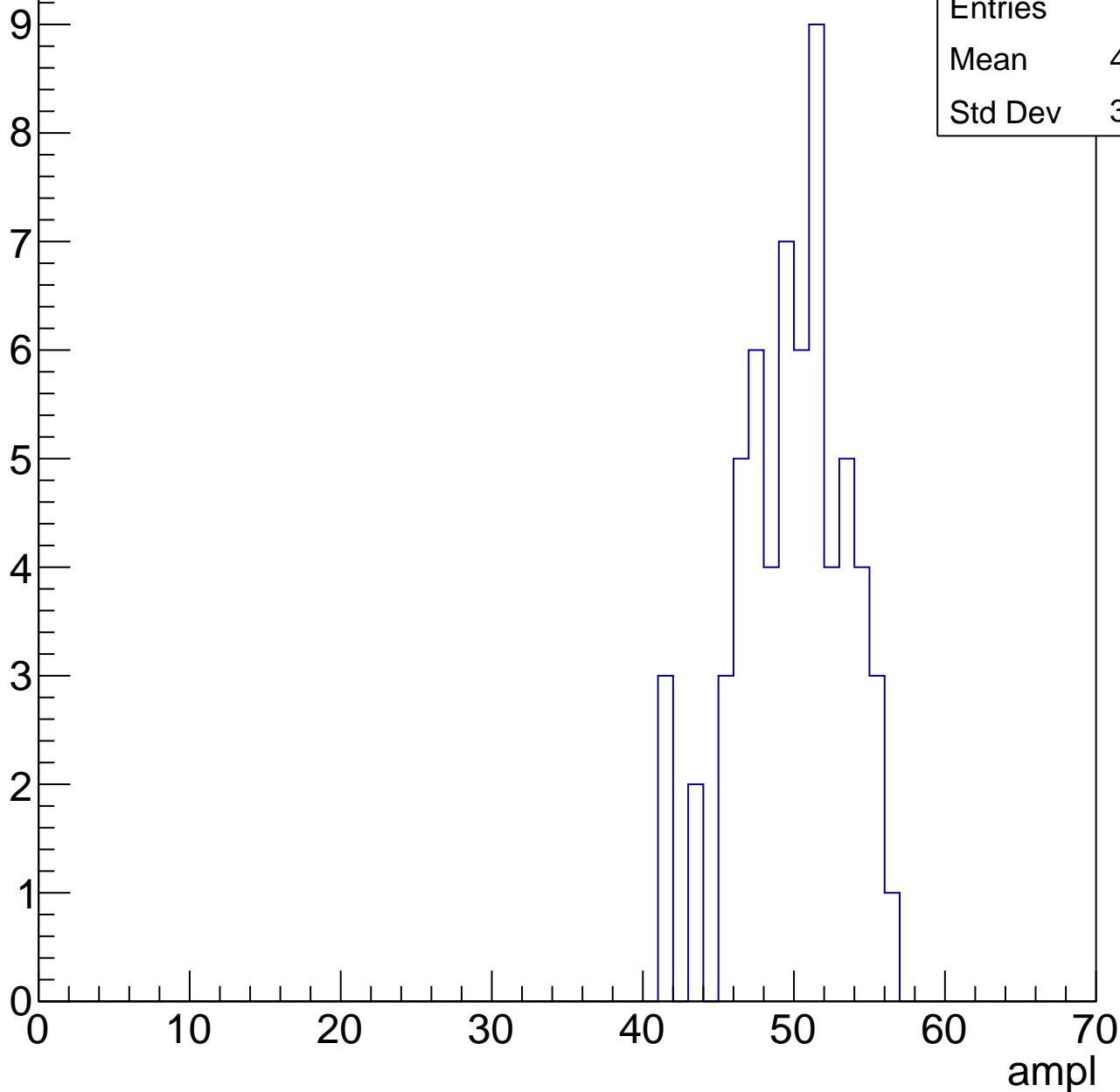


# B0L001S, U17-ch76, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	49.35
Std Dev	3.575

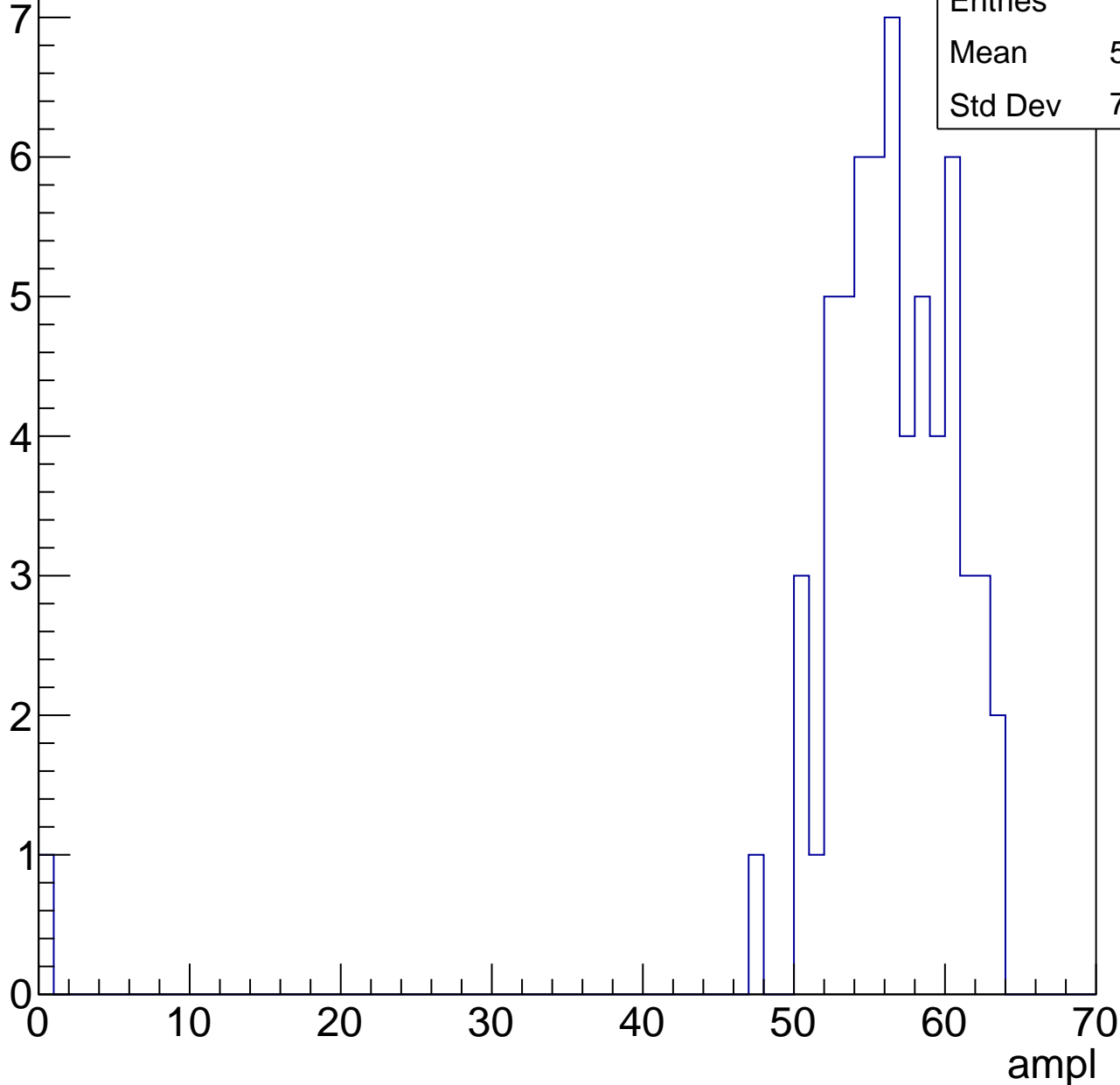


# B0L001S, U17-ch76, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	55.29
Std Dev	7.942

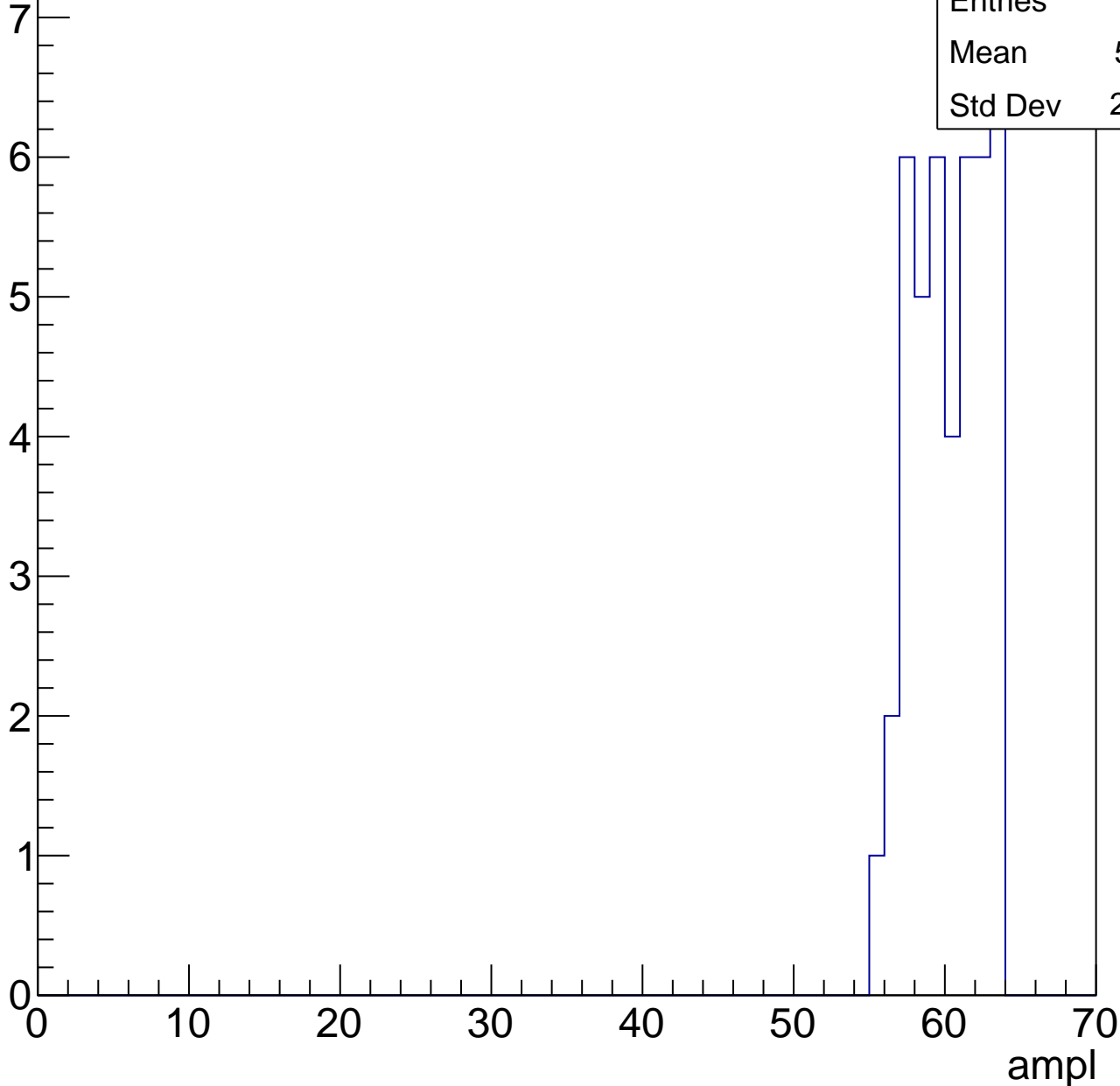


# B0L001S, U17-ch76, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	43
Mean	59.81
Std Dev	2.305



# B0L001S, U17-ch76, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch76, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U17-ch77, adc0

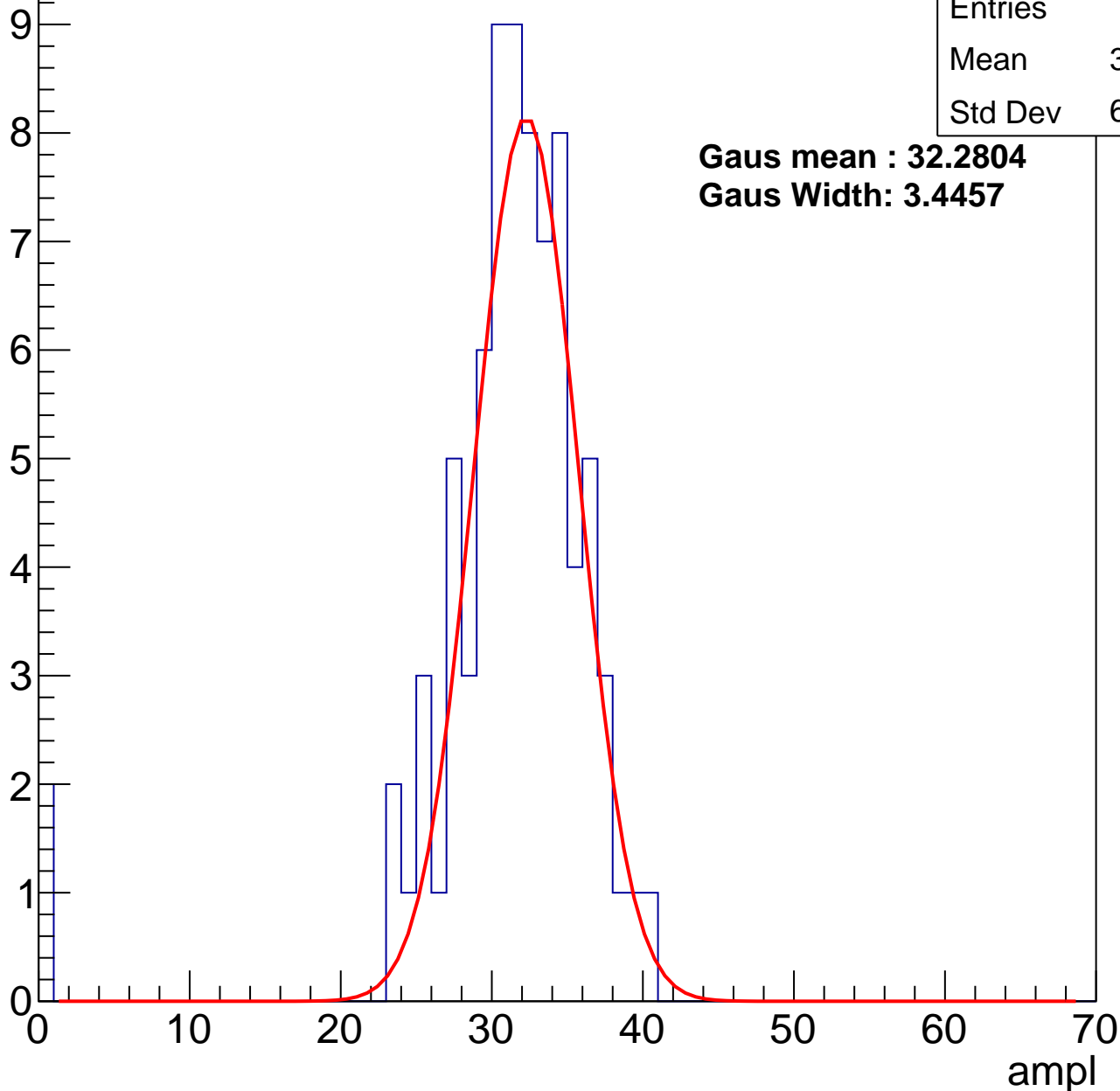
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	79
Mean	30.63
Std Dev	6.122

**Gaus mean : 32.2804**

**Gaus Width: 3.4457**



# B0L001S, U17-ch77, adc1

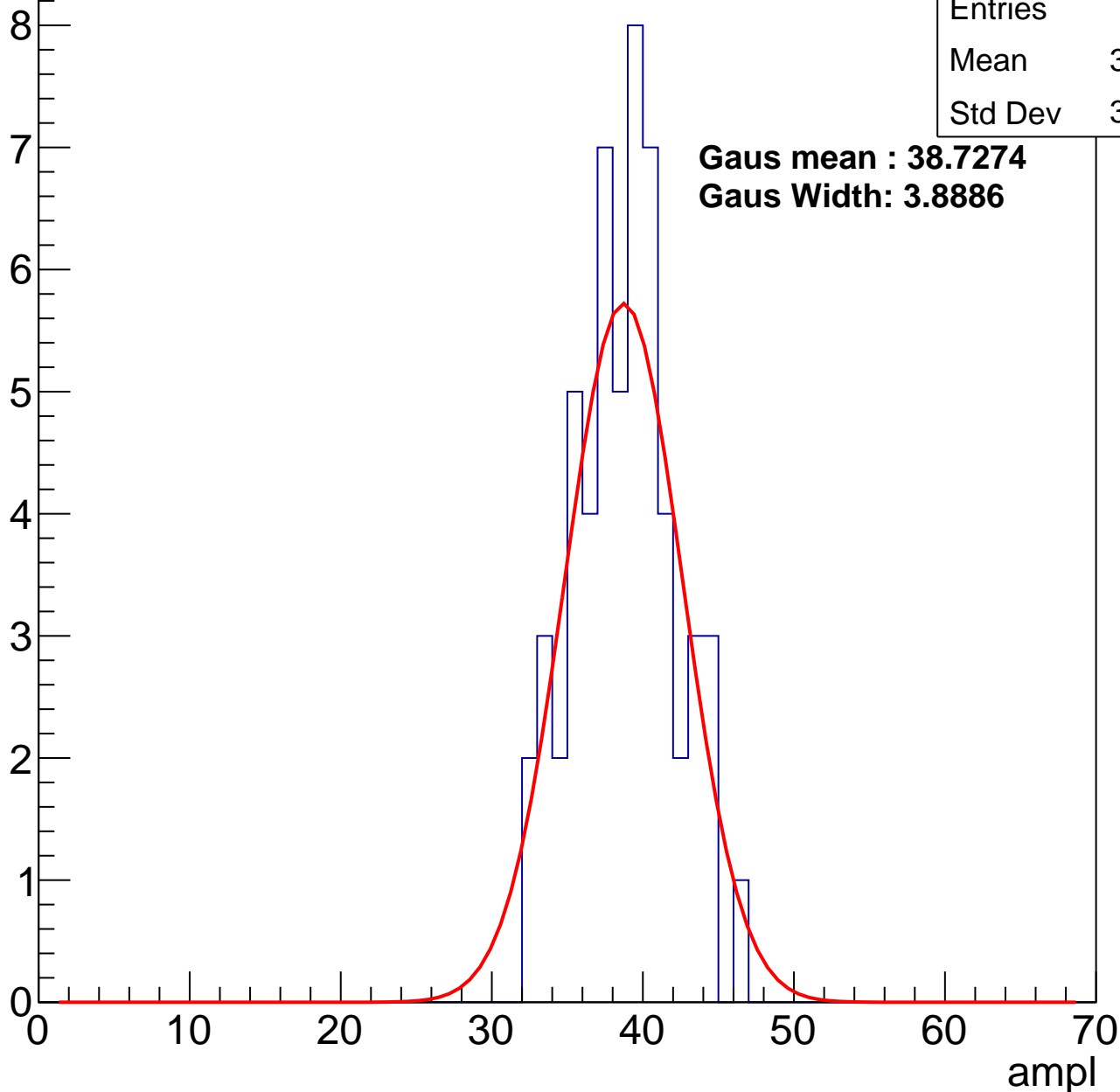
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	38.32
Std Dev	3.252

**Gaus mean : 38.7274**

**Gaus Width: 3.8886**



# B0L001S, U17-ch77, adc2

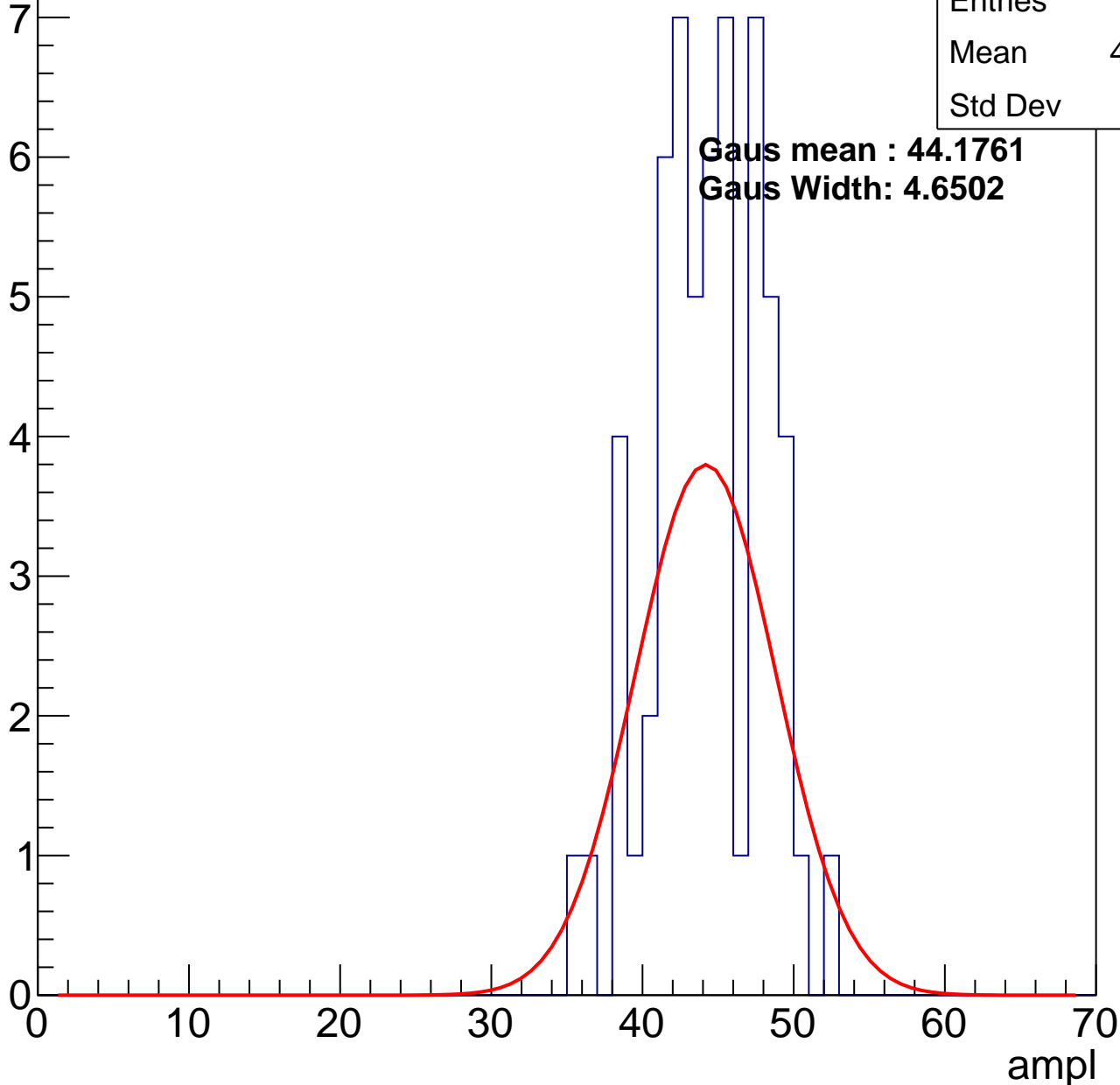
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	43.88
Std Dev	3.65

**Gaus mean : 44.1761**

**Gaus Width: 4.6502**

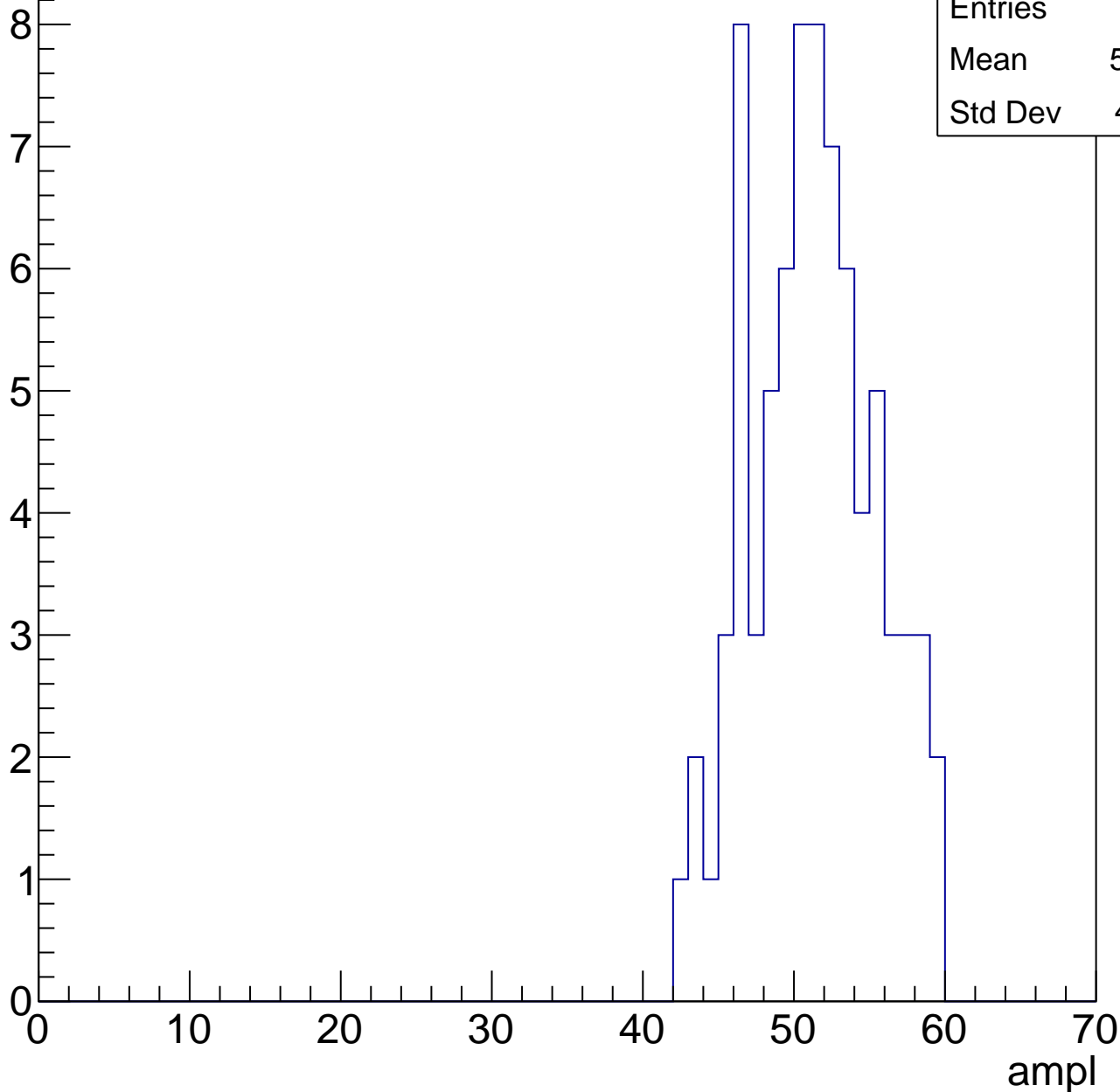


# B0L001S, U17-ch77, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

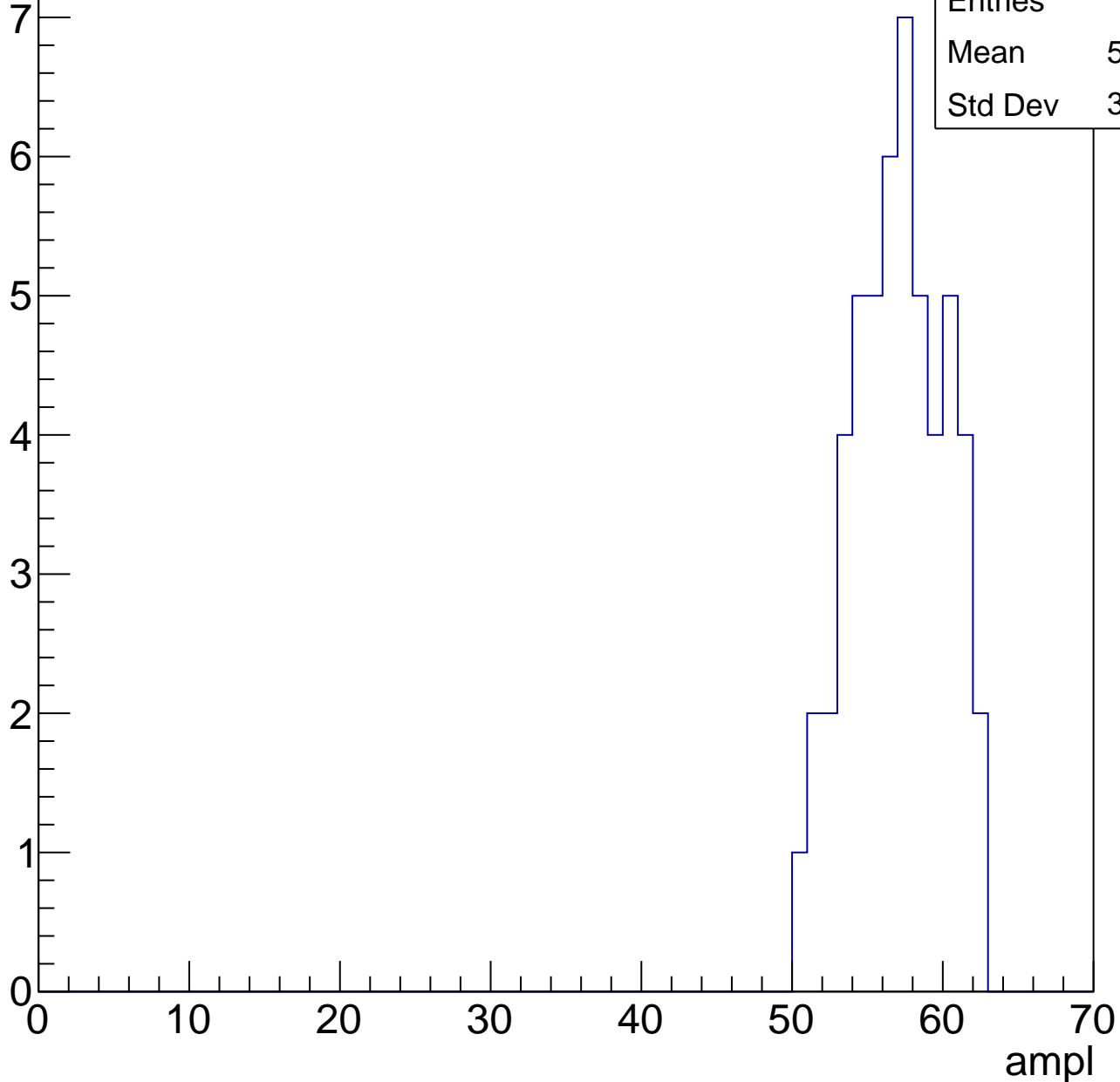
Entries	78
Mean	50.79
Std Dev	4.071



# B0L001S, U17-ch77, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



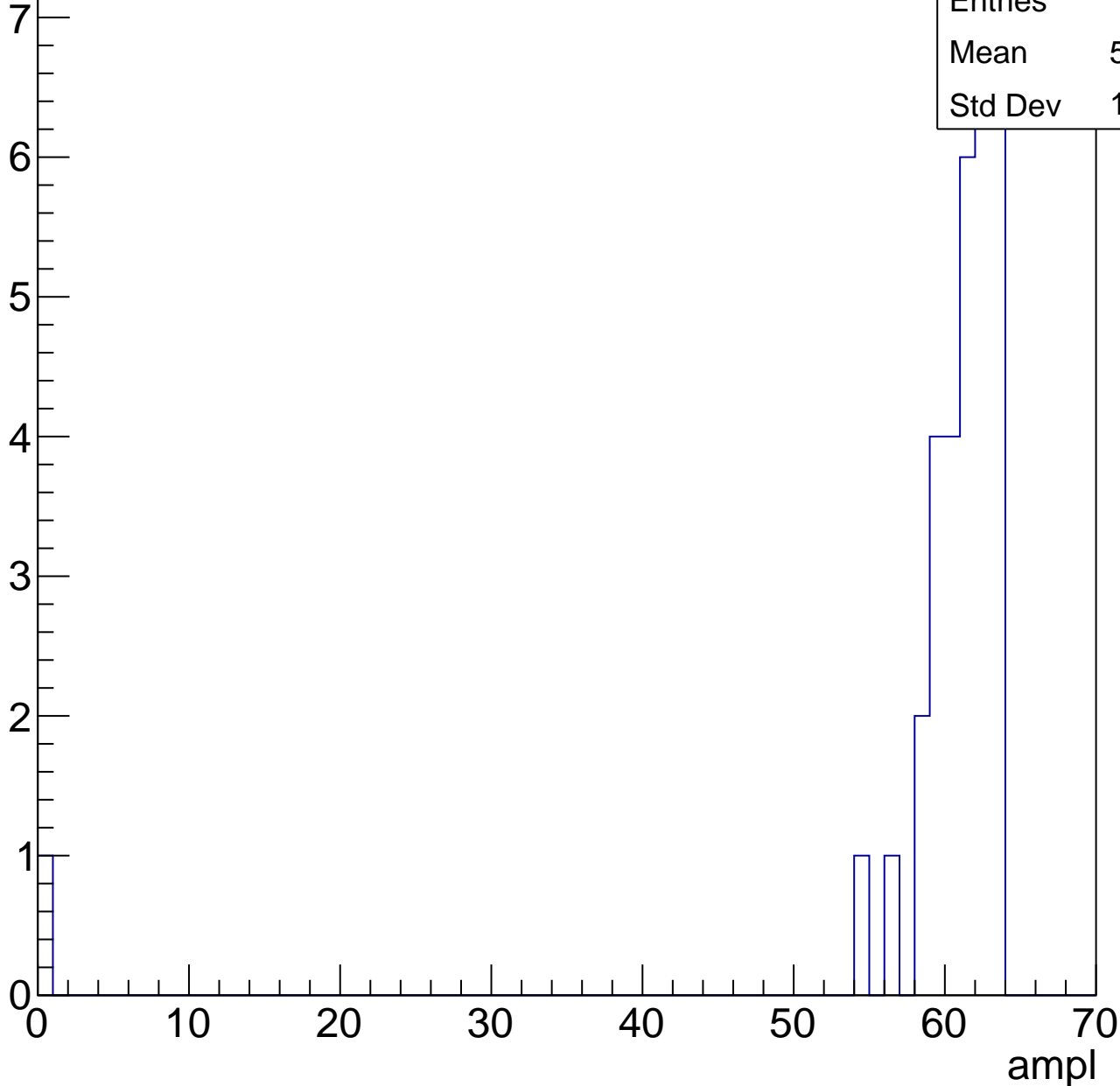
Entries	52
Mean	56.58
Std Dev	3.028

# B0L001S, U17-ch77, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

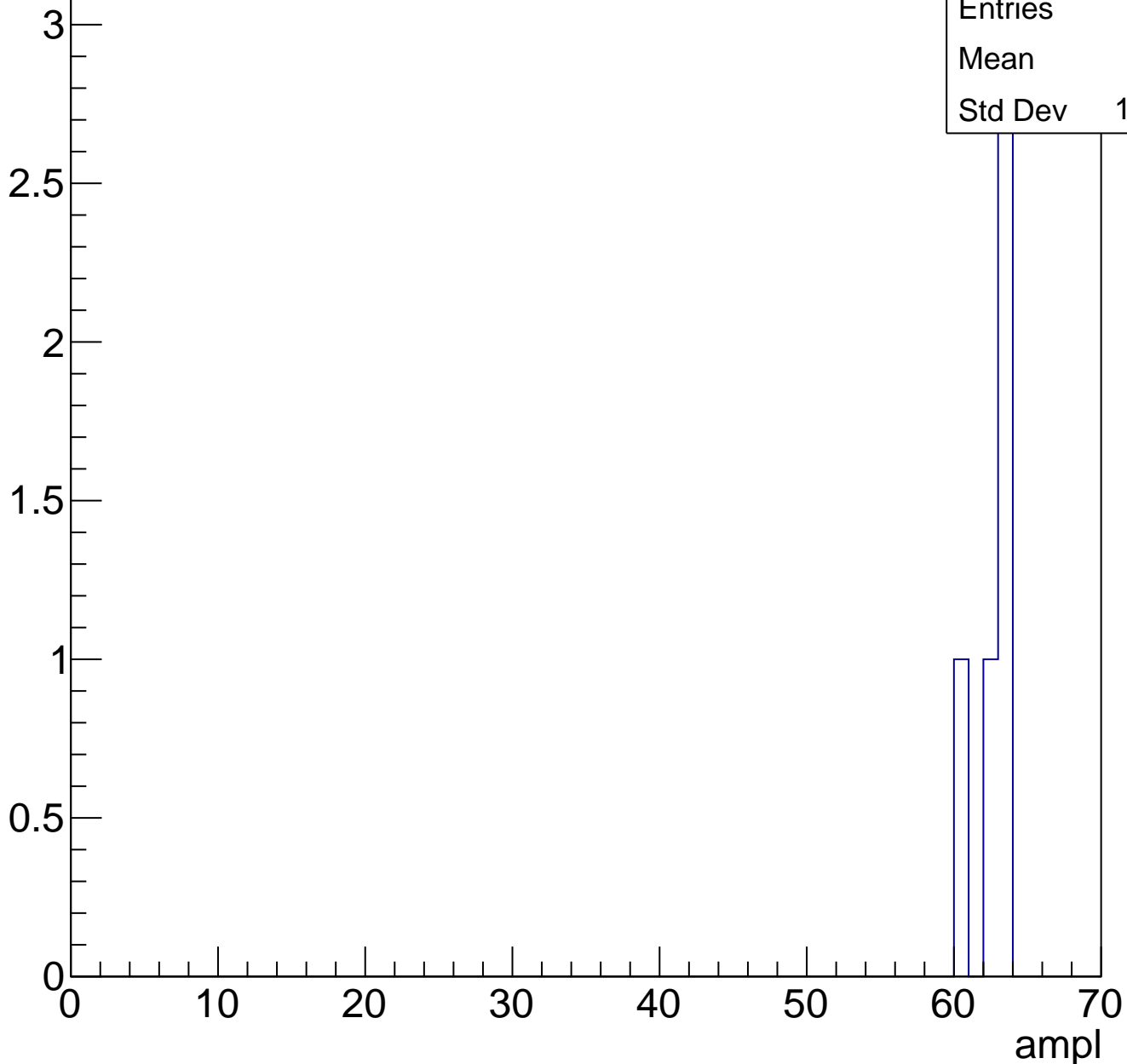
Entries	33
Mean	58.88
Std Dev	10.62



# B0L001S, U17-ch77, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch77, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U17-ch78, adc0

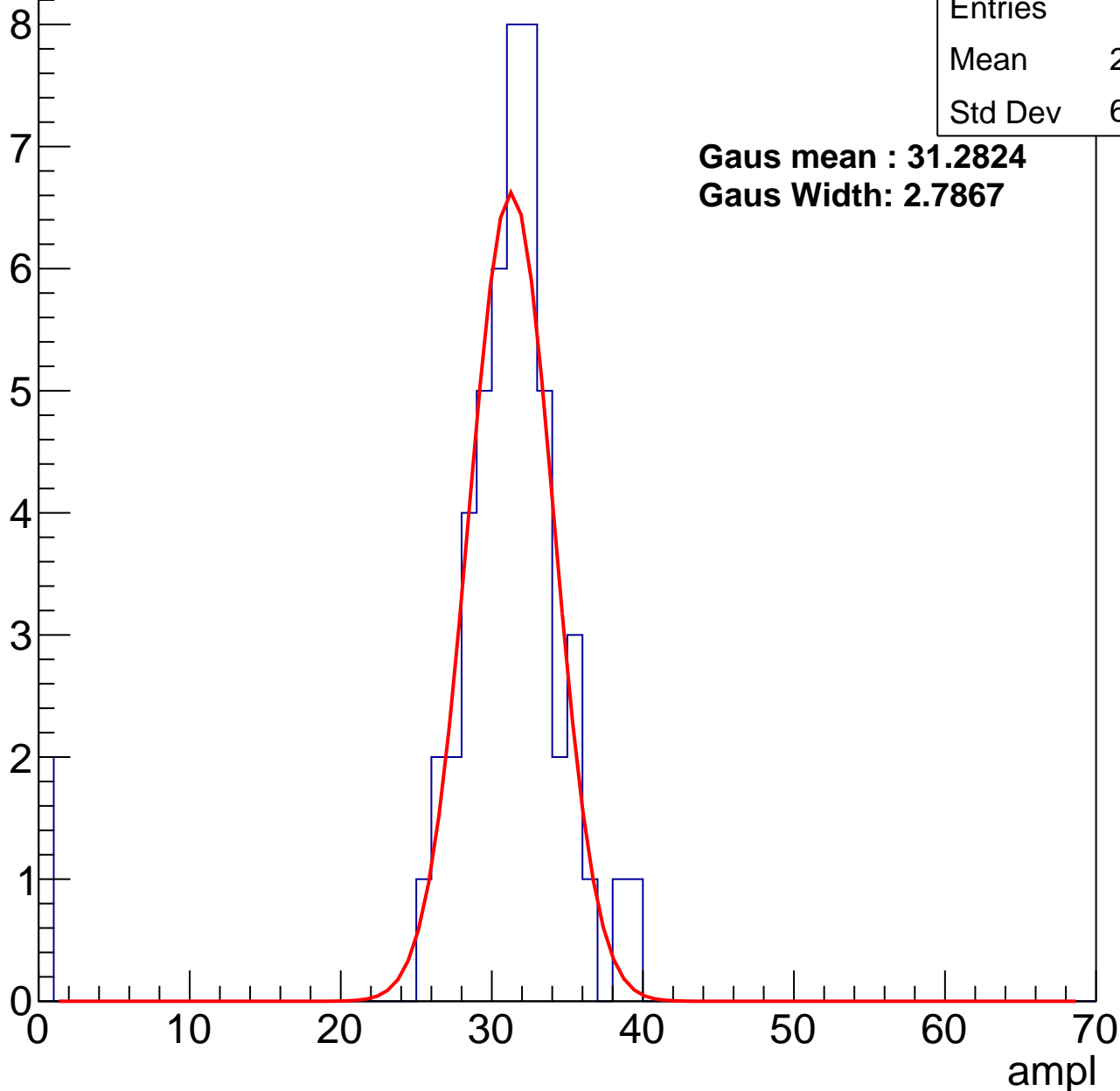
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	51
Mean	29.86
Std Dev	6.669

**Gaus mean : 31.2824**

**Gaus Width: 2.7867**



# B0L001S, U17-ch78, adc1

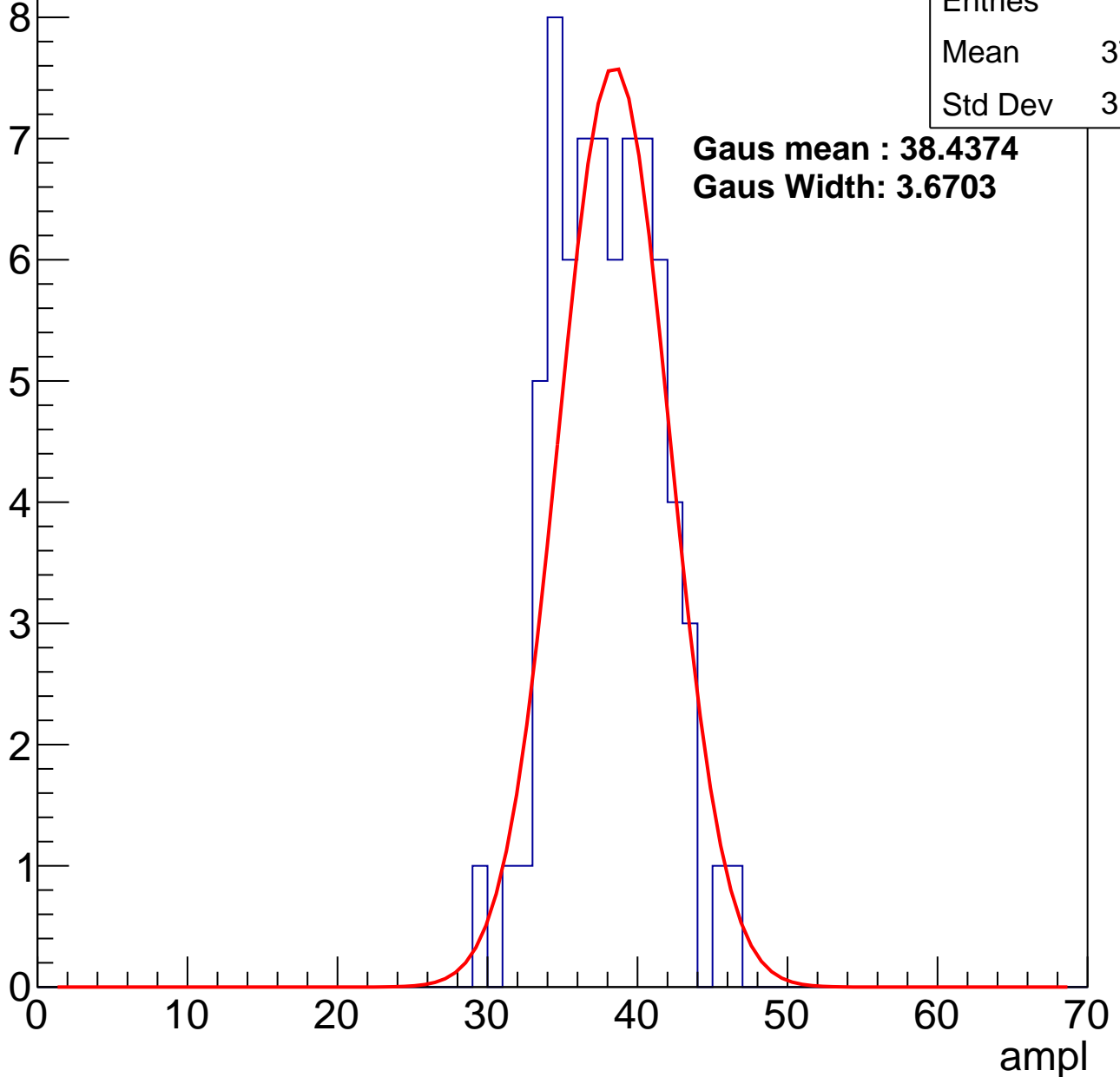
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	37.54
Std Dev	3.427

**Gaus mean : 38.4374**

**Gaus Width: 3.6703**



# B0L001S, U17-ch78, adc2

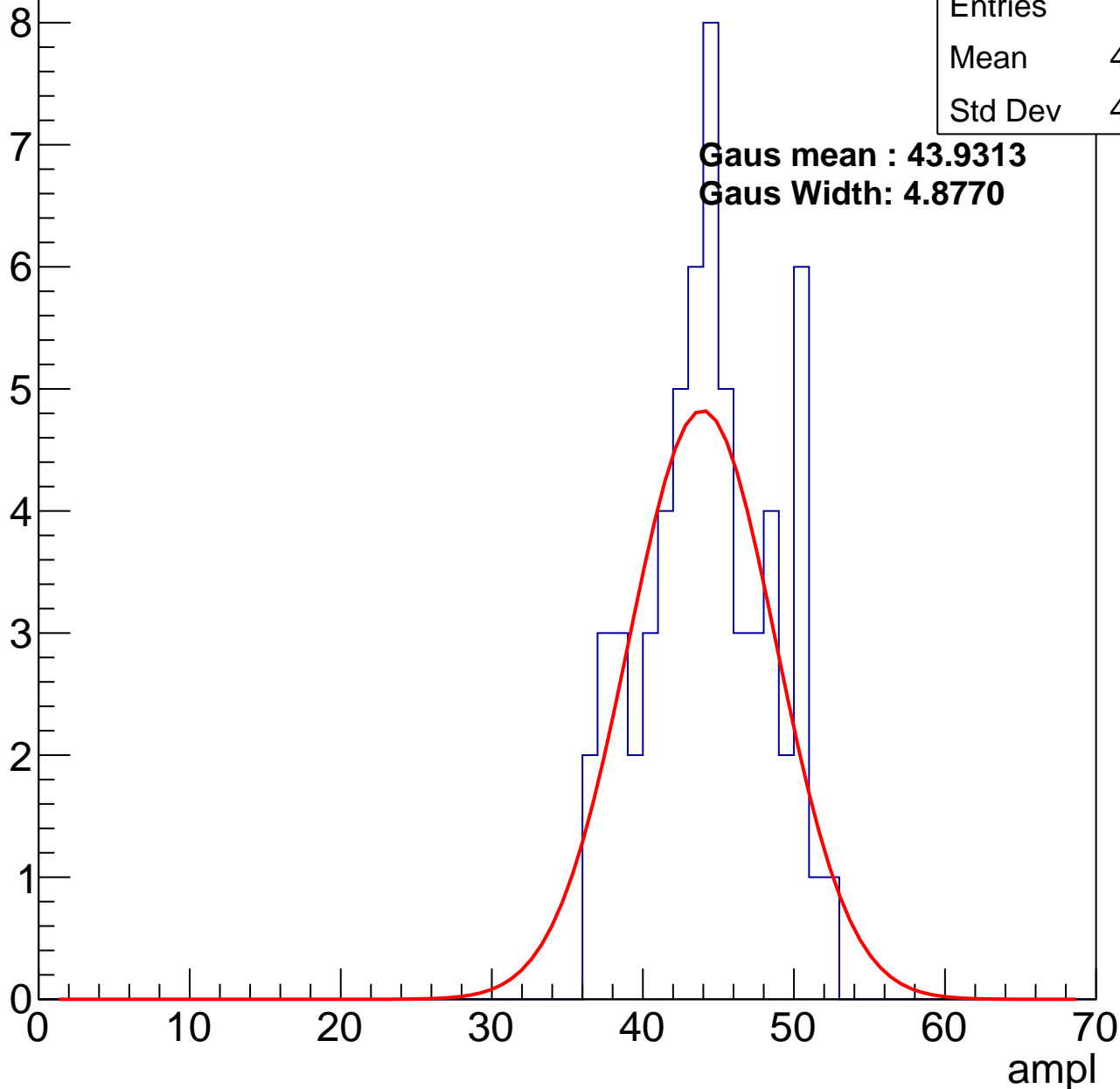
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	43.87
Std Dev	4.107

**Gaus mean : 43.9313**

**Gaus Width: 4.8770**

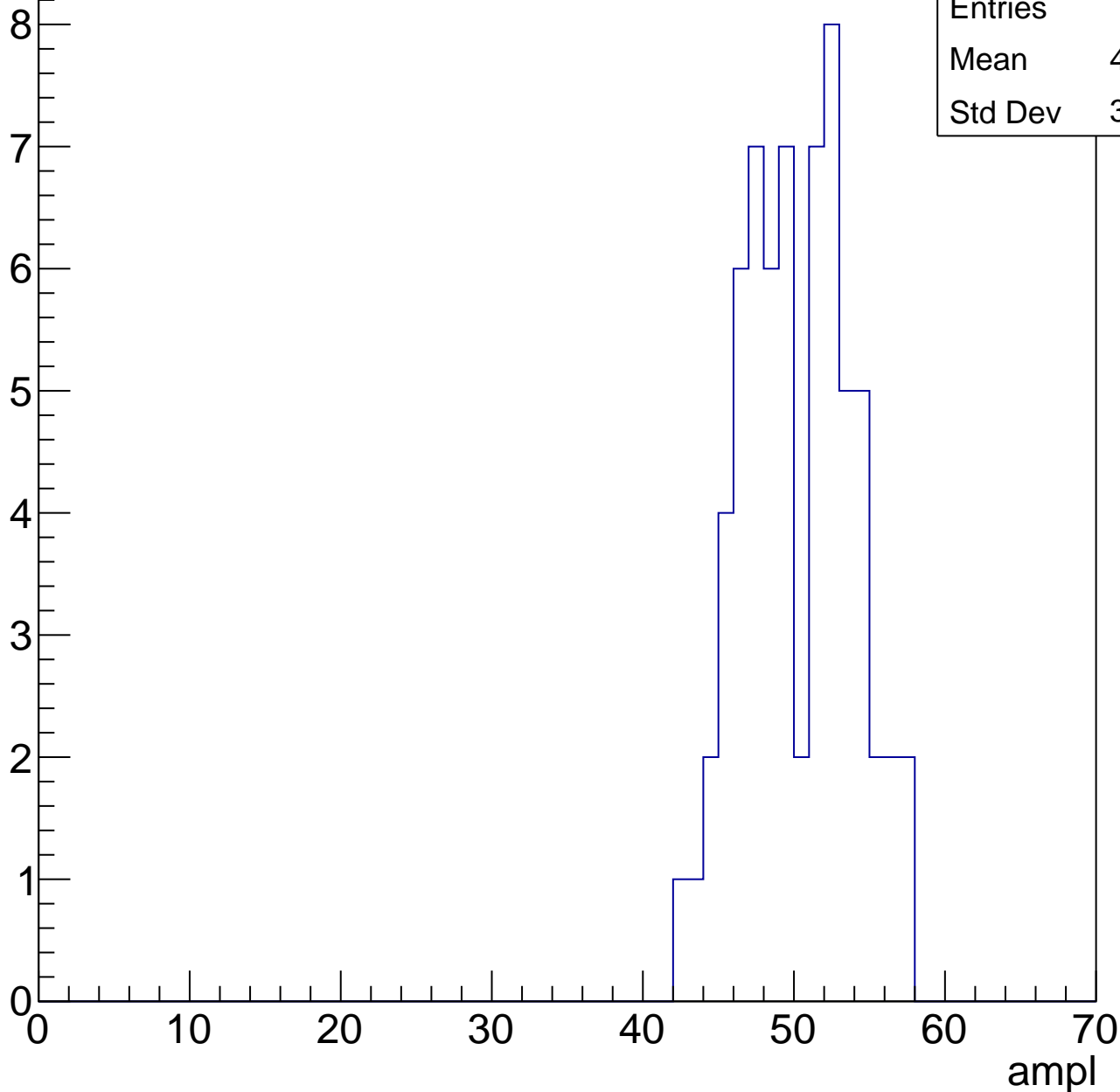


# B0L001S, U17-ch78, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	49.75
Std Dev	3.572

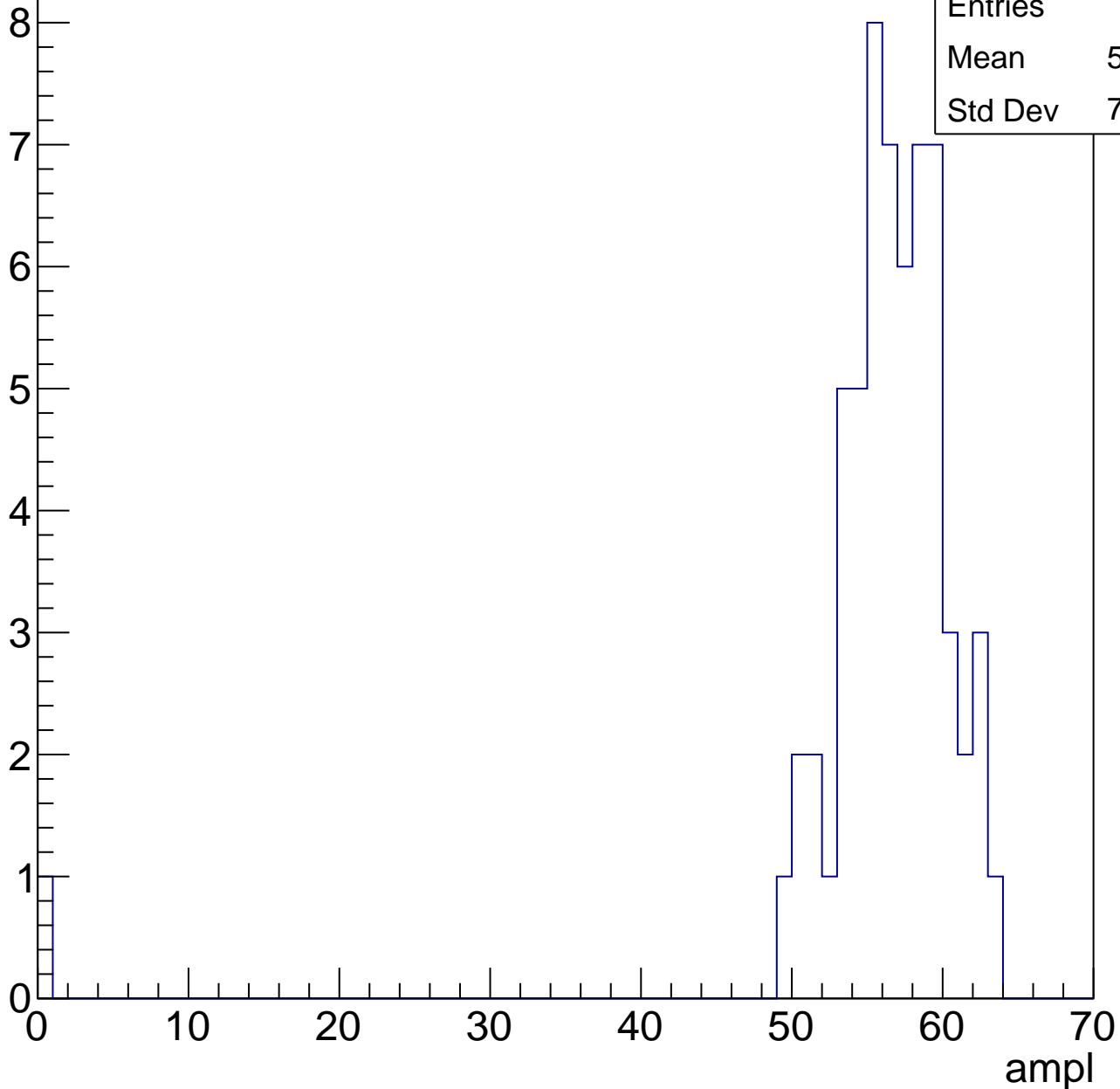


# B0L001S, U17-ch78, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	55.44
Std Dev	7.819



# B0L001S, U17-ch78, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

7

6

5

4

3

2

1

0

Entries

34

Mean

60.44

Std Dev

1.866

0

10

20

30

40

50

60

70

ampl

0

10

20

30

40

50

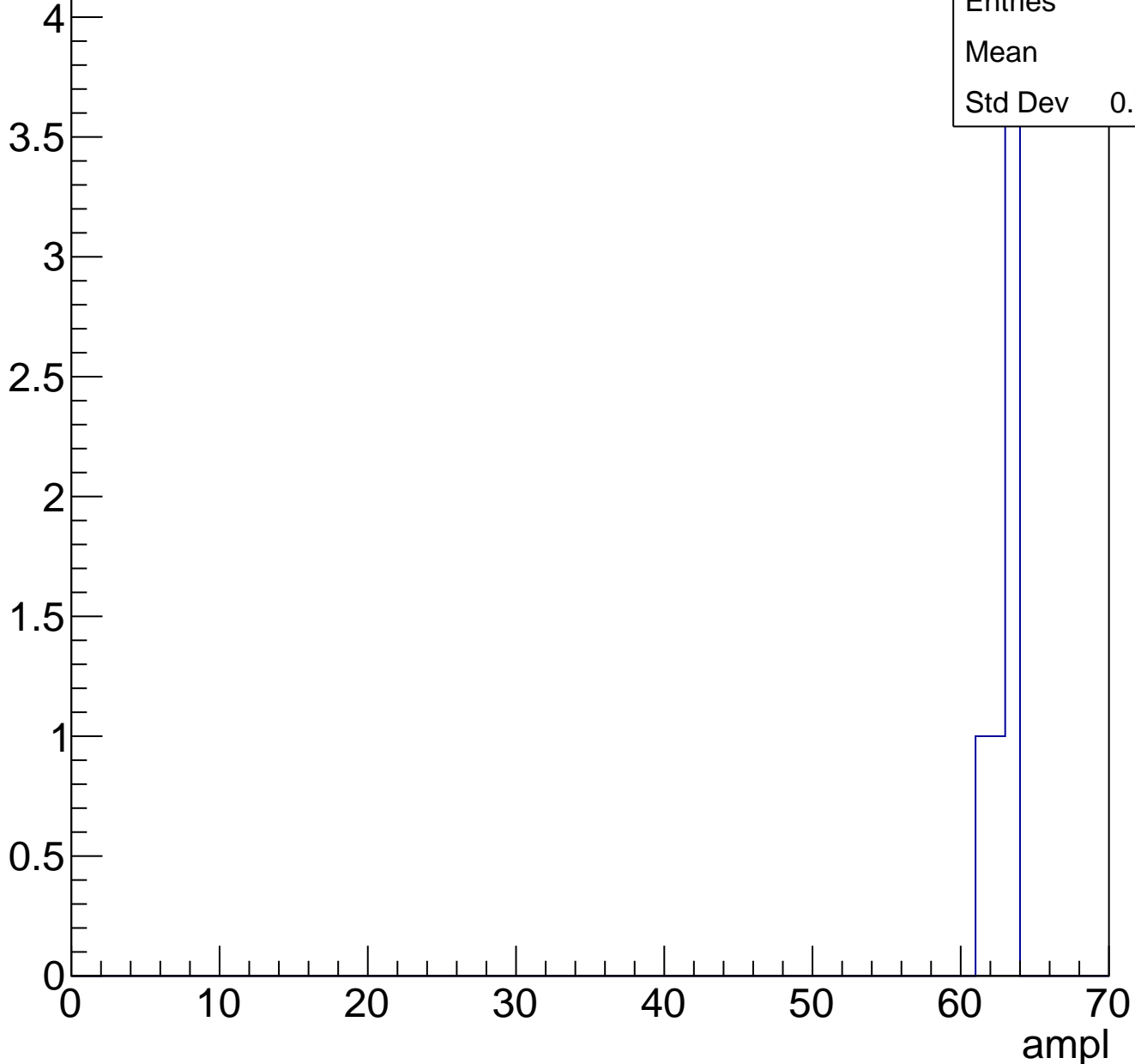
60

70

# B0L001S, U17-ch78, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch78, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U17-ch79, adc0

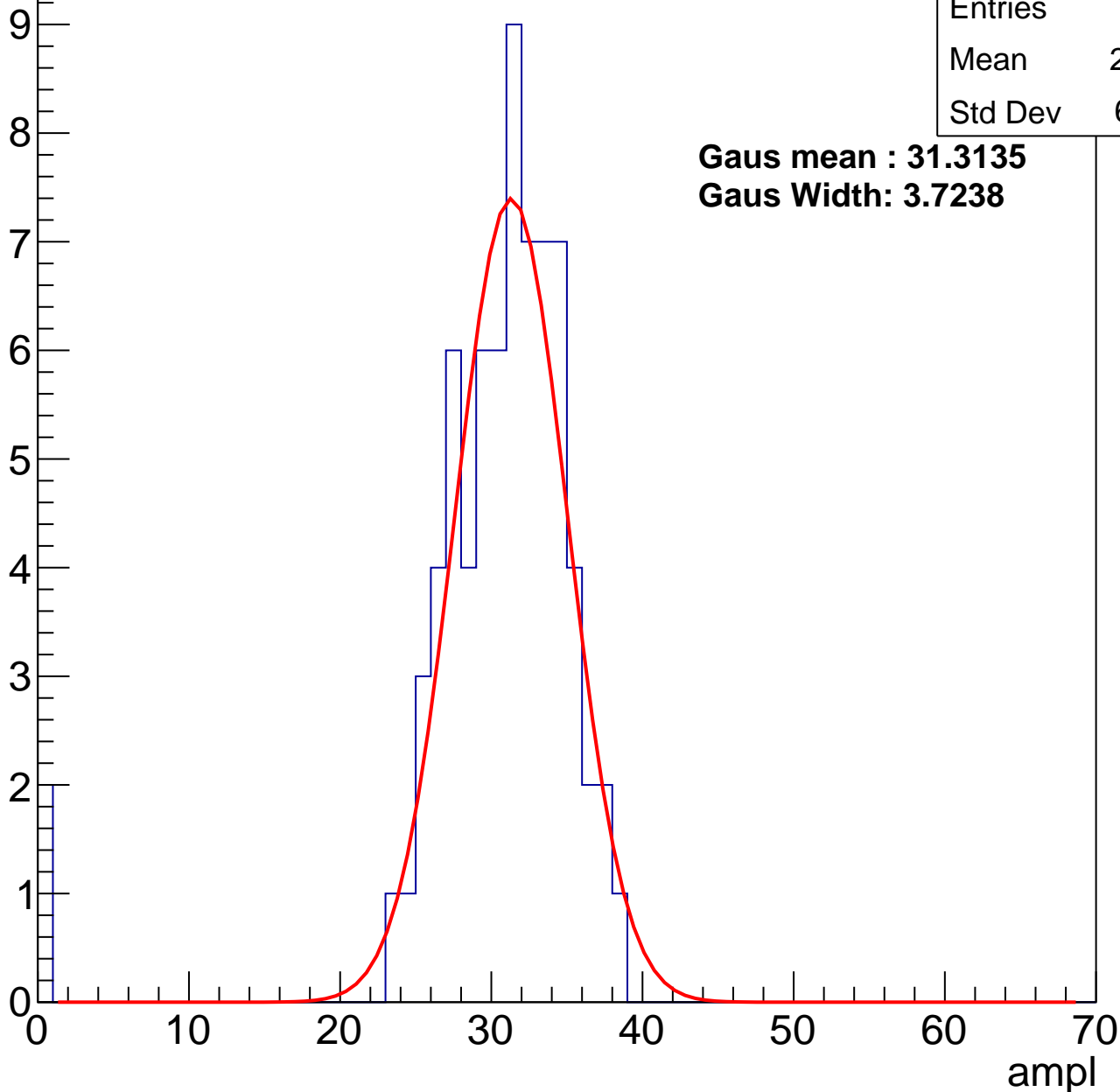
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	29.86
Std Dev	6.061

**Gaus mean : 31.3135**

**Gaus Width: 3.7238**



# B0L001S, U17-ch79, adc1

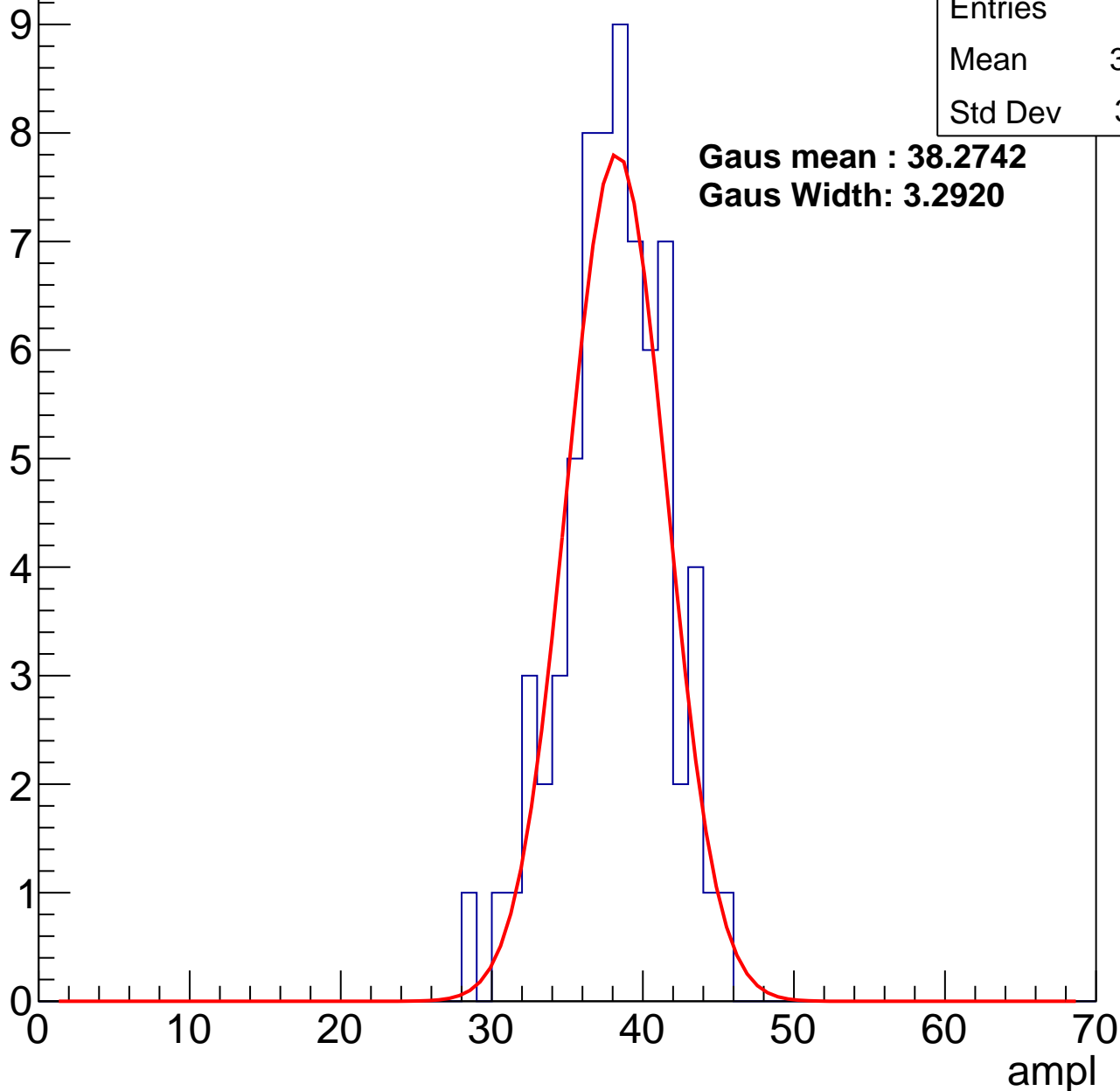
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	37.67
Std Dev	3.421

**Gaus mean : 38.2742**

**Gaus Width: 3.2920**



# B0L001S, U17-ch79, adc2

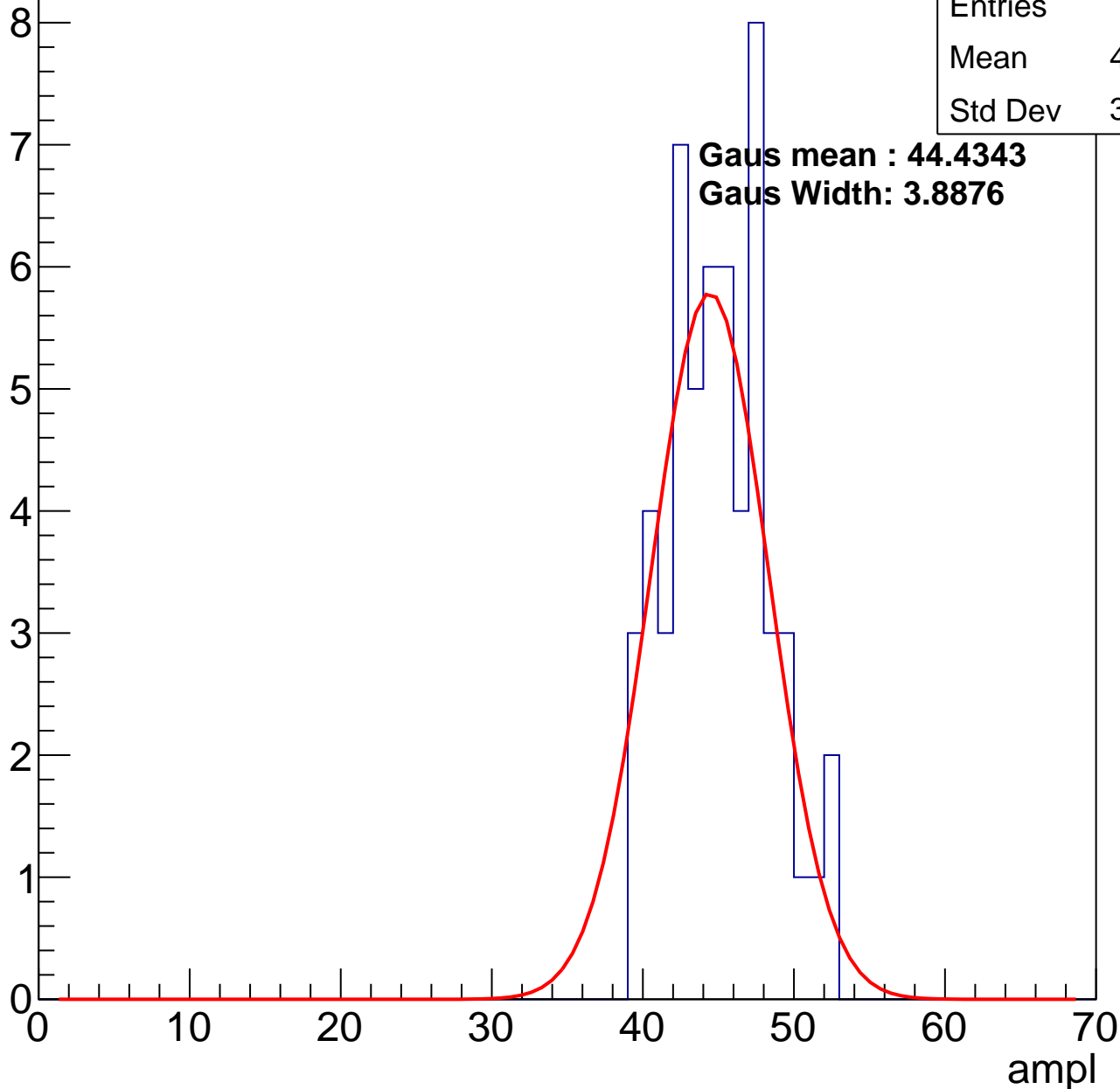
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	44.62
Std Dev	3.293

**Gaus mean : 44.4343**

**Gaus Width: 3.8876**

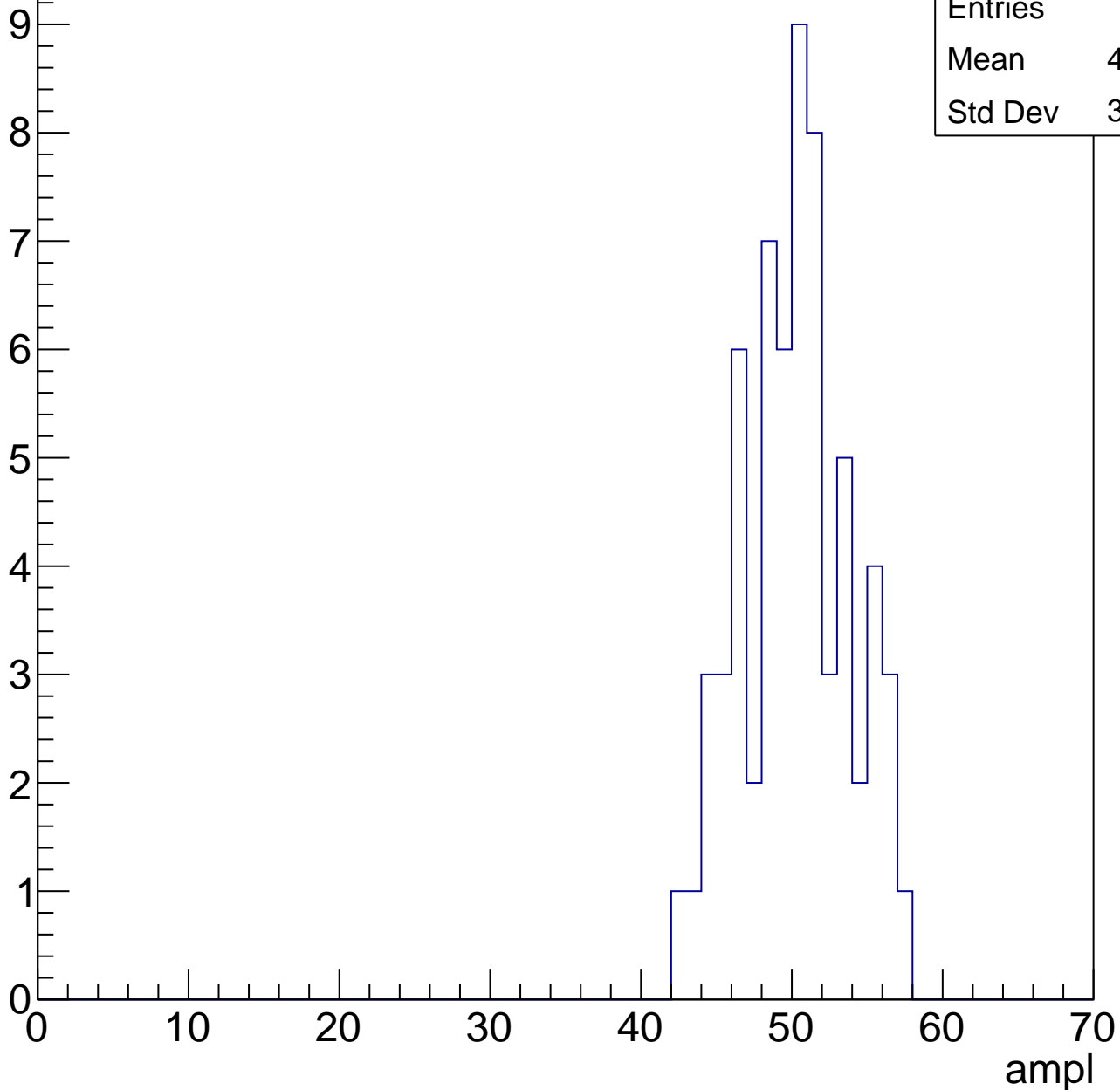


# B0L001S, U17-ch79, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	49.75
Std Dev	3.522

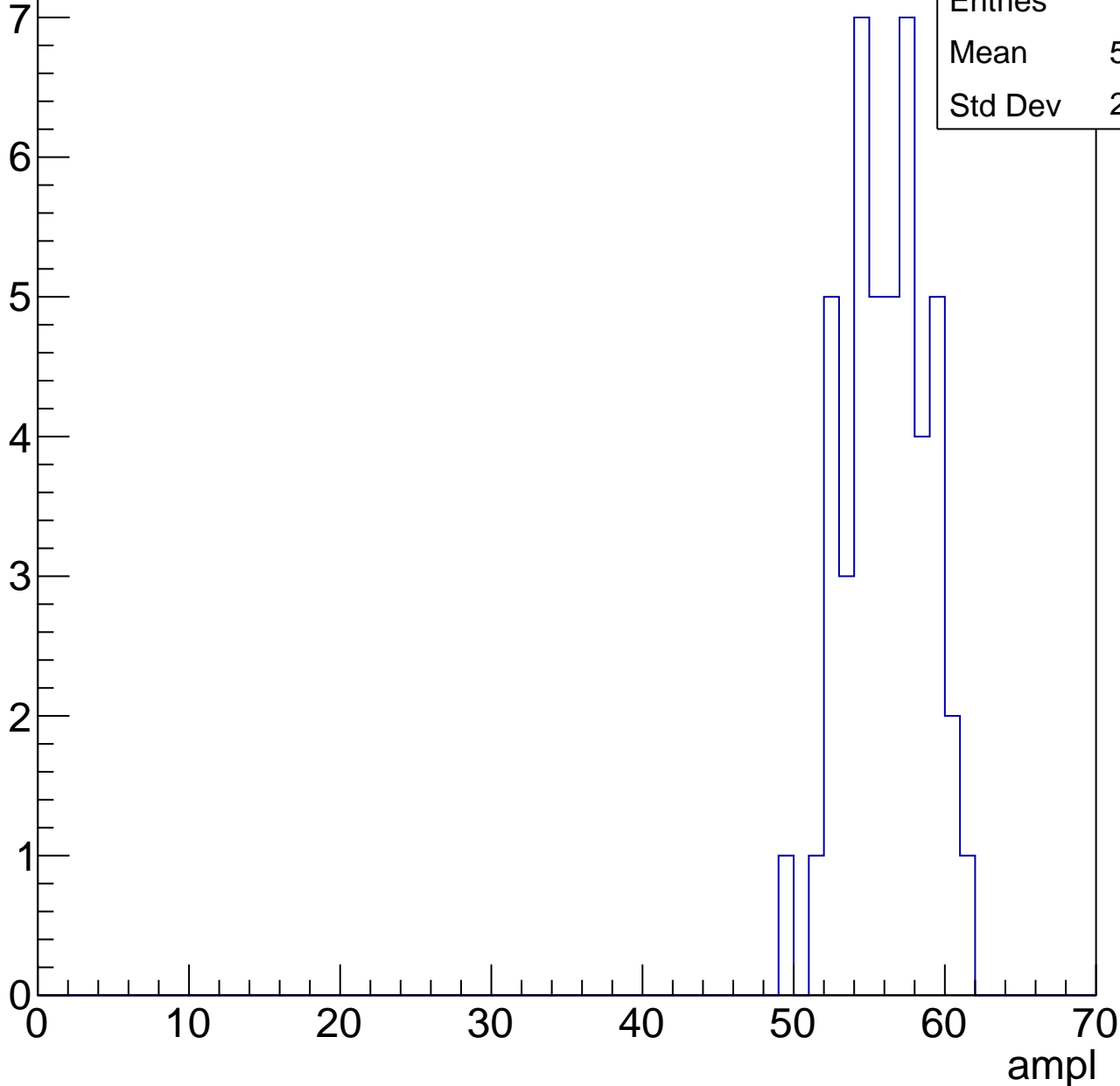


# B0L001S, U17-ch79, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	46
Mean	55.63
Std Dev	2.689

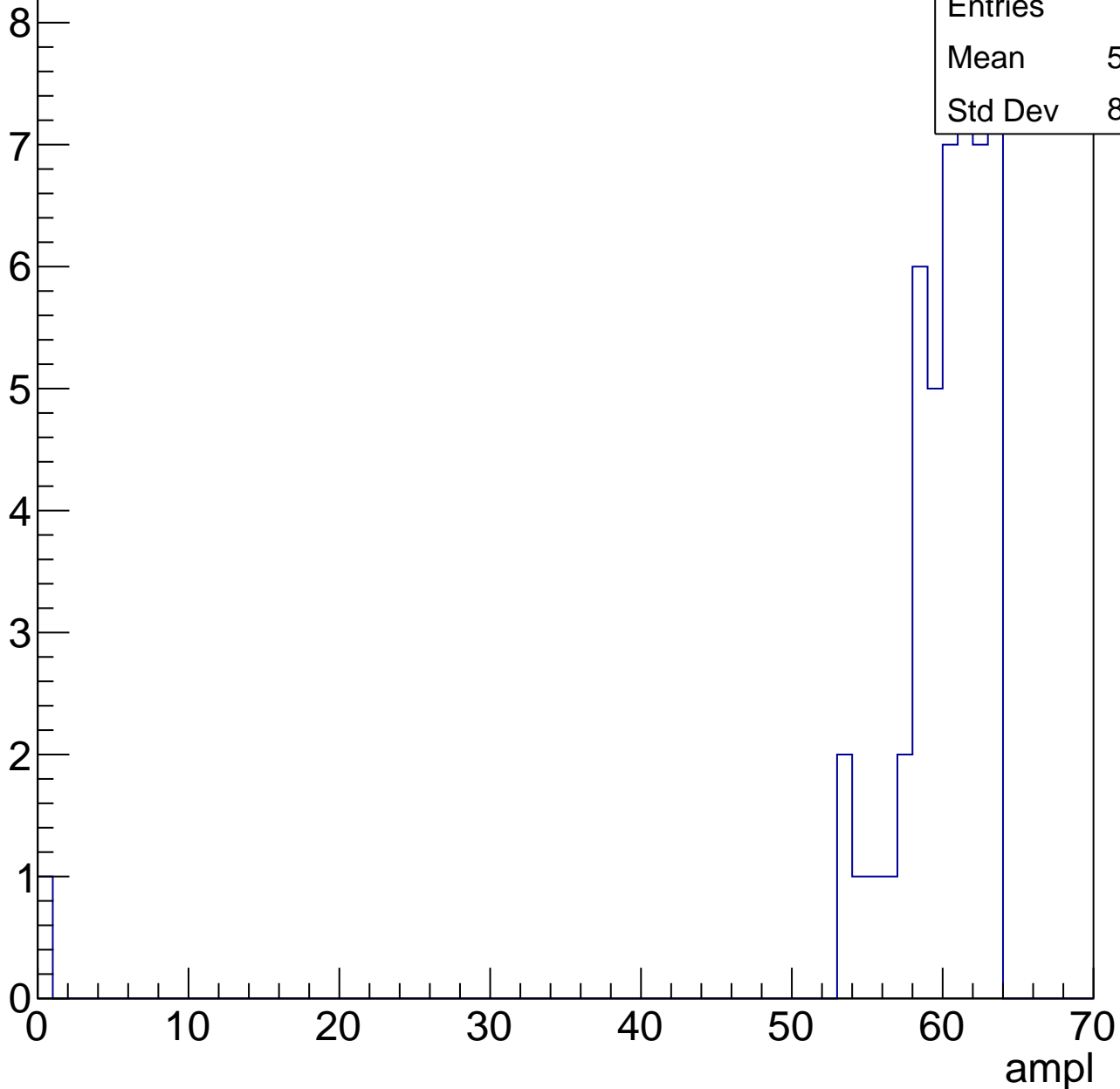


# B0L001S, U17-ch79, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

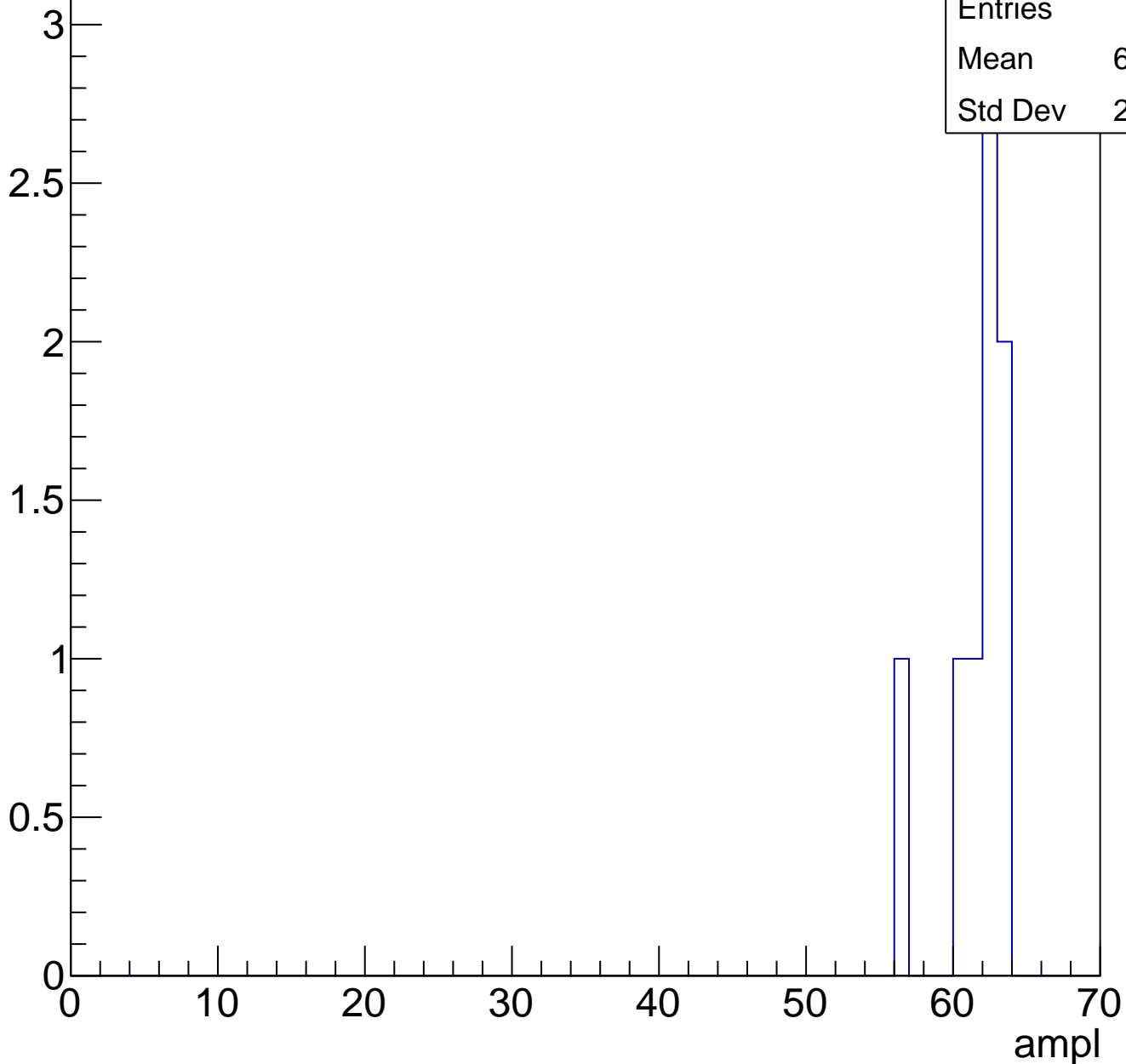
Entries	49
Mean	58.65
Std Dev	8.854



# B0L001S, U17-ch79, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch79, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U17-ch80, adc0

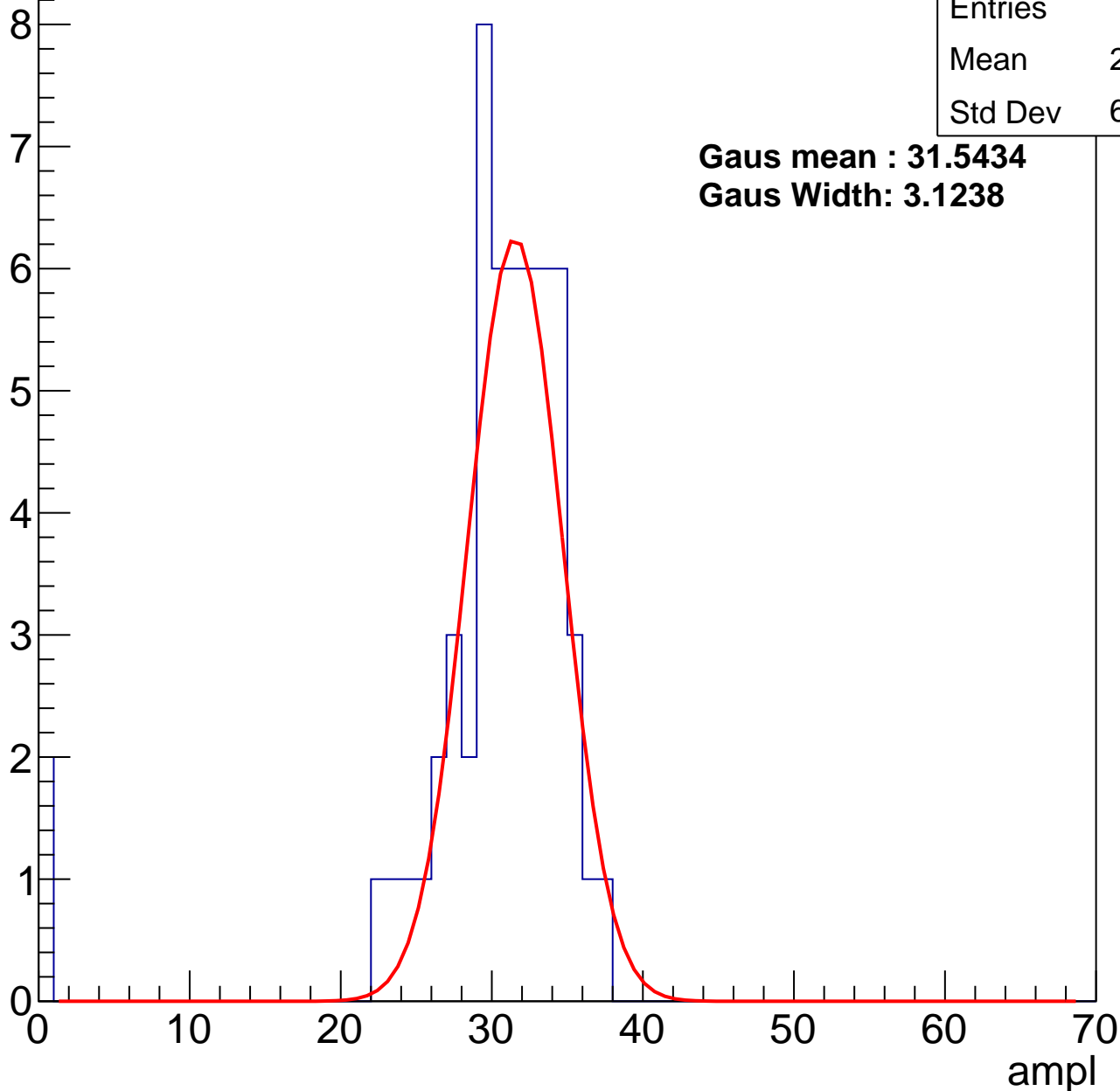
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	29.52
Std Dev	6.514

**Gaus mean : 31.5434**

**Gaus Width: 3.1238**



# B0L001S, U17-ch80, adc1

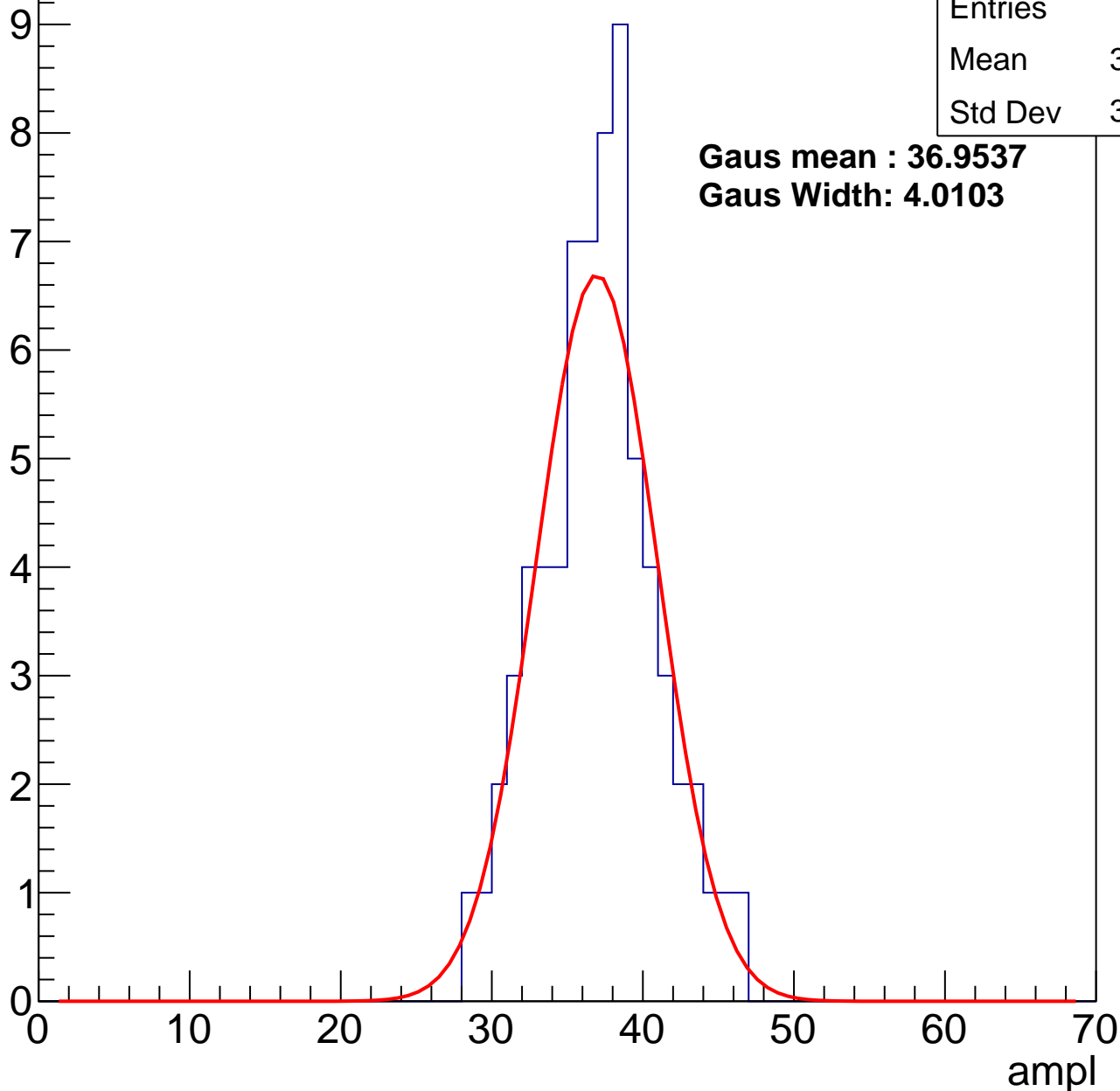
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	36.58
Std Dev	3.812

**Gaus mean : 36.9537**

**Gaus Width: 4.0103**



# B0L001S, U17-ch80, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

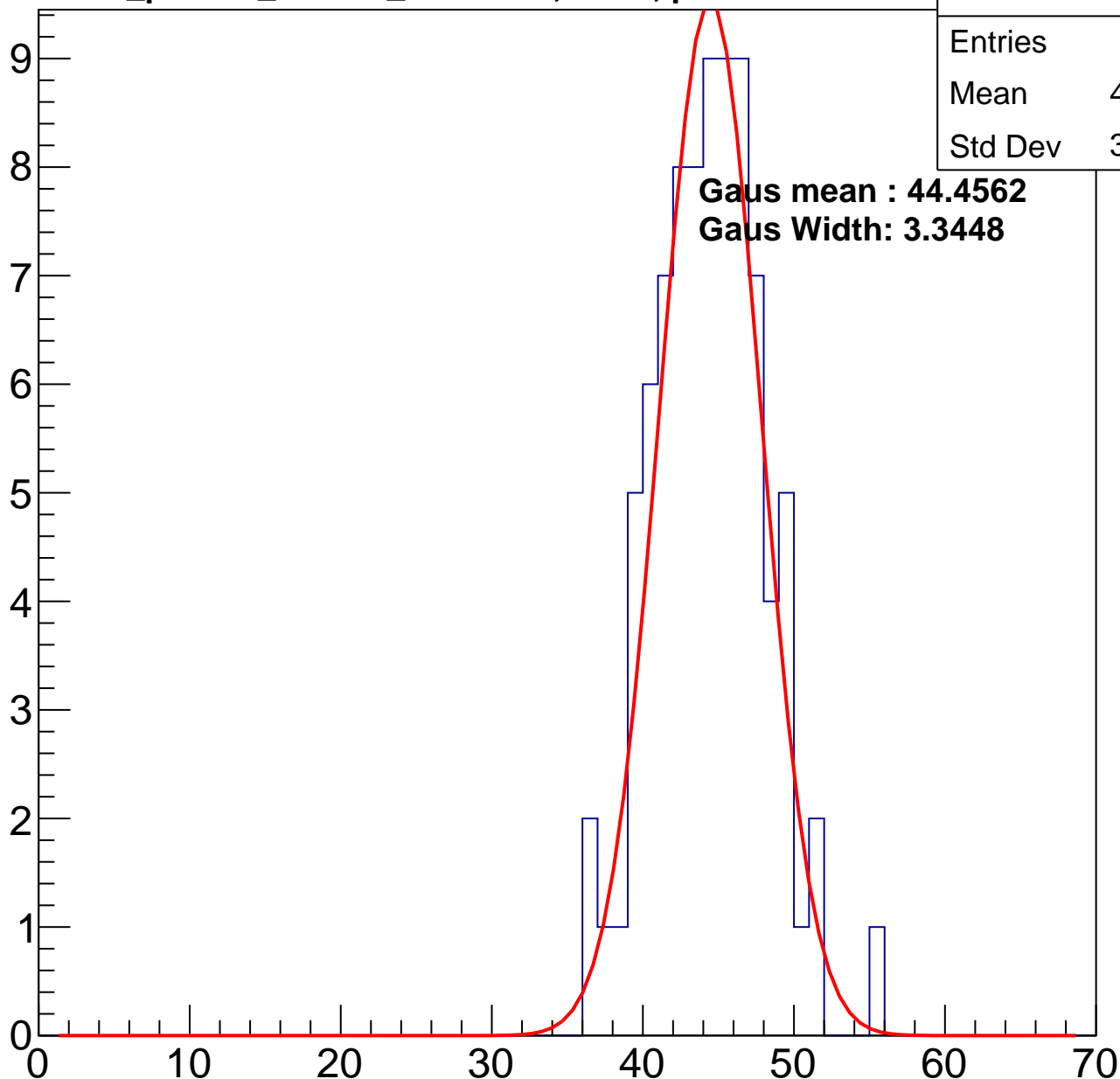
9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	85
Mean	43.96
Std Dev	3.579

**Gaus mean : 44.4562**

**Gaus Width: 3.3448**

ampl

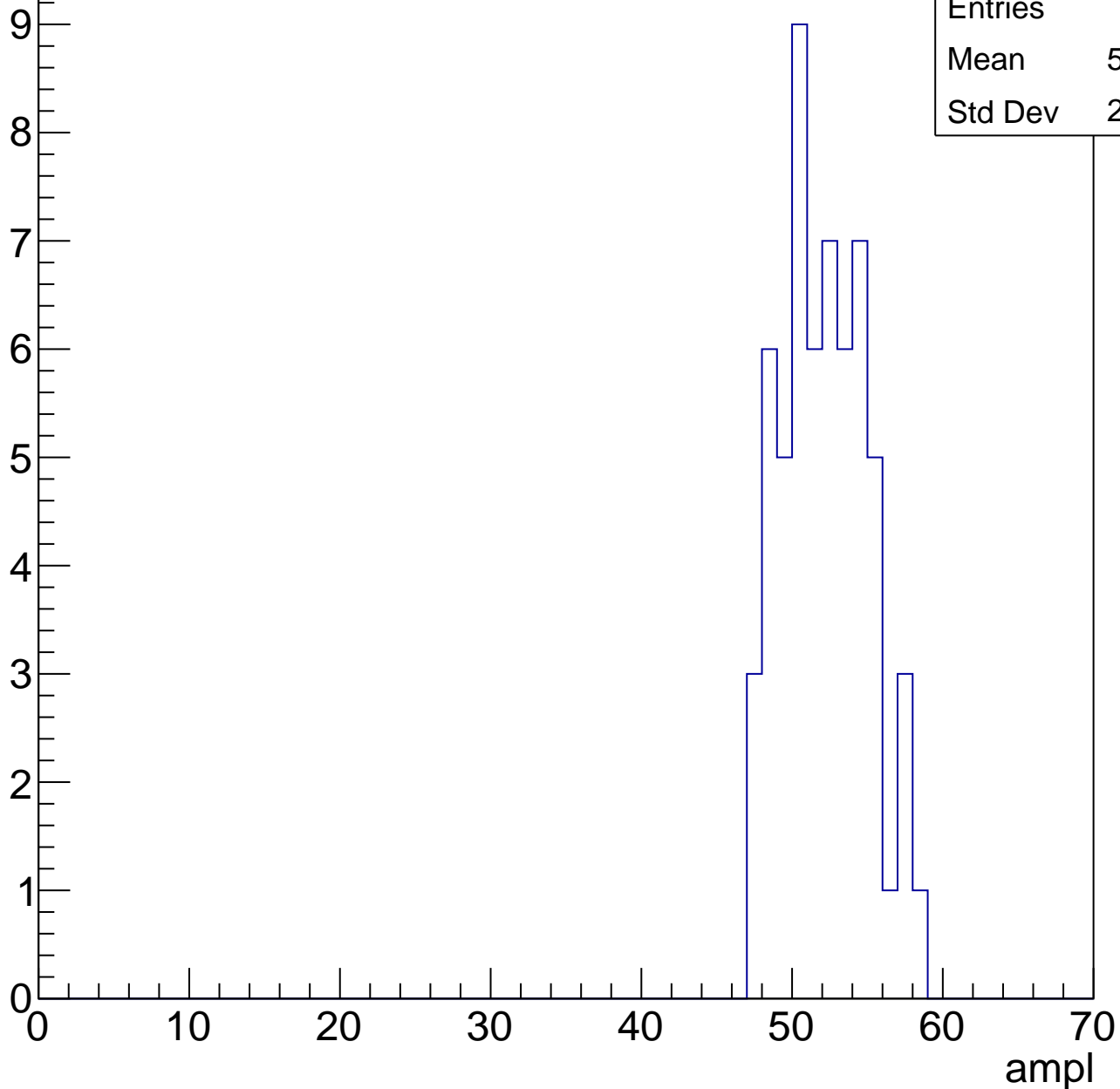


# B0L001S, U17-ch80, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	51.69
Std Dev	2.788

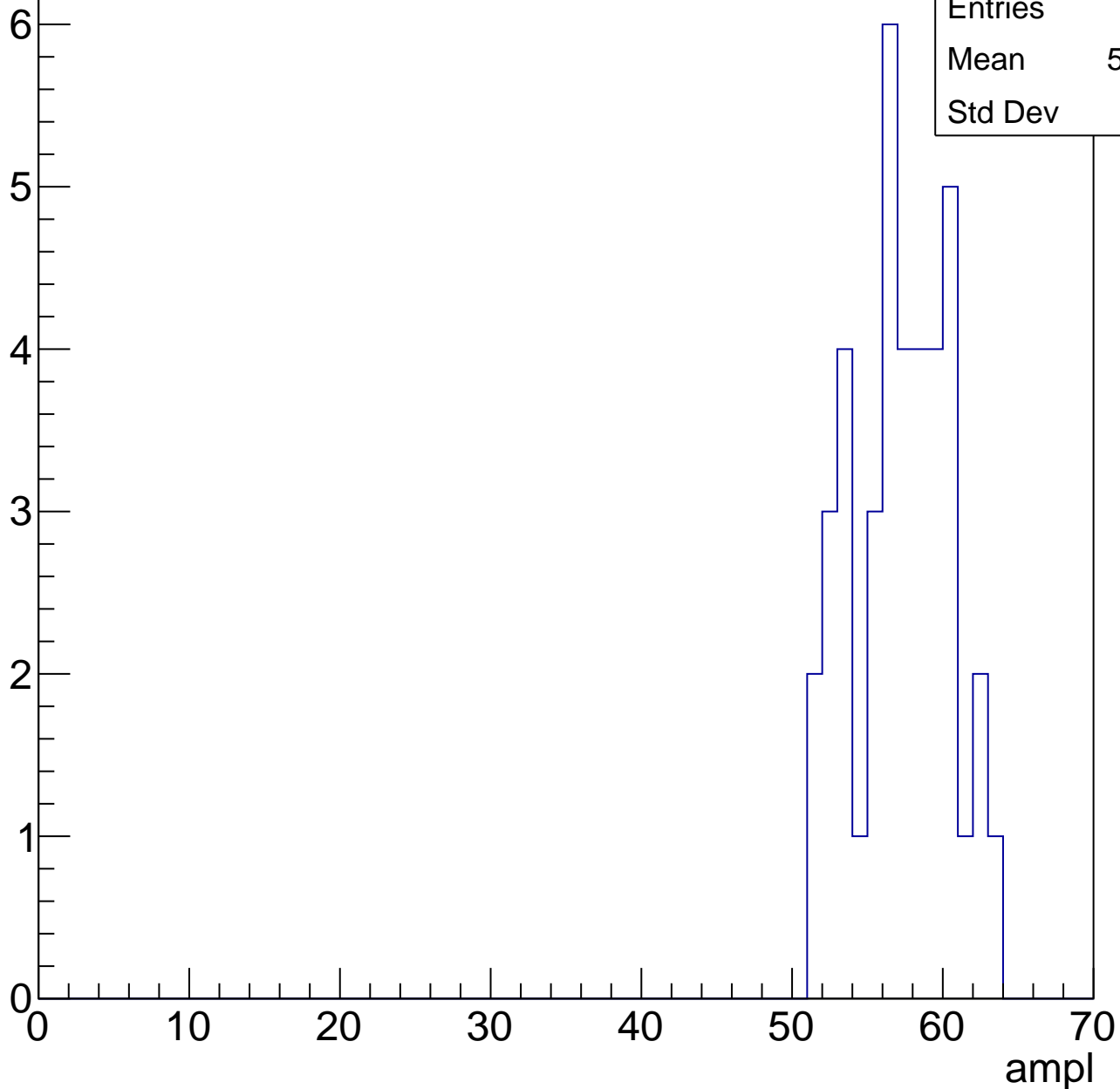


# B0L001S, U17-ch80, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	40
Mean	56.73
Std Dev	3.17

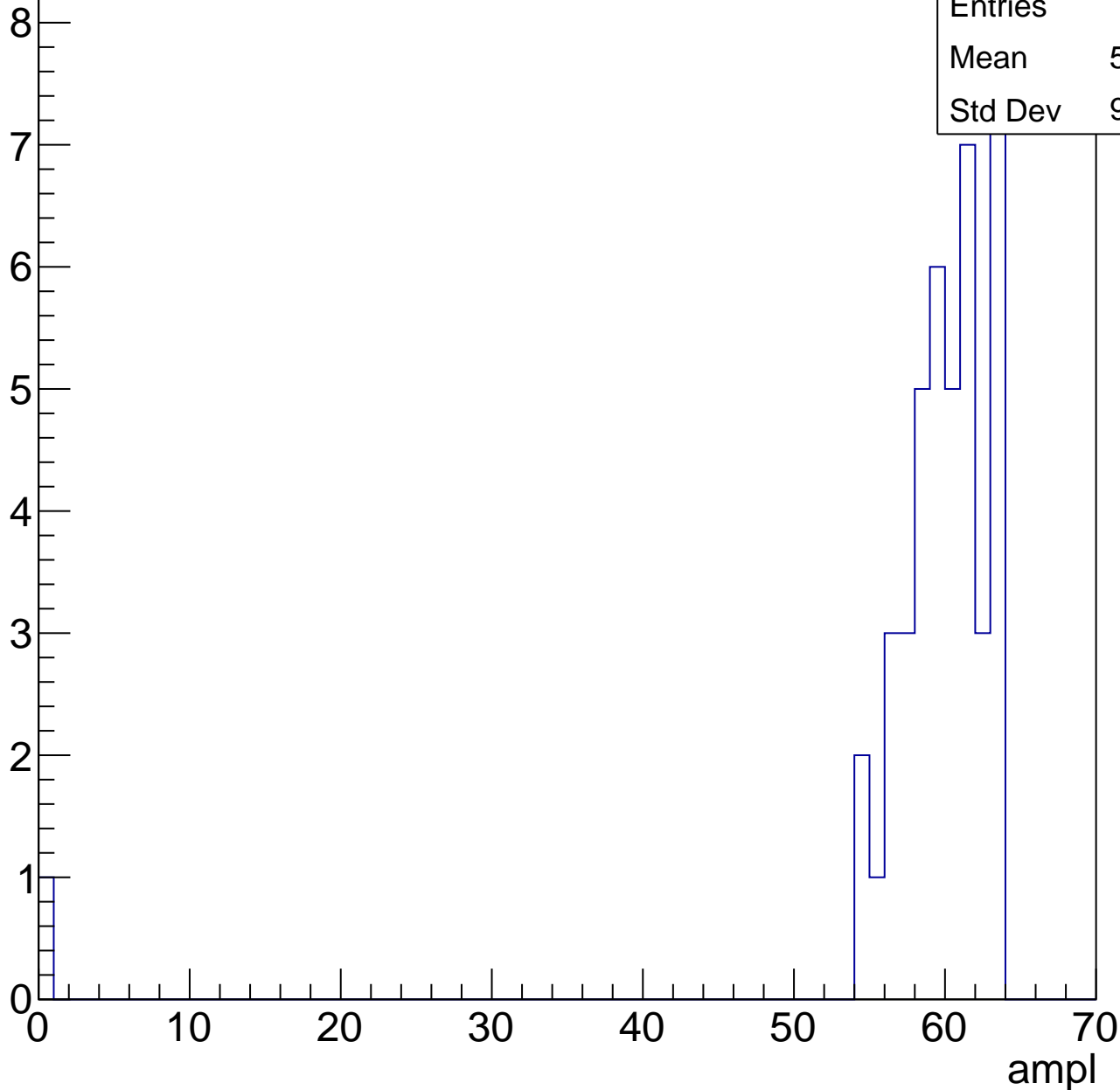


# B0L001S, U17-ch80, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

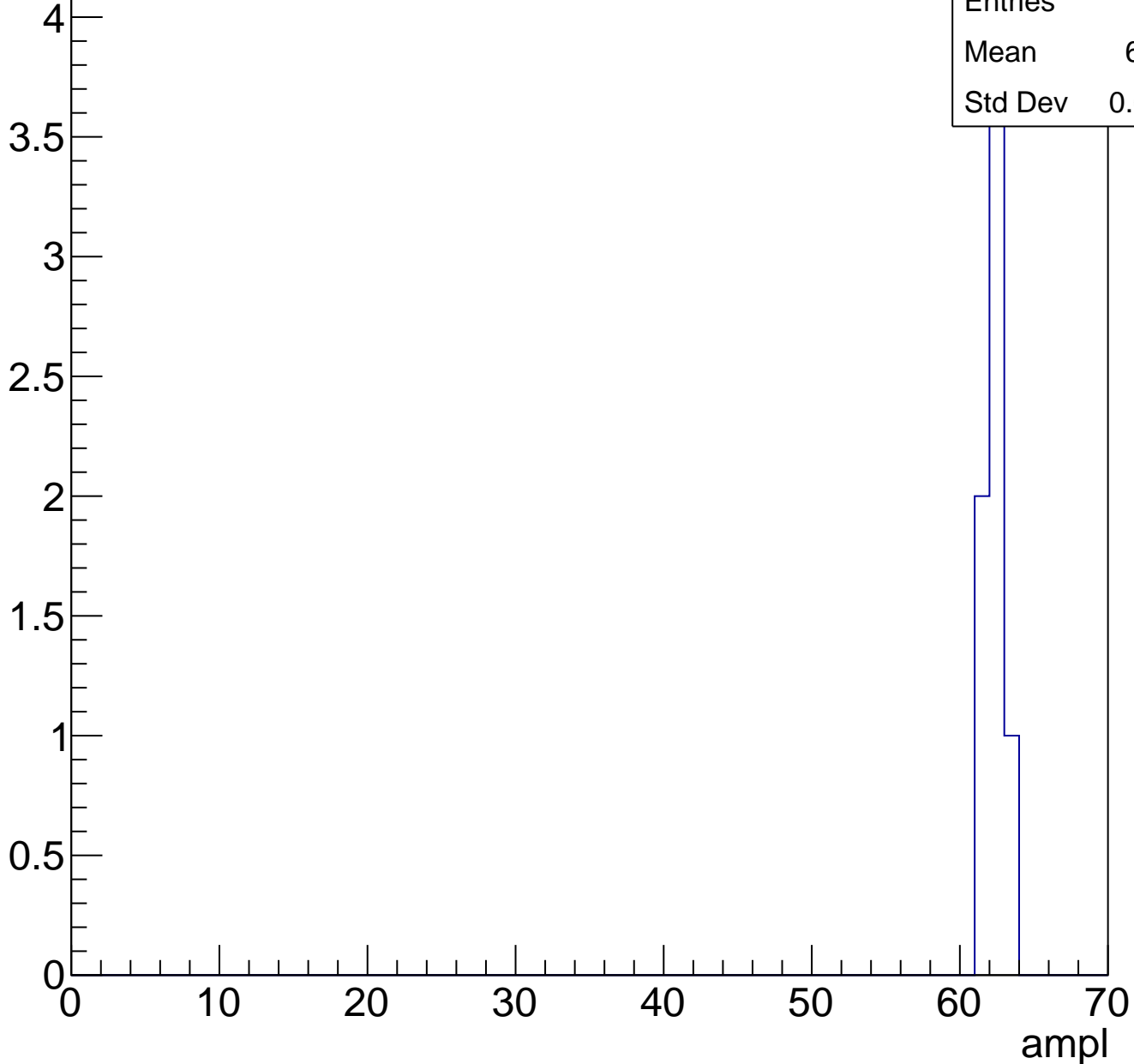
Entries	44
Mean	58.25
Std Dev	9.237



# B0L001S, U17-ch80, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch80, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	3
Mean	20.67
Std Dev	29.23

# B0L001S, U17-ch81, adc0

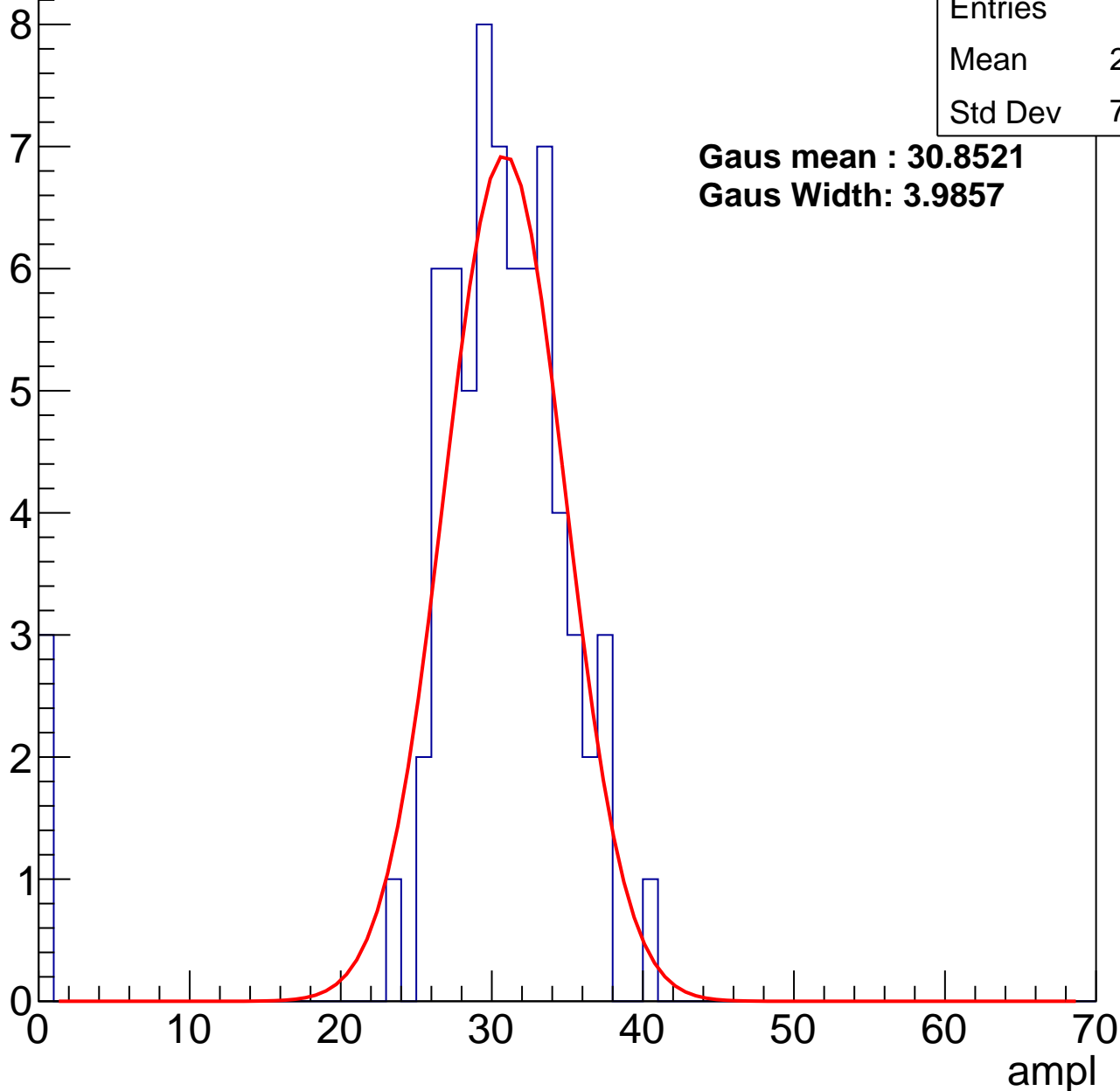
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	29.23
Std Dev	7.057

**Gaus mean : 30.8521**

**Gaus Width: 3.9857**



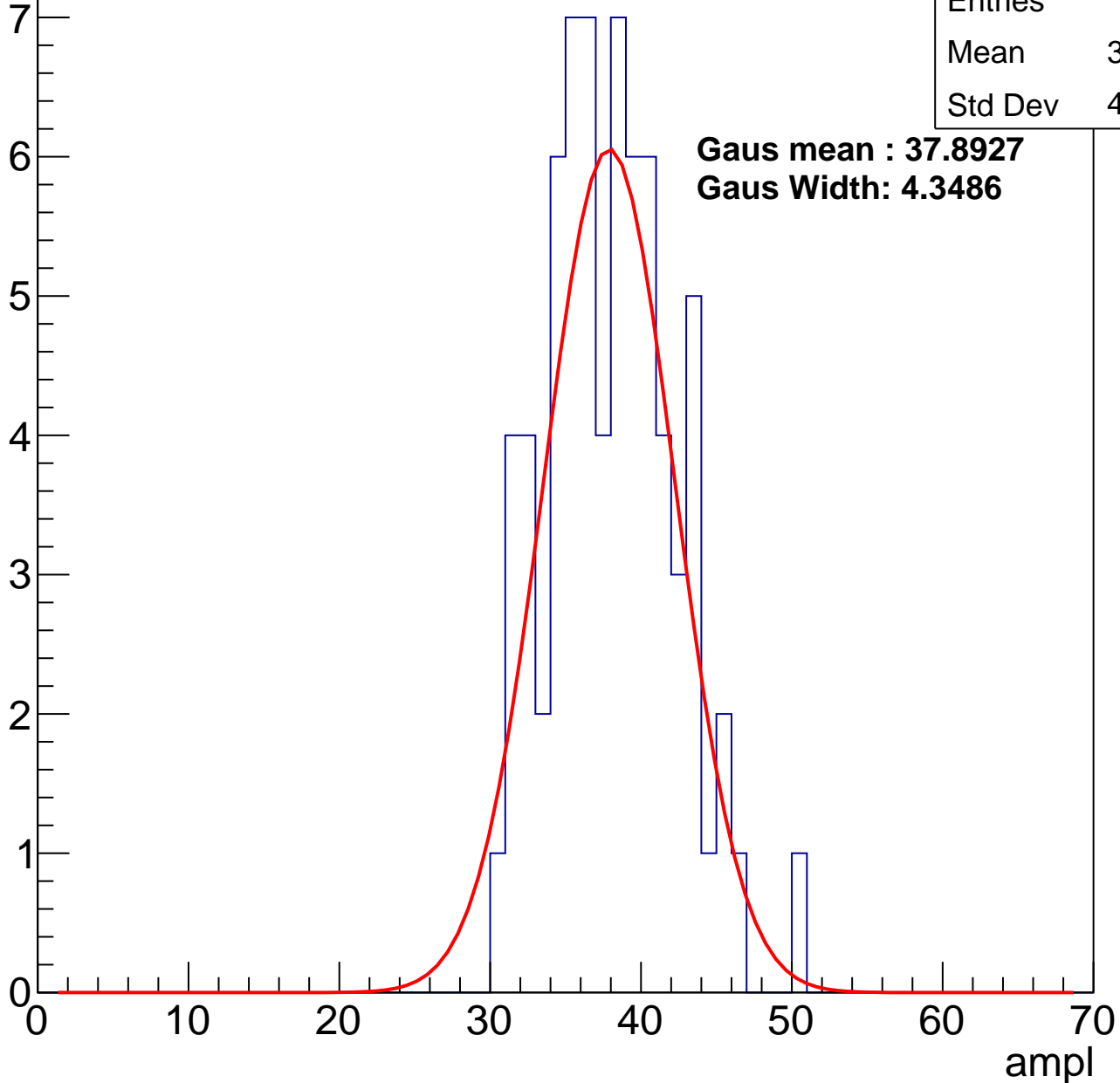
# B0L001S, U17-ch81, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	37.63
Std Dev	4.139

**Gaus mean : 37.8927**  
**Gaus Width: 4.3486**



# B0L001S, U17-ch81, adc2

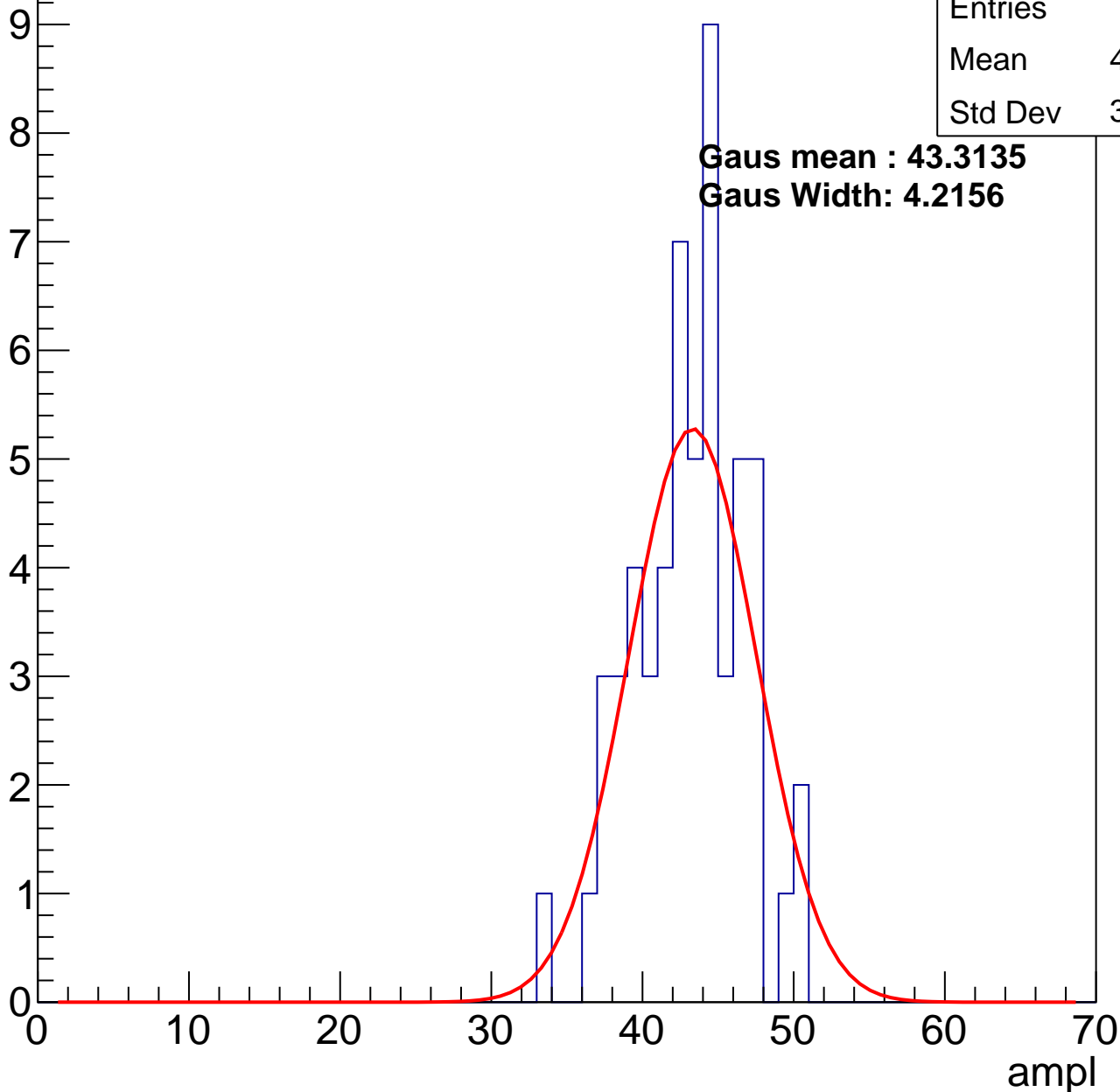
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	42.64
Std Dev	3.583

**Gaus mean : 43.3135**

**Gaus Width: 4.2156**

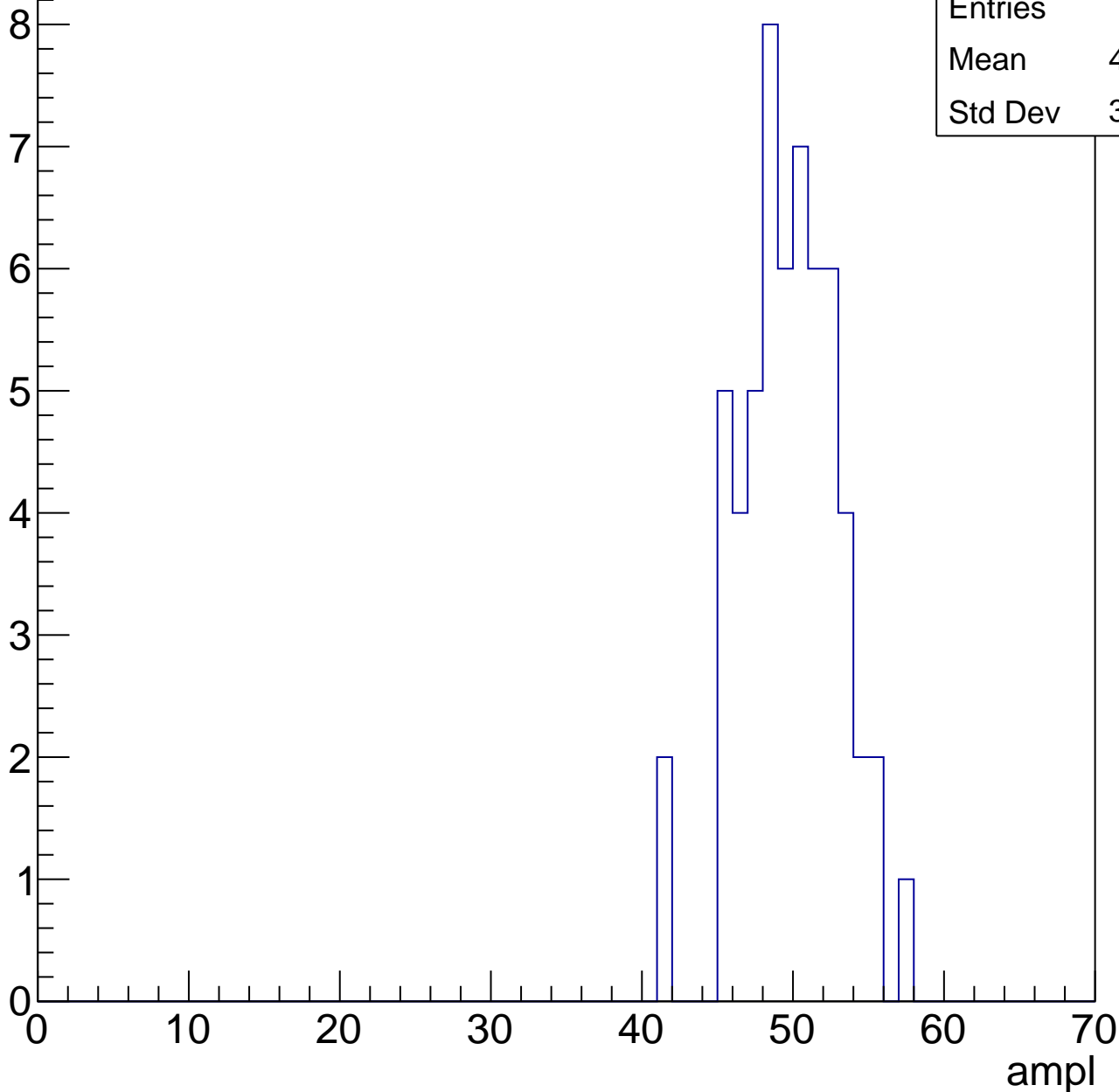


# B0L001S, U17-ch81, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	49.29
Std Dev	3.222

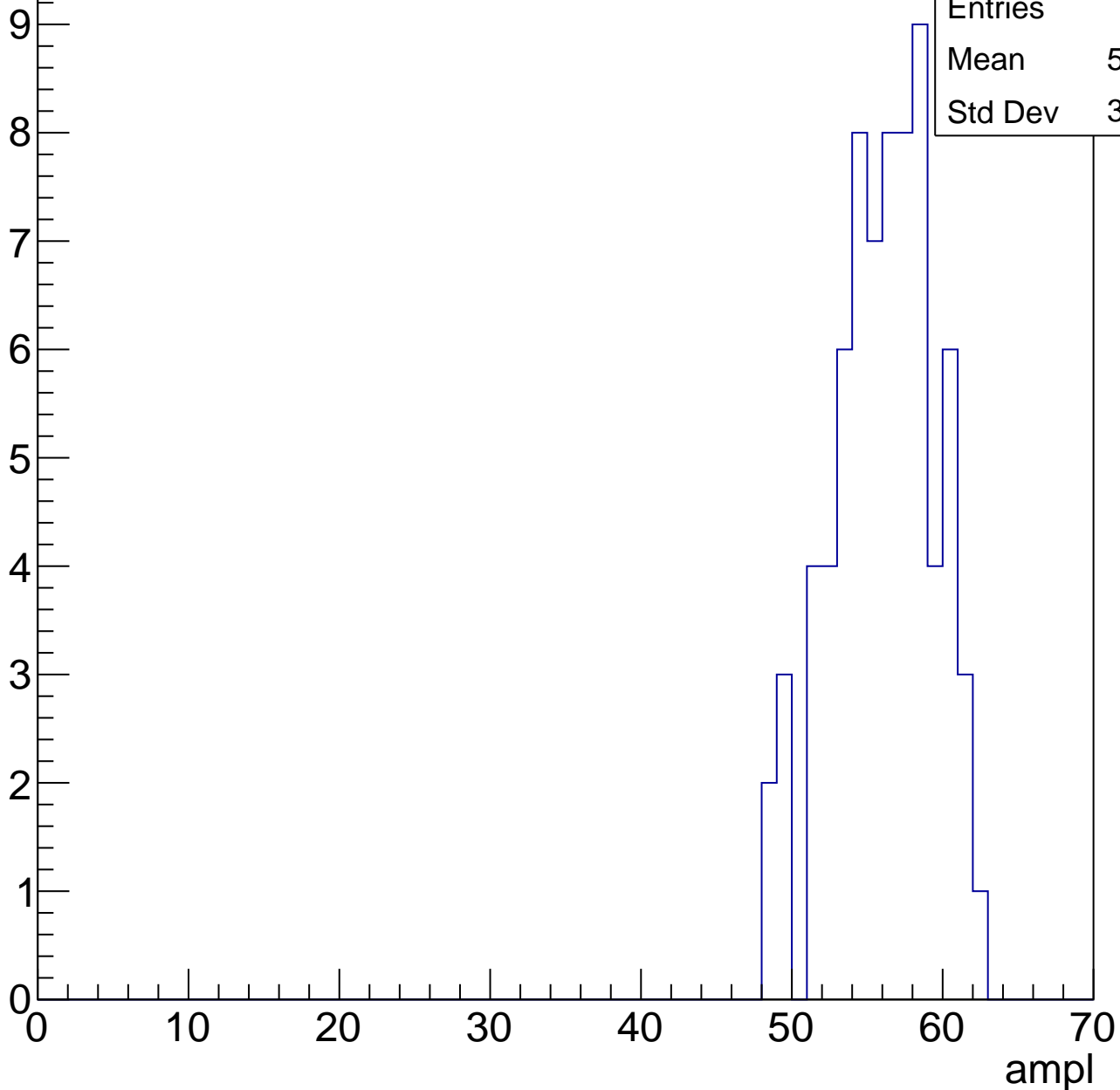


# B0L001S, U17-ch81, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	55.58
Std Dev	3.322

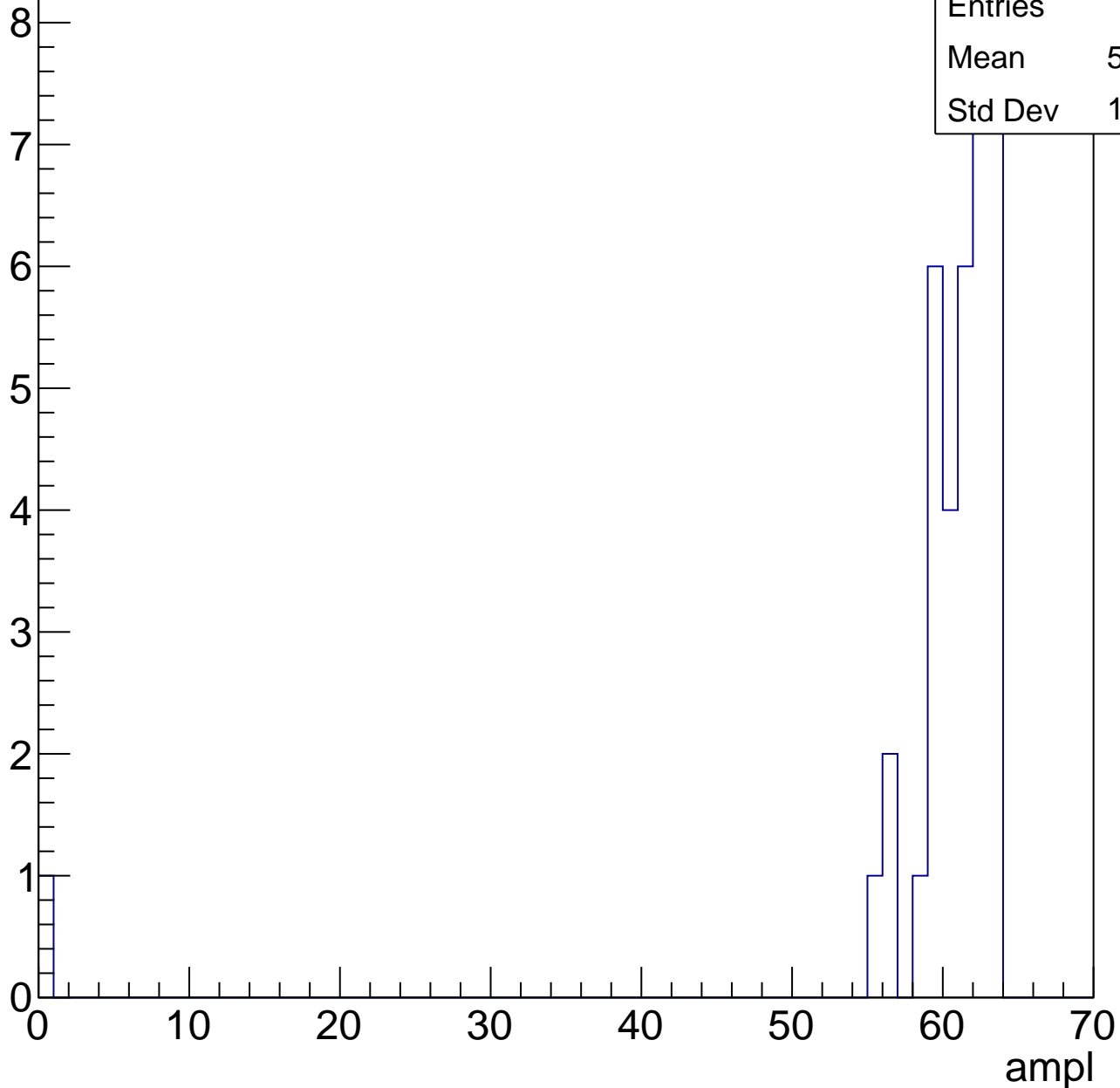


# B0L001S, U17-ch81, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

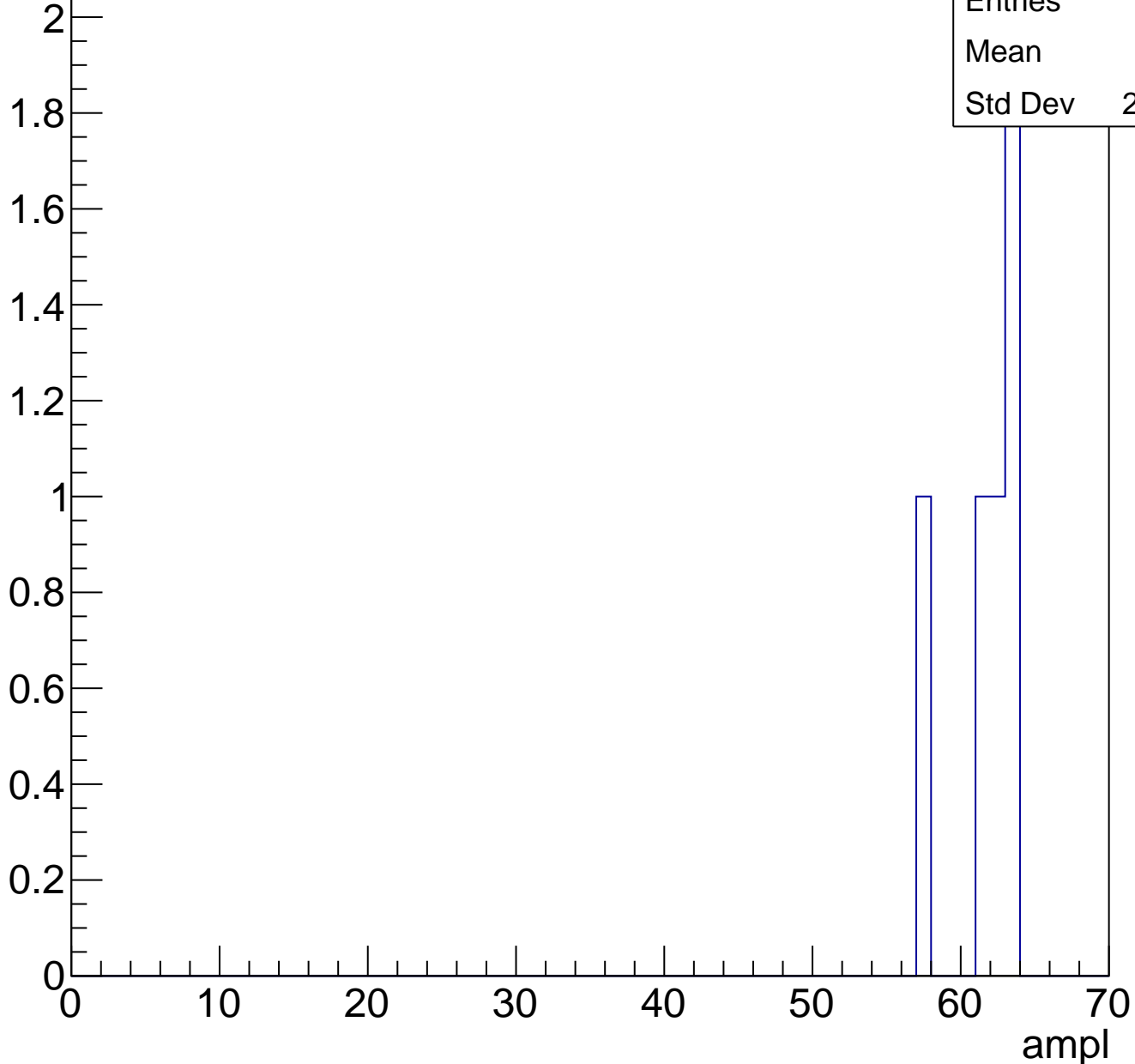
Entries	37
Mean	59.05
Std Dev	10.06



# B0L001S, U17-ch81, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch81, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	3
Mean	0
Std Dev	0

# B0L001S, U17-ch82, adc0

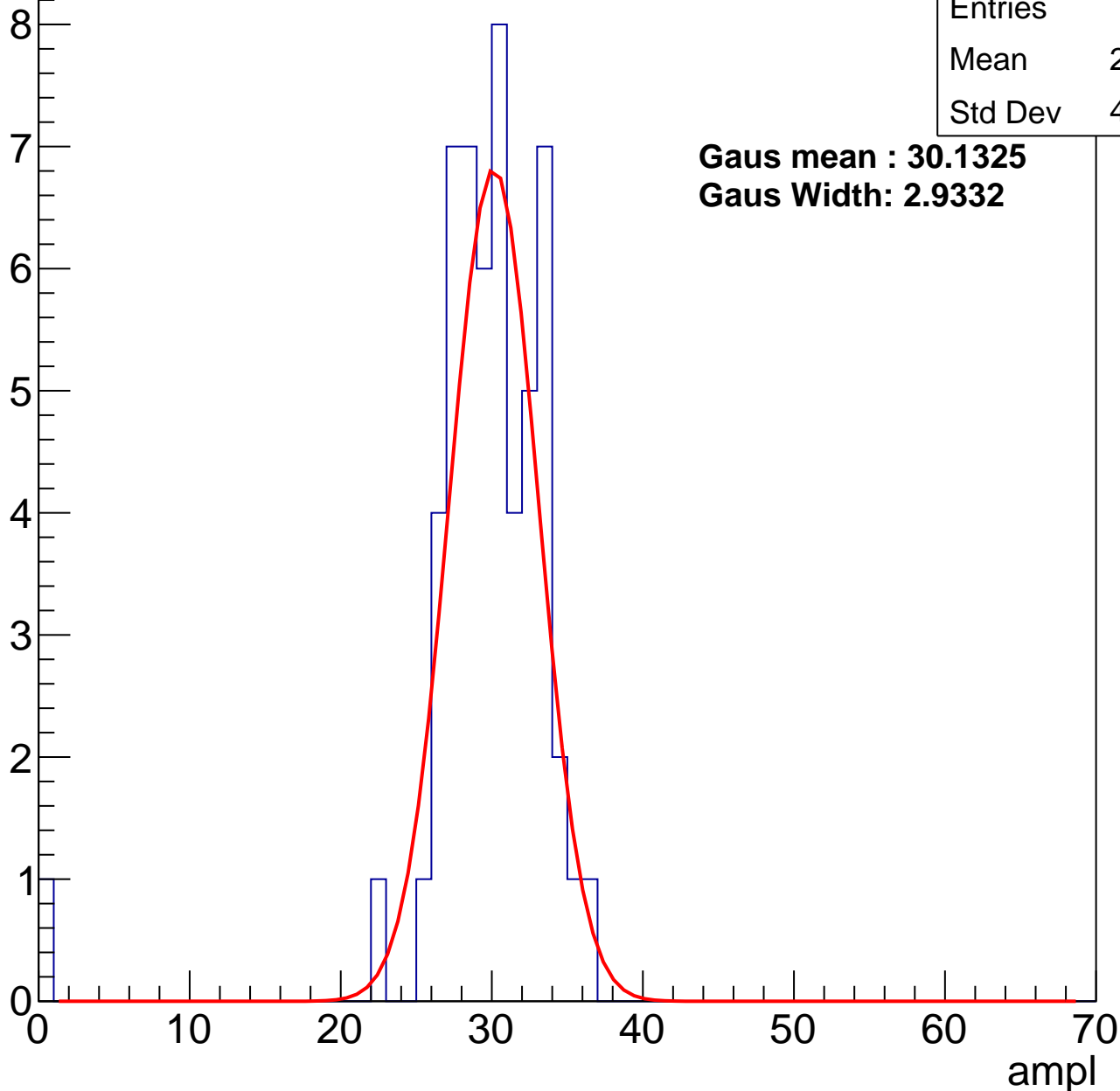
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	29.16
Std Dev	4.846

**Gaus mean : 30.1325**

**Gaus Width: 2.9332**



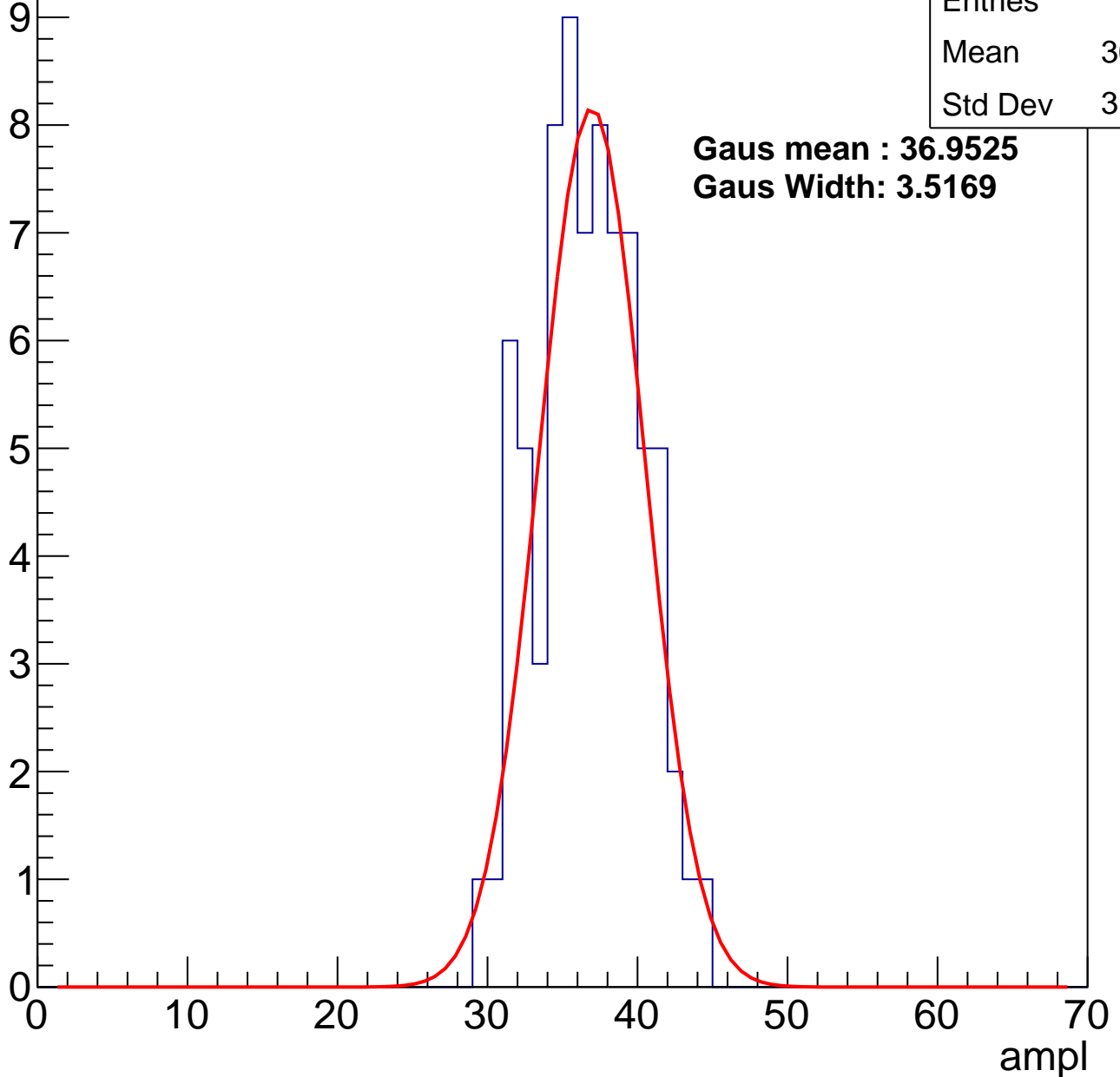
# B0L001S, U17-ch82, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	76
Mean	36.24
Std Dev	3.379

**Gaus mean : 36.9525**  
**Gaus Width: 3.5169**



# B0L001S, U17-ch82, adc2

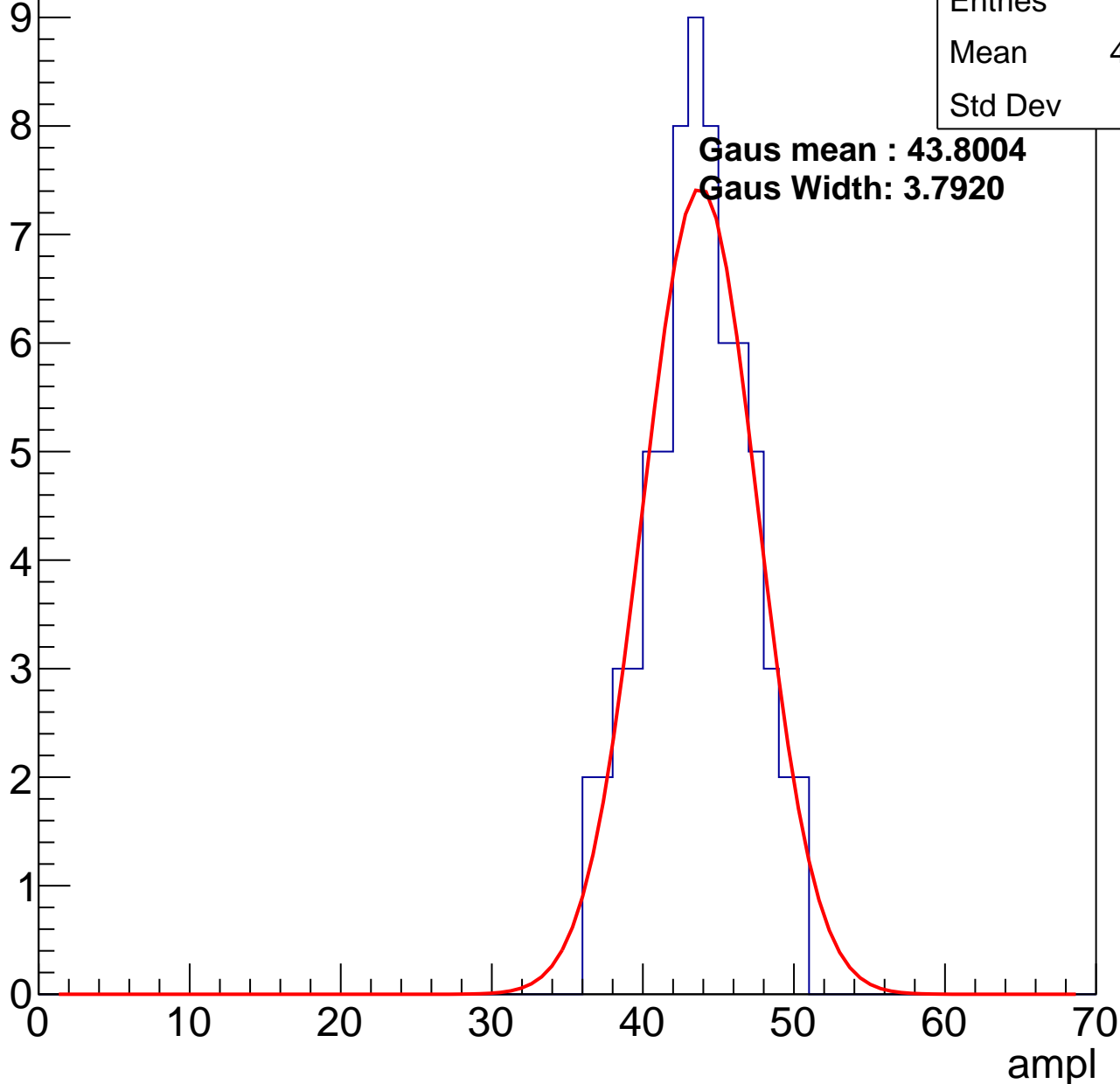
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	43.19
Std Dev	3.35

**Gaus mean : 43.8004**

**Gaus Width: 3.7920**

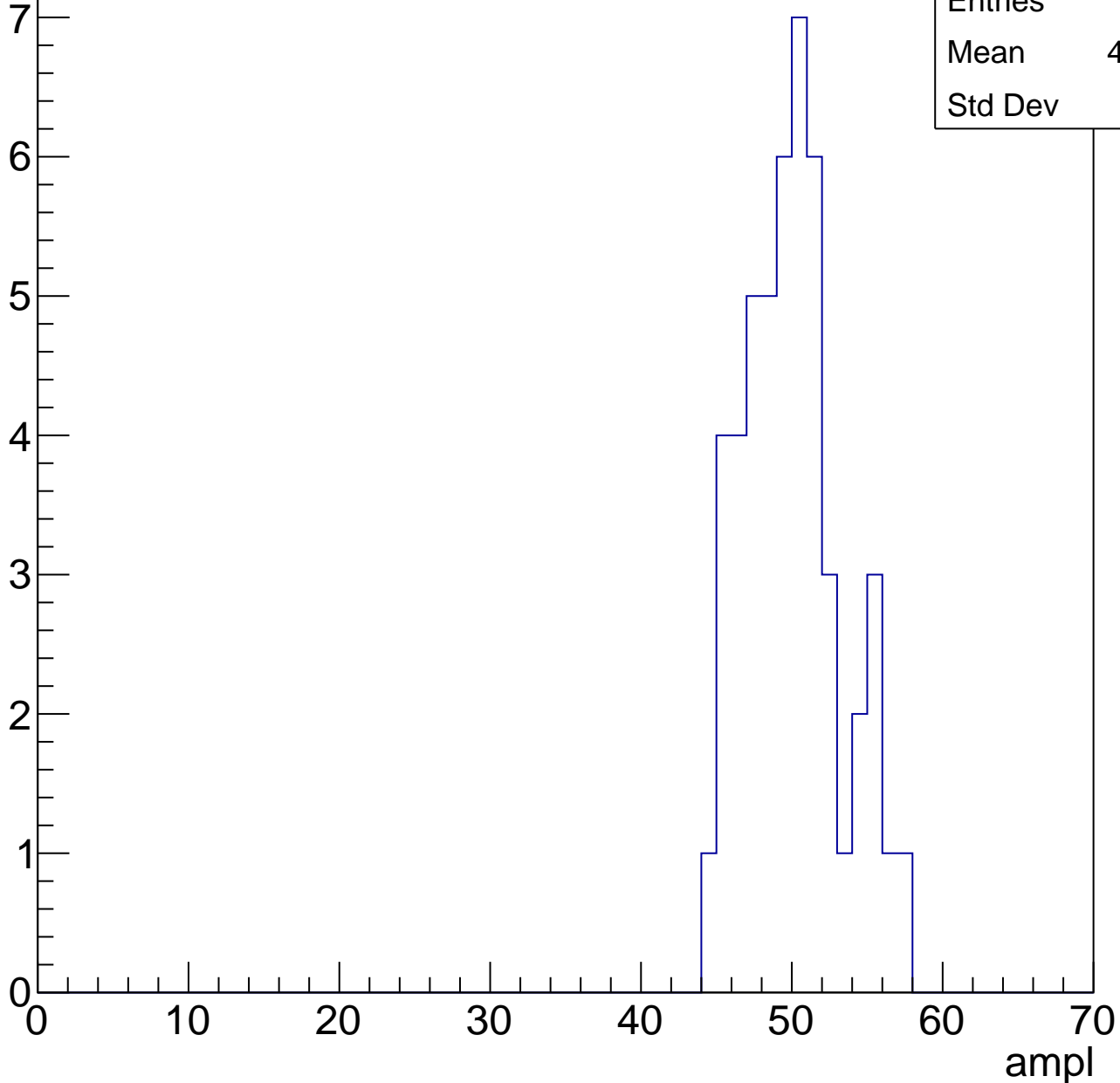


# B0L001S, U17-ch82, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

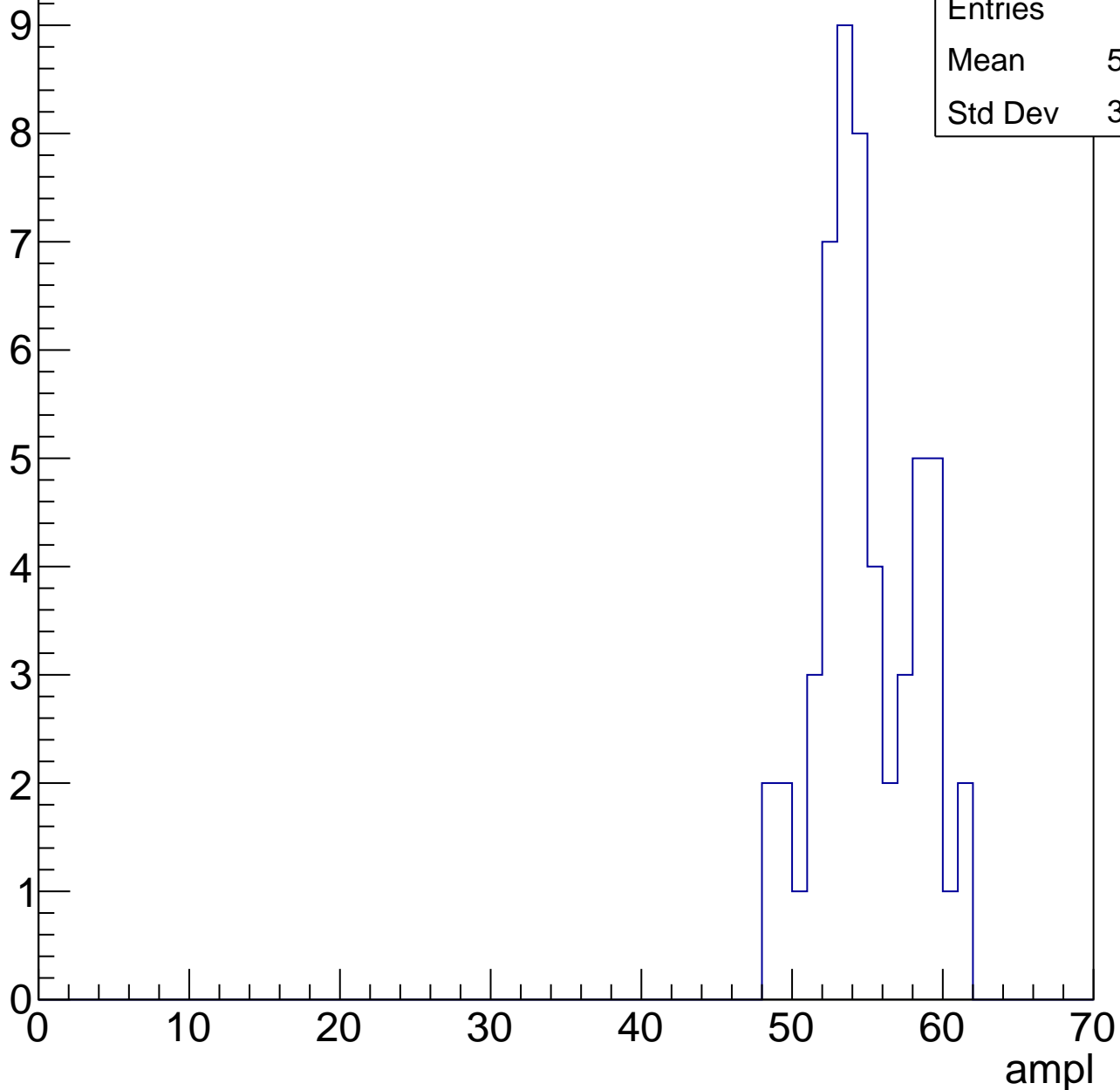
Entries	49
Mean	49.55
Std Dev	3.13



# B0L001S, U17-ch82, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



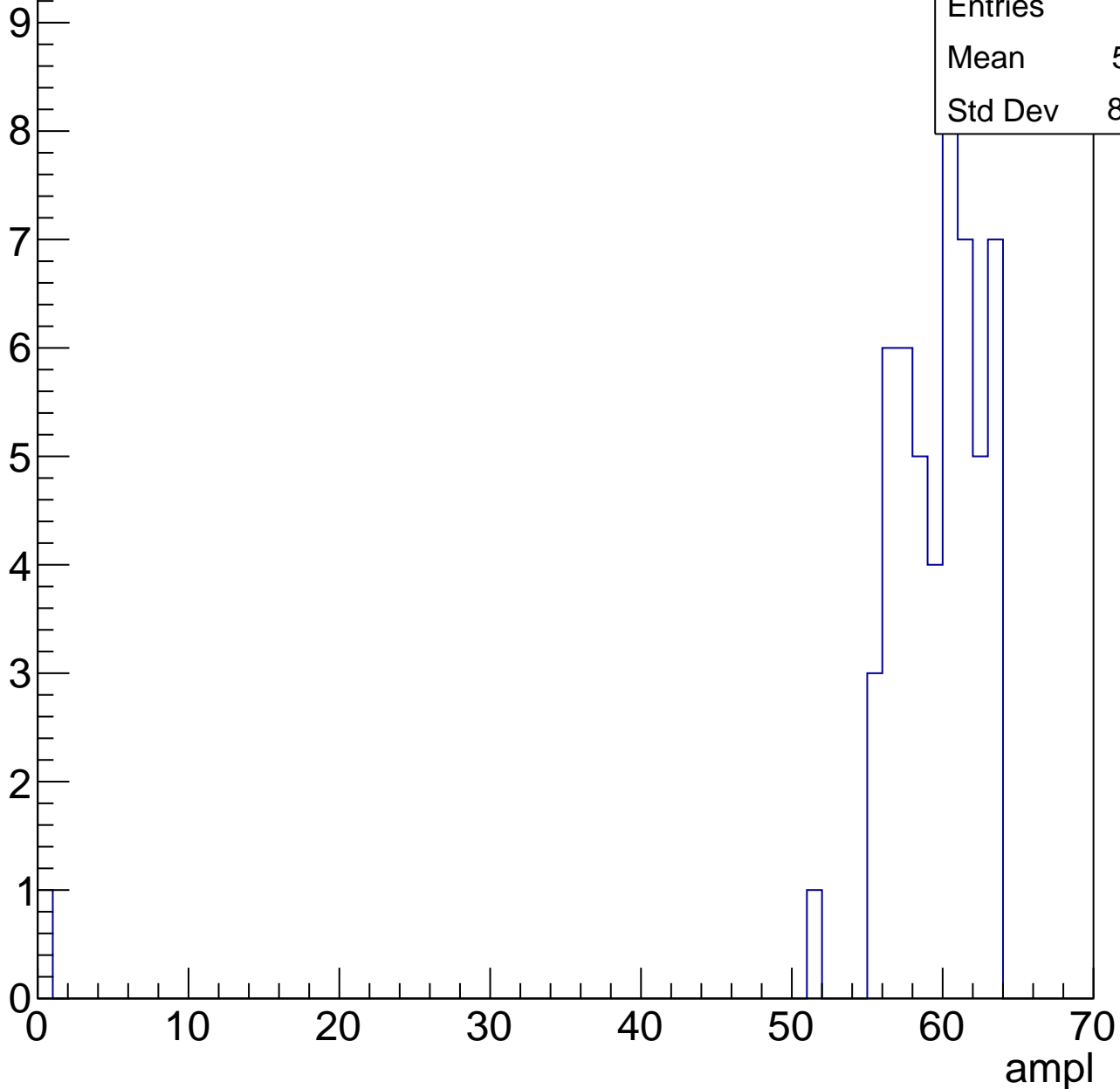
Entries	54
Mean	54.44
Std Dev	3.247

# B0L001S, U17-ch82, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

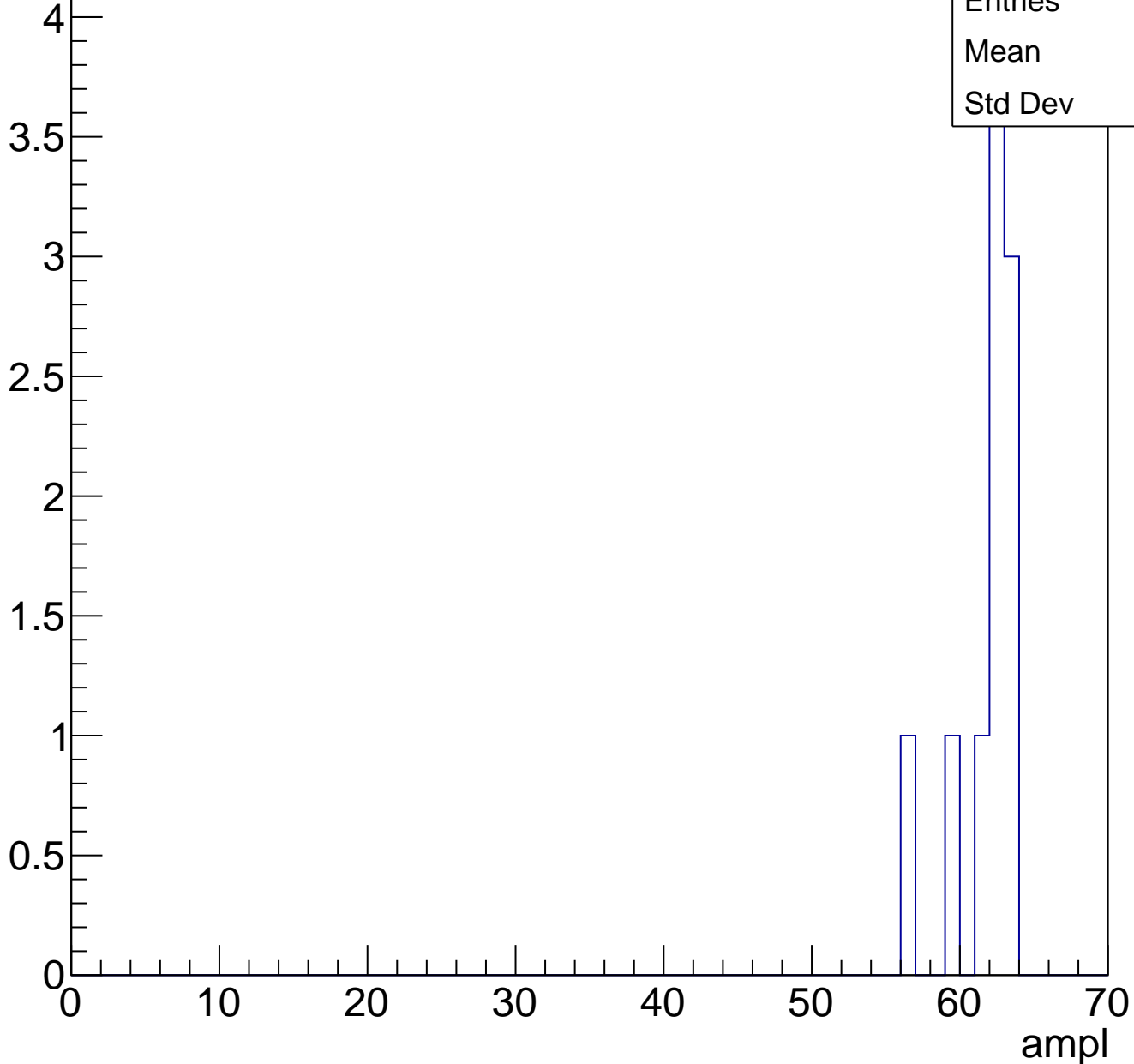
Entries	54
Mean	58.11
Std Dev	8.419



# B0L001S, U17-ch82, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	10
Mean	61.3
Std Dev	2.1



# B0L001S, U17-ch82, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	62
Std Dev	0

# B0L001S, U17-ch83, adc0

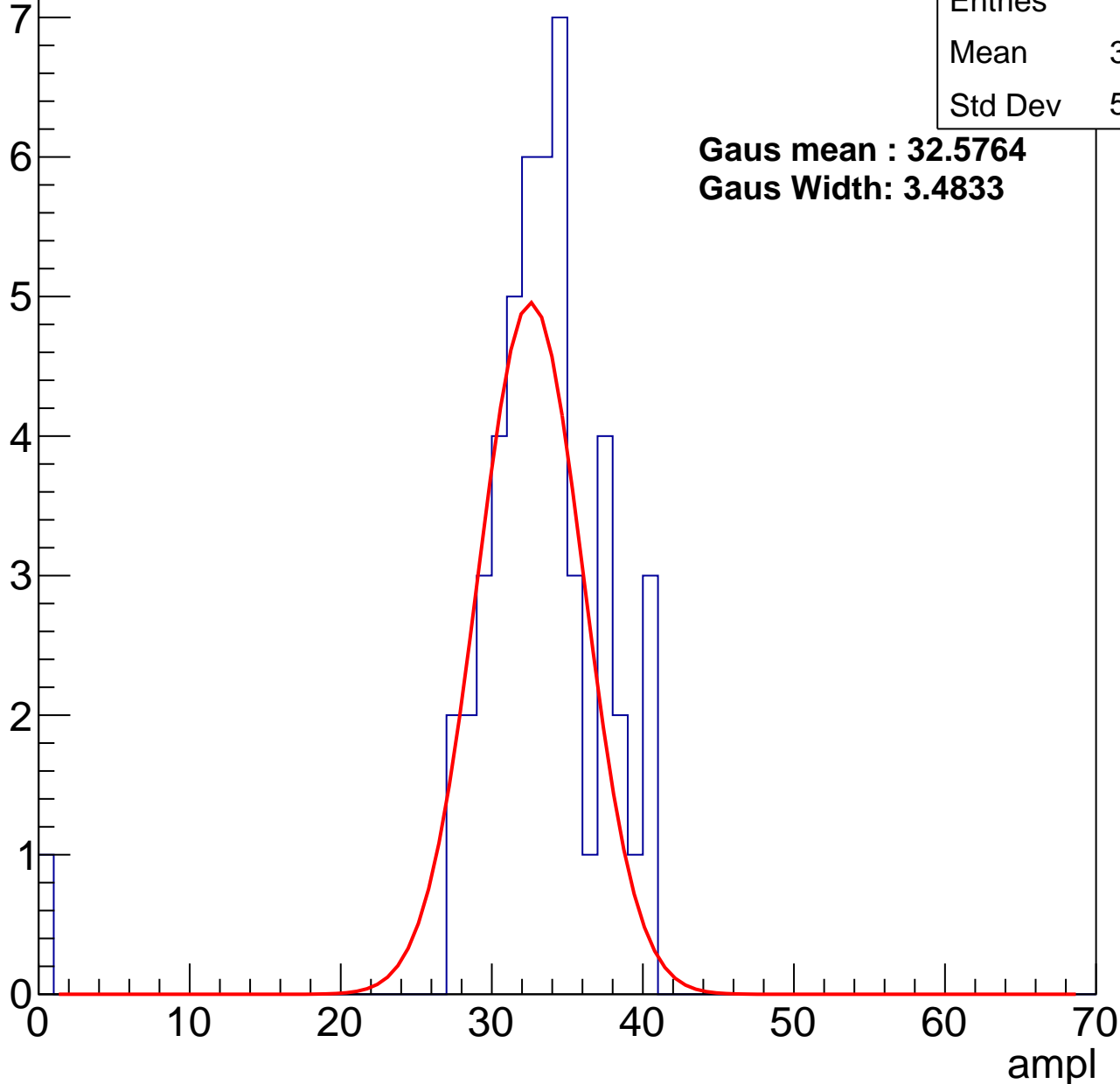
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	50
Mean	32.48
Std Dev	5.714

**Gaus mean : 32.5764**

**Gaus Width: 3.4833**



# B0L001S, U17-ch83, adc1

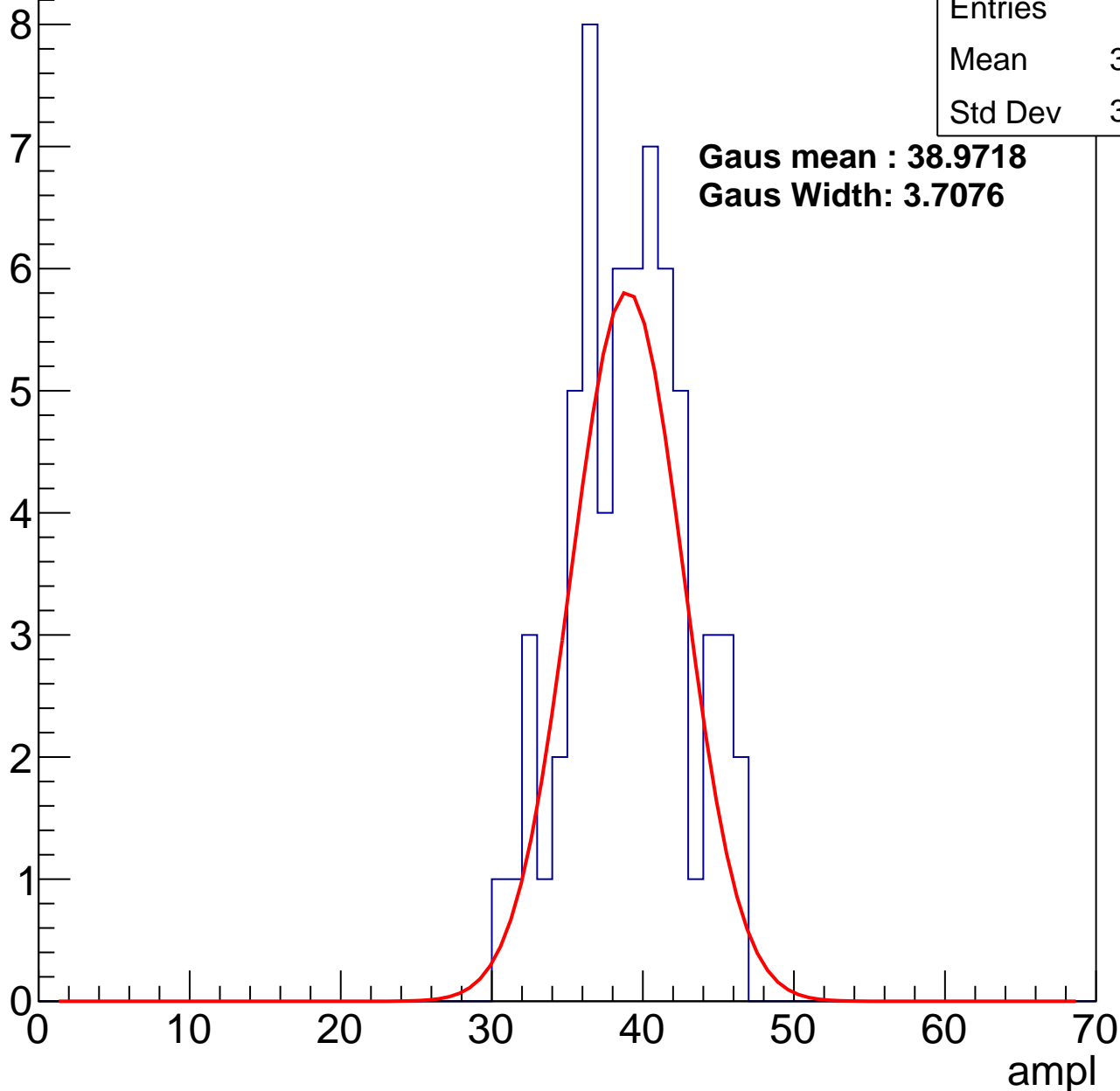
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	38.58
Std Dev	3.778

**Gaus mean : 38.9718**

**Gaus Width: 3.7076**



# B0L001S, U17-ch83, adc2

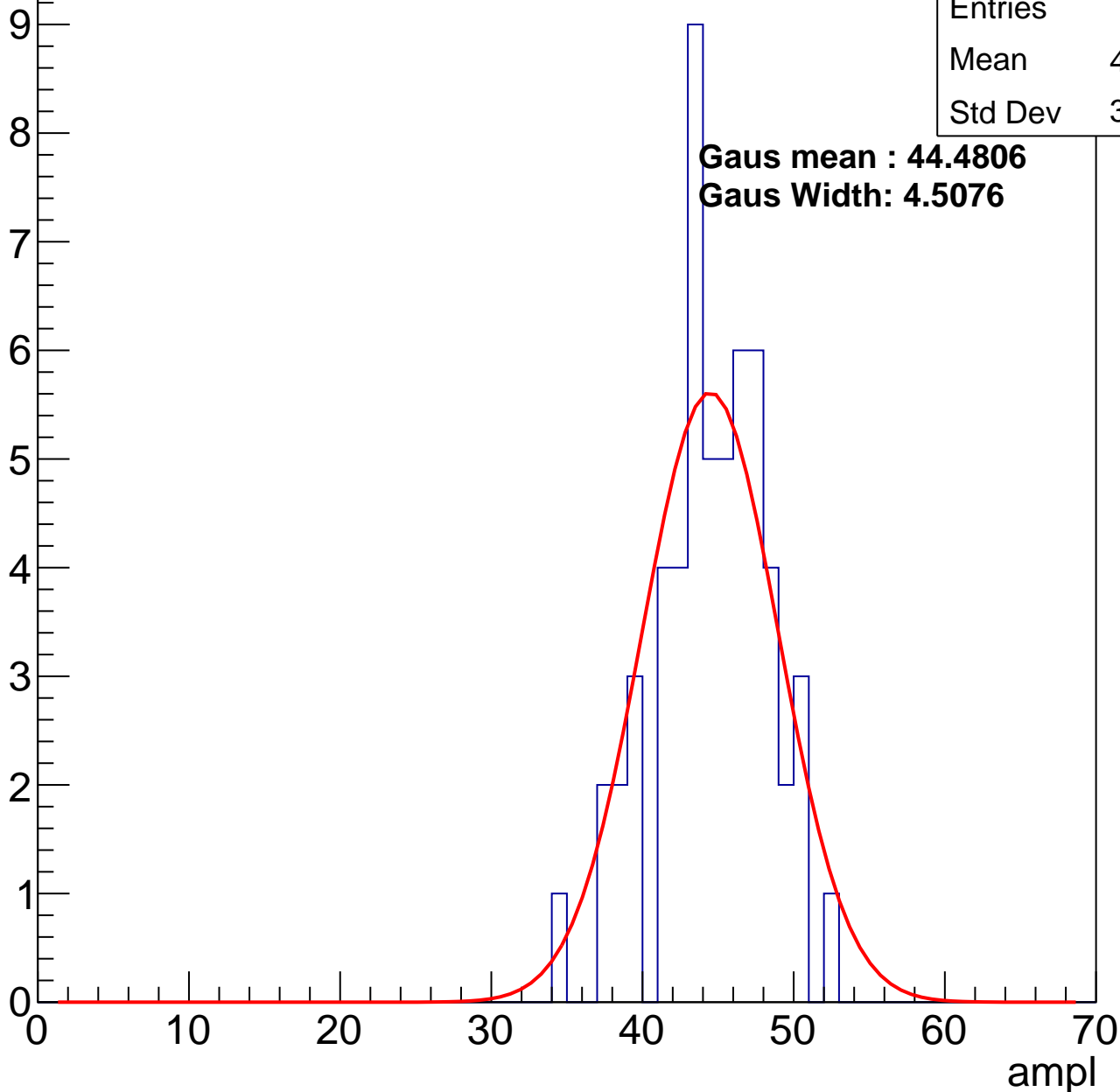
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	44.12
Std Dev	3.685

**Gaus mean : 44.4806**

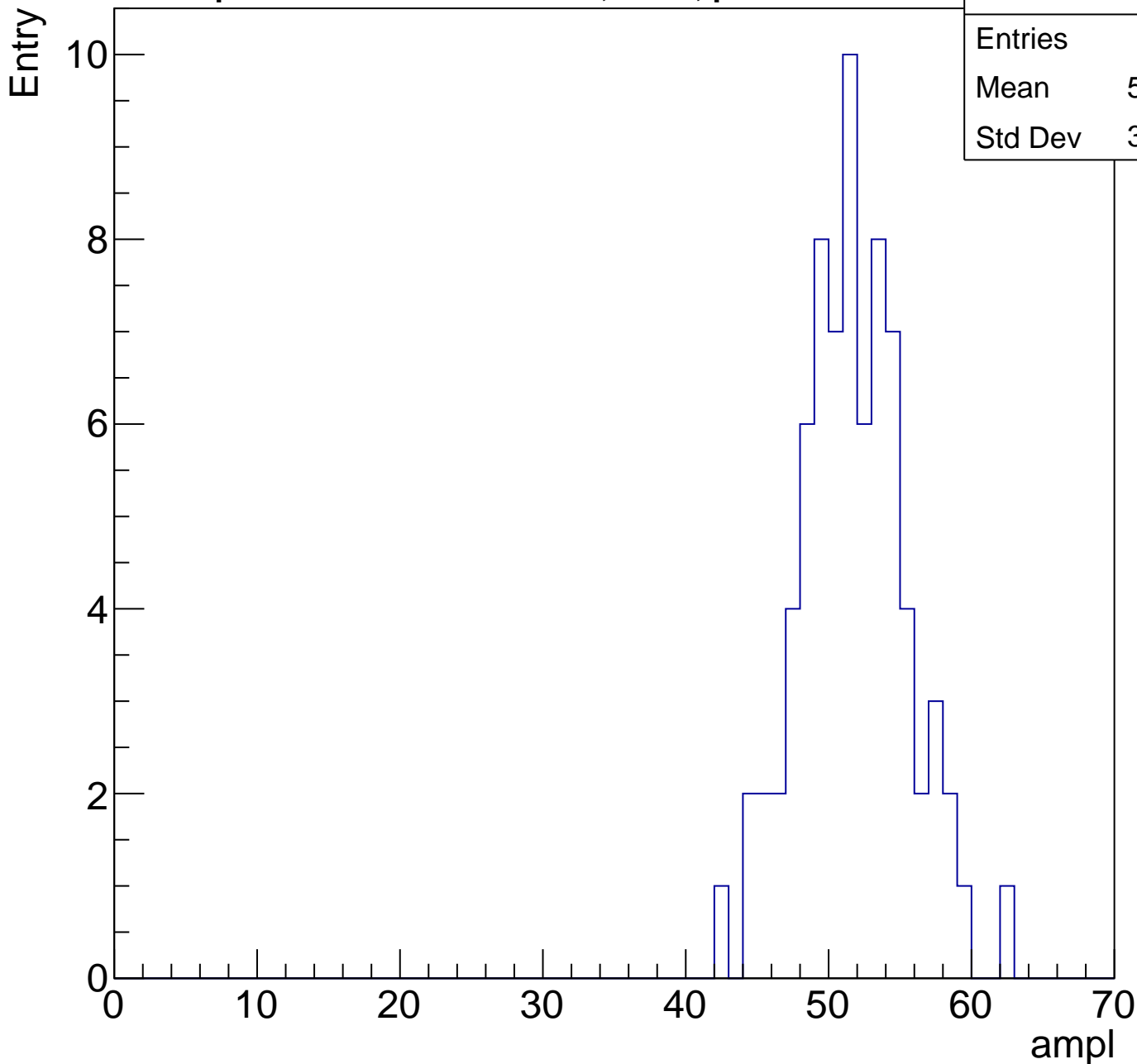
**Gaus Width: 4.5076**



# B0L001S, U17-ch83, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

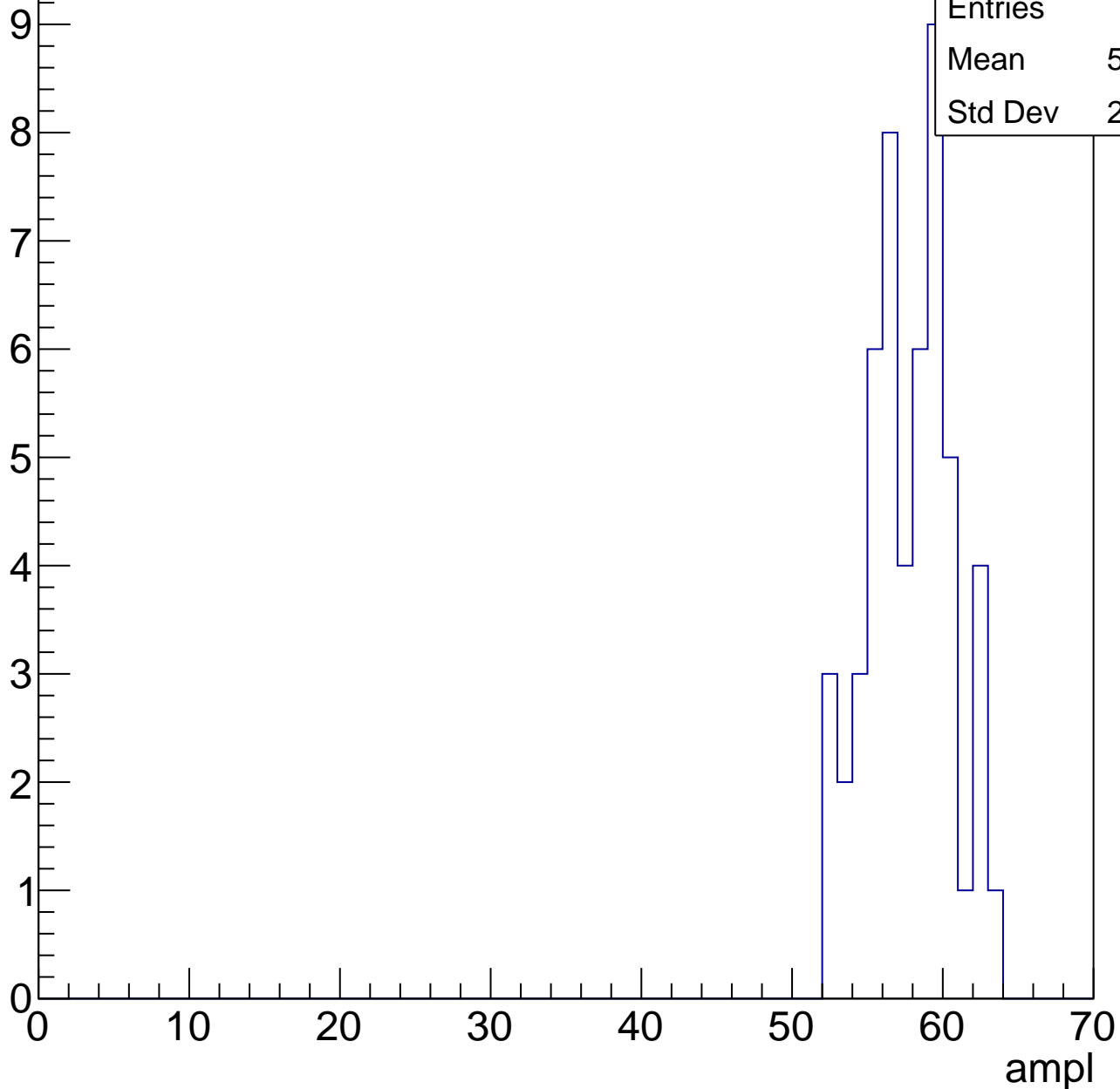
Entries	76
Mean	51.24
Std Dev	3.734



# B0L001S, U17-ch83, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



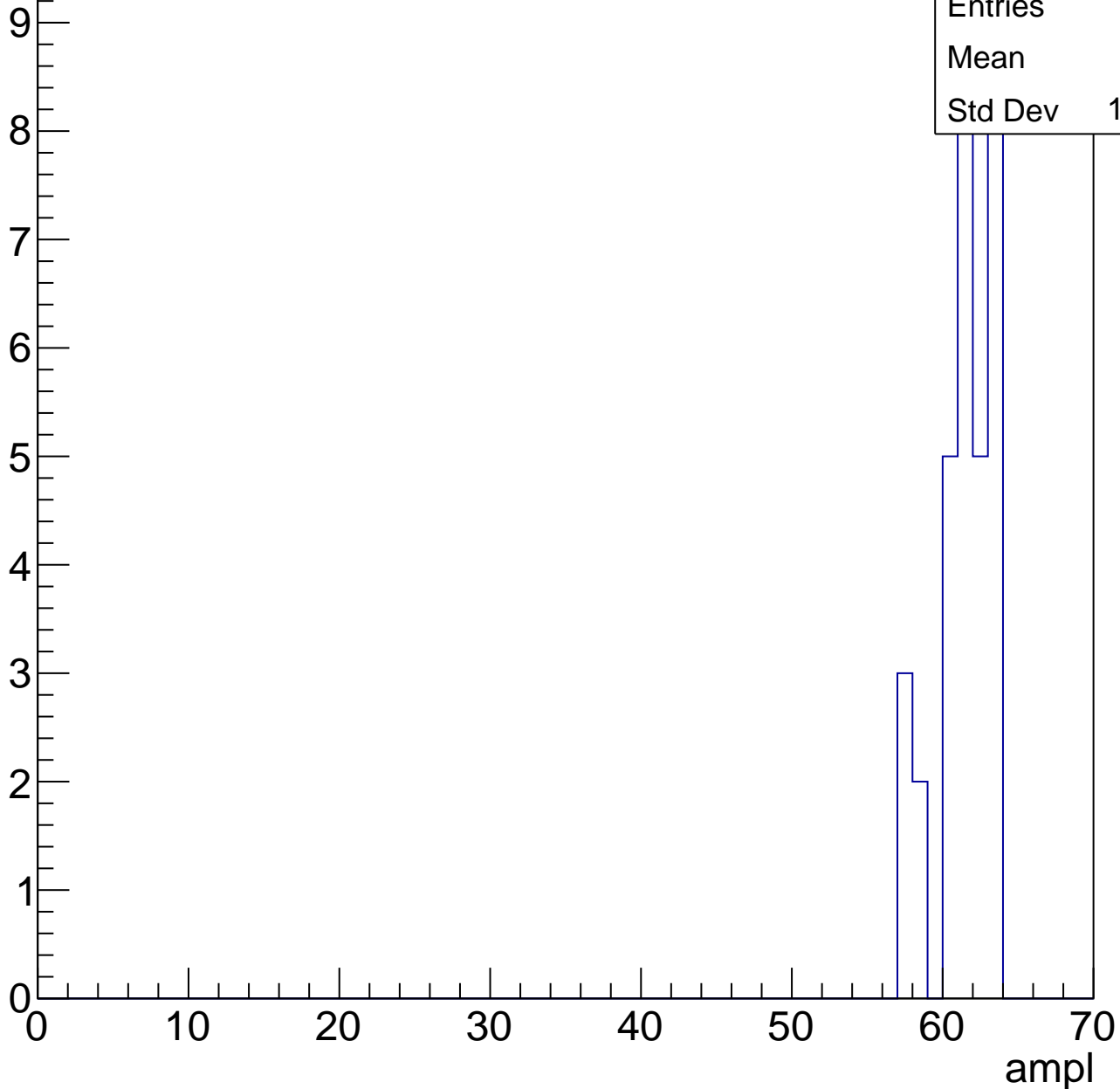
Entries	52
Mean	57.33
Std Dev	2.772

# B0L001S, U17-ch83, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	33
Mean	61
Std Dev	1.842



# B0L001S, U17-ch83, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0



# B0L001S, U17-ch83, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U17-ch84, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	69
Mean	31.61
Std Dev	5.063

**Gaus mean : 32.4290**

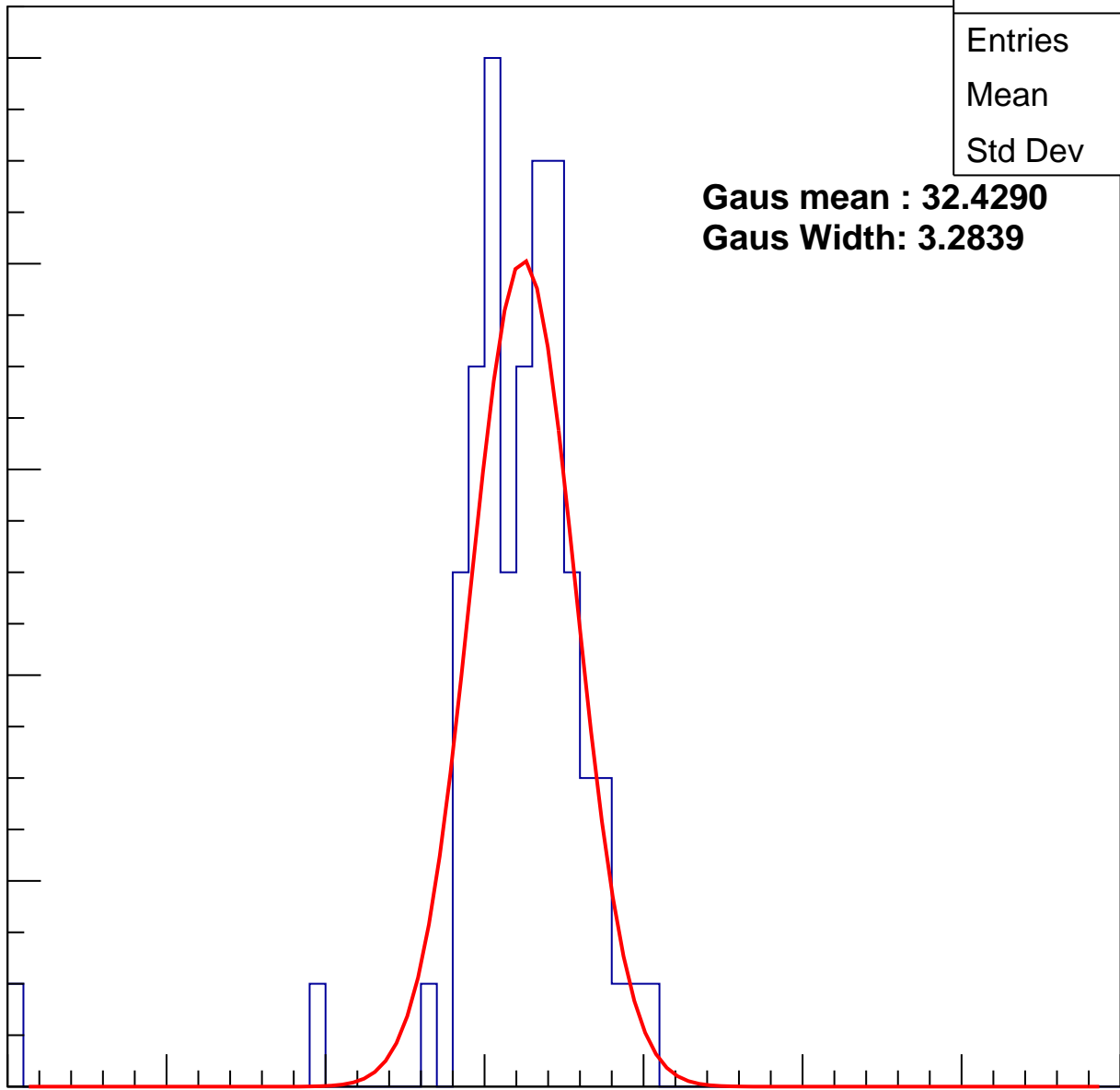
**Gaus Width: 3.2839**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



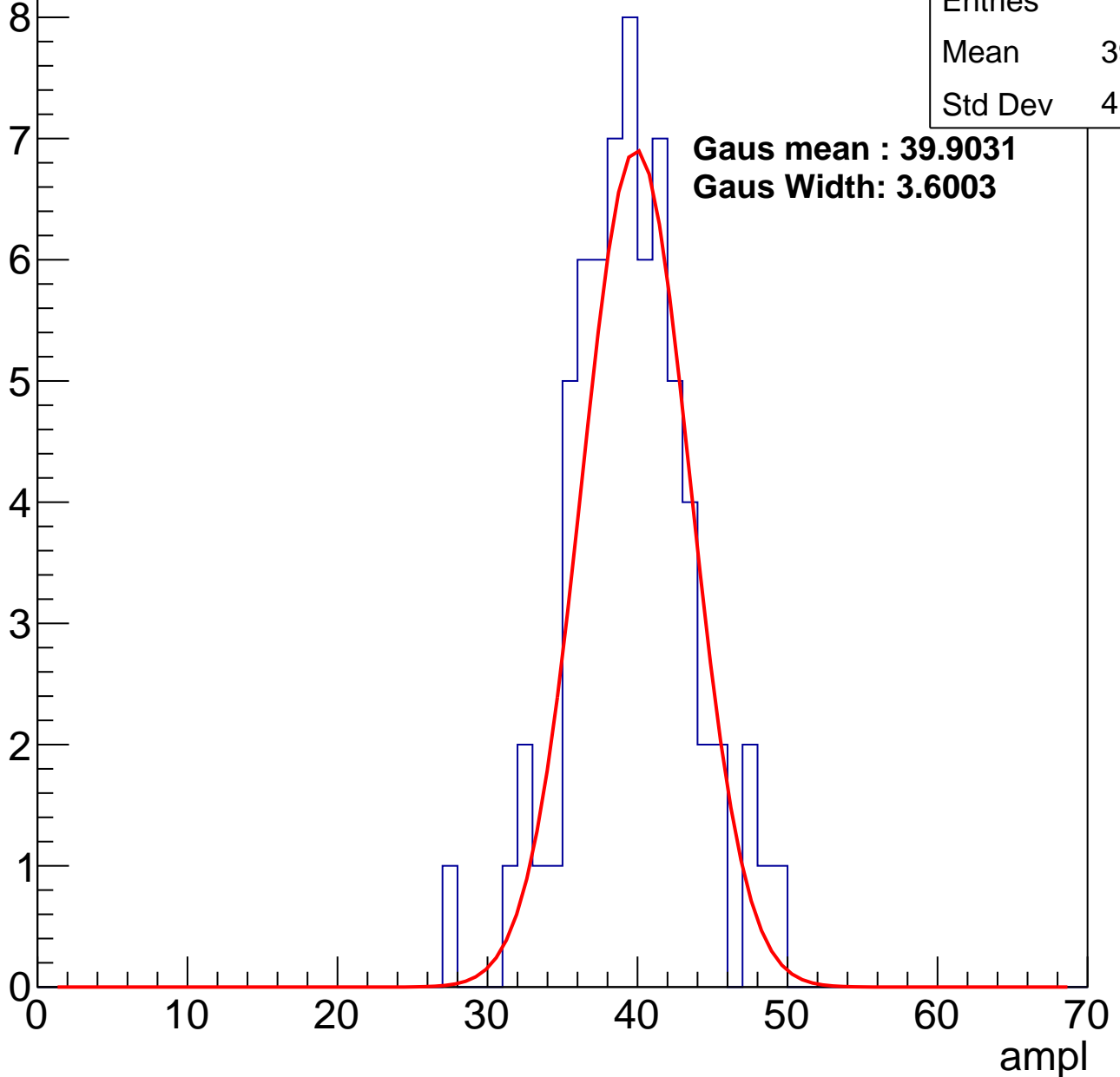
# B0L001S, U17-ch84, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	39.09
Std Dev	4.032

**Gaus mean : 39.9031**  
**Gaus Width: 3.6003**



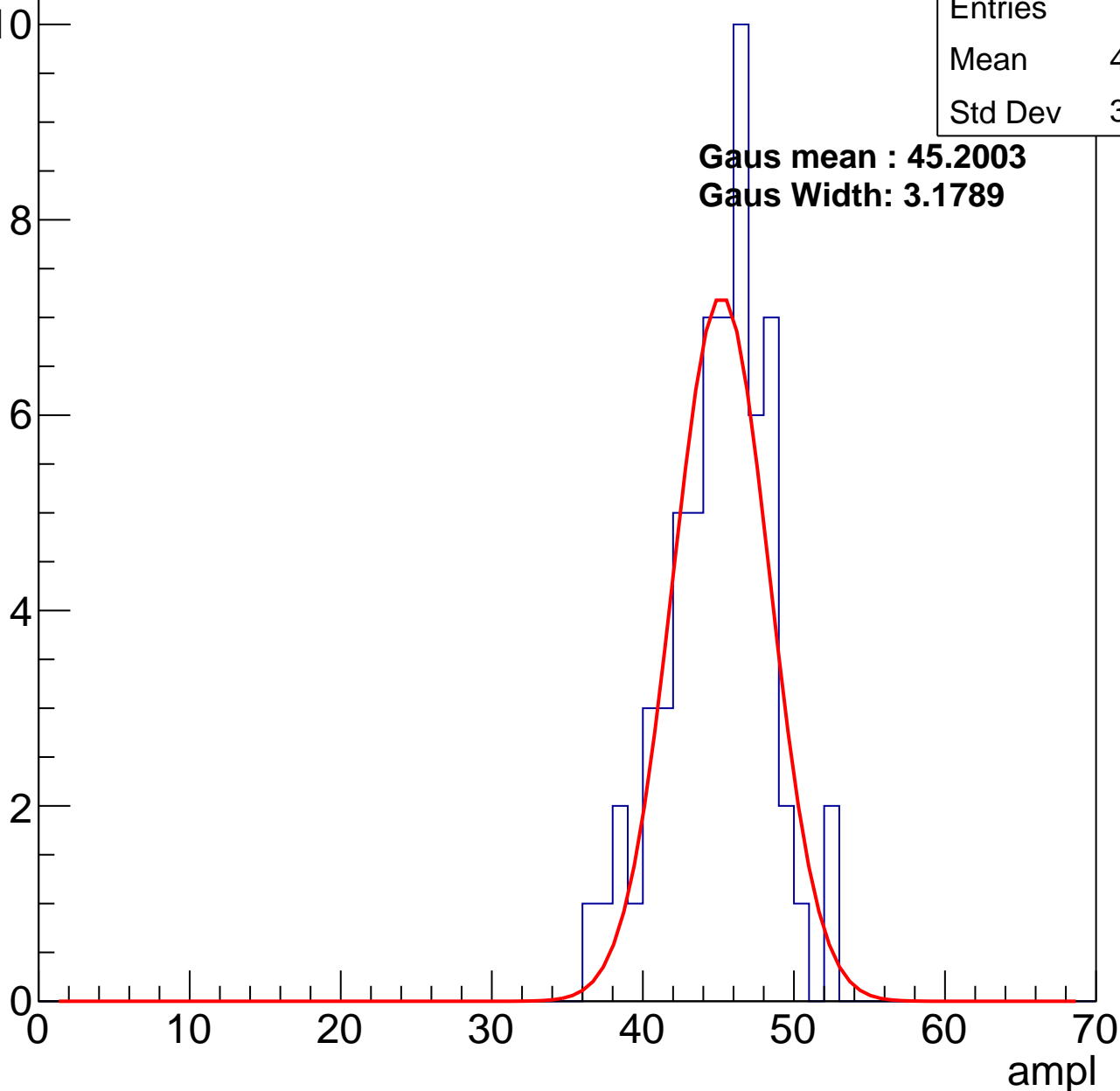
# B0L001S, U17-ch84, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	63
Mean	44.59
Std Dev	3.369

**Gaus mean : 45.2003**  
**Gaus Width: 3.1789**

Entry

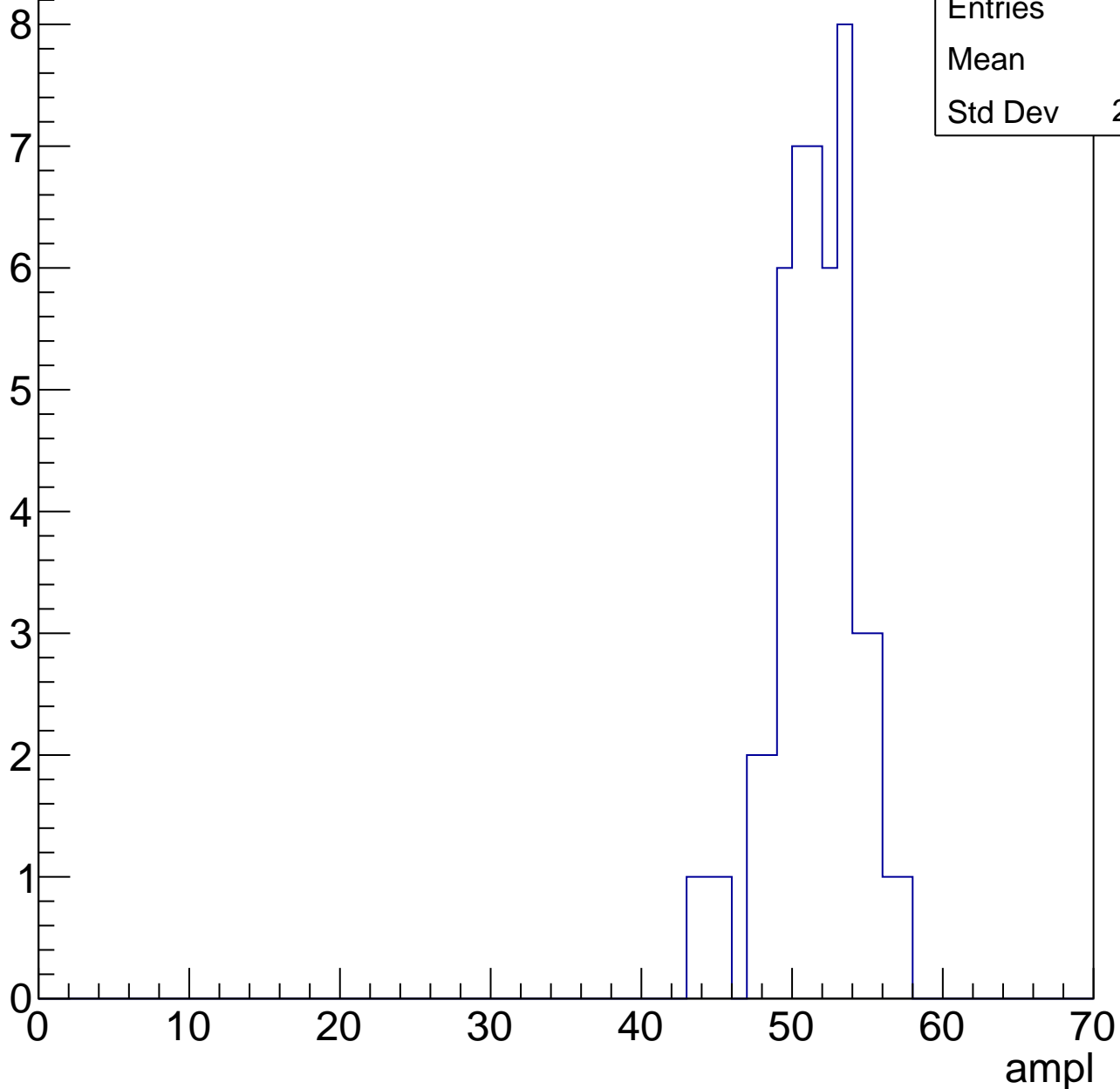


# B0L001S, U17-ch84, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	49
Mean	51
Std Dev	2.871

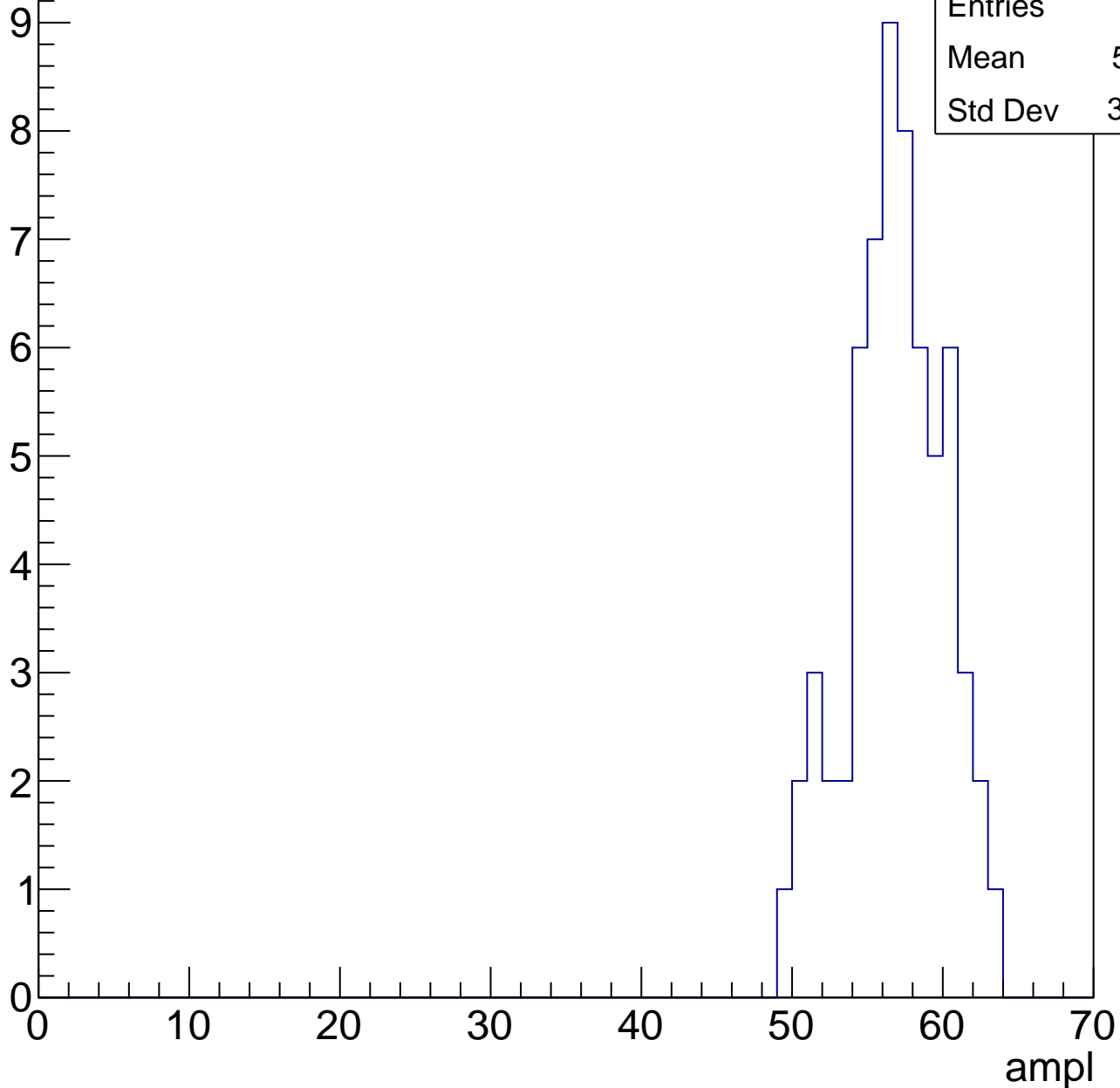


# B0L001S, U17-ch84, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	56.41
Std Dev	3.175

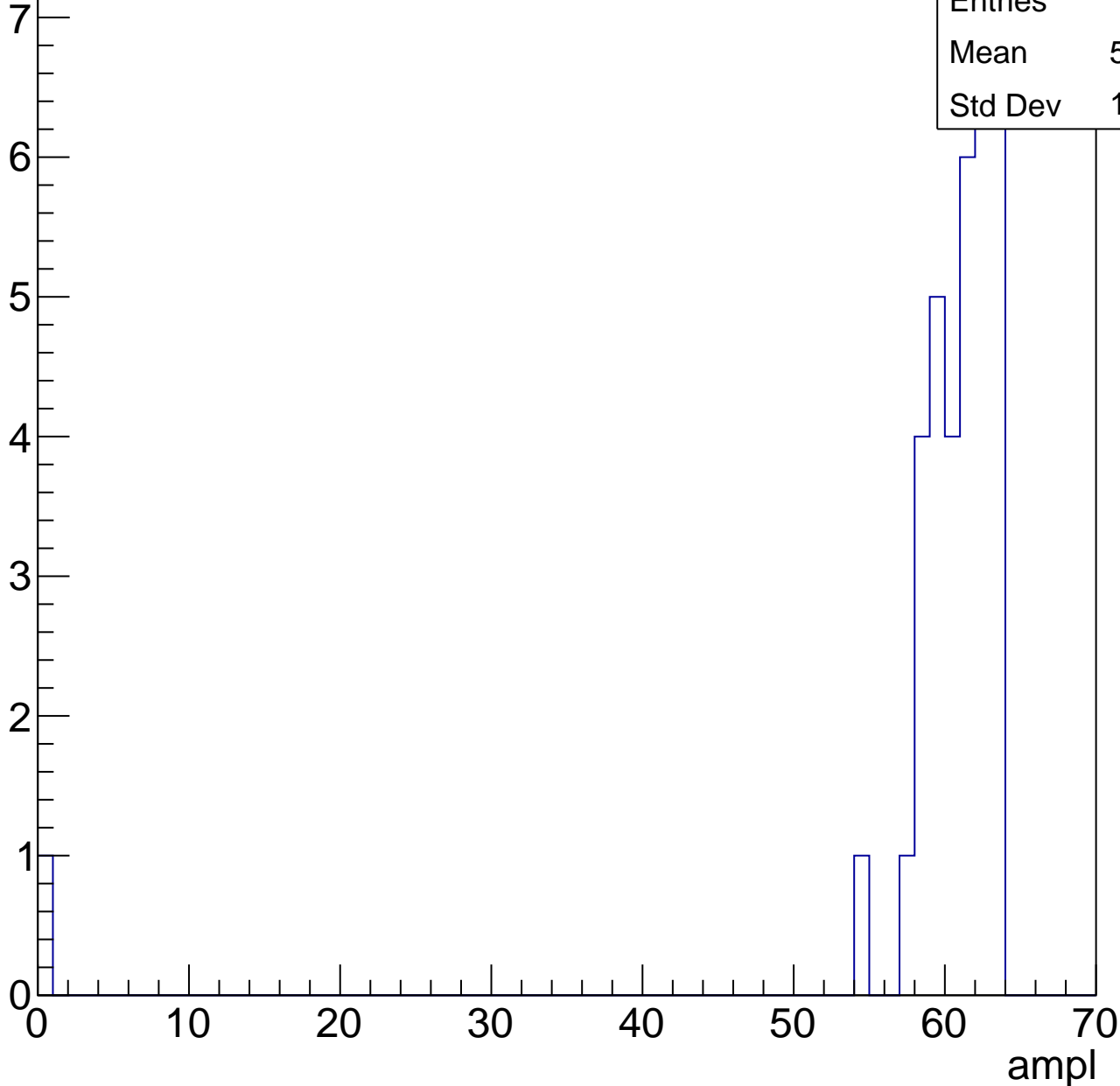


# B0L001S, U17-ch84, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	36
Mean	58.86
Std Dev	10.16



# B0L001S, U17-ch84, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch84, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U17-ch85, adc0

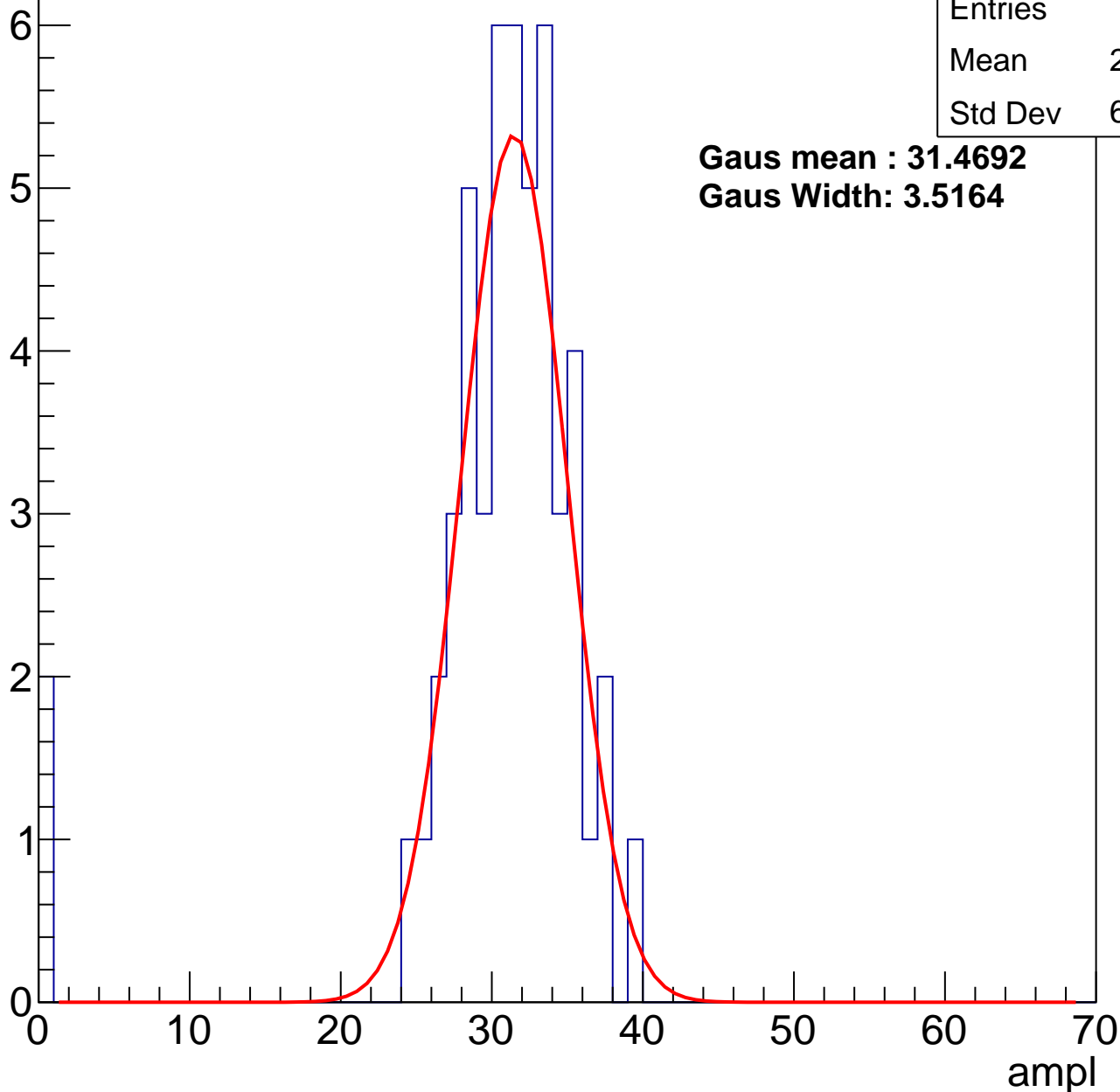
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	51
Mean	29.88
Std Dev	6.839

**Gaus mean : 31.4692**

**Gaus Width: 3.5164**



# B0L001S, U17-ch85, adc1

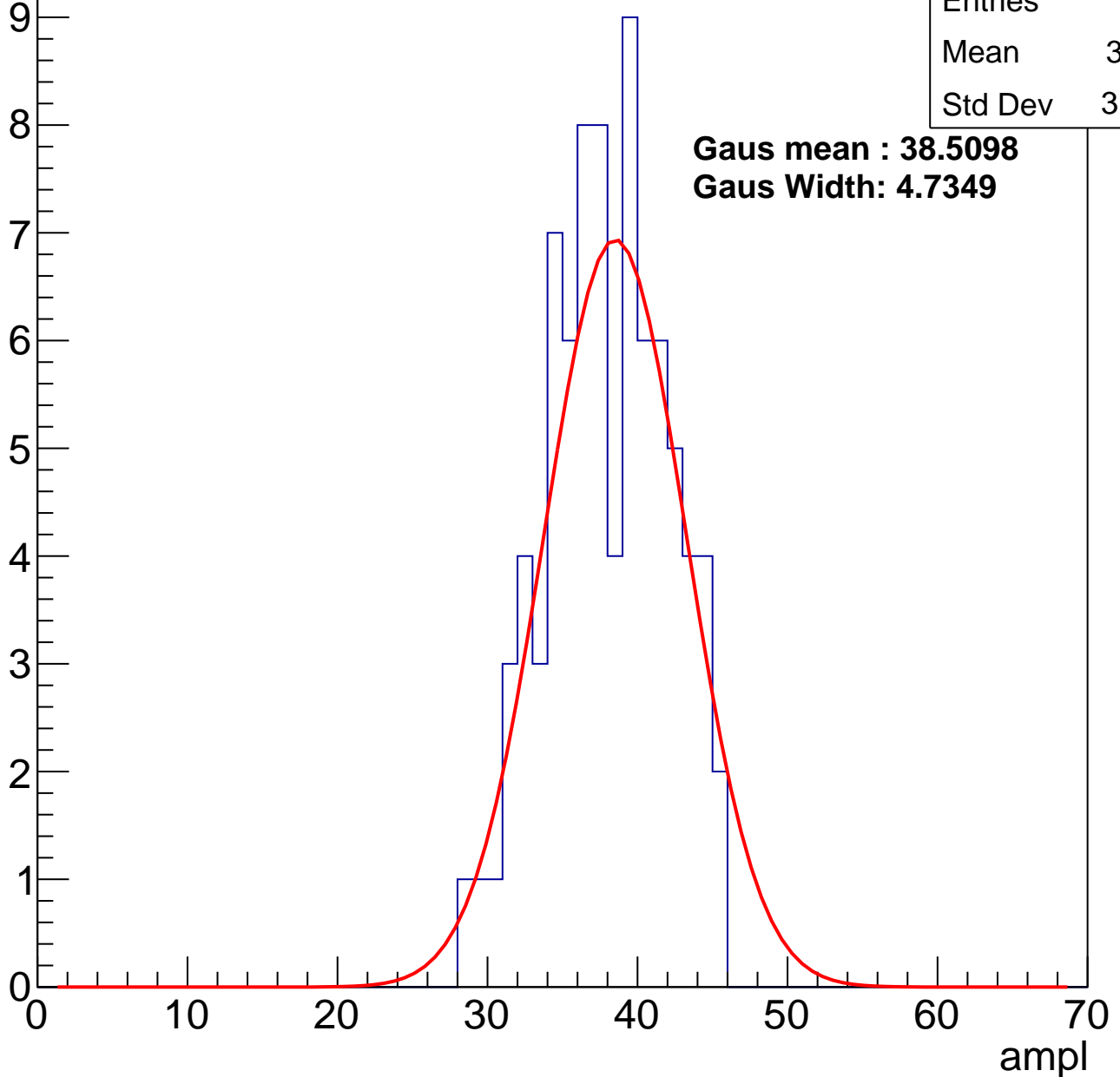
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	82
Mean	37.51
Std Dev	3.992

**Gaus mean : 38.5098**

**Gaus Width: 4.7349**



# B0L001S, U17-ch85, adc2

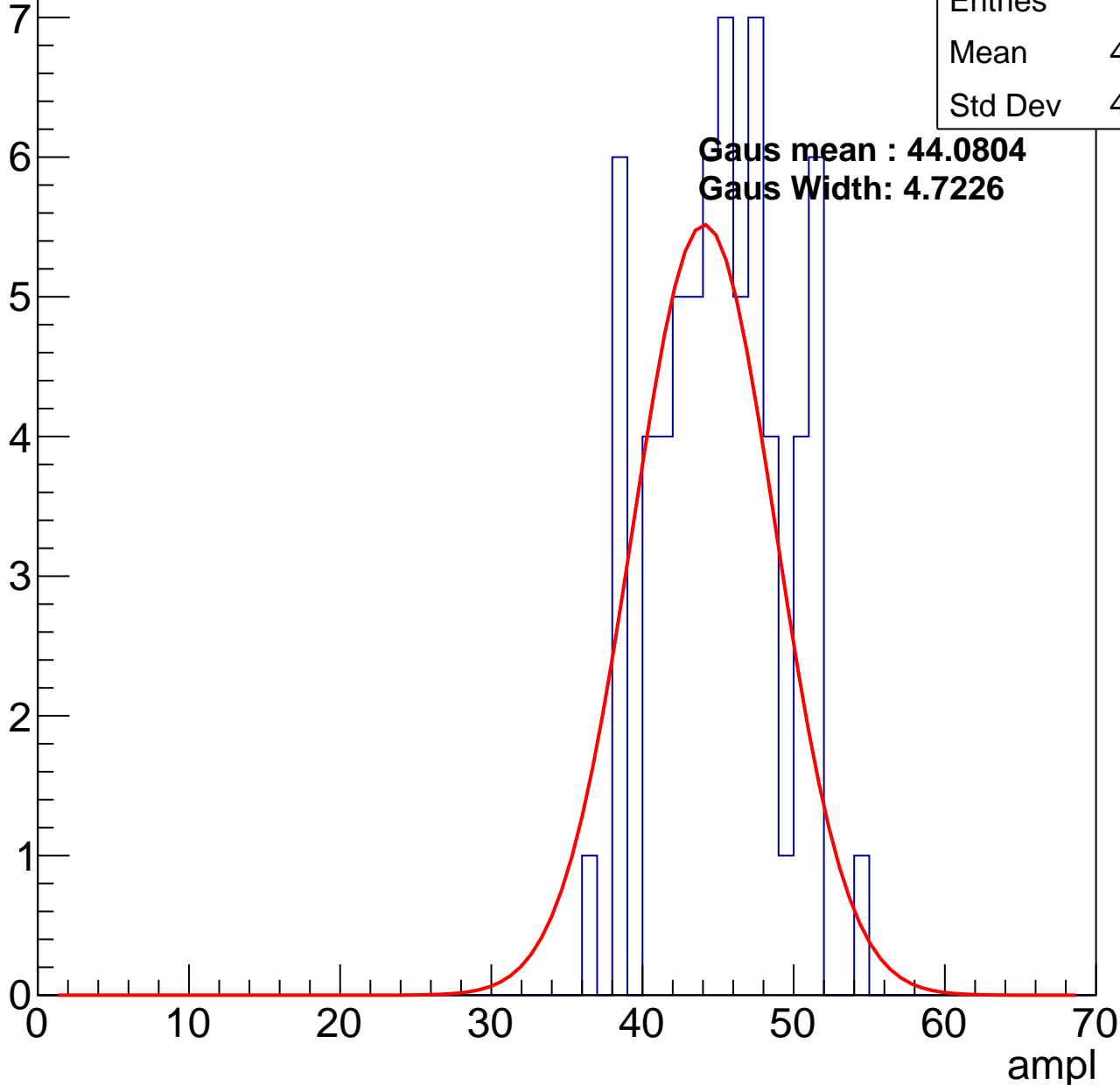
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	44.73
Std Dev	4.058

**Gaus mean : 44.0804**

**Gaus Width: 4.7226**

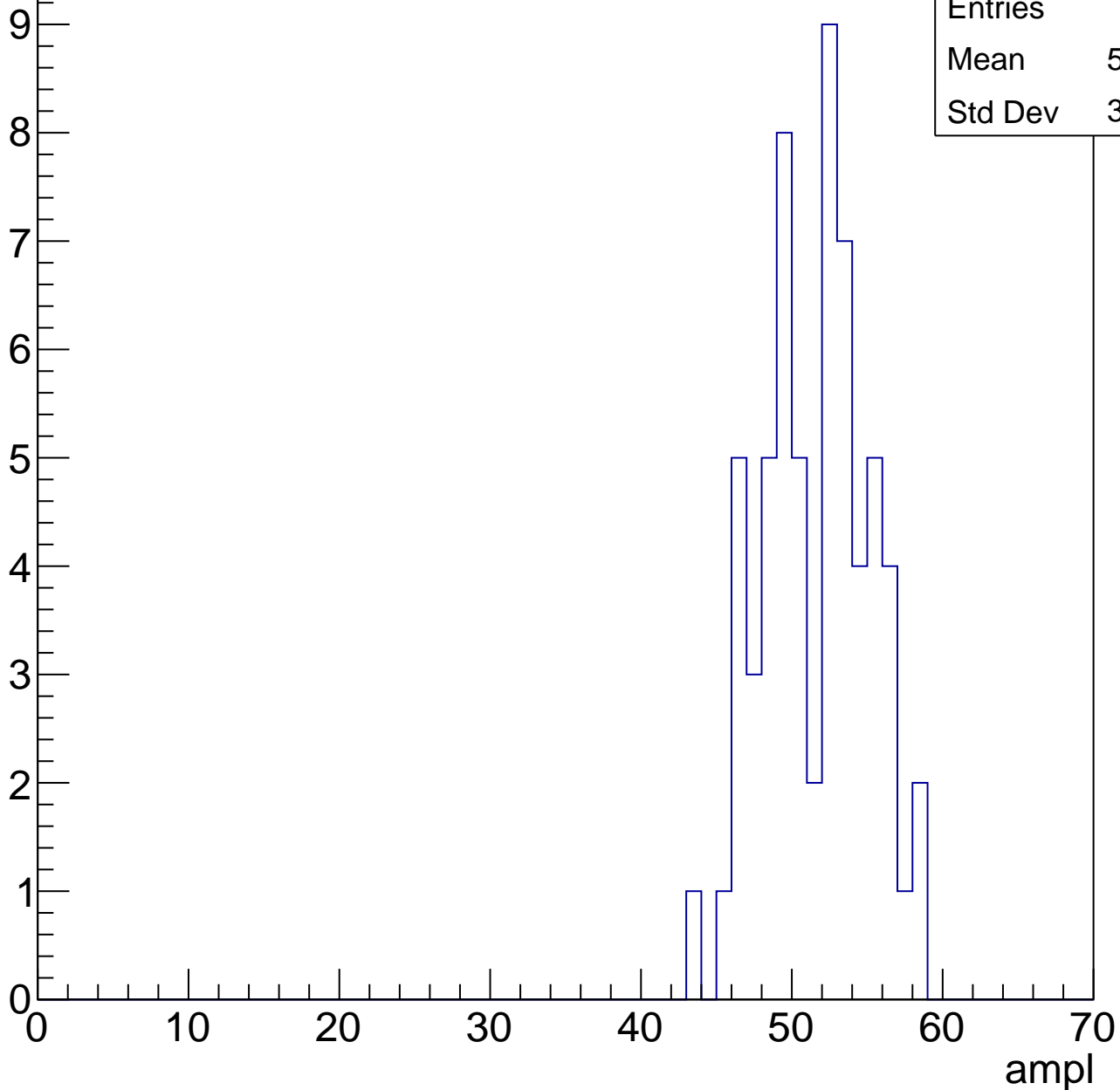


# B0L001S, U17-ch85, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	51.13
Std Dev	3.457

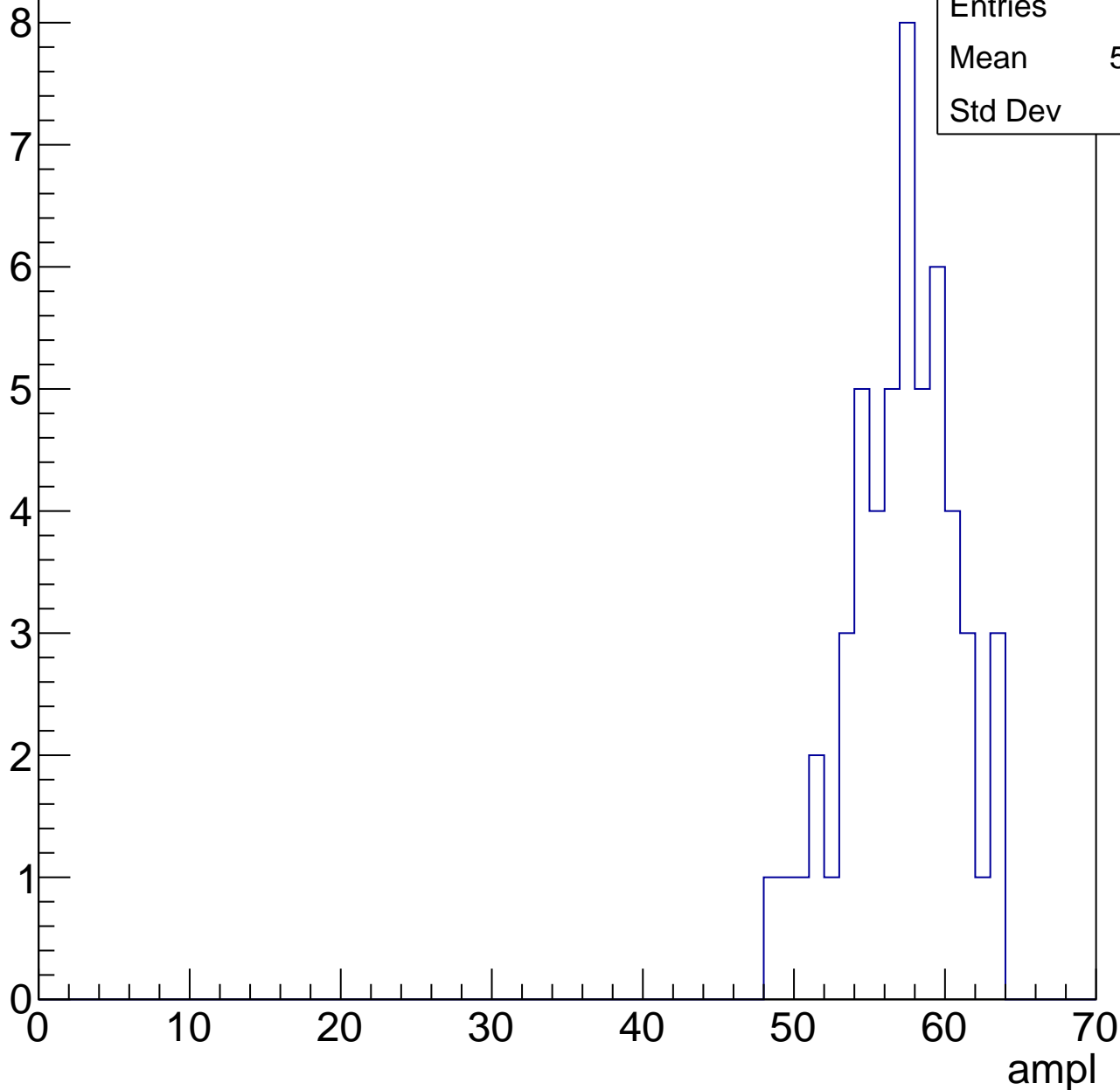


# B0L001S, U17-ch85, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	56.68
Std Dev	3.49

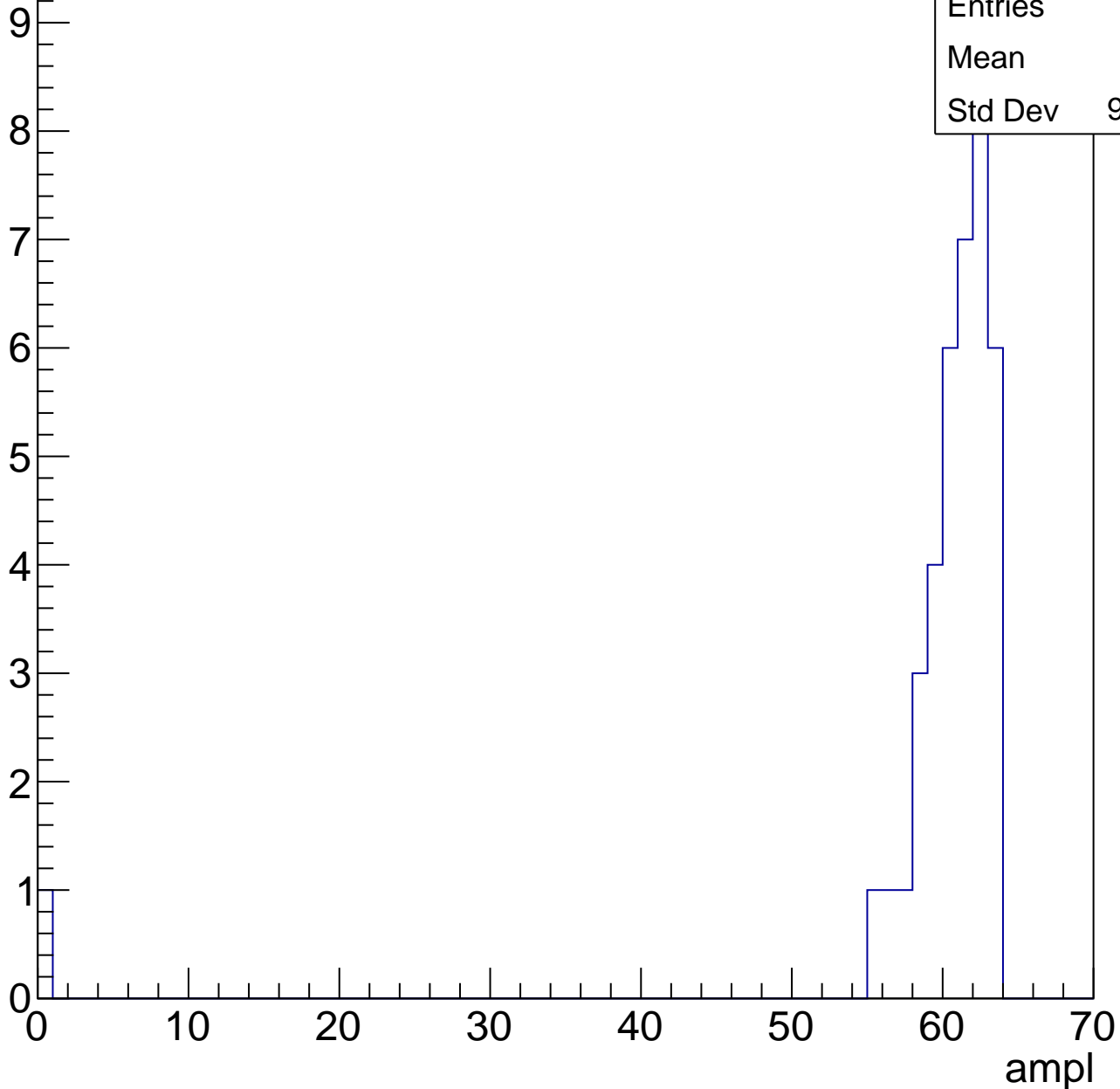


# B0L001S, U17-ch85, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	39
Mean	59
Std Dev	9.772



# B0L001S, U17-ch85, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch85, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U17-ch86, adc0

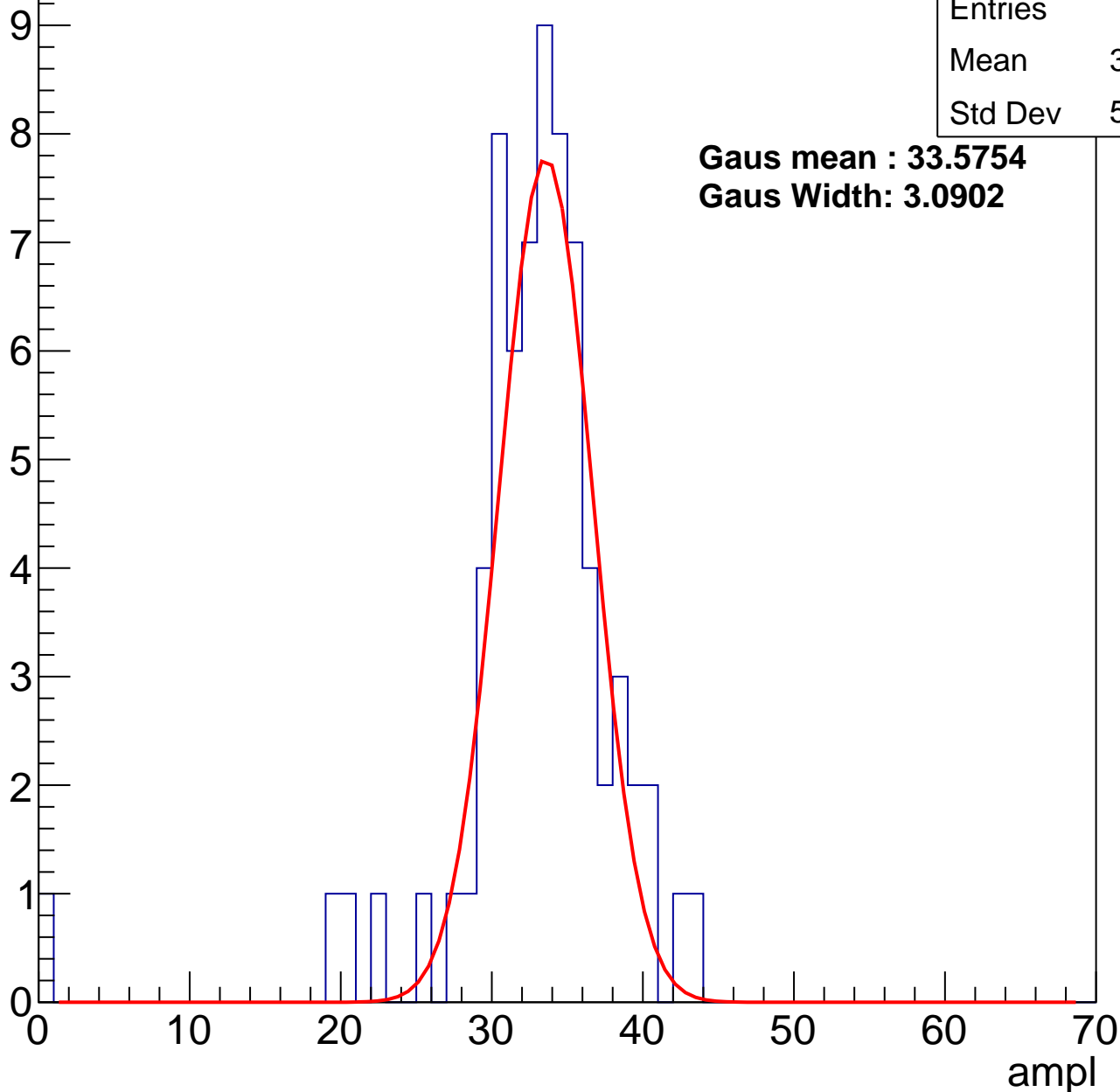
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	32.34
Std Dev	5.773

**Gaus mean : 33.5754**

**Gaus Width: 3.0902**



# B0L001S, U17-ch86, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	39.55
Std Dev	3.388

7

6

5

4

3

2

1

0

**Gaus mean : 40.2370**

**Gaus Width: 3.6772**

ampl

0

10

20

30

40

50

60

70

0

# B0L001S, U17-ch86, adc2

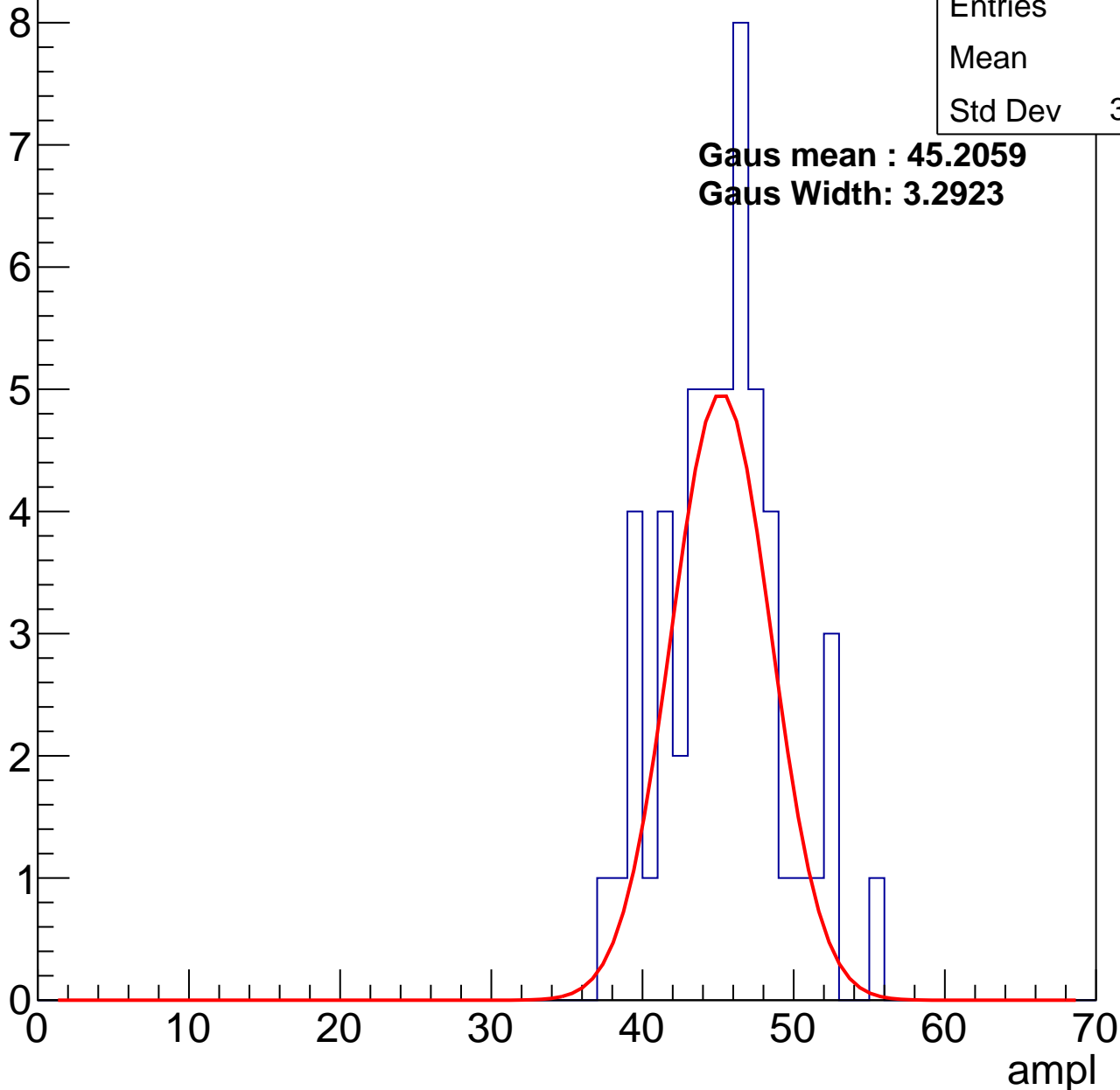
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	44.9
Std Dev	3.864

**Gaus mean : 45.2059**

**Gaus Width: 3.2923**

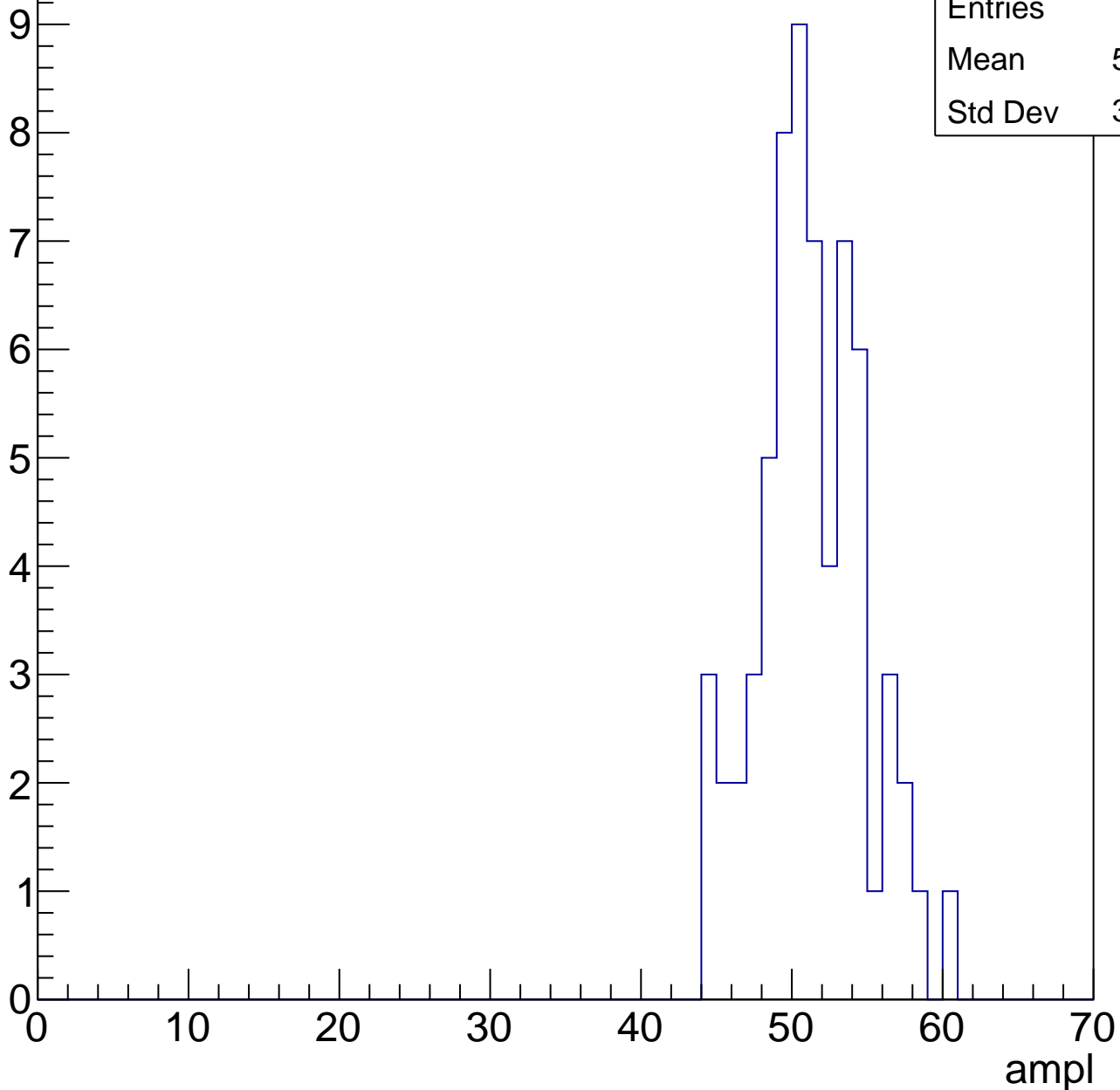


# B0L001S, U17-ch86, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	50.81
Std Dev	3.491

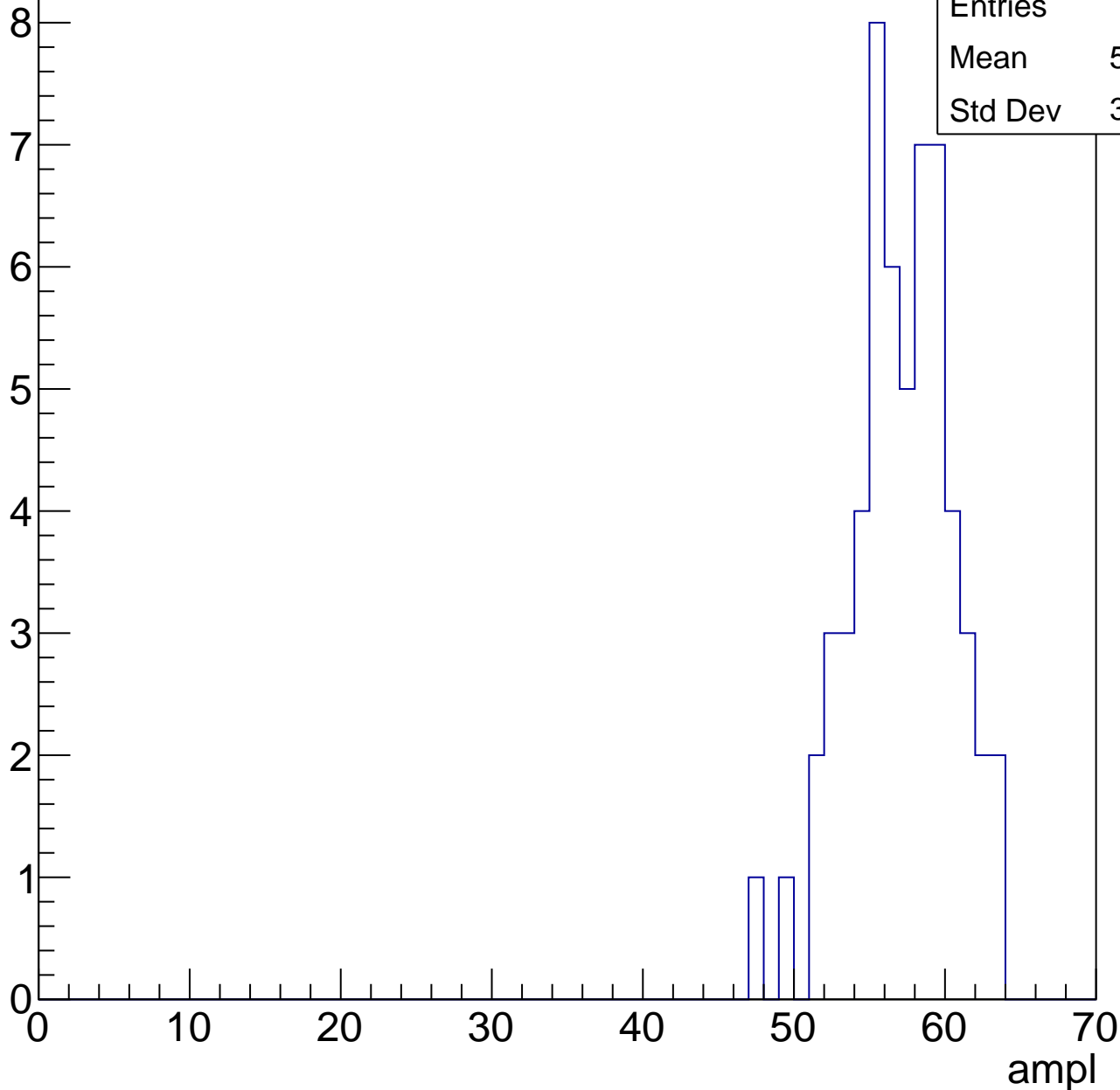


# B0L001S, U17-ch86, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	56.59
Std Dev	3.384

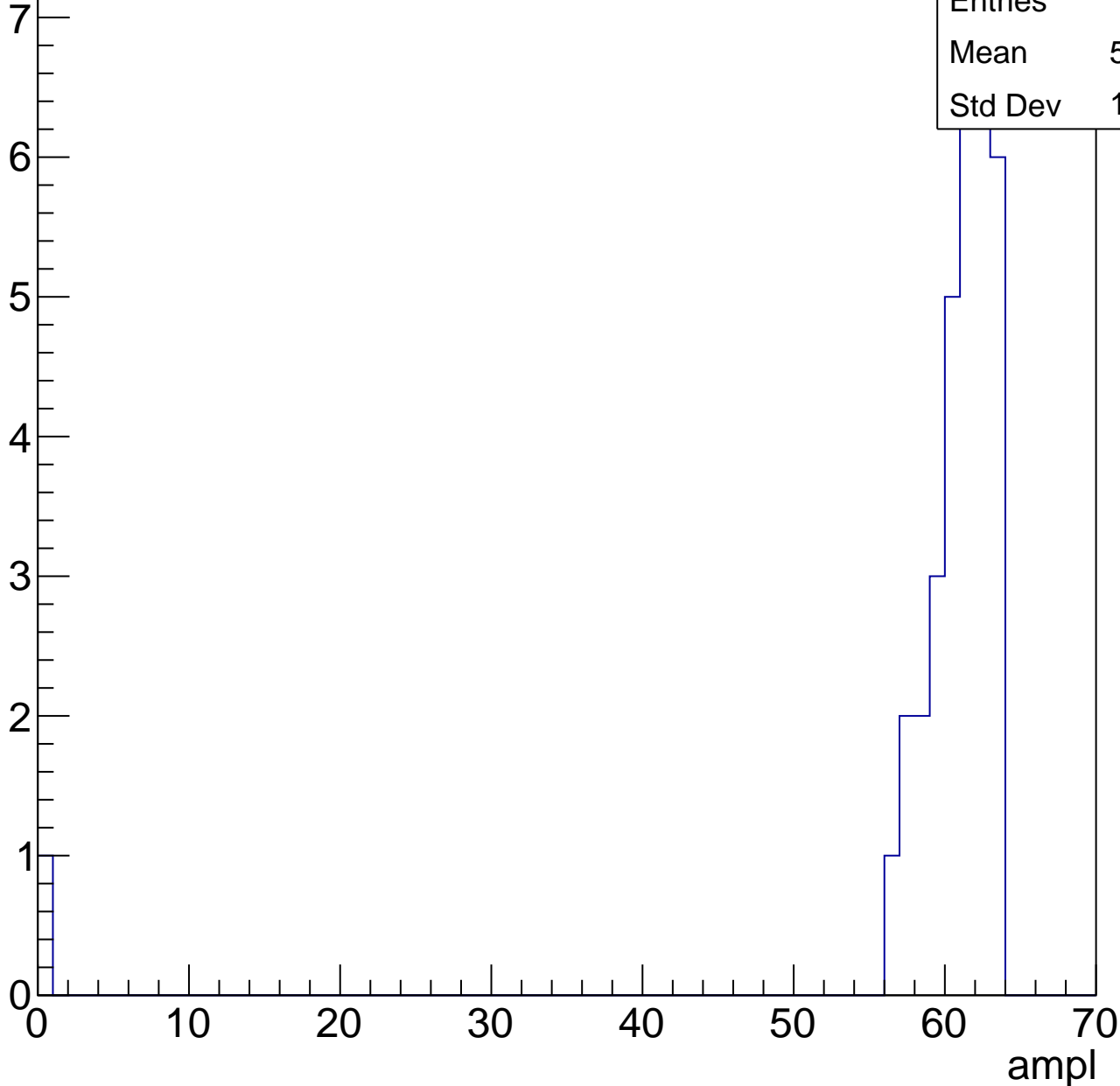


# B0L001S, U17-ch86, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

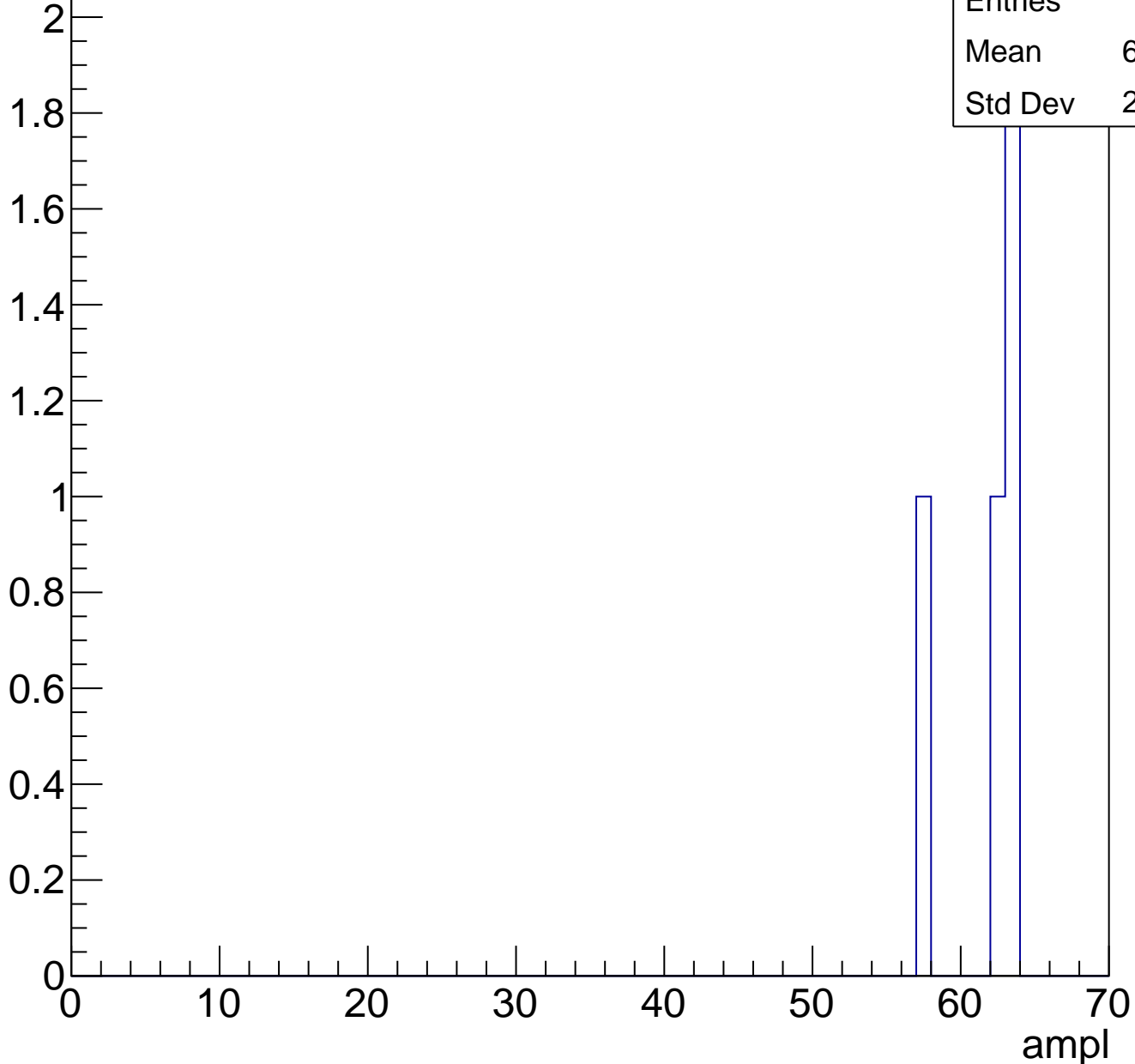
Entries	34
Mean	58.88
Std Dev	10.42



# B0L001S, U17-ch86, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch86, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U17-ch87, adc0

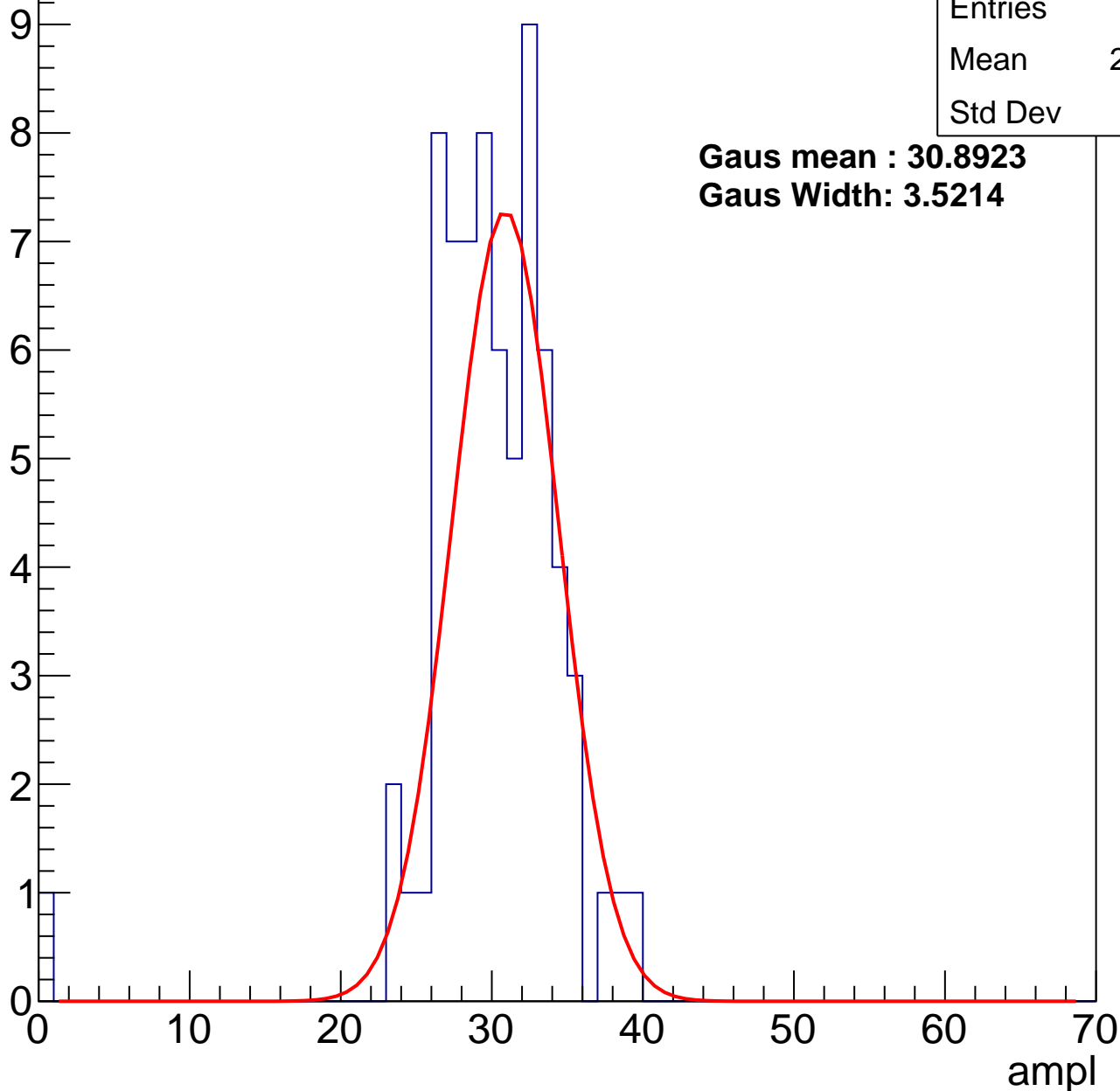
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	29.52
Std Dev	4.89

**Gaus mean : 30.8923**

**Gaus Width: 3.5214**



# B0L001S, U17-ch87, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	79
Mean	37.06
Std Dev	3.743

**Gaus mean : 37.9584**

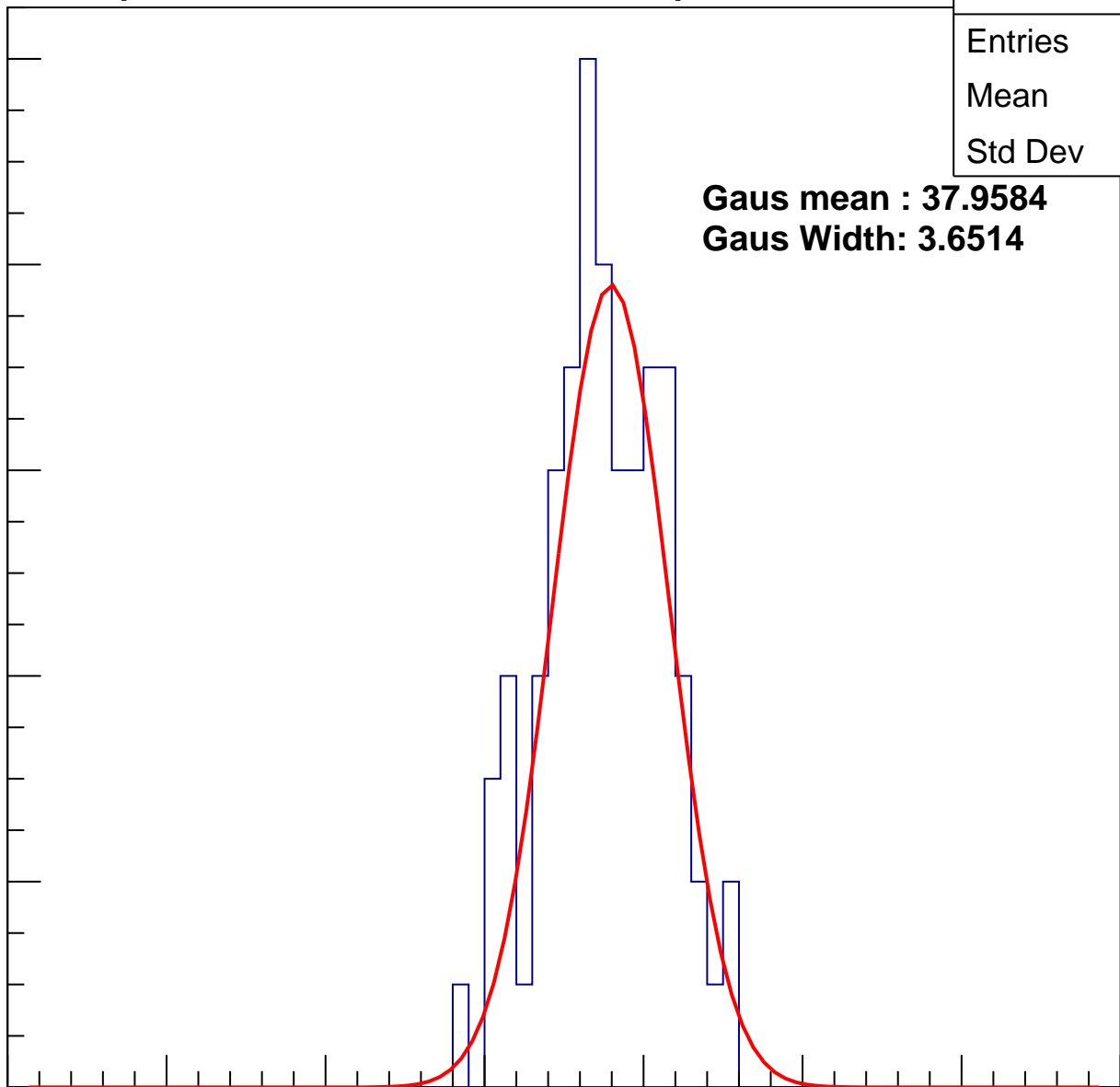
**Gaus Width: 3.6514**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U17-ch87, adc2

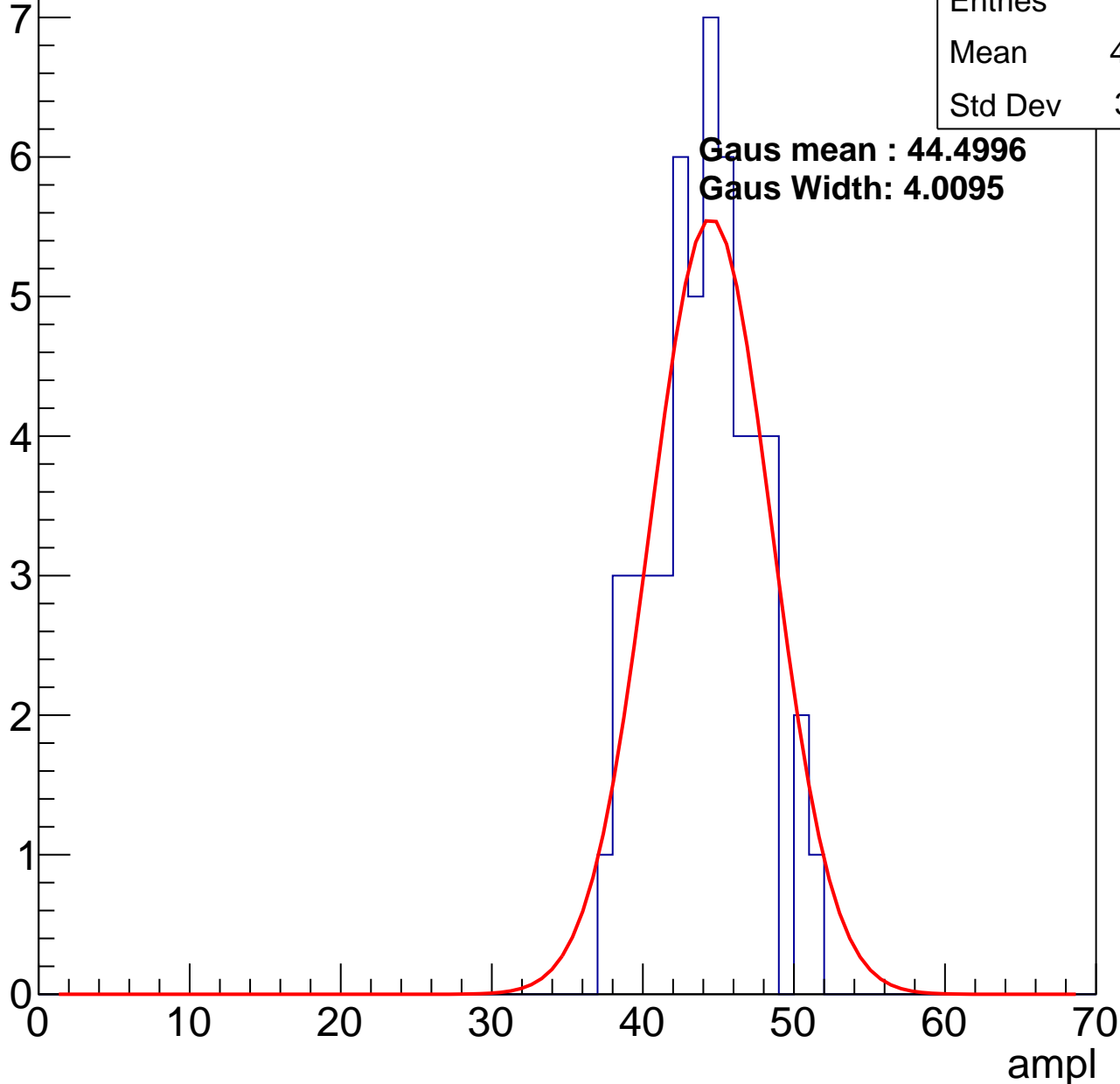
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	43.67
Std Dev	3.321

**Gaus mean : 44.4996**

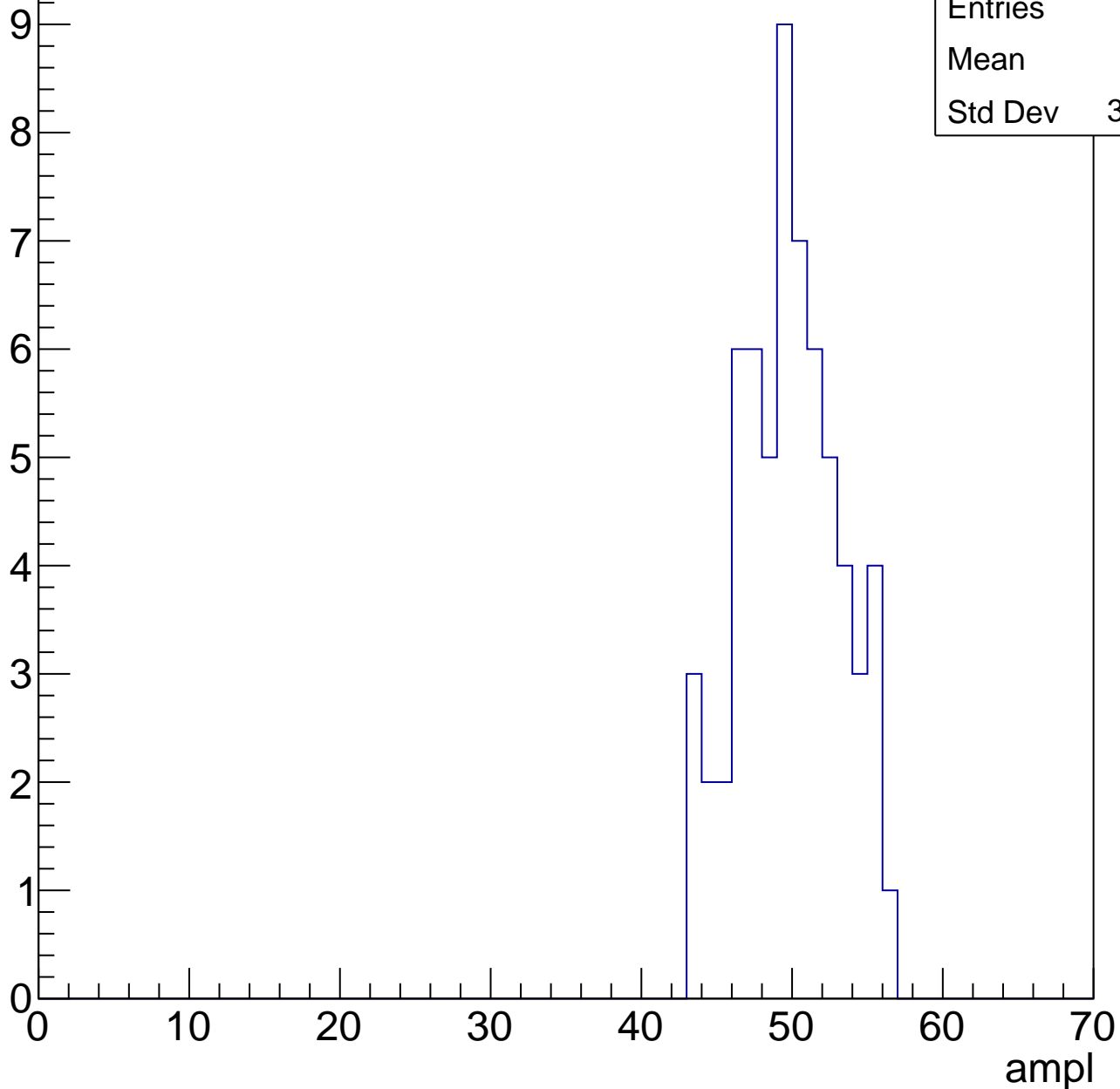
**Gaus Width: 4.0095**



# B0L001S, U17-ch87, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

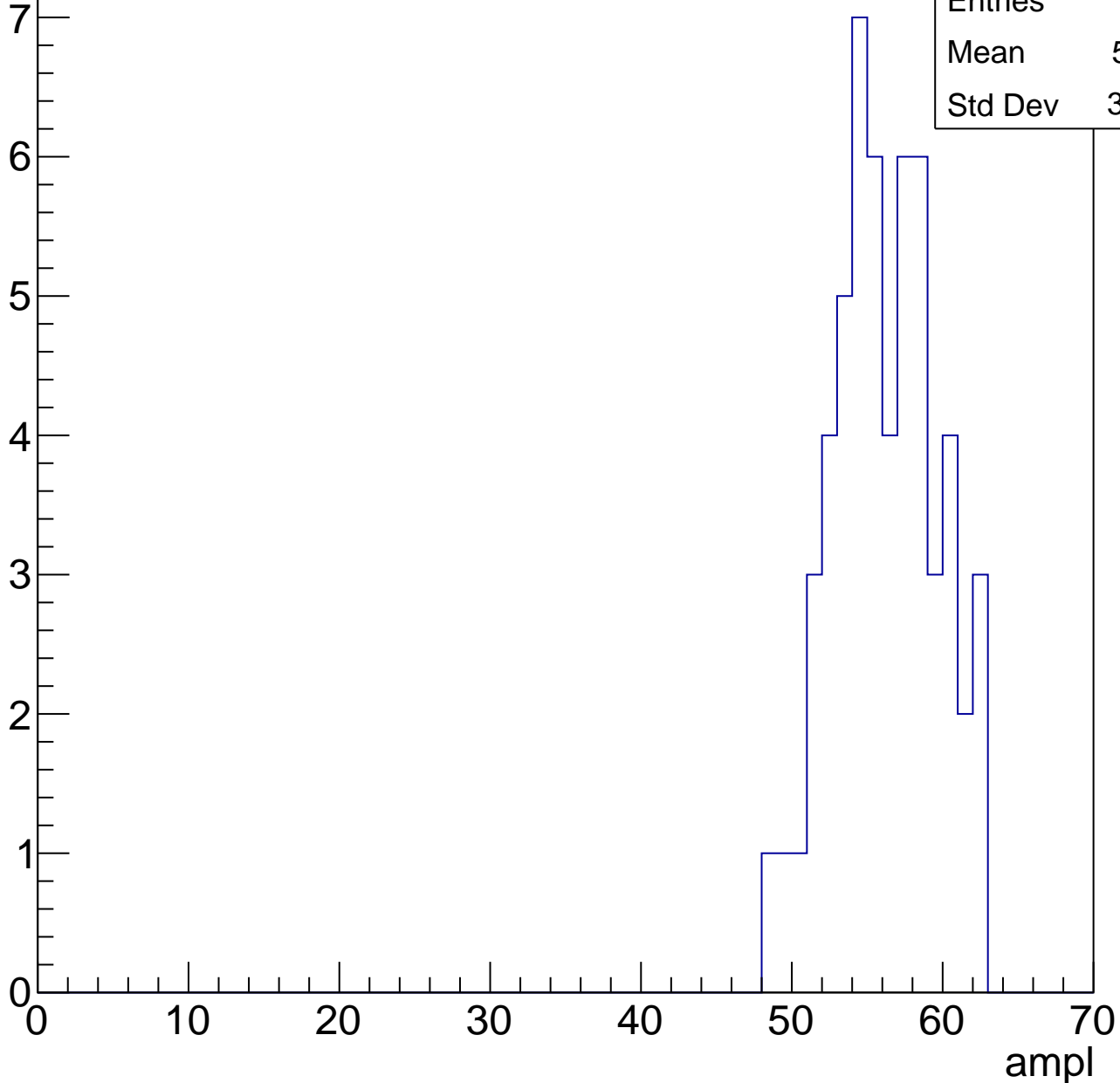


# B0L001S, U17-ch87, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	55.71
Std Dev	3.384

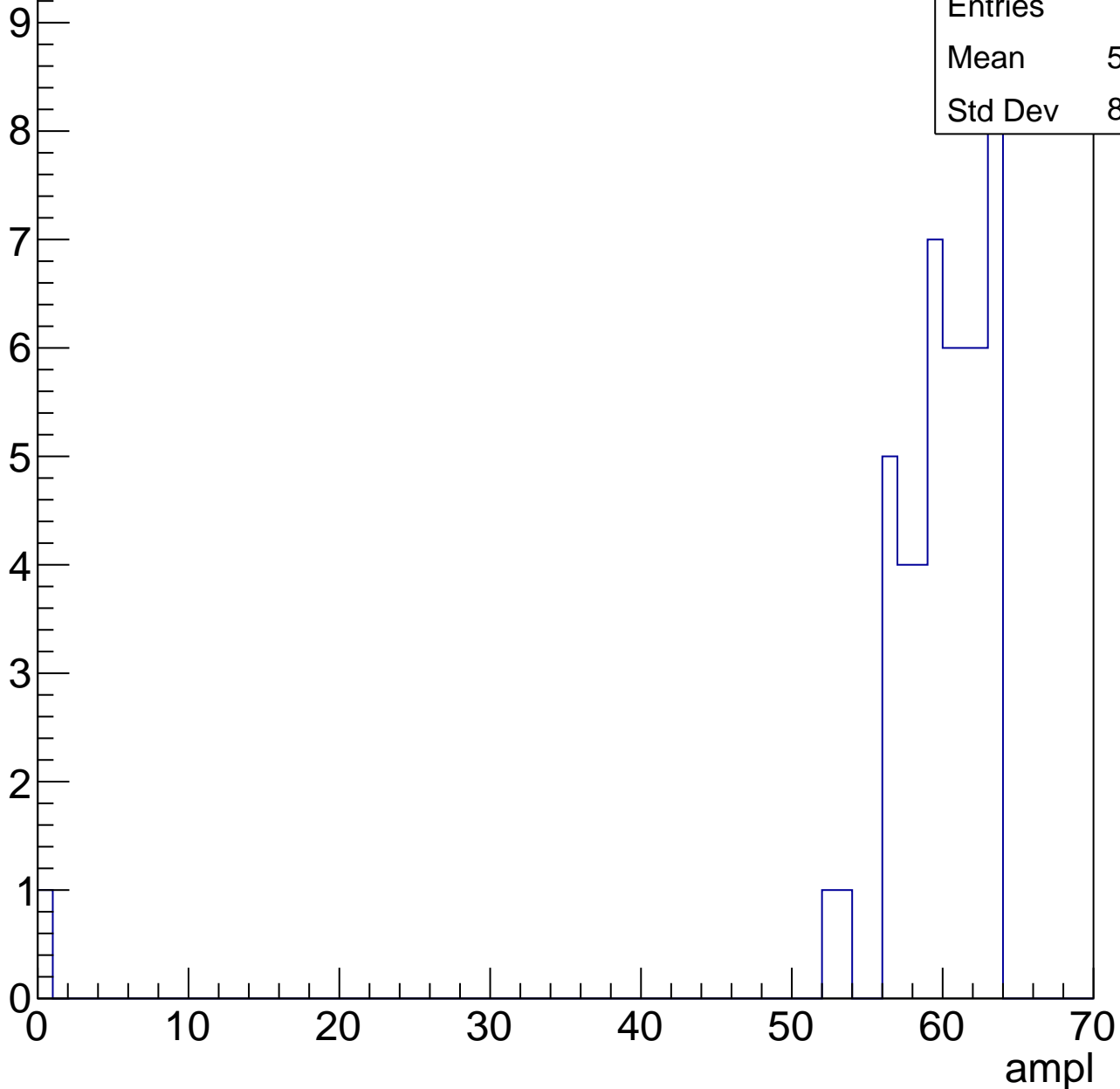


# B0L001S, U17-ch87, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	50
Mean	58.46
Std Dev	8.769



# B0L001S, U17-ch87, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	61.75
Std Dev	0.8292

ampl

0 10 20 30 40 50 60 70



# B0L001S, U17-ch87, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U17-ch88, adc0

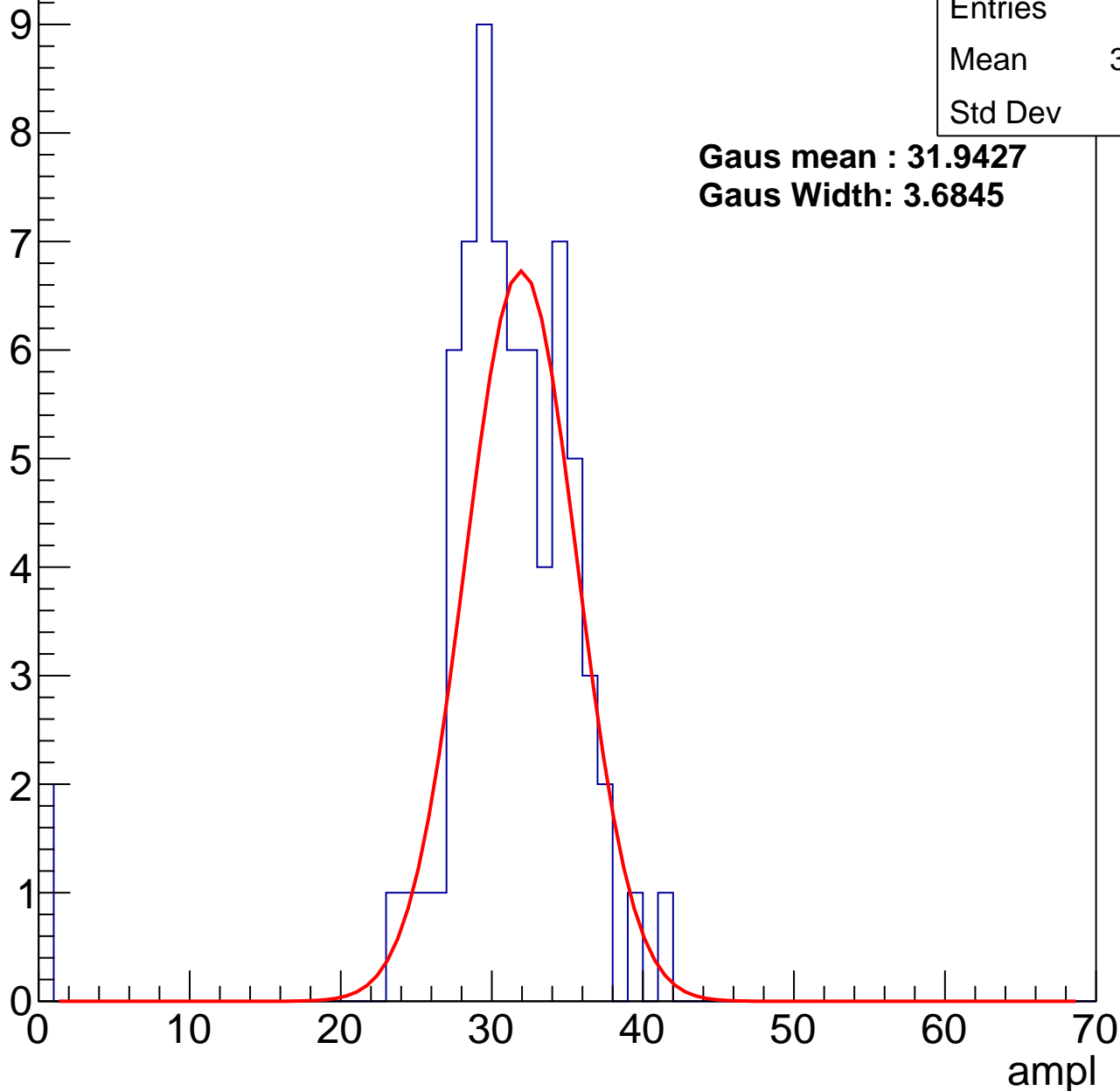
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	30.17
Std Dev	6.24

**Gaus mean : 31.9427**

**Gaus Width: 3.6845**



# B0L001S, U17-ch88, adc1

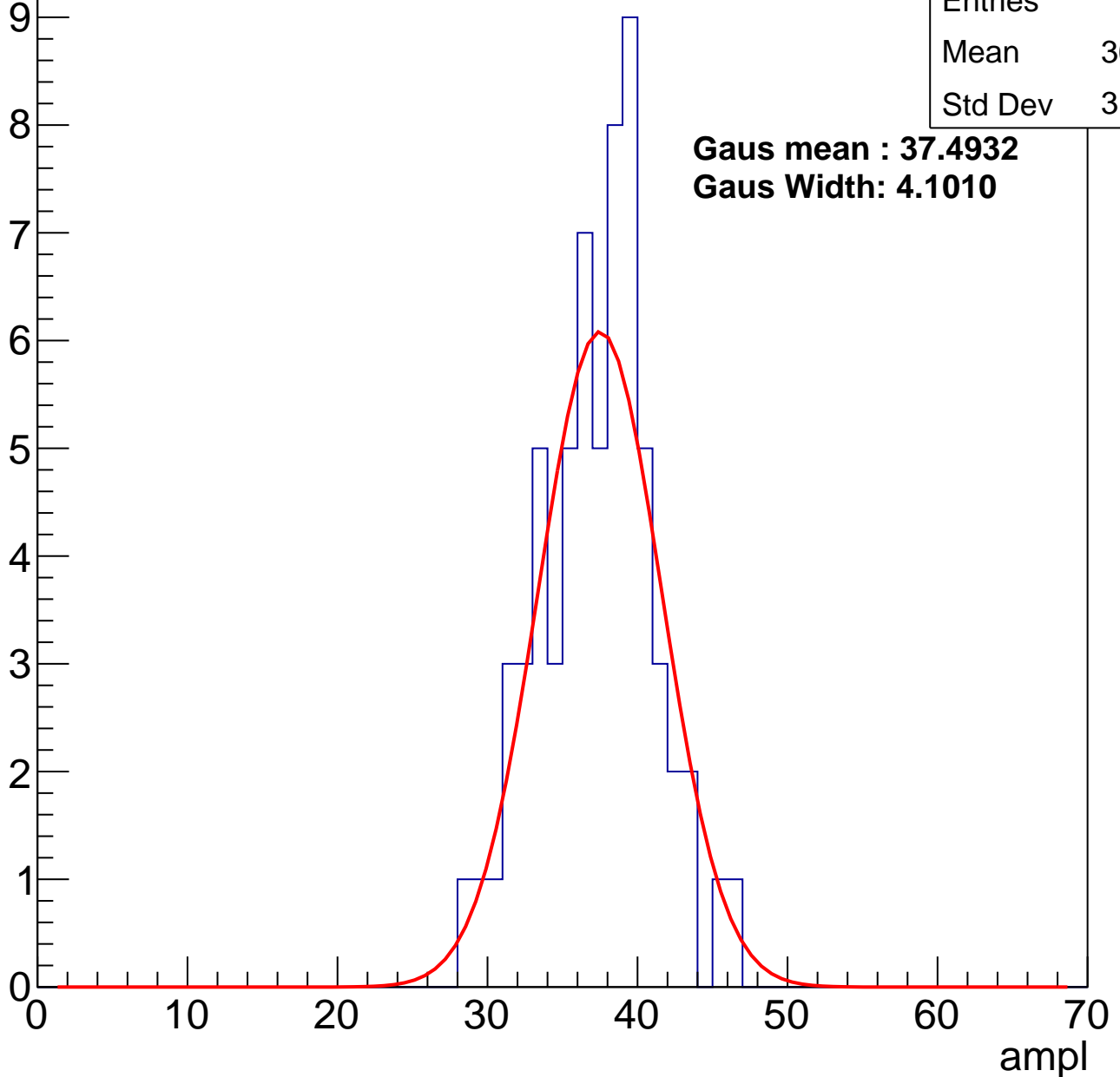
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	36.83
Std Dev	3.748

**Gaus mean : 37.4932**

**Gaus Width: 4.1010**



# B0L001S, U17-ch88, adc2

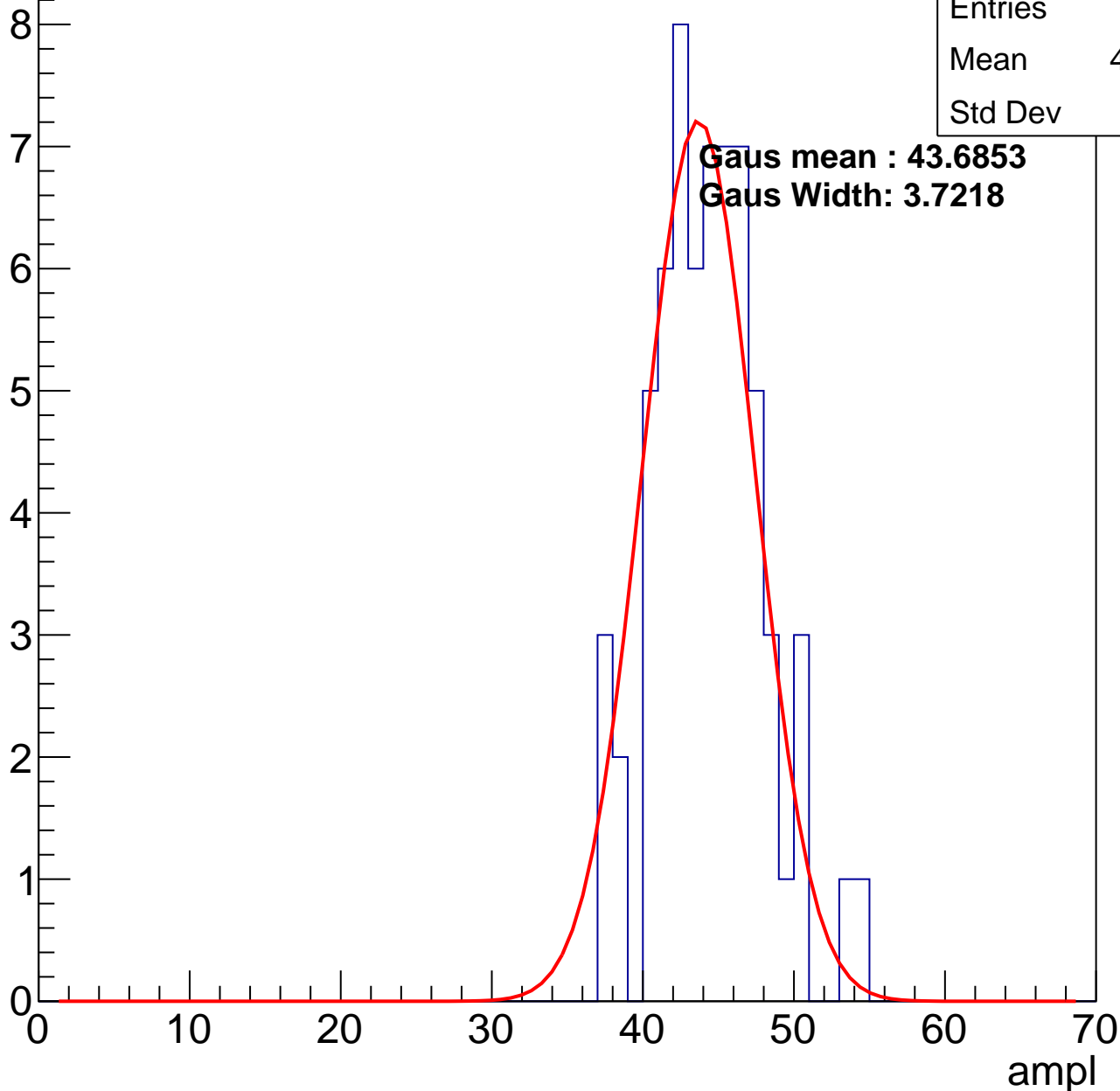
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	43.95
Std Dev	3.58

**Gaus mean : 43.6853**

**Gaus Width: 3.7218**

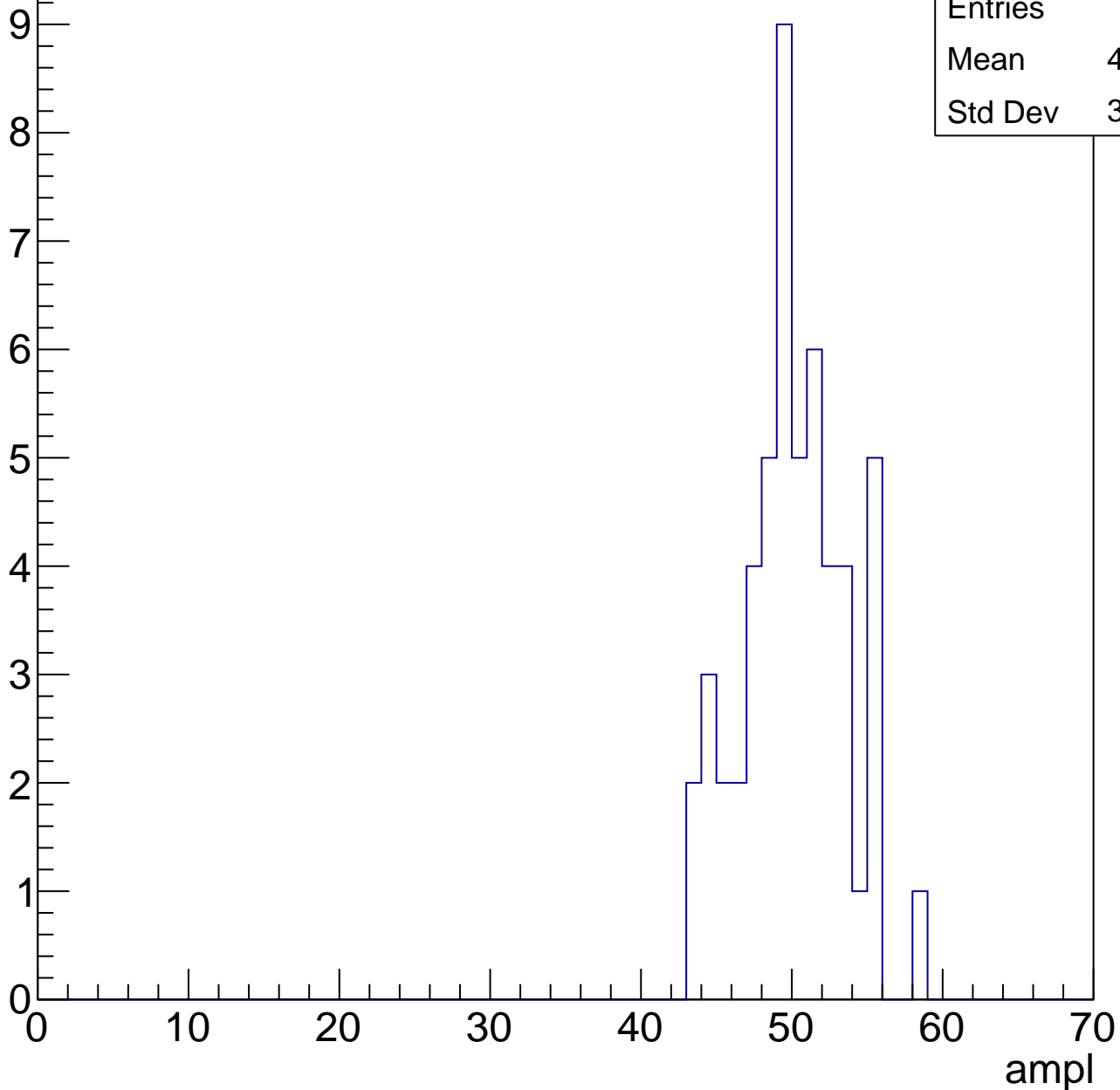


# B0L001S, U17-ch88, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	49.66
Std Dev	3.392

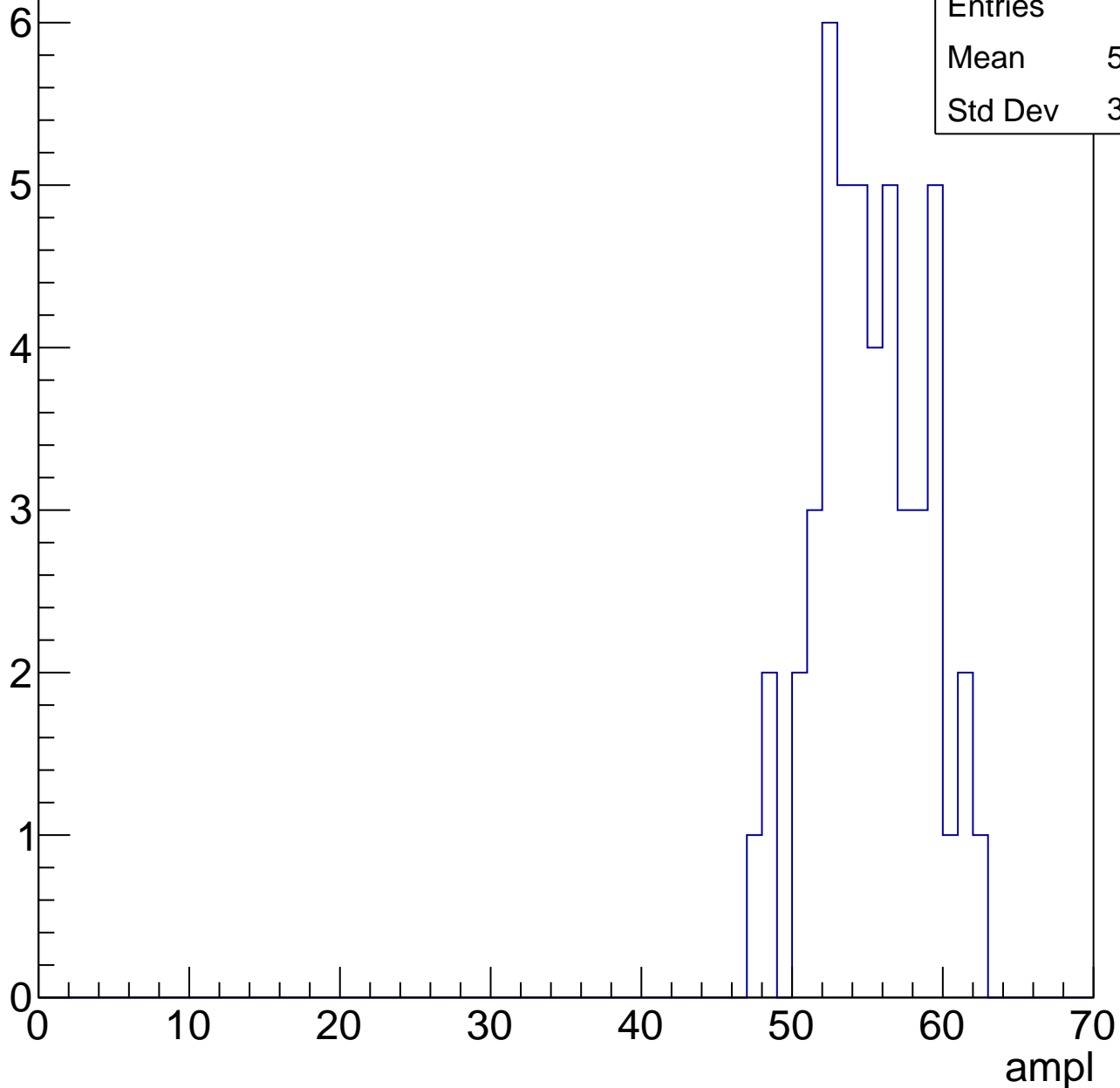


# B0L001S, U17-ch88, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	48
Mean	54.73
Std Dev	3.552

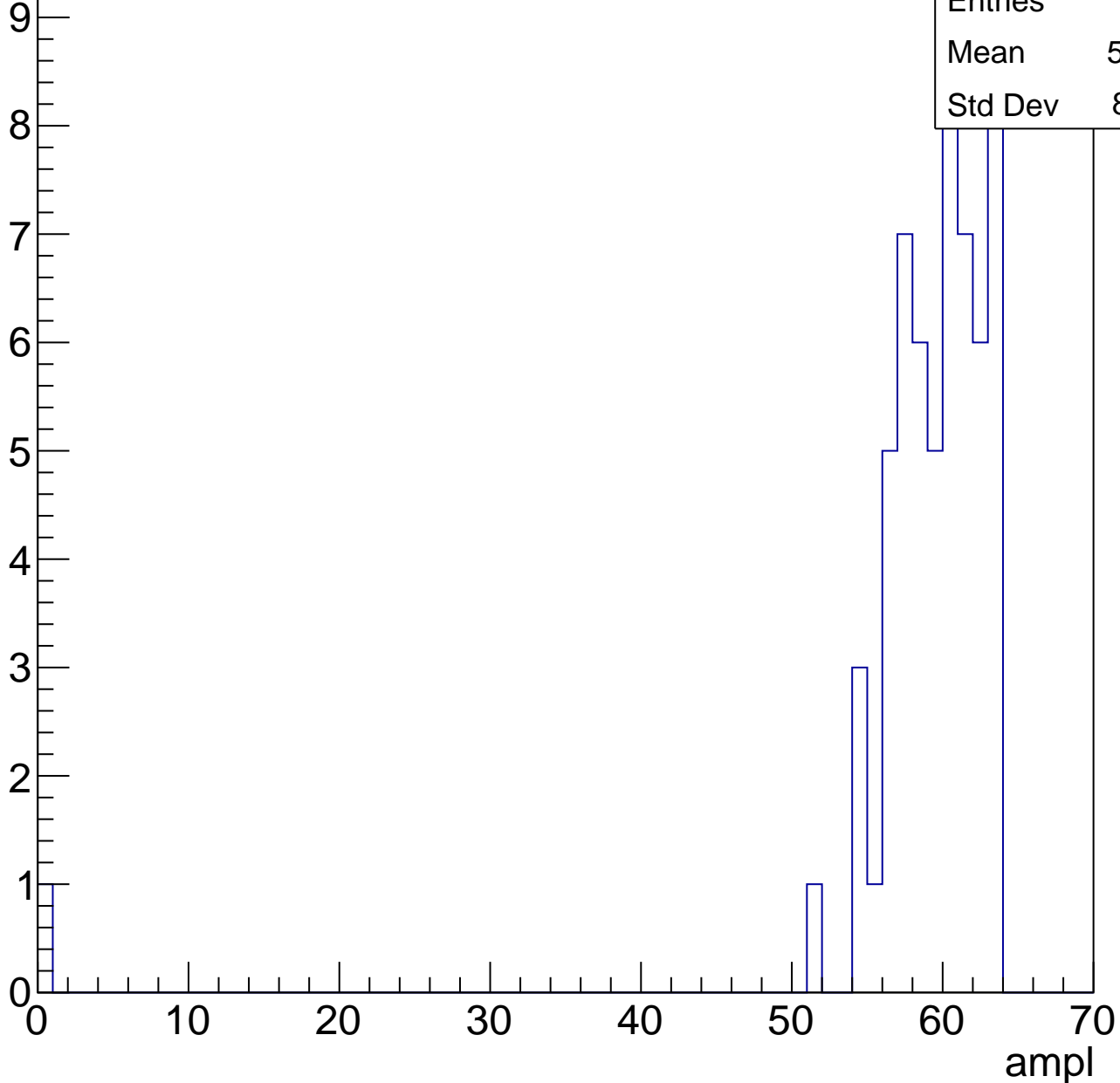


# B0L001S, U17-ch88, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

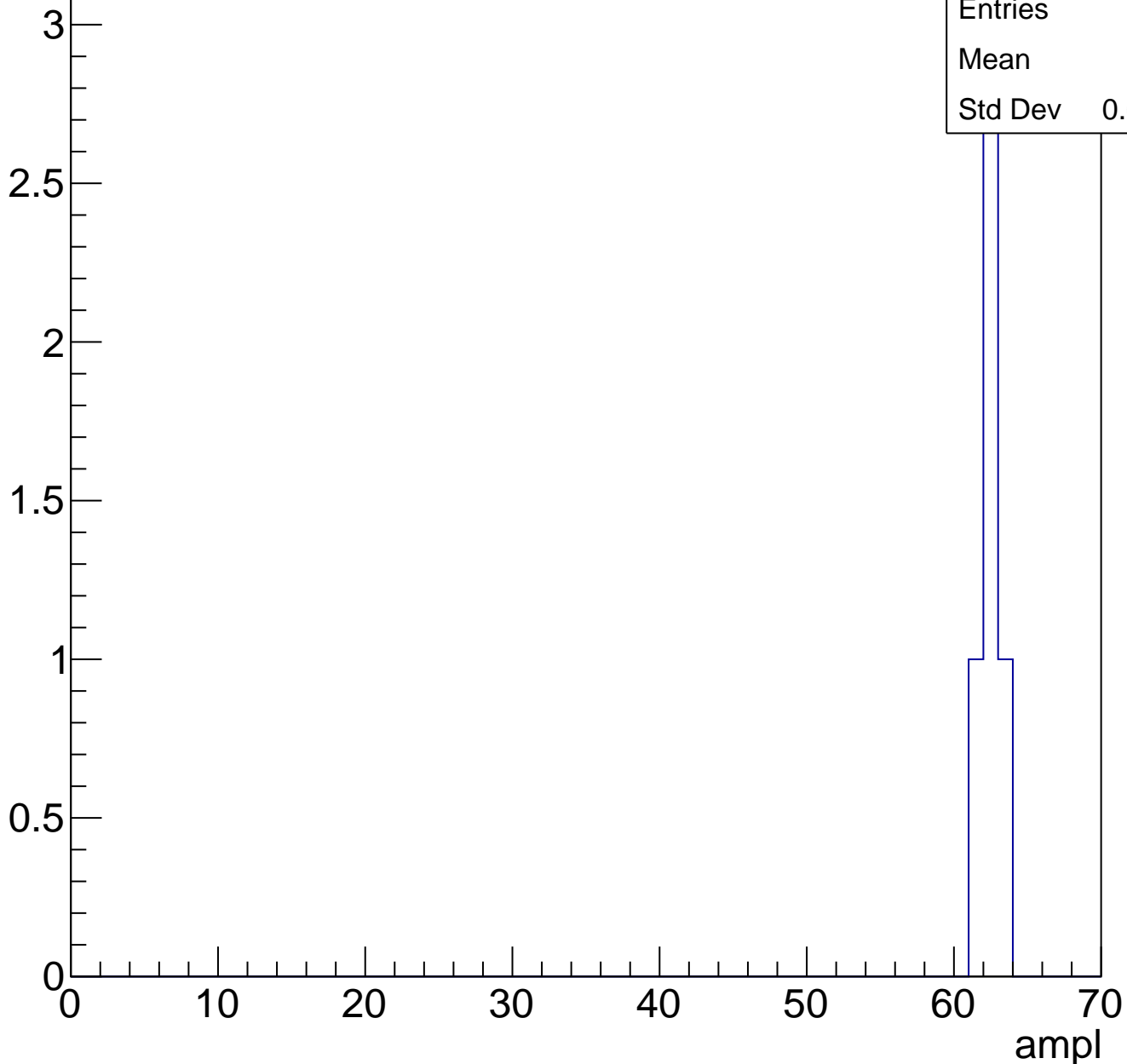
Entries	60
Mean	58.27
Std Dev	8.081



# B0L001S, U17-ch88, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch88, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U17-ch89, adc0

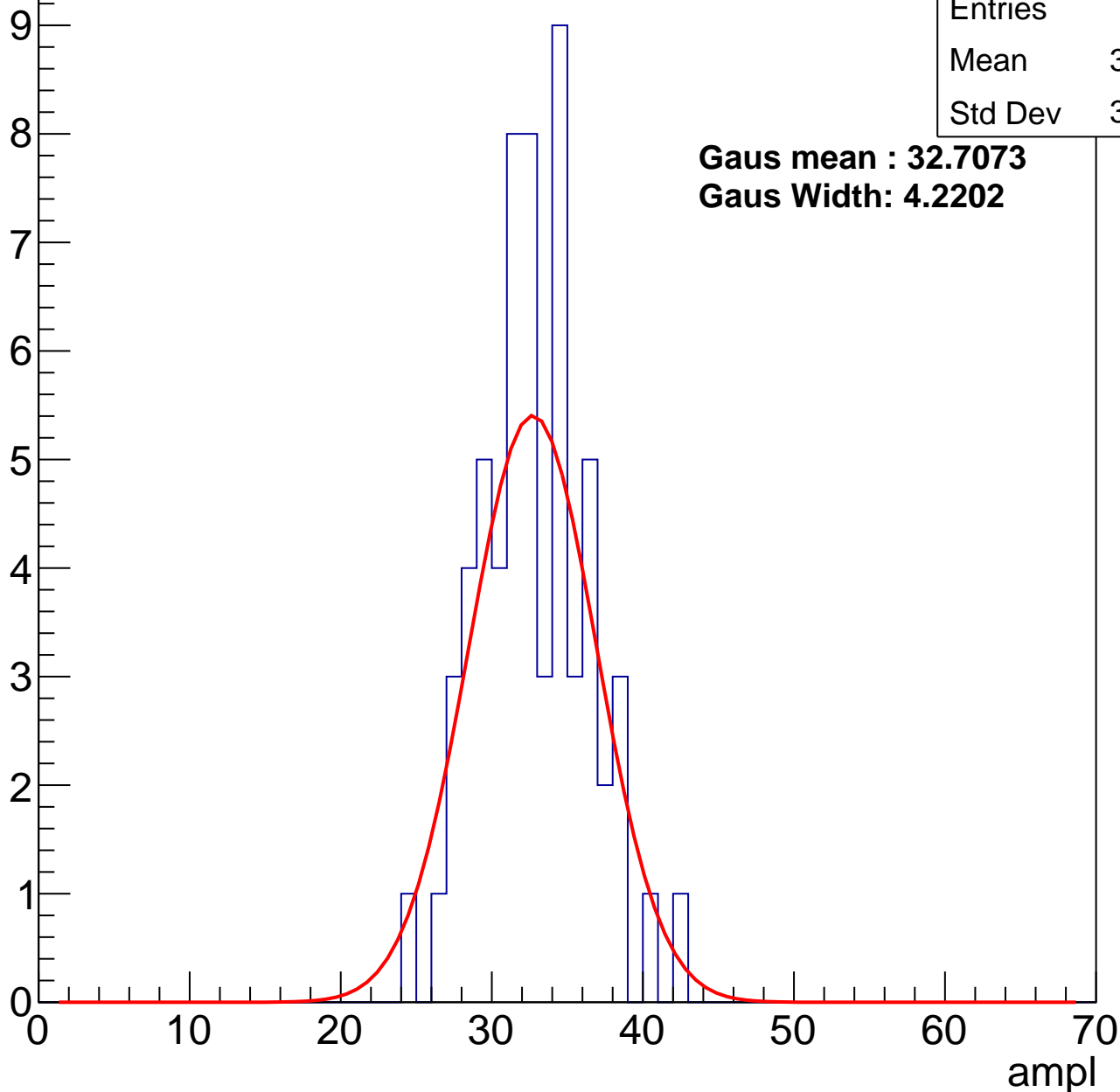
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	32.33
Std Dev	3.552

**Gaus mean : 32.7073**

**Gaus Width: 4.2202**



# B0L001S, U17-ch89, adc1

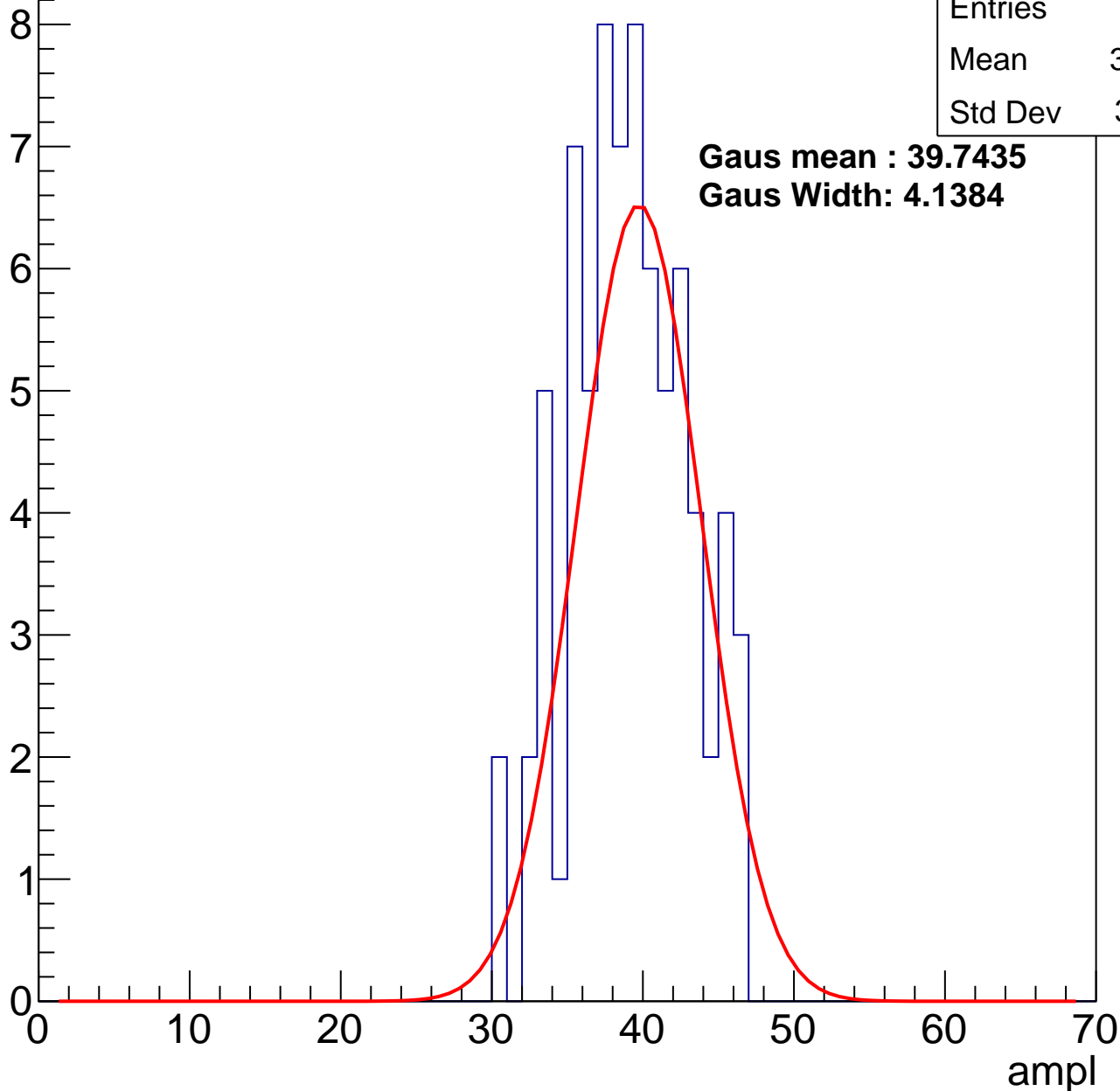
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	75
Mean	38.63
Std Dev	3.891

**Gaus mean : 39.7435**

**Gaus Width: 4.1384**



# B0L001S, U17-ch89, adc2

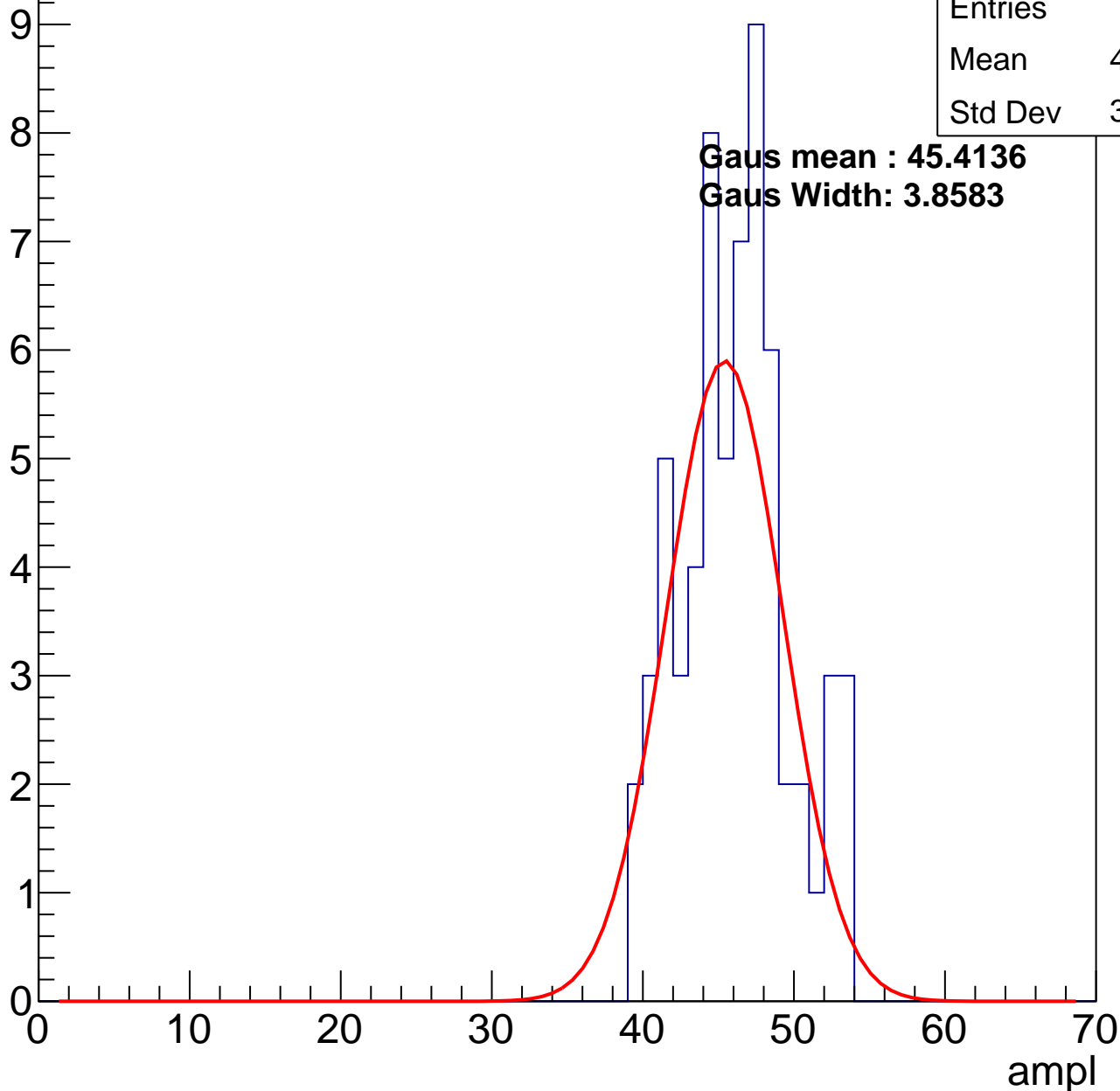
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	45.63
Std Dev	3.578

**Gaus mean : 45.4136**

**Gaus Width: 3.8583**

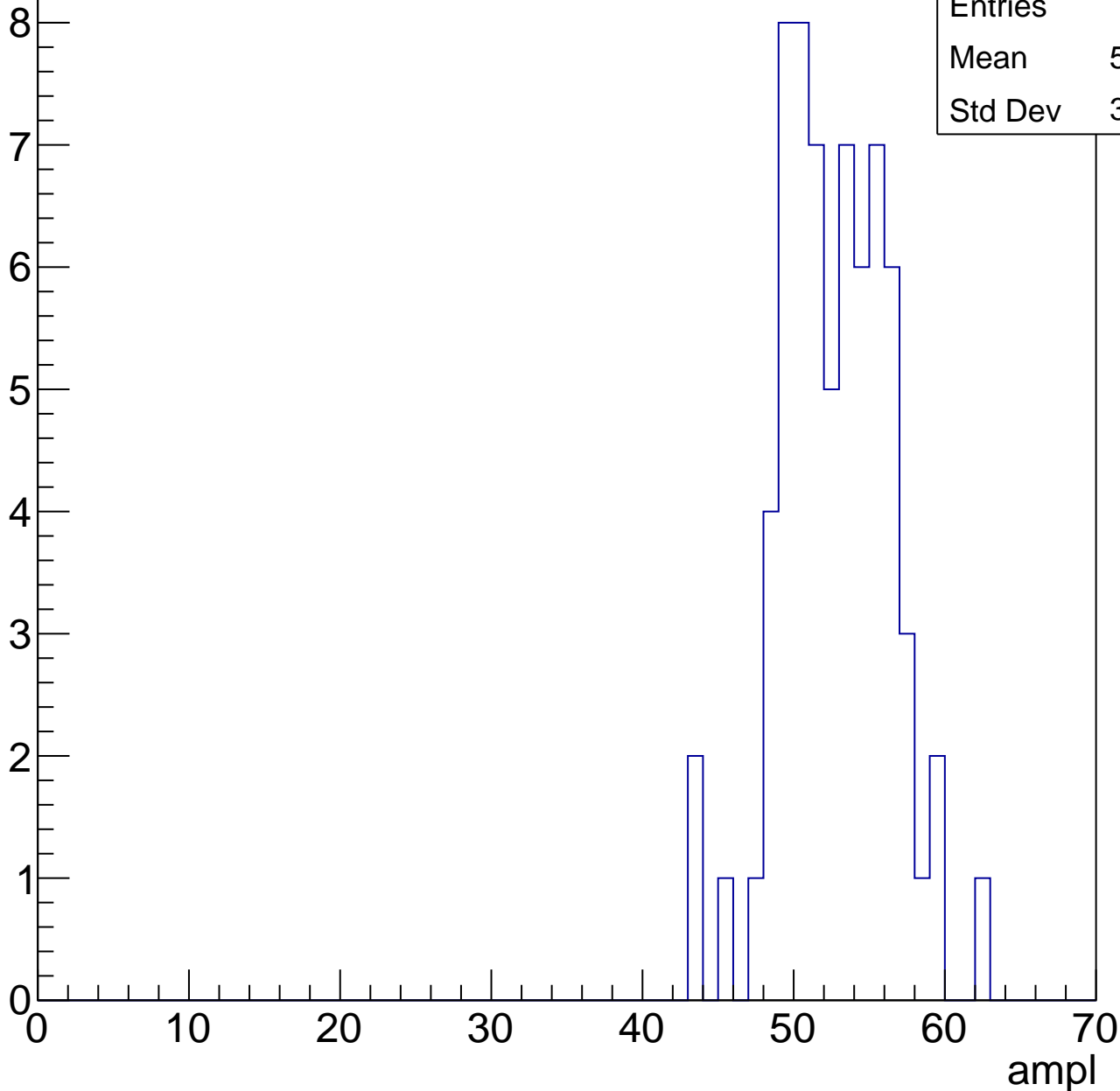


# B0L001S, U17-ch89, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	52.23
Std Dev	3.624

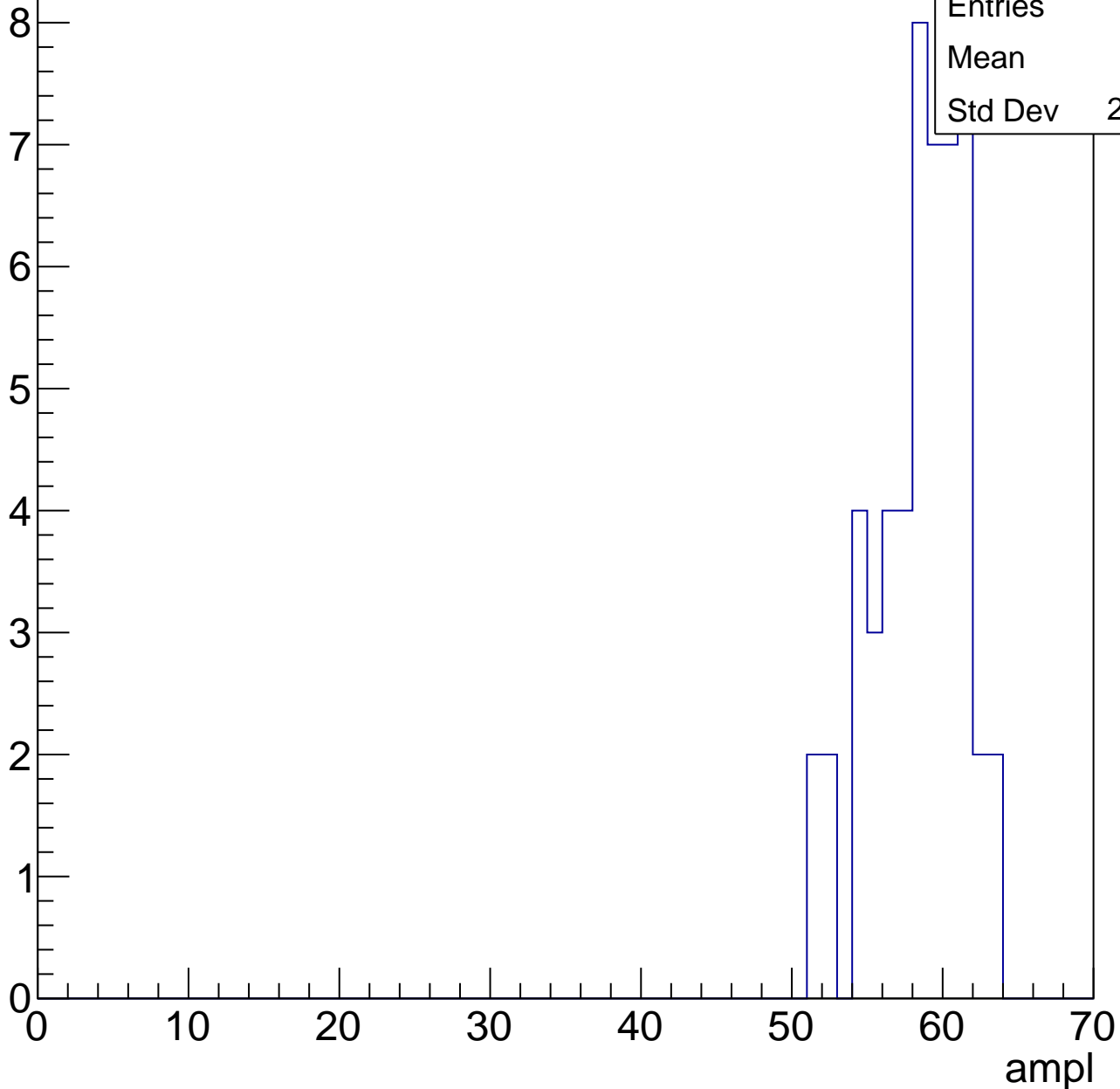


# B0L001S, U17-ch89, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	58
Std Dev	2.978

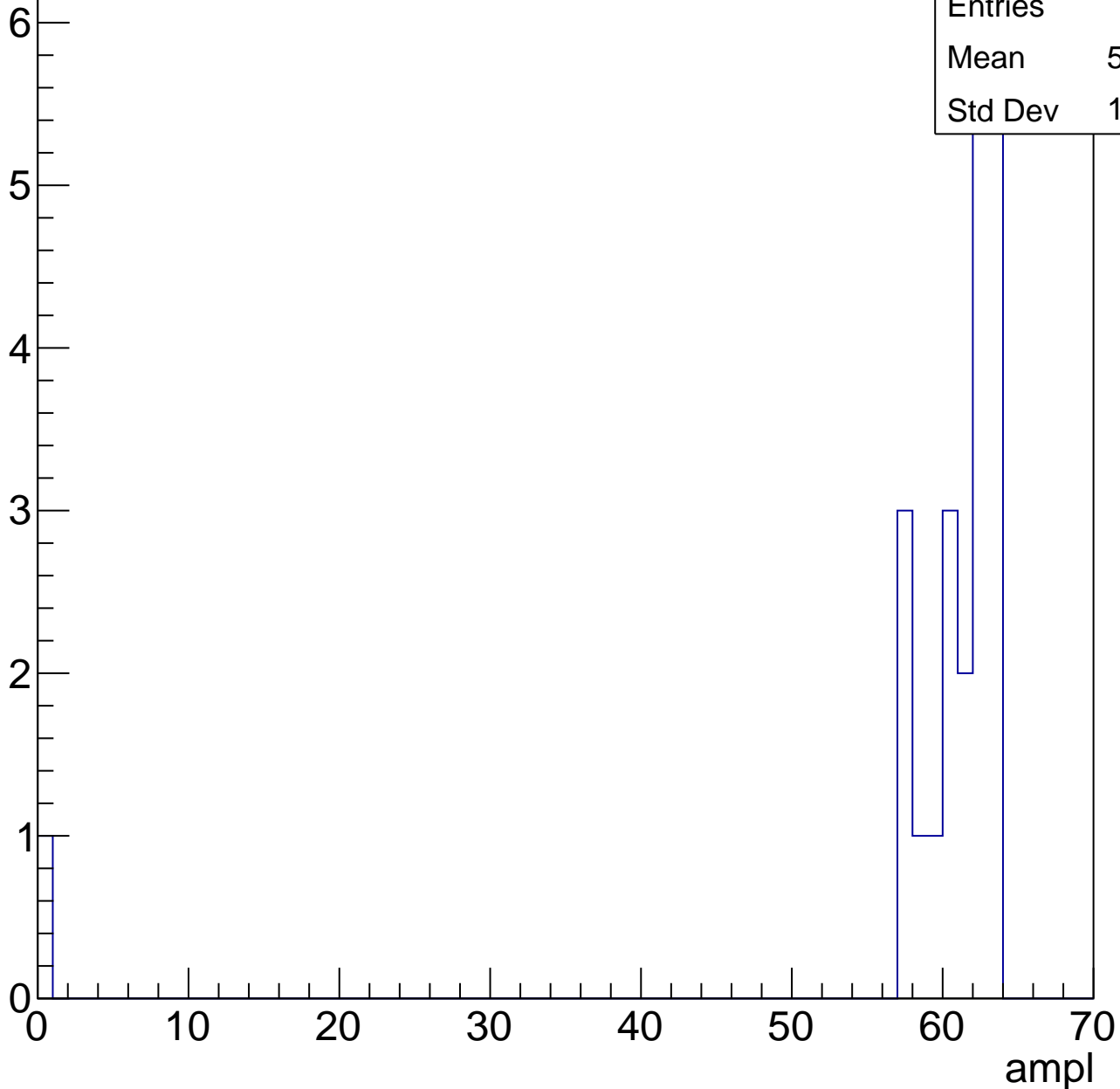


# B0L001S, U17-ch89, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	23
Mean	58.26
Std Dev	12.58



# B0L001S, U17-ch89, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.67
Std Dev	0.4714

ampl

0 10 20 30 40 50 60 70



# B0L001S, U17-ch89, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U17-ch90, adc0

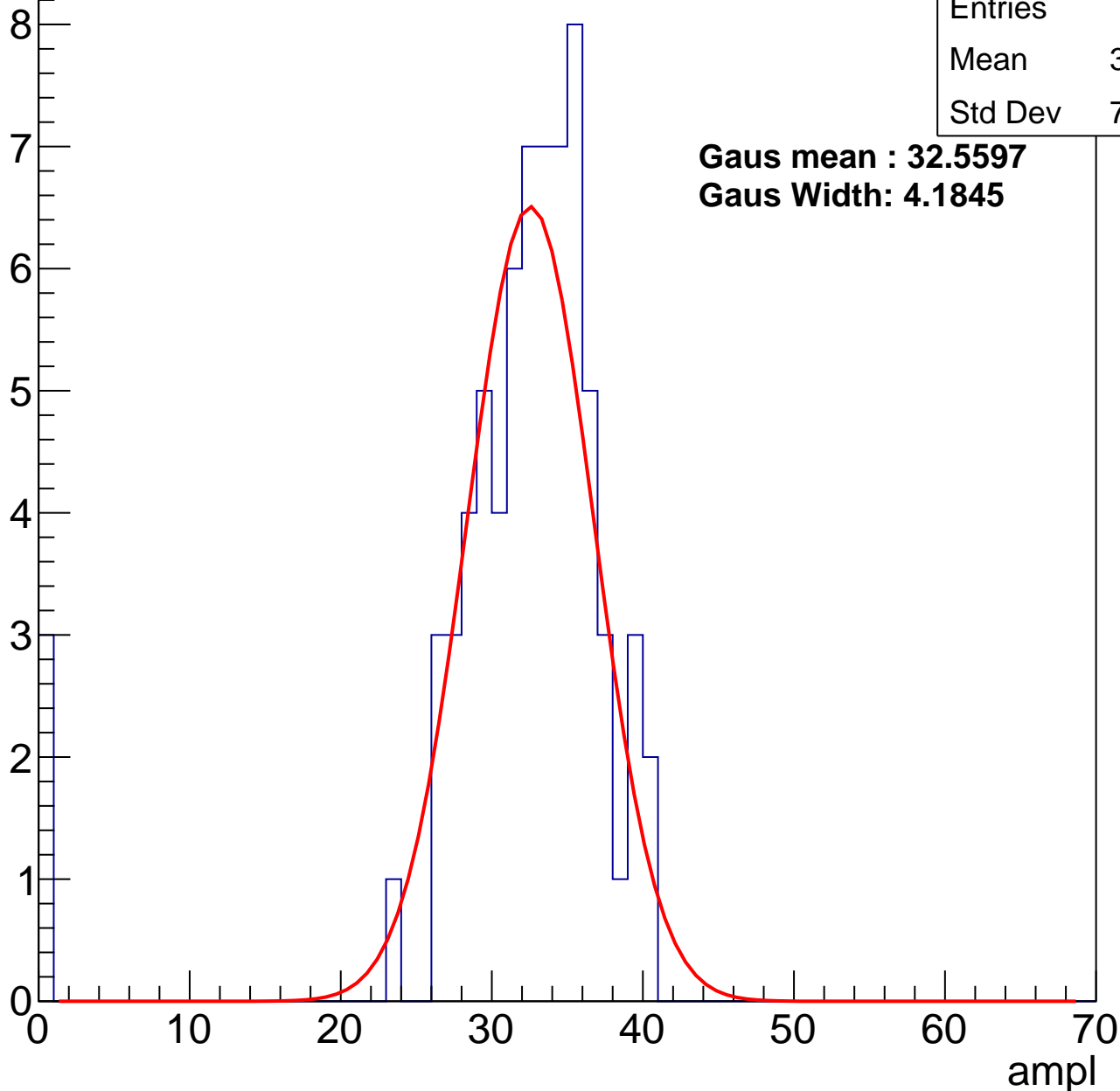
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	31.17
Std Dev	7.444

**Gaus mean : 32.5597**

**Gaus Width: 4.1845**



# B0L001S, U17-ch90, adc1

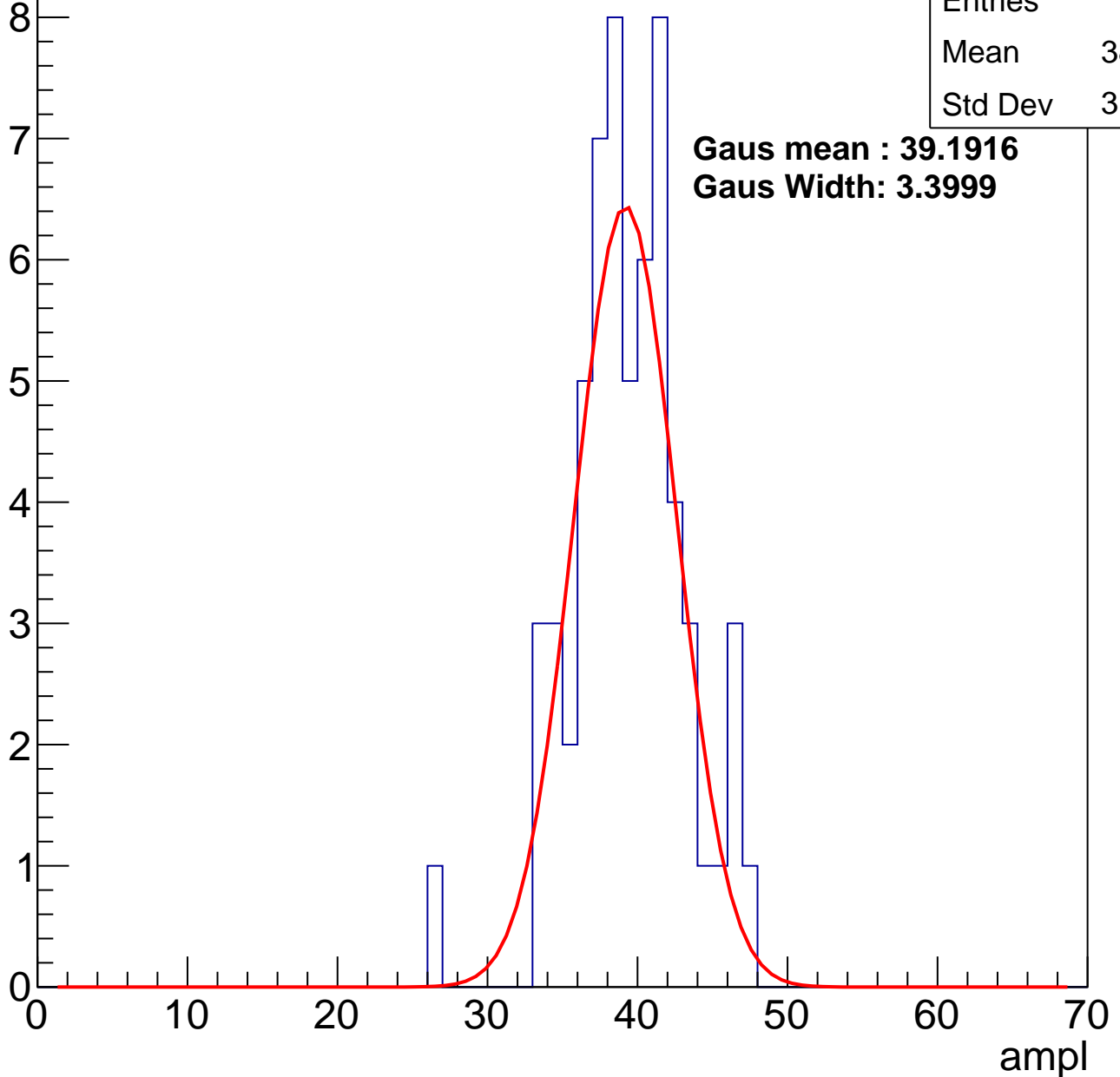
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	38.92
Std Dev	3.752

**Gaus mean : 39.1916**

**Gaus Width: 3.3999**



# B0L001S, U17-ch90, adc2

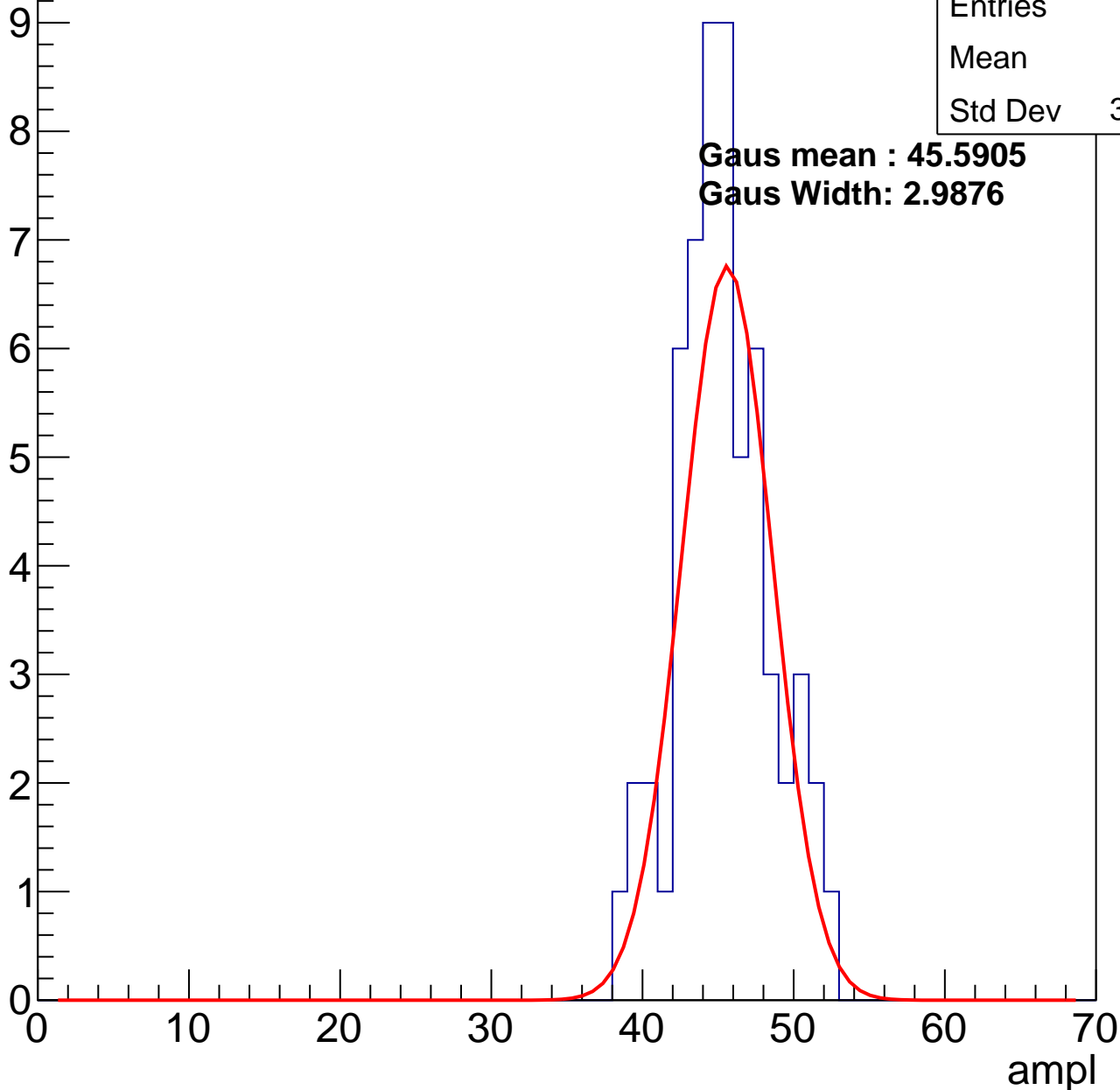
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	44.9
Std Dev	3.085

**Gaus mean : 45.5905**

**Gaus Width: 2.9876**

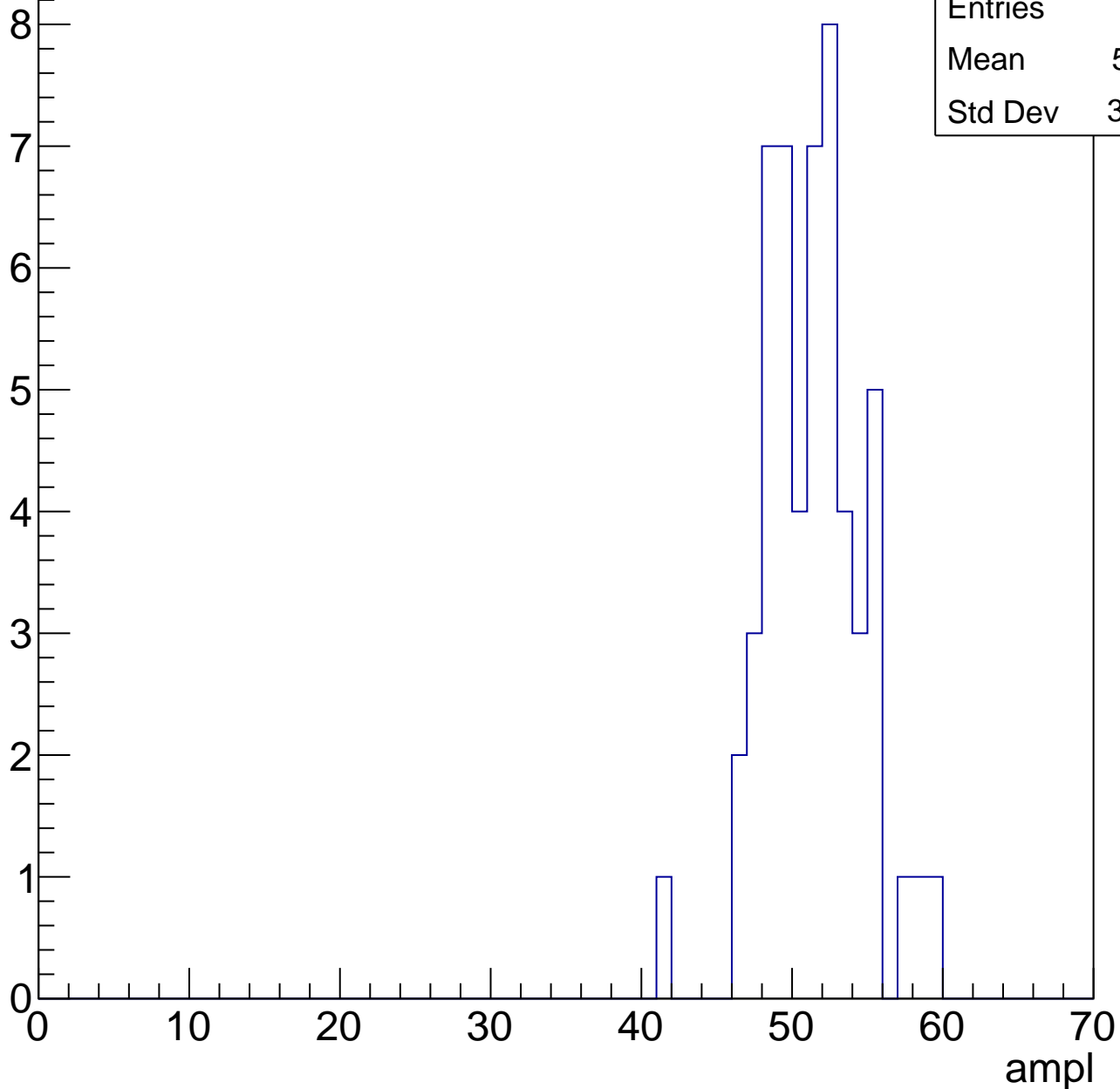


# B0L001S, U17-ch90, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	50.91
Std Dev	3.256

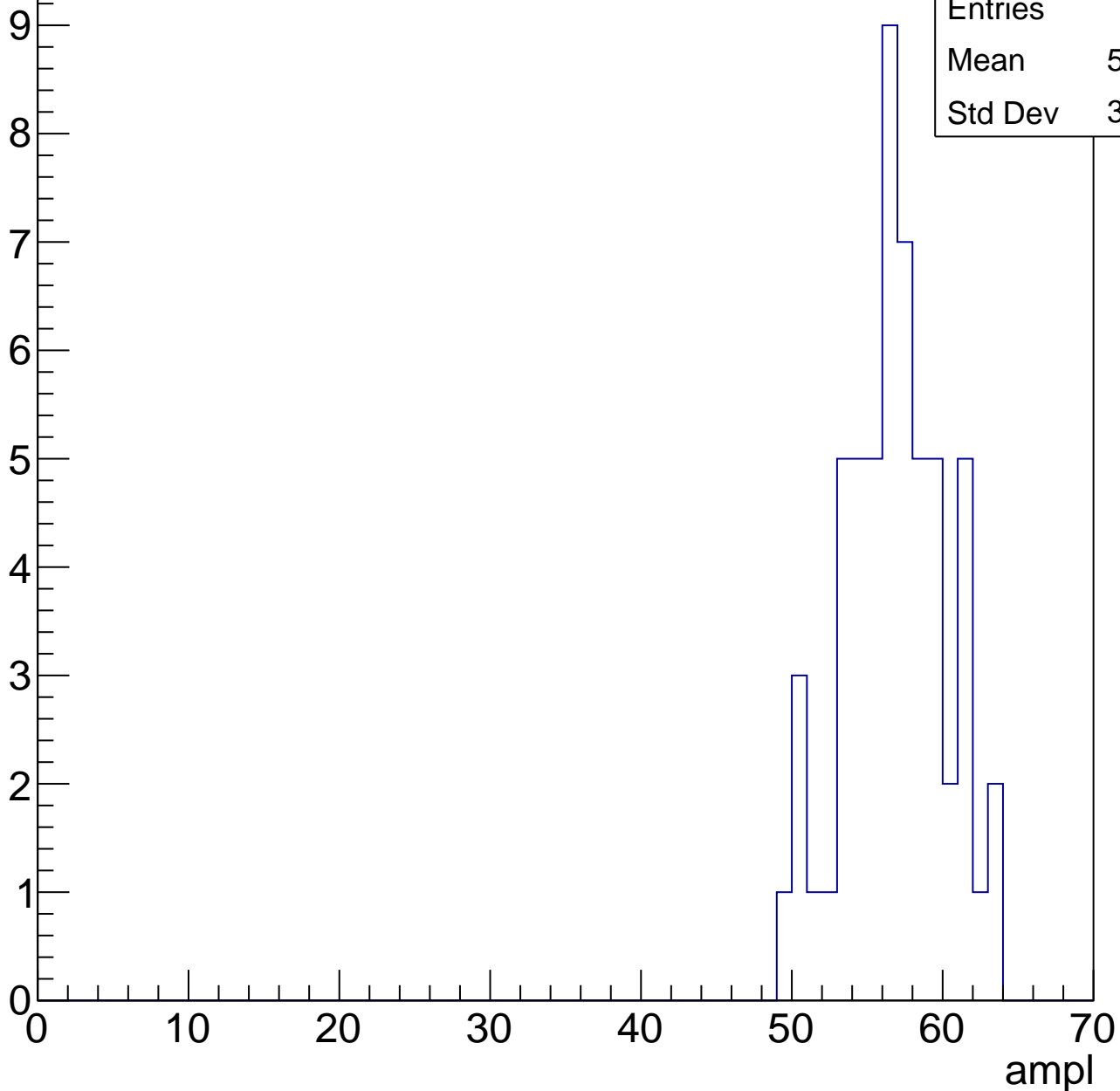


# B0L001S, U17-ch90, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	56.37
Std Dev	3.307

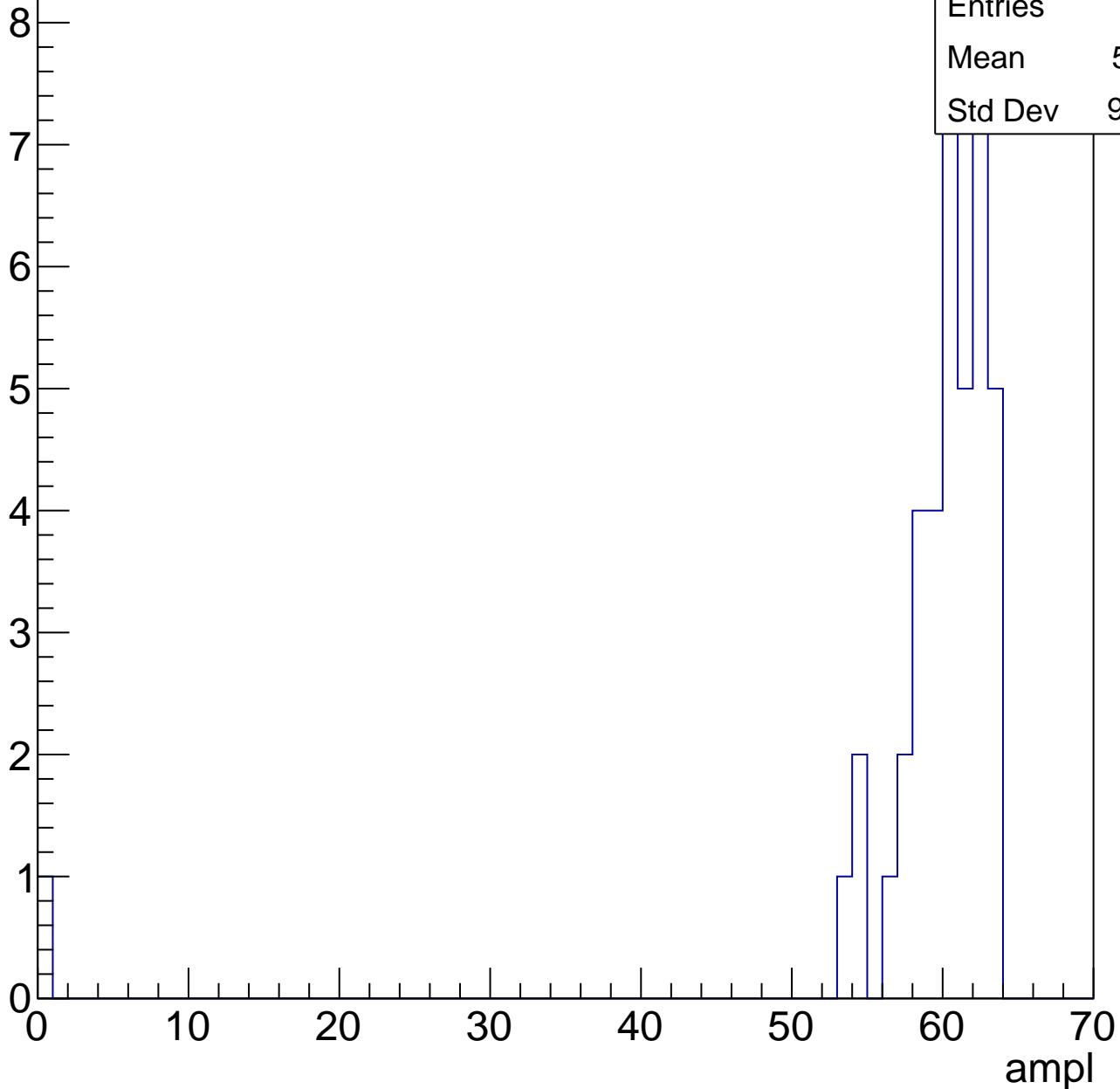


# B0L001S, U17-ch90, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	41
Mean	58.41
Std Dev	9.569



# B0L001S, U17-ch90, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	4
Mean	62.75
Std Dev	0.433



# B0L001S, U17-ch90, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U17-ch91, adc0

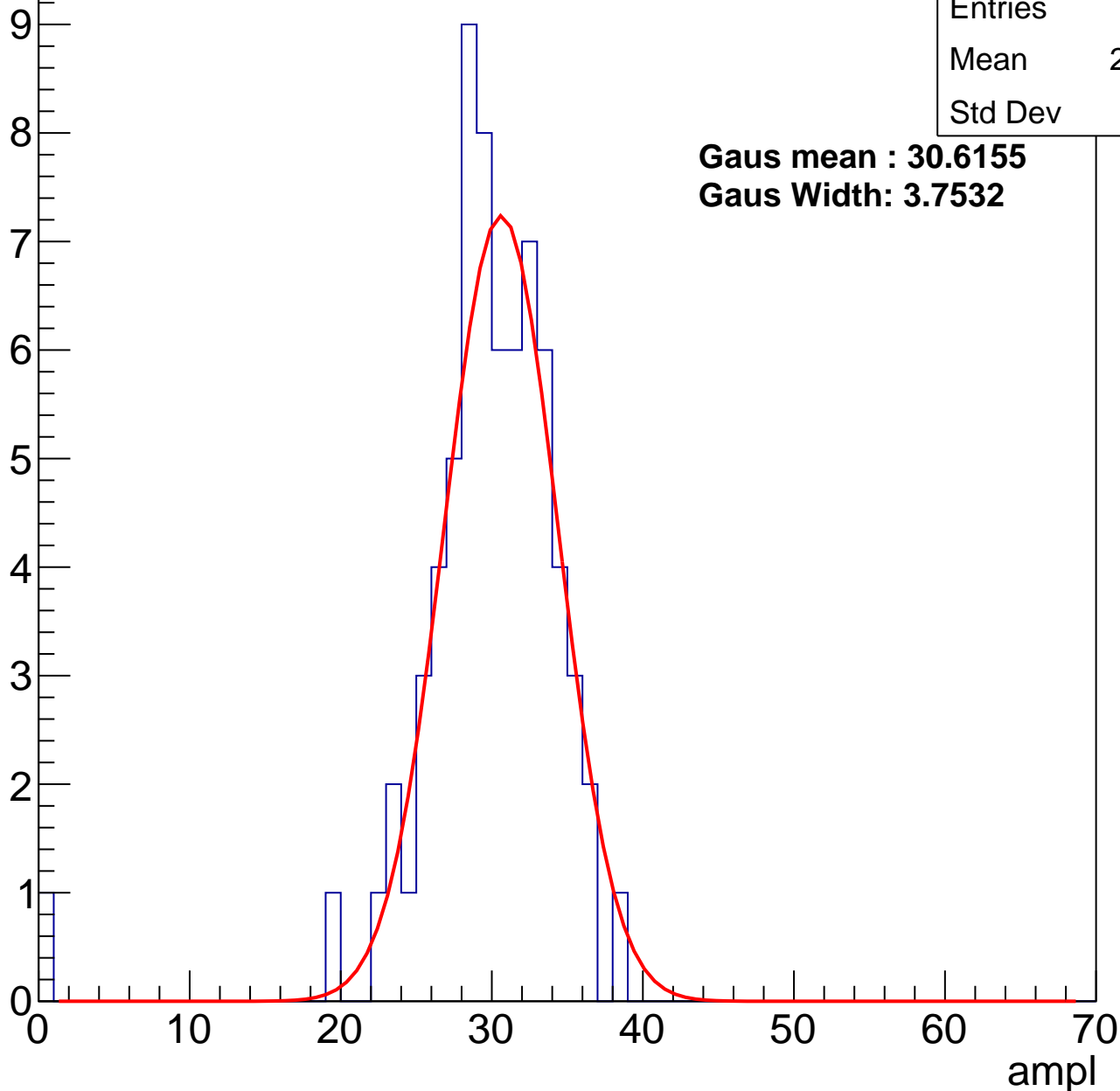
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	29.26
Std Dev	5.03

**Gaus mean : 30.6155**

**Gaus Width: 3.7532**



# B0L001S, U17-ch91, adc1

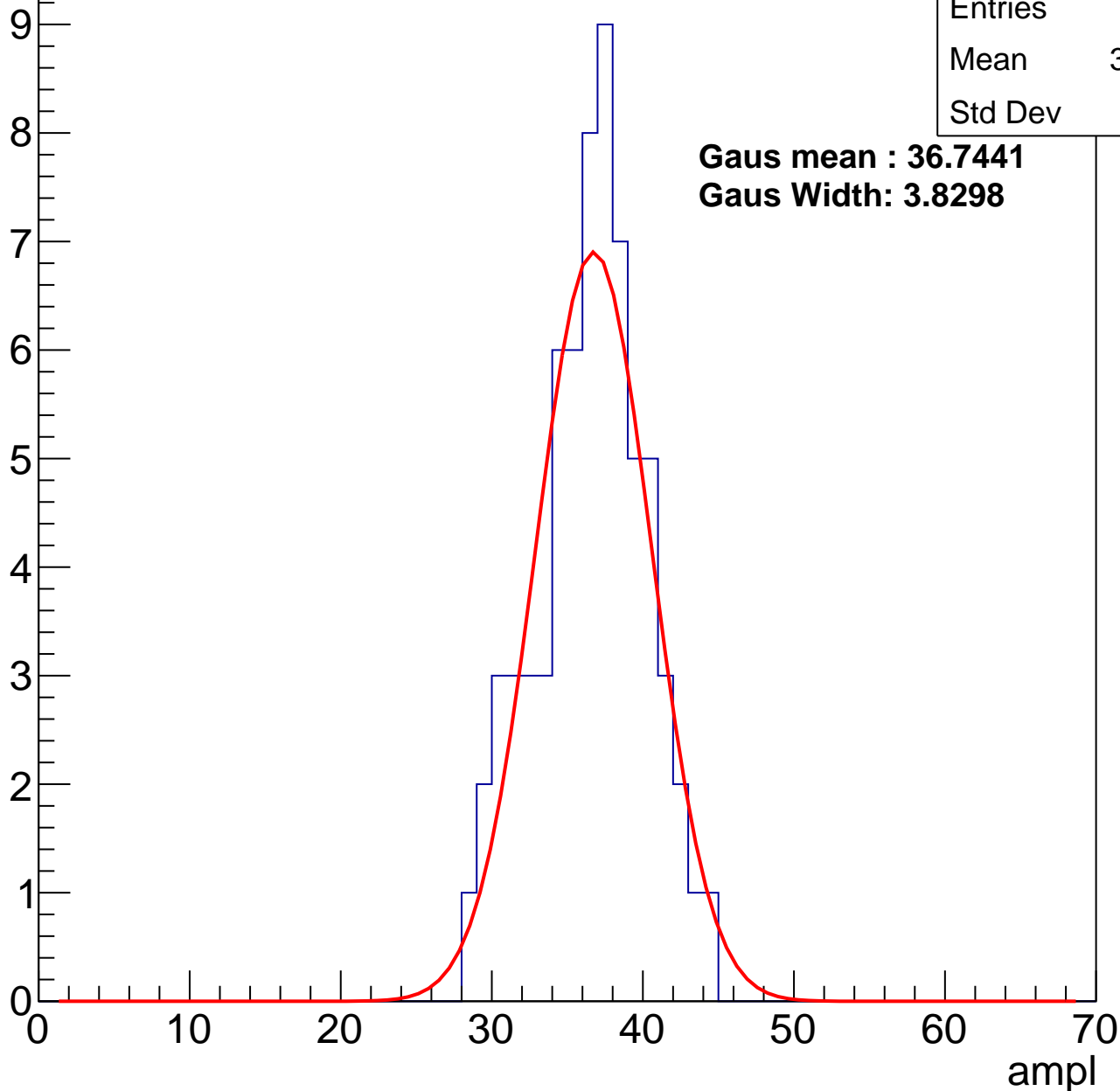
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	36.09
Std Dev	3.58

**Gaus mean : 36.7441**

**Gaus Width: 3.8298**



# B0L001S, U17-ch91, adc2

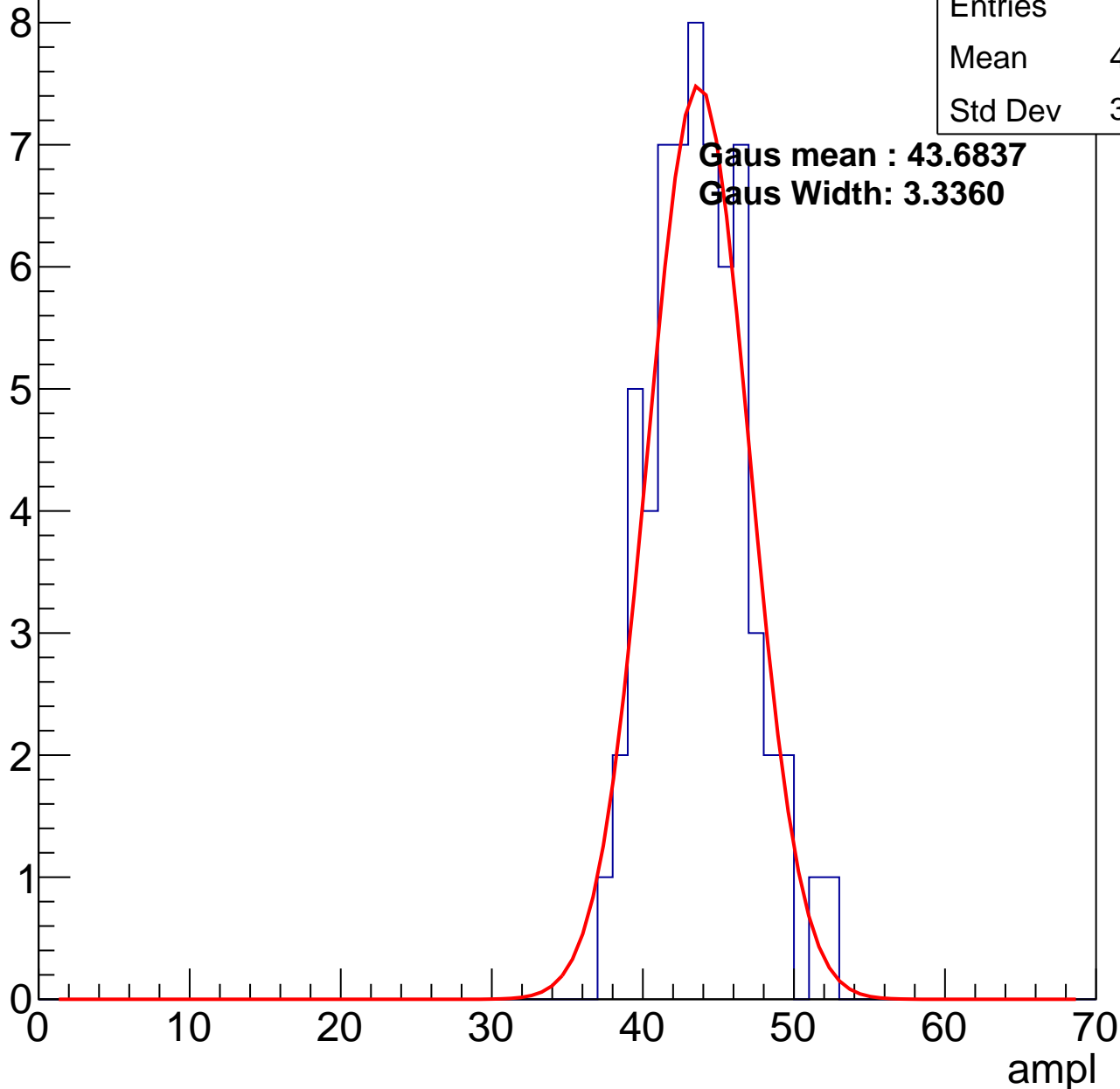
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	43.35
Std Dev	3.183

**Gaus mean : 43.6837**

**Gaus Width: 3.3360**

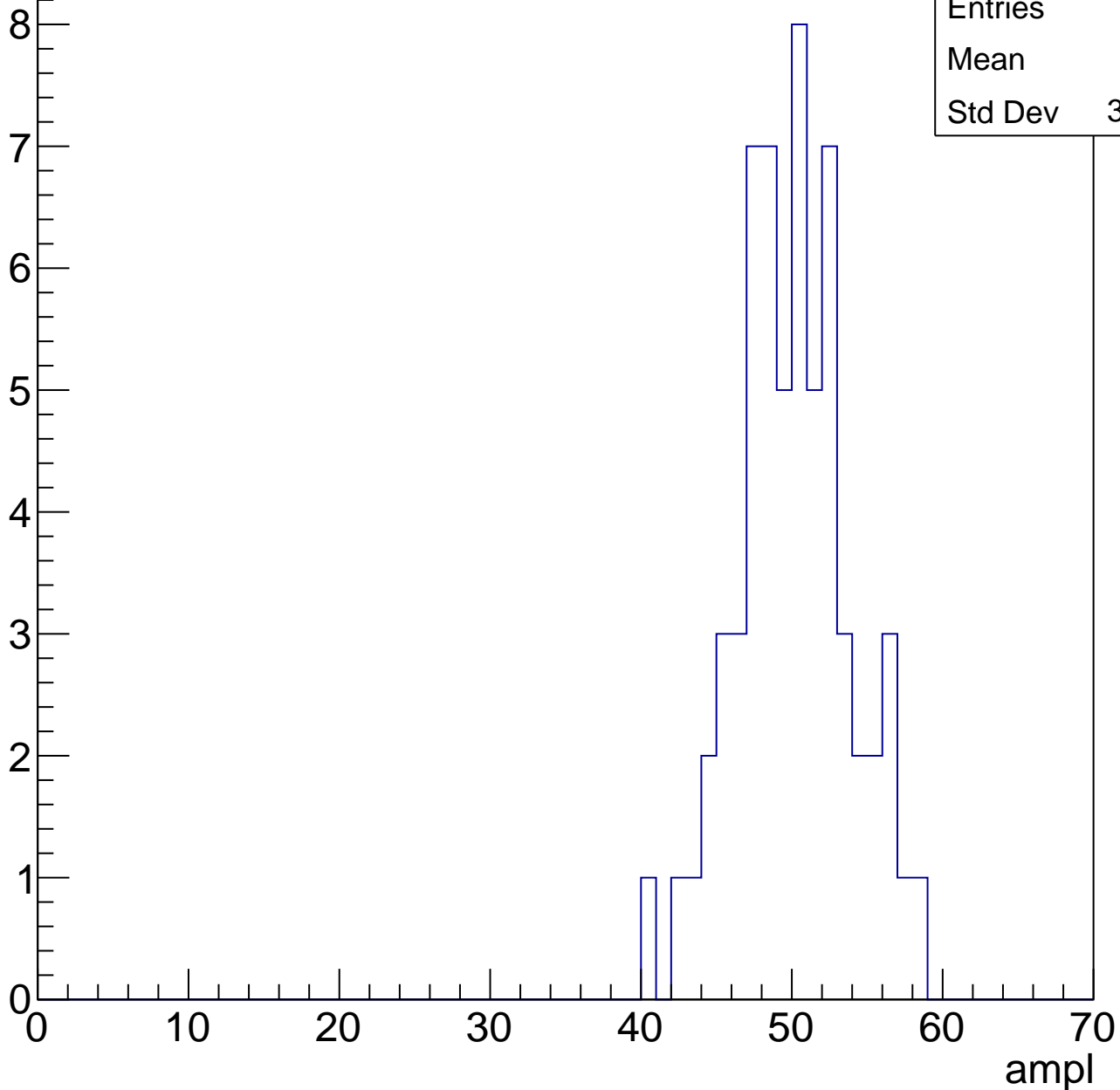


# B0L001S, U17-ch91, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	49.6
Std Dev	3.718

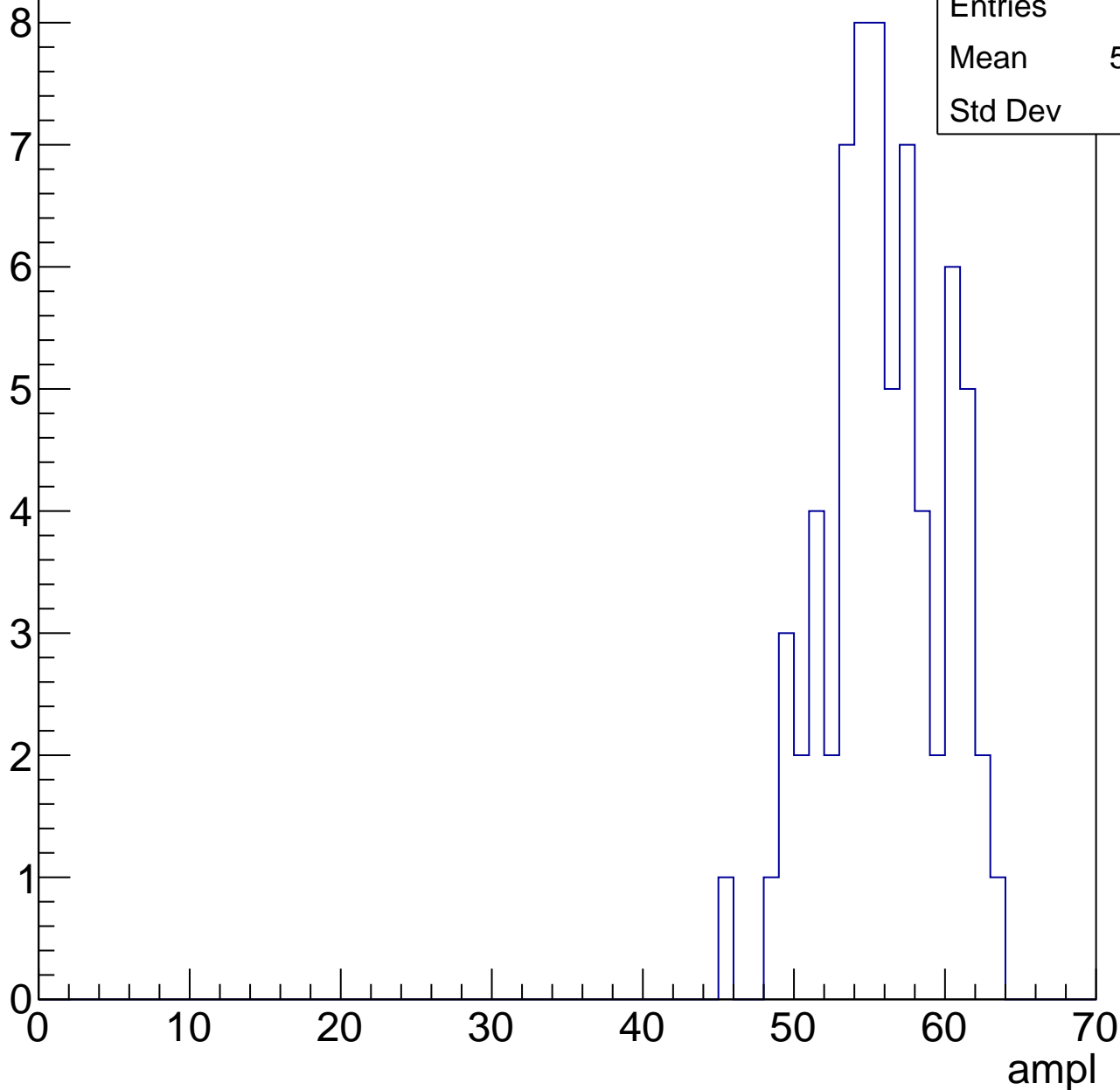


# B0L001S, U17-ch91, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	55.47
Std Dev	3.84

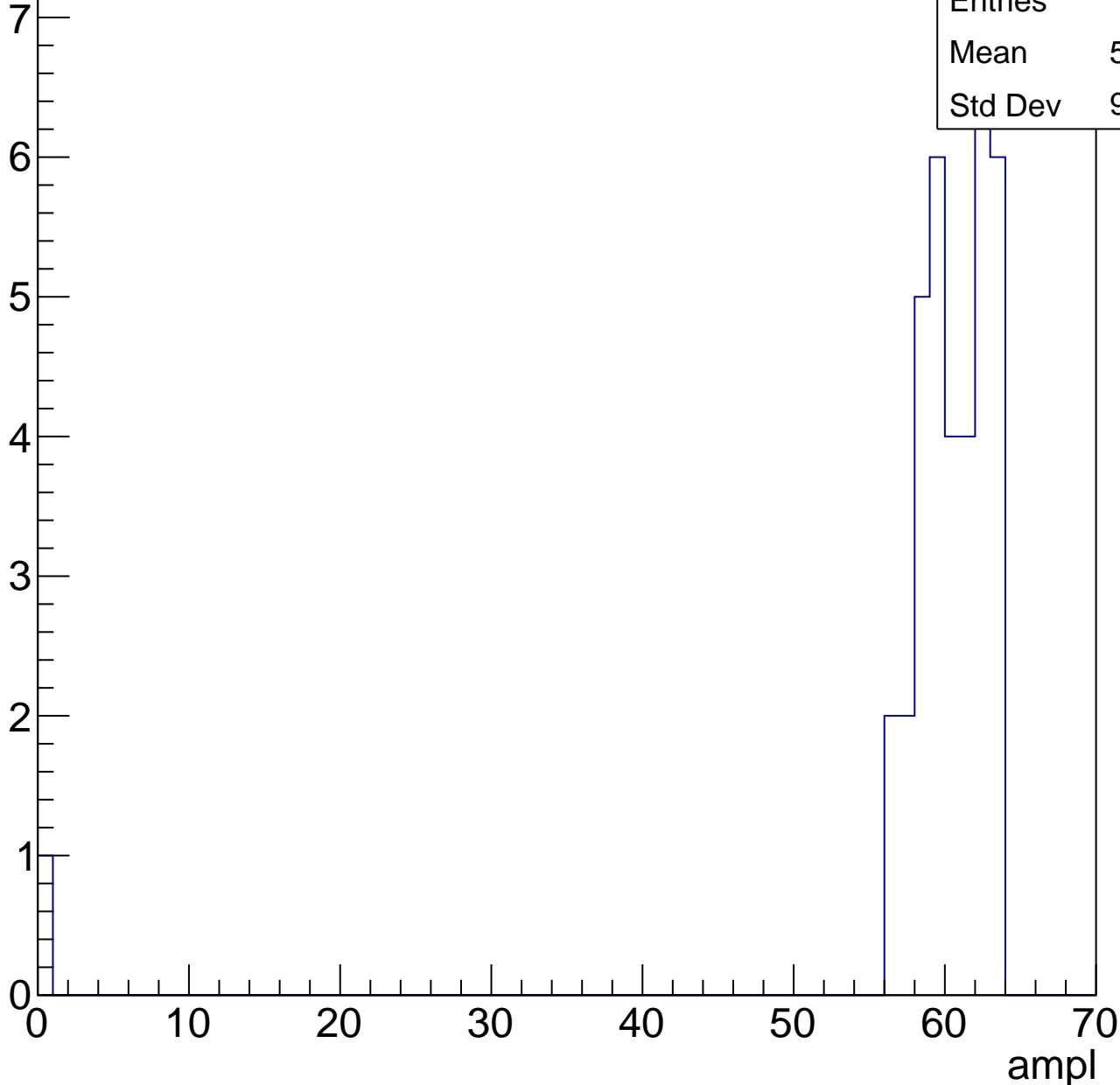


# B0L001S, U17-ch91, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

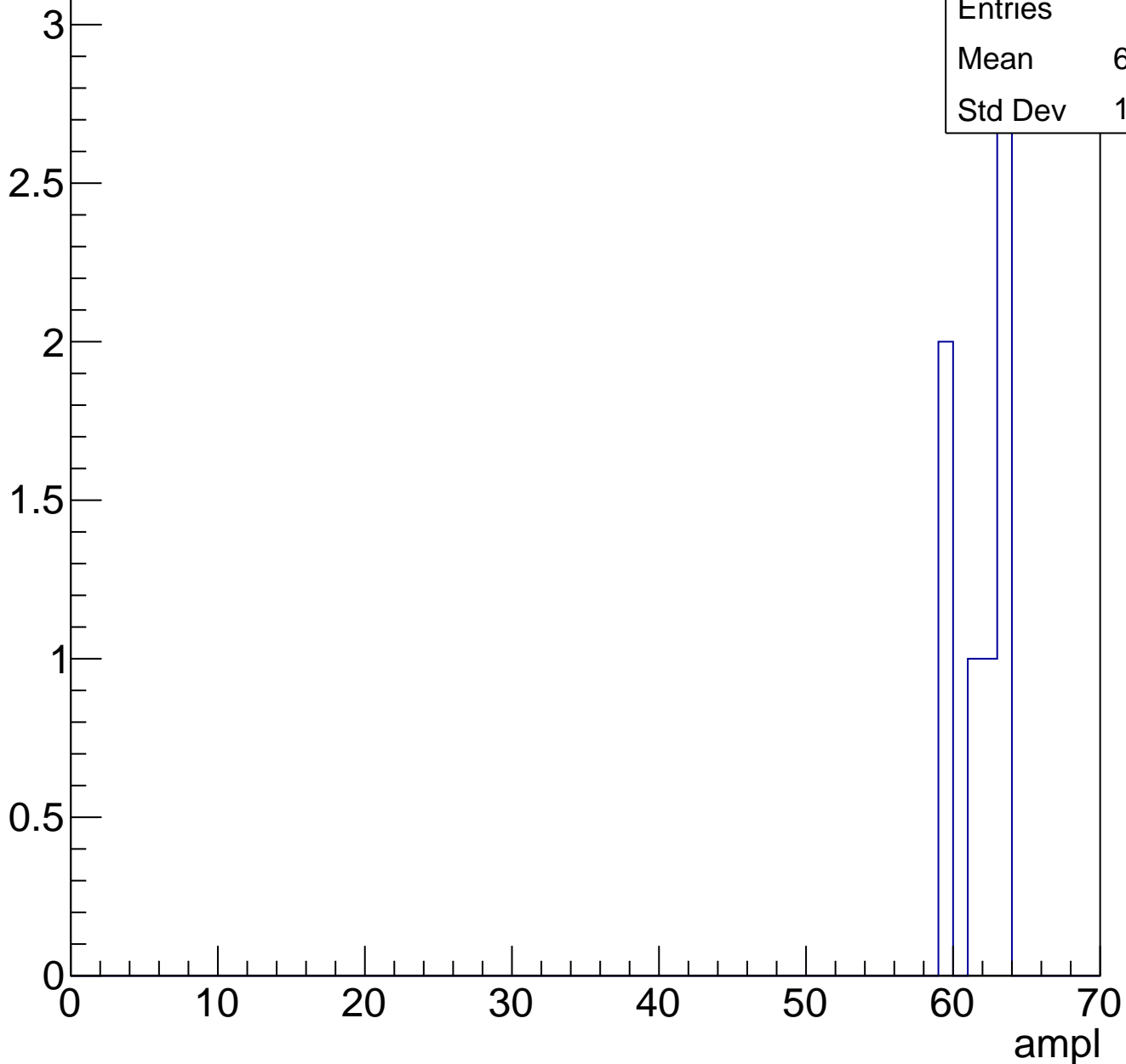
Entries	37
Mean	58.54
Std Dev	9.977



# B0L001S, U17-ch91, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch91, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U17-ch92, adc0

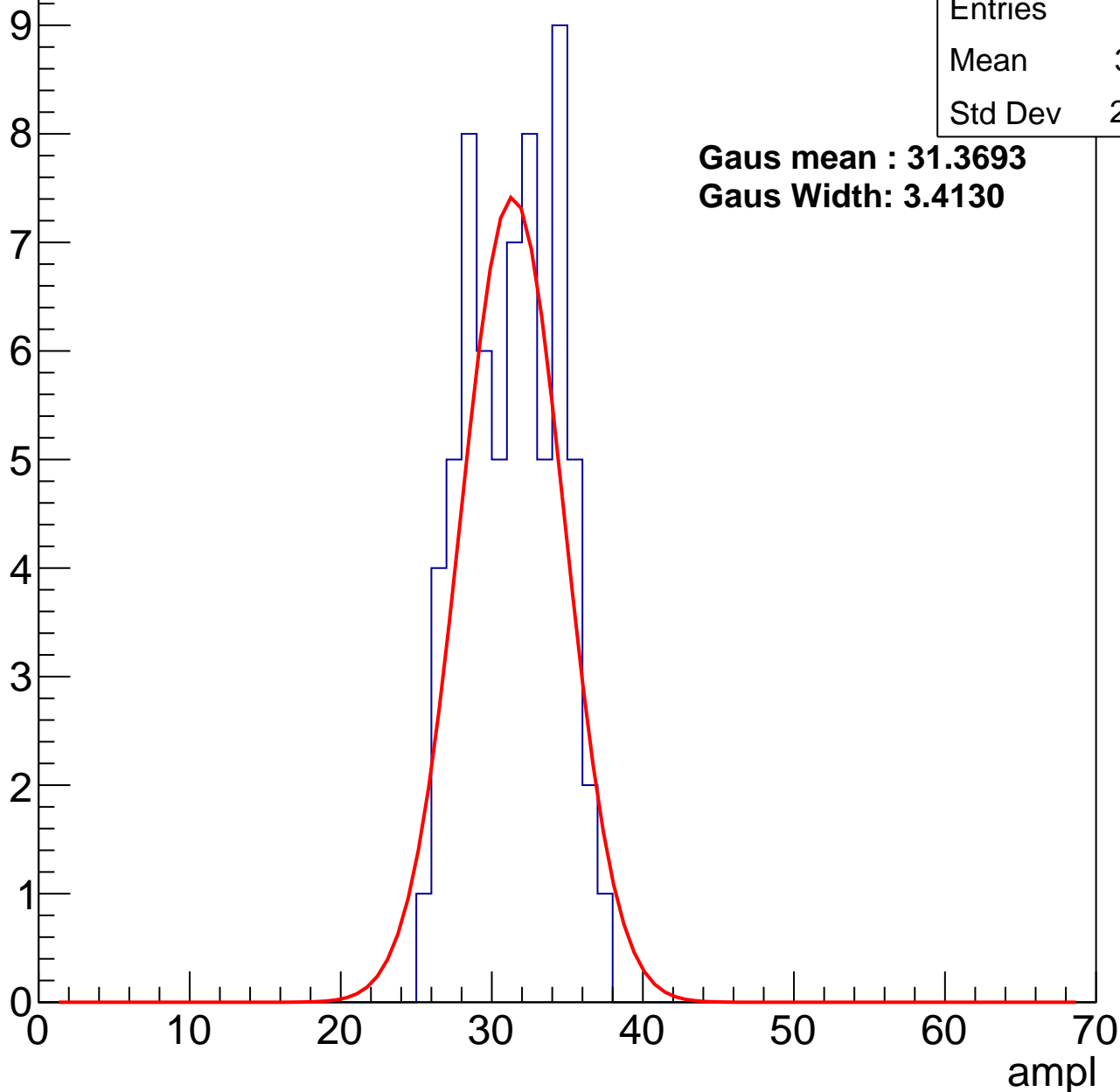
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	30.91
Std Dev	2.994

**Gaus mean : 31.3693**

**Gaus Width: 3.4130**



# B0L001S, U17-ch92, adc1

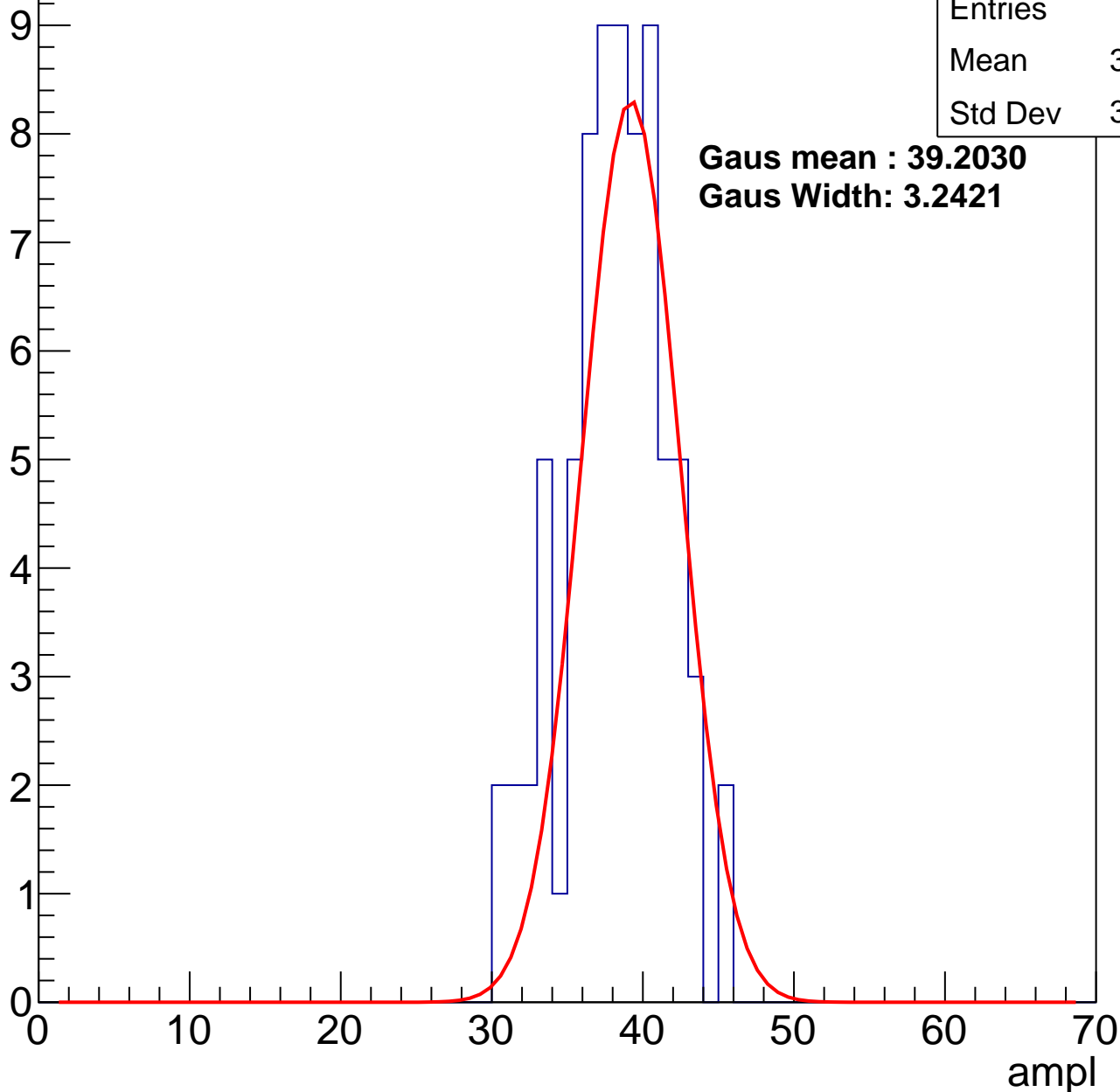
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	75
Mean	37.72
Std Dev	3.388

**Gaus mean : 39.2030**

**Gaus Width: 3.2421**



# B0L001S, U17-ch92, adc2

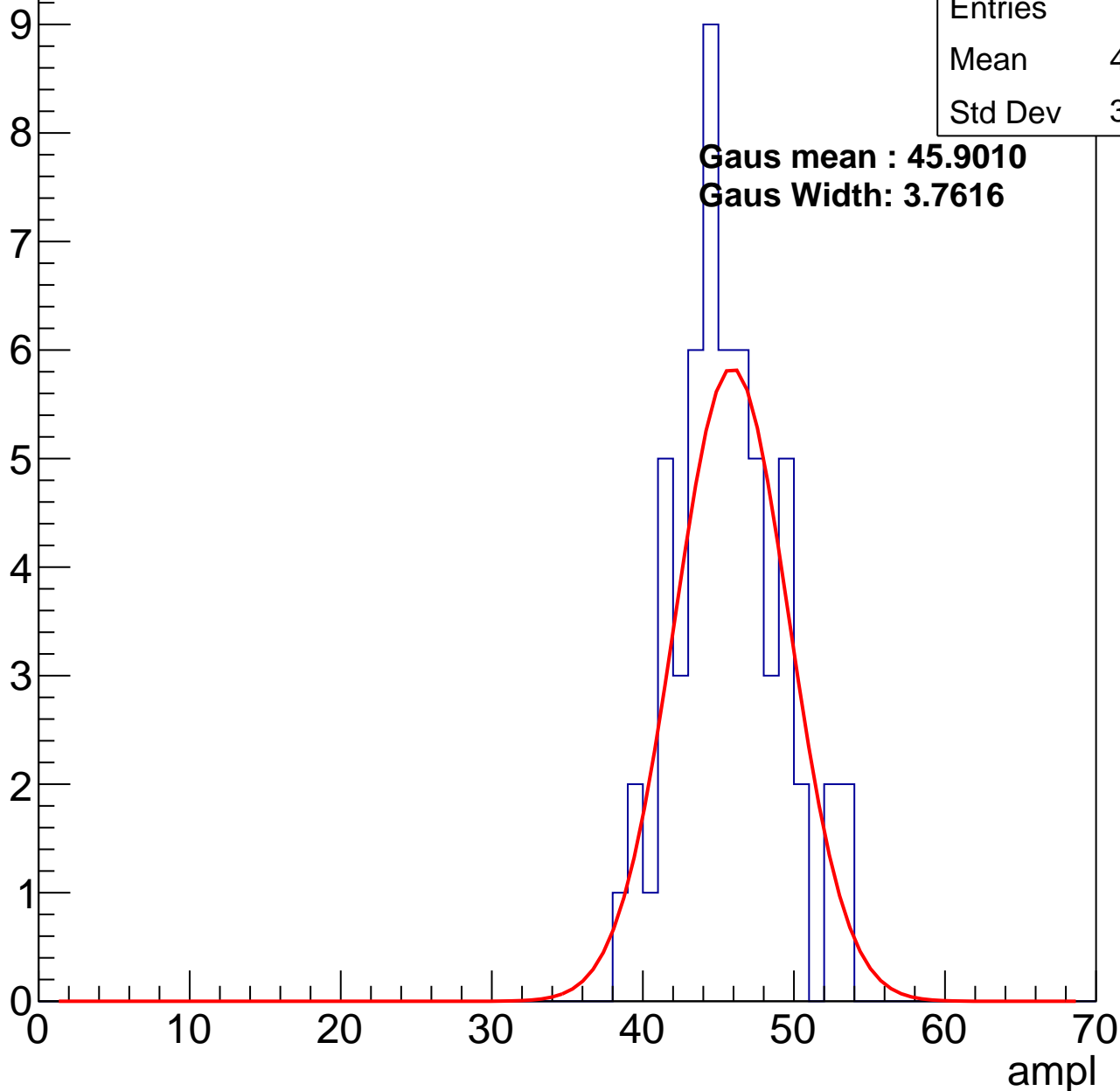
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	45.19
Std Dev	3.456

**Gaus mean : 45.9010**

**Gaus Width: 3.7616**

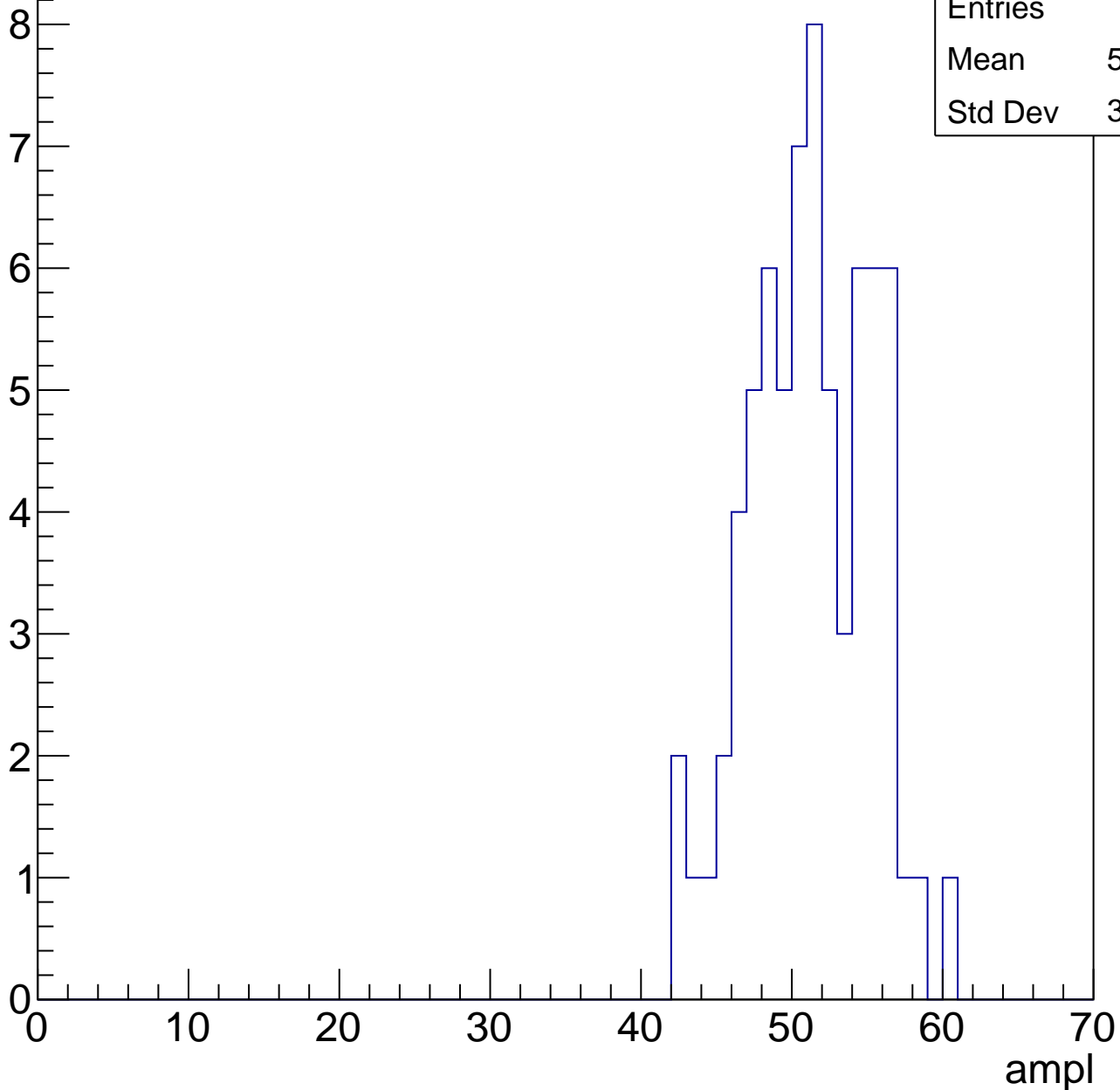


# B0L001S, U17-ch92, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	50.79
Std Dev	3.942

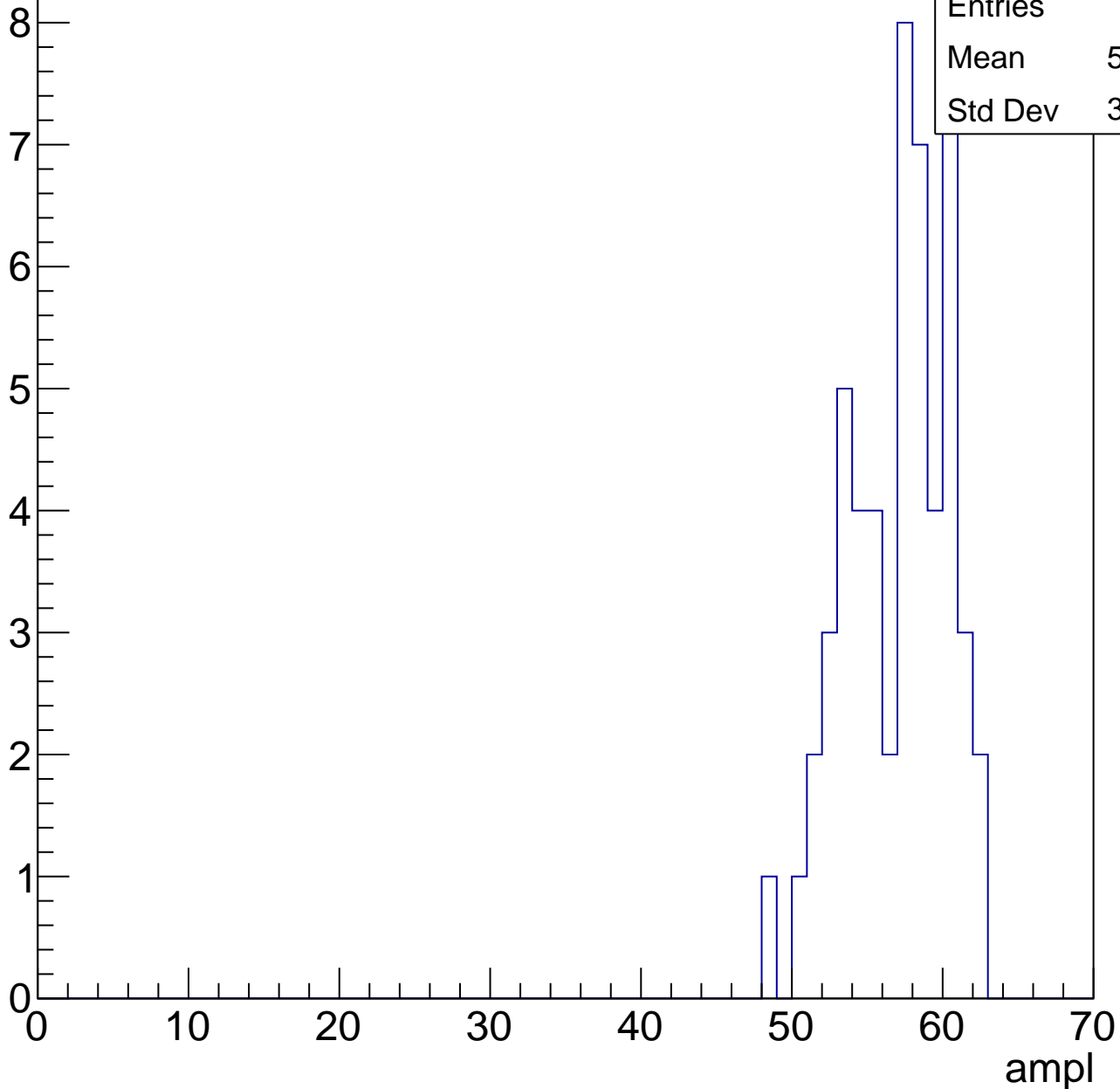


# B0L001S, U17-ch92, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	56.56
Std Dev	3.315

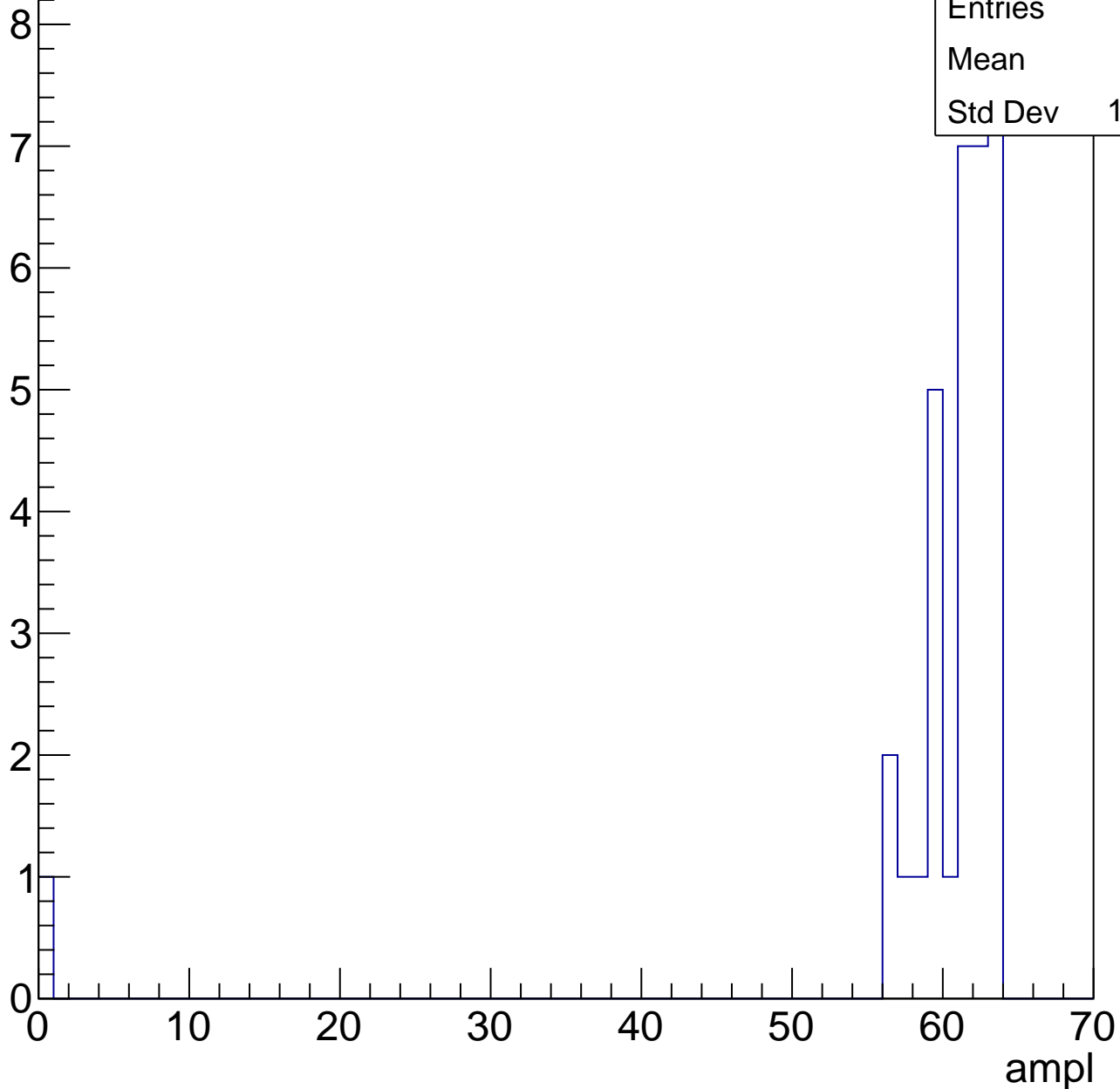


# B0L001S, U17-ch92, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	33
Mean	59
Std Dev	10.62



# B0L001S, U17-ch92, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

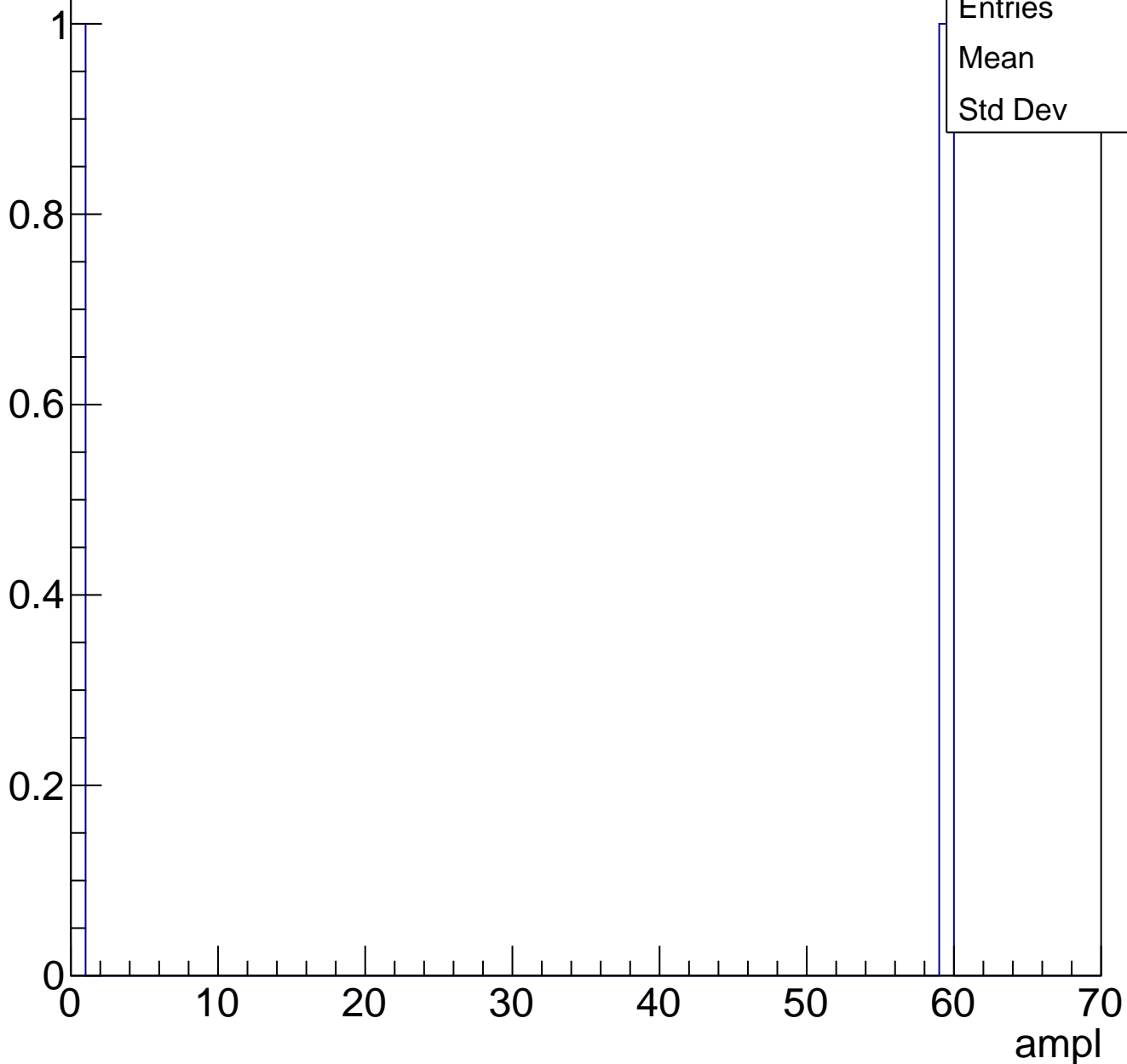




# B0L001S, U17-ch92, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U17-ch93, adc0

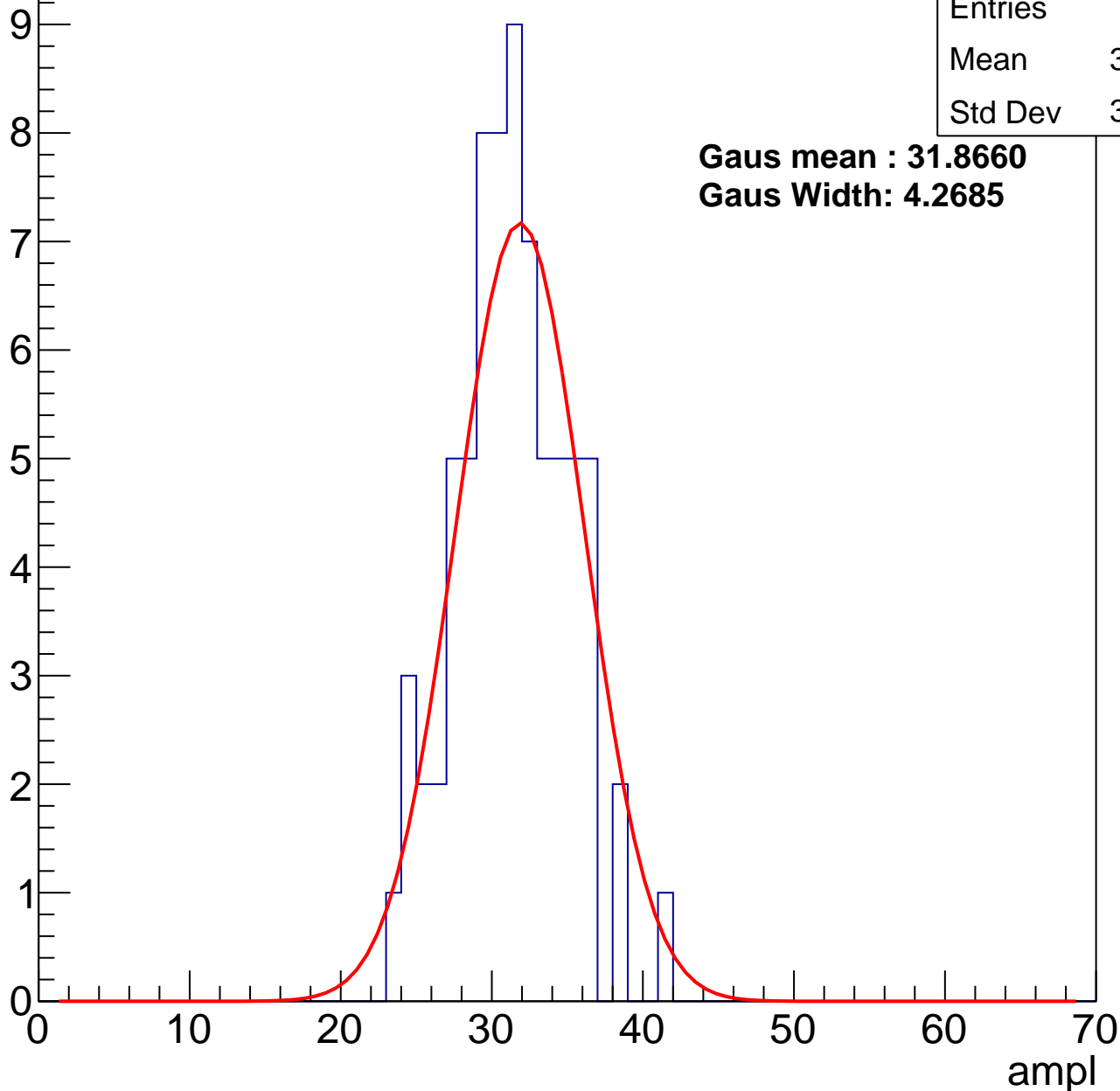
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	30.88
Std Dev	3.649

**Gaus mean : 31.8660**

**Gaus Width: 4.2685**



# B0L001S, U17-ch93, adc1

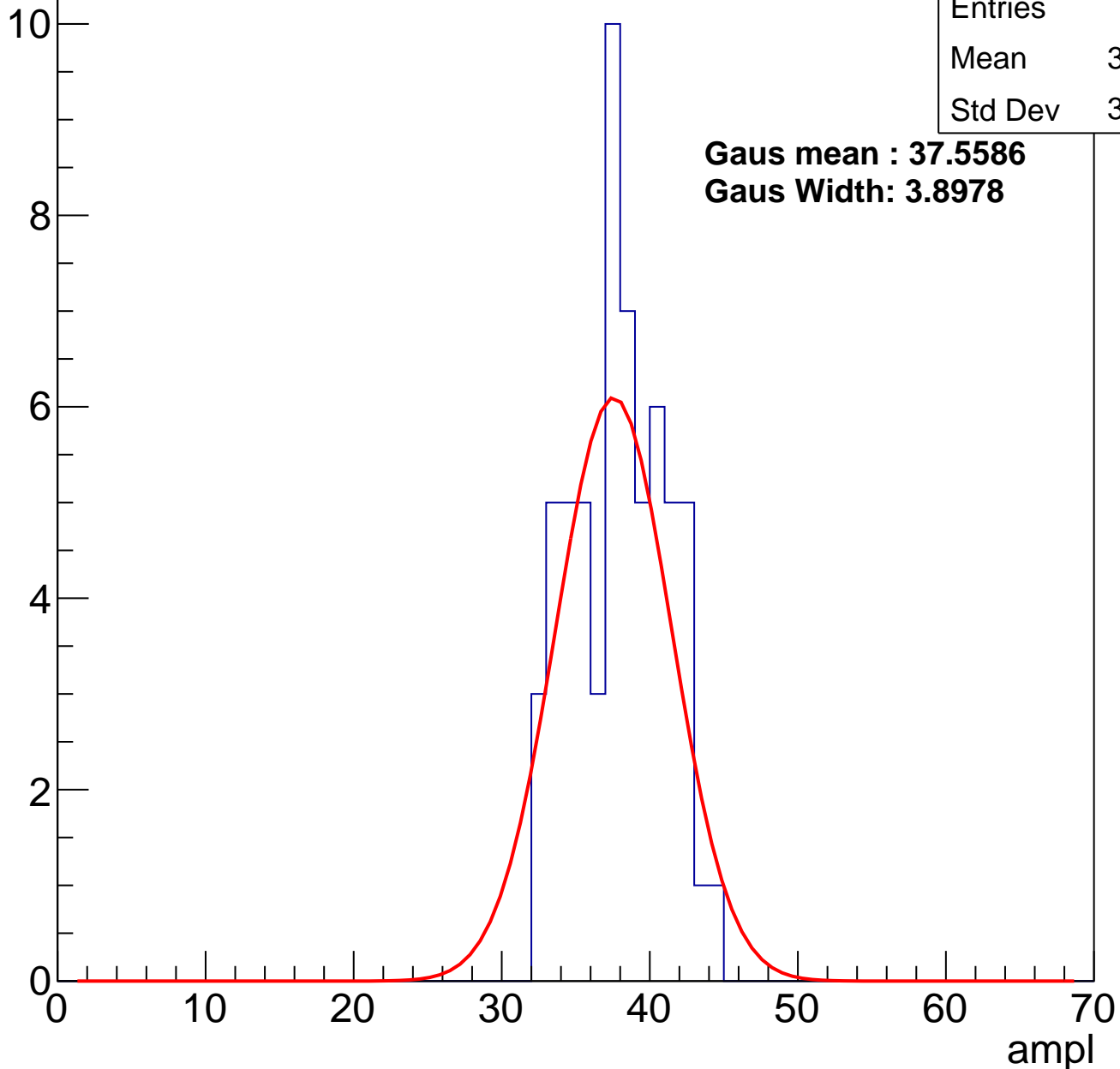
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	61
Mean	37.49
Std Dev	3.082

**Gaus mean : 37.5586**

**Gaus Width: 3.8978**

Entry



# B0L001S, U17-ch93, adc2

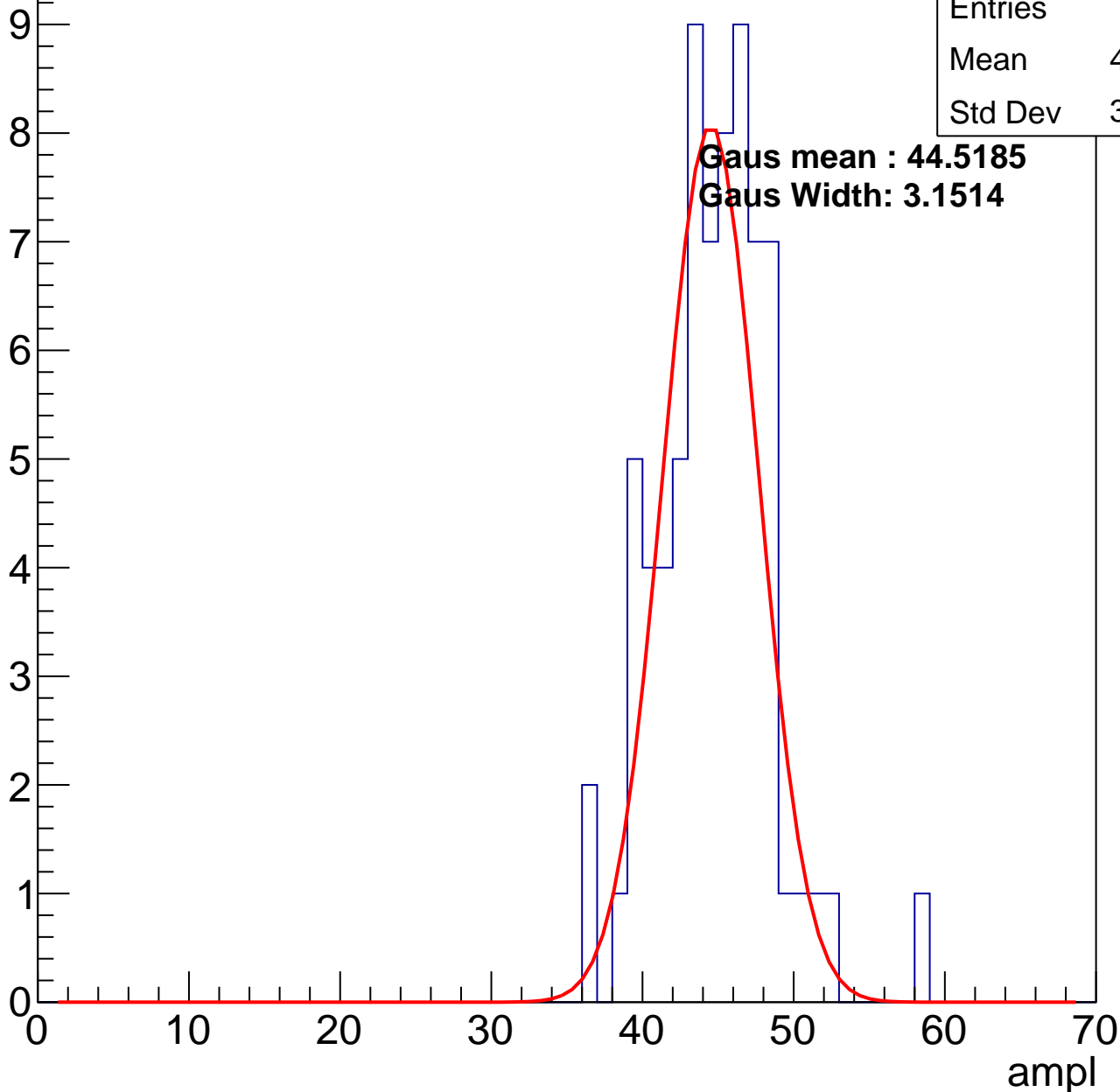
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	44.29
Std Dev	3.703

**Gaus mean : 44.5185**

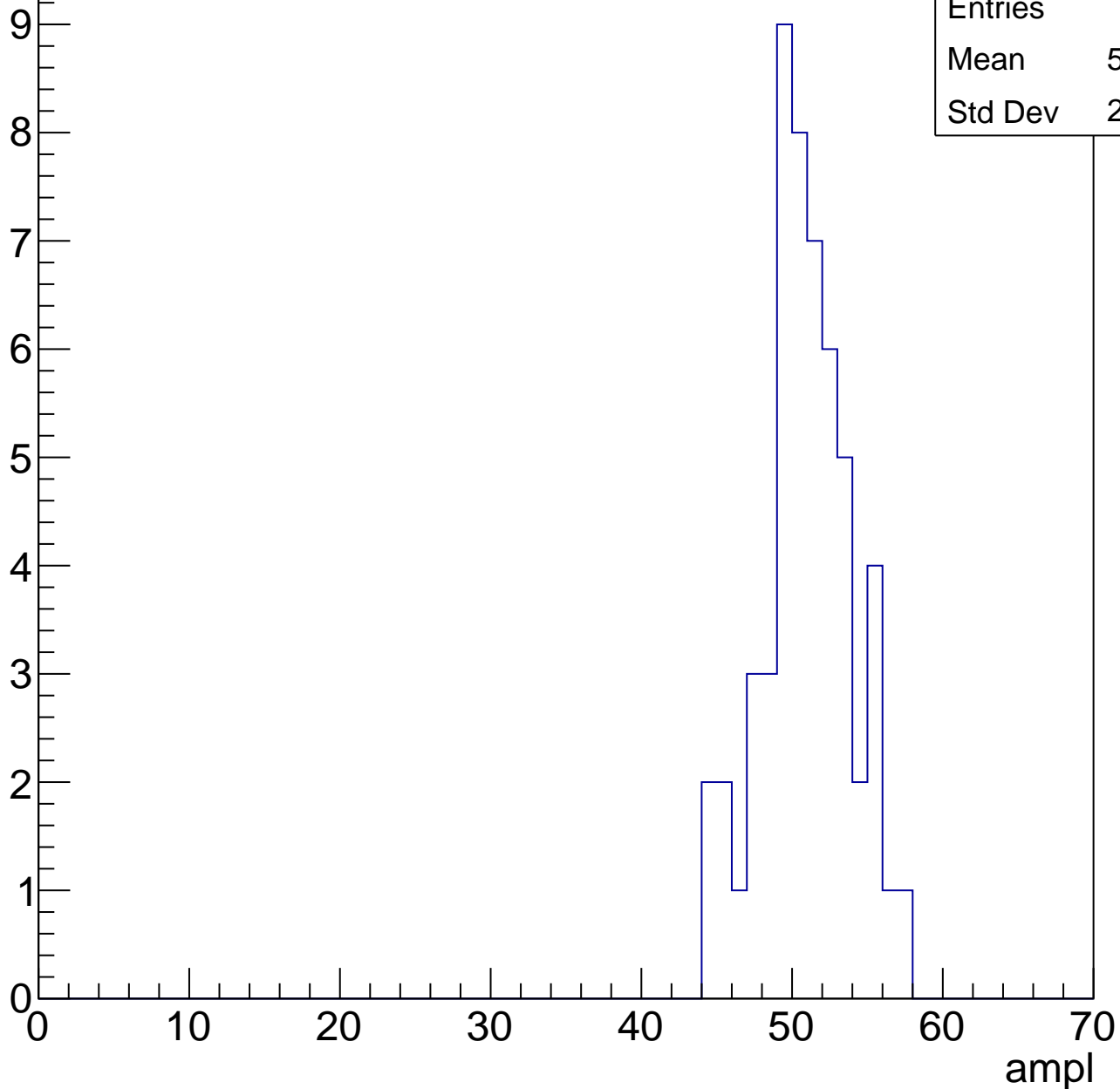
**Gaus Width: 3.1514**



# B0L001S, U17-ch93, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

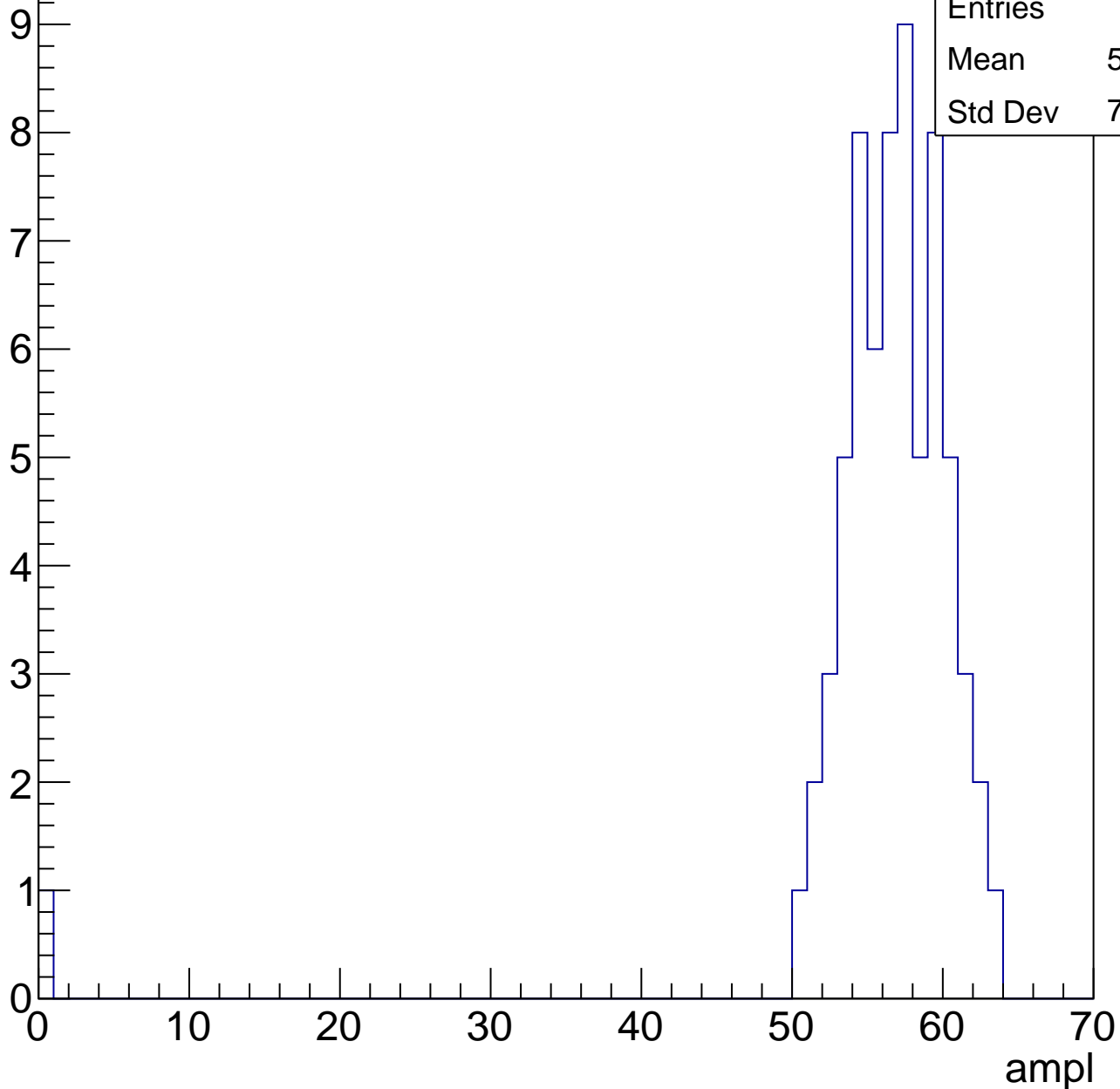


Entries	54
Mean	50.46
Std Dev	2.942

# B0L001S, U17-ch93, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

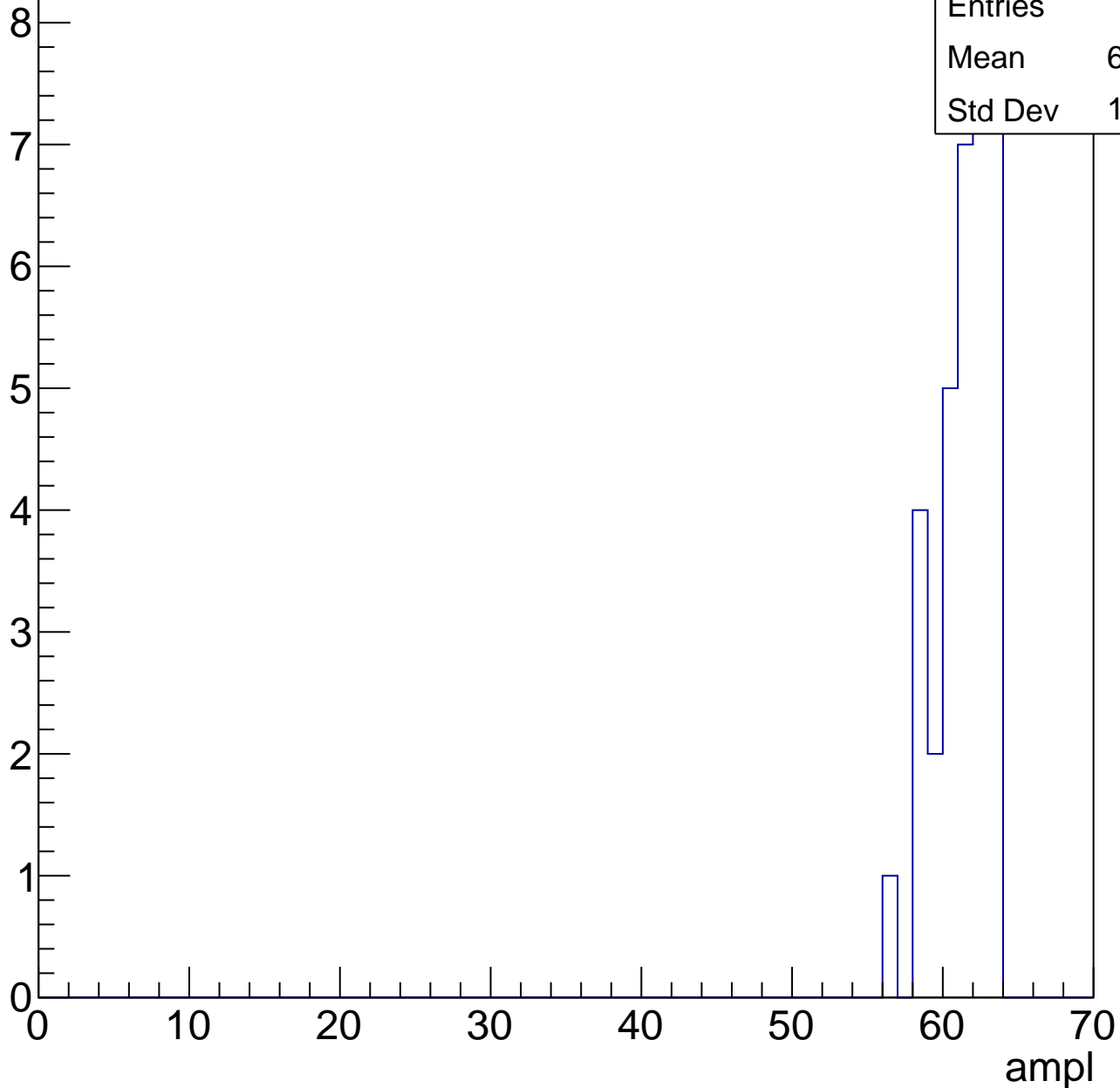


# B0L001S, U17-ch93, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	35
Mean	60.94
Std Dev	1.804



# B0L001S, U17-ch93, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch93, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U17-ch94, adc0

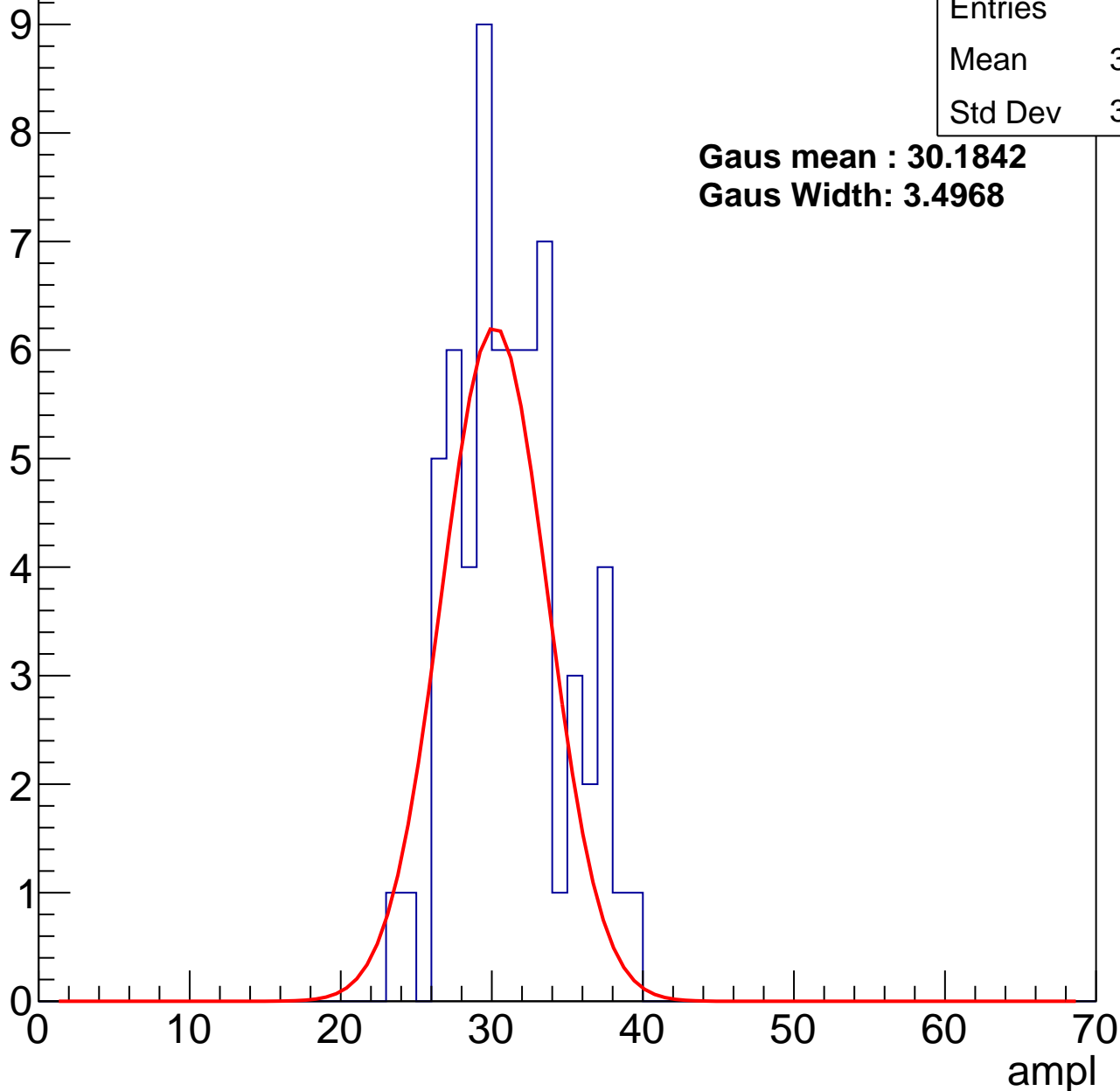
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	30.75
Std Dev	3.577

**Gaus mean : 30.1842**

**Gaus Width: 3.4968**



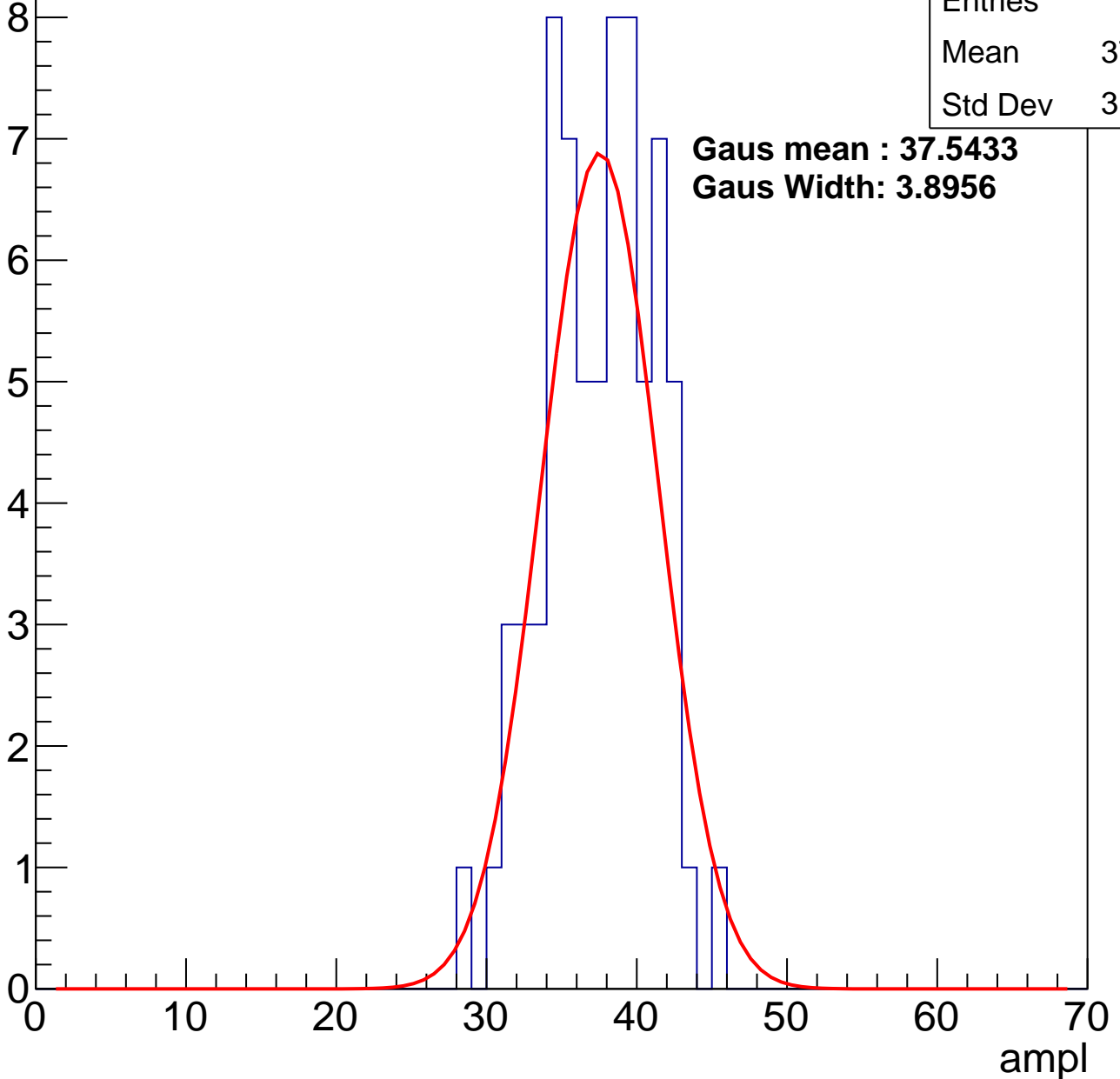
# B0L001S, U17-ch94, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	37.03
Std Dev	3.536

**Gaus mean : 37.5433**  
**Gaus Width: 3.8956**



# B0L001S, U17-ch94, adc2

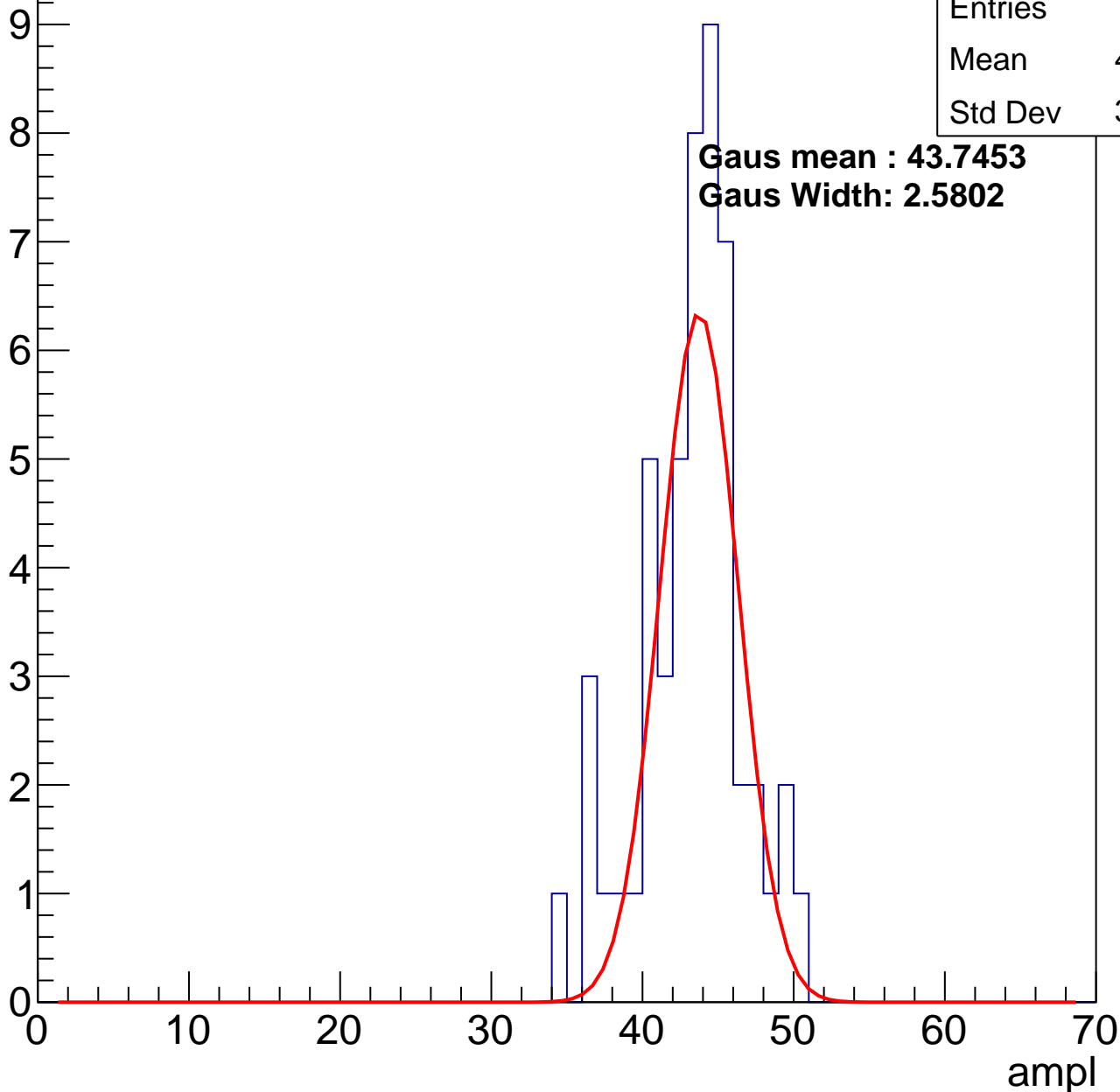
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	42.81
Std Dev	3.391

**Gaus mean : 43.7453**

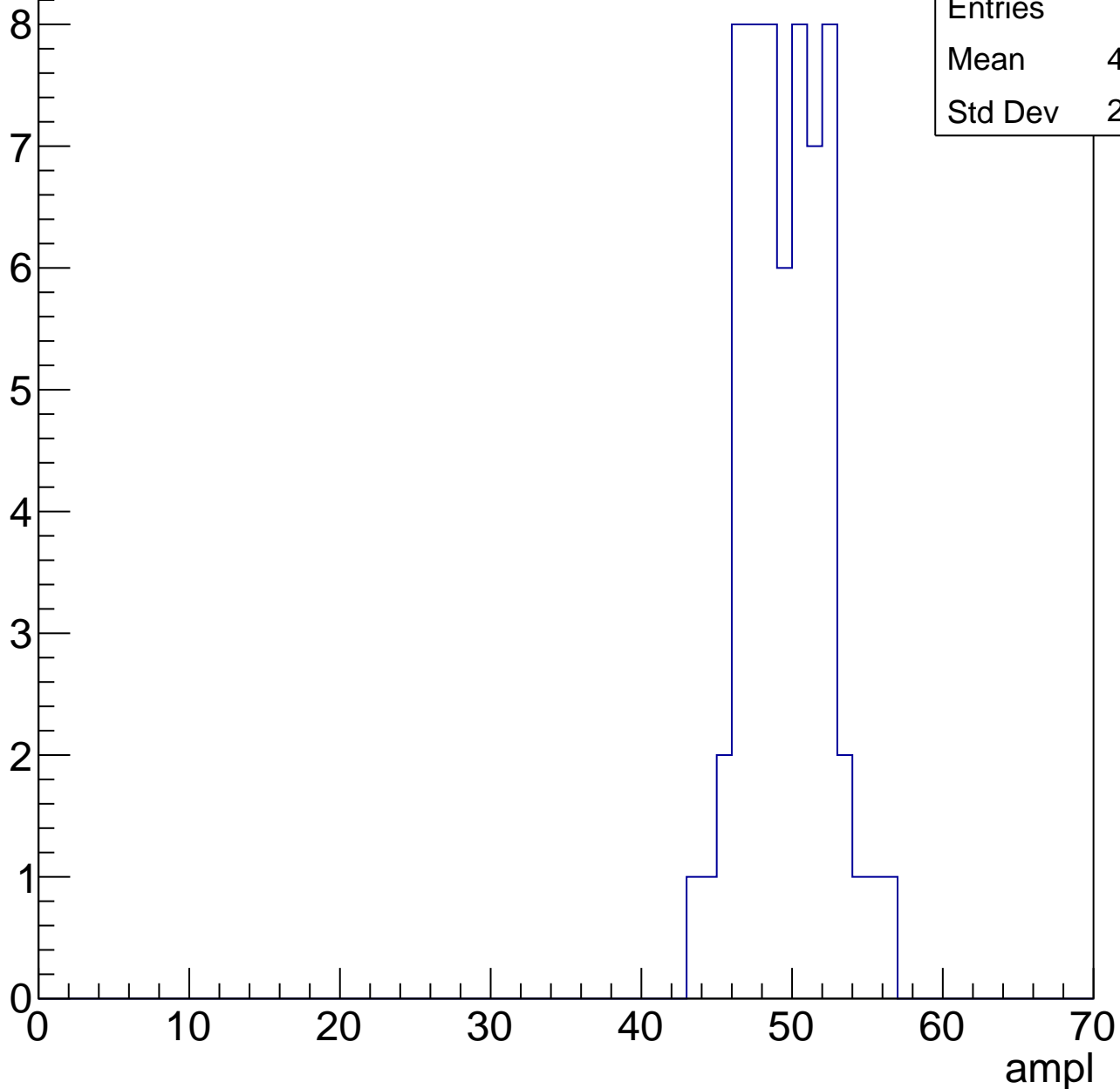
**Gaus Width: 2.5802**



# B0L001S, U17-ch94, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



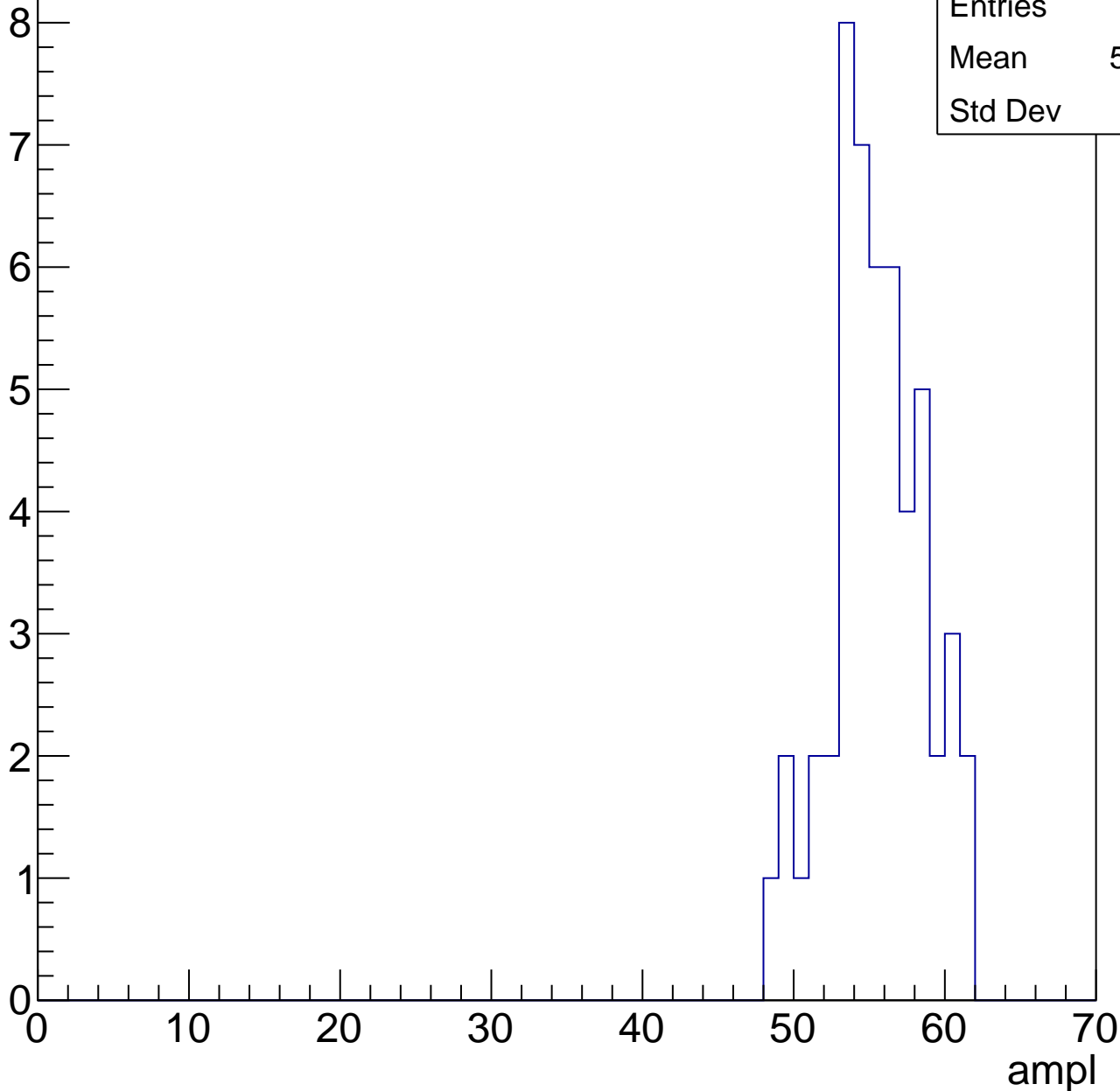
Entries	62
Mean	49.08
Std Dev	2.708

# B0L001S, U17-ch94, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	51
Mean	55.06
Std Dev	3.07

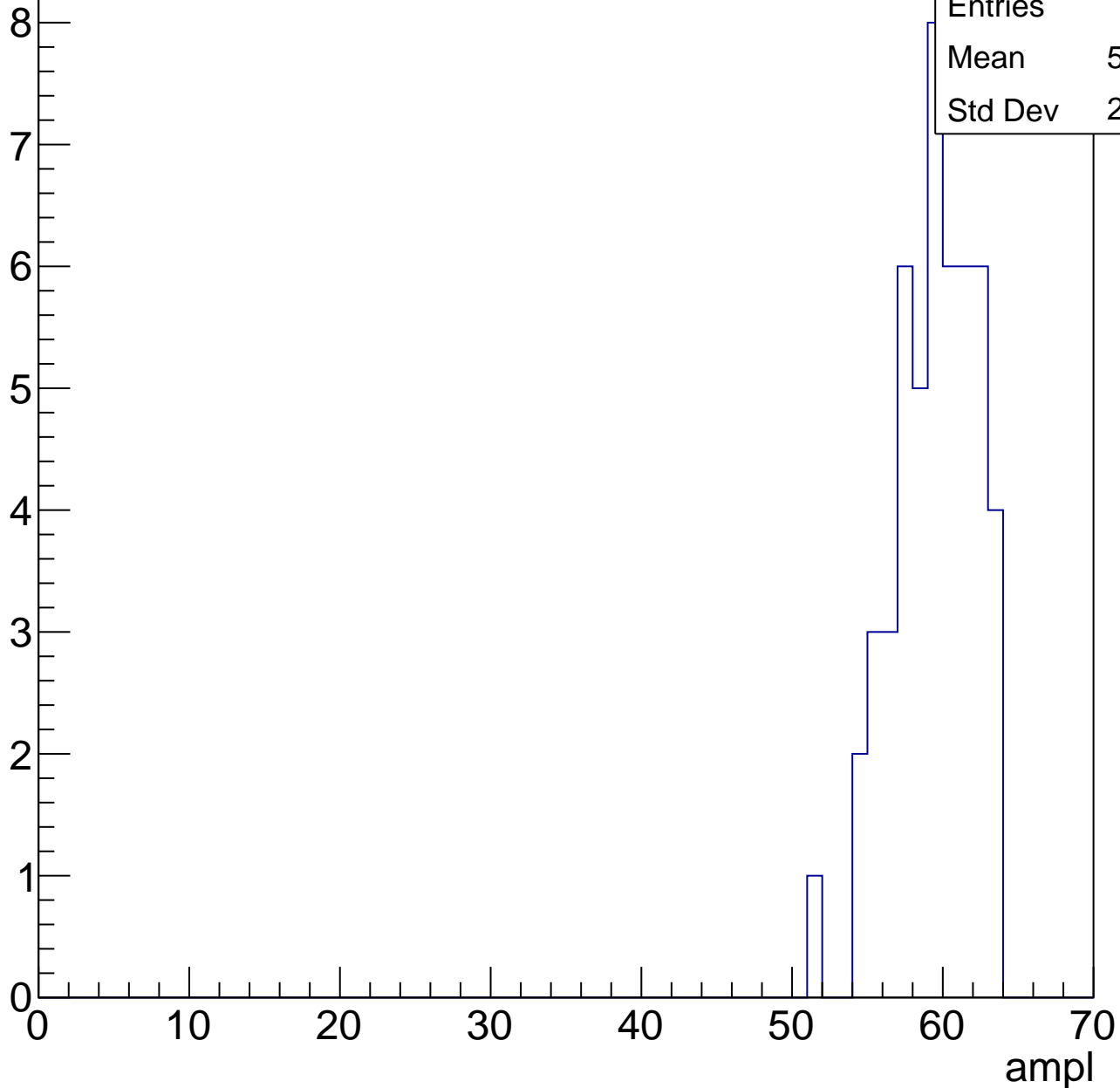


# B0L001S, U17-ch94, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	50
Mean	58.92
Std Dev	2.704

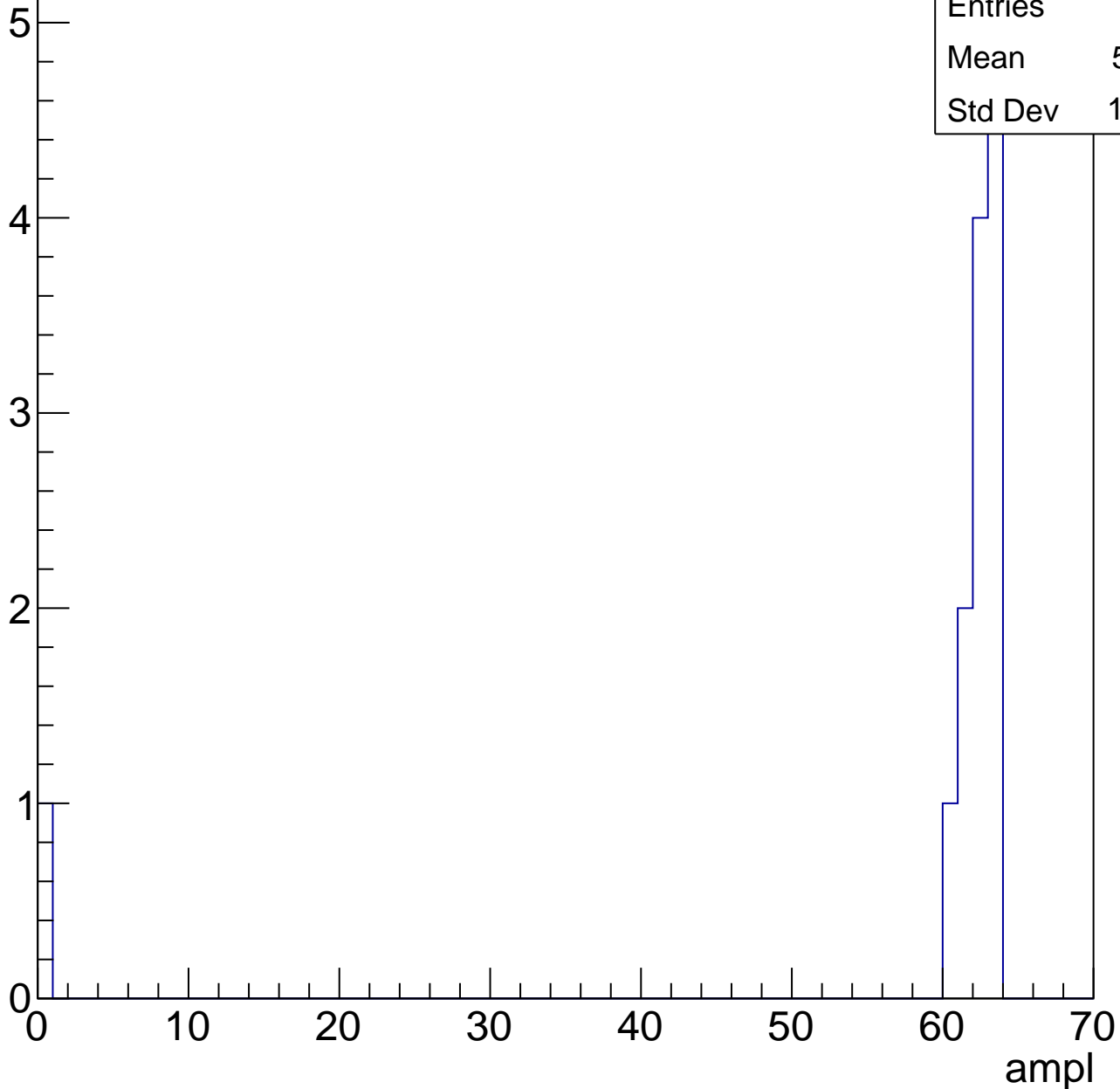


# B0L001S, U17-ch94, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	13
Mean	57.31
Std Dev	16.57

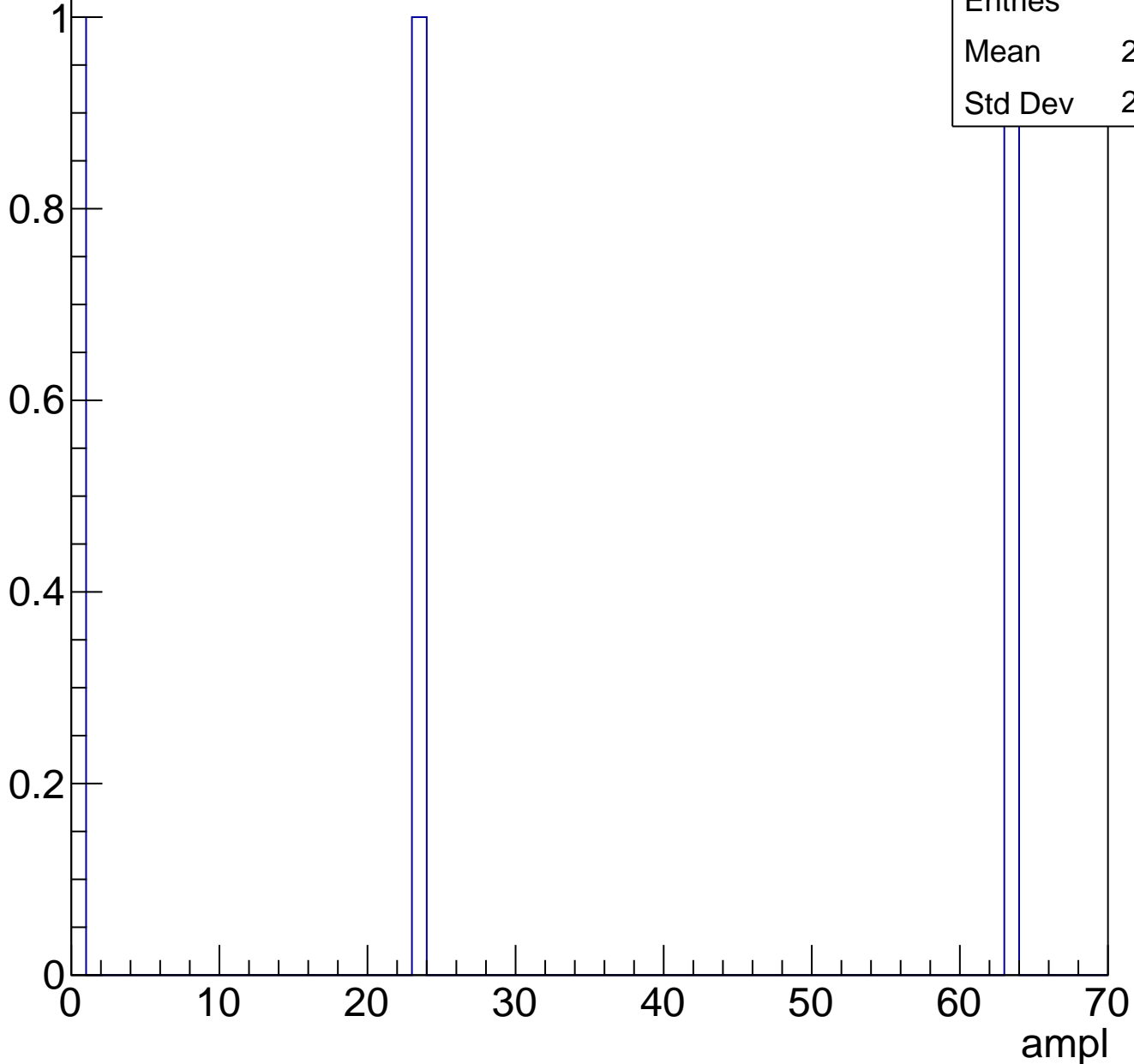




# B0L001S, U17-ch94, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	3
Mean	28.67
Std Dev	26.03

# B0L001S, U17-ch95, adc0

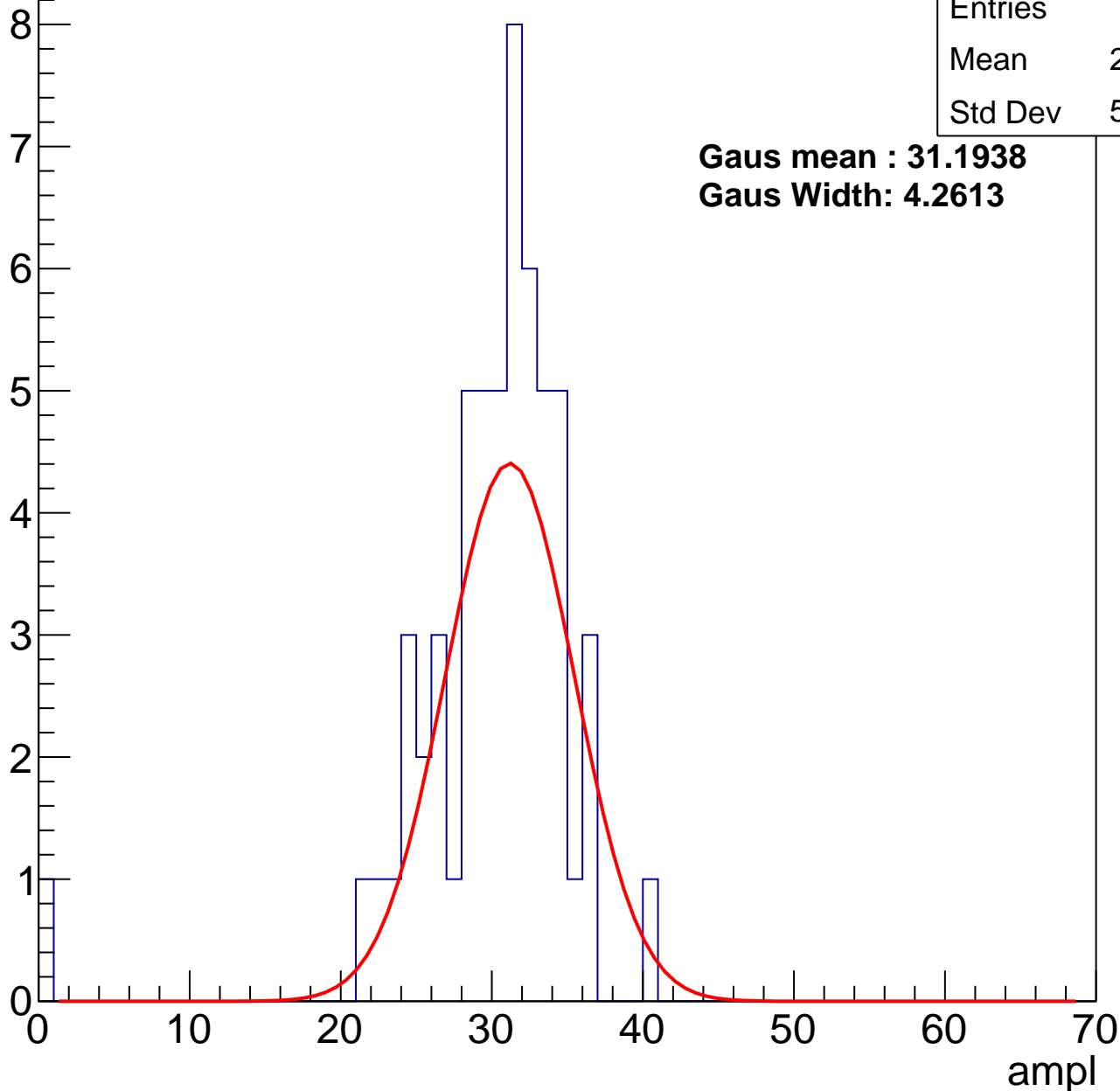
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	29.58
Std Dev	5.483

**Gaus mean : 31.1938**

**Gaus Width: 4.2613**



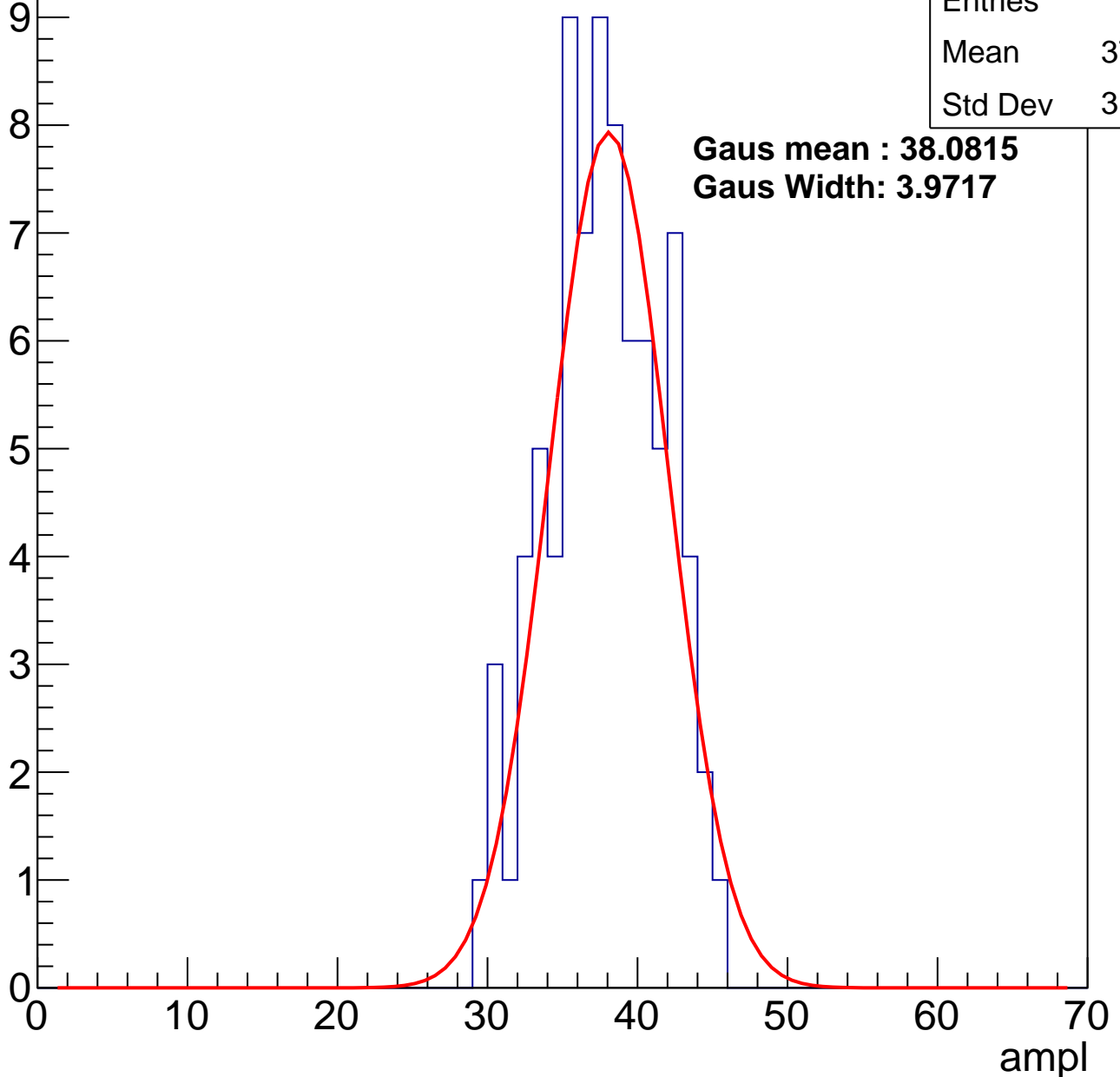
# B0L001S, U17-ch95, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	82
Mean	37.33
Std Dev	3.735

**Gaus mean : 38.0815**  
**Gaus Width: 3.9717**



# B0L001S, U17-ch95, adc2

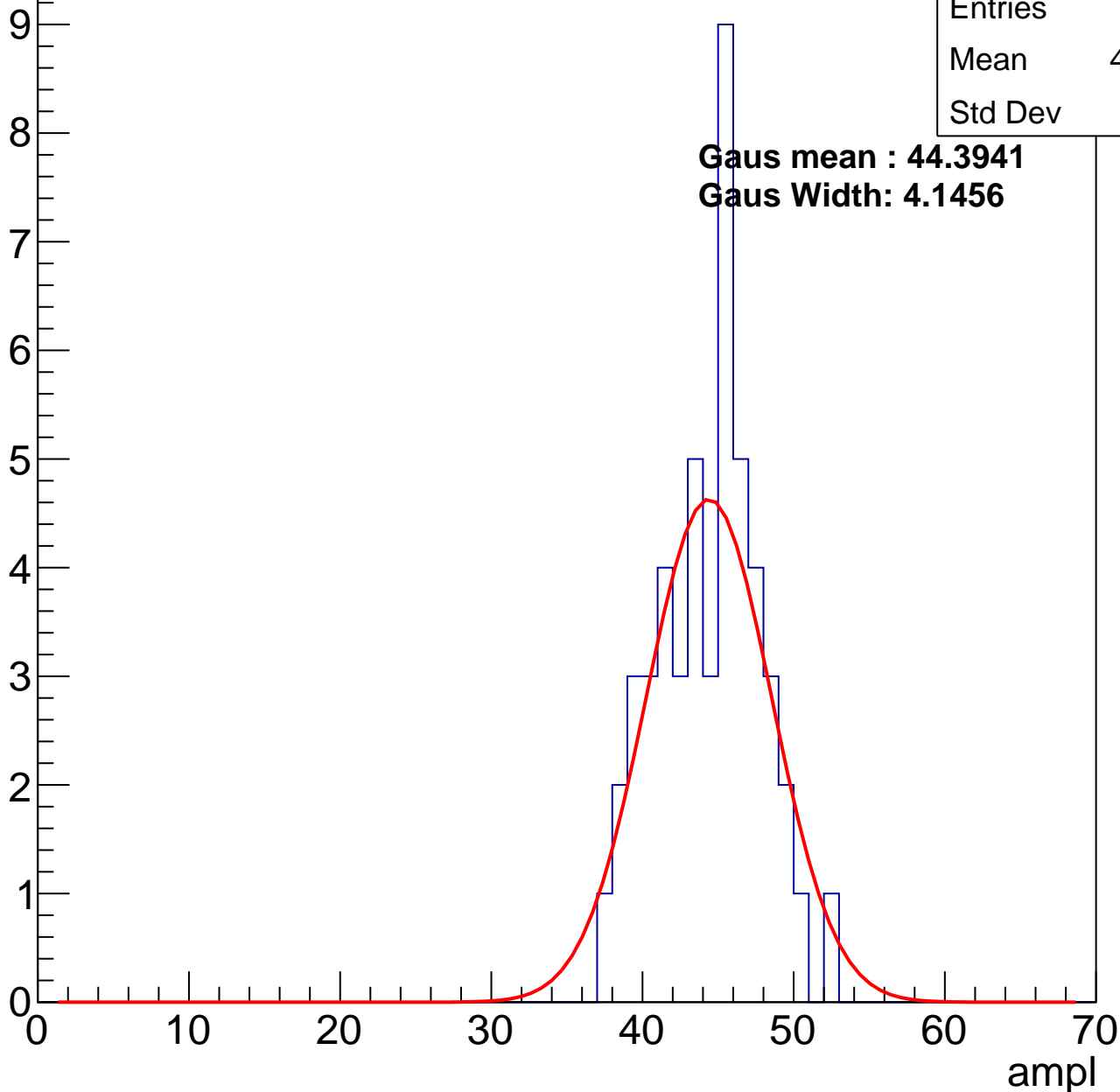
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	49
Mean	43.96
Std Dev	3.38

**Gaus mean : 44.3941**

**Gaus Width: 4.1456**

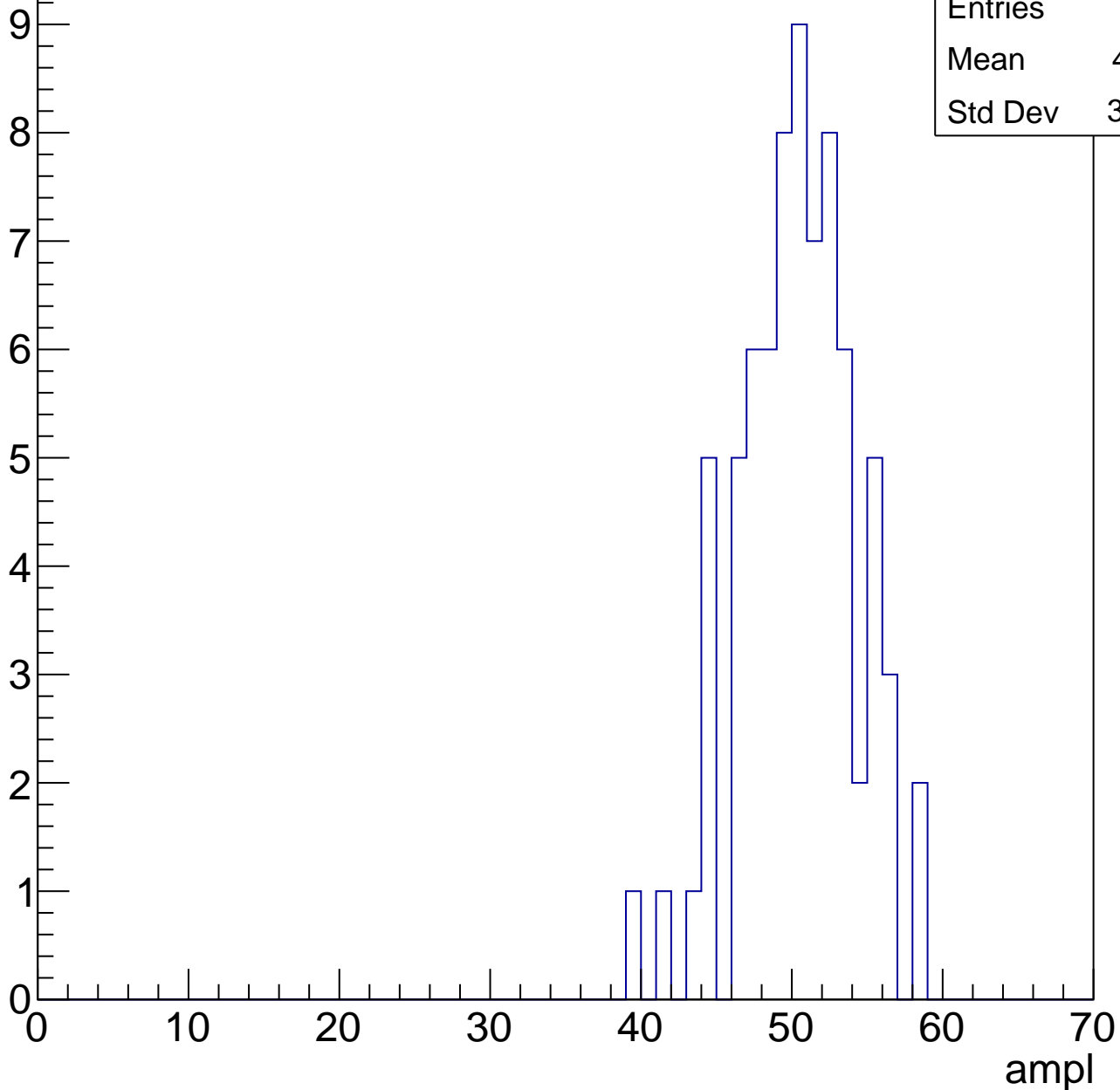


# B0L001S, U17-ch95, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

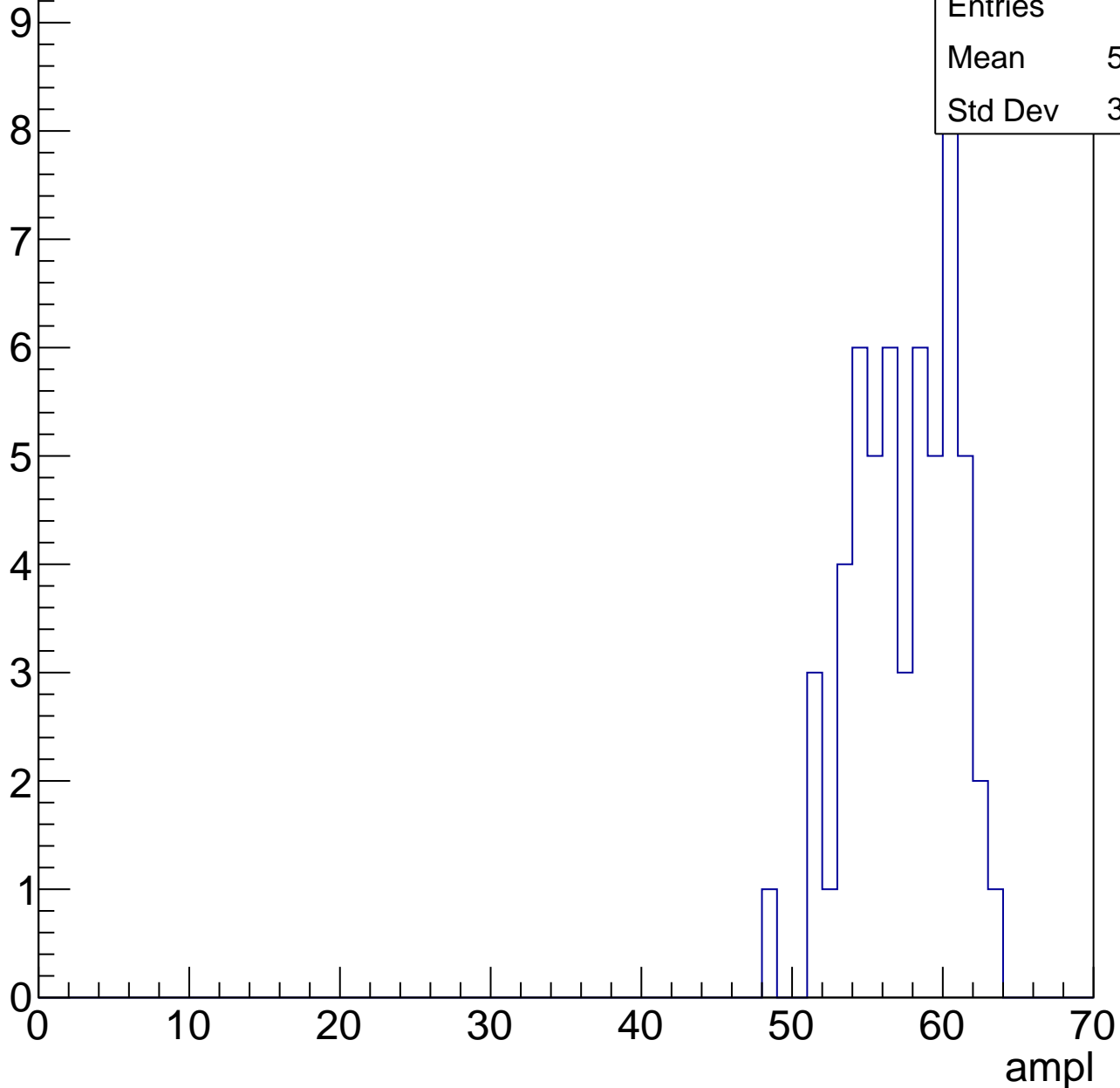
Entries	75
Mean	49.91
Std Dev	3.799



# B0L001S, U17-ch95, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

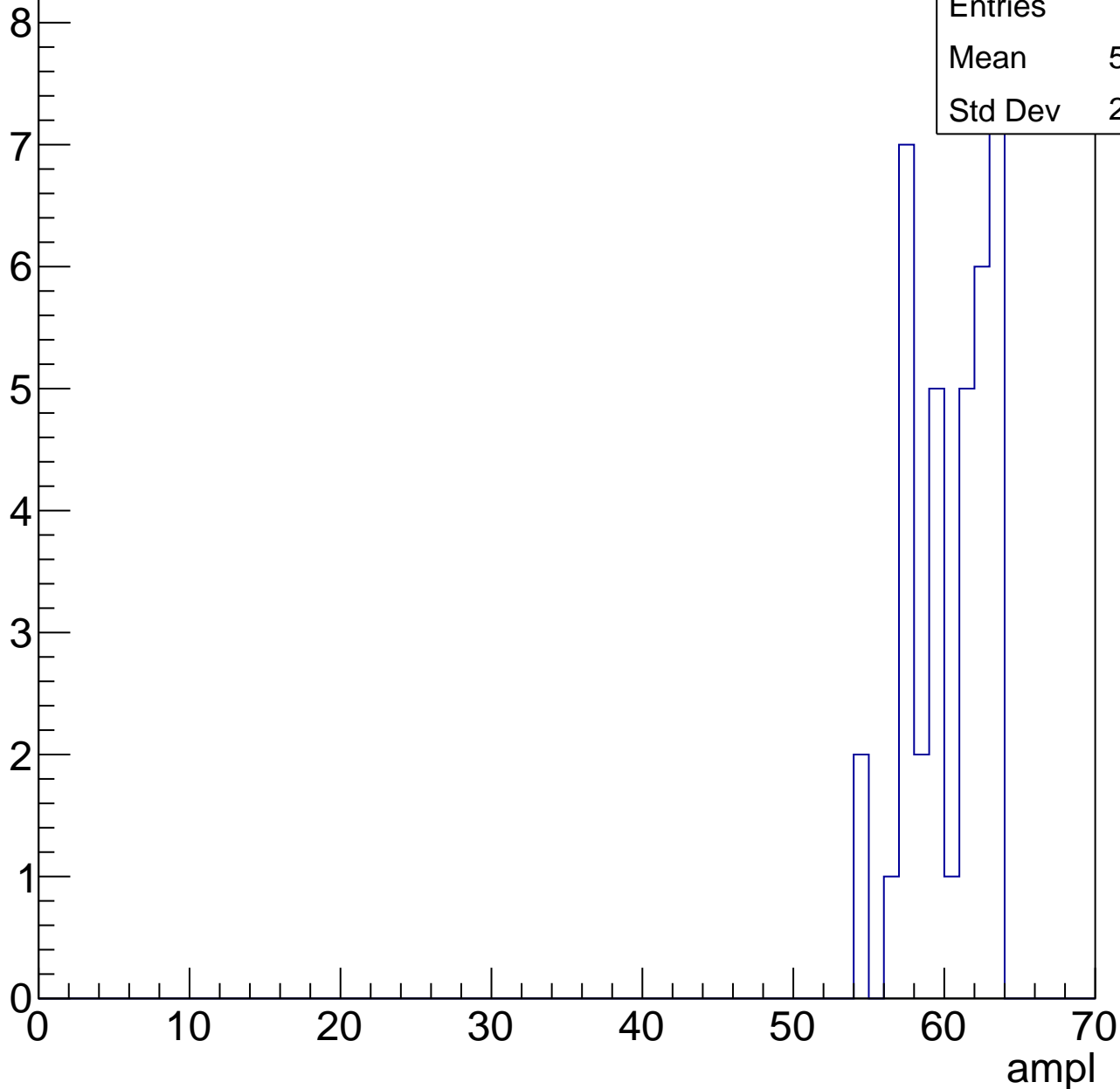


# B0L001S, U17-ch95, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

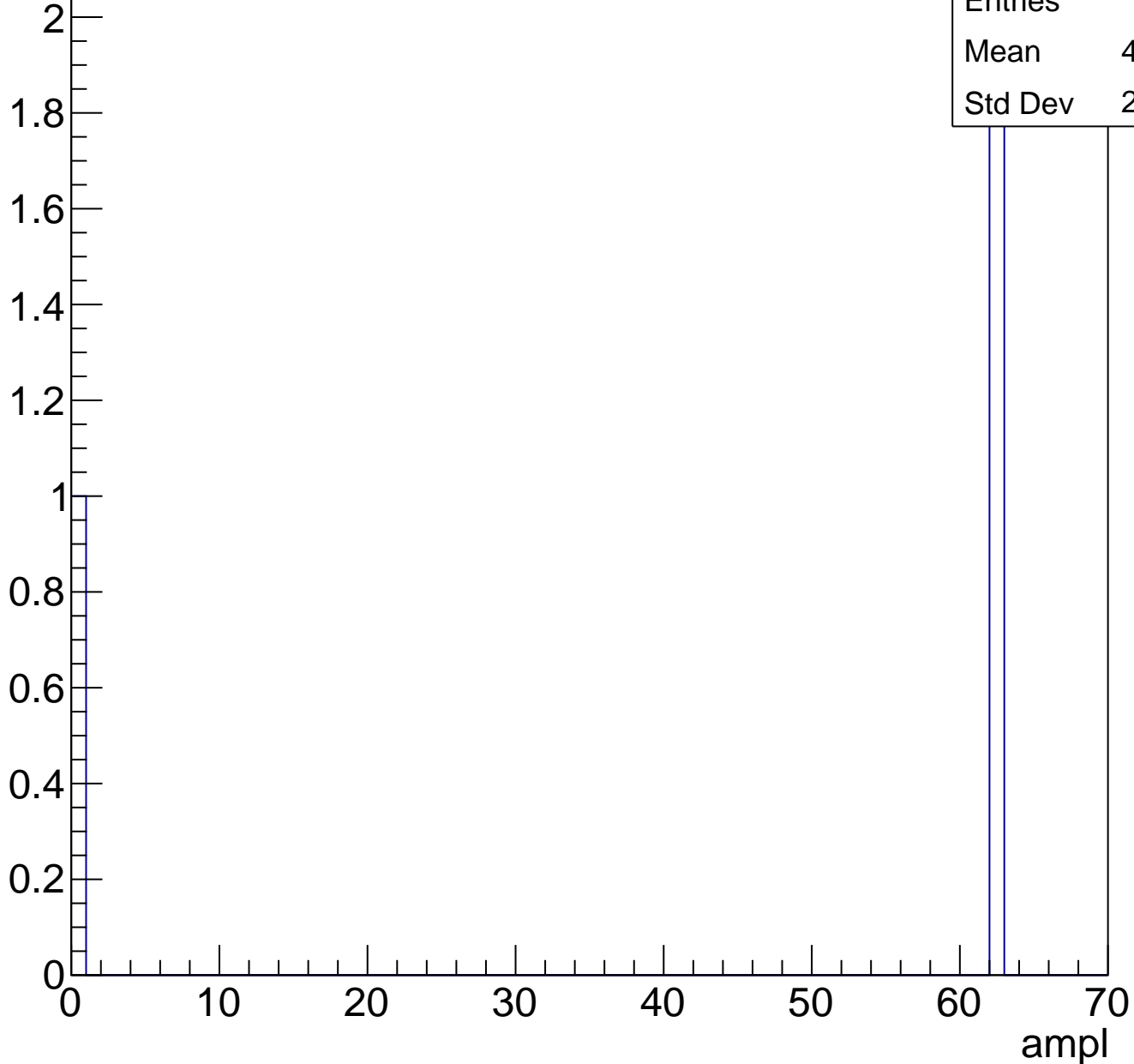
Entries	37
Mean	59.86
Std Dev	2.673



# B0L001S, U17-ch95, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch95, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U17-ch96, adc0

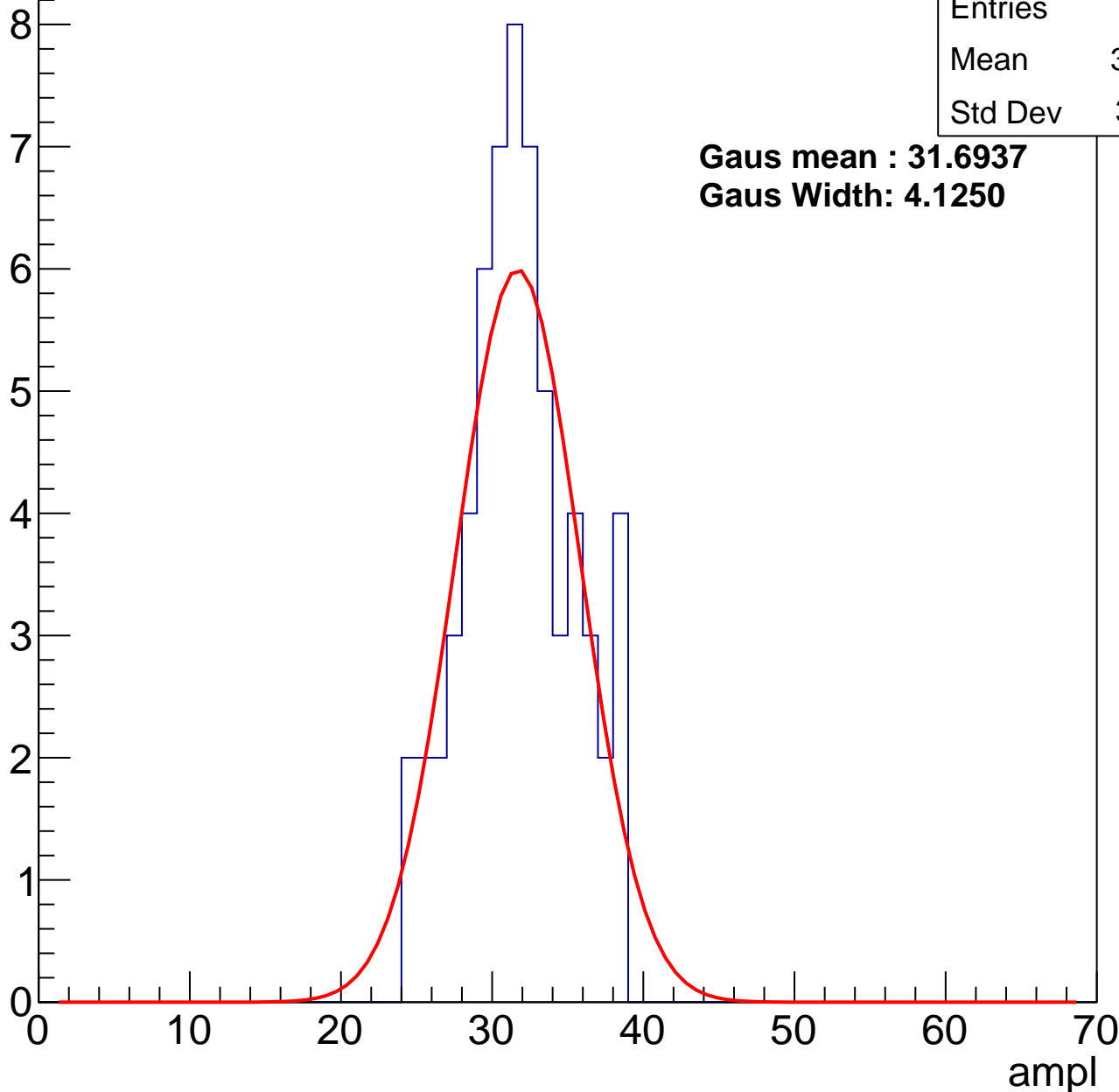
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	31.29
Std Dev	3.571

**Gaus mean : 31.6937**

**Gaus Width: 4.1250**



# B0L001S, U17-ch96, adc1

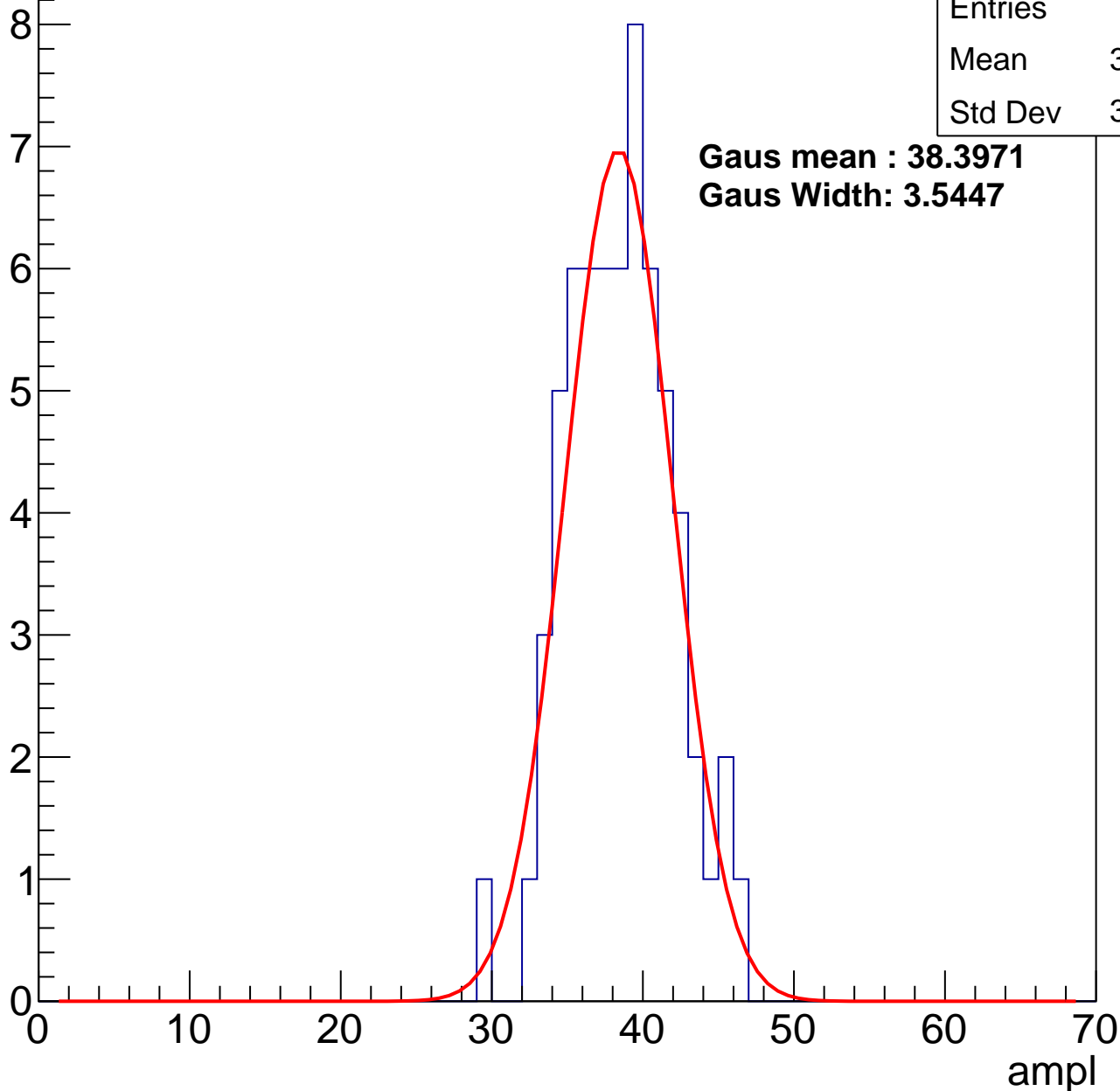
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	38.05
Std Dev	3.438

**Gaus mean : 38.3971**

**Gaus Width: 3.5447**



# B0L001S, U17-ch96, adc2

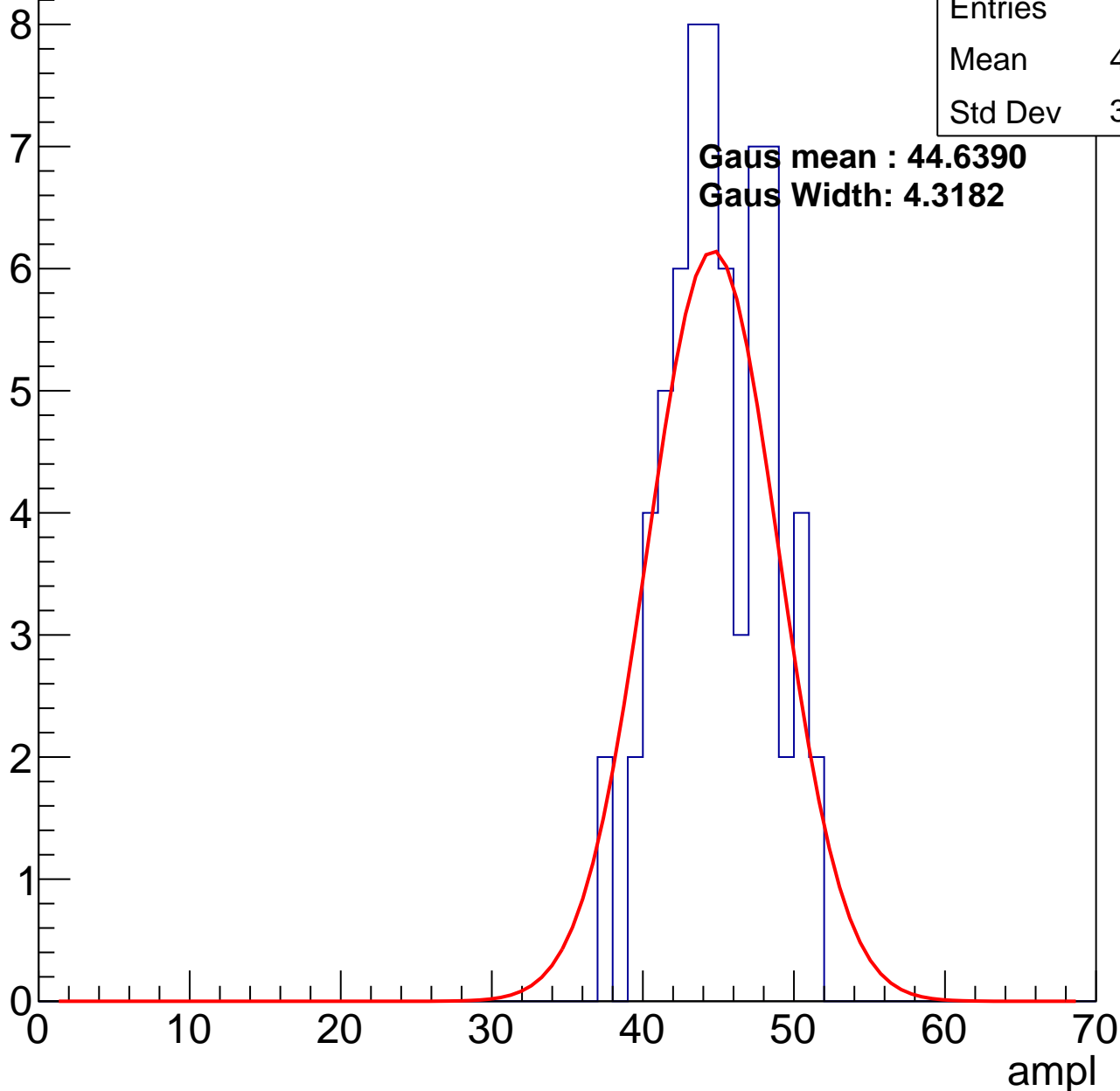
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	44.52
Std Dev	3.386

**Gaus mean : 44.6390**

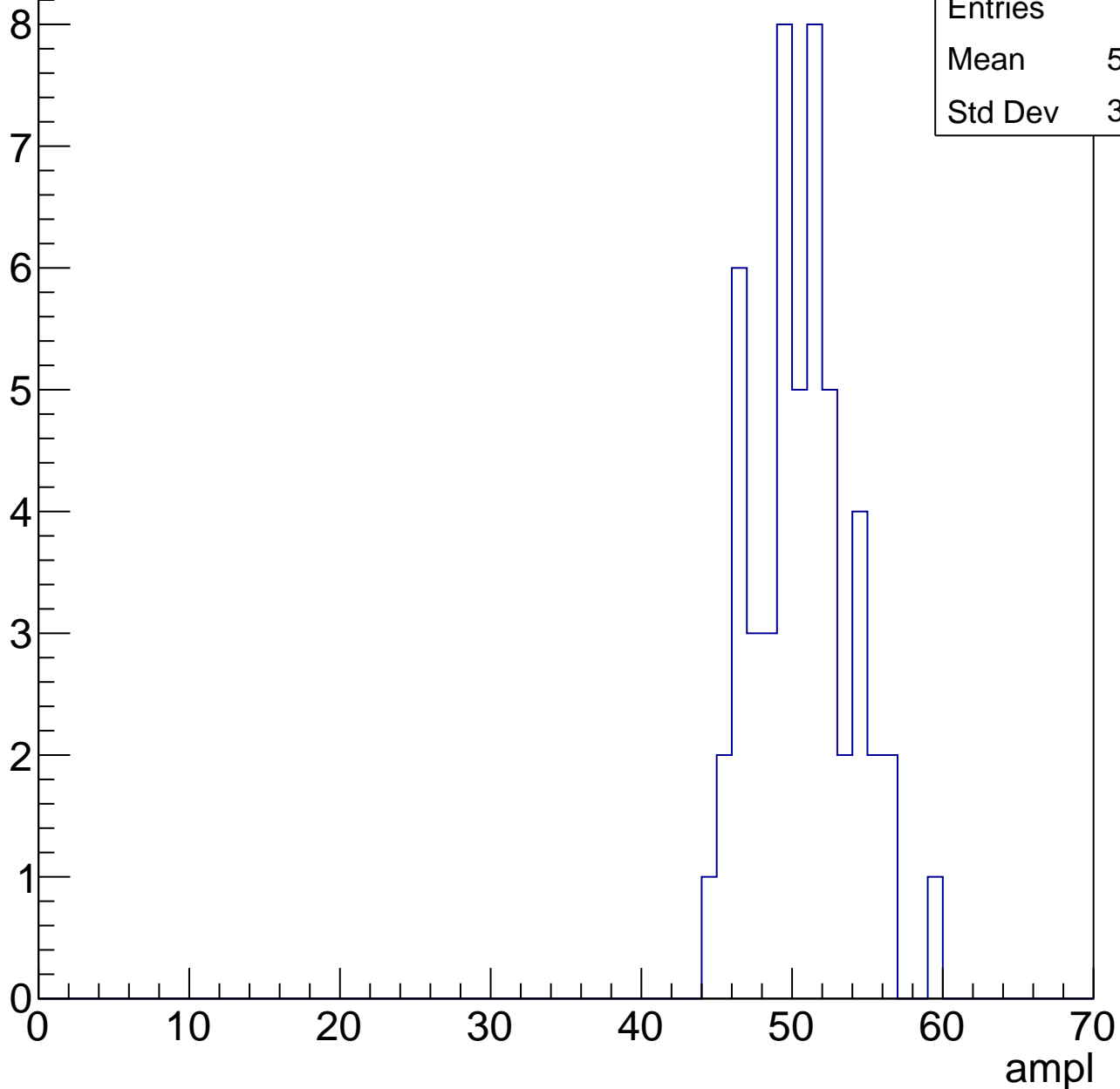
**Gaus Width: 4.3182**



# B0L001S, U17-ch96, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

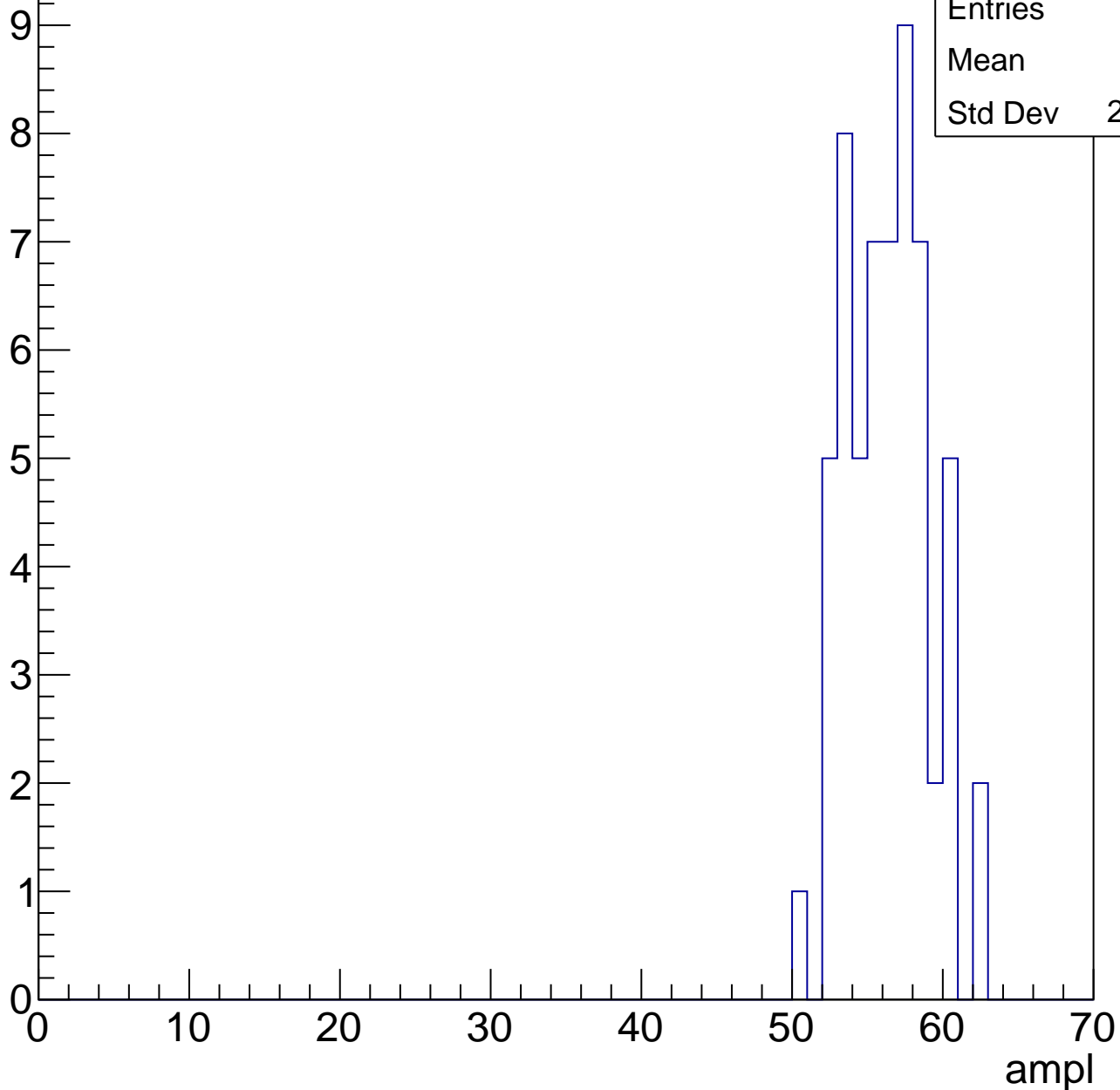
Entry



# B0L001S, U17-ch96, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



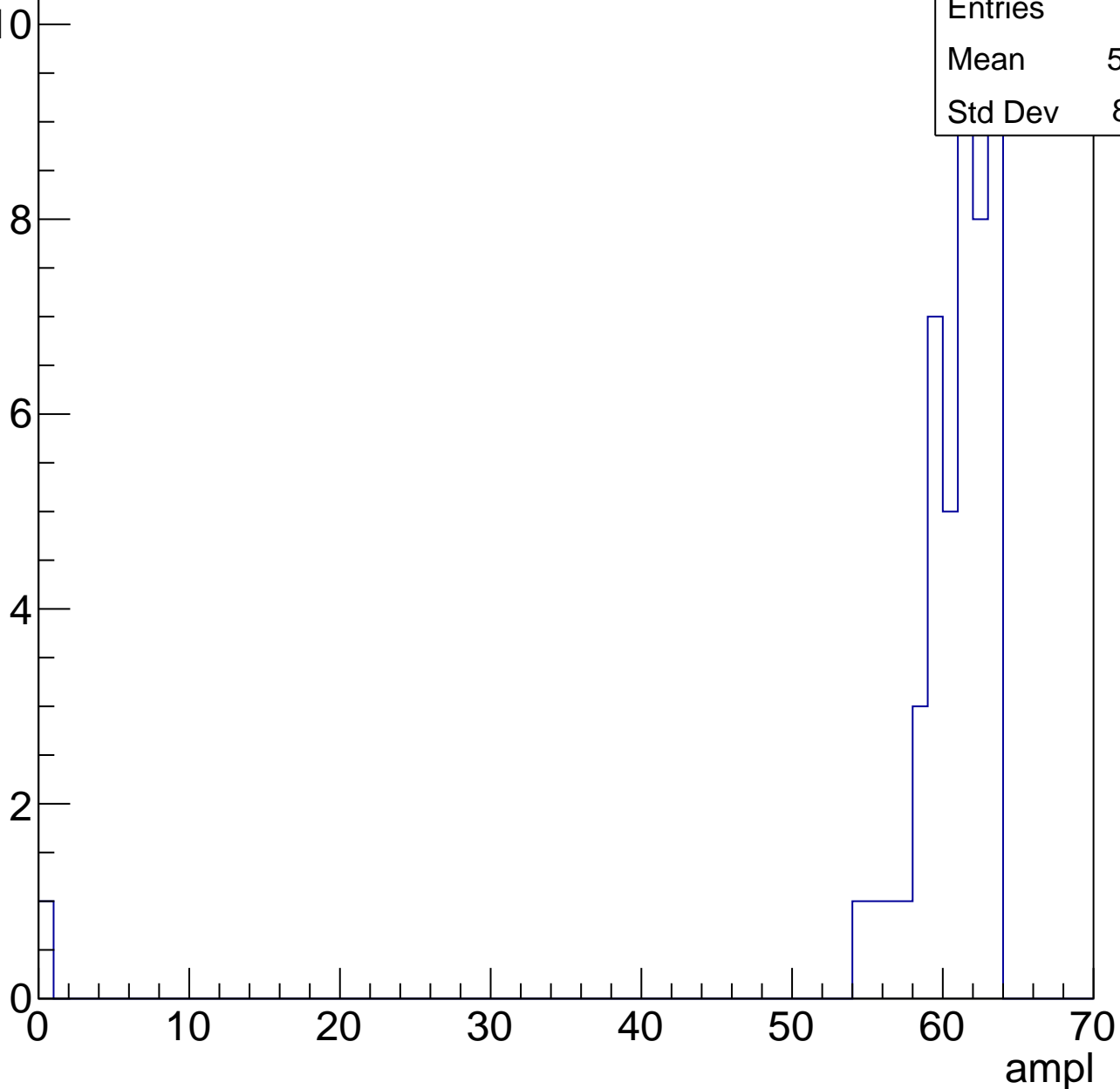
Entries	58
Mean	55.9
Std Dev	2.695

# B0L001S, U17-ch96, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	48
Mean	59.27
Std Dev	8.911



# B0L001S, U17-ch96, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch96, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U17-ch97, adc0

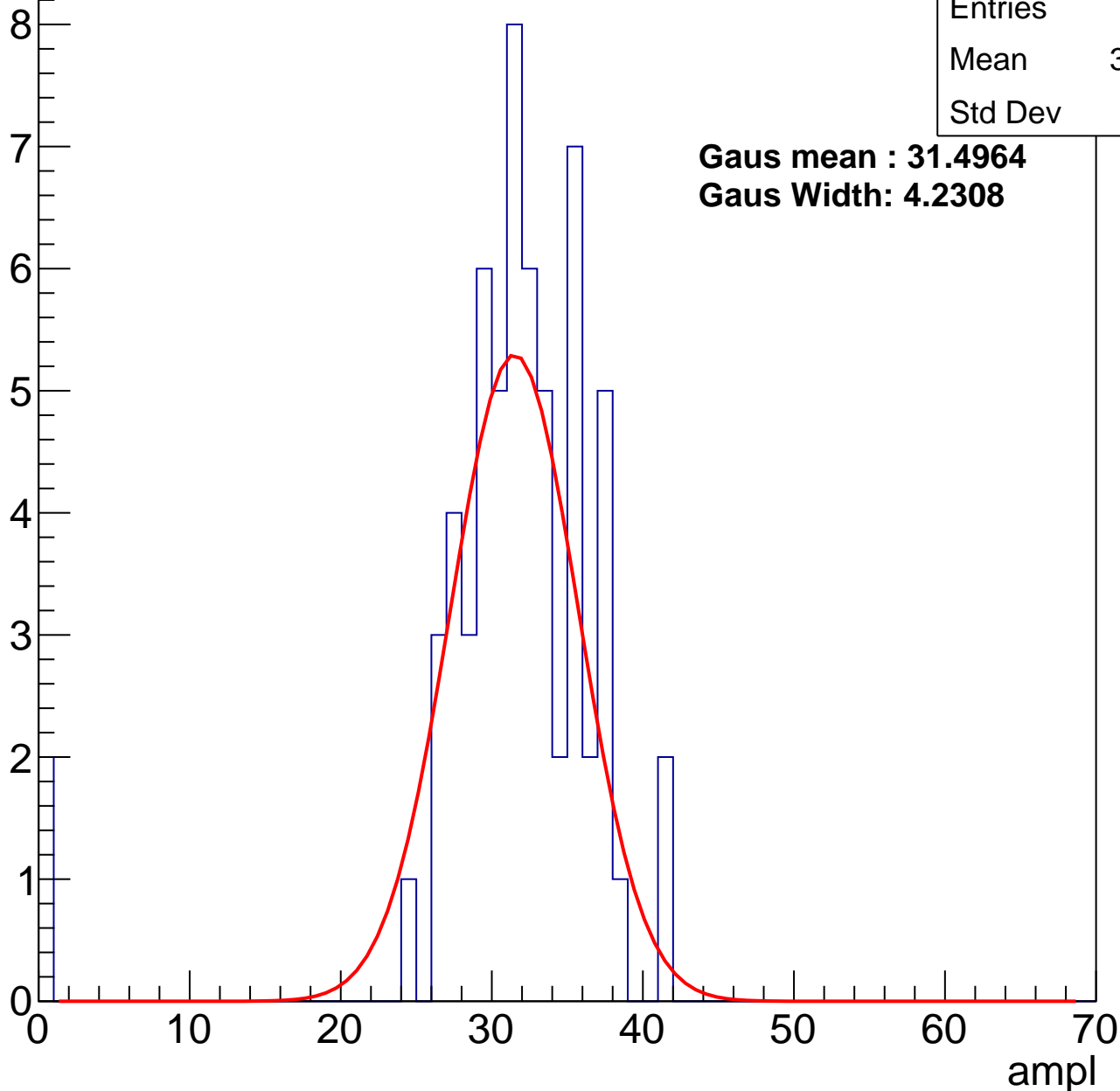
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	30.85
Std Dev	6.72

**Gaus mean : 31.4964**

**Gaus Width: 4.2308**



# B0L001S, U17-ch97, adc1

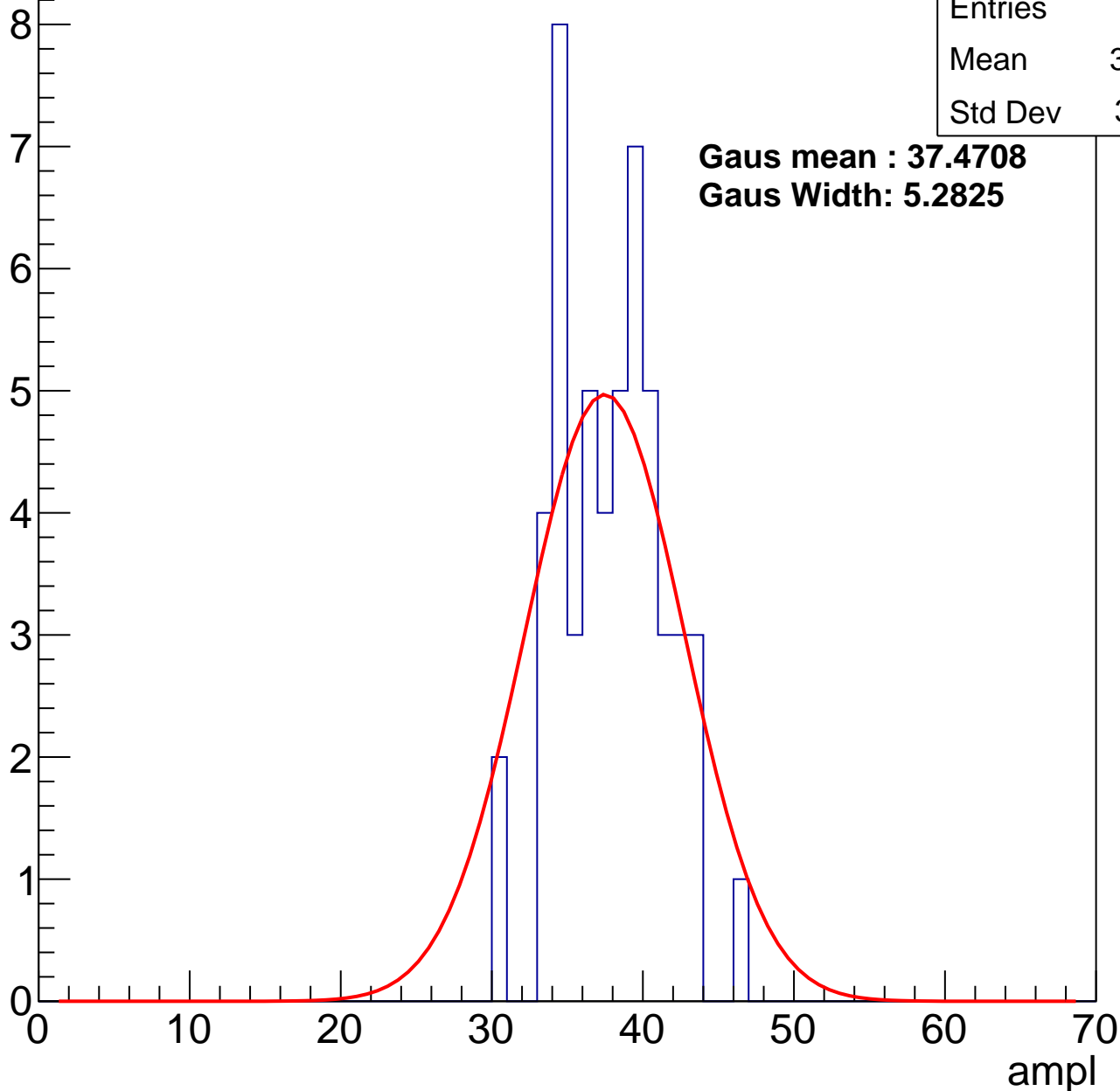
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	37.43
Std Dev	3.451

**Gaus mean : 37.4708**

**Gaus Width: 5.2825**



# B0L001S, U17-ch97, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	86
Mean	44.42
Std Dev	3.774

**Gaus mean : 45.1273**

**Gaus Width: 4.0743**

10

8

6

4

2

0

0

10

20

30

40

50

60

ampl

0

2

4

6

8

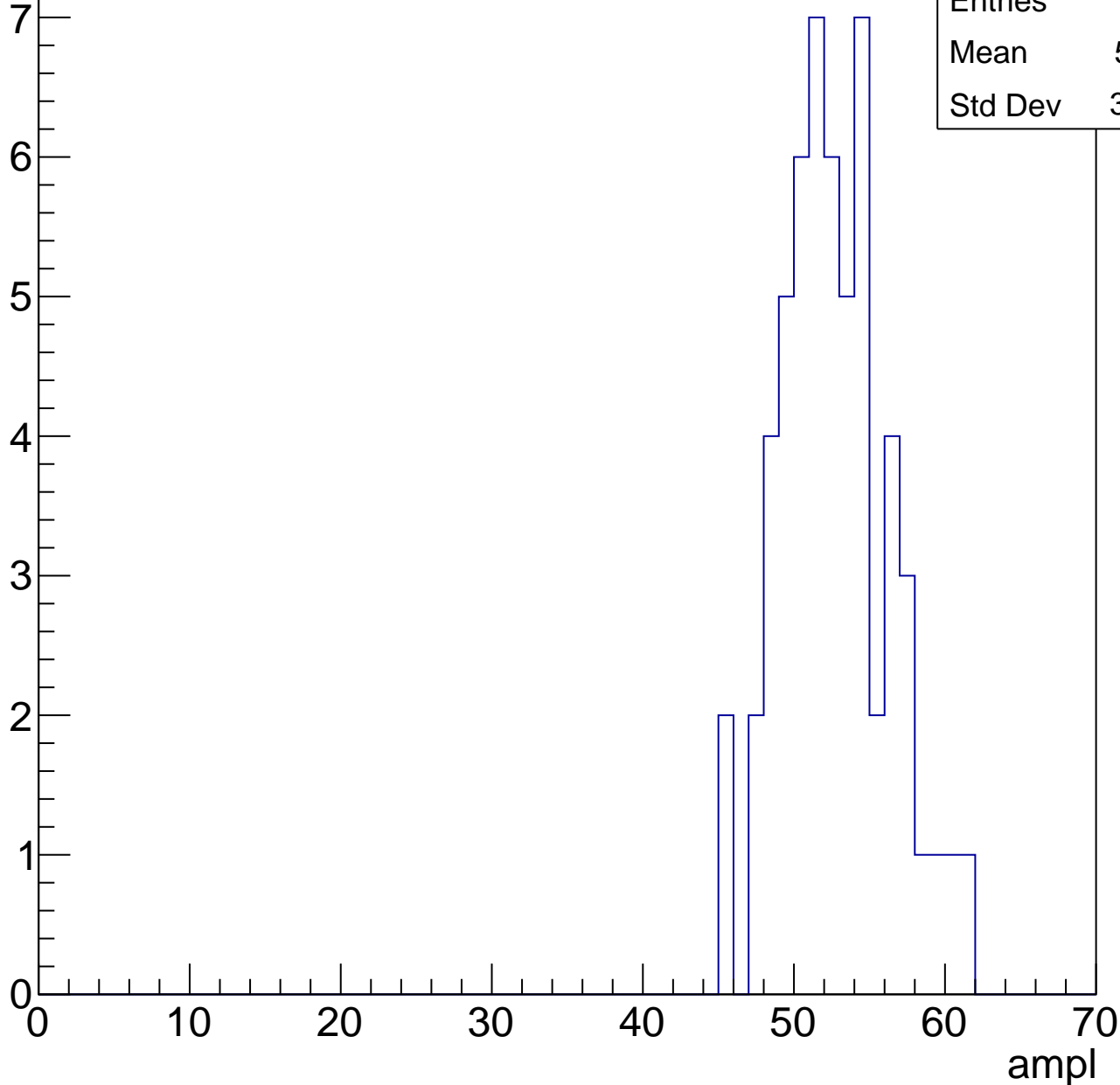
10

# B0L001S, U17-ch97, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	52.21
Std Dev	3.518

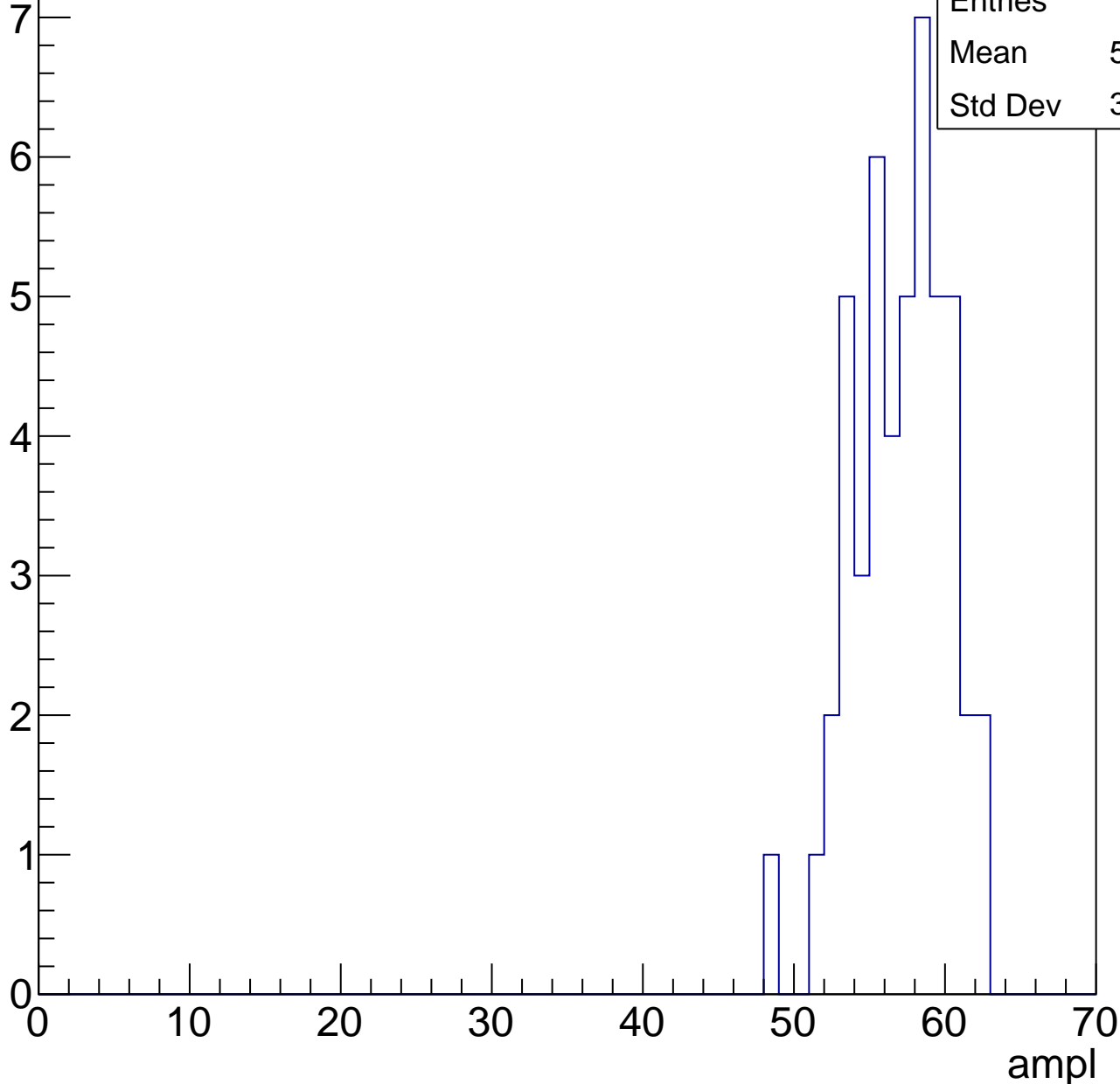


# B0L001S, U17-ch97, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

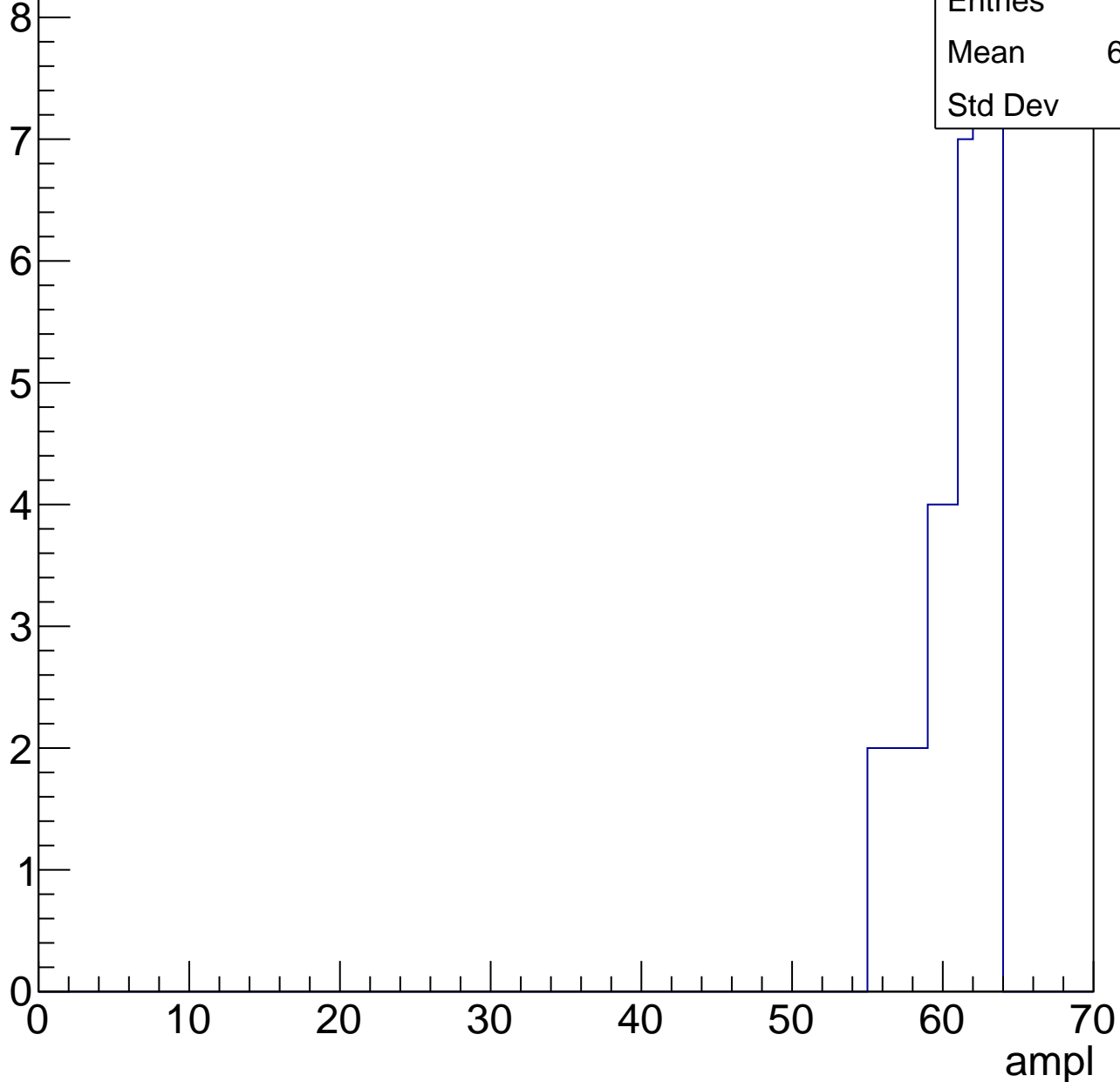
Entries	48
Mean	56.58
Std Dev	3.054



# B0L001S, U17-ch97, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U17-ch97, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch97, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U17-ch98, adc0

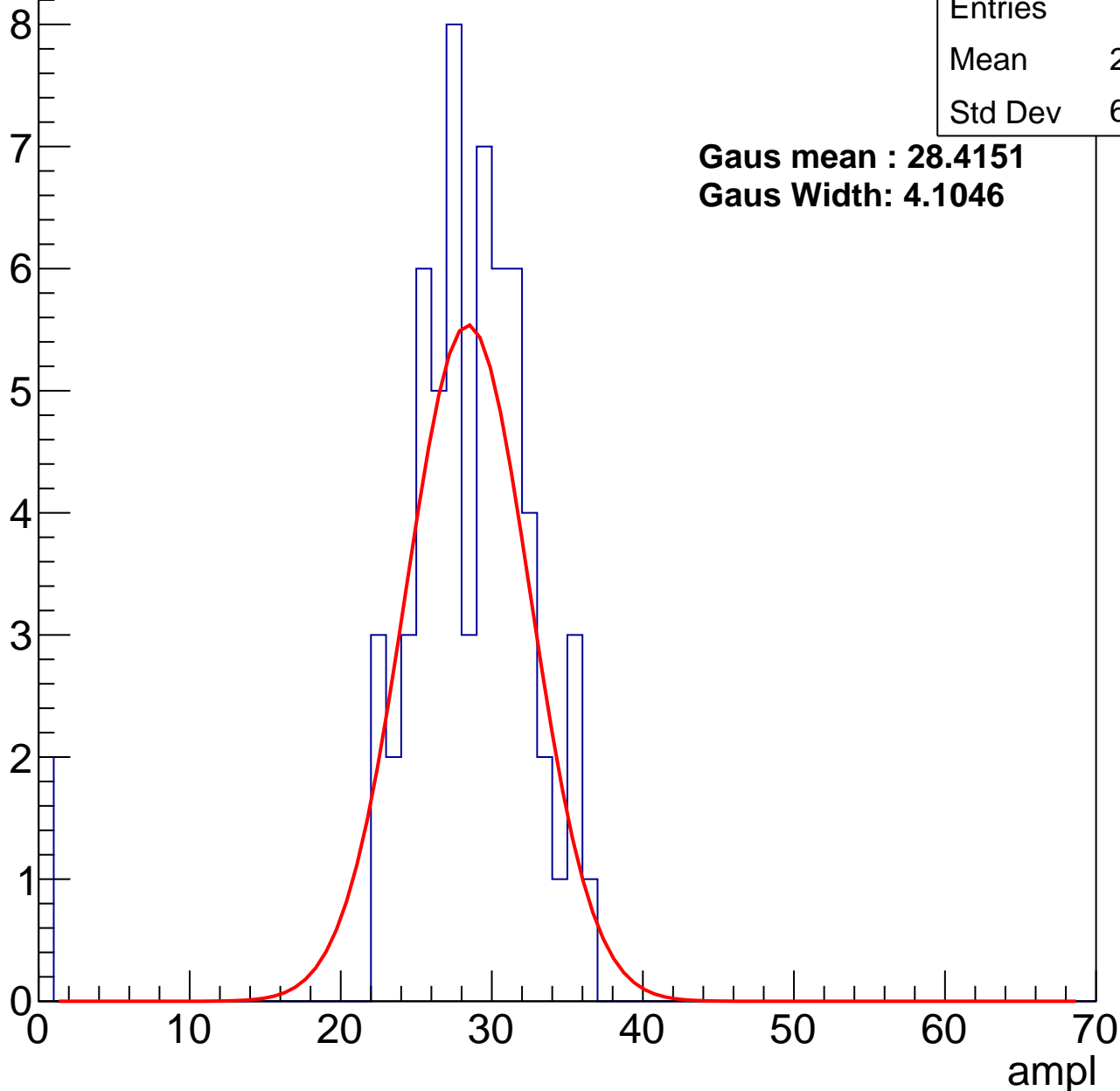
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	27.45
Std Dev	6.069

**Gaus mean : 28.4151**

**Gaus Width: 4.1046**



# B0L001S, U17-ch98, adc1

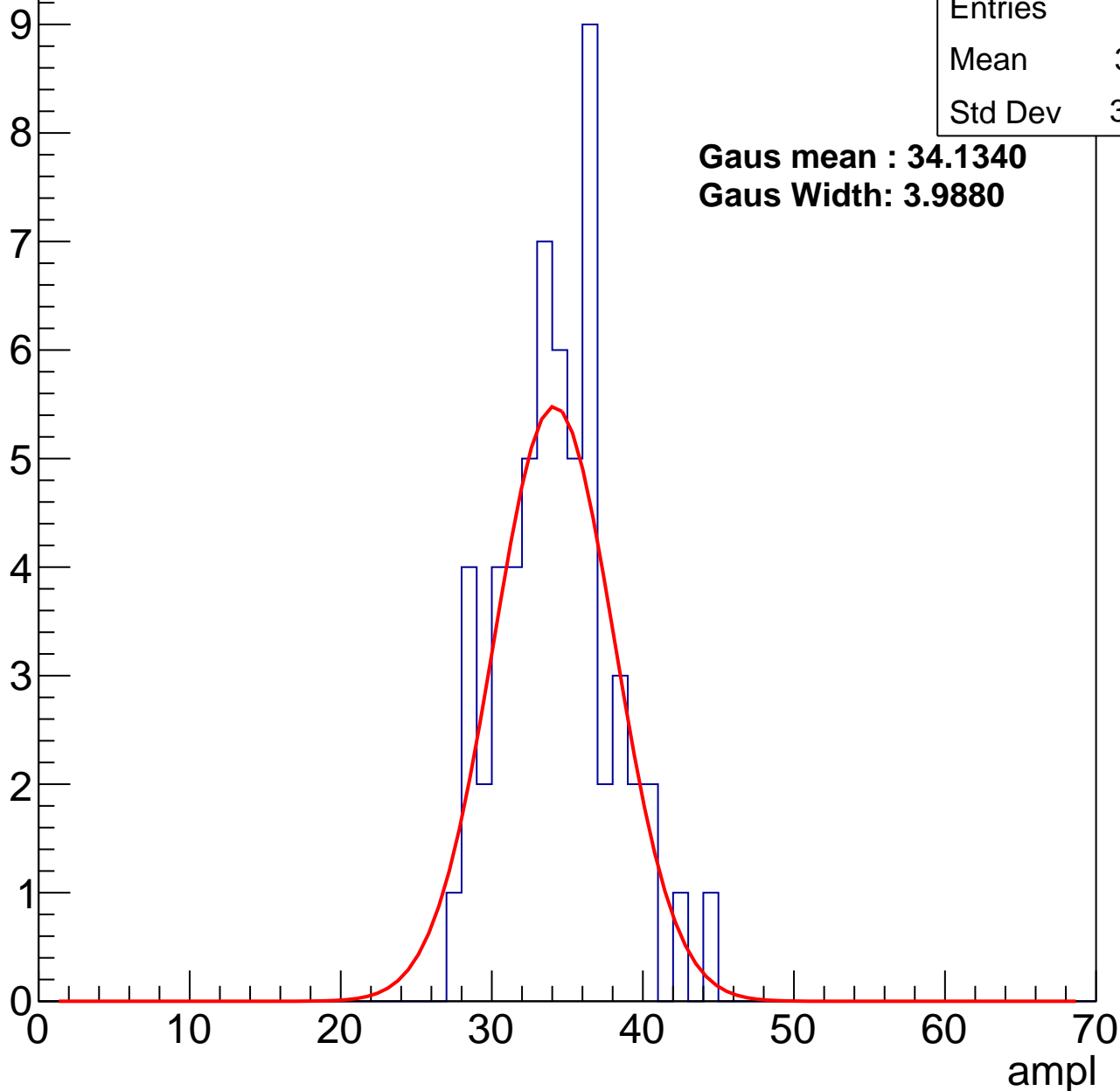
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	33.91
Std Dev	3.626

**Gaus mean : 34.1340**

**Gaus Width: 3.9880**



# B0L001S, U17-ch98, adc2

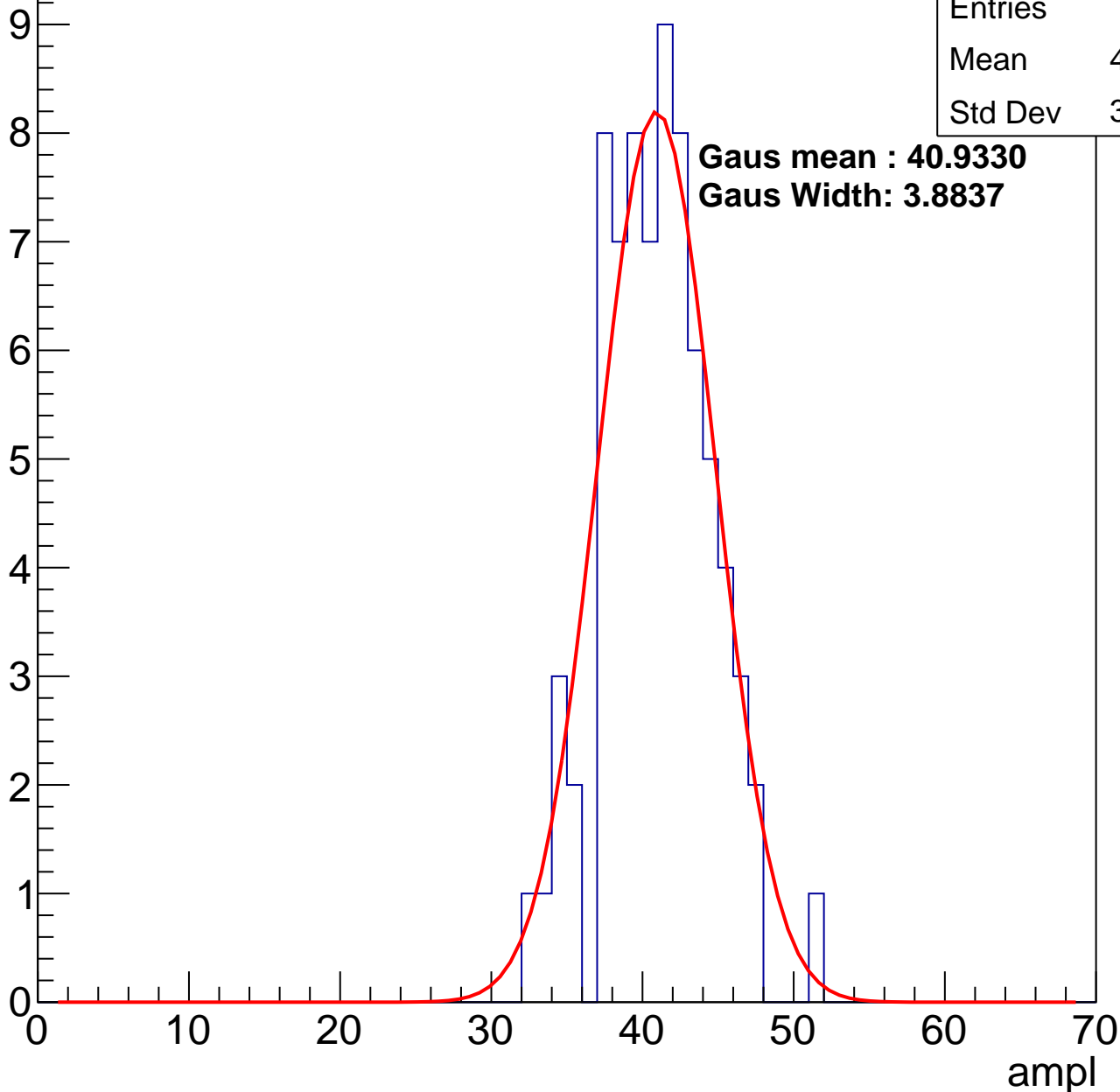
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	75
Mean	40.49
Std Dev	3.583

**Gaus mean : 40.9330**

**Gaus Width: 3.8837**



# B0L001S, U17-ch98, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

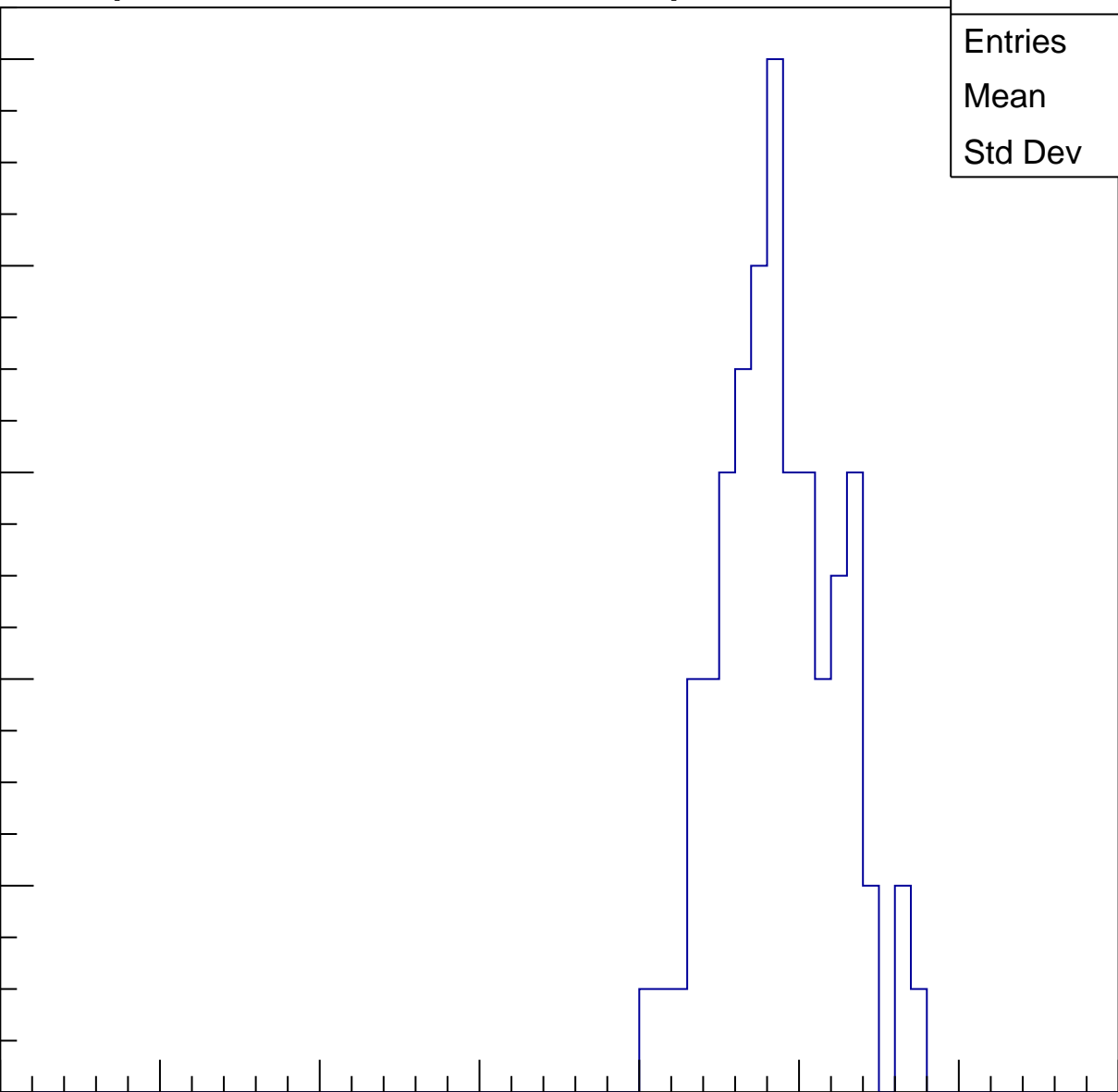
Entries	74
Mean	48.27
Std Dev	3.629

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

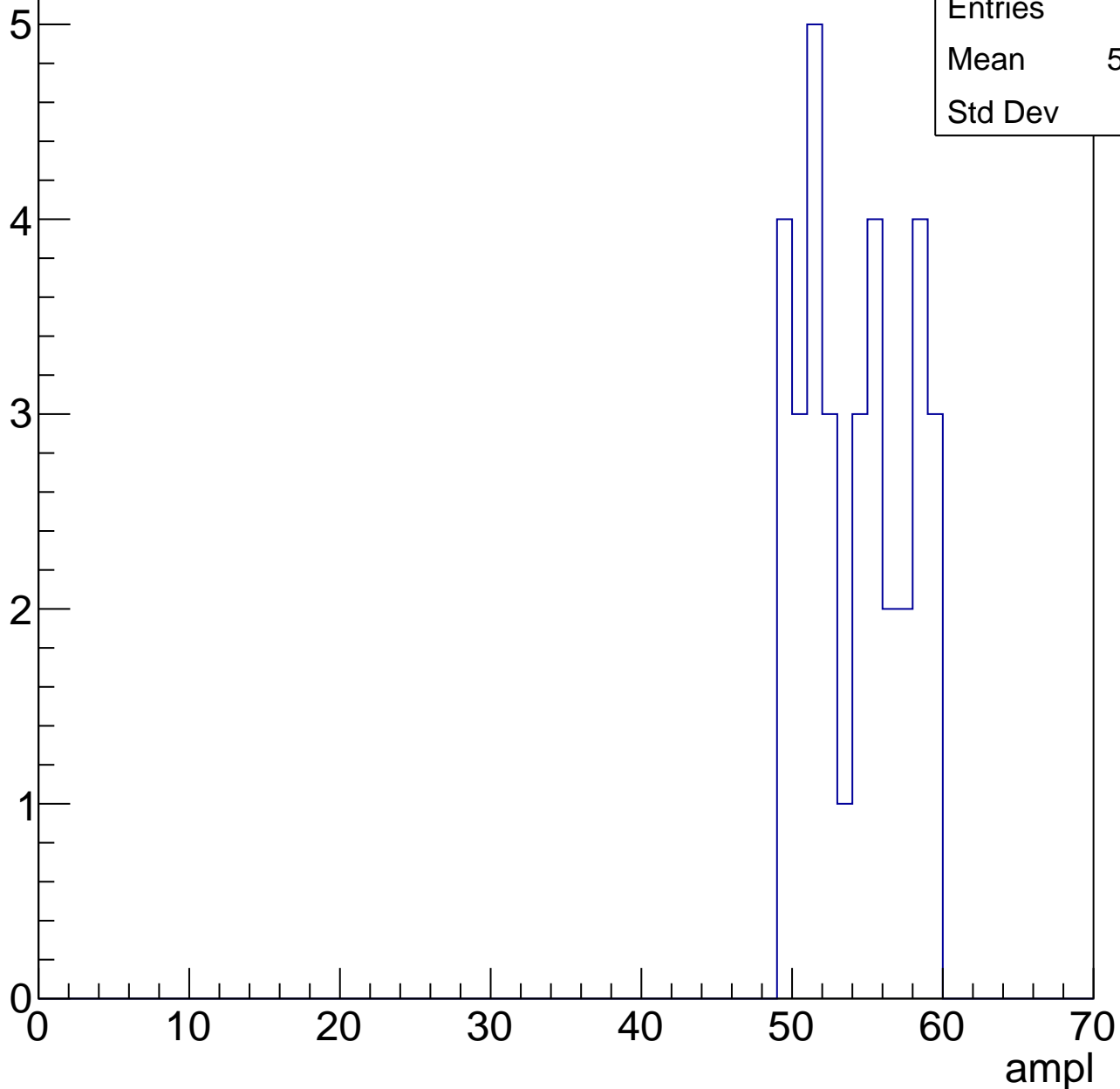
ampl



# B0L001S, U17-ch98, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



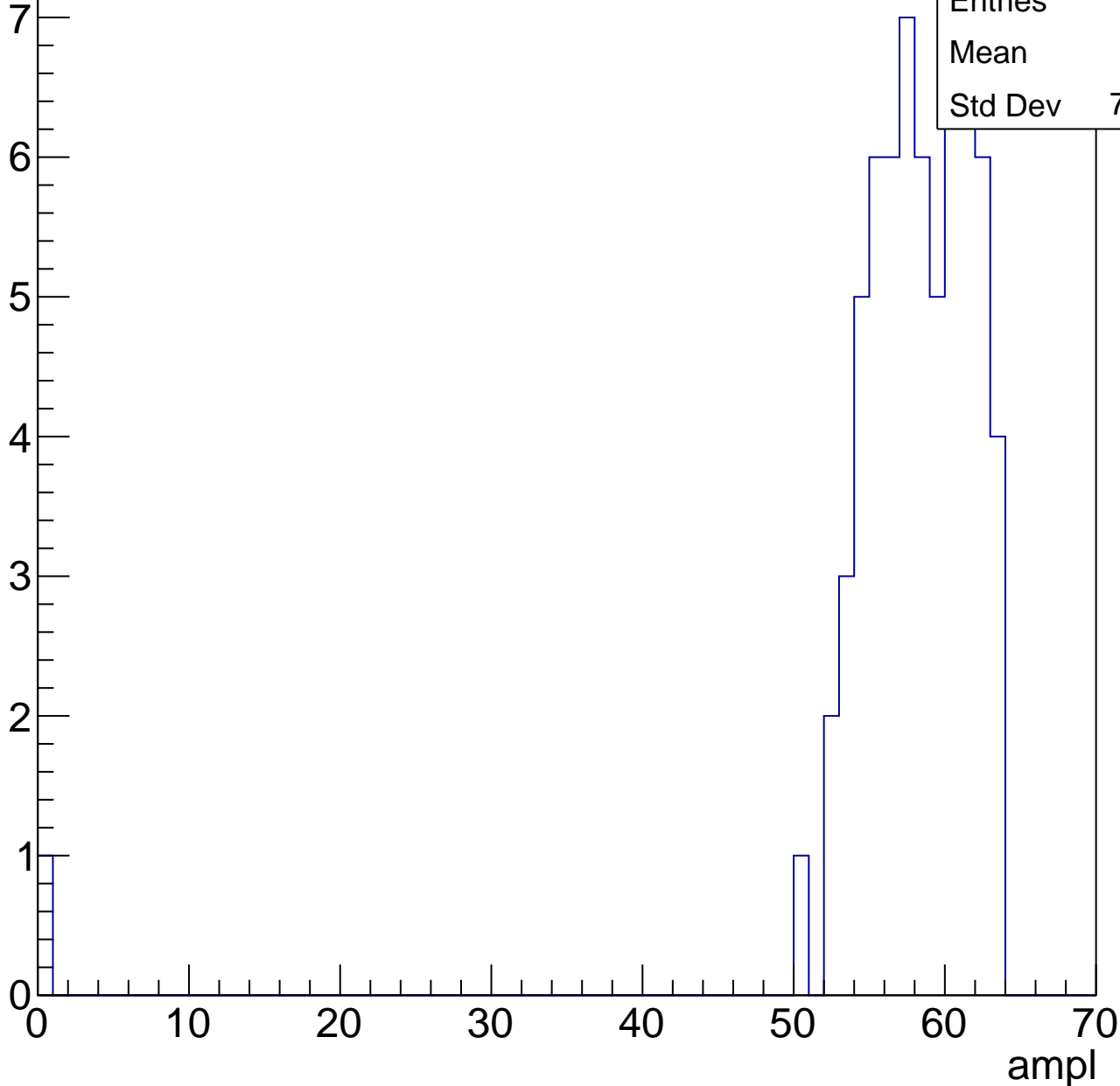
Entries	34
Mean	53.74
Std Dev	3.31

# B0L001S, U17-ch98, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	57
Std Dev	7.752

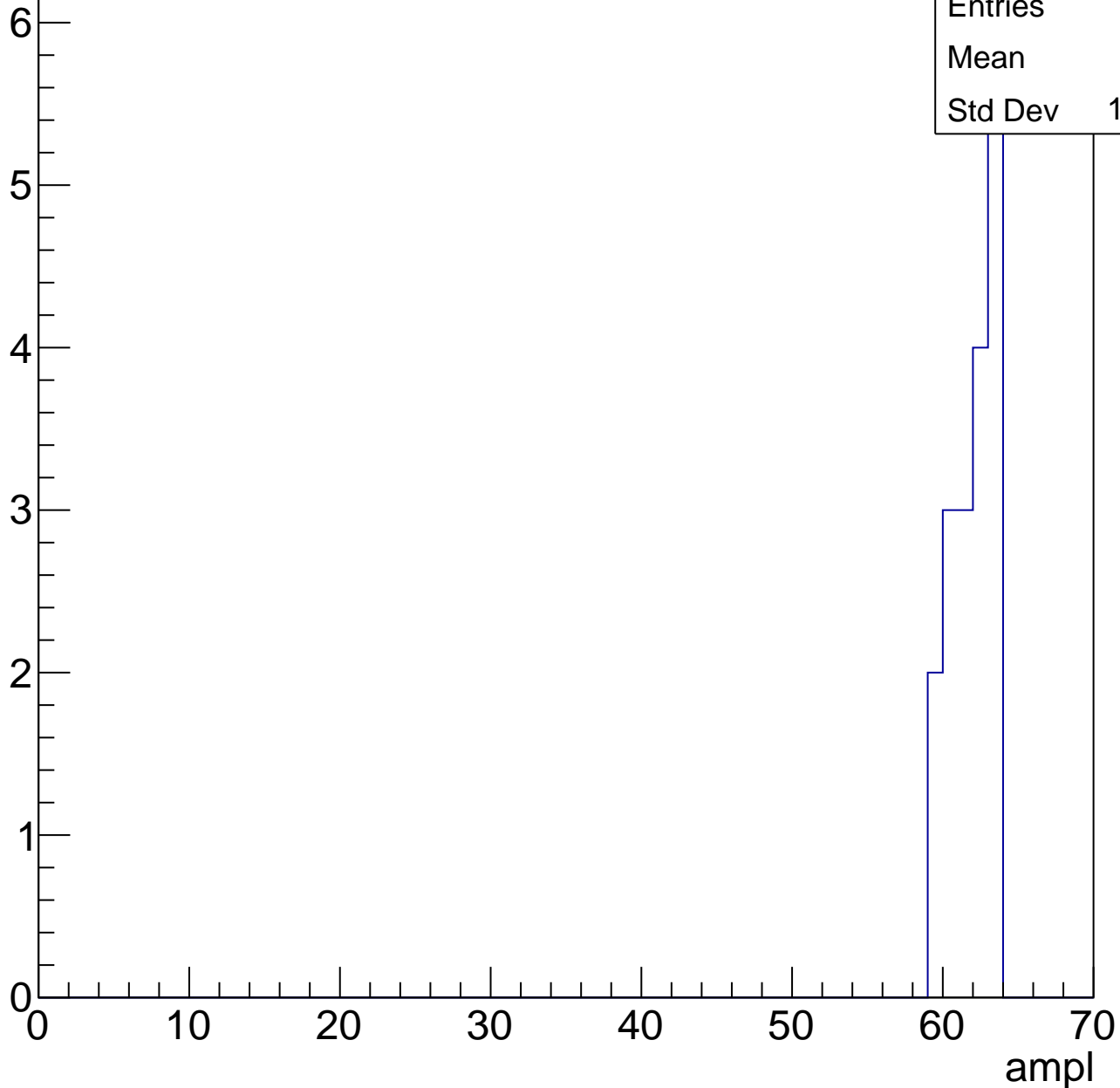


# B0L001S, U17-ch98, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	18
Mean	61.5
Std Dev	1.384





# B0L001S, U17-ch98, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U17-ch99, adc0

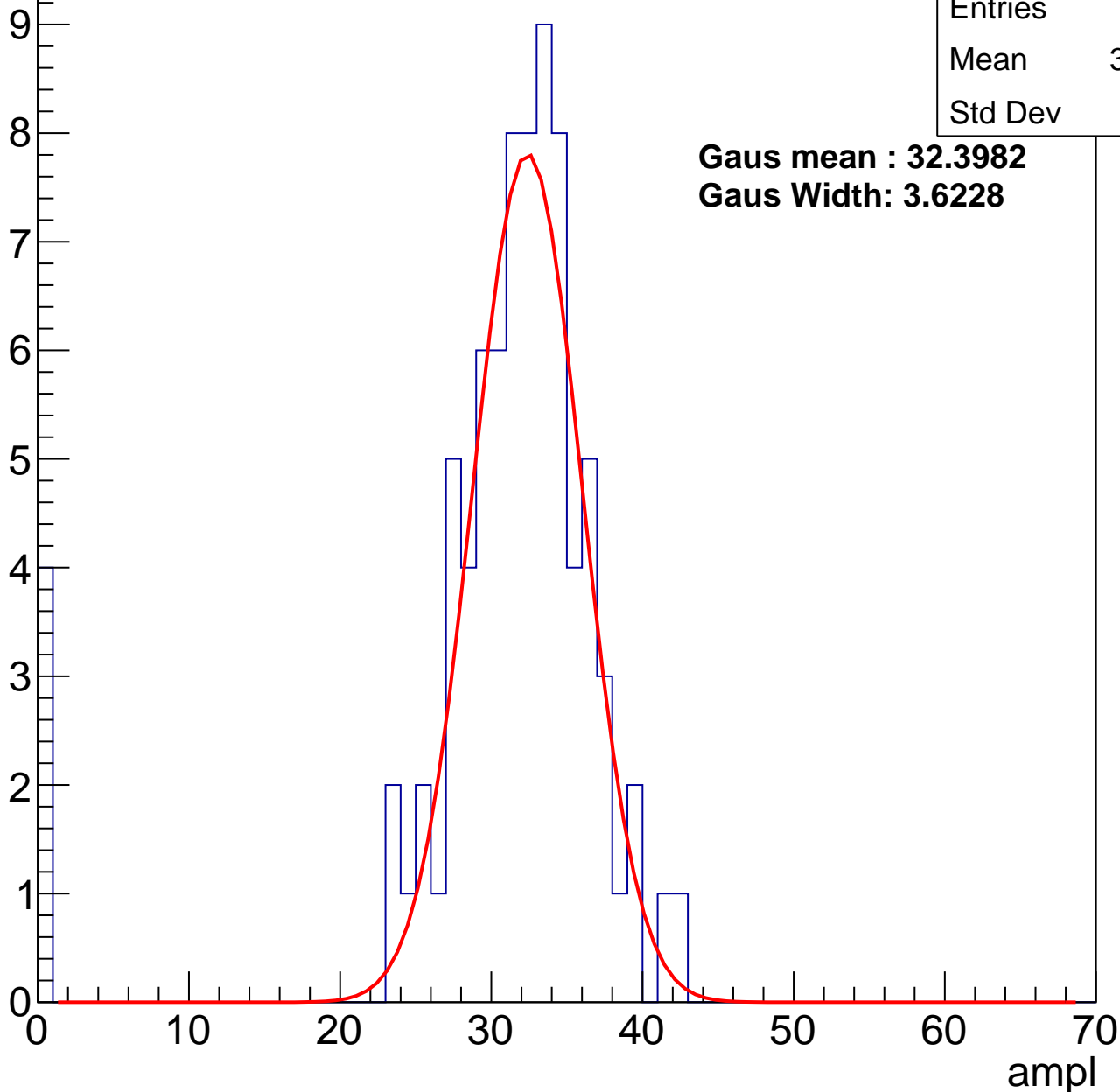
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	81
Mean	30.25
Std Dev	7.88

**Gaus mean : 32.3982**

**Gaus Width: 3.6228**



# B0L001S, U17-ch99, adc1

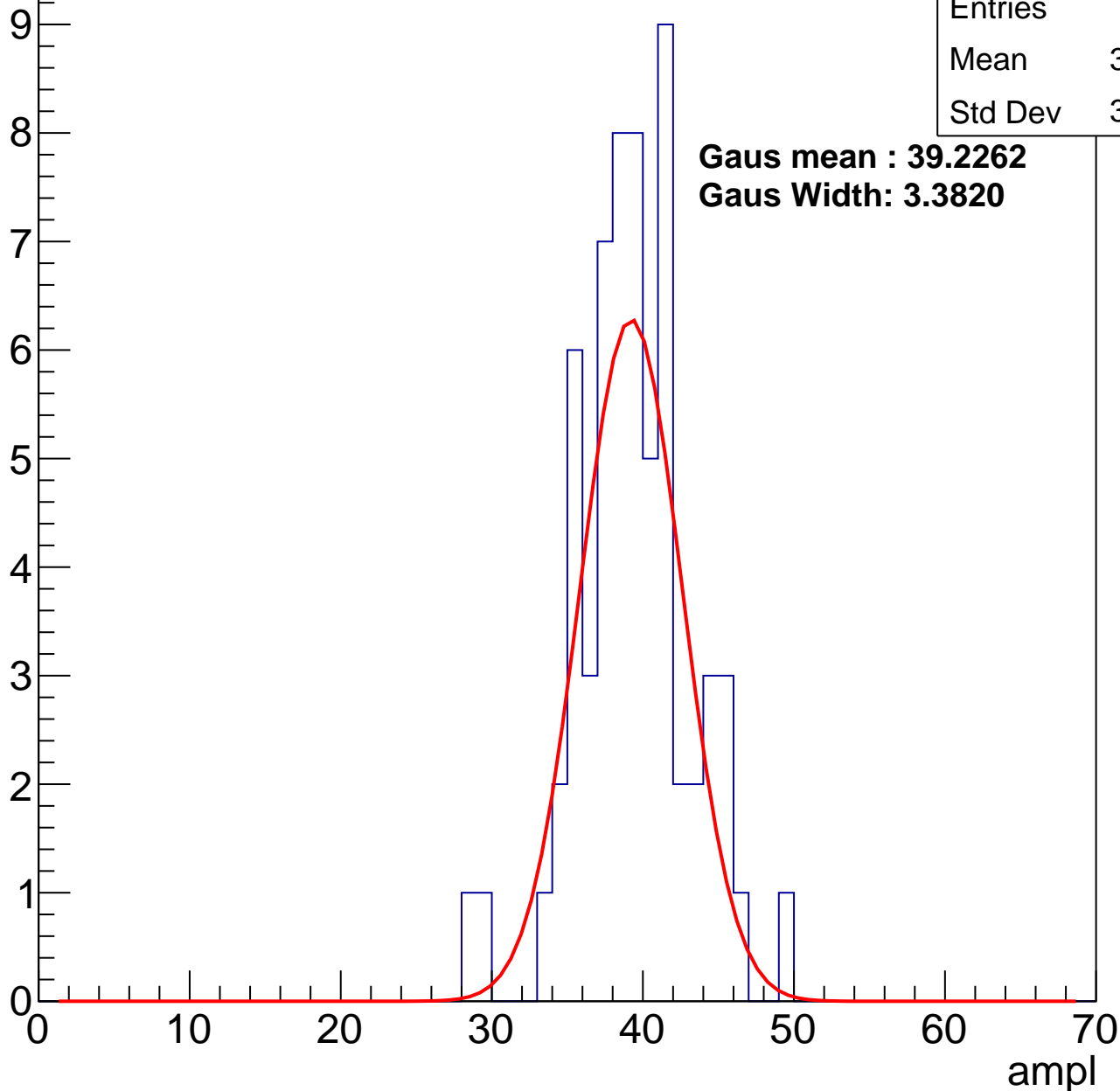
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	38.92
Std Dev	3.756

**Gaus mean : 39.2262**

**Gaus Width: 3.3820**



# B0L001S, U17-ch99, adc2

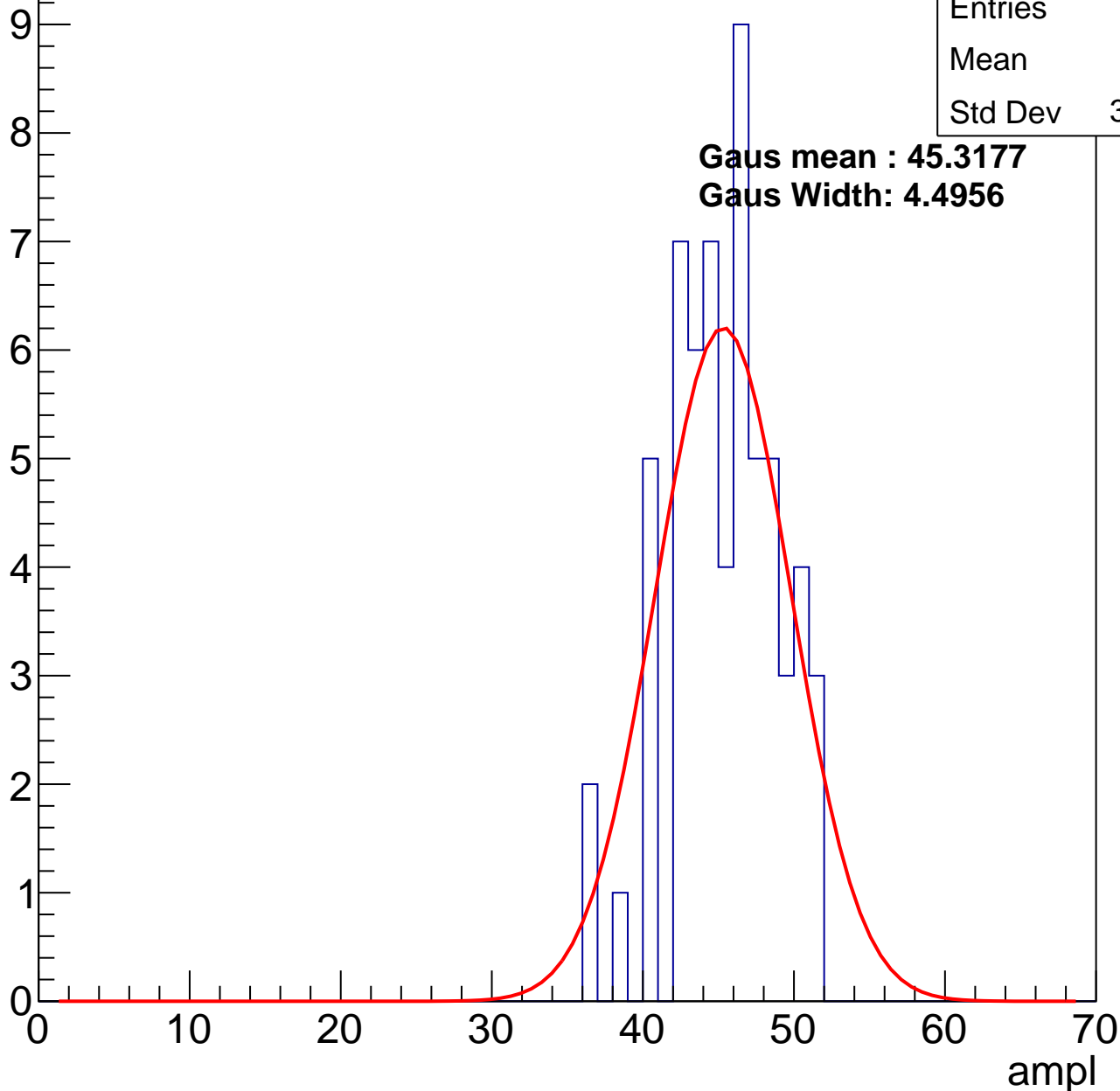
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	44.9
Std Dev	3.528

**Gaus mean : 45.3177**

**Gaus Width: 4.4956**



# B0L001S, U17-ch99, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	74
Mean	51.72
Std Dev	3.765

Entry

10

8

6

4

2

0

0

10

20

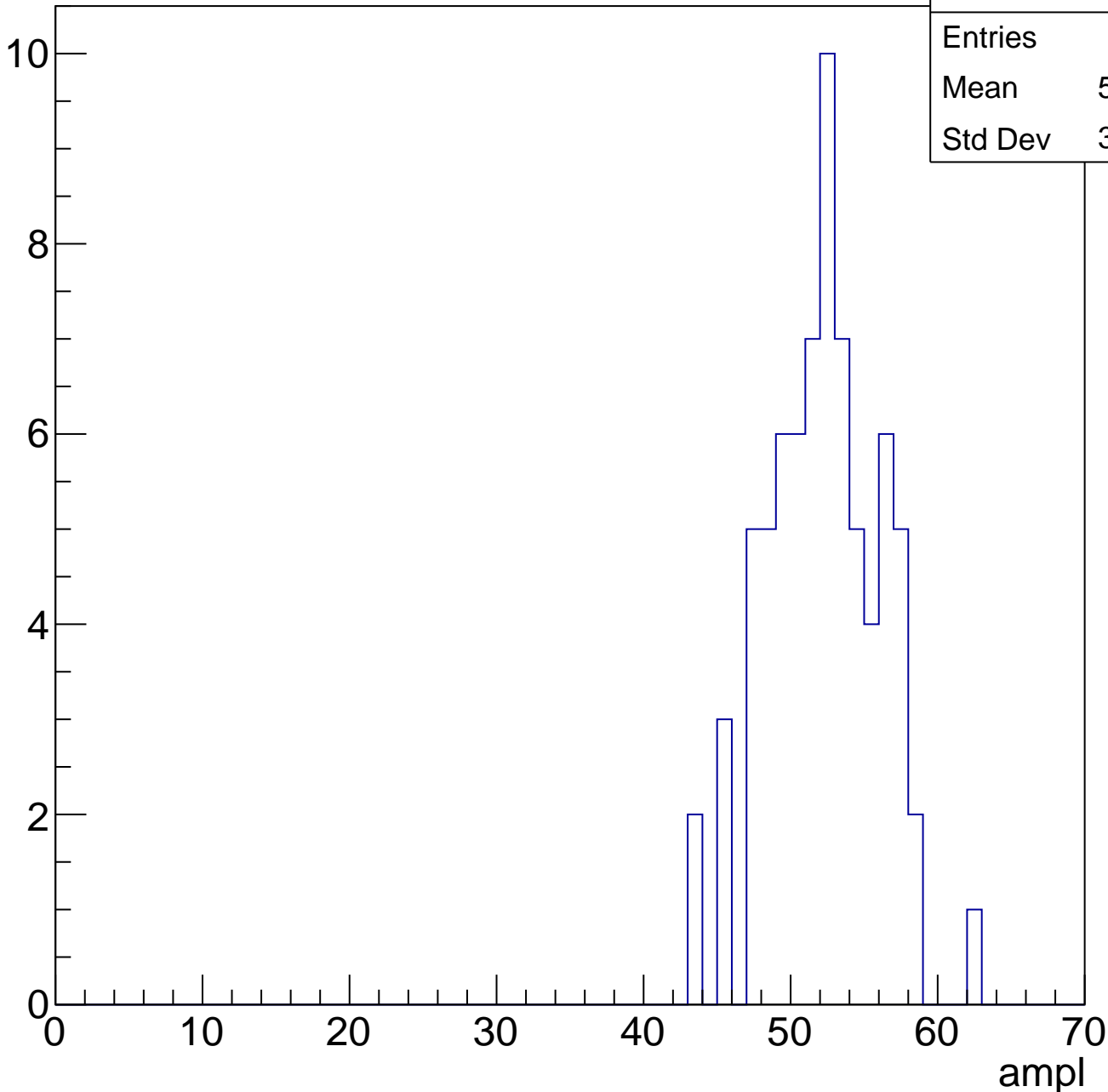
30

40

50

60

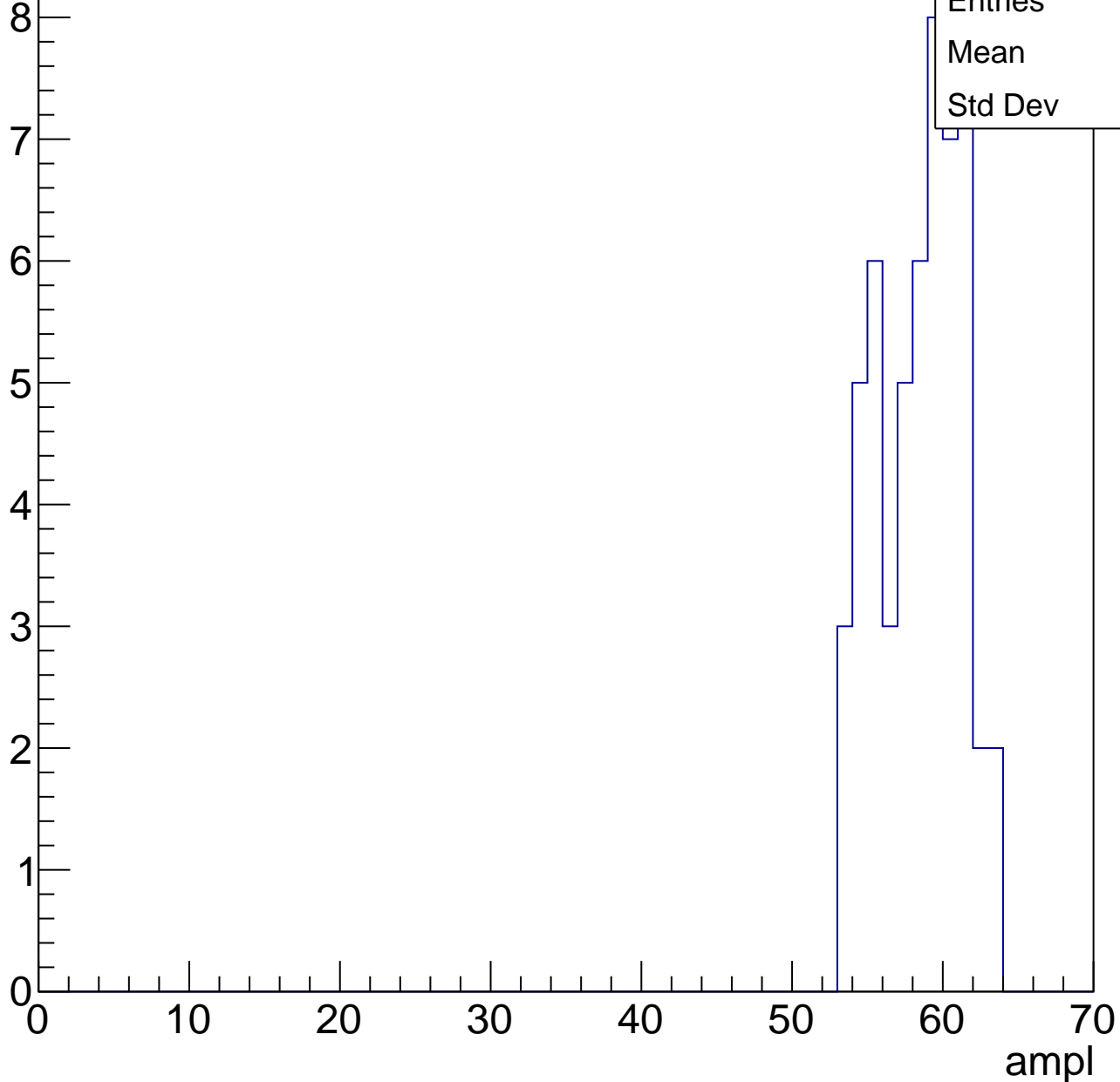
ampl



# B0L001S, U17-ch99, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

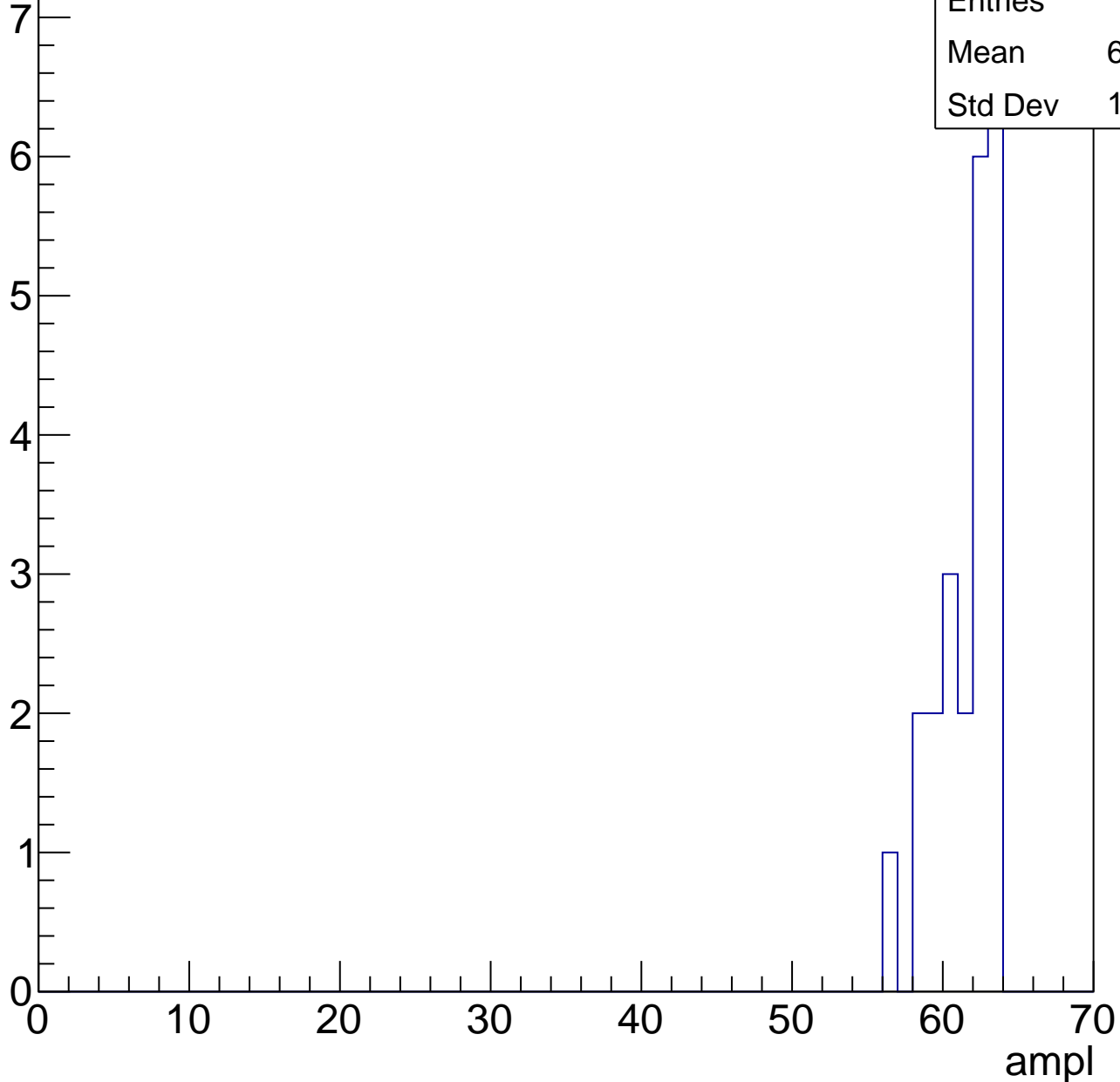


# B0L001S, U17-ch99, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	23
Mean	61.09
Std Dev	1.954



# B0L001S, U17-ch99, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch99, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U17-ch100, adc0

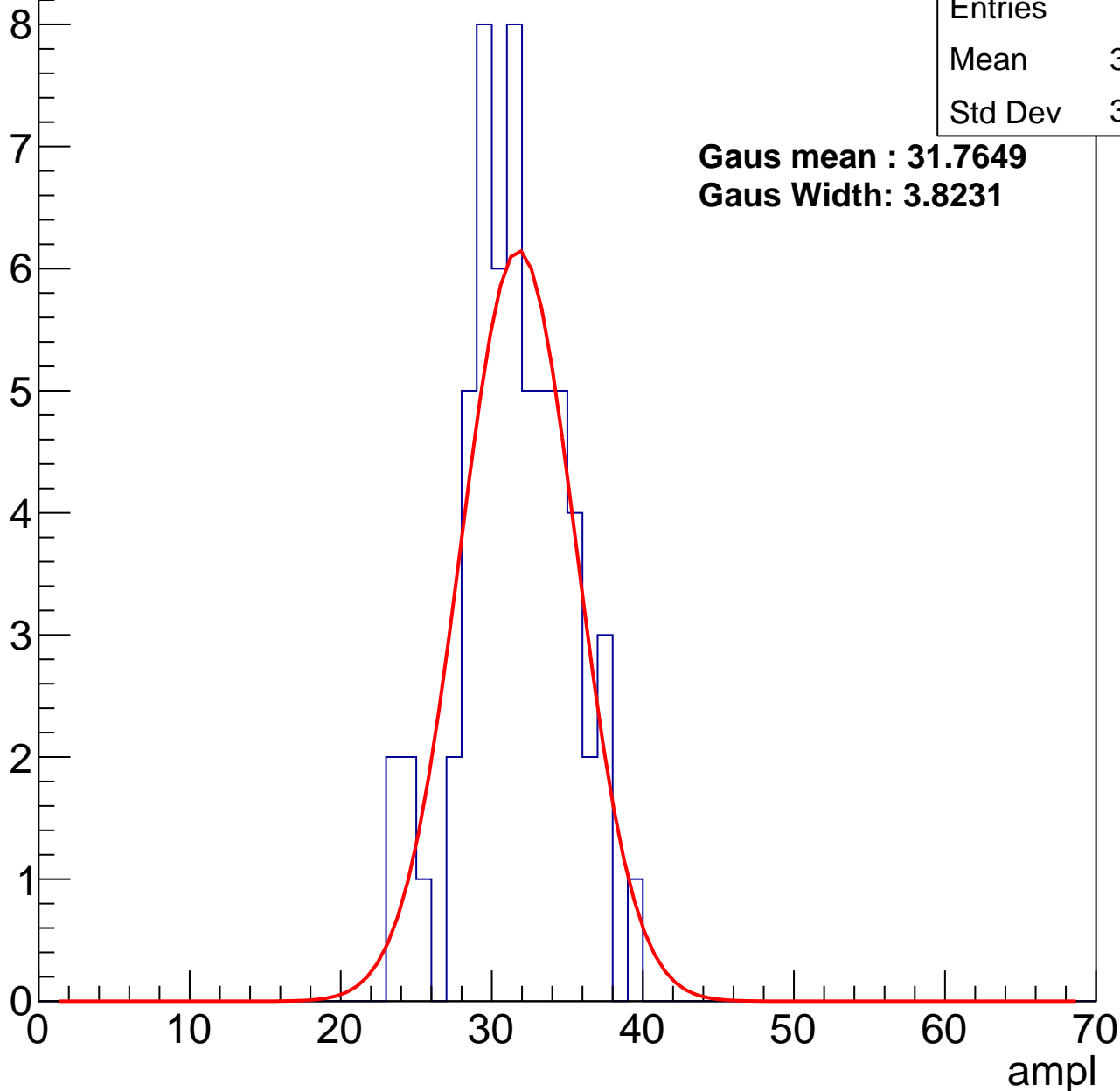
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	31.02
Std Dev	3.525

**Gaus mean : 31.7649**

**Gaus Width: 3.8231**



# B0L001S, U17-ch100, adc1

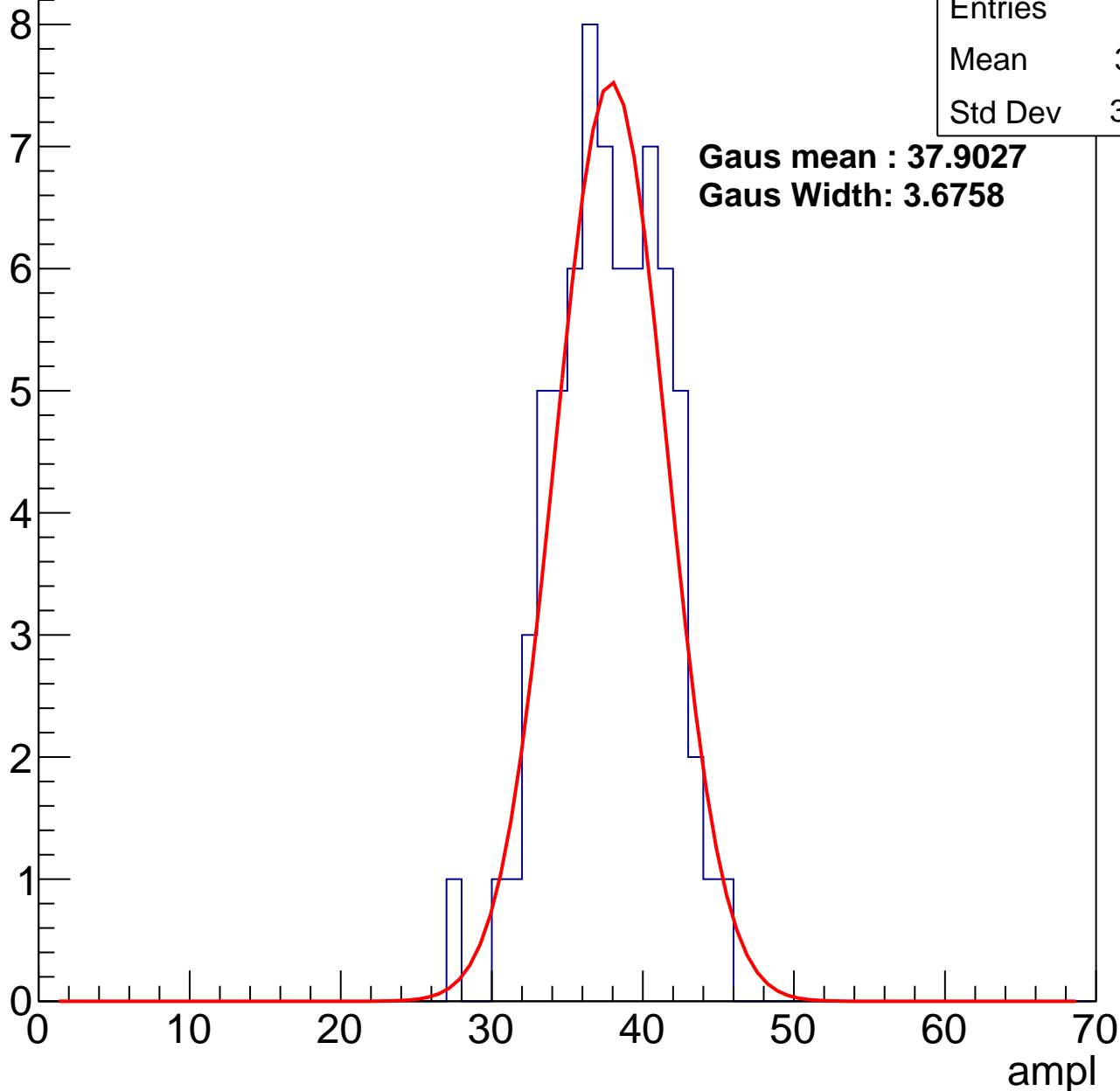
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	37.31
Std Dev	3.578

**Gaus mean : 37.9027**

**Gaus Width: 3.6758**



# B0L001S, U17-ch100, adc2

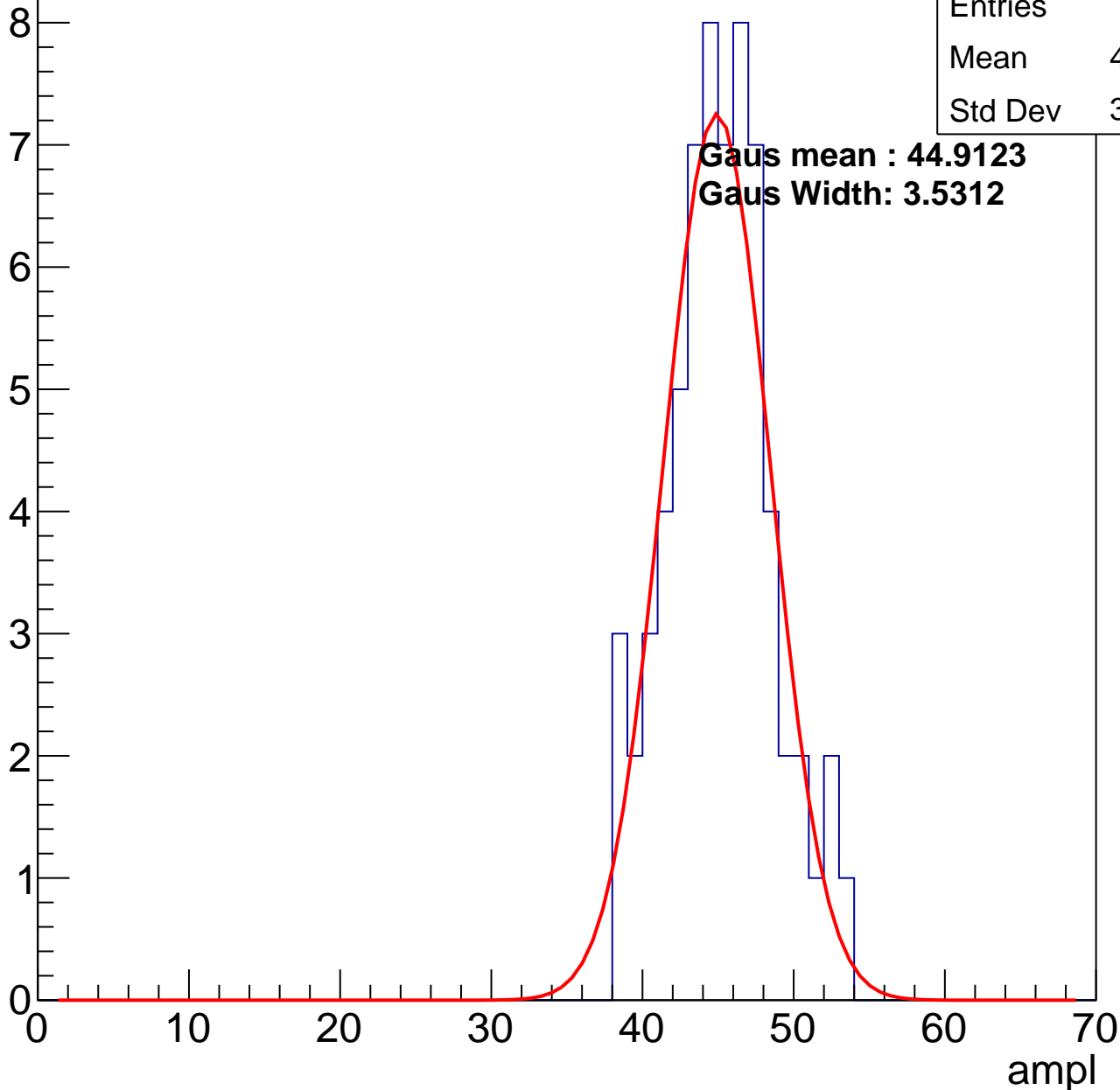
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	44.68
Std Dev	3.447

**Gaus mean : 44.9123**

**Gaus Width: 3.5312**

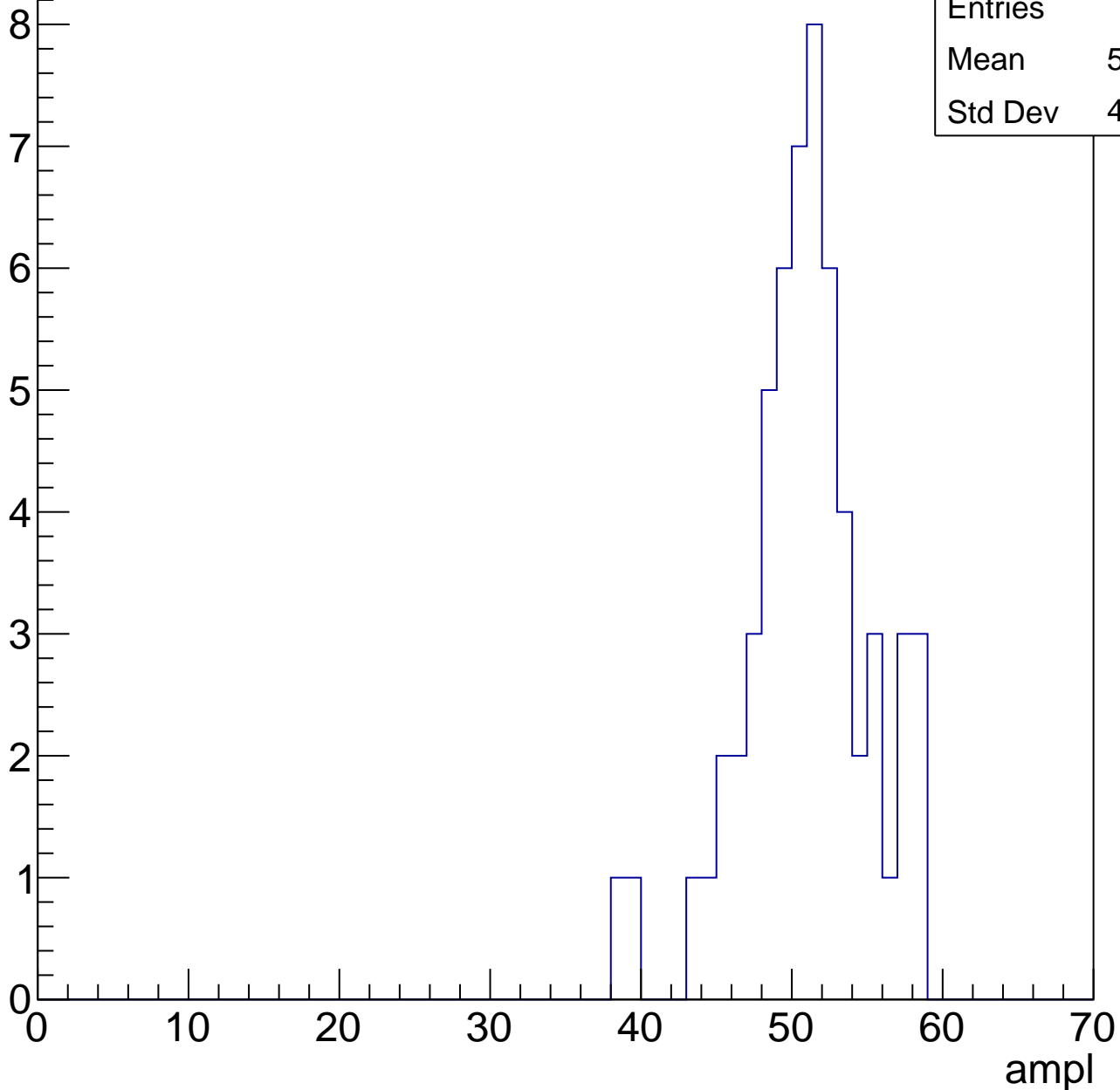


# B0L001S, U17-ch100, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	50.46
Std Dev	4.163

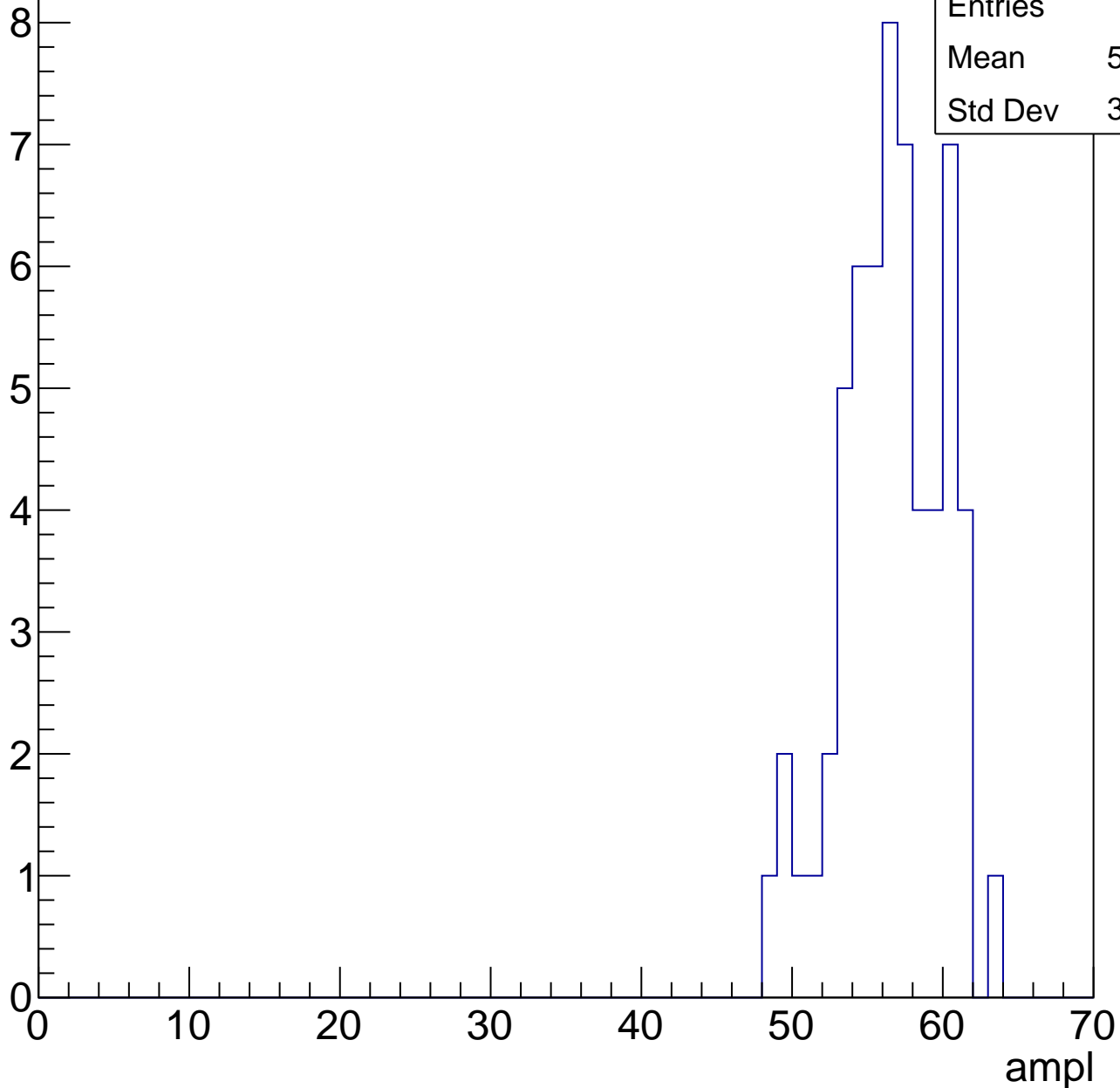


# B0L001S, U17-ch100, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	56.14
Std Dev	3.316

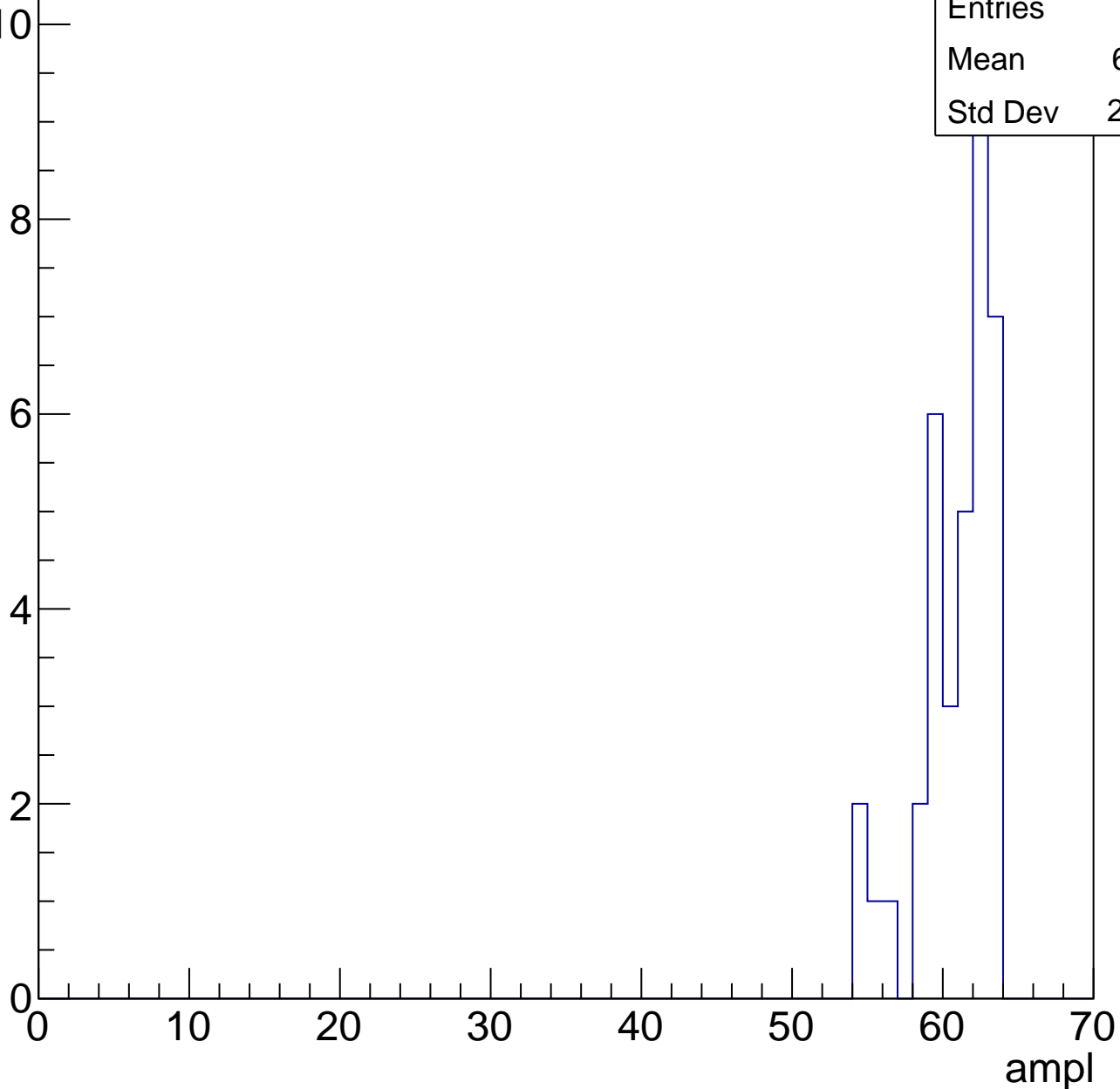


# B0L001S, U17-ch100, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

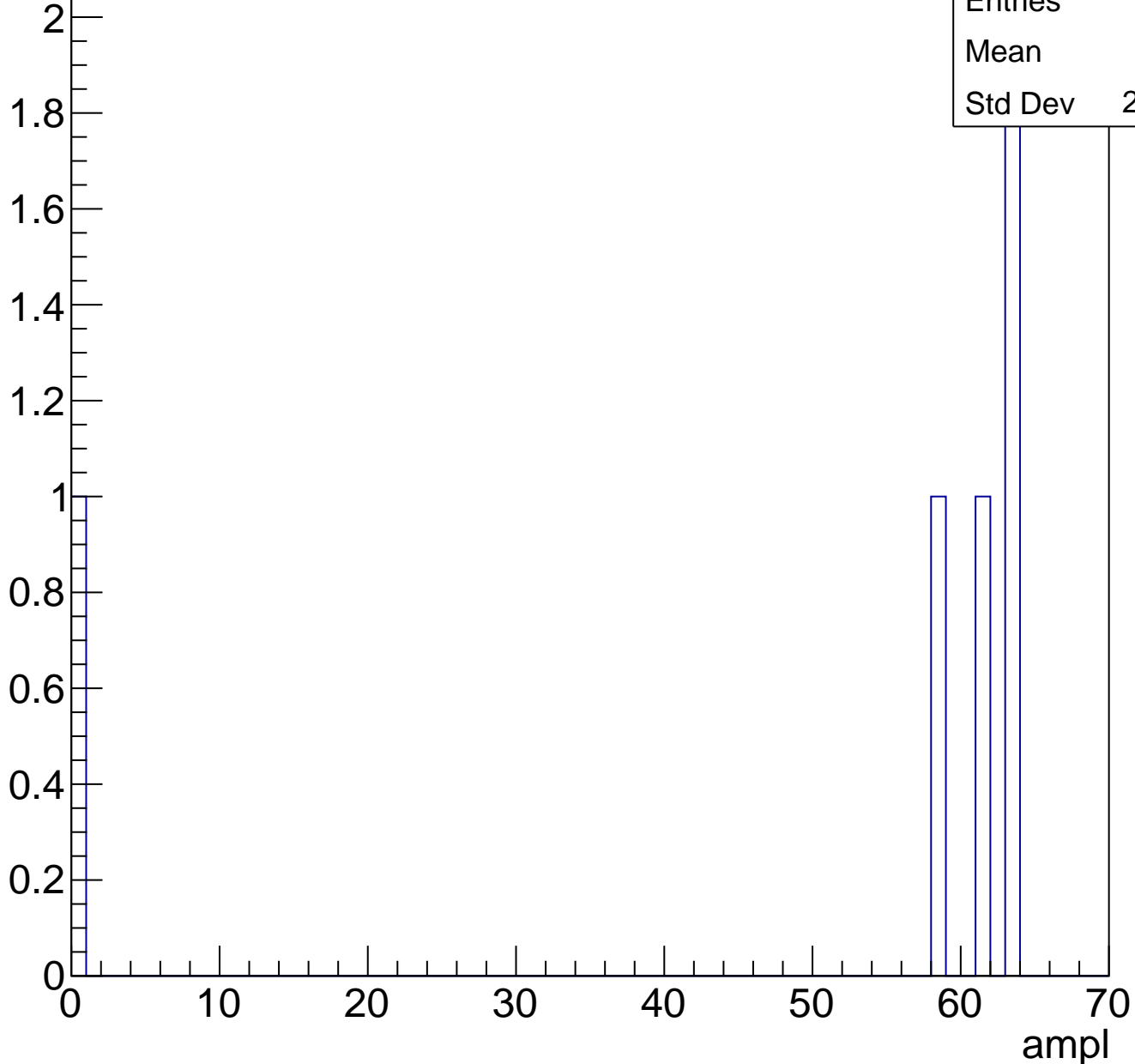
Entries	37
Mean	60.41
Std Dev	2.487



# B0L001S, U17-ch100, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	5
Mean	49
Std Dev	24.57



# B0L001S, U17-ch100, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U17-ch101, adc0

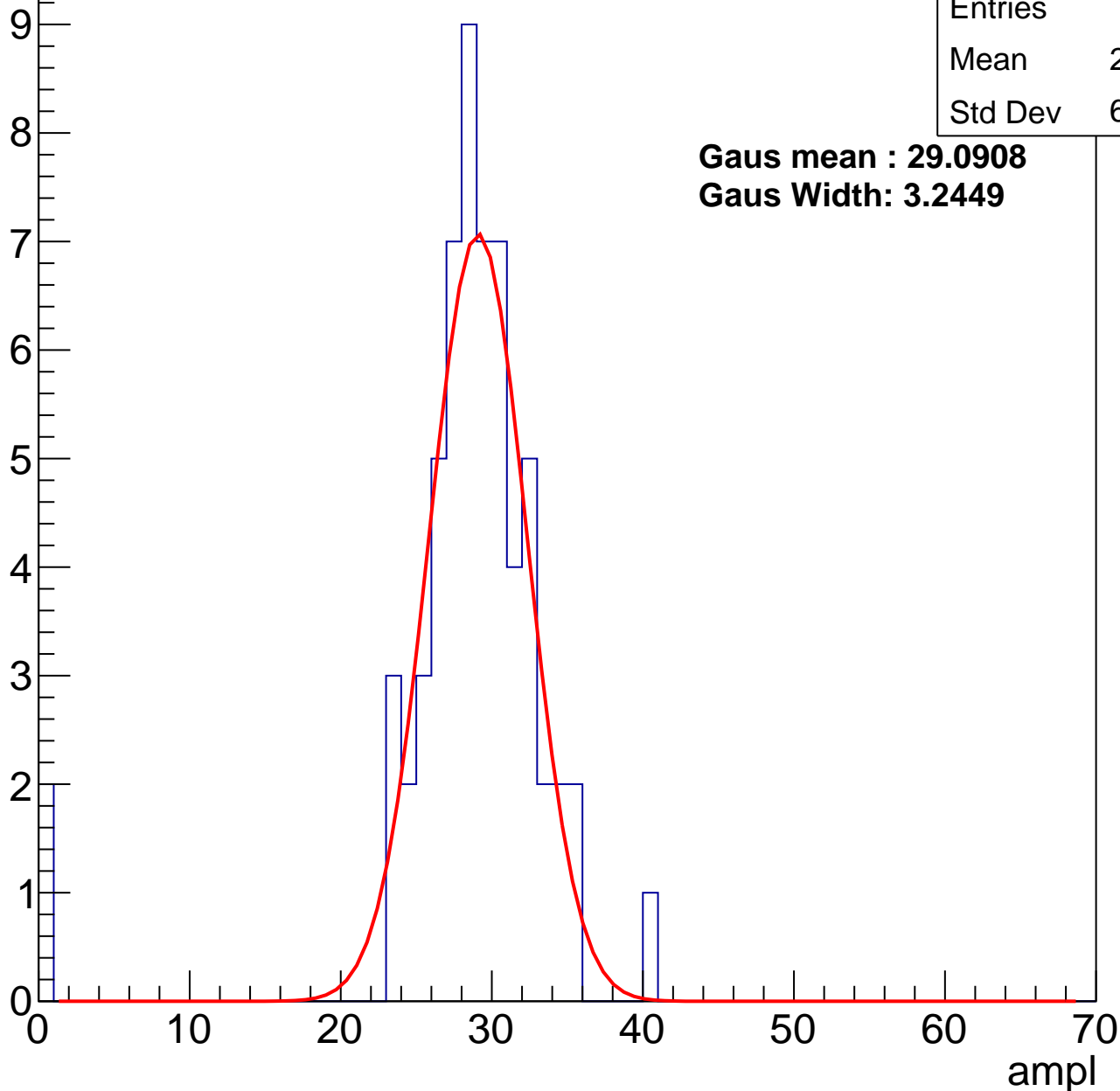
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	27.93
Std Dev	6.065

**Gaus mean : 29.0908**

**Gaus Width: 3.2449**



# B0L001S, U17-ch101, adc1

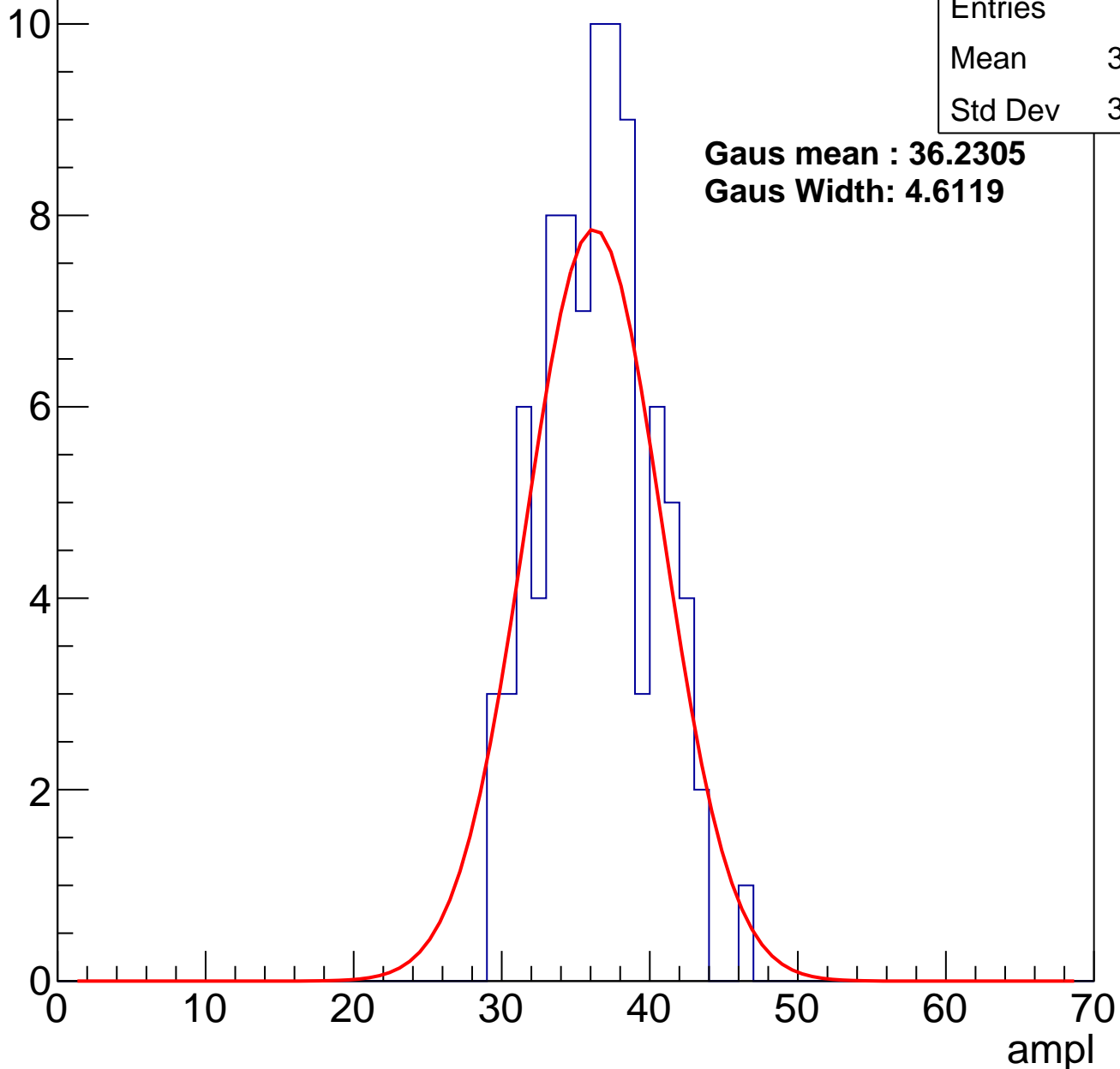
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	89
Mean	36.02
Std Dev	3.696

**Gaus mean : 36.2305**

**Gaus Width: 4.6119**

Entry



# B0L001S, U17-ch101, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	70
Mean	43.93
Std Dev	3.296

**Gaus mean : 44.7609**

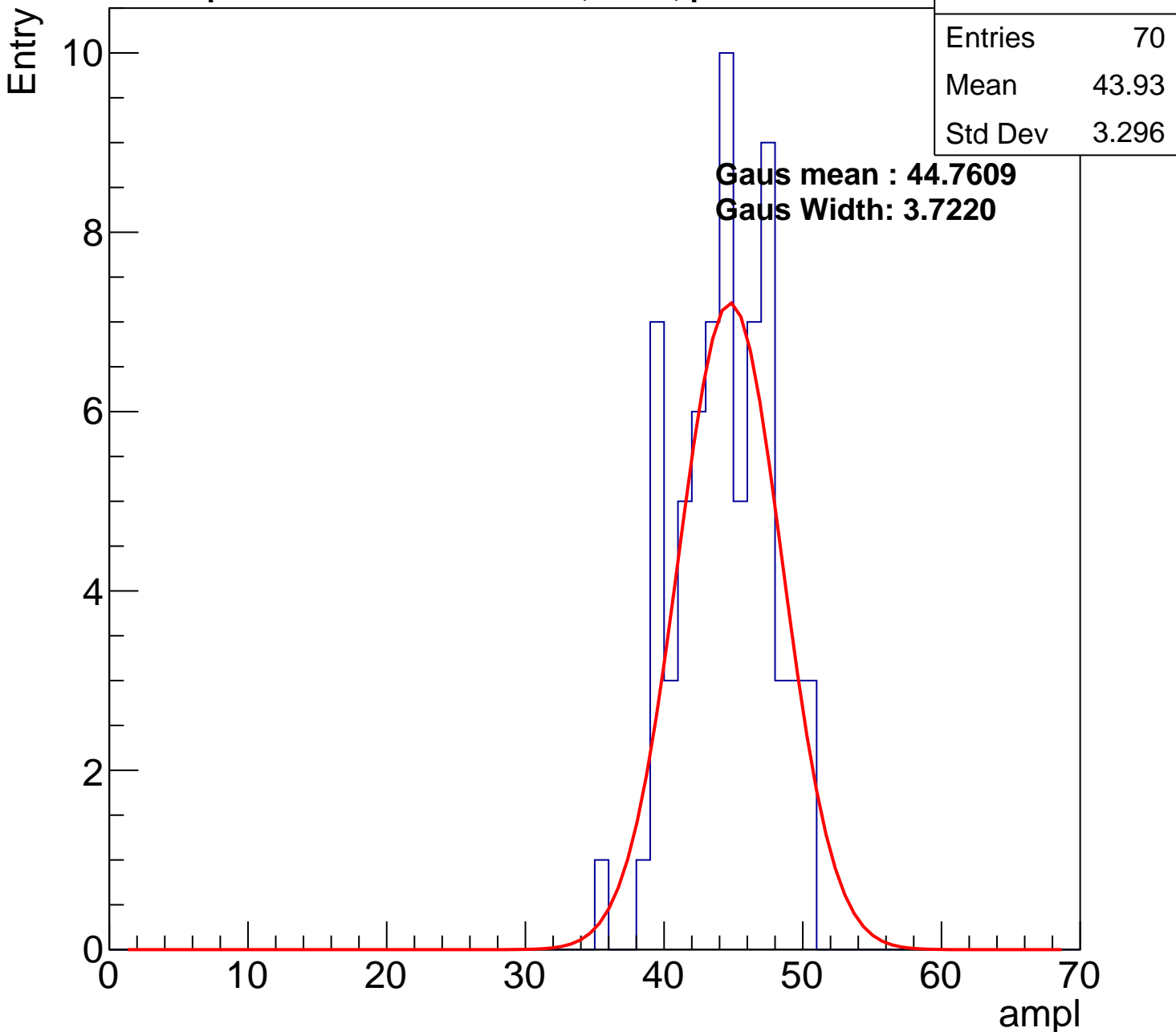
**Gaus Width: 3.7220**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

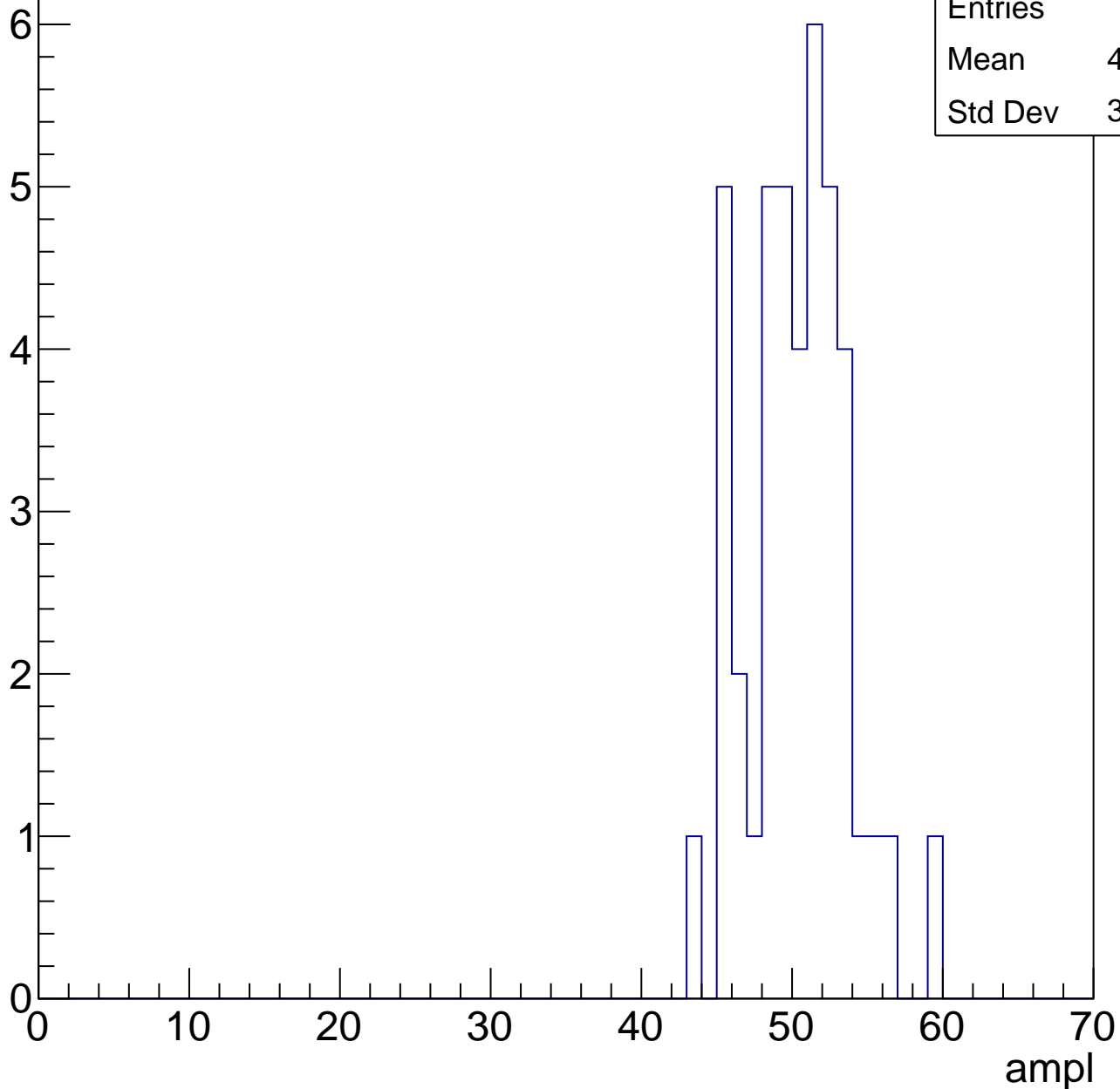


# B0L001S, U17-ch101, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

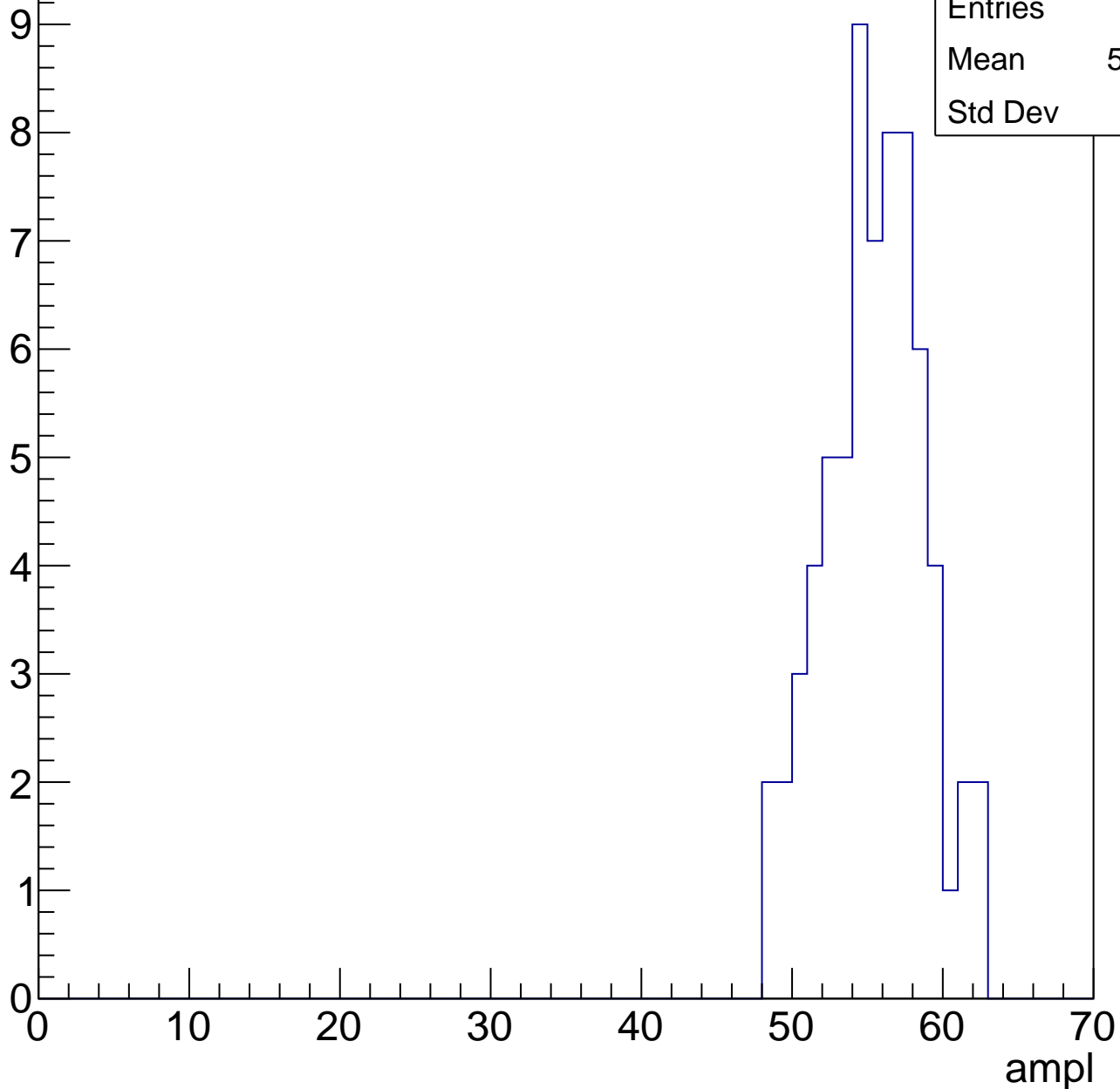
Entries	42
Mean	49.86
Std Dev	3.306



# B0L001S, U17-ch101, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

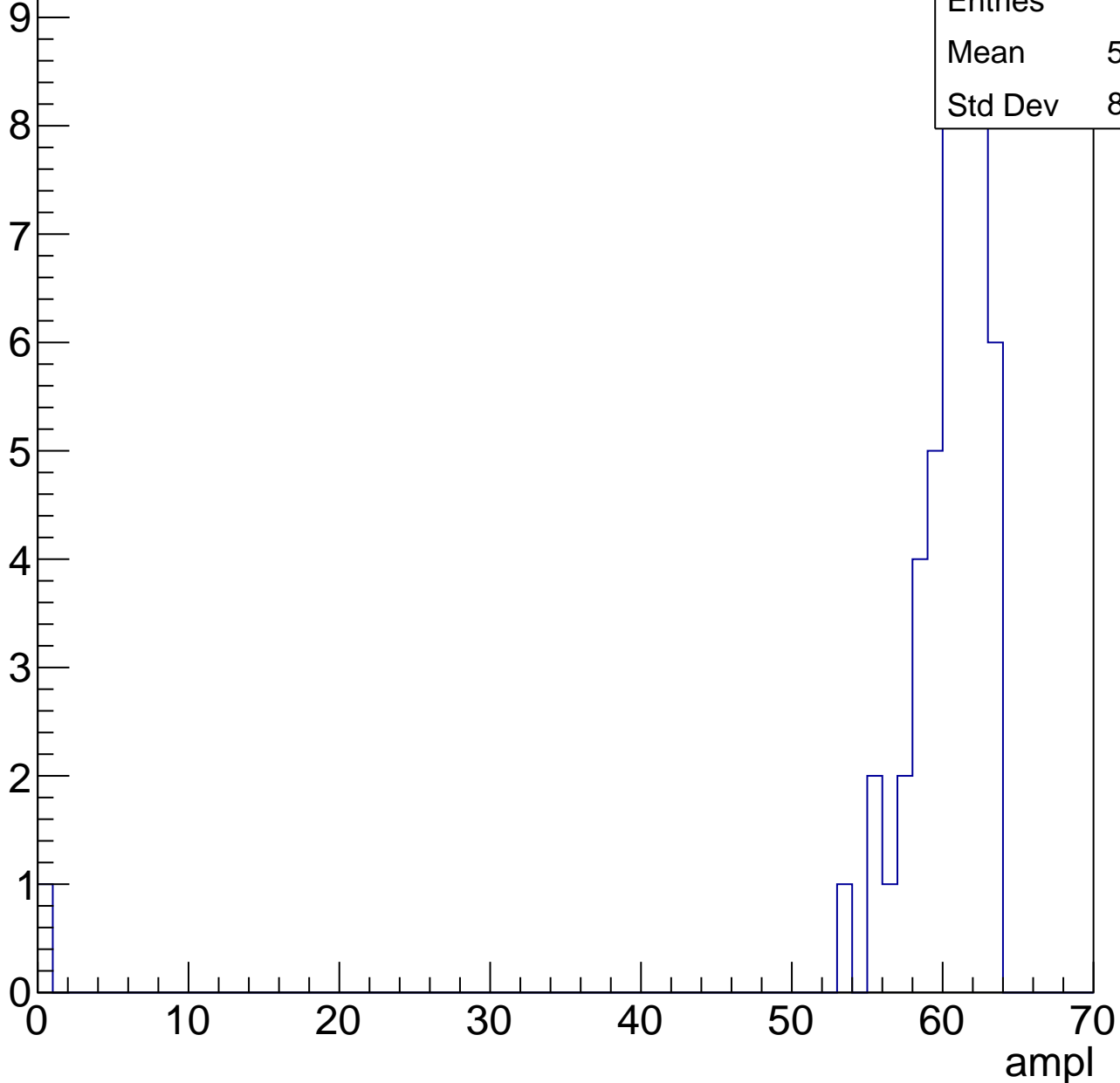


# B0L001S, U17-ch101, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	47
Mean	58.77
Std Dev	8.964



# B0L001S, U17-ch101, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch101, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



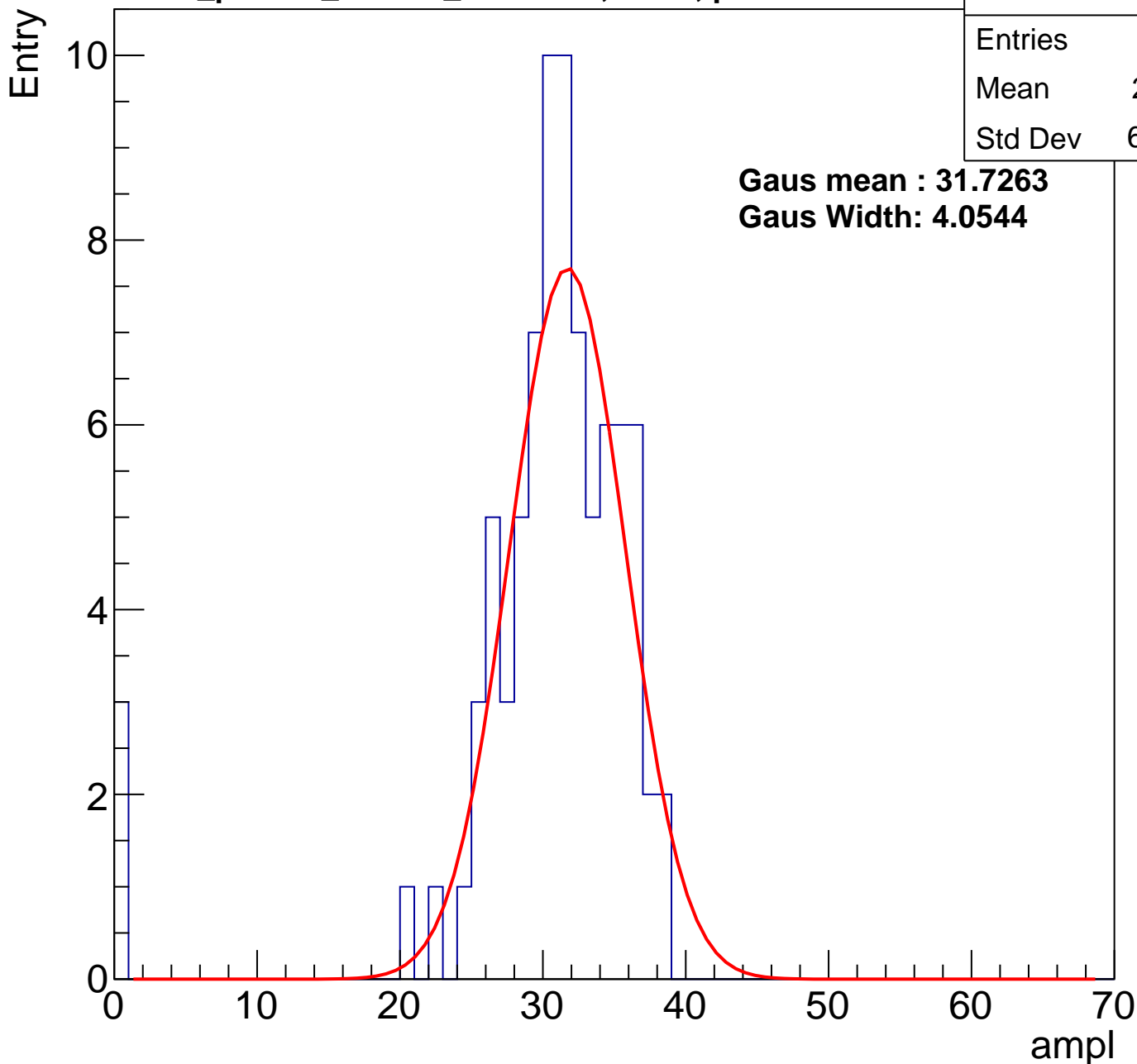
# B0L001S, U17-ch102, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	83
Mean	29.81
Std Dev	6.834

**Gaus mean : 31.7263**

**Gaus Width: 4.0544**



# B0L001S, U17-ch102, adc1

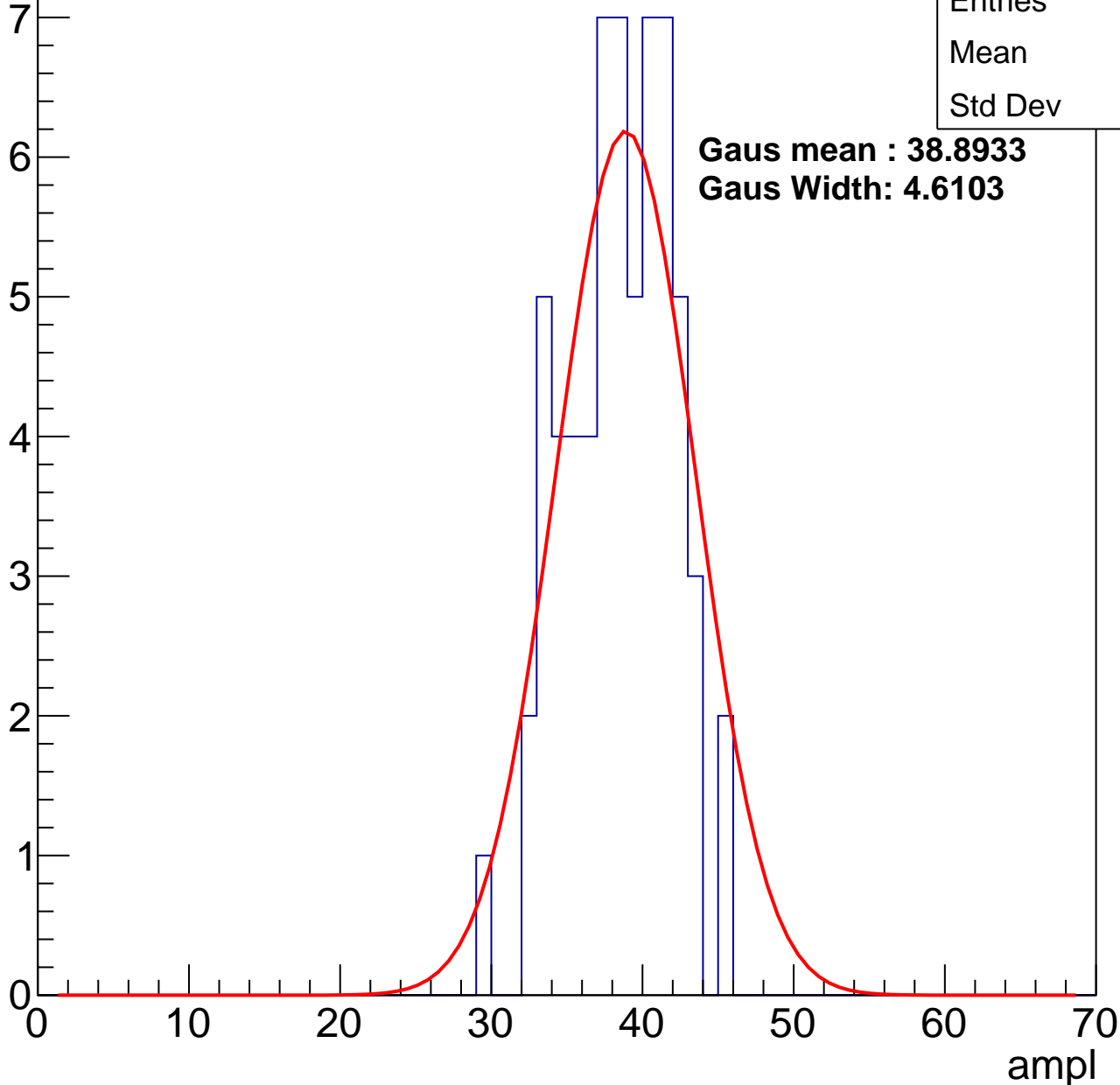
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	38
Std Dev	3.45

**Gaus mean : 38.8933**

**Gaus Width: 4.6103**



# B0L001S, U17-ch102, adc2

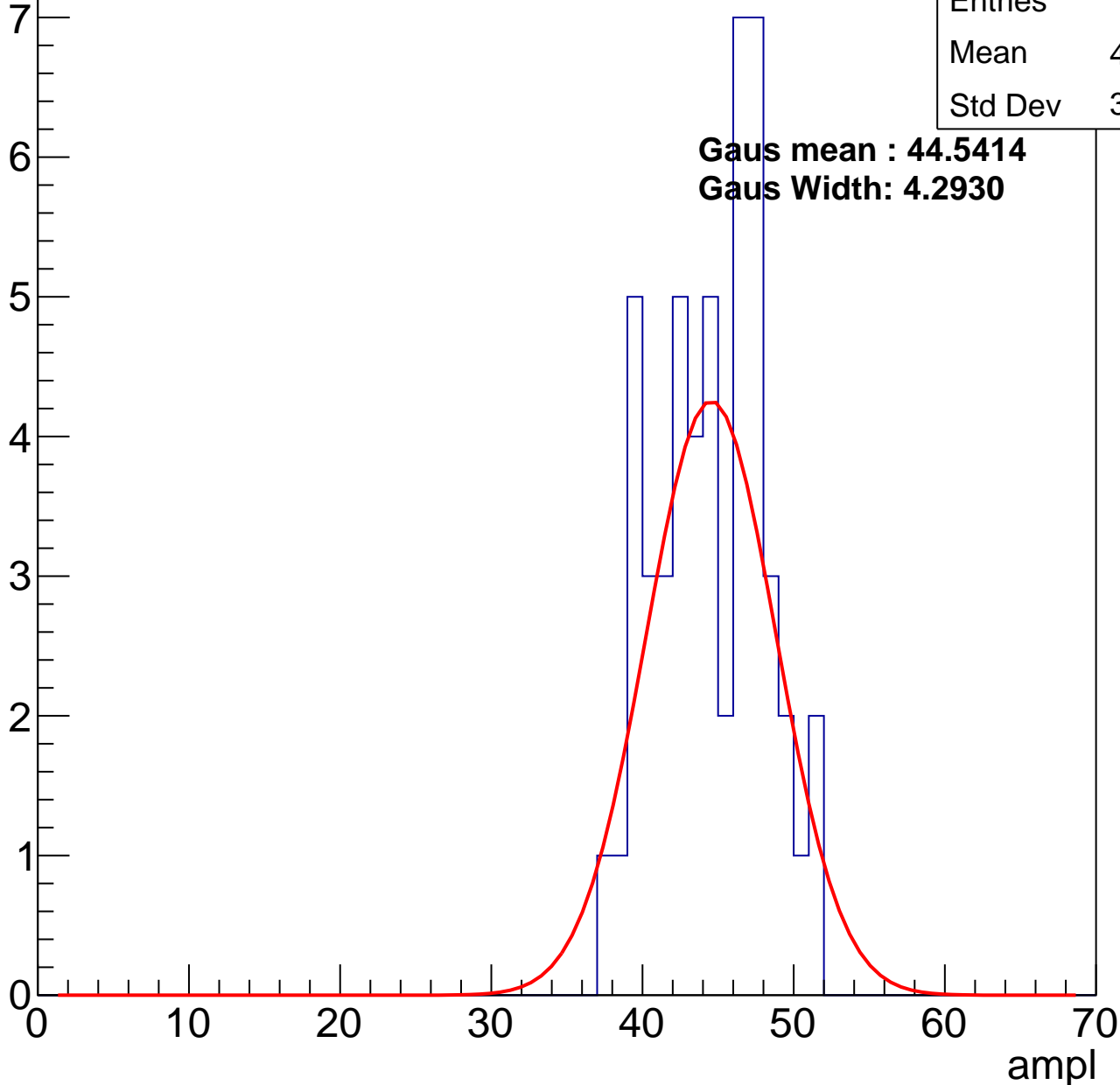
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	51
Mean	44.12
Std Dev	3.524

**Gaus mean : 44.5414**

**Gaus Width: 4.2930**

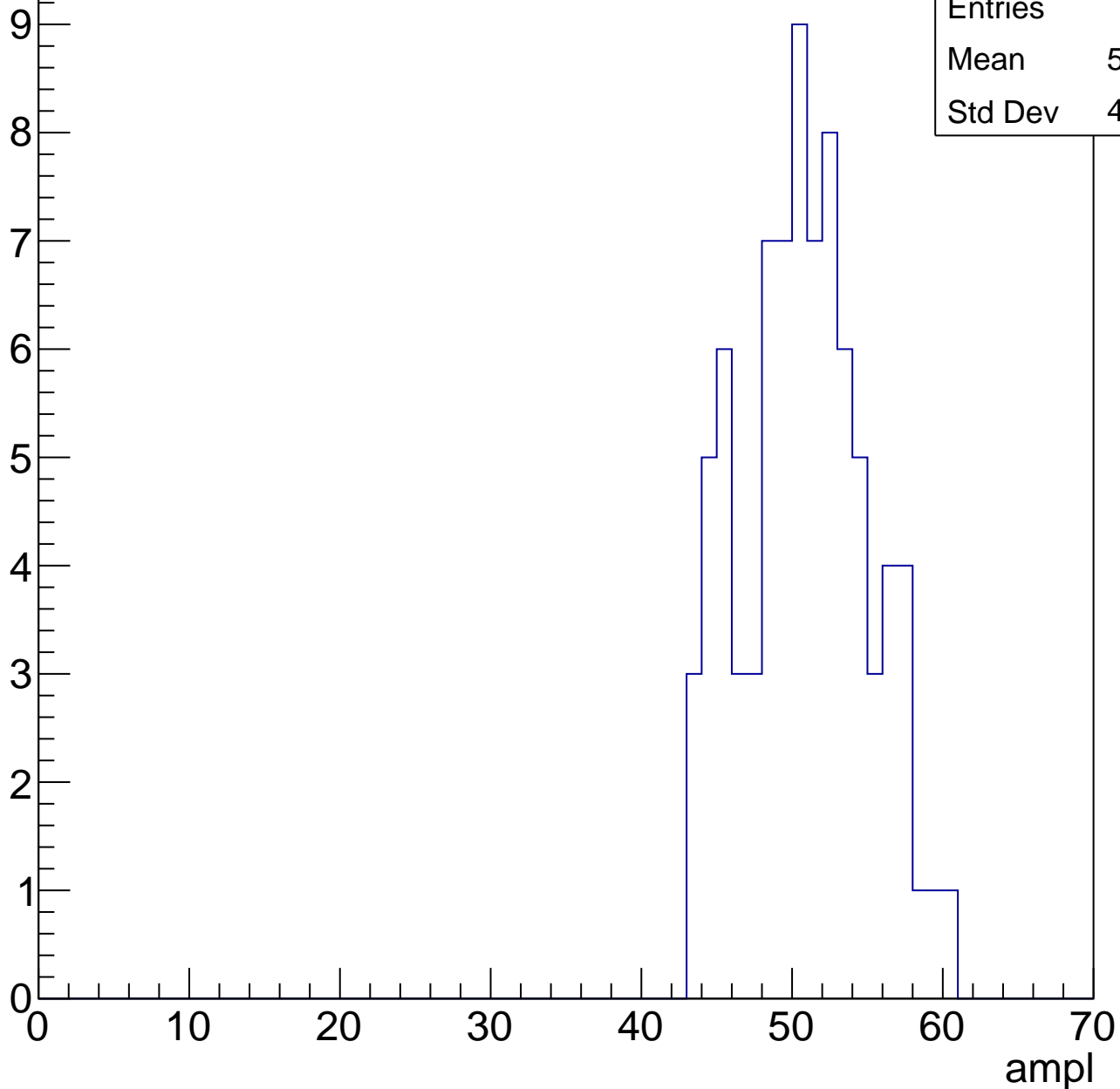


# B0L001S, U17-ch102, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	83
Mean	50.39
Std Dev	4.118

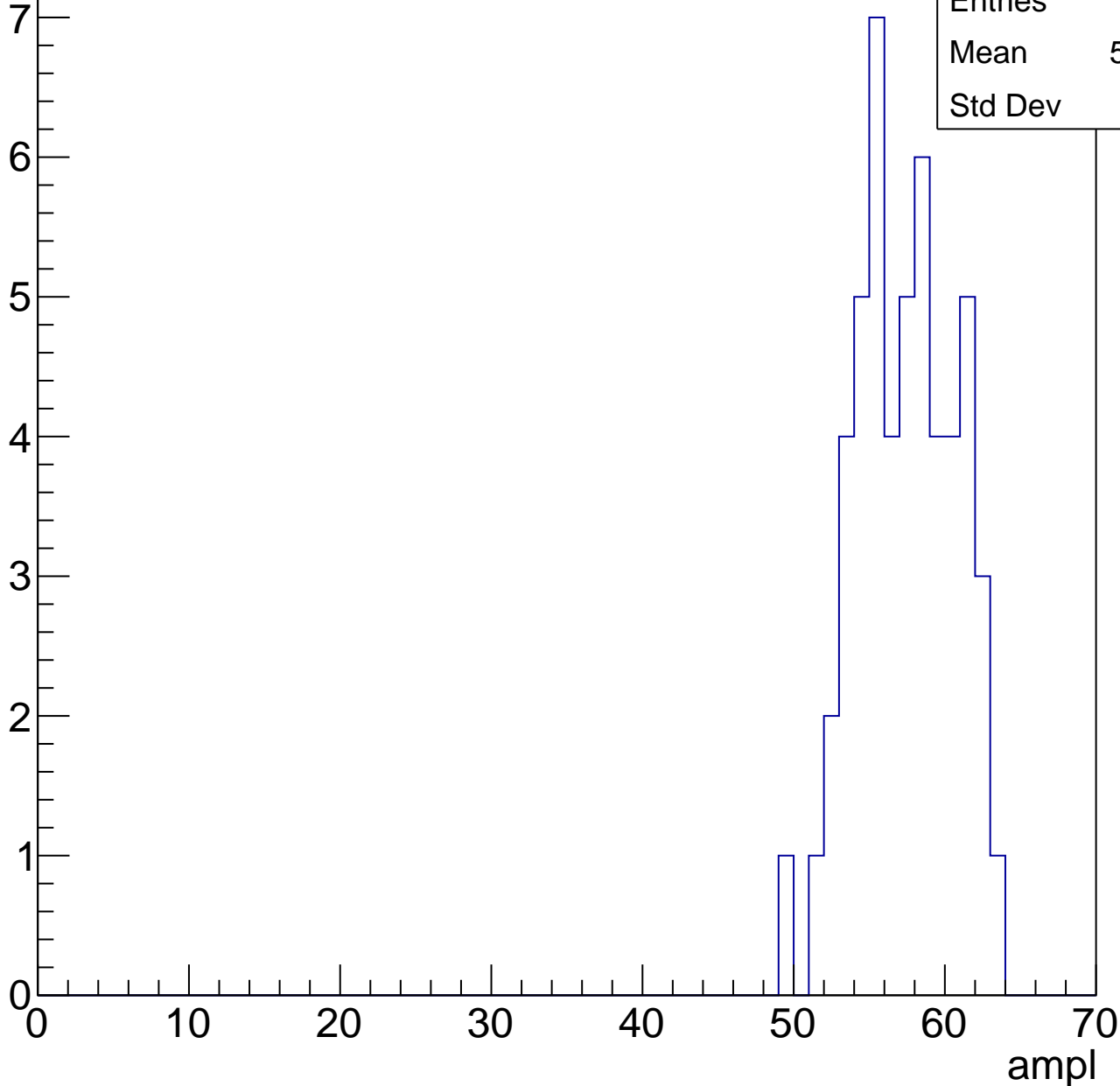


# B0L001S, U17-ch102, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	56.88
Std Dev	3.22

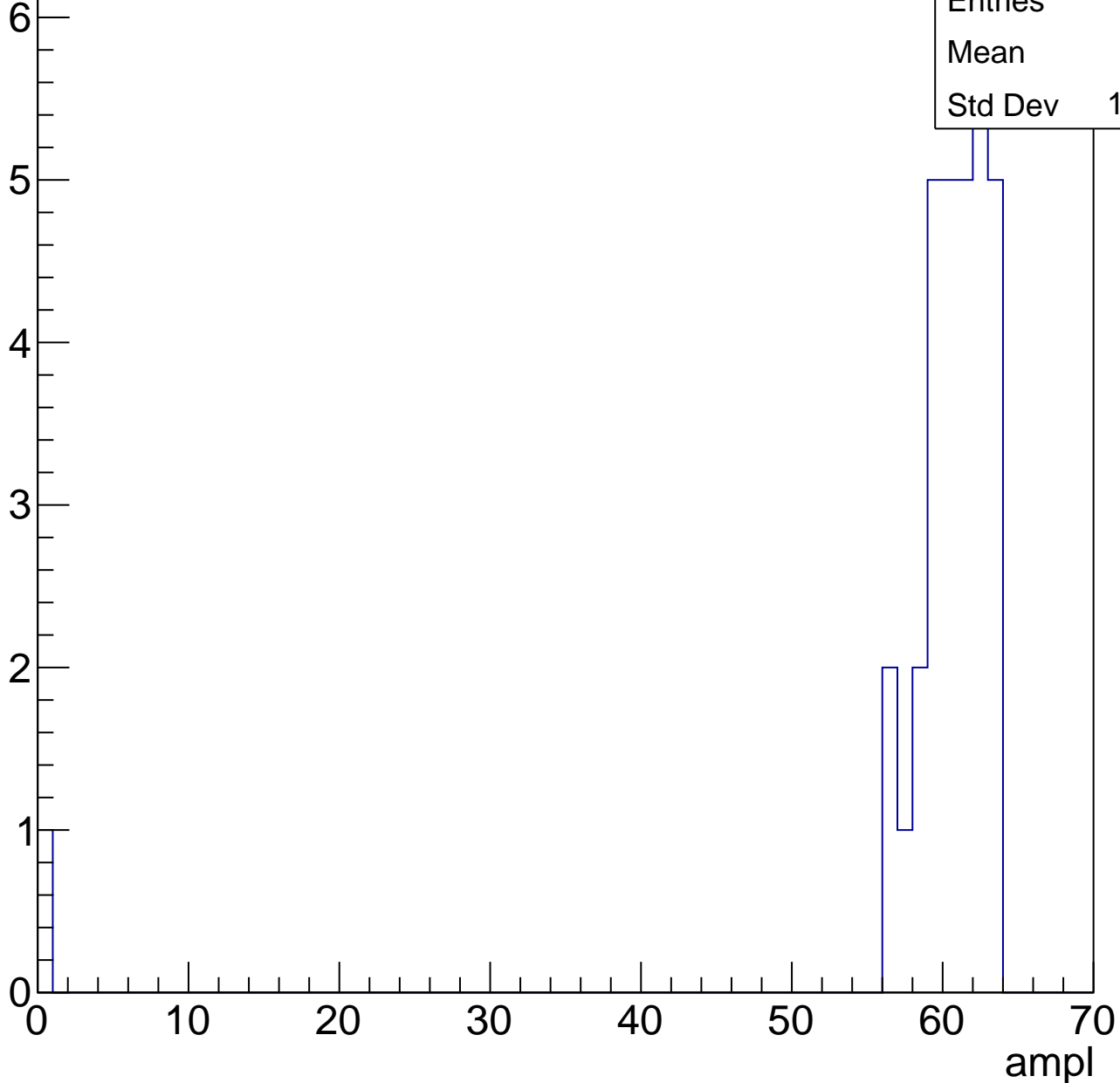


# B0L001S, U17-ch102, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

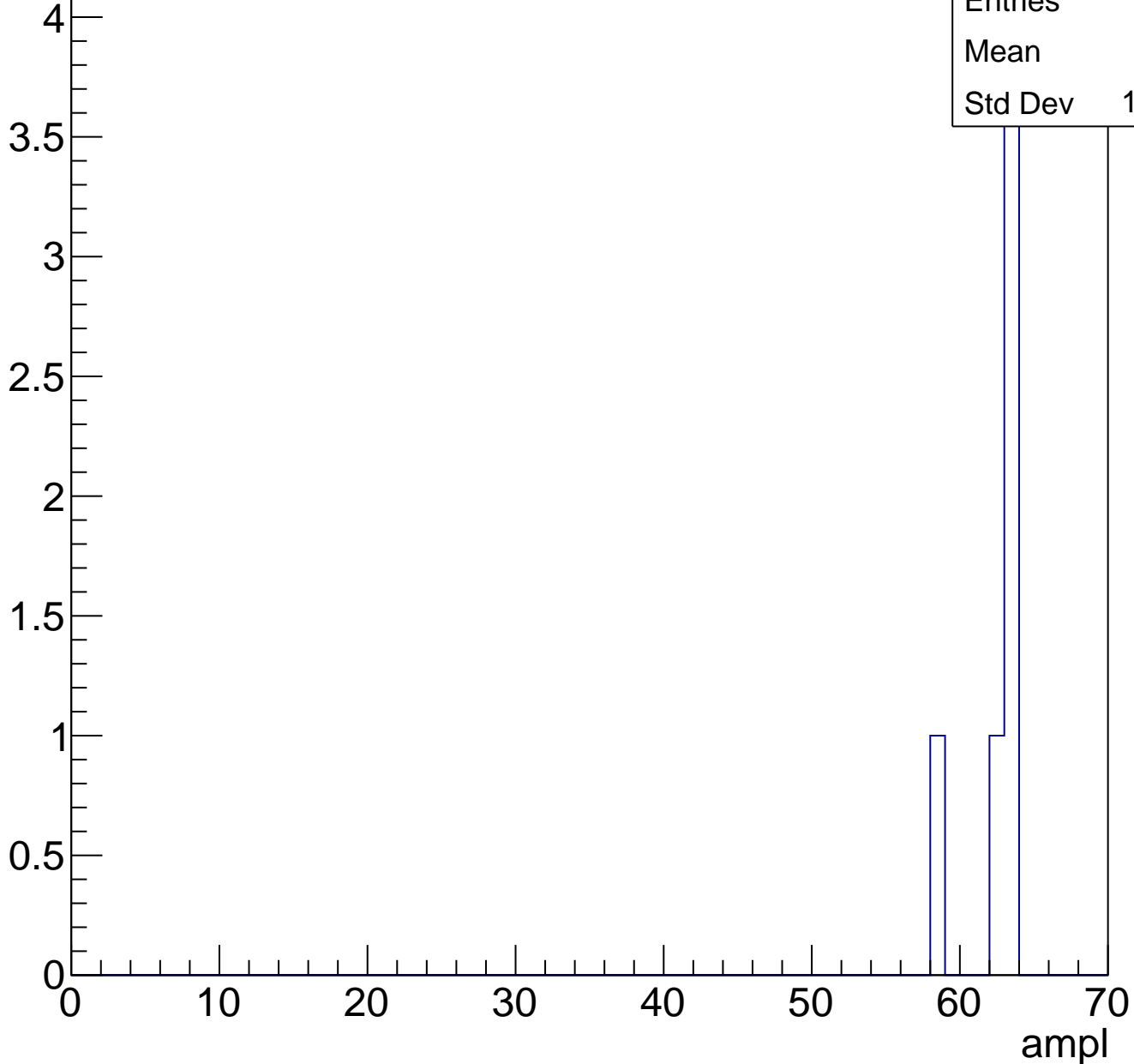
Entries	32
Mean	58.5
Std Dev	10.69



# B0L001S, U17-ch102, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch102, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U17-ch103, adc0

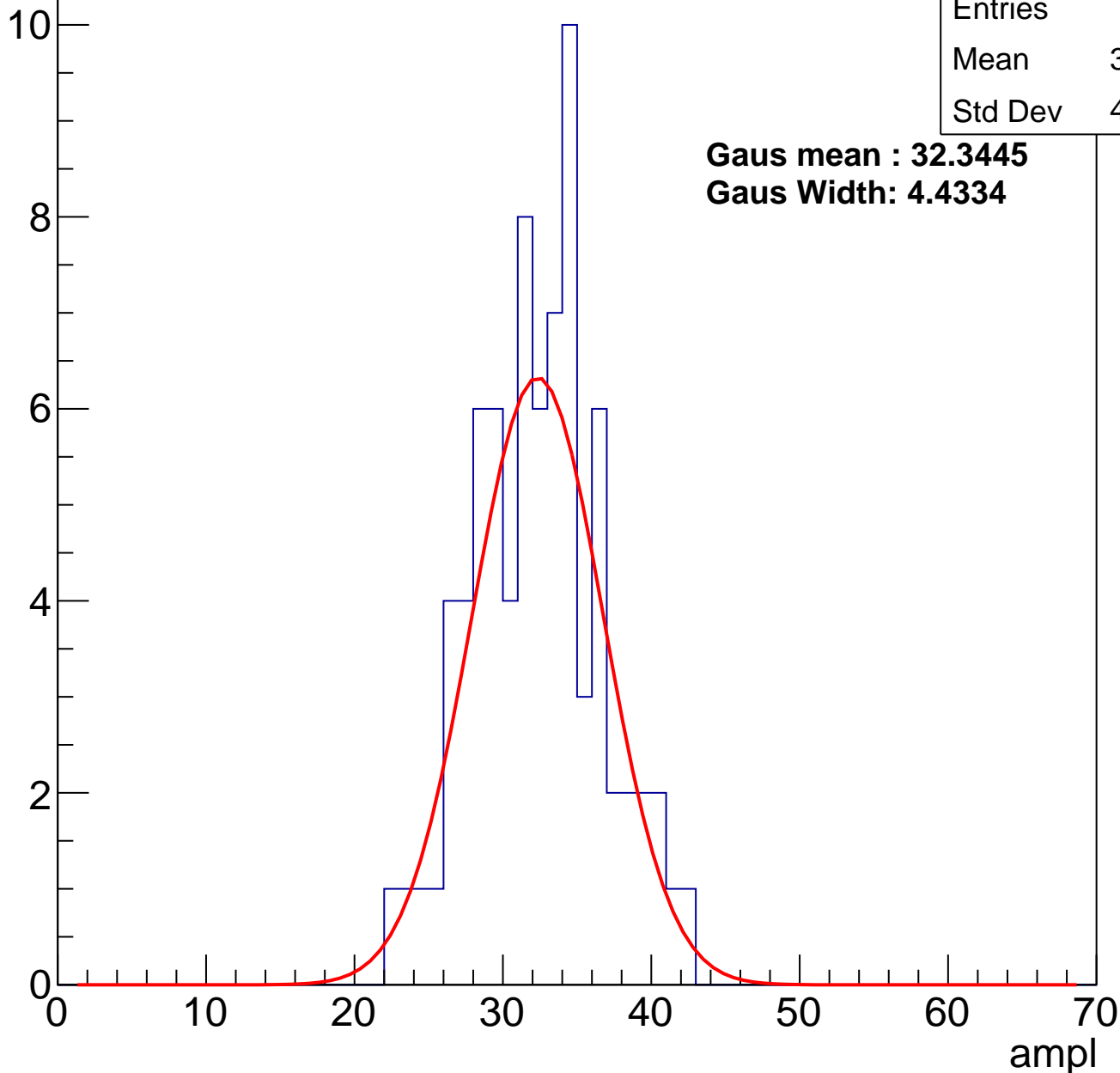
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	78
Mean	31.94
Std Dev	4.253

**Gaus mean : 32.3445**

**Gaus Width: 4.4334**

Entry



# B0L001S, U17-ch103, adc1

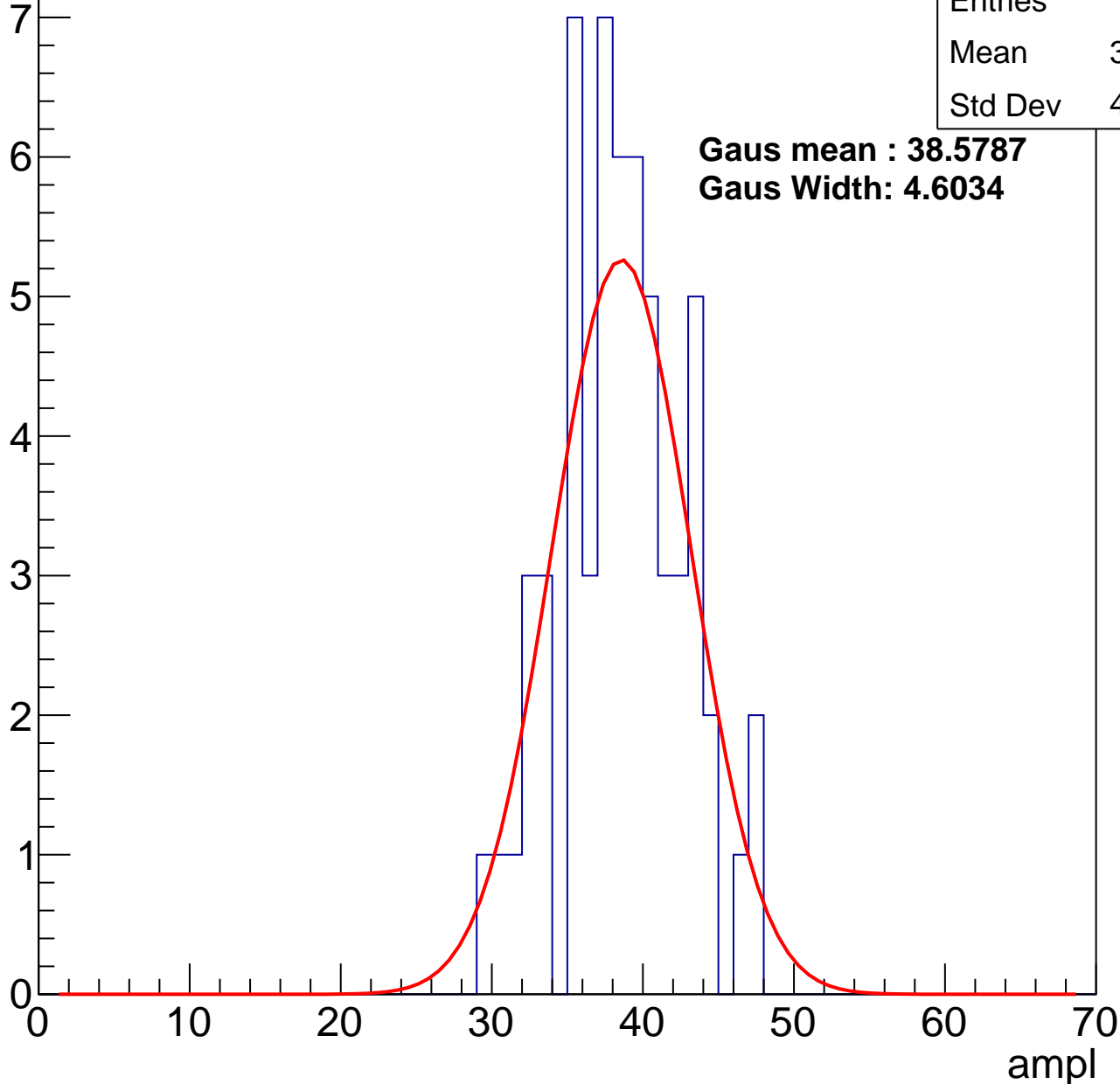
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	38.15
Std Dev	4.079

**Gaus mean : 38.5787**

**Gaus Width: 4.6034**



# B0L001S, U17-ch103, adc2

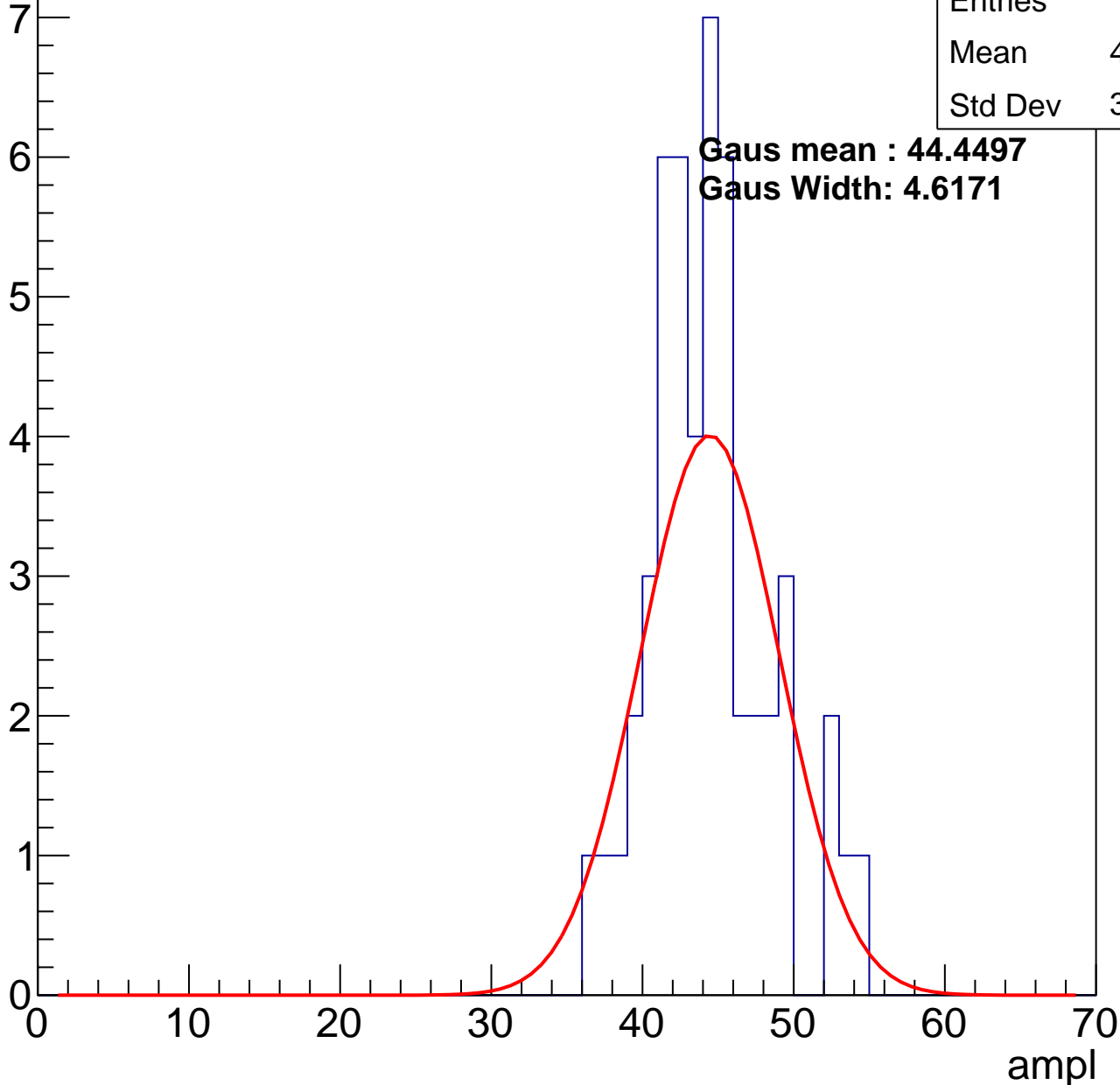
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	50
Mean	43.94
Std Dev	3.942

**Gaus mean : 44.4497**

**Gaus Width: 4.6171**

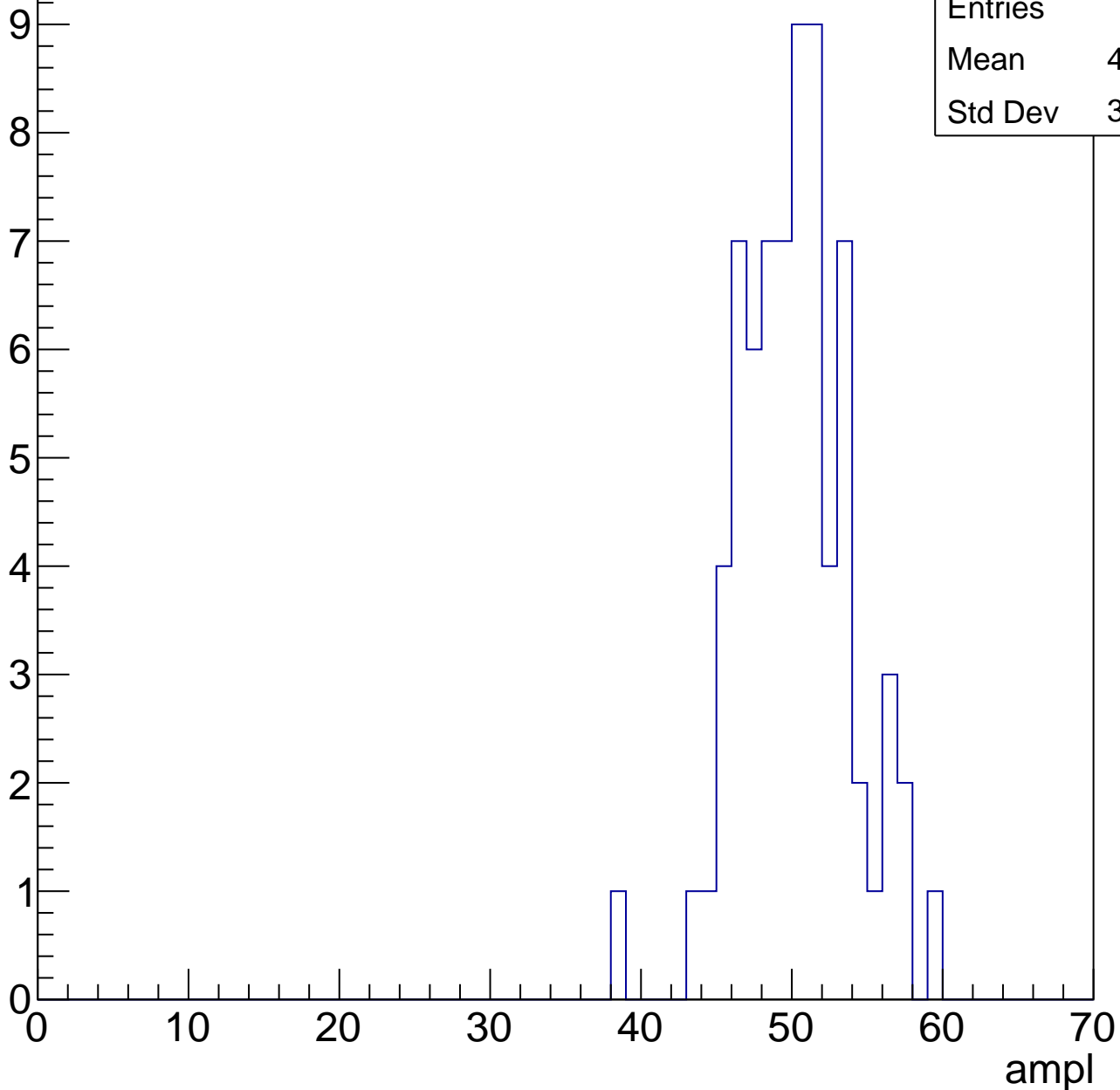


# B0L001S, U17-ch103, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	49.72
Std Dev	3.645

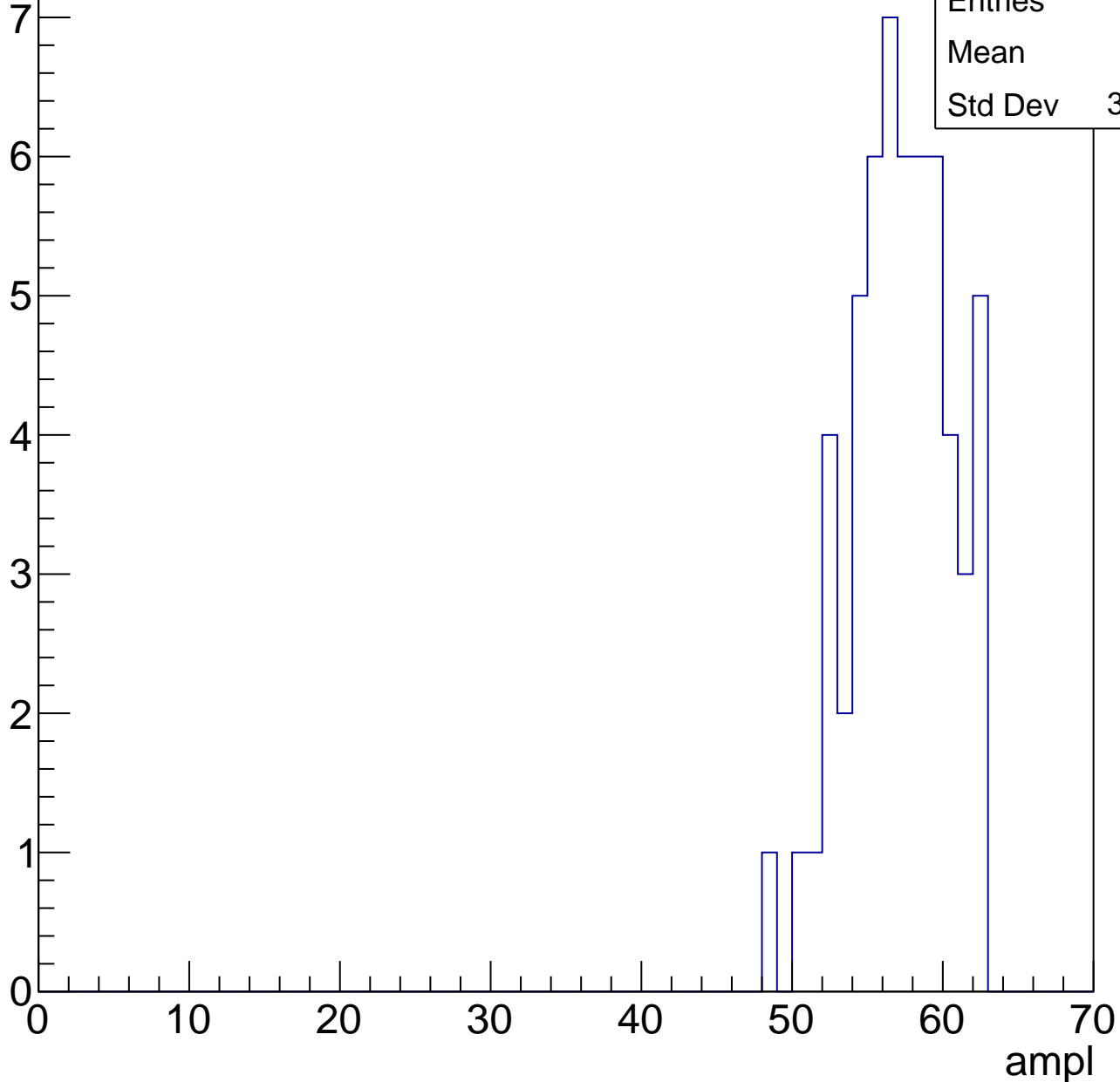


# B0L001S, U17-ch103, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

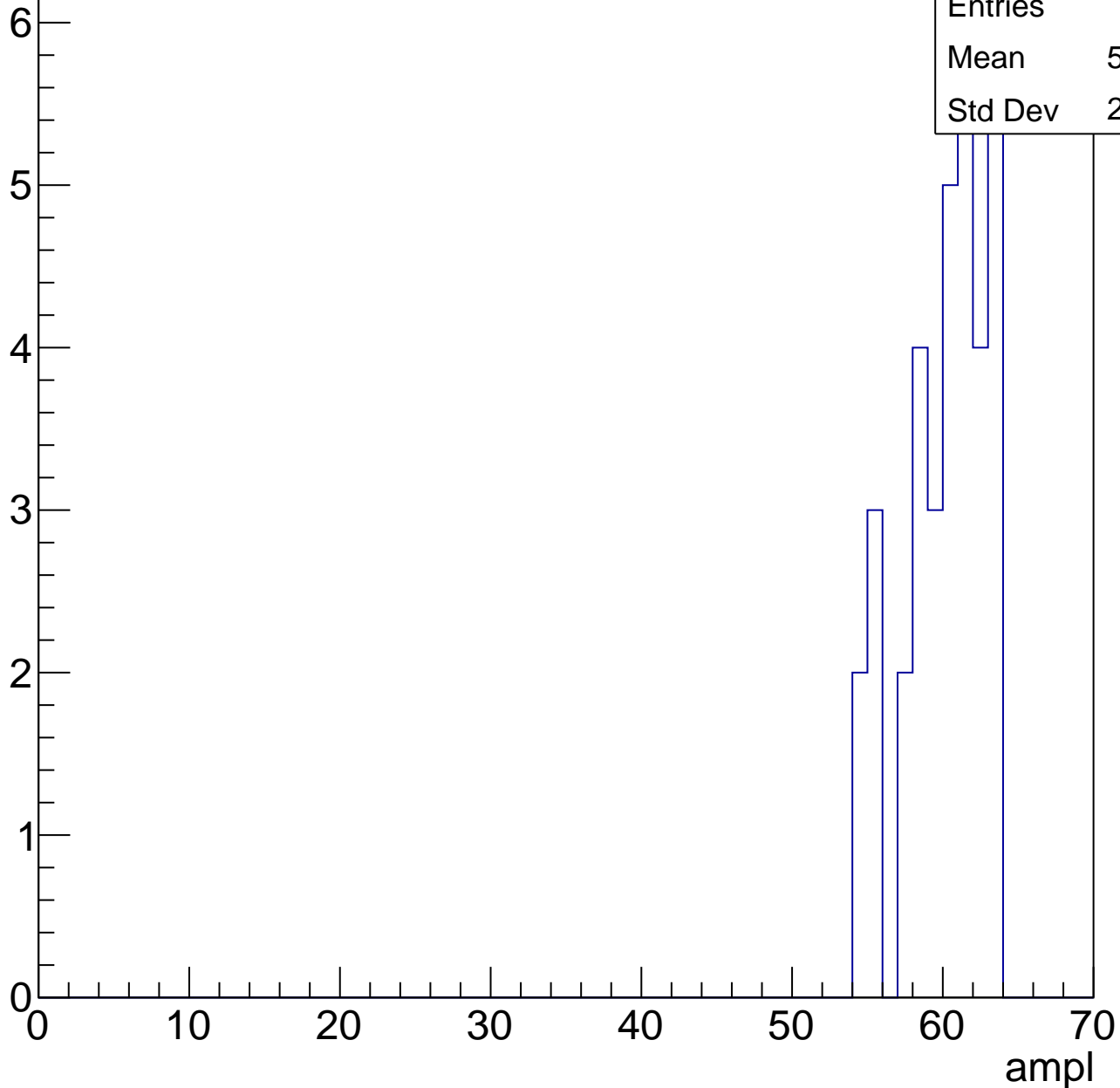
Entries	57
Mean	56.7
Std Dev	3.266



# B0L001S, U17-ch103, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

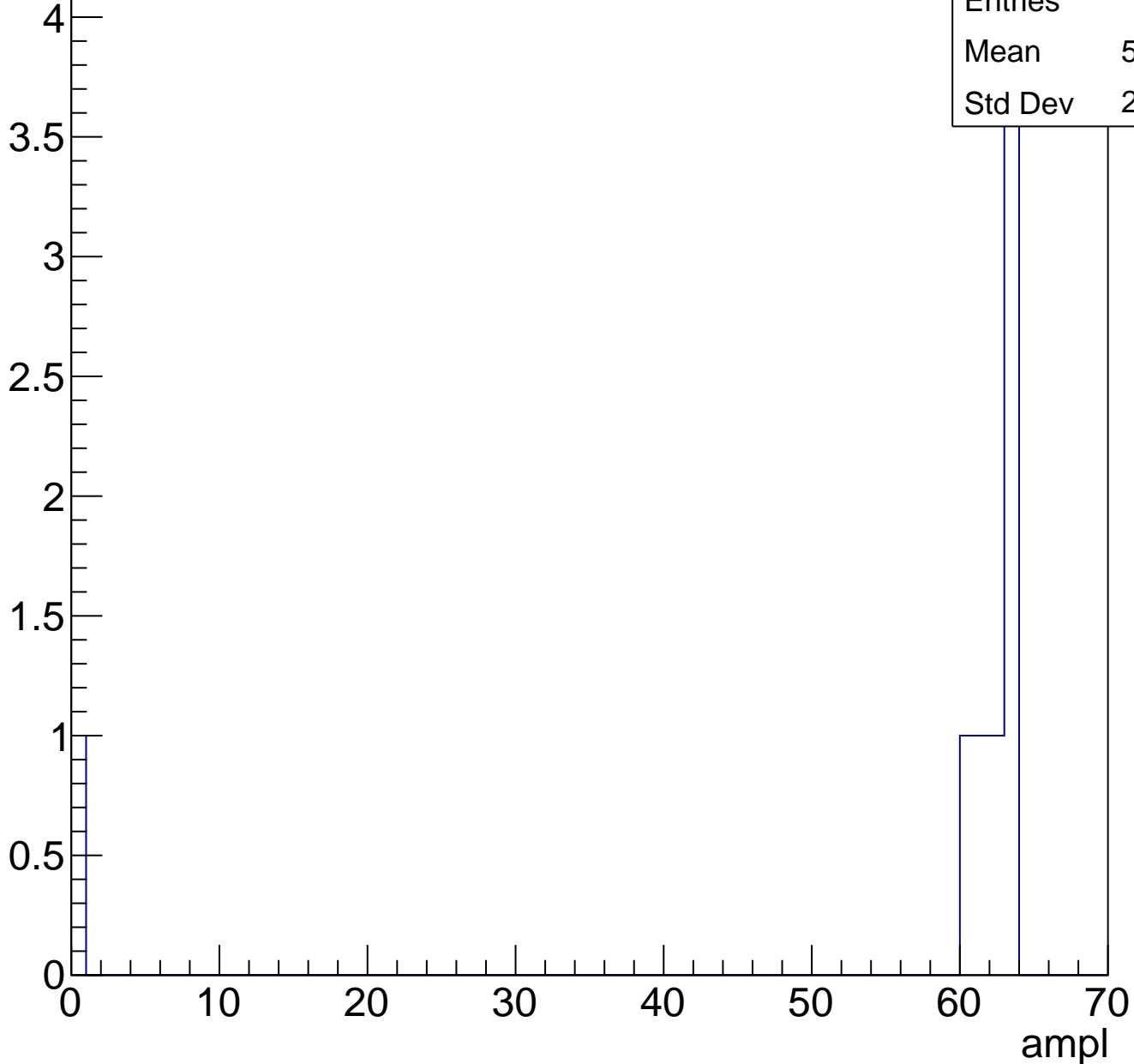
Entry



# B0L001S, U17-ch103, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch103, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	3
Mean	0
Std Dev	0

# B0L001S, U17-ch104, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	93
Mean	30.7
Std Dev	5.001

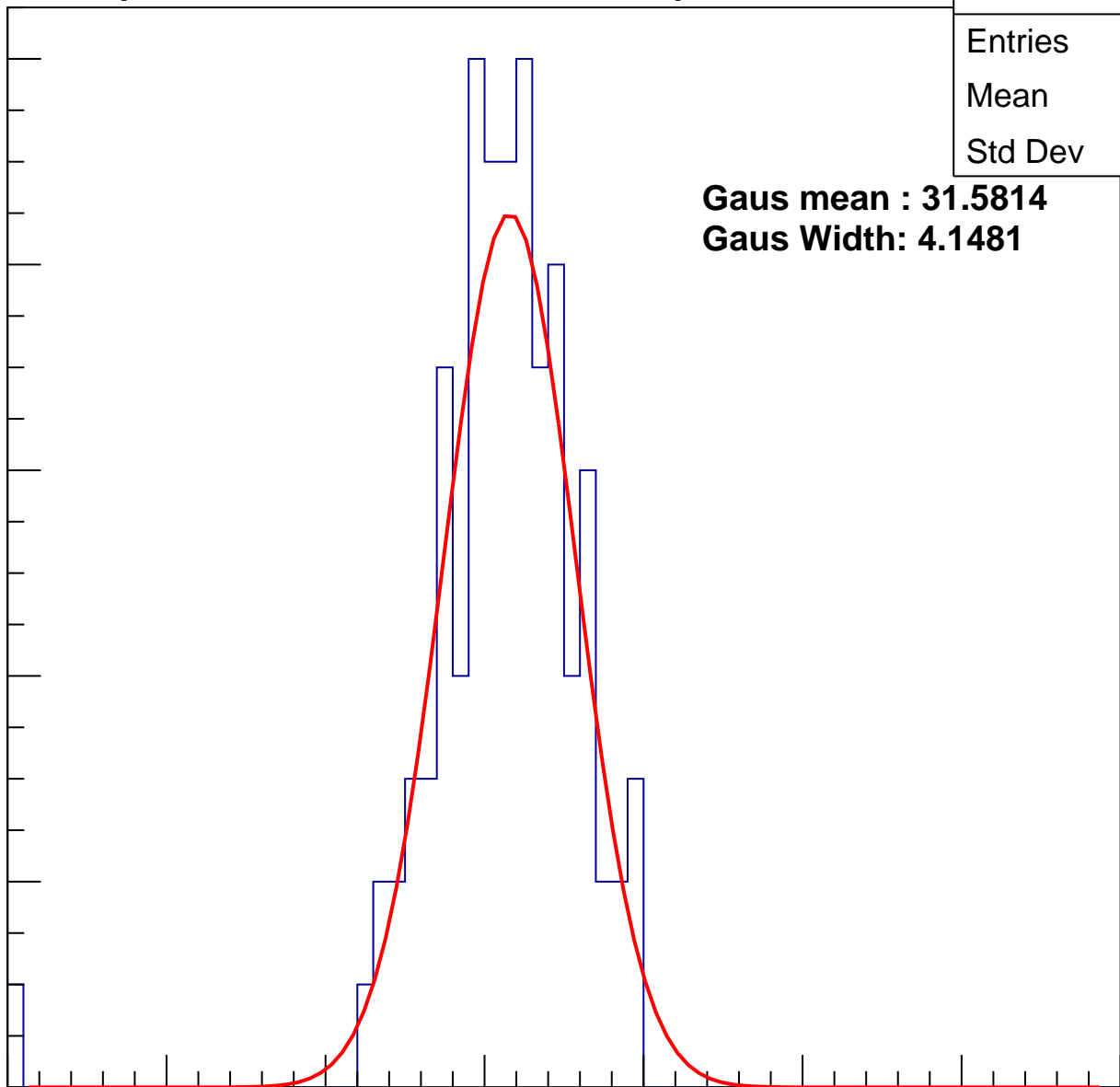
**Gaus mean : 31.5814**  
**Gaus Width: 4.1481**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U17-ch104, adc1

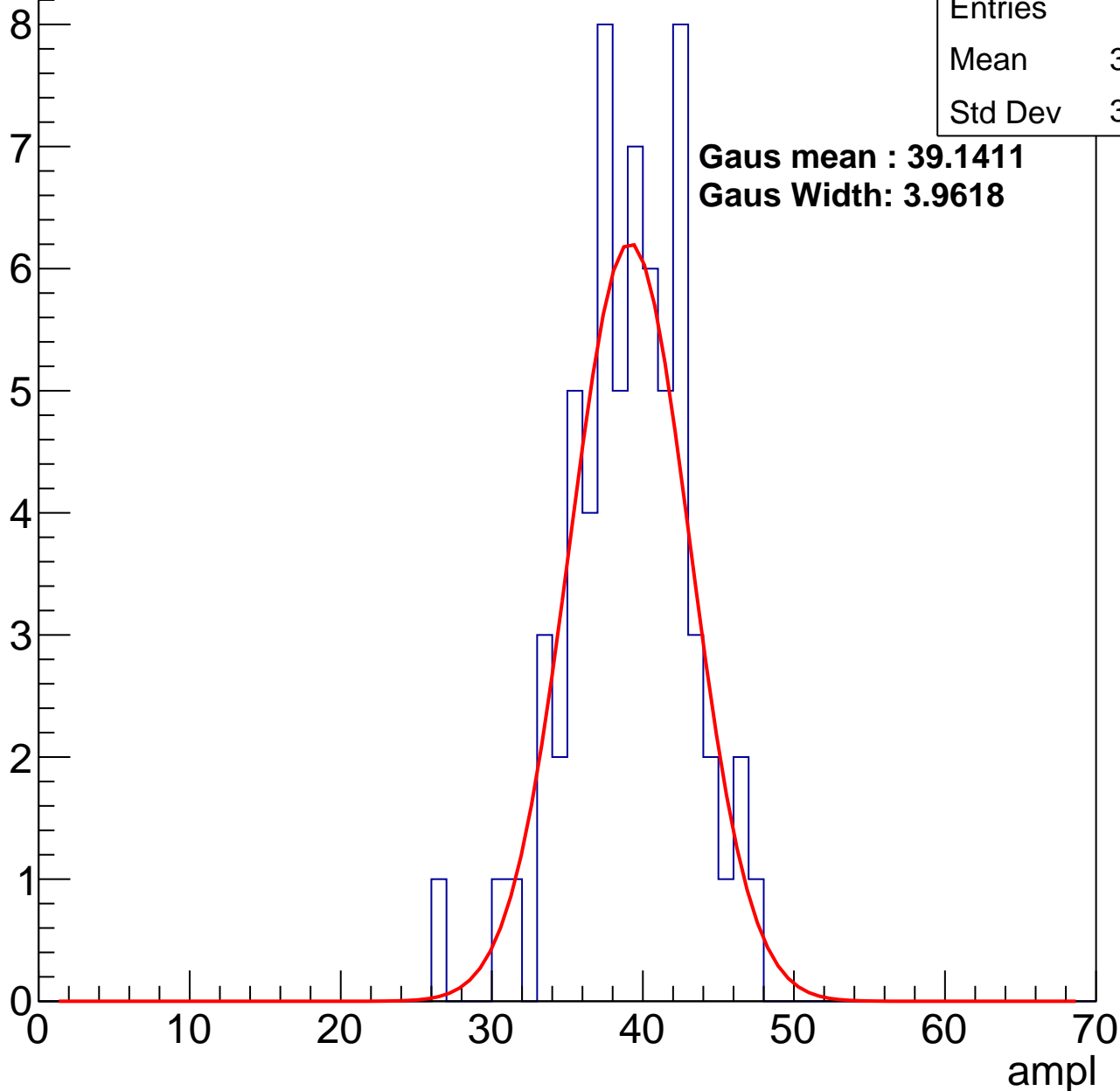
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	38.68
Std Dev	3.946

**Gaus mean : 39.1411**

**Gaus Width: 3.9618**



# B0L001S, U17-ch104, adc2

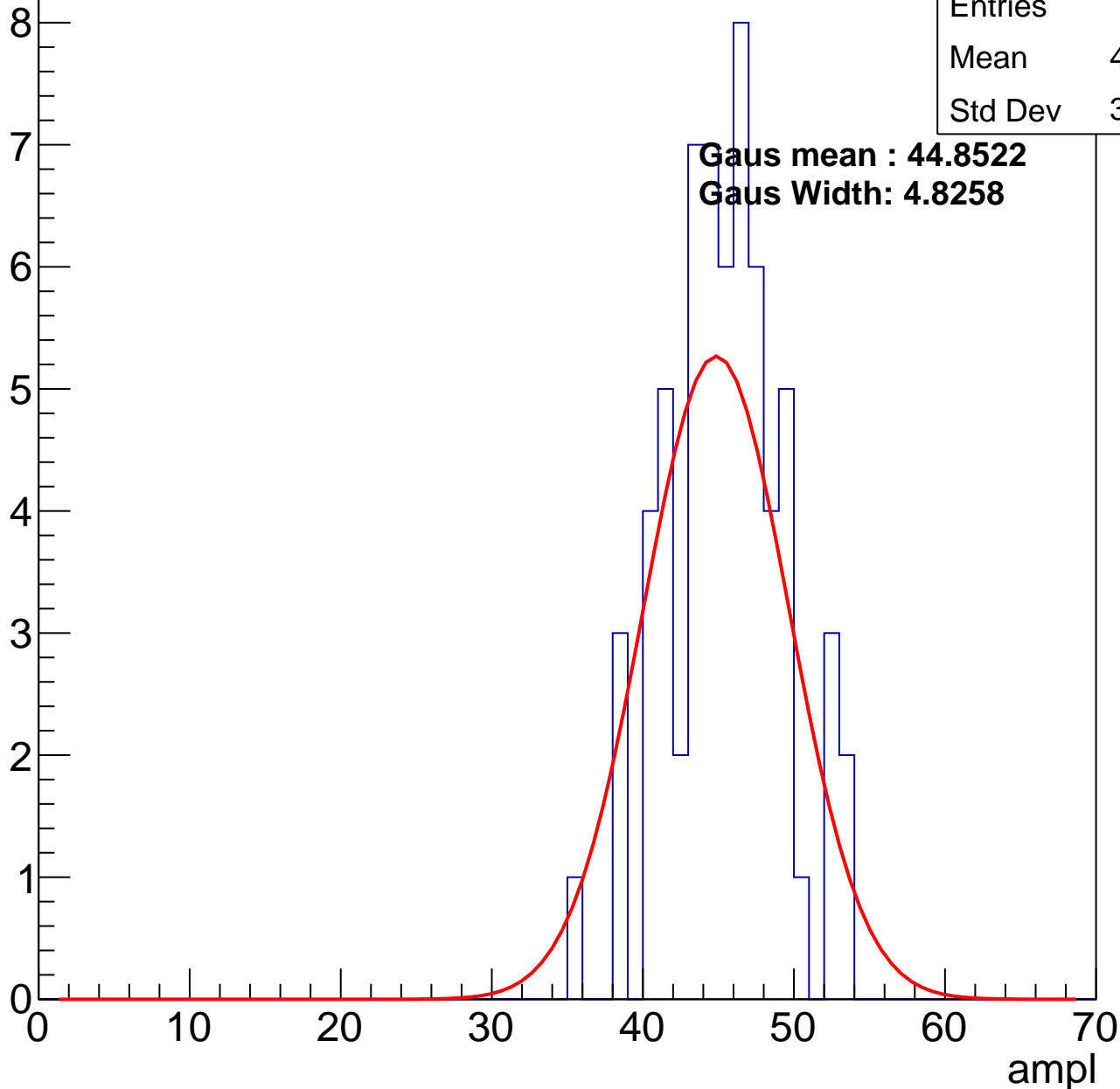
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	44.94
Std Dev	3.807

**Gaus mean : 44.8522**

**Gaus Width: 4.8258**

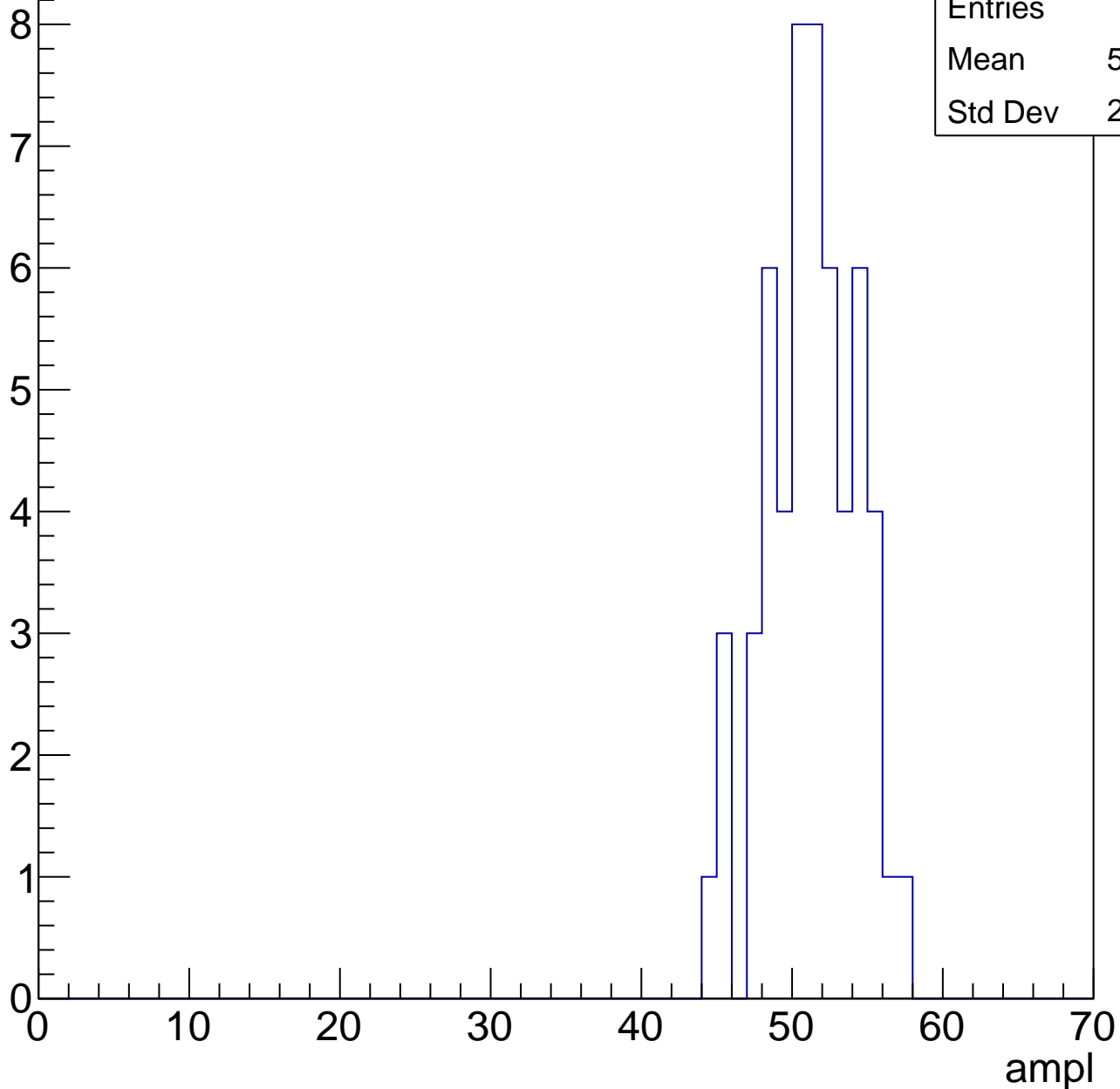


# B0L001S, U17-ch104, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	50.78
Std Dev	2.958

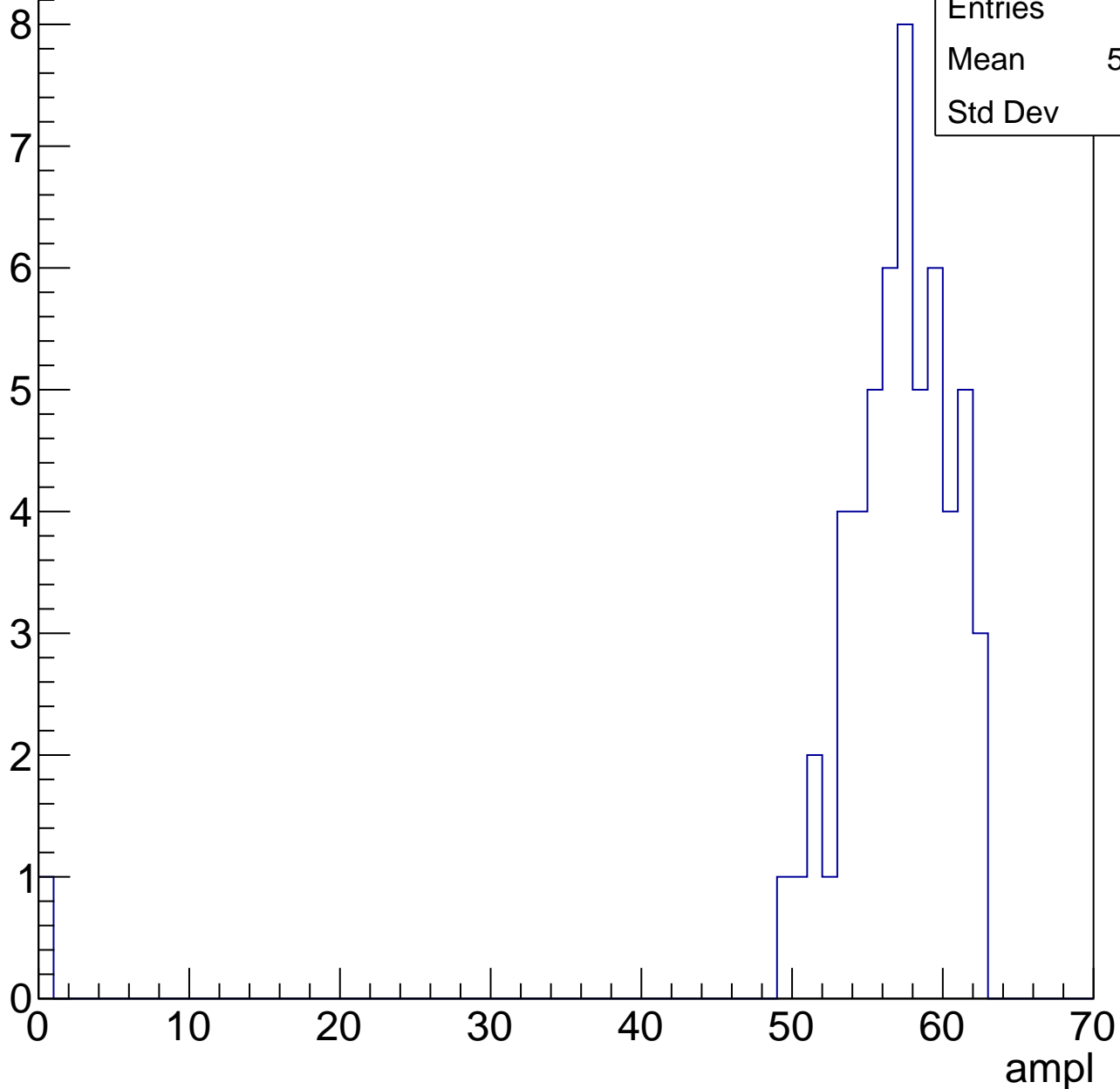


# B0L001S, U17-ch104, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	55.77
Std Dev	8.15

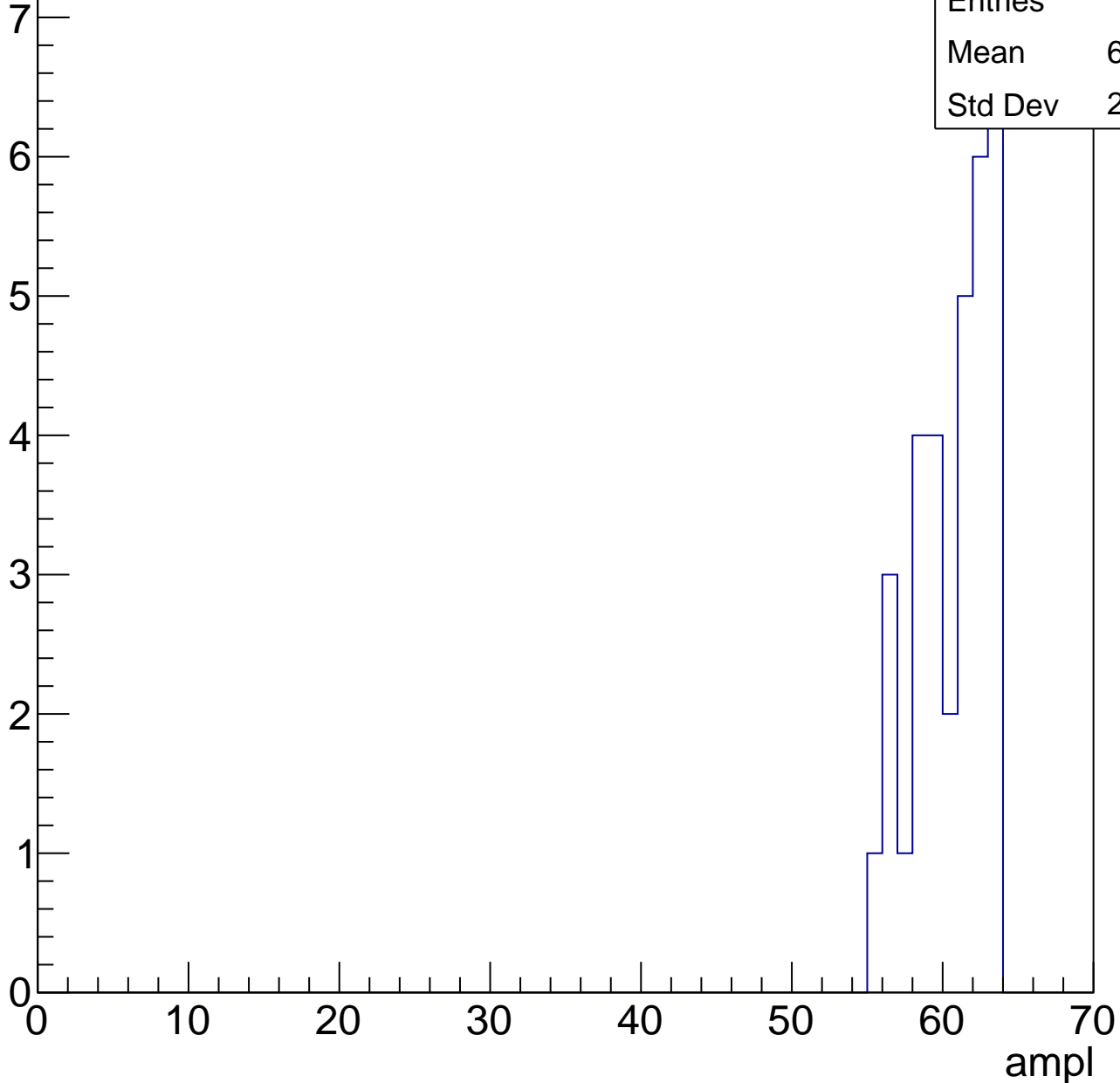


# B0L001S, U17-ch104, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	33
Mean	60.18
Std Dev	2.418



# B0L001S, U17-ch104, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

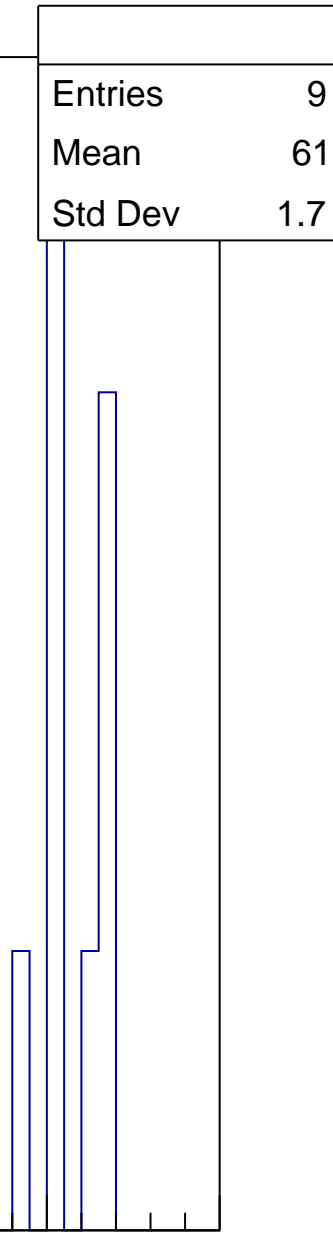
Entry

4  
3.5  
3  
2.5  
2  
1.5  
1  
0.5  
0

Entries	9
Mean	61
Std Dev	1.7

ampl

0 10 20 30 40 50 60 70





# B0L001S, U17-ch104, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U17-ch105, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	91
Mean	29.84
Std Dev	4.9

**Gaus mean : 30.3803**

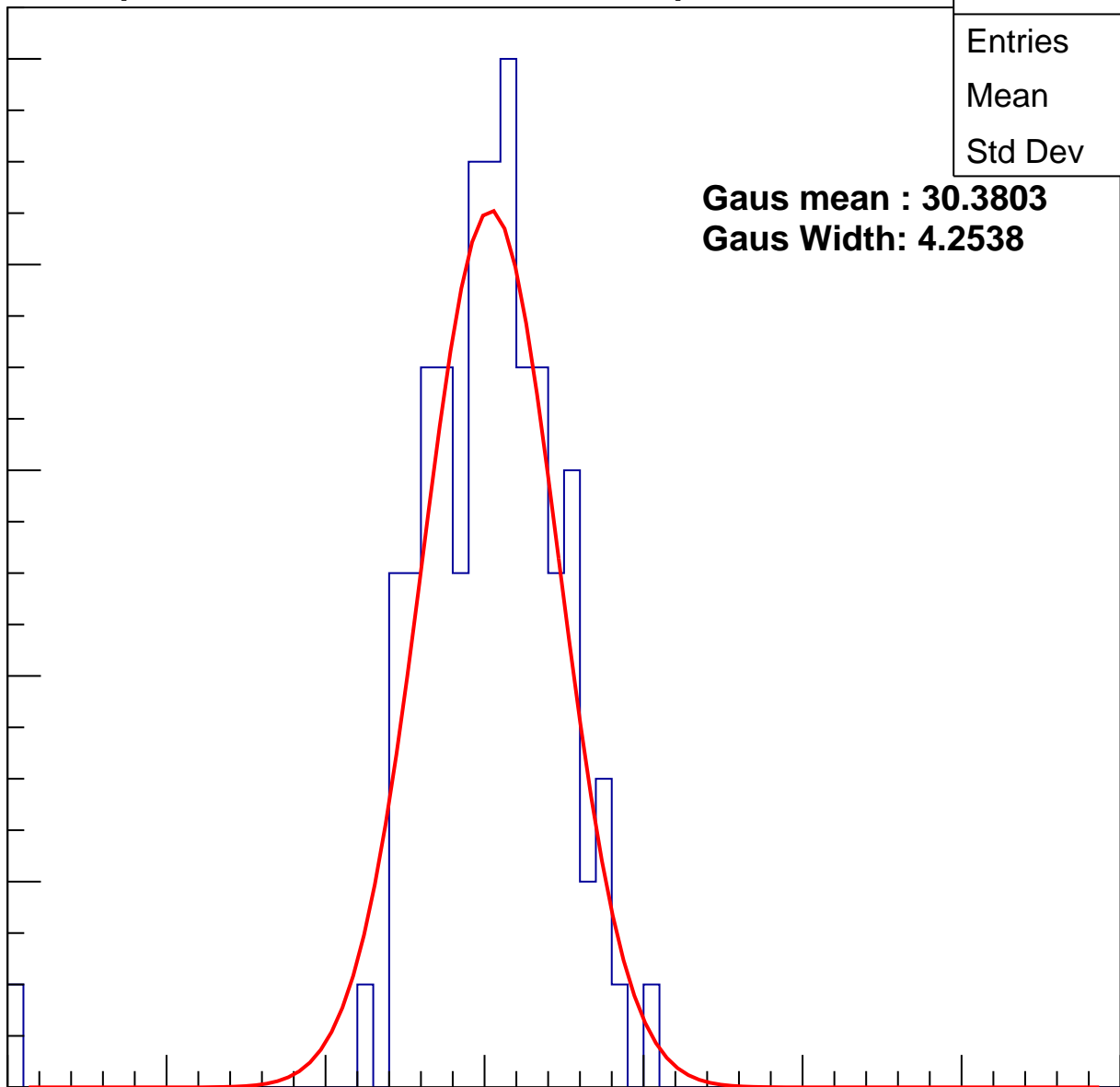
**Gaus Width: 4.2538**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U17-ch105, adc1

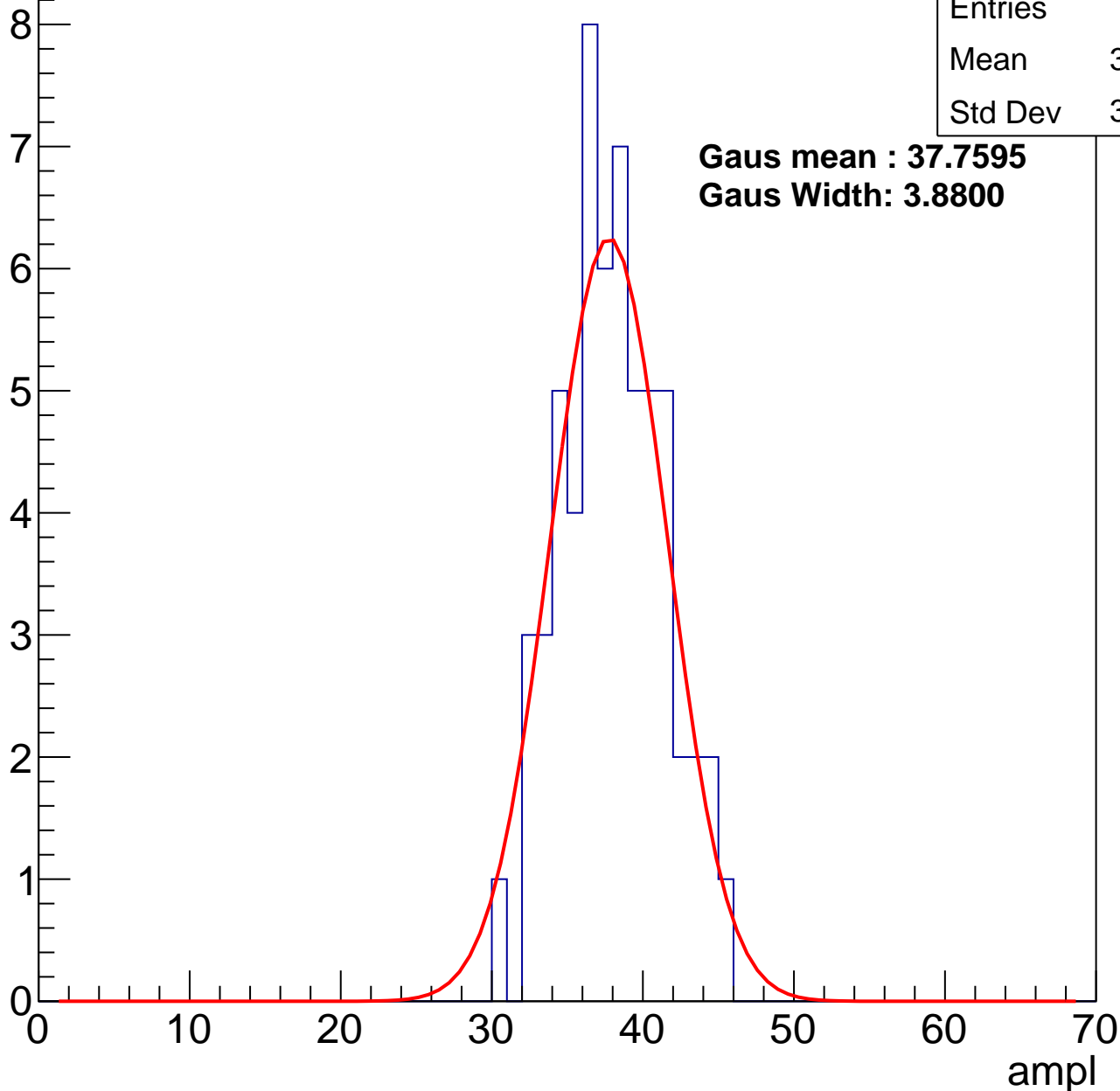
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	37.53
Std Dev	3.346

**Gaus mean : 37.7595**

**Gaus Width: 3.8800**



# B0L001S, U17-ch105, adc2

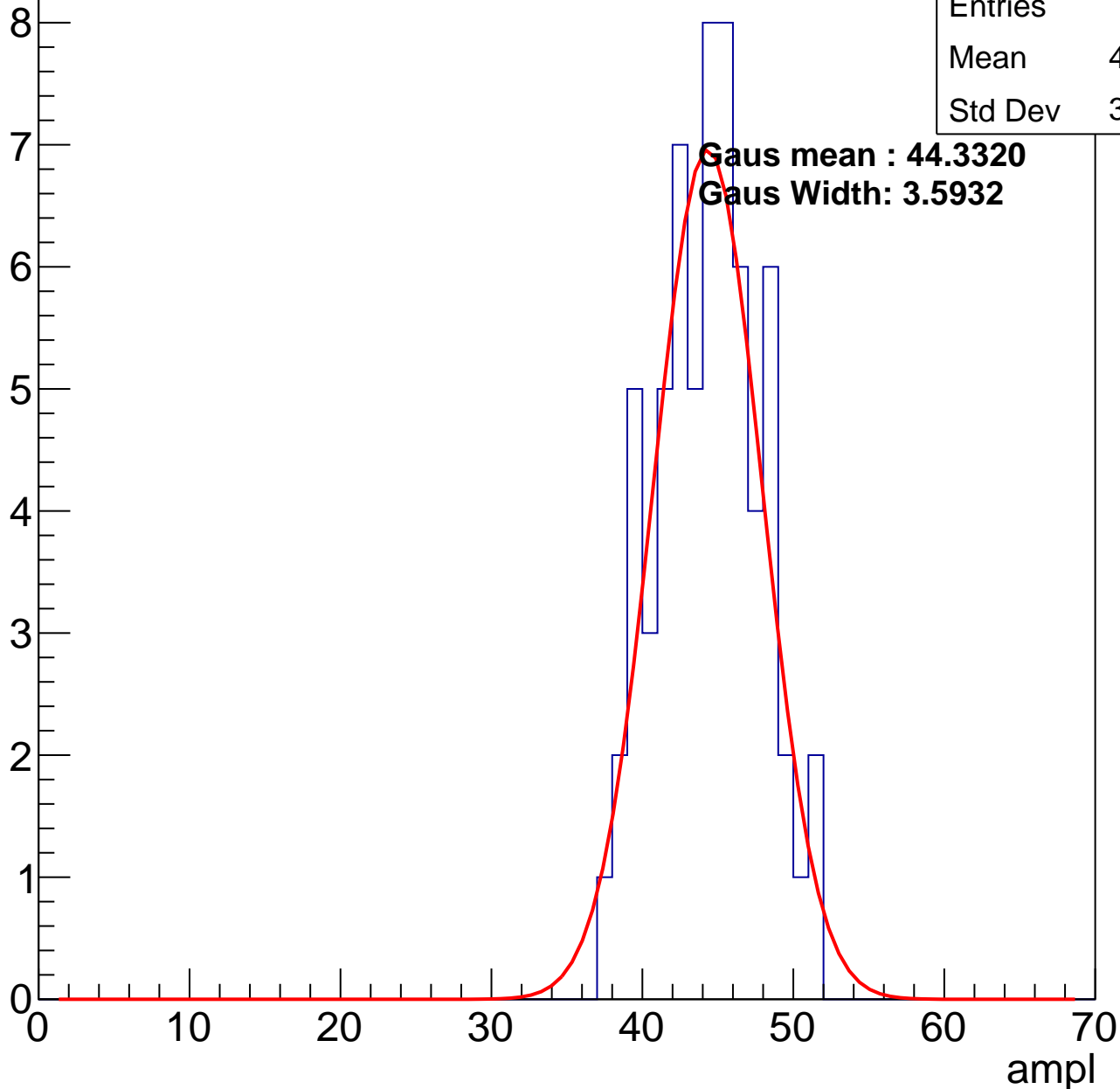
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	43.94
Std Dev	3.328

**Gaus mean : 44.3320**

**Gaus Width: 3.5932**

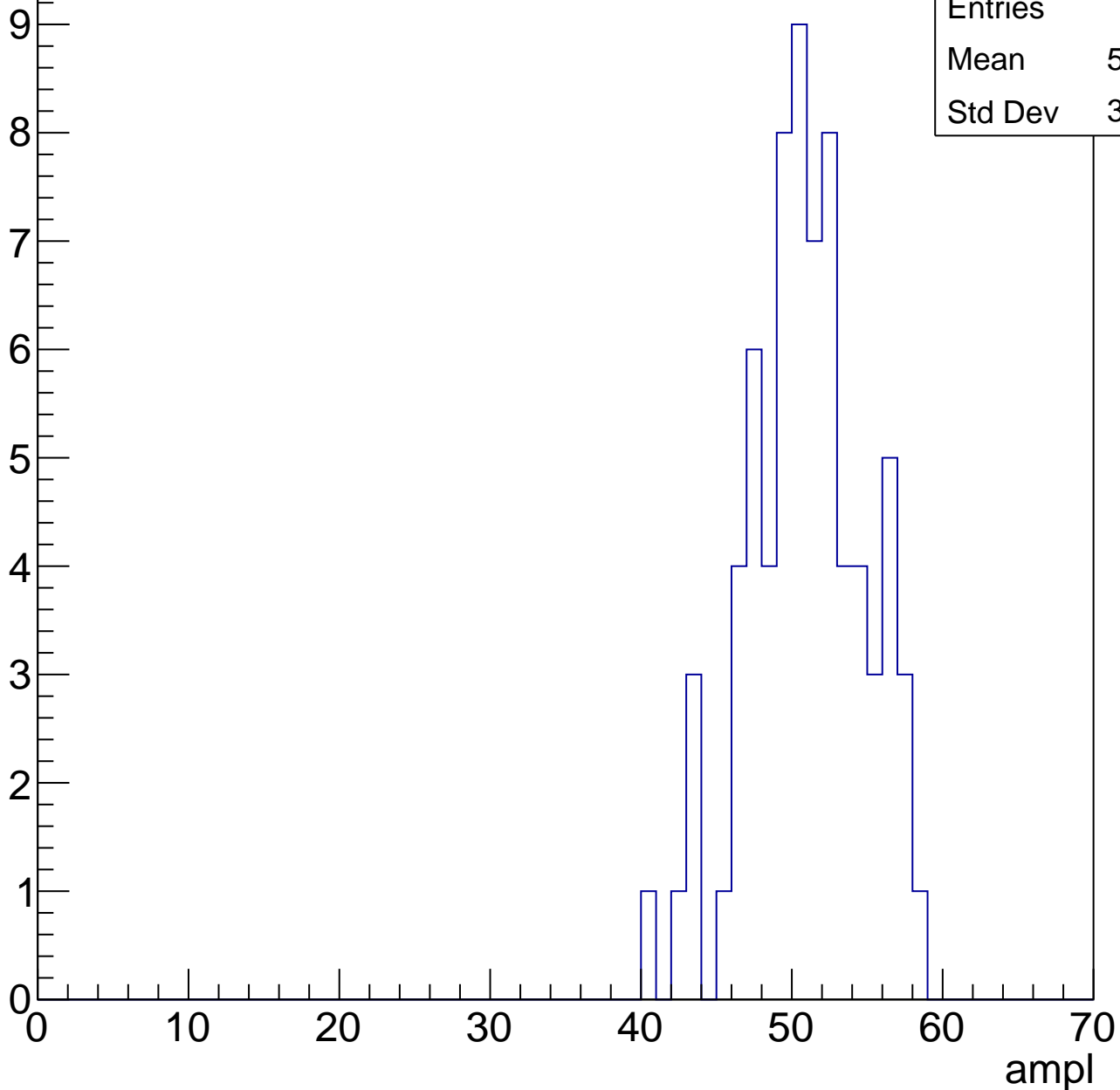


# B0L001S, U17-ch105, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	50.43
Std Dev	3.854

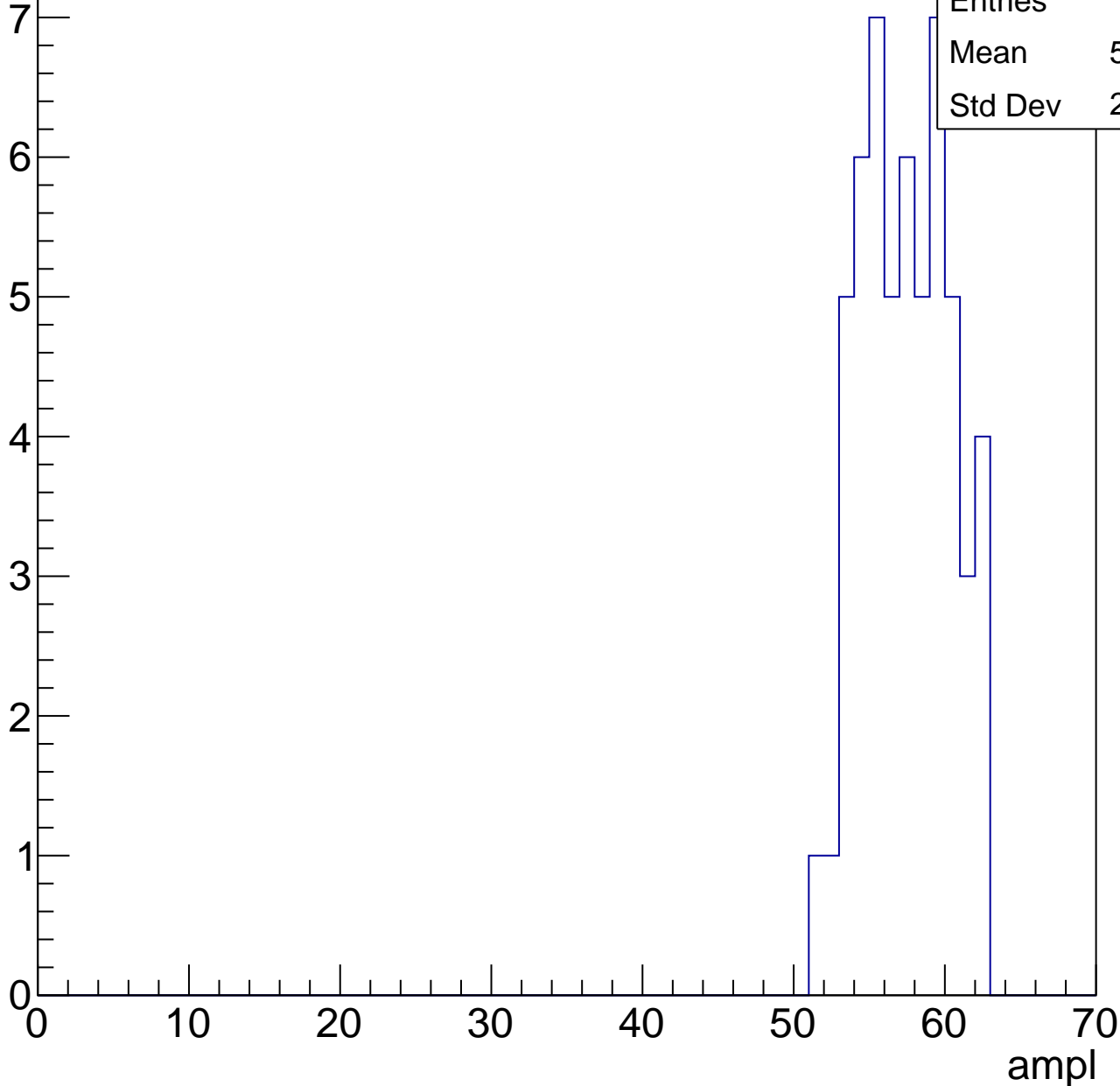


# B0L001S, U17-ch105, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	56.96
Std Dev	2.873

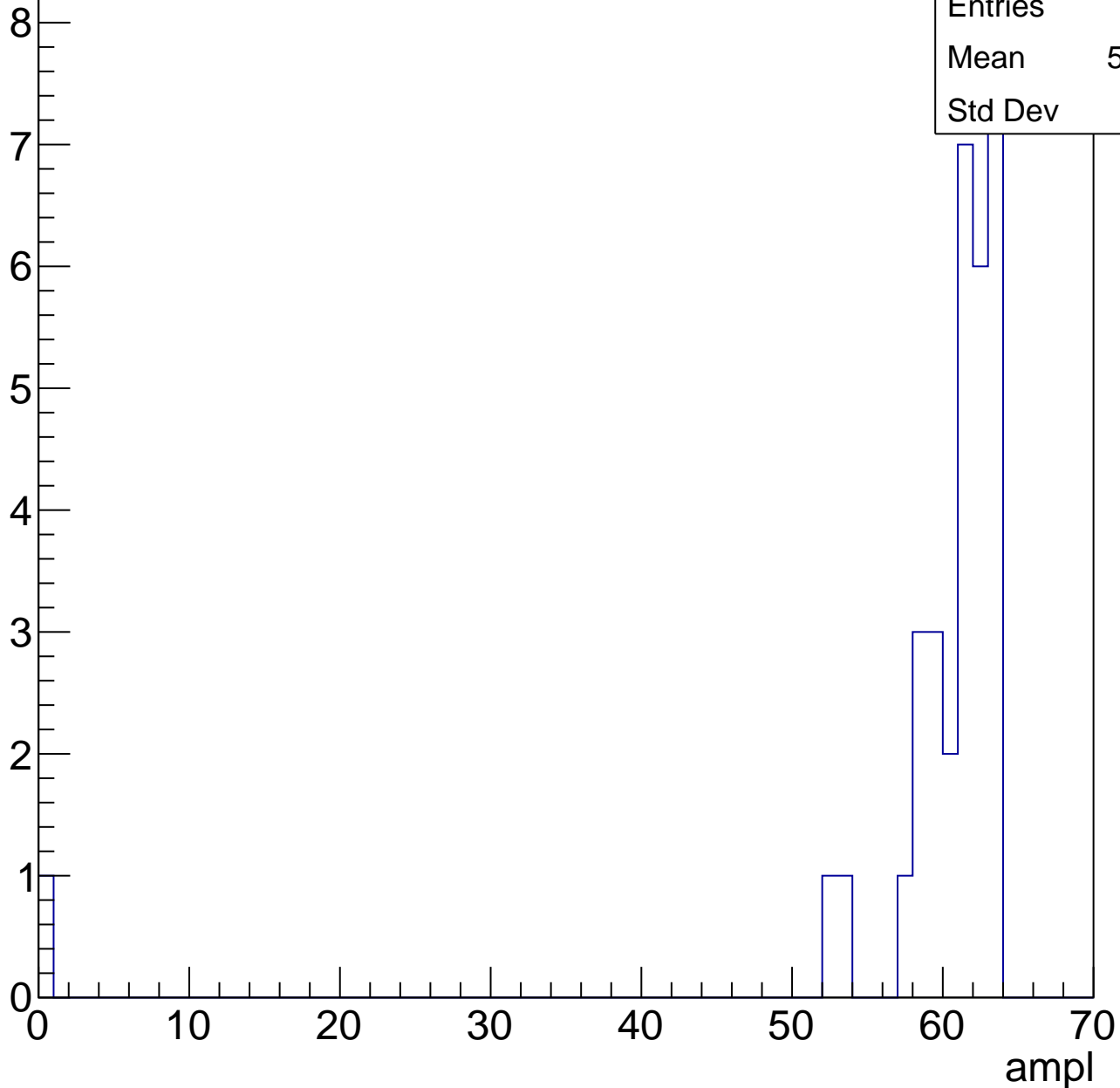


# B0L001S, U17-ch105, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

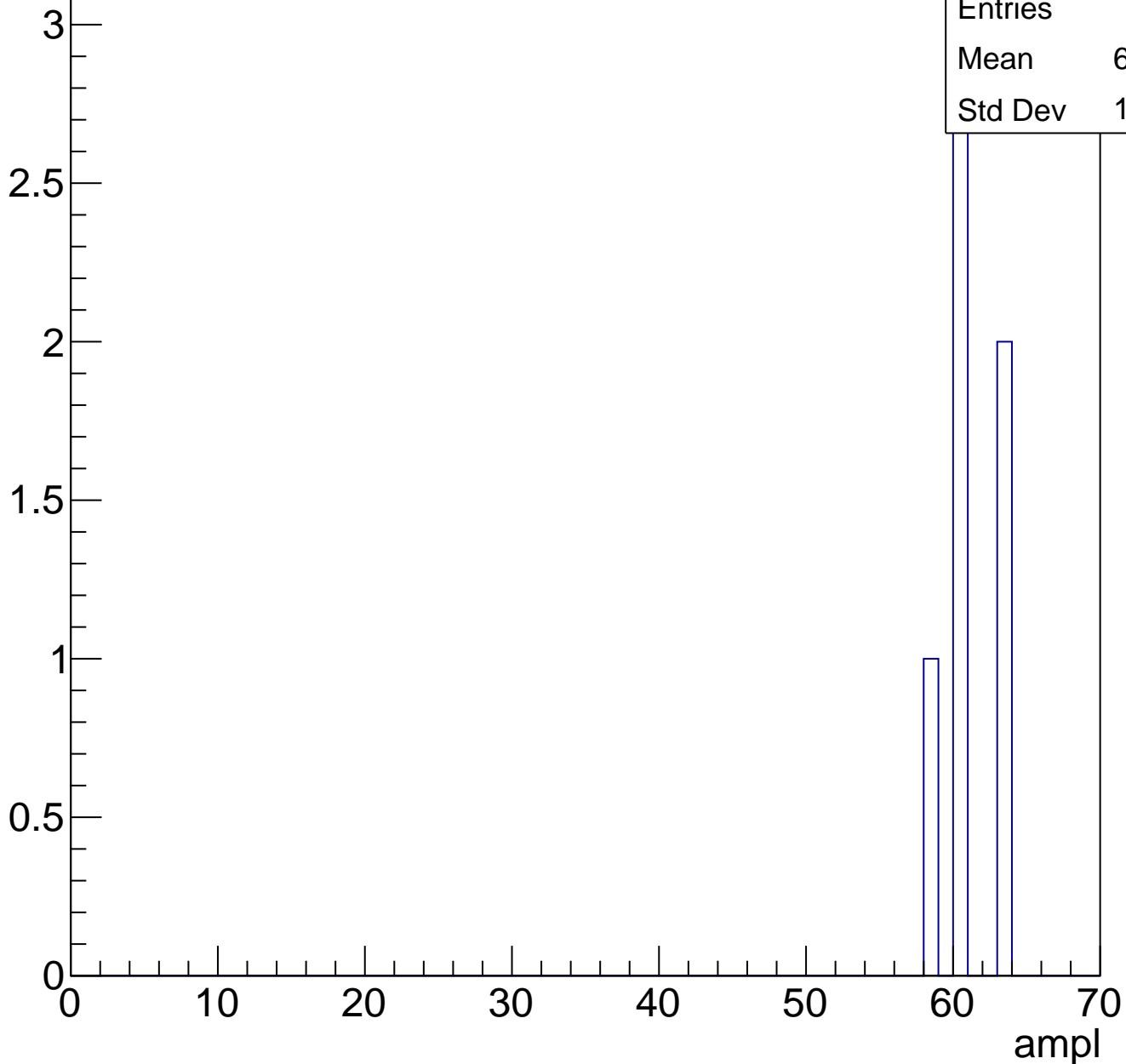
Entries	33
Mean	58.67
Std Dev	10.7



# B0L001S, U17-ch105, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch105, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	10
Std Dev	10

# B0L001S, U17-ch106, adc0

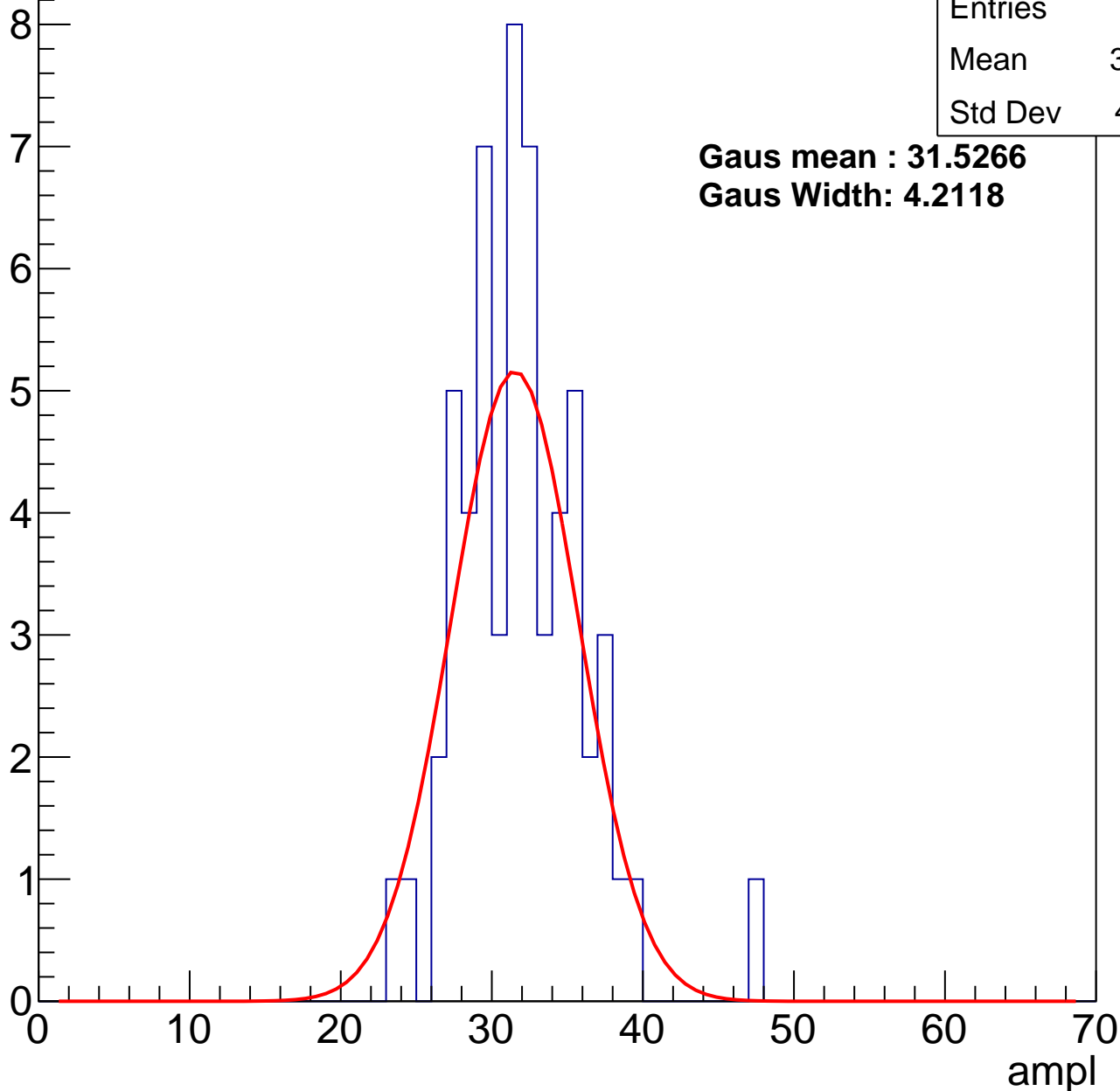
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	31.52
Std Dev	4.061

**Gaus mean : 31.5266**

**Gaus Width: 4.2118**



# B0L001S, U17-ch106, adc1

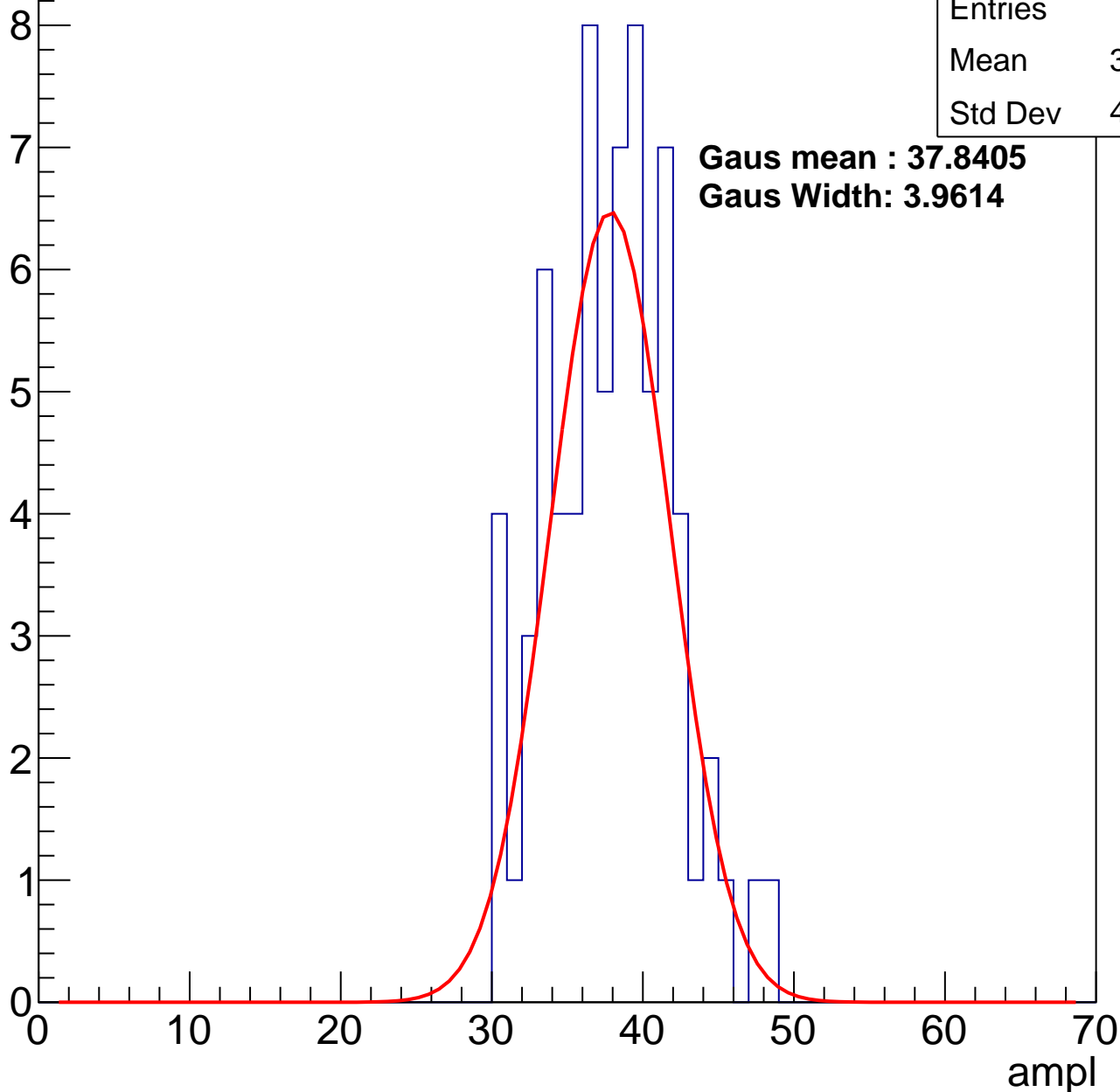
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	37.47
Std Dev	4.017

**Gaus mean : 37.8405**

**Gaus Width: 3.9614**



# B0L001S, U17-ch106, adc2

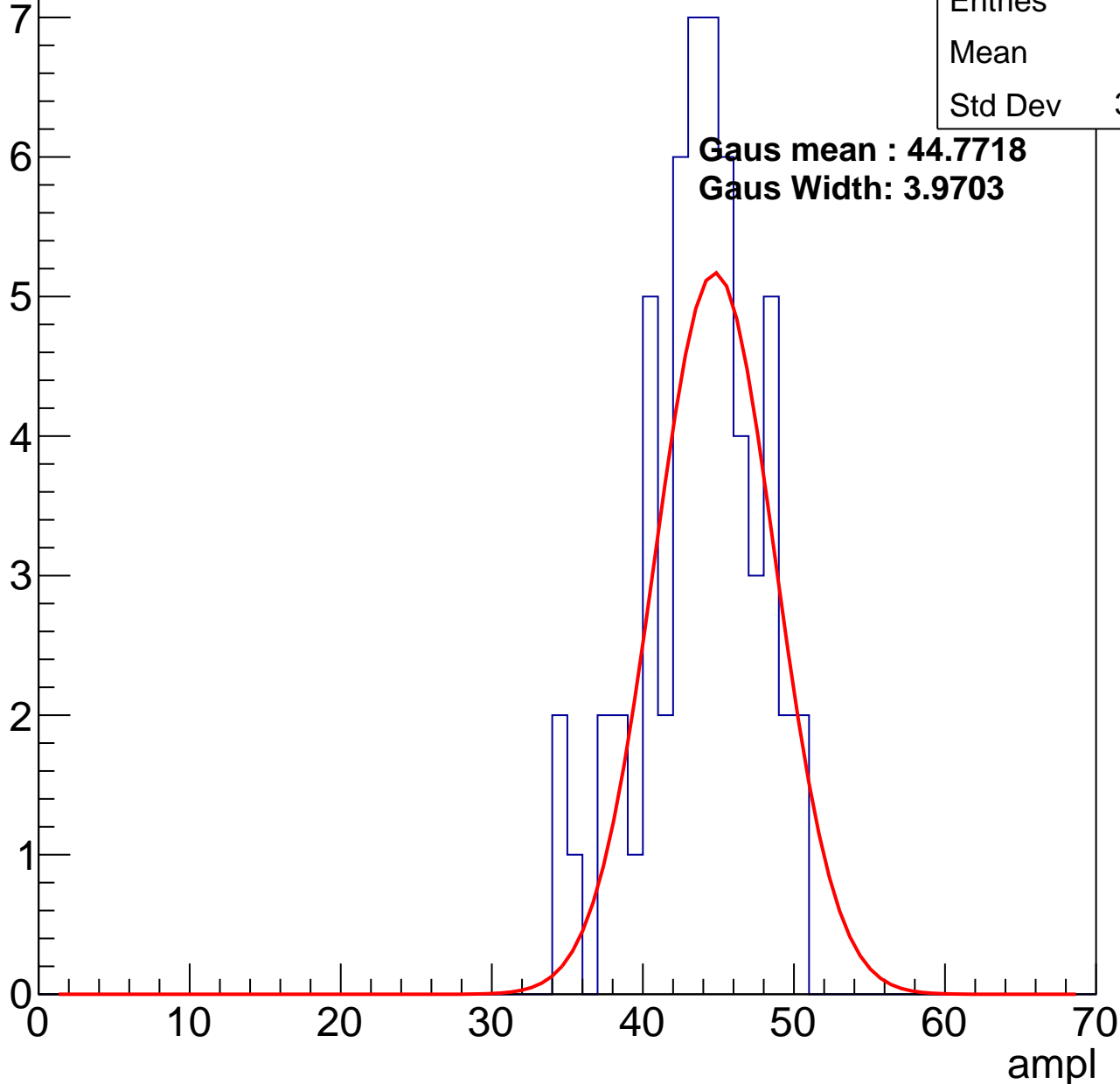
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	43.3
Std Dev	3.811

**Gaus mean : 44.7718**

**Gaus Width: 3.9703**

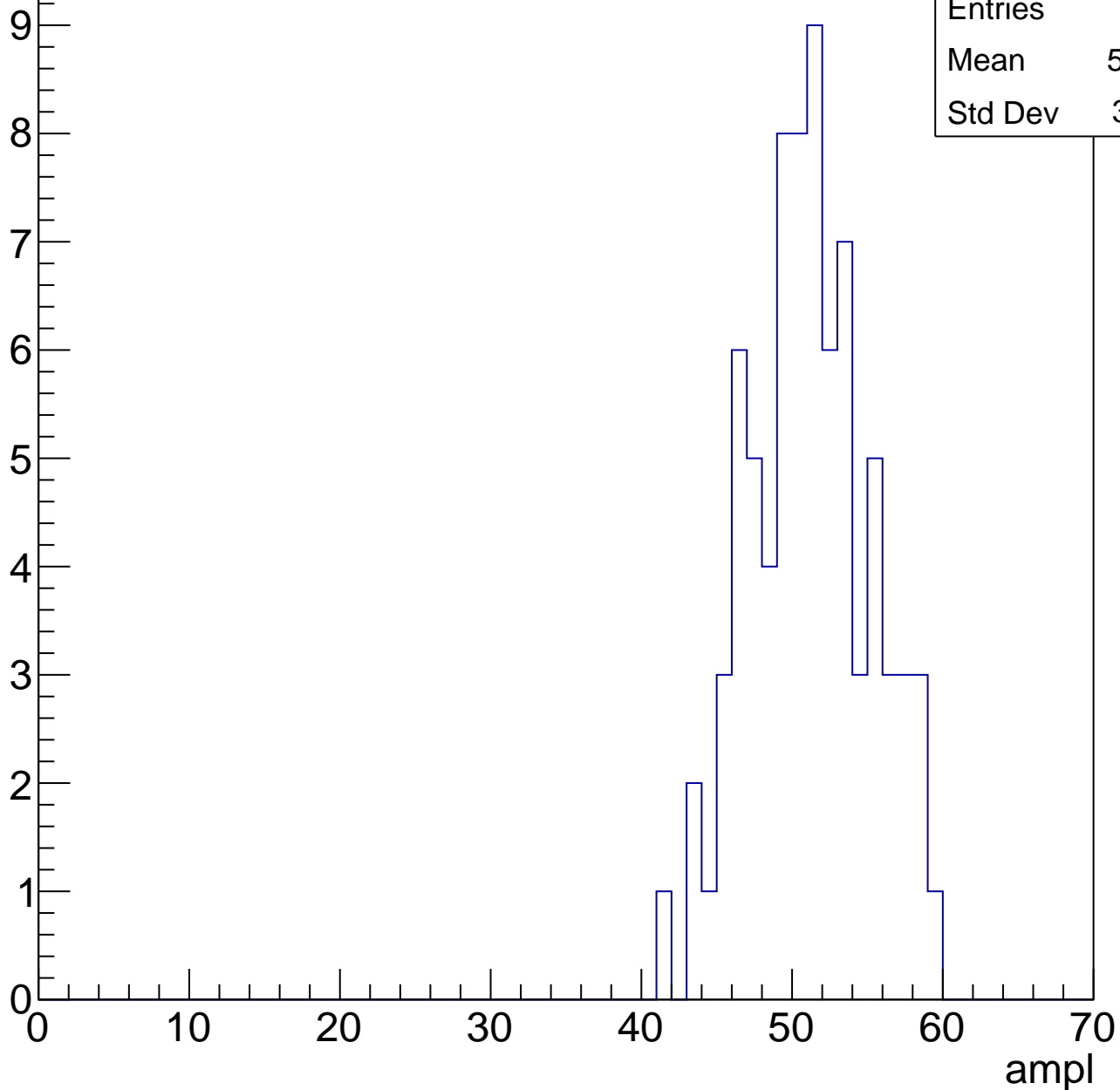


# B0L001S, U17-ch106, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	78
Mean	50.67
Std Dev	3.951

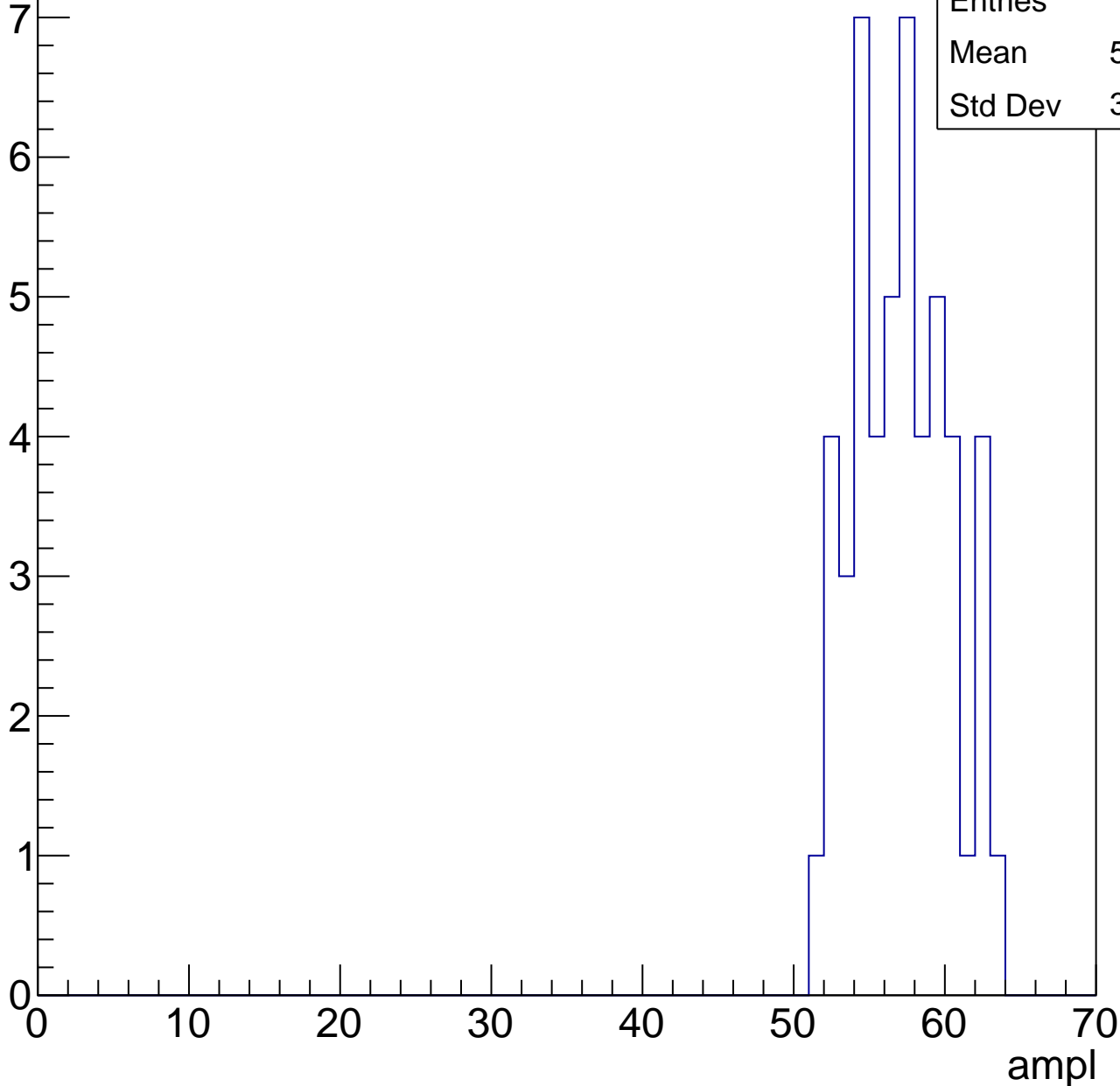


# B0L001S, U17-ch106, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	50
Mean	56.68
Std Dev	3.082

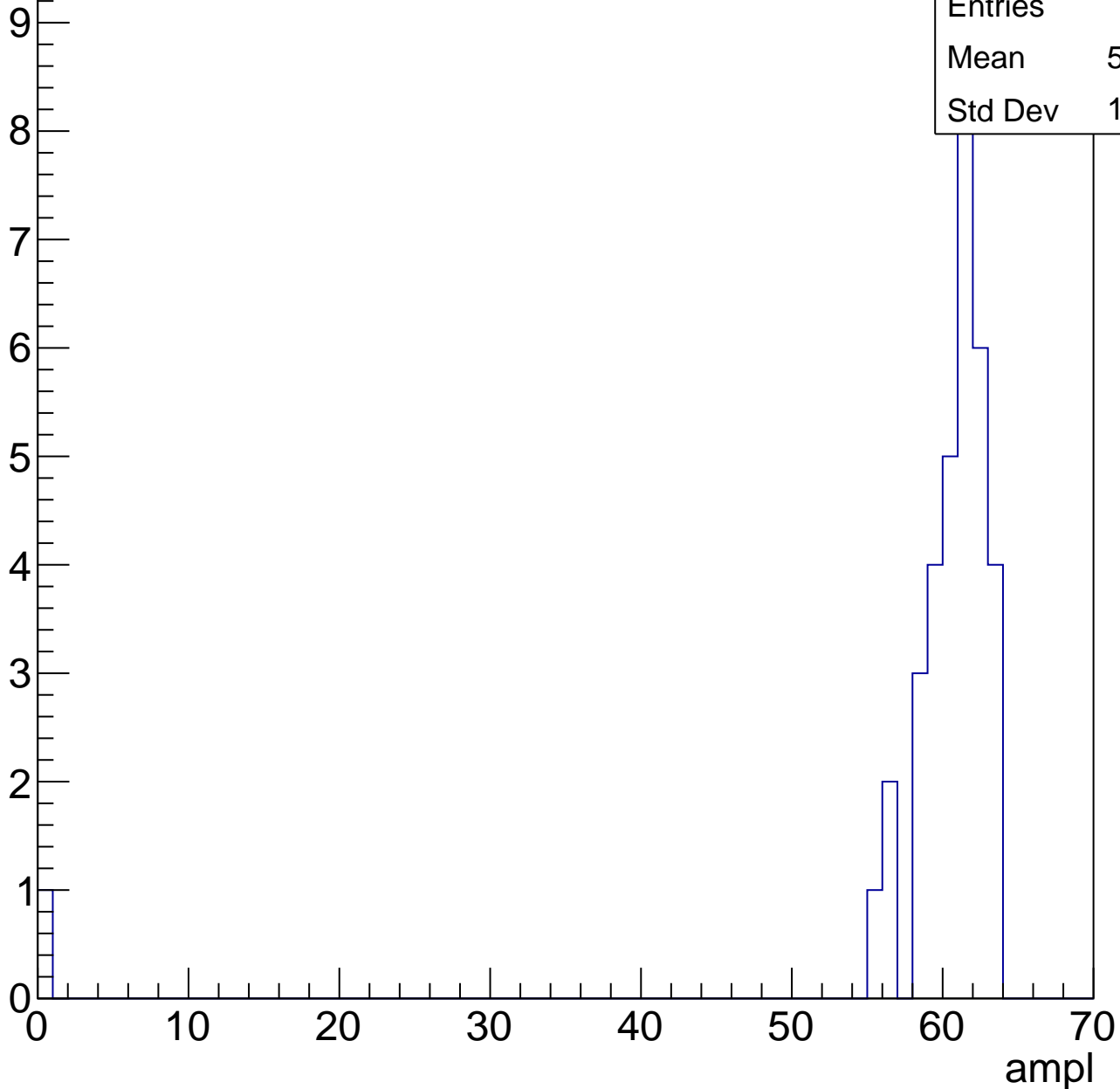


# B0L001S, U17-ch106, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	35
Mean	58.57
Std Dev	10.24

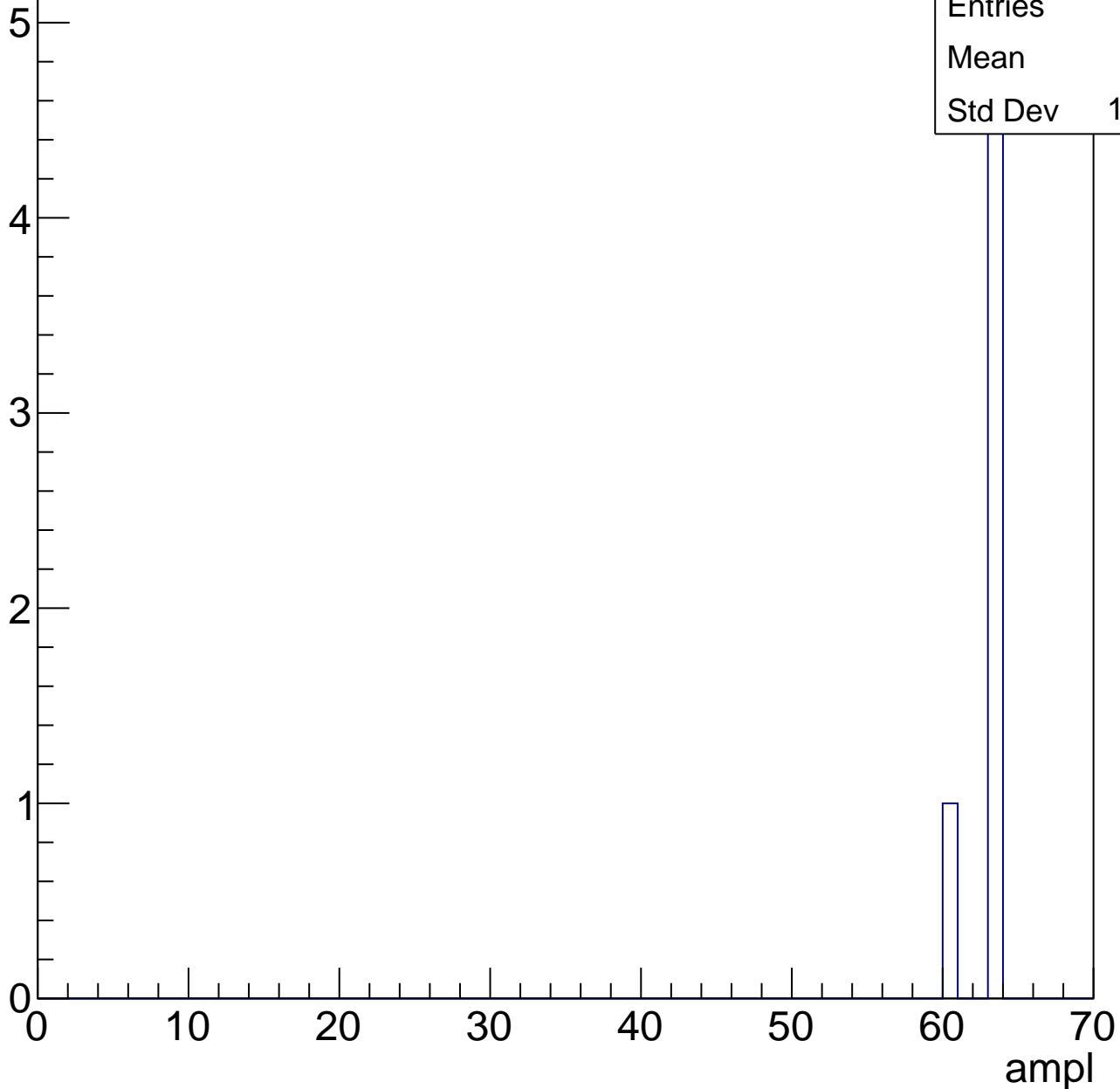


# B0L001S, U17-ch106, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	6
Mean	62.5
Std Dev	1.118





# B0L001S, U17-ch106, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U17-ch107, adc0

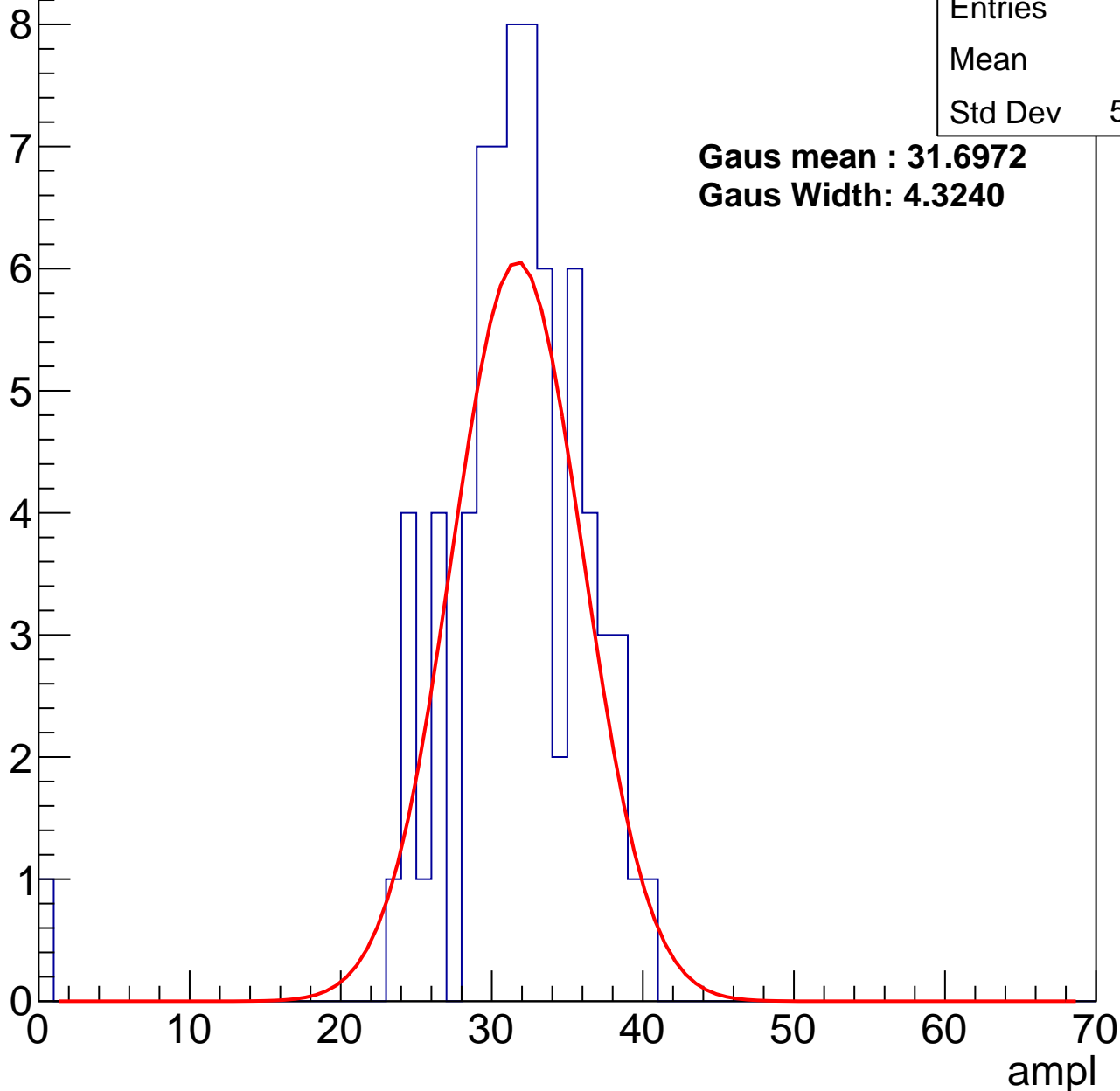
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	31
Std Dev	5.405

**Gaus mean : 31.6972**

**Gaus Width: 4.3240**



# B0L001S, U17-ch107, adc1

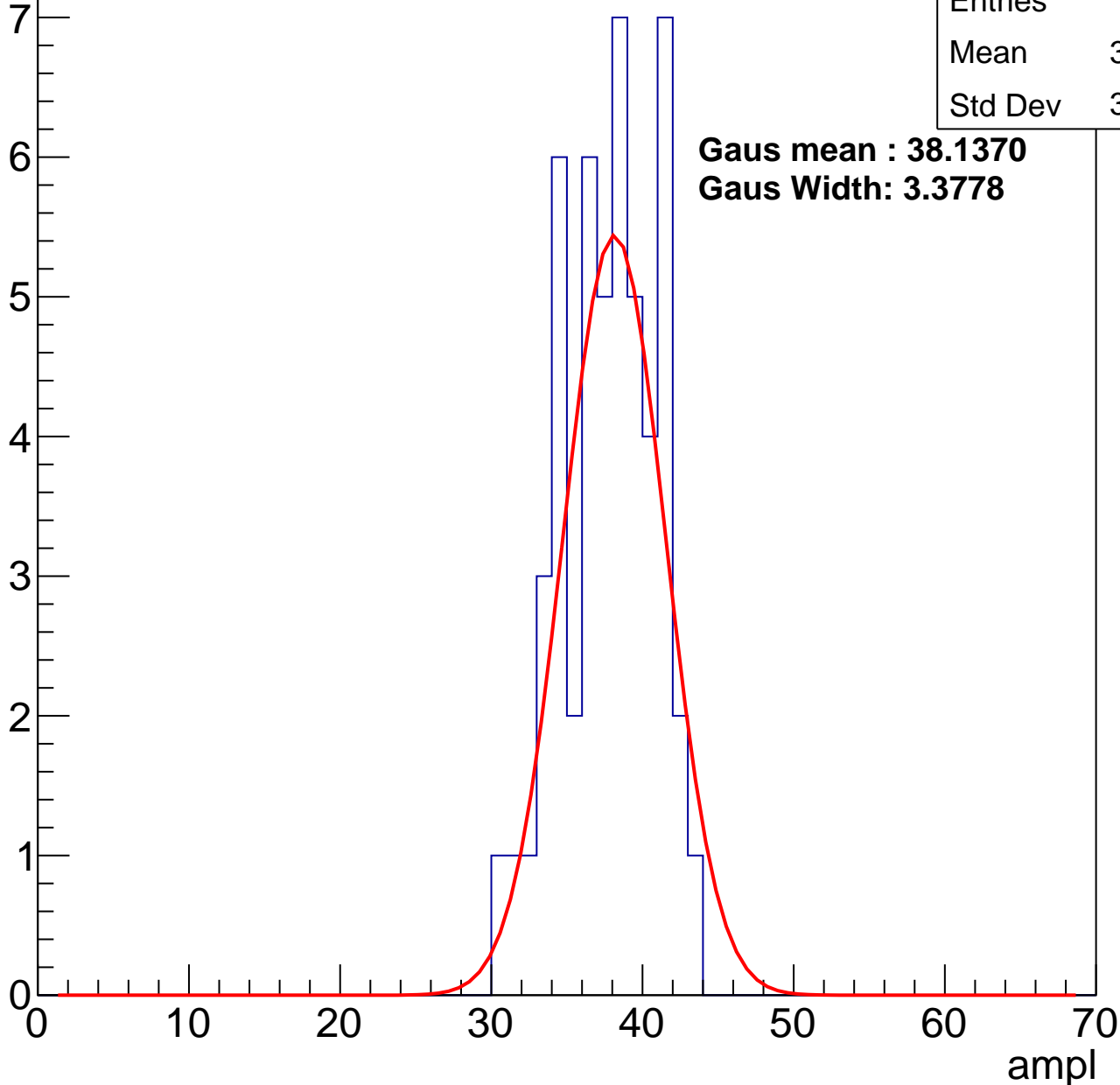
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	51
Mean	37.29
Std Dev	3.076

**Gaus mean : 38.1370**

**Gaus Width: 3.3778**



# B0L001S, U17-ch107, adc2

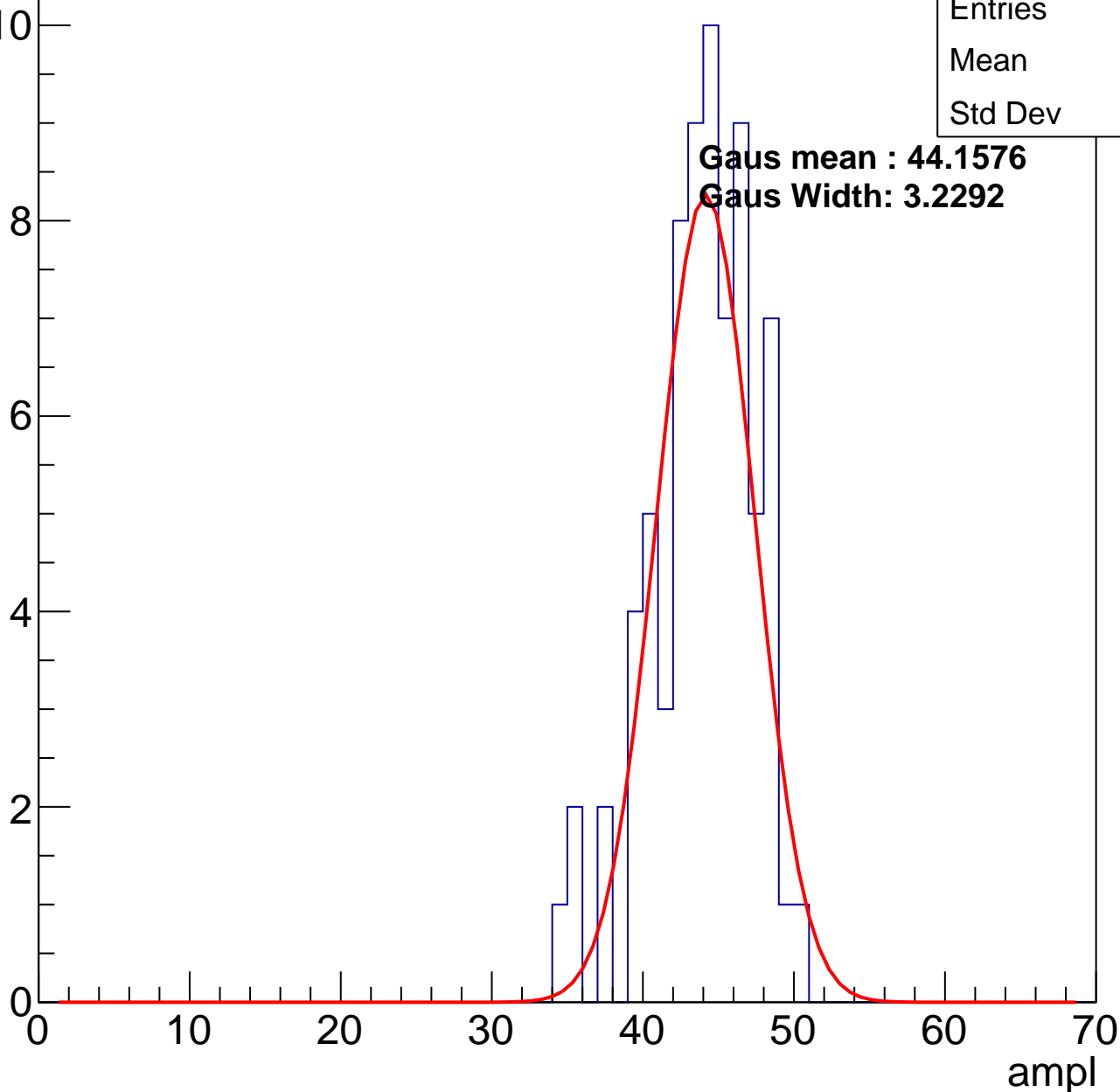
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	43.5
Std Dev	3.39

**Gaus mean : 44.1576**

**Gaus Width: 3.2292**

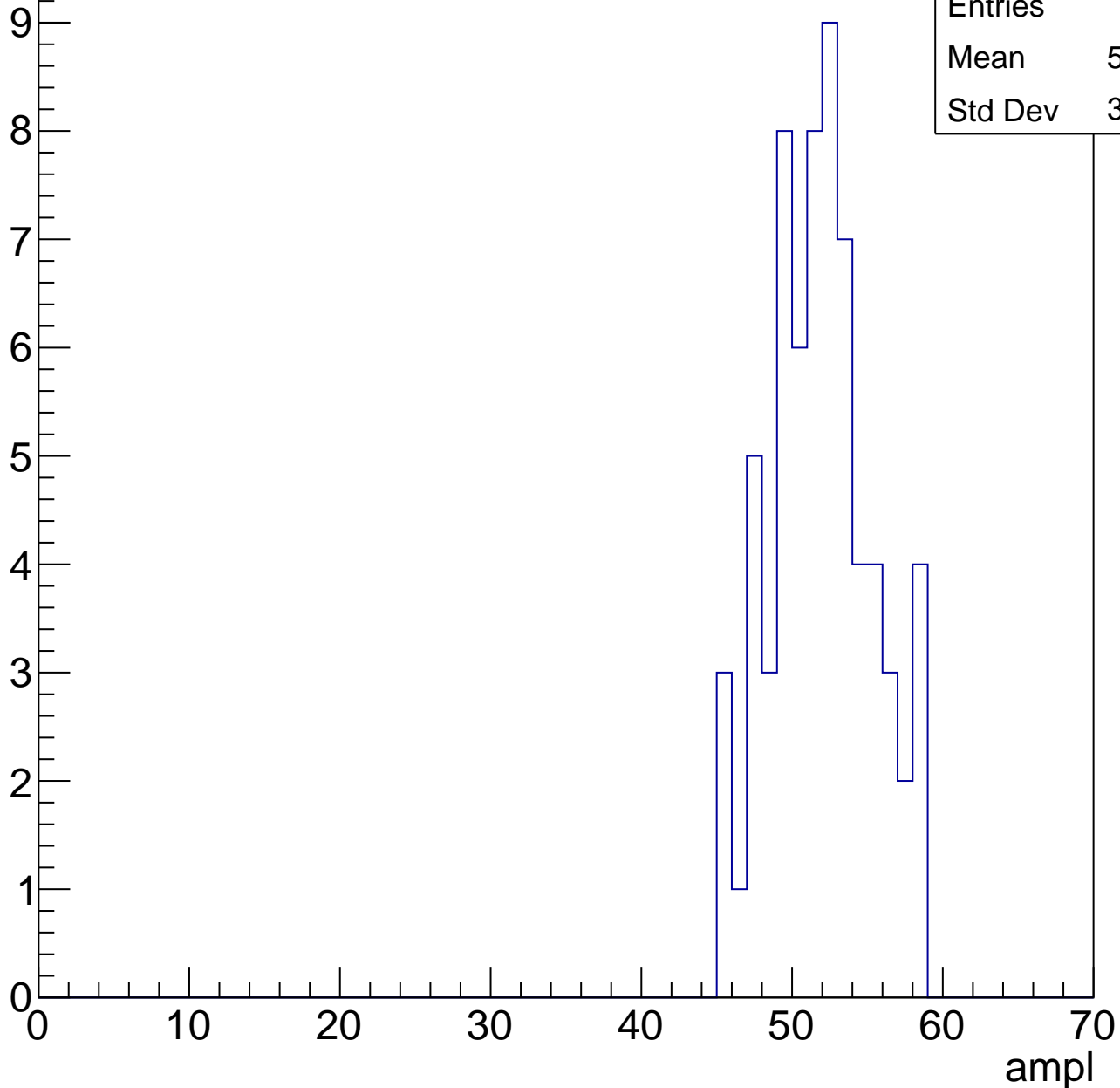


# B0L001S, U17-ch107, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	51.48
Std Dev	3.329

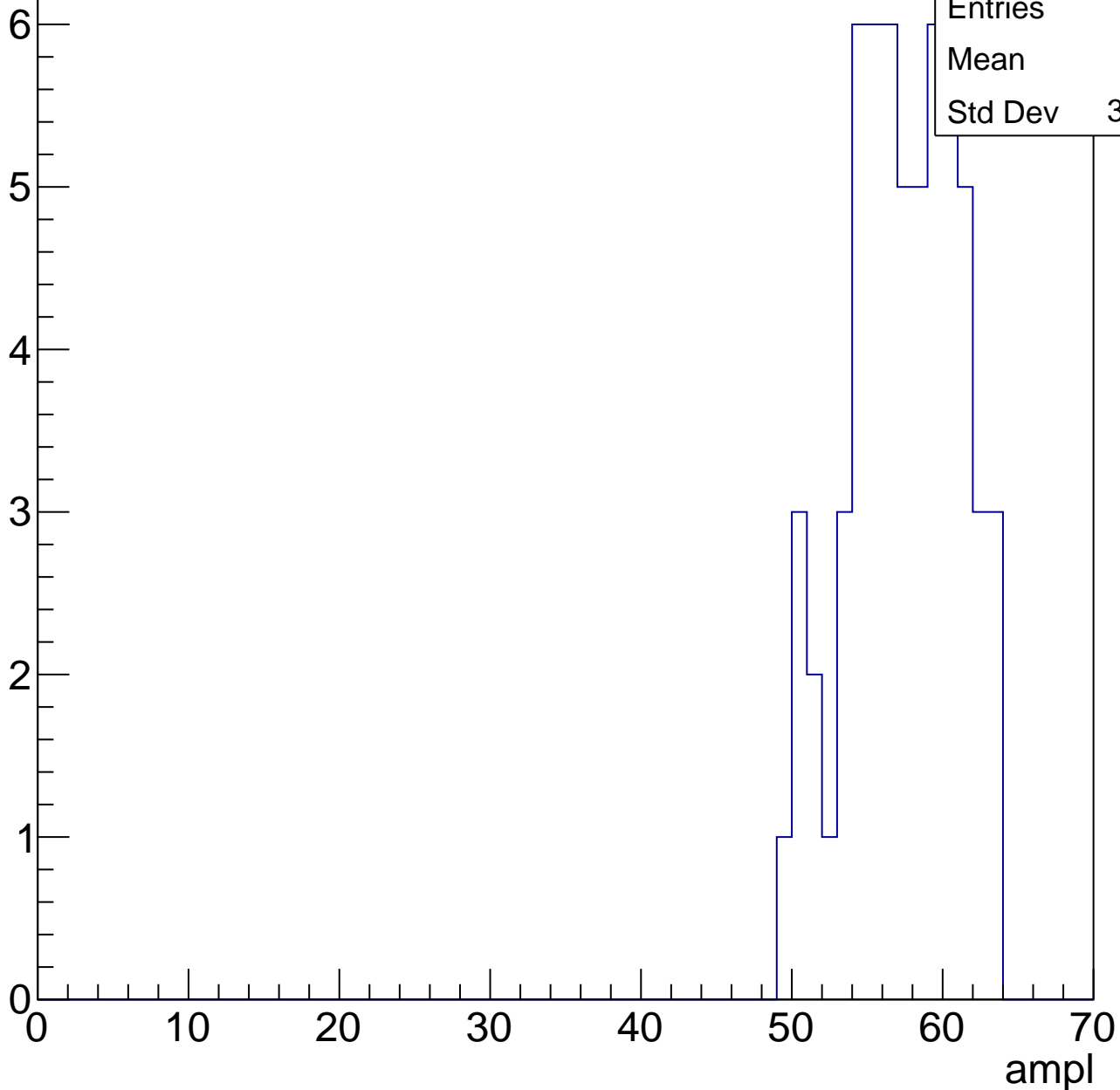


# B0L001S, U17-ch107, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	56.9
Std Dev	3.588

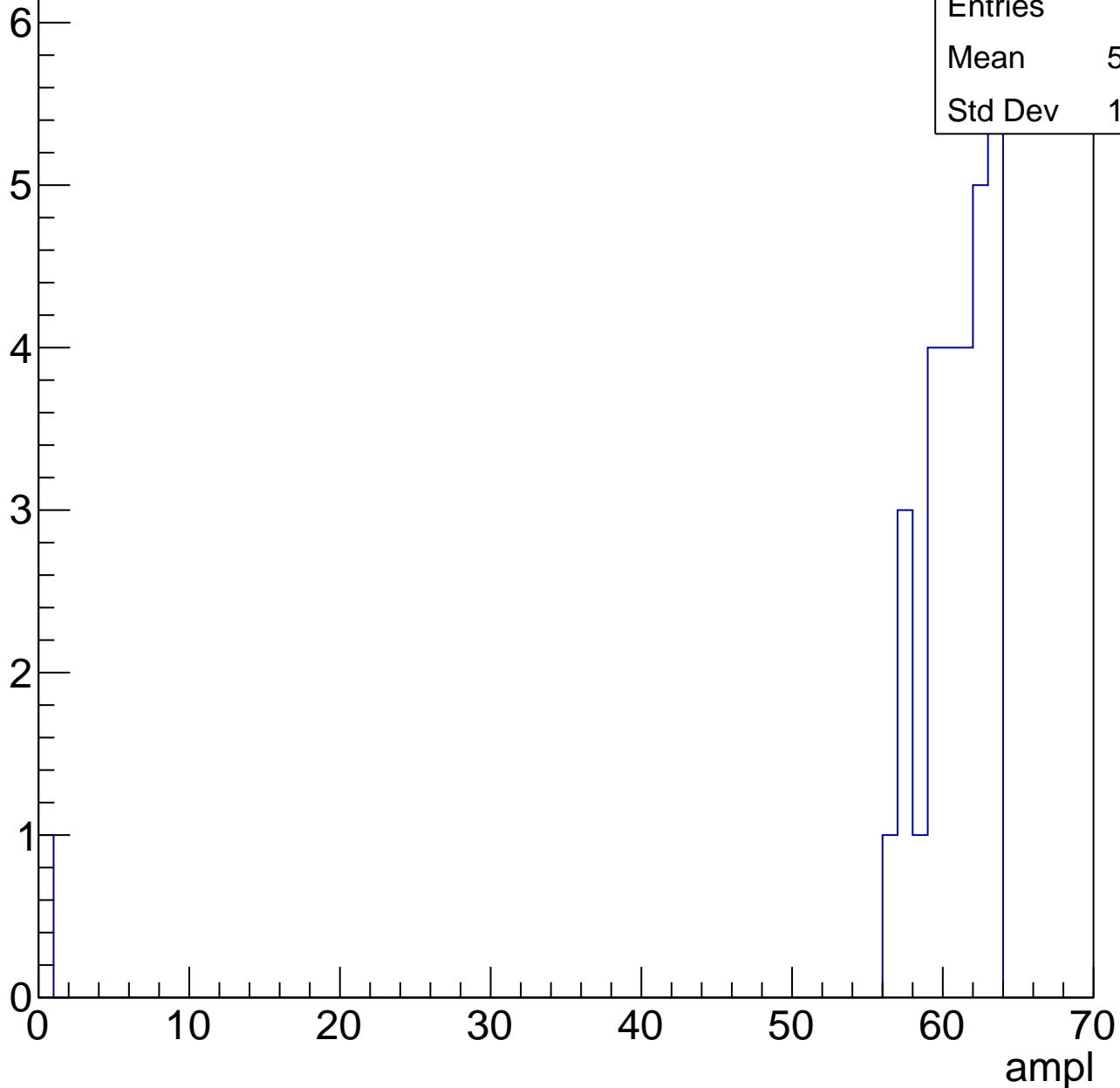


# B0L001S, U17-ch107, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	29
Mean	58.38
Std Dev	11.22



# B0L001S, U17-ch107, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	4
Mean	62
Std Dev	0.7071



# B0L001S, U17-ch107, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U17-ch108, adc0

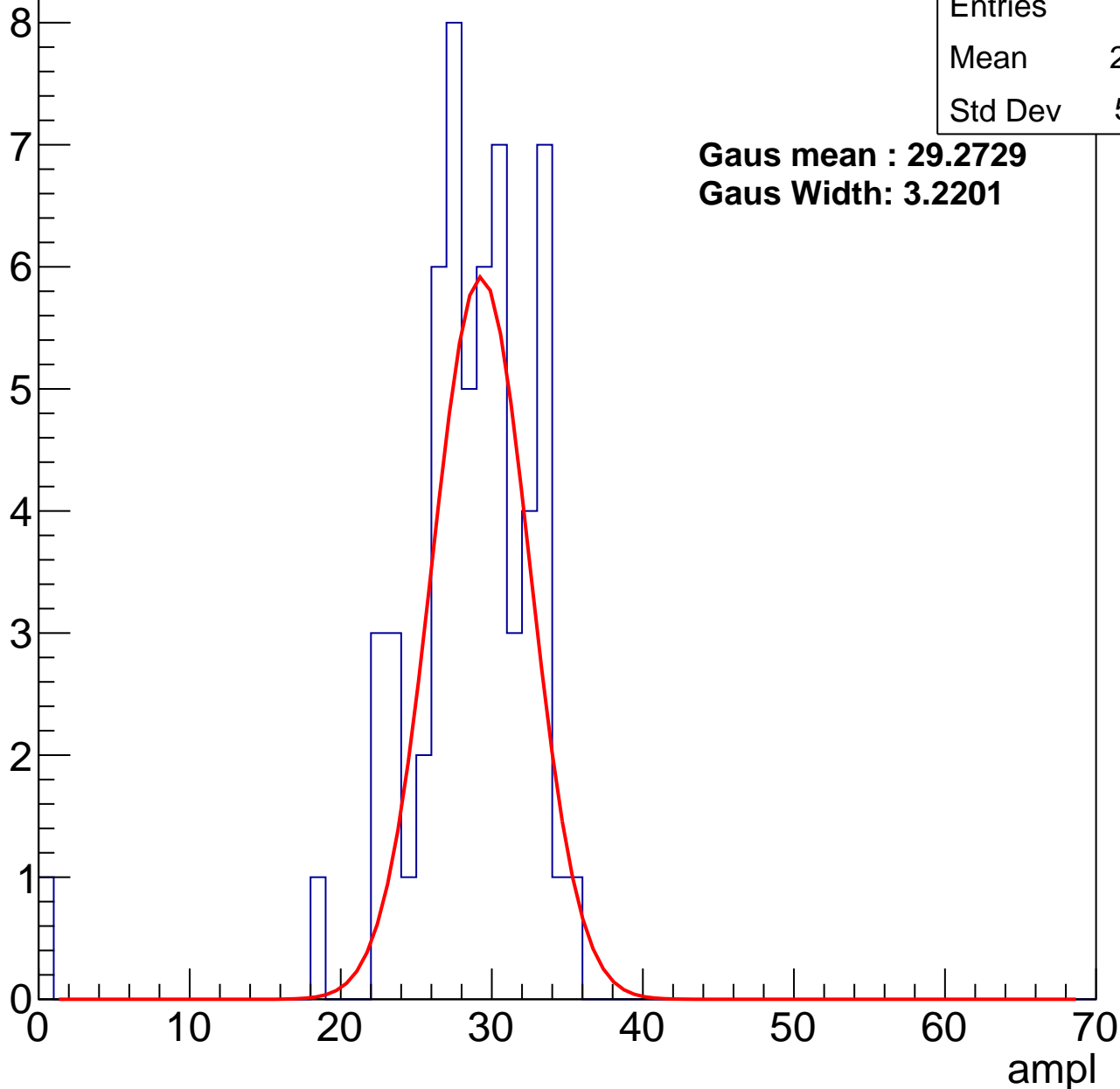
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	27.86
Std Dev	5.071

**Gaus mean : 29.2729**

**Gaus Width: 3.2201**



# B0L001S, U17-ch108, adc1

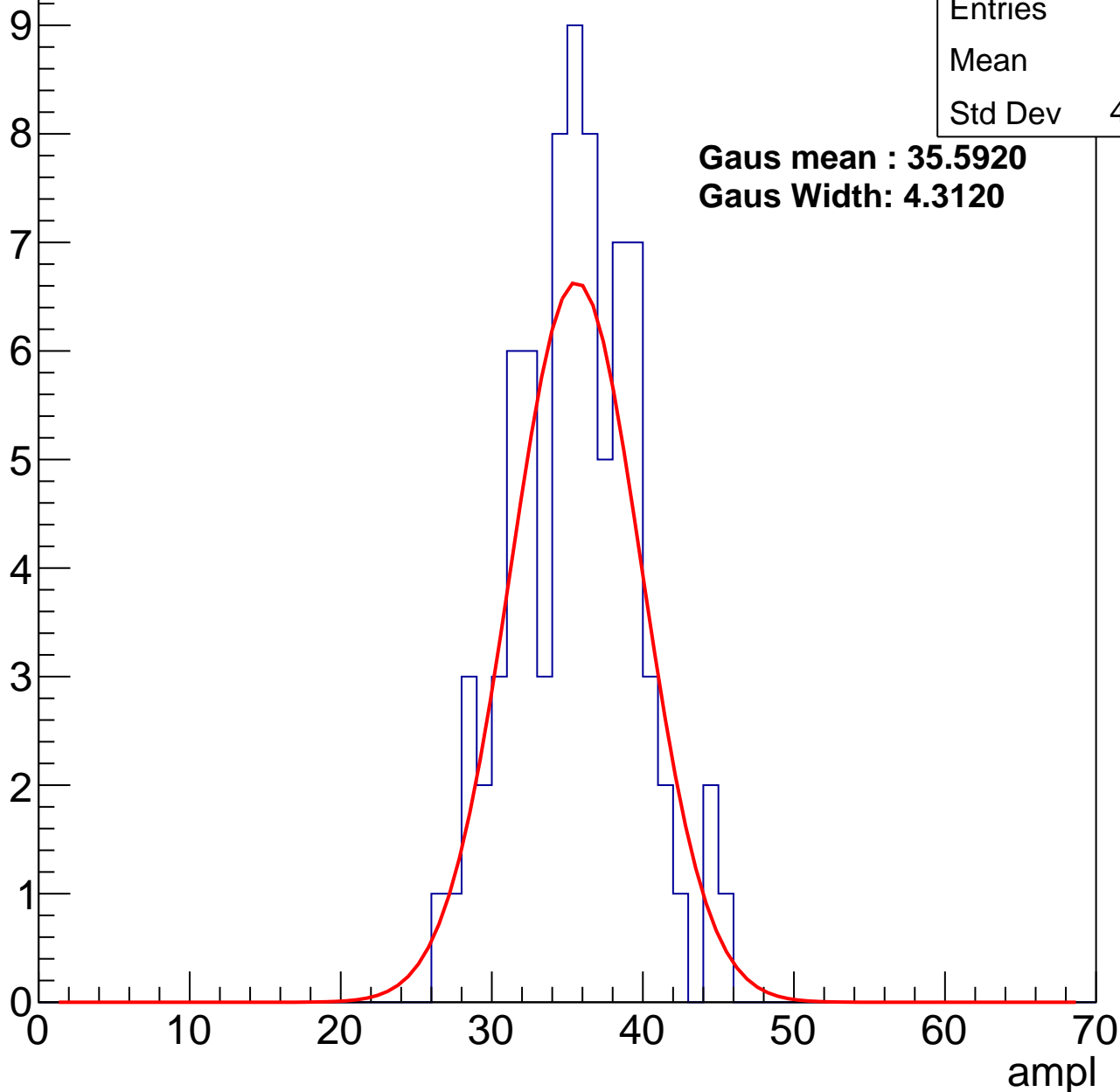
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	78
Mean	35.1
Std Dev	4.034

**Gaus mean : 35.5920**

**Gaus Width: 4.3120**



# B0L001S, U17-ch108, adc2

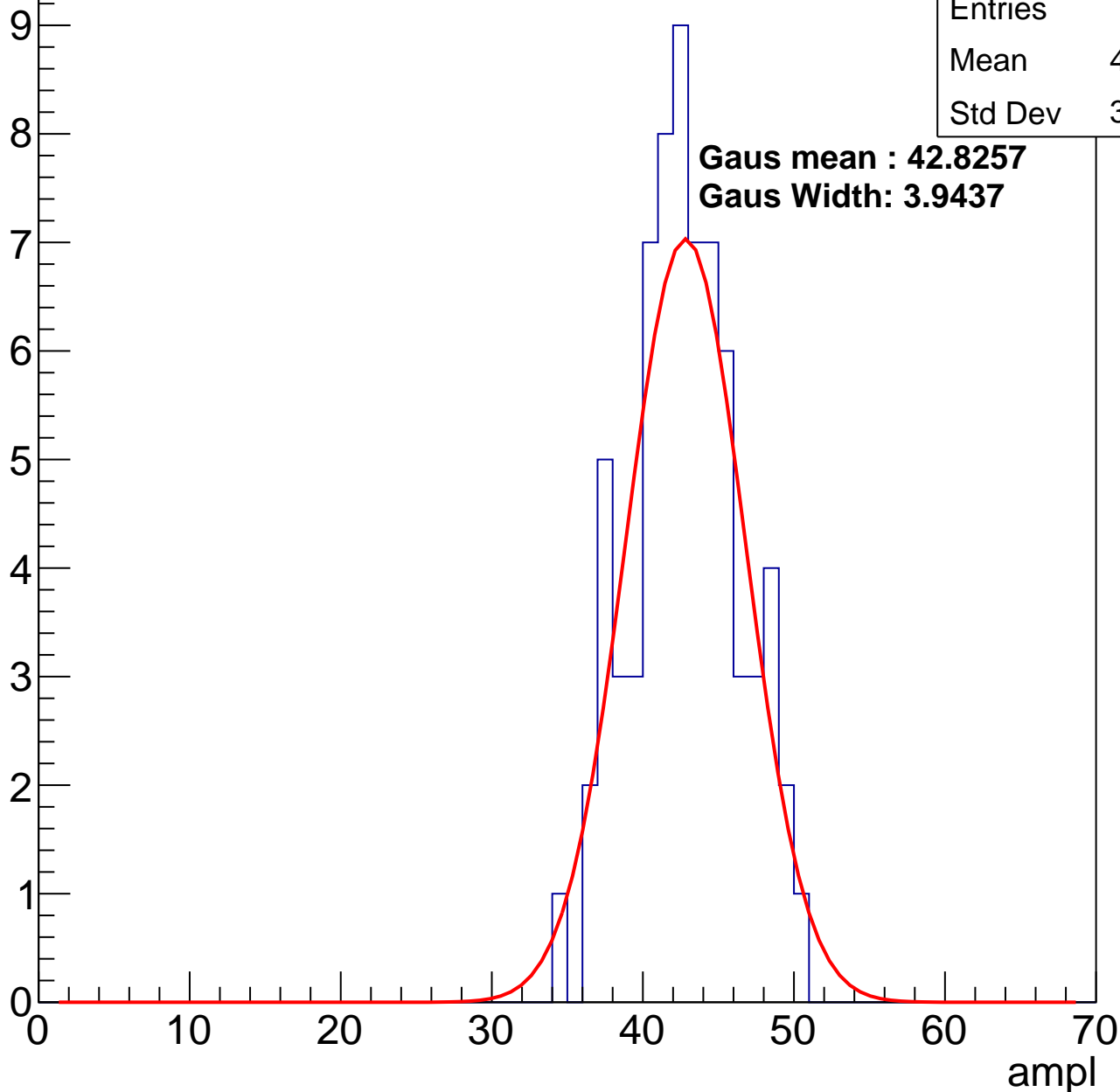
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	42.34
Std Dev	3.524

**Gaus mean : 42.8257**

**Gaus Width: 3.9437**

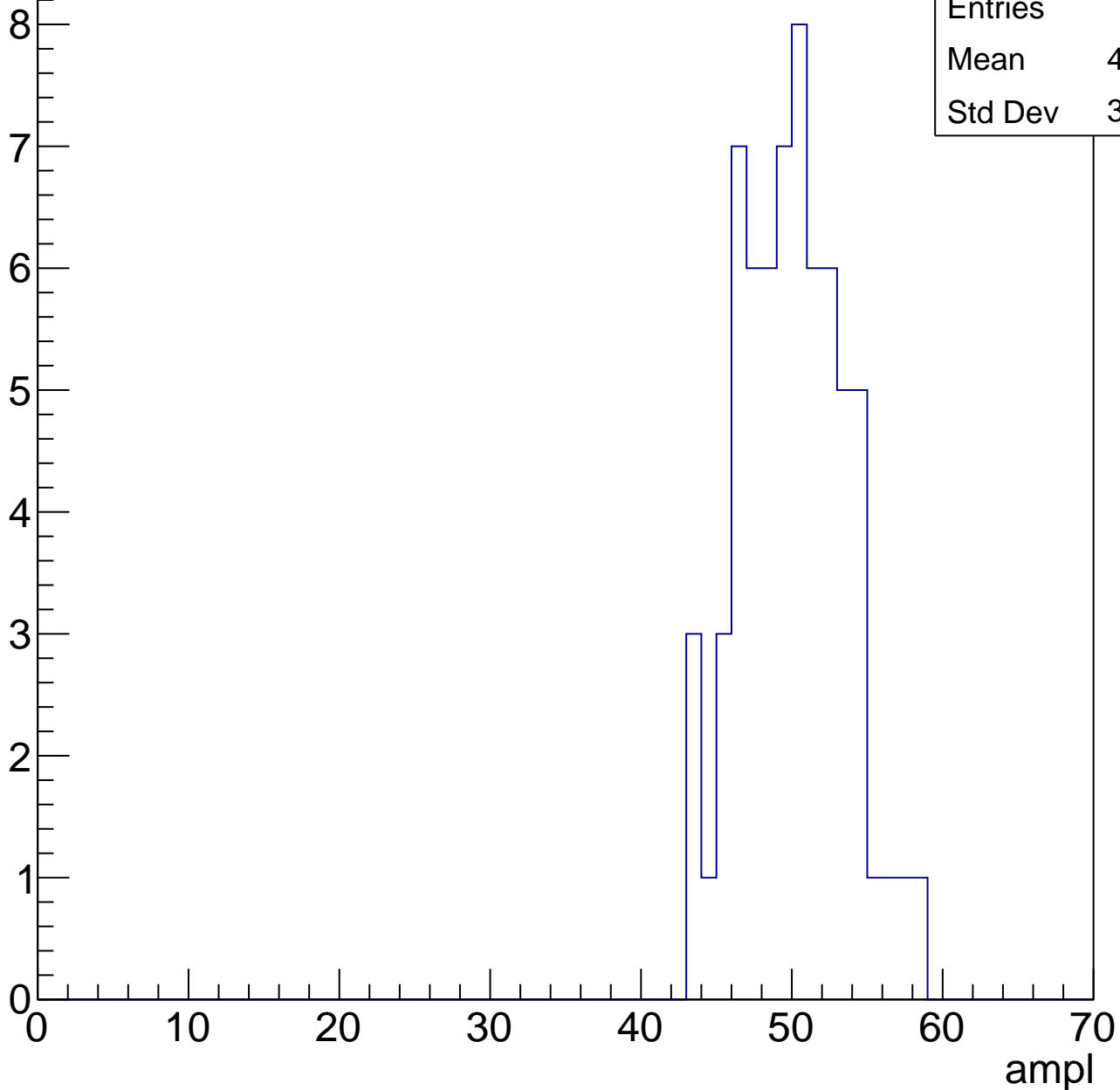


# B0L001S, U17-ch108, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	49.58
Std Dev	3.395

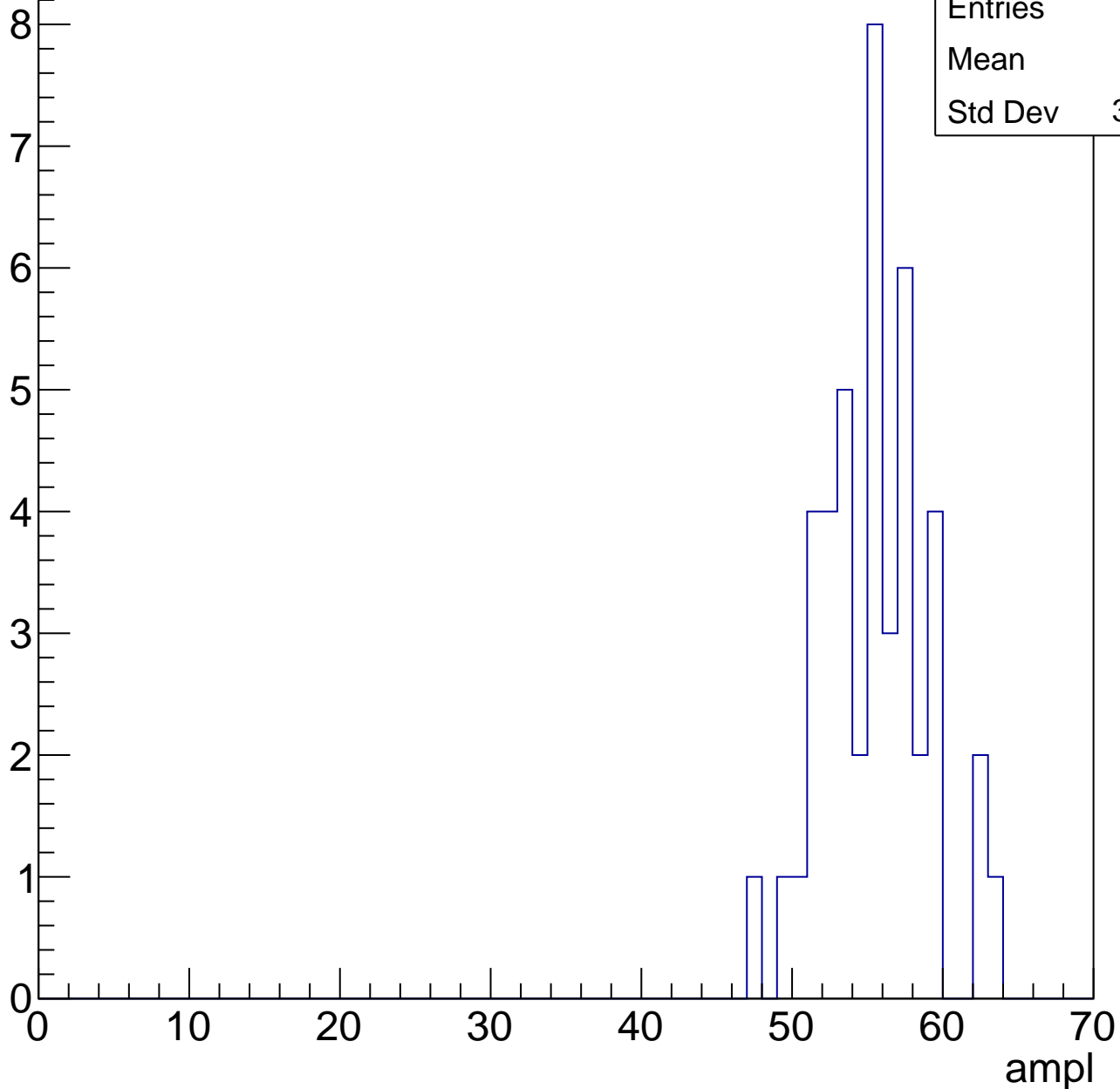


# B0L001S, U17-ch108, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	44
Mean	55
Std Dev	3.431

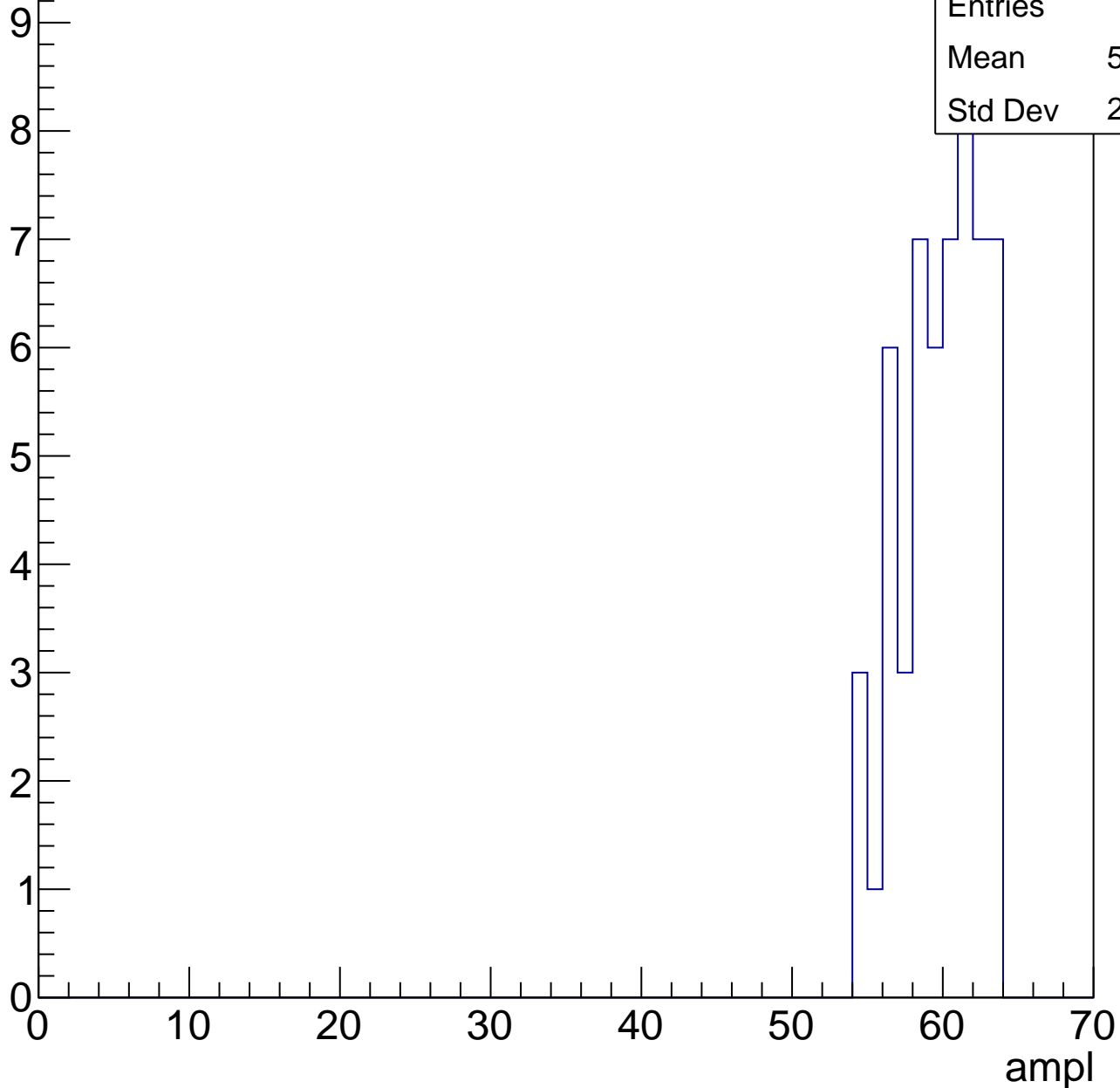


# B0L001S, U17-ch108, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	59.43
Std Dev	2.576



# B0L001S, U17-ch108, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries

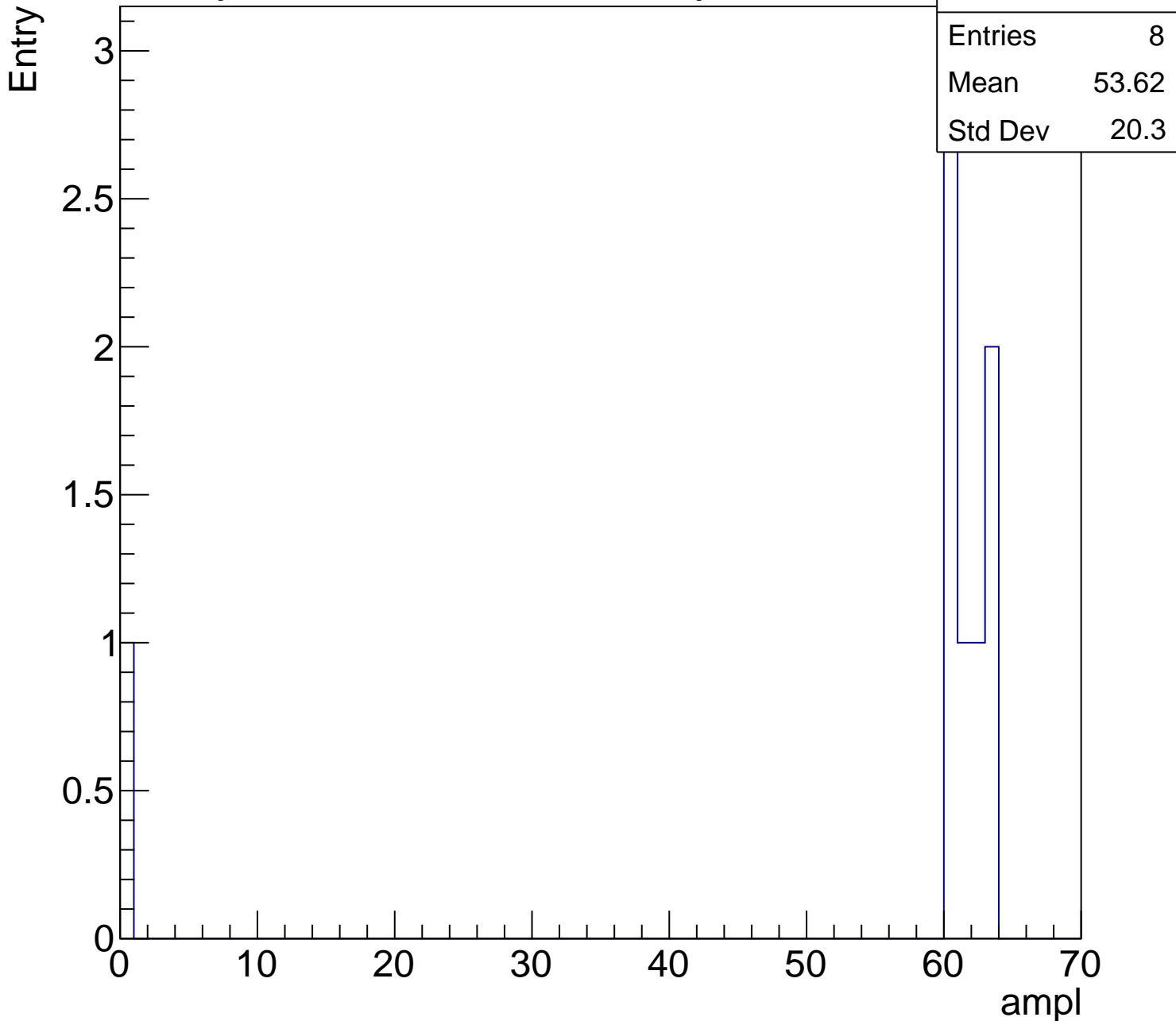
8

Mean

53.62

Std Dev

20.3





# B0L001S, U17-ch108, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U17-ch109, adc0

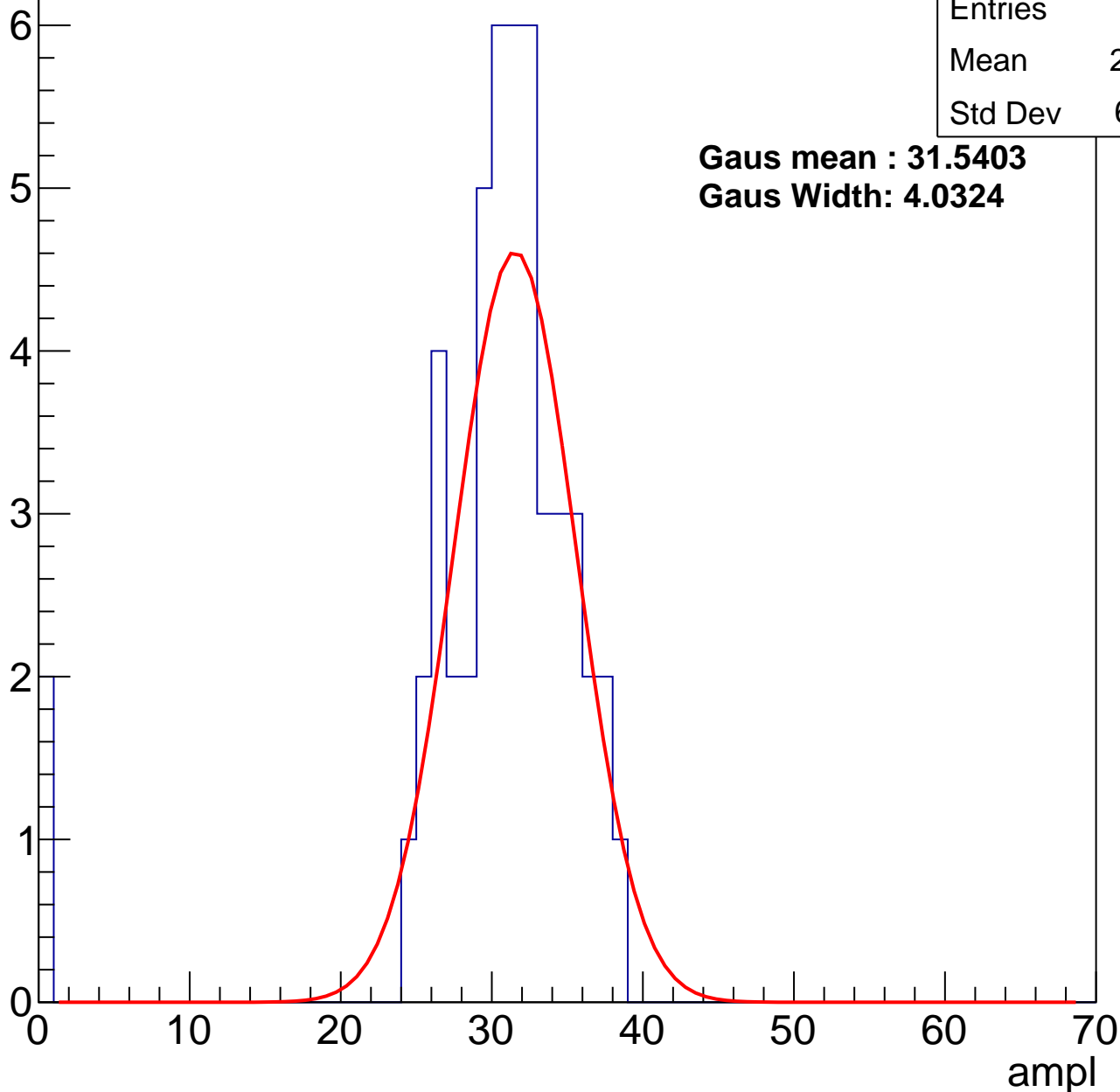
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	50
Mean	29.62
Std Dev	6.911

**Gaus mean : 31.5403**

**Gaus Width: 4.0324**



# B0L001S, U17-ch109, adc1

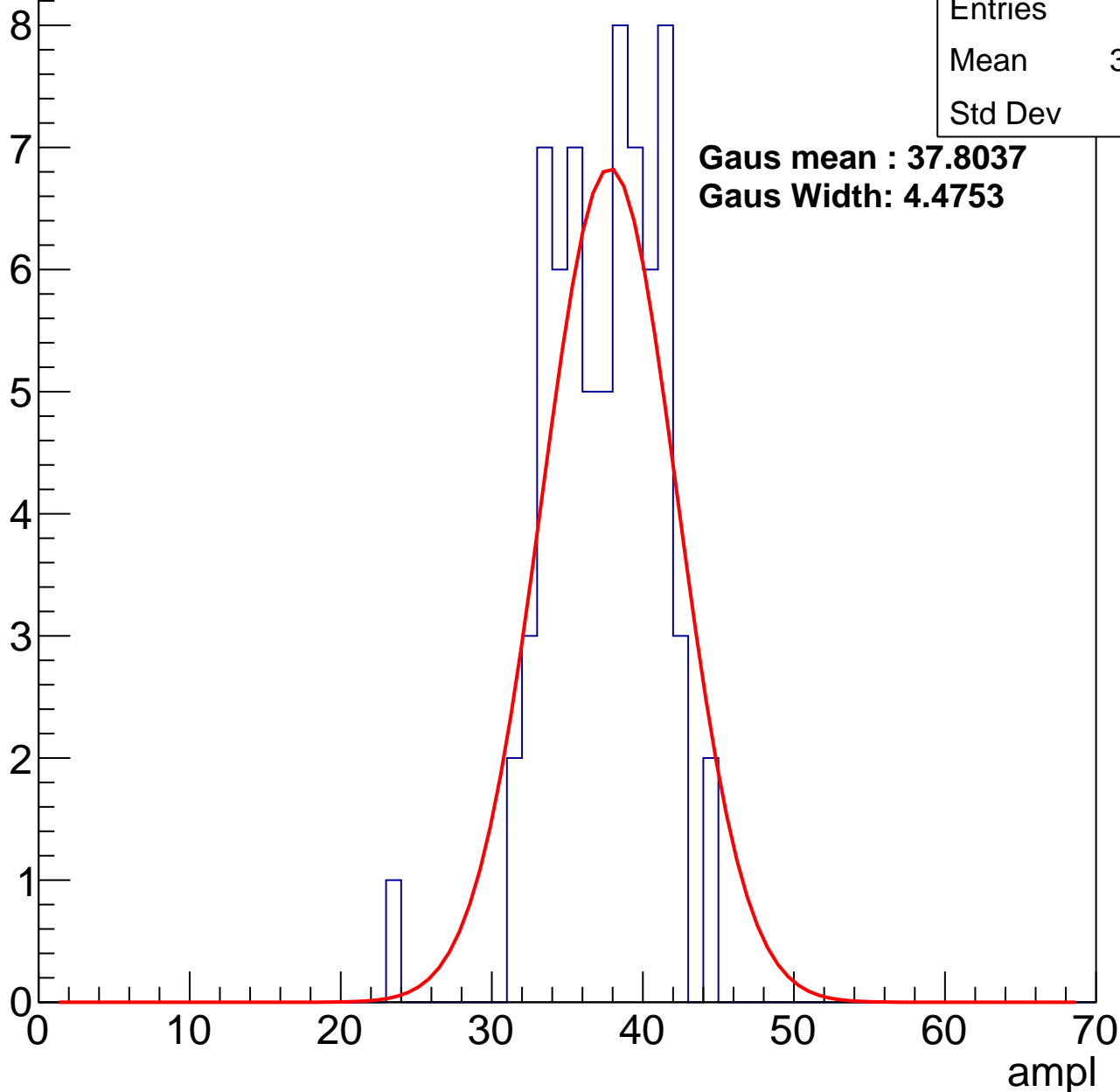
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	36.93
Std Dev	3.65

**Gaus mean : 37.8037**

**Gaus Width: 4.4753**



# B0L001S, U17-ch109, adc2

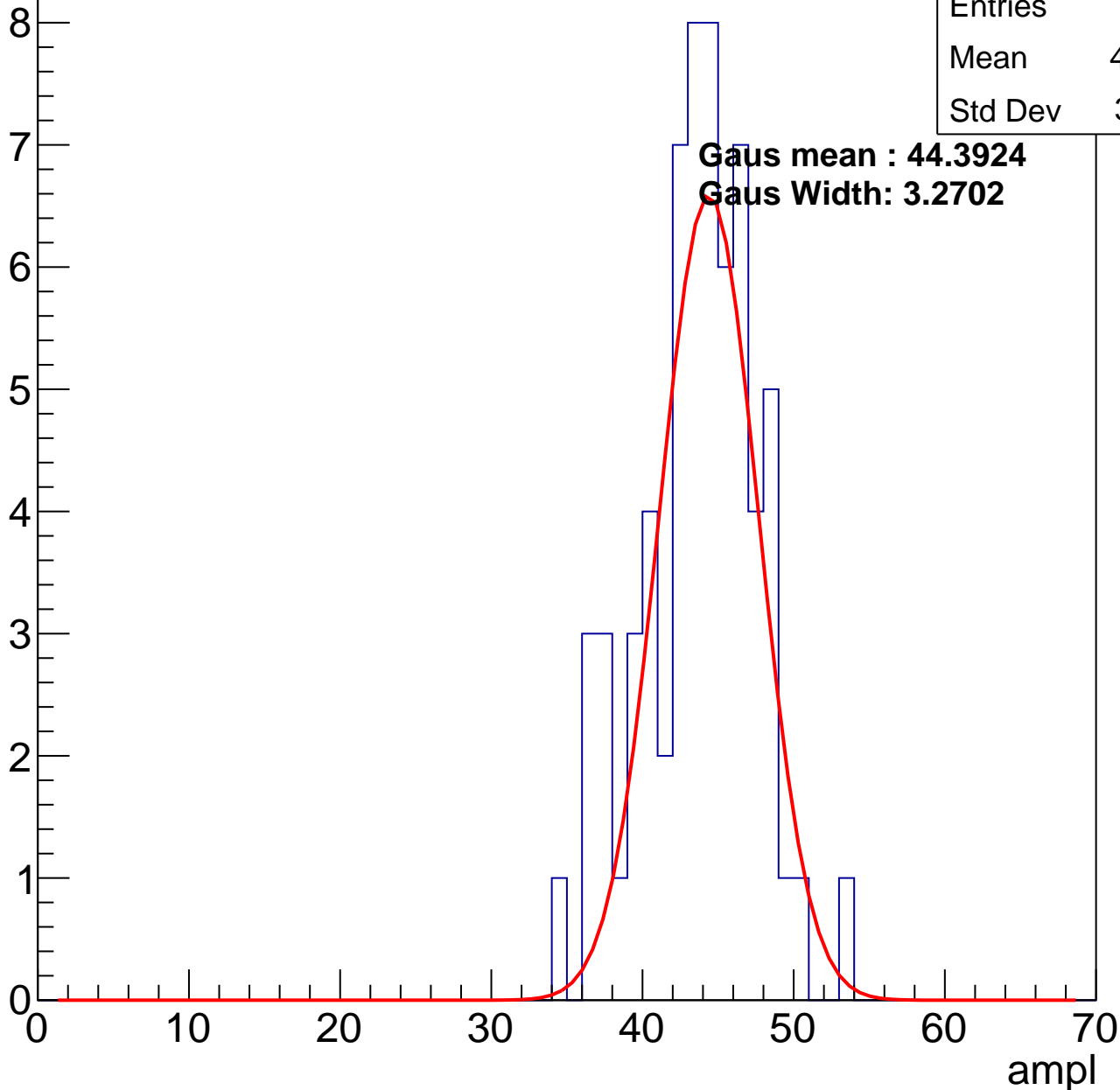
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	43.26
Std Dev	3.771

**Gaus mean : 44.3924**

**Gaus Width: 3.2702**

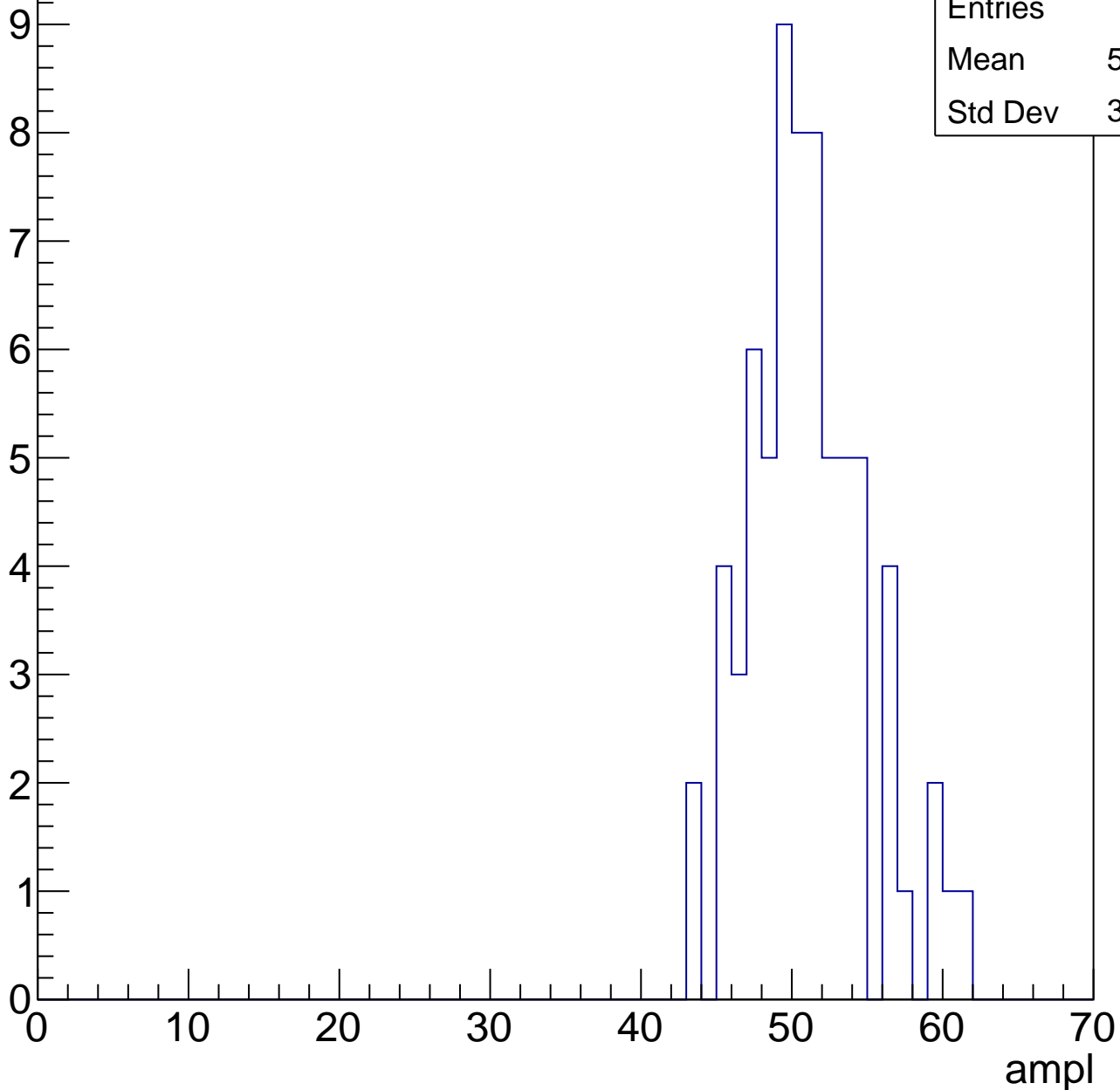


# B0L001S, U17-ch109, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	50.58
Std Dev	3.873

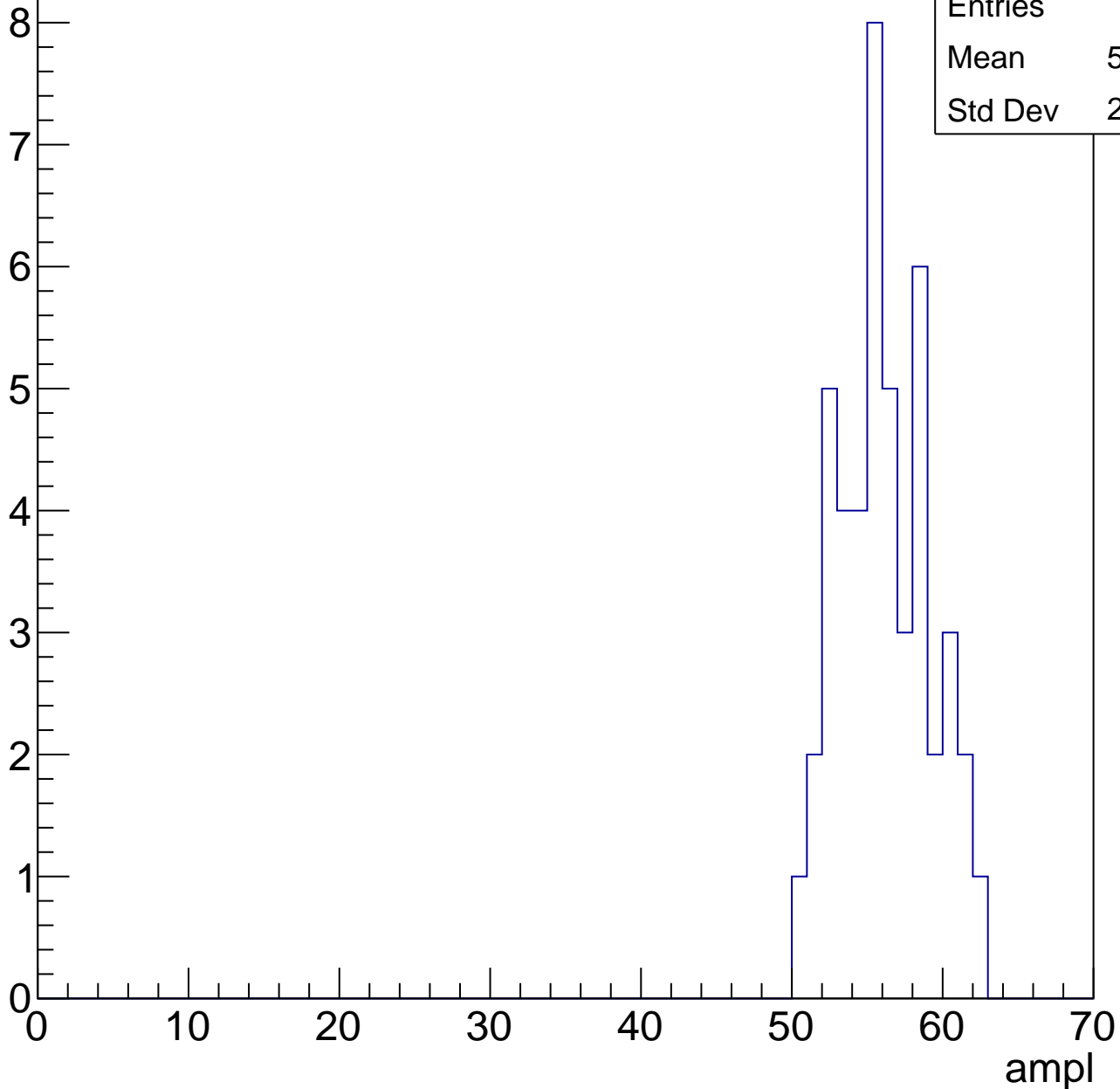


# B0L001S, U17-ch109, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	46
Mean	55.67
Std Dev	2.949

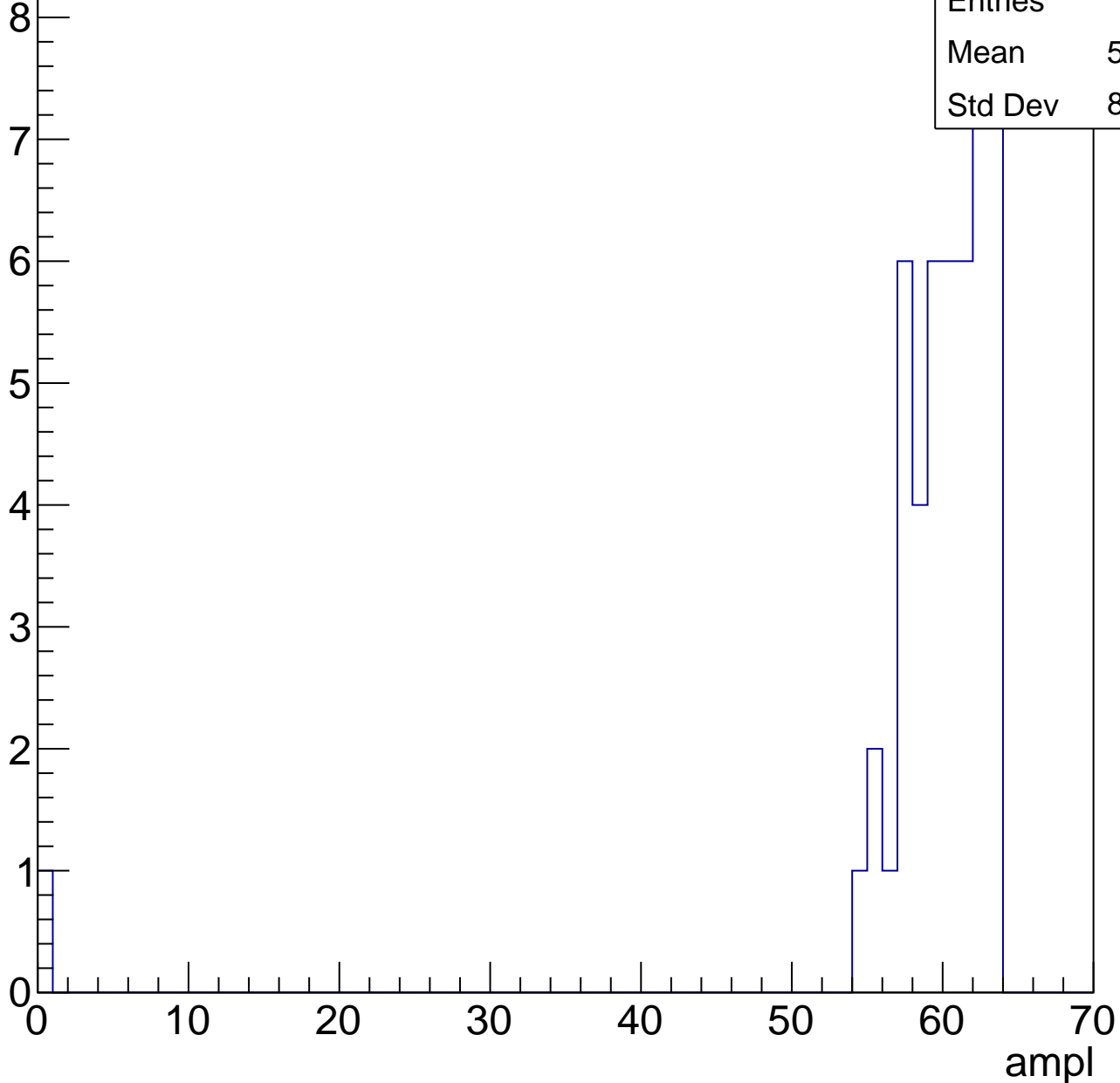


# B0L001S, U17-ch109, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	49
Mean	58.65
Std Dev	8.805



# B0L001S, U17-ch109, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	62.25
Std Dev	0.8292

ampl

0 10 20 30 40 50 60 70



# B0L001S, U17-ch109, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U17-ch110, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	79
Mean	30.75
Std Dev	4.675

**Gaus mean : 31.7818**

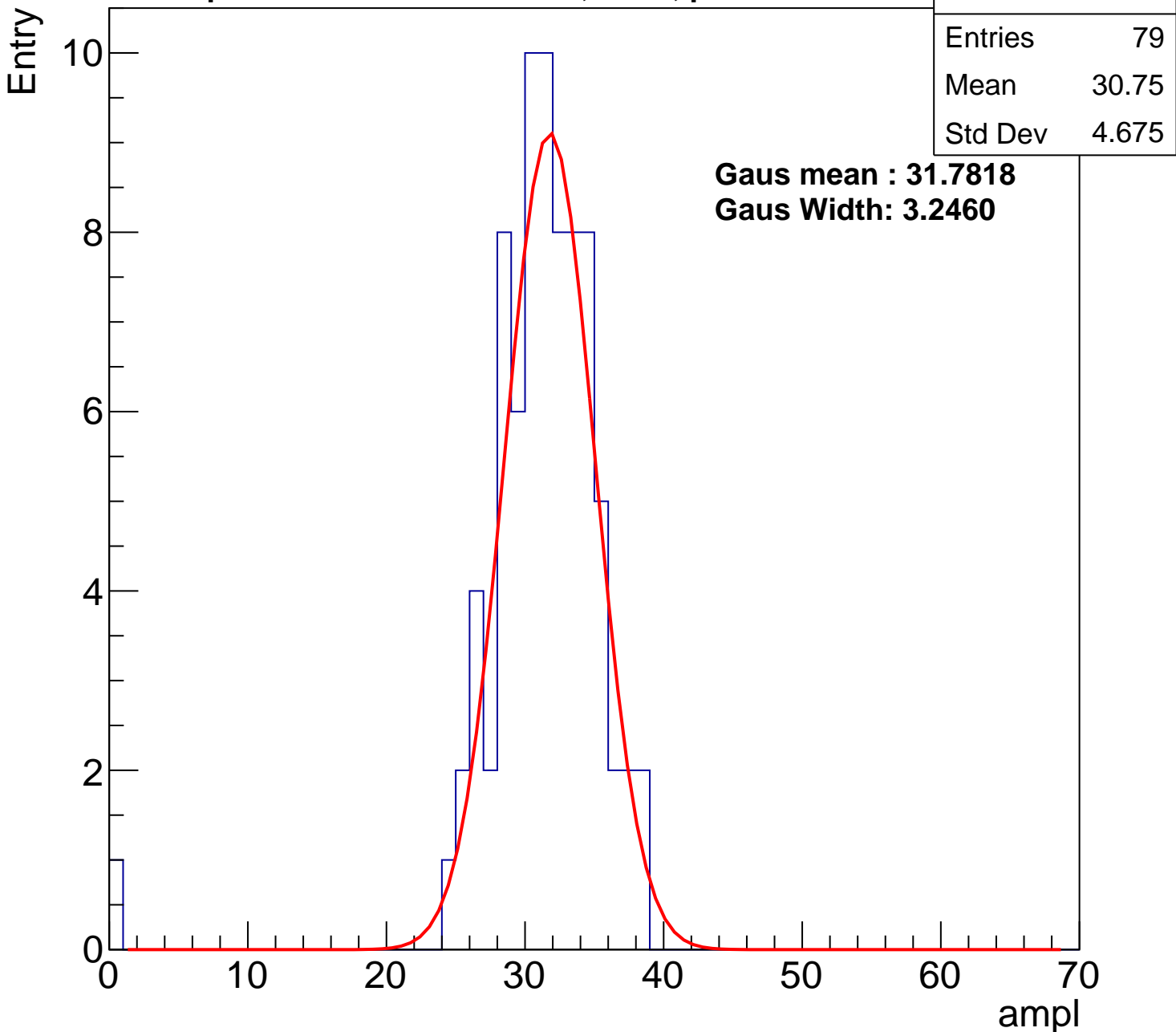
**Gaus Width: 3.2460**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U17-ch110, adc1

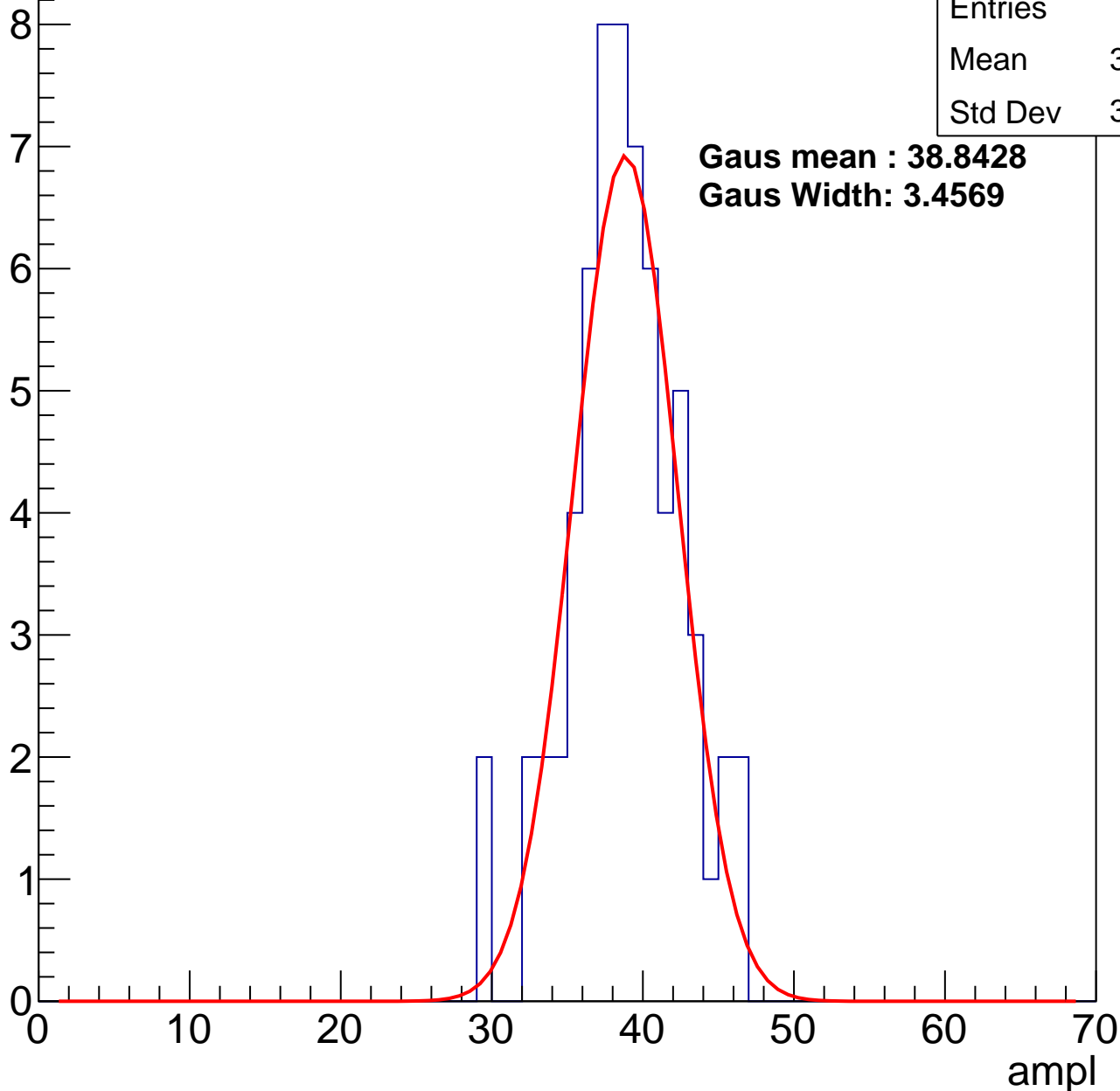
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	38.34
Std Dev	3.667

**Gaus mean : 38.8428**

**Gaus Width: 3.4569**



# B0L001S, U17-ch110, adc2

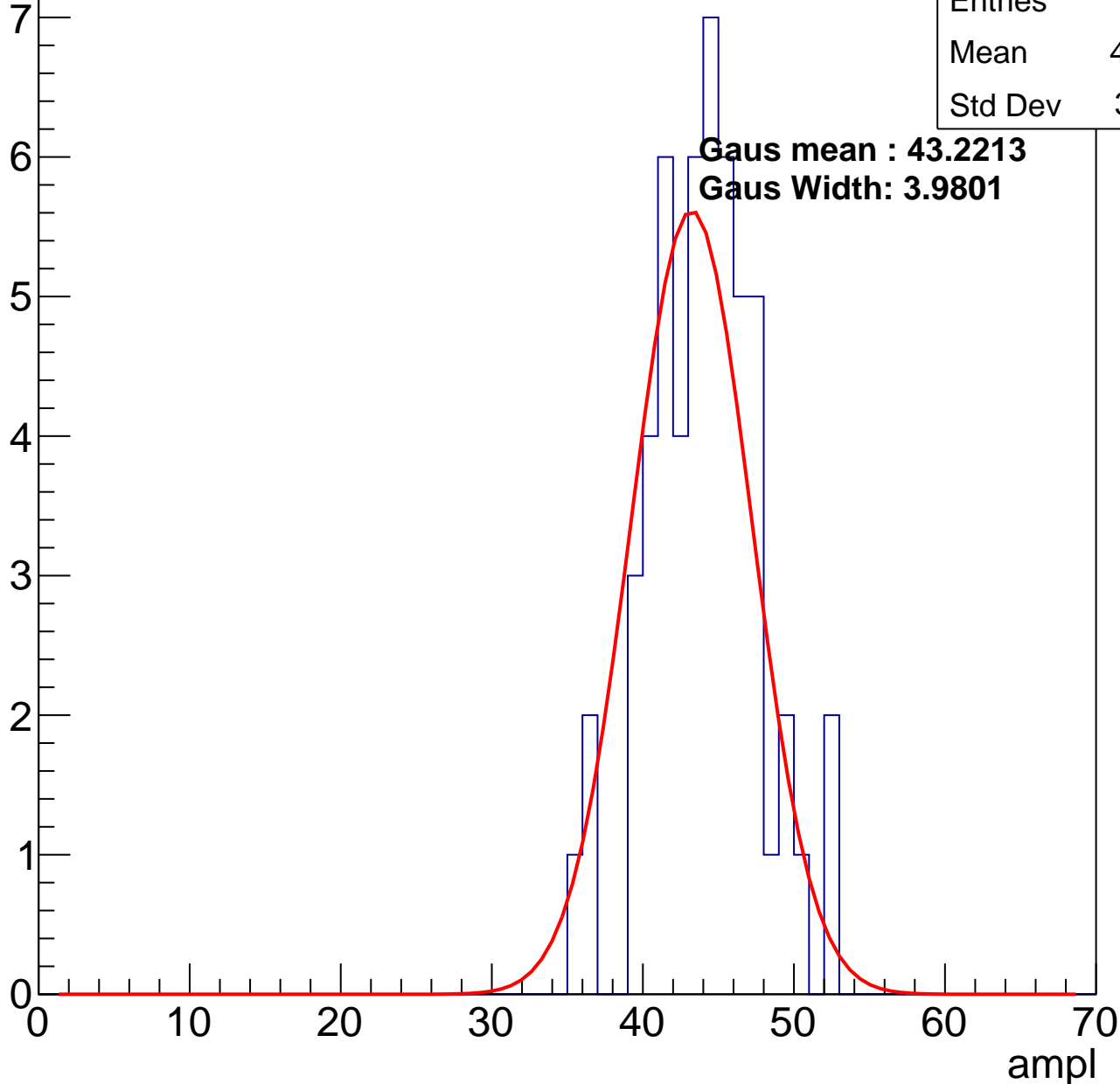
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	43.62
Std Dev	3.611

**Gaus mean : 43.2213**

**Gaus Width: 3.9801**

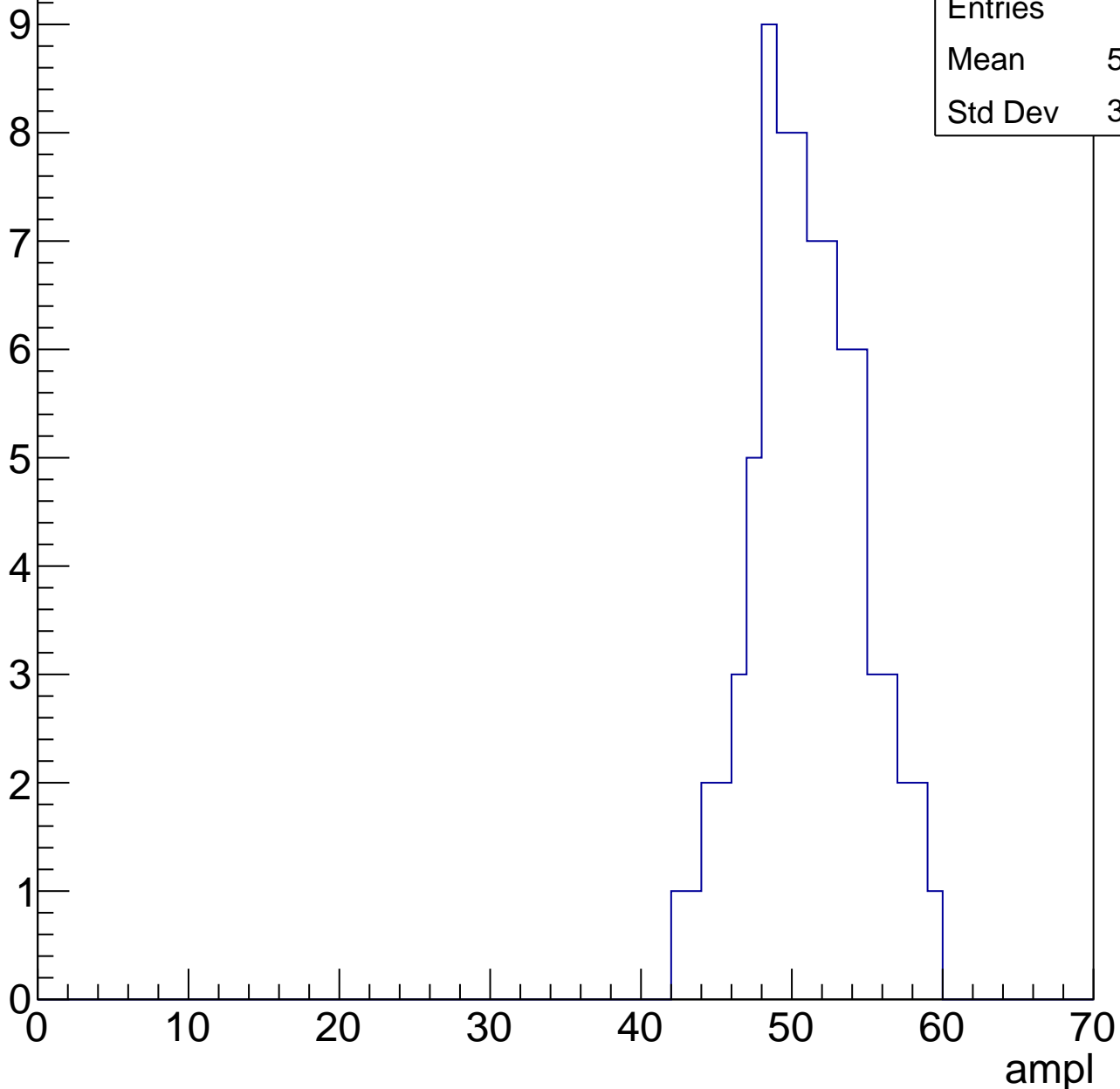


# B0L001S, U17-ch110, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

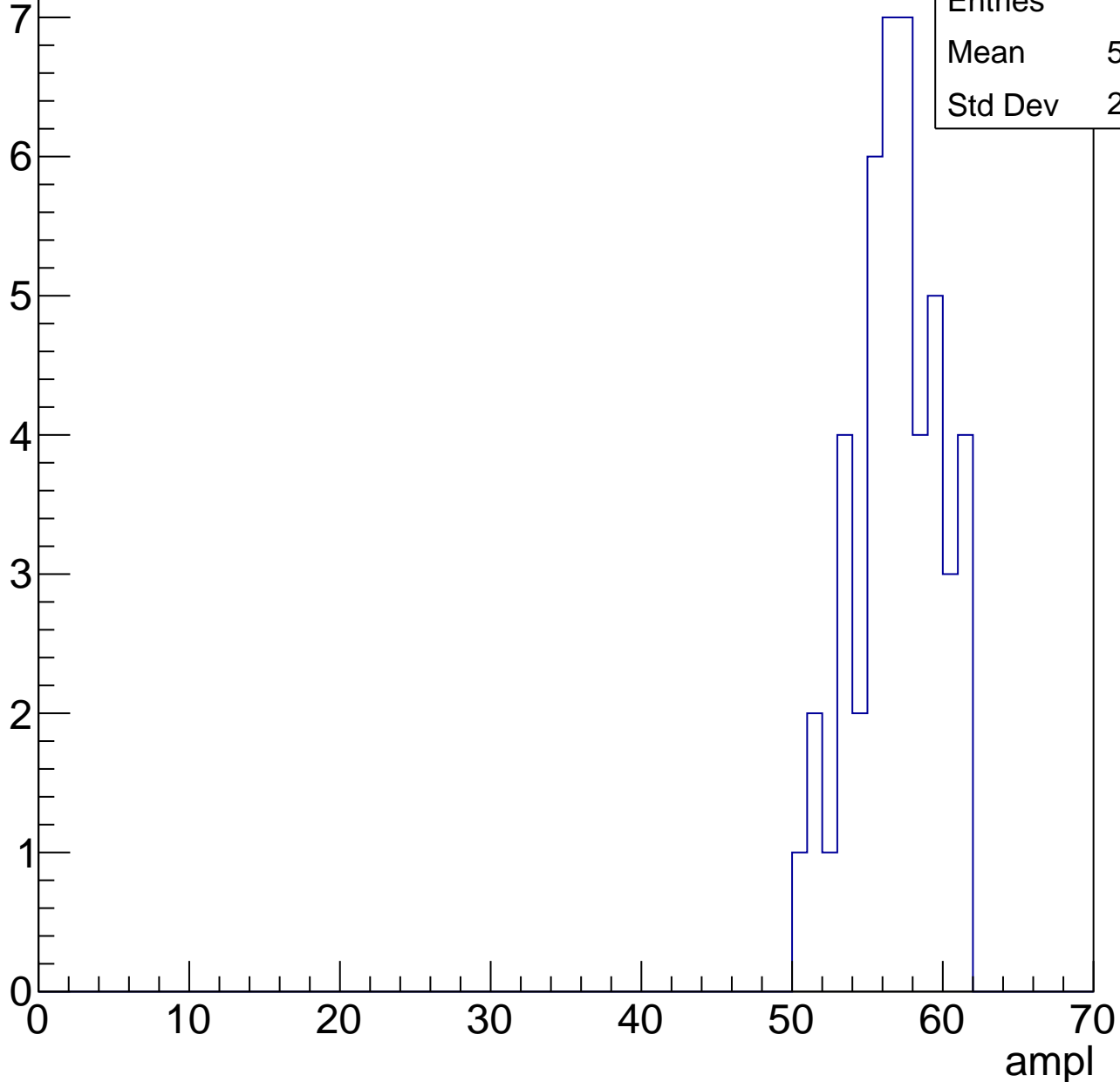
Entries	76
Mean	50.59
Std Dev	3.664



# B0L001S, U17-ch110, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



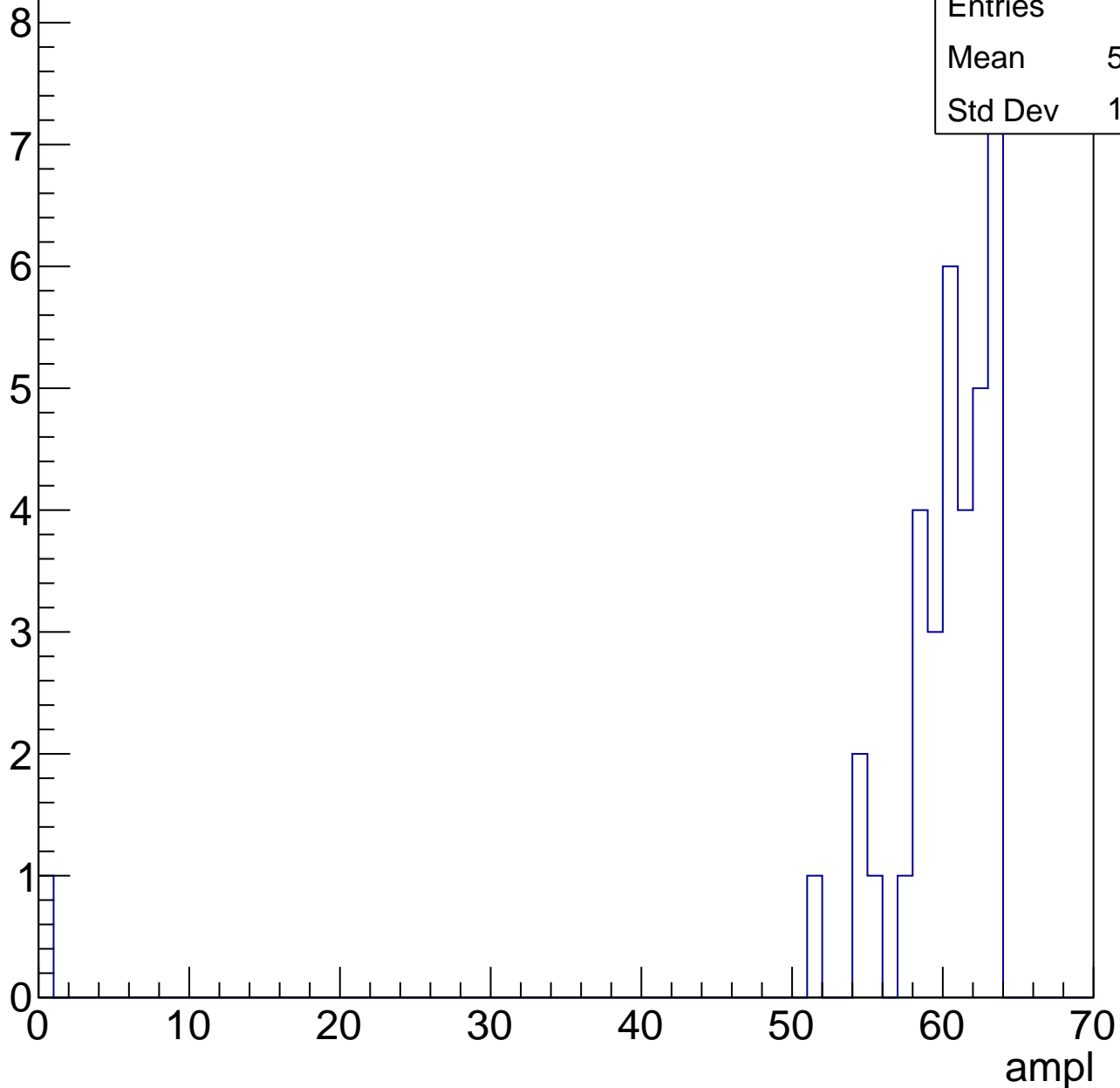
Entries	46
Mean	56.43
Std Dev	2.795

# B0L001S, U17-ch110, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	36
Mean	58.28
Std Dev	10.27

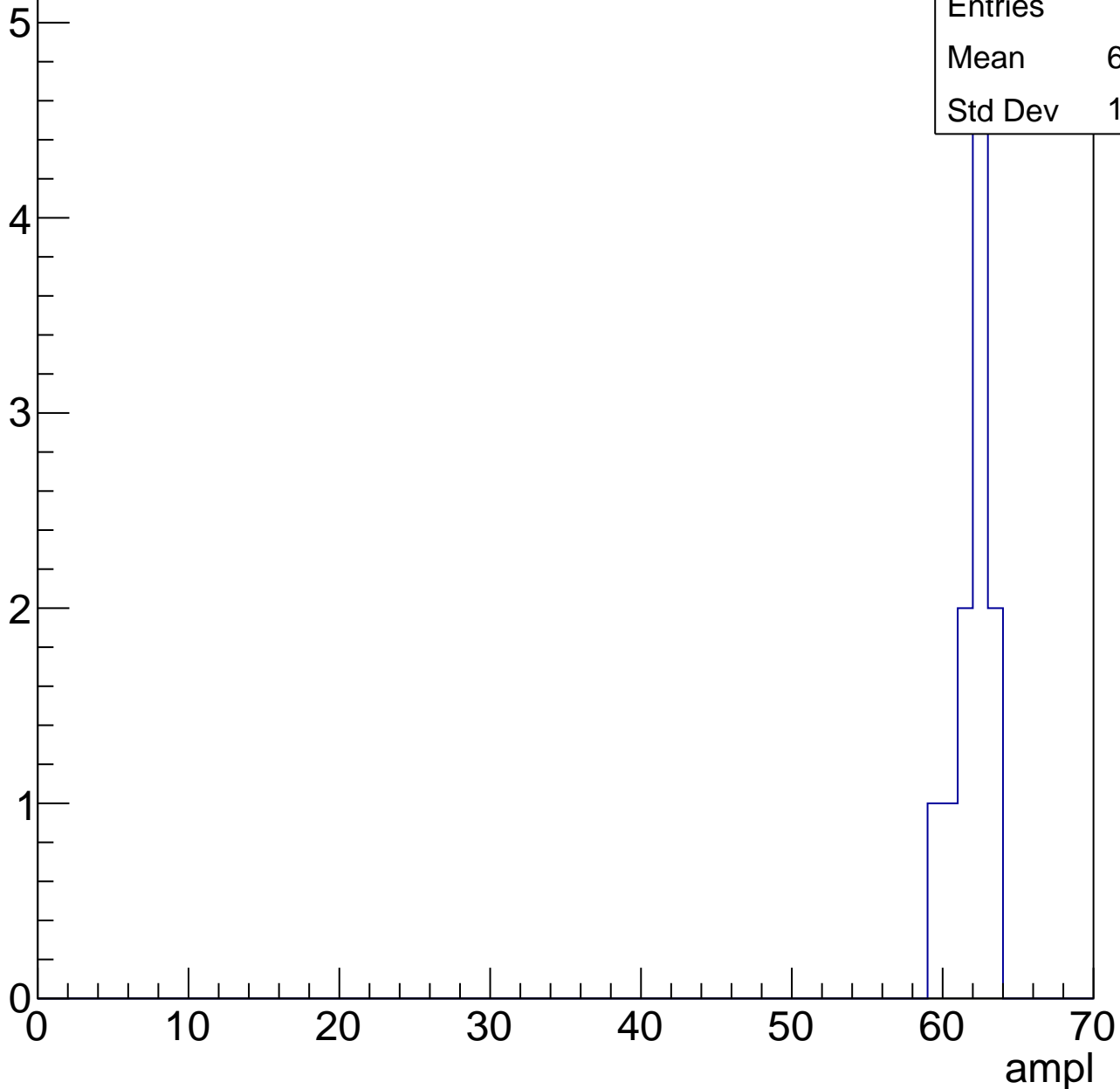


# B0L001S, U17-ch110, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	11
Mean	61.55
Std Dev	1.157





# B0L001S, U17-ch110, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	3
Mean	0
Std Dev	0

# B0L001S, U17-ch111, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	62
Mean	30.15
Std Dev	6.418

**Gaus mean : 32.2249**

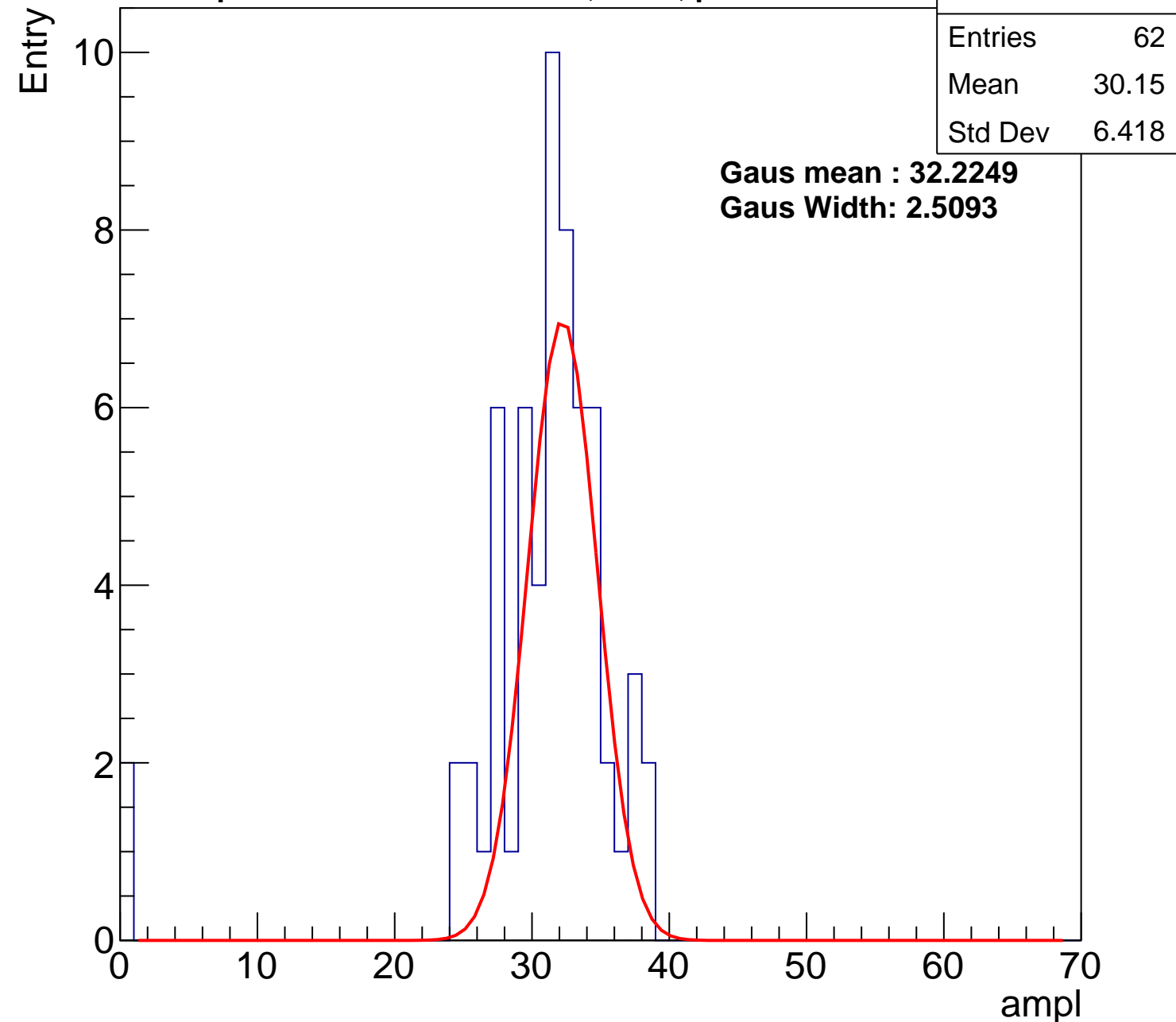
**Gaus Width: 2.5093**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U17-ch111, adc1

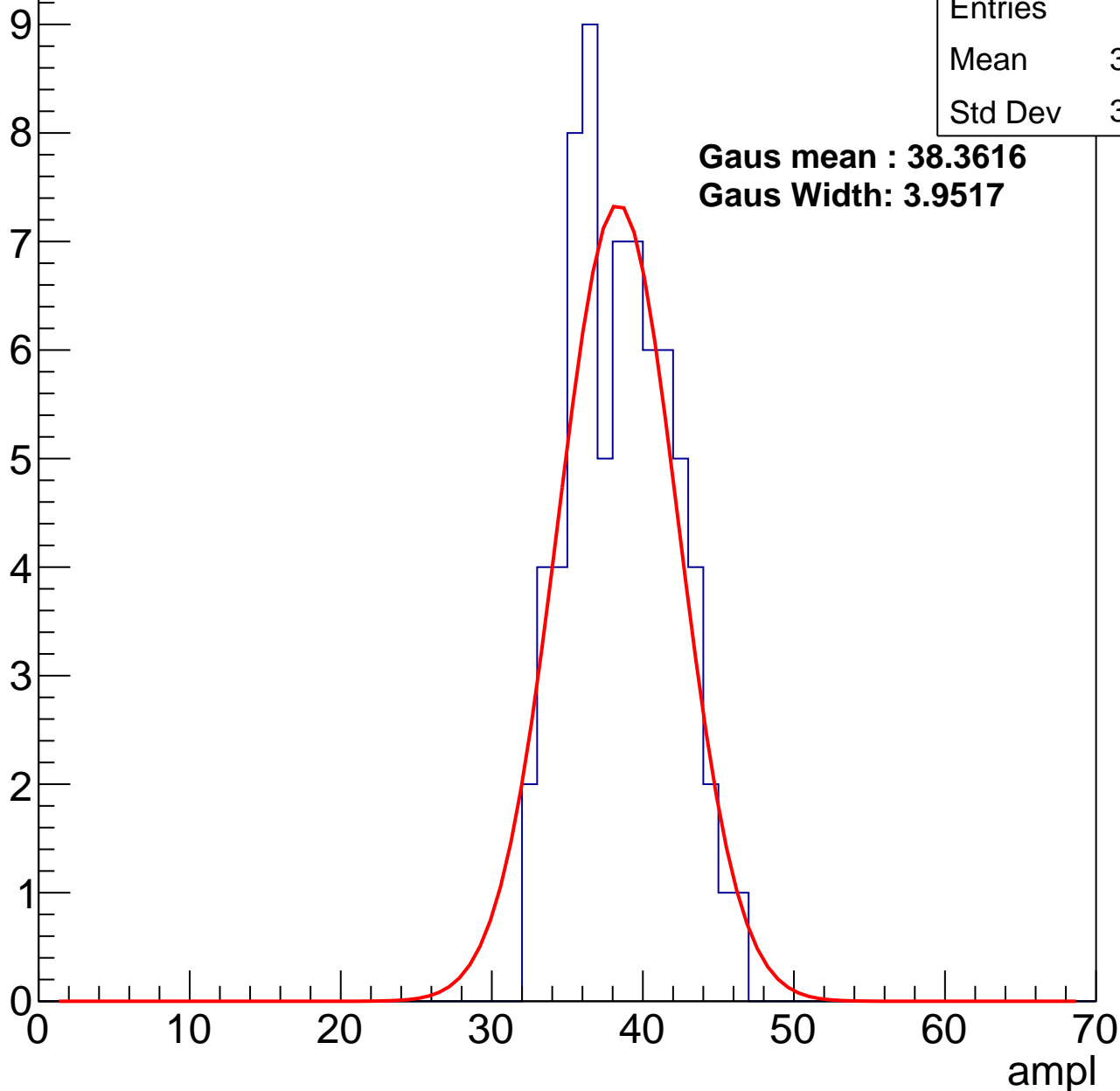
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	38.13
Std Dev	3.352

**Gaus mean : 38.3616**

**Gaus Width: 3.9517**



# B0L001S, U17-ch111, adc2

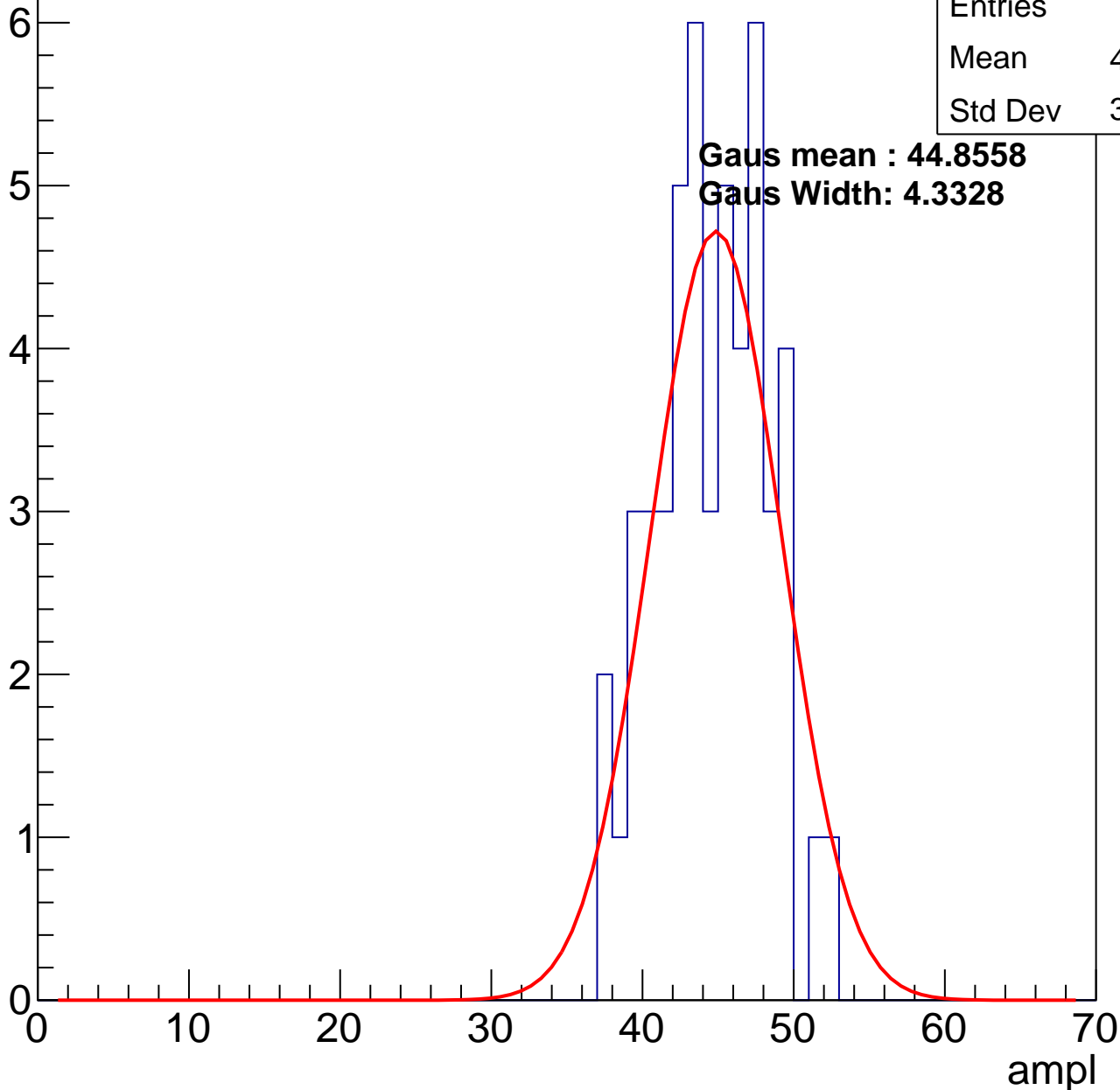
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	50
Mean	44.12
Std Dev	3.592

**Gaus mean : 44.8558**

**Gaus Width: 4.3328**

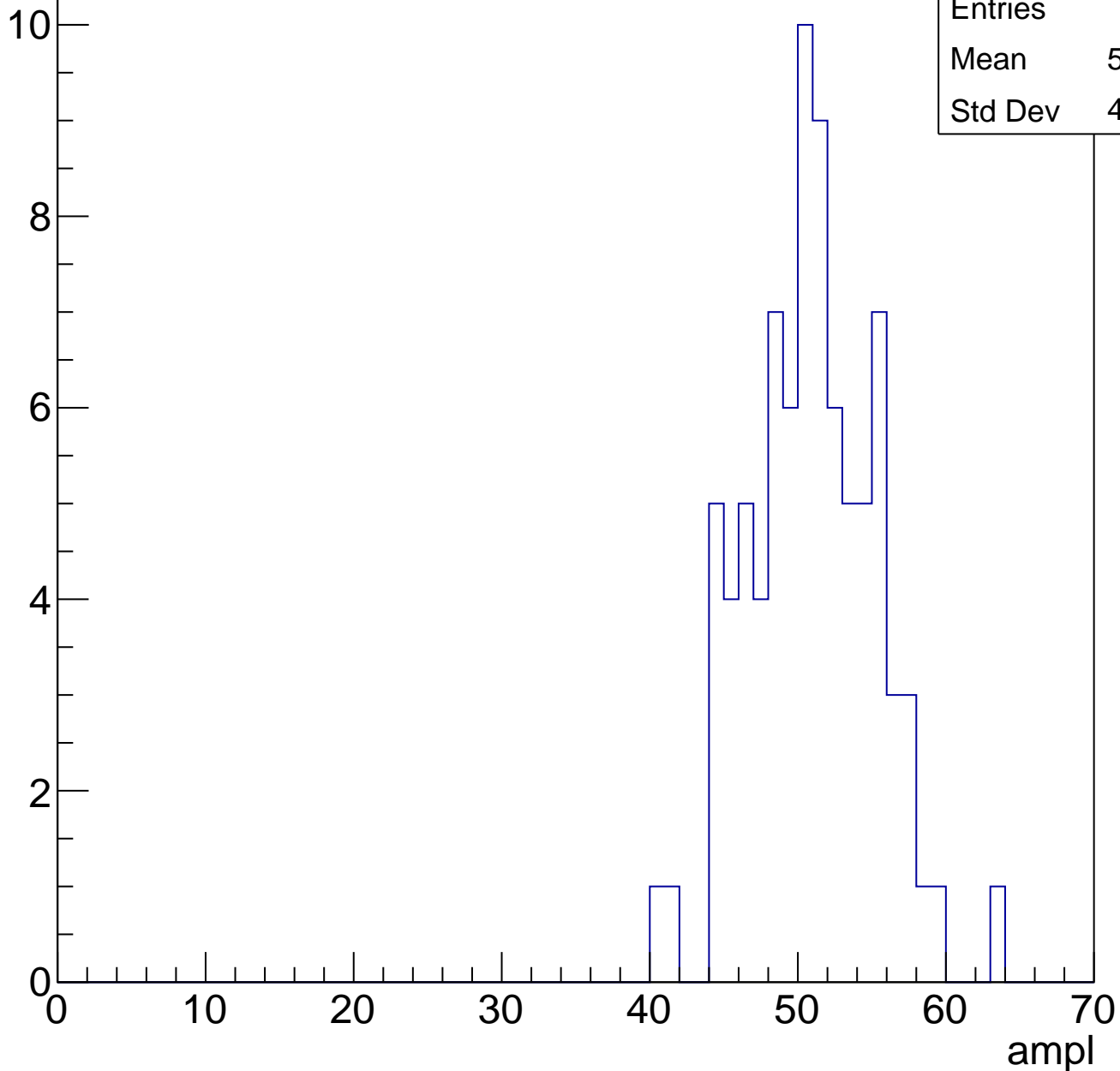


# B0L001S, U17-ch111, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	84
Mean	50.46
Std Dev	4.219

Entry

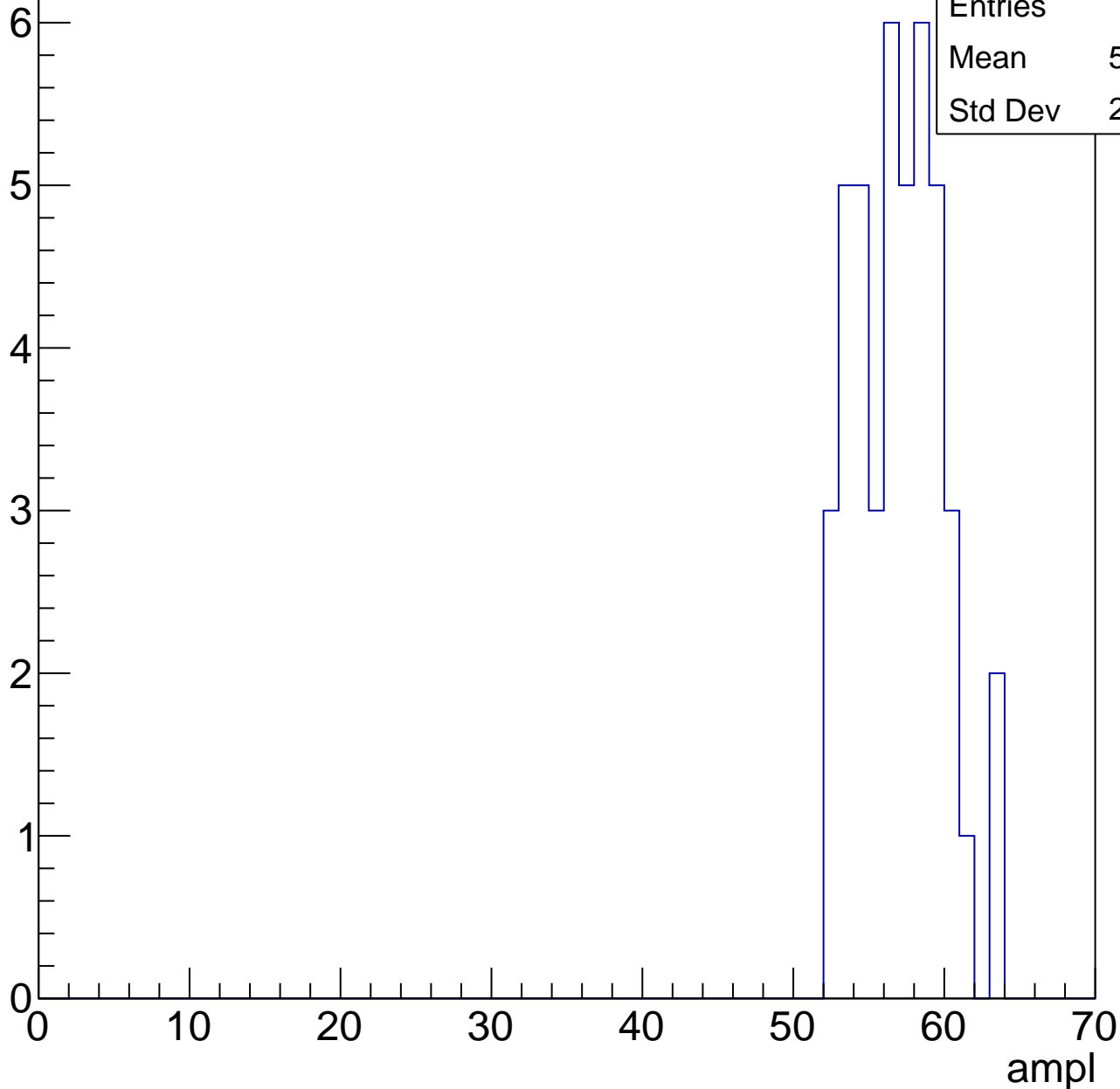


# B0L001S, U17-ch111, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	44
Mean	56.52
Std Dev	2.816

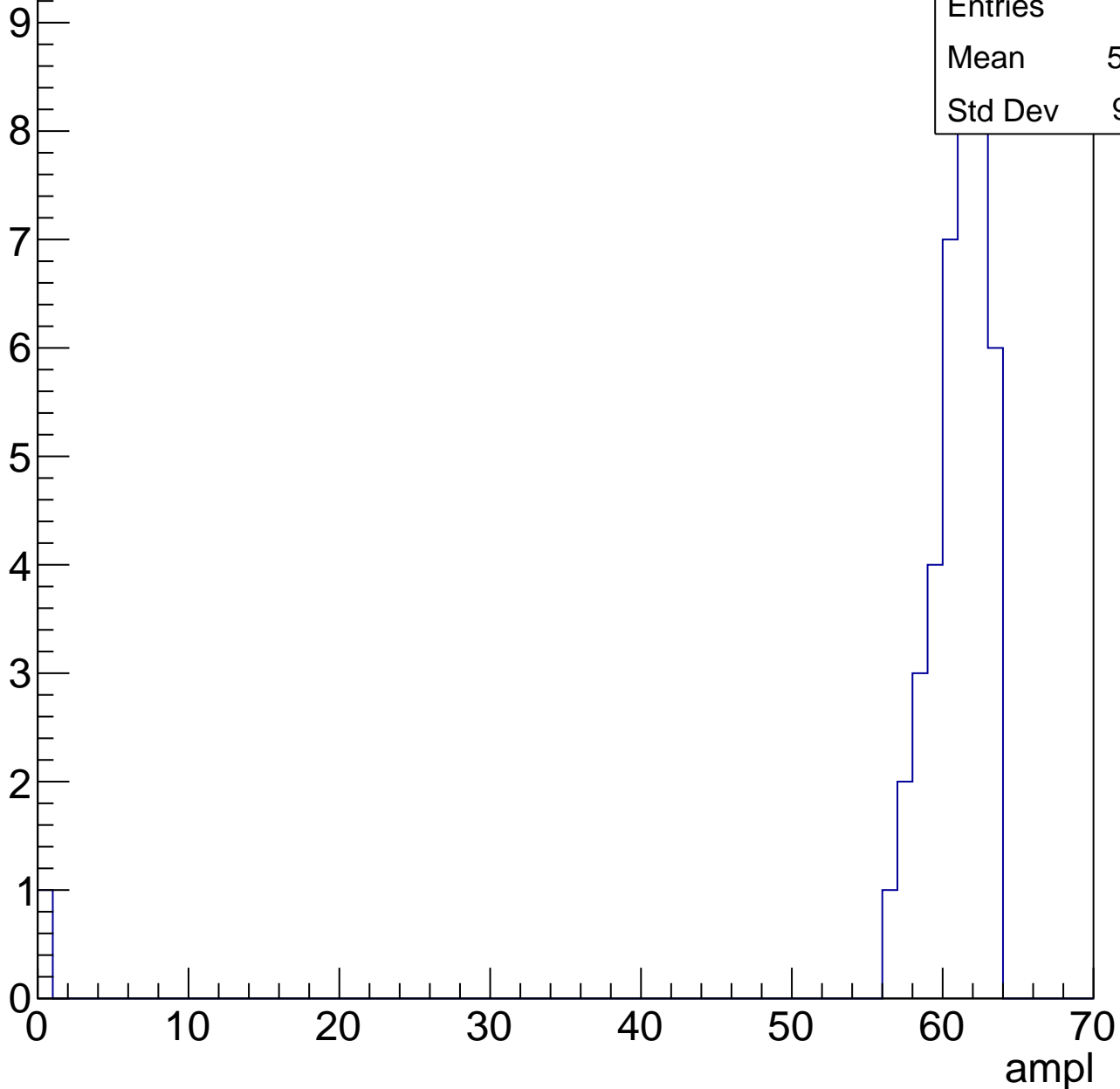


# B0L001S, U17-ch111, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

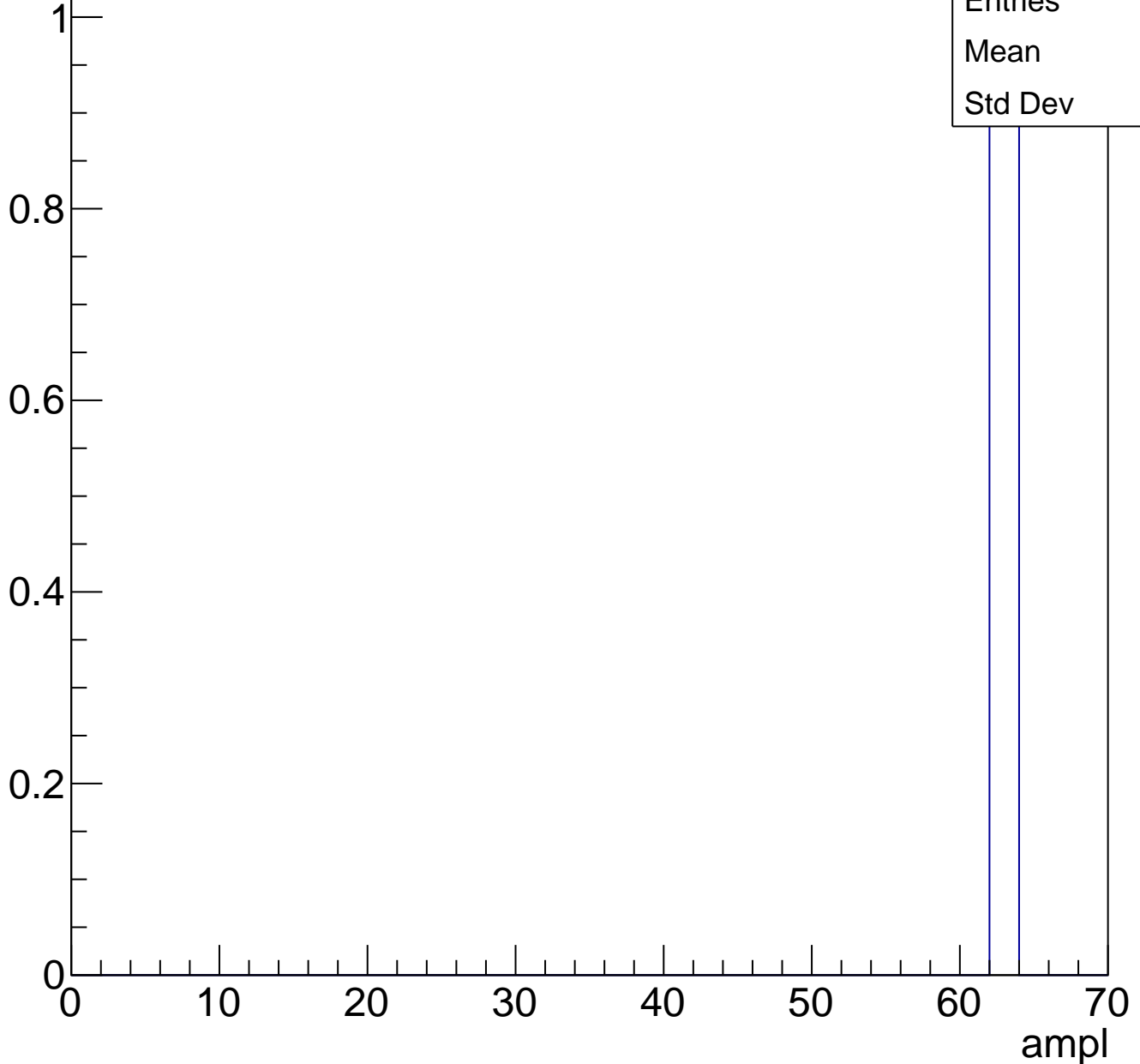
Entries	42
Mean	59.17
Std Dev	9.411



# B0L001S, U17-ch111, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch111, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U17-ch112, adc0

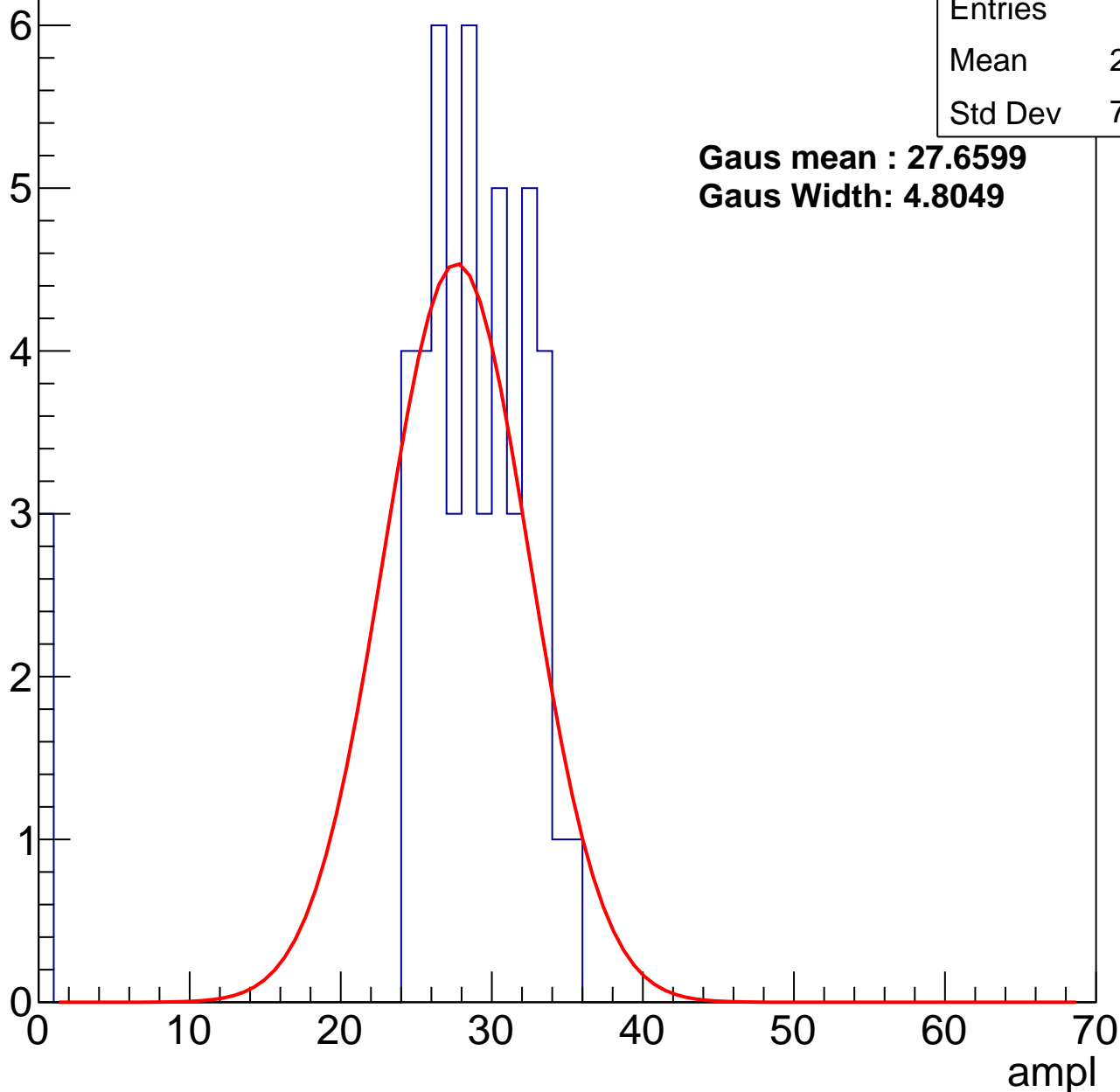
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	48
Mean	26.92
Std Dev	7.552

**Gaus mean : 27.6599**

**Gaus Width: 4.8049**



# B0L001S, U17-ch112, adc1

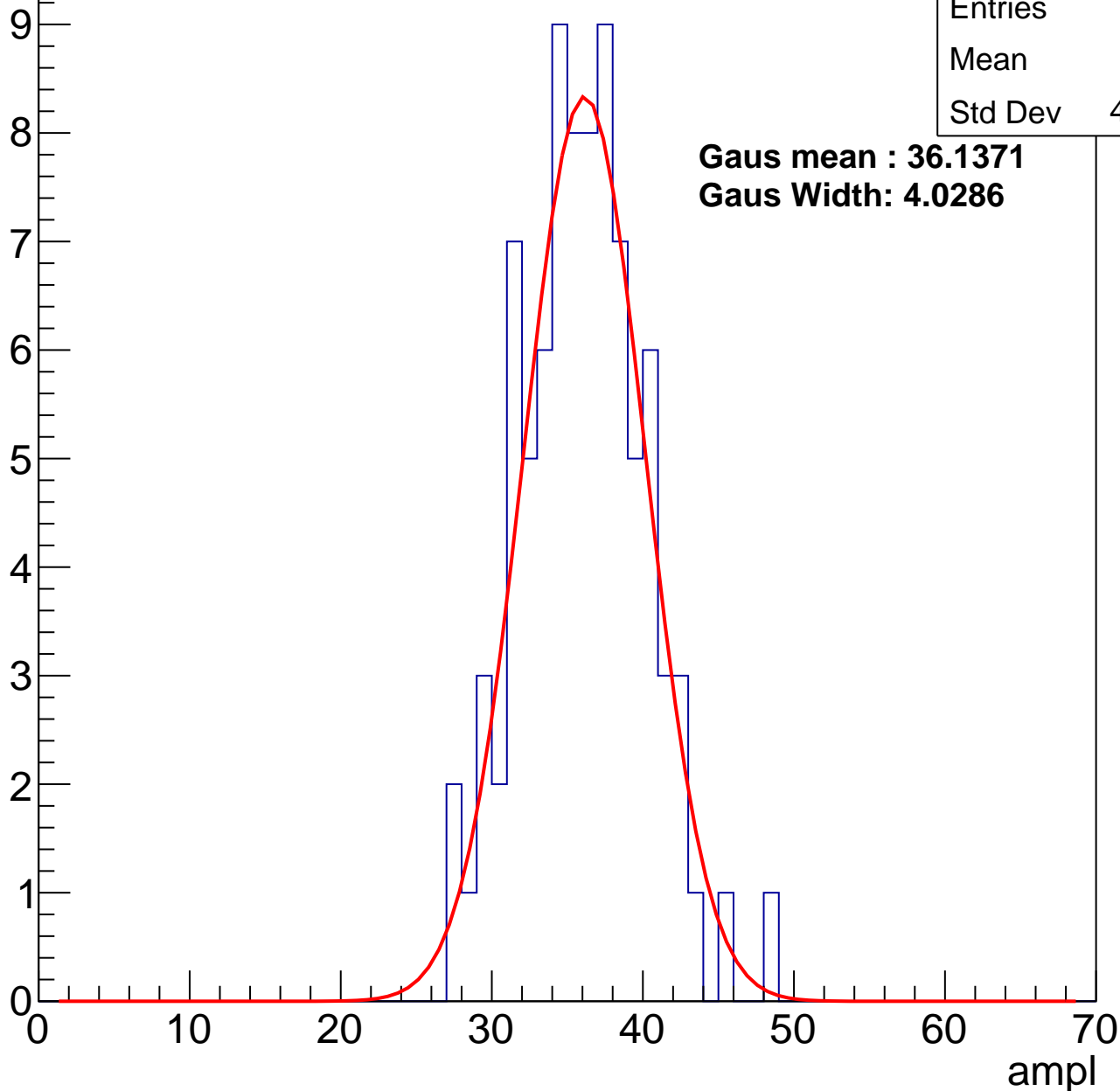
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	87
Mean	35.6
Std Dev	4.038

**Gaus mean : 36.1371**

**Gaus Width: 4.0286**



# B0L001S, U17-ch112, adc2

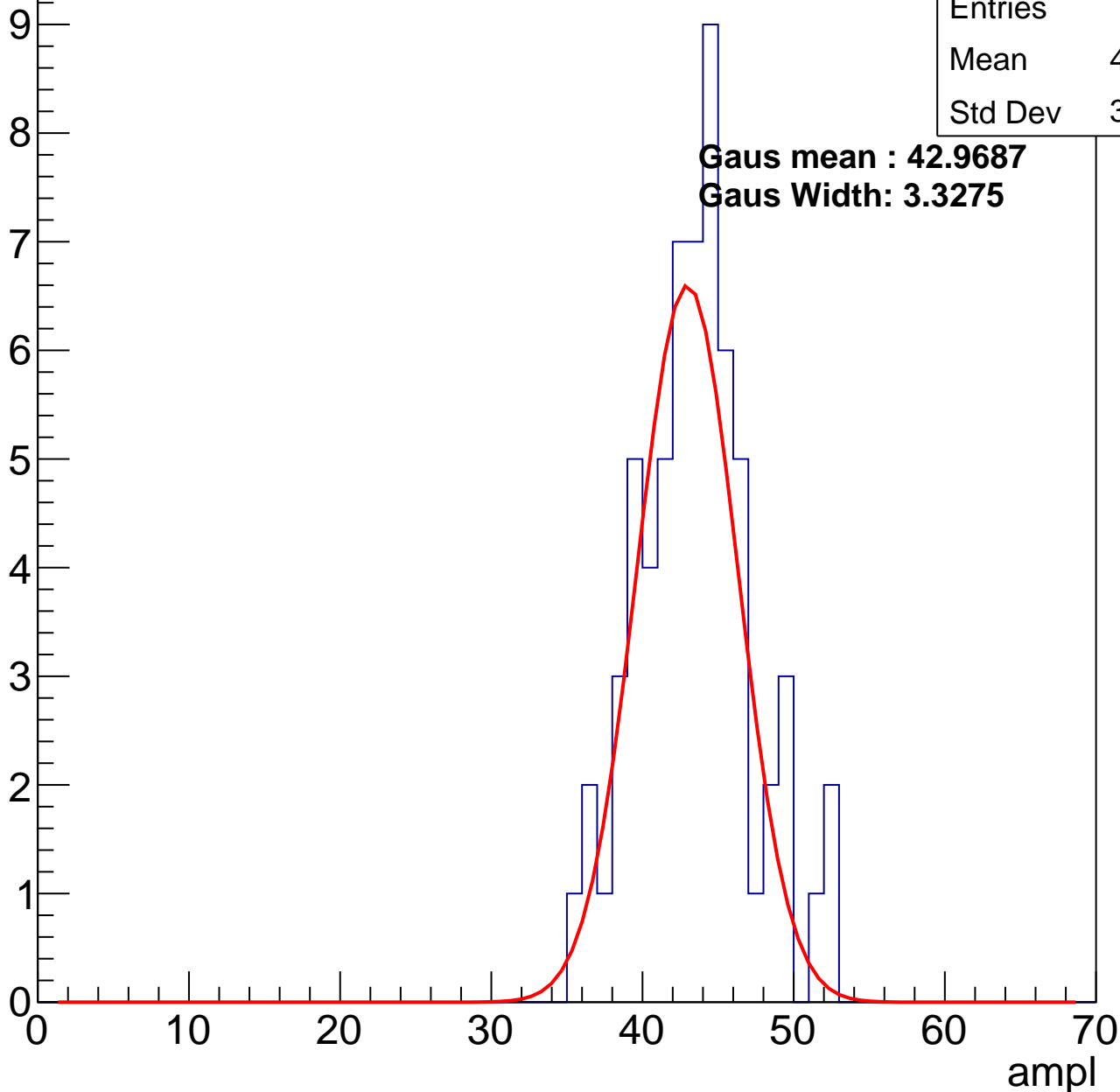
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	43.03
Std Dev	3.737

**Gaus mean : 42.9687**

**Gaus Width: 3.3275**

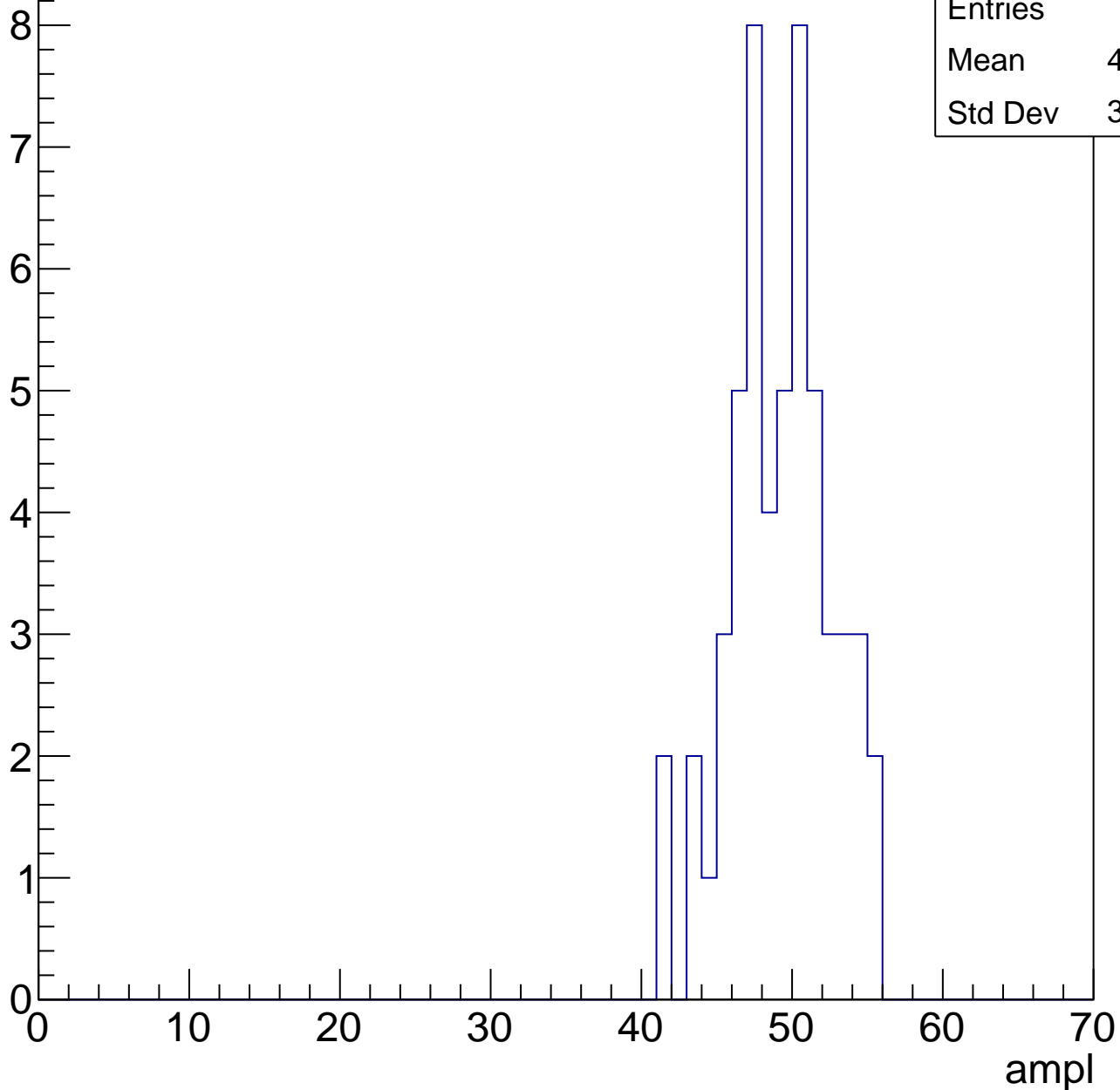


# B0L001S, U17-ch112, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	48.74
Std Dev	3.334

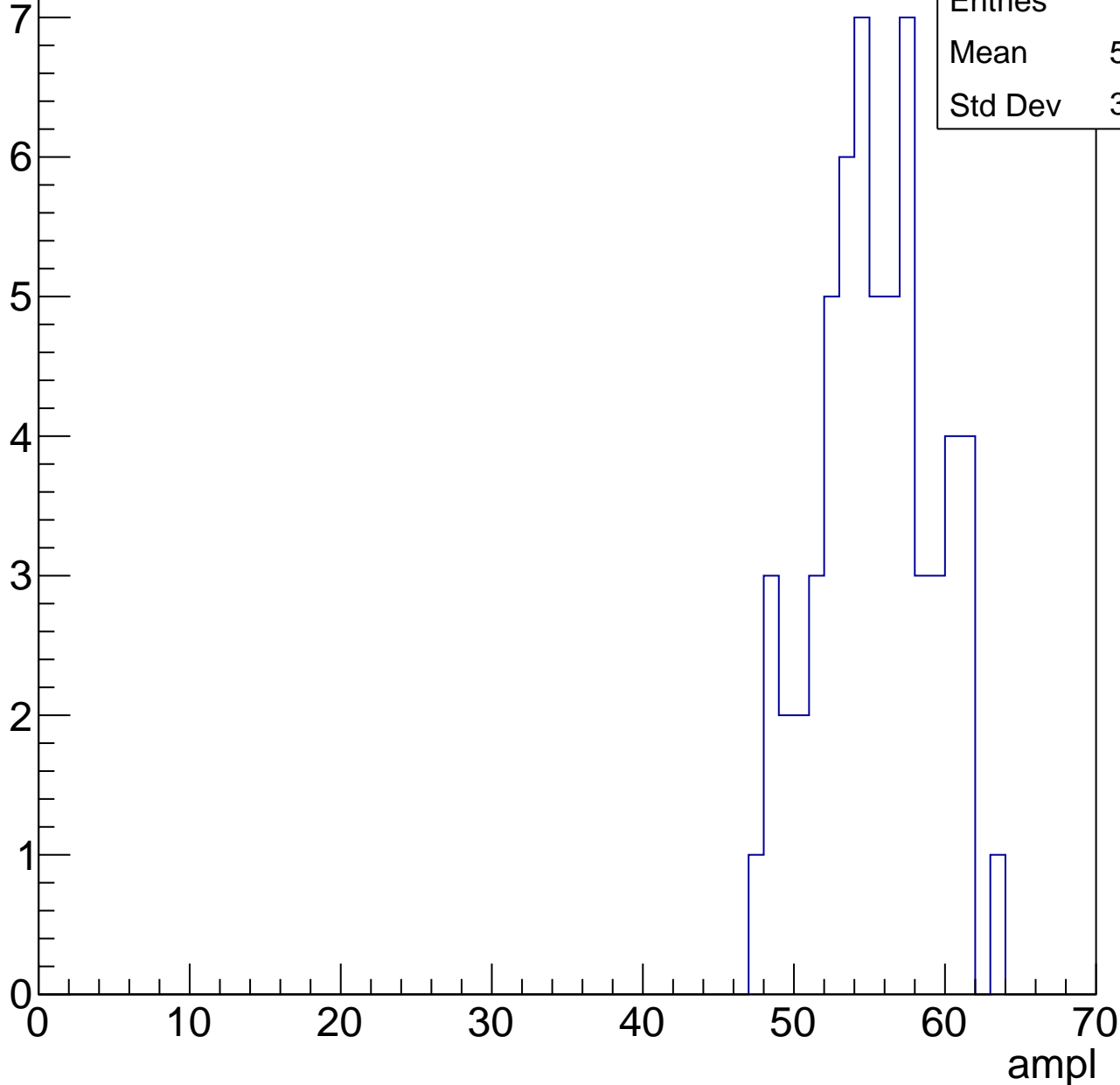


# B0L001S, U17-ch112, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	54.92
Std Dev	3.782

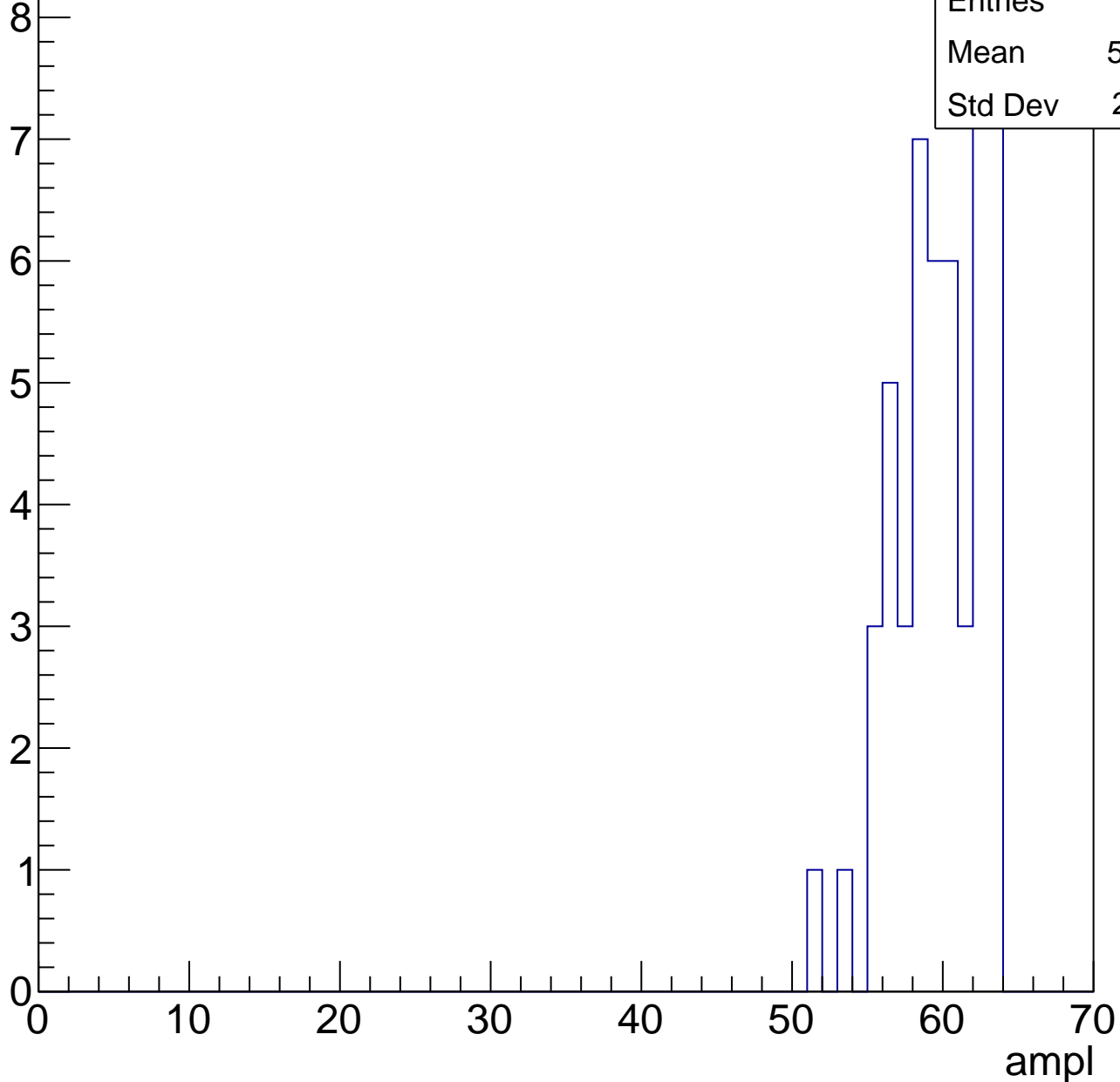


# B0L001S, U17-ch112, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

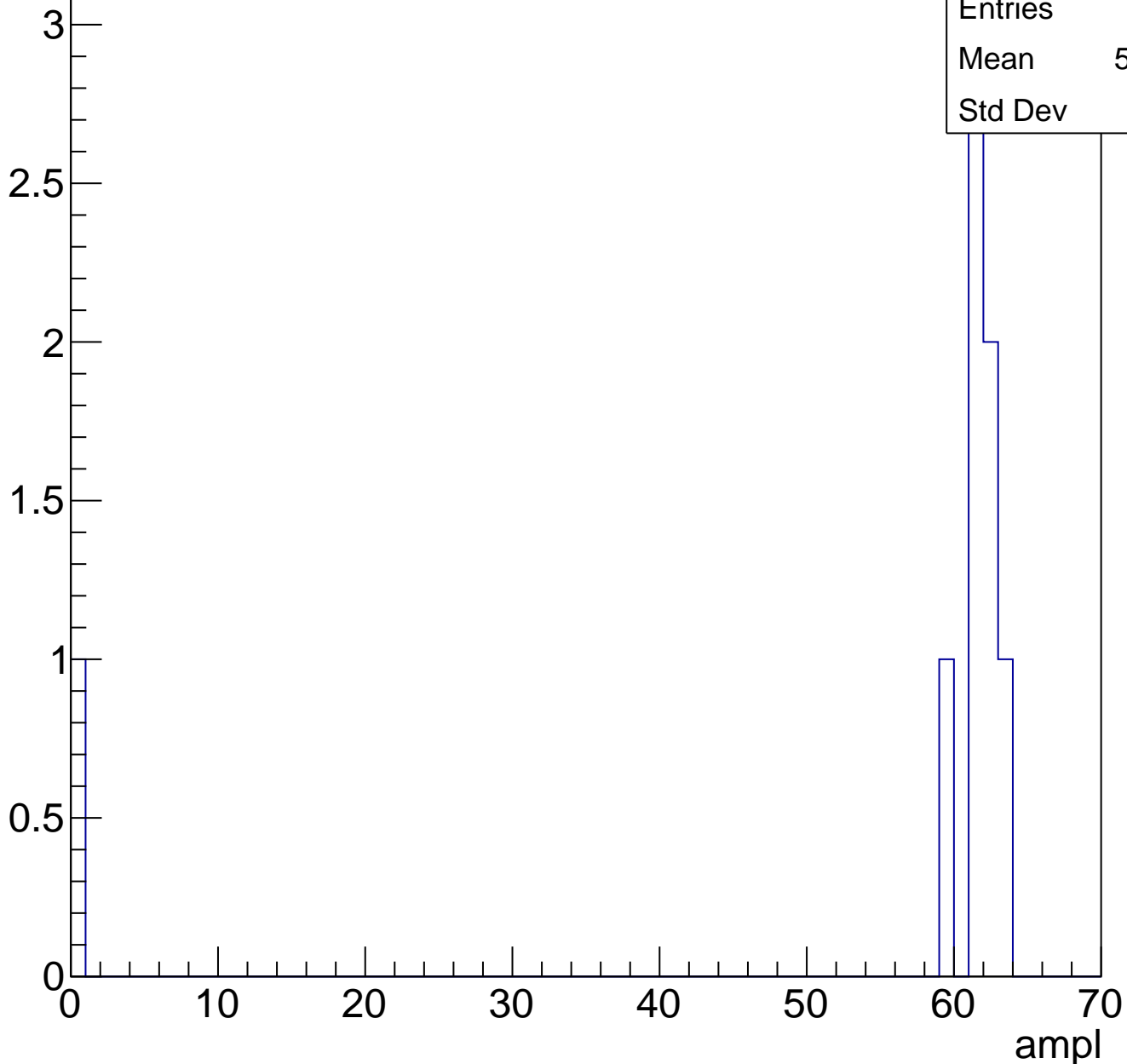
Entries	51
Mean	59.27
Std Dev	2.891



# B0L001S, U17-ch112, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch112, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U17-ch113, adc0

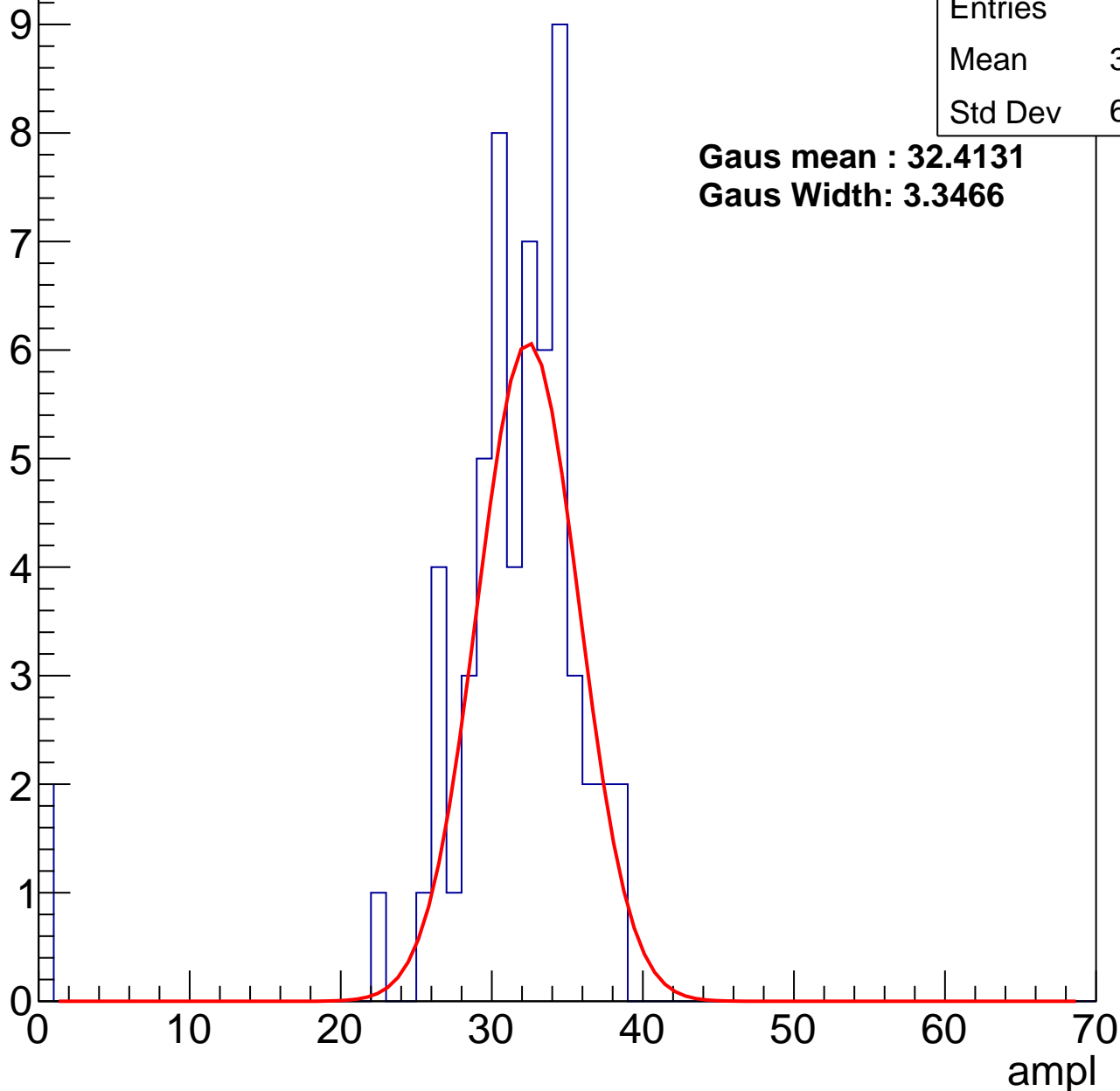
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	30.43
Std Dev	6.546

**Gaus mean : 32.4131**

**Gaus Width: 3.3466**



# B0L001S, U17-ch113, adc1

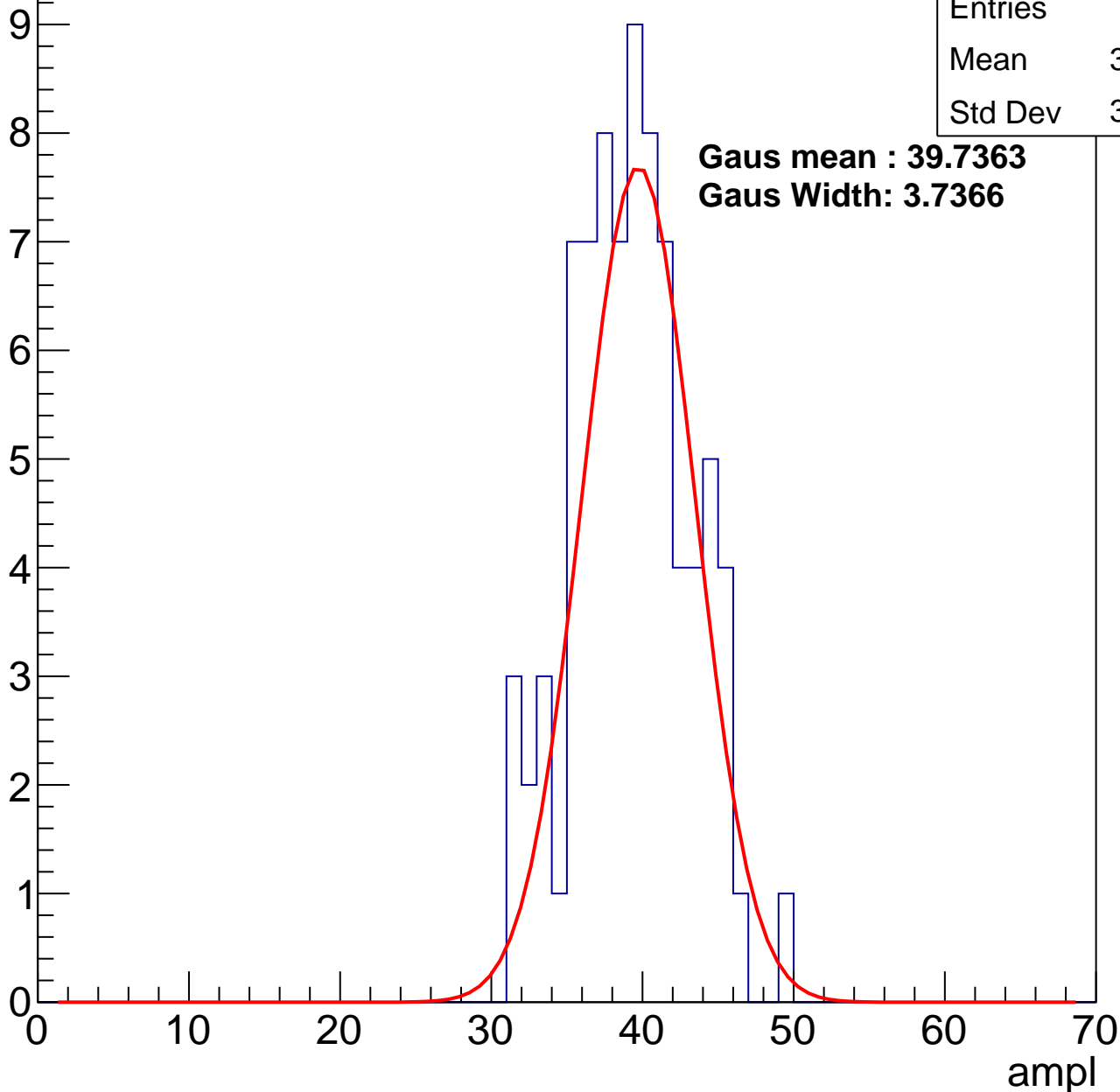
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	81
Mean	38.79
Std Dev	3.829

**Gaus mean : 39.7363**

**Gaus Width: 3.7366**



# B0L001S, U17-ch113, adc2

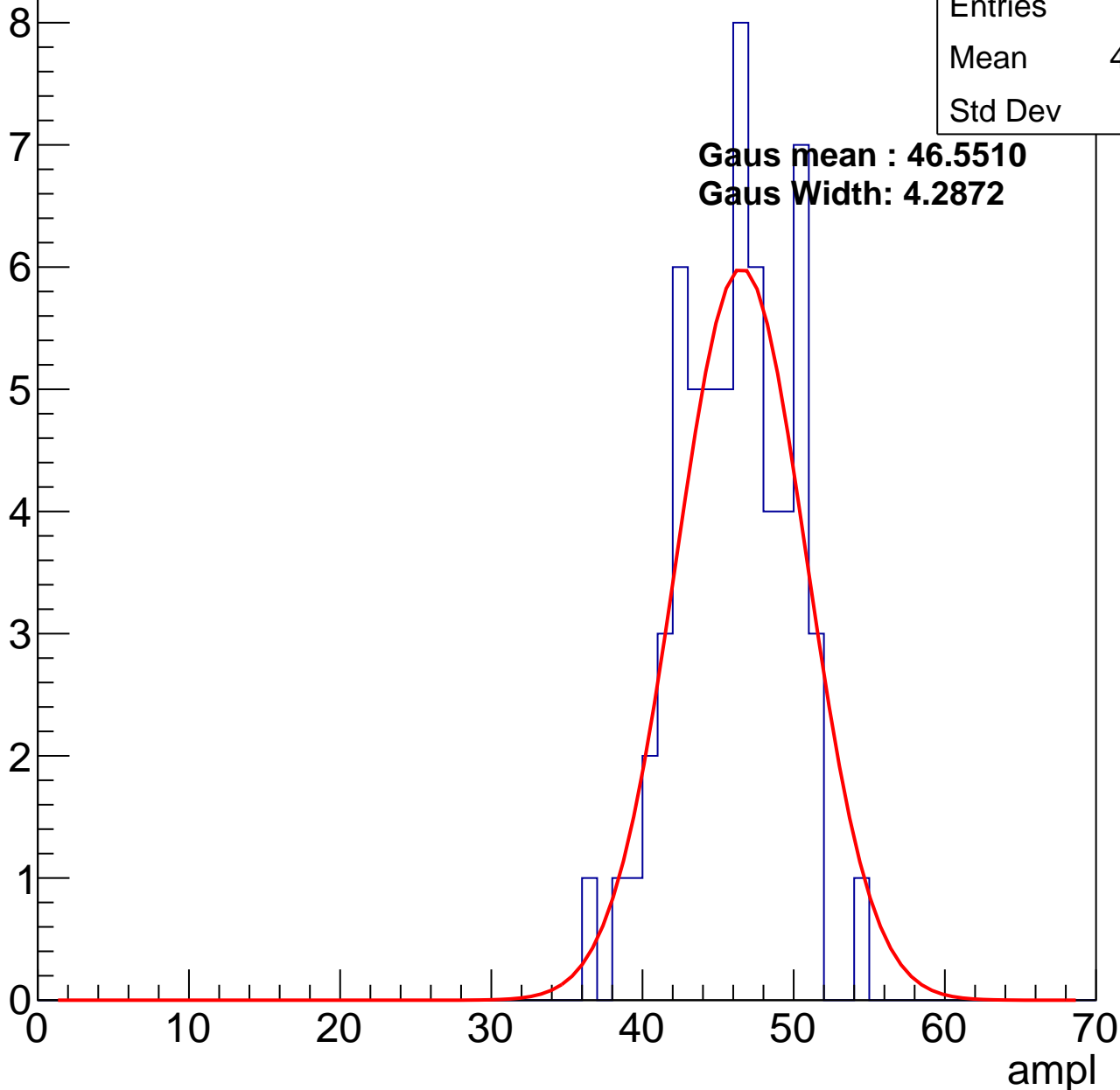
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	45.53
Std Dev	3.64

**Gaus mean : 46.5510**

**Gaus Width: 4.2872**

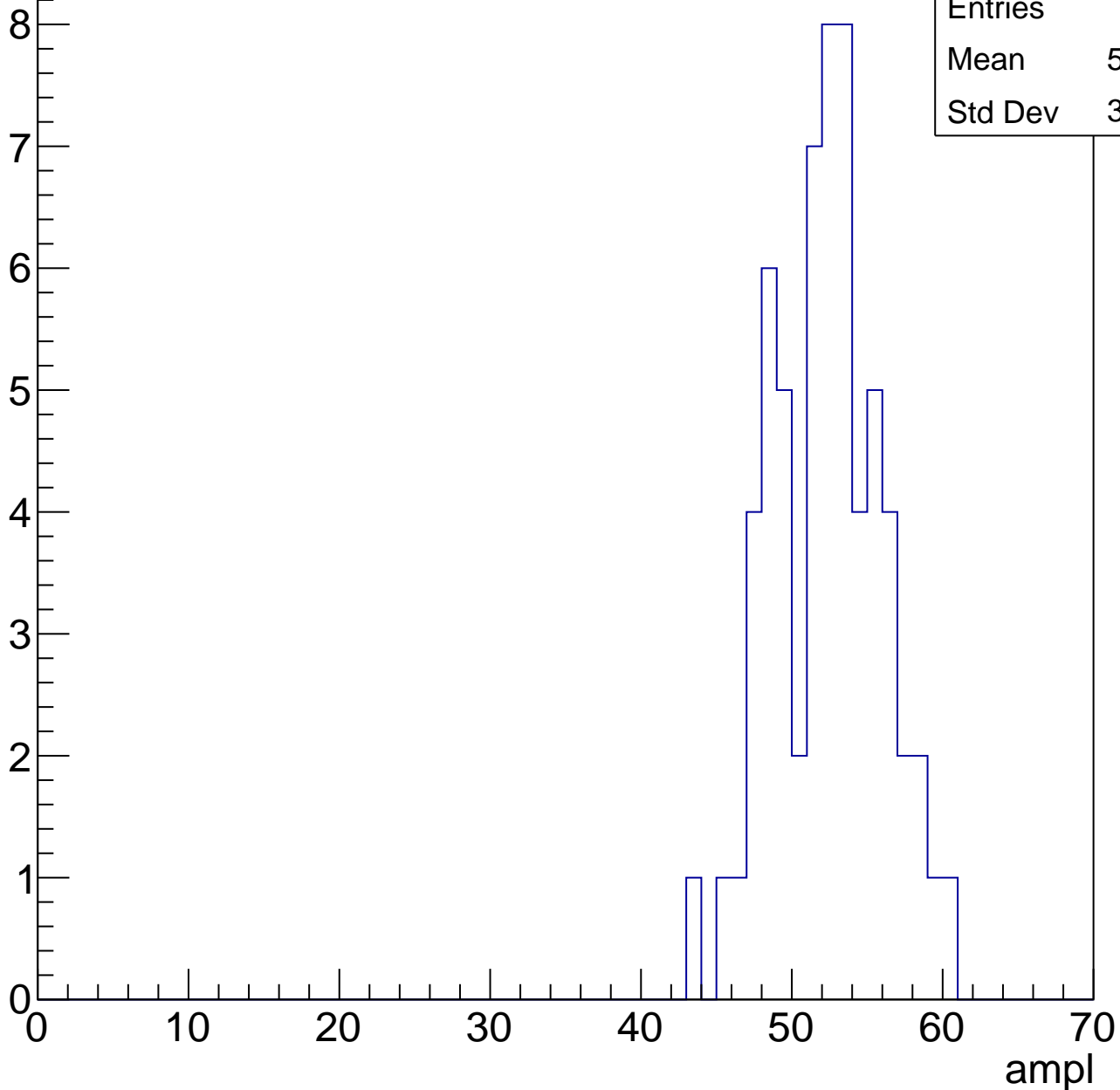


# B0L001S, U17-ch113, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	51.87
Std Dev	3.567

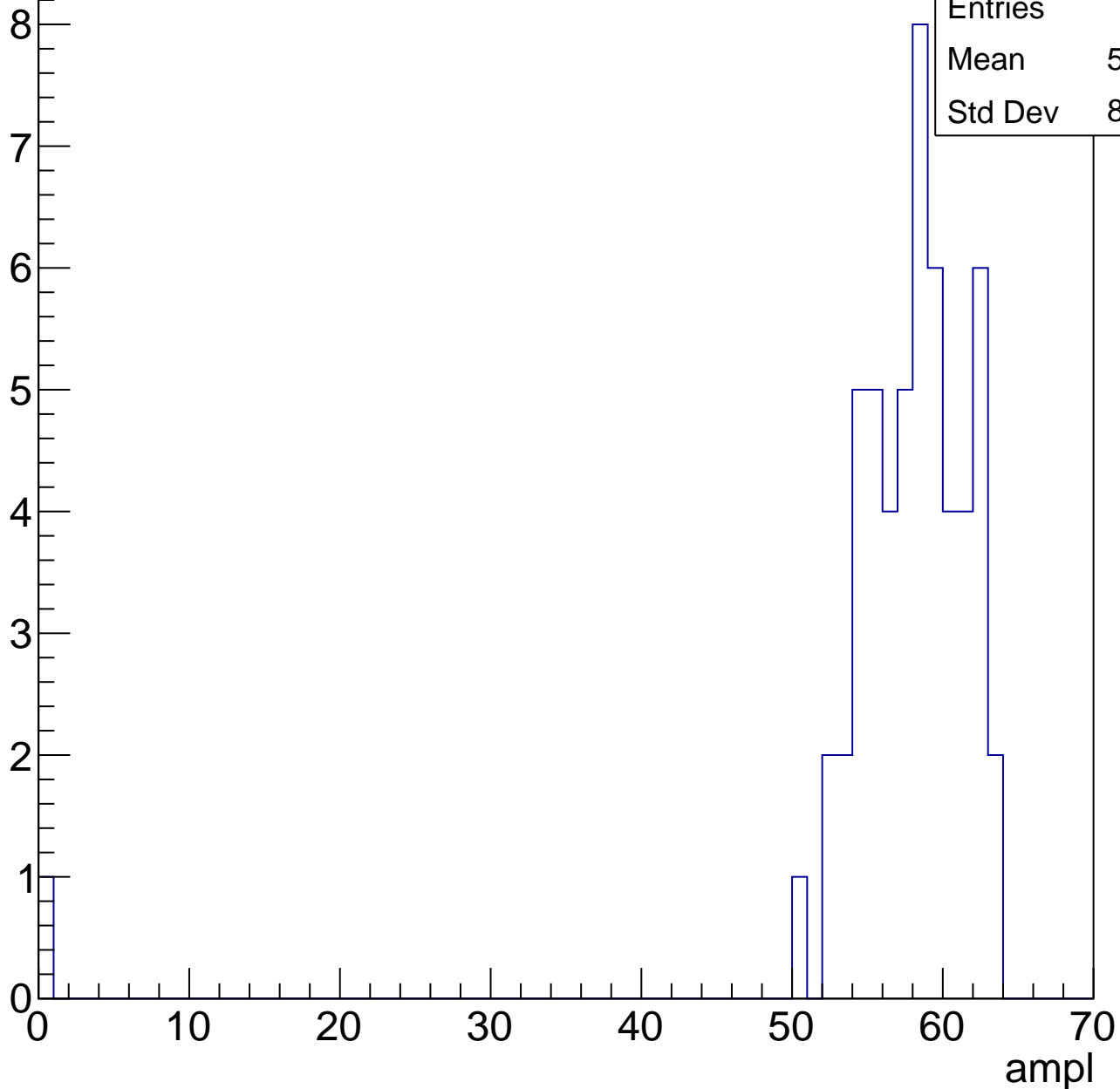


# B0L001S, U17-ch113, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	56.62
Std Dev	8.307

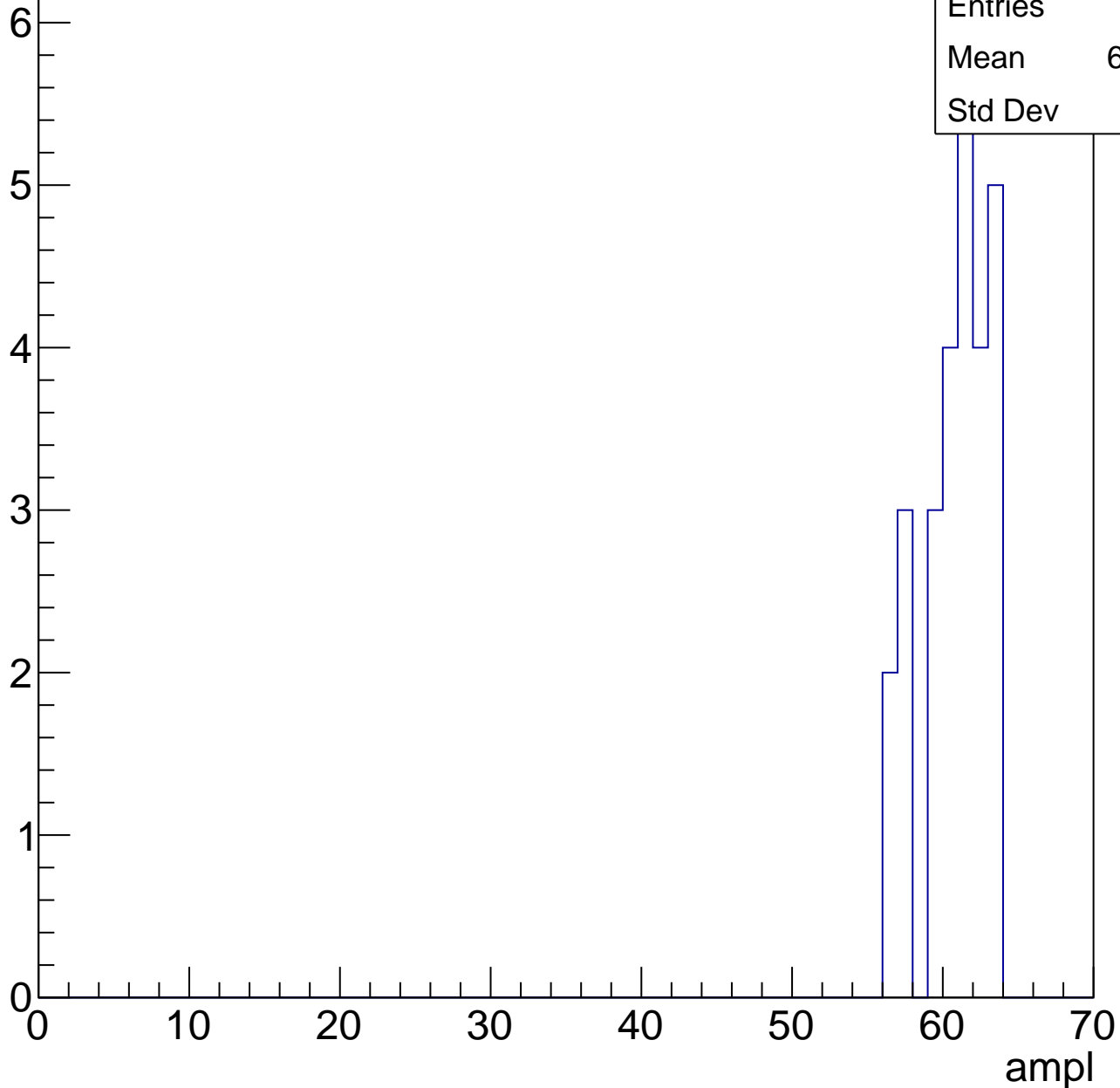


# B0L001S, U17-ch113, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	27
Mean	60.33
Std Dev	2.16



# B0L001S, U17-ch113, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch113, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

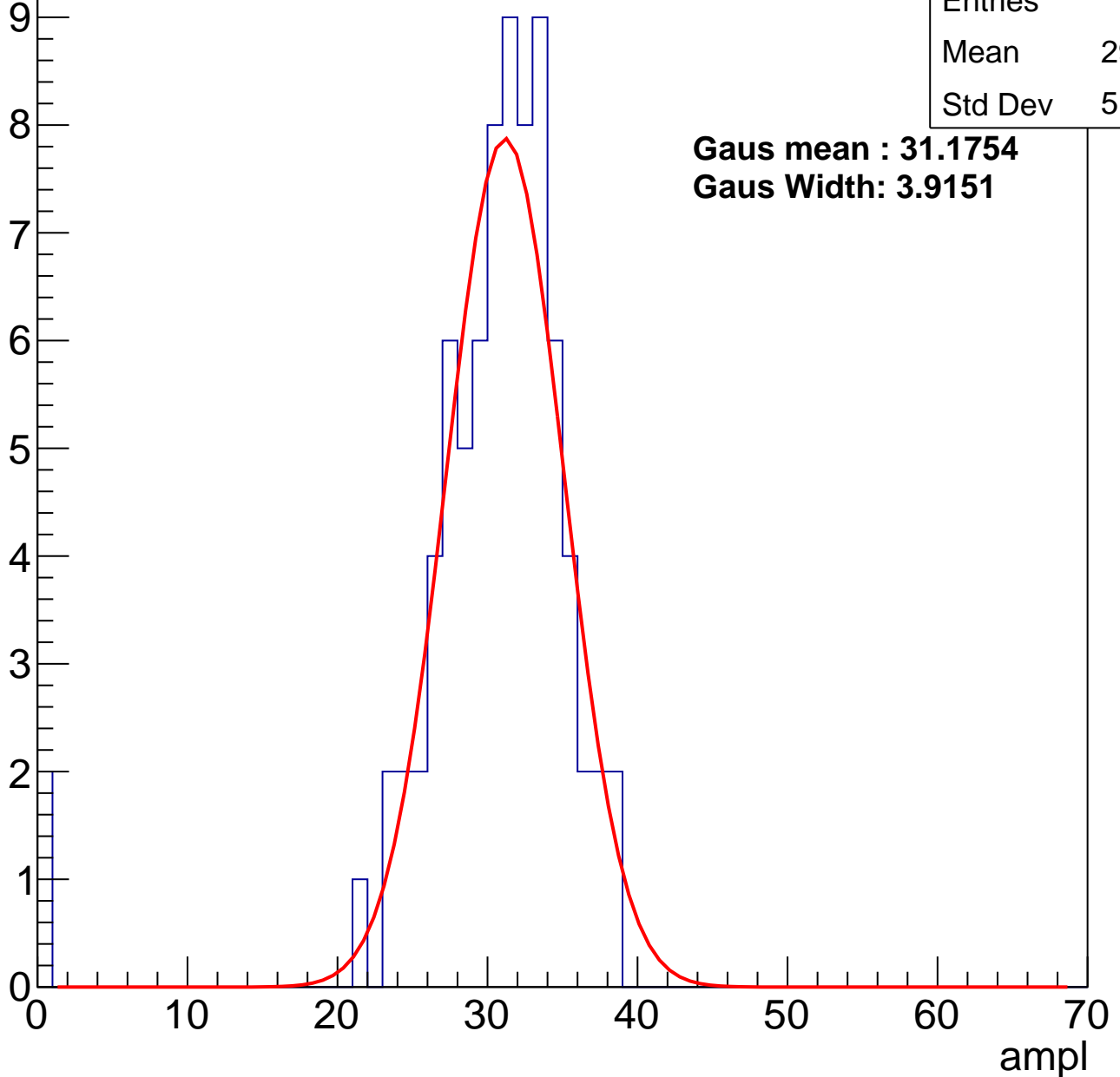
# B0L001S, U17-ch114, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	80
Mean	29.79
Std Dev	5.976

**Gaus mean : 31.1754**  
**Gaus Width: 3.9151**



# B0L001S, U17-ch114, adc1

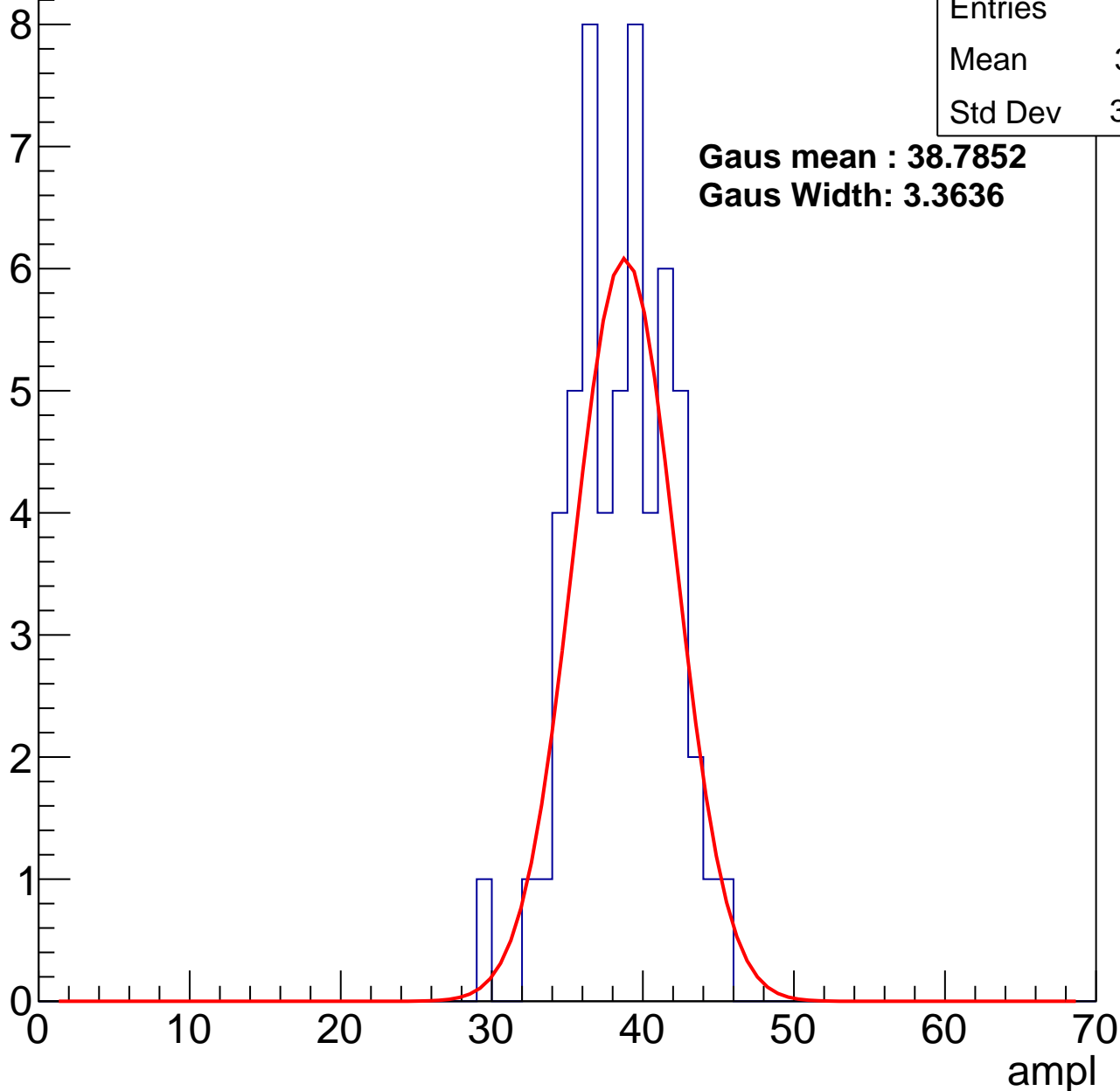
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	38.11
Std Dev	3.216

**Gaus mean : 38.7852**

**Gaus Width: 3.3636**



# B0L001S, U17-ch114, adc2

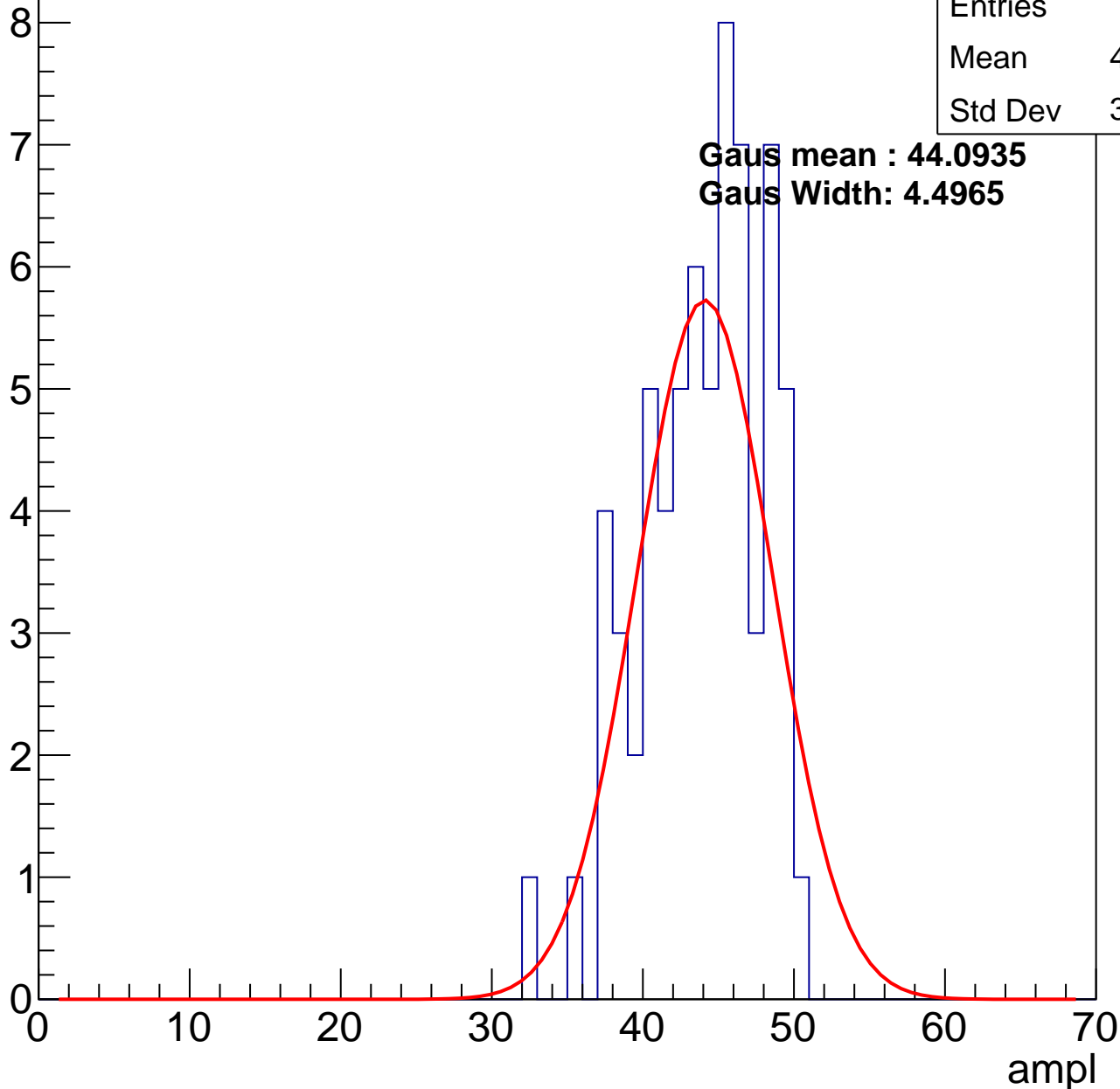
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	43.48
Std Dev	3.937

**Gaus mean : 44.0935**

**Gaus Width: 4.4965**

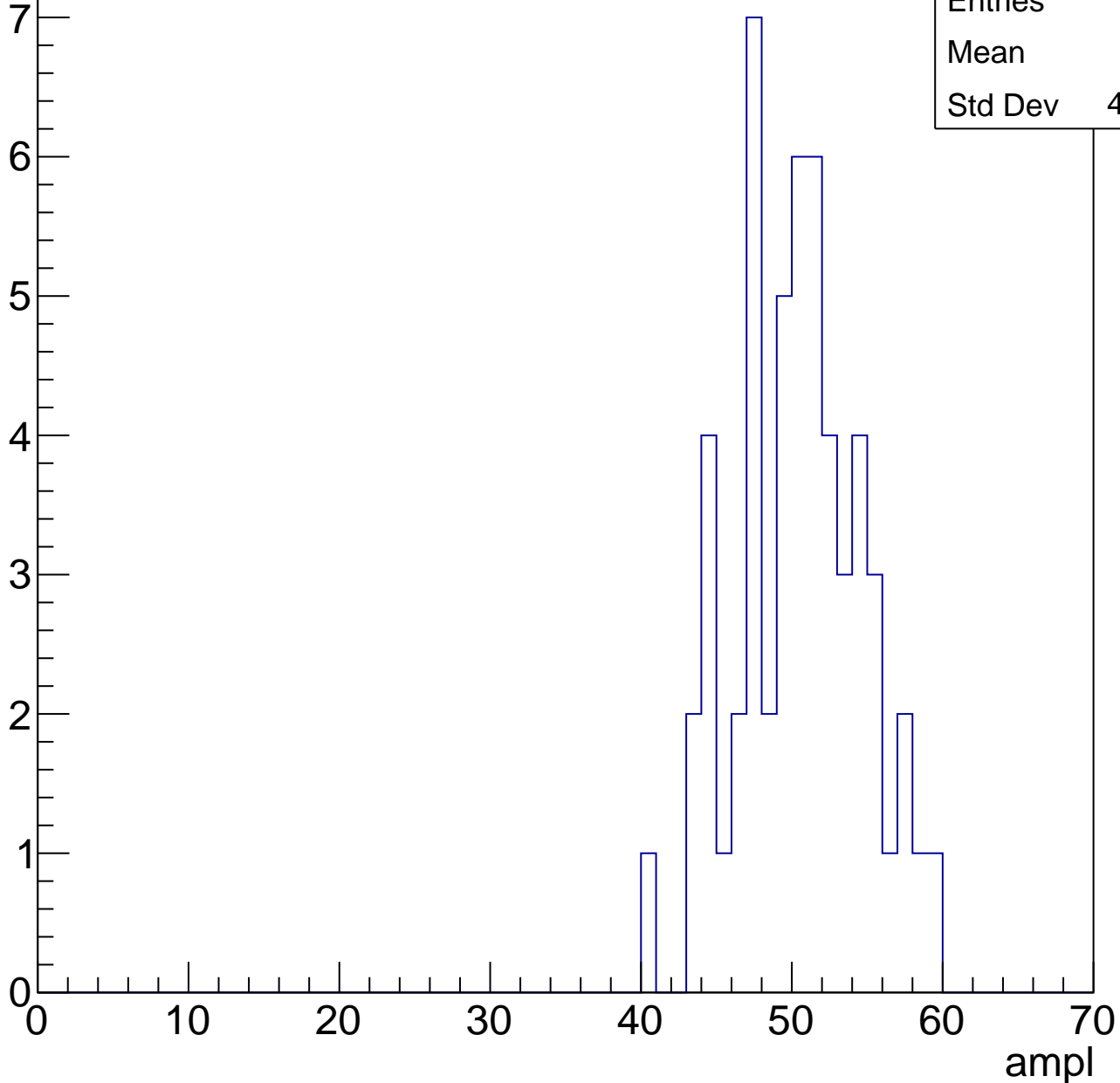


# B0L001S, U17-ch114, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	50
Std Dev	4.139

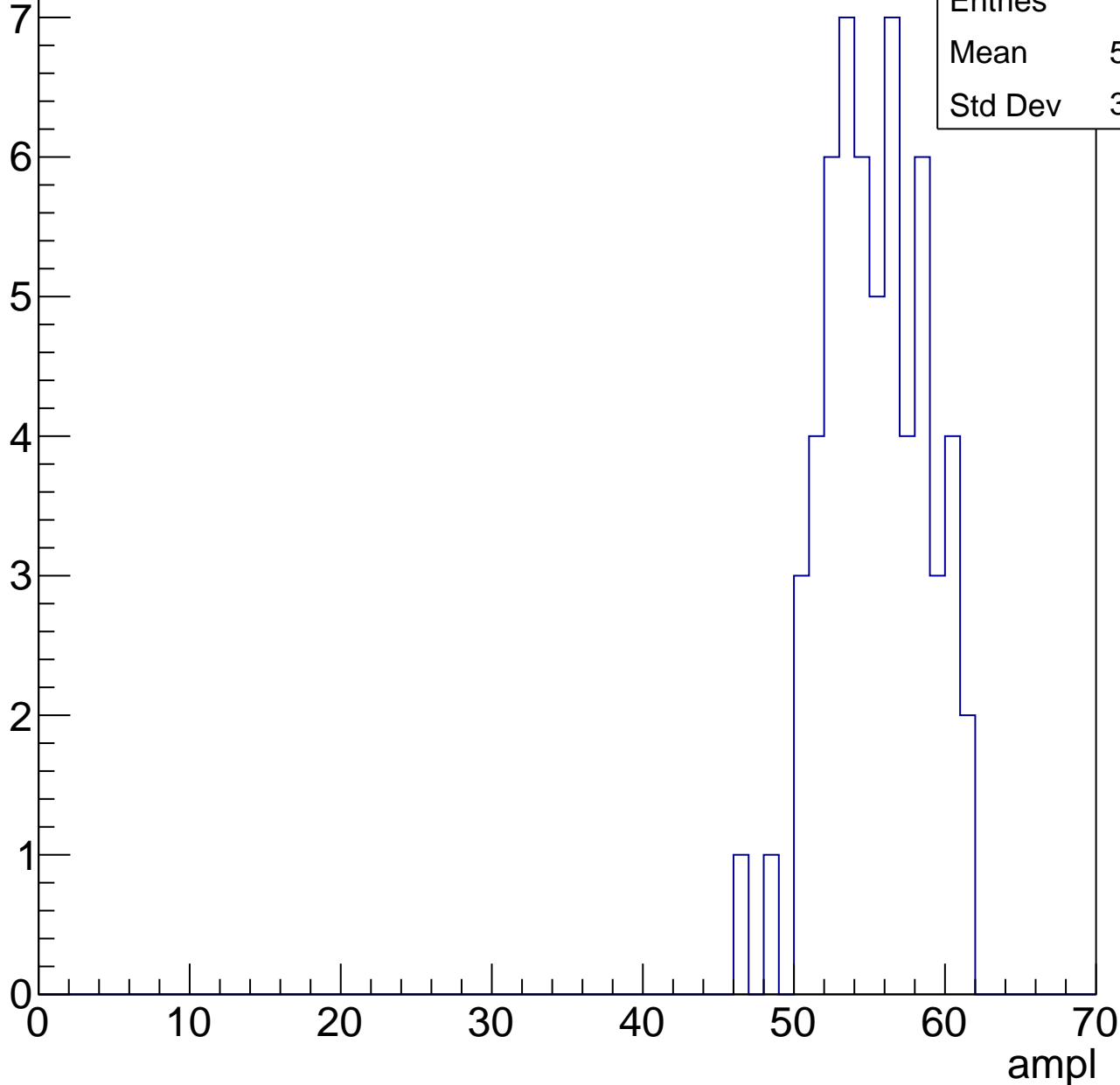


# B0L001S, U17-ch114, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	54.86
Std Dev	3.327

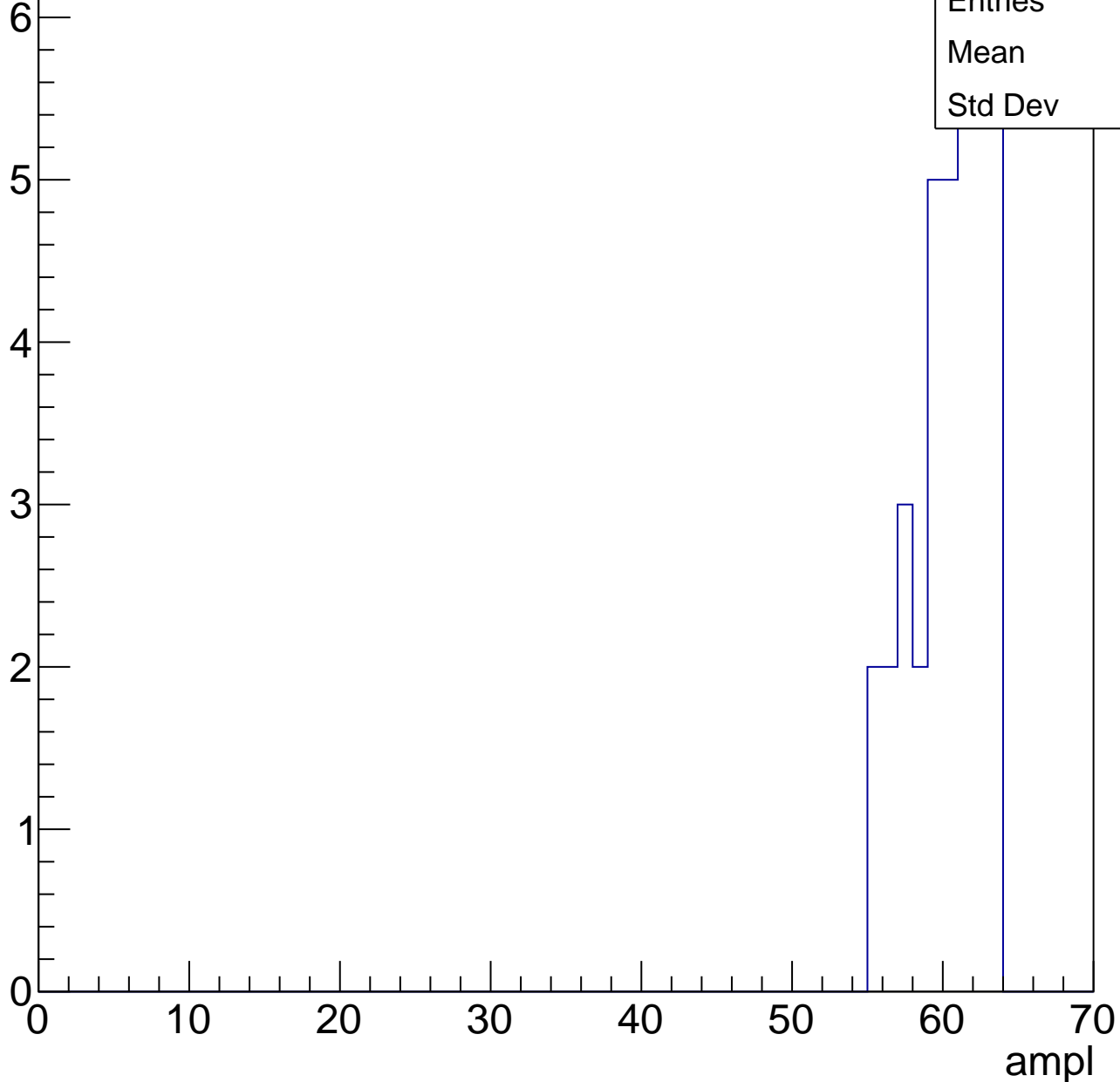


# B0L001S, U17-ch114, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

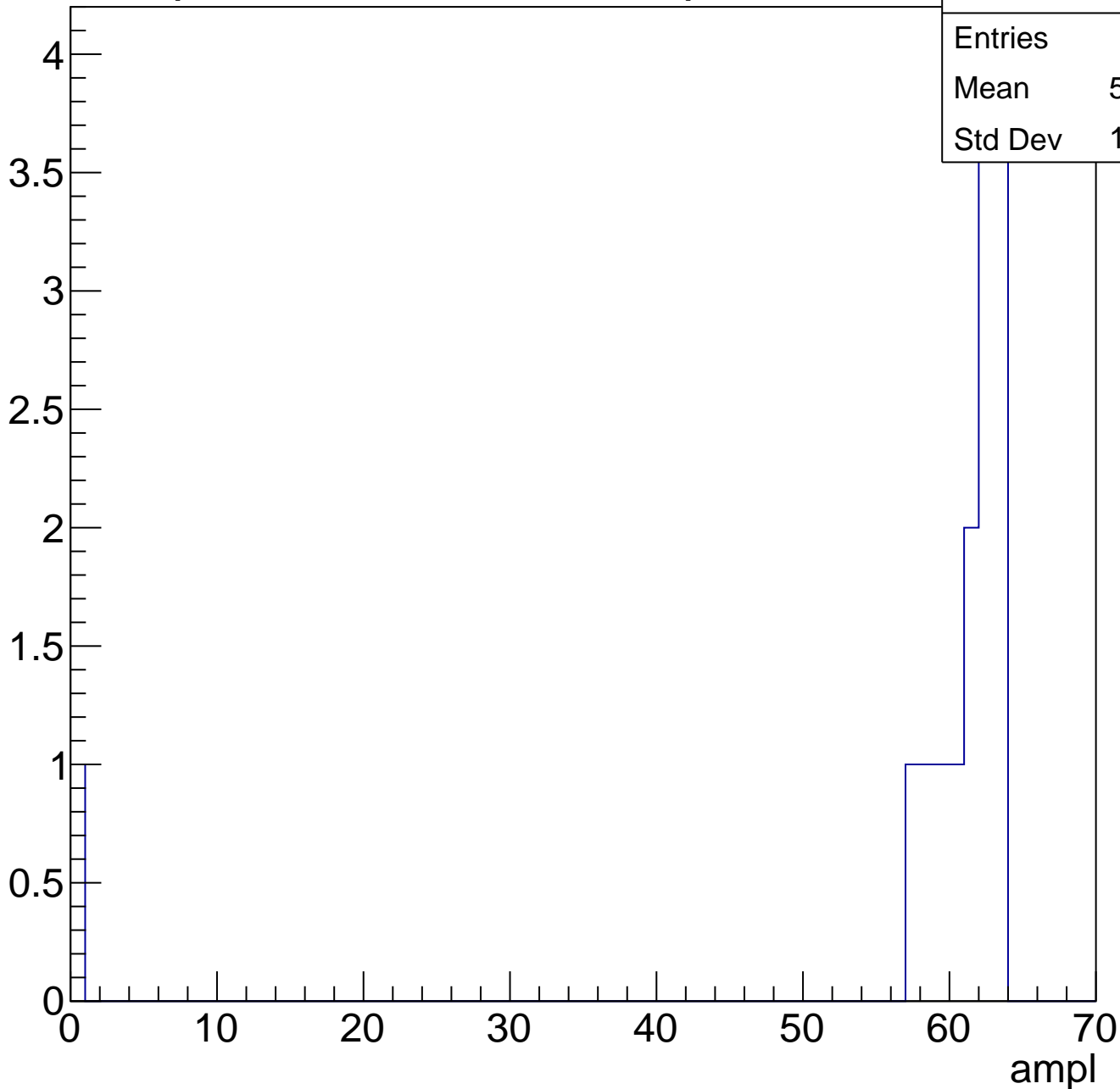
Entries	37
Mean	60
Std Dev	2.36



# B0L001S, U17-ch114, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch114, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L001S, U17-ch115, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	60
Mean	29.53
Std Dev	5.182

**Gaus mean : 30.3016**

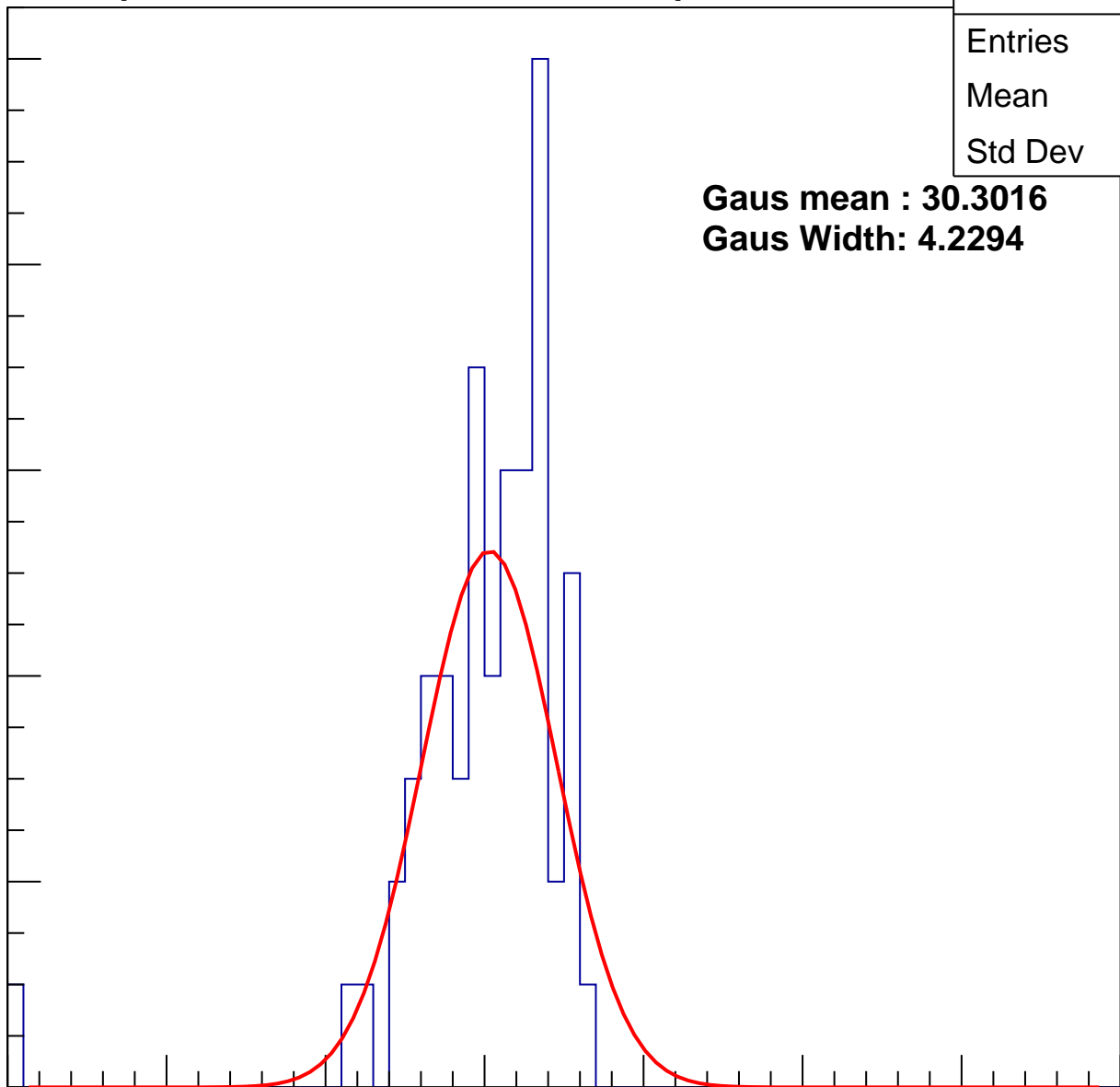
**Gaus Width: 4.2294**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U17-ch115, adc1

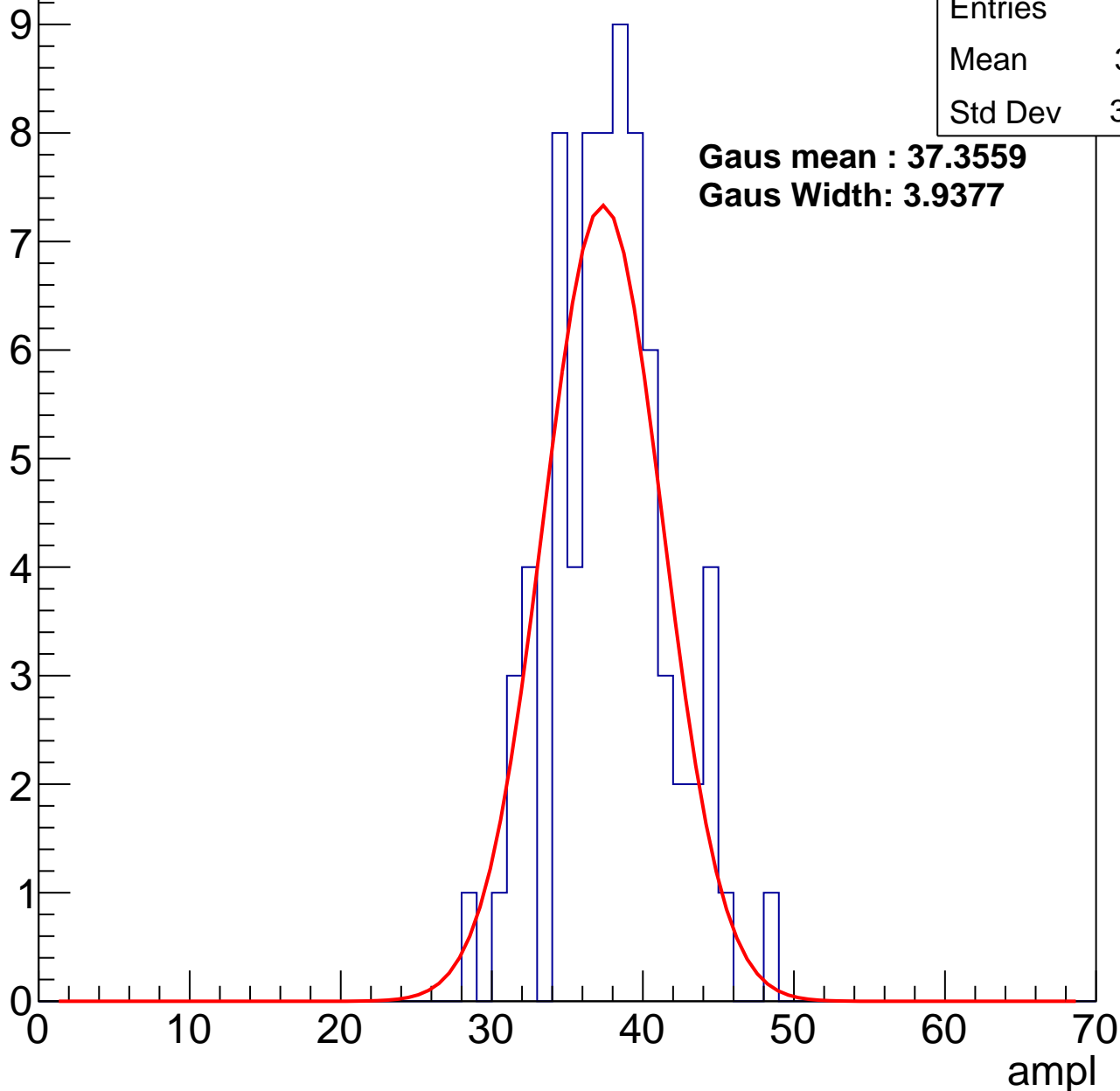
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	37.41
Std Dev	3.824

**Gaus mean : 37.3559**

**Gaus Width: 3.9377**



# B0L001S, U17-ch115, adc2

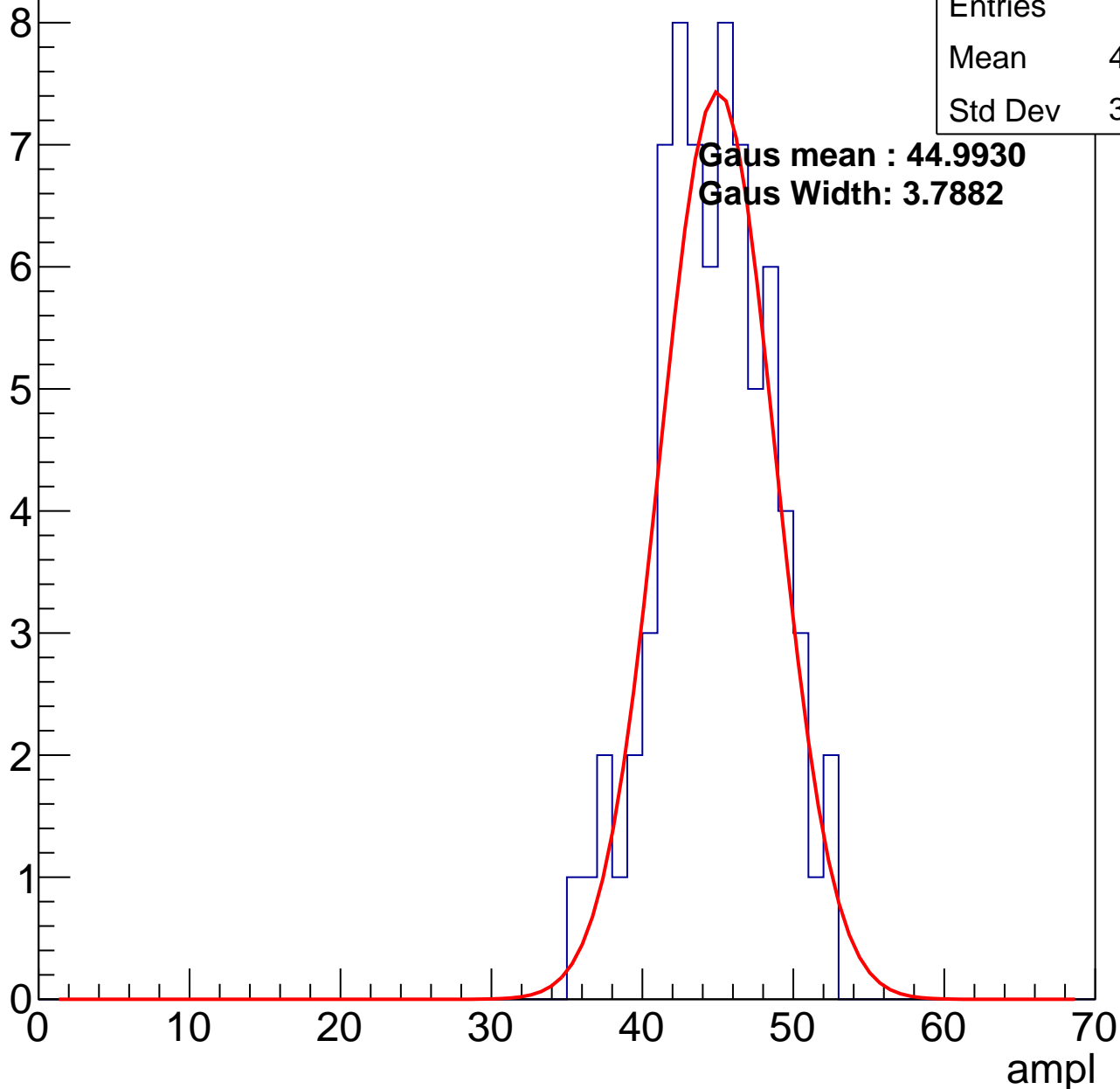
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	44.26
Std Dev	3.742

**Gaus mean : 44.9930**

**Gaus Width: 3.7882**

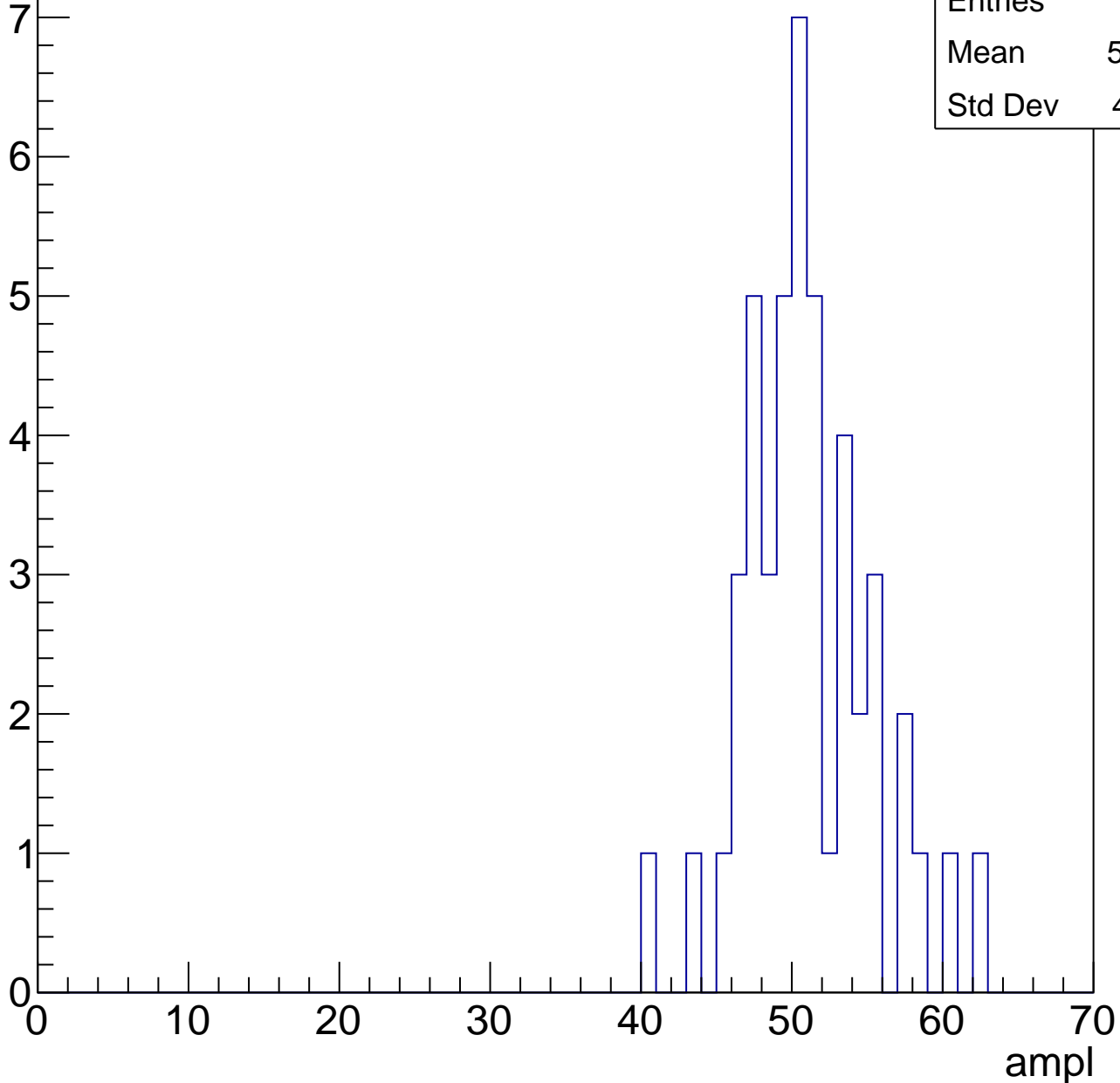


# B0L001S, U17-ch115, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	46
Mean	50.57
Std Dev	4.241

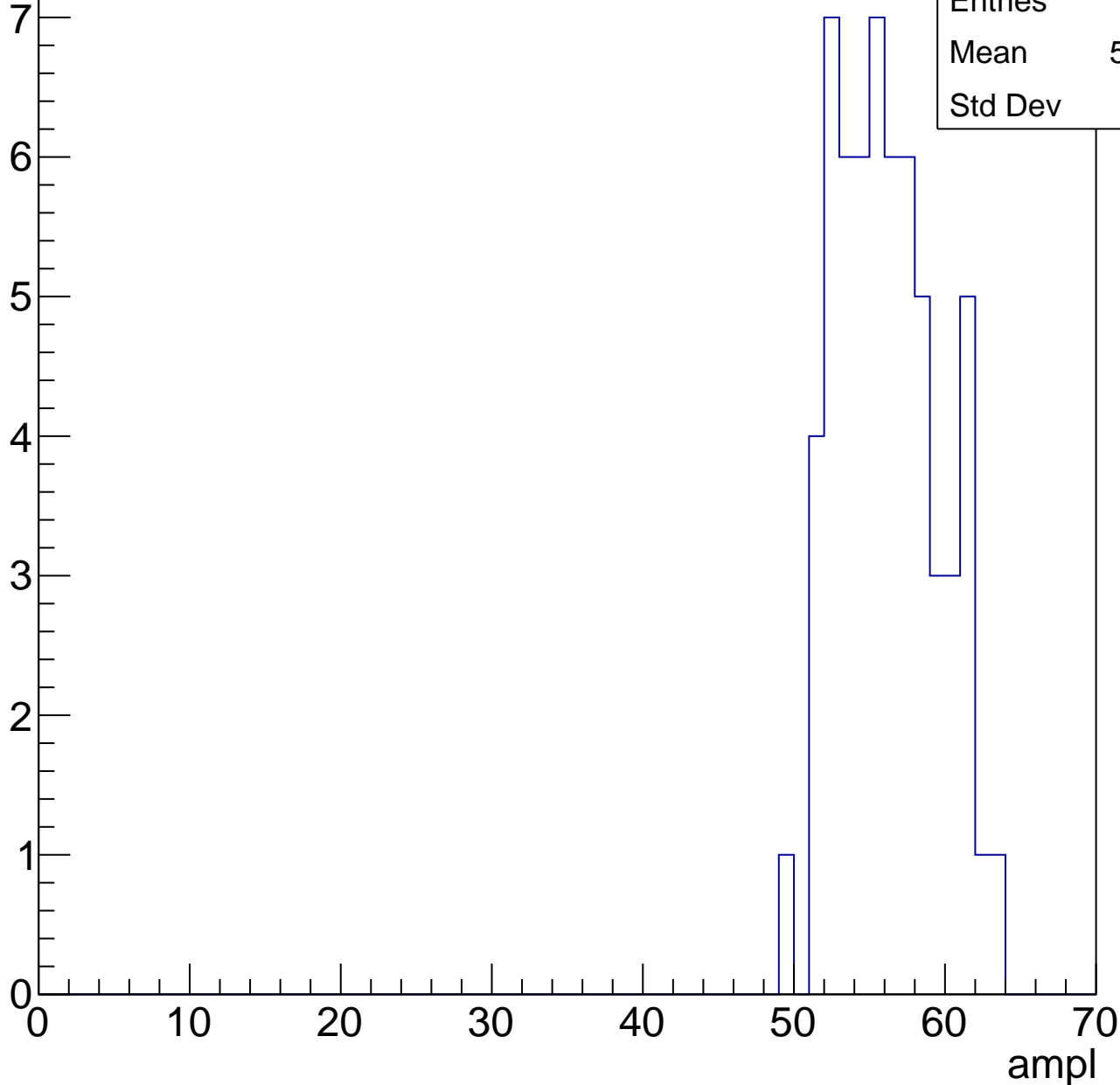


# B0L001S, U17-ch115, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	55.72
Std Dev	3.27

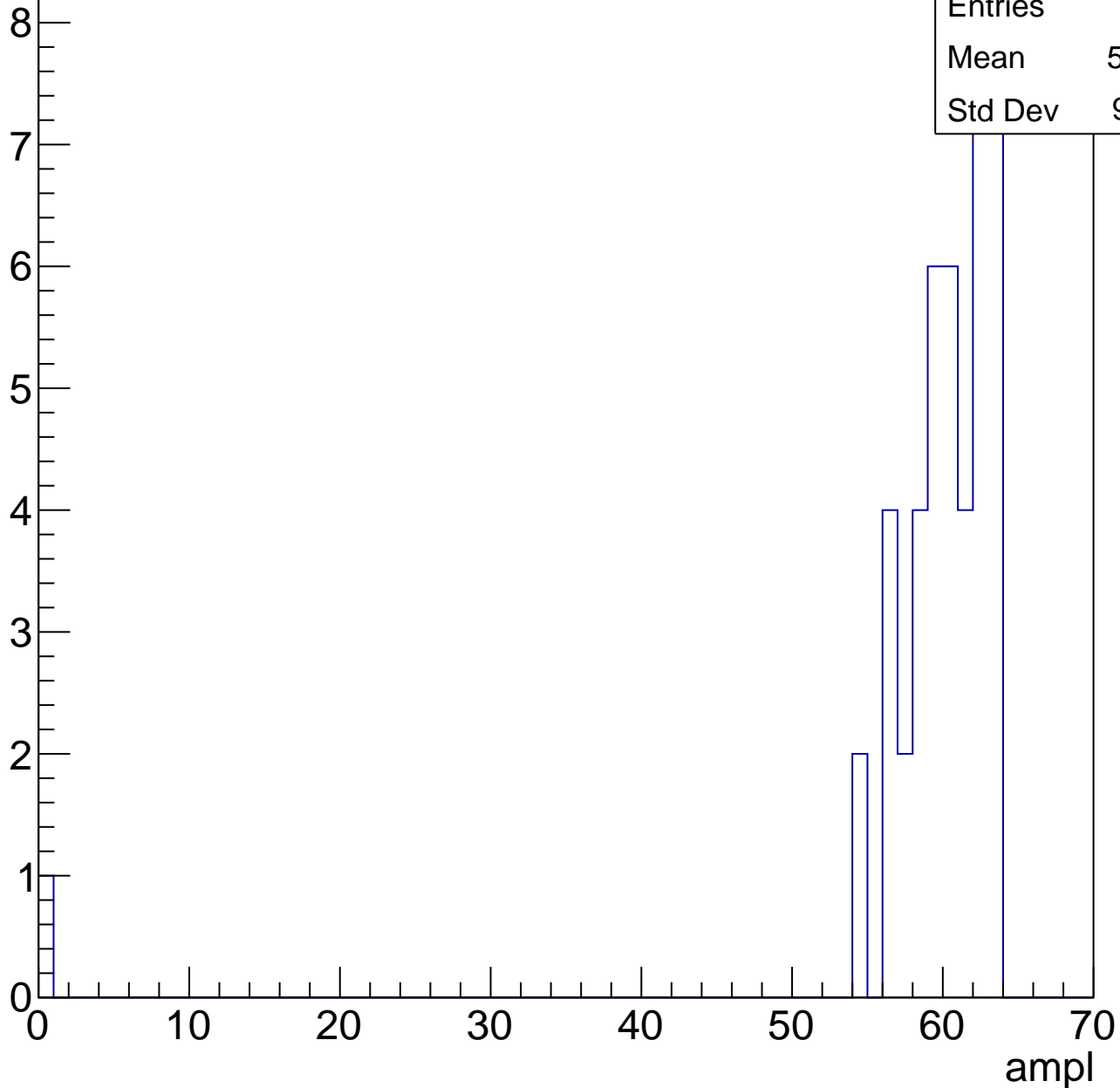


# B0L001S, U17-ch115, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	45
Mean	58.58
Std Dev	9.181



# B0L001S, U17-ch115, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

ampl

Entries	3
Mean	61
Std Dev	1.633



# B0L001S, U17-ch115, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U17-ch116, adc0

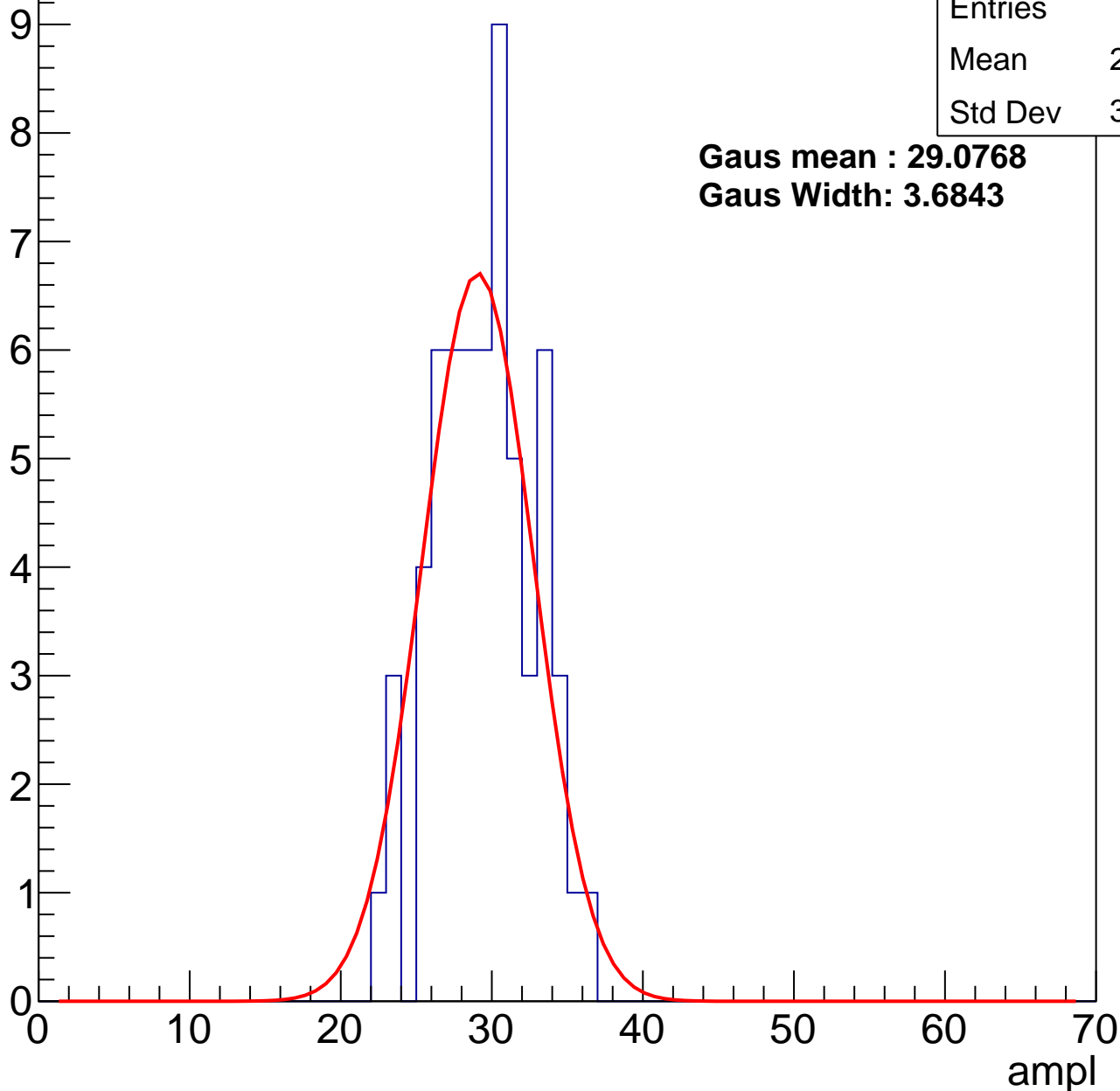
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	29.05
Std Dev	3.206

**Gaus mean : 29.0768**

**Gaus Width: 3.6843**



# B0L001S, U17-ch116, adc1

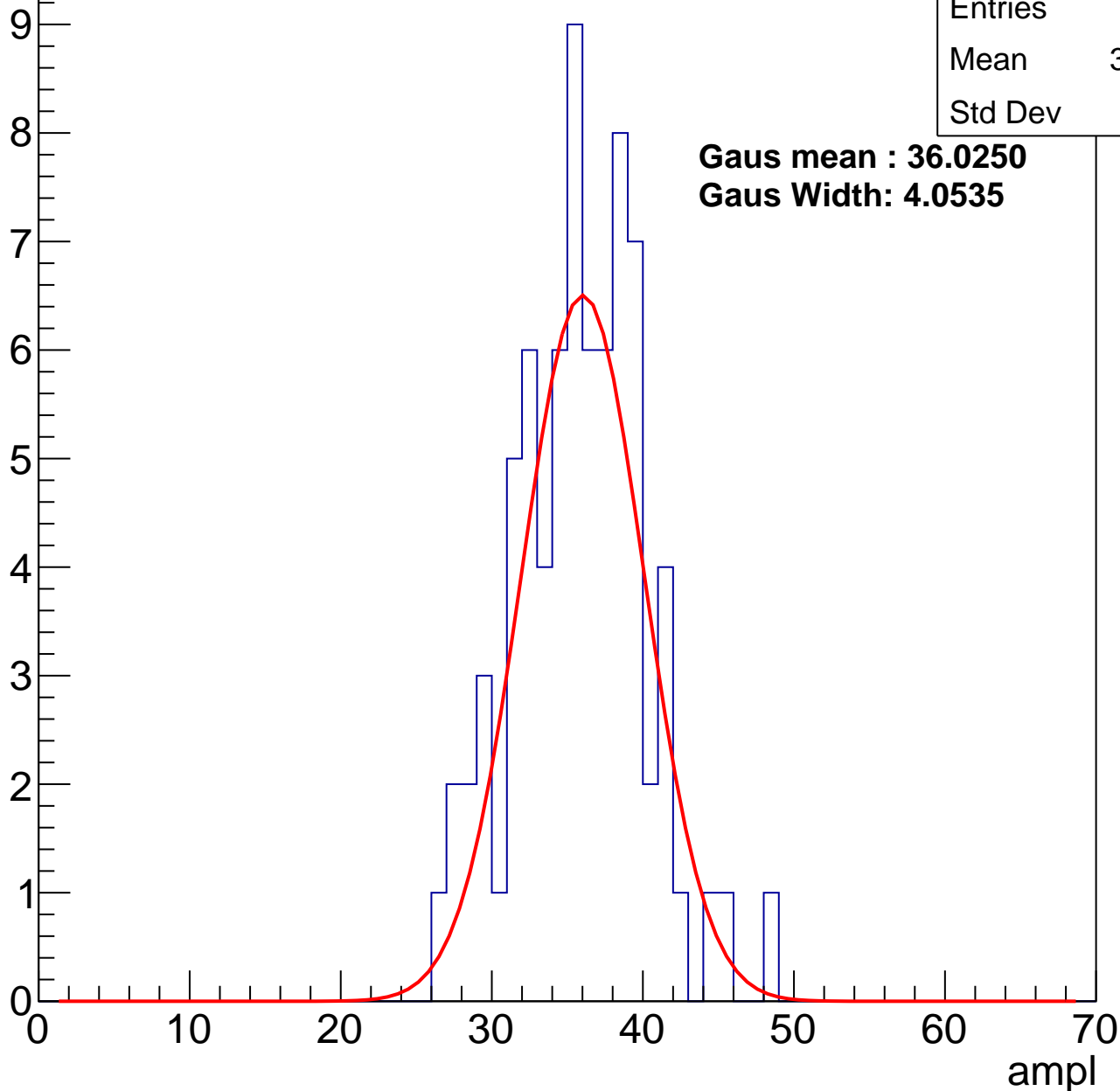
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	76
Mean	35.38
Std Dev	4.28

**Gaus mean : 36.0250**

**Gaus Width: 4.0535**



# B0L001S, U17-ch116, adc2

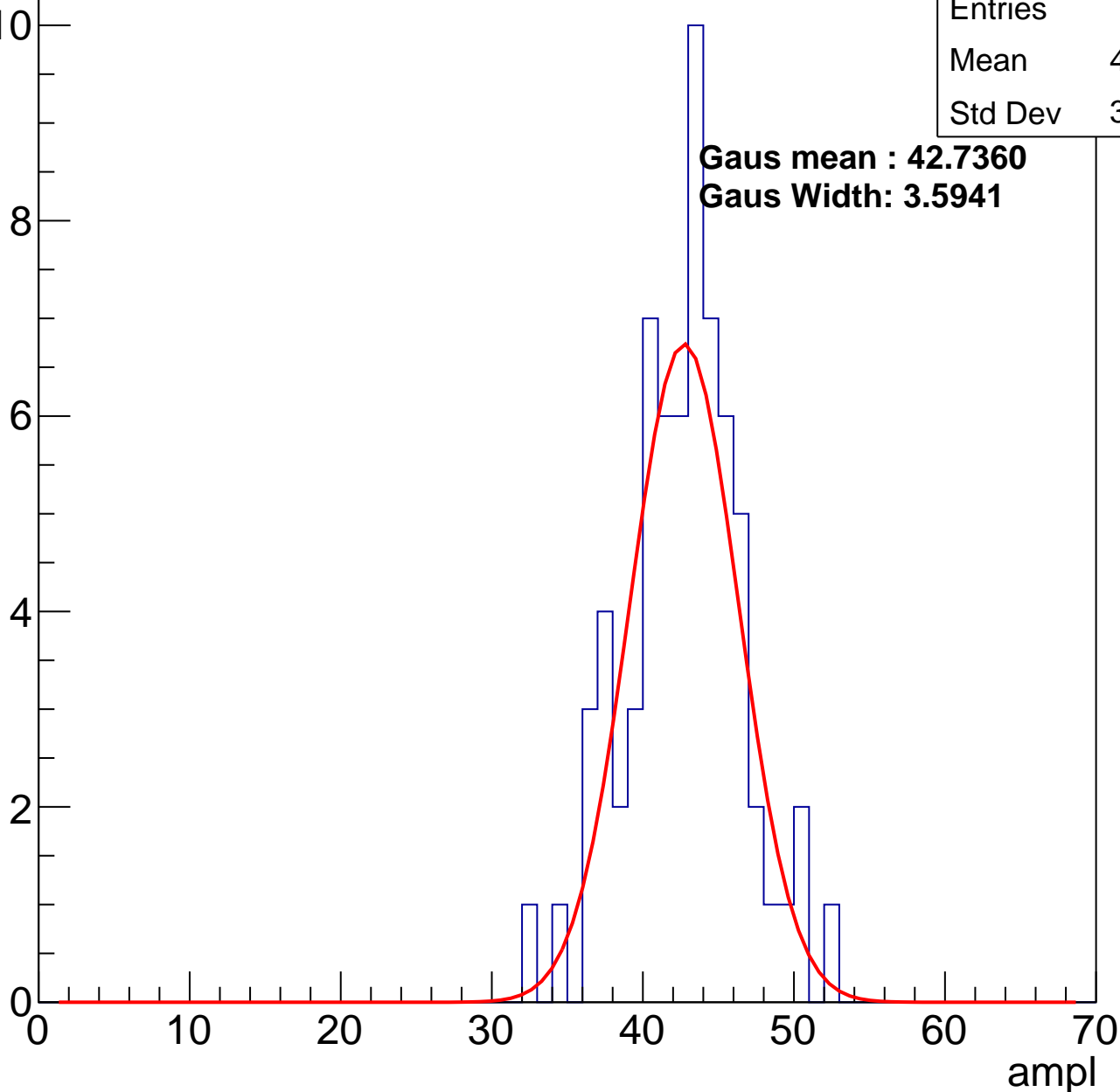
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	42.26
Std Dev	3.826

**Gaus mean : 42.7360**

**Gaus Width: 3.5941**

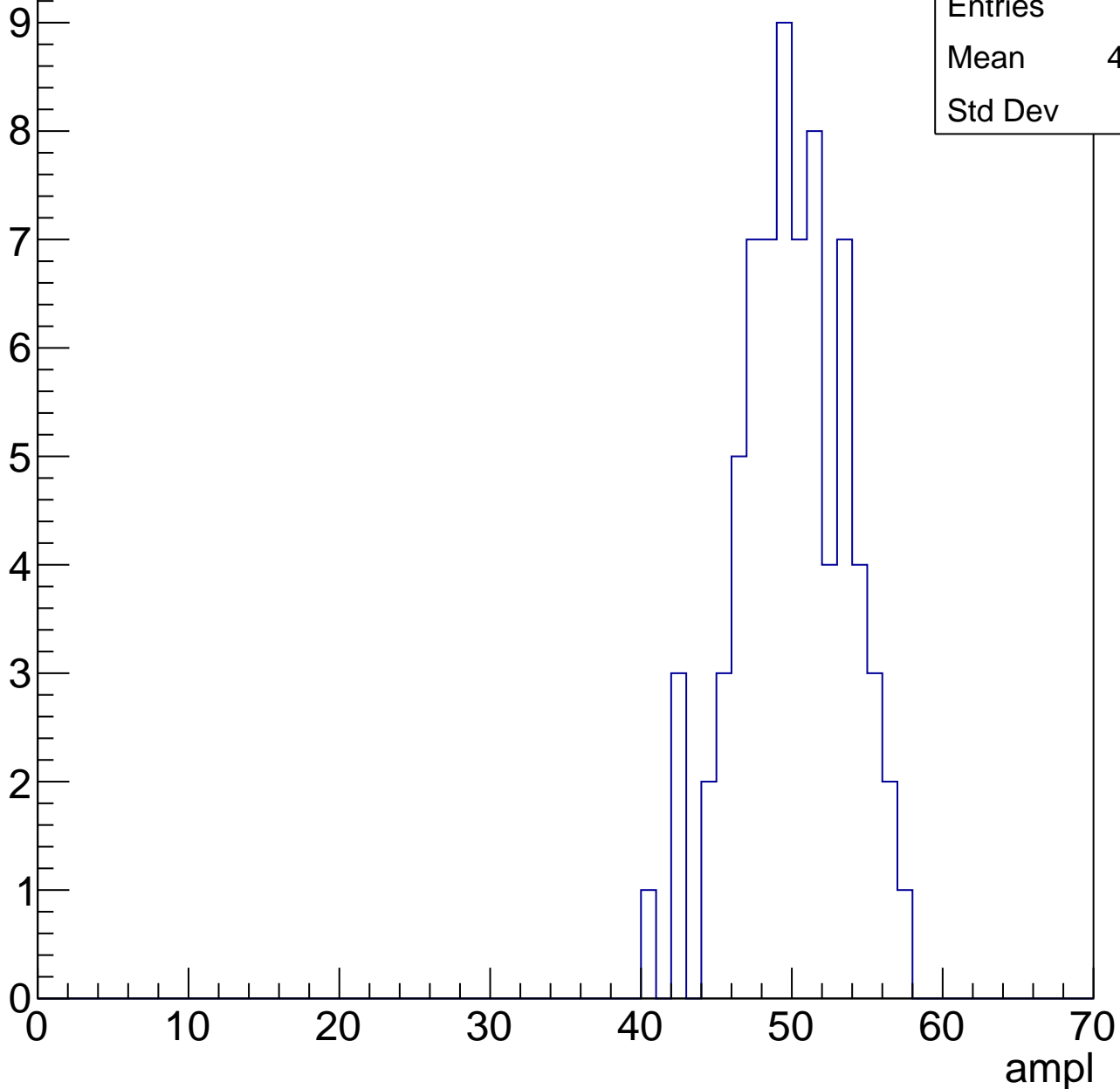


# B0L001S, U17-ch116, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	49.48
Std Dev	3.6

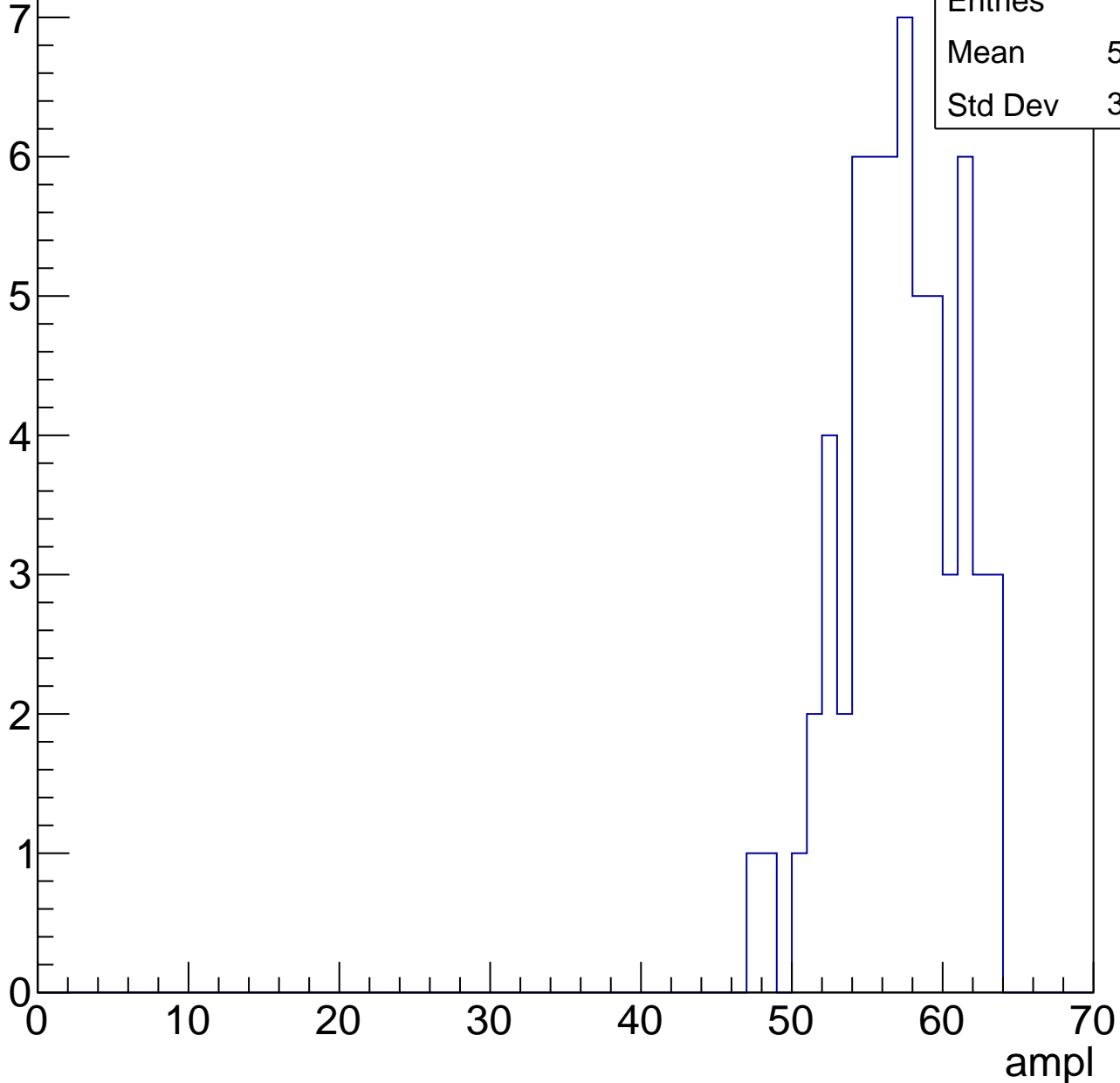


# B0L001S, U17-ch116, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

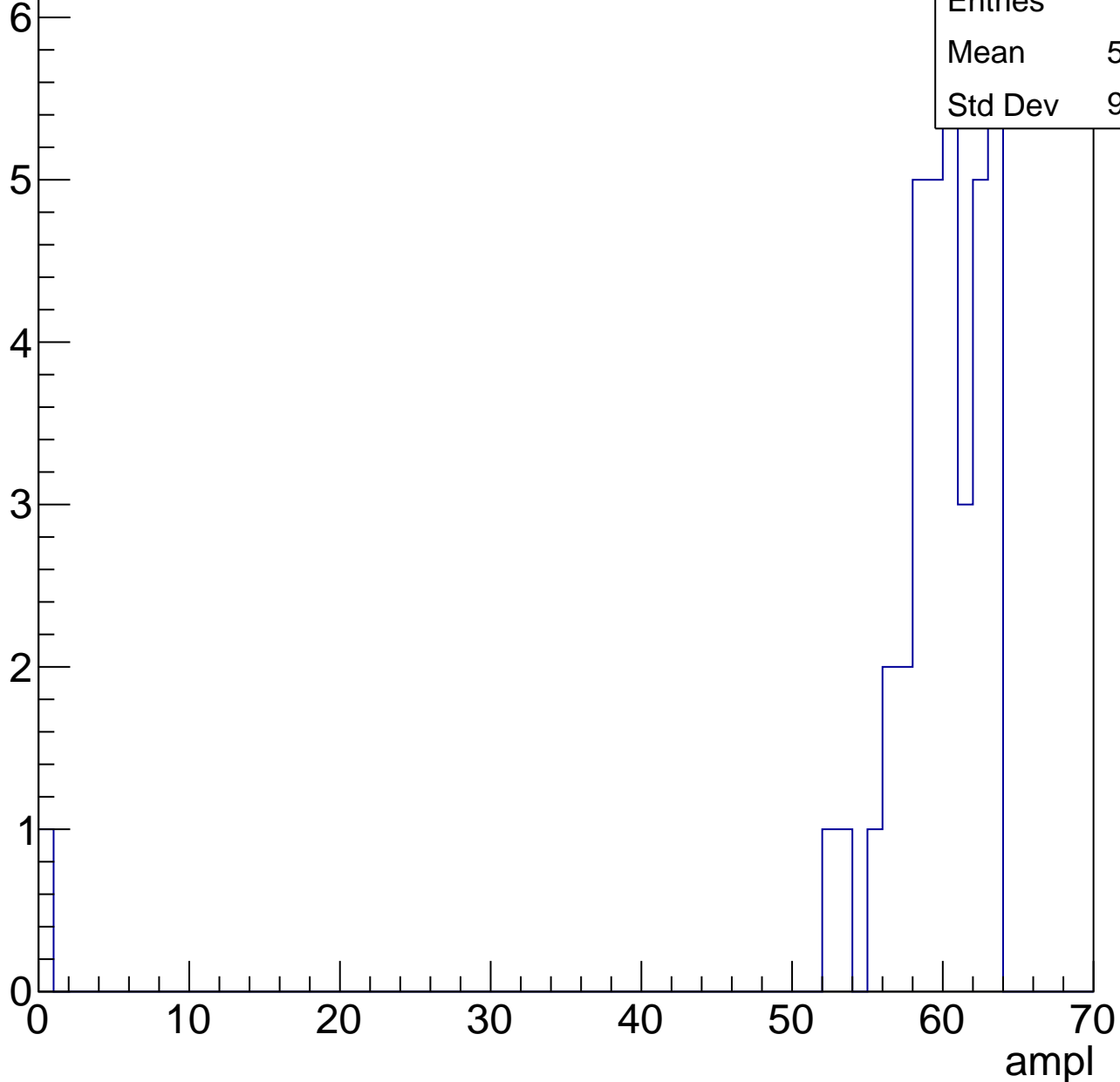
Entries	61
Mean	56.66
Std Dev	3.715



# B0L001S, U17-ch116, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U17-ch116, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	5
Mean	61.6
Std Dev	1.02



# B0L001S, U17-ch116, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

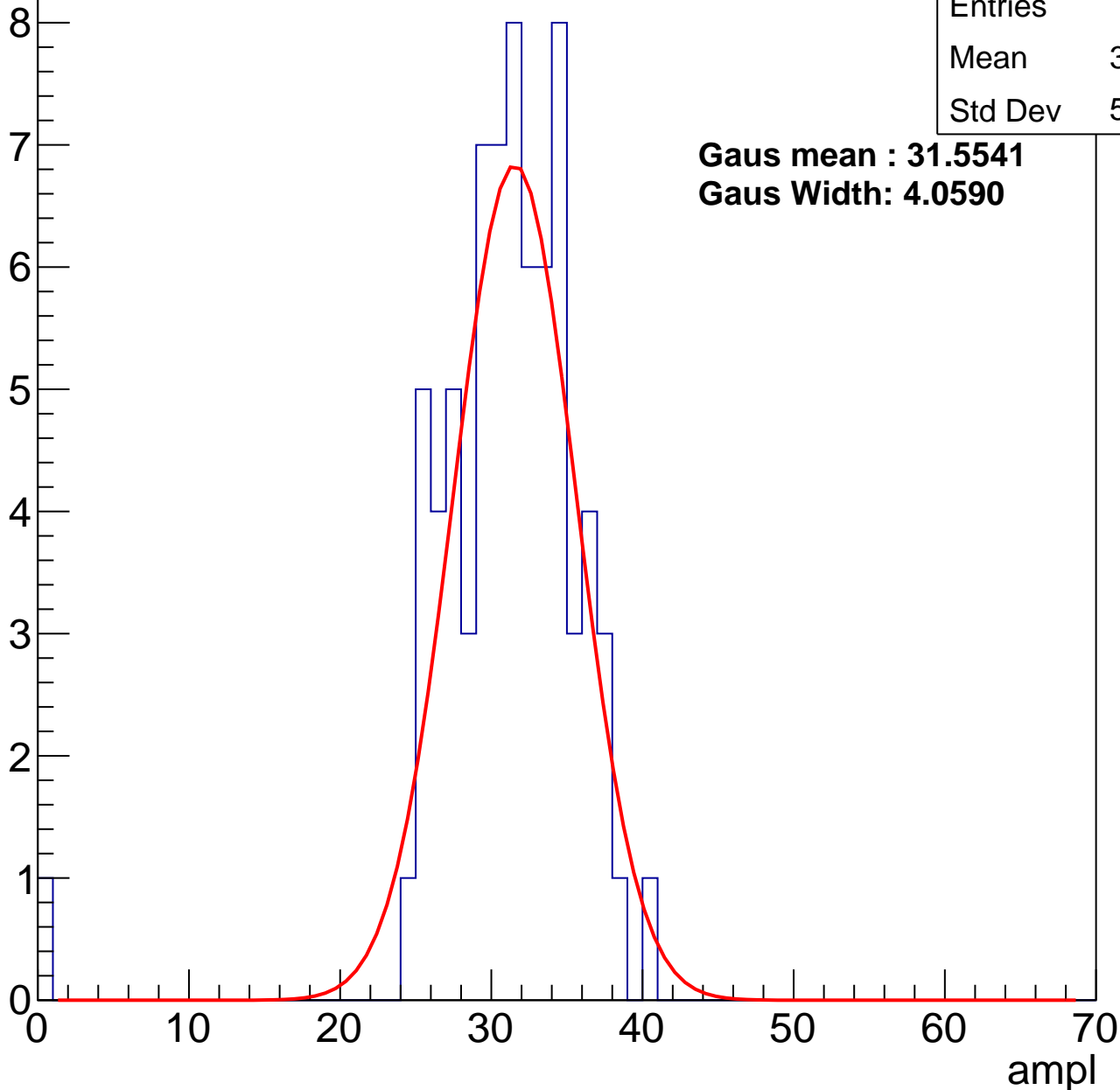
# B0L001S, U17-ch117, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	30.59
Std Dev	5.112

**Gaus mean : 31.5541**  
**Gaus Width: 4.0590**



# B0L001S, U17-ch117, adc1

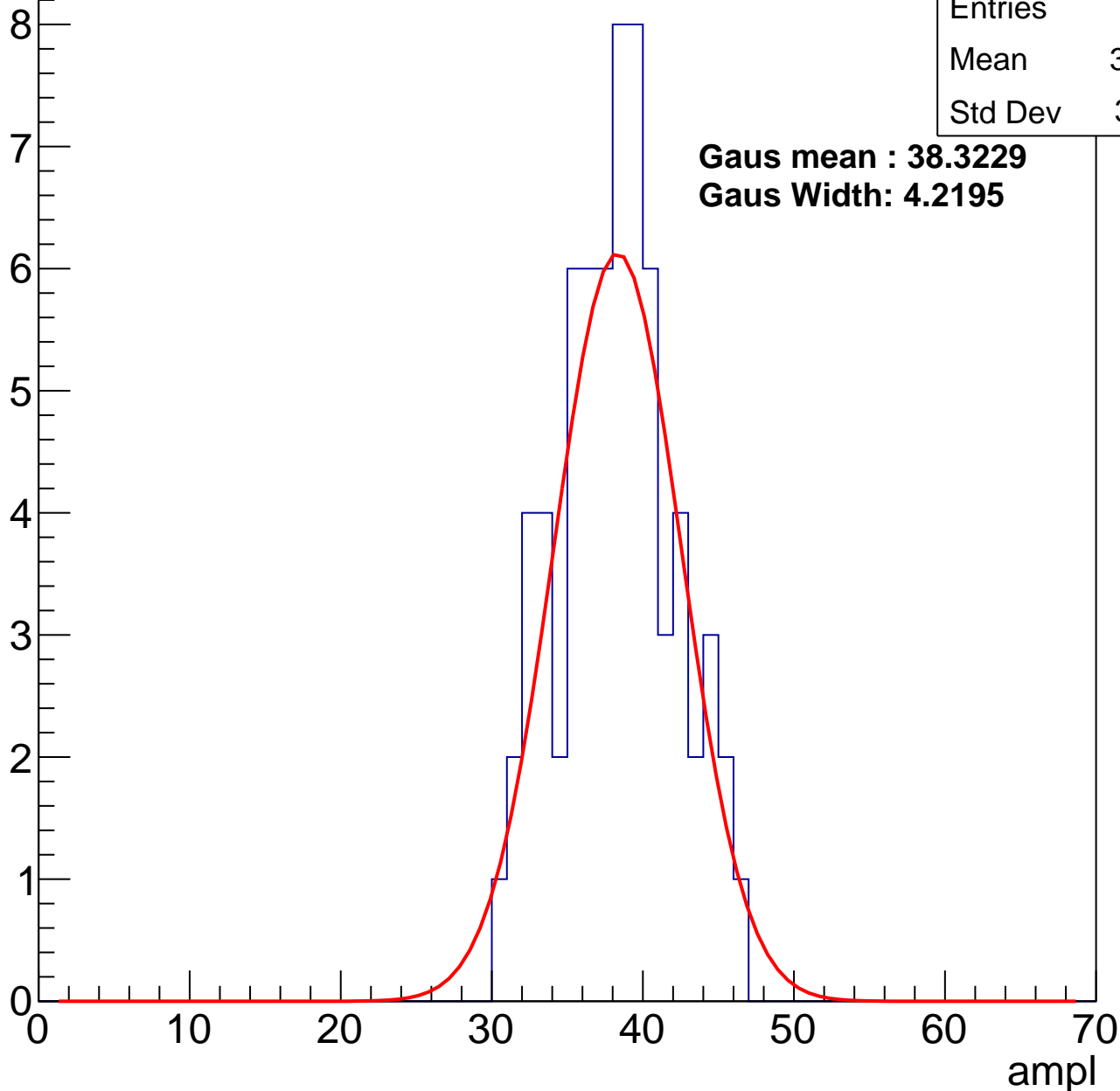
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	37.78
Std Dev	3.761

**Gaus mean : 38.3229**

**Gaus Width: 4.2195**



# B0L001S, U17-ch117, adc2

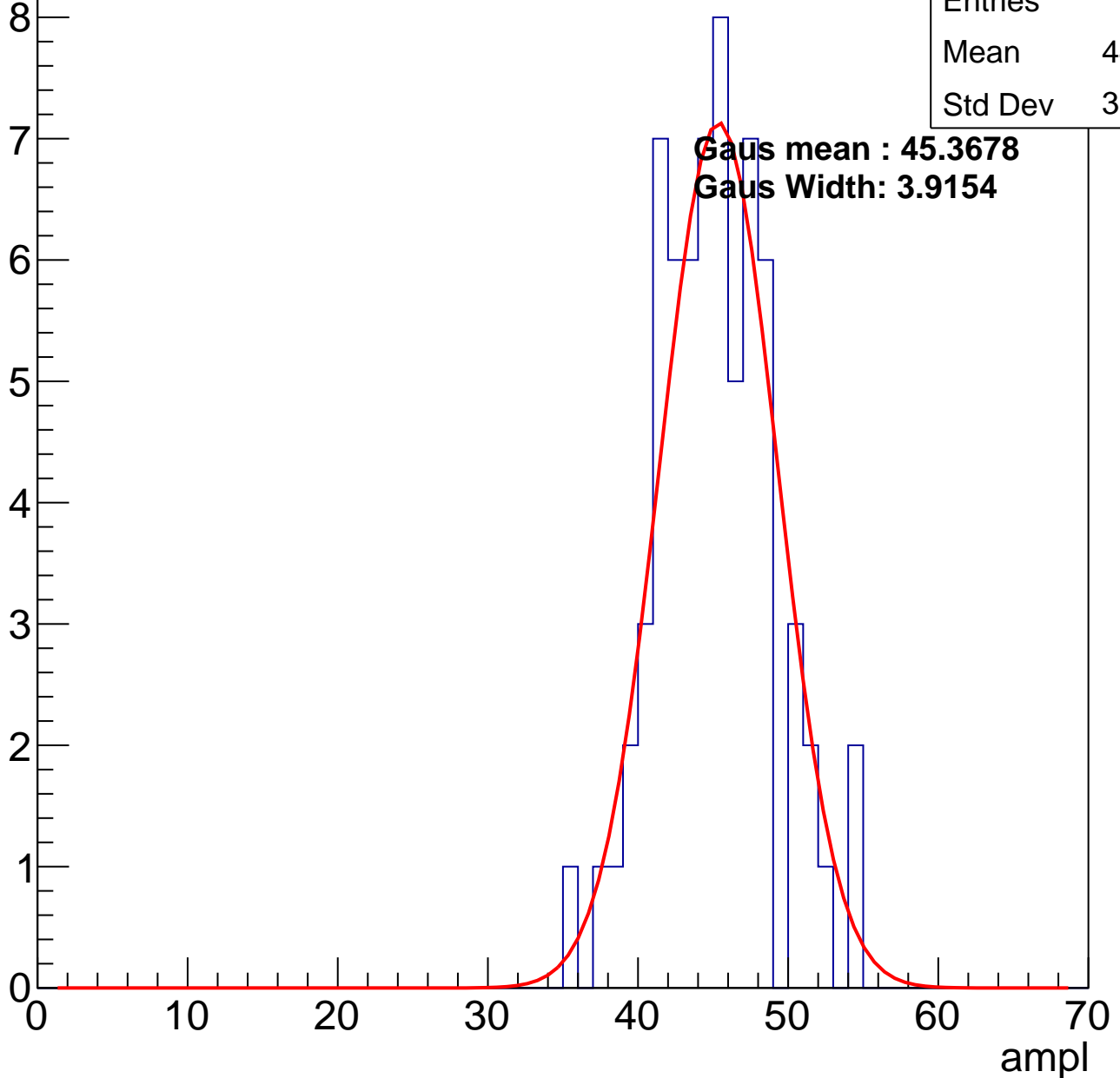
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	44.59
Std Dev	3.817

**Gaus mean : 45.3678**

**Gaus Width: 3.9154**



# B0L001S, U17-ch117, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	73
Mean	51.67
Std Dev	3.724

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

2

4

6

8

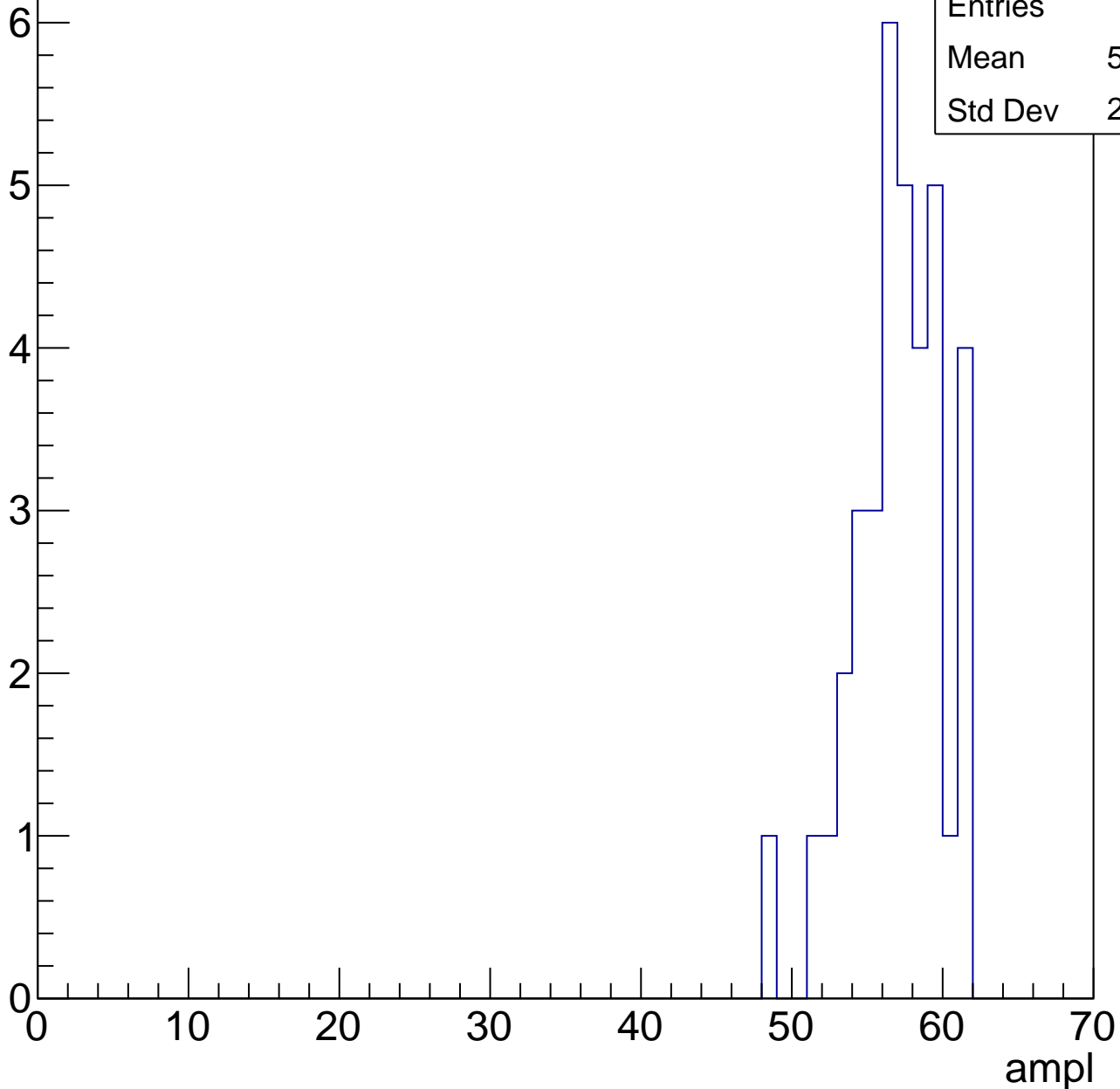
10

# B0L001S, U17-ch117, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	36
Mean	56.56
Std Dev	2.929



# B0L001S, U17-ch117, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	45
Mean	59.11
Std Dev	9.183

Entry

10

8

6

4

2

0

0

10

20

30

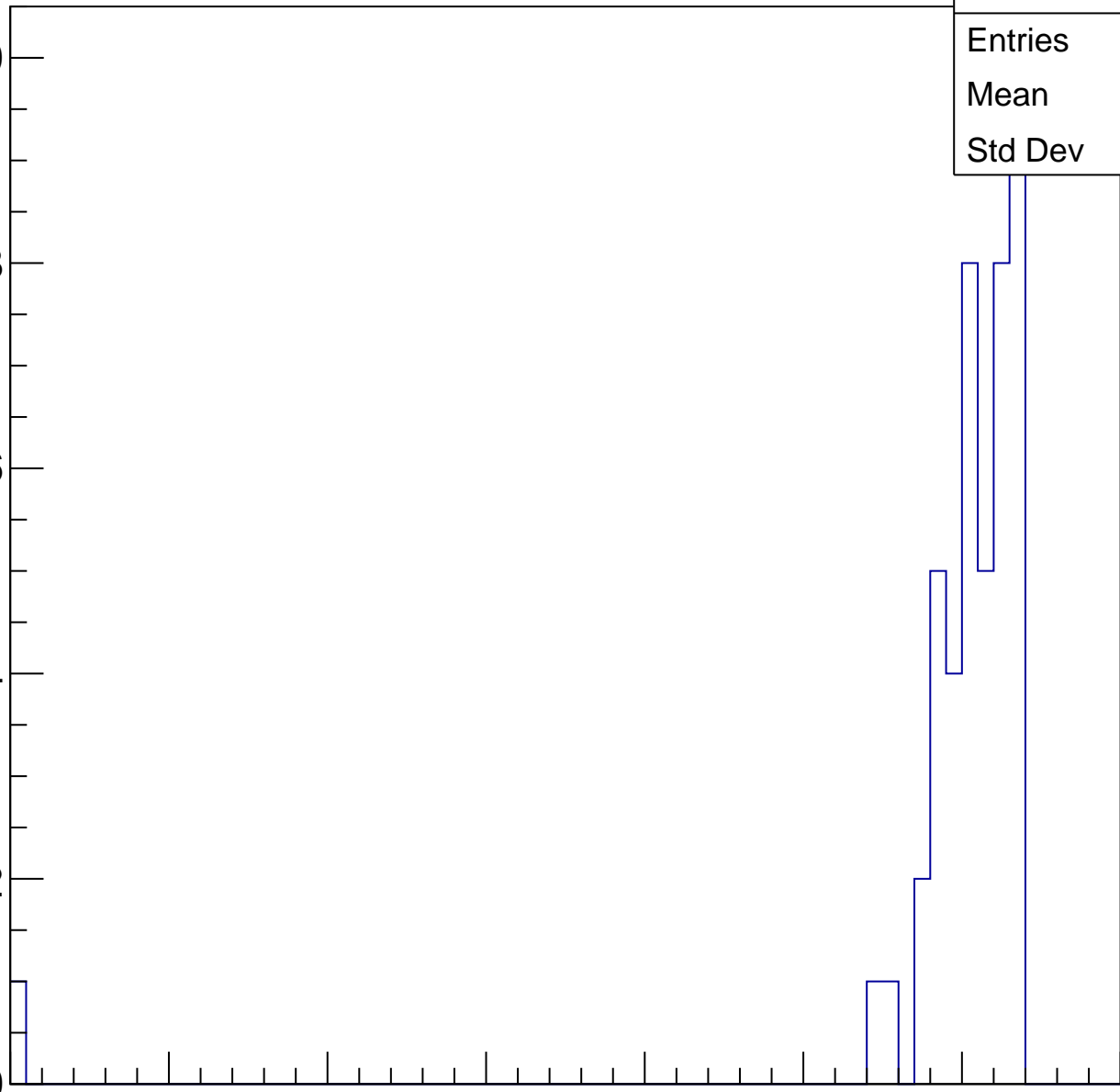
40

50

60

ampl

70



# B0L001S, U17-ch117, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch117, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U17-ch118, adc0

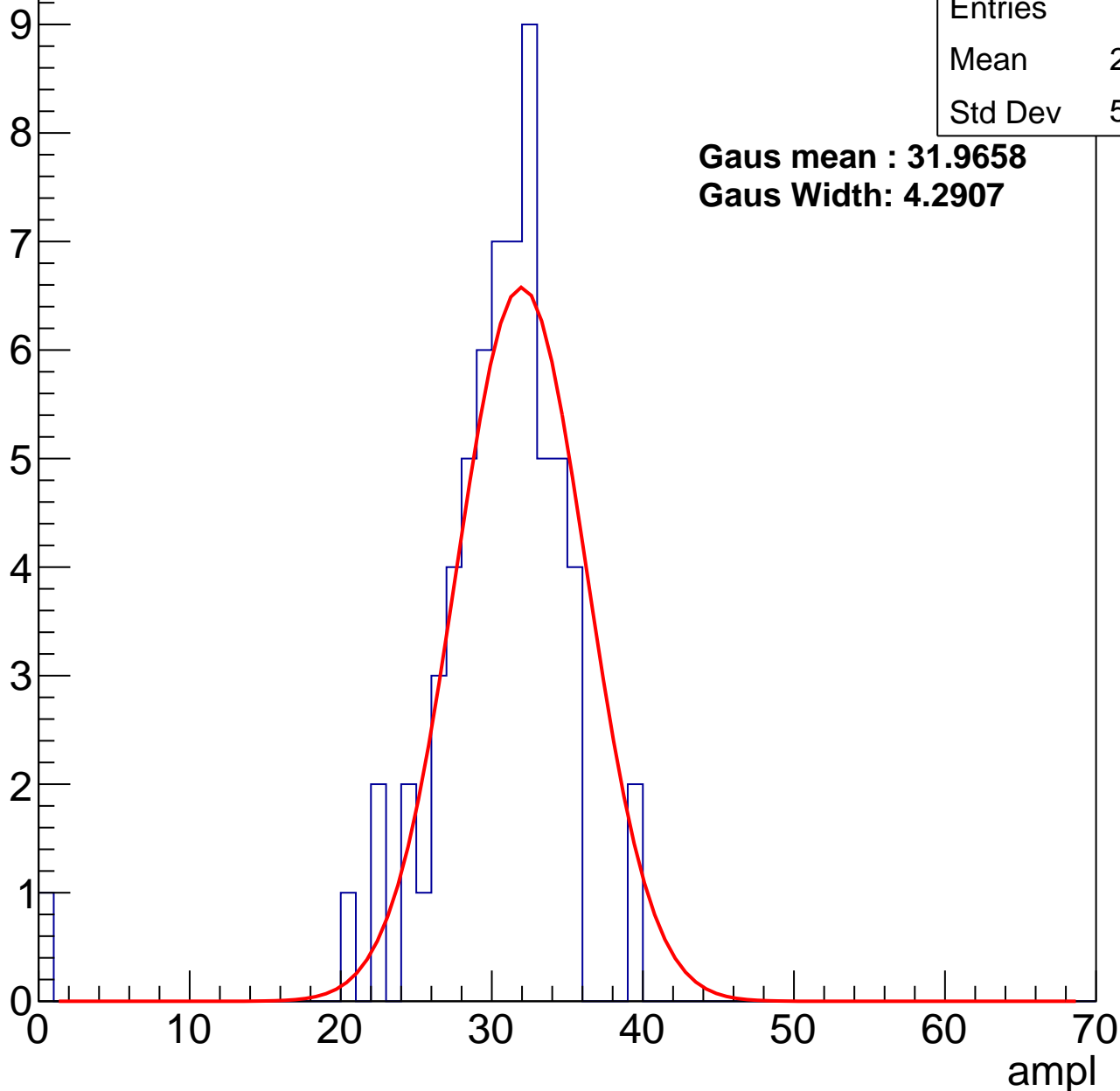
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	29.77
Std Dev	5.246

**Gaus mean : 31.9658**

**Gaus Width: 4.2907**



# B0L001S, U17-ch118, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	66
Mean	36.8
Std Dev	3.465

**Gaus mean : 37.5505**

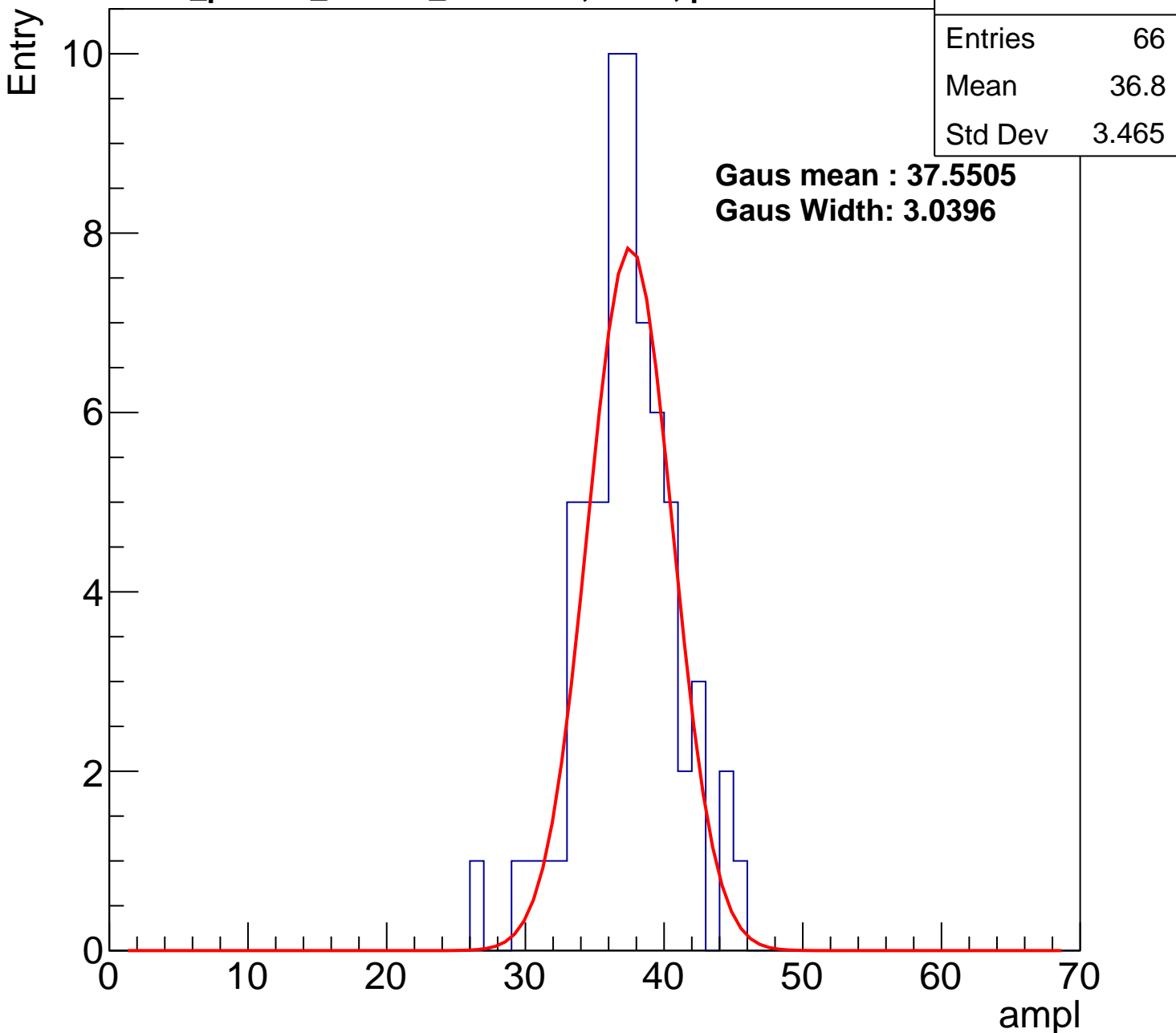
**Gaus Width: 3.0396**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B0L001S, U17-ch118, adc2

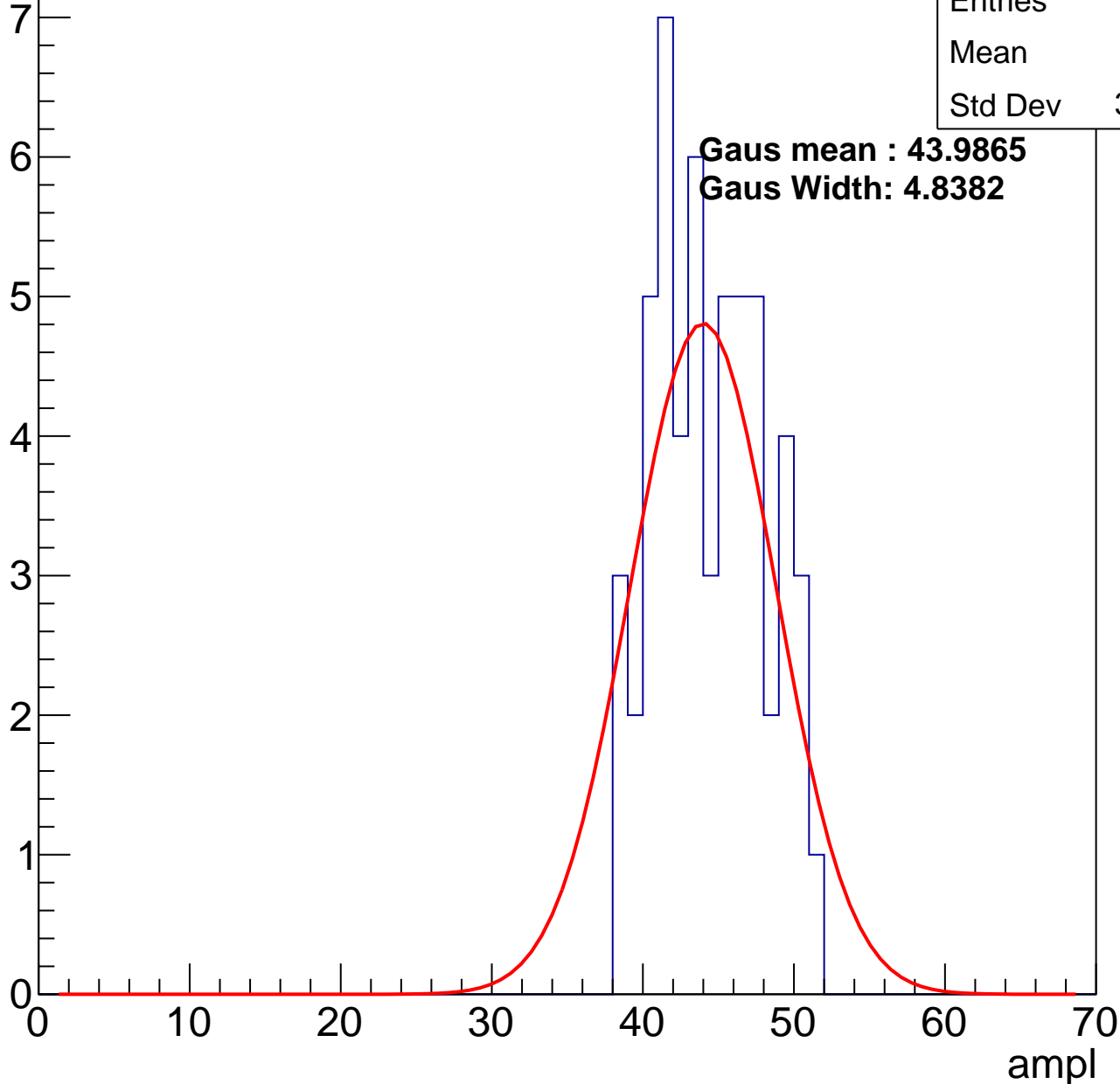
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	44
Std Dev	3.521

**Gaus mean : 43.9865**

**Gaus Width: 4.8382**

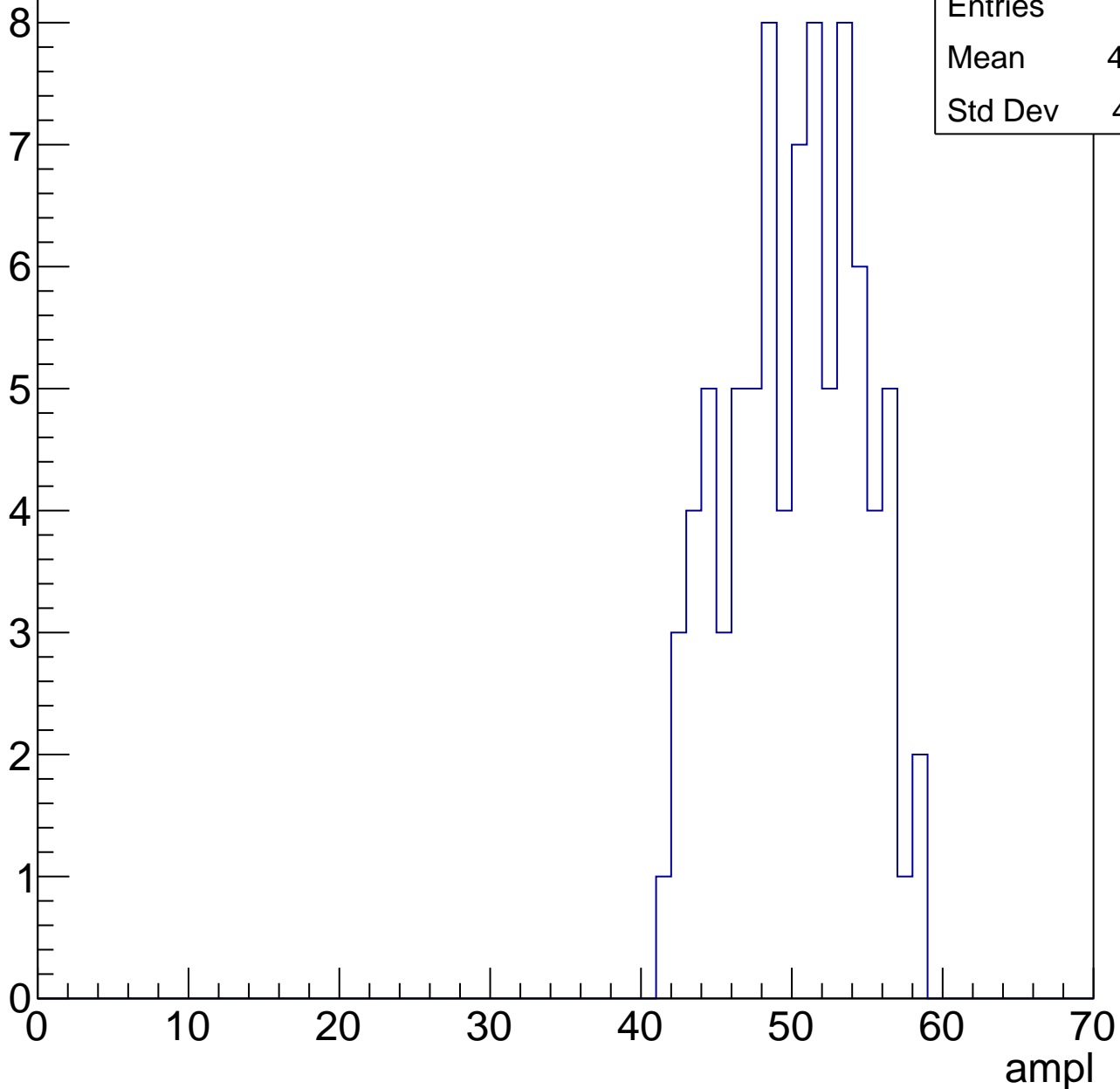


# B0L001S, U17-ch118, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

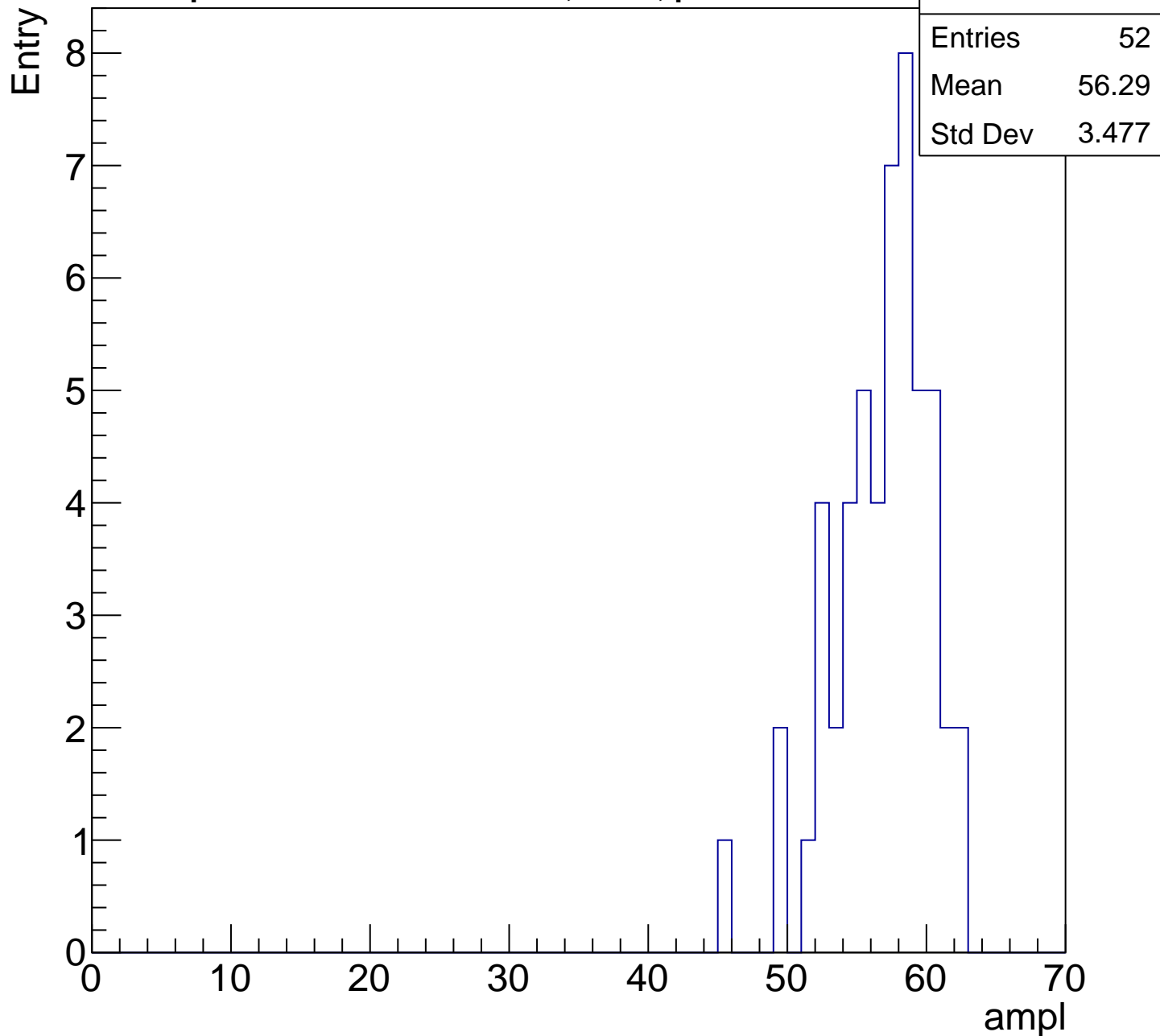
Entry

Entries	84
Mean	49.74
Std Dev	4.271



# B0L001S, U17-ch118, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

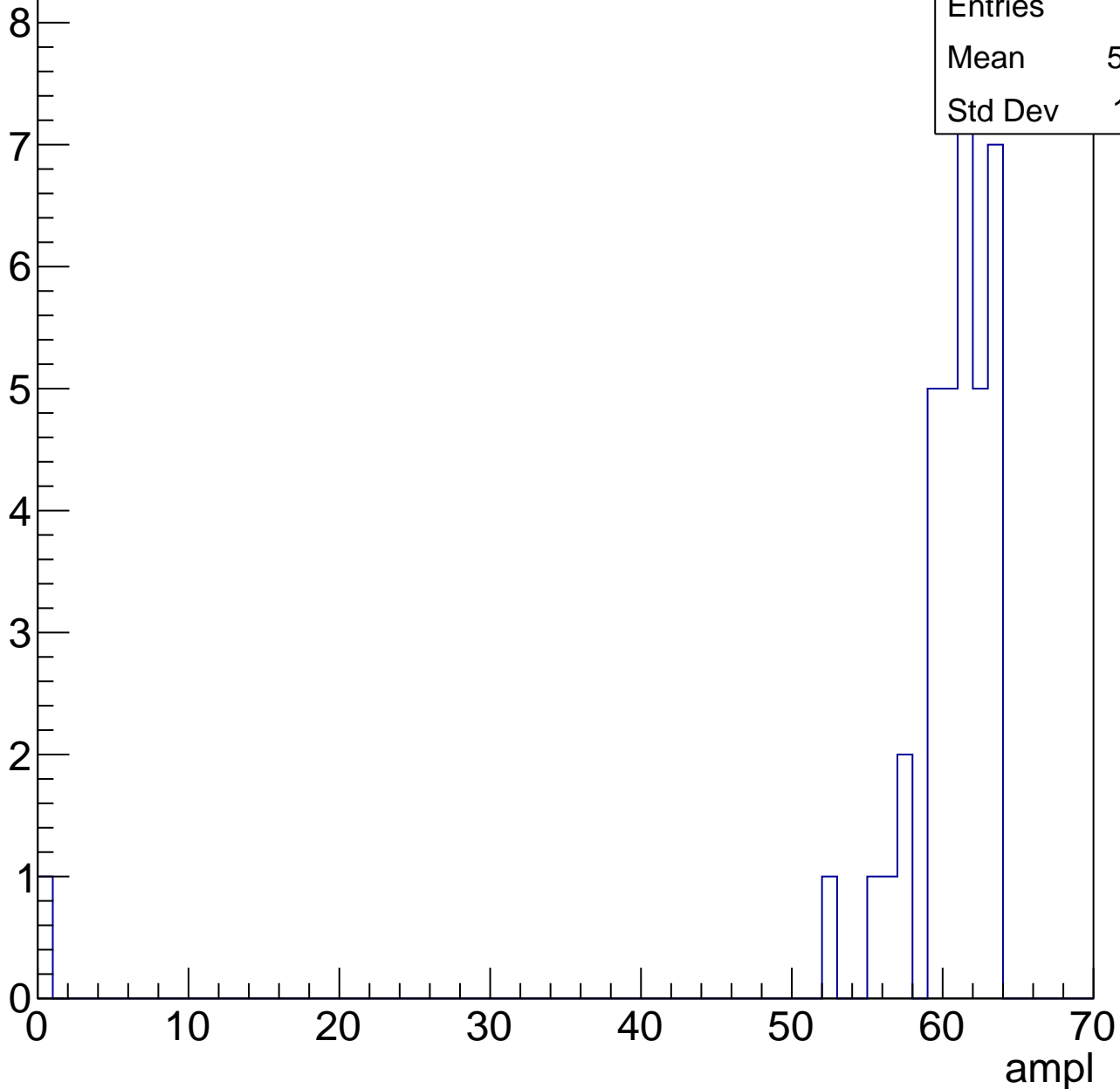


# B0L001S, U17-ch118, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	36
Mean	58.64
Std Dev	10.21



# B0L001S, U17-ch118, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch118, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U17-ch119, adc0

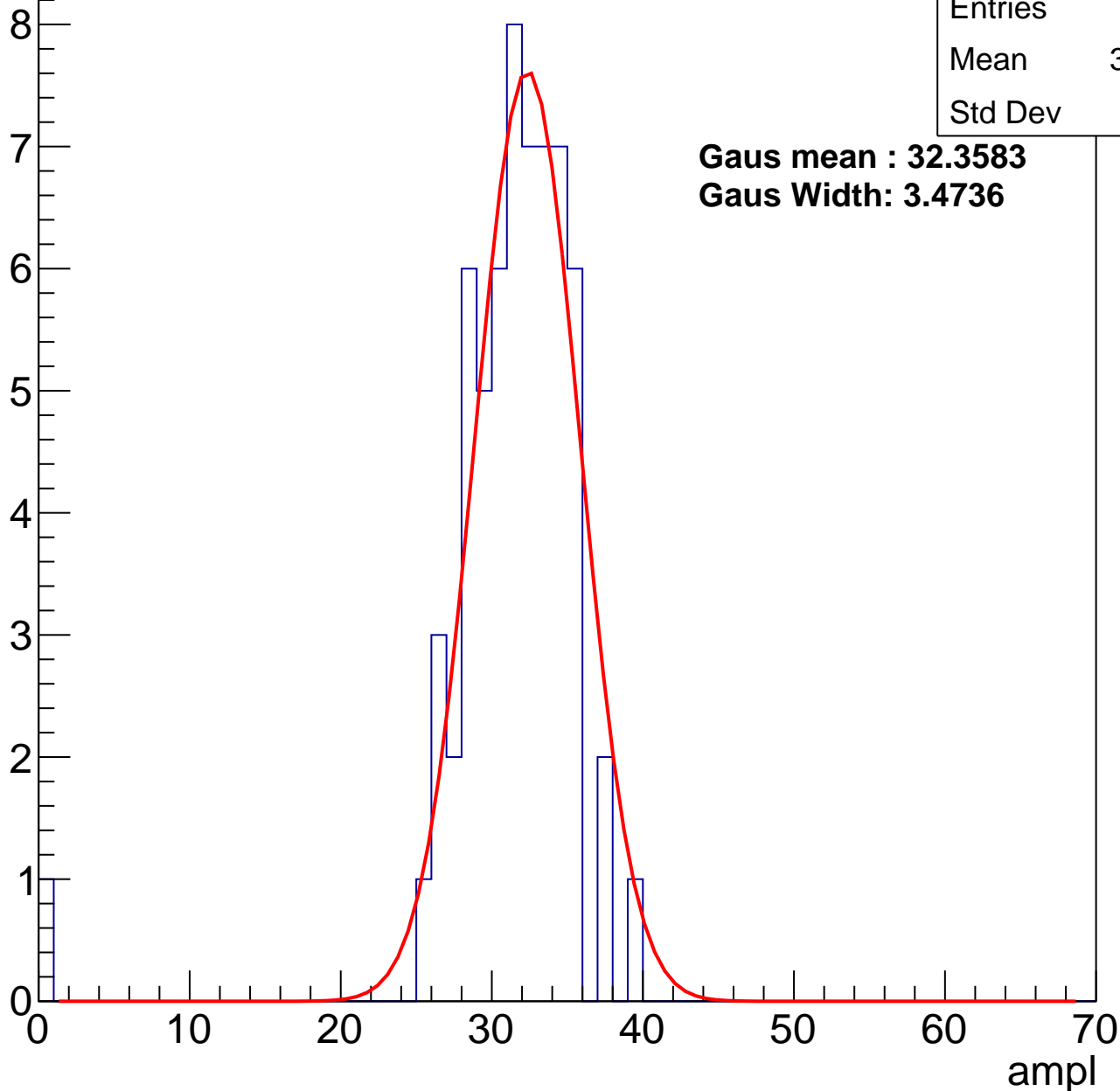
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	30.87
Std Dev	4.94

**Gaus mean : 32.3583**

**Gaus Width: 3.4736**



# B0L001S, U17-ch119, adc1

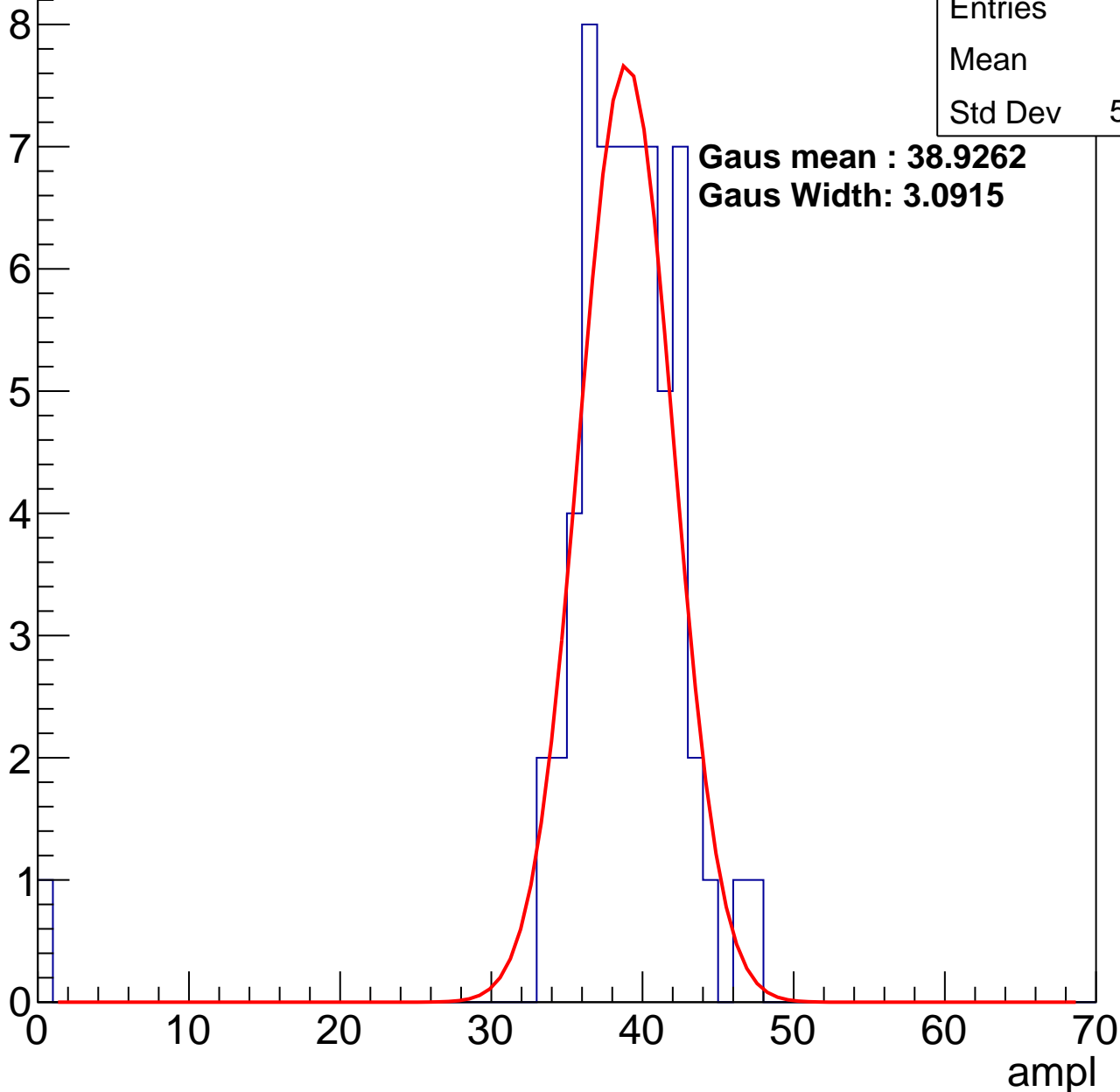
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	38.1
Std Dev	5.713

**Gaus mean : 38.9262**

**Gaus Width: 3.0915**



# B0L001S, U17-ch119, adc2

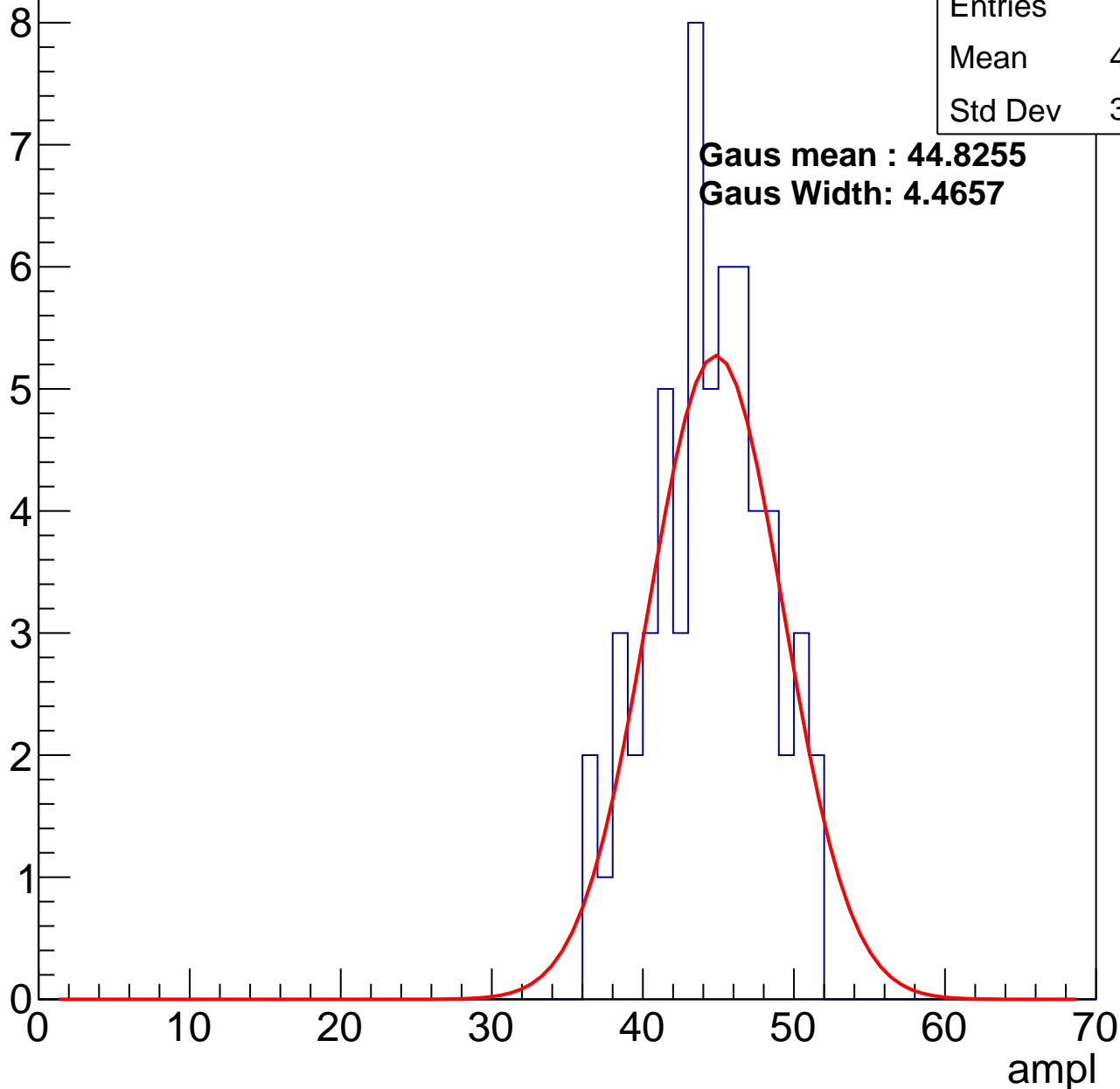
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	43.93
Std Dev	3.759

**Gaus mean : 44.8255**

**Gaus Width: 4.4657**

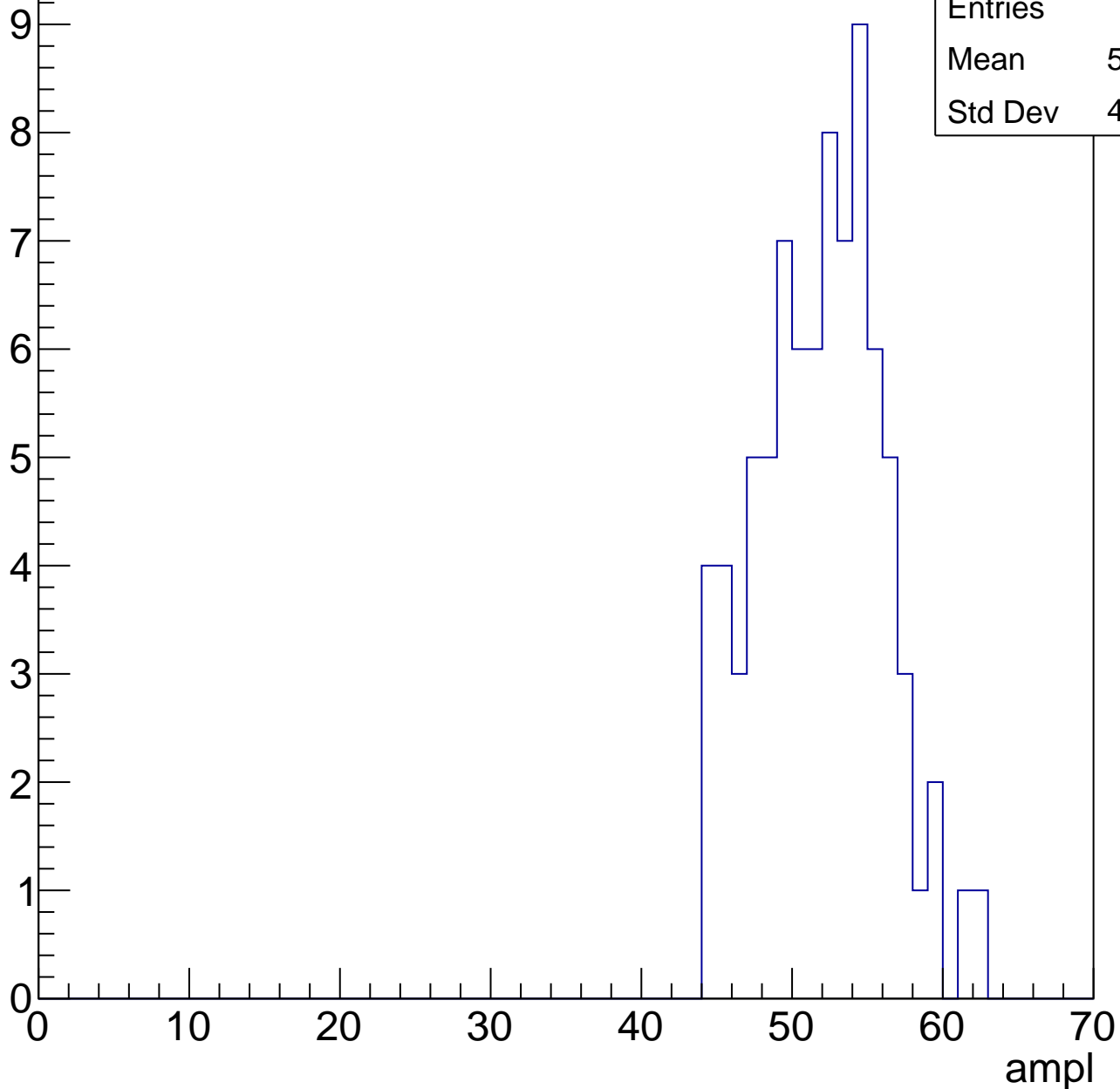


# B0L001S, U17-ch119, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	83
Mean	51.46
Std Dev	4.108

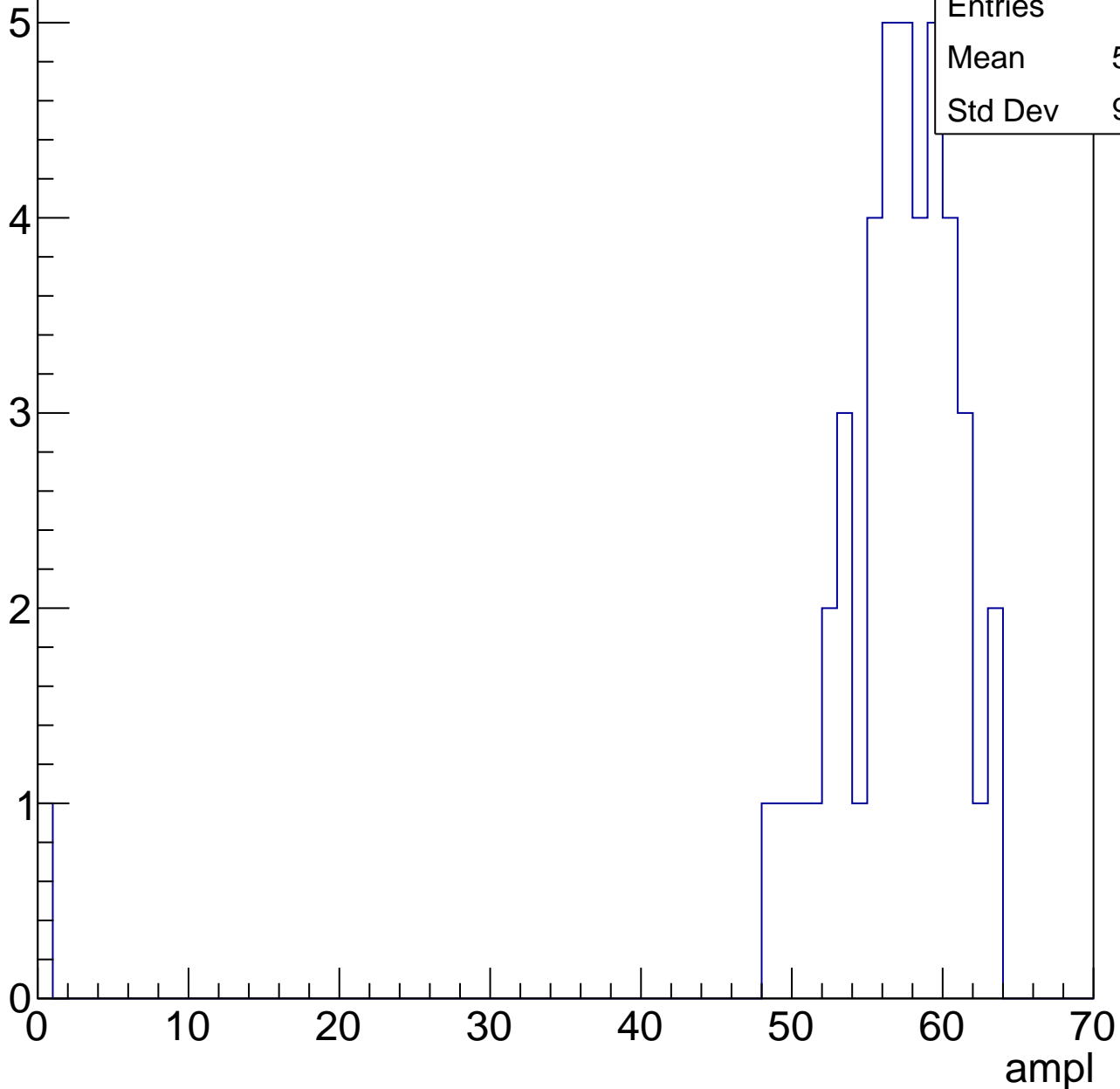


# B0L001S, U17-ch119, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	44
Mean	55.41
Std Dev	9.171

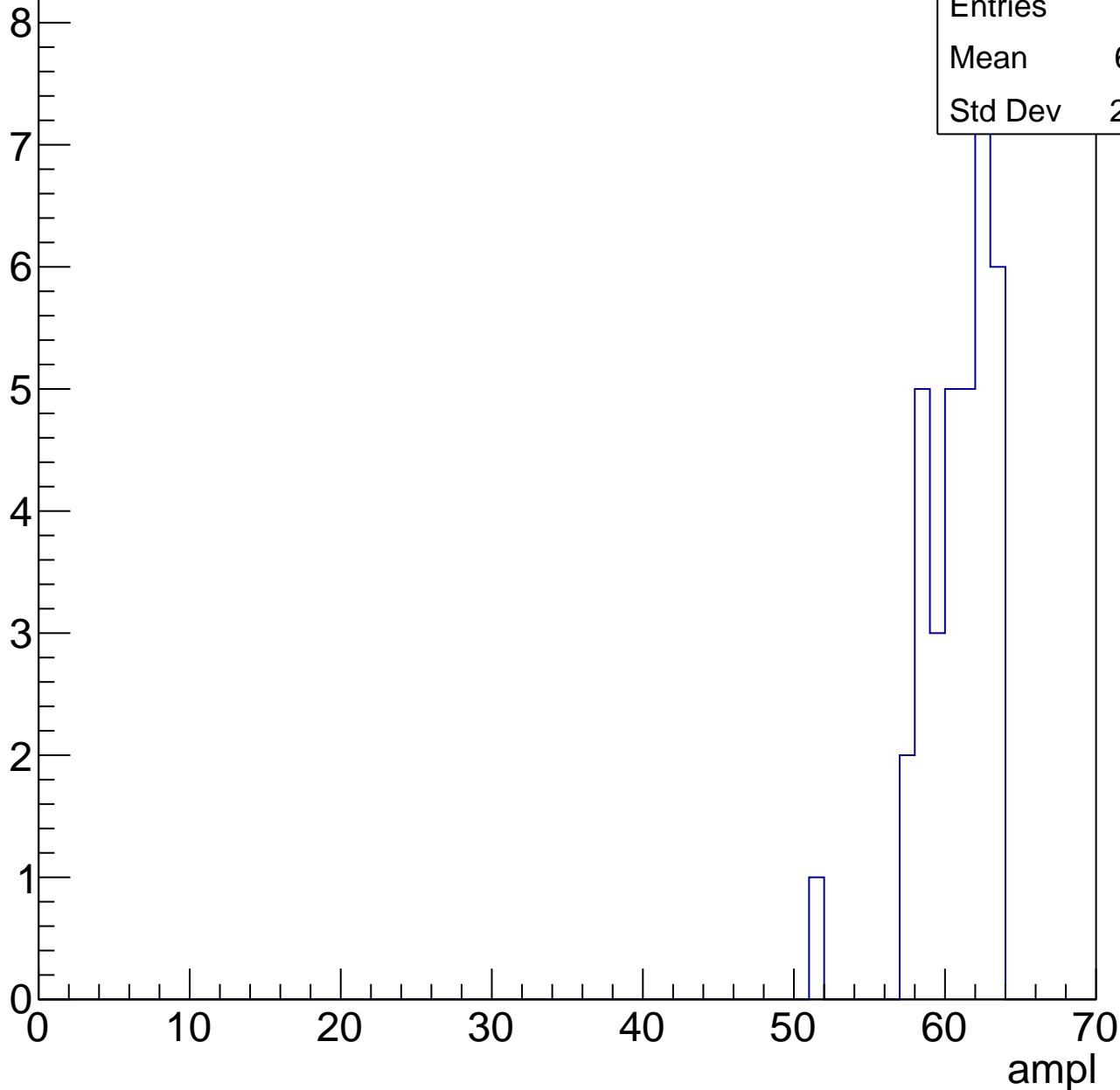


# B0L001S, U17-ch119, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	35
Mean	60.31
Std Dev	2.447



# B0L001S, U17-ch119, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch119, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	12.5
Std Dev	12.5

# B0L001S, U17-ch120, adc0

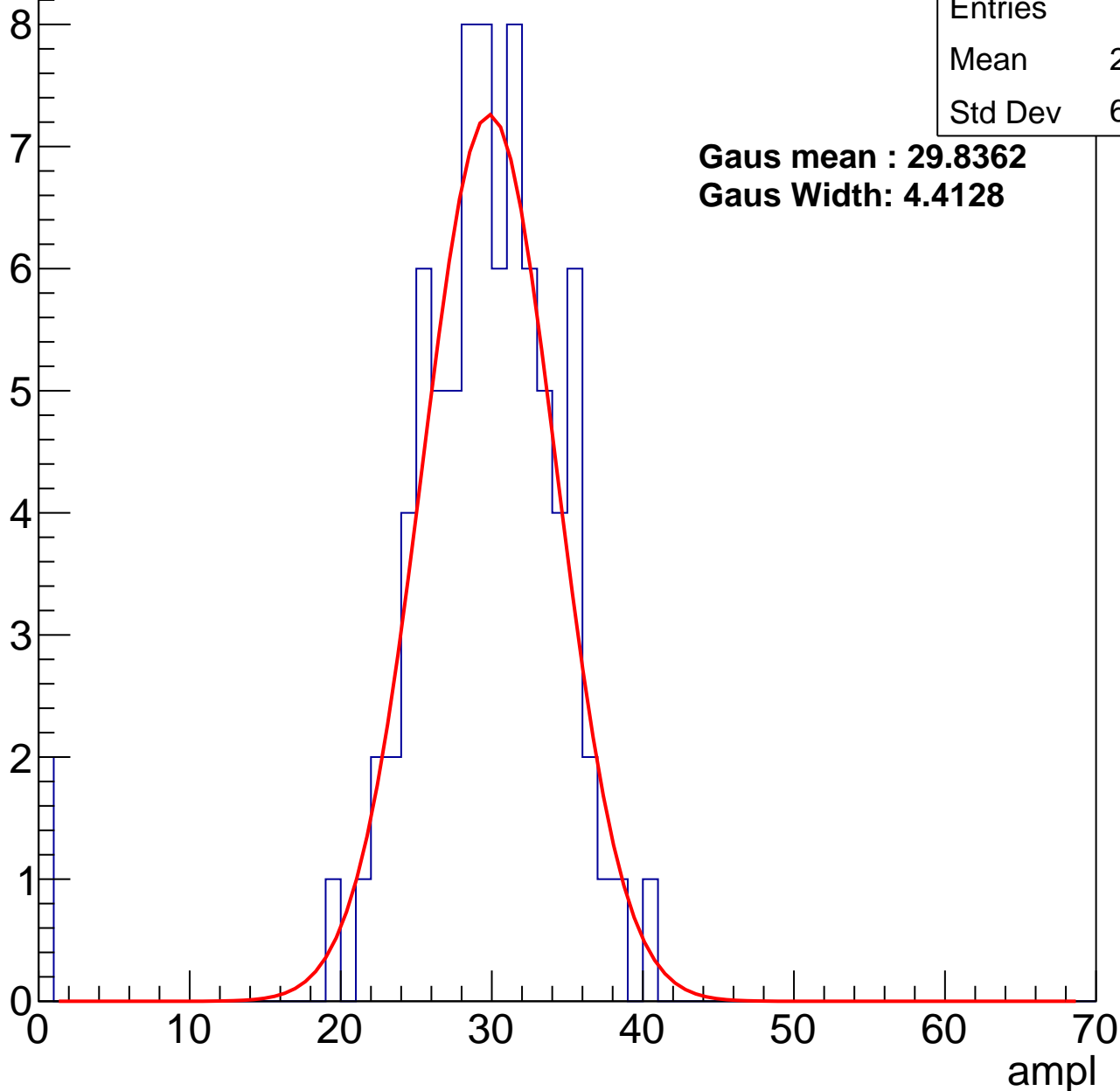
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	84
Mean	28.75
Std Dev	6.106

**Gaus mean : 29.8362**

**Gaus Width: 4.4128**



# B0L001S, U17-ch120, adc1

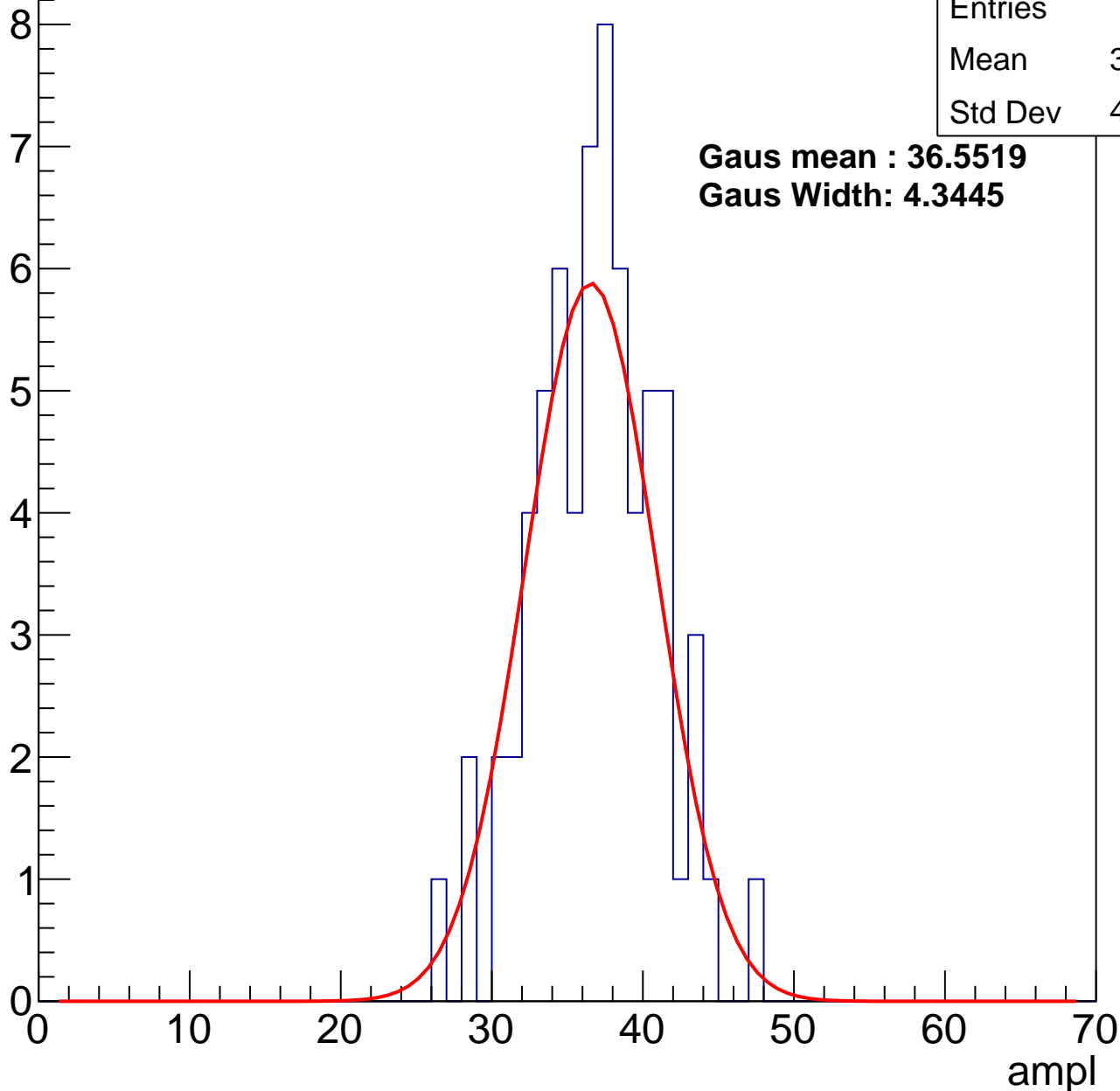
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	36.42
Std Dev	4.082

**Gaus mean : 36.5519**

**Gaus Width: 4.3445**



# B0L001S, U17-ch120, adc2

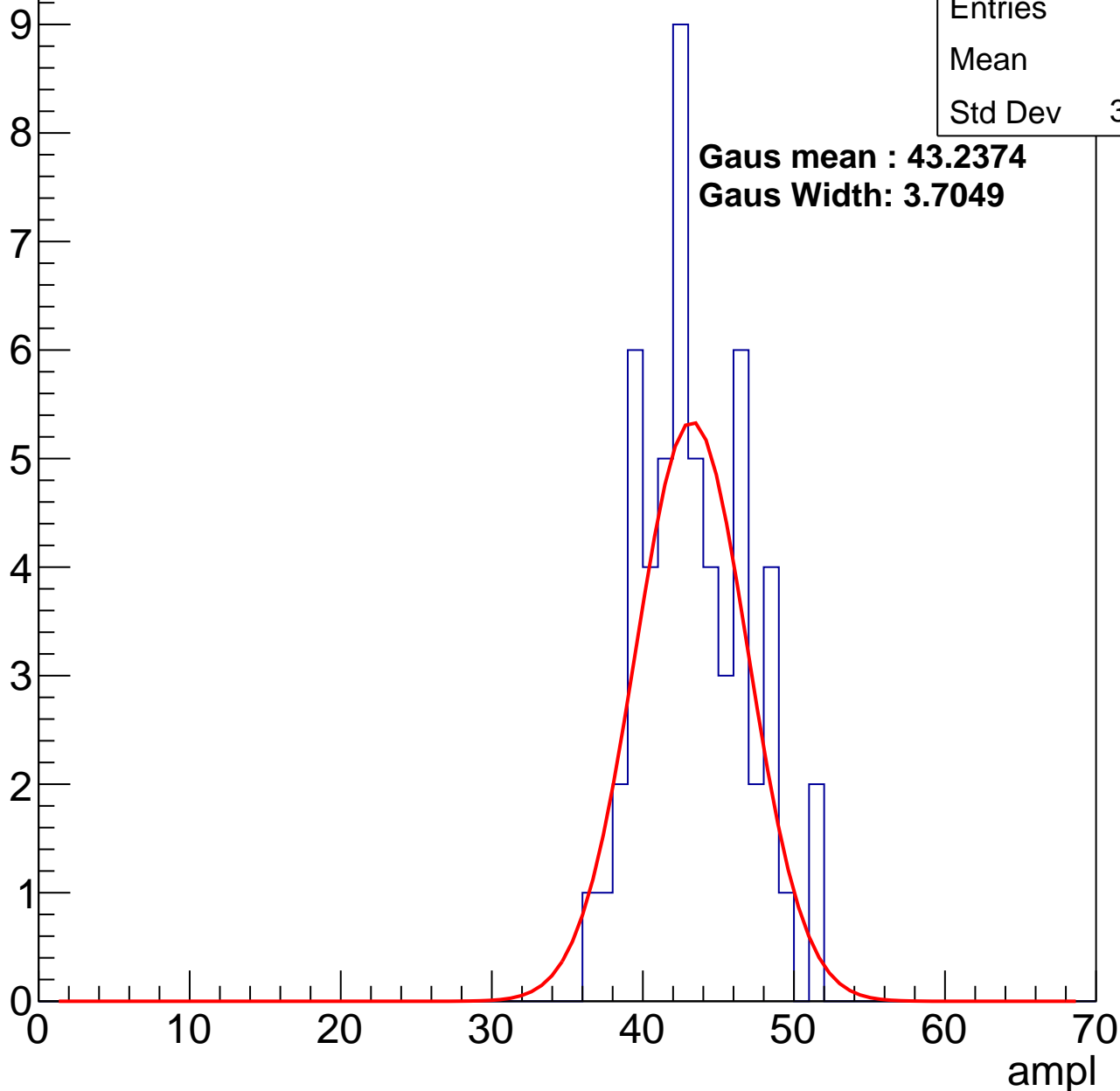
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	43
Std Dev	3.469

**Gaus mean : 43.2374**

**Gaus Width: 3.7049**

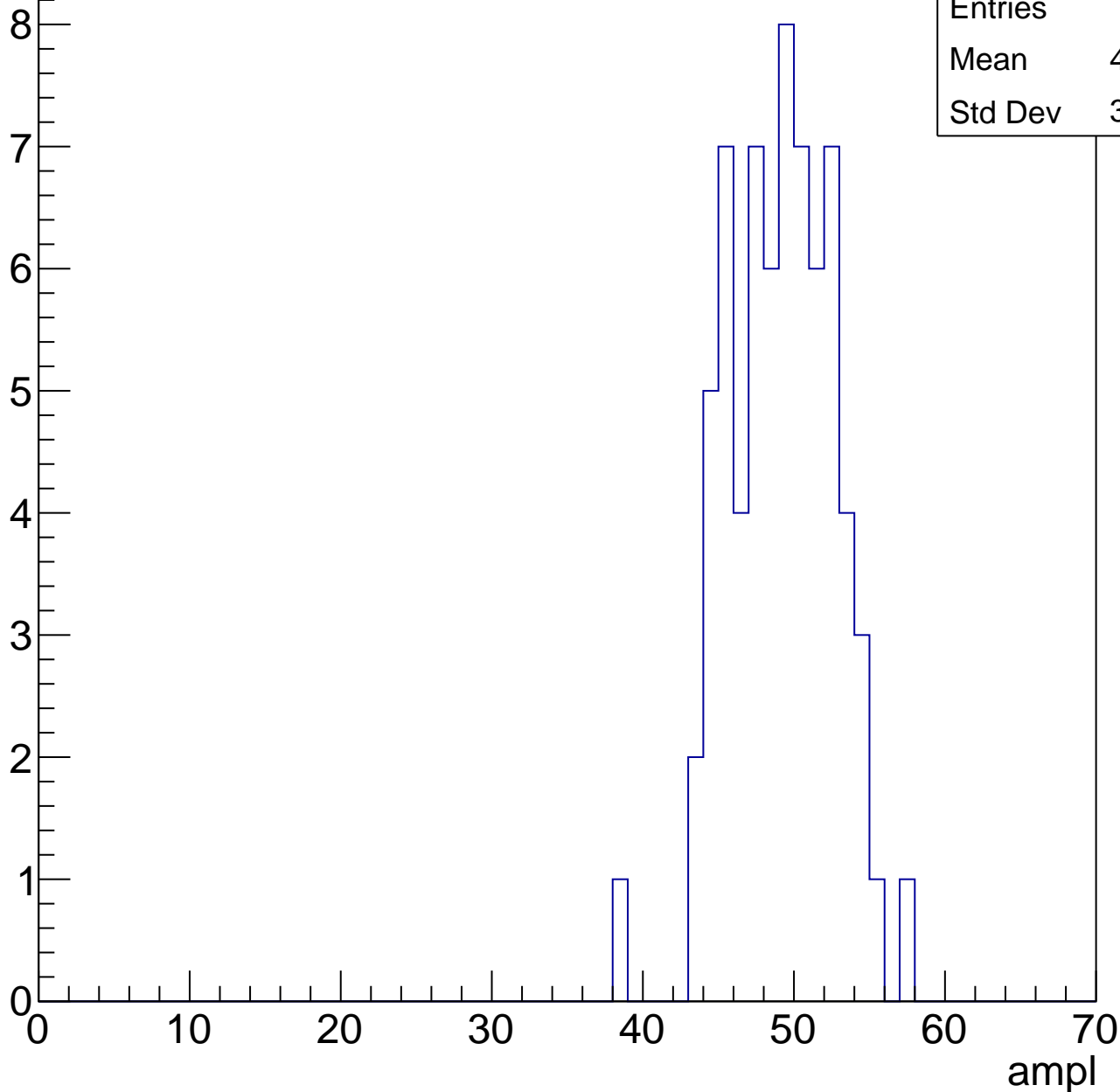


# B0L001S, U17-ch120, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	48.67
Std Dev	3.459

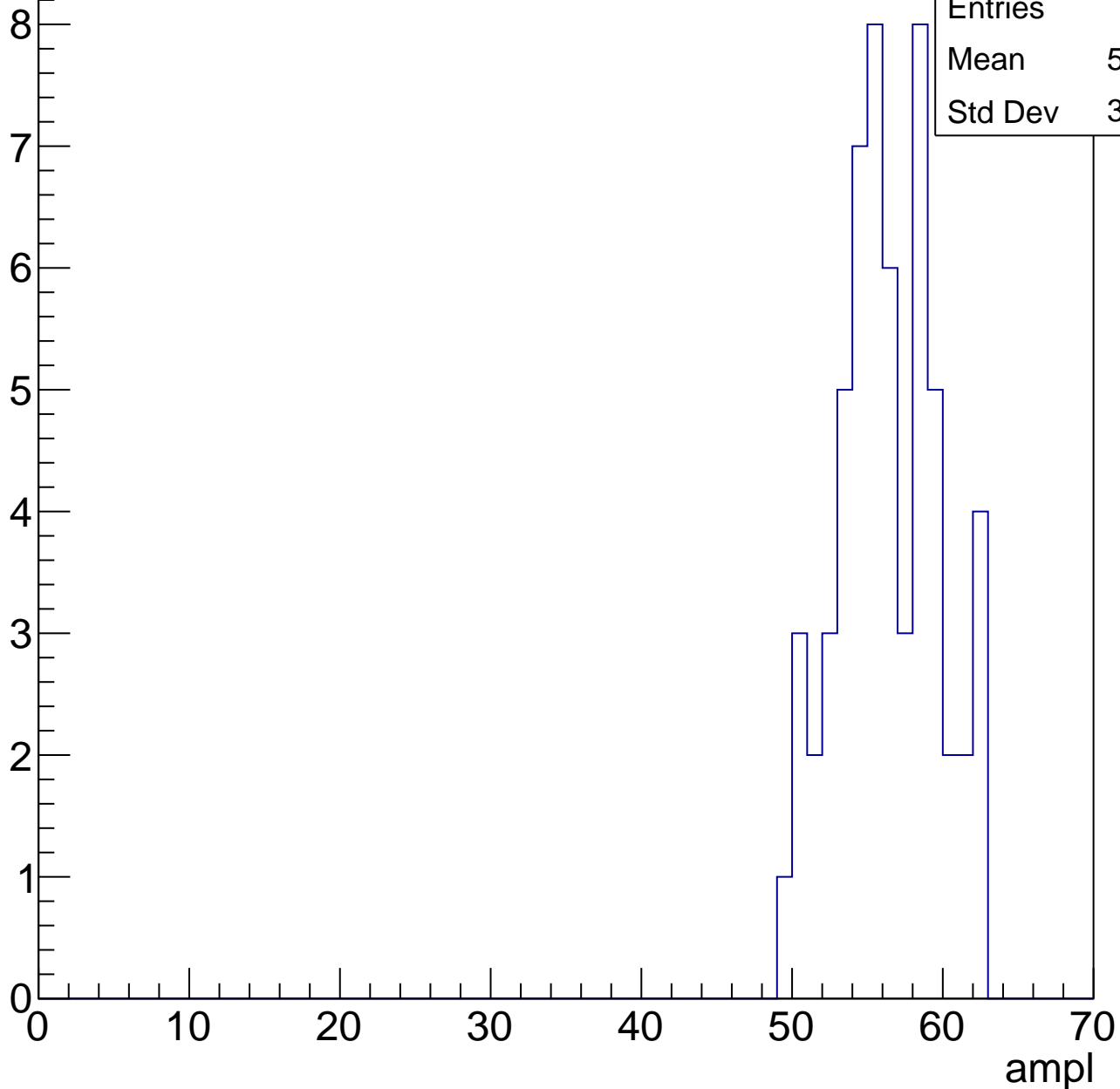


# B0L001S, U17-ch120, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	55.86
Std Dev	3.296

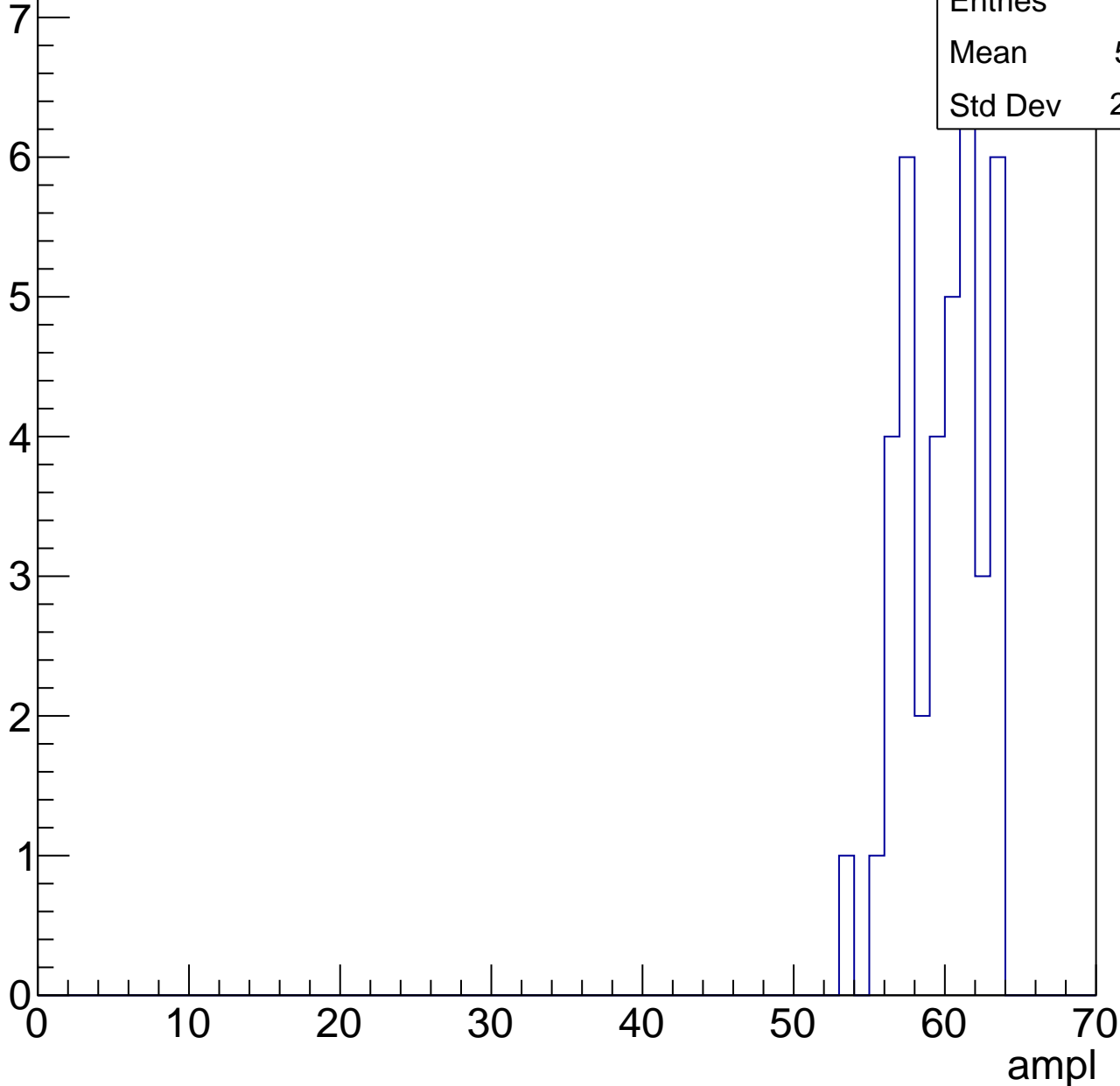


# B0L001S, U17-ch120, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

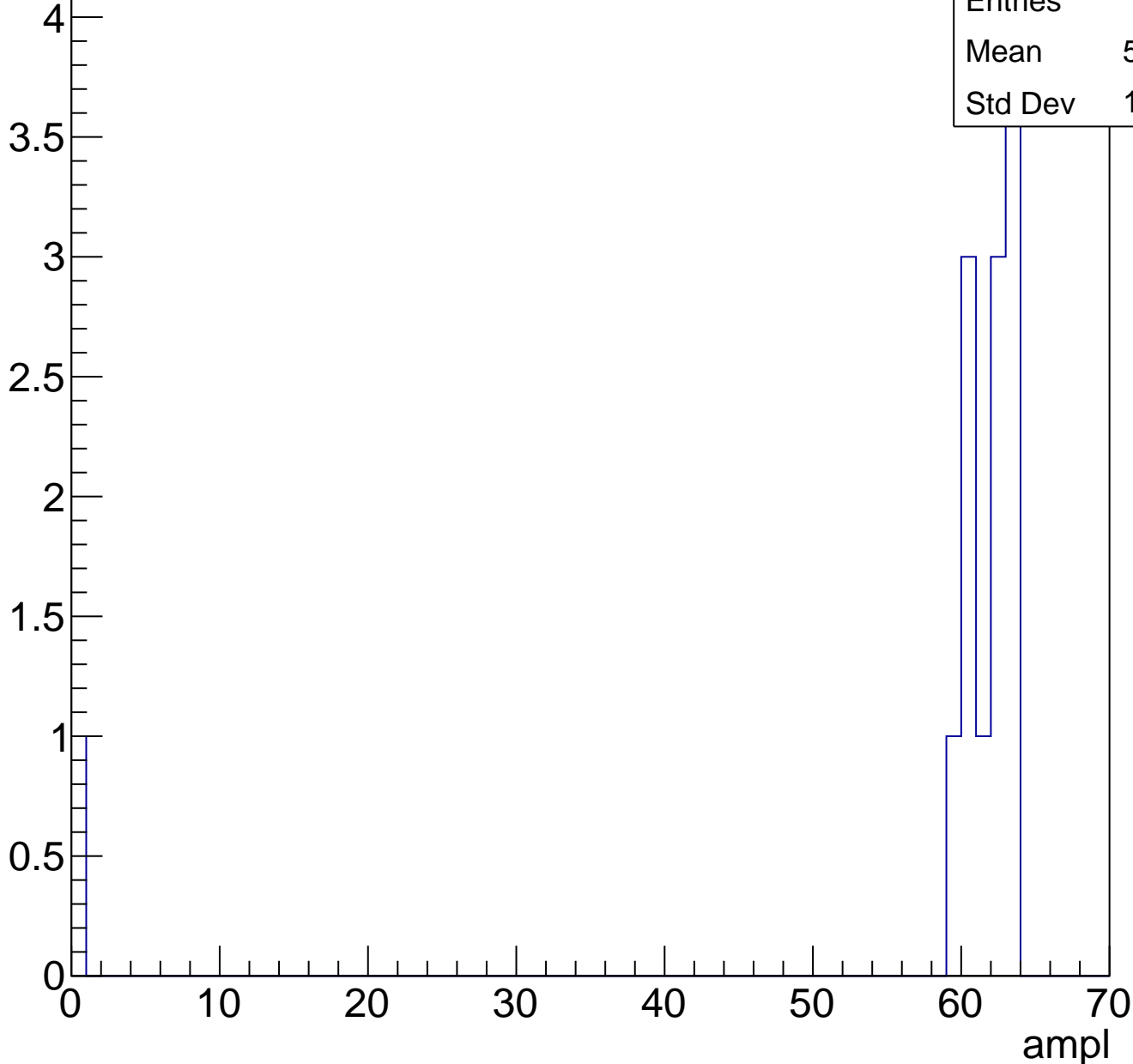
Entries	39
Mean	59.41
Std Dev	2.599



# B0L001S, U17-ch120, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch120, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	3
Mean	0
Std Dev	0

# B0L001S, U17-ch121, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	77
Mean	28.42
Std Dev	7.666

**Gaus mean : 30.6213**

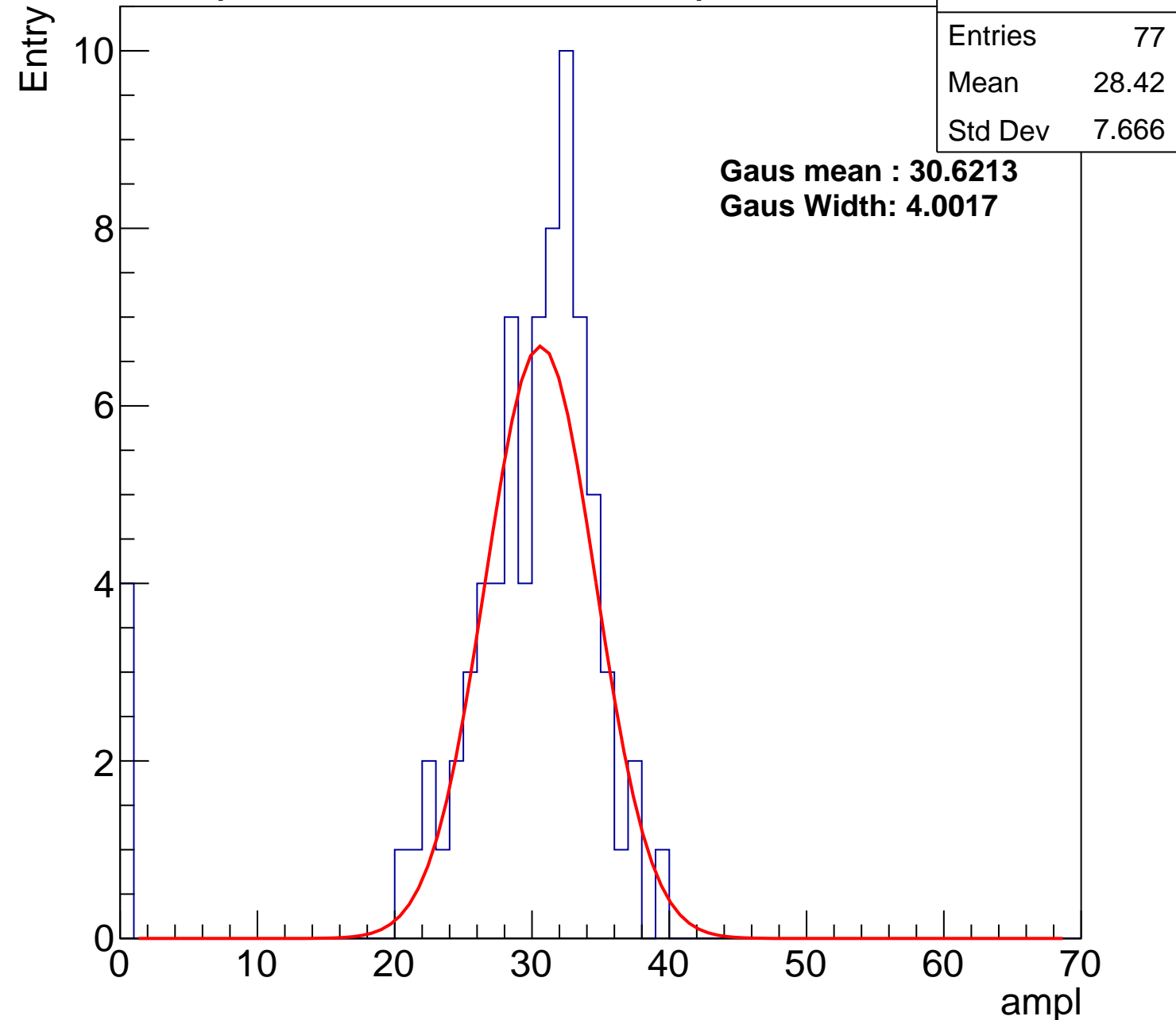
**Gaus Width: 4.0017**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U17-ch121, adc1

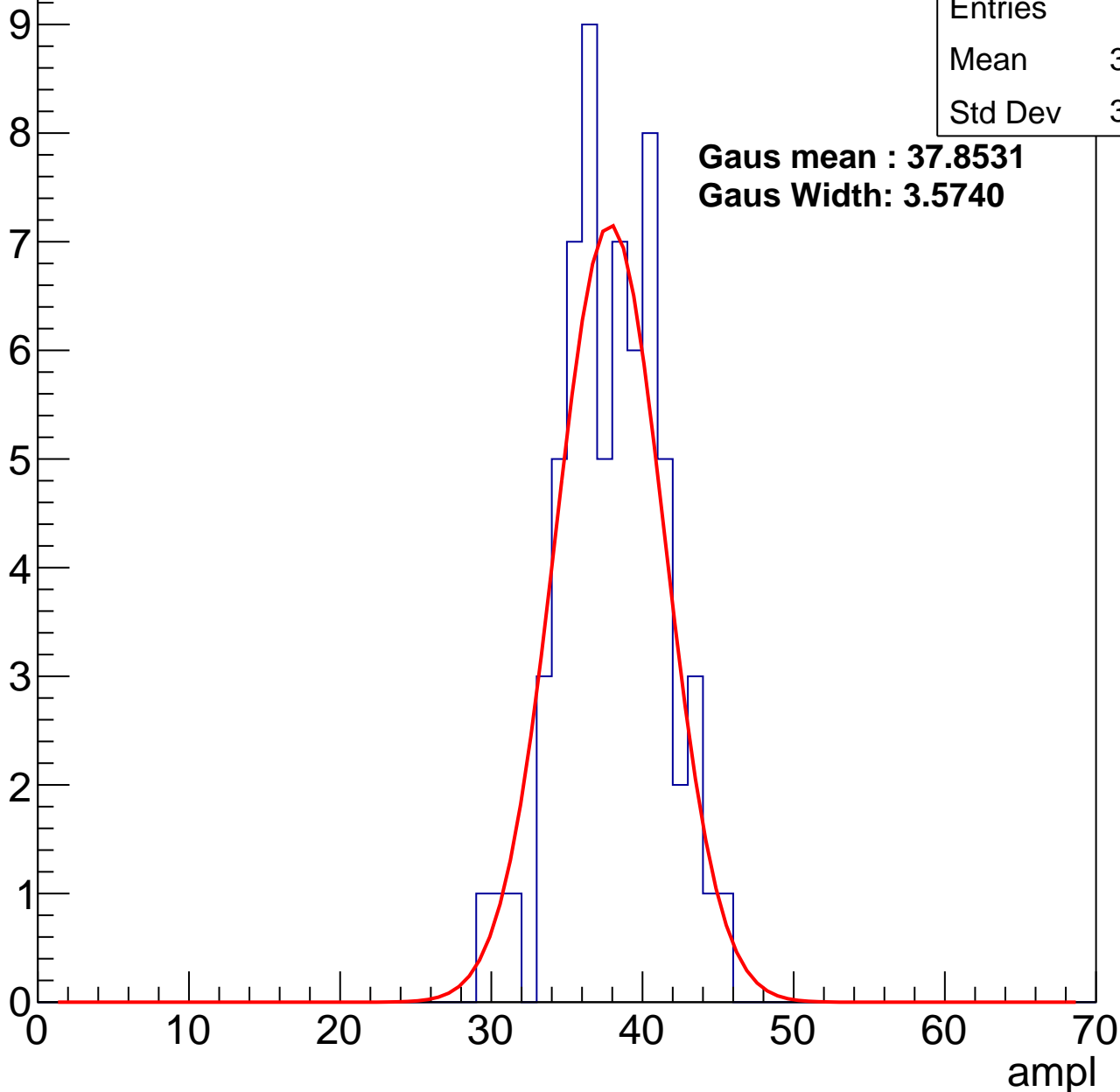
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	37.54
Std Dev	3.315

**Gaus mean : 37.8531**

**Gaus Width: 3.5740**



# B0L001S, U17-ch121, adc2

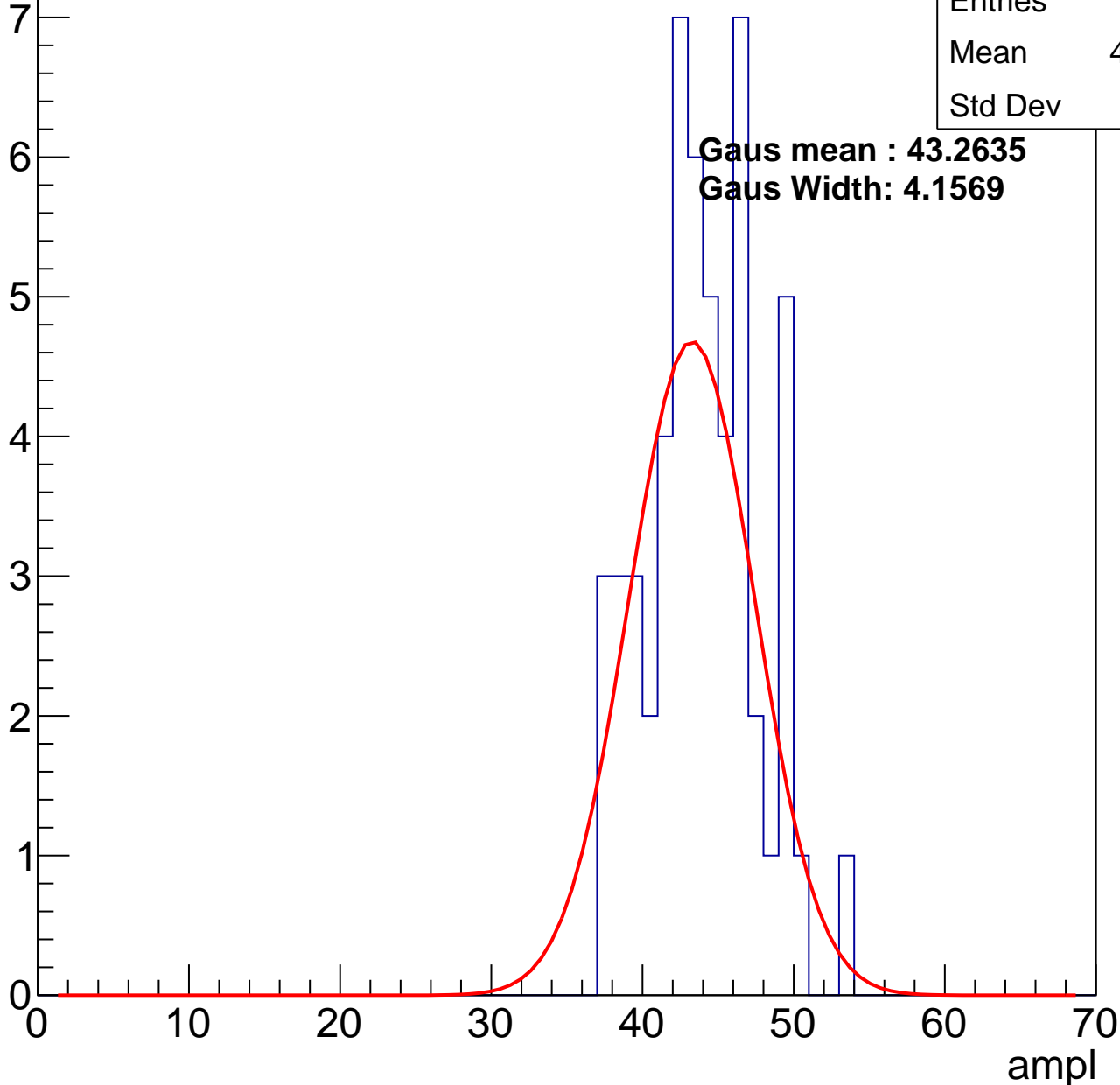
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	43.52
Std Dev	3.67

**Gaus mean : 43.2635**

**Gaus Width: 4.1569**

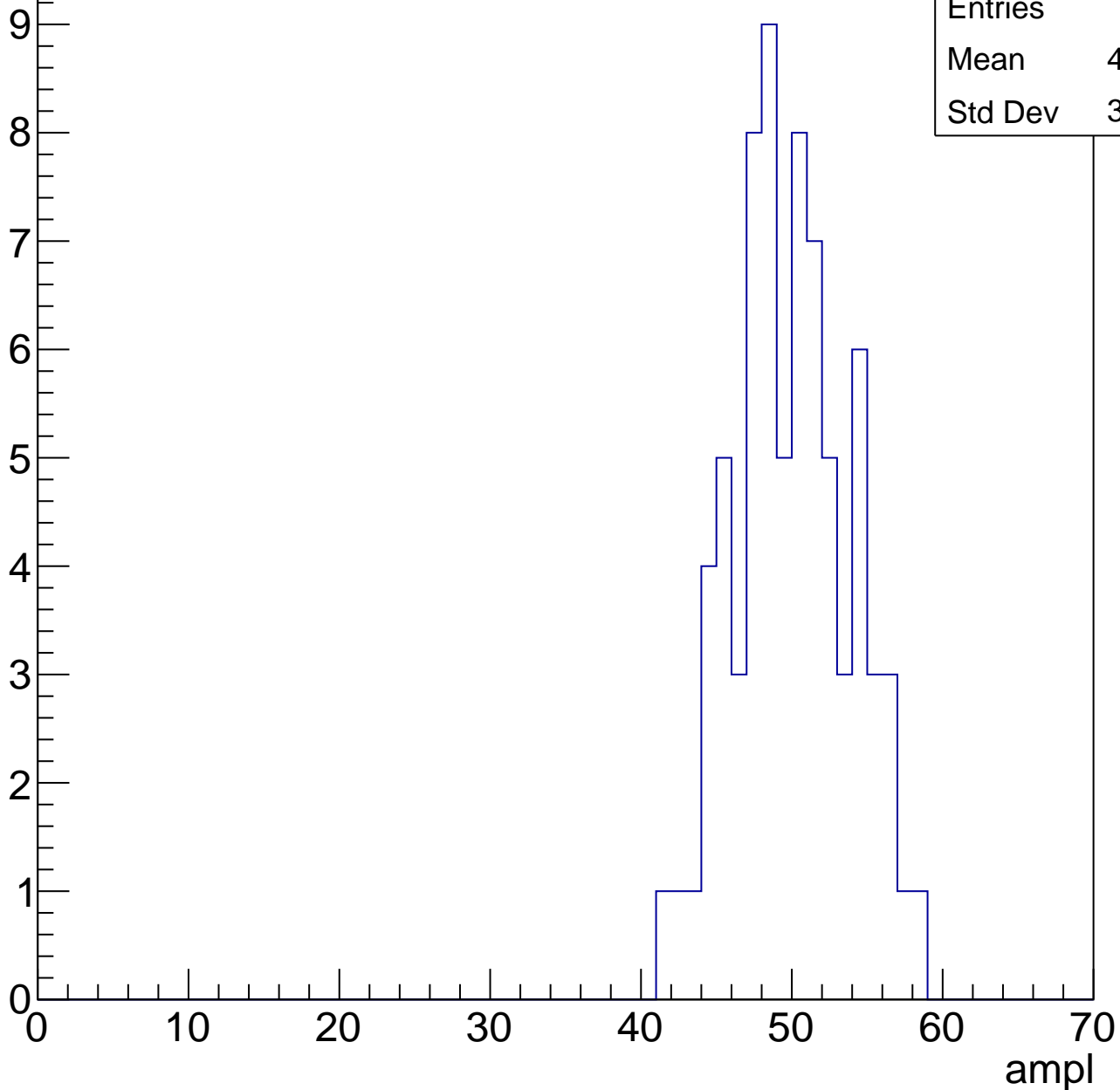


# B0L001S, U17-ch121, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	49.54
Std Dev	3.775

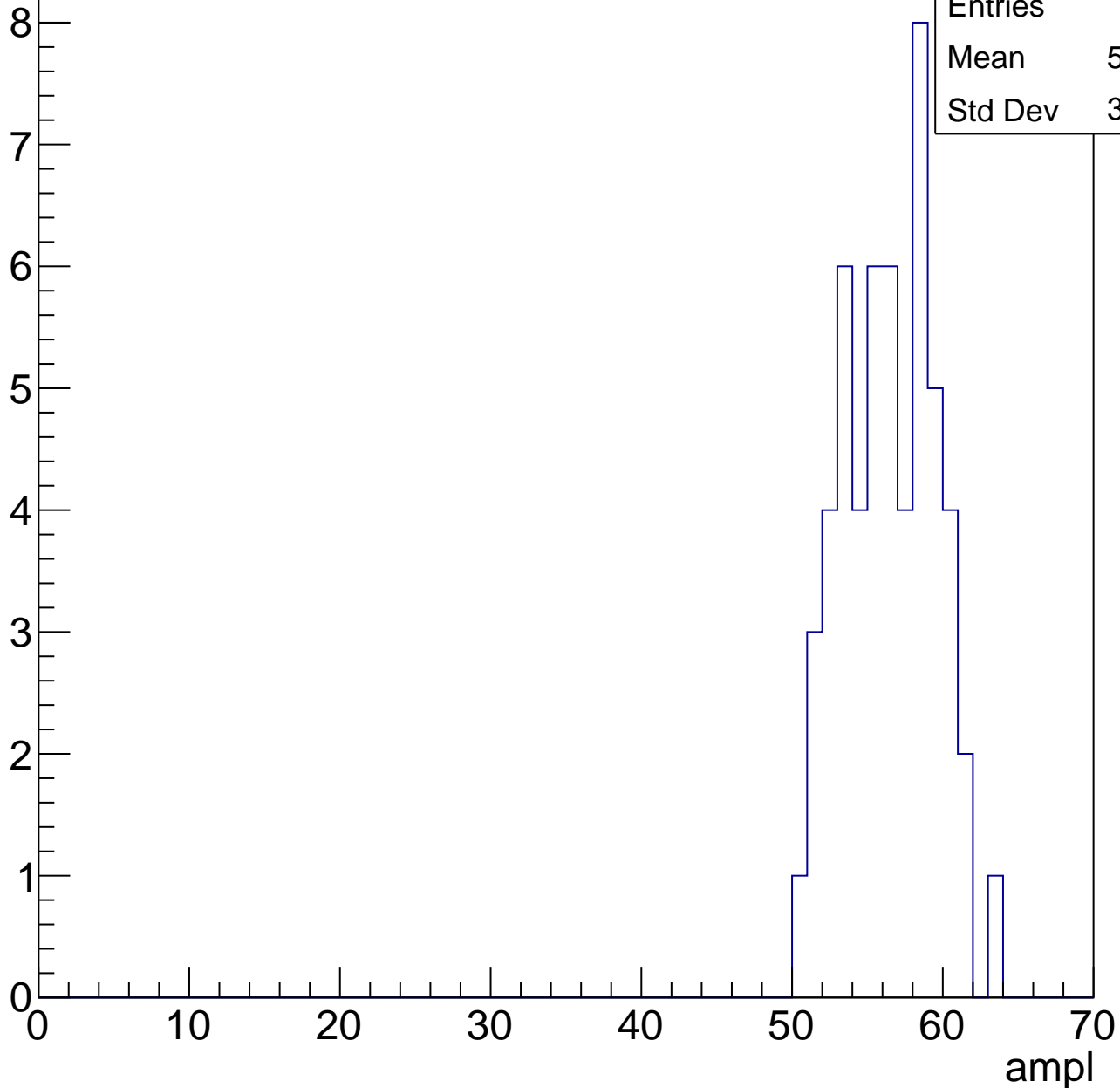


# B0L001S, U17-ch121, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	55.98
Std Dev	3.028

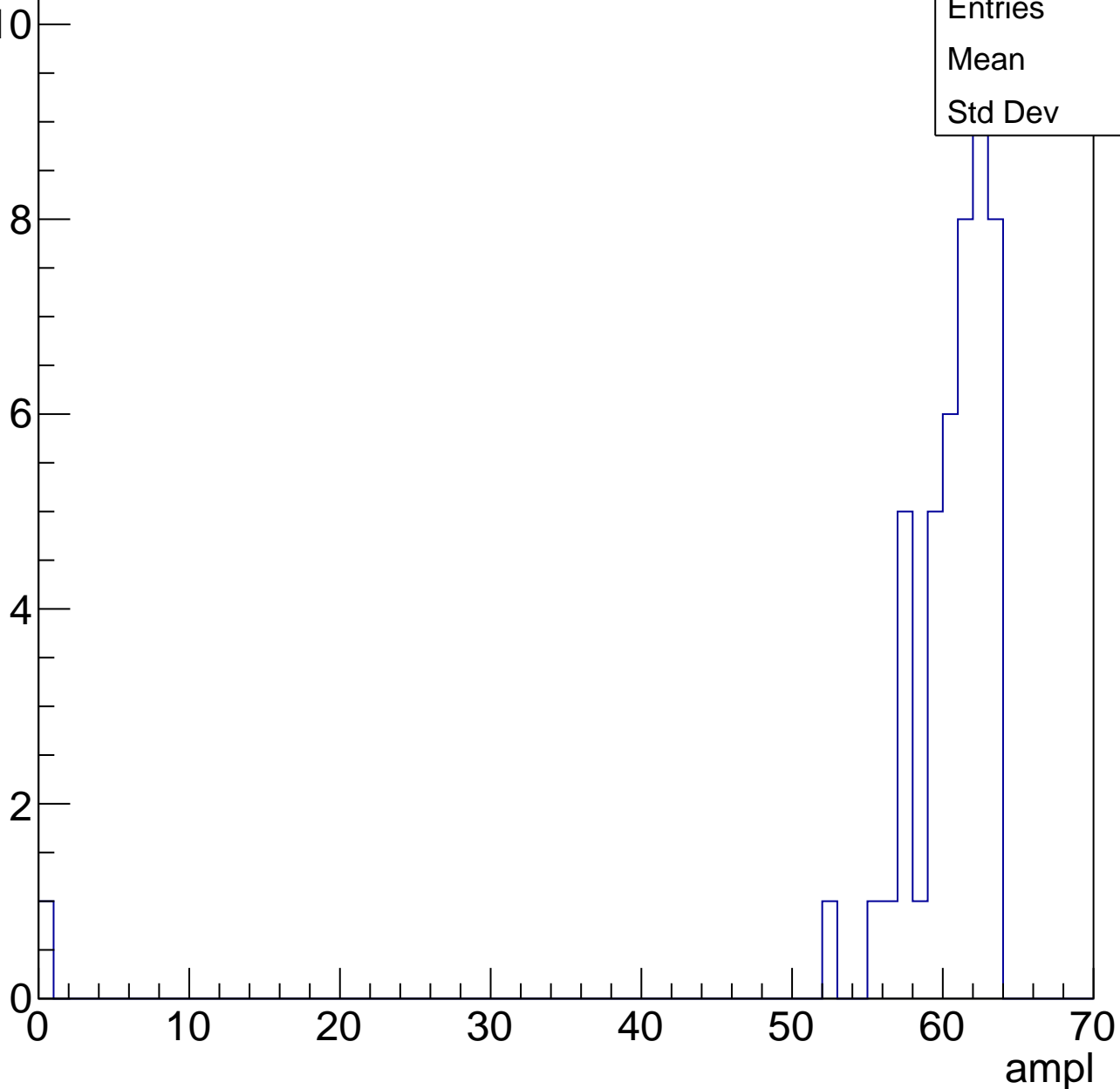


# B0L001S, U17-ch121, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	47
Mean	59
Std Dev	9.03



# B0L001S, U17-ch121, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch121, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U17-ch122, adc0

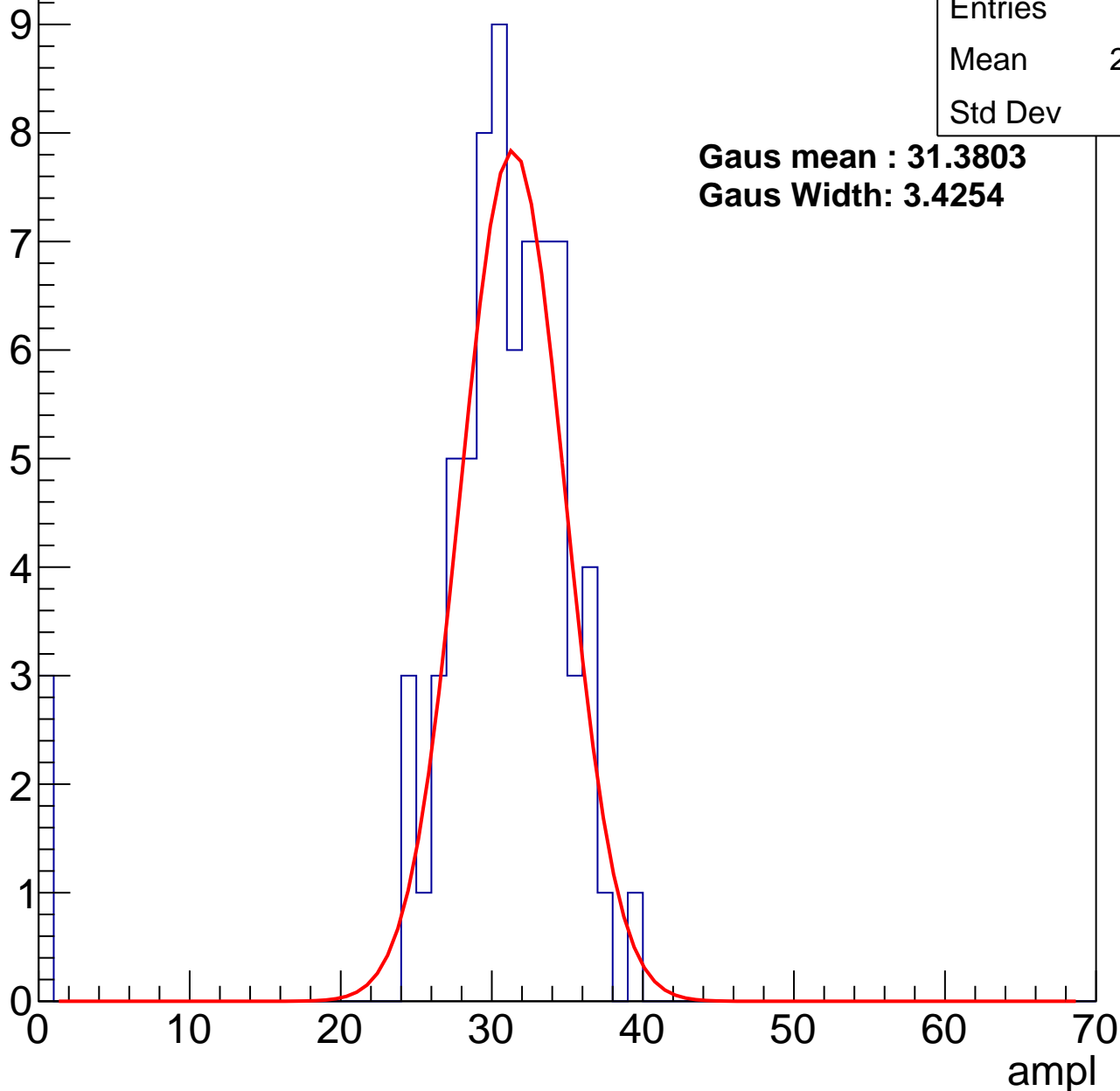
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	29.53
Std Dev	6.92

**Gaus mean : 31.3803**

**Gaus Width: 3.4254**



# B0L001S, U17-ch122, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	62
Mean	37.1
Std Dev	3.216

**Gaus mean : 38.0531**

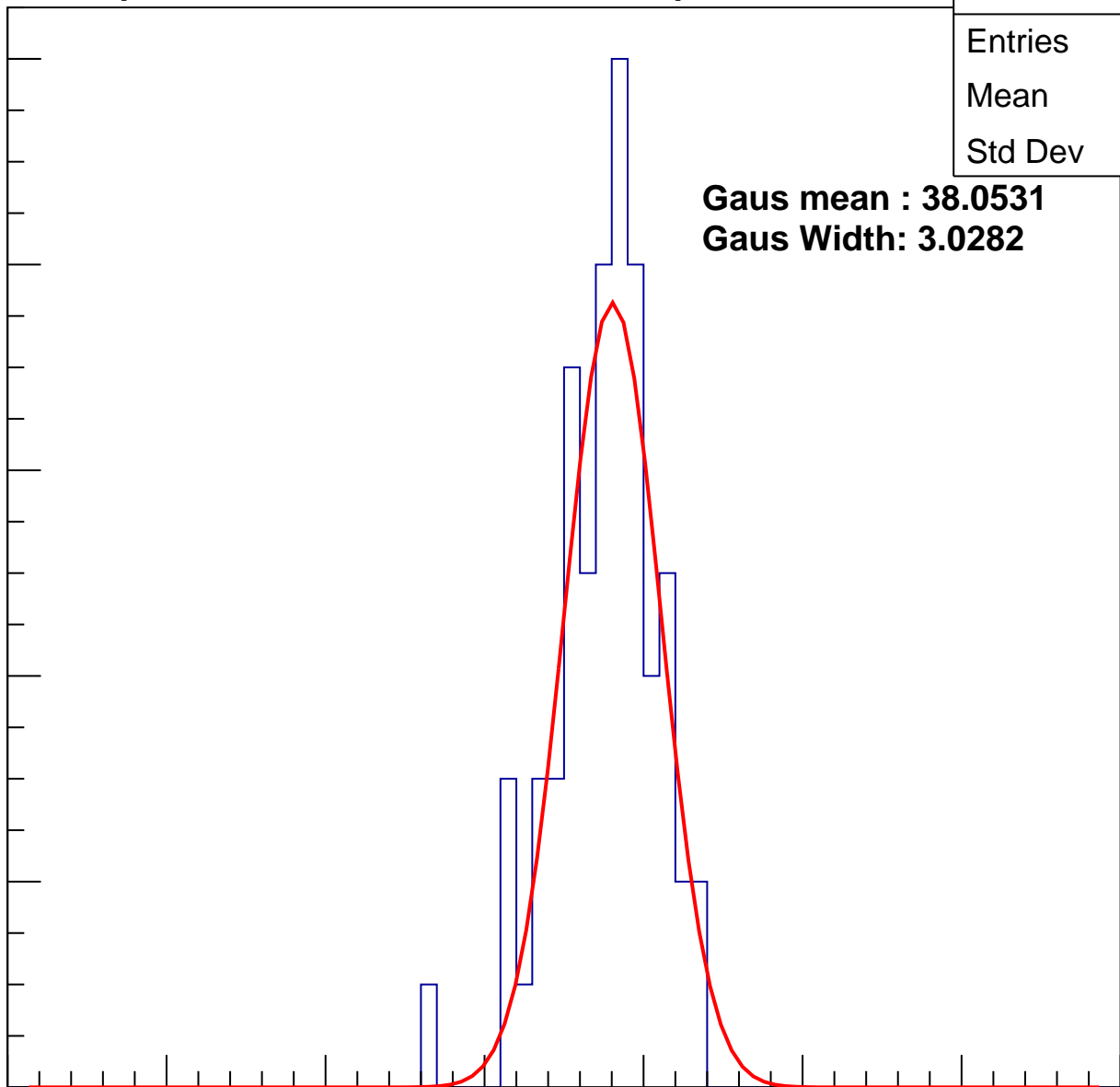
**Gaus Width: 3.0282**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U17-ch122, adc2

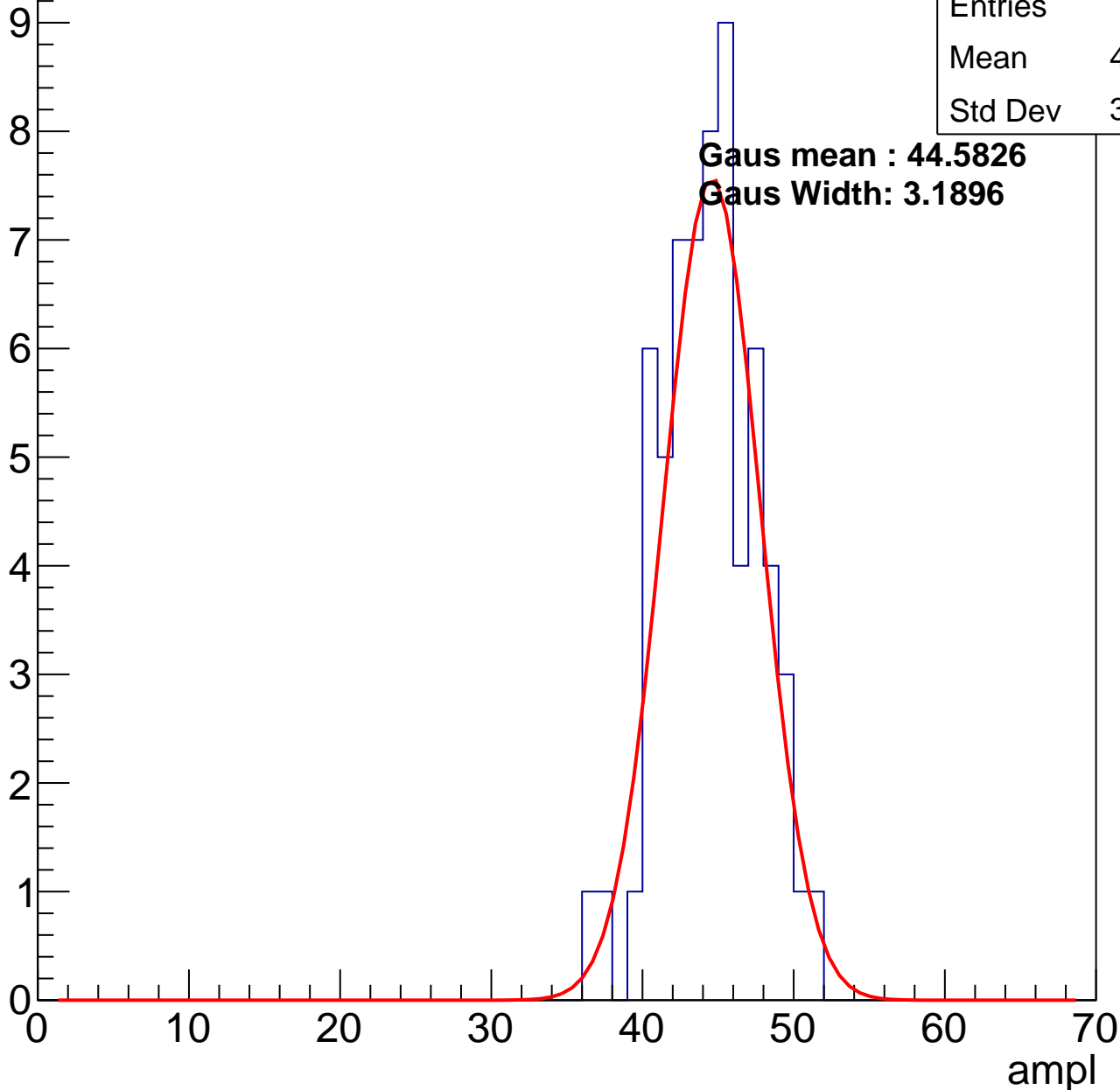
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	43.98
Std Dev	3.105

**Gaus mean : 44.5826**

**Gaus Width: 3.1896**

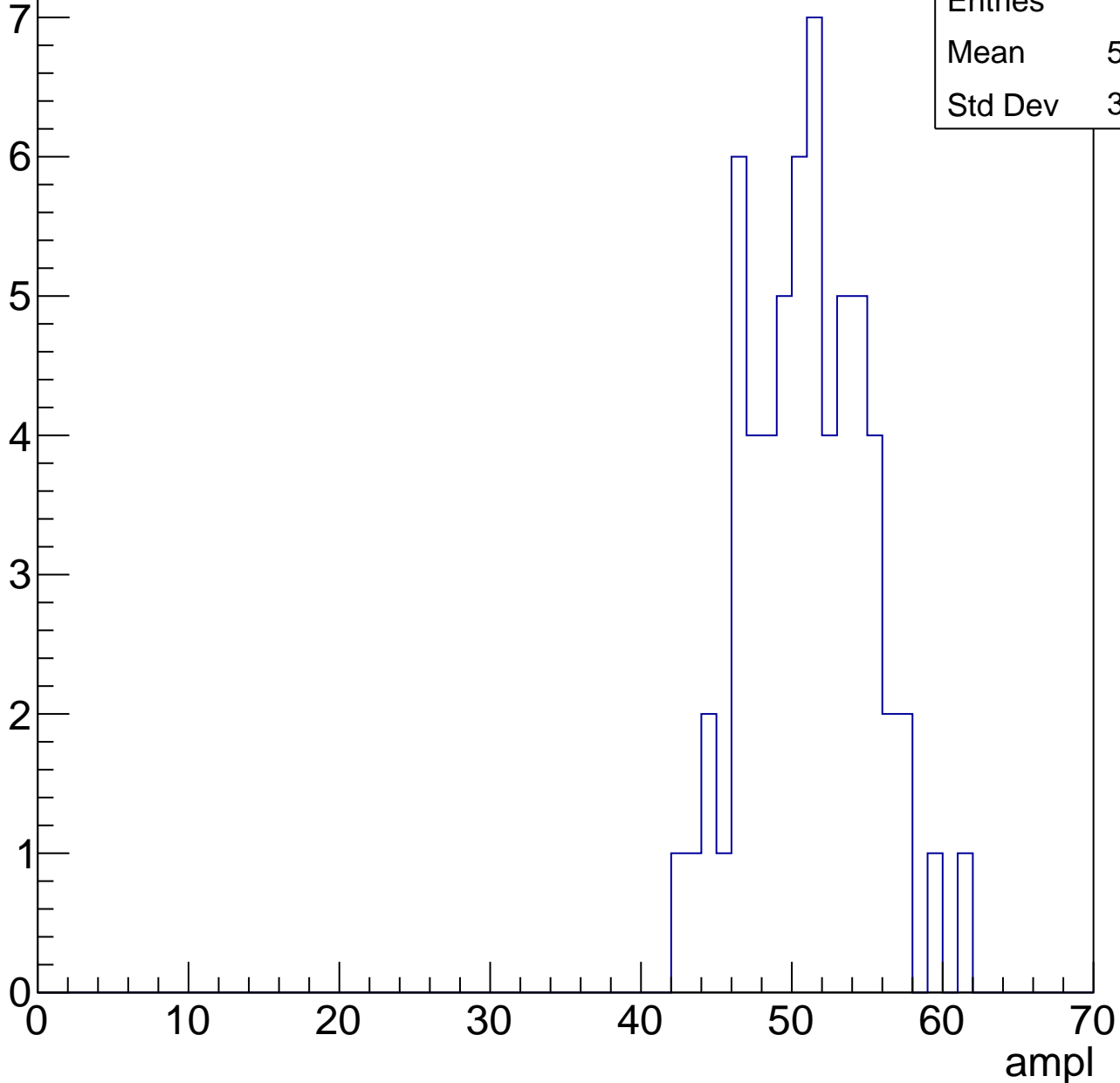


# B0L001S, U17-ch122, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	50.57
Std Dev	3.973

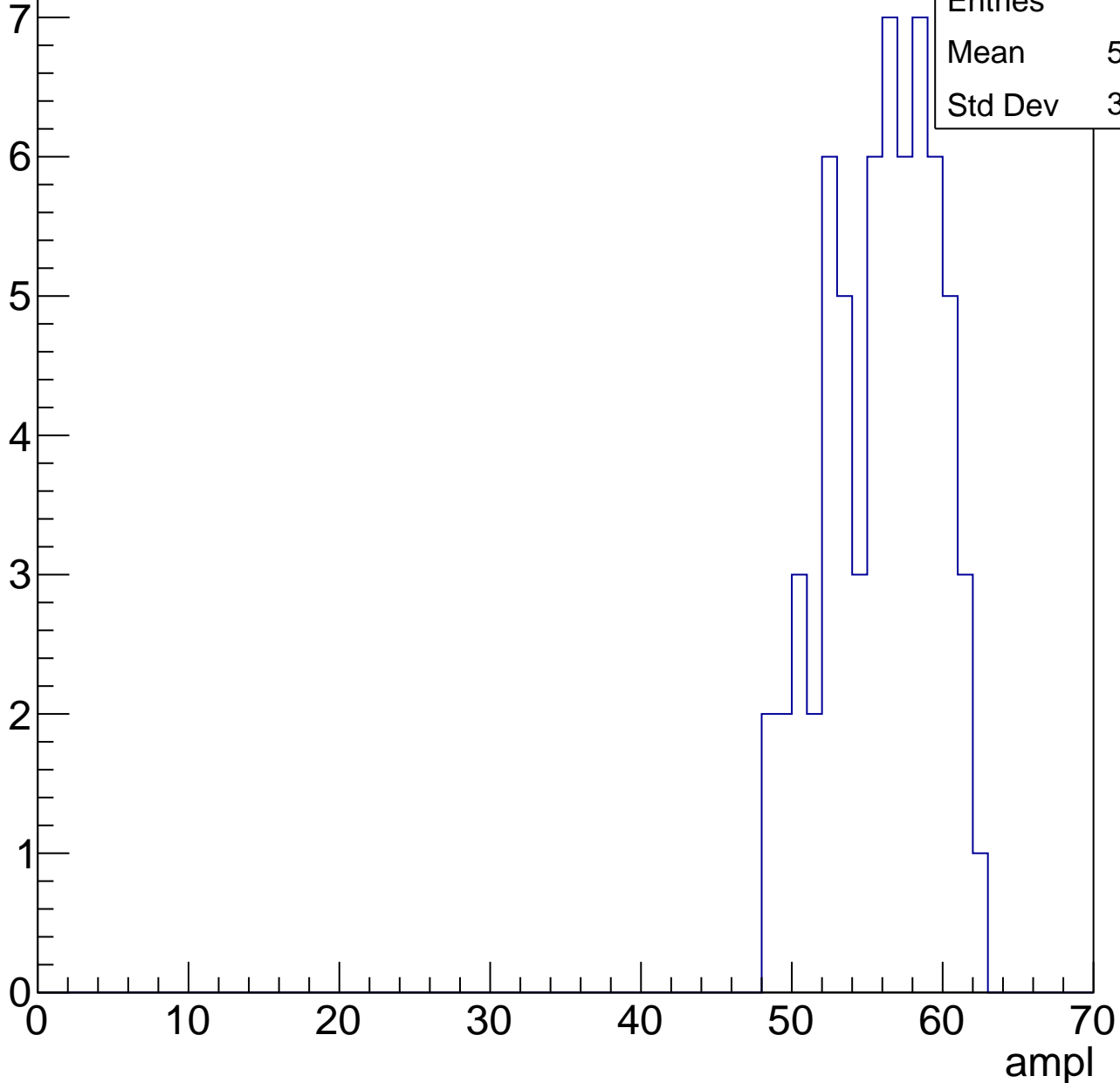


# B0L001S, U17-ch122, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	55.53
Std Dev	3.553

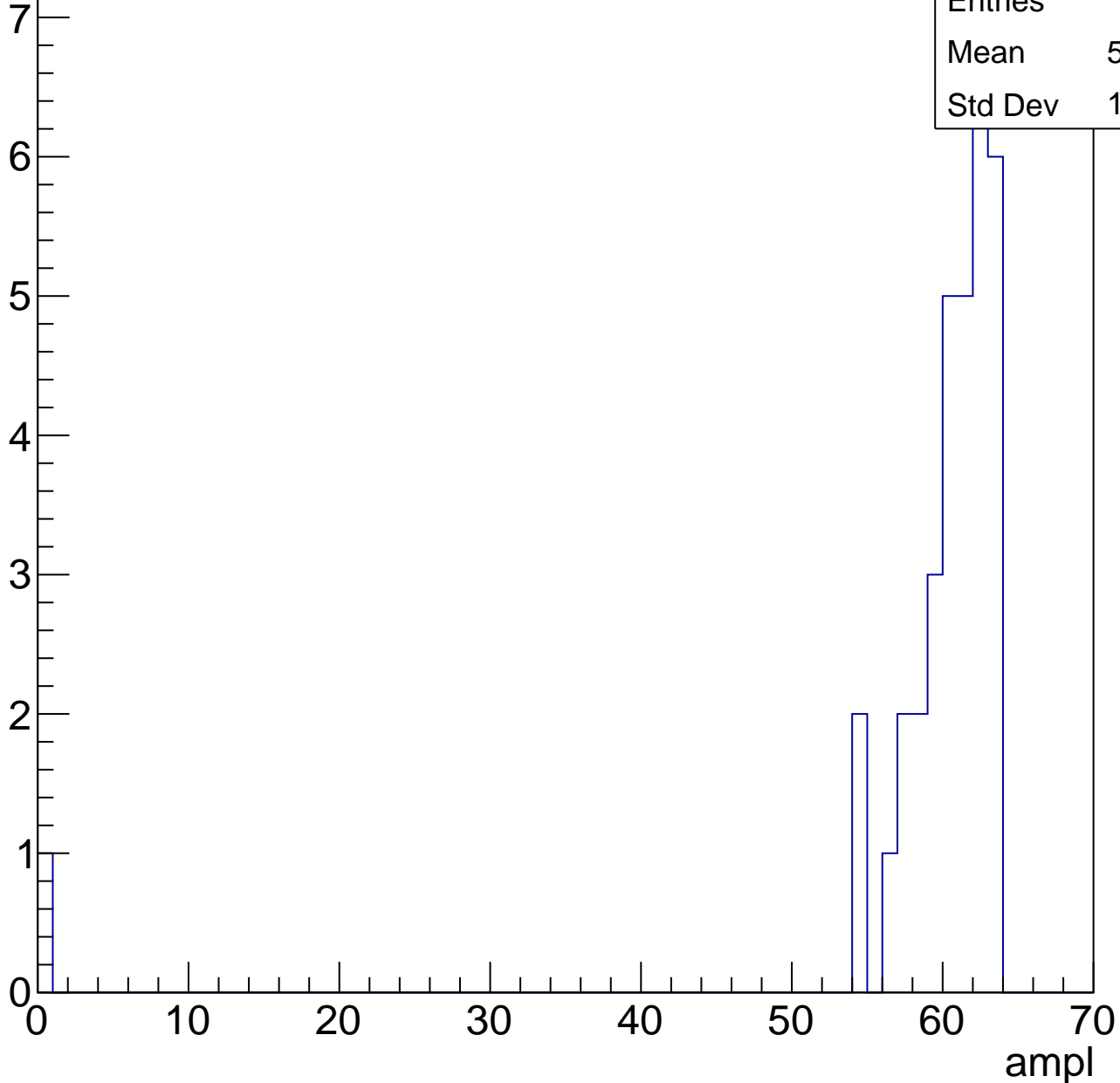


# B0L001S, U17-ch122, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

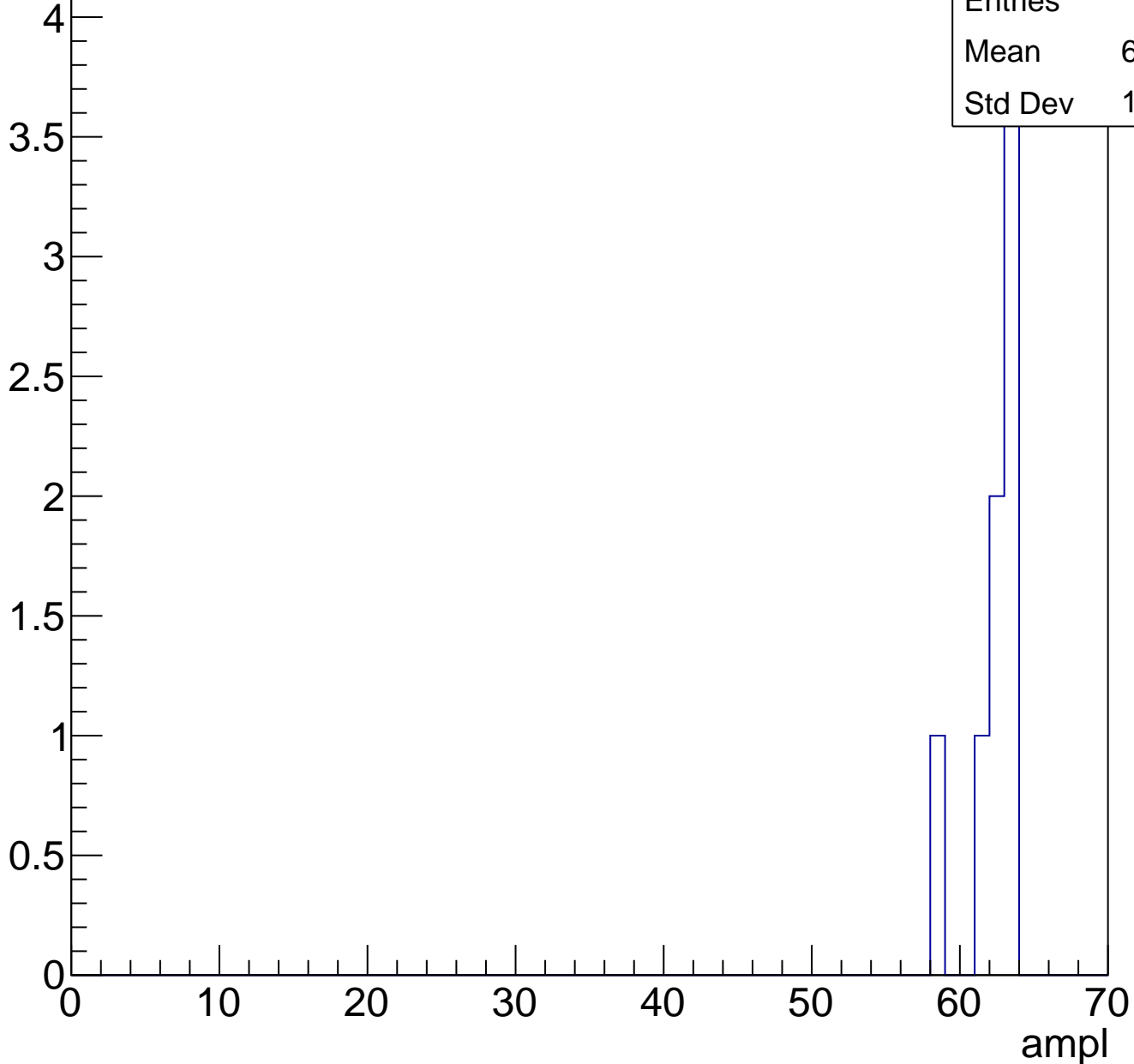
Entries	34
Mean	58.47
Std Dev	10.47



# B0L001S, U17-ch122, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch122, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	22
Std Dev	0

# B0L001S, U17-ch123, adc0

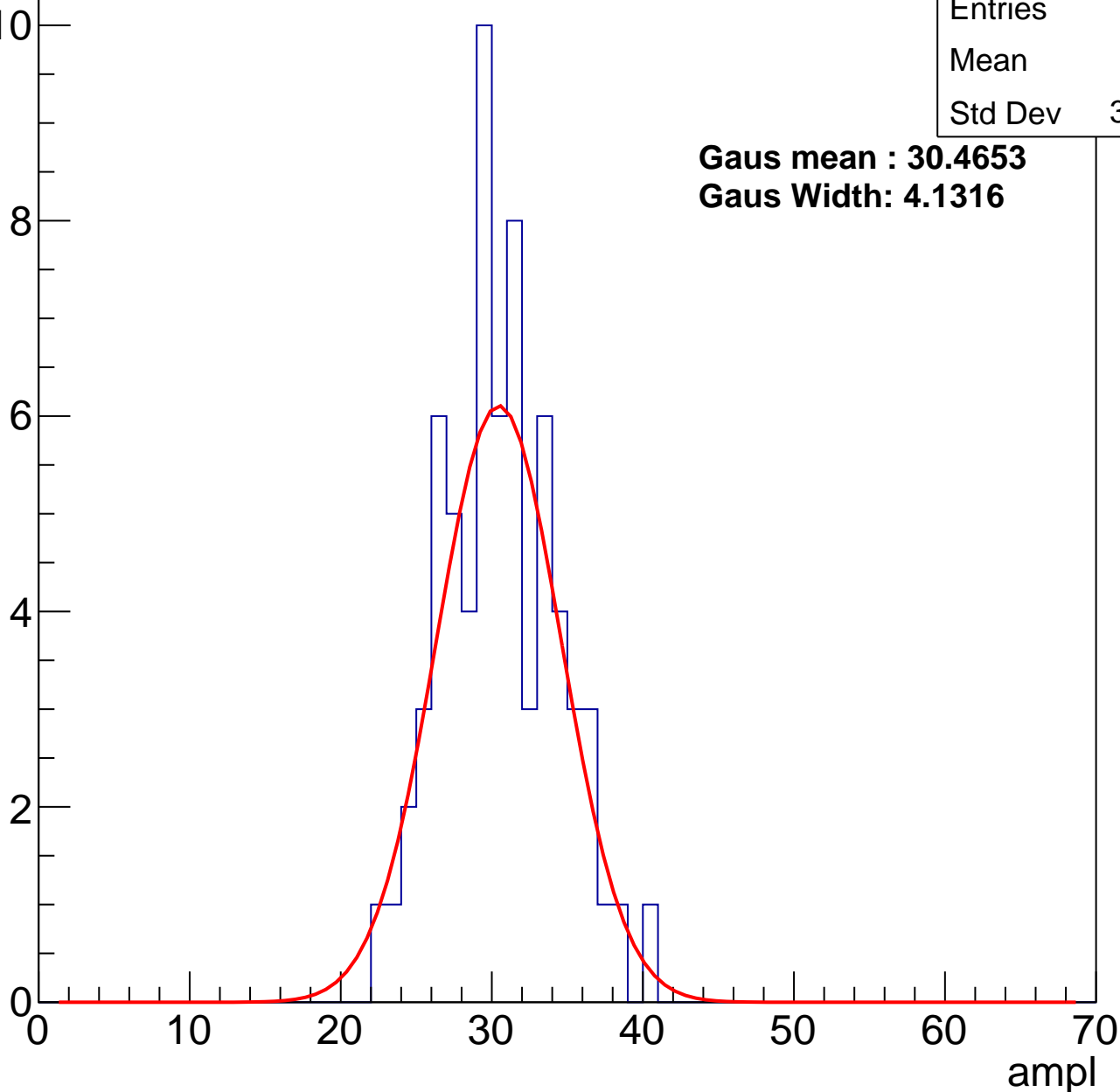
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	30.1
Std Dev	3.758

**Gaus mean : 30.4653**

**Gaus Width: 4.1316**



# B0L001S, U17-ch123, adc1

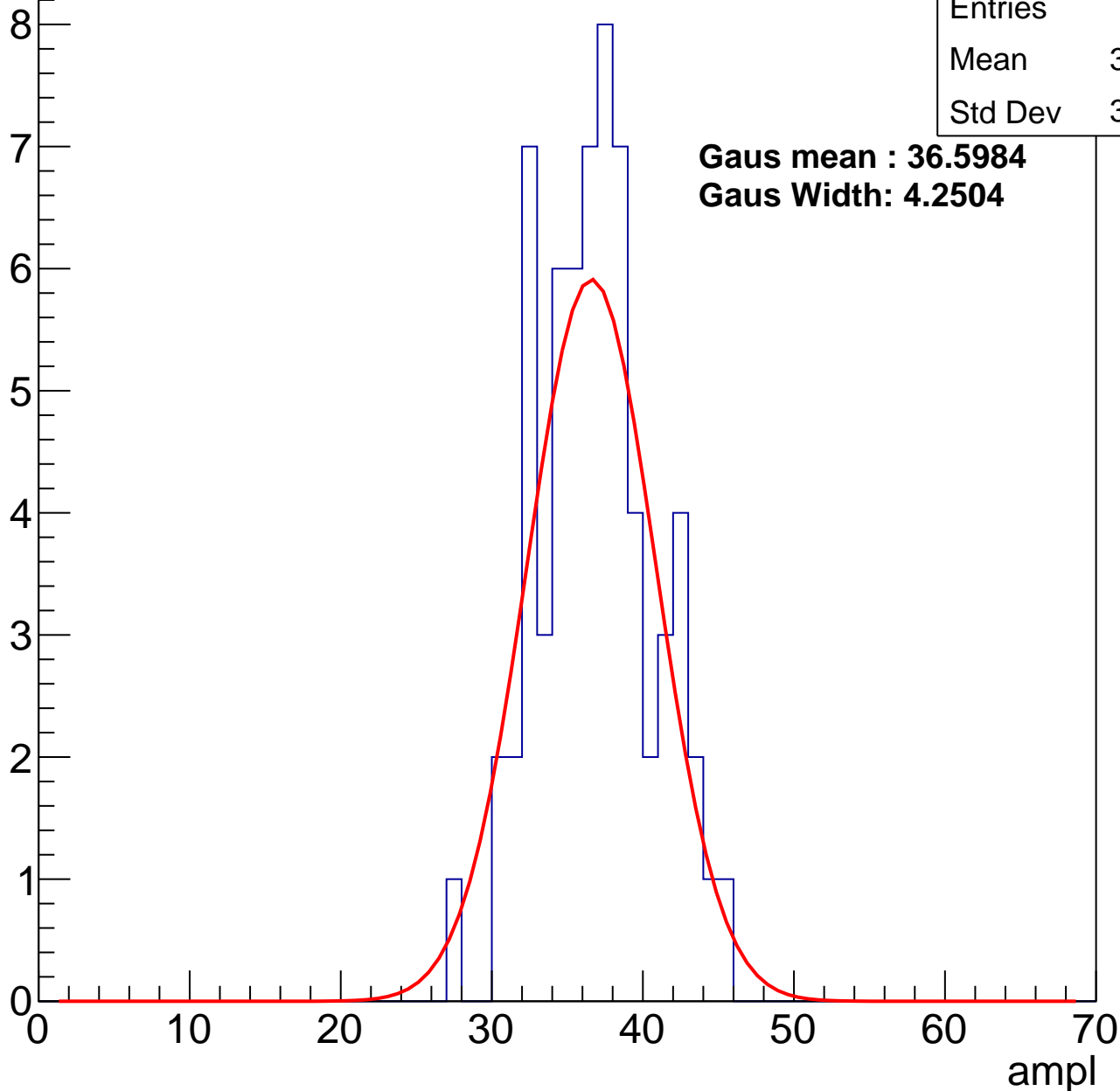
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	36.39
Std Dev	3.749

**Gaus mean : 36.5984**

**Gaus Width: 4.2504**



# B0L001S, U17-ch123, adc2

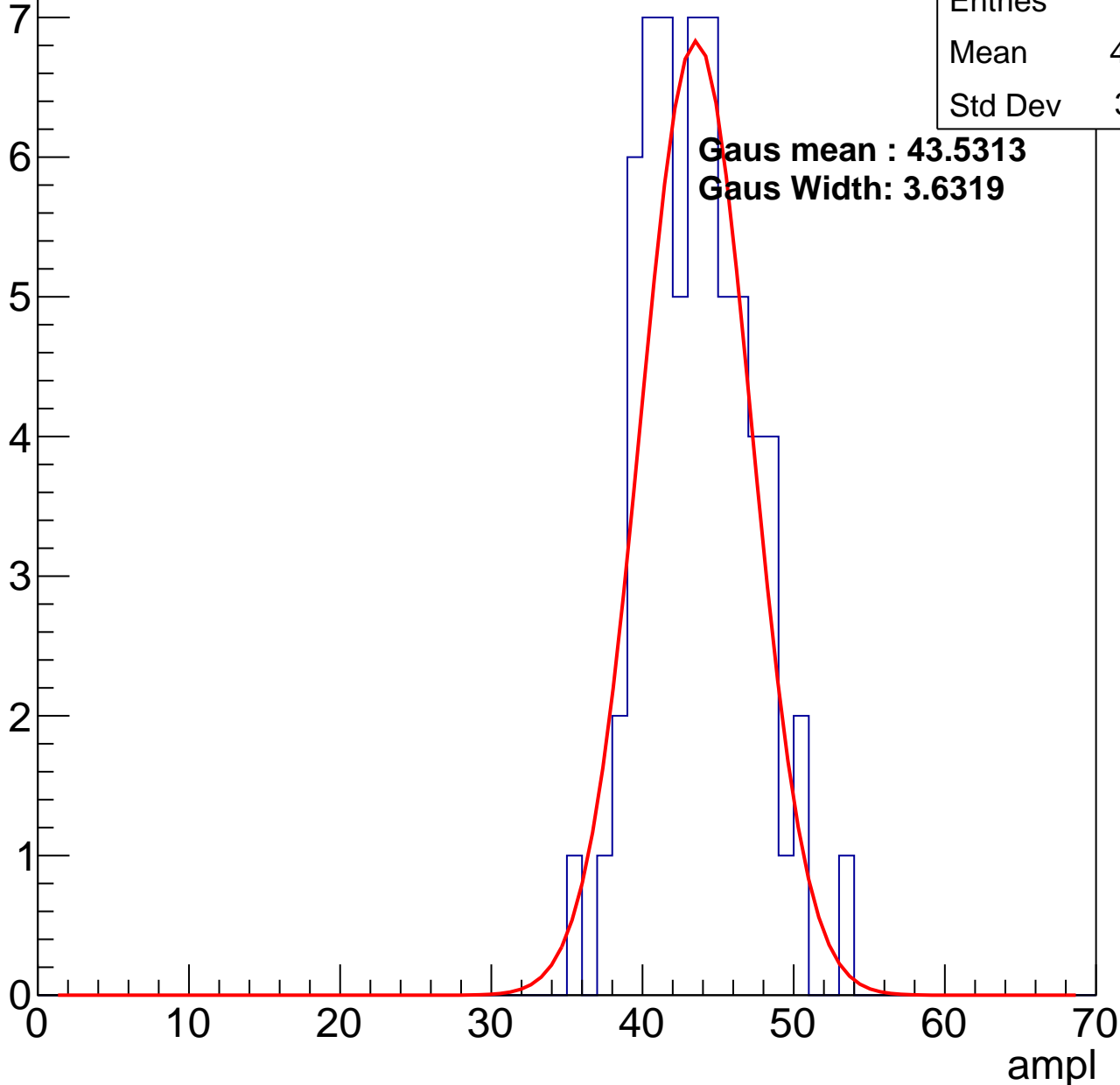
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	43.15
Std Dev	3.531

**Gaus mean : 43.5313**

**Gaus Width: 3.6319**

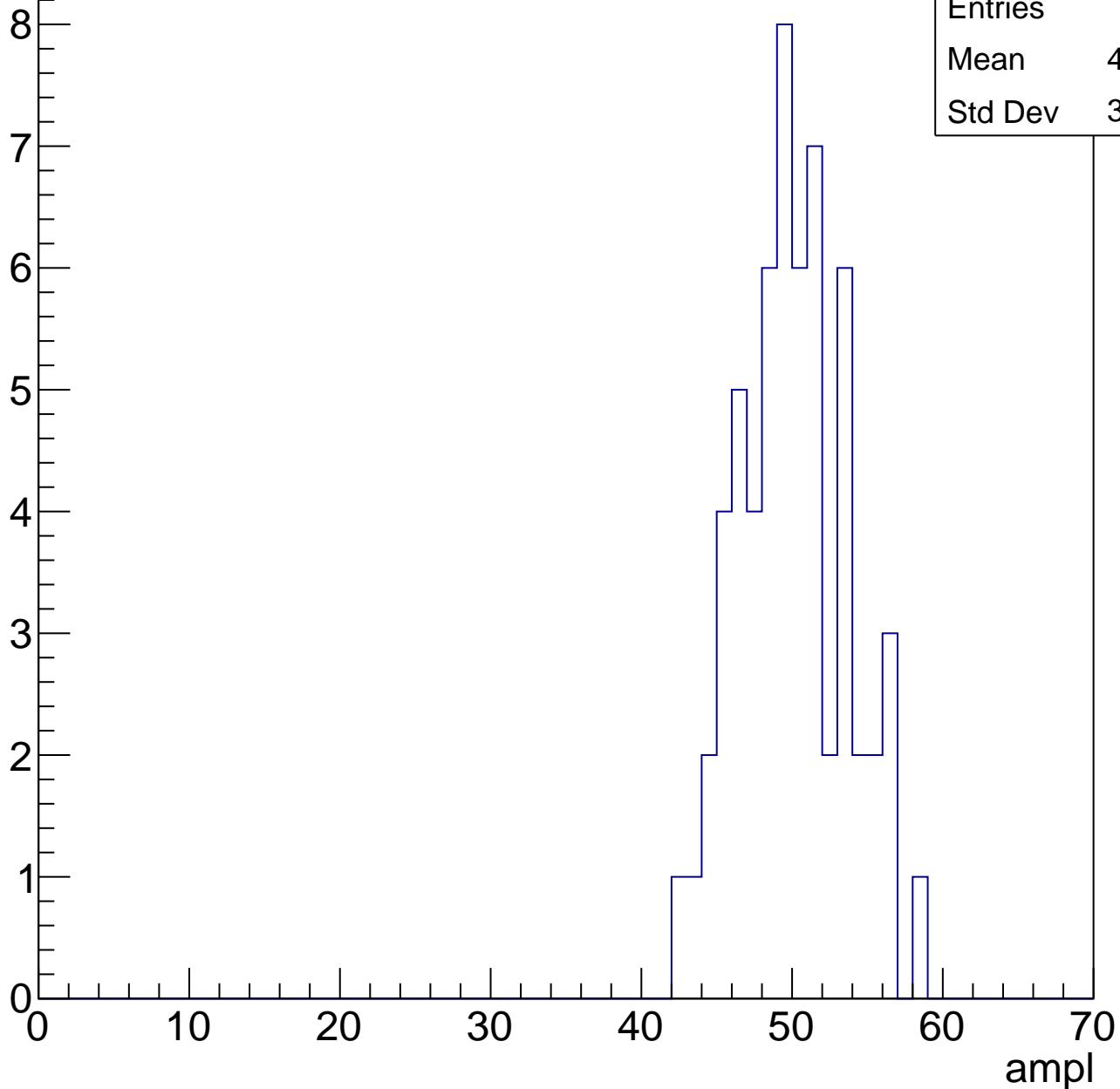


# B0L001S, U17-ch123, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	49.57
Std Dev	3.523

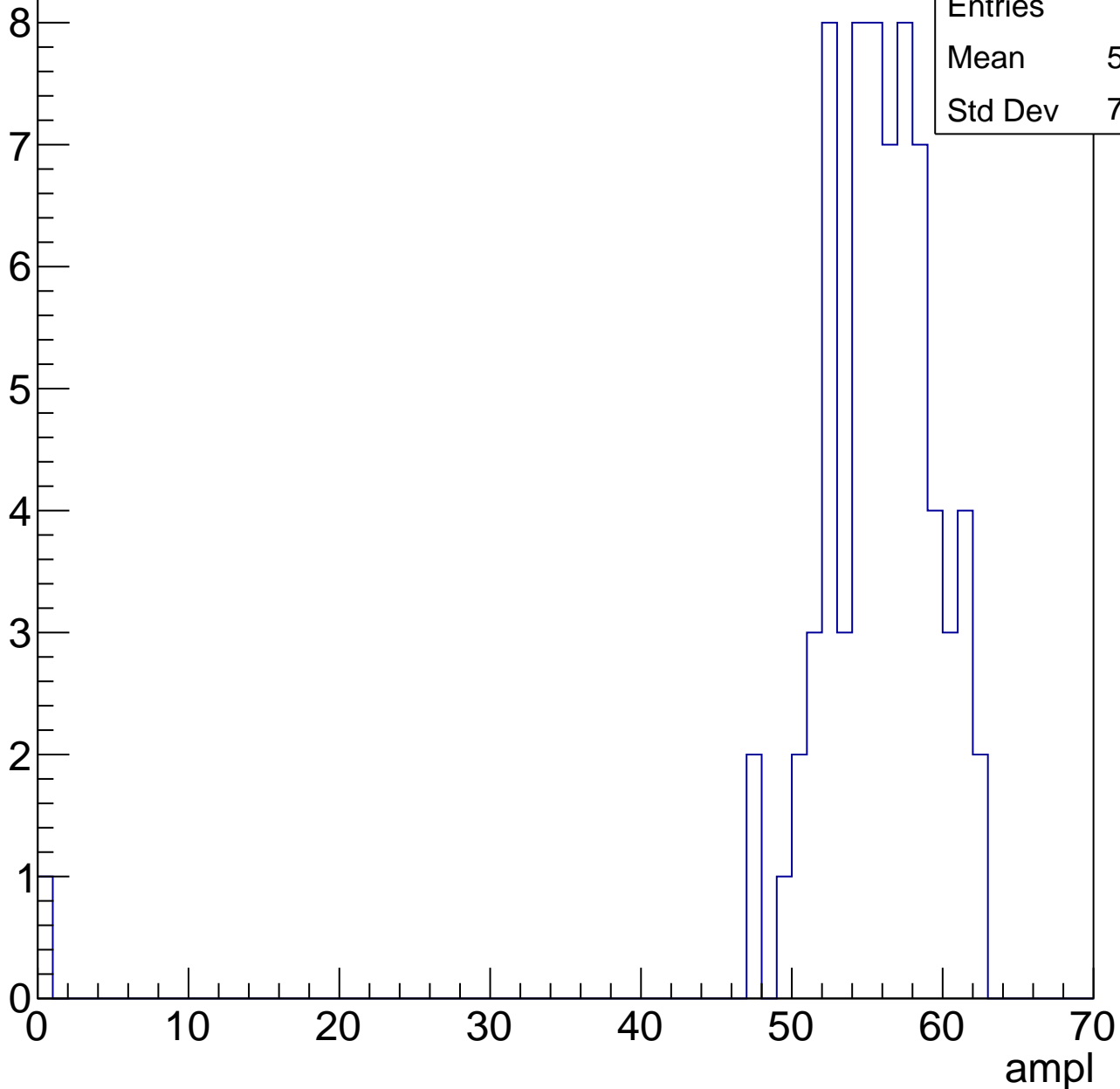


# B0L001S, U17-ch123, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

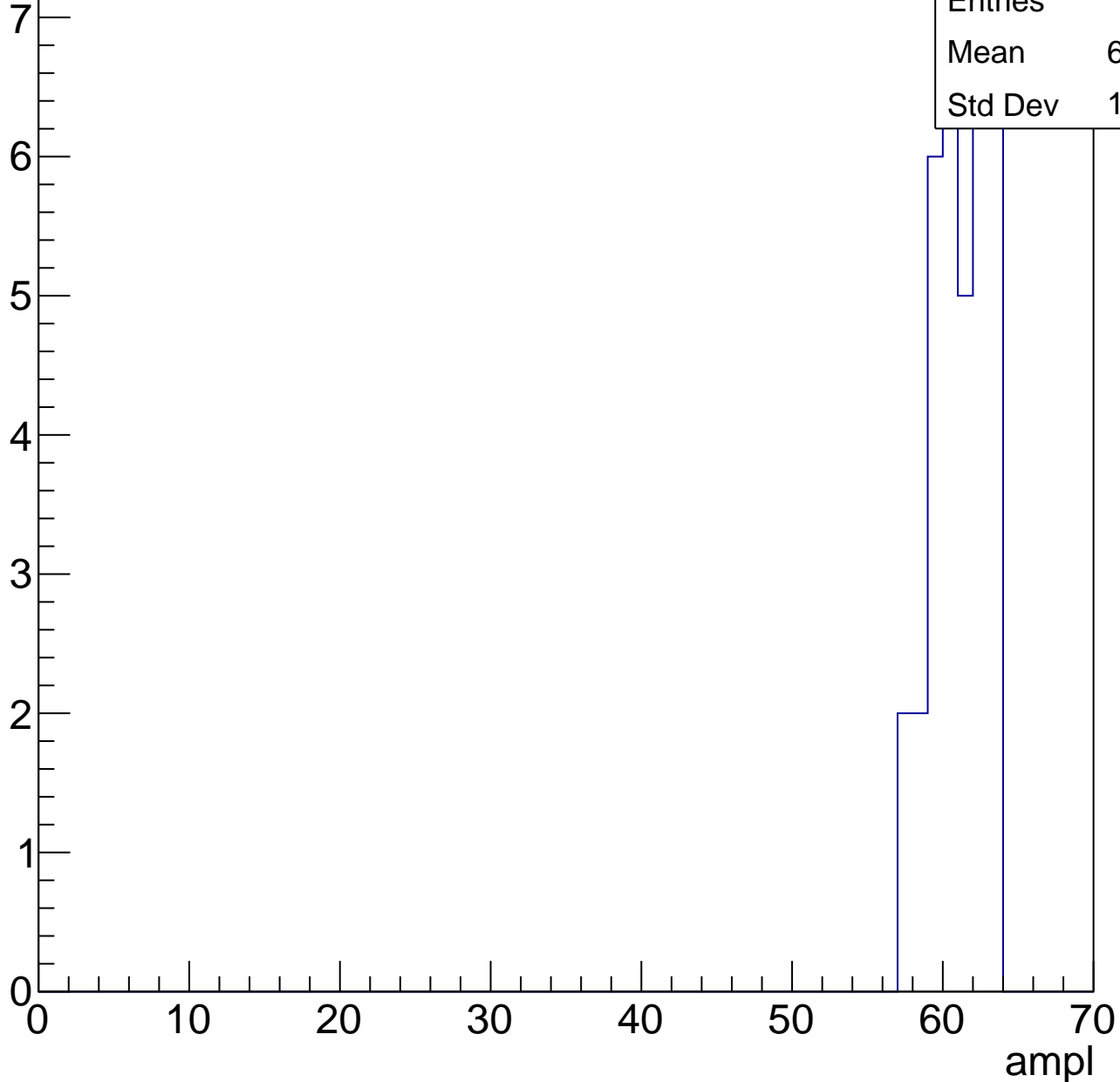
Entries	71
Mean	54.66
Std Dev	7.368



# B0L001S, U17-ch123, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

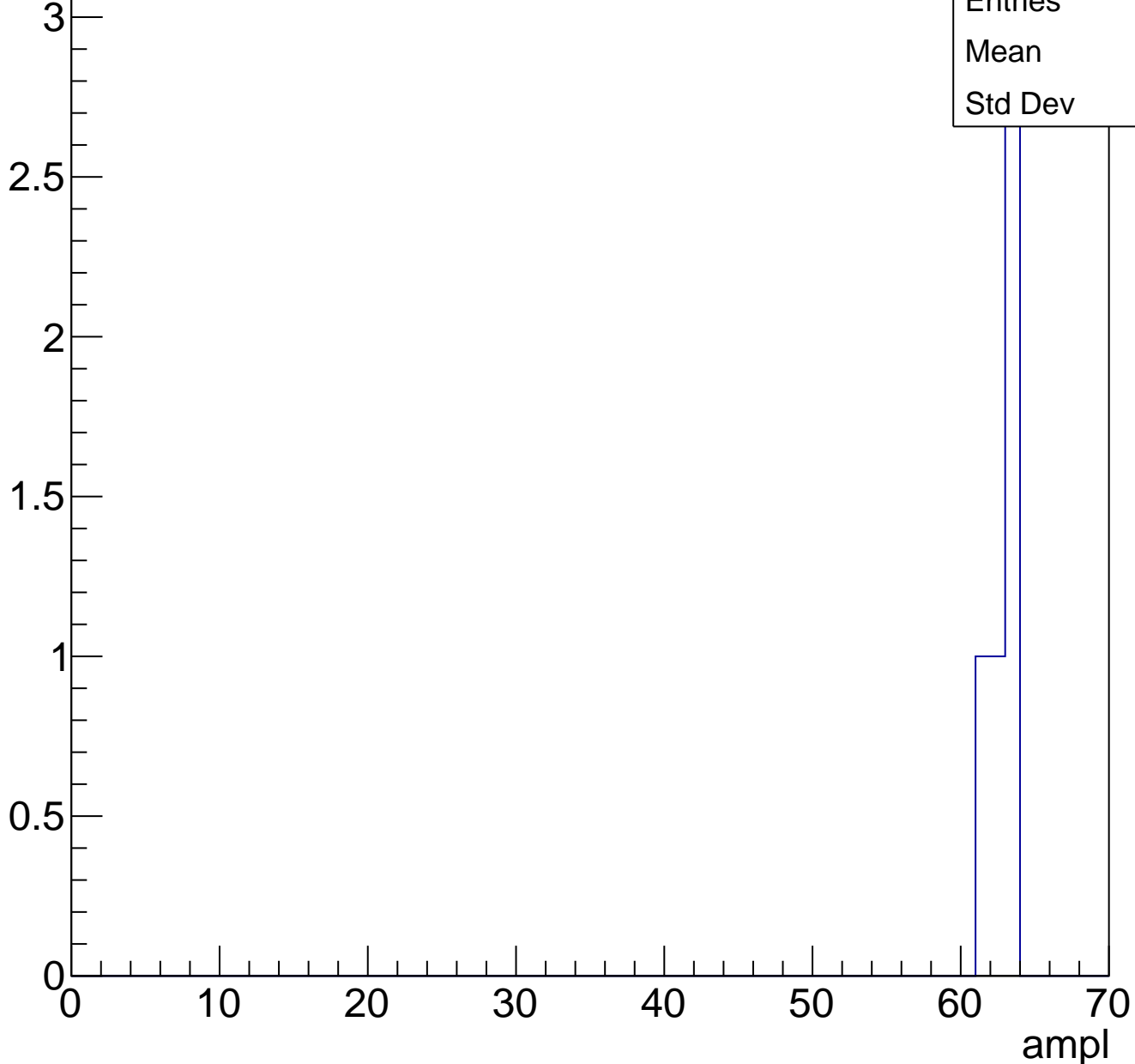


Entries	36
Mean	60.67
Std Dev	1.764

# B0L001S, U17-ch123, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	5
Mean	62.4
Std Dev	0.8



# B0L001S, U17-ch123, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U17-ch124, adc0

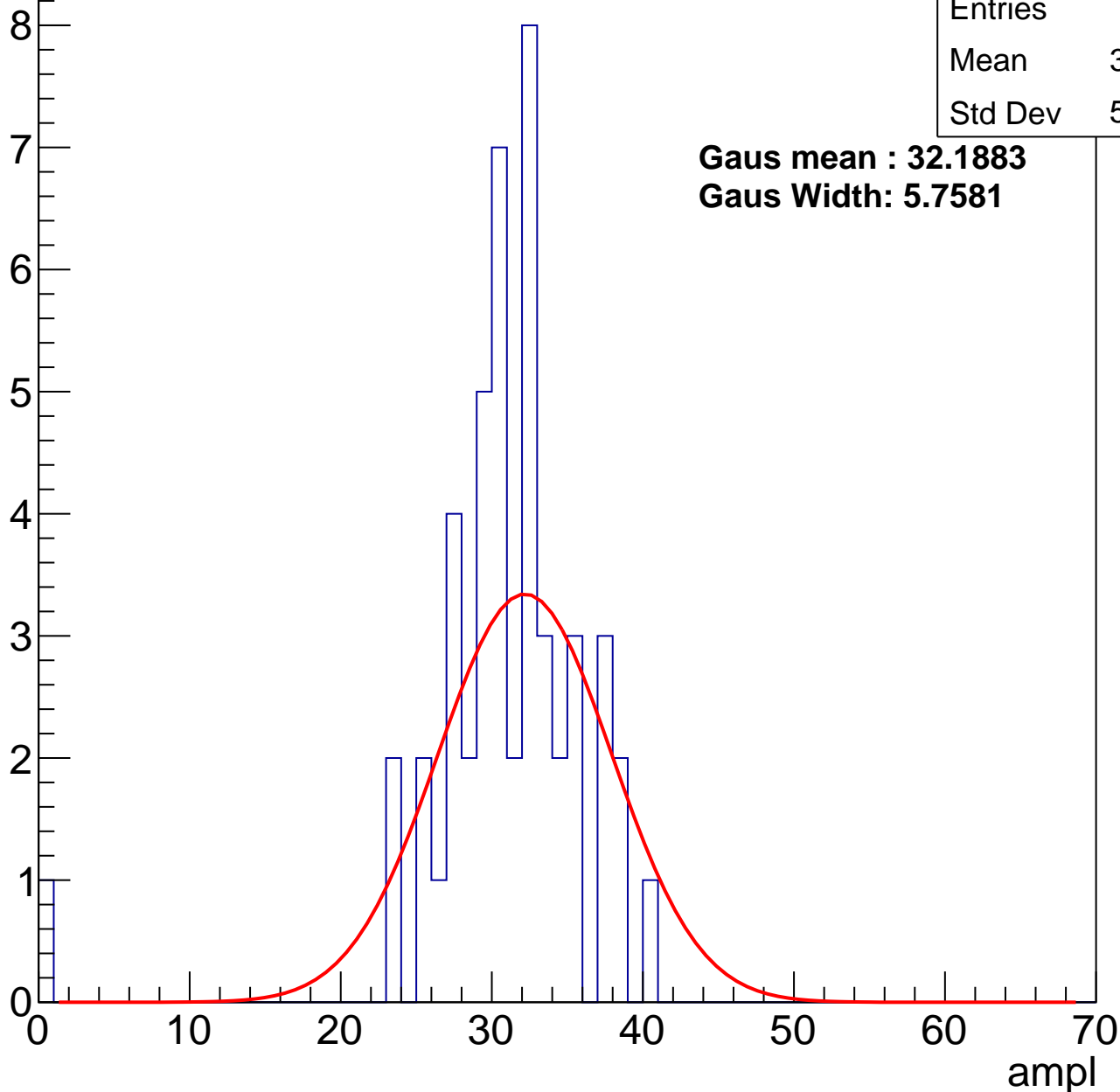
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	48
Mean	30.38
Std Dev	5.862

**Gaus mean : 32.1883**

**Gaus Width: 5.7581**



# B0L001S, U17-ch124, adc1

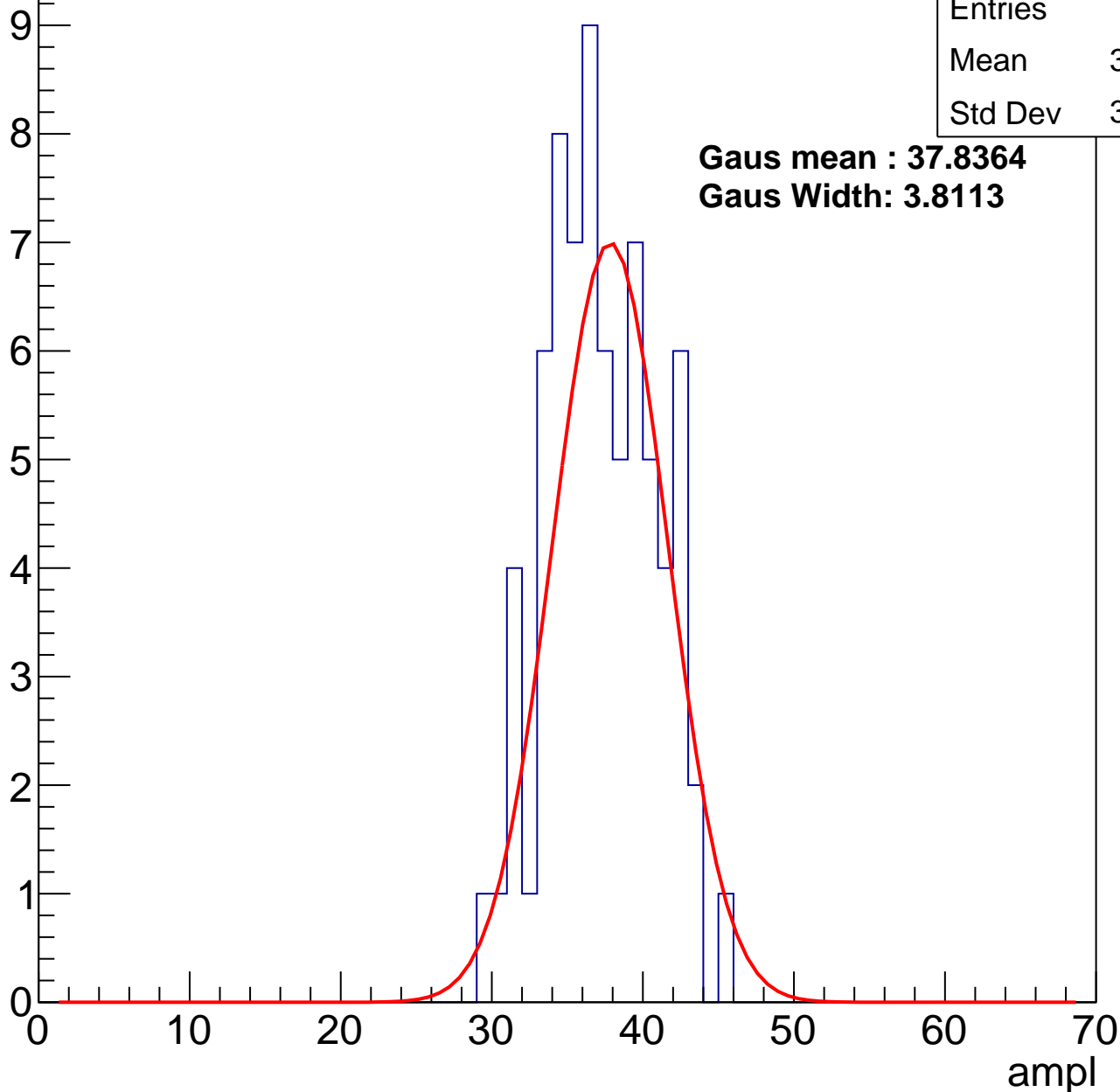
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	36.79
Std Dev	3.534

**Gaus mean : 37.8364**

**Gaus Width: 3.8113**



# B0L001S, U17-ch124, adc2

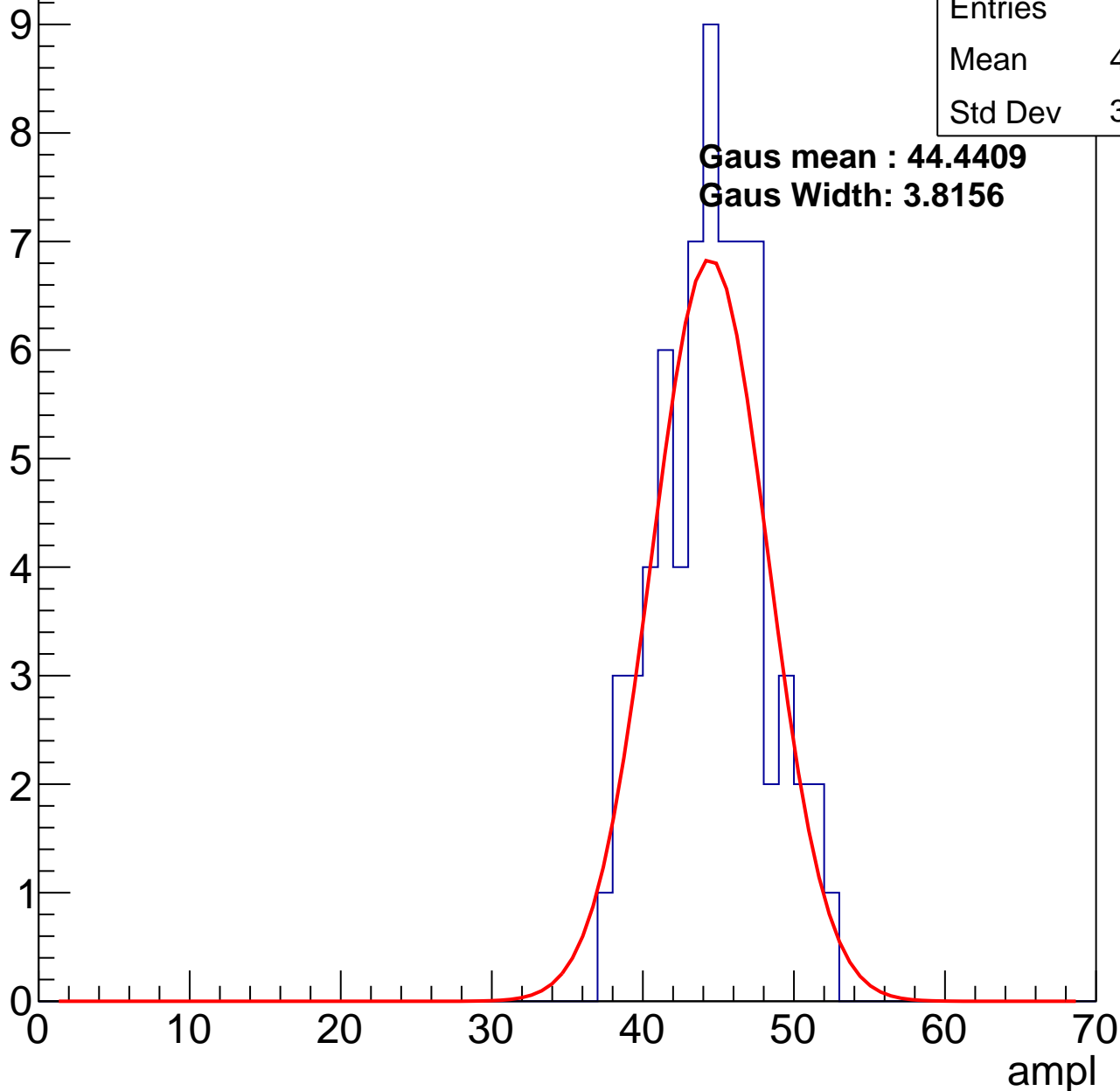
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	44.15
Std Dev	3.452

**Gaus mean : 44.4409**

**Gaus Width: 3.8156**

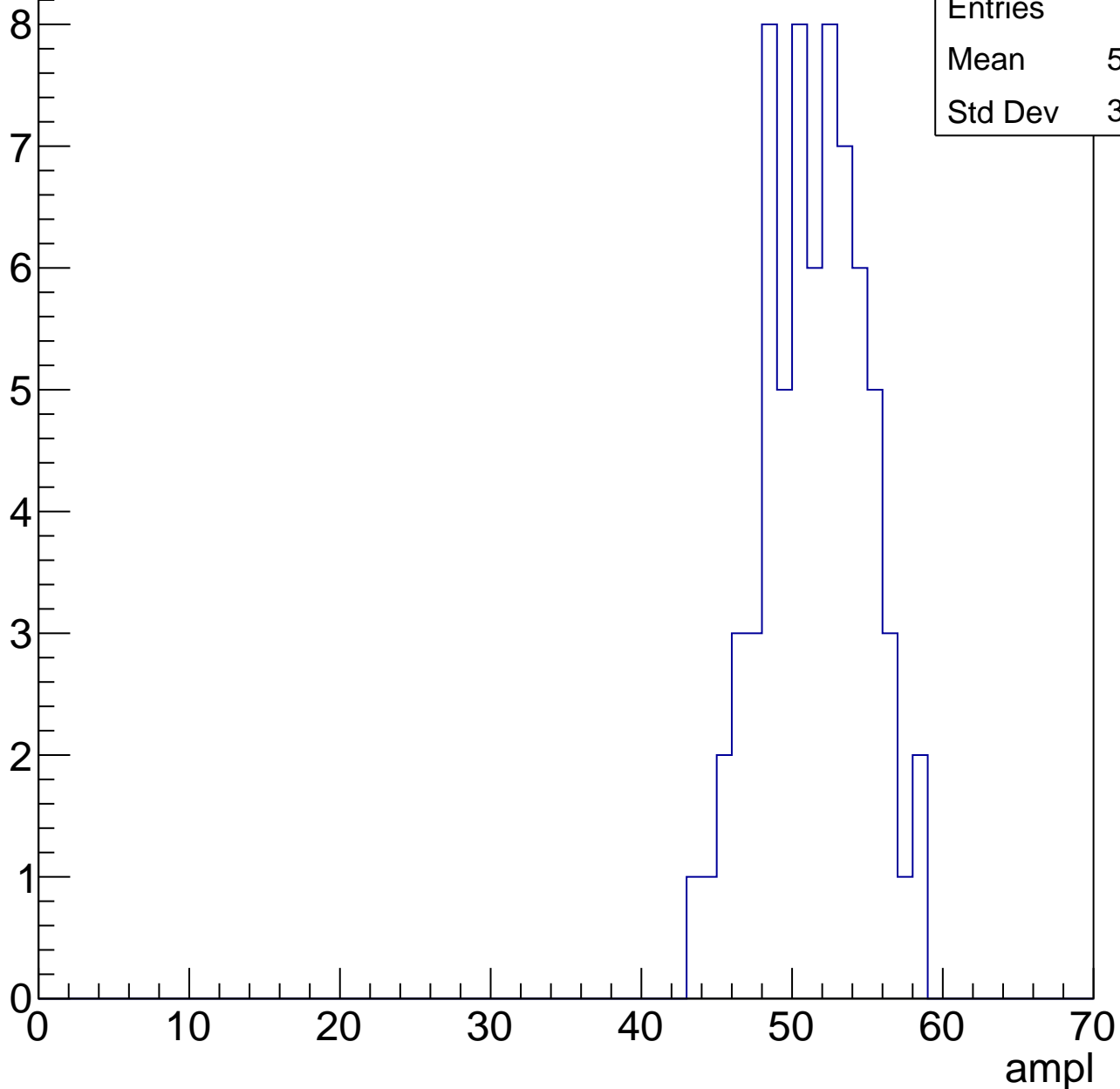


# B0L001S, U17-ch124, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	50.99
Std Dev	3.377

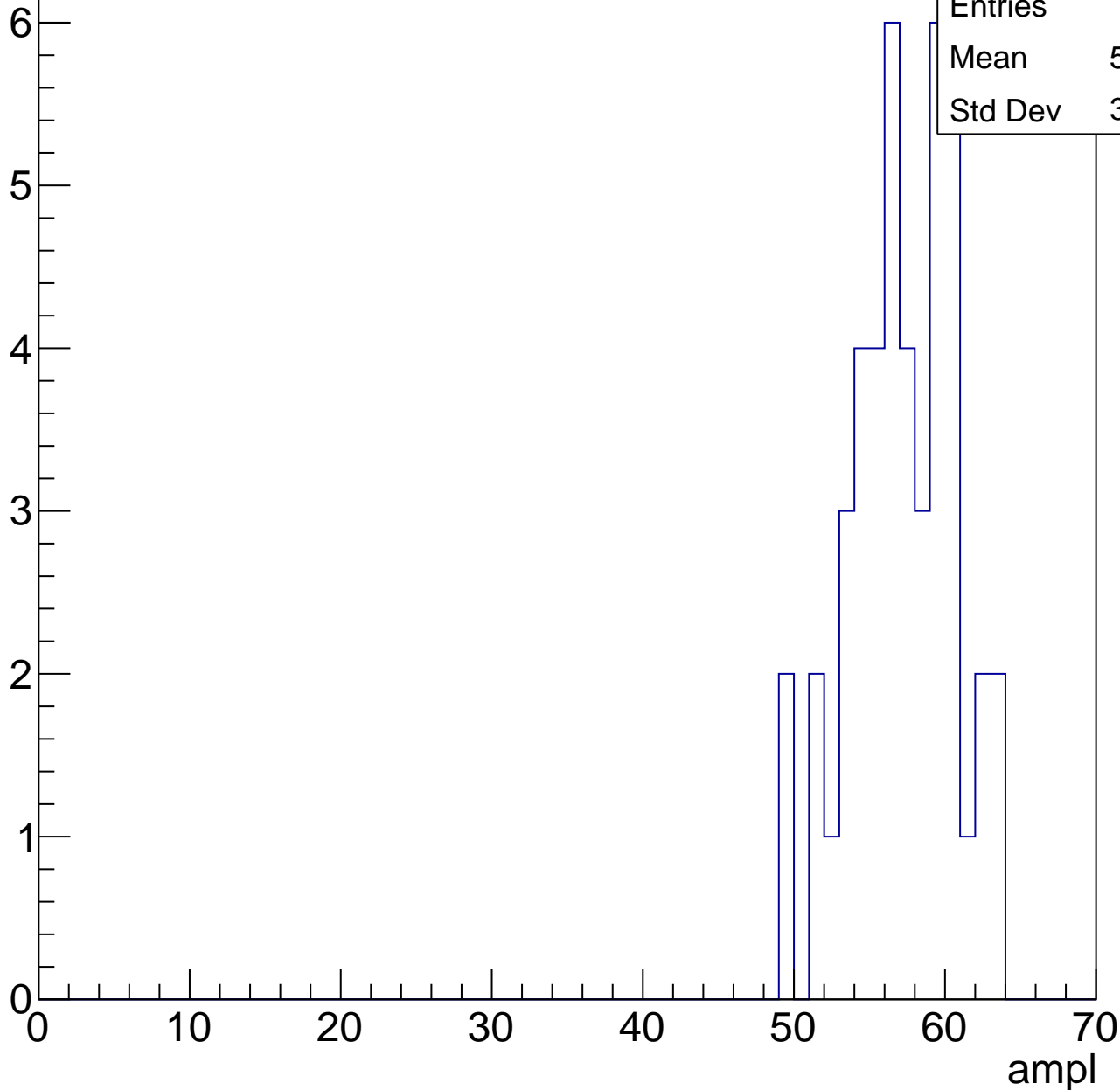


# B0L001S, U17-ch124, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	46
Mean	56.74
Std Dev	3.448

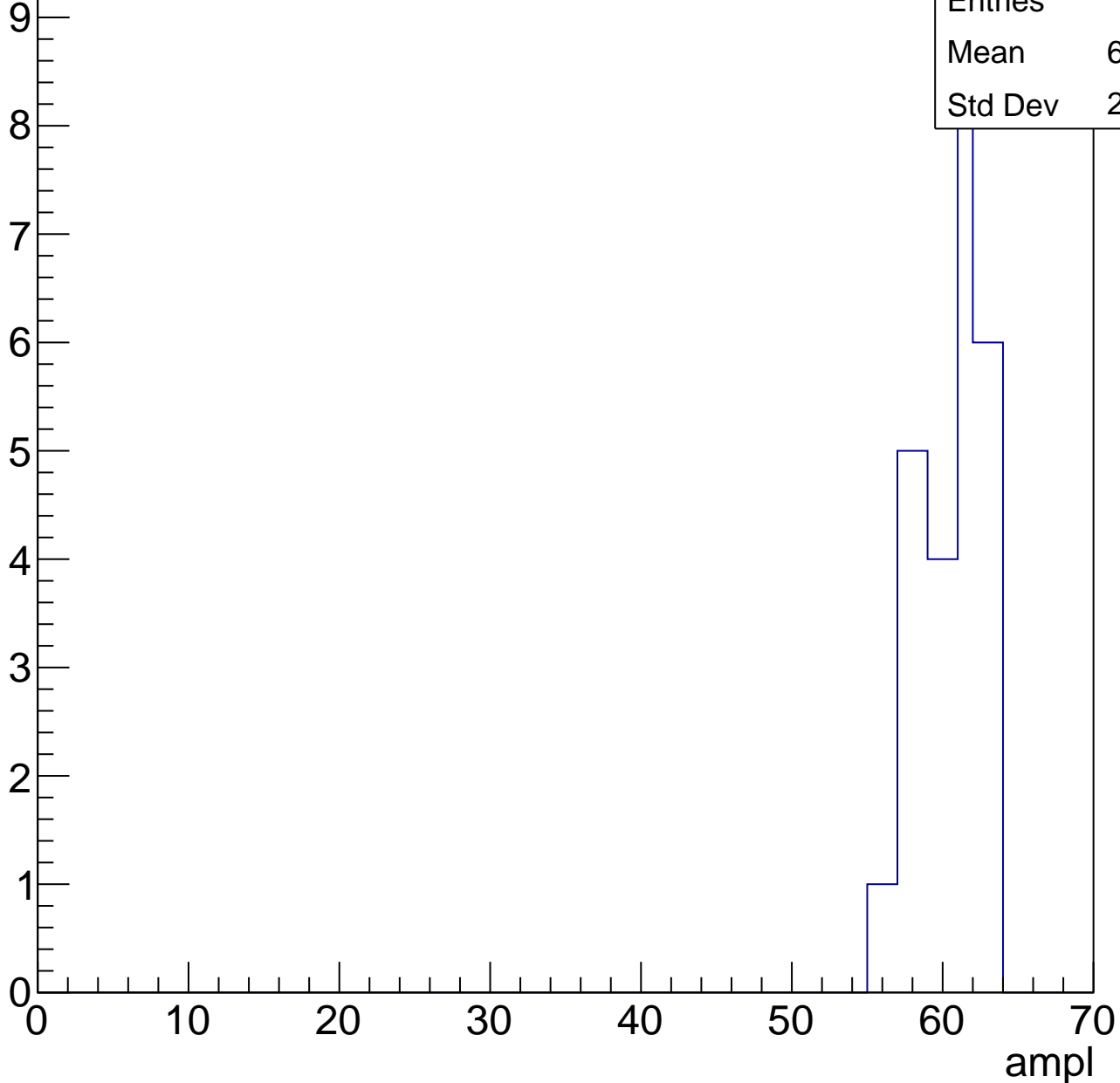


# B0L001S, U17-ch124, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

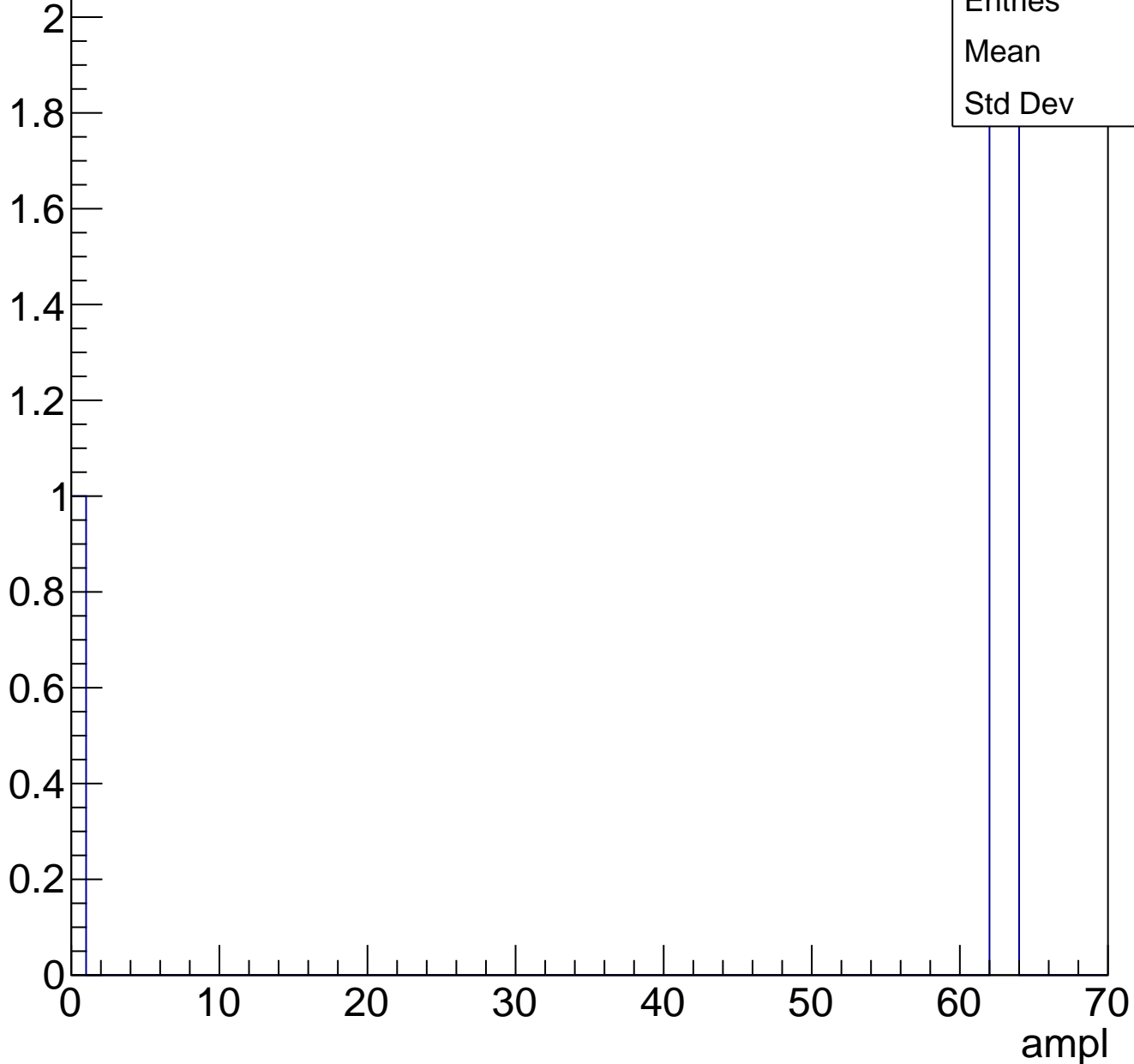
Entries	41
Mean	60.02
Std Dev	2.192



# B0L001S, U17-ch124, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch124, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U17-ch125, adc0

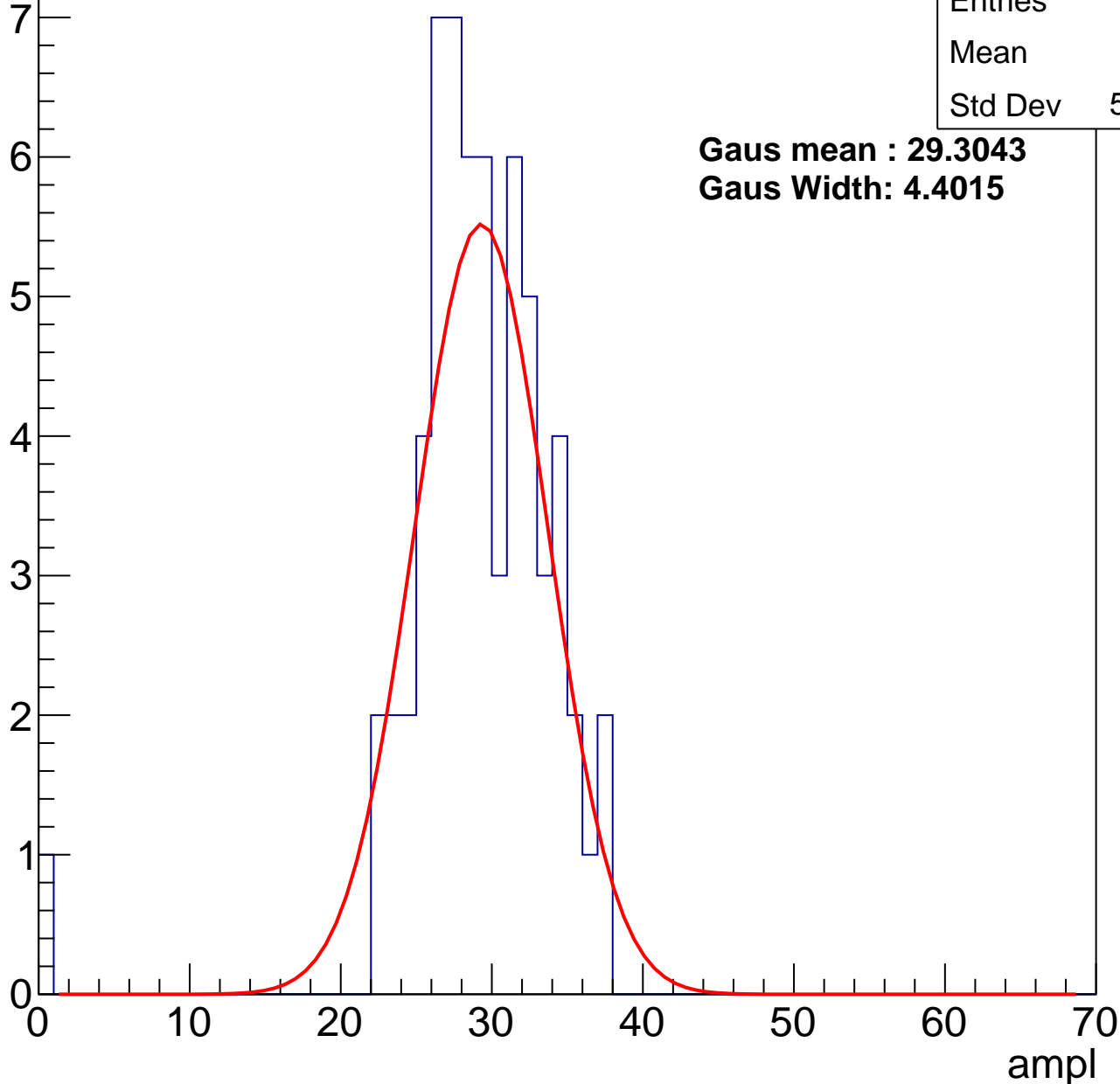
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	28.6
Std Dev	5.166

**Gaus mean : 29.3043**

**Gaus Width: 4.4015**



# B0L001S, U17-ch125, adc1

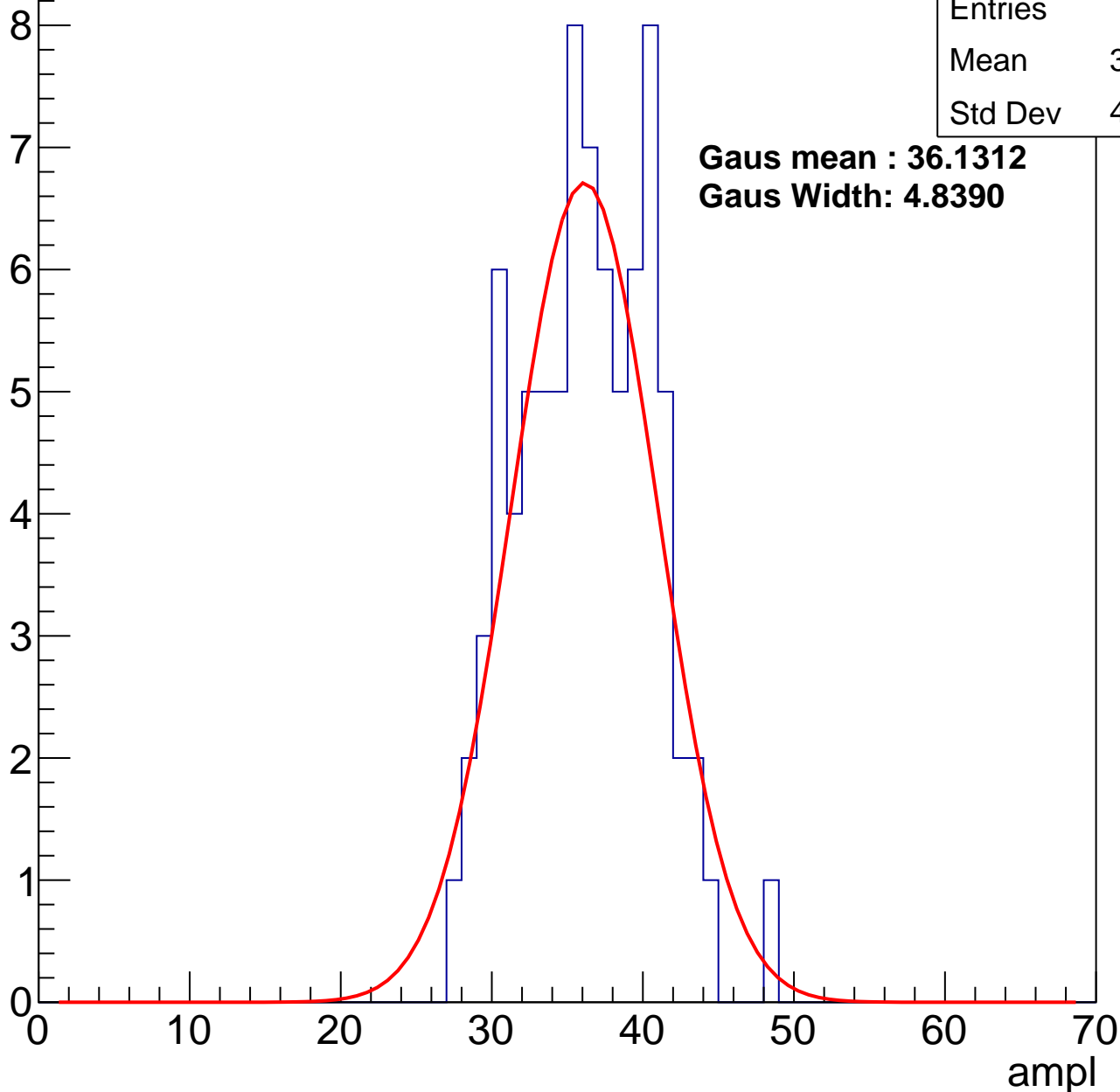
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	82
Mean	35.78
Std Dev	4.322

**Gaus mean : 36.1312**

**Gaus Width: 4.8390**



# B0L001S, U17-ch125, adc2

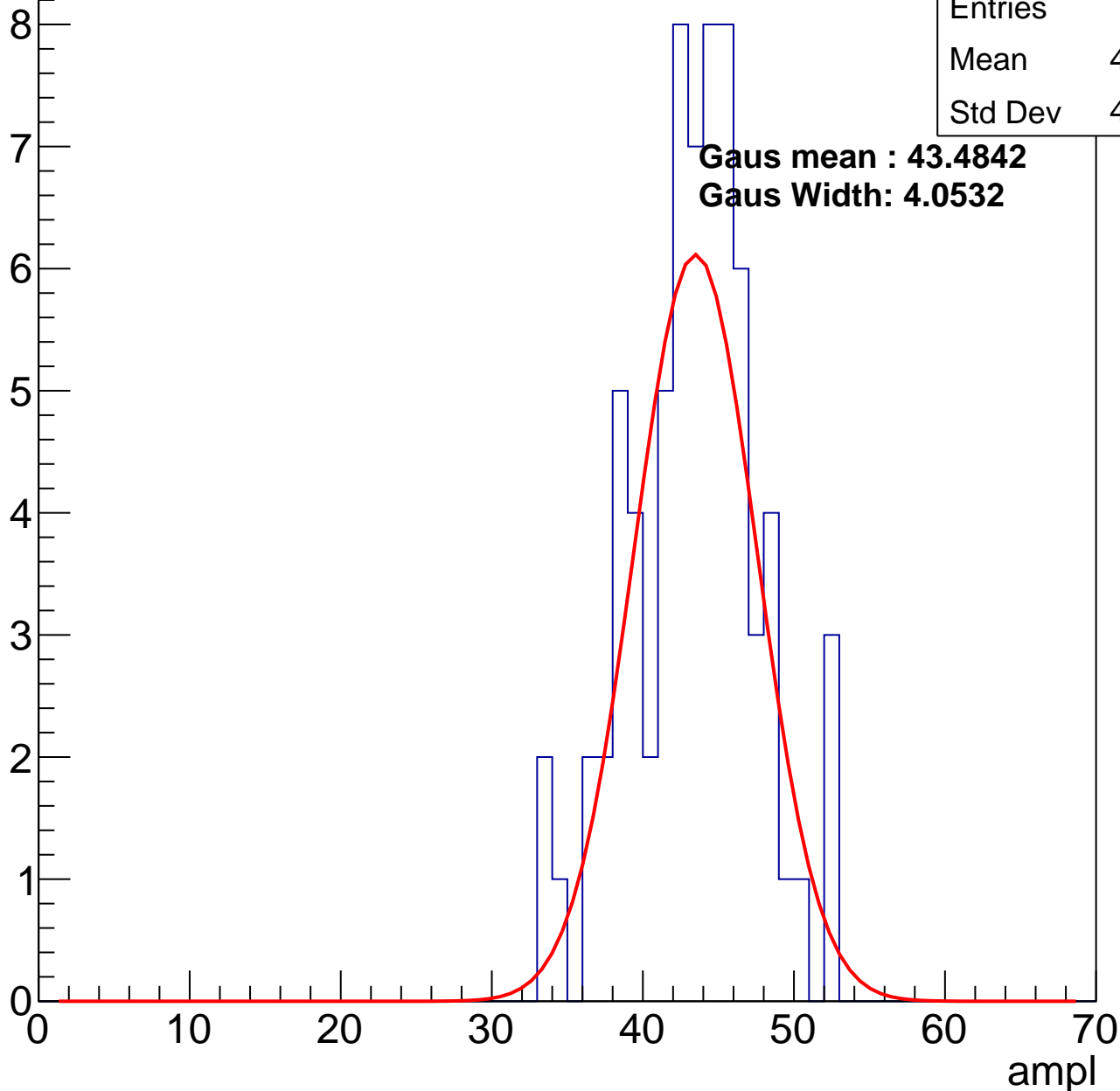
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	42.92
Std Dev	4.176

**Gaus mean : 43.4842**

**Gaus Width: 4.0532**

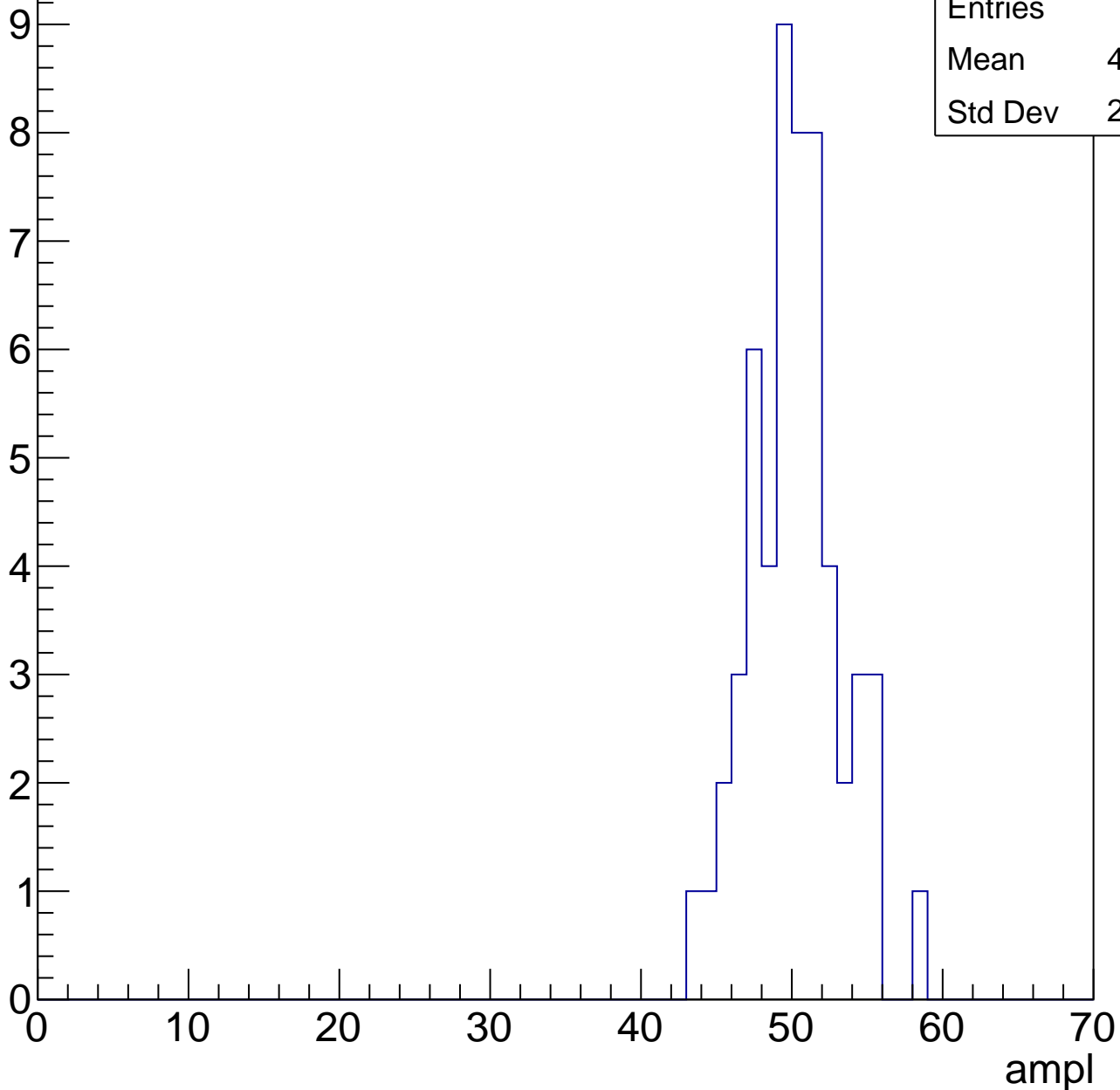


# B0L001S, U17-ch125, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	49.76
Std Dev	2.978

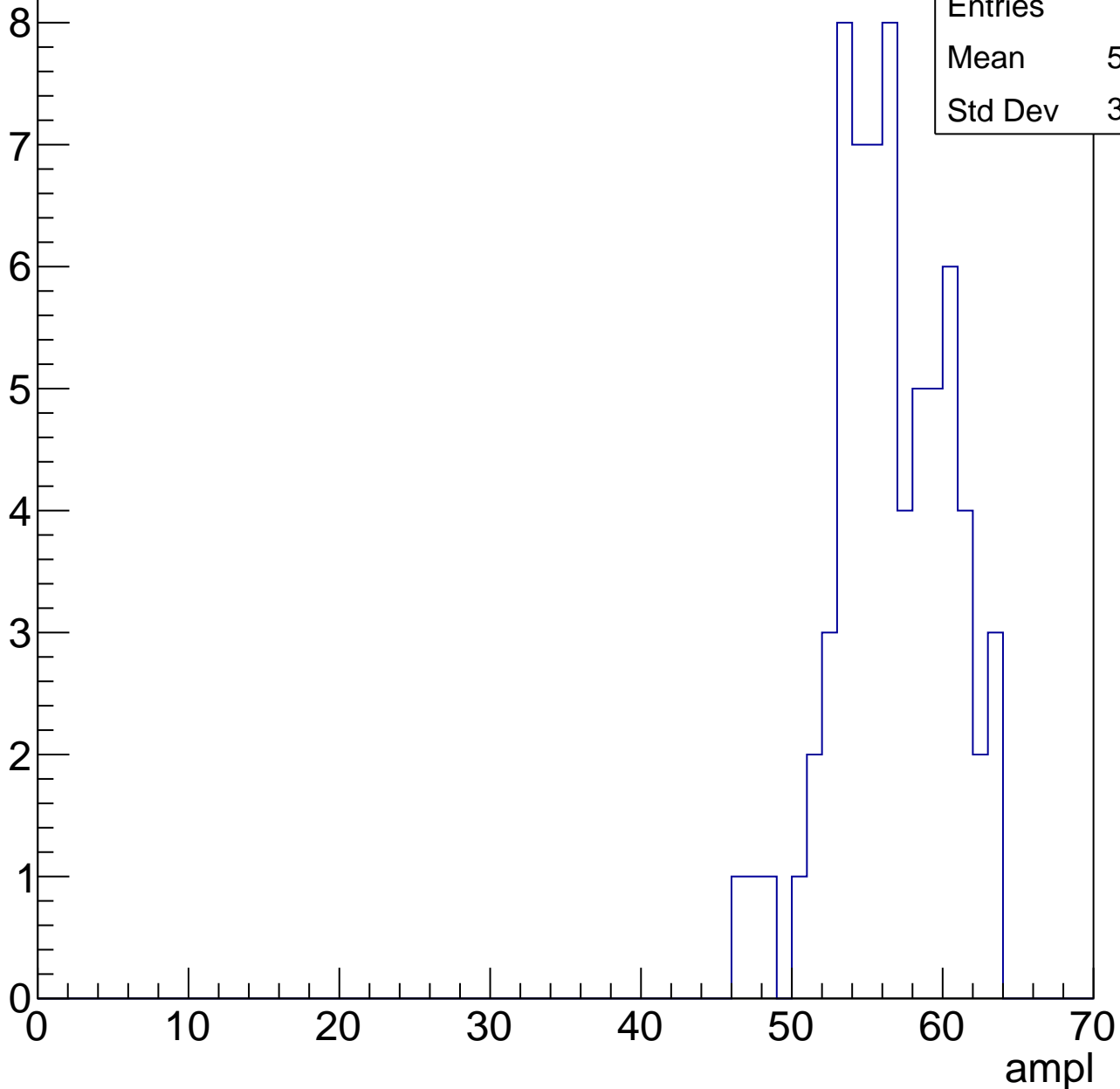


# B0L001S, U17-ch125, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	56.09
Std Dev	3.776



# B0L001S, U17-ch125, adc5

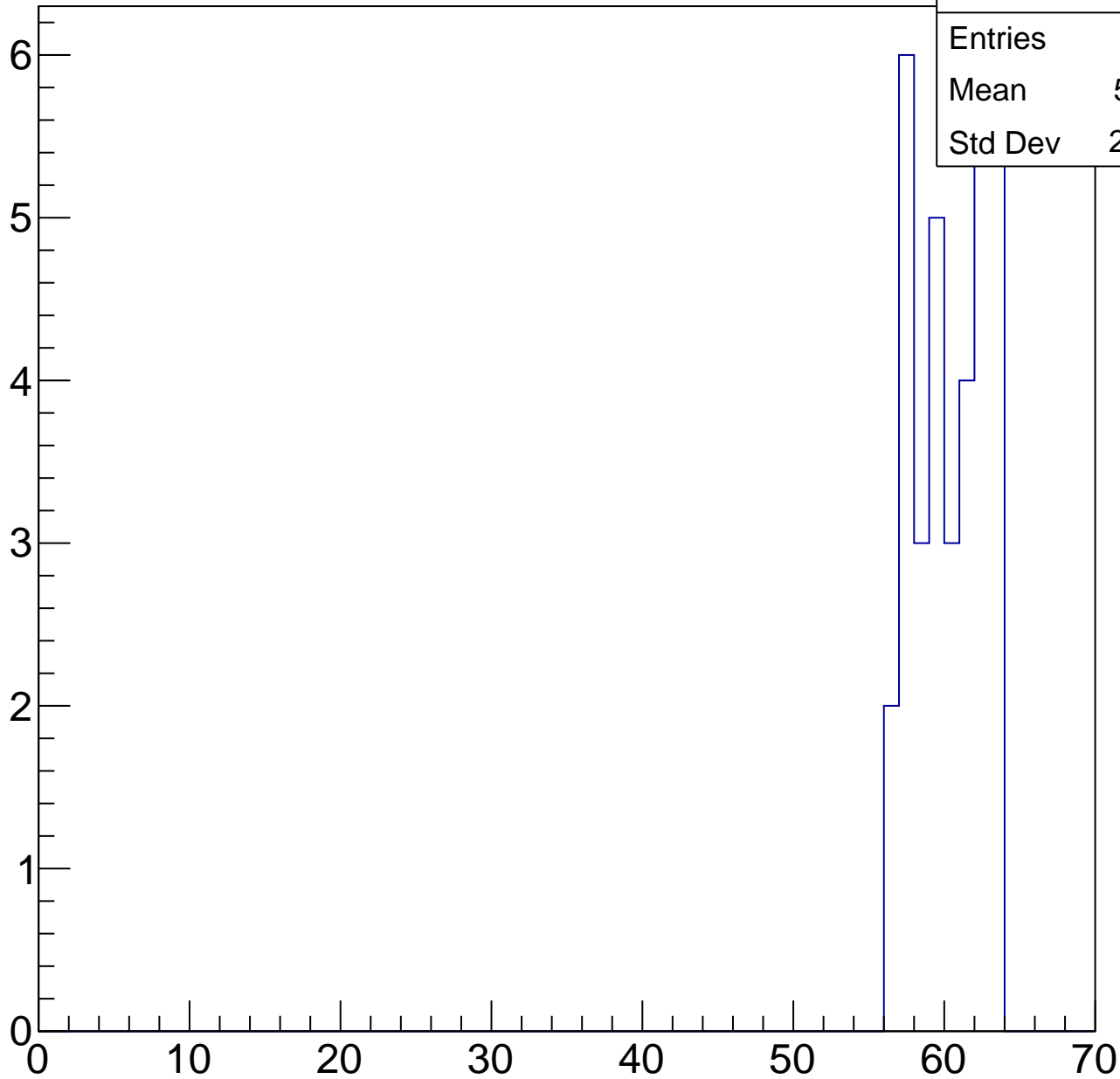
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

6  
5  
4  
3  
2  
1  
0

Entries	35
Mean	59.91
Std Dev	2.297

ampl



# B0L001S, U17-ch125, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

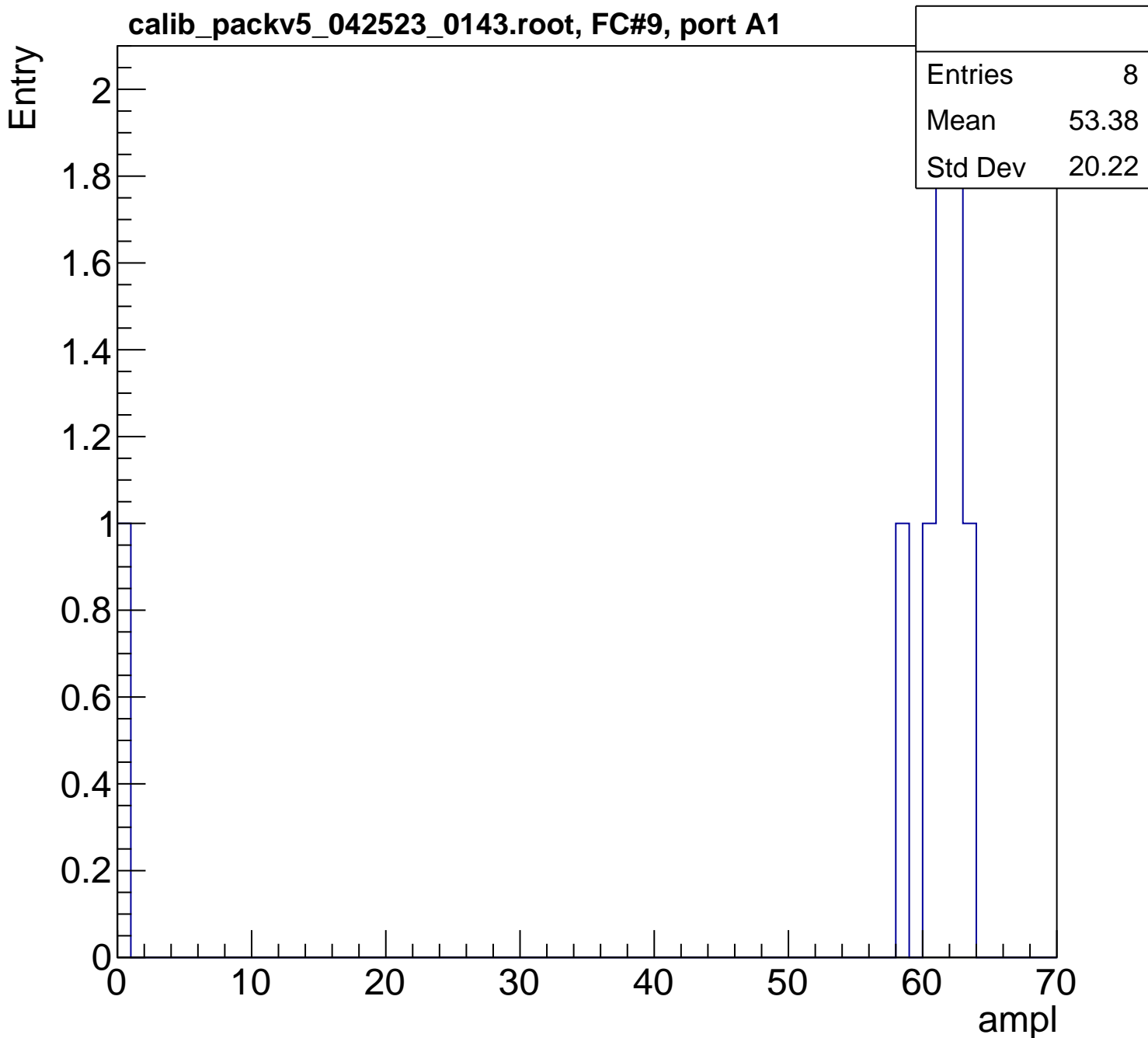
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	8
Mean	53.38
Std Dev	20.22

0 10 20 30 40 50 60 70

ampl





# B0L001S, U17-ch125, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L001S, U17-ch126, adc0

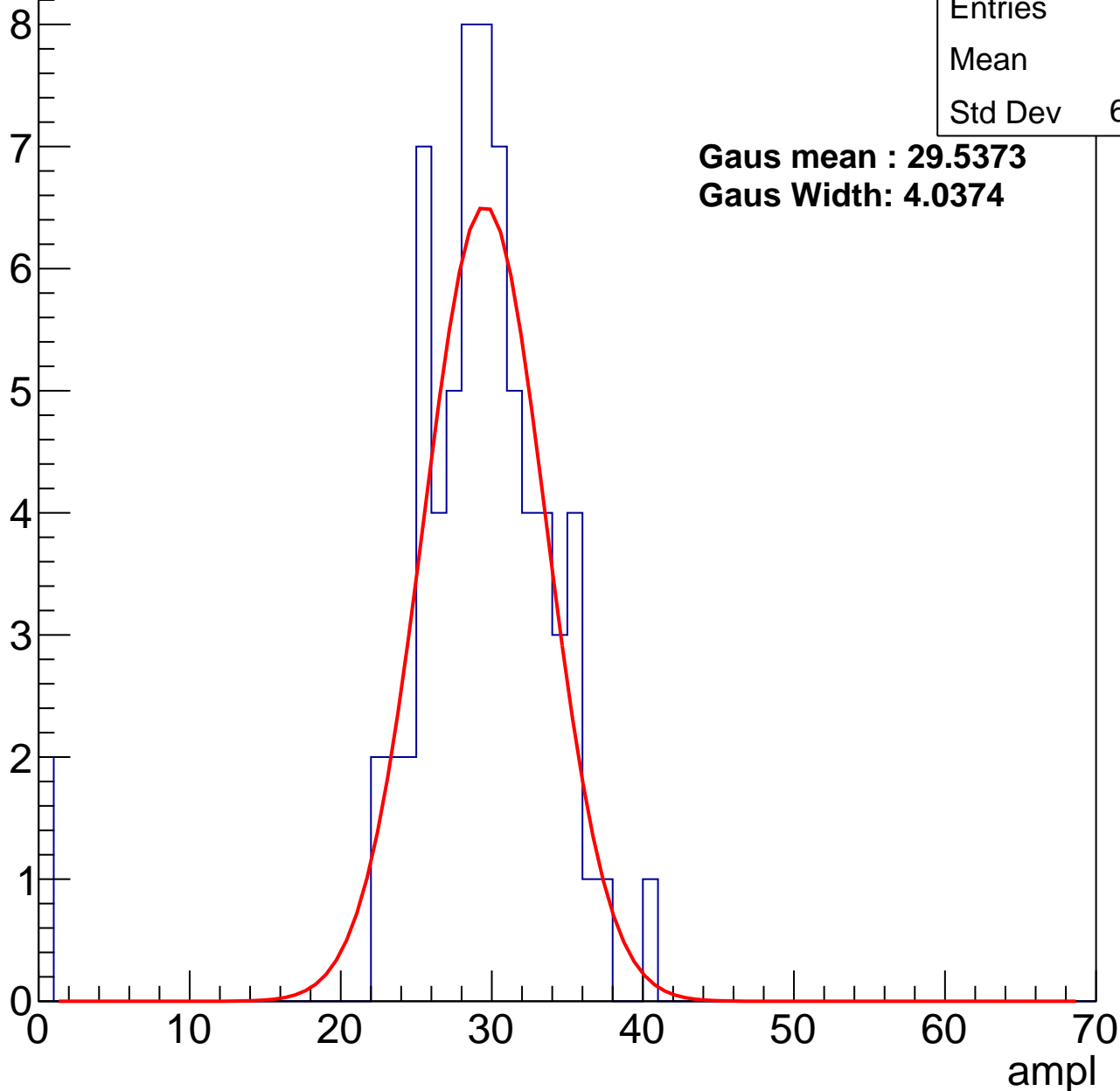
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	28.4
Std Dev	6.133

**Gaus mean : 29.5373**

**Gaus Width: 4.0374**



# B0L001S, U17-ch126, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	62
Mean	35.66
Std Dev	3.307

**Gaus mean : 36.2694**

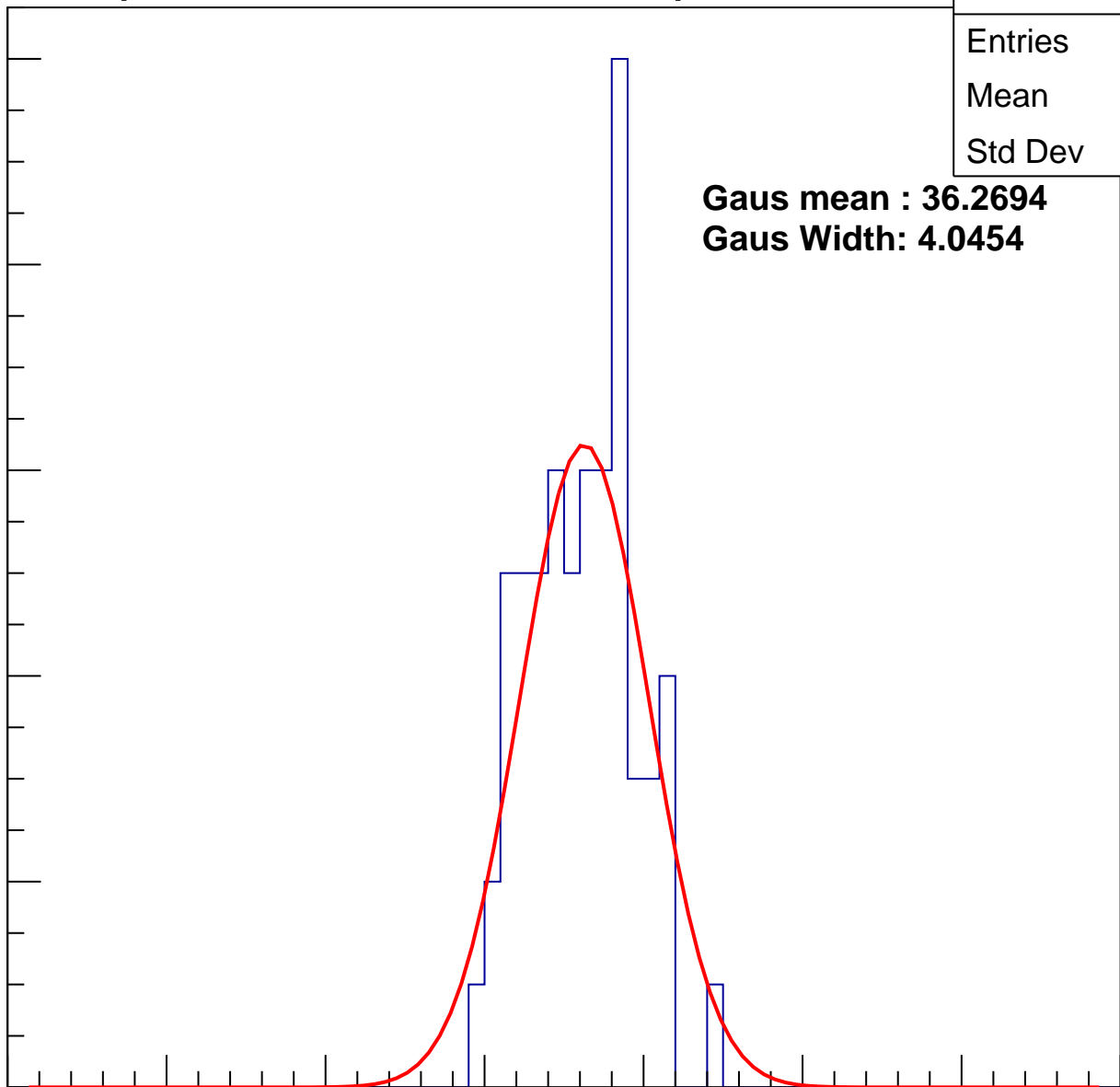
**Gaus Width: 4.0454**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U17-ch126, adc2

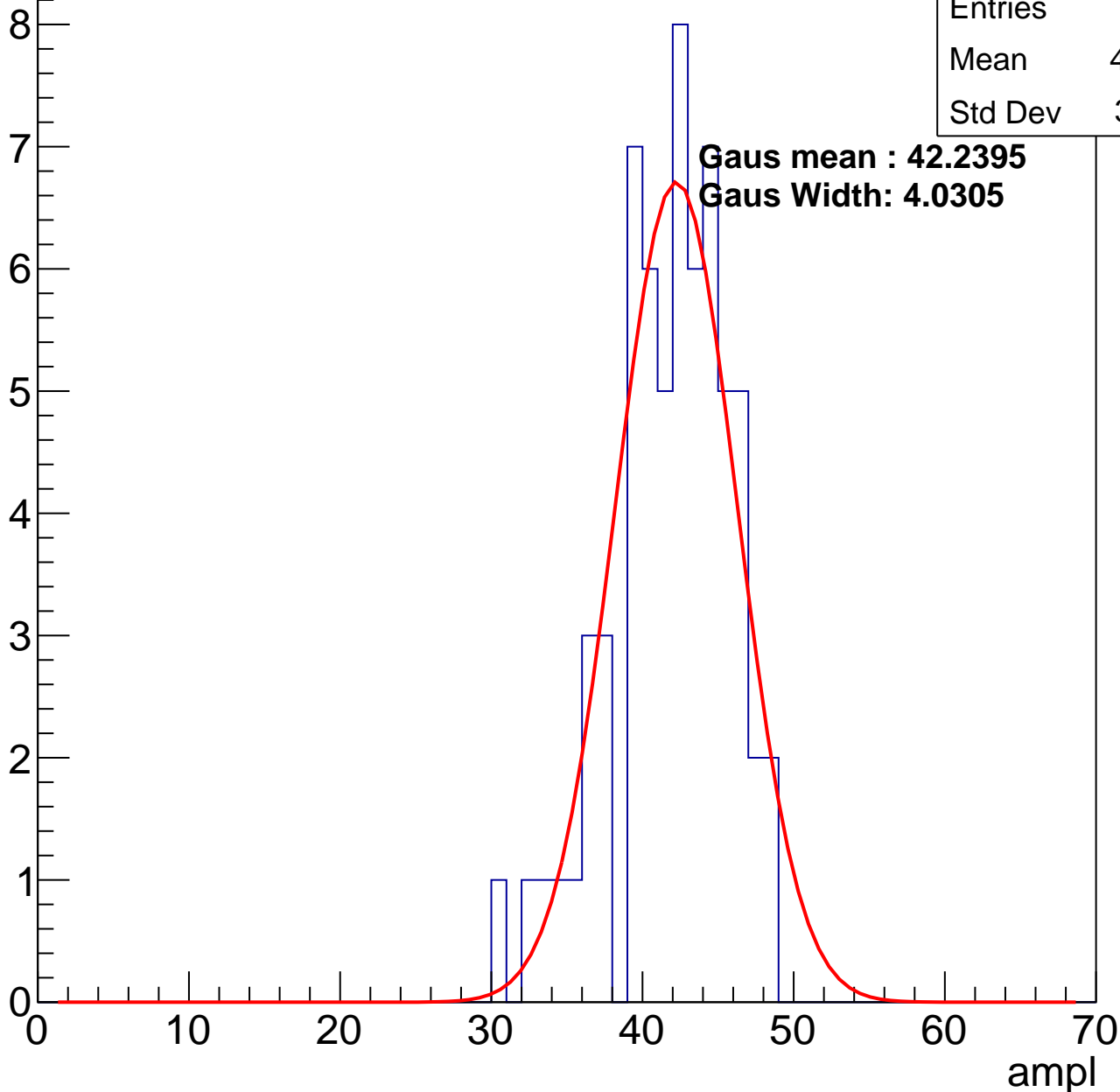
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	41.38
Std Dev	3.891

**Gaus mean : 42.2395**

**Gaus Width: 4.0305**

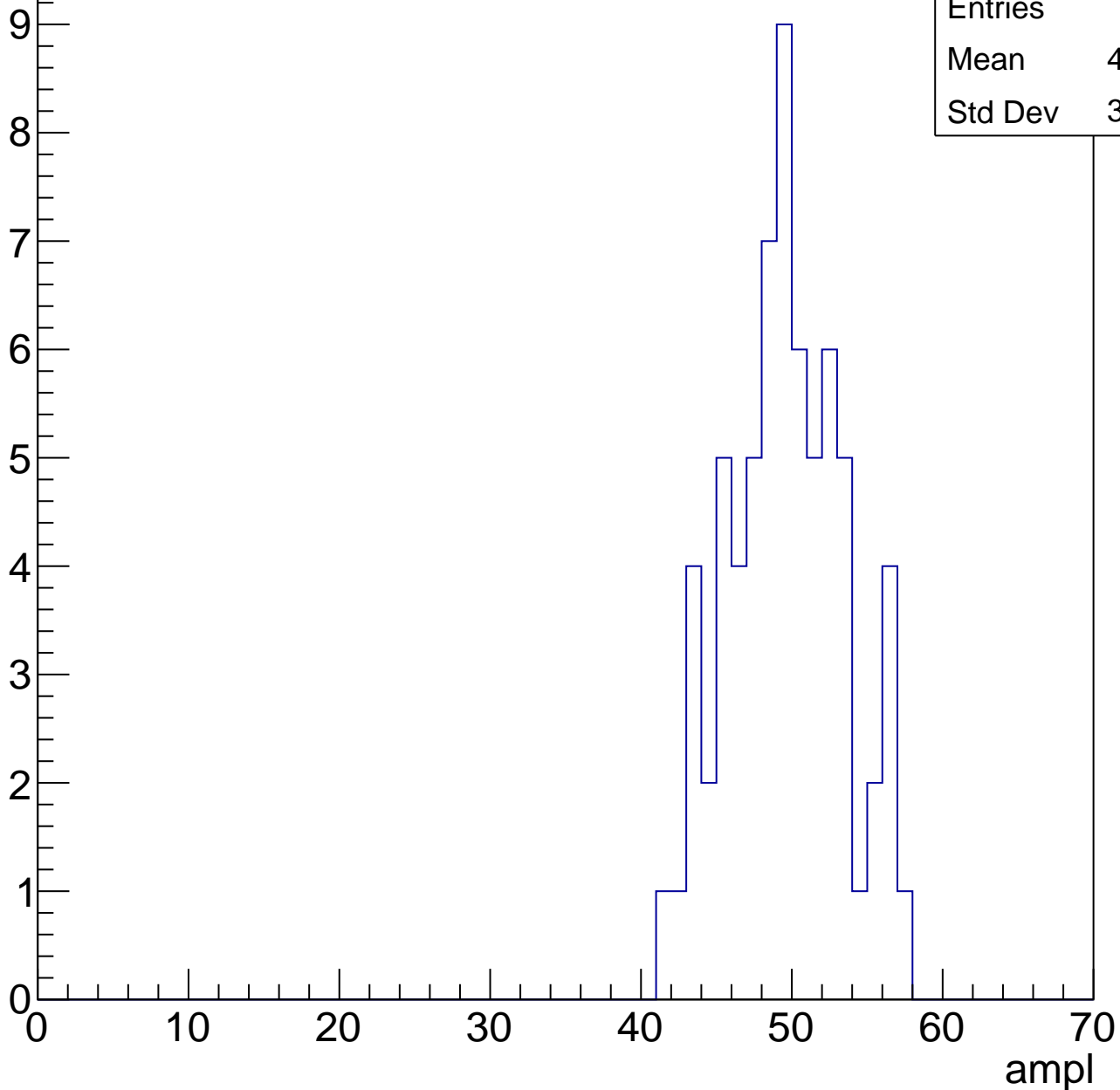


# B0L001S, U17-ch126, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	49.13
Std Dev	3.769

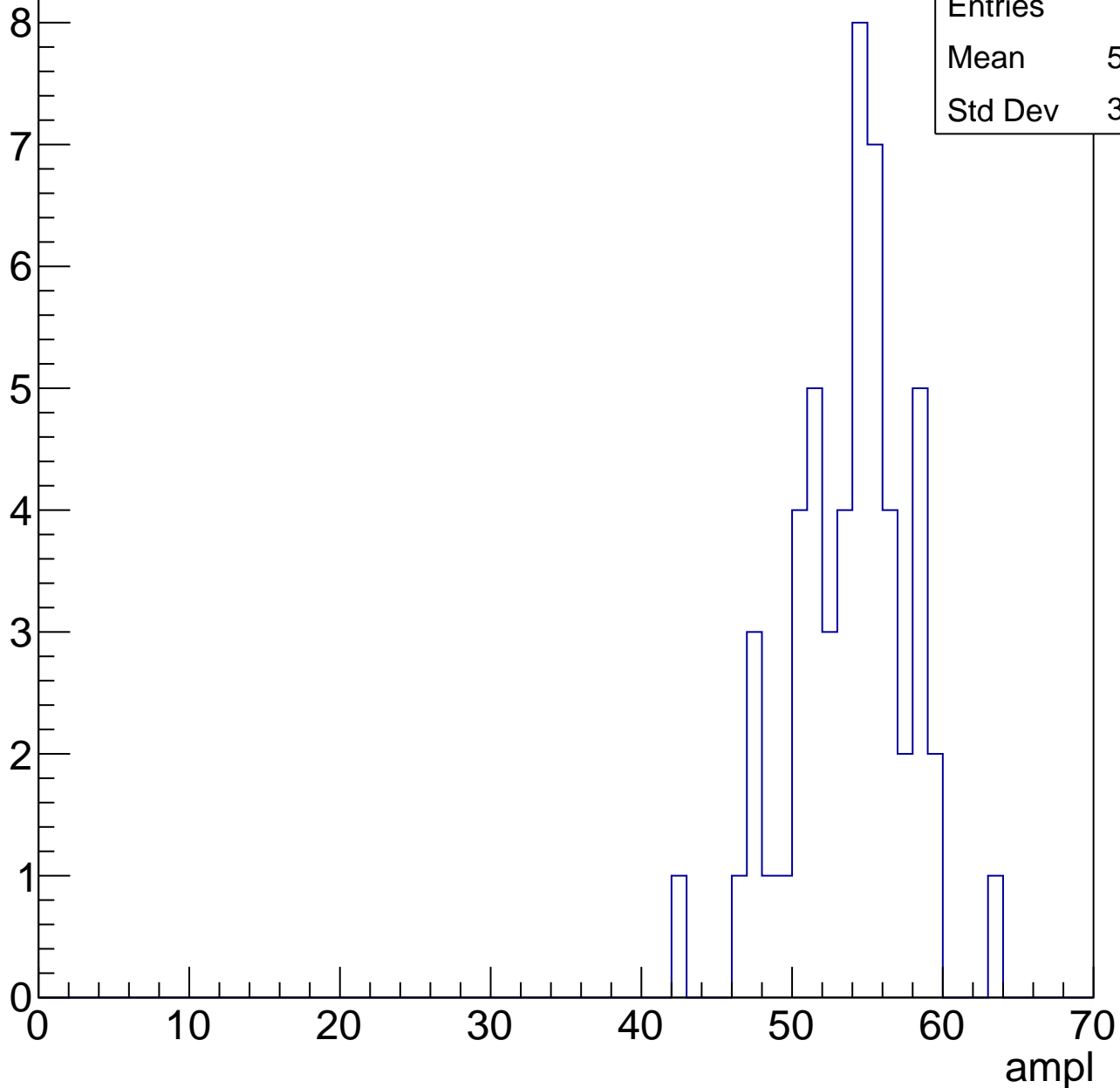


# B0L001S, U17-ch126, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

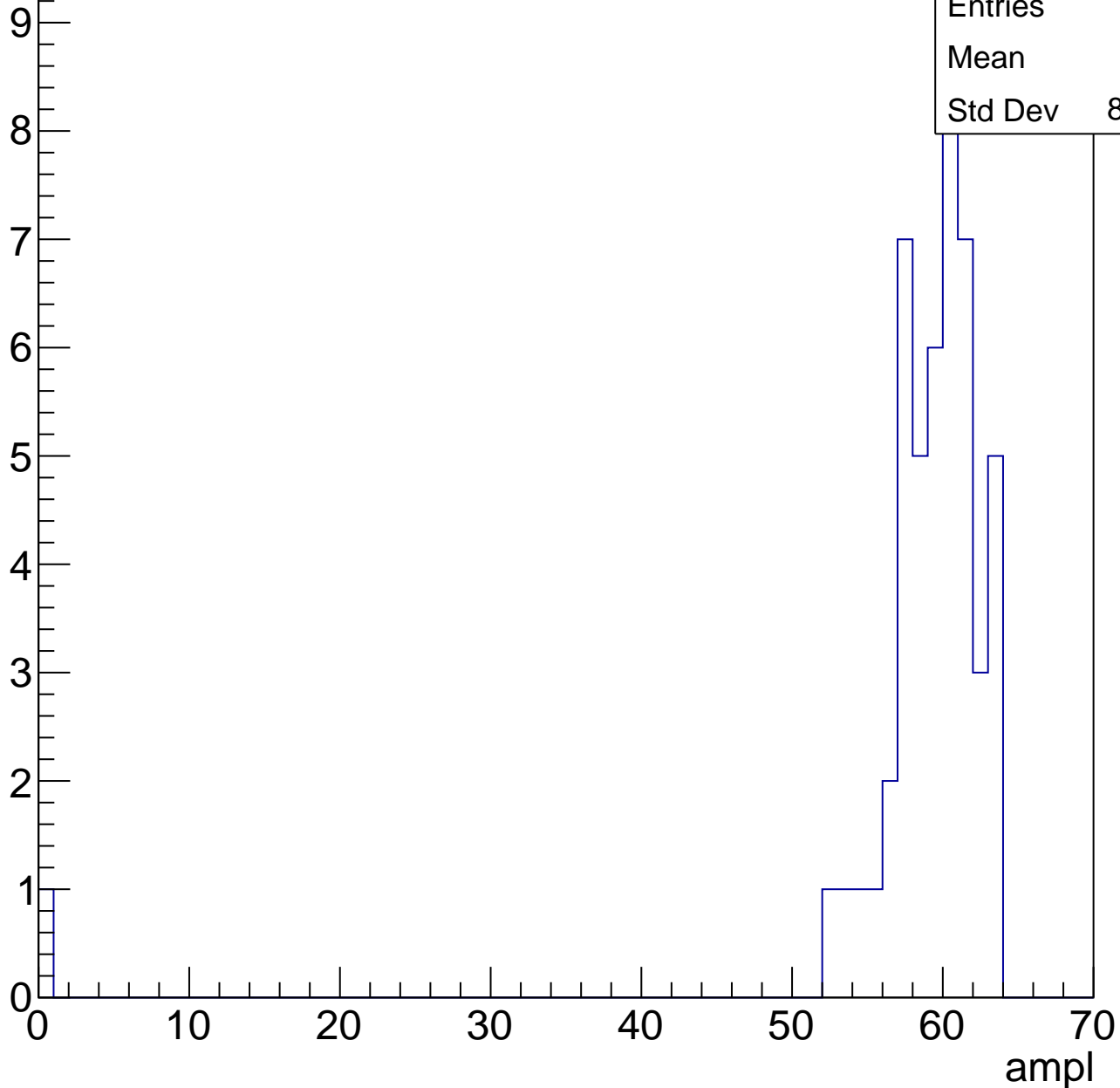
Entries	52
Mean	53.37
Std Dev	3.853



# B0L001S, U17-ch126, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

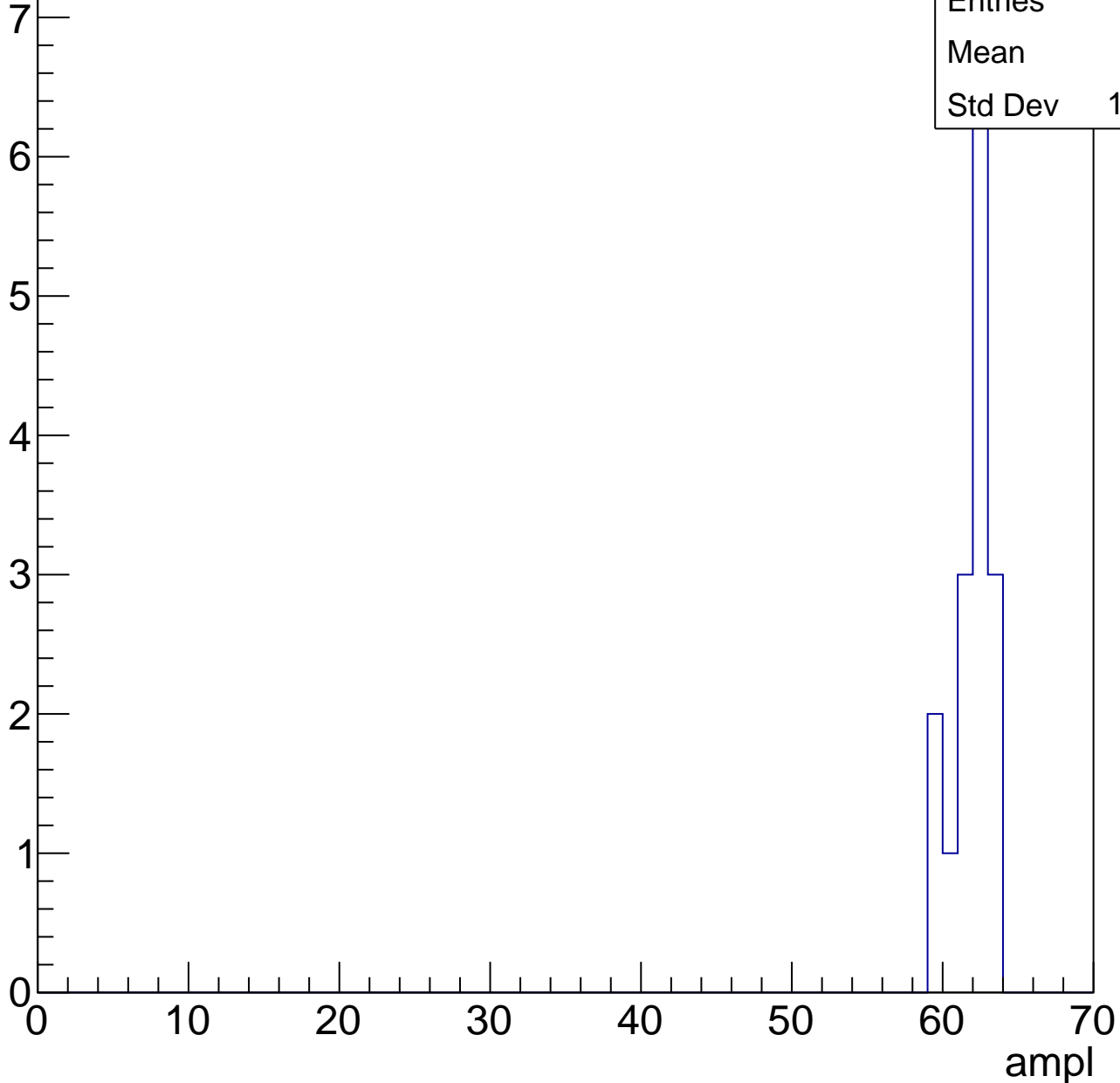


# B0L001S, U17-ch126, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	16
Mean	61.5
Std Dev	1.225

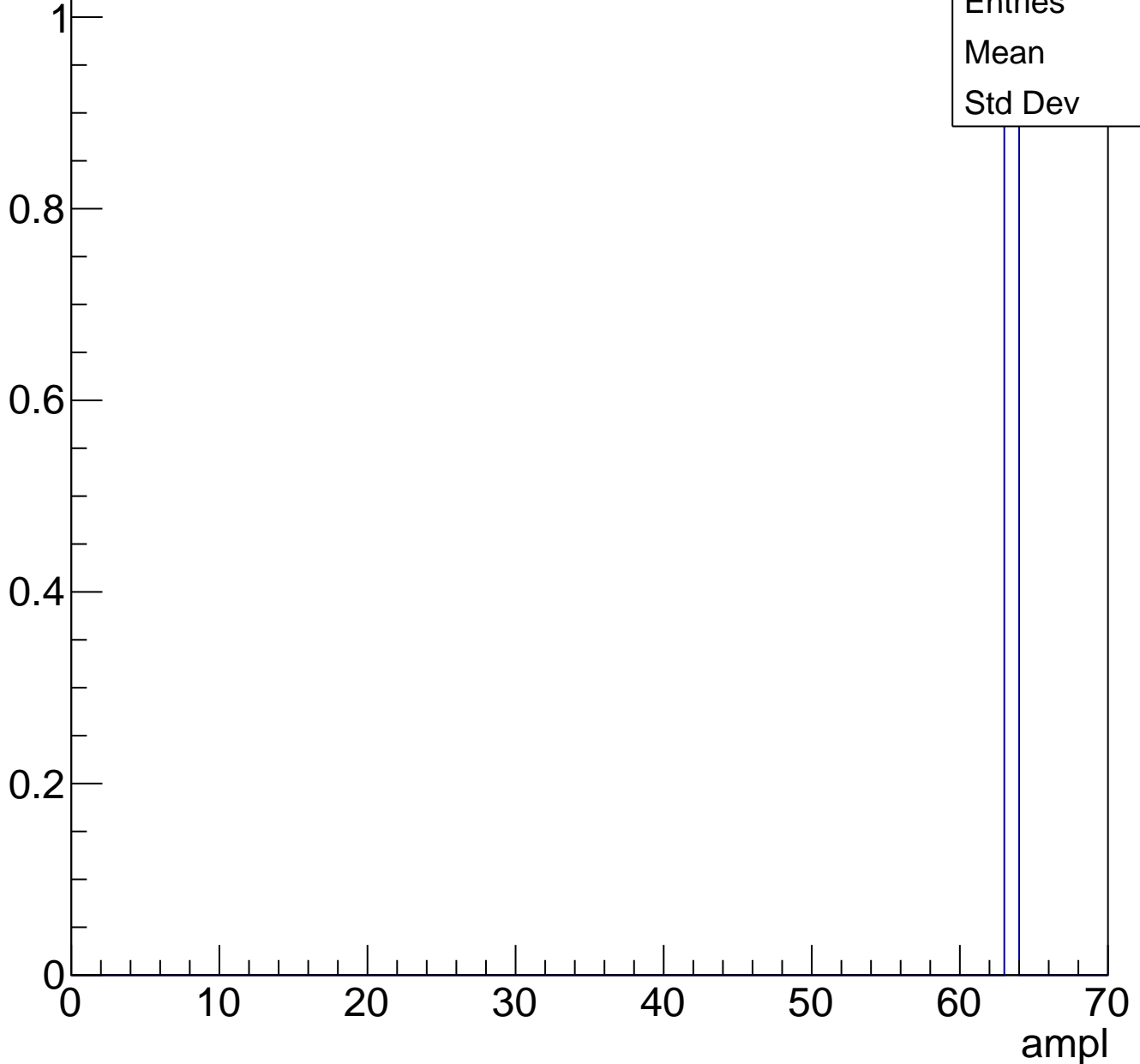




# B0L001S, U17-ch126, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U17-ch127, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	67
Mean	30.75
Std Dev	4.798

**Gaus mean : 31.7099**

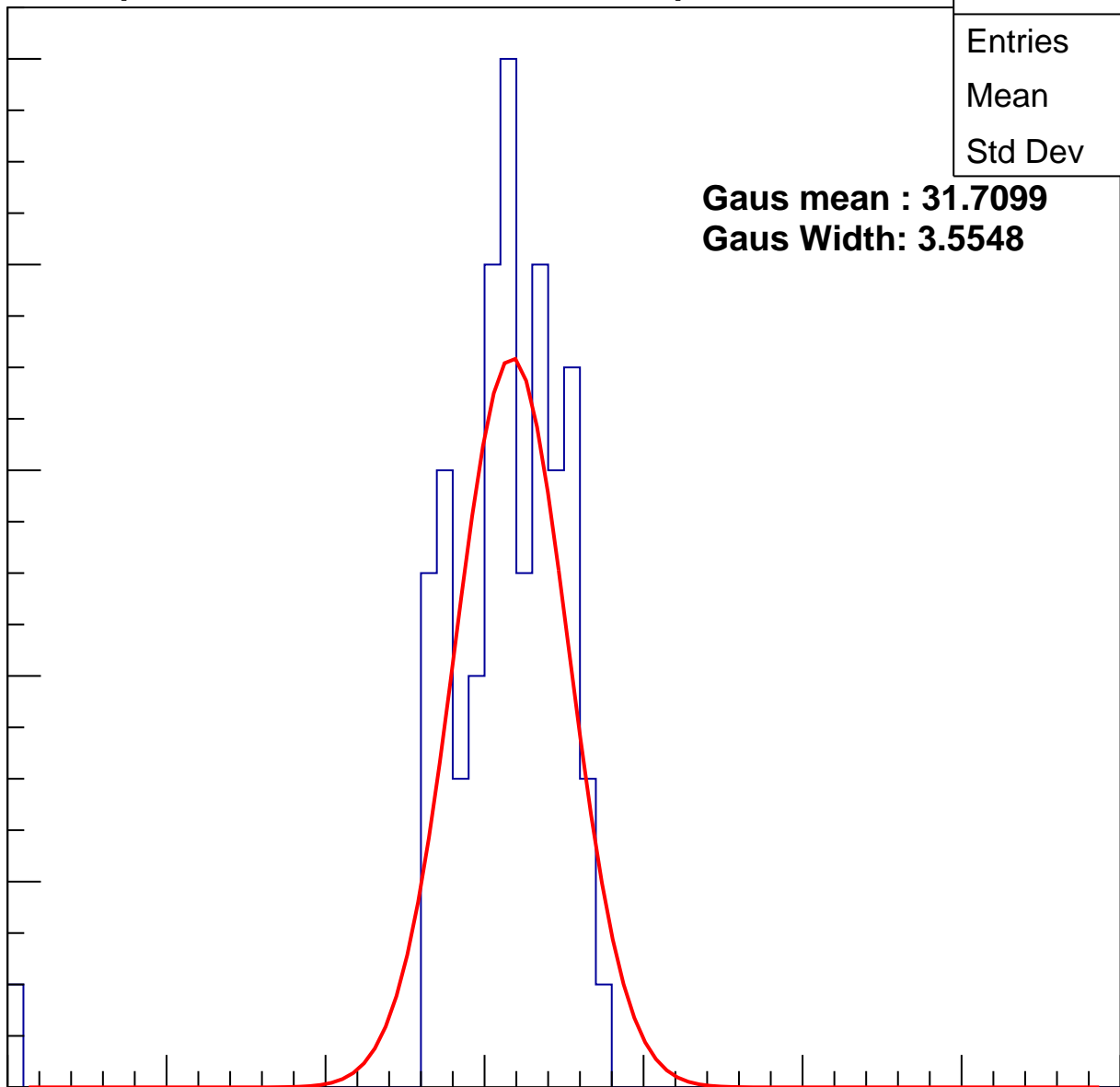
**Gaus Width: 3.5548**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U17-ch127, adc1

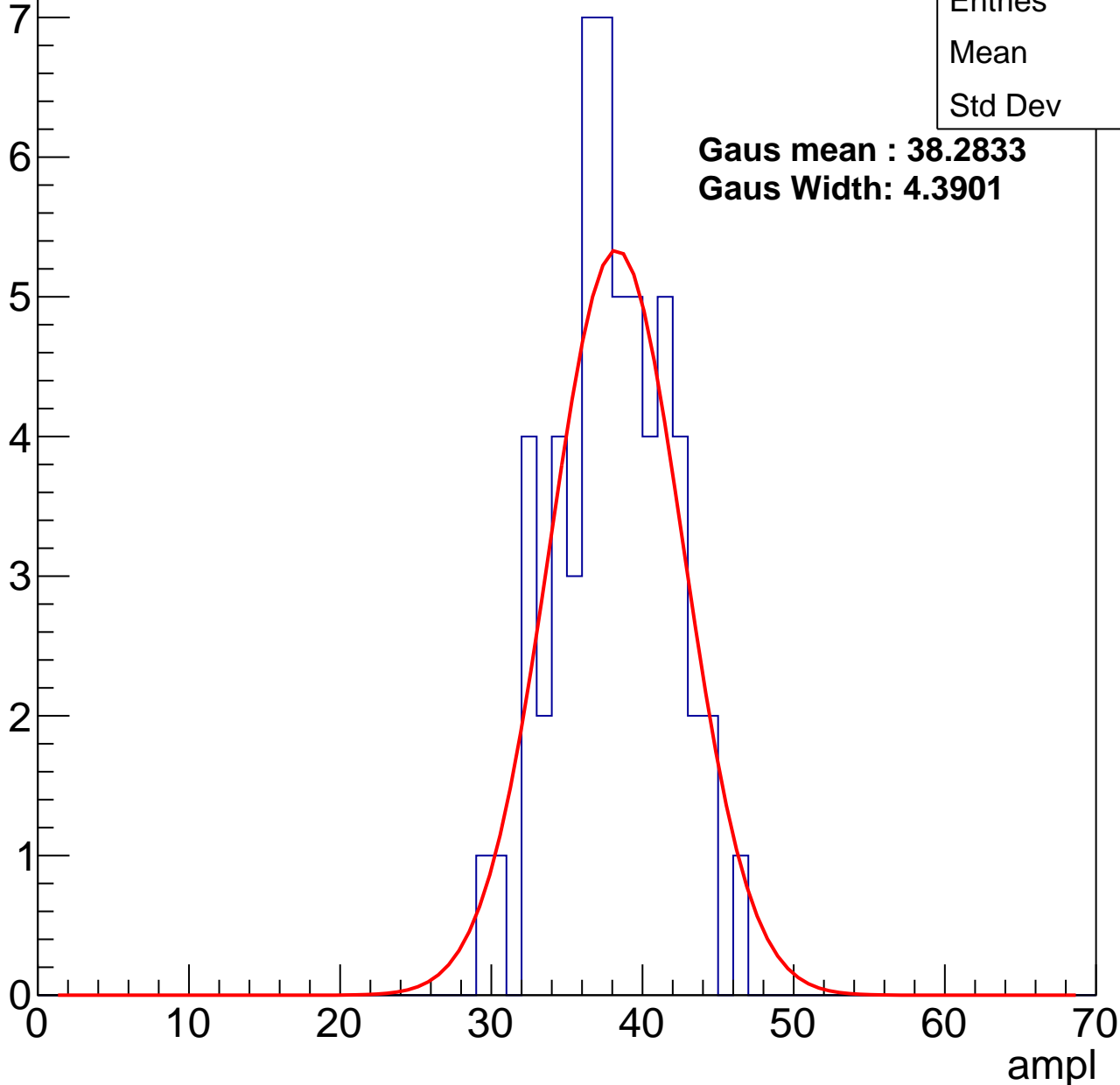
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	37.6
Std Dev	3.68

**Gaus mean : 38.2833**

**Gaus Width: 4.3901**



# B0L001S, U17-ch127, adc2

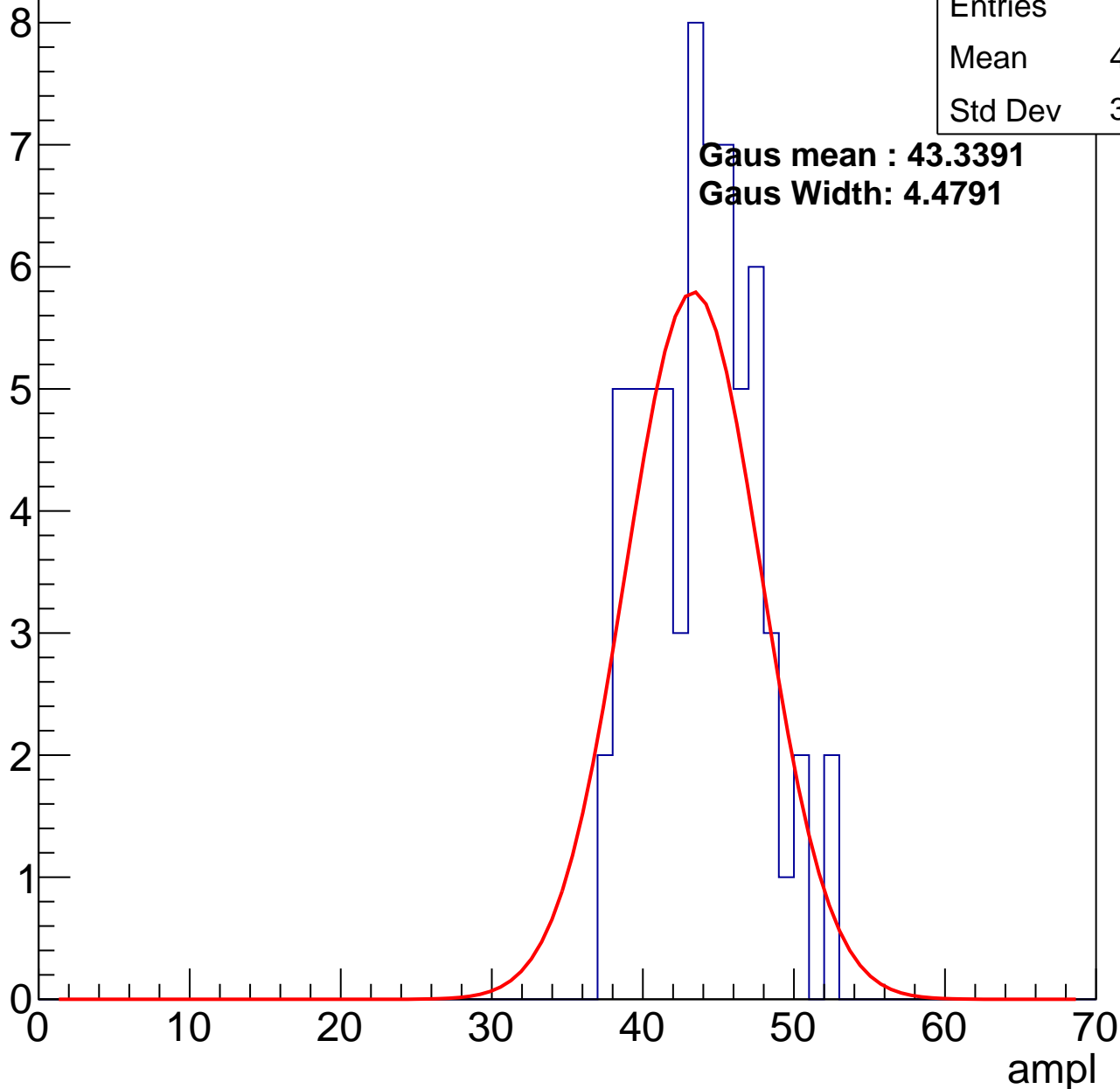
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	43.42
Std Dev	3.652

**Gaus mean : 43.3391**

**Gaus Width: 4.4791**

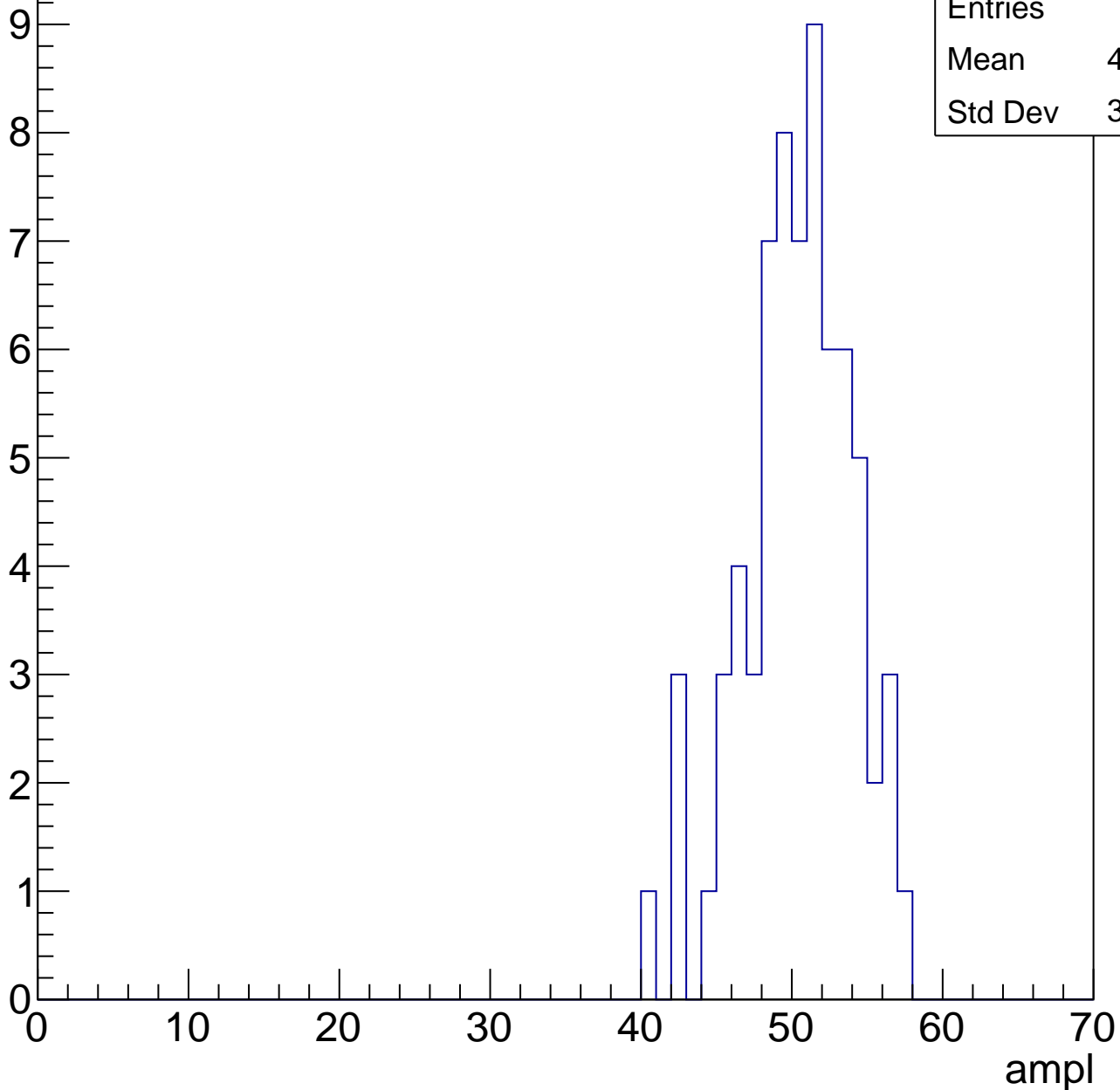


# B0L001S, U17-ch127, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	49.88
Std Dev	3.618

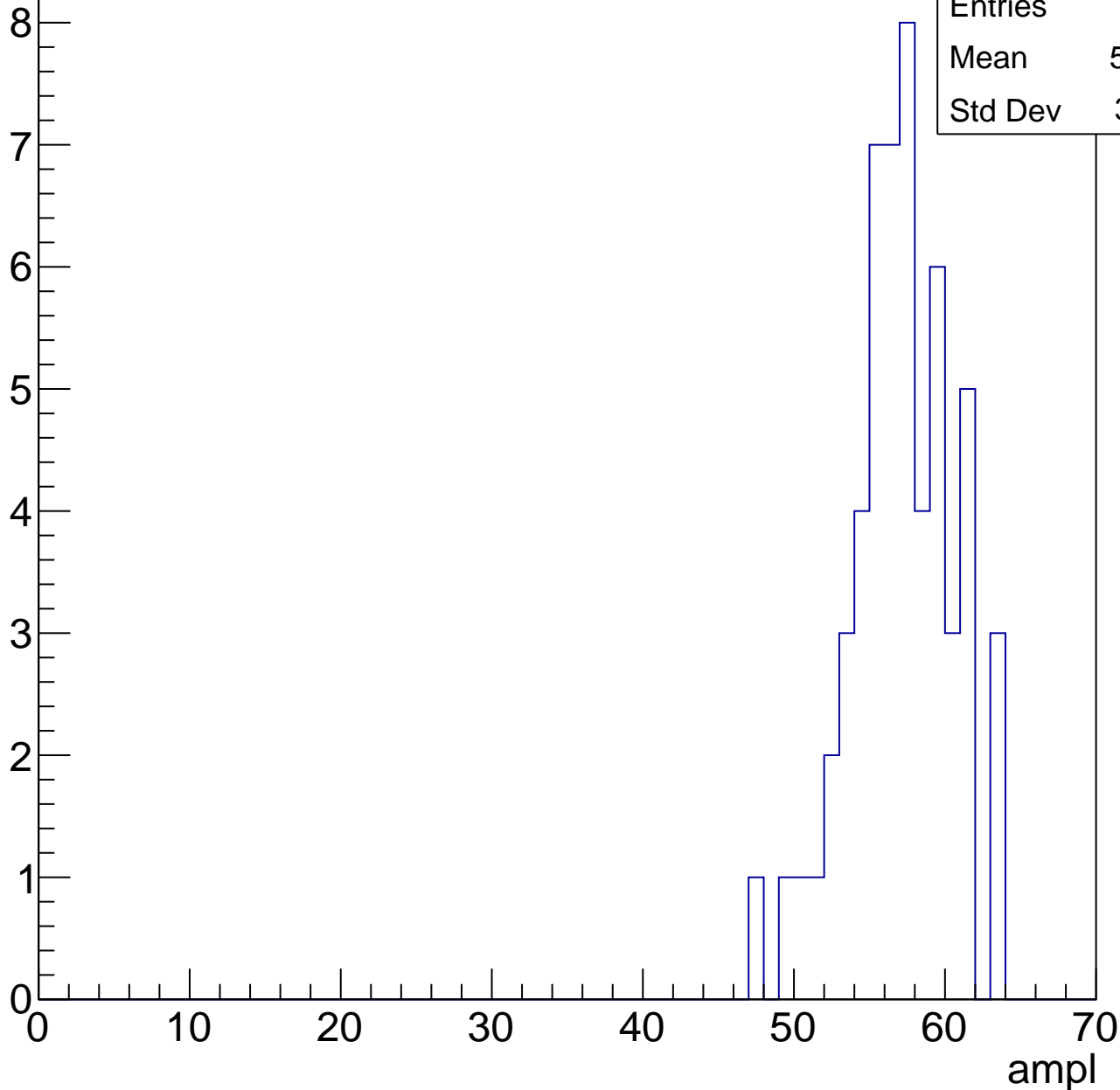


# B0L001S, U17-ch127, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	56.59
Std Dev	3.411

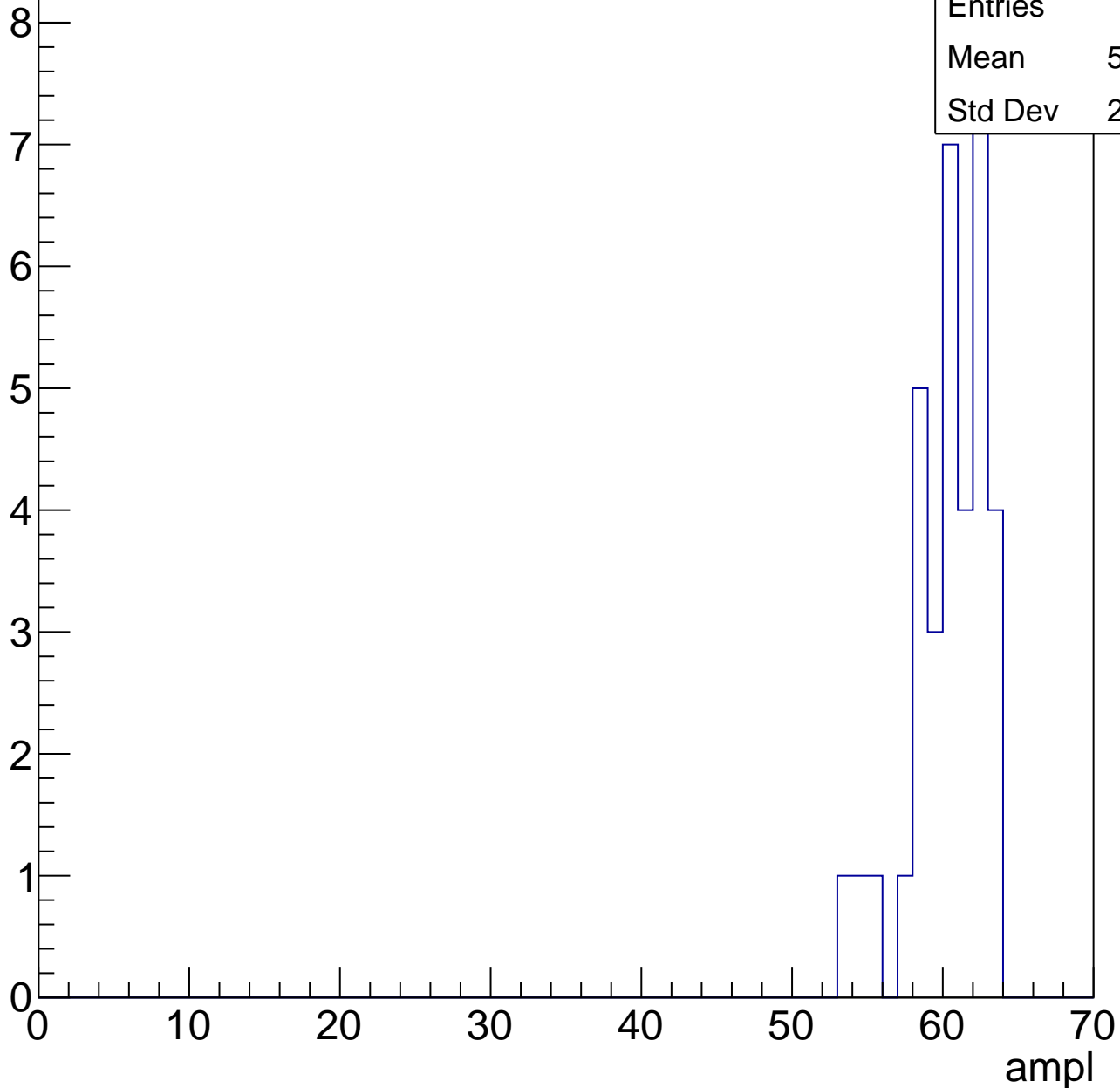


# B0L001S, U17-ch127, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

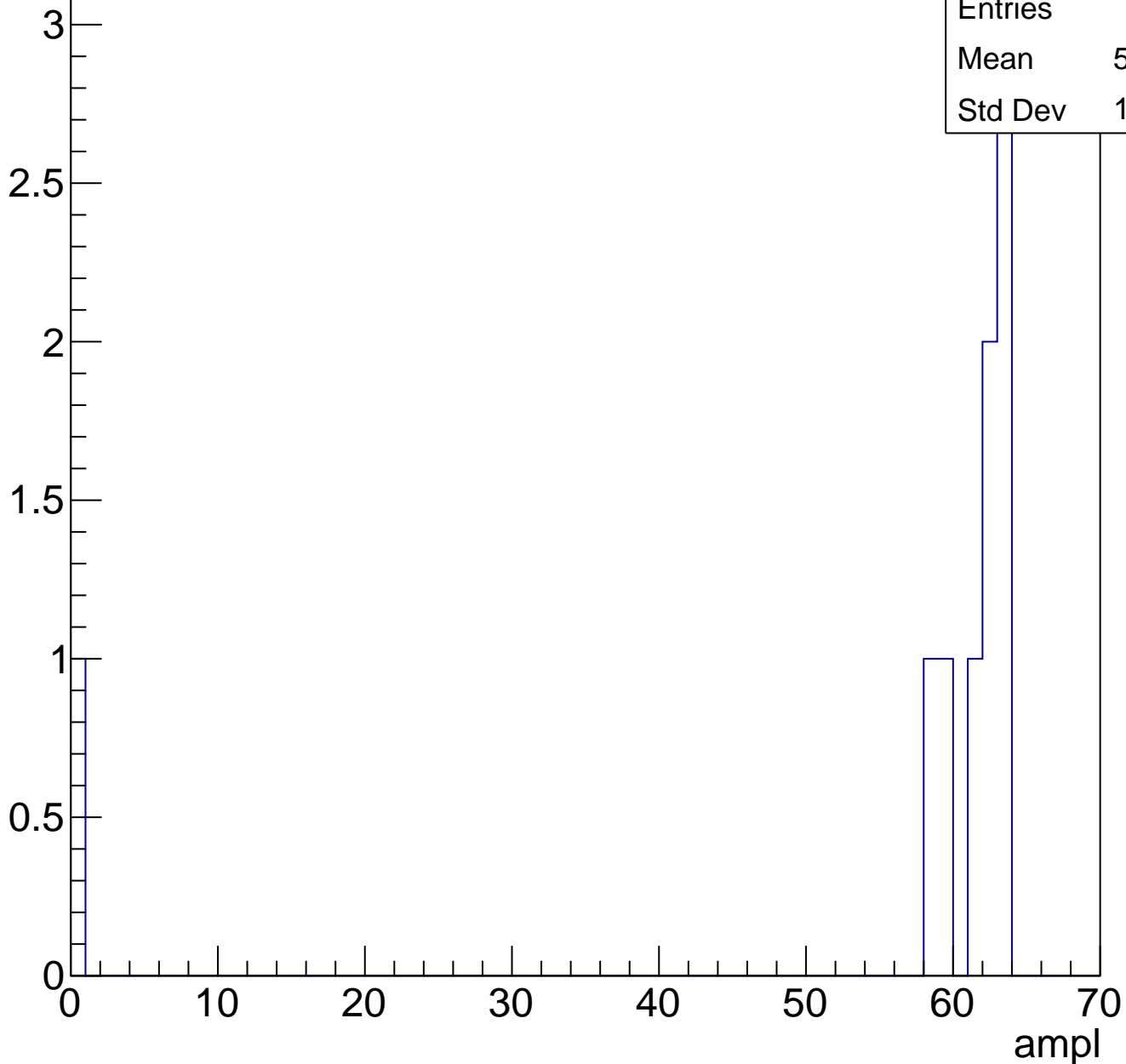
Entries	35
Mean	59.94
Std Dev	2.472



# B0L001S, U17-ch127, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U17-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U17-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0