



# B1L103S, U3-ch0, adc0

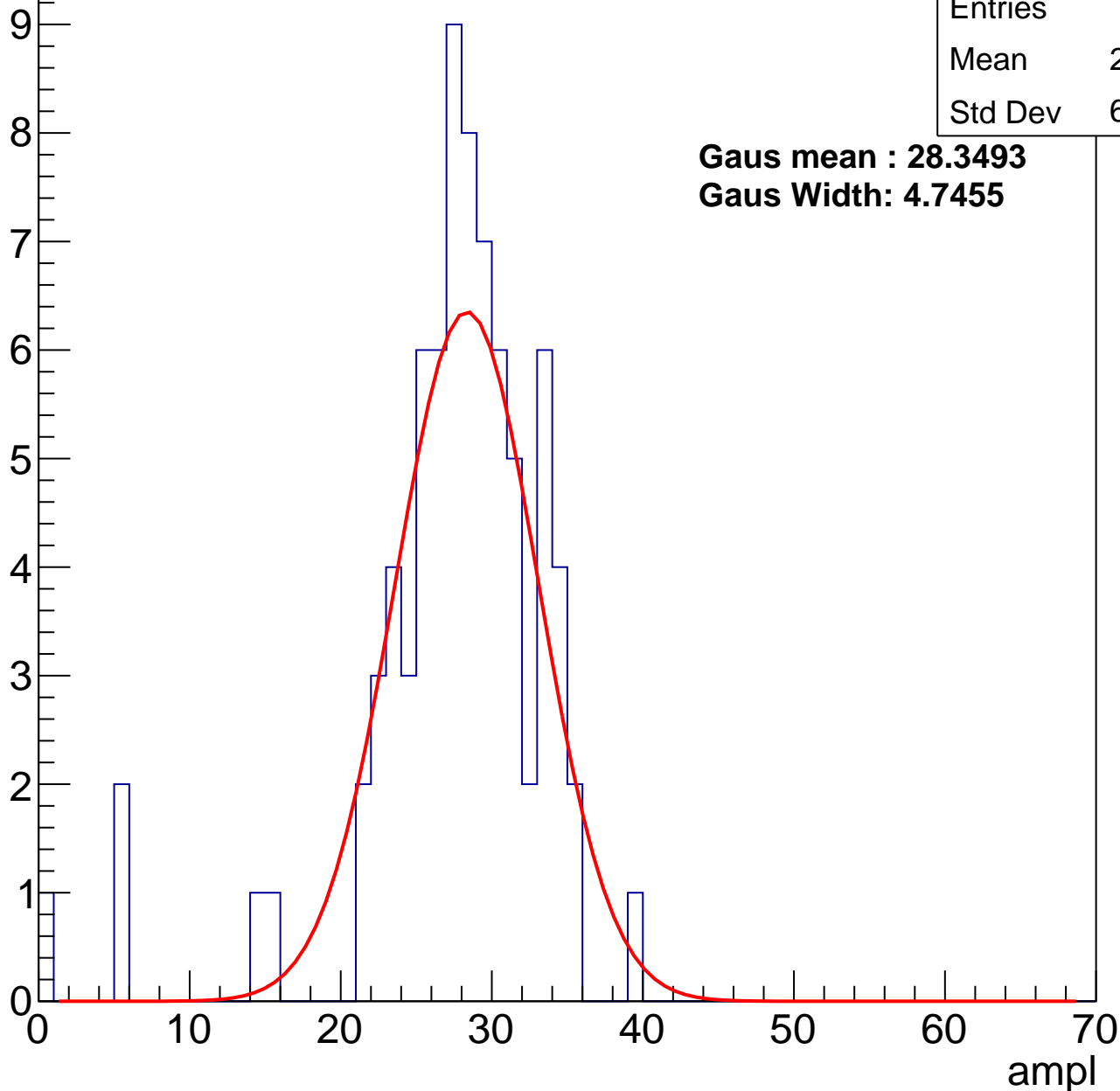
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	79
Mean	26.95
Std Dev	6.346

**Gaus mean : 28.3493**

**Gaus Width: 4.7455**



# B1L103S, U3-ch0, adc1

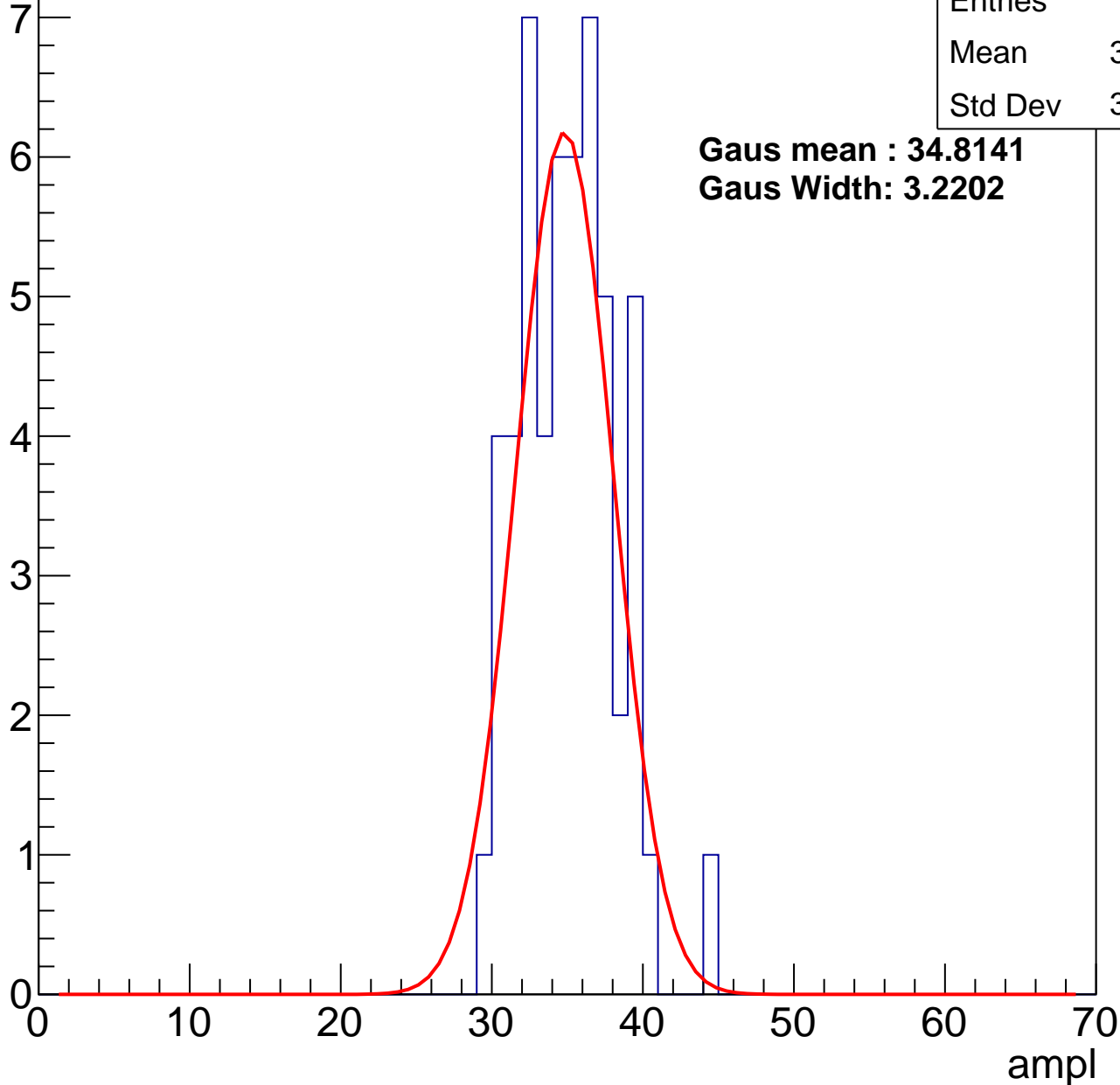
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	34.62
Std Dev	3.097

**Gaus mean : 34.8141**

**Gaus Width: 3.2202**



# B1L103S, U3-ch0, adc2

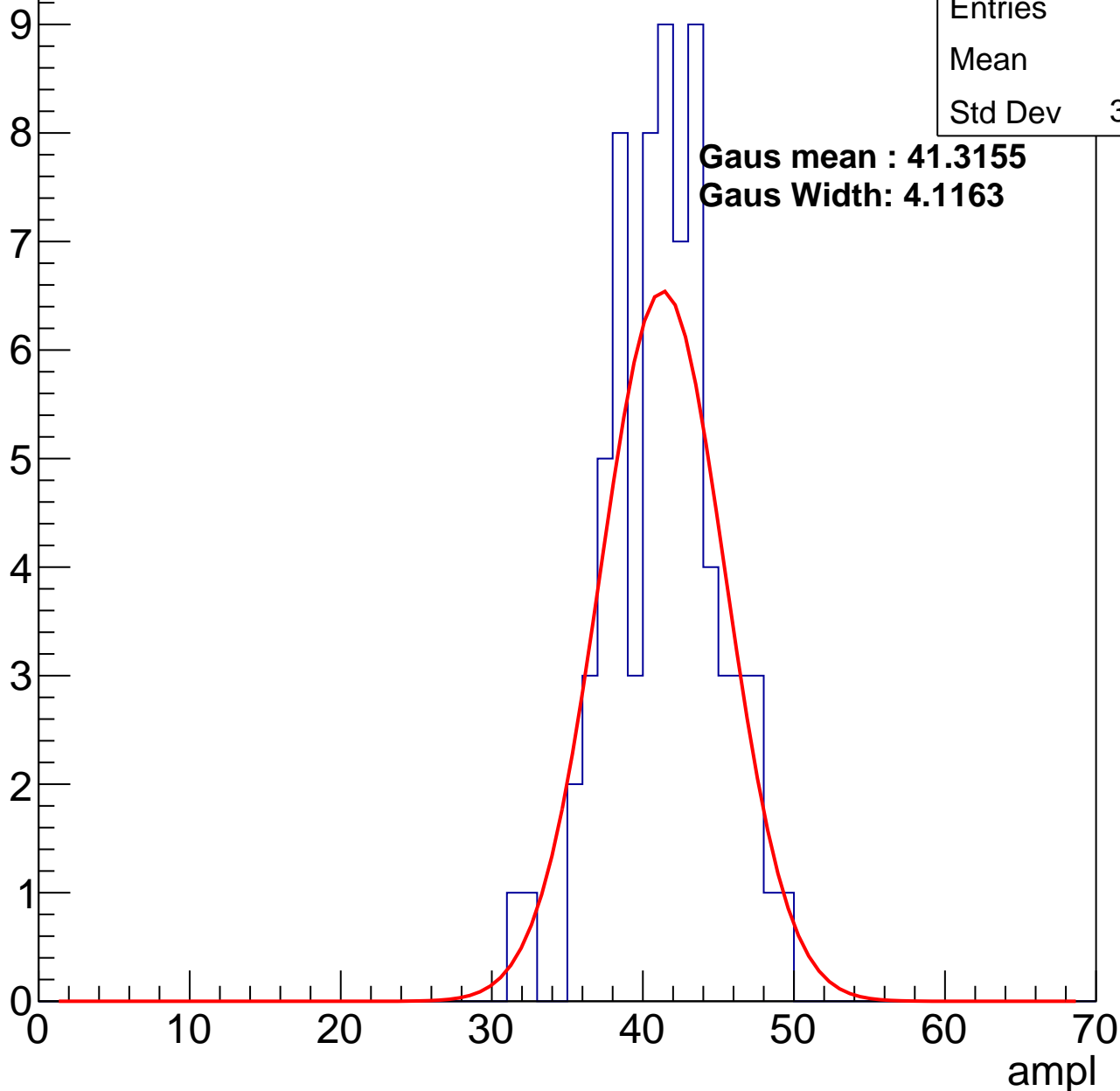
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	40.9
Std Dev	3.604

**Gaus mean : 41.3155**

**Gaus Width: 4.1163**

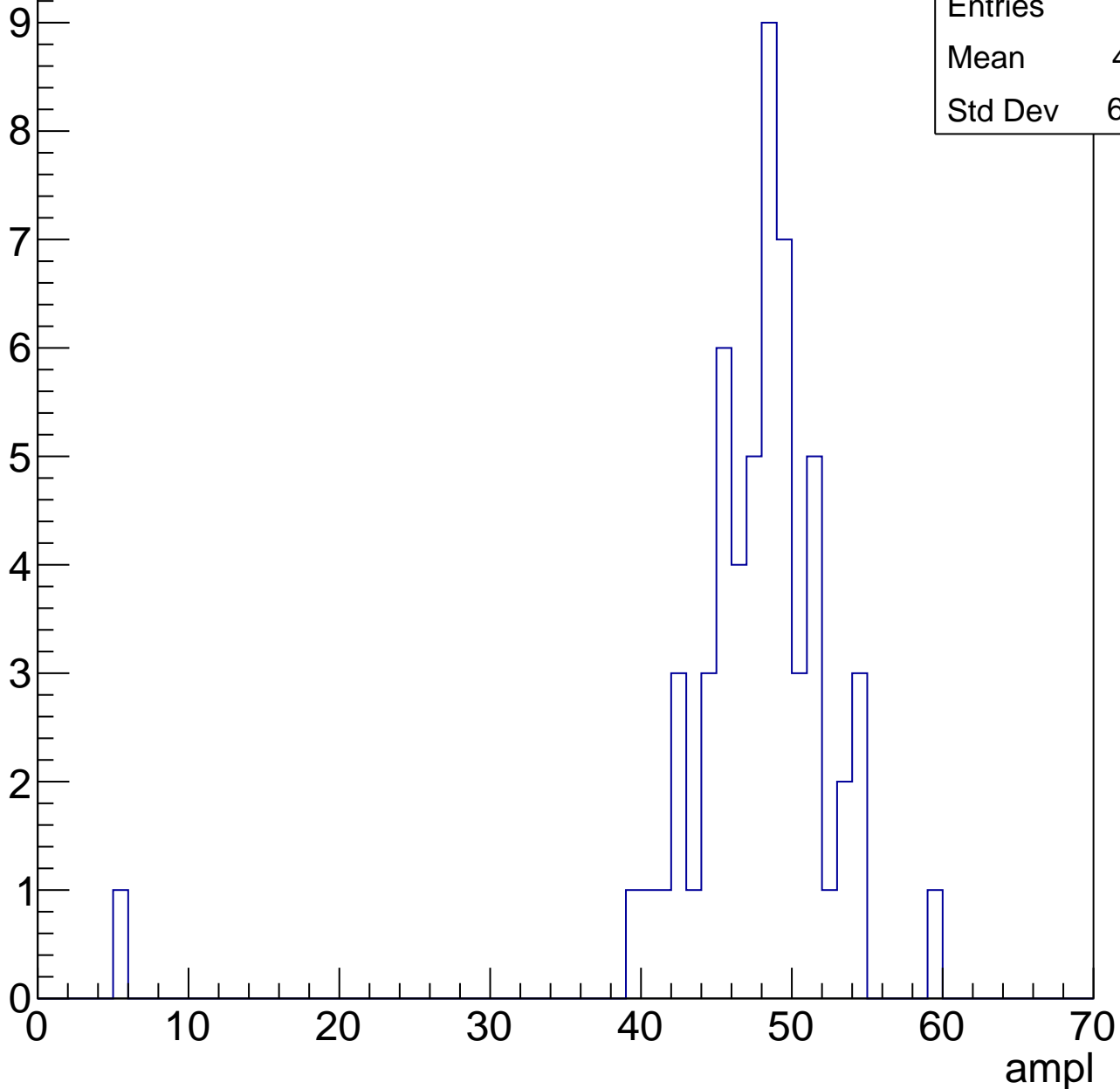


# B1L103S, U3-ch0, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

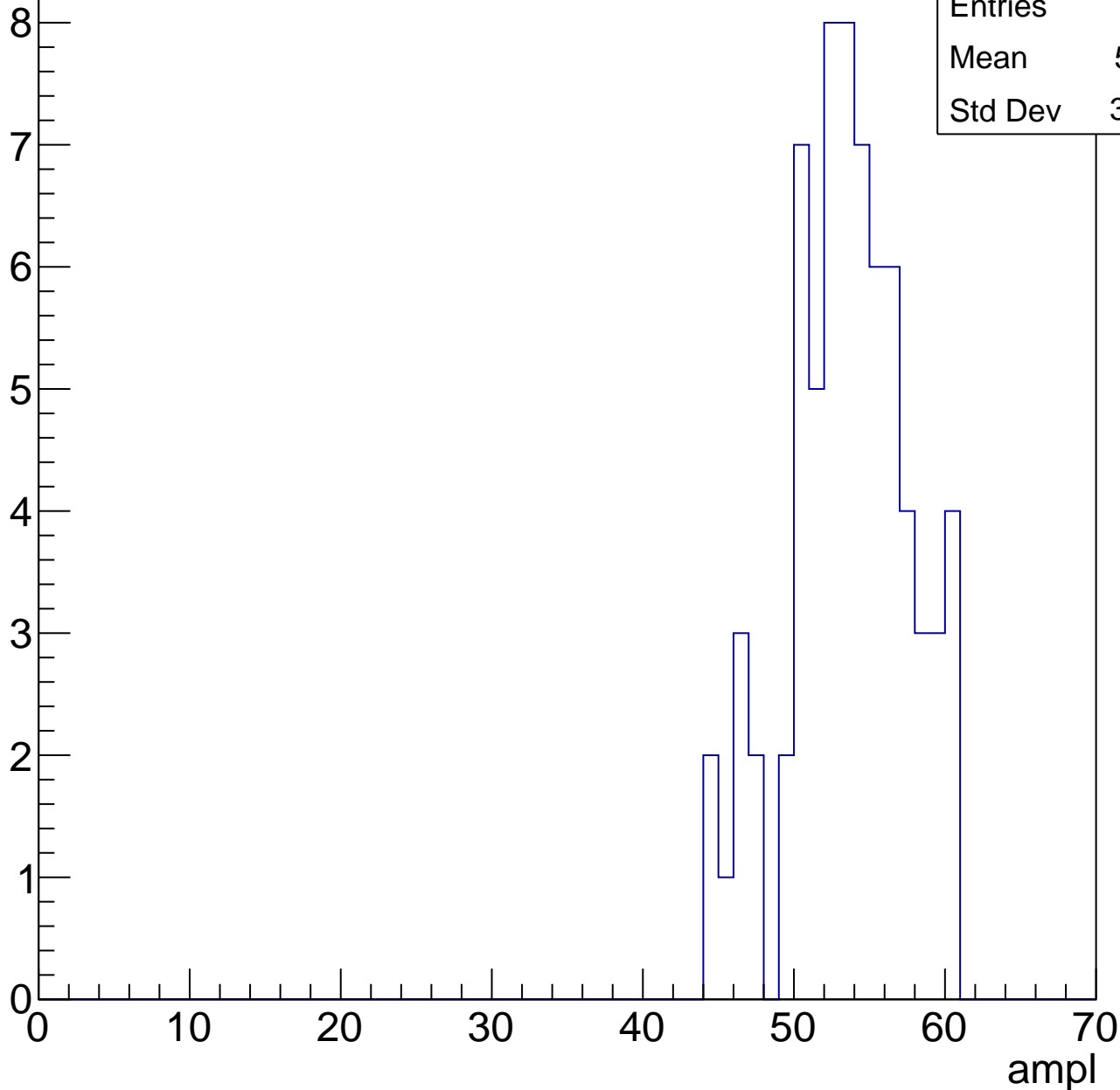
Entries	57
Mean	46.91
Std Dev	6.742



# B1L103S, U3-ch0, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



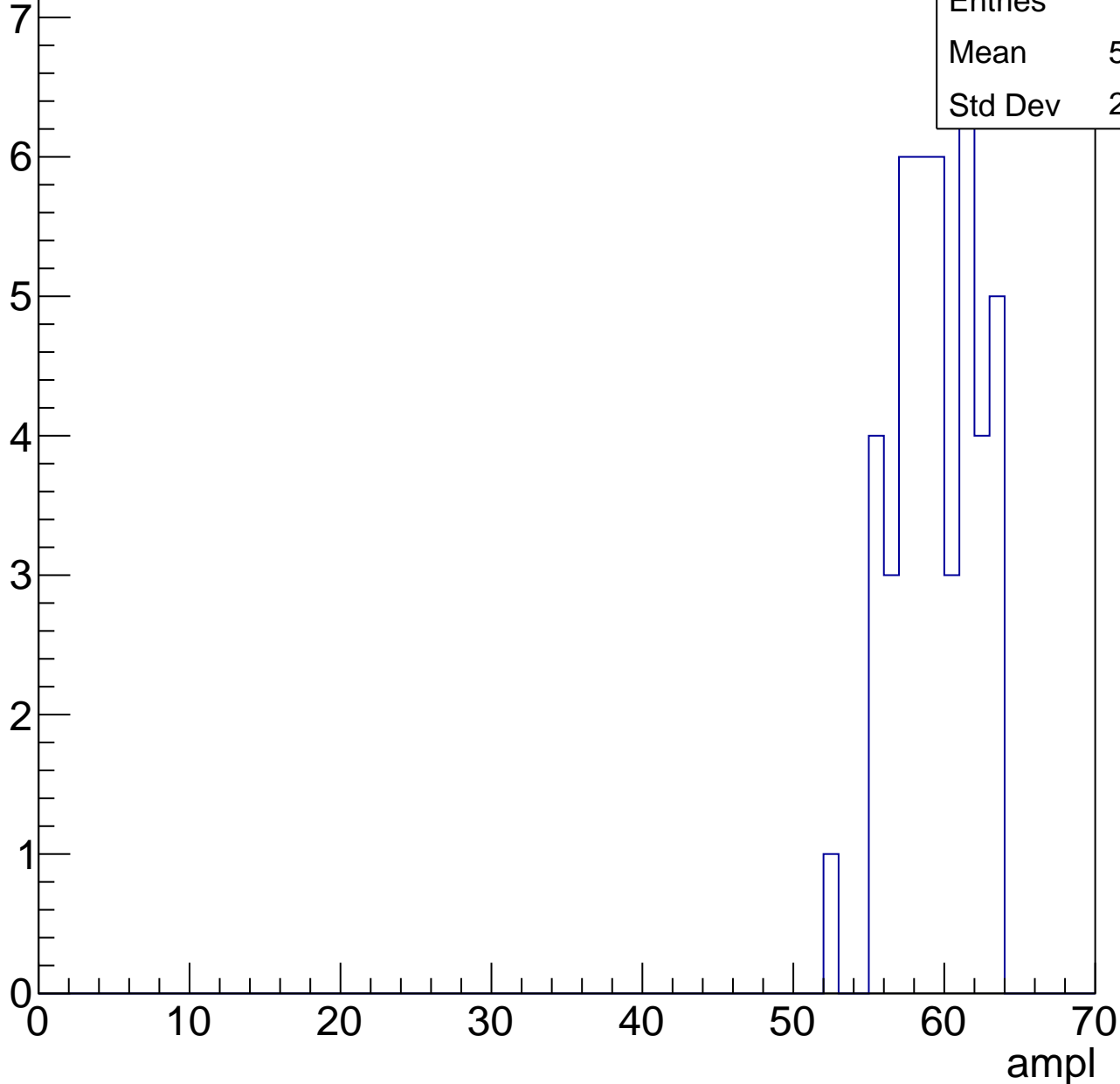
Entries	71
Mean	53.11
Std Dev	3.927

# B1L103S, U3-ch0, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	45
Mean	58.98
Std Dev	2.654

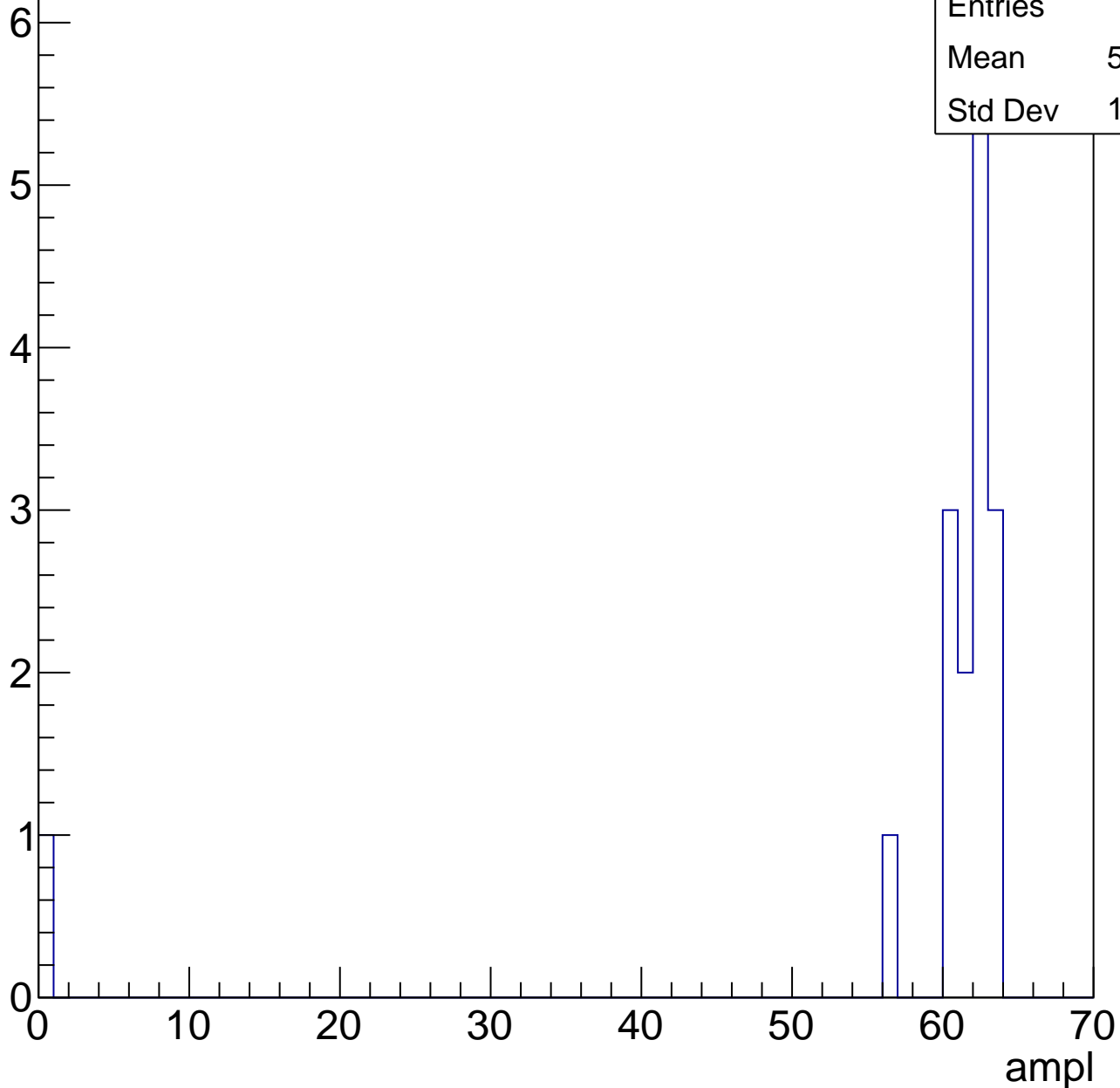


# B1L103S, U3-ch0, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	16
Mean	57.44
Std Dev	14.92

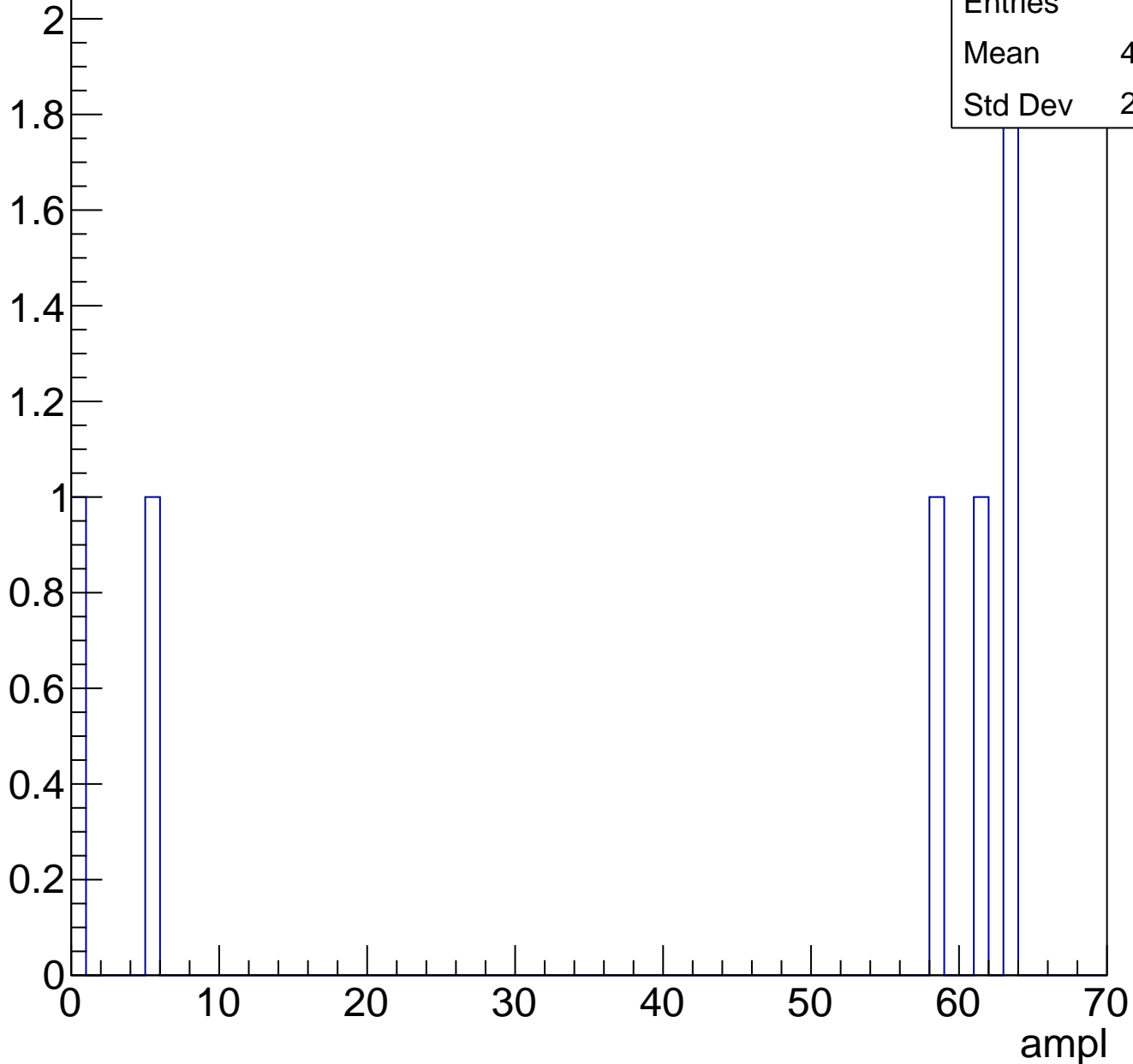




# B1L103S, U3-ch0, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch1, adc0

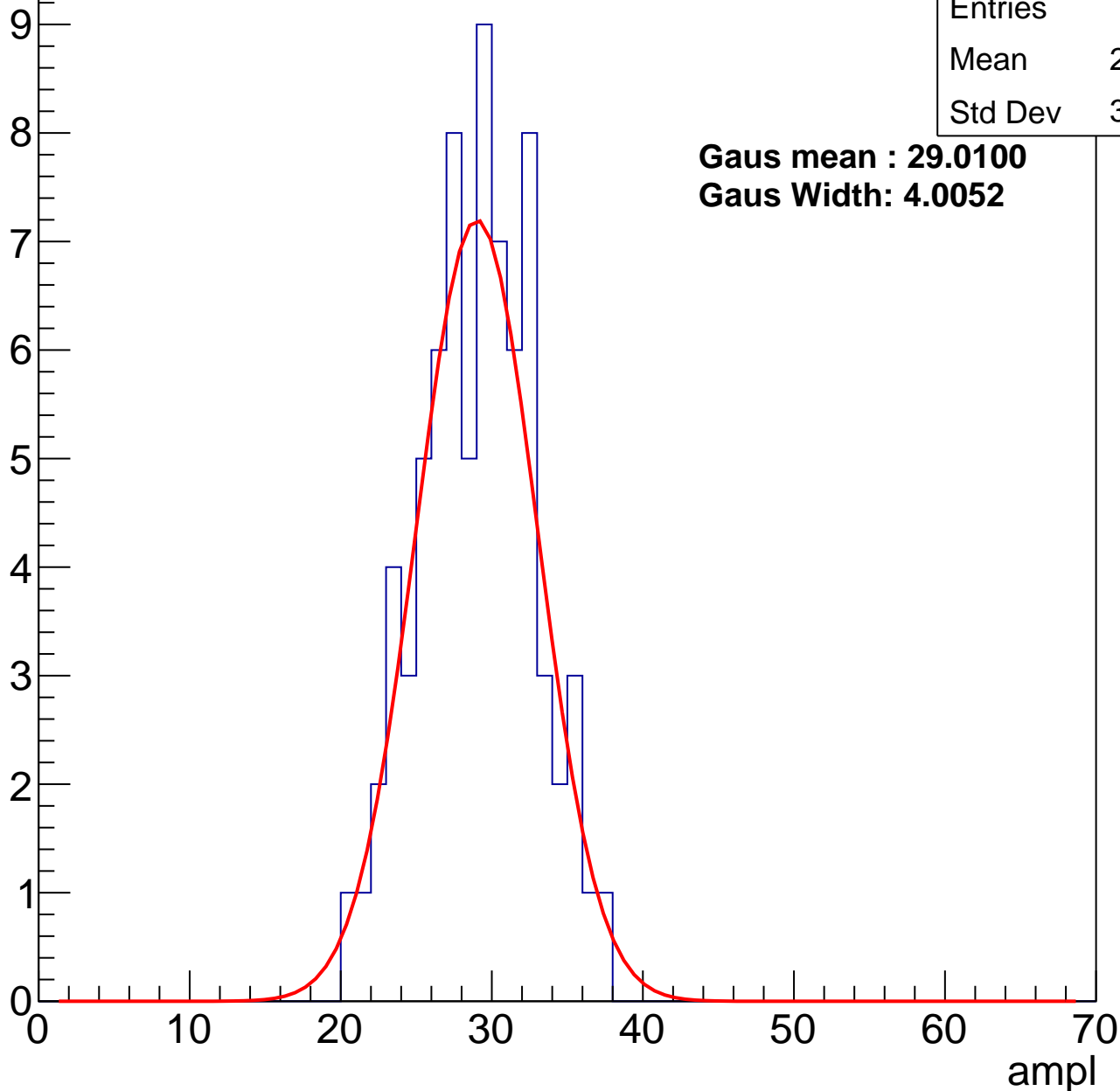
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	28.59
Std Dev	3.728

**Gaus mean : 29.0100**

**Gaus Width: 4.0052**



# B1L103S, U3-ch1, adc1

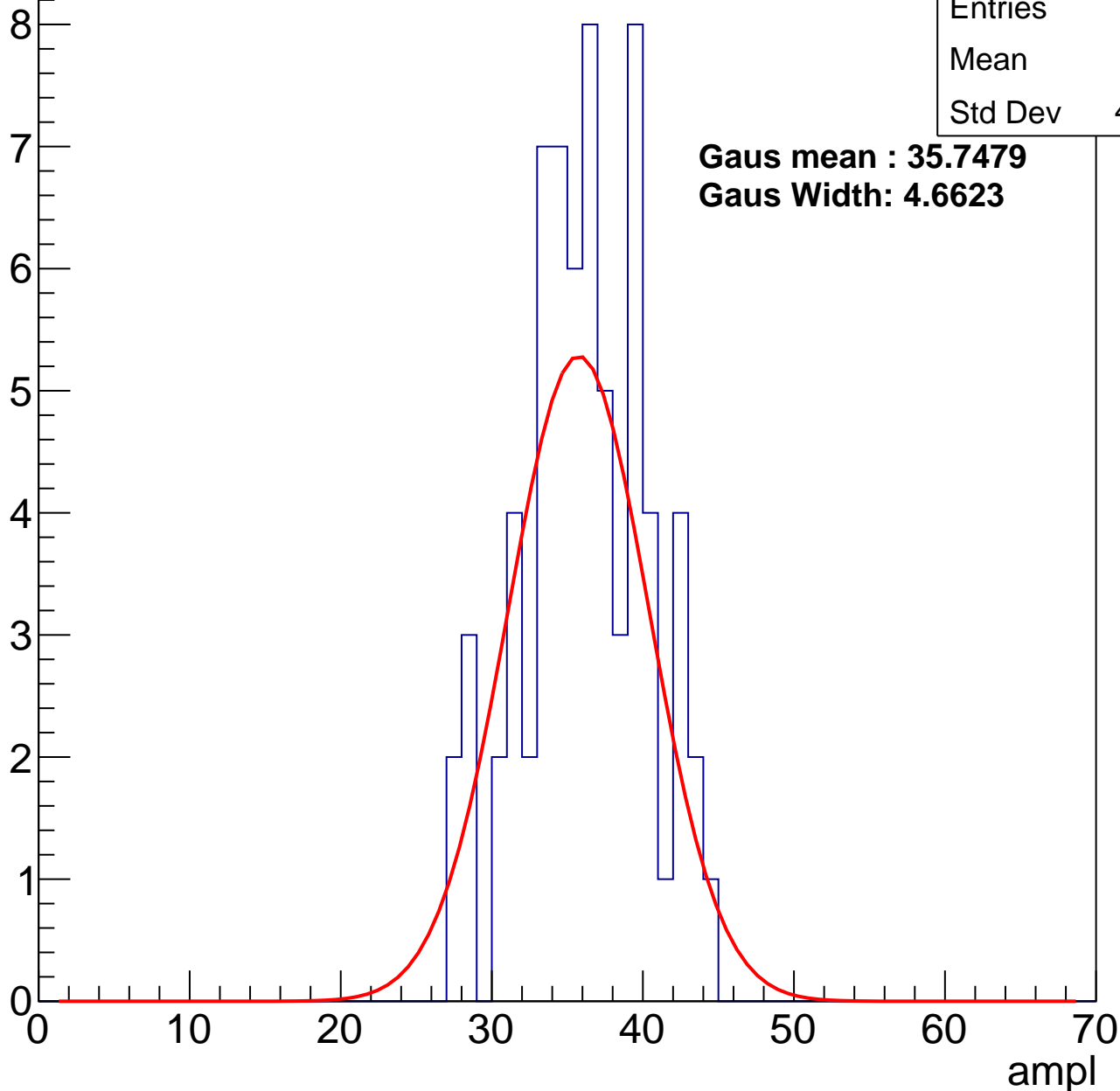
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	35.7
Std Dev	4.051

**Gaus mean : 35.7479**

**Gaus Width: 4.6623**



# B1L103S, U3-ch1, adc2

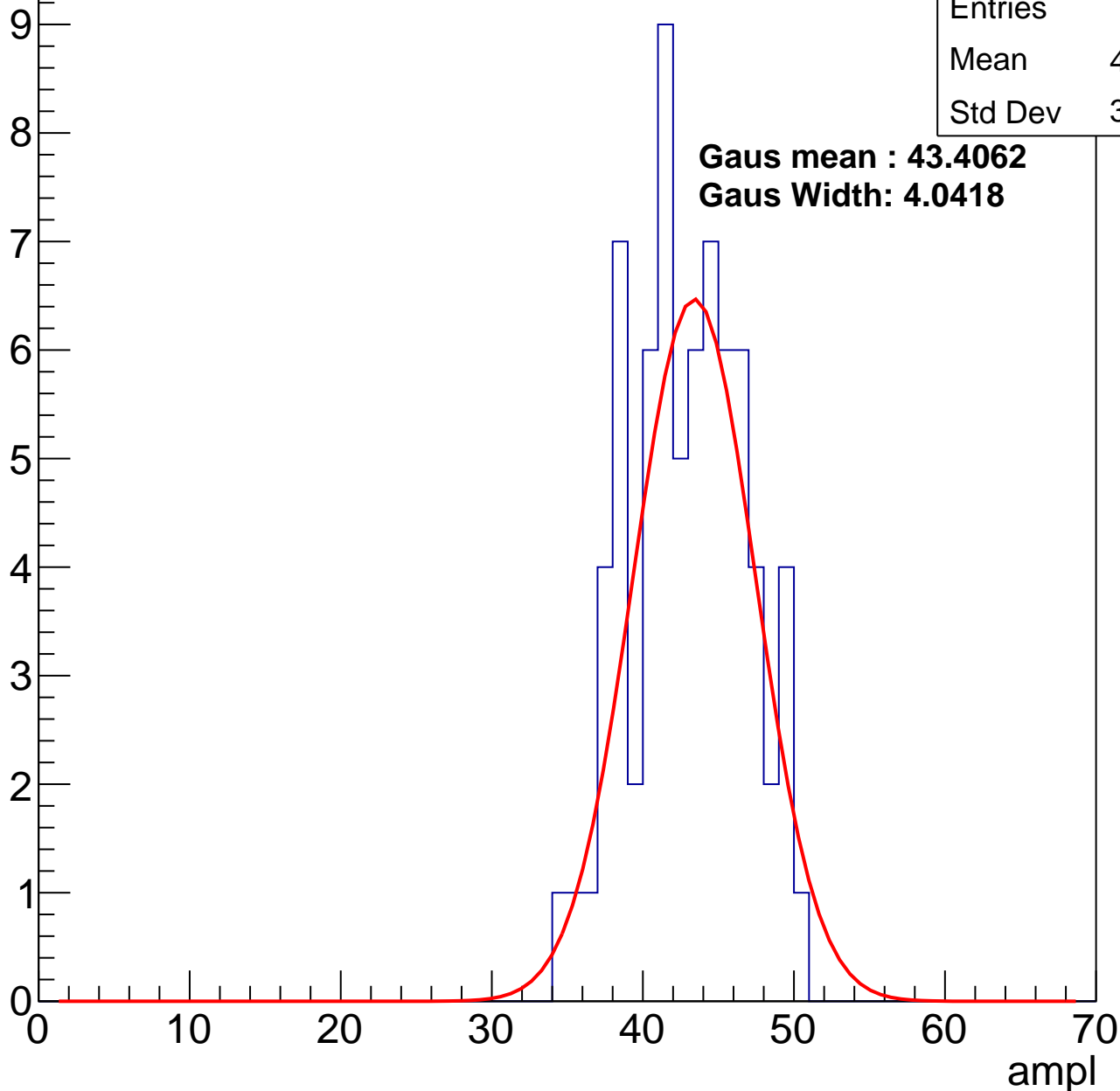
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	42.47
Std Dev	3.749

**Gaus mean : 43.4062**

**Gaus Width: 4.0418**

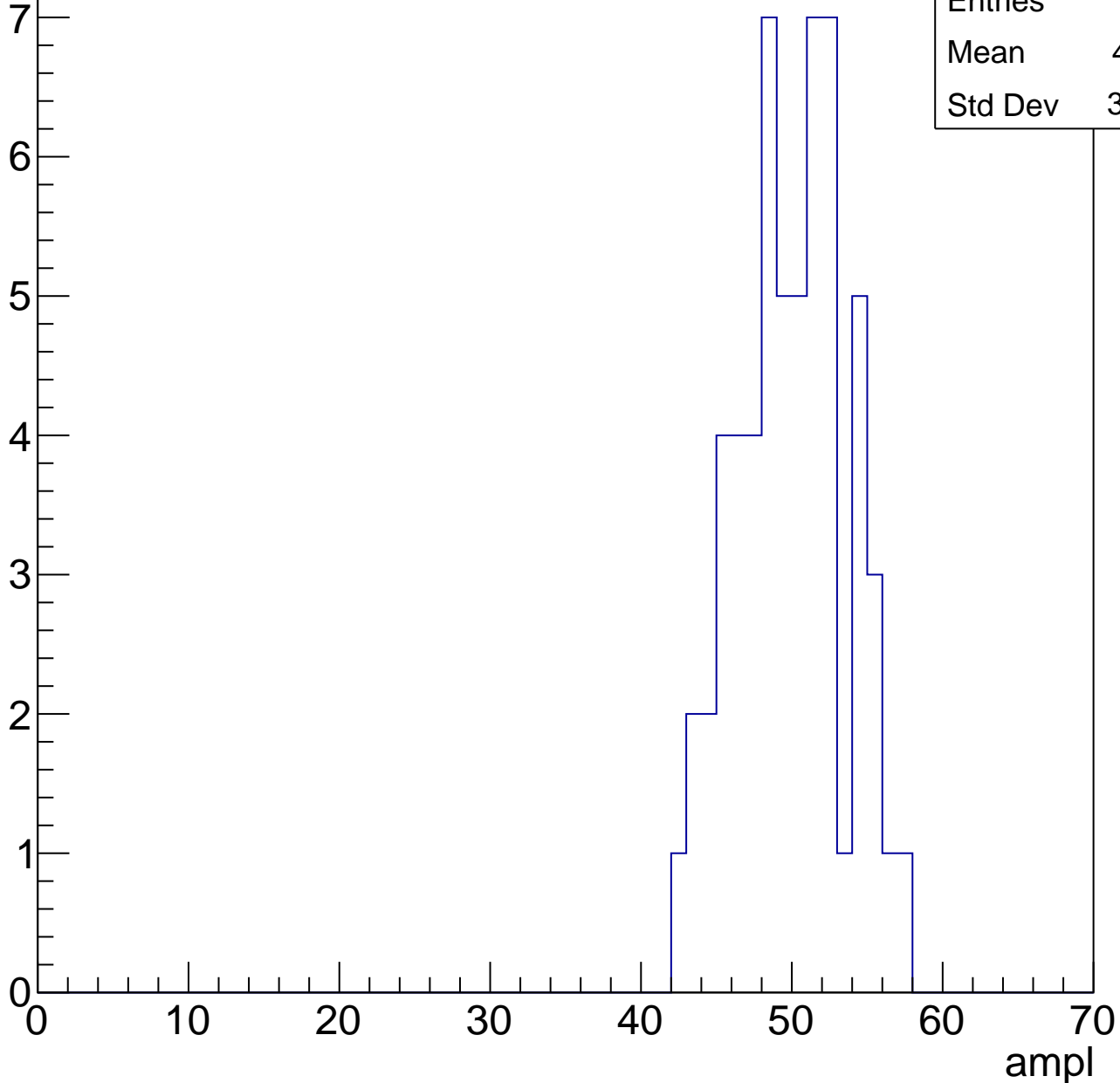


# B1L103S, U3-ch1, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

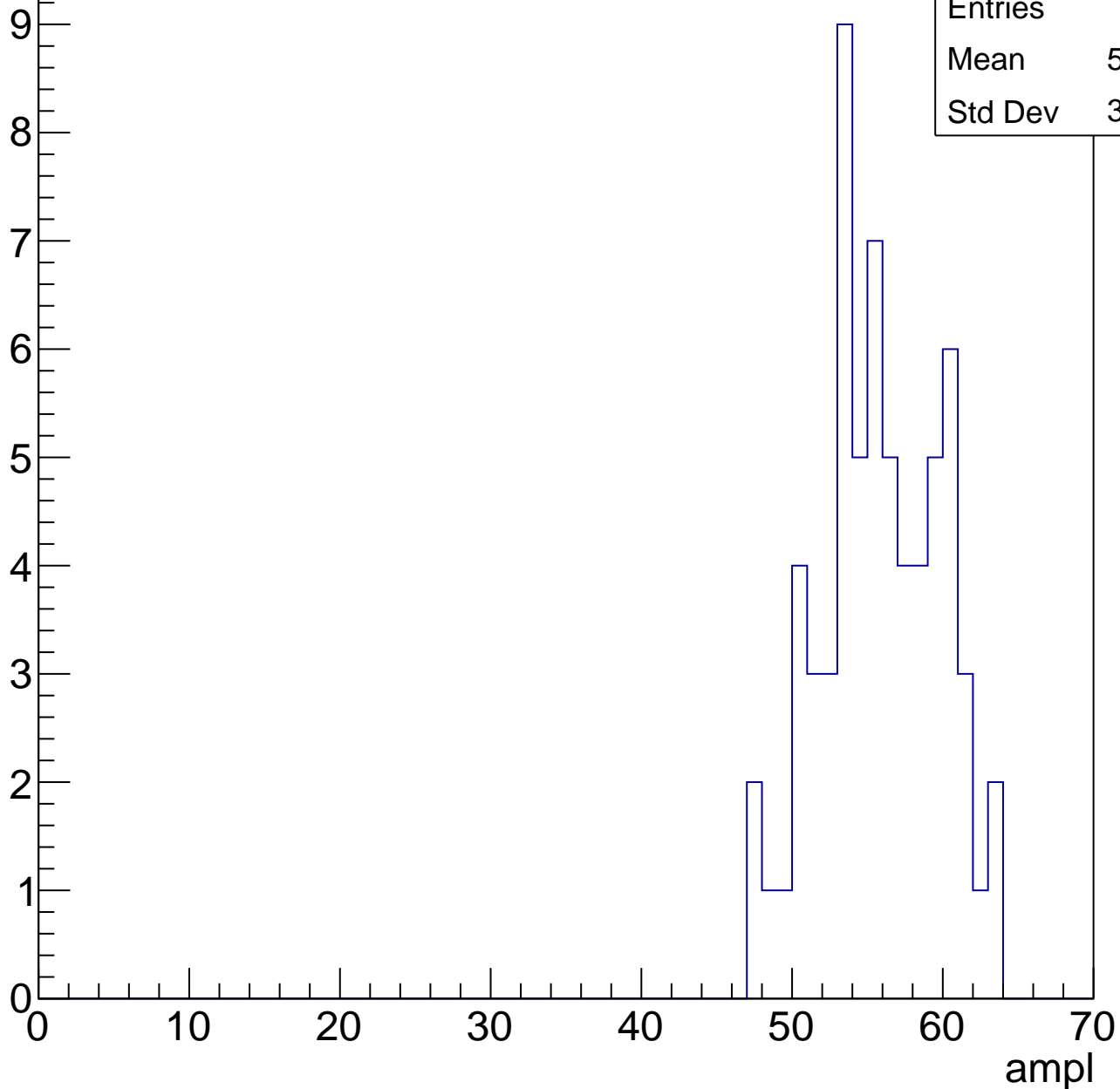
Entries	59
Mean	49.51
Std Dev	3.534



# B1L103S, U3-ch1, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



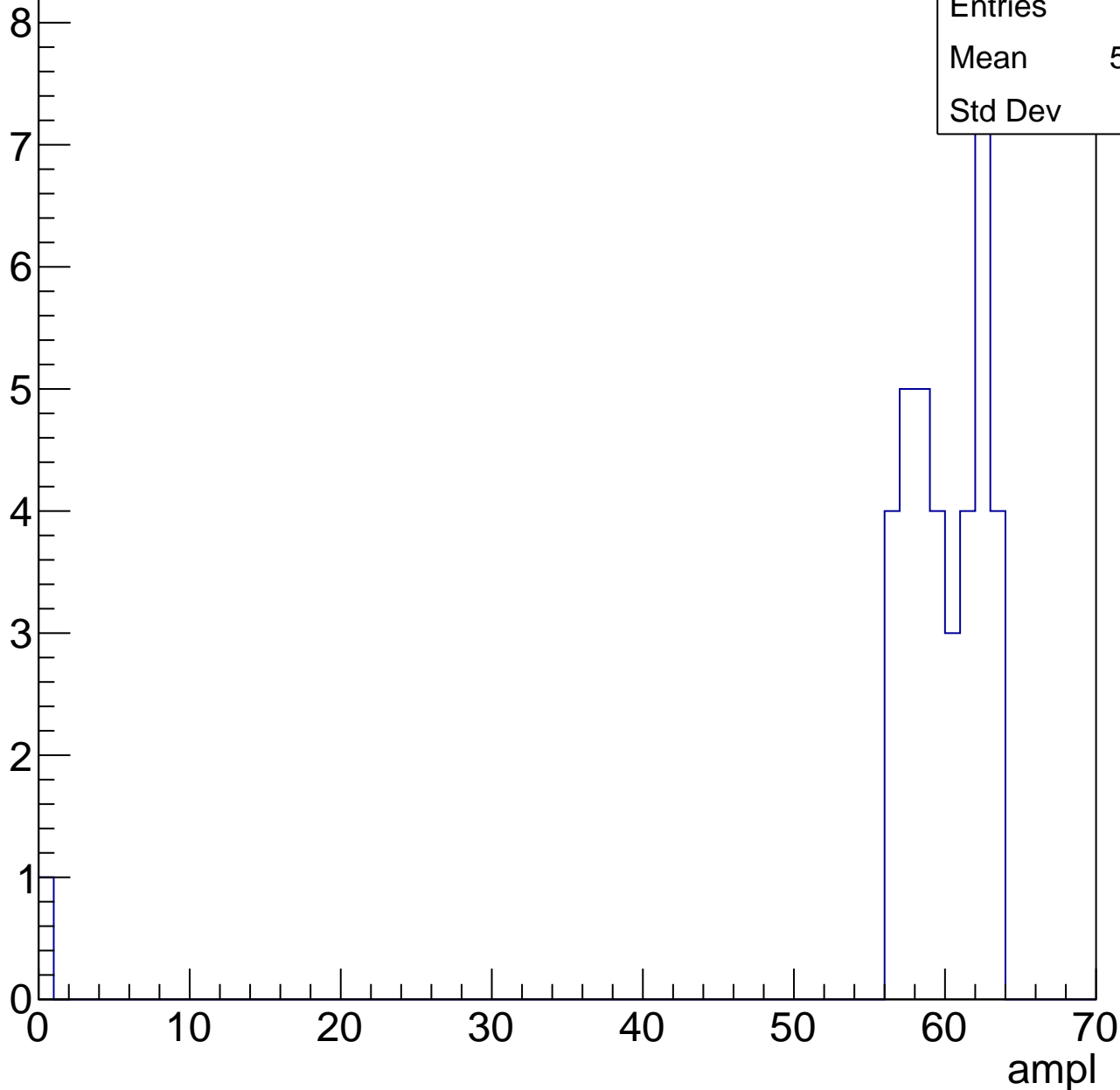
Entries	65
Mean	55.35
Std Dev	3.908

# B1L103S, U3-ch1, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

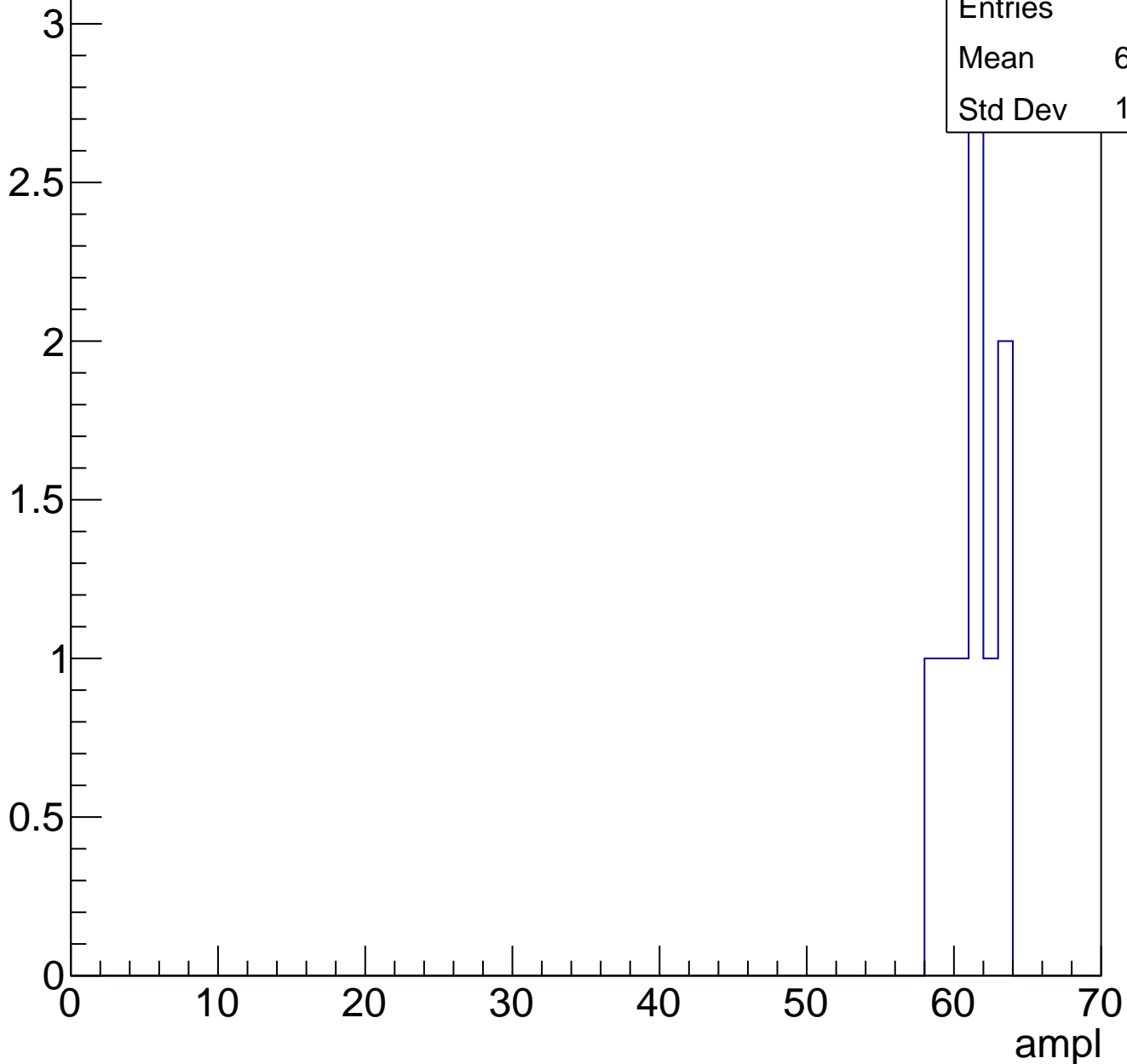
Entries	38
Mean	58.08
Std Dev	9.82



# B1L103S, U3-ch1, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	9
Mean	60.89
Std Dev	1.595



# B1L103S, U3-ch1, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch2, adc0

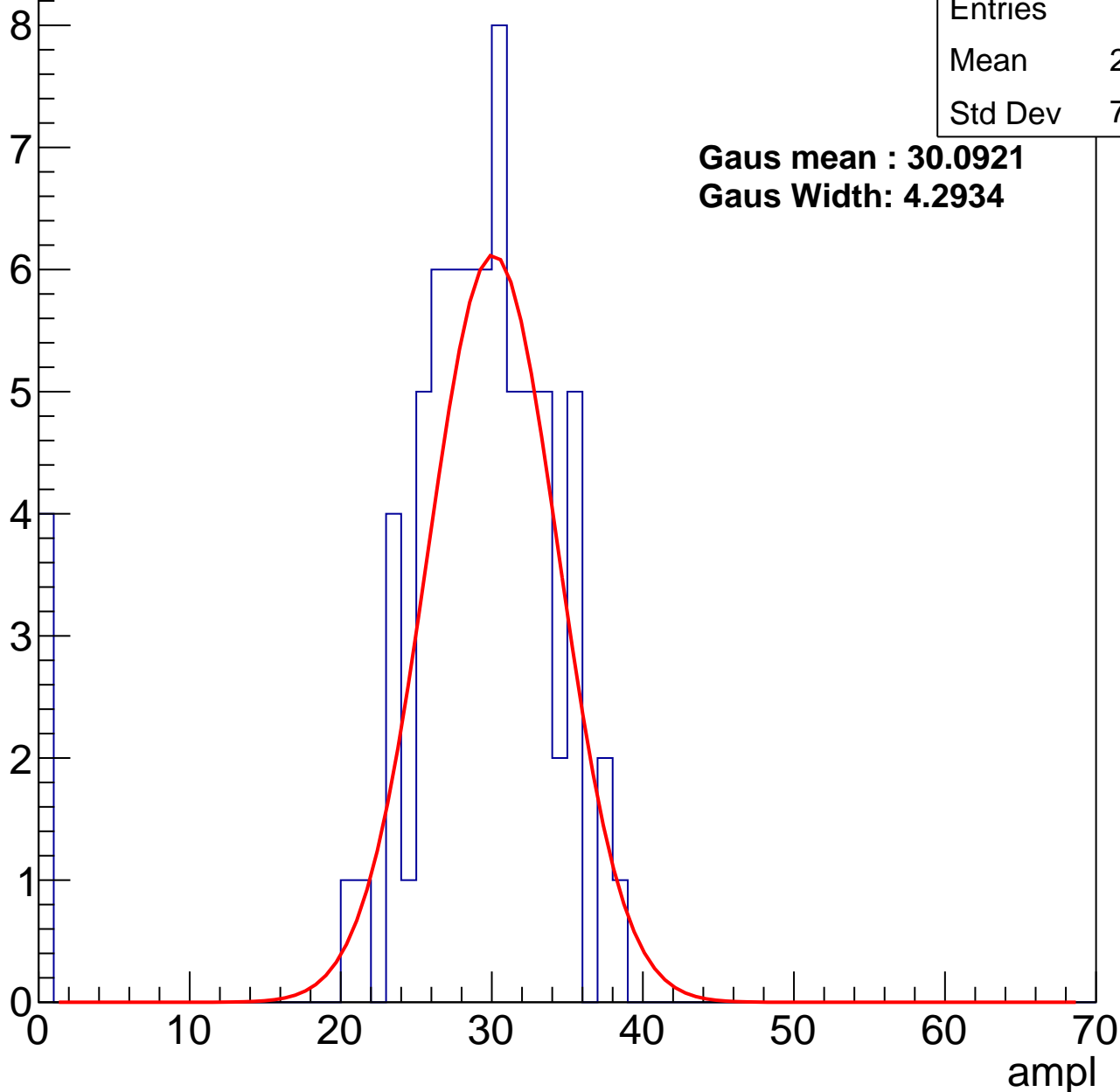
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	27.63
Std Dev	7.672

**Gaus mean : 30.0921**

**Gaus Width: 4.2934**



# B1L103S, U3-ch2, adc1

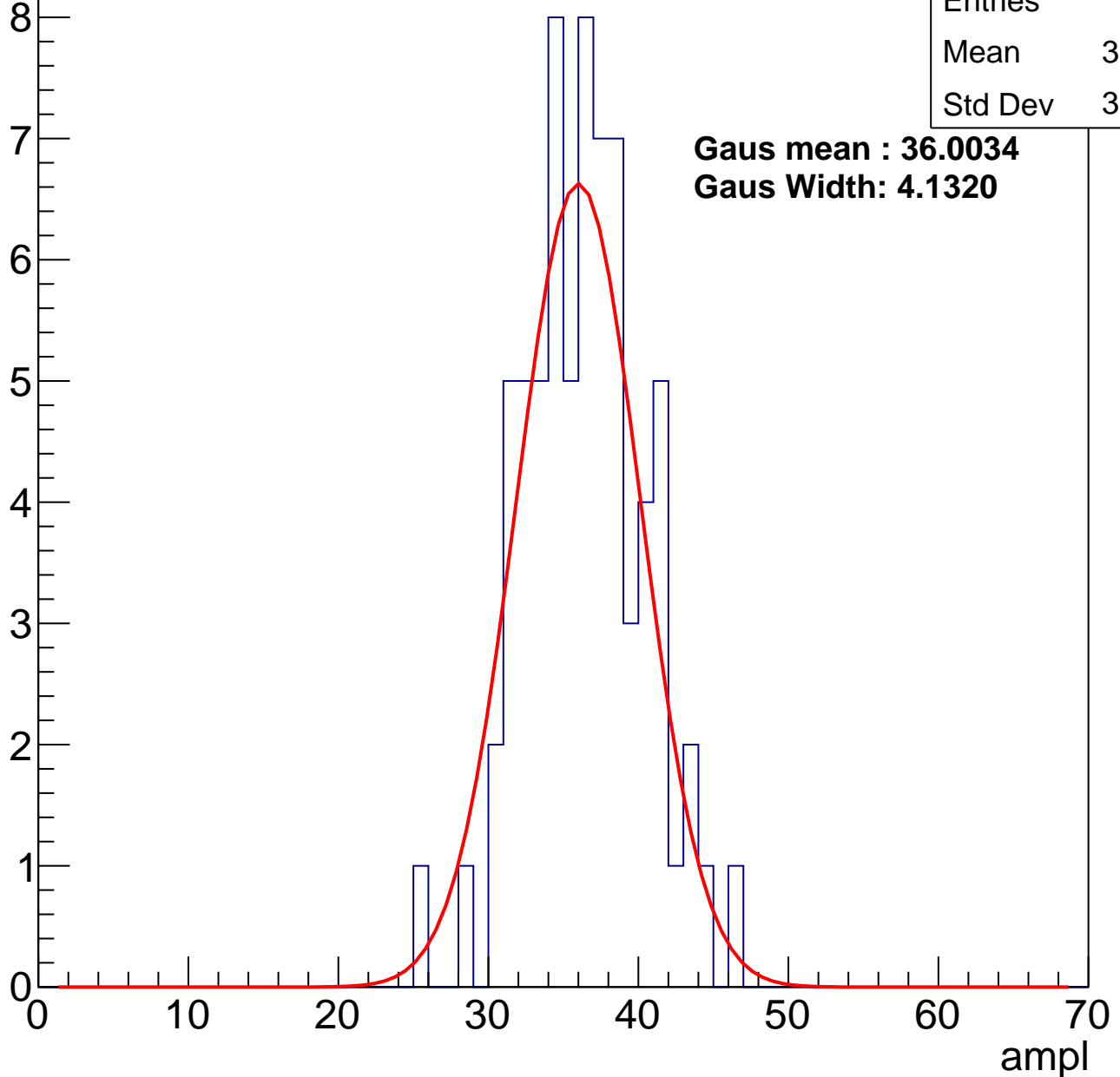
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	35.96
Std Dev	3.923

**Gaus mean : 36.0034**

**Gaus Width: 4.1320**



# B1L103S, U3-ch2, adc2

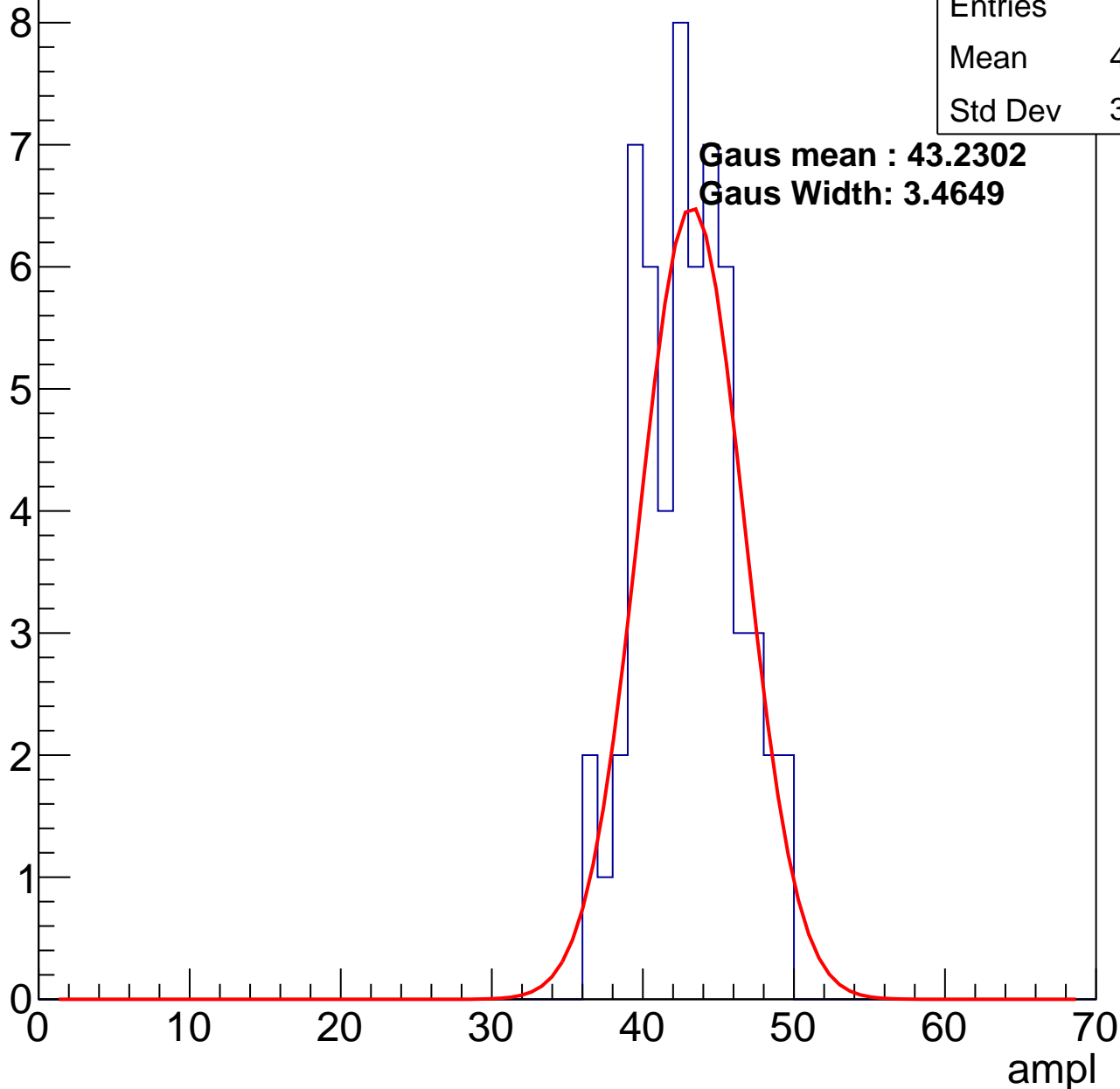
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	42.49
Std Dev	3.154

**Gaus mean : 43.2302**

**Gaus Width: 3.4649**

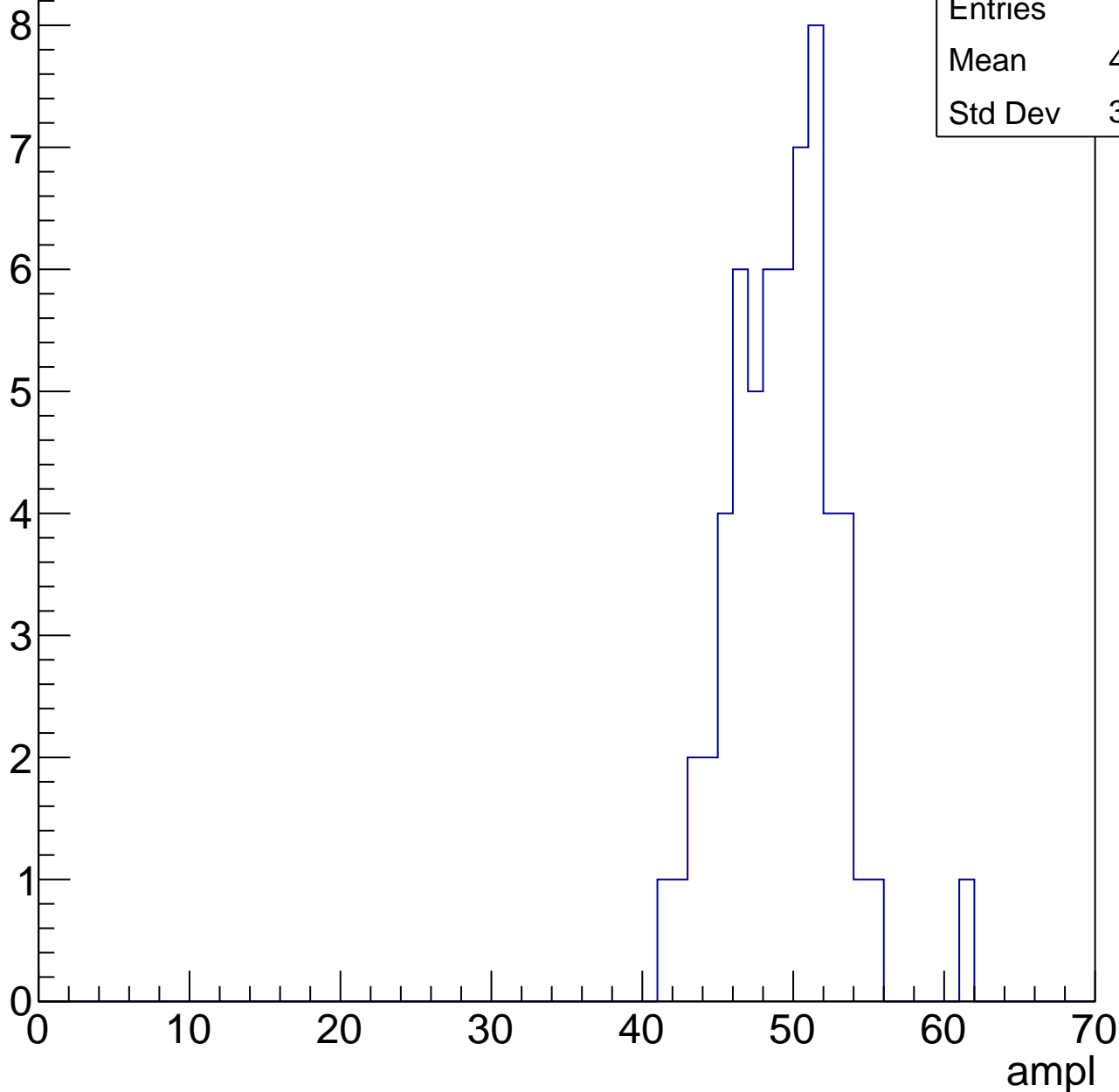


# B1L103S, U3-ch2, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

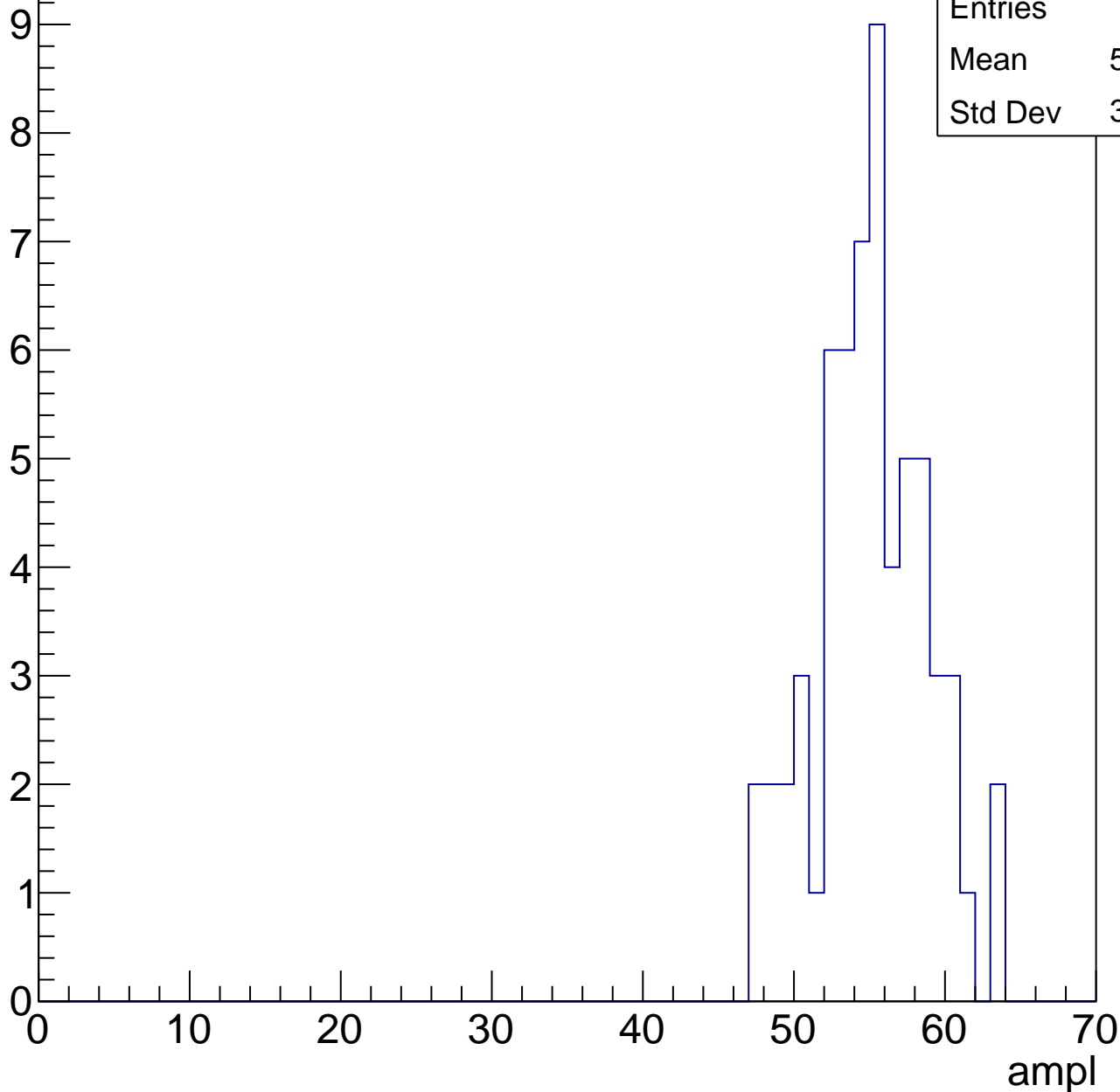
Entries	59
Mean	48.78
Std Dev	3.494



# B1L103S, U3-ch2, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

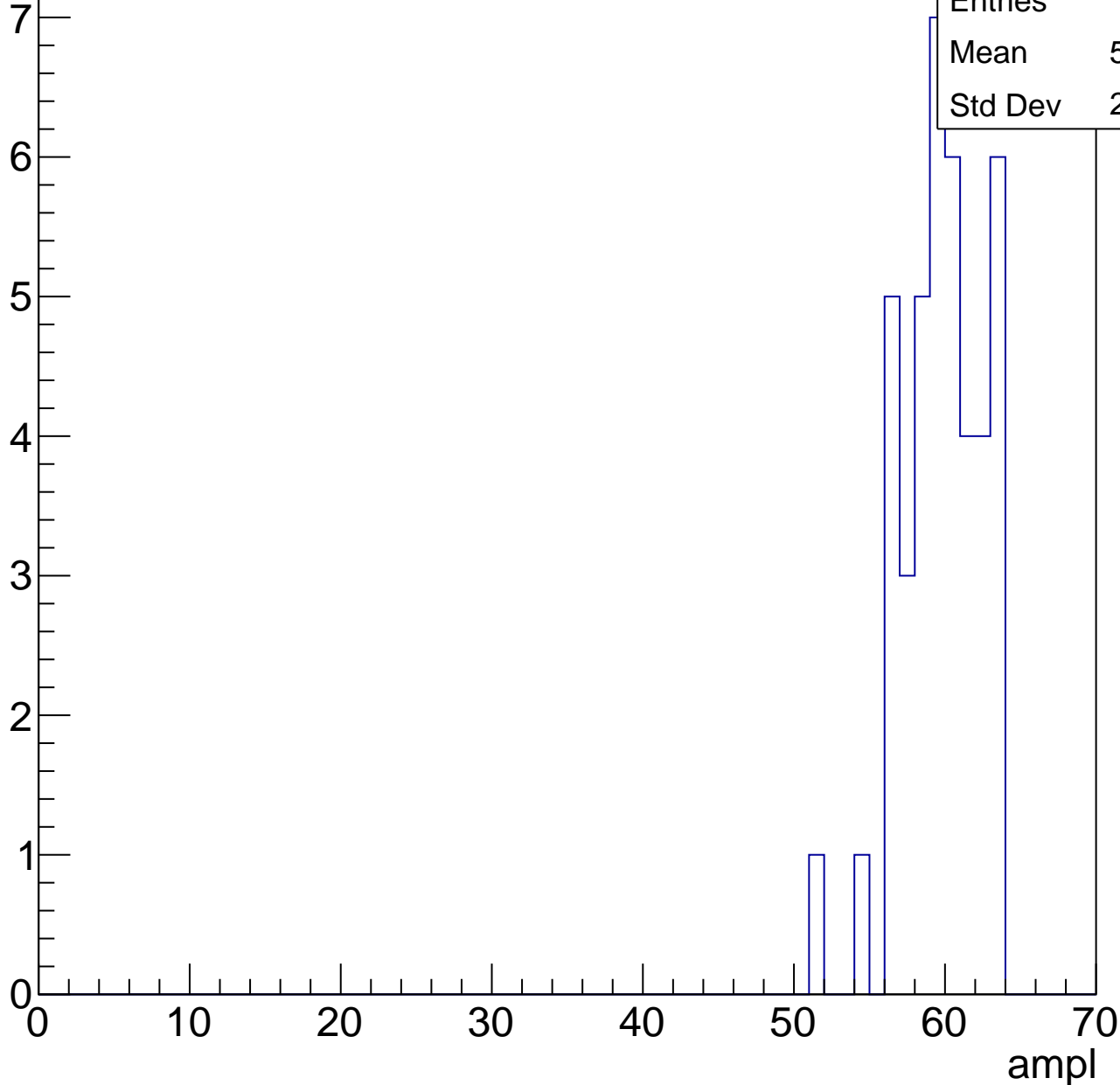
Entry



# B1L103S, U3-ch2, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

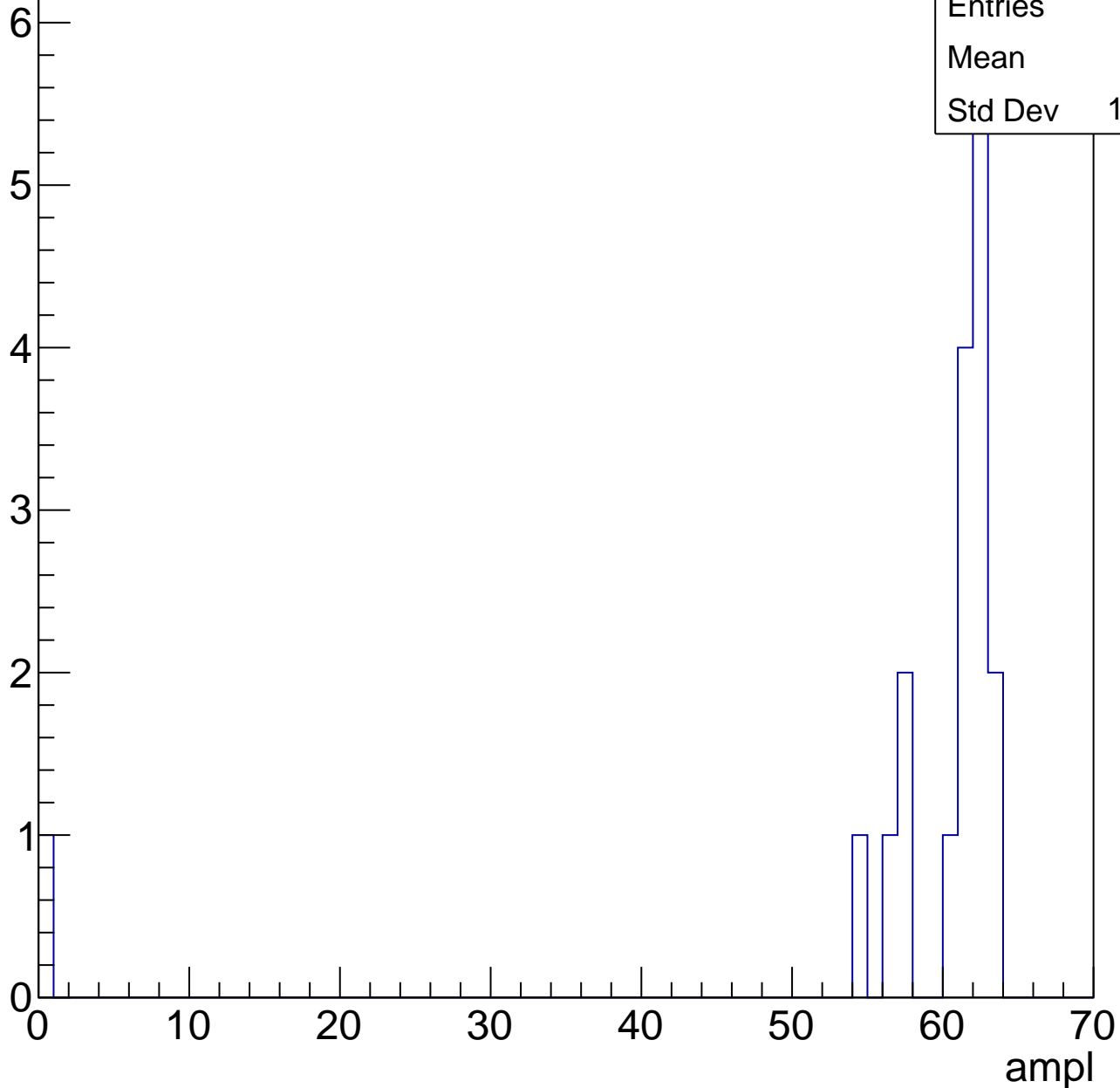


# B1L103S, U3-ch2, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	18
Mean	57
Std Dev	14.05





# B1L103S, U3-ch2, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U3-ch3, adc0

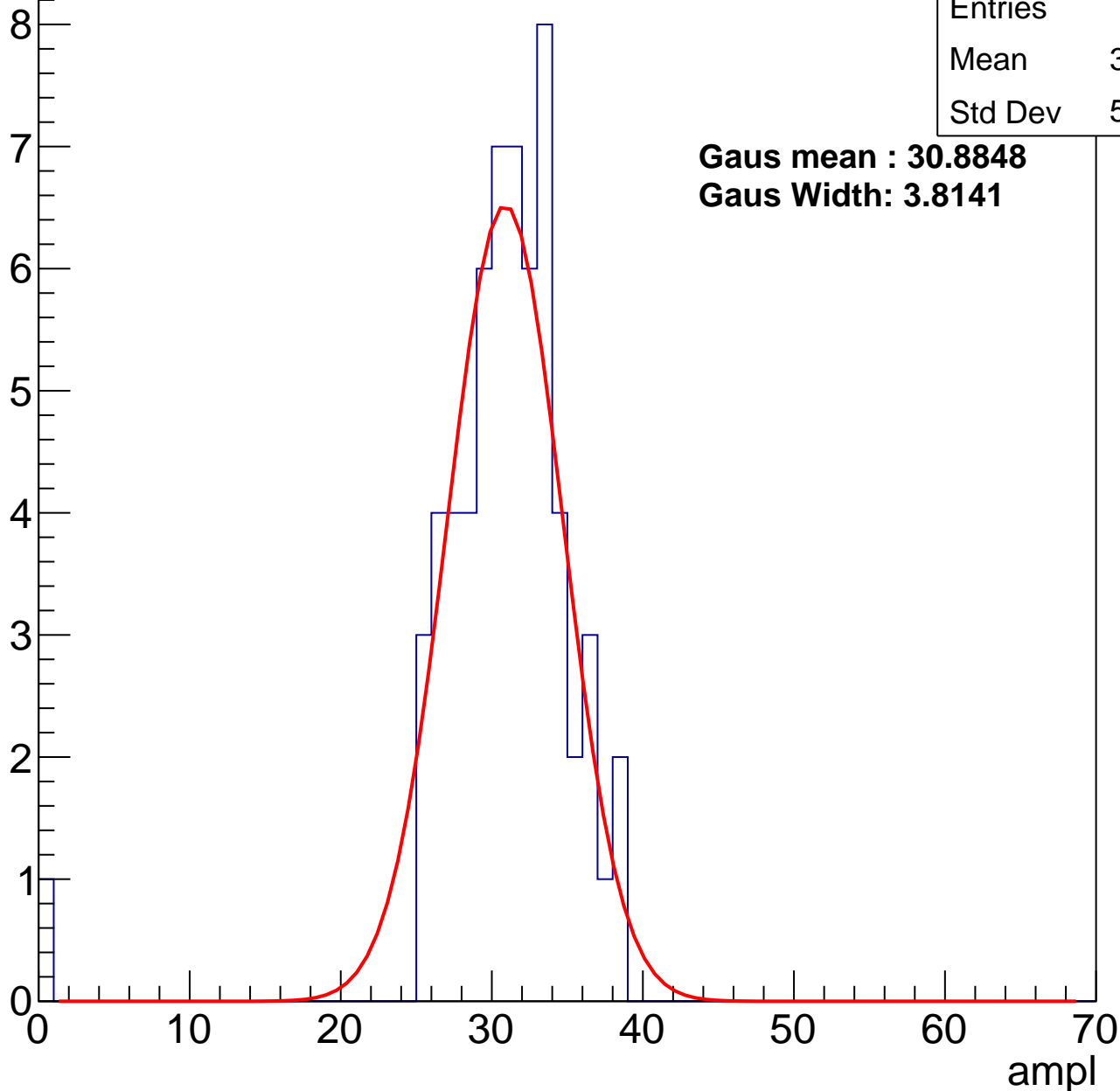
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	30.37
Std Dev	5.065

**Gaus mean : 30.8848**

**Gaus Width: 3.8141**



# B1L103S, U3-ch3, adc1

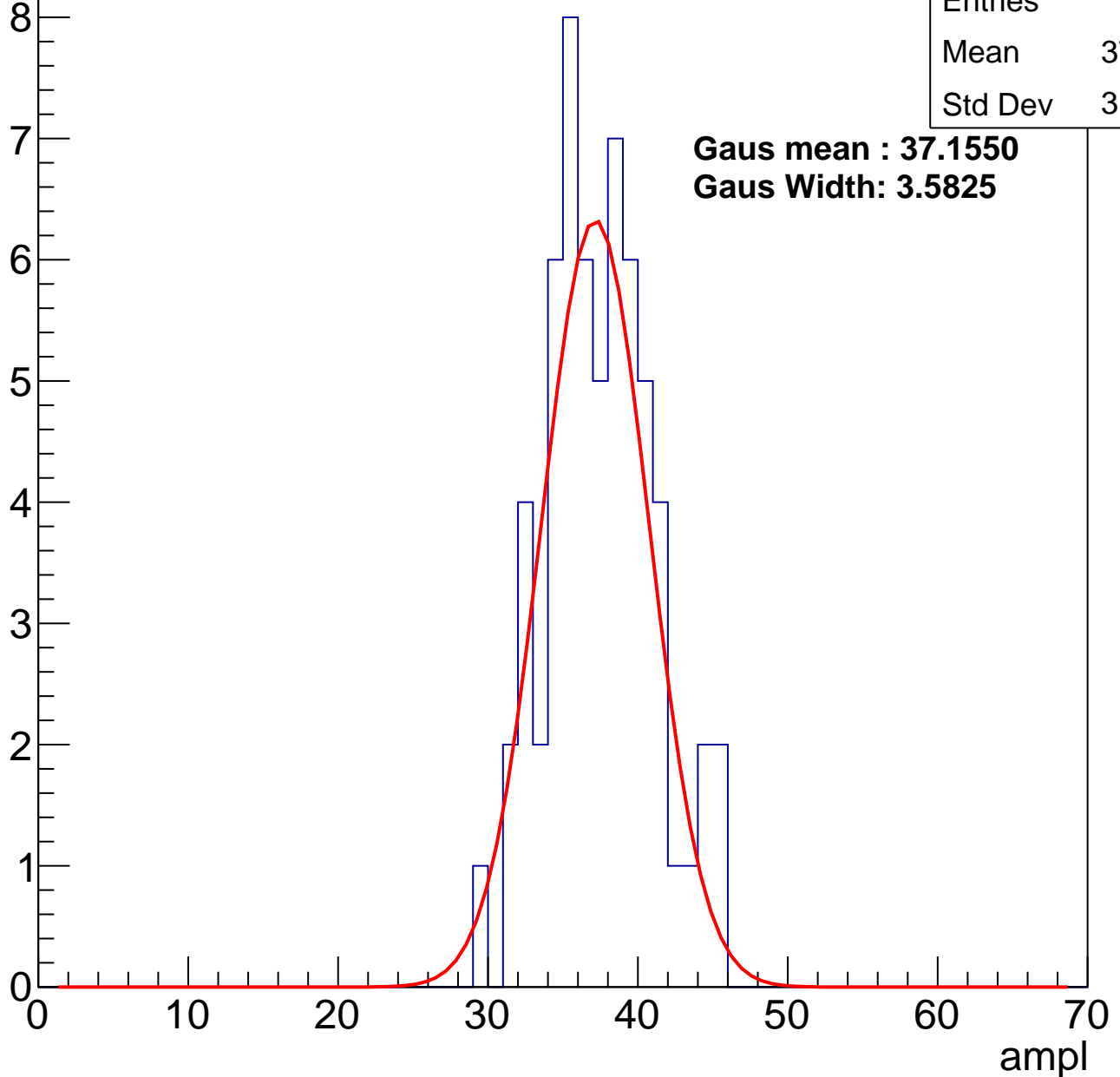
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	37.05
Std Dev	3.562

**Gaus mean : 37.1550**

**Gaus Width: 3.5825**



# B1L103S, U3-ch3, adc2

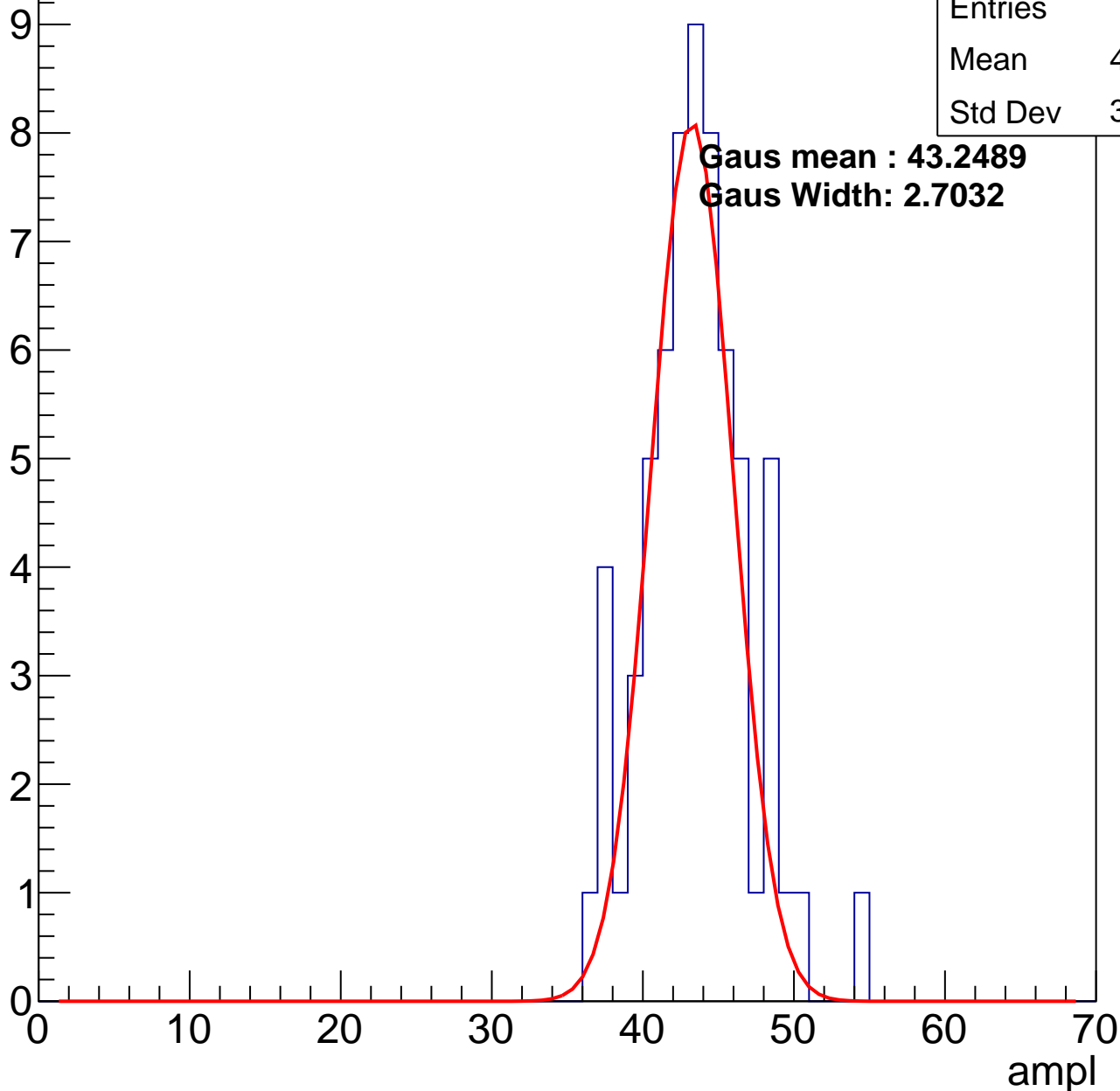
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	43.08
Std Dev	3.434

**Gaus mean : 43.2489**

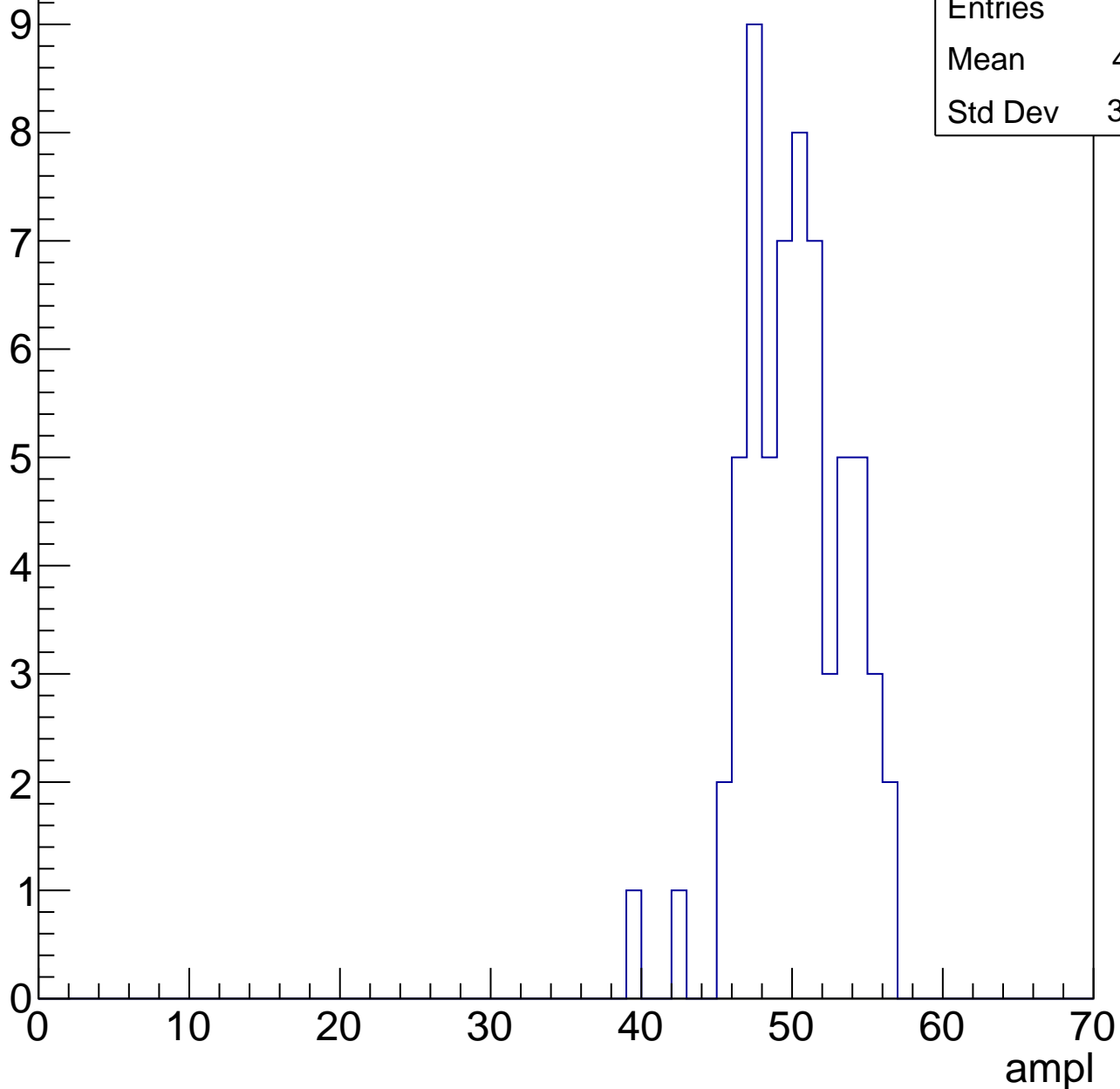
**Gaus Width: 2.7032**



# B1L103S, U3-ch3, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

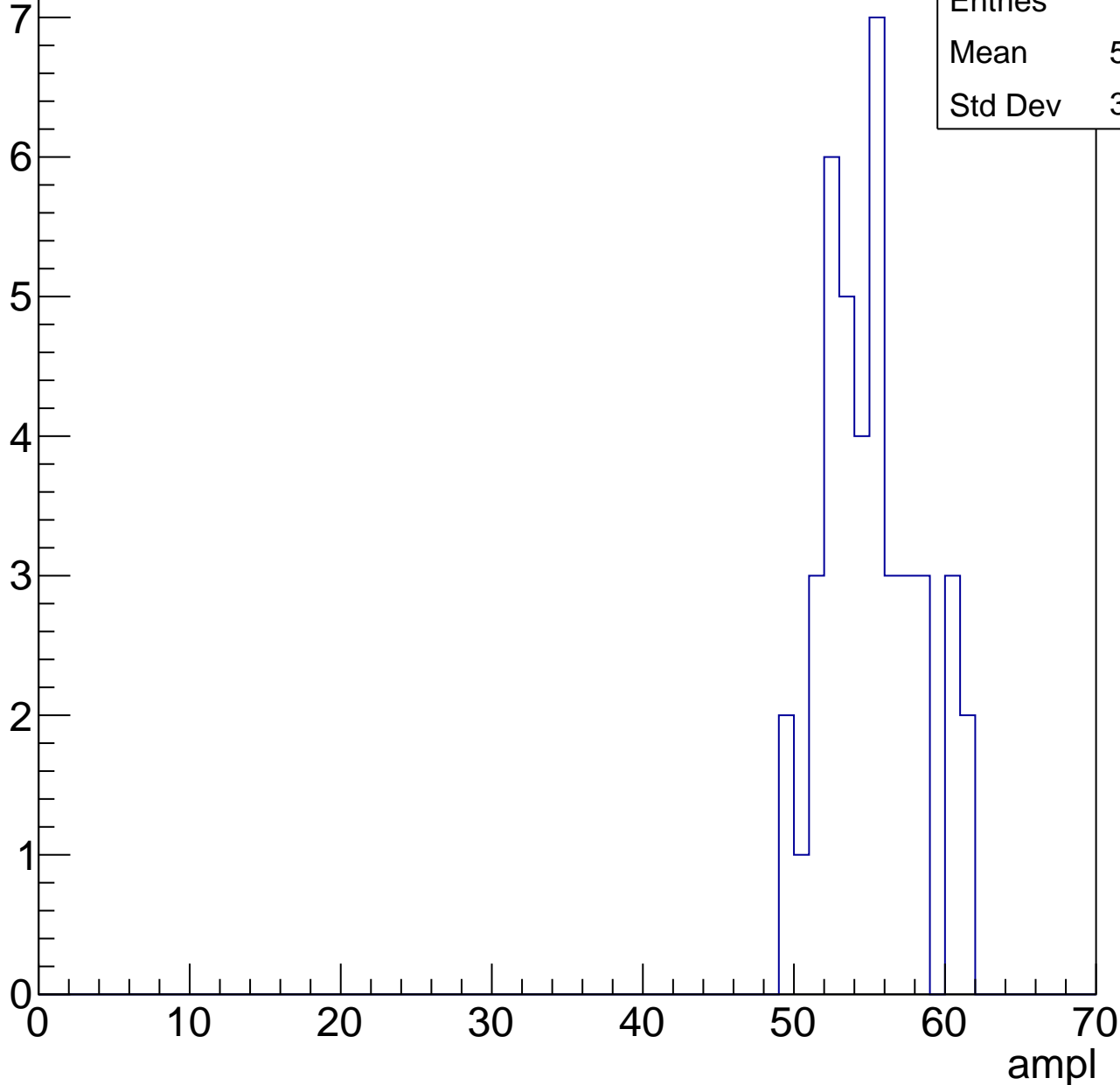


Entries	63
Mean	49.71
Std Dev	3.354

# B1L103S, U3-ch3, adc4

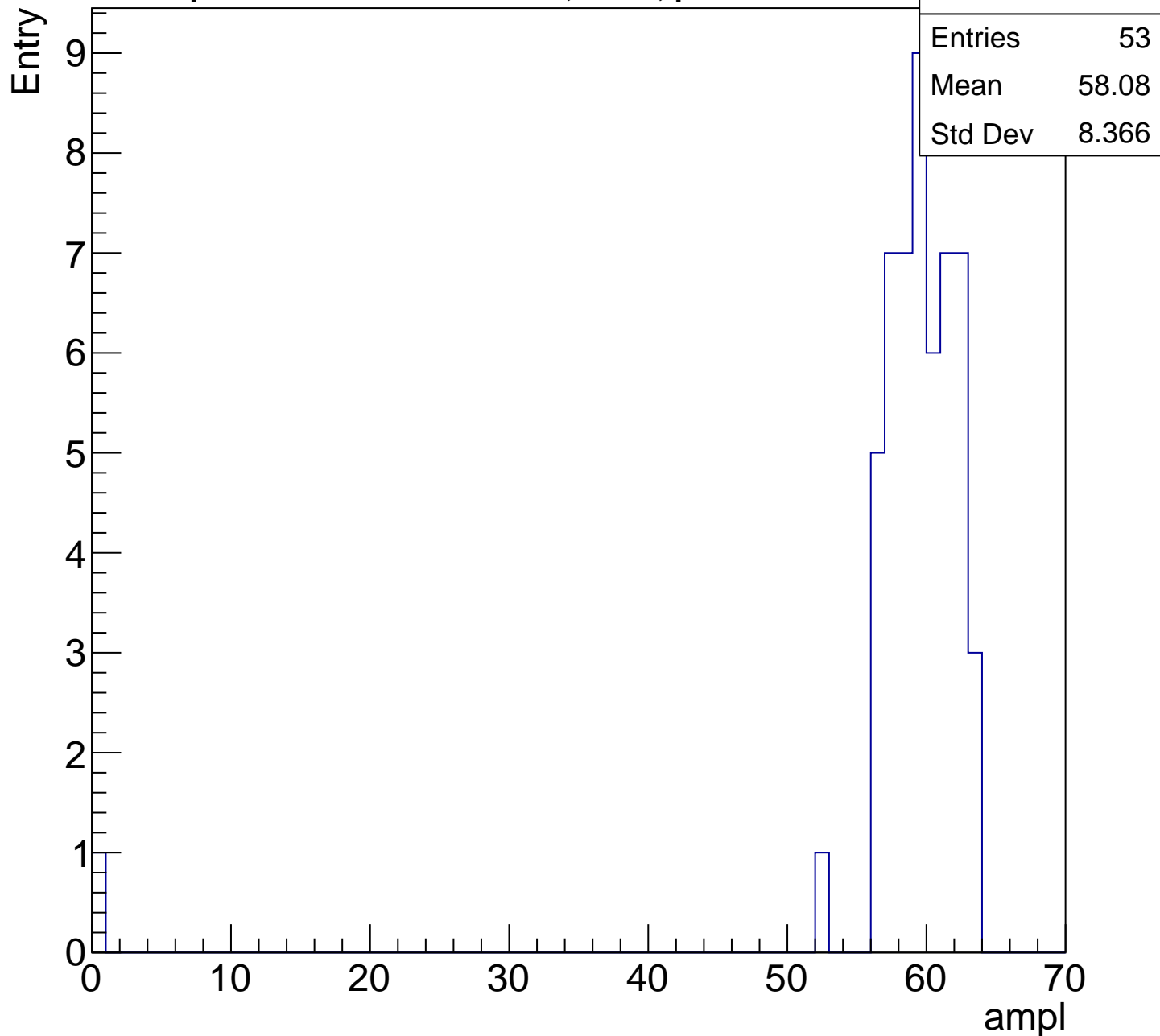
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch3, adc5

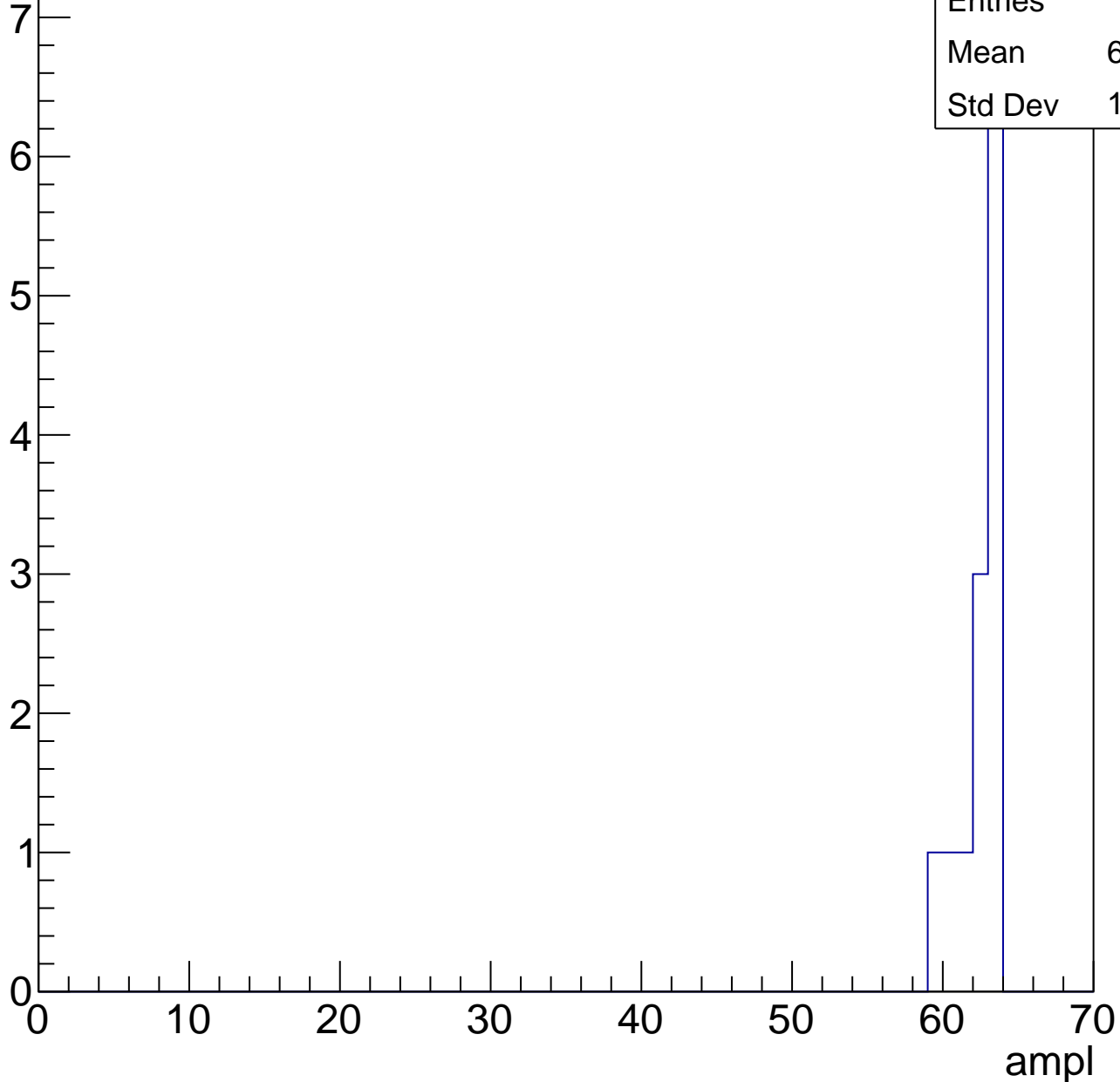
calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U3-ch3, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U3-ch3, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch4, adc0

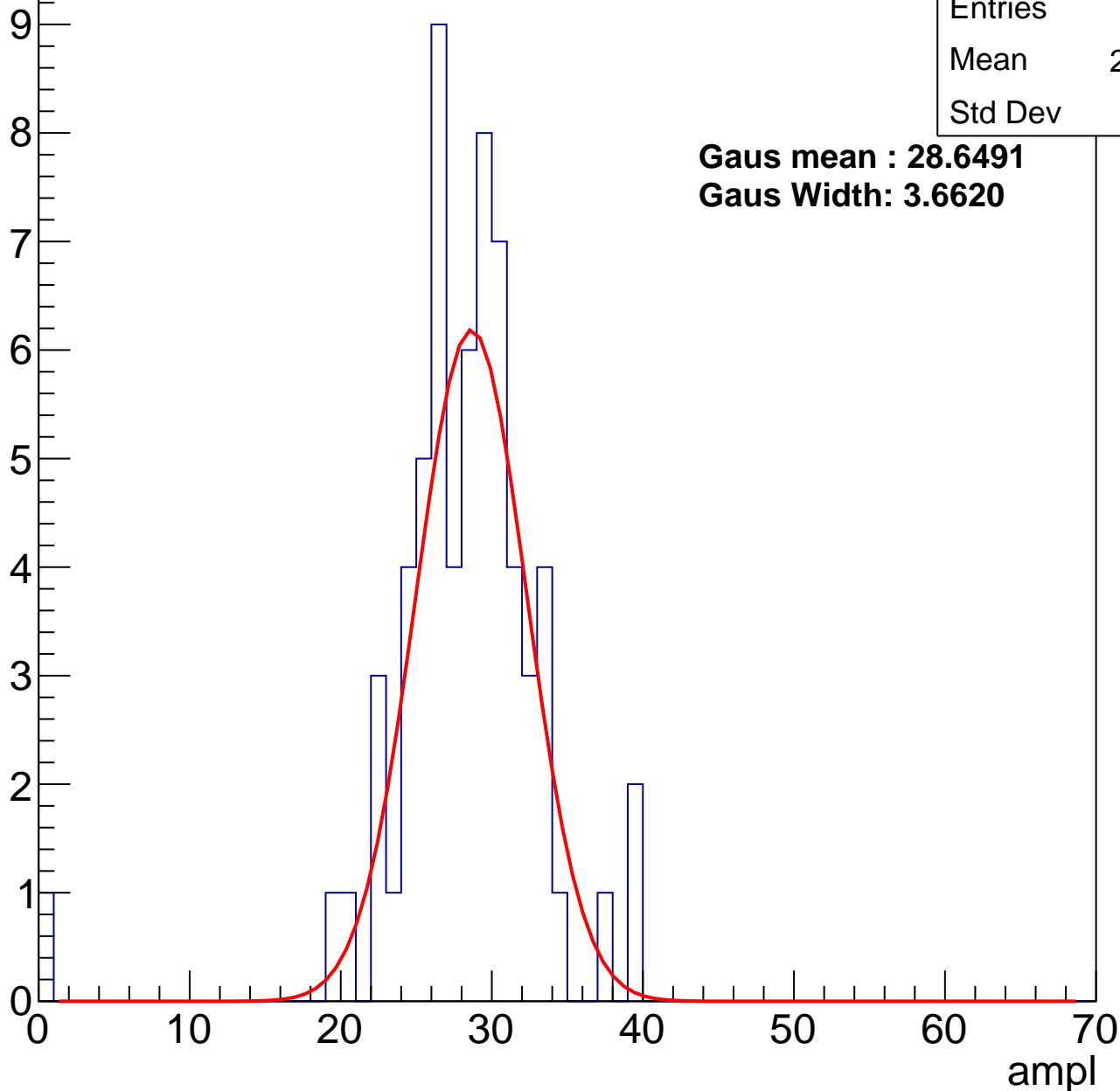
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	27.72
Std Dev	5.24

**Gaus mean : 28.6491**

**Gaus Width: 3.6620**



# B1L103S, U3-ch4, adc1

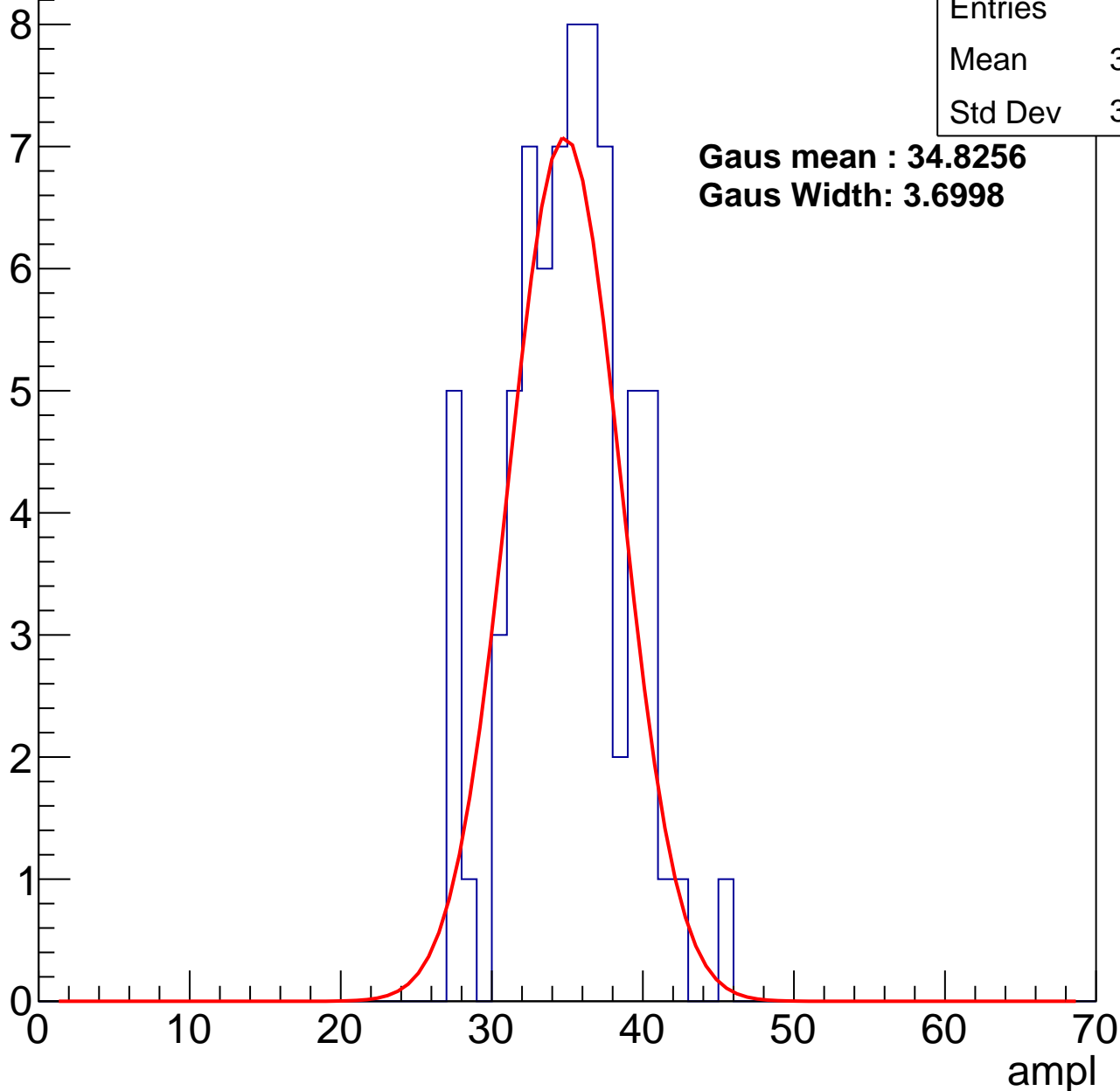
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	34.64
Std Dev	3.824

**Gaus mean : 34.8256**

**Gaus Width: 3.6998**



# B1L103S, U3-ch4, adc2

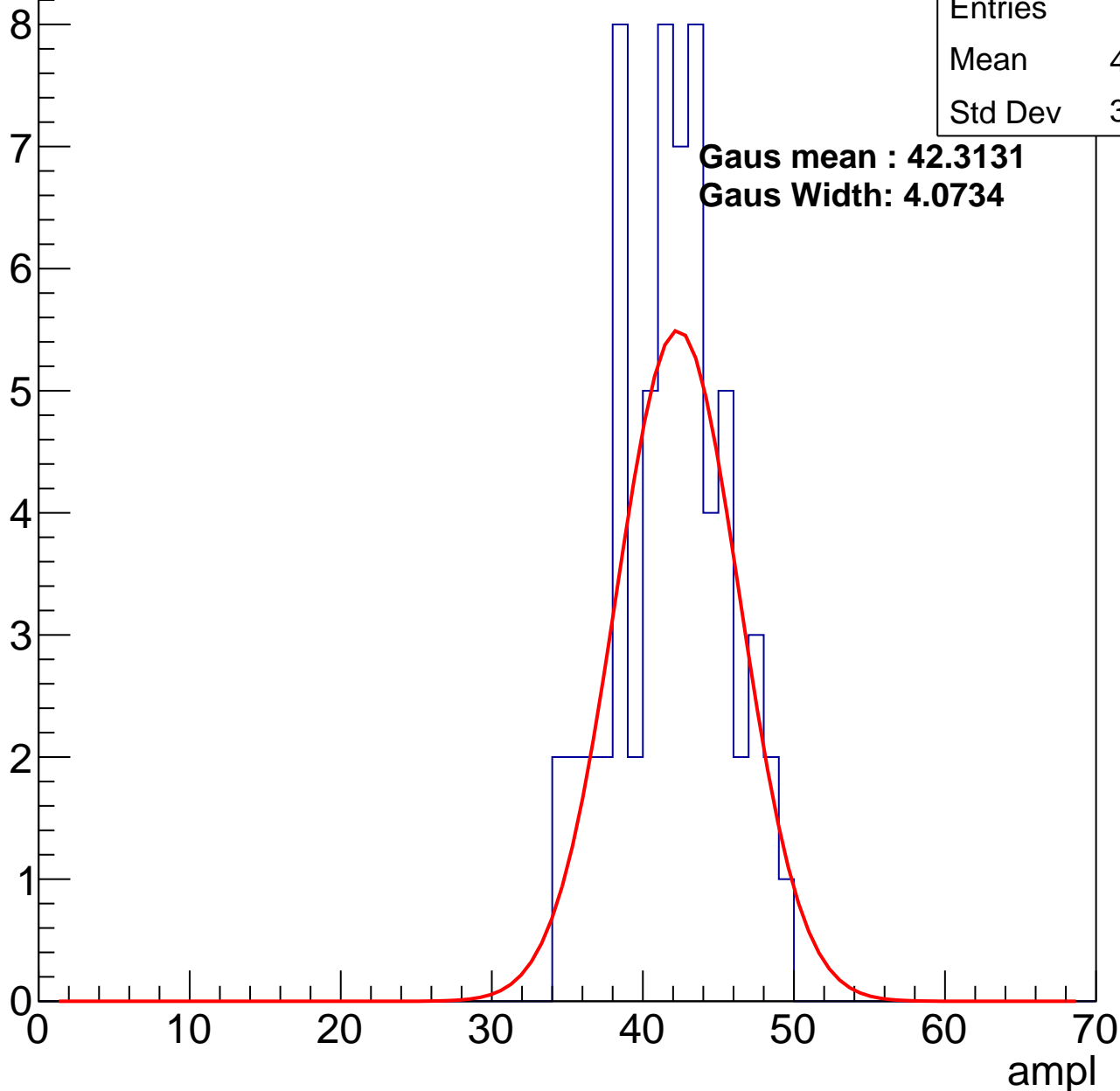
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	41.44
Std Dev	3.562

**Gaus mean : 42.3131**

**Gaus Width: 4.0734**

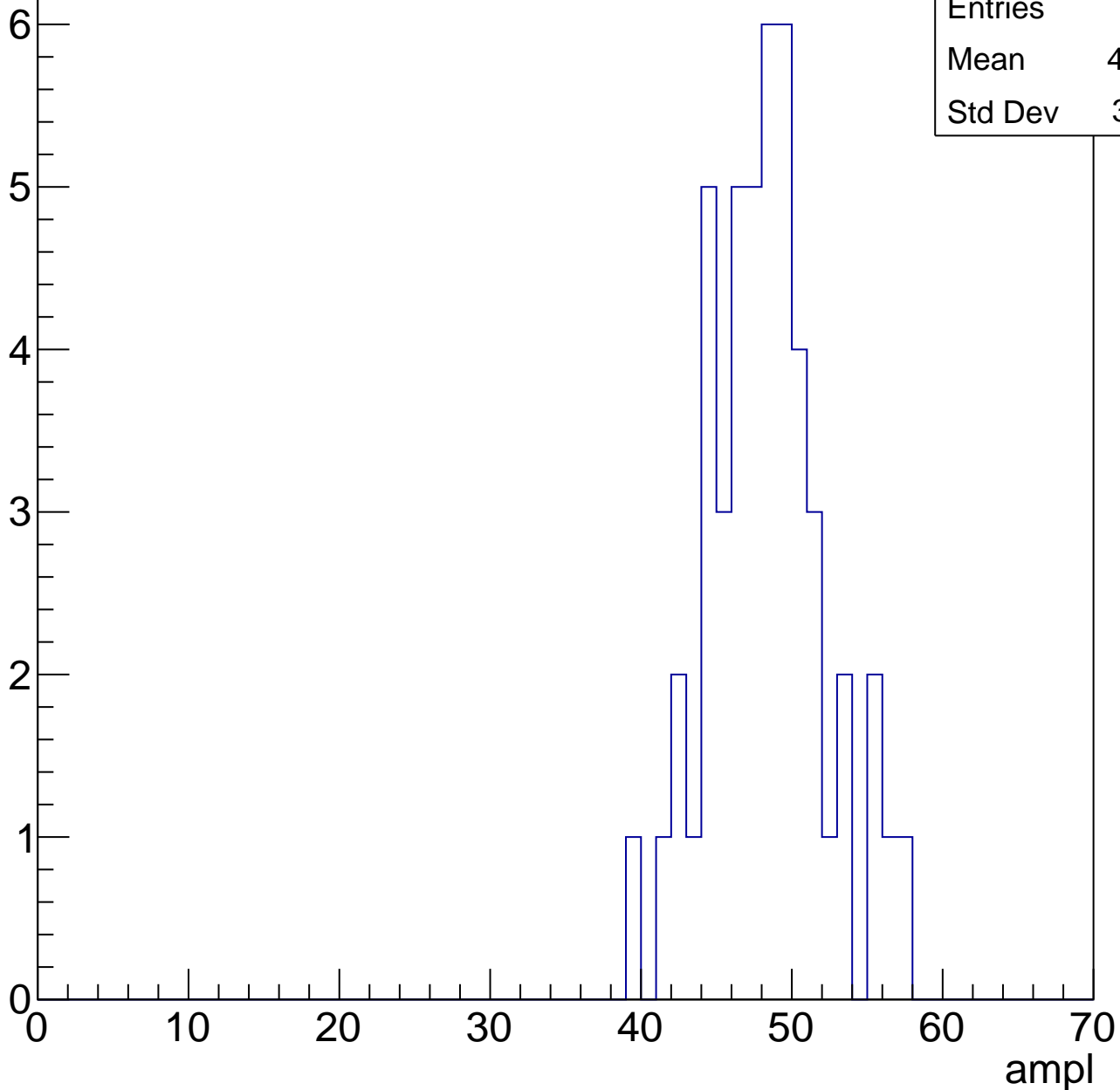


# B1L103S, U3-ch4, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

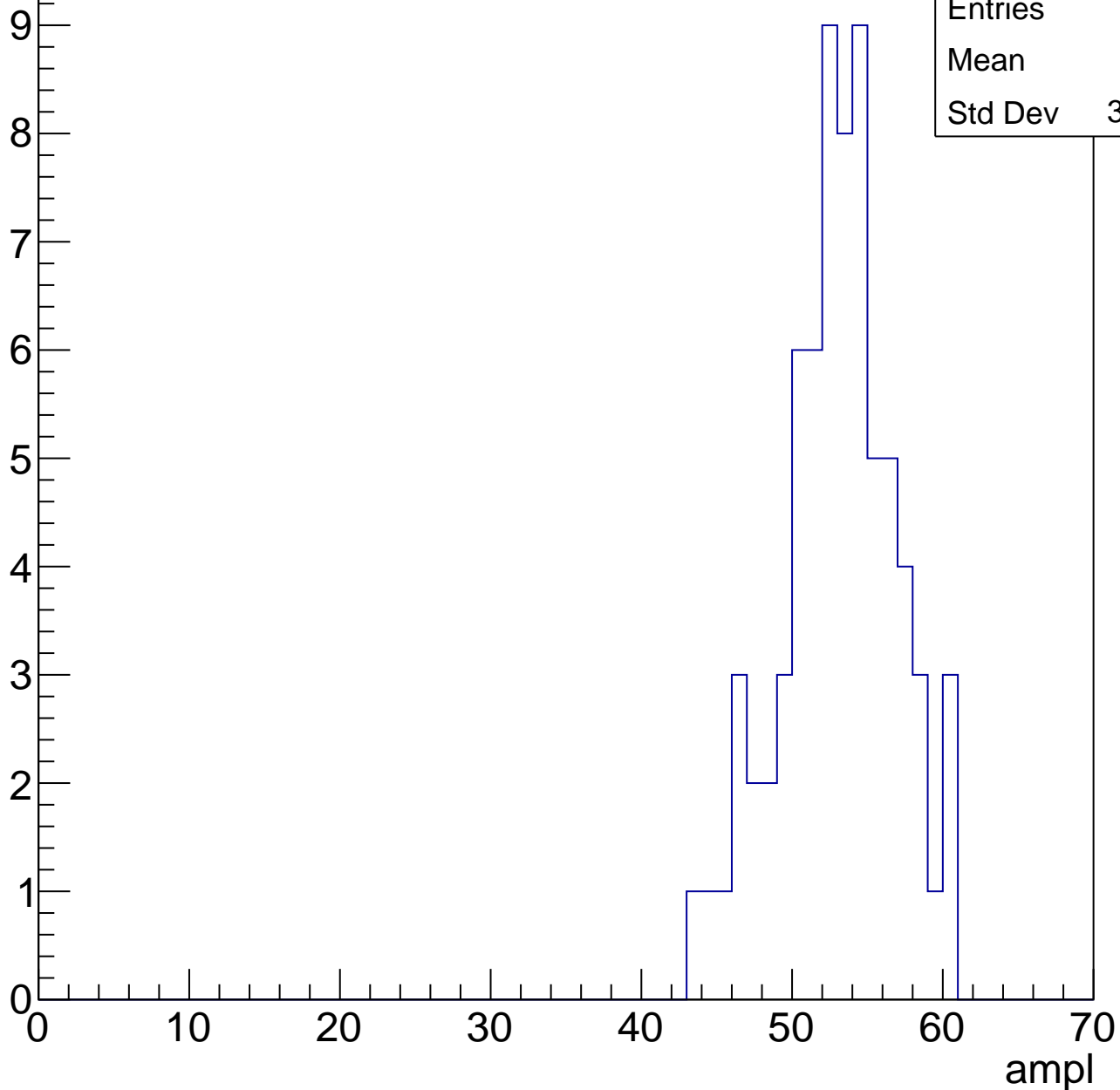
Entries	49
Mean	47.82
Std Dev	3.821



# B1L103S, U3-ch4, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



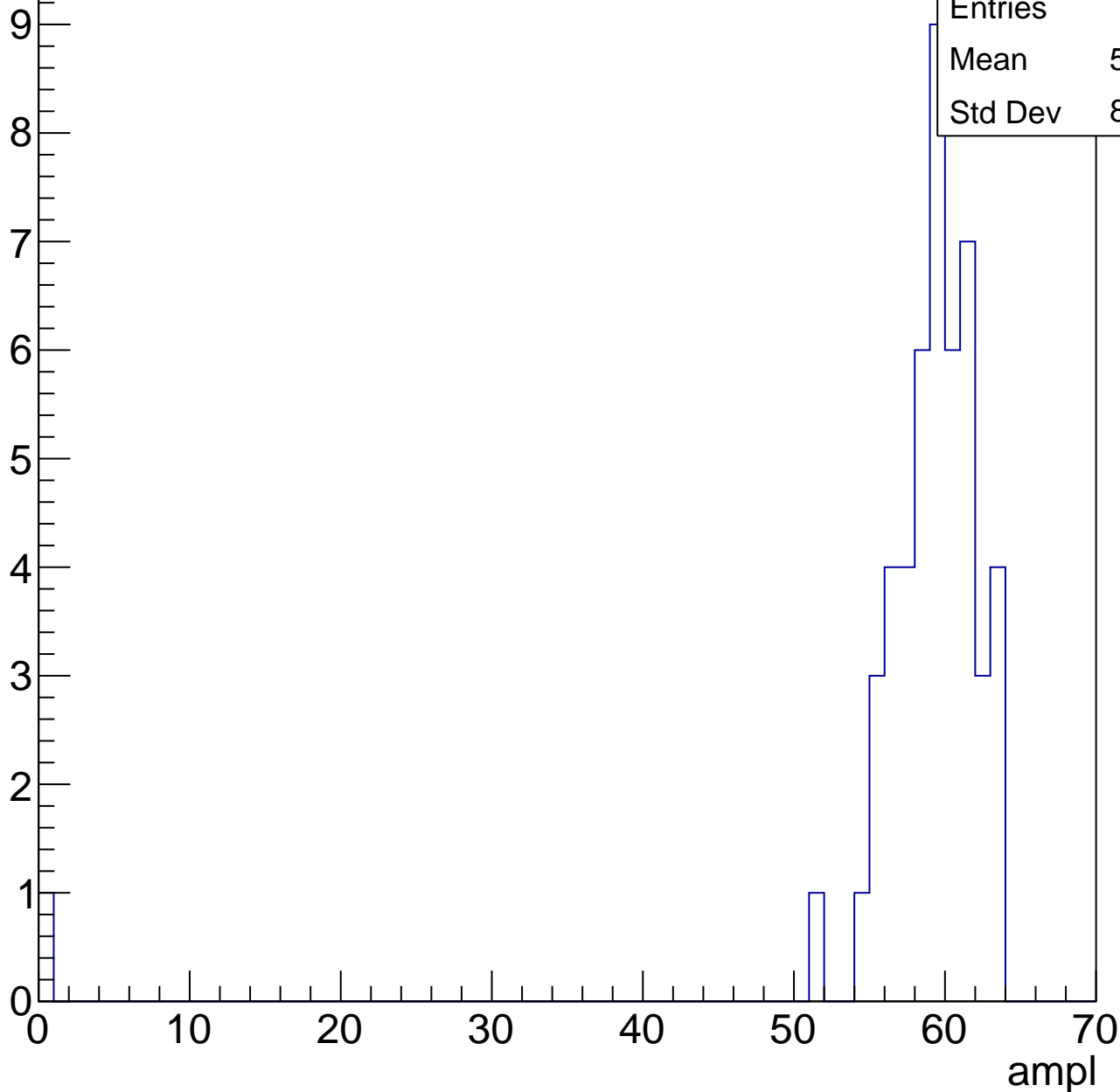
Entries	72
Mean	52.6
Std Dev	3.788

# B1L103S, U3-ch4, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	57.67
Std Dev	8.707

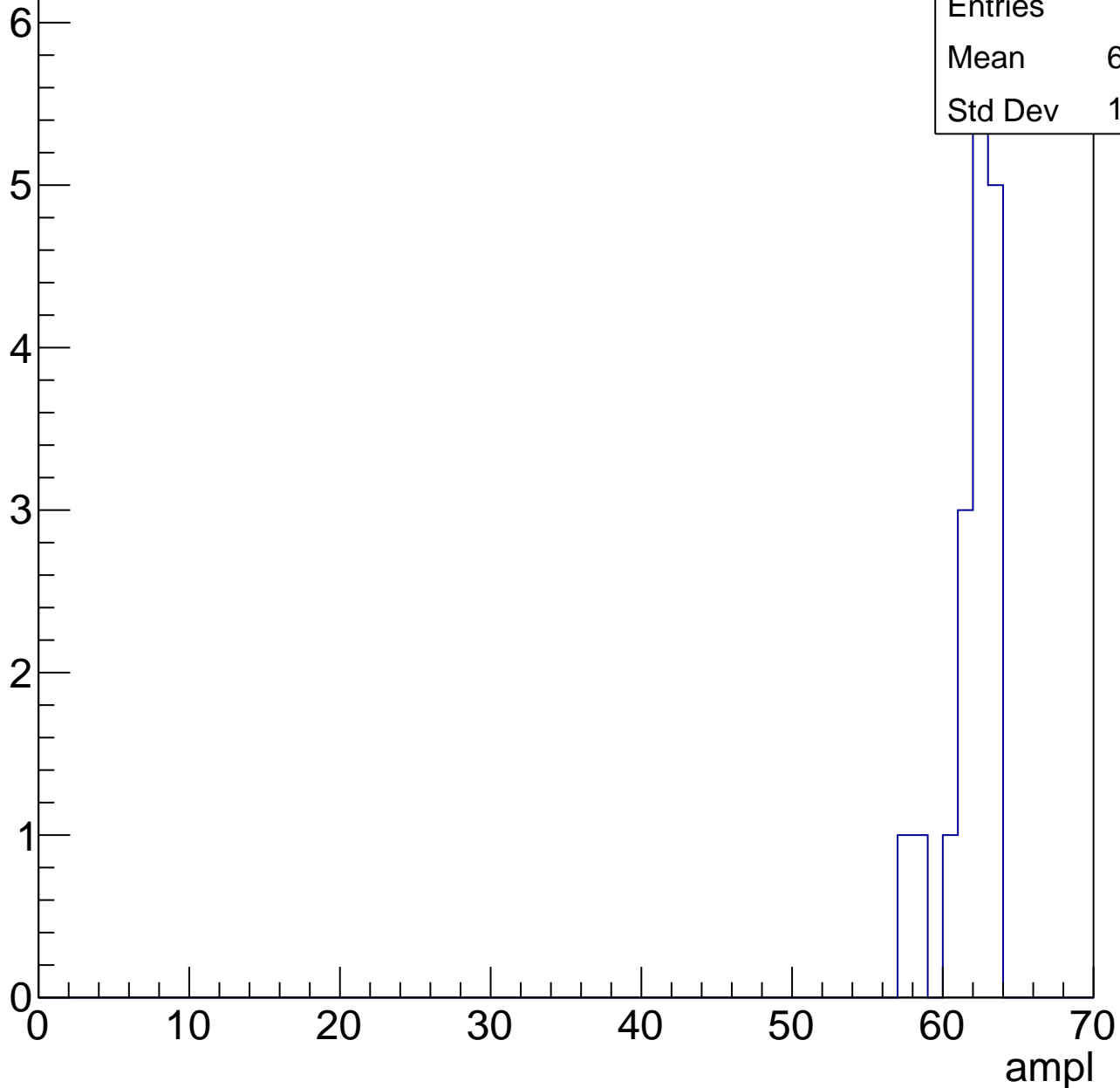


# B1L103S, U3-ch4, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	17
Mean	61.47
Std Dev	1.684

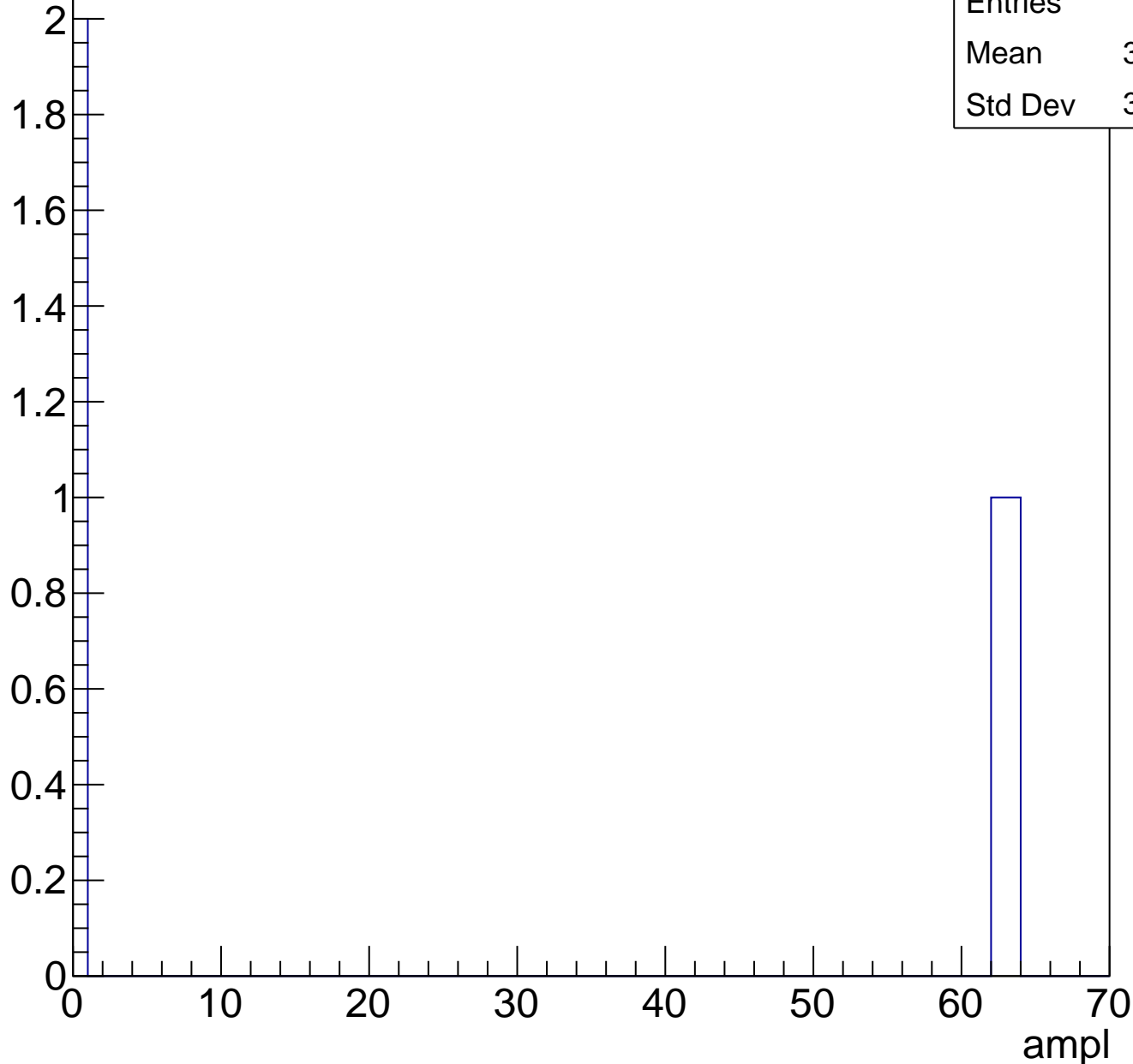




# B1L103S, U3-ch4, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch5, adc0

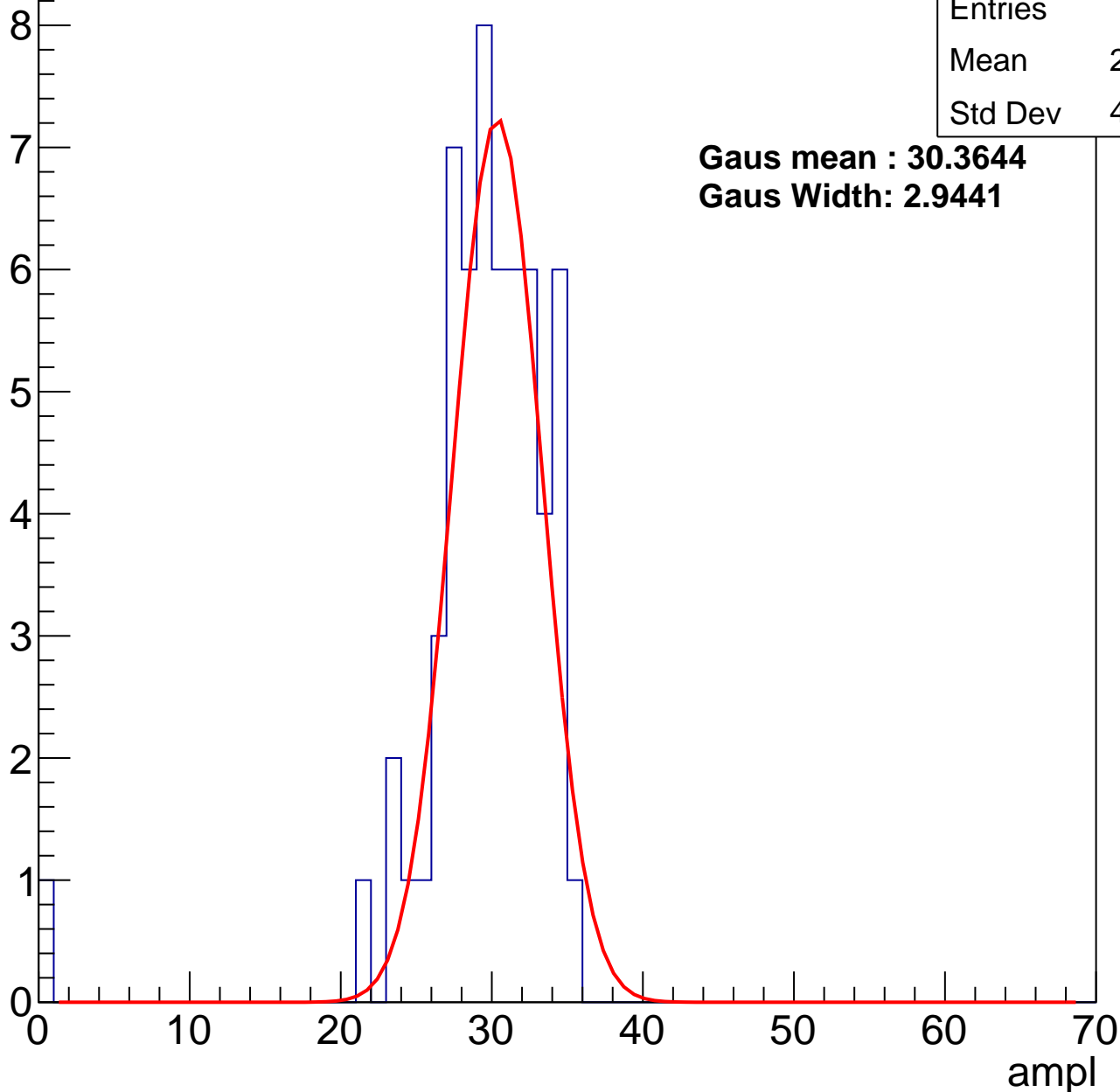
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	29.02
Std Dev	4.894

**Gaus mean : 30.3644**

**Gaus Width: 2.9441**



# B1L103S, U3-ch5, adc1

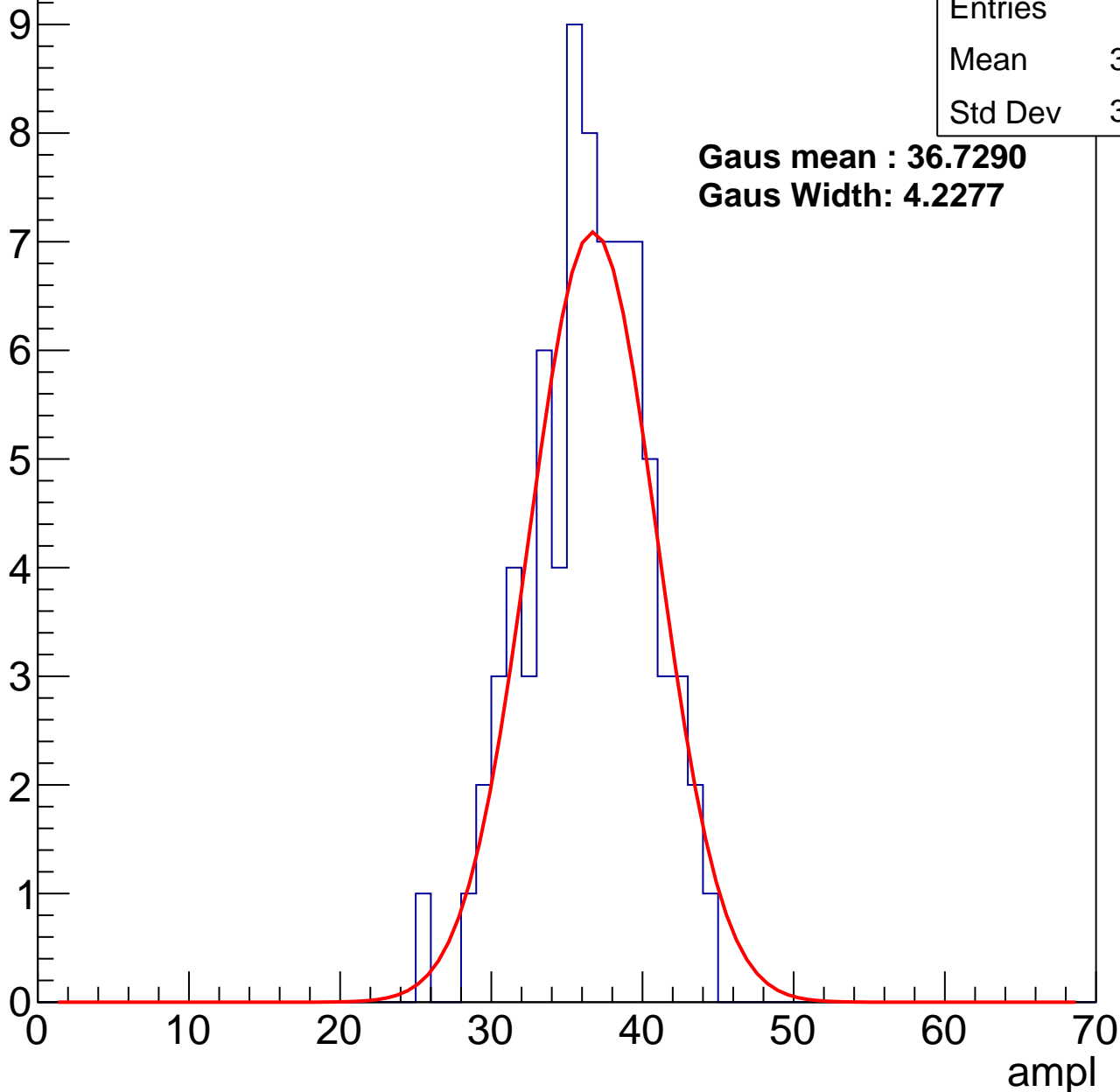
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	35.99
Std Dev	3.875

**Gaus mean : 36.7290**

**Gaus Width: 4.2277**



# B1L103S, U3-ch5, adc2

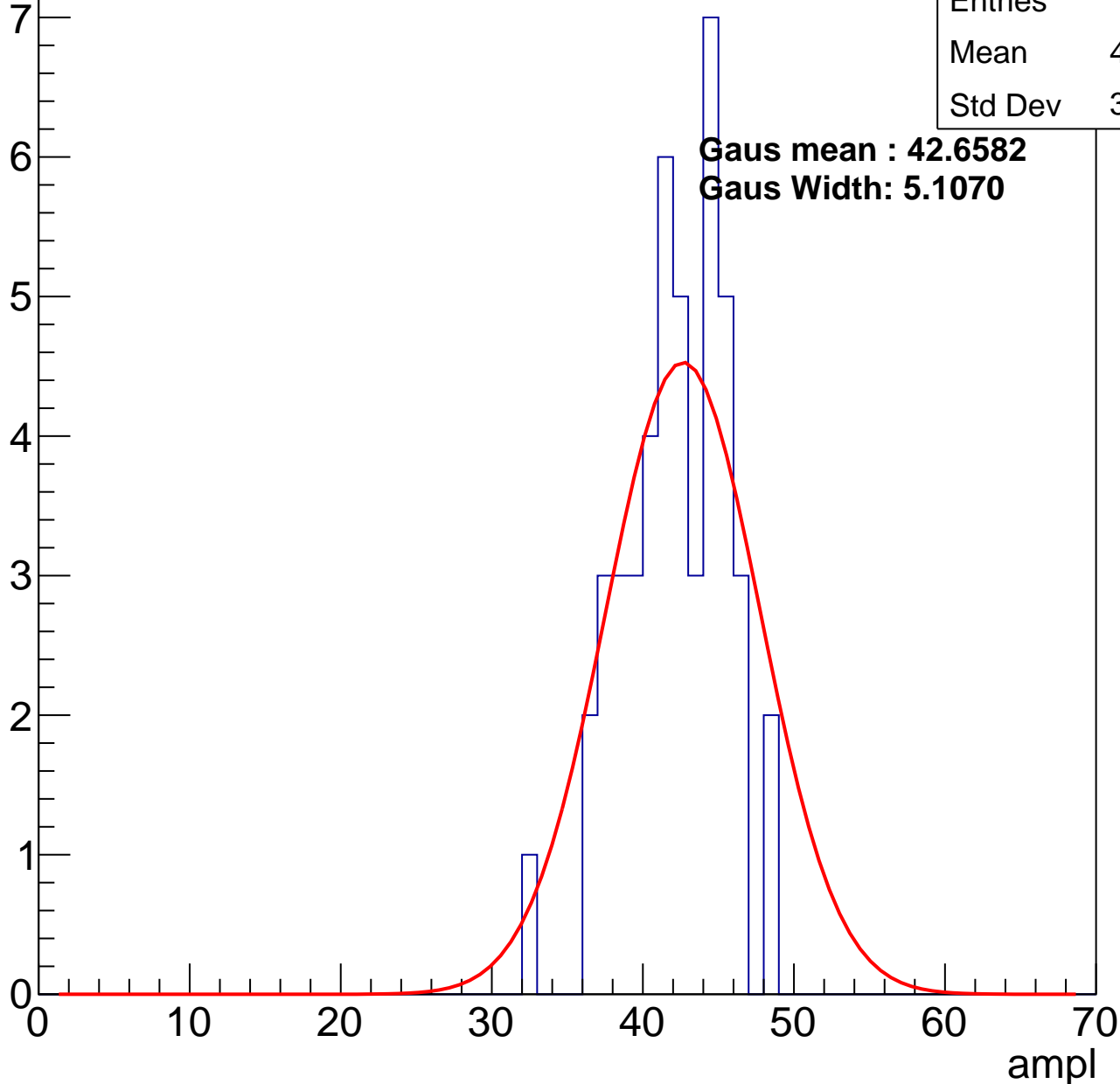
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	47
Mean	41.66
Std Dev	3.372

**Gaus mean : 42.6582**

**Gaus Width: 5.1070**

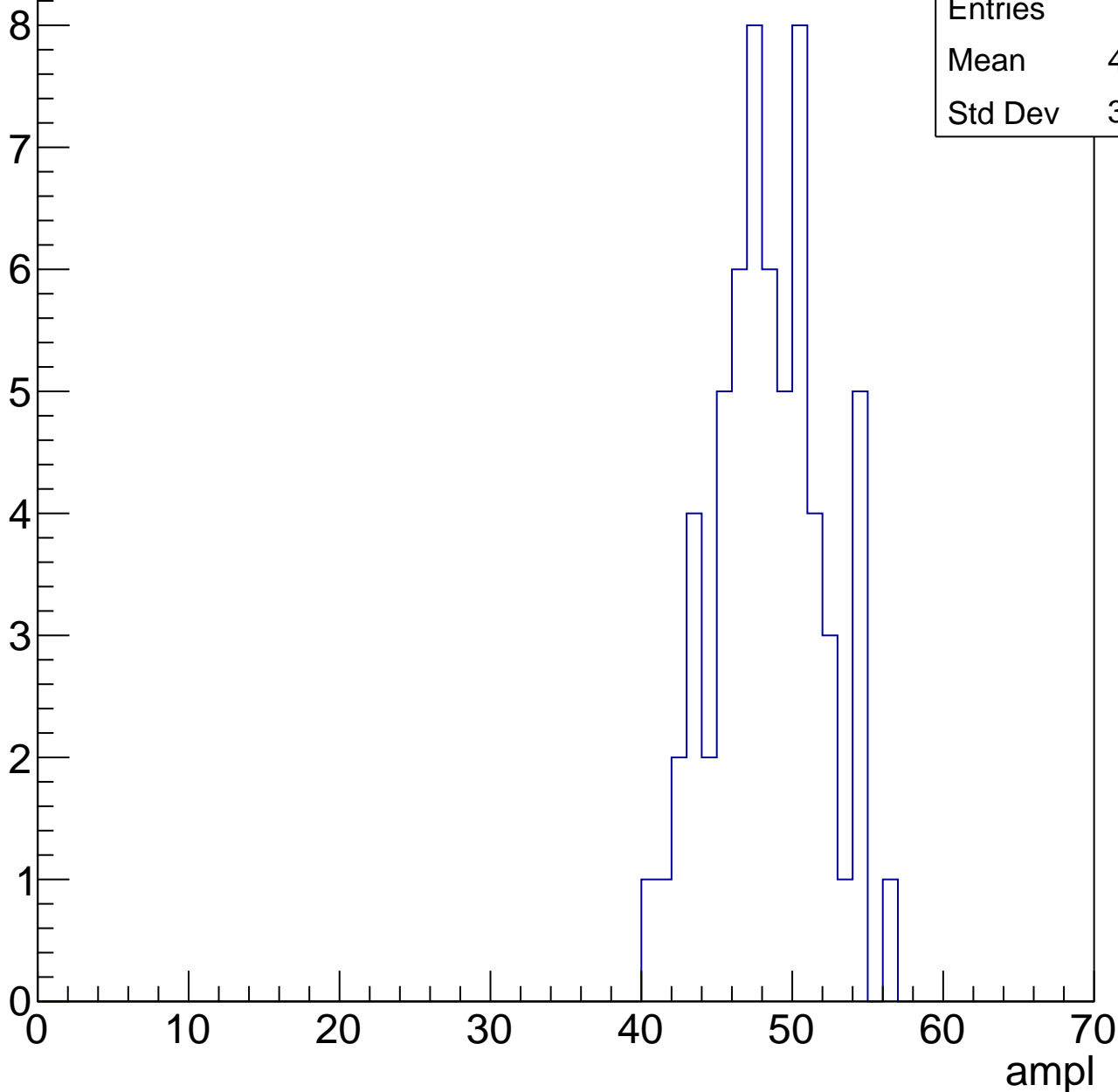


# B1L103S, U3-ch5, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	47.97
Std Dev	3.556

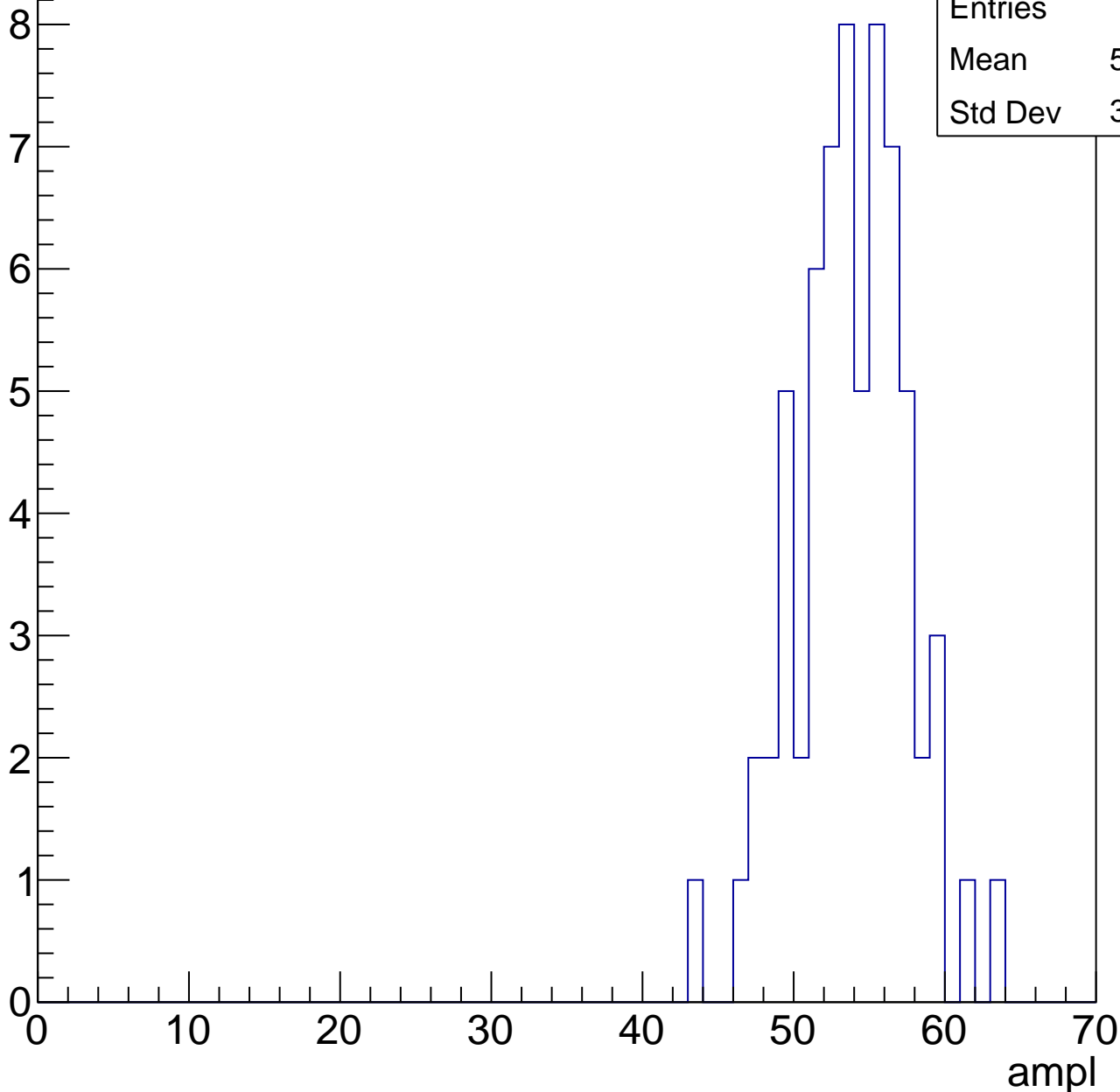


# B1L103S, U3-ch5, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	53.36
Std Dev	3.679

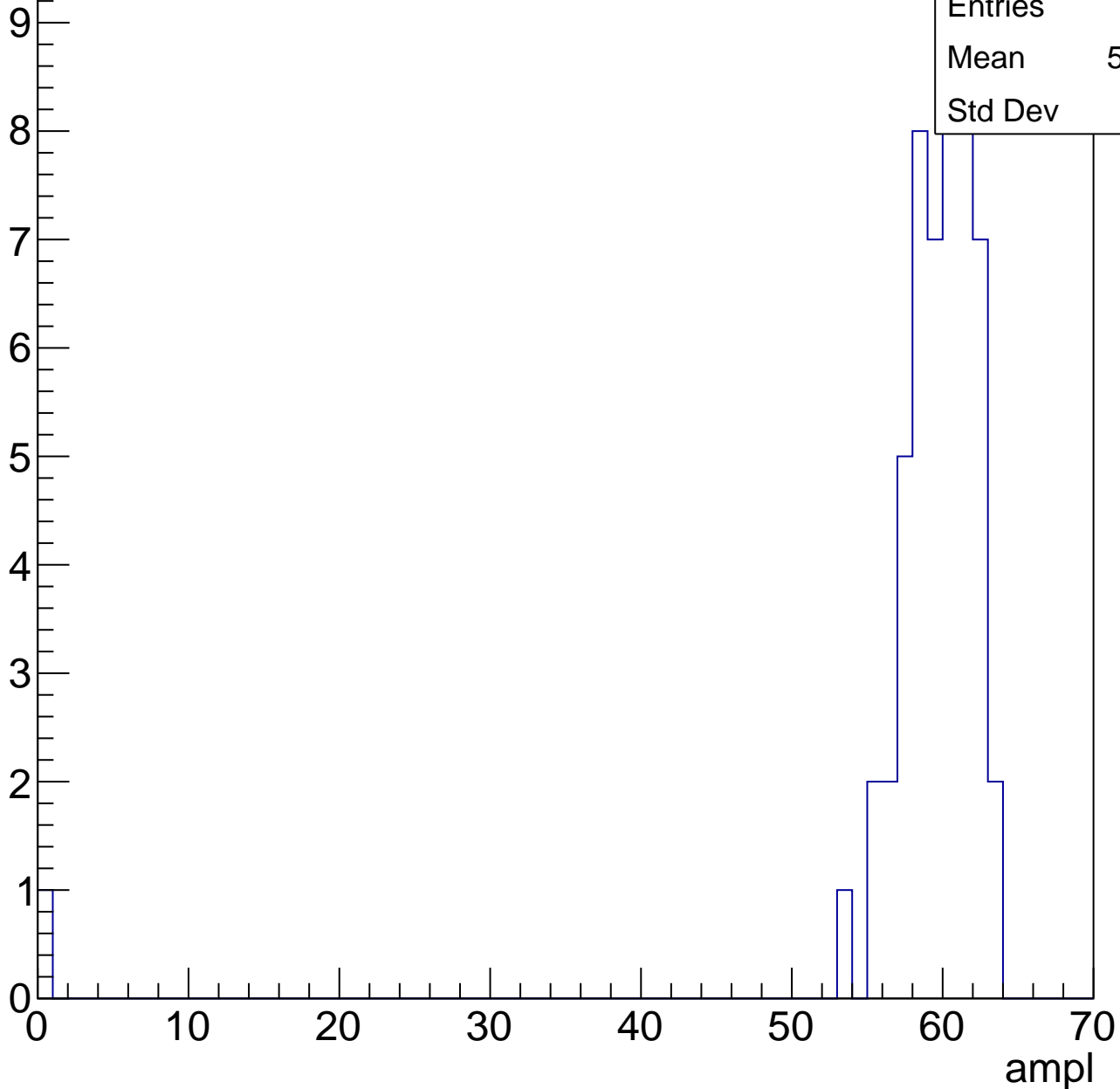


# B1L103S, U3-ch5, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	58.17
Std Dev	8.43

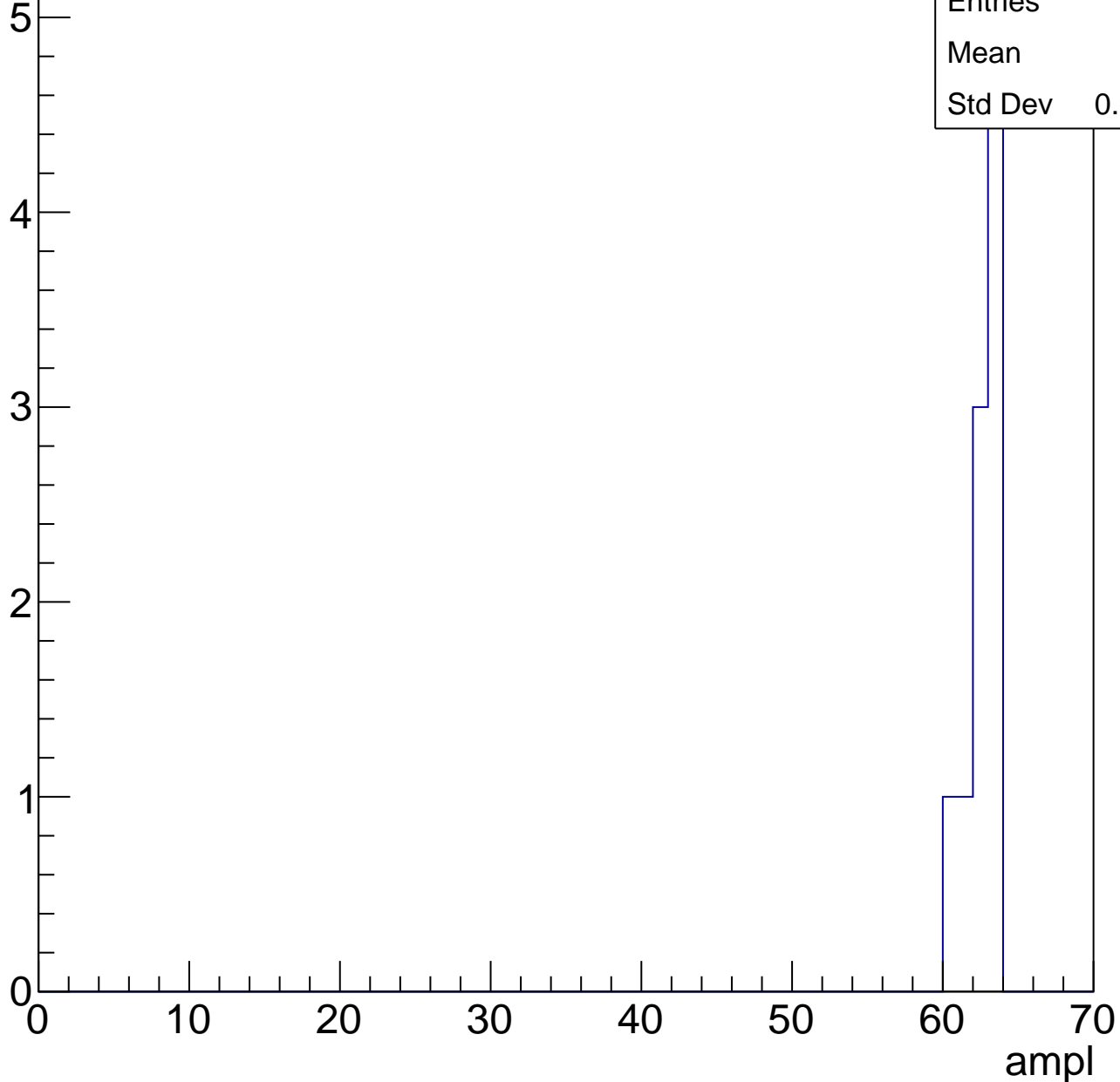


# B1L103S, U3-ch5, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	10
Mean	62.2
Std Dev	0.9798





# B1L103S, U3-ch5, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch6, adc0

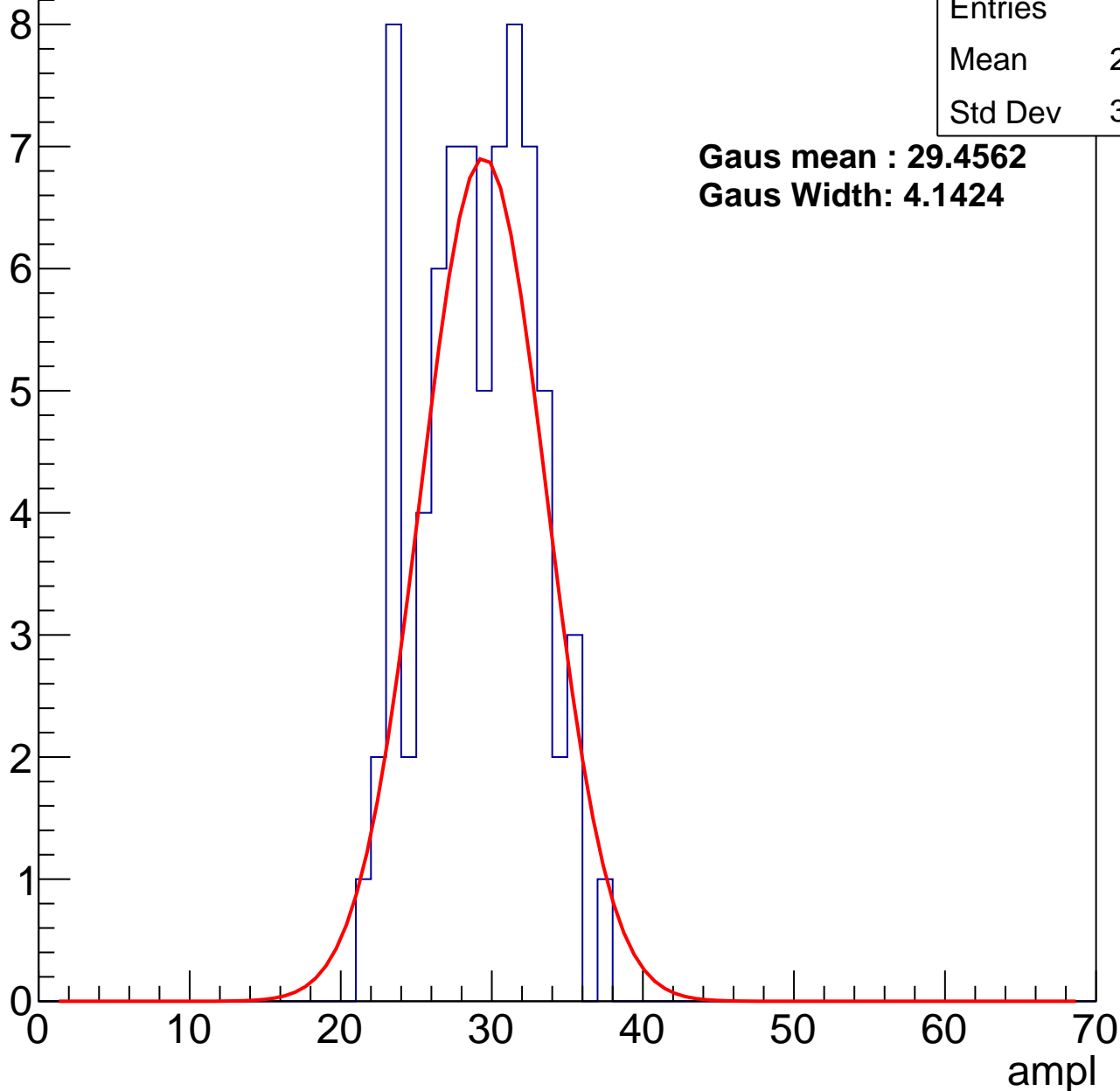
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	28.53
Std Dev	3.725

**Gaus mean : 29.4562**

**Gaus Width: 4.1424**



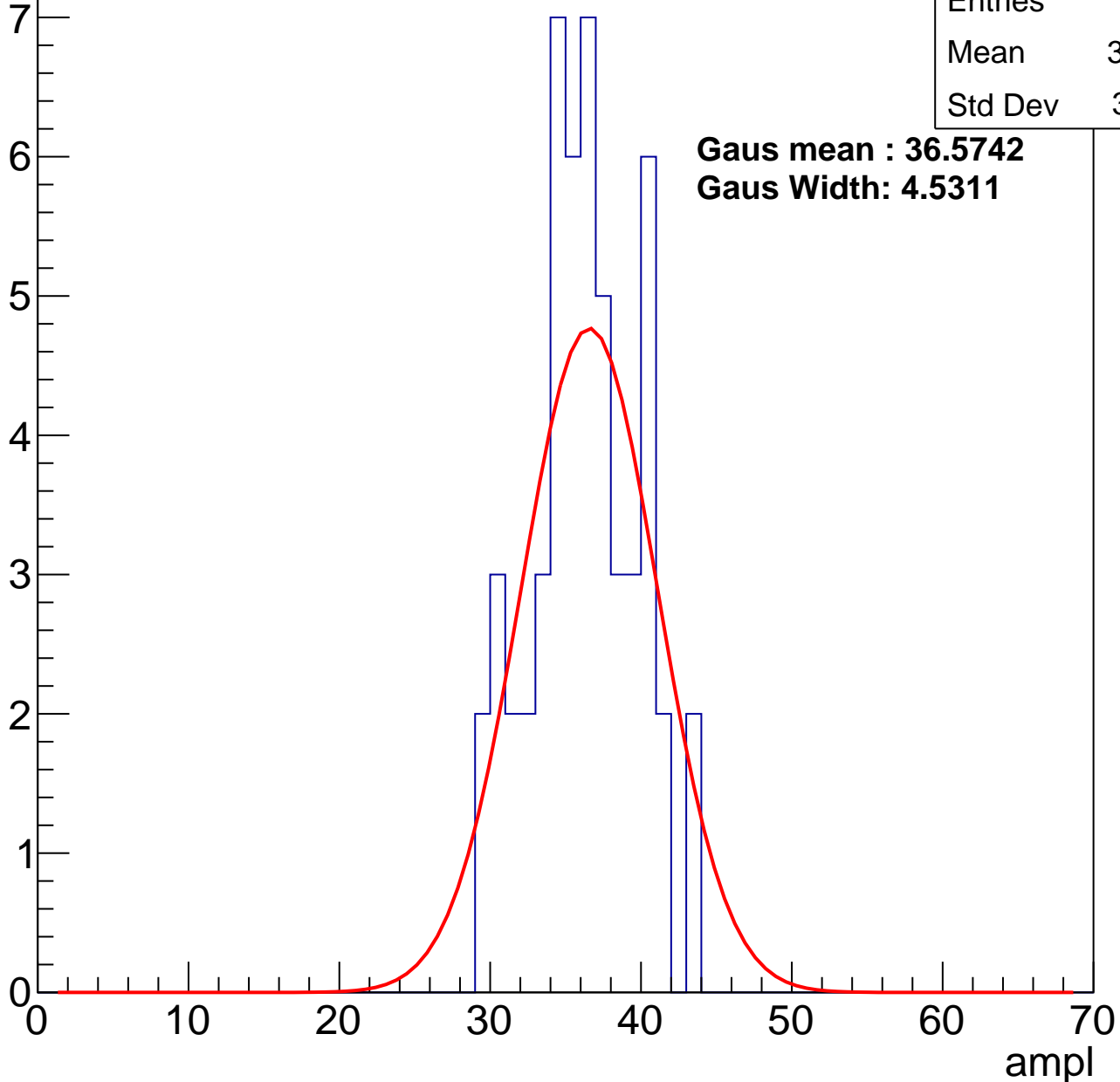
# B1L103S, U3-ch6, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	35.79
Std Dev	3.461

**Gaus mean : 36.5742**  
**Gaus Width: 4.5311**



# B1L103S, U3-ch6, adc2

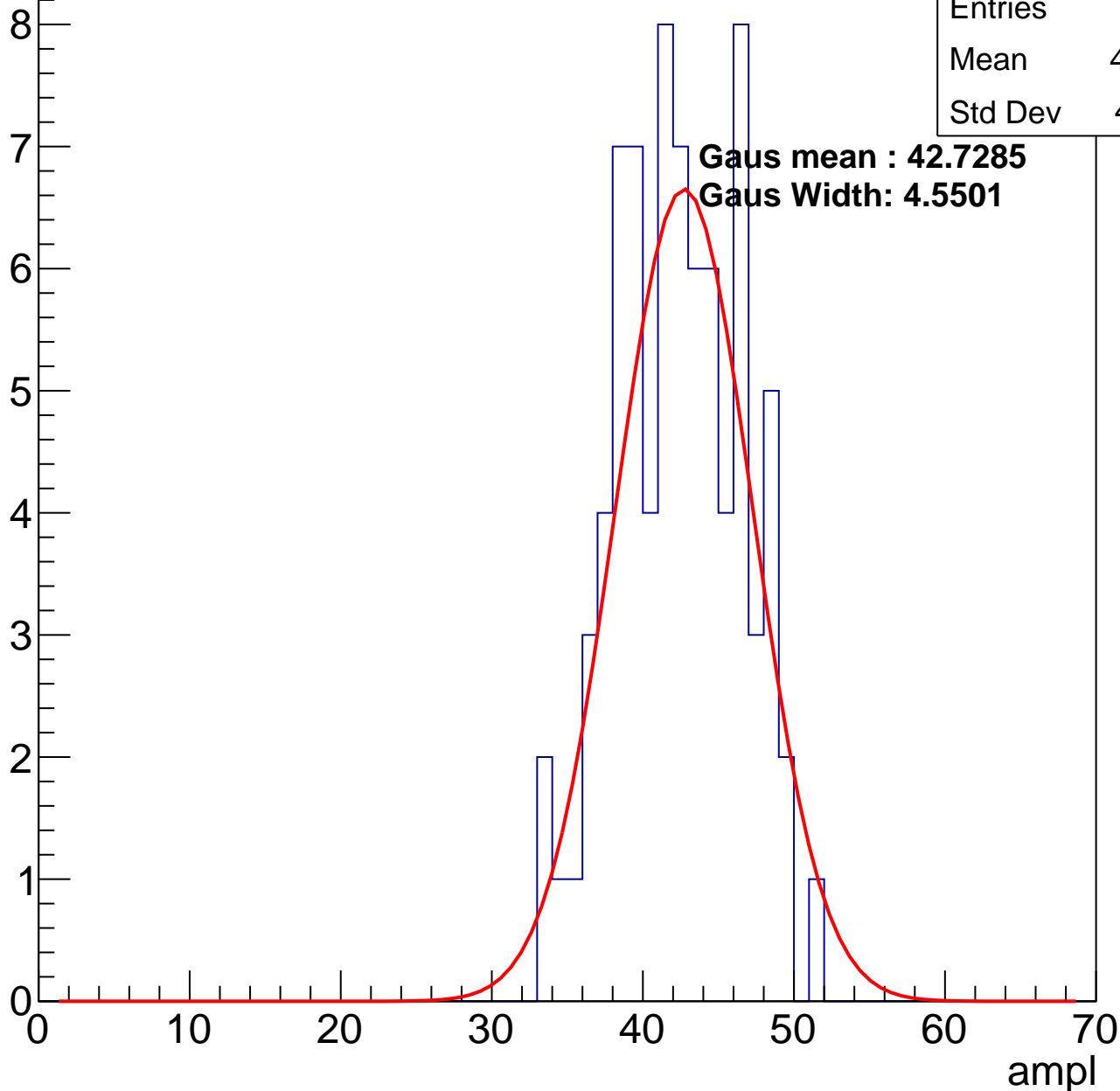
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	79
Mean	41.92
Std Dev	4.071

**Gaus mean : 42.7285**

**Gaus Width: 4.5501**

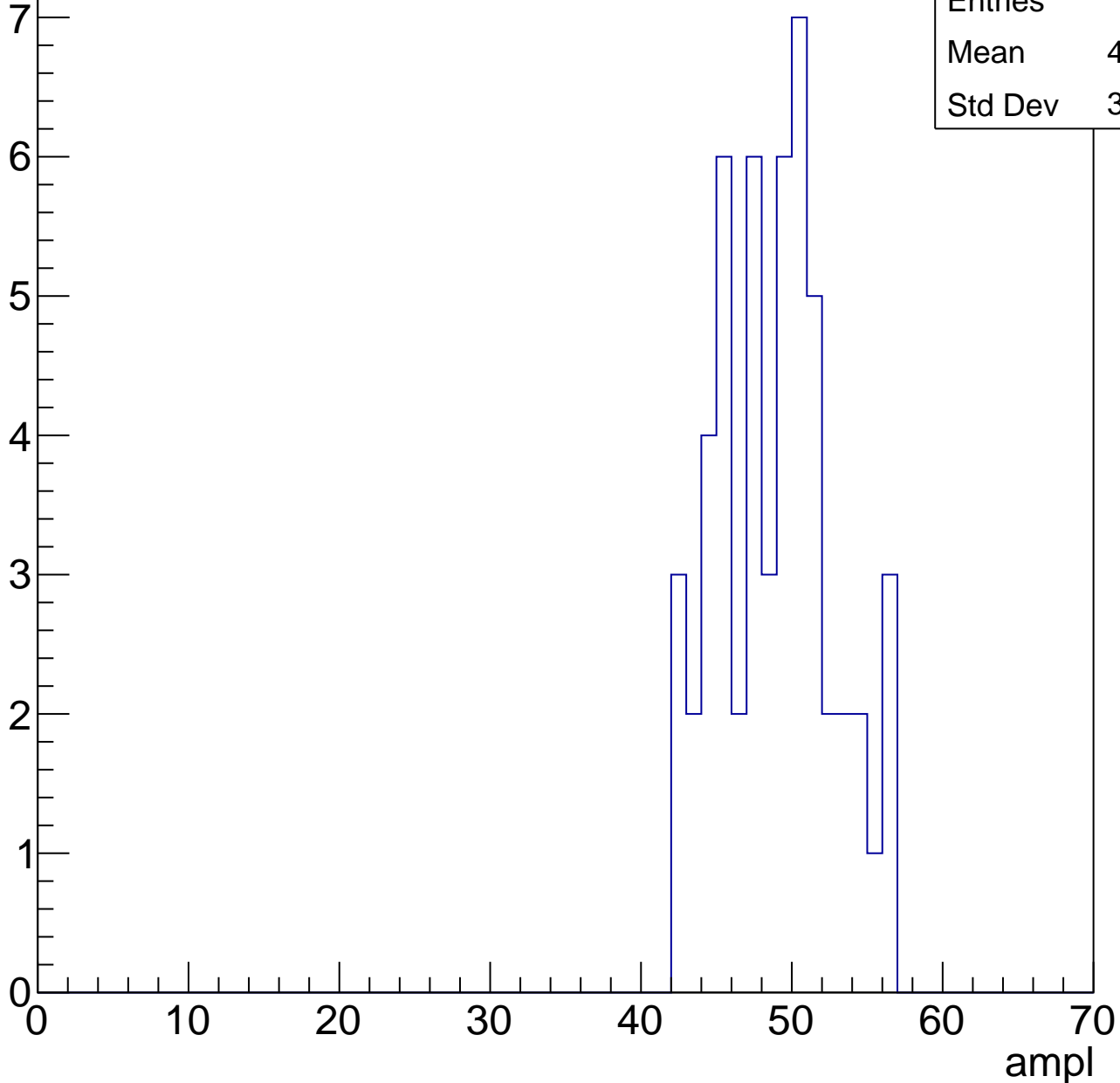


# B1L103S, U3-ch6, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	48.44
Std Dev	3.735

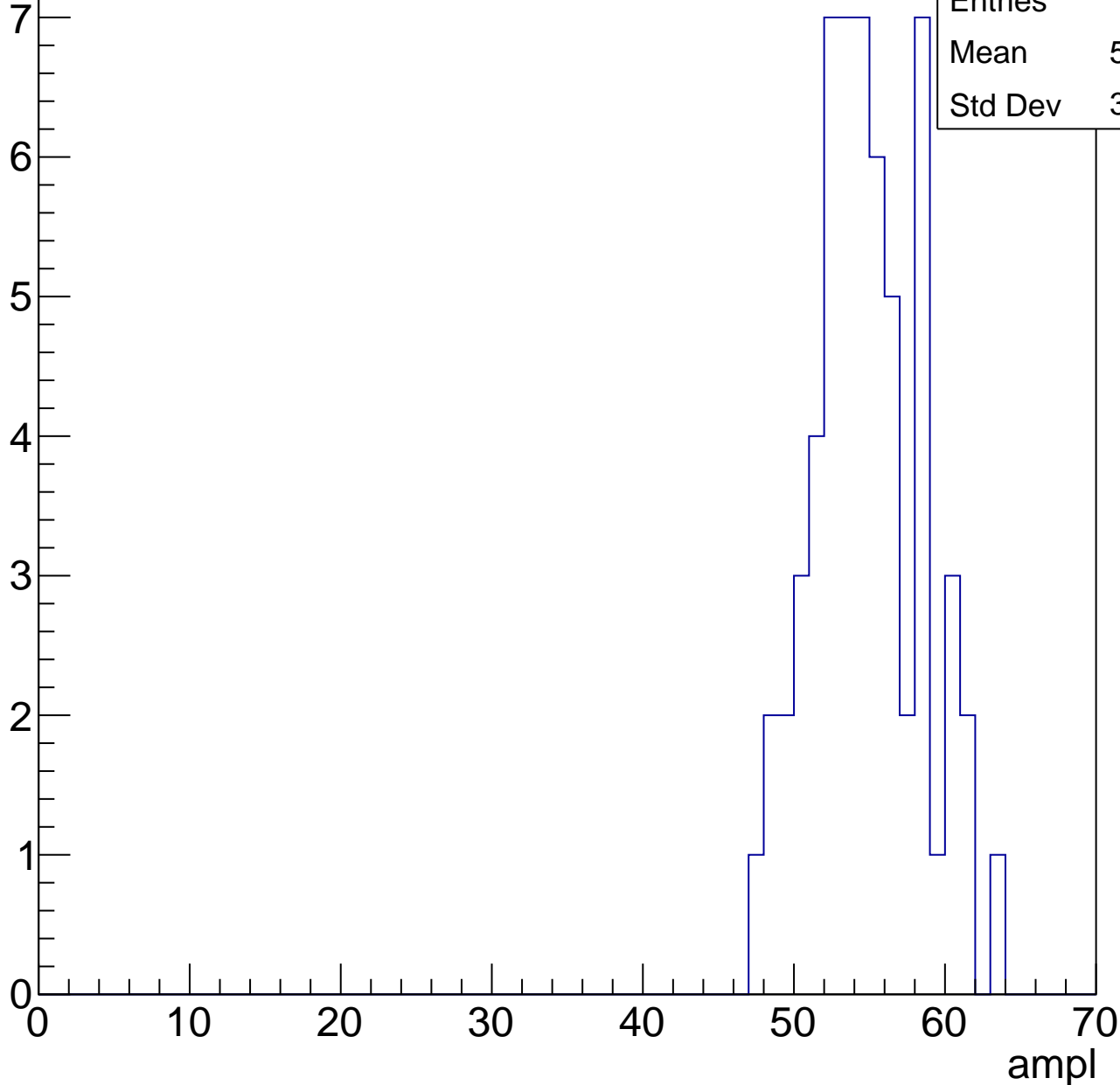


# B1L103S, U3-ch6, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

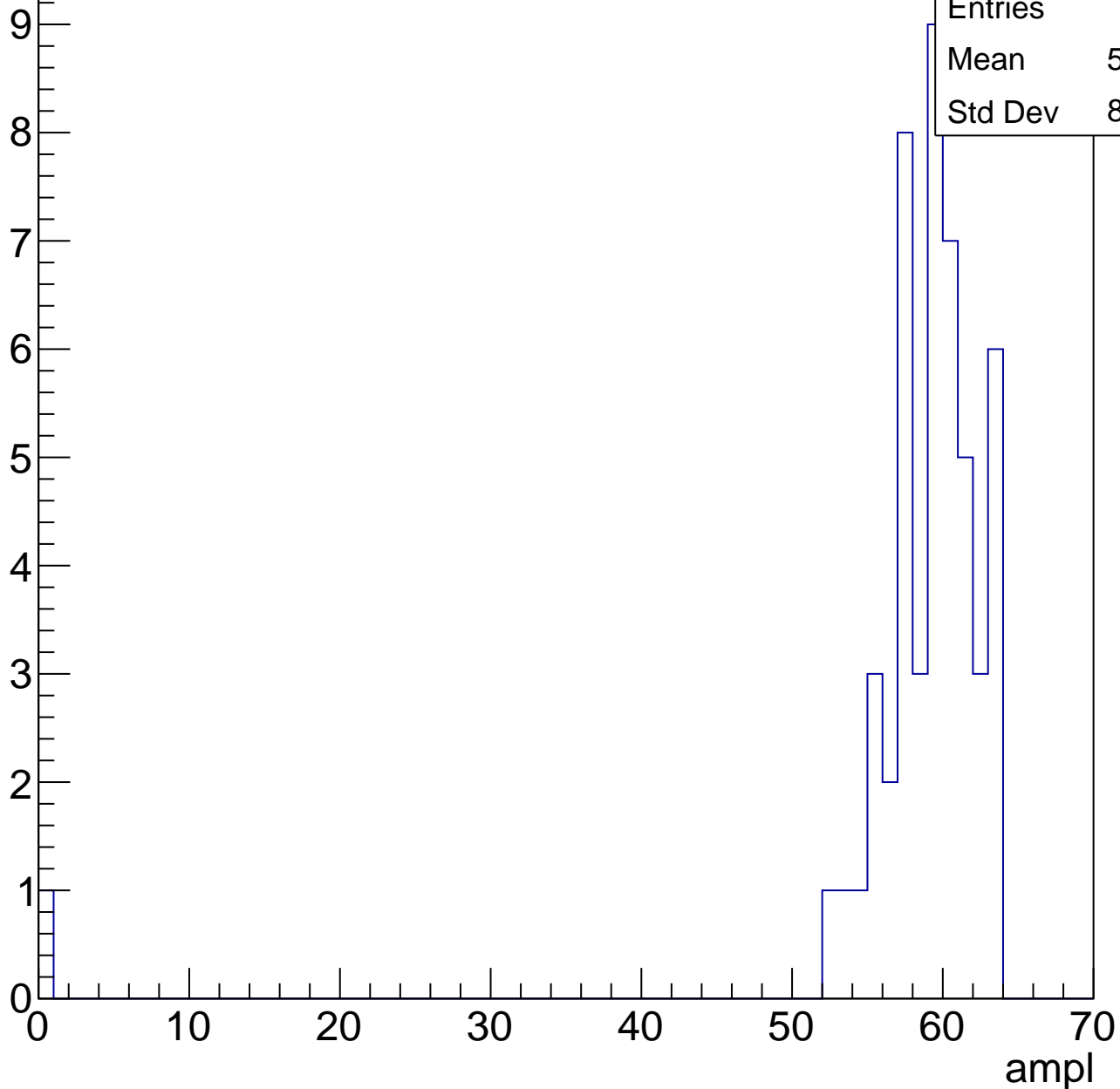
Entries	60
Mean	54.37
Std Dev	3.535



# B1L103S, U3-ch6, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

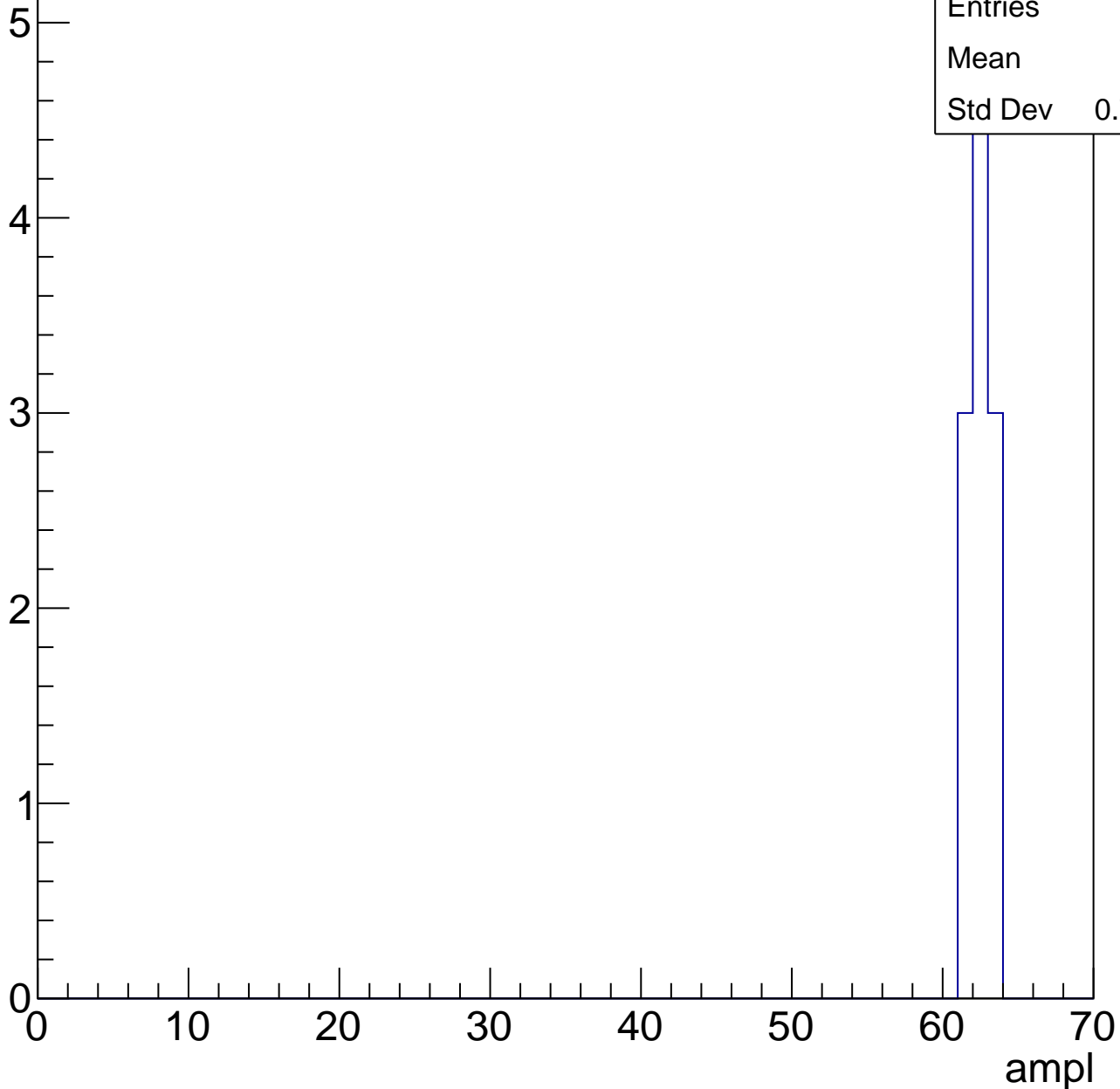


# B1L103S, U3-ch6, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	11
Mean	62
Std Dev	0.7385





# B1L103S, U3-ch6, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	62
Std Dev	0

0 10 20 30 40 50 60 70

ampl

# B1L103S, U3-ch7, adc0

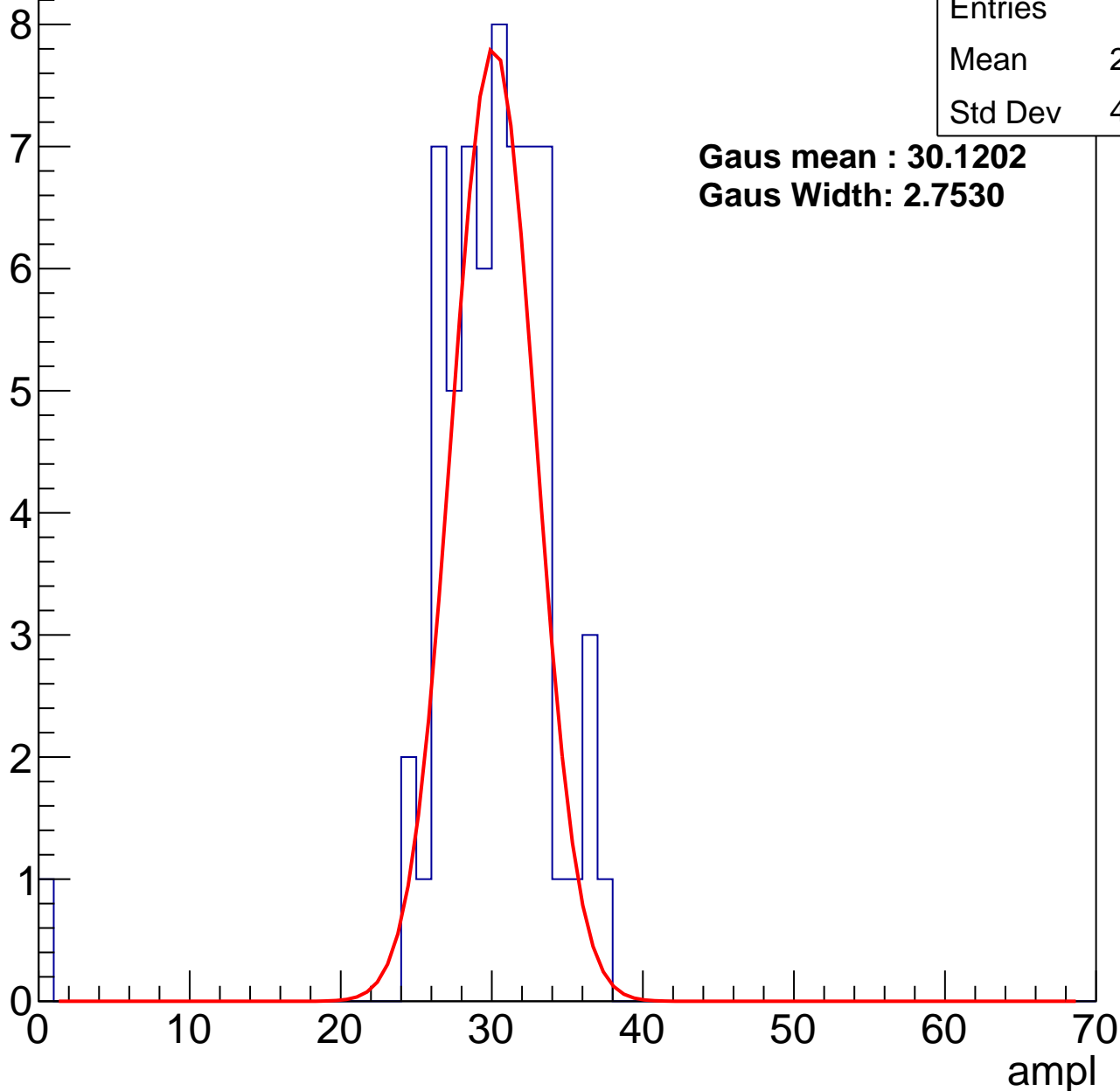
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	29.47
Std Dev	4.786

**Gaus mean : 30.1202**

**Gaus Width: 2.7530**



# B1L103S, U3-ch7, adc1

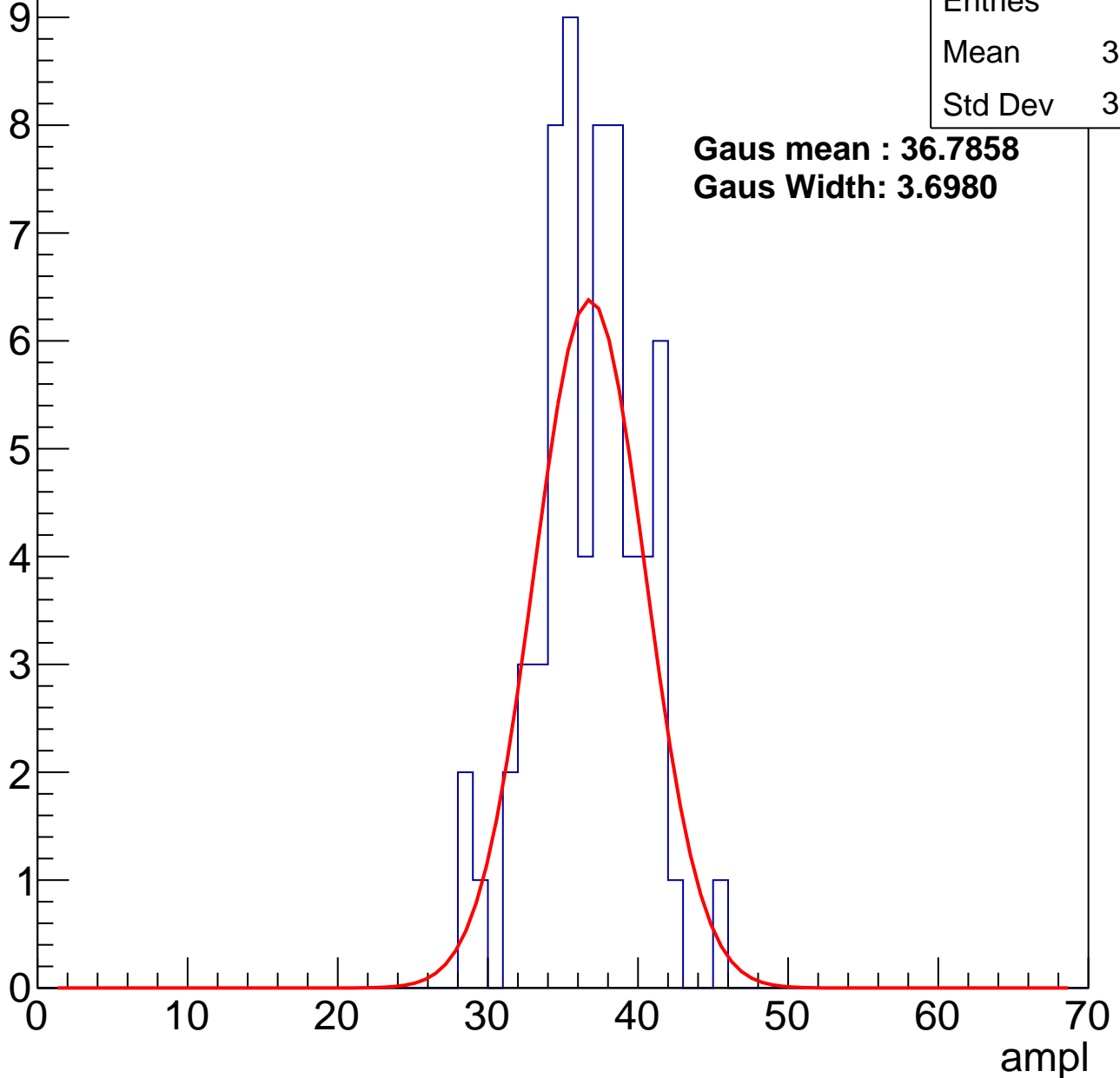
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	36.28
Std Dev	3.412

**Gaus mean : 36.7858**

**Gaus Width: 3.6980**



# B1L103S, U3-ch7, adc2

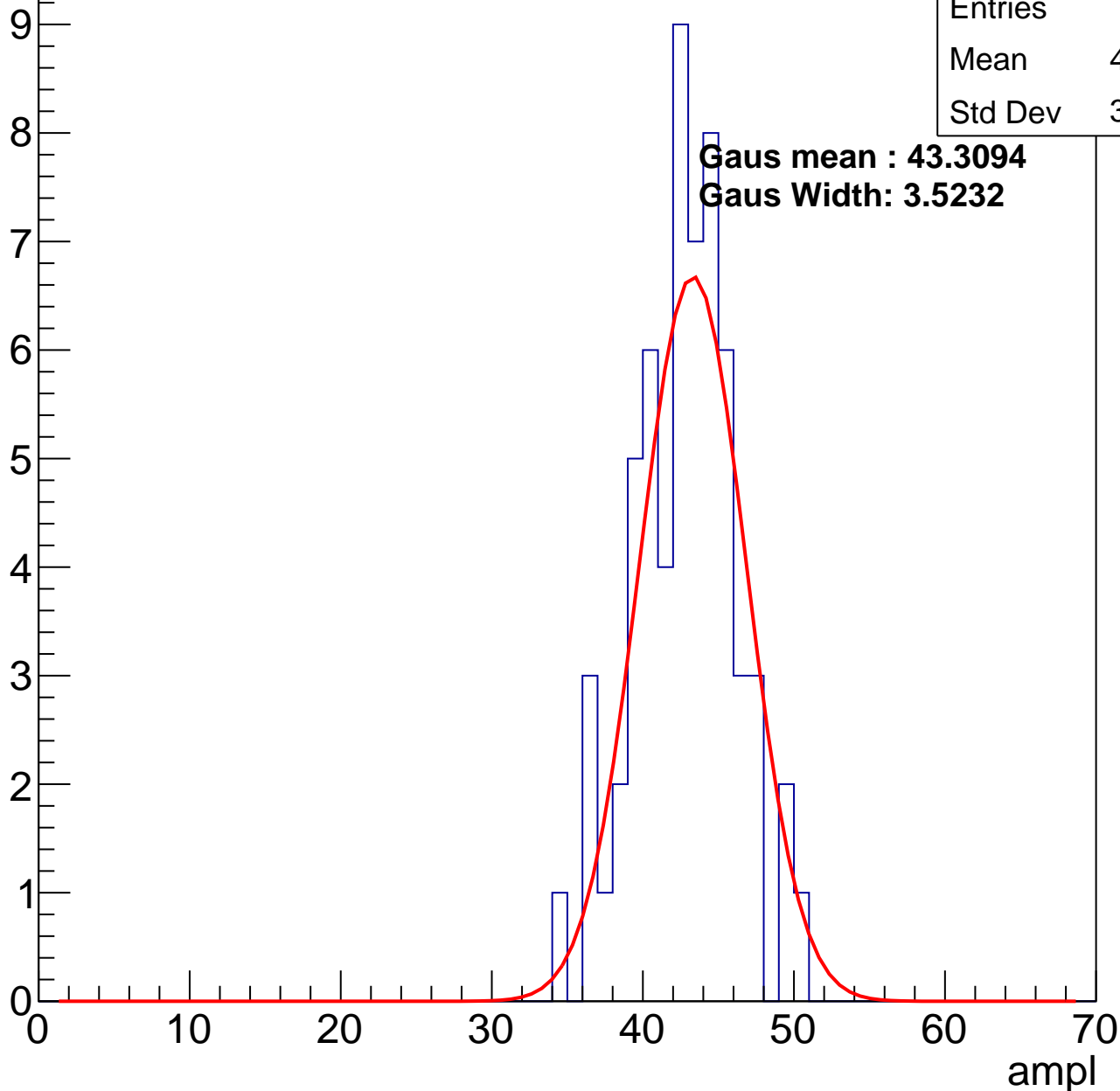
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	42.33
Std Dev	3.323

**Gaus mean : 43.3094**

**Gaus Width: 3.5232**

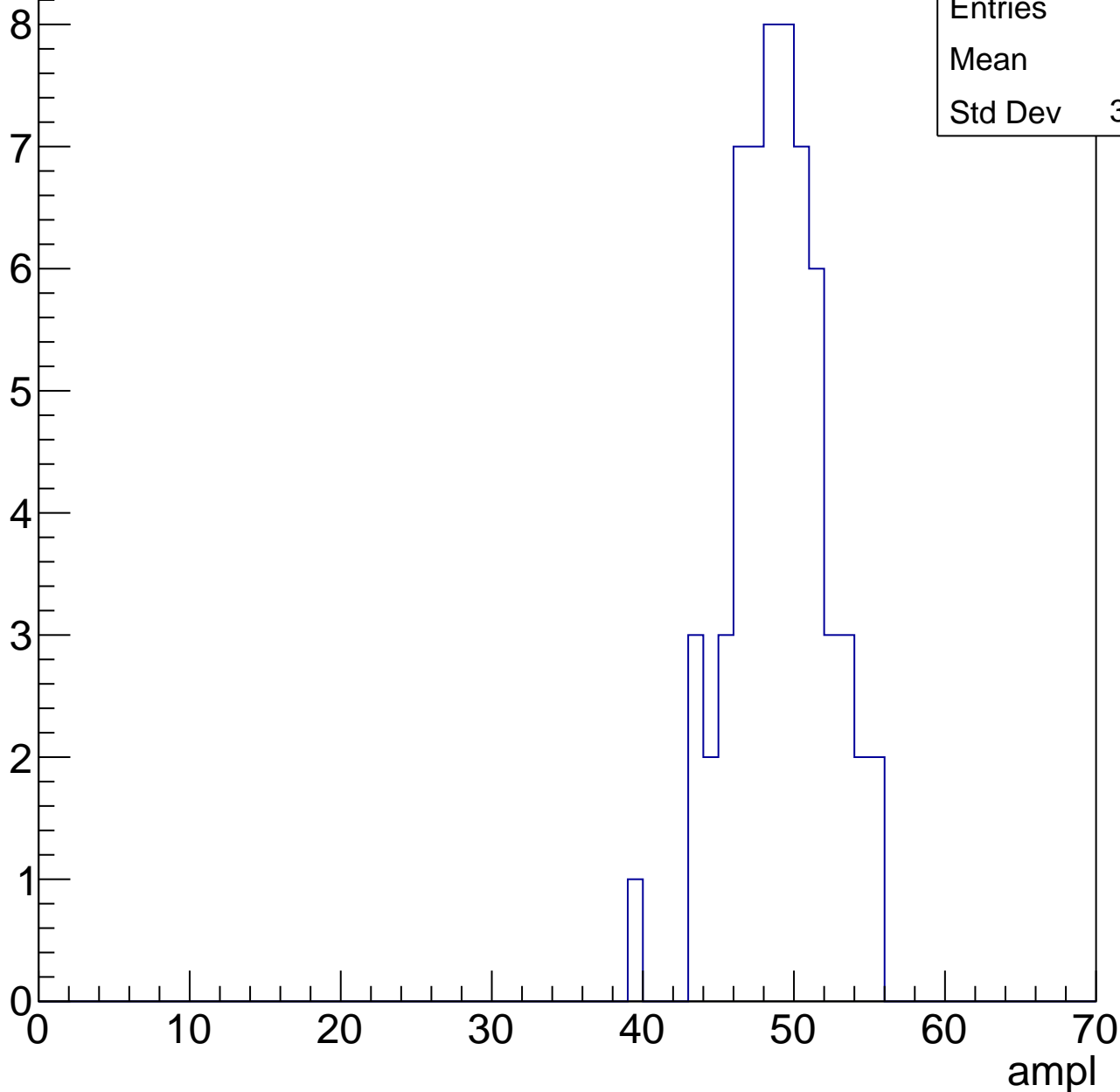


# B1L103S, U3-ch7, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	48.5
Std Dev	3.156

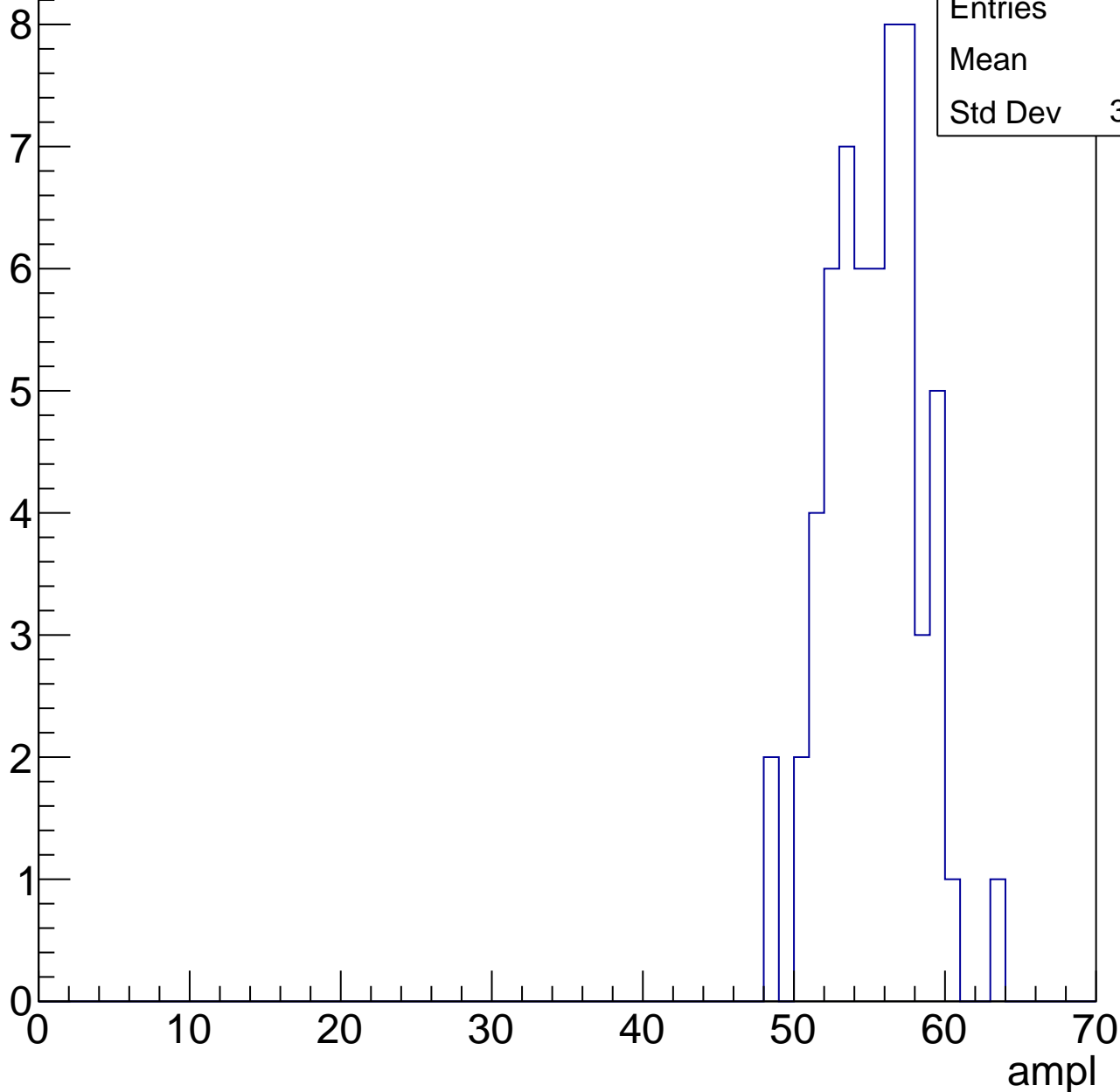


# B1L103S, U3-ch7, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	54.8
Std Dev	3.007



# B1L103S, U3-ch7, adc5

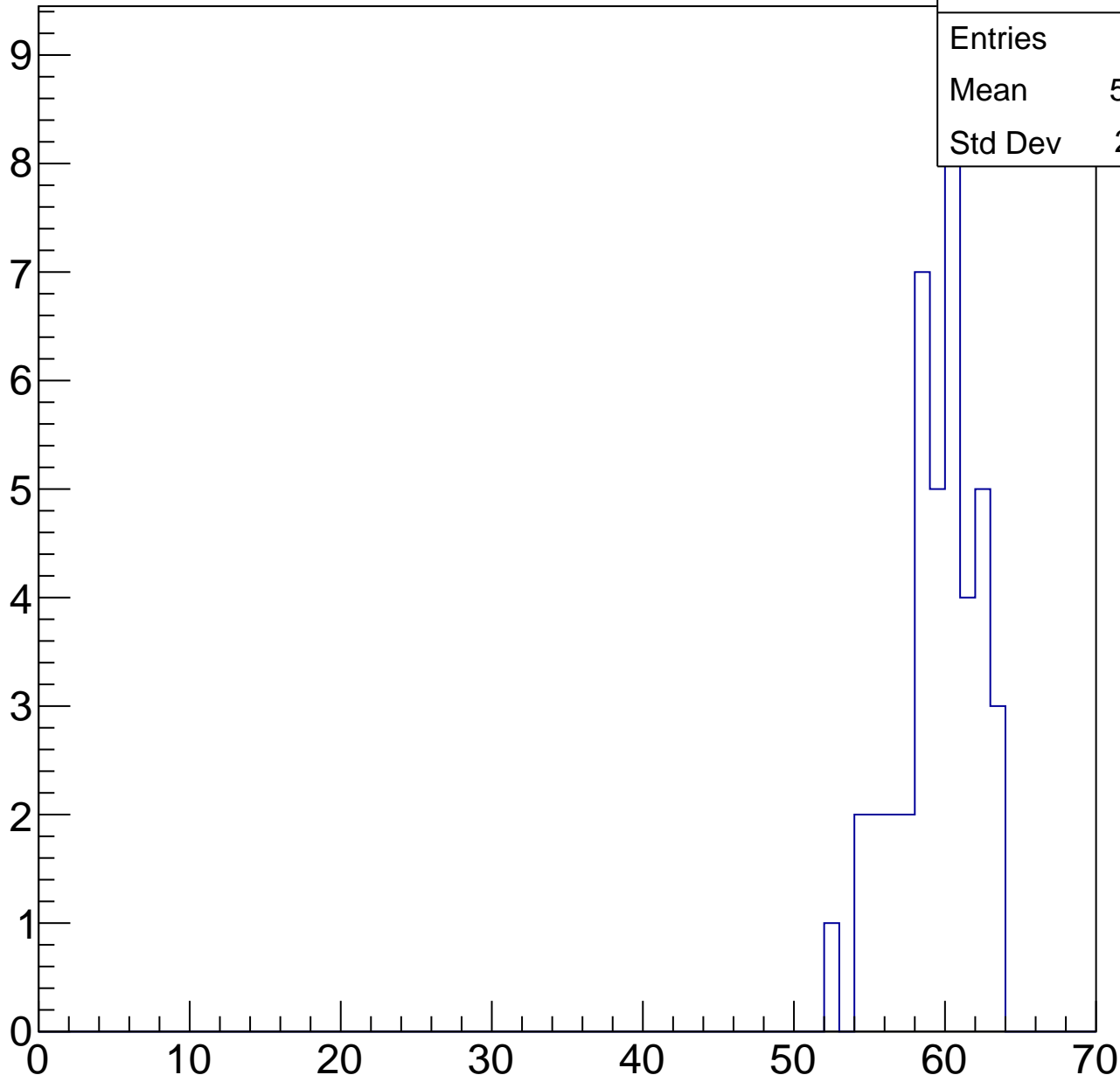
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	42
Mean	59.05
Std Dev	2.591

ampl

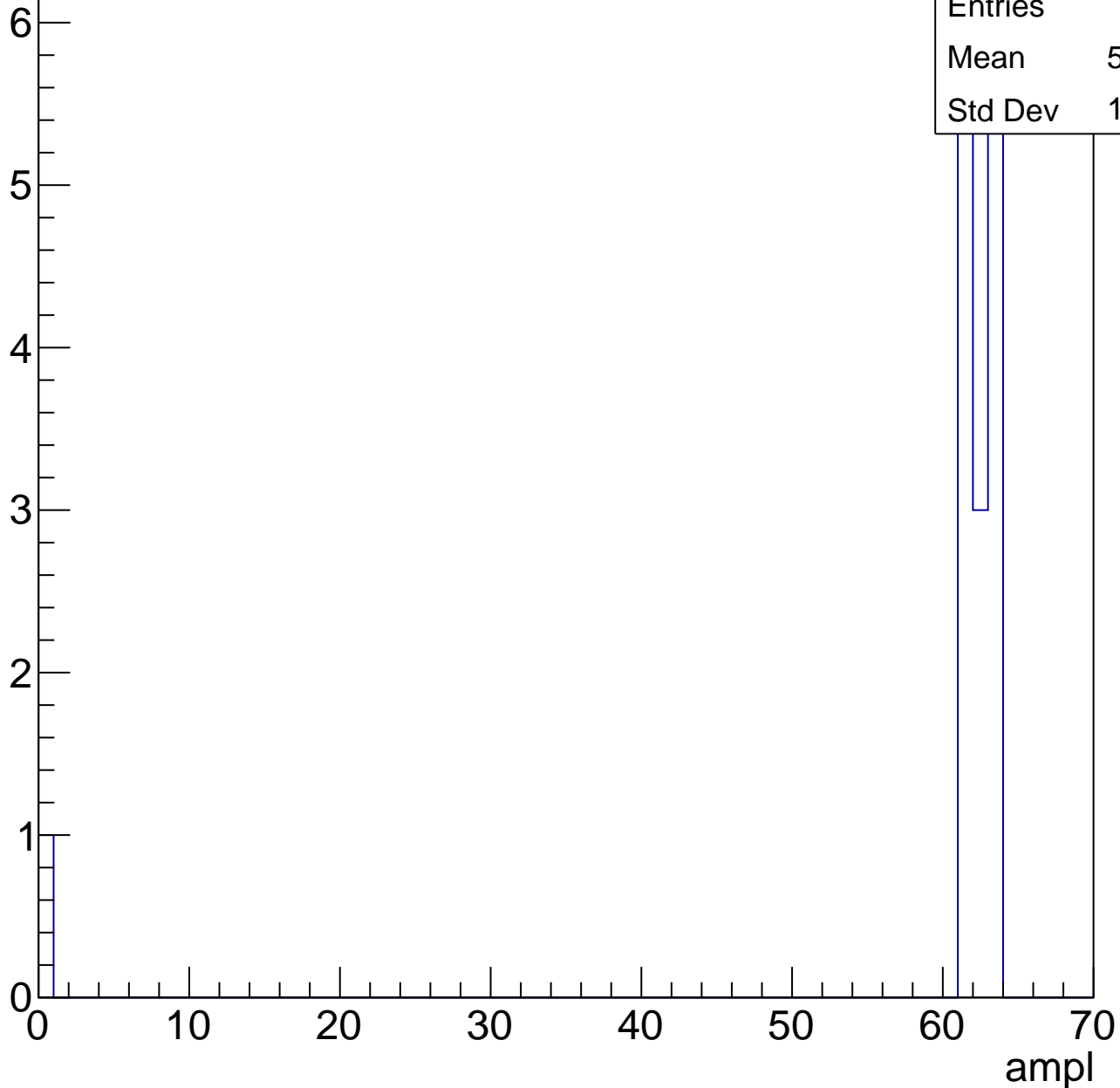


# B1L103S, U3-ch7, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	16
Mean	58.12
Std Dev	15.03

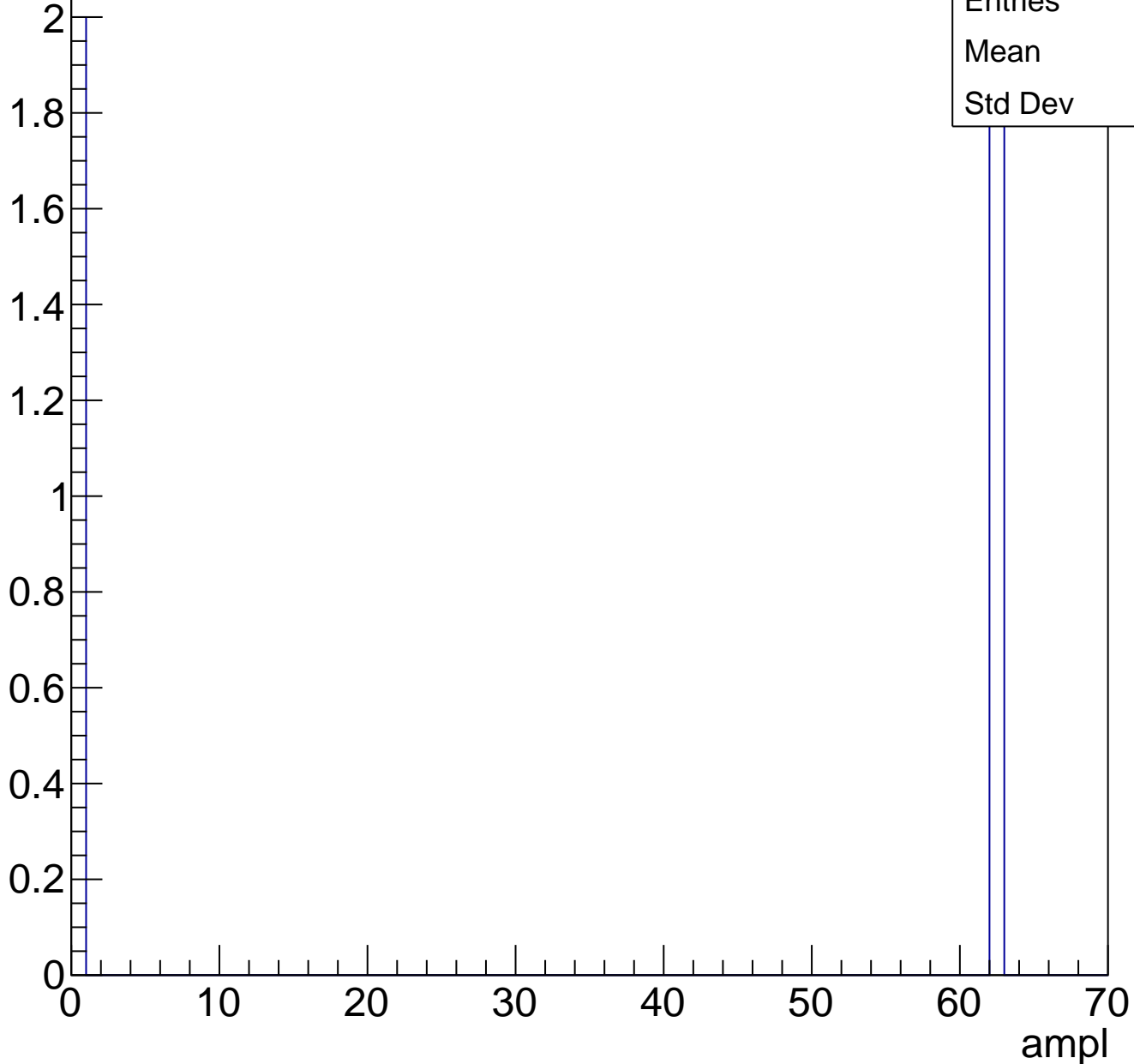




# B1L103S, U3-ch7, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch8, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	92
Mean	28.61
Std Dev	3.986

**Gaus mean : 29.0401**

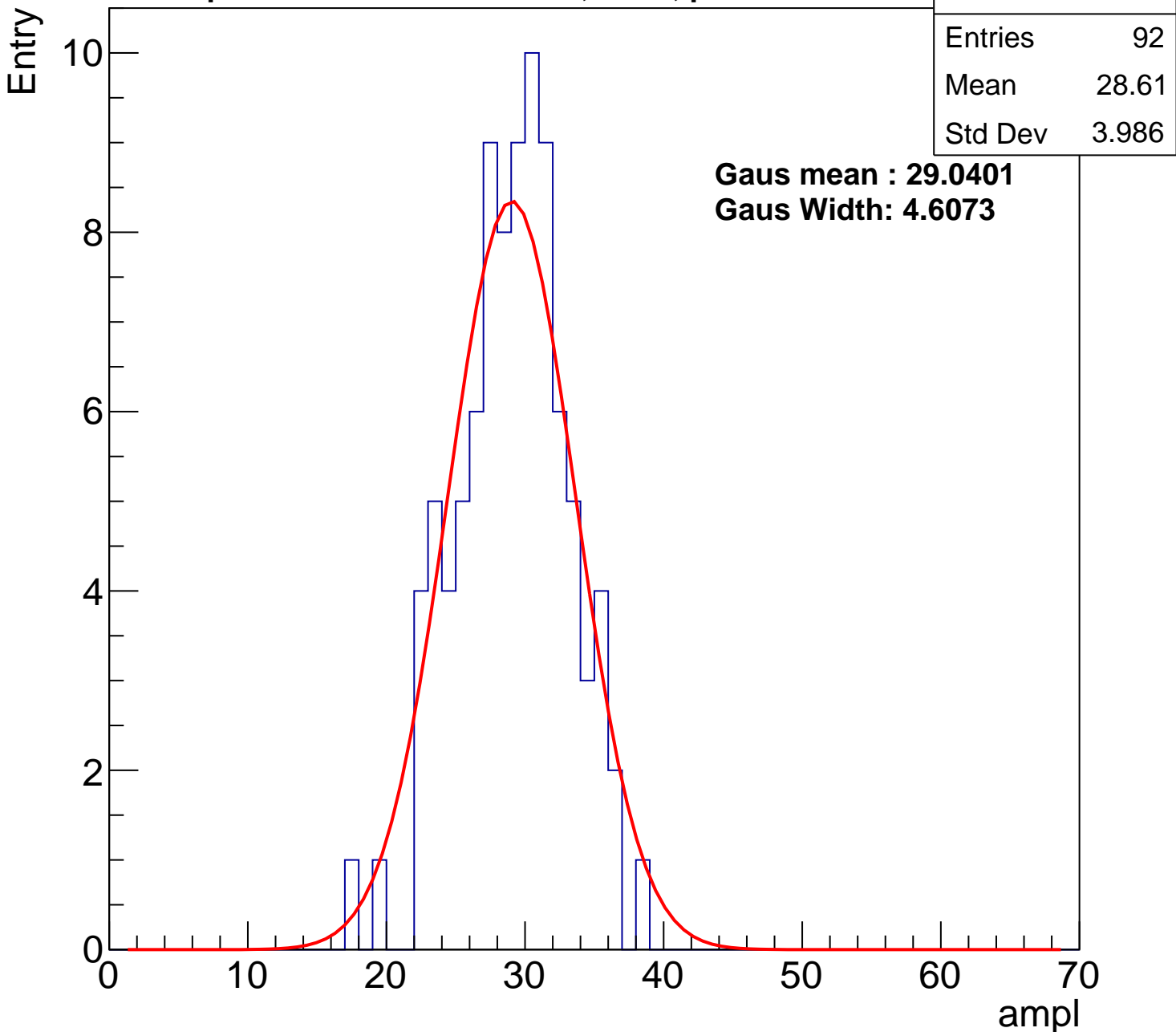
**Gaus Width: 4.6073**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U3-ch8, adc1

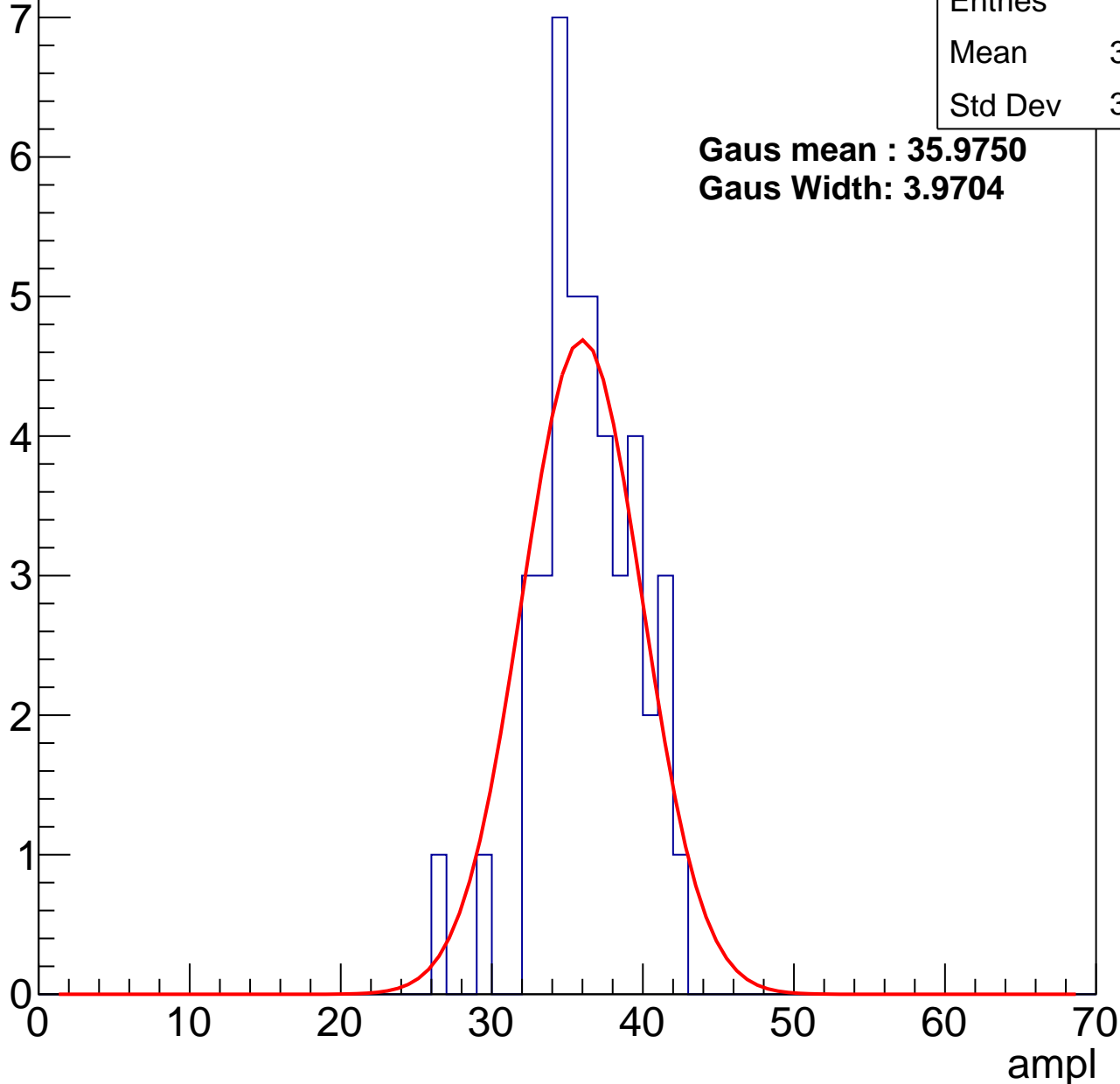
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	42
Mean	35.86
Std Dev	3.277

**Gaus mean : 35.9750**

**Gaus Width: 3.9704**



# B1L103S, U3-ch8, adc2

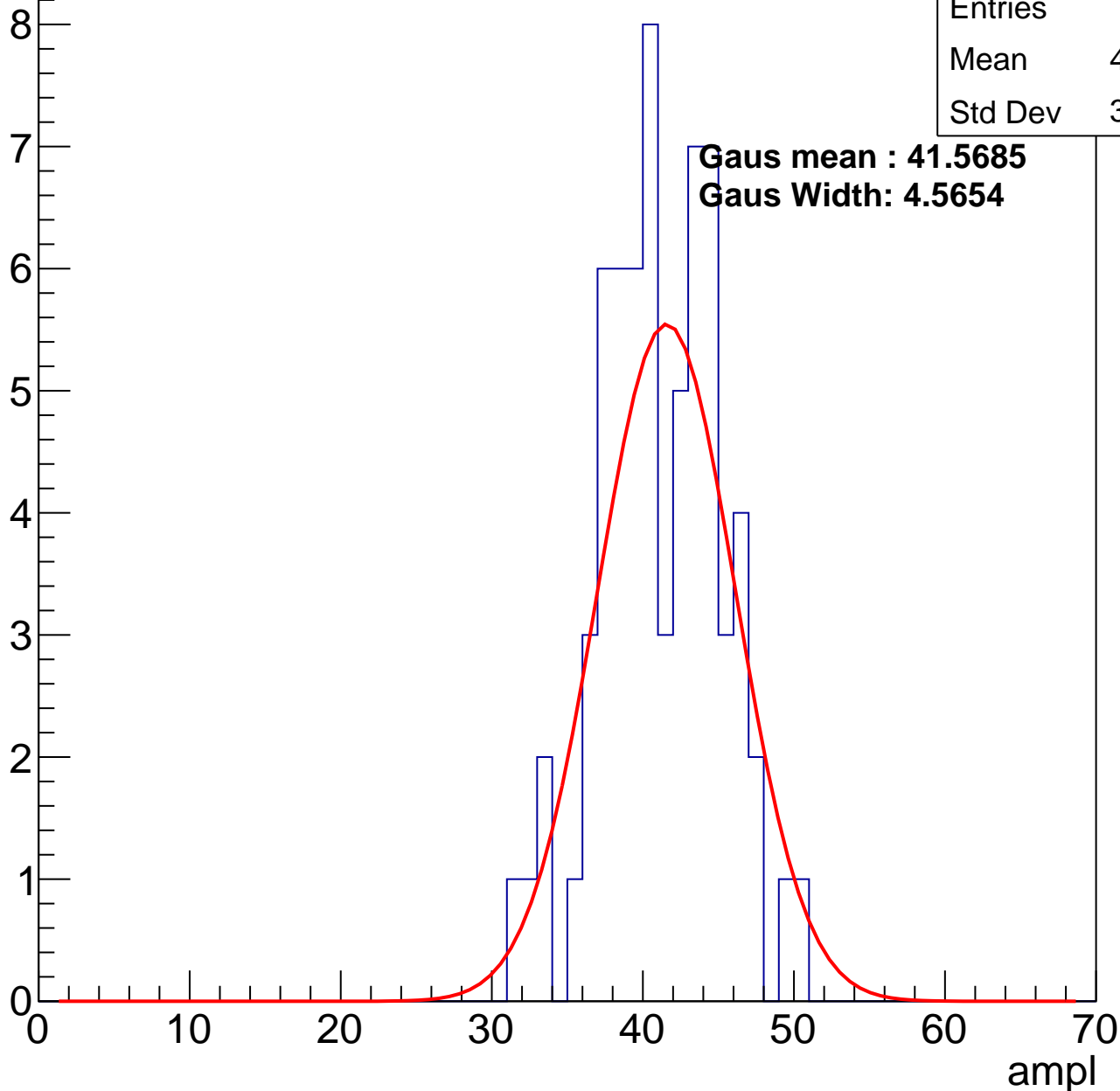
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	40.75
Std Dev	3.975

**Gaus mean : 41.5685**

**Gaus Width: 4.5654**

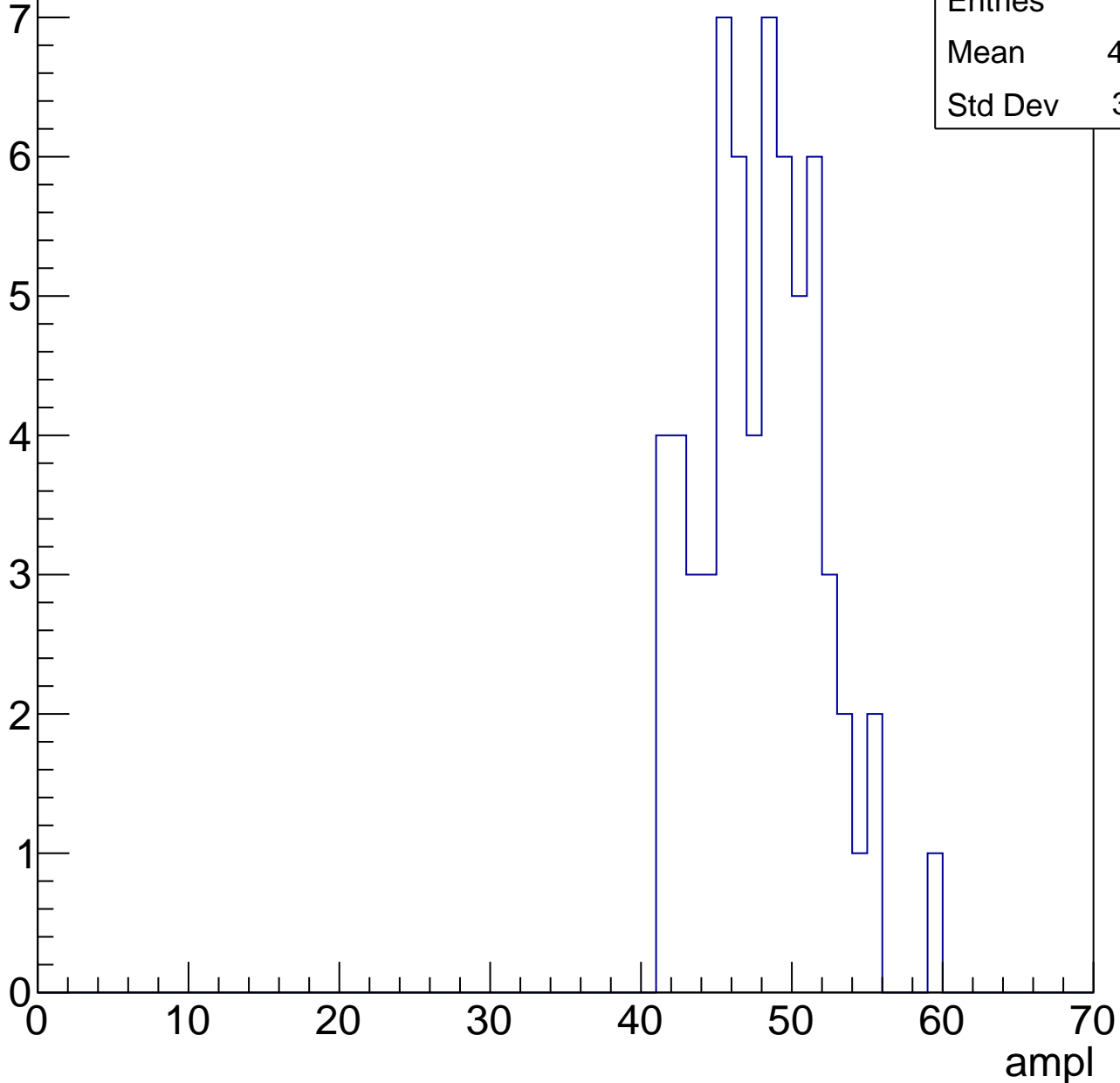


# B1L103S, U3-ch8, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	47.55
Std Dev	3.901

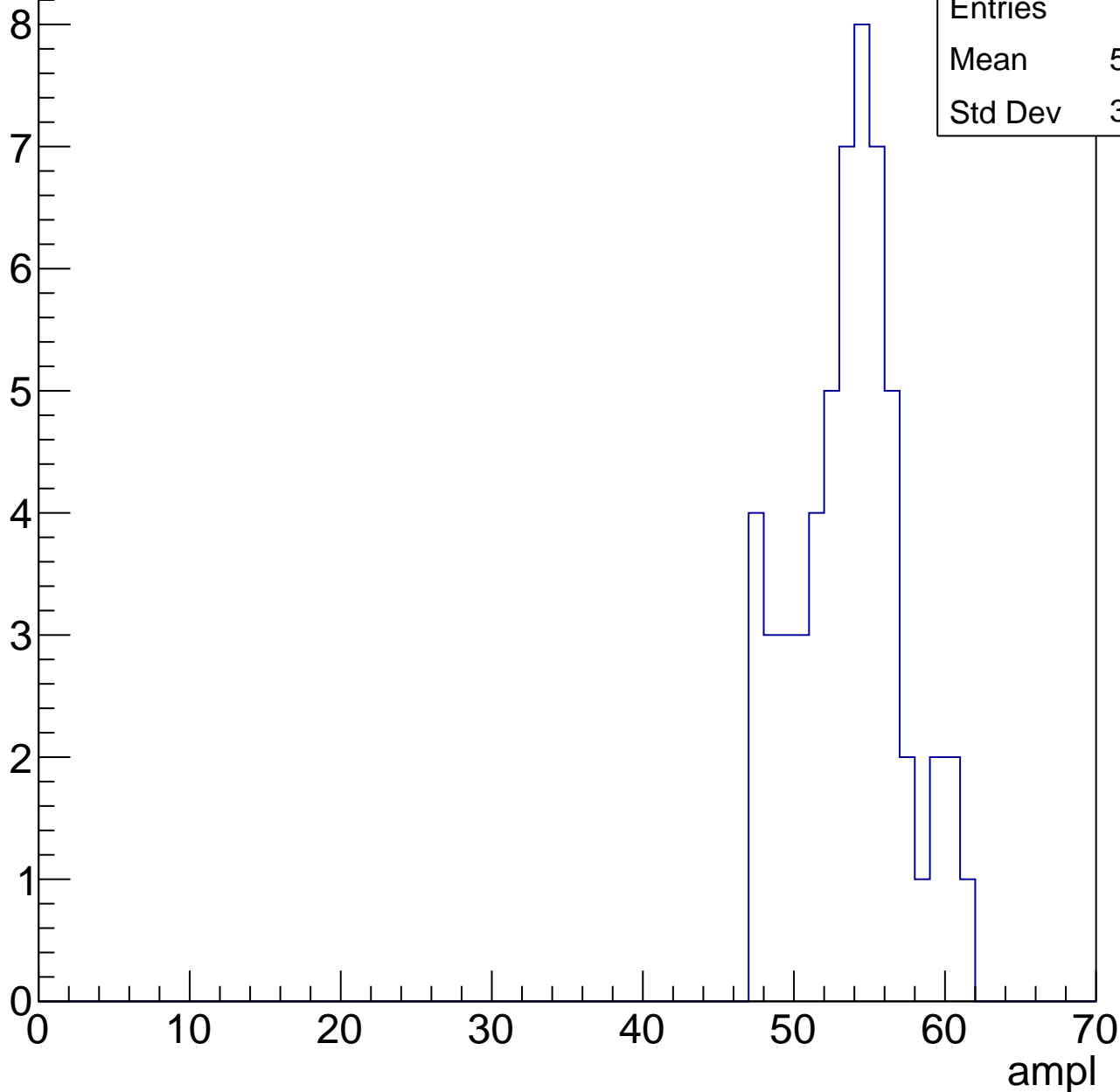


# B1L103S, U3-ch8, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	53.19
Std Dev	3.466

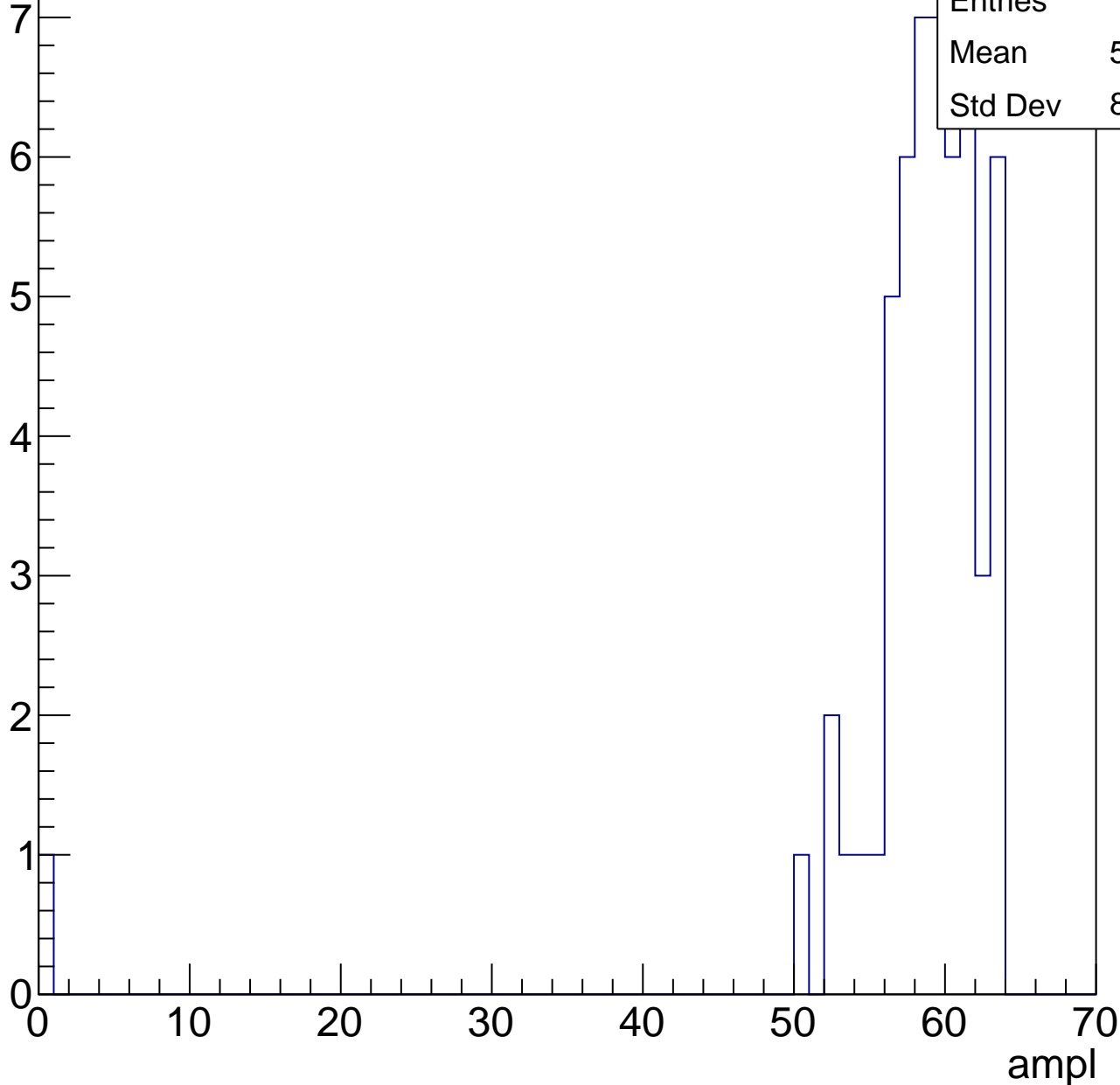


# B1L103S, U3-ch8, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	57.56
Std Dev	8.452

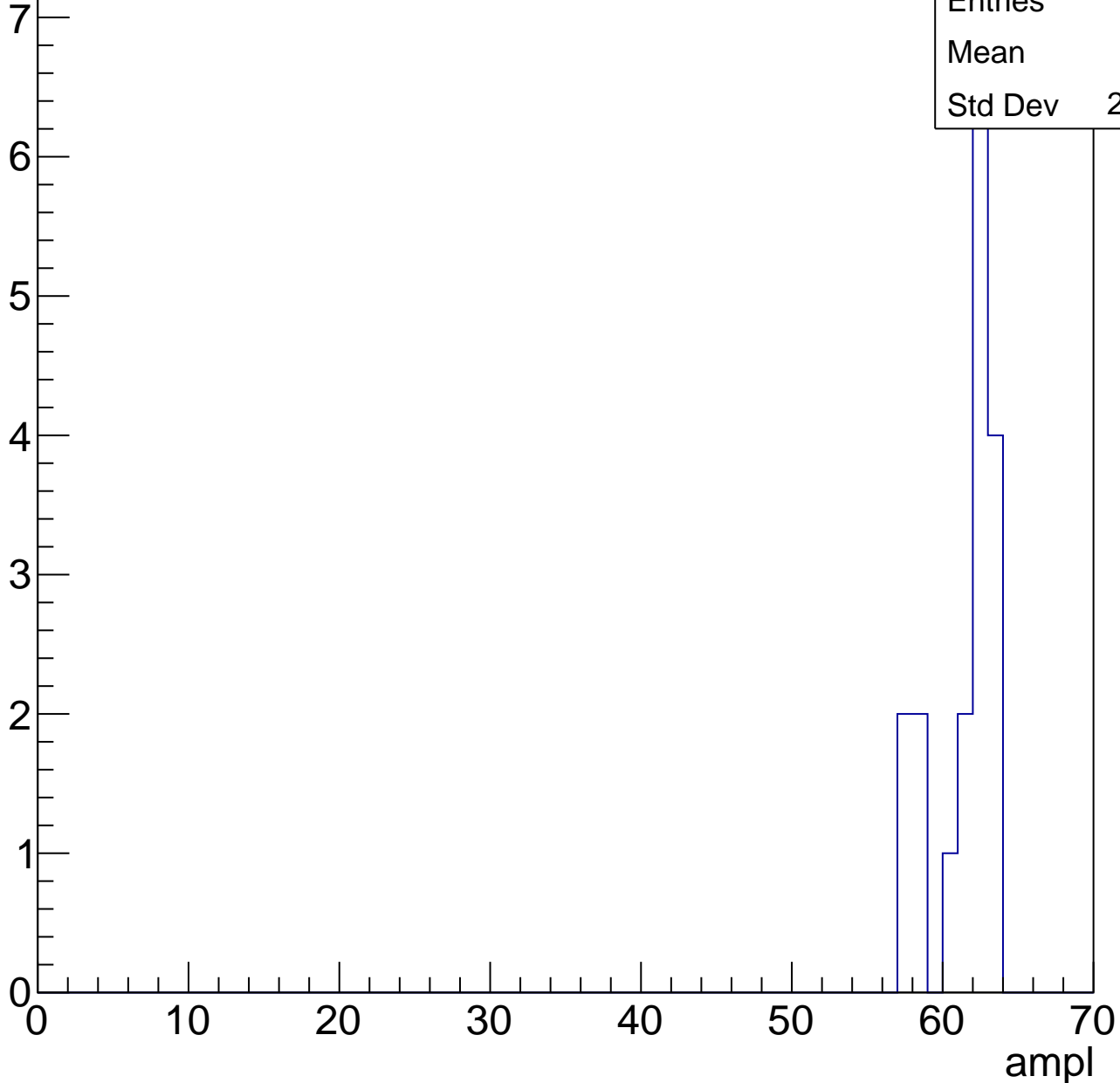


# B1L103S, U3-ch8, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	18
Mean	61
Std Dev	2.028

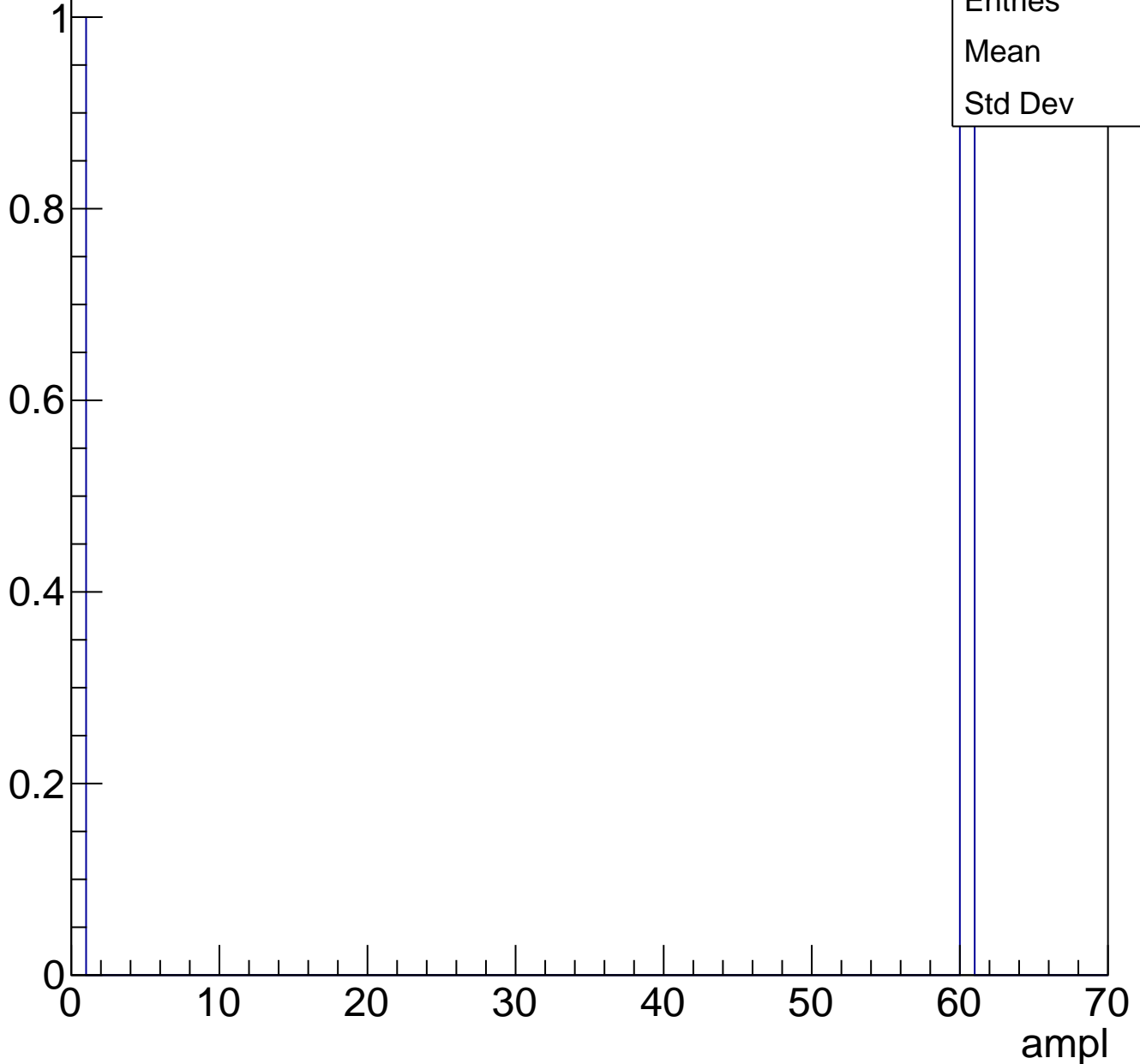




# B1L103S, U3-ch8, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch9, adc0

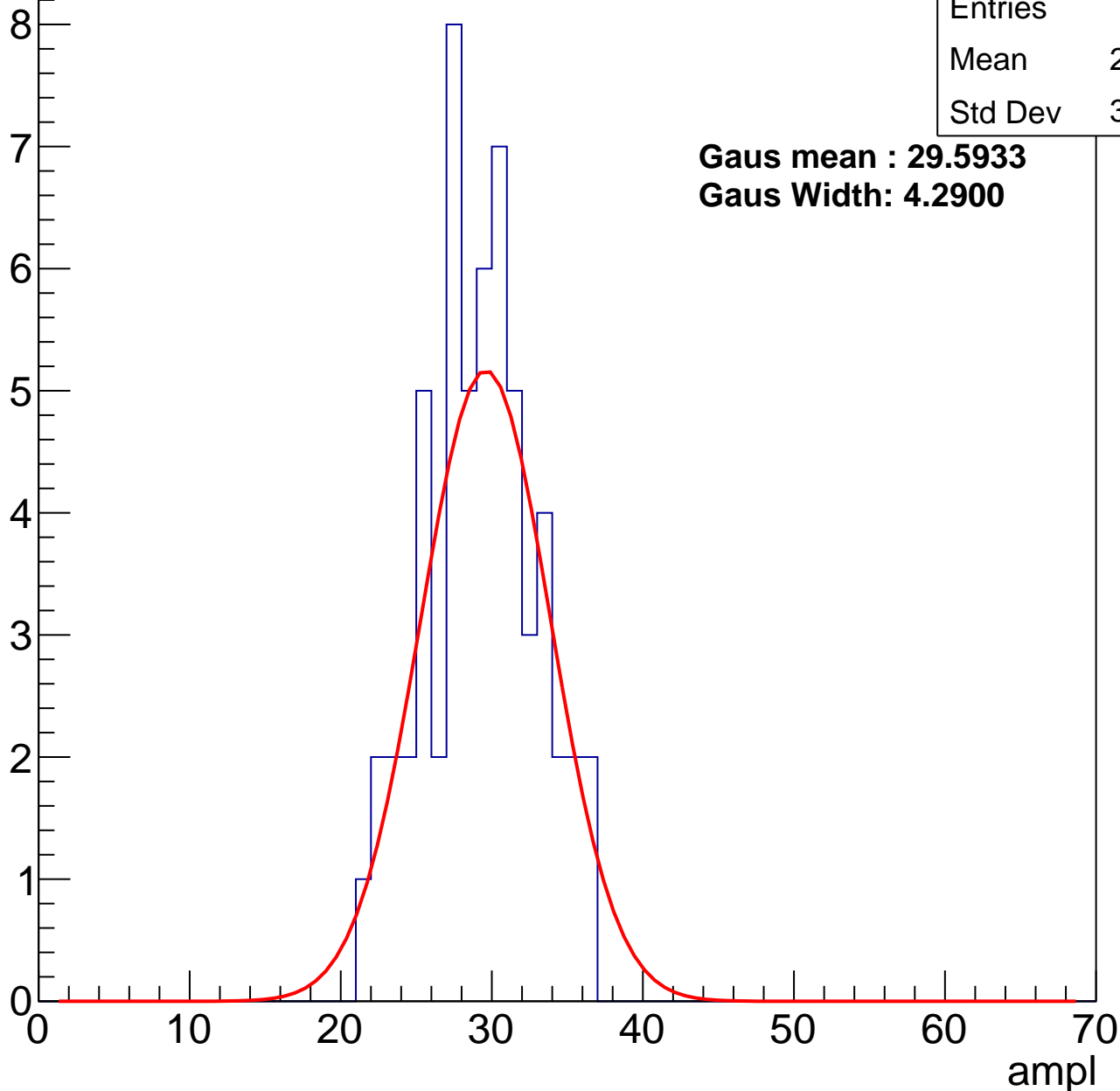
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	28.78
Std Dev	3.606

**Gaus mean : 29.5933**

**Gaus Width: 4.2900**



# B1L103S, U3-ch9, adc1

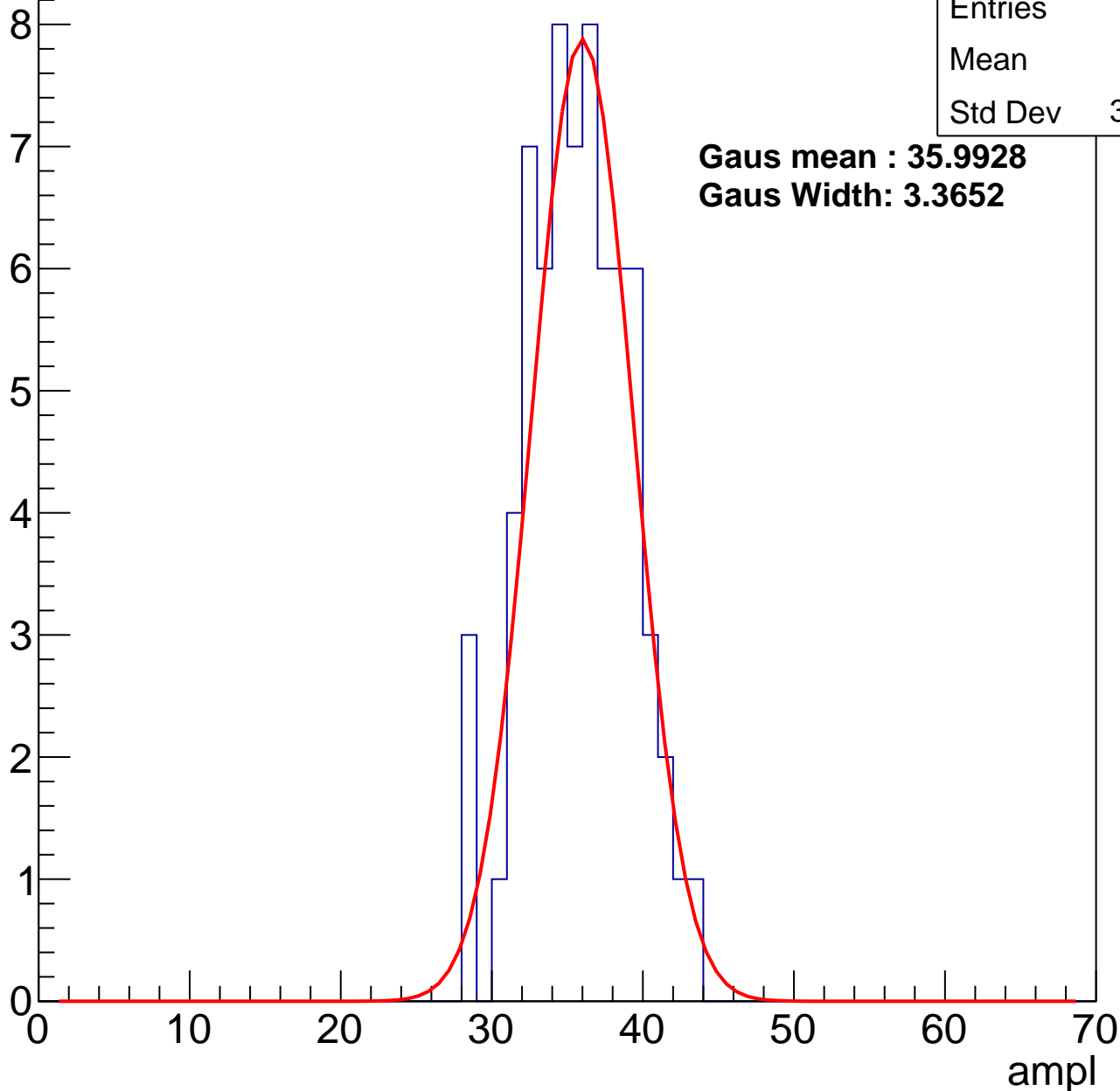
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	35.3
Std Dev	3.333

**Gaus mean : 35.9928**

**Gaus Width: 3.3652**



# B1L103S, U3-ch9, adc2

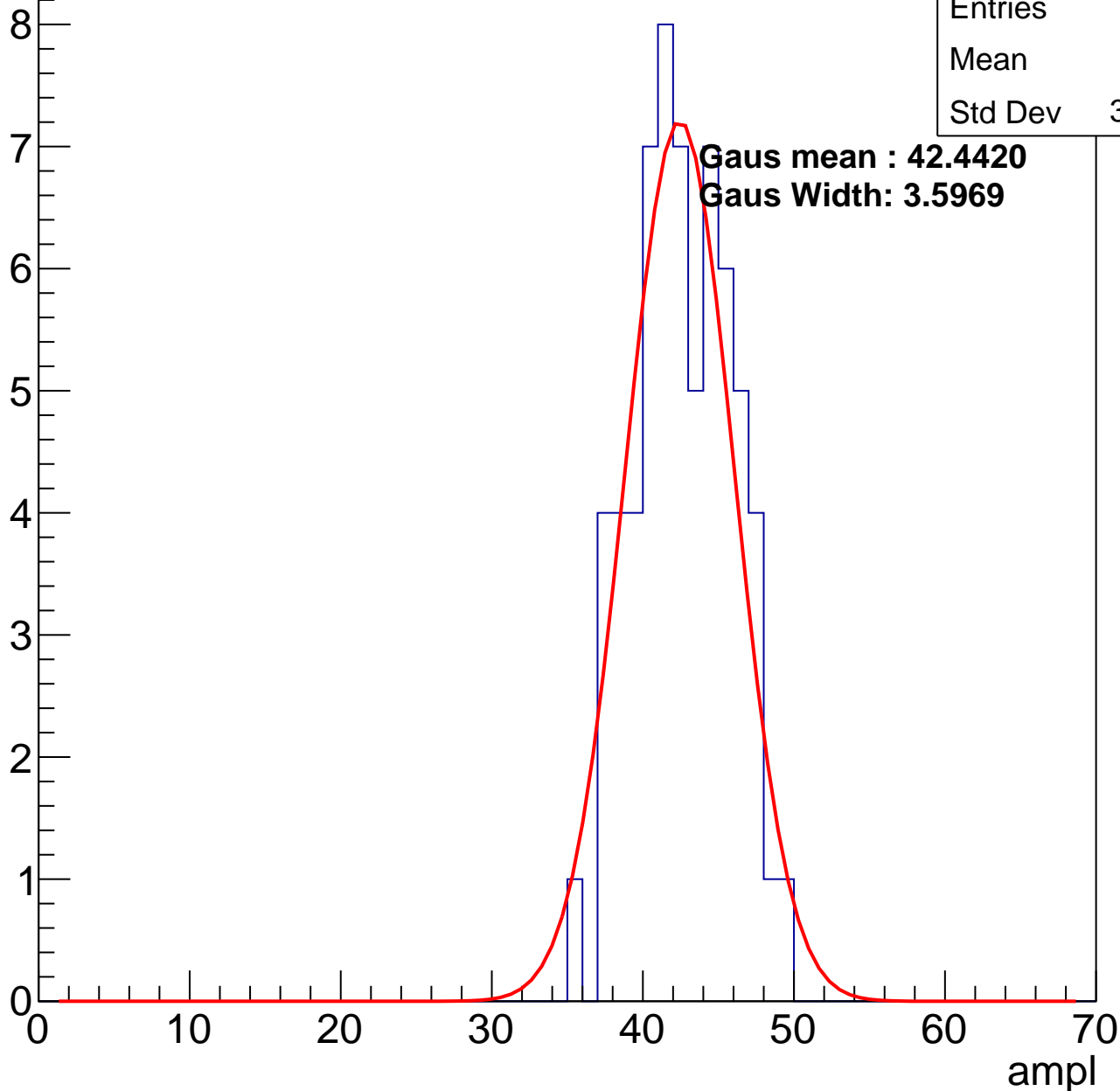
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	42.2
Std Dev	3.148

**Gaus mean : 42.4420**

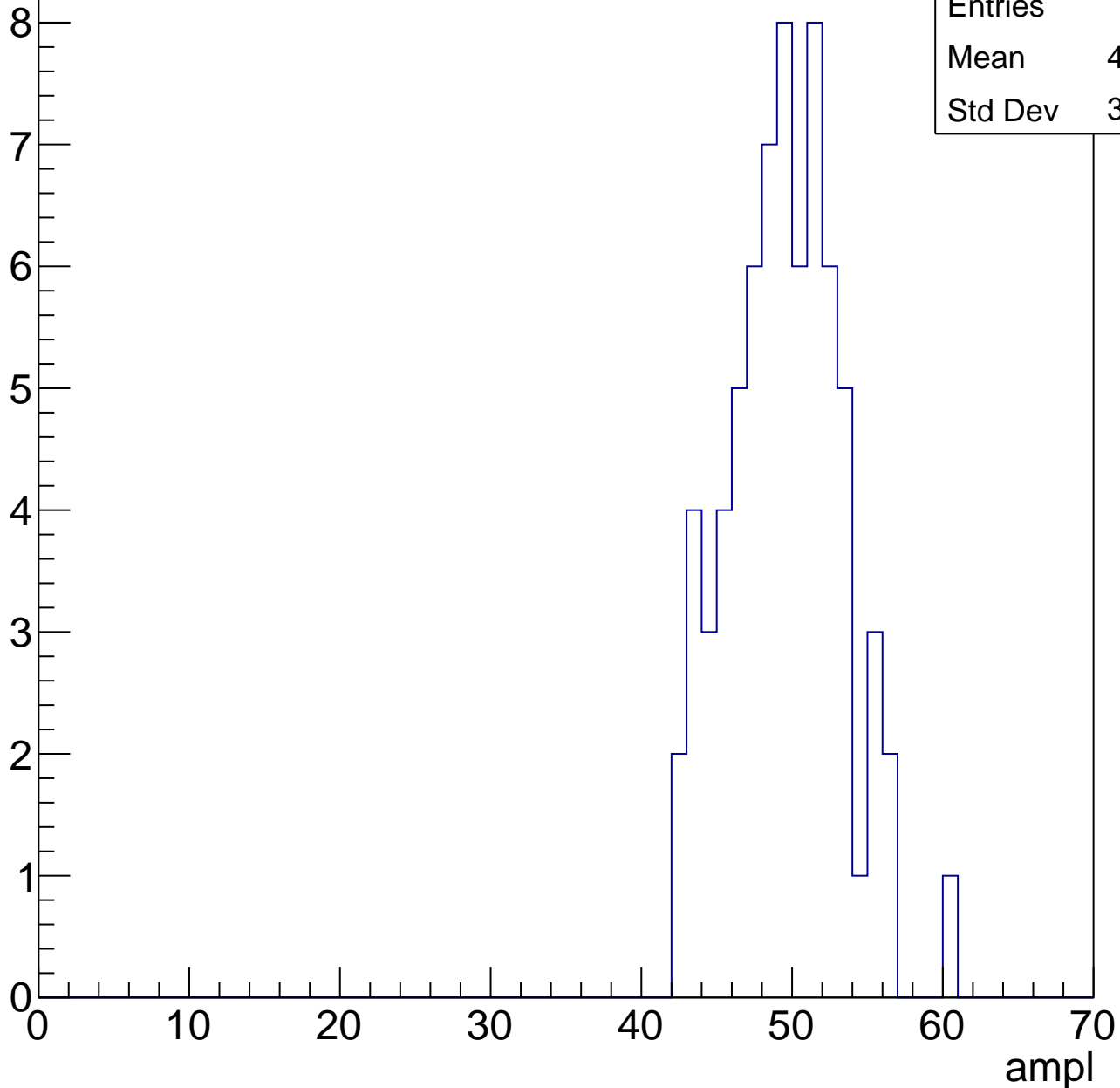
**Gaus Width: 3.5969**



# B1L103S, U3-ch9, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



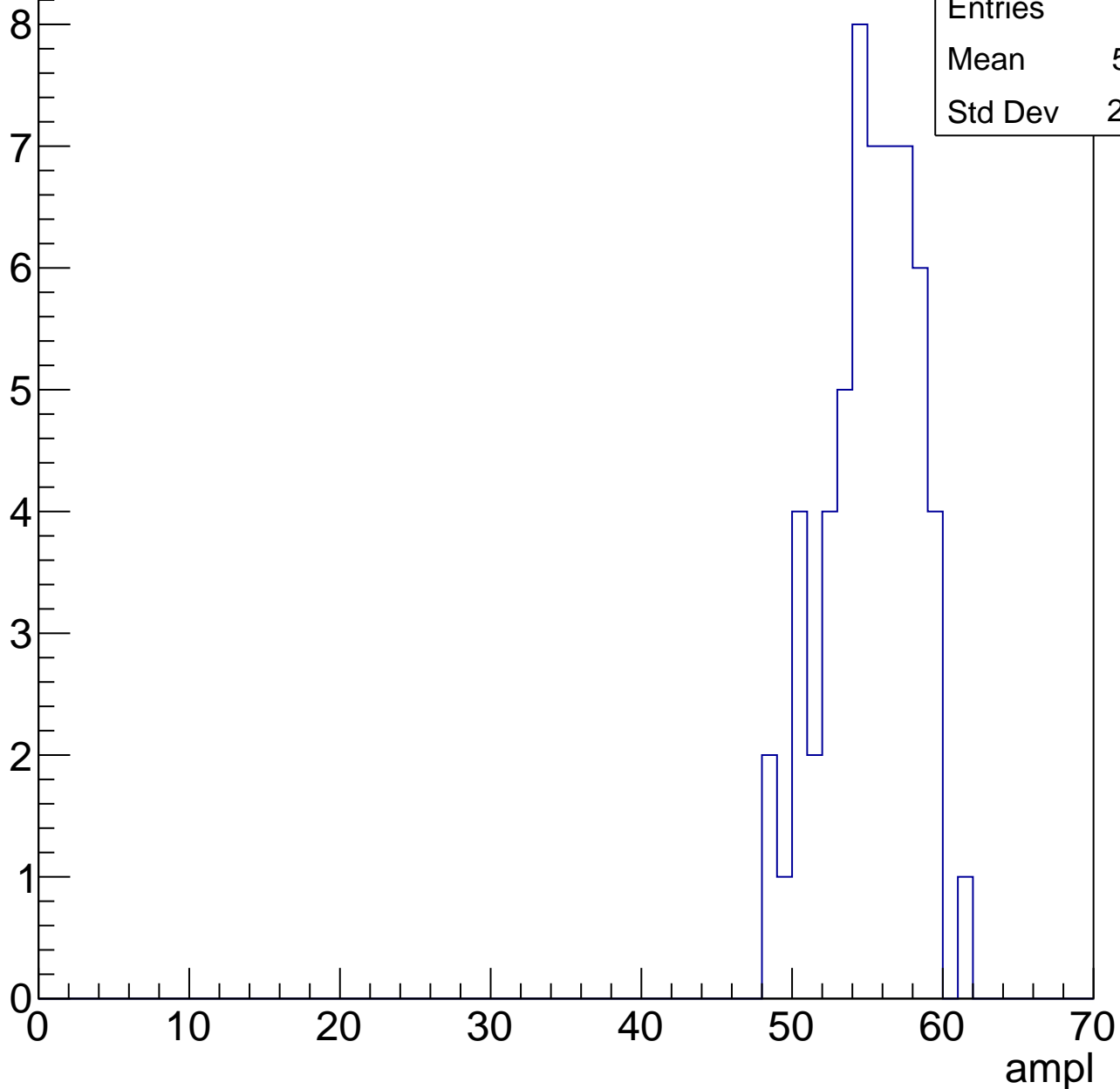
Entries	71
Mean	49.07
Std Dev	3.716

# B1L103S, U3-ch9, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

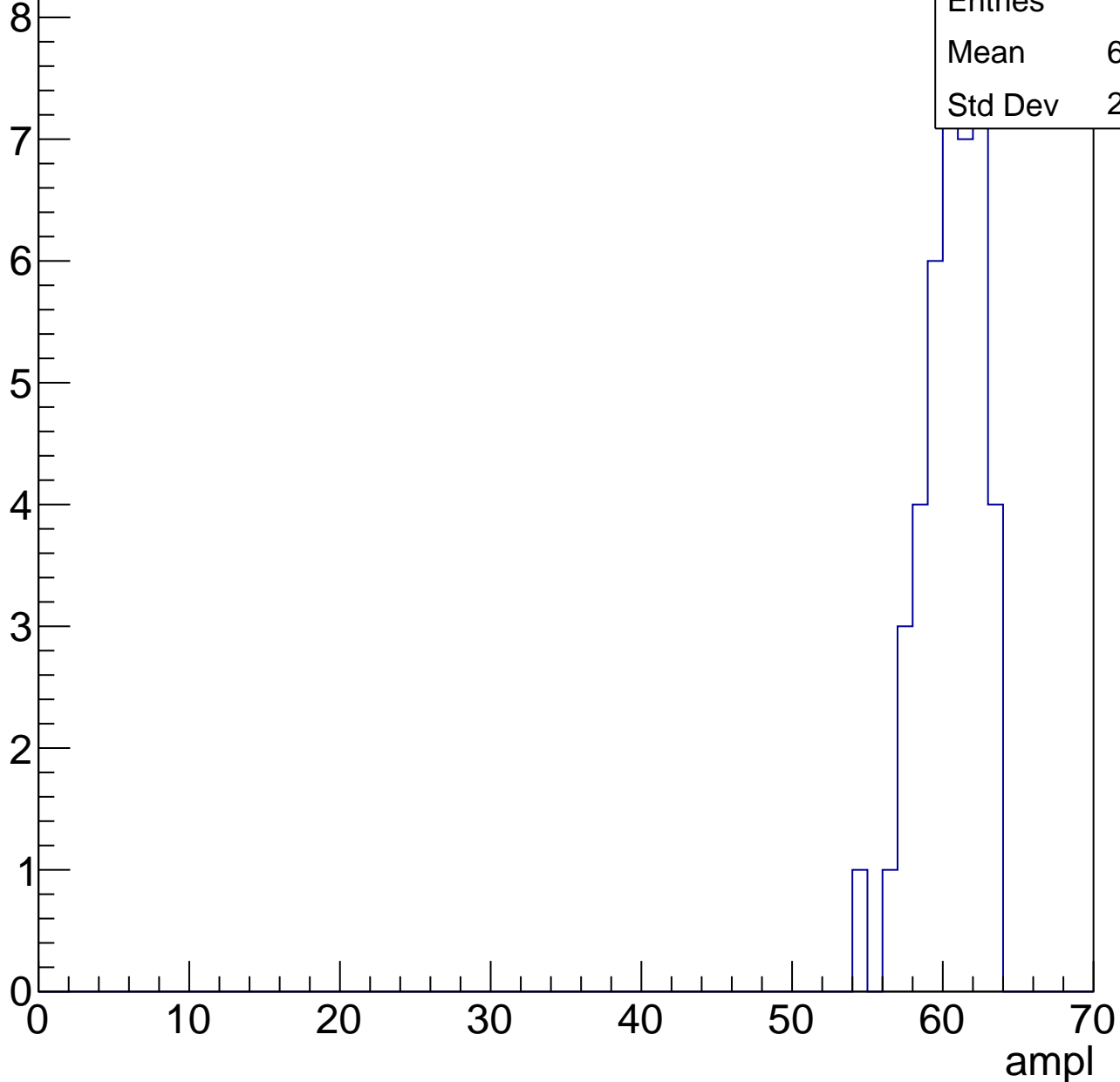
Entries	58
Mean	54.71
Std Dev	2.977



# B1L103S, U3-ch9, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

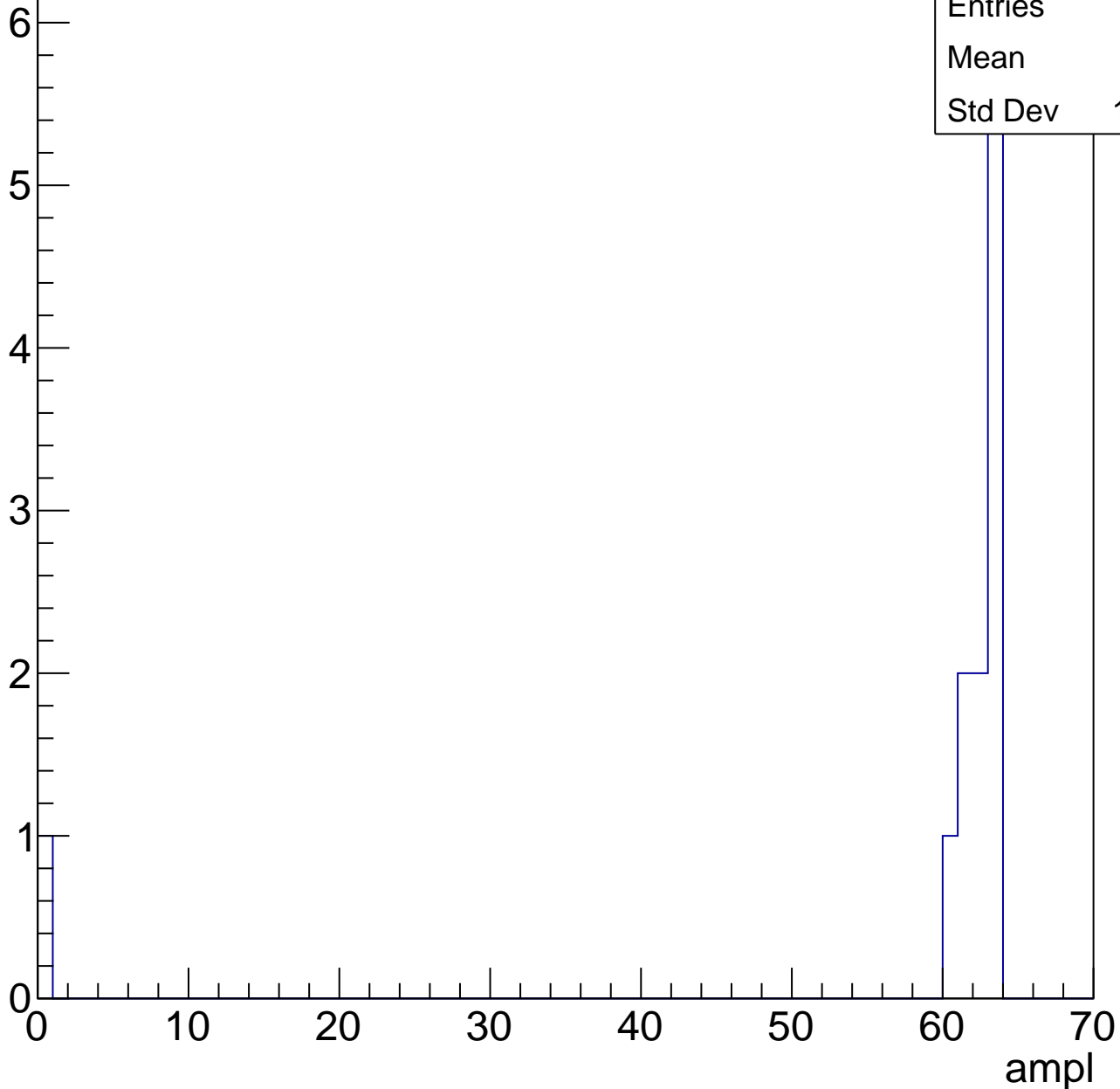


# B1L103S, U3-ch9, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	12
Mean	57
Std Dev	17.21





# B1L103S, U3-ch9, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U3-ch10, adc0

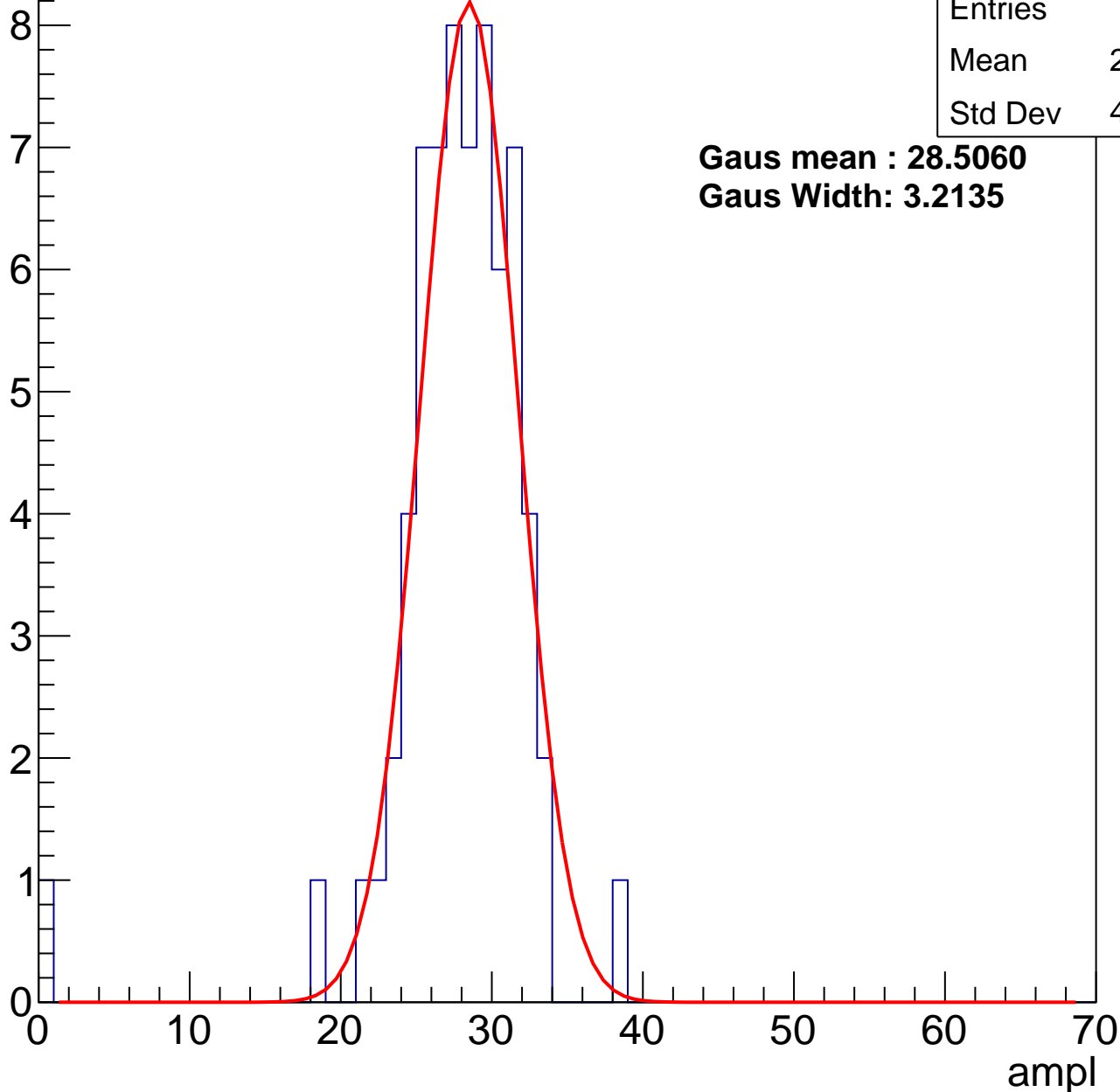
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	27.36
Std Dev	4.674

**Gaus mean : 28.5060**

**Gaus Width: 3.2135**



# B1L103S, U3-ch10, adc1

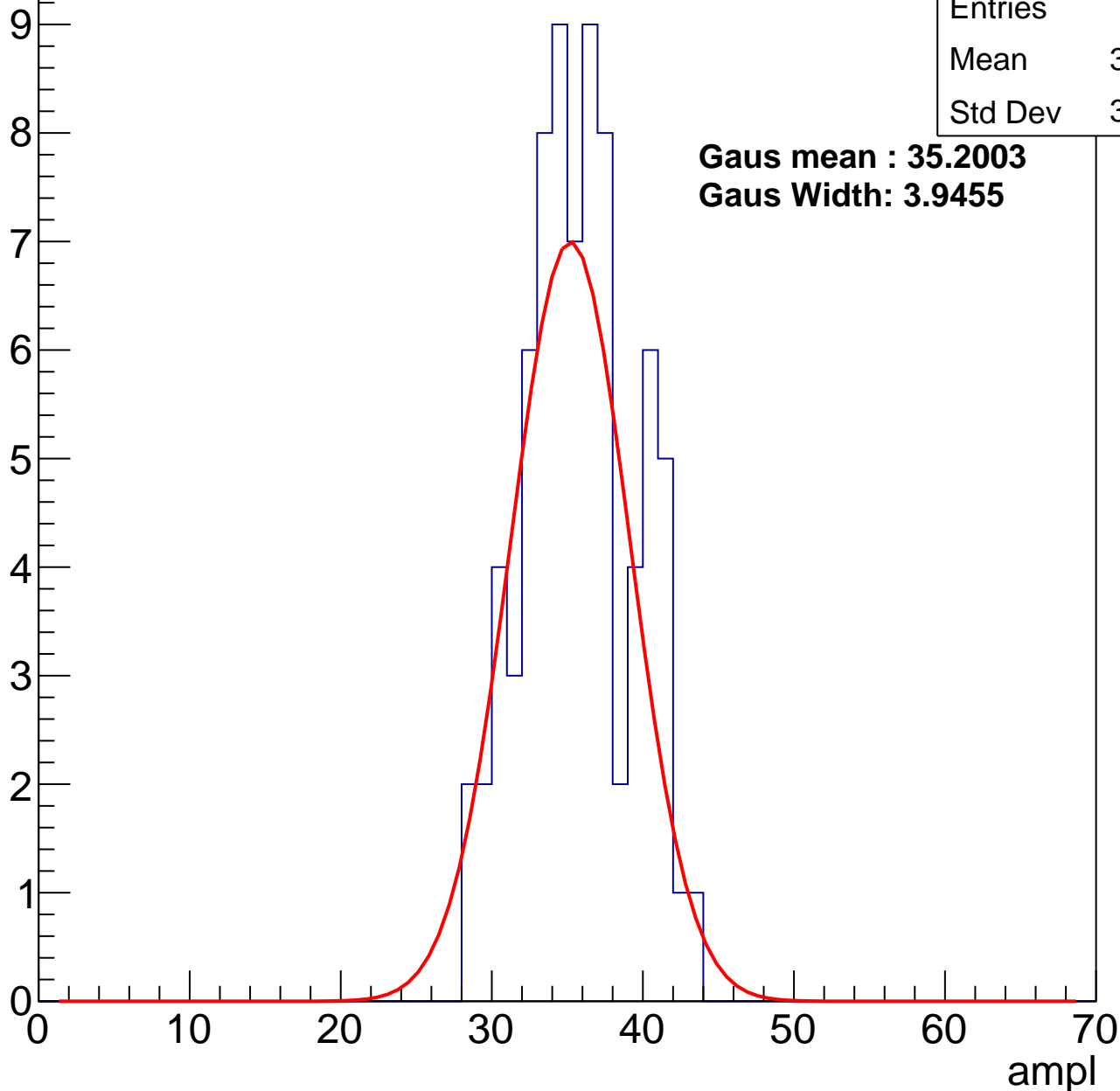
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	35.27
Std Dev	3.555

**Gaus mean : 35.2003**

**Gaus Width: 3.9455**



# B1L103S, U3-ch10, adc2

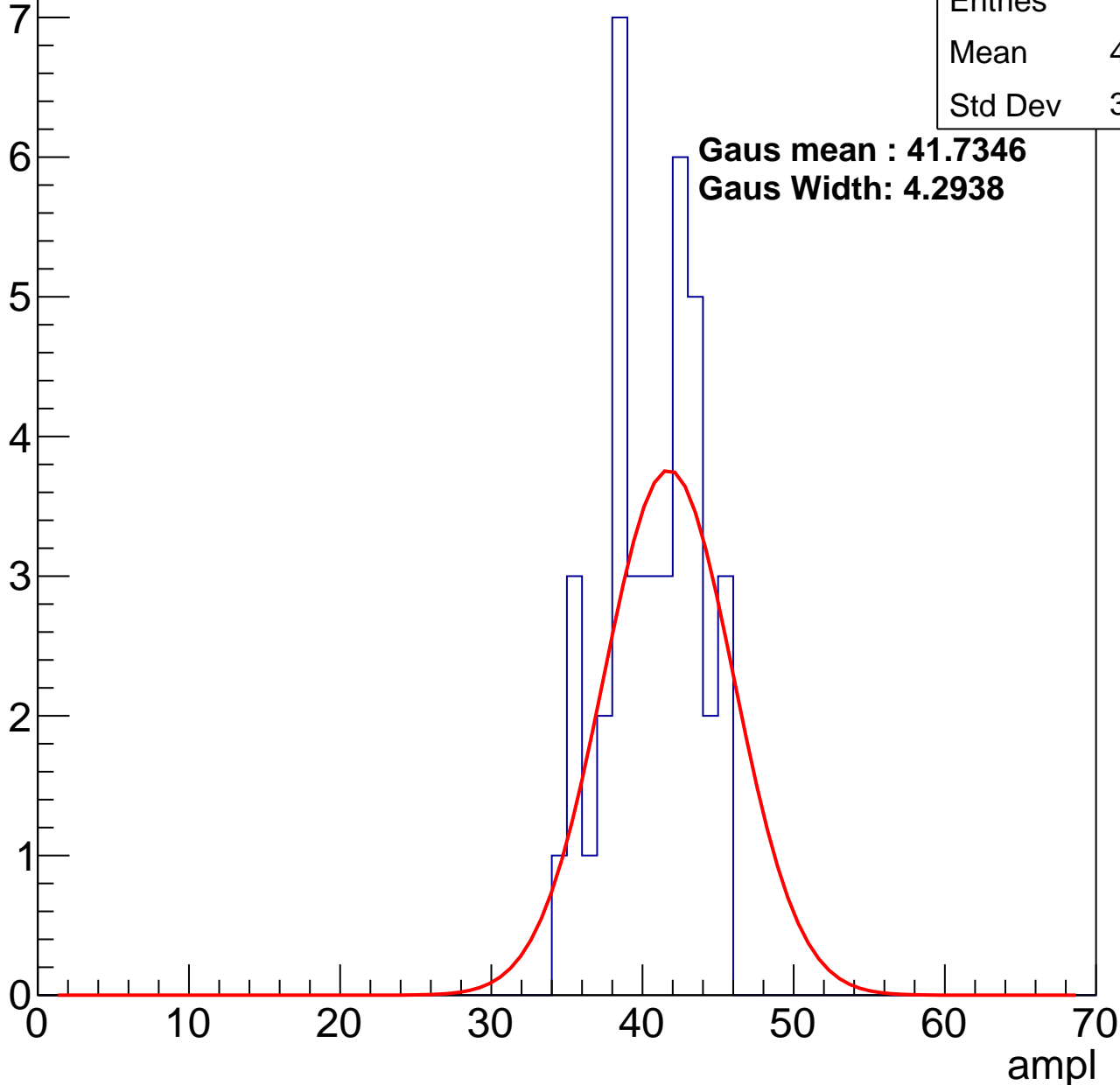
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	39
Mean	40.13
Std Dev	3.014

**Gaus mean : 41.7346**

**Gaus Width: 4.2938**



# B1L103S, U3-ch10, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	84
Mean	47.44
Std Dev	4.23

Entry

10

8

6

4

2

0

0

10

20

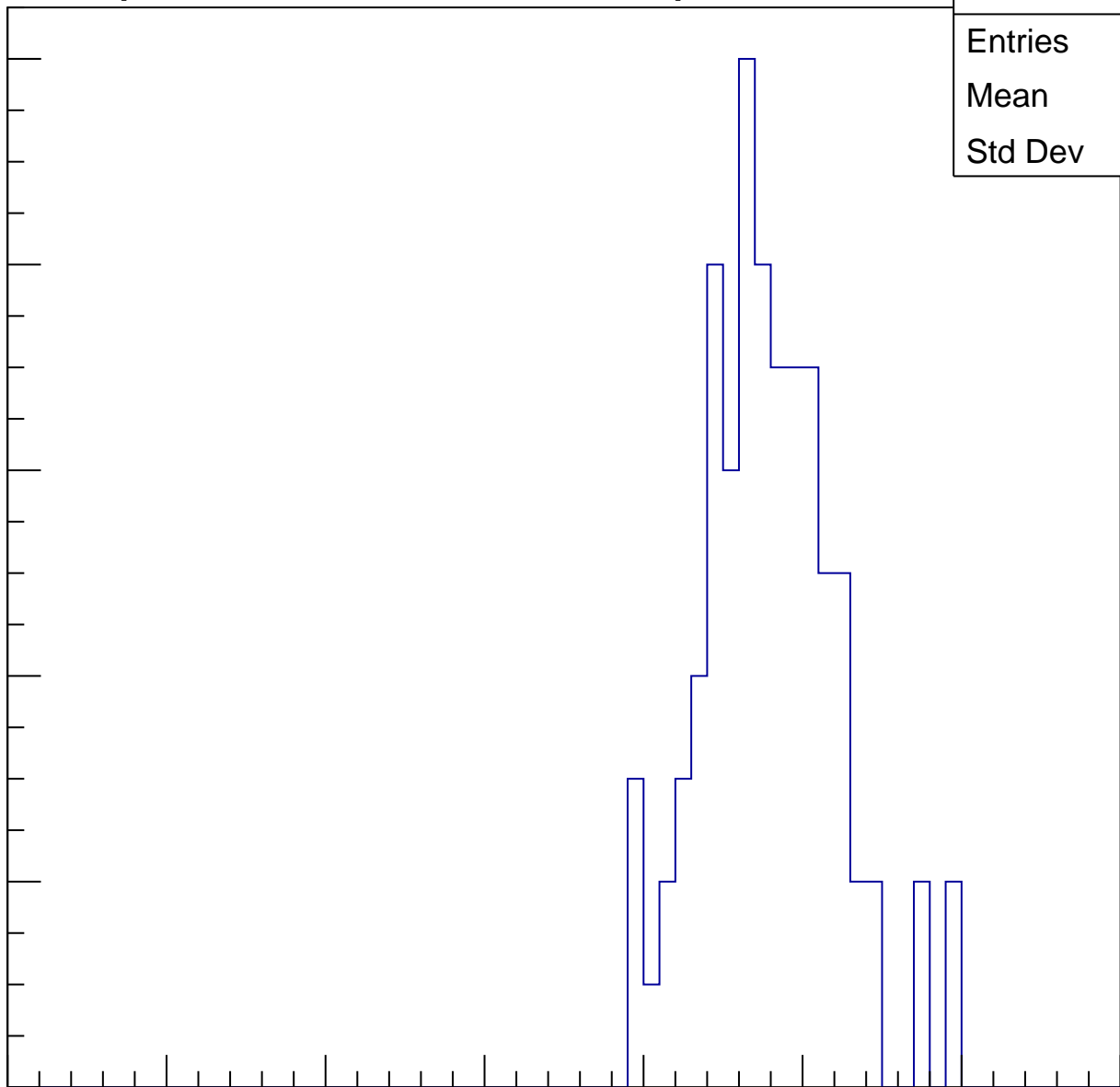
30

40

50

60

ampl

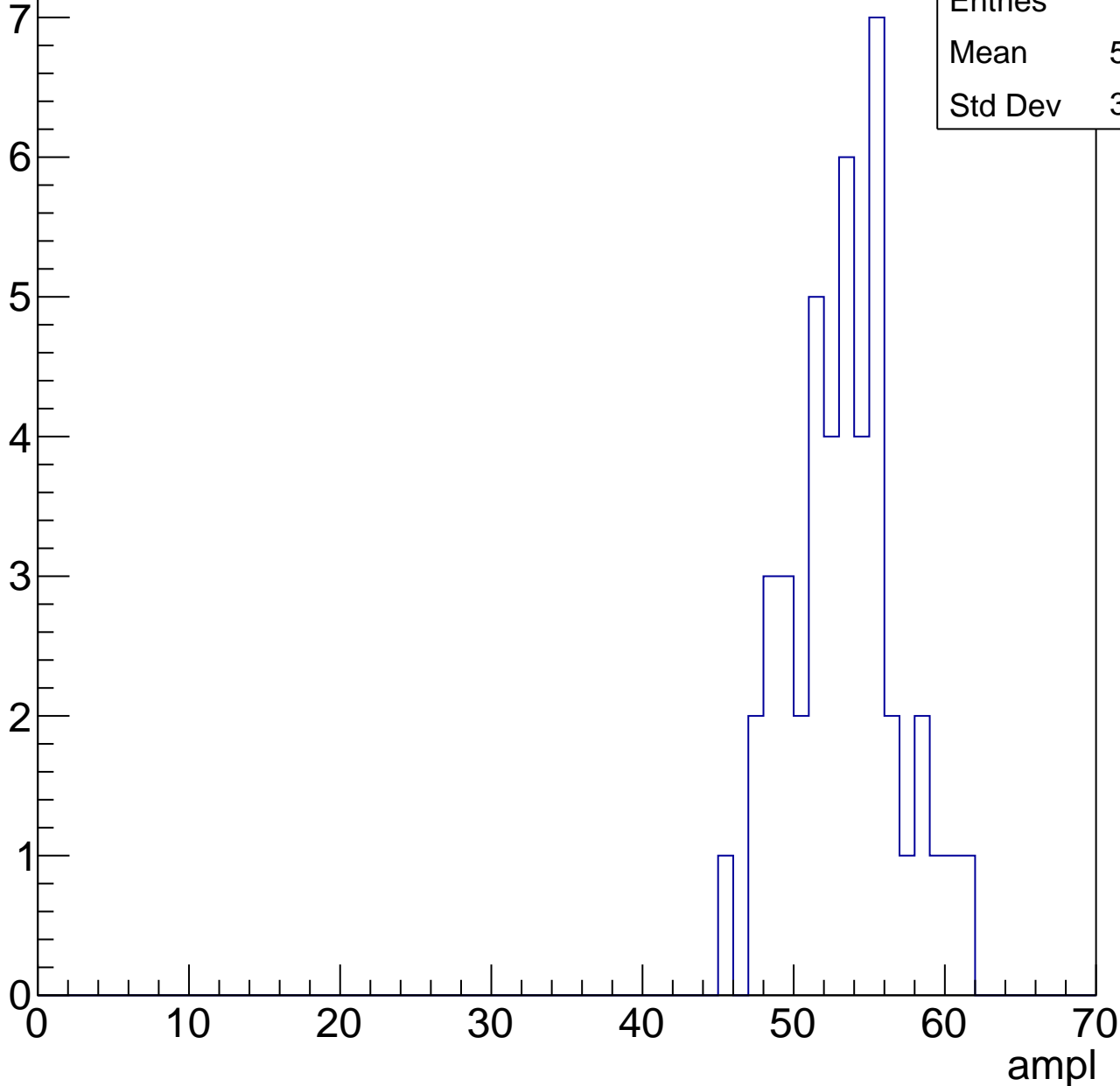


# B1L103S, U3-ch10, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	45
Mean	52.82
Std Dev	3.542

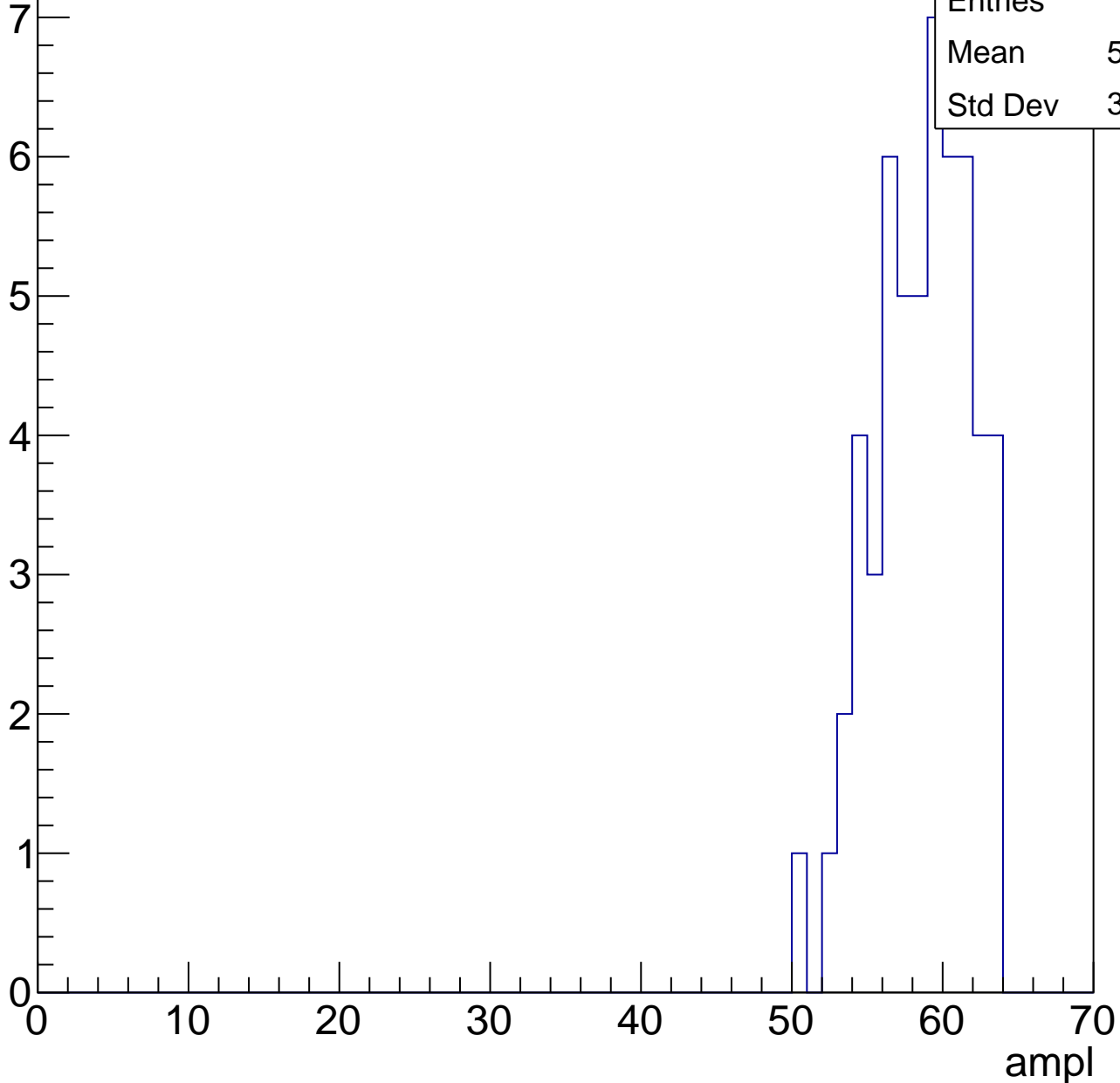


# B1L103S, U3-ch10, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	58.13
Std Dev	3.097

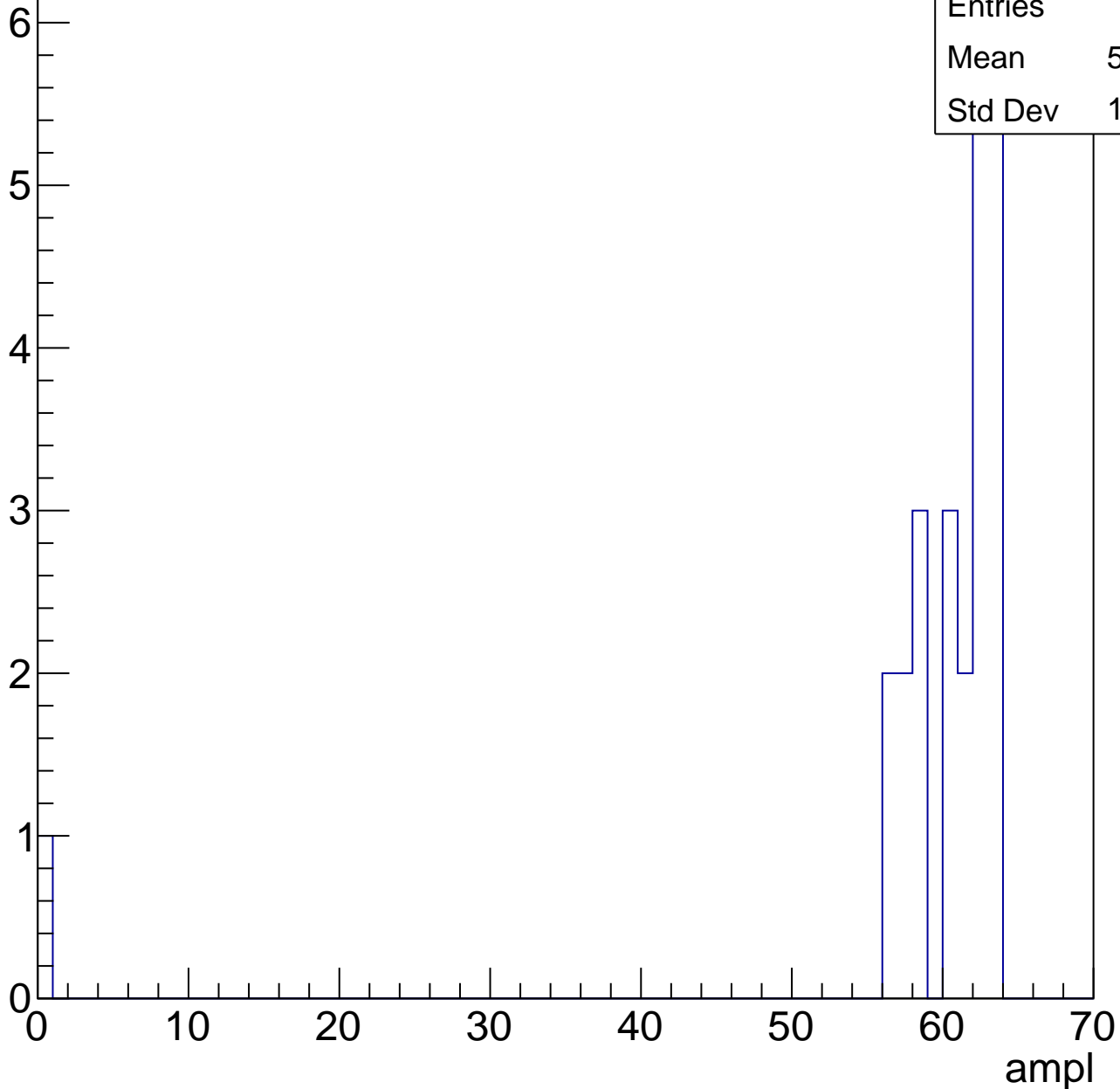


# B1L103S, U3-ch10, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	25
Mean	58.08
Std Dev	12.08





# B1L103S, U3-ch10, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch11, adc0

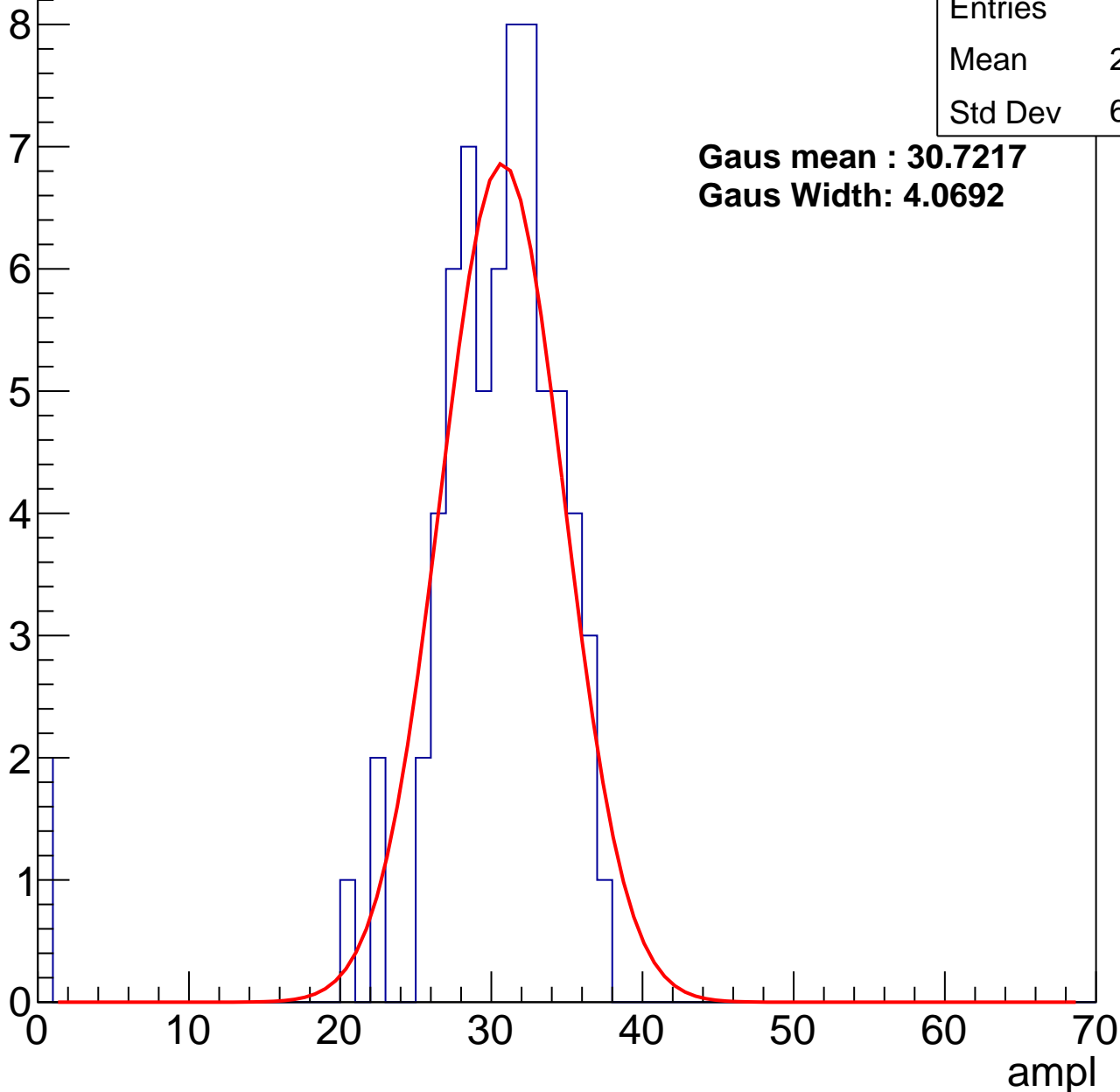
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	29.35
Std Dev	6.164

**Gaus mean : 30.7217**

**Gaus Width: 4.0692**



# B1L103S, U3-ch11, adc1

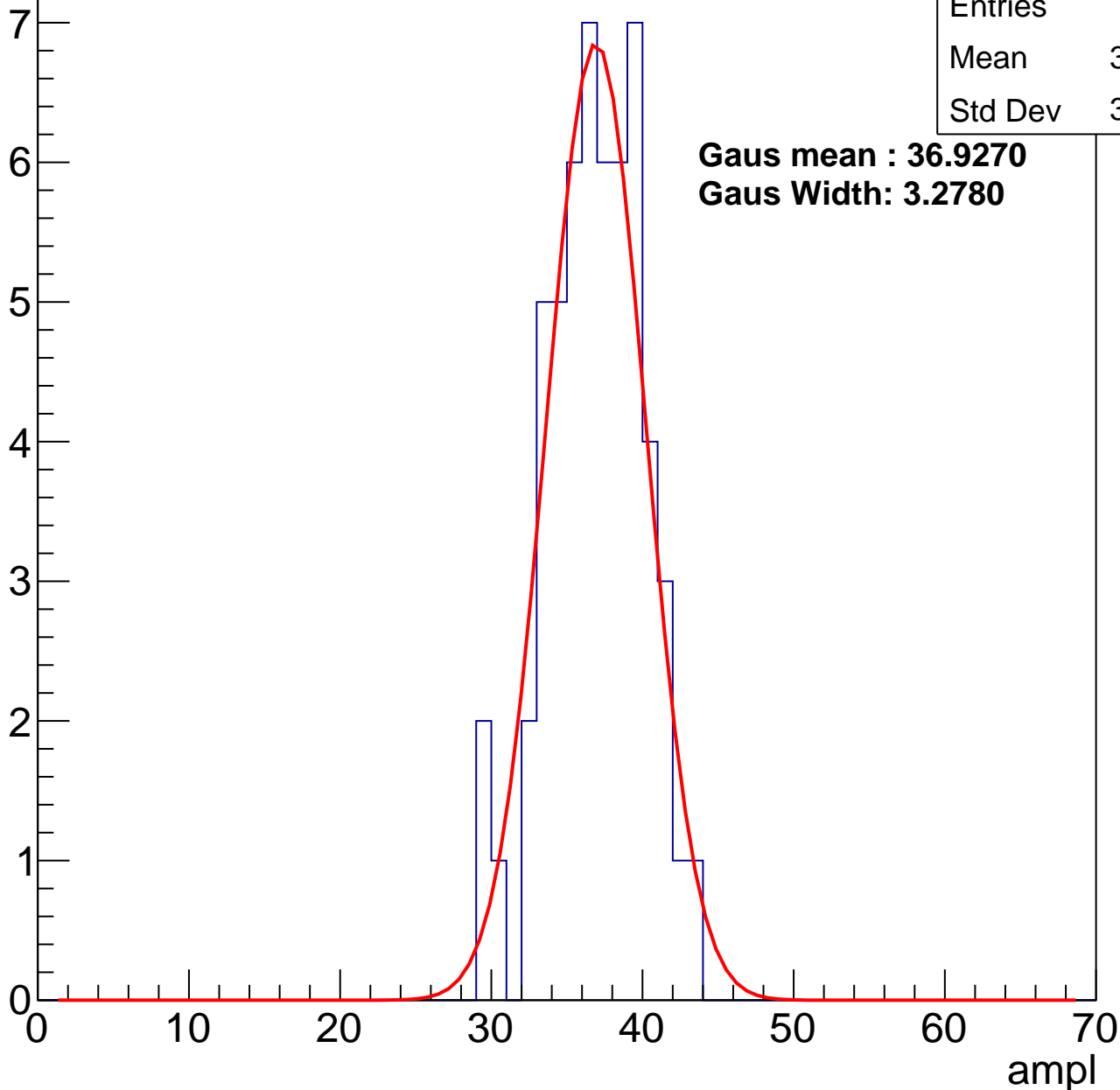
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	36.43
Std Dev	3.116

**Gaus mean : 36.9270**

**Gaus Width: 3.2780**



# B1L103S, U3-ch11, adc2

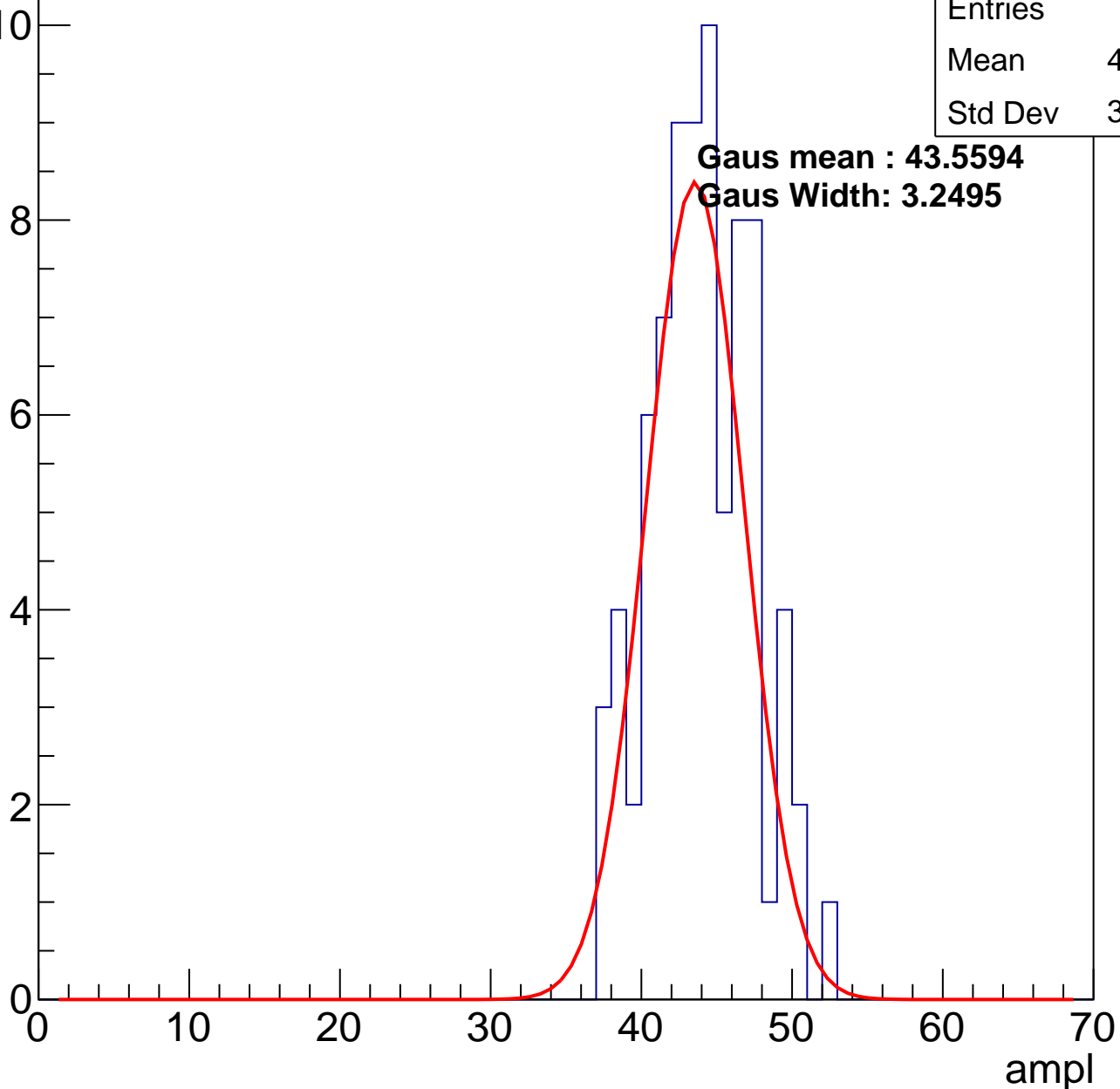
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	79
Mean	43.52
Std Dev	3.352

**Gaus mean : 43.5594**

**Gaus Width: 3.2495**

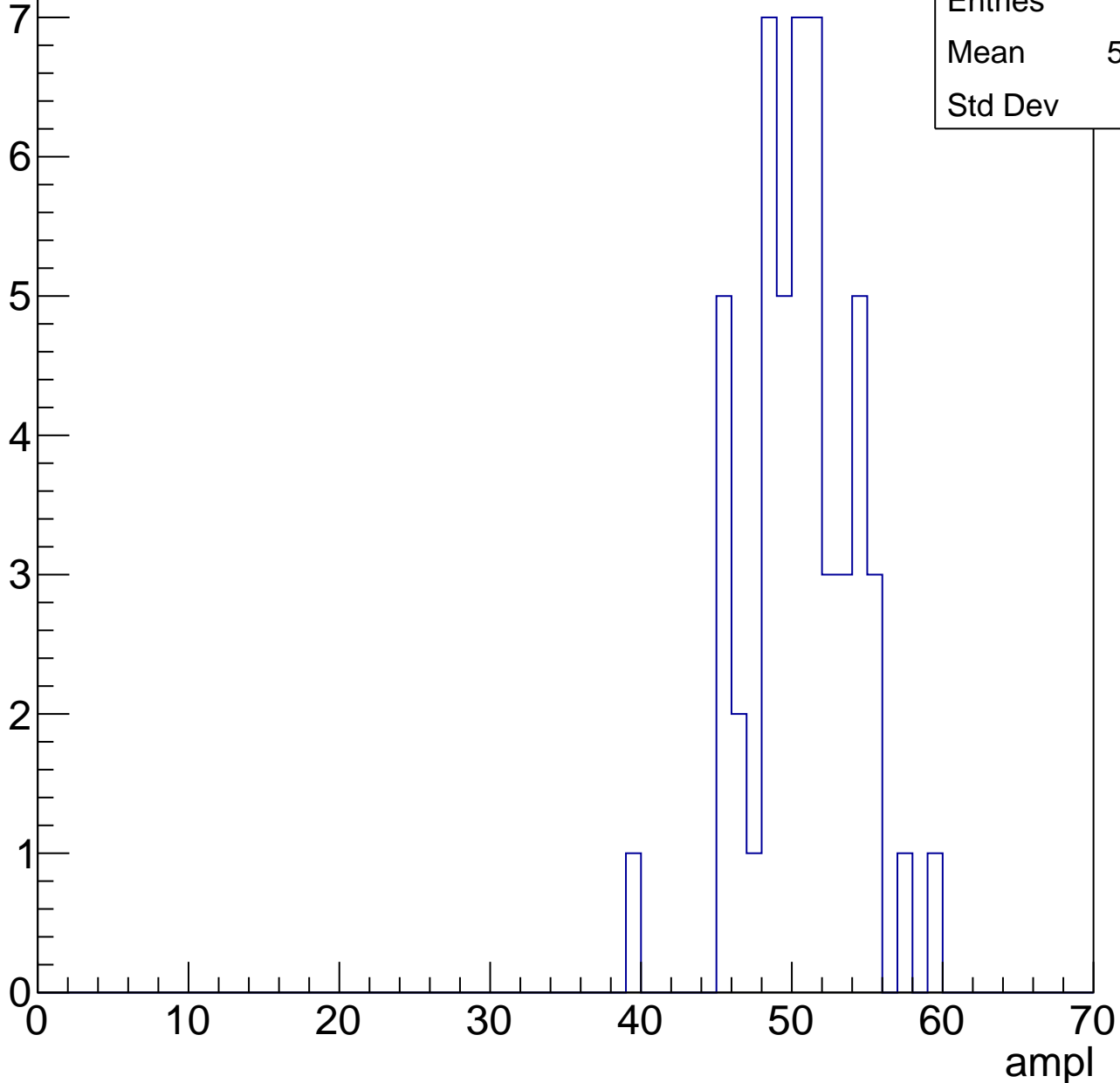


# B1L103S, U3-ch11, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

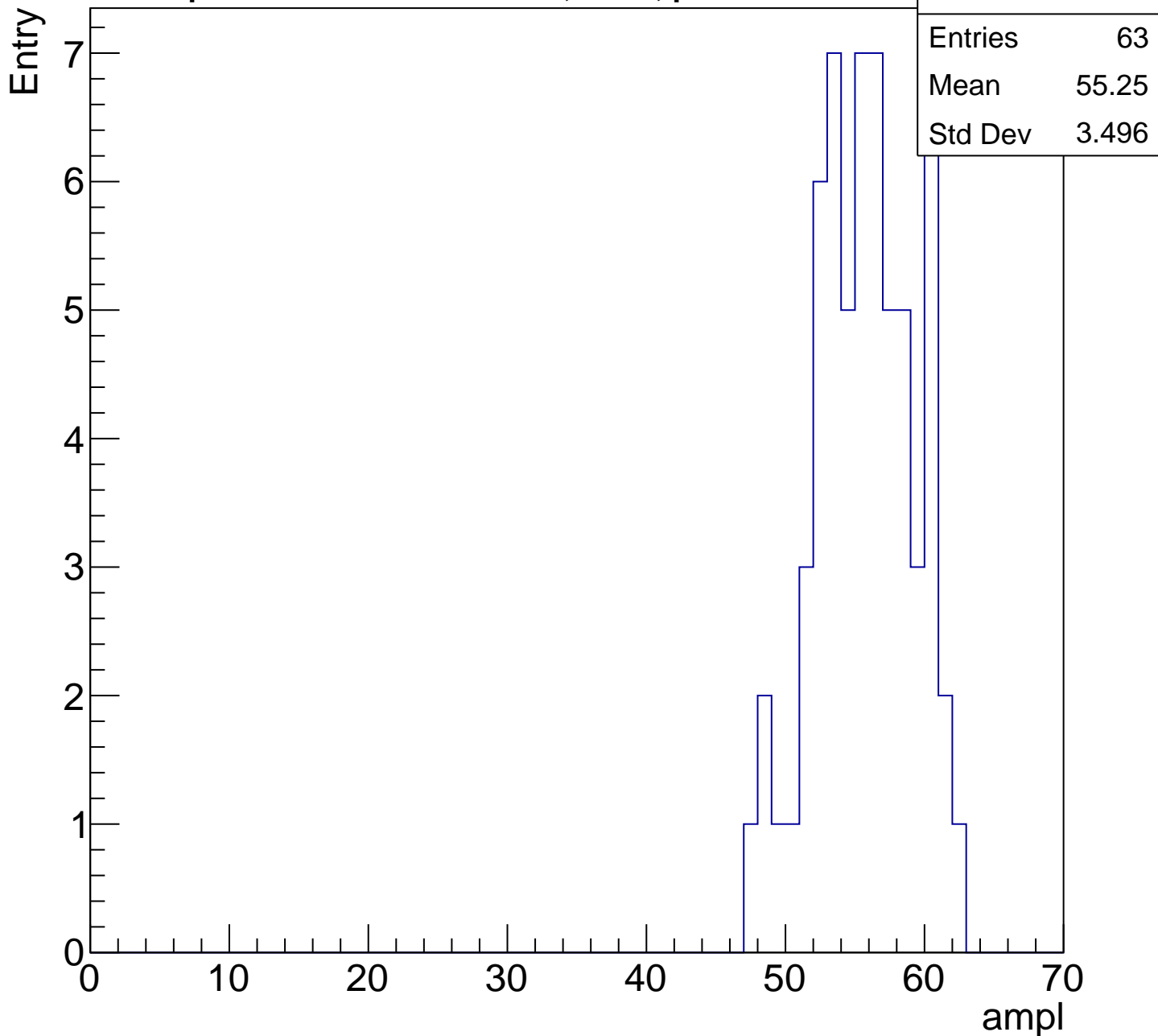
Entry

Entries	51
Mean	50.14
Std Dev	3.57



# B1L103S, U3-ch11, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

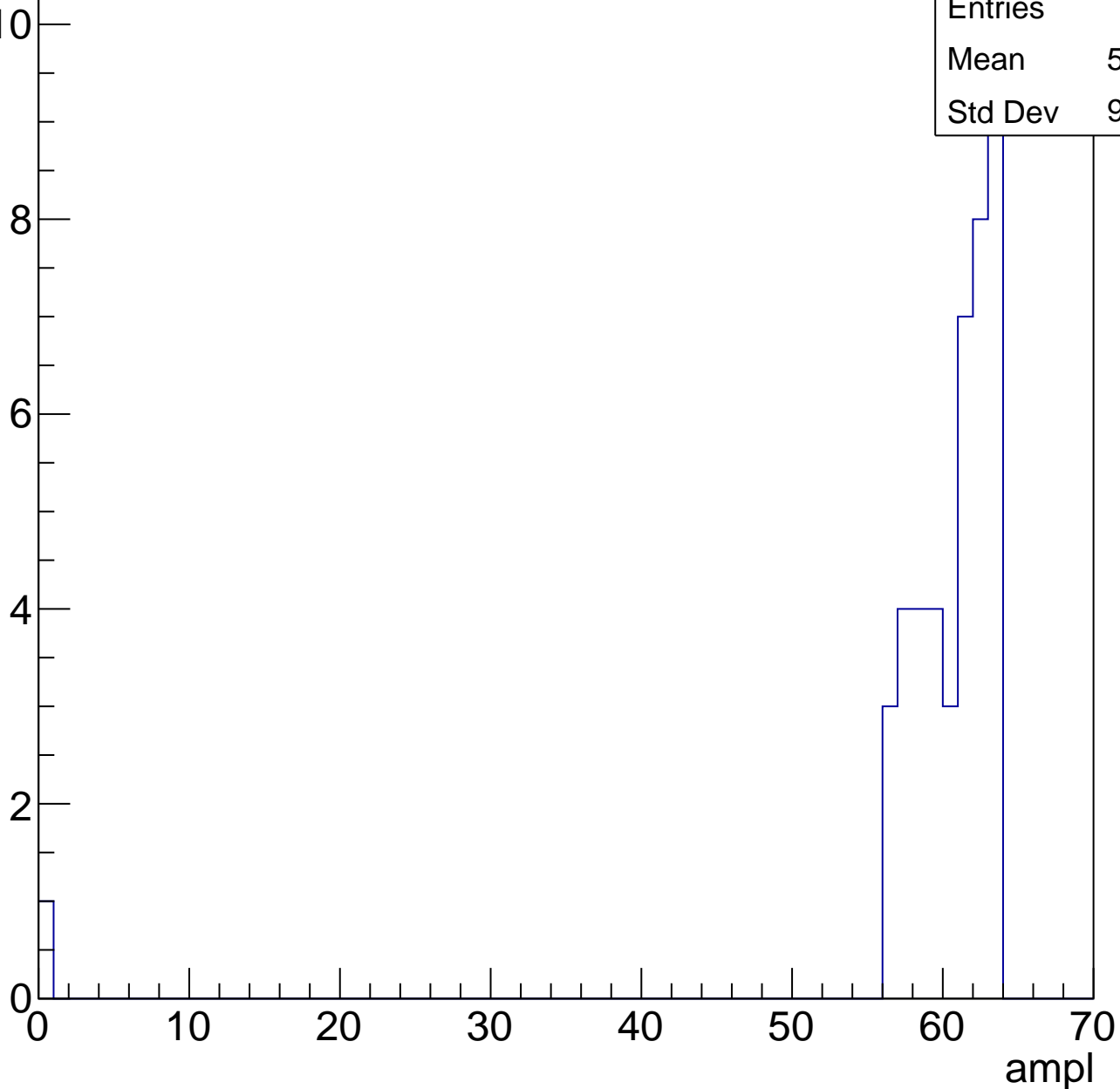


# B1L103S, U3-ch11, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	44
Mean	59.02
Std Dev	9.282



# B1L103S, U3-ch11, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

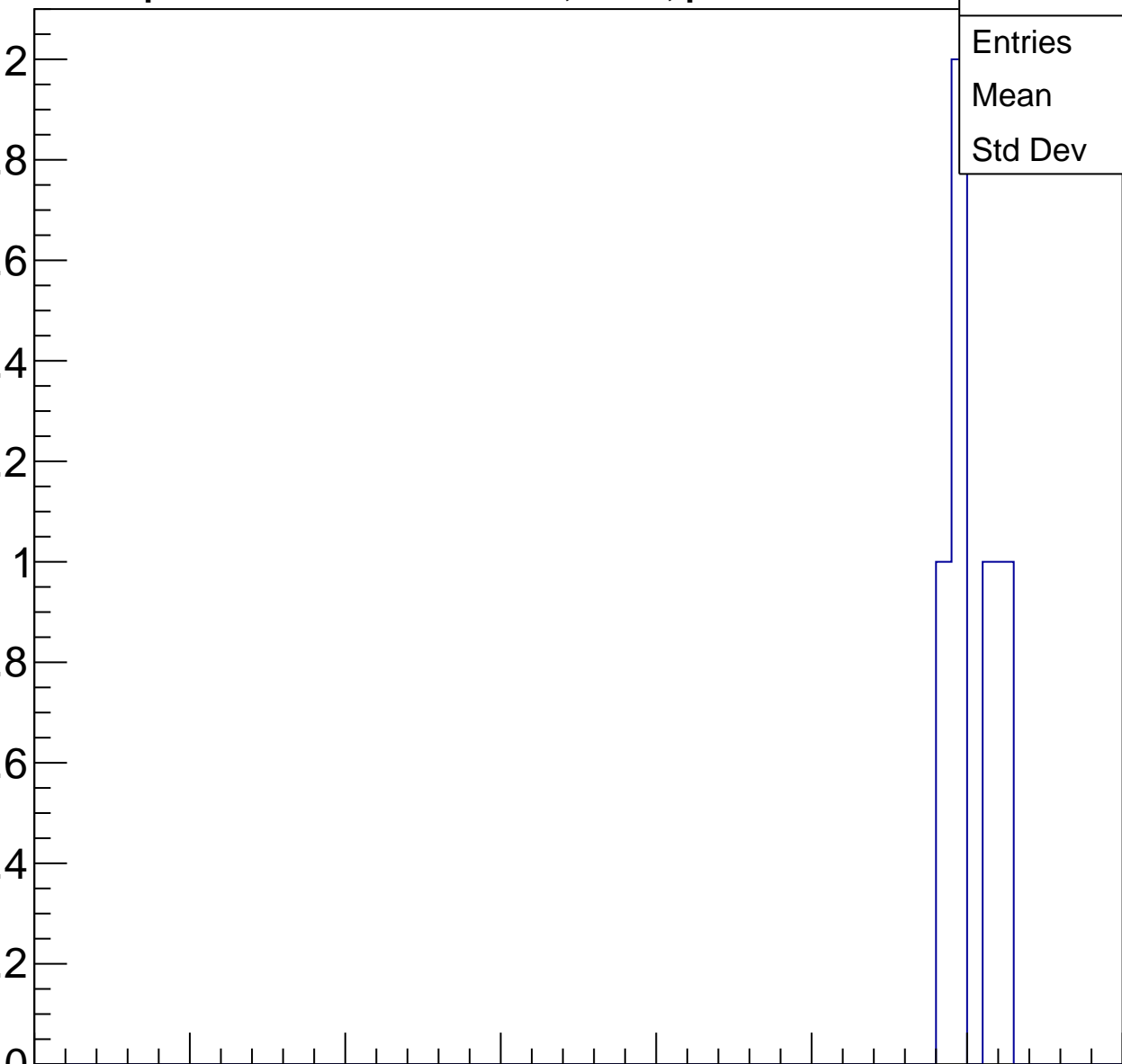
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	59.8
Std Dev	1.47

0 10 20 30 40 50 60 70

ampl





# B1L103S, U3-ch11, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U3-ch12, adc0

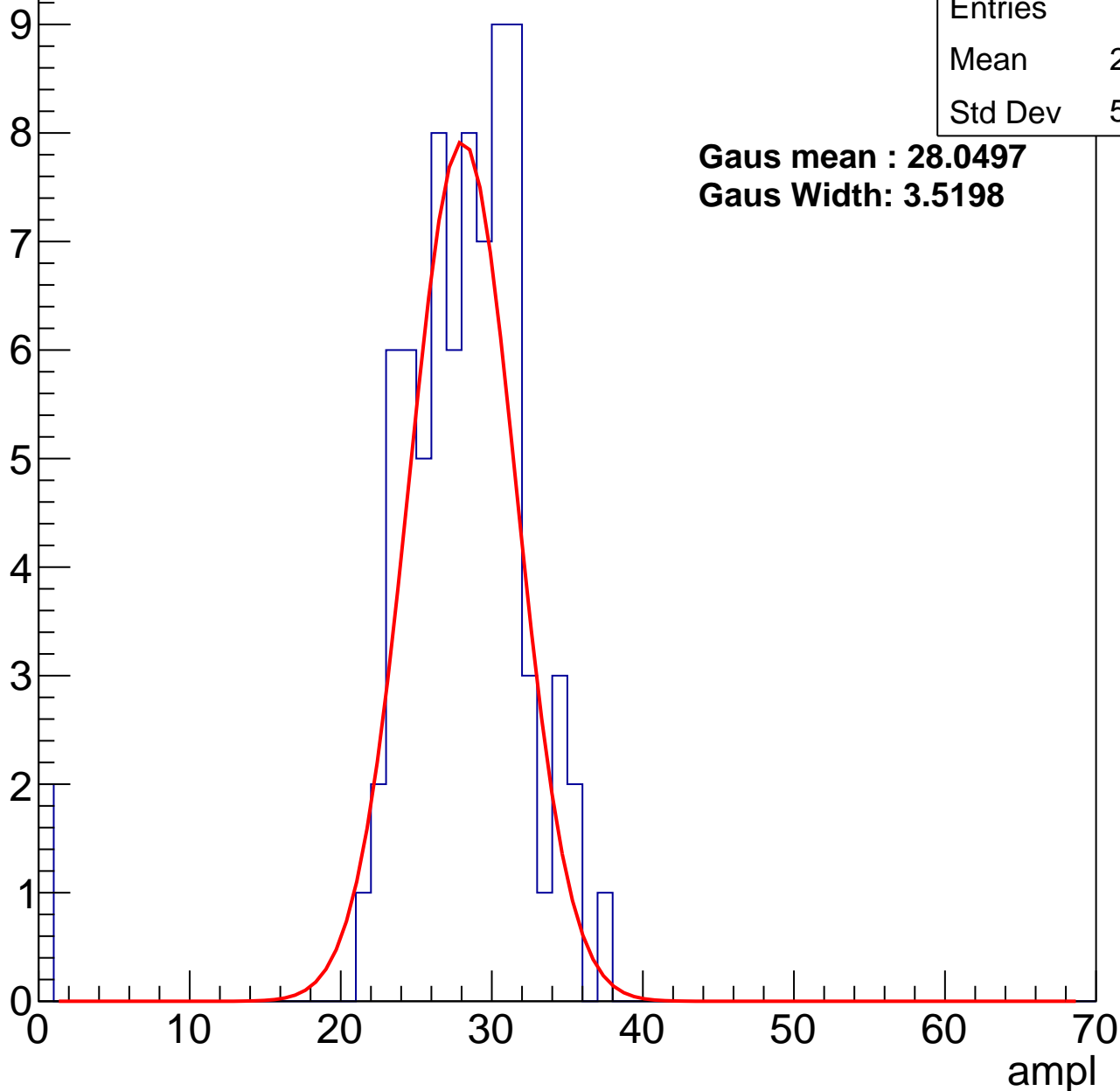
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	79
Mean	27.29
Std Dev	5.583

**Gaus mean : 28.0497**

**Gaus Width: 3.5198**



# B1L103S, U3-ch12, adc1

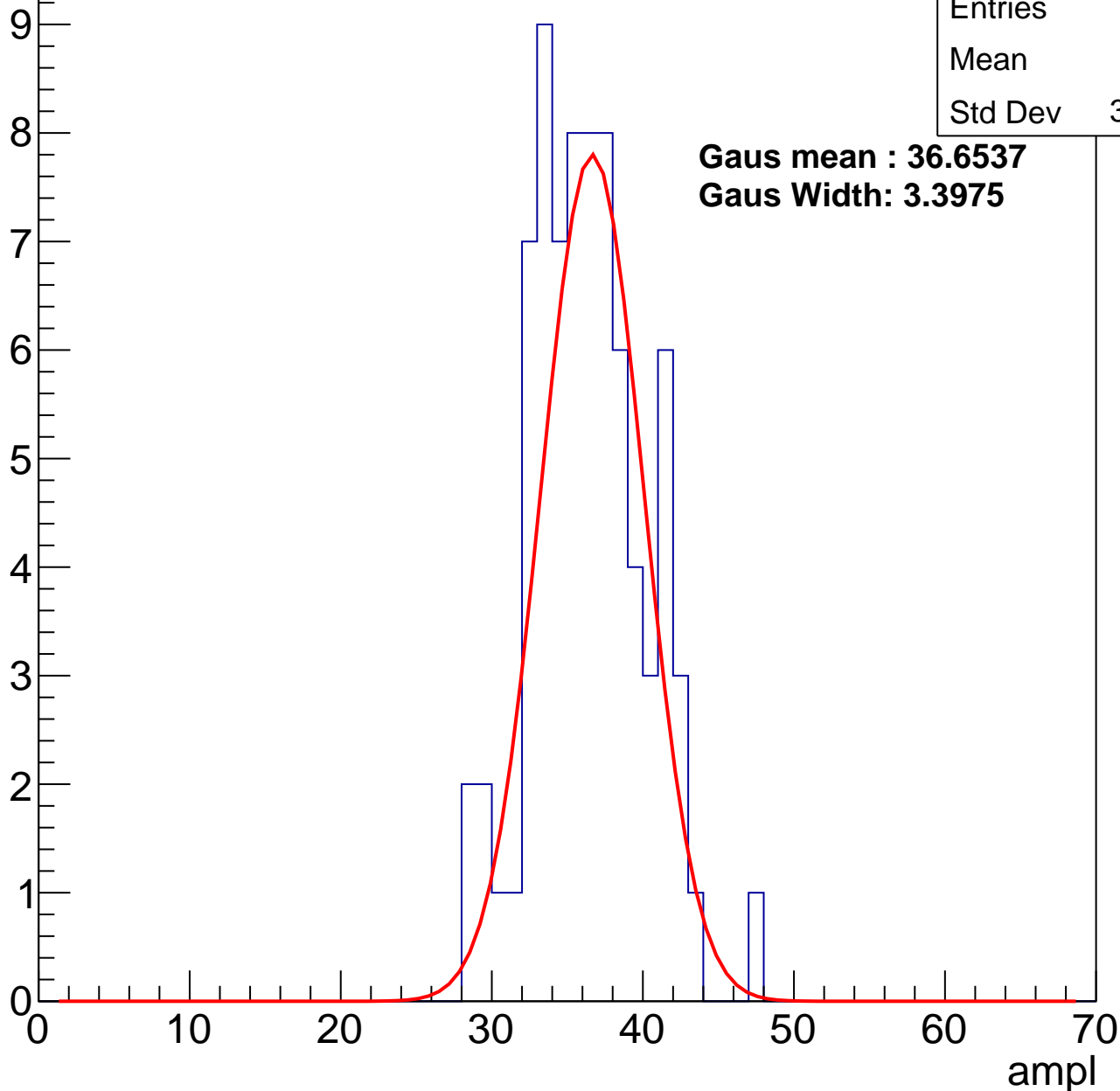
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	35.9
Std Dev	3.709

**Gaus mean : 36.6537**

**Gaus Width: 3.3975**



# B1L103S, U3-ch12, adc2

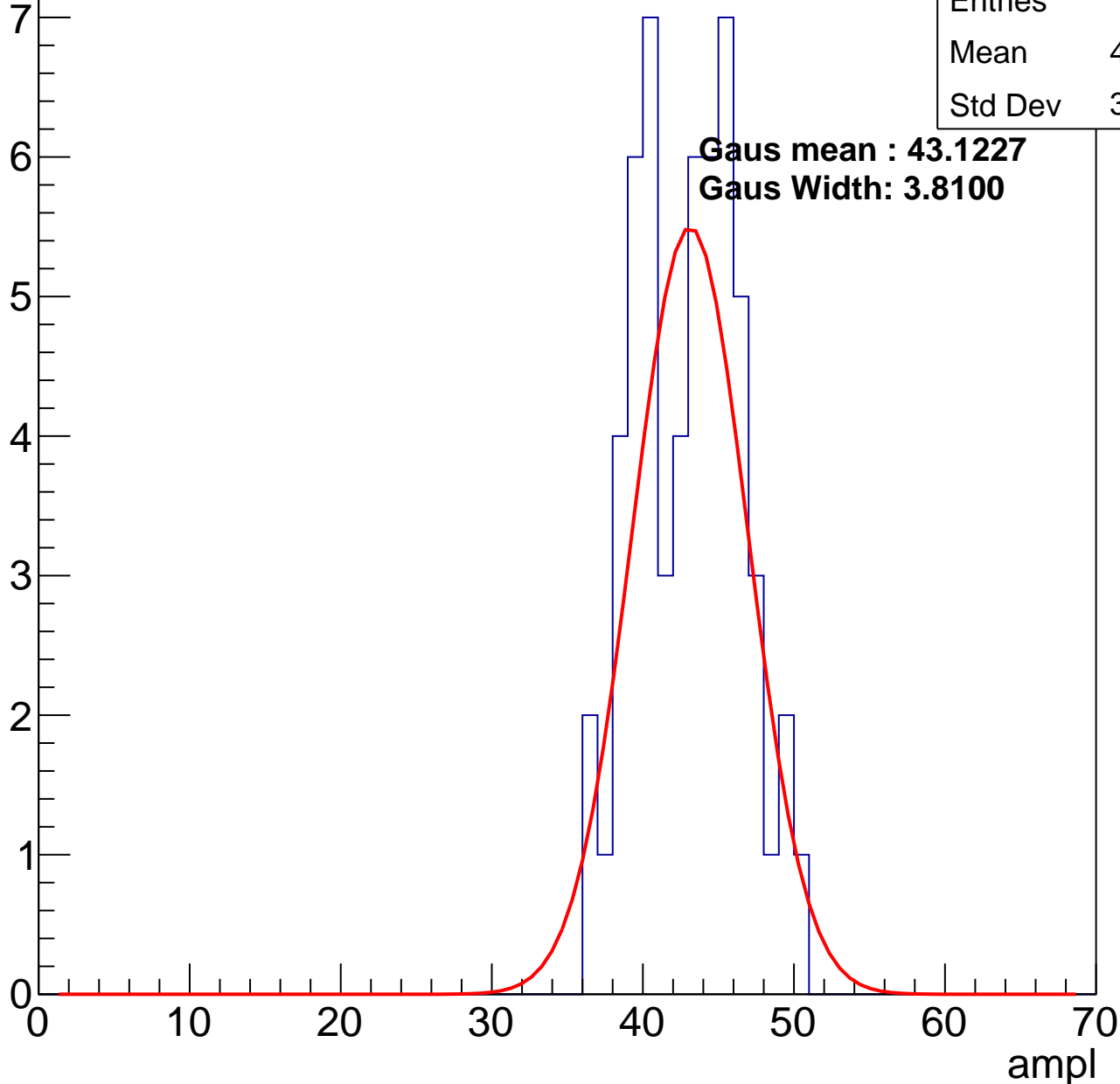
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	42.59
Std Dev	3.404

**Gaus mean : 43.1227**

**Gaus Width: 3.8100**

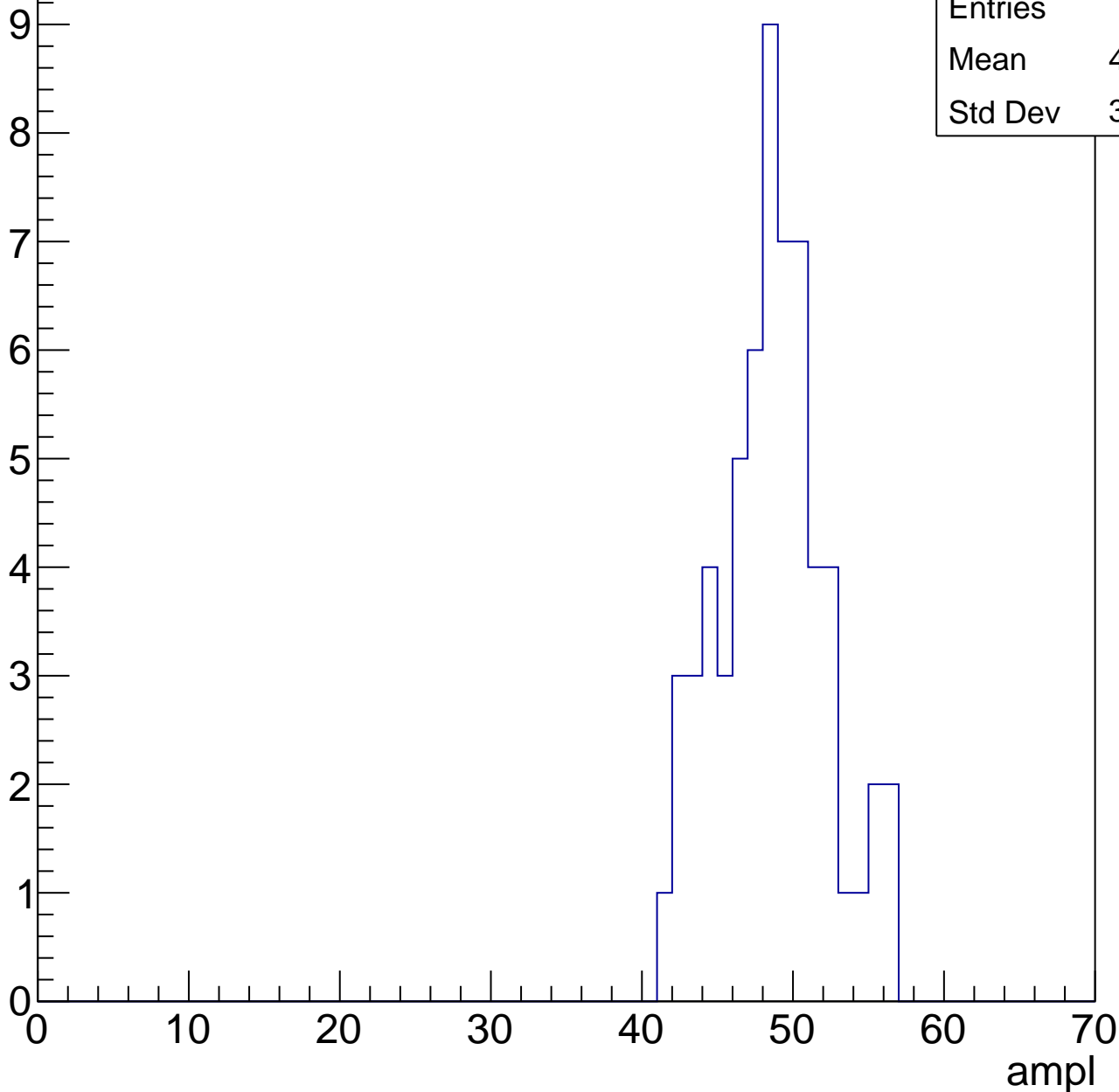


# B1L103S, U3-ch12, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

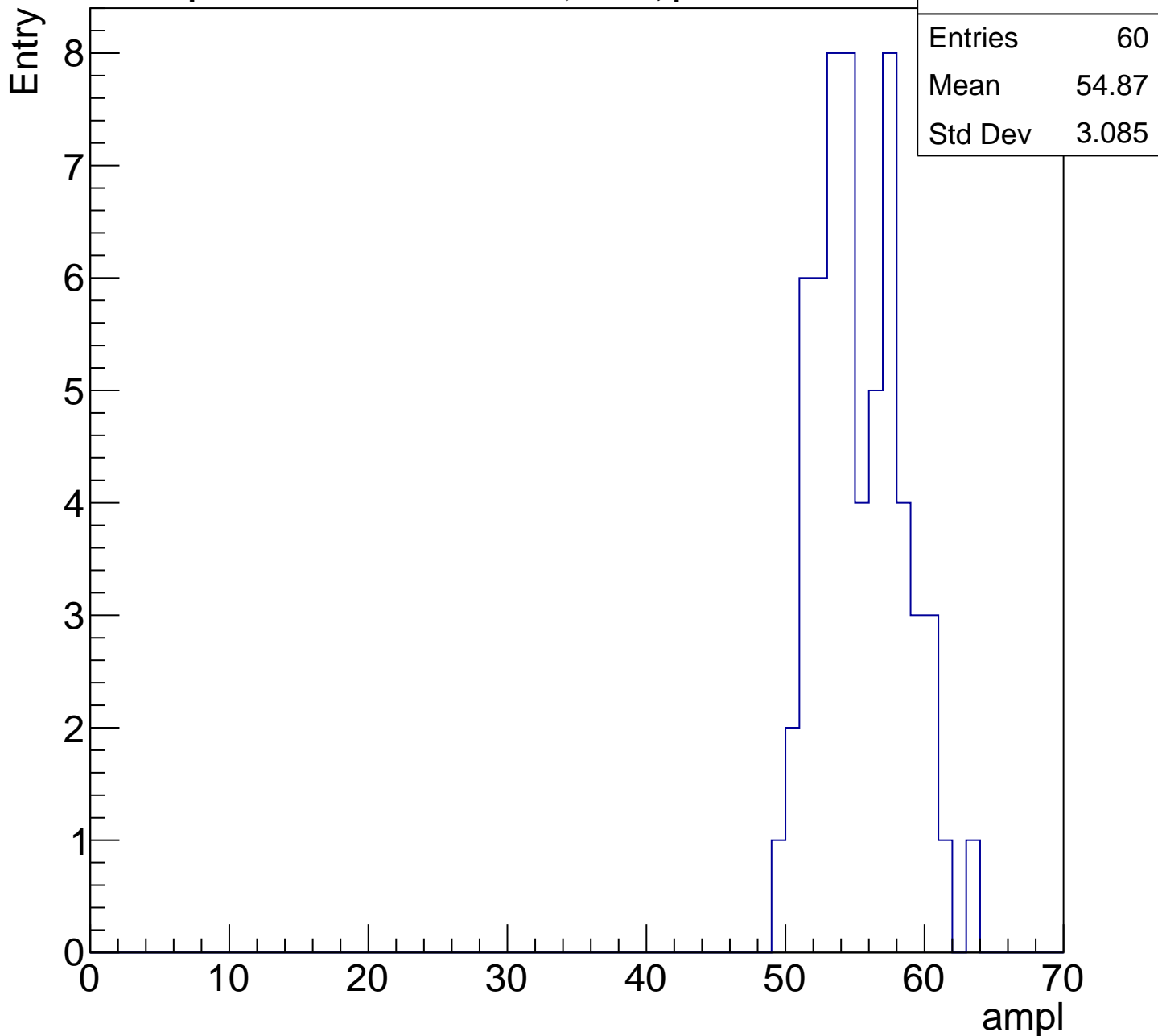
Entry

Entries	62
Mean	48.15
Std Dev	3.523



# B1L103S, U3-ch12, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

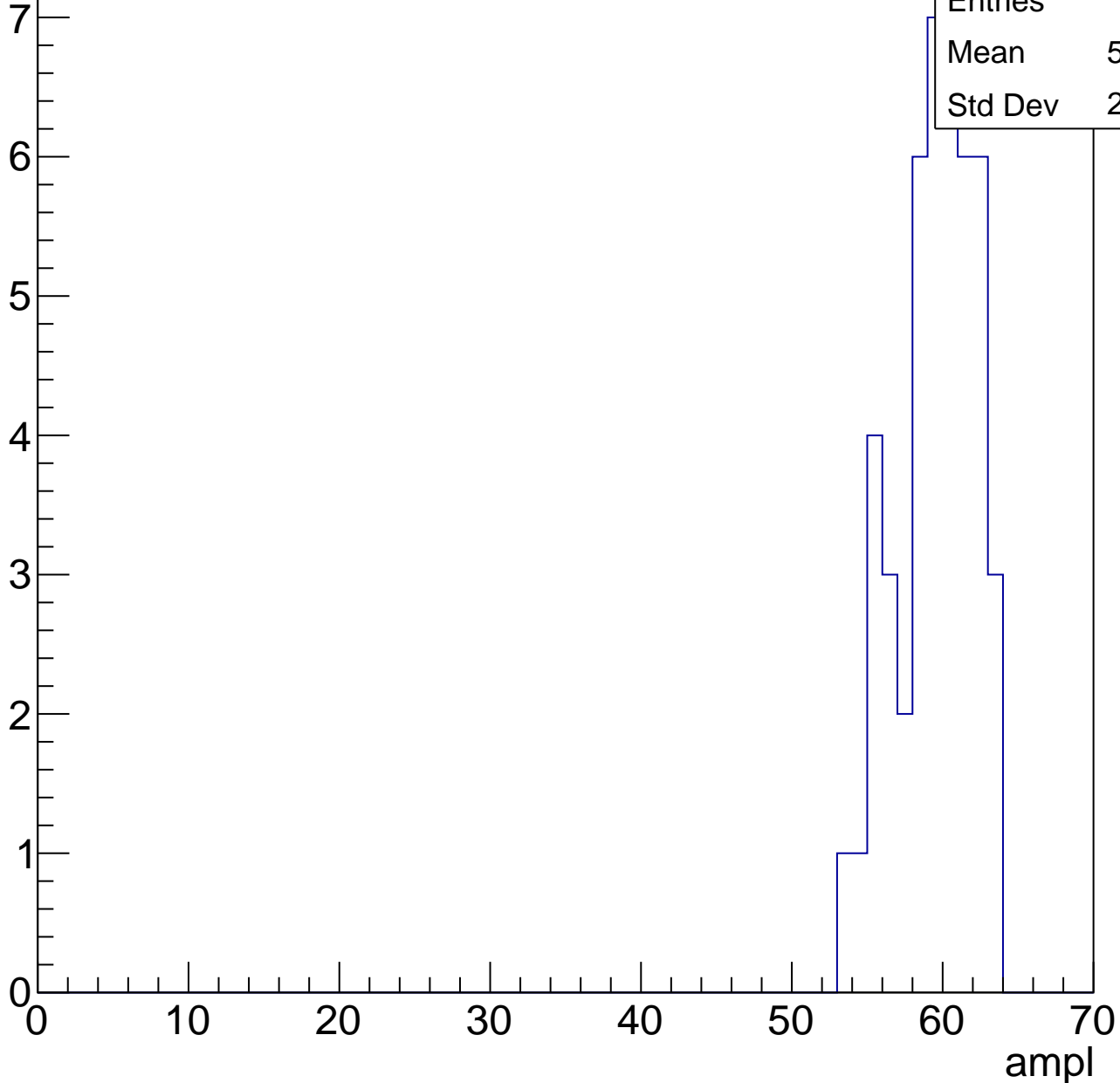


# B1L103S, U3-ch12, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	46
Mean	59.07
Std Dev	2.549

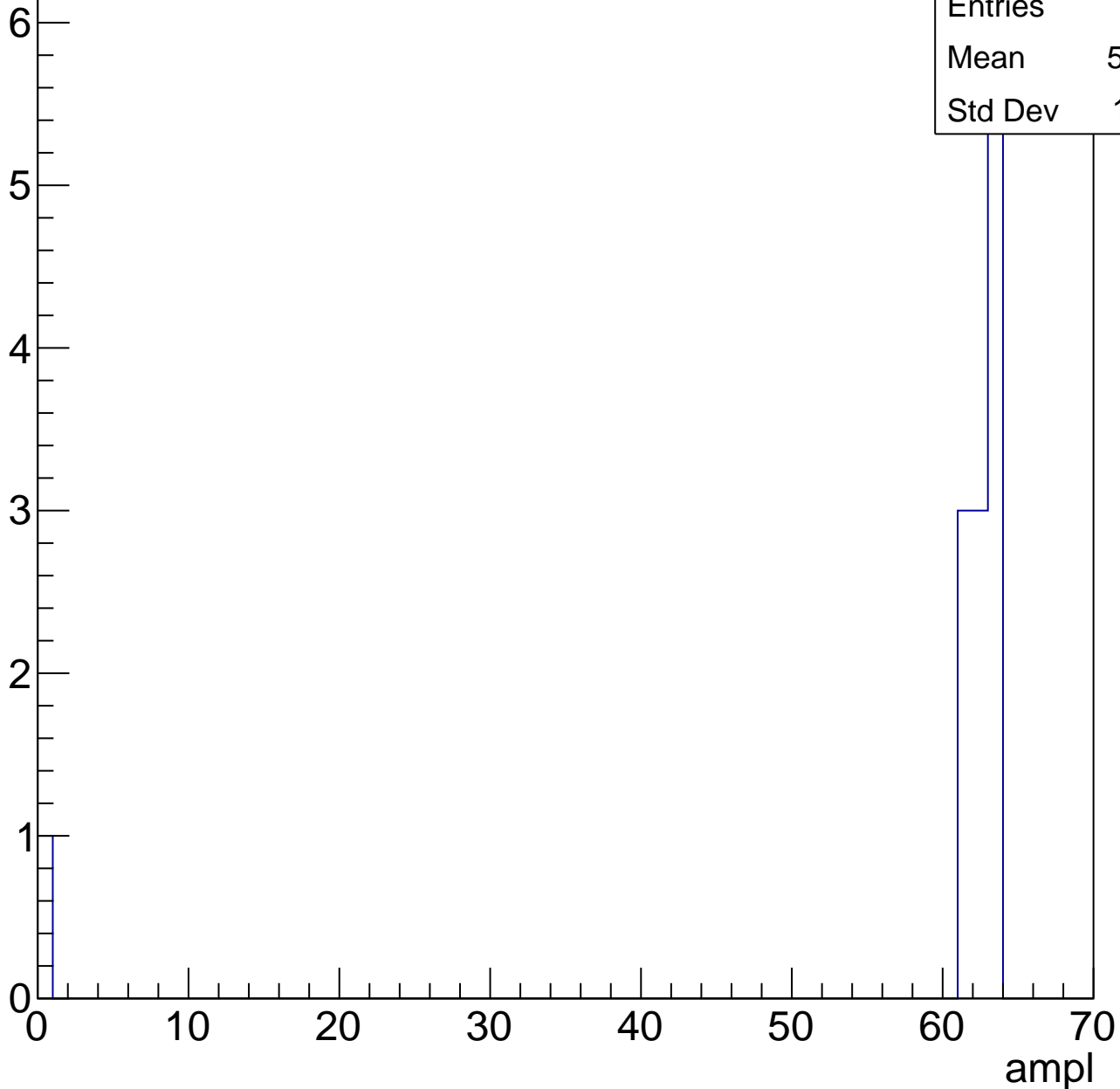


# B1L103S, U3-ch12, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	13
Mean	57.46
Std Dev	16.61





# B1L103S, U3-ch12, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch13, adc0

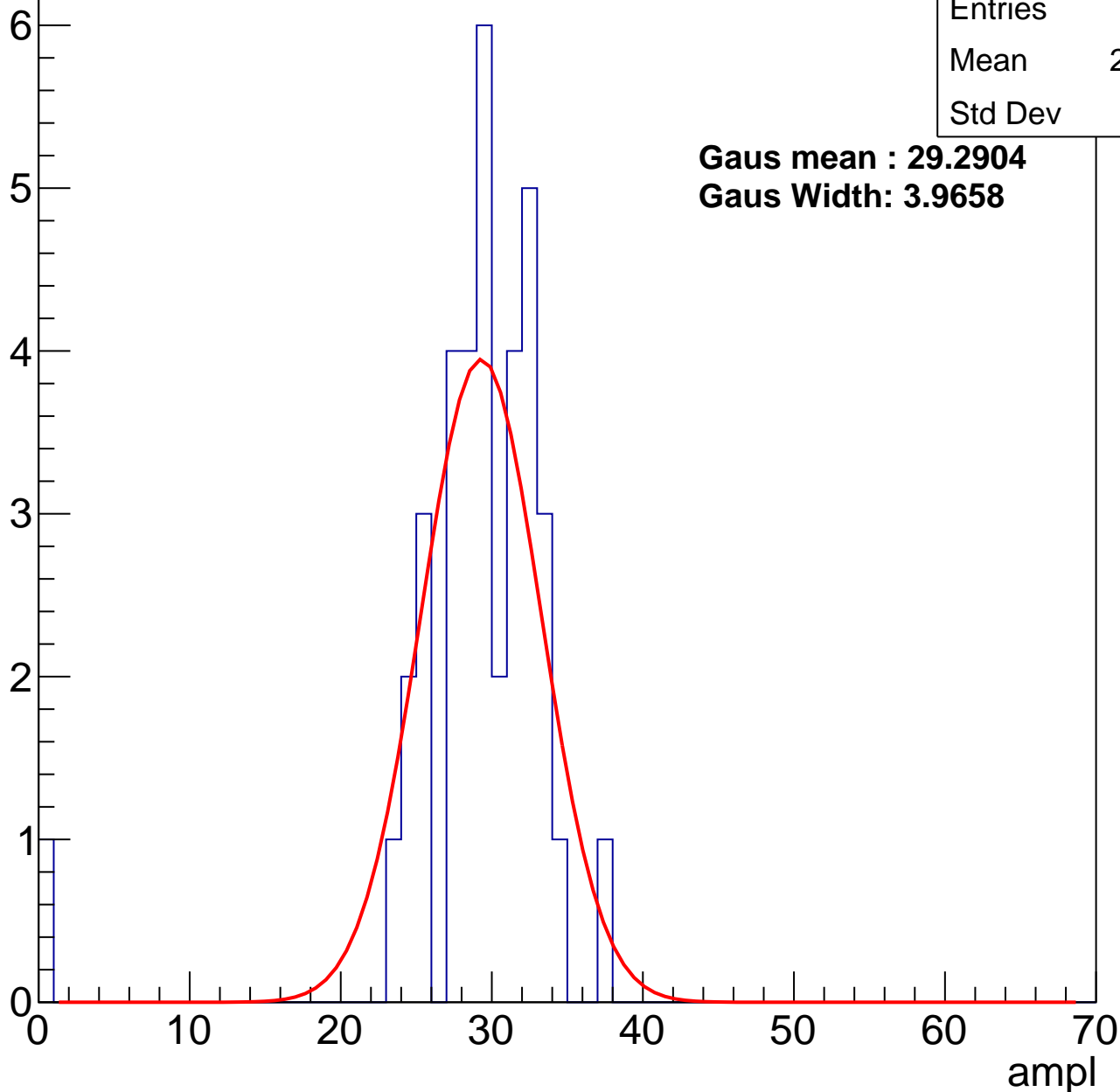
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	37
Mean	28.49
Std Dev	5.66

**Gaus mean : 29.2904**

**Gaus Width: 3.9658**



# B1L103S, U3-ch13, adc1

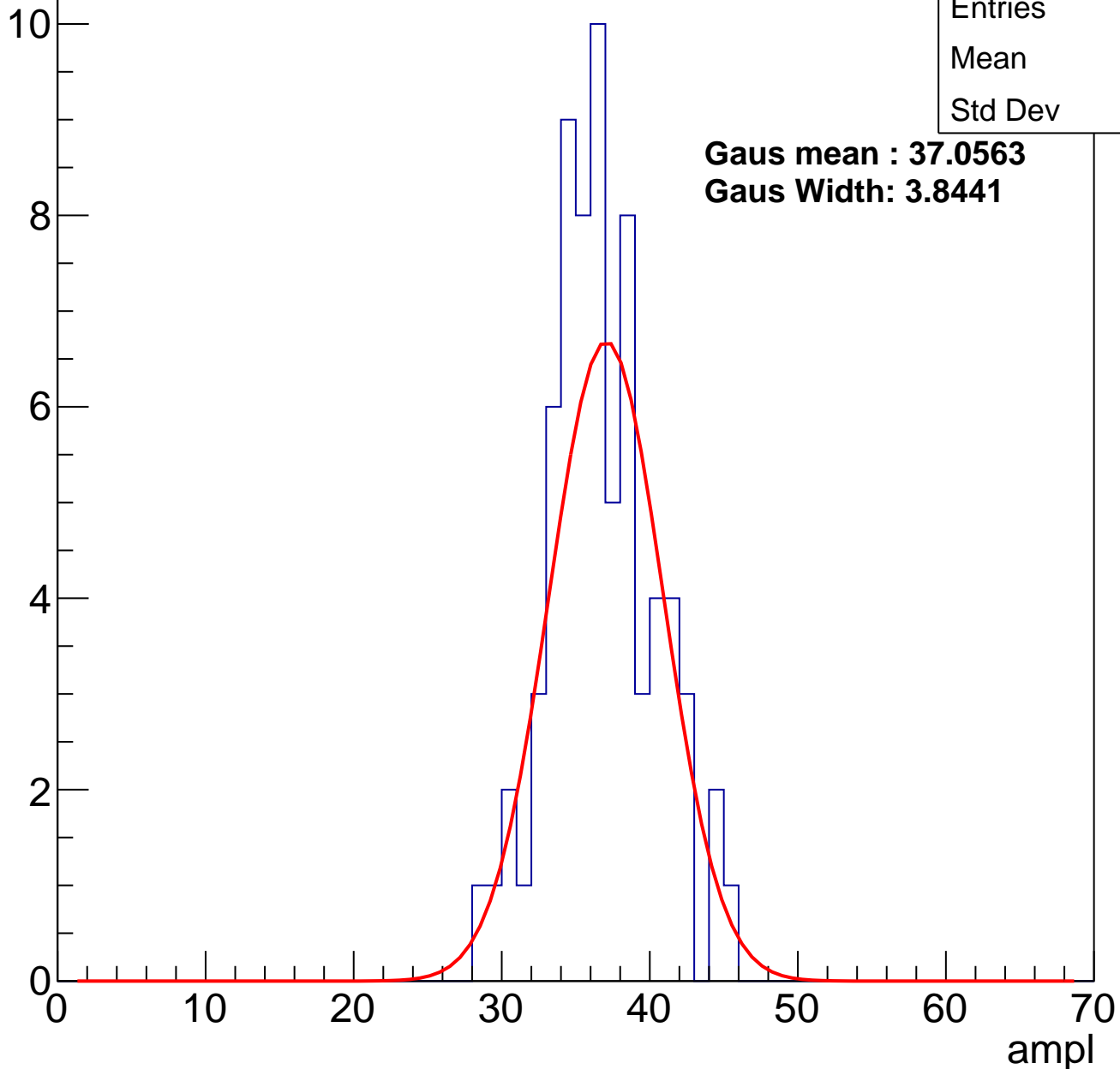
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	71
Mean	36.3
Std Dev	3.55

**Gaus mean : 37.0563**

**Gaus Width: 3.8441**

Entry



# B1L103S, U3-ch13, adc2

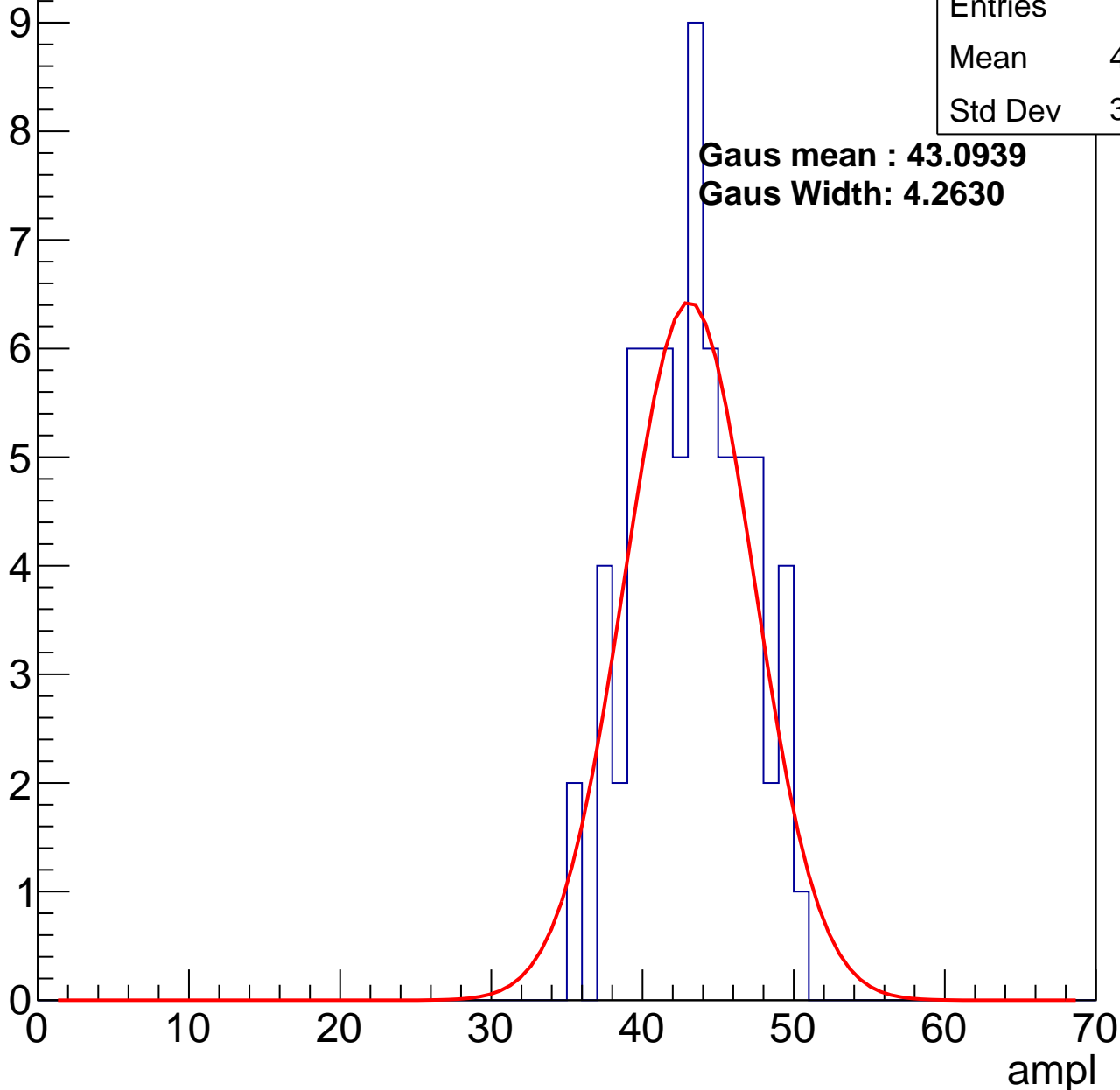
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	42.75
Std Dev	3.619

**Gaus mean : 43.0939**

**Gaus Width: 4.2630**

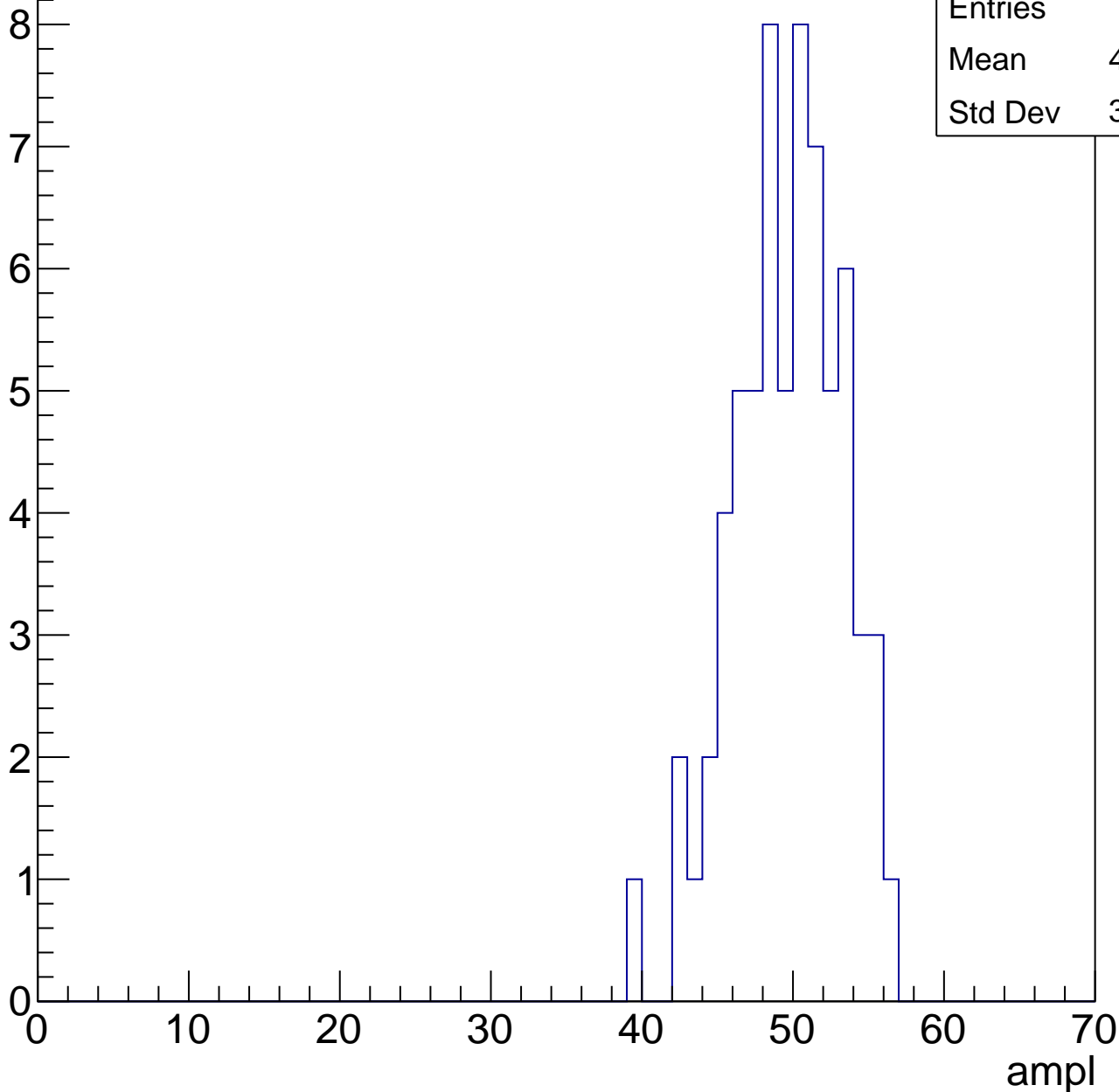


# B1L103S, U3-ch13, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	49.18
Std Dev	3.542

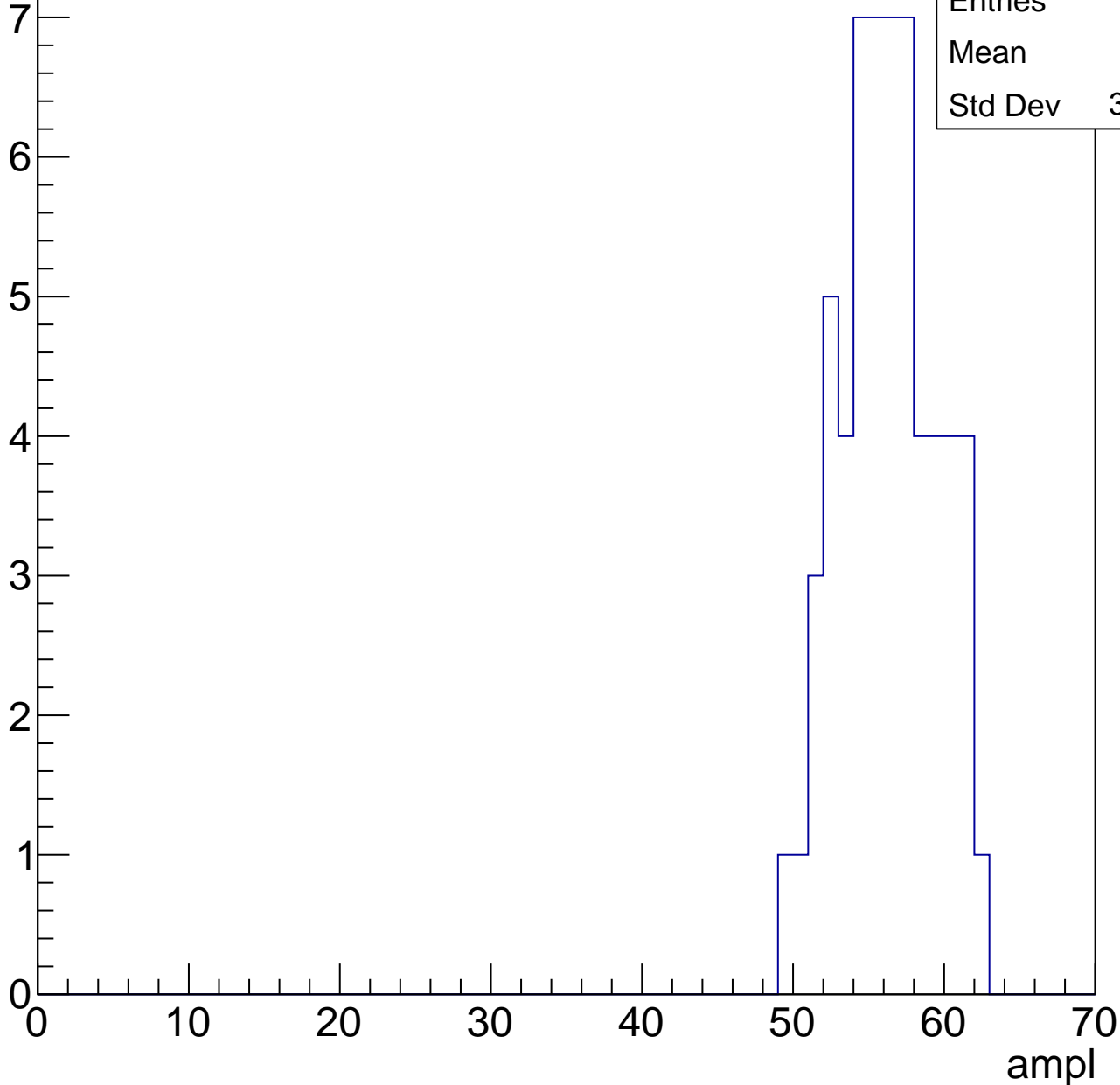


# B1L103S, U3-ch13, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	55.8
Std Dev	3.102

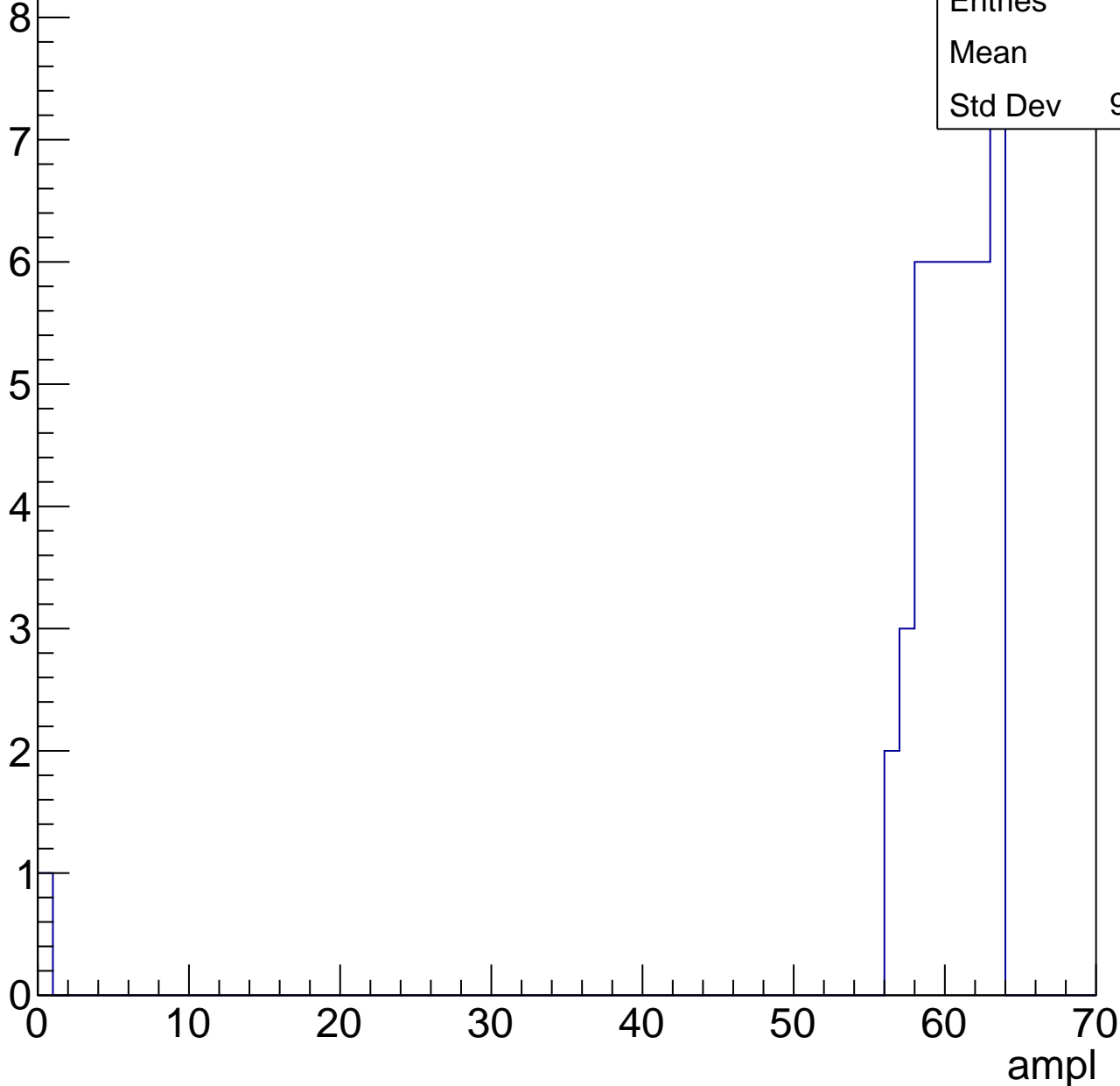


# B1L103S, U3-ch13, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

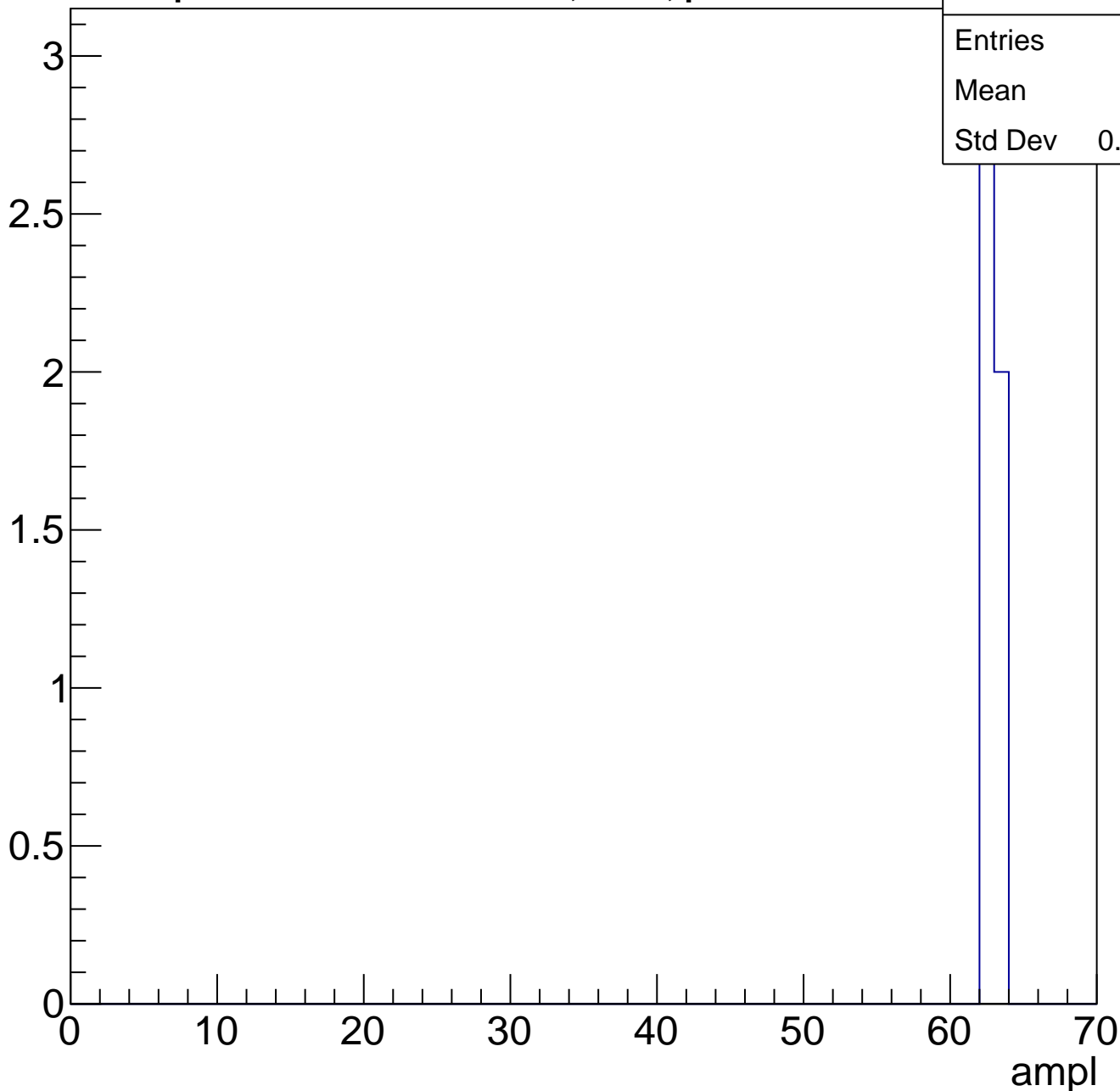
Entries	44
Mean	58.8
Std Dev	9.204



# B1L103S, U3-ch13, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U3-ch13, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U3-ch14, adc0

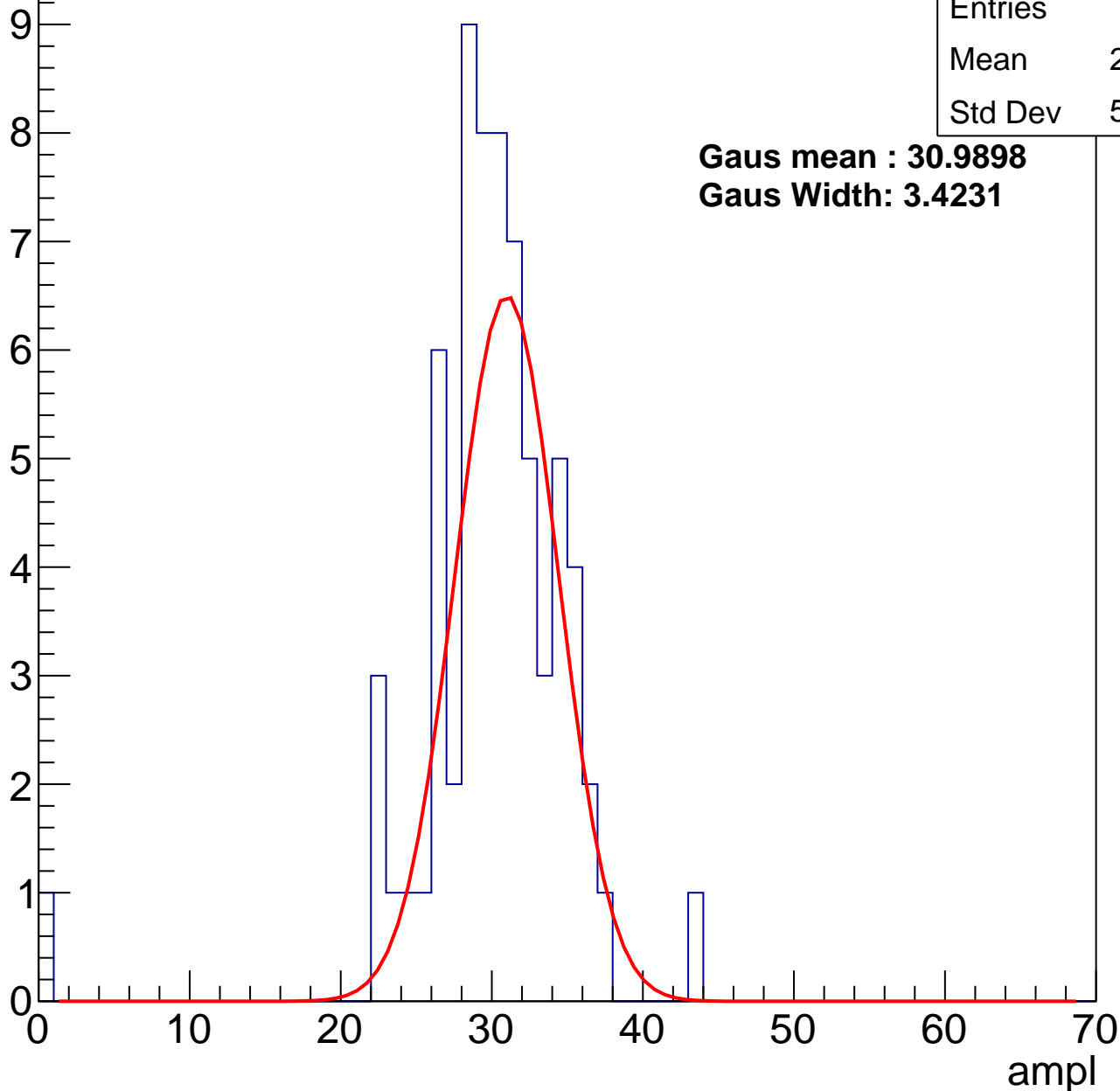
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	29.56
Std Dev	5.245

**Gaus mean : 30.9898**

**Gaus Width: 3.4231**



# B1L103S, U3-ch14, adc1

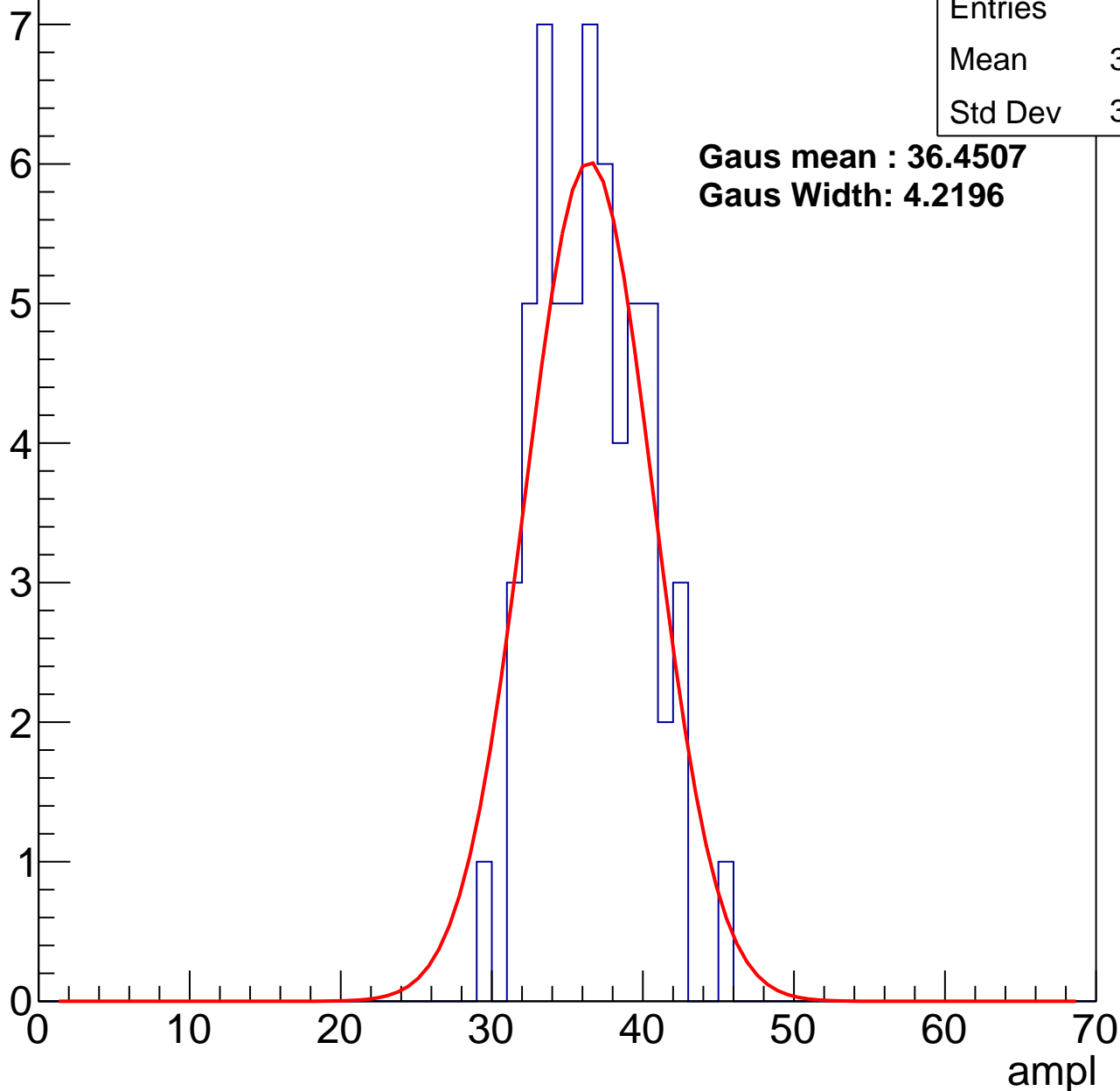
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	36.14
Std Dev	3.387

**Gaus mean : 36.4507**

**Gaus Width: 4.2196**



# B1L103S, U3-ch14, adc2

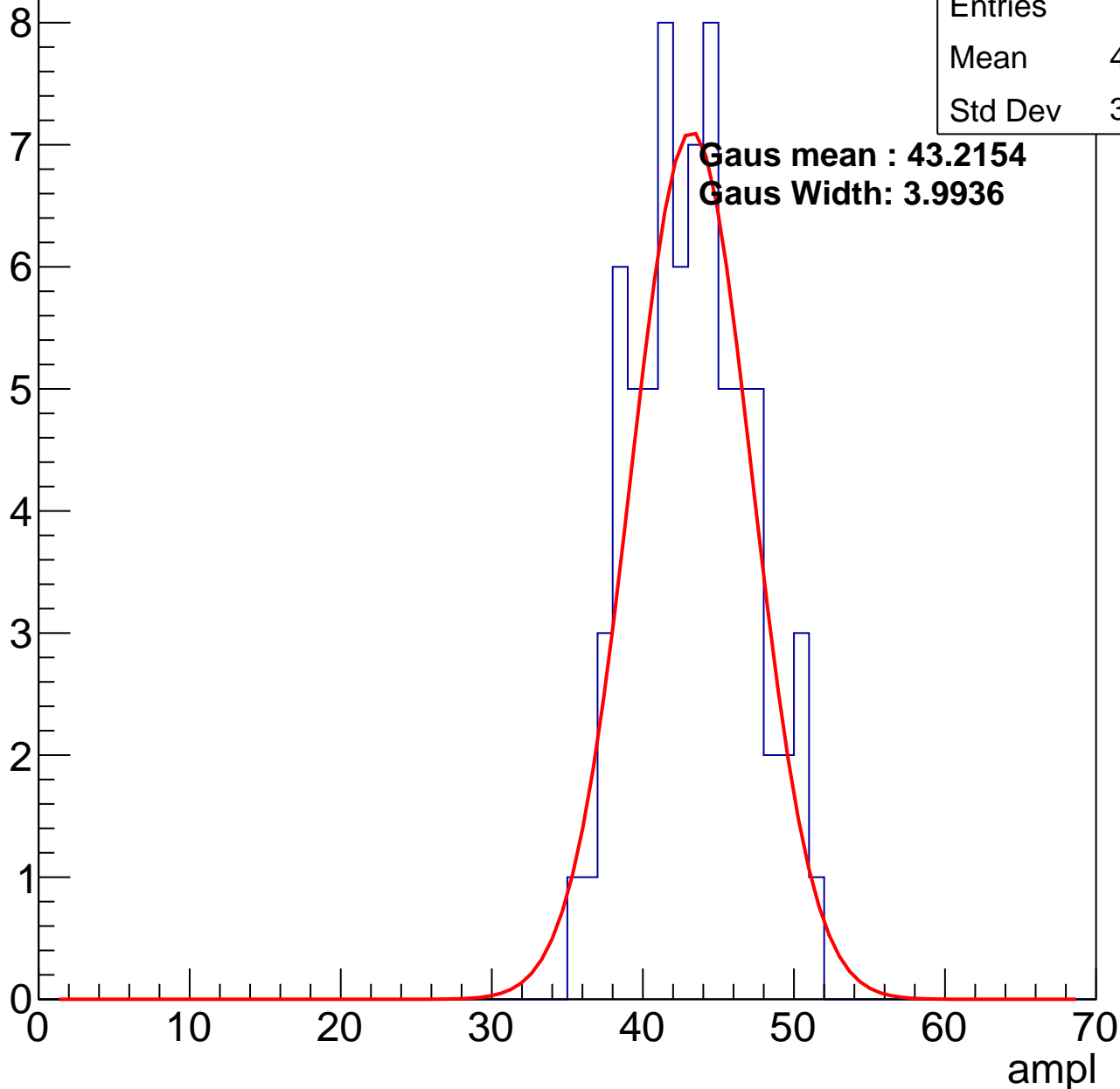
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	42.78
Std Dev	3.732

**Gaus mean : 43.2154**

**Gaus Width: 3.9936**

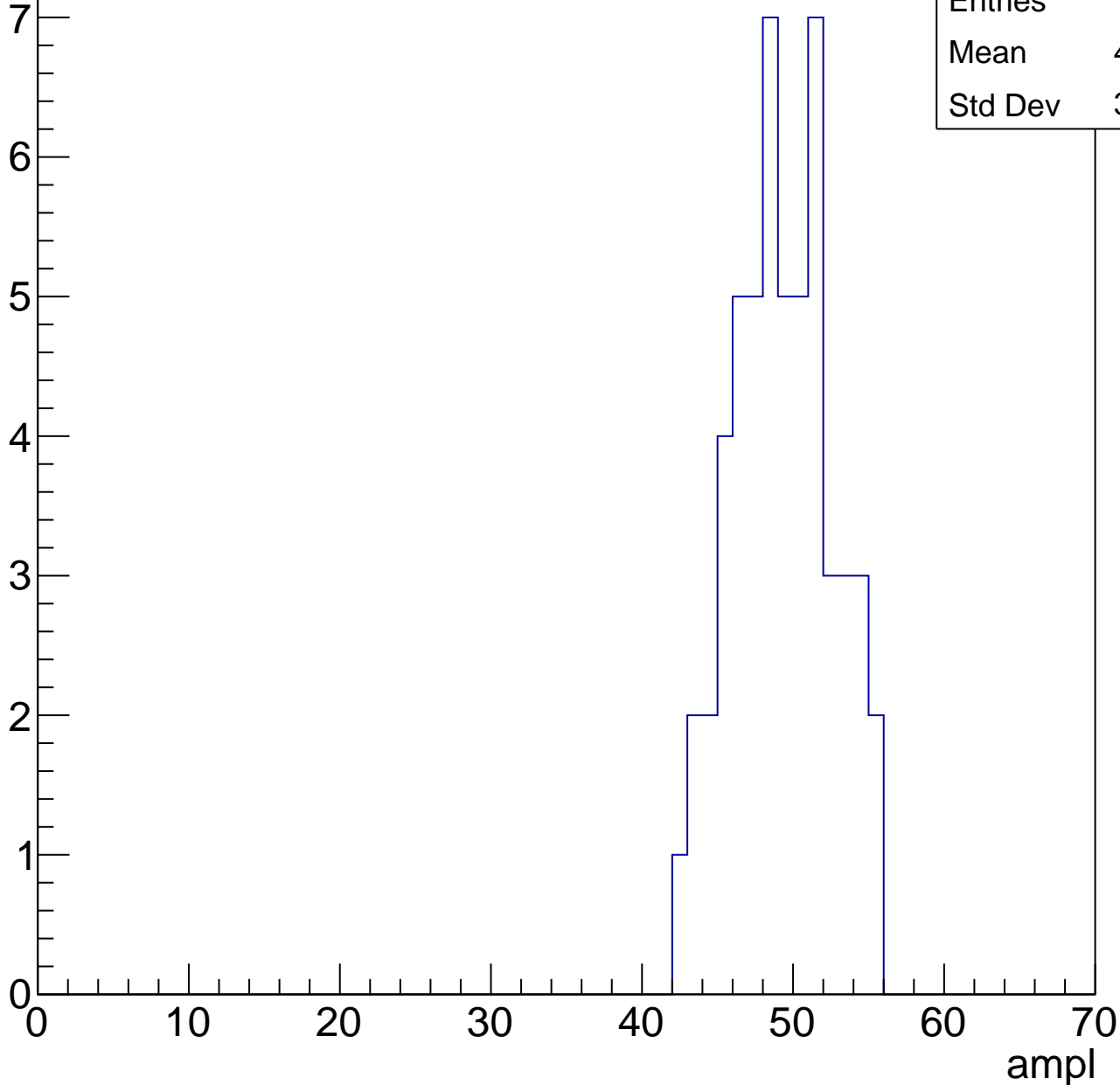


# B1L103S, U3-ch14, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	48.81
Std Dev	3.221

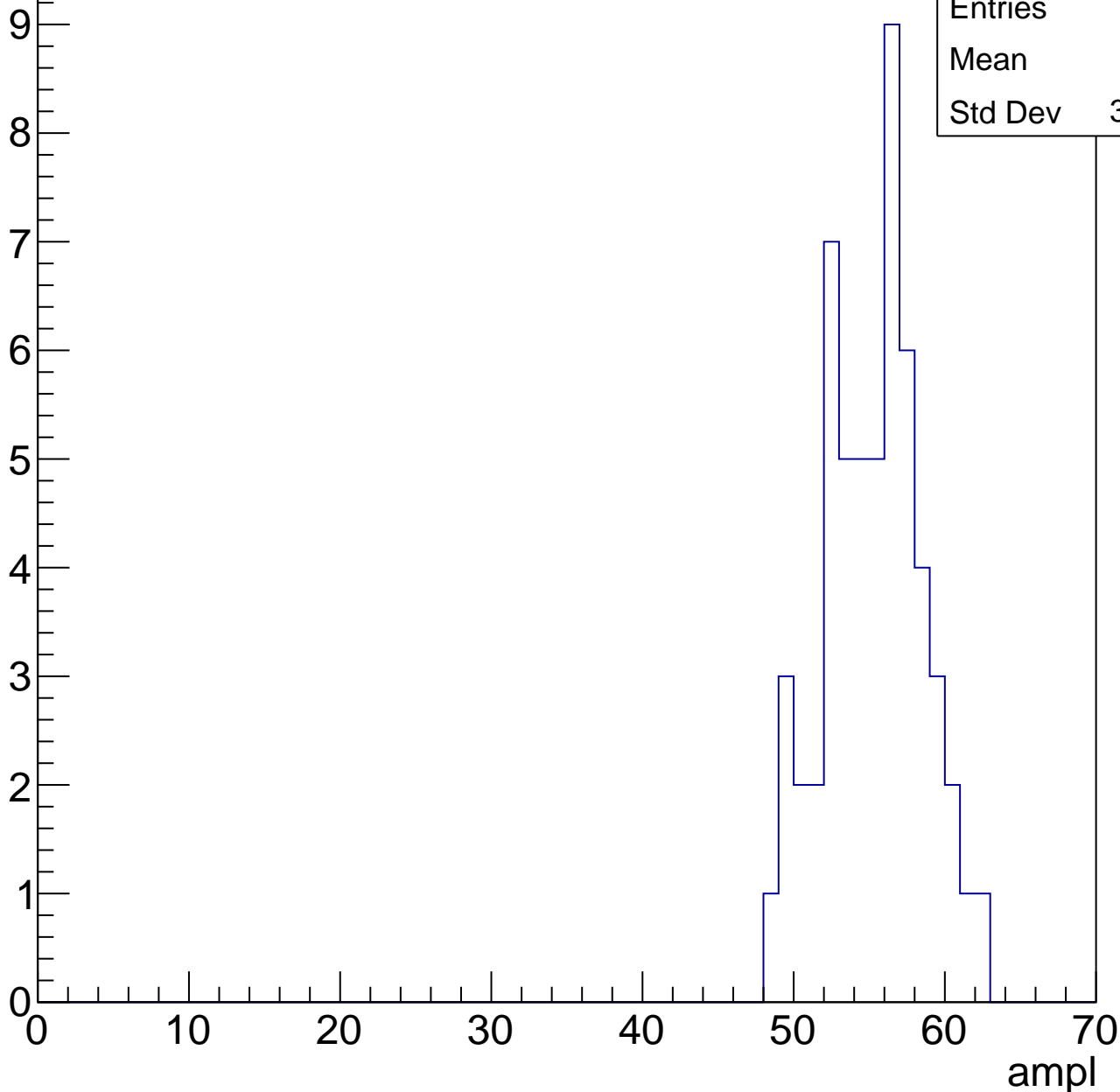


# B1L103S, U3-ch14, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	54.8
Std Dev	3.209

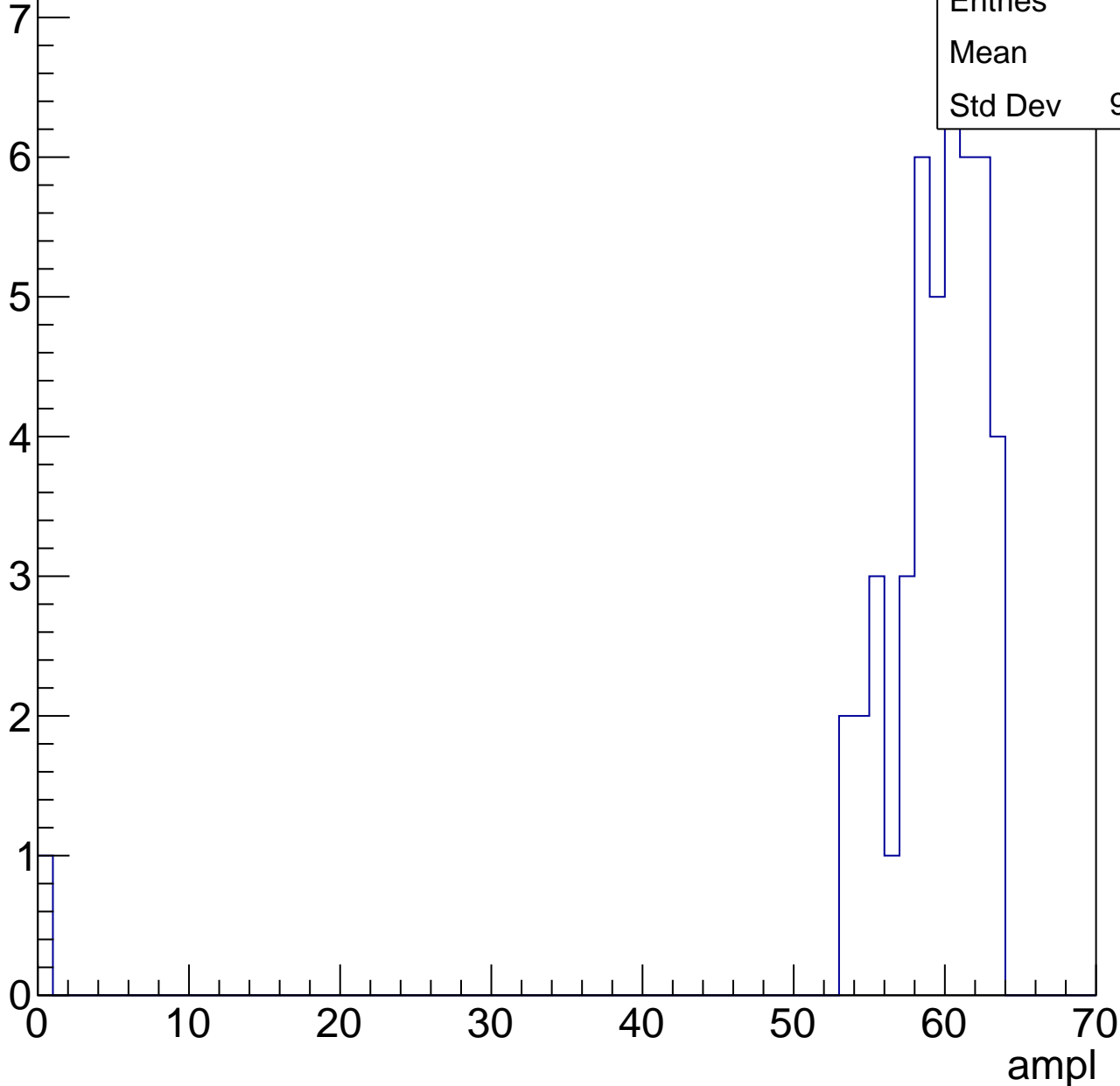


# B1L103S, U3-ch14, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	46
Mean	57.8
Std Dev	9.042

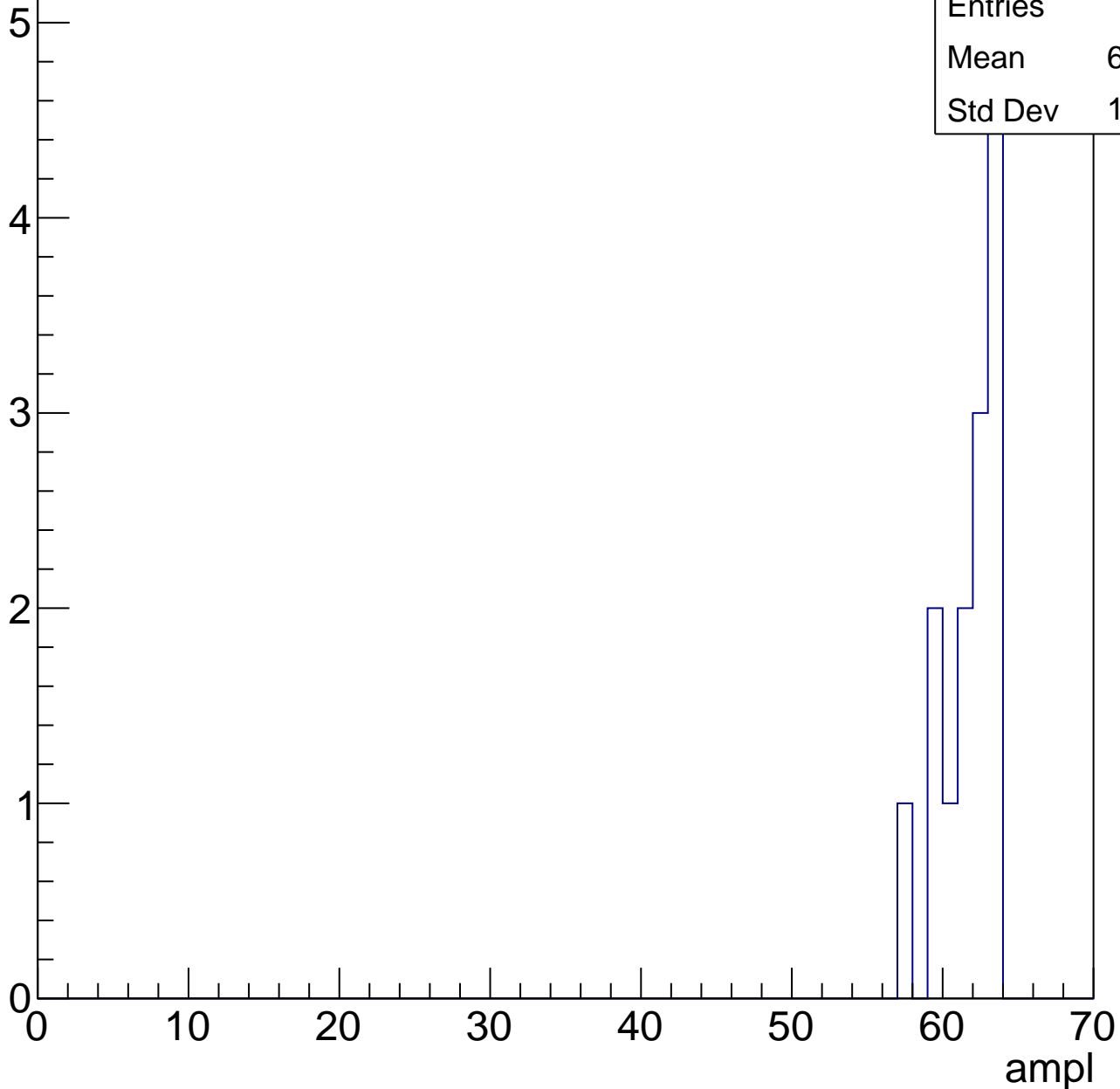


# B1L103S, U3-ch14, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	14
Mean	61.29
Std Dev	1.829

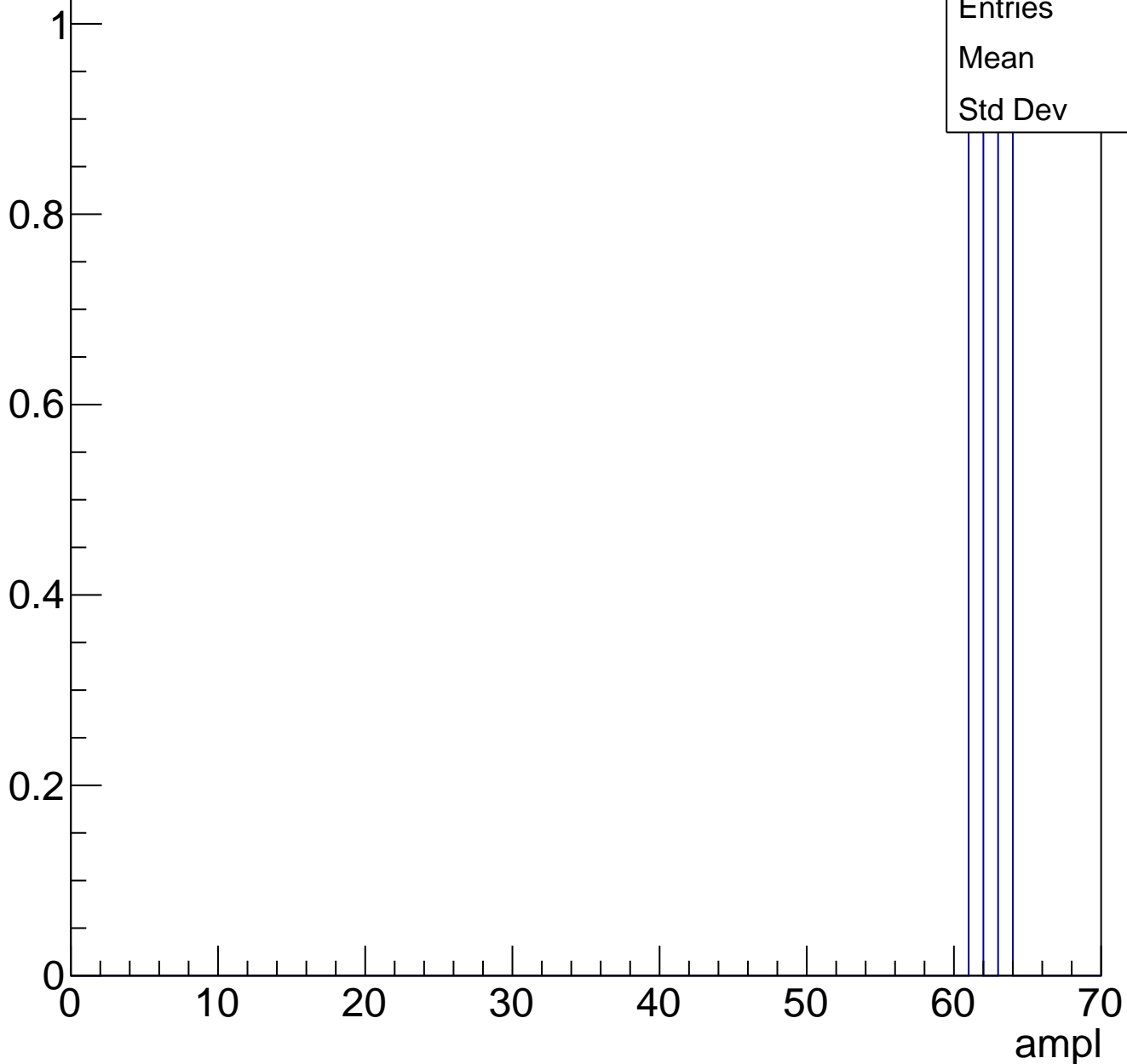




# B1L103S, U3-ch14, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



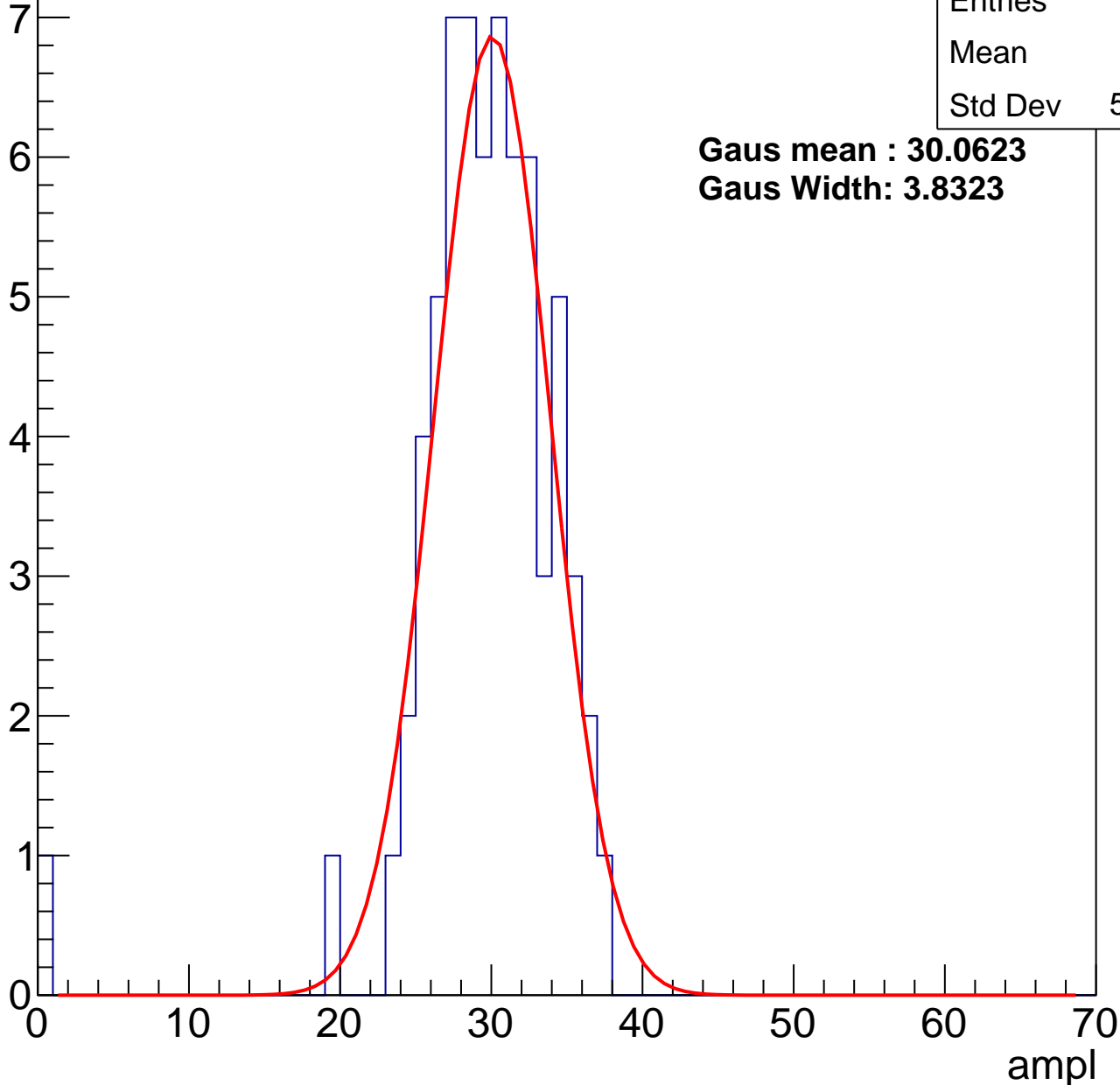
# B1L103S, U3-ch15, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	29.1
Std Dev	5.035

**Gaus mean : 30.0623**  
**Gaus Width: 3.8323**



# B1L103S, U3-ch15, adc1

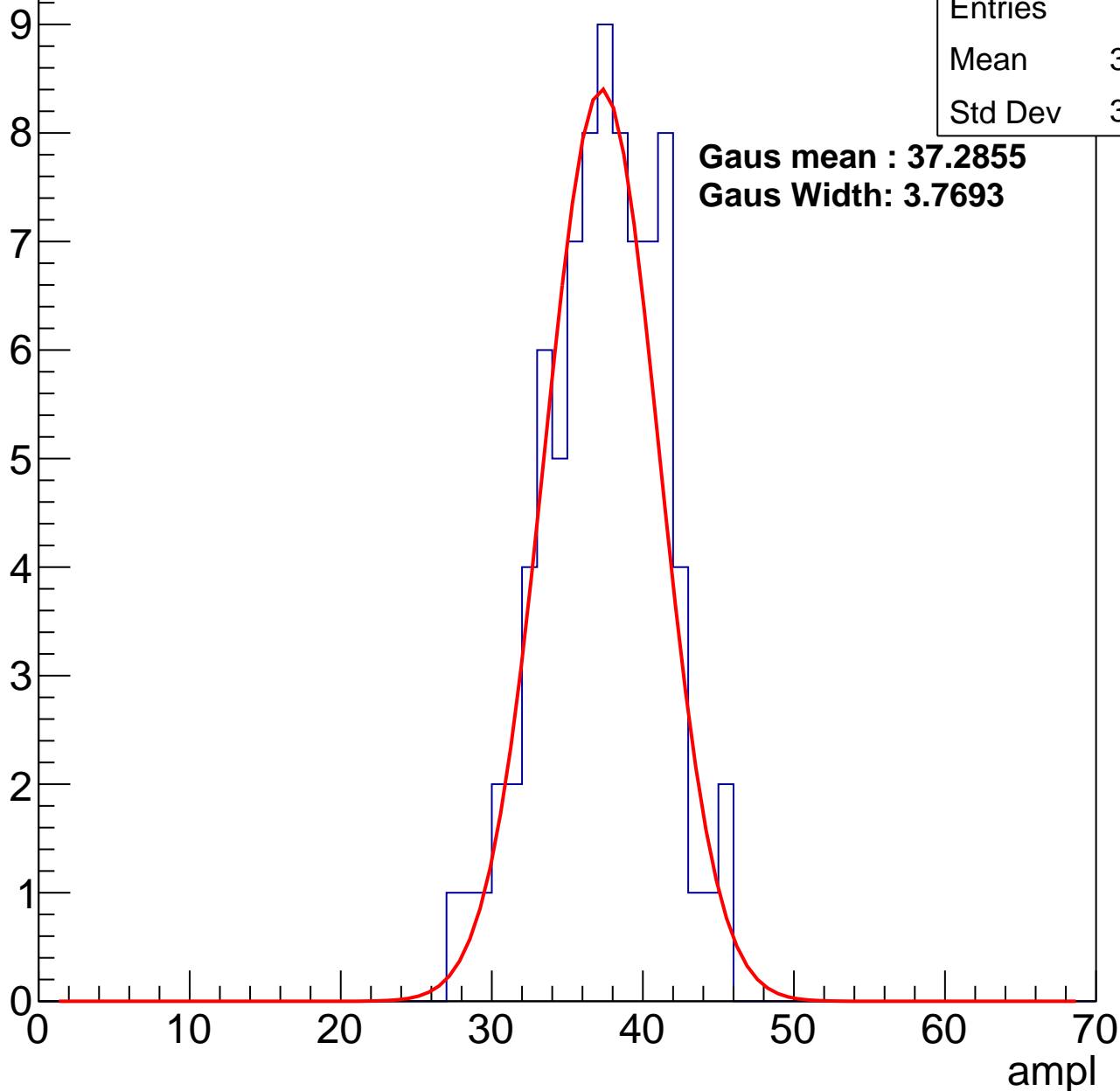
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	84
Mean	36.88
Std Dev	3.828

**Gaus mean : 37.2855**

**Gaus Width: 3.7693**



# B1L103S, U3-ch15, adc2

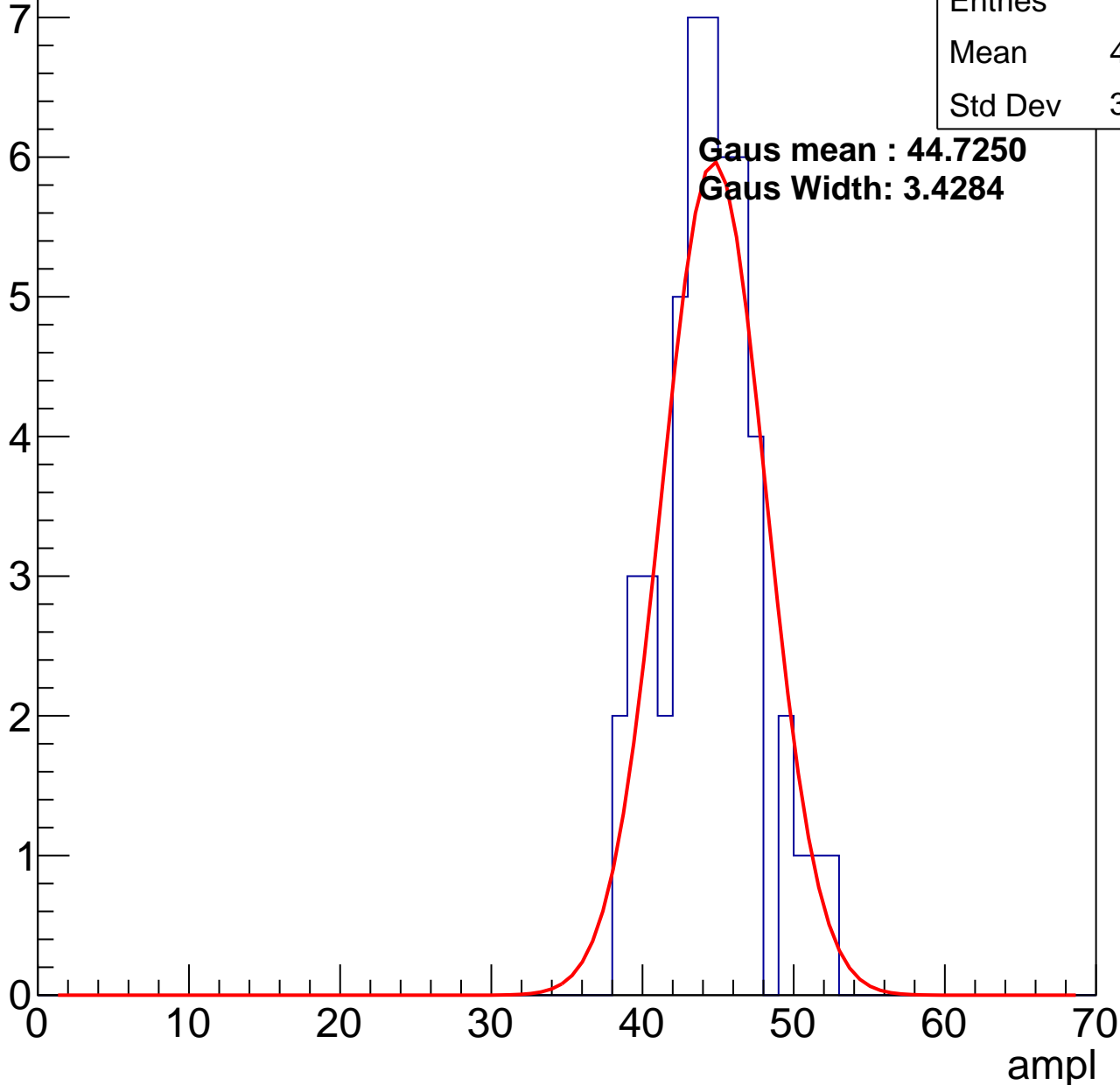
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	43.98
Std Dev	3.178

**Gaus mean : 44.7250**

**Gaus Width: 3.4284**

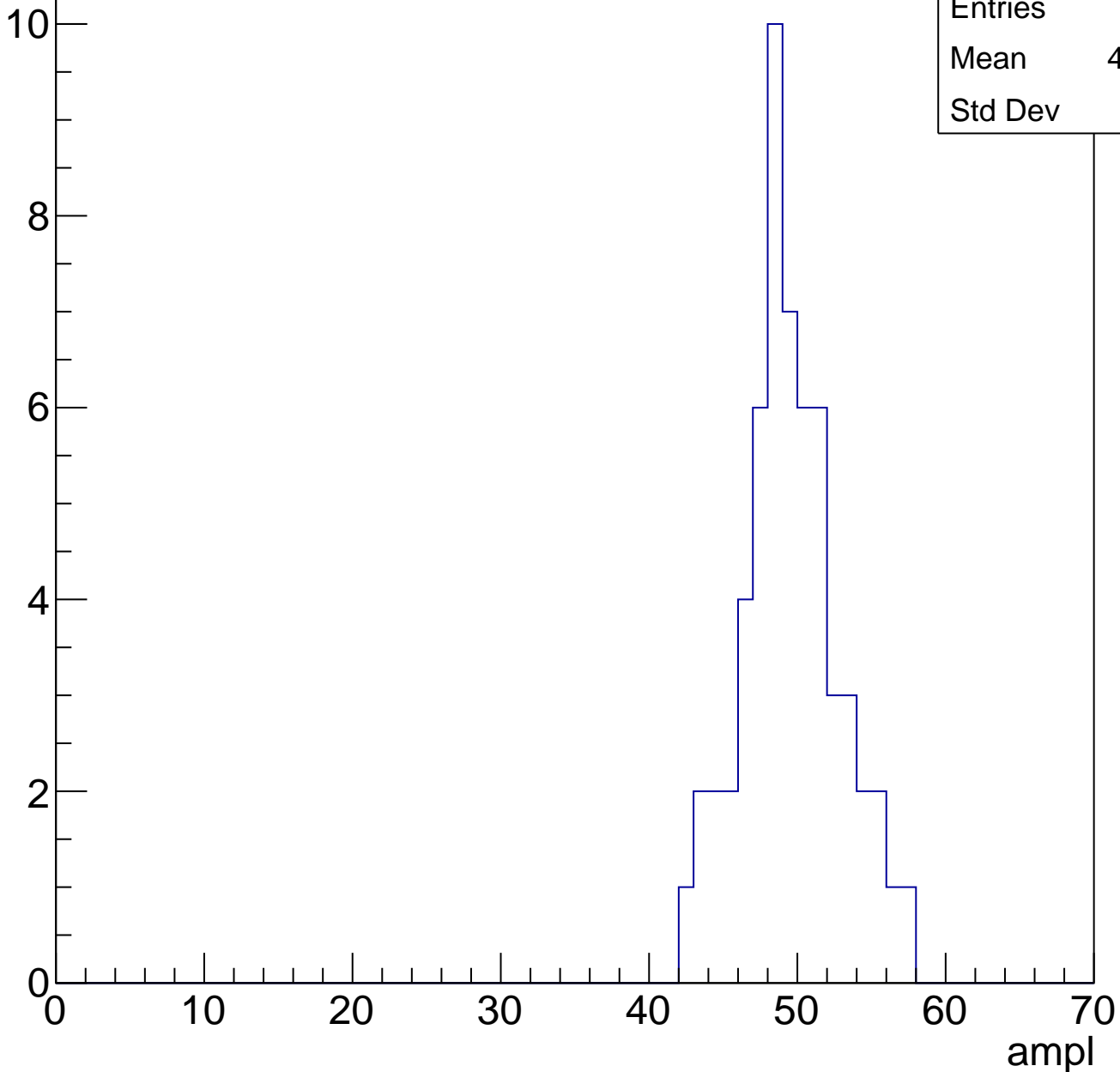


# B1L103S, U3-ch15, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

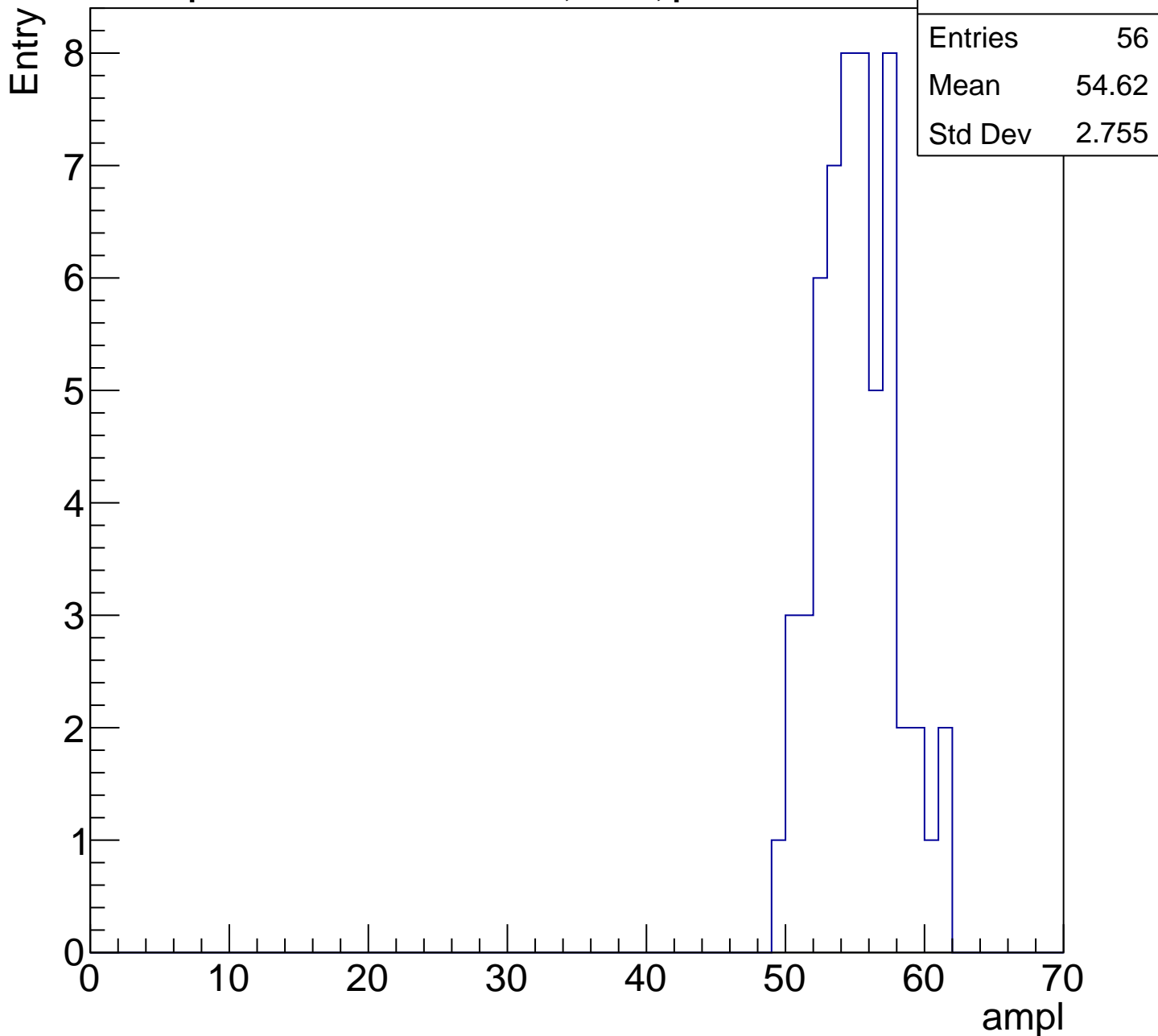
Entries	58
Mean	49.09
Std Dev	3.25

Entry



# B1L103S, U3-ch15, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

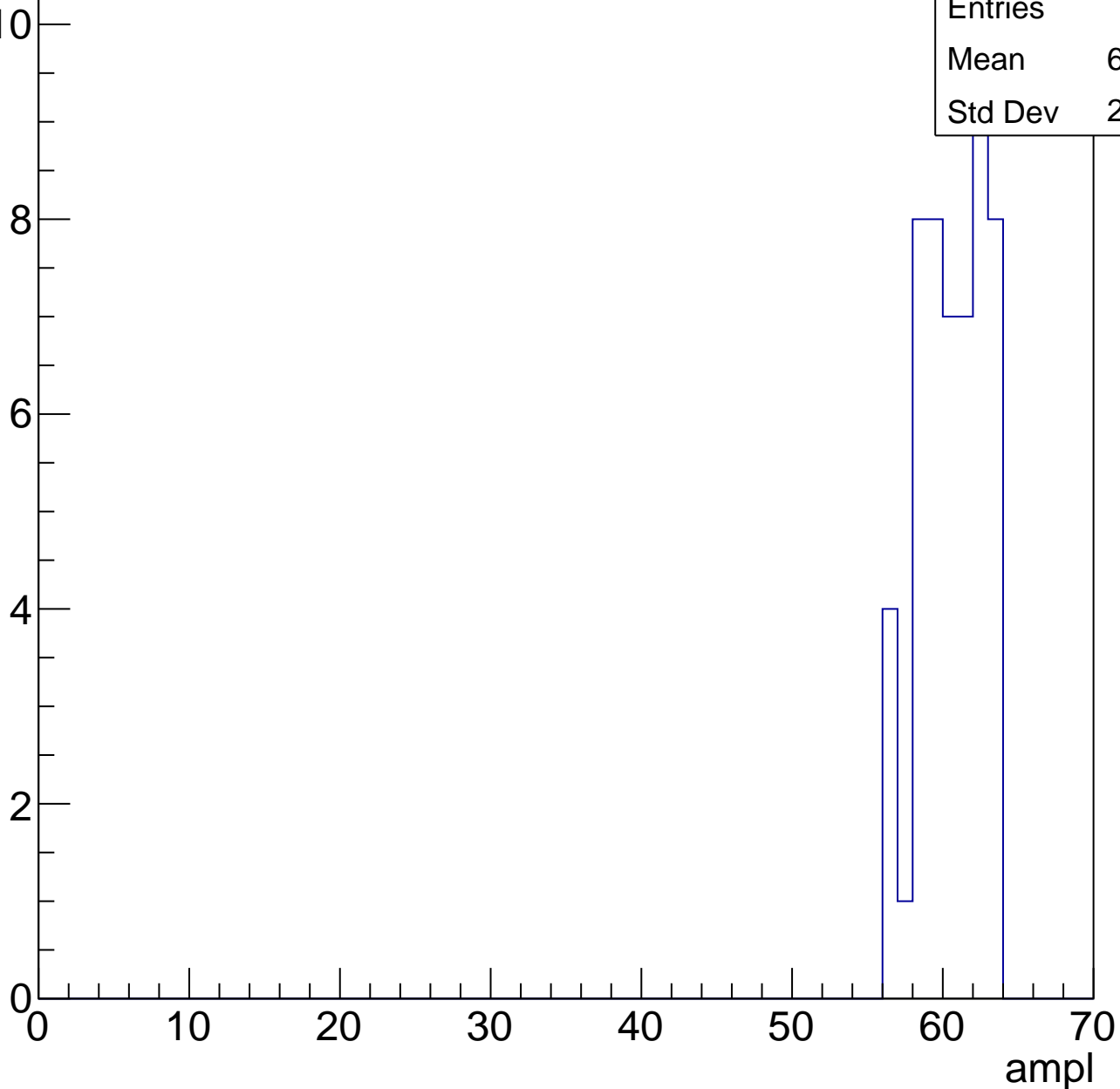


# B1L103S, U3-ch15, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	60.15
Std Dev	2.087



# B1L103S, U3-ch15, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	51.17
Std Dev	22.92

ampl

0 10 20 30 40 50 60 70



# B1L103S, U3-ch15, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U3-ch16, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	65
Mean	28.32
Std Dev	4.658

**Gaus mean : 30.8277**

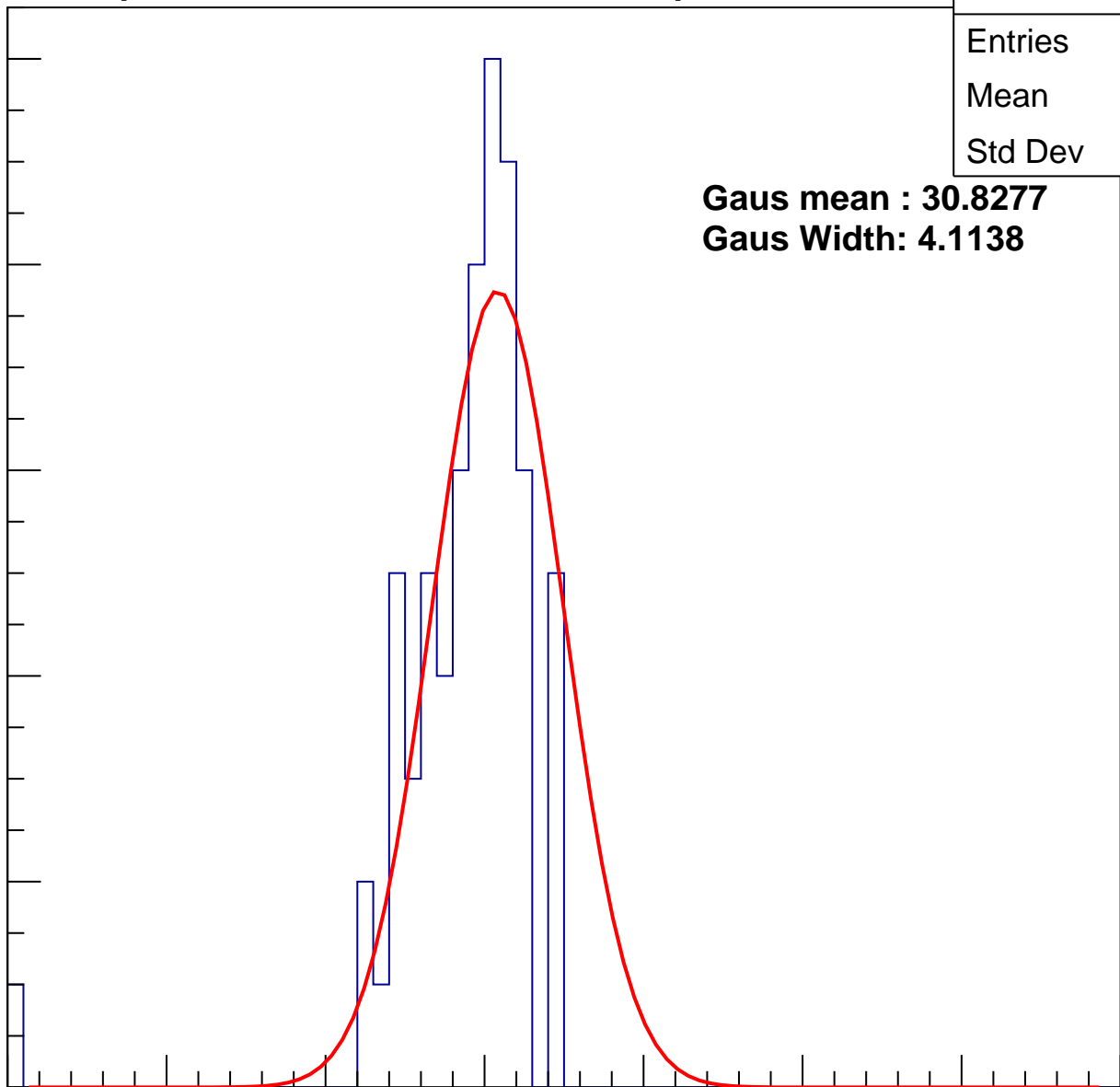
**Gaus Width: 4.1138**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U3-ch16, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	77
Mean	36.17
Std Dev	3.893

**Gaus mean : 36.8058**

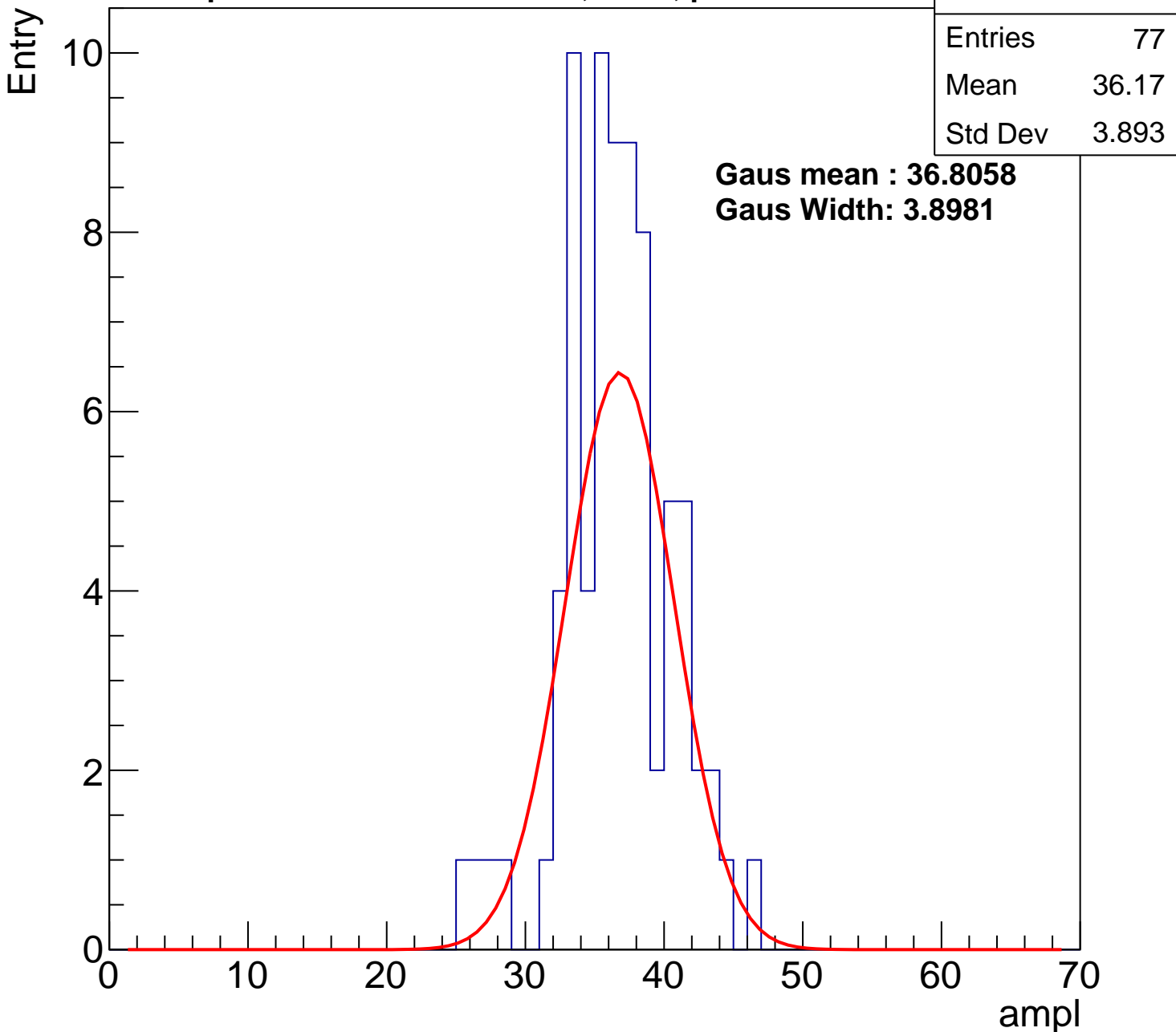
**Gaus Width: 3.8981**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U3-ch16, adc2

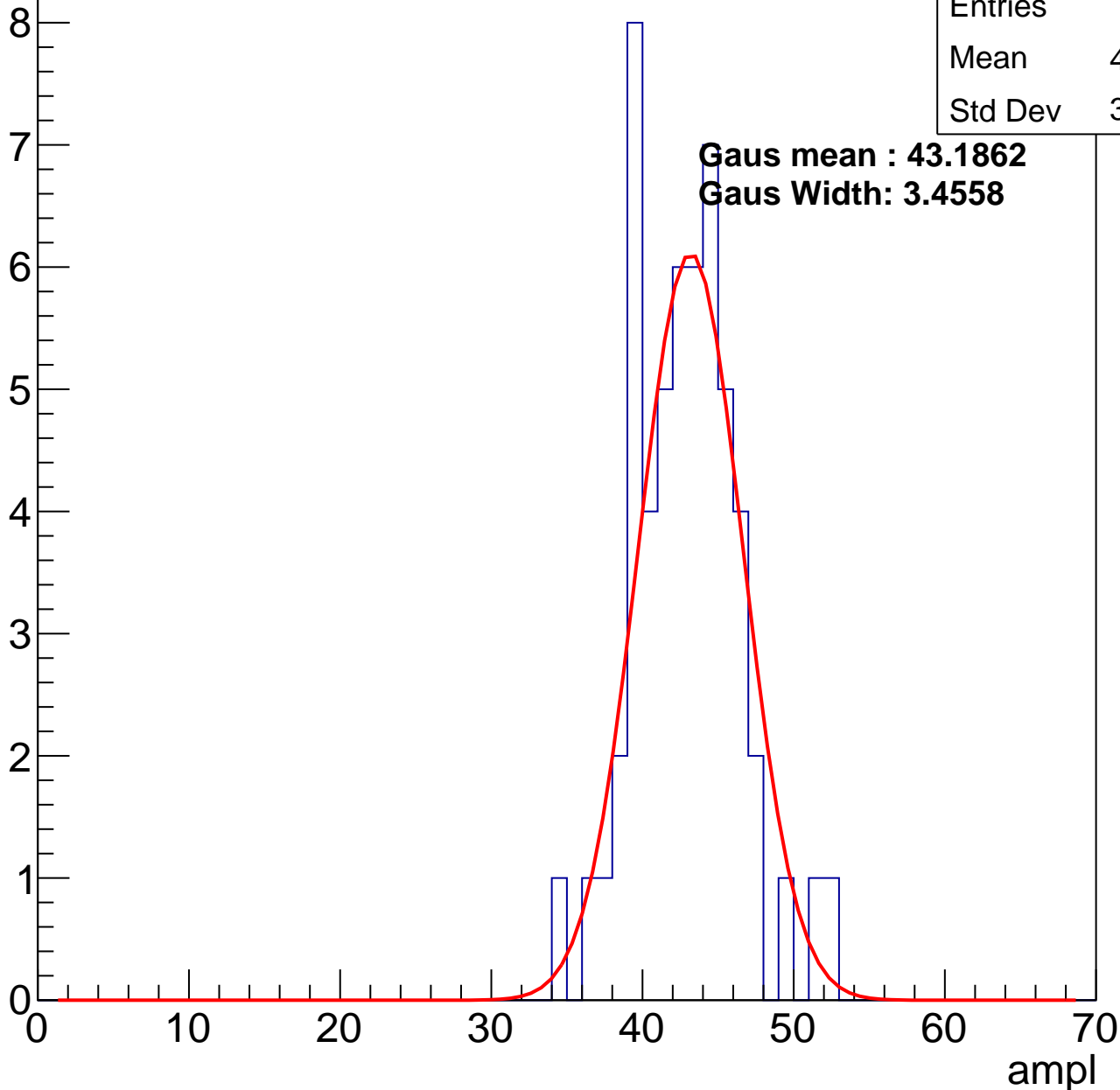
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	42.42
Std Dev	3.473

**Gaus mean : 43.1862**

**Gaus Width: 3.4558**

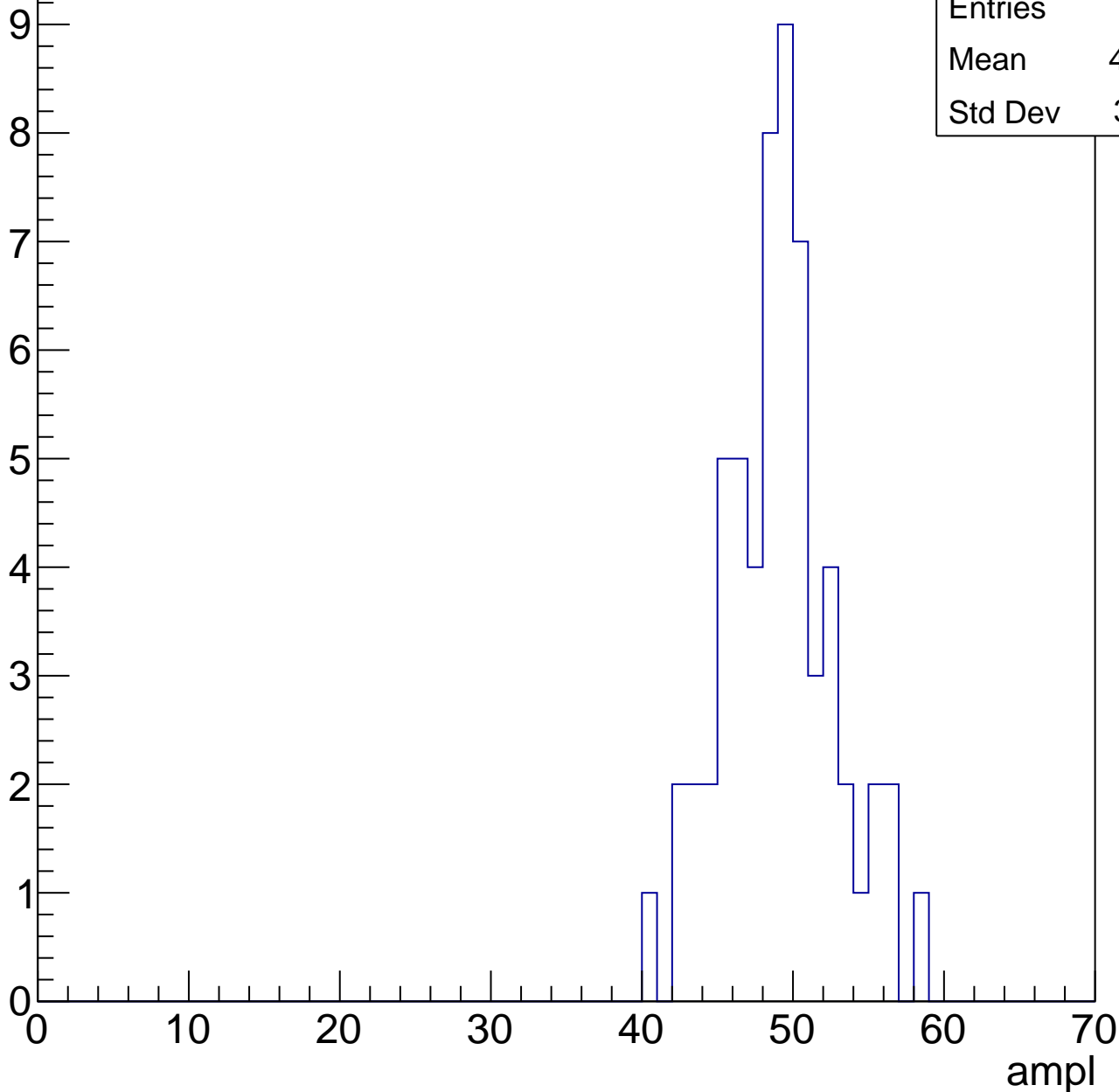


# B1L103S, U3-ch16, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	48.62
Std Dev	3.661

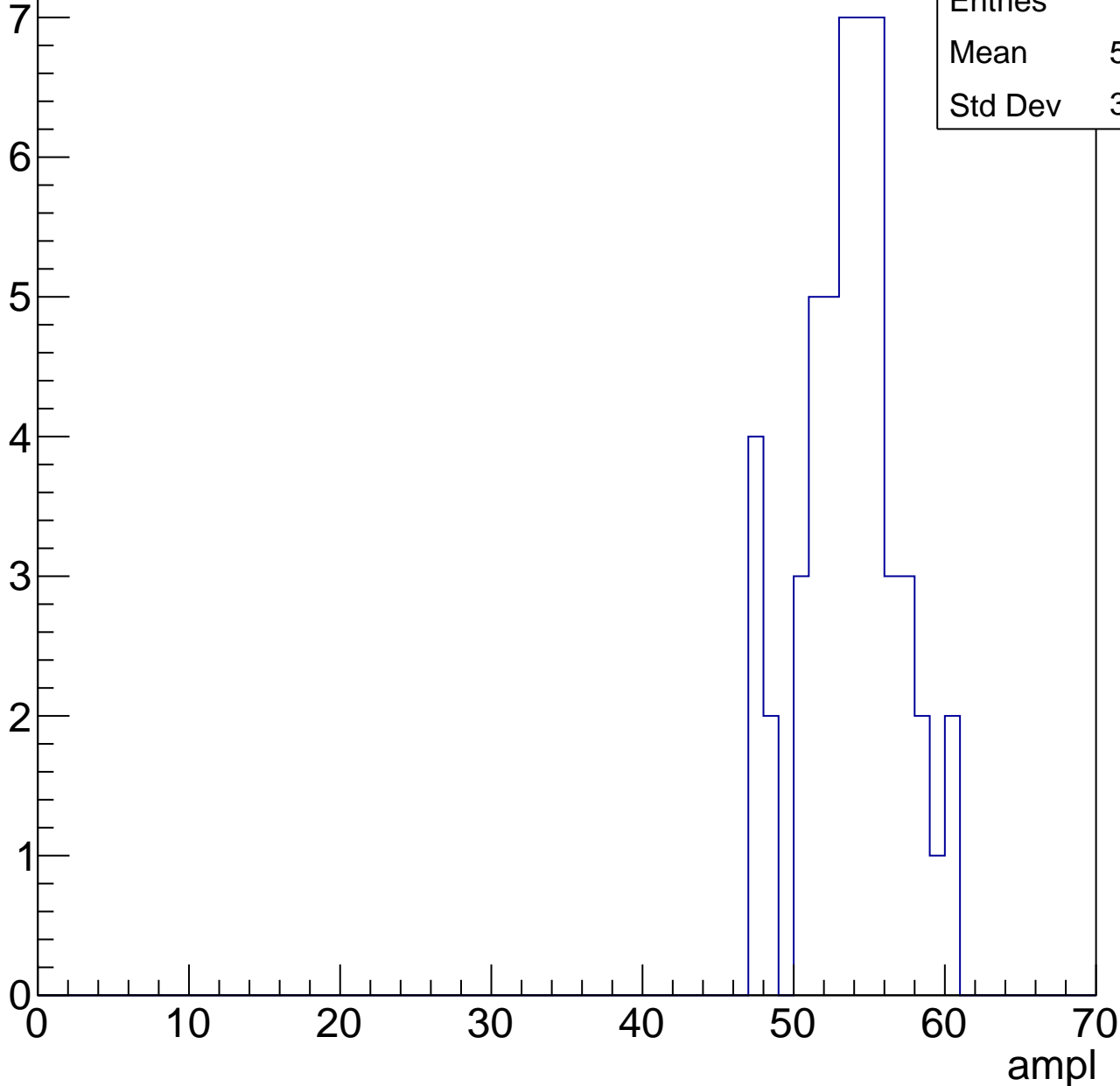


# B1L103S, U3-ch16, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	53.27
Std Dev	3.242

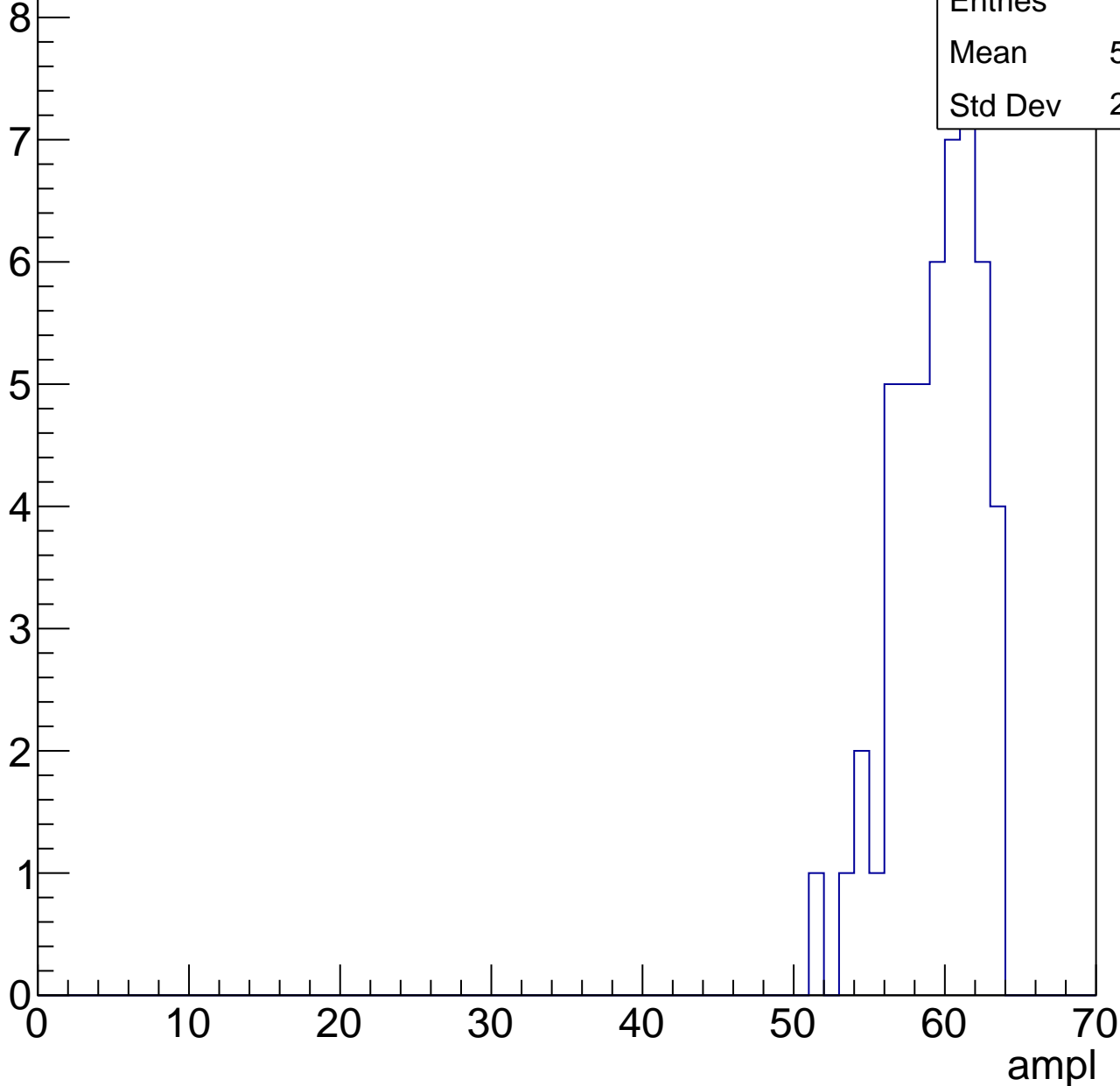


# B1L103S, U3-ch16, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	58.98
Std Dev	2.776

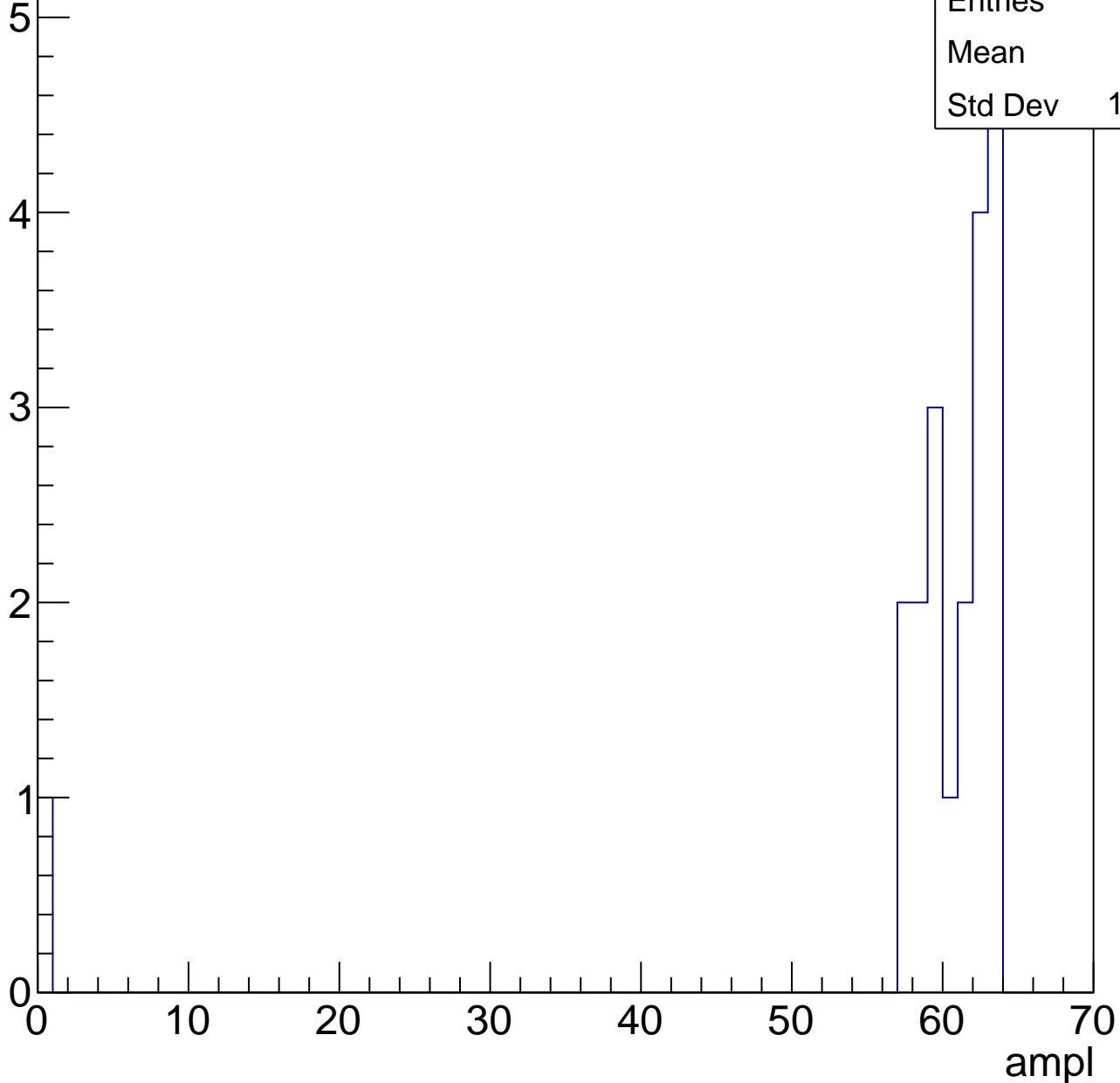


# B1L103S, U3-ch16, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	20
Mean	57.6
Std Dev	13.37





# B1L103S, U3-ch16, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch17, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	60
Mean	29.05
Std Dev	3.533

**Gaus mean : 30.1004**

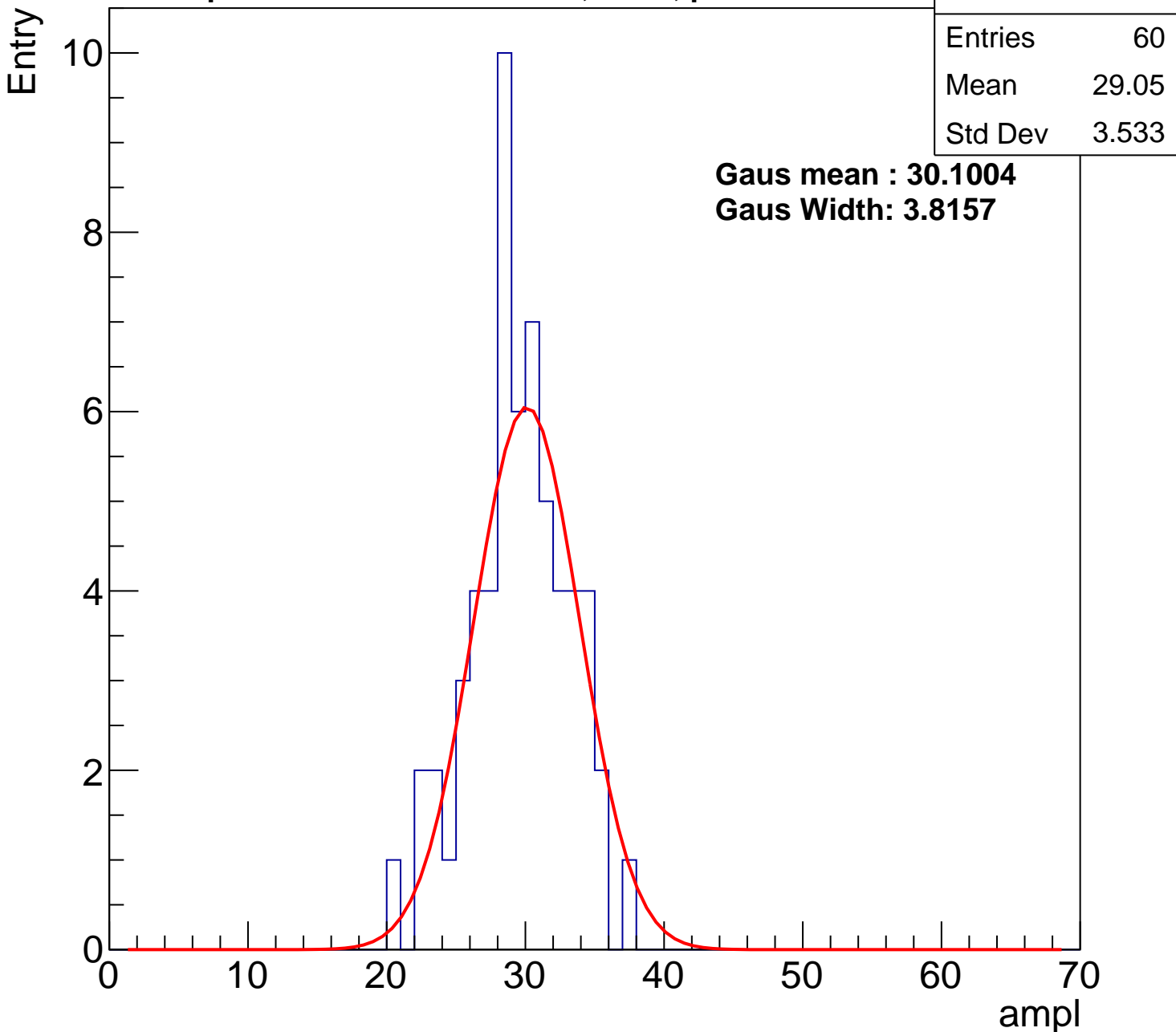
**Gaus Width: 3.8157**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U3-ch17, adc1

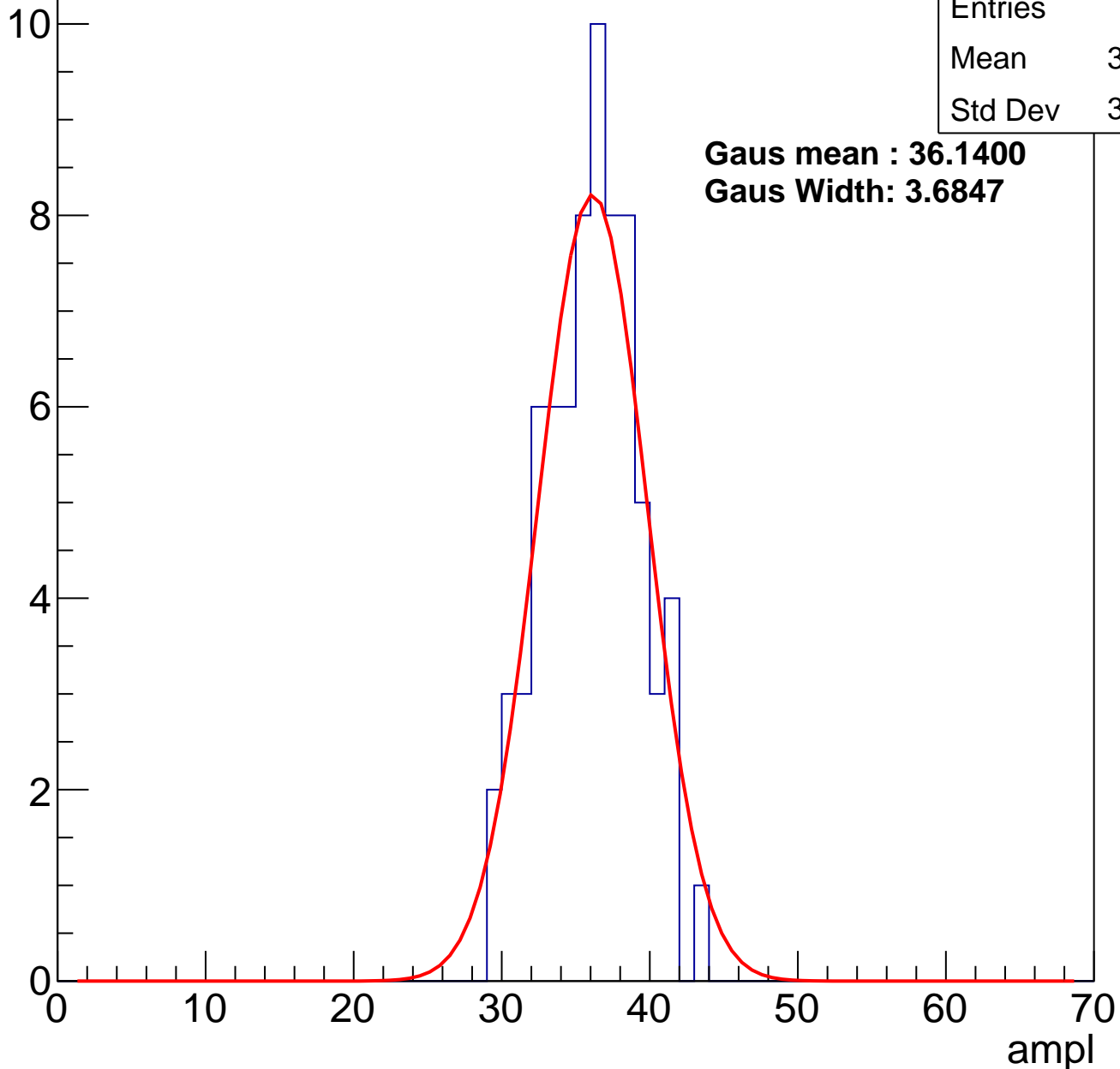
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	73
Mean	35.58
Std Dev	3.166

**Gaus mean : 36.1400**

**Gaus Width: 3.6847**

Entry



# B1L103S, U3-ch17, adc2

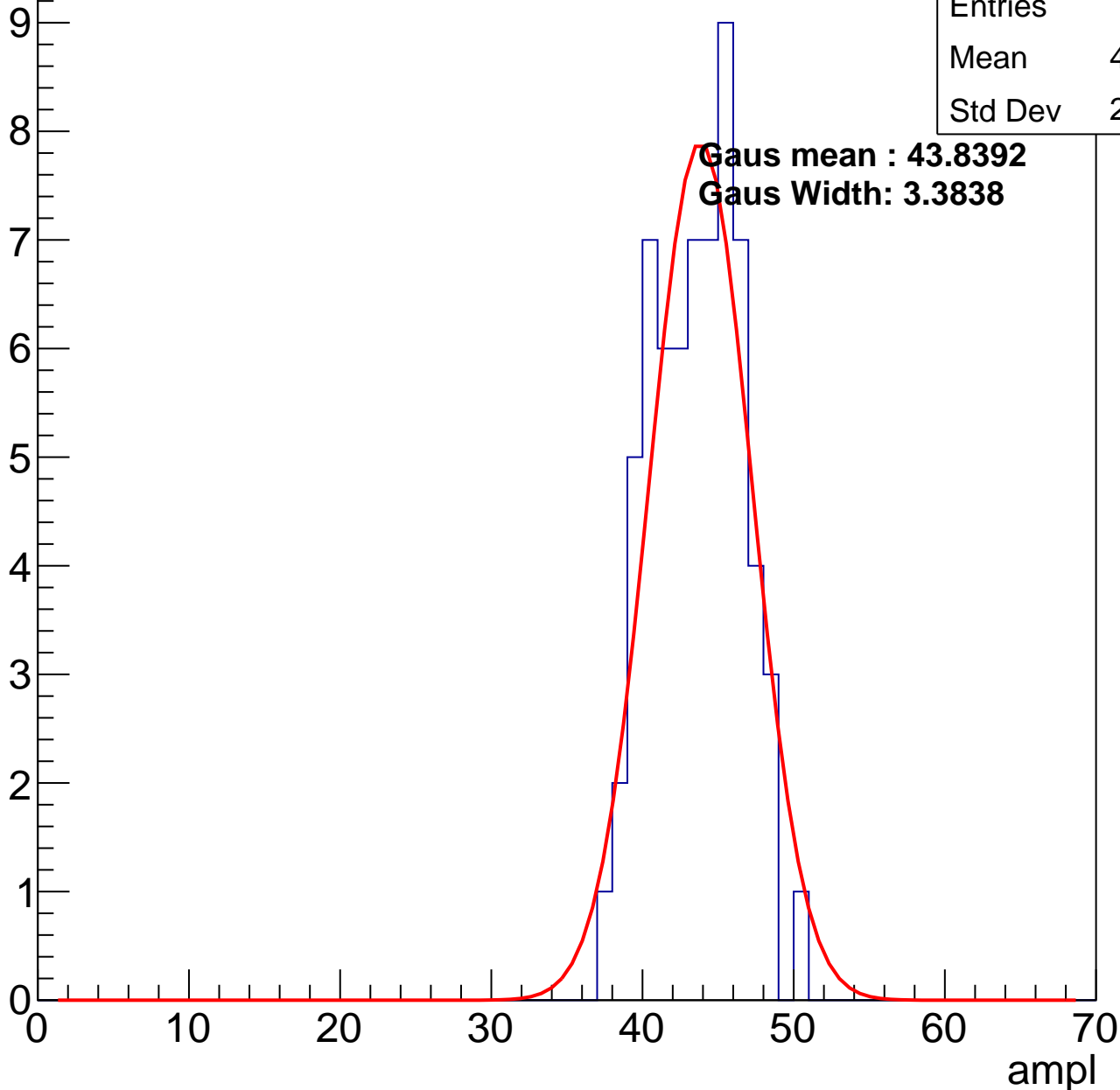
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	43.14
Std Dev	2.914

**Gaus mean : 43.8392**

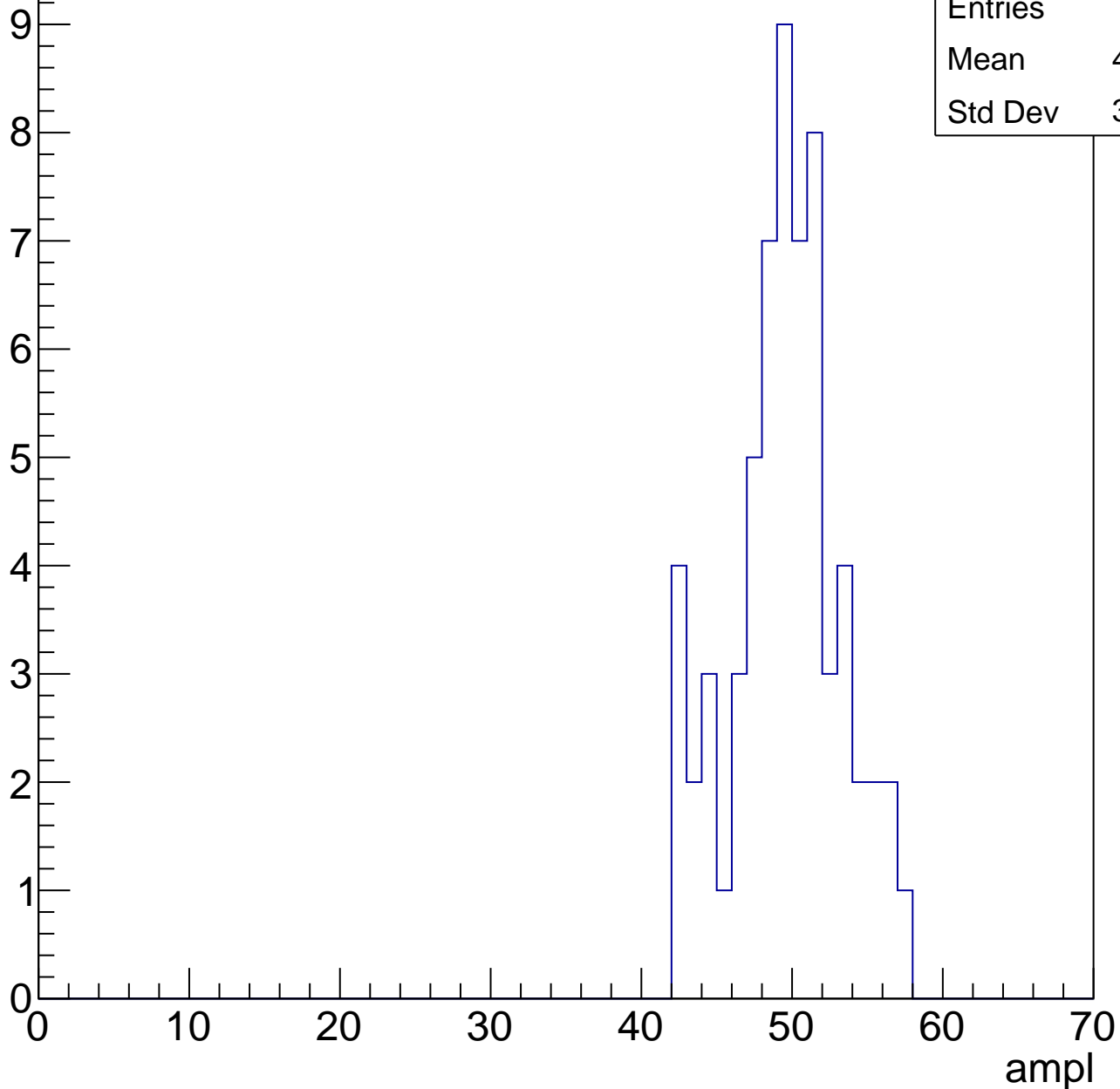
**Gaus Width: 3.3838**



# B1L103S, U3-ch17, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



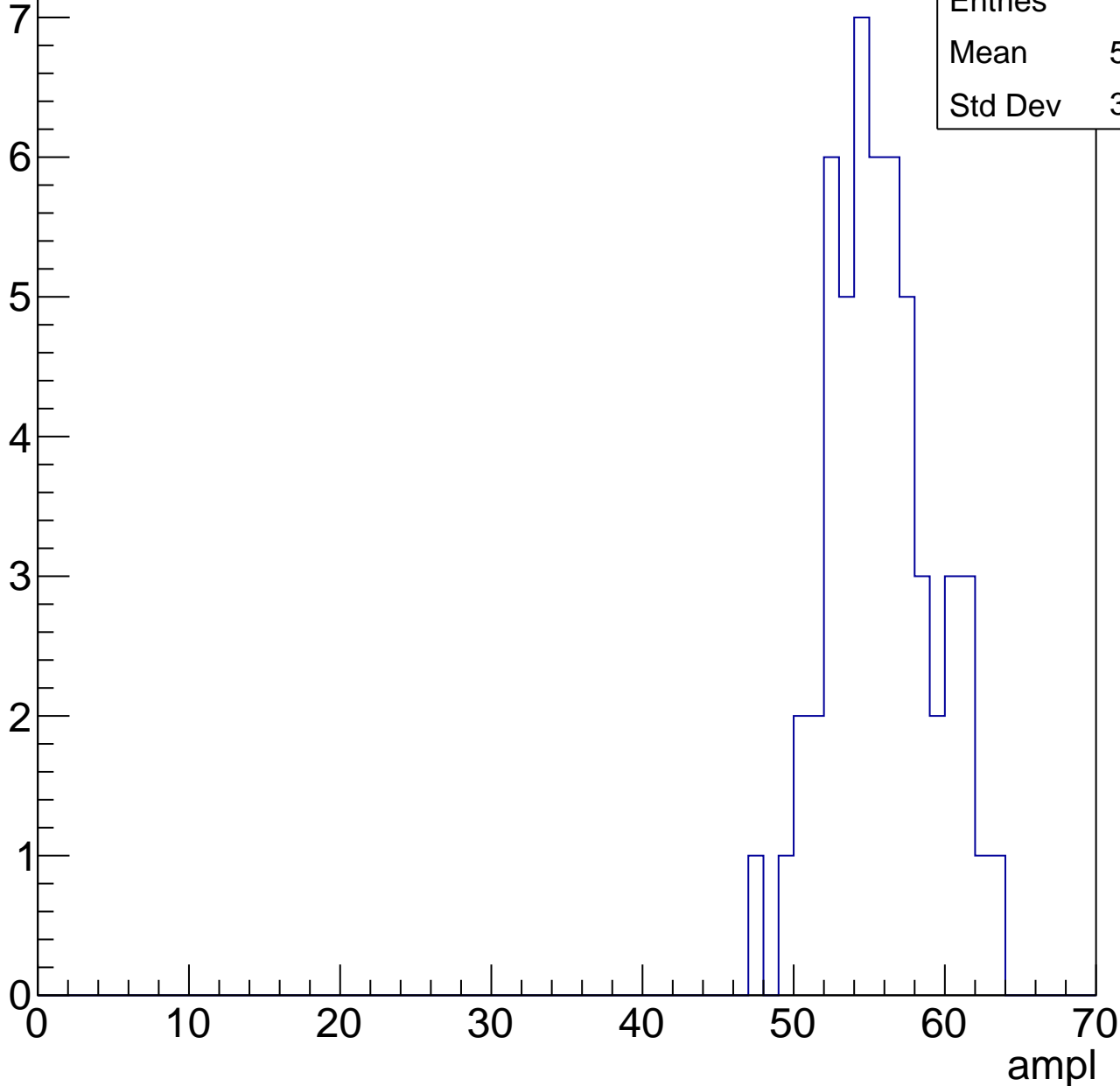
Entries	63
Mean	49.11
Std Dev	3.621

# B1L103S, U3-ch17, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	55.26
Std Dev	3.444

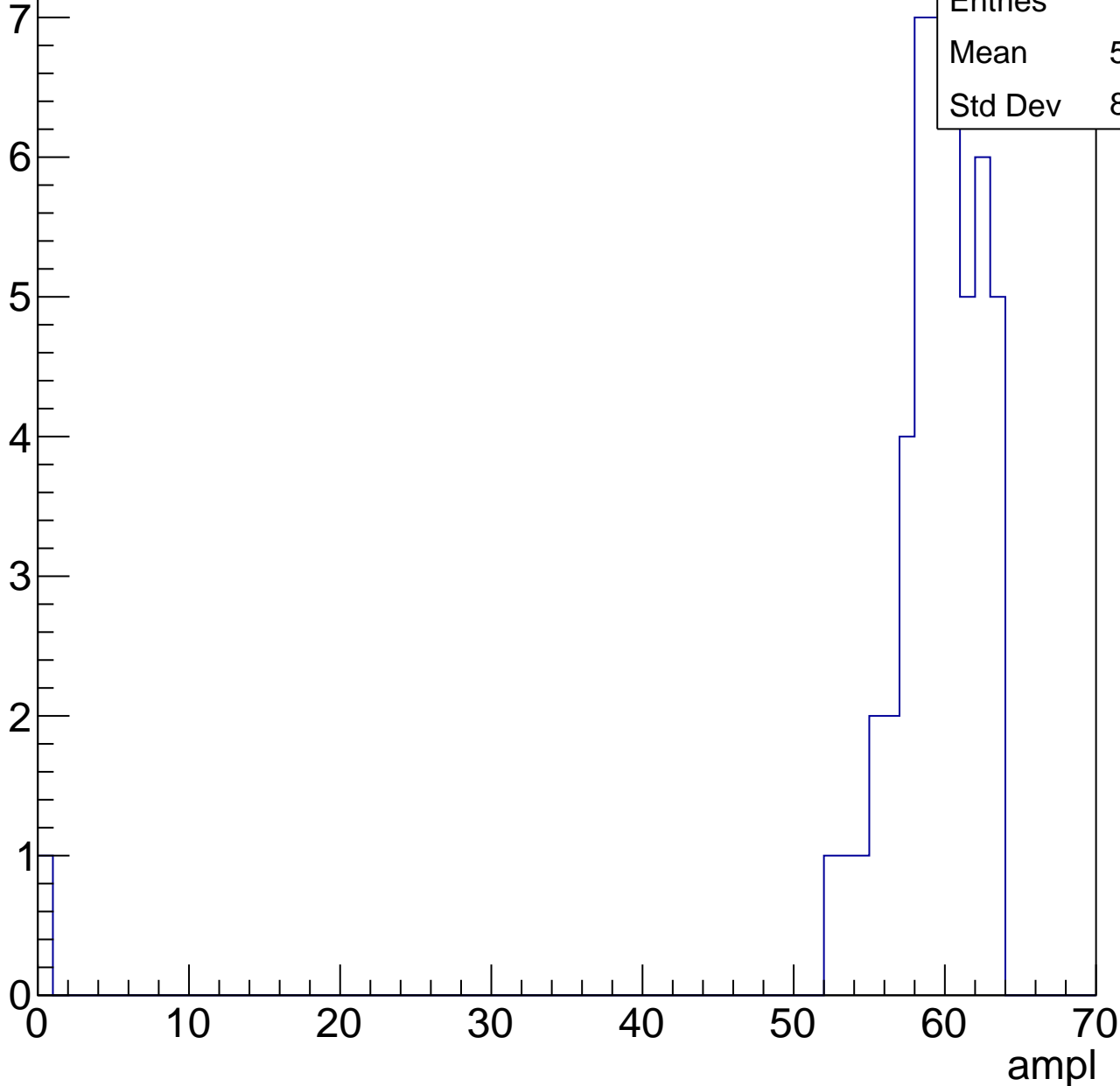


# B1L103S, U3-ch17, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

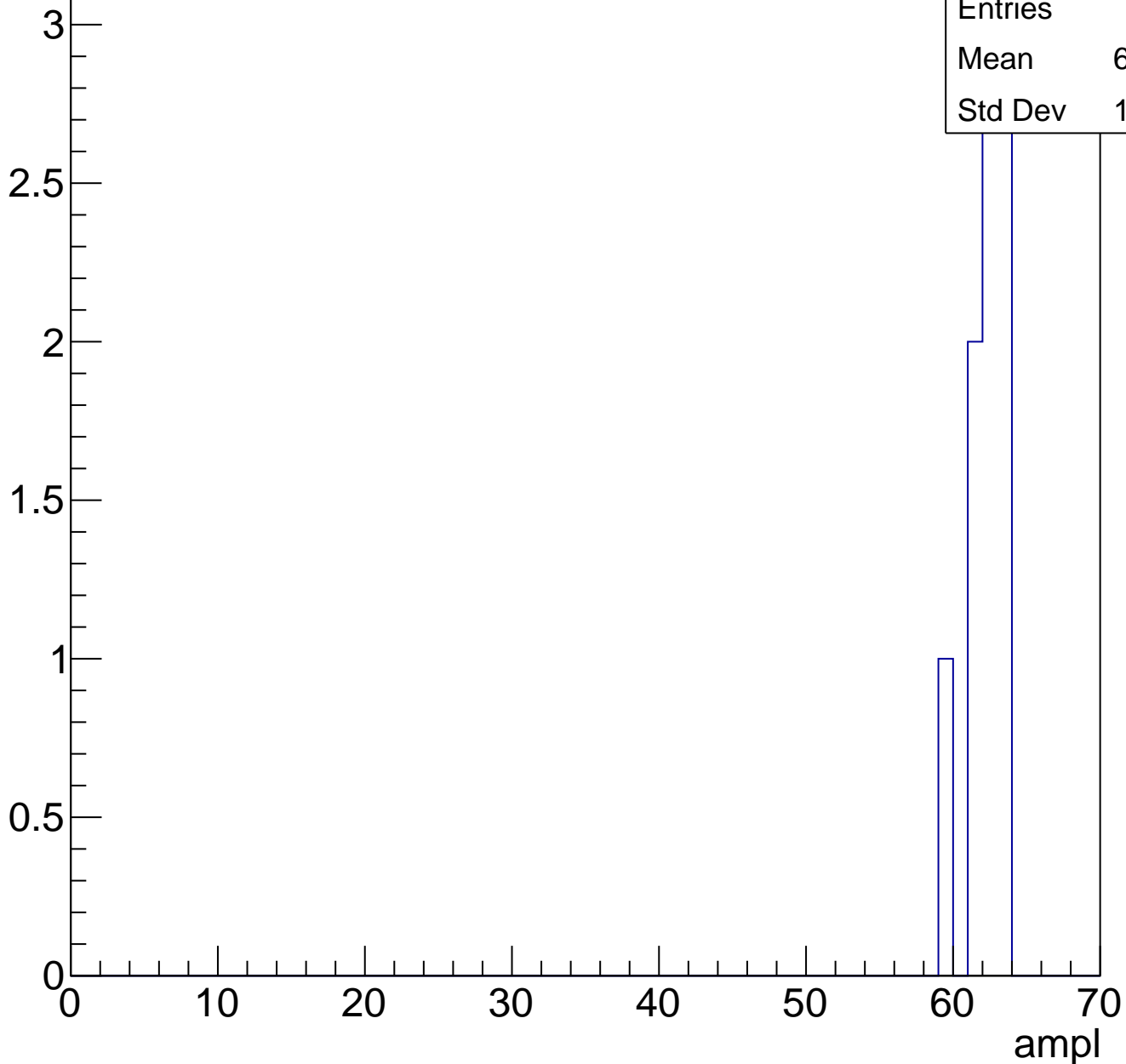
Entries	49
Mean	57.96
Std Dev	8.774



# B1L103S, U3-ch17, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U3-ch17, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch18, adc0

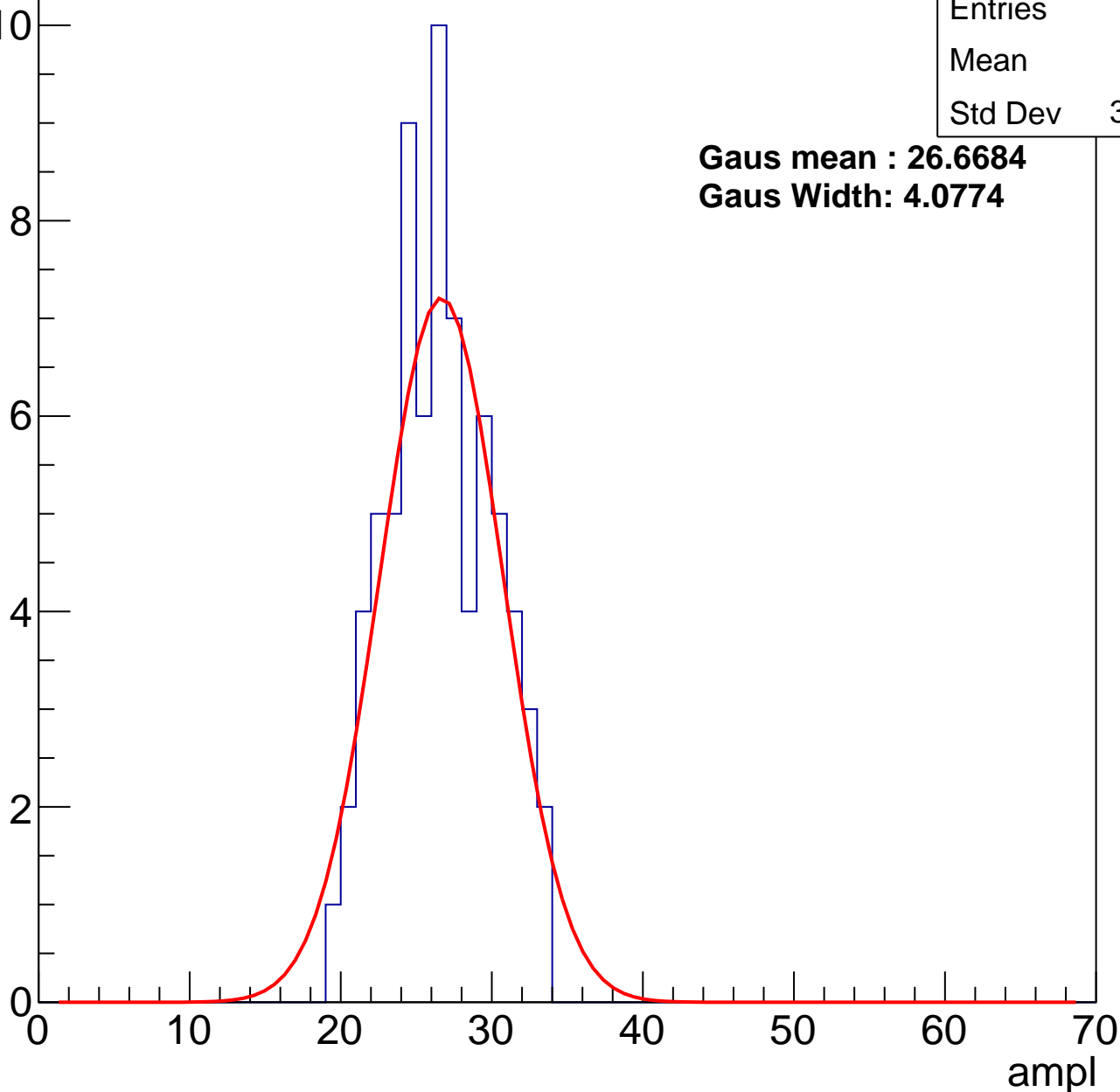
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	26.1
Std Dev	3.413

**Gaus mean : 26.6684**

**Gaus Width: 4.0774**



# B1L103S, U3-ch18, adc1

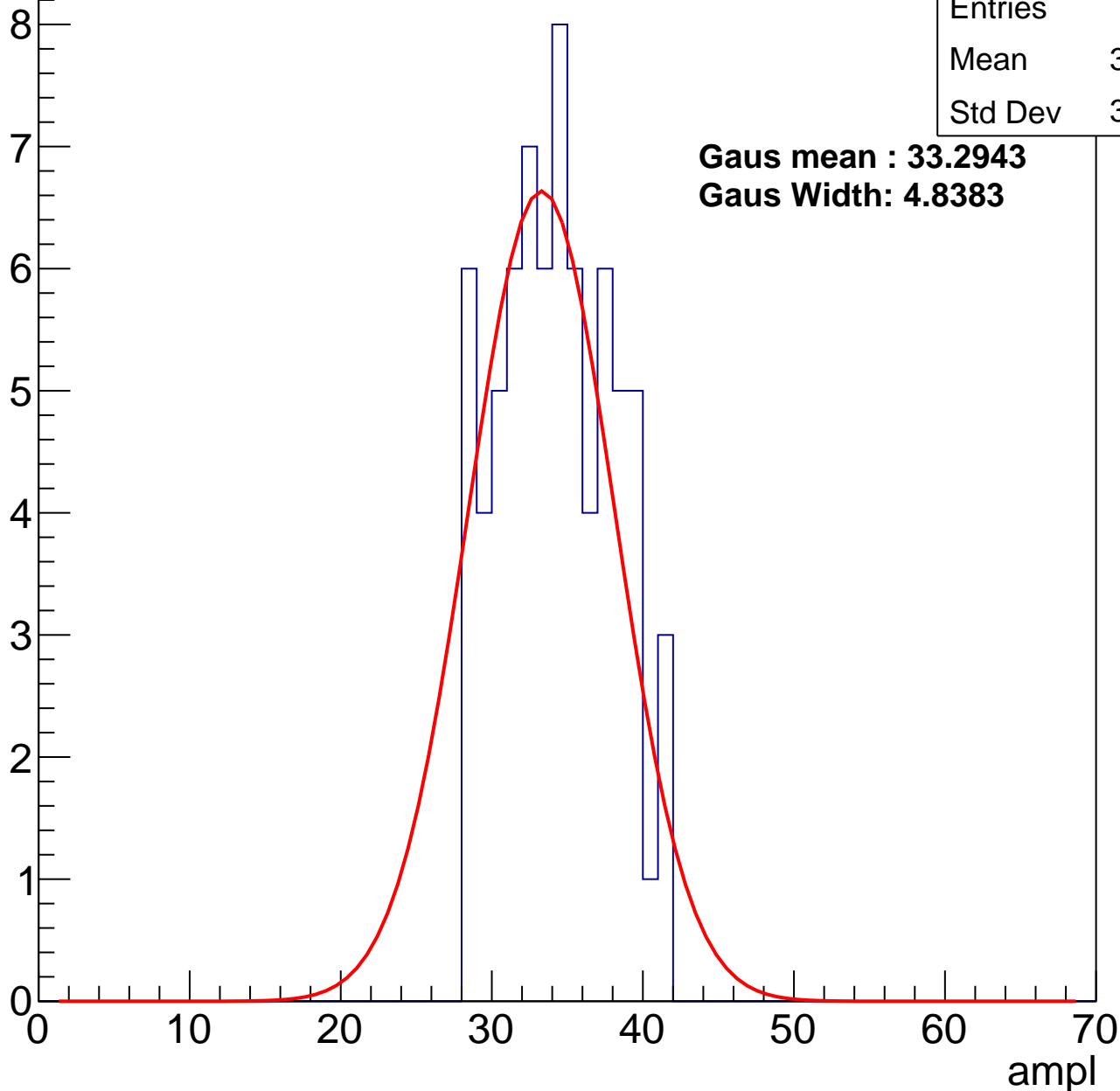
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	33.86
Std Dev	3.626

**Gaus mean : 33.2943**

**Gaus Width: 4.8383**



# B1L103S, U3-ch18, adc2

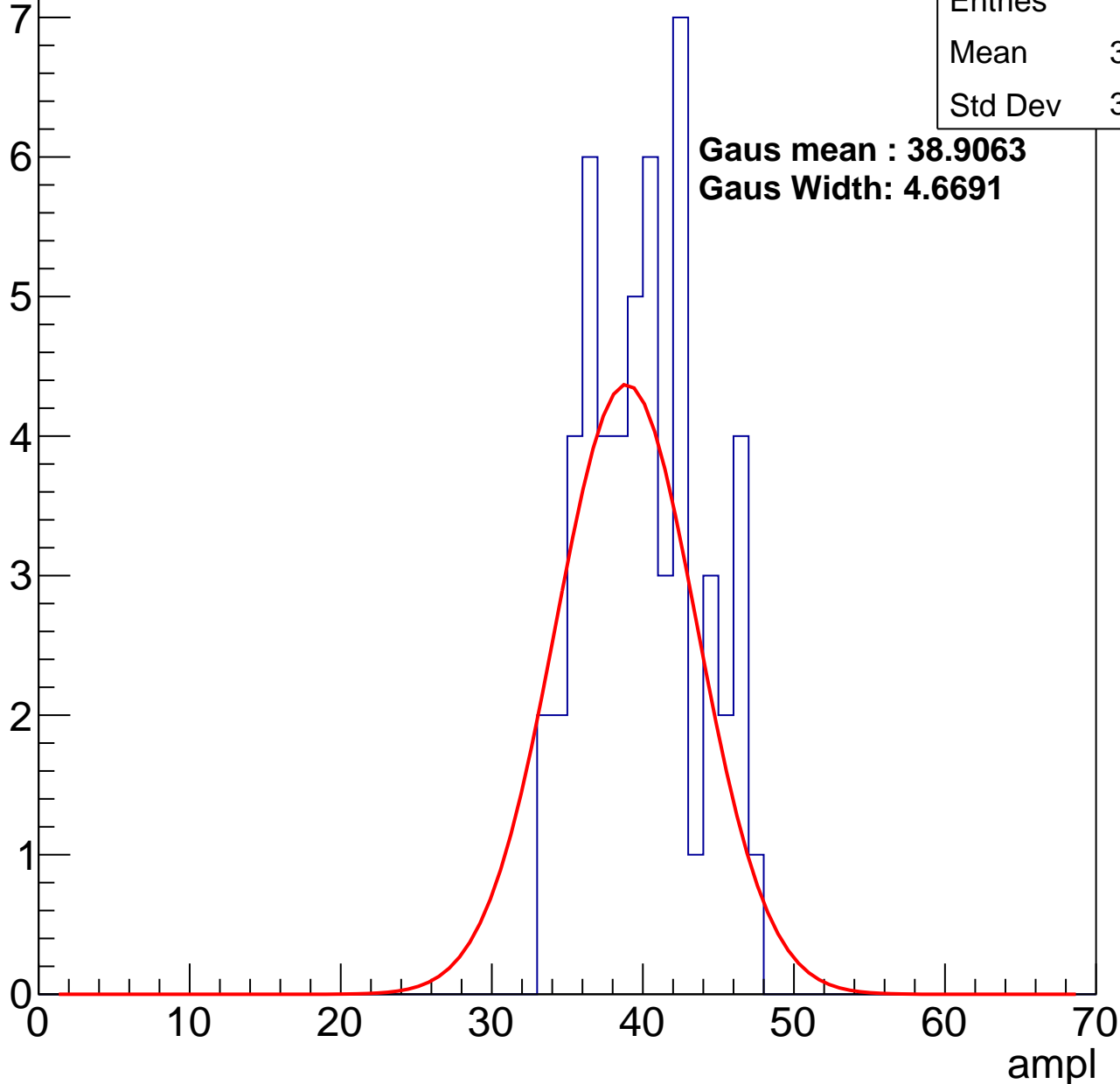
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	39.59
Std Dev	3.714

**Gaus mean : 38.9063**

**Gaus Width: 4.6691**



# B1L103S, U3-ch18, adc3

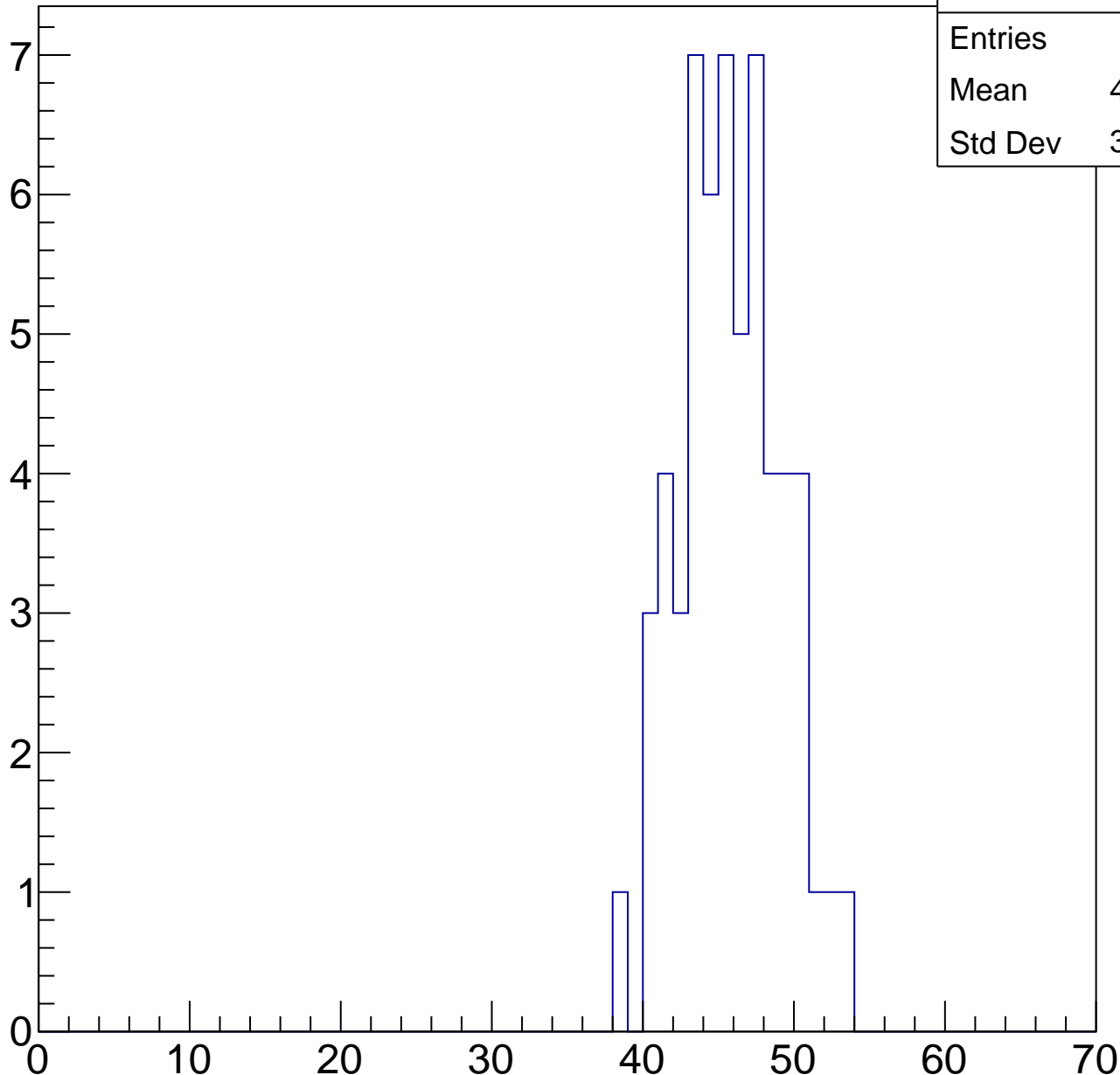
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

7  
6  
5  
4  
3  
2  
1  
0

Entries	58
Mean	45.36
Std Dev	3.278

ampl

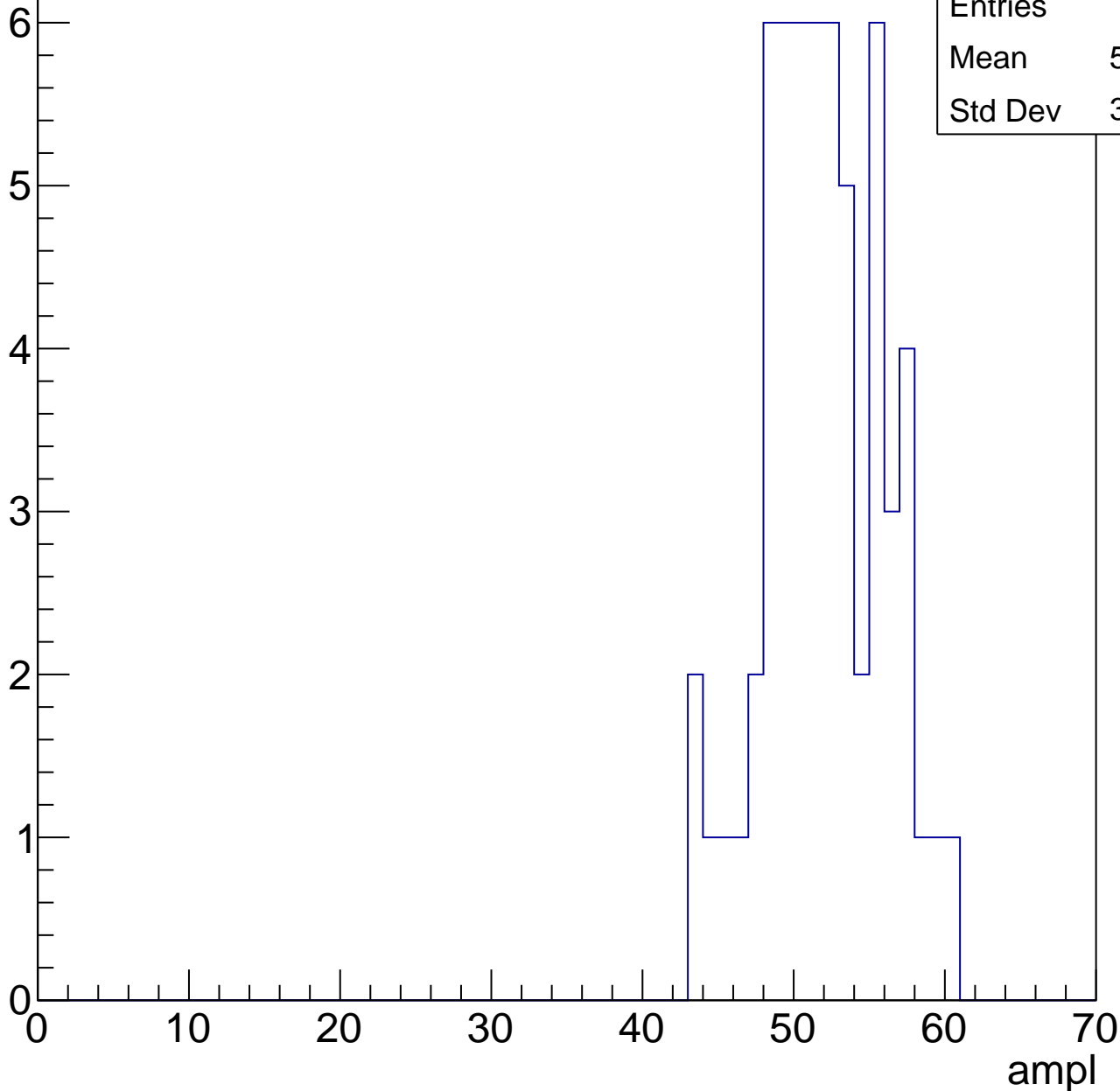


# B1L103S, U3-ch18, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	51.52
Std Dev	3.854

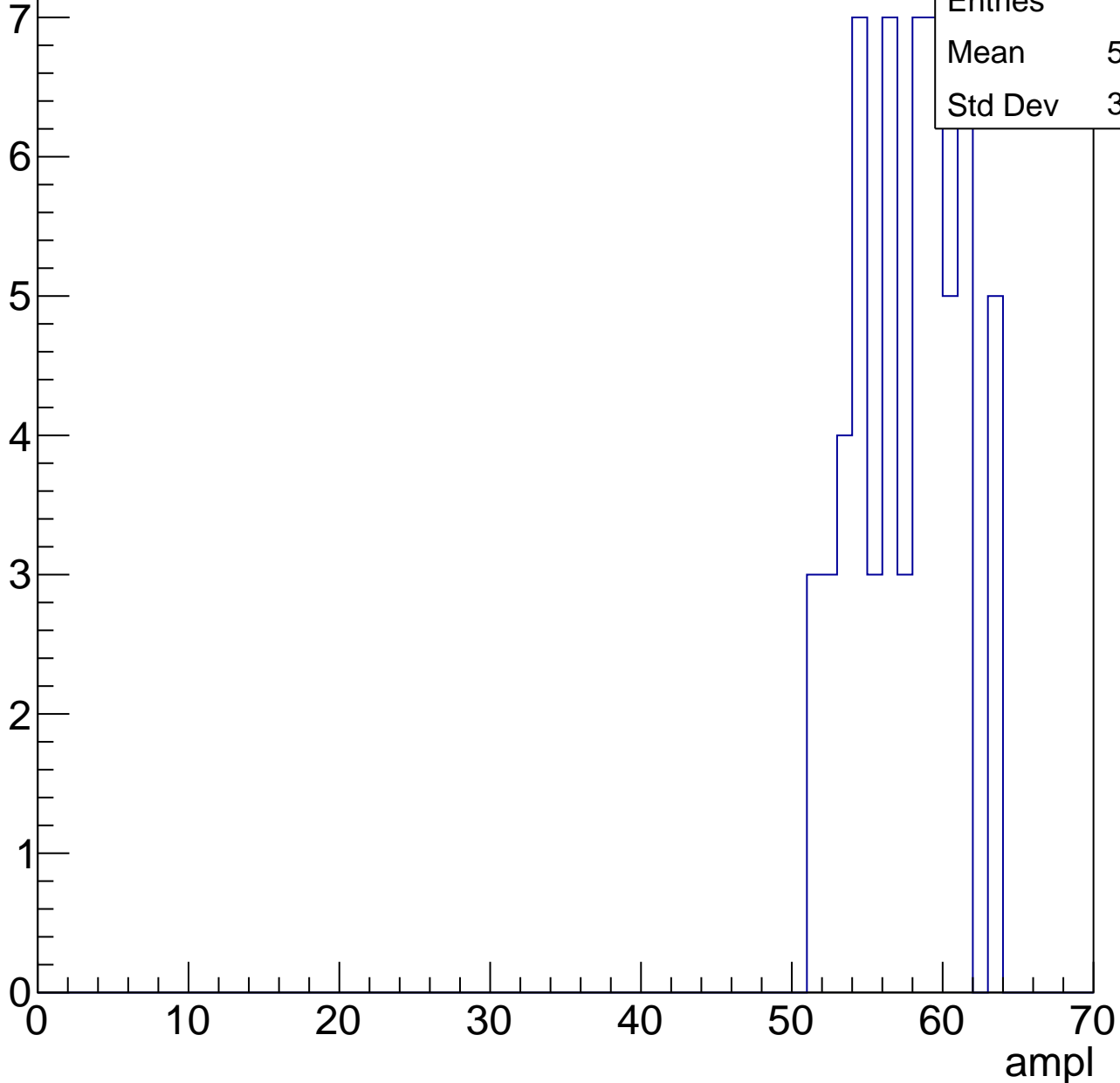


# B1L103S, U3-ch18, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	57.18
Std Dev	3.385

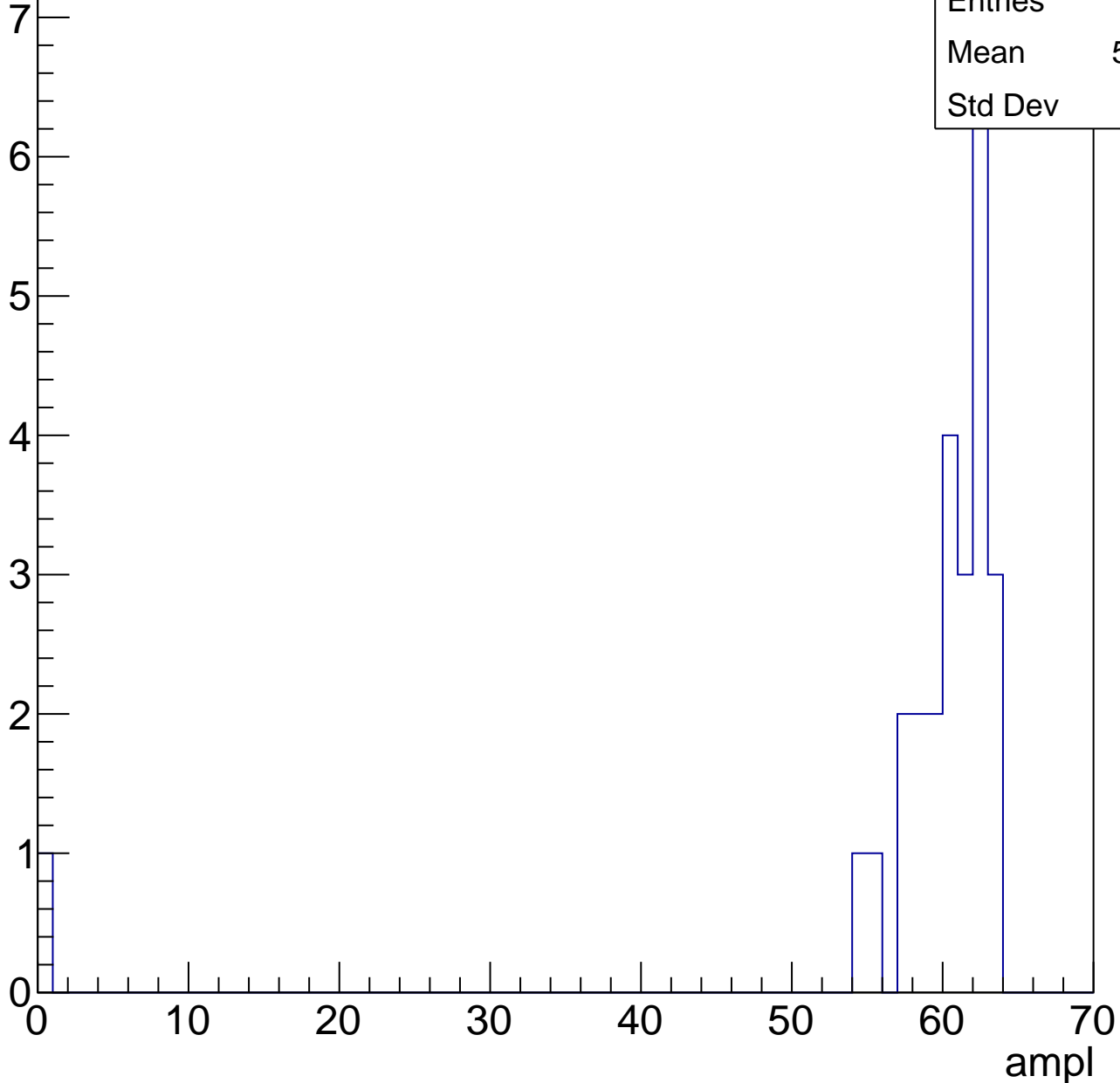


# B1L103S, U3-ch18, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	26
Mean	57.81
Std Dev	11.8

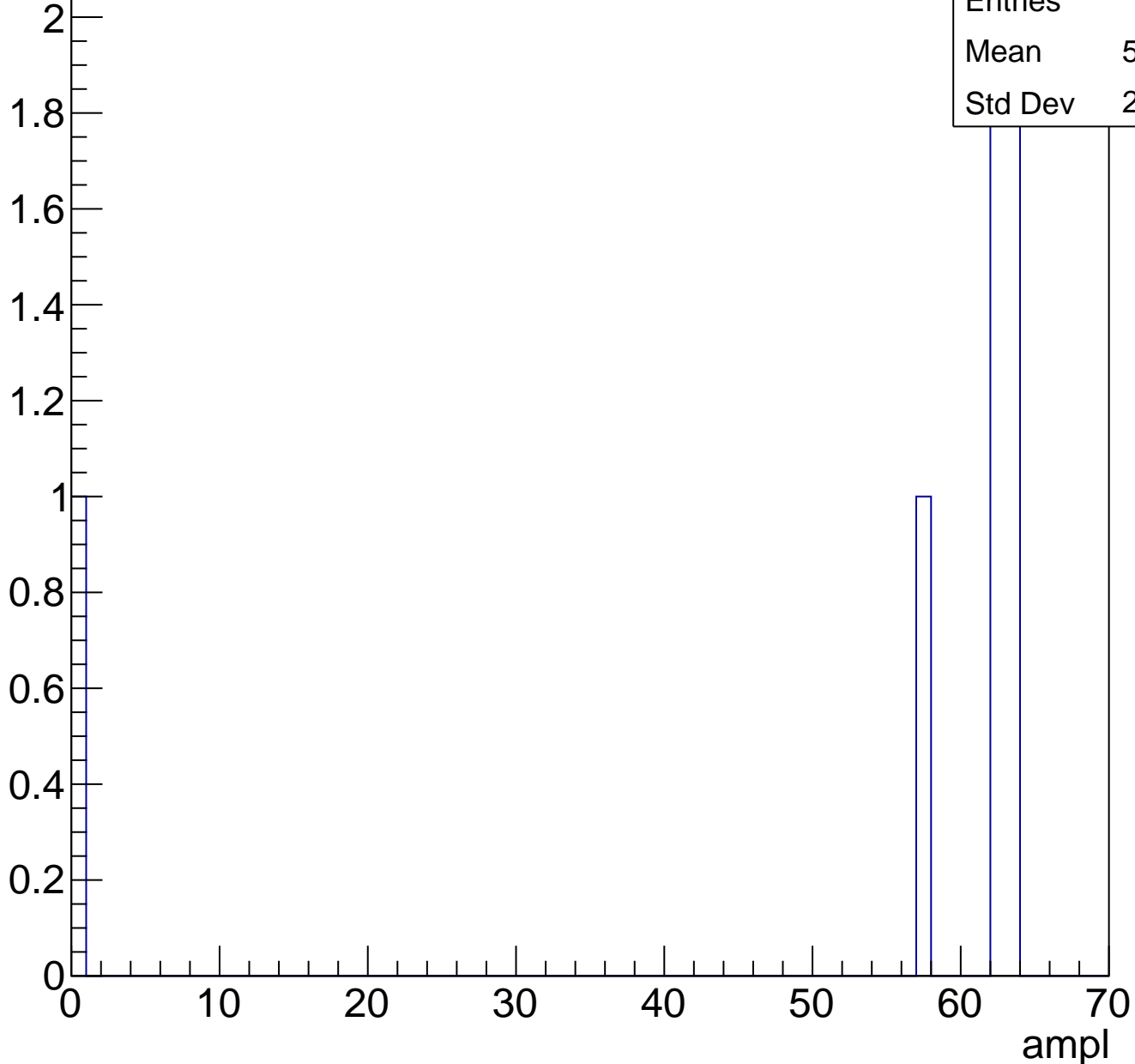




# B1L103S, U3-ch18, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	6
Mean	51.17
Std Dev	22.97

# B1L103S, U3-ch19, adc0

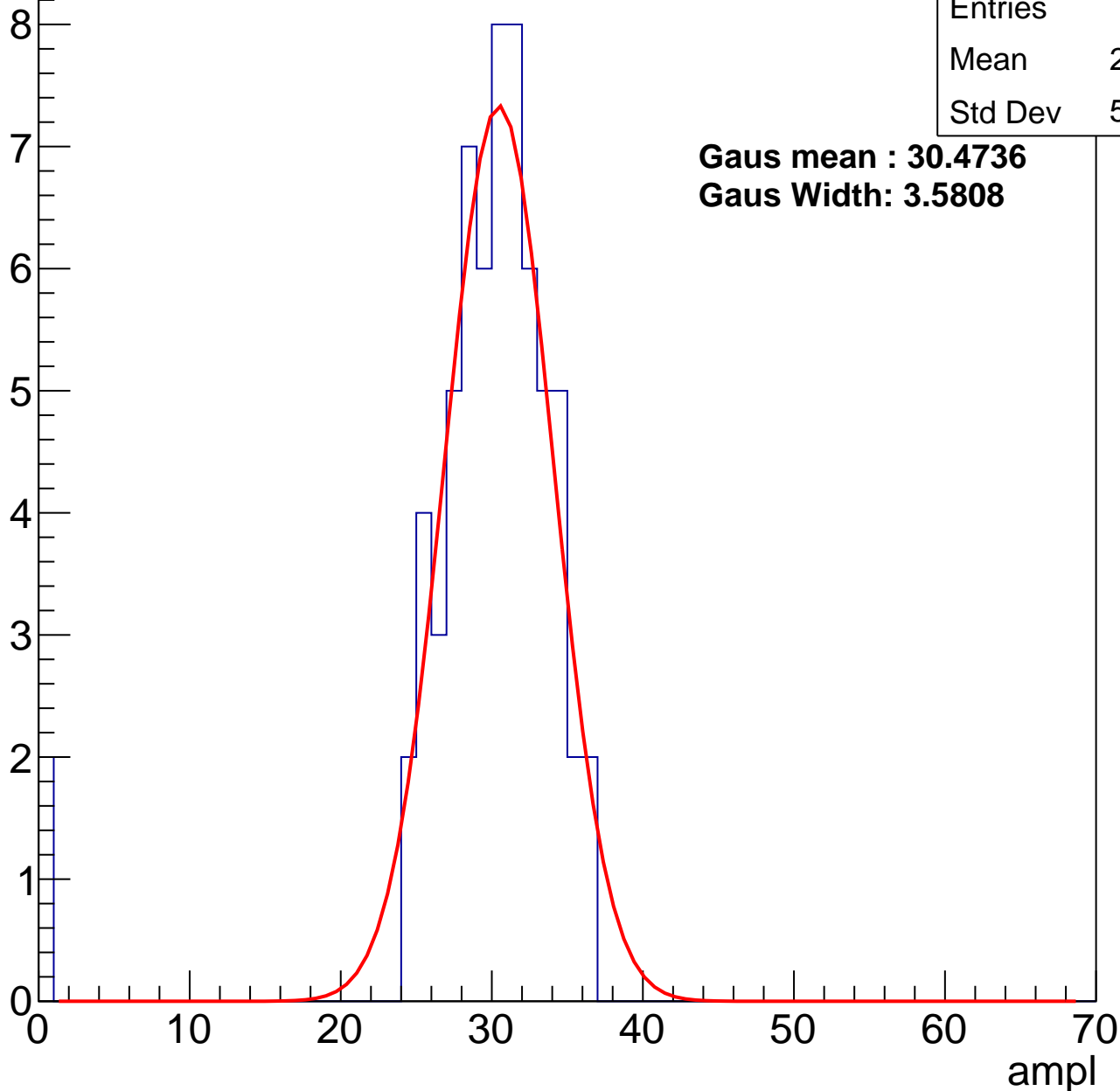
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	29.05
Std Dev	5.973

**Gaus mean : 30.4736**

**Gaus Width: 3.5808**



# B1L103S, U3-ch19, adc1

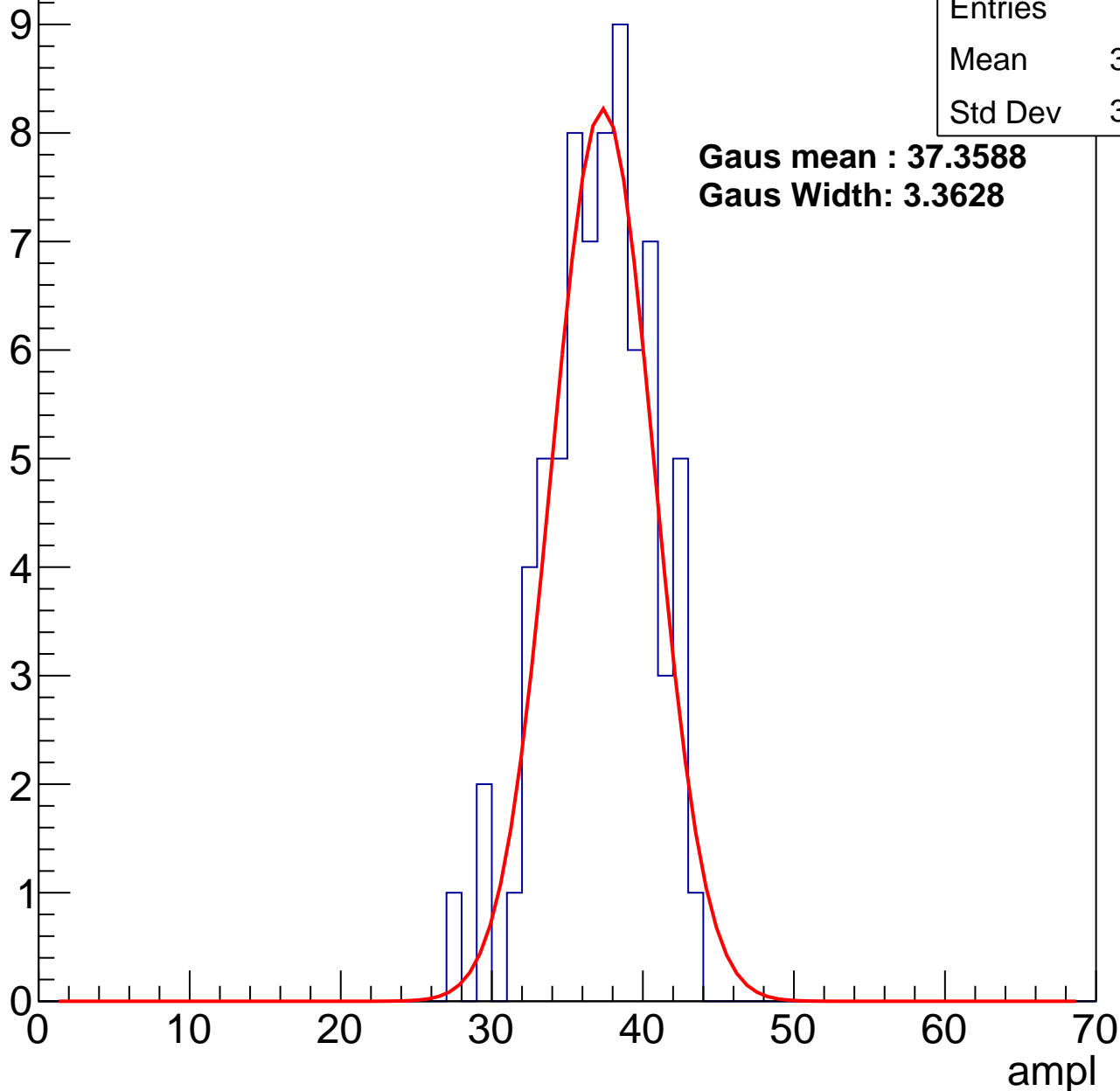
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	36.65
Std Dev	3.384

**Gaus mean : 37.3588**

**Gaus Width: 3.3628**



# B1L103S, U3-ch19, adc2

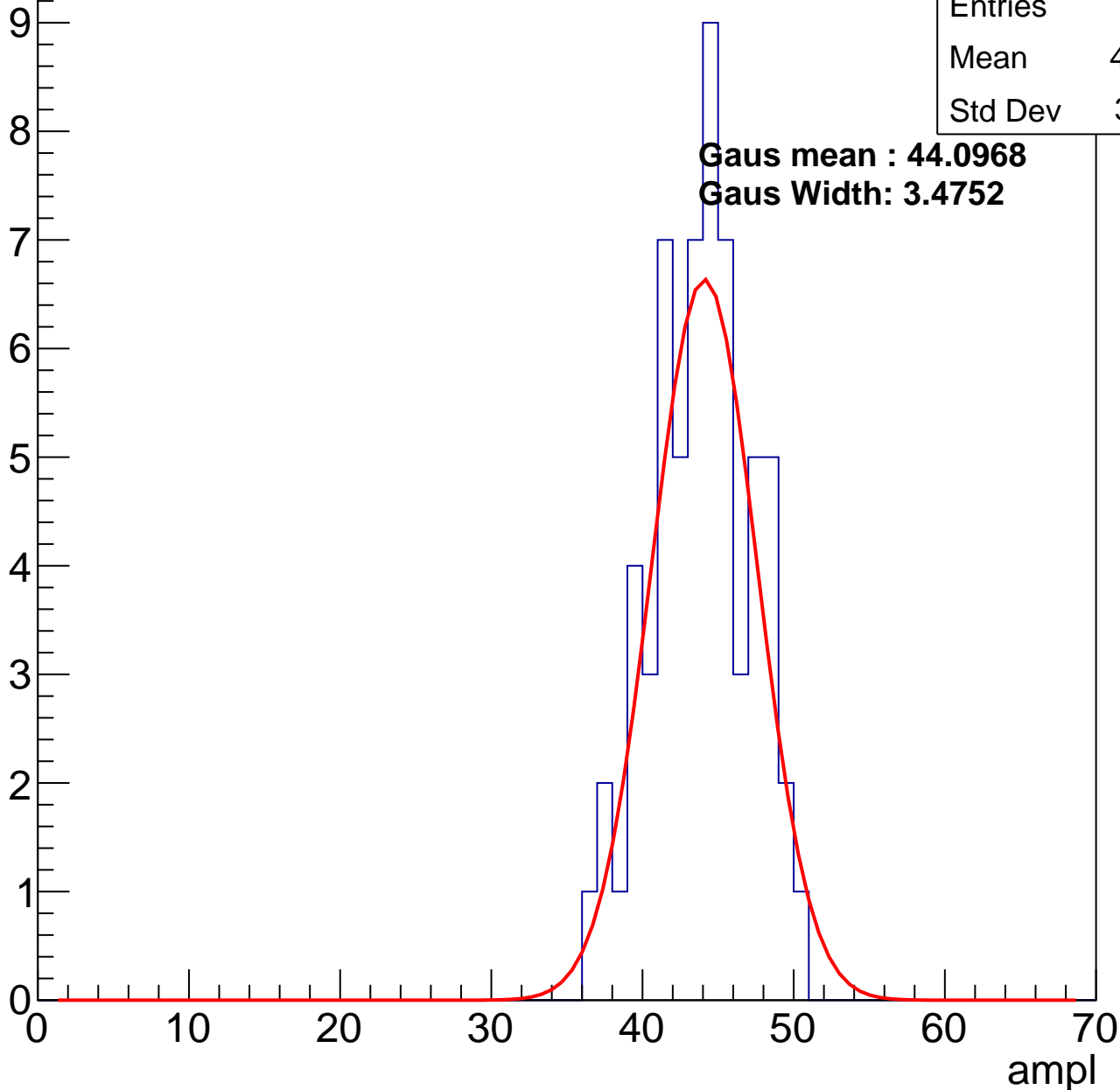
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	43.45
Std Dev	3.231

**Gaus mean : 44.0968**

**Gaus Width: 3.4752**

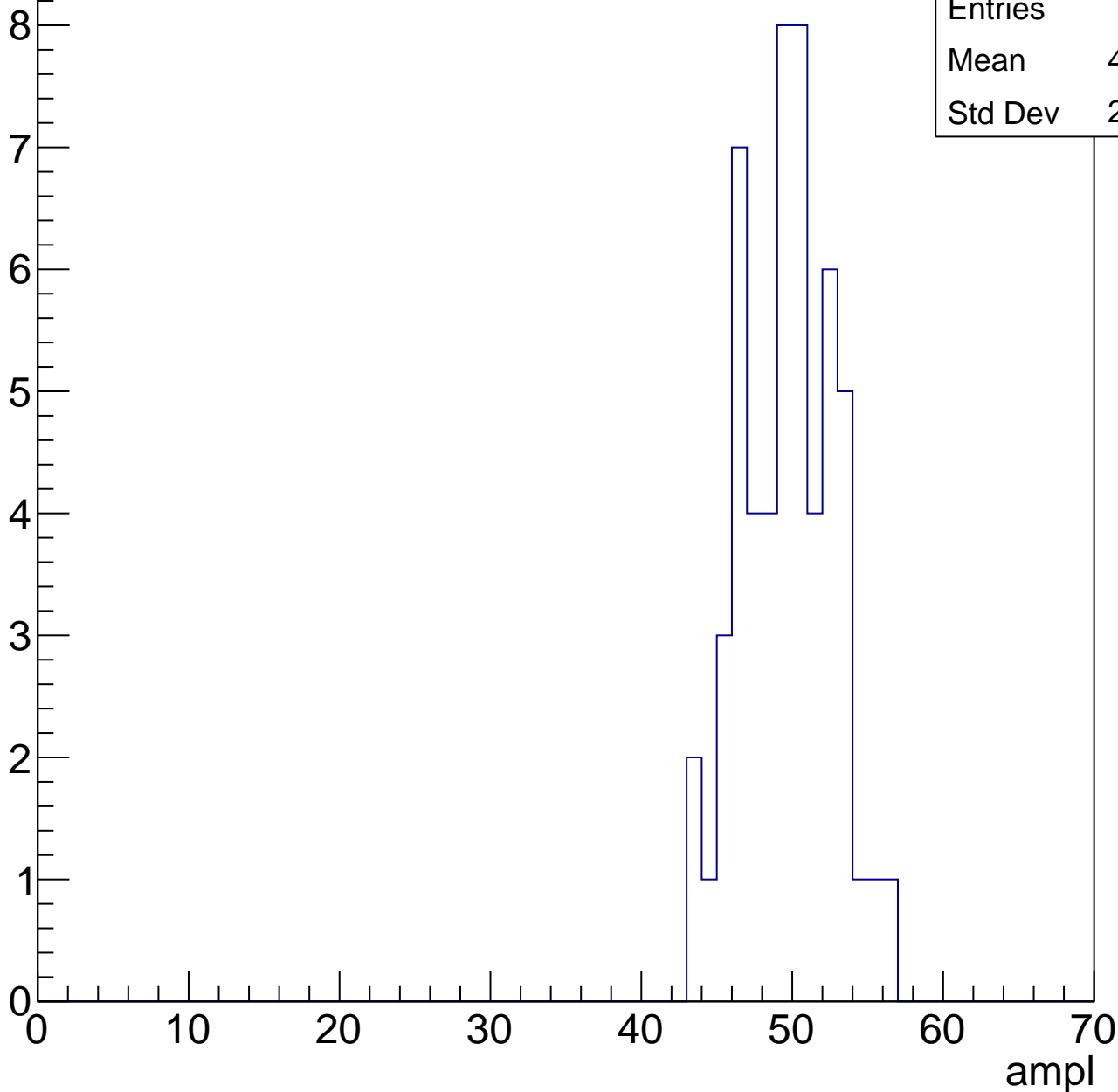


# B1L103S, U3-ch19, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	49.18
Std Dev	2.998

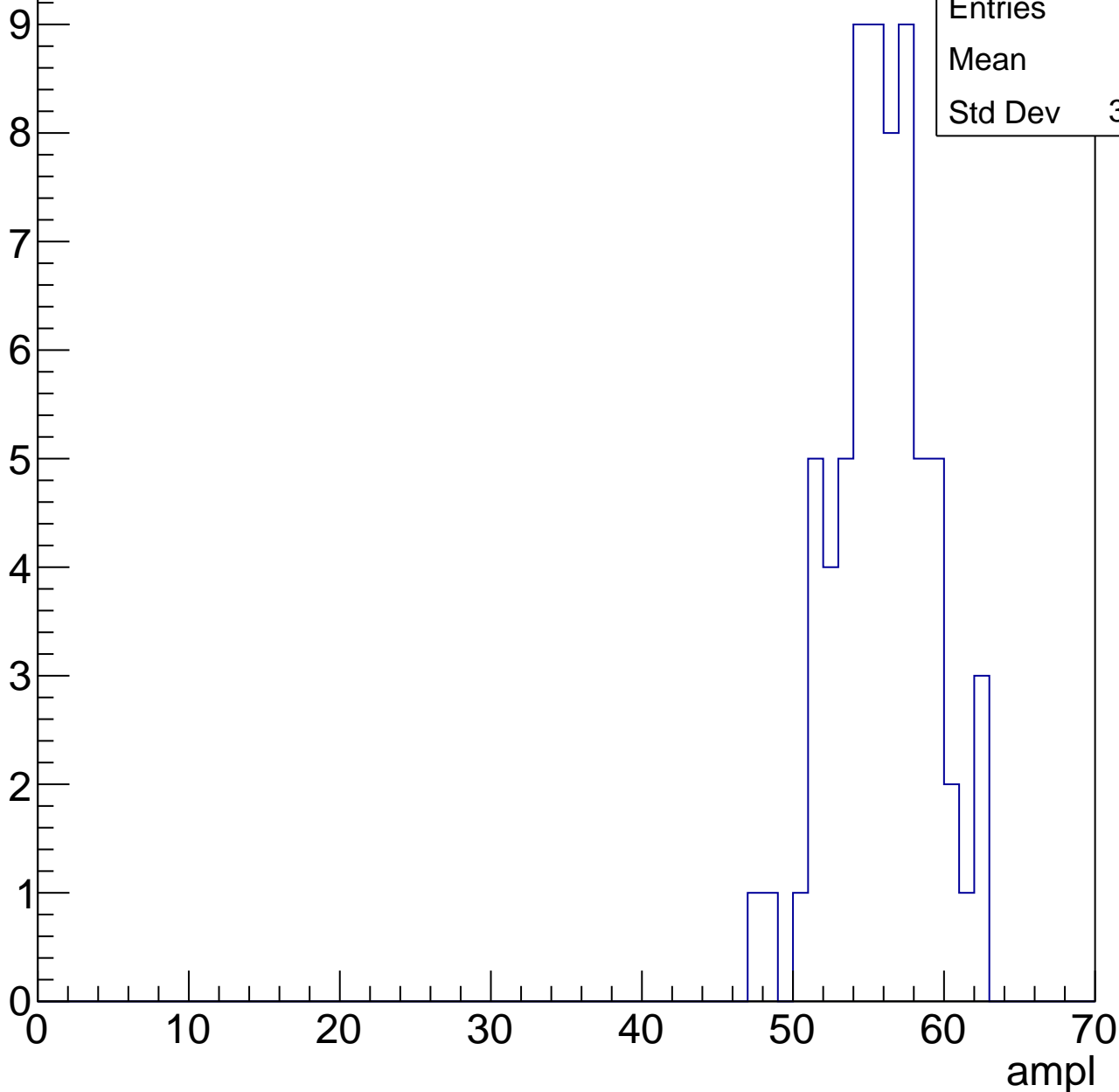


# B1L103S, U3-ch19, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	55.4
Std Dev	3.149



# B1L103S, U3-ch19, adc5

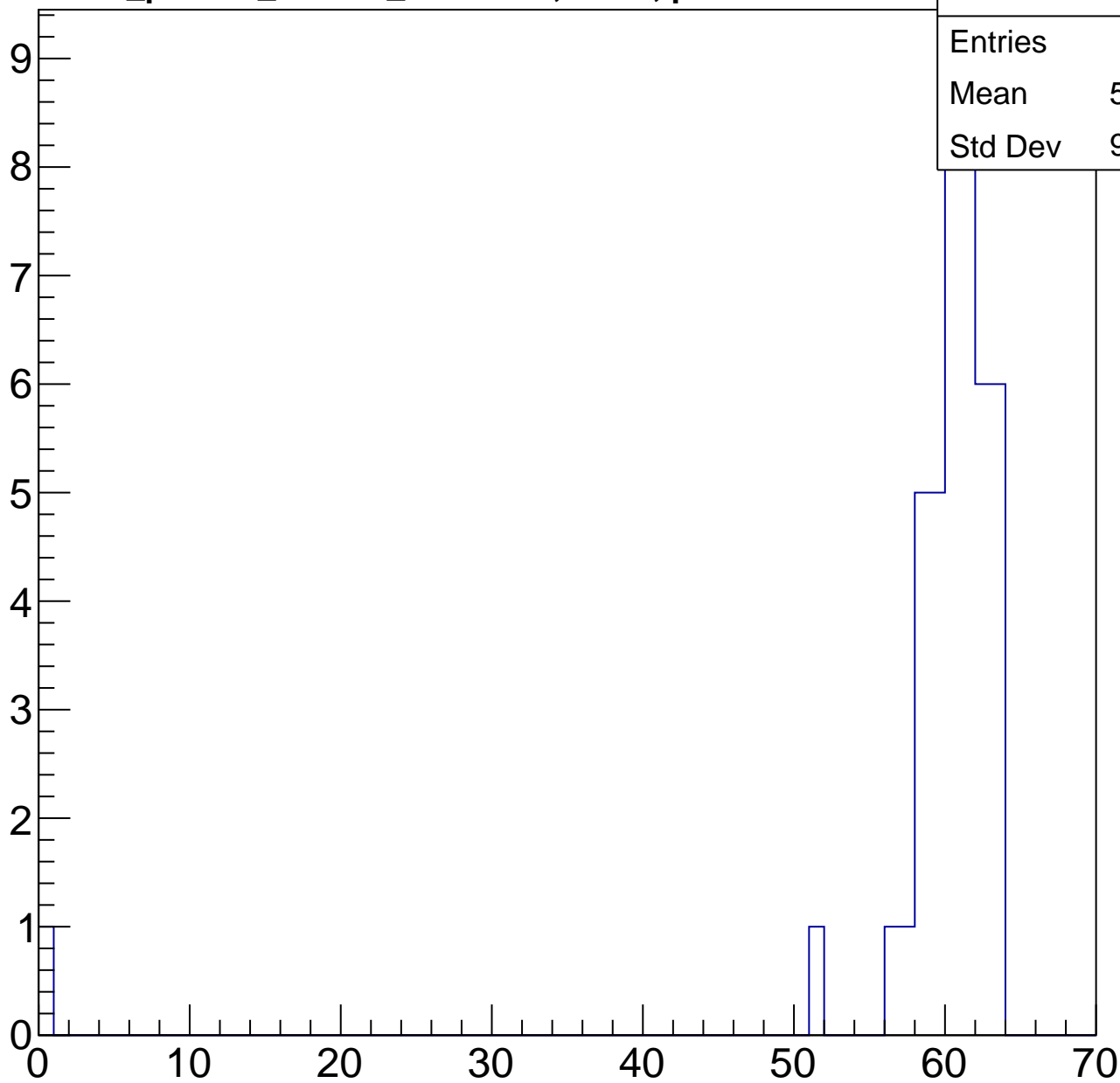
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	43
Mean	58.79
Std Dev	9.345

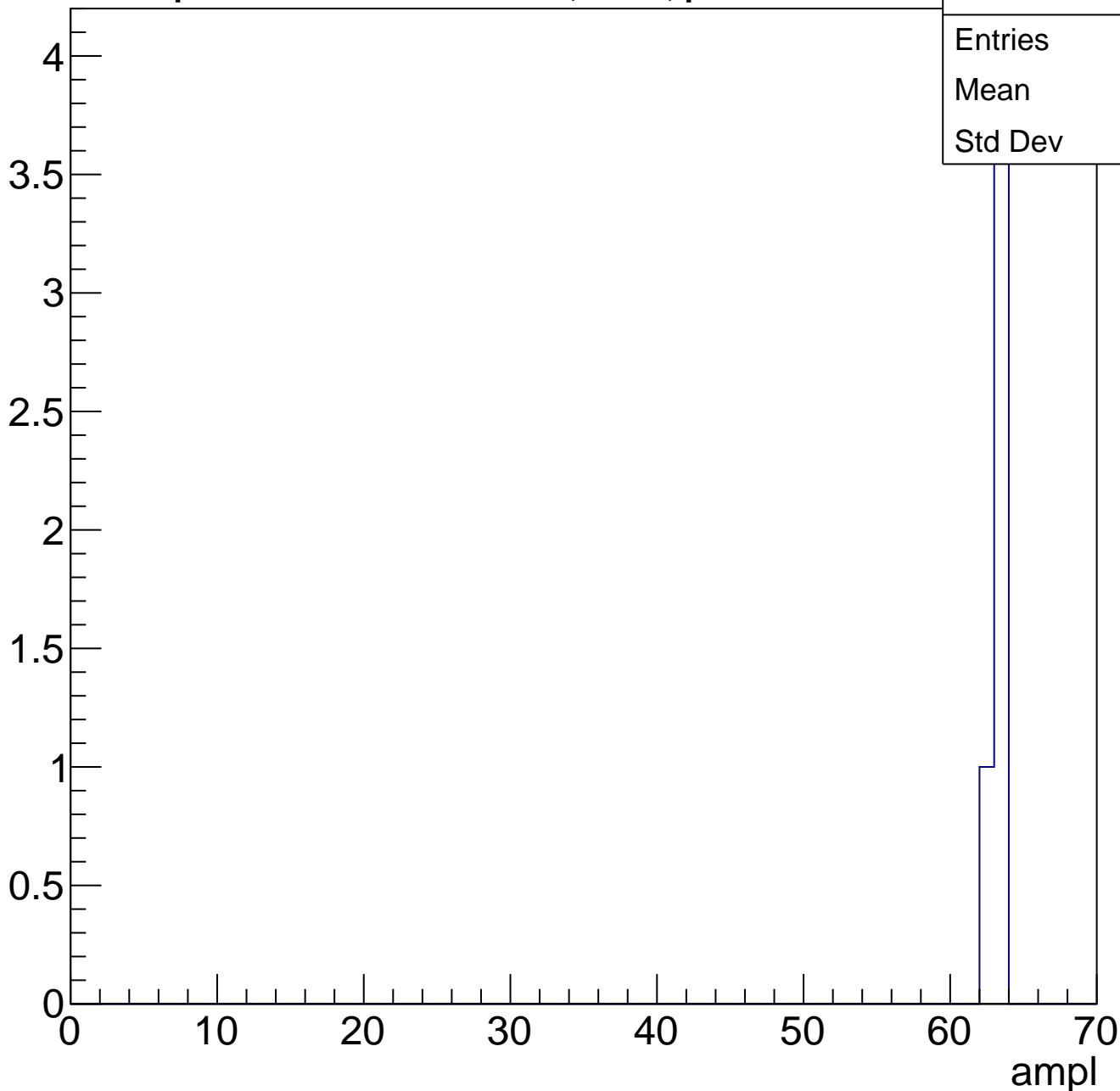
ampl



# B1L103S, U3-ch19, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

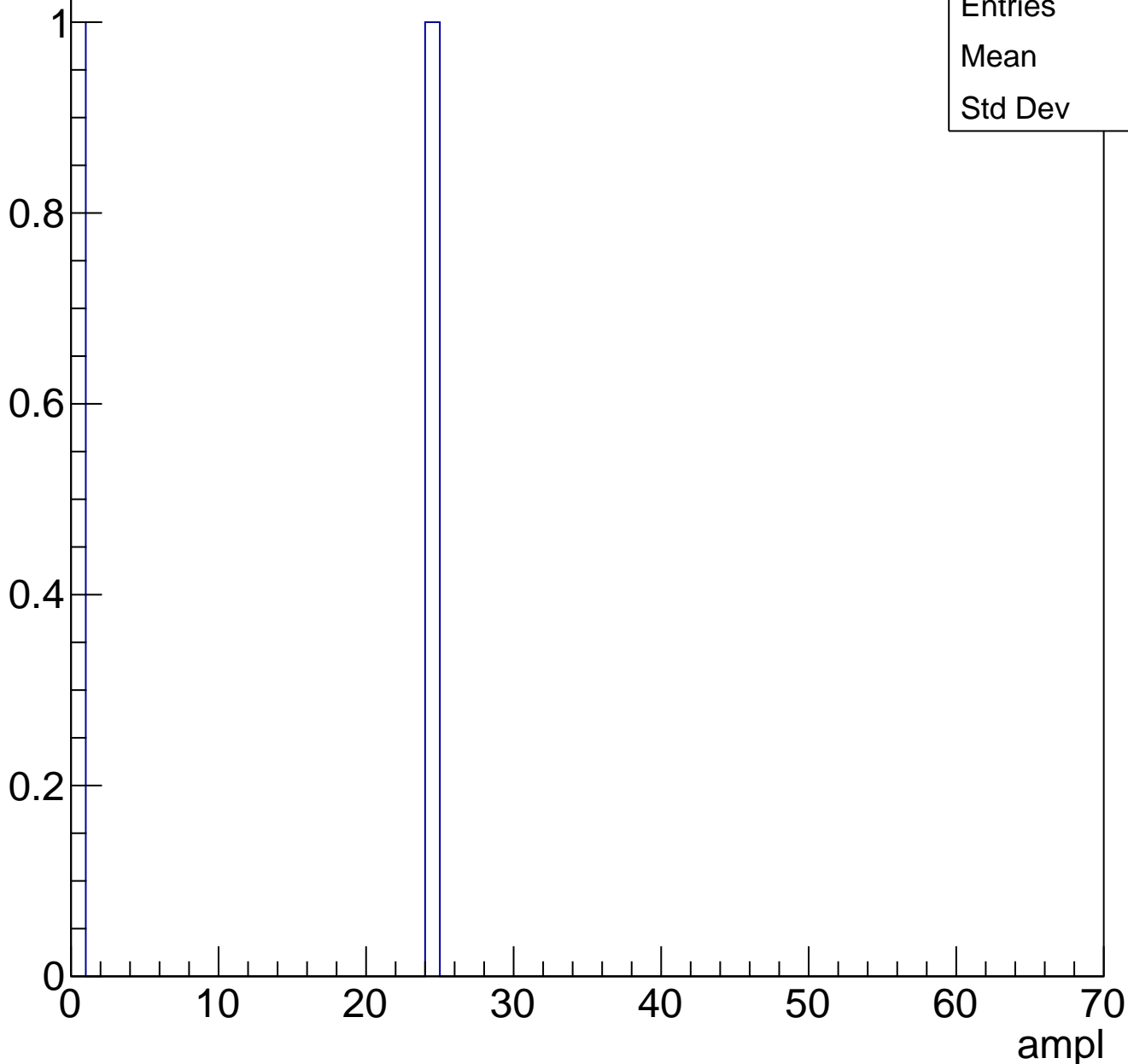




# B1L103S, U3-ch19, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch20, adc0

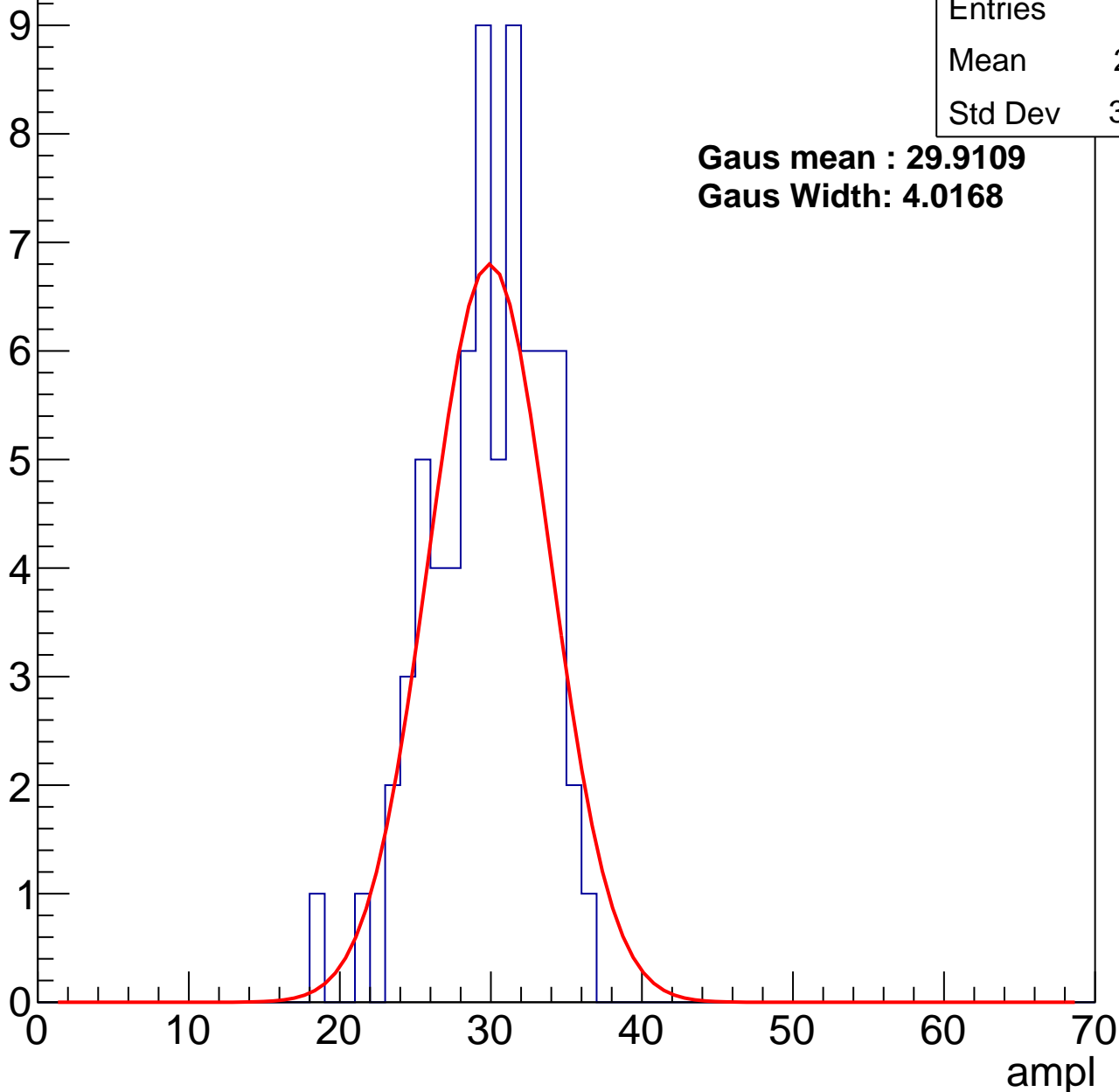
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	29.31
Std Dev	3.635

**Gaus mean : 29.9109**

**Gaus Width: 4.0168**



# B1L103S, U3-ch20, adc1

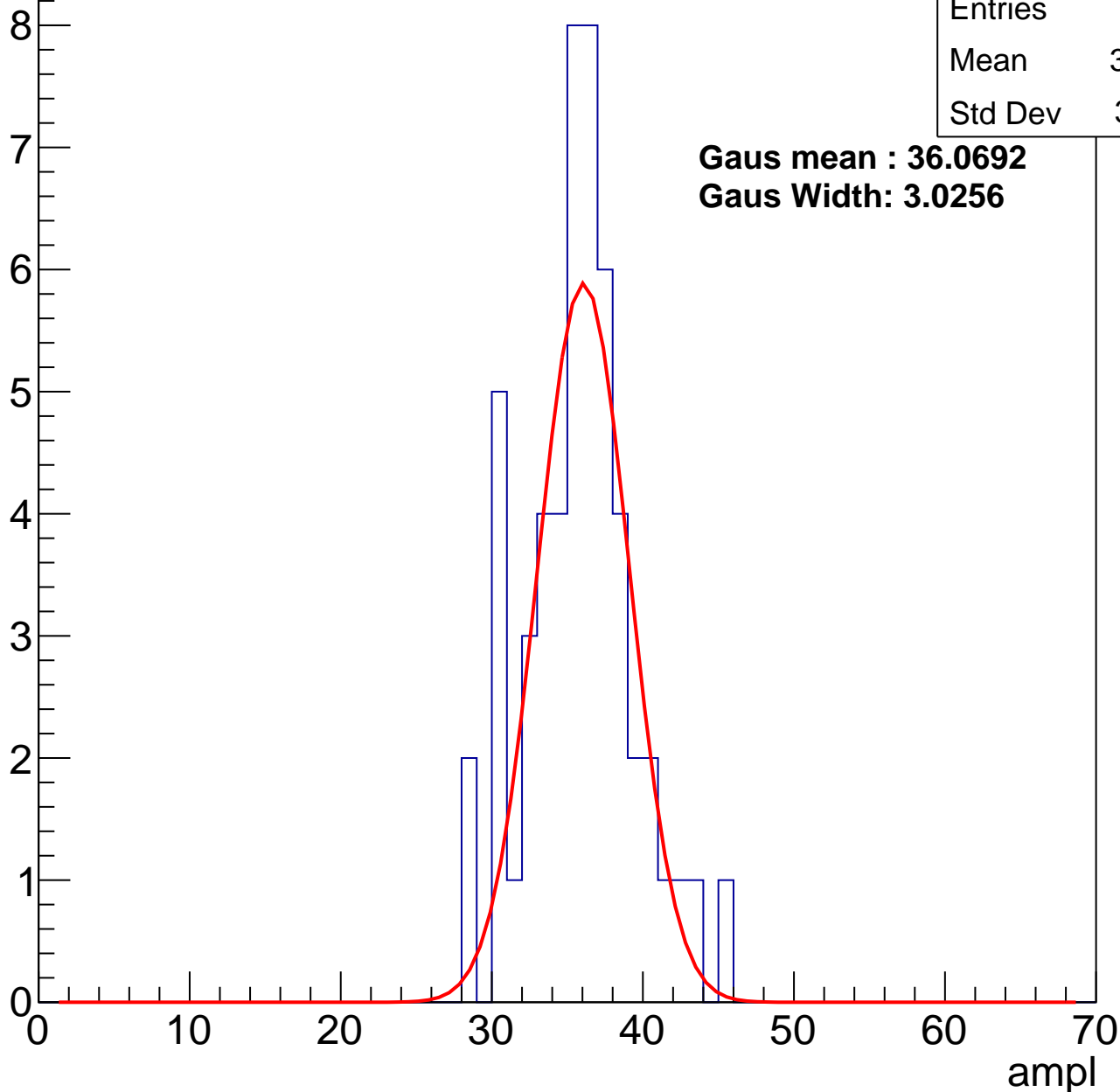
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	35.32
Std Dev	3.581

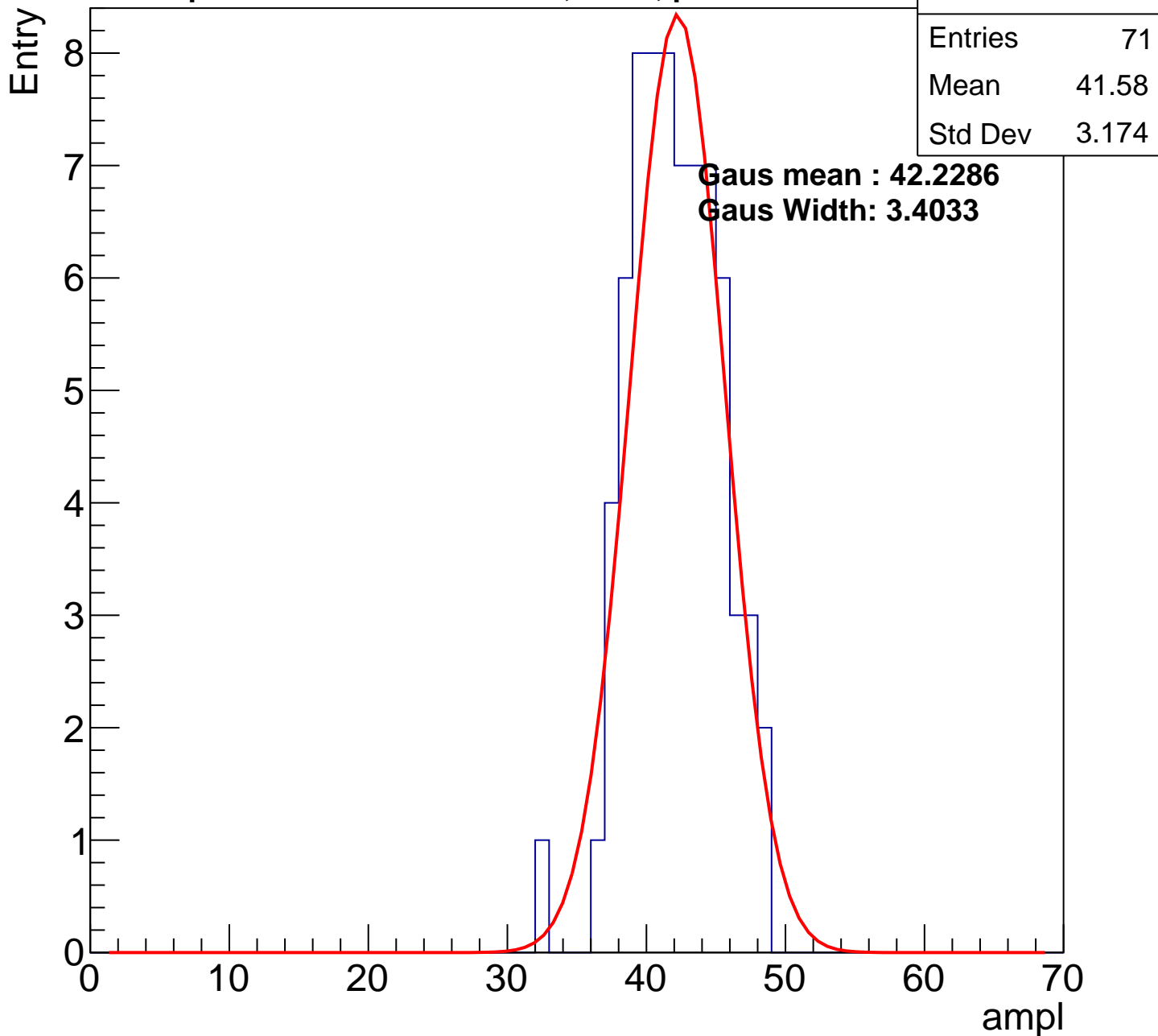
**Gaus mean : 36.0692**

**Gaus Width: 3.0256**



# B1L103S, U3-ch20, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

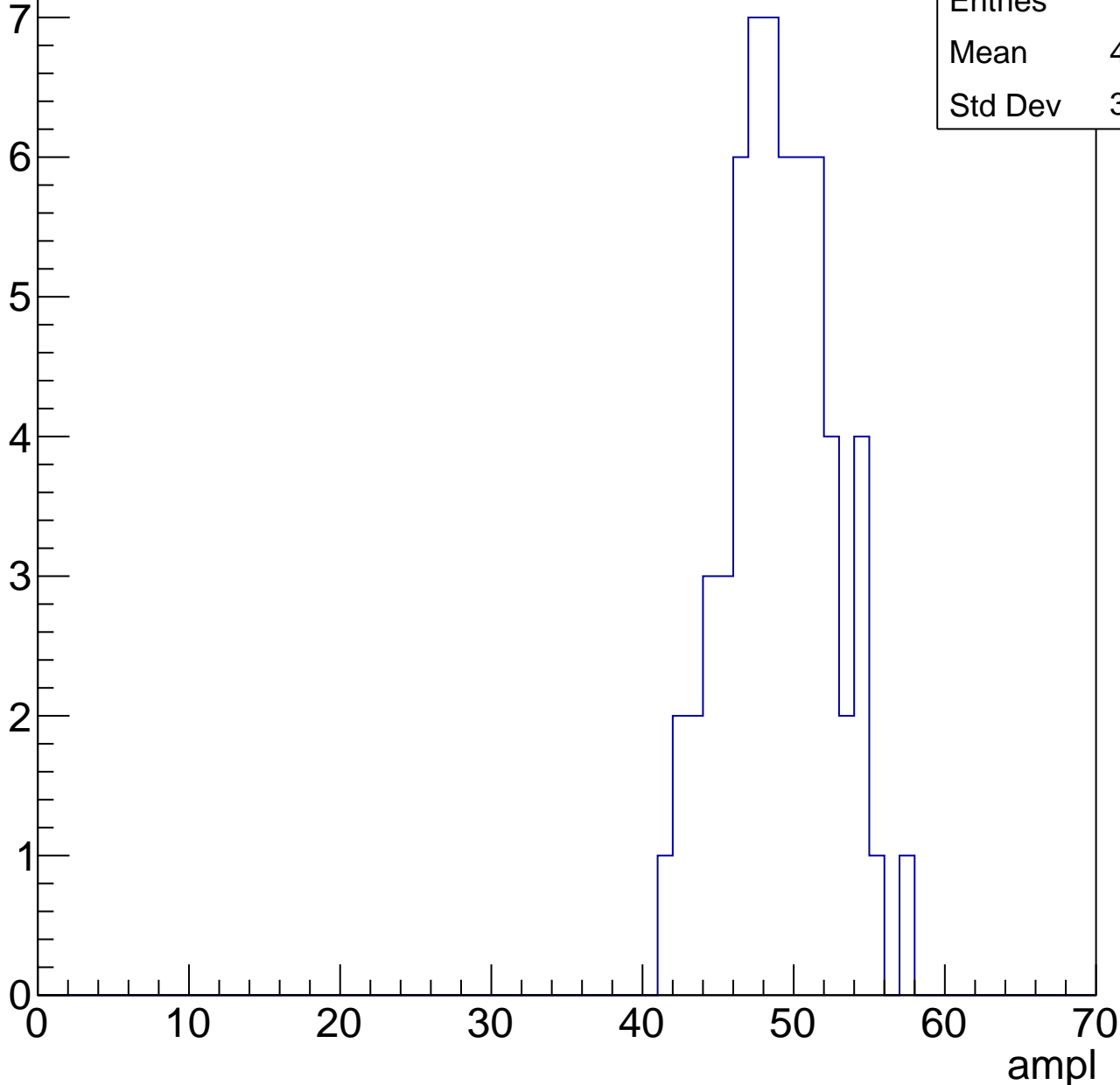


# B1L103S, U3-ch20, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

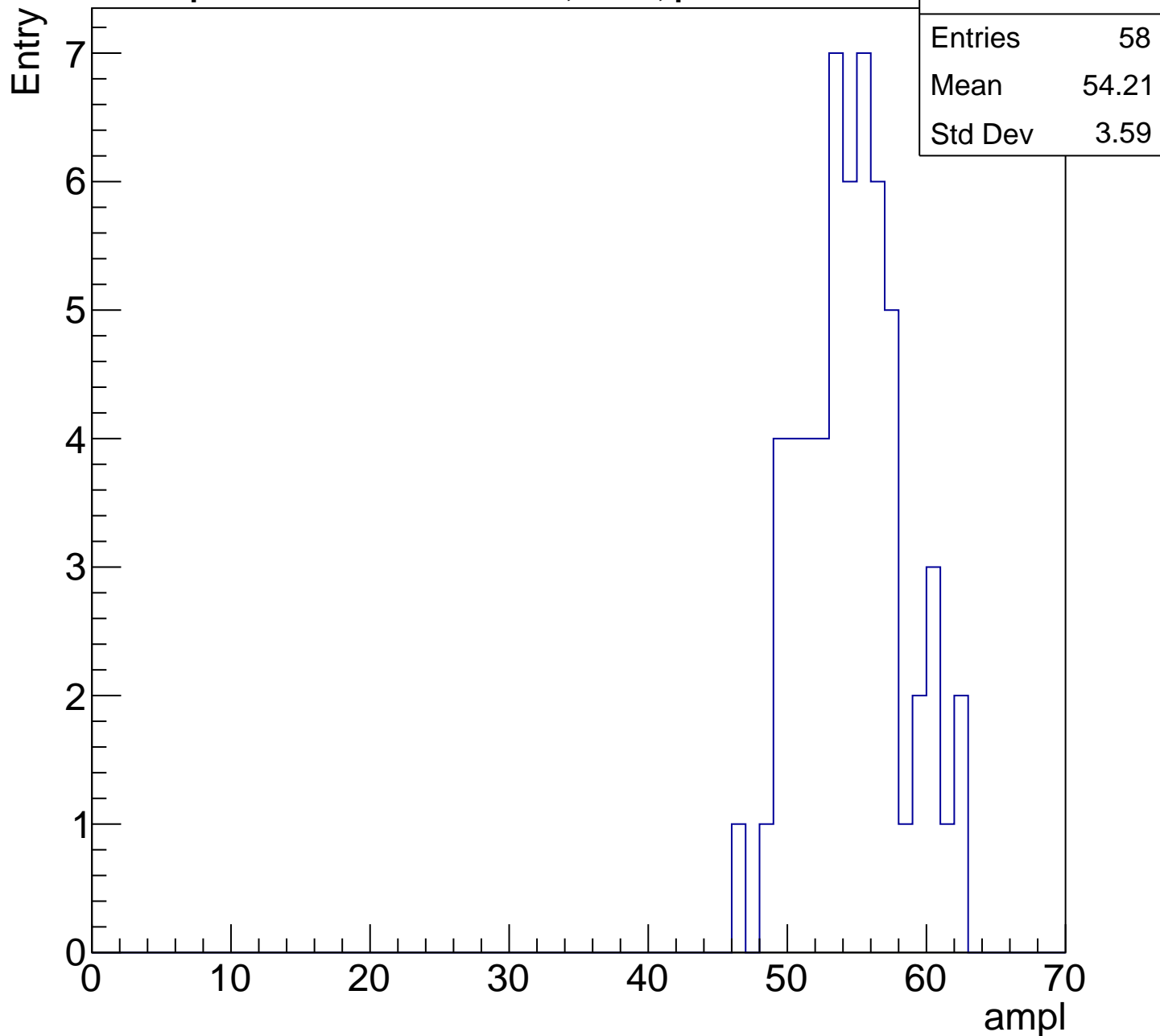
Entry

Entries	61
Mean	48.54
Std Dev	3.462



# B1L103S, U3-ch20, adc4

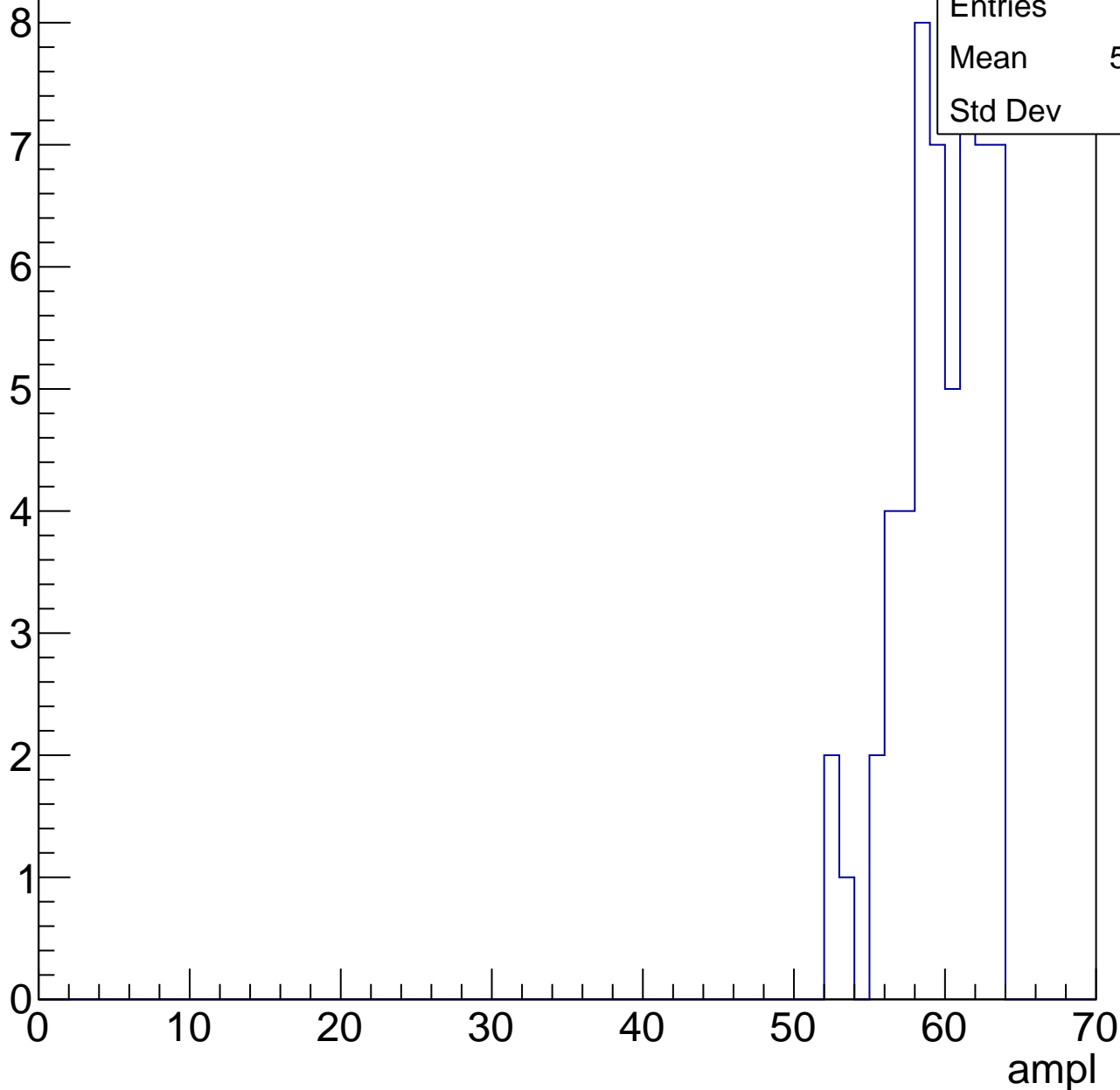
calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U3-ch20, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

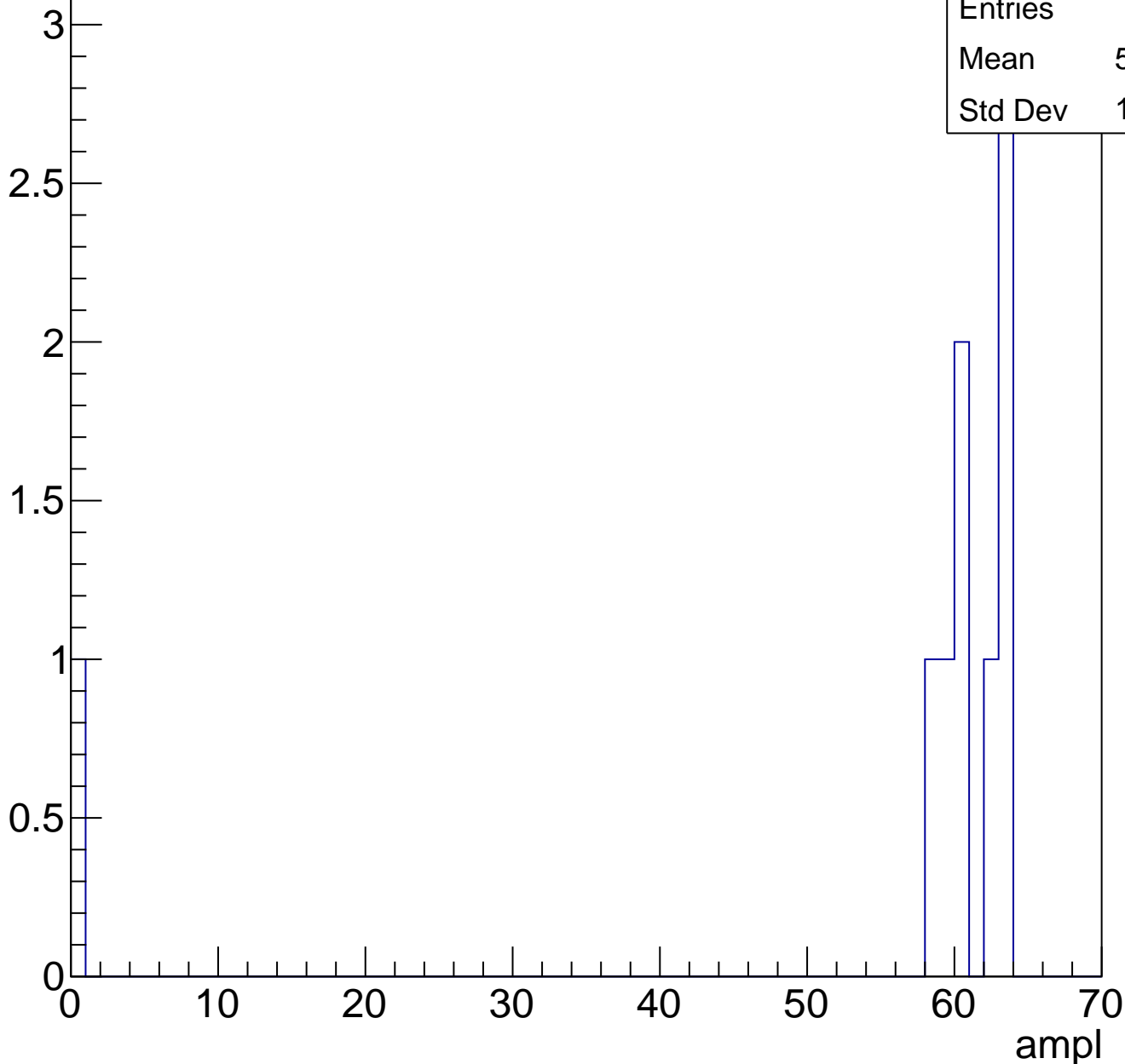


Entries	55
Mean	59.25
Std Dev	2.81

# B1L103S, U3-ch20, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

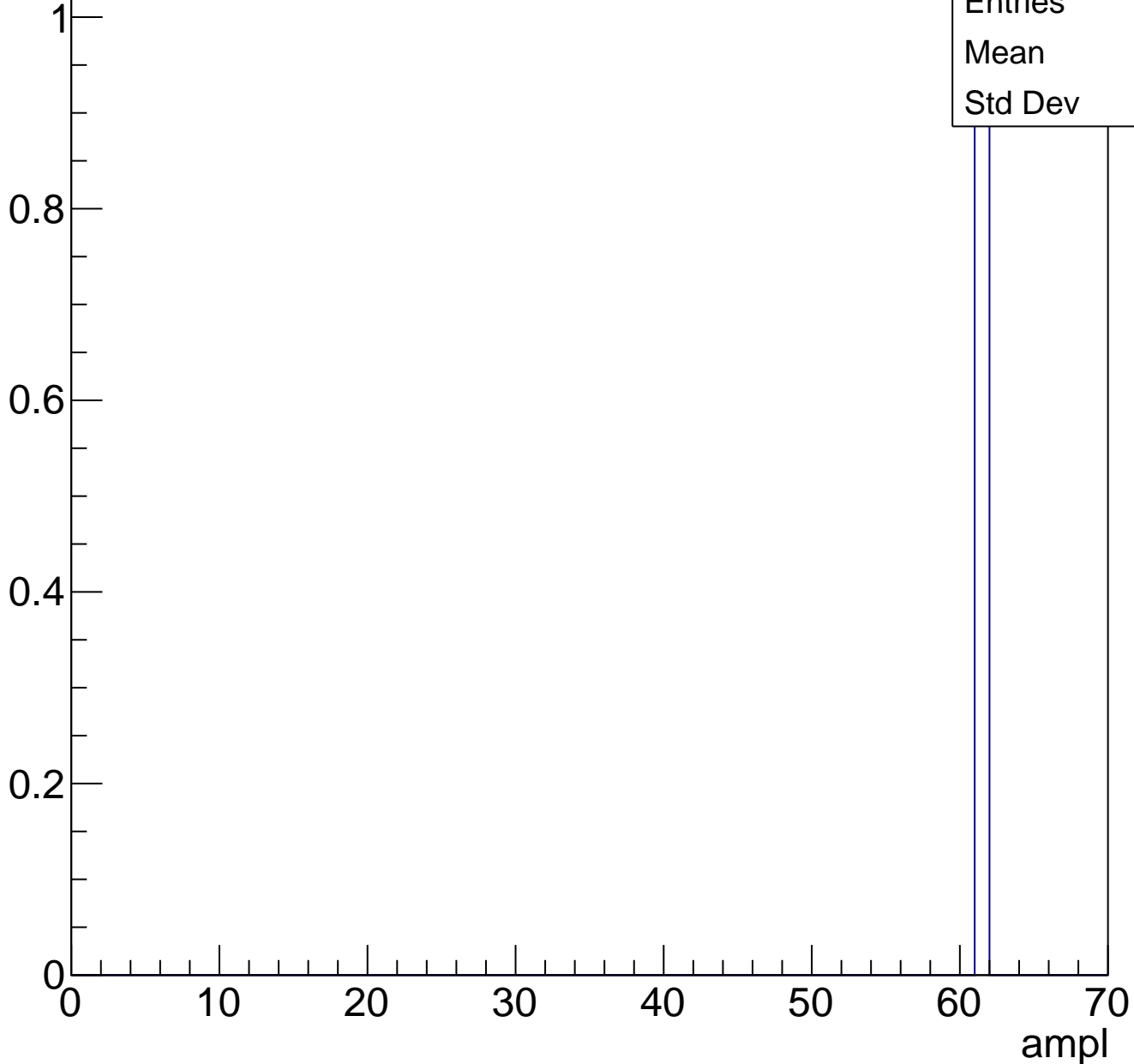




# B1L103S, U3-ch20, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch21, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	69
Mean	29.87
Std Dev	4.656

**Gaus mean : 30.9844**

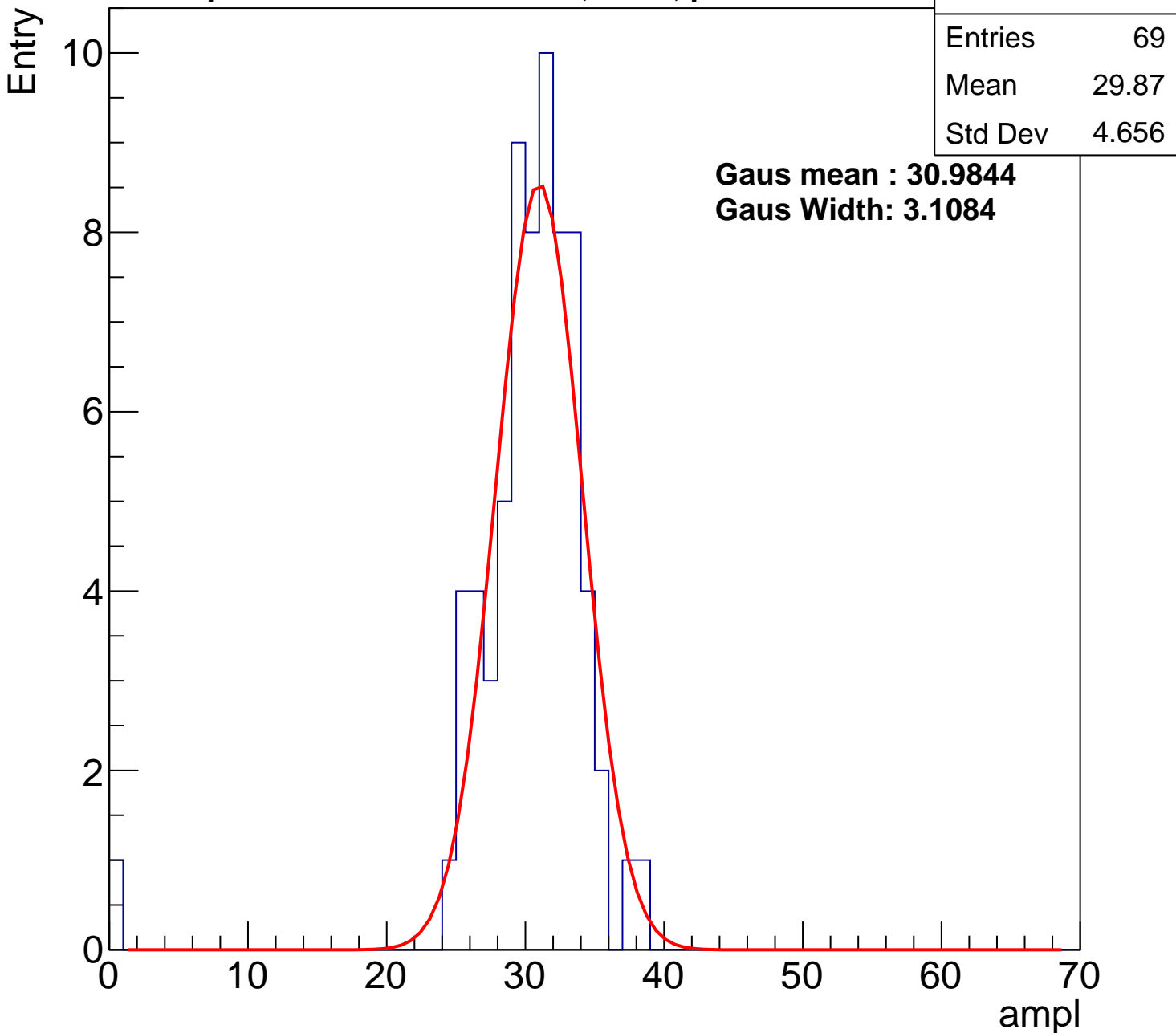
**Gaus Width: 3.1084**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U3-ch21, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	60
Mean	37.37
Std Dev	2.483

**Gaus mean : 37.9591**

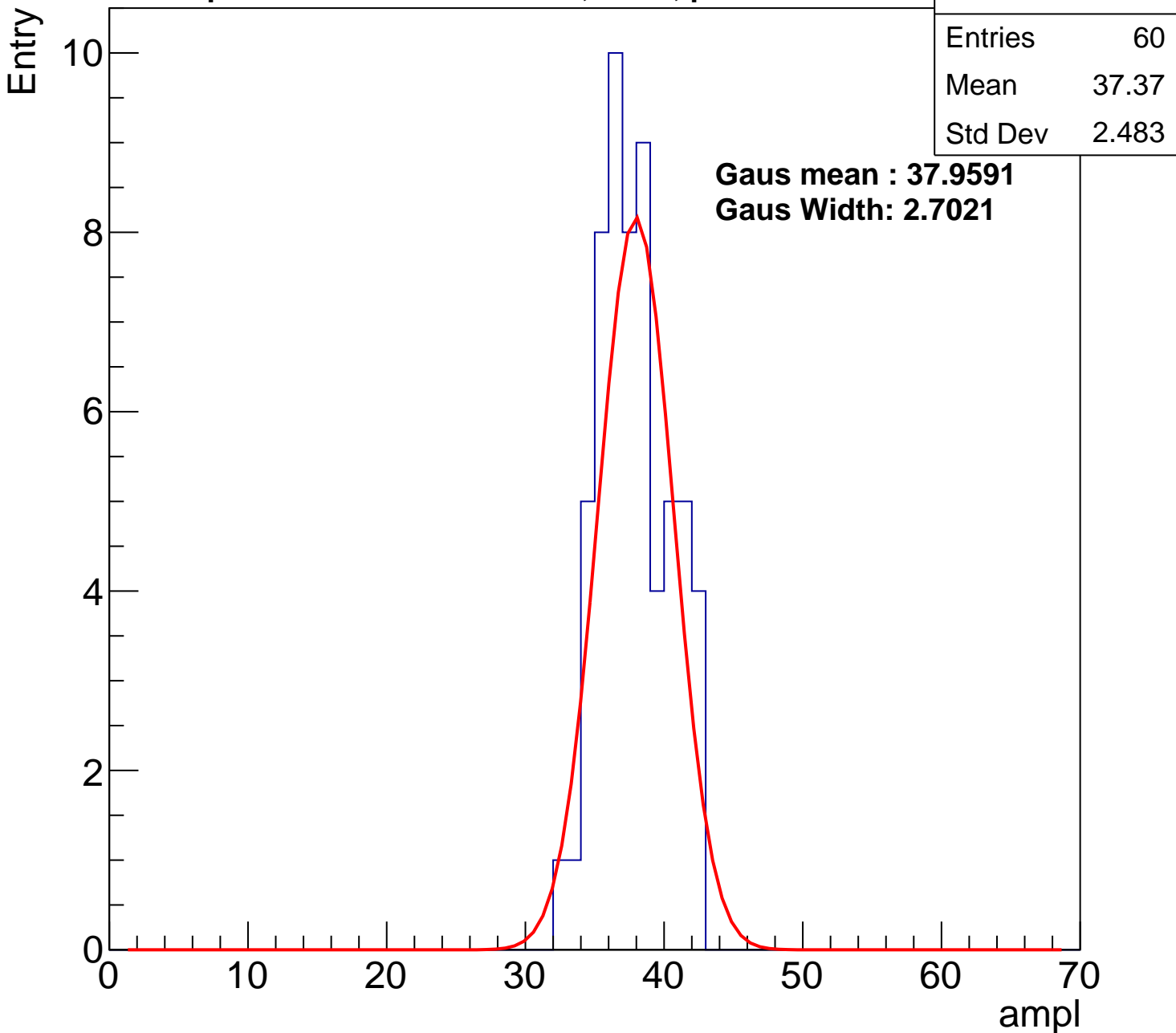
**Gaus Width: 2.7021**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L103S, U3-ch21, adc2

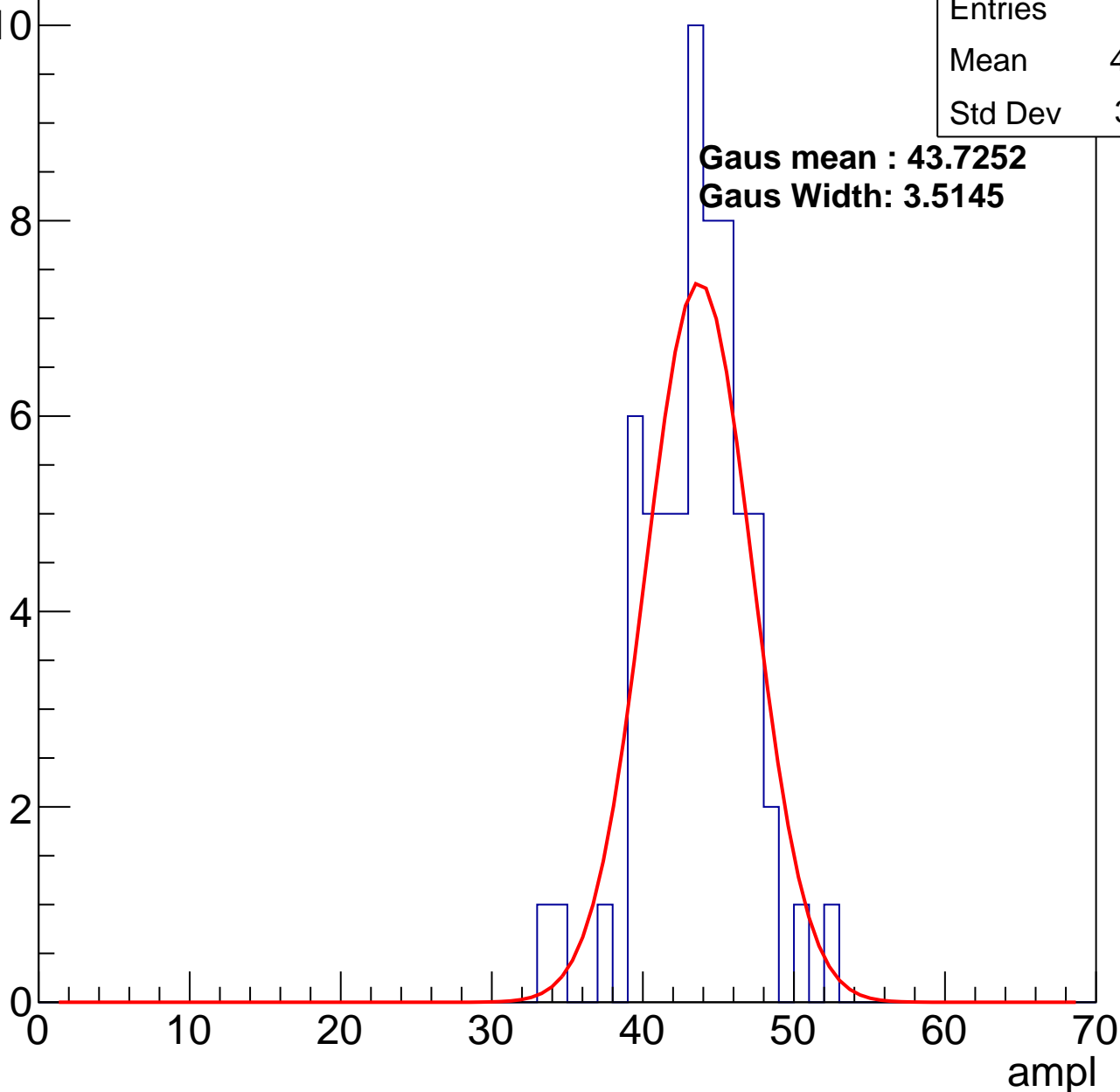
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	43.09
Std Dev	3.371

**Gaus mean : 43.7252**

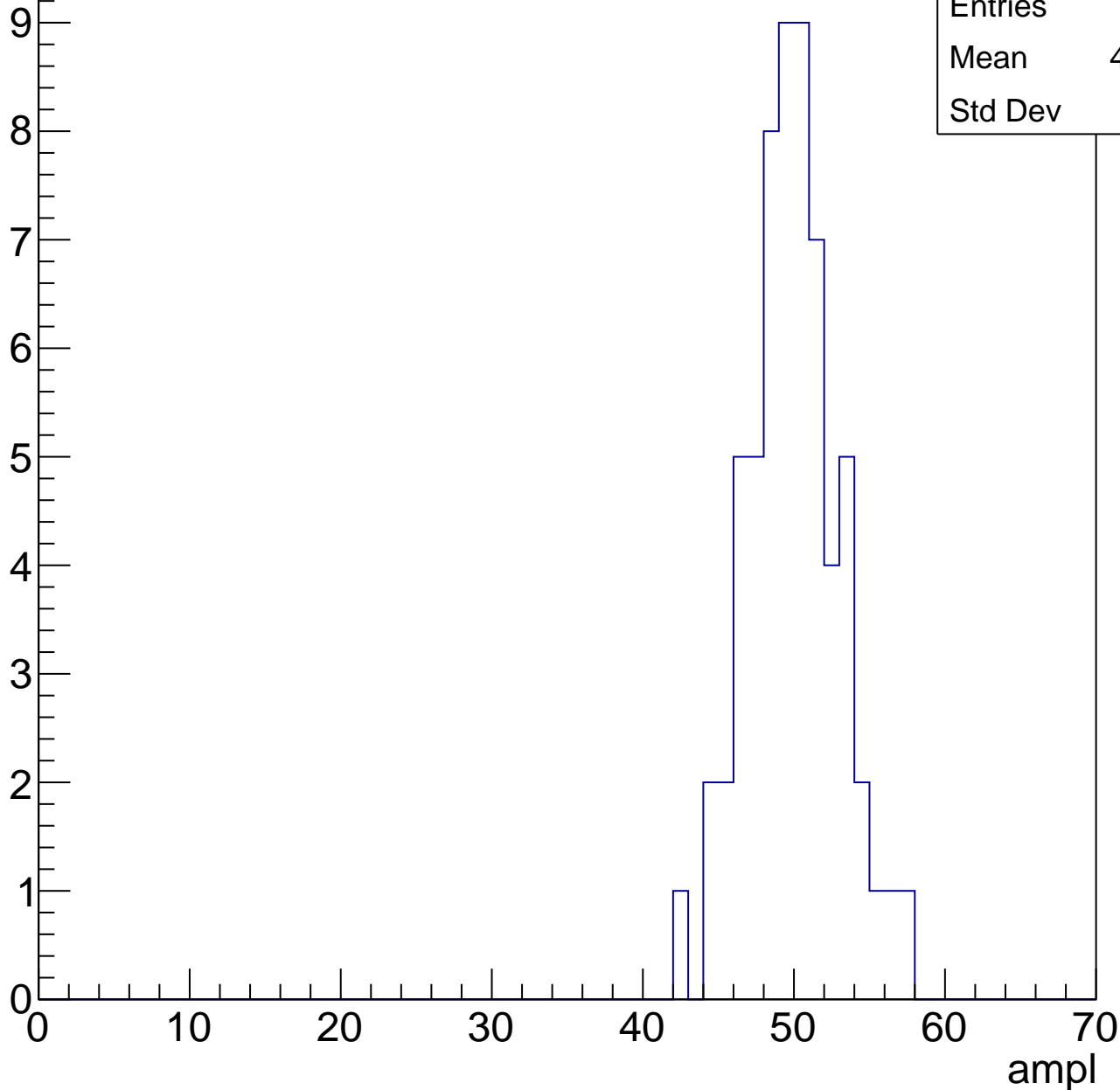
**Gaus Width: 3.5145**



# B1L103S, U3-ch21, adc3

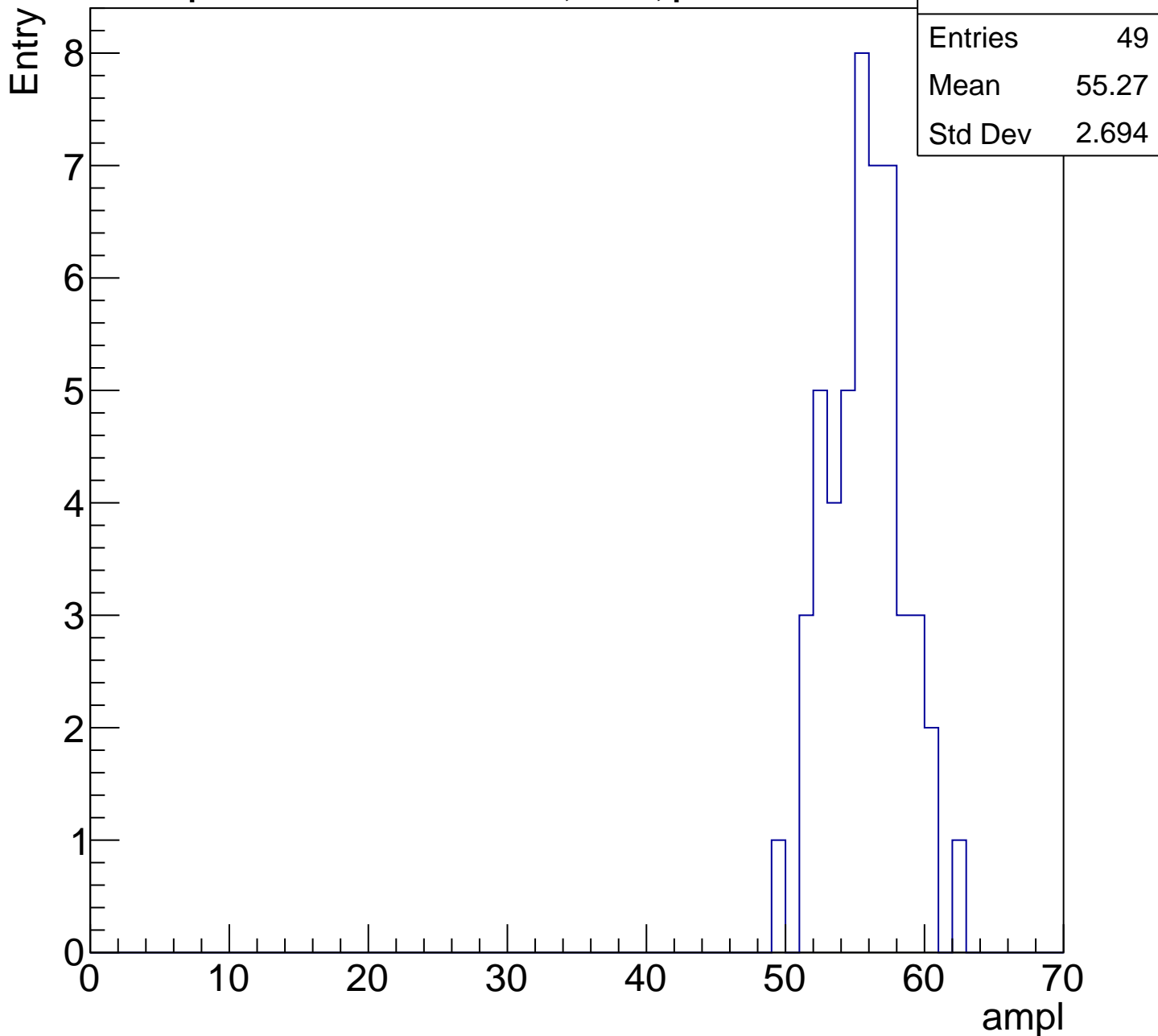
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch21, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

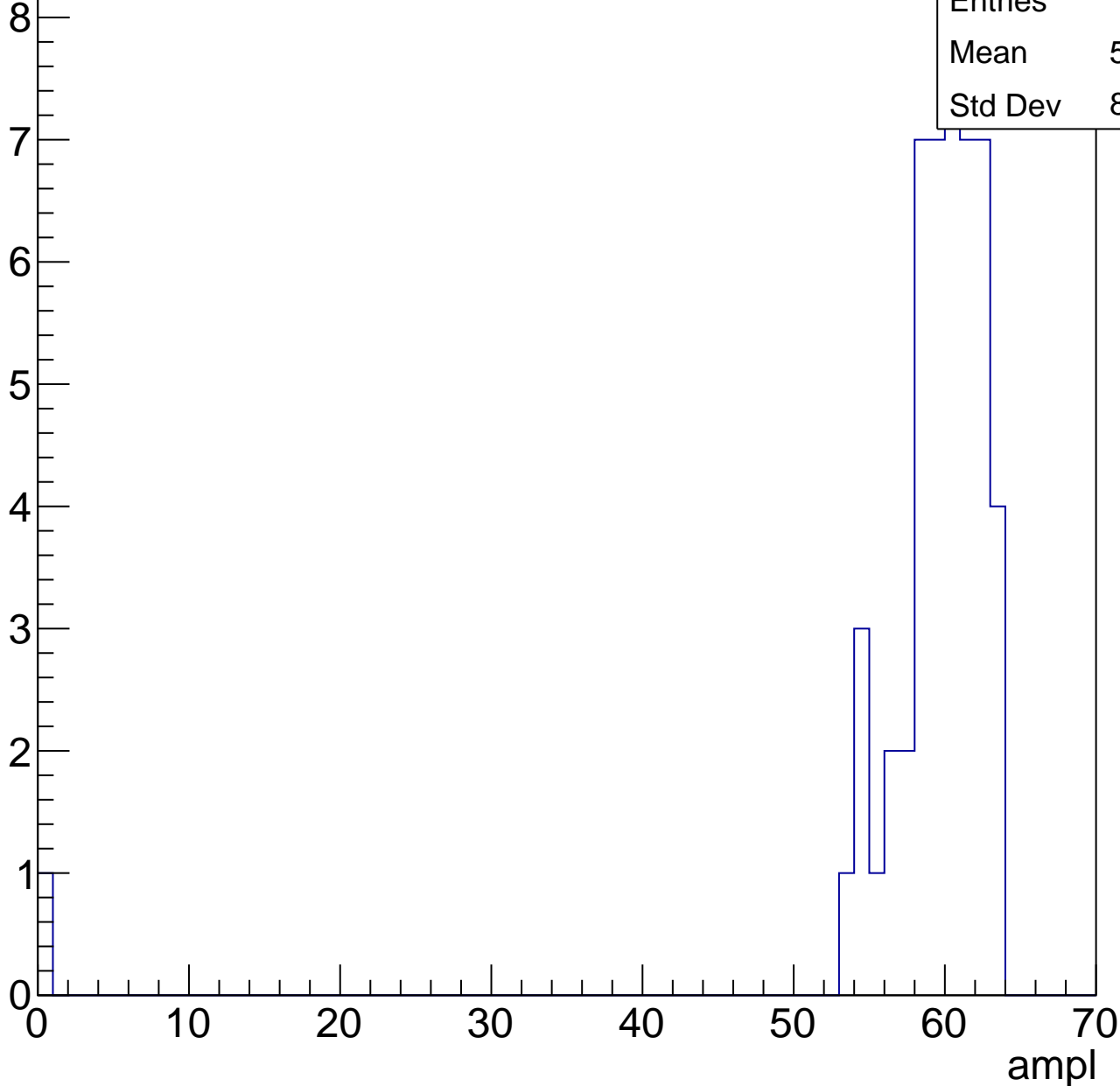


# B1L103S, U3-ch21, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	58.16
Std Dev	8.682

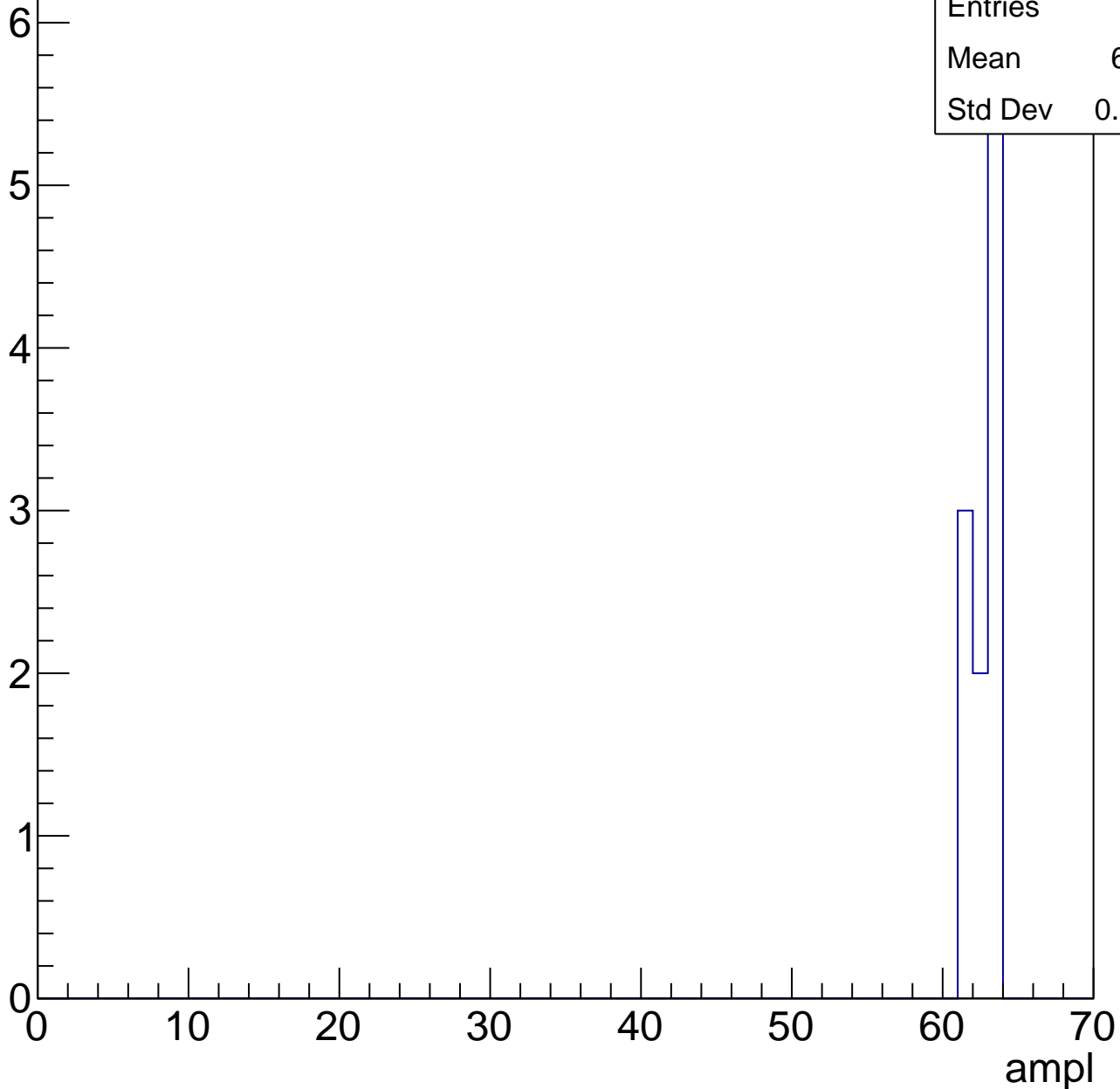


# B1L103S, U3-ch21, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	11
Mean	62.27
Std Dev	0.8624





# B1L103S, U3-ch21, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch22, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	93
Mean	29.03
Std Dev	4.246

**Gaus mean : 29.8326**

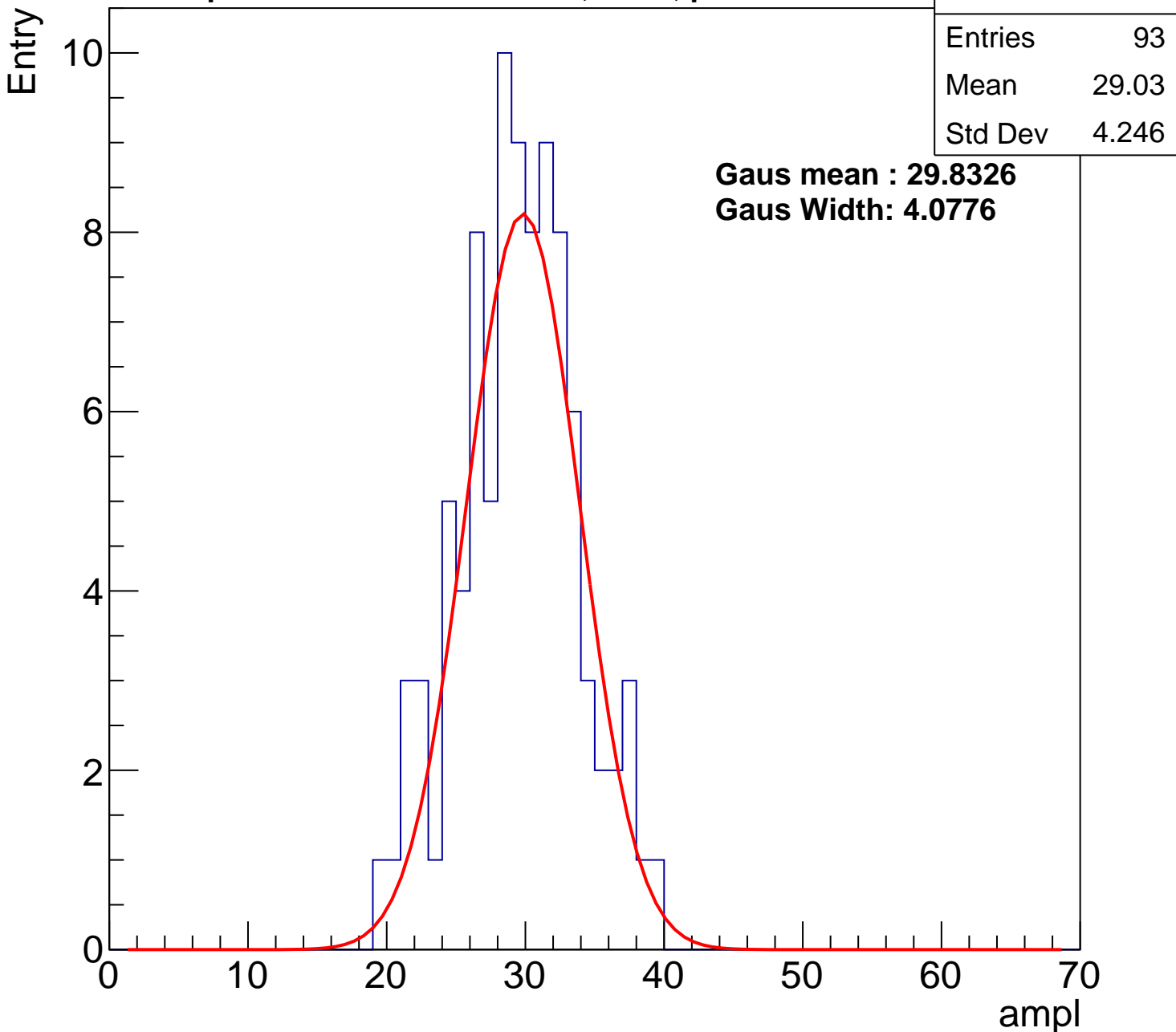
**Gaus Width: 4.0776**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U3-ch22, adc1

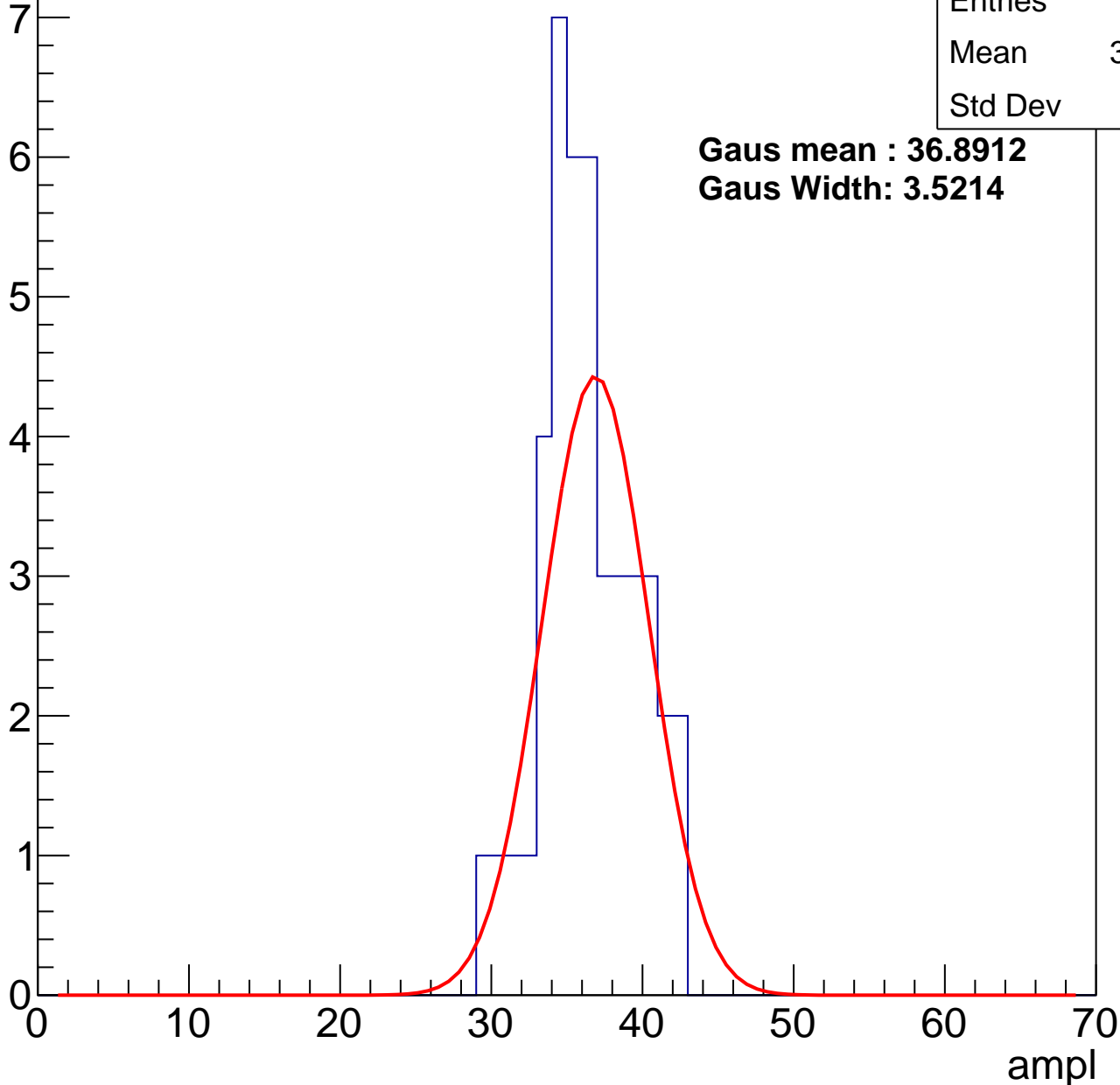
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	43
Mean	35.95
Std Dev	3.08

**Gaus mean : 36.8912**

**Gaus Width: 3.5214**



# B1L103S, U3-ch22, adc2

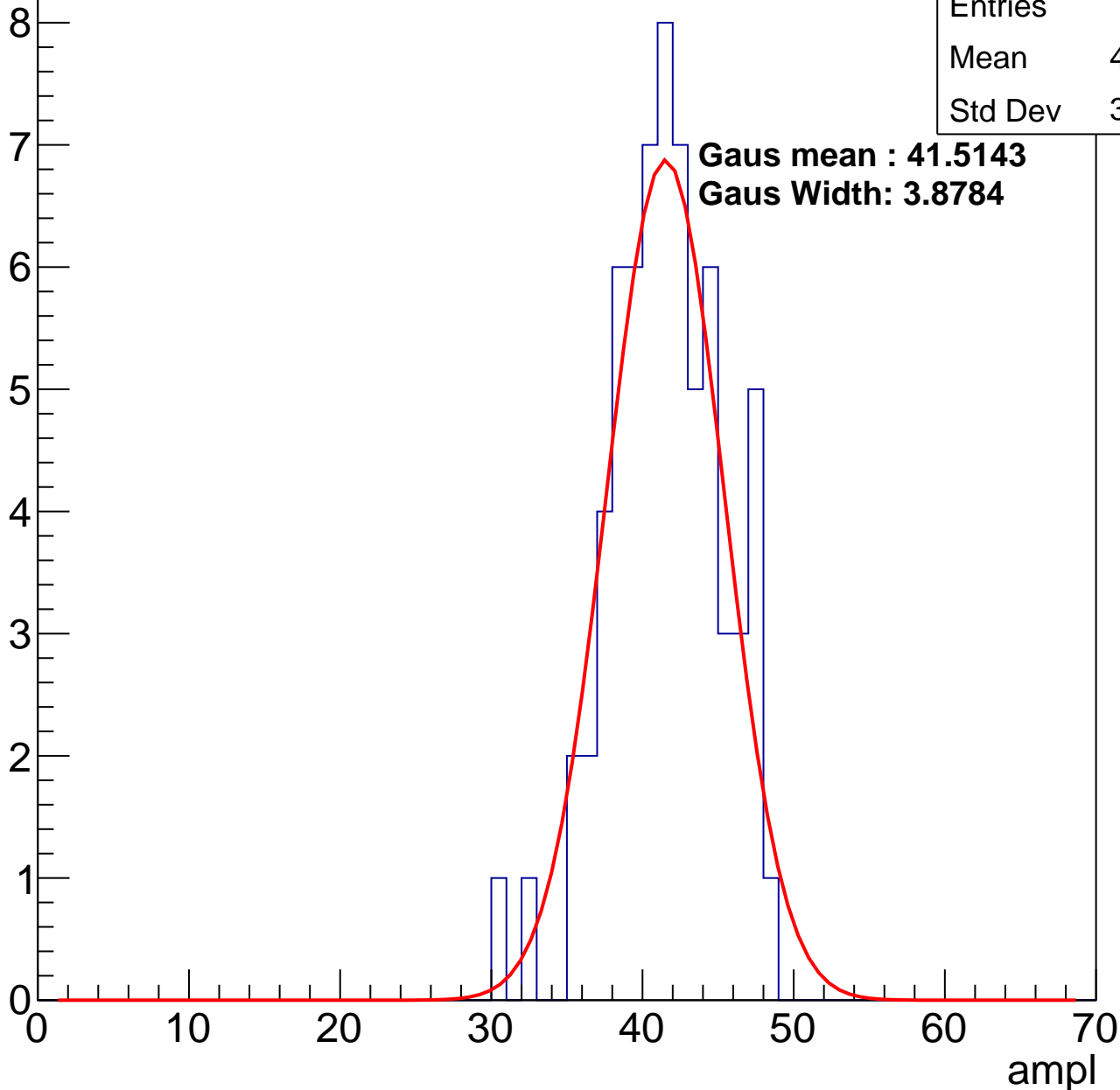
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	41.06
Std Dev	3.677

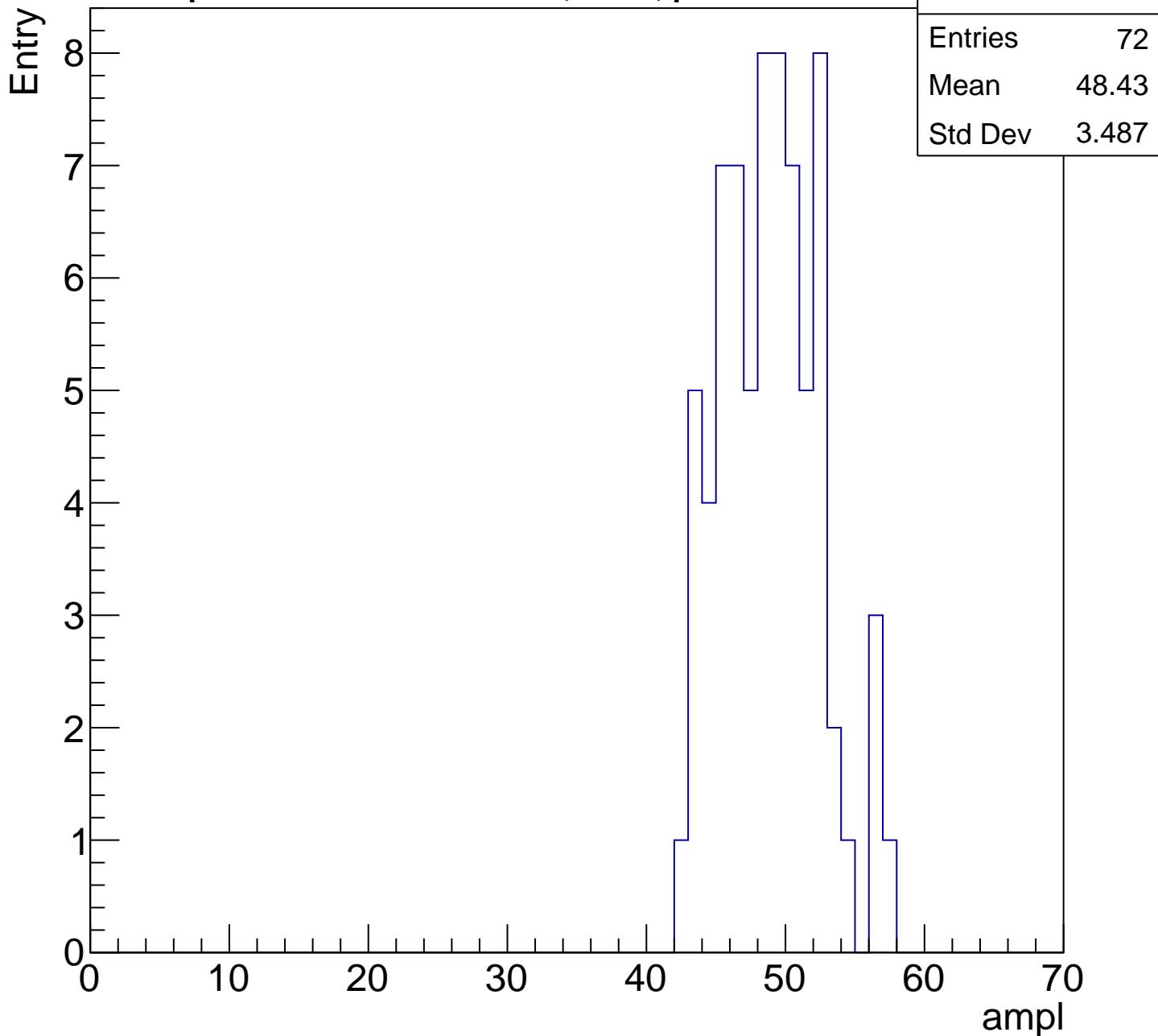
**Gaus mean : 41.5143**

**Gaus Width: 3.8784**



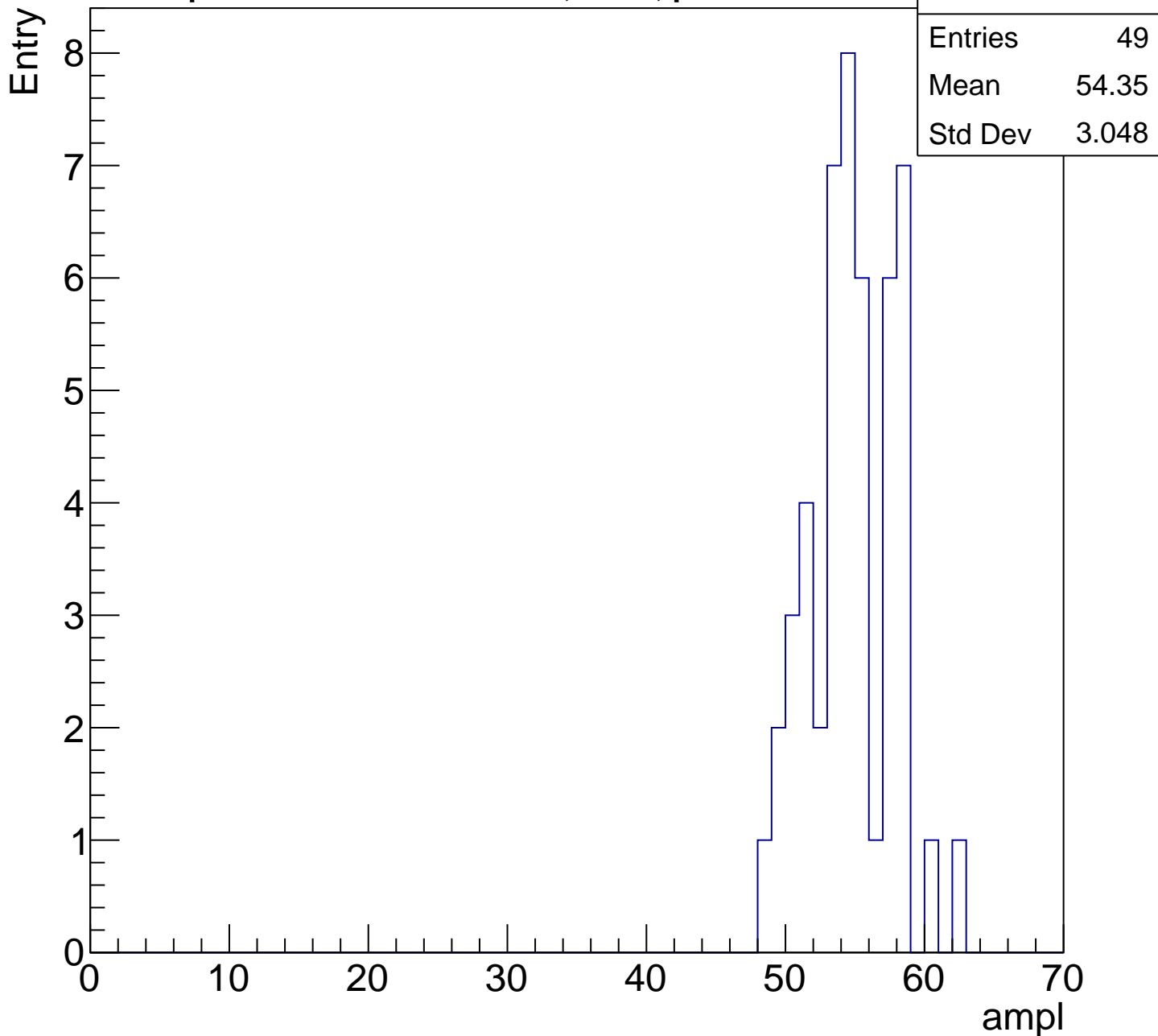
# B1L103S, U3-ch22, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U3-ch22, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U3-ch22, adc5

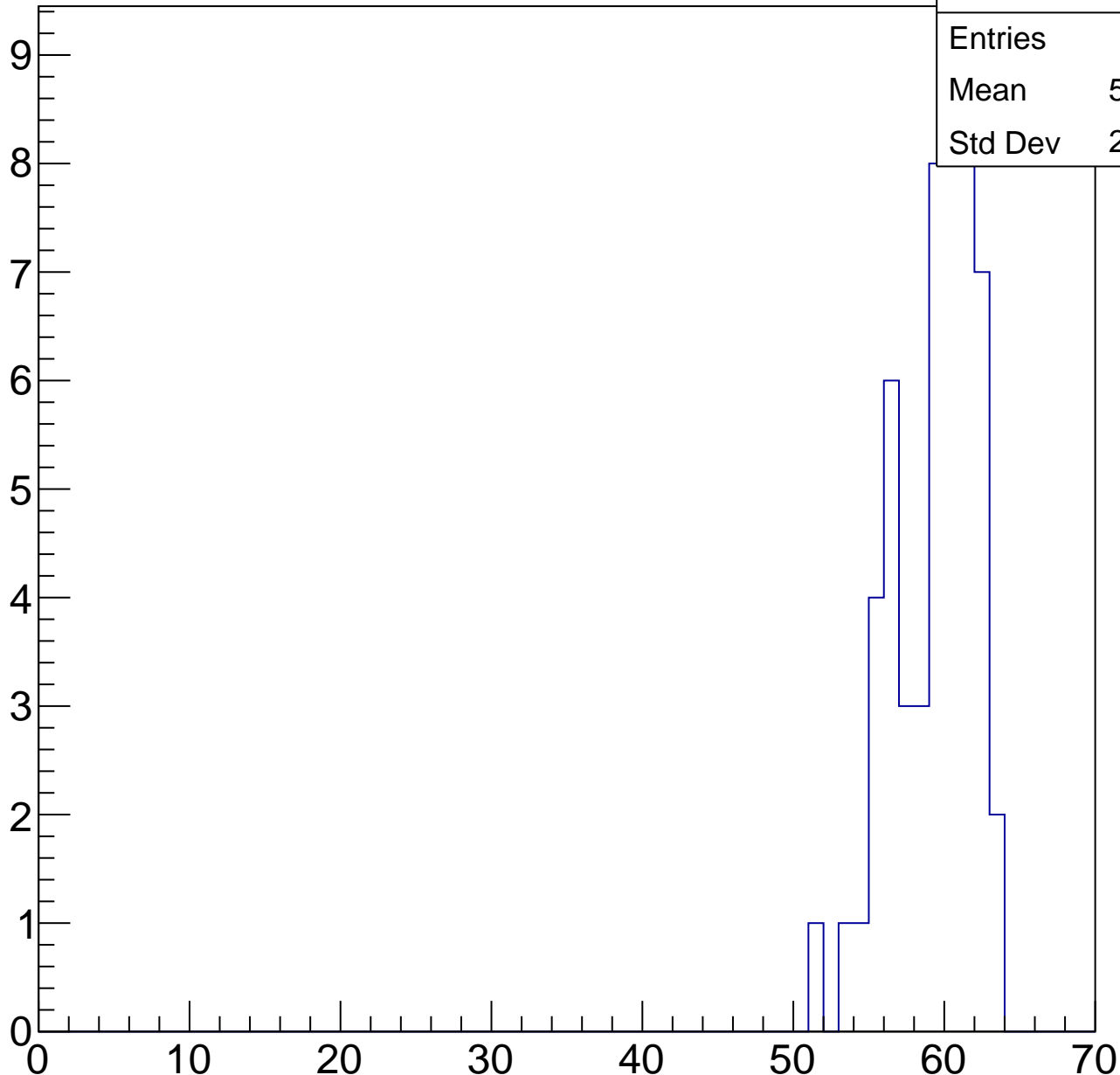
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	54
Mean	58.89
Std Dev	2.713

ampl

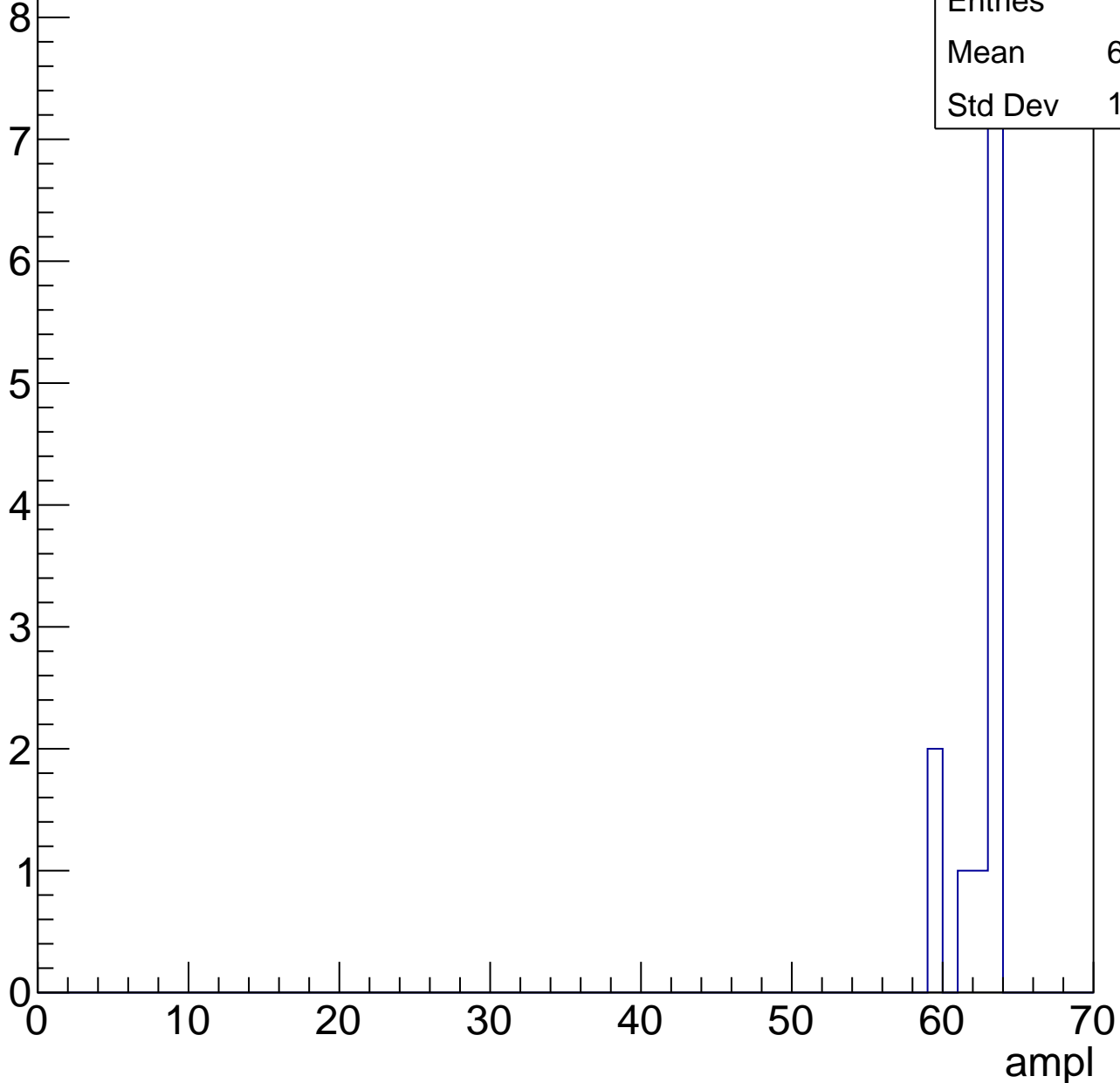


# B1L103S, U3-ch22, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	12
Mean	62.08
Std Dev	1.498

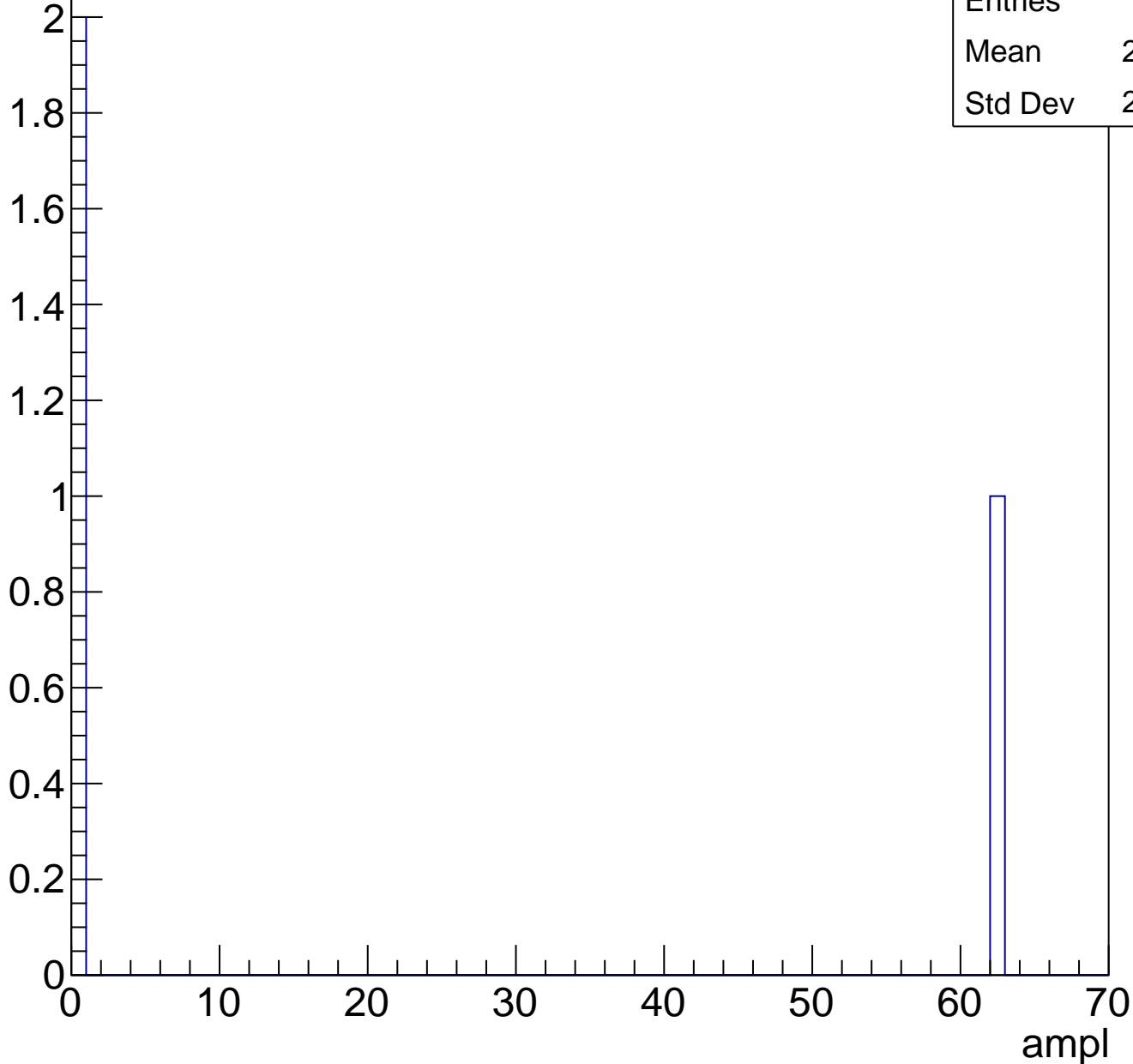




# B1L103S, U3-ch22, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch23, adc0

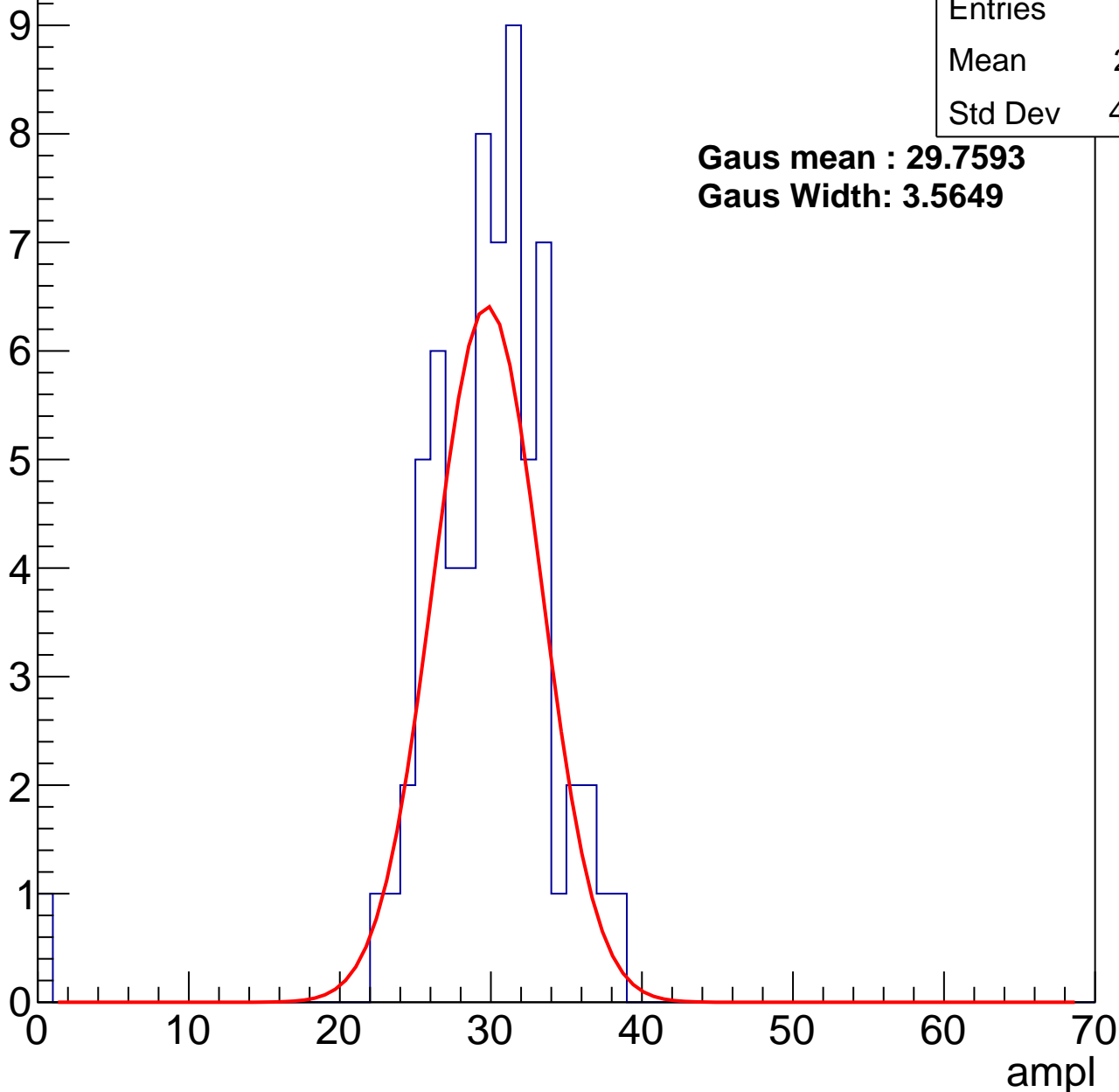
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	29.21
Std Dev	4.988

**Gaus mean : 29.7593**

**Gaus Width: 3.5649**



# B1L103S, U3-ch23, adc1

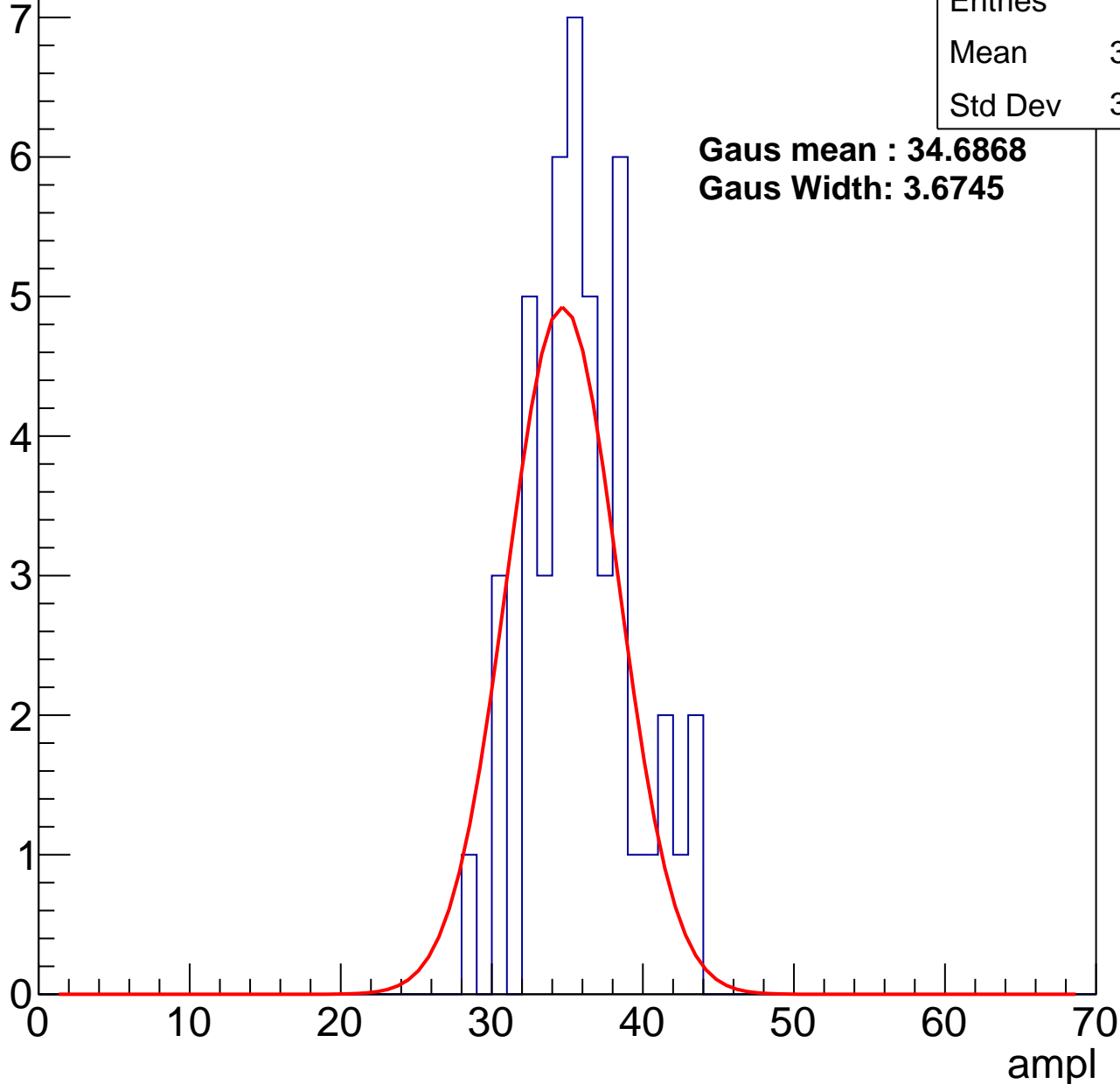
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	46
Mean	35.52
Std Dev	3.412

**Gaus mean : 34.6868**

**Gaus Width: 3.6745**



# B1L103S, U3-ch23, adc2

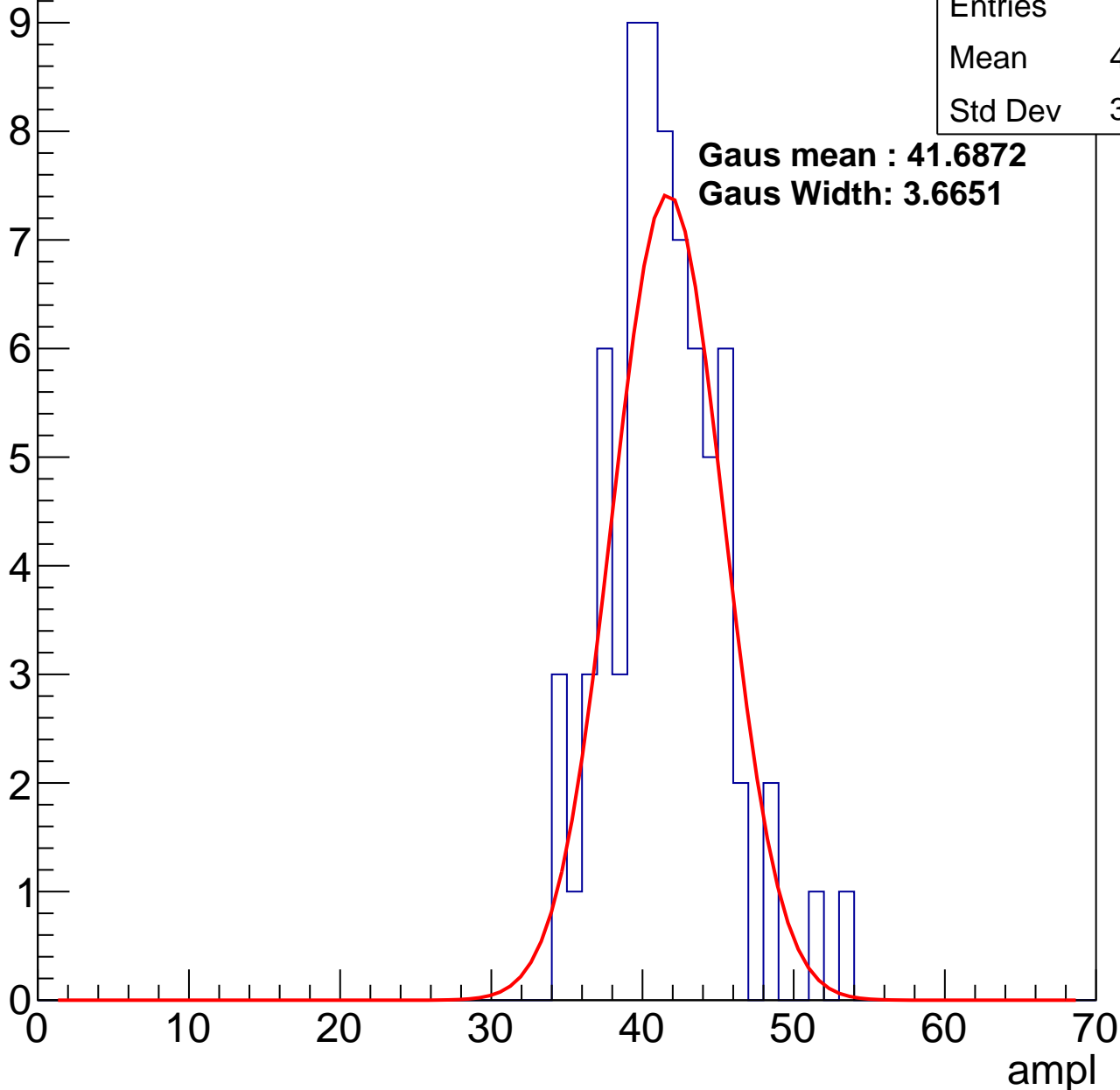
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	41.03
Std Dev	3.708

**Gaus mean : 41.6872**

**Gaus Width: 3.6651**



# B1L103S, U3-ch23, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	76
Mean	48.66
Std Dev	3.303

Entry

10

8

6

4

2

0

0

10

20

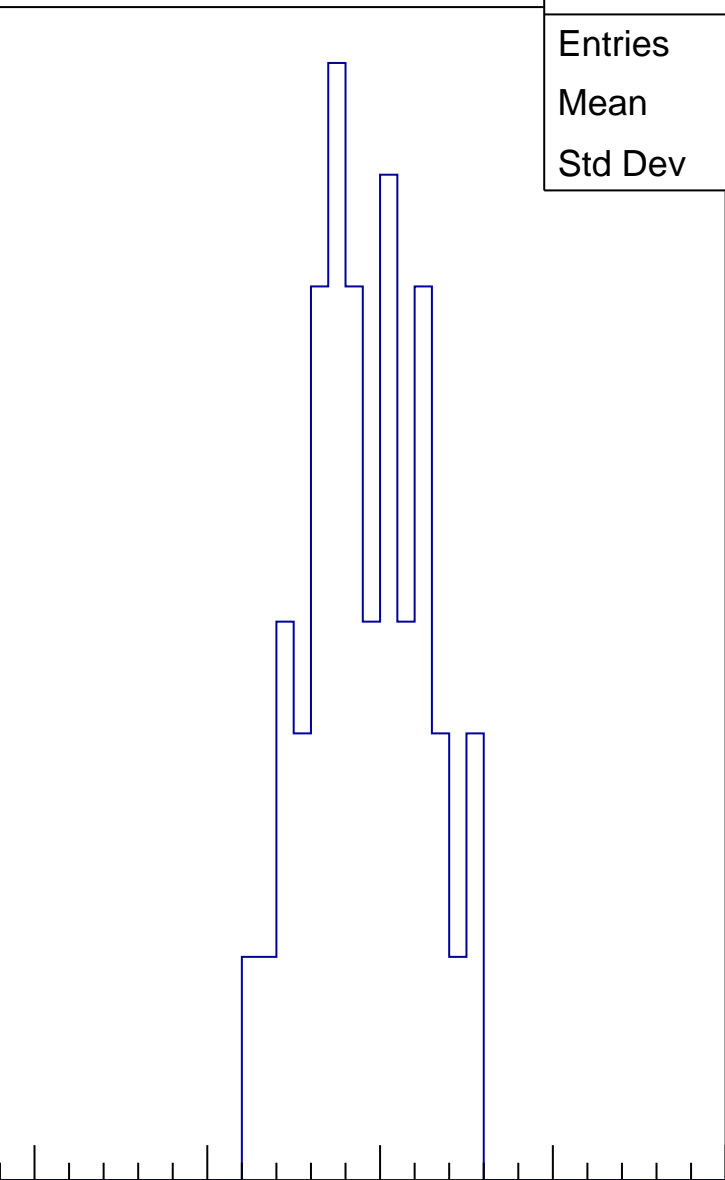
30

40

50

60

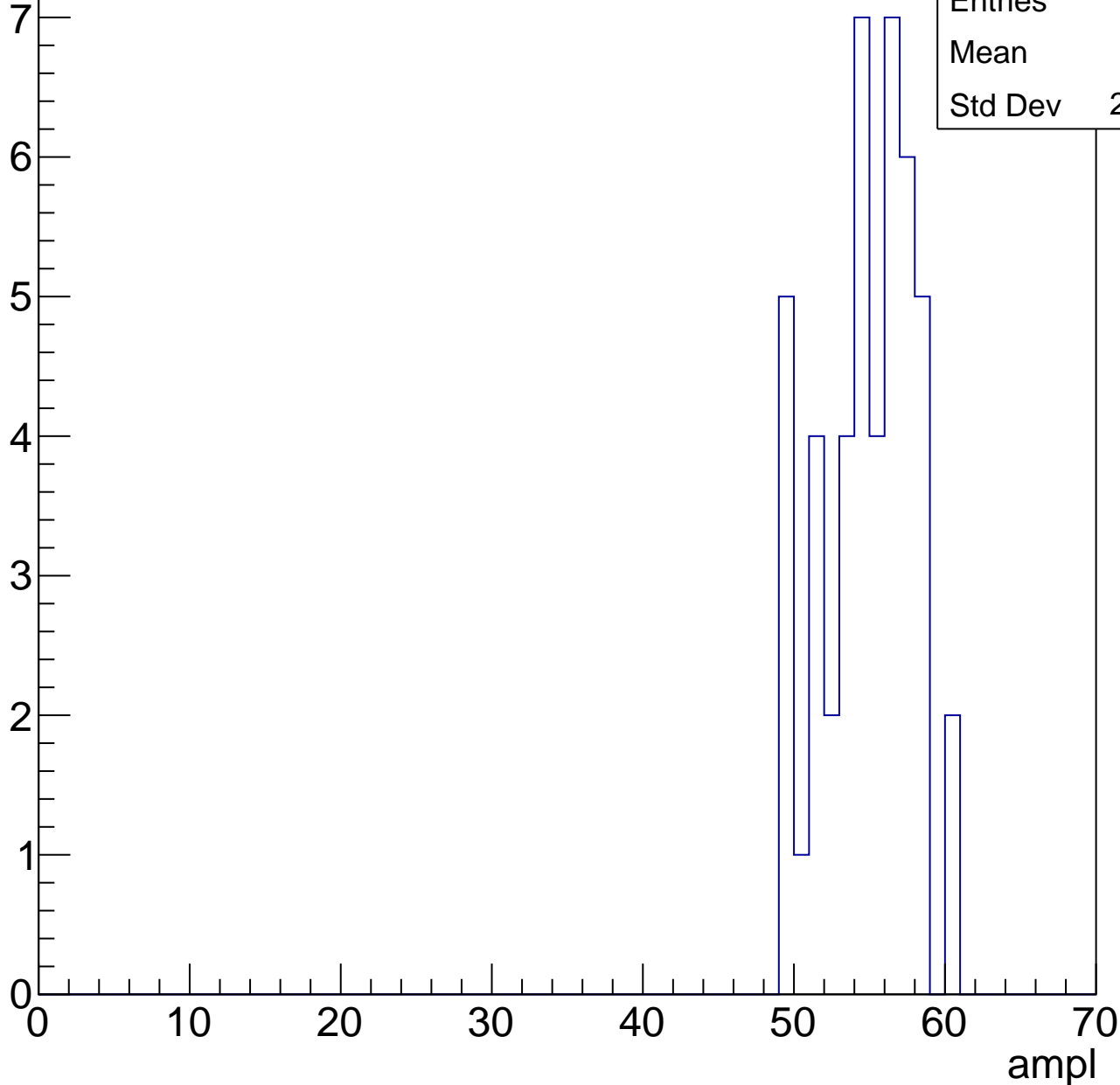
ampl



# B1L103S, U3-ch23, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

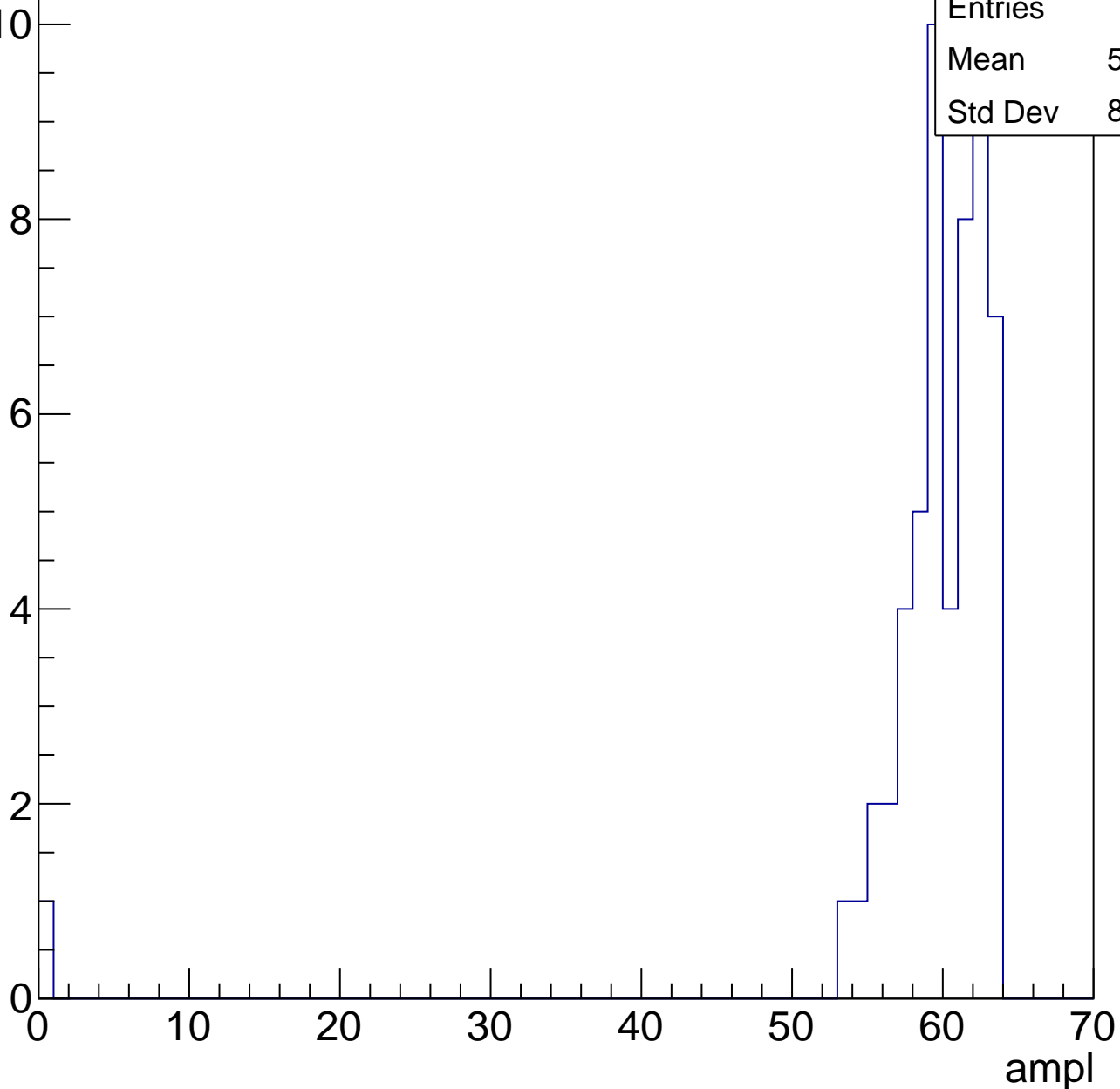


# B1L103S, U3-ch23, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

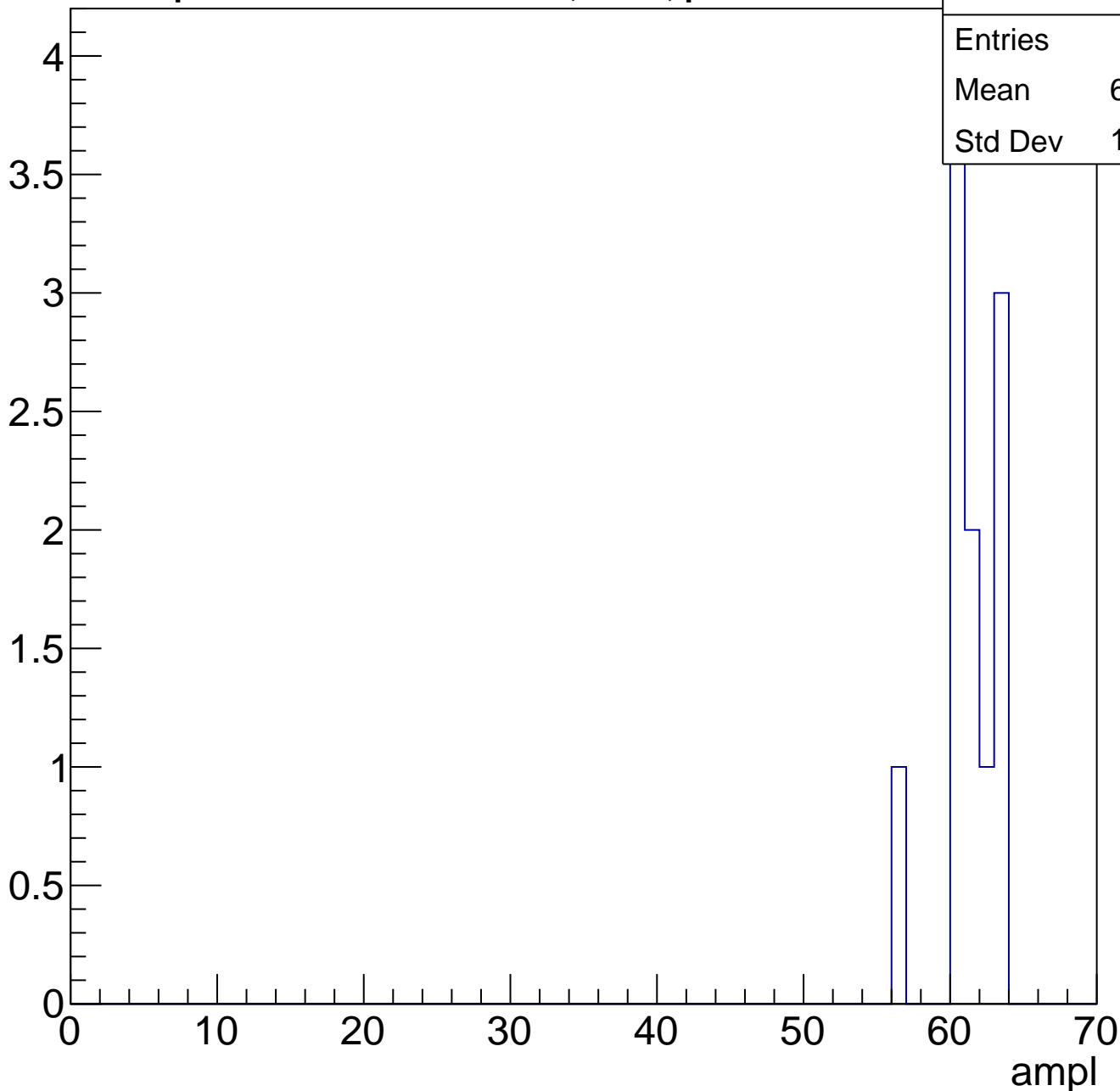
Entries	54
Mean	58.59
Std Dev	8.425



# B1L103S, U3-ch23, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	11
Mean	60.82
Std Dev	1.946



# B1L103S, U3-ch23, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch24, adc0

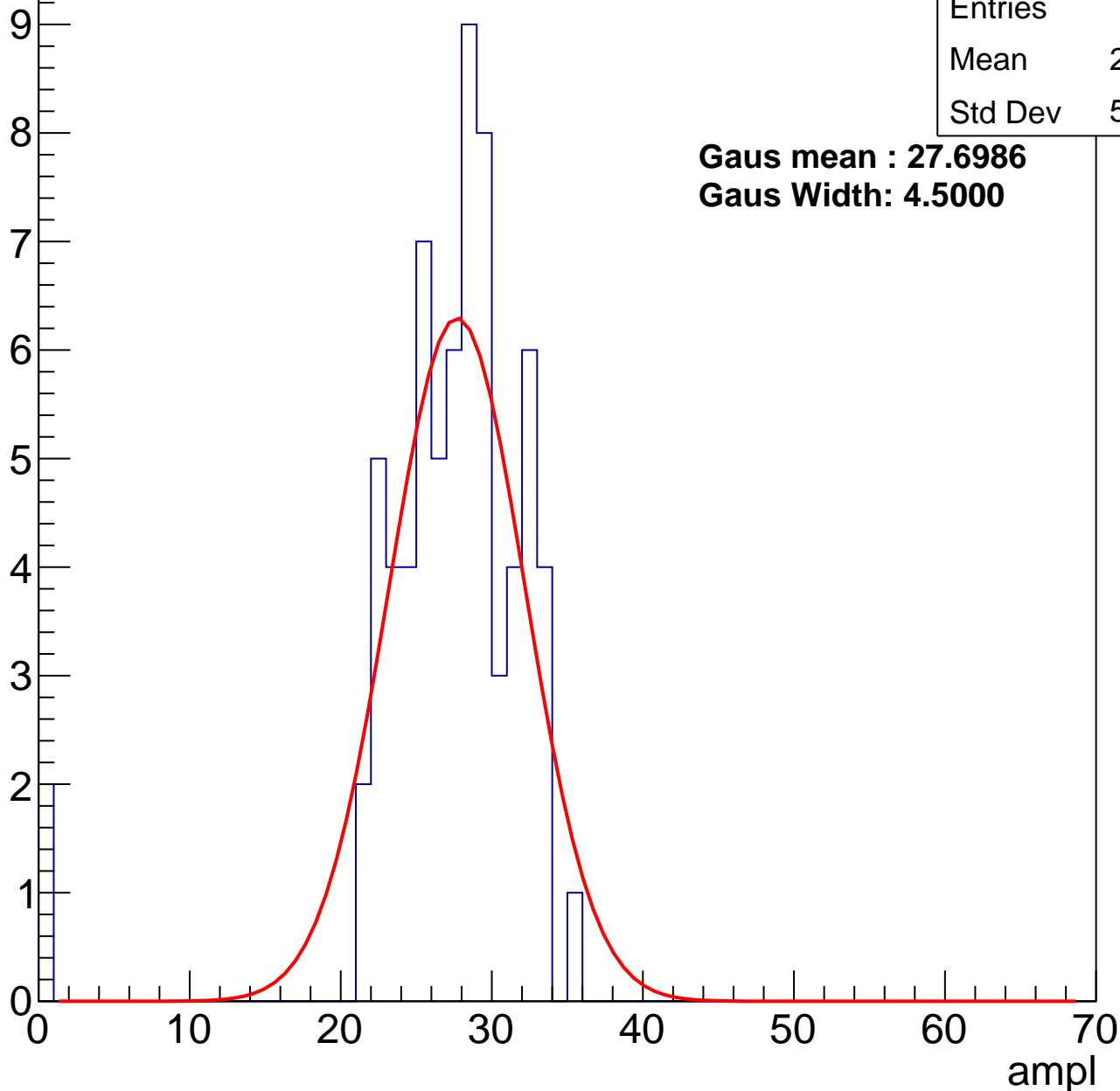
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	26.63
Std Dev	5.693

**Gaus mean : 27.6986**

**Gaus Width: 4.5000**



# B1L103S, U3-ch24, adc1

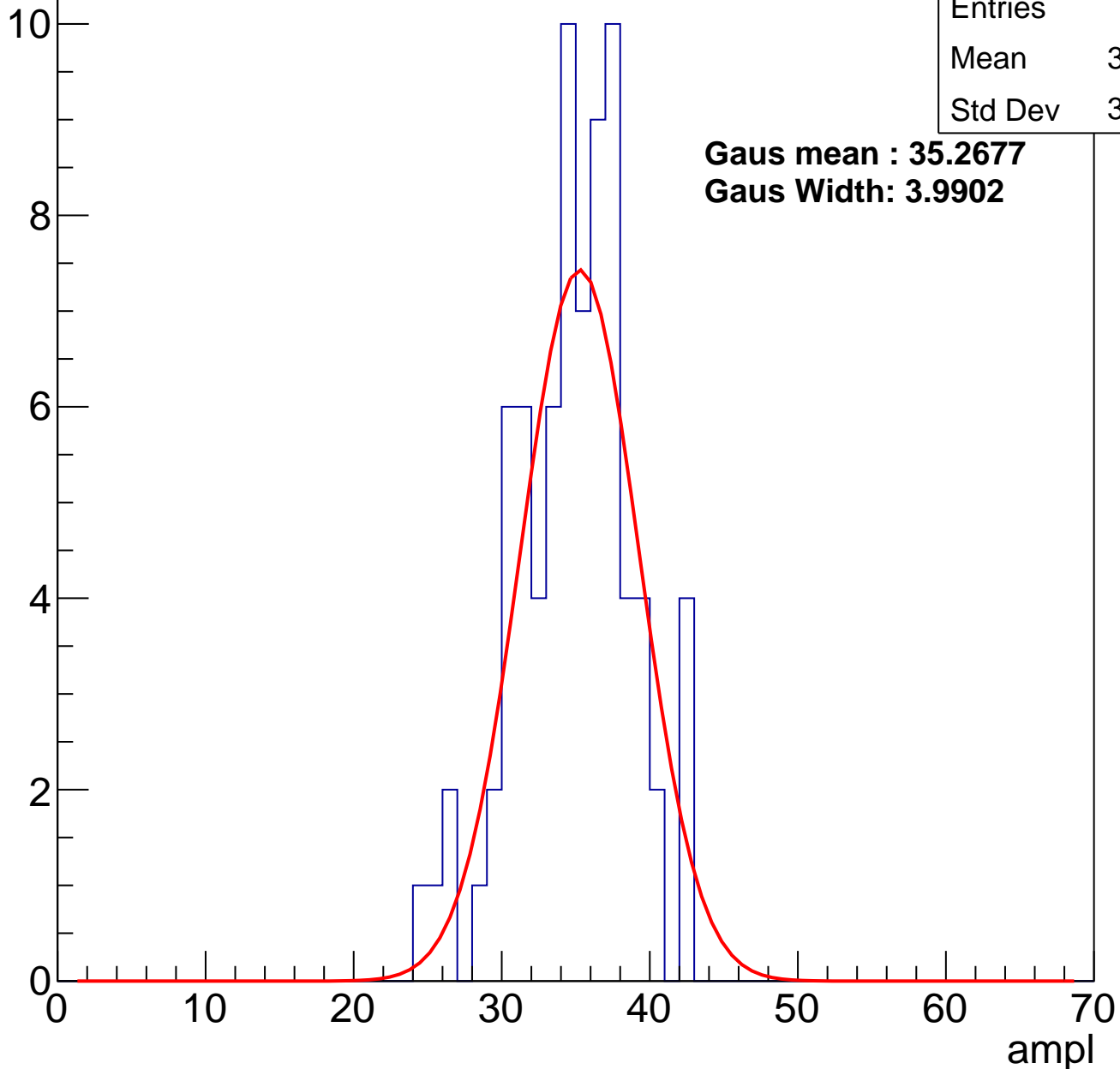
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	79
Mean	34.35
Std Dev	3.868

**Gaus mean : 35.2677**

**Gaus Width: 3.9902**

Entry



# B1L103S, U3-ch24, adc2

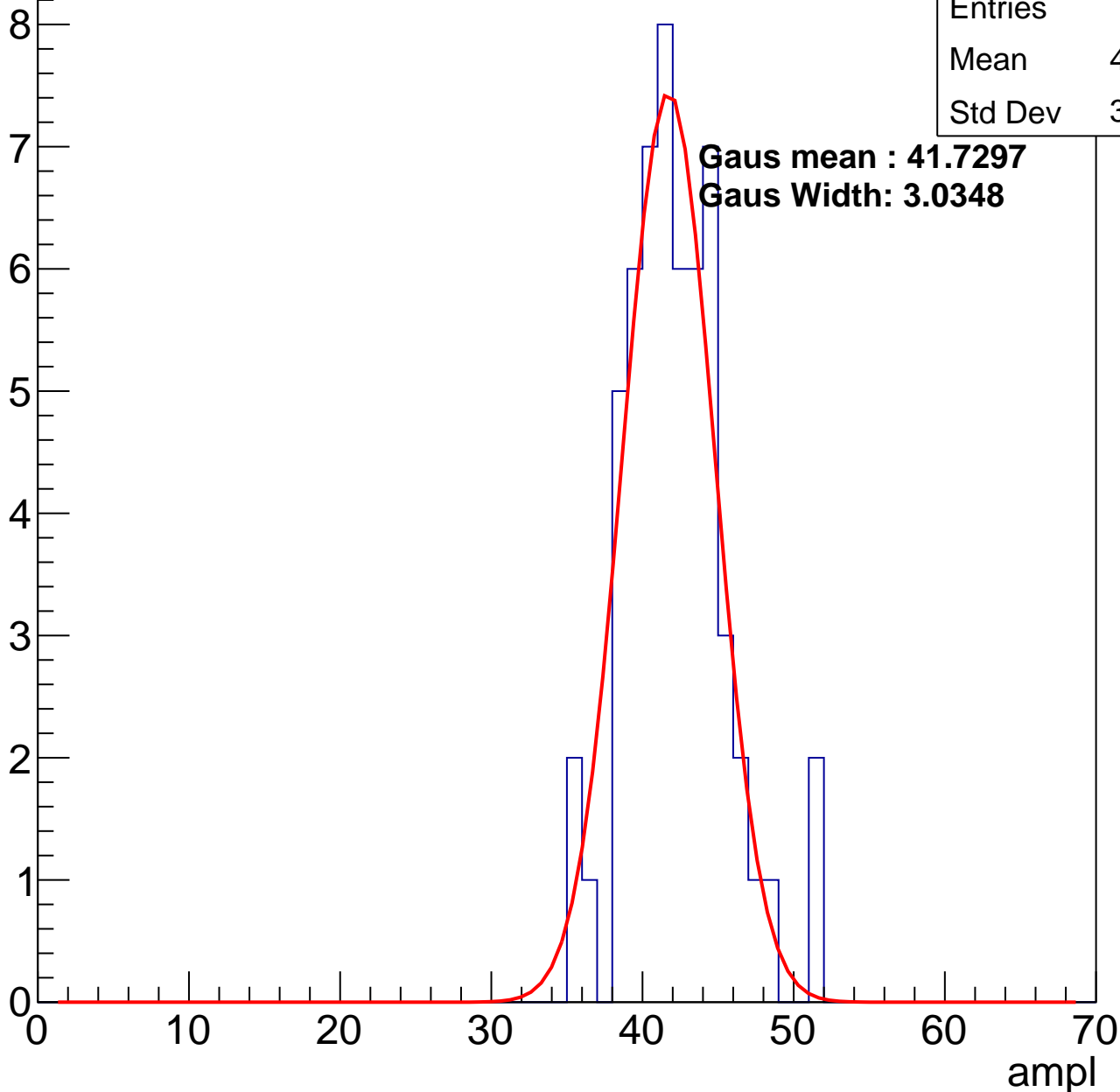
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	41.75
Std Dev	3.289

**Gaus mean : 41.7297**

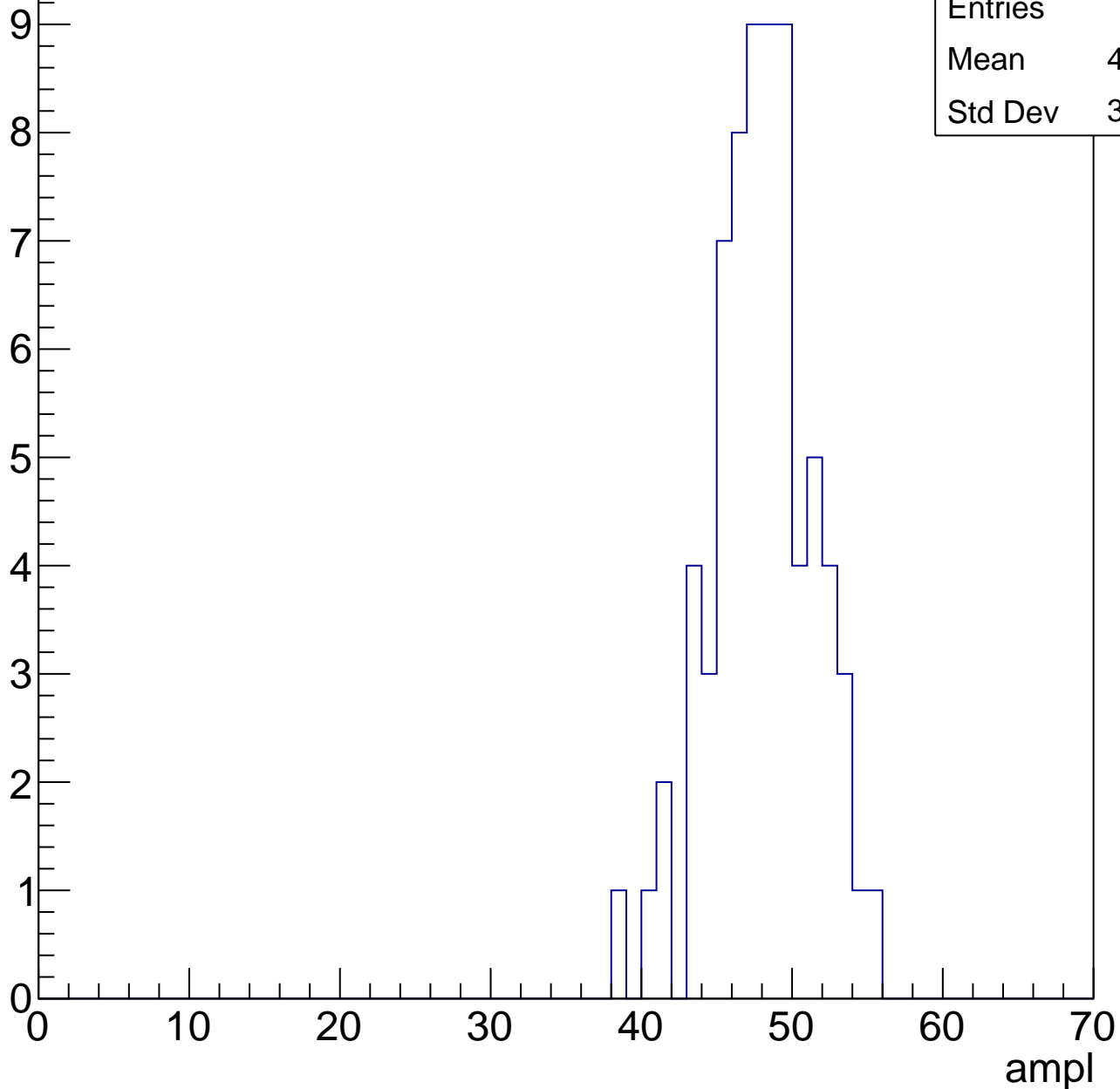
**Gaus Width: 3.0348**



# B1L103S, U3-ch24, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



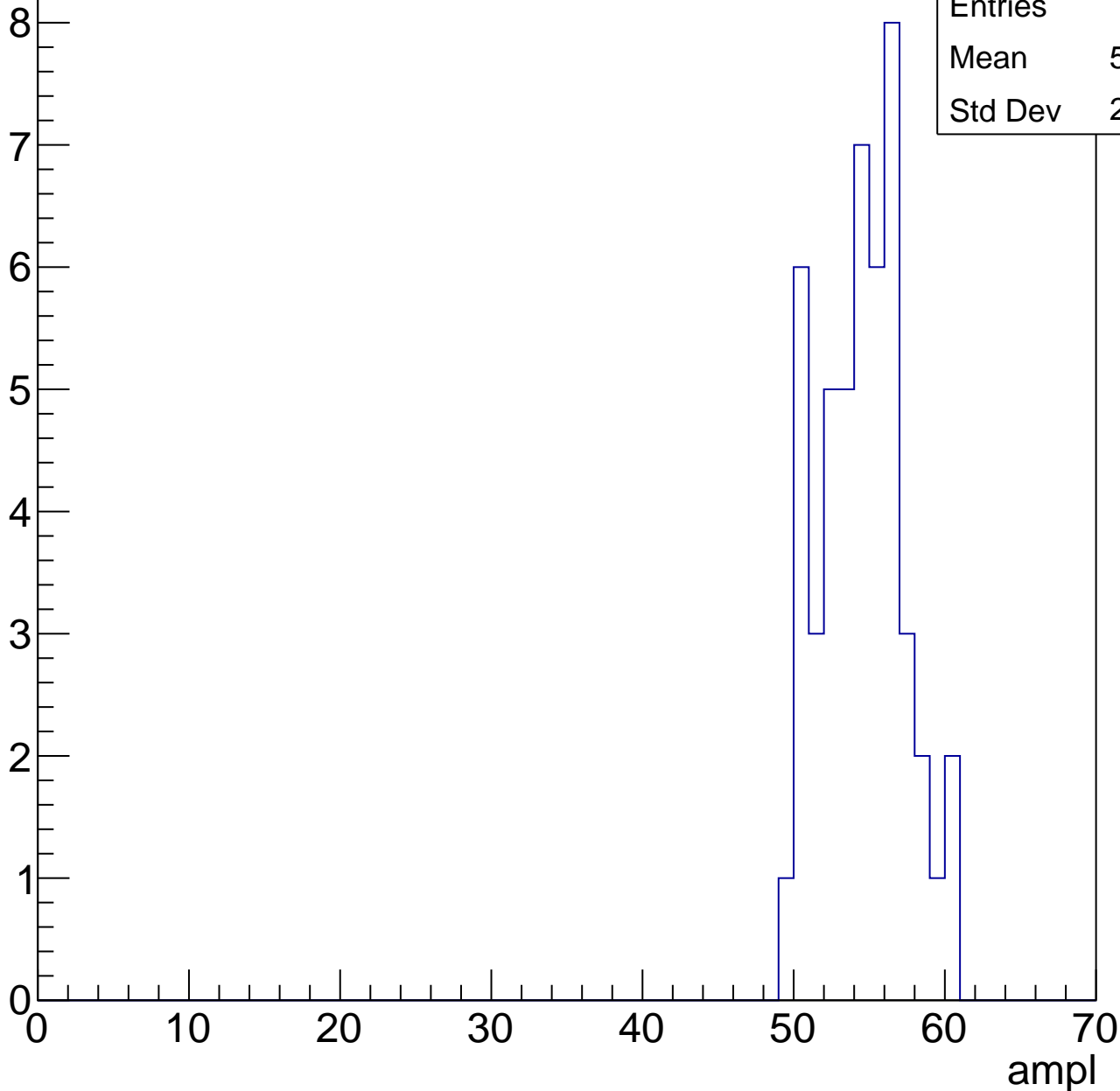
Entries	71
Mean	47.52
Std Dev	3.339

# B1L103S, U3-ch24, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

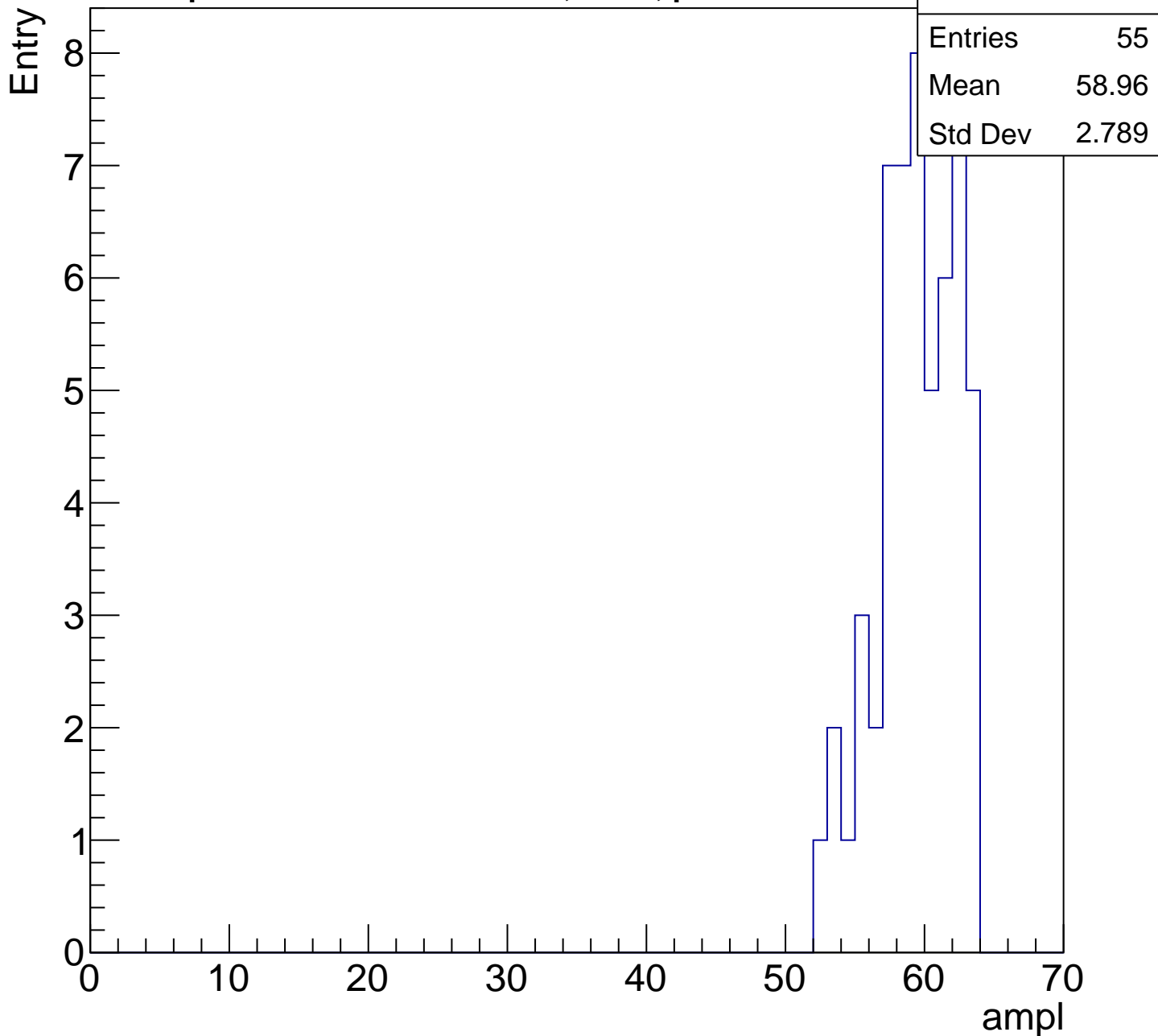
Entry

Entries	49
Mean	54.06
Std Dev	2.736



# B1L103S, U3-ch24, adc5

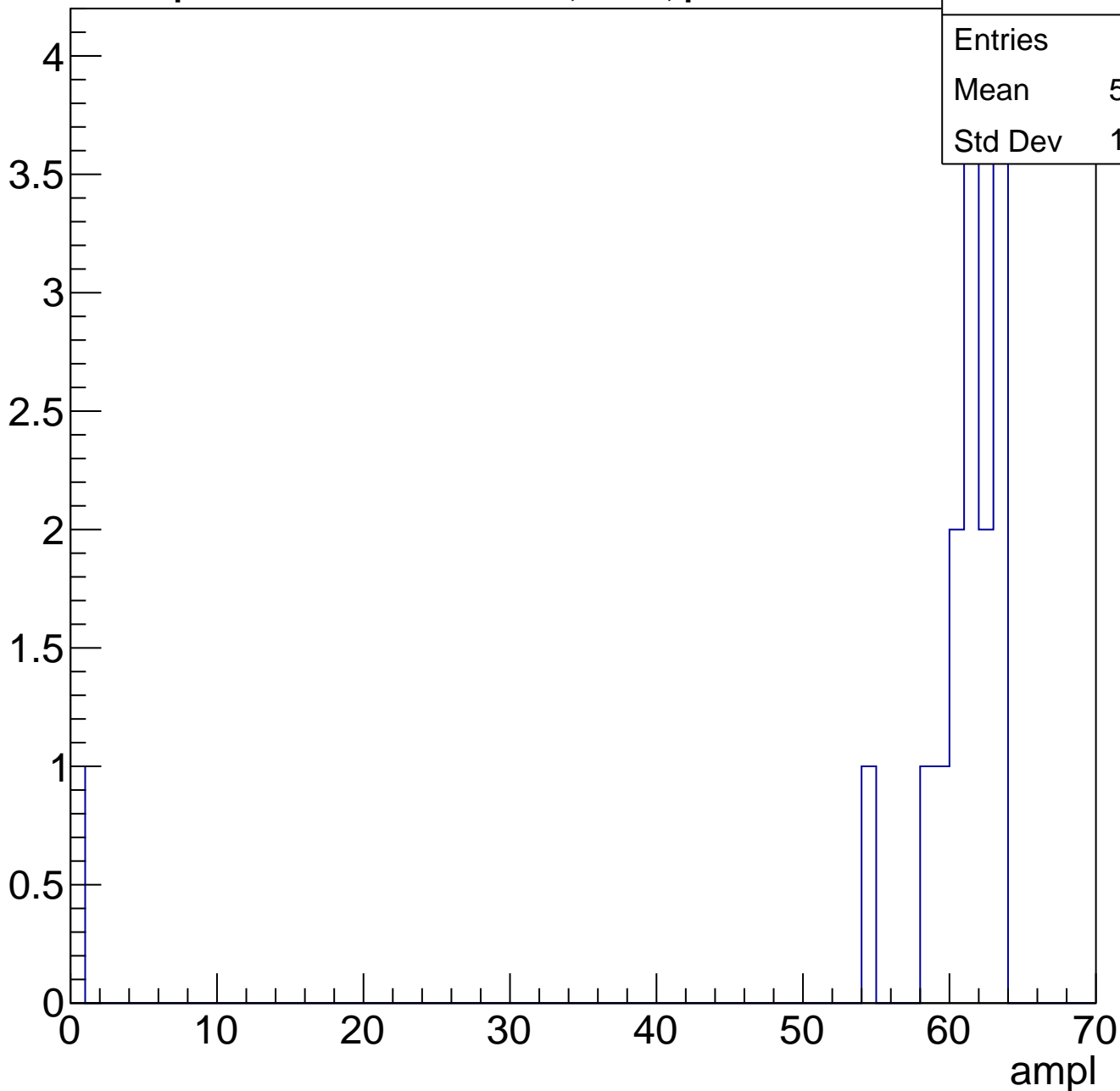
calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U3-ch24, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

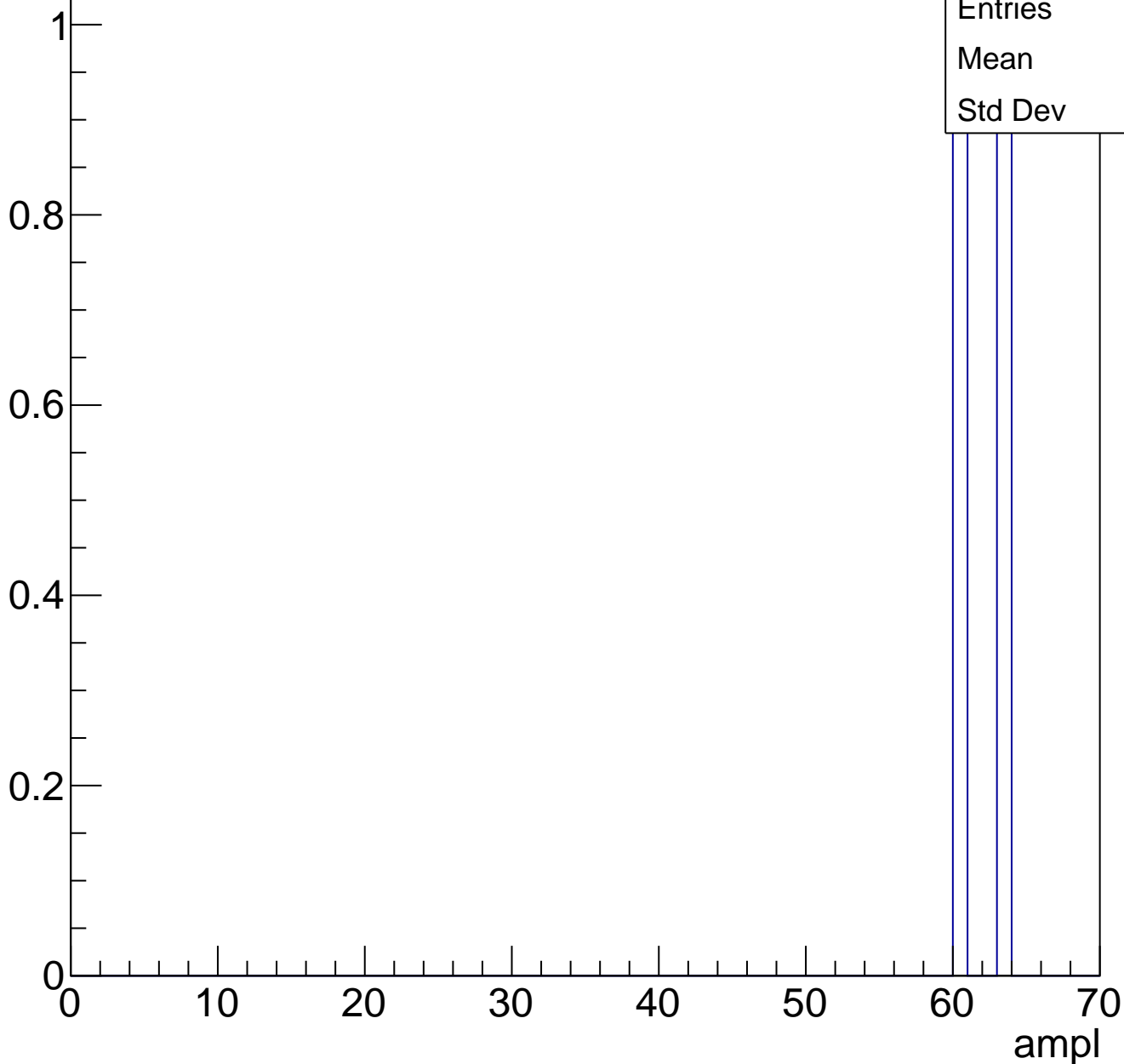




# B1L103S, U3-ch24, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch25, adc0

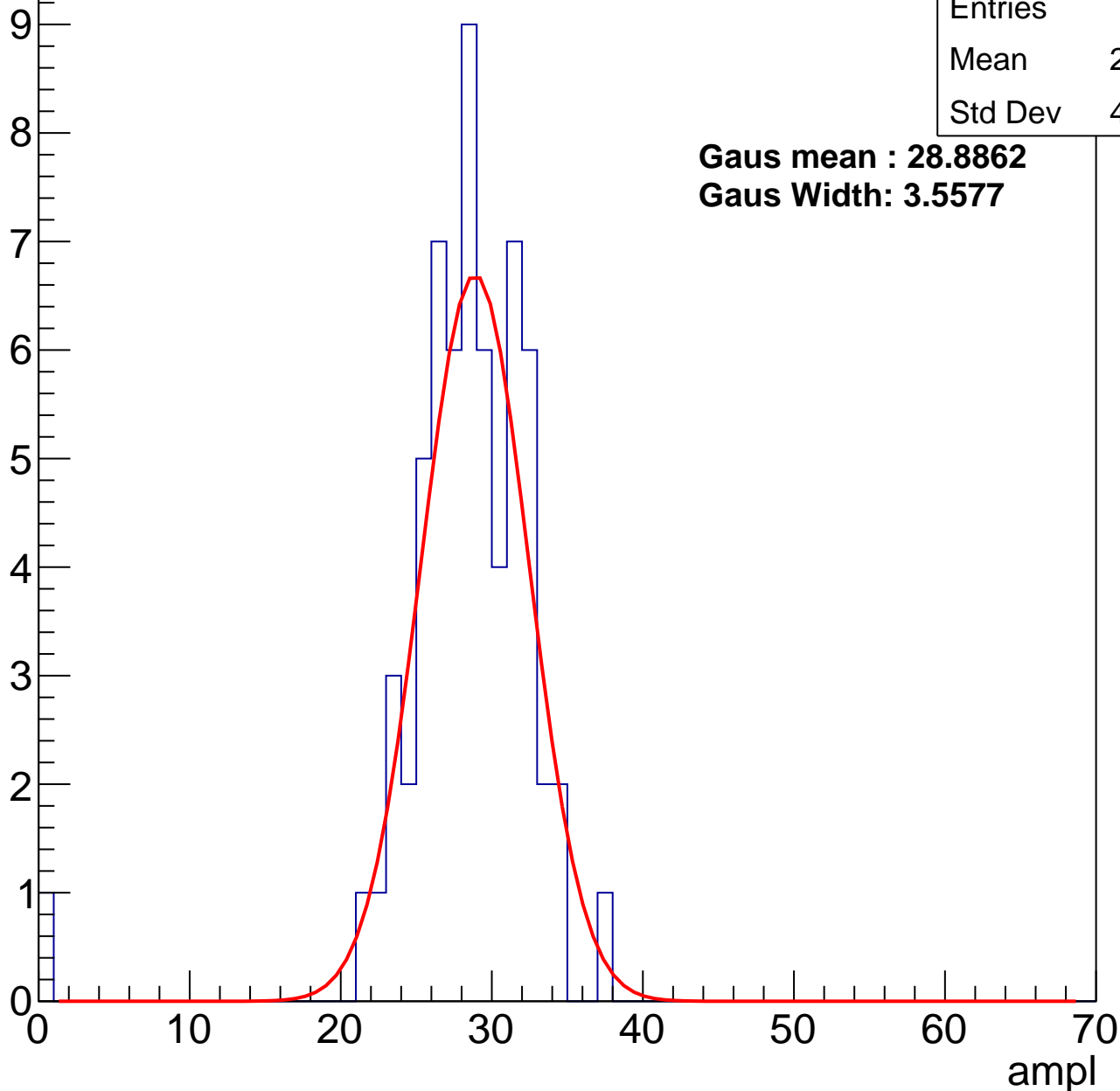
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	27.86
Std Dev	4.777

**Gaus mean : 28.8862**

**Gaus Width: 3.5577**



# B1L103S, U3-ch25, adc1

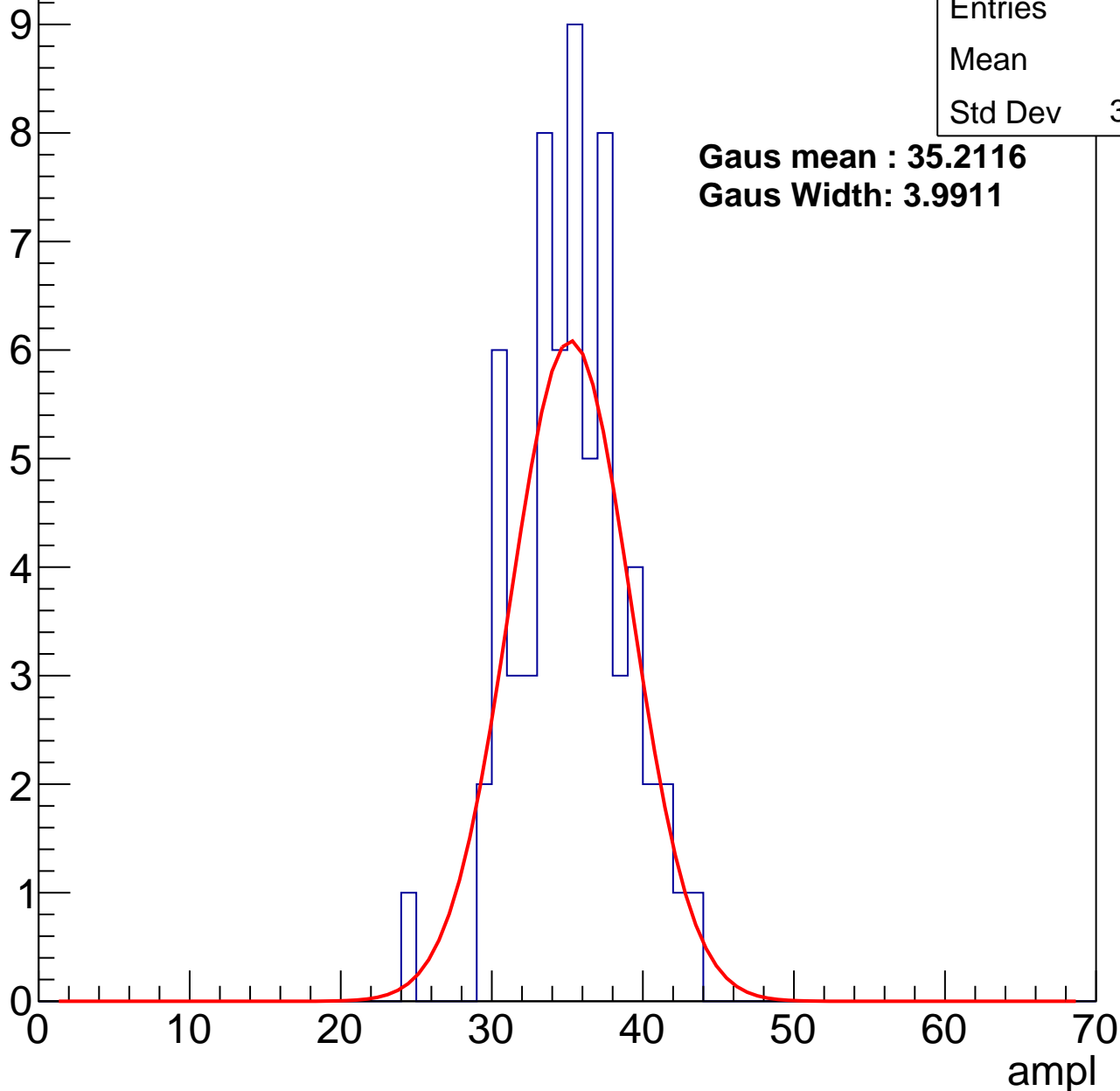
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	34.8
Std Dev	3.572

**Gaus mean : 35.2116**

**Gaus Width: 3.9911**



# B1L103S, U3-ch25, adc2

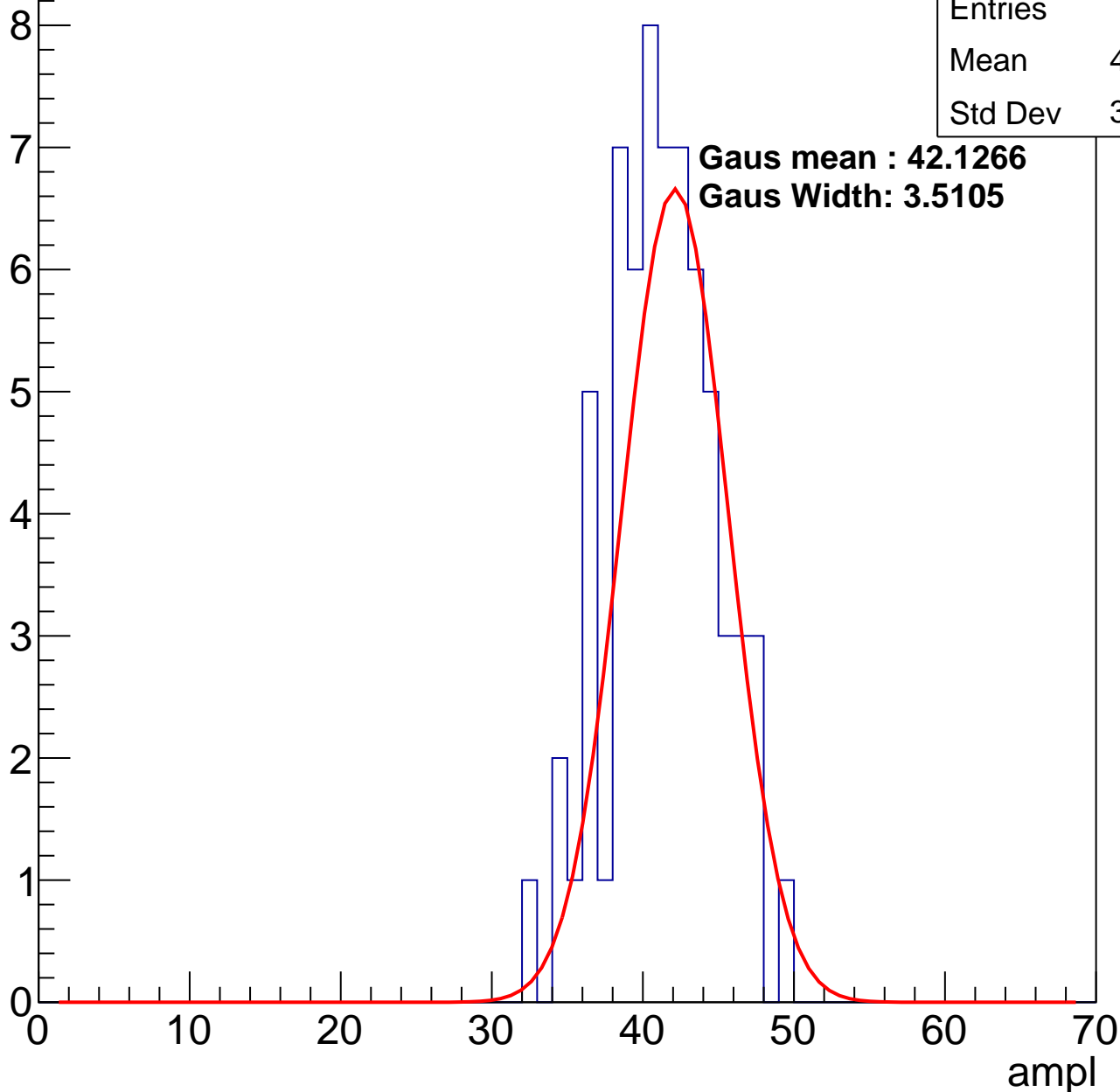
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	40.82
Std Dev	3.524

**Gaus mean : 42.1266**

**Gaus Width: 3.5105**

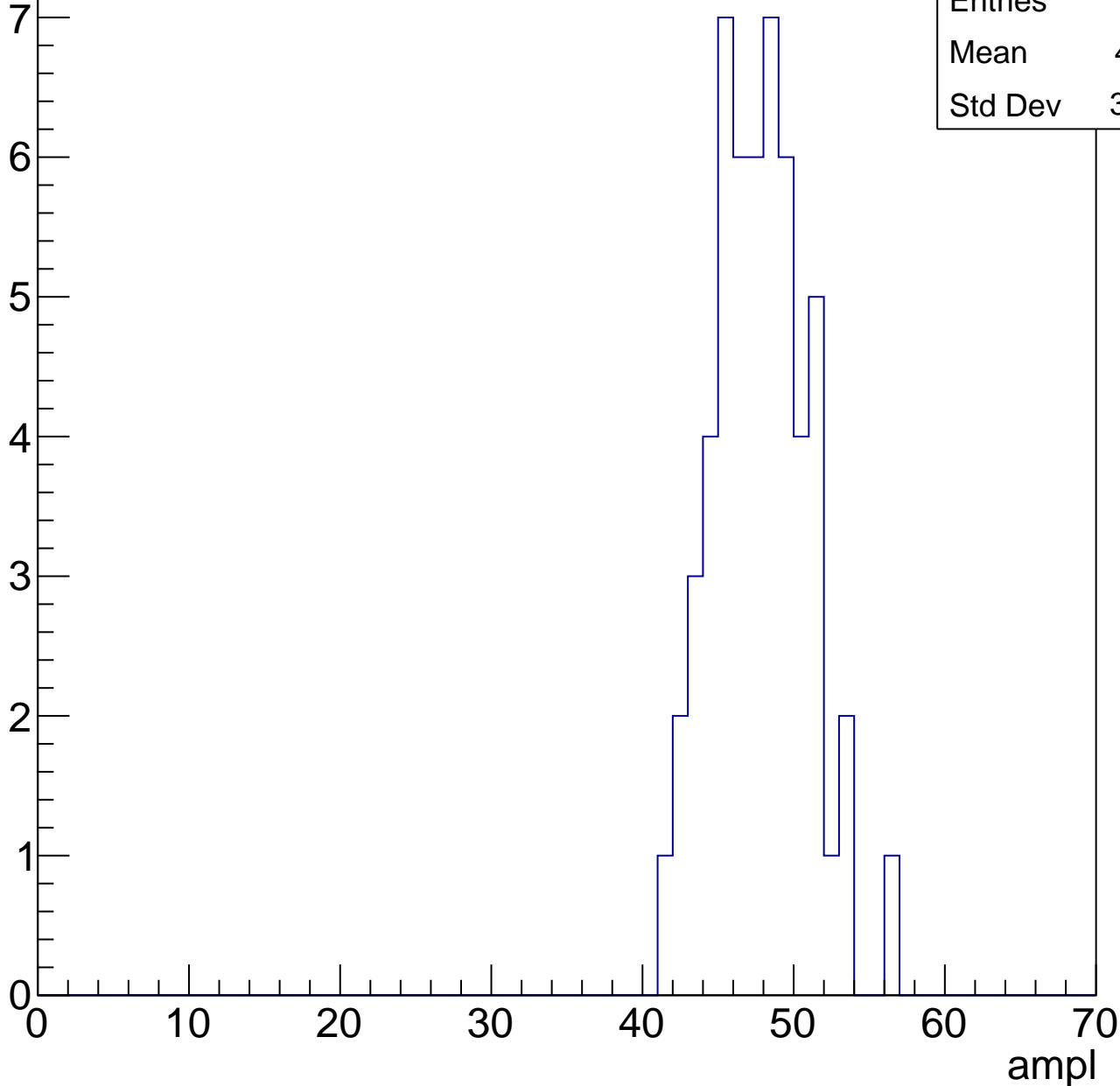


# B1L103S, U3-ch25, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	47.31
Std Dev	3.086

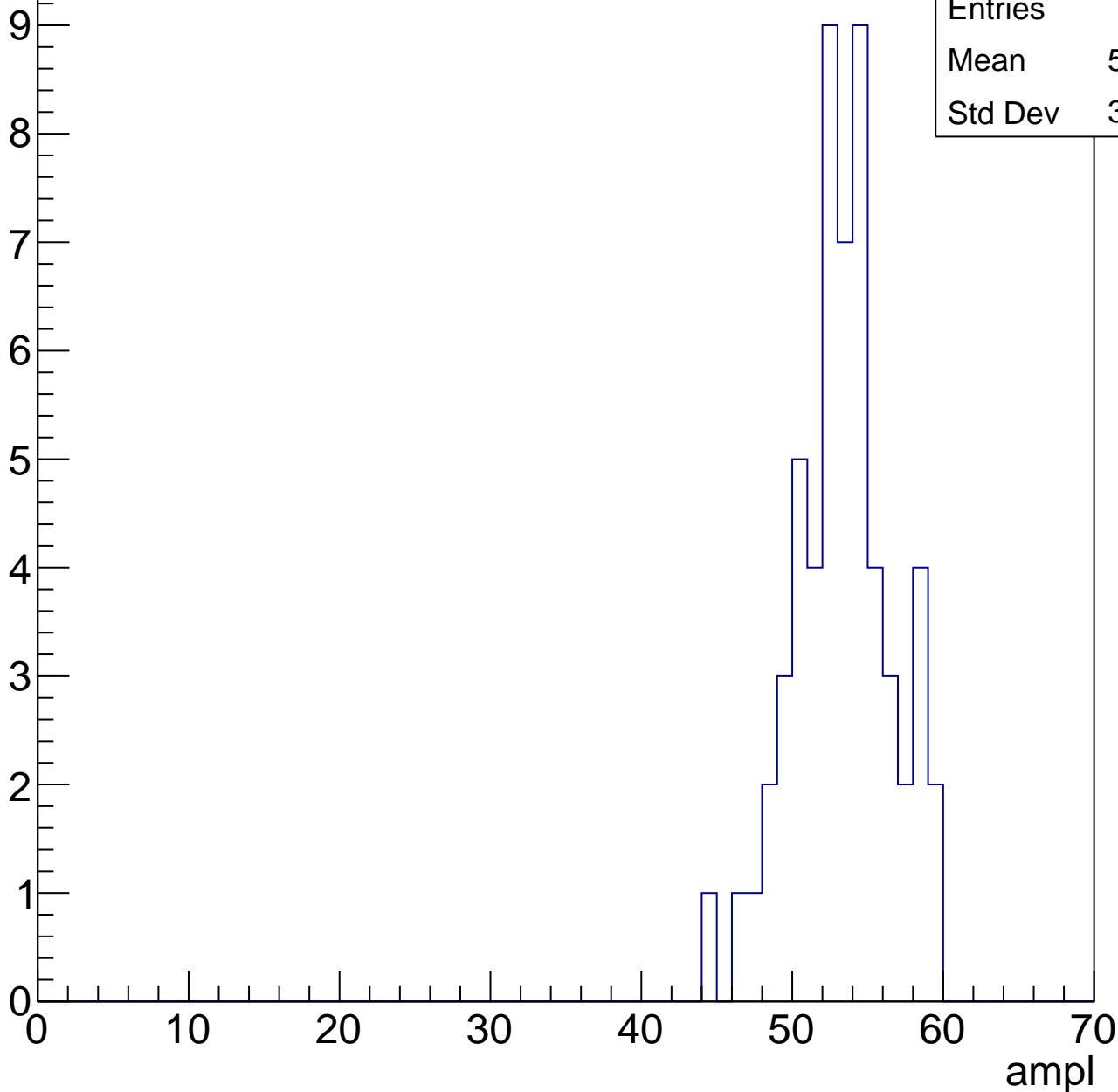


# B1L103S, U3-ch25, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	52.82
Std Dev	3.212

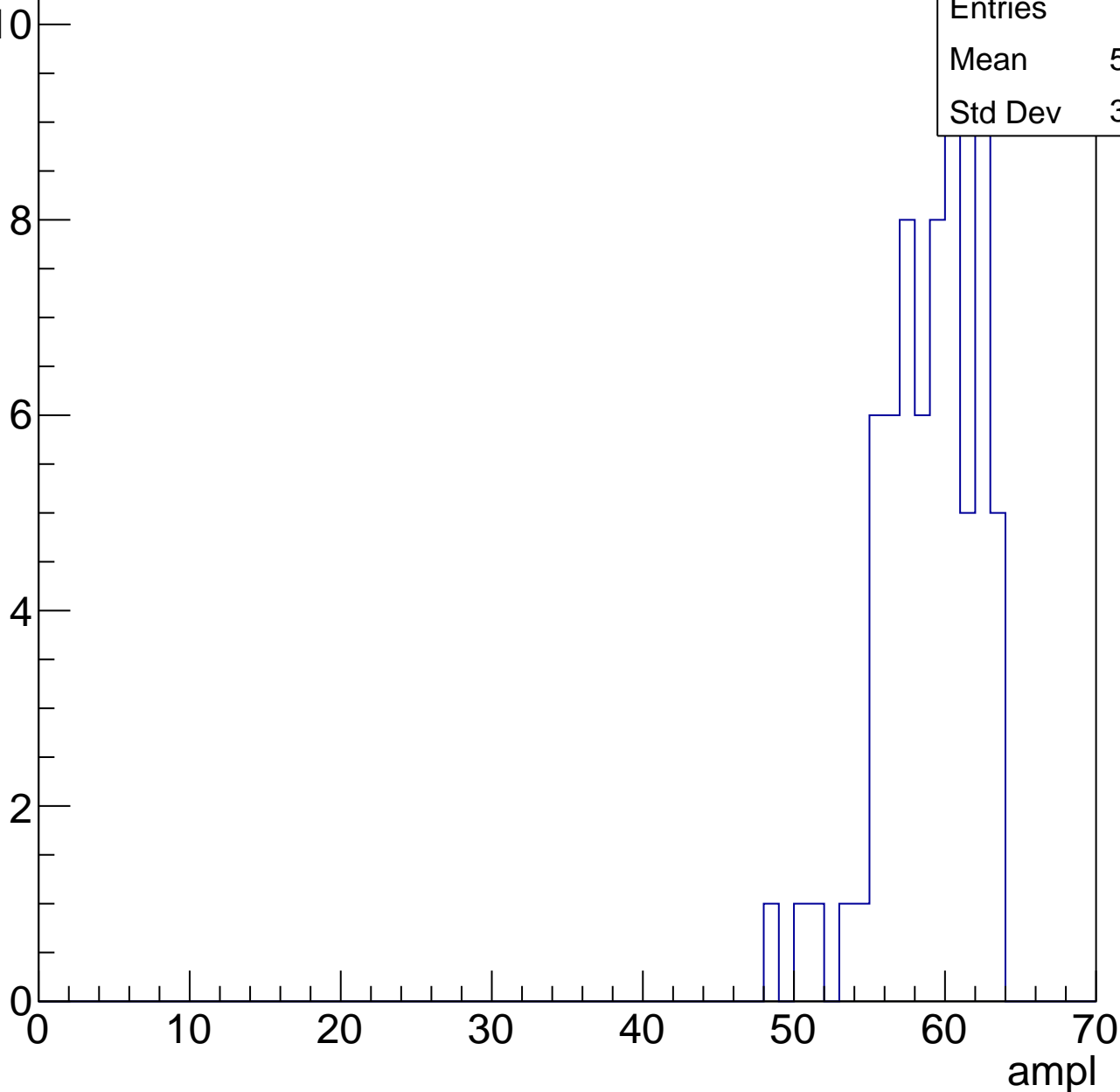


# B1L103S, U3-ch25, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	58.47
Std Dev	3.178

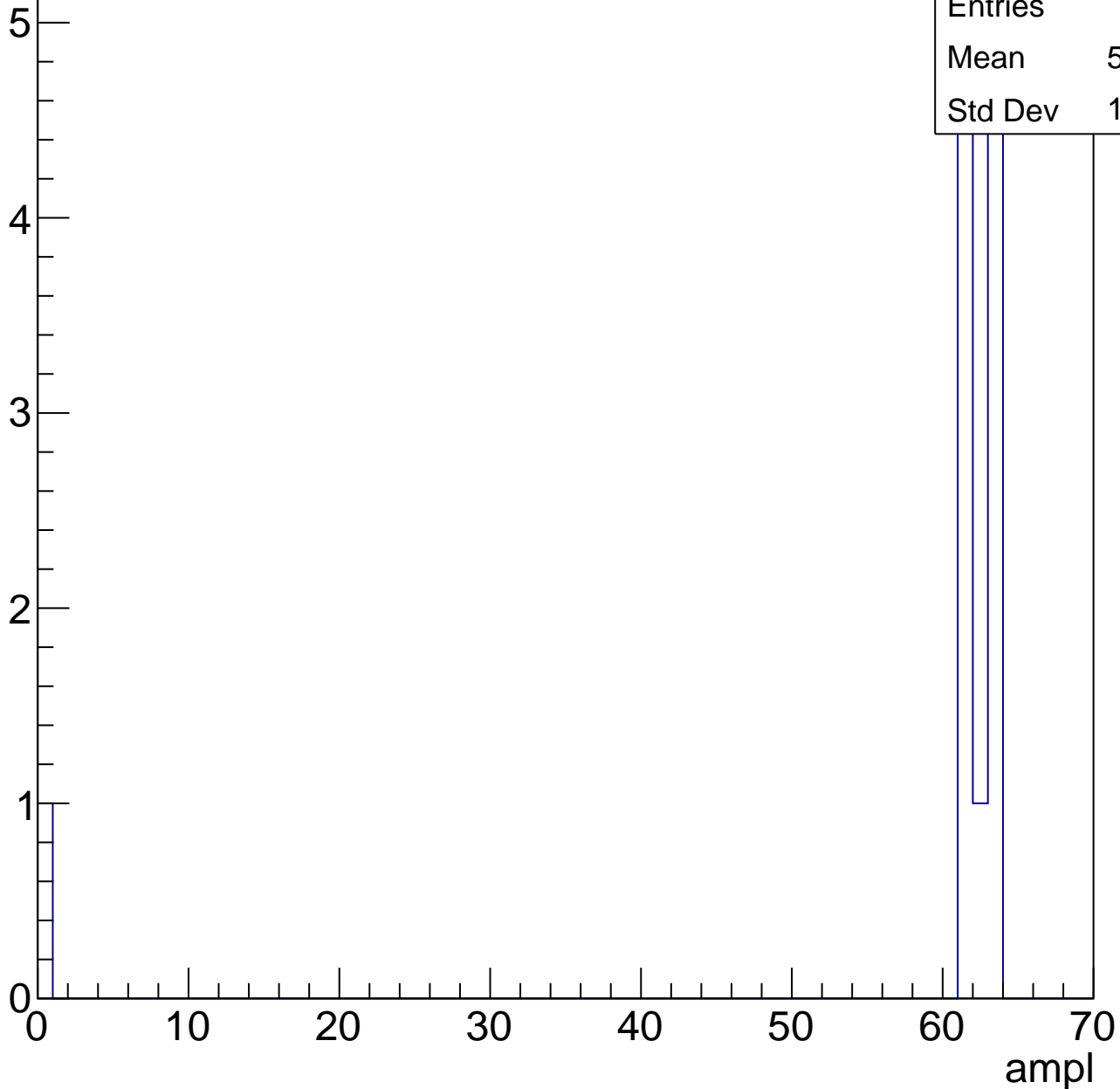


# B1L103S, U3-ch25, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	12
Mean	56.83
Std Dev	17.16





# B1L103S, U3-ch25, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch26, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	86
Mean	29.21
Std Dev	6.625

**Gaus mean : 30.5253**

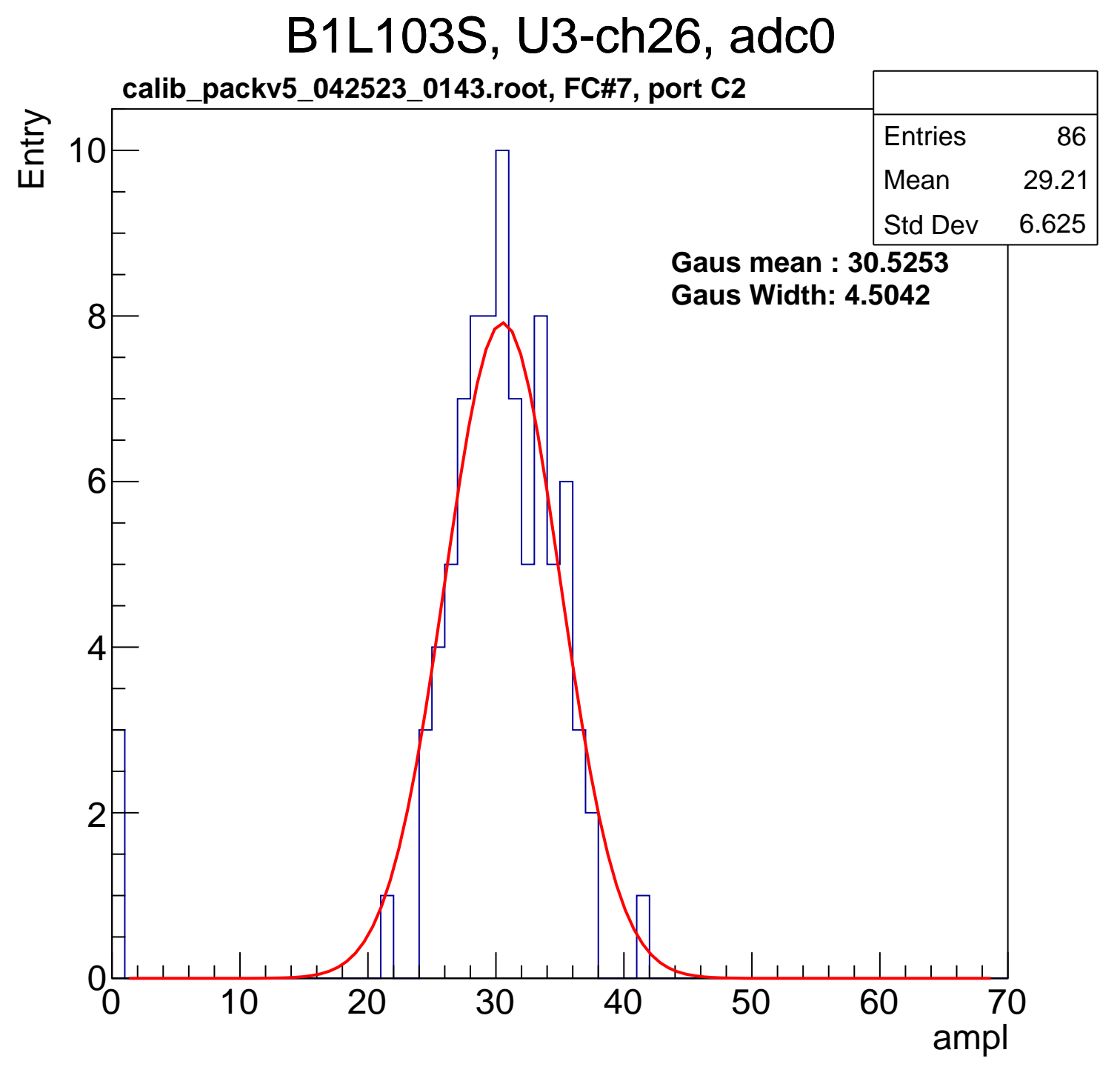
**Gaus Width: 4.5042**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U3-ch26, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	63
Mean	37.37
Std Dev	3.316

**Gaus mean : 38.0392**

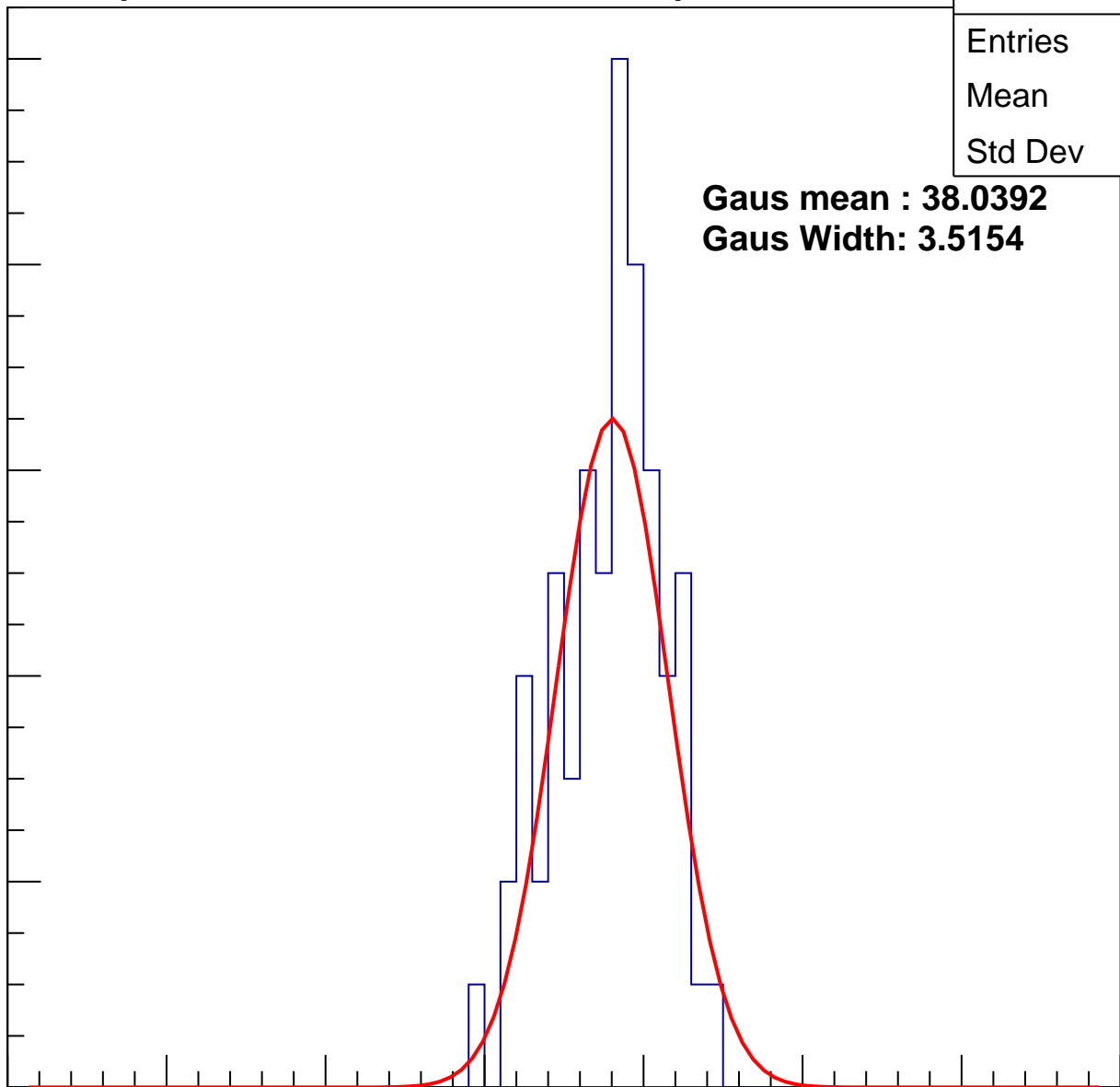
**Gaus Width: 3.5154**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U3-ch26, adc2

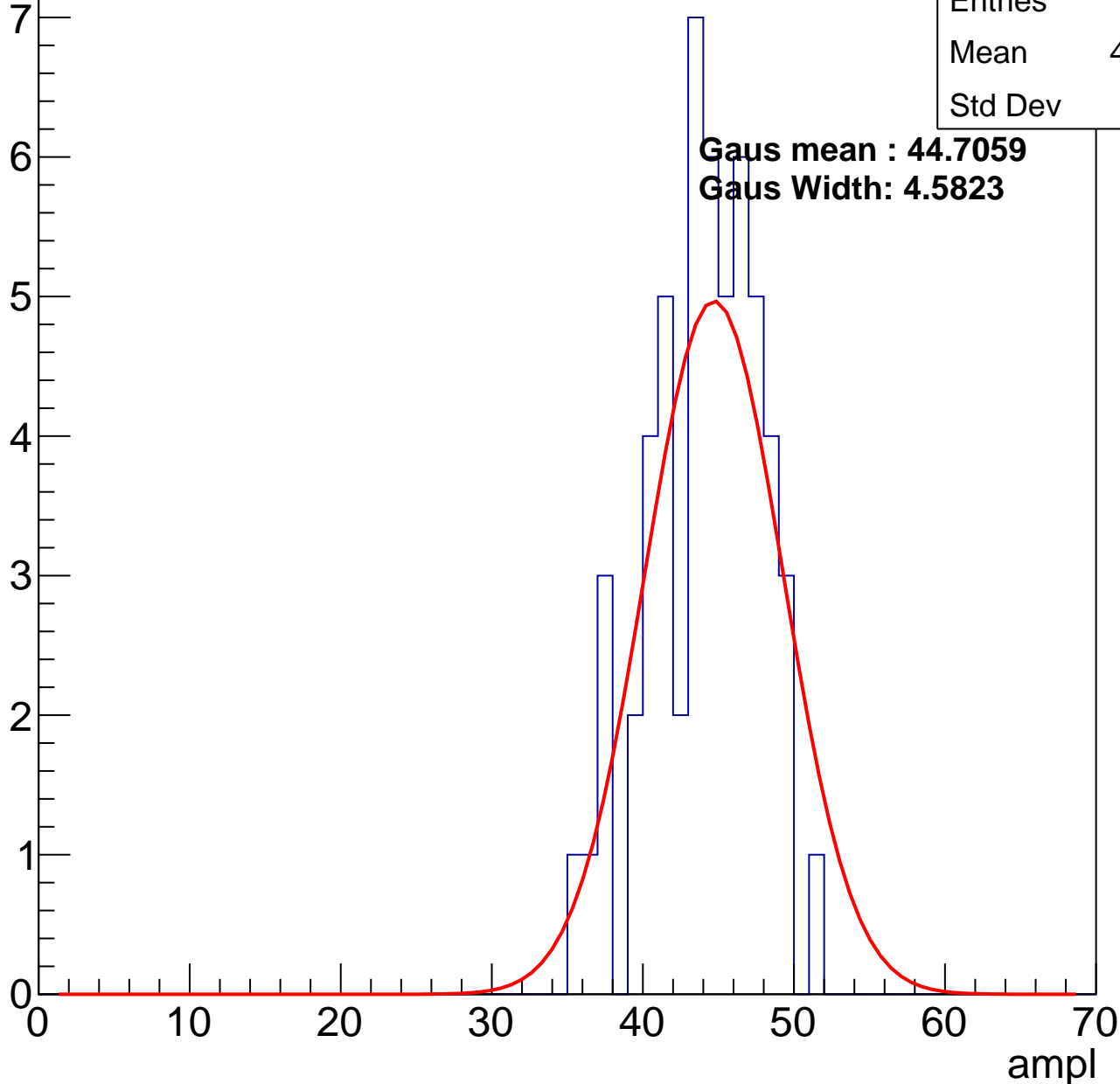
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	43.64
Std Dev	3.62

**Gaus mean : 44.7059**

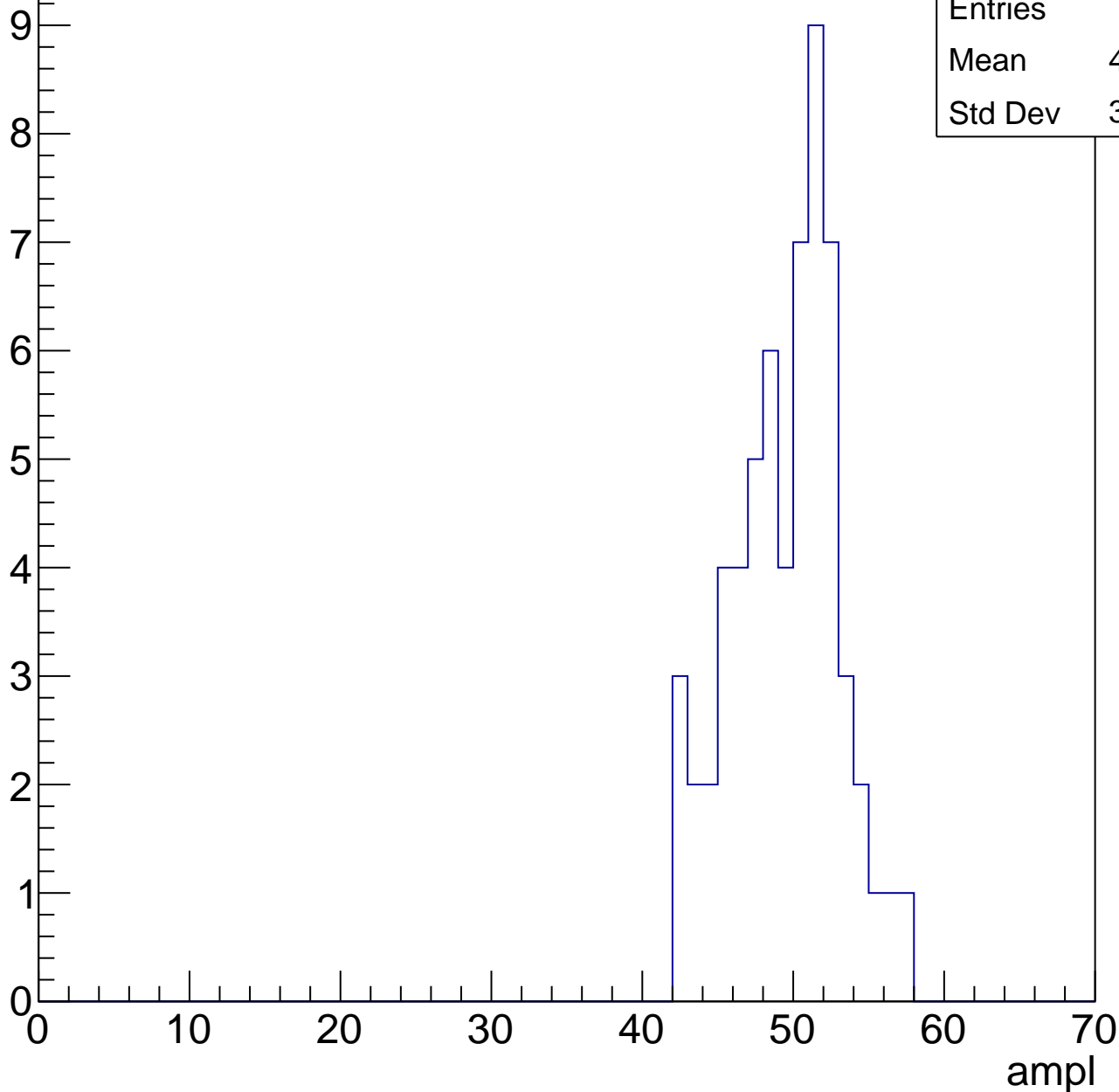
**Gaus Width: 4.5823**



# B1L103S, U3-ch26, adc3

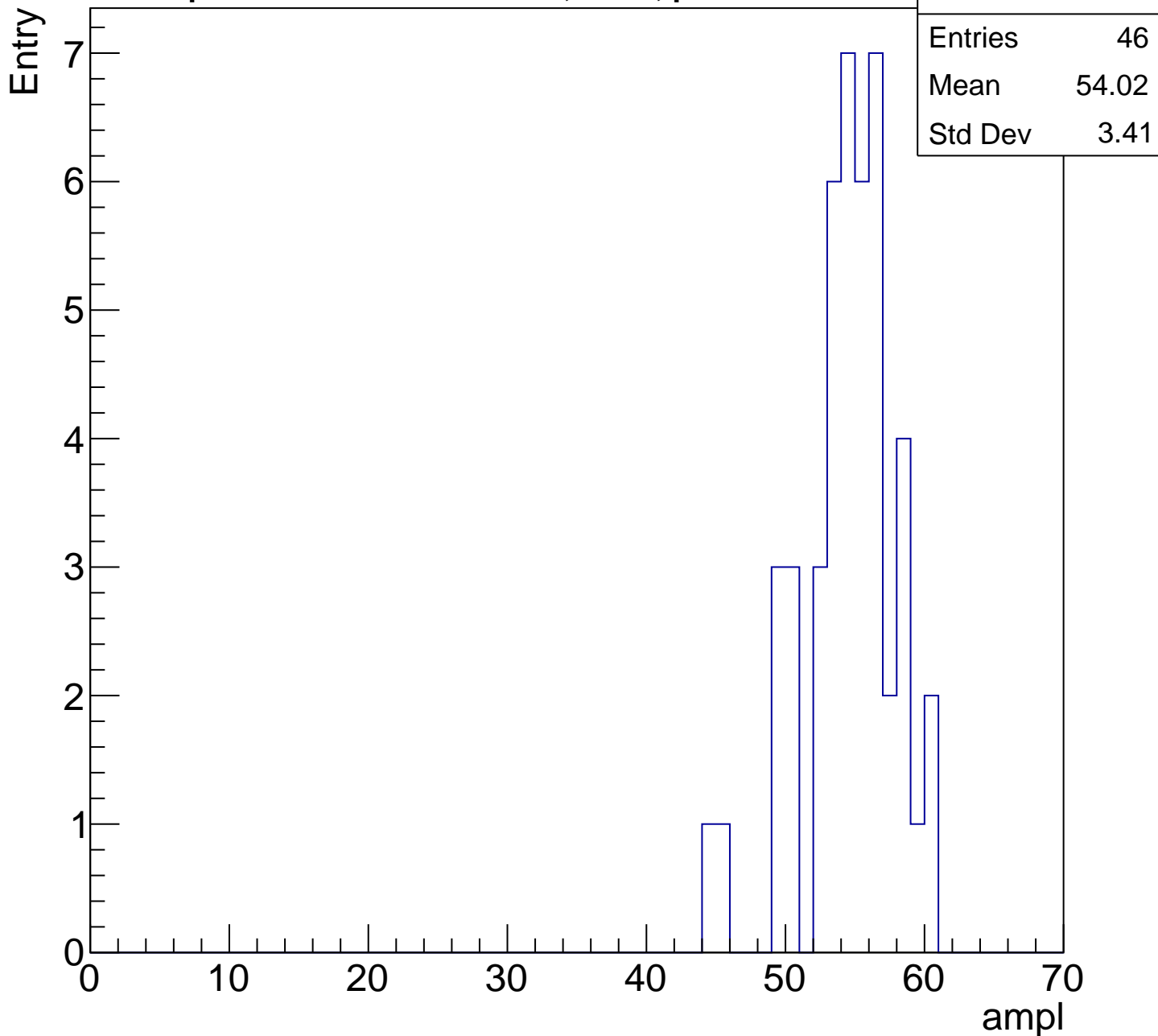
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch26, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

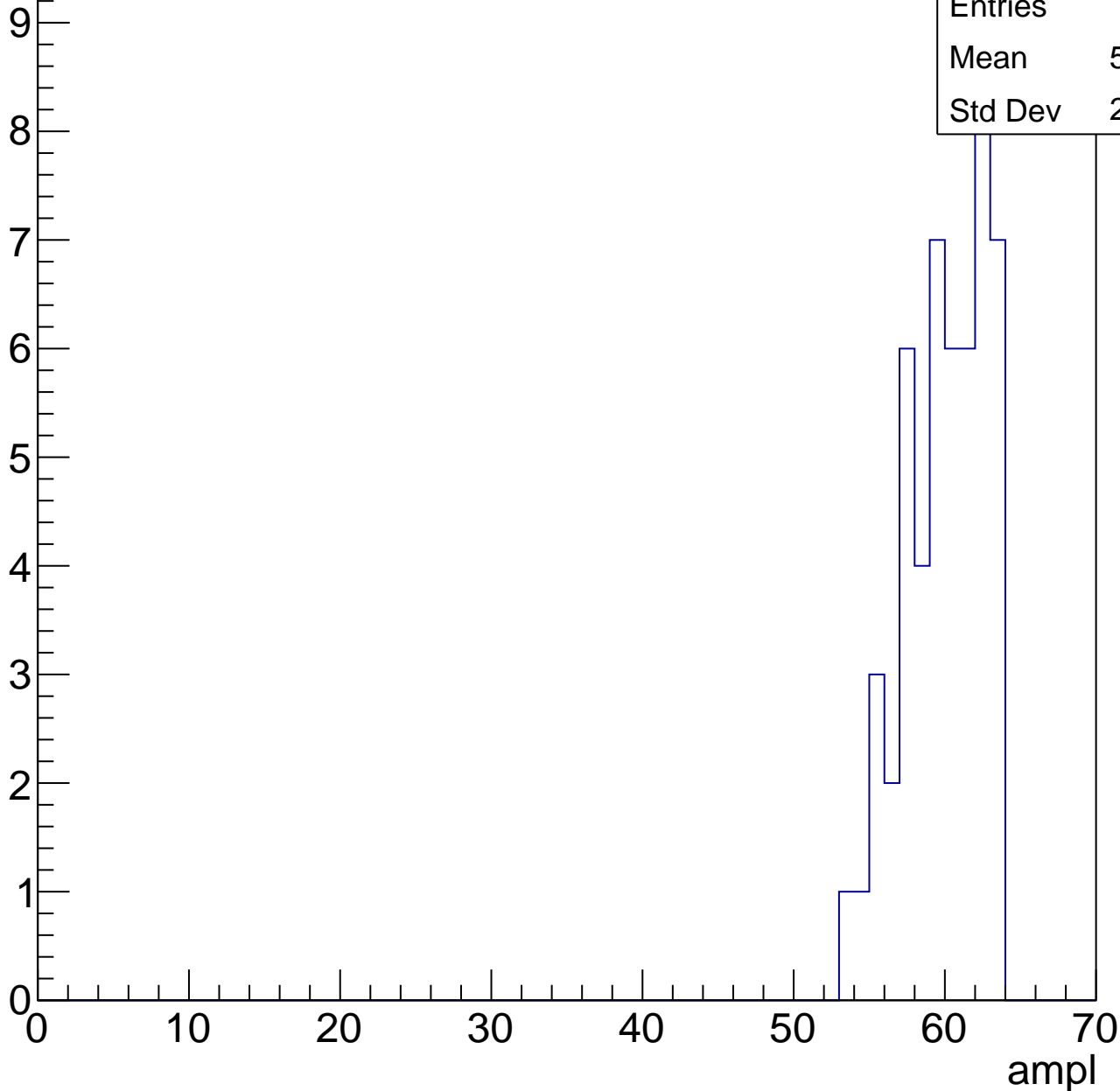


# B1L103S, U3-ch26, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

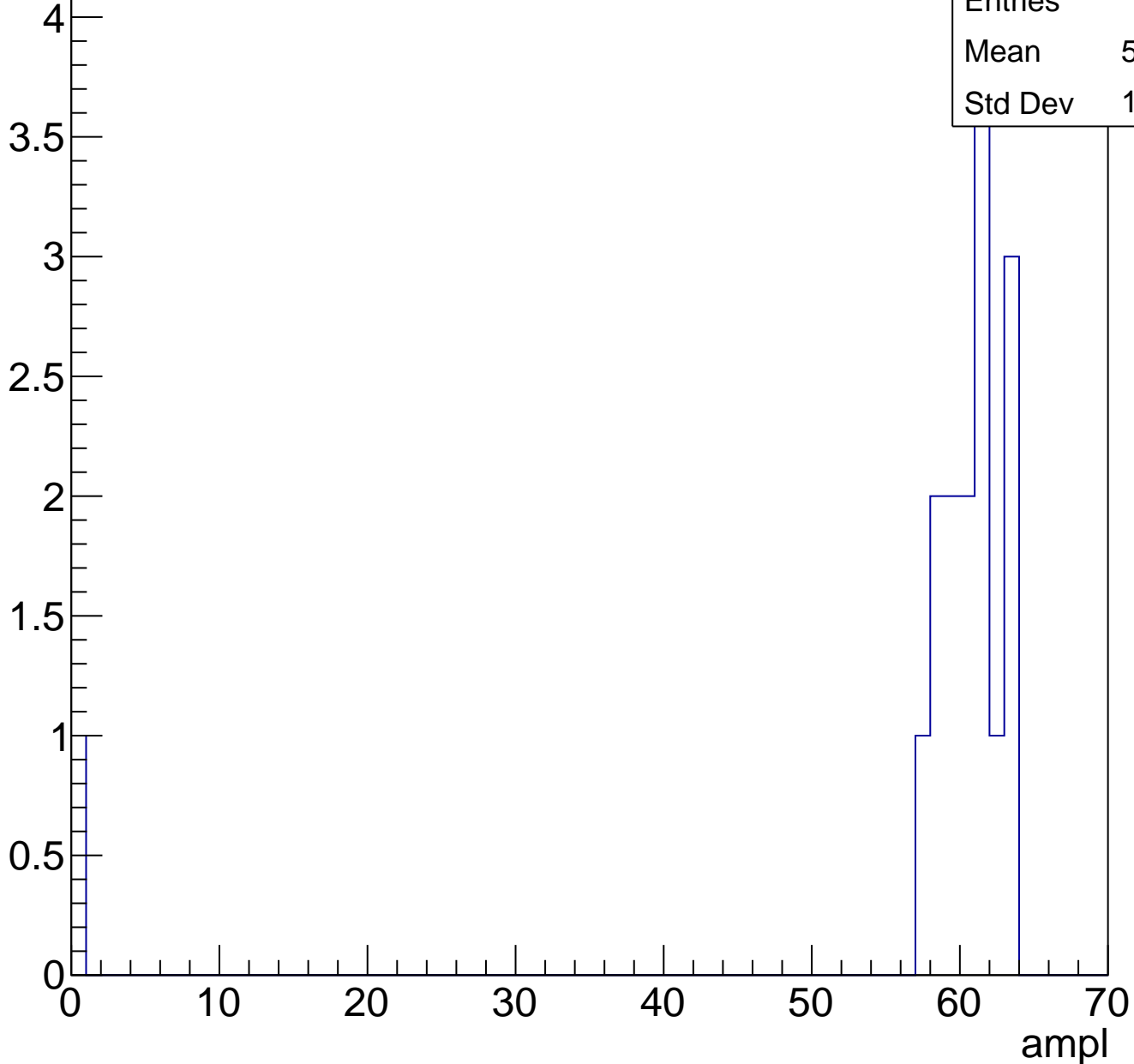
Entries	52
Mean	59.54
Std Dev	2.642



# B1L103S, U3-ch26, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U3-ch26, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U3-ch27, adc0

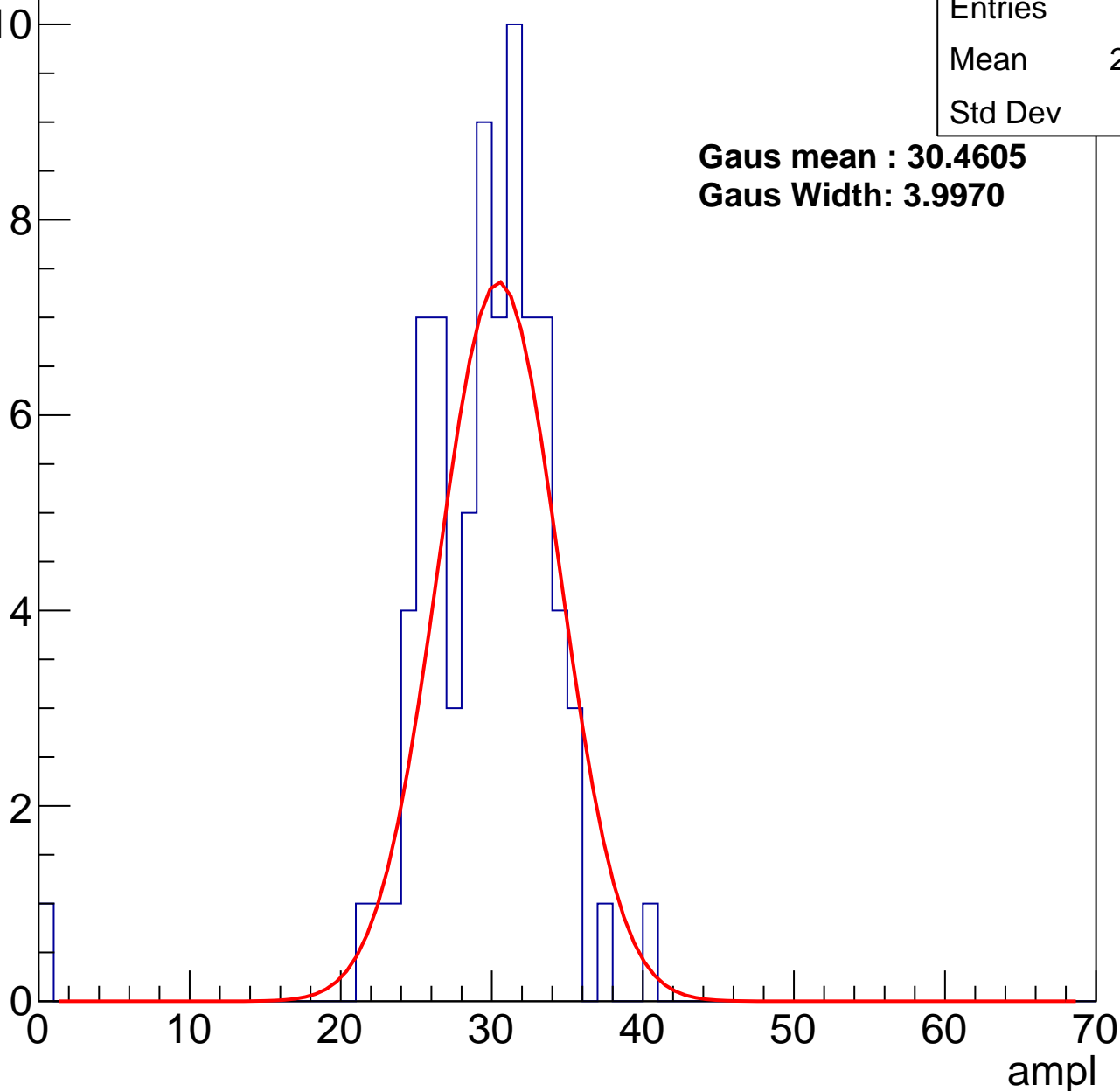
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	79
Mean	29.04
Std Dev	4.9

**Gaus mean : 30.4605**

**Gaus Width: 3.9970**



# B1L103S, U3-ch27, adc1

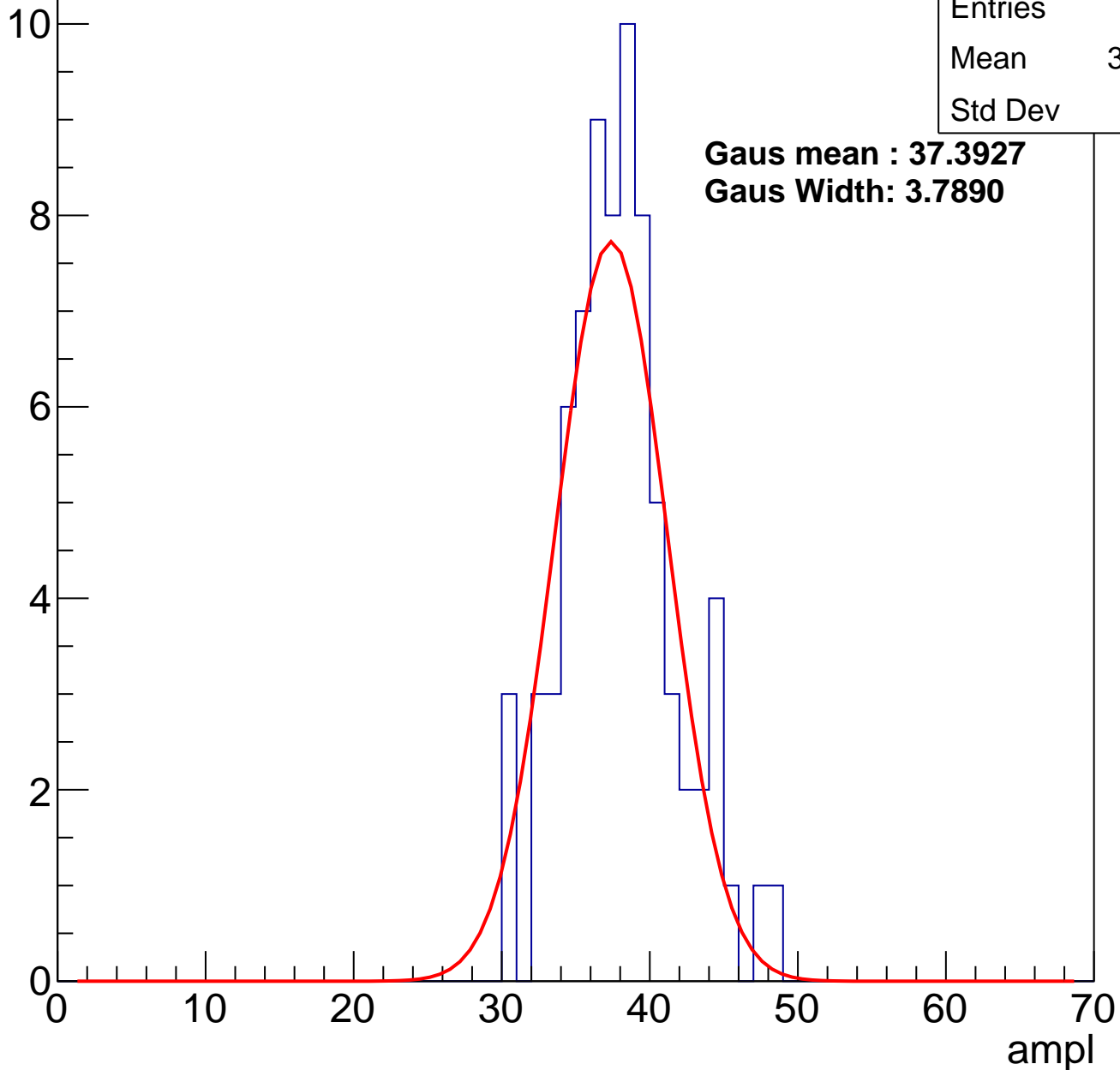
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	76
Mean	37.57
Std Dev	3.76

**Gaus mean : 37.3927**

**Gaus Width: 3.7890**

Entry



# B1L103S, U3-ch27, adc2

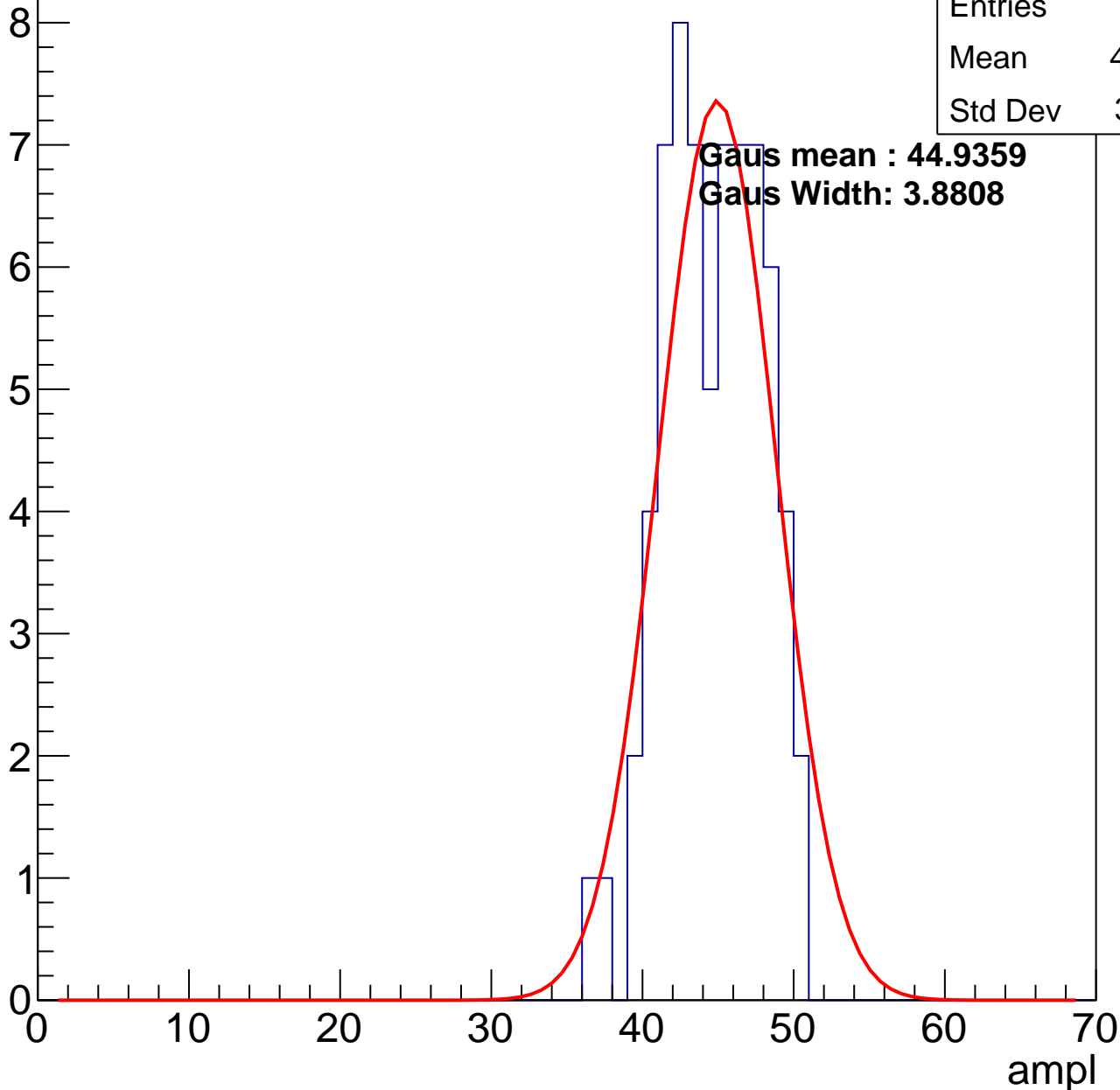
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	44.19
Std Dev	3.191

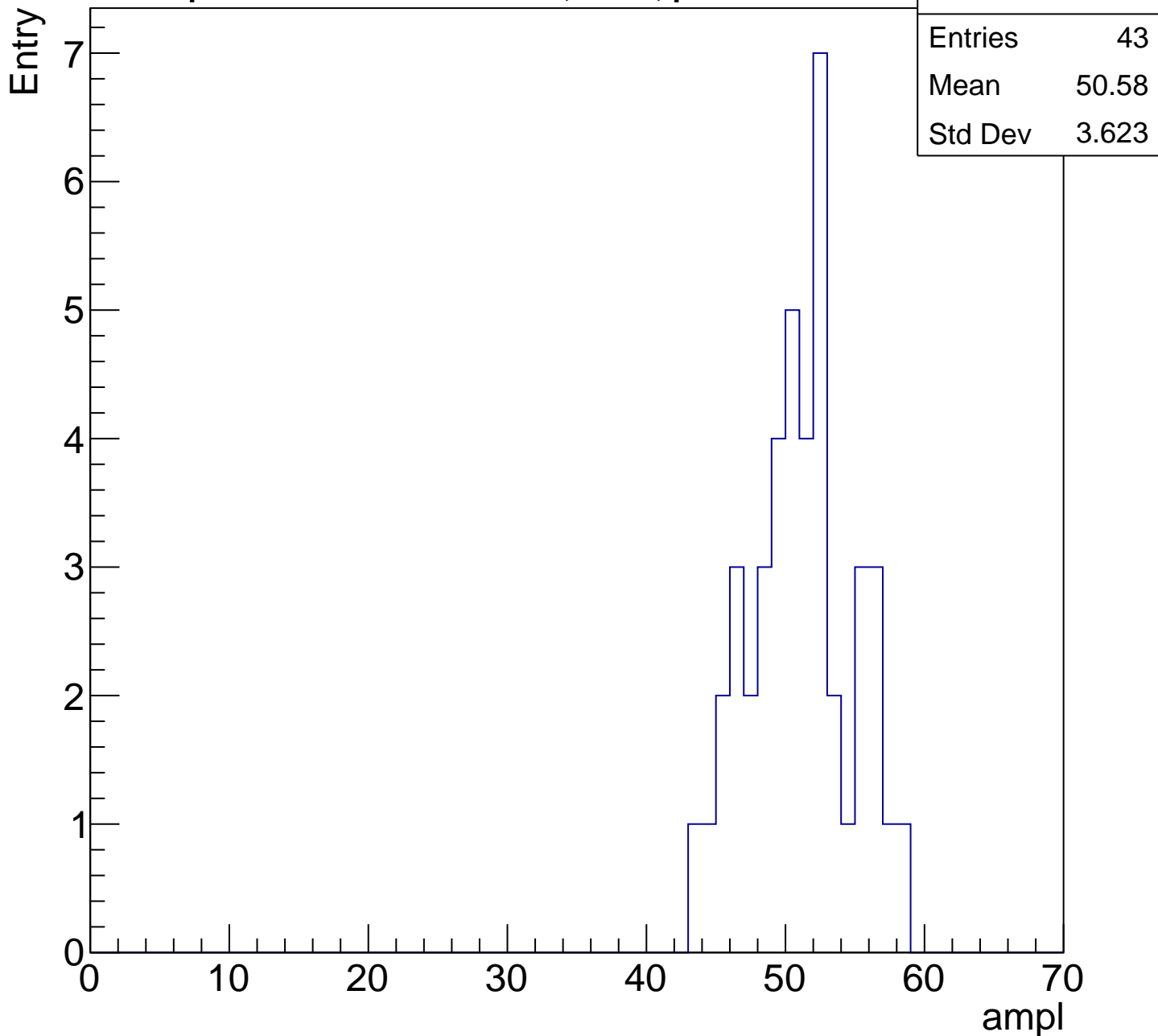
**Gaus mean : 44.9359**

**Gaus Width: 3.8808**



# B1L103S, U3-ch27, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

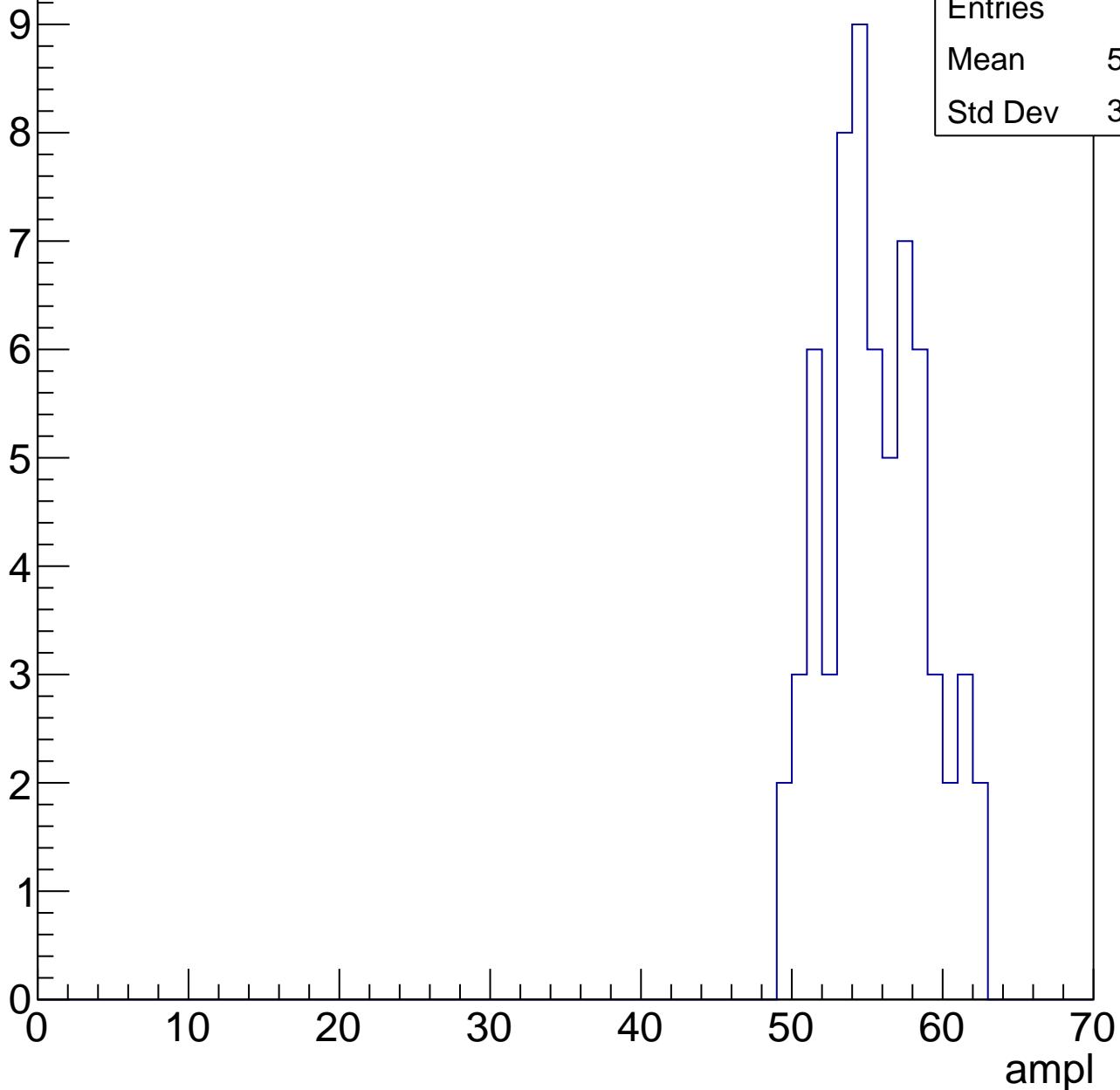


# B1L103S, U3-ch27, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	55.09
Std Dev	3.285



# B1L103S, U3-ch27, adc5

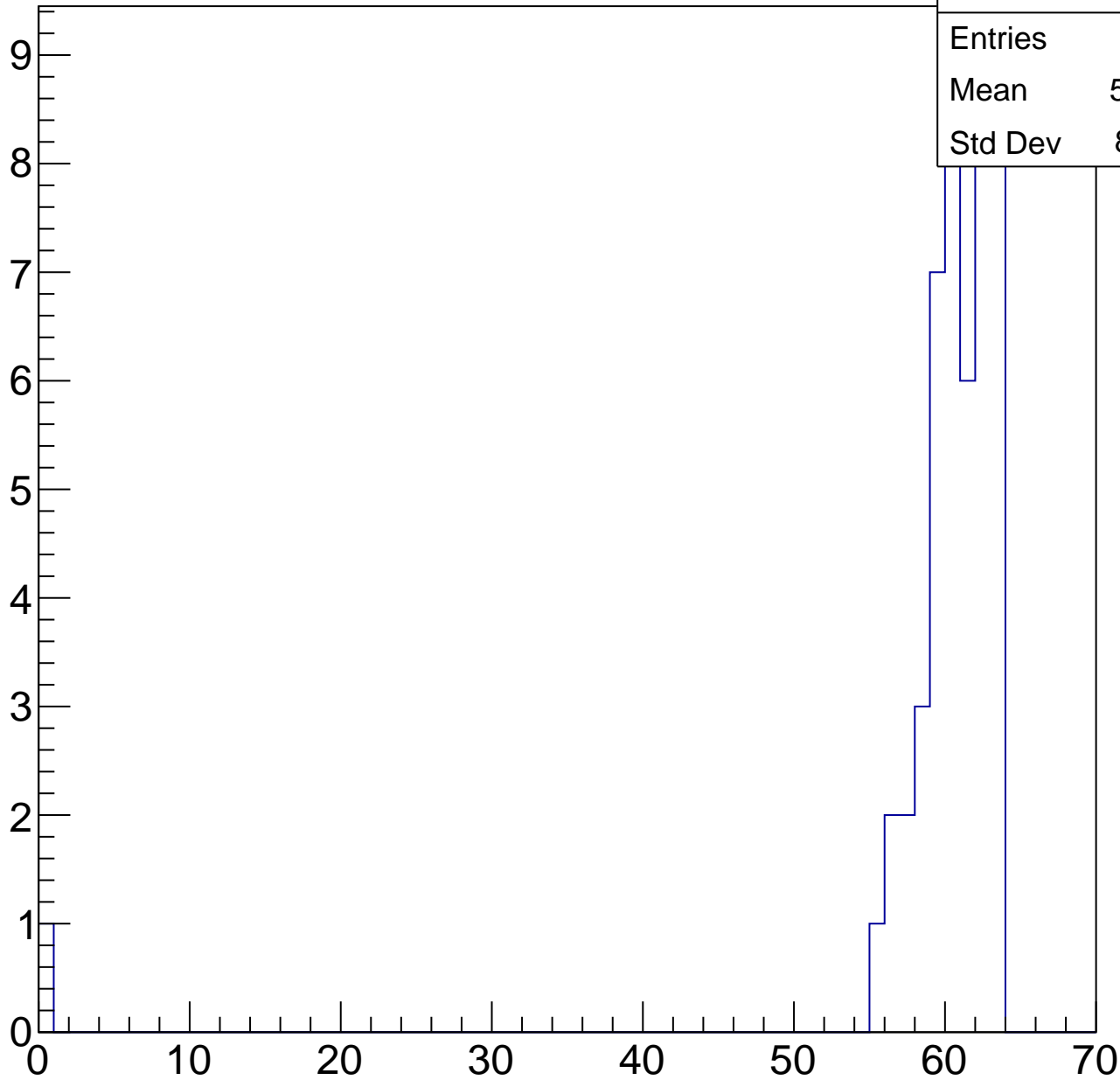
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	47
Mean	59.09
Std Dev	8.961

ampl



# B1L103S, U3-ch27, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

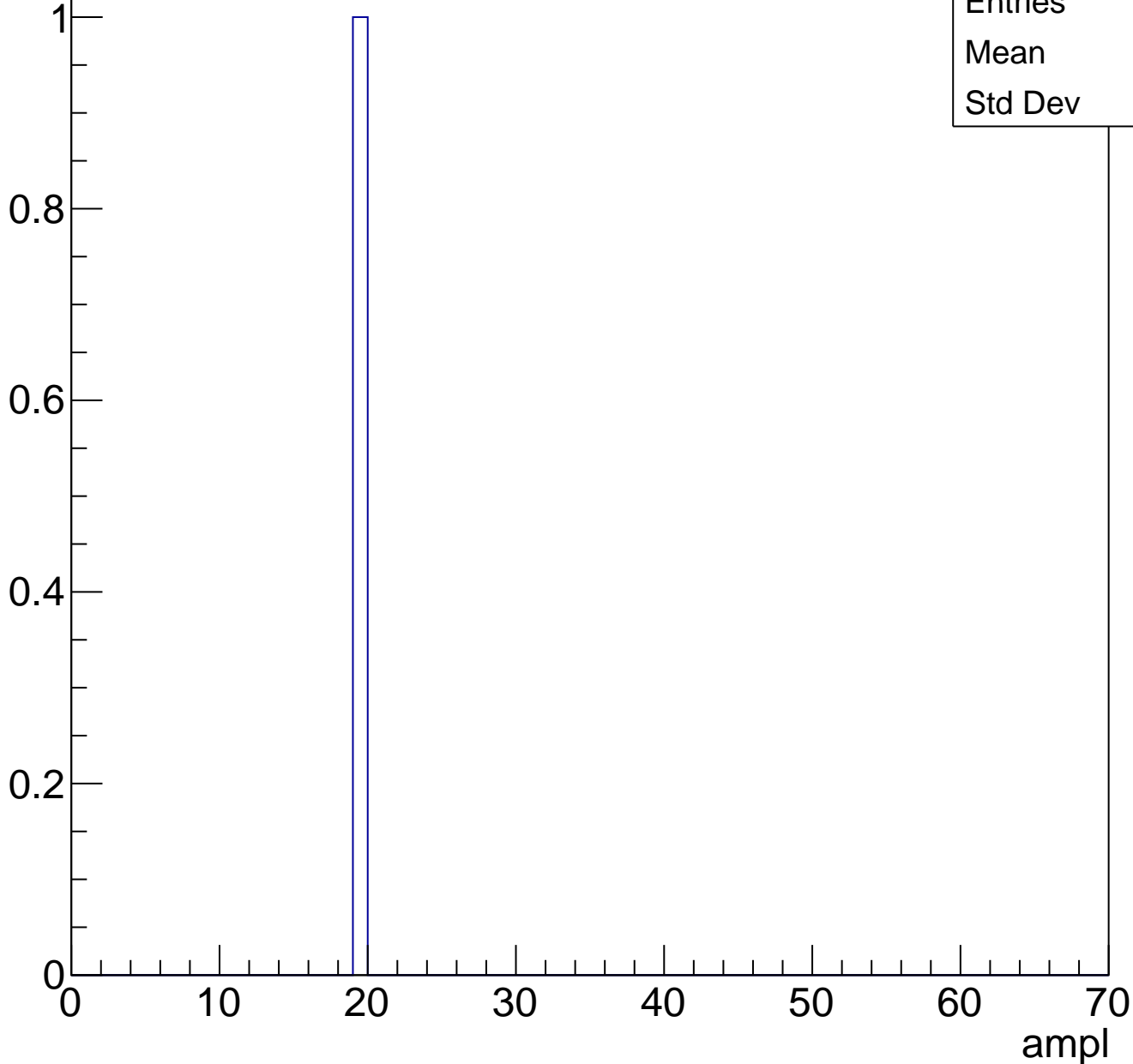




# B1L103S, U3-ch27, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch28, adc0

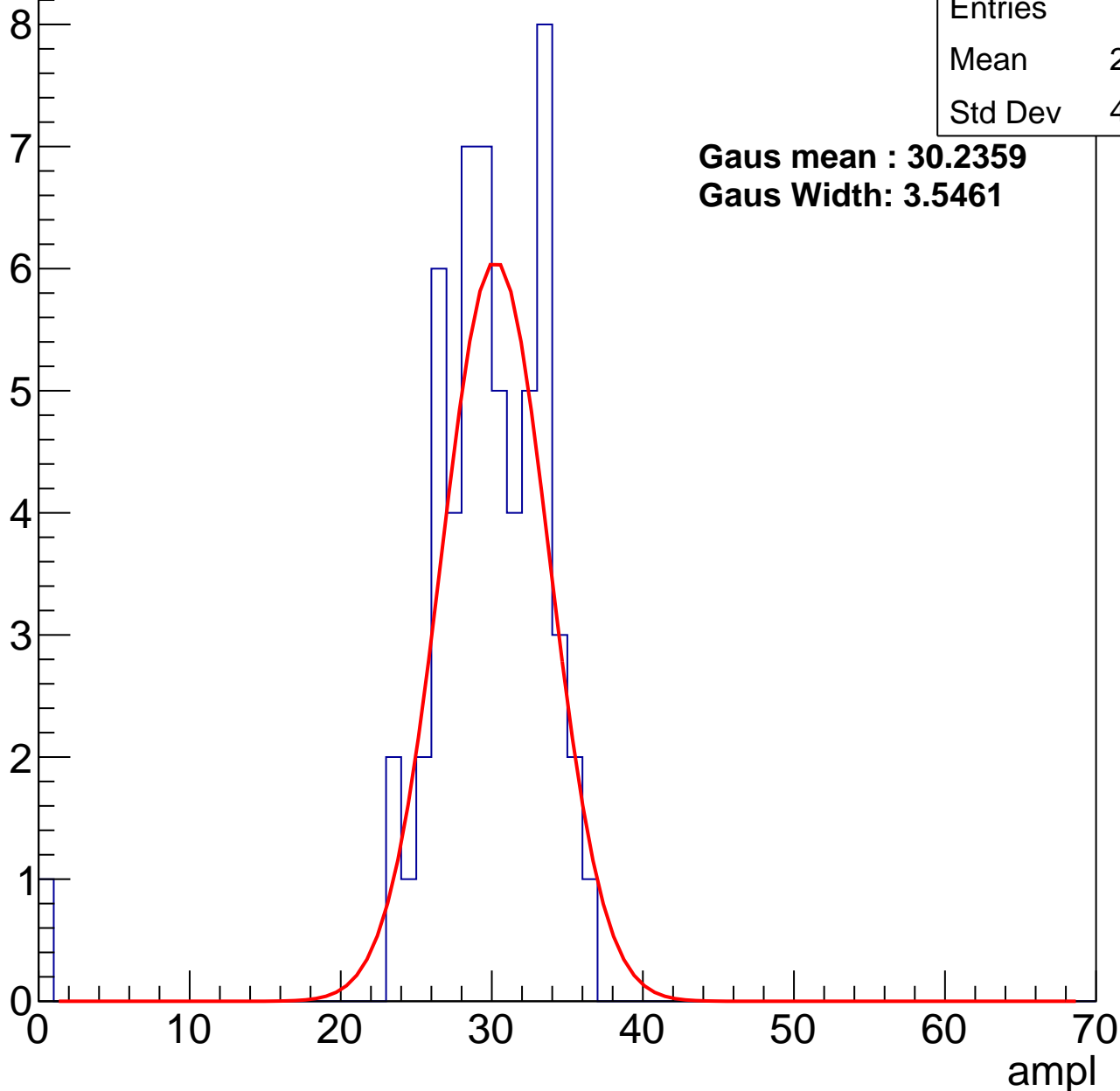
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	29.12
Std Dev	4.976

**Gaus mean : 30.2359**

**Gaus Width: 3.5461**



# B1L103S, U3-ch28, adc1

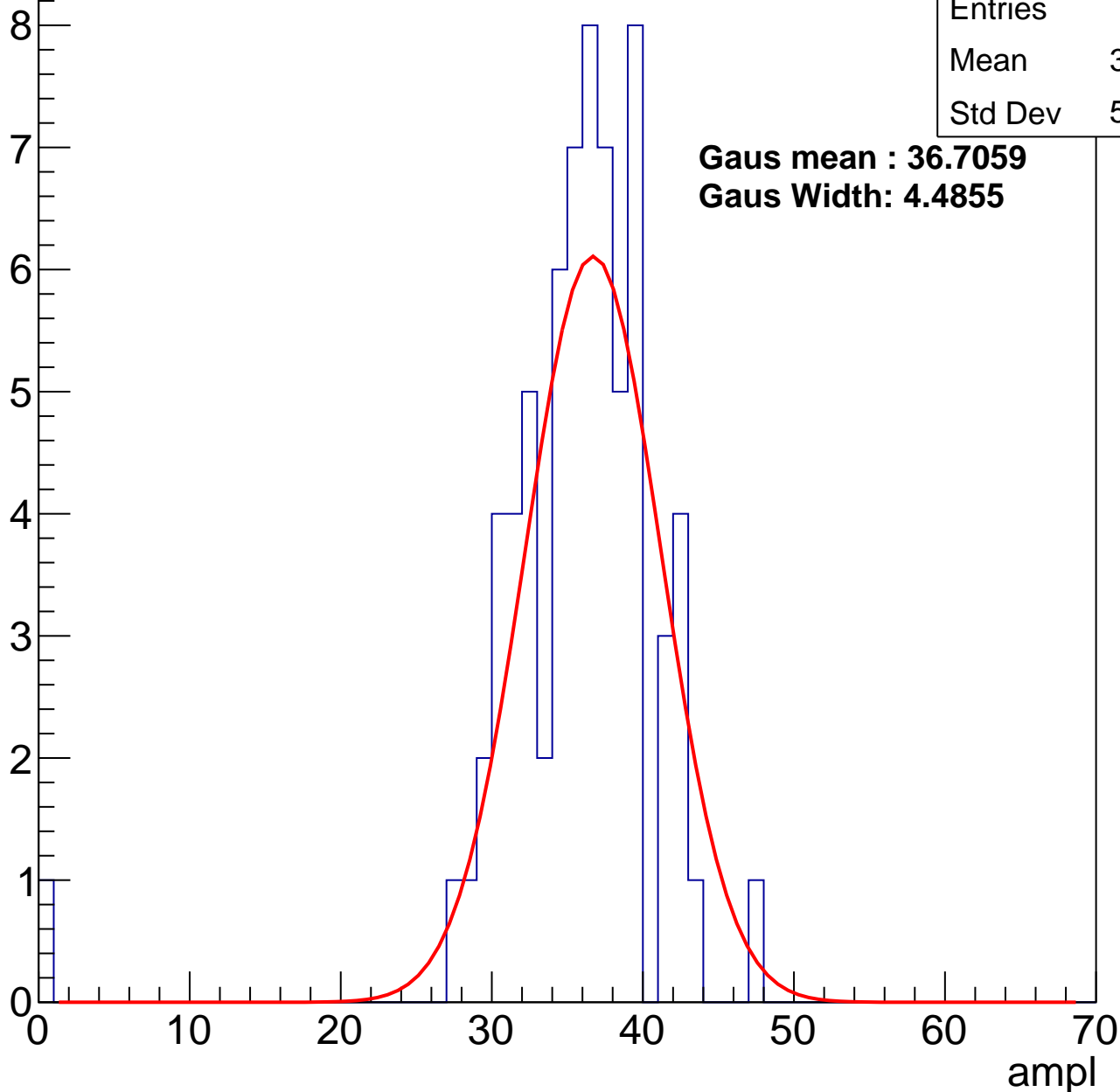
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	35.17
Std Dev	5.796

**Gaus mean : 36.7059**

**Gaus Width: 4.4855**



# B1L103S, U3-ch28, adc2

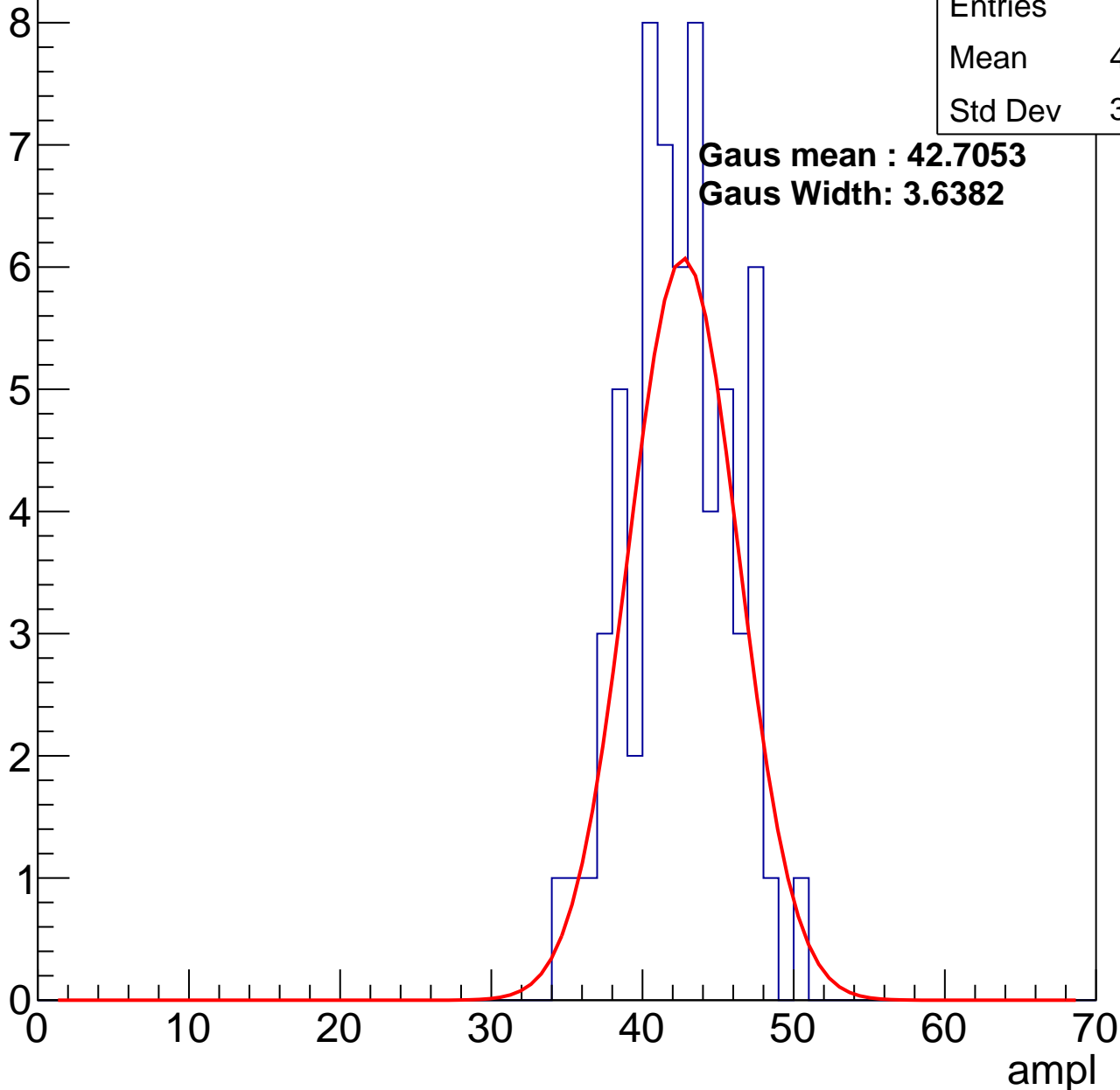
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	42.03
Std Dev	3.426

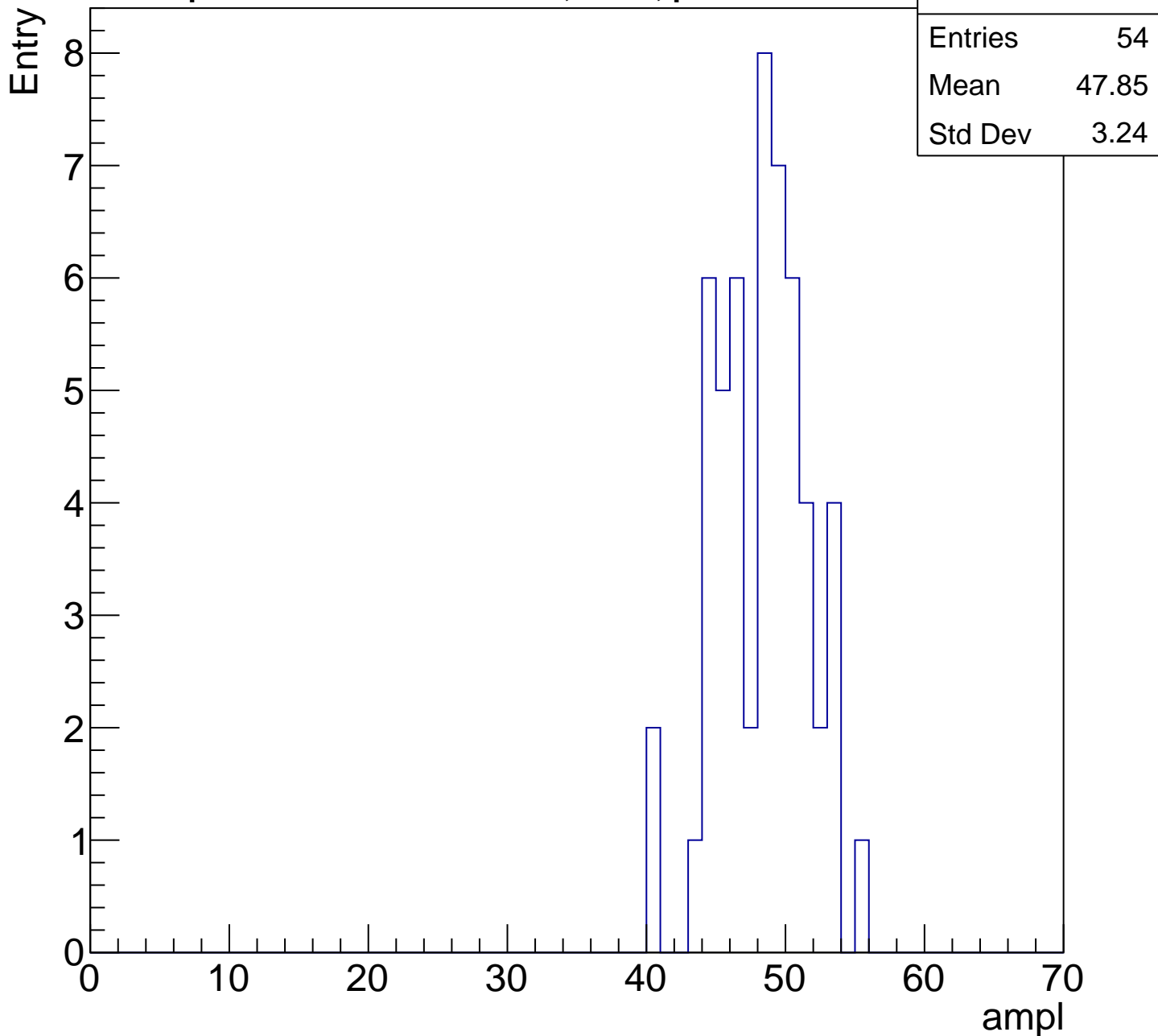
**Gaus mean : 42.7053**

**Gaus Width: 3.6382**



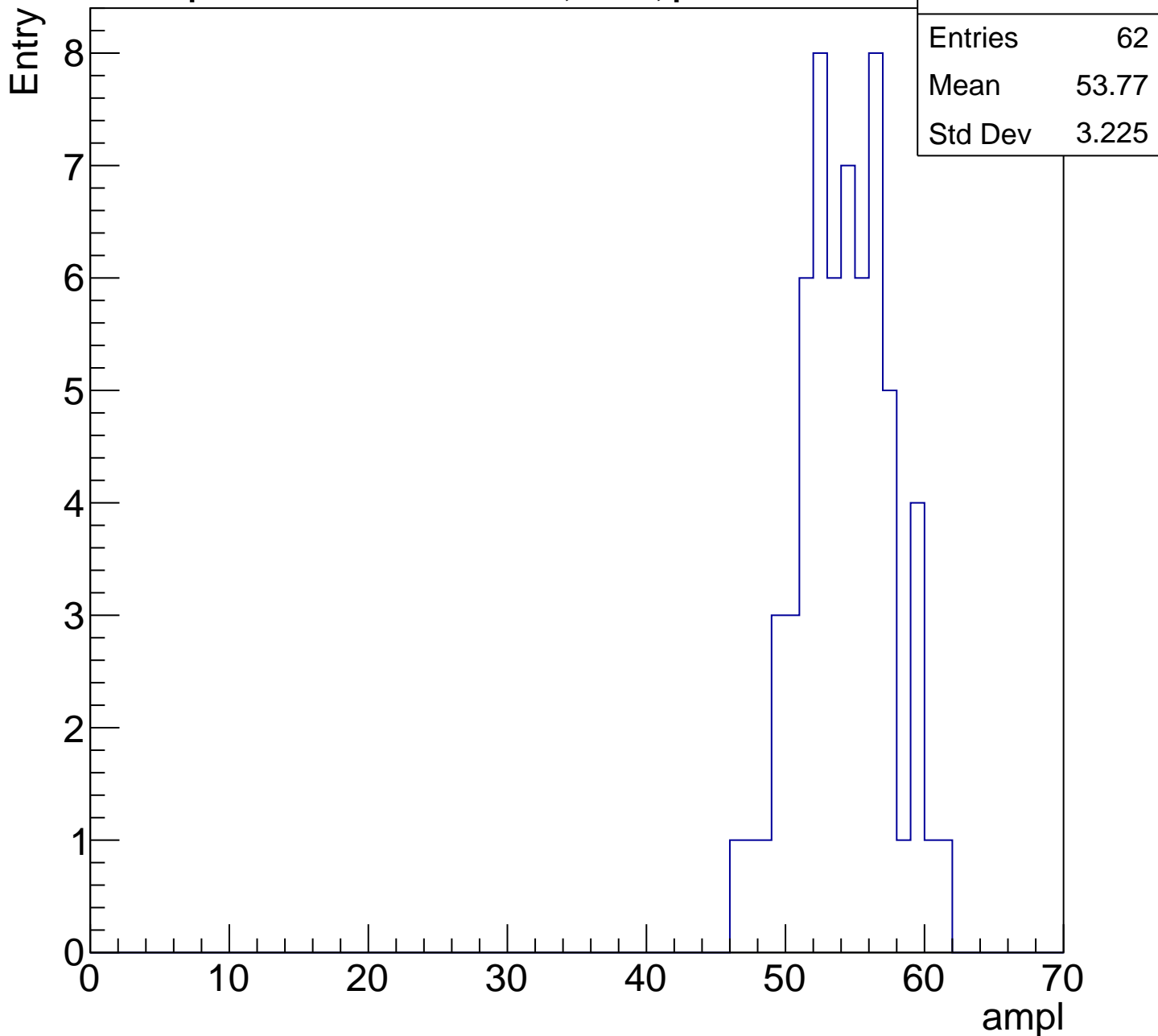
# B1L103S, U3-ch28, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U3-ch28, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U3-ch28, adc5

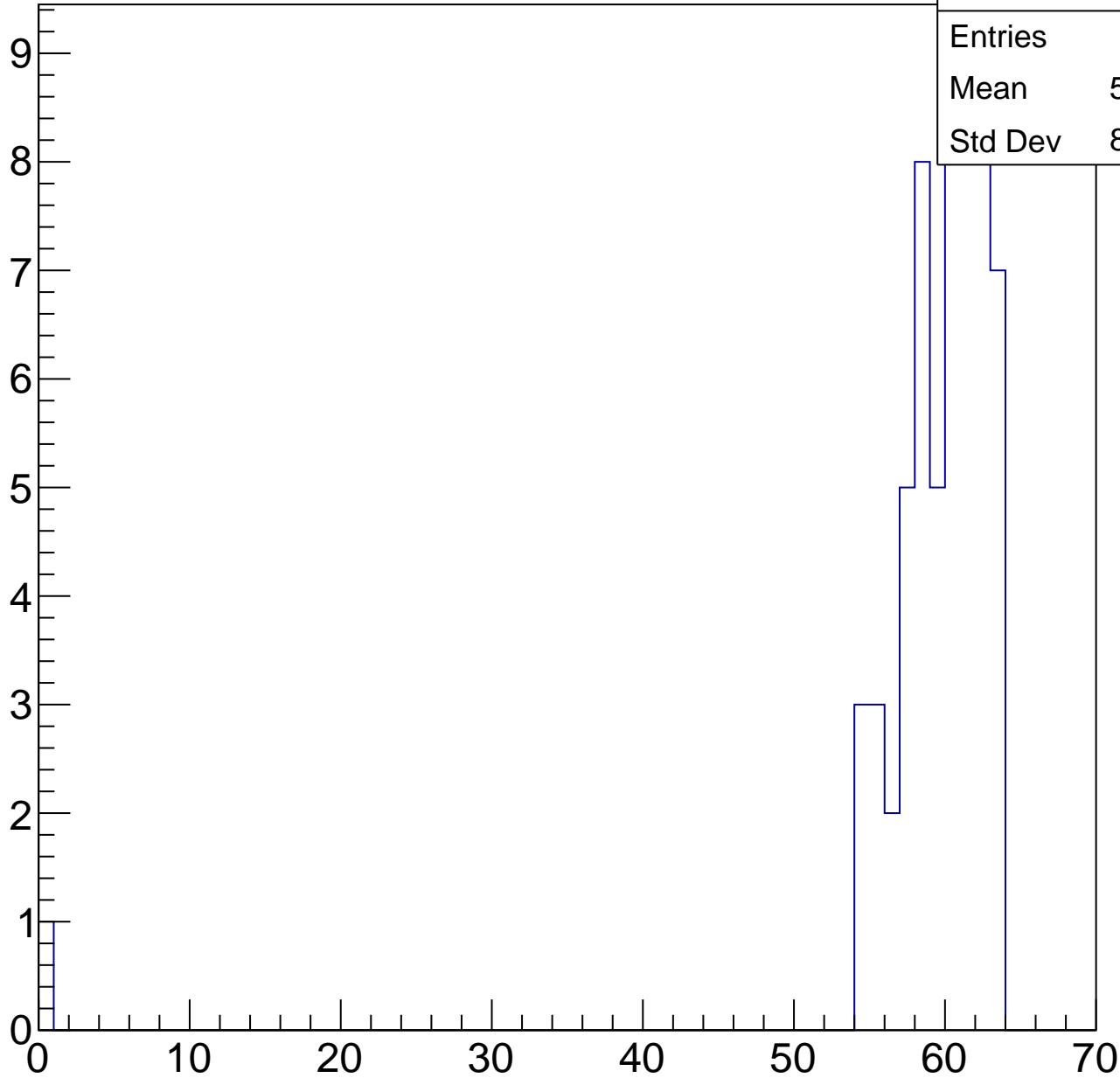
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	59
Mean	58.46
Std Dev	8.089

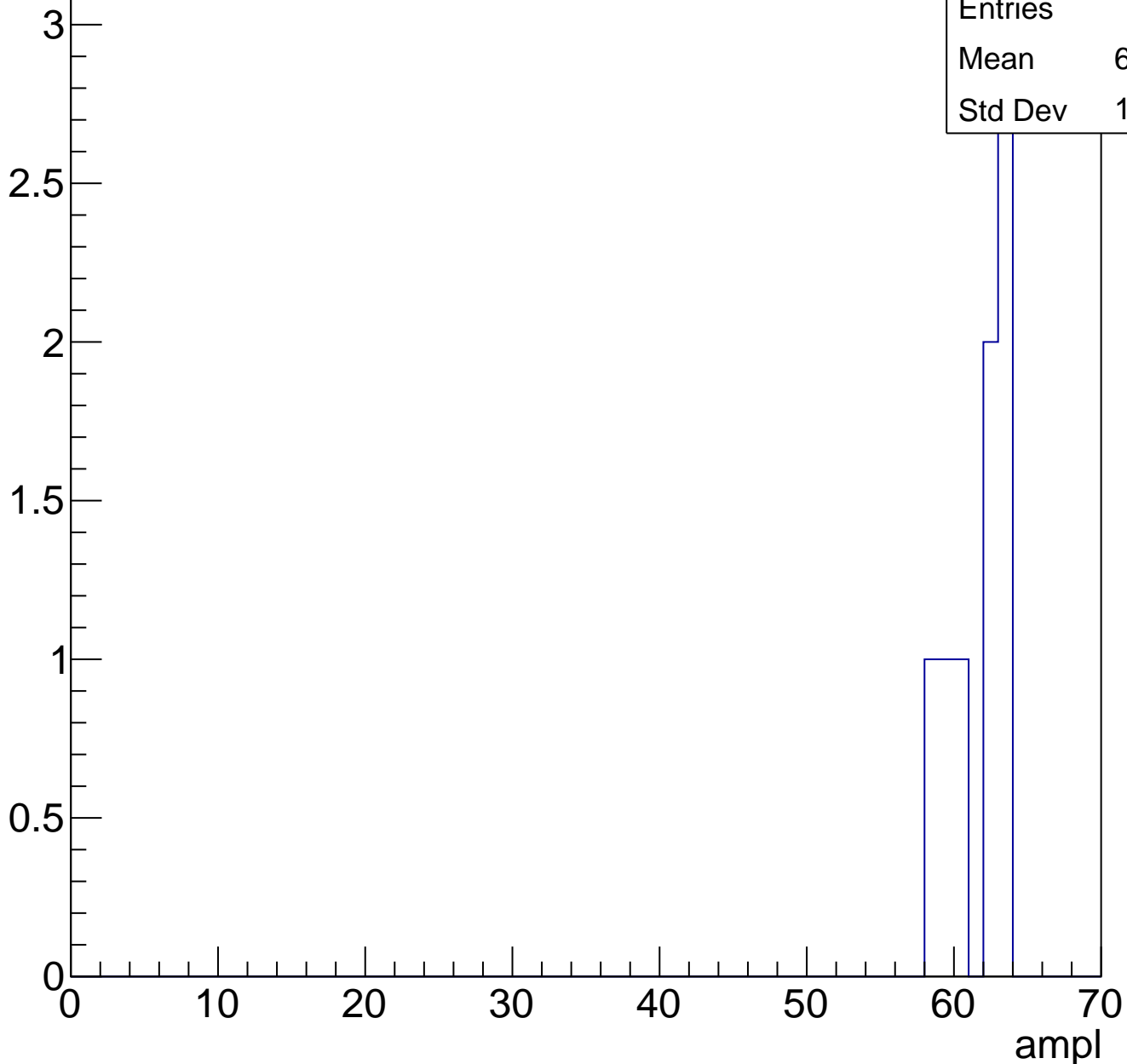
ampl



# B1L103S, U3-ch28, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U3-ch28, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U3-ch29, adc0

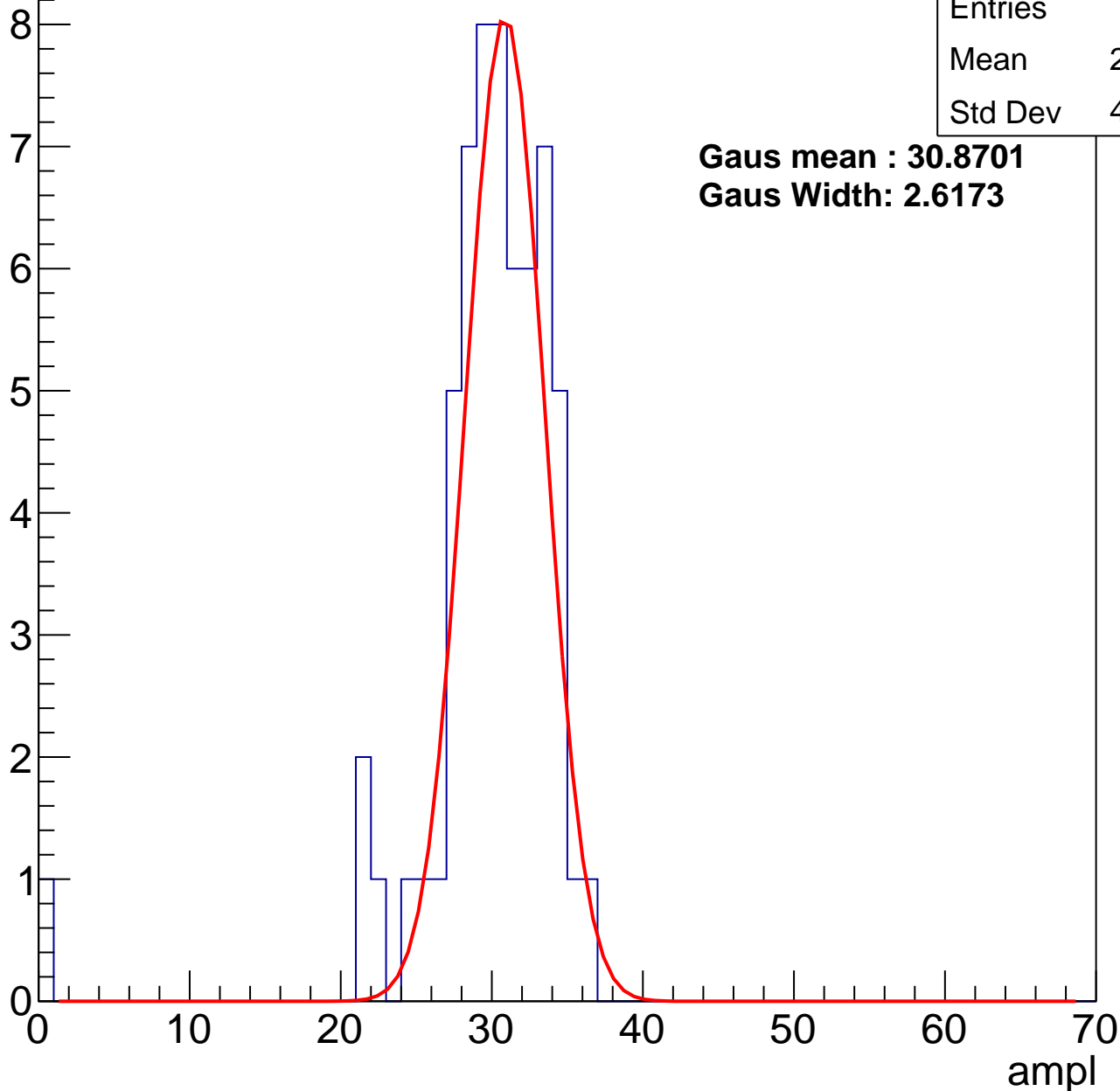
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	29.38
Std Dev	4.949

**Gaus mean : 30.8701**

**Gaus Width: 2.6173**



# B1L103S, U3-ch29, adc1

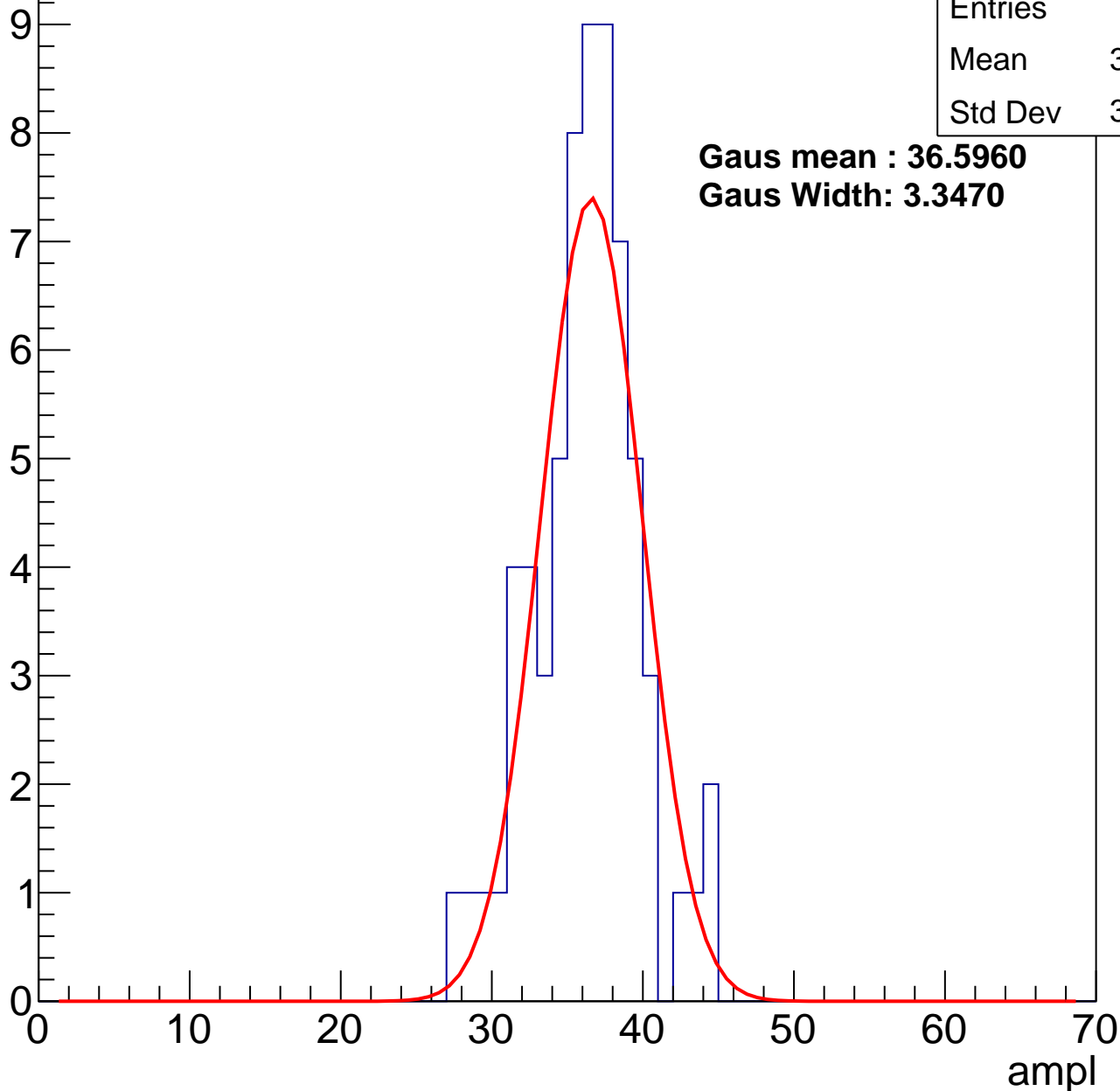
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	35.78
Std Dev	3.484

**Gaus mean : 36.5960**

**Gaus Width: 3.3470**



# B1L103S, U3-ch29, adc2

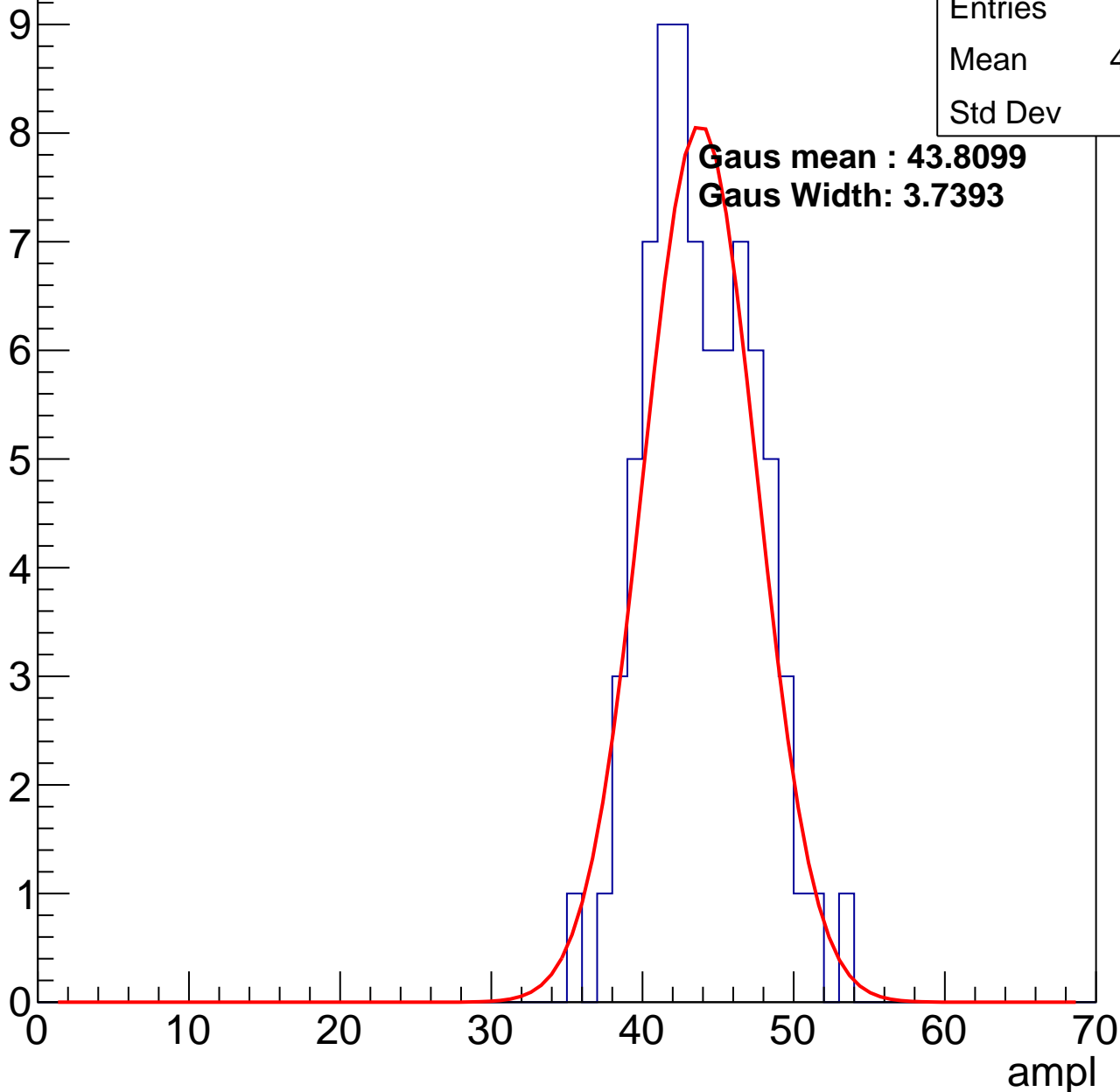
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	43.44
Std Dev	3.55

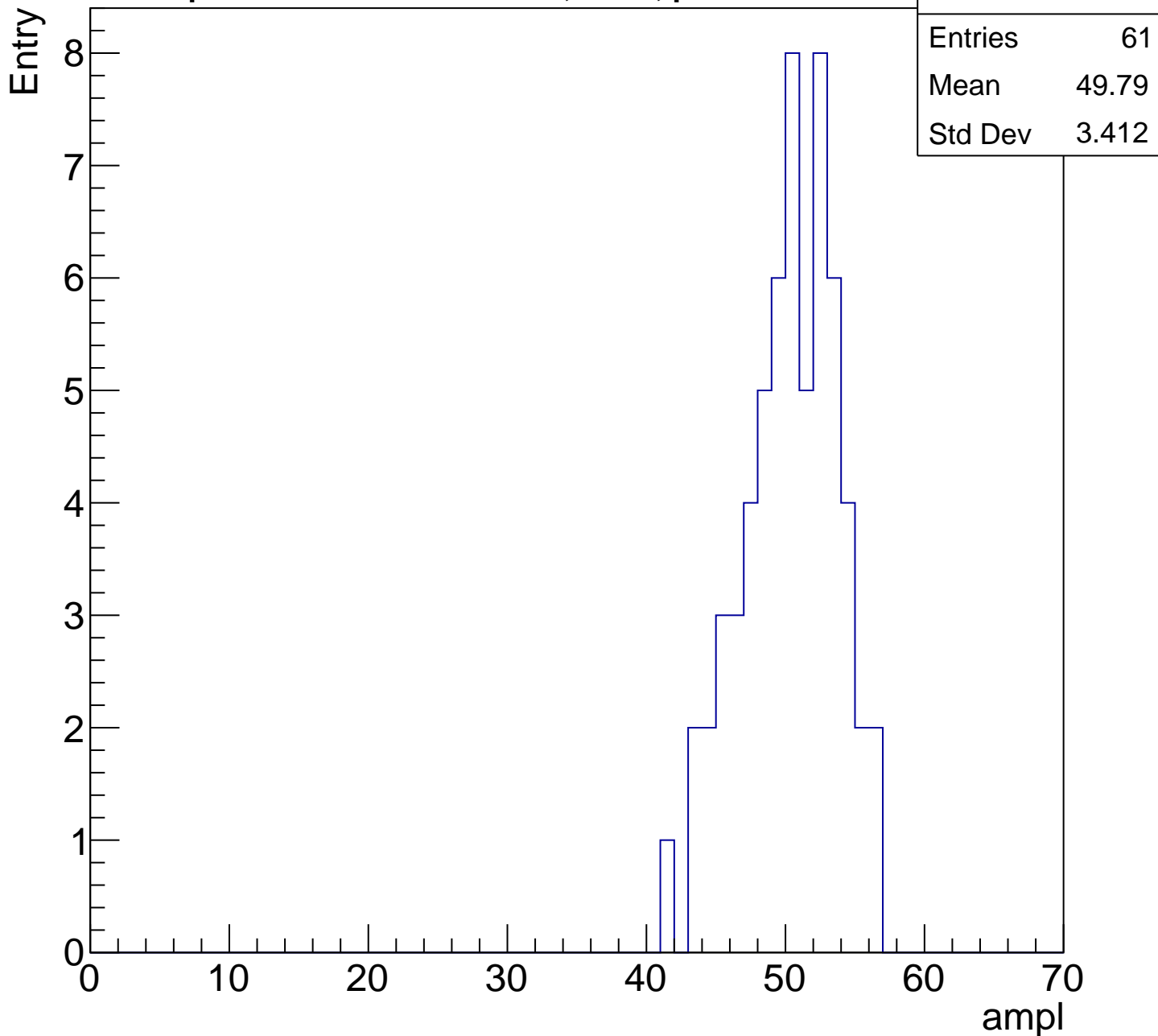
**Gaus mean : 43.8099**

**Gaus Width: 3.7393**



# B1L103S, U3-ch29, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

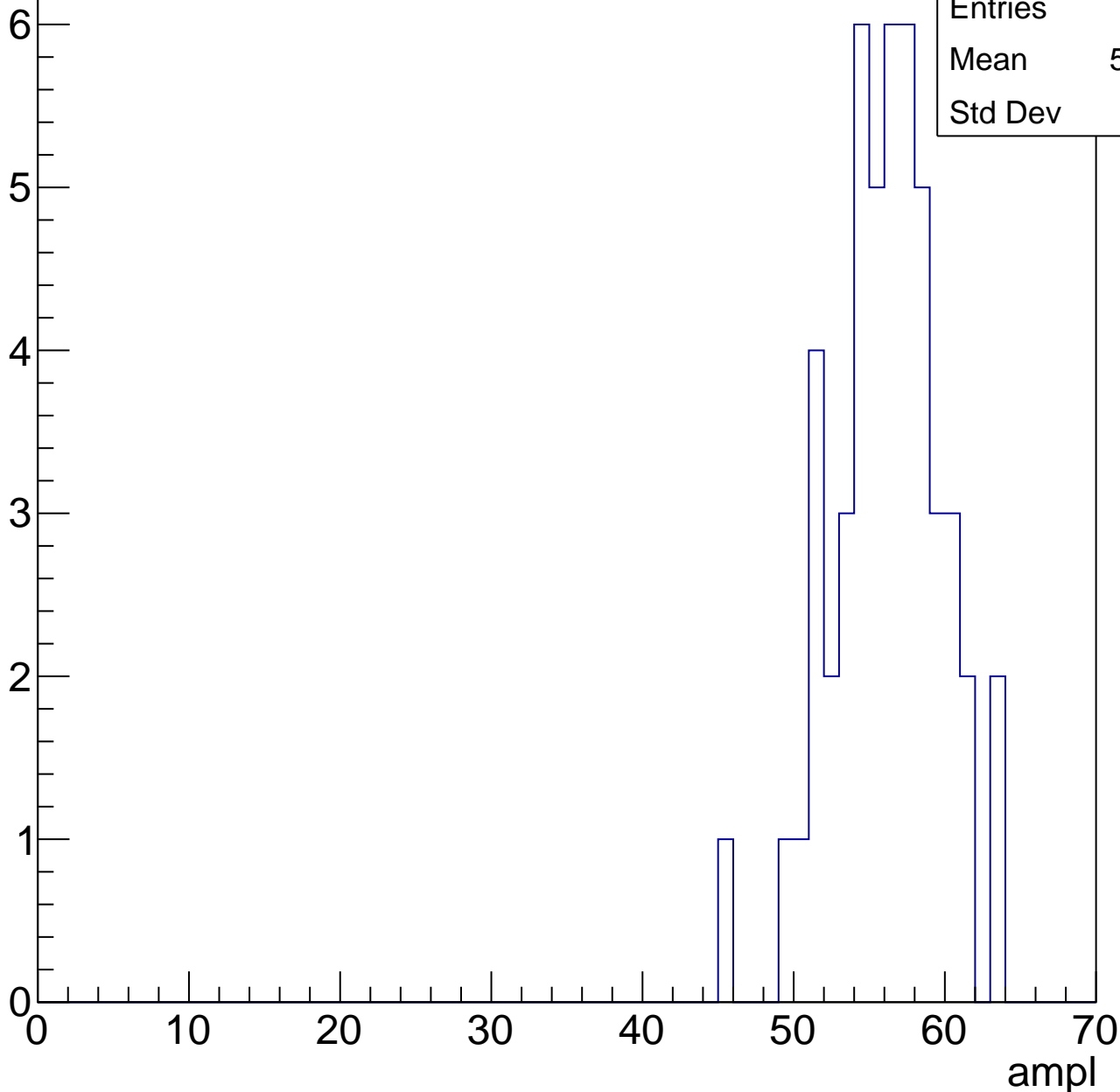


# B1L103S, U3-ch29, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

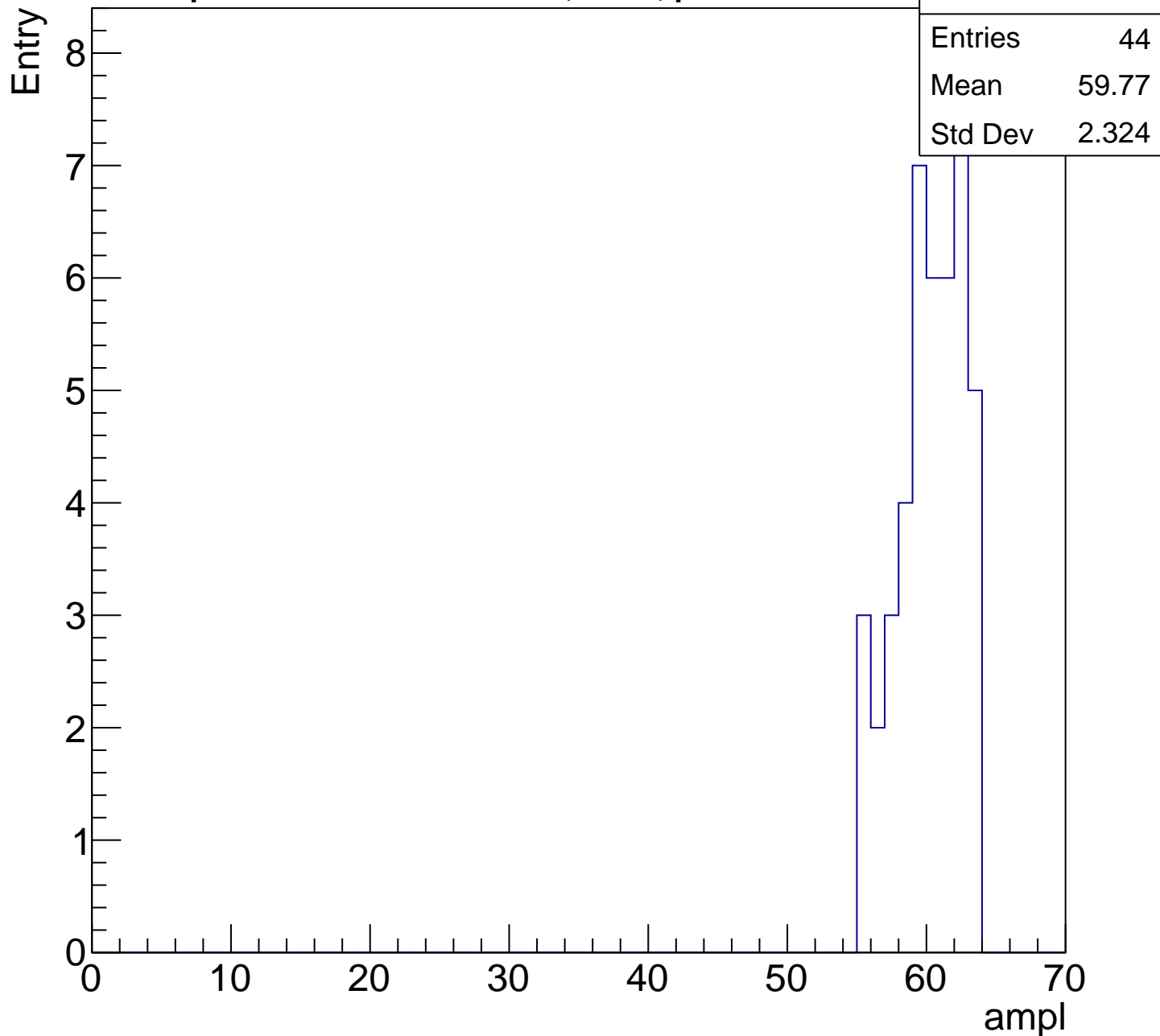
Entry

Entries	50
Mean	55.66
Std Dev	3.57



# B1L103S, U3-ch29, adc5

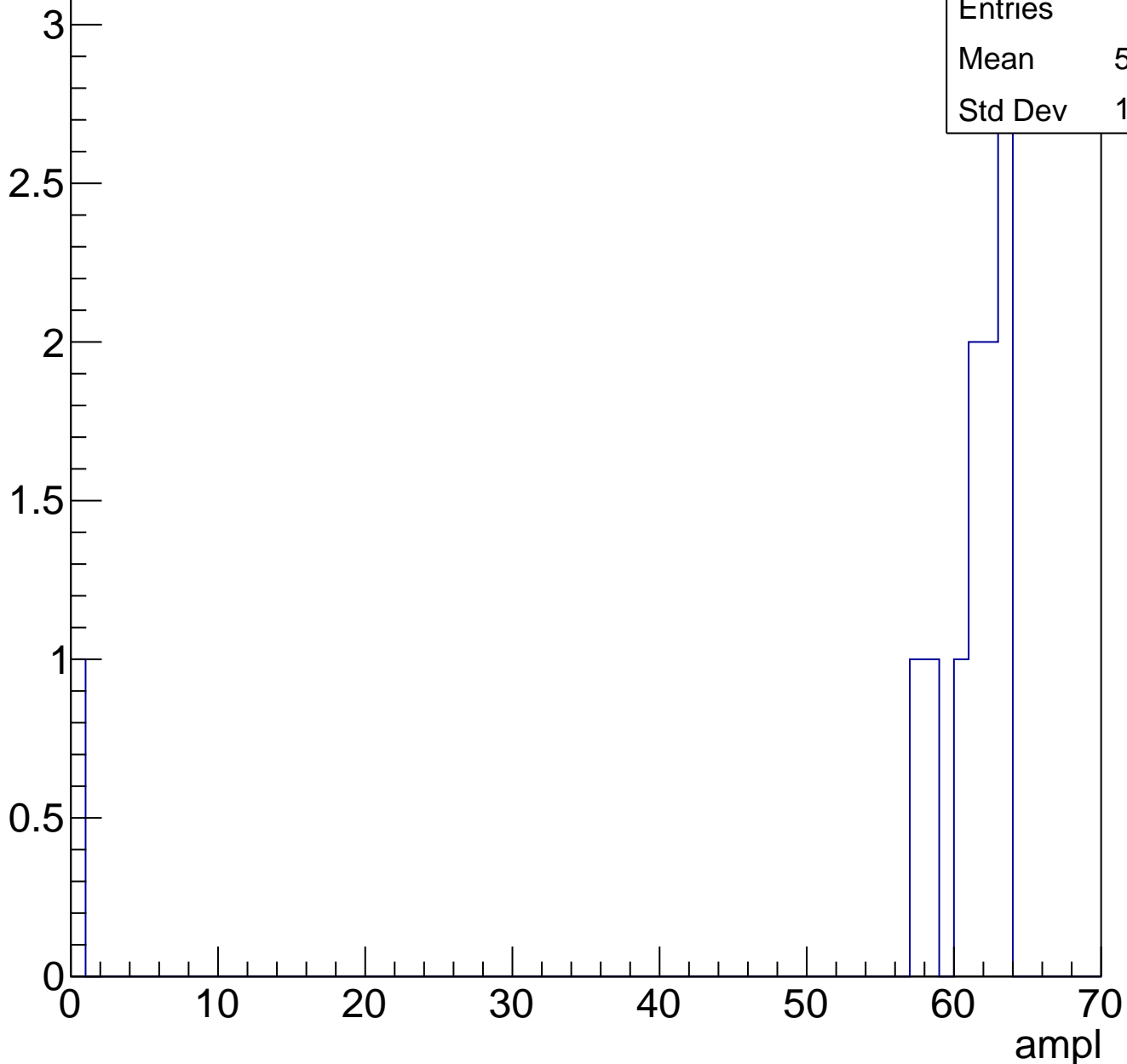
calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U3-ch29, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U3-ch29, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U3-ch30, adc0

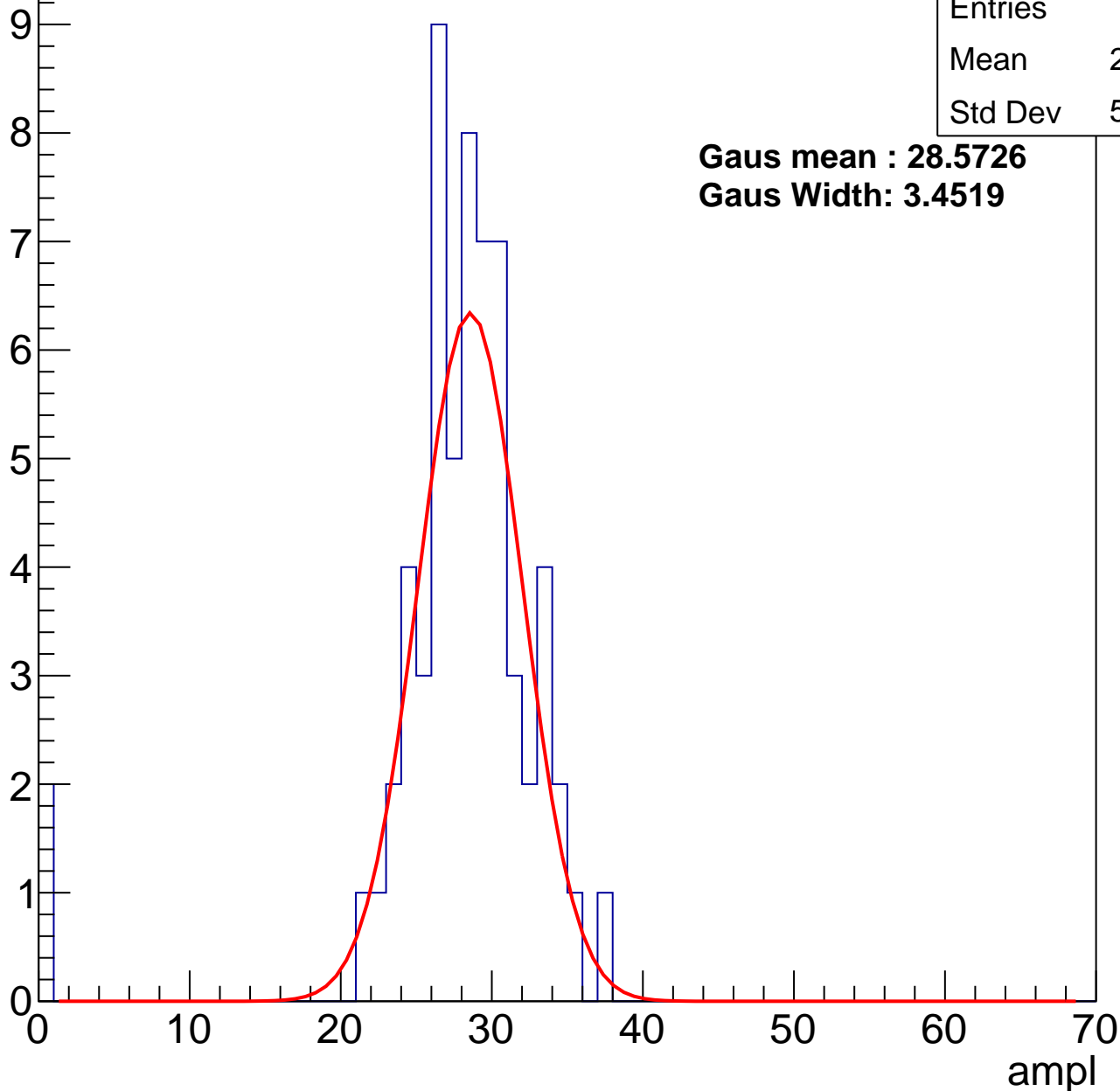
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	27.34
Std Dev	5.962

**Gaus mean : 28.5726**

**Gaus Width: 3.4519**



# B1L103S, U3-ch30, adc1

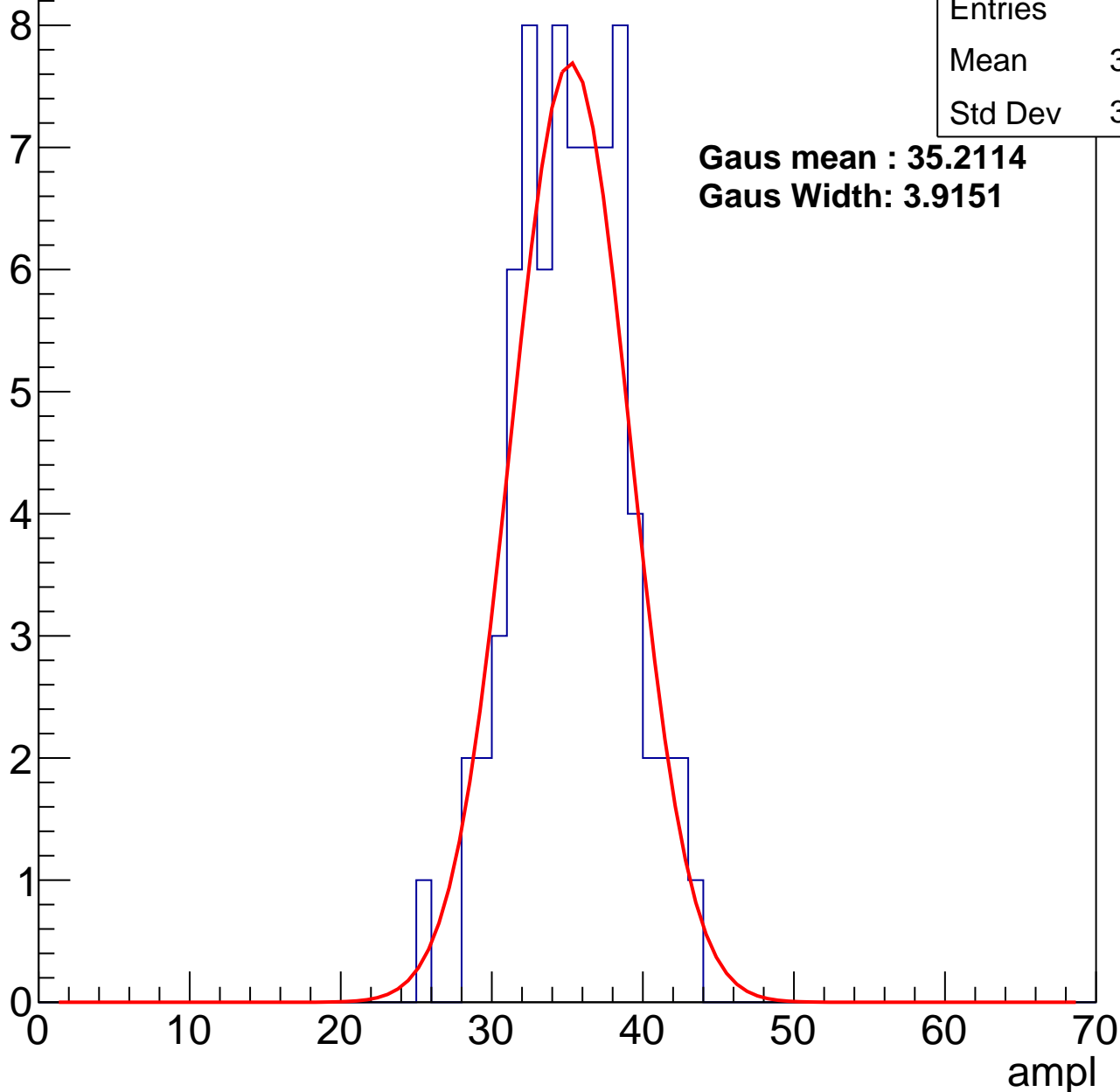
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	34.82
Std Dev	3.623

**Gaus mean : 35.2114**

**Gaus Width: 3.9151**



# B1L103S, U3-ch30, adc2

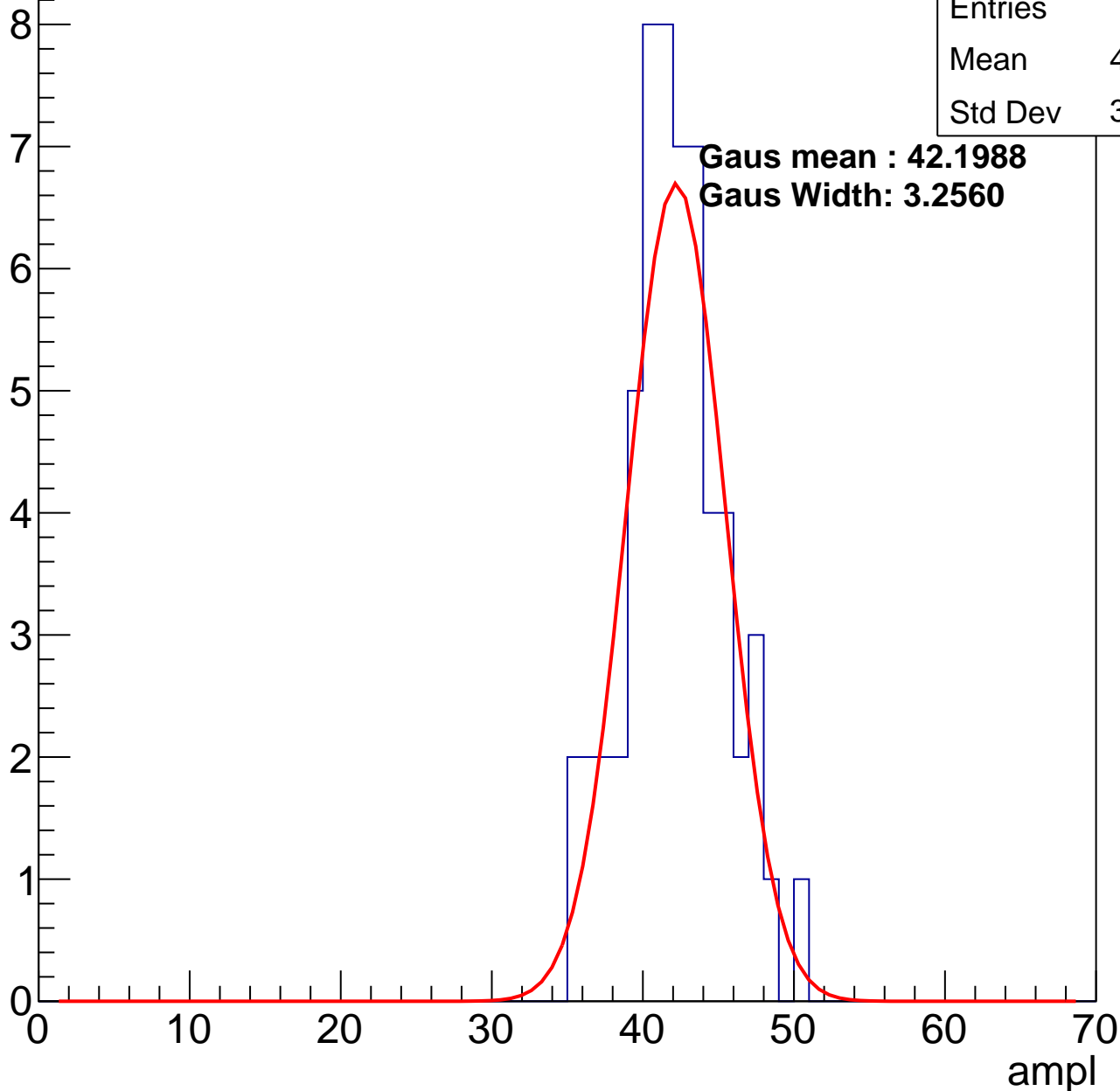
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	41.67
Std Dev	3.208

**Gaus mean : 42.1988**

**Gaus Width: 3.2560**

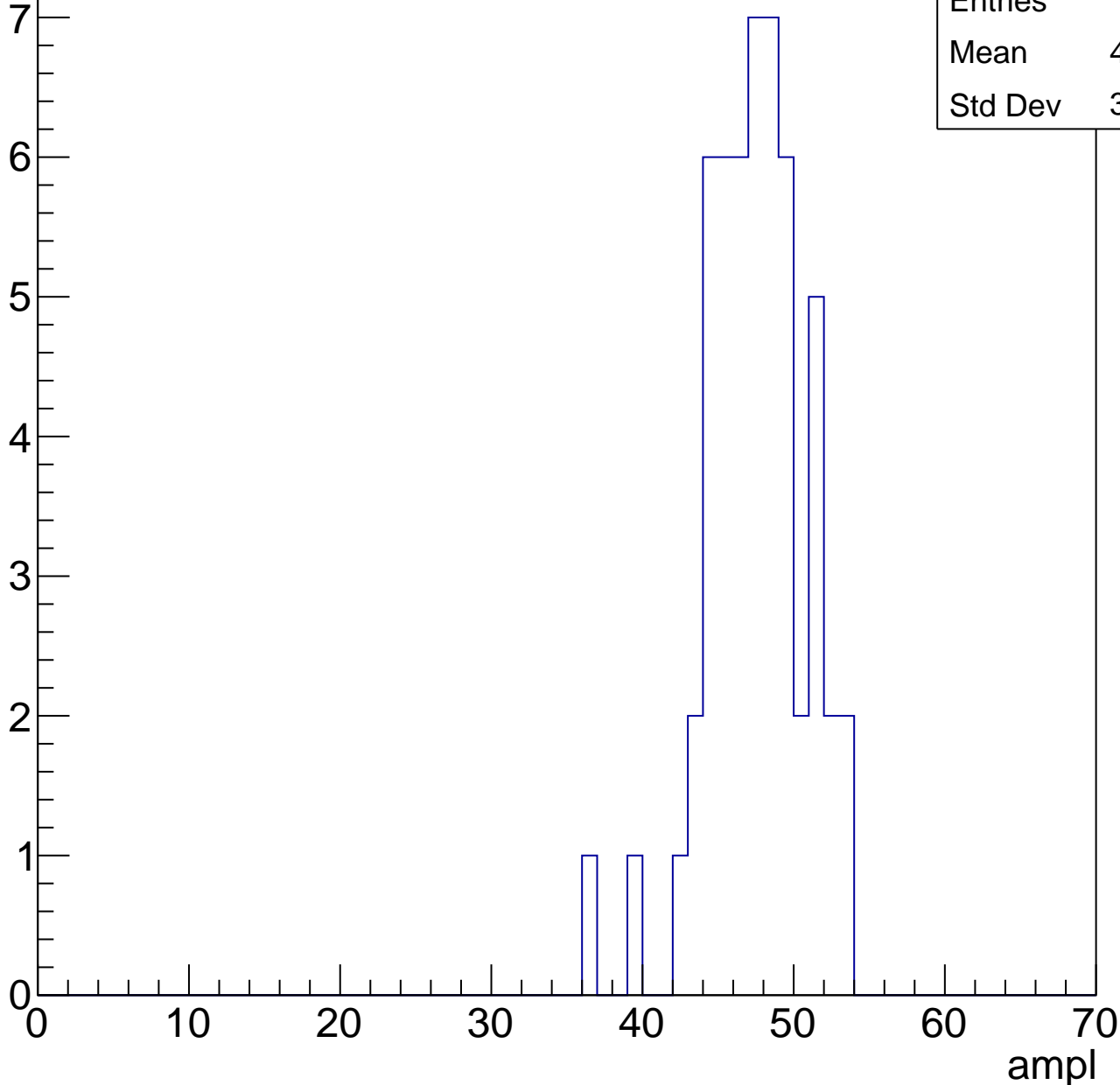


# B1L103S, U3-ch30, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

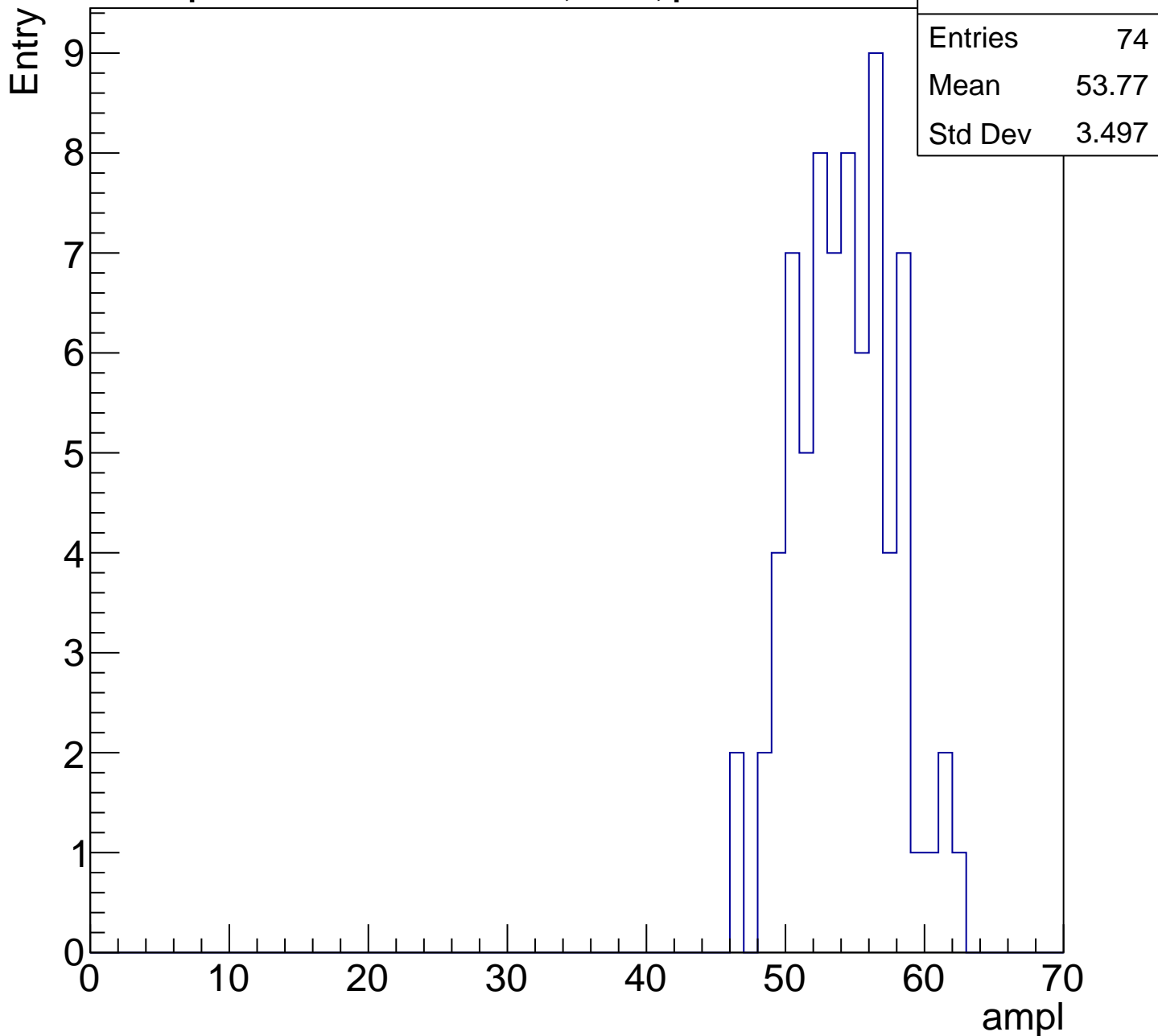
Entry

Entries	54
Mean	46.98
Std Dev	3.269



# B1L103S, U3-ch30, adc4

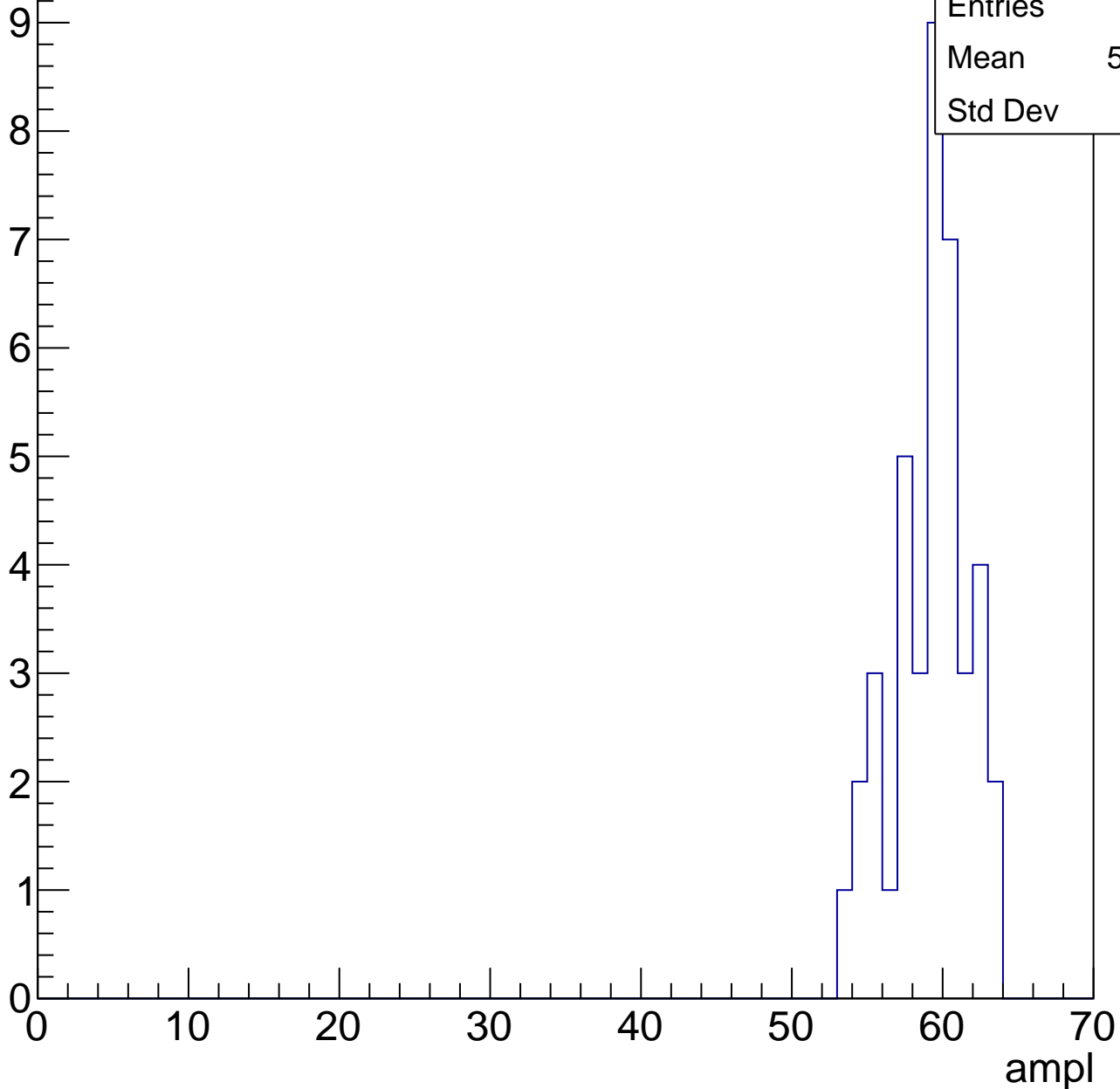
calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U3-ch30, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

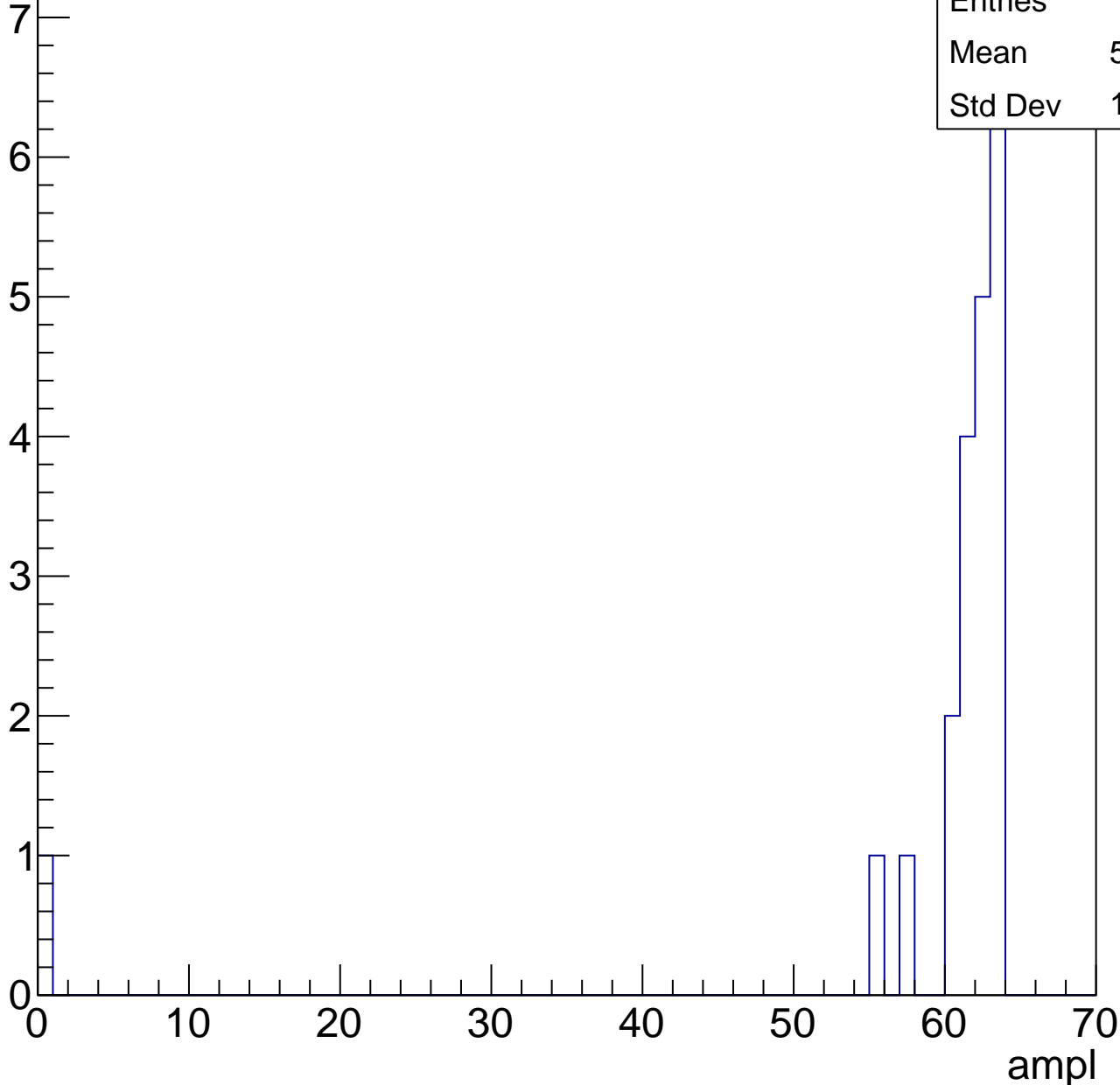


# B1L103S, U3-ch30, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	21
Mean	58.43
Std Dev	13.22

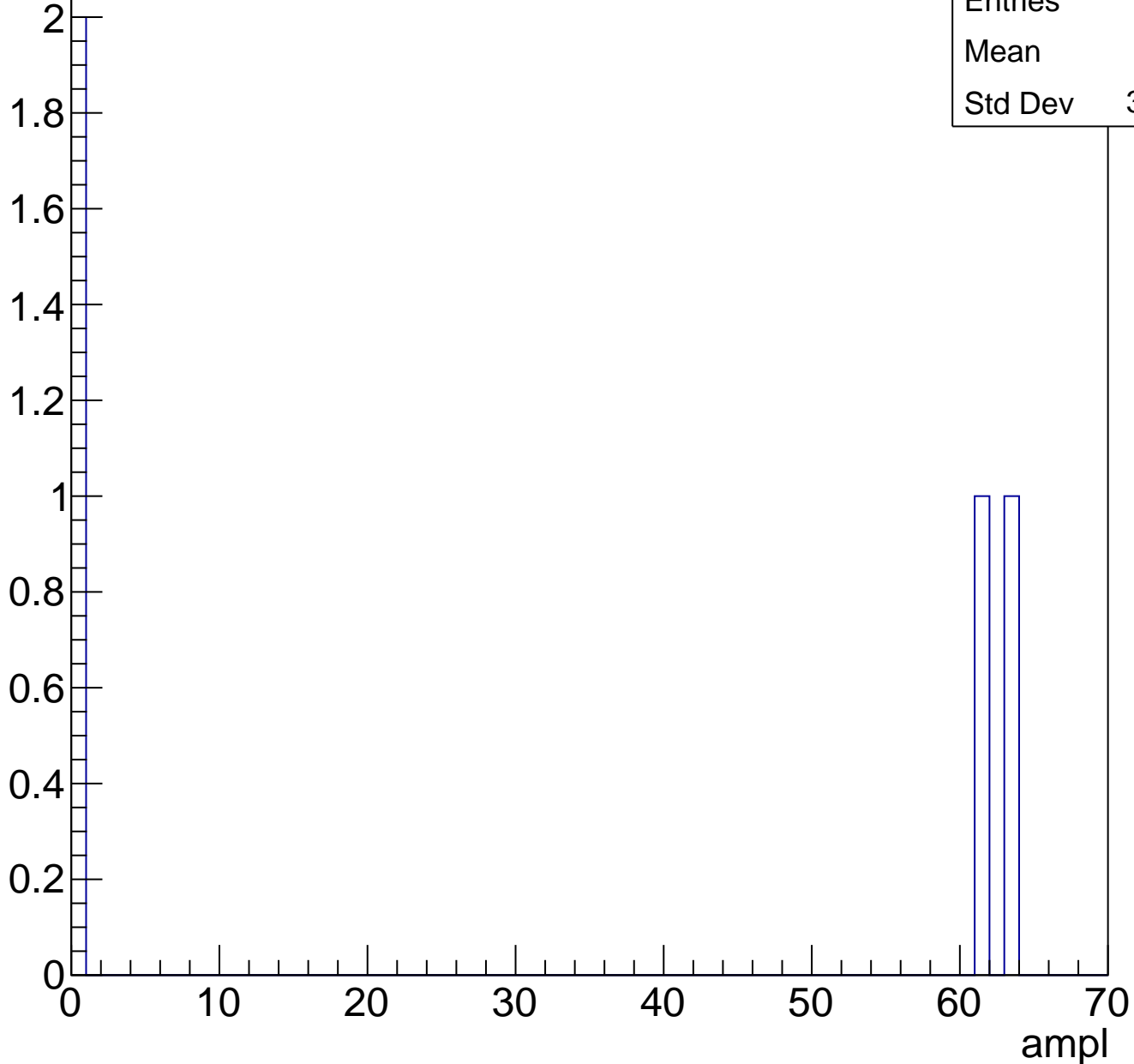




# B1L103S, U3-ch30, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch31, adc0

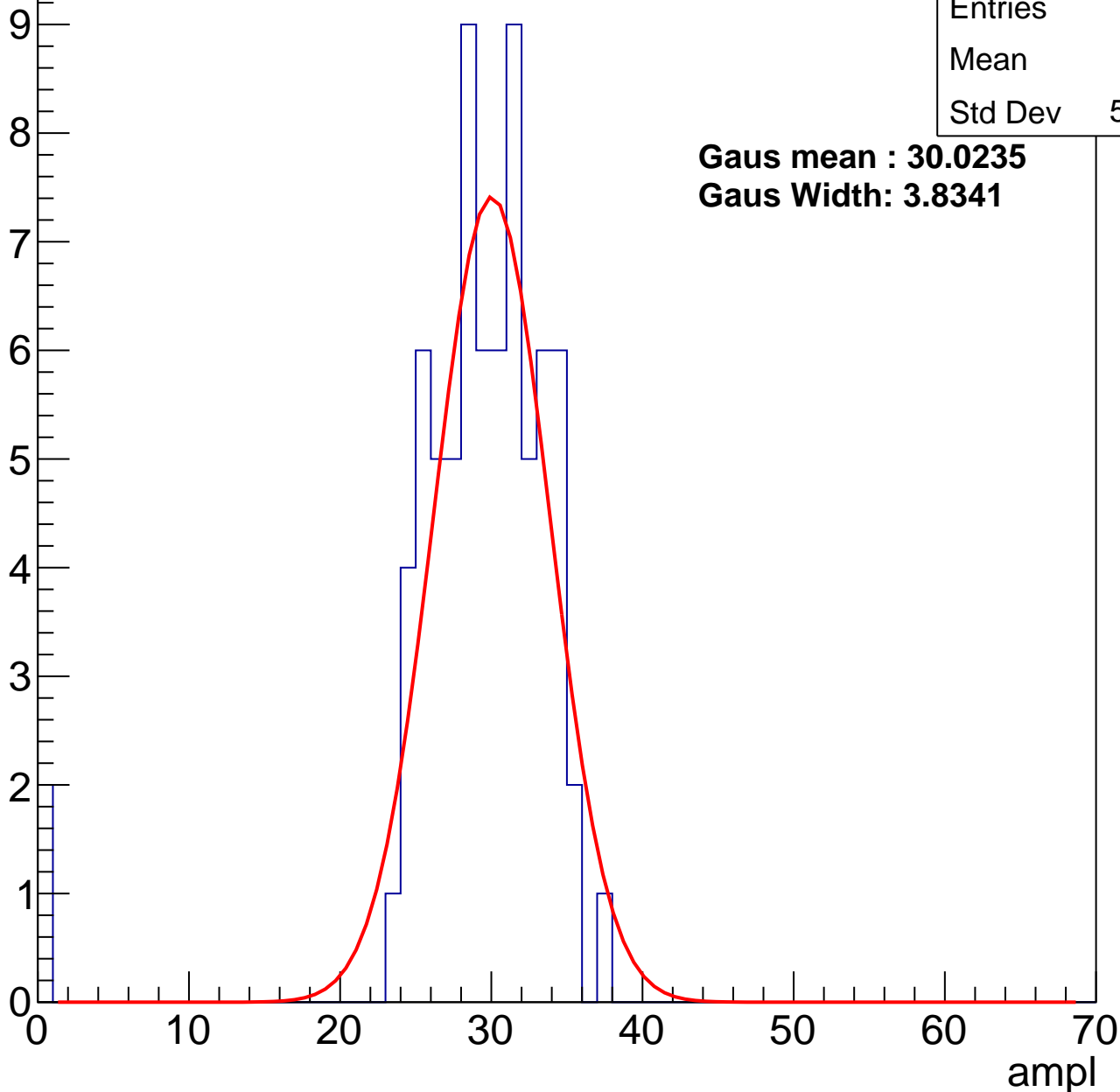
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	28.6
Std Dev	5.788

**Gaus mean : 30.0235**

**Gaus Width: 3.8341**



# B1L103S, U3-ch31, adc1

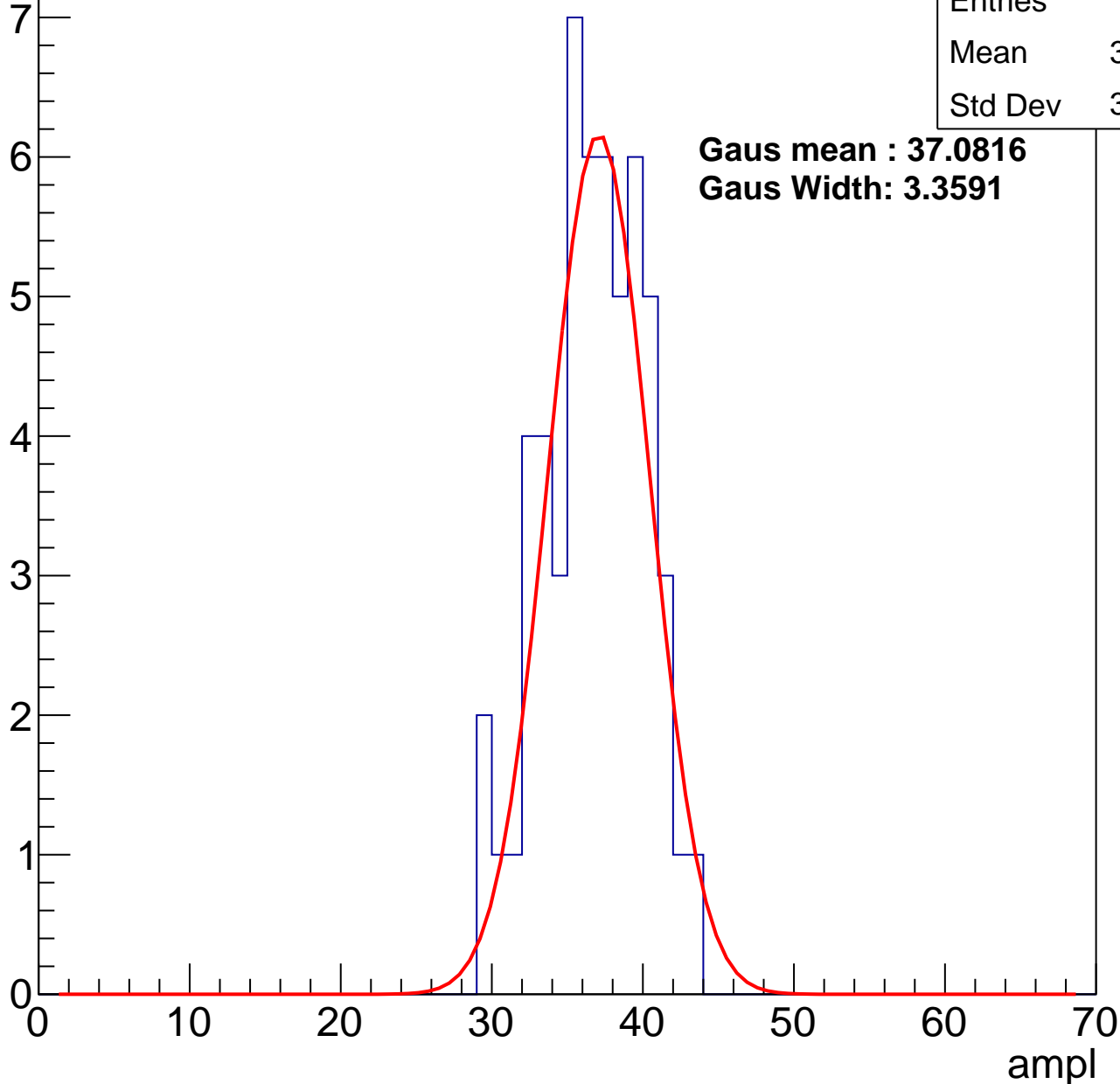
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	36.29
Std Dev	3.285

**Gaus mean : 37.0816**

**Gaus Width: 3.3591**



# B1L103S, U3-ch31, adc2

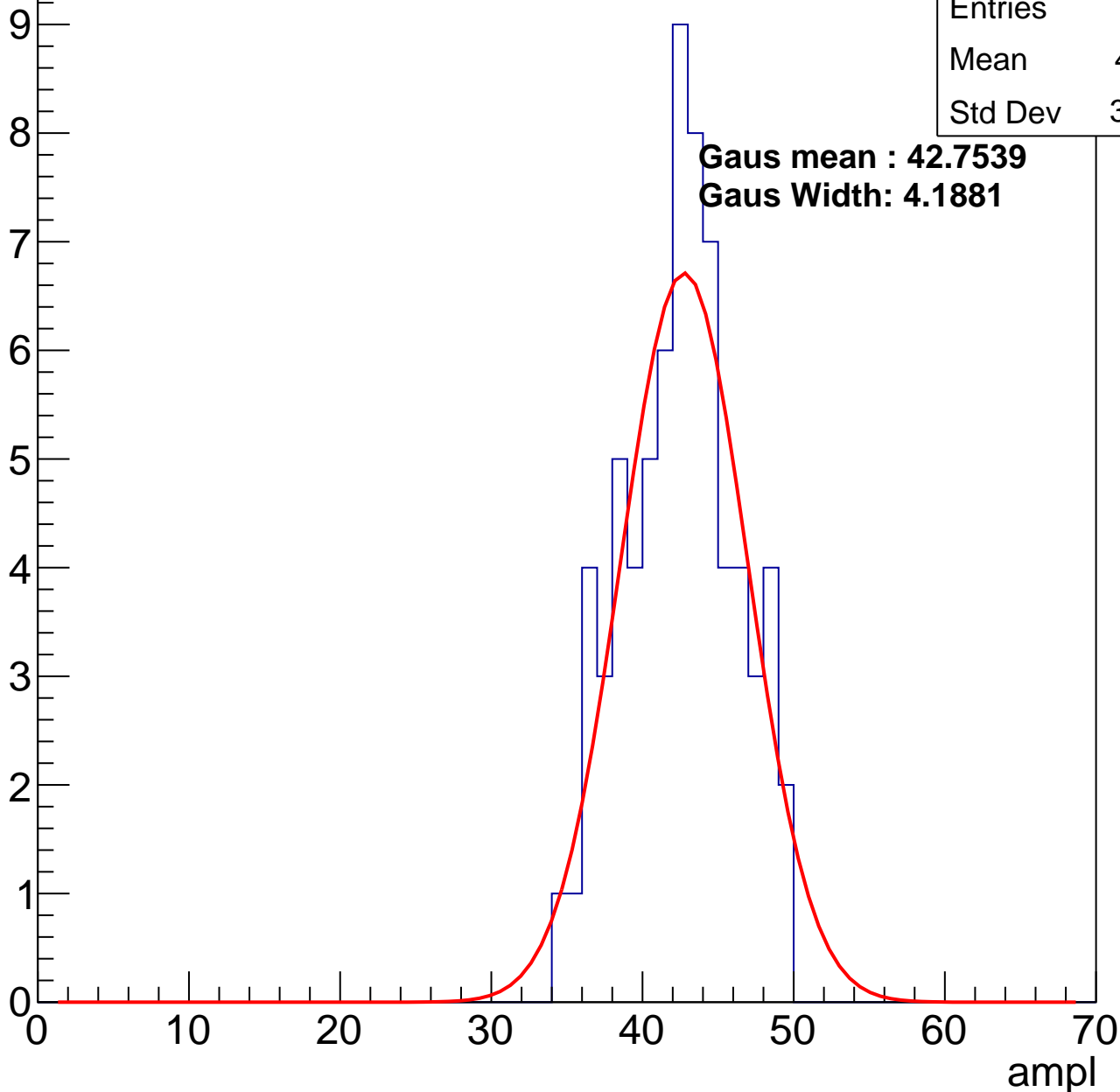
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	42.01
Std Dev	3.639

**Gaus mean : 42.7539**

**Gaus Width: 4.1881**

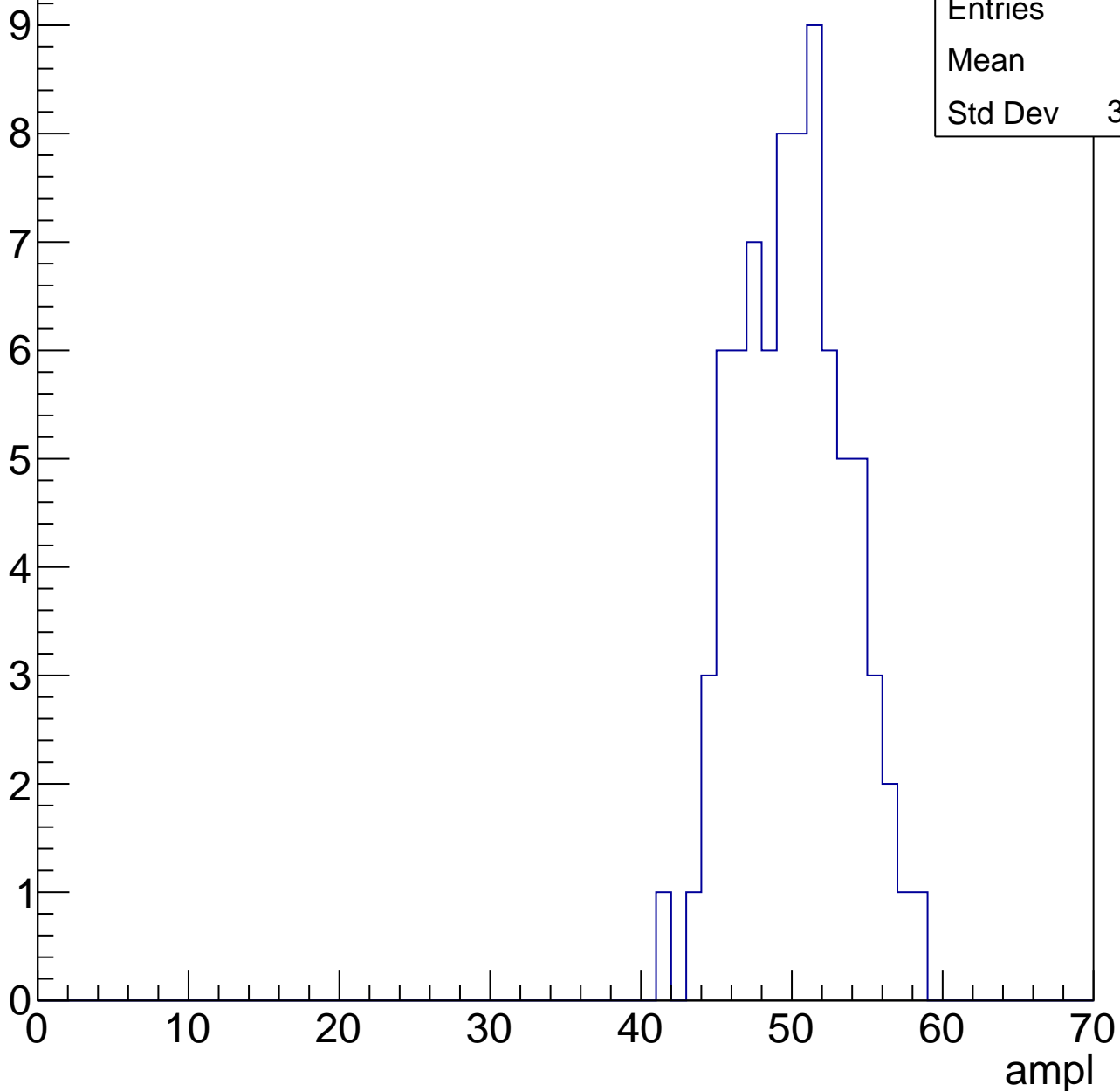


# B1L103S, U3-ch31, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

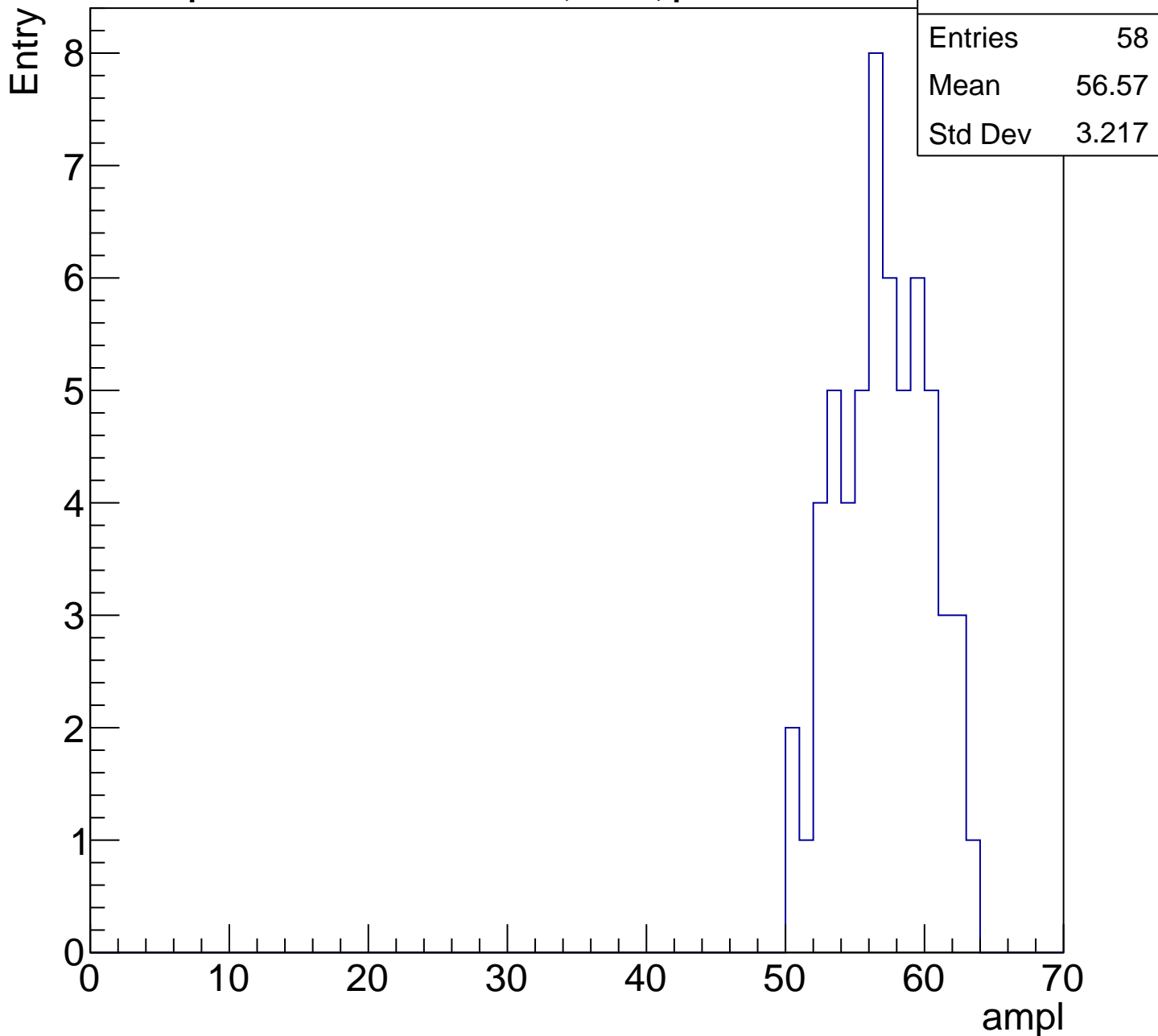
Entry

Entries	78
Mean	49.6
Std Dev	3.553



# B1L103S, U3-ch31, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

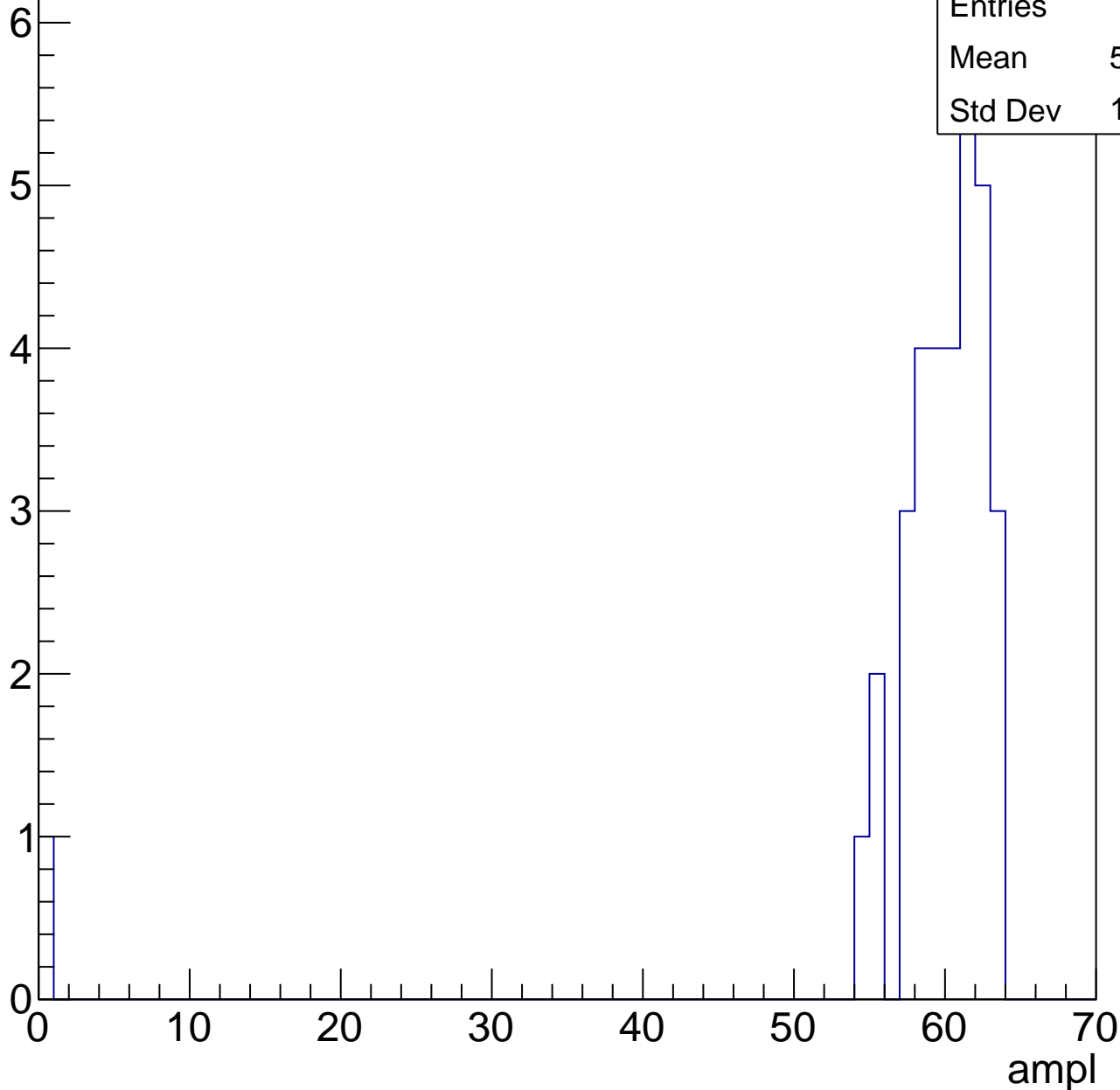


# B1L103S, U3-ch31, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	33
Mean	57.82
Std Dev	10.49

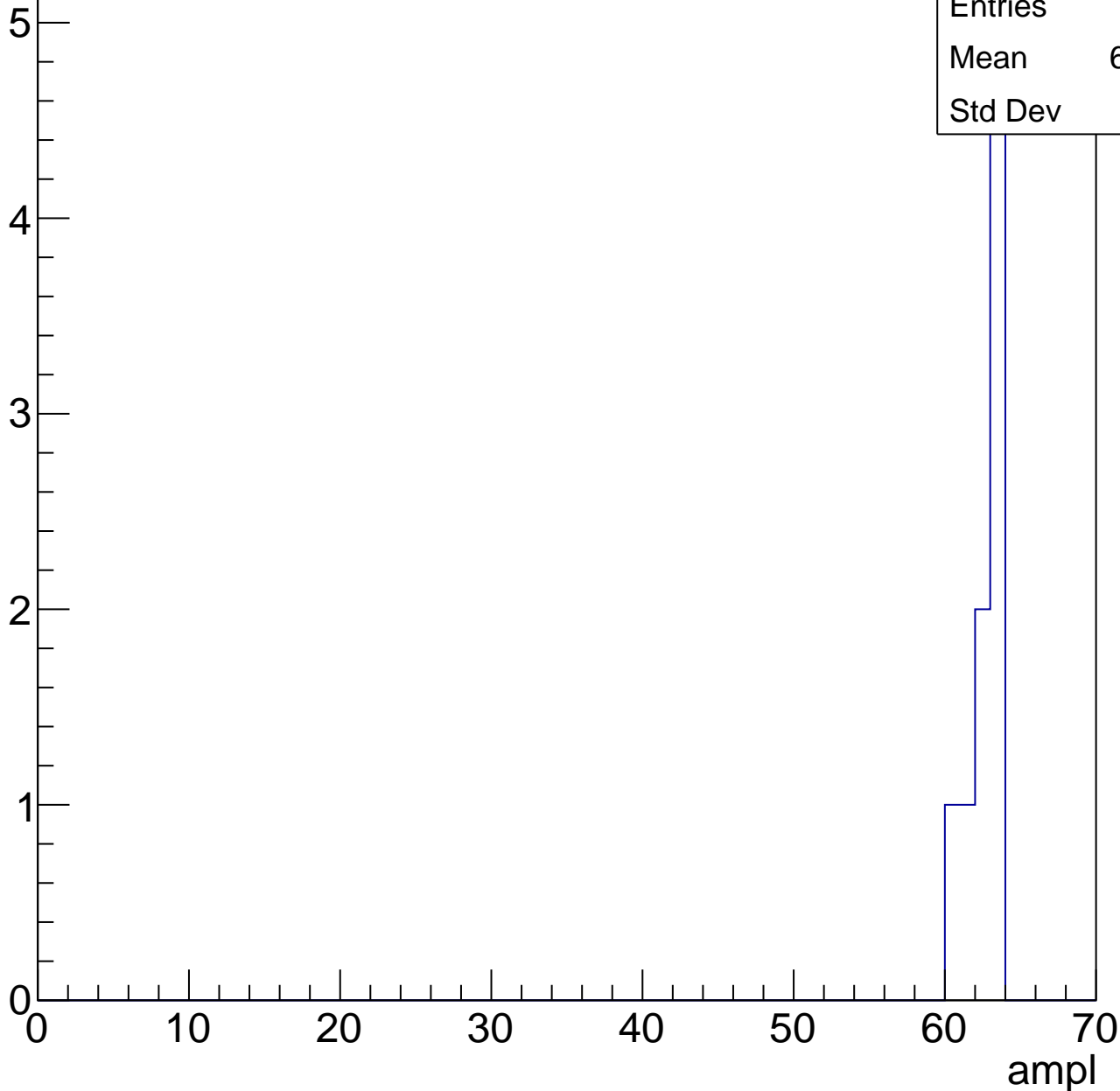


# B1L103S, U3-ch31, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	9
Mean	62.22
Std Dev	1.03





# B1L103S, U3-ch31, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	3
Mean	21
Std Dev	29.7

# B1L103S, U3-ch32, adc0

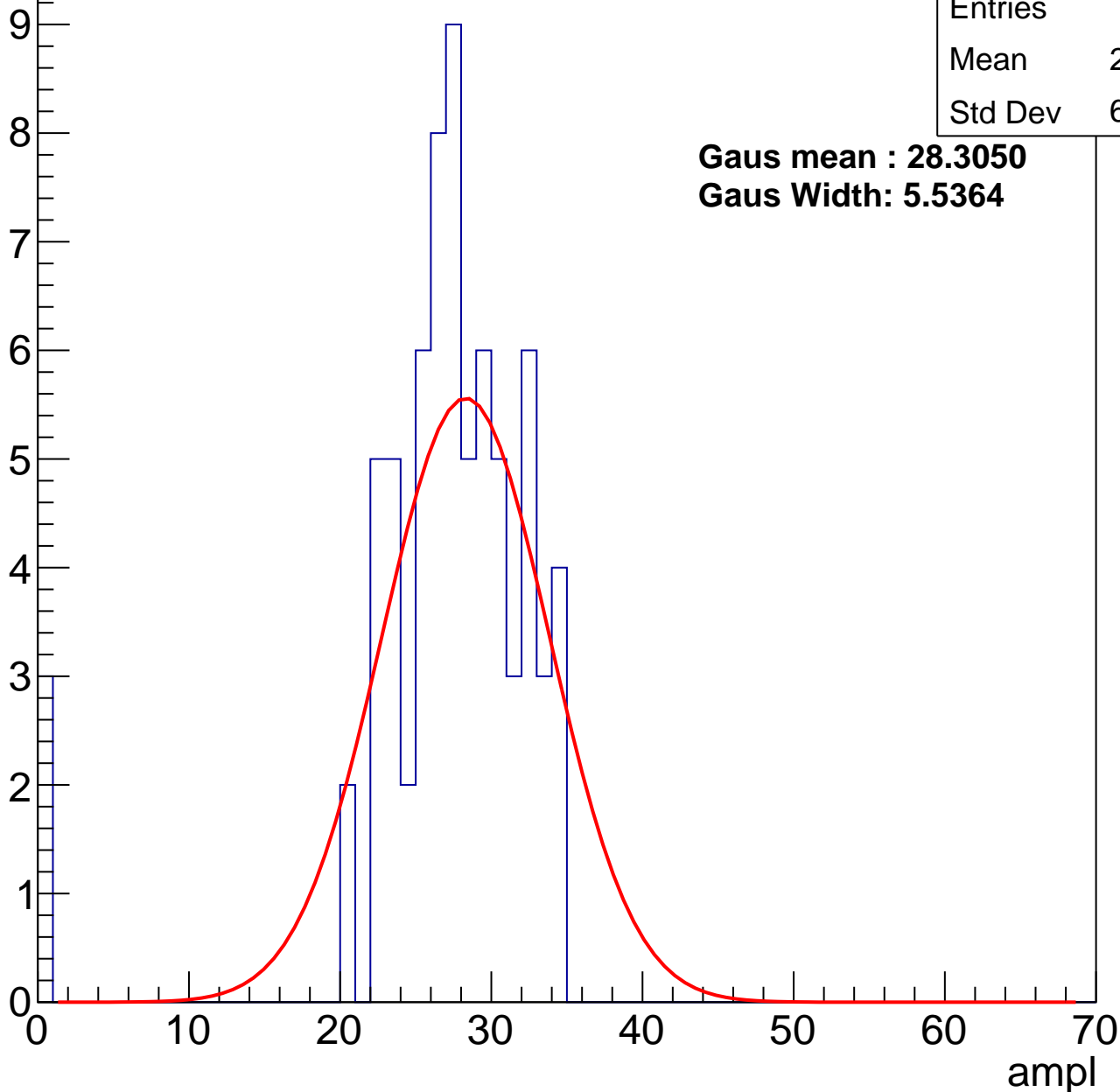
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	26.36
Std Dev	6.547

**Gaus mean : 28.3050**

**Gaus Width: 5.5364**



# B1L103S, U3-ch32, adc1

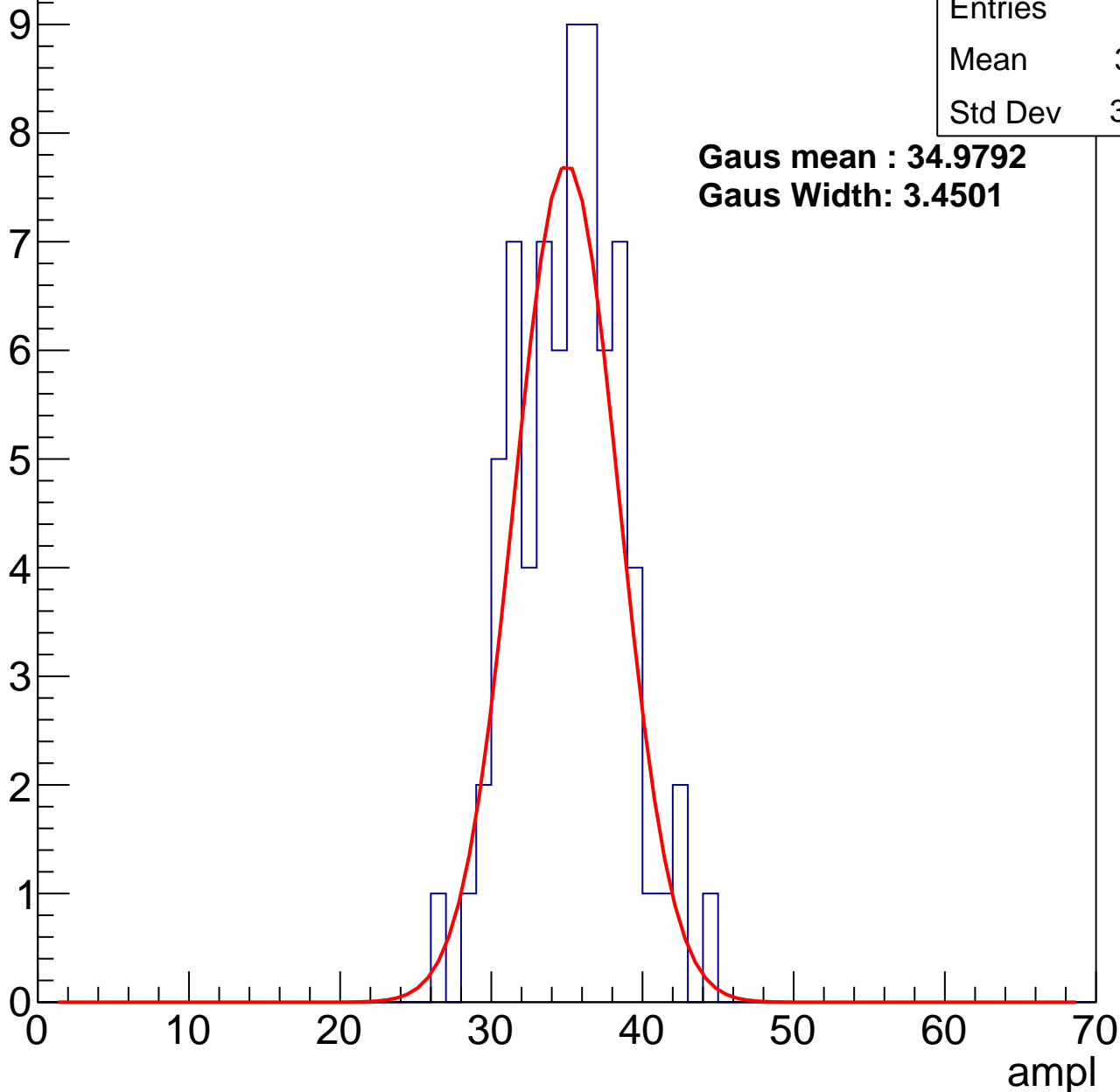
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	34.71
Std Dev	3.517

**Gaus mean : 34.9792**

**Gaus Width: 3.4501**



# B1L103S, U3-ch32, adc2

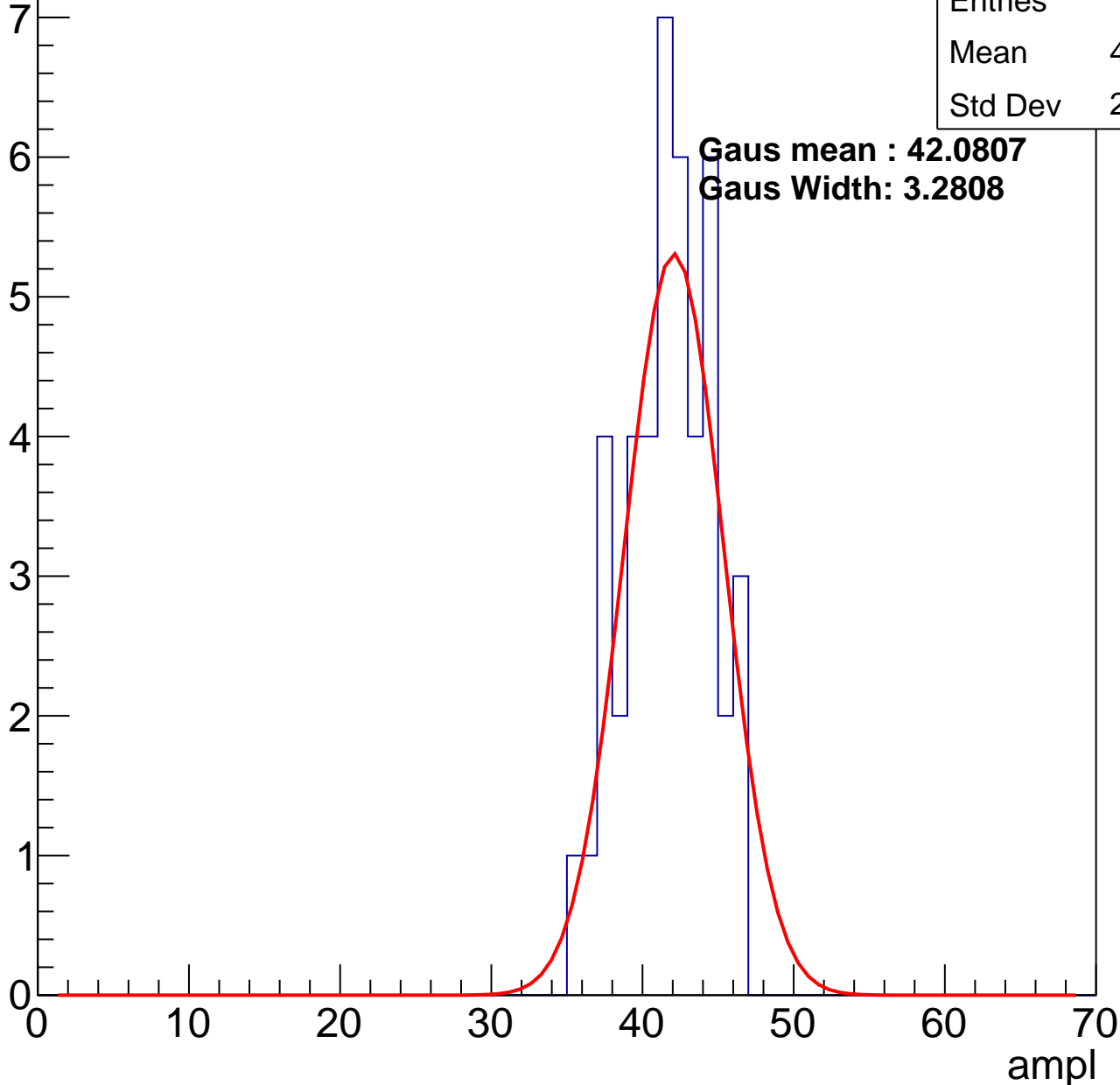
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	44
Mean	41.23
Std Dev	2.795

**Gaus mean : 42.0807**

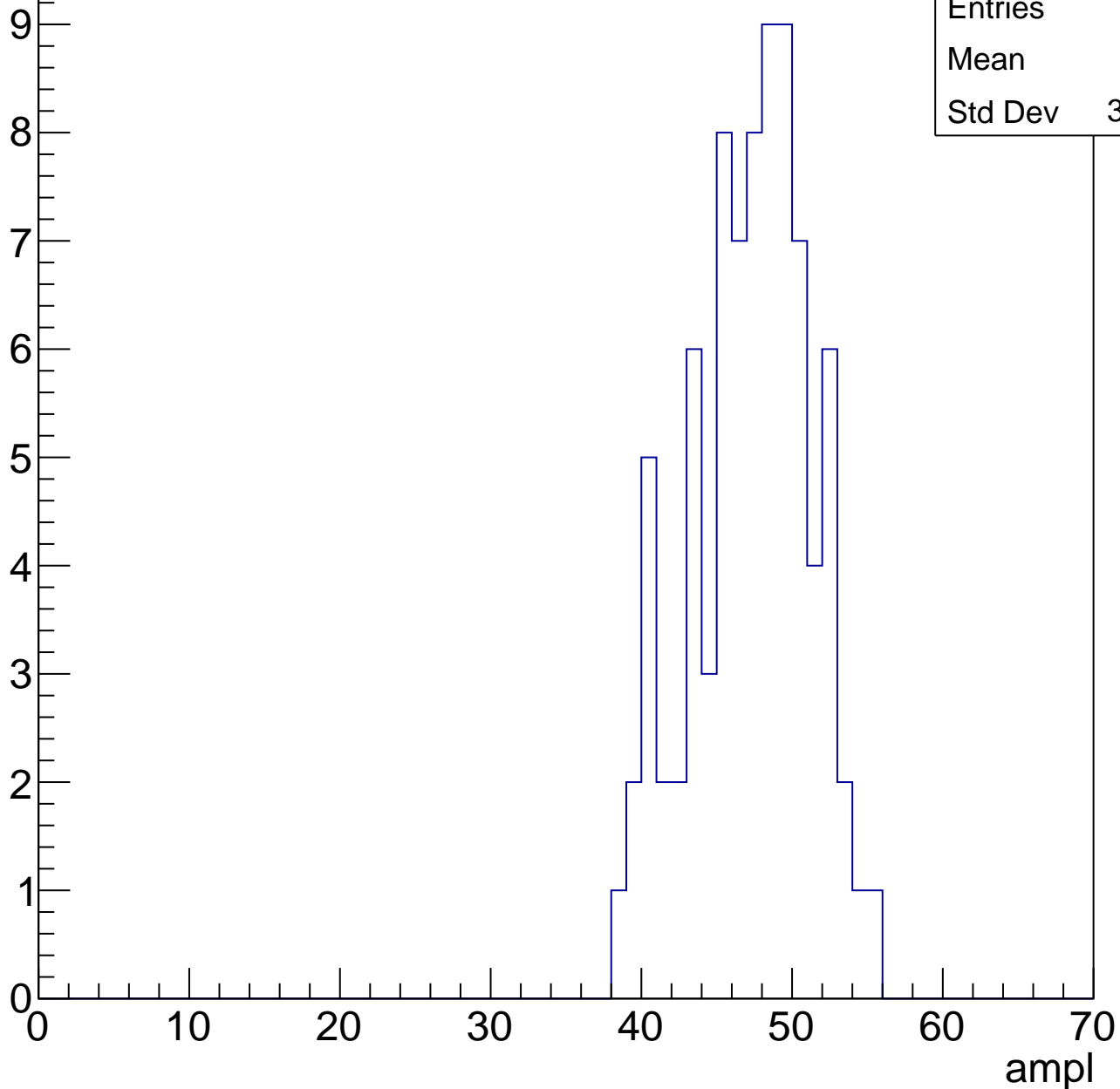
**Gaus Width: 3.2808**



# B1L103S, U3-ch32, adc3

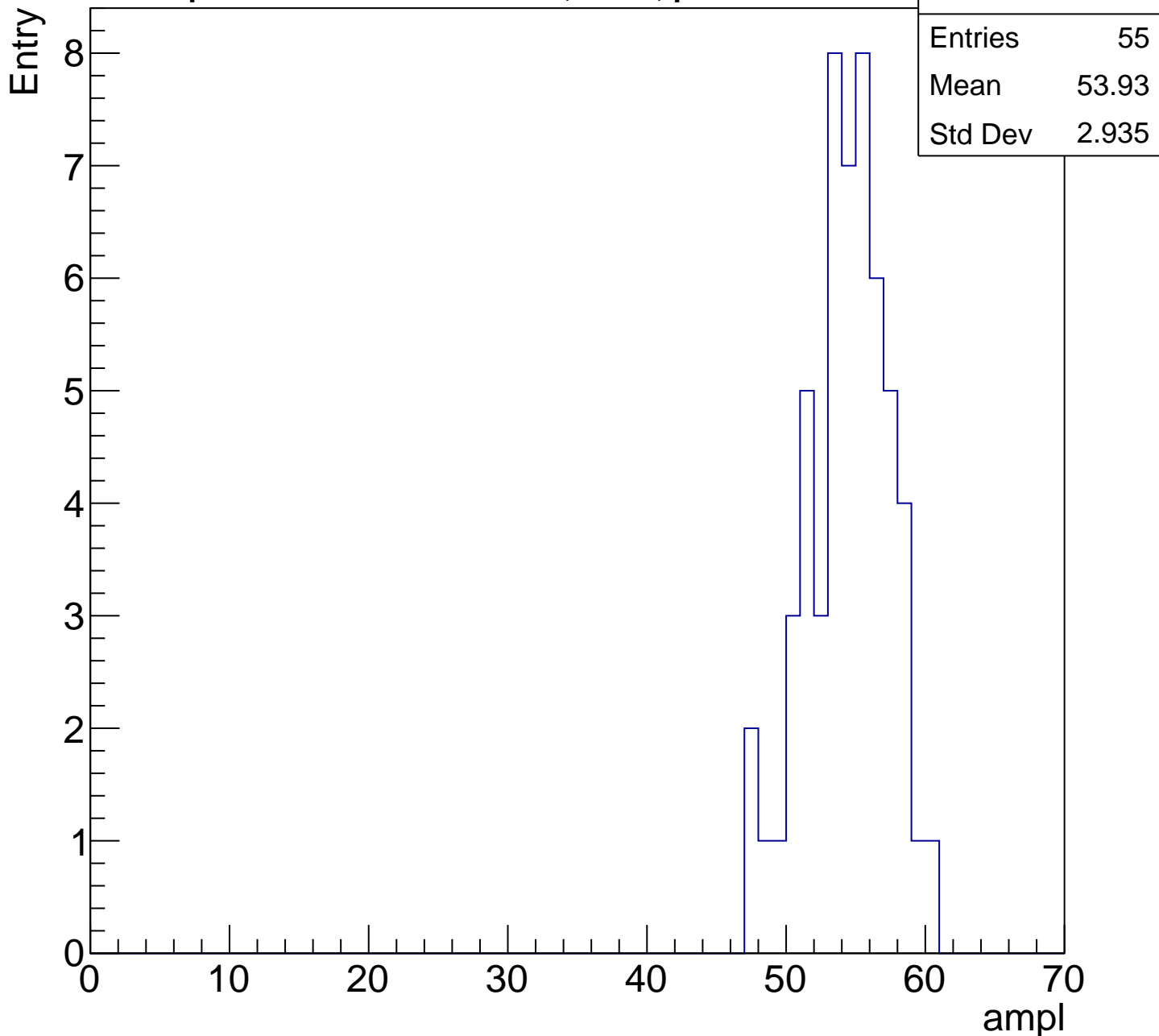
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch32, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

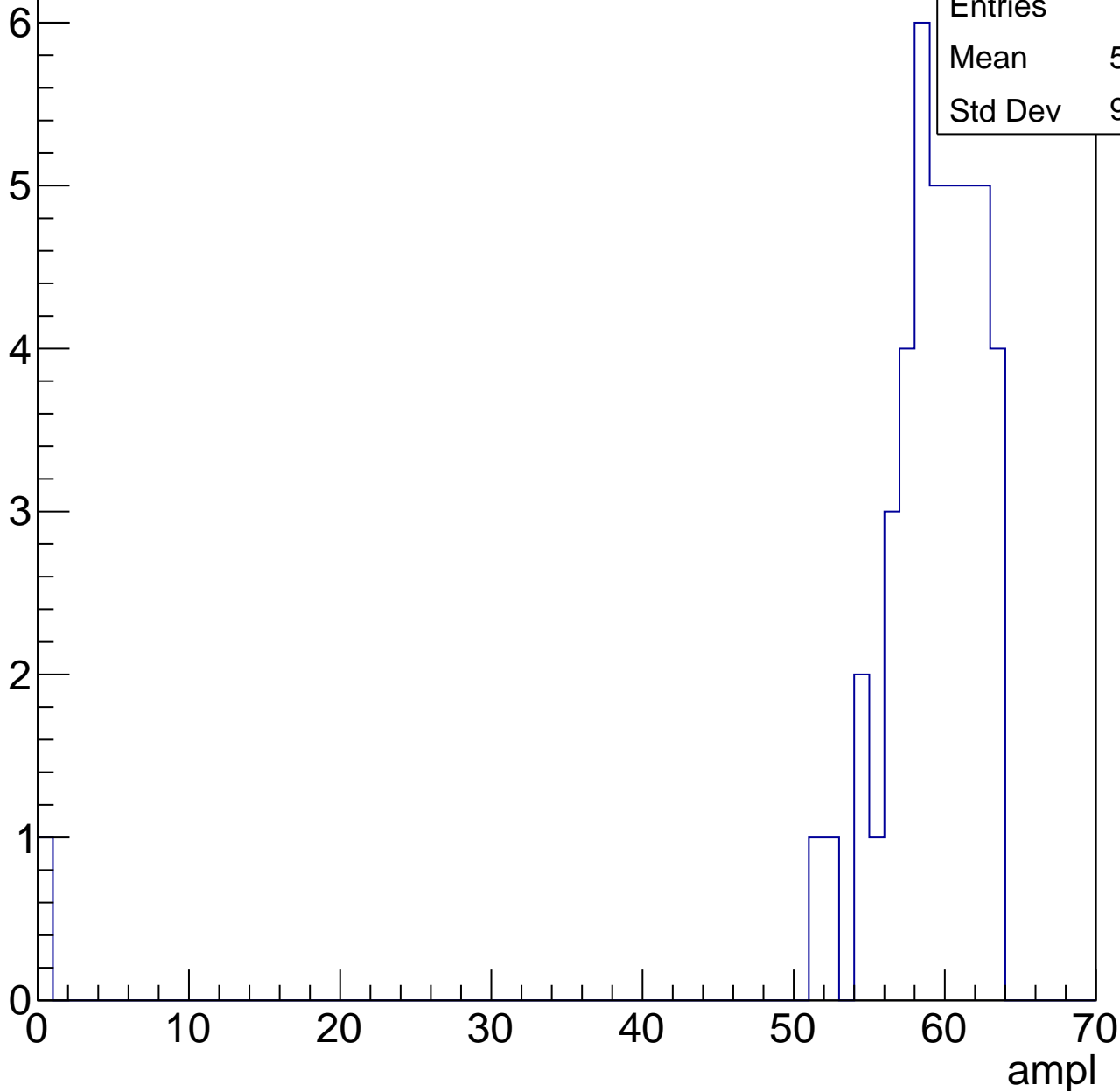


# B1L103S, U3-ch32, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	43
Mean	57.49
Std Dev	9.332

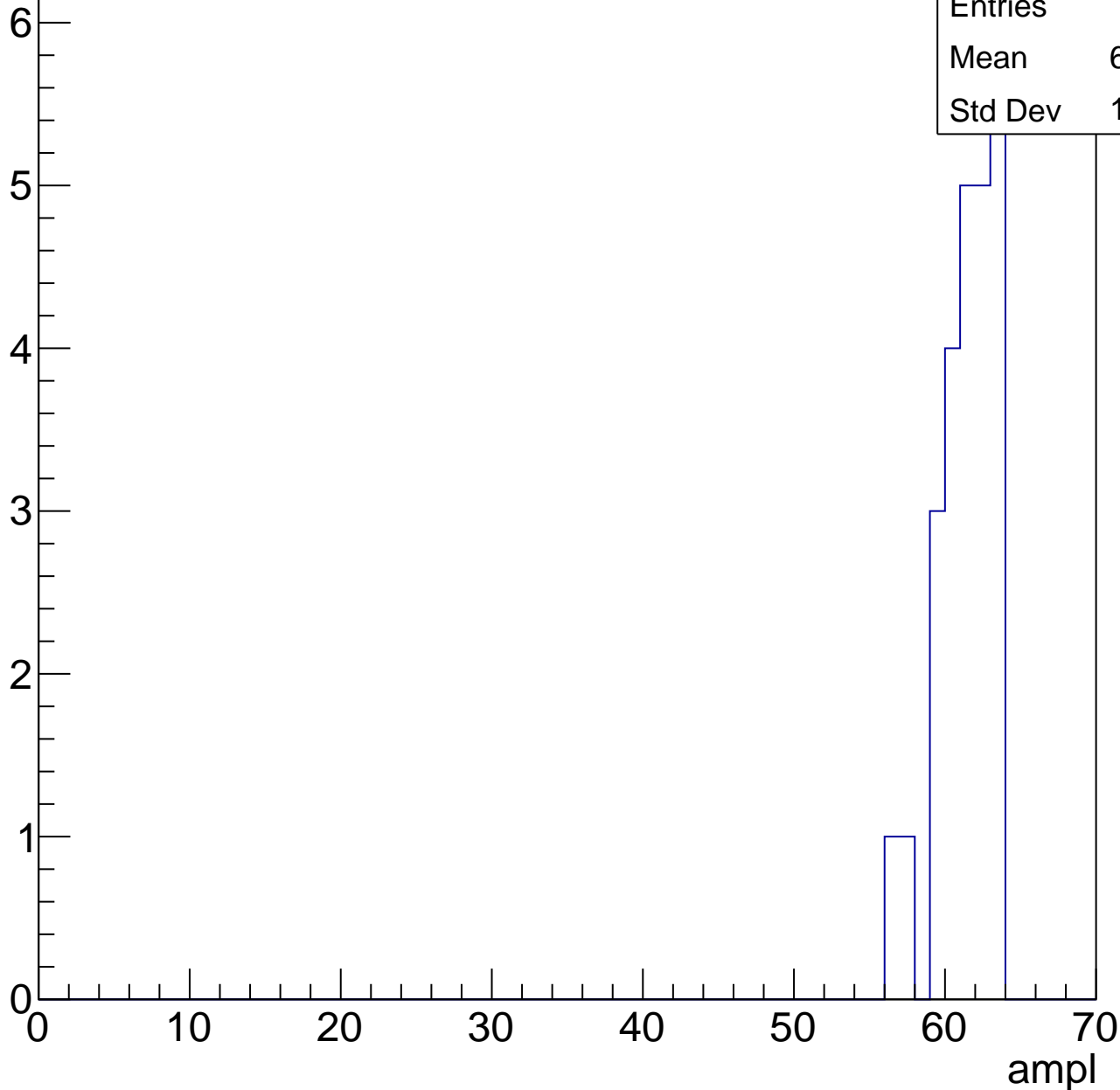


# B1L103S, U3-ch32, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	25
Mean	60.92
Std Dev	1.853

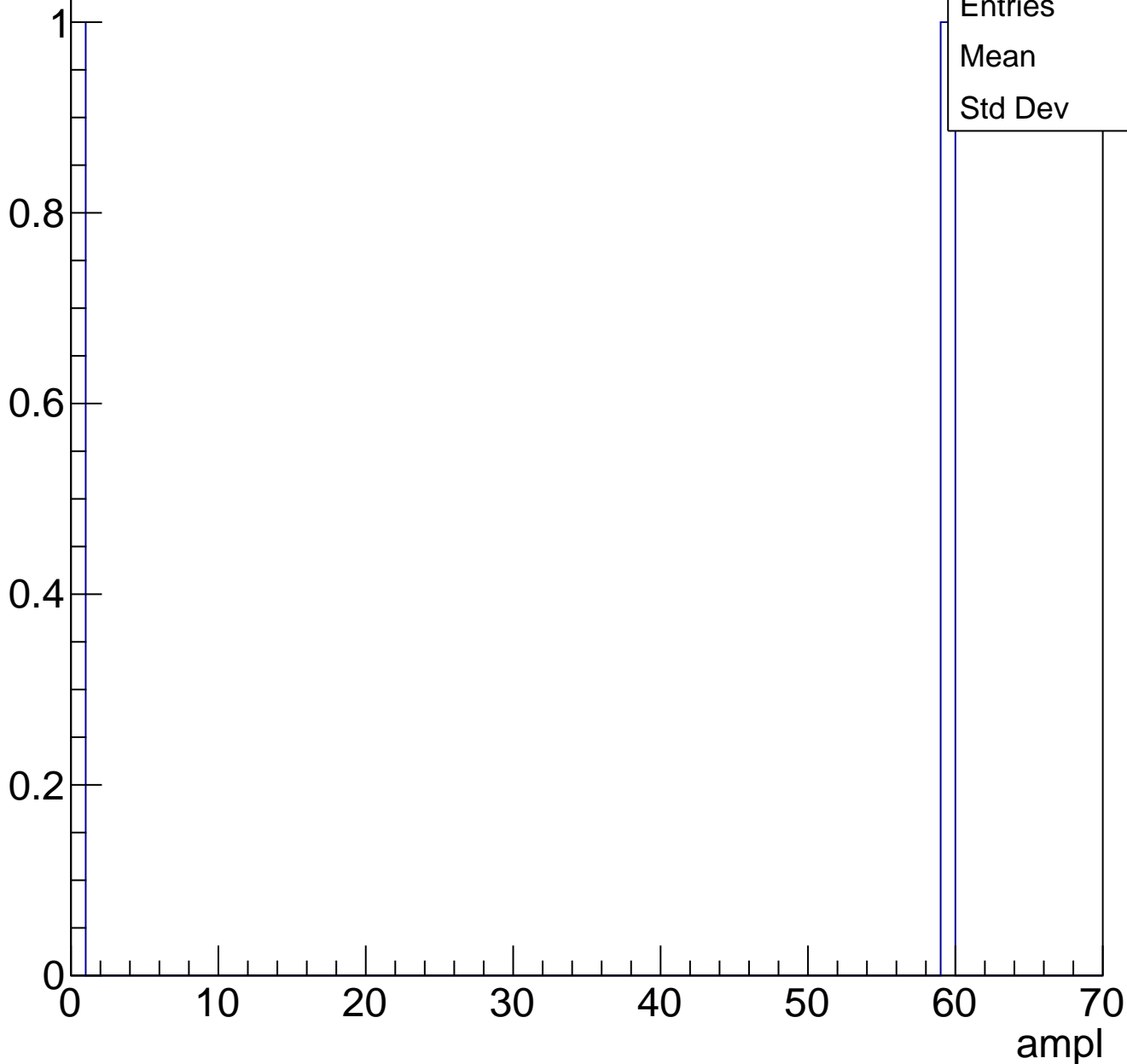




# B1L103S, U3-ch32, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch33, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	86
Mean	31.02
Std Dev	3.997

**Gaus mean : 31.8296**

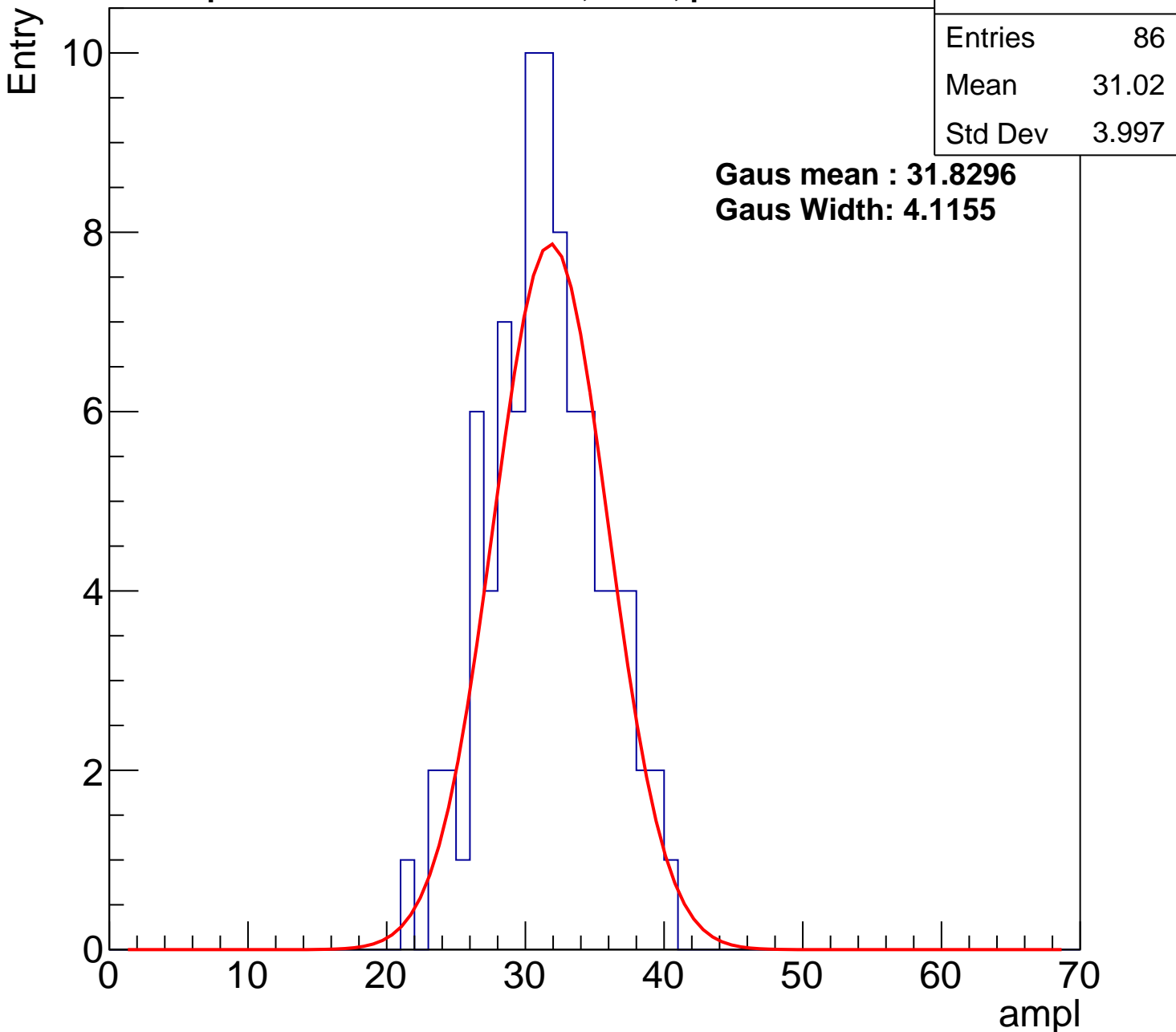
**Gaus Width: 4.1155**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U3-ch33, adc1

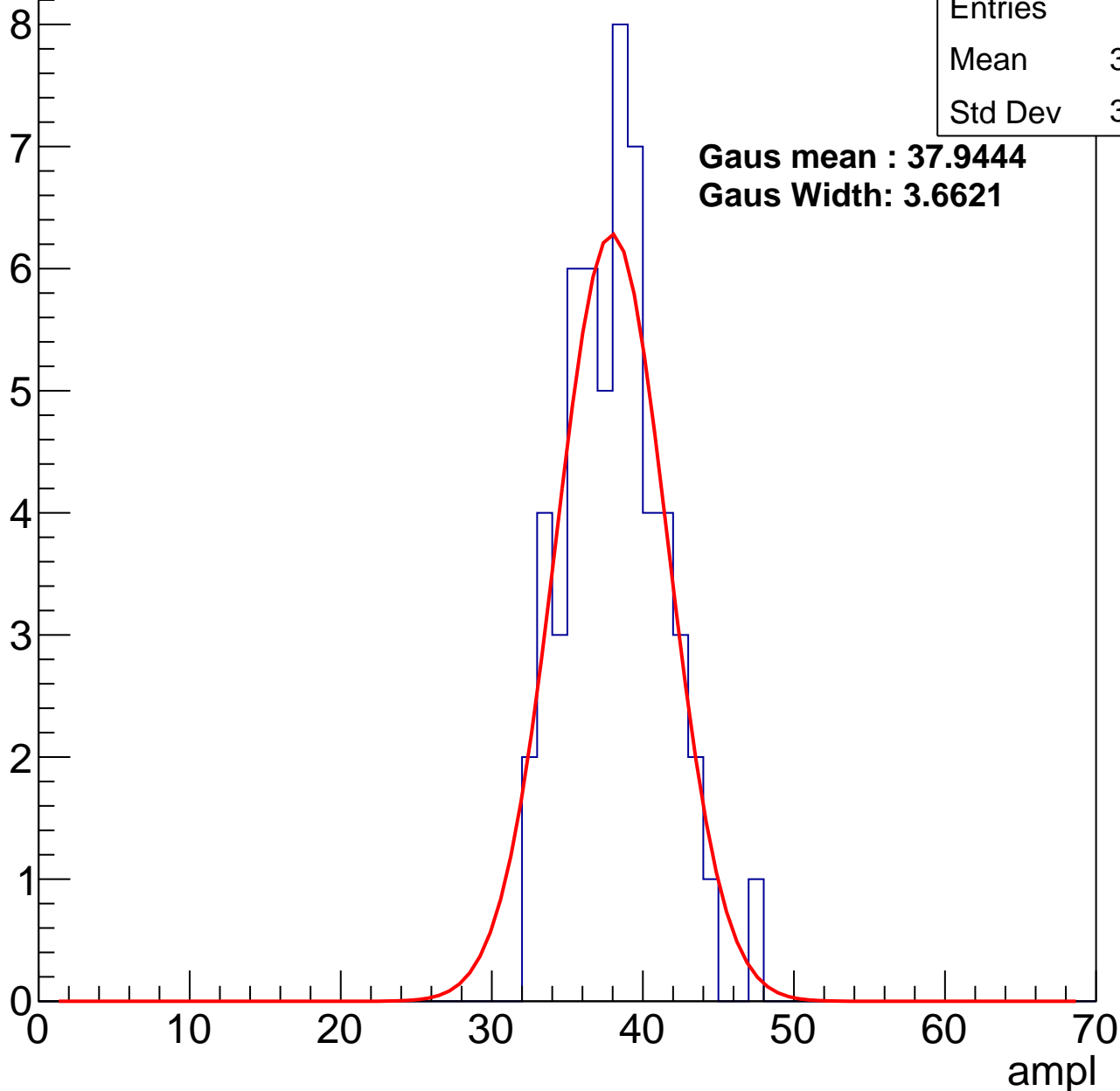
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	37.73
Std Dev	3.199

**Gaus mean : 37.9444**

**Gaus Width: 3.6621**



# B1L103S, U3-ch33, adc2

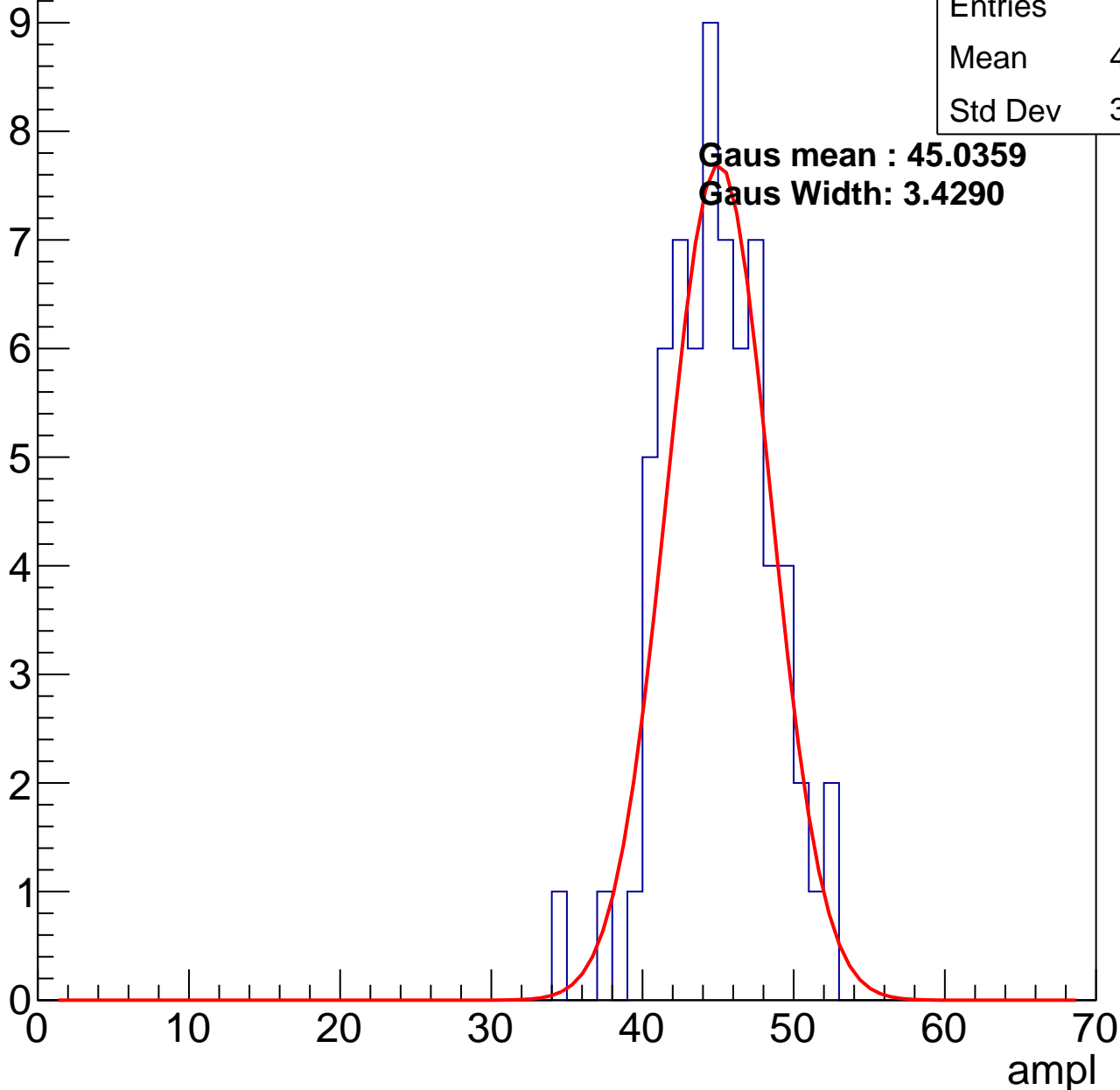
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	44.45
Std Dev	3.479

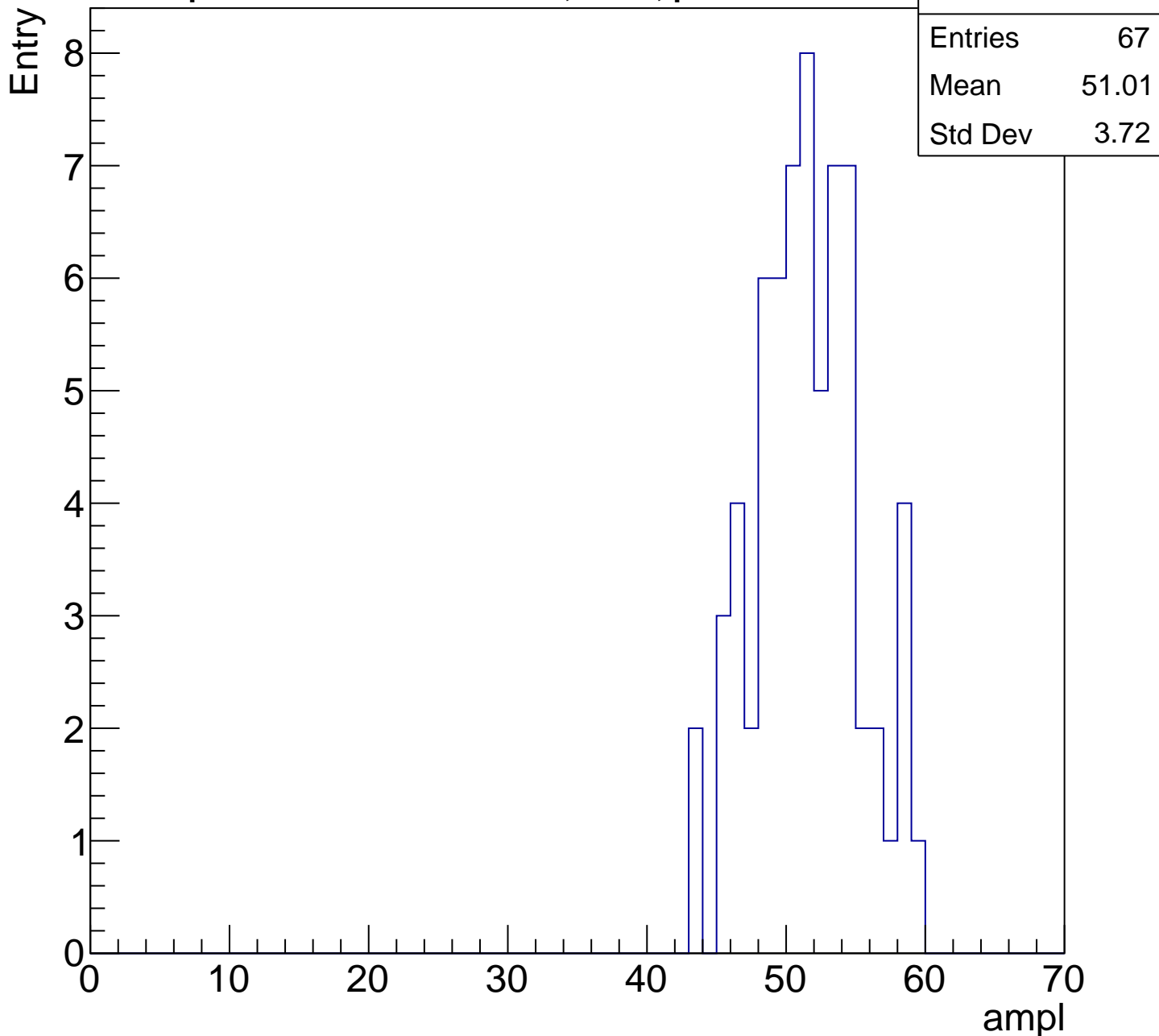
**Gaus mean : 45.0359**

**Gaus Width: 3.4290**



# B1L103S, U3-ch33, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

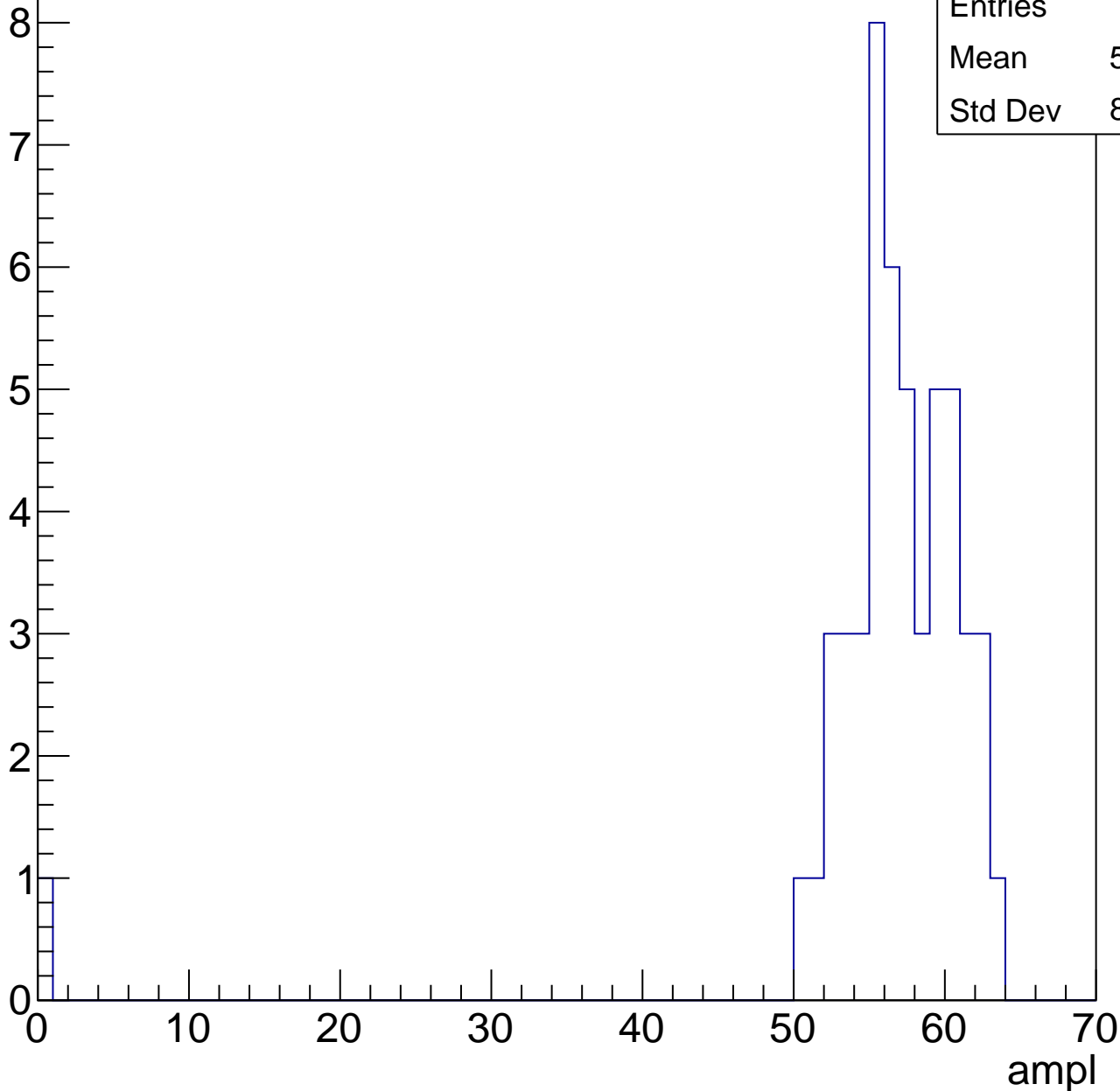


# B1L103S, U3-ch33, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	55.69
Std Dev	8.473



# B1L103S, U3-ch33, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

7

6

5

4

3

2

1

0

Entries

37

Mean

60.24

Std Dev

2.174

ampl

0

10

20

30

40

50

60

70

# B1L103S, U3-ch33, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U3-ch33, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch34, adc0

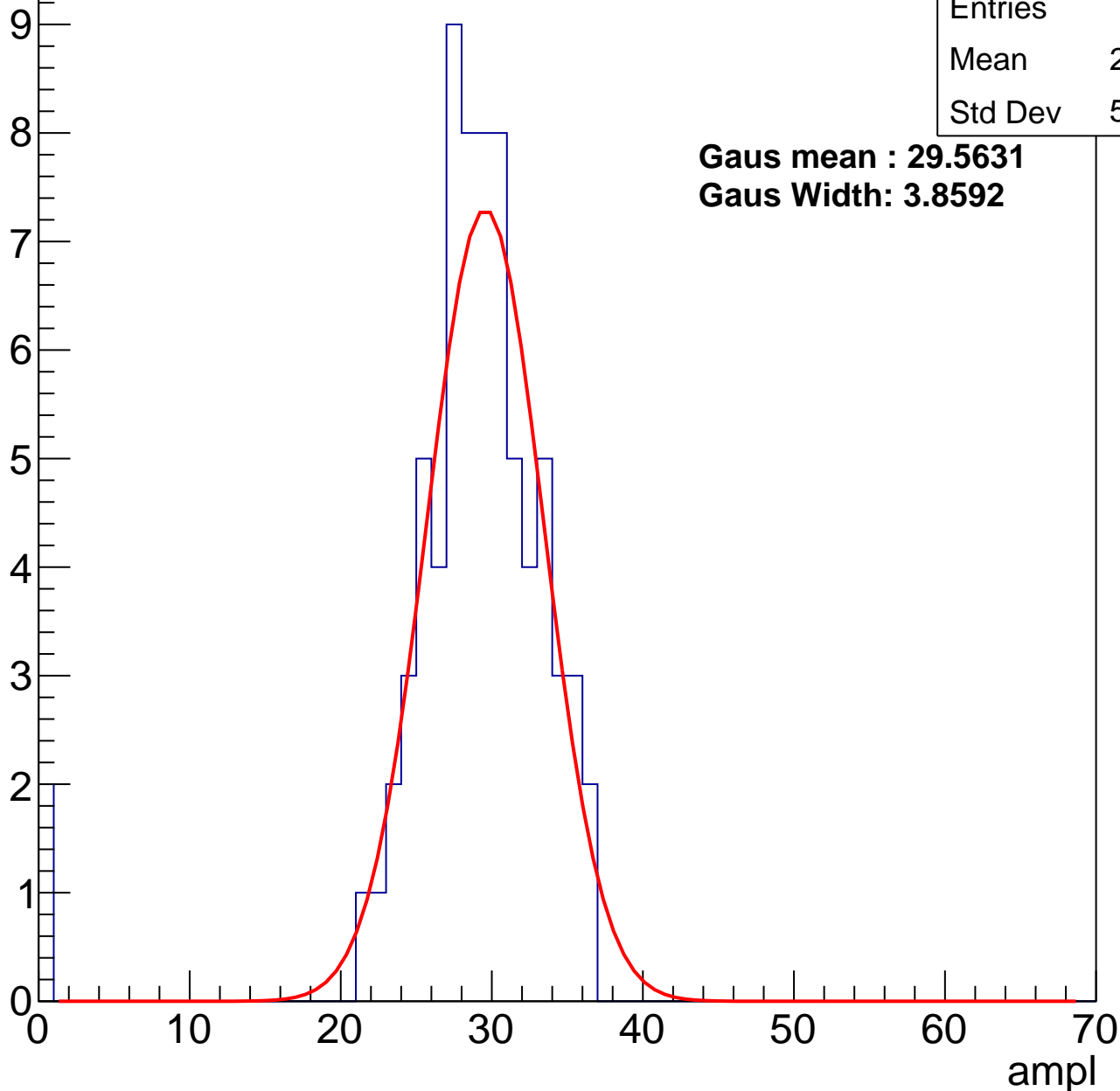
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	28.16
Std Dev	5.824

**Gaus mean : 29.5631**

**Gaus Width: 3.8592**



# B1L103S, U3-ch34, adc1

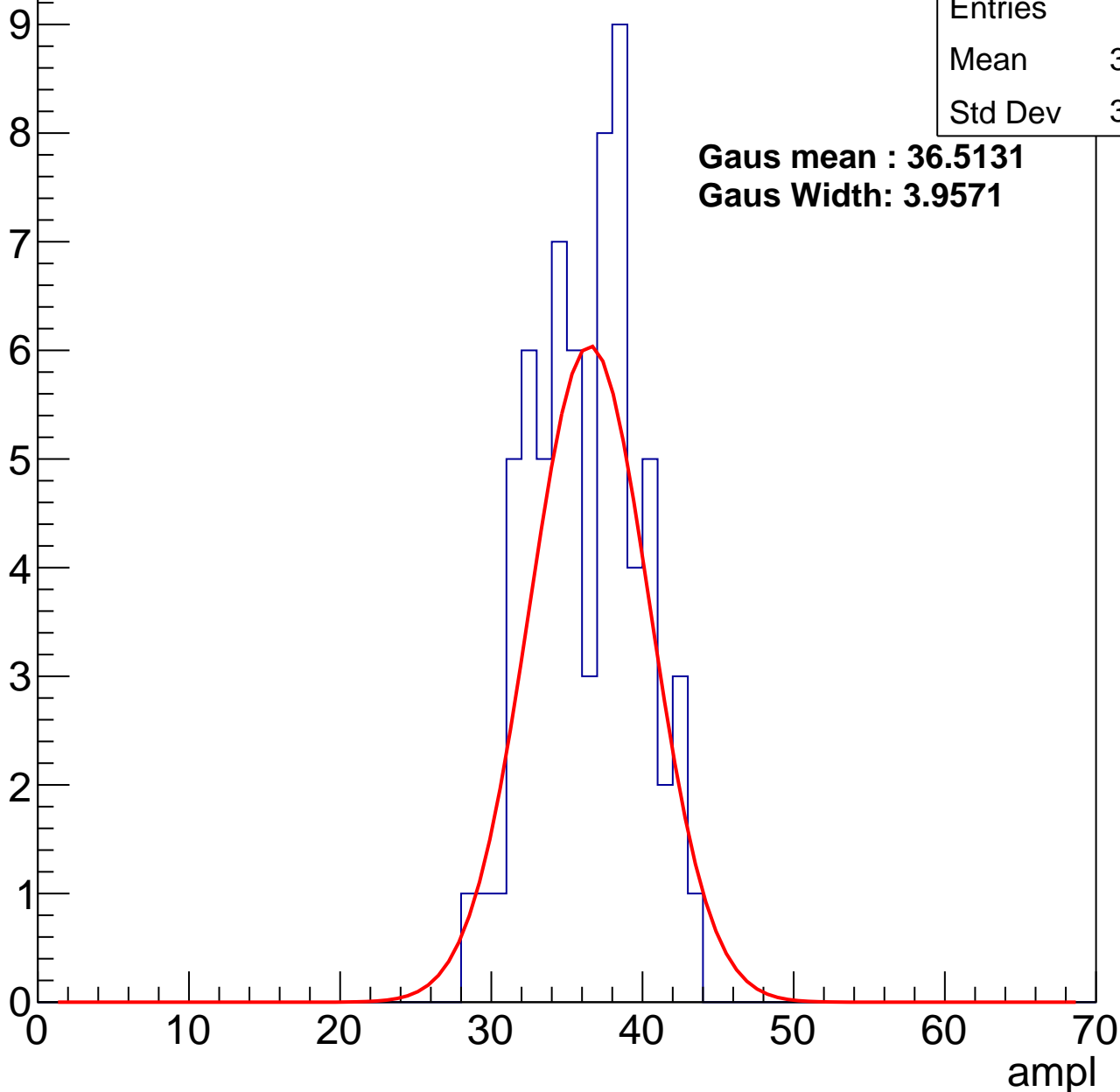
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	35.82
Std Dev	3.485

**Gaus mean : 36.5131**

**Gaus Width: 3.9571**



# B1L103S, U3-ch34, adc2

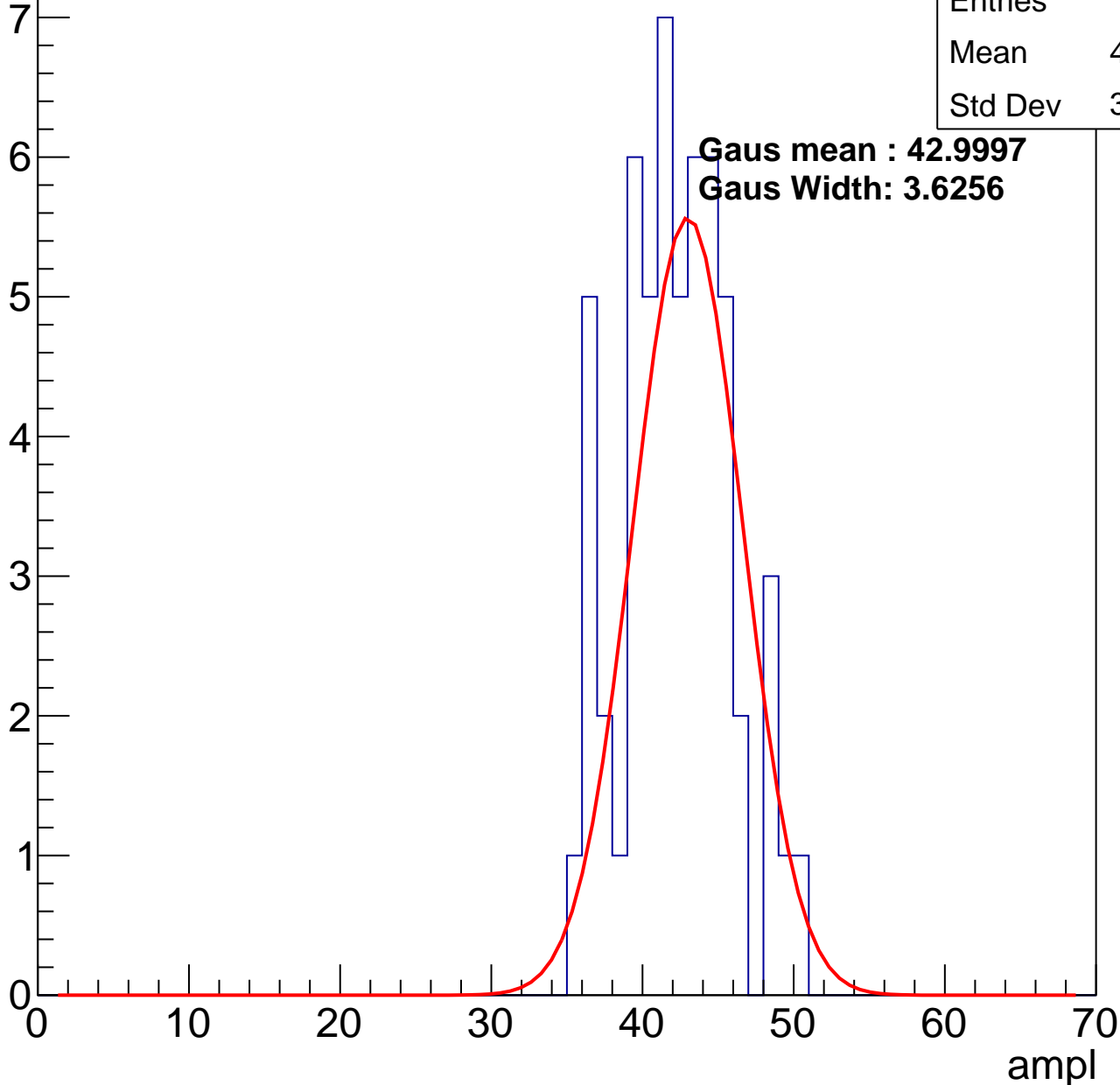
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	41.79
Std Dev	3.539

**Gaus mean : 42.9997**

**Gaus Width: 3.6256**

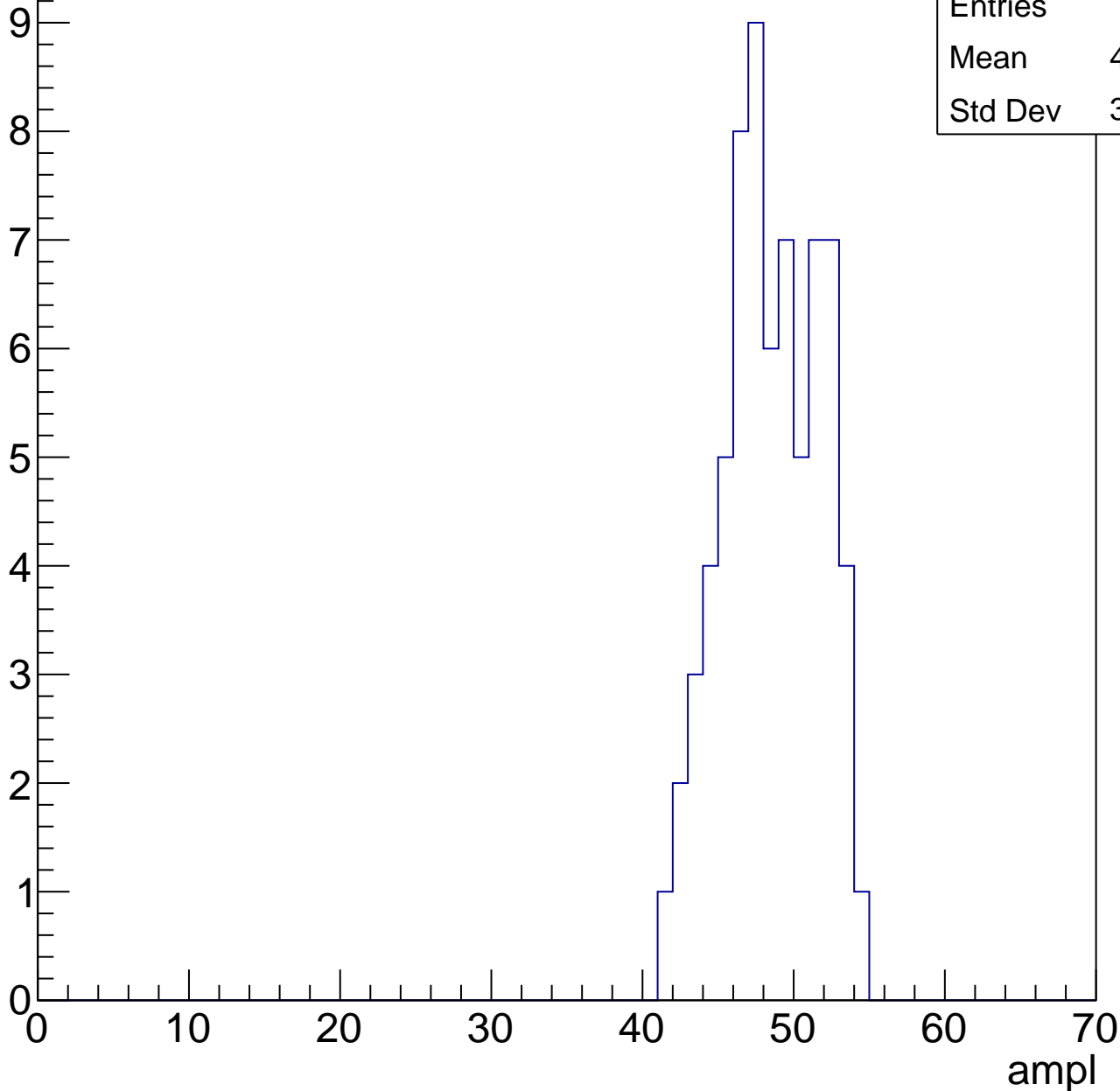


# B1L103S, U3-ch34, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	48.03
Std Dev	3.148

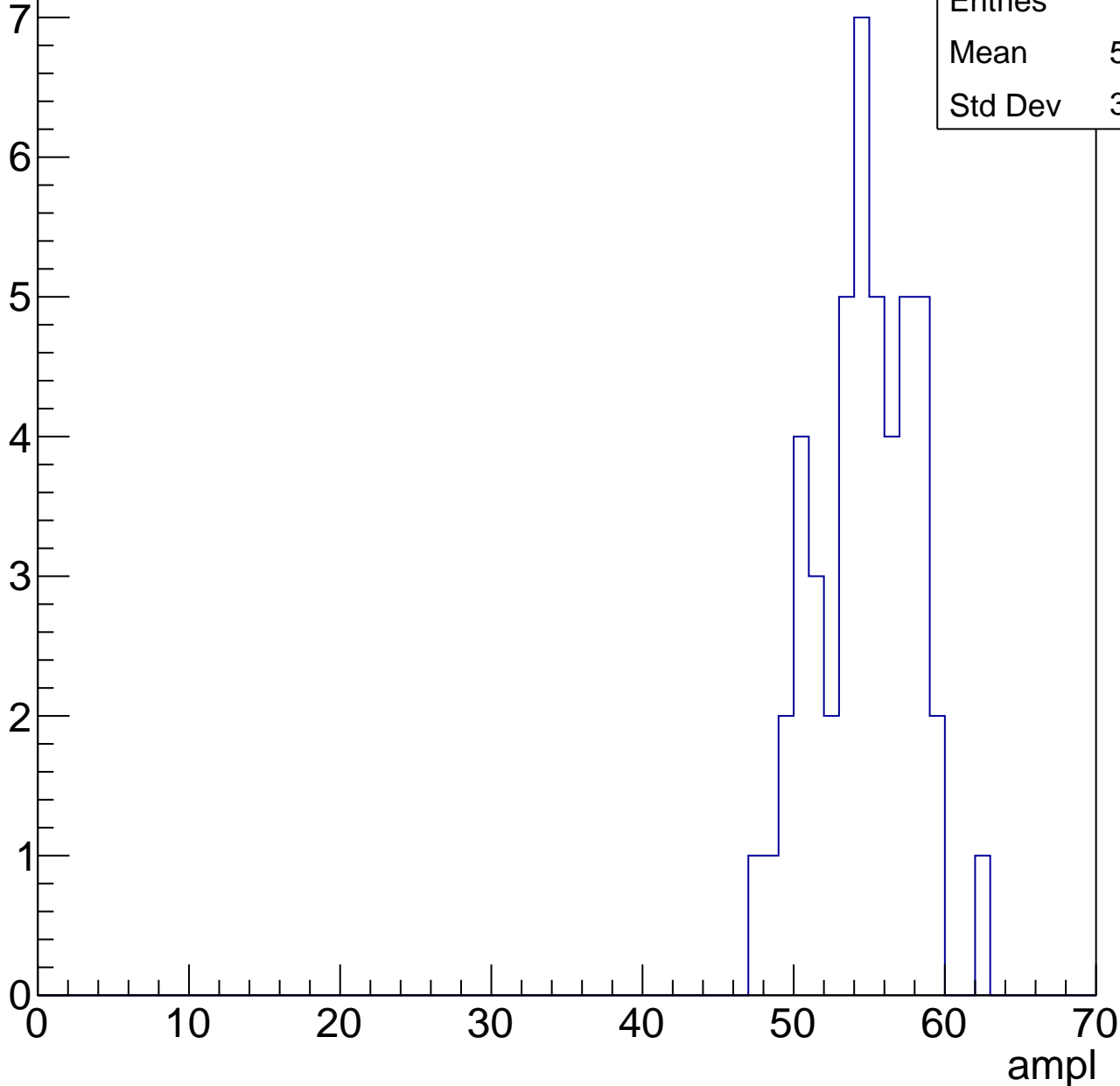


# B1L103S, U3-ch34, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	47
Mean	54.19
Std Dev	3.253



# B1L103S, U3-ch34, adc5

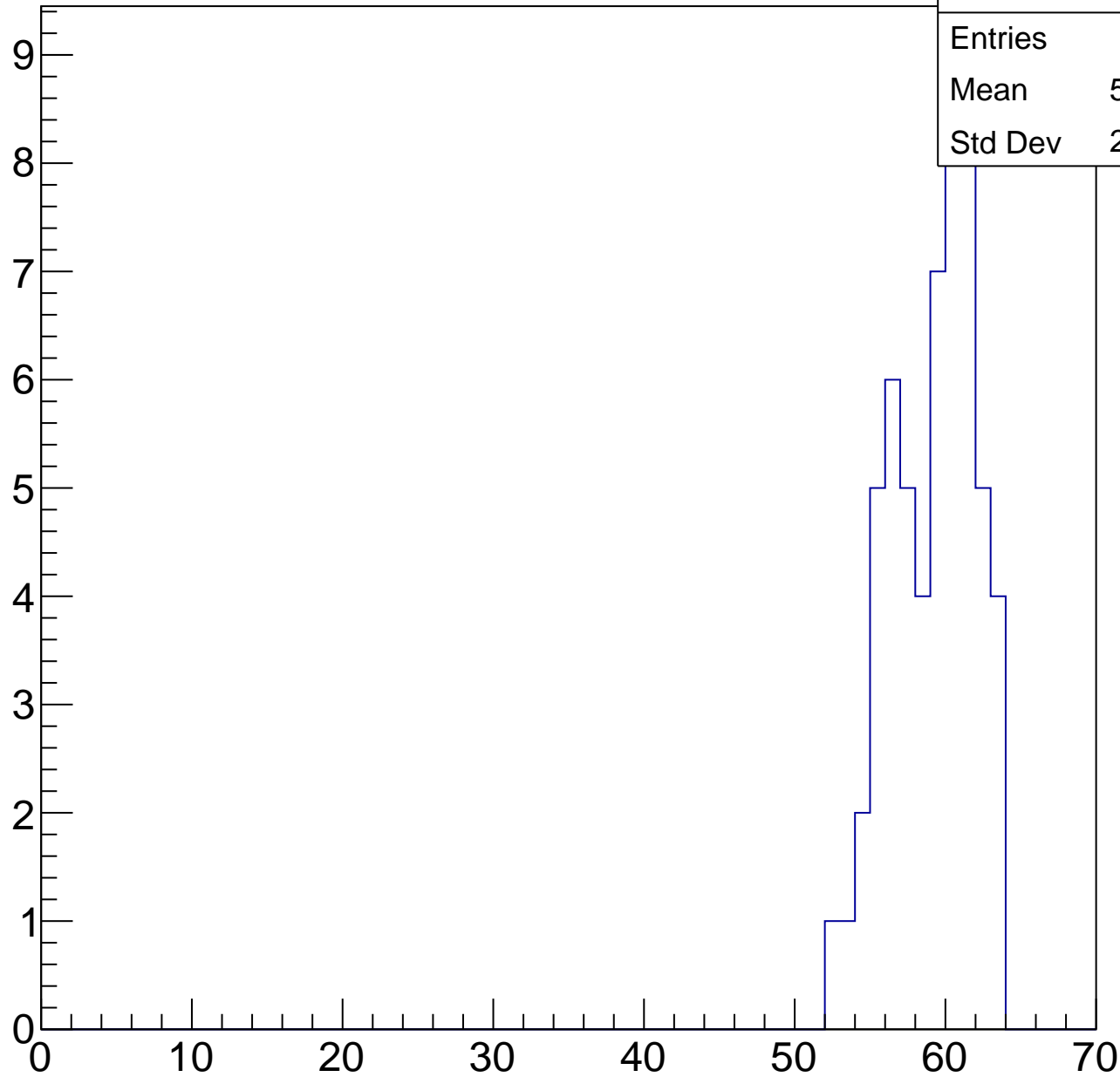
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	57
Mean	58.67
Std Dev	2.768

ampl

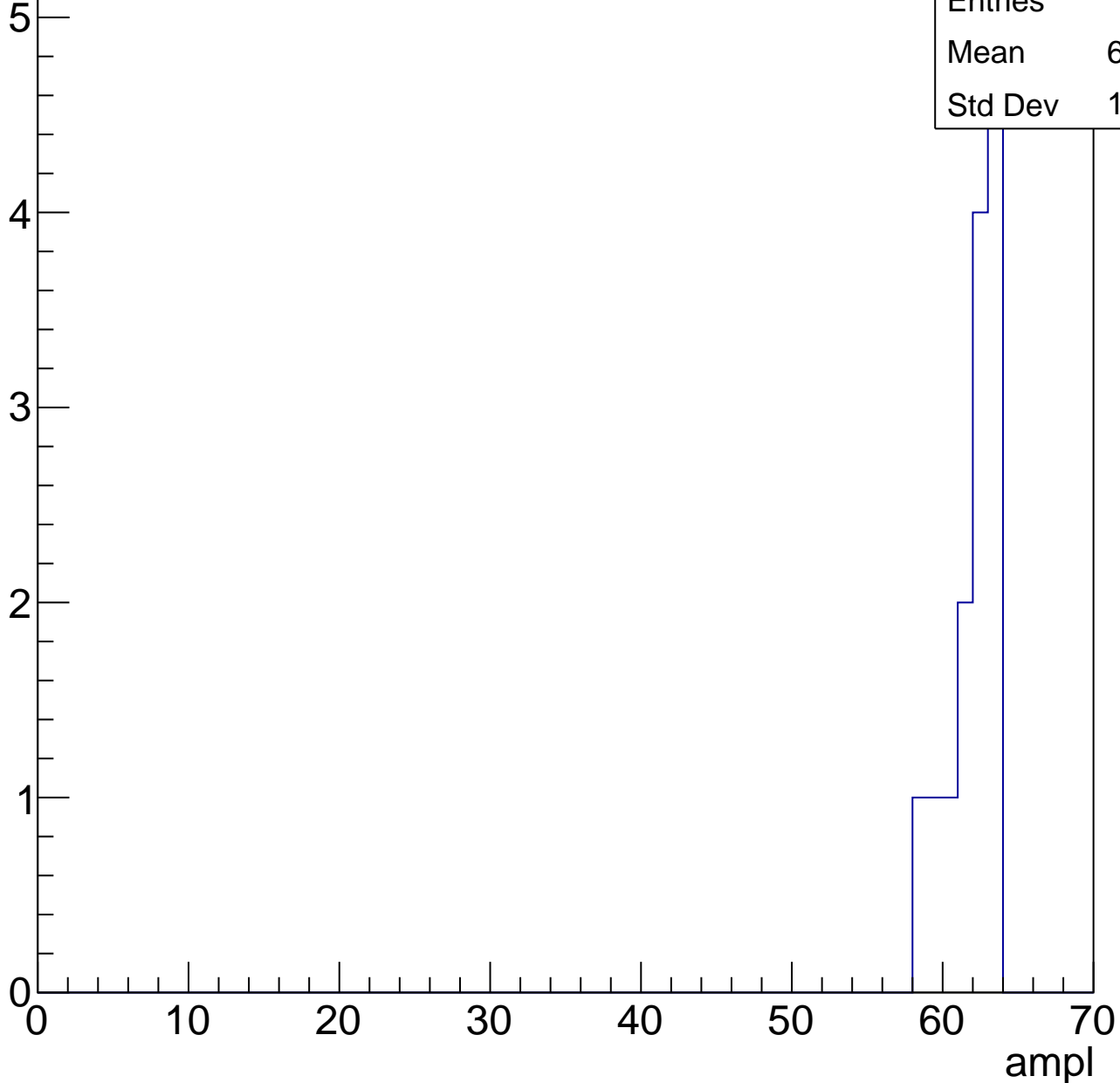


# B1L103S, U3-ch34, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	14
Mean	61.57
Std Dev	1.545

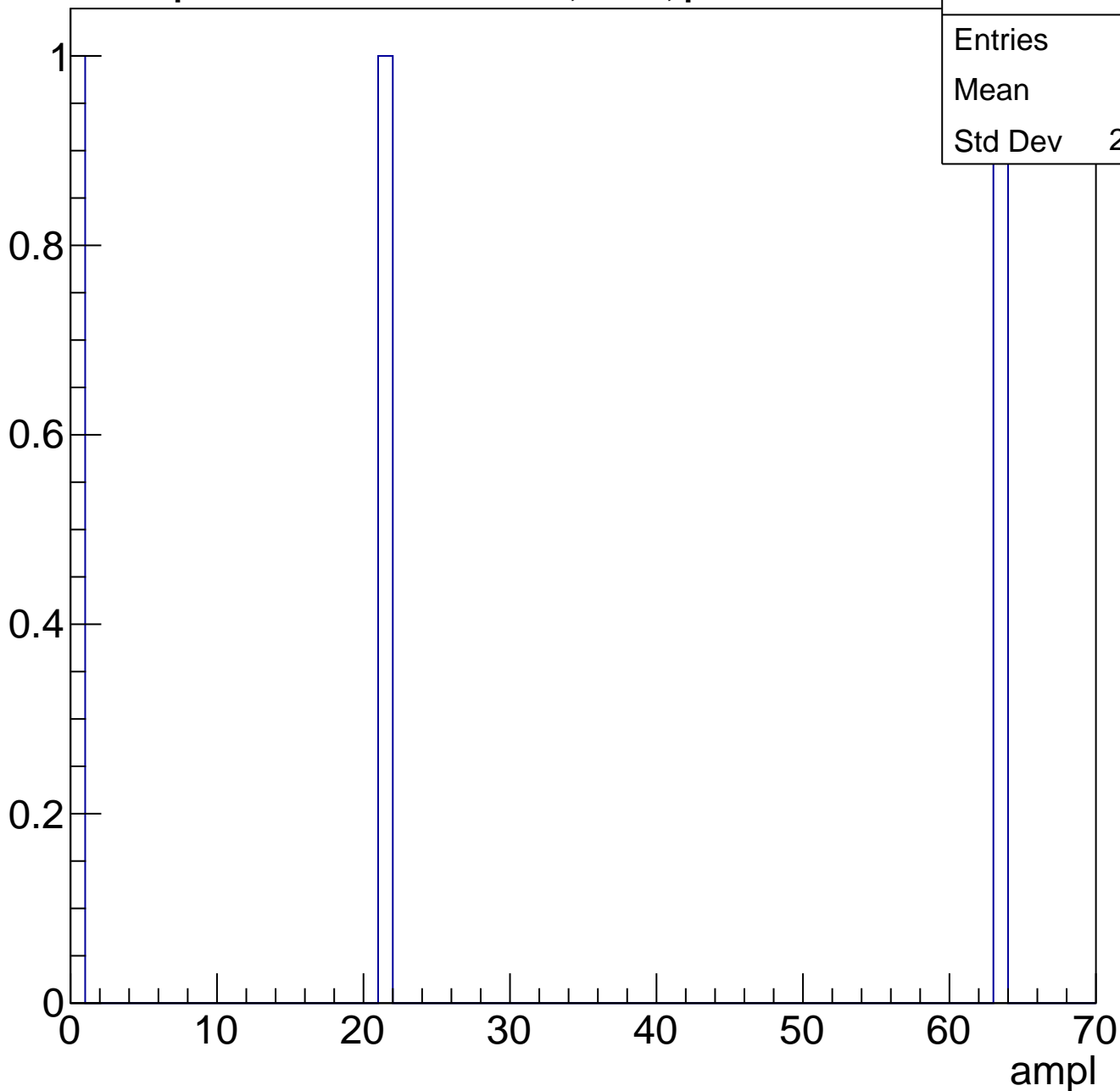




# B1L103S, U3-ch34, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	3
Mean	28
Std Dev	26.19

# B1L103S, U3-ch35, adc0

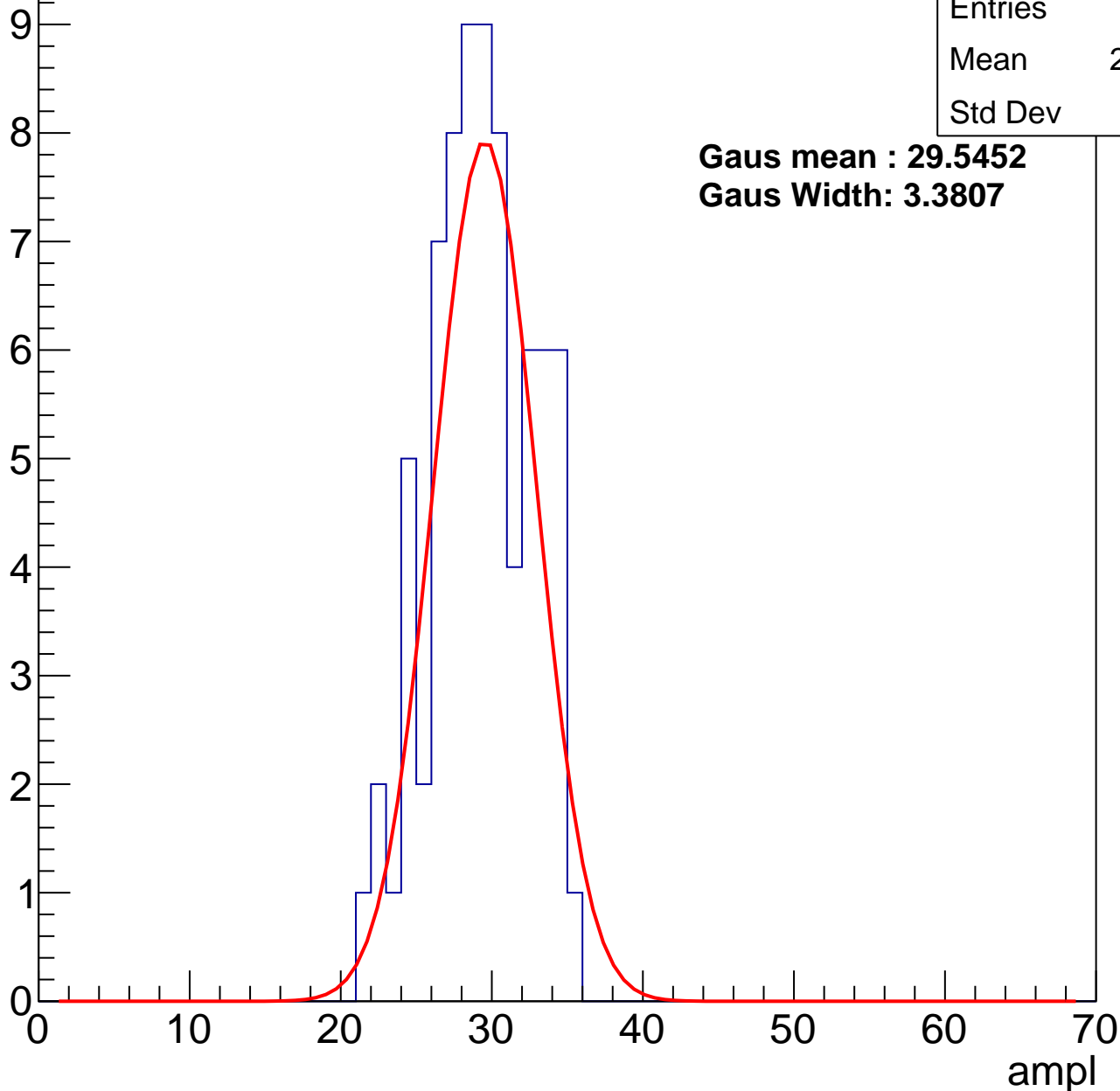
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	28.83
Std Dev	3.3

**Gaus mean : 29.5452**

**Gaus Width: 3.3807**



# B1L103S, U3-ch35, adc1

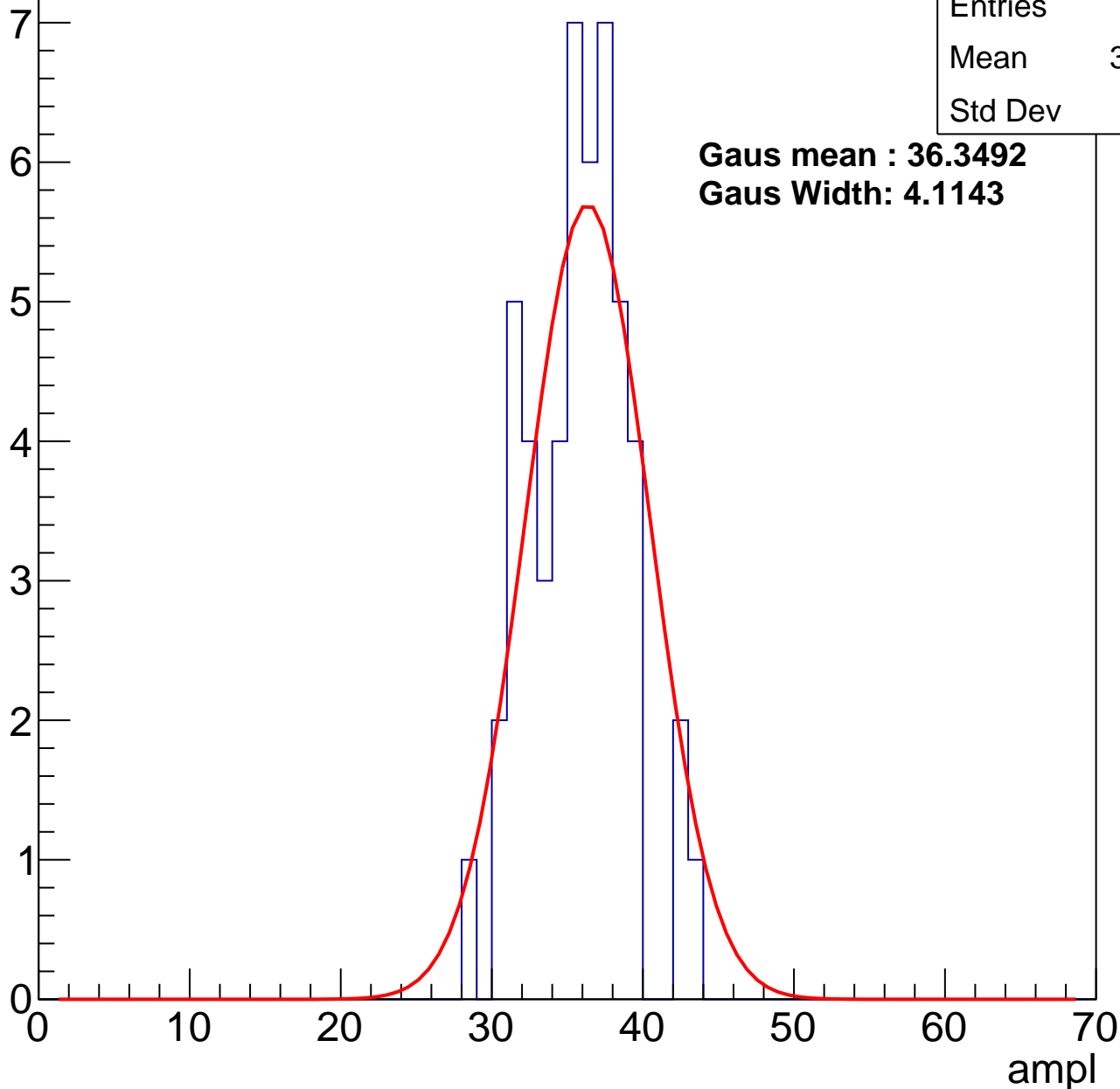
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	35.27
Std Dev	3.23

**Gaus mean : 36.3492**

**Gaus Width: 4.1143**



# B1L103S, U3-ch35, adc2

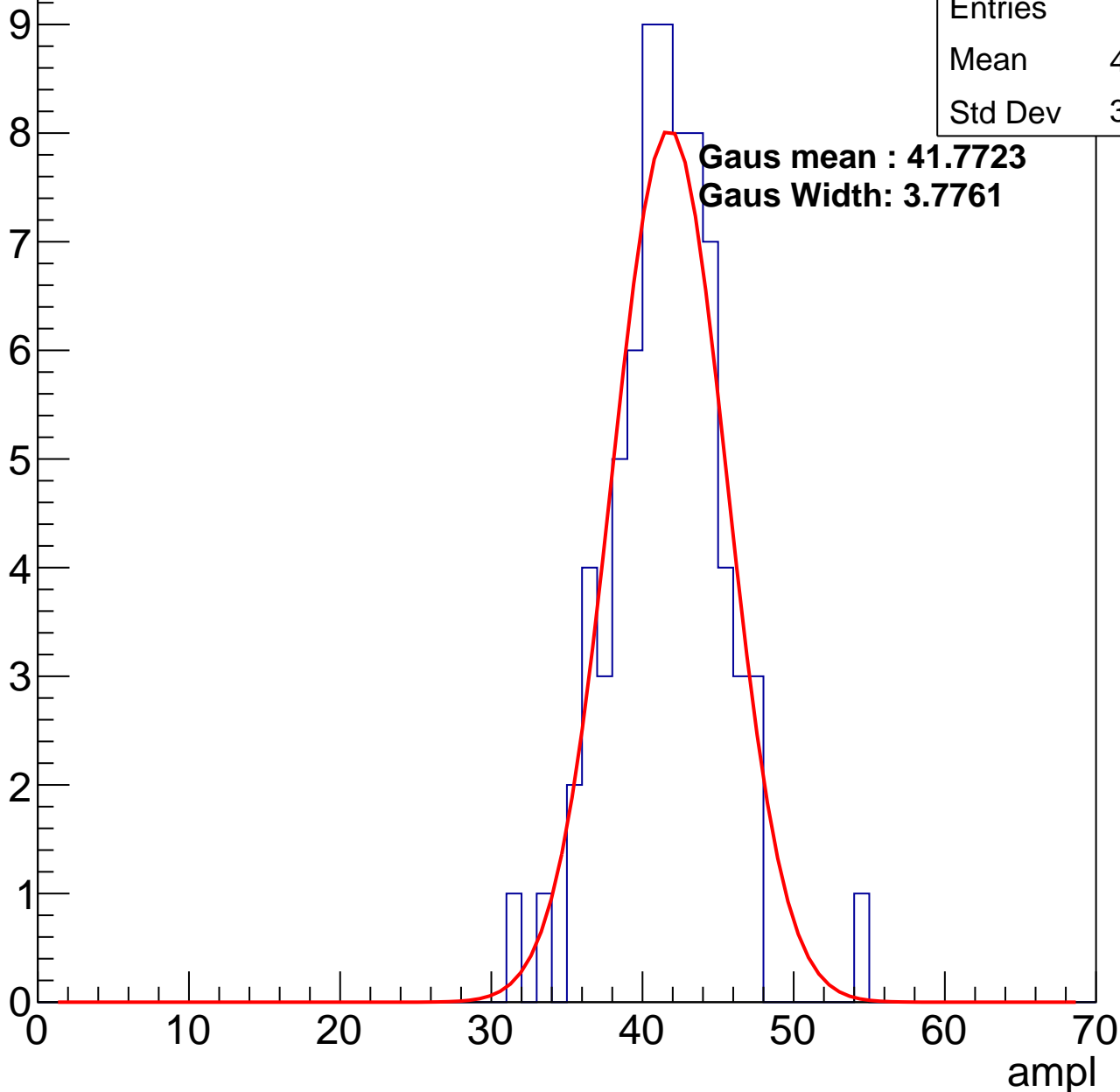
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	41.12
Std Dev	3.639

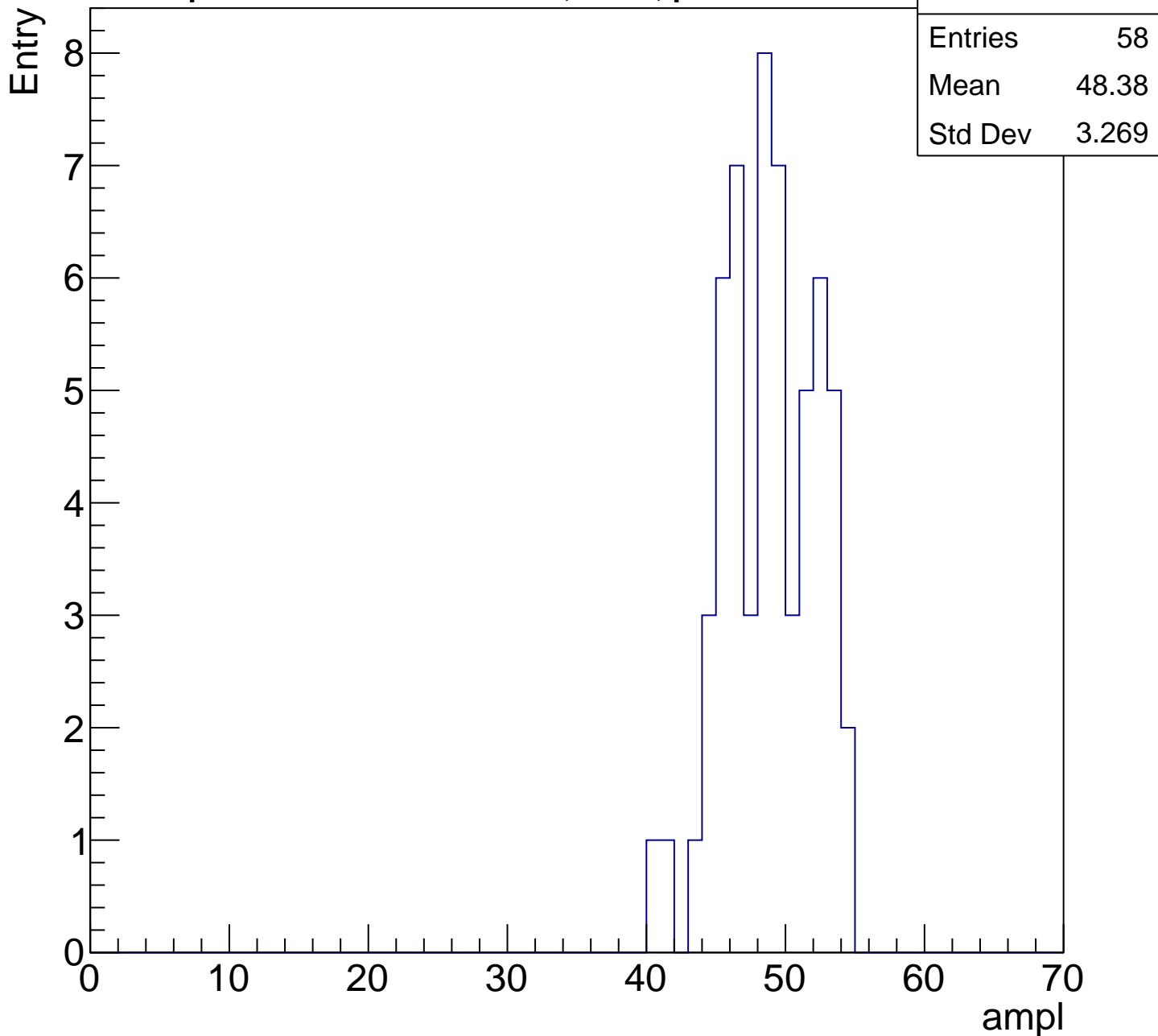
**Gaus mean : 41.7723**

**Gaus Width: 3.7761**



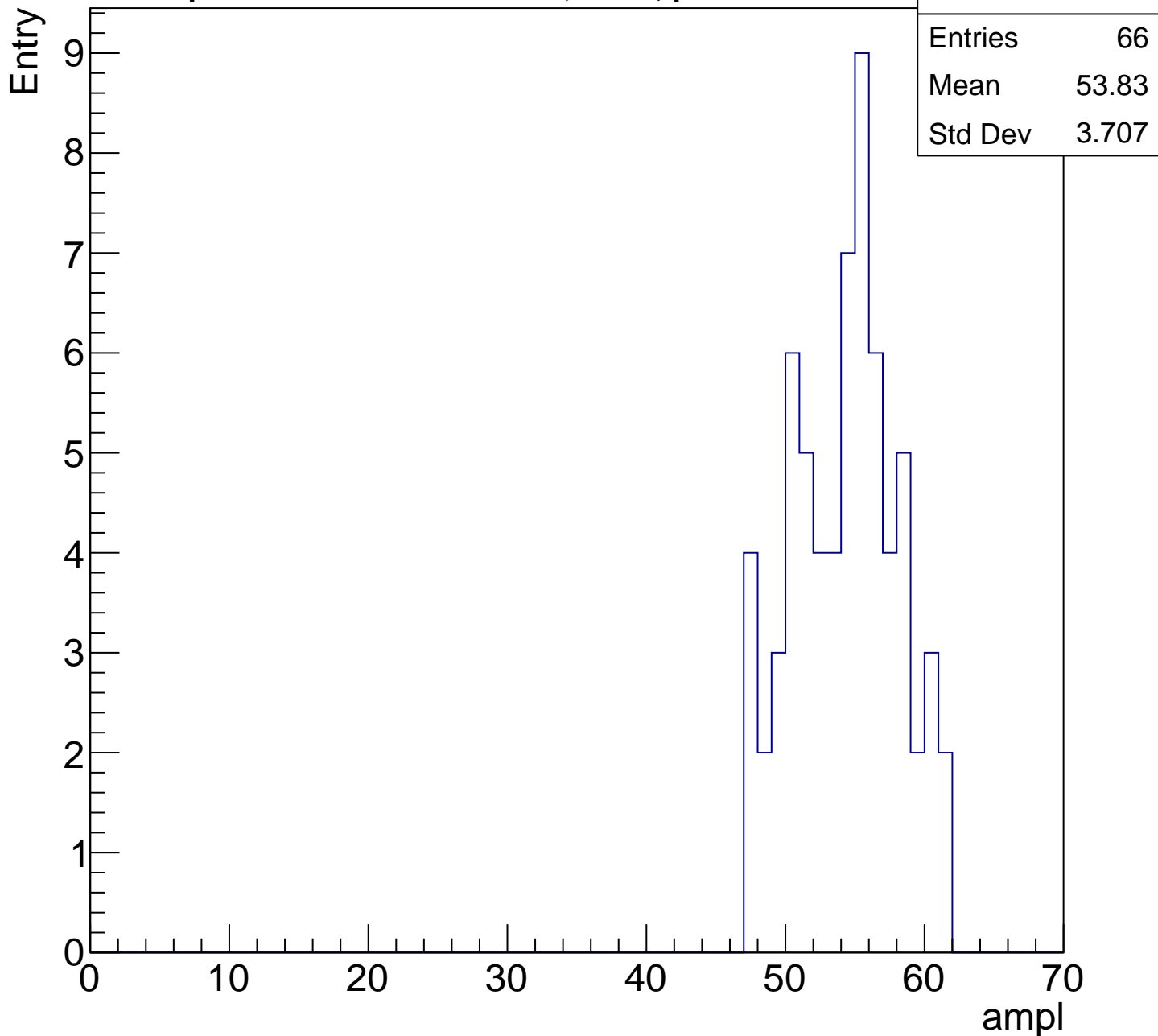
# B1L103S, U3-ch35, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U3-ch35, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

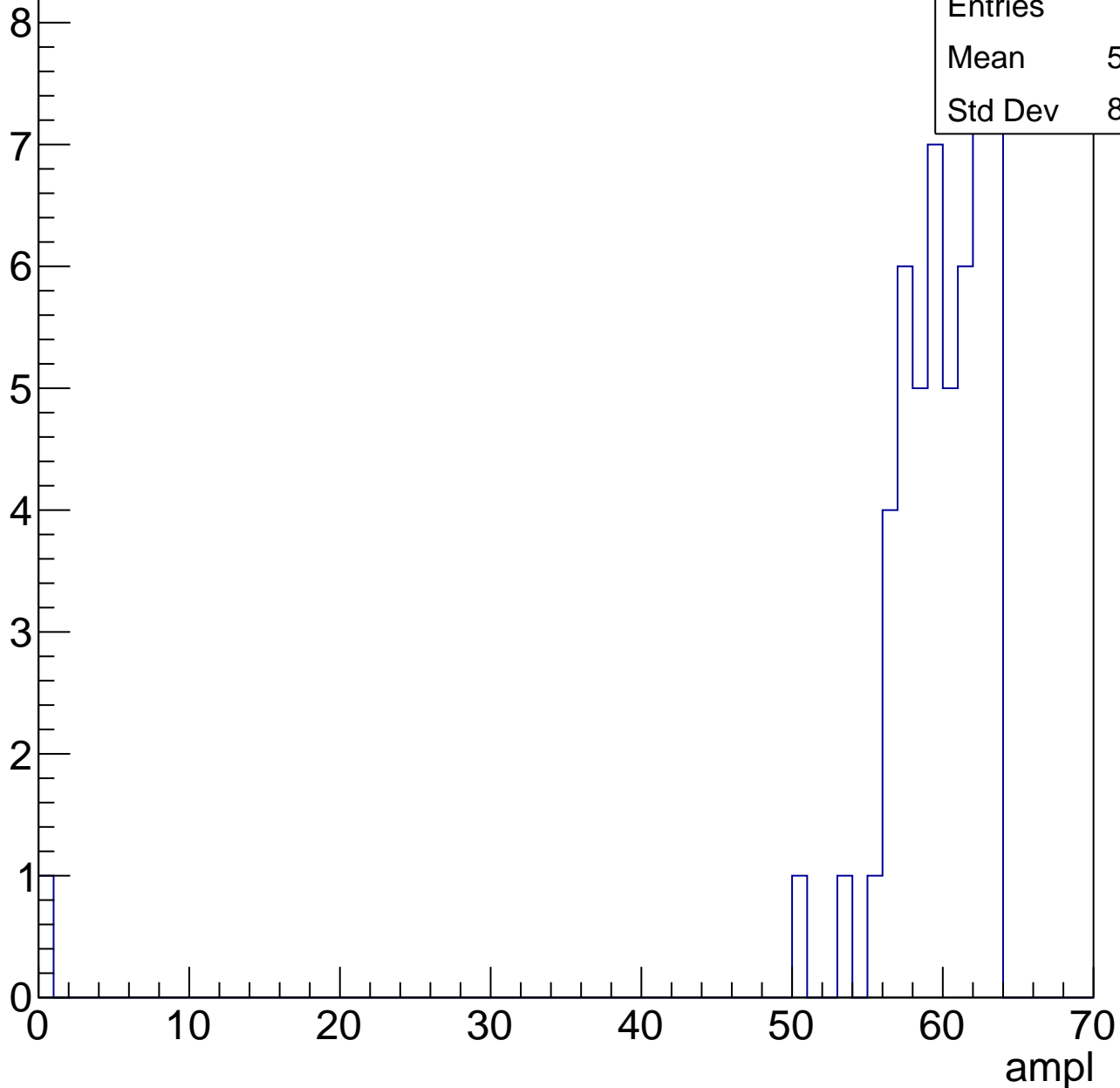


# B1L103S, U3-ch35, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	58.36
Std Dev	8.563



# B1L103S, U3-ch35, adc6

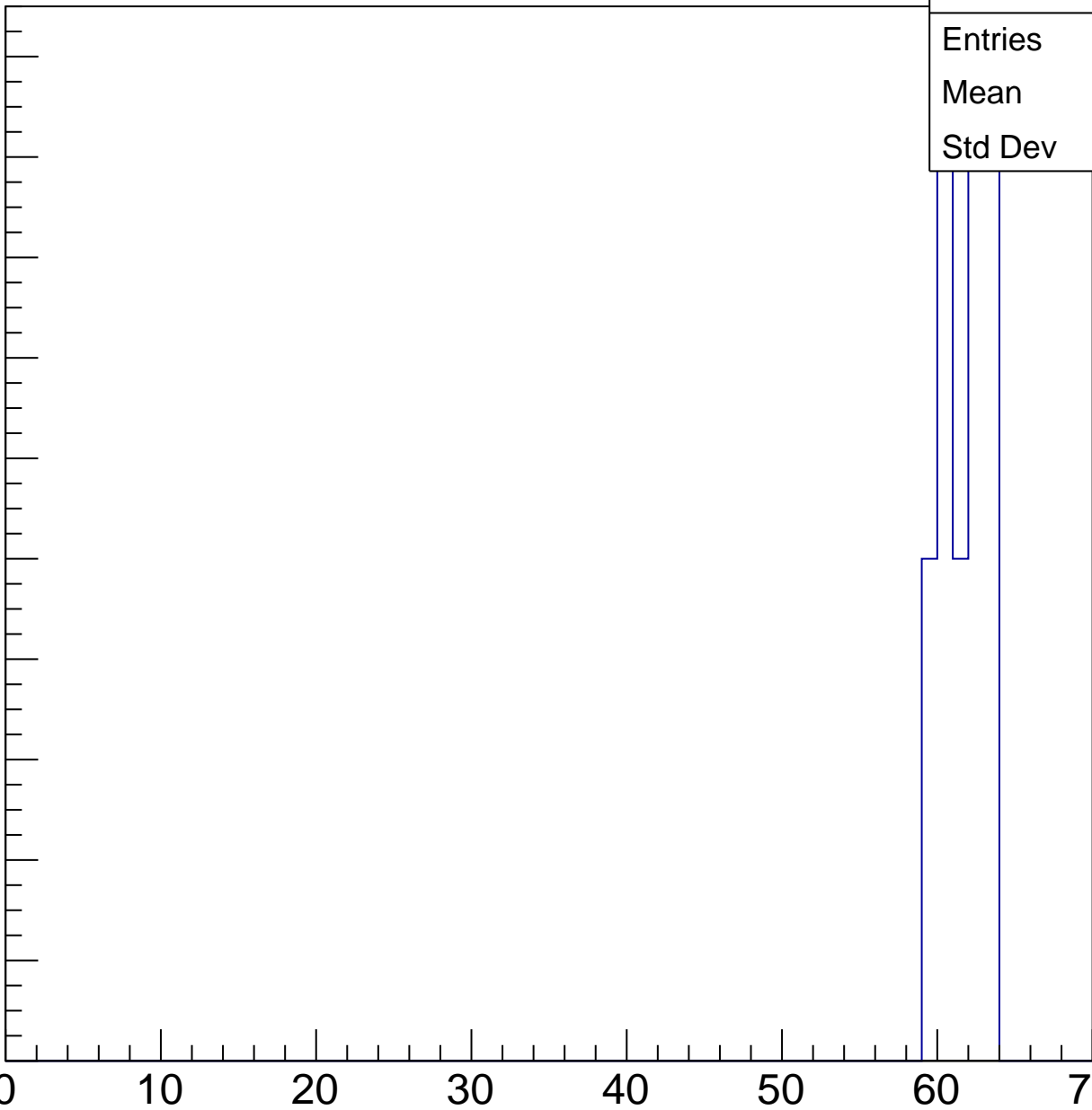
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	8
Mean	61.25
Std Dev	1.392

ampl

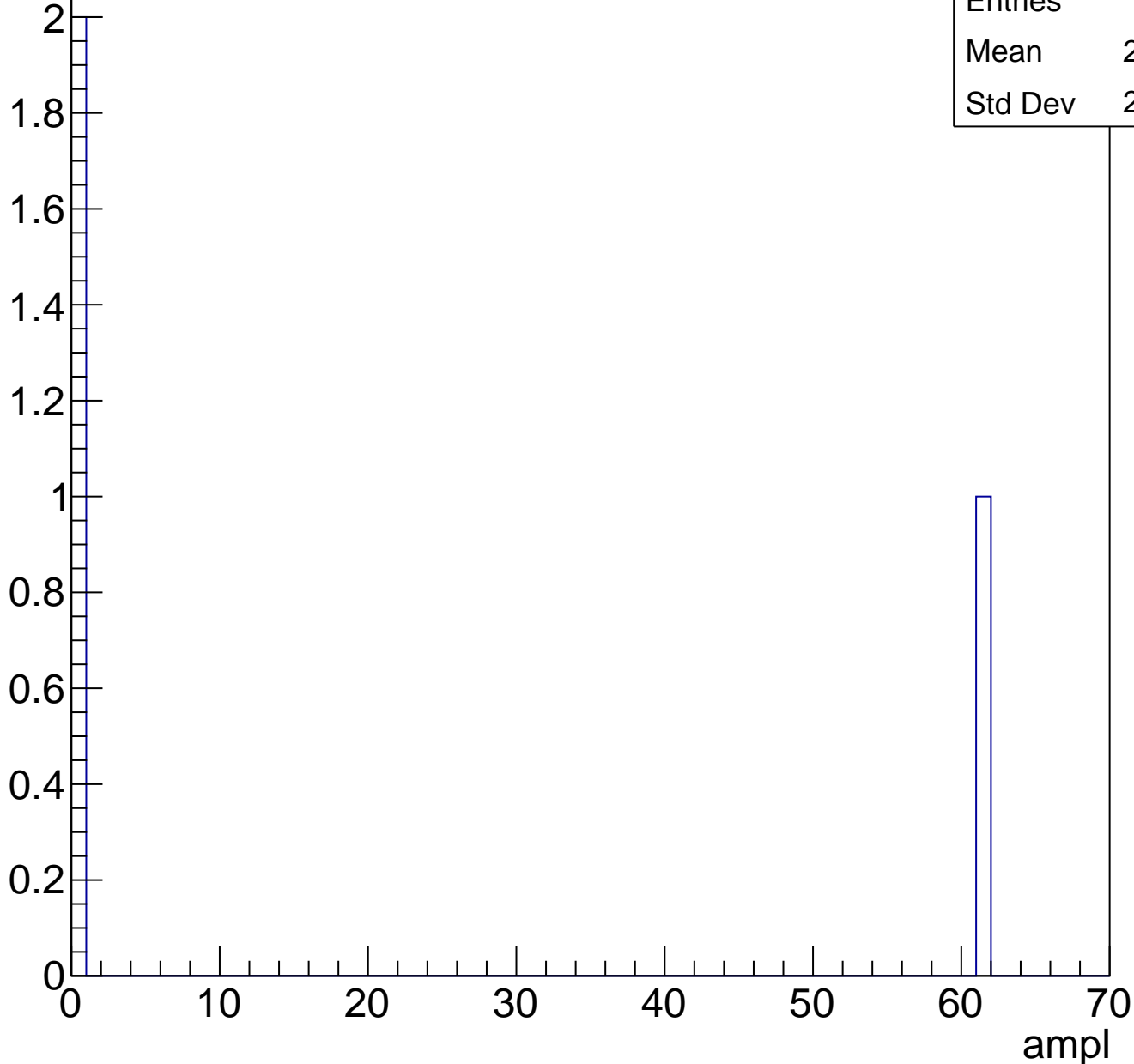




# B1L103S, U3-ch35, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch36, adc0

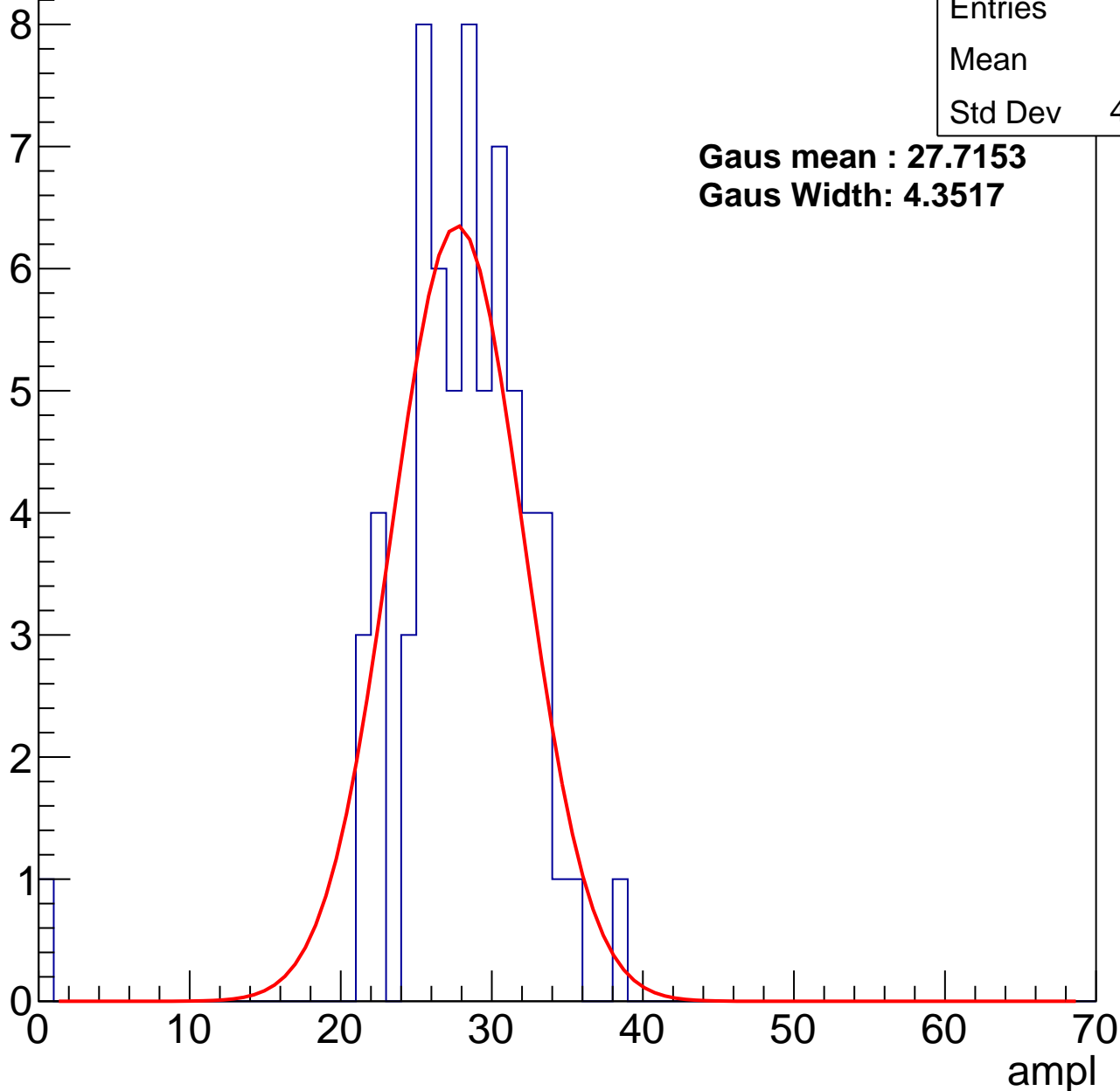
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	27.5
Std Dev	4.976

**Gaus mean : 27.7153**

**Gaus Width: 4.3517**



# B1L103S, U3-ch36, adc1

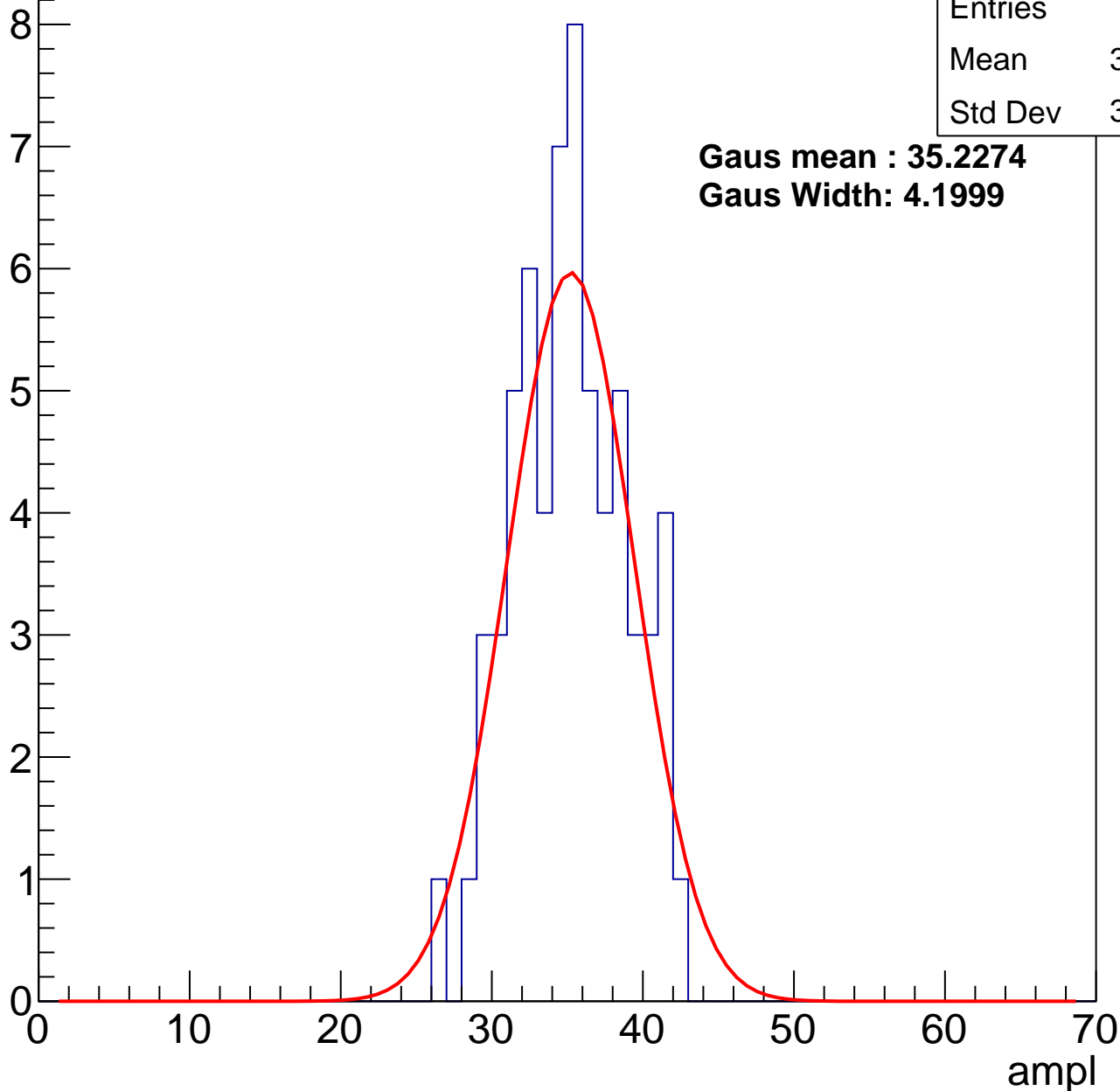
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	34.75
Std Dev	3.669

**Gaus mean : 35.2274**

**Gaus Width: 4.1999**



# B1L103S, U3-ch36, adc2

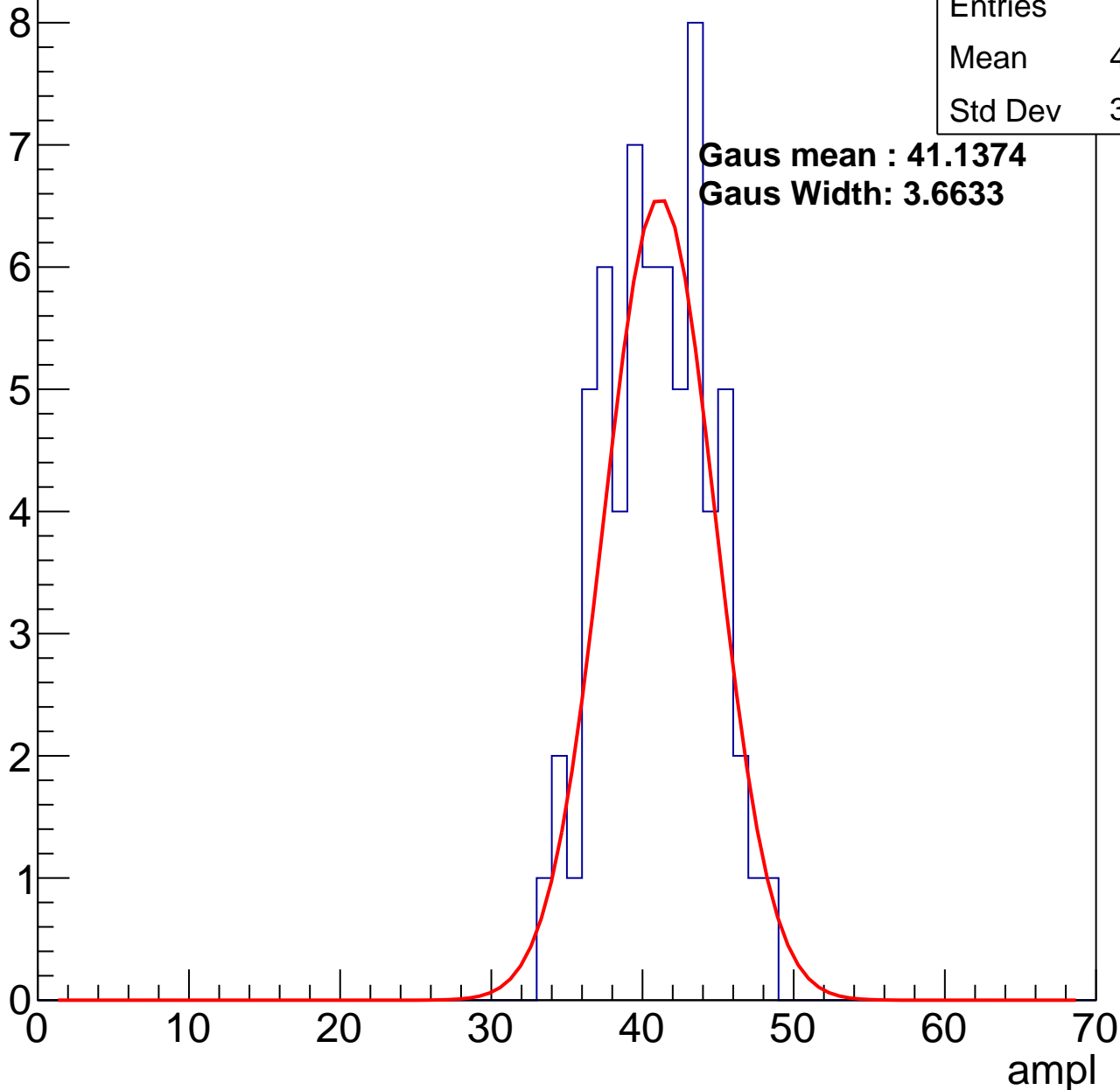
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	40.48
Std Dev	3.446

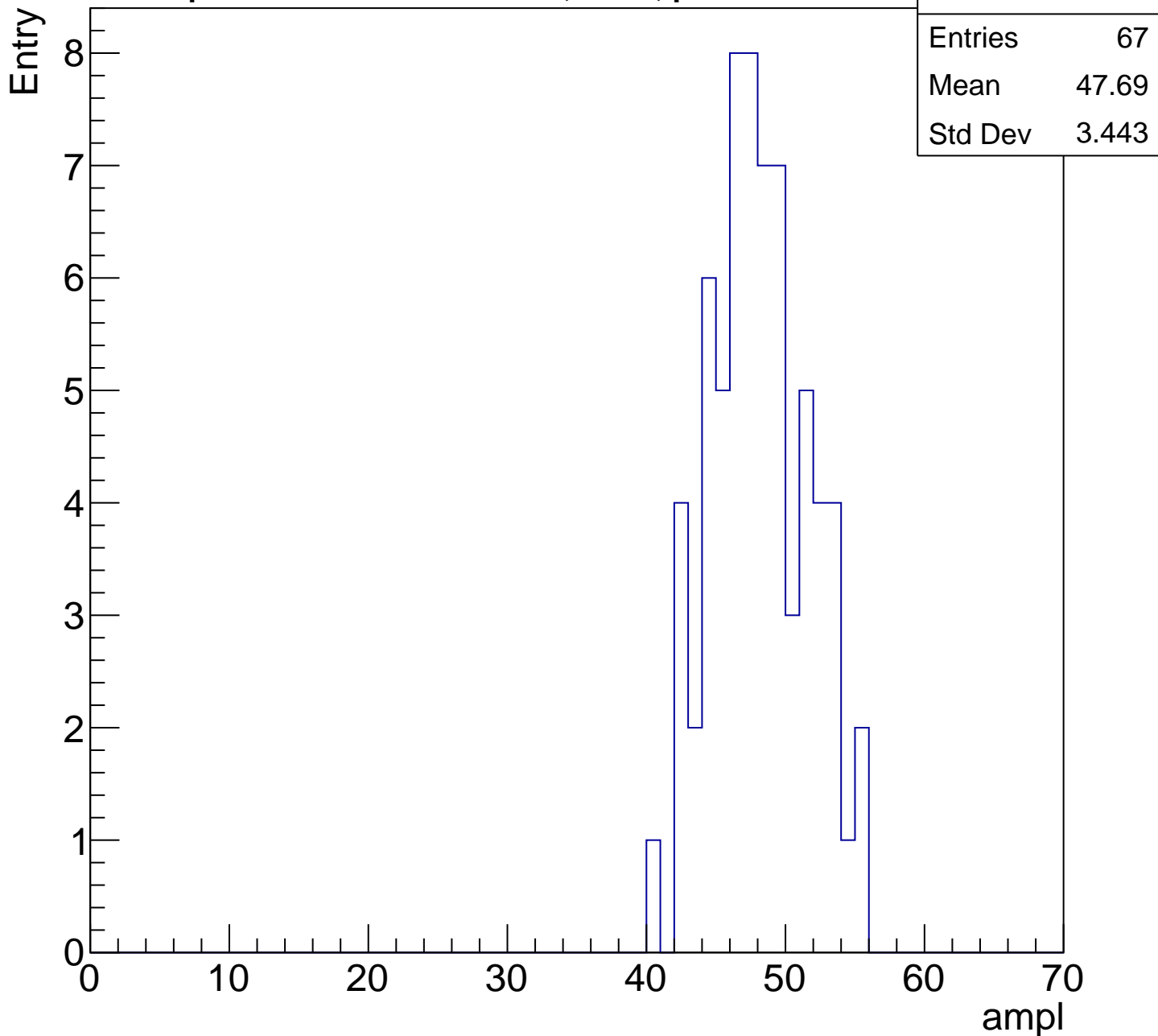
**Gaus mean : 41.1374**

**Gaus Width: 3.6633**



# B1L103S, U3-ch36, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

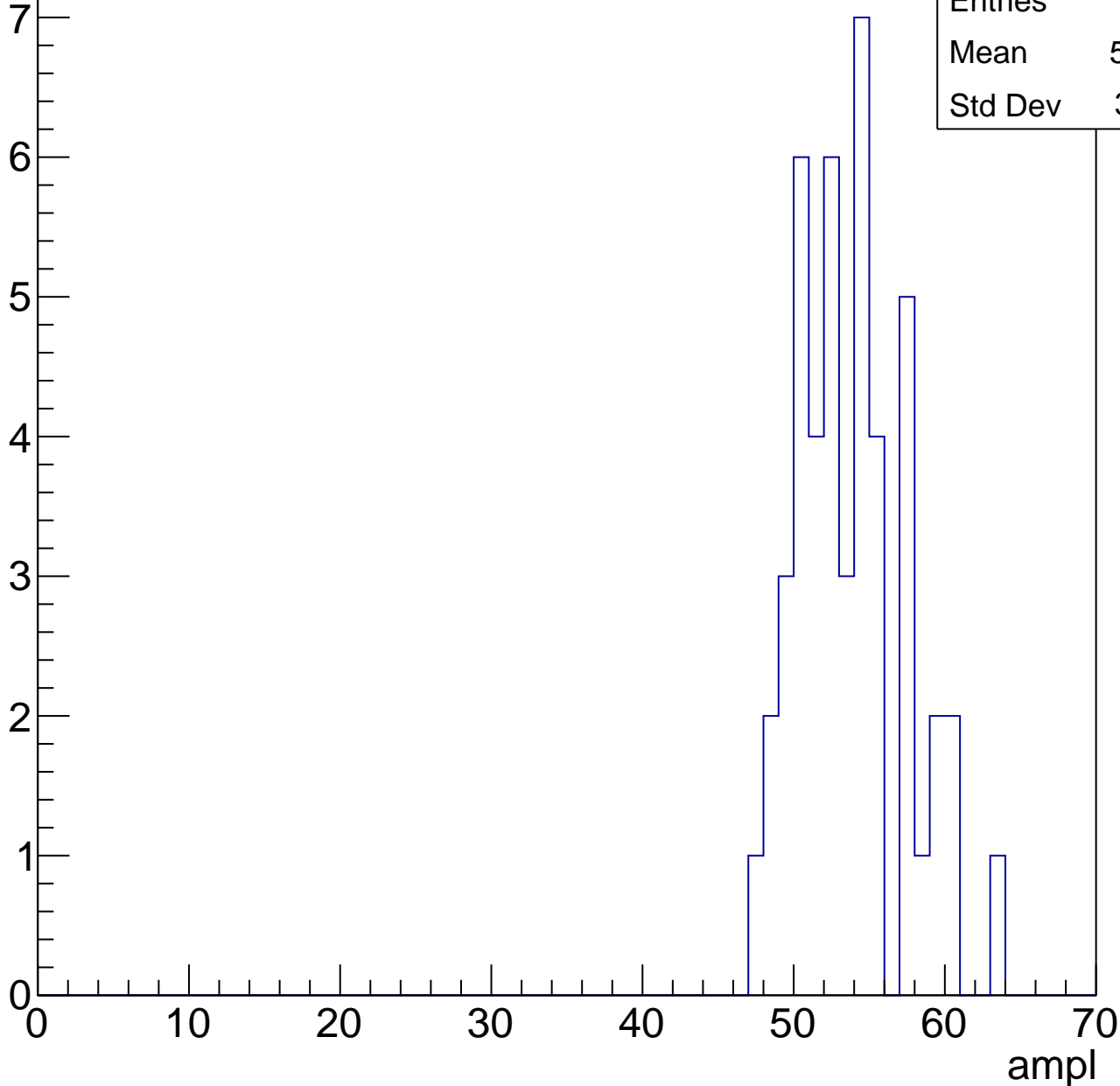


# B1L103S, U3-ch36, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

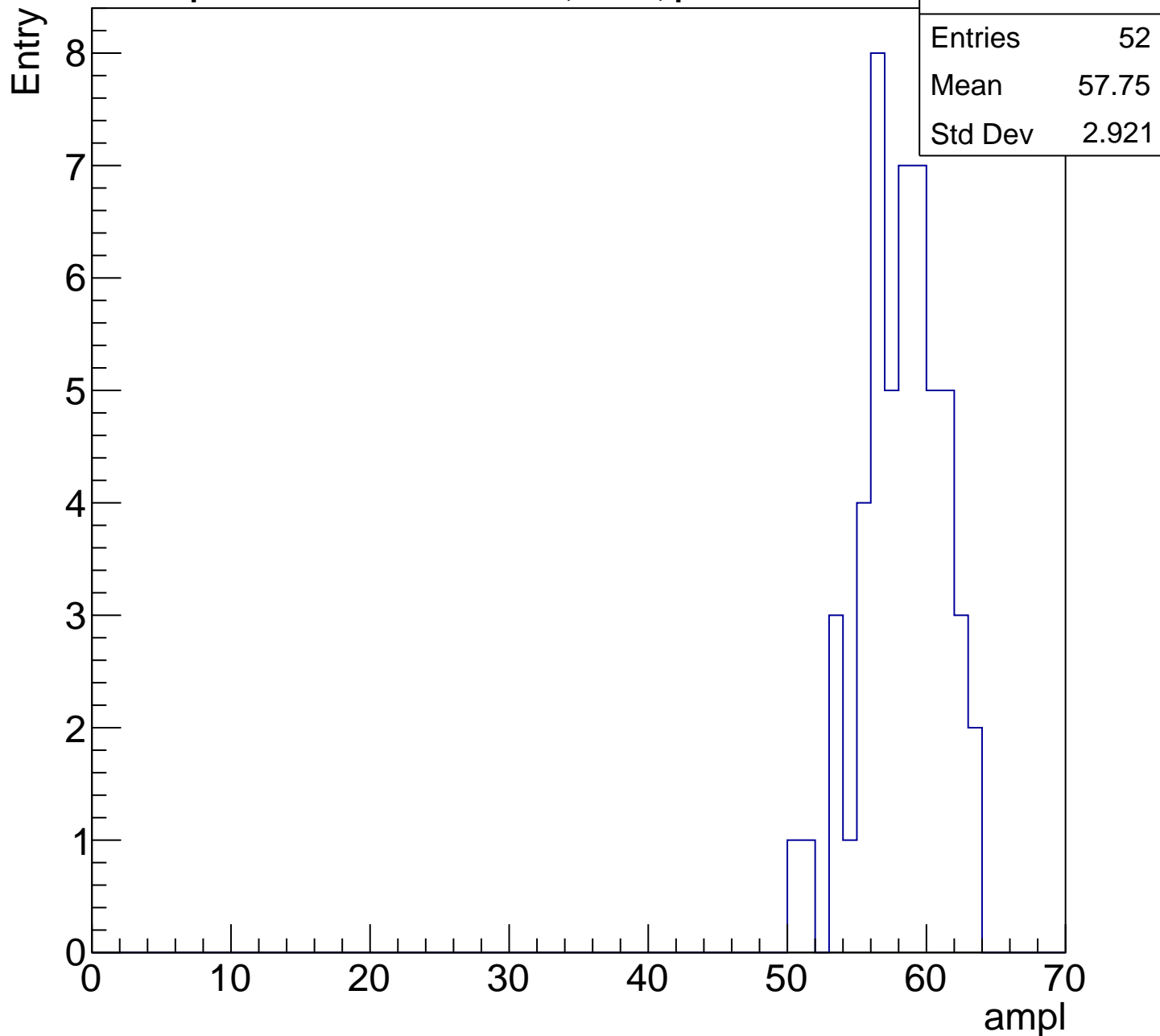
Entry

Entries	47
Mean	53.34
Std Dev	3.581



# B1L103S, U3-ch36, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

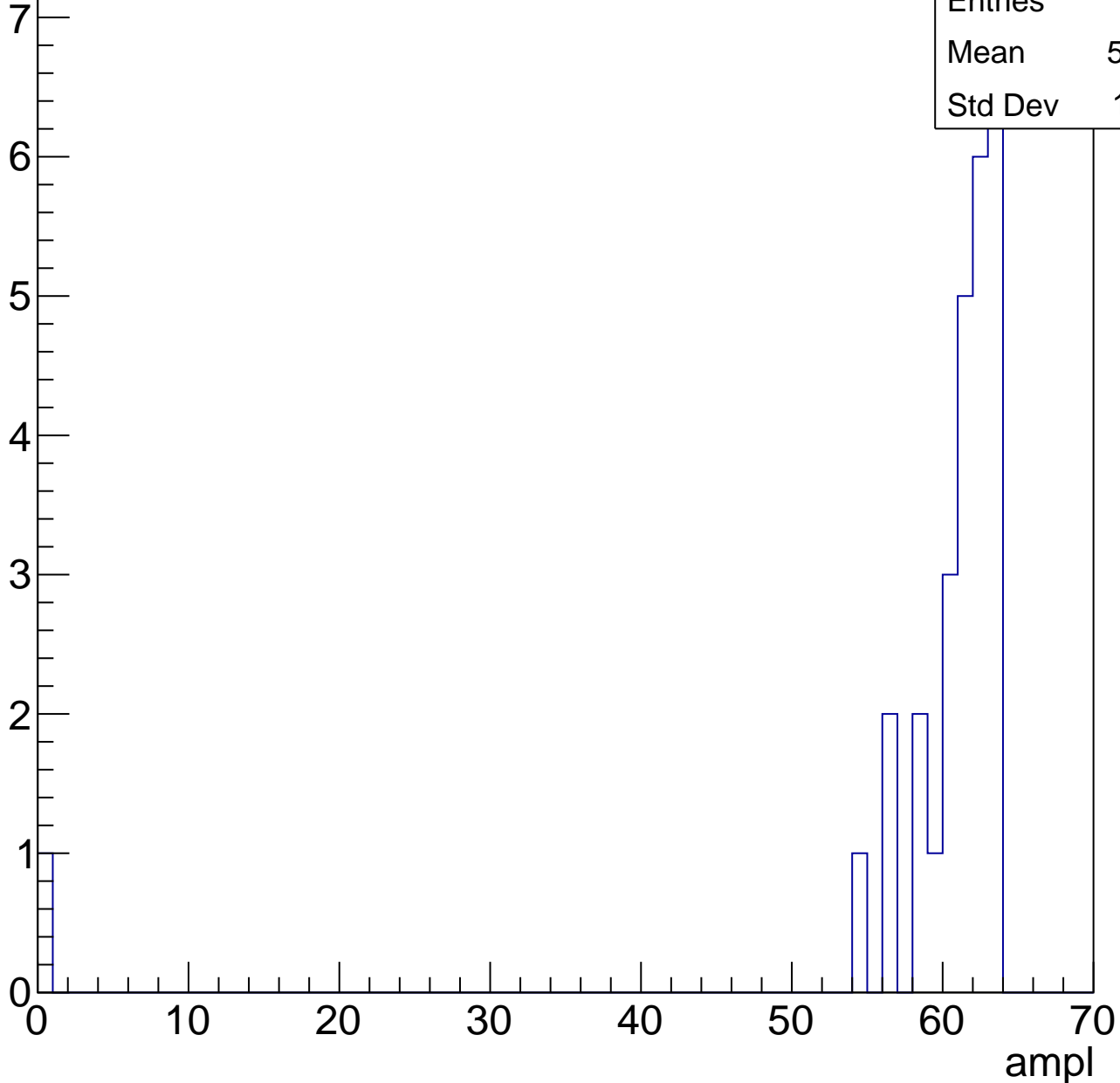


# B1L103S, U3-ch36, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	28
Mean	58.54
Std Dev	11.51

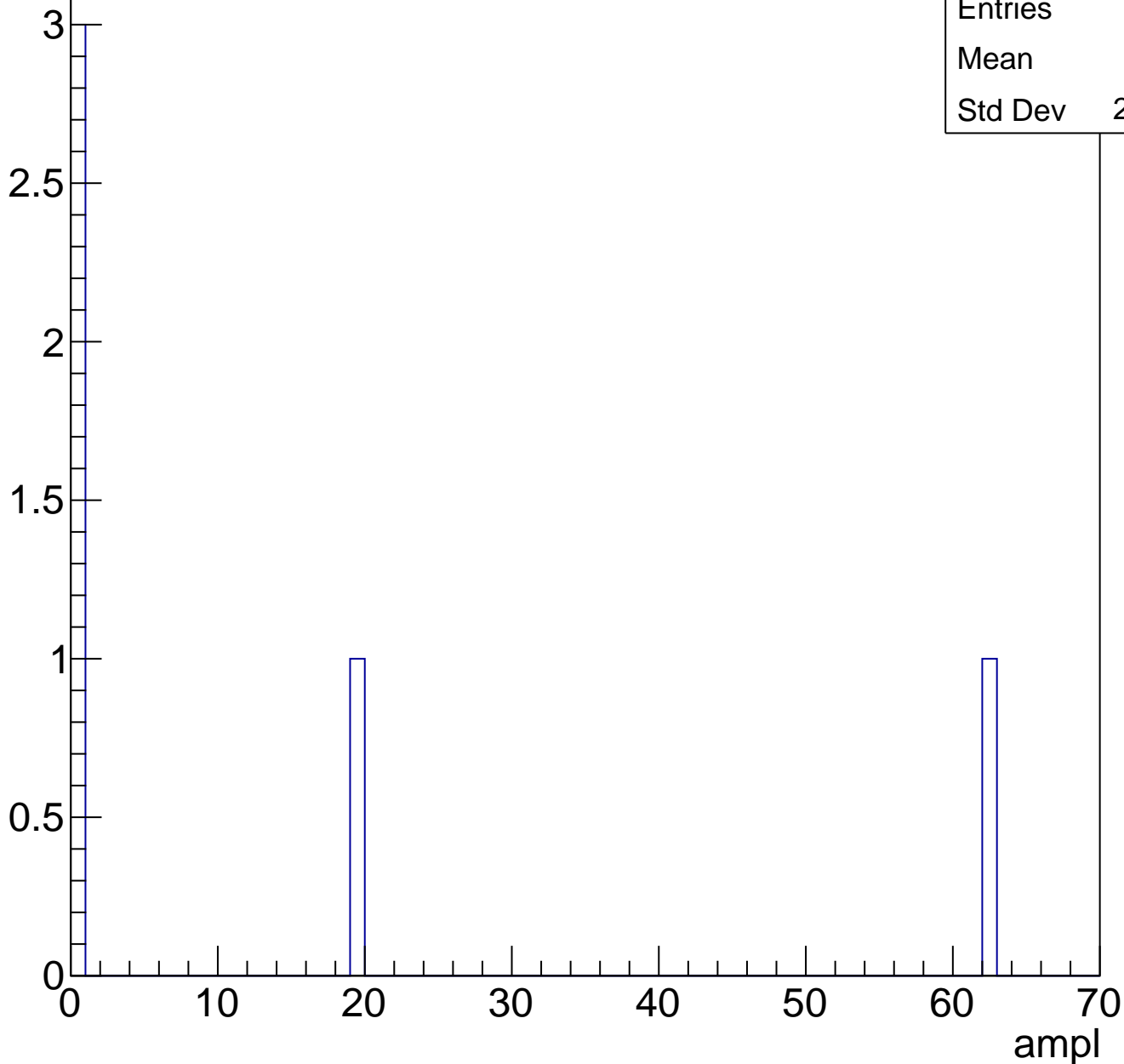




# B1L103S, U3-ch36, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	5
Mean	16.2
Std Dev	24.05

# B1L103S, U3-ch37, adc0

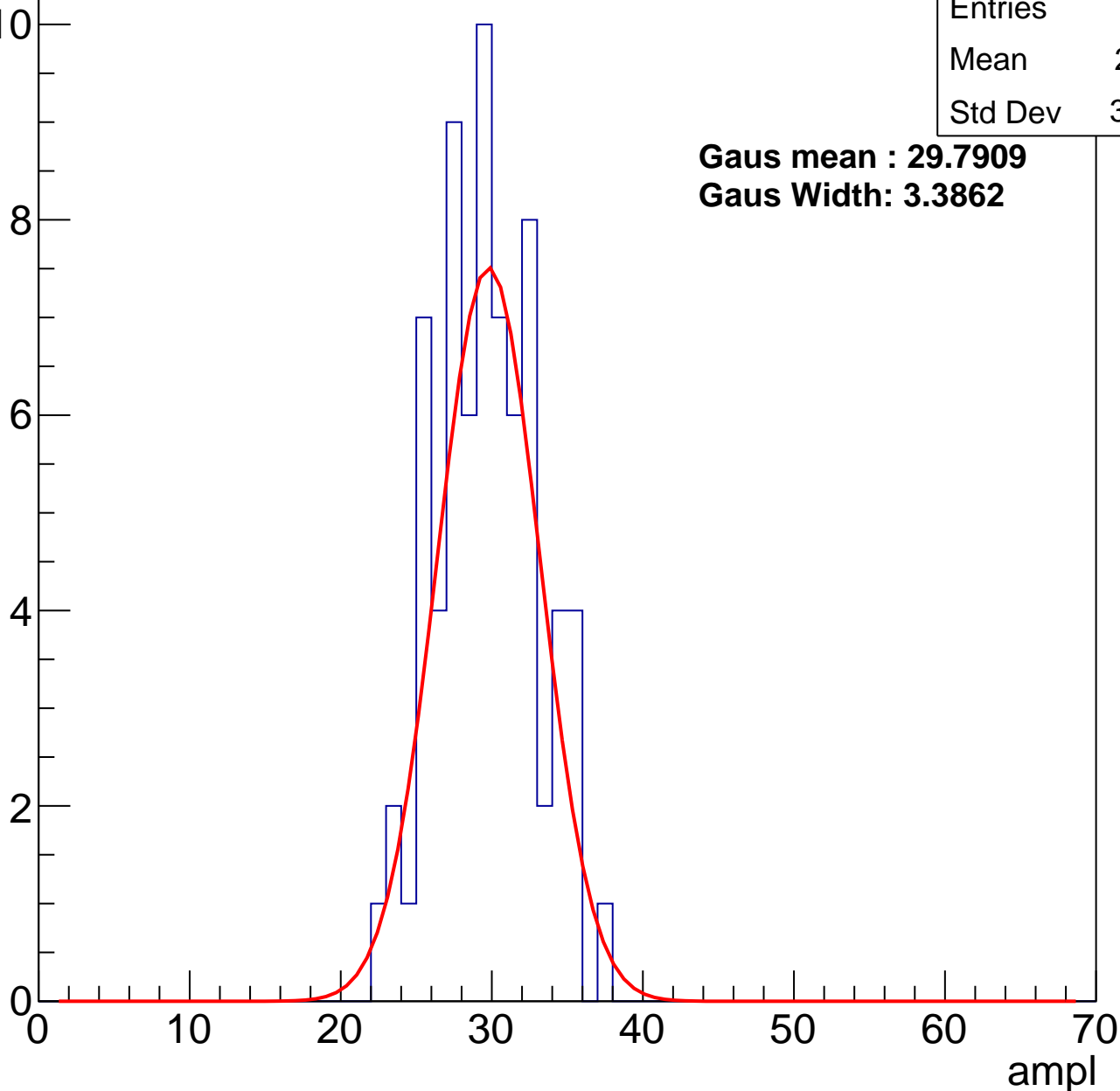
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	29.21
Std Dev	3.283

**Gaus mean : 29.7909**

**Gaus Width: 3.3862**



# B1L103S, U3-ch37, adc1

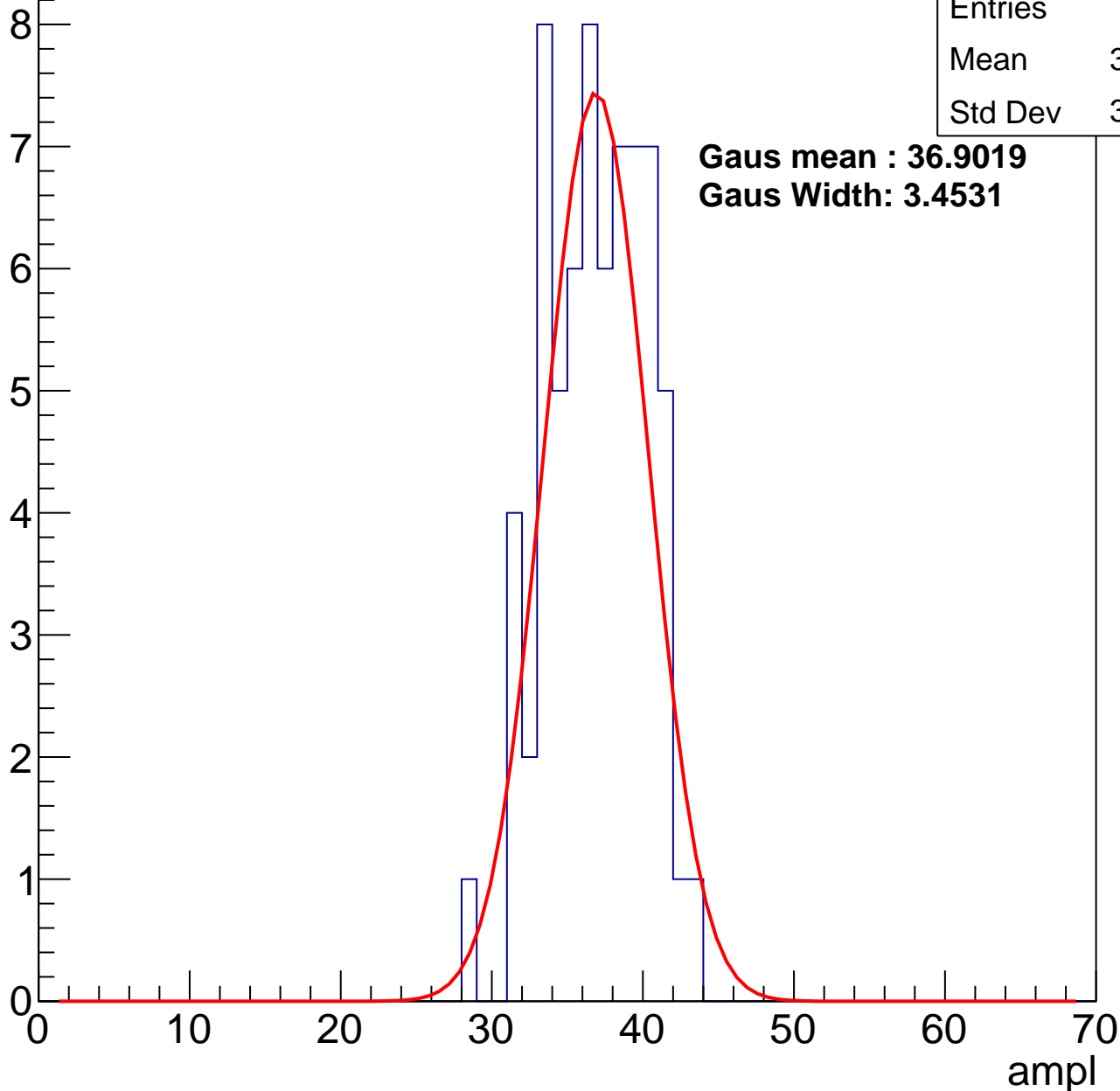
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	36.46
Std Dev	3.206

**Gaus mean : 36.9019**

**Gaus Width: 3.4531**



# B1L103S, U3-ch37, adc2

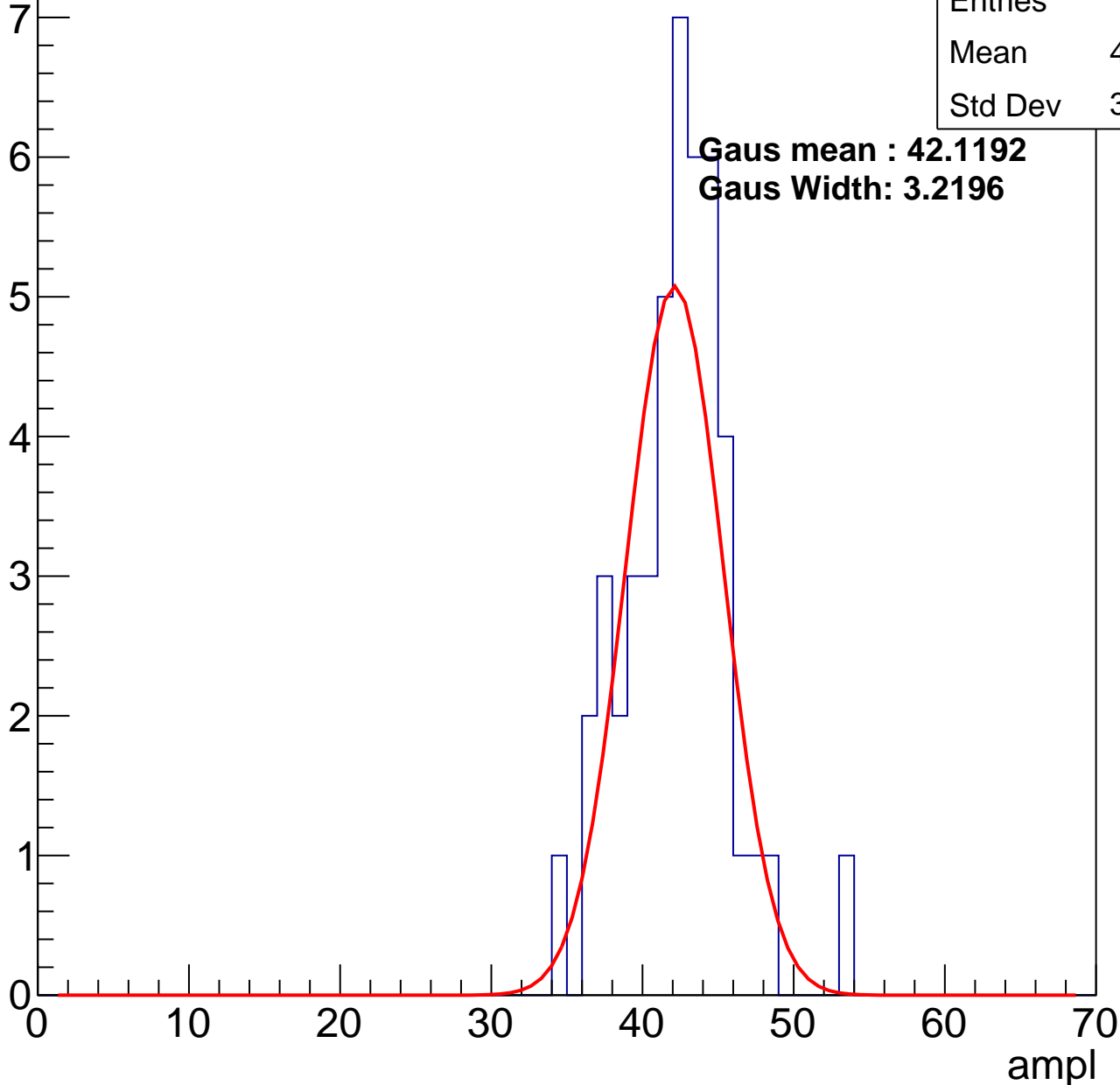
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	46
Mean	41.85
Std Dev	3.458

**Gaus mean : 42.1192**

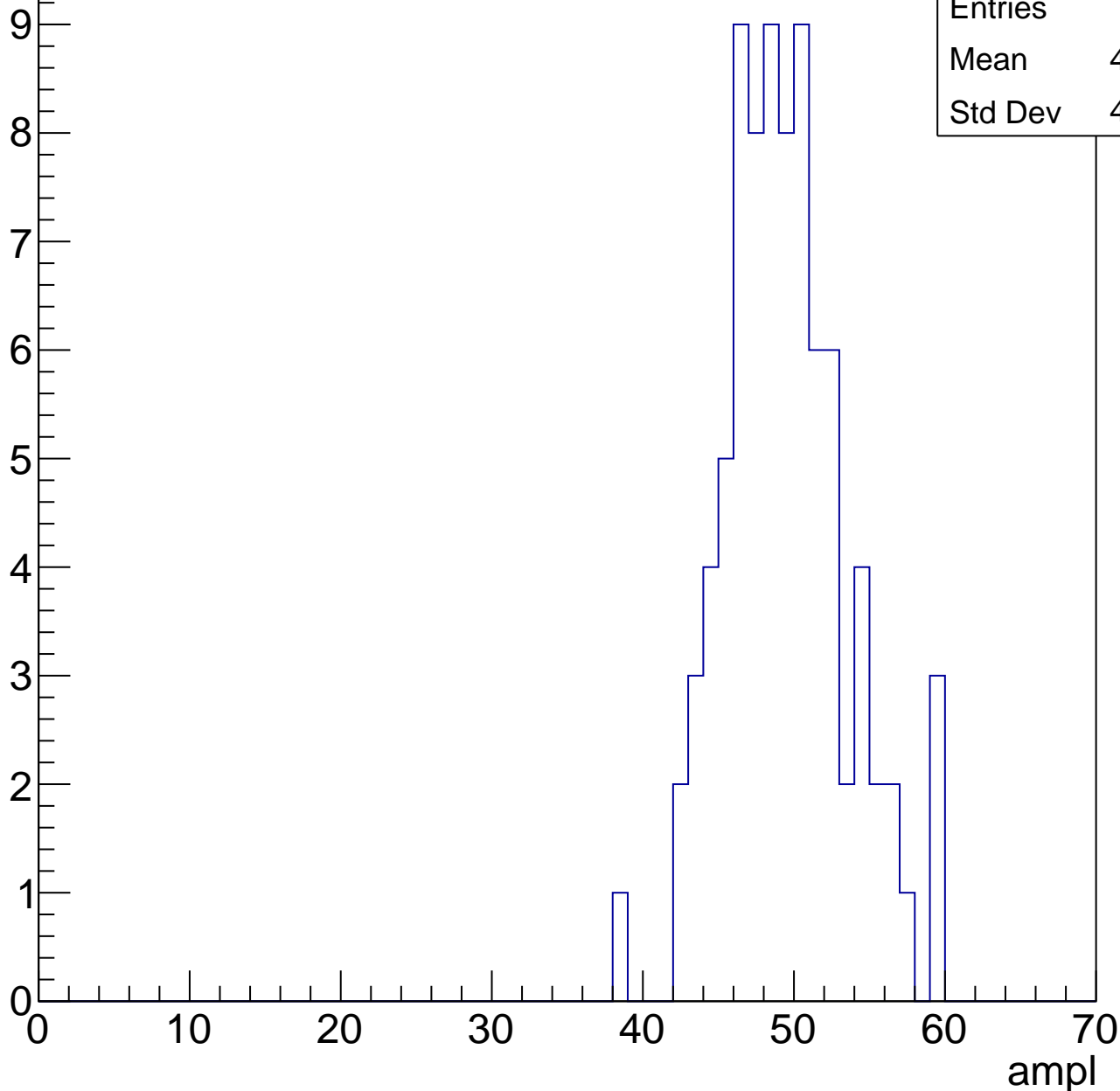
**Gaus Width: 3.2196**



# B1L103S, U3-ch37, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

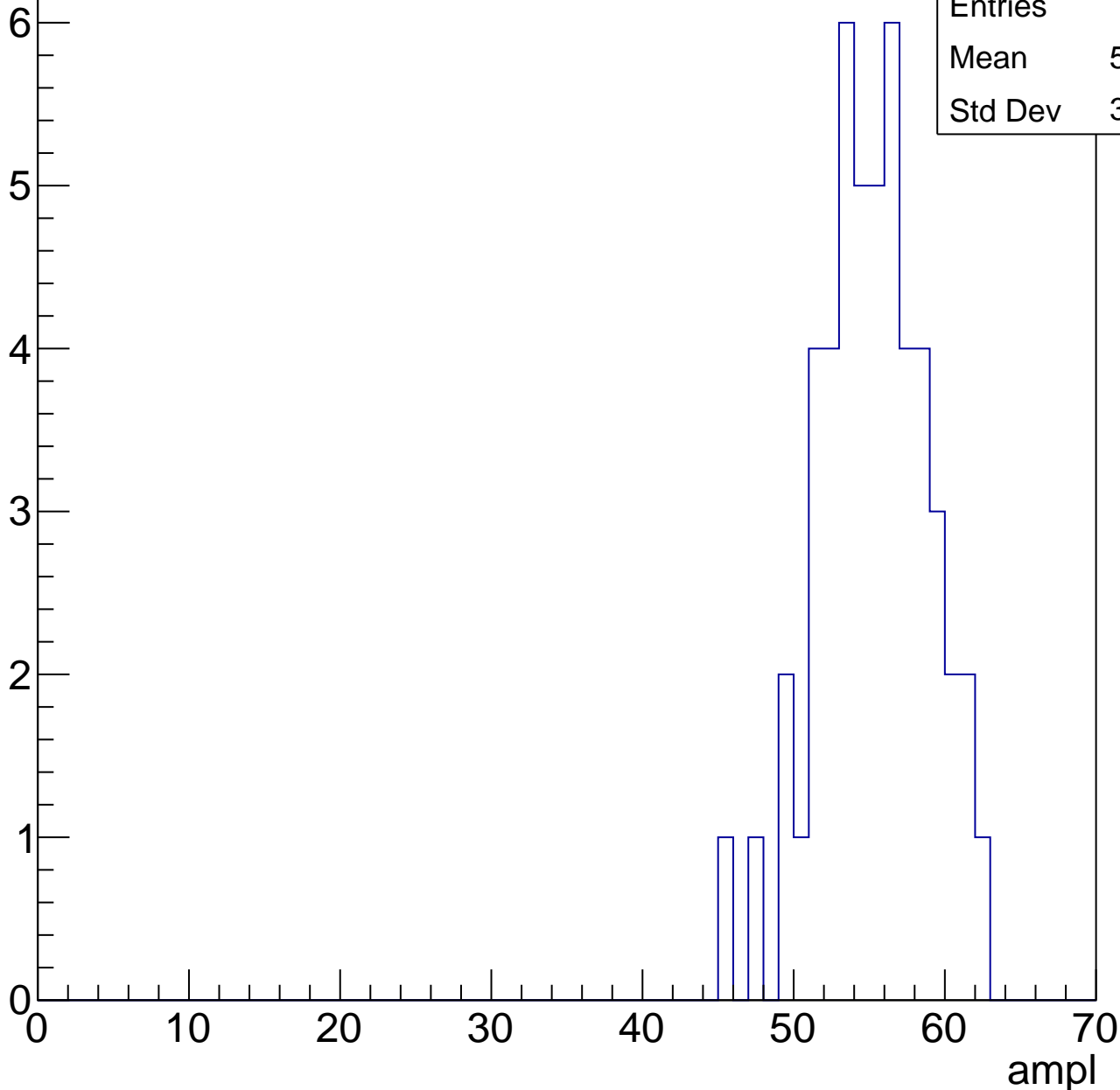


# B1L103S, U3-ch37, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

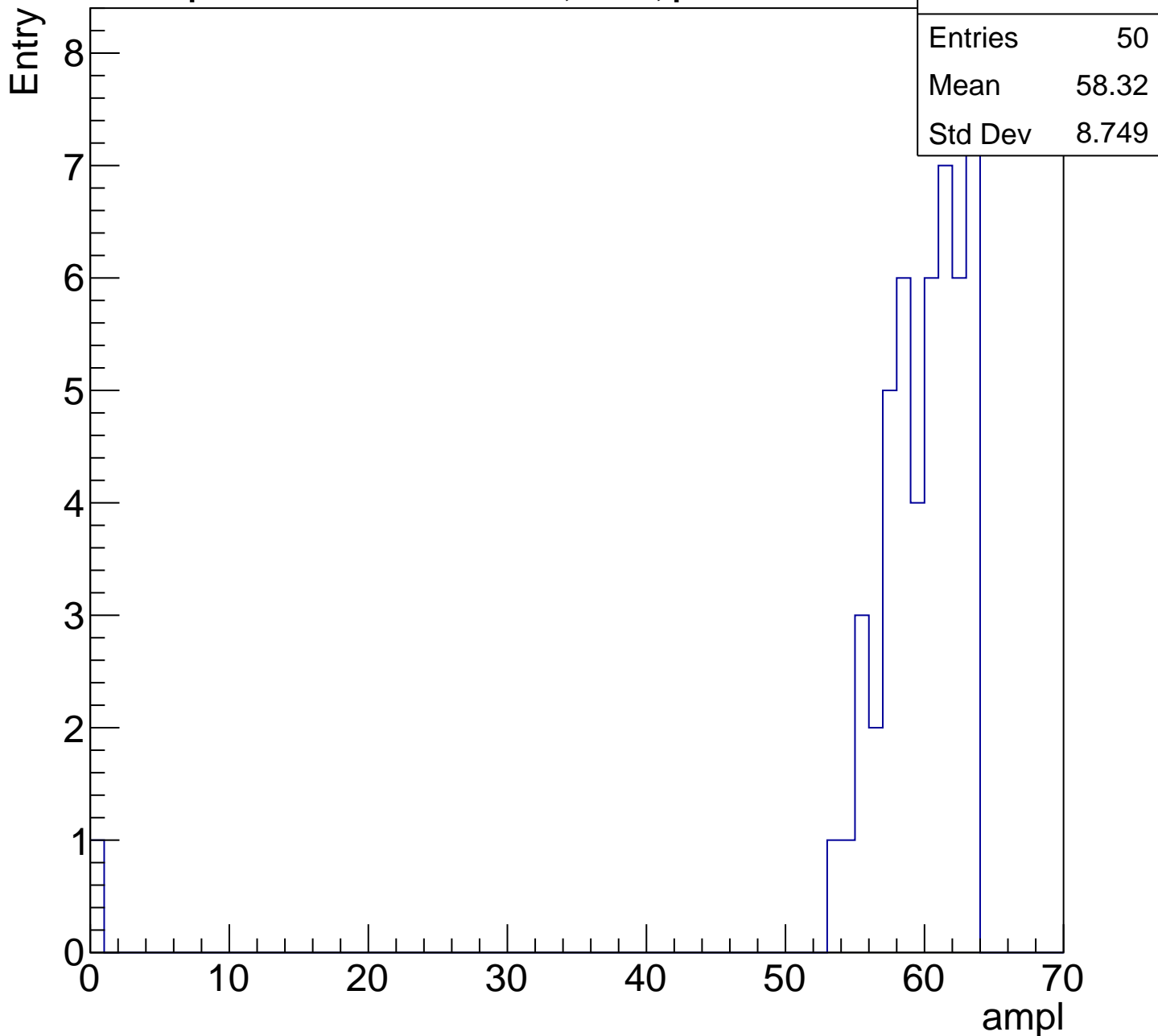
Entry

Entries	51
Mean	54.75
Std Dev	3.607



# B1L103S, U3-ch37, adc5

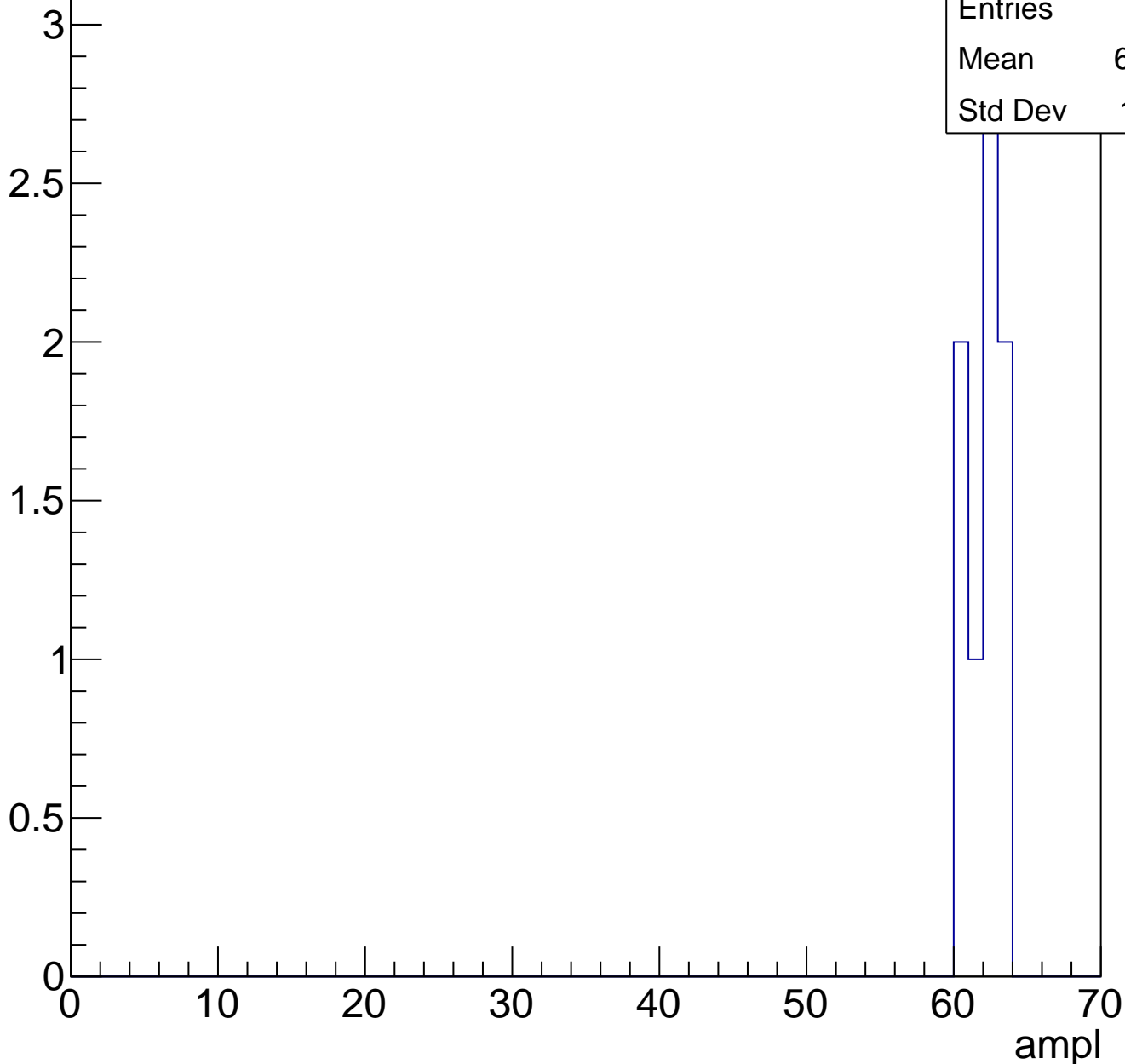
calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U3-ch37, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U3-ch37, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

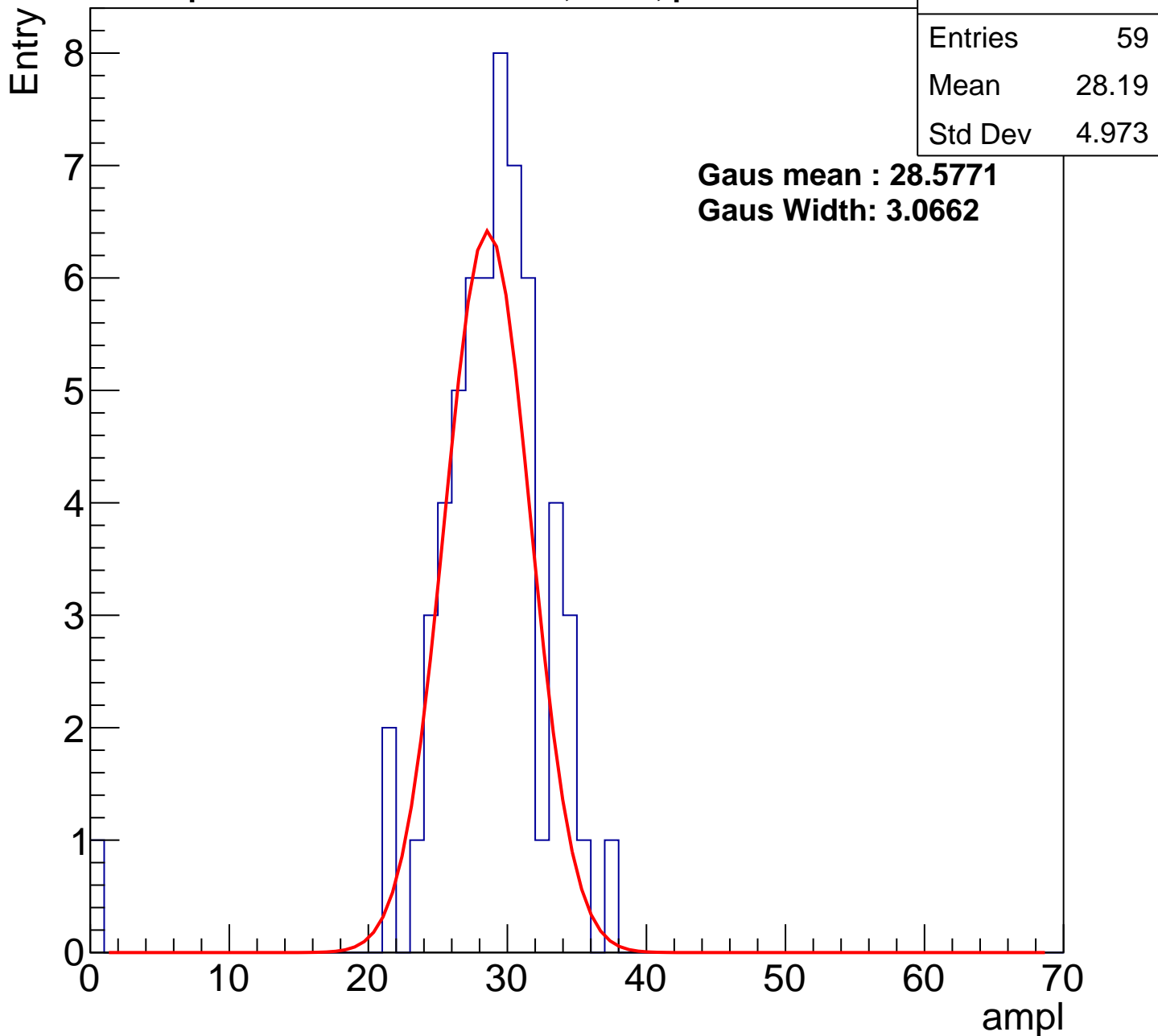
Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U3-ch38, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U3-ch38, adc1

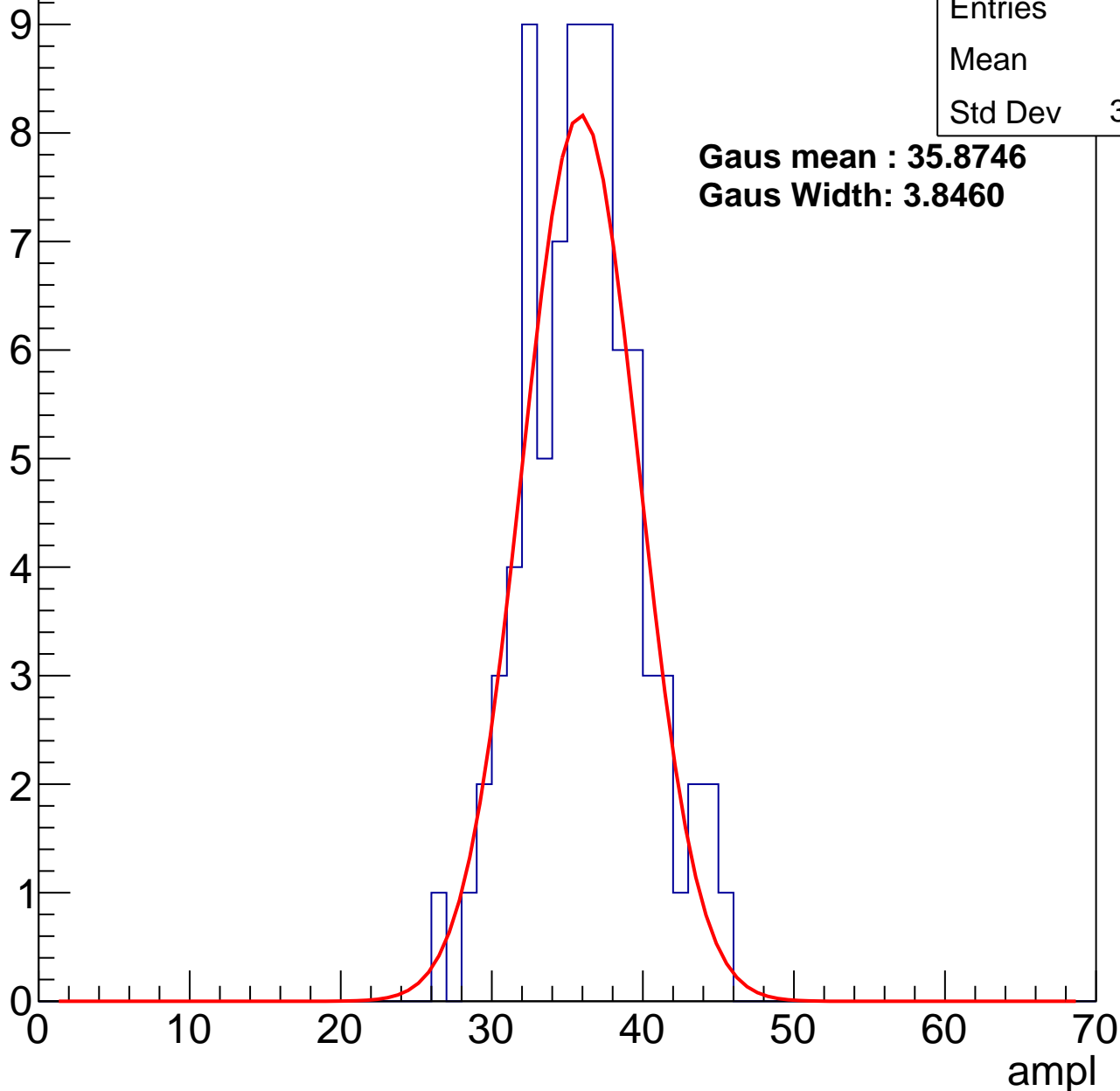
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	83
Mean	35.6
Std Dev	3.859

**Gaus mean : 35.8746**

**Gaus Width: 3.8460**



# B1L103S, U3-ch38, adc2

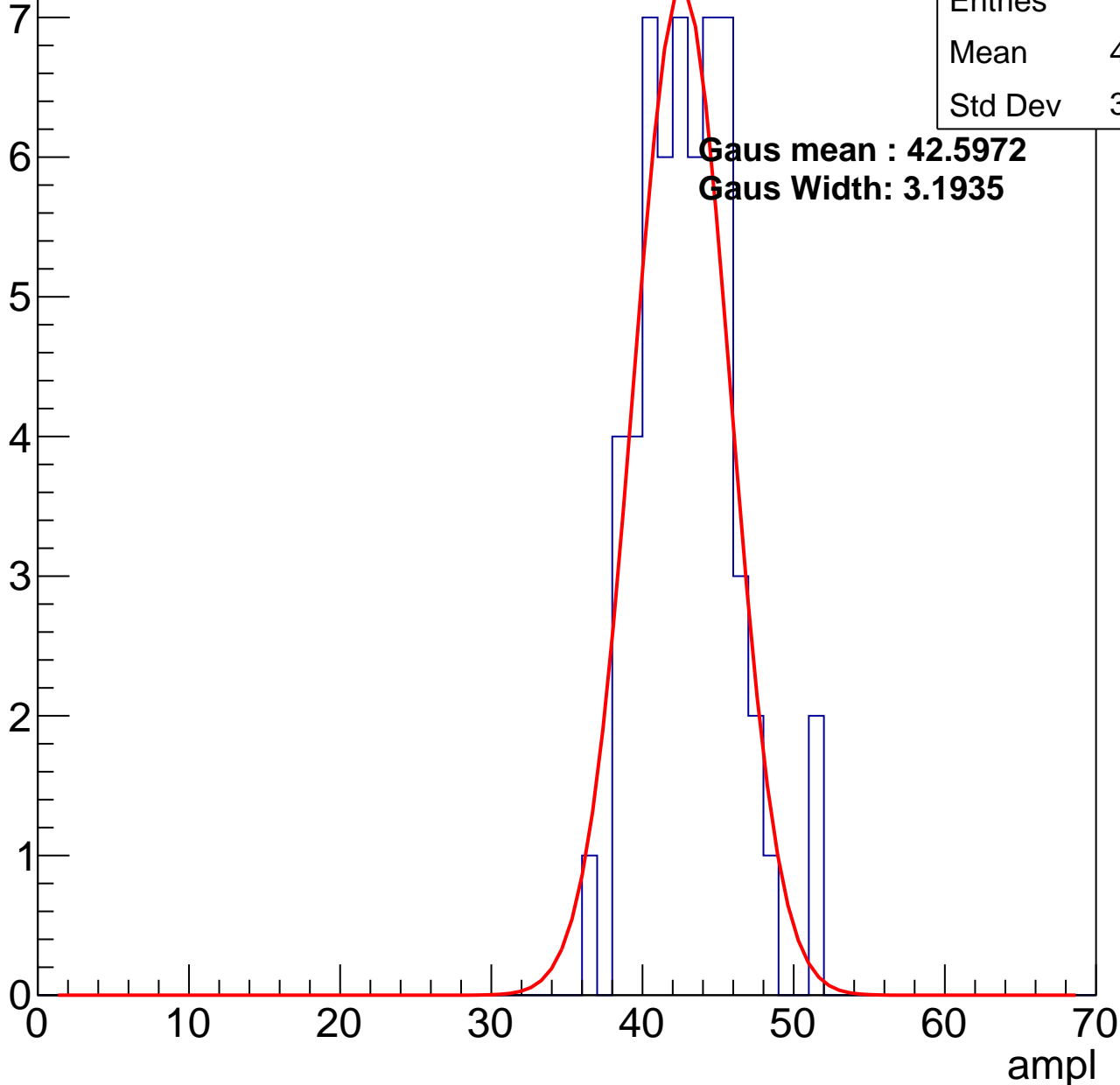
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	42.58
Std Dev	3.089

**Gaus mean : 42.5972**

**Gaus Width: 3.1935**

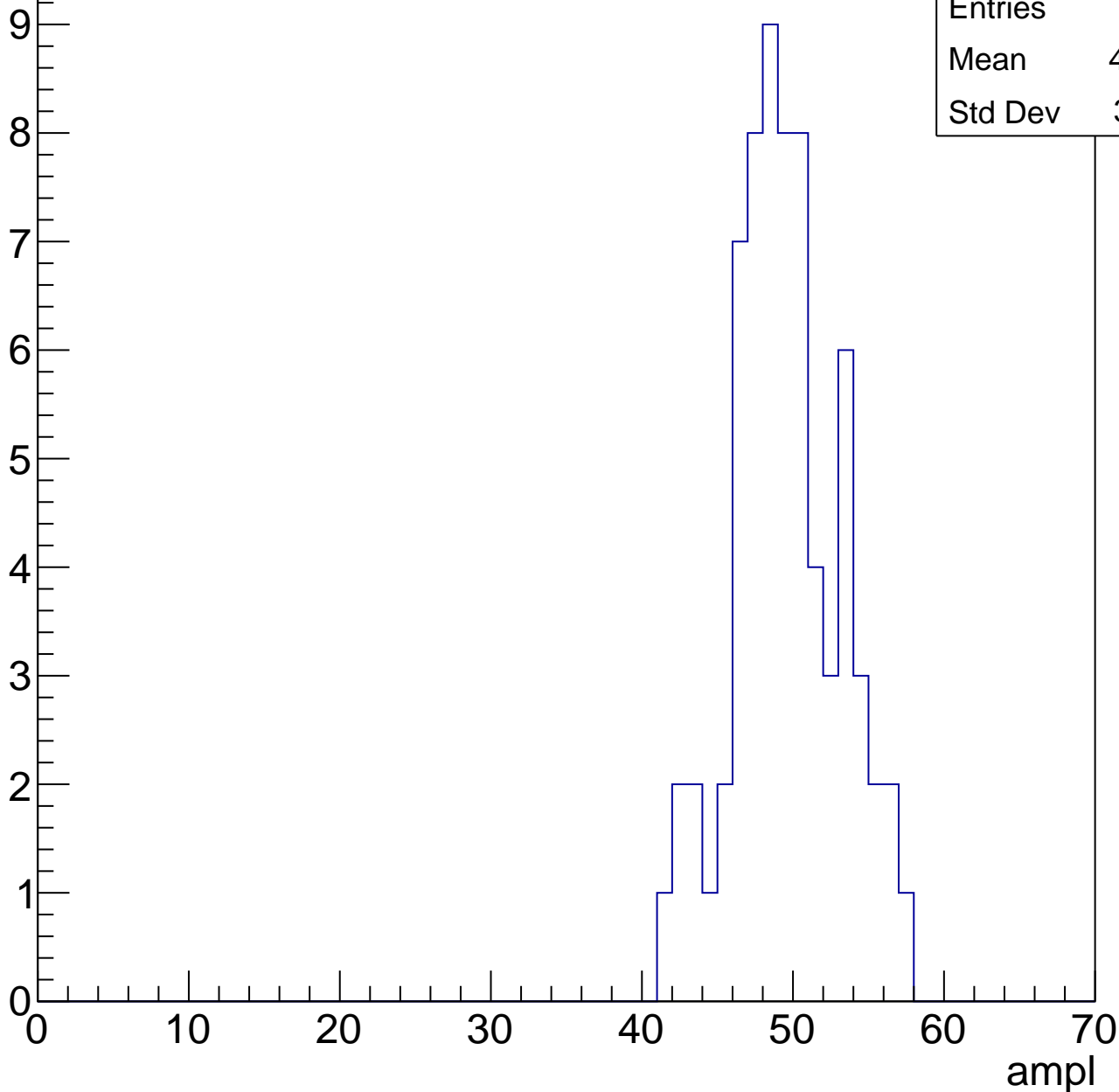


# B1L103S, U3-ch38, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	49.07
Std Dev	3.511

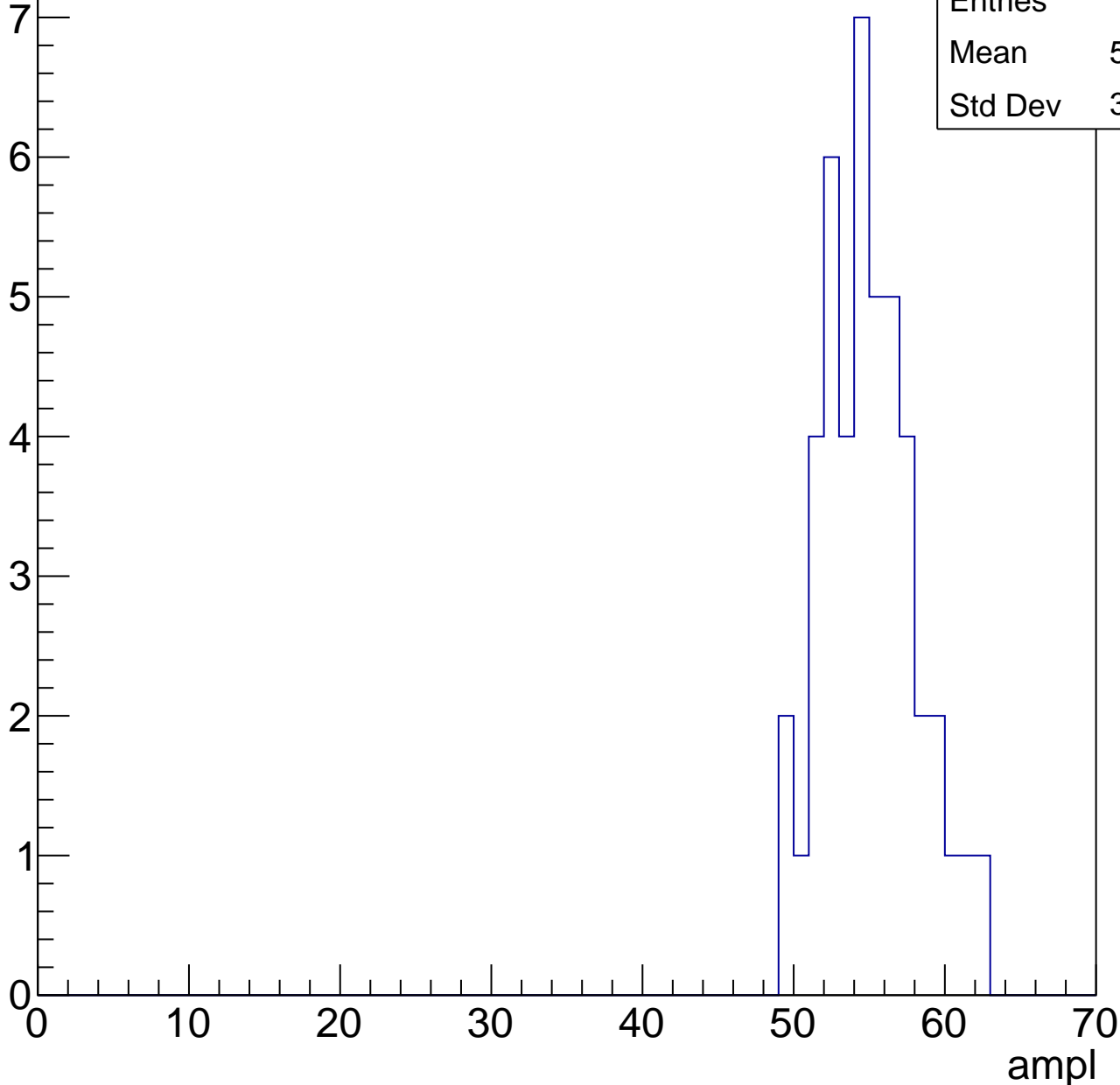


# B1L103S, U3-ch38, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	45
Mean	54.53
Std Dev	3.016

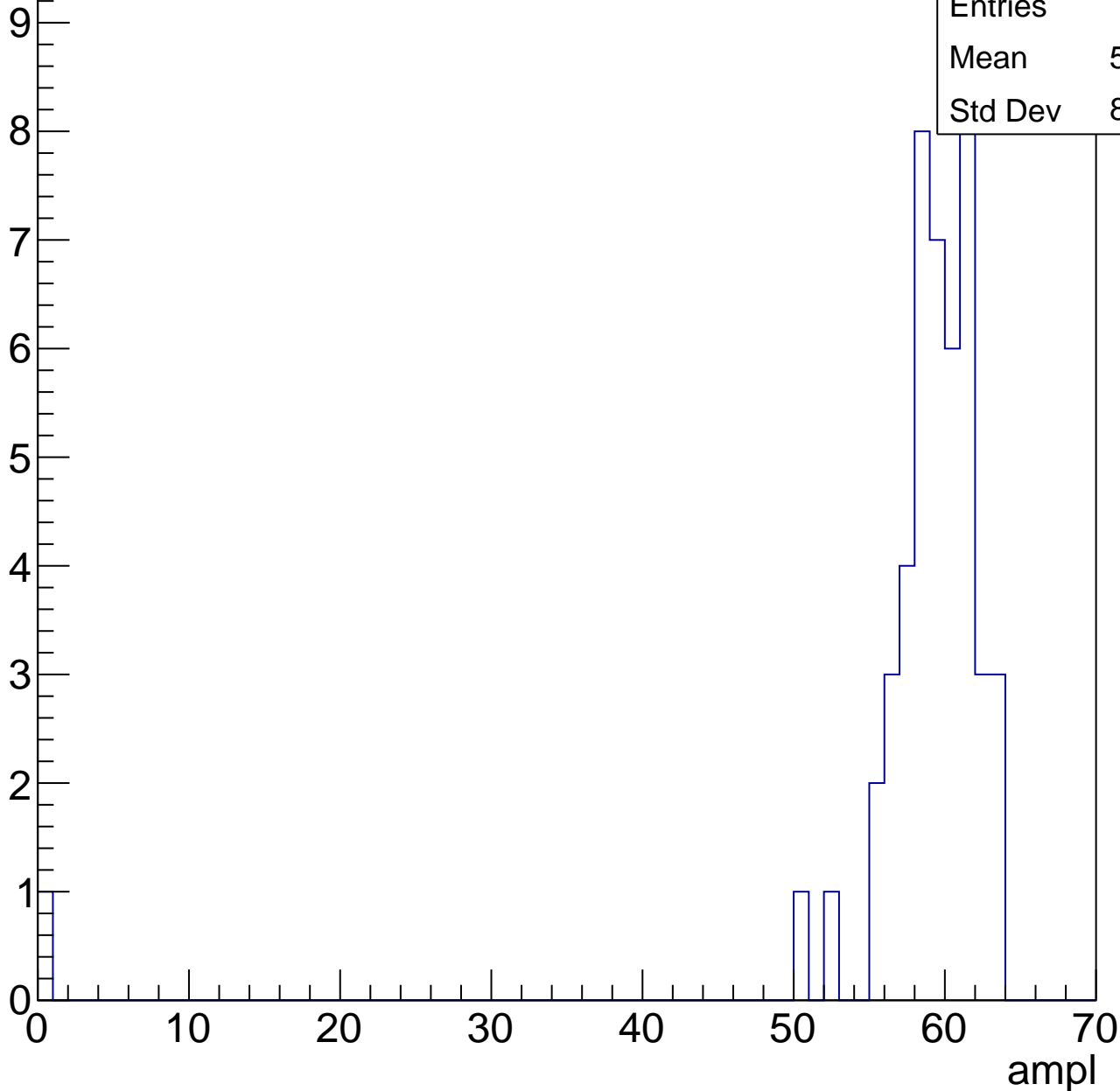


# B1L103S, U3-ch38, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	48
Mean	57.69
Std Dev	8.813

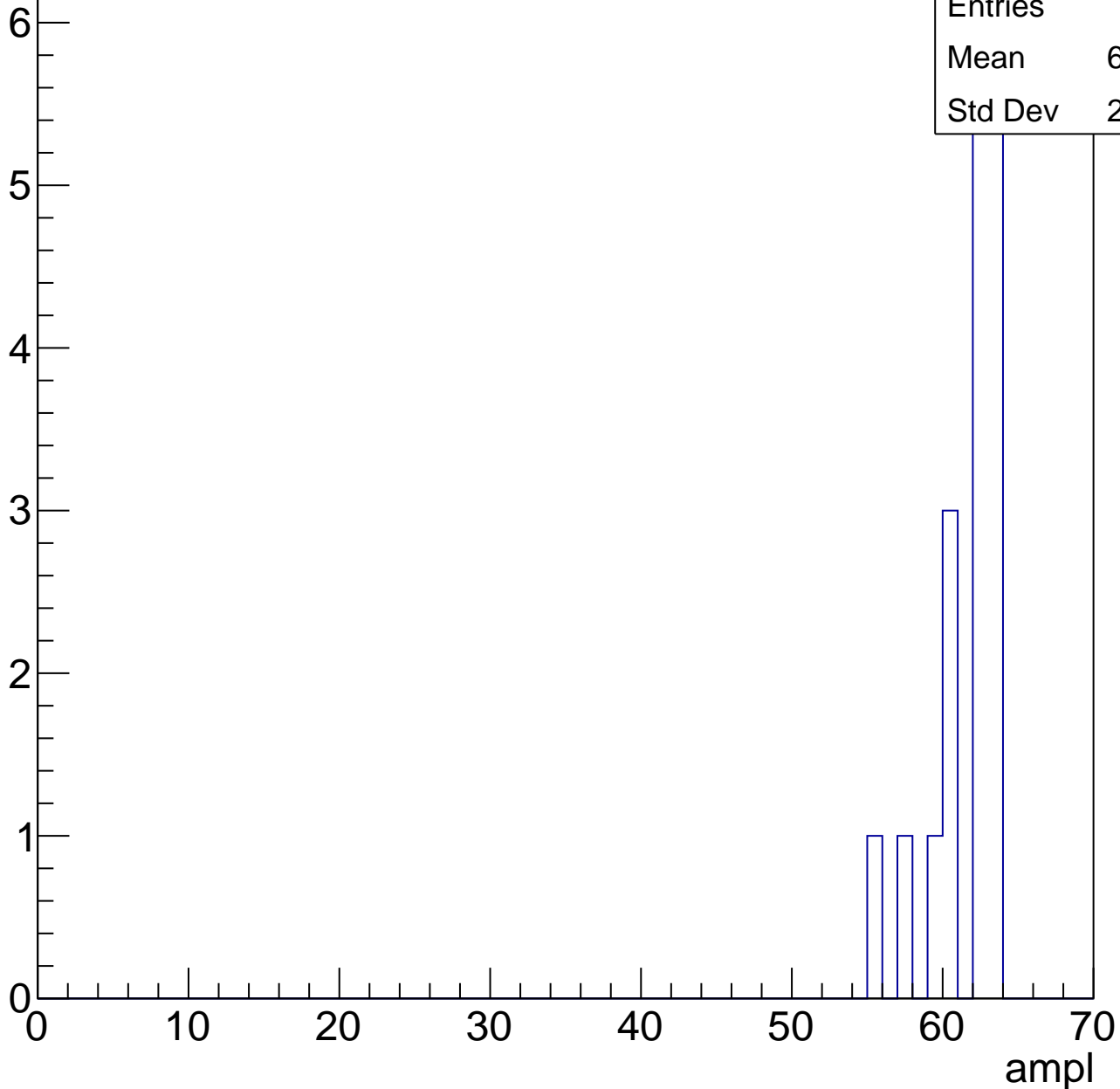


# B1L103S, U3-ch38, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	18
Mean	61.17
Std Dev	2.217





# B1L103S, U3-ch38, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch39, adc0

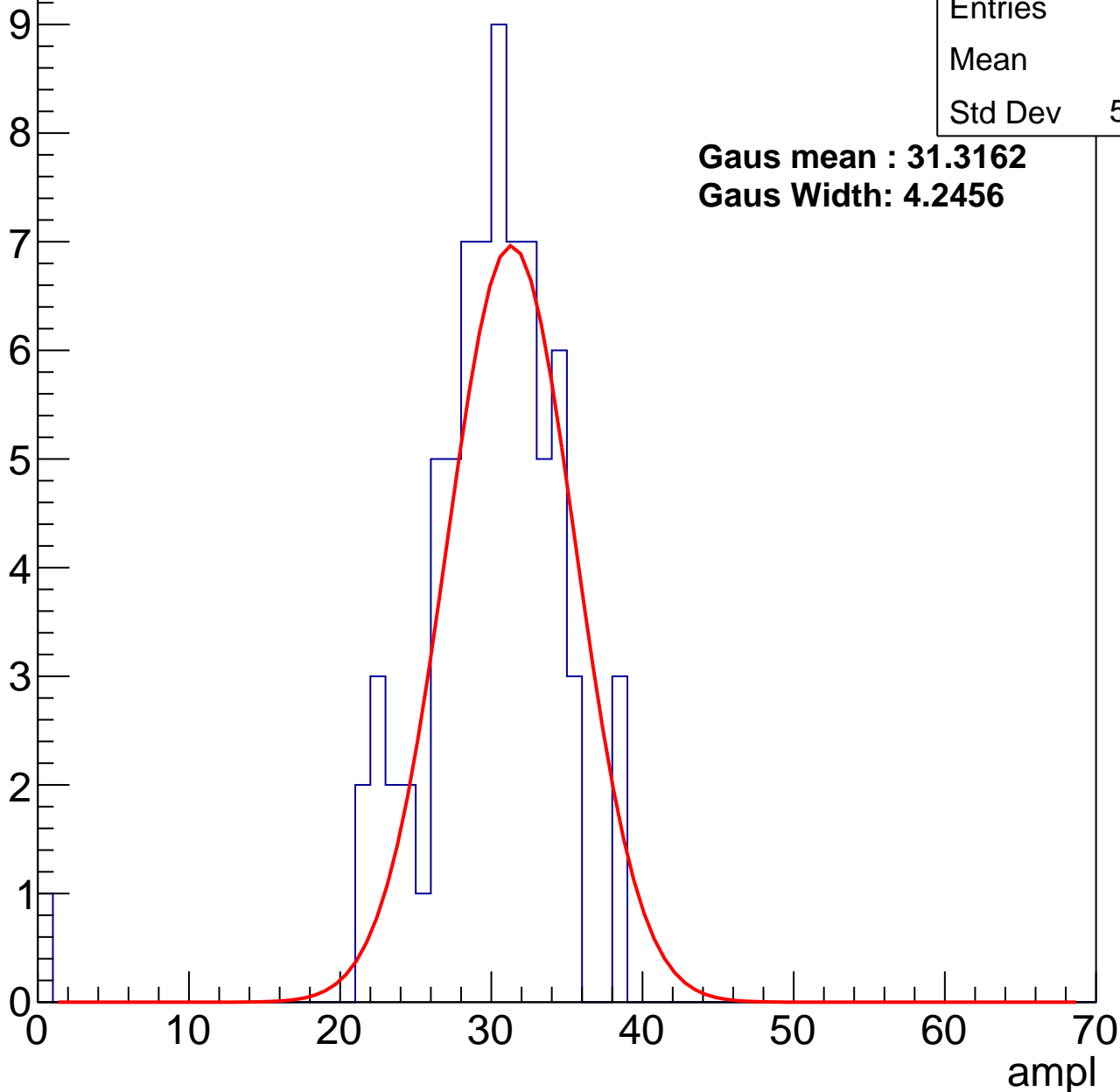
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	29.2
Std Dev	5.169

**Gaus mean : 31.3162**

**Gaus Width: 4.2456**



# B1L103S, U3-ch39, adc1

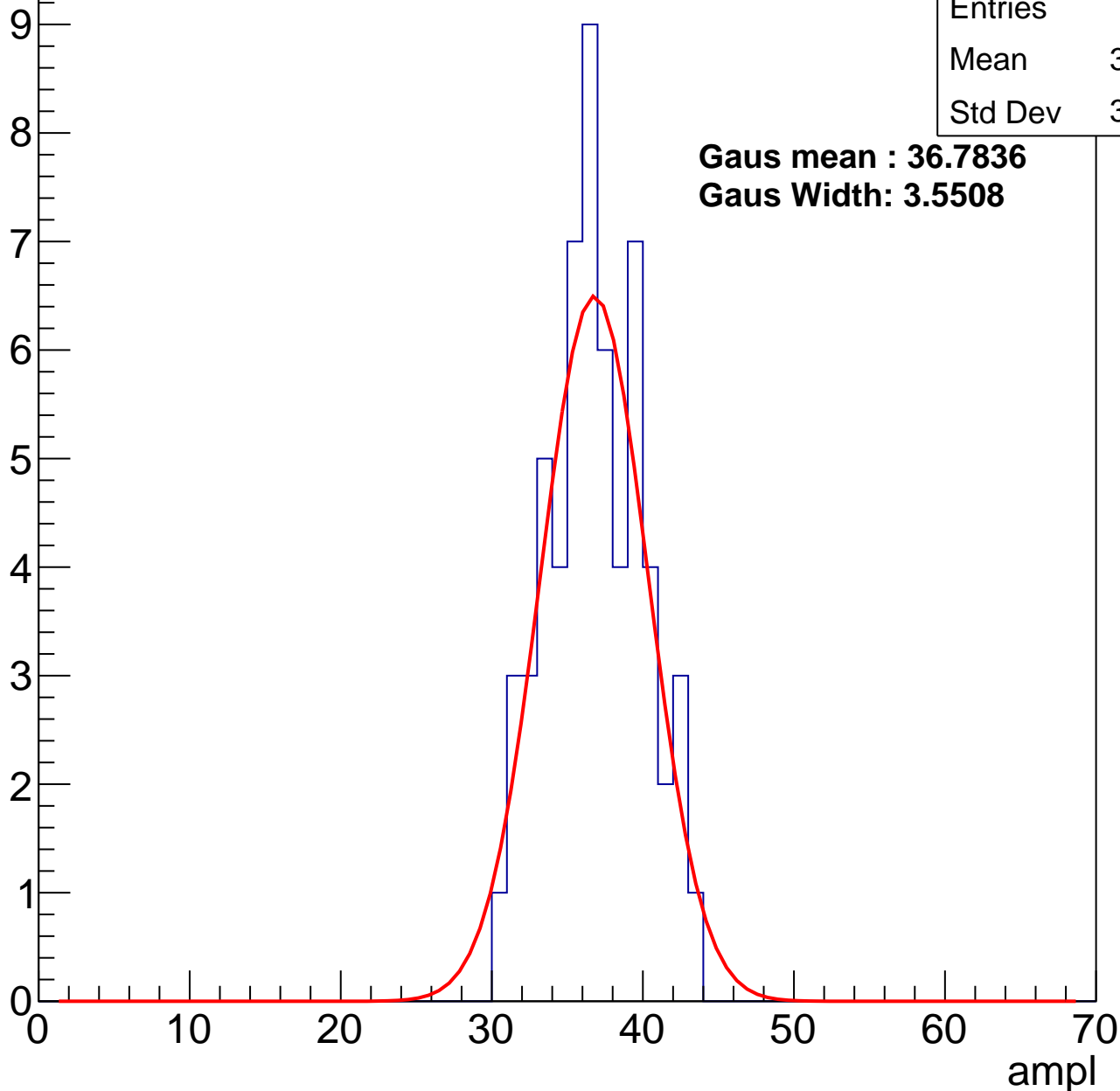
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	36.39
Std Dev	3.119

**Gaus mean : 36.7836**

**Gaus Width: 3.5508**



# B1L103S, U3-ch39, adc2

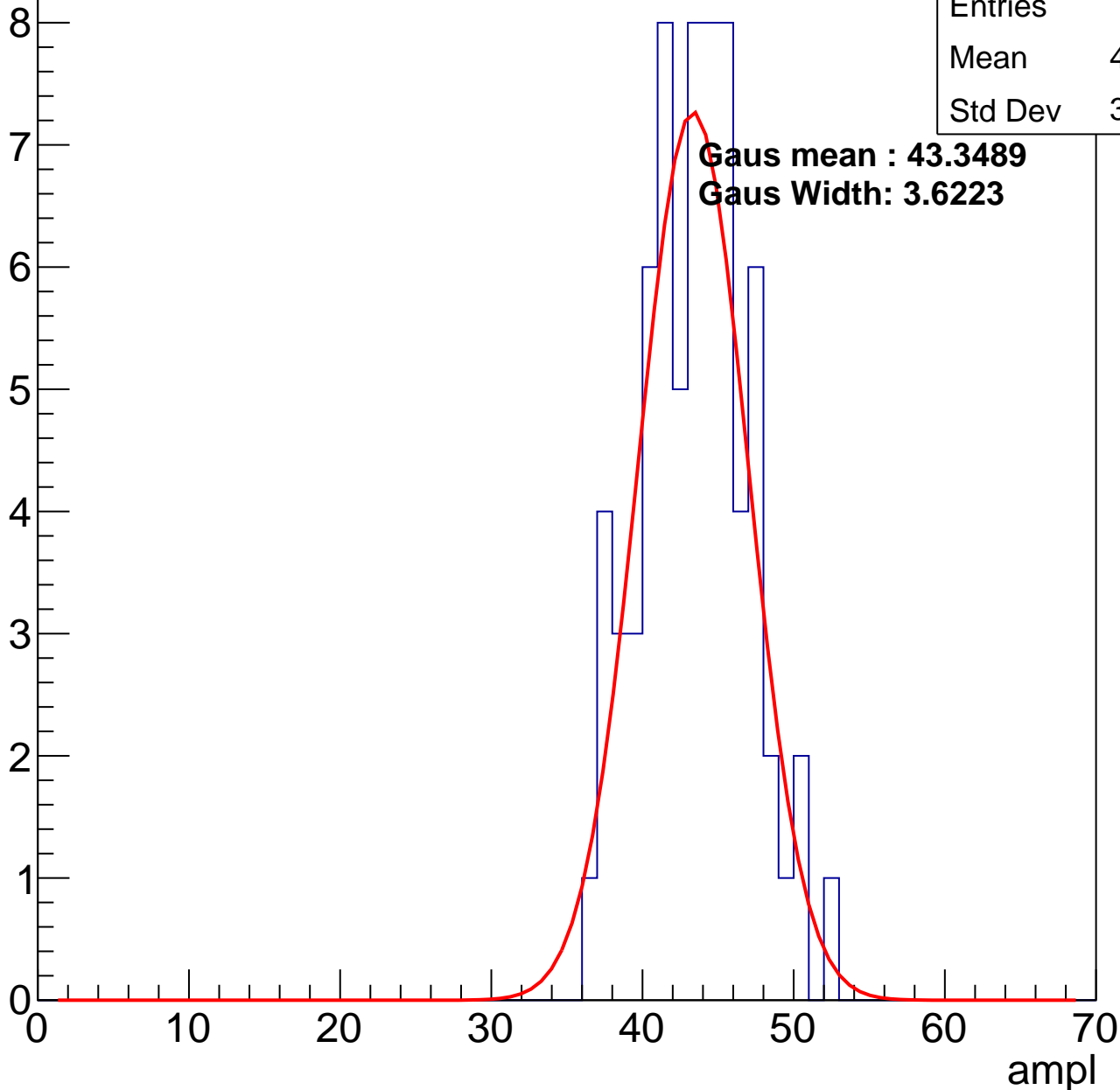
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	43.03
Std Dev	3.472

**Gaus mean : 43.3489**

**Gaus Width: 3.6223**

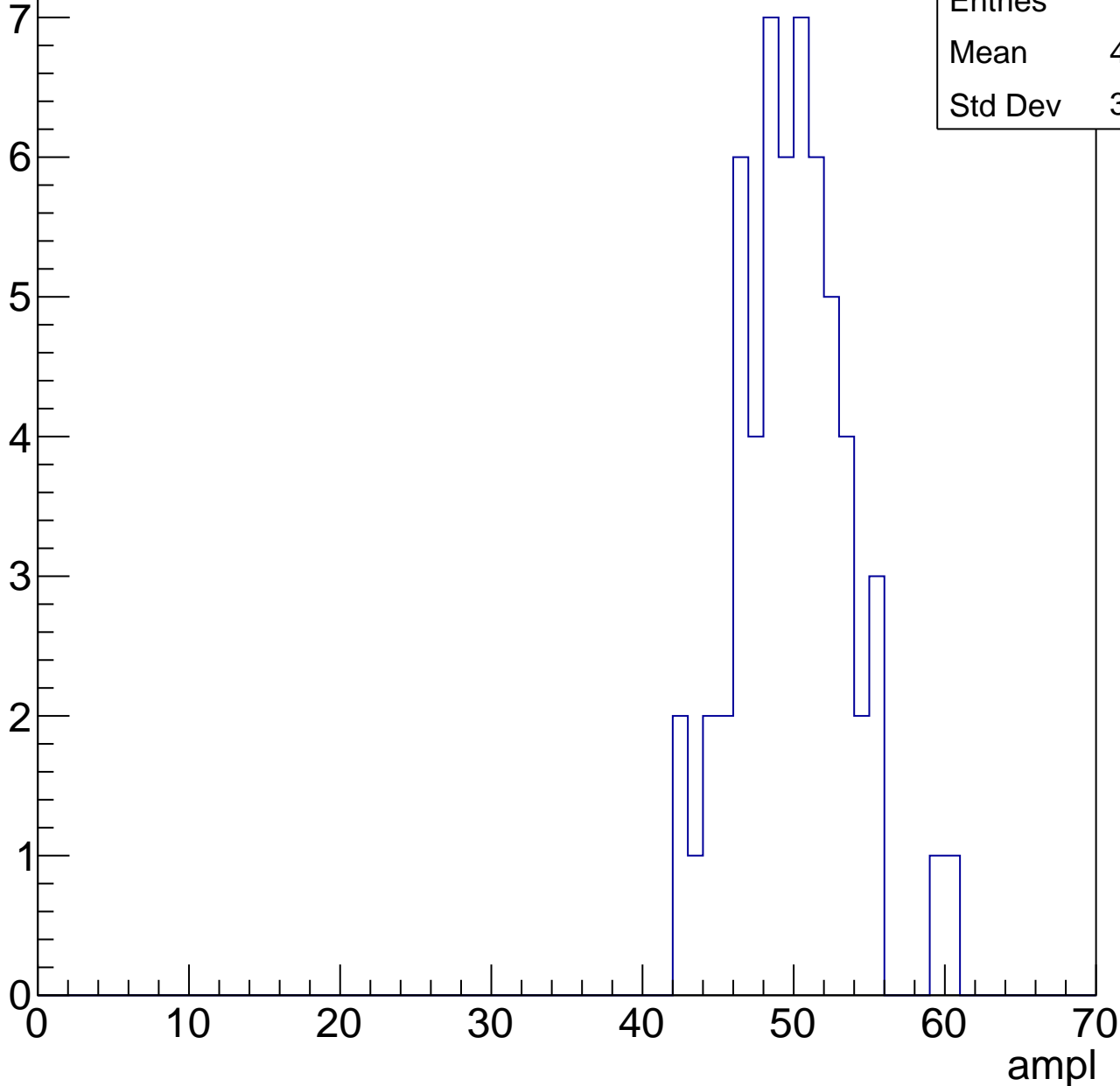


# B1L103S, U3-ch39, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	49.47
Std Dev	3.679

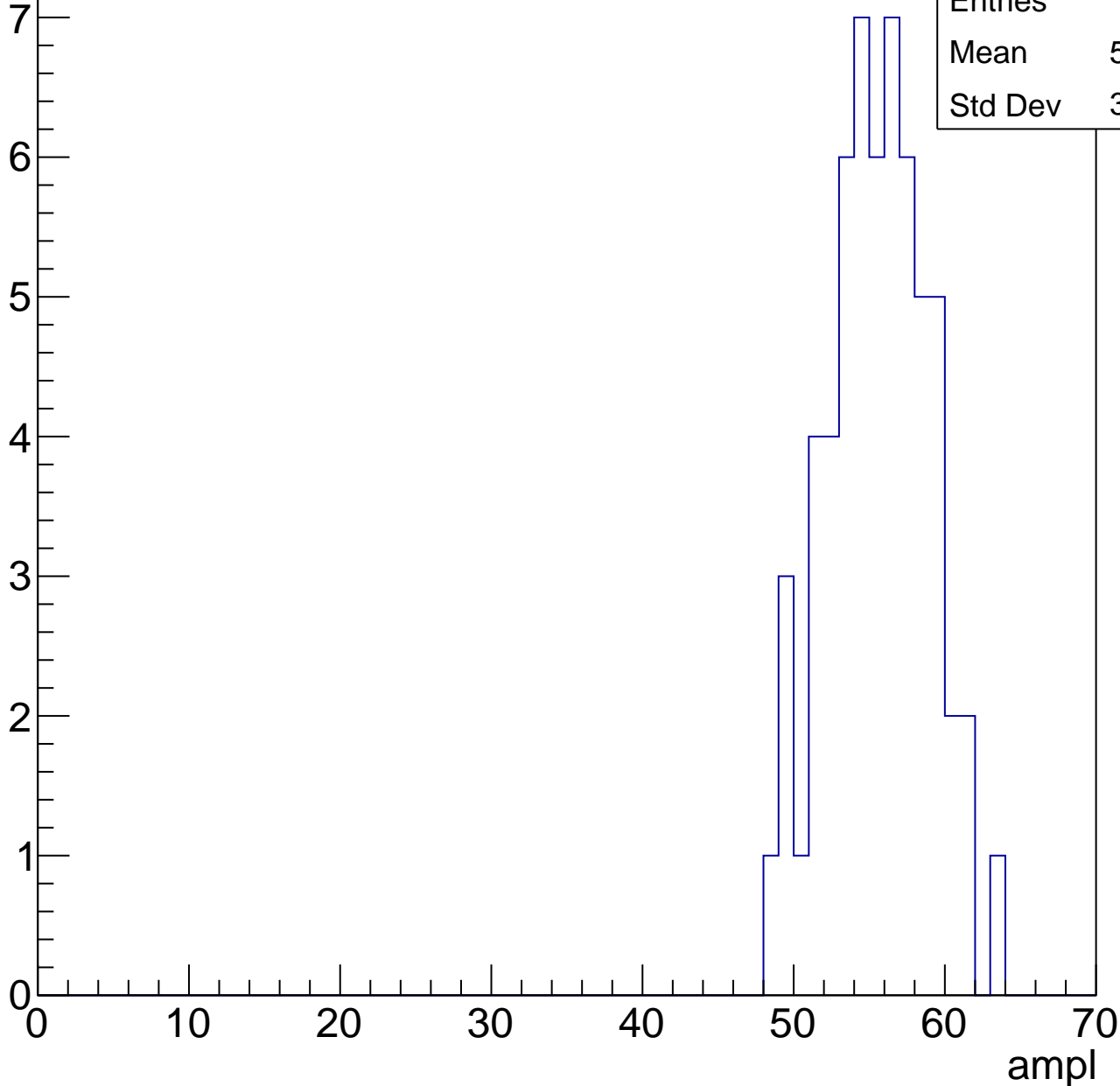


# B1L103S, U3-ch39, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	55.12
Std Dev	3.302



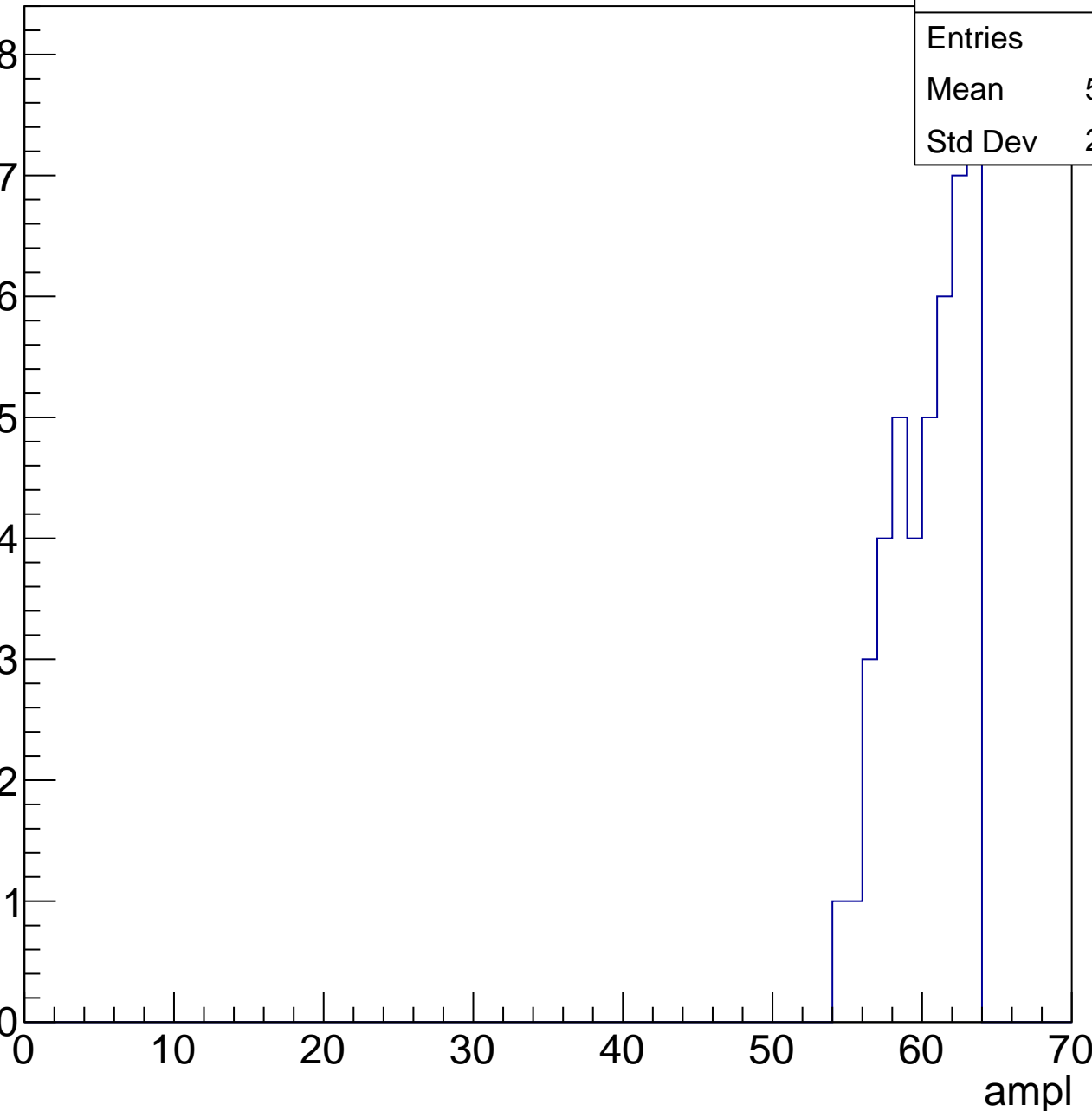
# B1L103S, U3-ch39, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	44
Mean	59.89
Std Dev	2.497

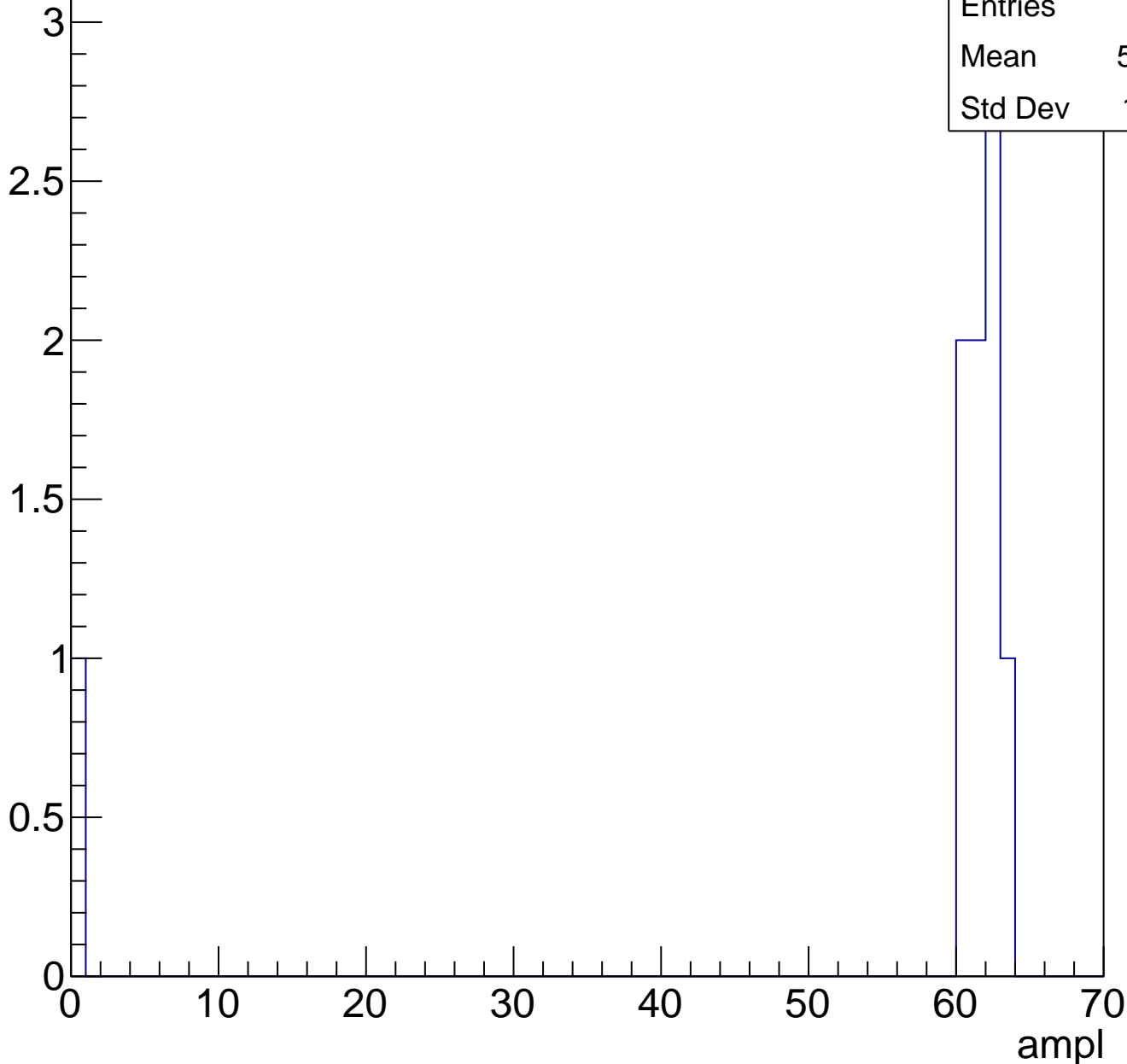
8  
7  
6  
5  
4  
3  
2  
1  
0



# B1L103S, U3-ch39, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U3-ch39, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U3-ch40, adc0

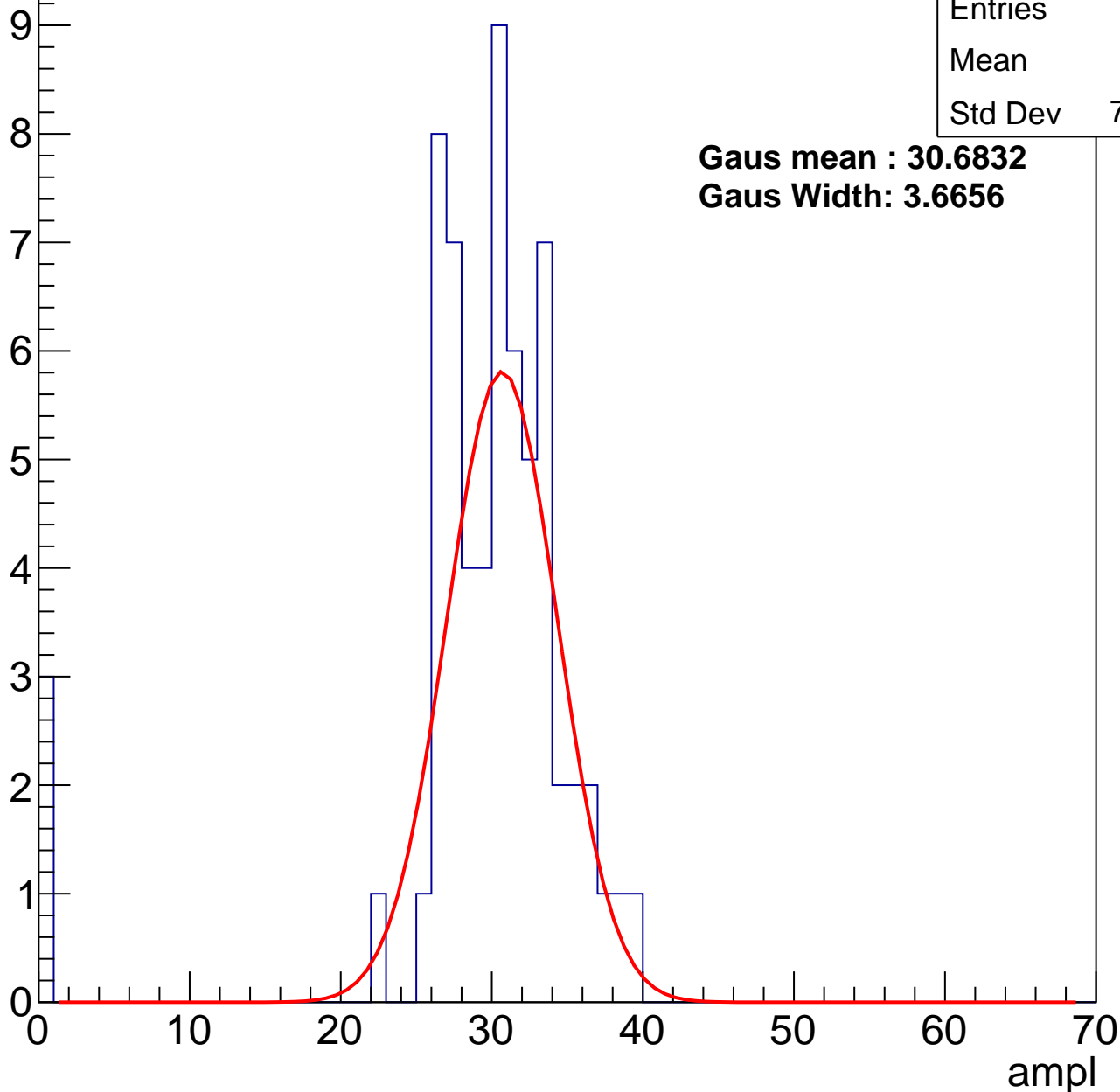
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	28.8
Std Dev	7.229

**Gaus mean : 30.6832**

**Gaus Width: 3.6656**



# B1L103S, U3-ch40, adc1

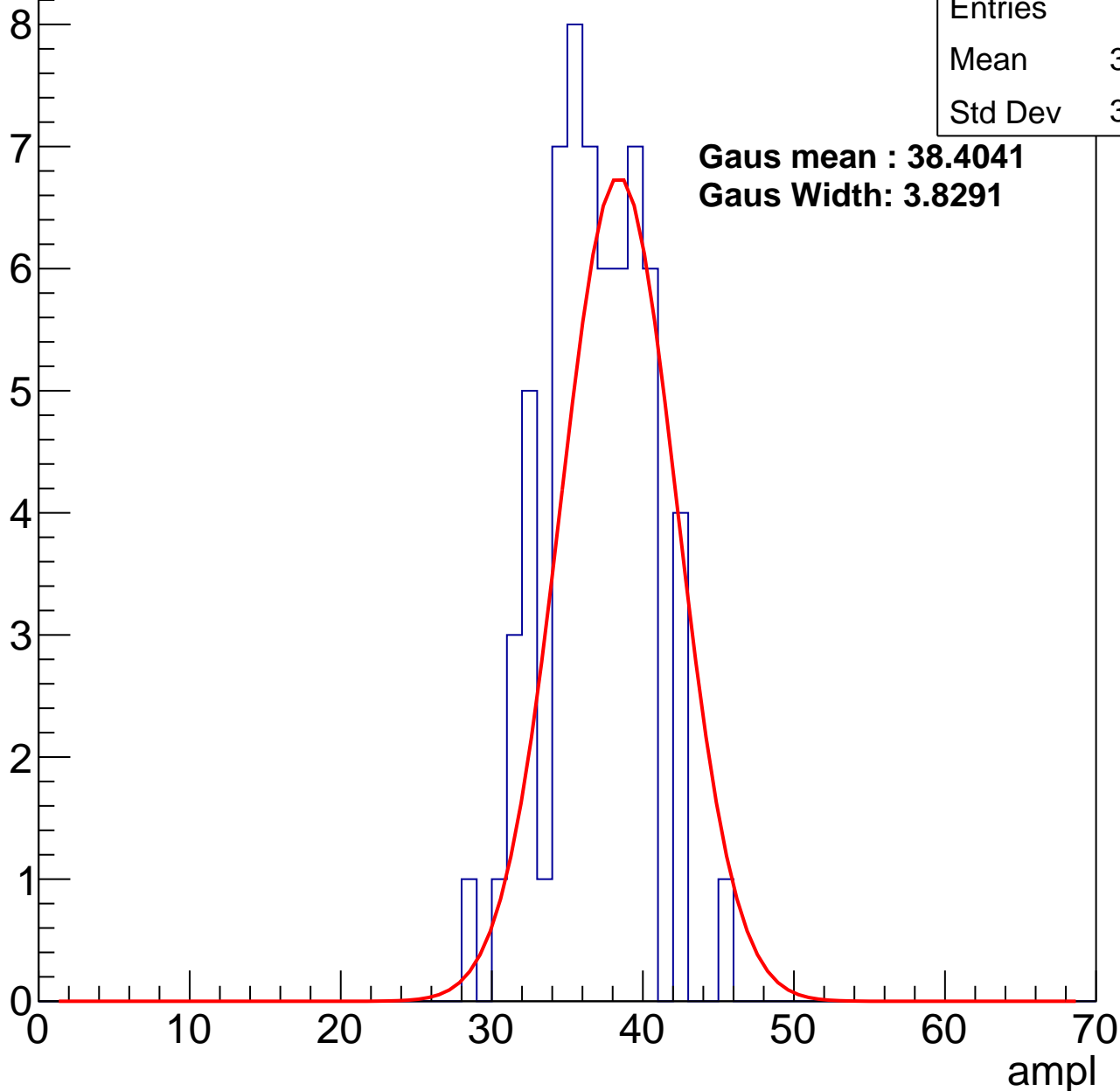
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	36.35
Std Dev	3.348

**Gaus mean : 38.4041**

**Gaus Width: 3.8291**



# B1L103S, U3-ch40, adc2

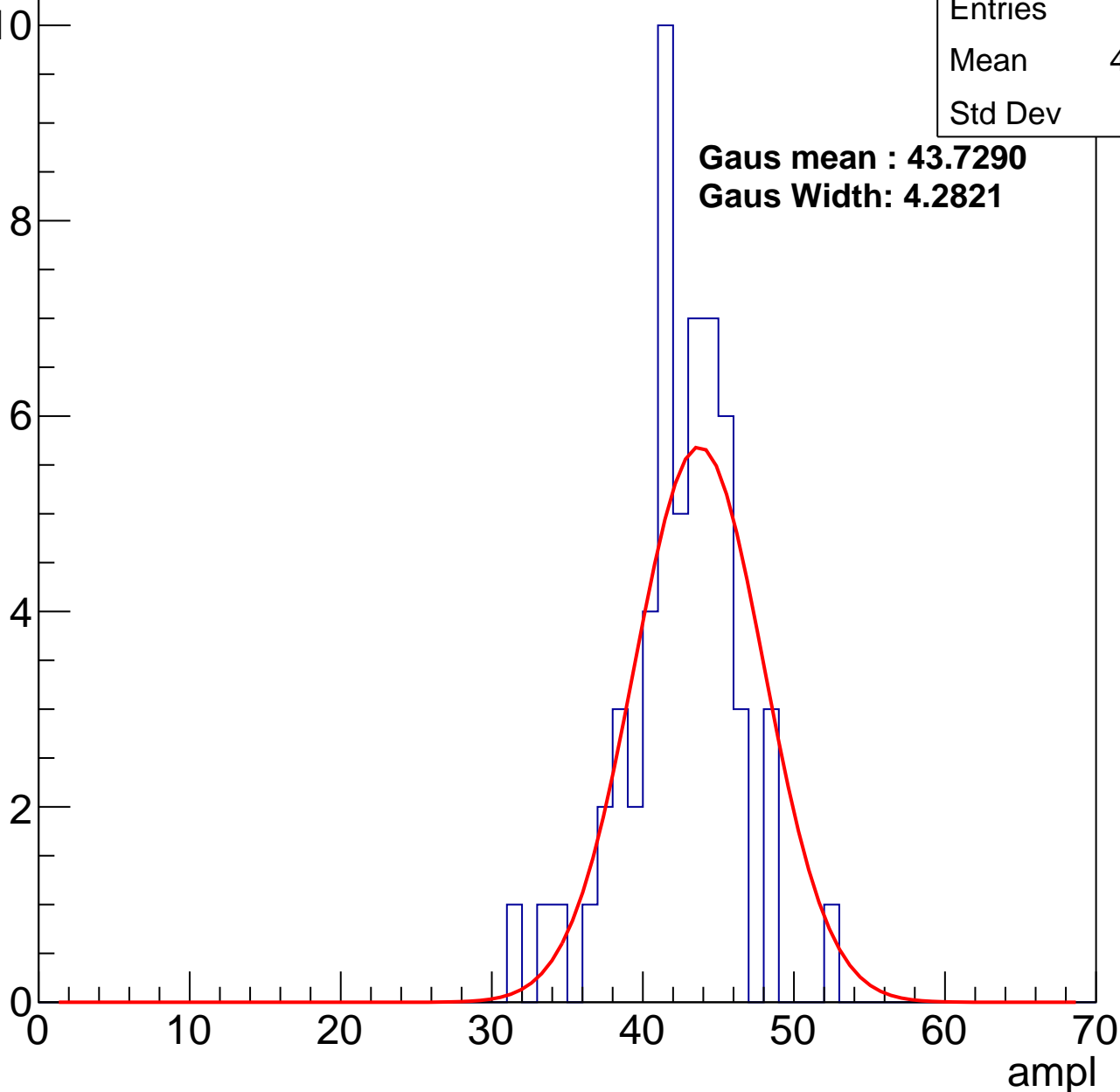
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	41.98
Std Dev	3.72

**Gaus mean : 43.7290**

**Gaus Width: 4.2821**



# B1L103S, U3-ch40, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	70
Mean	48.53
Std Dev	3.32

Entry

10

8

6

4

2

0

0

10

20

30

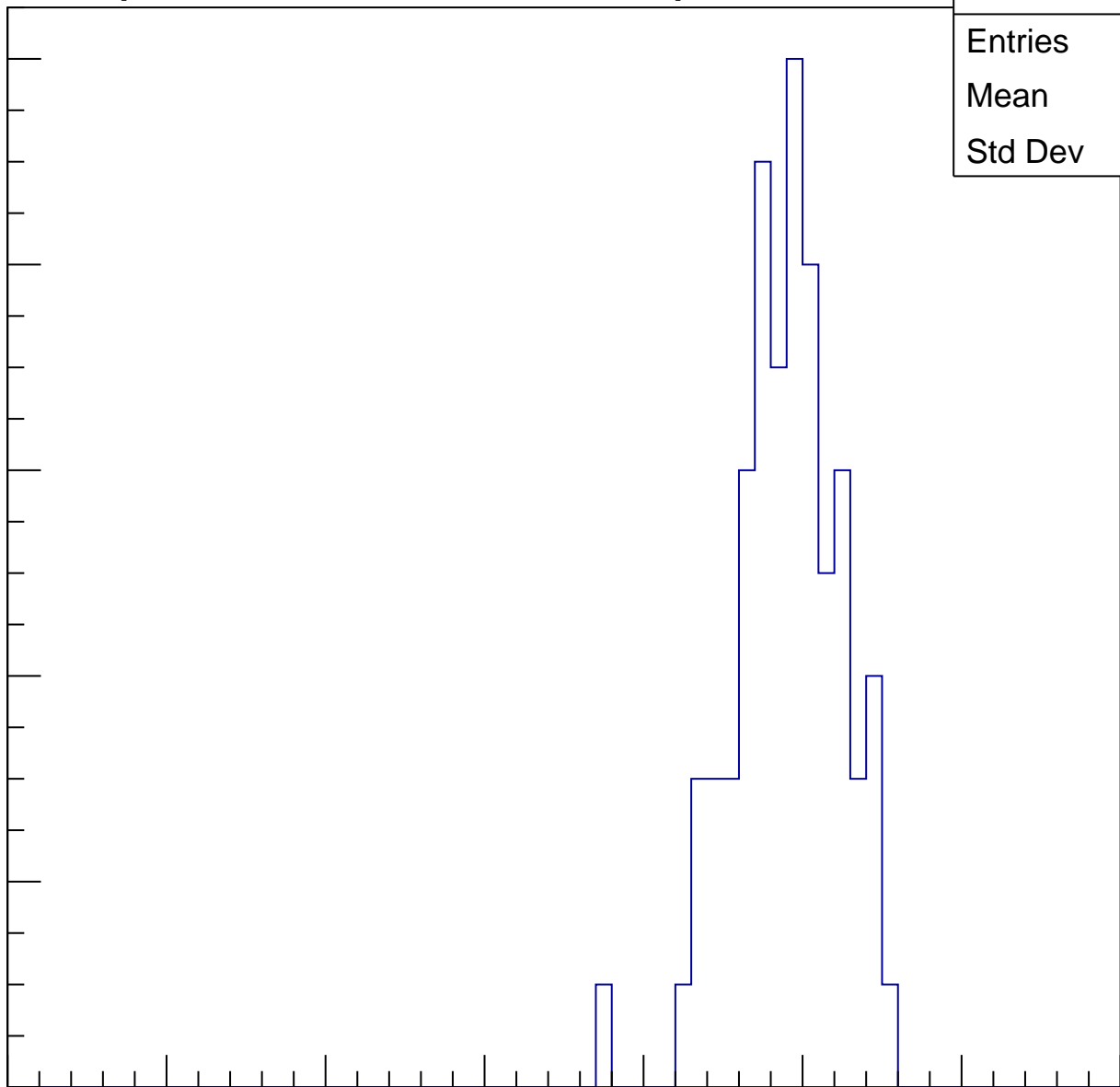
40

50

60

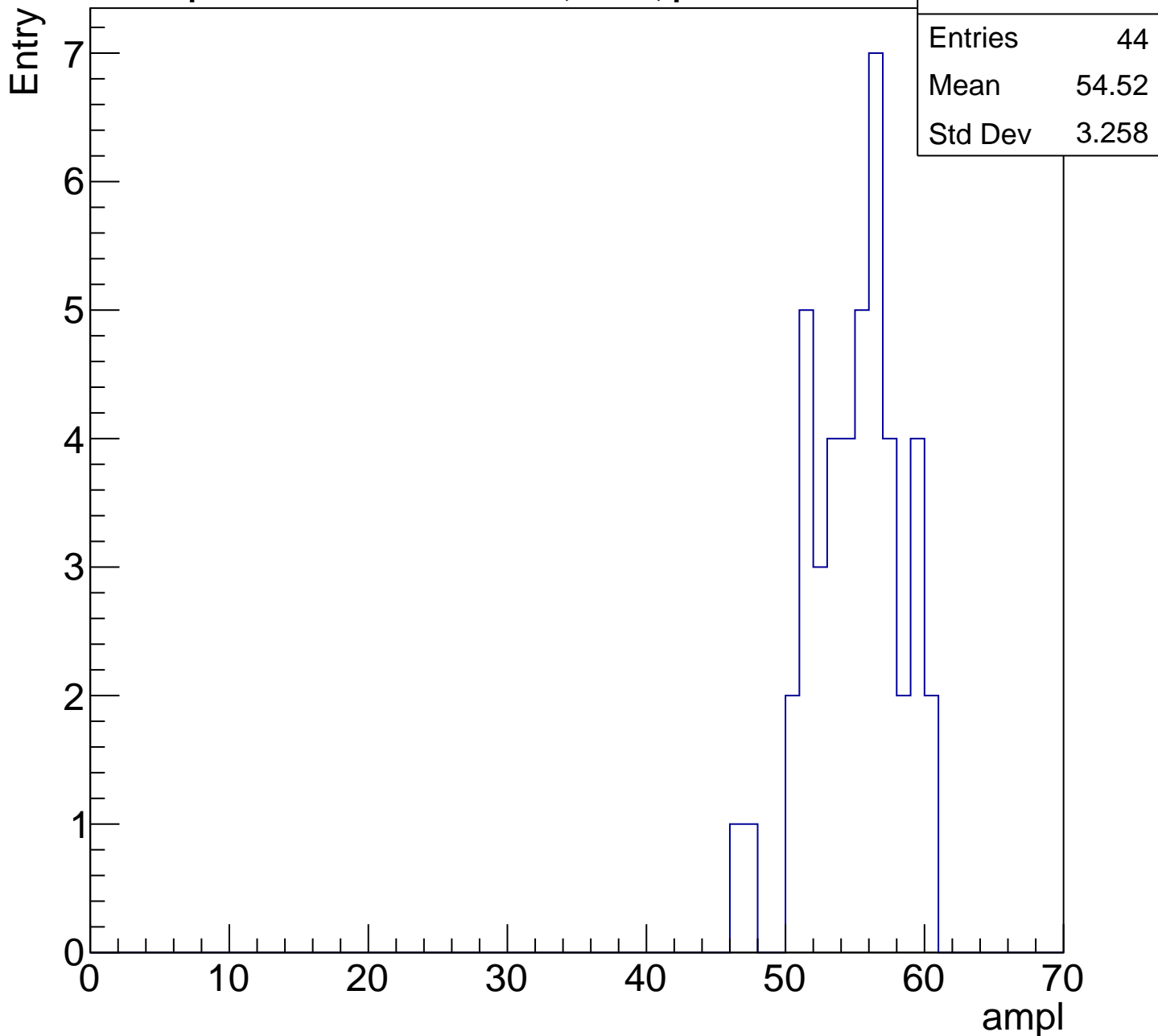
70

ampl



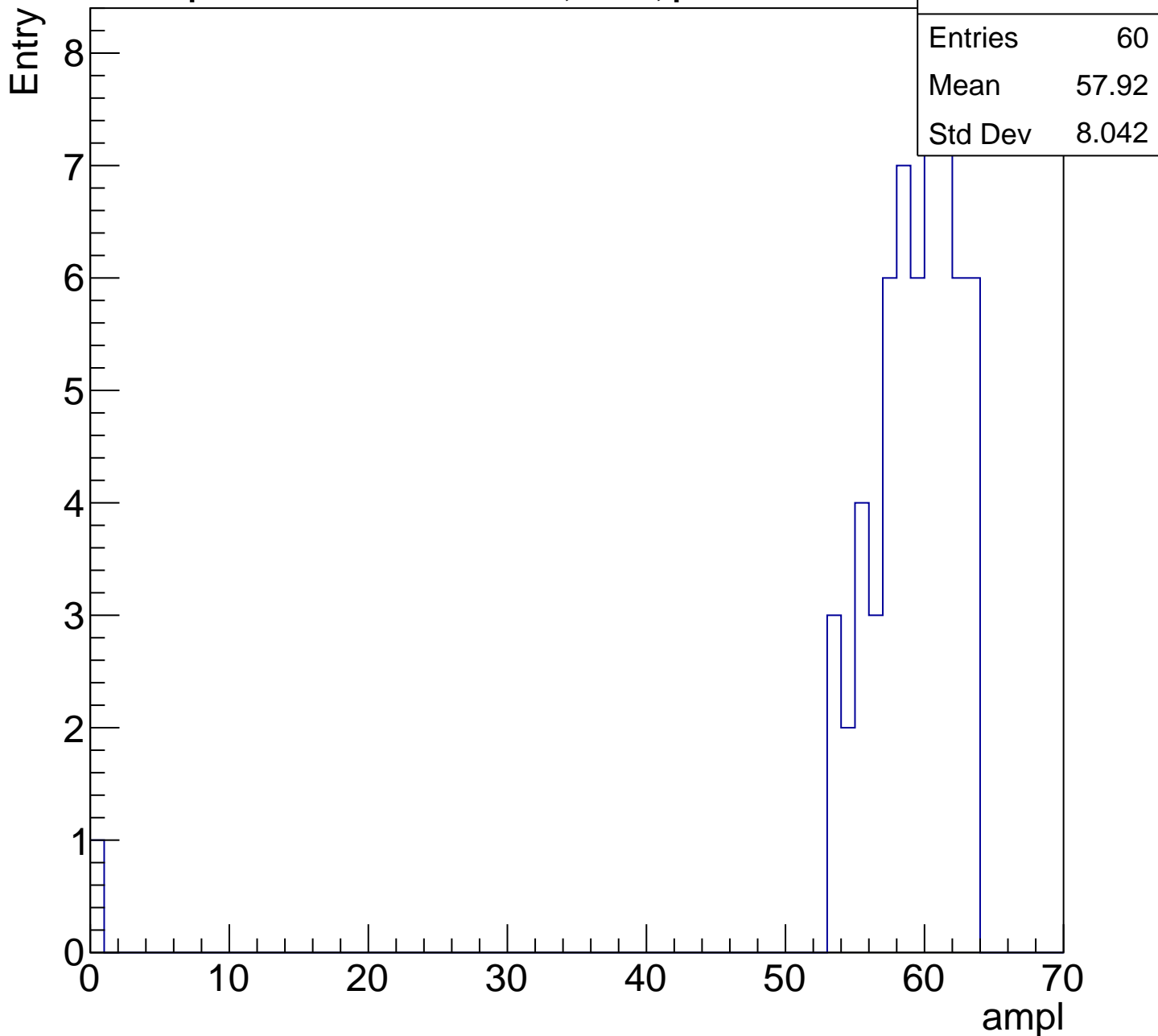
# B1L103S, U3-ch40, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U3-ch40, adc5

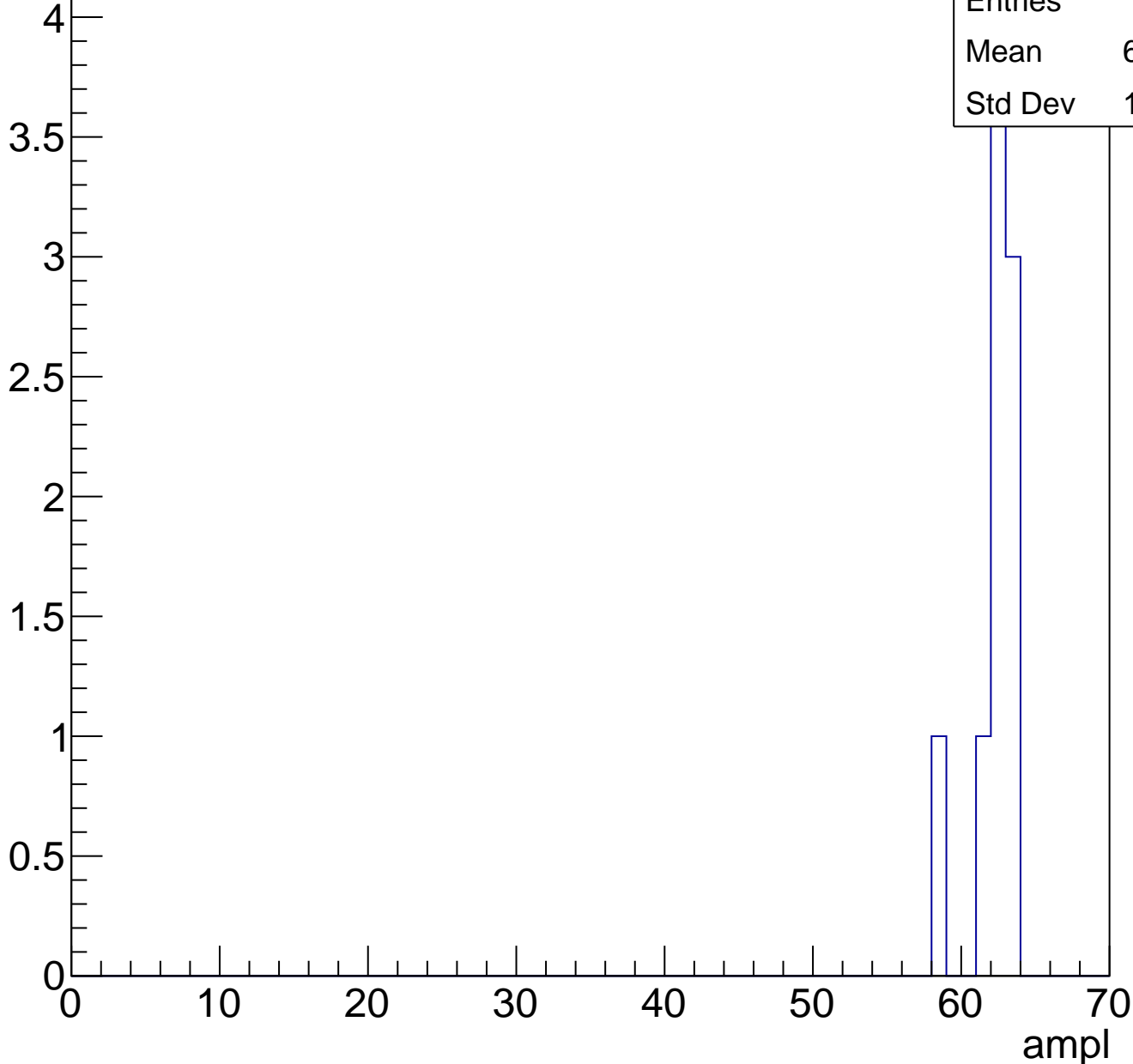
calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U3-ch40, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

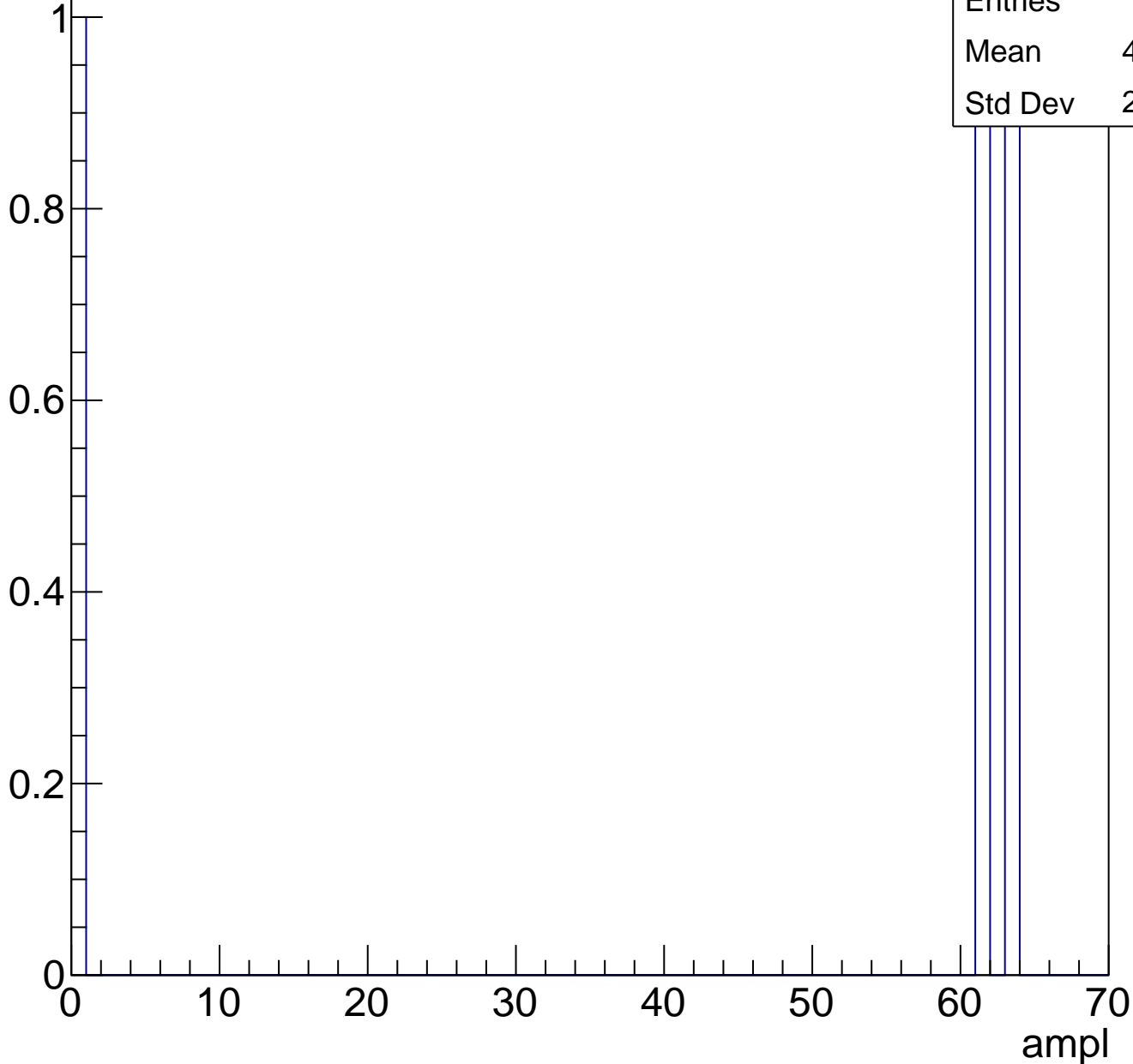




# B1L103S, U3-ch40, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch41, adc0

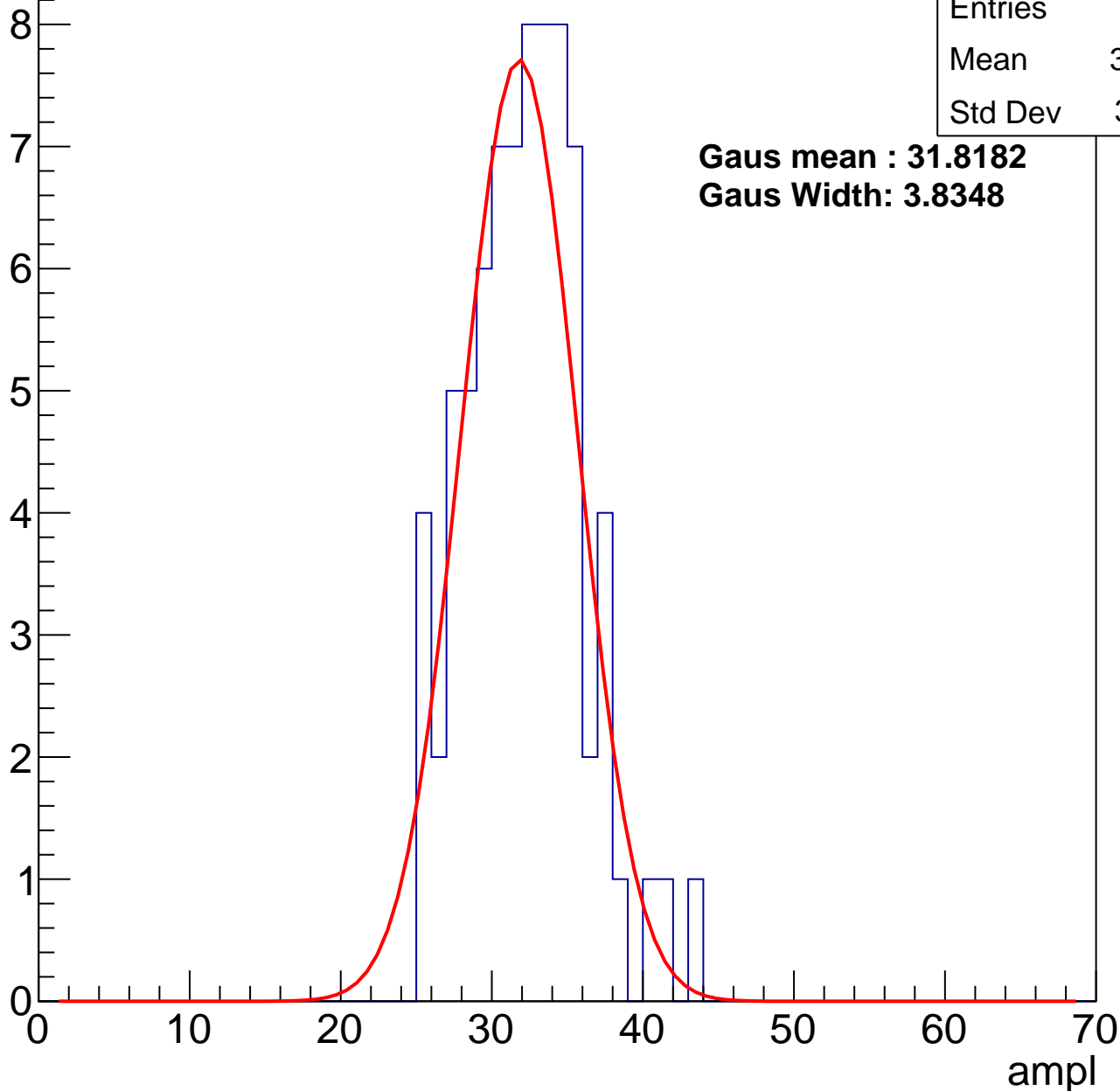
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	31.78
Std Dev	3.771

**Gaus mean : 31.8182**

**Gaus Width: 3.8348**



# B1L103S, U3-ch41, adc1

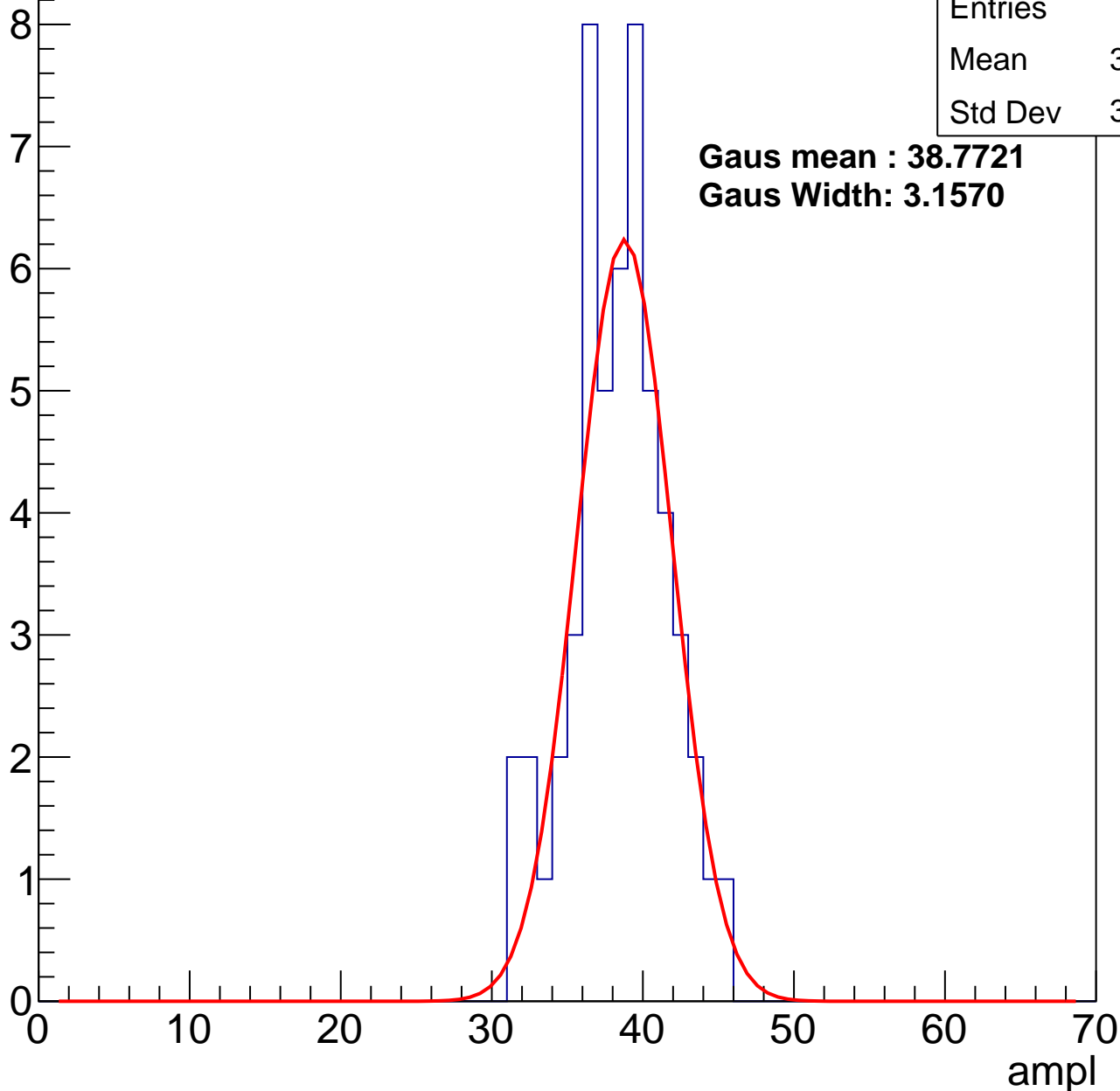
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	37.92
Std Dev	3.185

**Gaus mean : 38.7721**

**Gaus Width: 3.1570**



# B1L103S, U3-ch41, adc2

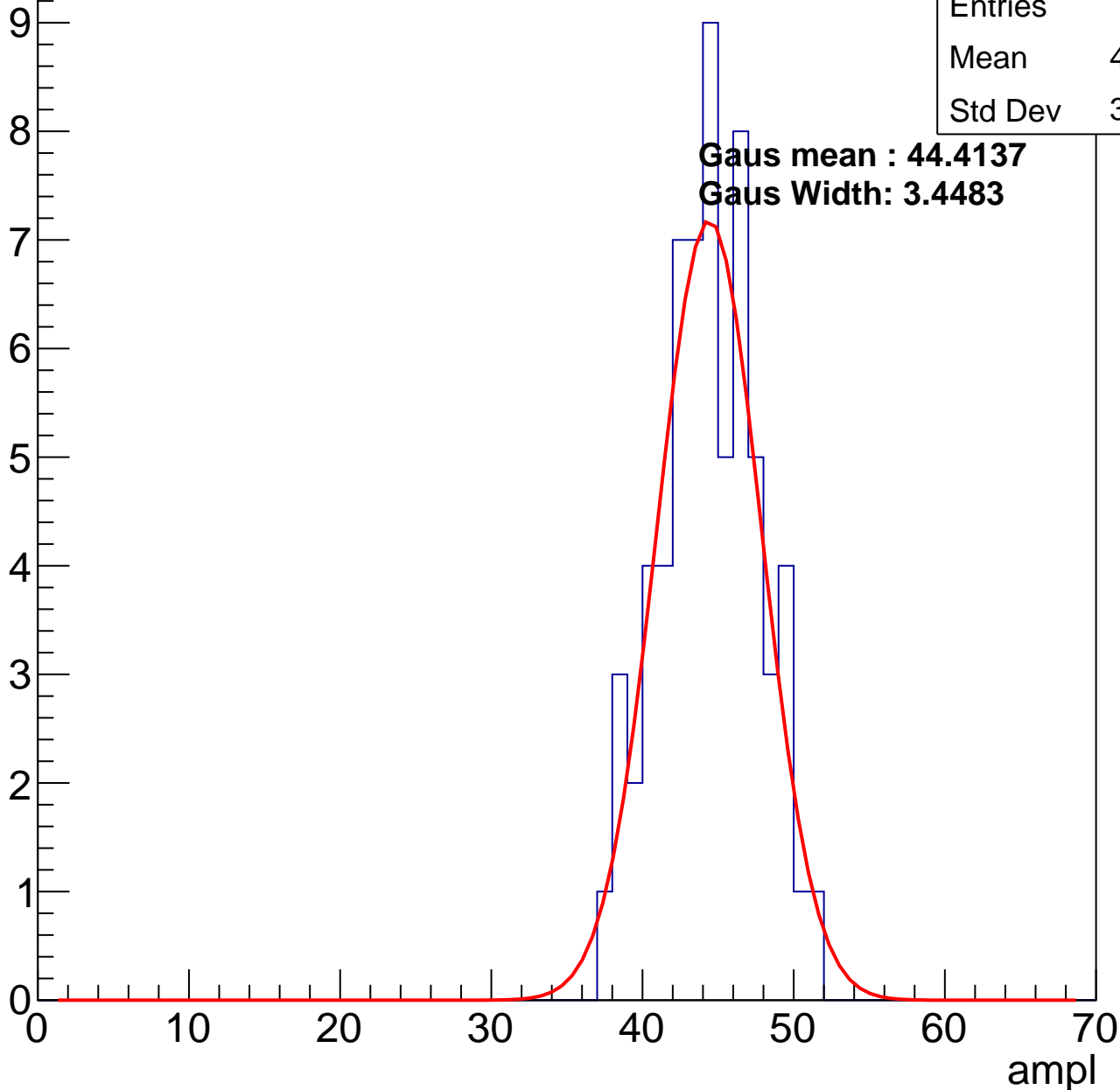
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	43.95
Std Dev	3.204

**Gaus mean : 44.4137**

**Gaus Width: 3.4483**

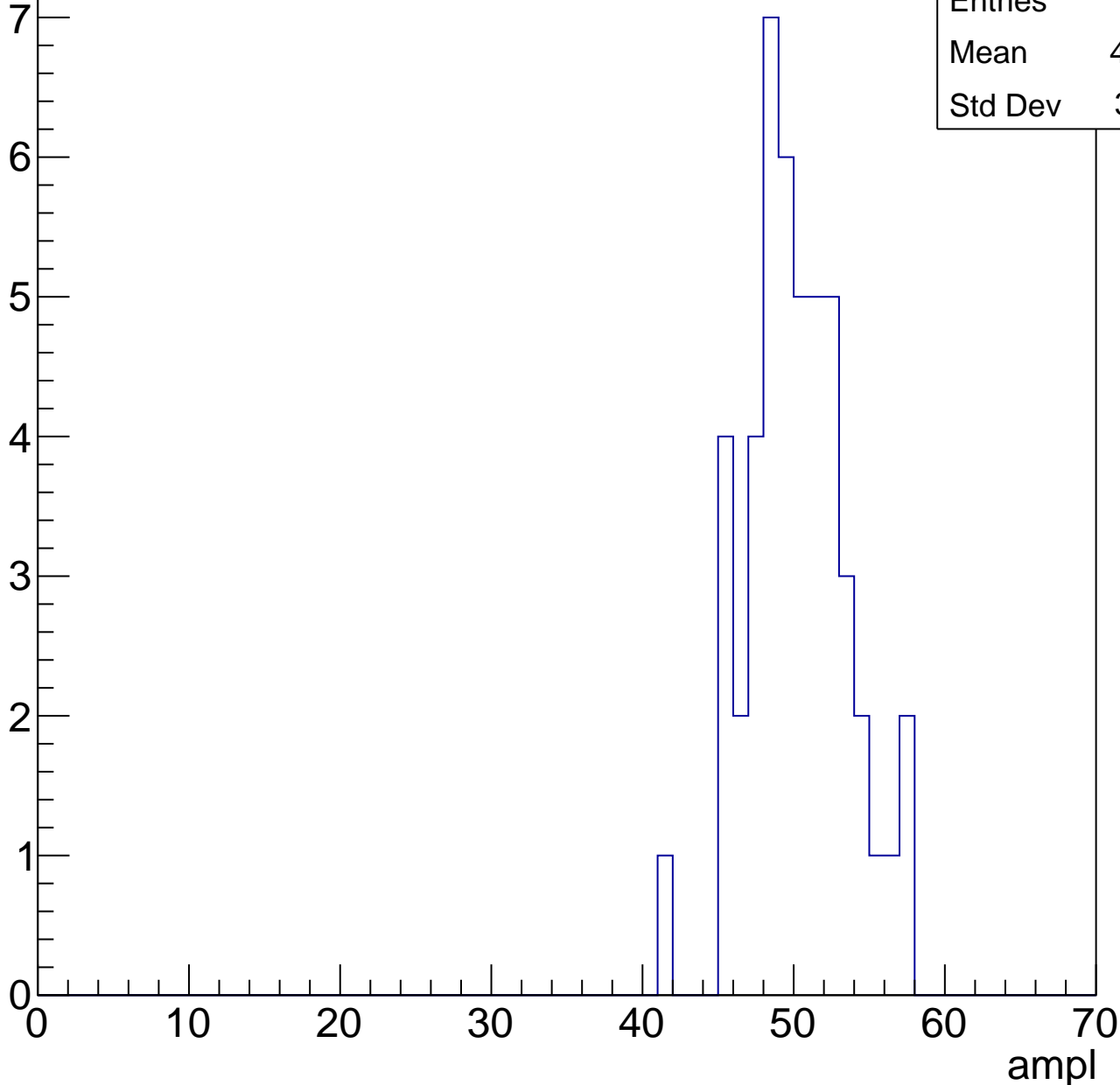


# B1L103S, U3-ch41, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	48
Mean	49.75
Std Dev	3.301

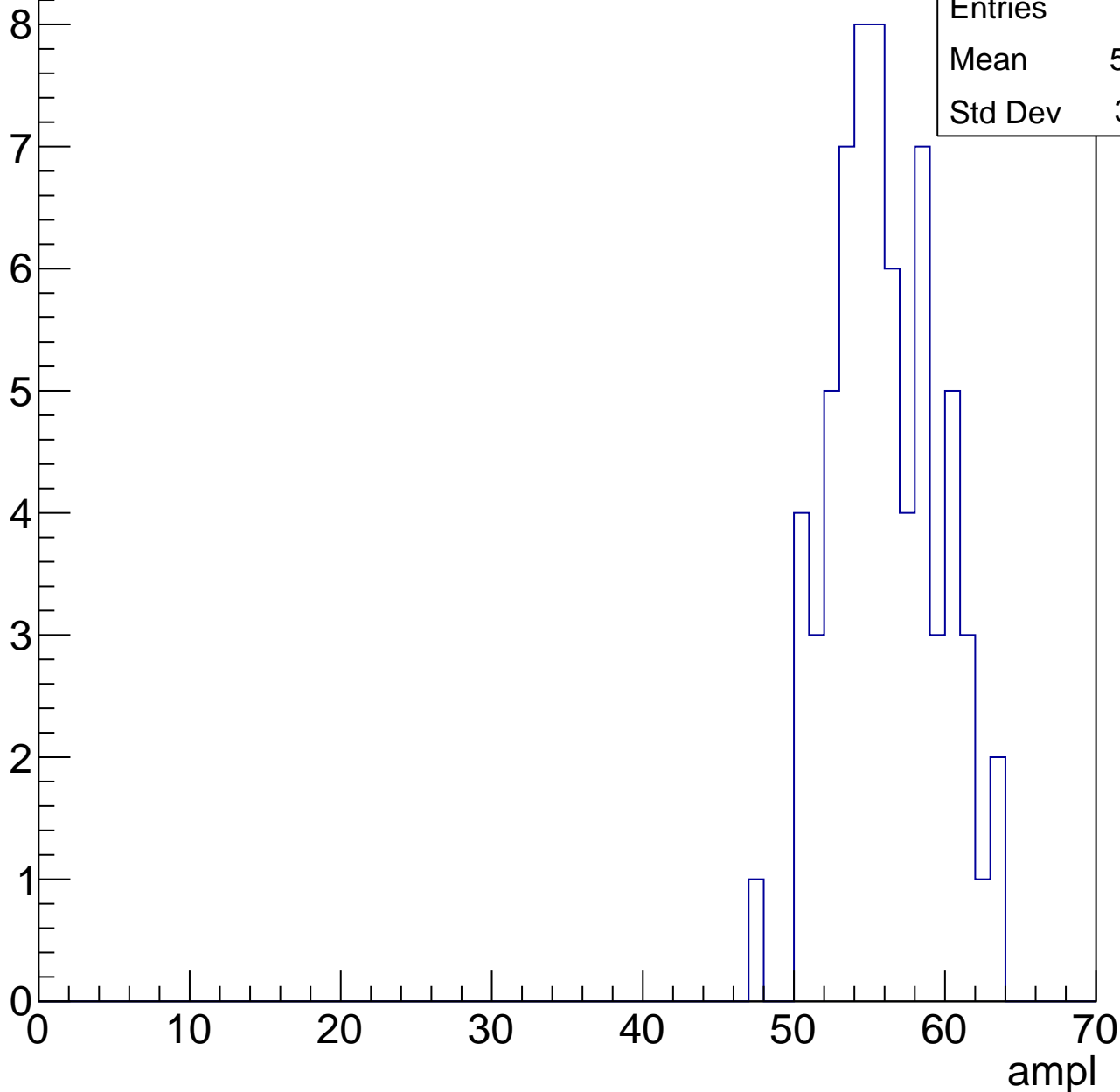


# B1L103S, U3-ch41, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	55.54
Std Dev	3.491

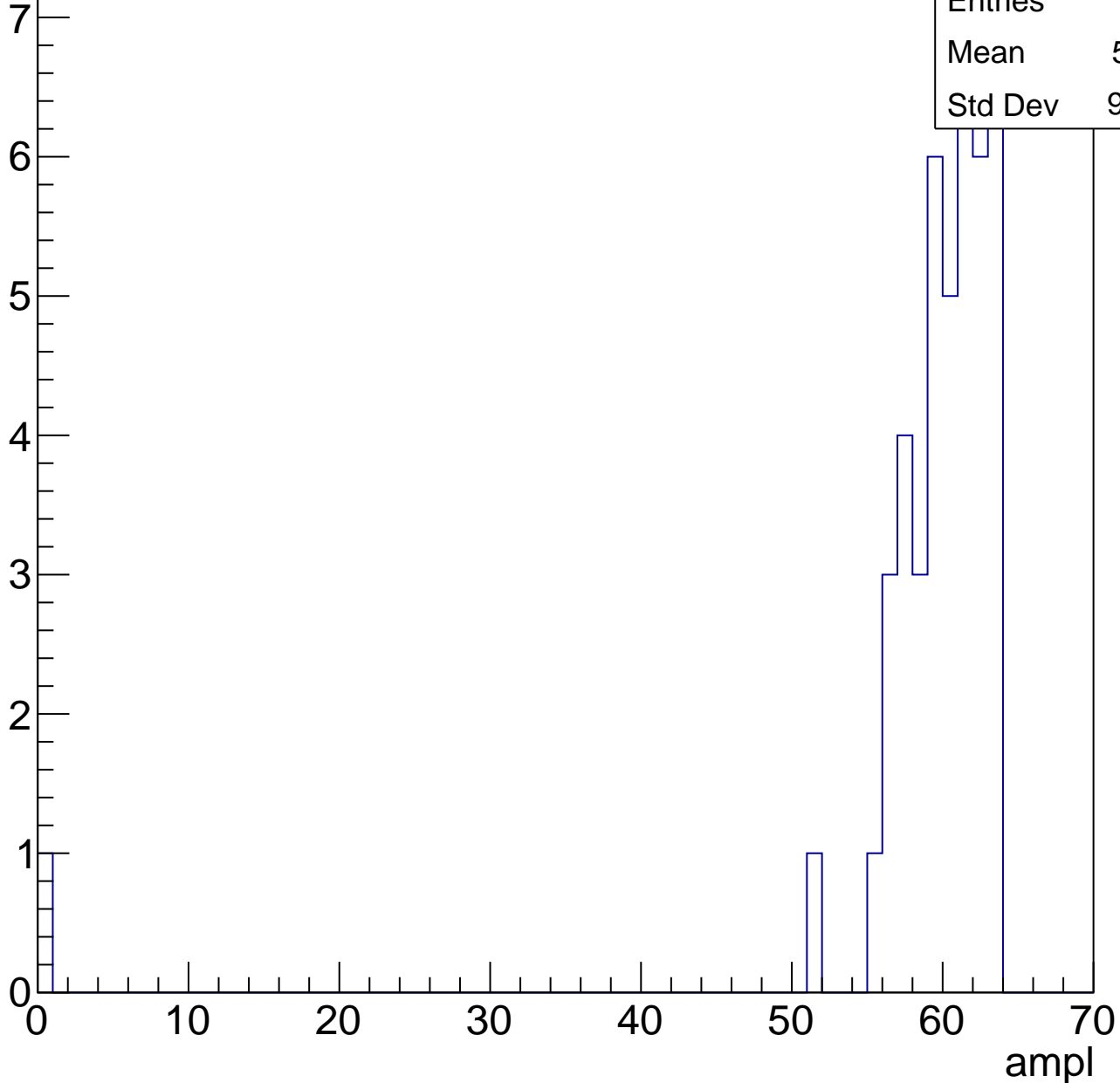


# B1L103S, U3-ch41, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

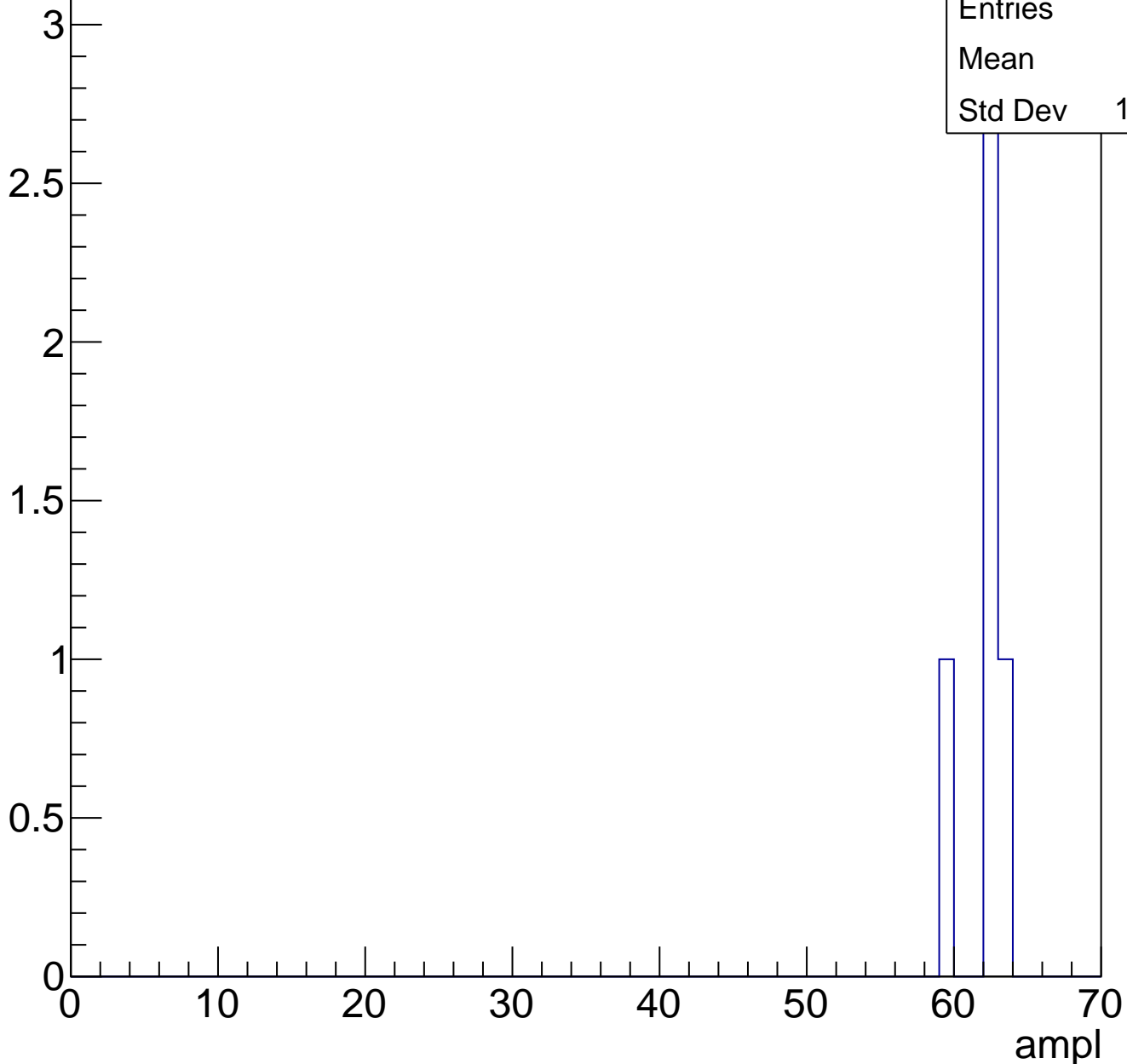
Entries	44
Mean	58.41
Std Dev	9.282



# B1L103S, U3-ch41, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	5
Mean	61.6
Std Dev	1.356



# B1L103S, U3-ch41, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	10
Std Dev	10

# B1L103S, U3-ch42, adc0

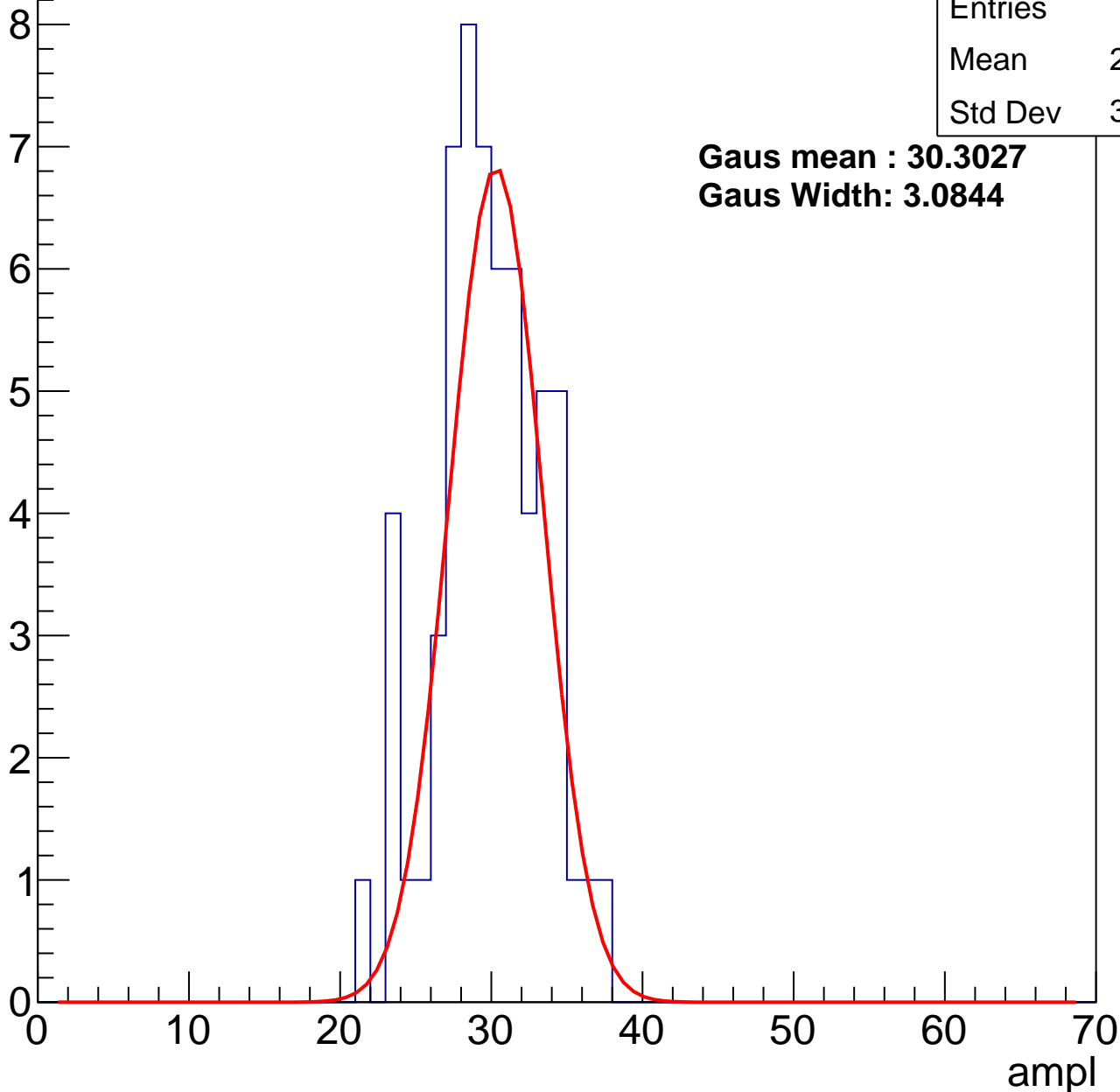
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	29.39
Std Dev	3.442

**Gaus mean : 30.3027**

**Gaus Width: 3.0844**



# B1L103S, U3-ch42, adc1

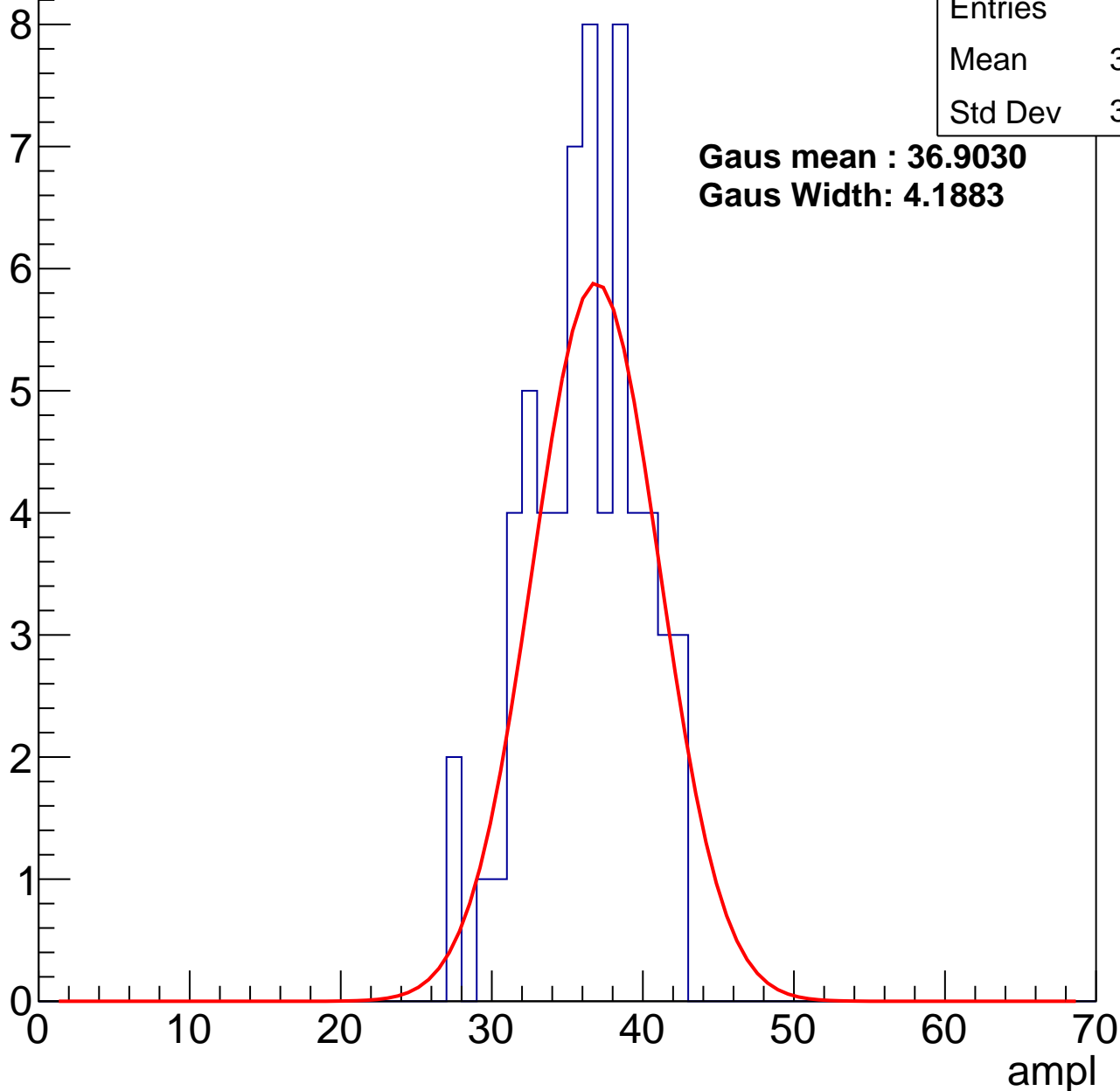
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	35.73
Std Dev	3.593

**Gaus mean : 36.9030**

**Gaus Width: 4.1883**



# B1L103S, U3-ch42, adc2

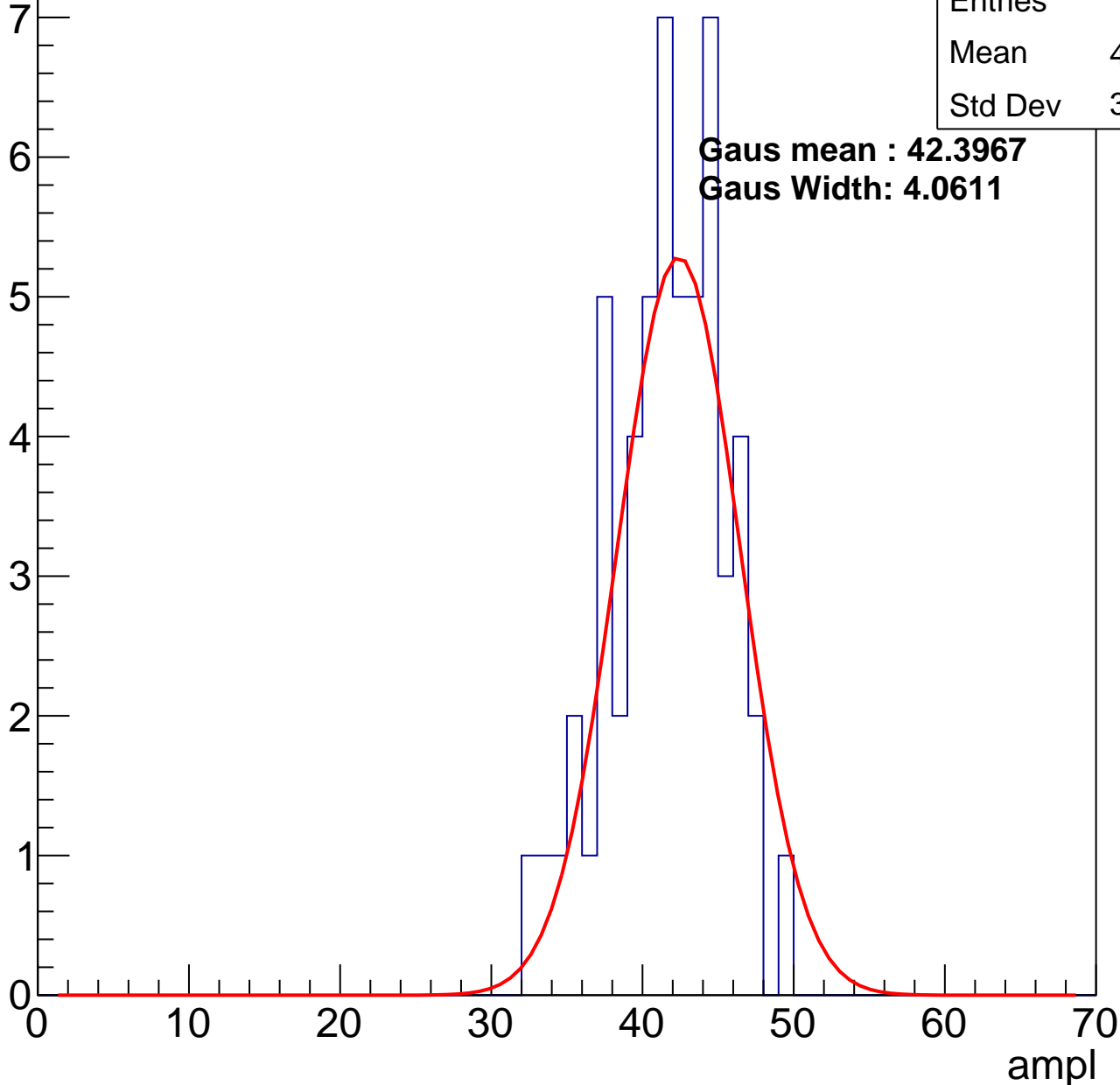
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	41.14
Std Dev	3.734

**Gaus mean : 42.3967**

**Gaus Width: 4.0611**

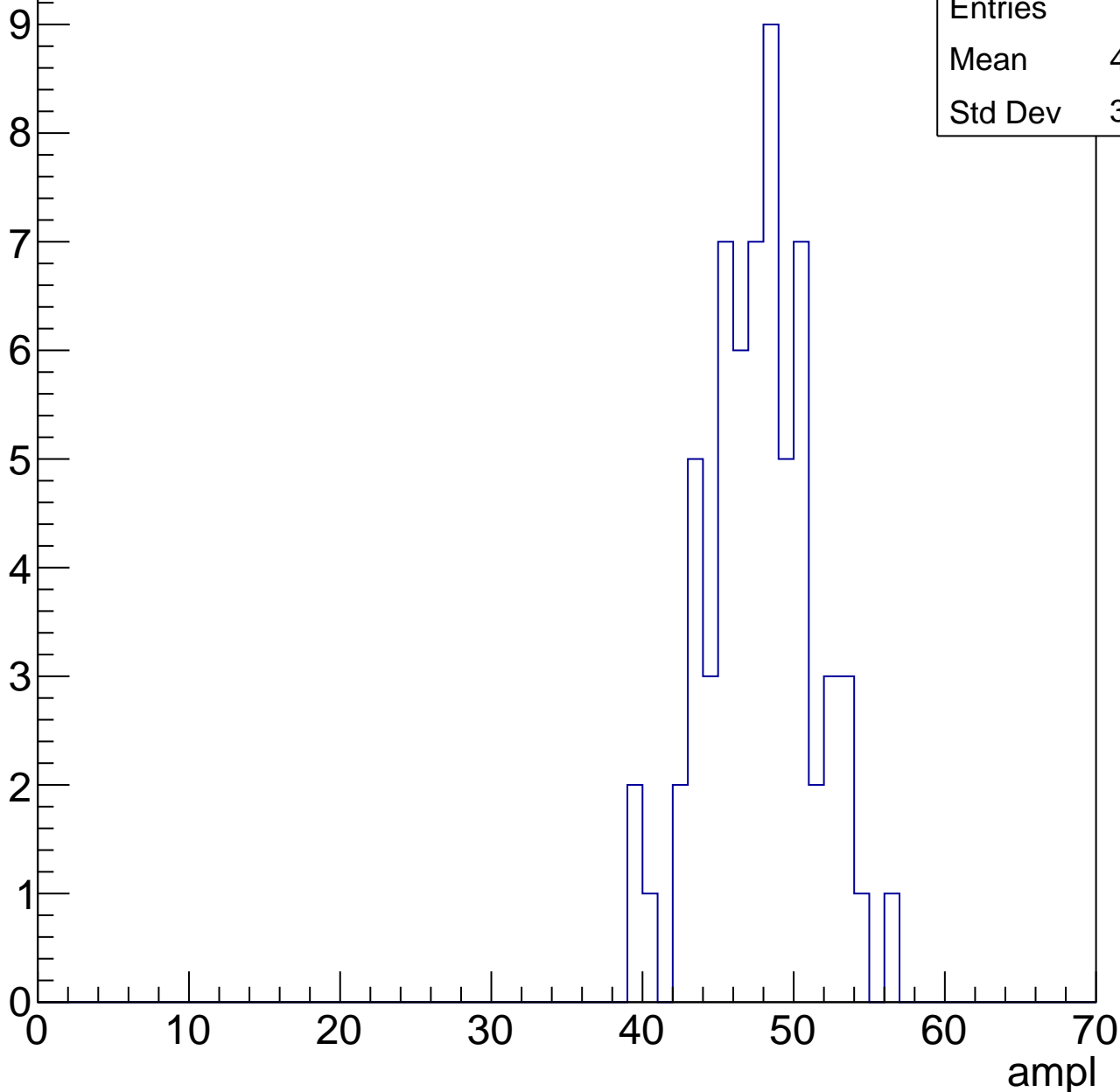


# B1L103S, U3-ch42, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	47.23
Std Dev	3.539

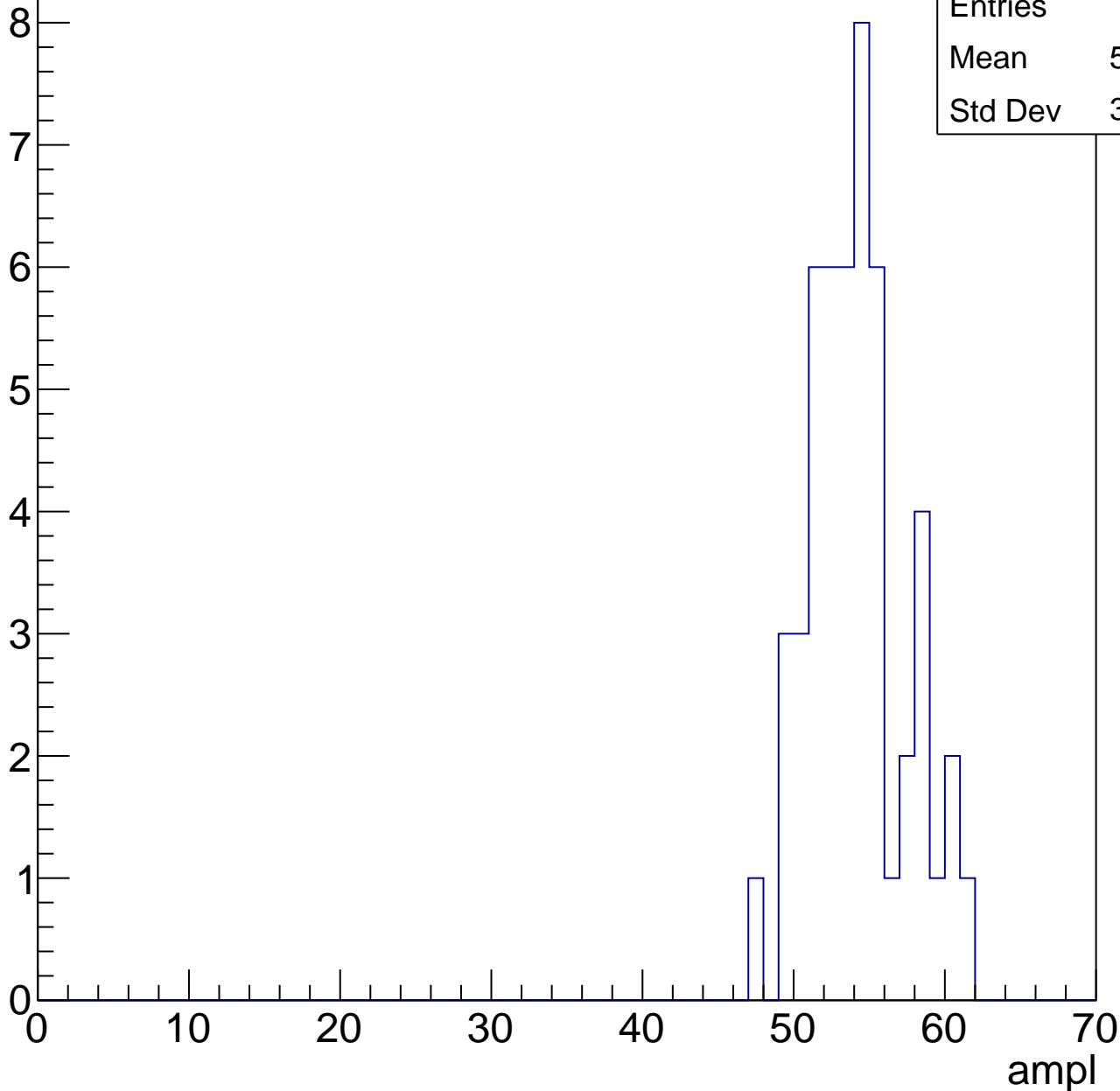


# B1L103S, U3-ch42, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

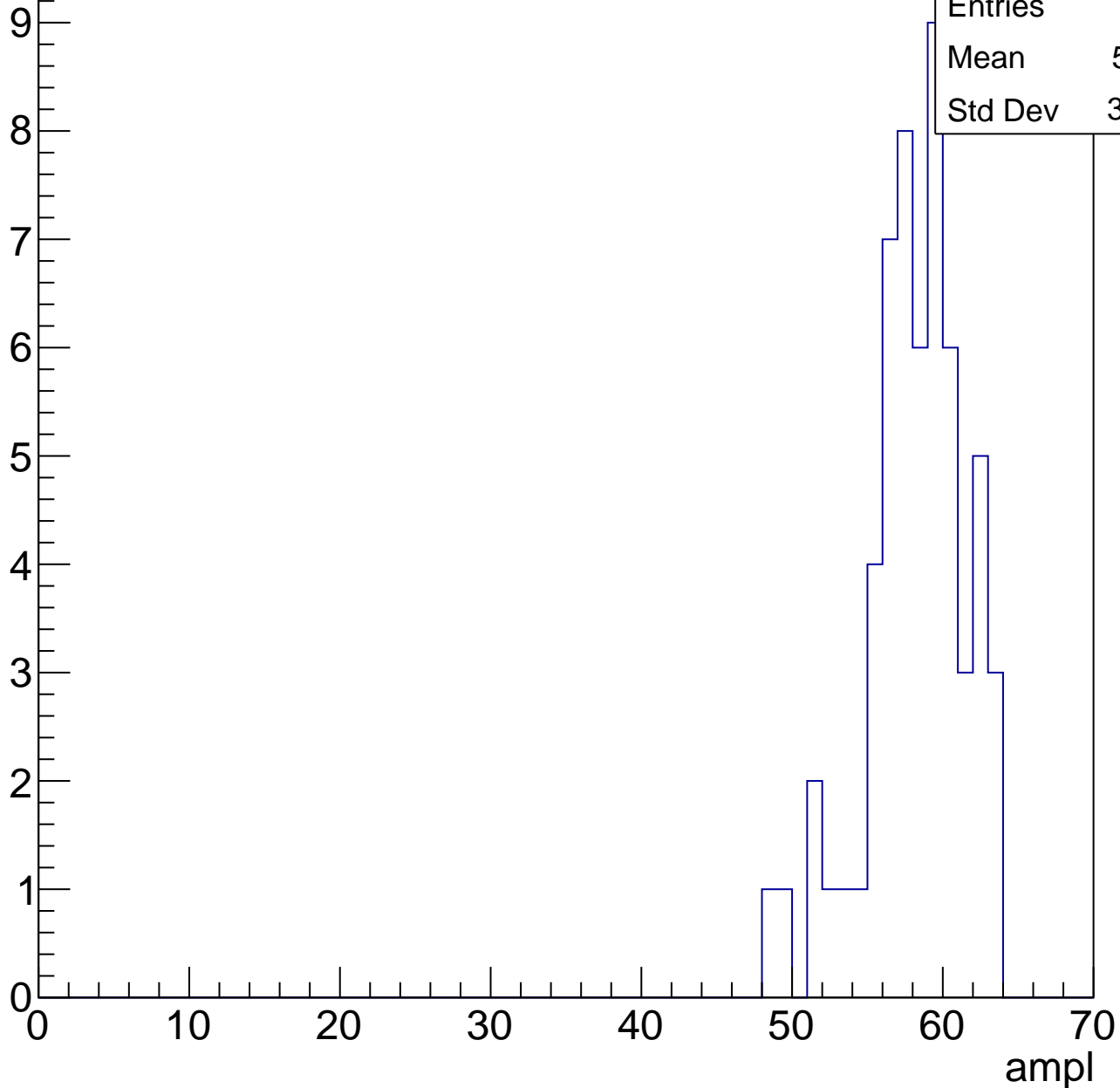
Entries	50
Mean	53.68
Std Dev	3.127



# B1L103S, U3-ch42, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

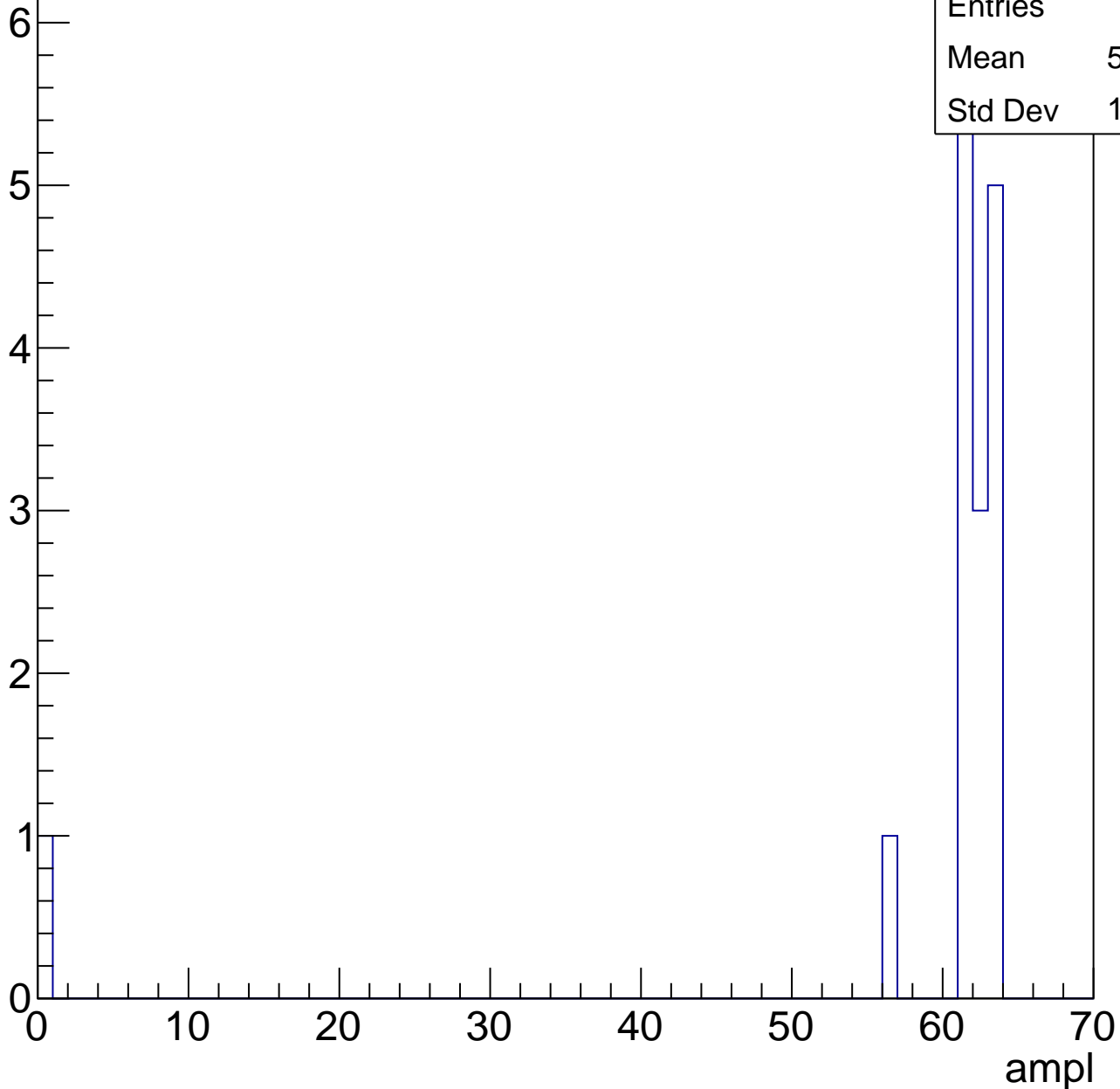


# B1L103S, U3-ch42, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	16
Mean	57.69
Std Dev	14.99

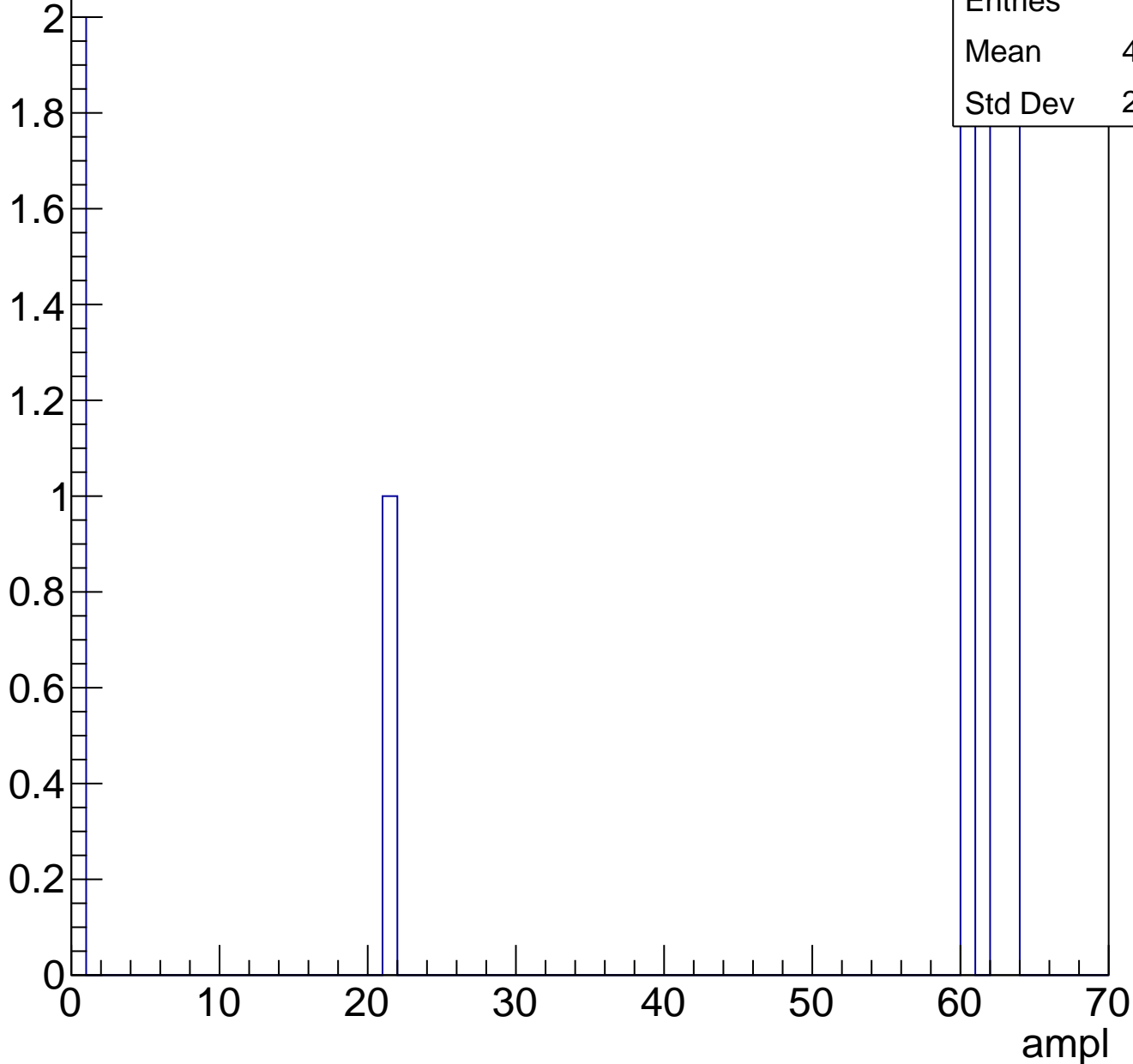




# B1L103S, U3-ch42, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch43, adc0

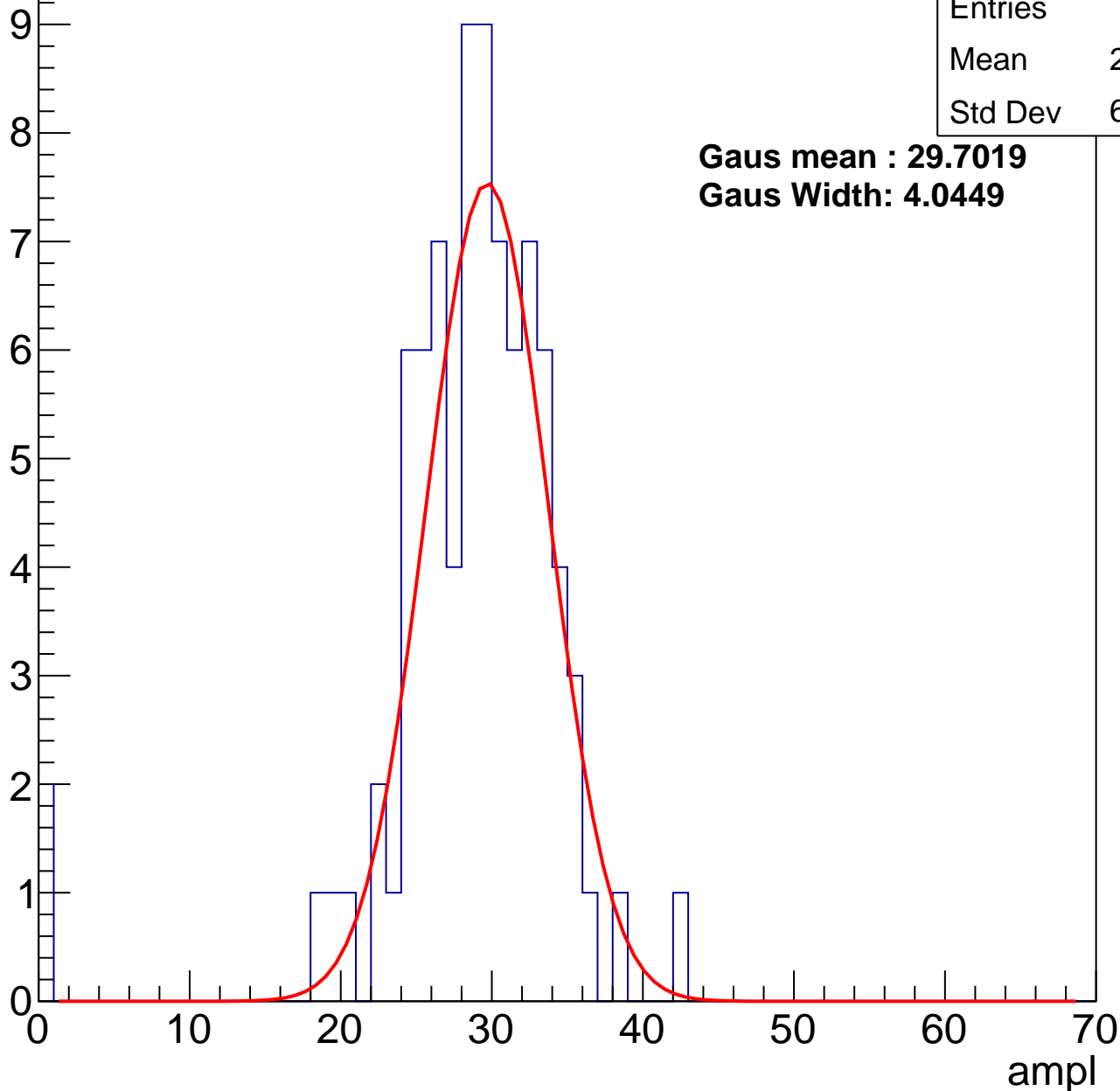
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	85
Mean	28.19
Std Dev	6.032

**Gaus mean : 29.7019**

**Gaus Width: 4.0449**



# B1L103S, U3-ch43, adc1

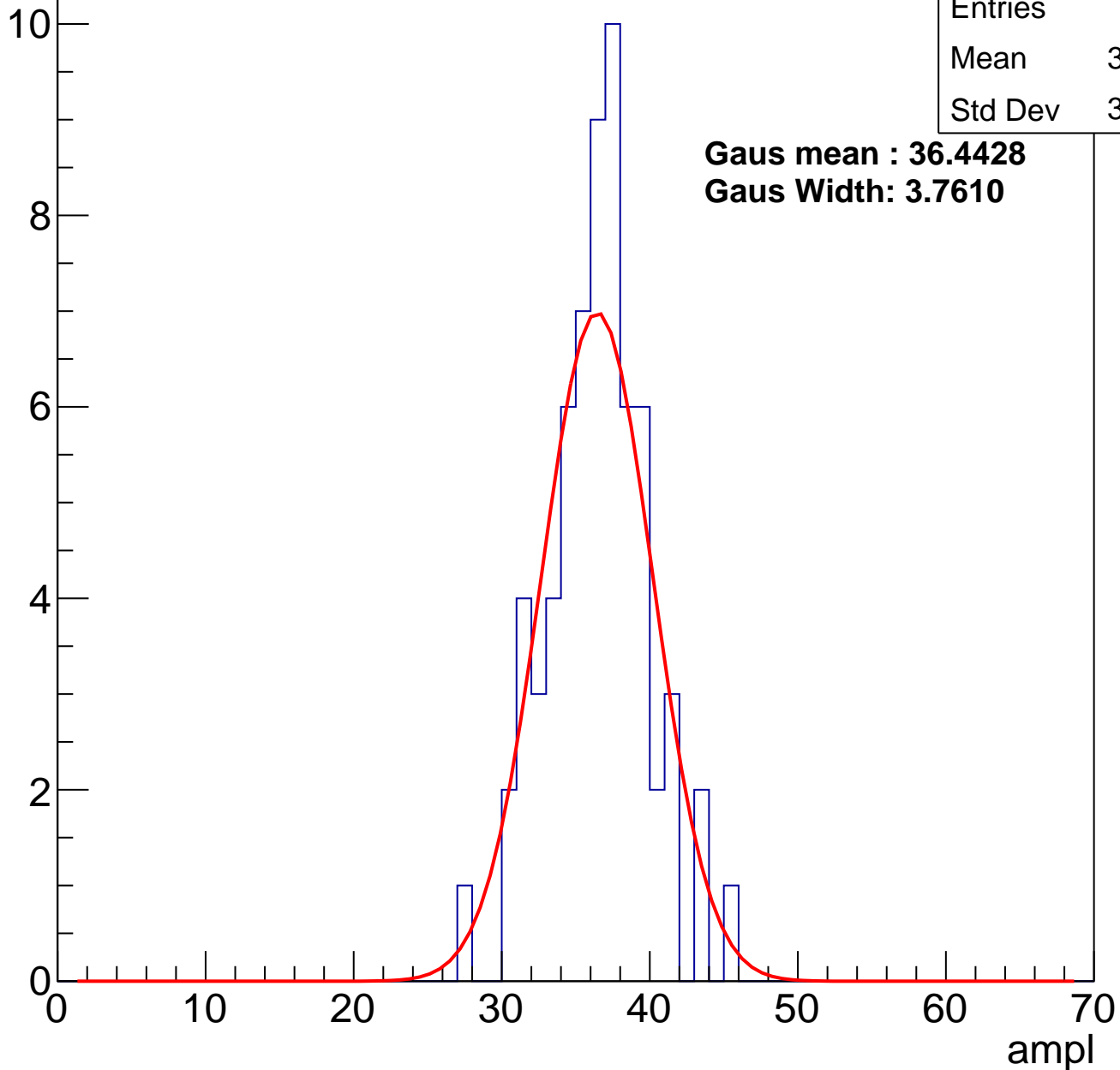
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	66
Mean	36.03
Std Dev	3.353

**Gaus mean : 36.4428**

**Gaus Width: 3.7610**

Entry



# B1L103S, U3-ch43, adc2

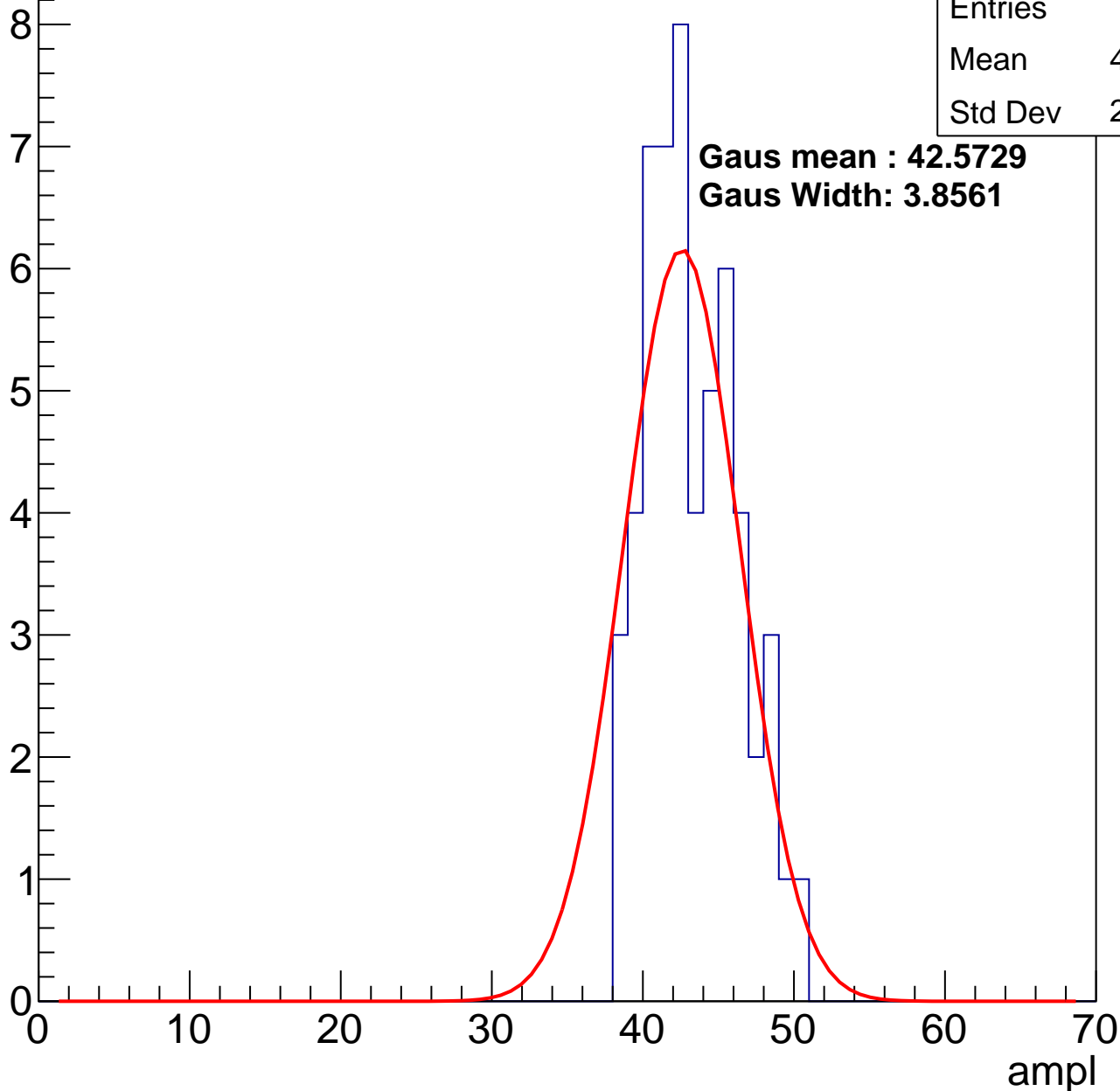
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	42.84
Std Dev	2.996

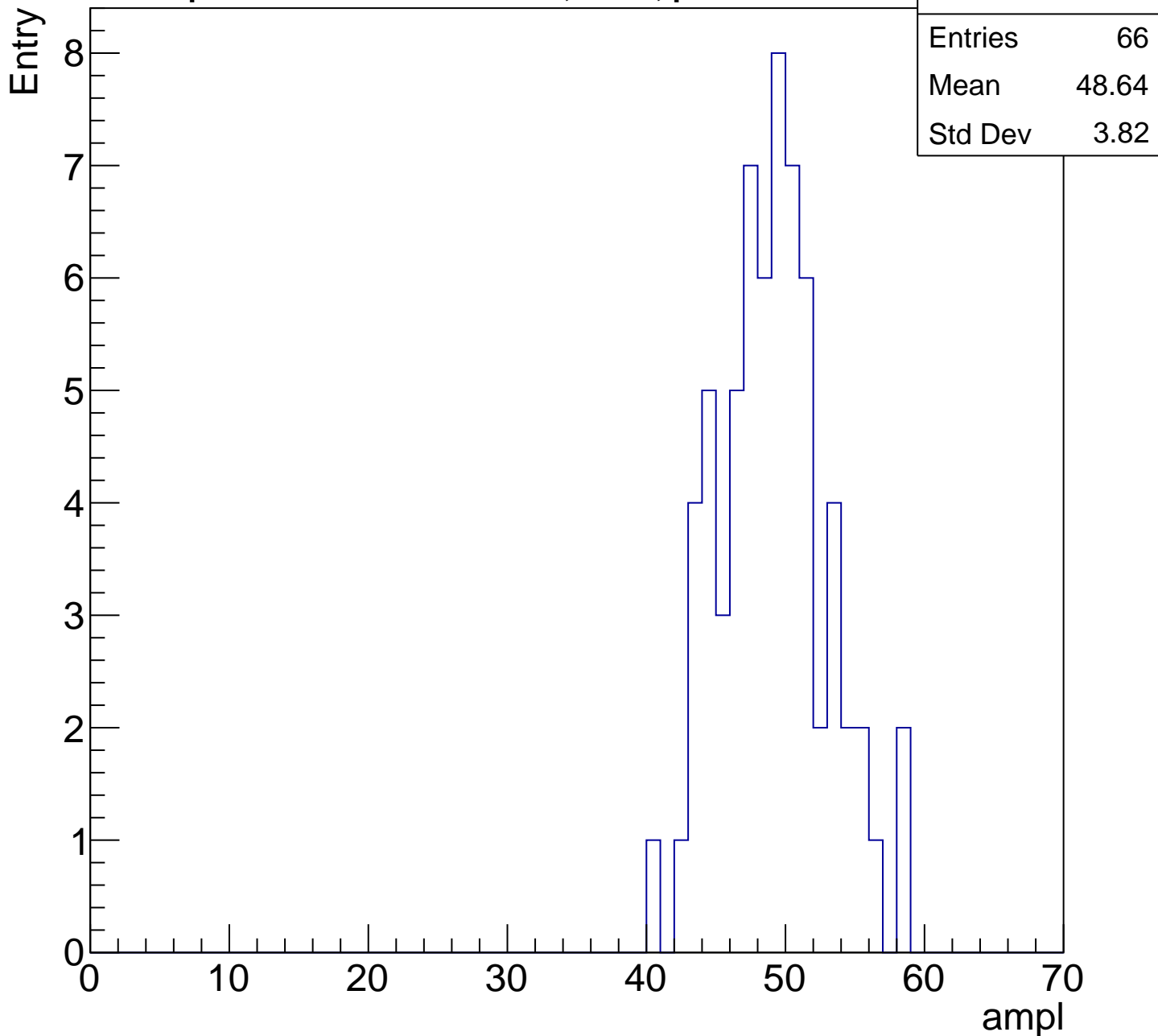
**Gaus mean : 42.5729**

**Gaus Width: 3.8561**



# B1L103S, U3-ch43, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

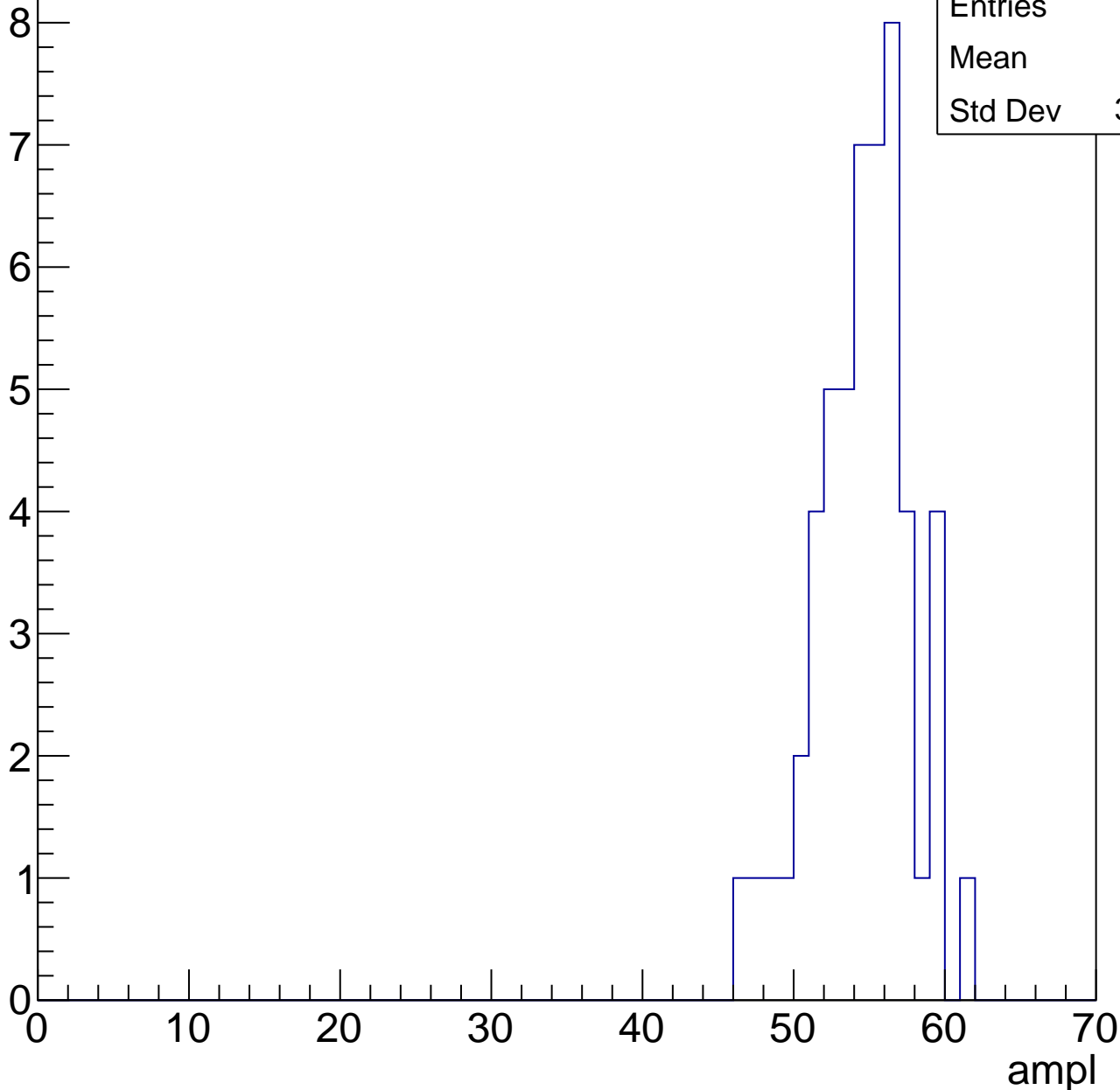


# B1L103S, U3-ch43, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	54.1
Std Dev	3.121



# B1L103S, U3-ch43, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

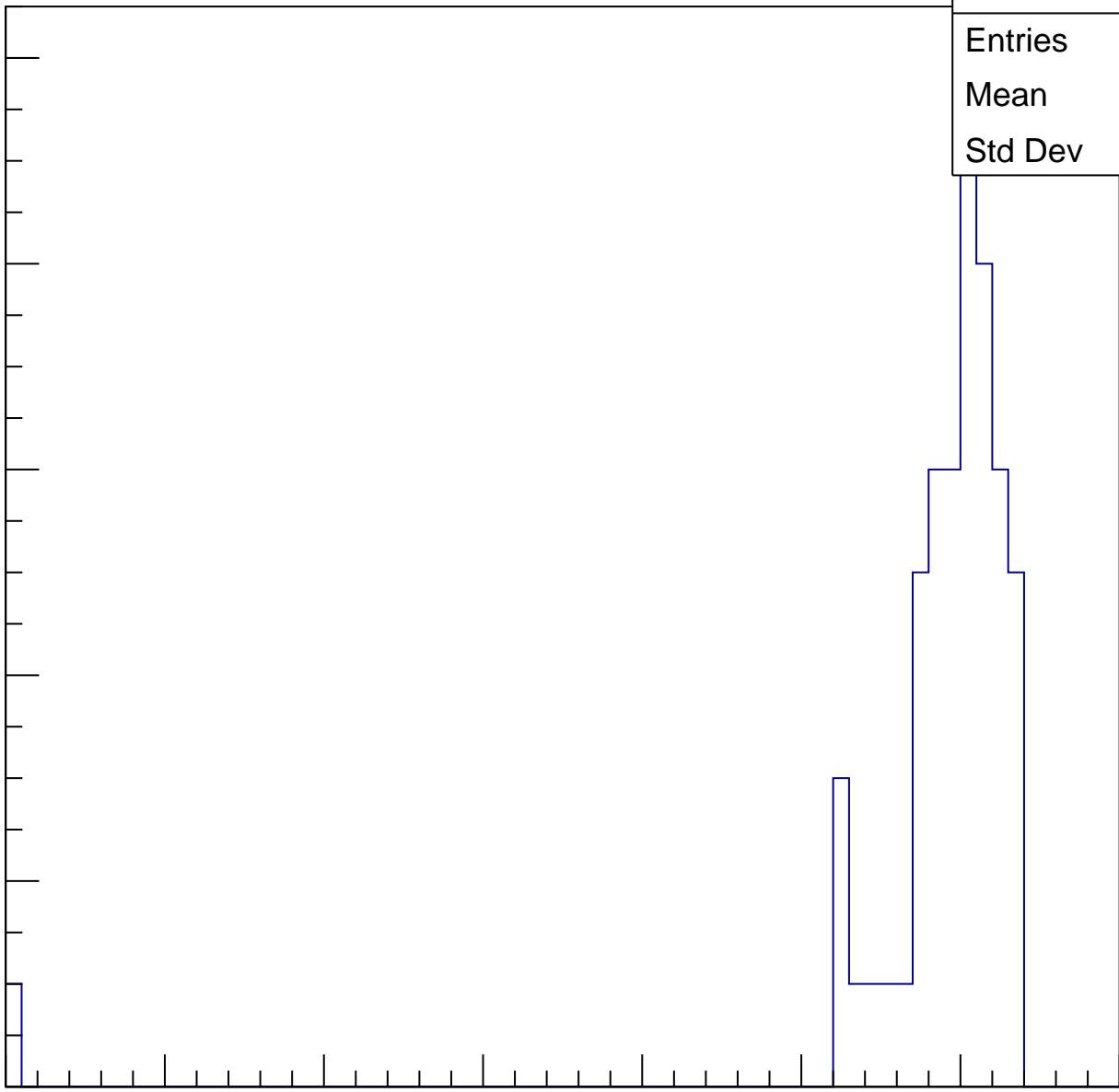
Entries	54
Mean	58.07
Std Dev	8.465

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

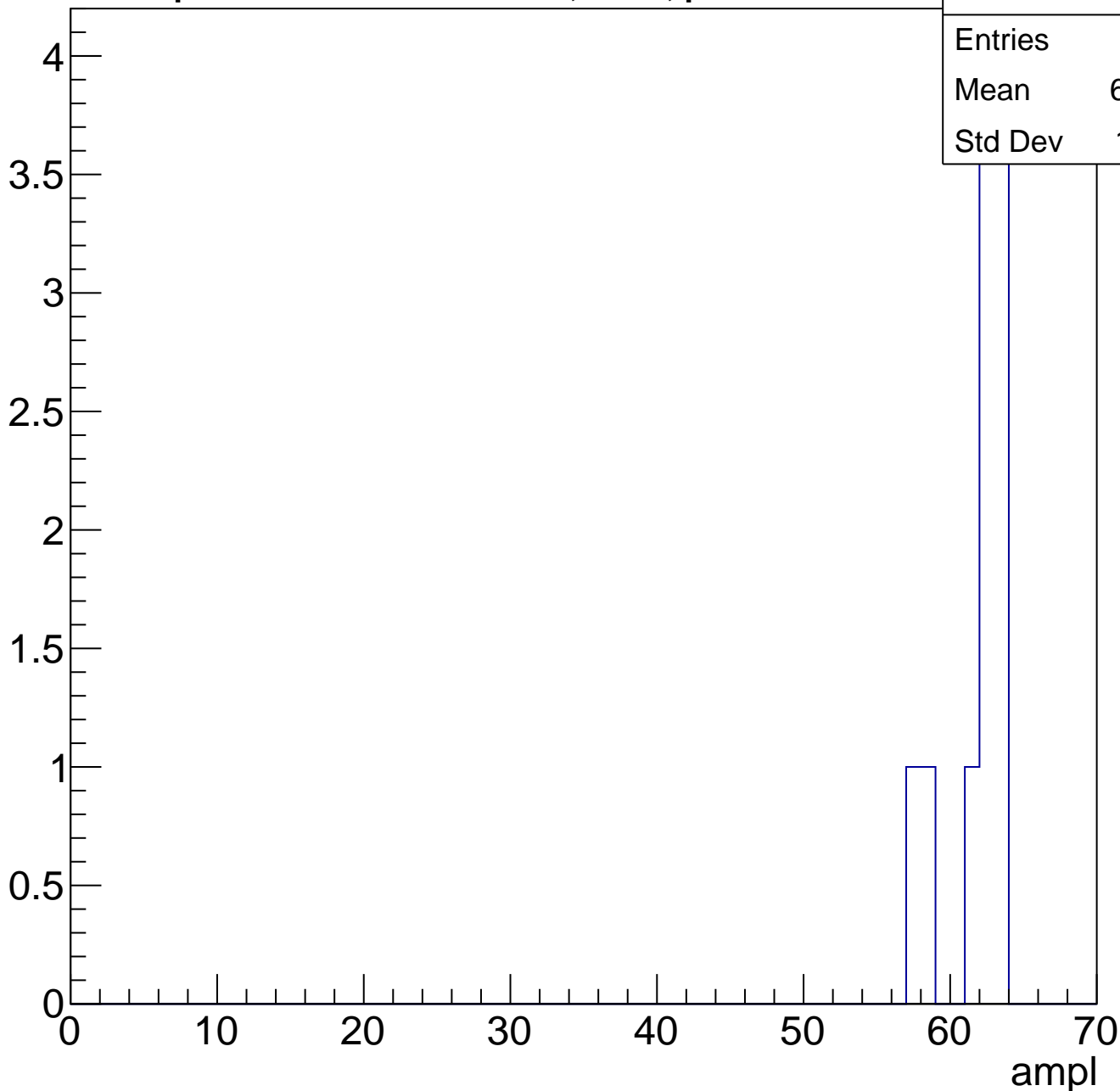
ampl



# B1L103S, U3-ch43, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U3-ch43, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch44, adc0

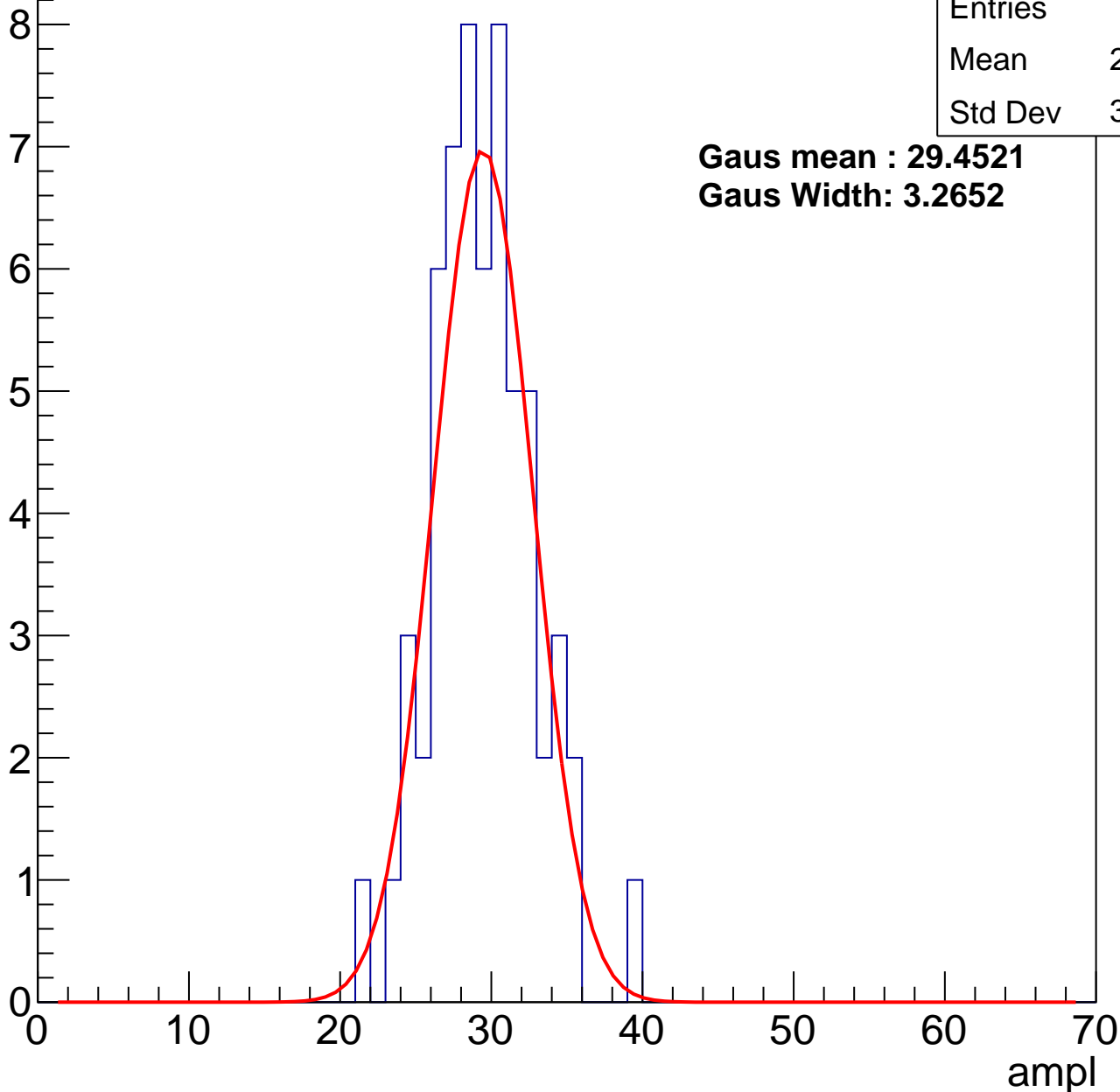
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	29.02
Std Dev	3.289

**Gaus mean : 29.4521**

**Gaus Width: 3.2652**



# B1L103S, U3-ch44, adc1

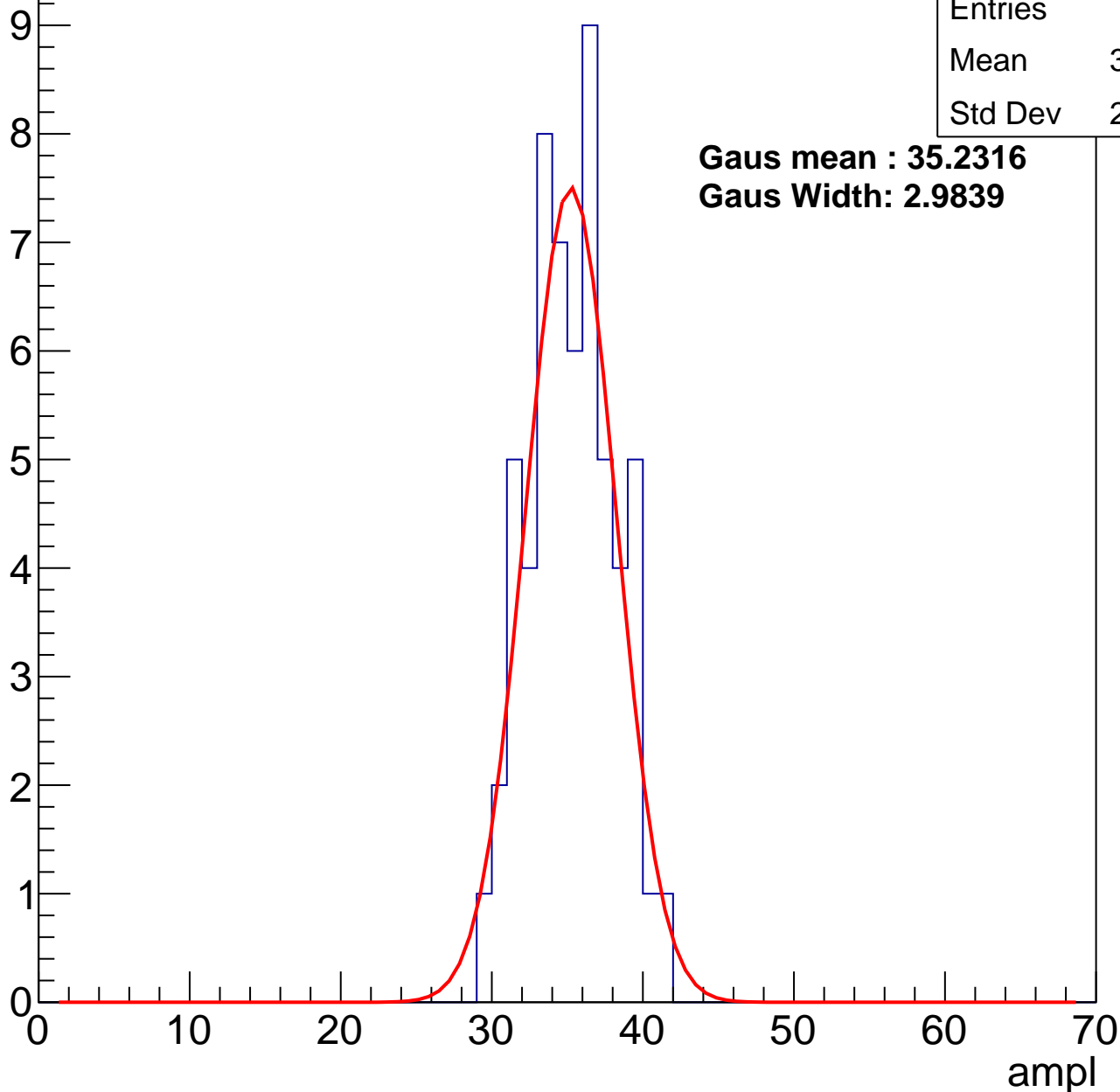
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	34.84
Std Dev	2.772

**Gaus mean : 35.2316**

**Gaus Width: 2.9839**



# B1L103S, U3-ch44, adc2

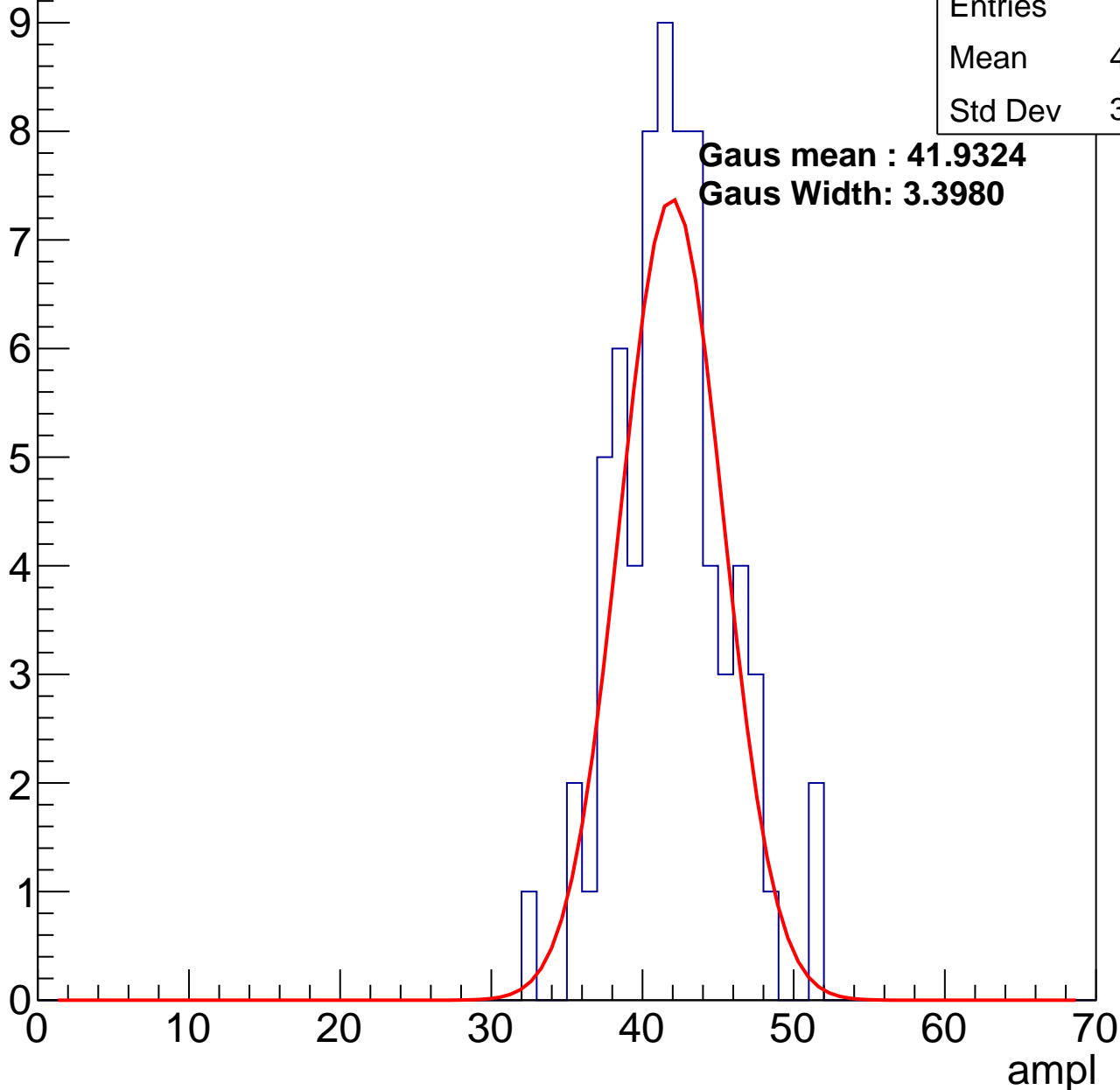
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	41.48
Std Dev	3.614

**Gaus mean : 41.9324**

**Gaus Width: 3.3980**

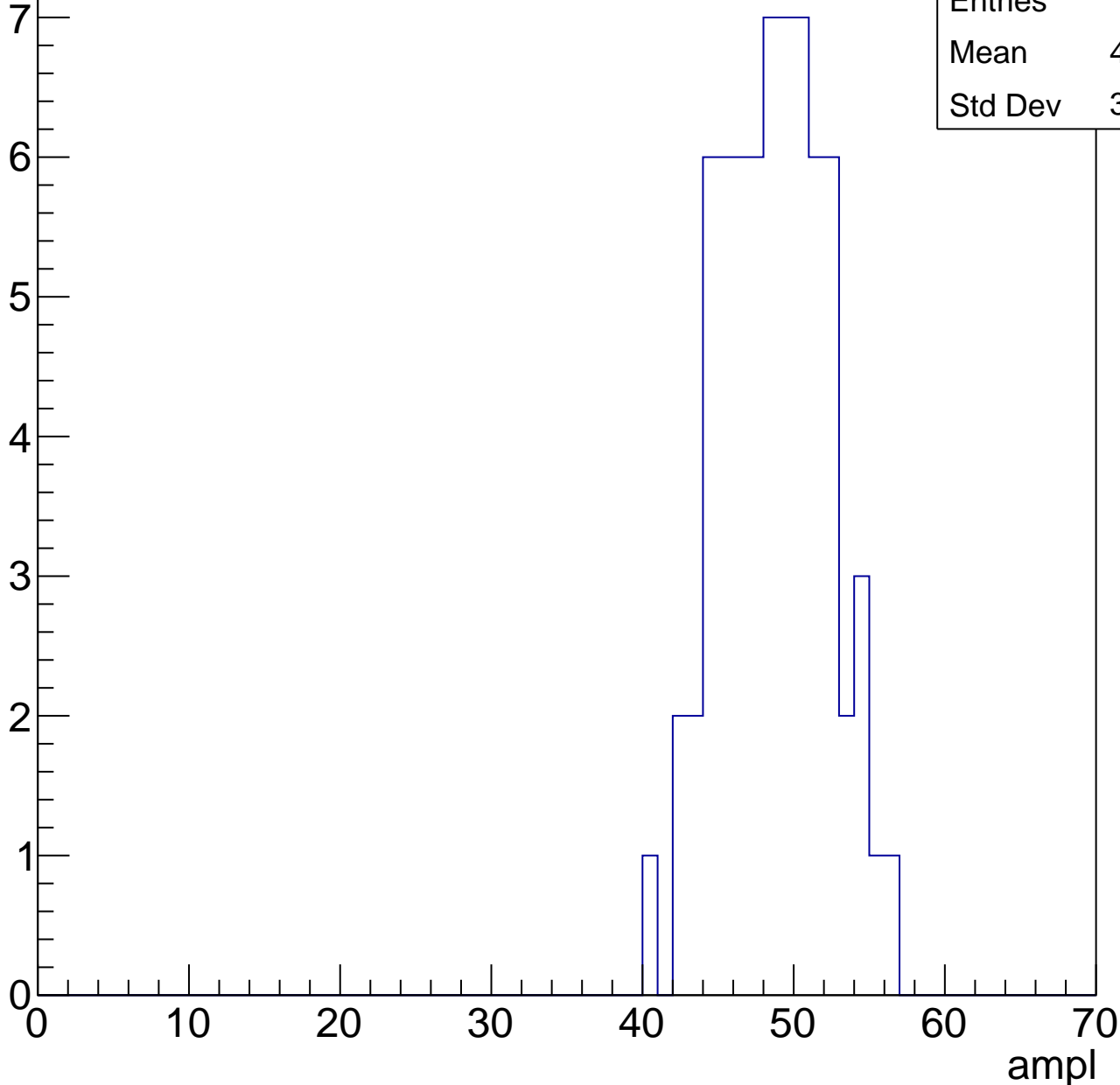


# B1L103S, U3-ch44, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	48.23
Std Dev	3.444

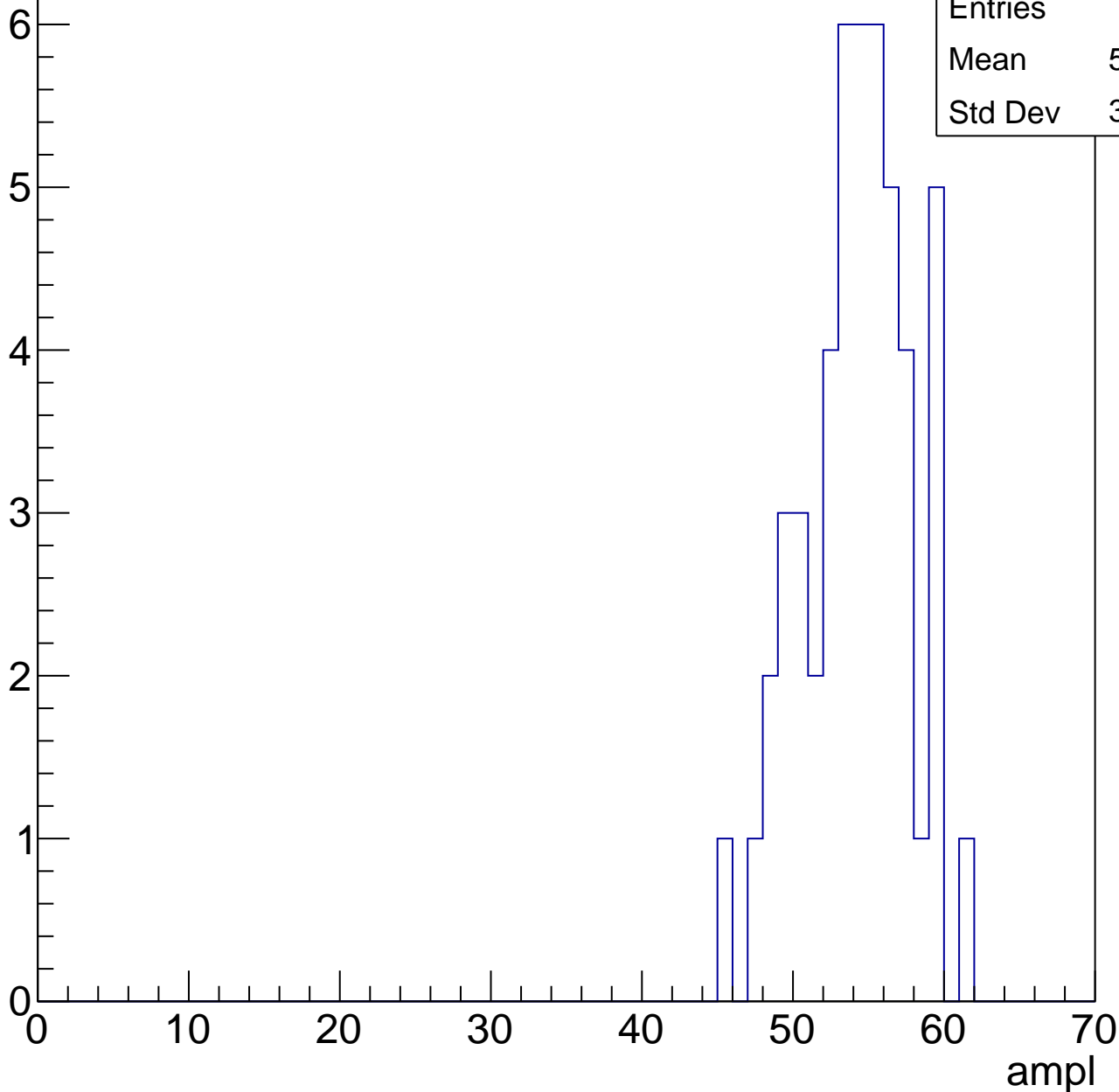


# B1L103S, U3-ch44, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

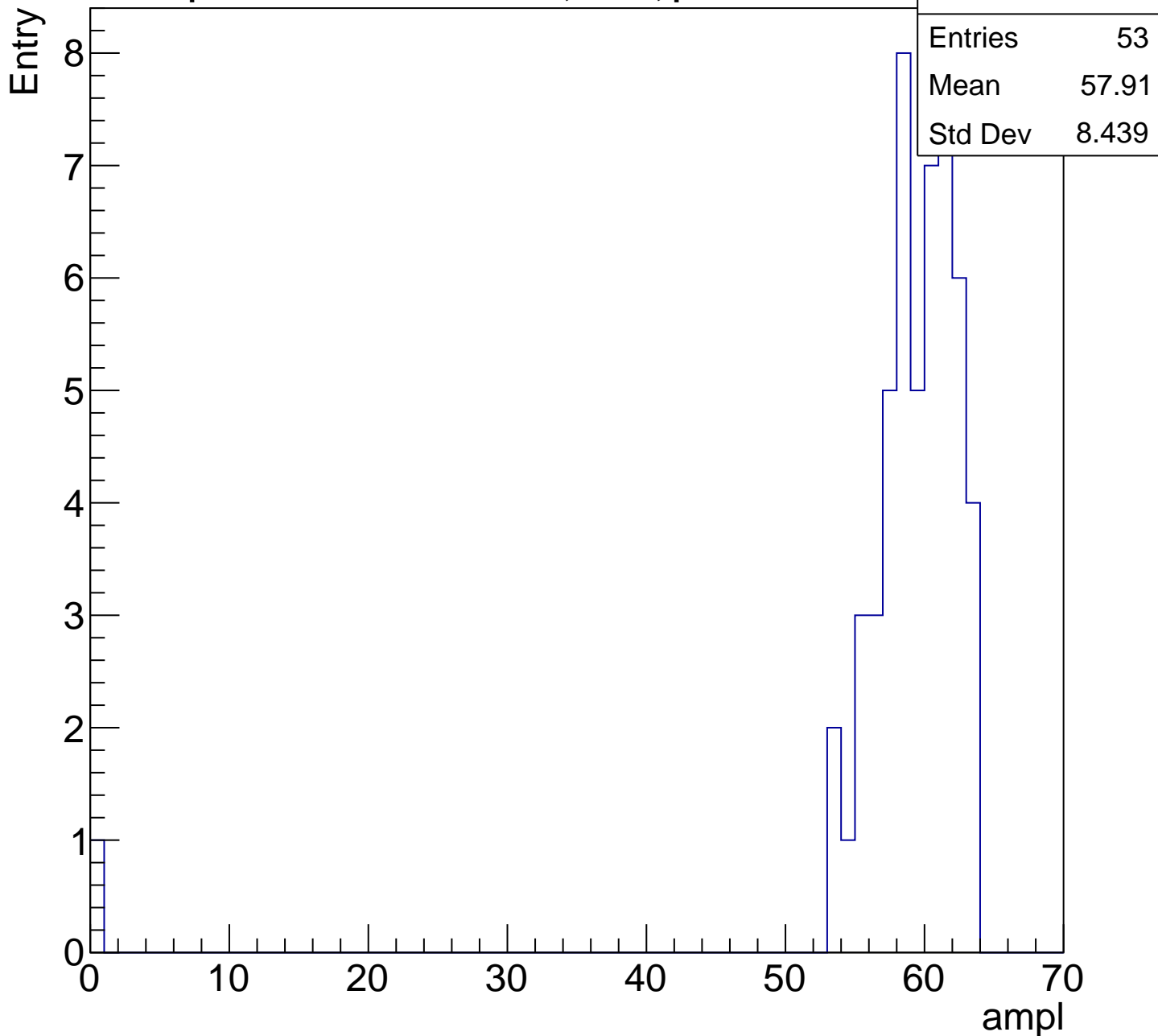
Entry

Entries	50
Mean	53.78
Std Dev	3.506



# B1L103S, U3-ch44, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

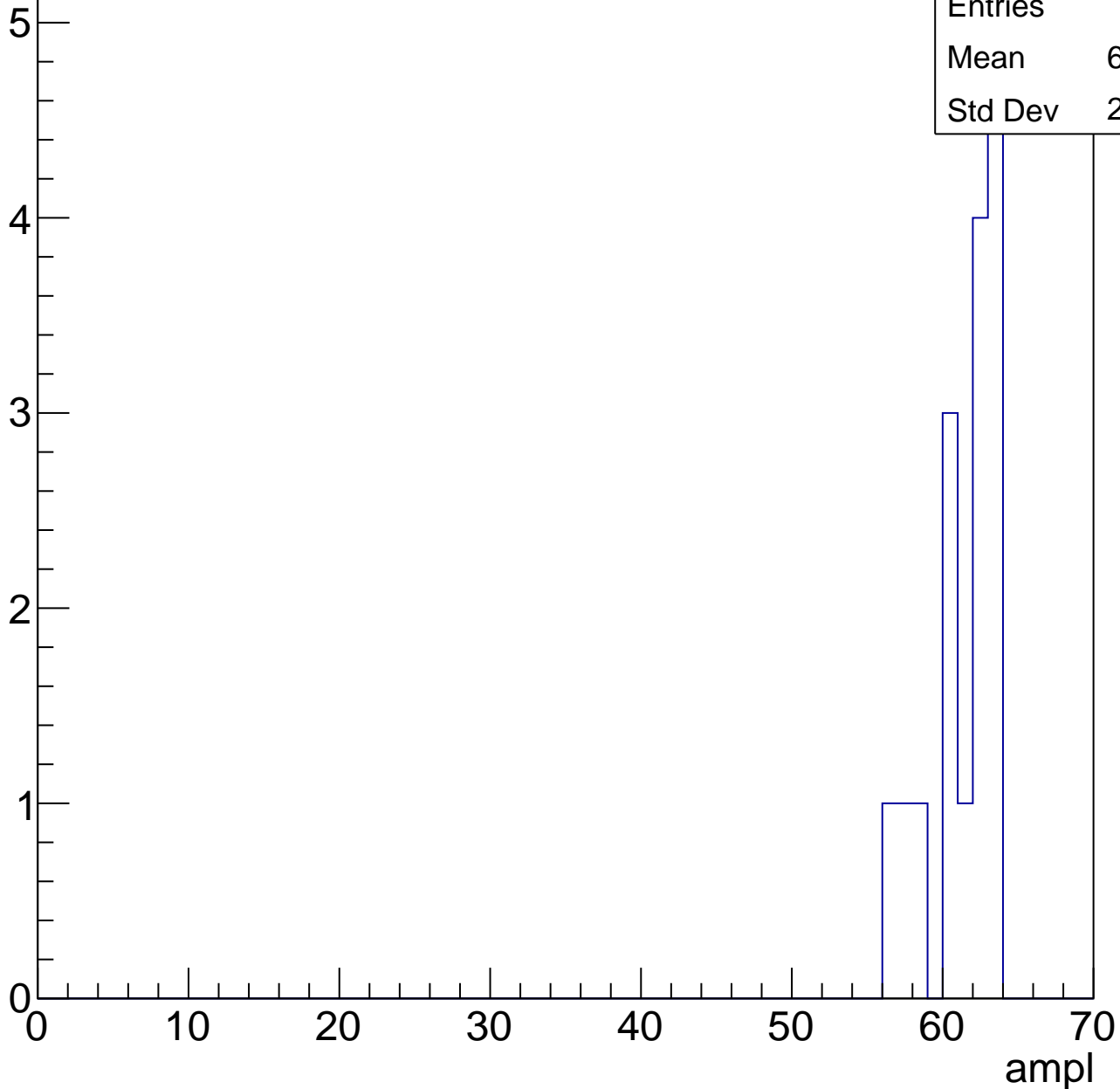


# B1L103S, U3-ch44, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	16
Mean	60.94
Std Dev	2.193





# B1L103S, U3-ch44, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch45, adc0

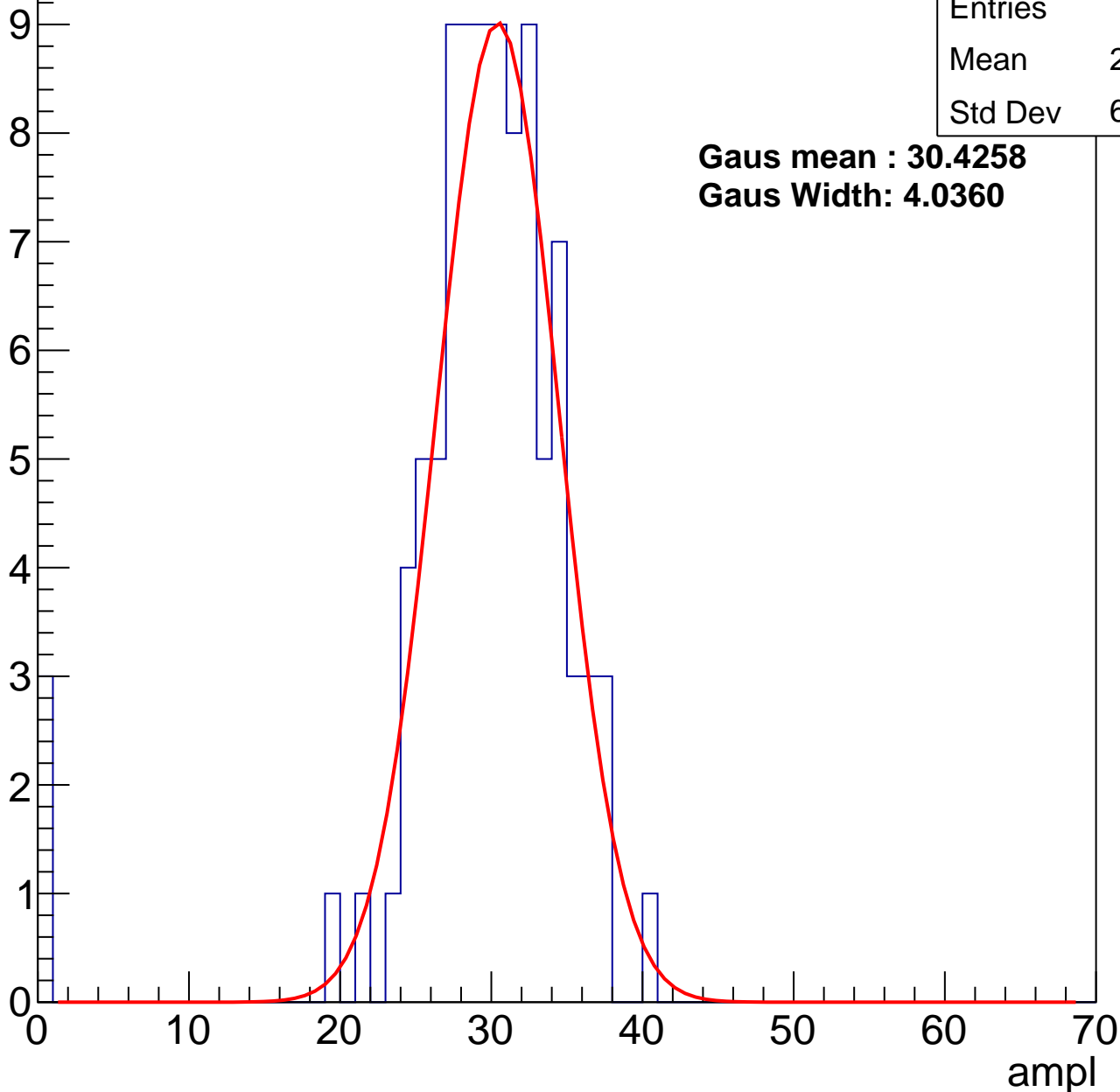
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	95
Mean	28.87
Std Dev	6.437

**Gaus mean : 30.4258**

**Gaus Width: 4.0360**



# B1L103S, U3-ch45, adc1

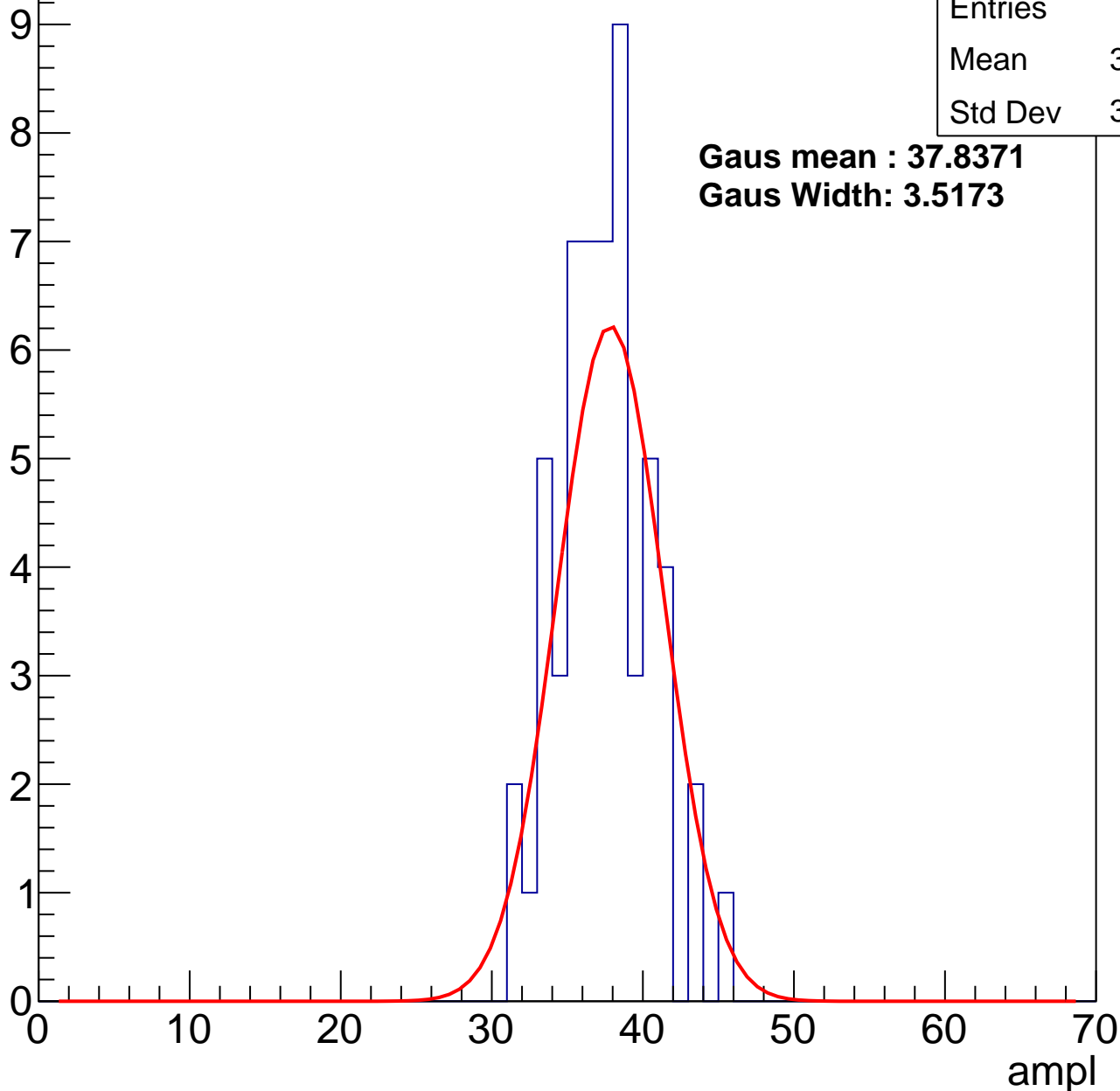
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	36.98
Std Dev	3.003

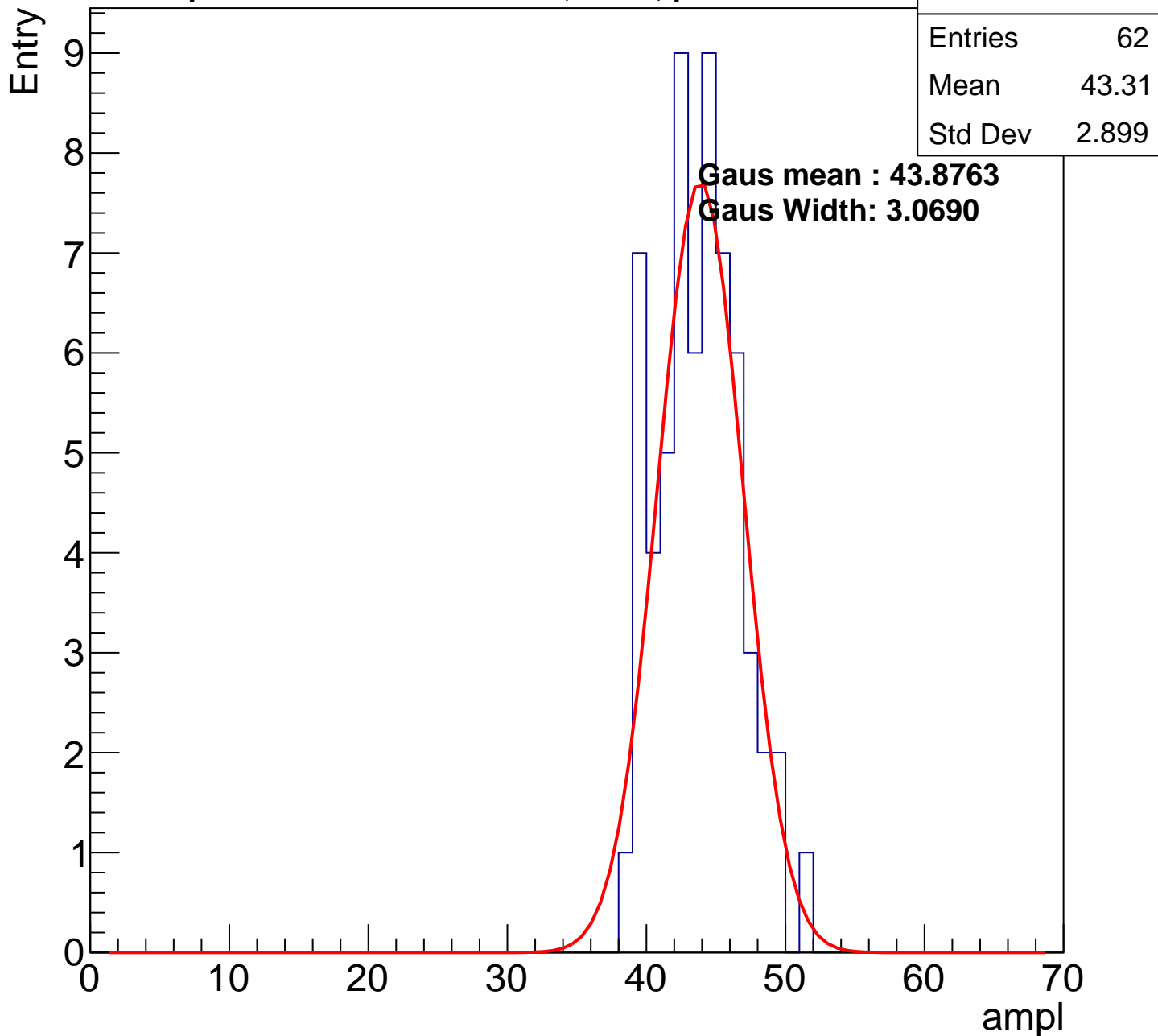
**Gaus mean : 37.8371**

**Gaus Width: 3.5173**



# B1L103S, U3-ch45, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

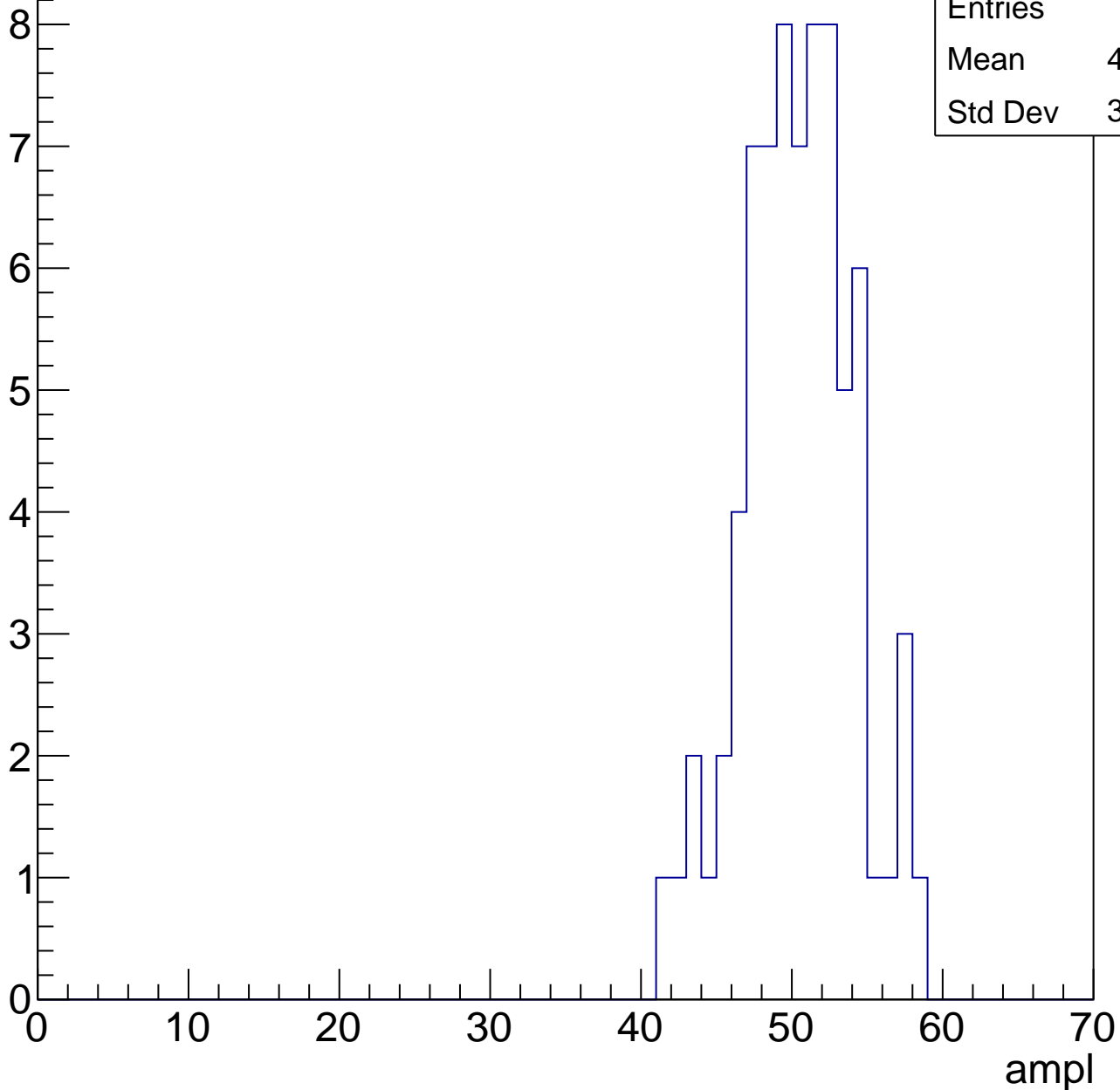


# B1L103S, U3-ch45, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	49.96
Std Dev	3.598

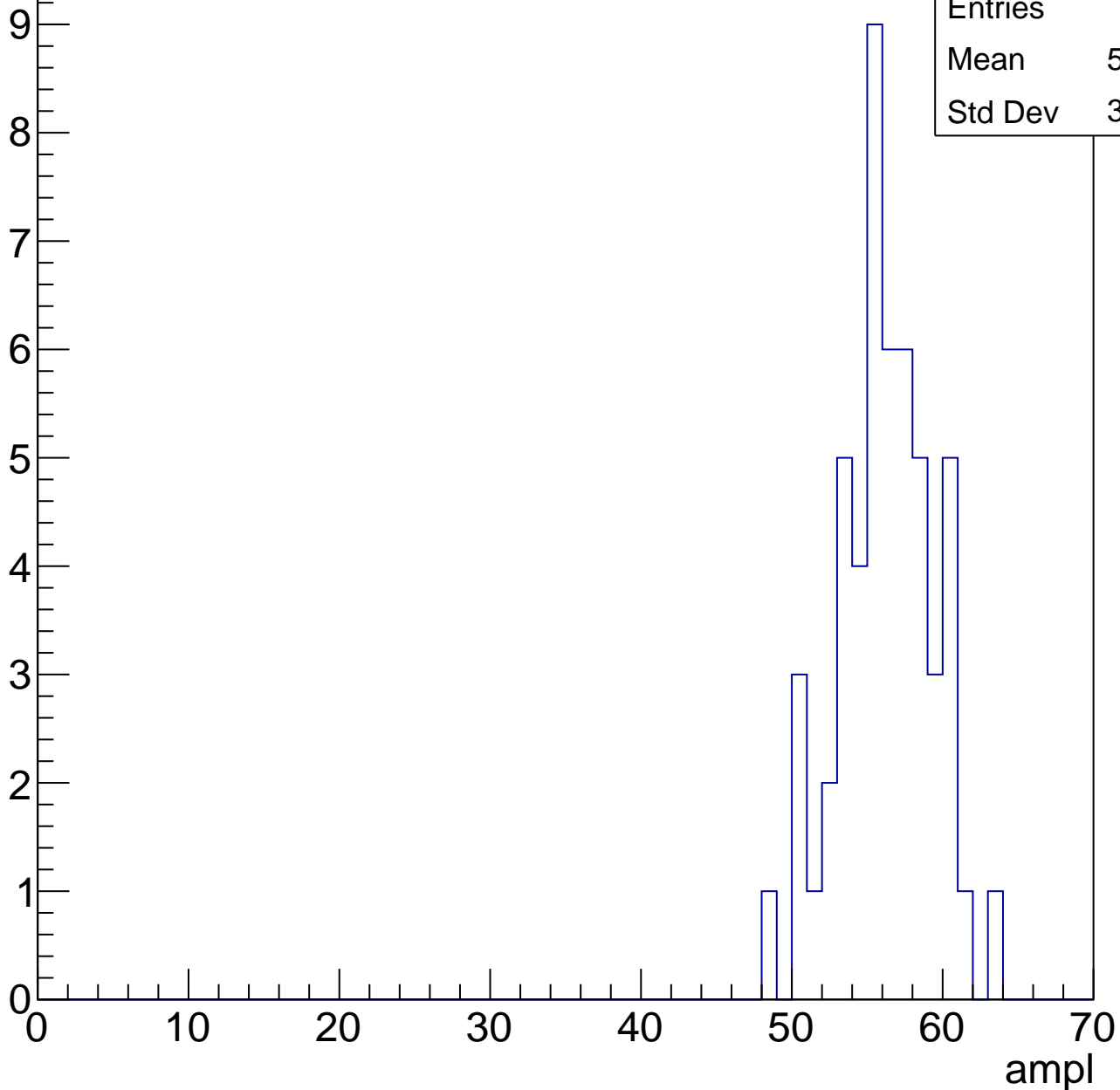


# B1L103S, U3-ch45, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	55.73
Std Dev	3.108

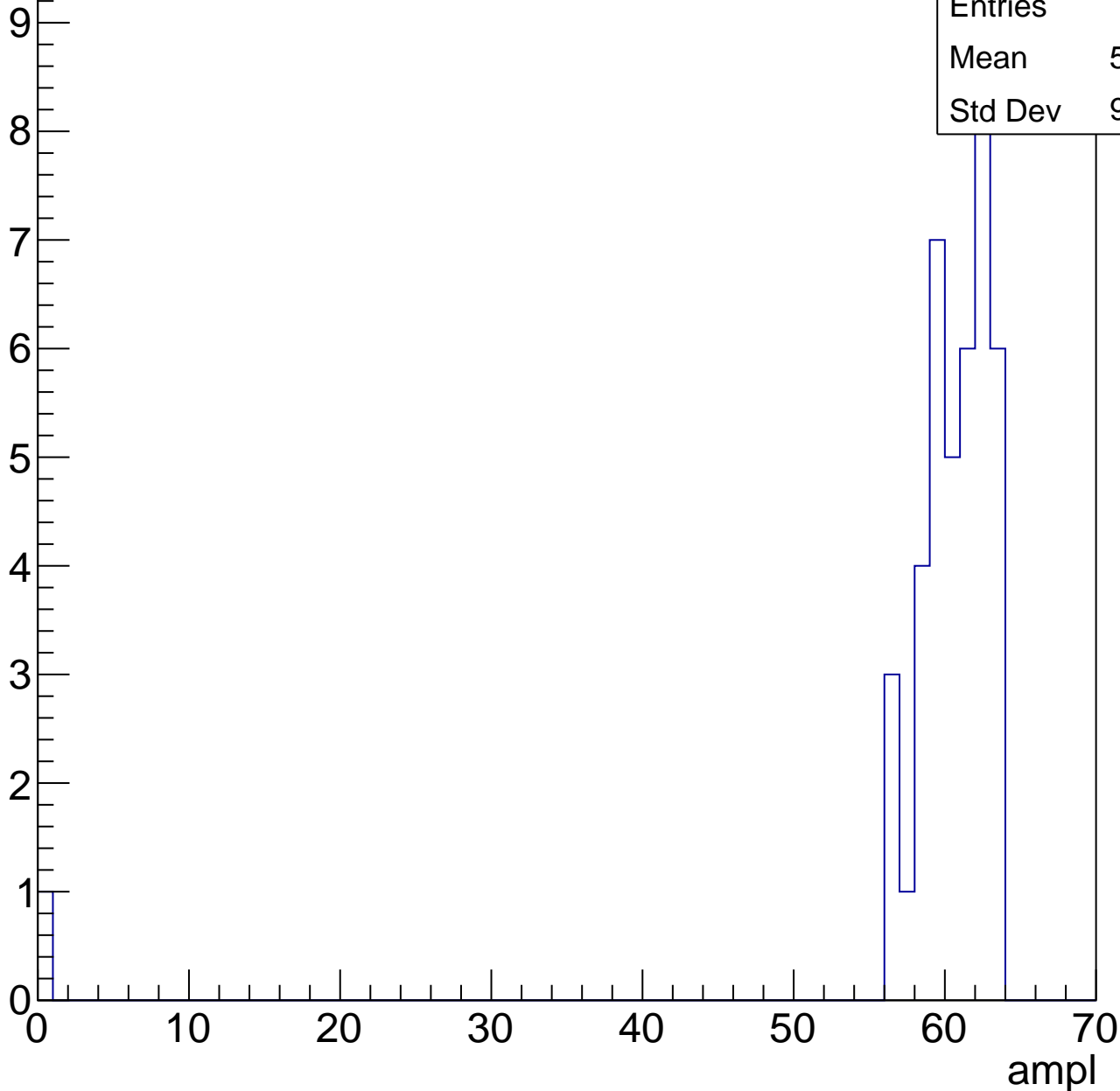


# B1L103S, U3-ch45, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

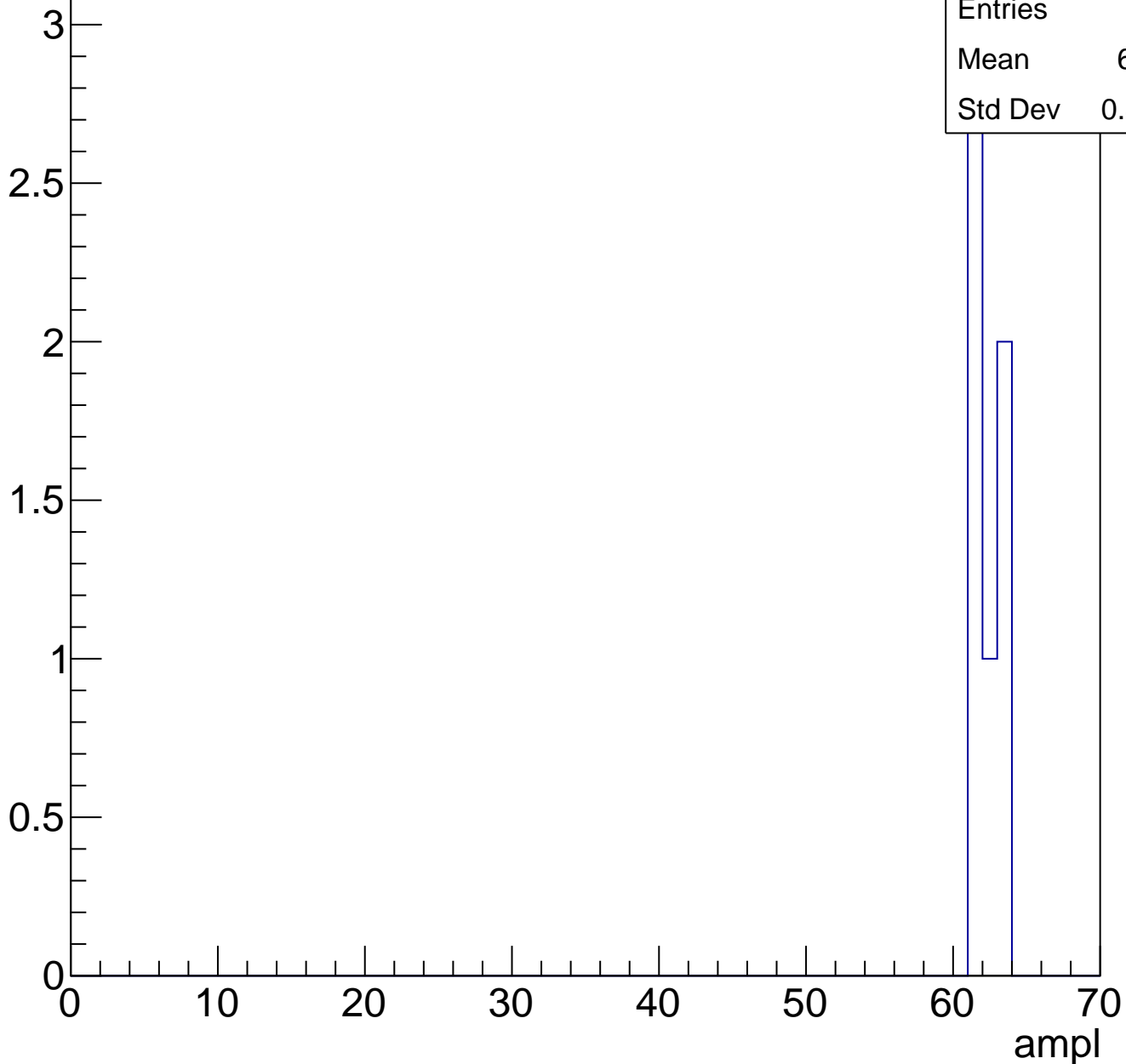
Entries	42
Mean	58.86
Std Dev	9.413



# B1L103S, U3-ch45, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U3-ch45, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch46, adc0

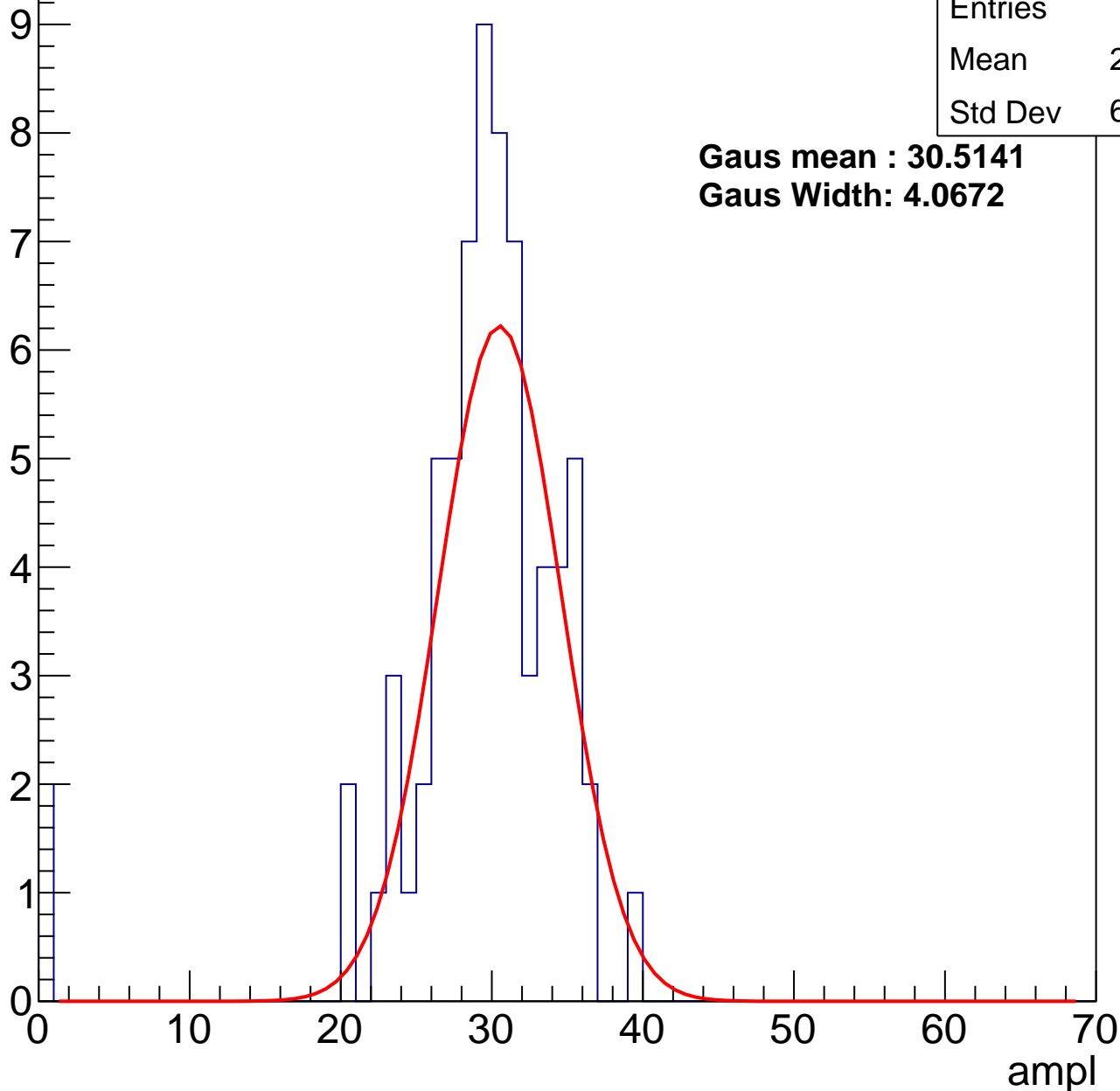
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	28.65
Std Dev	6.197

**Gaus mean : 30.5141**

**Gaus Width: 4.0672**



# B1L103S, U3-ch46, adc1

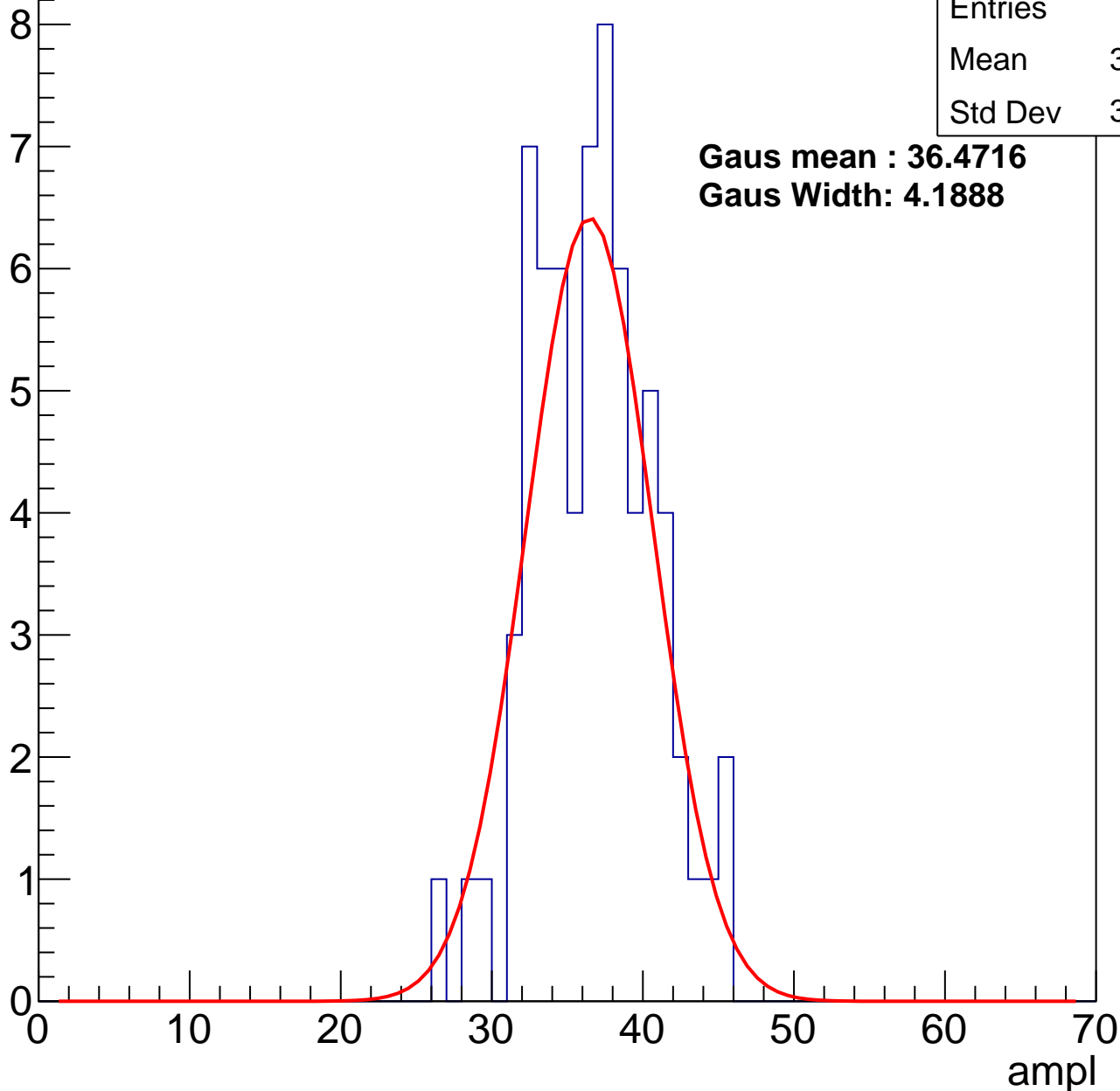
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	36.22
Std Dev	3.945

**Gaus mean : 36.4716**

**Gaus Width: 4.1888**



# B1L103S, U3-ch46, adc2

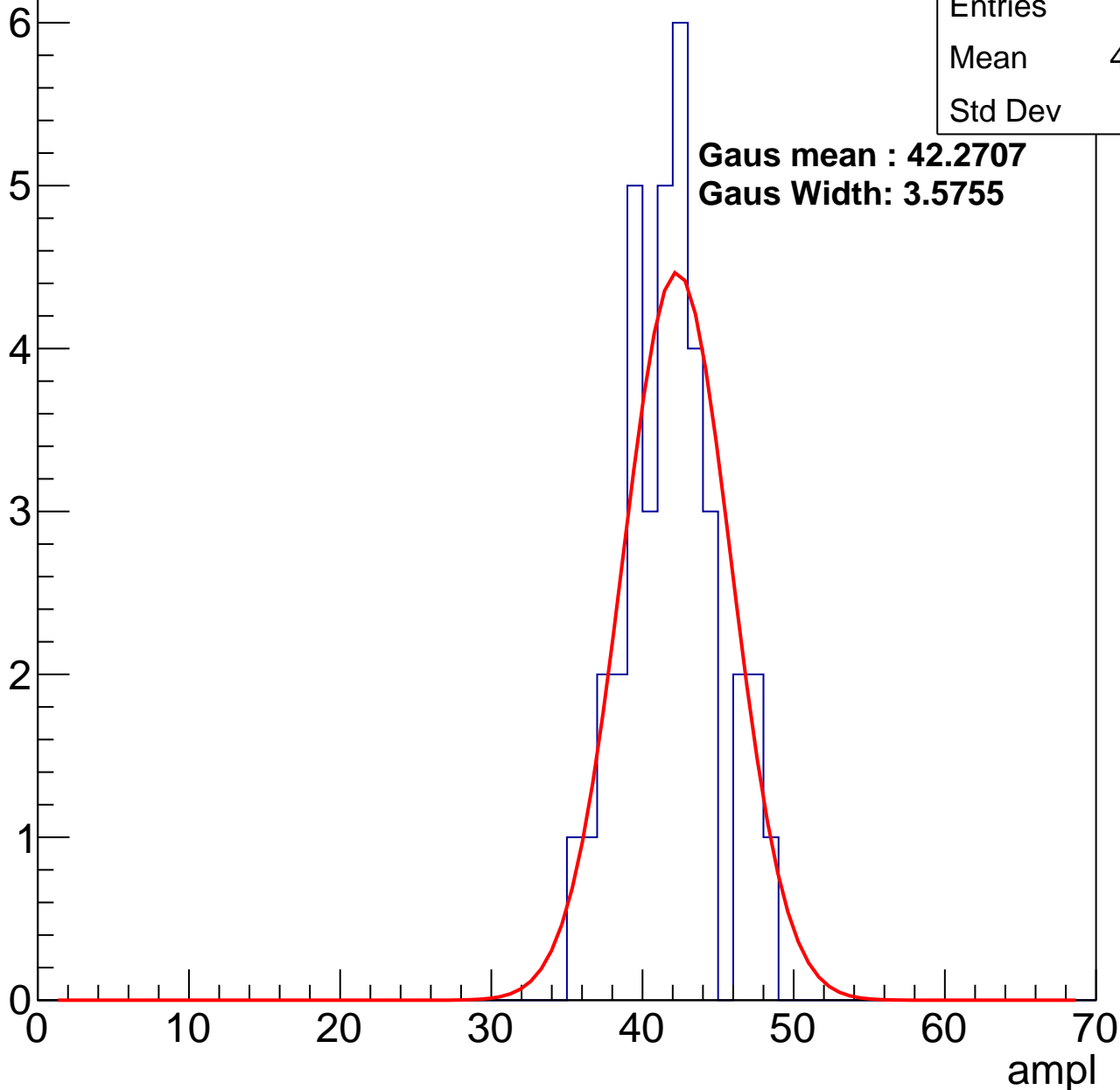
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	37
Mean	41.38
Std Dev	3.07

**Gaus mean : 42.2707**

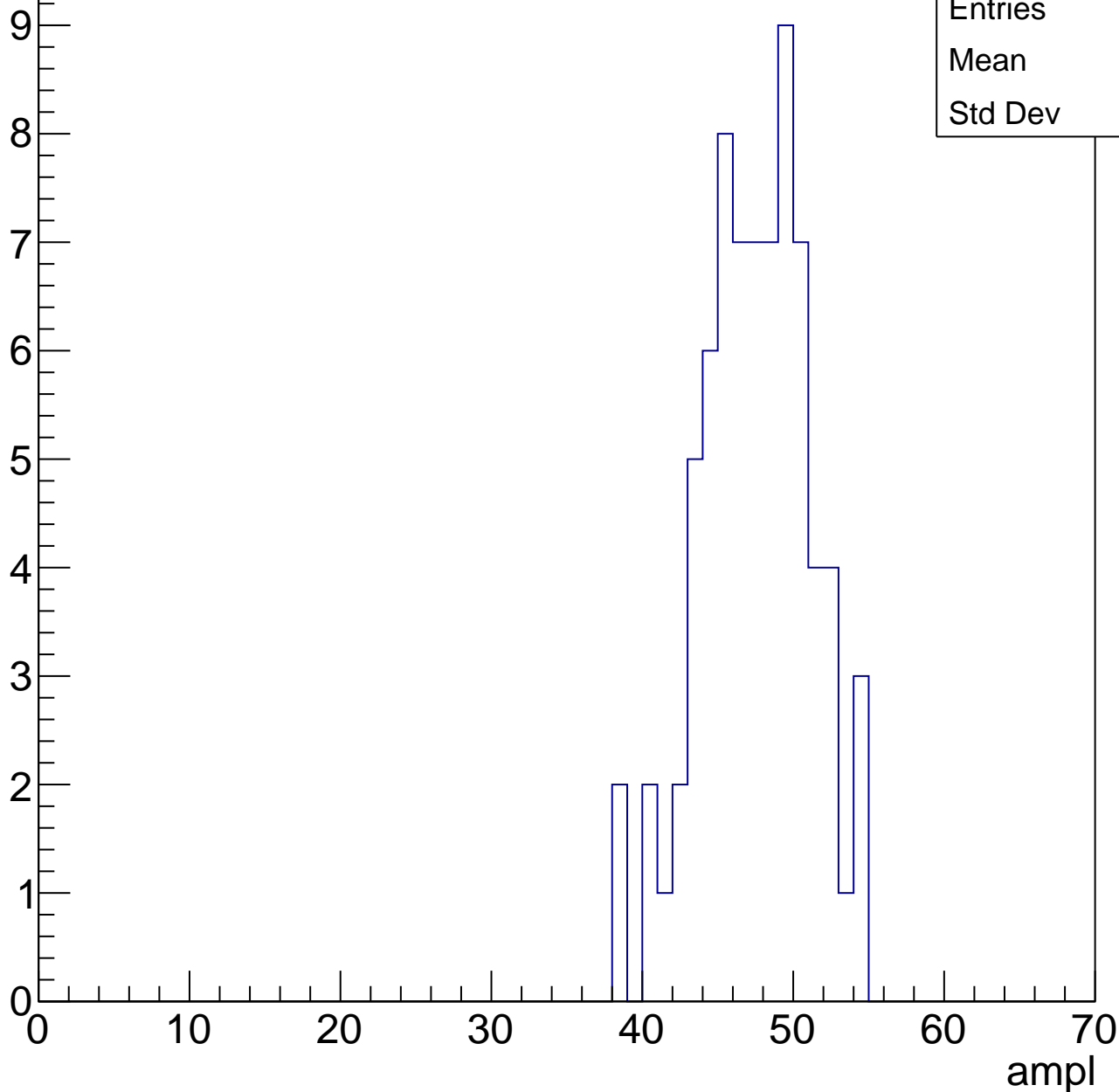
**Gaus Width: 3.5755**



# B1L103S, U3-ch46, adc3

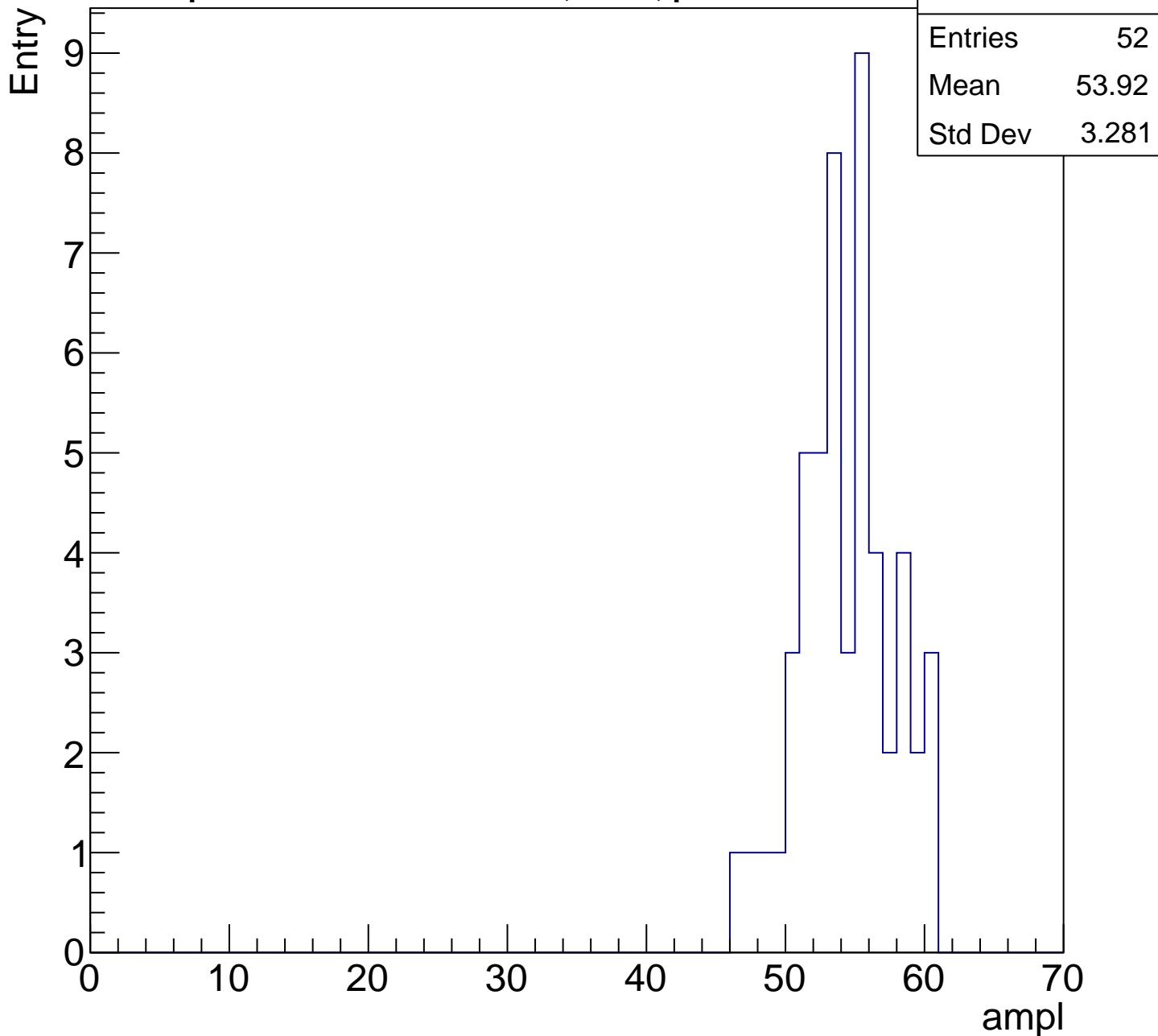
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



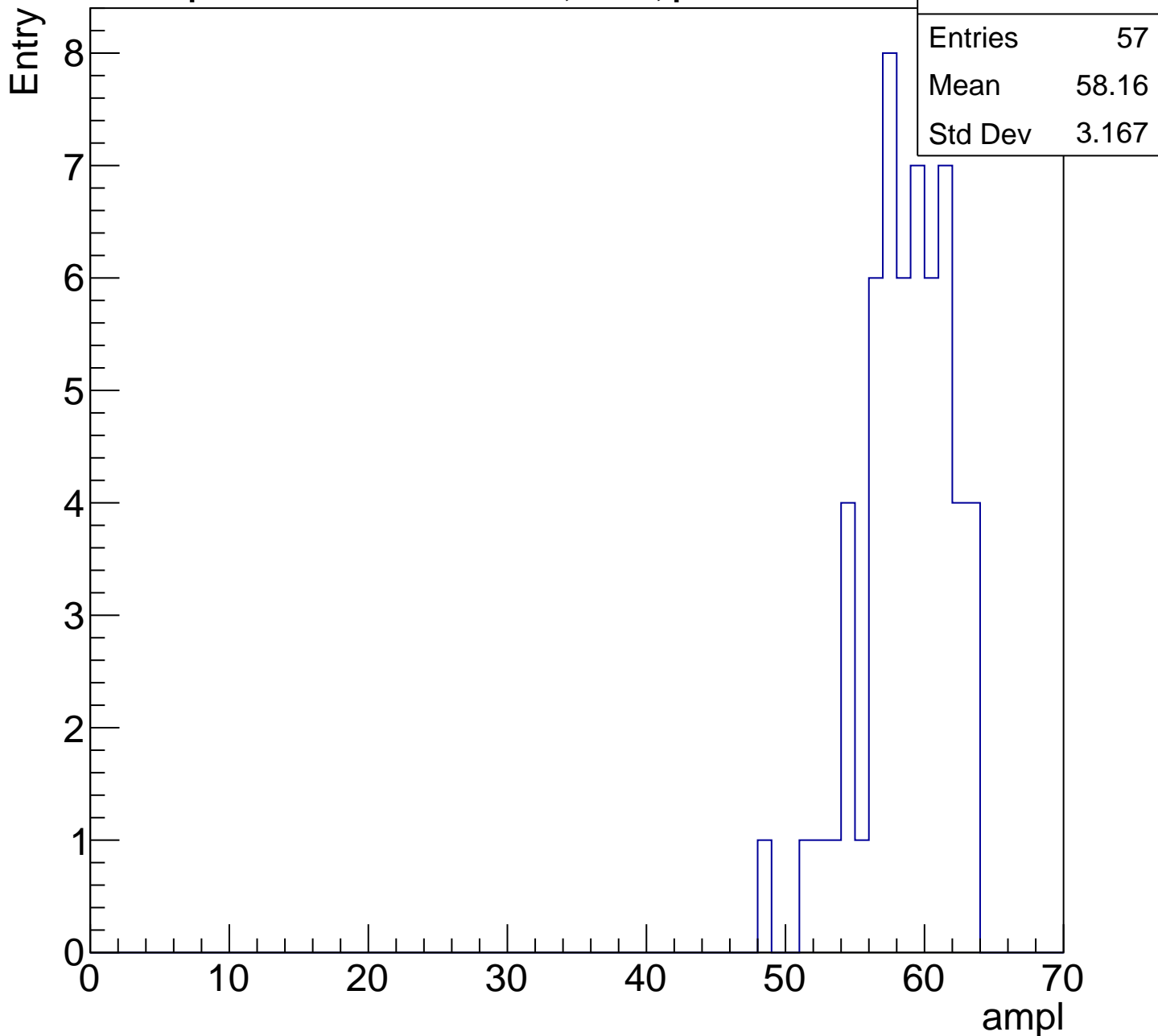
# B1L103S, U3-ch46, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U3-ch46, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

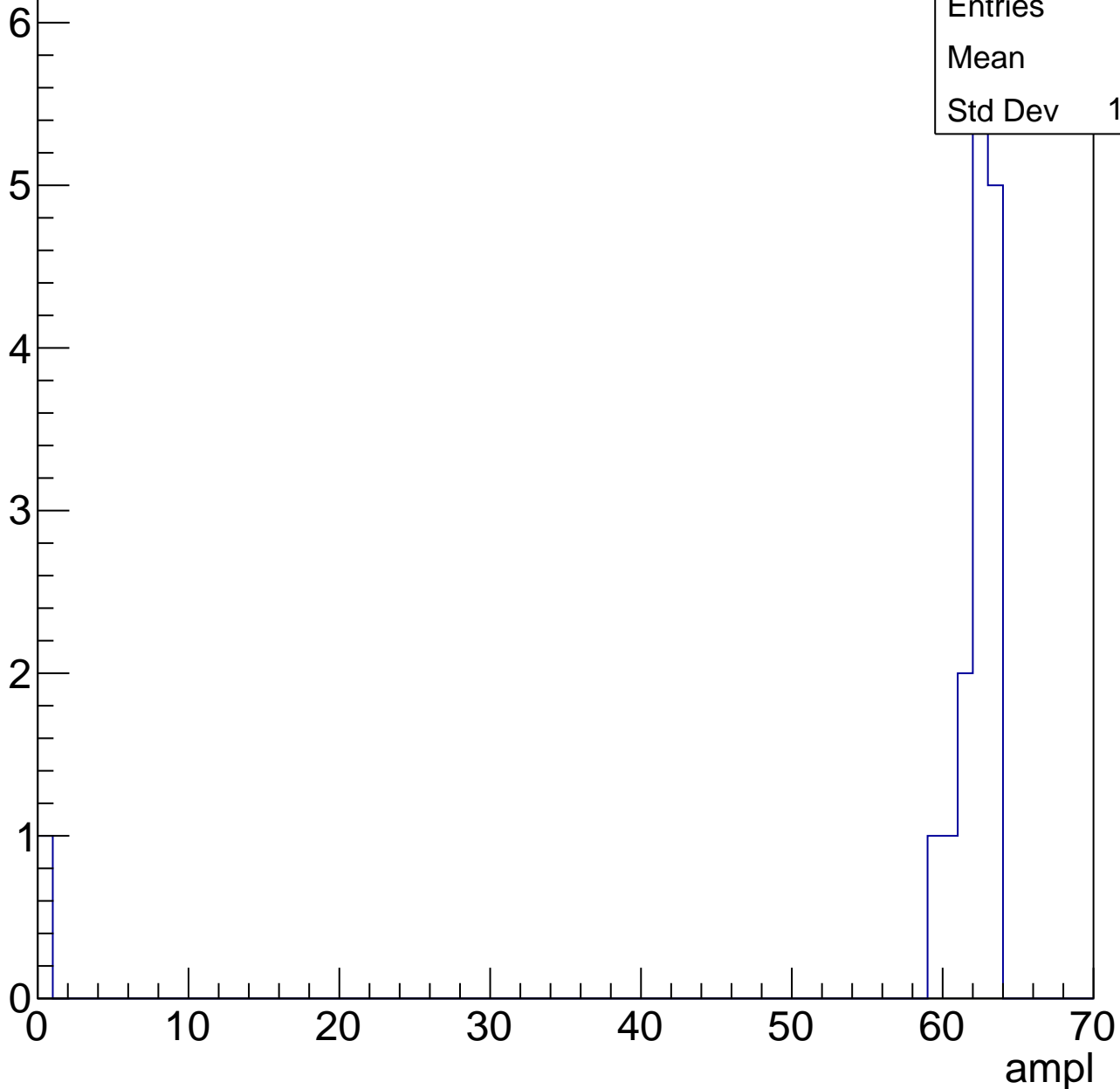


# B1L103S, U3-ch46, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	16
Mean	58
Std Dev	15.02

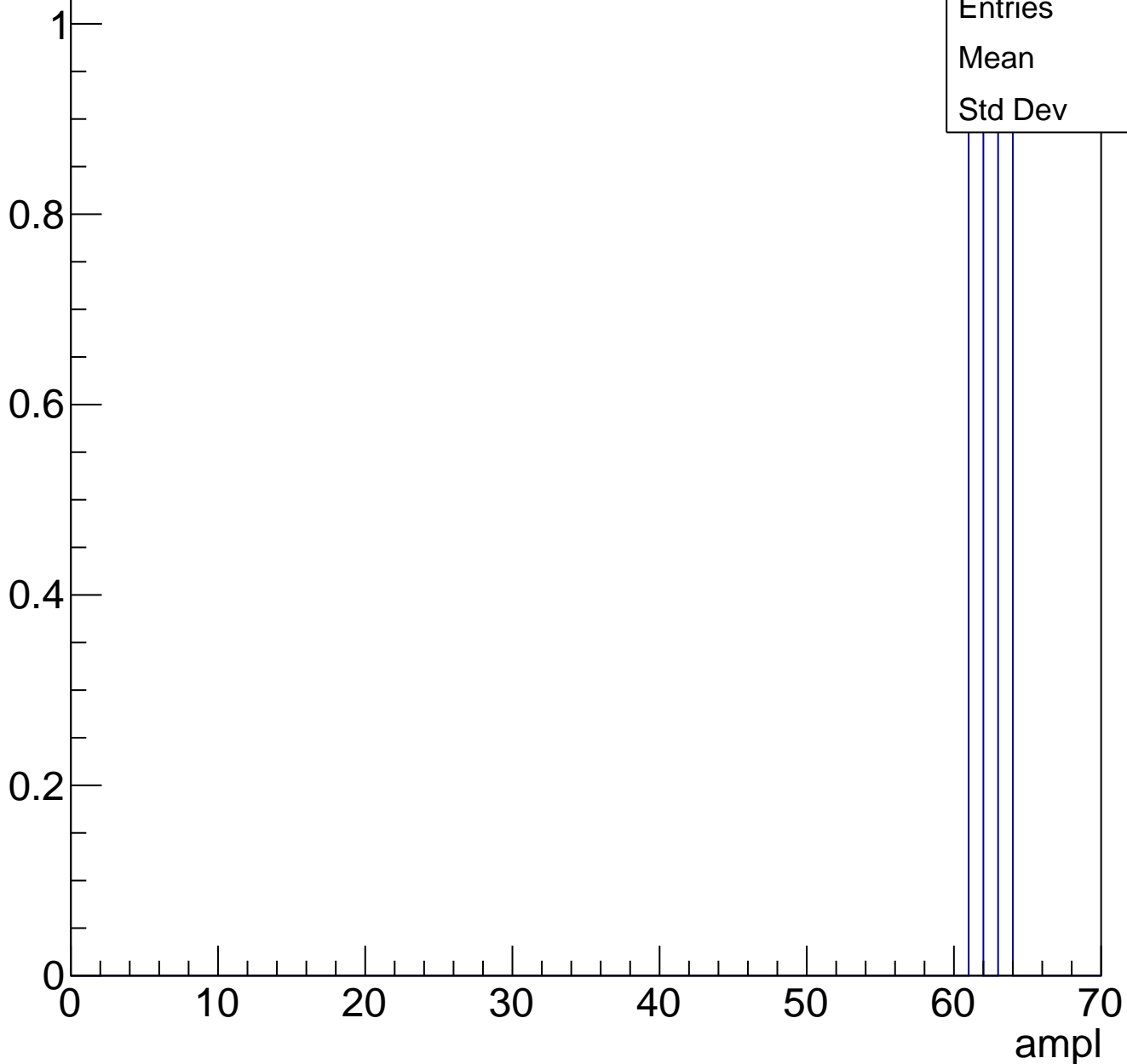




# B1L103S, U3-ch46, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch47, adc0

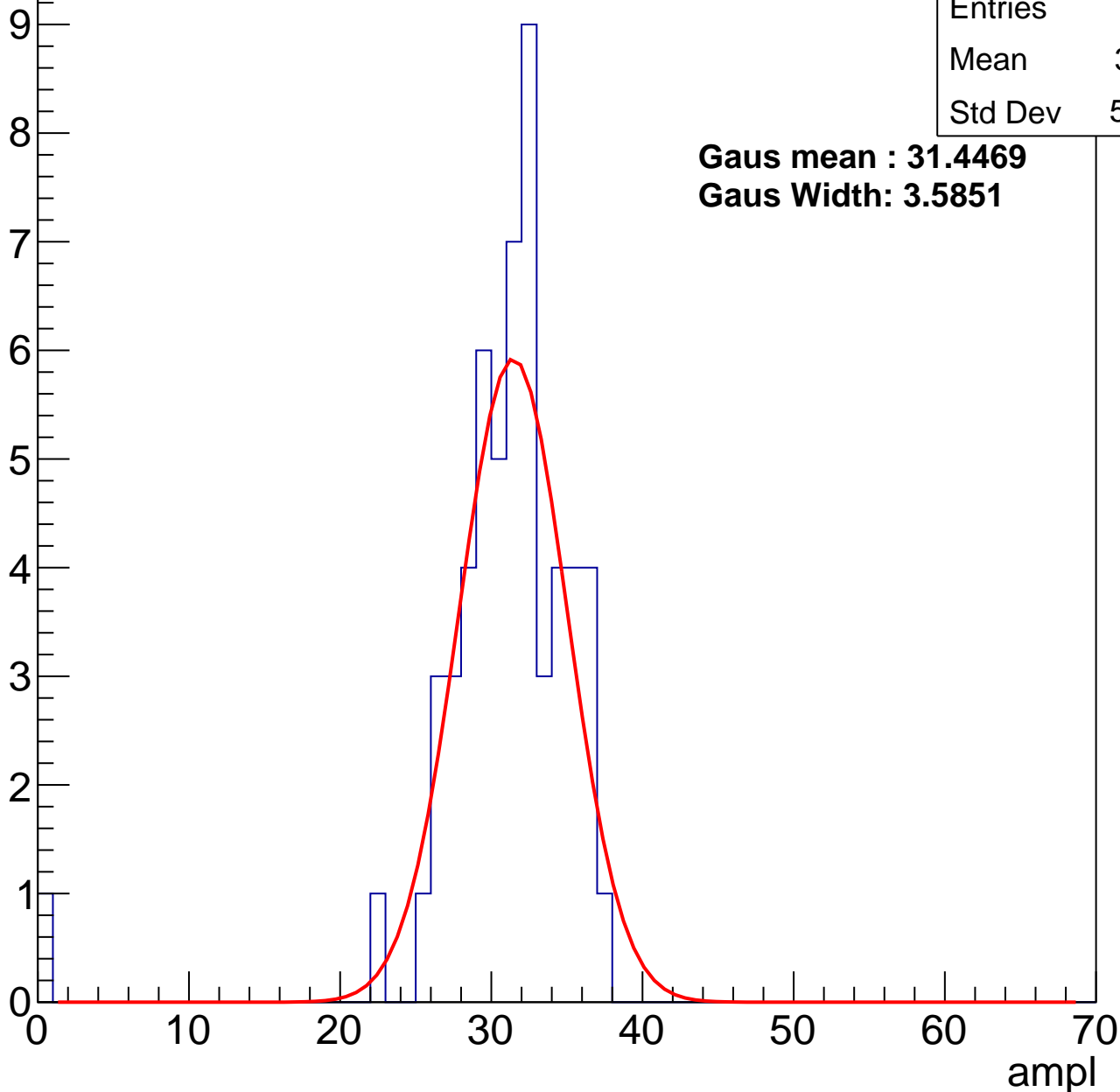
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	30.41
Std Dev	5.182

**Gaus mean : 31.4469**

**Gaus Width: 3.5851**



# B1L103S, U3-ch47, adc1

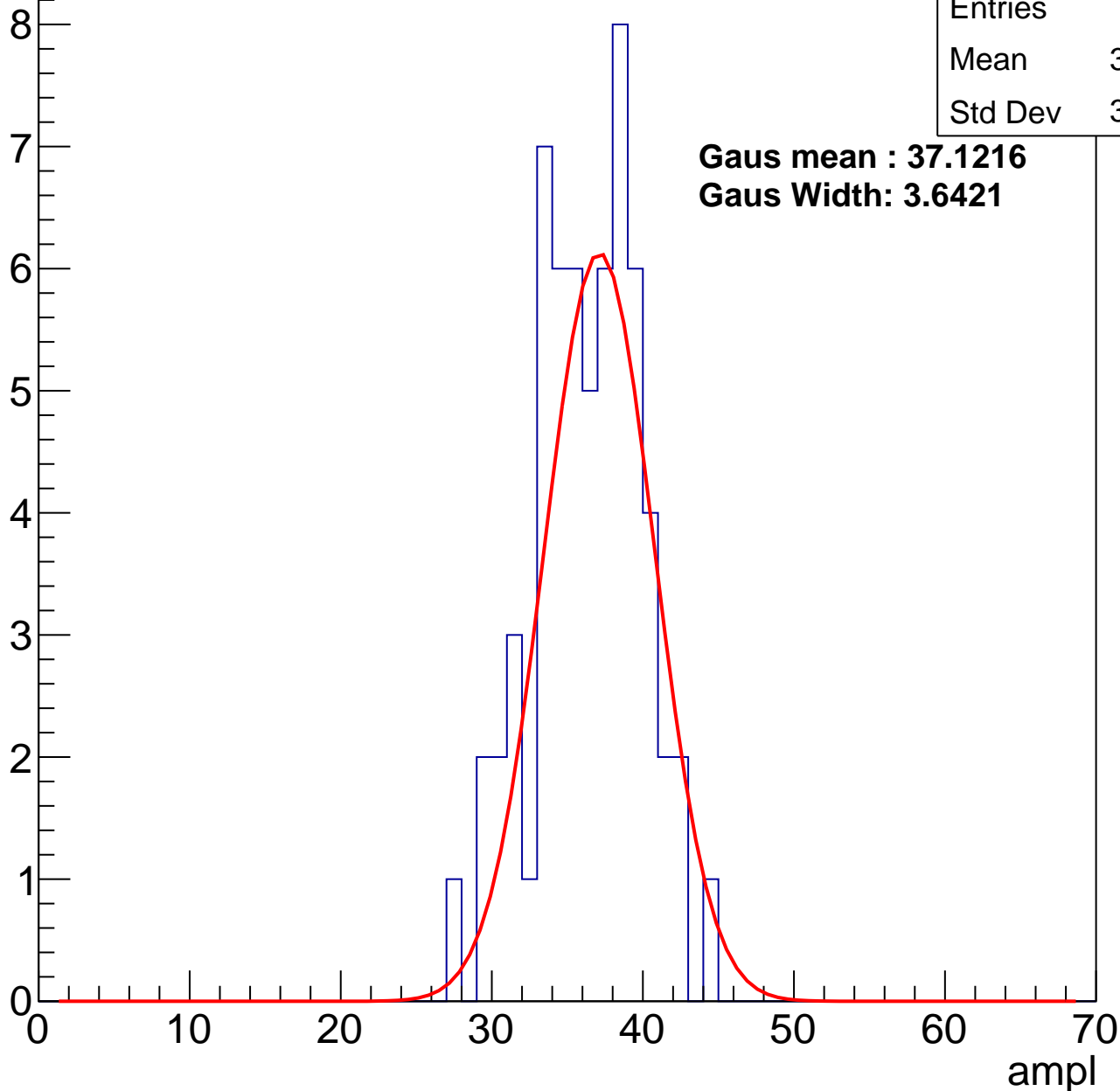
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	35.89
Std Dev	3.538

**Gaus mean : 37.1216**

**Gaus Width: 3.6421**



# B1L103S, U3-ch47, adc2

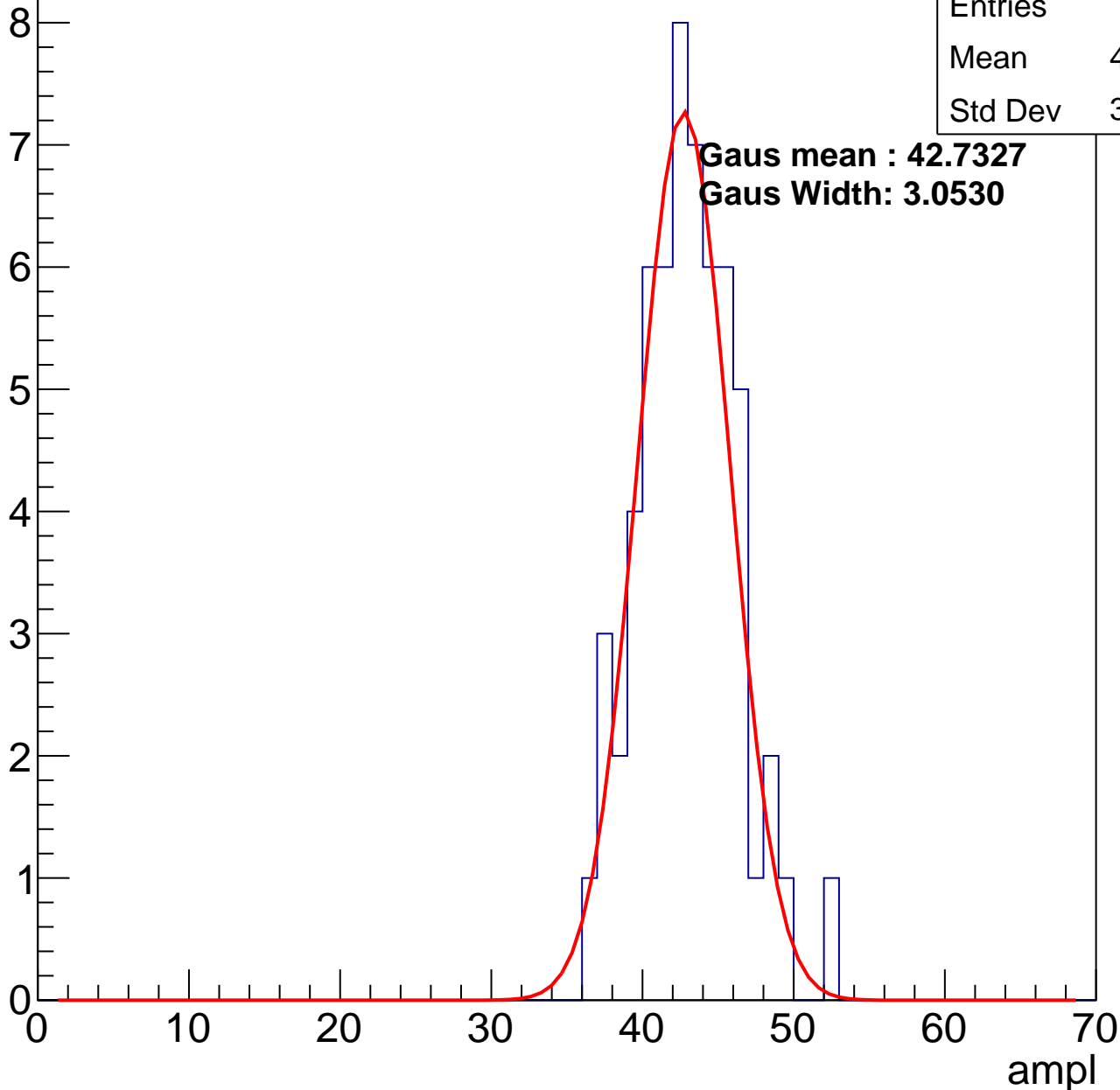
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	42.54
Std Dev	3.196

**Gaus mean : 42.7327**

**Gaus Width: 3.0530**

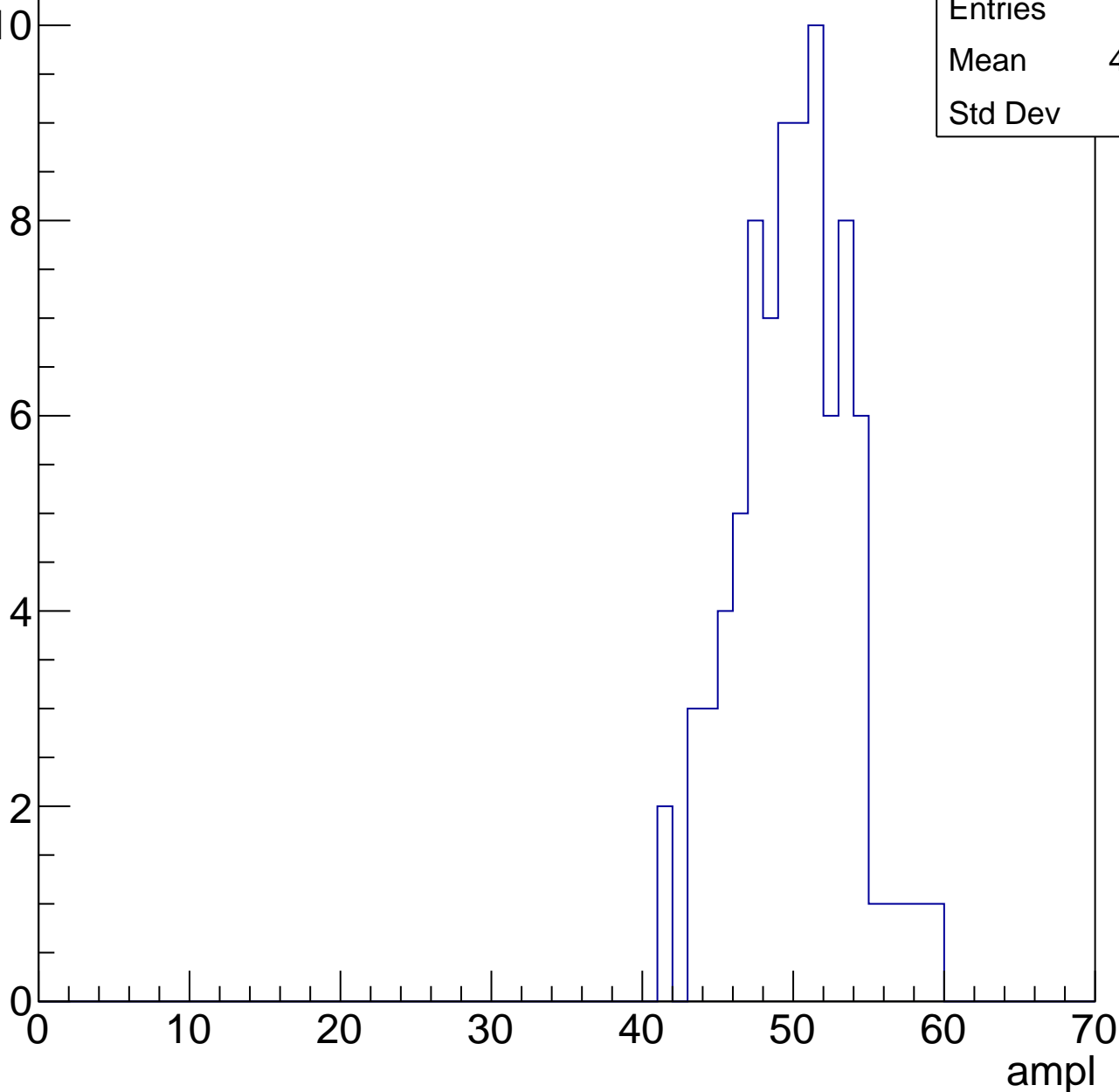


# B1L103S, U3-ch47, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	85
Mean	49.54
Std Dev	3.67

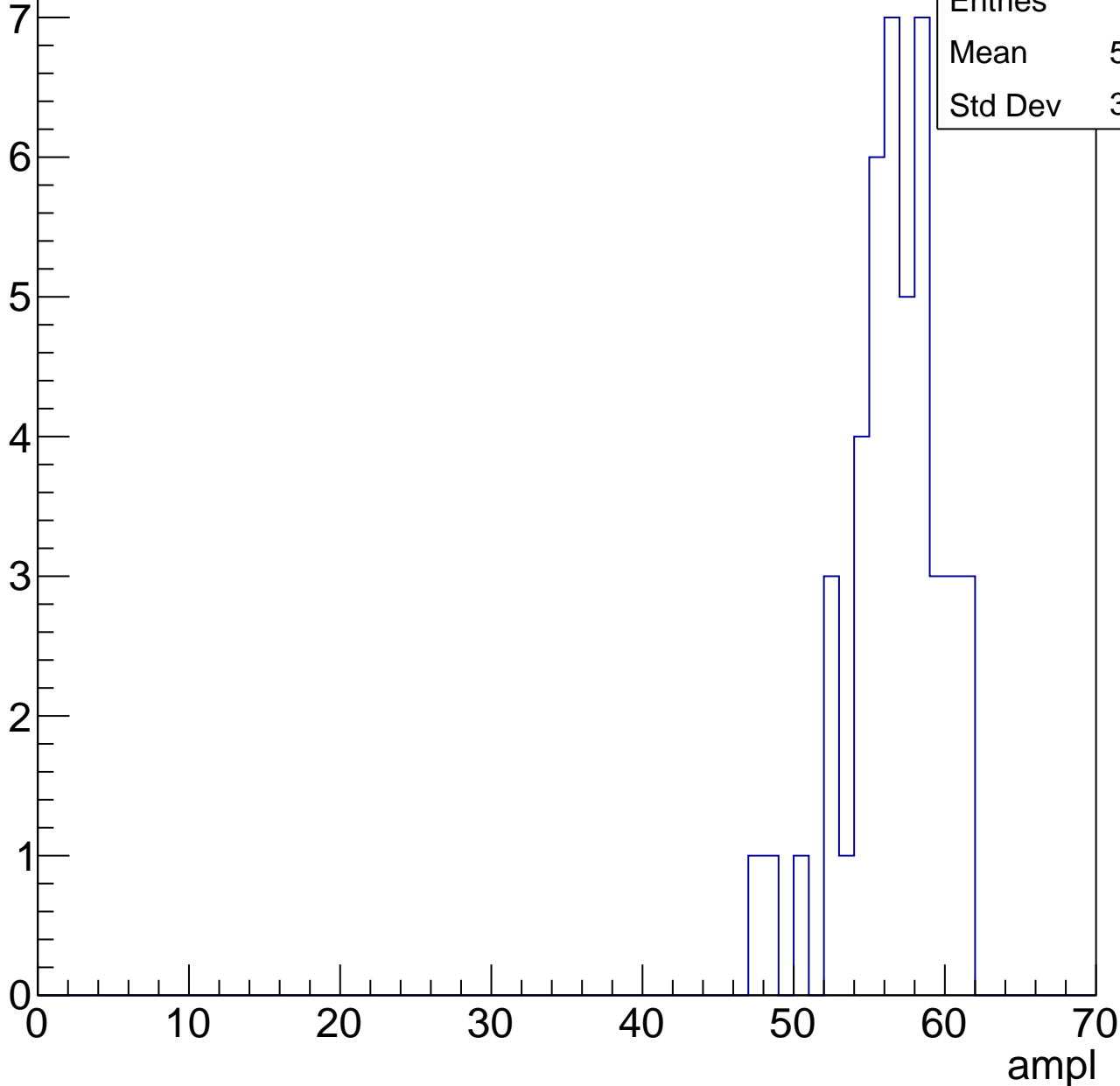


# B1L103S, U3-ch47, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	45
Mean	56.07
Std Dev	3.137



# B1L103S, U3-ch47, adc5

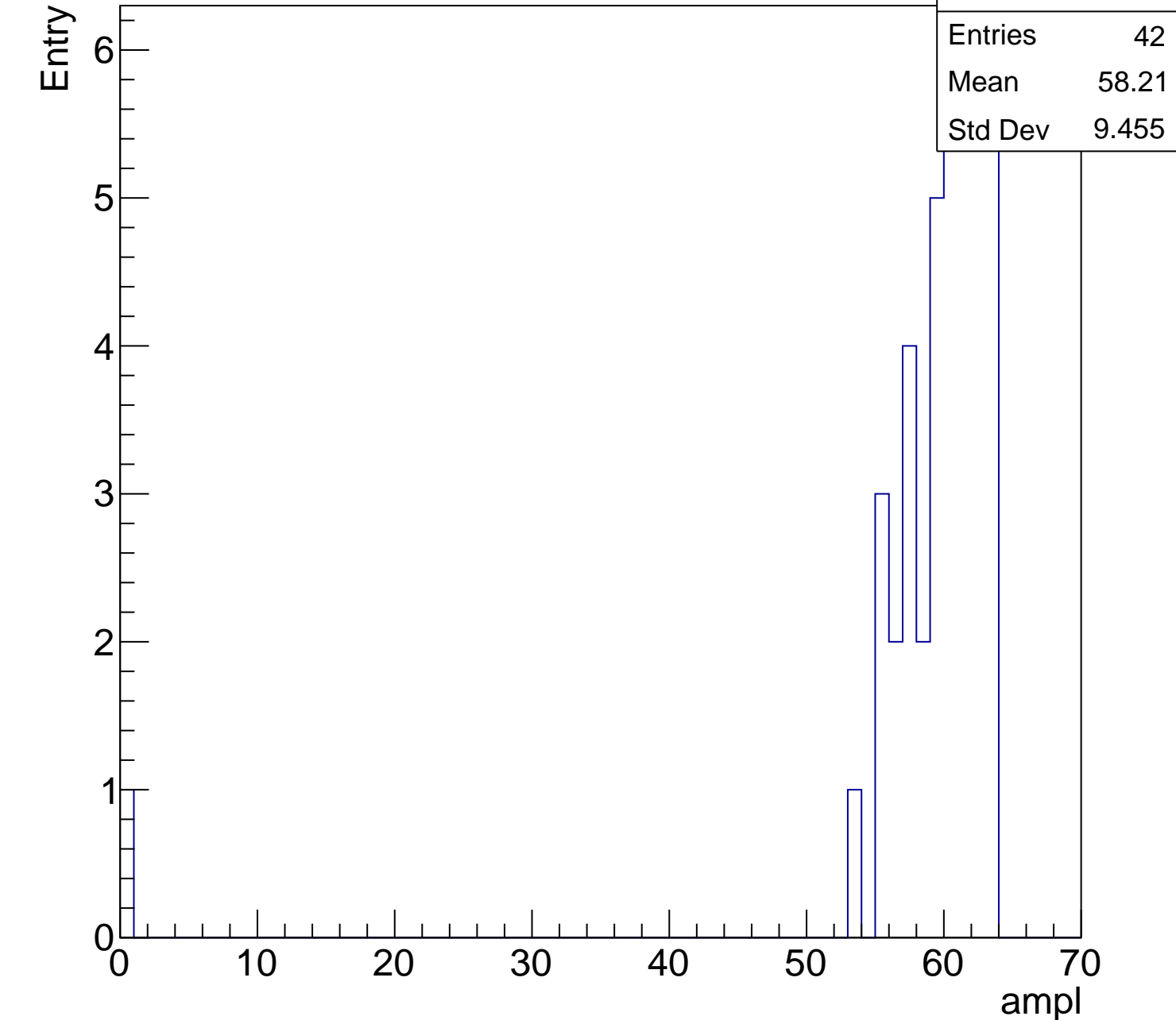
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

6  
5  
4  
3  
2  
1  
0

Entries	42
Mean	58.21
Std Dev	9.455

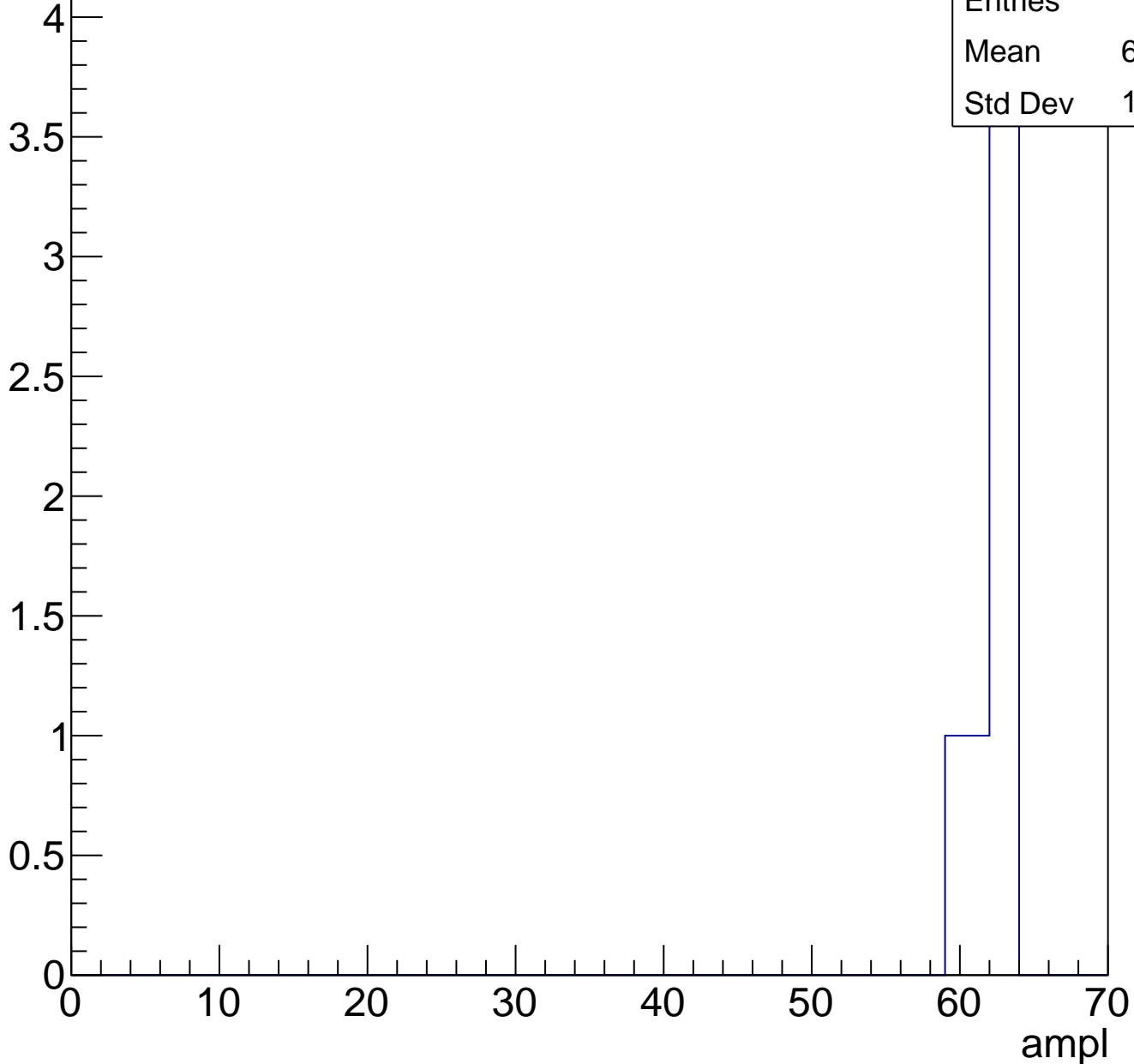
ampl



# B1L103S, U3-ch47, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U3-ch47, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U3-ch48, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	77
Mean	28.04
Std Dev	4.945

**Gaus mean : 29.0494**

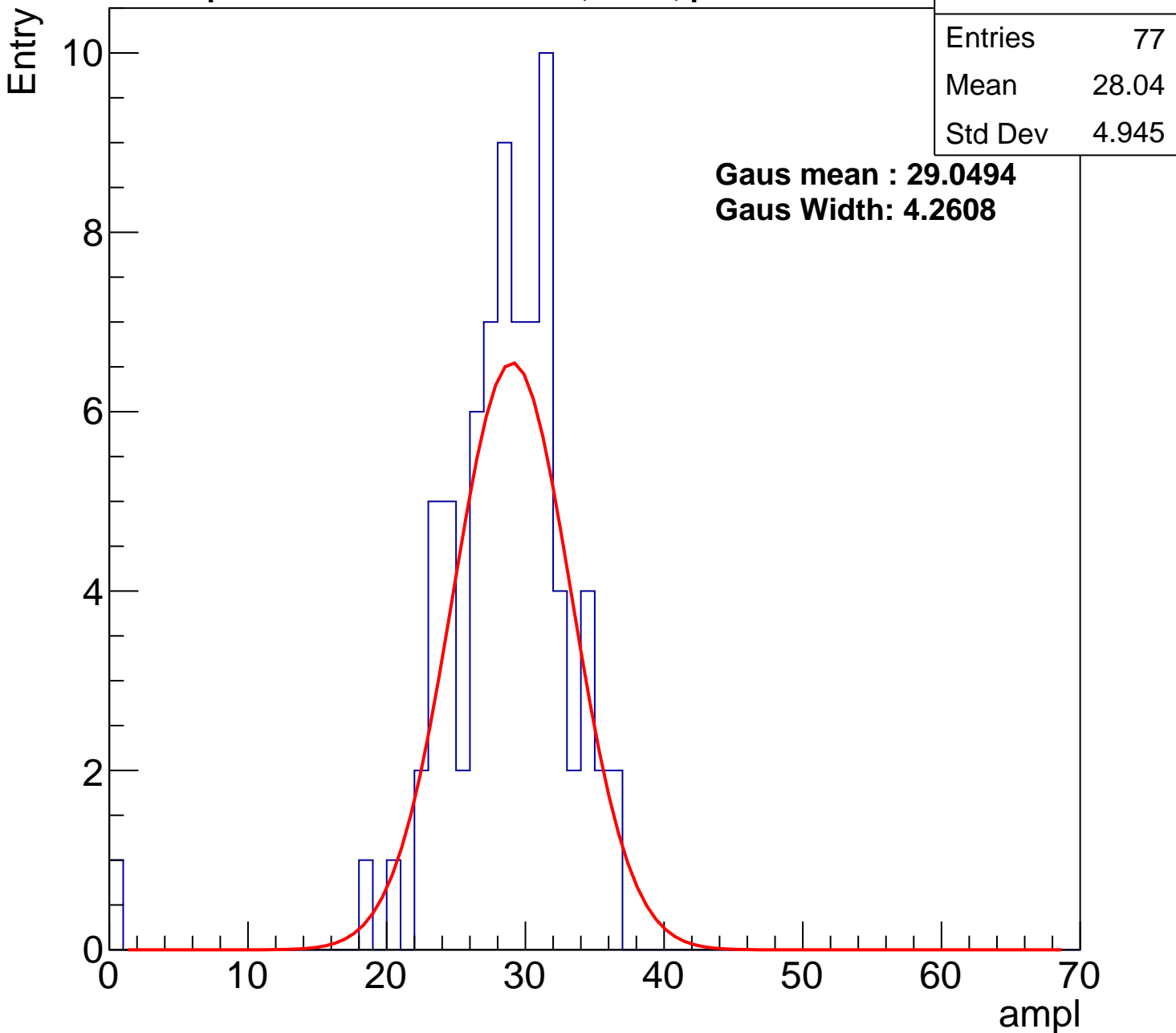
**Gaus Width: 4.2608**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U3-ch48, adc1

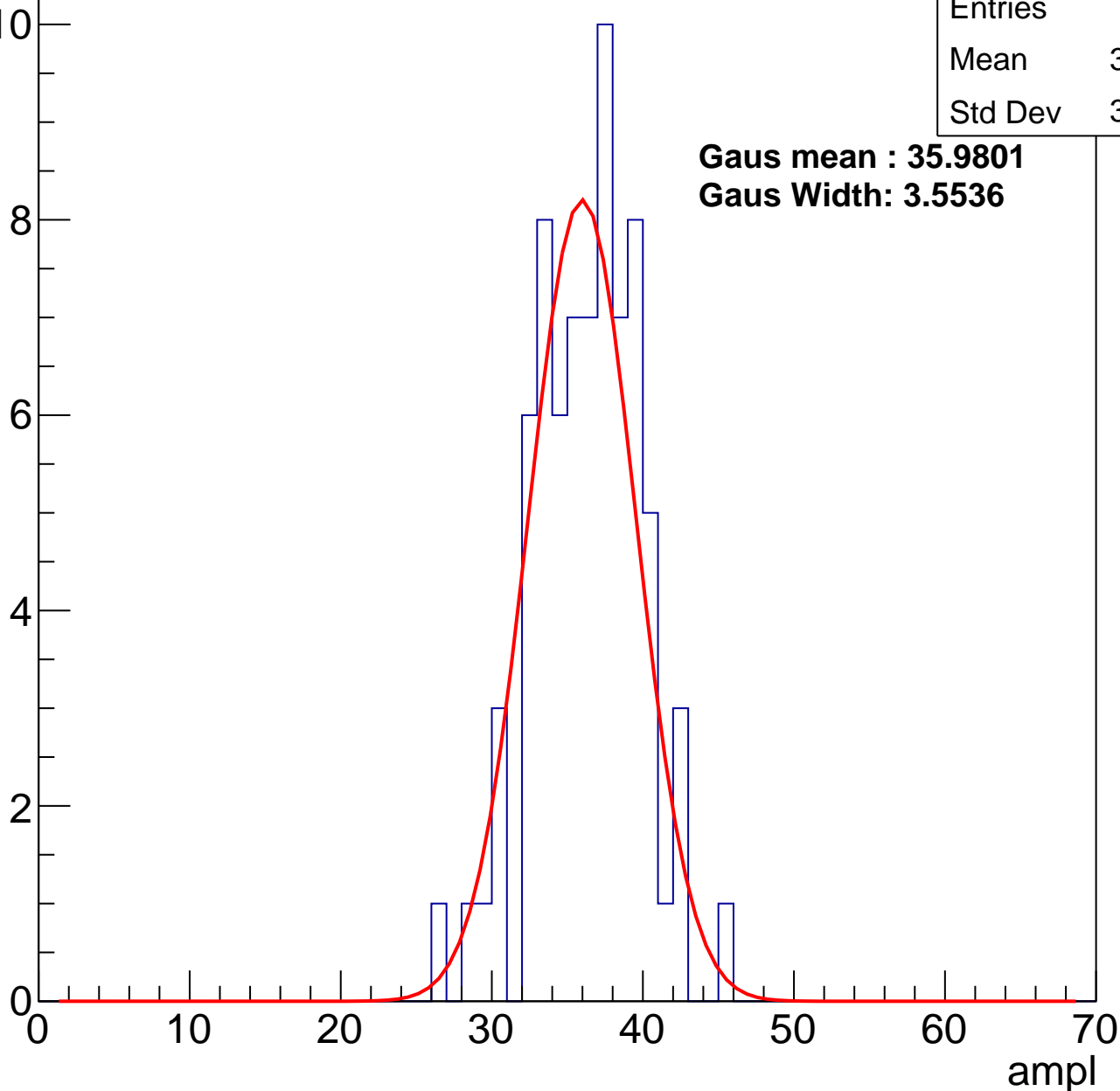
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	35.87
Std Dev	3.507

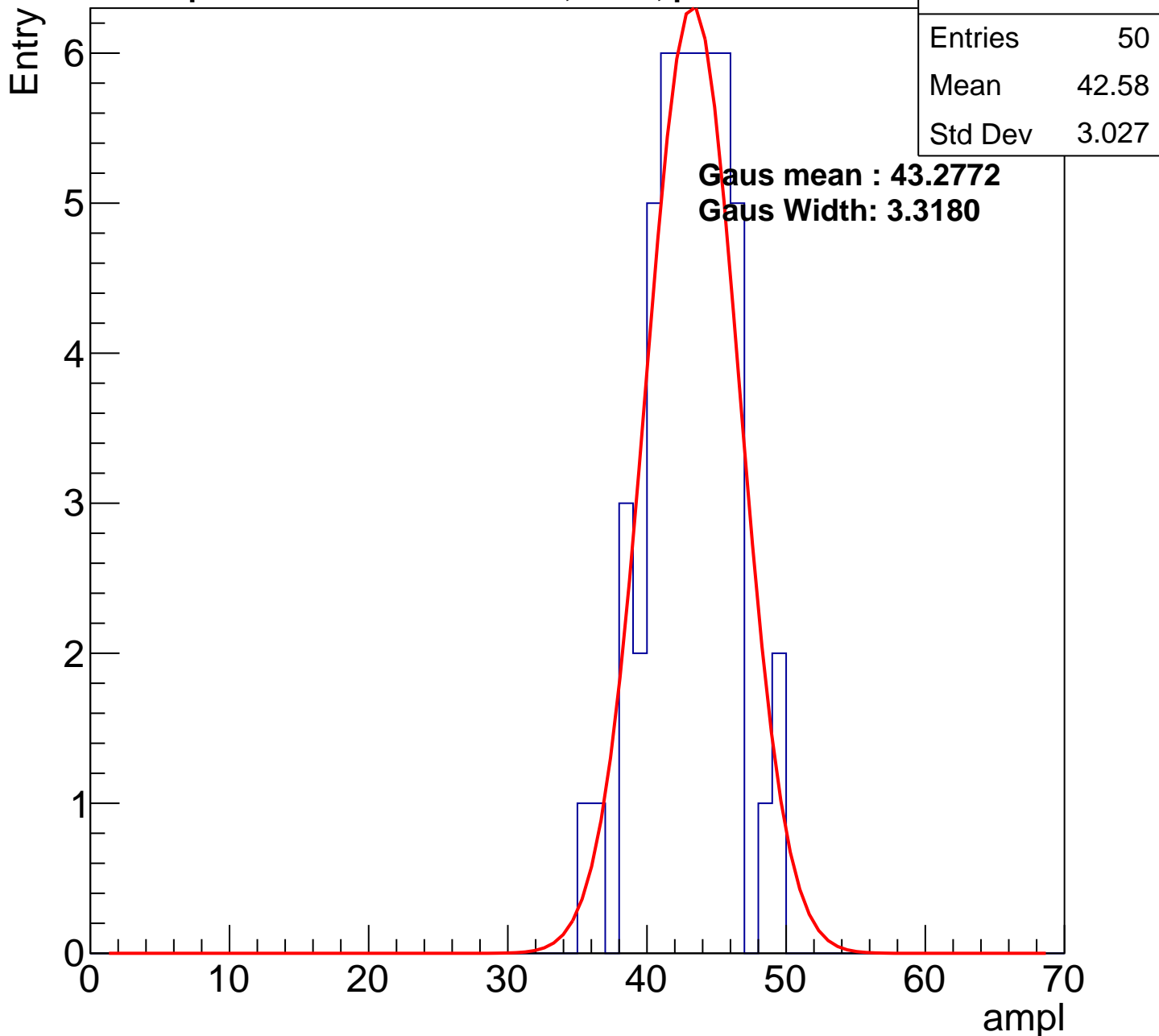
**Gaus mean : 35.9801**

**Gaus Width: 3.5536**



# B1L103S, U3-ch48, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

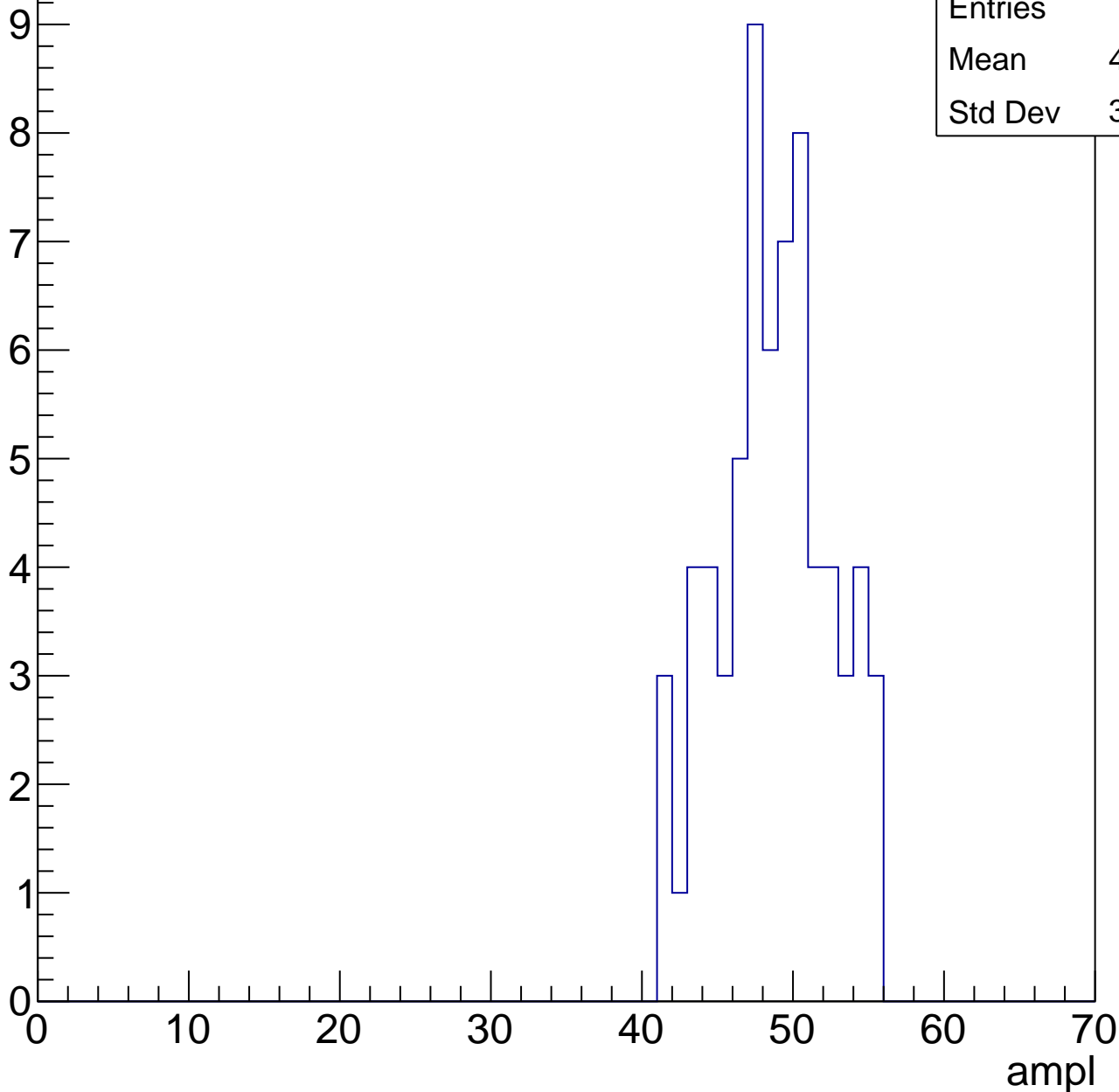


# B1L103S, U3-ch48, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

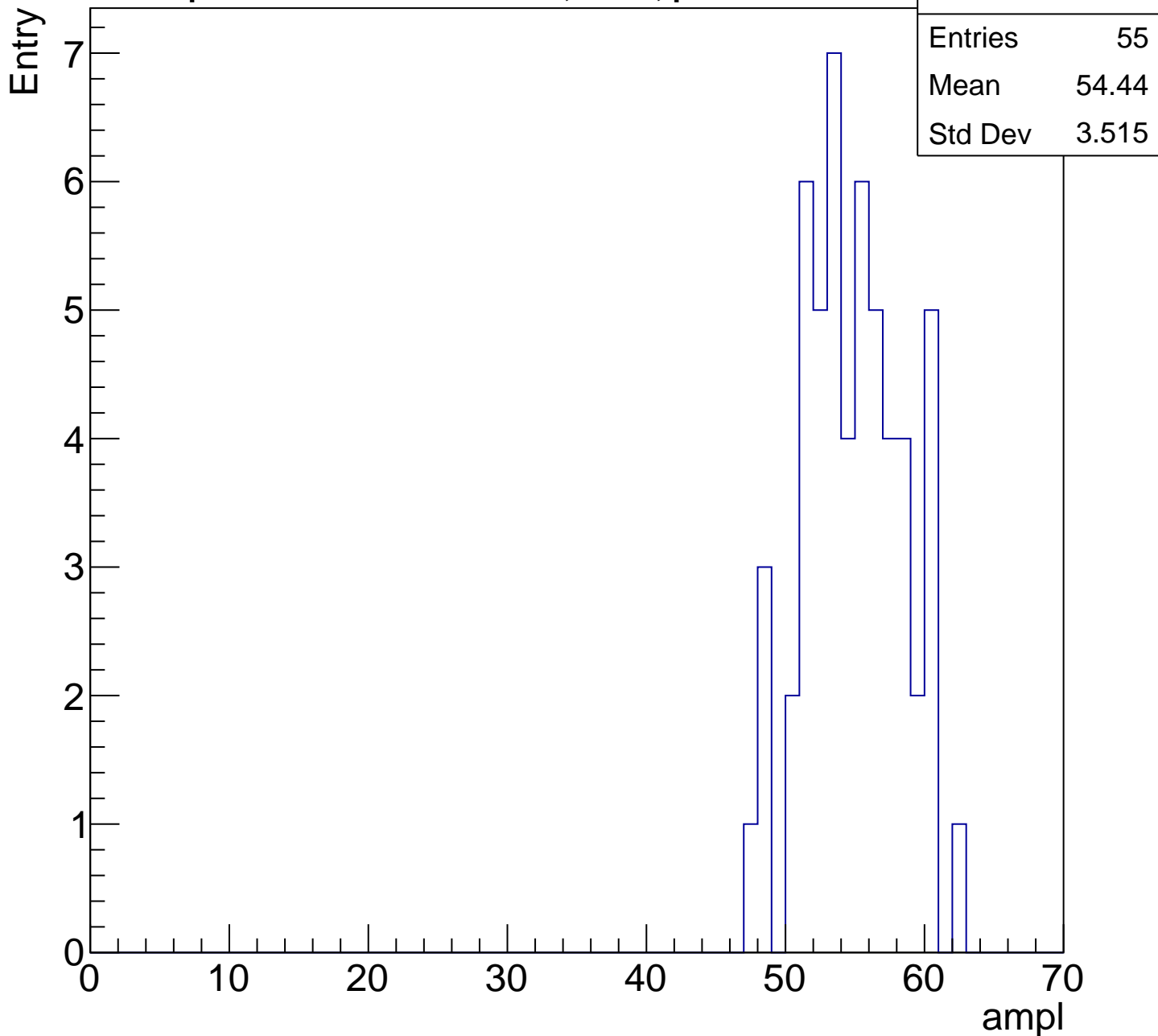
Entry

Entries	68
Mean	48.29
Std Dev	3.642



# B1L103S, U3-ch48, adc4

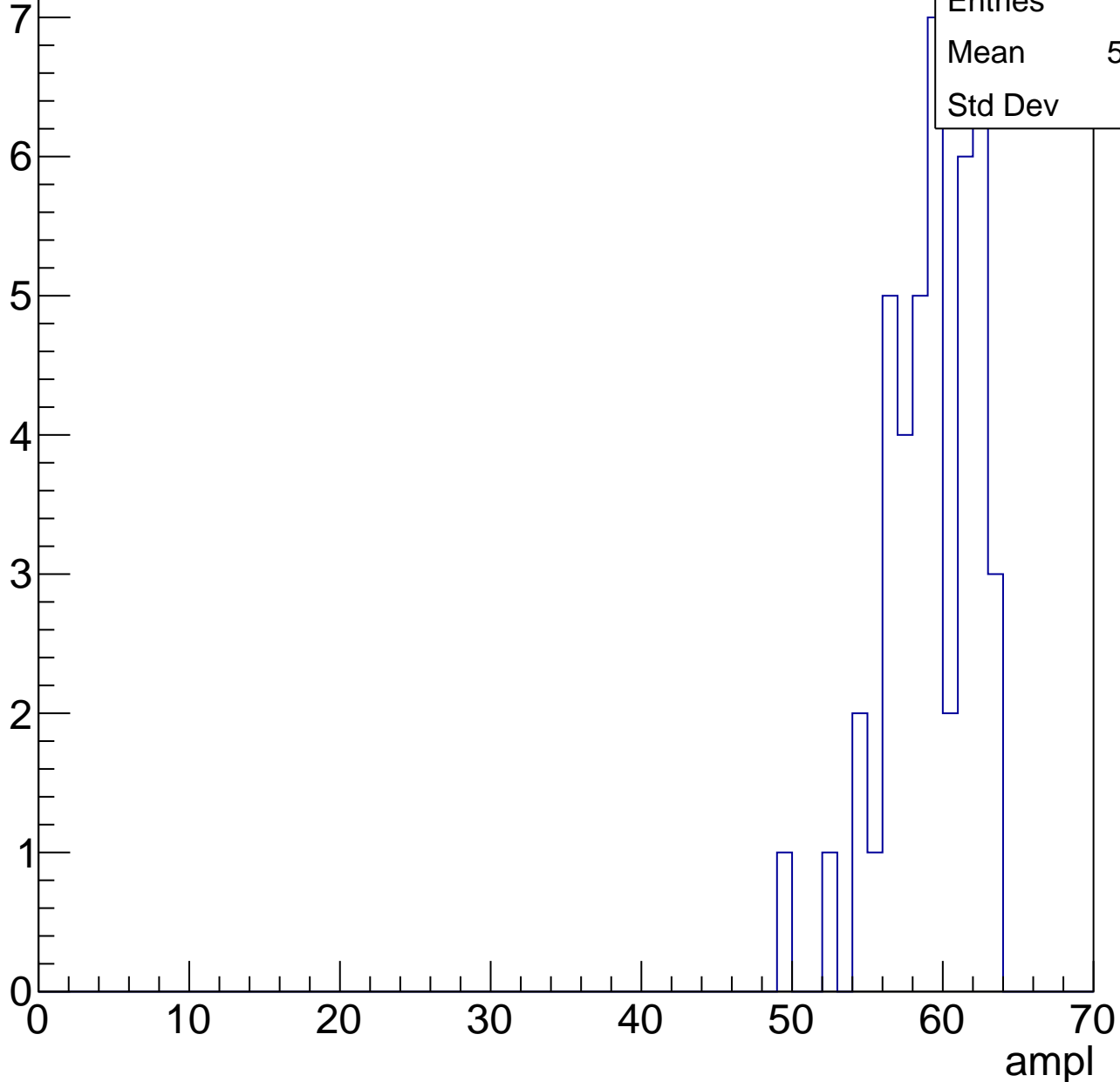
calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U3-ch48, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

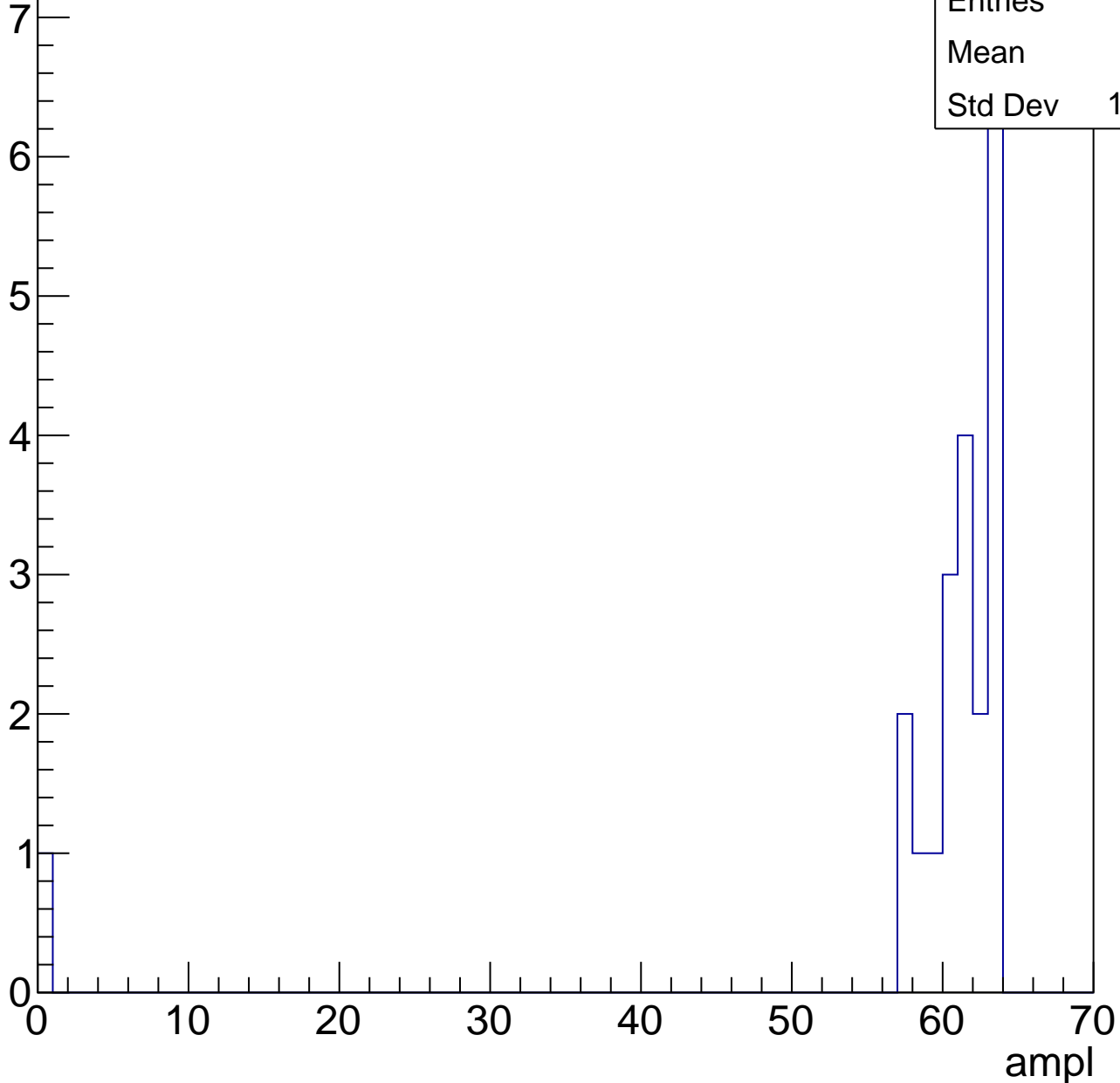


# B1L103S, U3-ch48, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	21
Mean	58.1
Std Dev	13.13





# B1L103S, U3-ch48, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch49, adc0

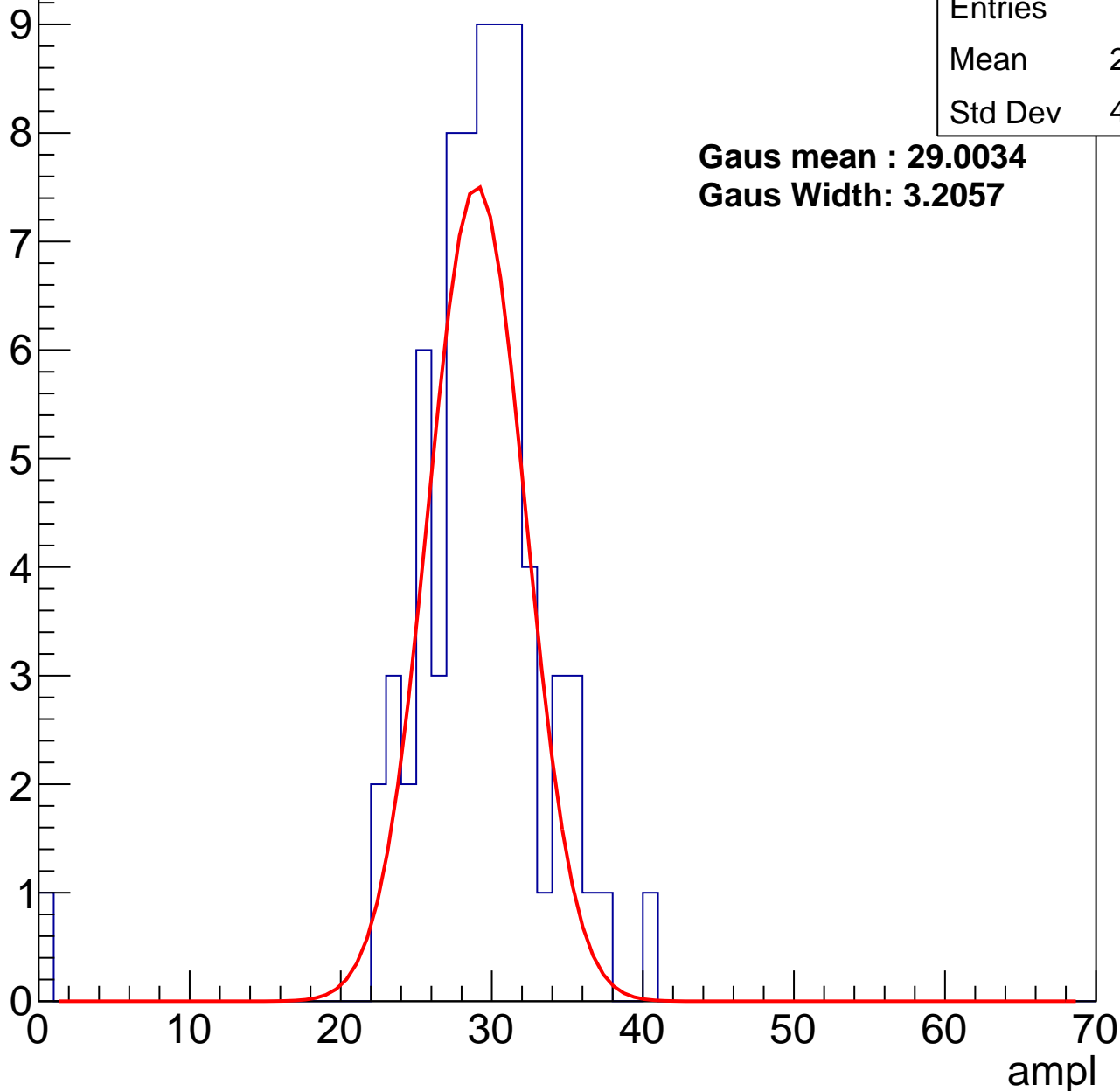
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	28.65
Std Dev	4.884

**Gaus mean : 29.0034**

**Gaus Width: 3.2057**



# B1L103S, U3-ch49, adc1

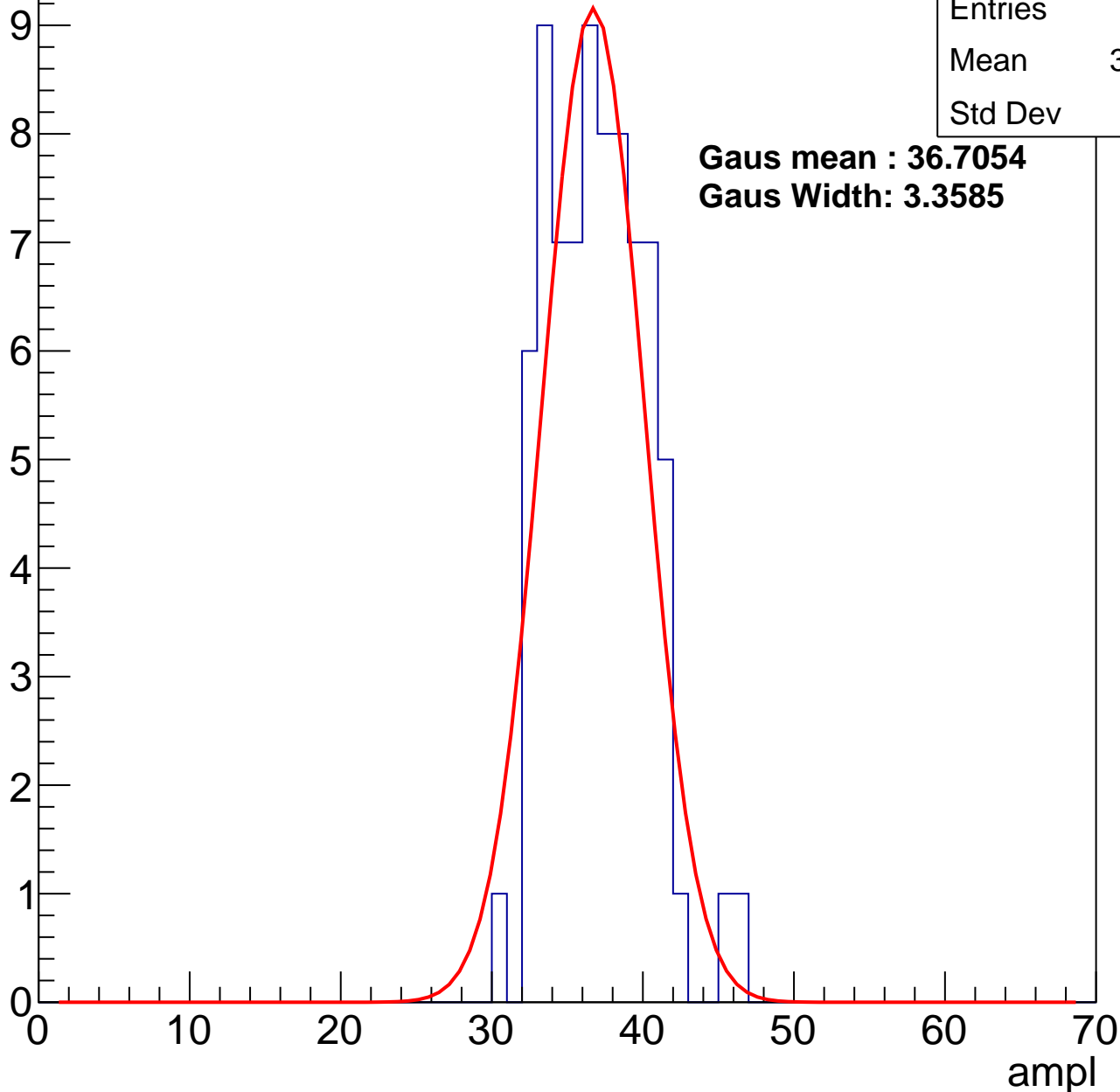
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	36.58
Std Dev	3.18

**Gaus mean : 36.7054**

**Gaus Width: 3.3585**



# B1L103S, U3-ch49, adc2

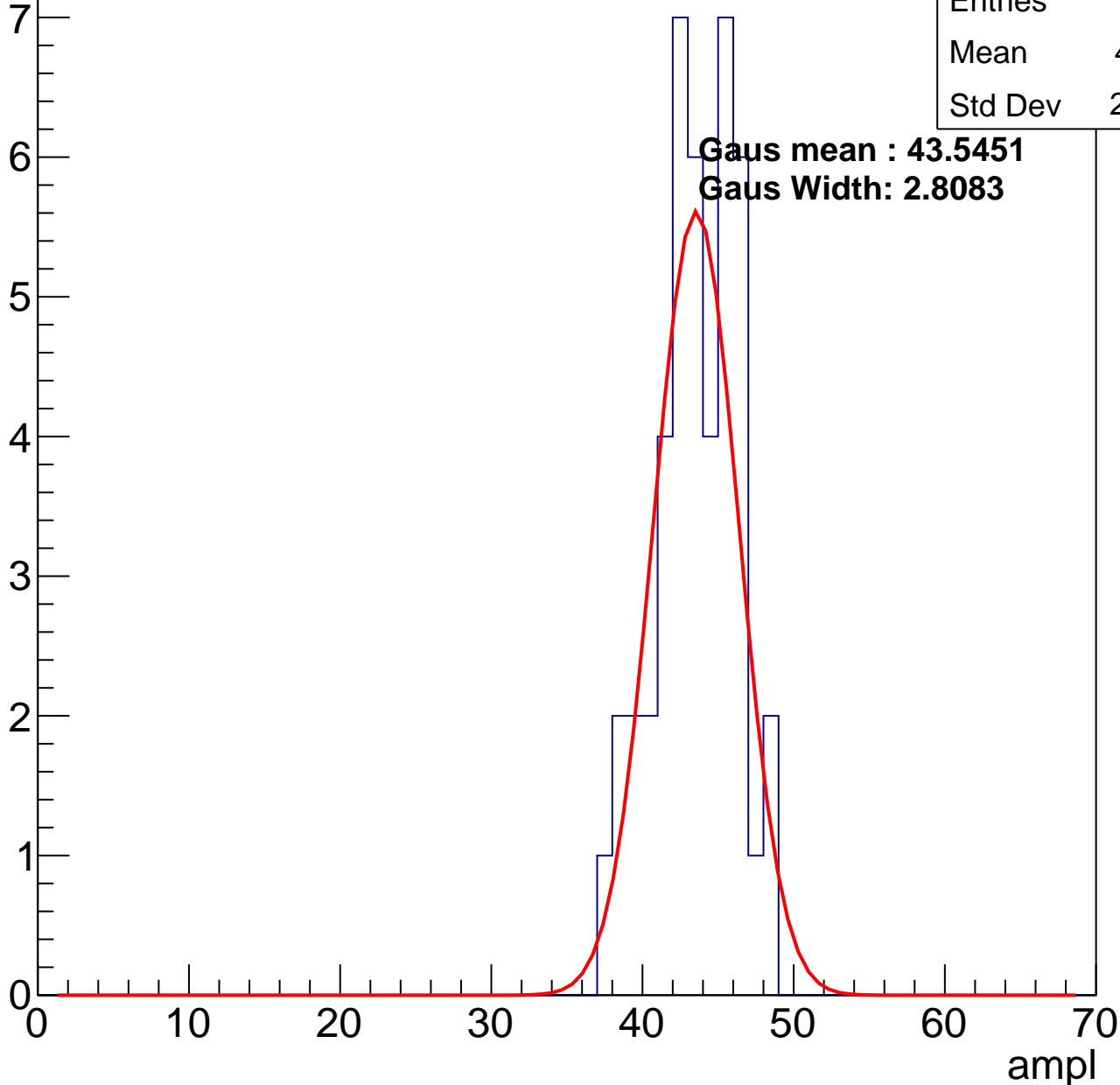
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	44
Mean	43.11
Std Dev	2.656

**Gaus mean : 43.5451**

**Gaus Width: 2.8083**



# B1L103S, U3-ch49, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

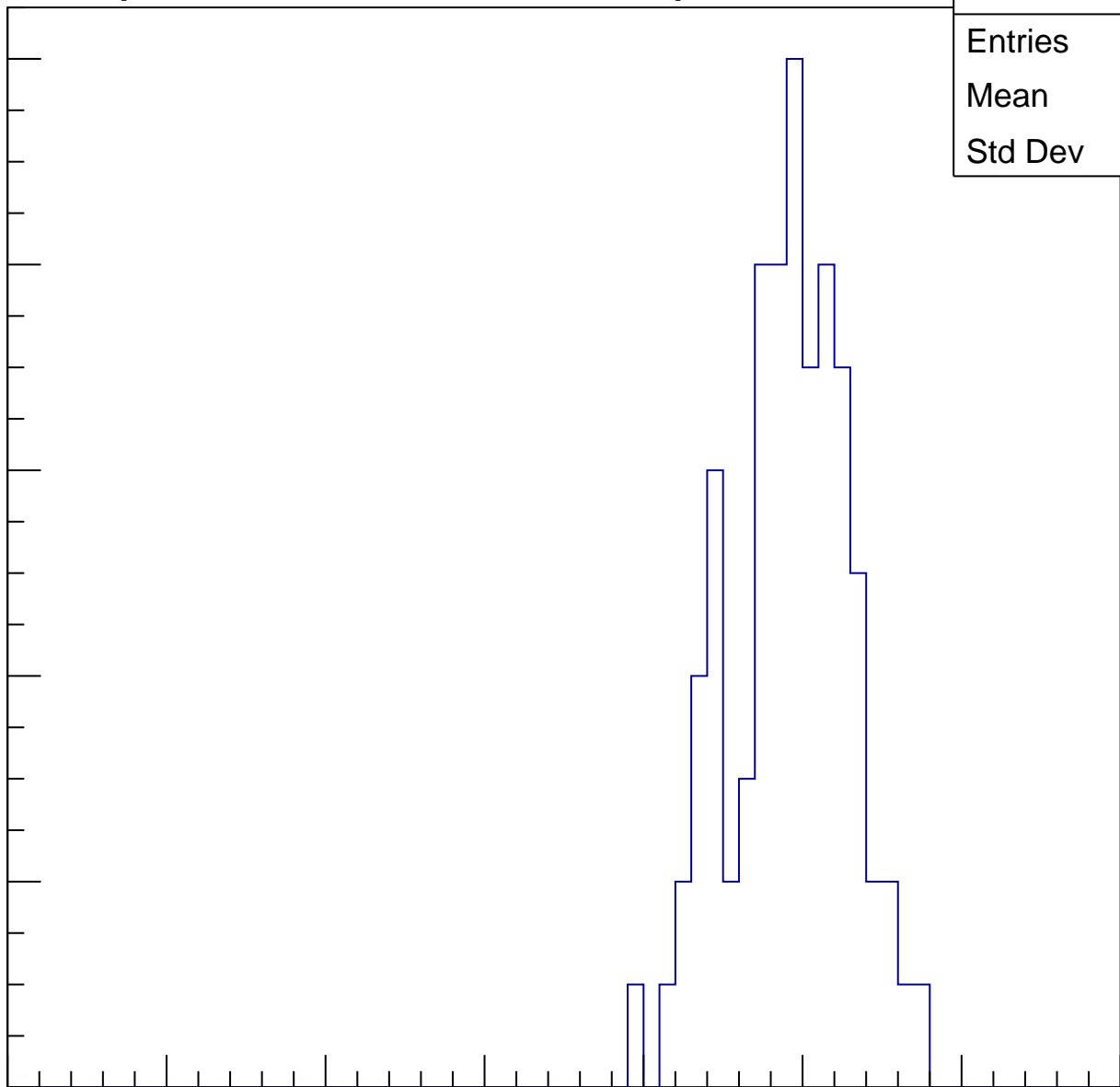
Entries	78
Mean	48.67
Std Dev	3.692

Entry

10  
8  
6  
4  
2  
0

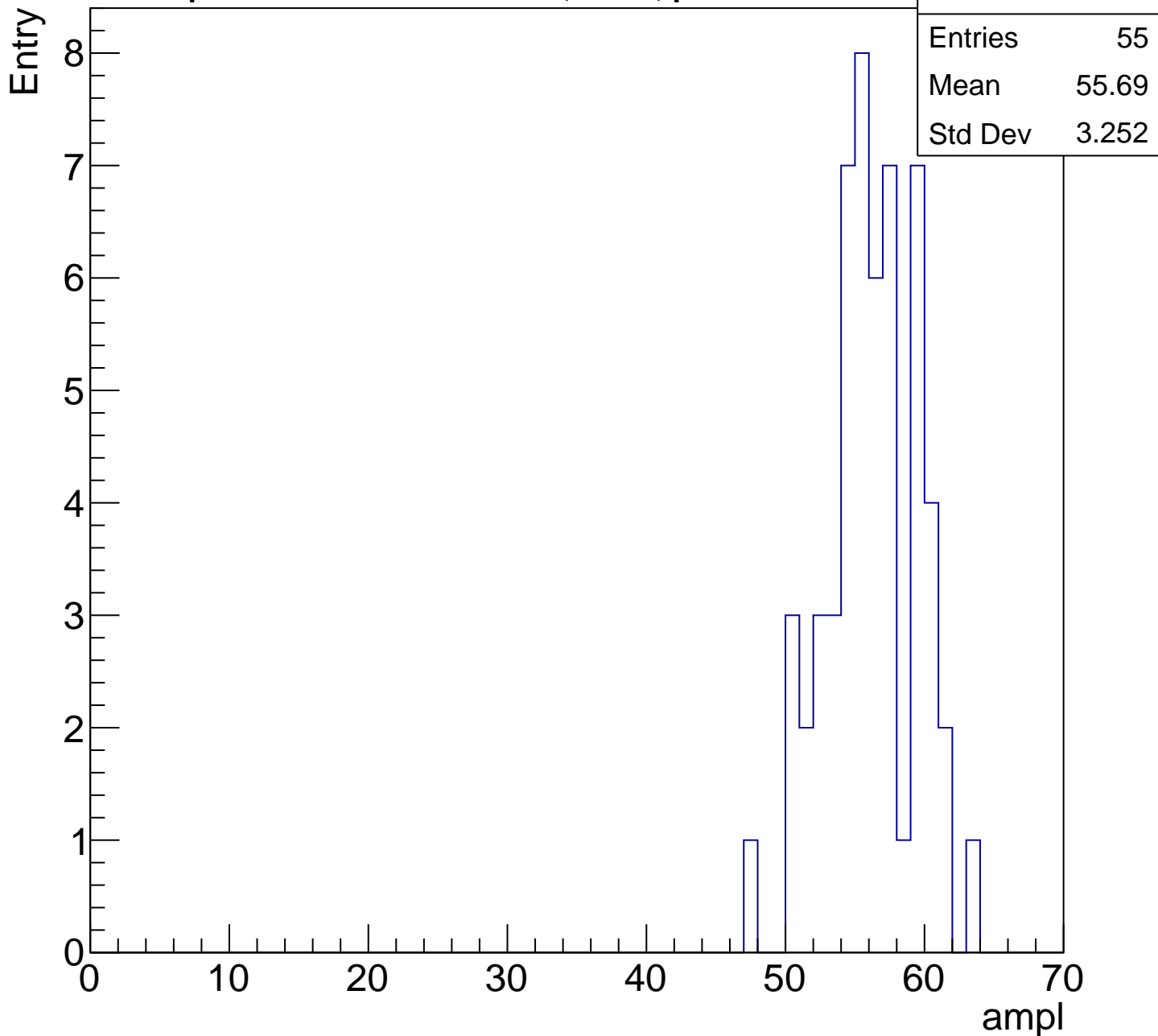
0 10 20 30 40 50 60 70

ampl



# B1L103S, U3-ch49, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

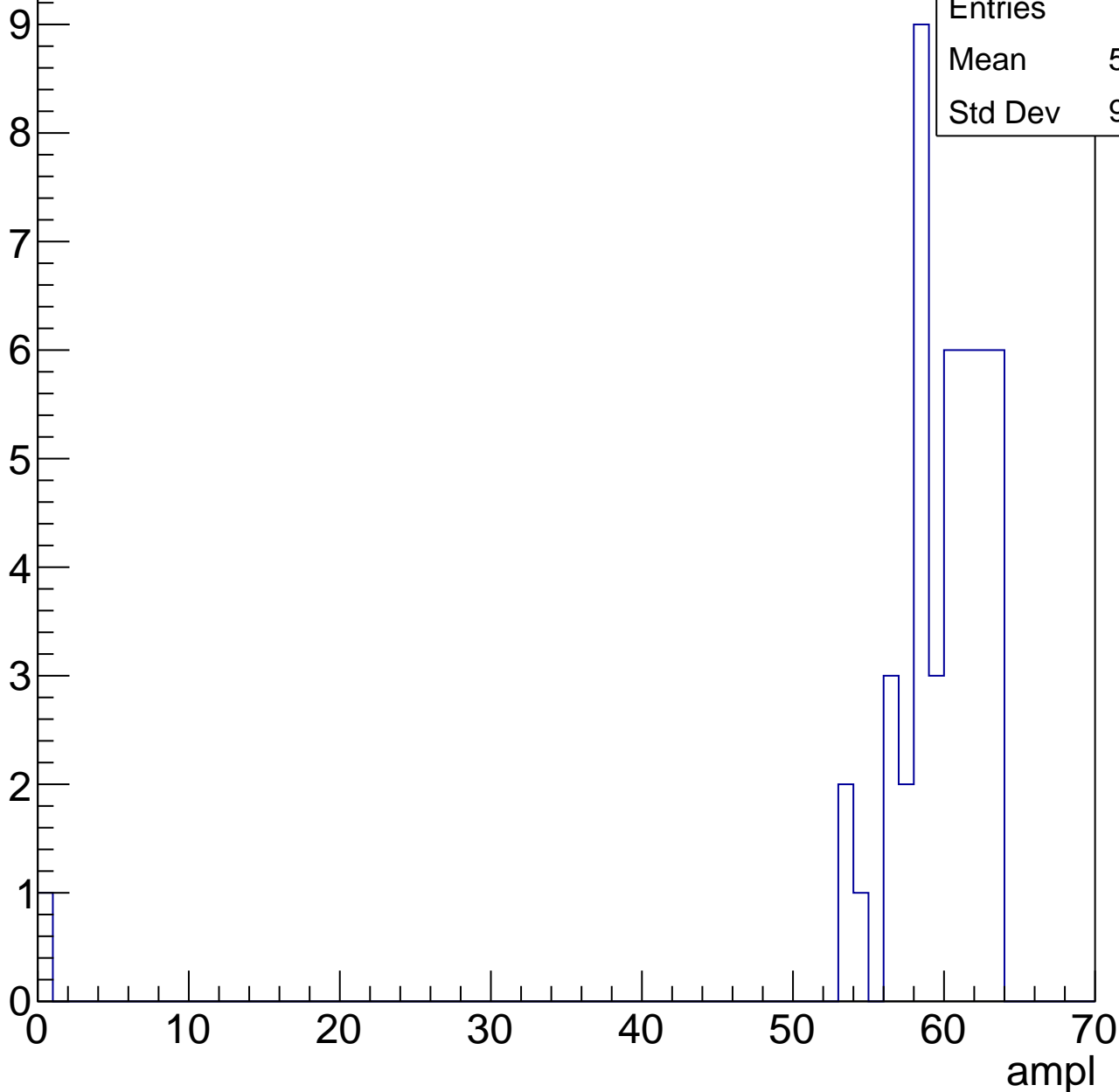


# B1L103S, U3-ch49, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

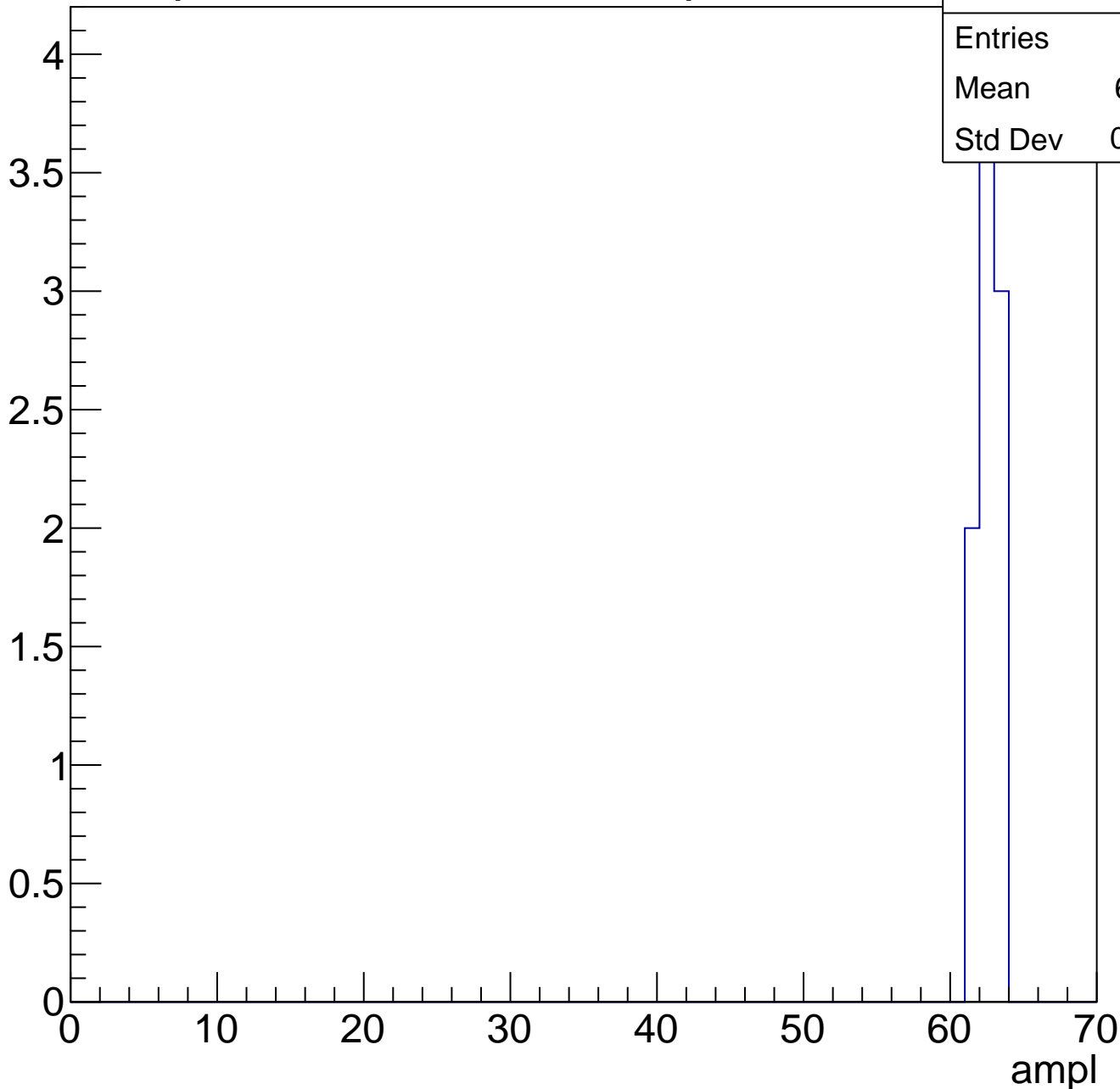
Entries	45
Mean	58.16
Std Dev	9.153



# B1L103S, U3-ch49, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U3-ch49, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch50, adc0

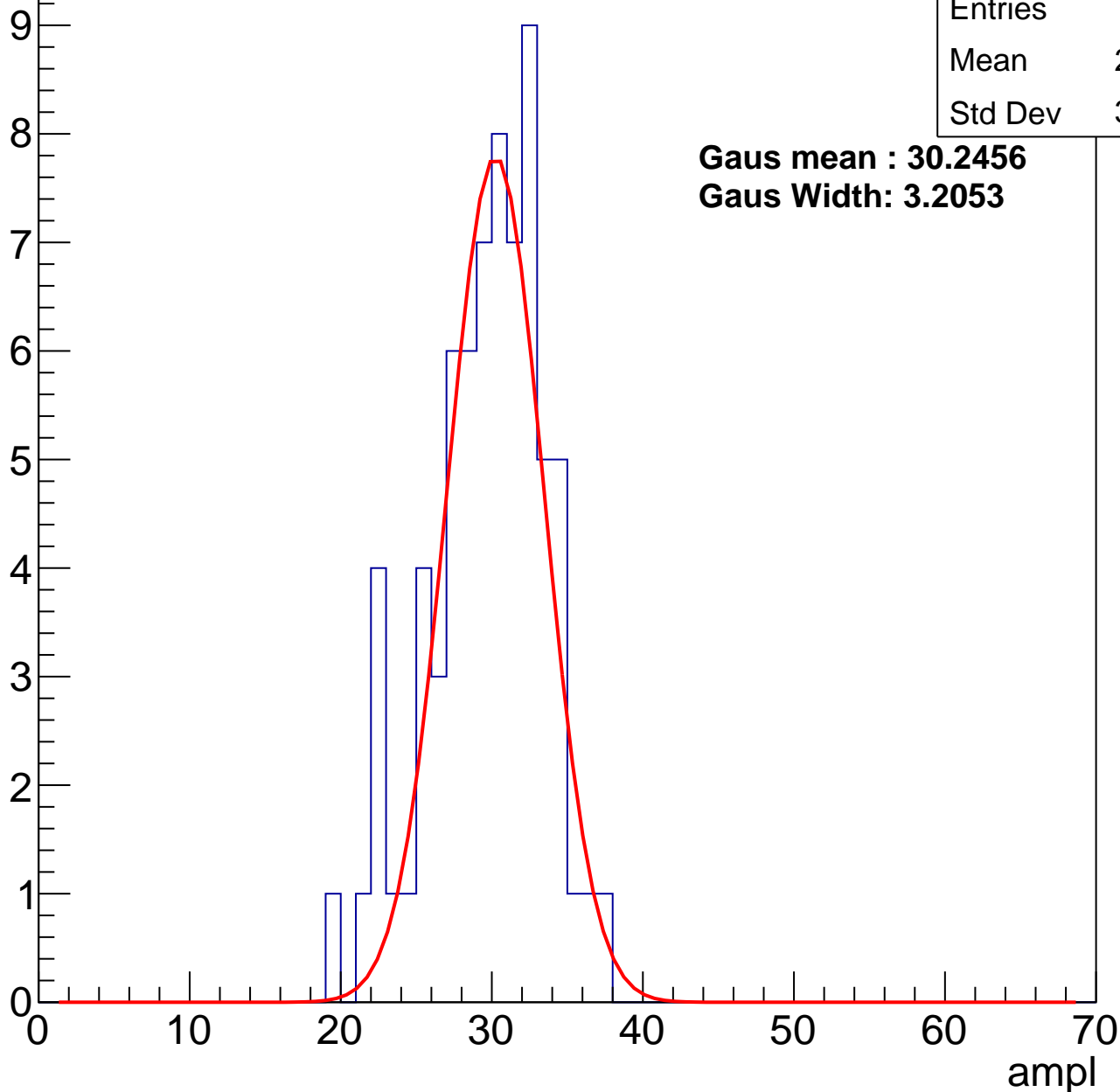
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	29.21
Std Dev	3.771

**Gaus mean : 30.2456**

**Gaus Width: 3.2053**



# B1L103S, U3-ch50, adc1

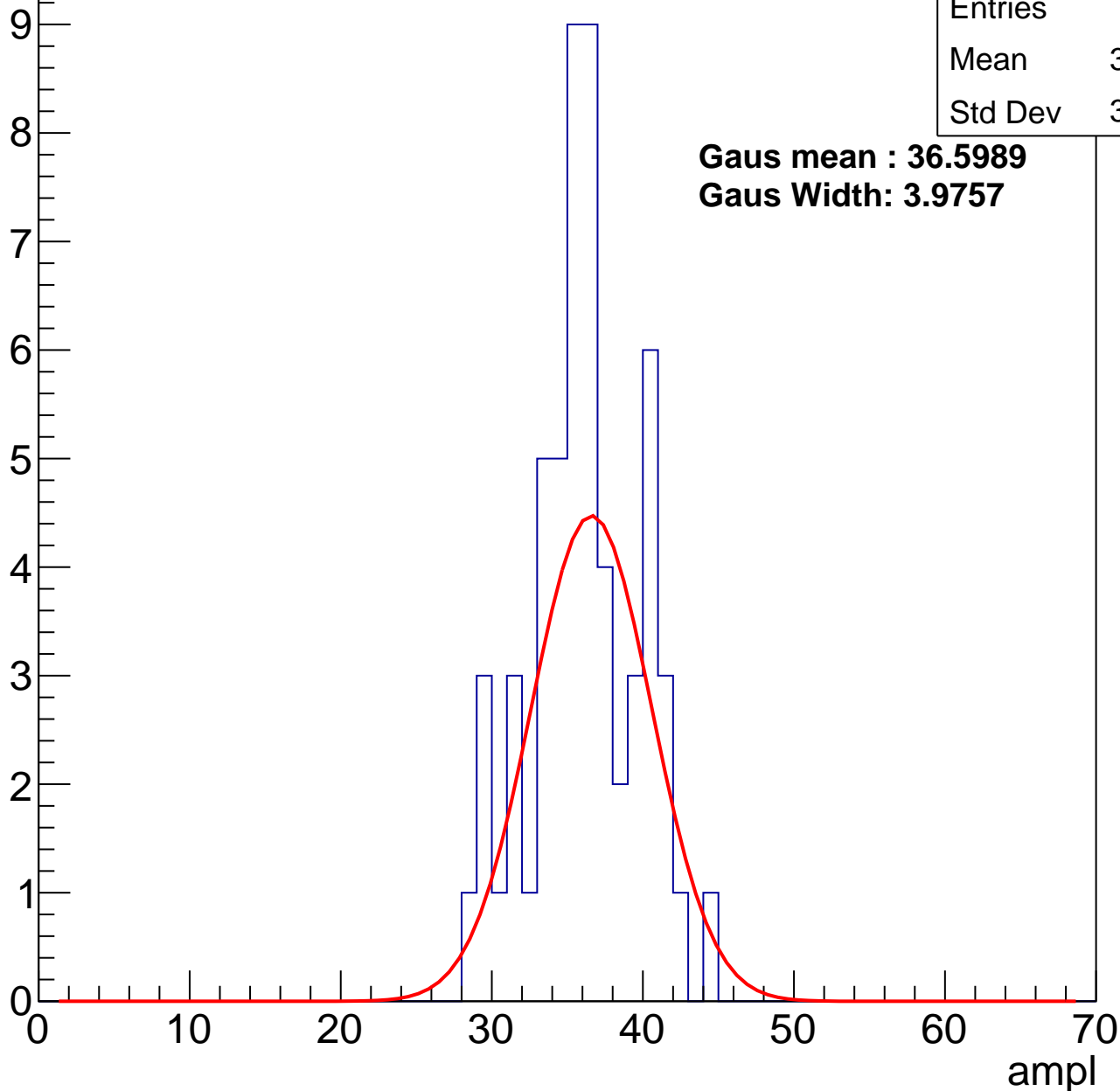
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	35.68
Std Dev	3.545

**Gaus mean : 36.5989**

**Gaus Width: 3.9757**



# B1L103S, U3-ch50, adc2

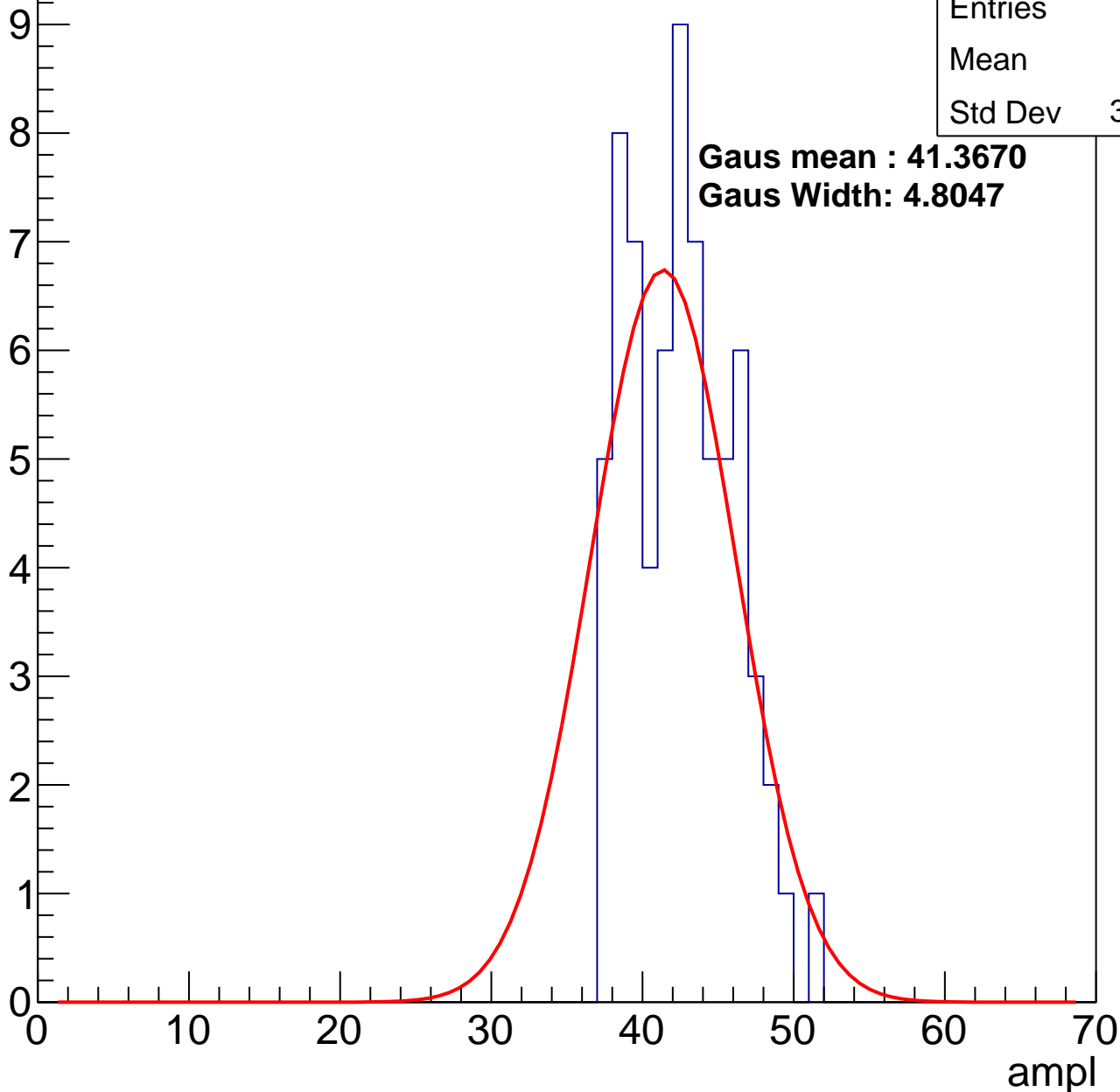
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	42.1
Std Dev	3.367

**Gaus mean : 41.3670**

**Gaus Width: 4.8047**

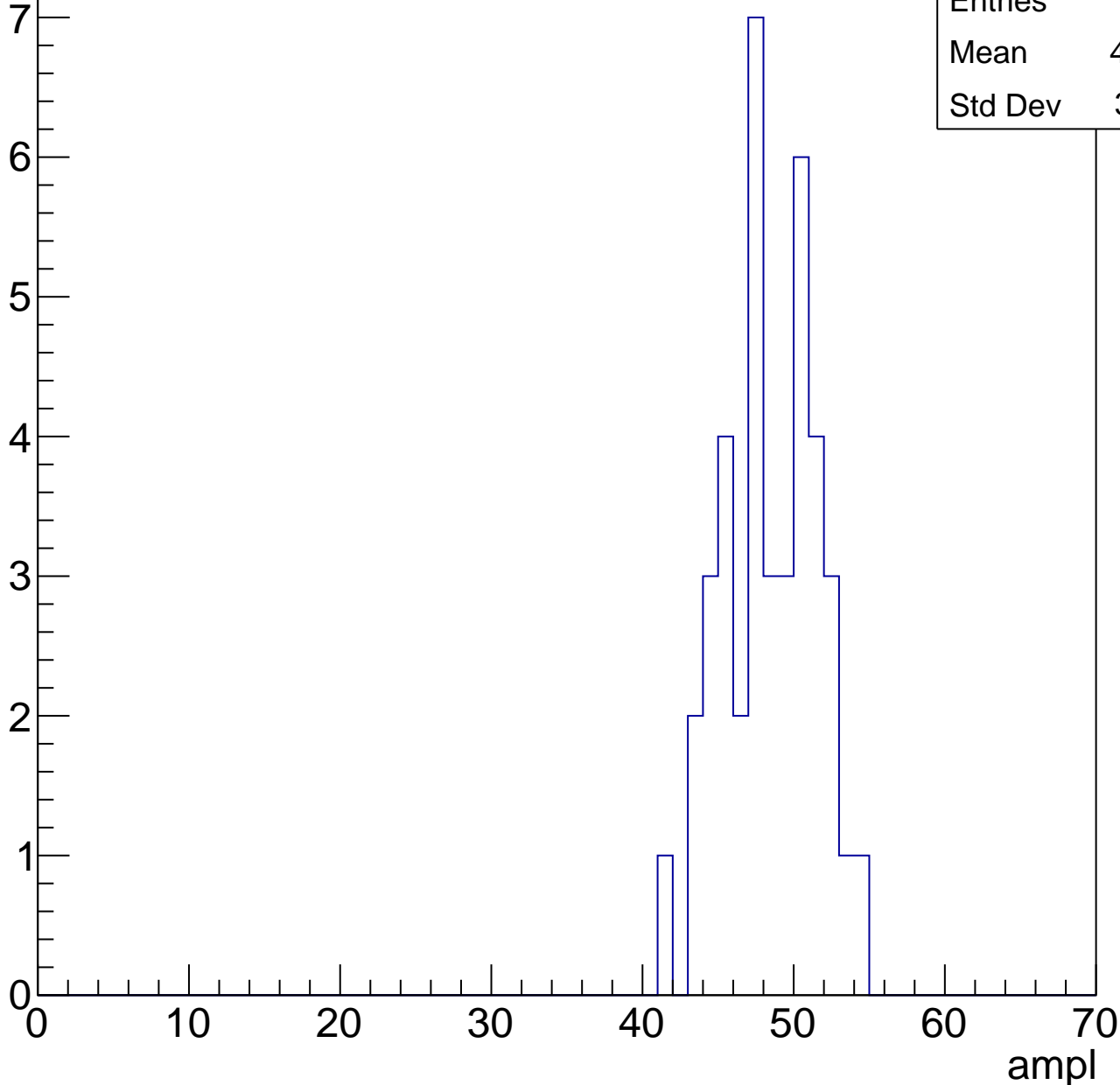


# B1L103S, U3-ch50, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

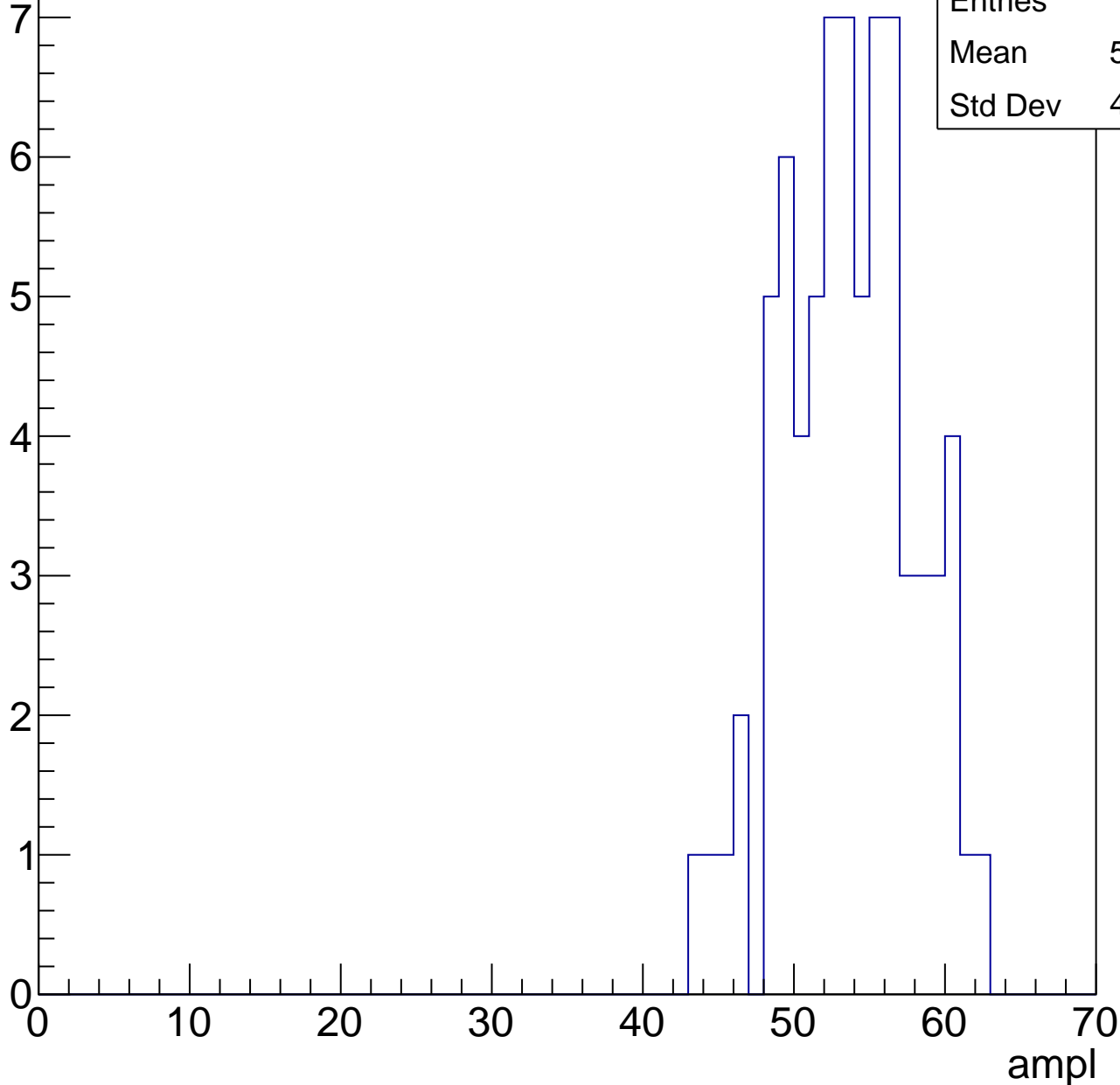
Entries	40
Mean	47.95
Std Dev	3.041



# B1L103S, U3-ch50, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

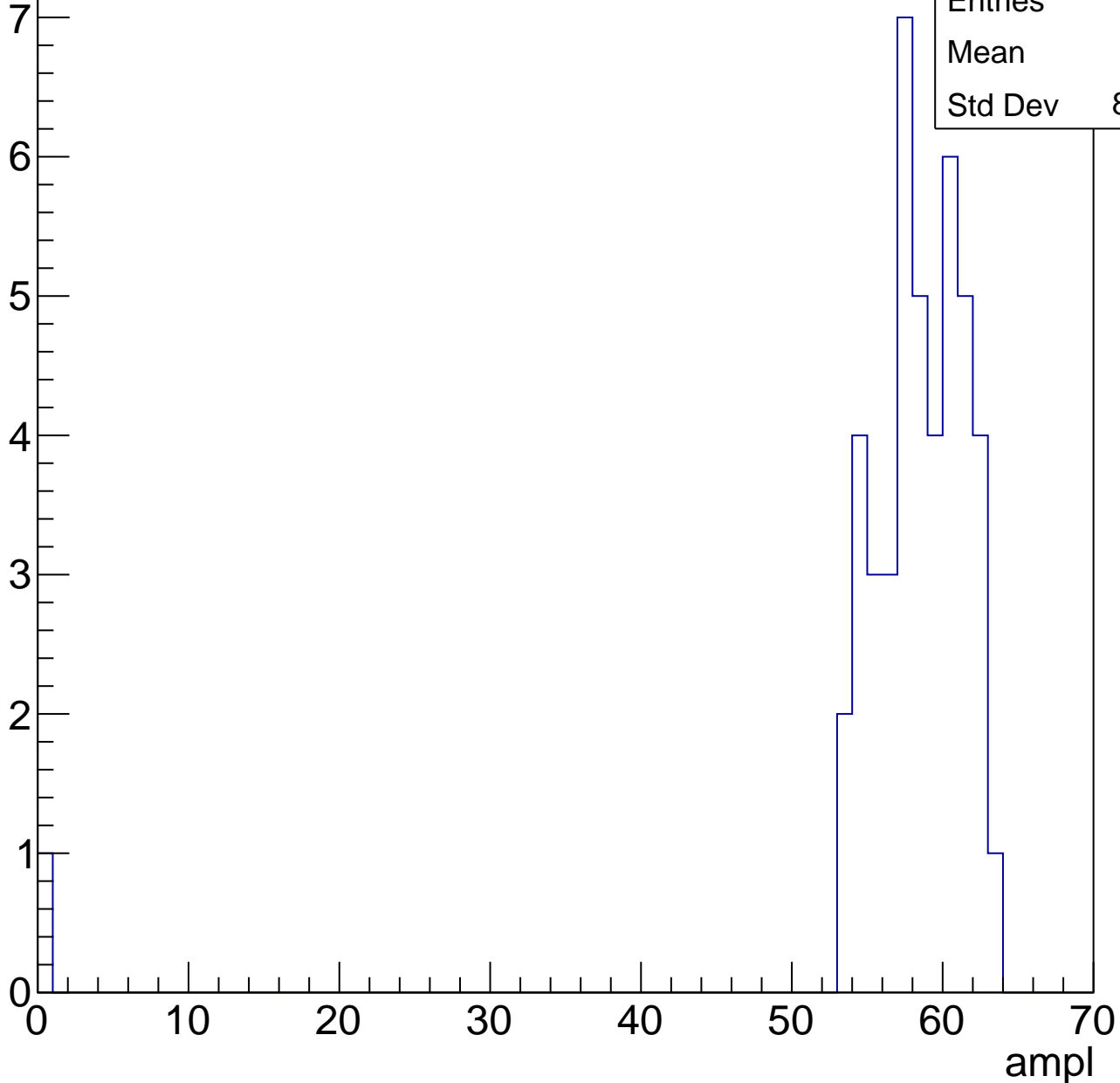


# B1L103S, U3-ch50, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	45
Mean	56.8
Std Dev	8.971

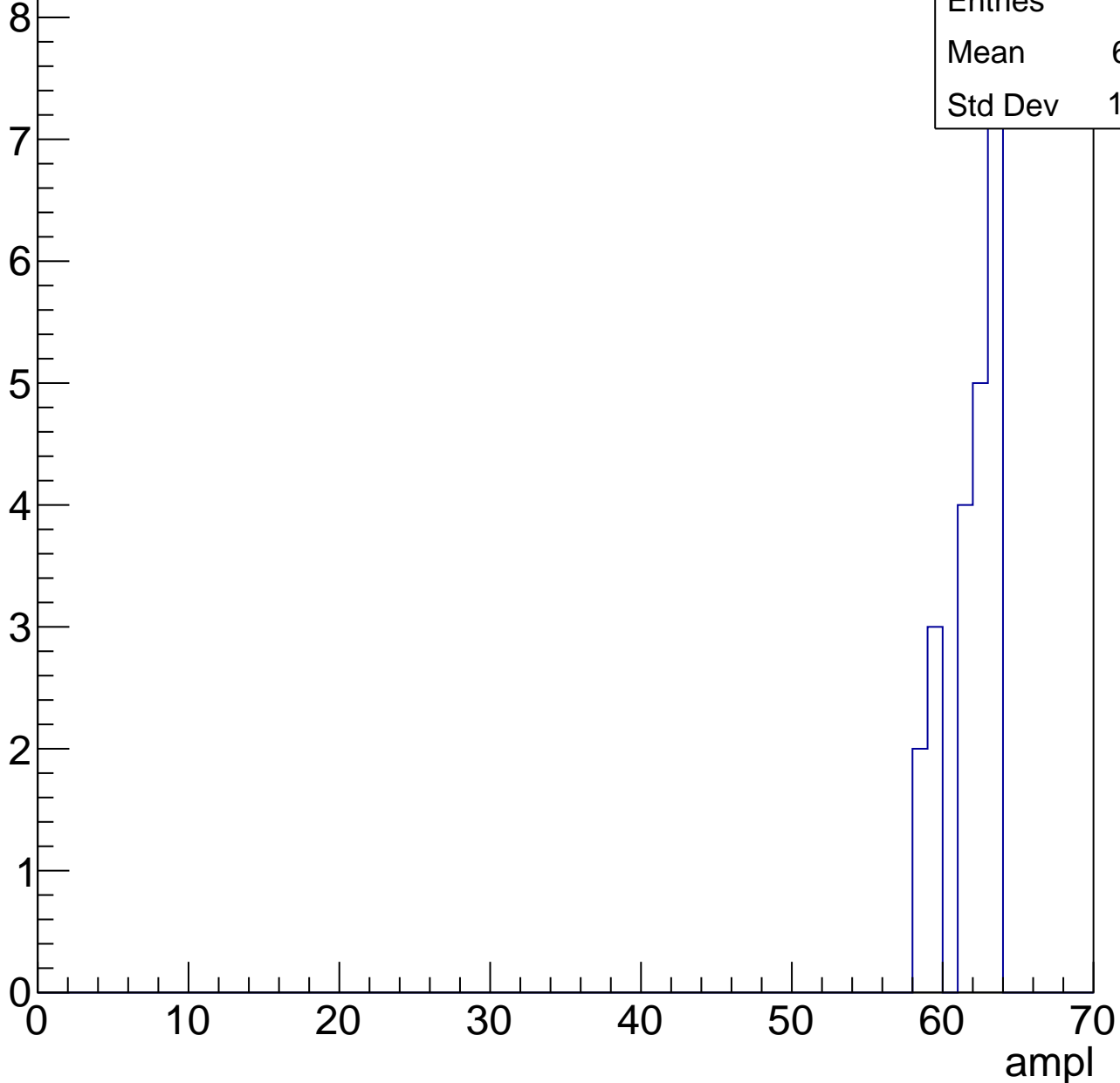


# B1L103S, U3-ch50, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	22
Mean	61.41
Std Dev	1.696





# B1L103S, U3-ch50, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch51, adc0

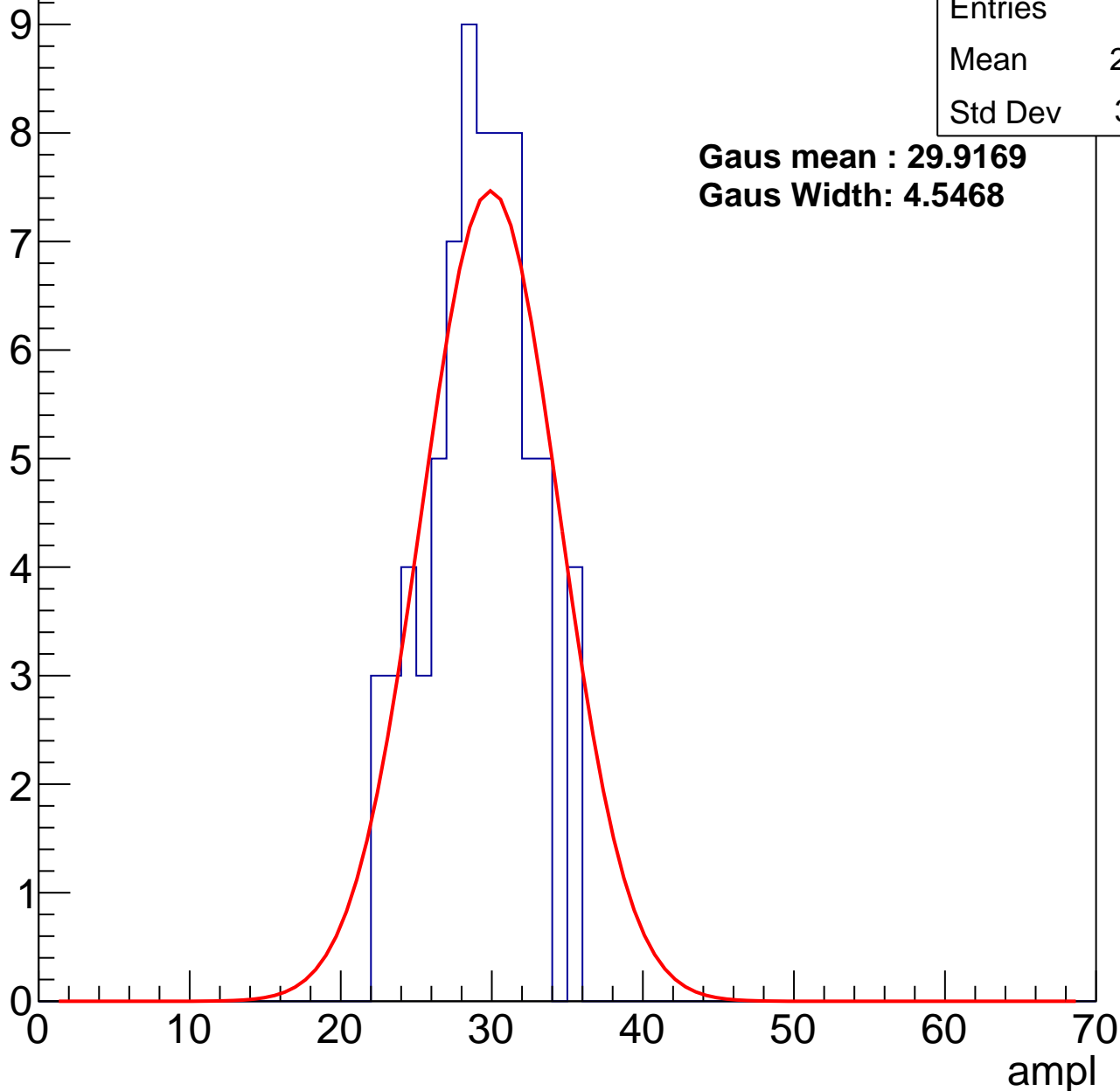
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	28.64
Std Dev	3.301

**Gaus mean : 29.9169**

**Gaus Width: 4.5468**



# B1L103S, U3-ch51, adc1

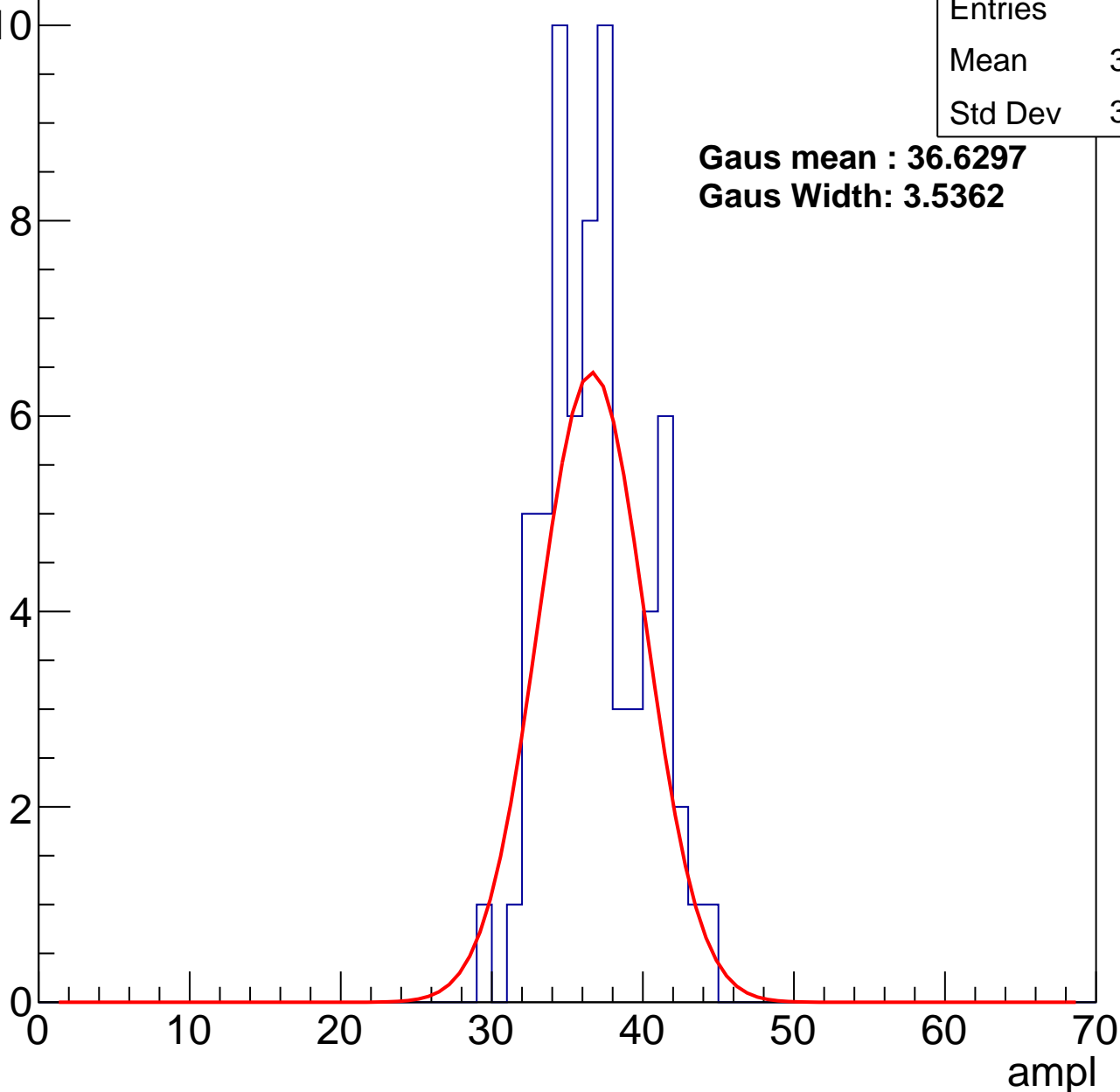
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	36.38
Std Dev	3.218

**Gaus mean : 36.6297**

**Gaus Width: 3.5362**



# B1L103S, U3-ch51, adc2

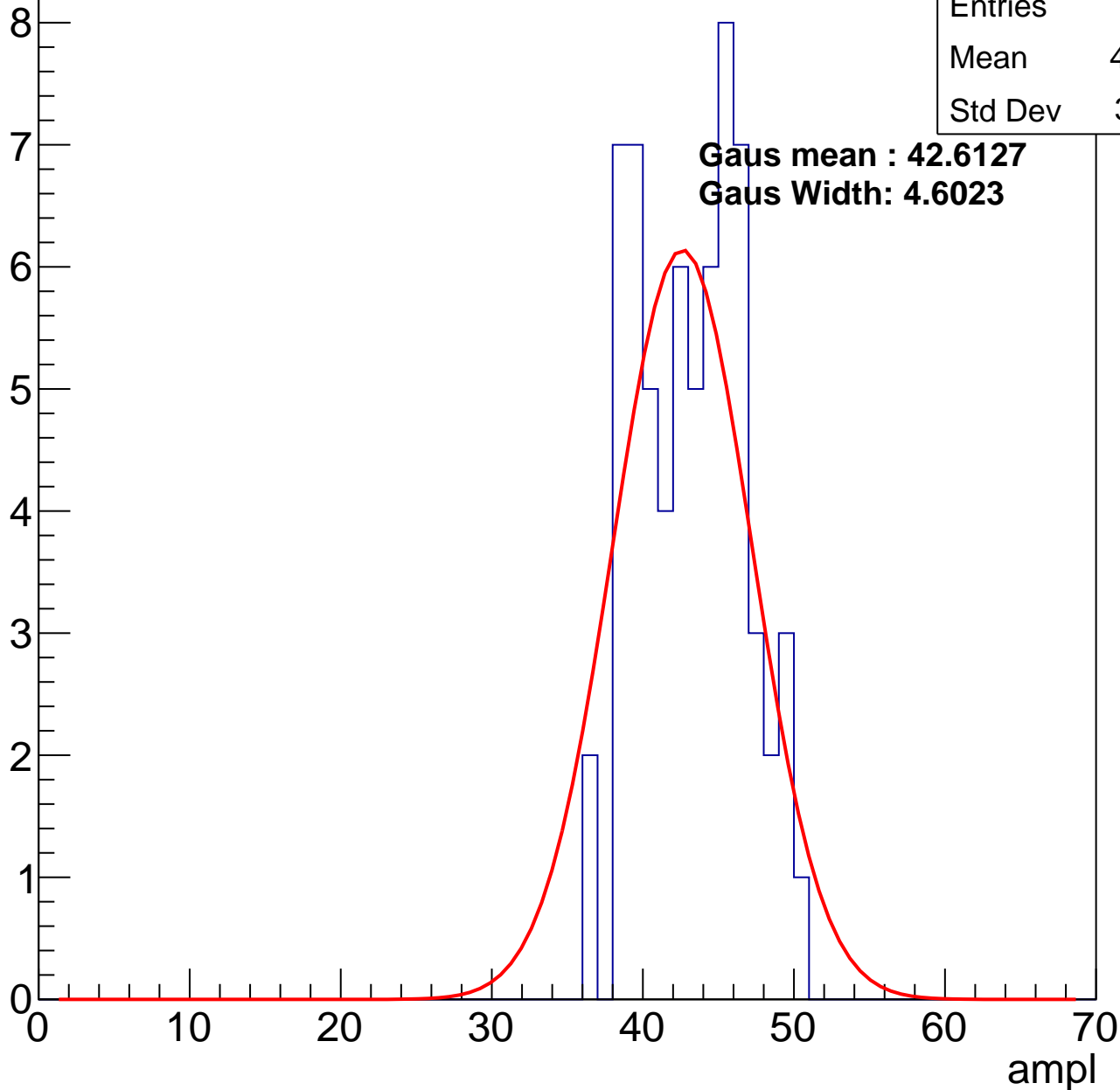
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	42.76
Std Dev	3.491

**Gaus mean : 42.6127**

**Gaus Width: 4.6023**

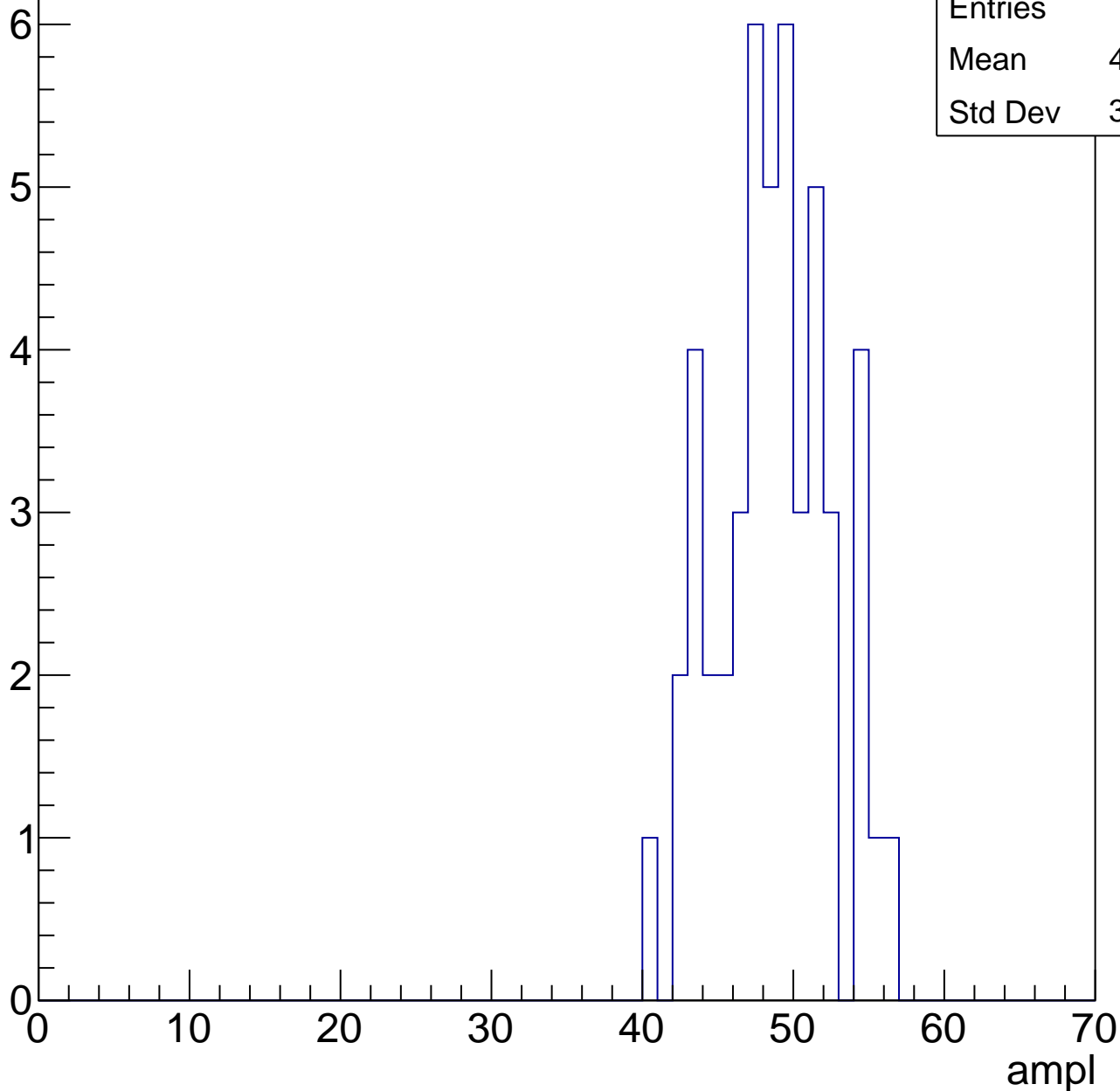


# B1L103S, U3-ch51, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

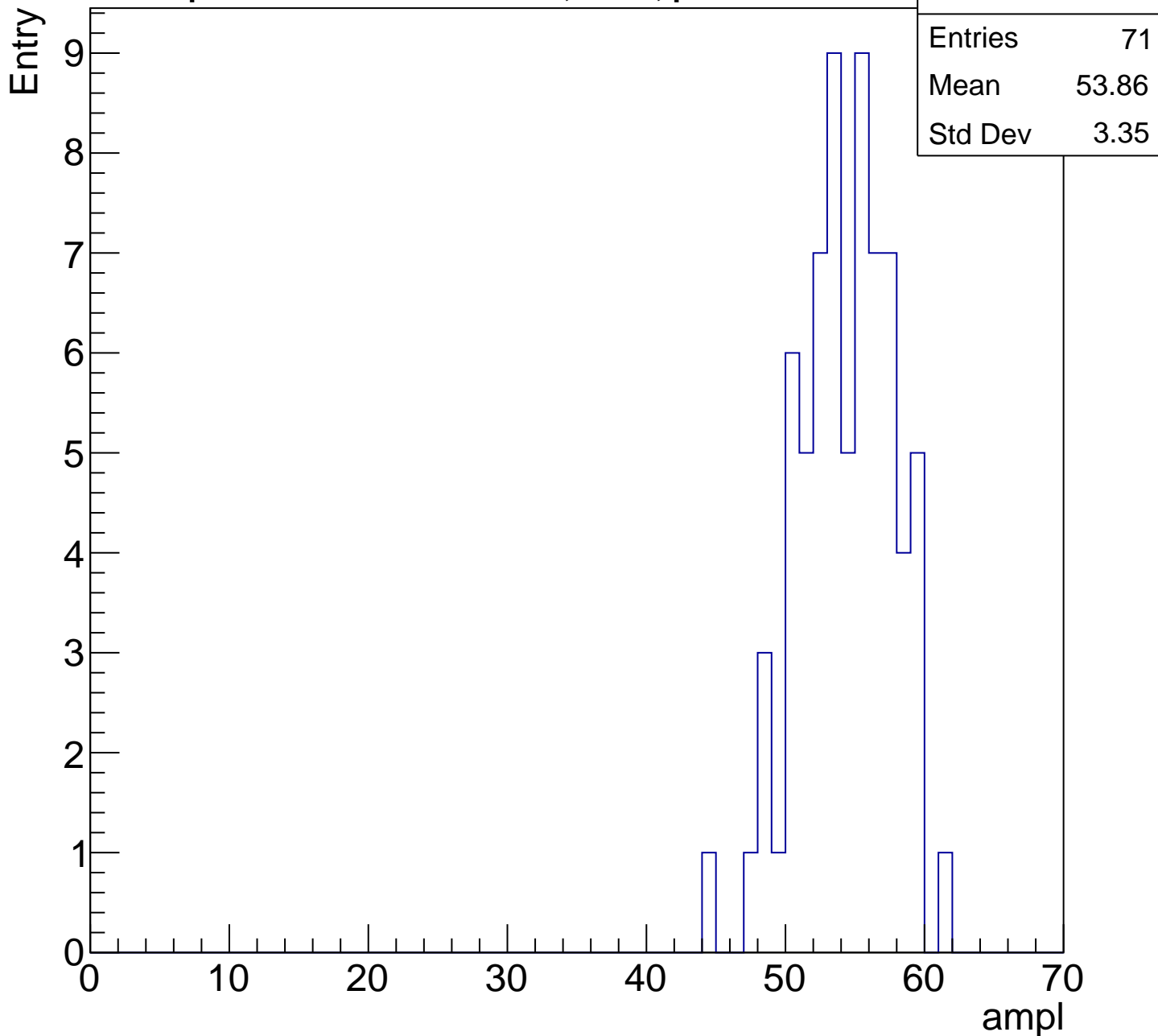
Entry

Entries	48
Mean	48.25
Std Dev	3.733



# B1L103S, U3-ch51, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U3-ch51, adc5

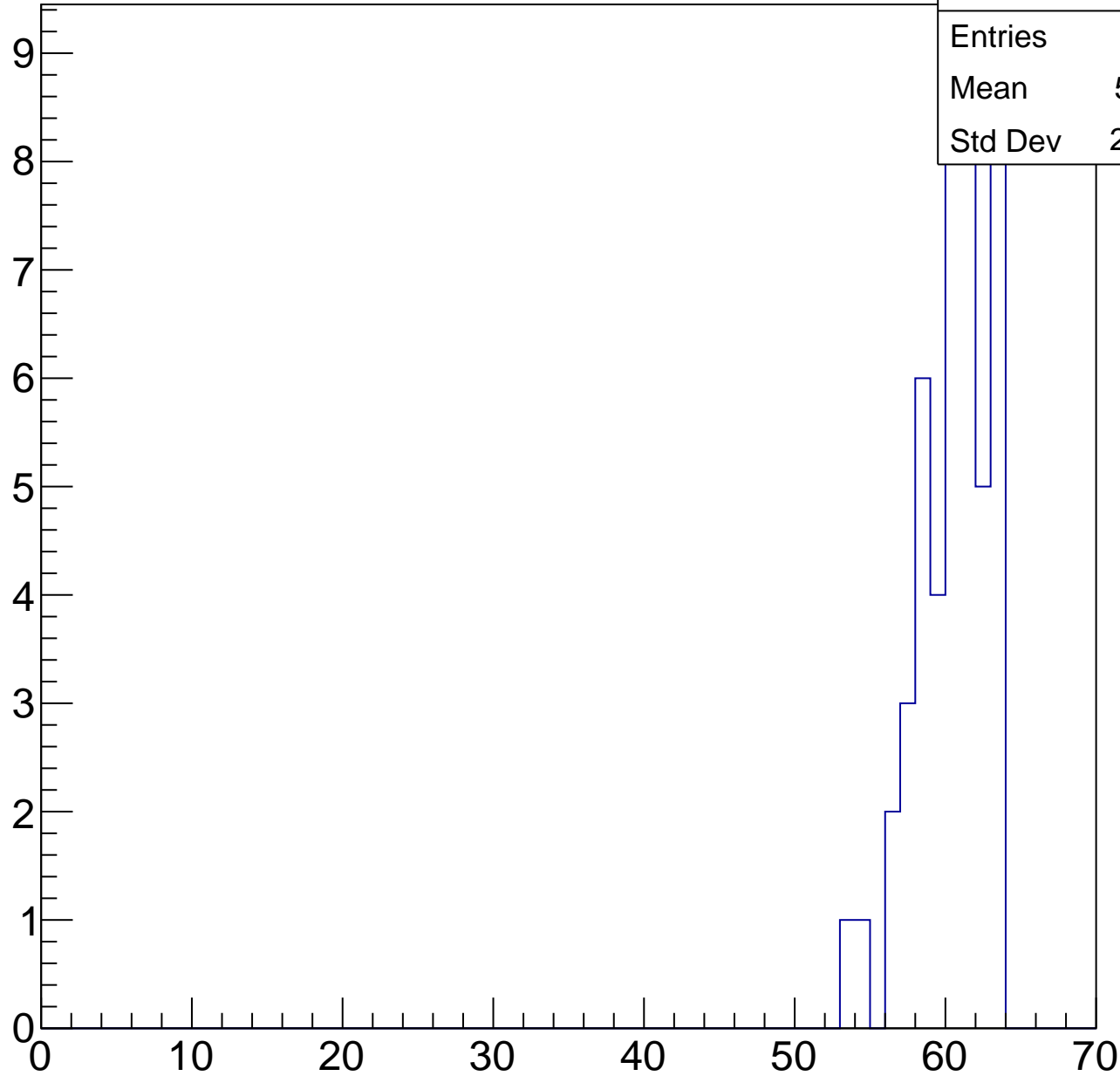
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	47
Mean	59.91
Std Dev	2.404

ampl

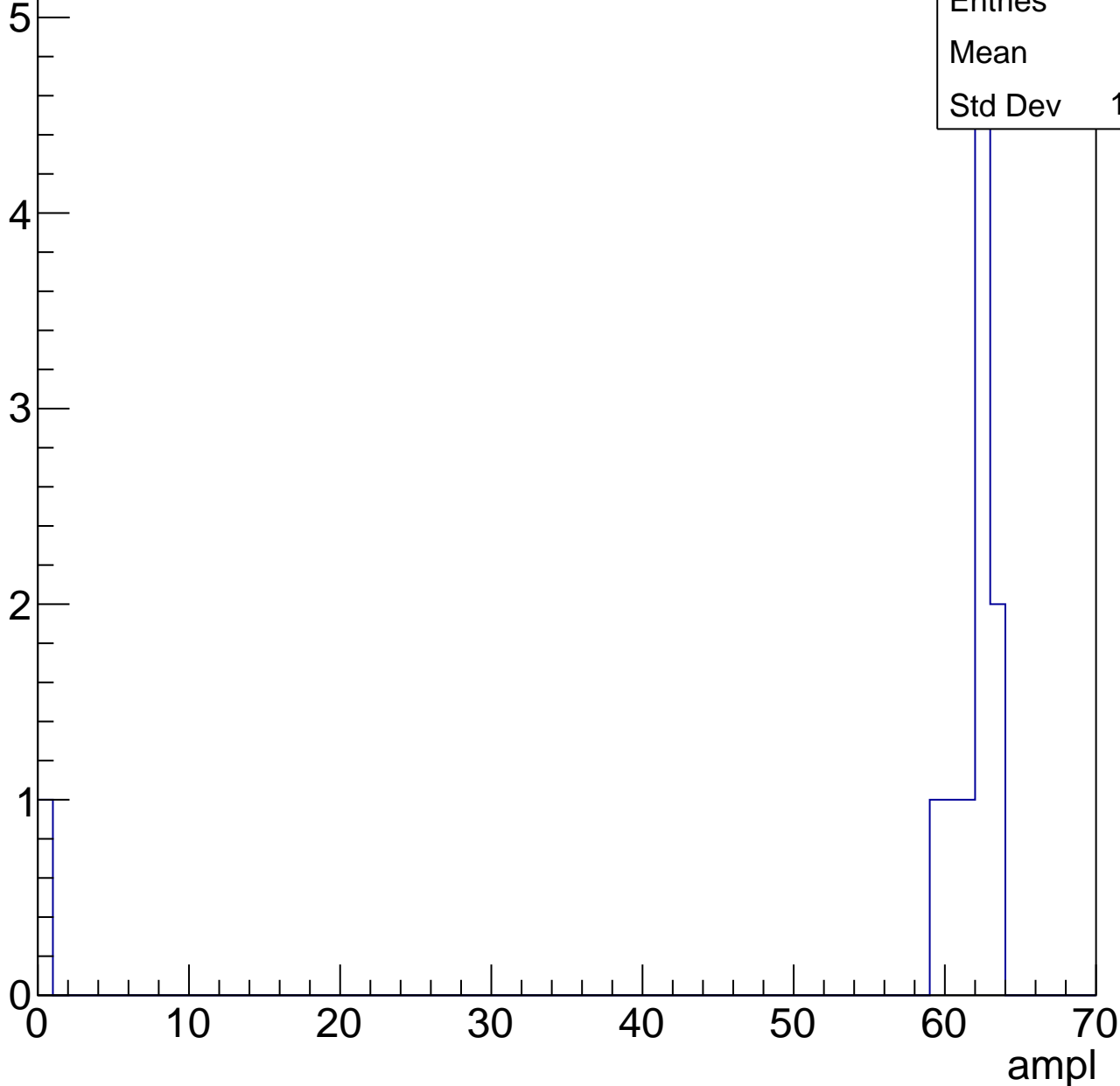


# B1L103S, U3-ch51, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	11
Mean	56
Std Dev	17.75





# B1L103S, U3-ch51, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U3-ch52, adc0

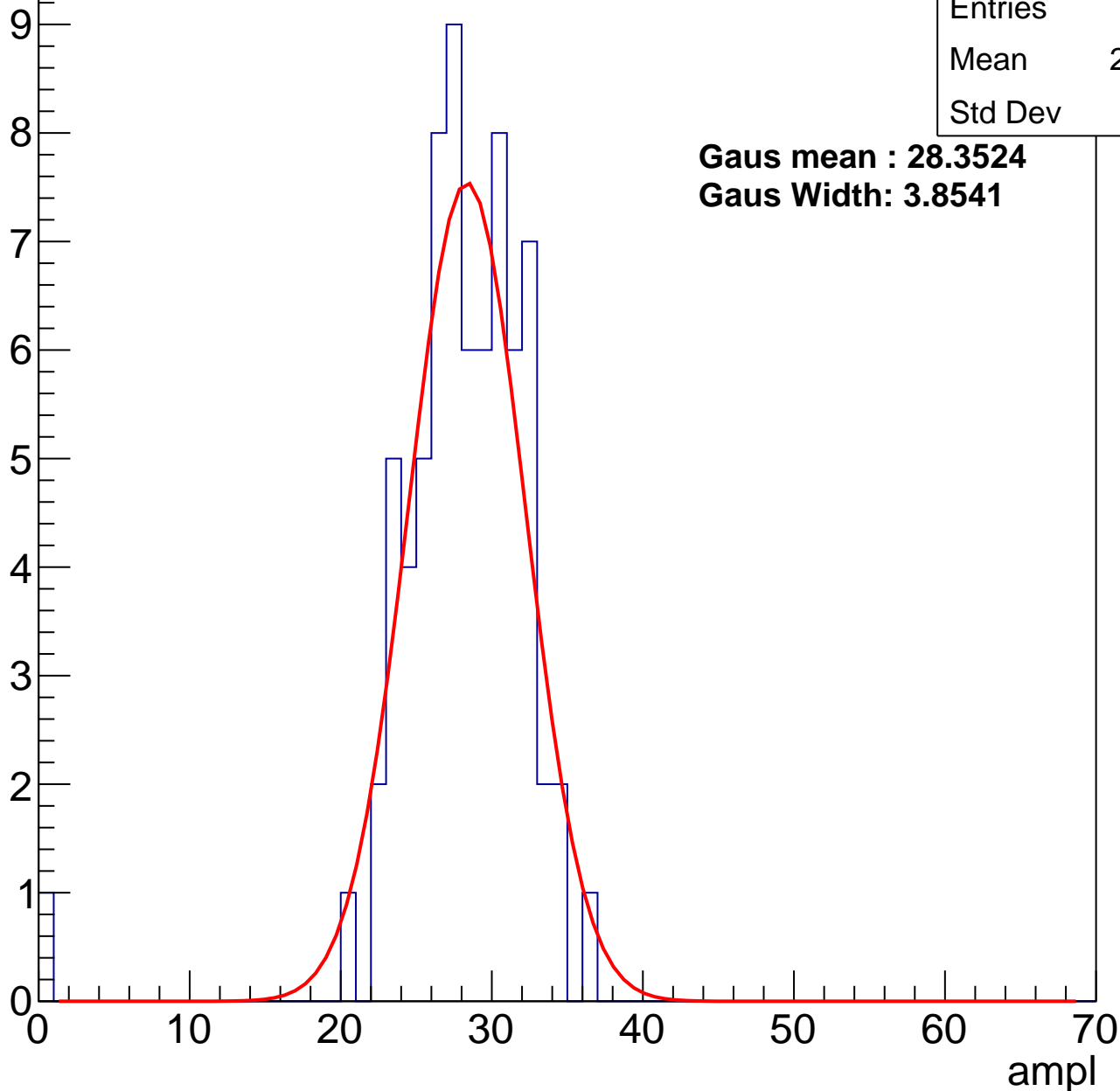
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	27.58
Std Dev	4.64

**Gaus mean : 28.3524**

**Gaus Width: 3.8541**



# B1L103S, U3-ch52, adc1

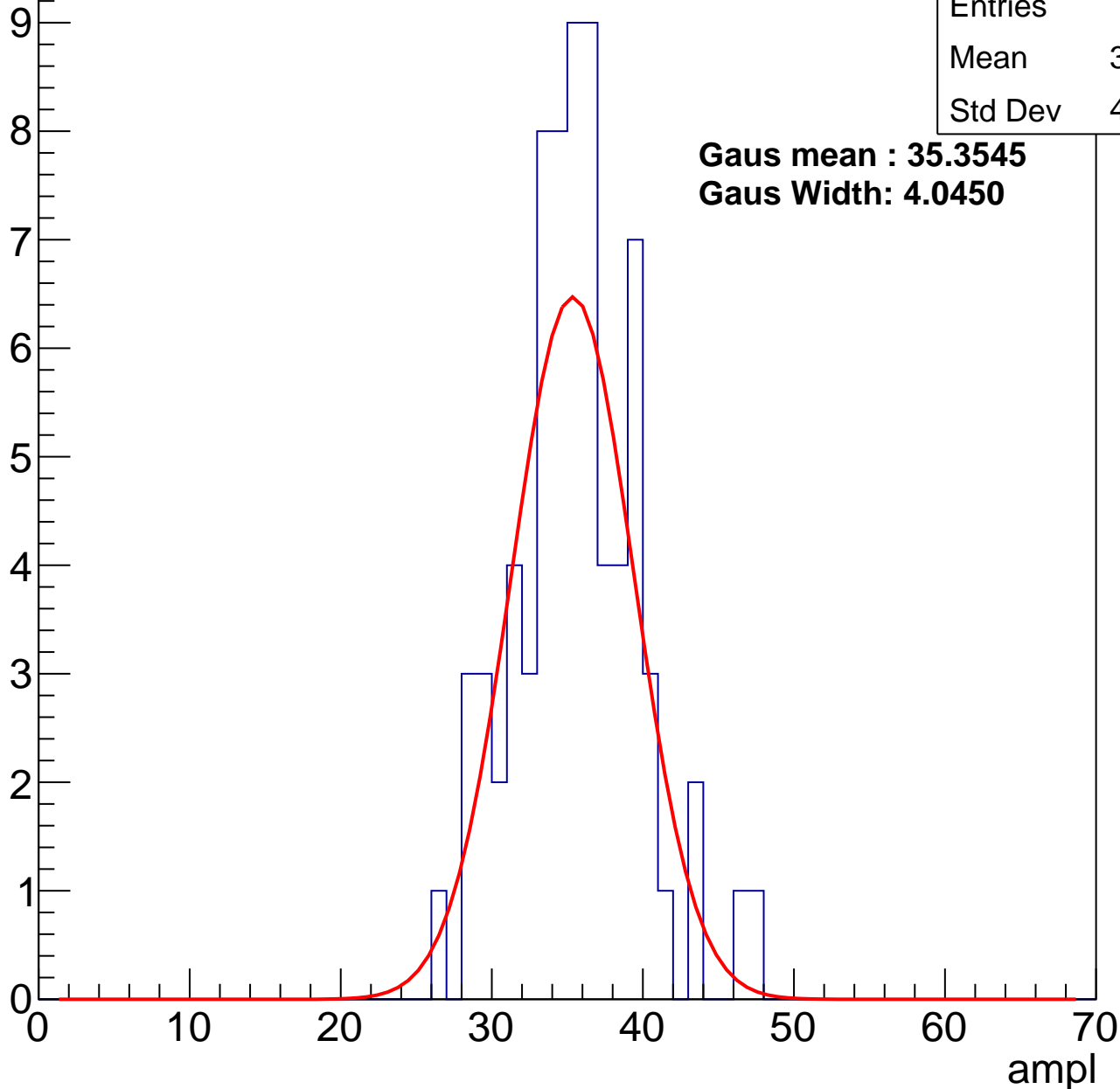
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	35.14
Std Dev	4.042

**Gaus mean : 35.3545**

**Gaus Width: 4.0450**



# B1L103S, U3-ch52, adc2

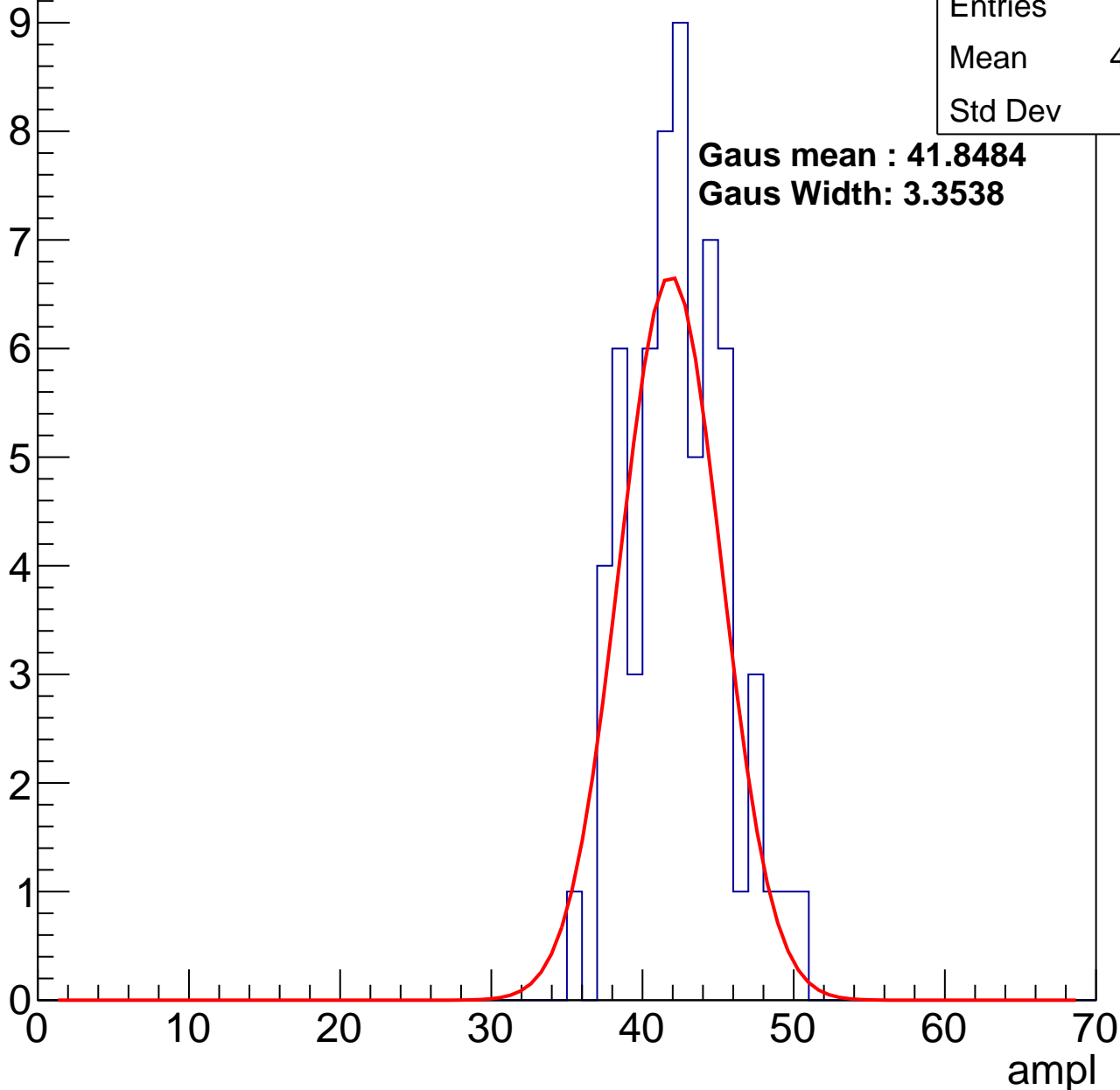
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	41.95
Std Dev	3.19

**Gaus mean : 41.8484**

**Gaus Width: 3.3538**

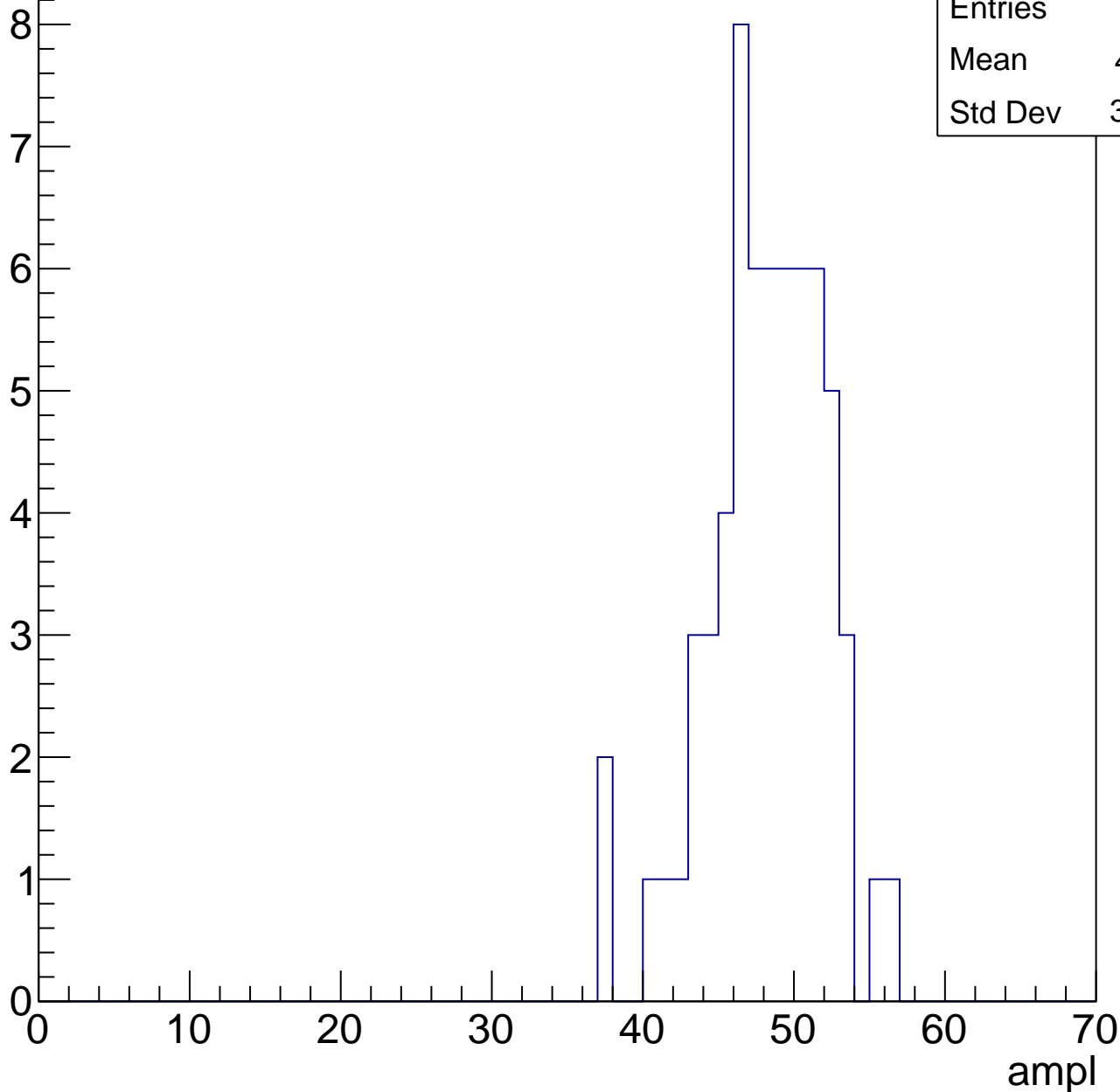


# B1L103S, U3-ch52, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	47.71
Std Dev	3.852

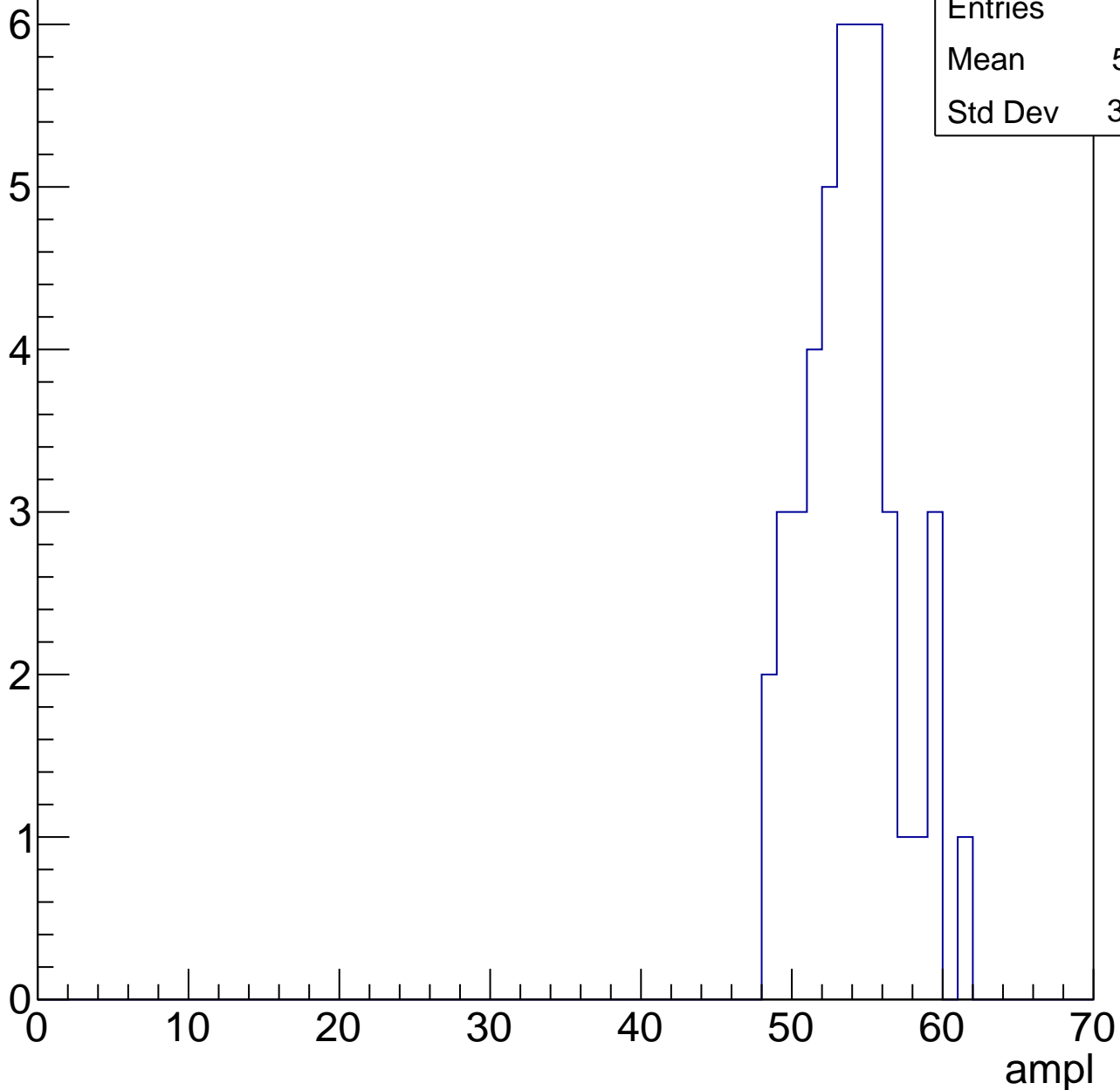


# B1L103S, U3-ch52, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

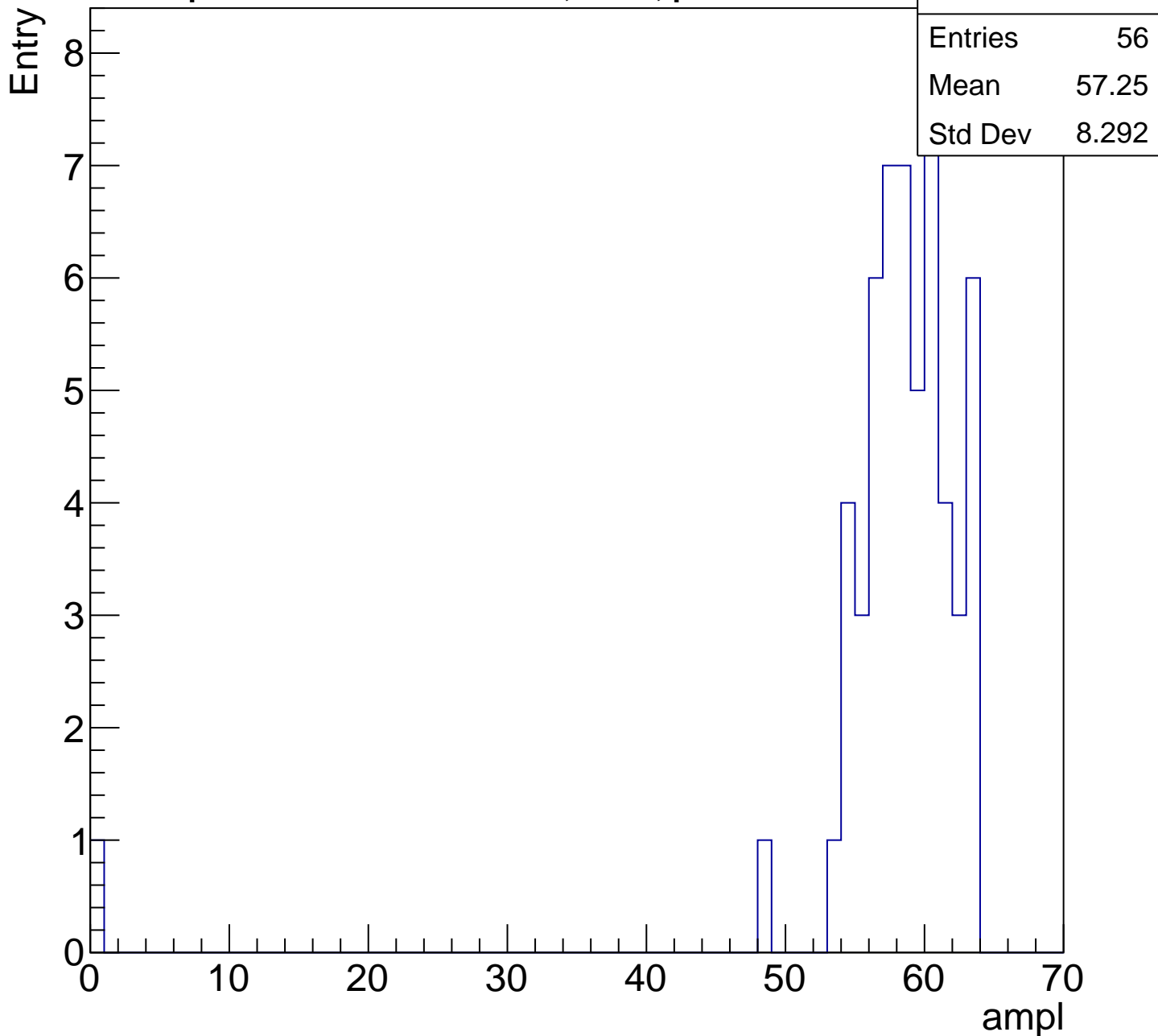
Entry

Entries	44
Mean	53.41
Std Dev	3.047



# B1L103S, U3-ch52, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

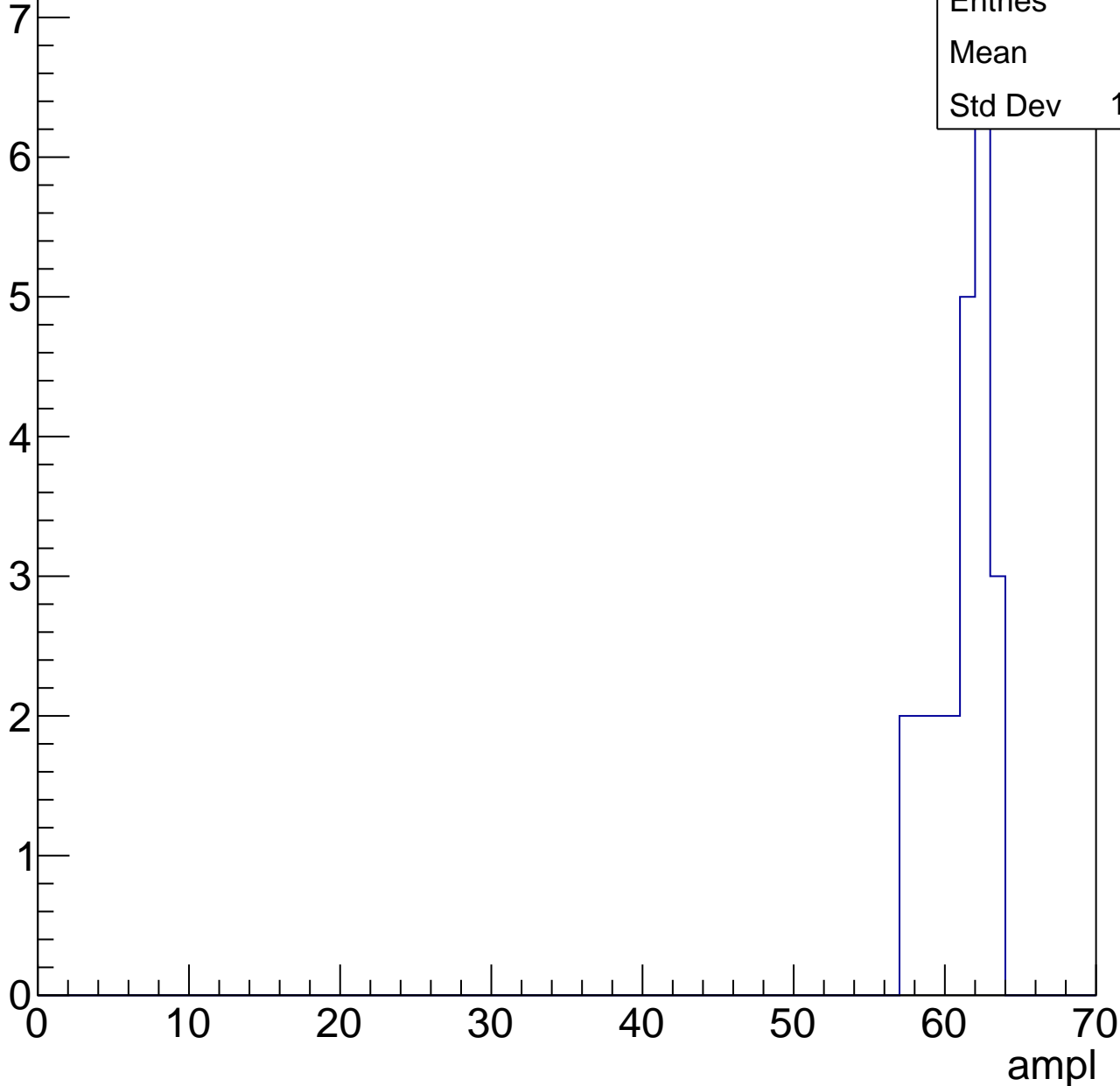


# B1L103S, U3-ch52, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	23
Mean	60.7
Std Dev	1.828





# B1L103S, U3-ch52, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch53, adc0

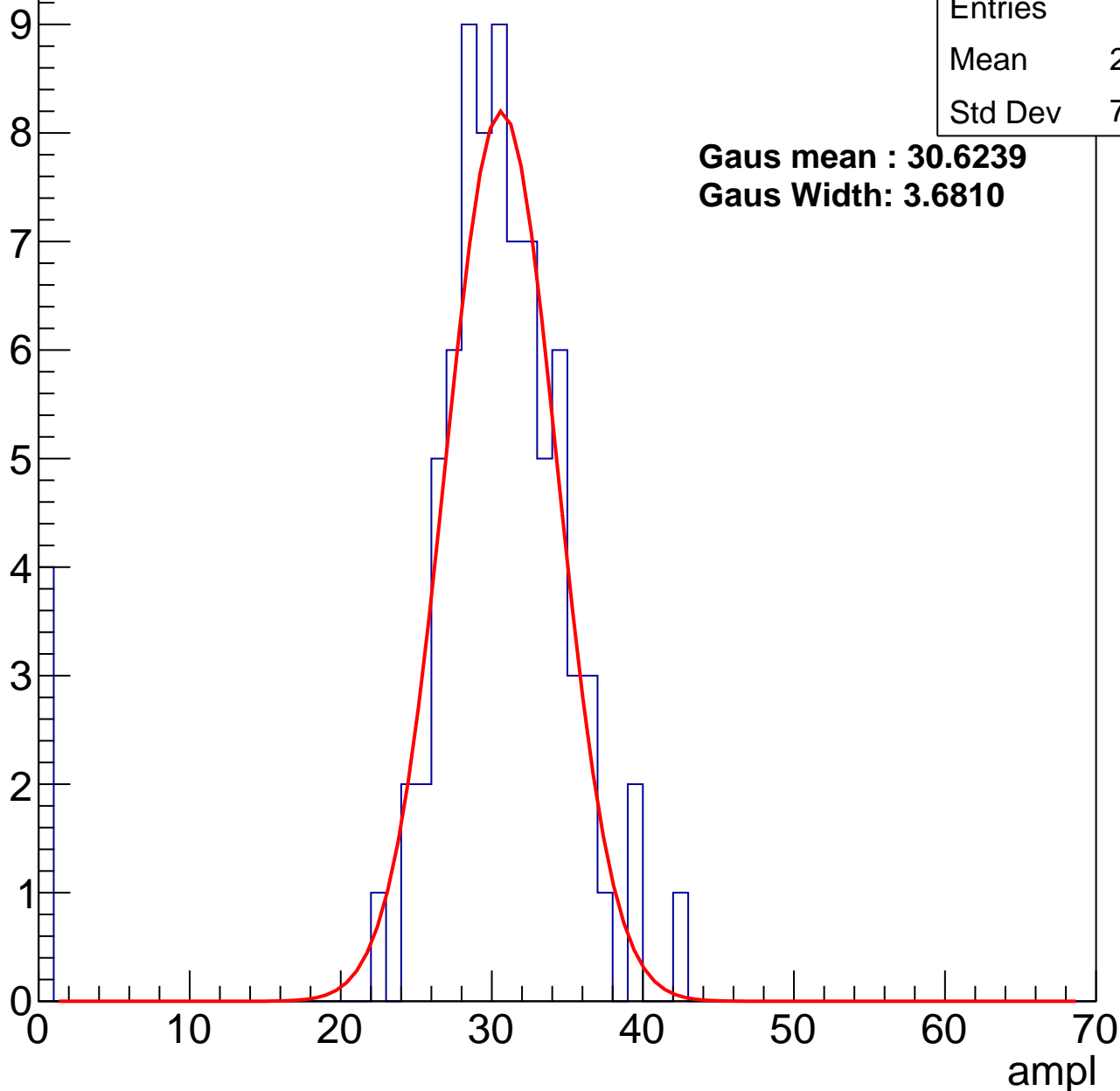
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	81
Mean	28.96
Std Dev	7.528

**Gaus mean : 30.6239**

**Gaus Width: 3.6810**



# B1L103S, U3-ch53, adc1

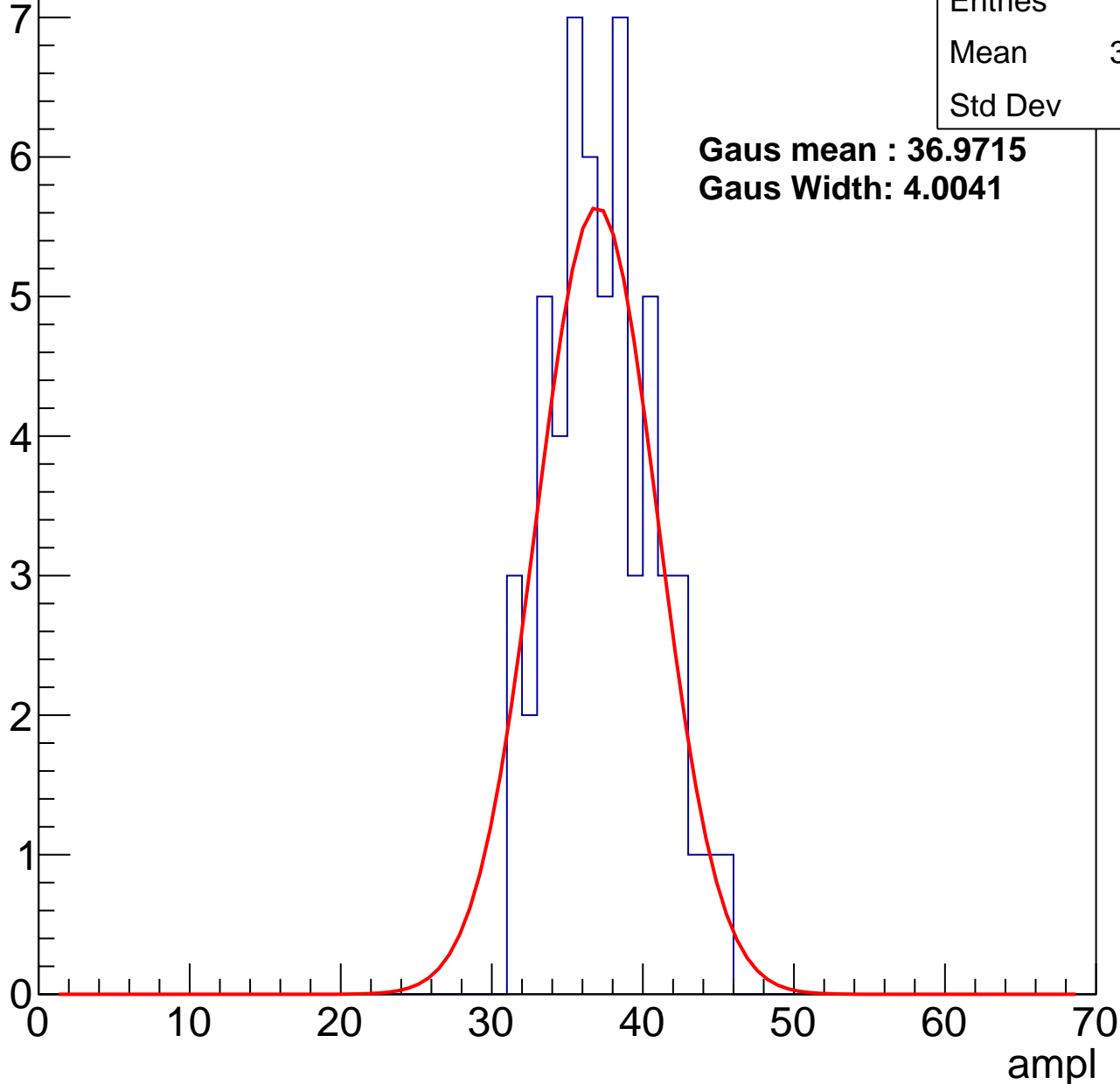
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	36.93
Std Dev	3.39

**Gaus mean : 36.9715**

**Gaus Width: 4.0041**



# B1L103S, U3-ch53, adc2

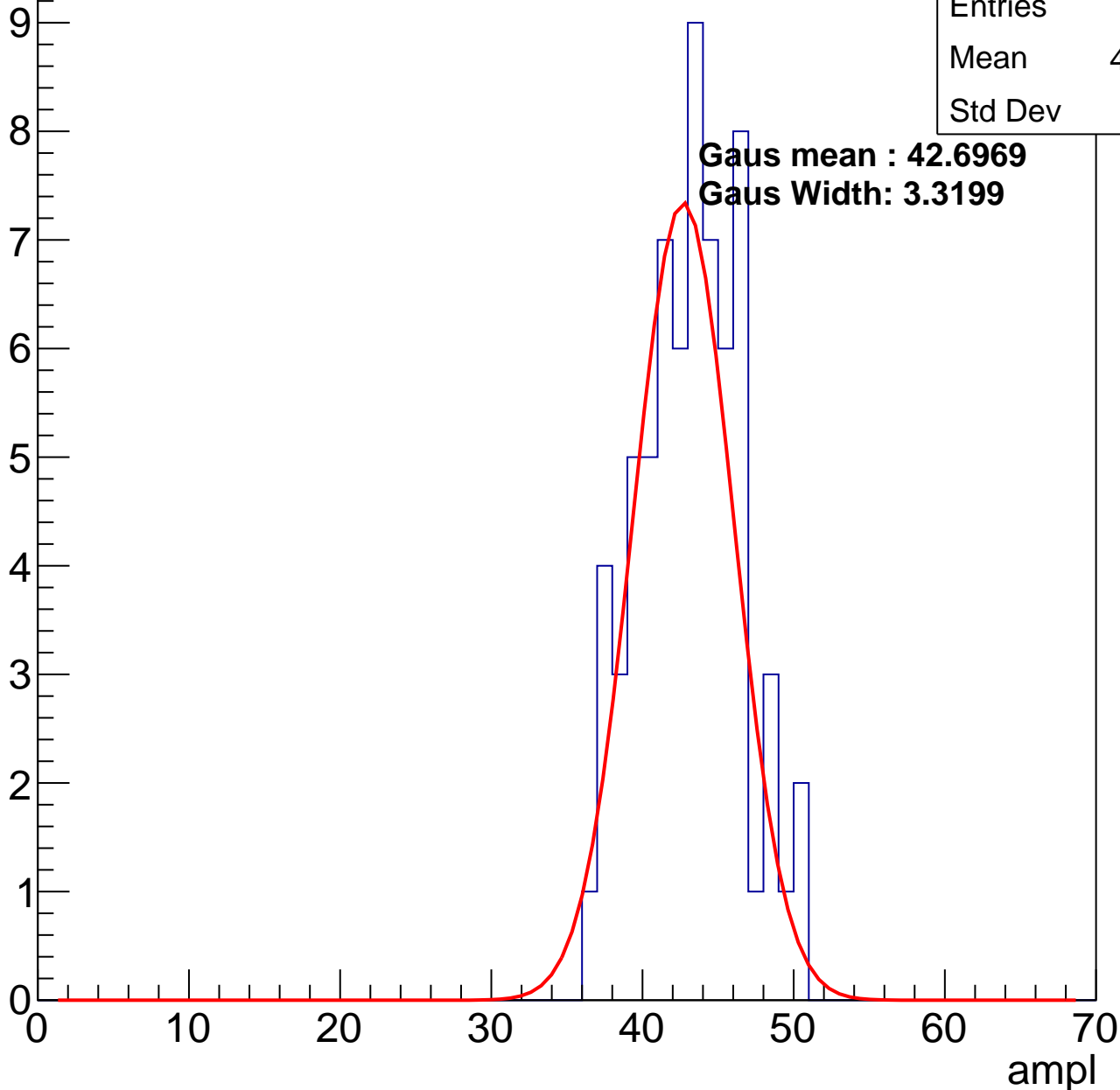
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	42.72
Std Dev	3.32

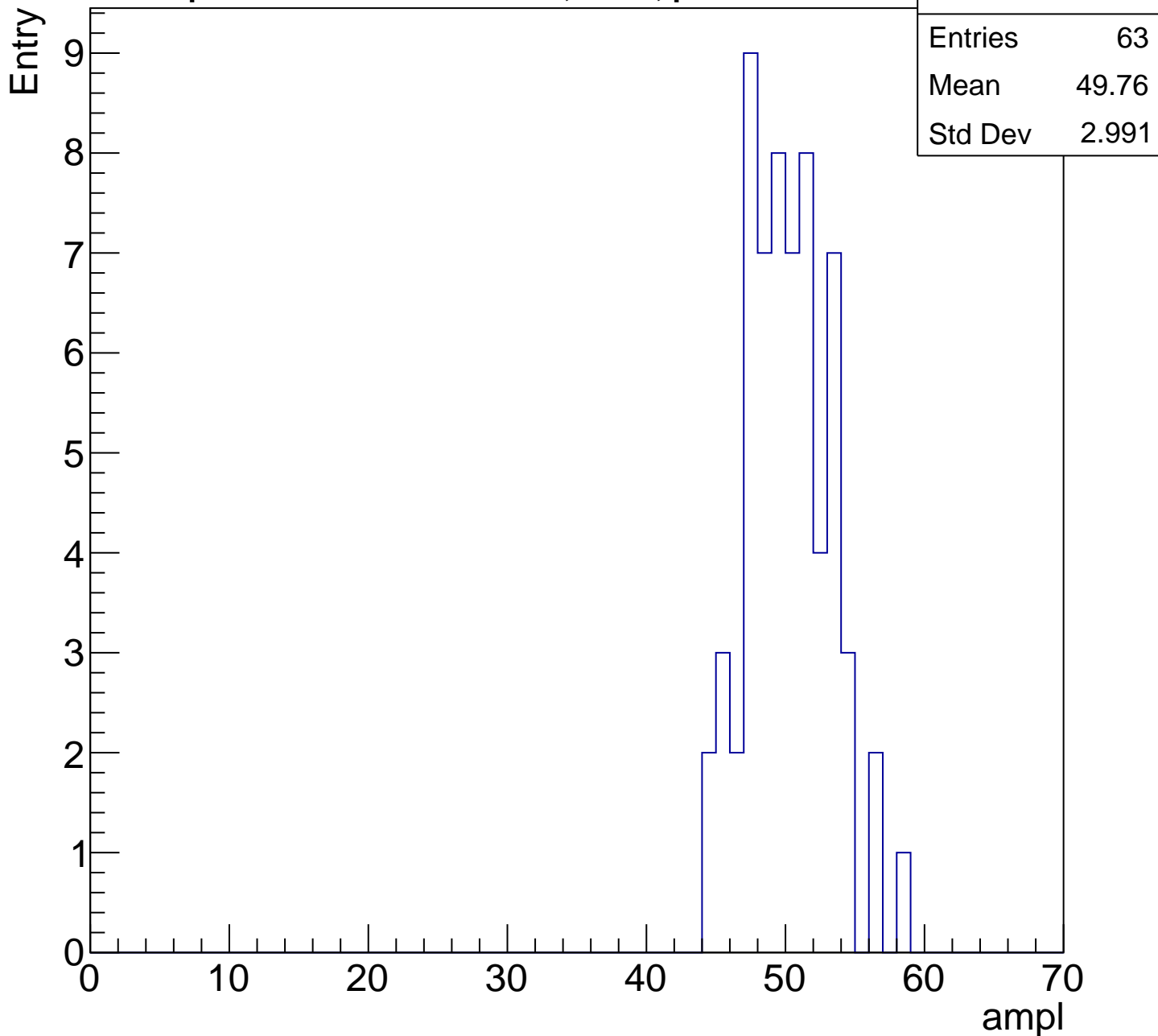
**Gaus mean : 42.6969**

**Gaus Width: 3.3199**



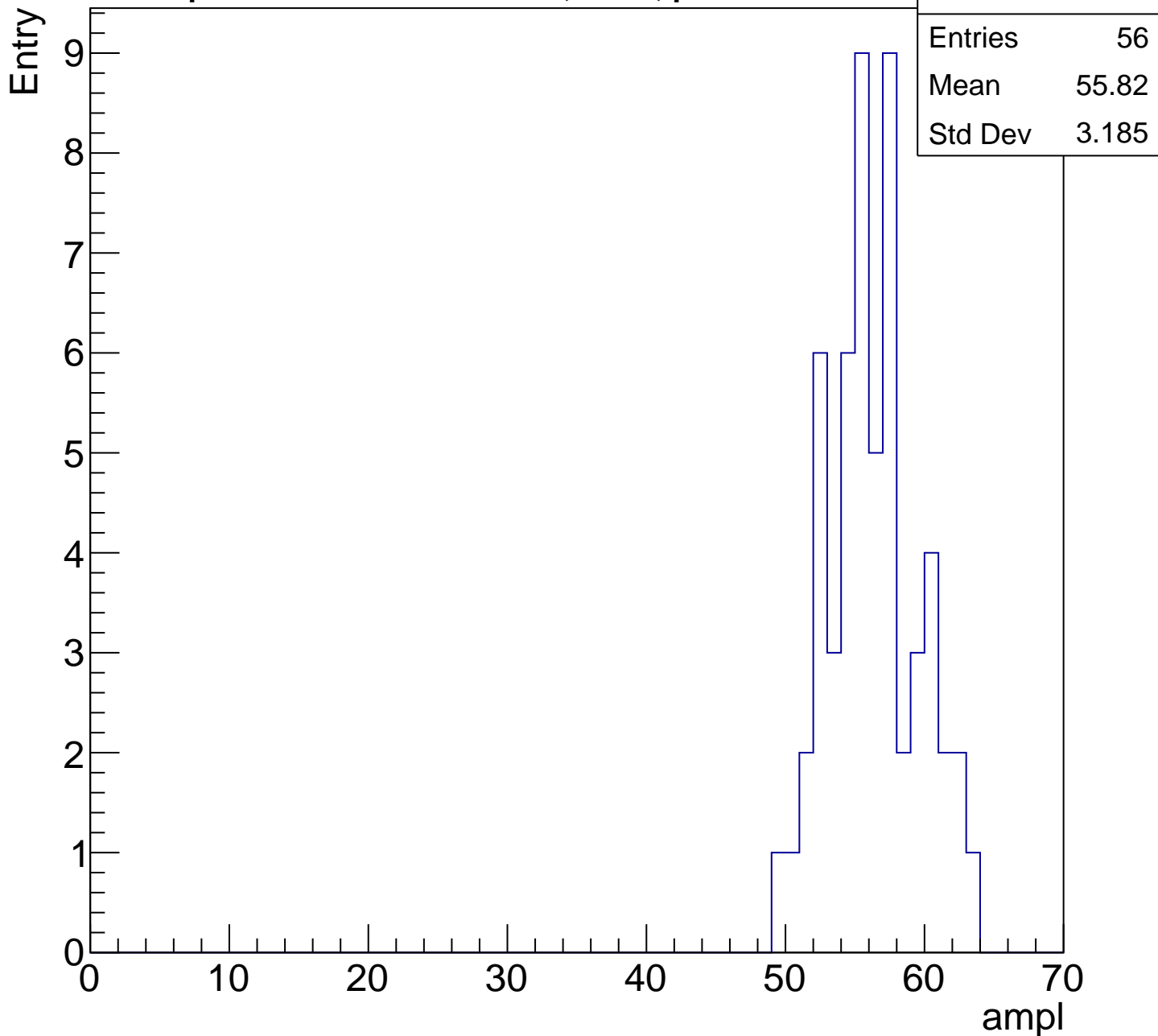
# B1L103S, U3-ch53, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2



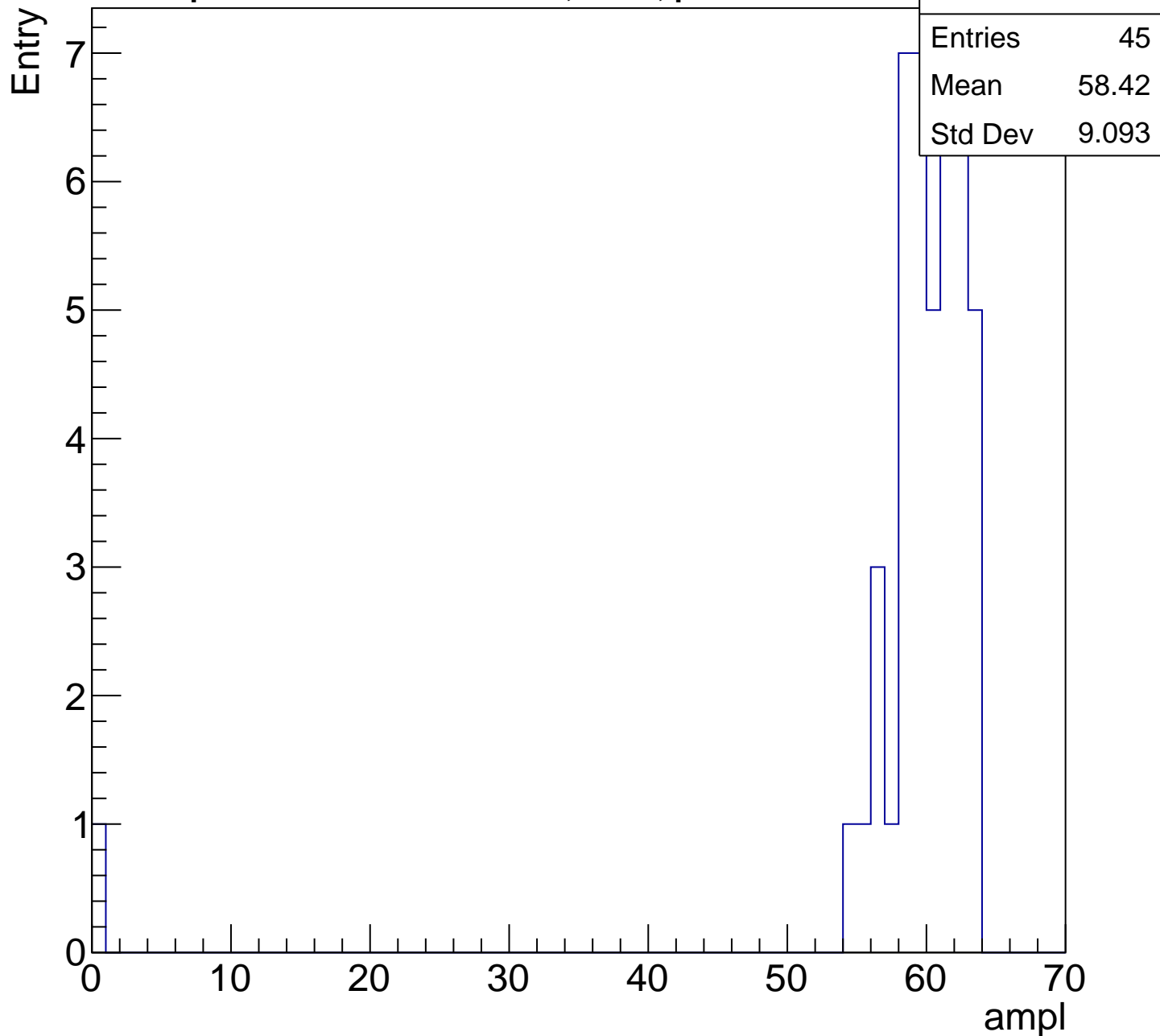
# B1L103S, U3-ch53, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U3-ch53, adc5

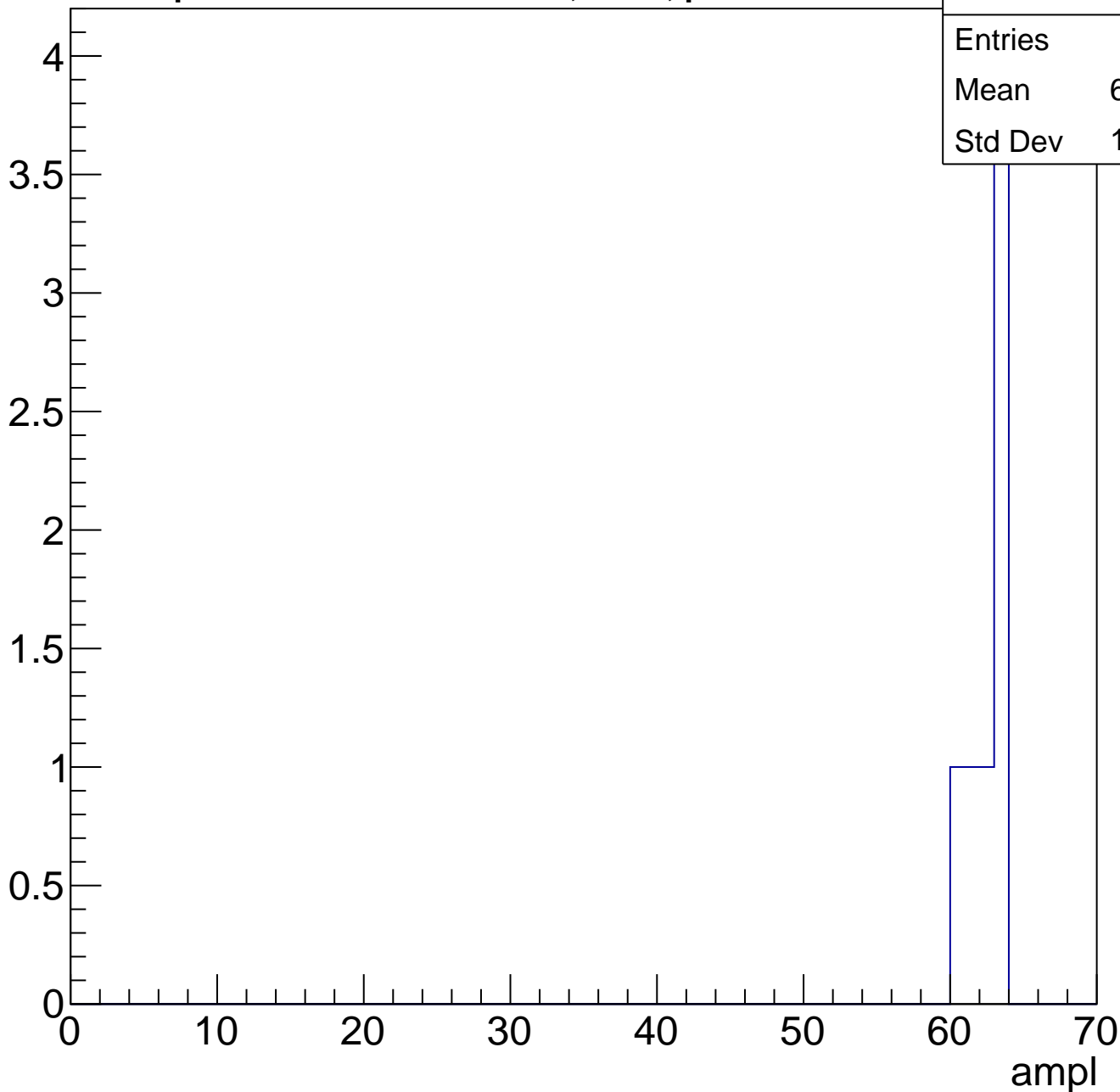
calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U3-ch53, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U3-ch53, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch54, adc0

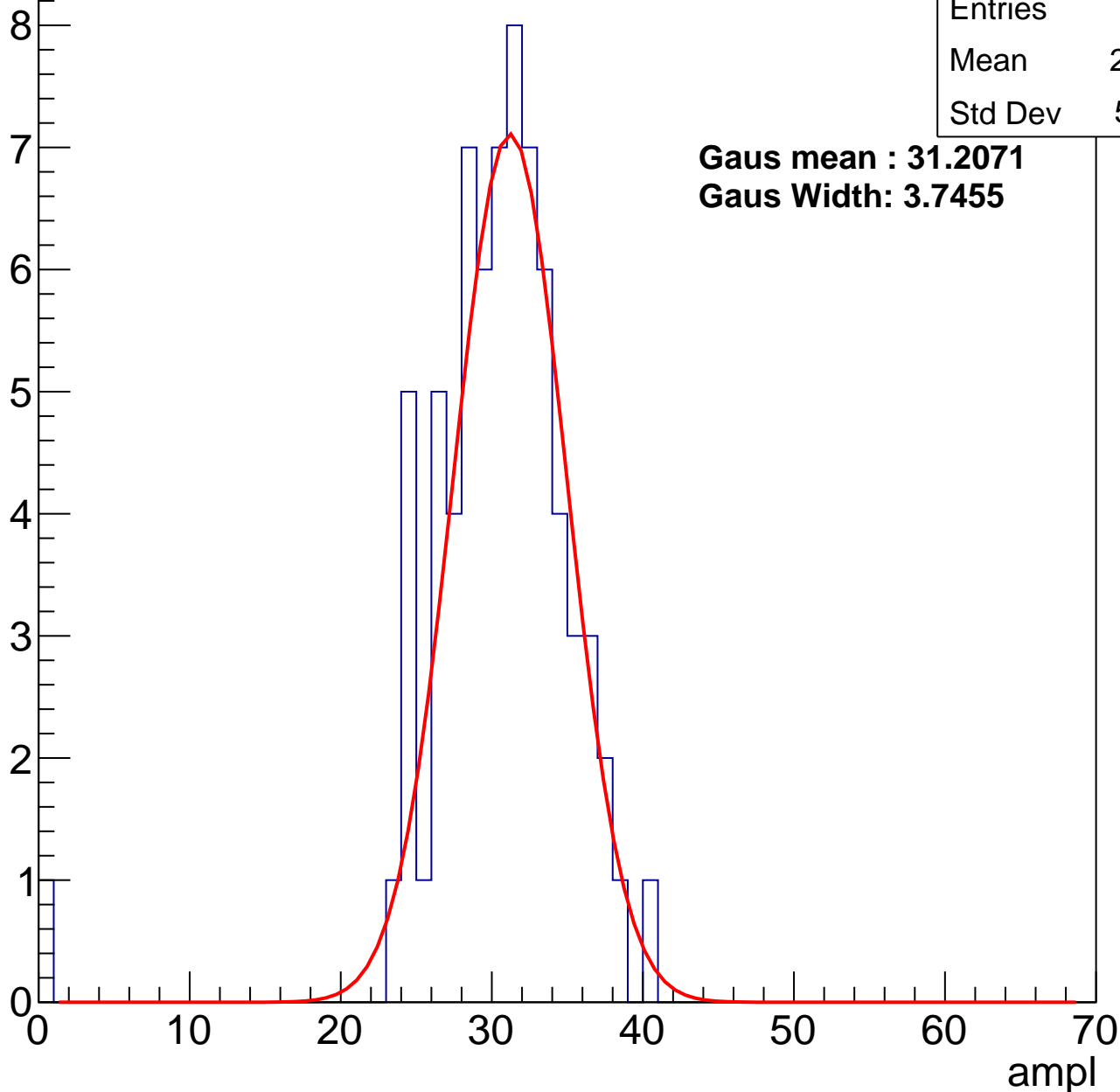
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	29.96
Std Dev	5.141

**Gaus mean : 31.2071**

**Gaus Width: 3.7455**



# B1L103S, U3-ch54, adc1

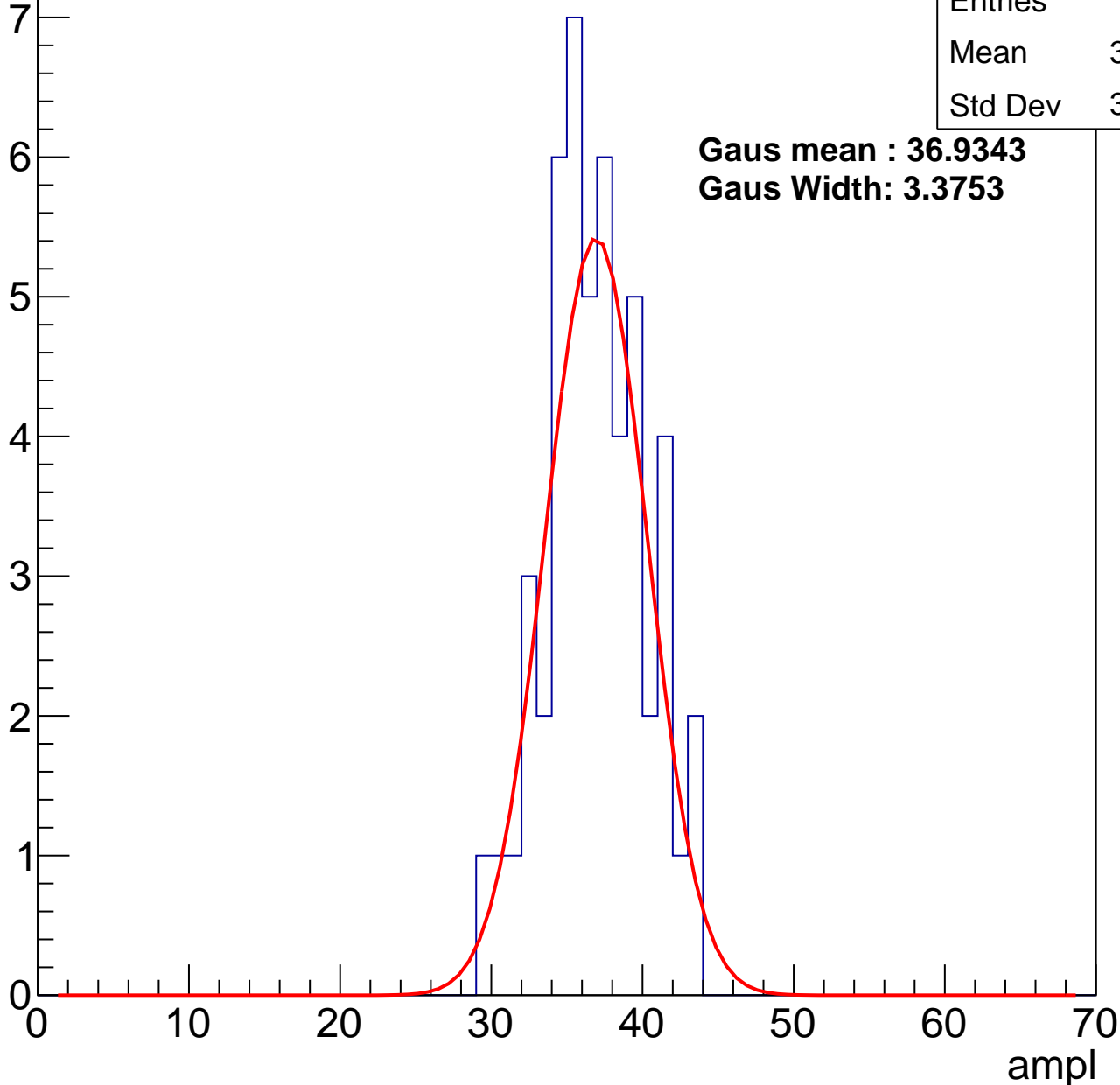
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	36.44
Std Dev	3.257

**Gaus mean : 36.9343**

**Gaus Width: 3.3753**



# B1L103S, U3-ch54, adc2

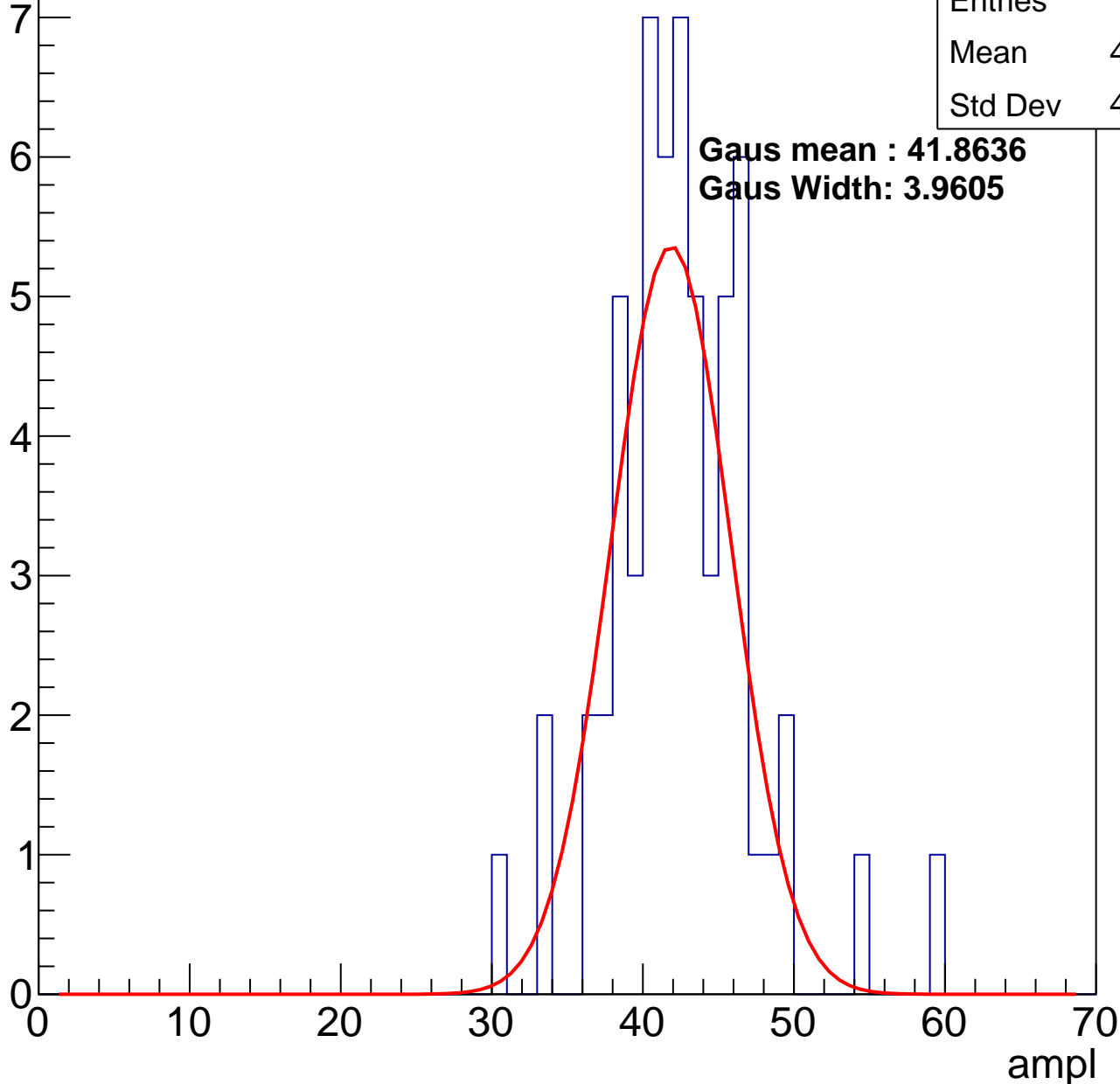
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	42.05
Std Dev	4.688

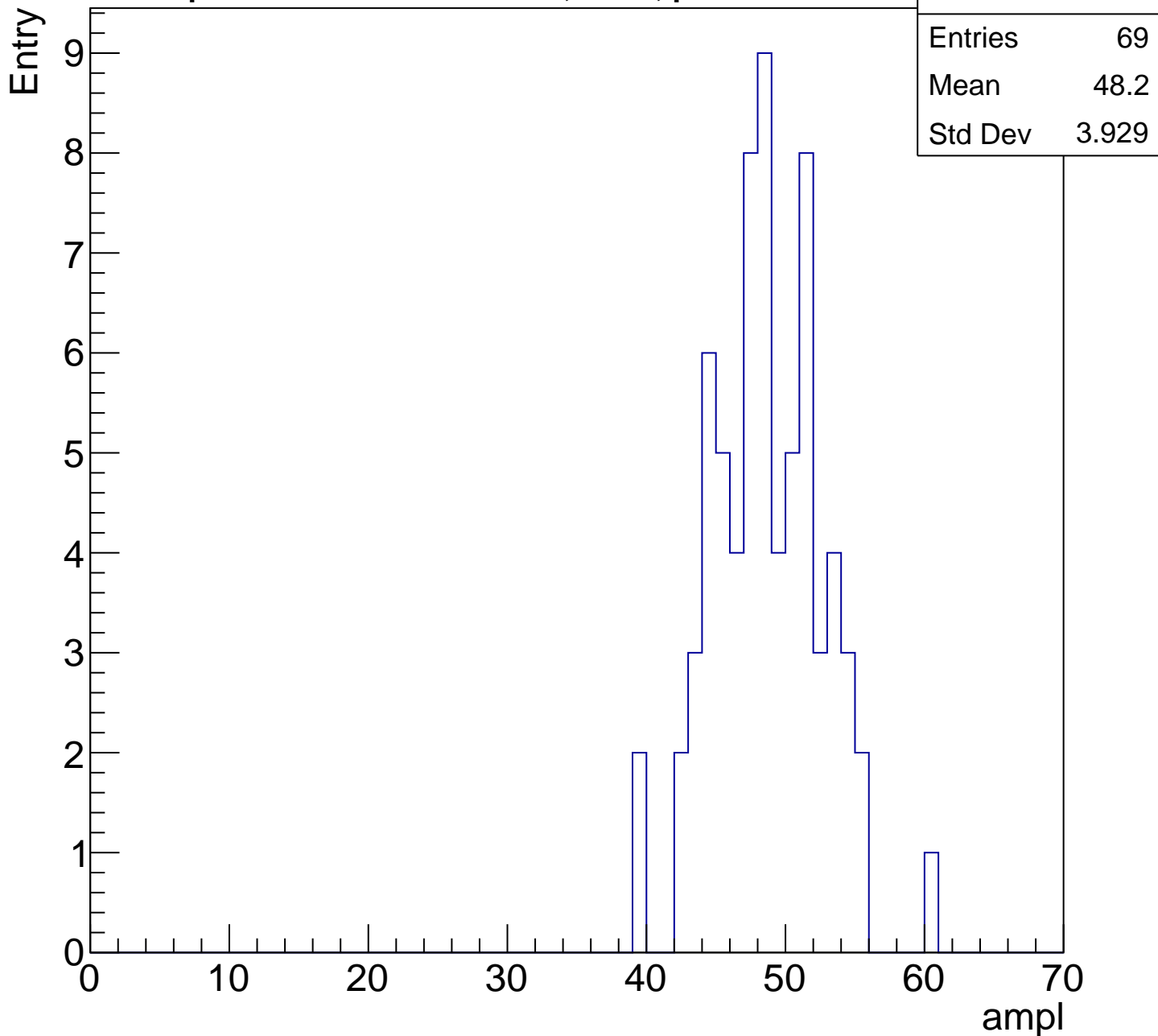
**Gaus mean : 41.8636**

**Gaus Width: 3.9605**



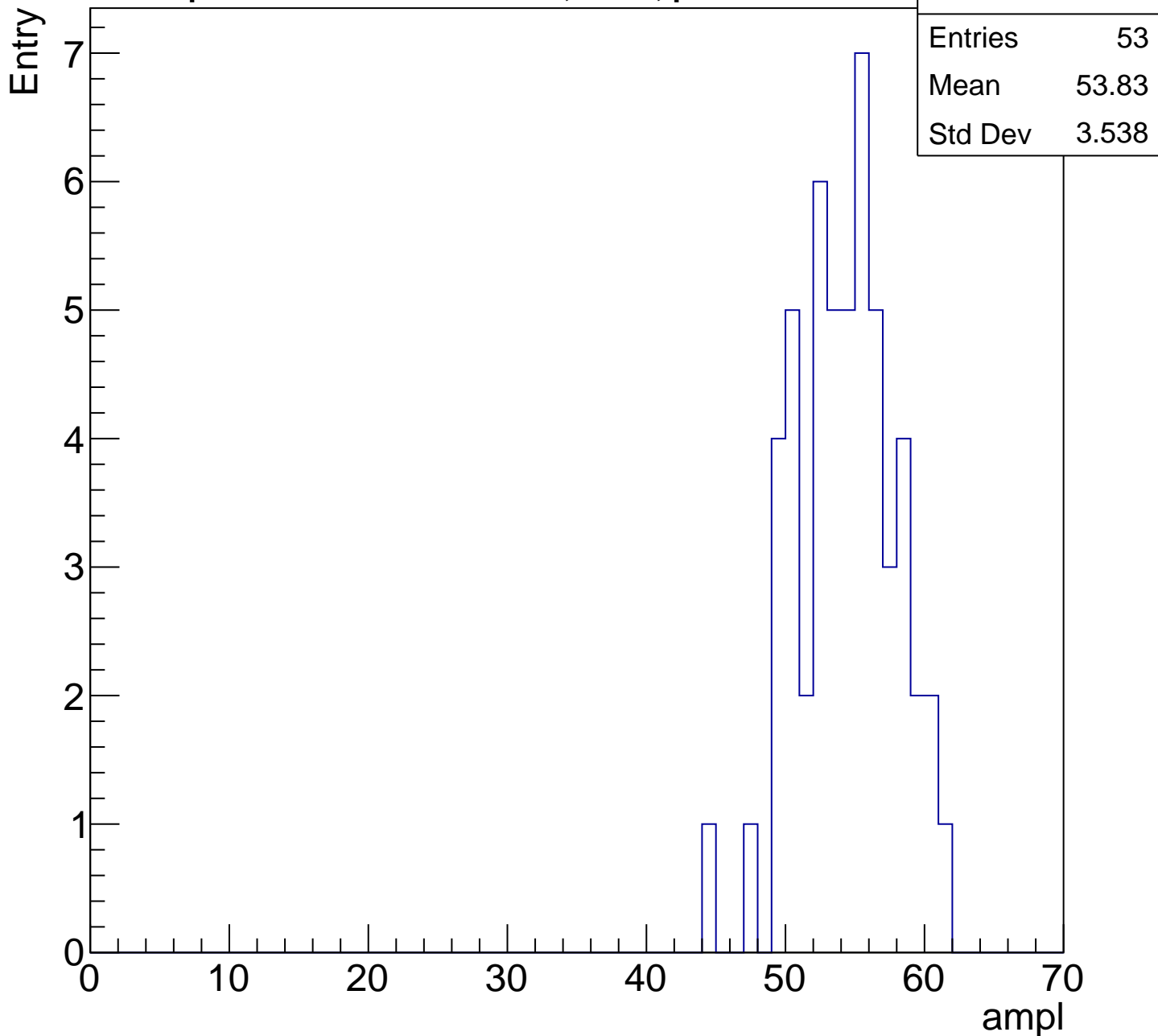
# B1L103S, U3-ch54, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U3-ch54, adc4

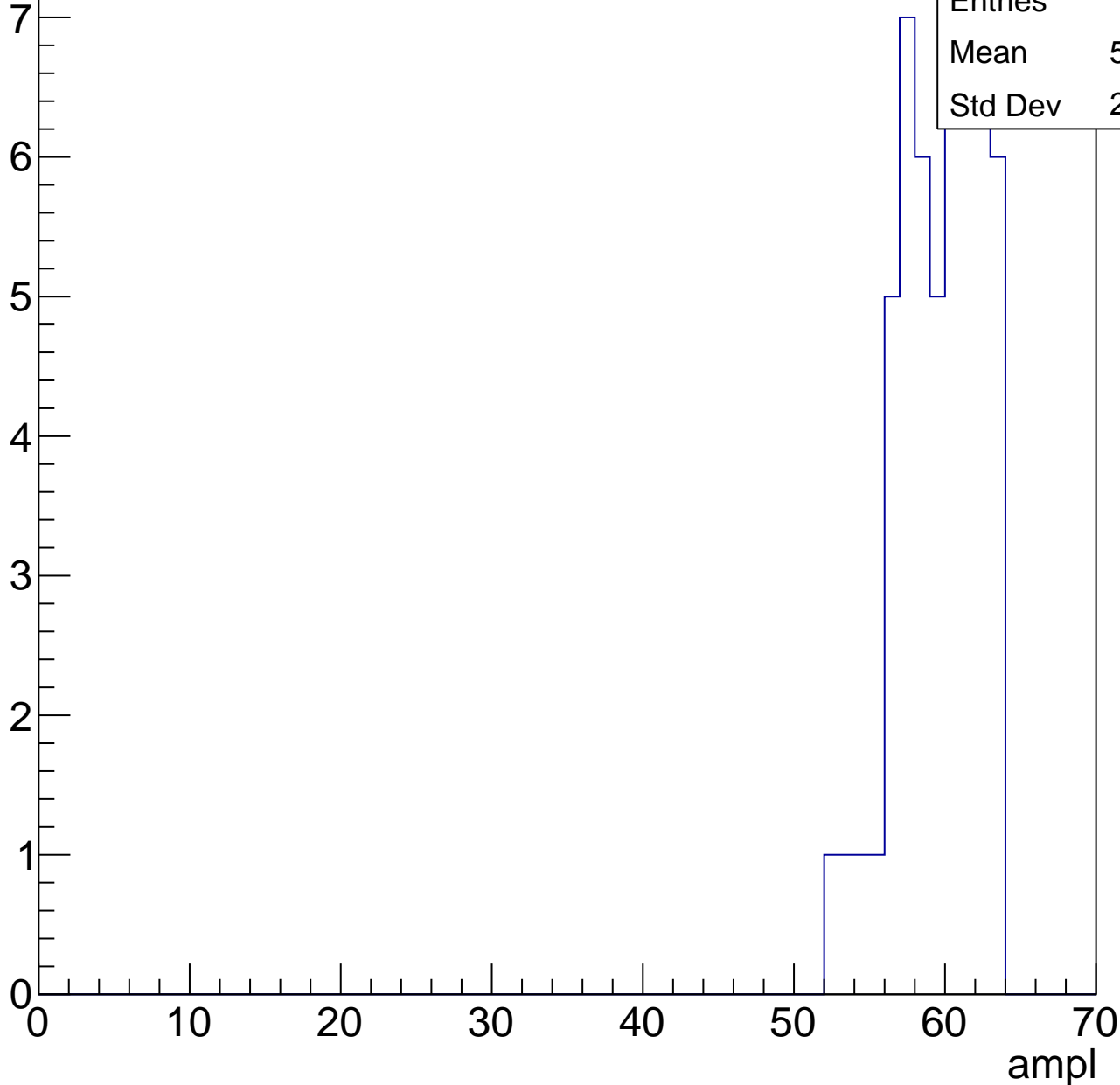
calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U3-ch54, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

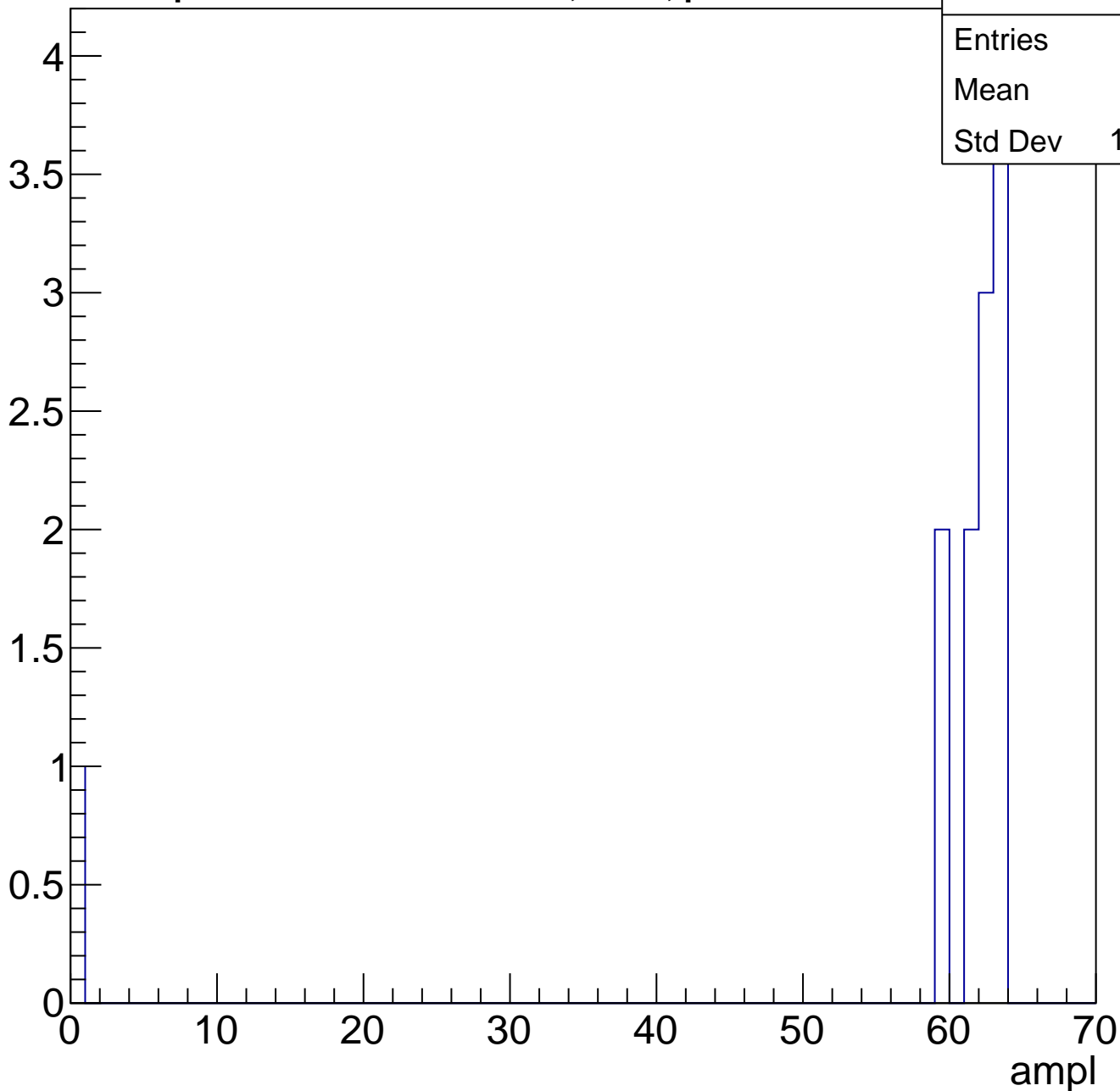


Entries	54
Mean	59.17
Std Dev	2.713

# B1L103S, U3-ch54, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U3-ch54, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U3-ch55, adc0

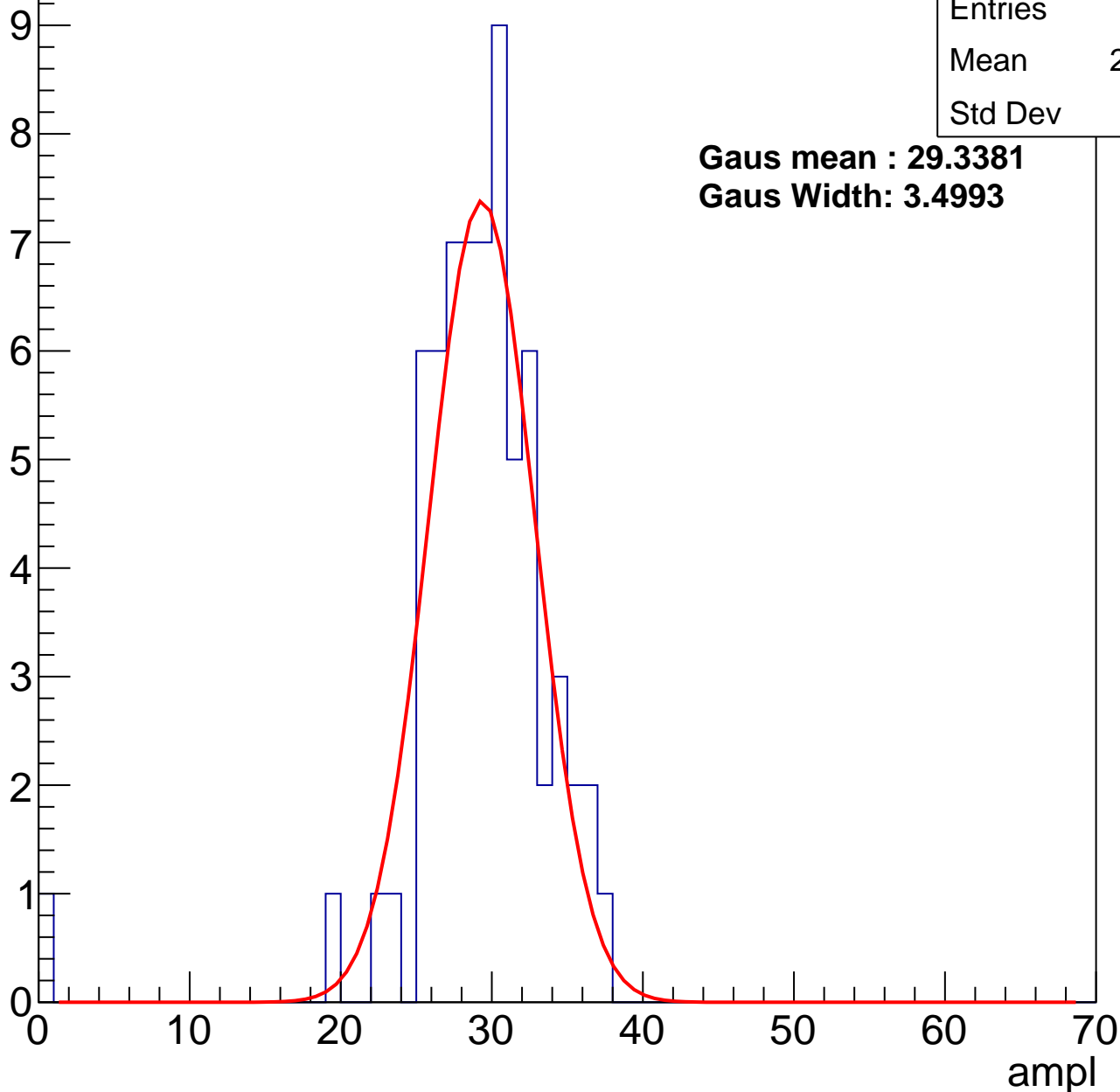
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	28.69
Std Dev	4.93

**Gaus mean : 29.3381**

**Gaus Width: 3.4993**



# B1L103S, U3-ch55, adc1

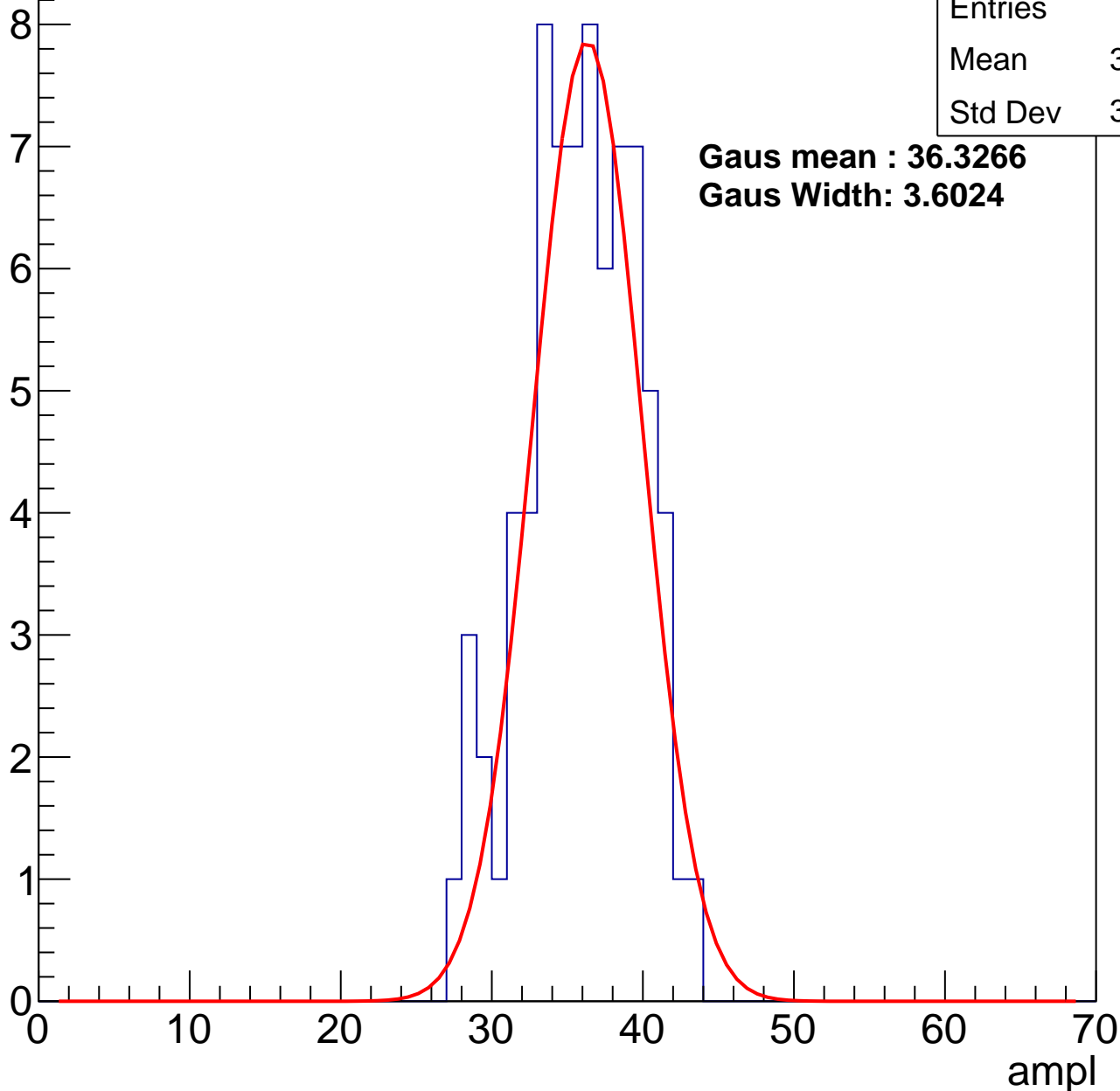
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	35.47
Std Dev	3.662

**Gaus mean : 36.3266**

**Gaus Width: 3.6024**



# B1L103S, U3-ch55, adc2

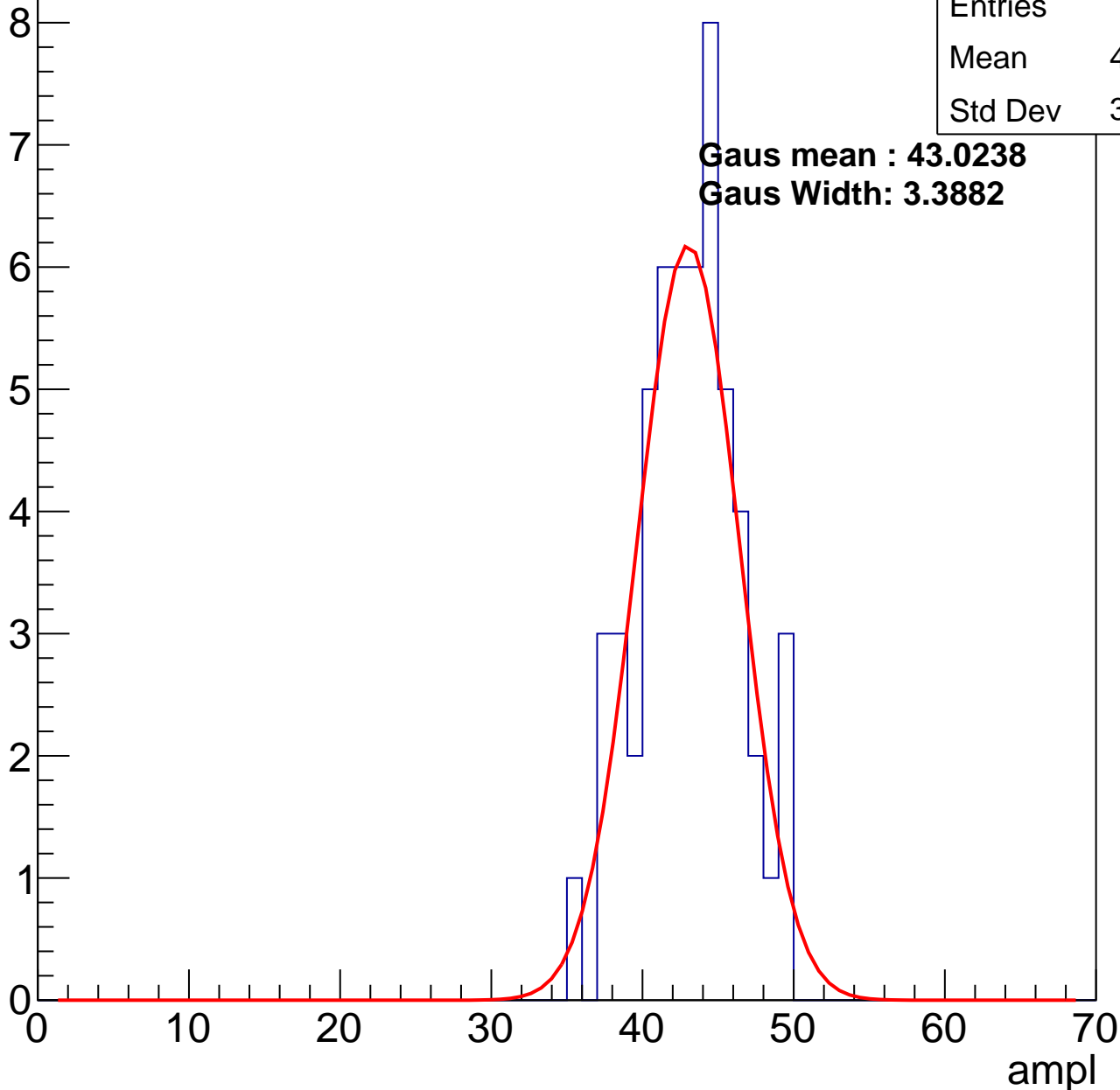
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	42.62
Std Dev	3.233

**Gaus mean : 43.0238**

**Gaus Width: 3.3882**

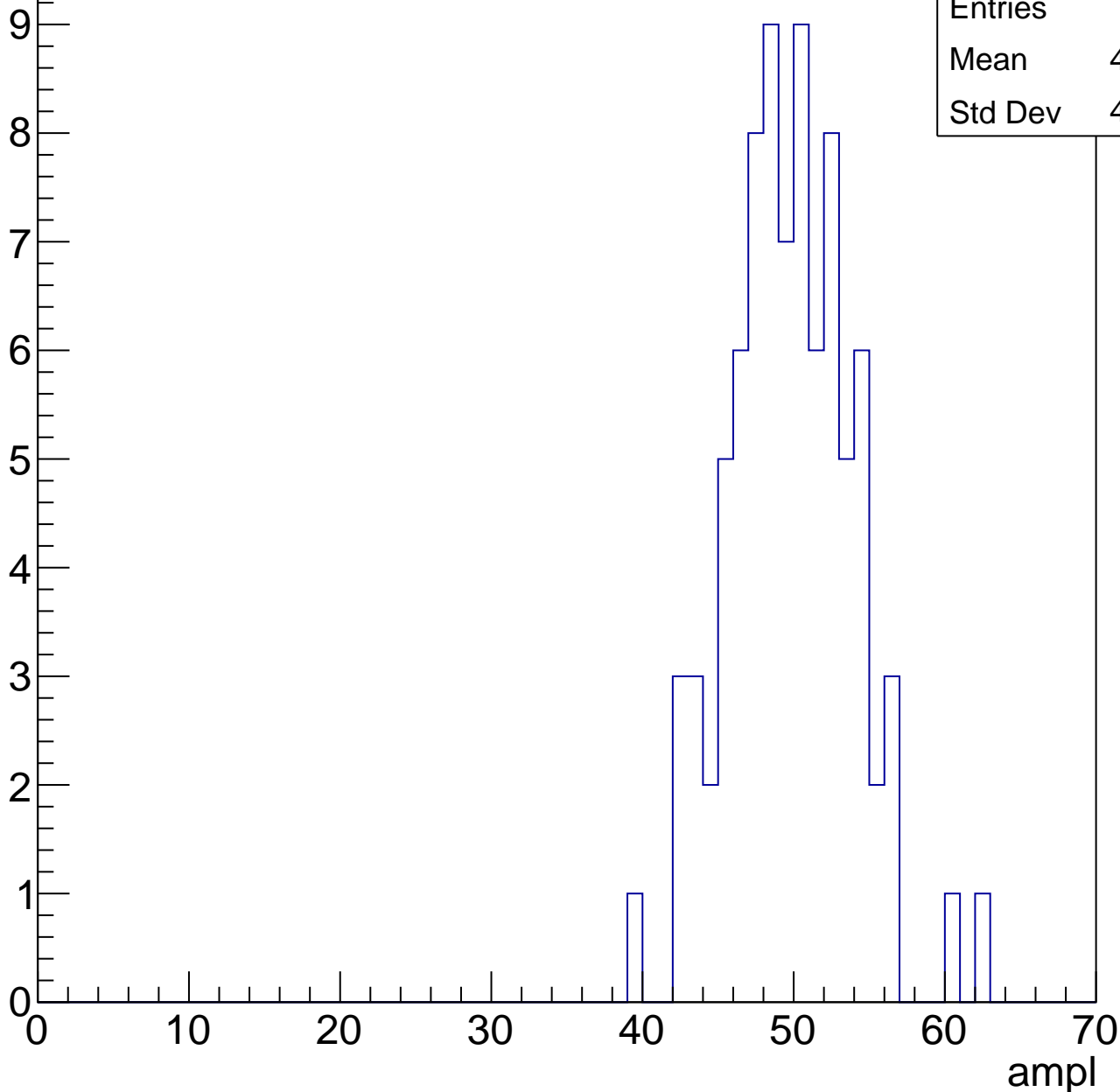


# B1L103S, U3-ch55, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

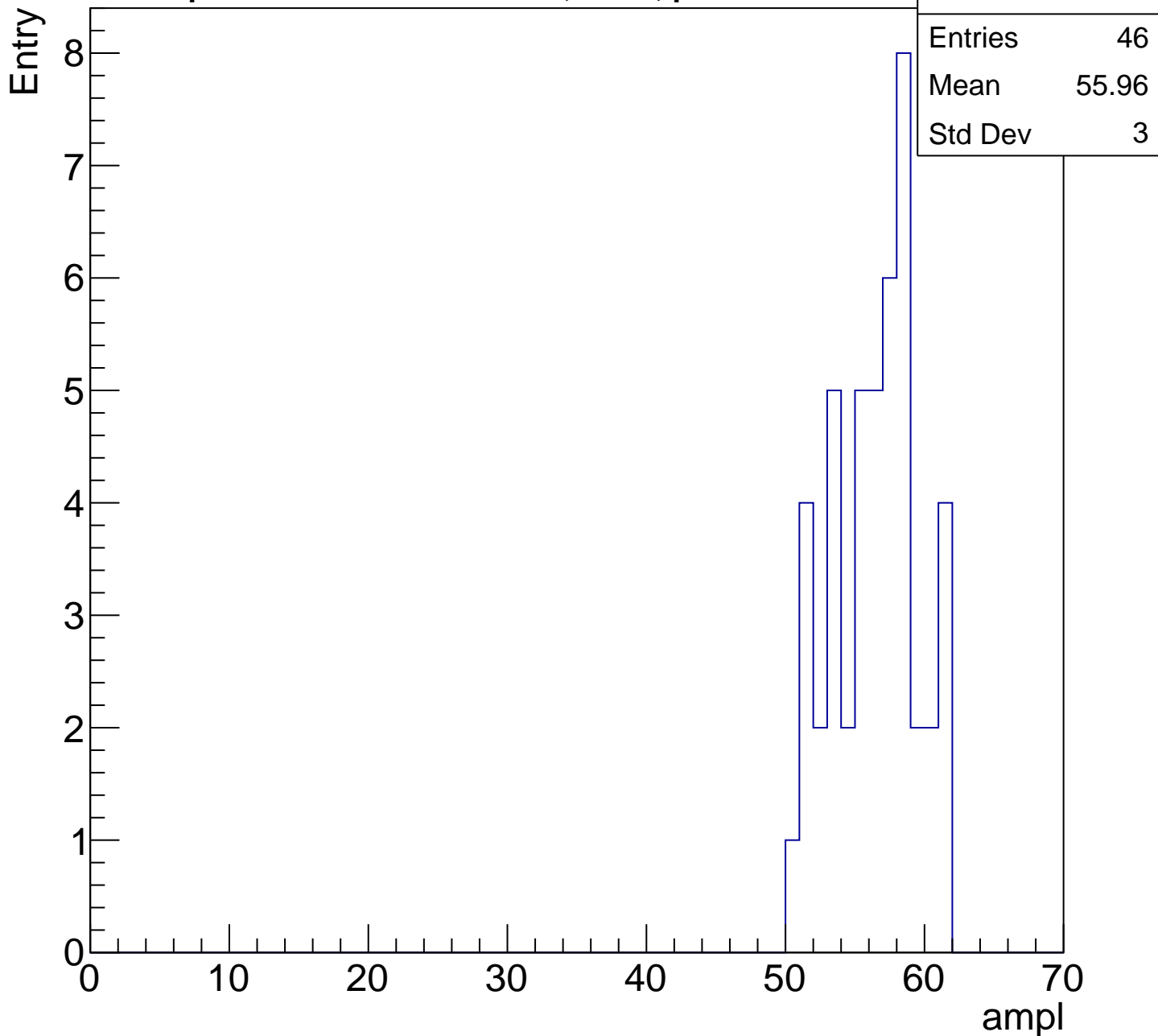
Entry

Entries	85
Mean	49.35
Std Dev	4.078



# B1L103S, U3-ch55, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

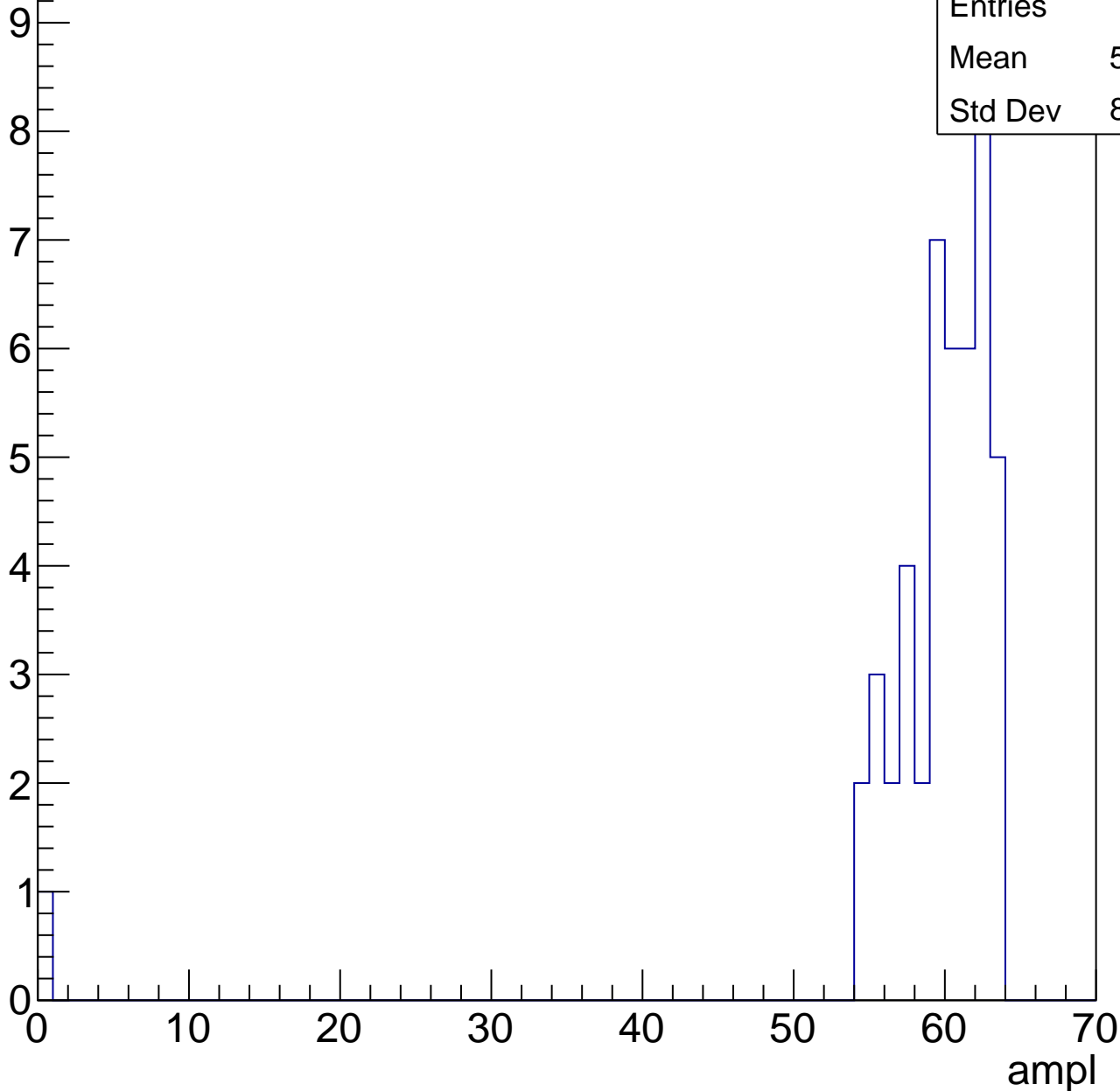


# B1L103S, U3-ch55, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	47
Mean	58.32
Std Dev	8.973

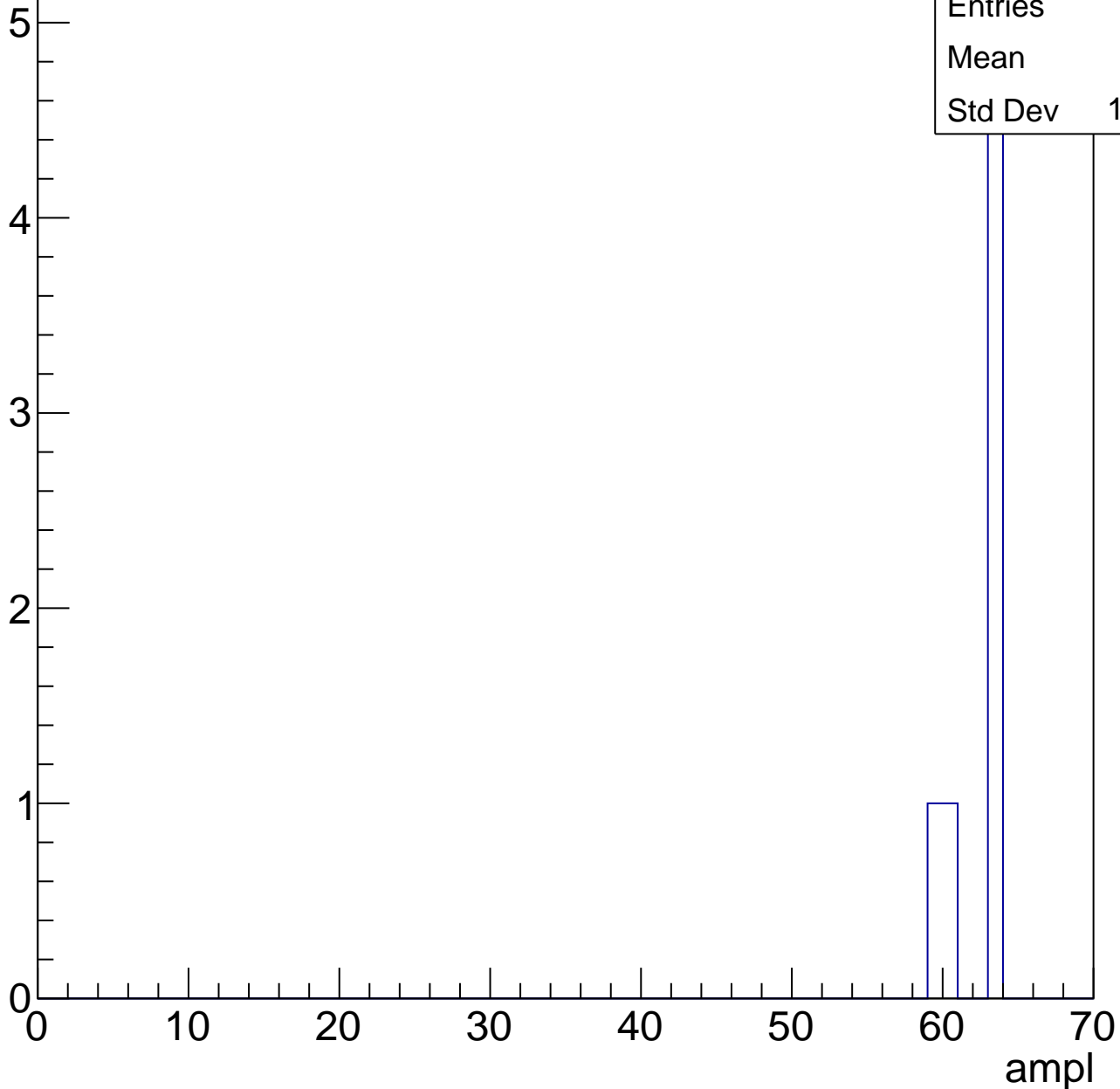


# B1L103S, U3-ch55, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	7
Mean	62
Std Dev	1.604





# B1L103S, U3-ch55, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch56, adc0

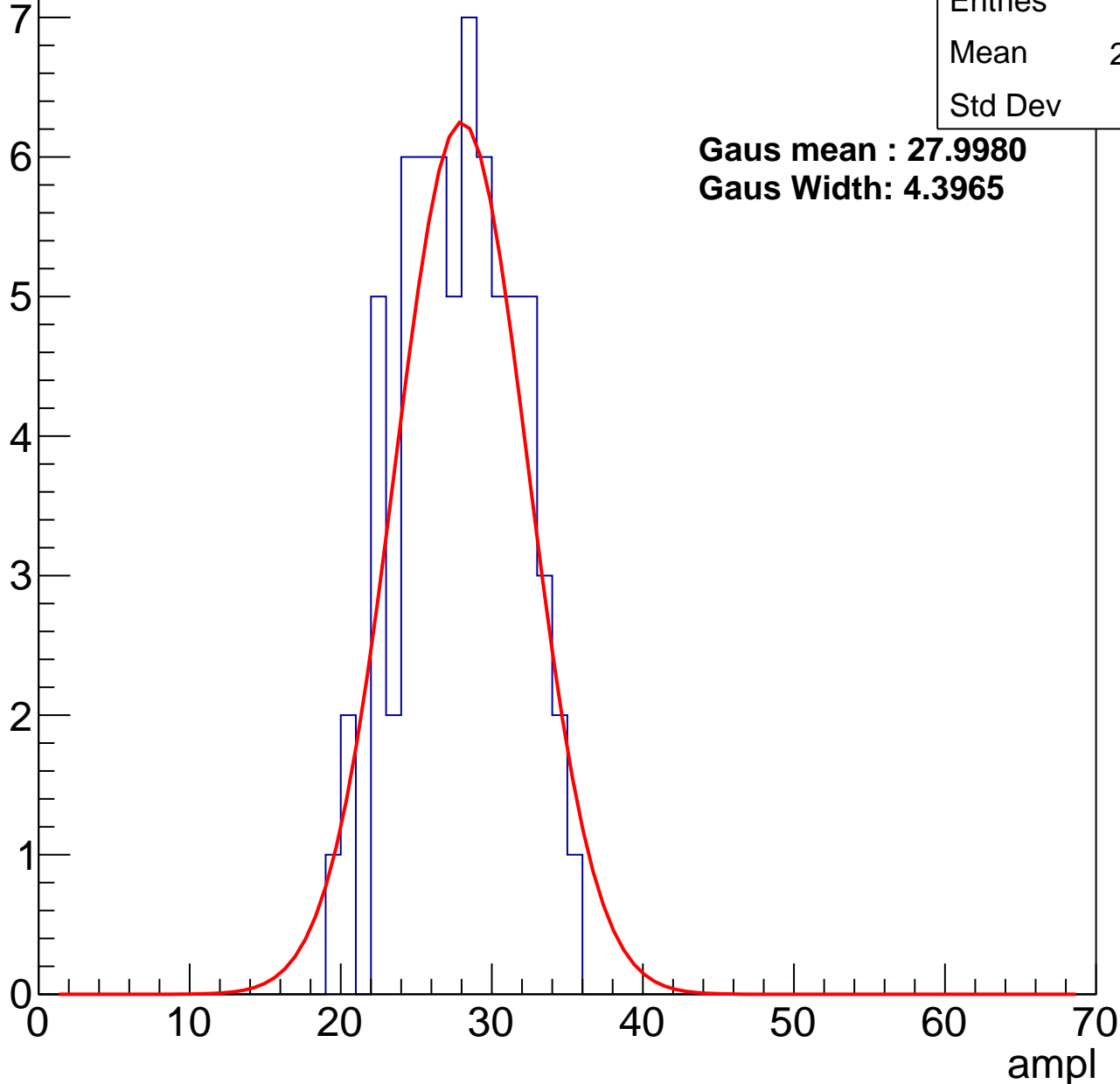
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	27.42
Std Dev	3.75

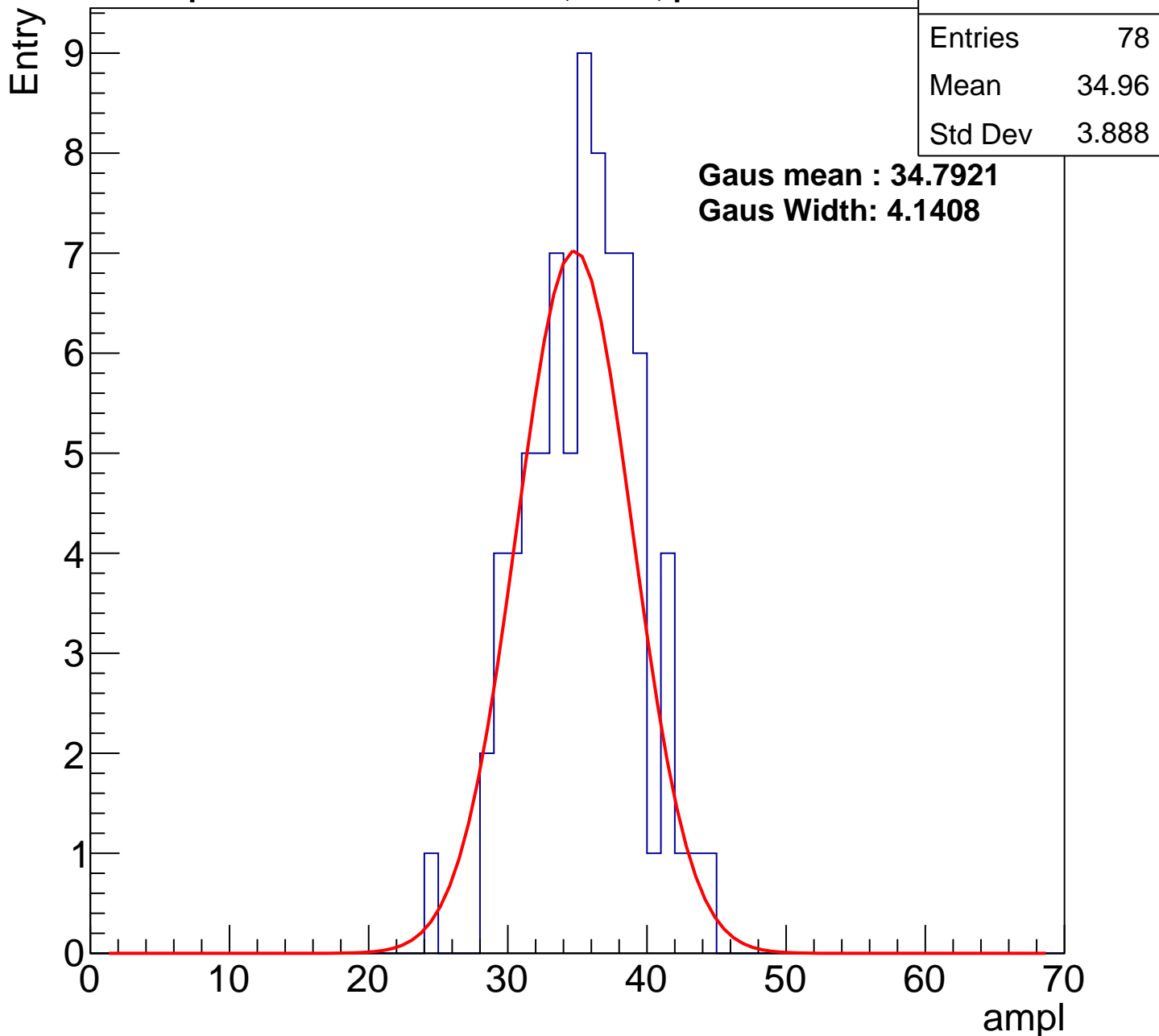
**Gaus mean : 27.9980**

**Gaus Width: 4.3965**



# B1L103S, U3-ch56, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U3-ch56, adc2

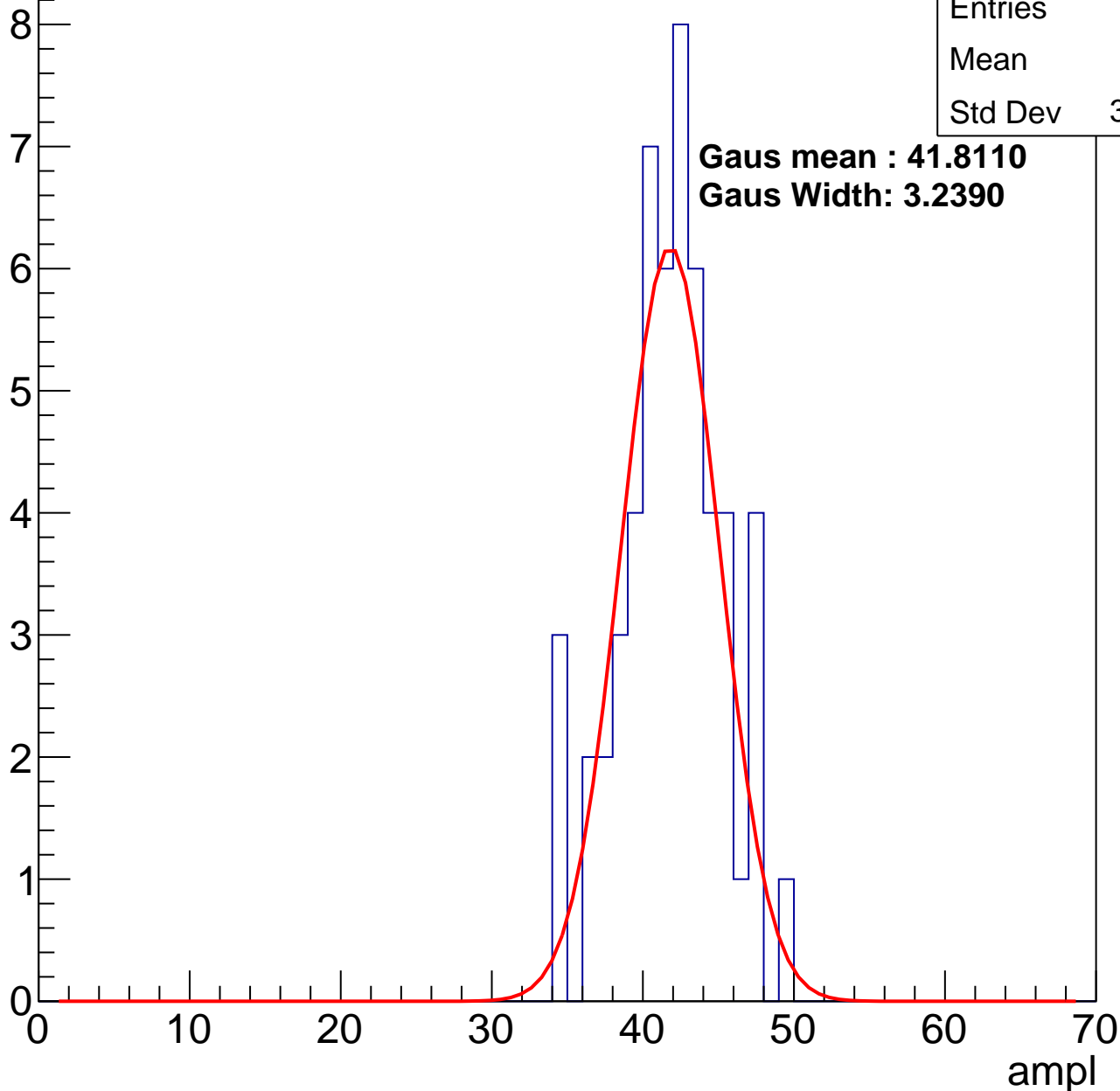
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	41.4
Std Dev	3.398

**Gaus mean : 41.8110**

**Gaus Width: 3.2390**

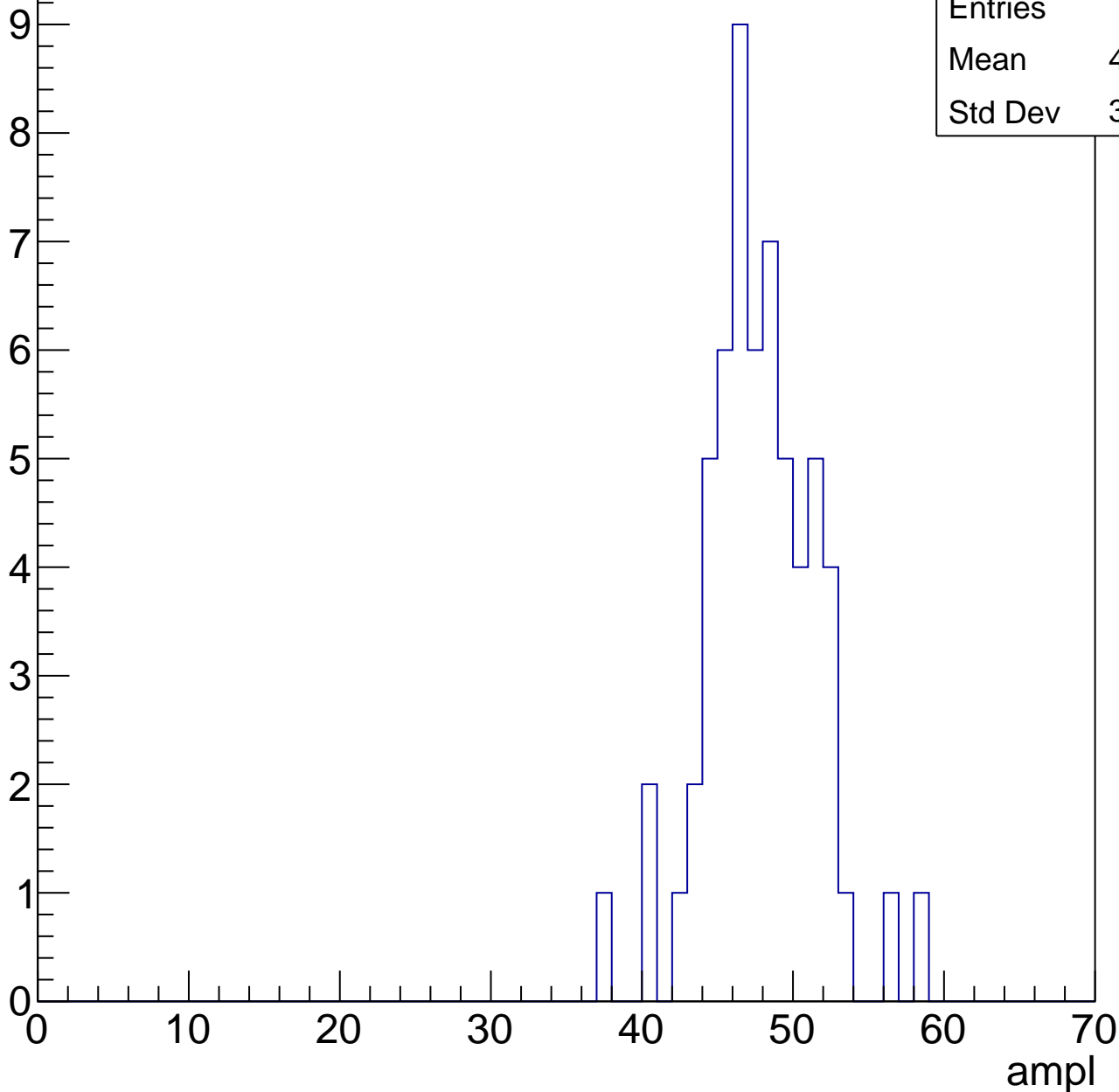


# B1L103S, U3-ch56, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

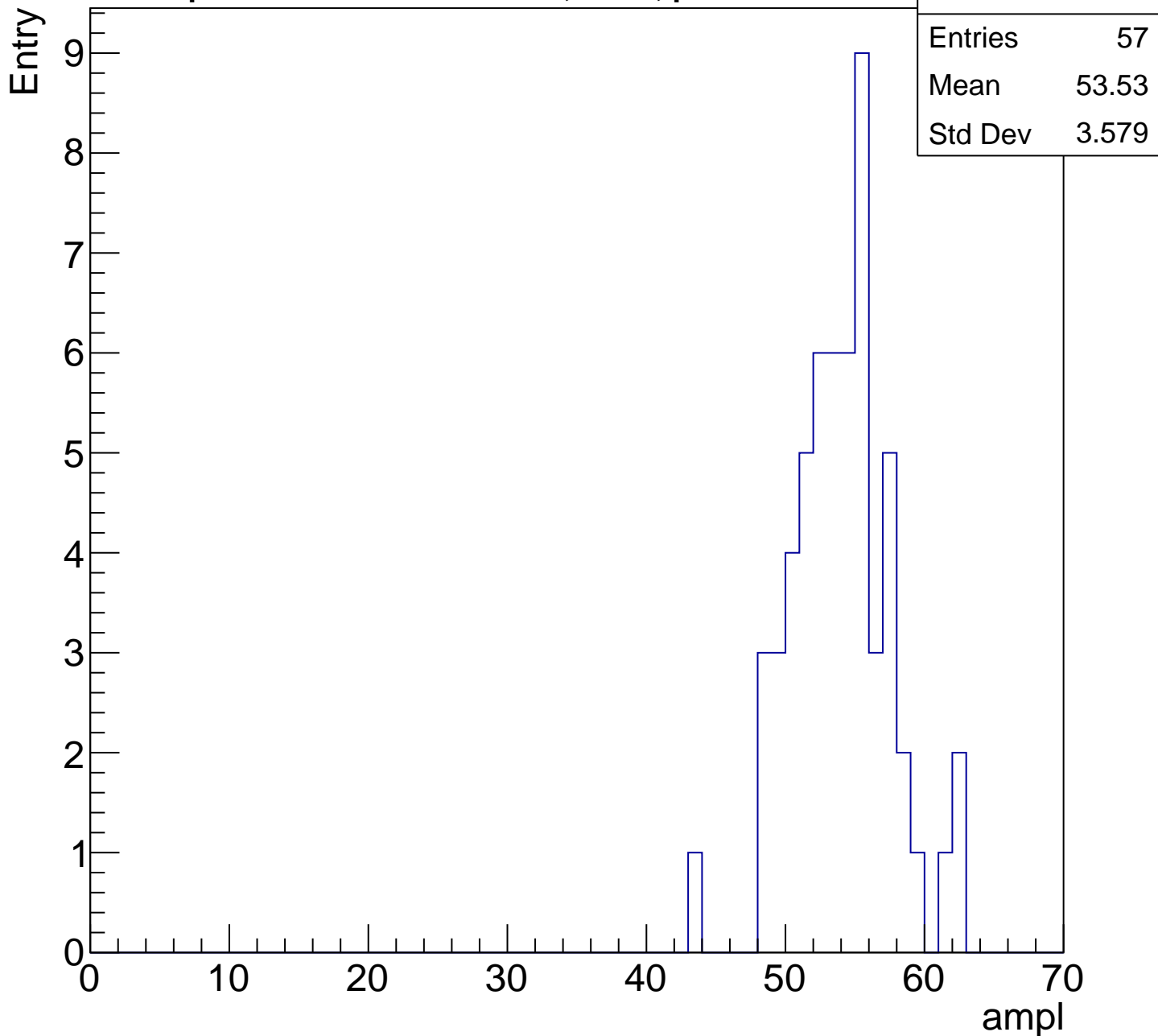
Entry

Entries	60
Mean	47.37
Std Dev	3.665



# B1L103S, U3-ch56, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

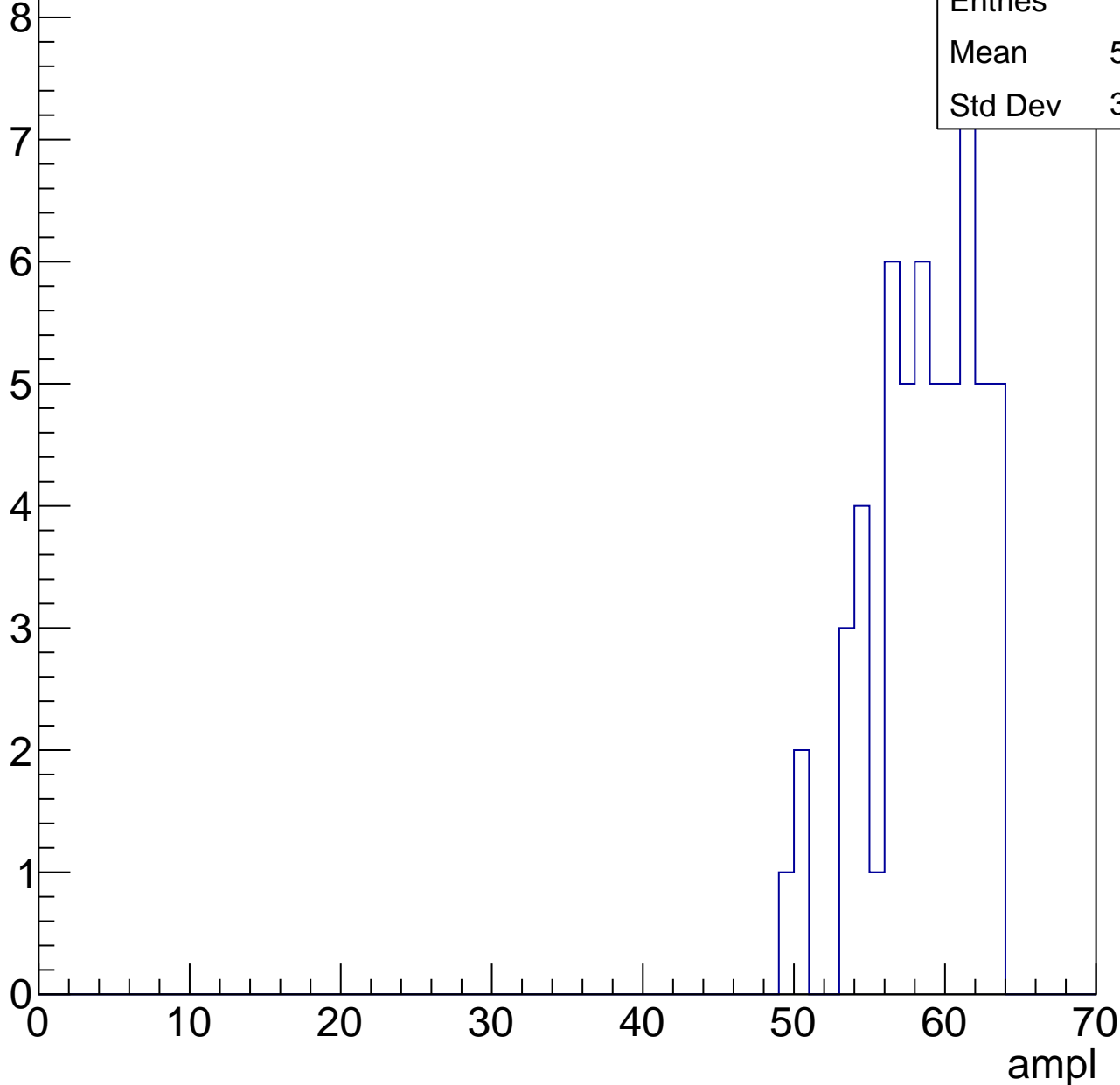


# B1L103S, U3-ch56, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	58.14
Std Dev	3.502

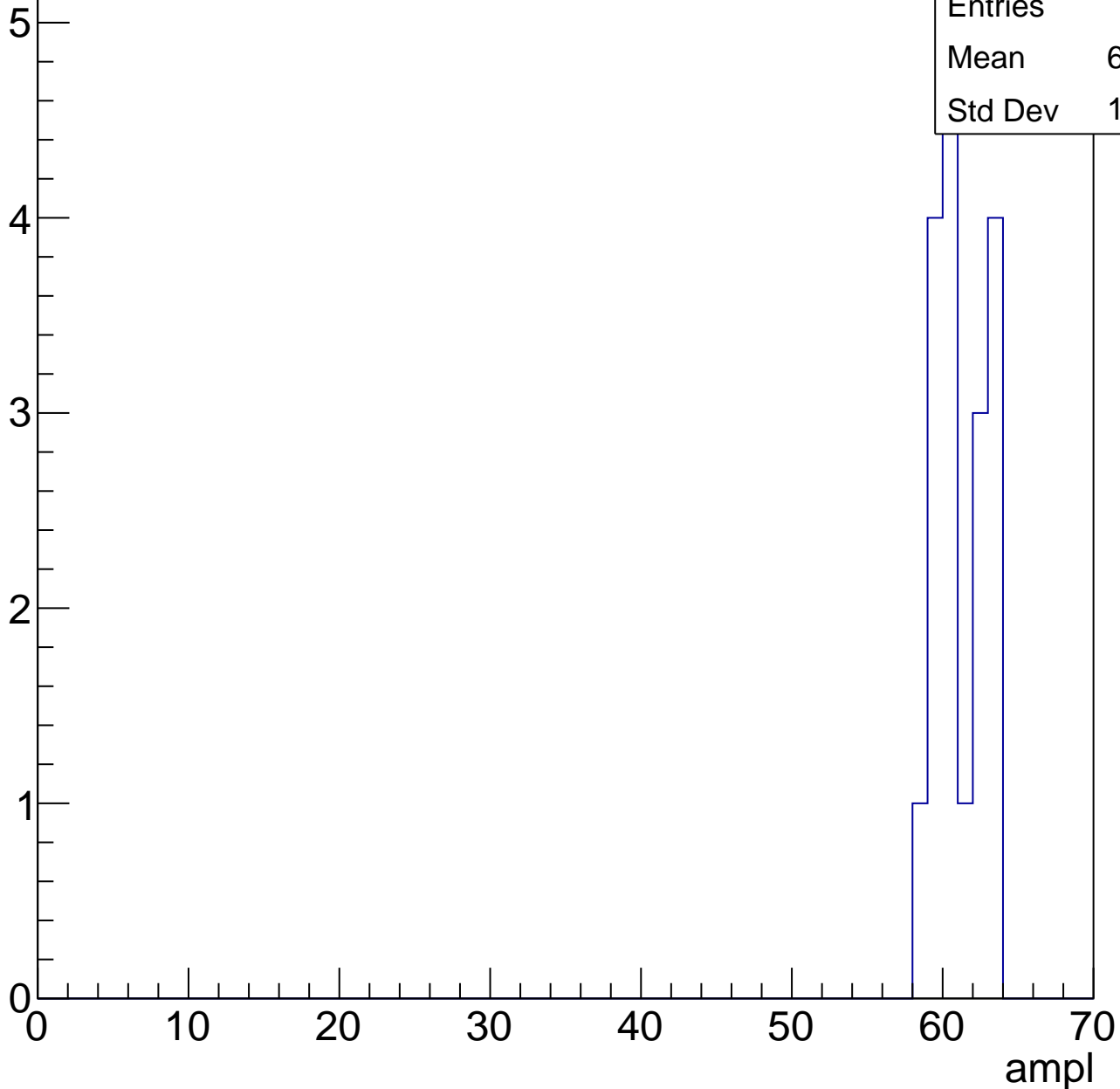


# B1L103S, U3-ch56, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	18
Mean	60.72
Std Dev	1.626





# B1L103S, U3-ch56, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	3
Mean	21
Std Dev	29.7

# B1L103S, U3-ch57, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	76
Mean	28.78
Std Dev	5.028

**Gaus mean : 29.0423**

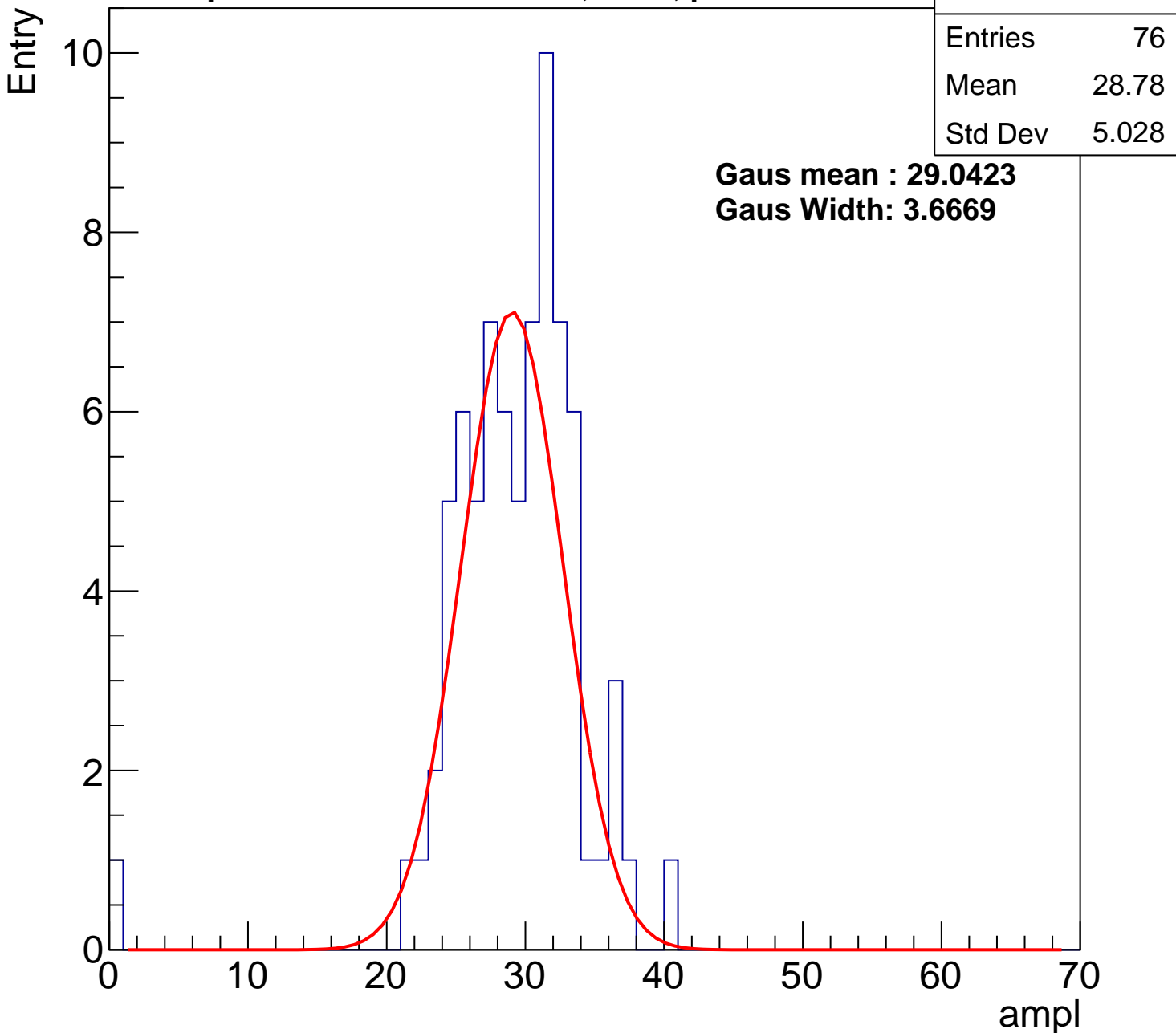
**Gaus Width: 3.6669**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U3-ch57, adc1

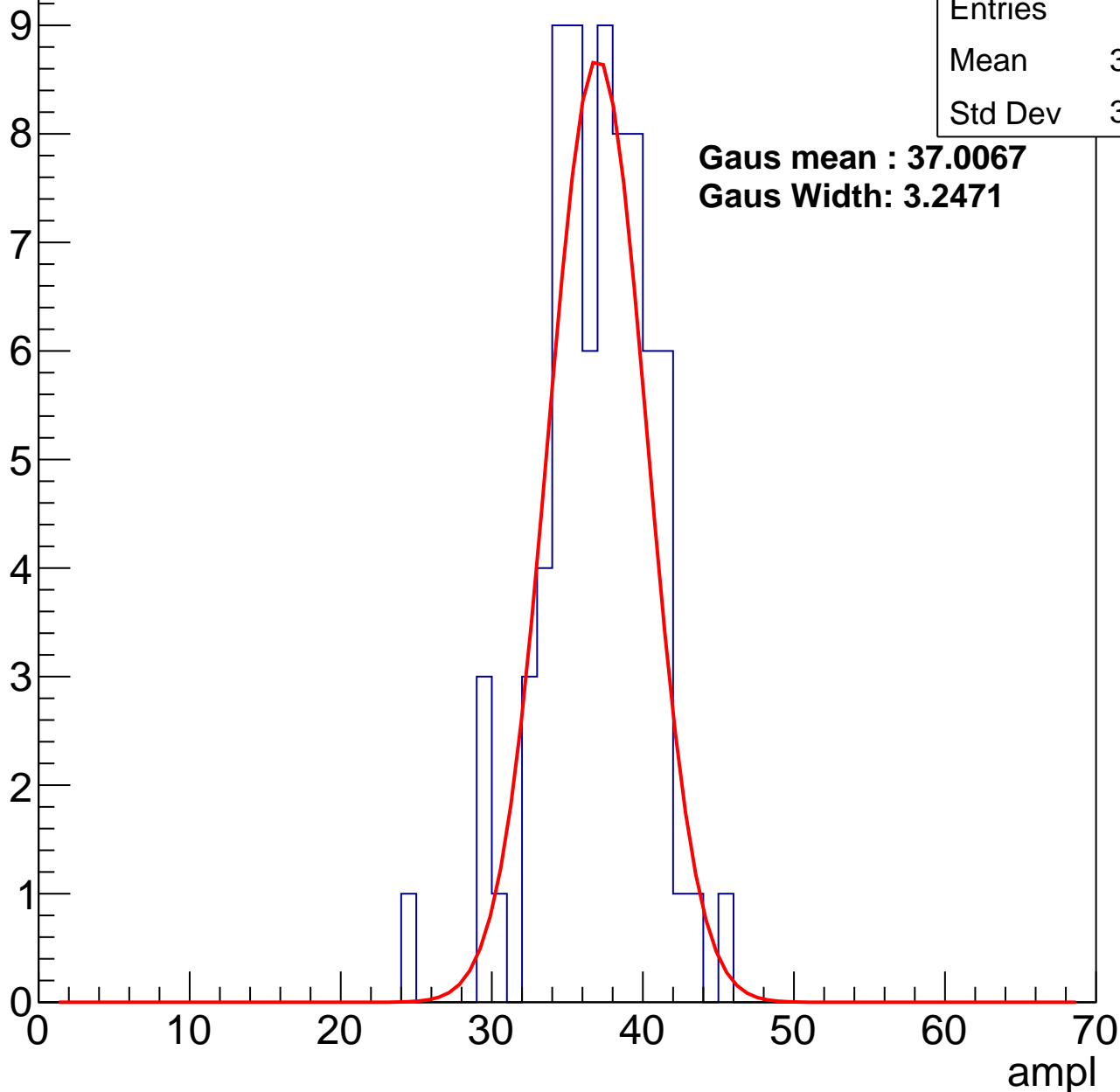
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	36.46
Std Dev	3.563

**Gaus mean : 37.0067**

**Gaus Width: 3.2471**



# B1L103S, U3-ch57, adc2

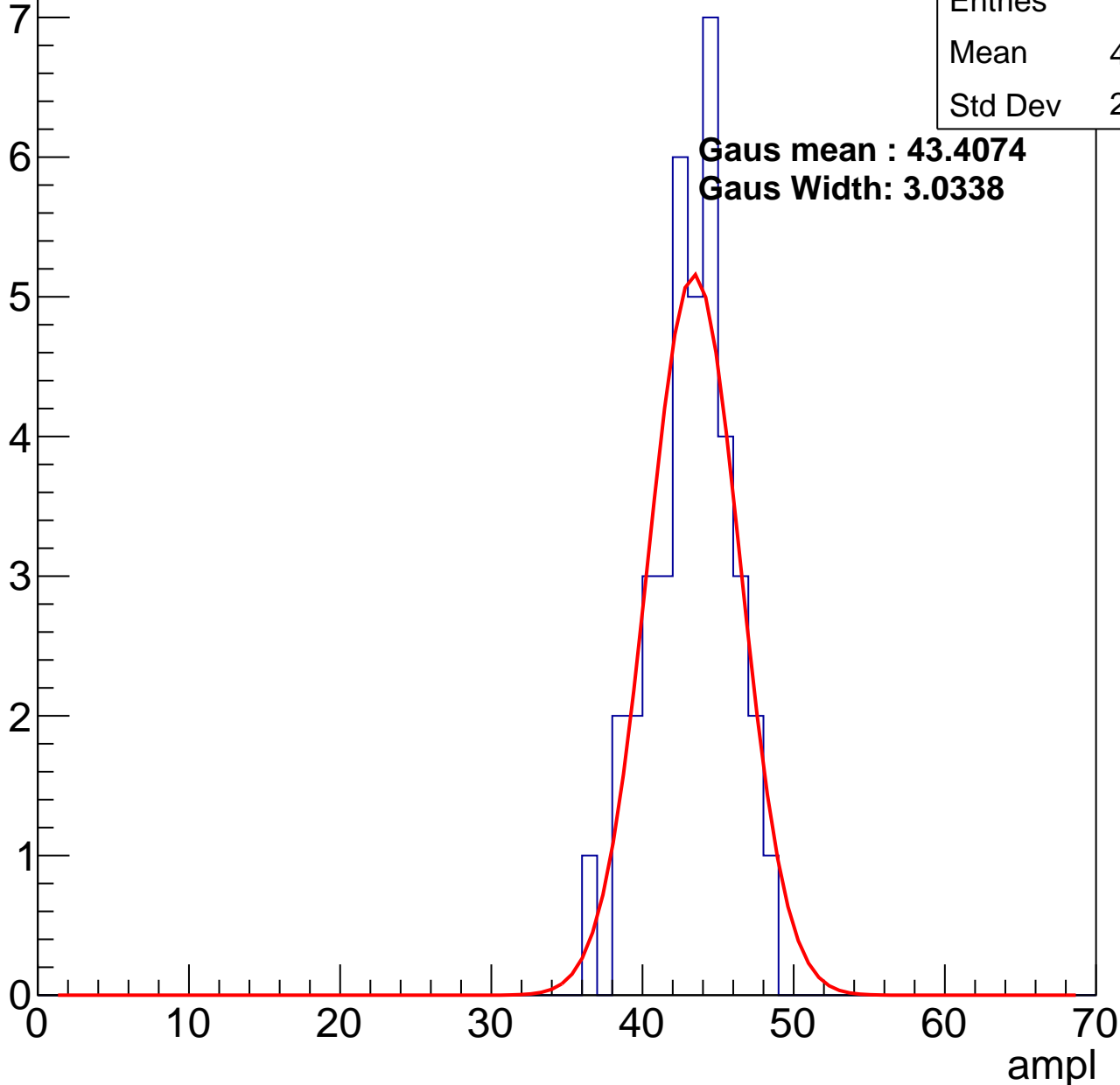
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	39
Mean	42.77
Std Dev	2.684

**Gaus mean : 43.4074**

**Gaus Width: 3.0338**

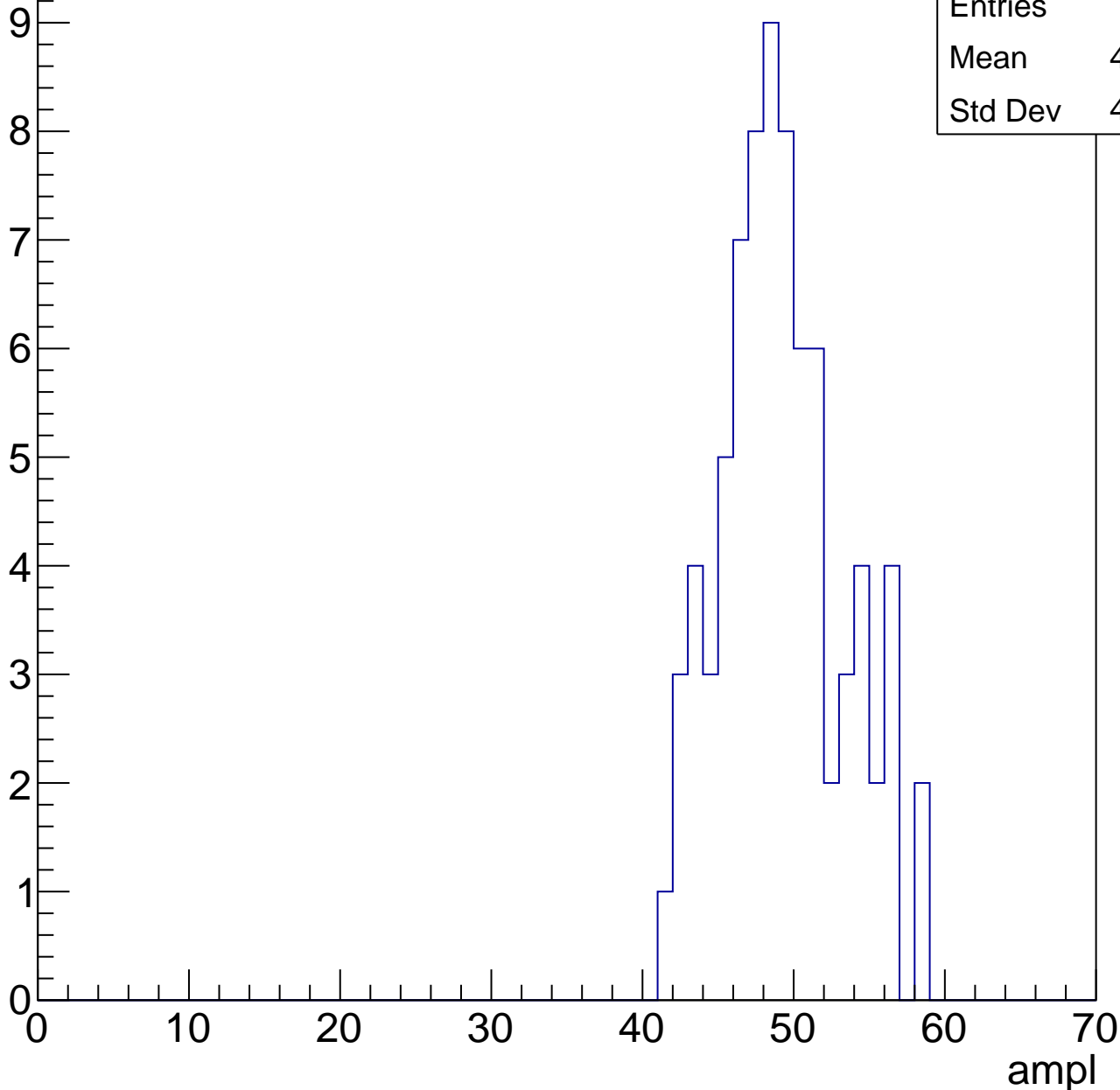


# B1L103S, U3-ch57, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	48.74
Std Dev	4.005

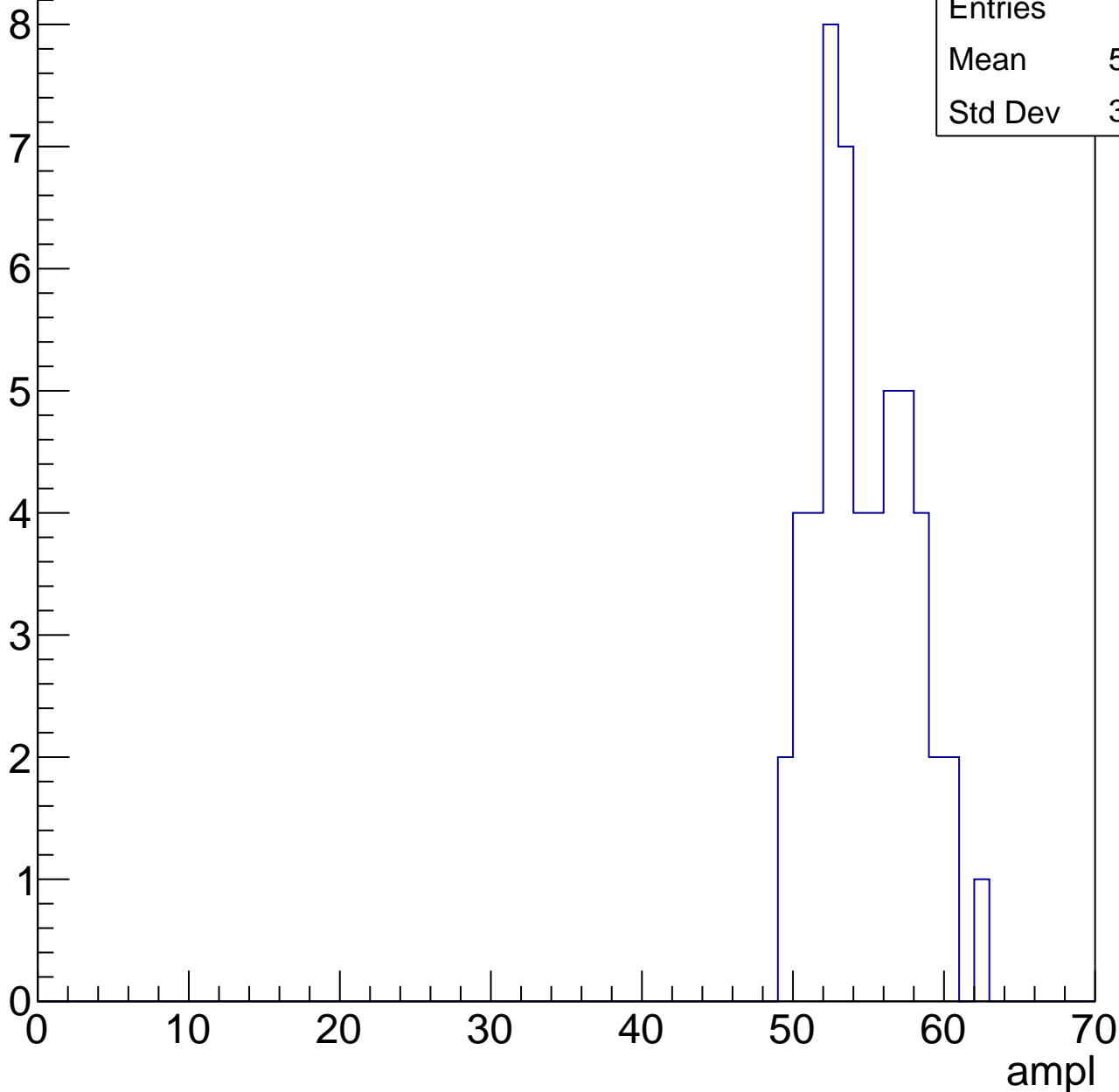


# B1L103S, U3-ch57, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	54.27
Std Dev	3.114

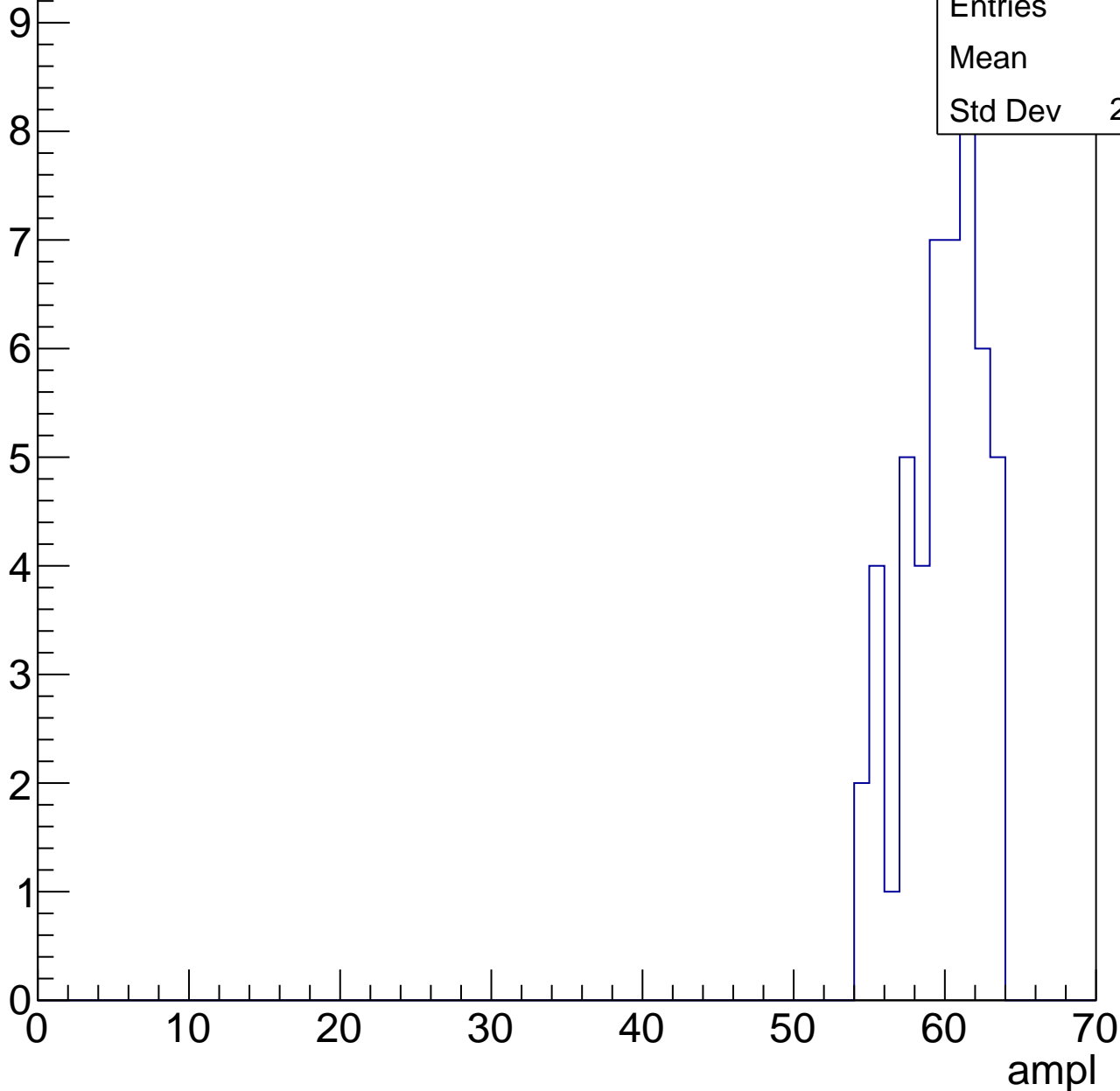


# B1L103S, U3-ch57, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

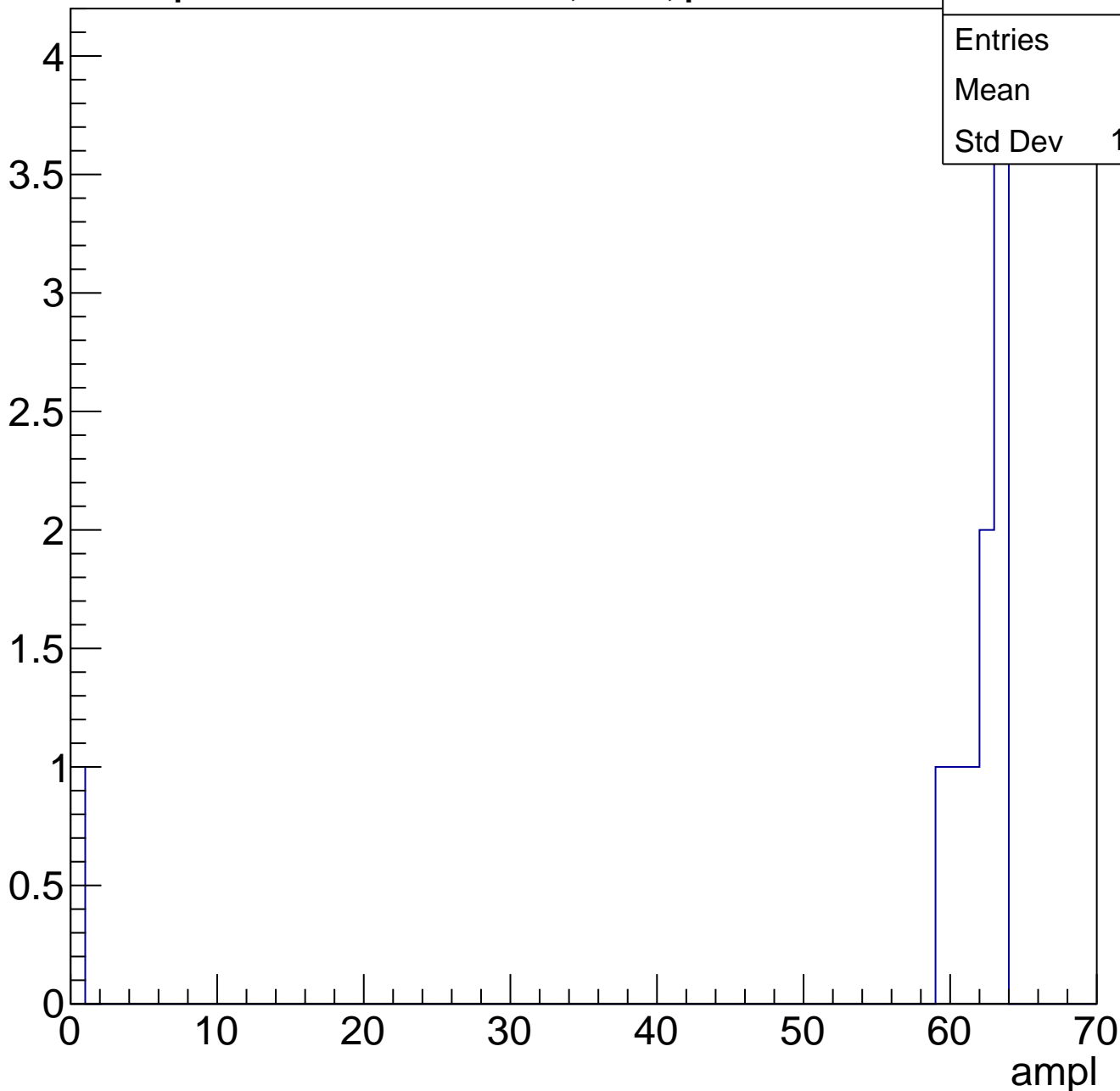
Entries	50
Mean	59.4
Std Dev	2.514



# B1L103S, U3-ch57, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U3-ch57, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch58, adc0

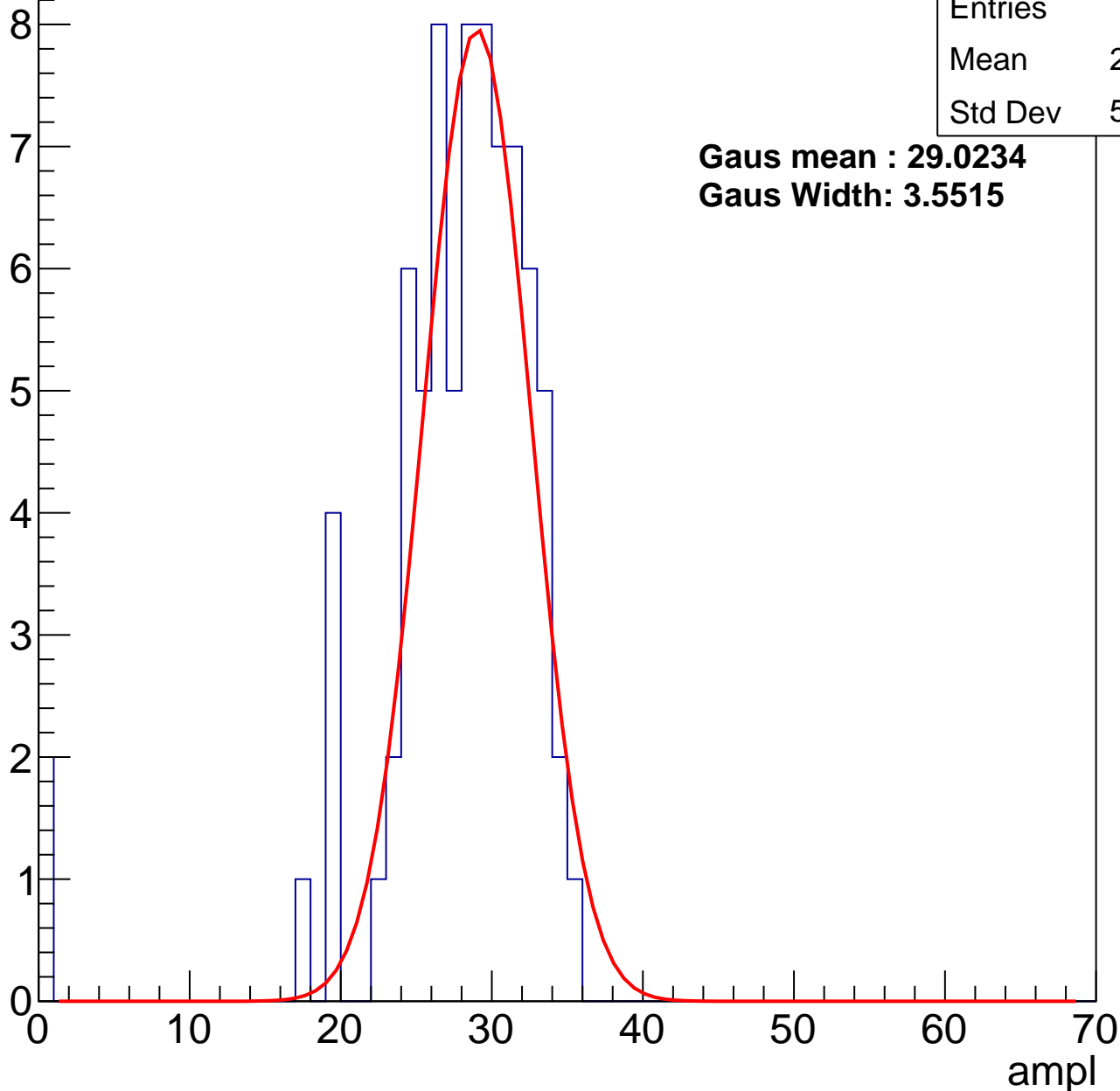
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	27.13
Std Dev	5.838

**Gaus mean : 29.0234**

**Gaus Width: 3.5515**



# B1L103S, U3-ch58, adc1

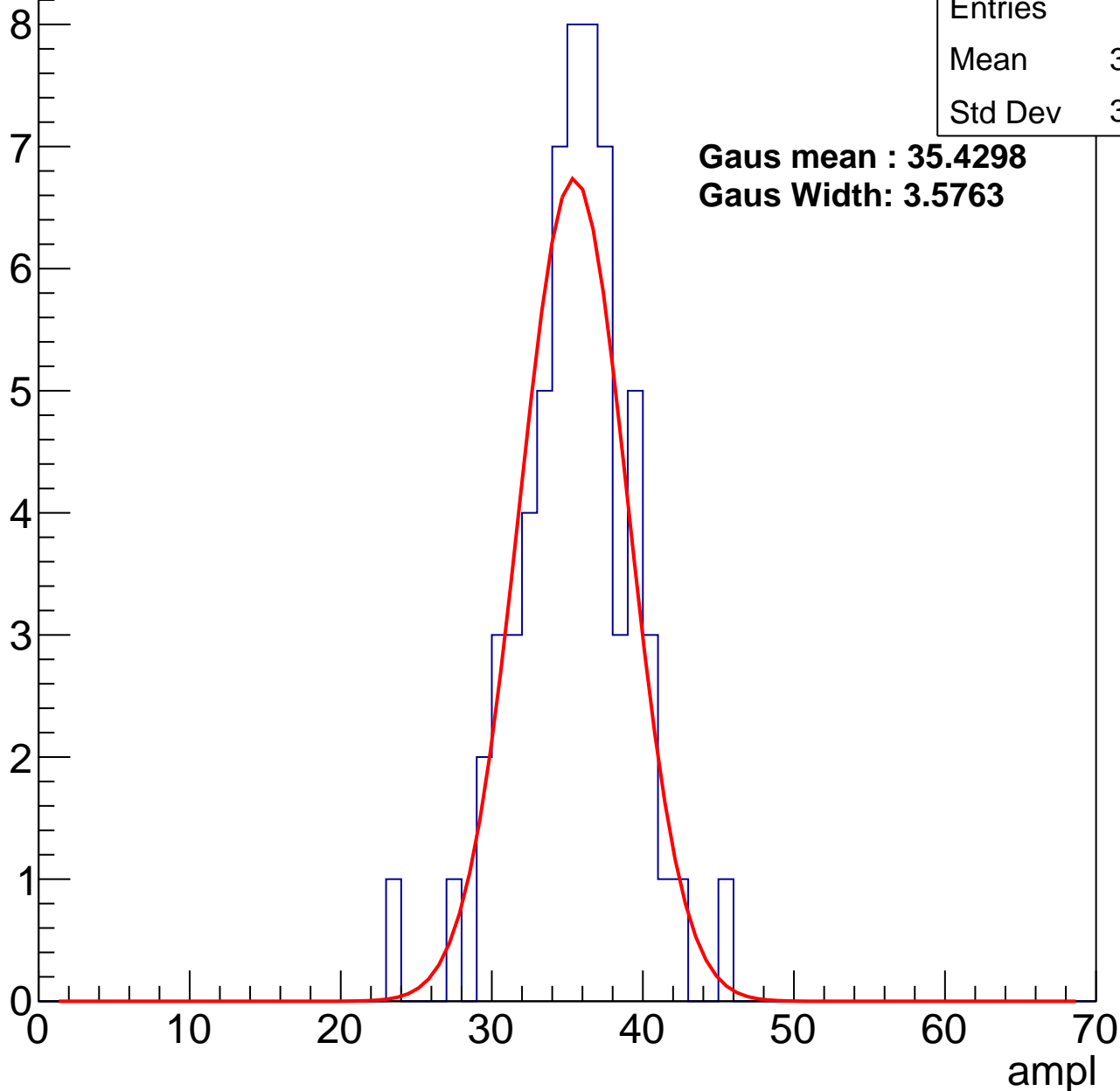
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	35.02
Std Dev	3.714

**Gaus mean : 35.4298**

**Gaus Width: 3.5763**



# B1L103S, U3-ch58, adc2

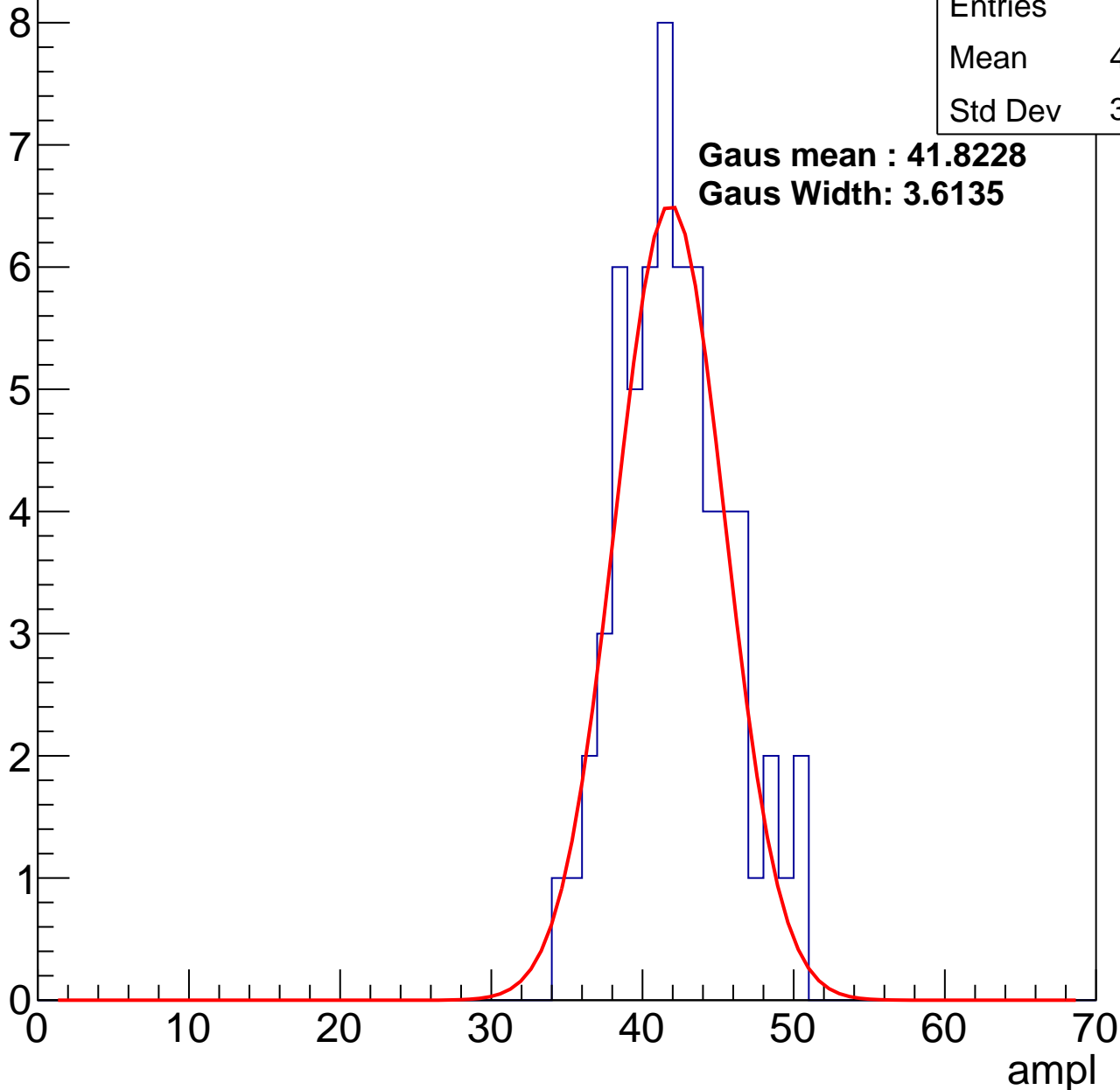
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	41.69
Std Dev	3.644

**Gaus mean : 41.8228**

**Gaus Width: 3.6135**

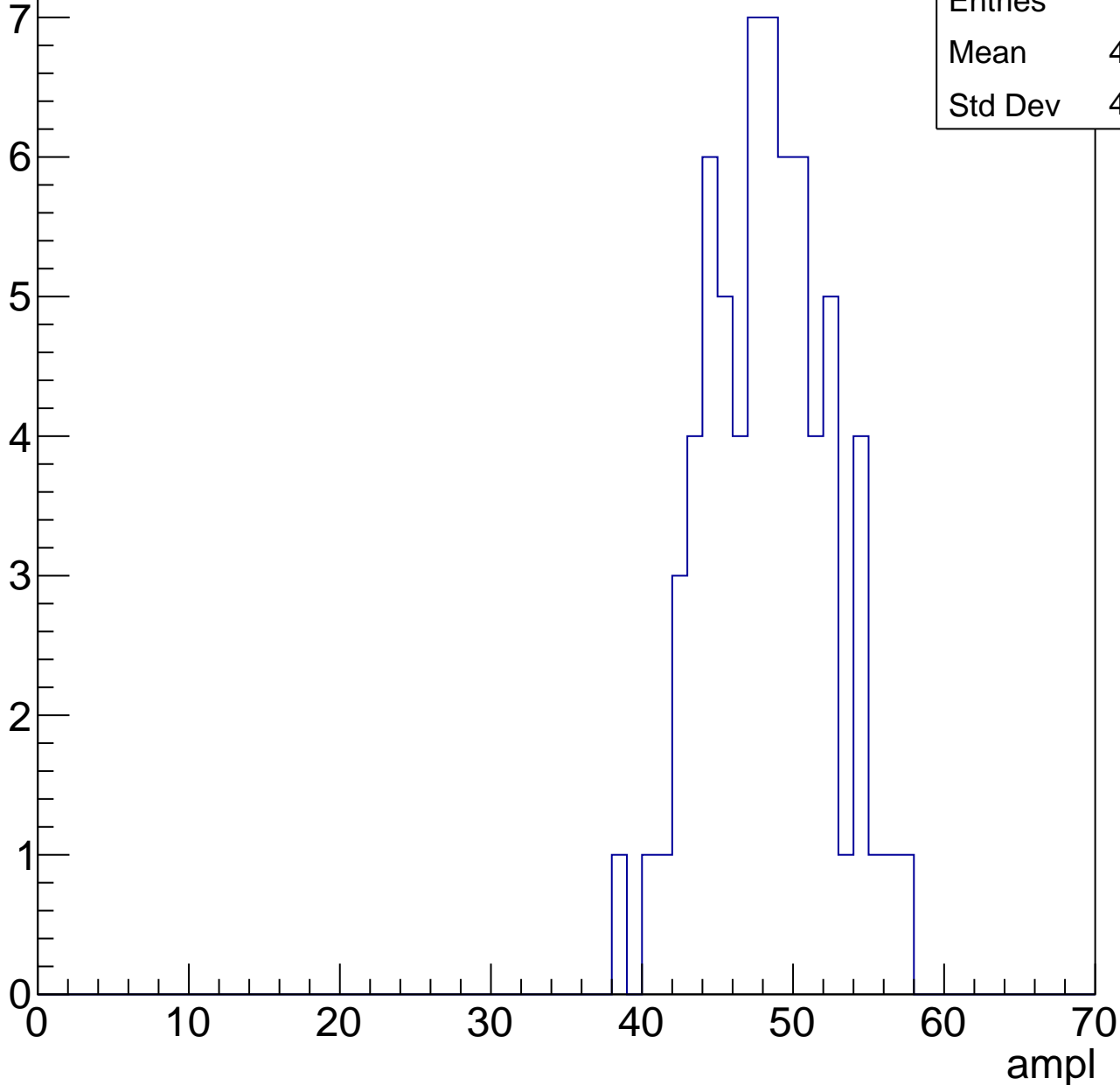


# B1L103S, U3-ch58, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

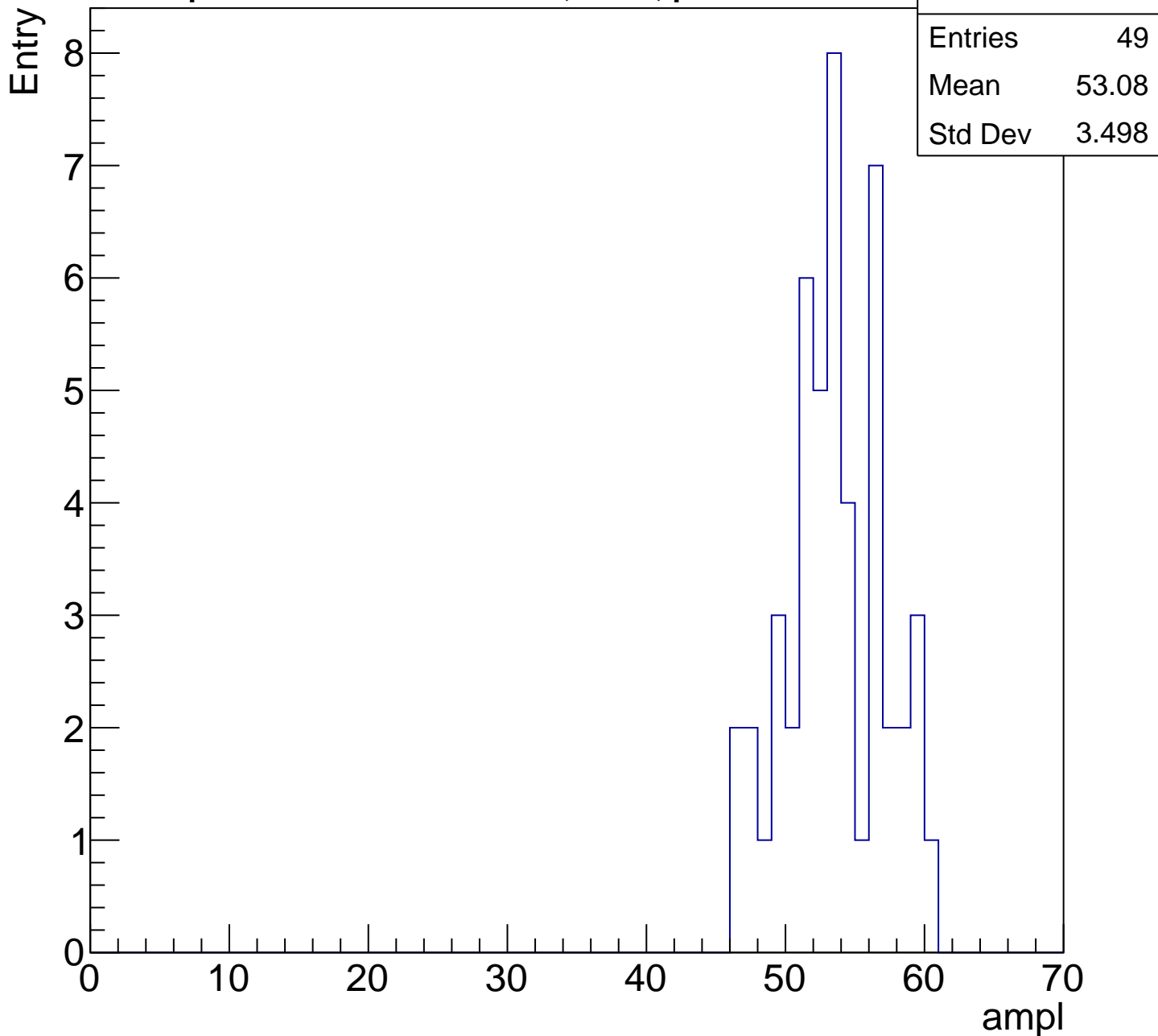
Entry

Entries	68
Mean	47.79
Std Dev	4.006



# B1L103S, U3-ch58, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

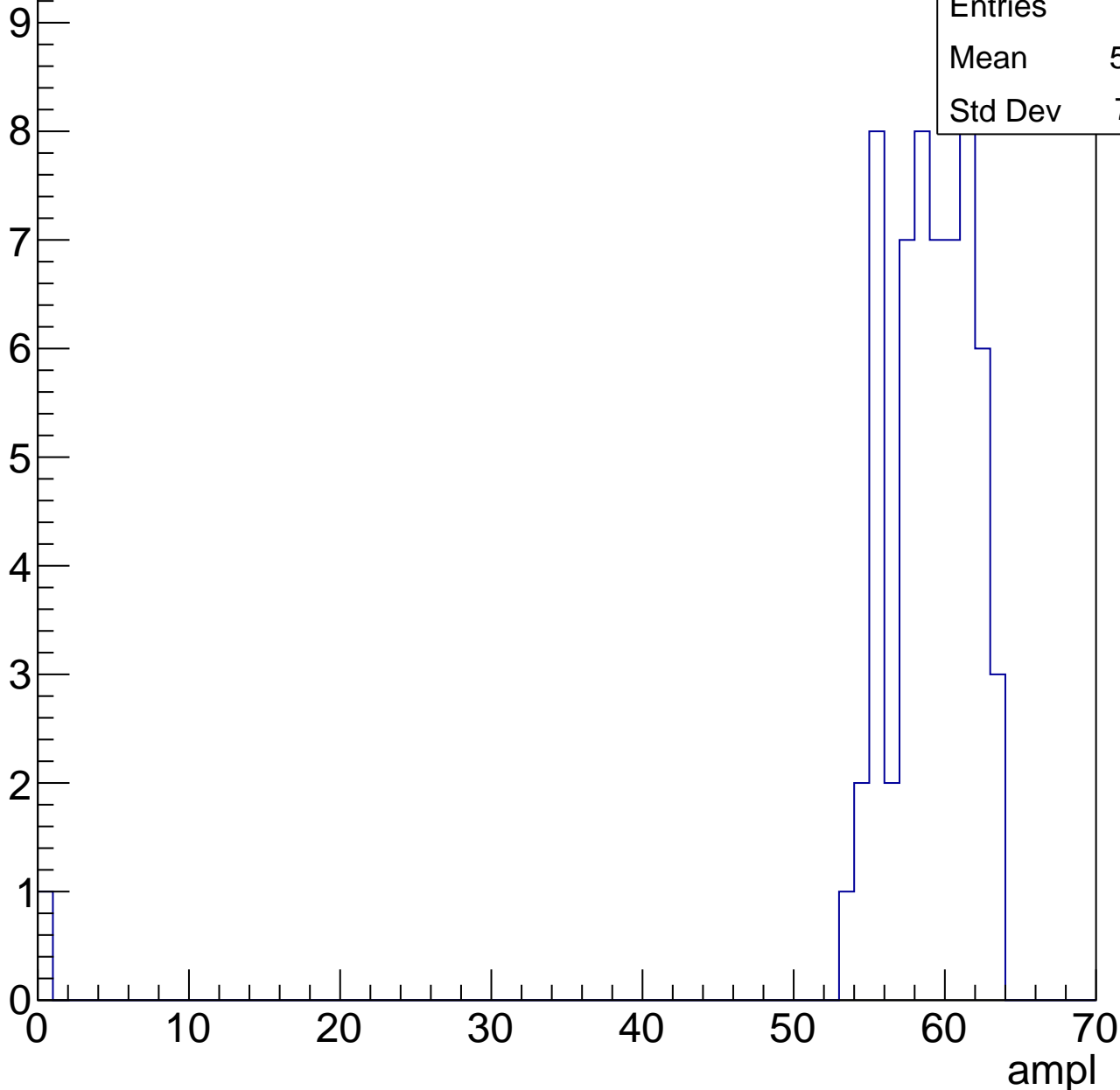


# B1L103S, U3-ch58, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	57.69
Std Dev	7.881

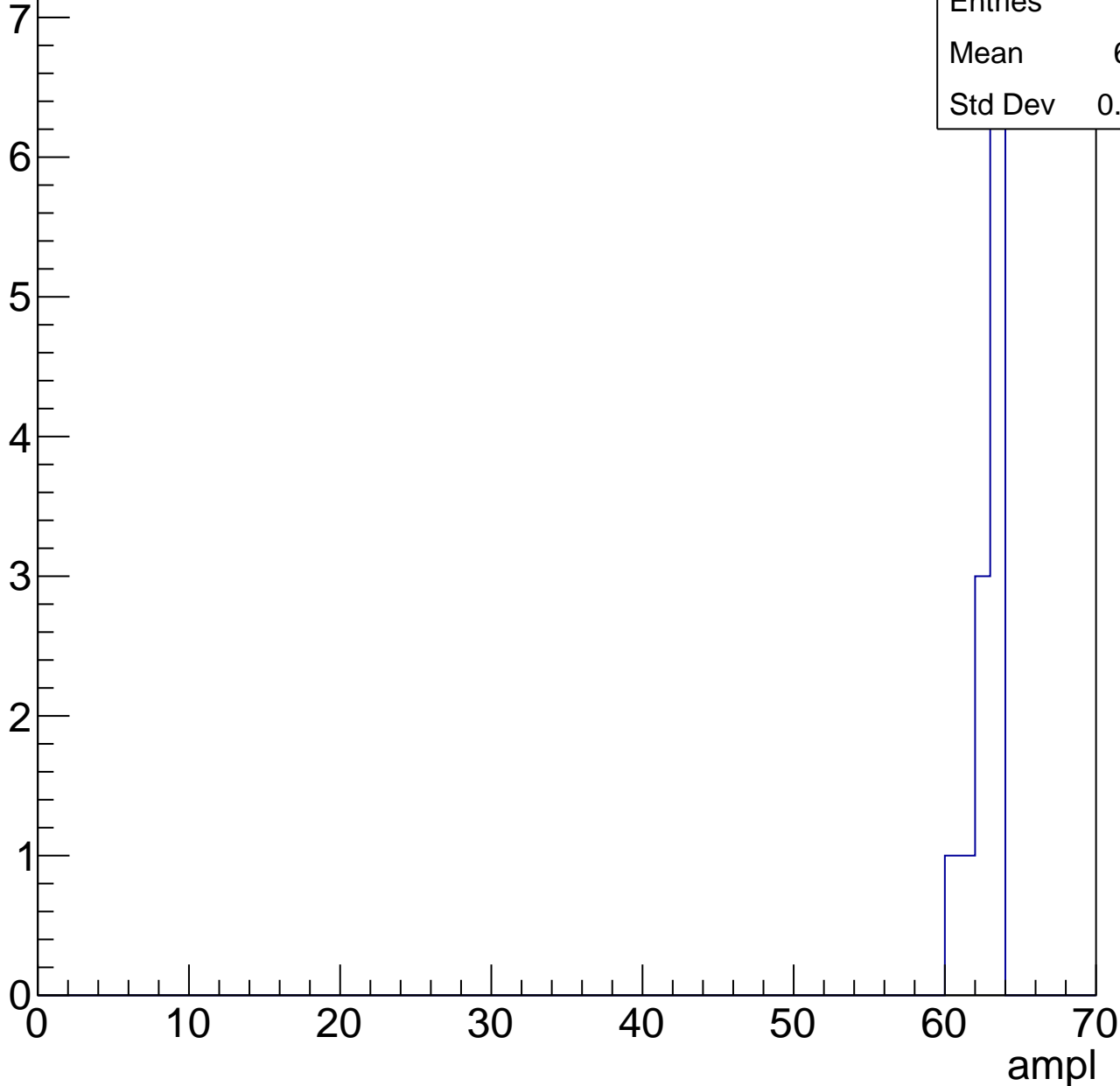


# B1L103S, U3-ch58, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	12
Mean	62.33
Std Dev	0.9428

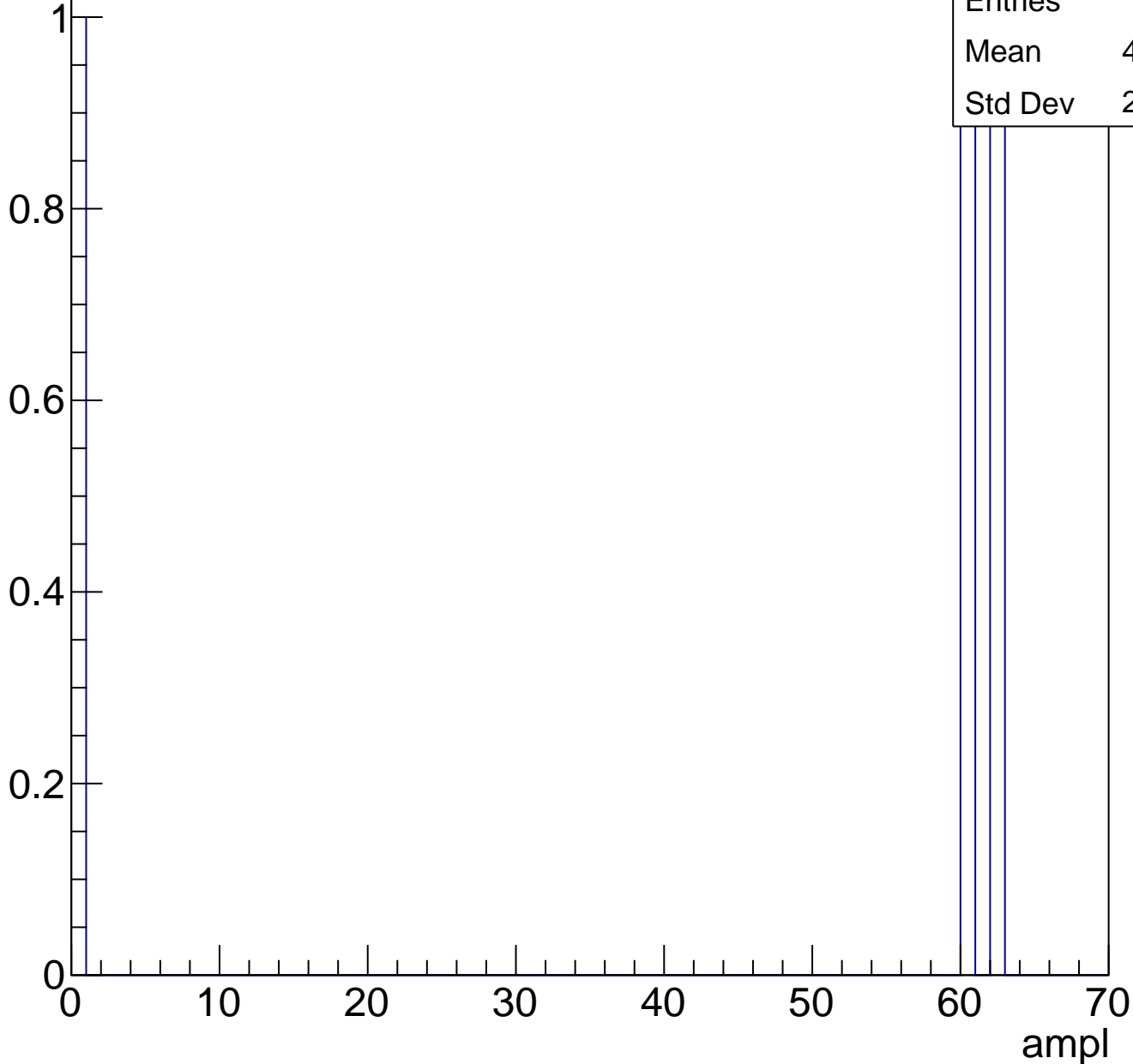




# B1L103S, U3-ch58, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch59, adc0

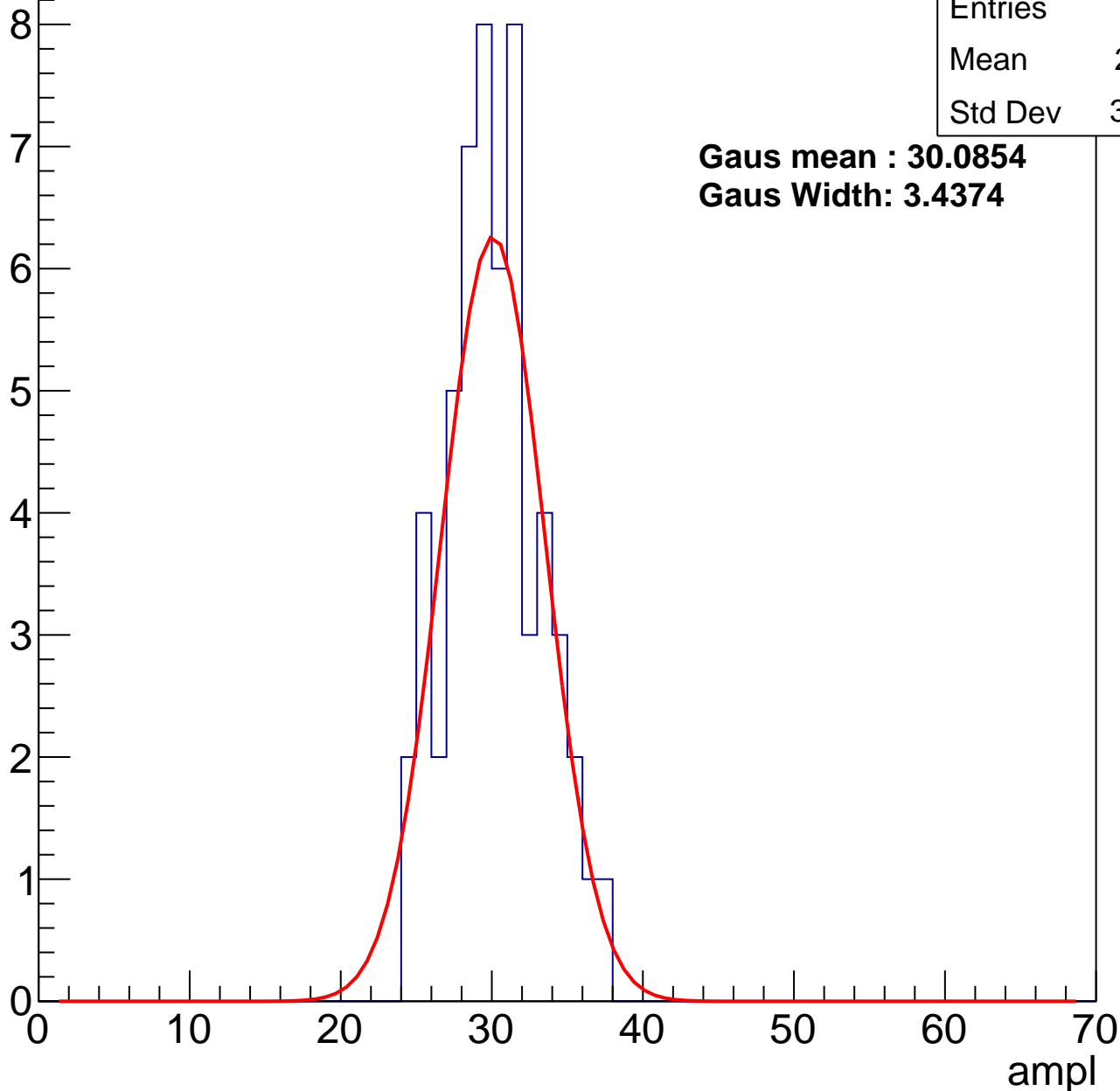
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	29.71
Std Dev	3.046

**Gaus mean : 30.0854**

**Gaus Width: 3.4374**



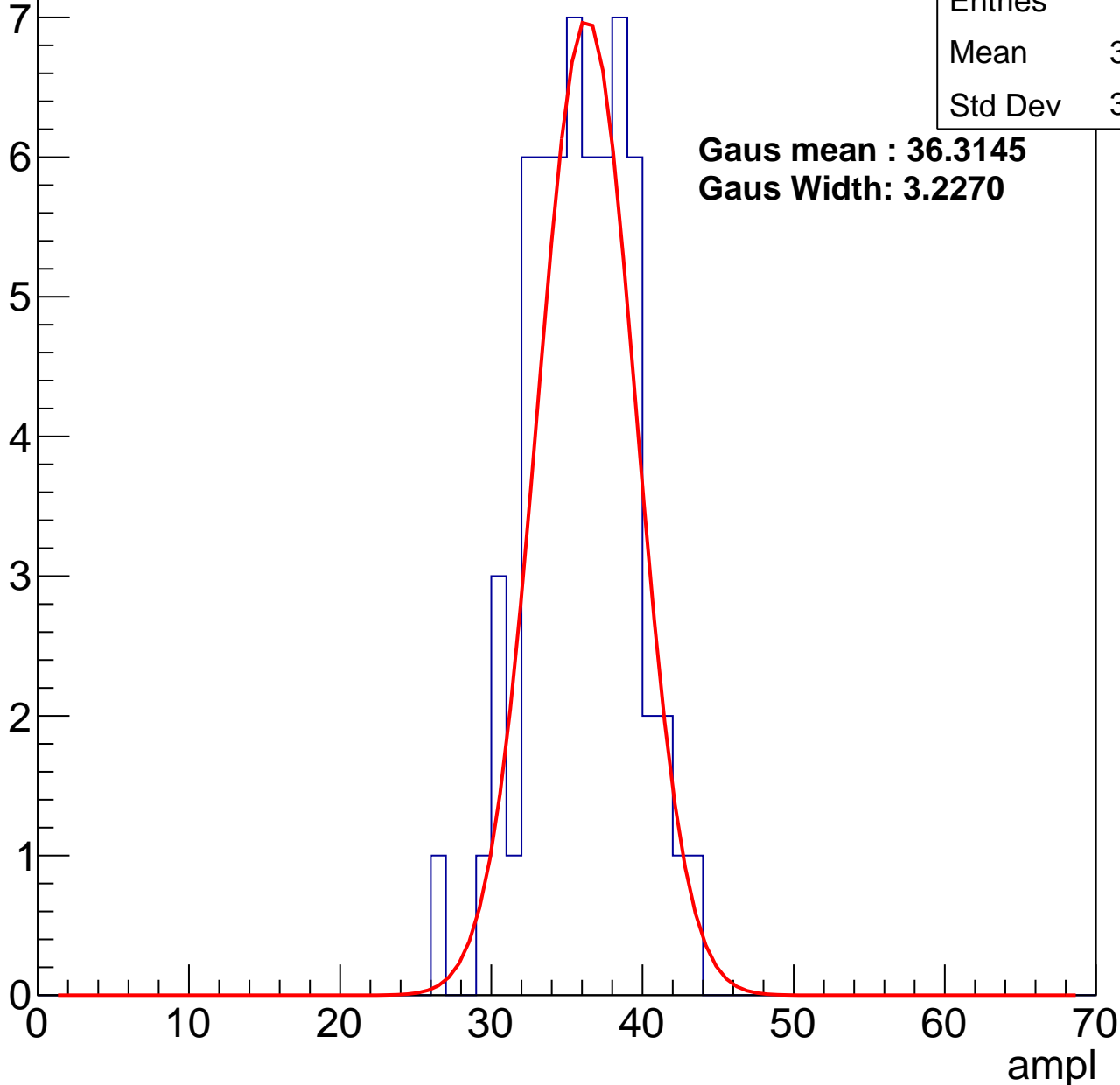
# B1L103S, U3-ch59, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	35.48
Std Dev	3.364

**Gaus mean : 36.3145**  
**Gaus Width: 3.2270**



# B1L103S, U3-ch59, adc2

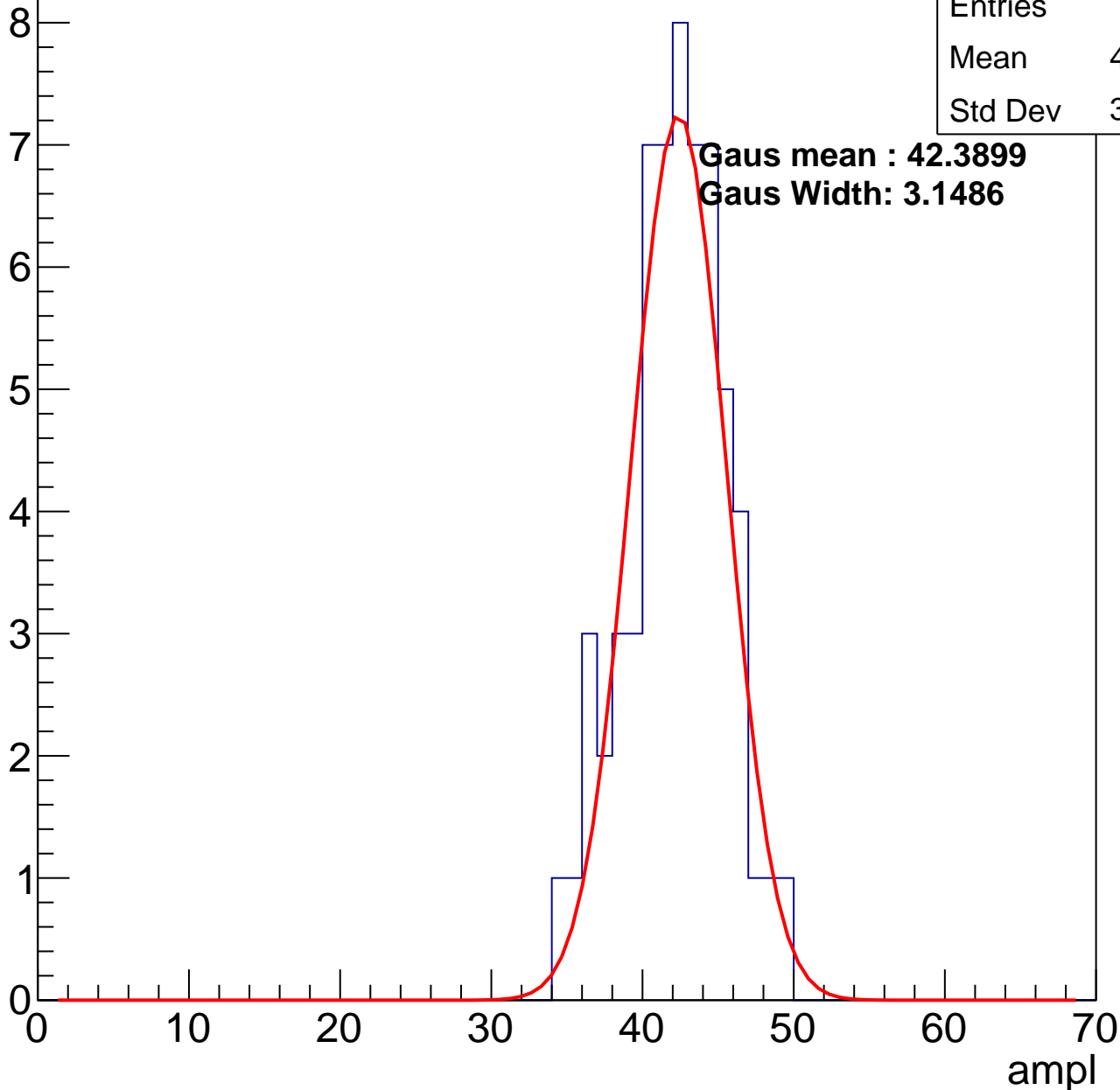
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	41.75
Std Dev	3.217

**Gaus mean : 42.3899**

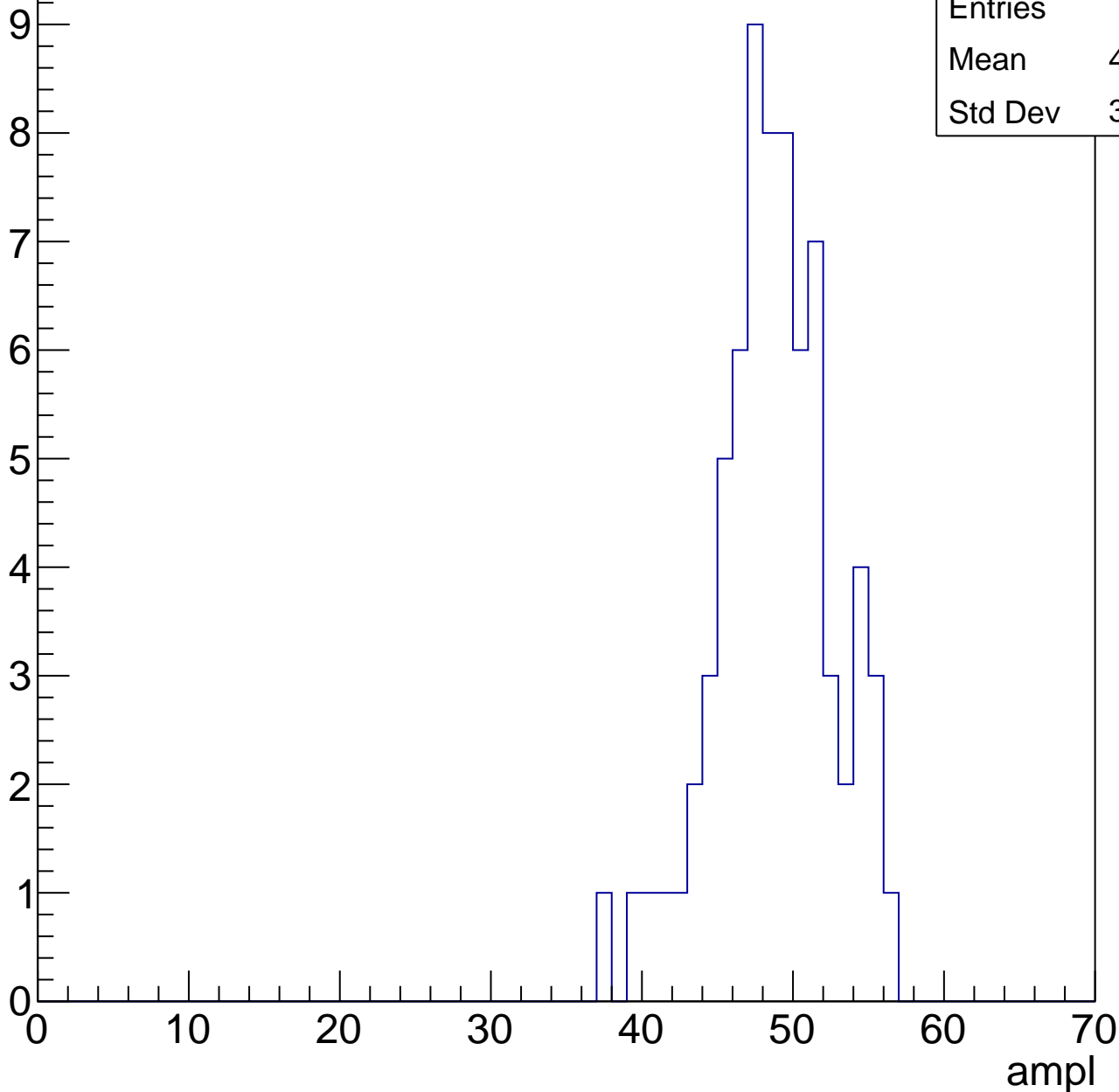
**Gaus Width: 3.1486**



# B1L103S, U3-ch59, adc3

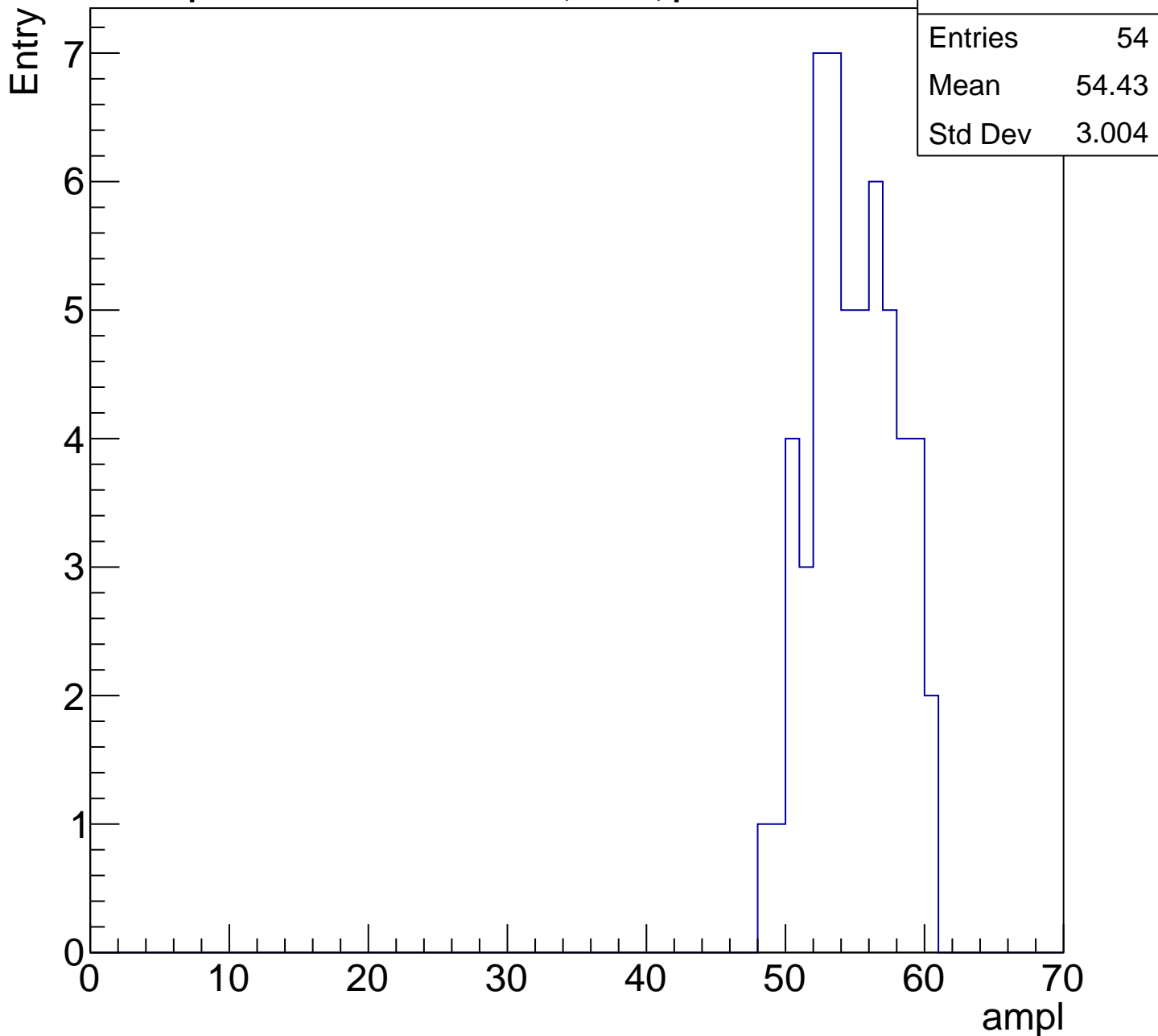
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



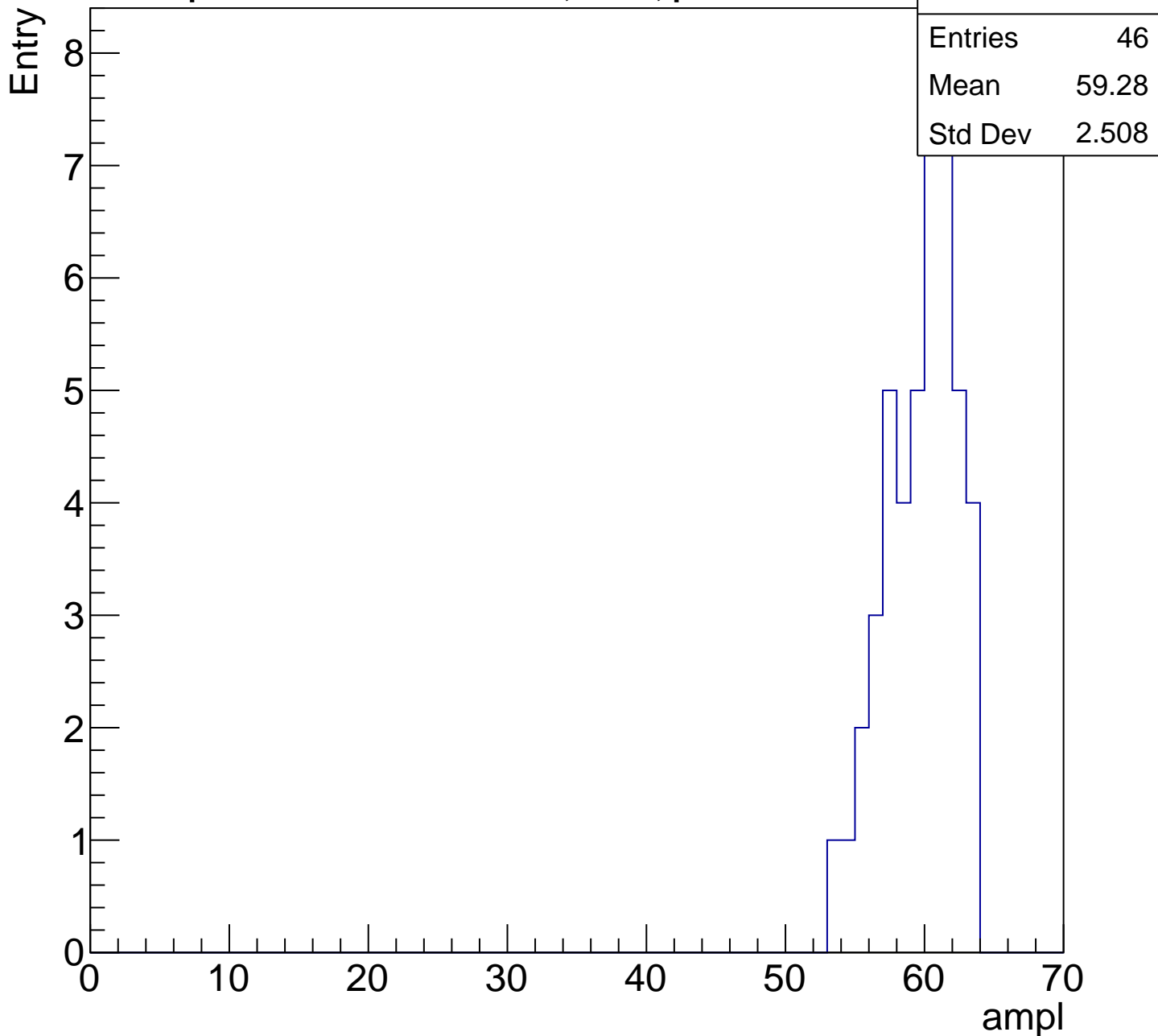
# B1L103S, U3-ch59, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U3-ch59, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

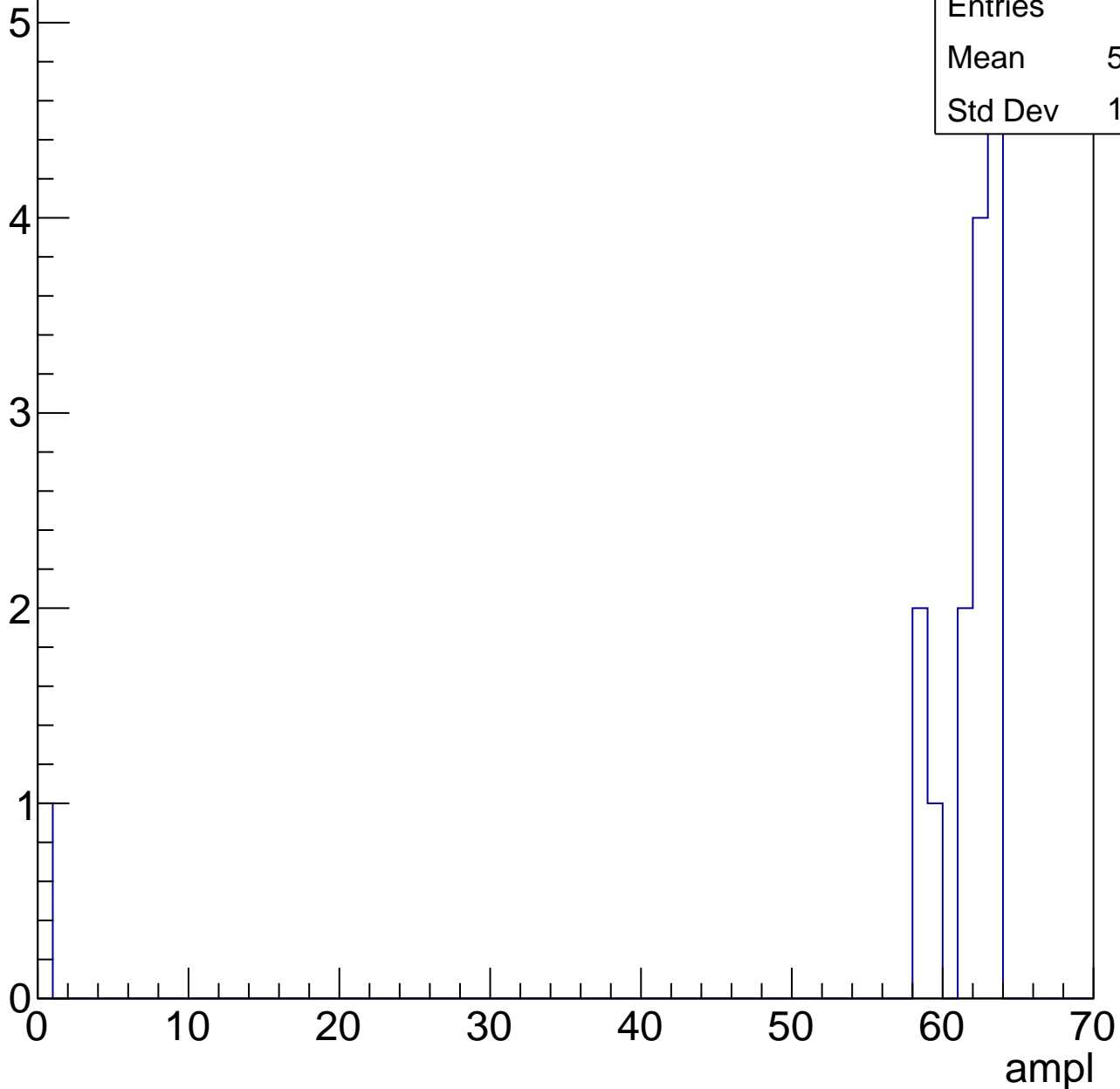


# B1L103S, U3-ch59, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	15
Mean	57.33
Std Dev	15.42





# B1L103S, U3-ch59, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch60, adc0

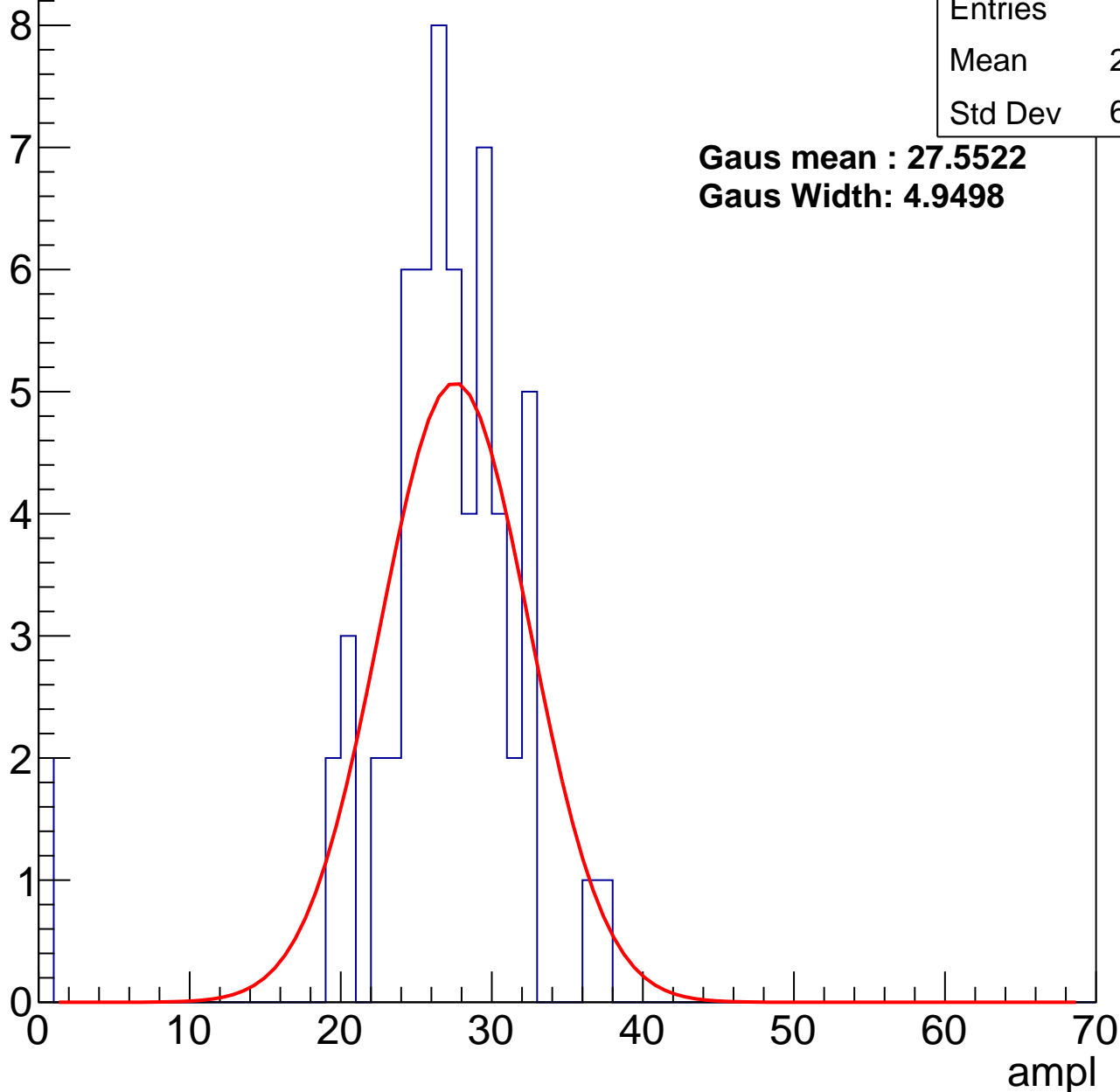
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	25.93
Std Dev	6.057

**Gaus mean : 27.5522**

**Gaus Width: 4.9498**



# B1L103S, U3-ch60, adc1

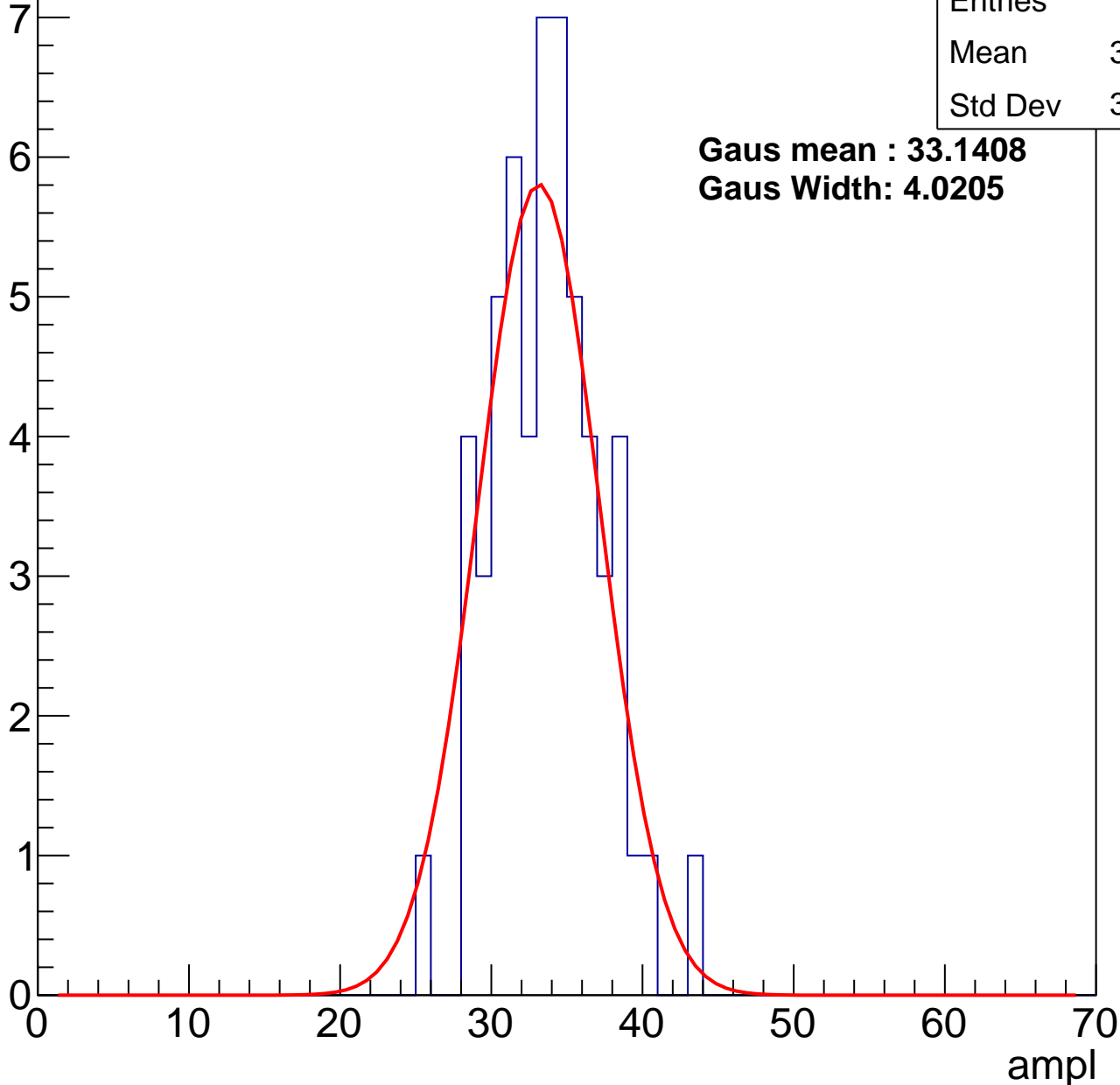
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	33.23
Std Dev	3.479

**Gaus mean : 33.1408**

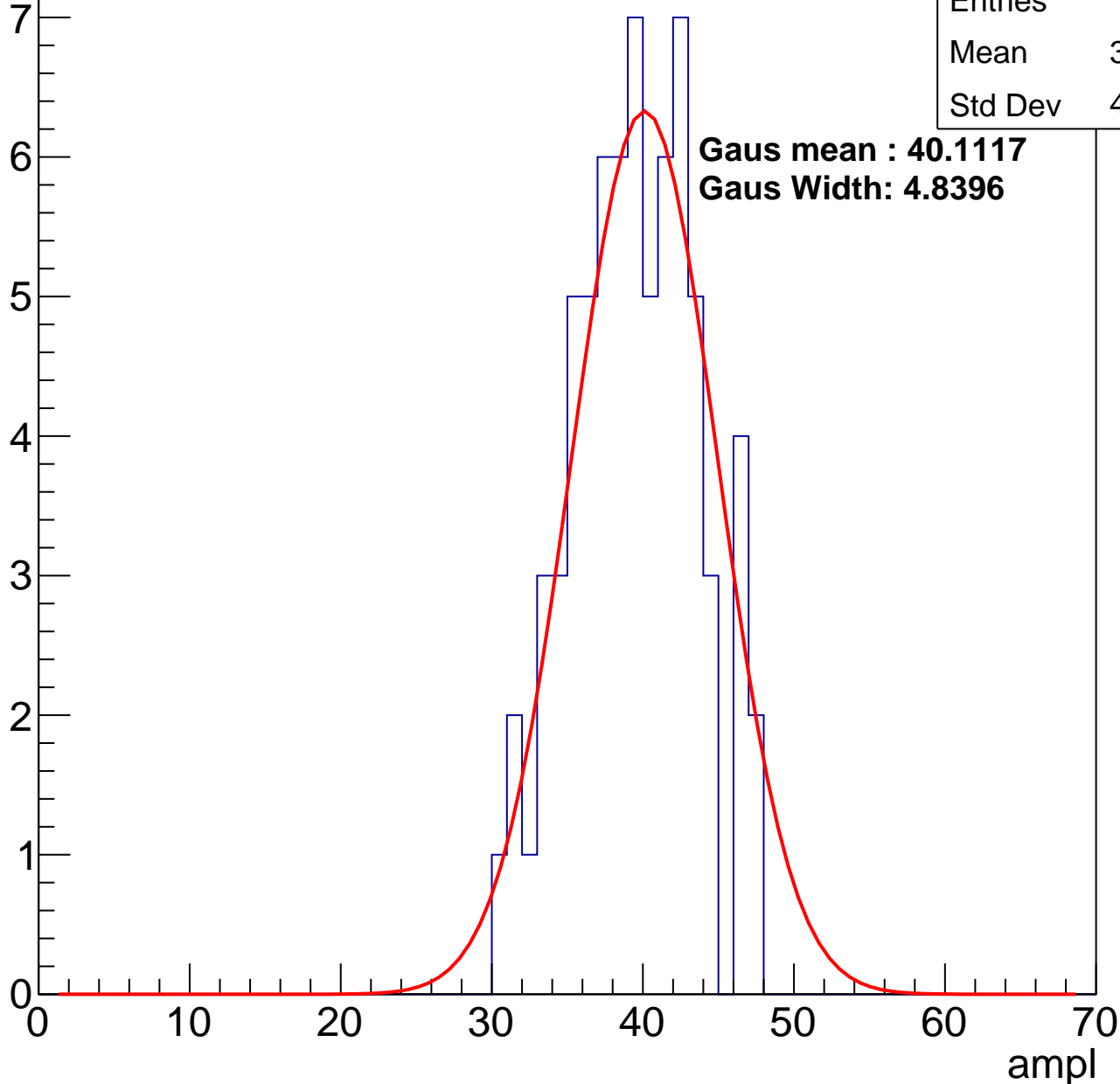
**Gaus Width: 4.0205**



# B1L103S, U3-ch60, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch60, adc3

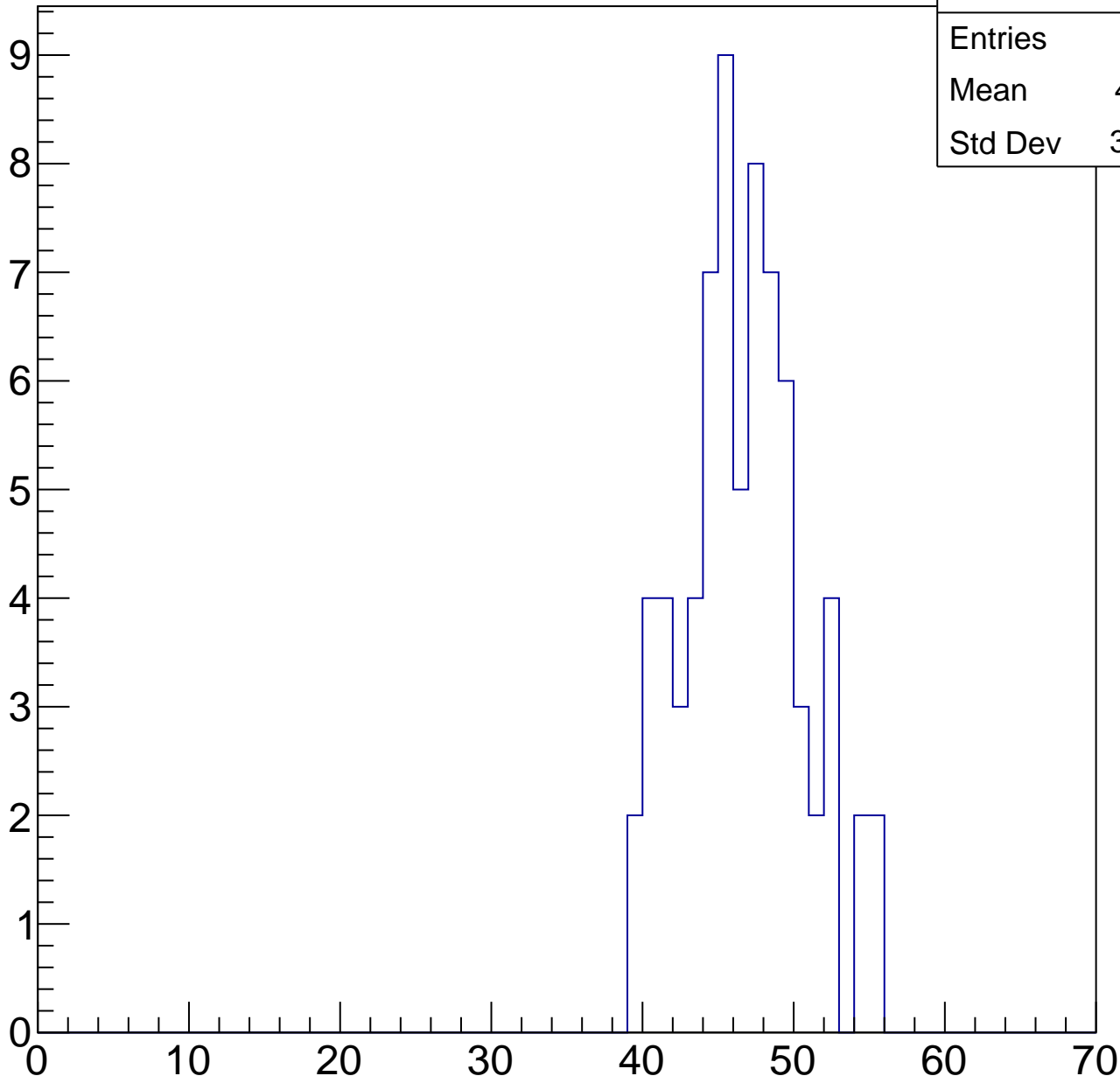
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

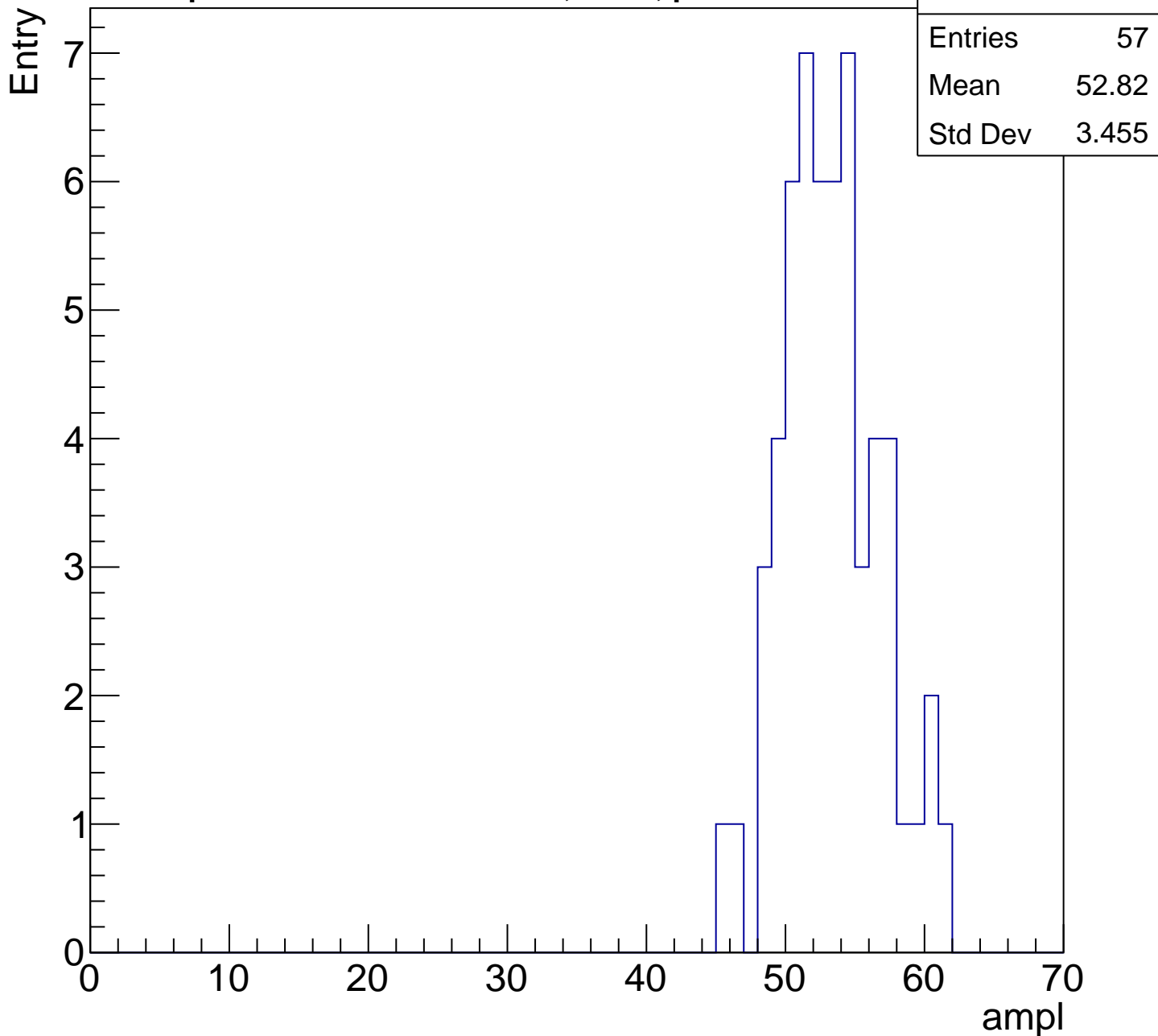
Entries	72
Mean	46.21
Std Dev	3.876

ampl



# B1L103S, U3-ch60, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

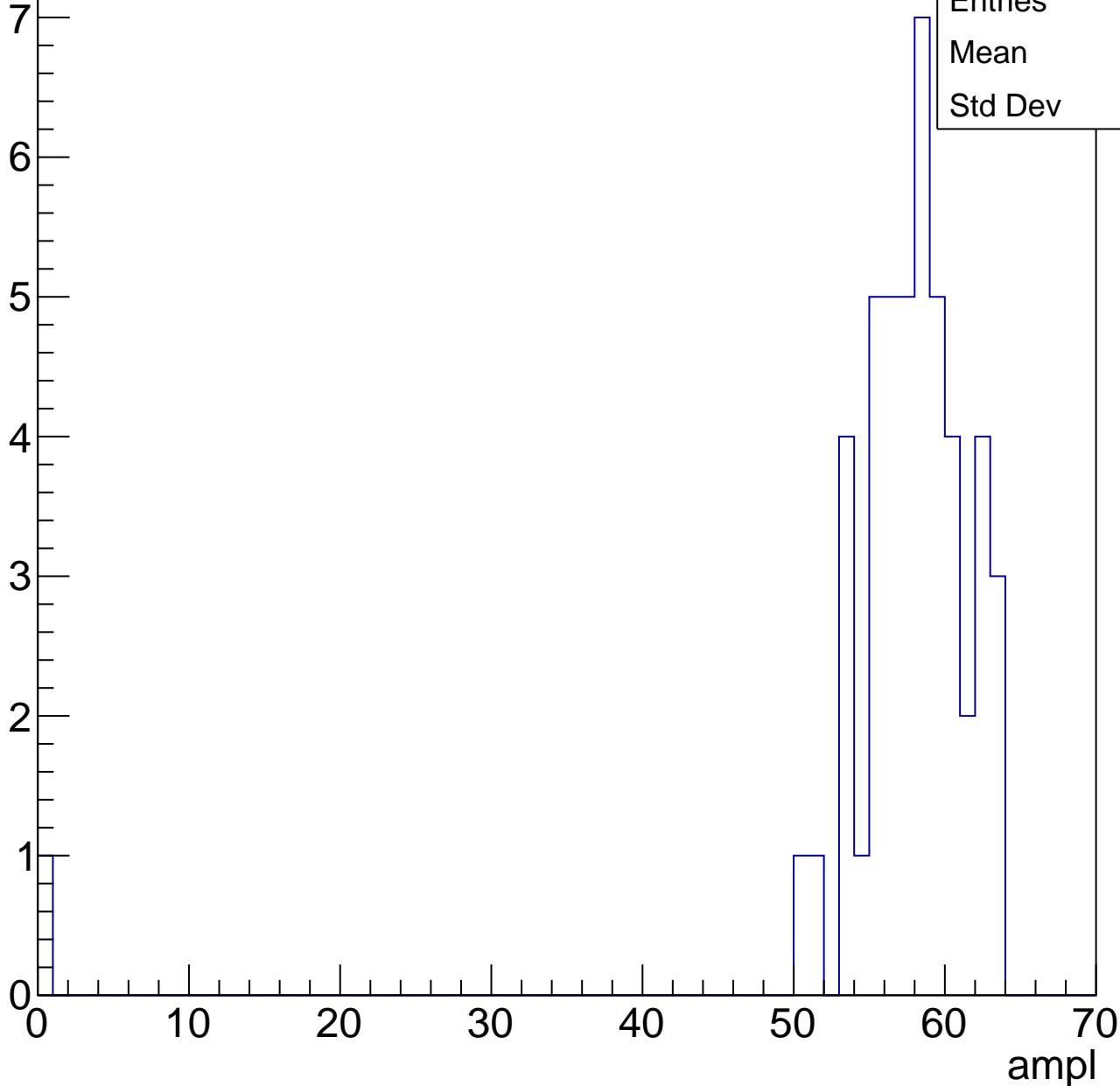


# B1L103S, U3-ch60, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	48
Mean	56.4
Std Dev	8.8

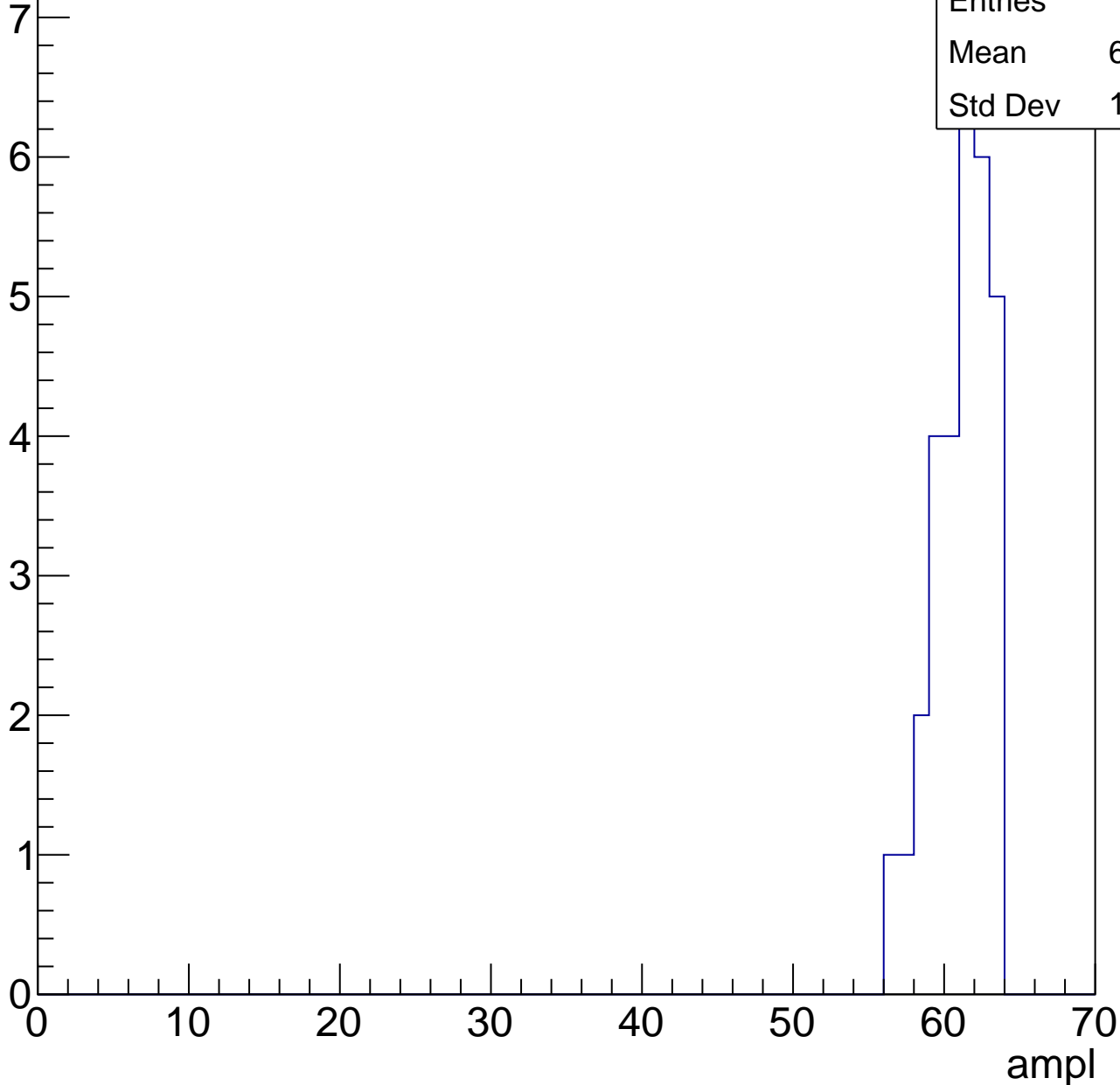


# B1L103S, U3-ch60, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	30
Mean	60.63
Std Dev	1.835





# B1L103S, U3-ch60, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch61, adc0

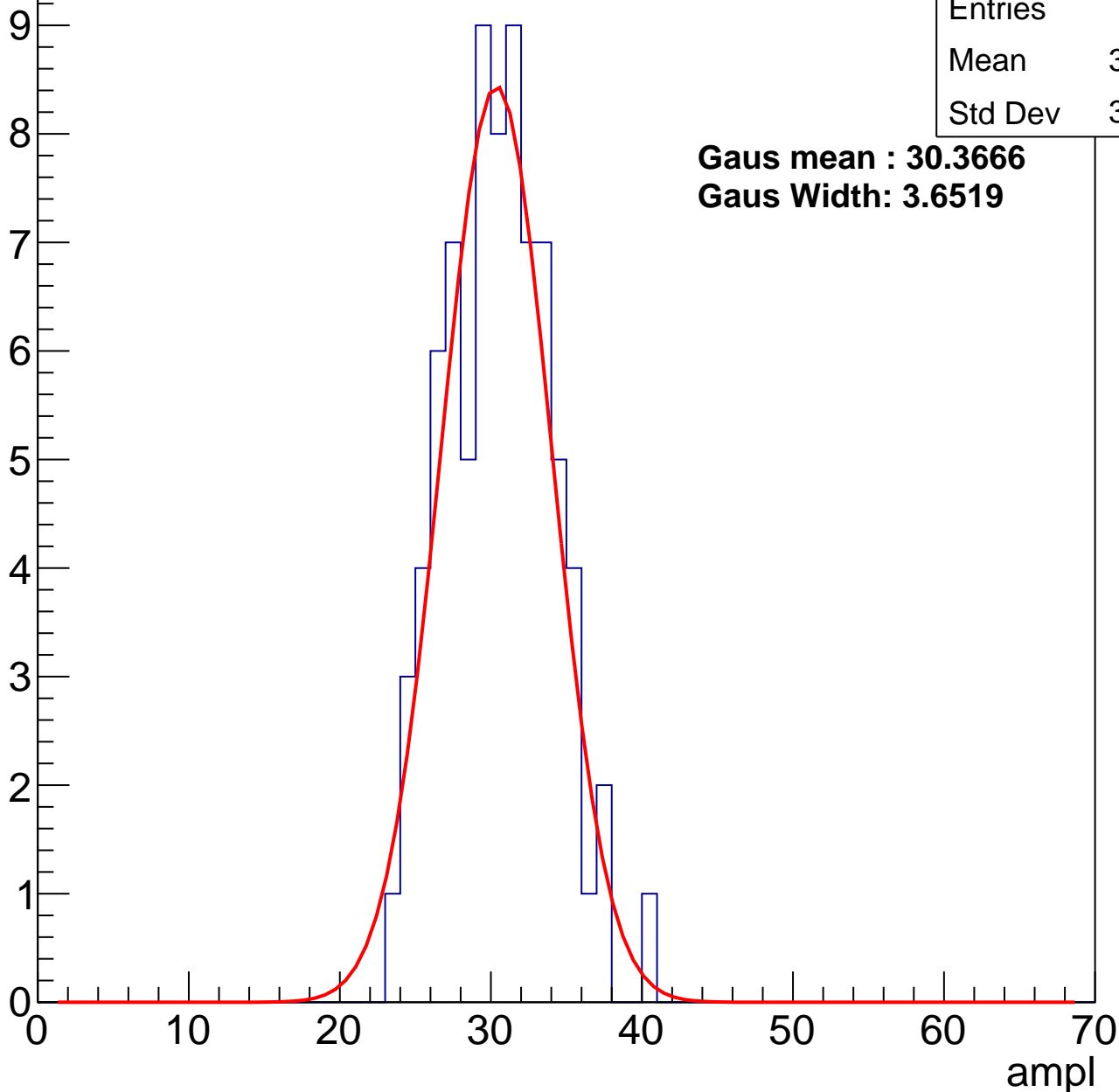
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	79
Mean	30.06
Std Dev	3.484

**Gaus mean : 30.3666**

**Gaus Width: 3.6519**



# B1L103S, U3-ch61, adc1

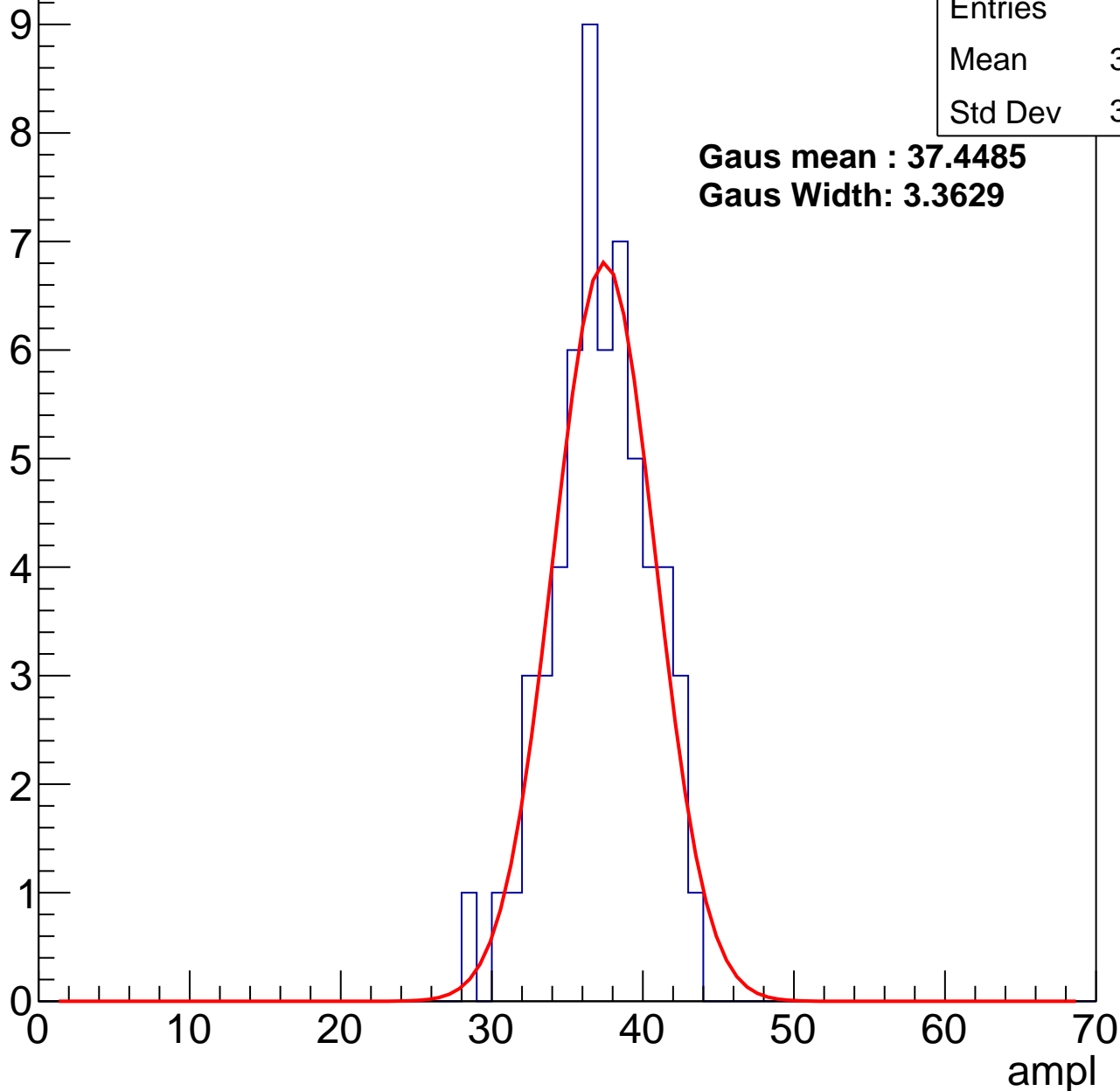
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	36.72
Std Dev	3.194

**Gaus mean : 37.4485**

**Gaus Width: 3.3629**



# B1L103S, U3-ch61, adc2

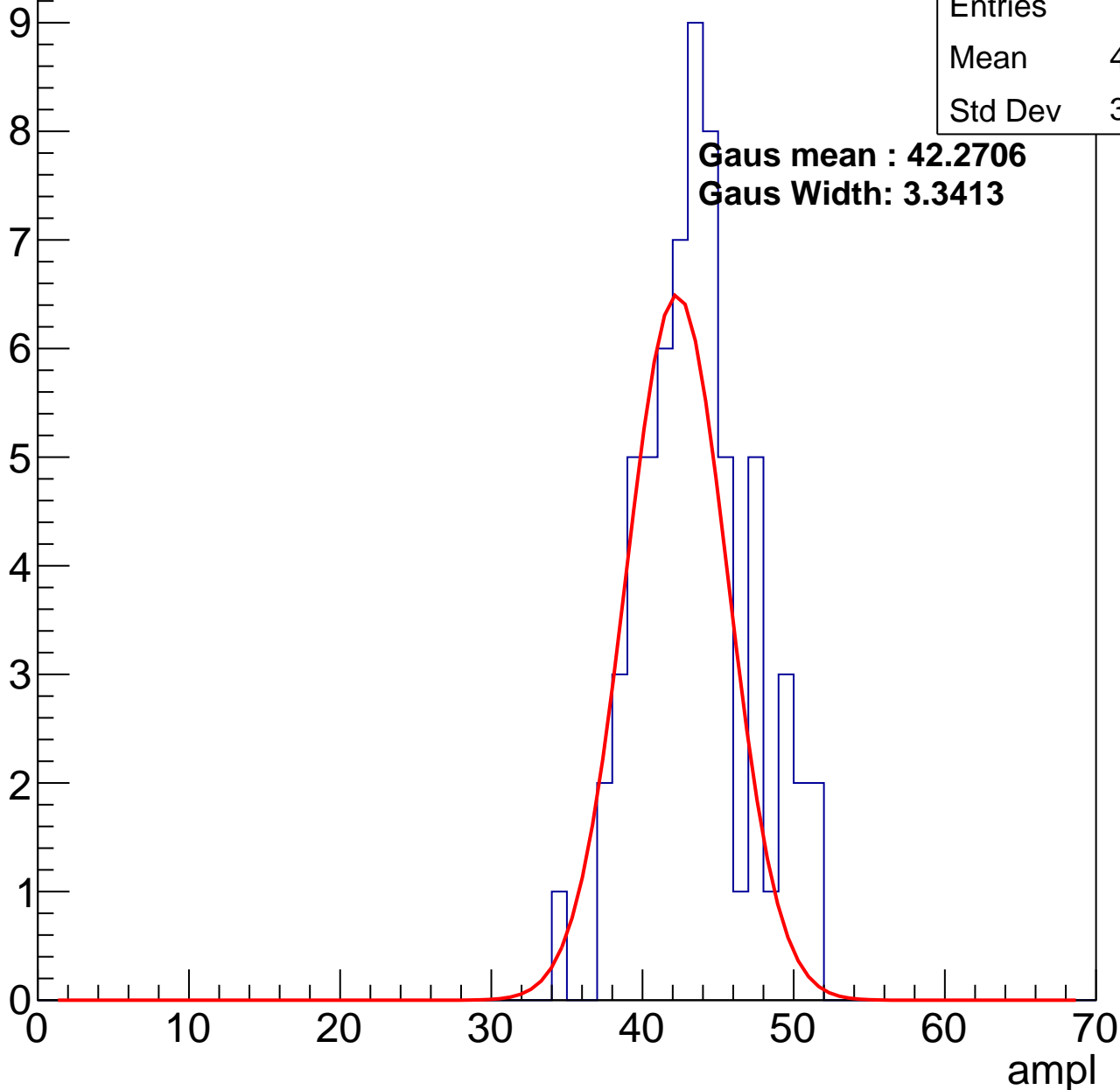
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	43.06
Std Dev	3.637

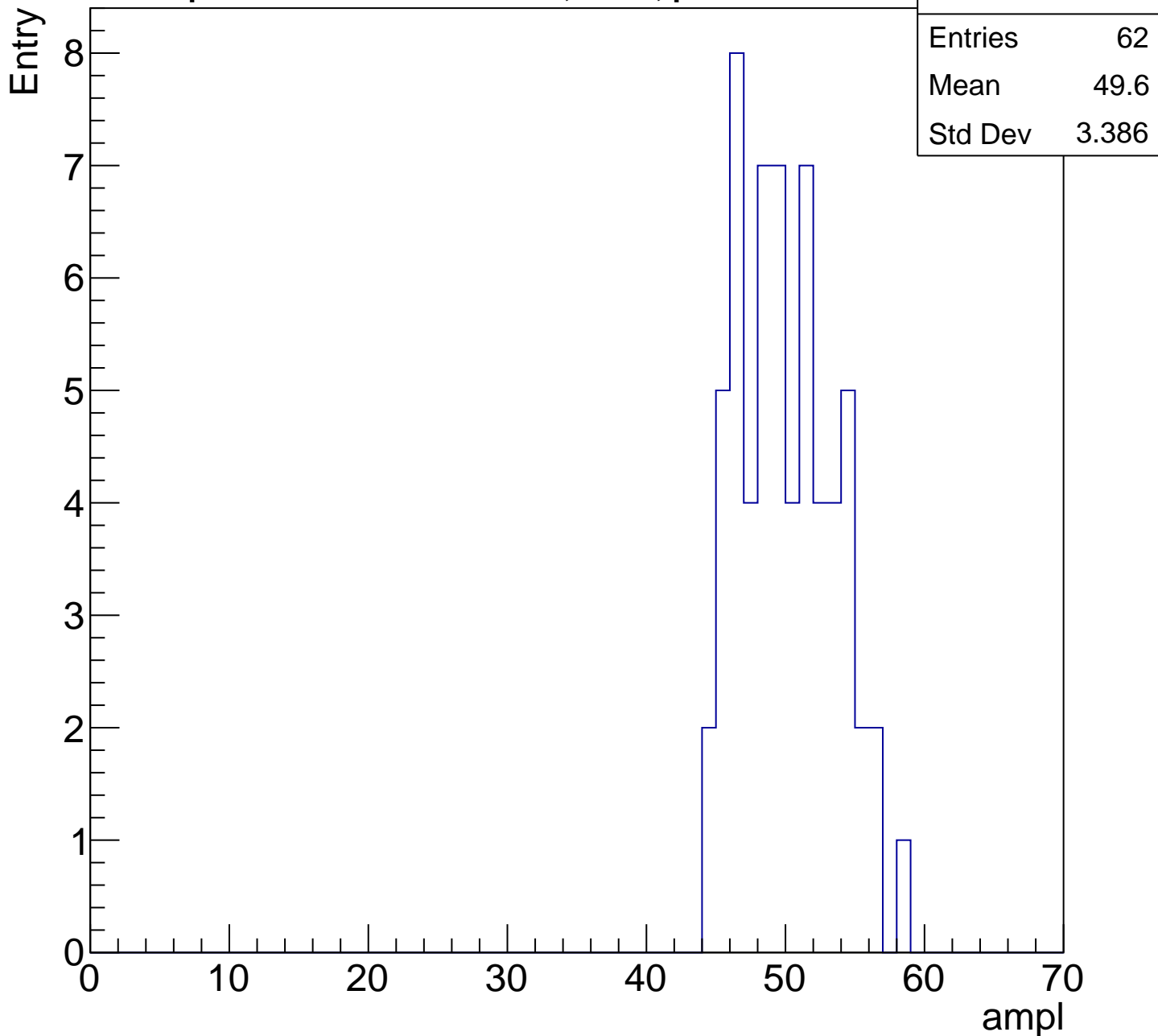
**Gaus mean : 42.2706**

**Gaus Width: 3.3413**



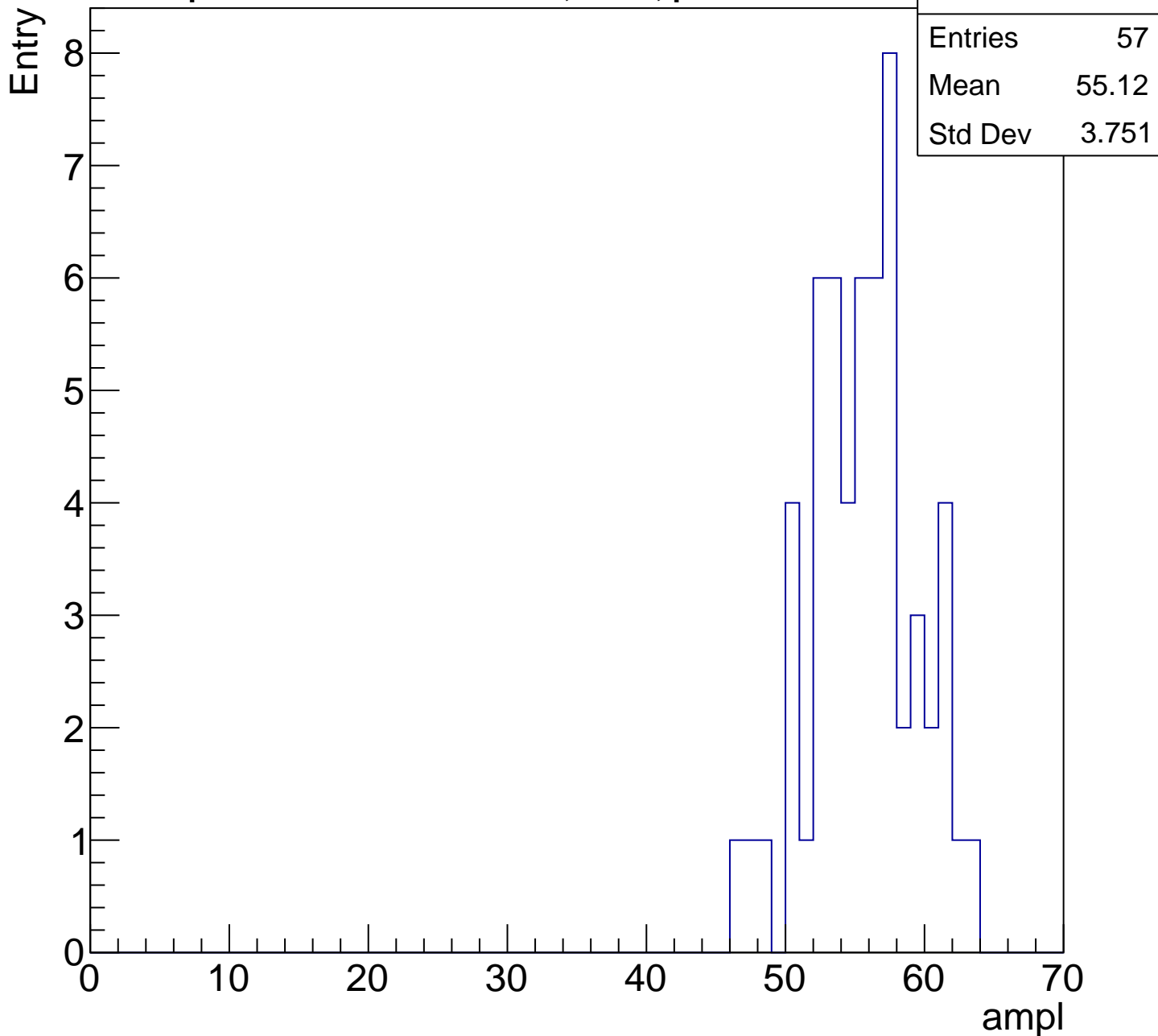
# B1L103S, U3-ch61, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U3-ch61, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

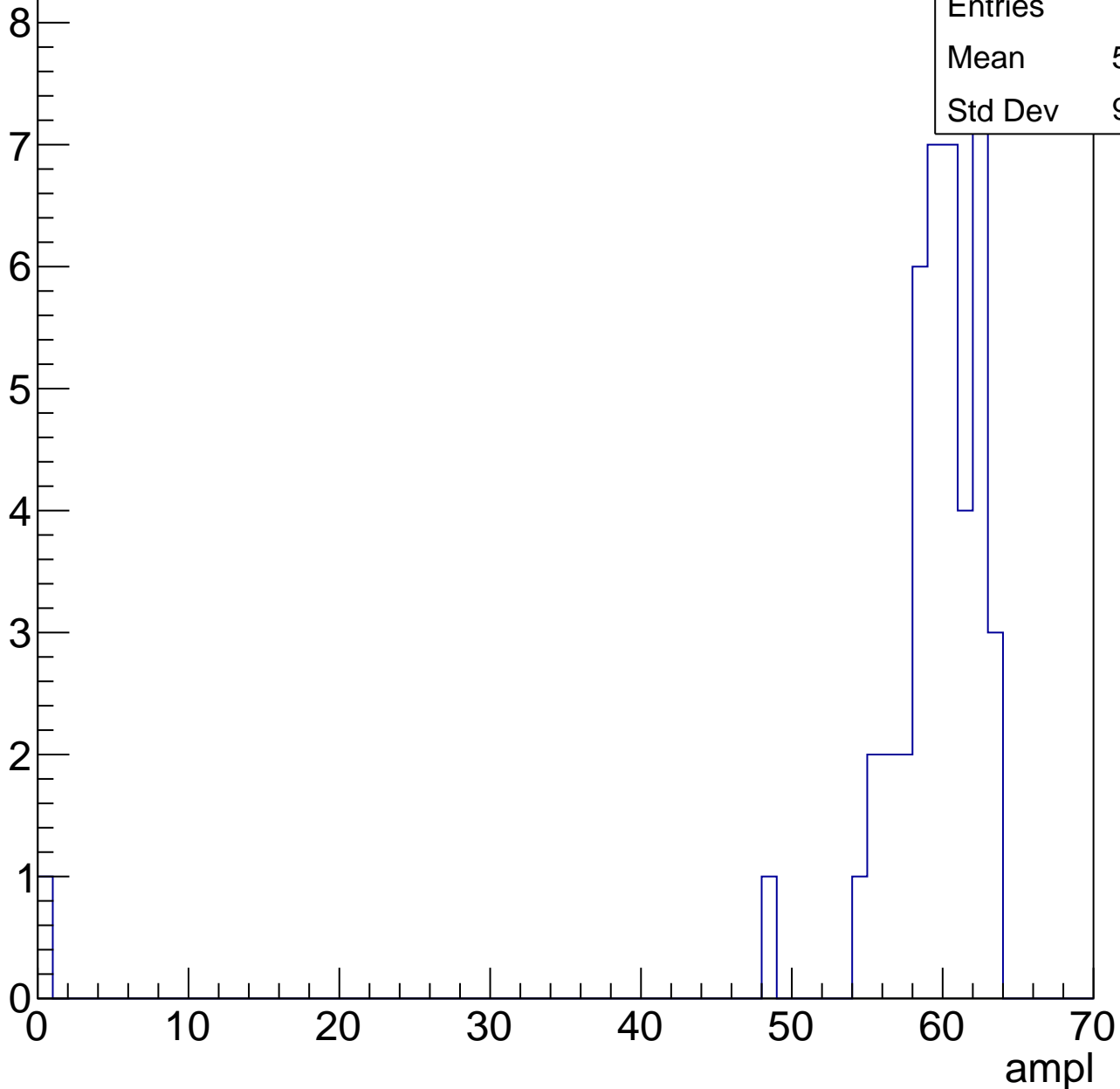


# B1L103S, U3-ch61, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	44
Mean	57.91
Std Dev	9.271

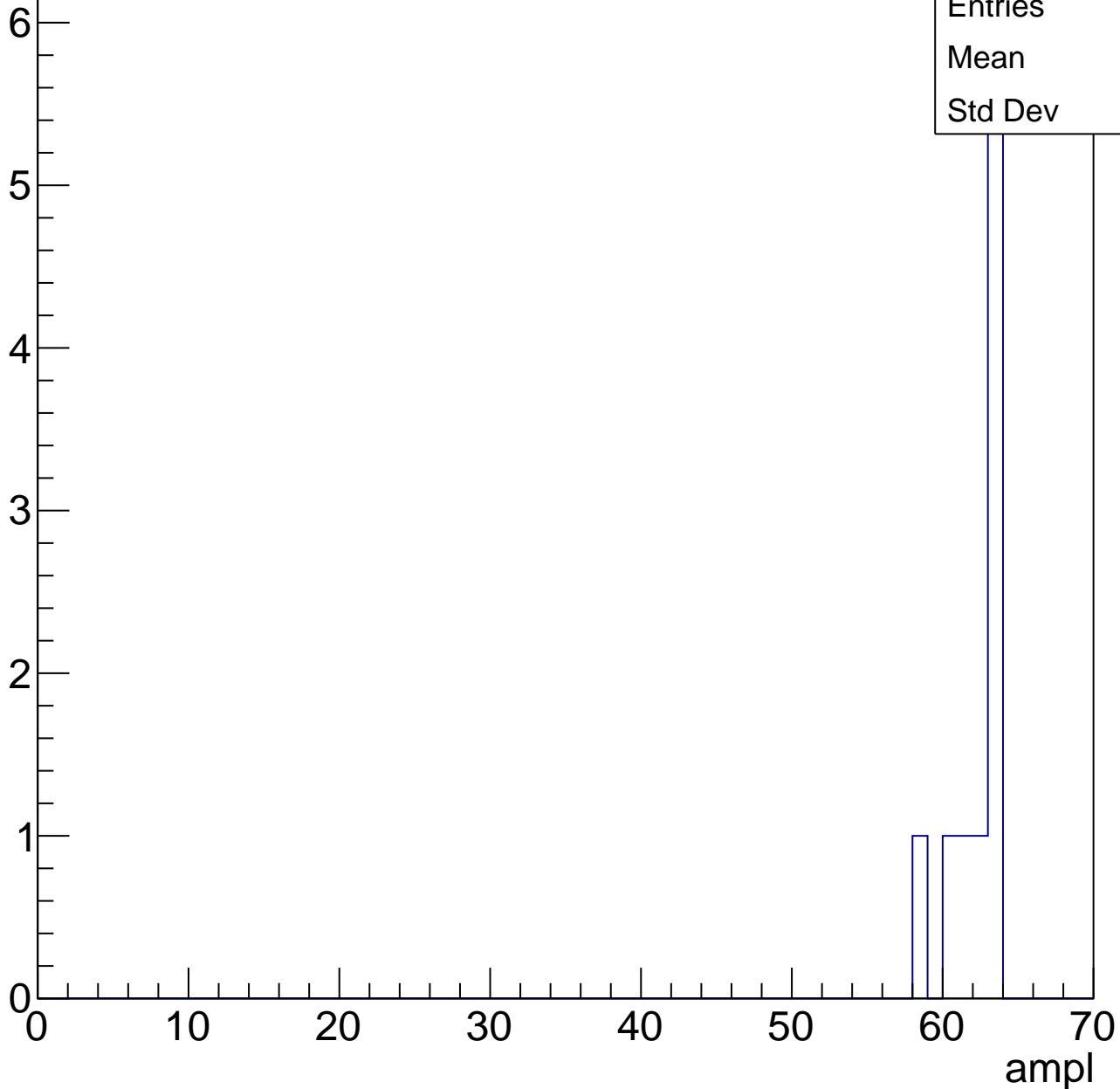


# B1L103S, U3-ch61, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	10
Mean	61.9
Std Dev	1.64





# B1L103S, U3-ch61, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	3
Mean	20.33
Std Dev	28.76

# B1L103S, U3-ch62, adc0

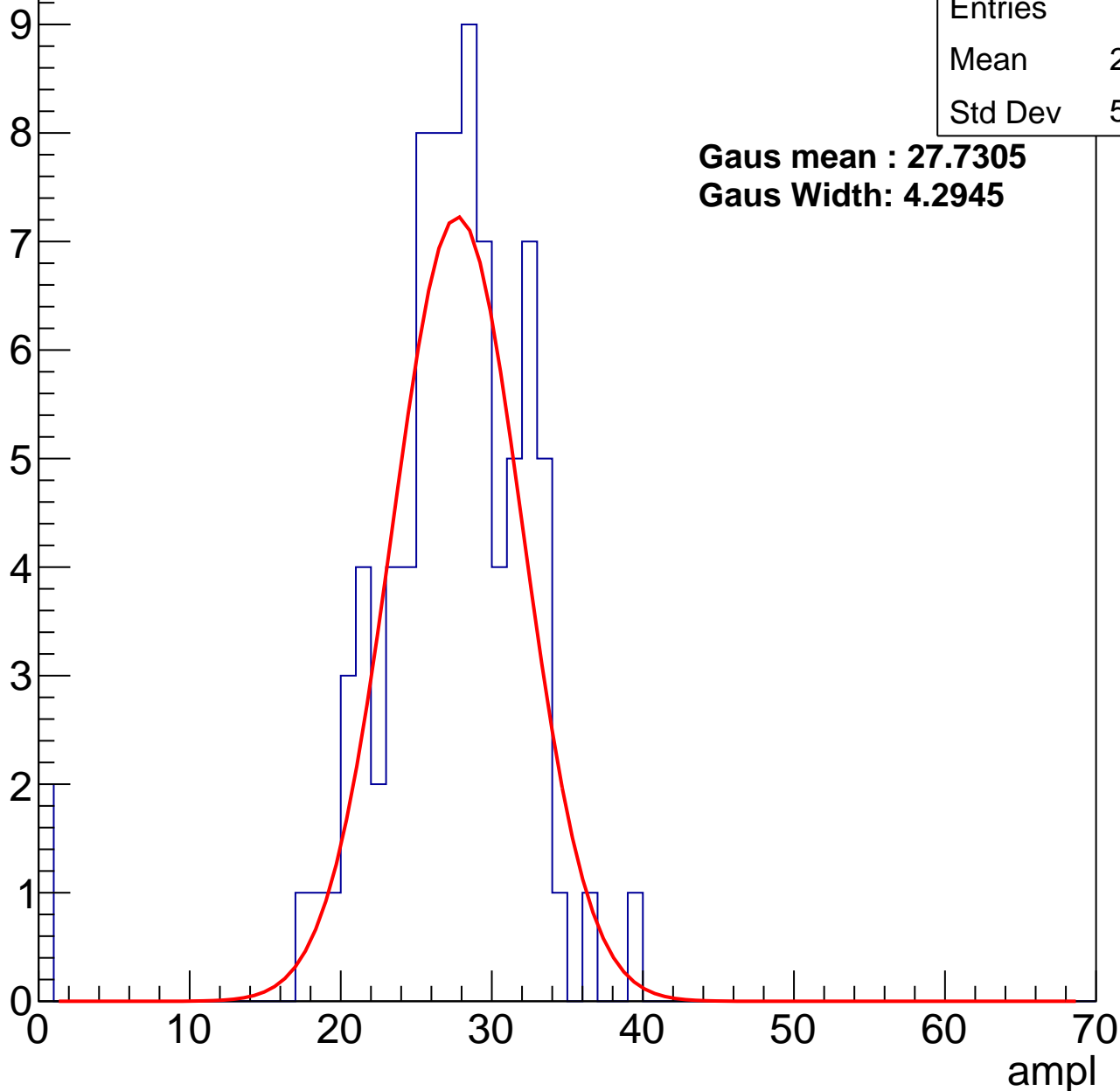
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	86
Mean	26.53
Std Dev	5.854

**Gaus mean : 27.7305**

**Gaus Width: 4.2945**



# B1L103S, U3-ch62, adc1

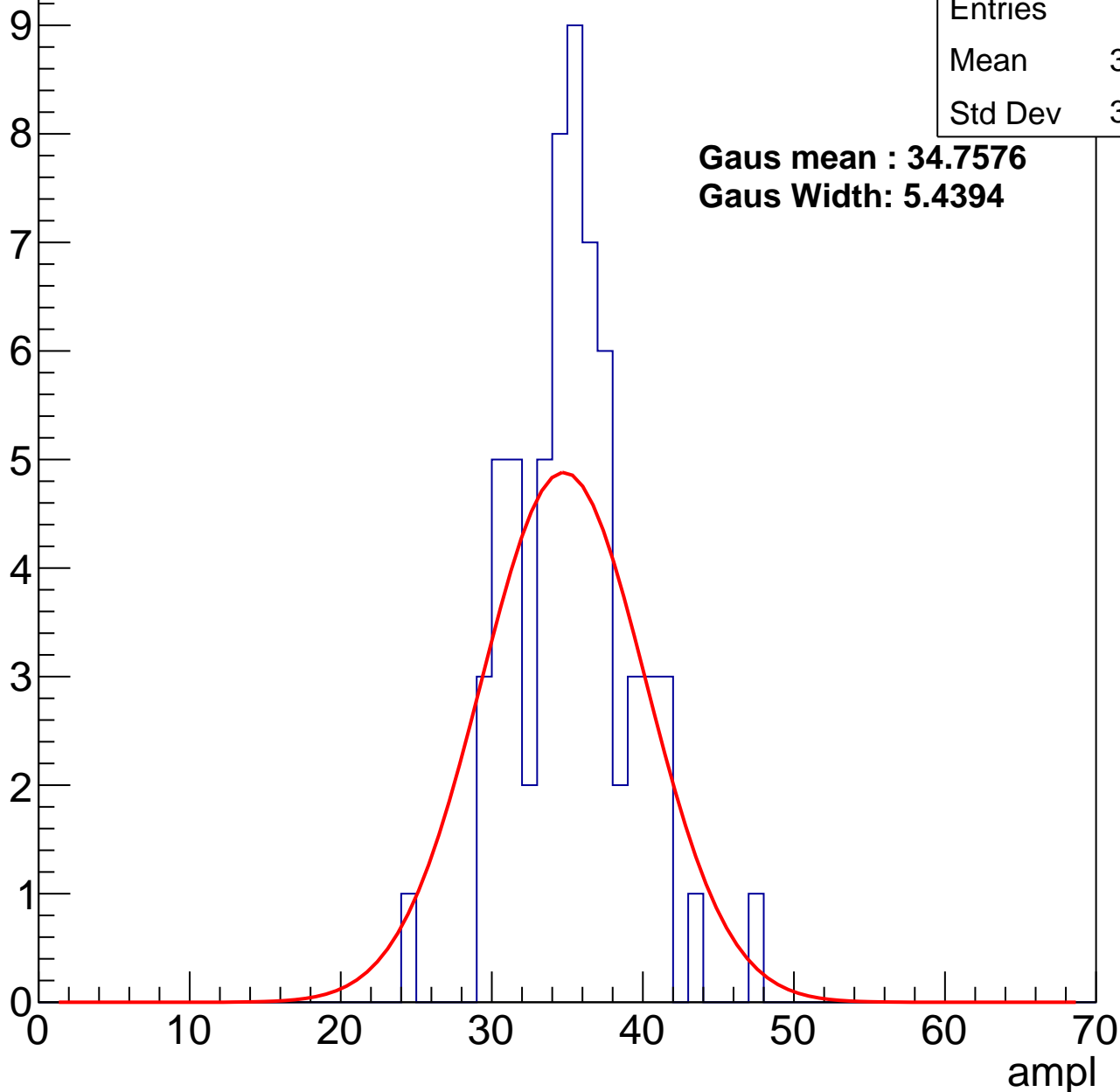
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	34.88
Std Dev	3.887

**Gaus mean : 34.7576**

**Gaus Width: 5.4394**



# B1L103S, U3-ch62, adc2

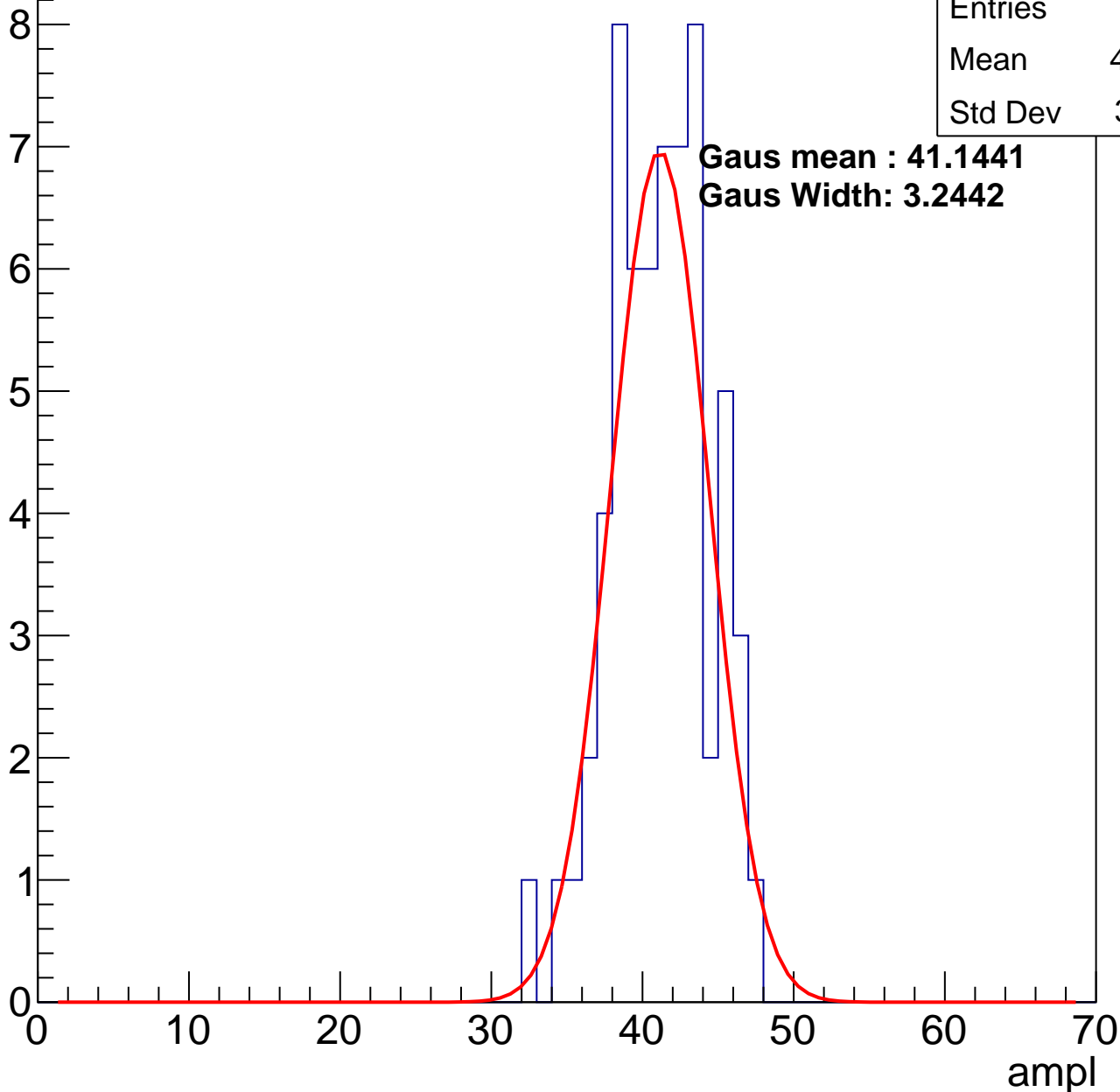
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	40.68
Std Dev	3.171

**Gaus mean : 41.1441**

**Gaus Width: 3.2442**

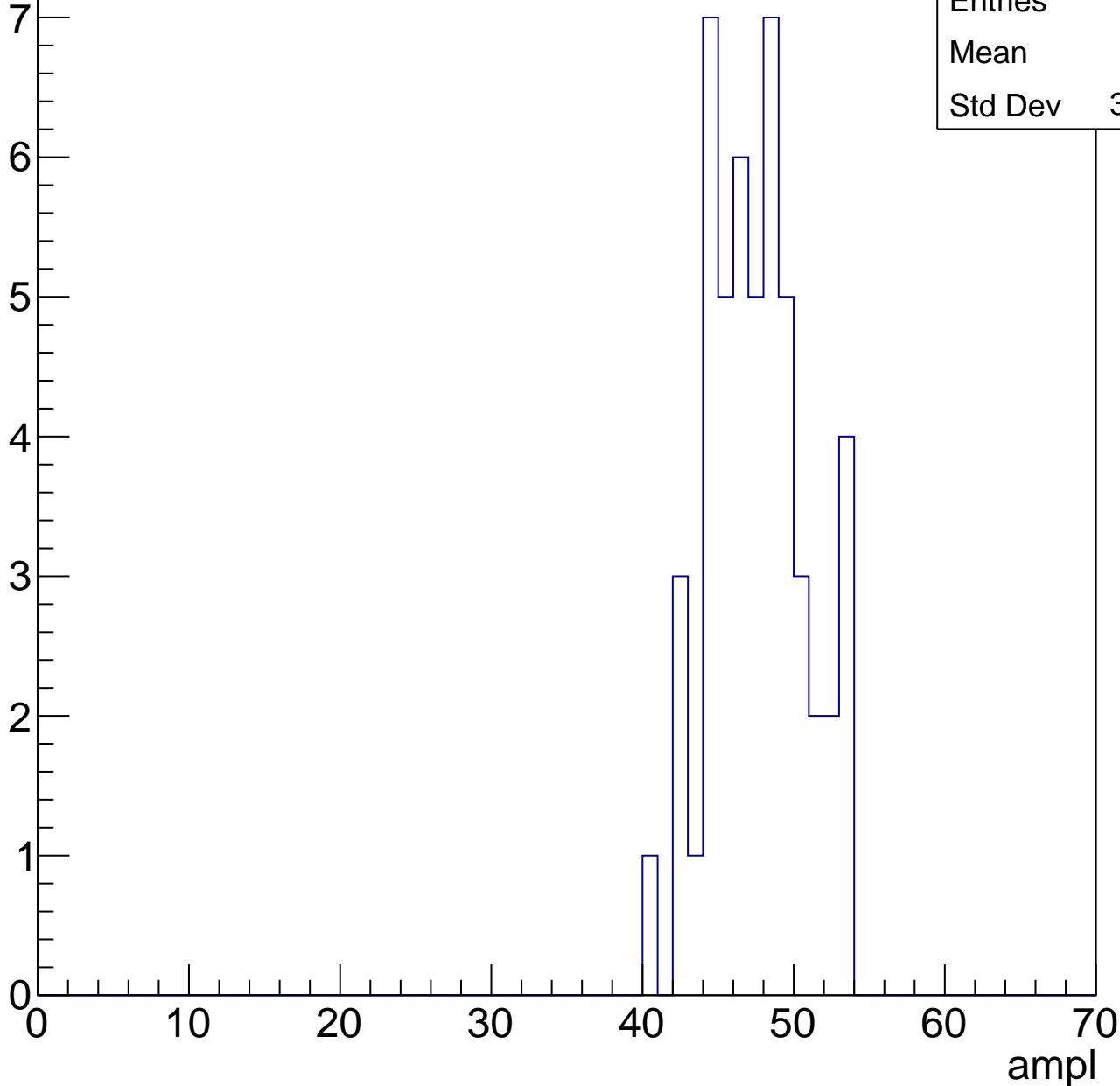


# B1L103S, U3-ch62, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

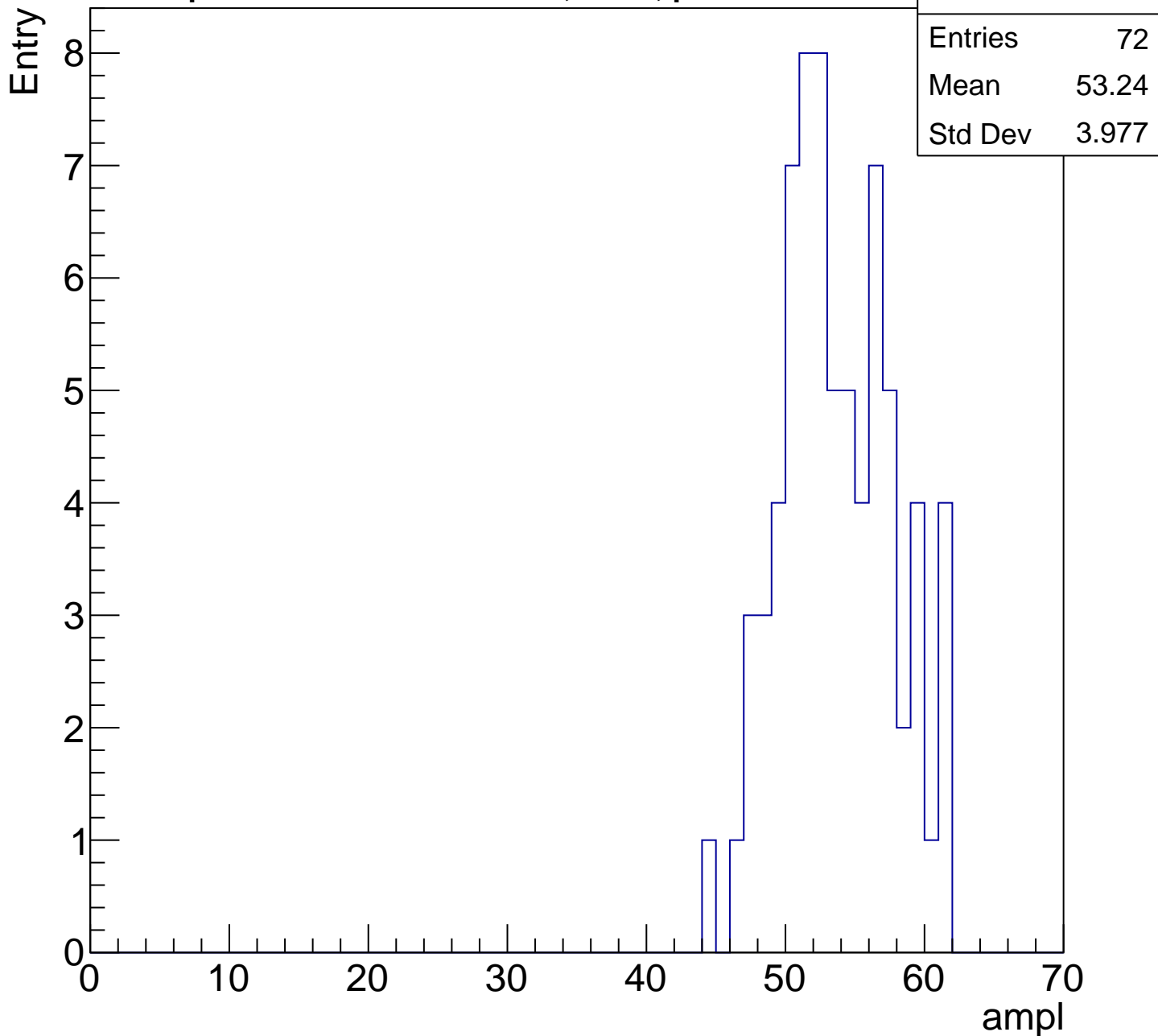
Entry

Entries	51
Mean	47.1
Std Dev	3.158



# B1L103S, U3-ch62, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U3-ch62, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

6

5

4

3

2

1

0

Entries 51

Mean 58.59

Std Dev 3.225

ampl

0

10

20

30

40

50

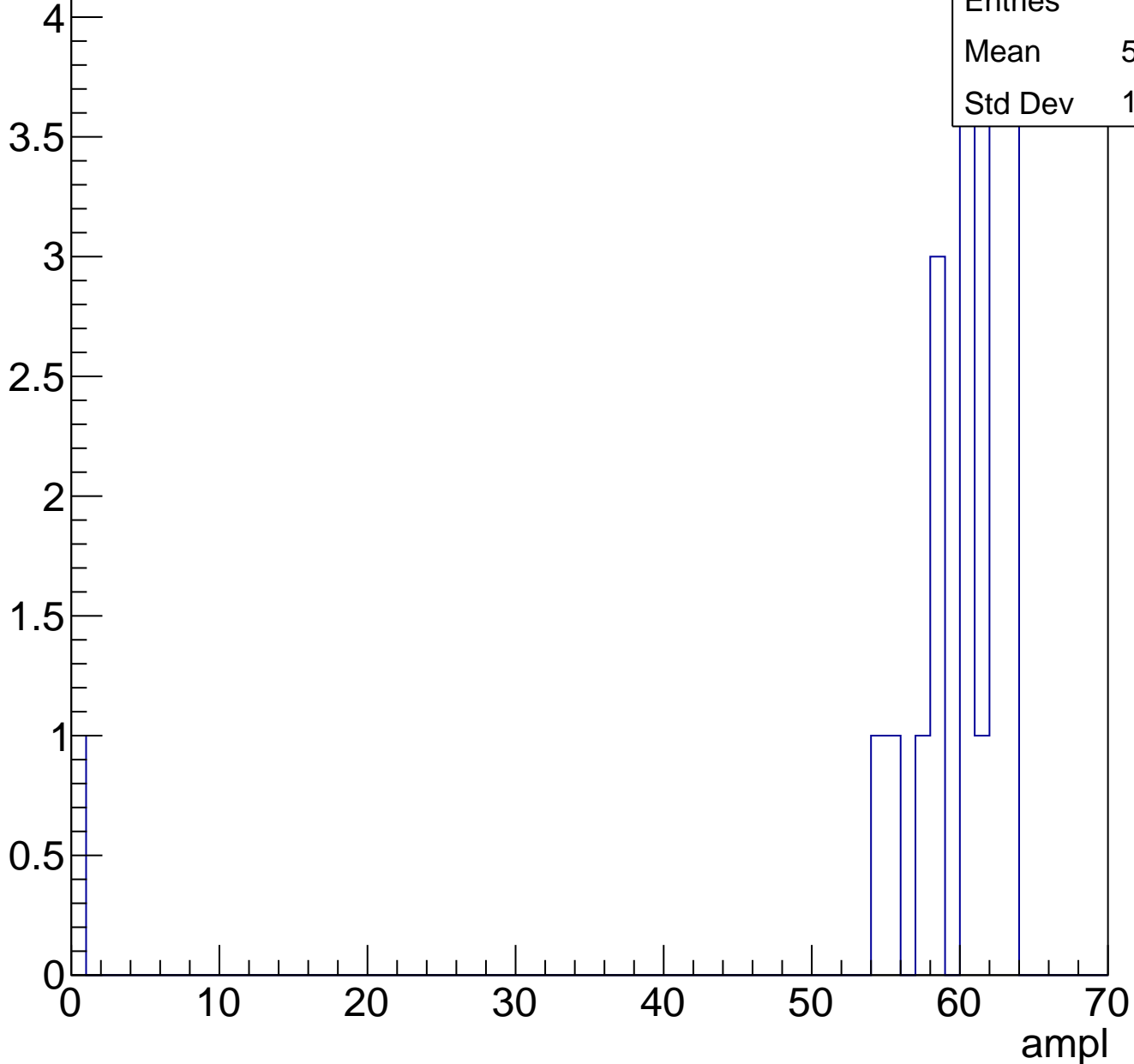
60

70

# B1L103S, U3-ch62, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U3-ch62, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L103S, U3-ch63, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	76
Mean	27.82
Std Dev	3.691

**Gaus mean : 28.2490**

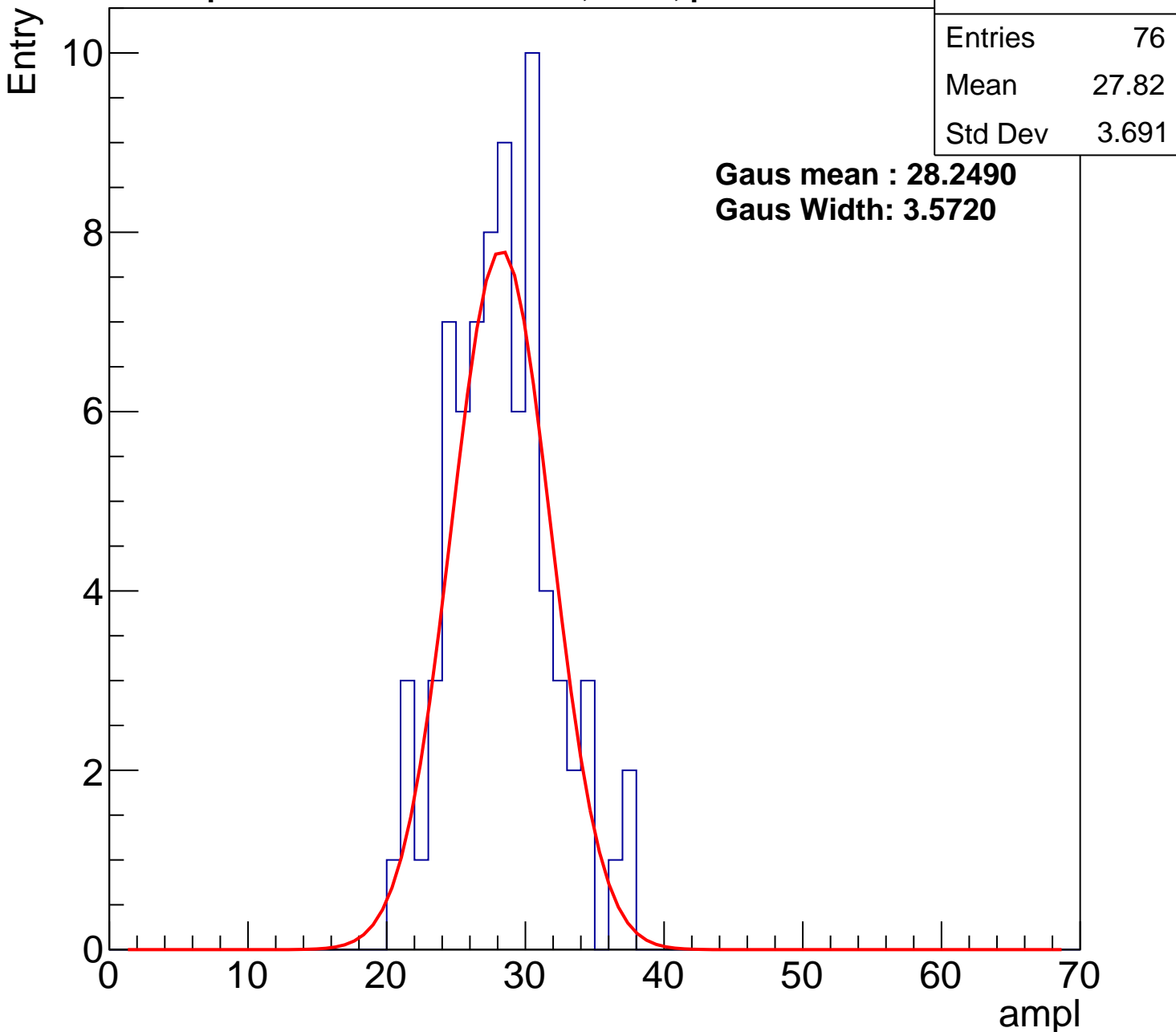
**Gaus Width: 3.5720**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U3-ch63, adc1

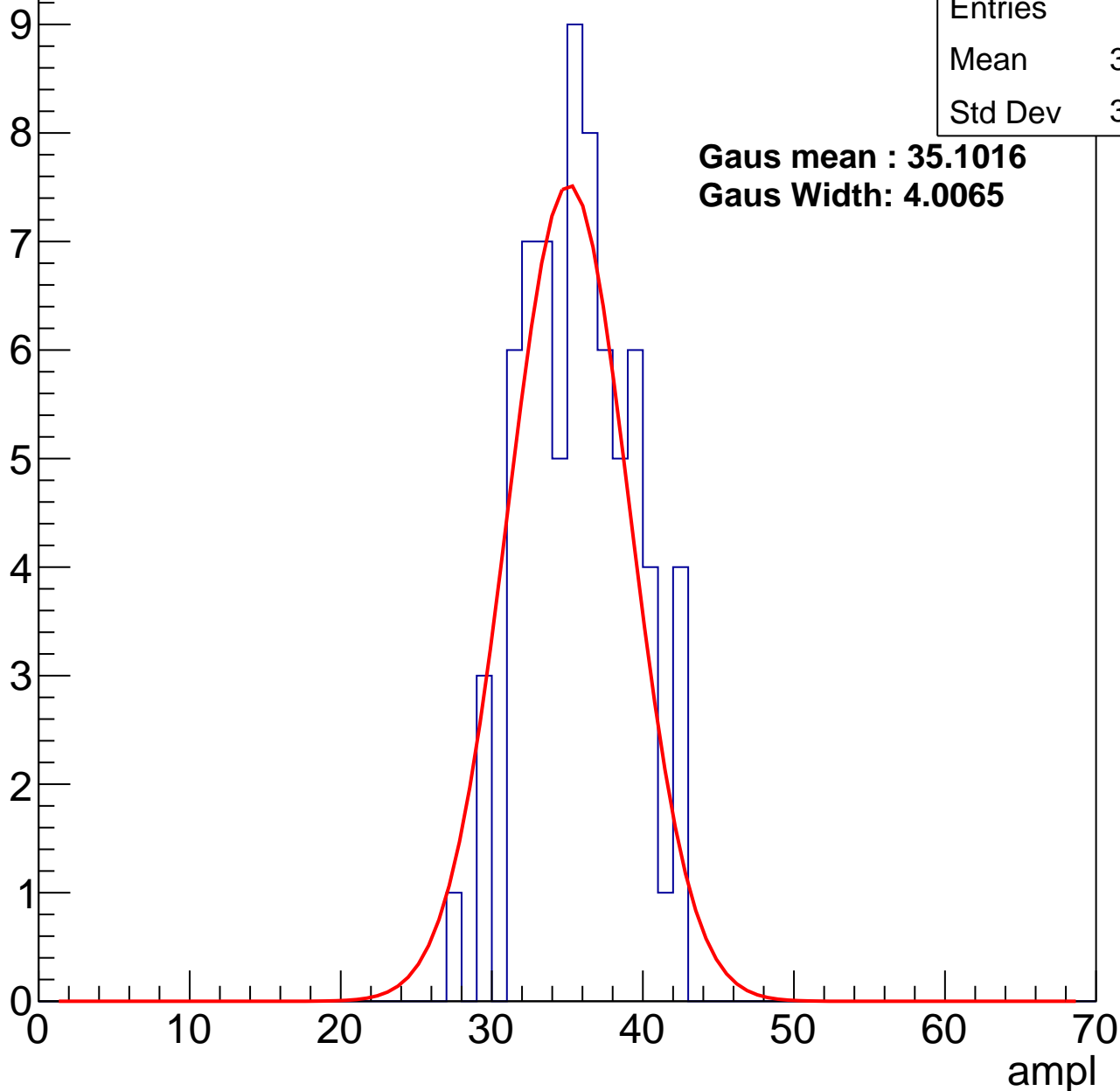
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	35.32
Std Dev	3.459

**Gaus mean : 35.1016**

**Gaus Width: 4.0065**



# B1L103S, U3-ch63, adc2

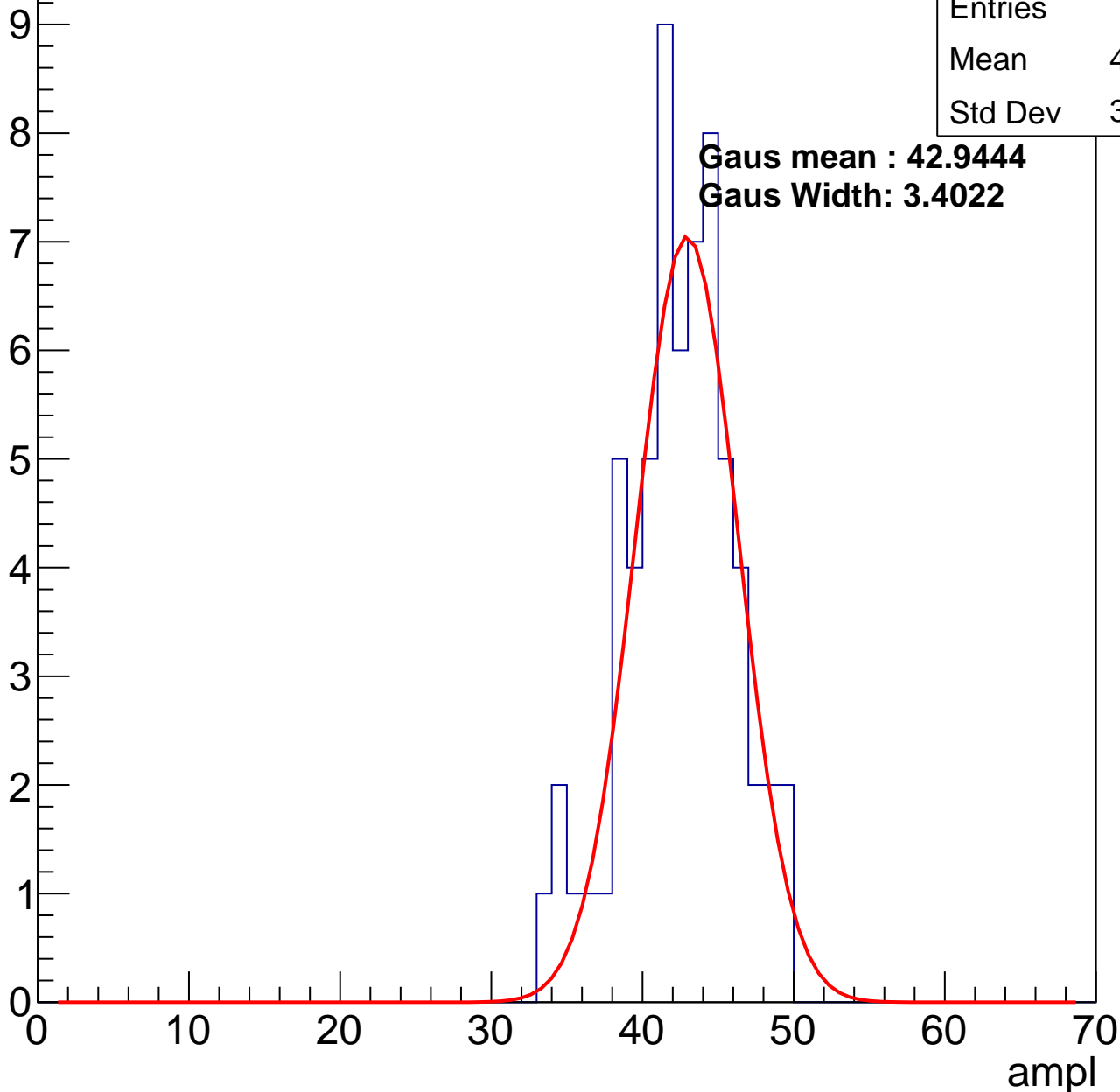
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	41.94
Std Dev	3.577

**Gaus mean : 42.9444**

**Gaus Width: 3.4022**

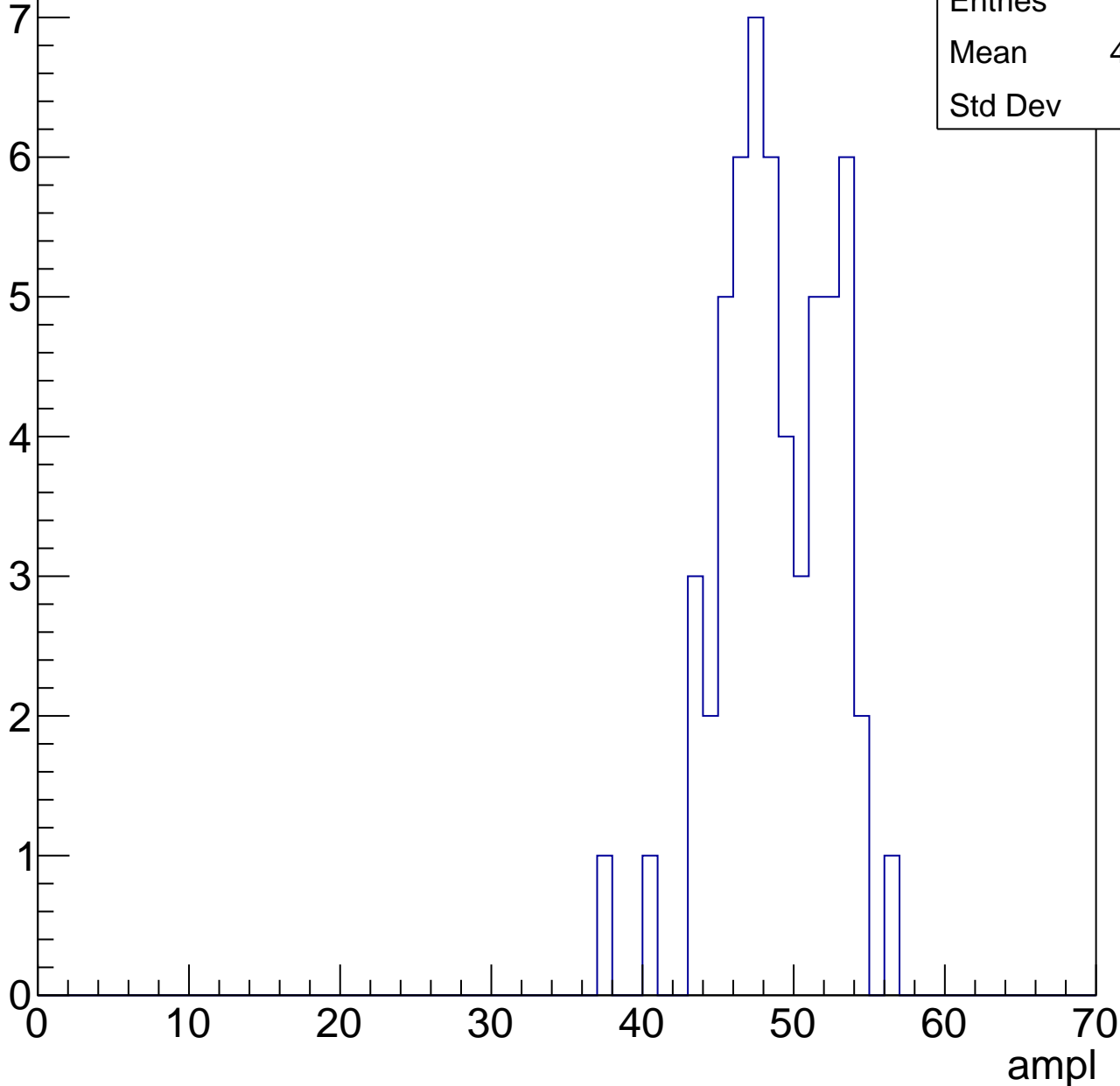


# B1L103S, U3-ch63, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

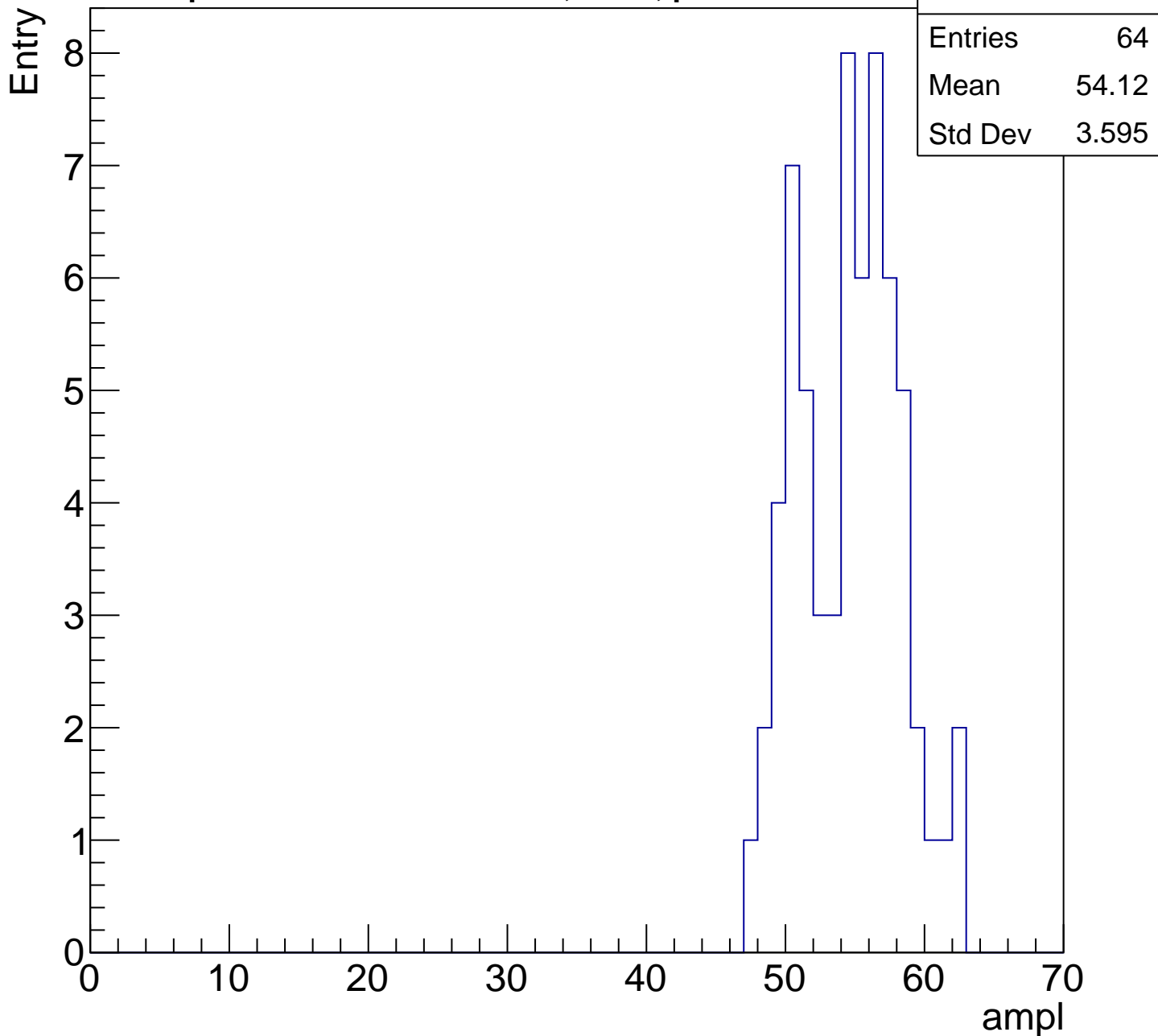
Entry

Entries	57
Mean	48.33
Std Dev	3.72



# B1L103S, U3-ch63, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U3-ch63, adc5

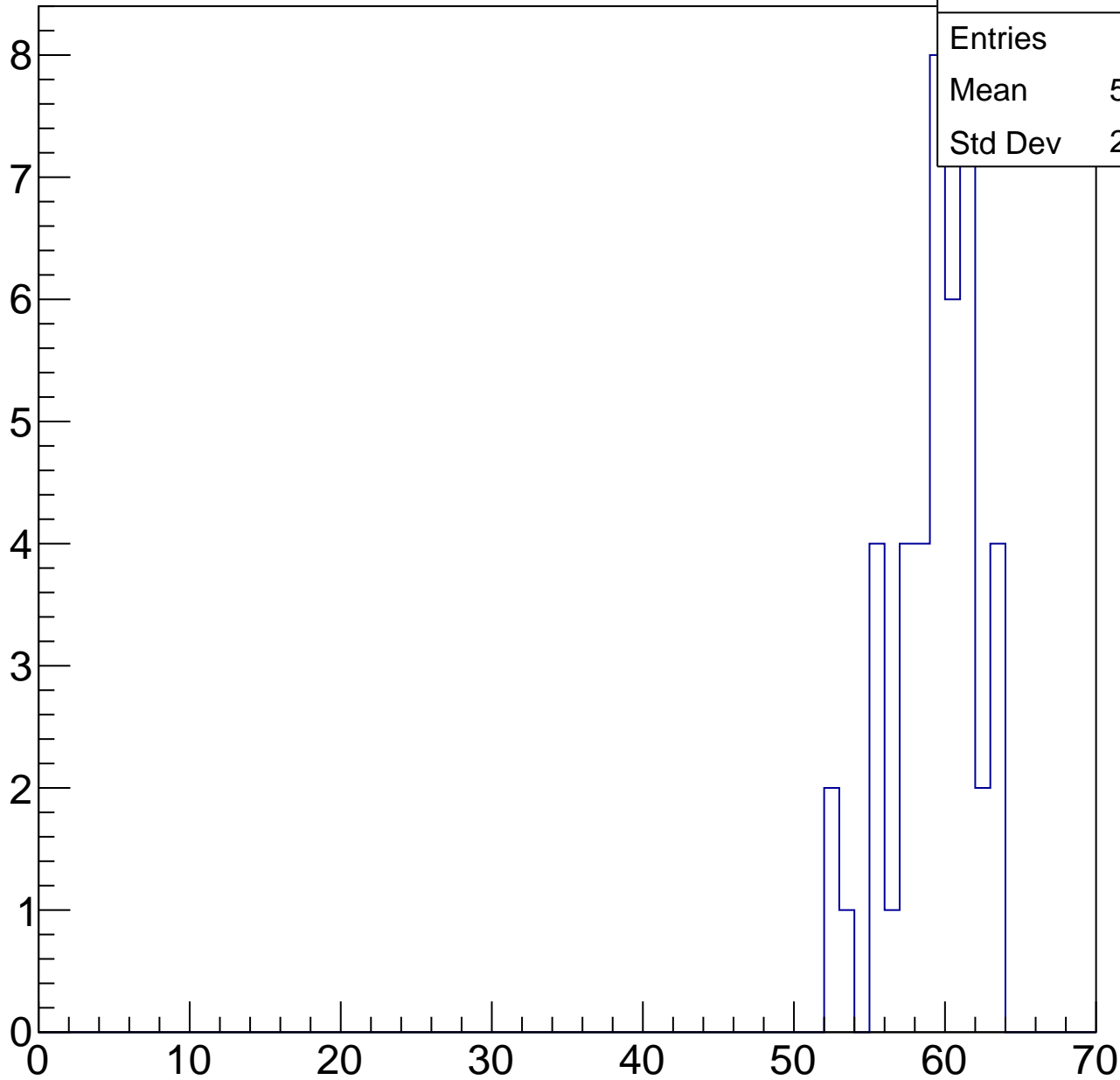
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	44
Mean	58.84
Std Dev	2.804

ampl

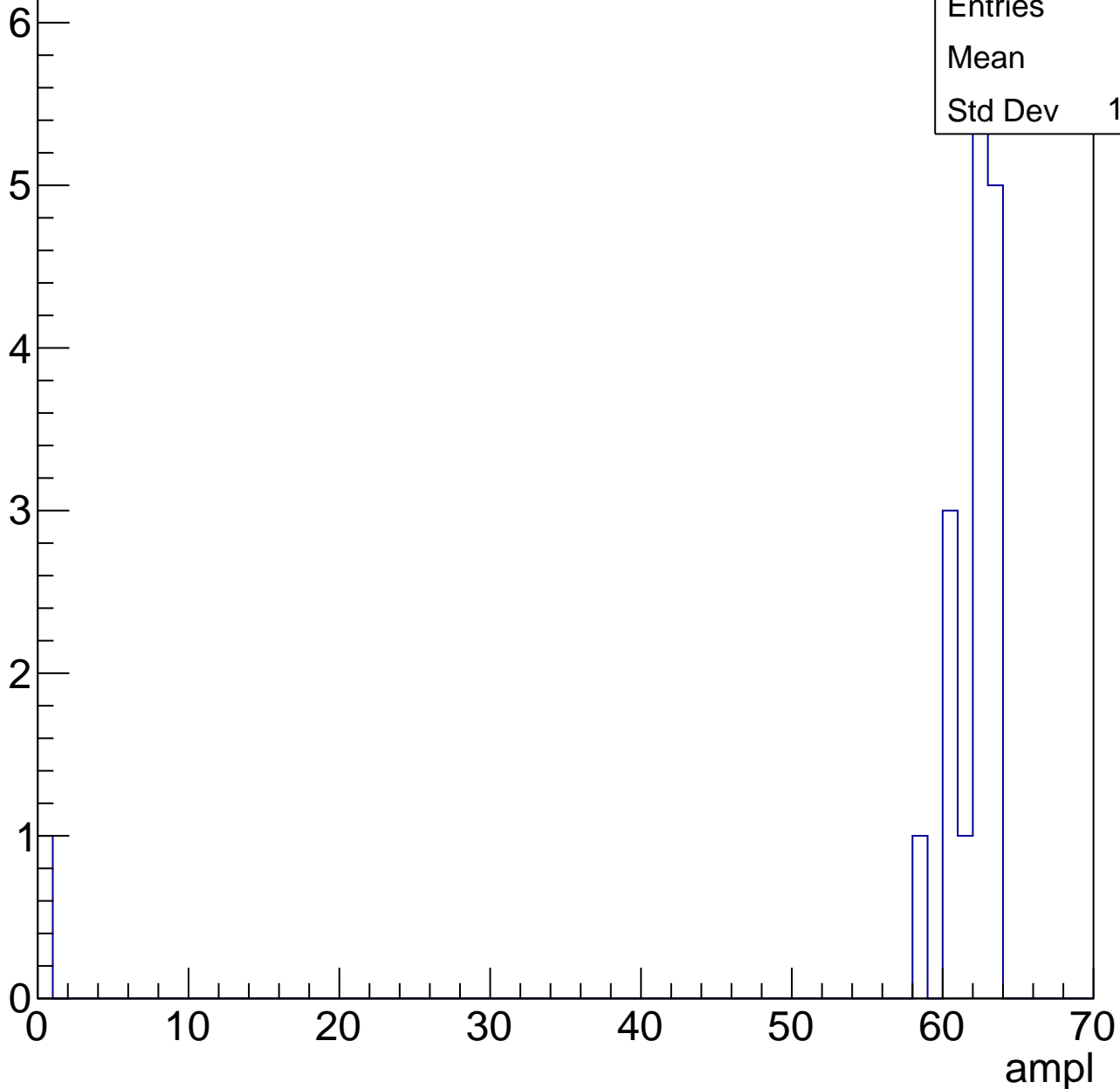


# B1L103S, U3-ch63, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	17
Mean	58
Std Dev	14.56





# B1L103S, U3-ch63, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch64, adc0

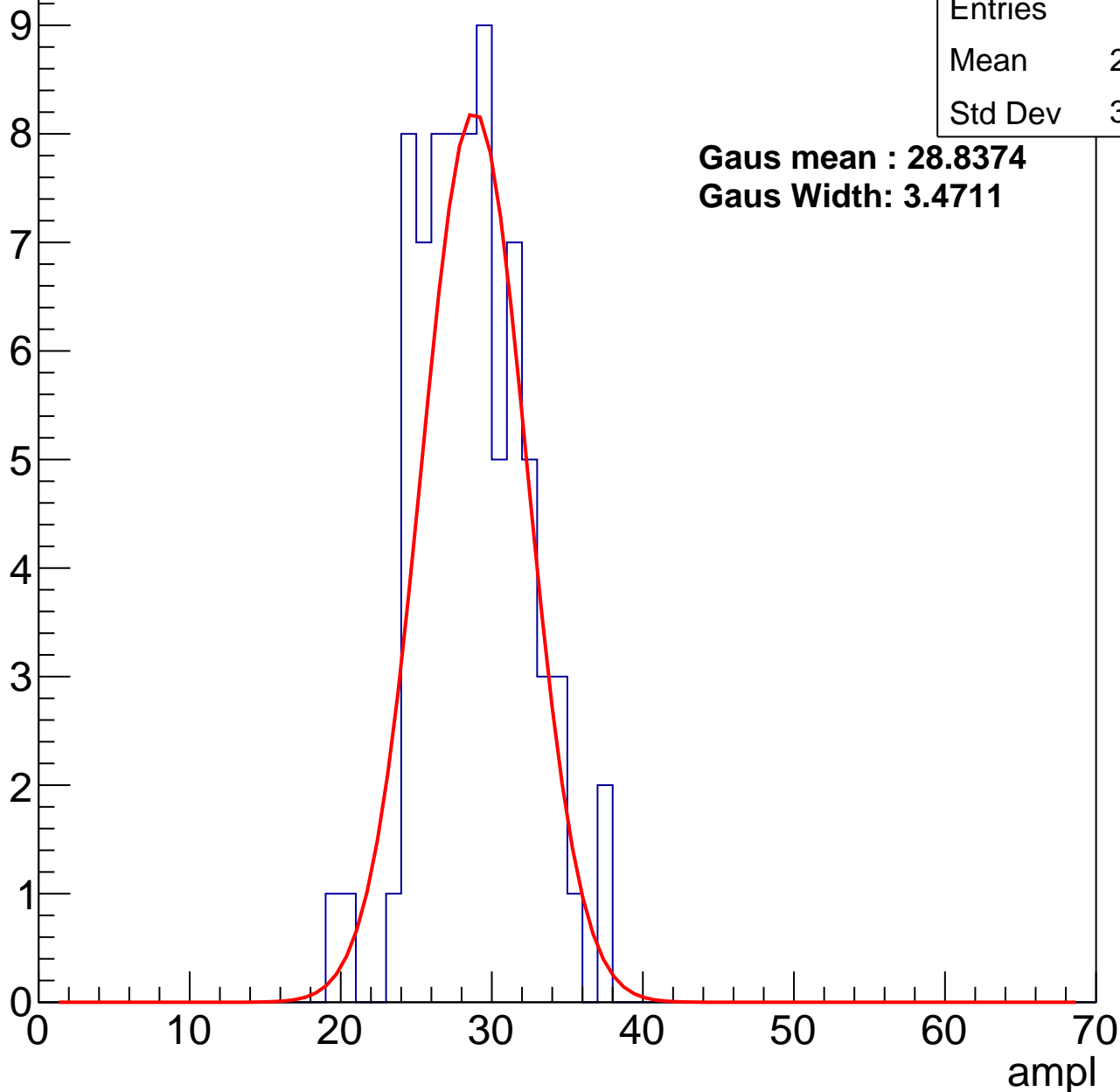
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	28.25
Std Dev	3.535

**Gaus mean : 28.8374**

**Gaus Width: 3.4711**



# B1L103S, U3-ch64, adc1

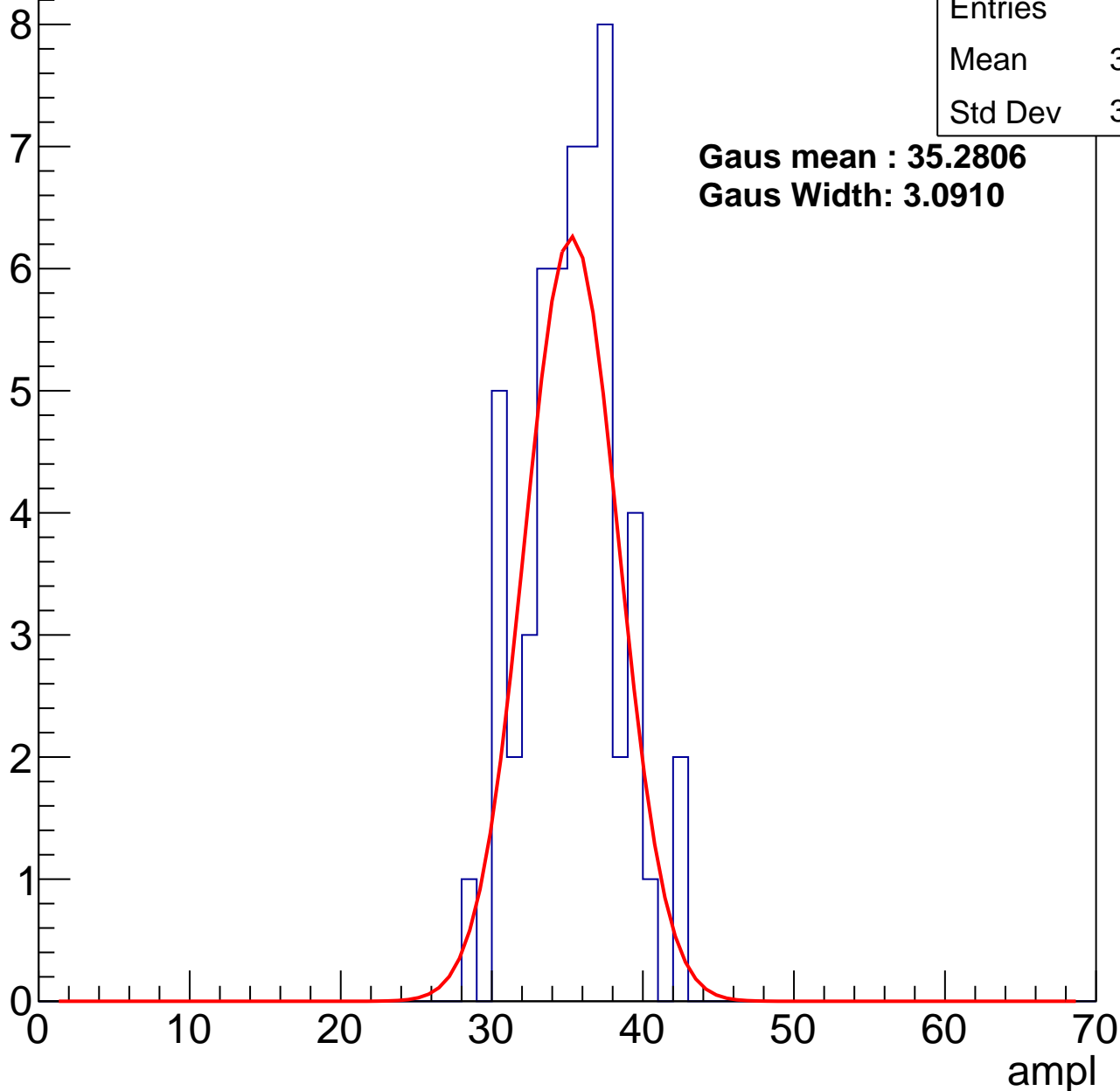
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	34.94
Std Dev	3.064

**Gaus mean : 35.2806**

**Gaus Width: 3.0910**



# B1L103S, U3-ch64, adc2

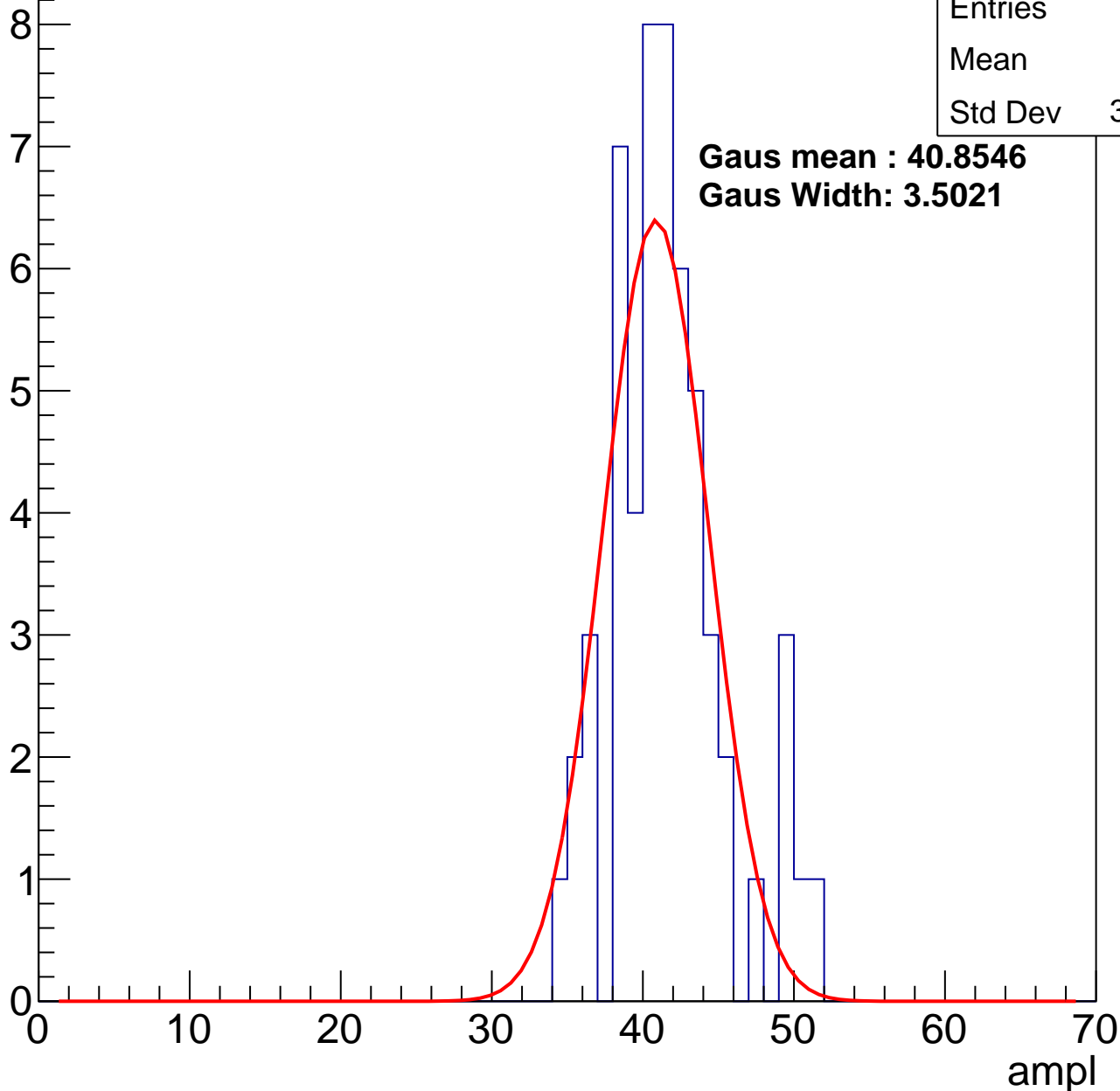
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	41.2
Std Dev	3.753

**Gaus mean : 40.8546**

**Gaus Width: 3.5021**



# B1L103S, U3-ch64, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

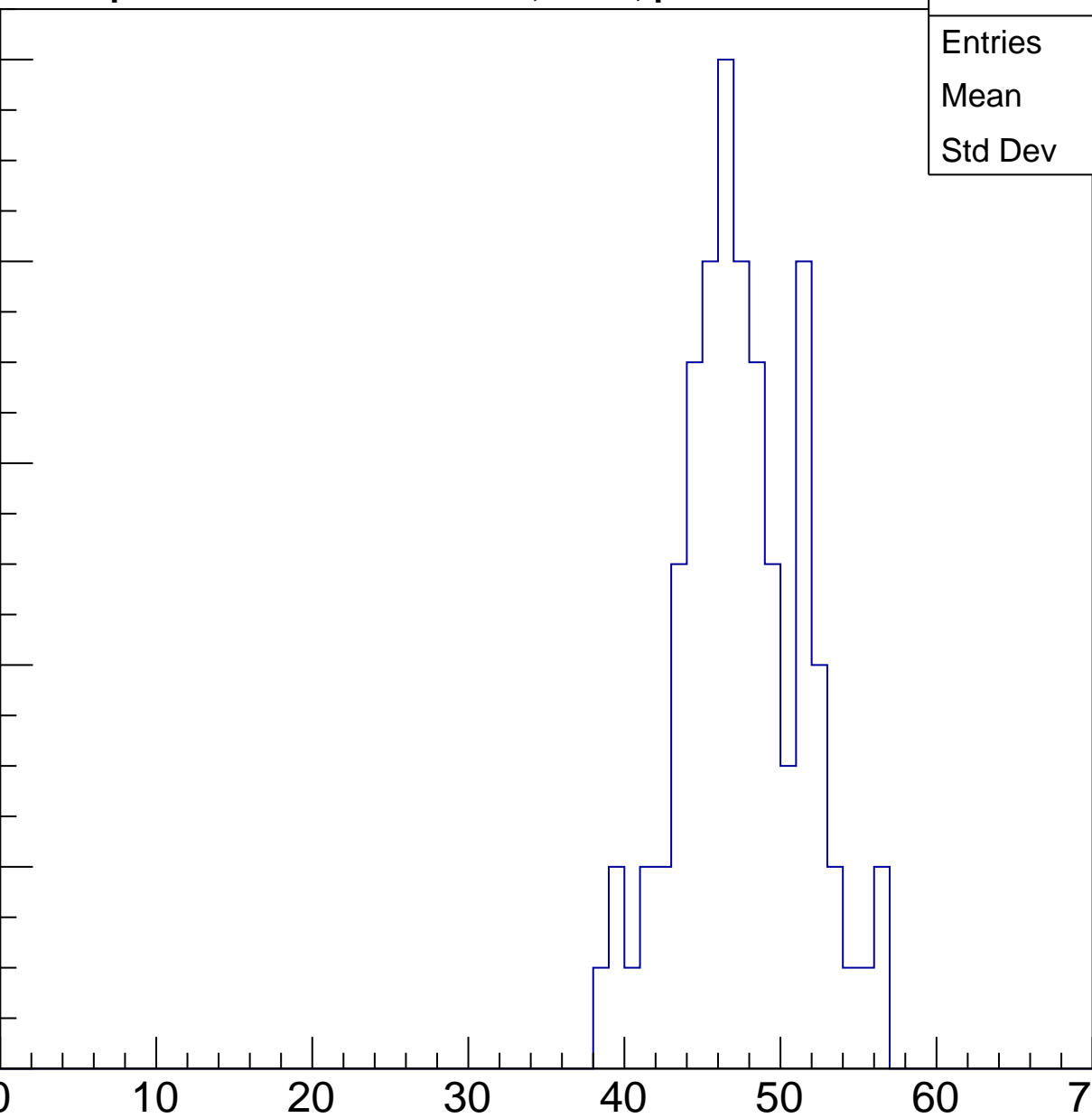
Entries	79
Mean	47.03
Std Dev	3.888

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

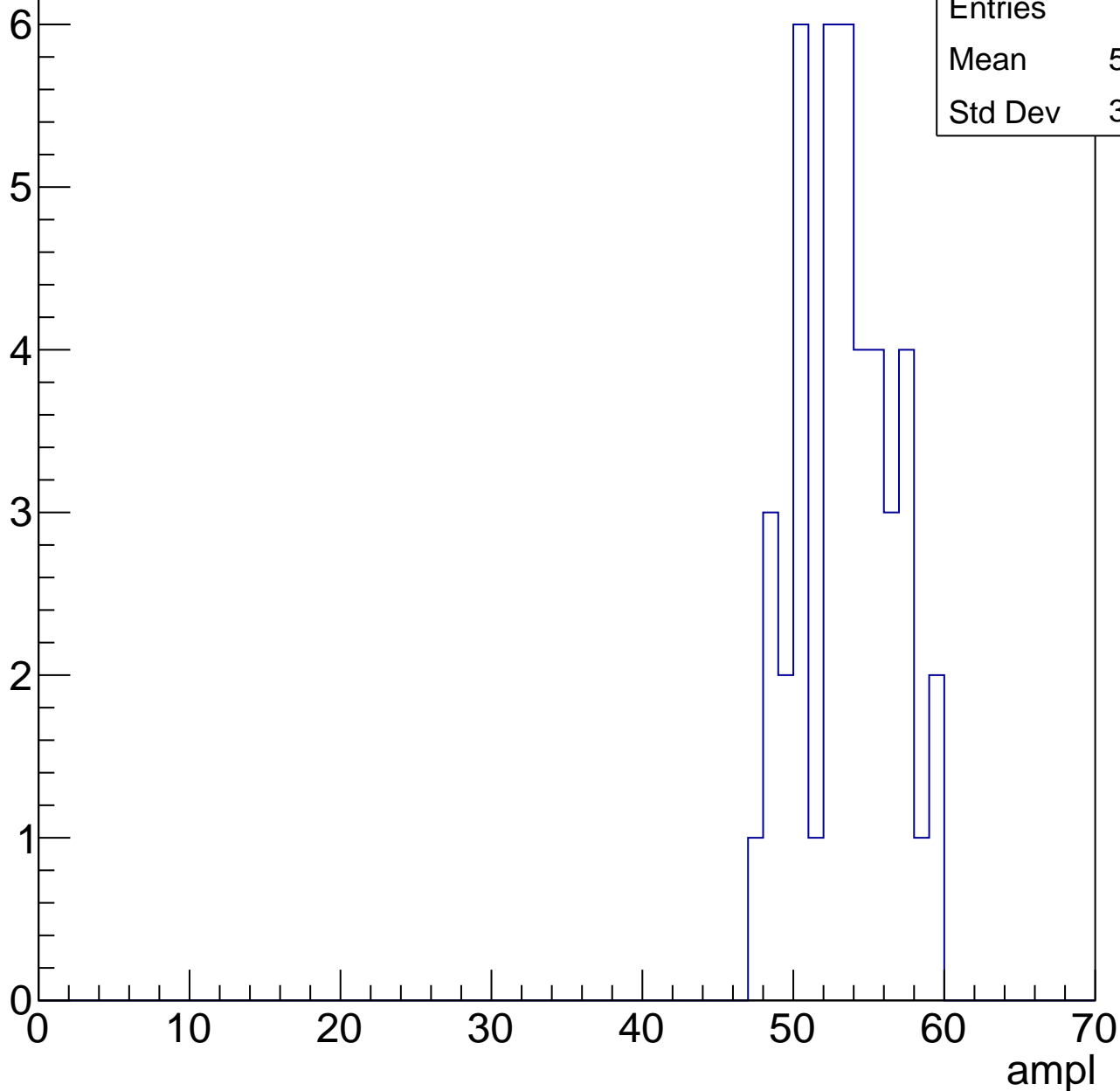


# B1L103S, U3-ch64, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

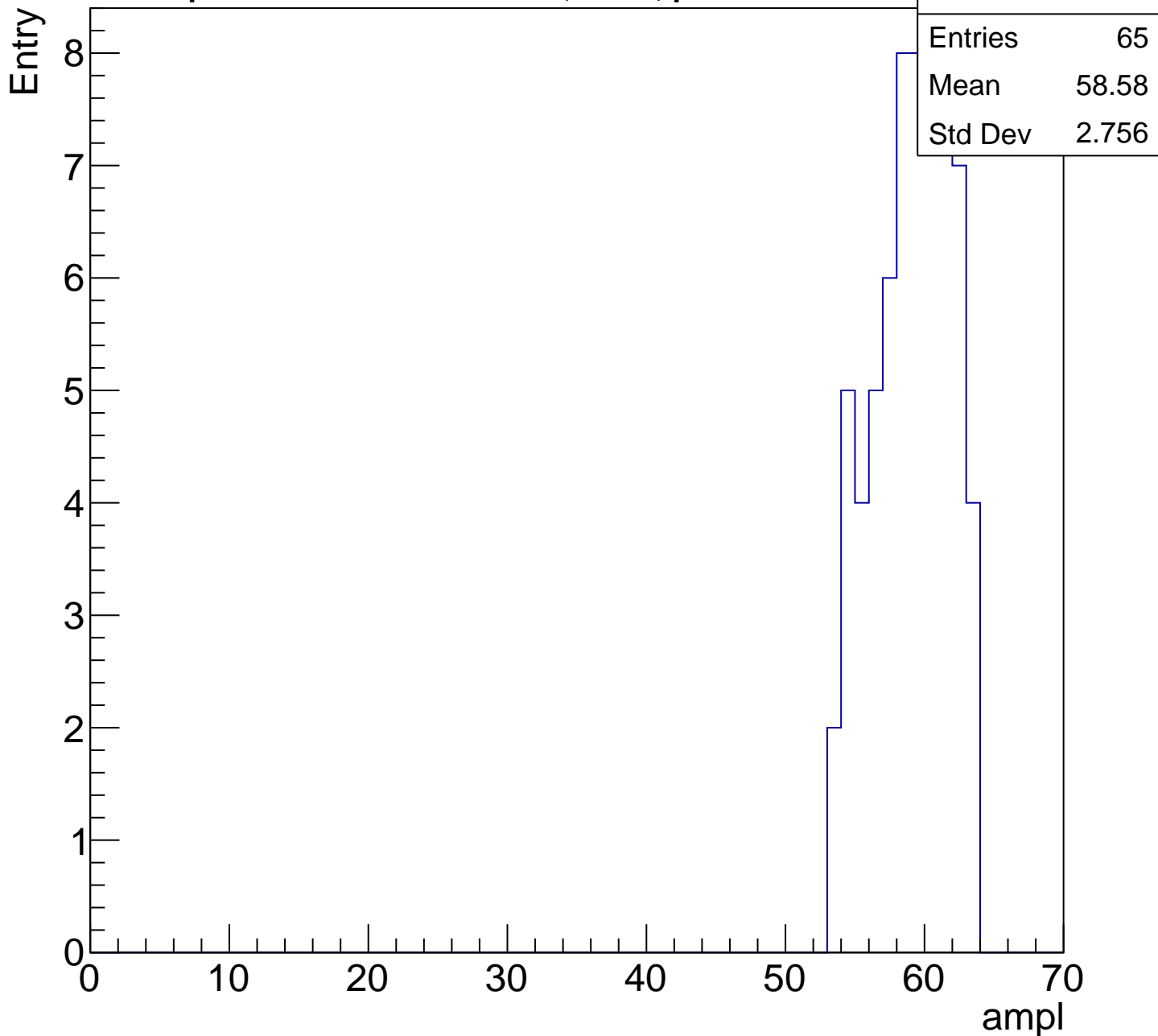
Entry

Entries	43
Mean	52.98
Std Dev	3.107



# B1L103S, U3-ch64, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

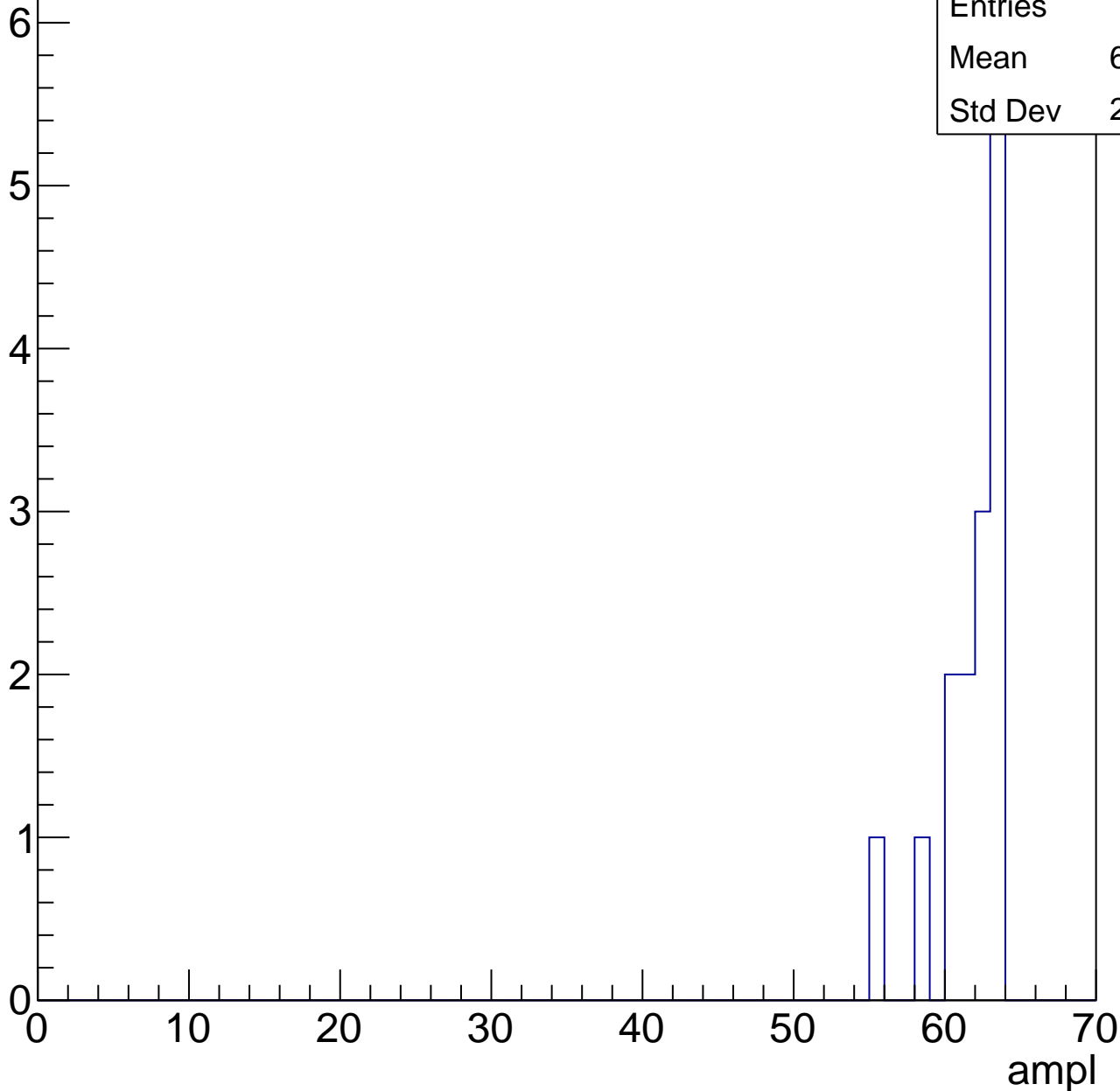


# B1L103S, U3-ch64, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	15
Mean	61.27
Std Dev	2.205





# B1L103S, U3-ch64, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch65, adc0

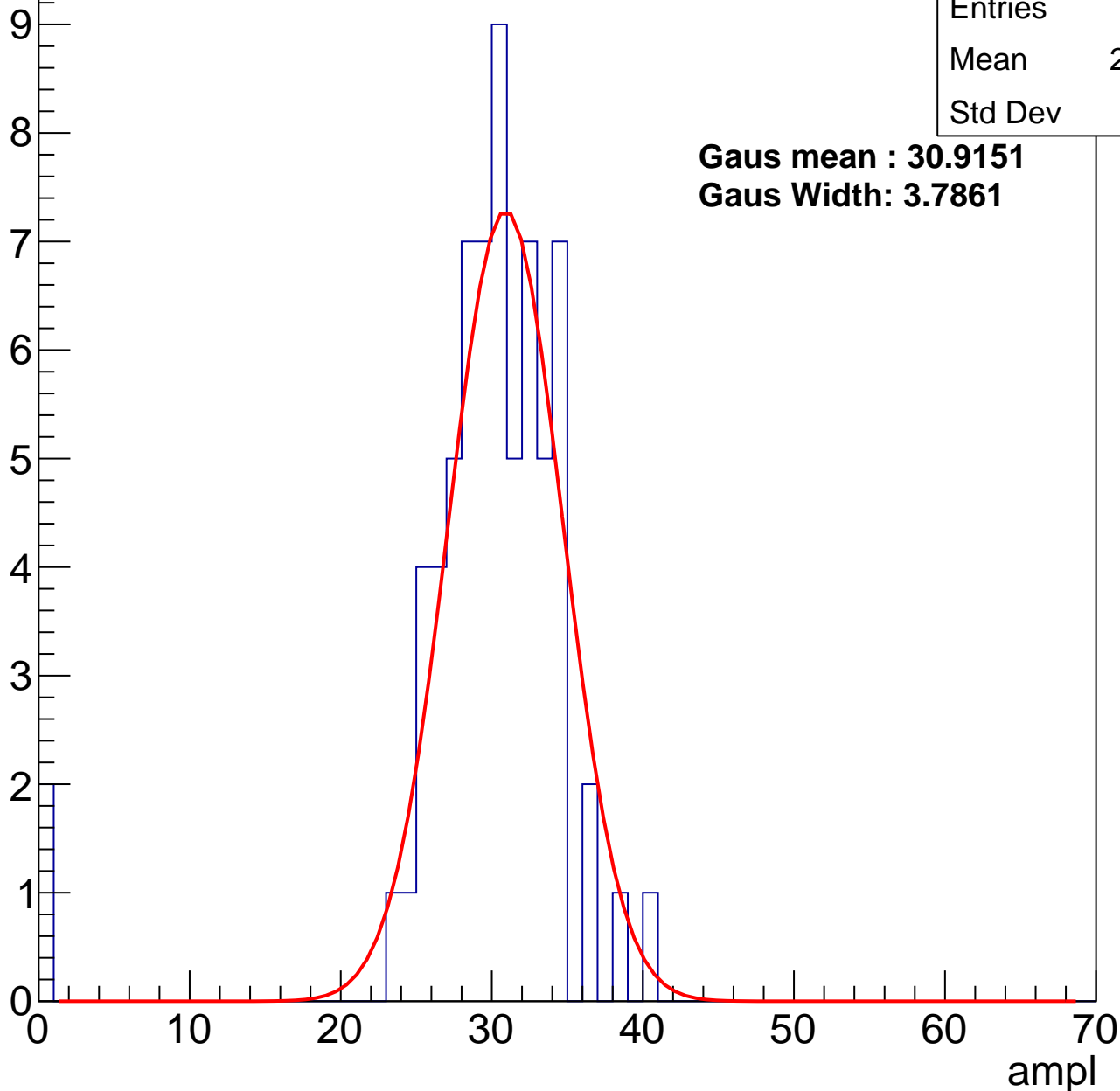
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	29.22
Std Dev	6.08

**Gaus mean : 30.9151**

**Gaus Width: 3.7861**



# B1L103S, U3-ch65, adc1

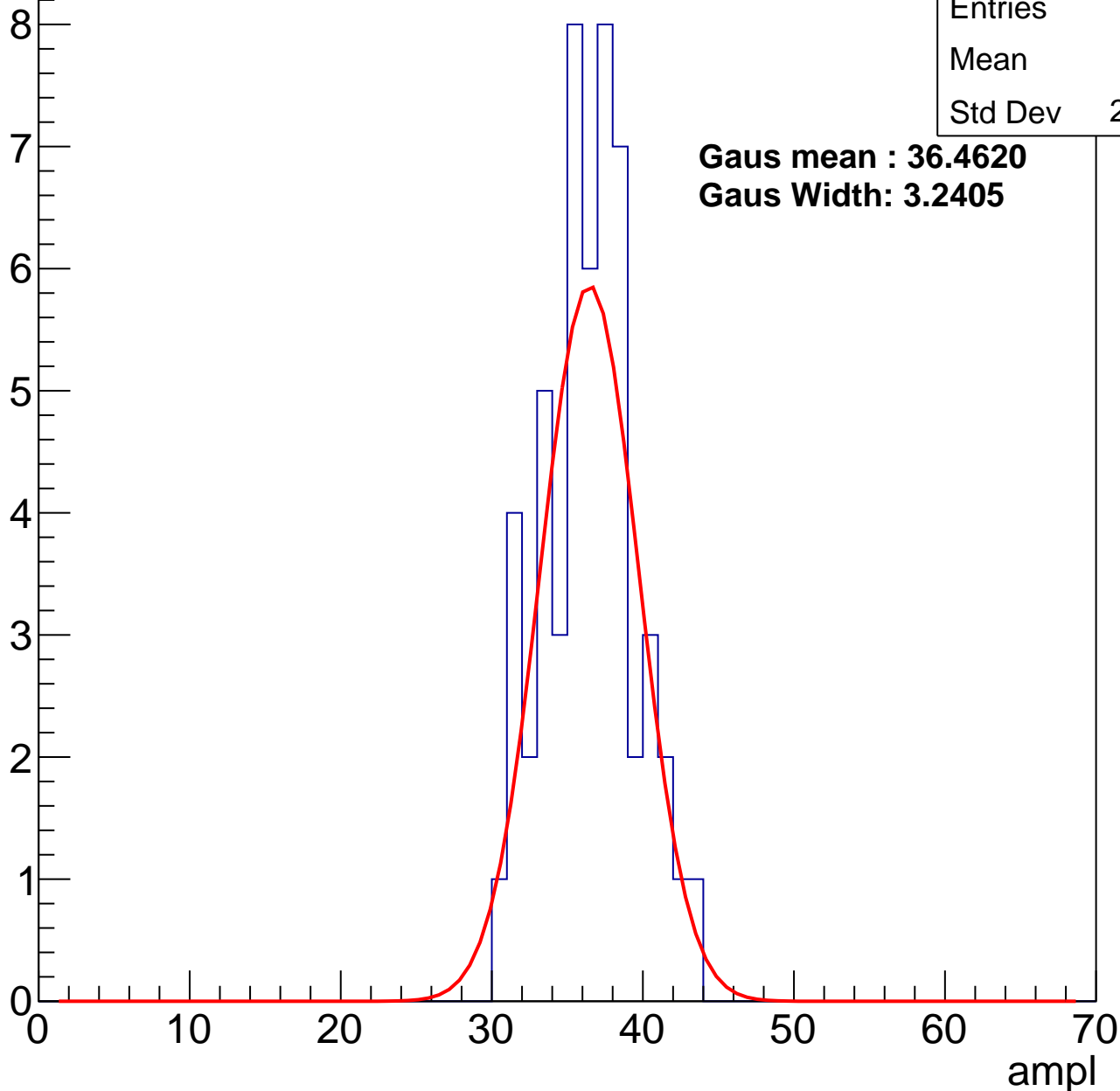
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	36
Std Dev	2.978

**Gaus mean : 36.4620**

**Gaus Width: 3.2405**



# B1L103S, U3-ch65, adc2

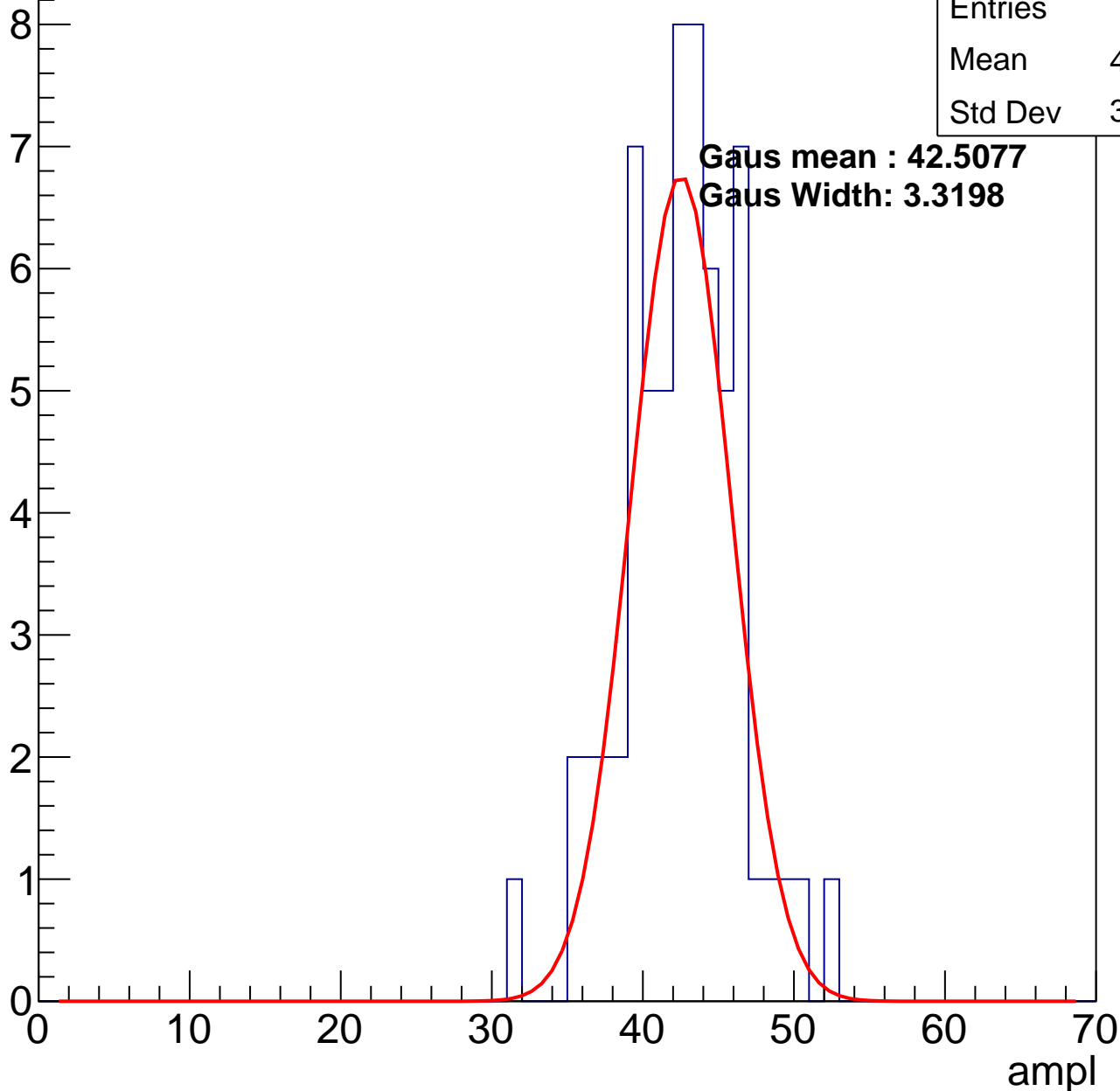
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	42.12
Std Dev	3.768

**Gaus mean : 42.5077**

**Gaus Width: 3.3198**

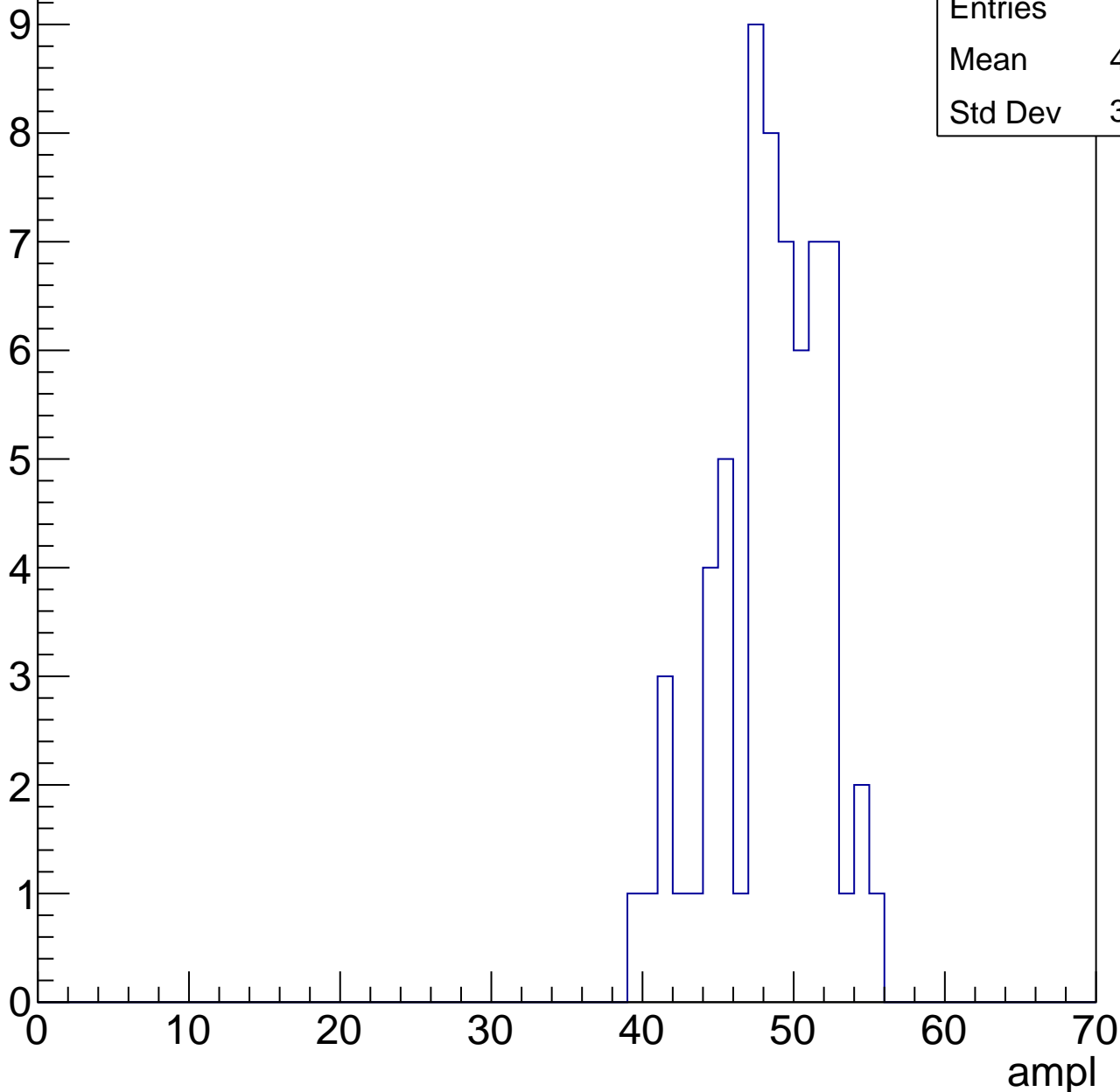


# B1L103S, U3-ch65, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	48.02
Std Dev	3.567

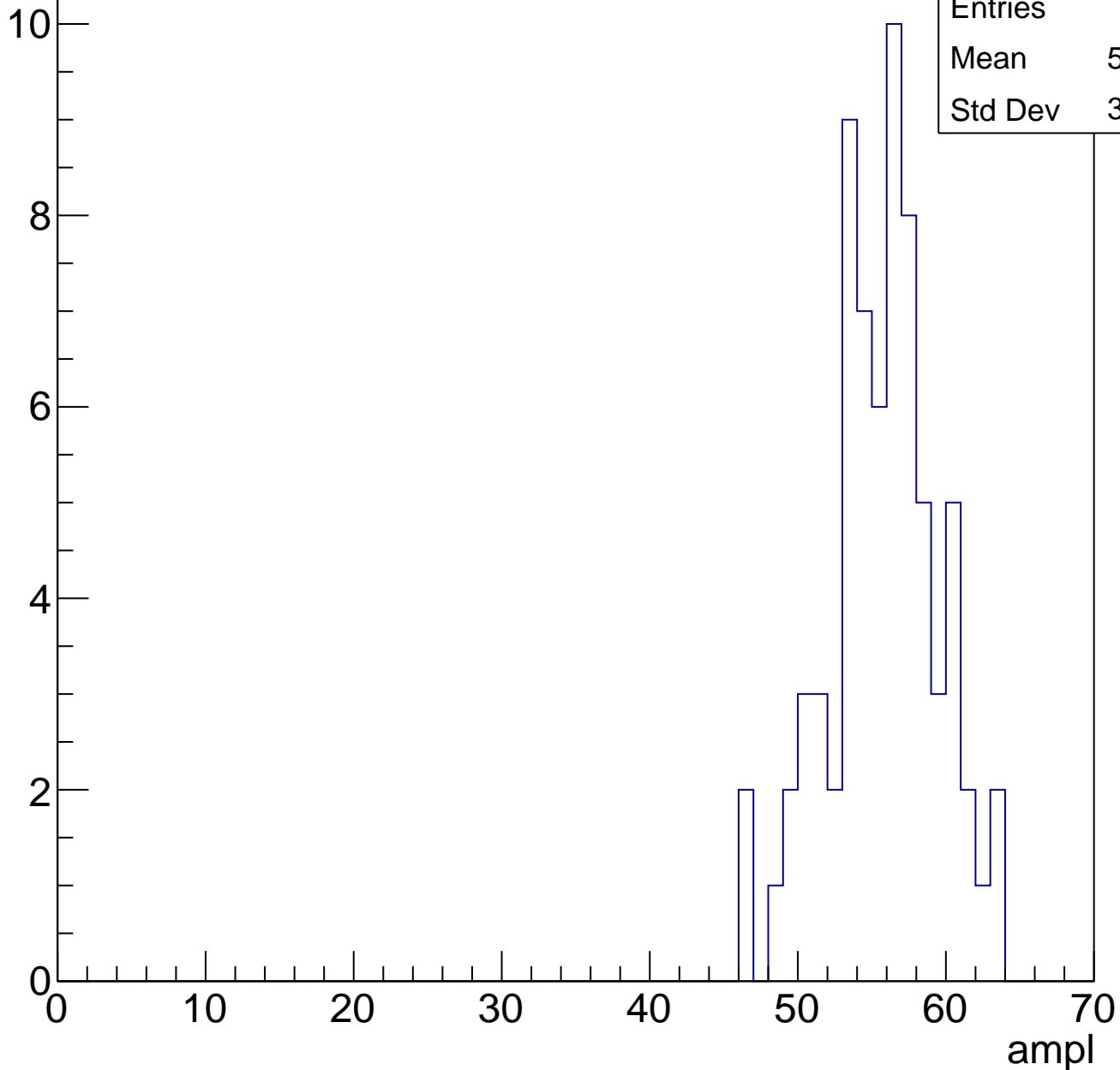


# B1L103S, U3-ch65, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	71
Mean	55.25
Std Dev	3.699

Entry

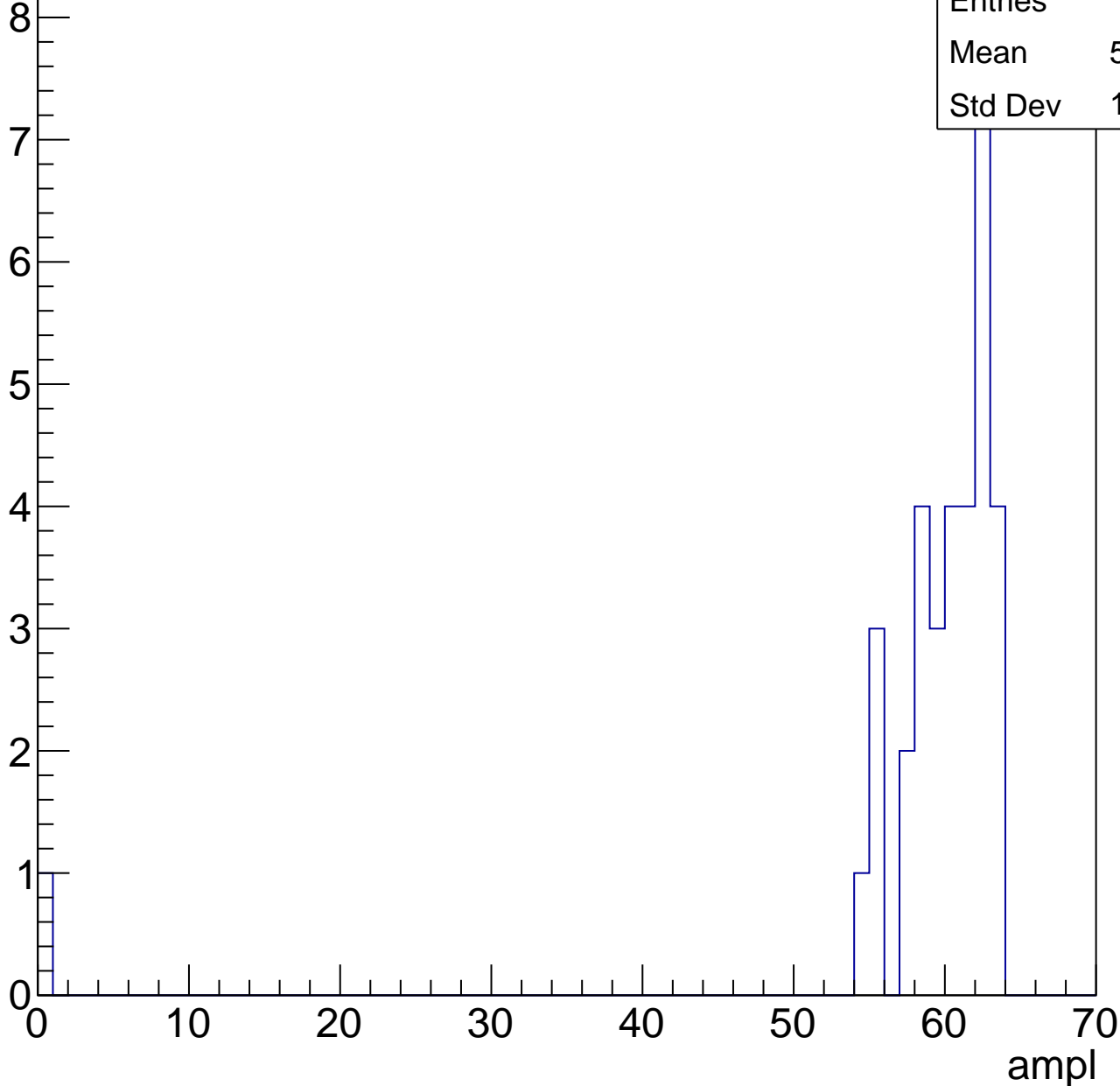


# B1L103S, U3-ch65, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

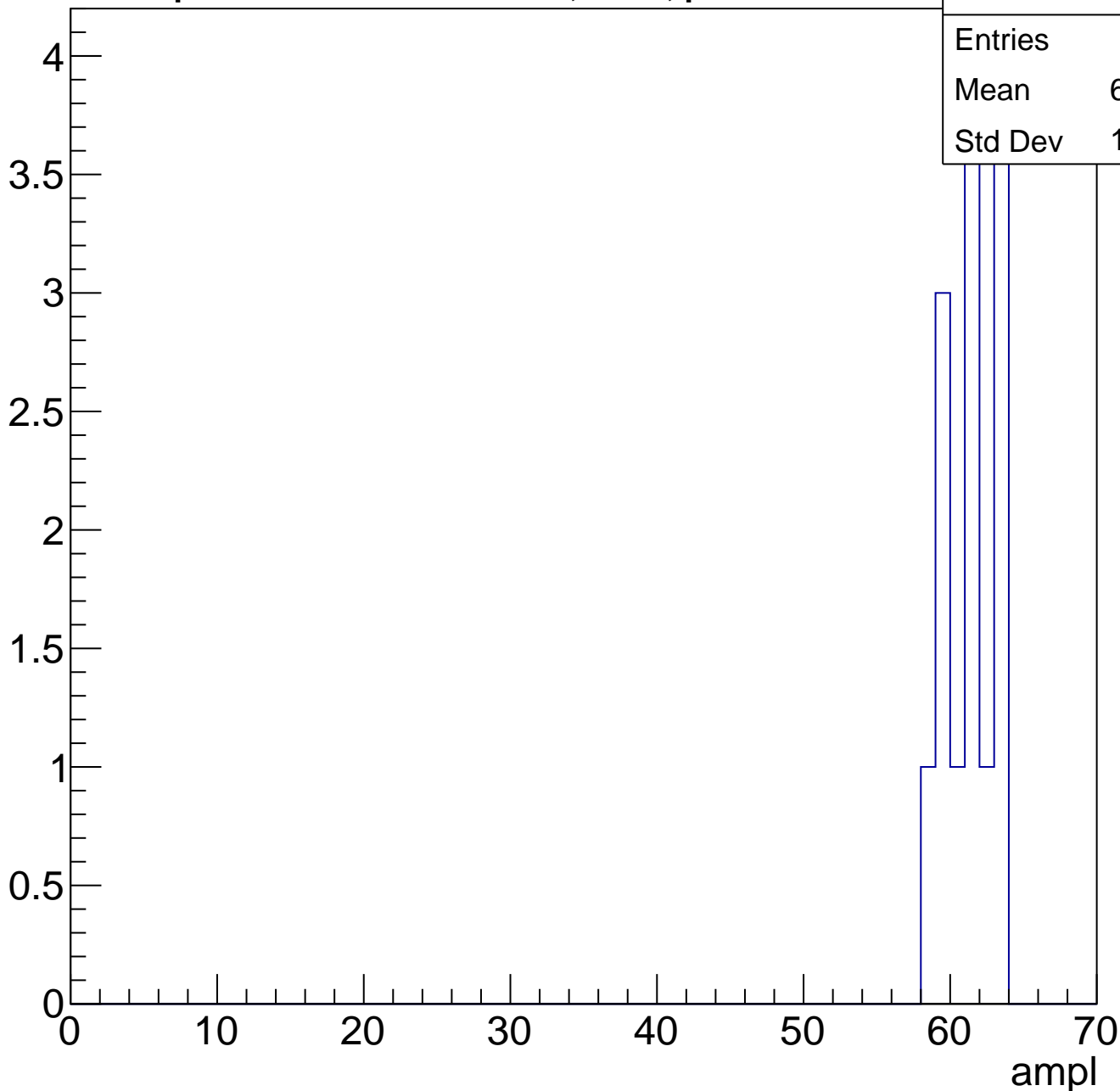
Entries	34
Mean	58.06
Std Dev	10.42



# B1L103S, U3-ch65, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



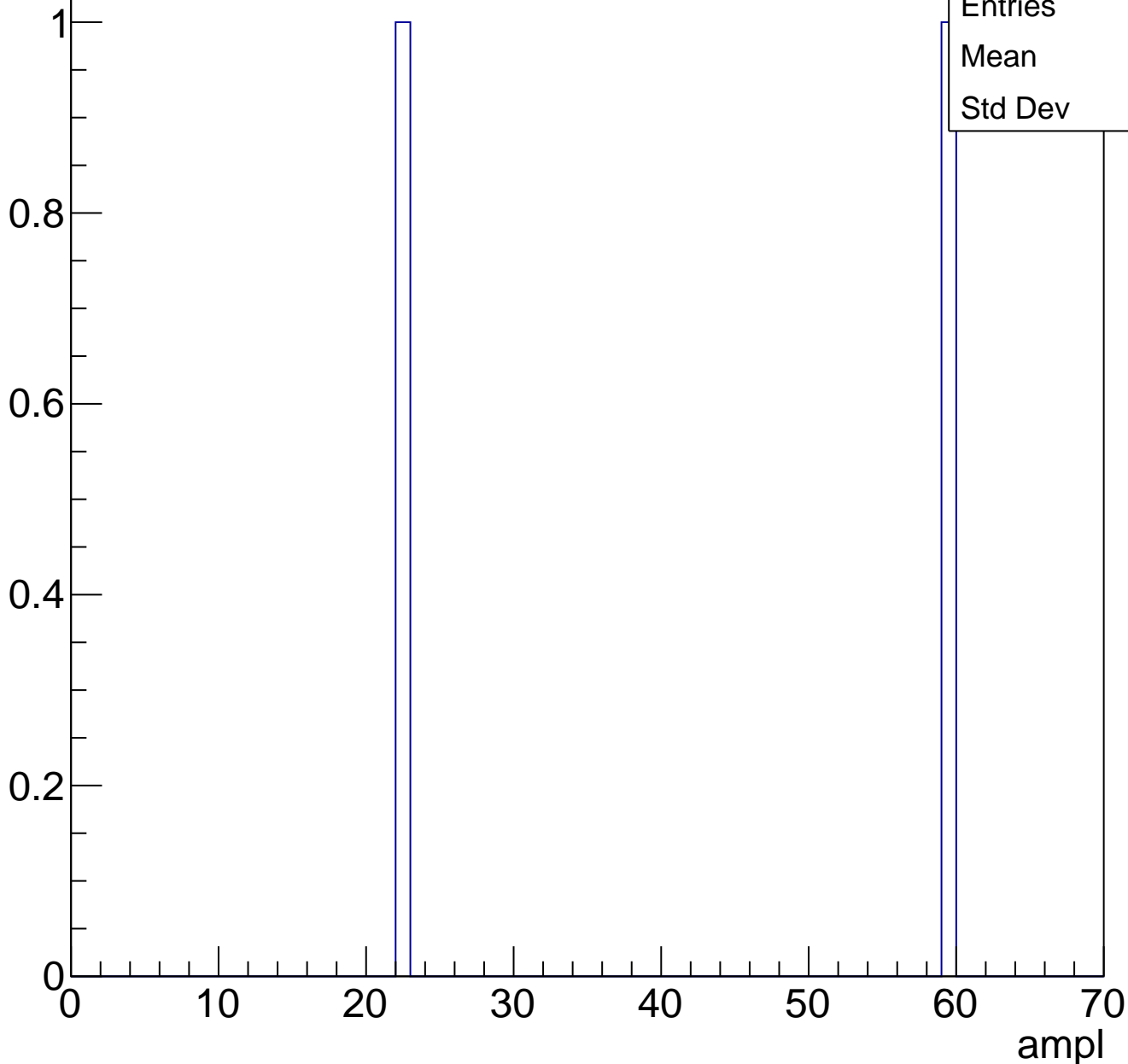
Entries	14
Mean	60.93
Std Dev	1.668



# B1L103S, U3-ch65, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch66, adc0

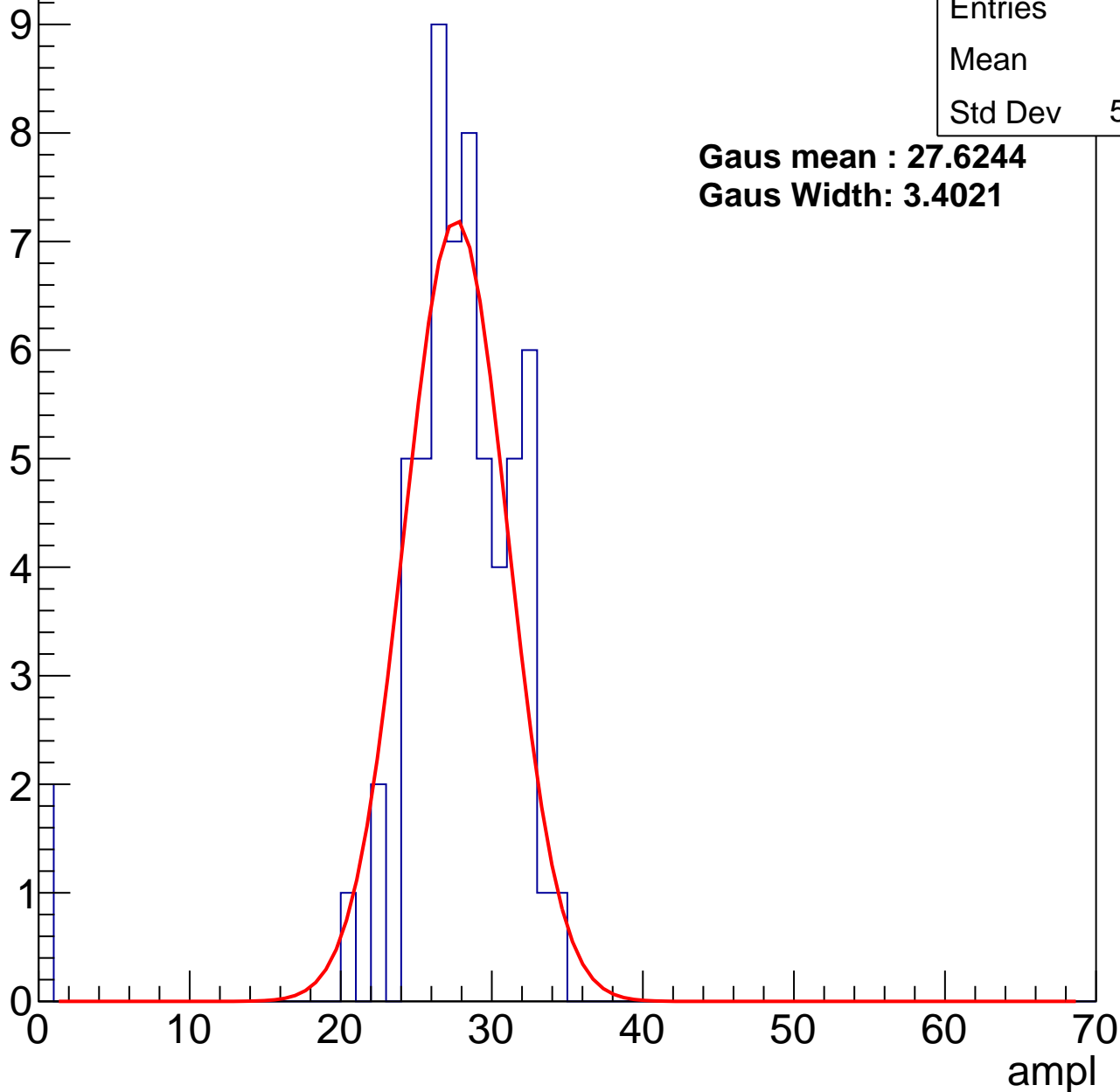
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	26.8
Std Dev	5.737

**Gaus mean : 27.6244**

**Gaus Width: 3.4021**



# B1L103S, U3-ch66, adc1

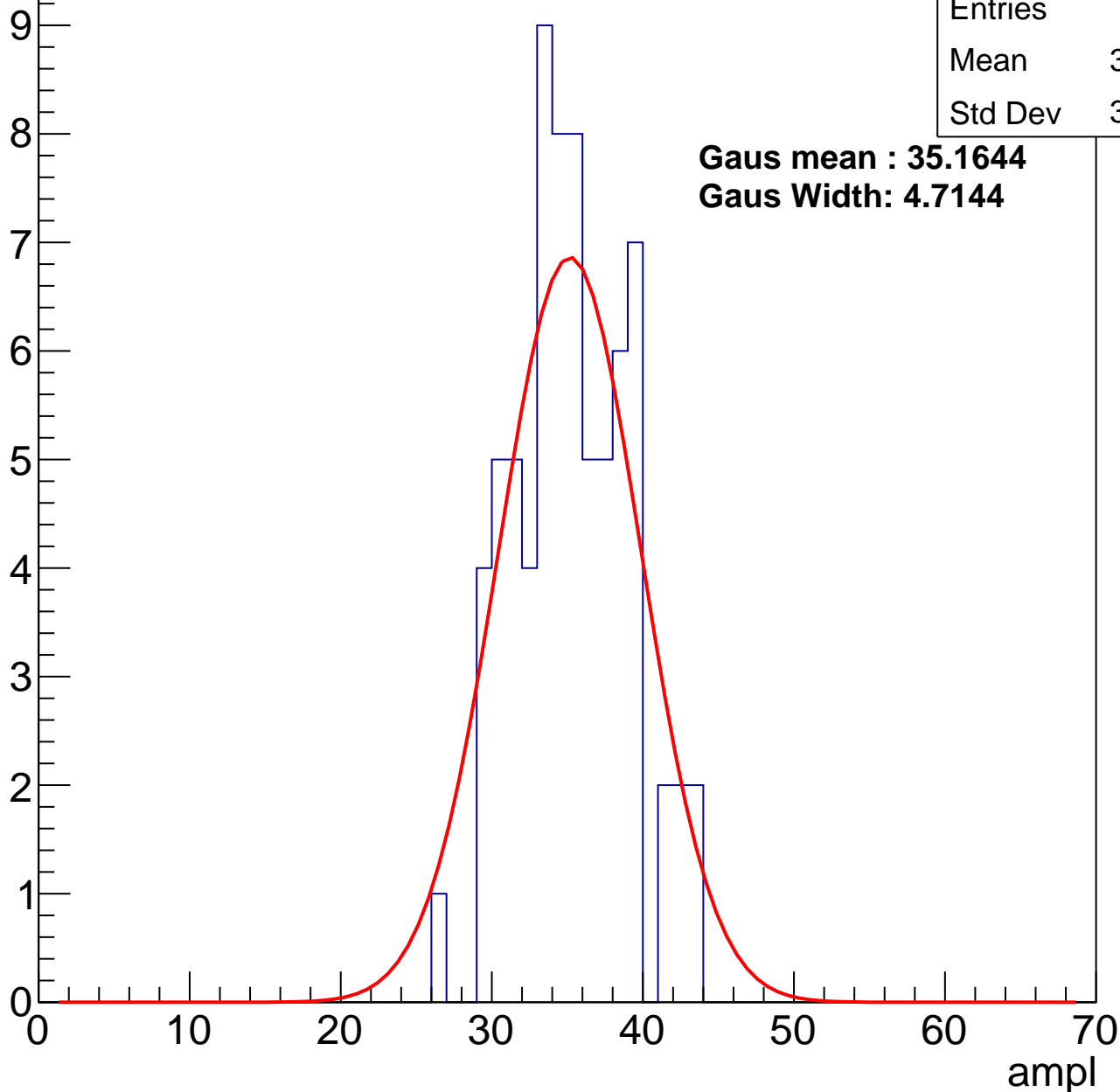
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	34.82
Std Dev	3.695

**Gaus mean : 35.1644**

**Gaus Width: 4.7144**



# B1L103S, U3-ch66, adc2

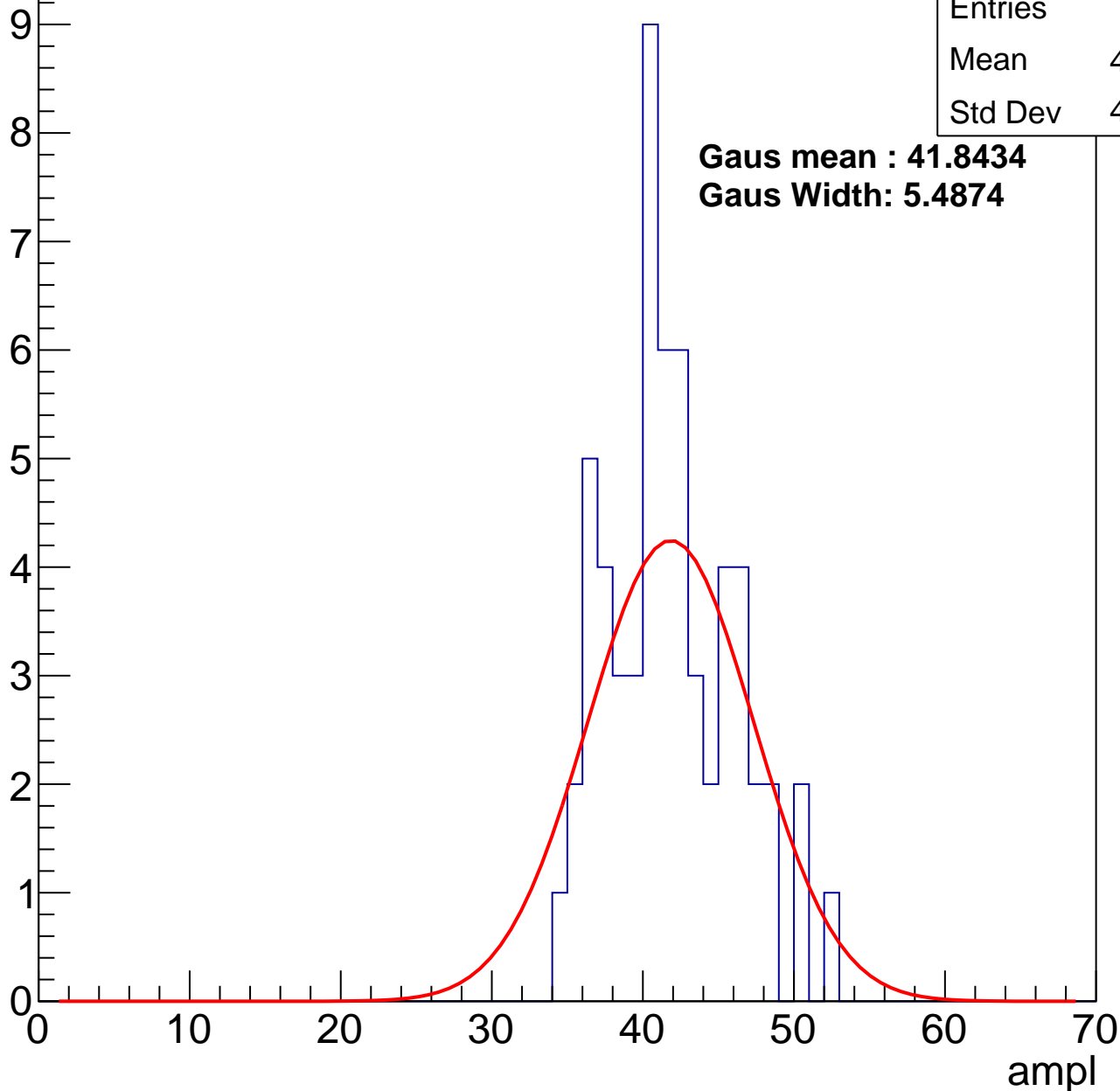
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	41.42
Std Dev	4.118

**Gaus mean : 41.8434**

**Gaus Width: 5.4874**

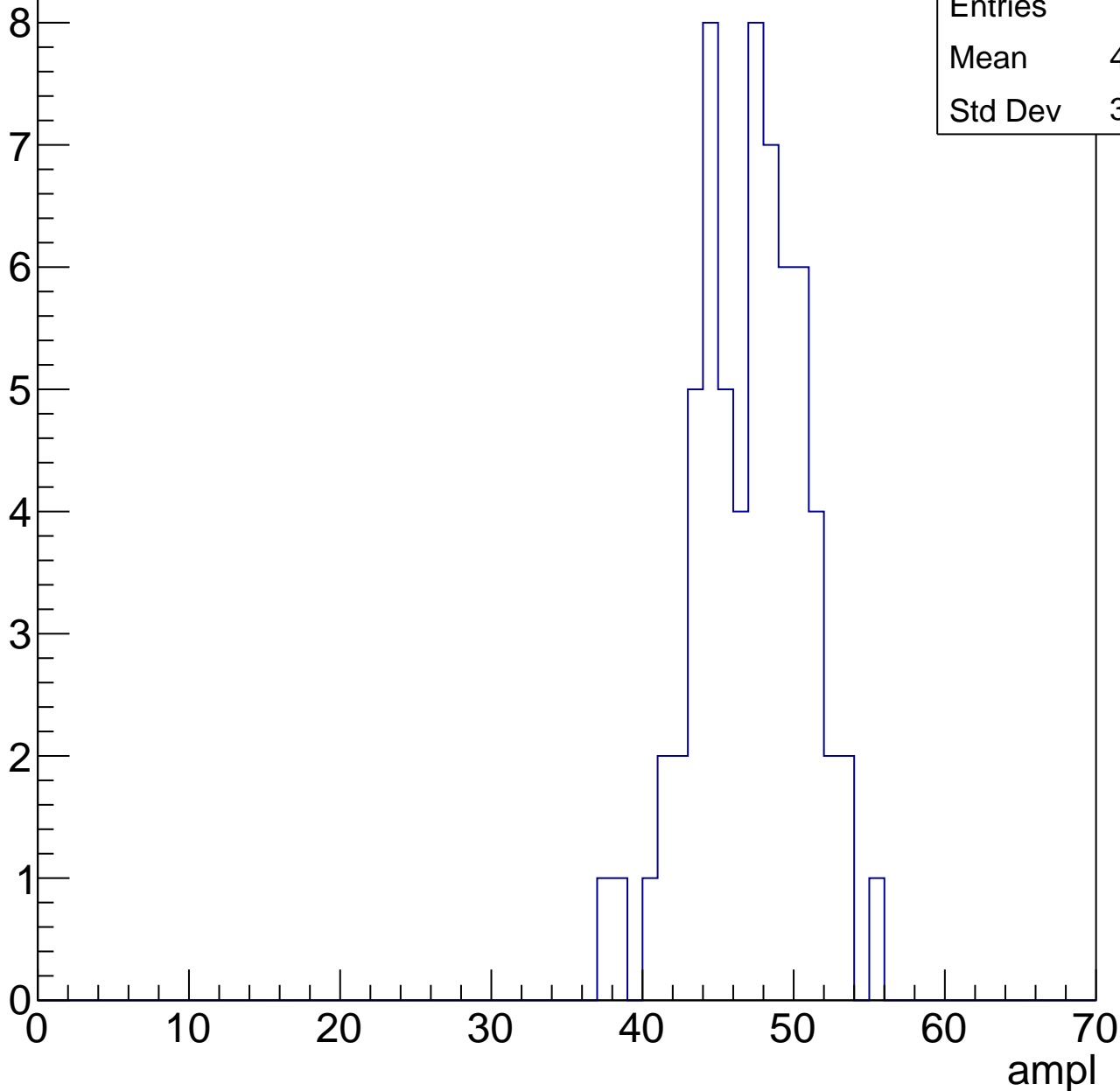


# B1L103S, U3-ch66, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

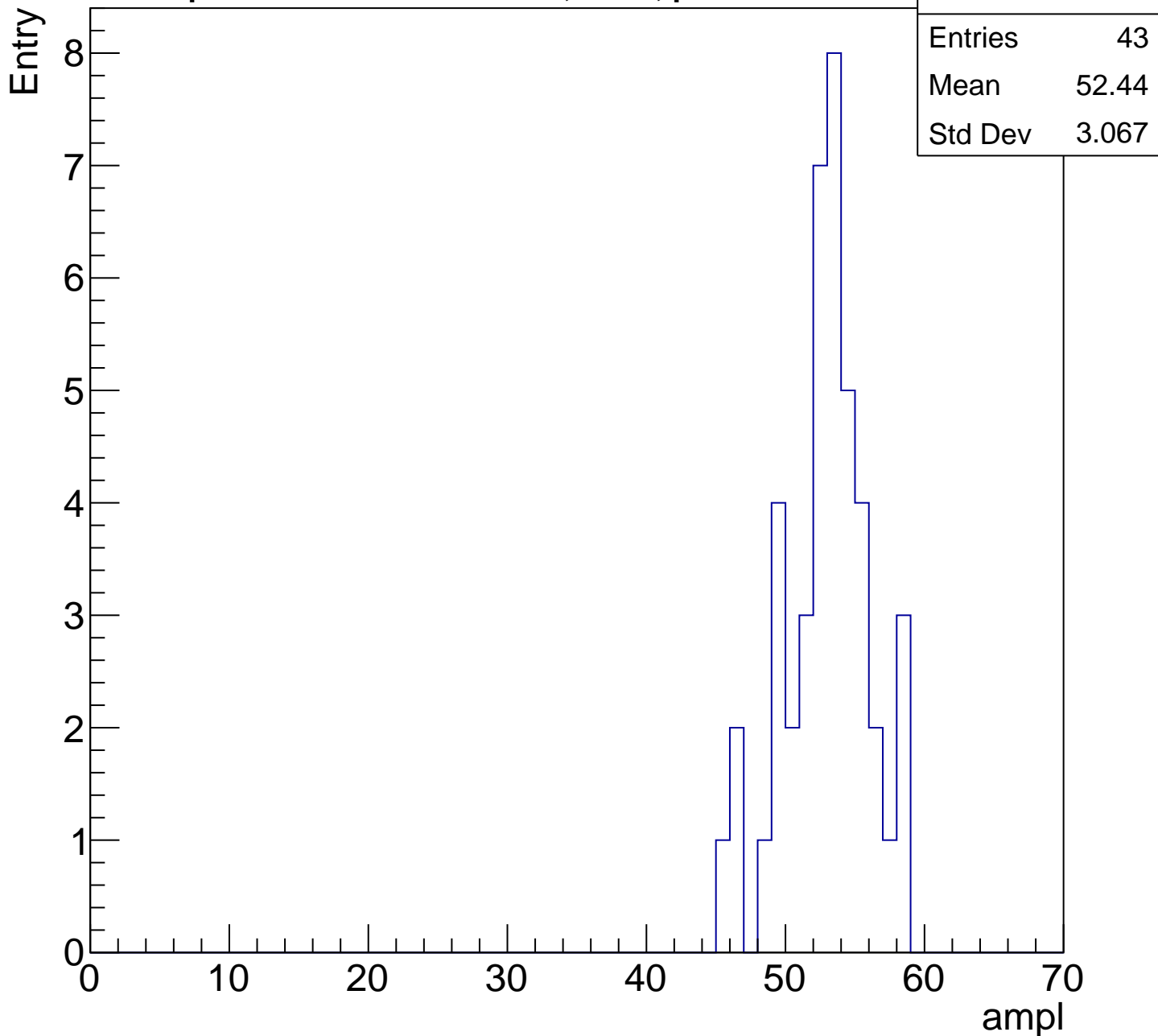
Entry

Entries	65
Mean	46.65
Std Dev	3.627



# B1L103S, U3-ch66, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

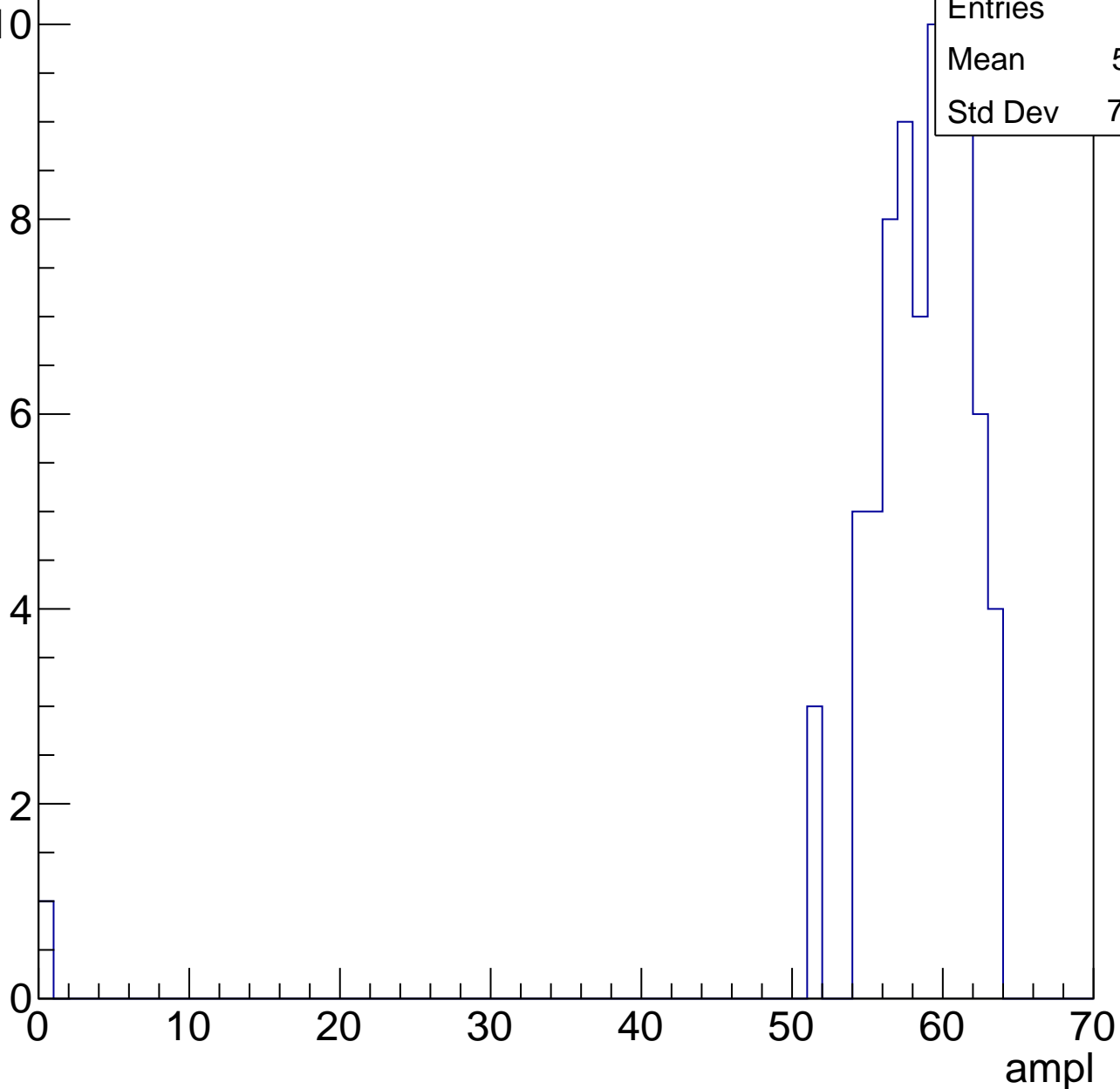


# B1L103S, U3-ch66, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	57.51
Std Dev	7.194

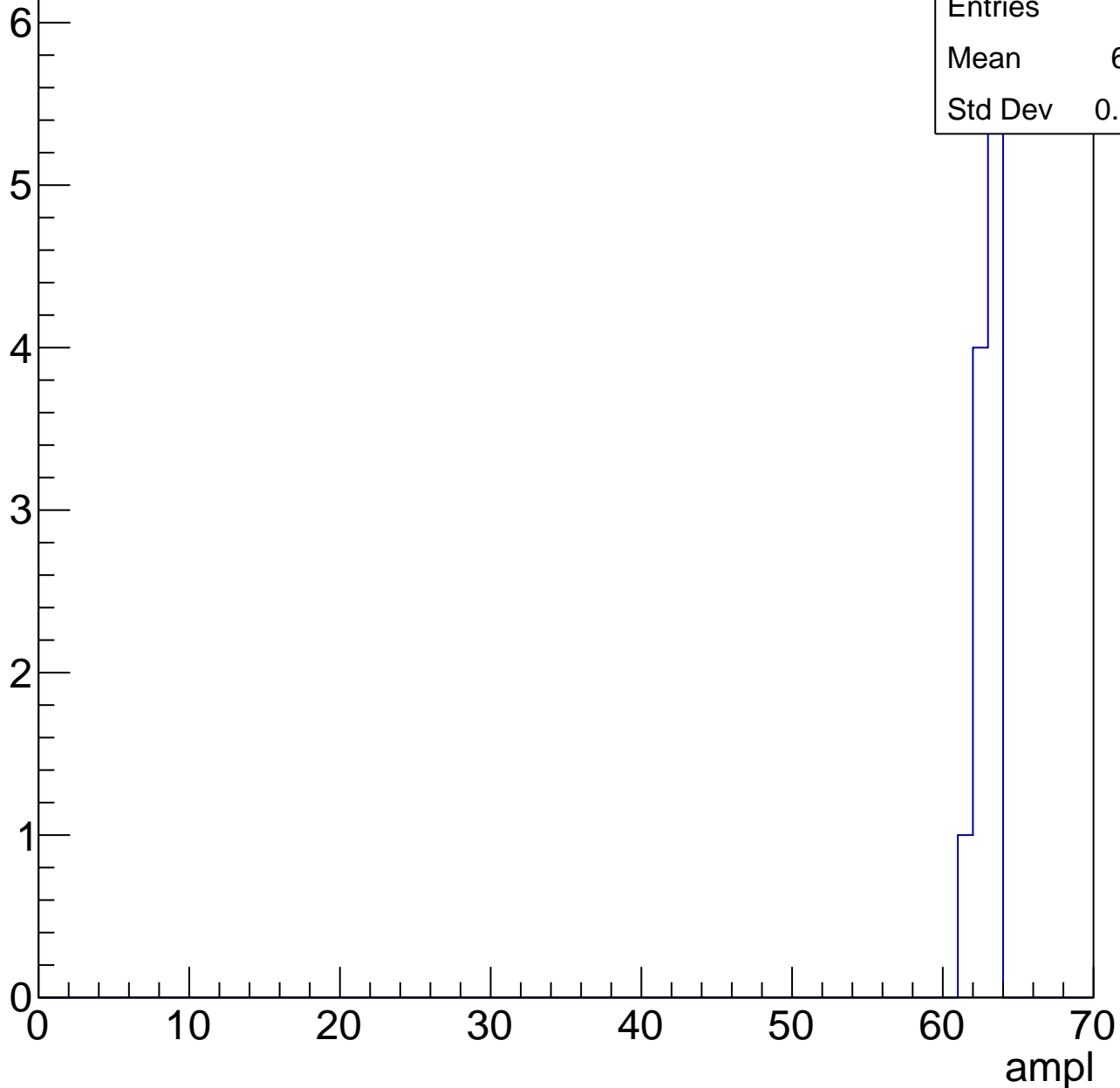


# B1L103S, U3-ch66, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	11
Mean	62.45
Std Dev	0.6556





# B1L103S, U3-ch66, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U3-ch67, adc0

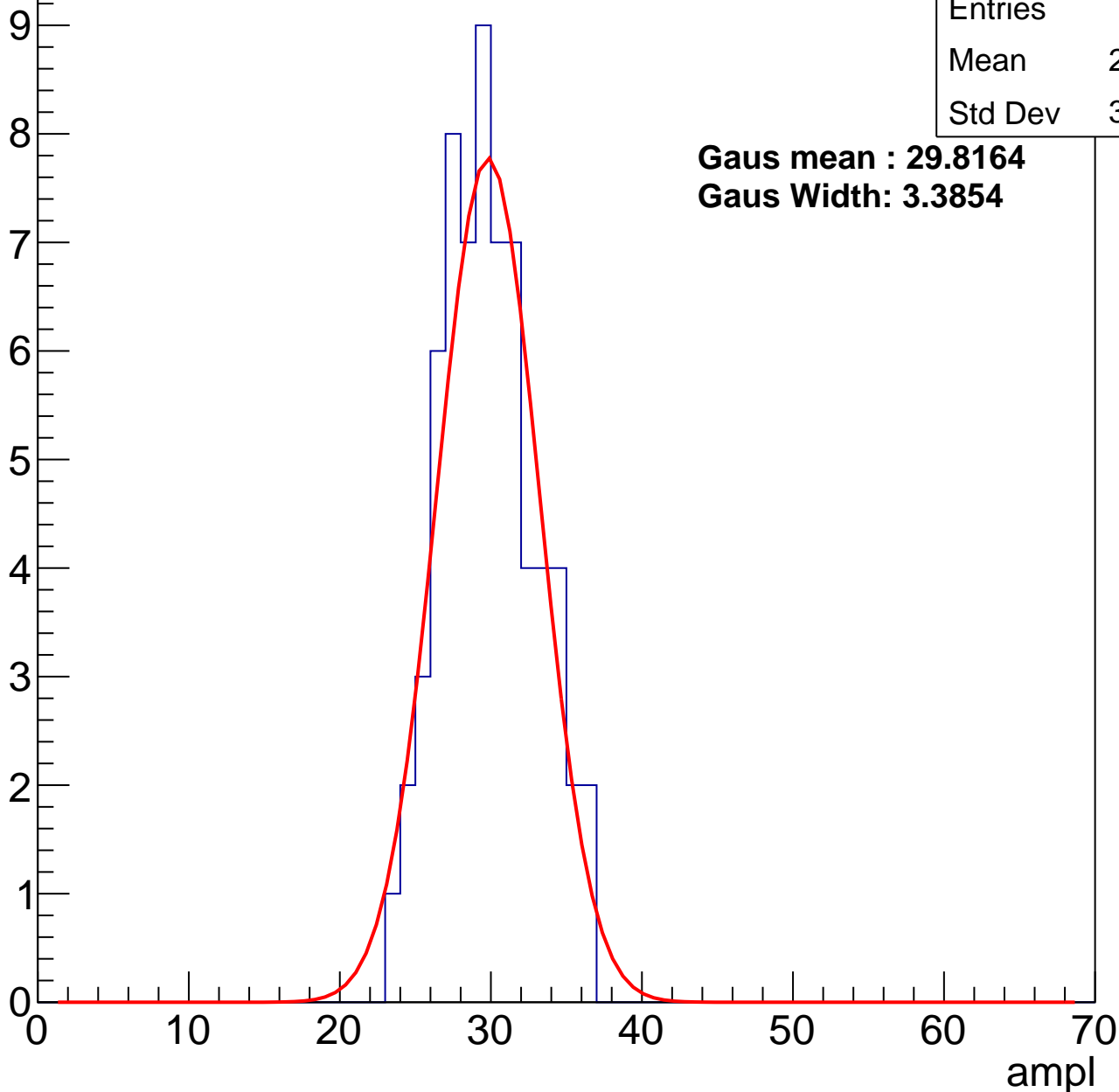
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	29.39
Std Dev	3.069

**Gaus mean : 29.8164**

**Gaus Width: 3.3854**



# B1L103S, U3-ch67, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	81
Mean	36.54
Std Dev	3.735

**Gaus mean : 36.6116**

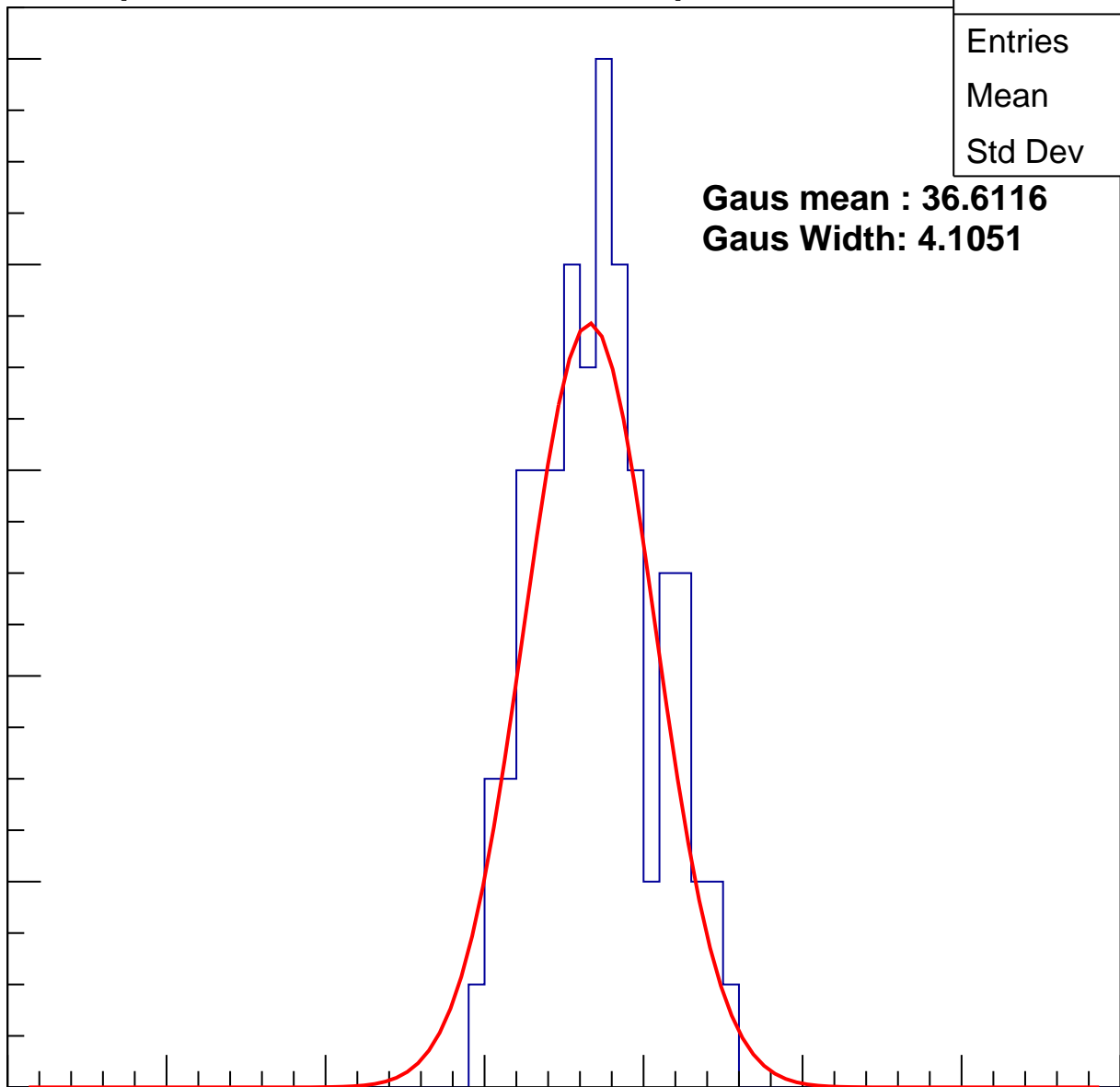
**Gaus Width: 4.1051**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U3-ch67, adc2

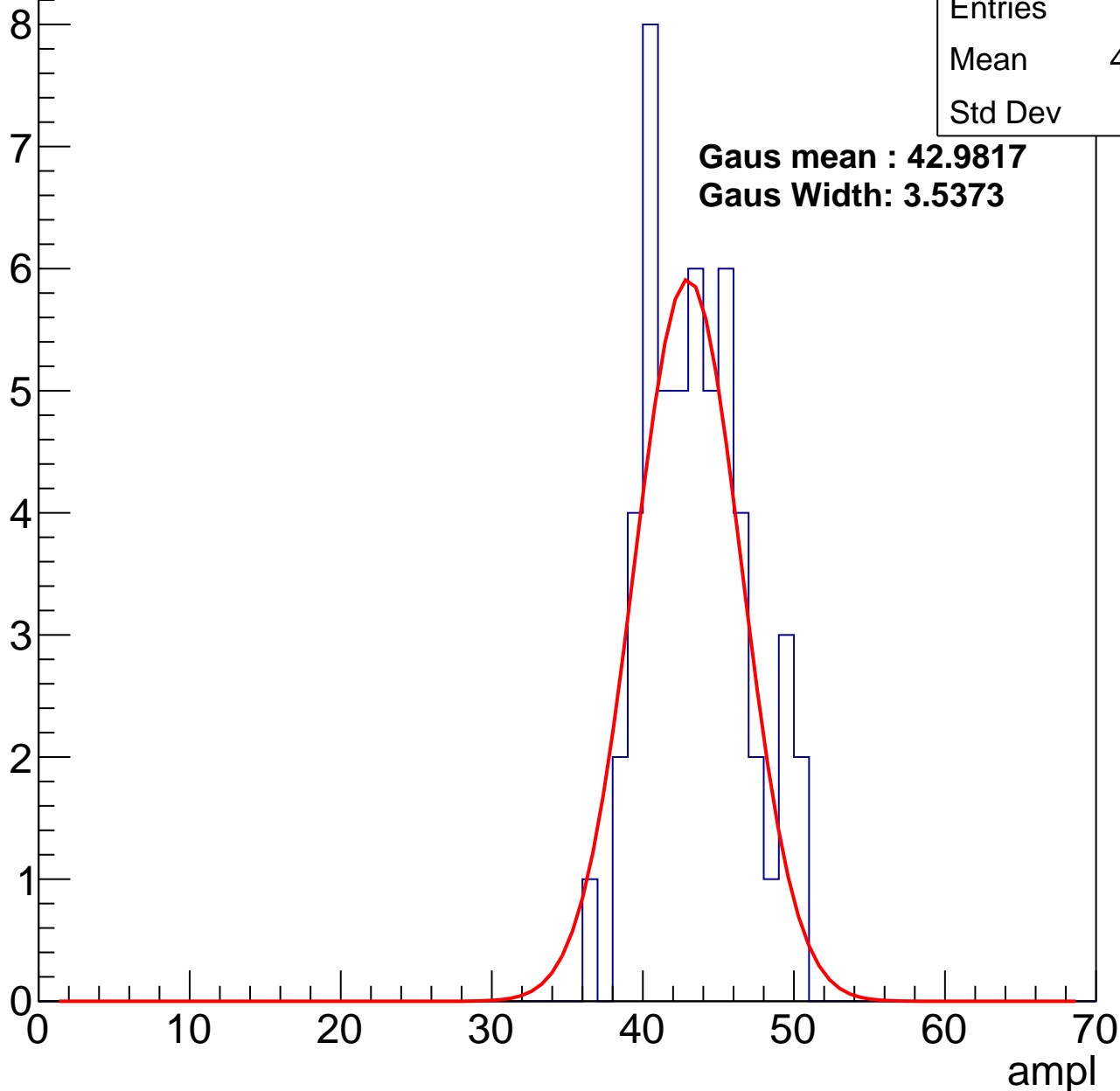
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	43.04
Std Dev	3.3

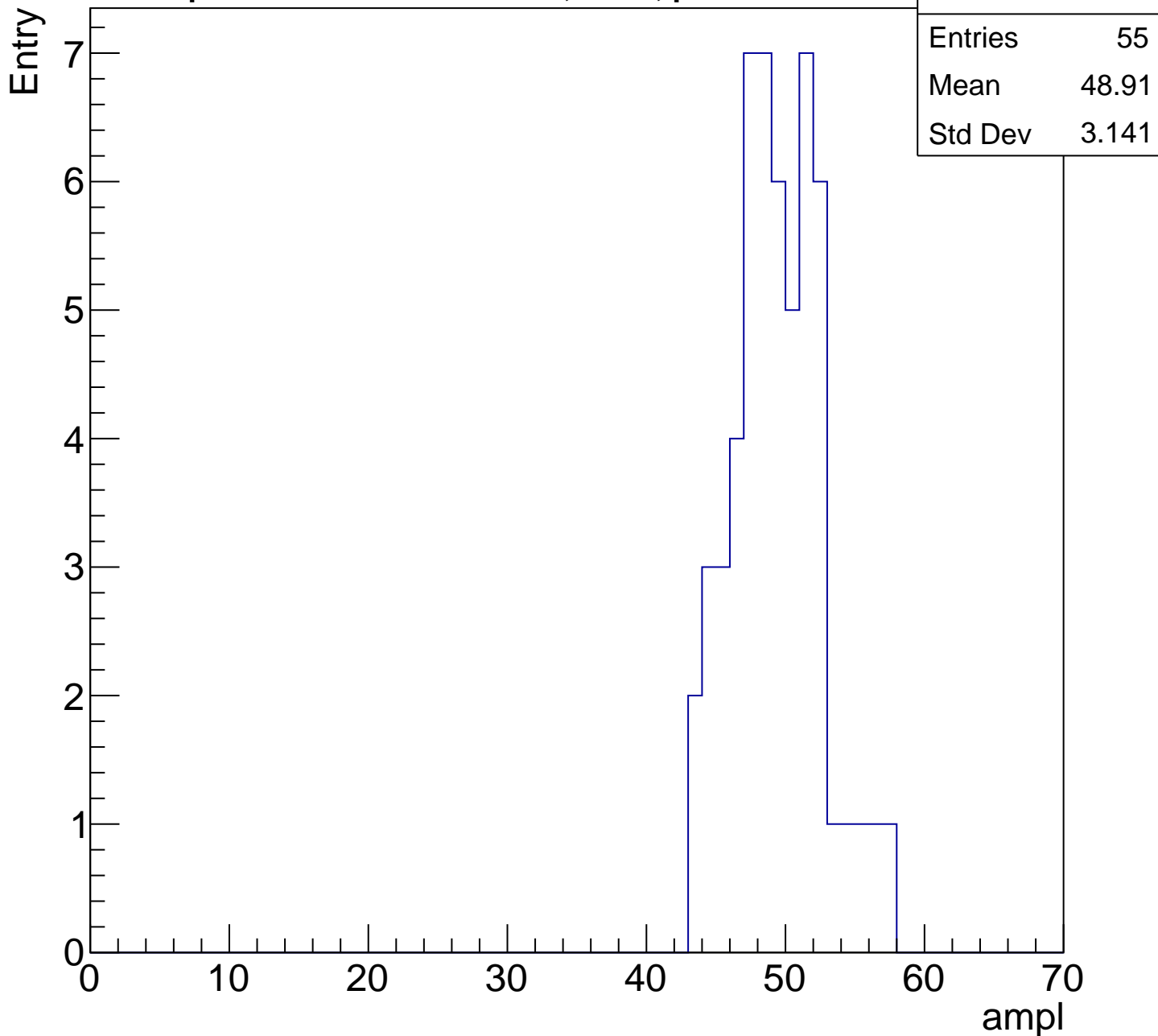
**Gaus mean : 42.9817**

**Gaus Width: 3.5373**



# B1L103S, U3-ch67, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

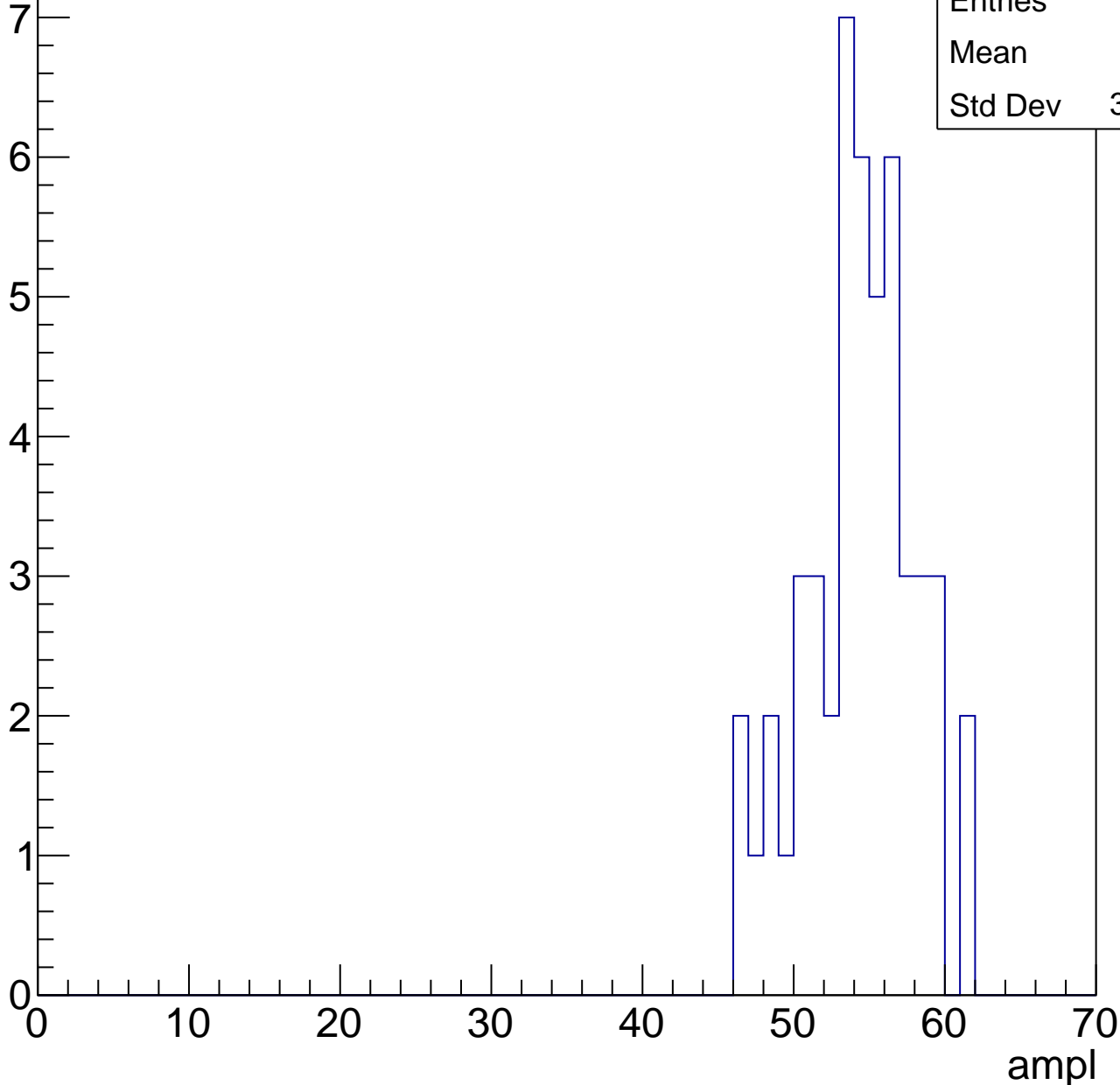


# B1L103S, U3-ch67, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	53.9
Std Dev	3.615



# B1L103S, U3-ch67, adc5

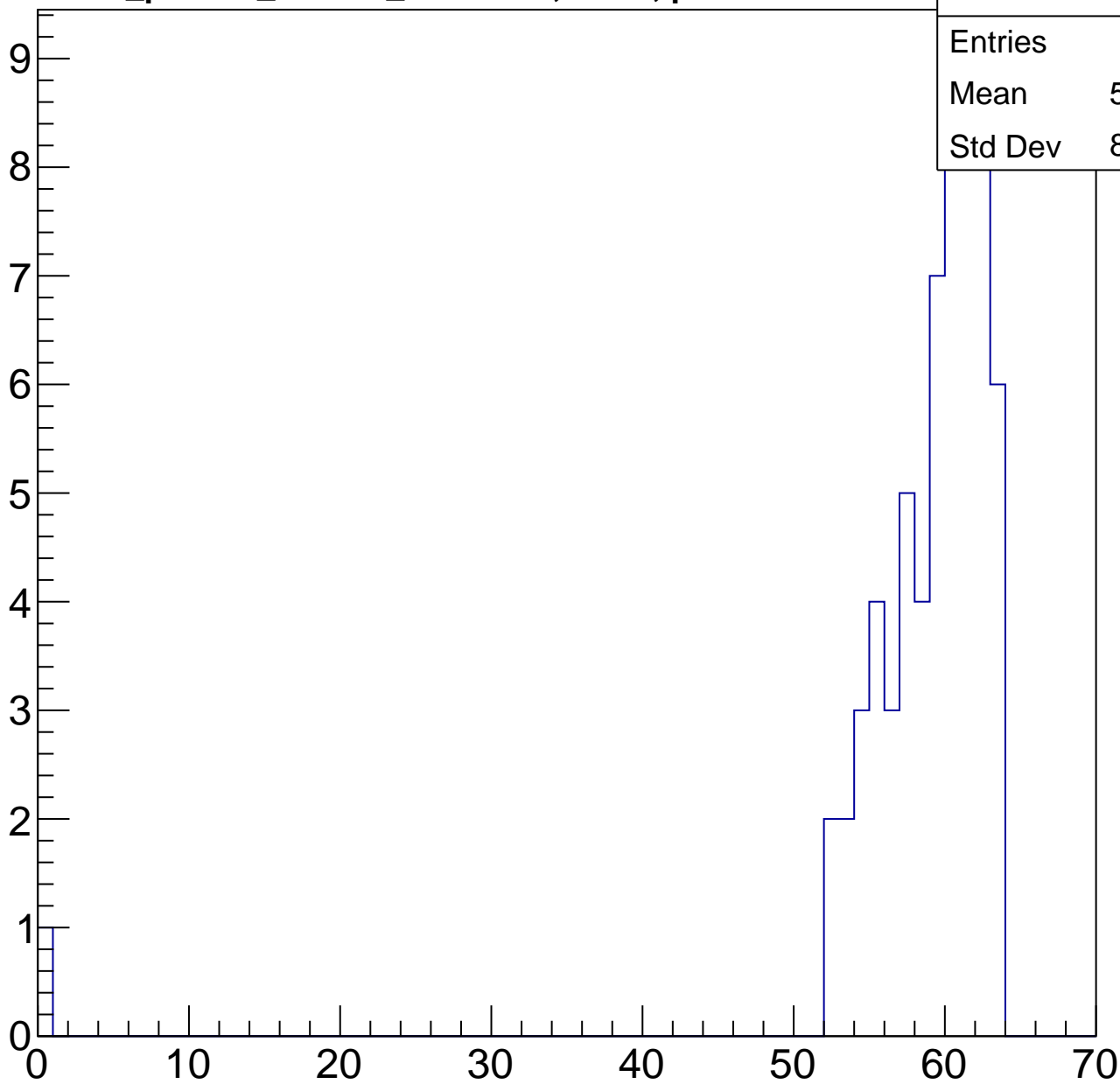
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	62
Mean	57.97
Std Dev	8.024

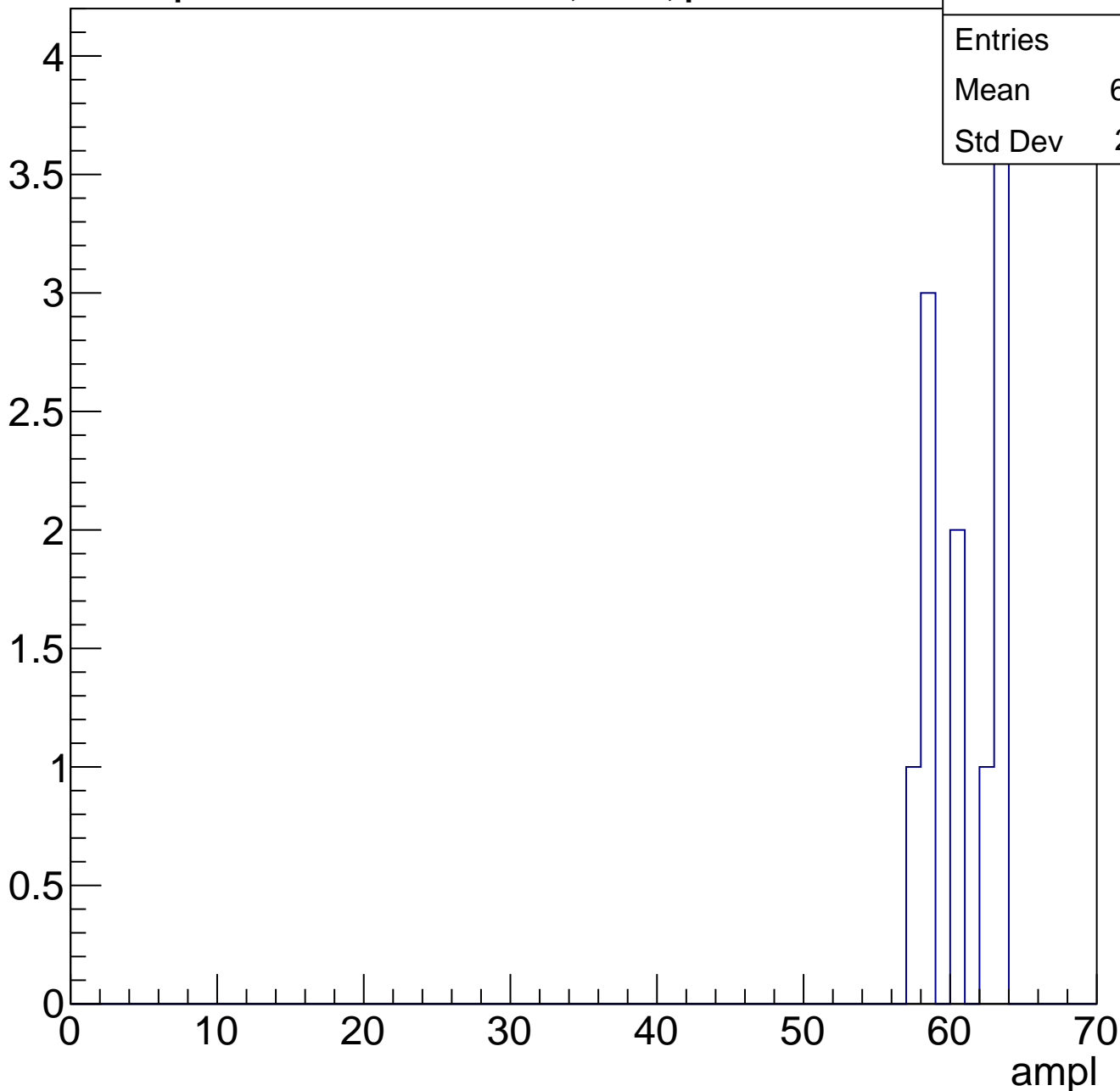
ampl



# B1L103S, U3-ch67, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U3-ch67, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L103S, U3-ch68, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	92
Mean	26.88
Std Dev	5.626

**Gaus mean : 28.0808**

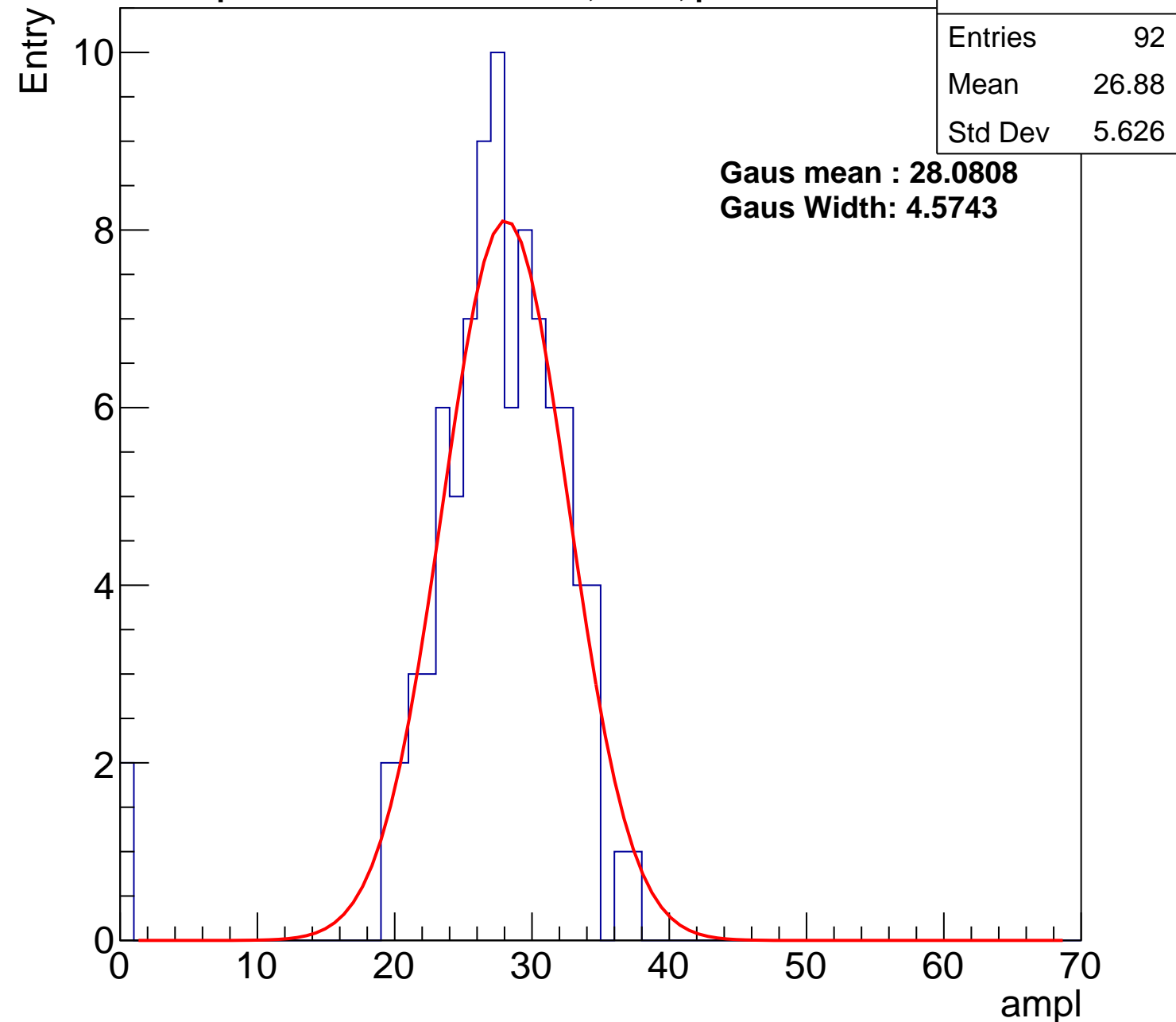
**Gaus Width: 4.5743**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U3-ch68, adc1

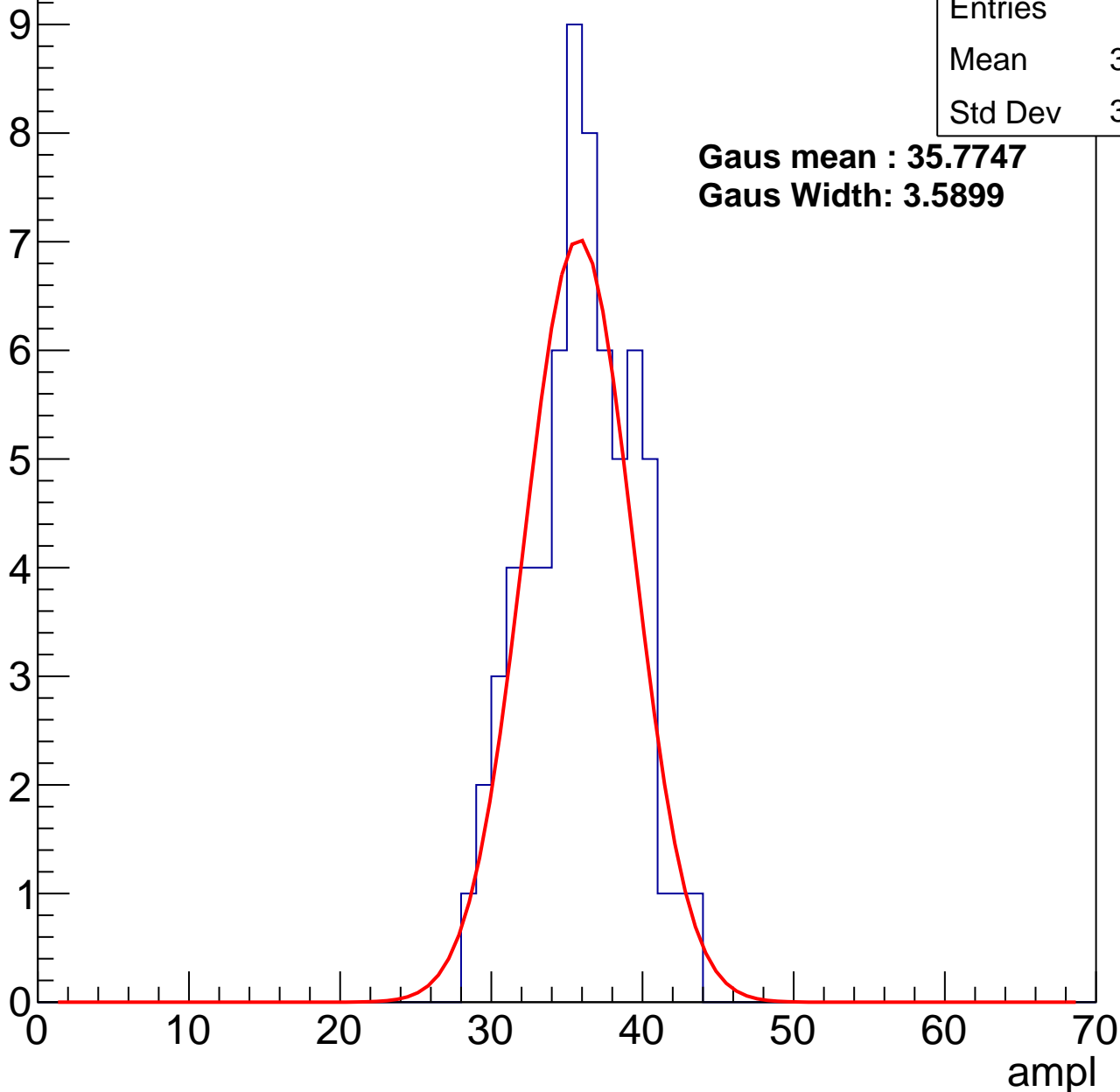
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	35.44
Std Dev	3.376

**Gaus mean : 35.7747**

**Gaus Width: 3.5899**



# B1L103S, U3-ch68, adc2

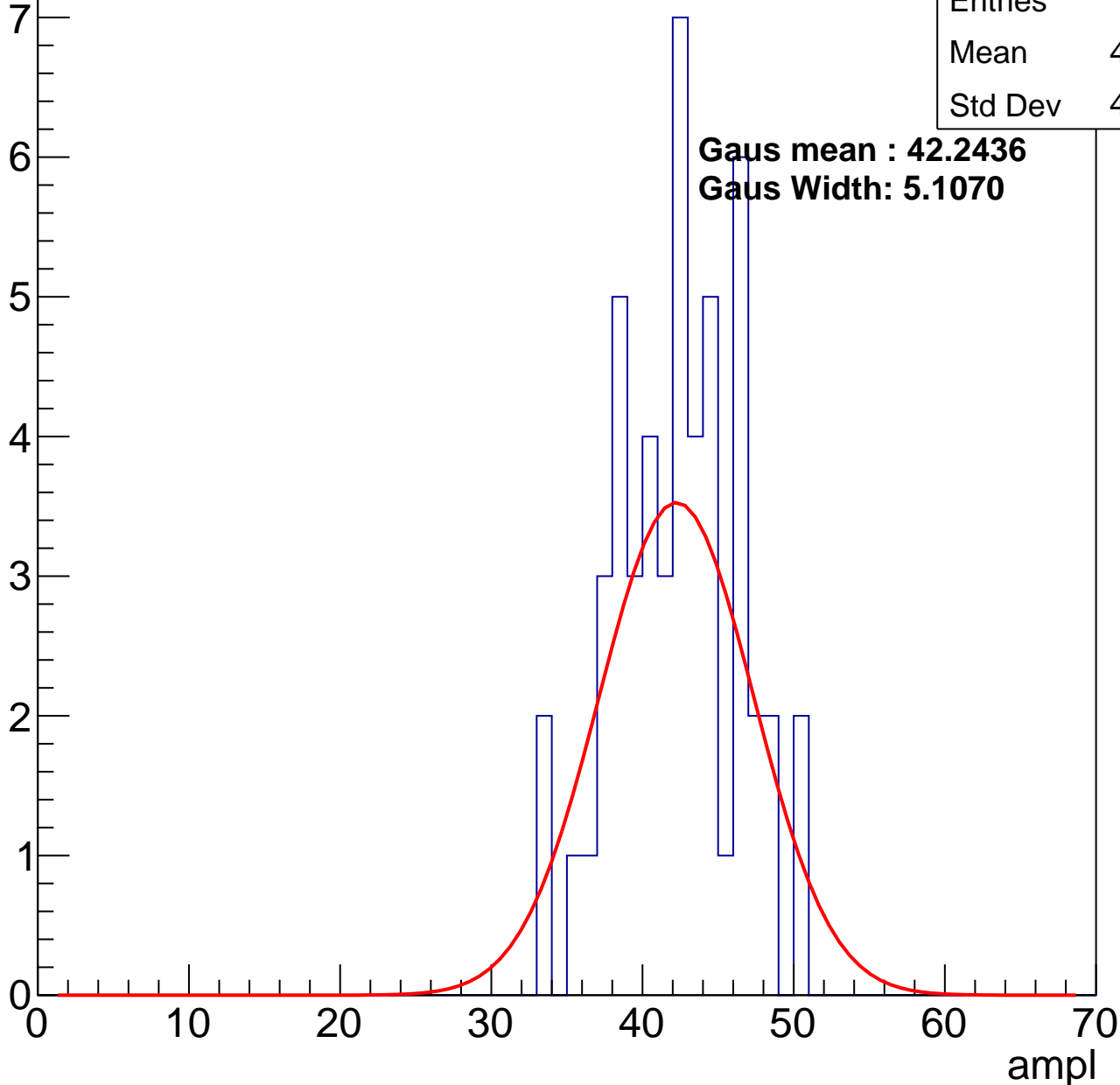
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	41.86
Std Dev	4.025

**Gaus mean : 42.2436**

**Gaus Width: 5.1070**

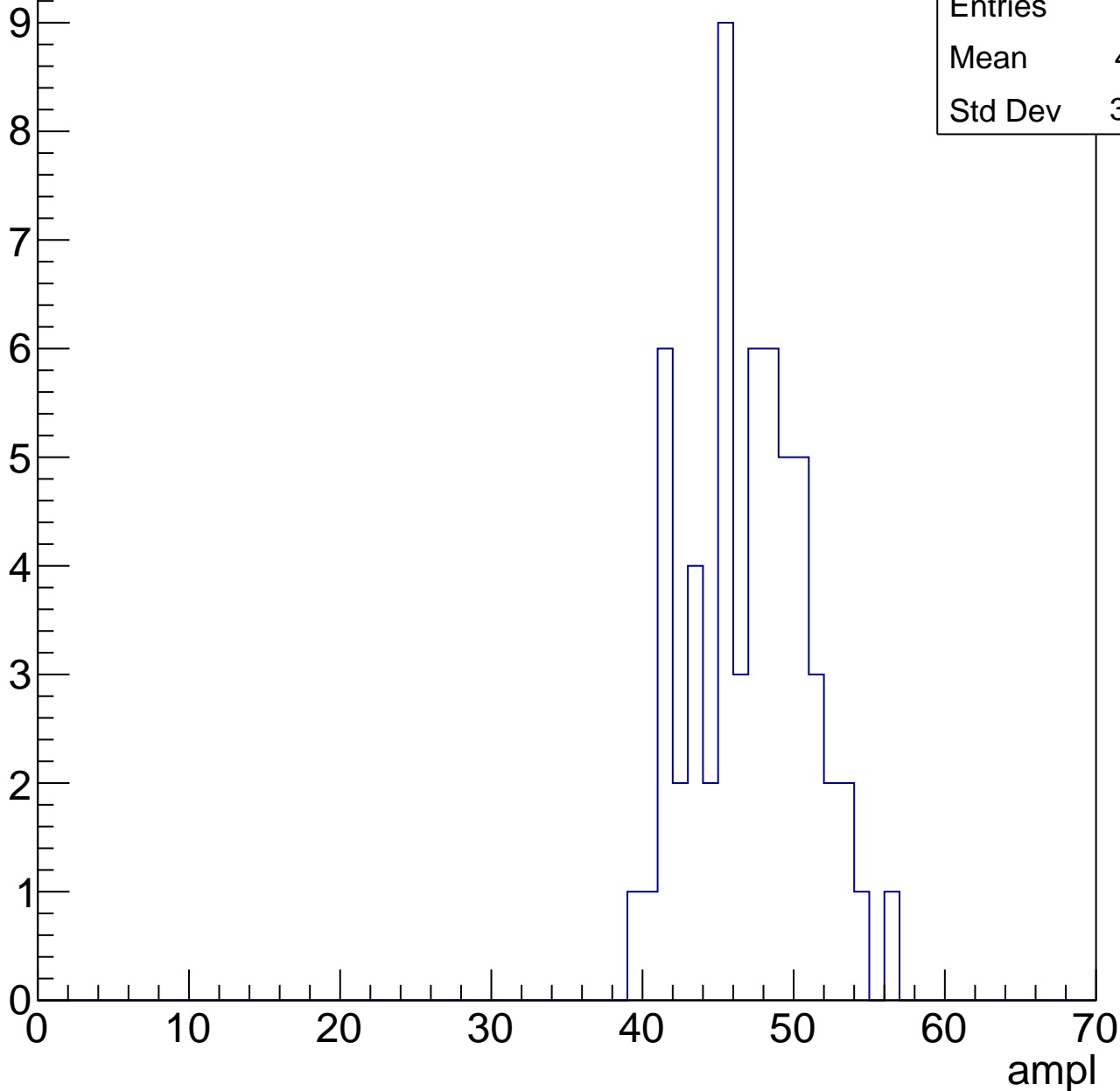


# B1L103S, U3-ch68, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

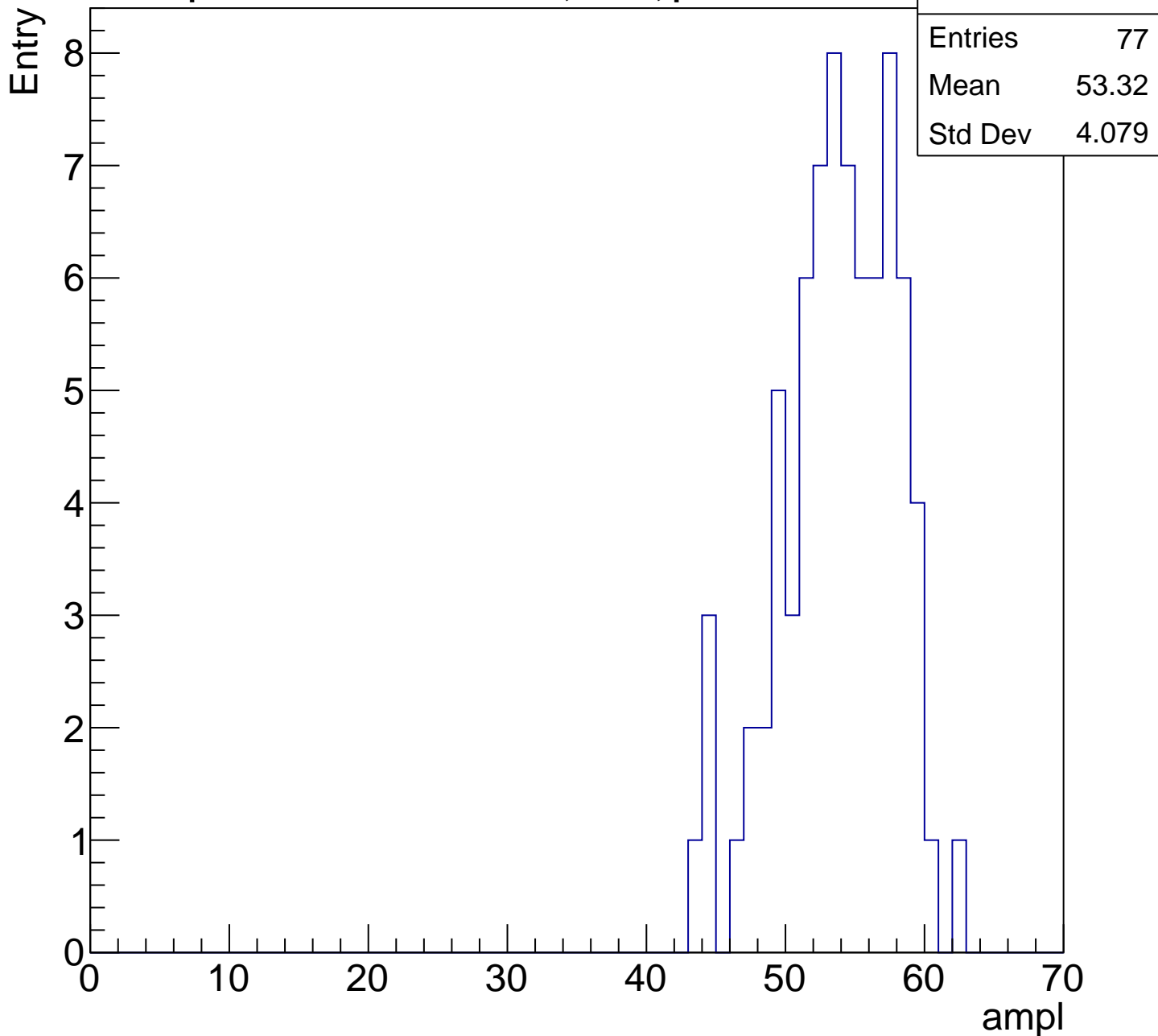
Entry

Entries	59
Mean	46.61
Std Dev	3.822



# B1L103S, U3-ch68, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

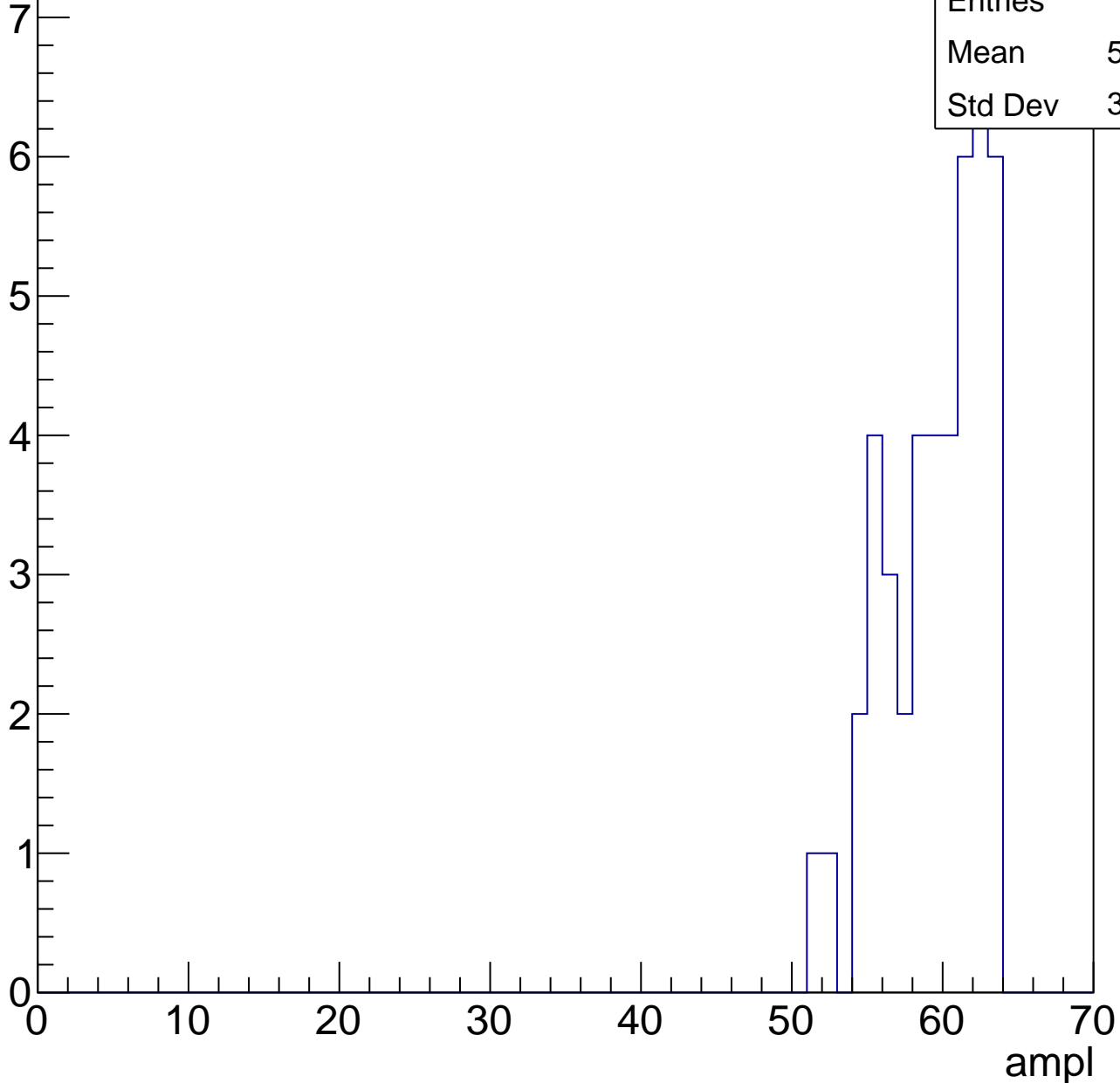


# B1L103S, U3-ch68, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	44
Mean	59.07
Std Dev	3.208

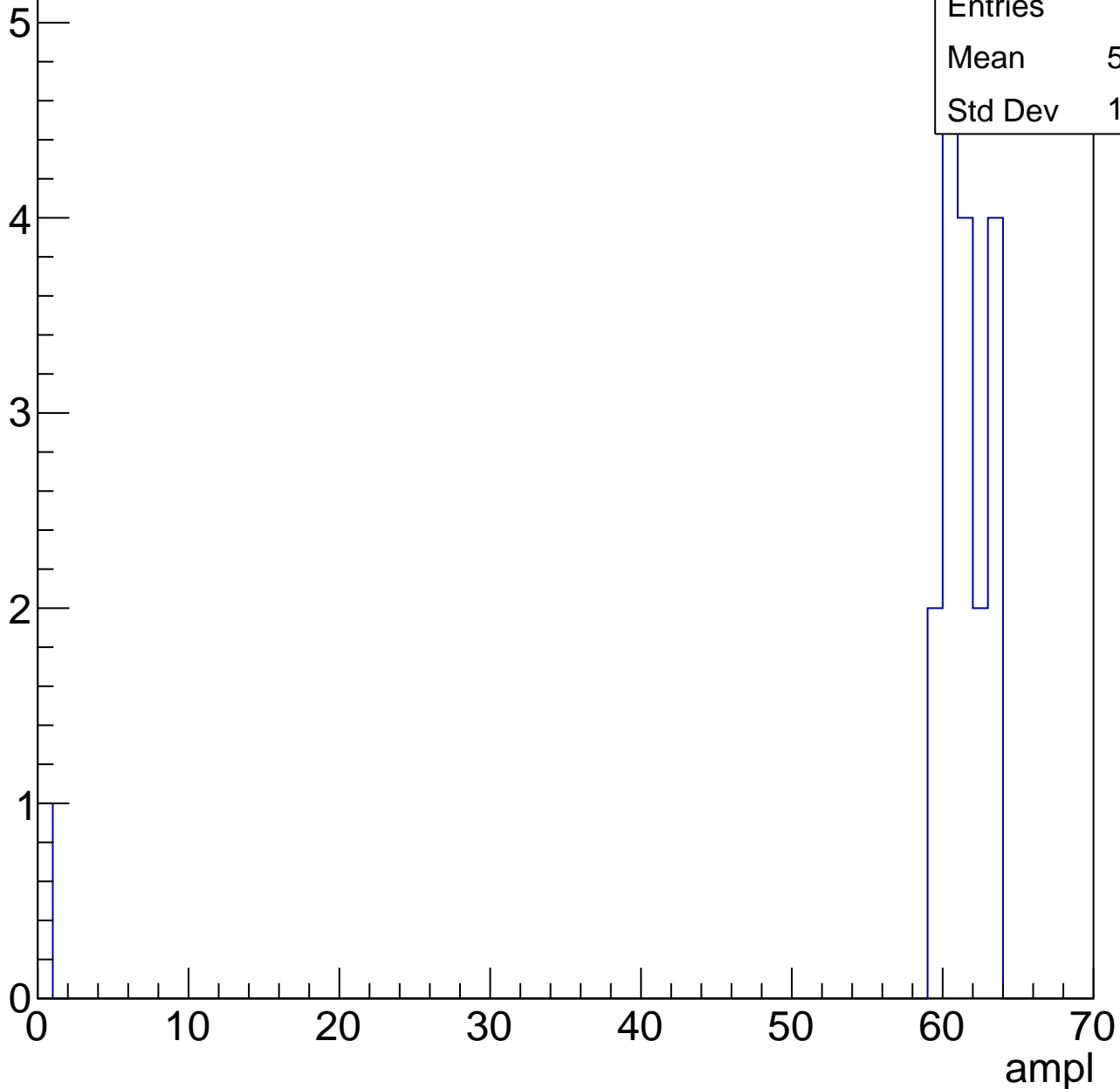


# B1L103S, U3-ch68, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	18
Mean	57.67
Std Dev	14.05





# B1L103S, U3-ch68, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U3-ch69, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	72
Mean	29.29
Std Dev	3.892

**Gaus mean : 29.3554**

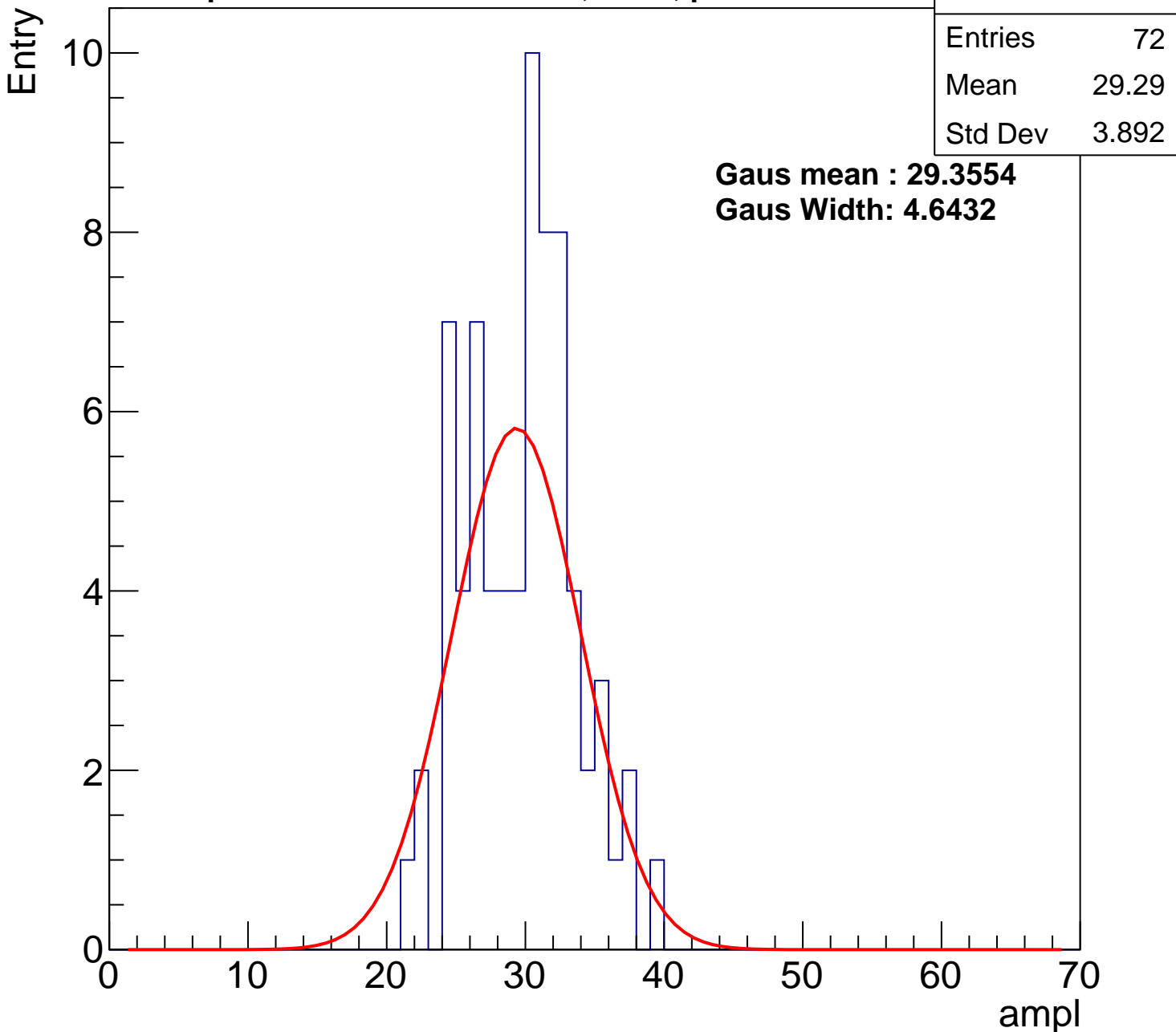
**Gaus Width: 4.6432**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U3-ch69, adc1

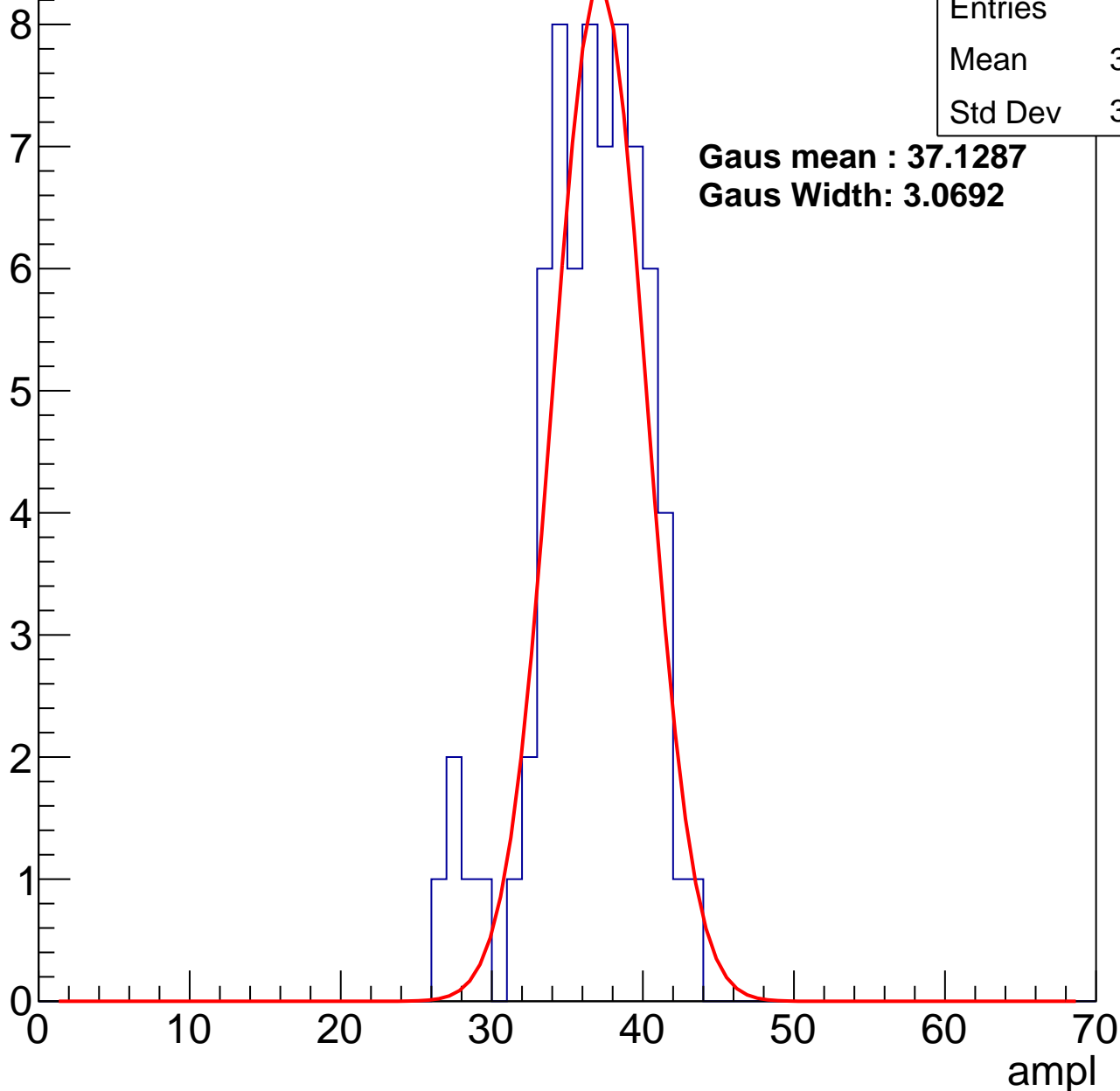
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	36.07
Std Dev	3.599

**Gaus mean : 37.1287**

**Gaus Width: 3.0692**

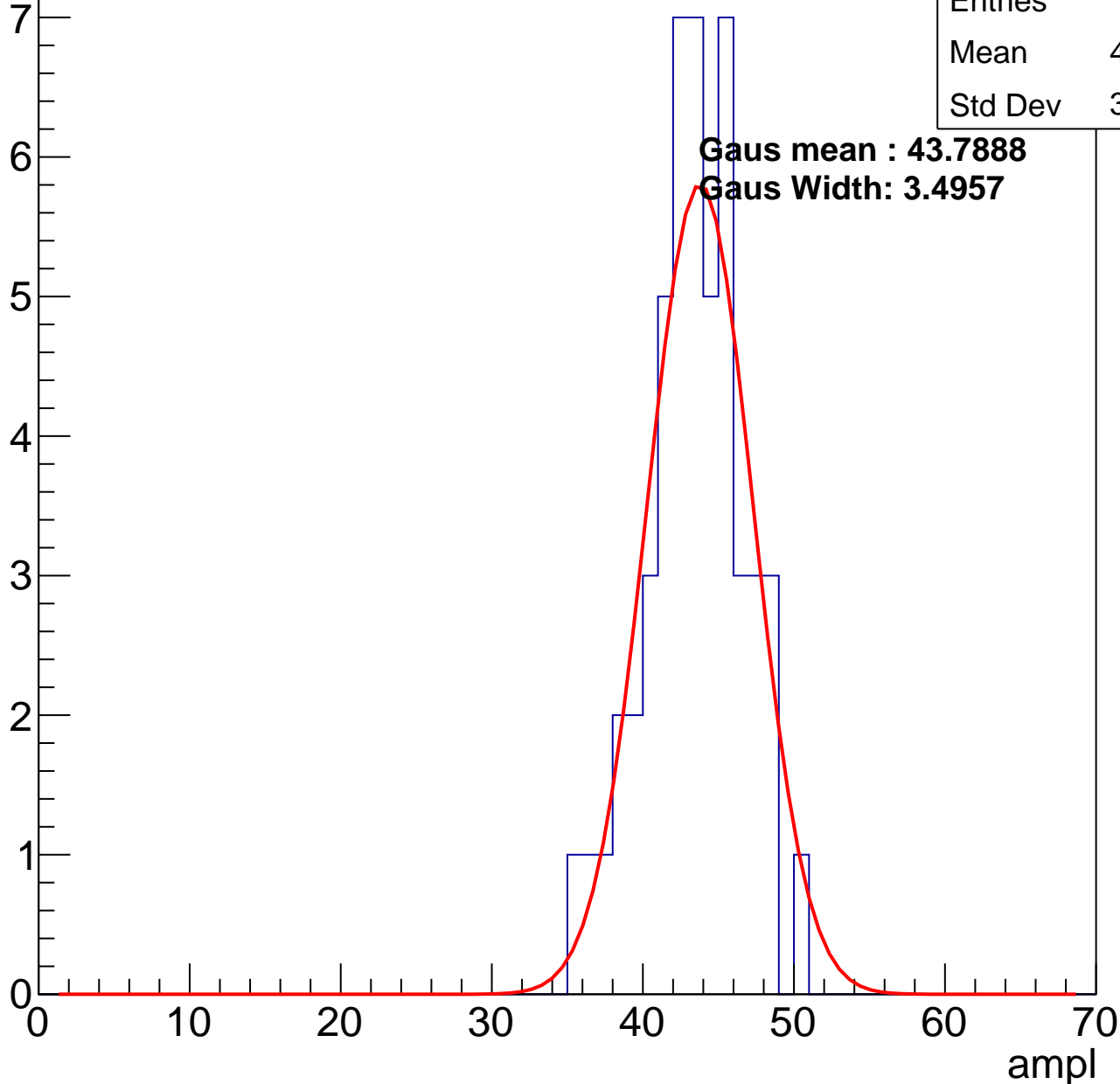


# B1L103S, U3-ch69, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

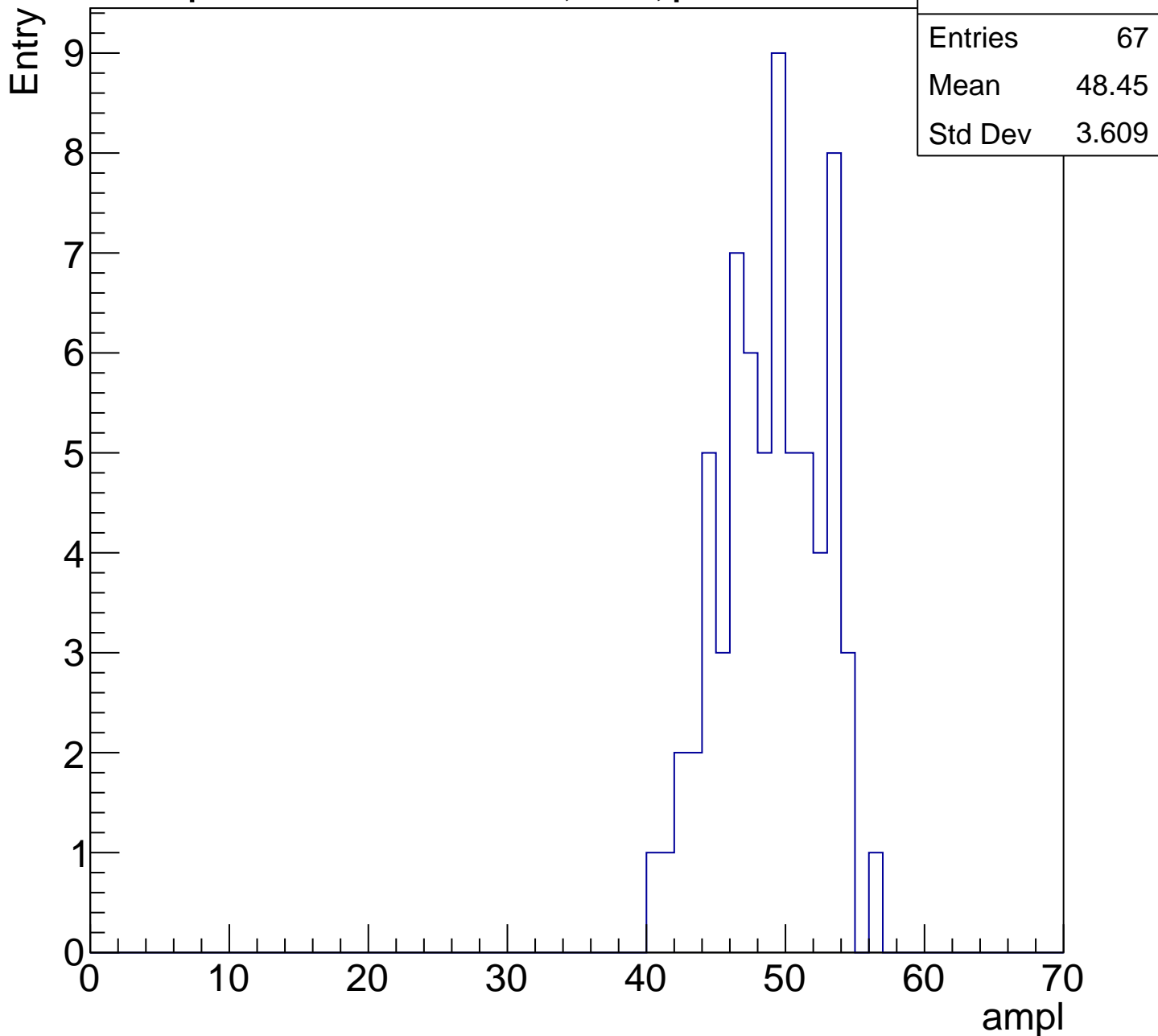
Entry

Entries	51
Mean	42.94
Std Dev	3.183



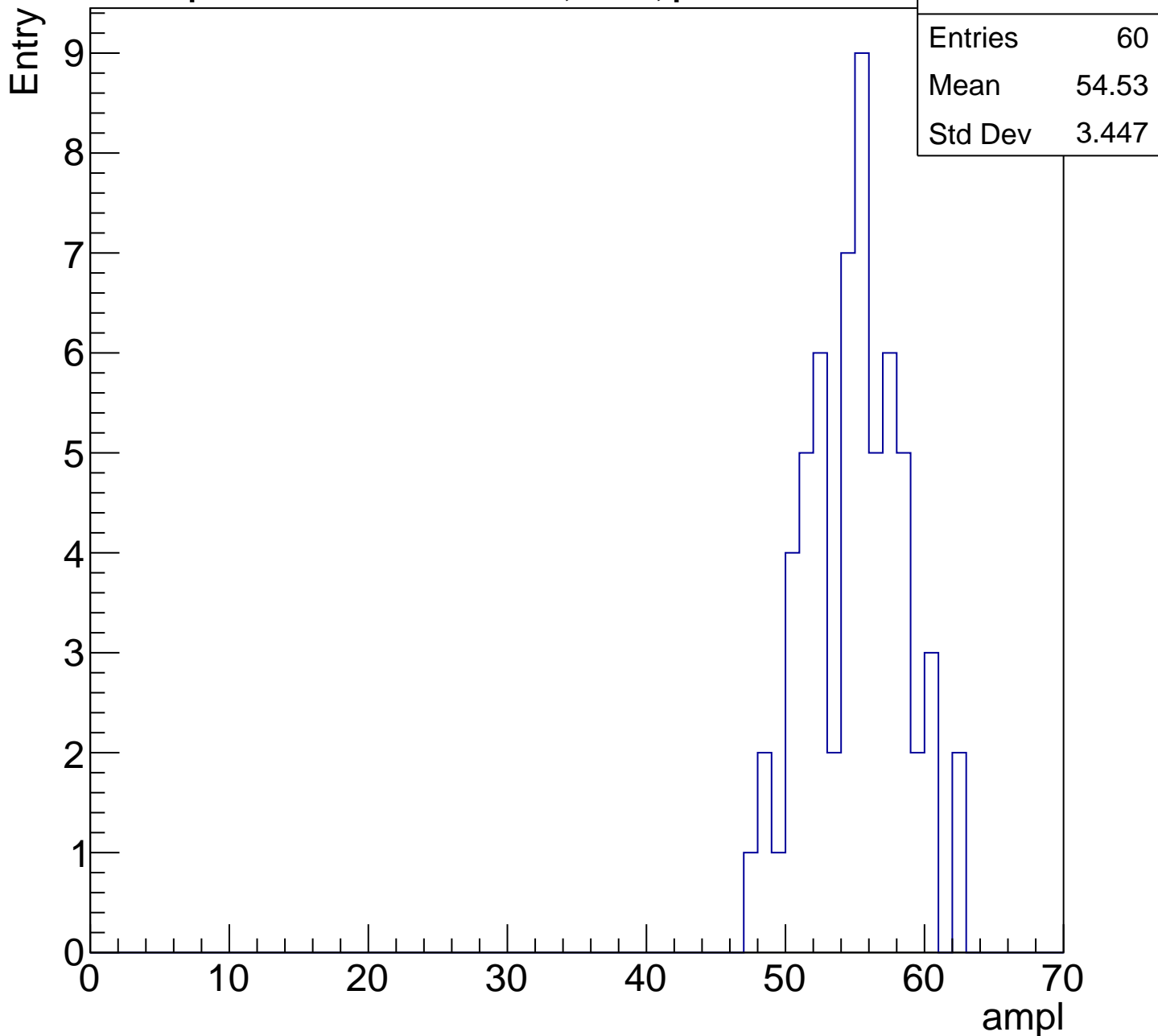
# B1L103S, U3-ch69, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2



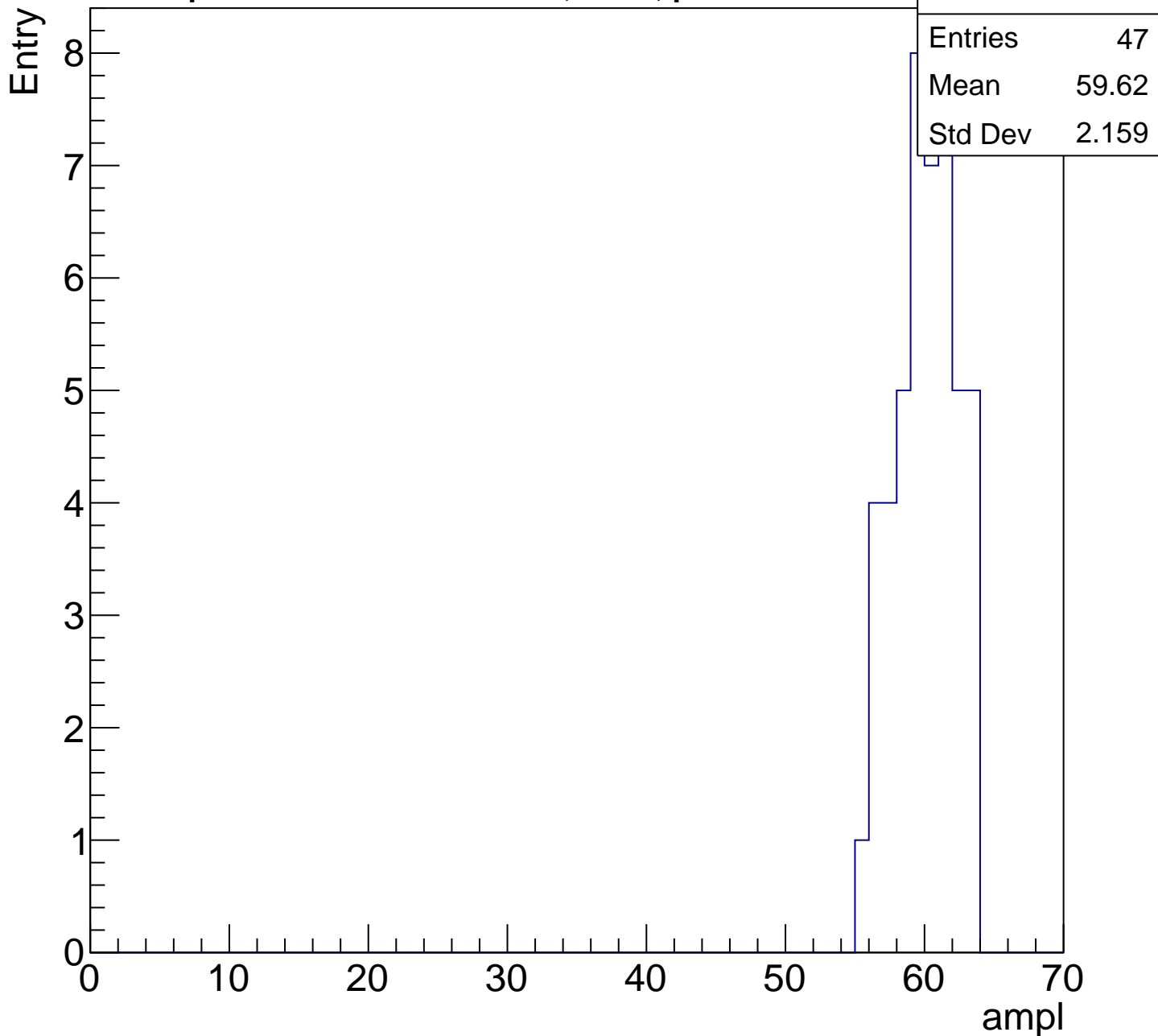
# B1L103S, U3-ch69, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U3-ch69, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U3-ch69, adc6

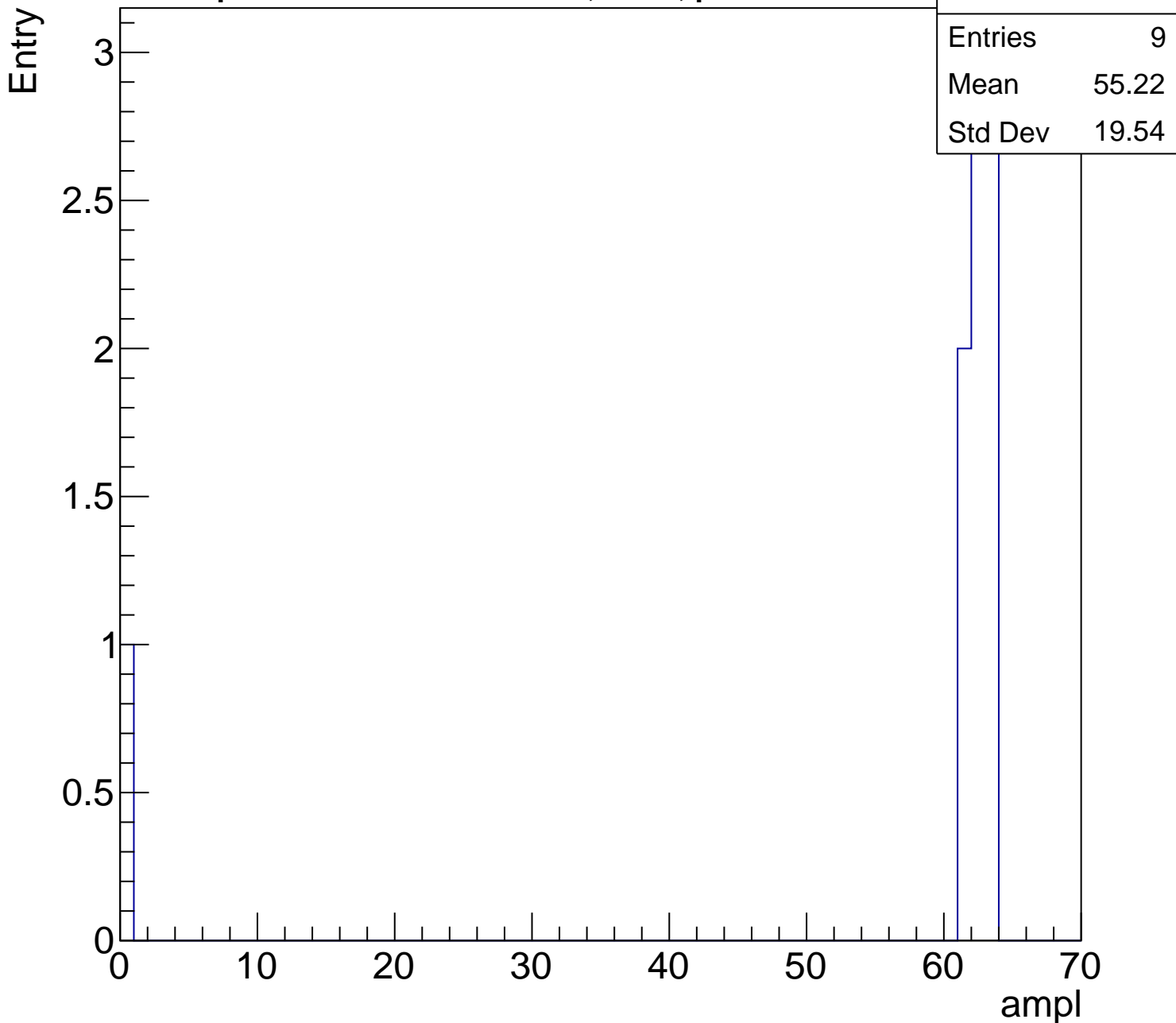
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

3  
2.5  
2  
1.5  
1  
0.5  
0

Entries	9
Mean	55.22
Std Dev	19.54

ampl

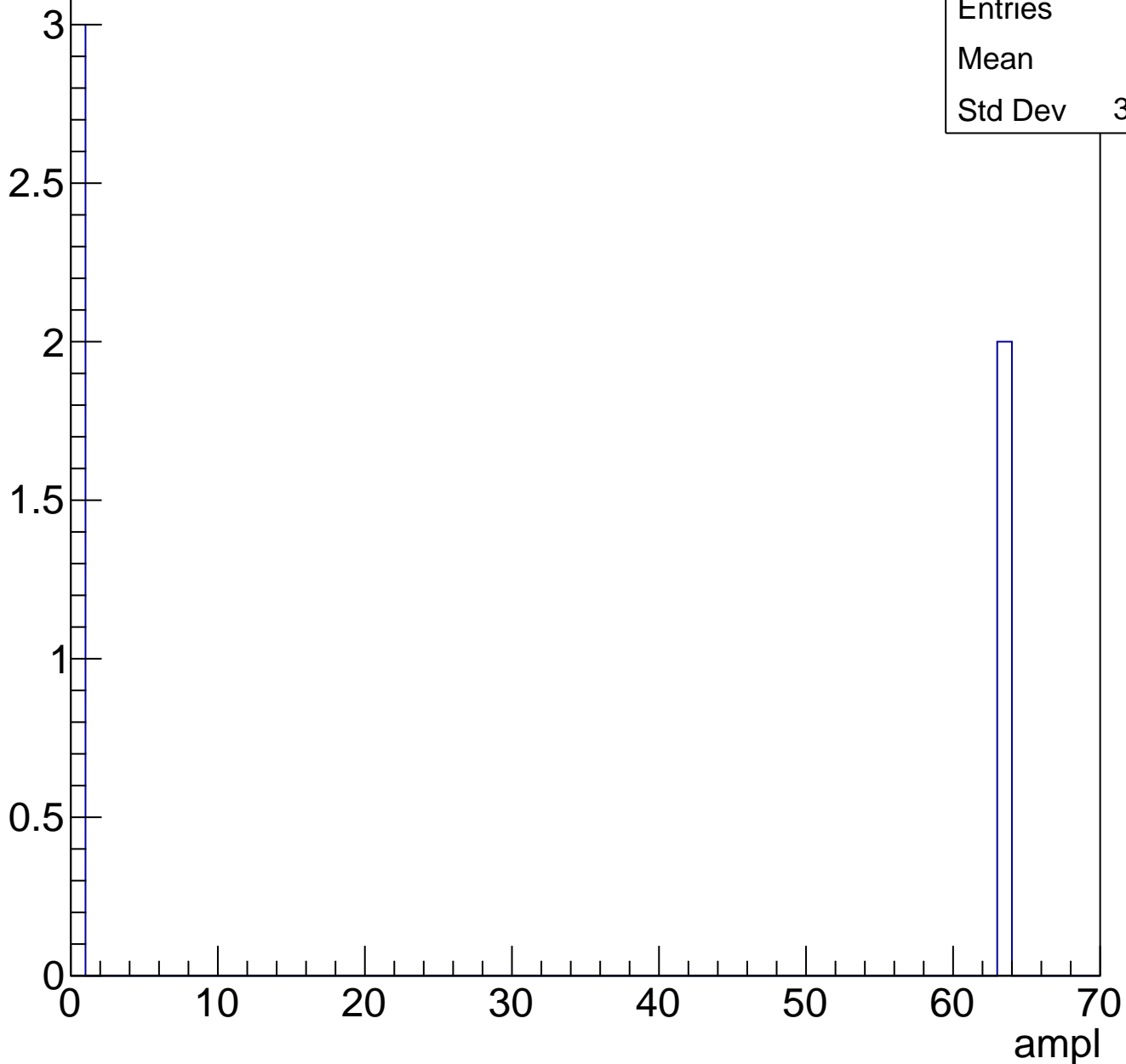




# B1L103S, U3-ch69, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch70, adc0

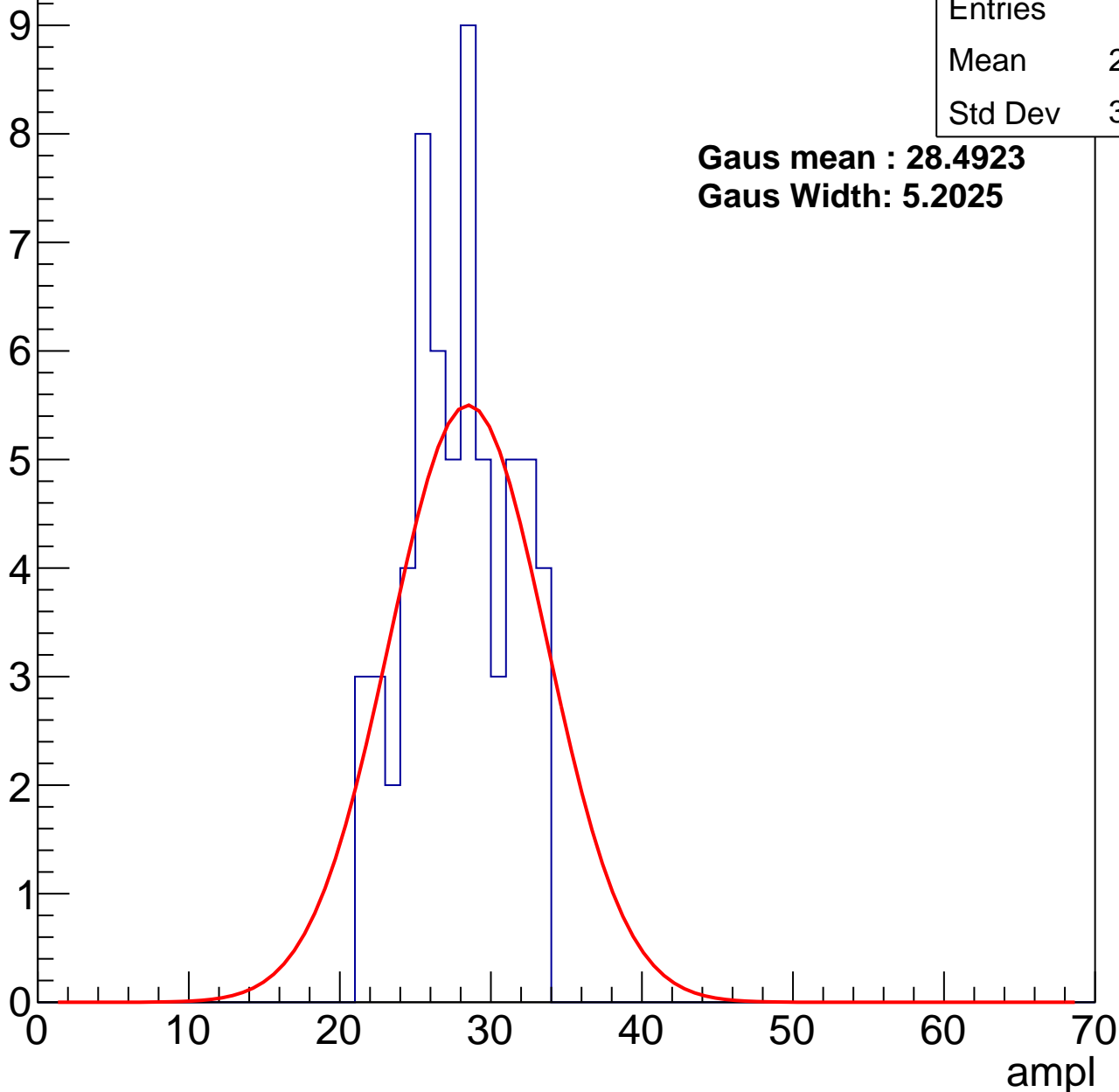
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	27.35
Std Dev	3.327

**Gaus mean : 28.4923**

**Gaus Width: 5.2025**



# B1L103S, U3-ch70, adc1

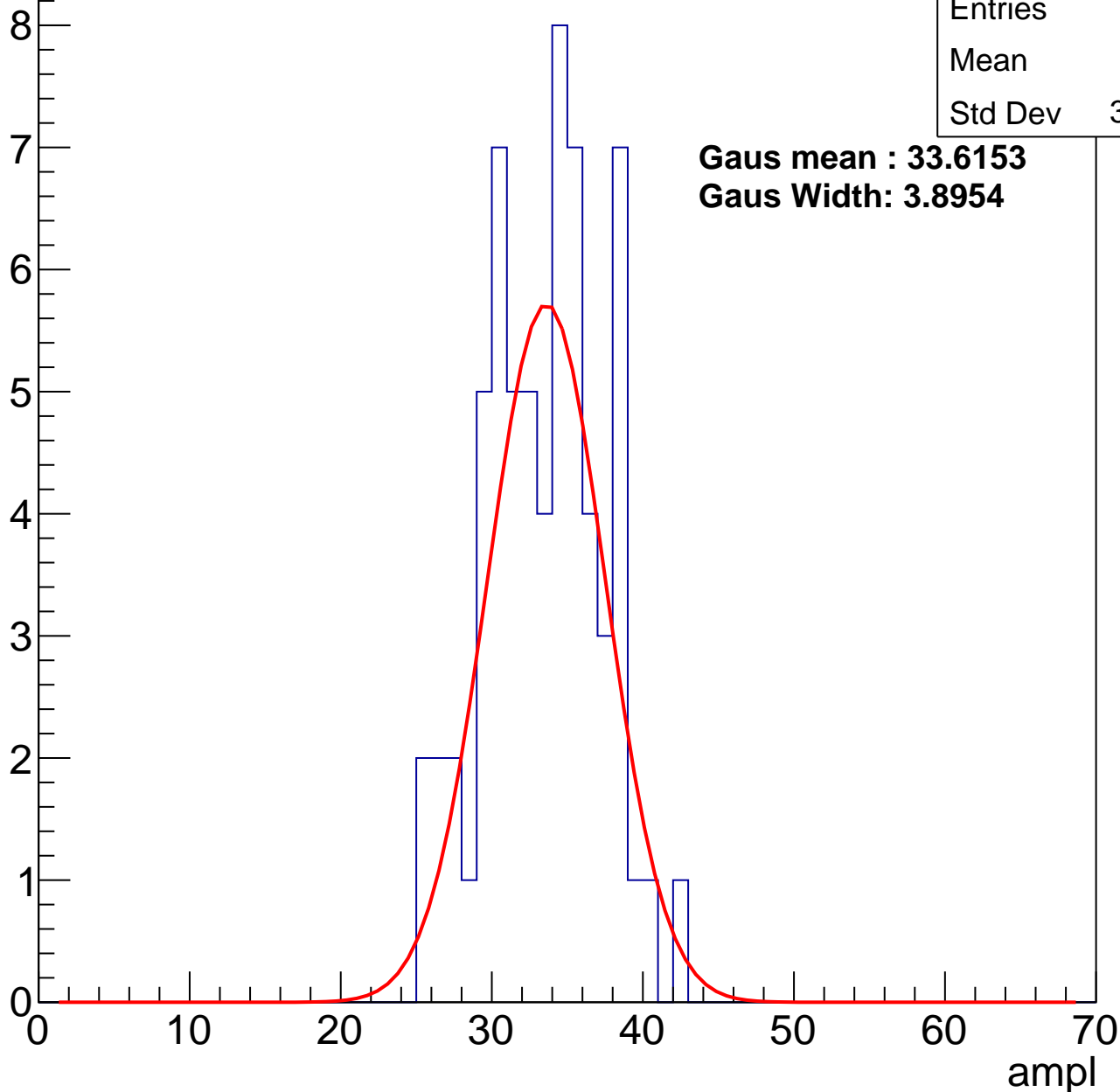
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	33
Std Dev	3.827

**Gaus mean : 33.6153**

**Gaus Width: 3.8954**



# B1L103S, U3-ch70, adc2

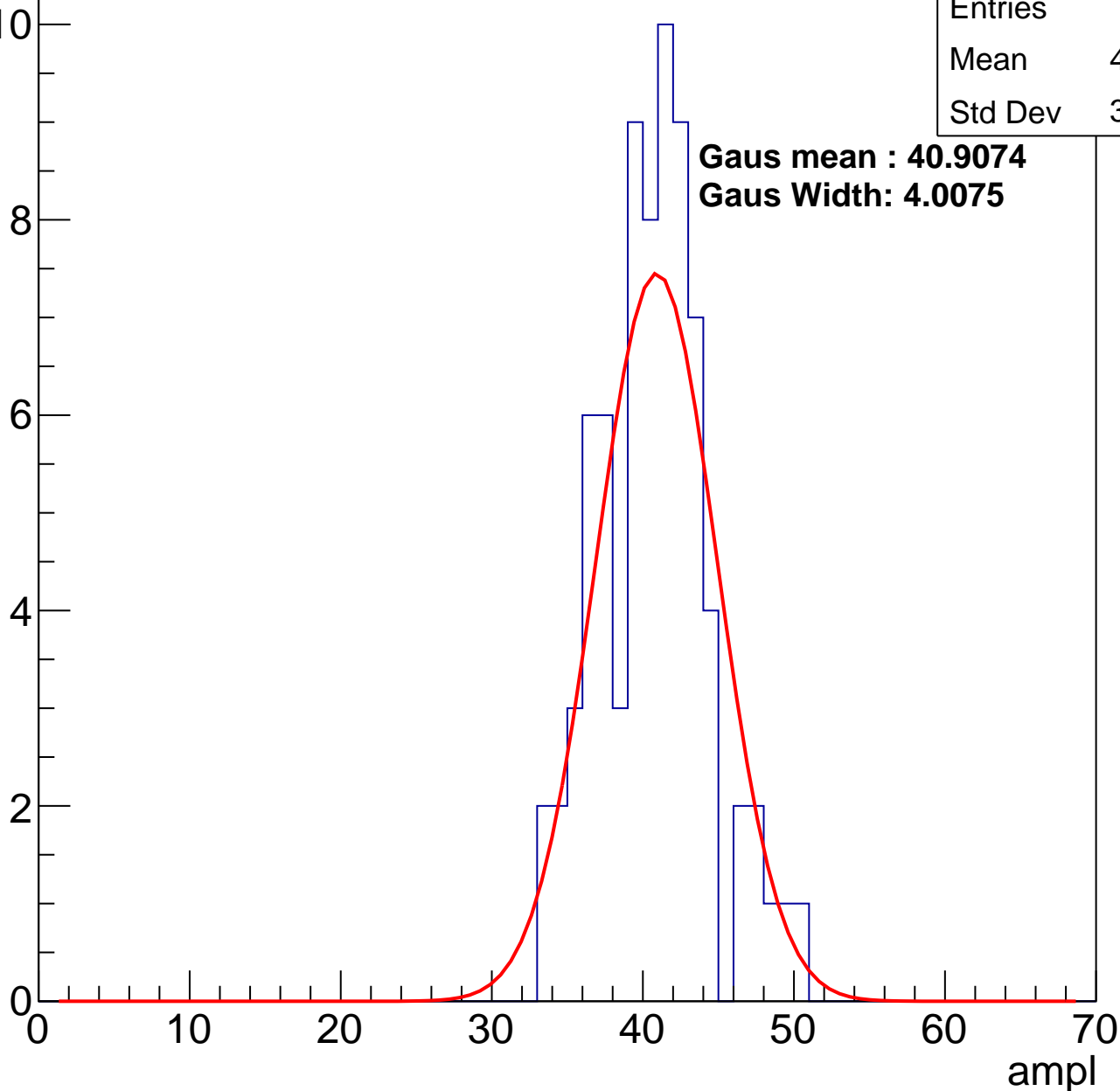
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	40.26
Std Dev	3.625

**Gaus mean : 40.9074**

**Gaus Width: 4.0075**

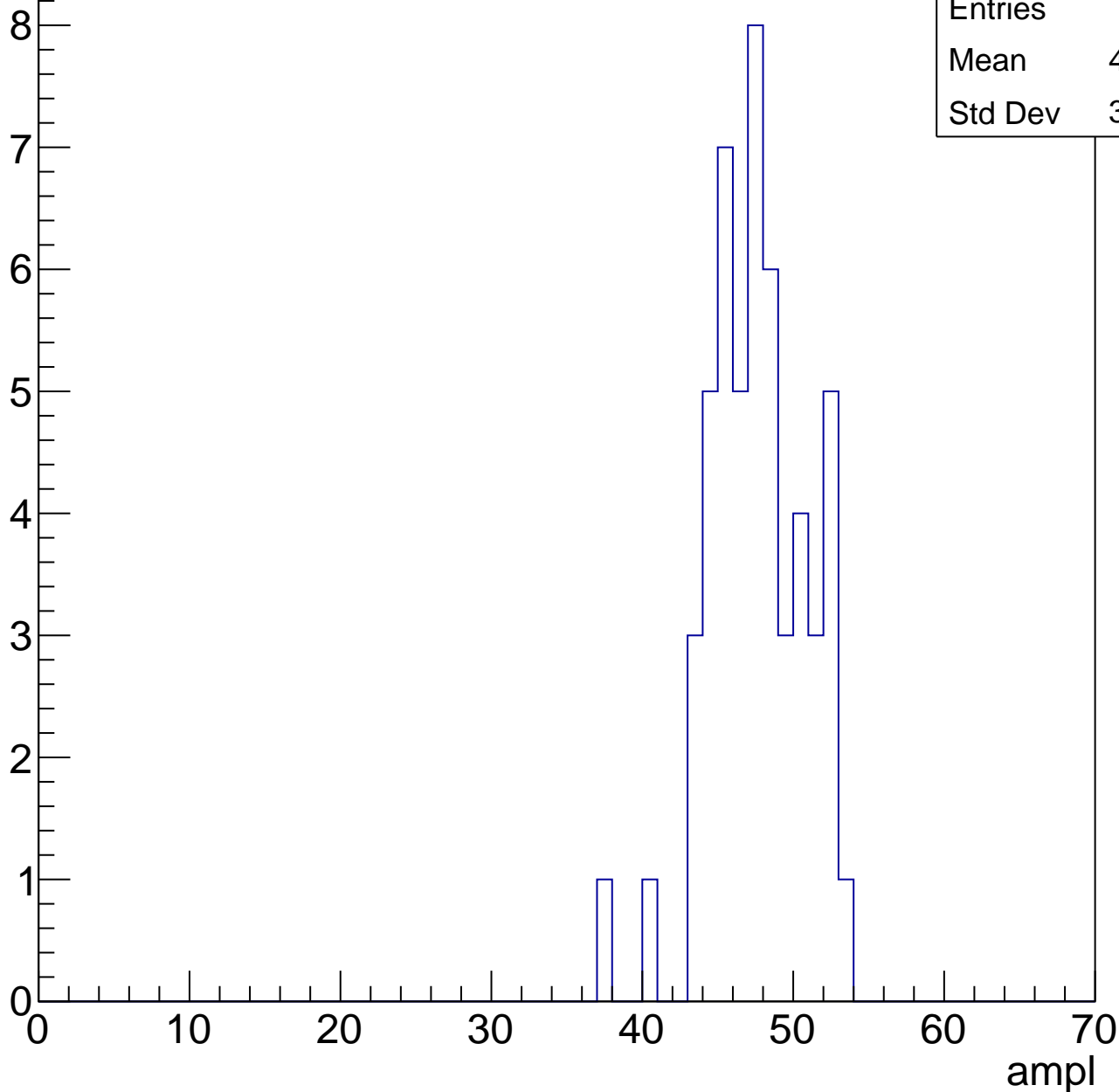


# B1L103S, U3-ch70, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

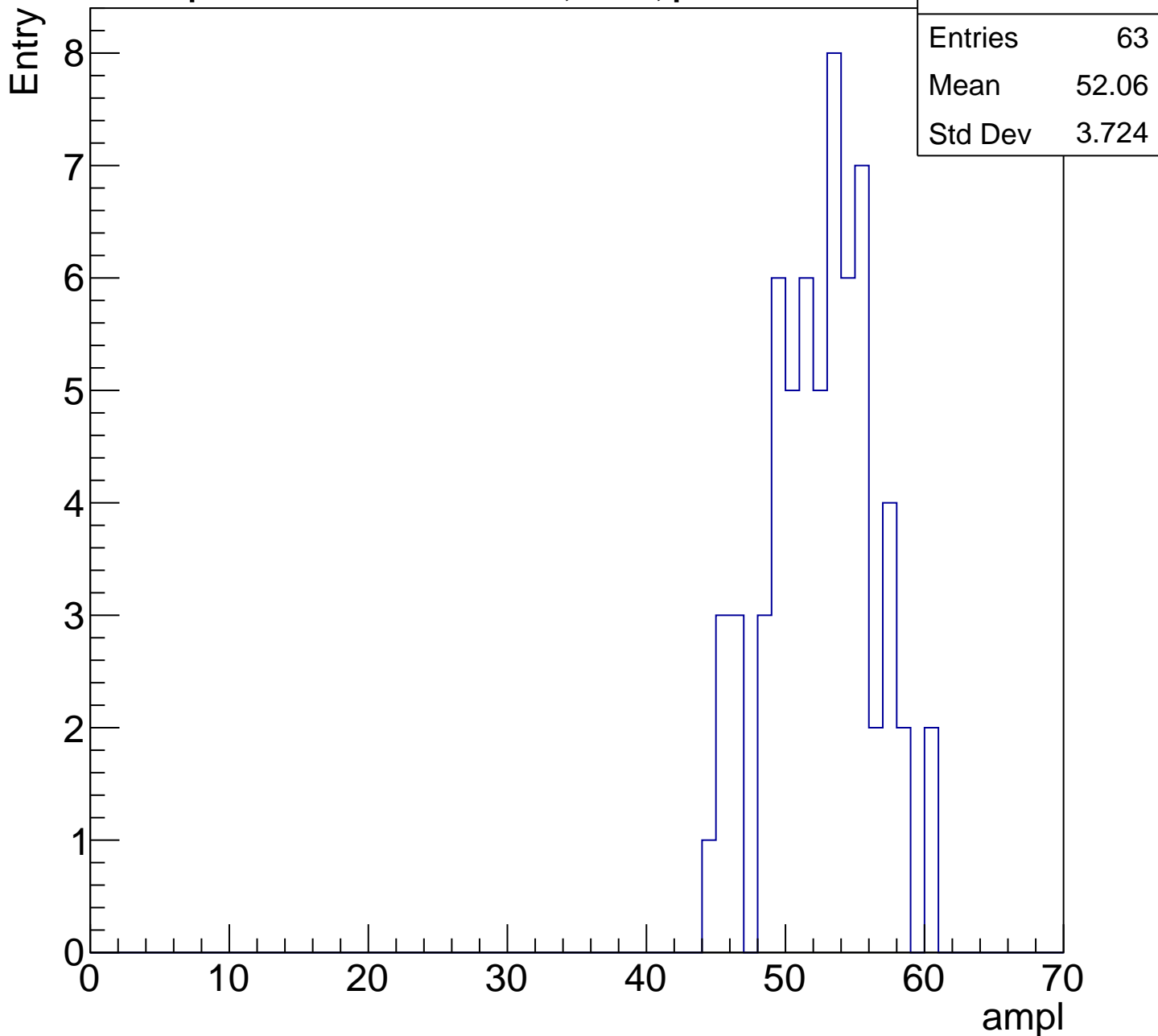
Entry

Entries	52
Mean	47.08
Std Dev	3.216



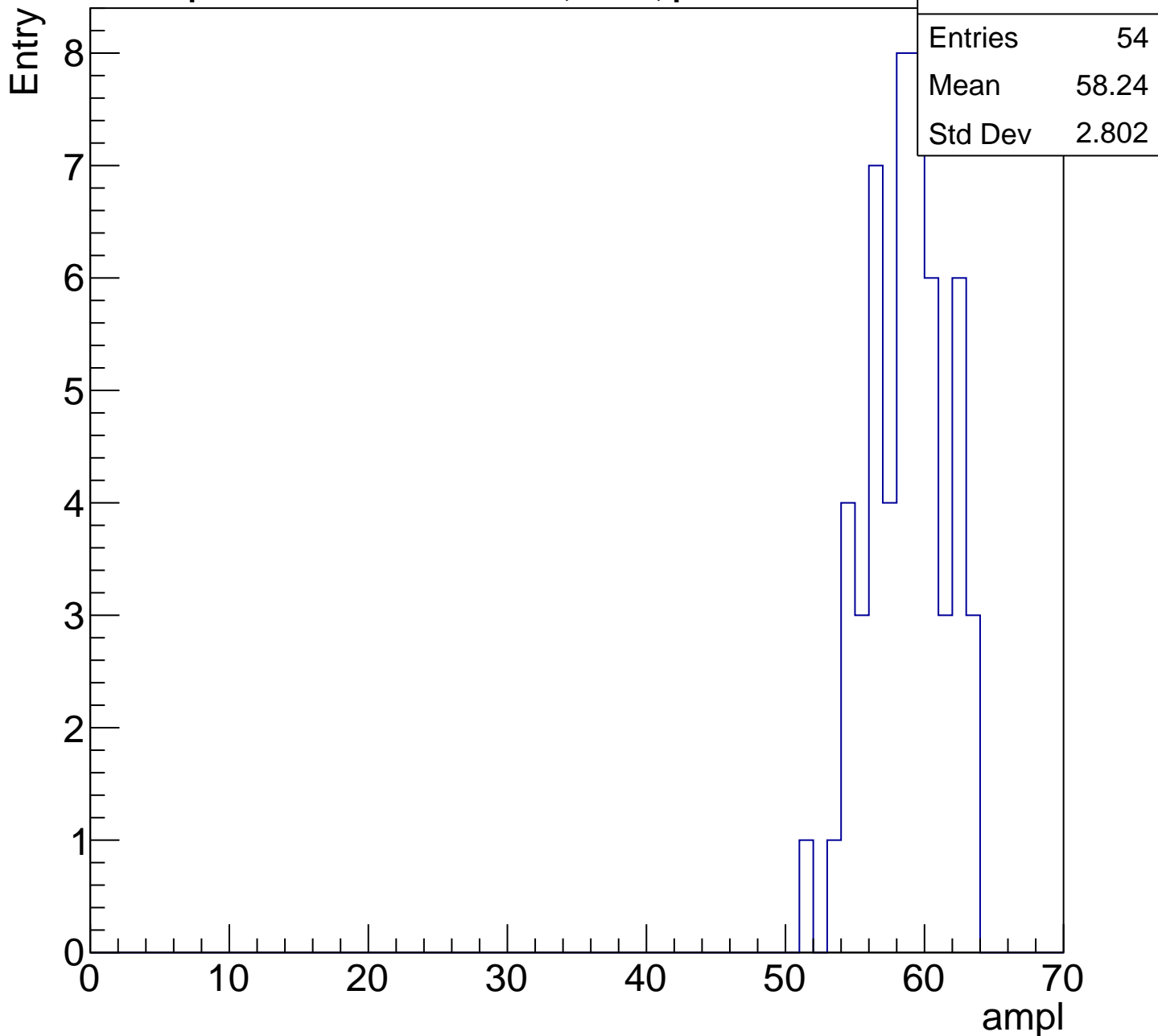
# B1L103S, U3-ch70, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U3-ch70, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

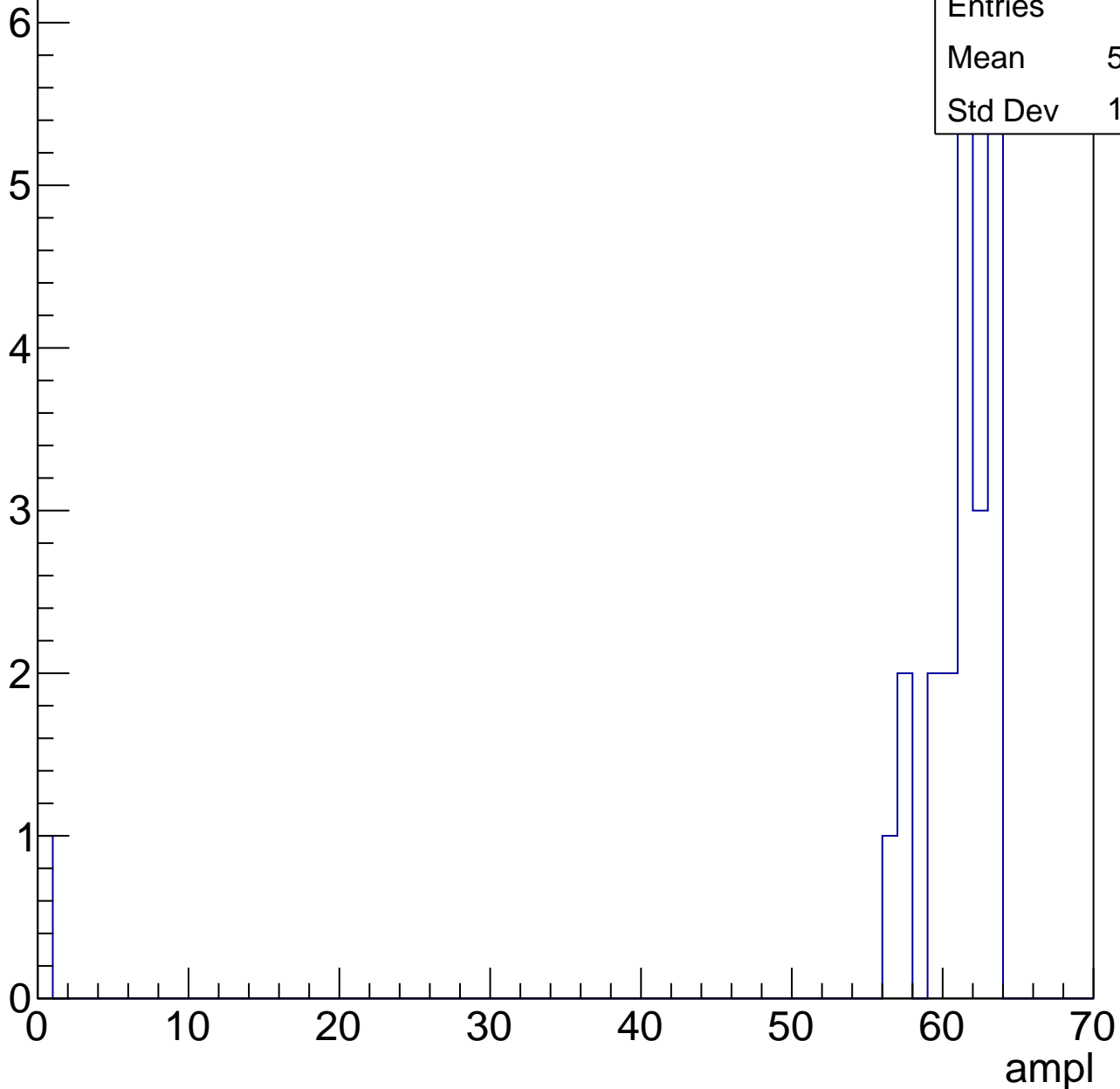


# B1L103S, U3-ch70, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	23
Mean	58.17
Std Dev	12.57

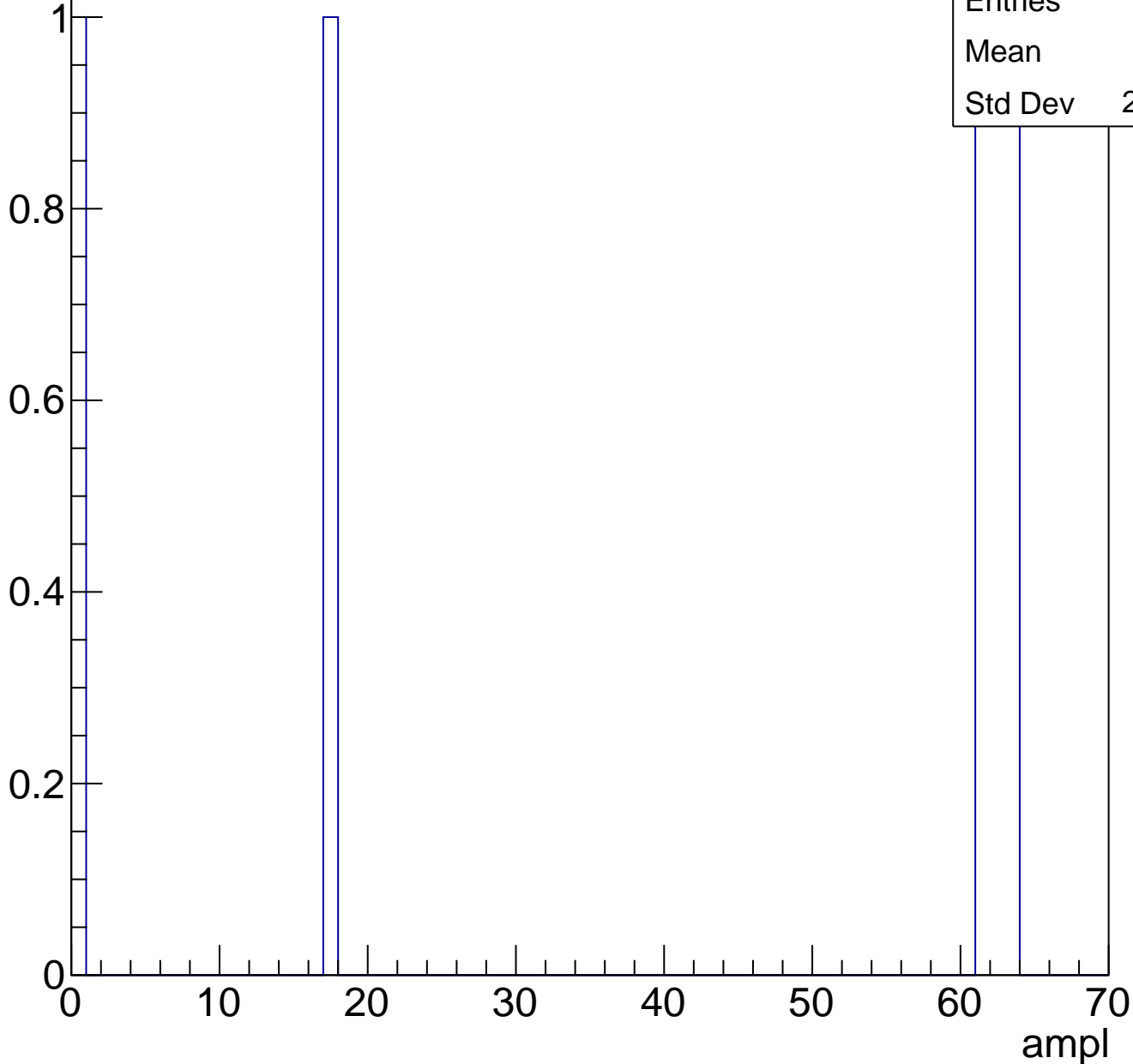




# B1L103S, U3-ch70, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch71, adc0

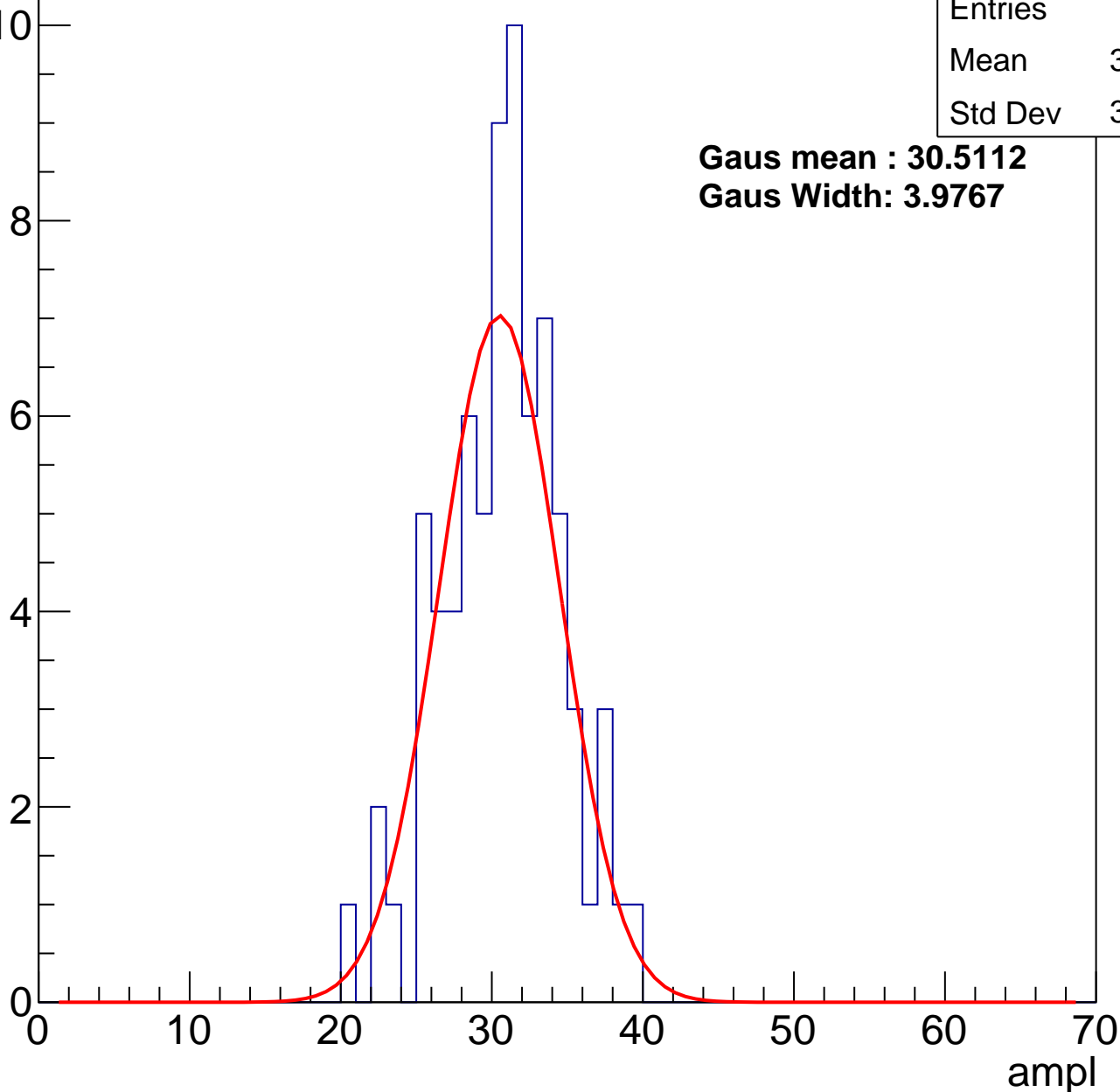
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	30.26
Std Dev	3.866

**Gaus mean : 30.5112**

**Gaus Width: 3.9767**



# B1L103S, U3-ch71, adc1

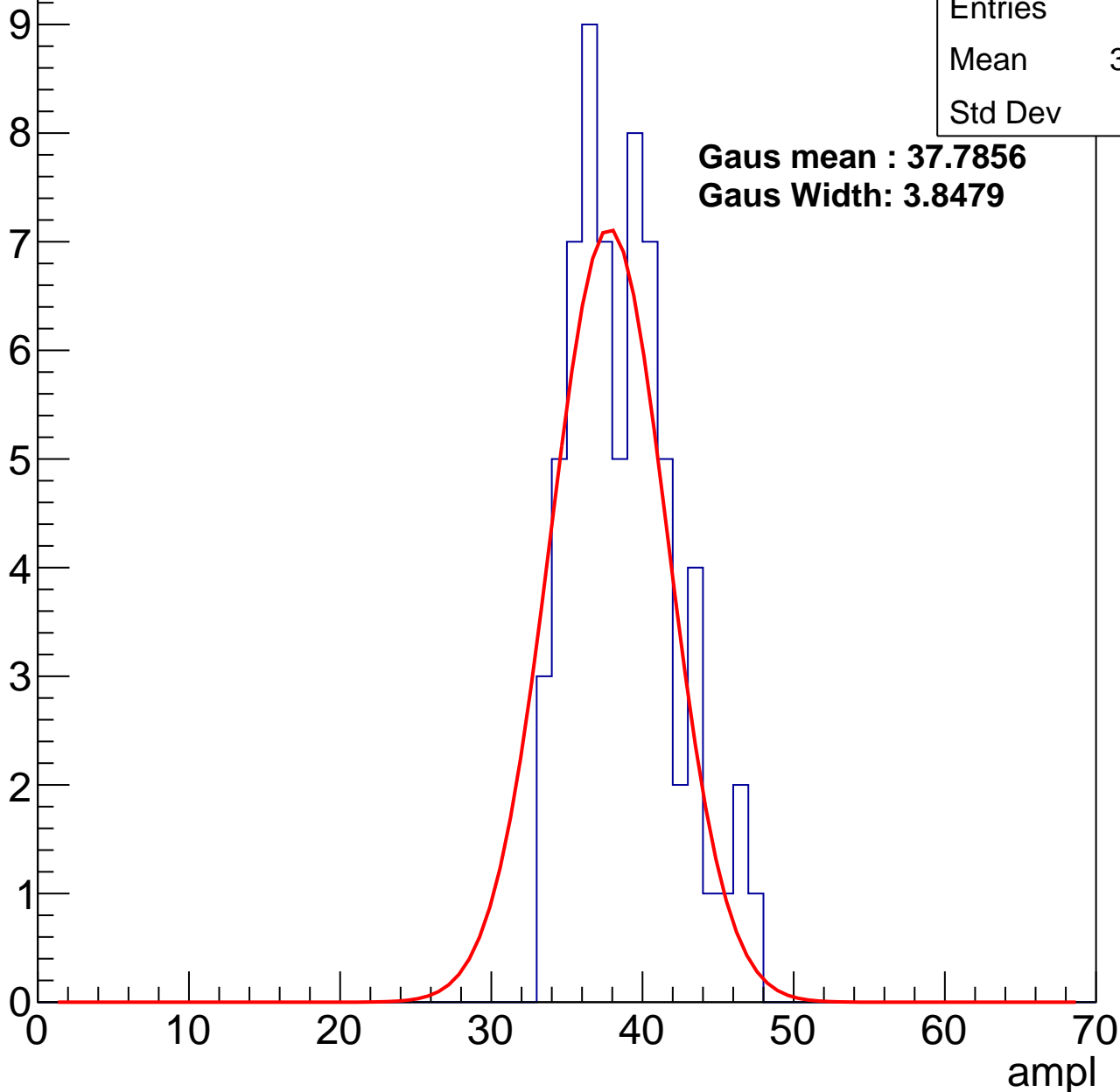
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	38.33
Std Dev	3.37

**Gaus mean : 37.7856**

**Gaus Width: 3.8479**



# B1L103S, U3-ch71, adc2

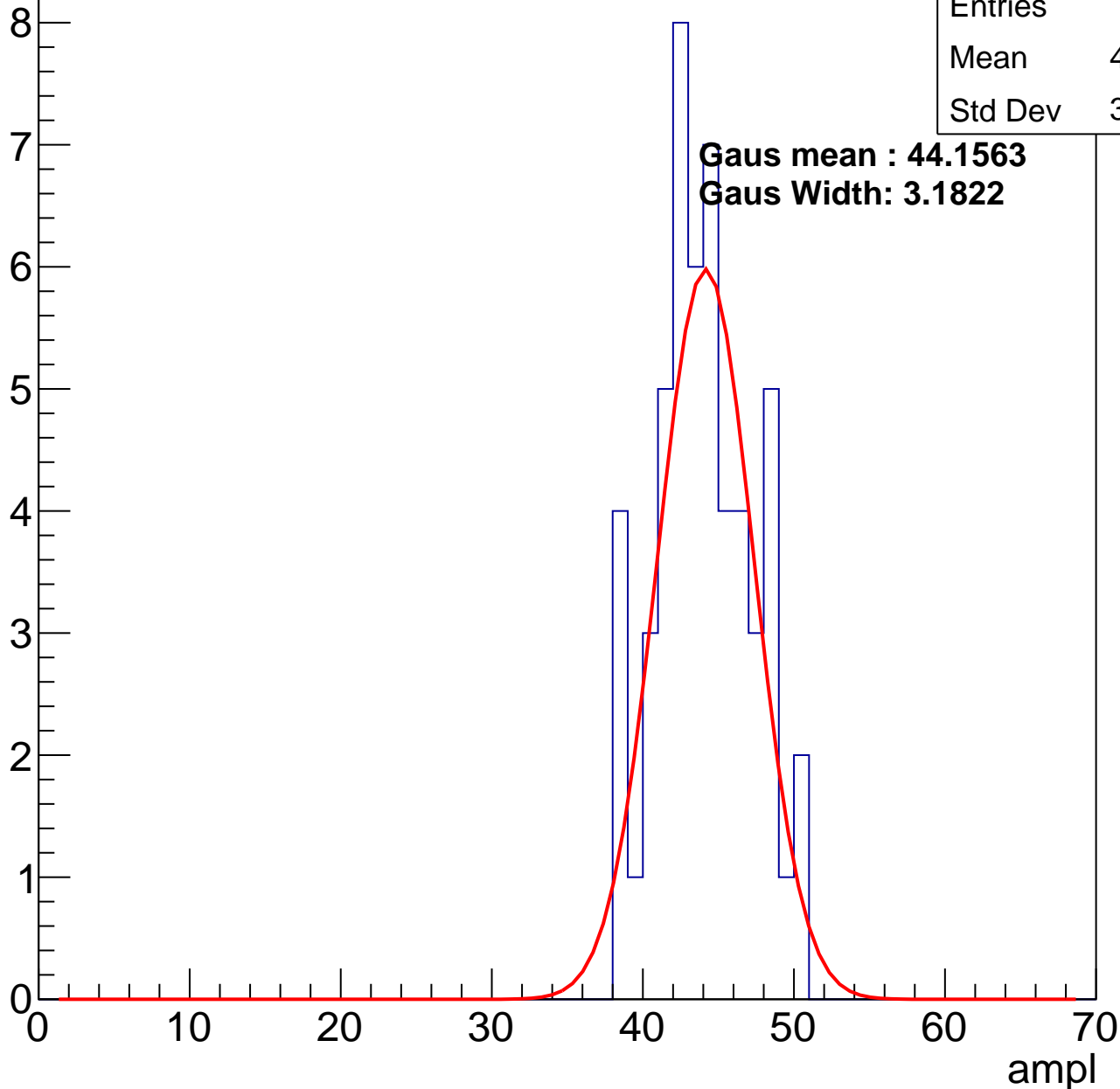
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	43.62
Std Dev	3.122

**Gaus mean : 44.1563**

**Gaus Width: 3.1822**

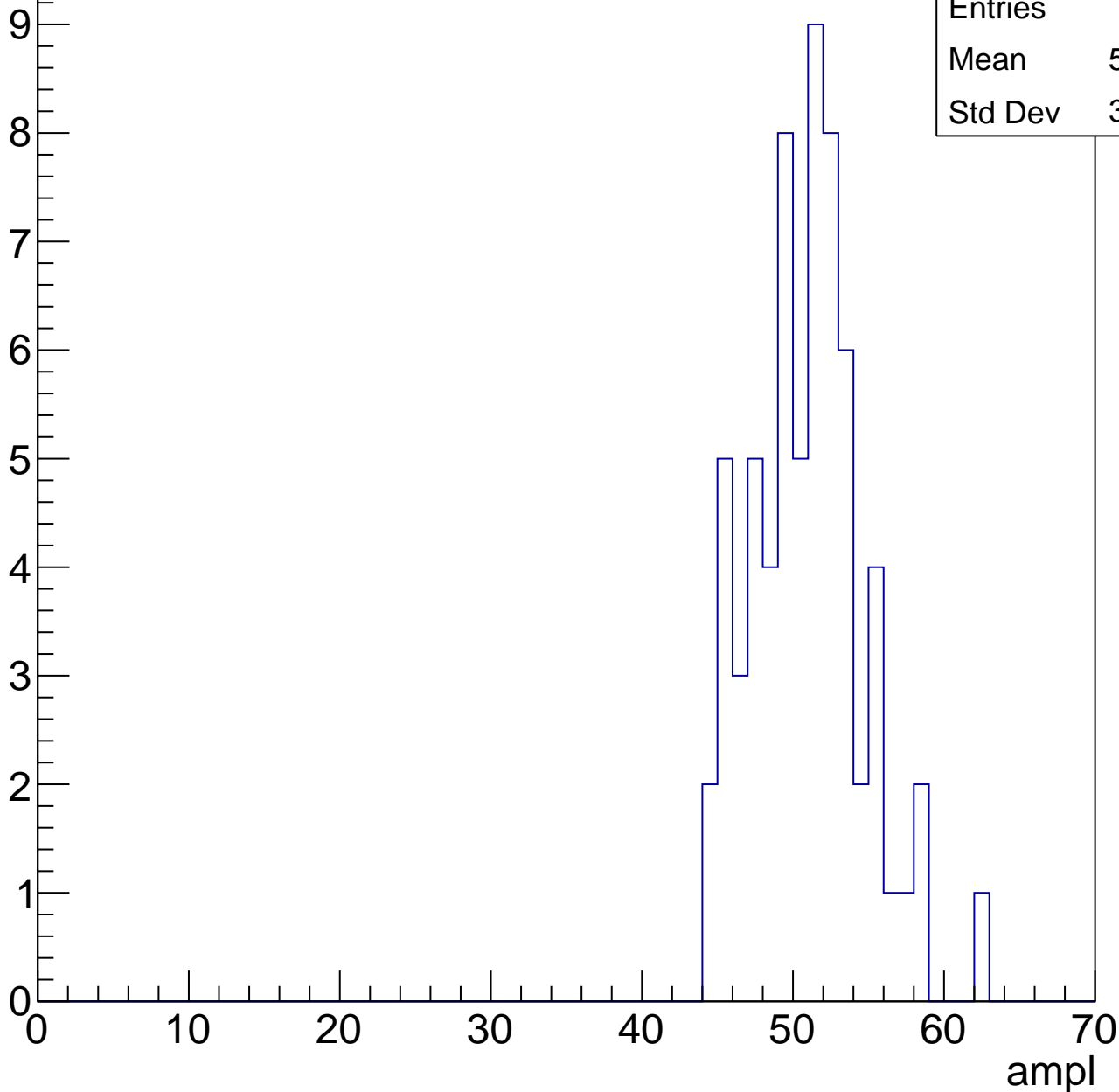


# B1L103S, U3-ch71, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

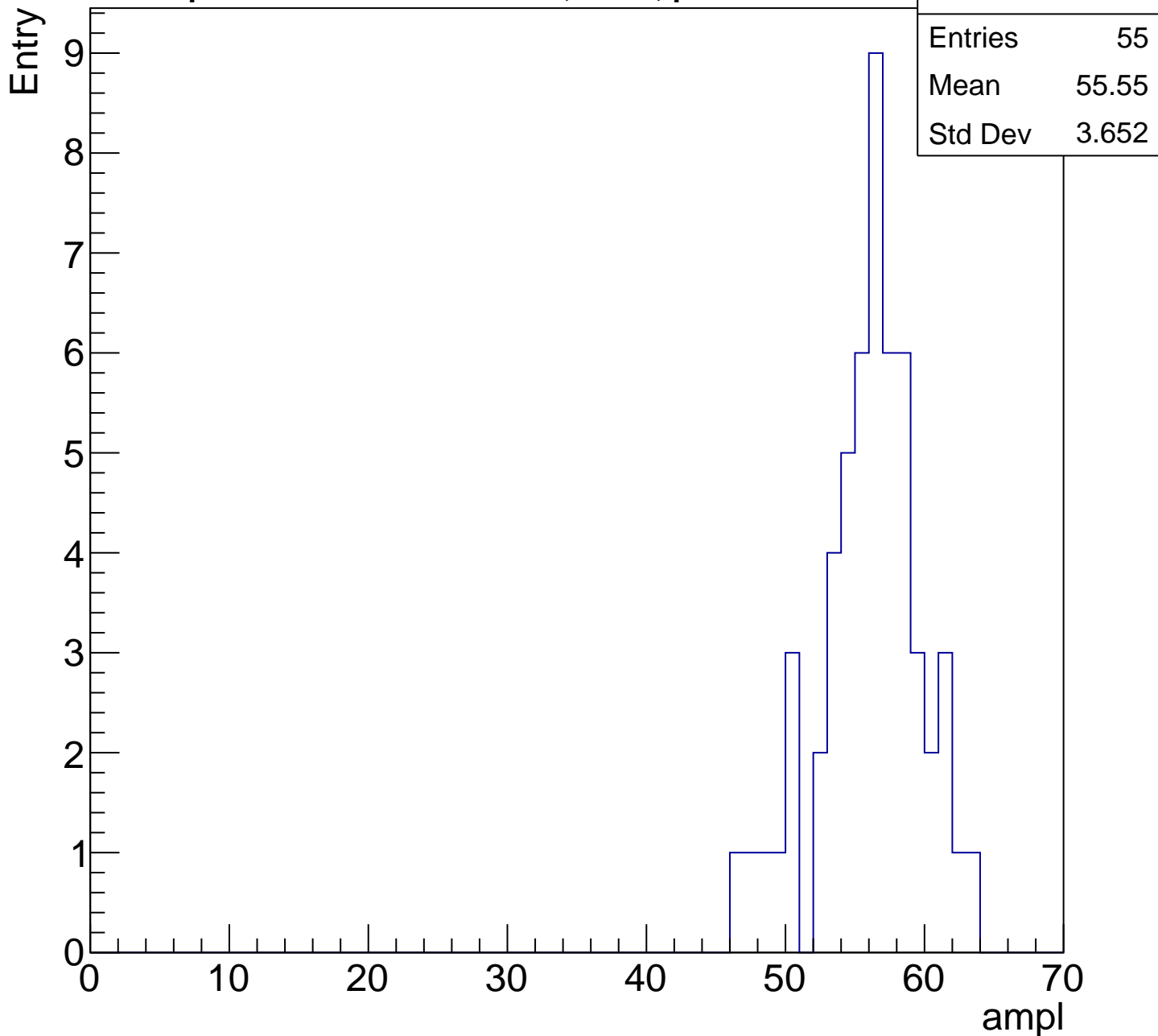
Entry

Entries	66
Mean	50.48
Std Dev	3.657



# B1L103S, U3-ch71, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U3-ch71, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

7

6

5

4

3

2

1

0

Entries 41

Mean 59.76

Std Dev 2.765

0

10

20

30

40

50

60

ampl

0

10

20

30

40

50

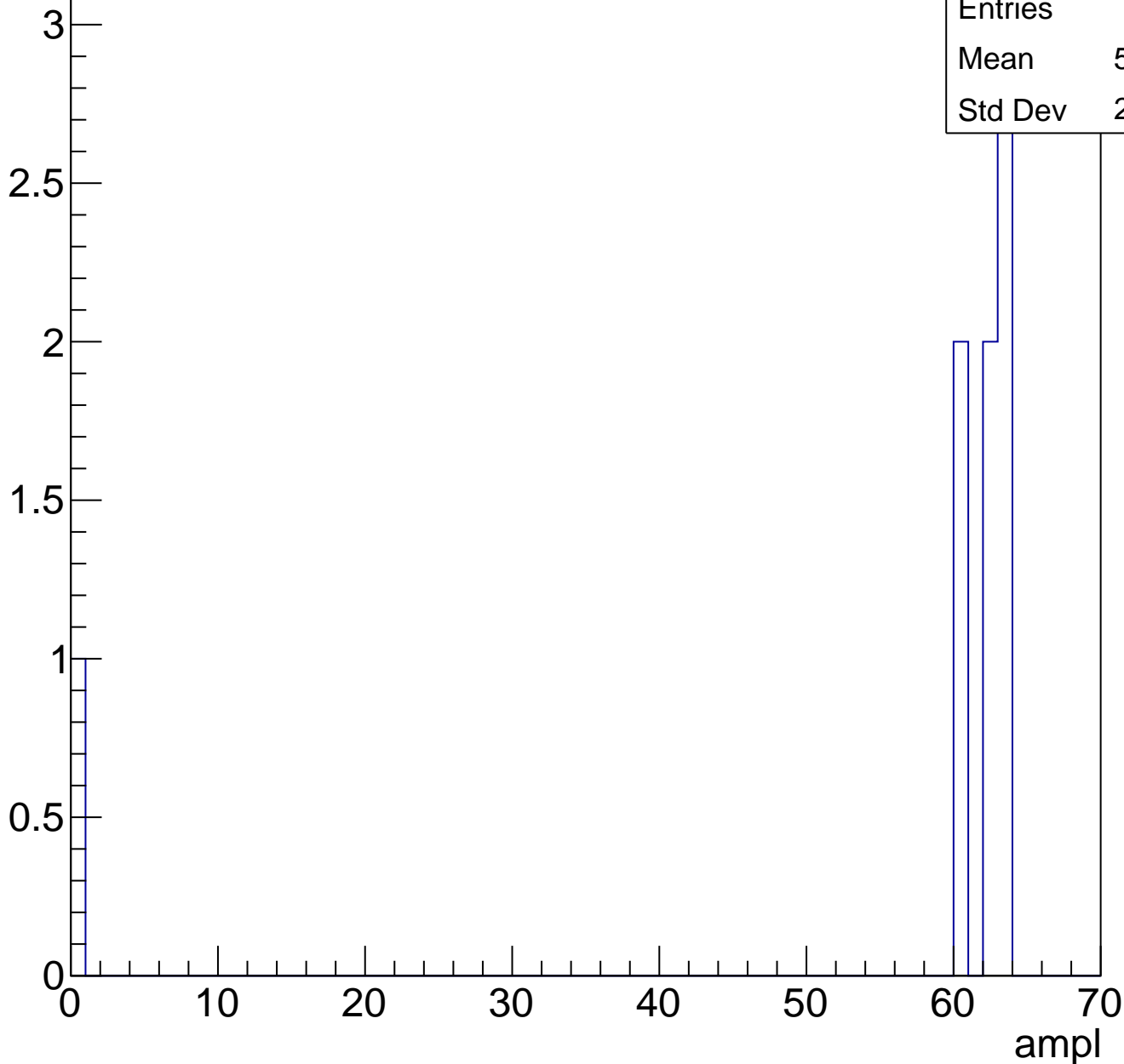
60

ampl

# B1L103S, U3-ch71, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U3-ch71, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L103S, U3-ch72, adc0

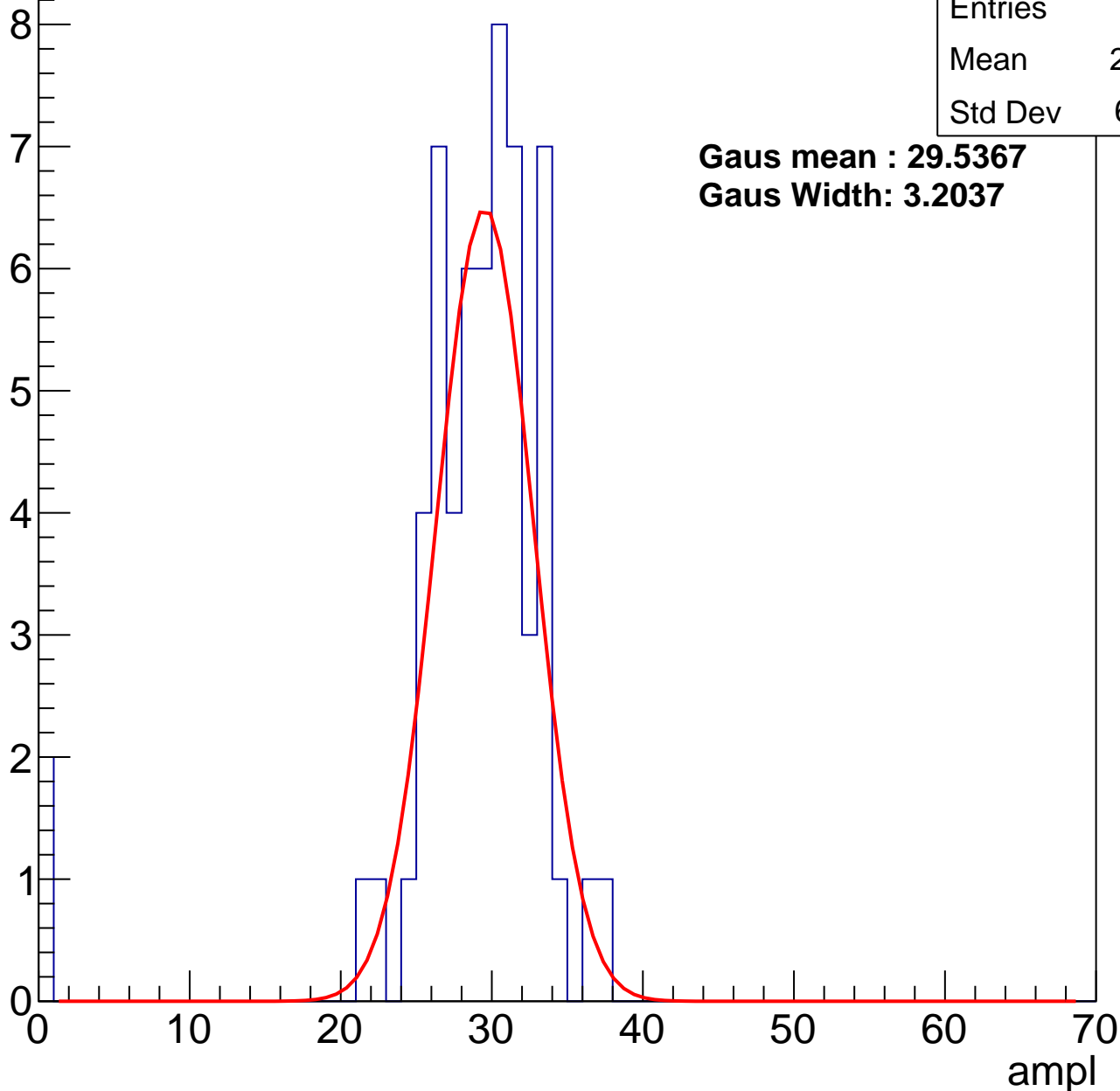
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	28.17
Std Dev	6.111

**Gaus mean : 29.5367**

**Gaus Width: 3.2037**



# B1L103S, U3-ch72, adc1

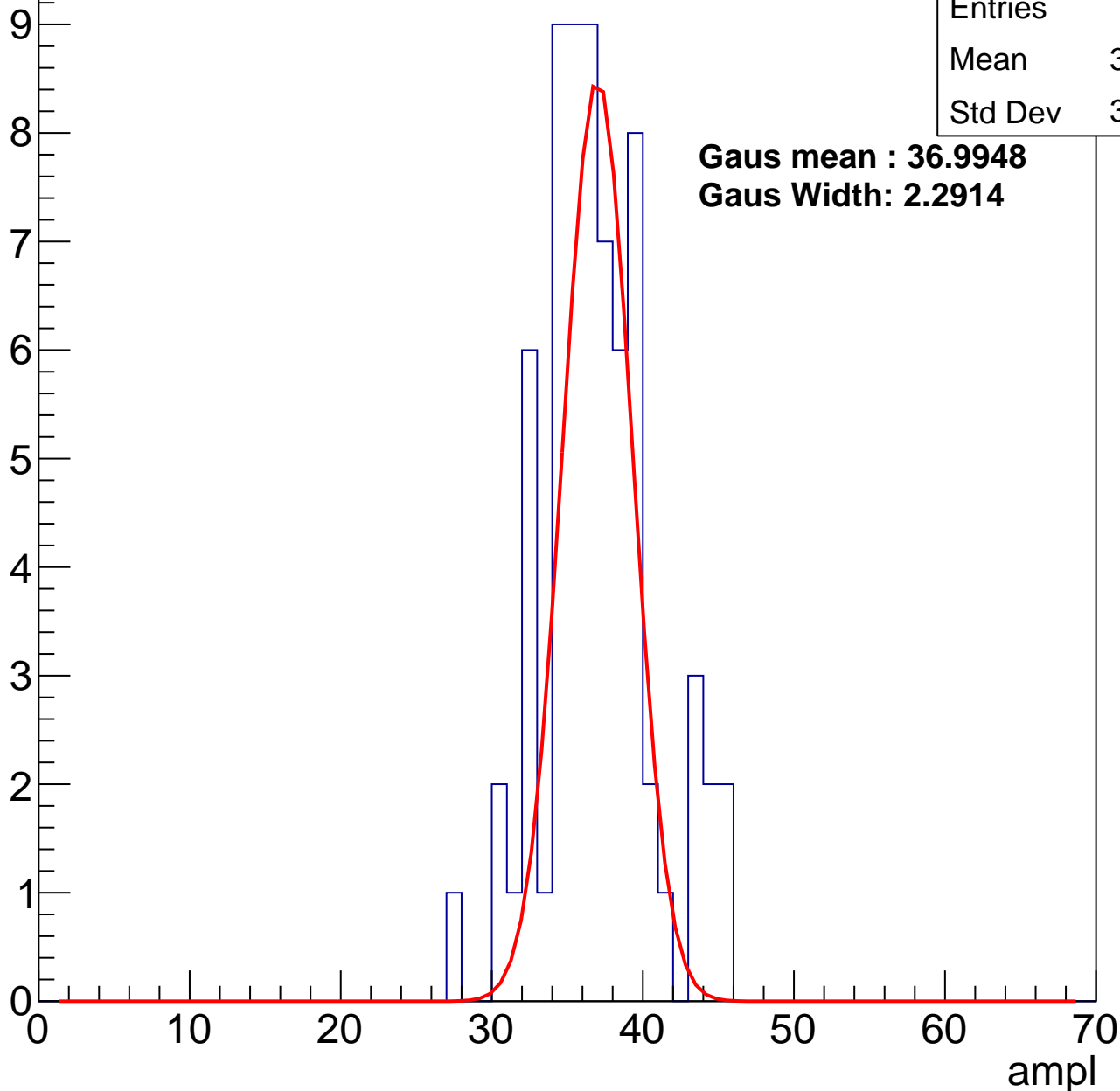
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	36.45
Std Dev	3.634

**Gaus mean : 36.9948**

**Gaus Width: 2.2914**



# B1L103S, U3-ch72, adc2

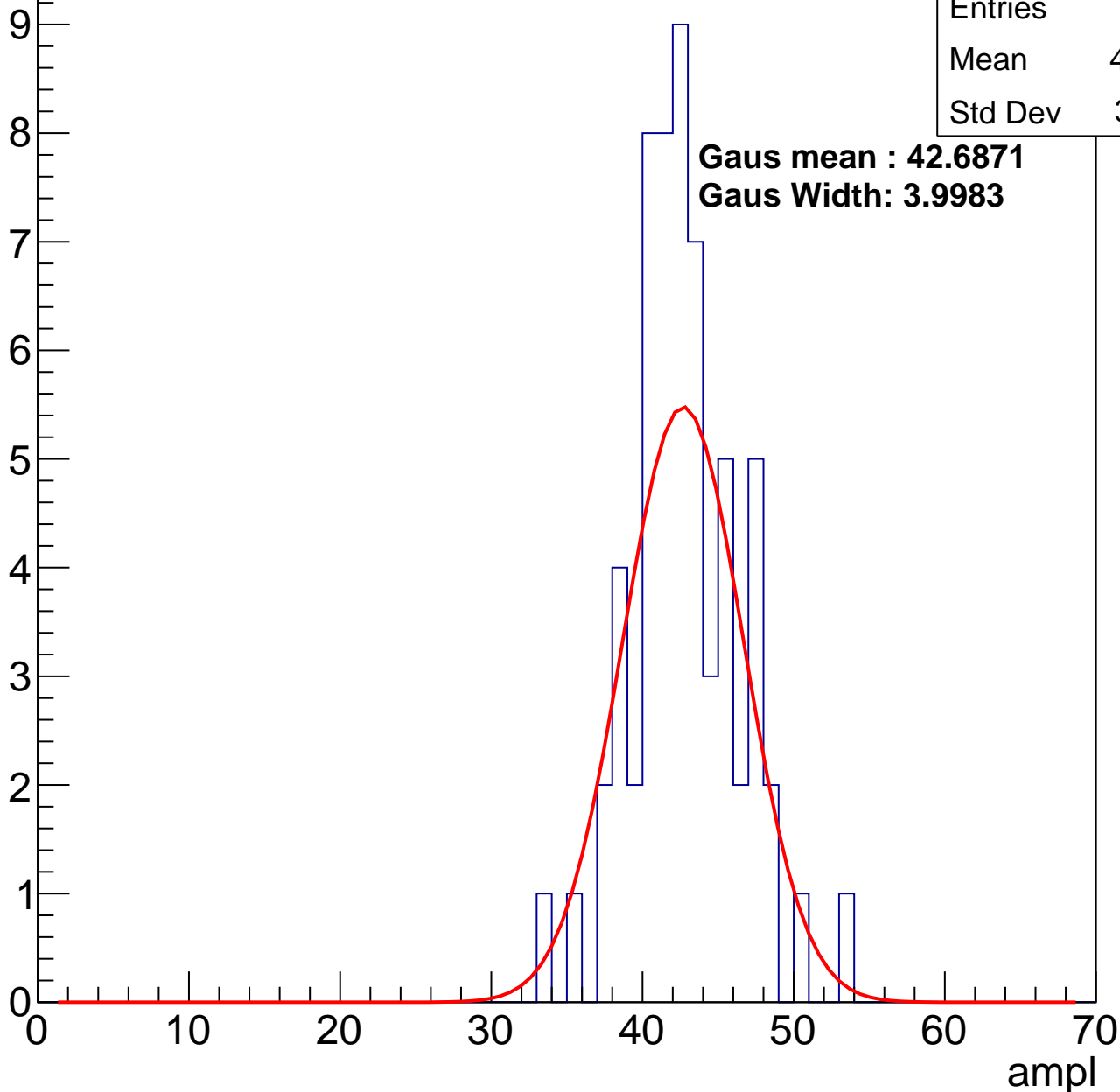
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	42.33
Std Dev	3.561

**Gaus mean : 42.6871**

**Gaus Width: 3.9983**

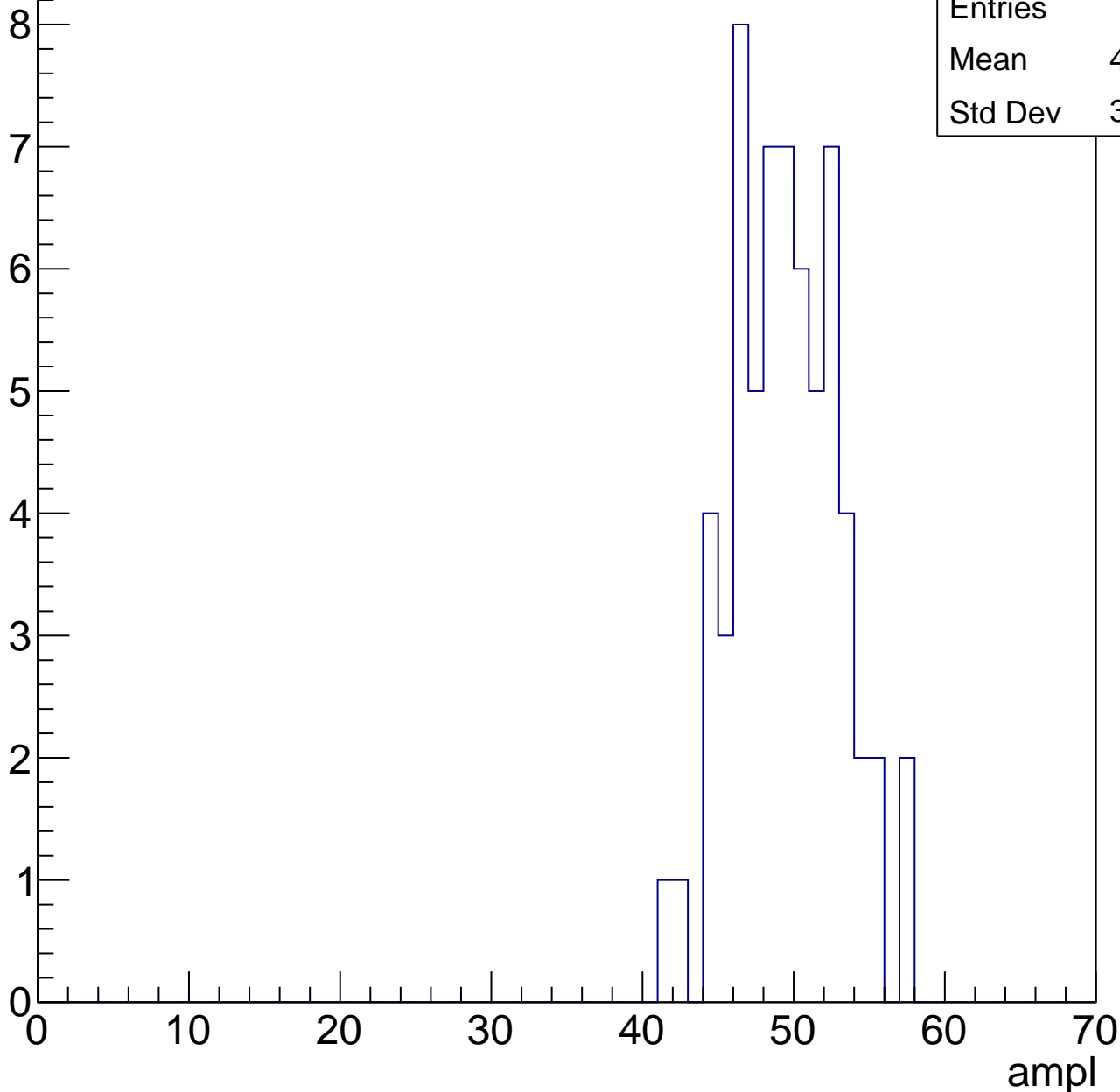


# B1L103S, U3-ch72, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

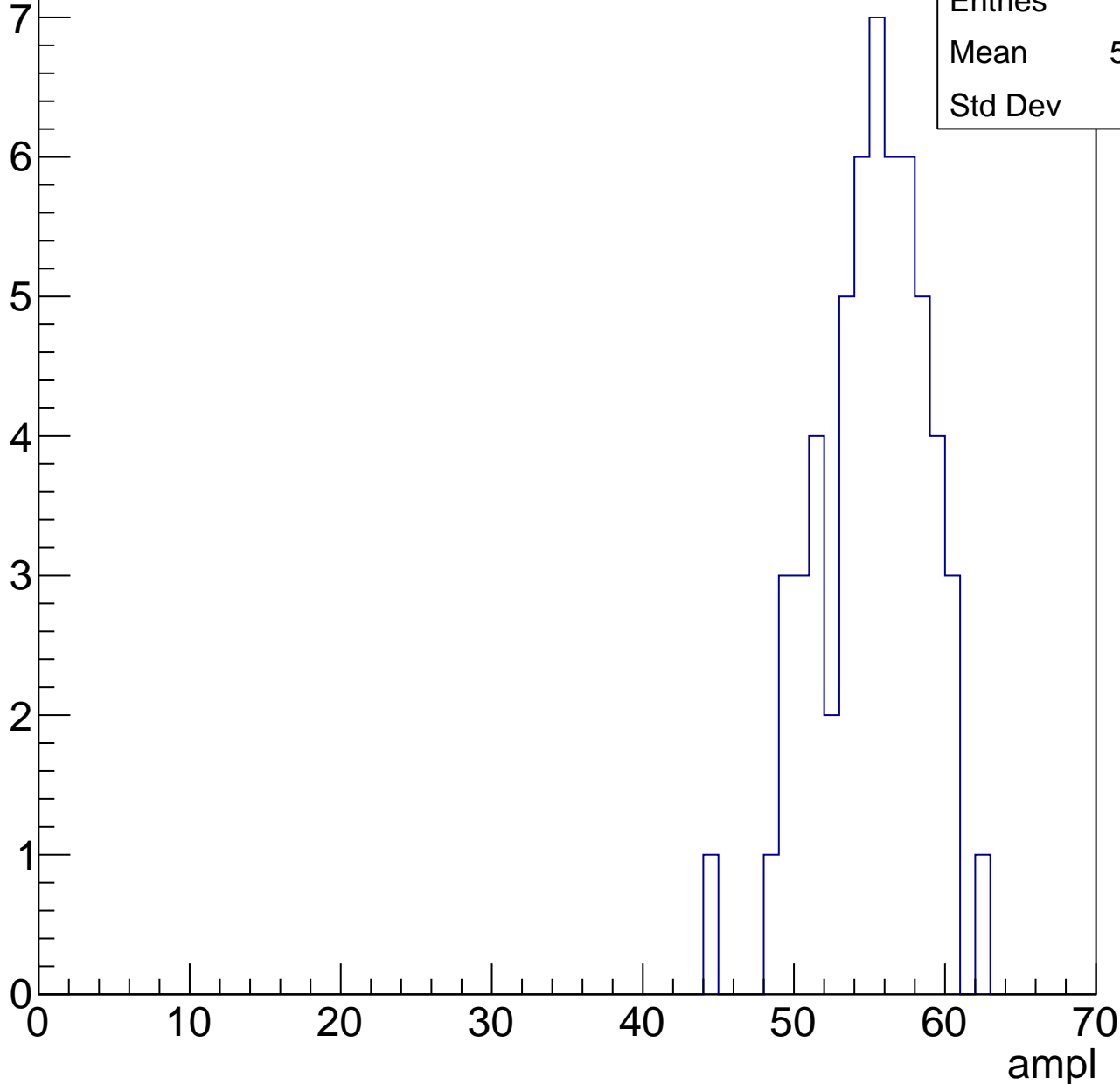
Entries	64
Mean	49.05
Std Dev	3.452



# B1L103S, U3-ch72, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



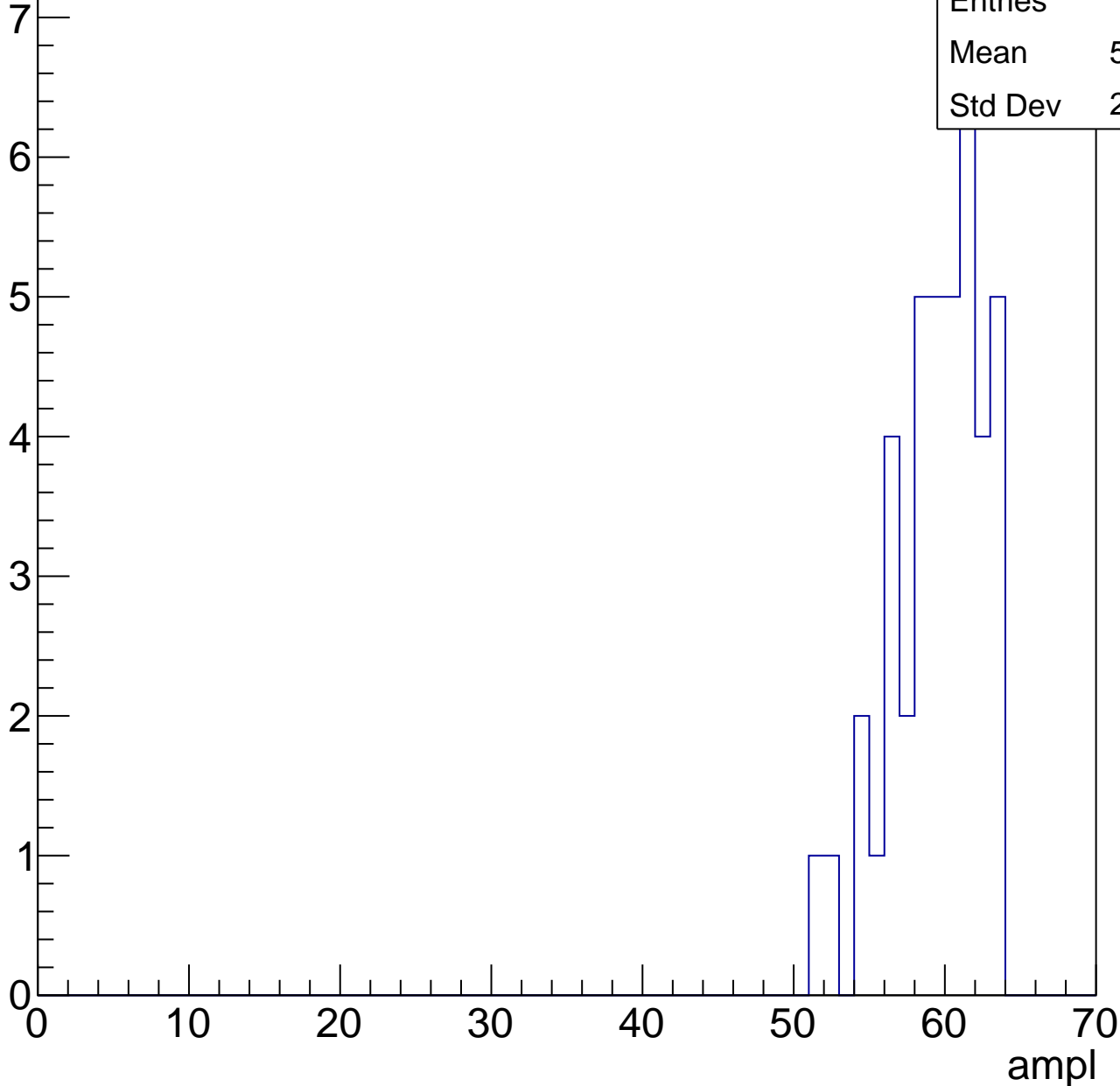
Entries	57
Mean	54.68
Std Dev	3.55

# B1L103S, U3-ch72, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	42
Mean	59.02
Std Dev	2.996

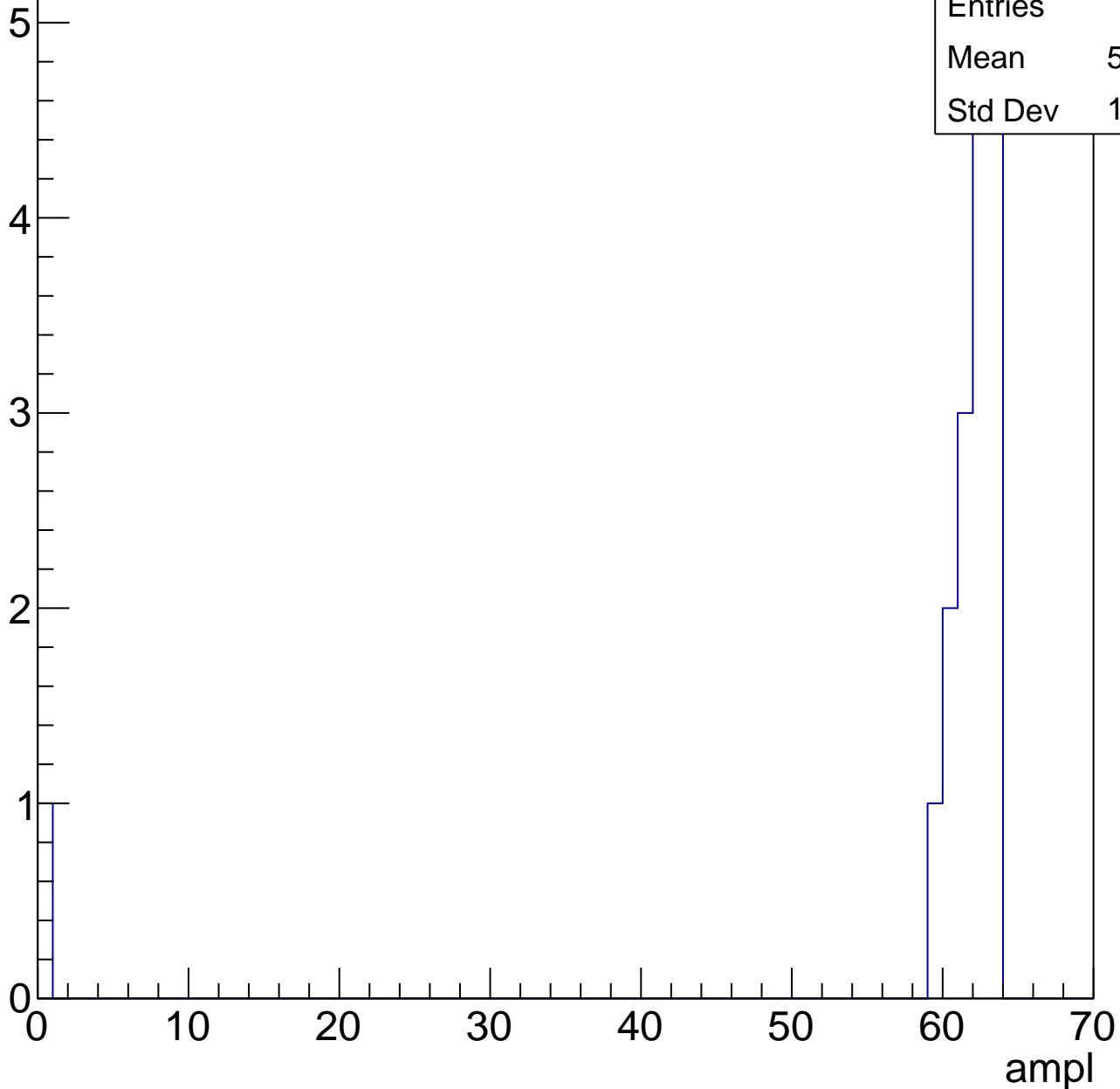


# B1L103S, U3-ch72, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	17
Mean	58.06
Std Dev	14.56





# B1L103S, U3-ch72, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch73, adc0

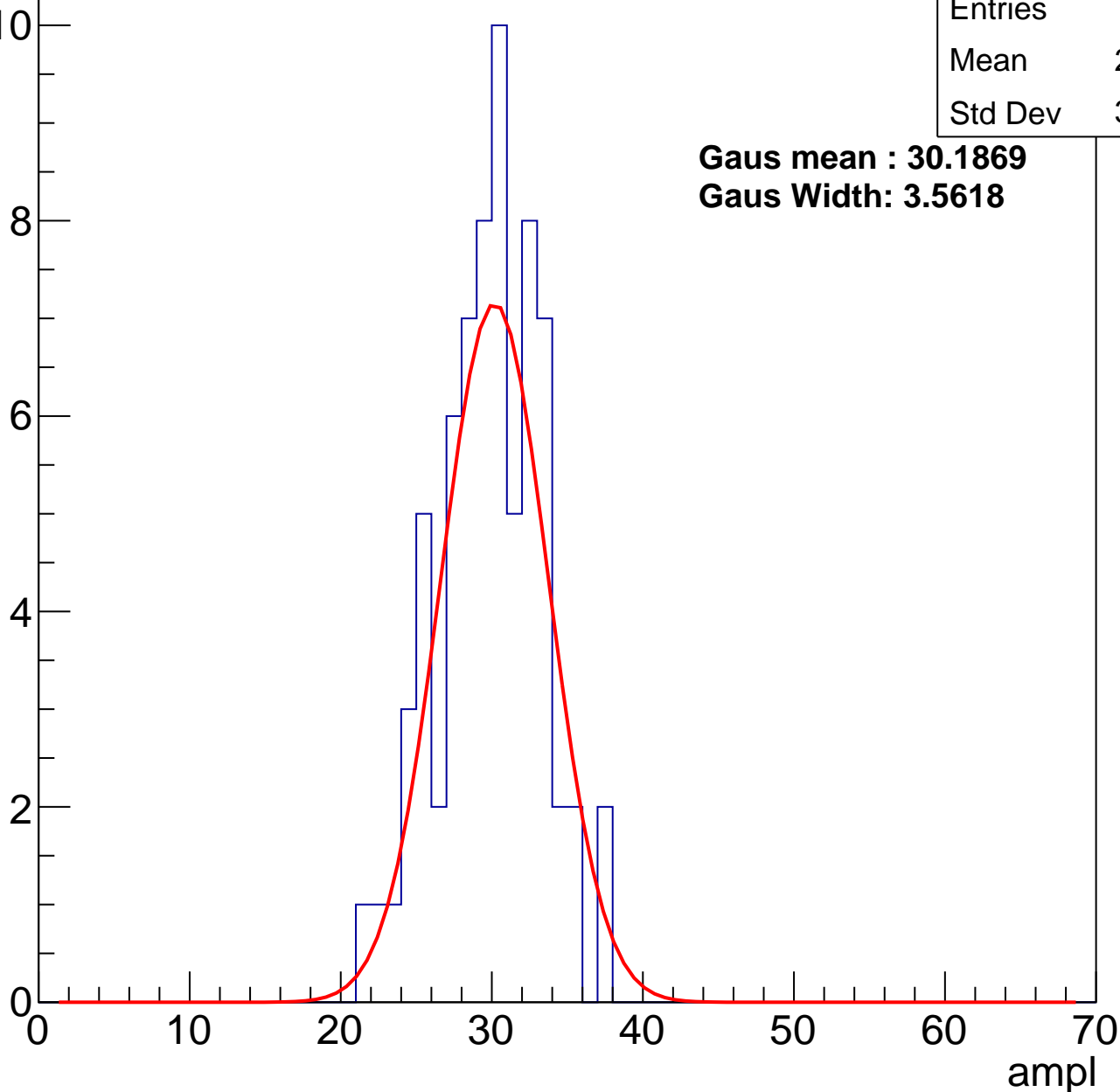
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	29.41
Std Dev	3.391

**Gaus mean : 30.1869**

**Gaus Width: 3.5618**



# B1L103S, U3-ch73, adc1

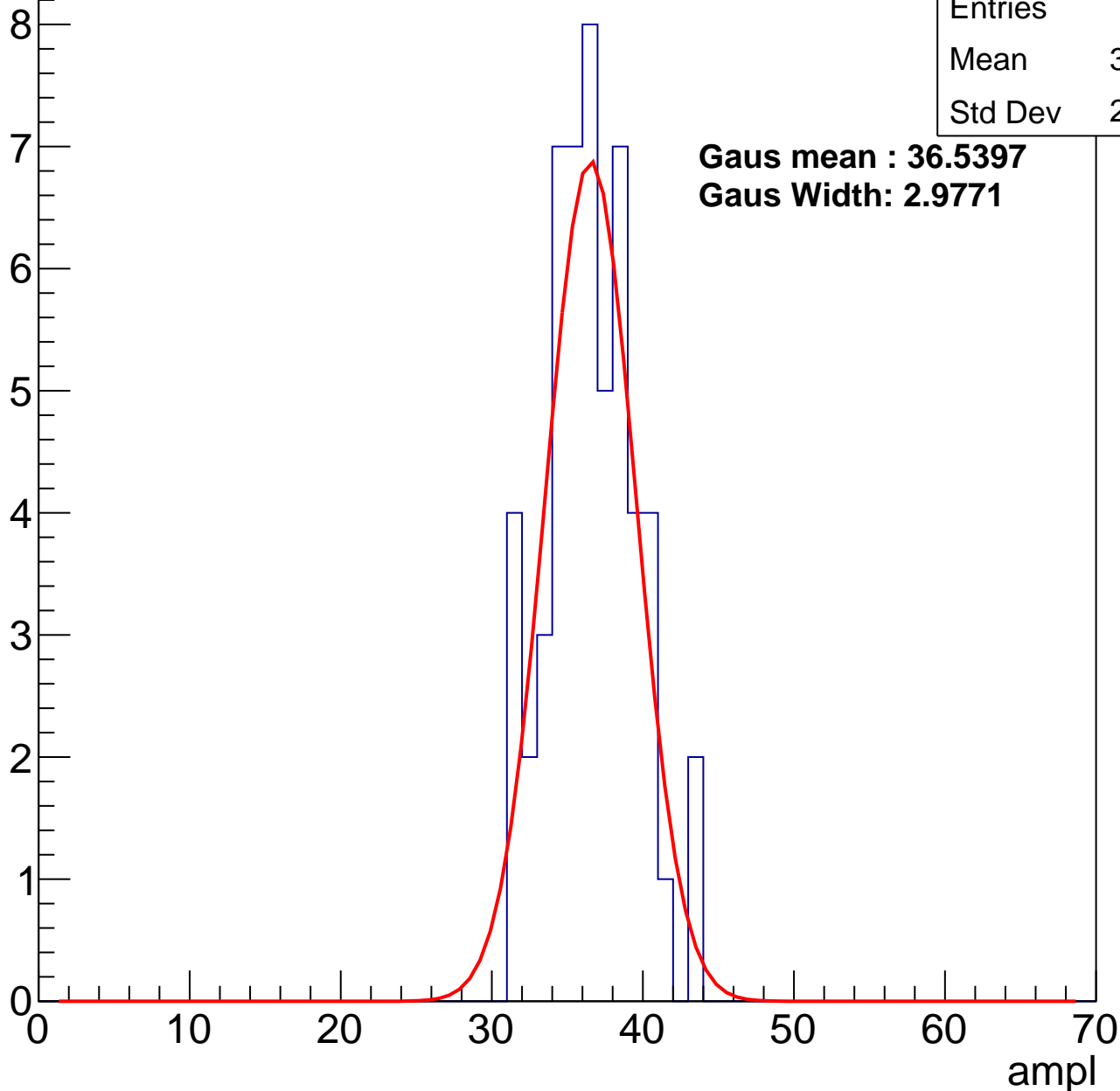
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	36.15
Std Dev	2.883

**Gaus mean : 36.5397**

**Gaus Width: 2.9771**



# B1L103S, U3-ch73, adc2

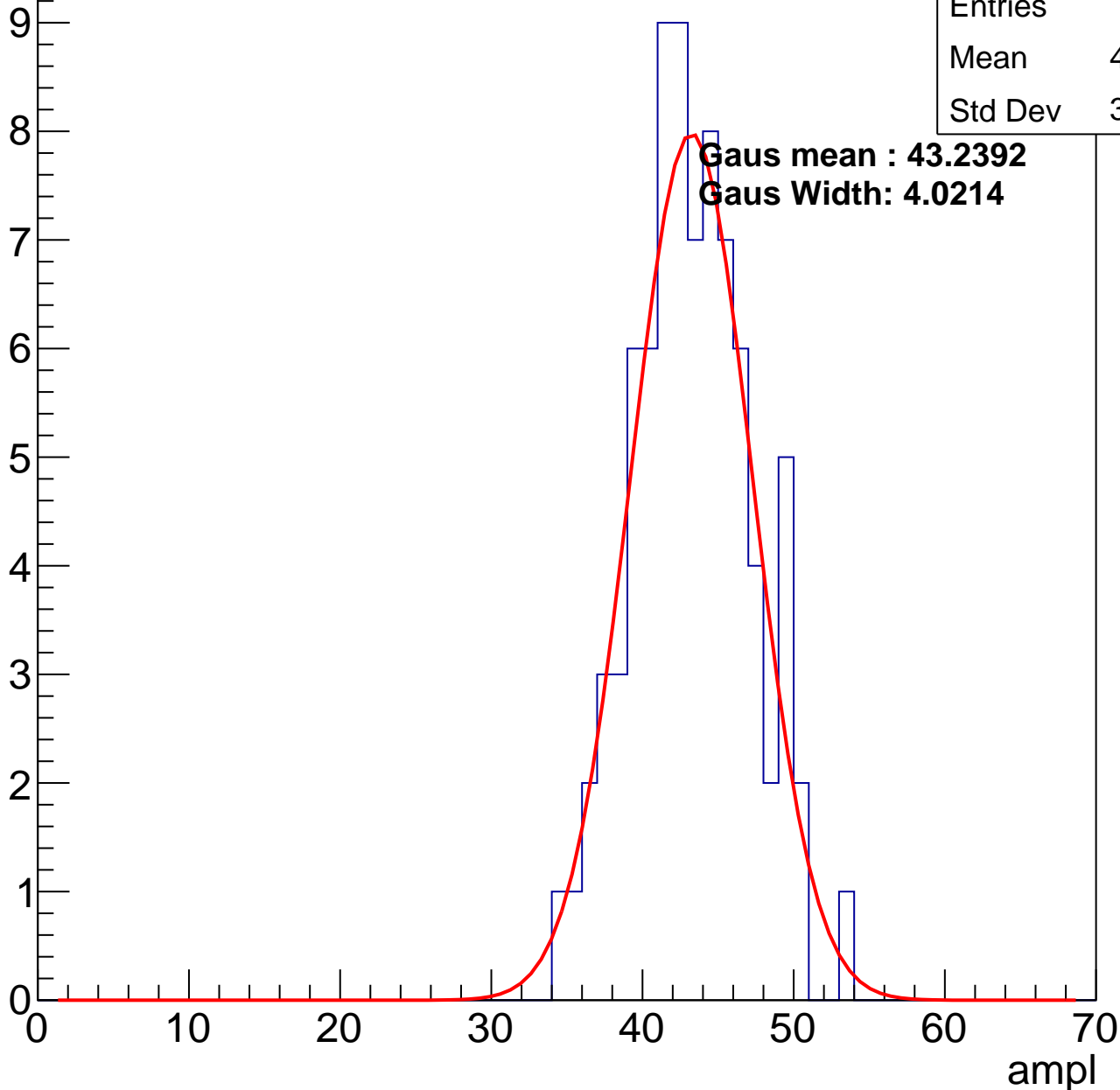
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	82
Mean	42.84
Std Dev	3.827

**Gaus mean : 43.2392**

**Gaus Width: 4.0214**

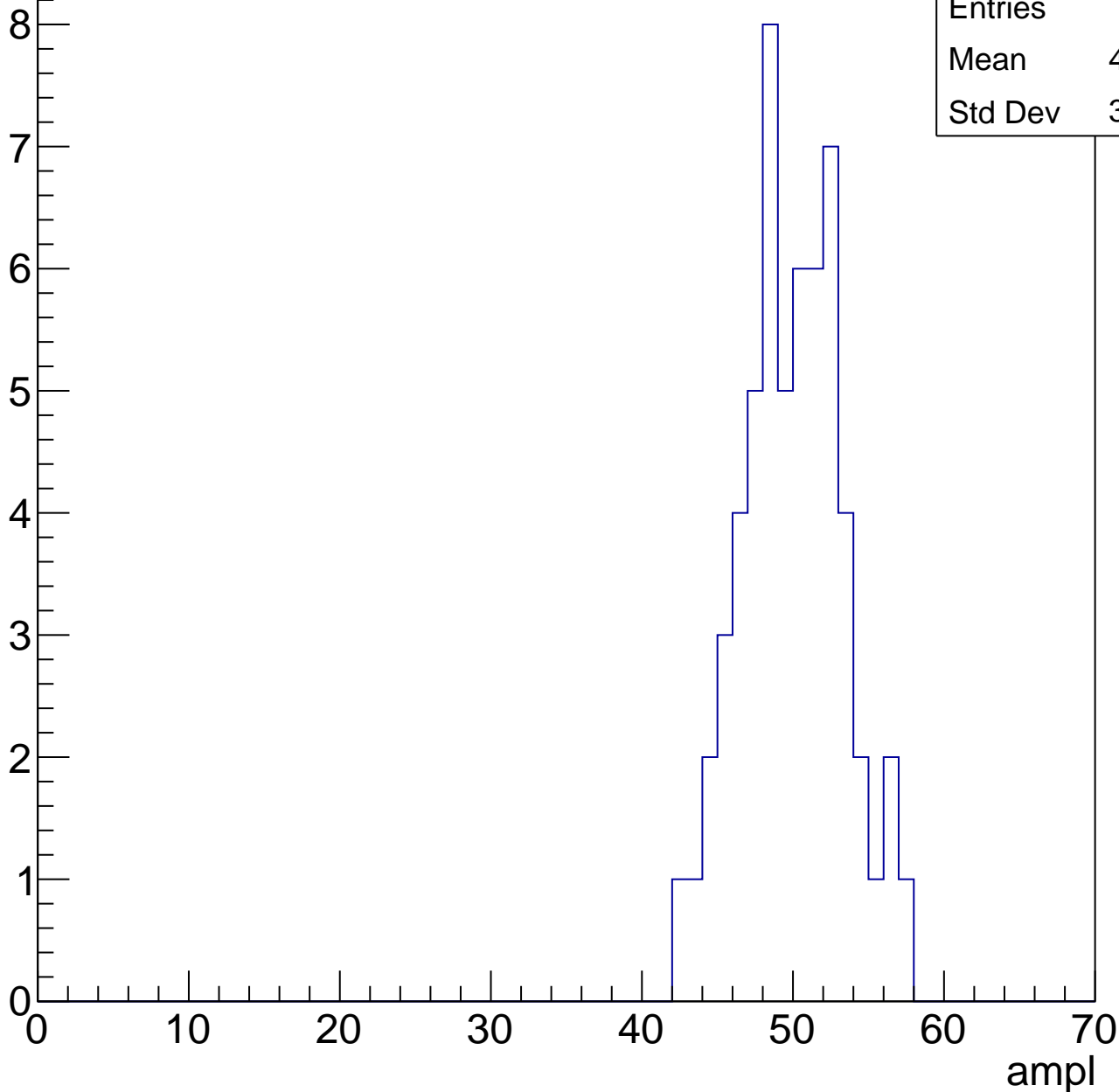


# B1L103S, U3-ch73, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

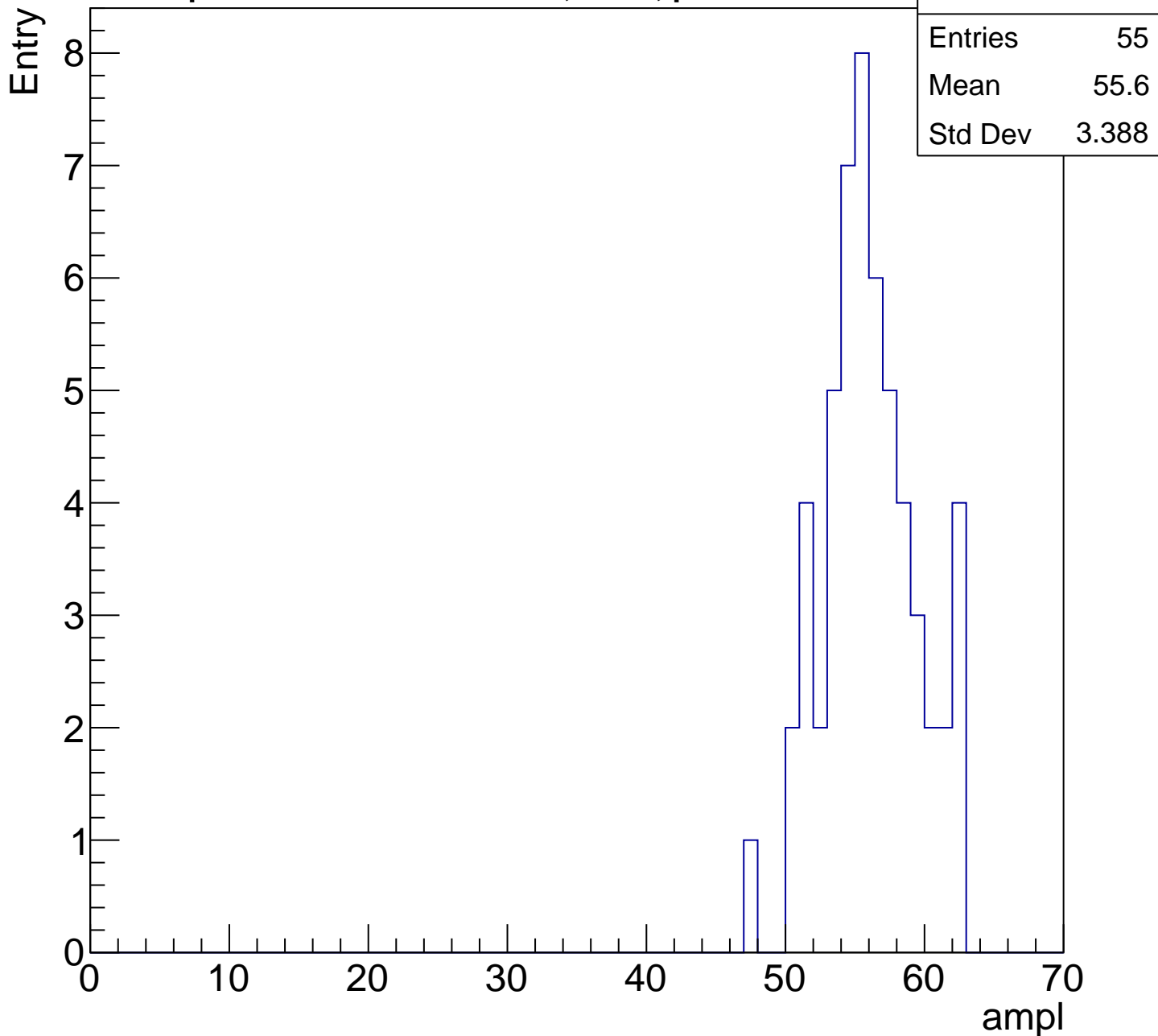
Entry

Entries	58
Mean	49.48
Std Dev	3.318



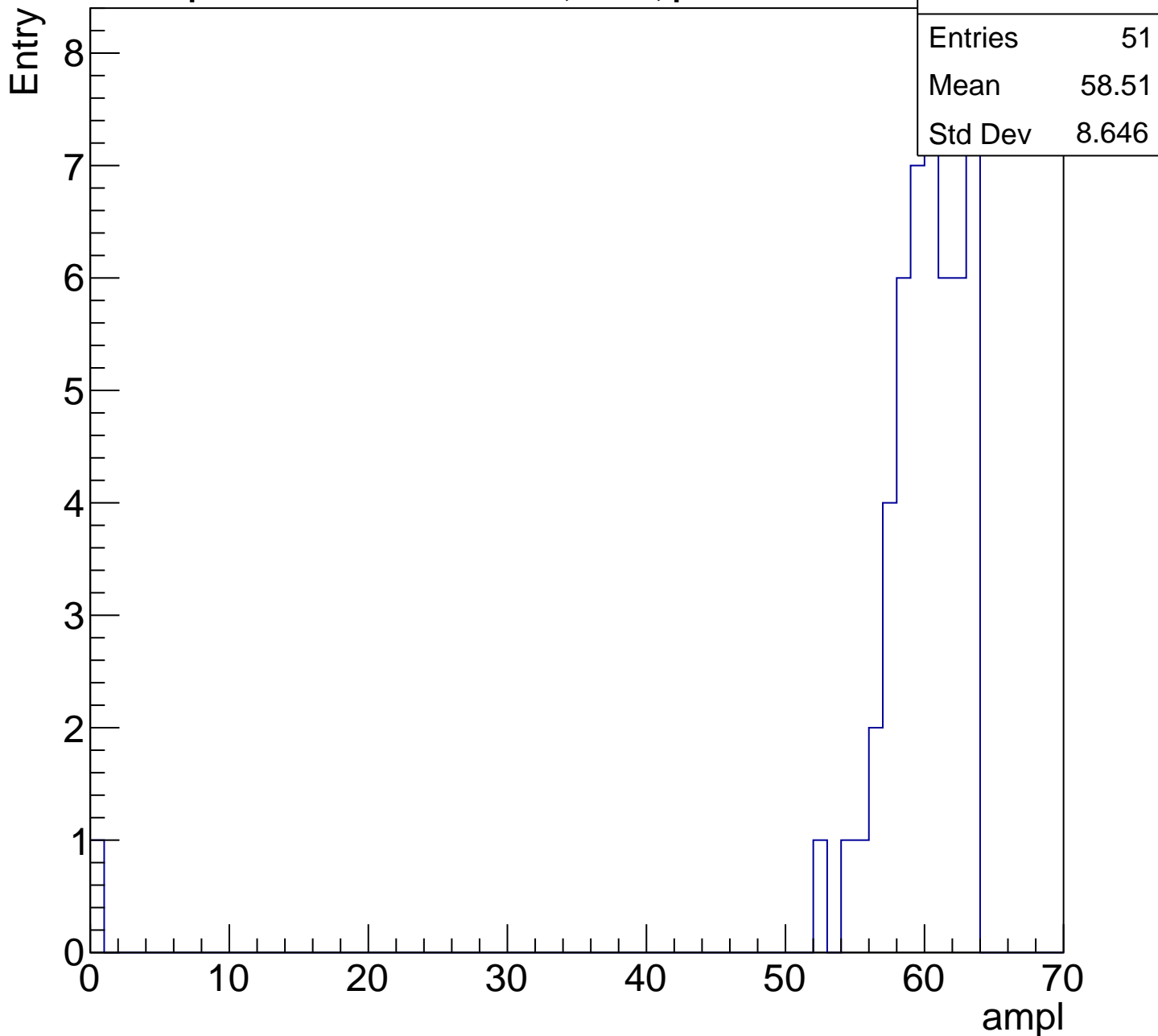
# B1L103S, U3-ch73, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U3-ch73, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U3-ch73, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U3-ch73, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch74, adc0

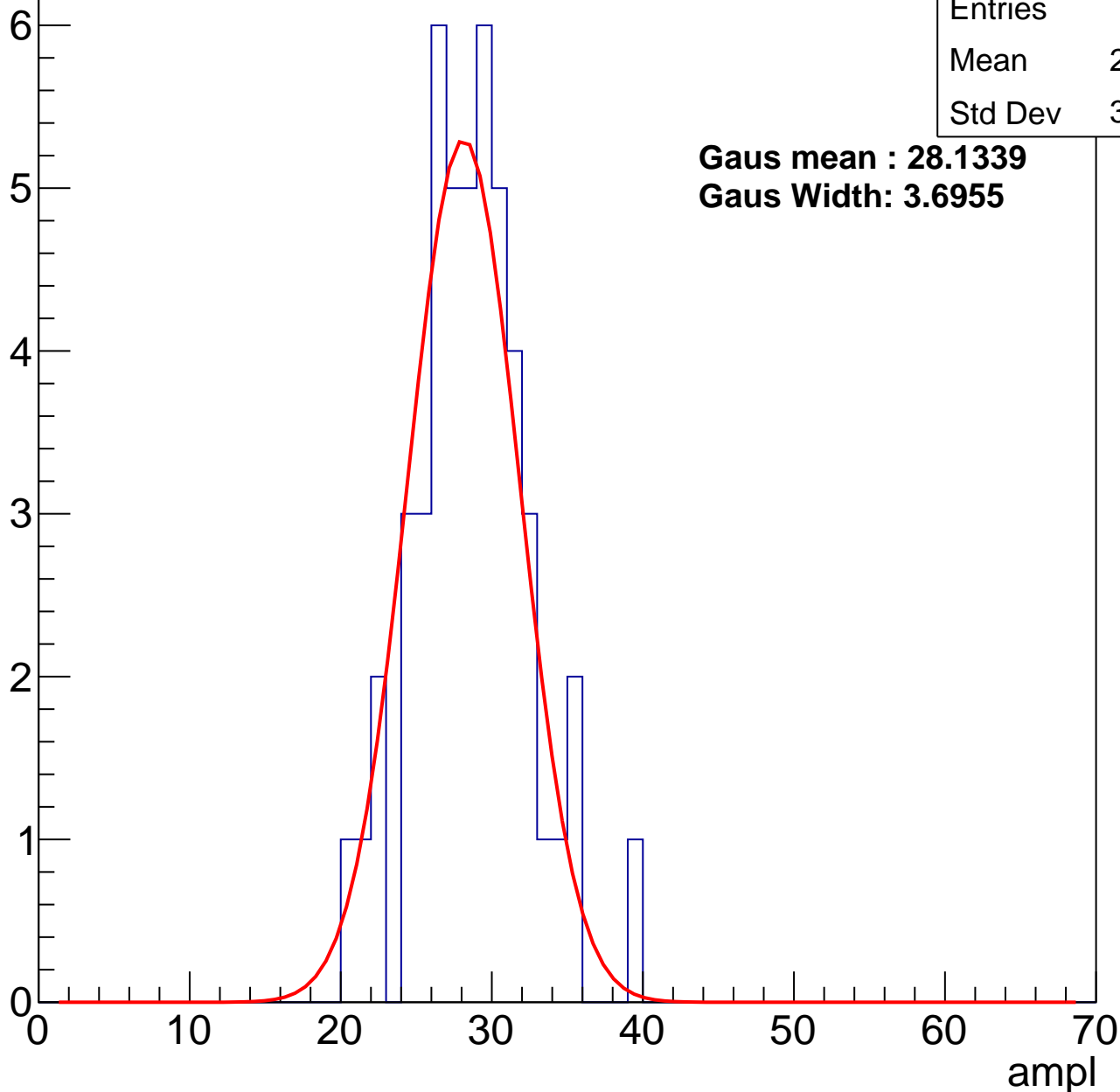
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	28.22
Std Dev	3.716

**Gaus mean : 28.1339**

**Gaus Width: 3.6955**



# B1L103S, U3-ch74, adc1

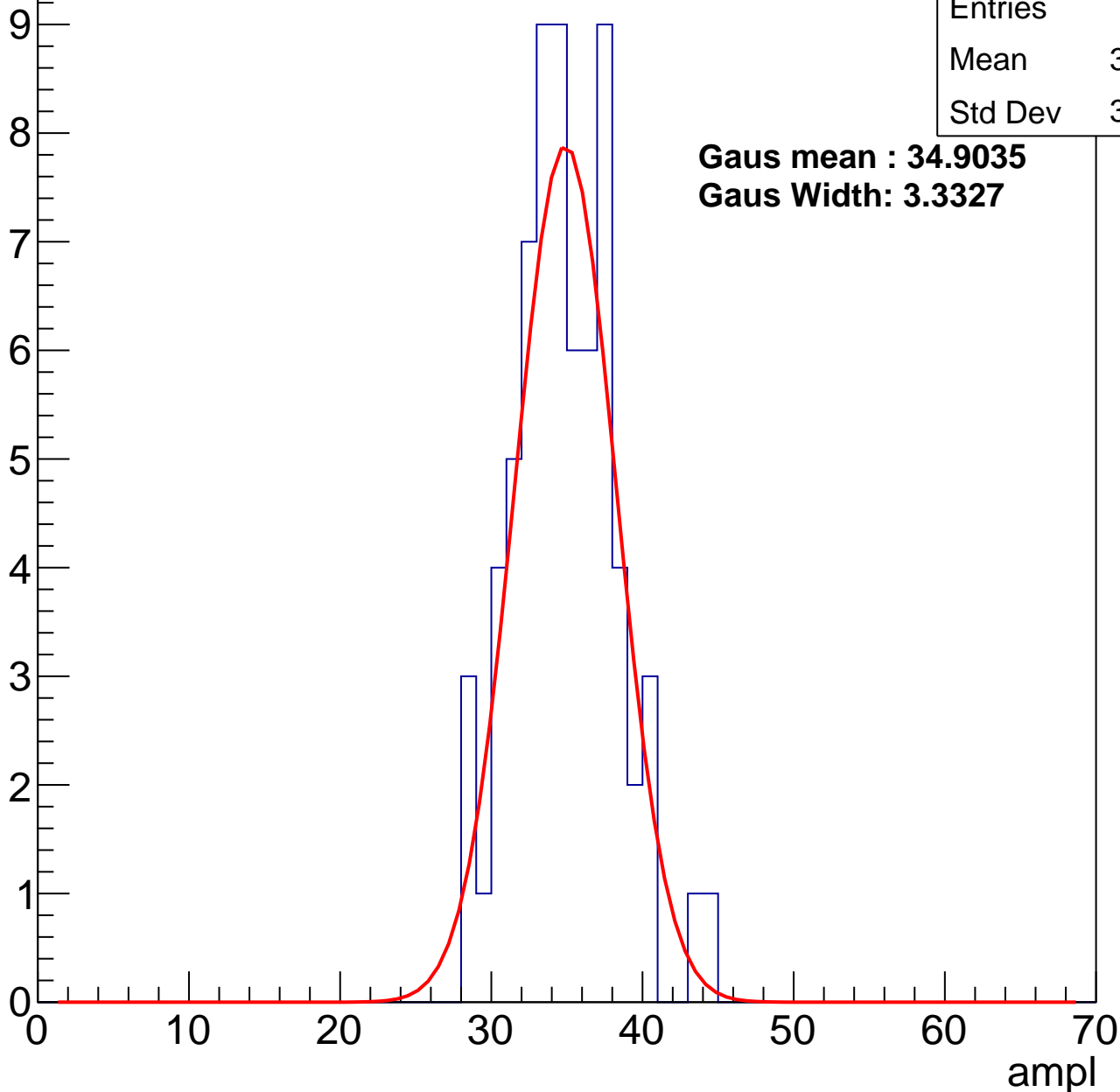
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	34.44
Std Dev	3.337

**Gaus mean : 34.9035**

**Gaus Width: 3.3327**



# B1L103S, U3-ch74, adc2

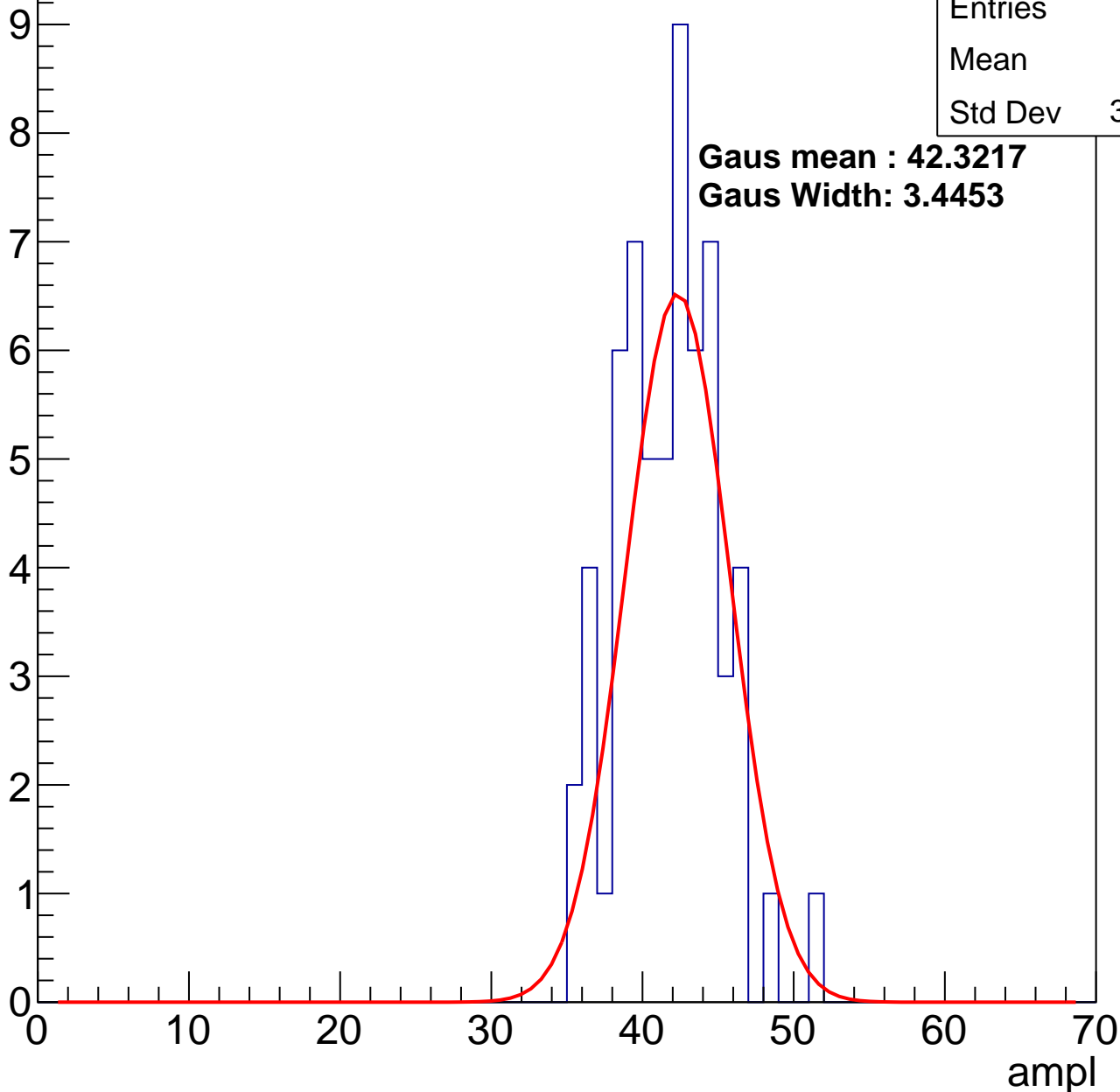
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	41.3
Std Dev	3.296

**Gaus mean : 42.3217**

**Gaus Width: 3.4453**

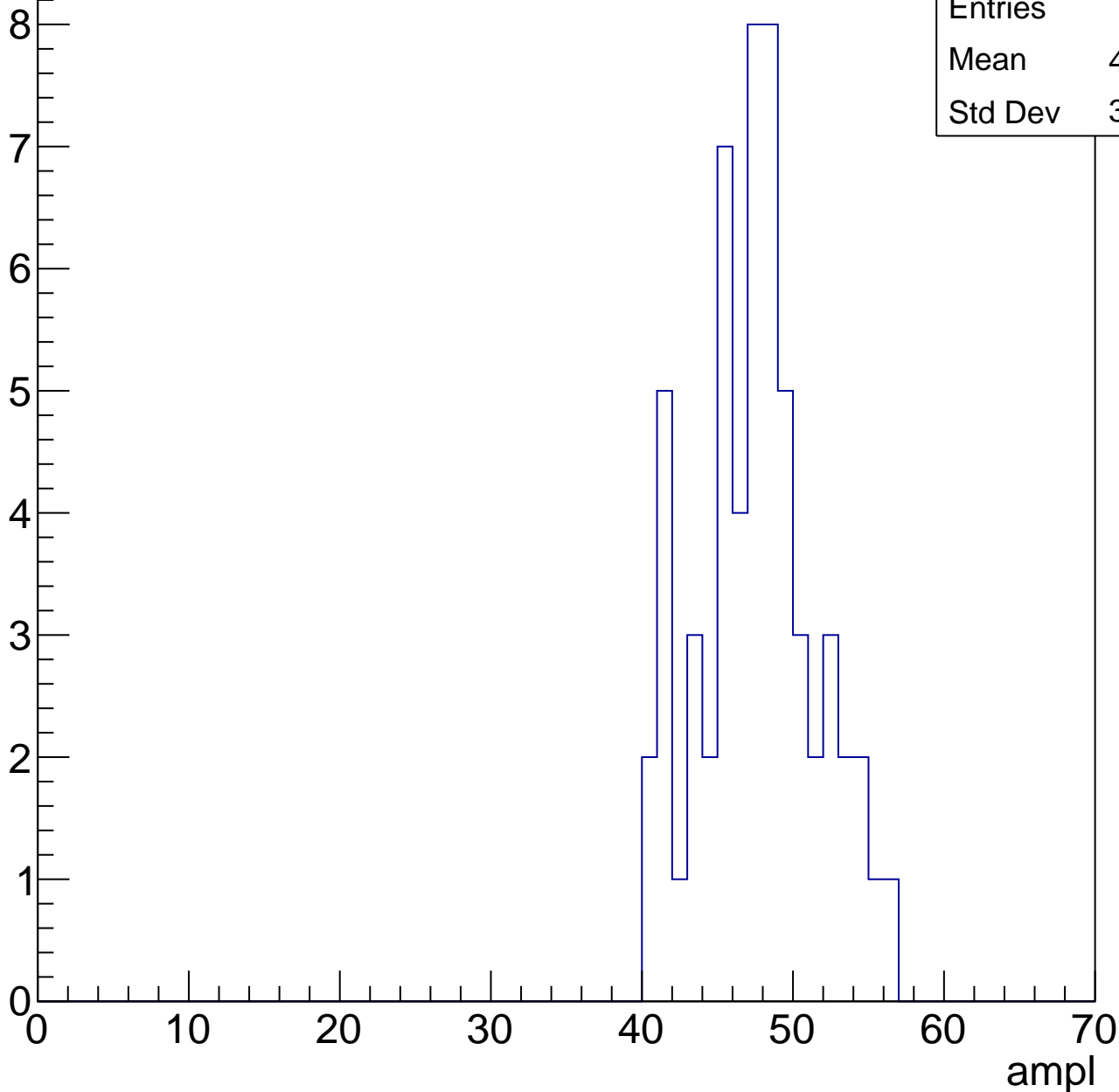


# B1L103S, U3-ch74, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

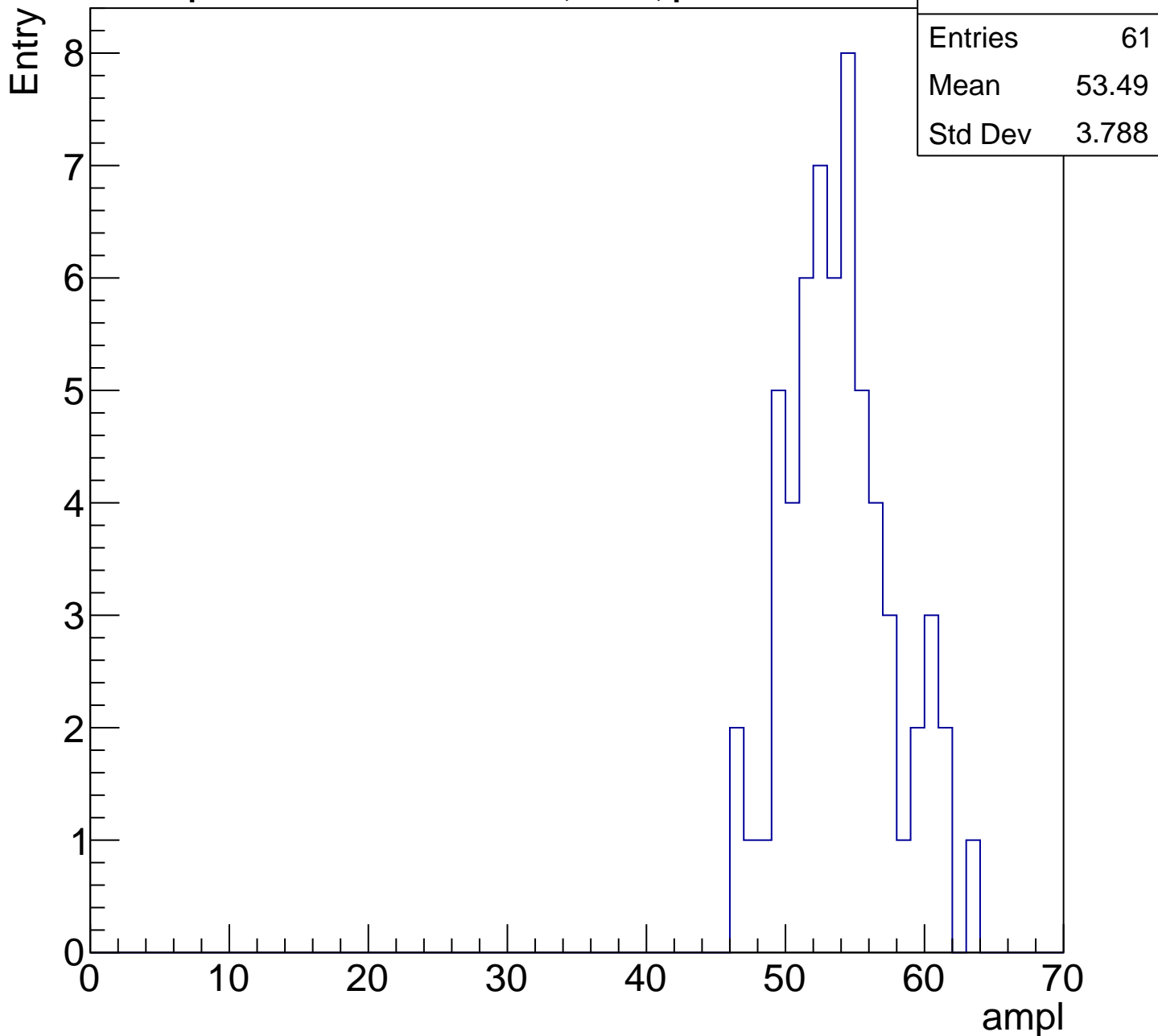
Entry

Entries	59
Mean	47.14
Std Dev	3.855



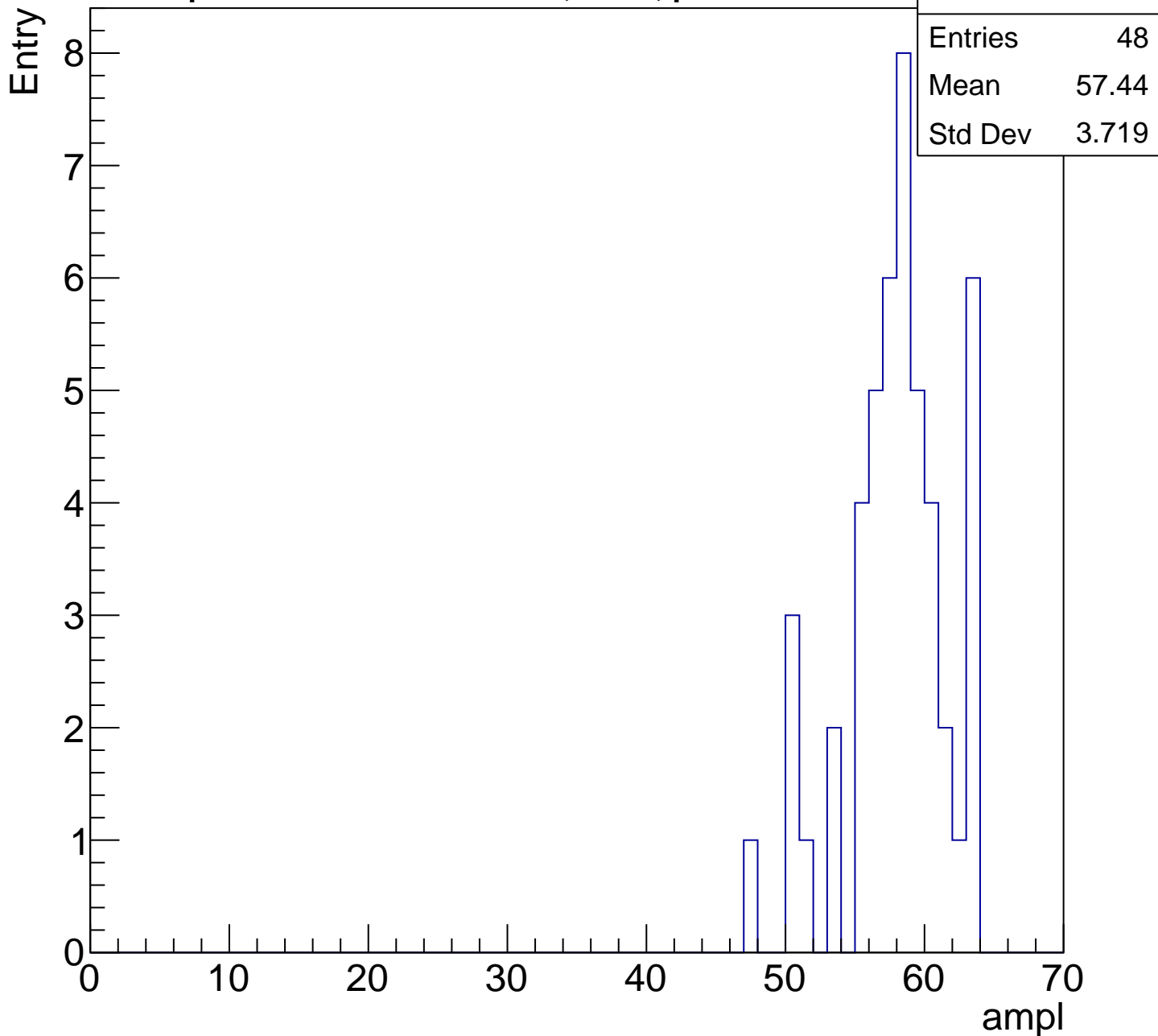
# B1L103S, U3-ch74, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U3-ch74, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

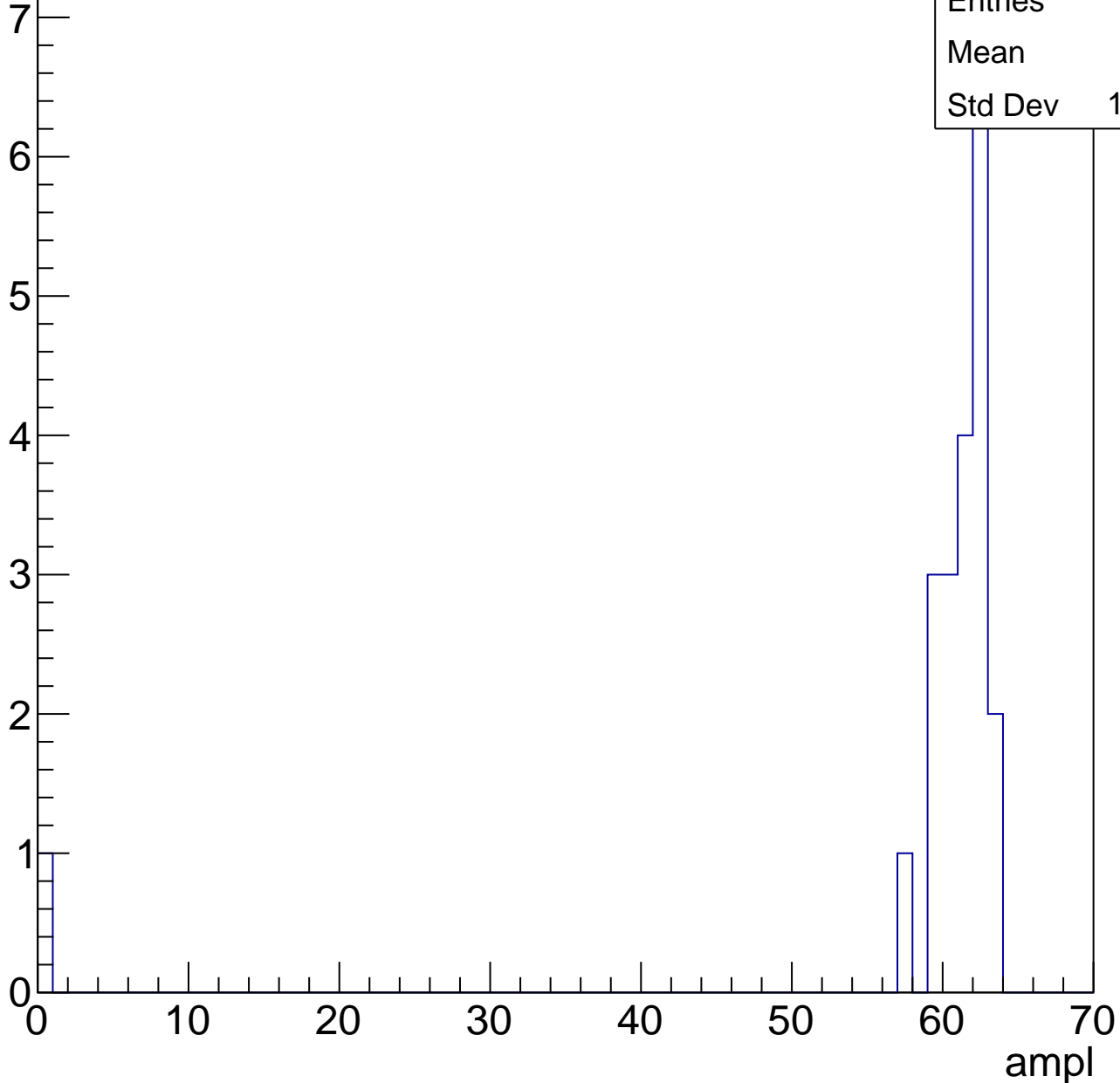


# B1L103S, U3-ch74, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	21
Mean	58
Std Dev	13.05

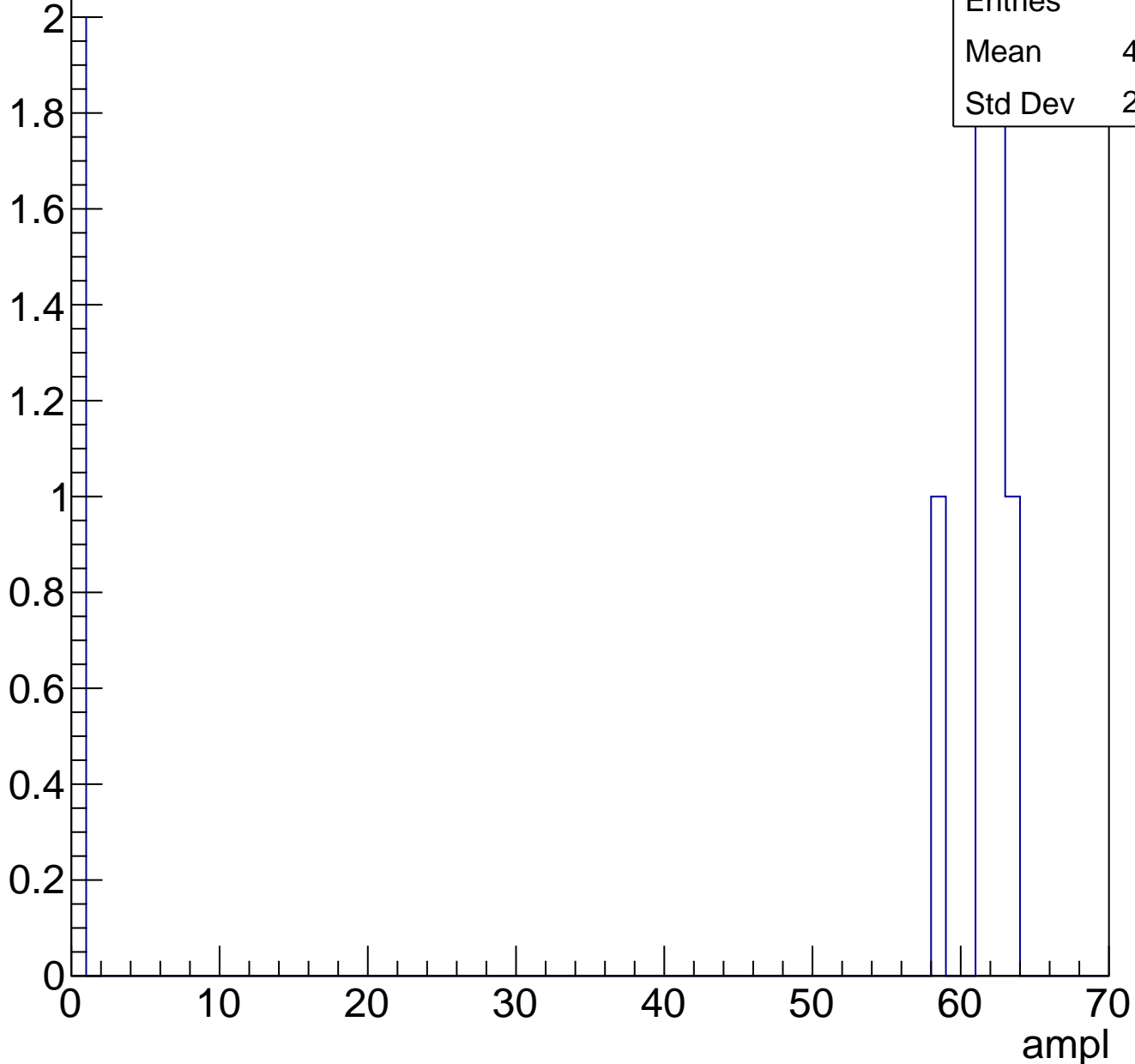




# B1L103S, U3-ch74, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	8
Mean	45.88
Std Dev	26.52

# B1L103S, U3-ch75, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	71
Mean	26.31
Std Dev	6.499

**Gaus mean : 27.4403**

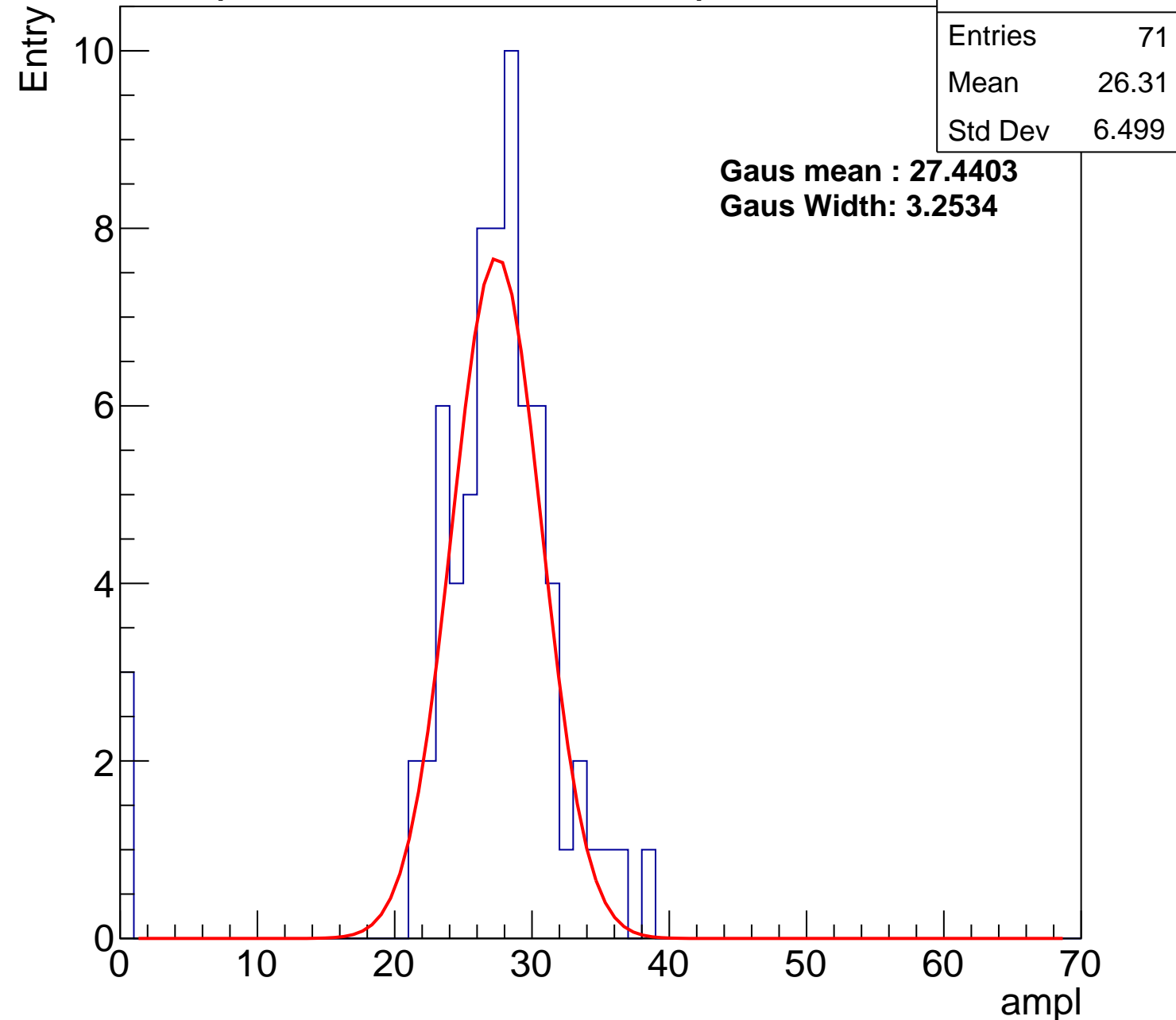
**Gaus Width: 3.2534**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U3-ch75, adc1

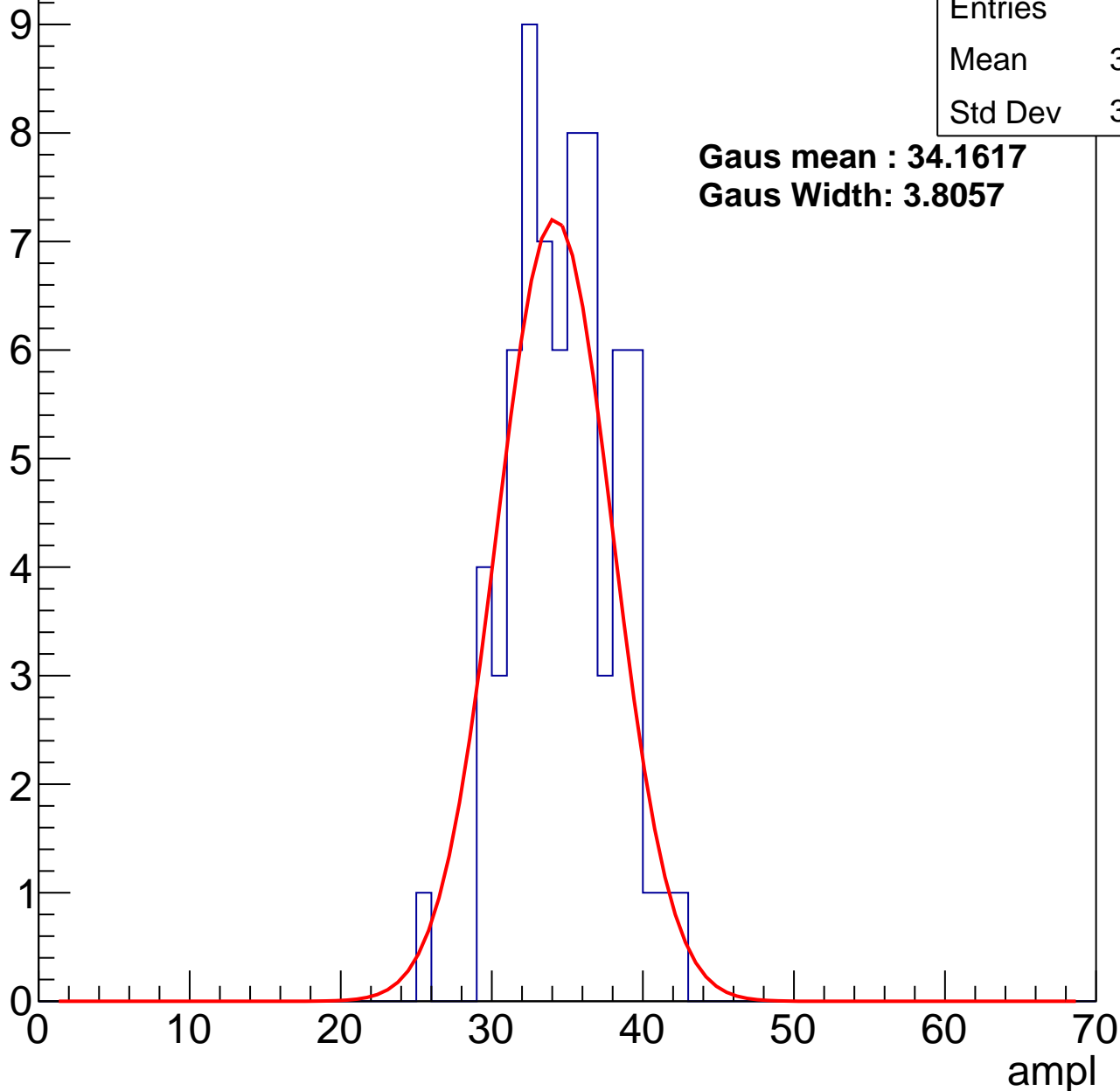
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	34.34
Std Dev	3.338

**Gaus mean : 34.1617**

**Gaus Width: 3.8057**



# B1L103S, U3-ch75, adc2

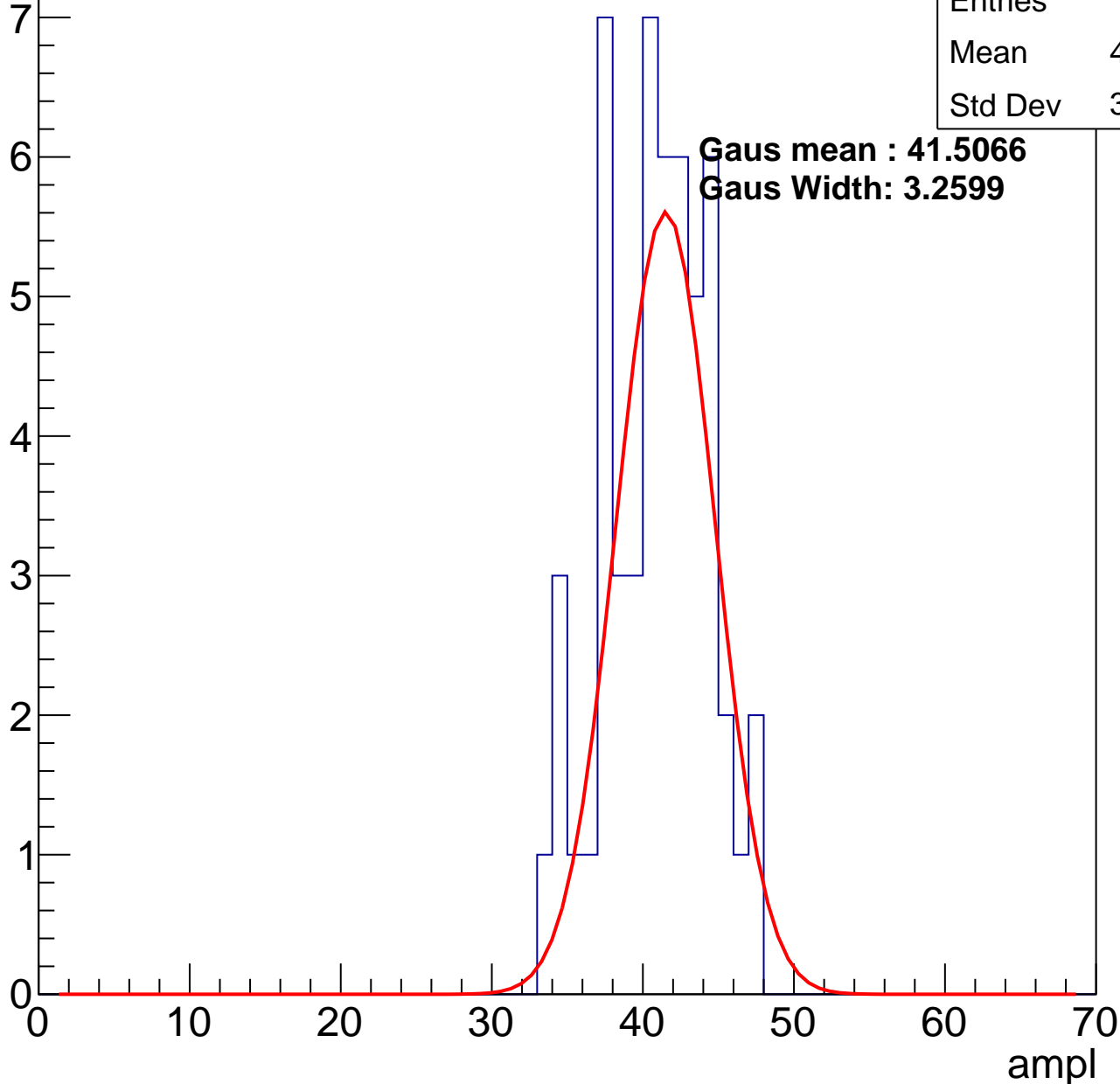
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	40.43
Std Dev	3.392

**Gaus mean : 41.5066**

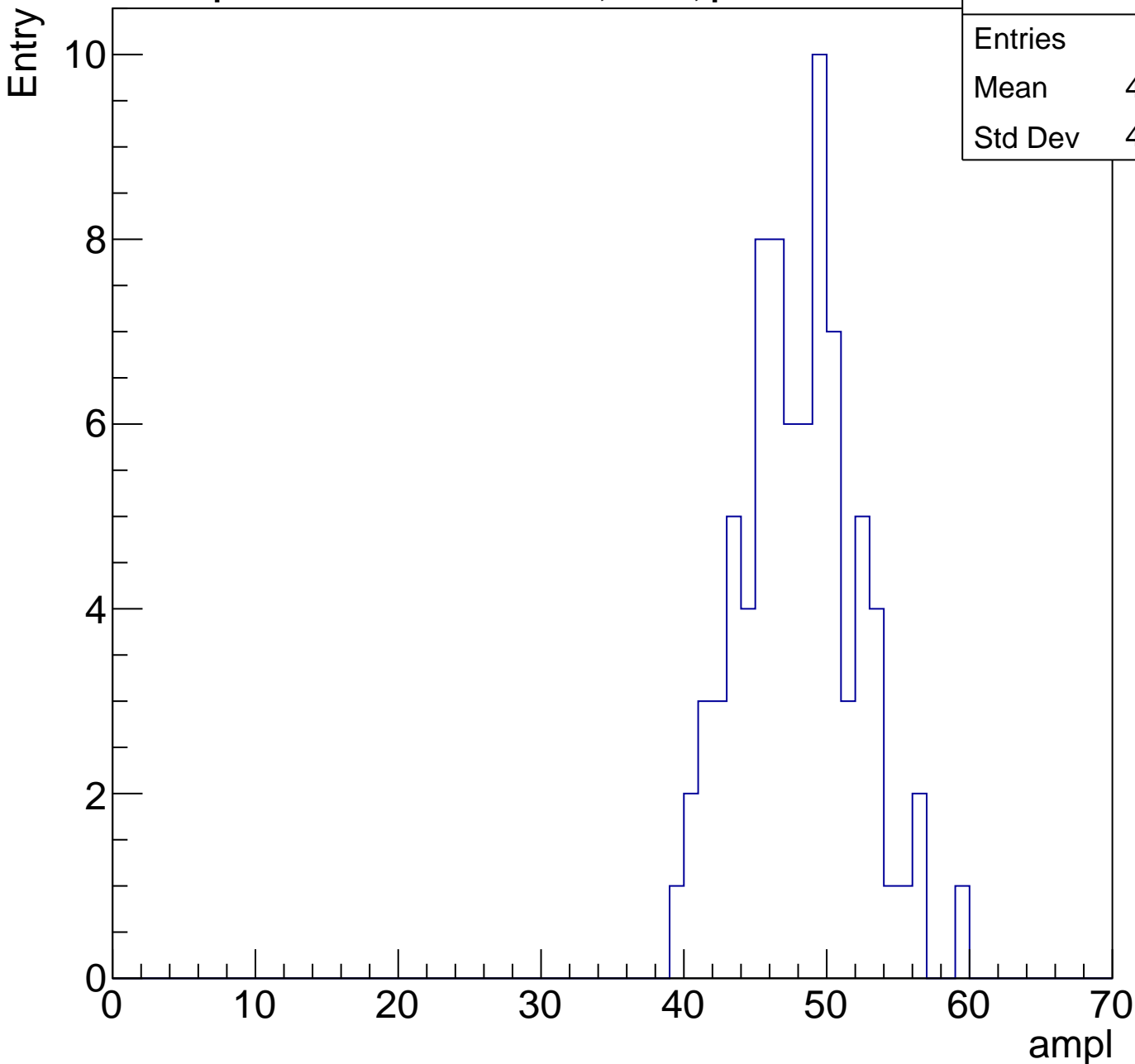
**Gaus Width: 3.2599**



# B1L103S, U3-ch75, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	80
Mean	47.52
Std Dev	4.068

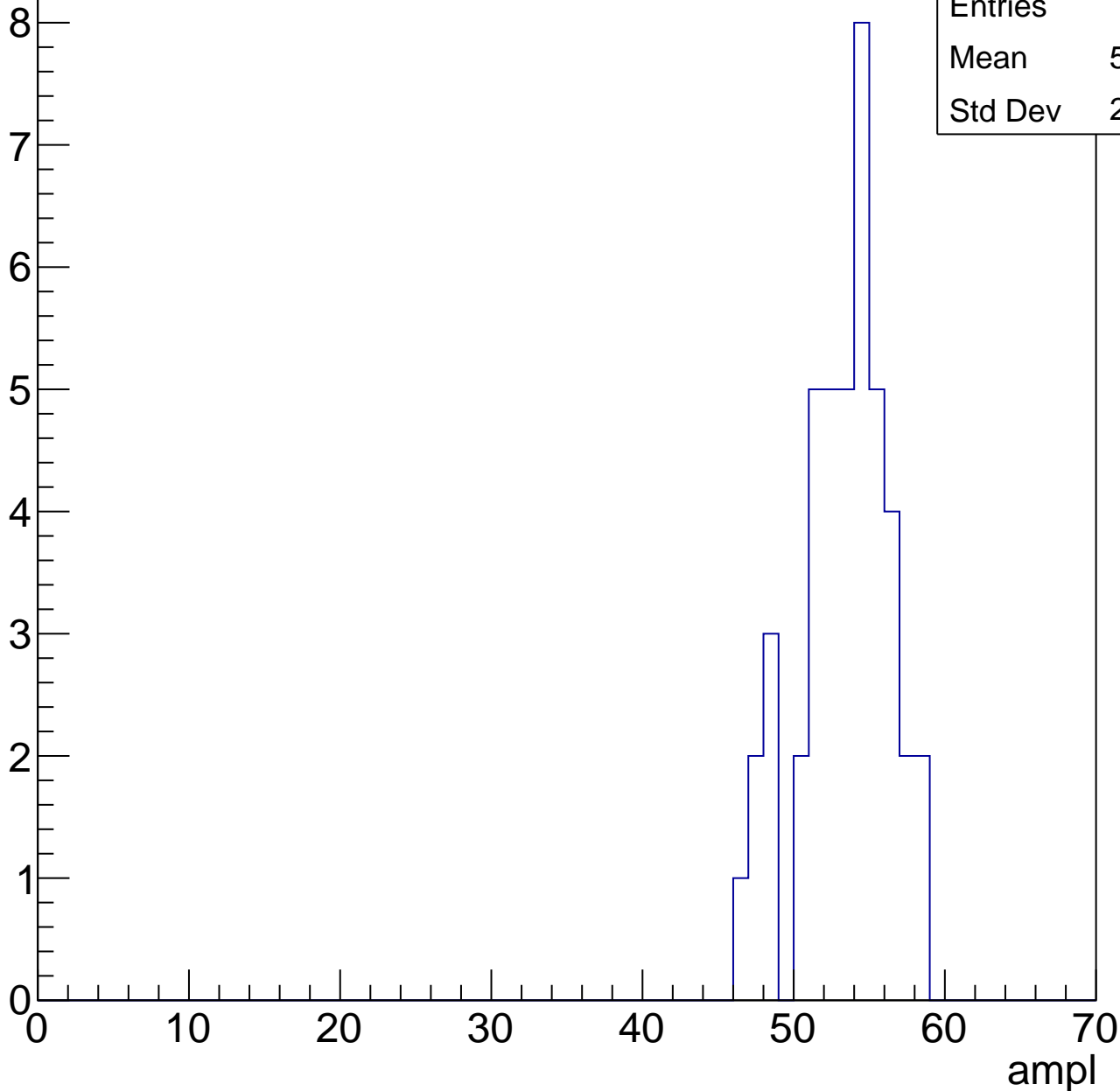


# B1L103S, U3-ch75, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

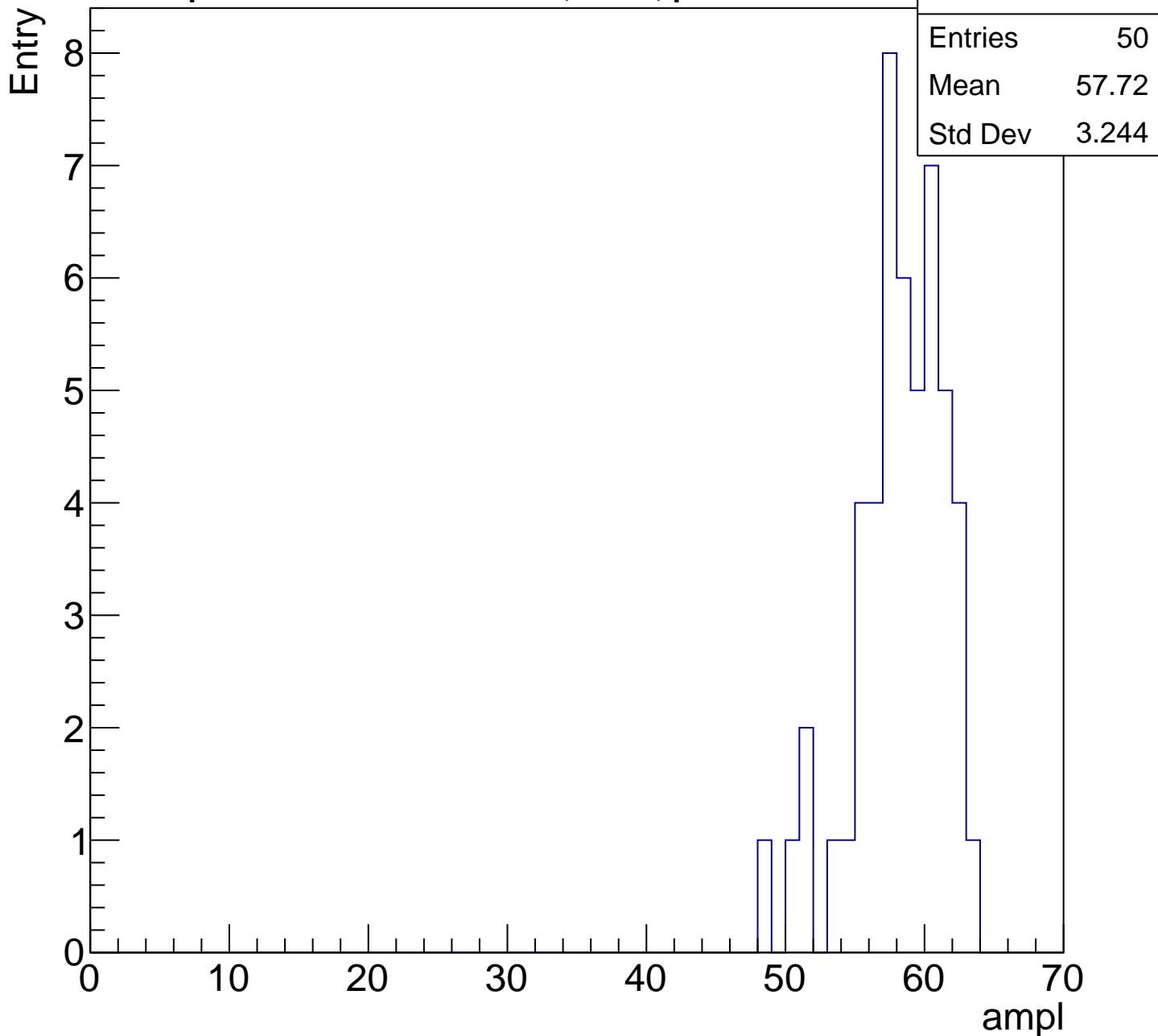
Entry

Entries	44
Mean	52.84
Std Dev	2.954



# B1L103S, U3-ch75, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

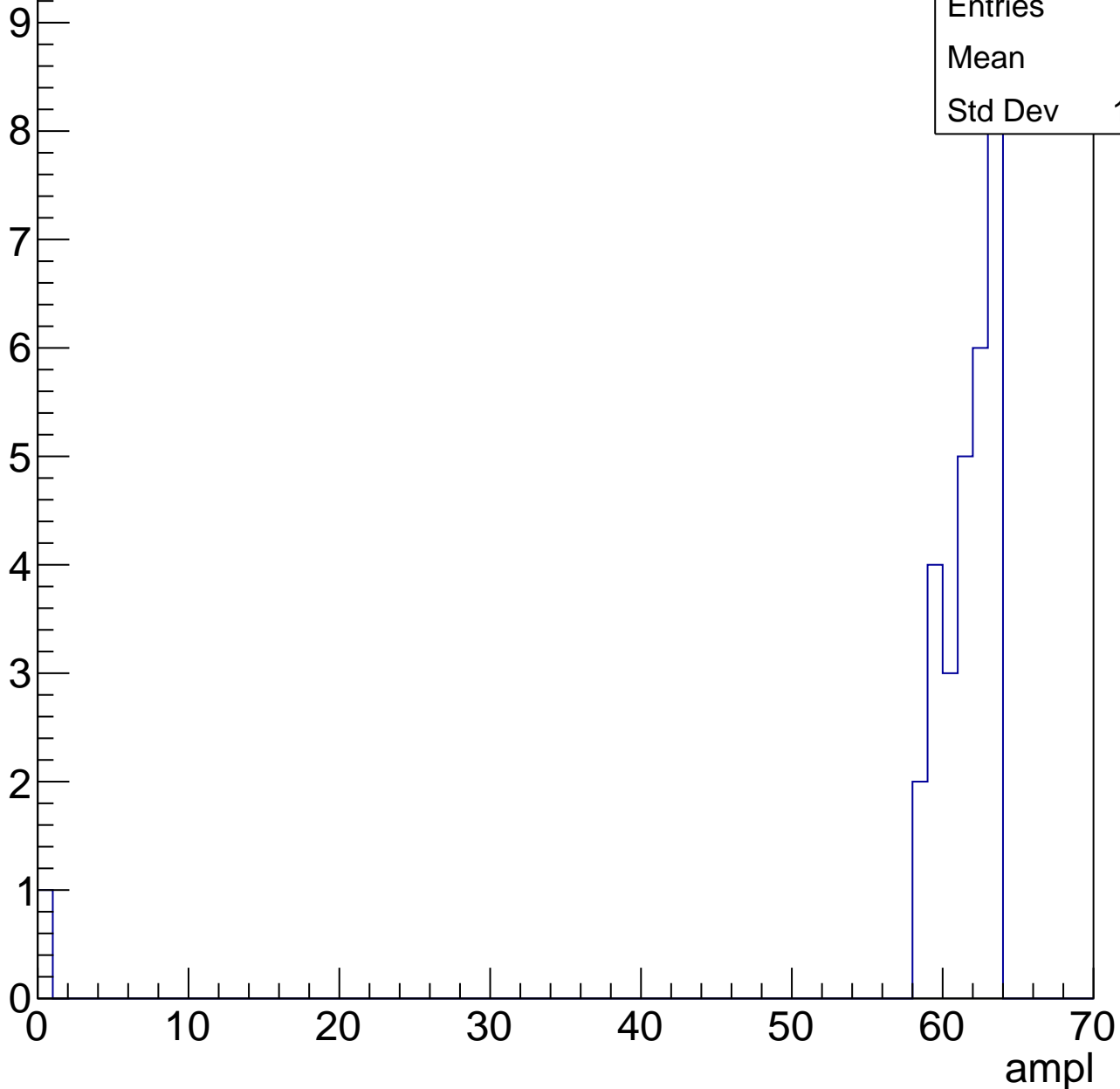


# B1L103S, U3-ch75, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	30
Mean	59.2
Std Dev	11.11





# B1L103S, U3-ch75, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch76, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	65
Mean	28.26
Std Dev	3.08

**Gaus mean : 28.5235**

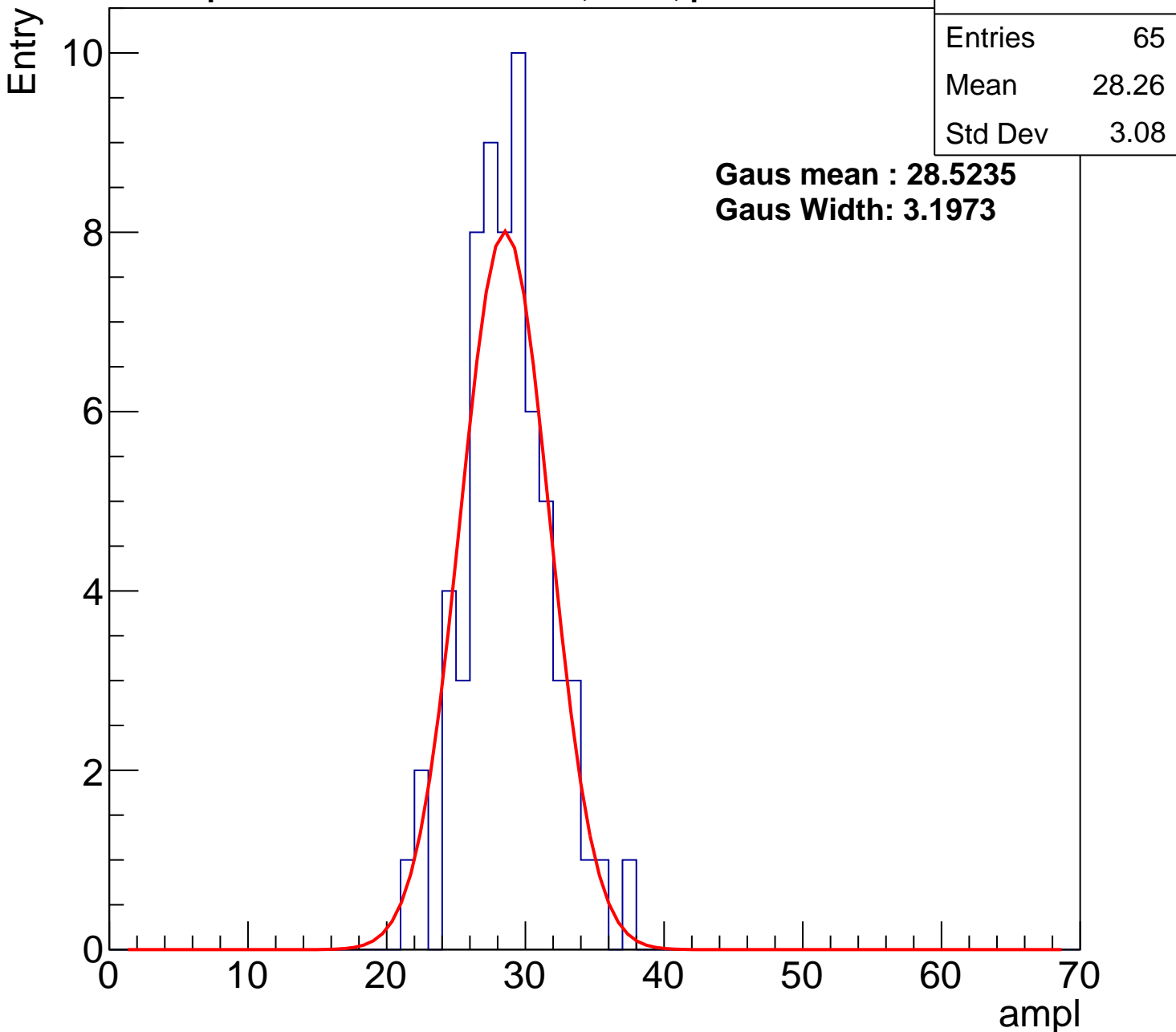
**Gaus Width: 3.1973**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U3-ch76, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	69
Mean	35.42
Std Dev	3.205

**Gaus mean : 35.8443**

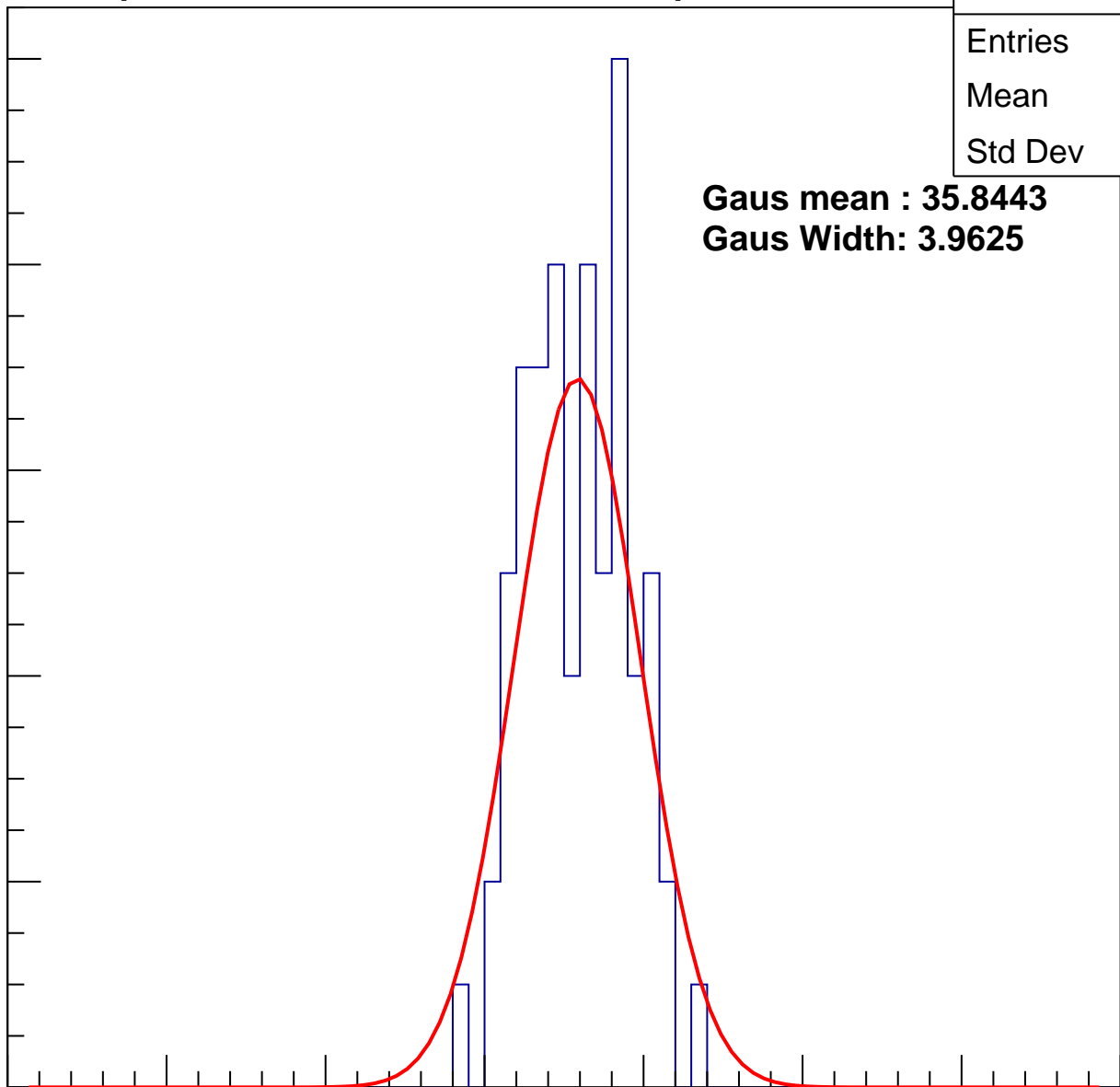
**Gaus Width: 3.9625**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U3-ch76, adc2

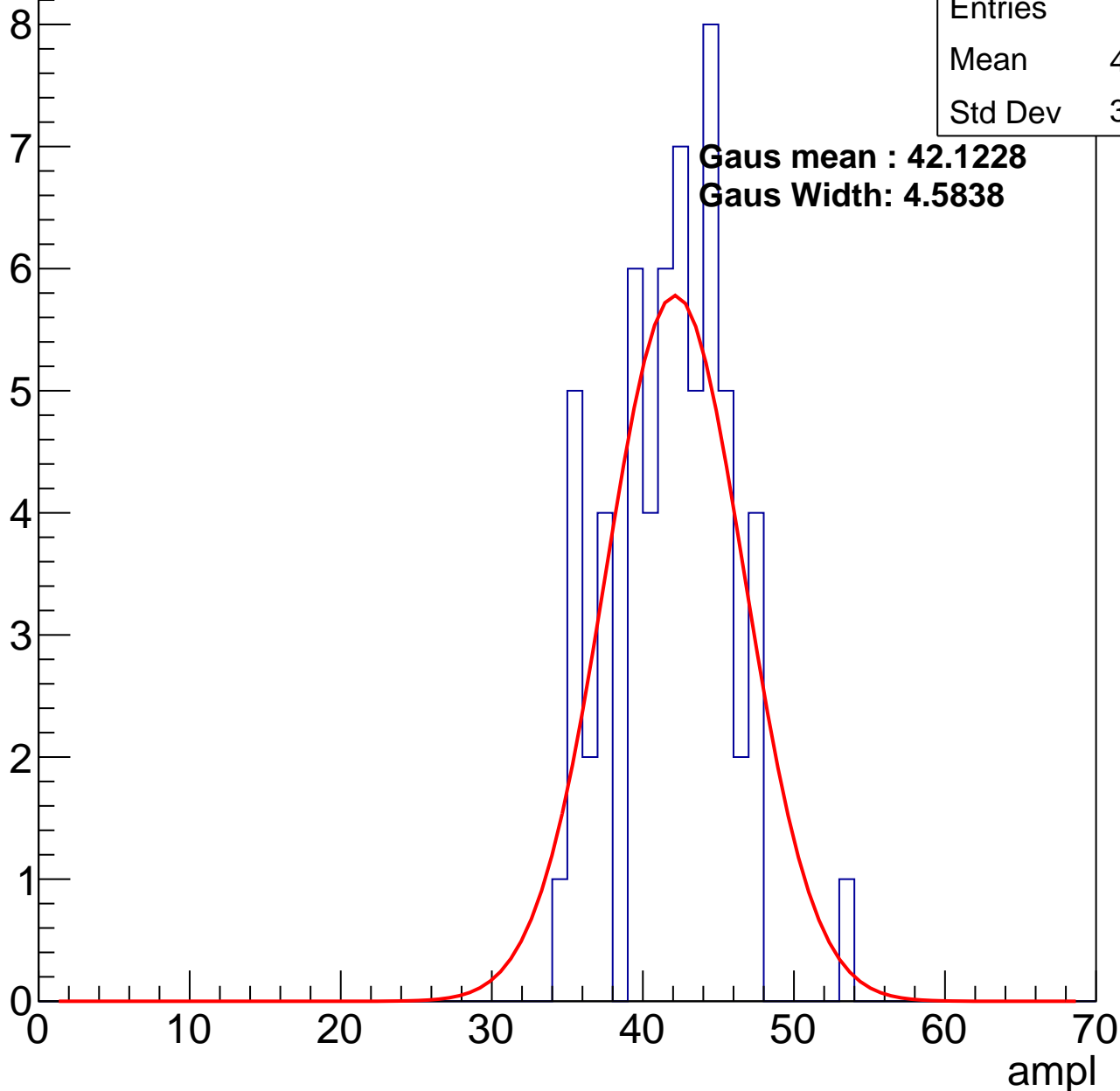
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	41.47
Std Dev	3.819

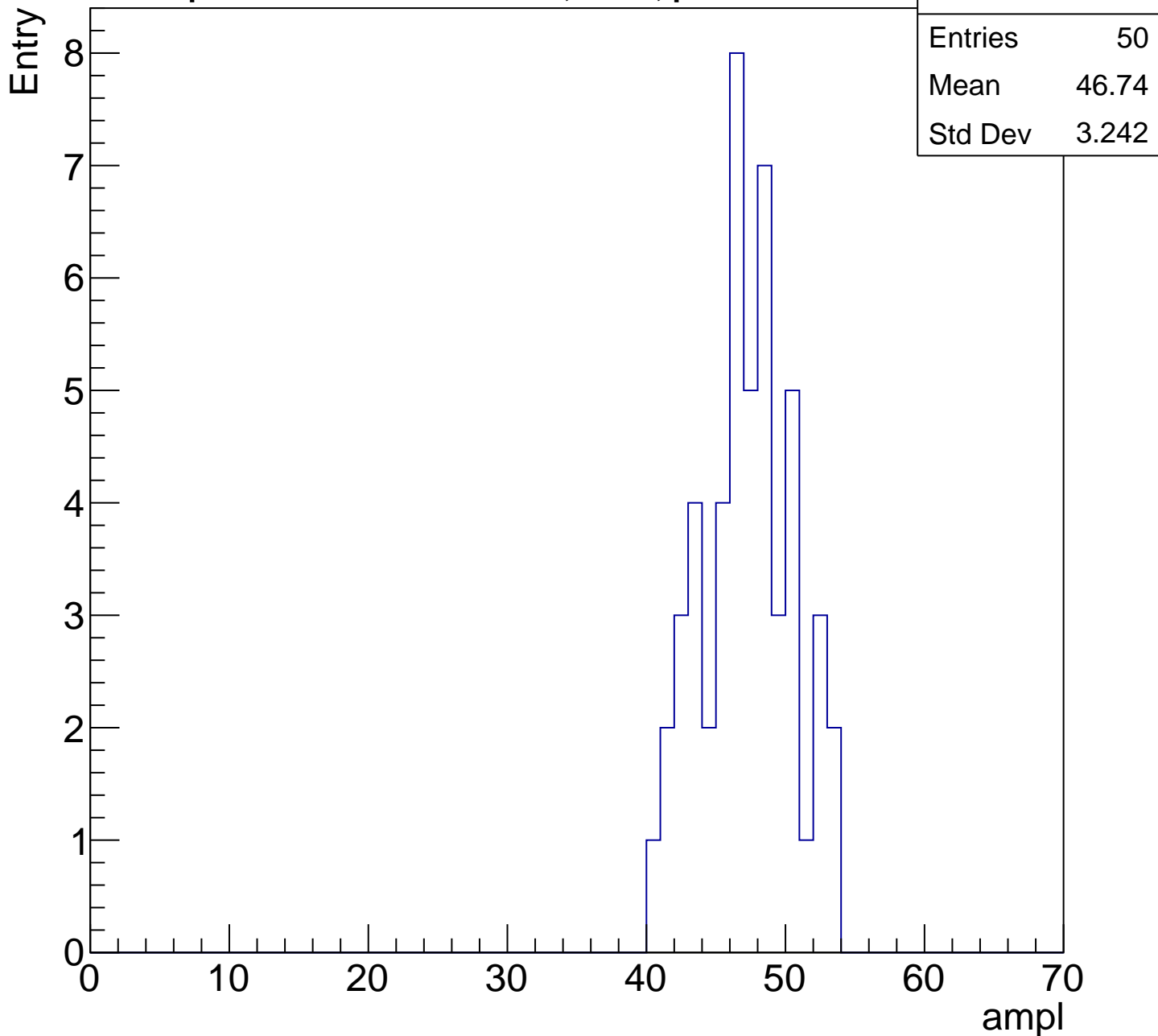
**Gaus mean : 42.1228**

**Gaus Width: 4.5838**



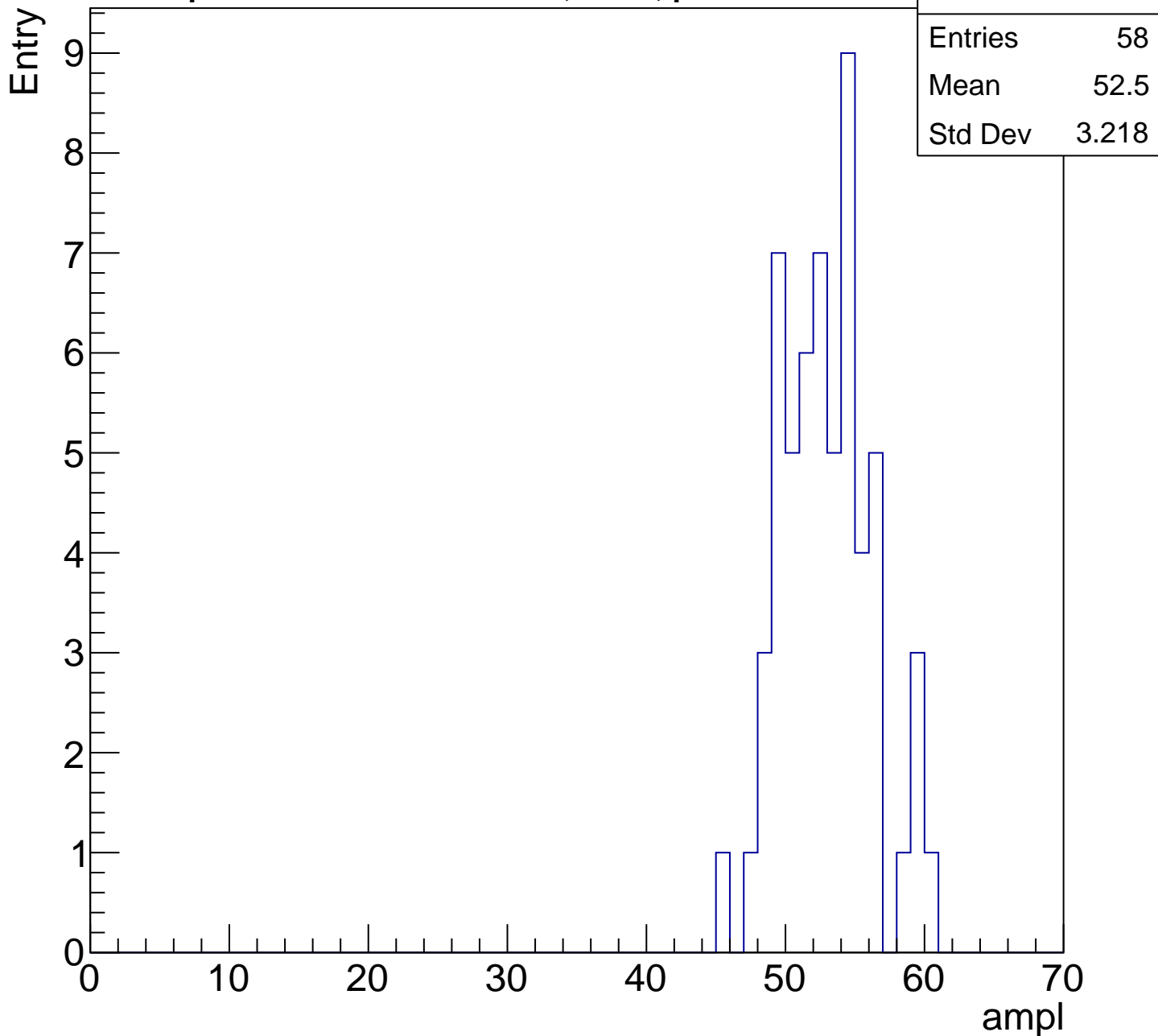
# B1L103S, U3-ch76, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2



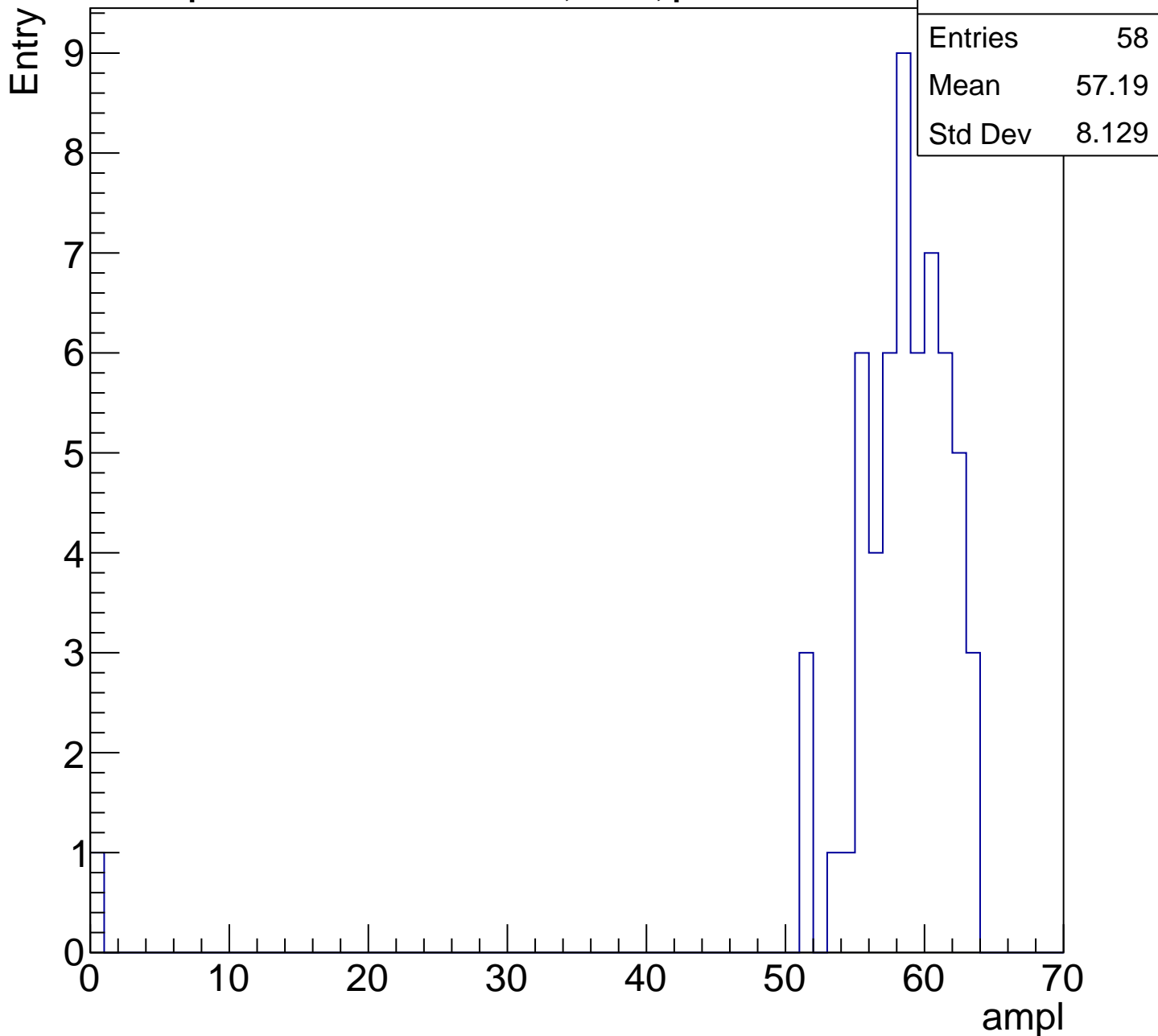
# B1L103S, U3-ch76, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U3-ch76, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

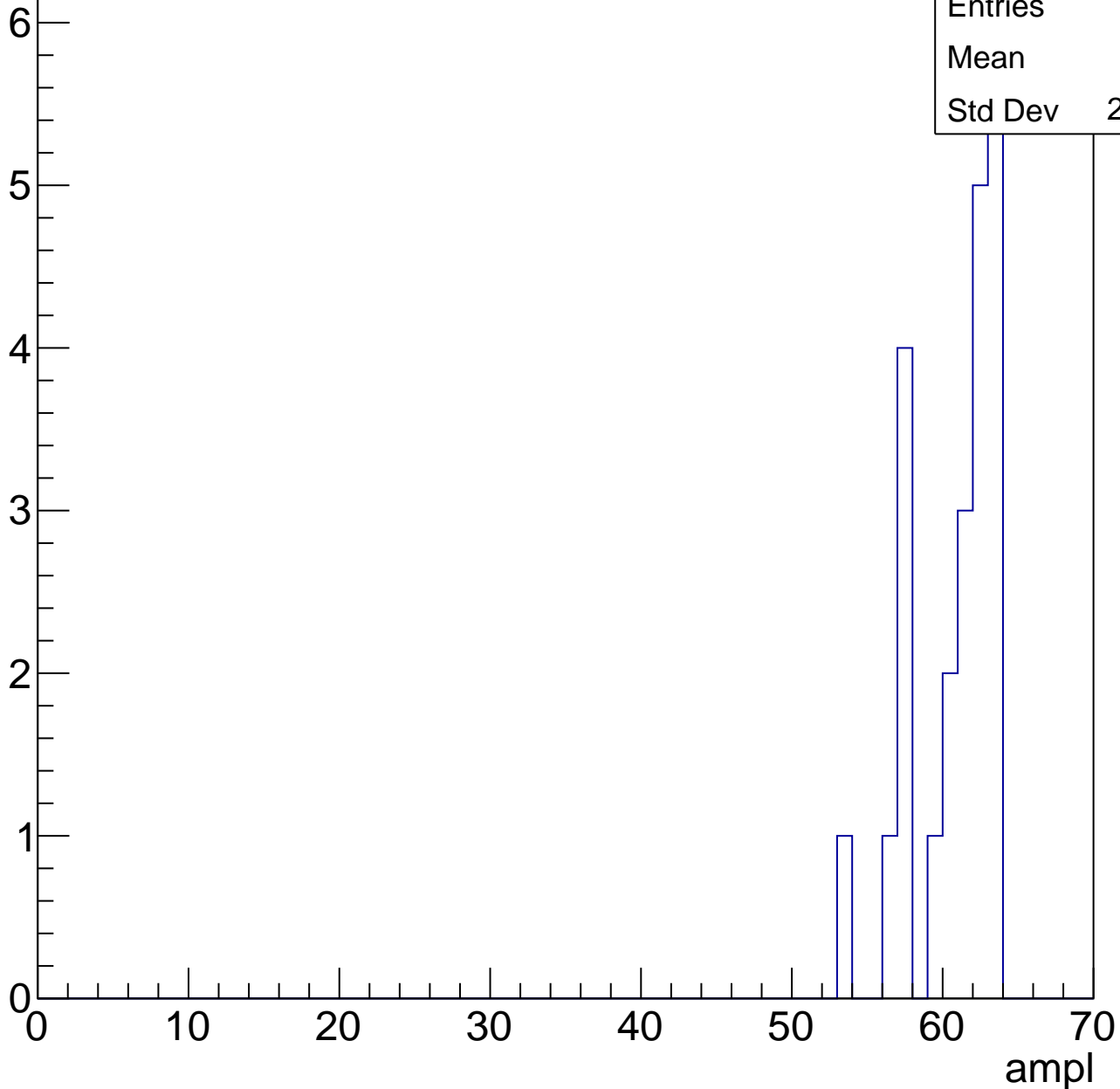


# B1L103S, U3-ch76, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	23
Mean	60.3
Std Dev	2.773

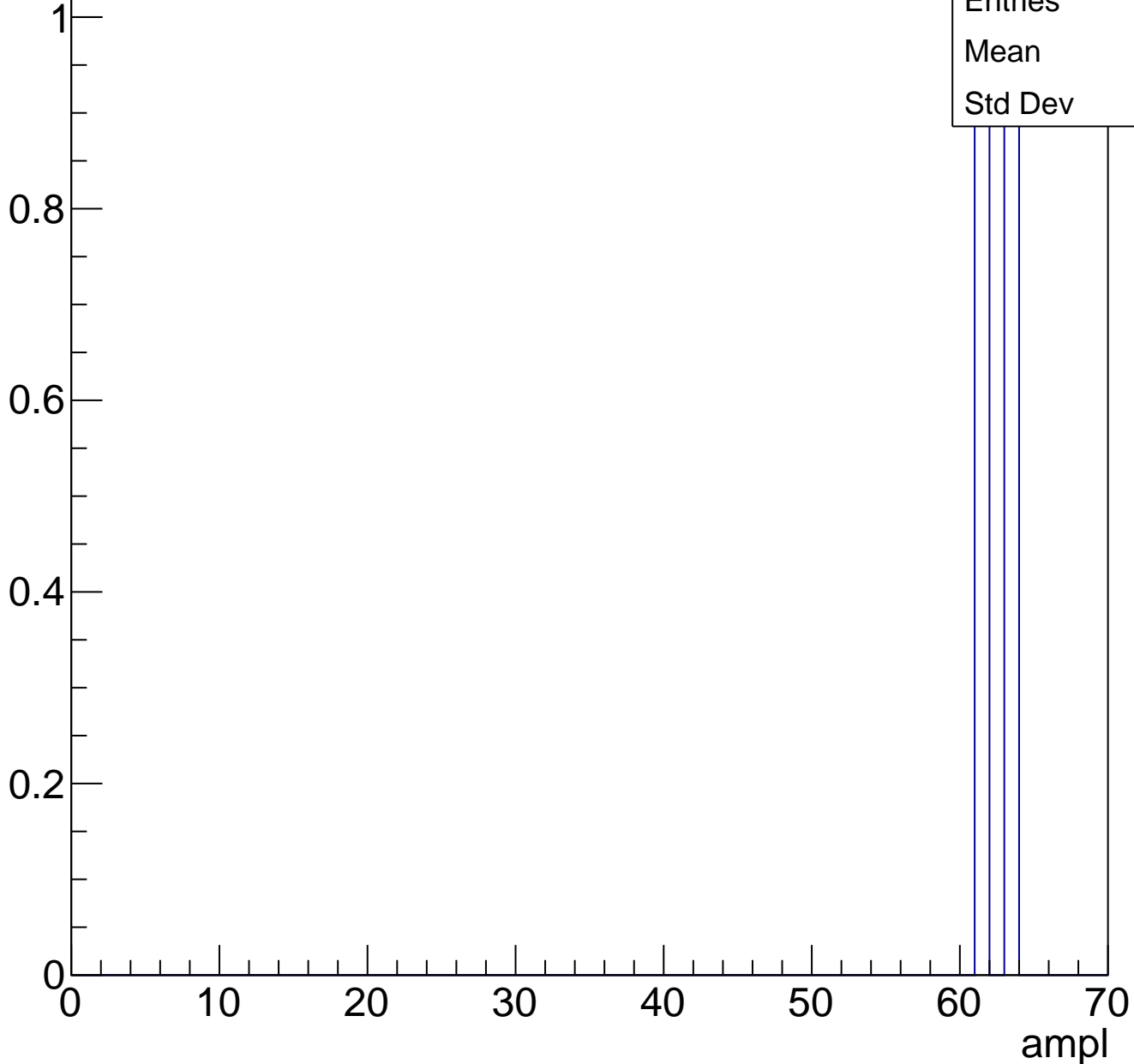




# B1L103S, U3-ch76, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch77, adc0

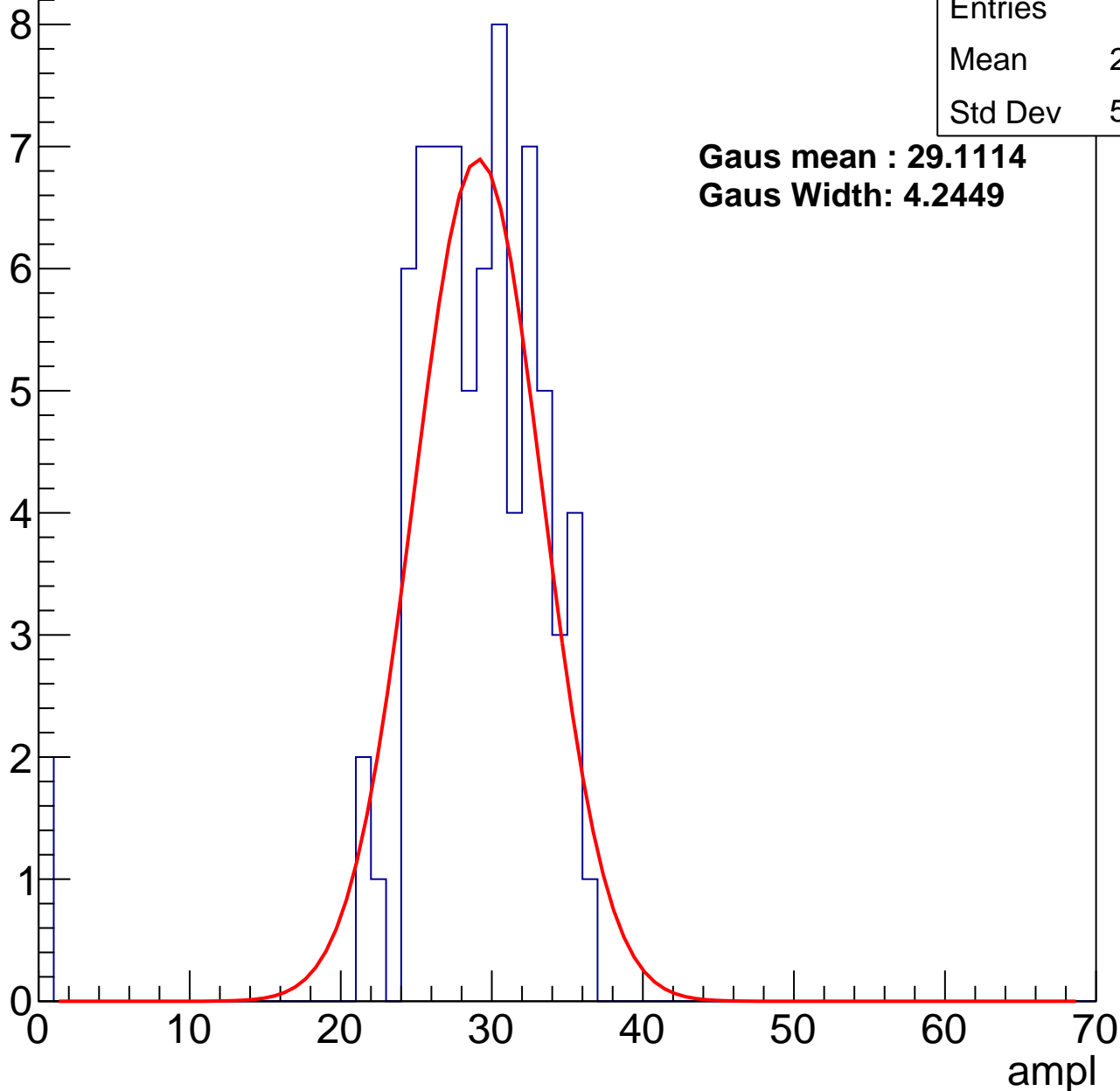
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	27.99
Std Dev	5.859

**Gaus mean : 29.1114**

**Gaus Width: 4.2449**



# B1L103S, U3-ch77, adc1

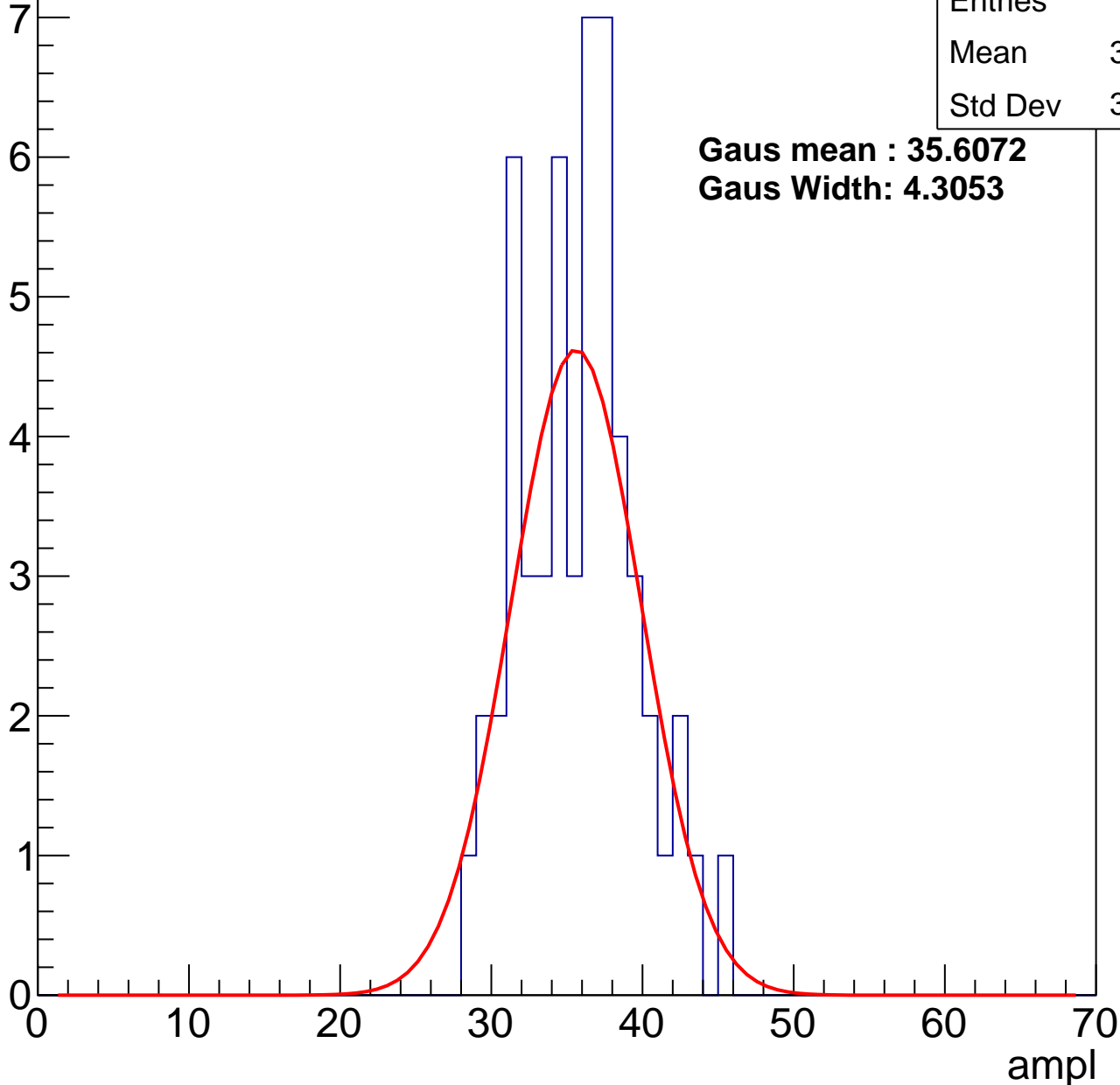
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	35.35
Std Dev	3.782

**Gaus mean : 35.6072**

**Gaus Width: 4.3053**



# B1L103S, U3-ch77, adc2

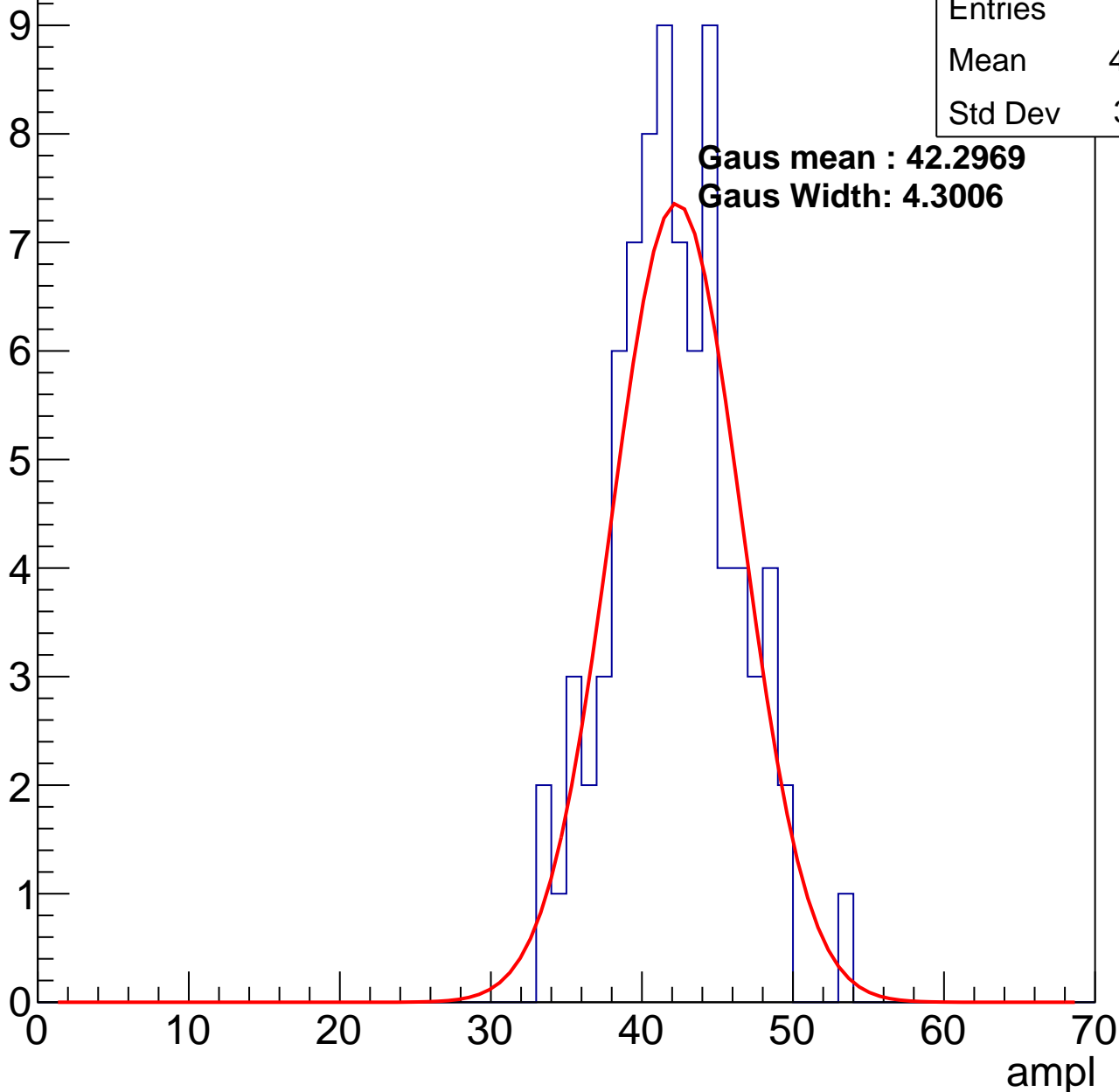
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	81
Mean	41.65
Std Dev	3.991

**Gaus mean : 42.2969**

**Gaus Width: 4.3006**



# B1L103S, U3-ch77, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

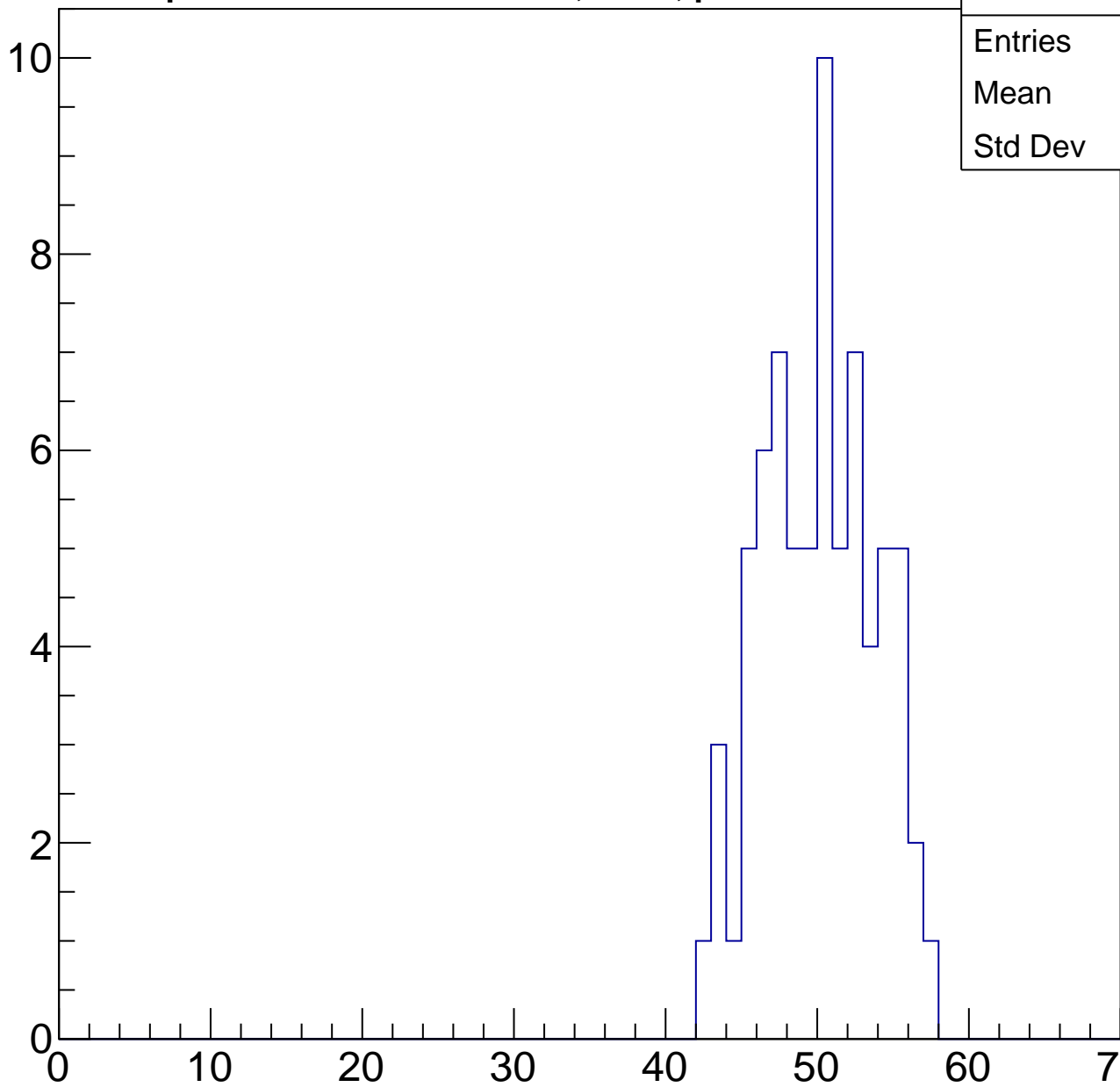
Entries	72
Mean	49.65
Std Dev	3.618

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

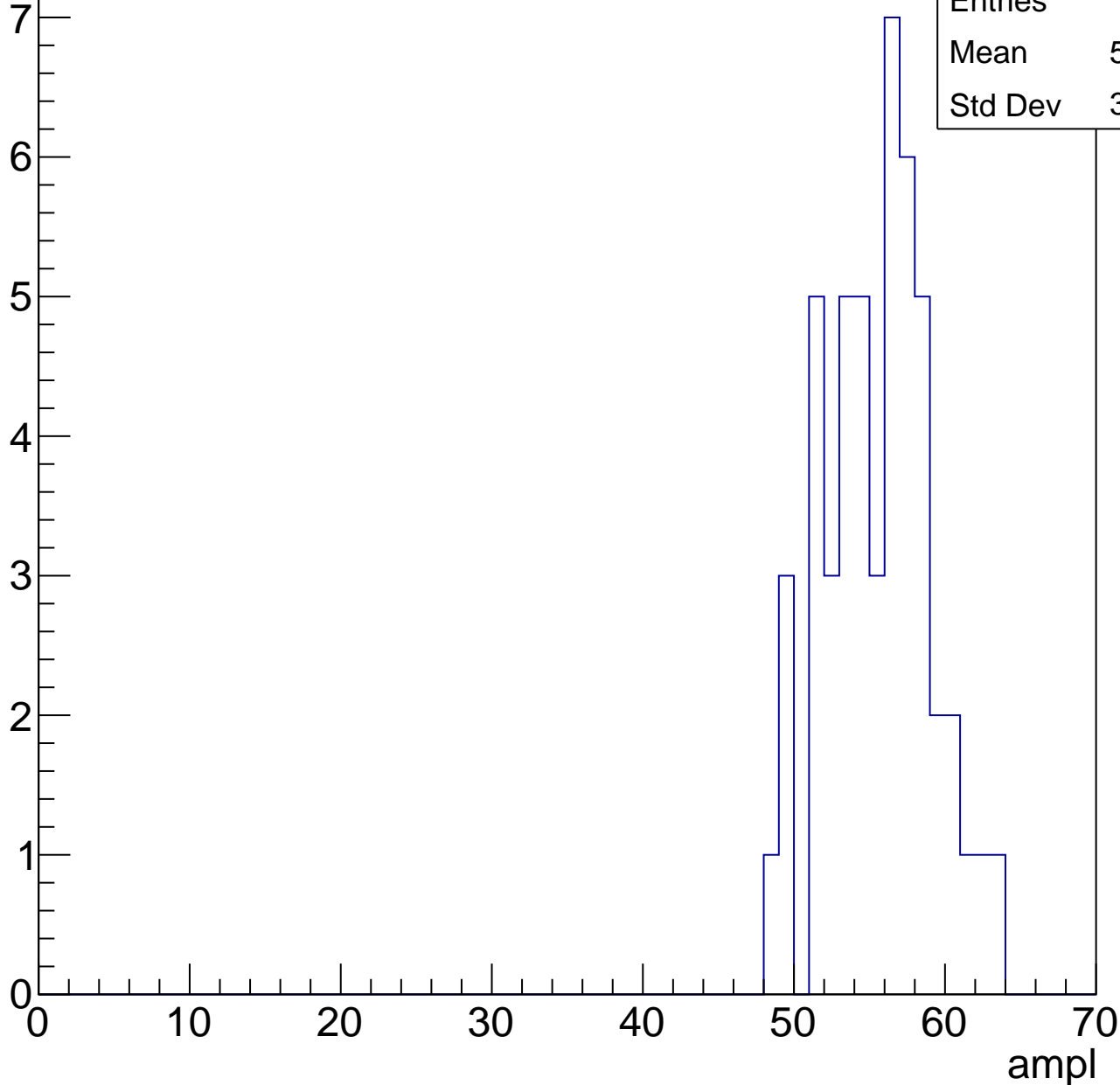


# B1L103S, U3-ch77, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

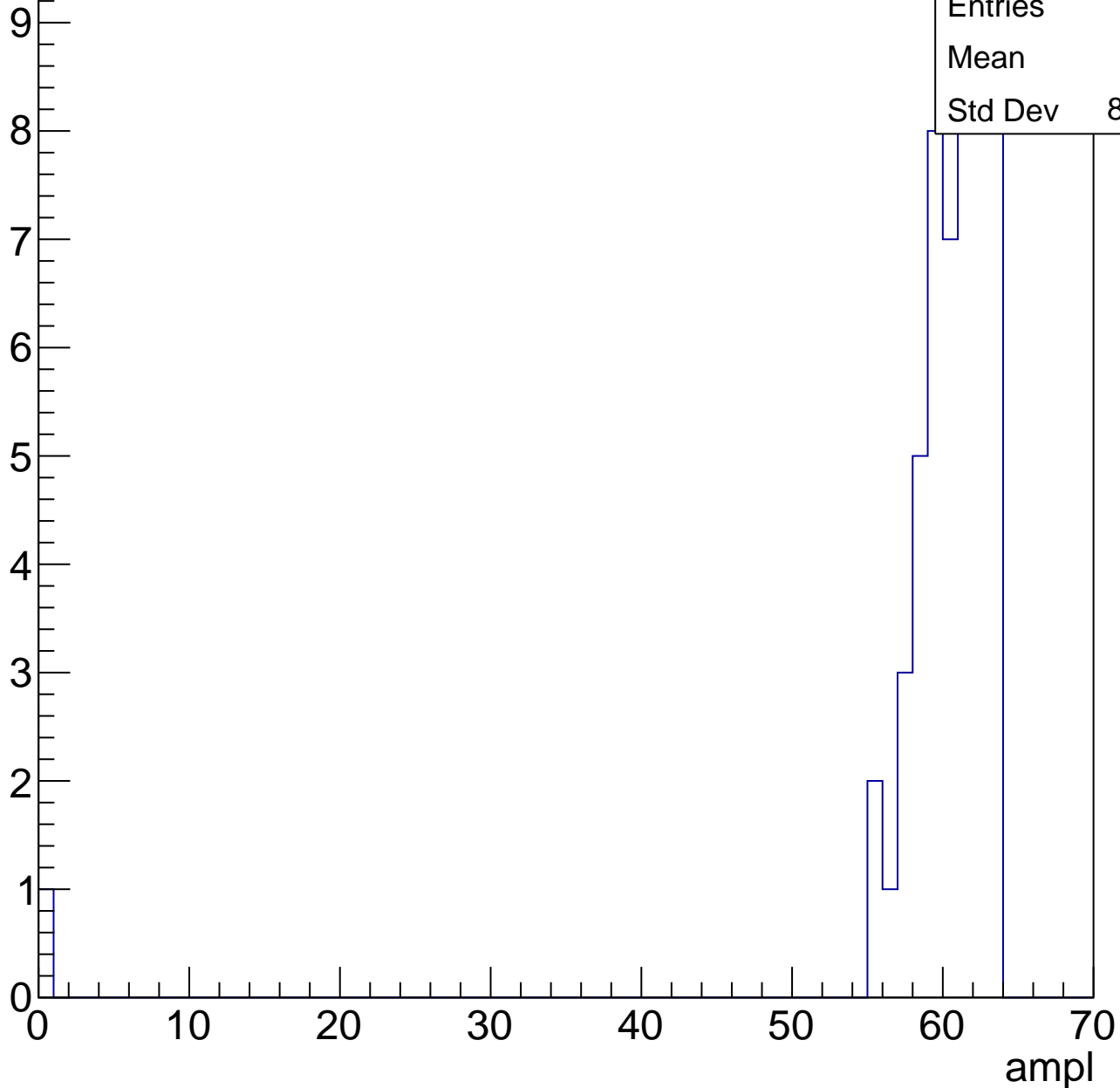
Entries	50
Mean	55.08
Std Dev	3.452



# B1L103S, U3-ch77, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

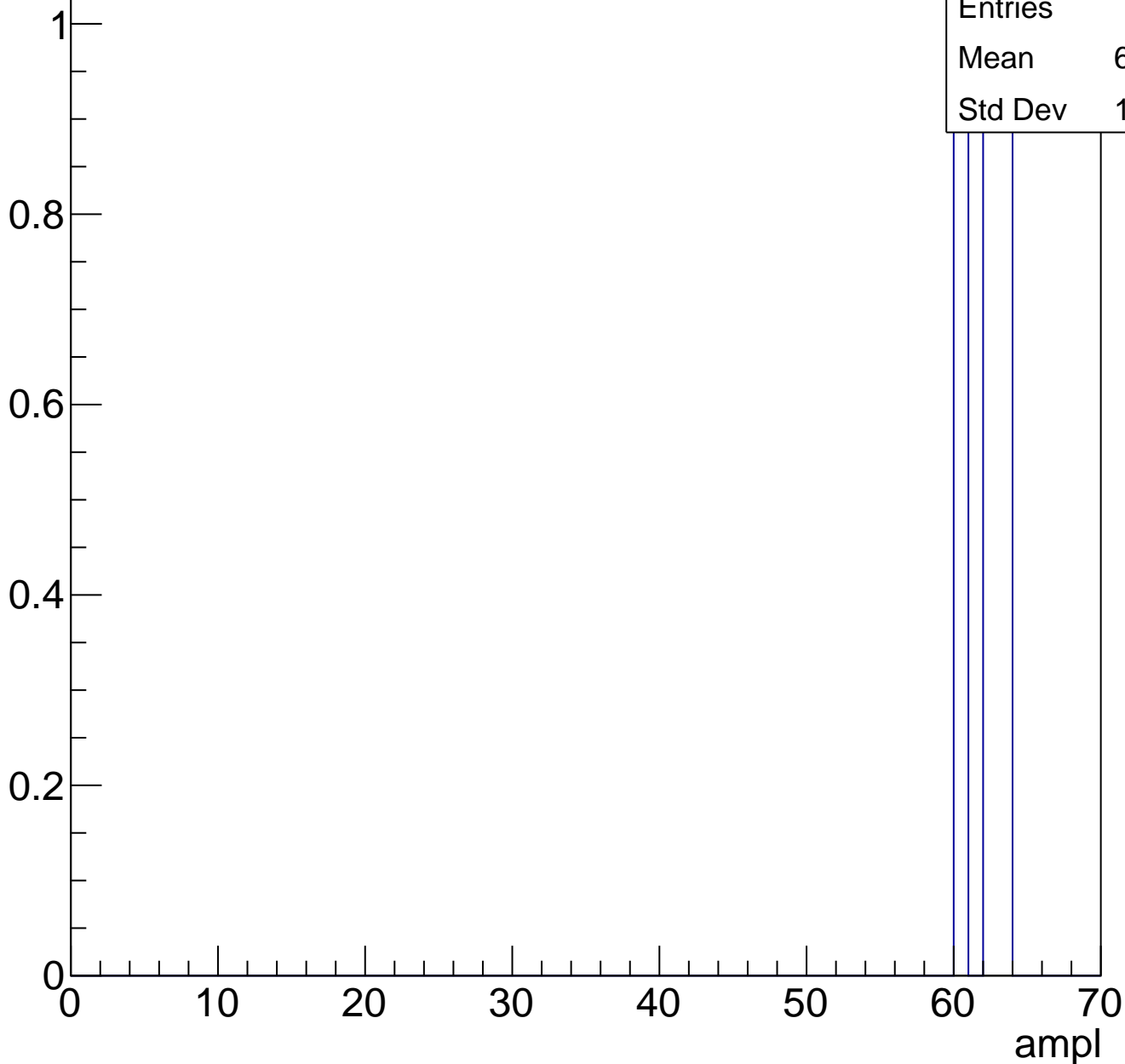
Entry



# B1L103S, U3-ch77, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U3-ch77, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch78, adc0

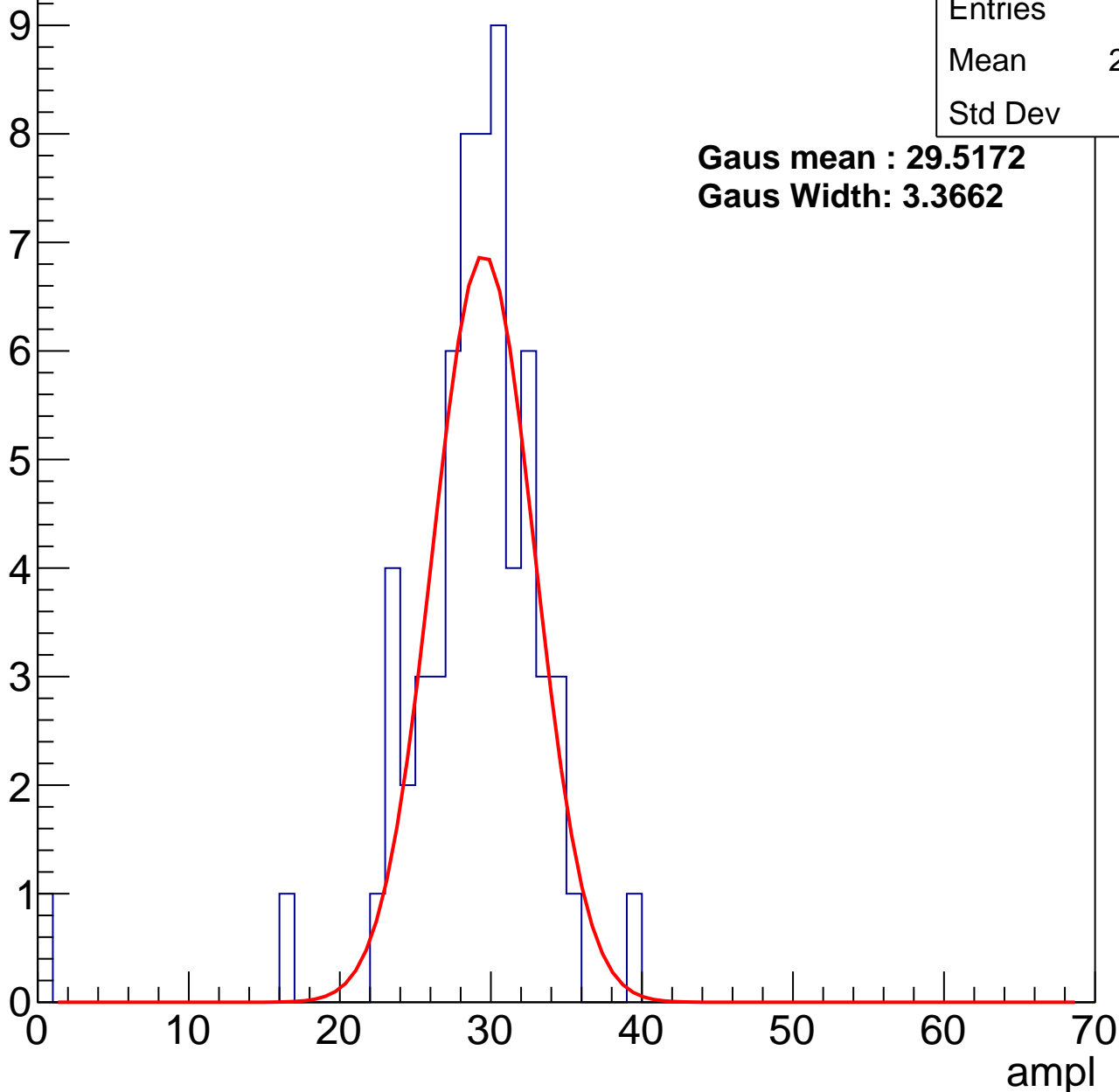
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	28.28
Std Dev	5.1

**Gaus mean : 29.5172**

**Gaus Width: 3.3662**



# B1L103S, U3-ch78, adc1

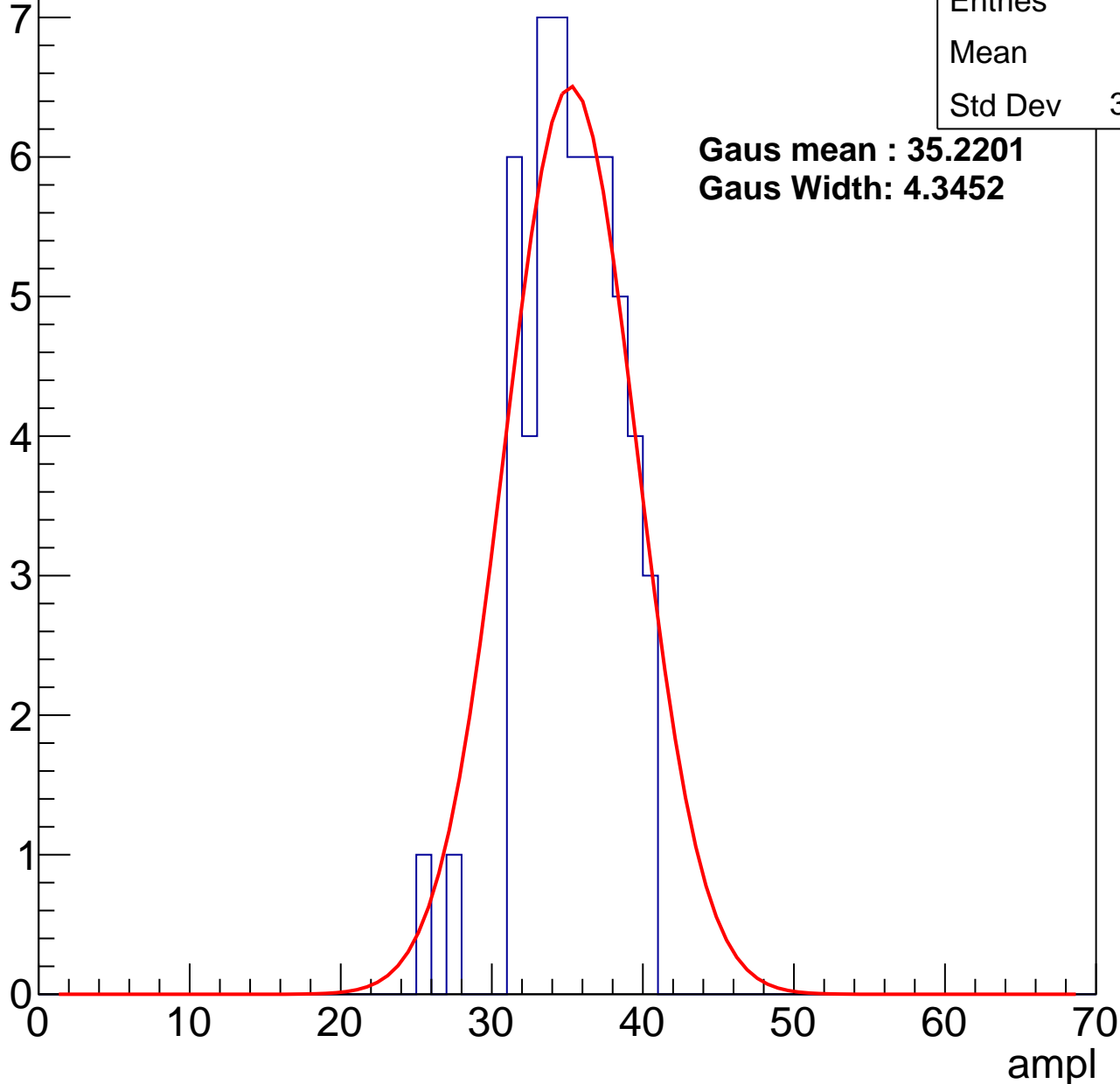
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	34.8
Std Dev	3.113

**Gaus mean : 35.2201**

**Gaus Width: 4.3452**



# B1L103S, U3-ch78, adc2

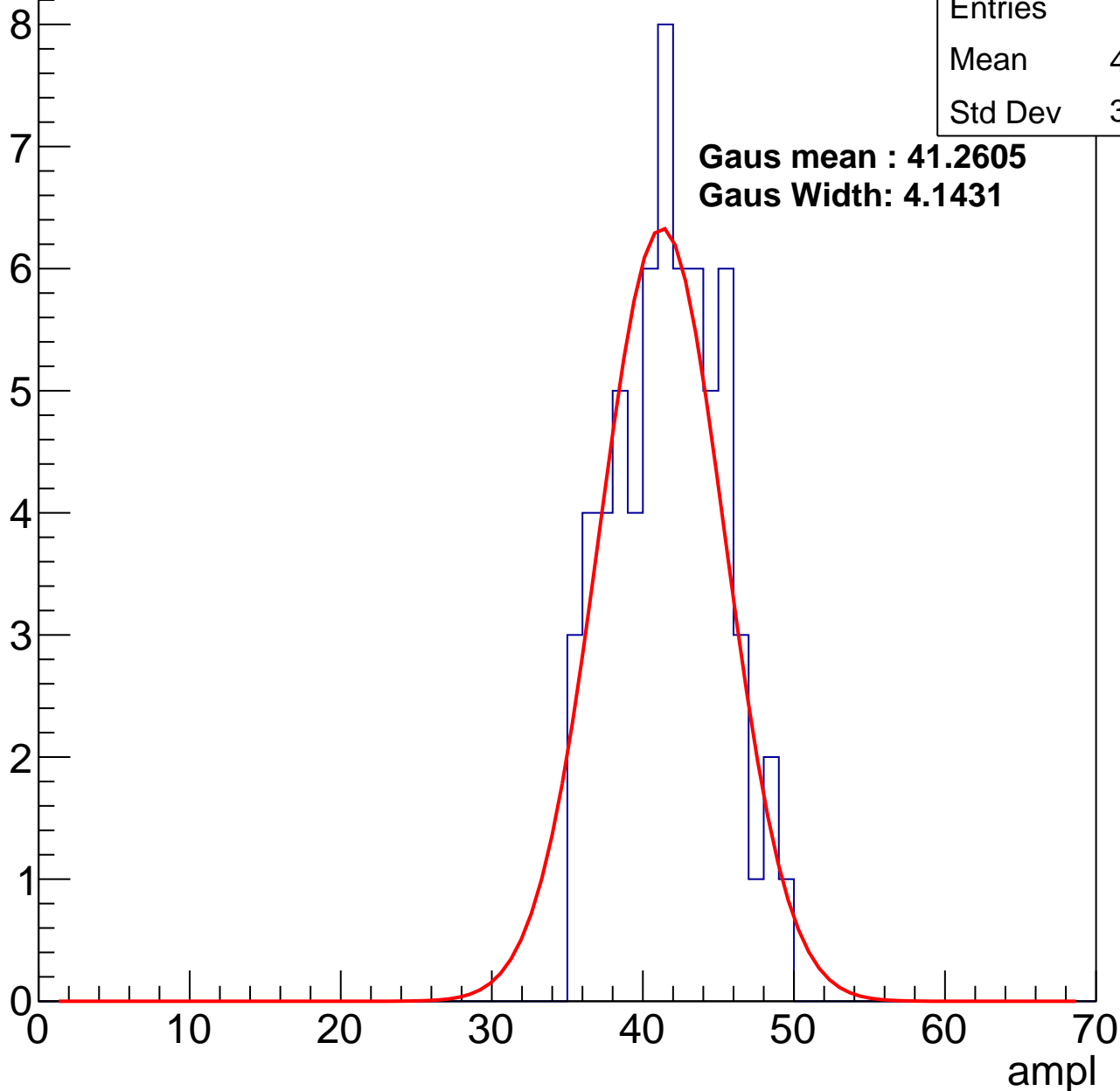
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	41.27
Std Dev	3.488

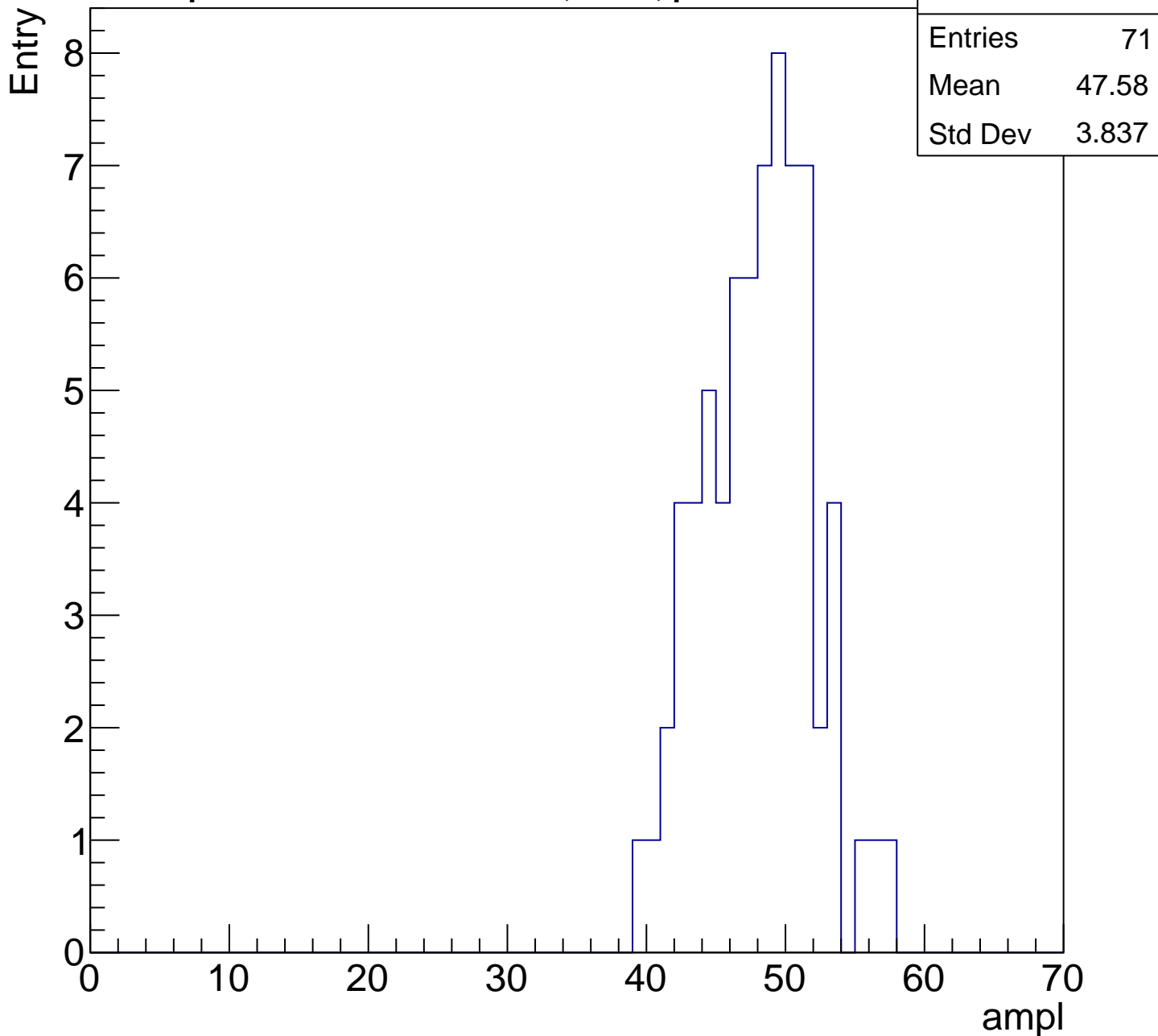
**Gaus mean : 41.2605**

**Gaus Width: 4.1431**



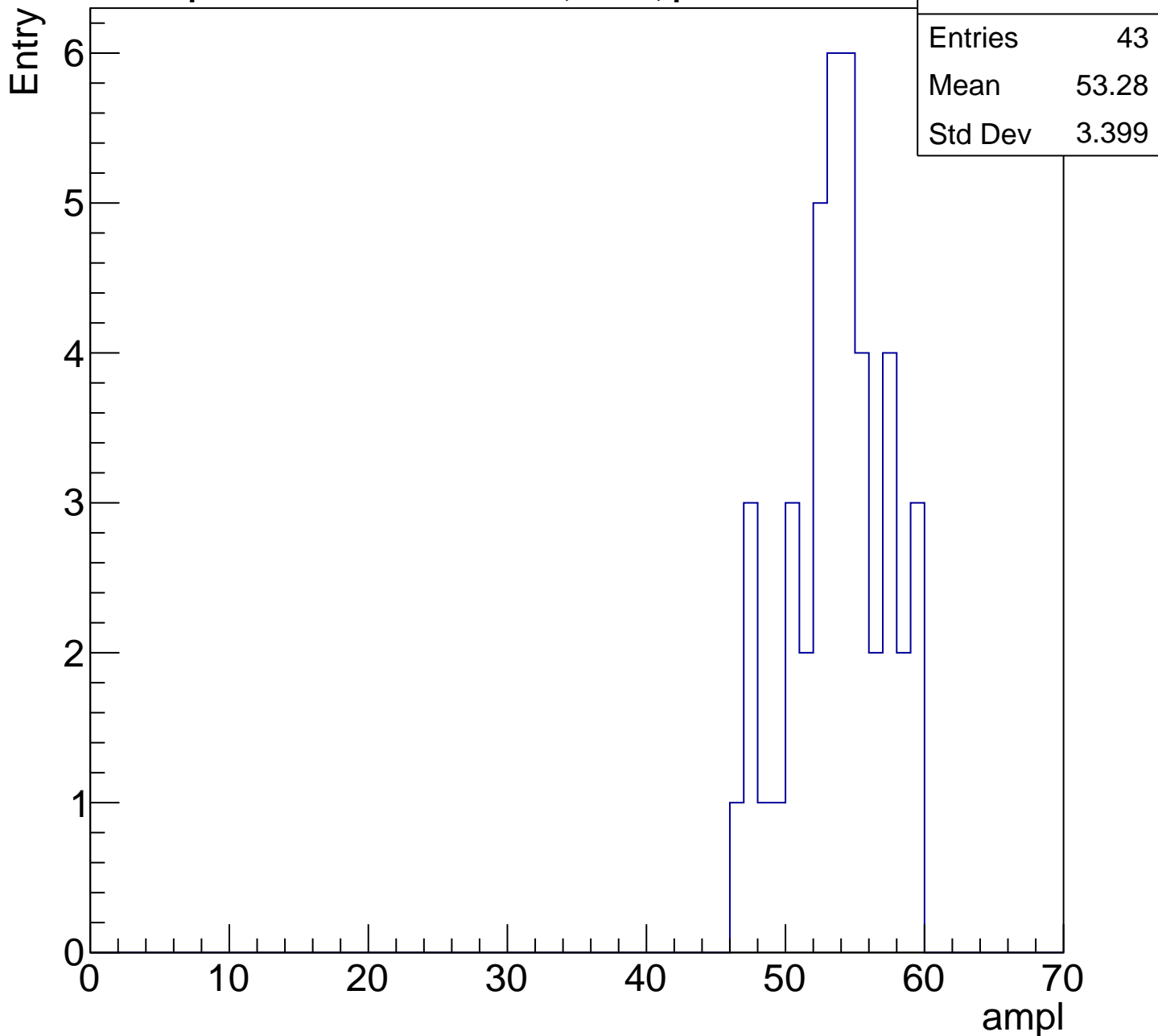
# B1L103S, U3-ch78, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2



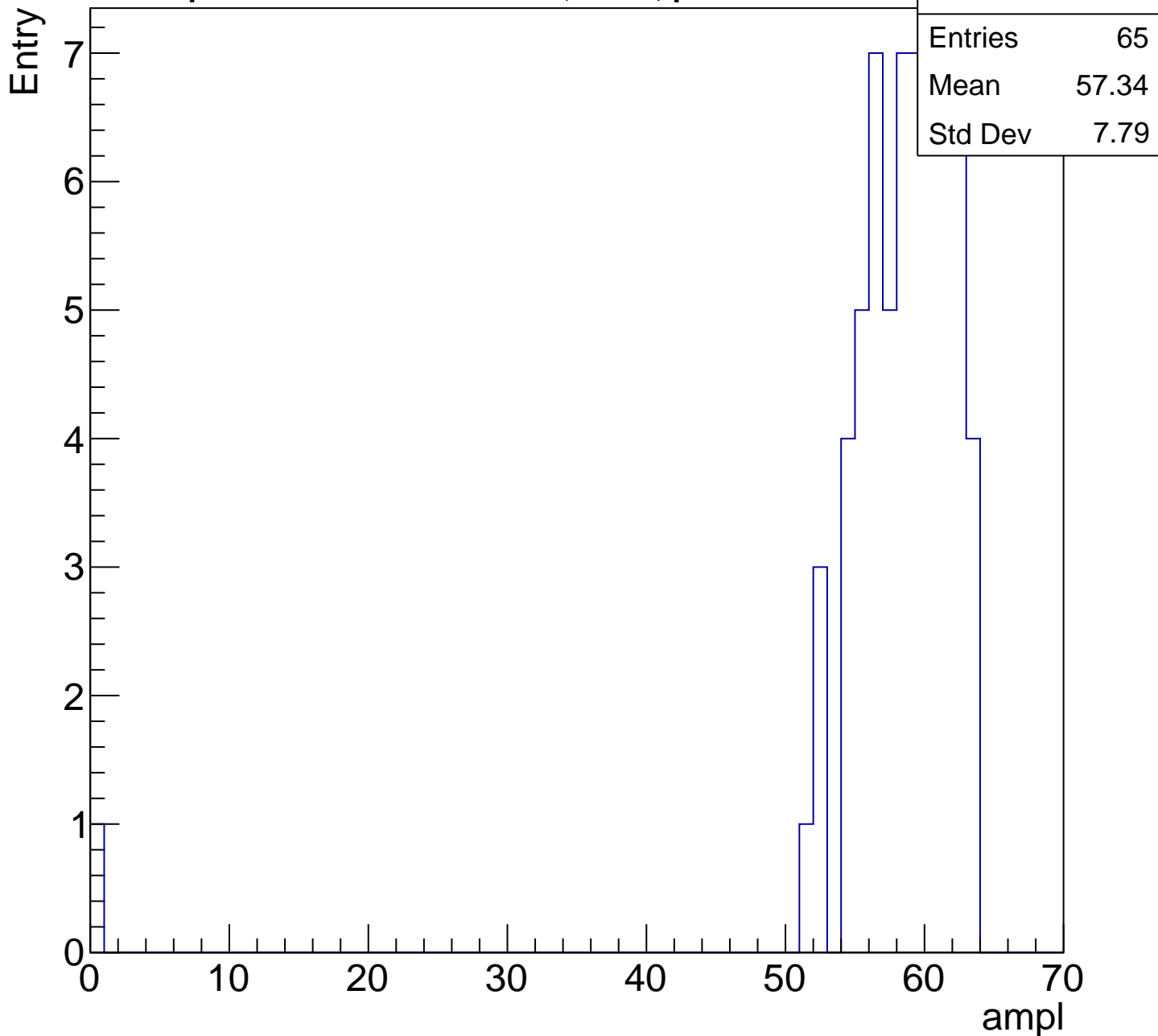
# B1L103S, U3-ch78, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U3-ch78, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

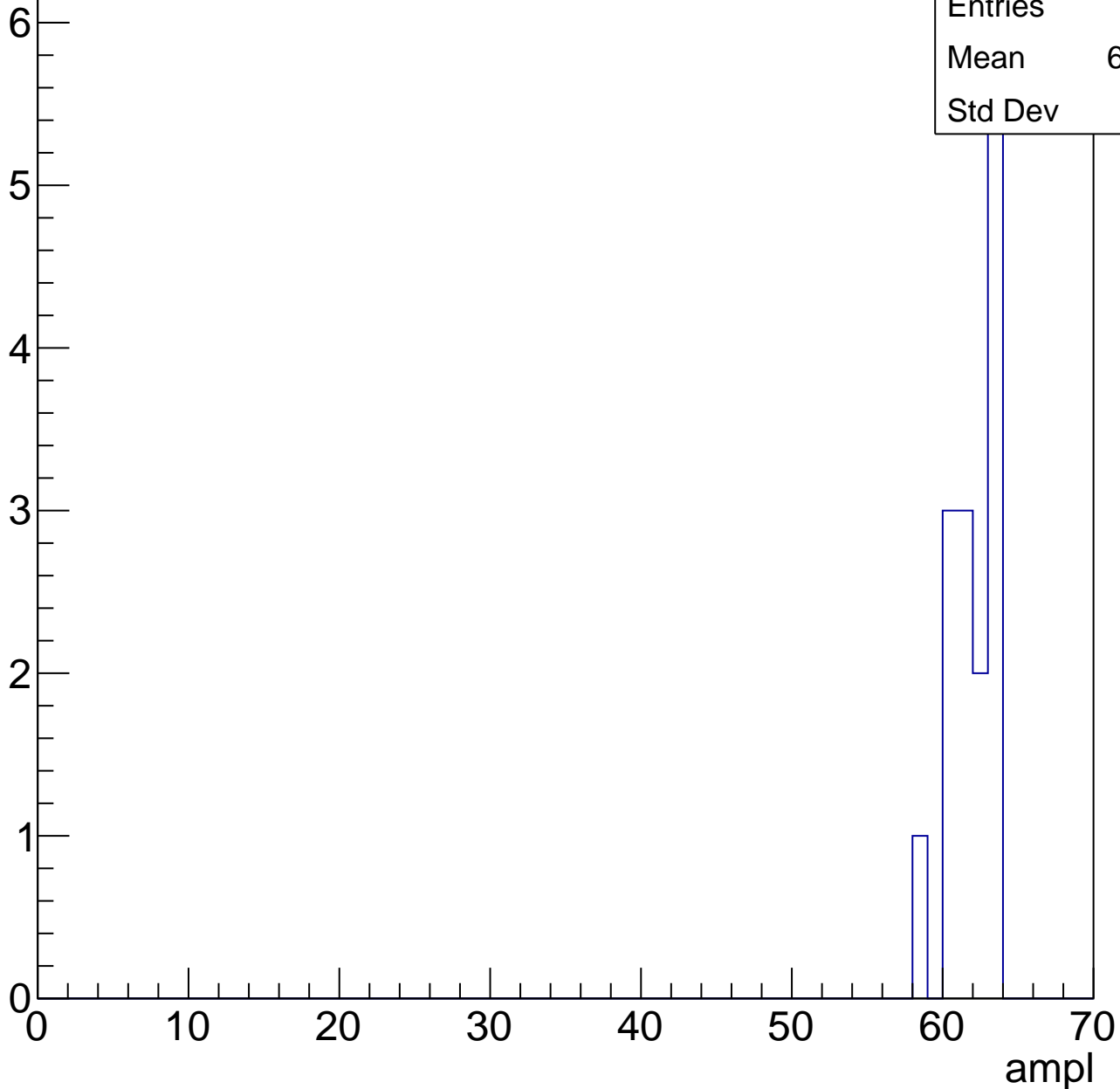


# B1L103S, U3-ch78, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	15
Mean	61.53
Std Dev	1.5

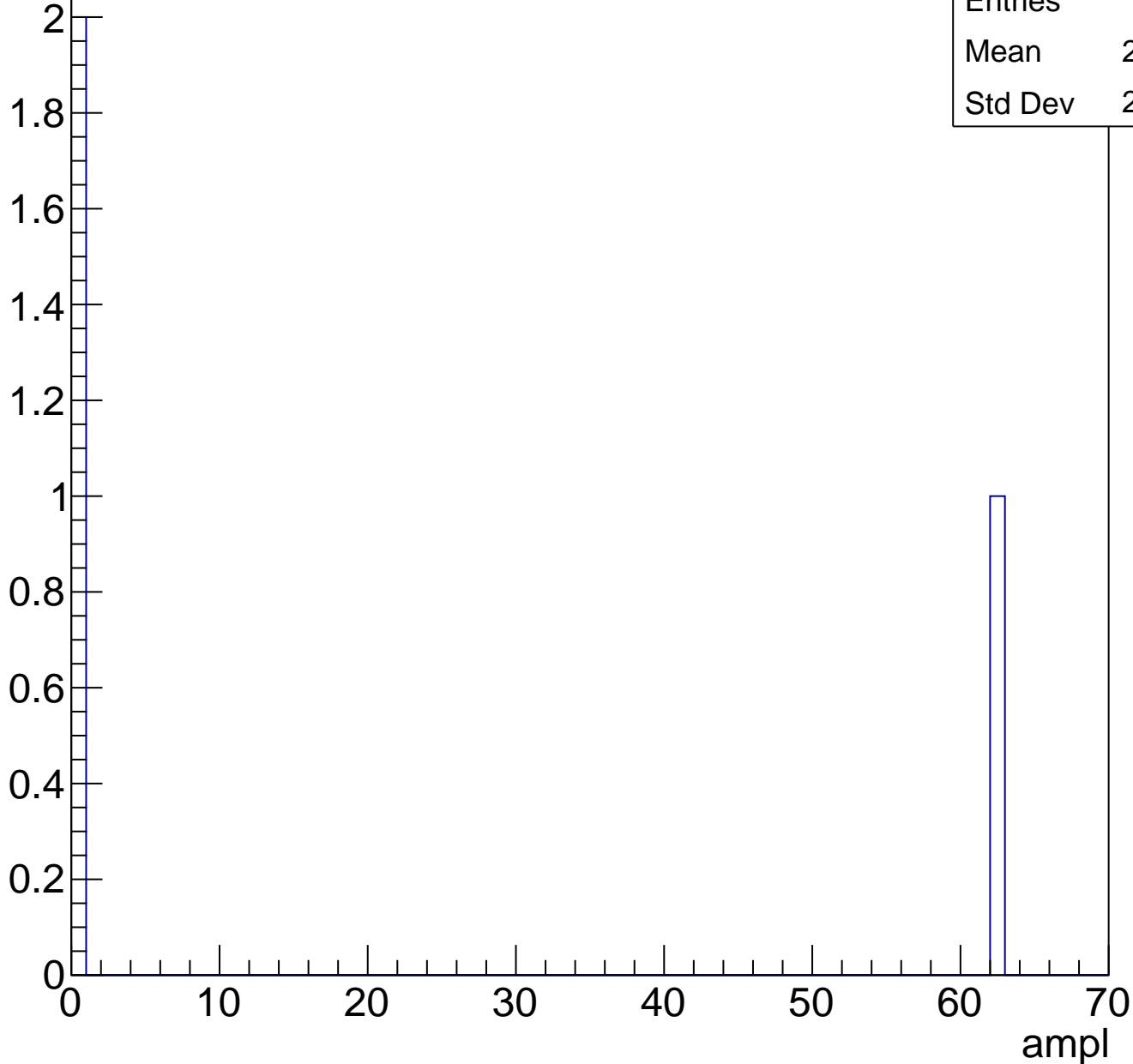




# B1L103S, U3-ch78, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch79, adc0

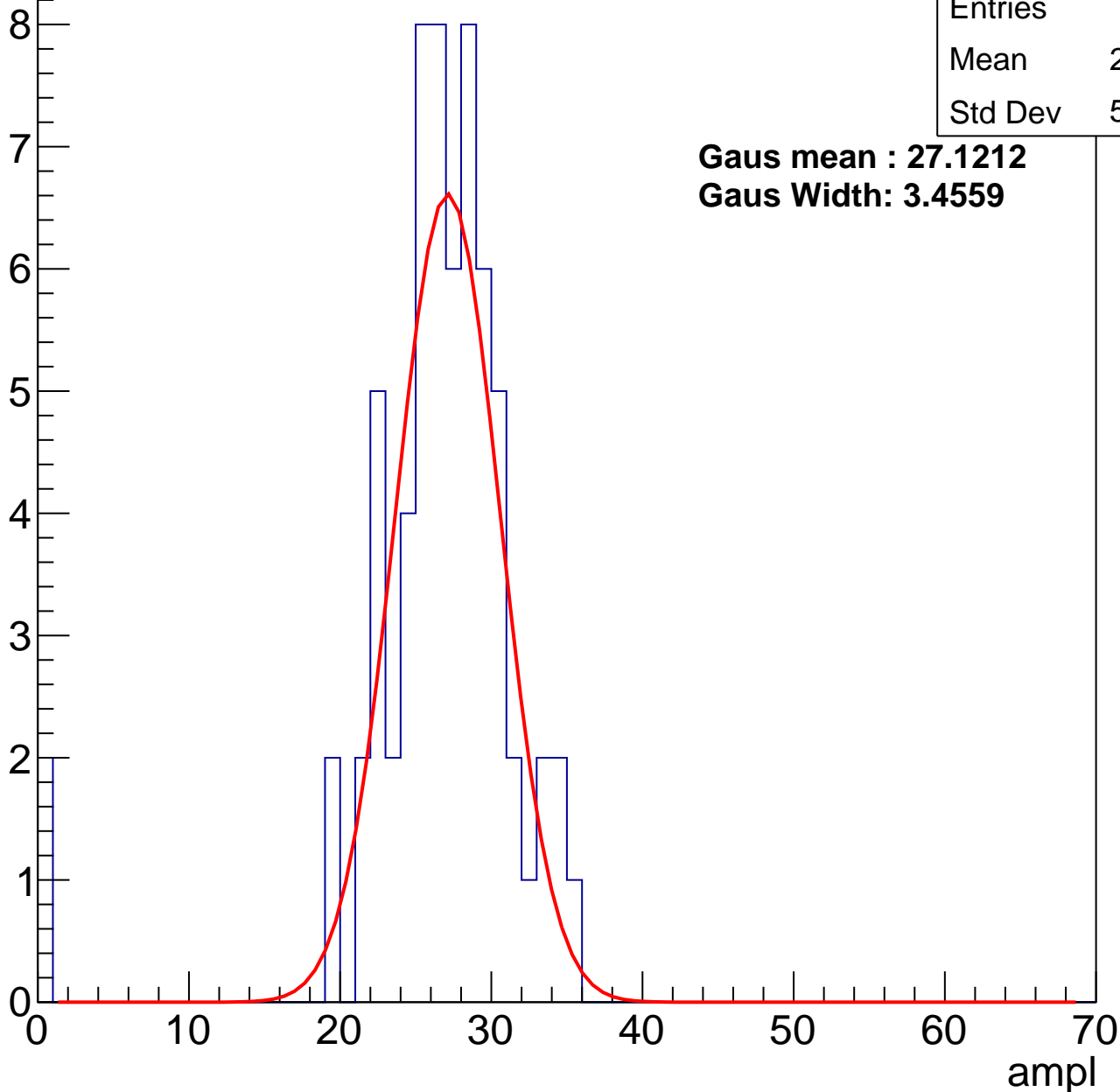
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	25.95
Std Dev	5.756

**Gaus mean : 27.1212**

**Gaus Width: 3.4559**



# B1L103S, U3-ch79, adc1

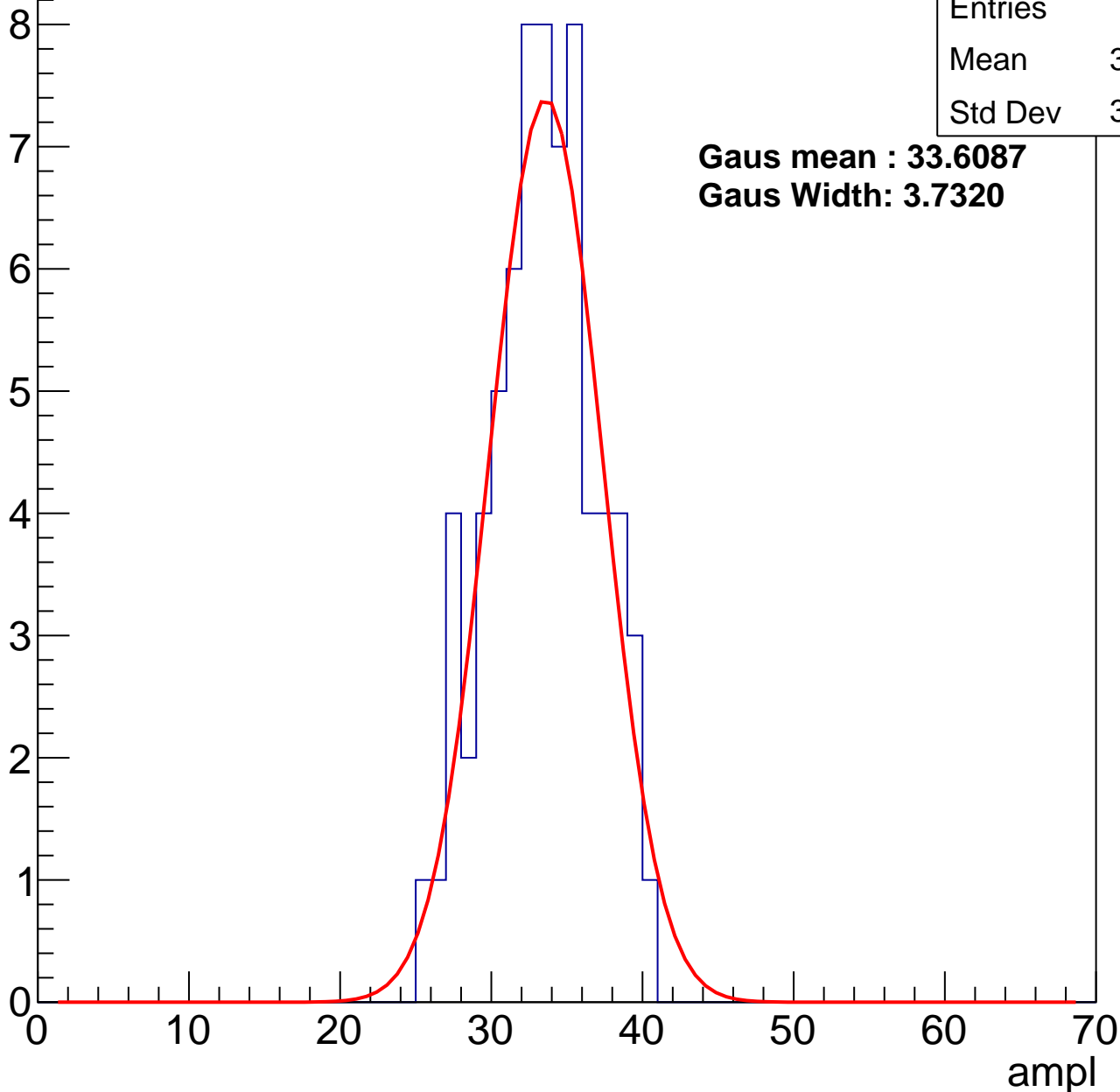
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	32.94
Std Dev	3.472

**Gaus mean : 33.6087**

**Gaus Width: 3.7320**



# B1L103S, U3-ch79, adc2

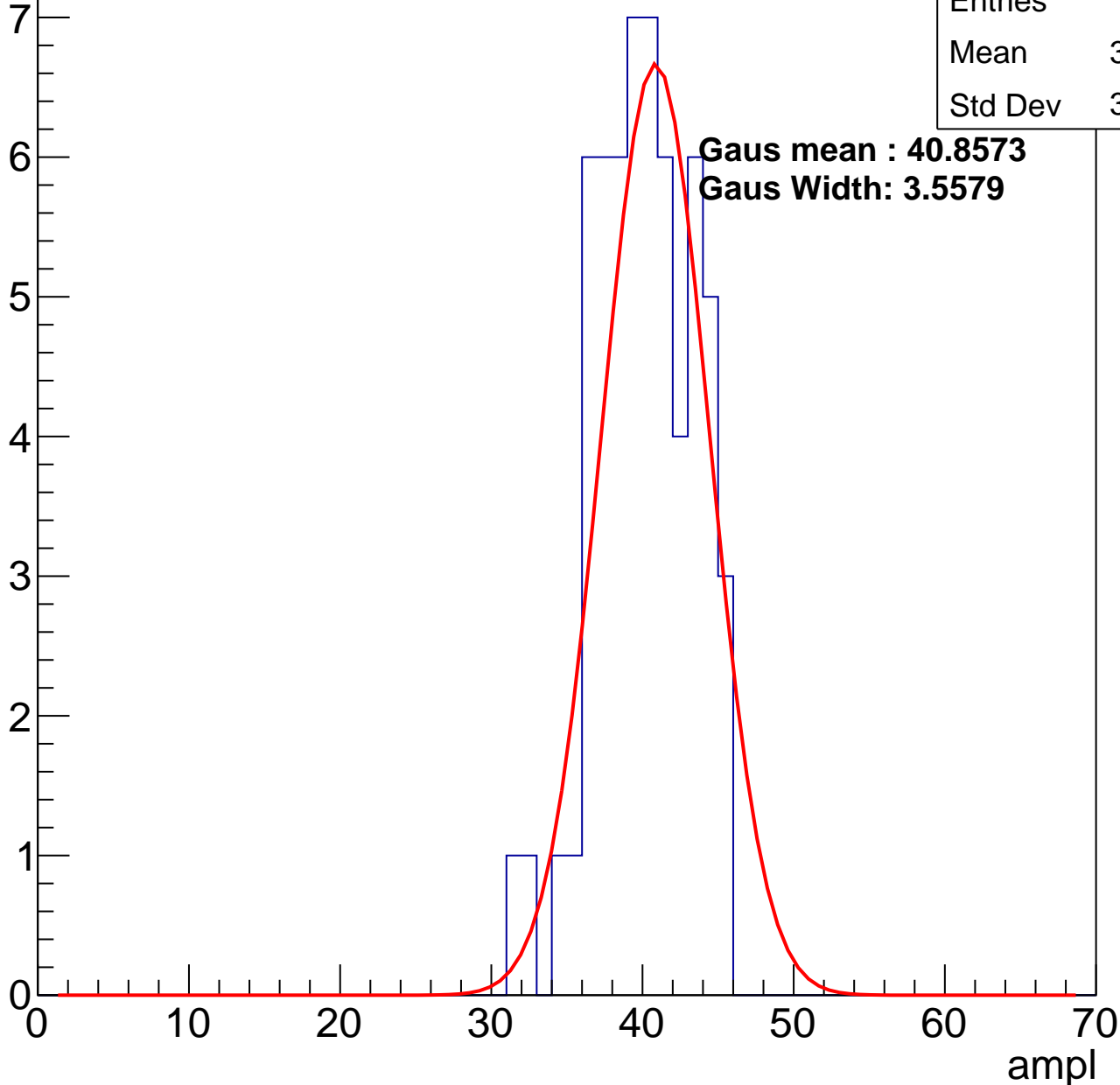
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	39.63
Std Dev	3.188

**Gaus mean : 40.8573**

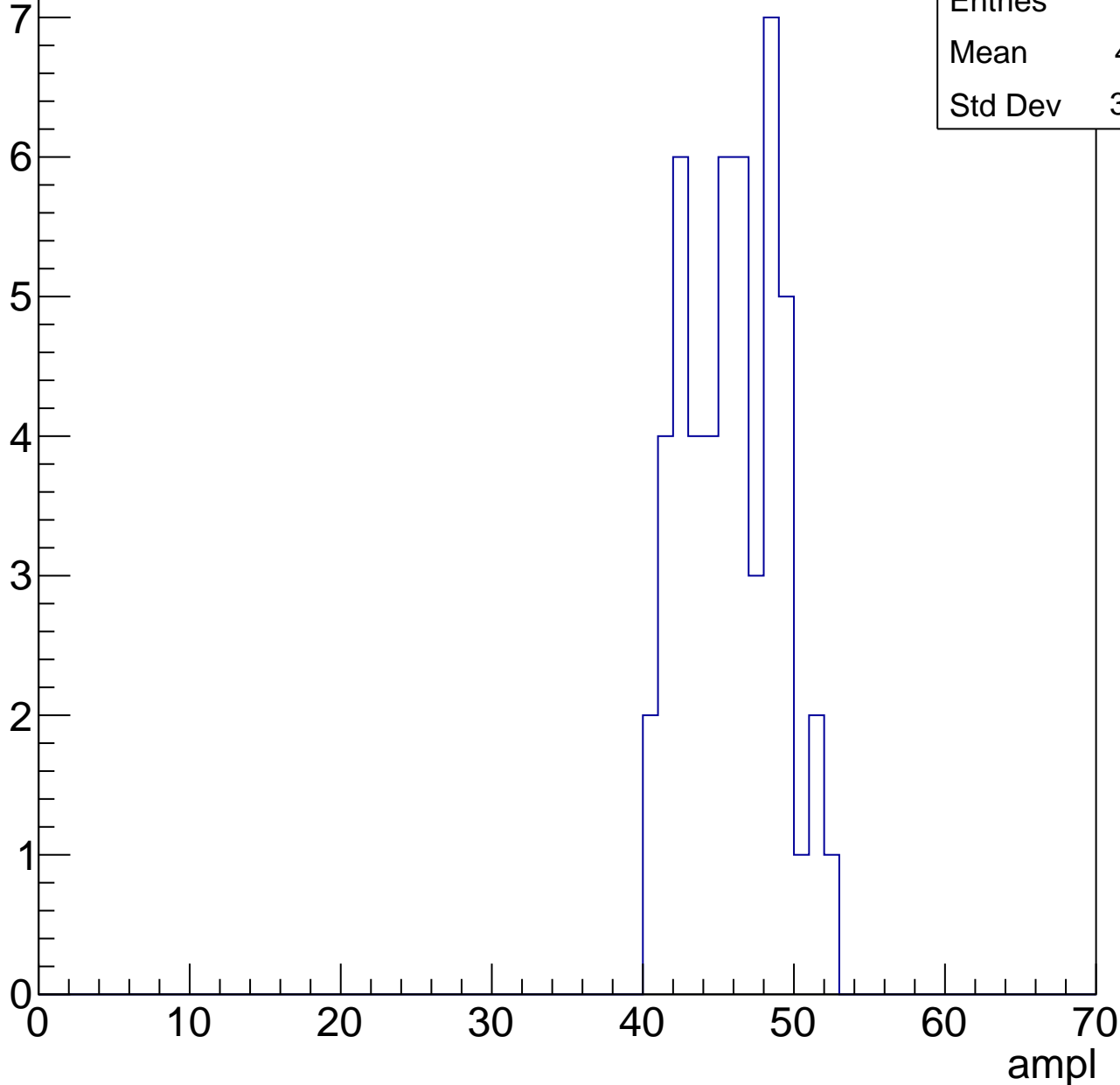
**Gaus Width: 3.5579**



# B1L103S, U3-ch79, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

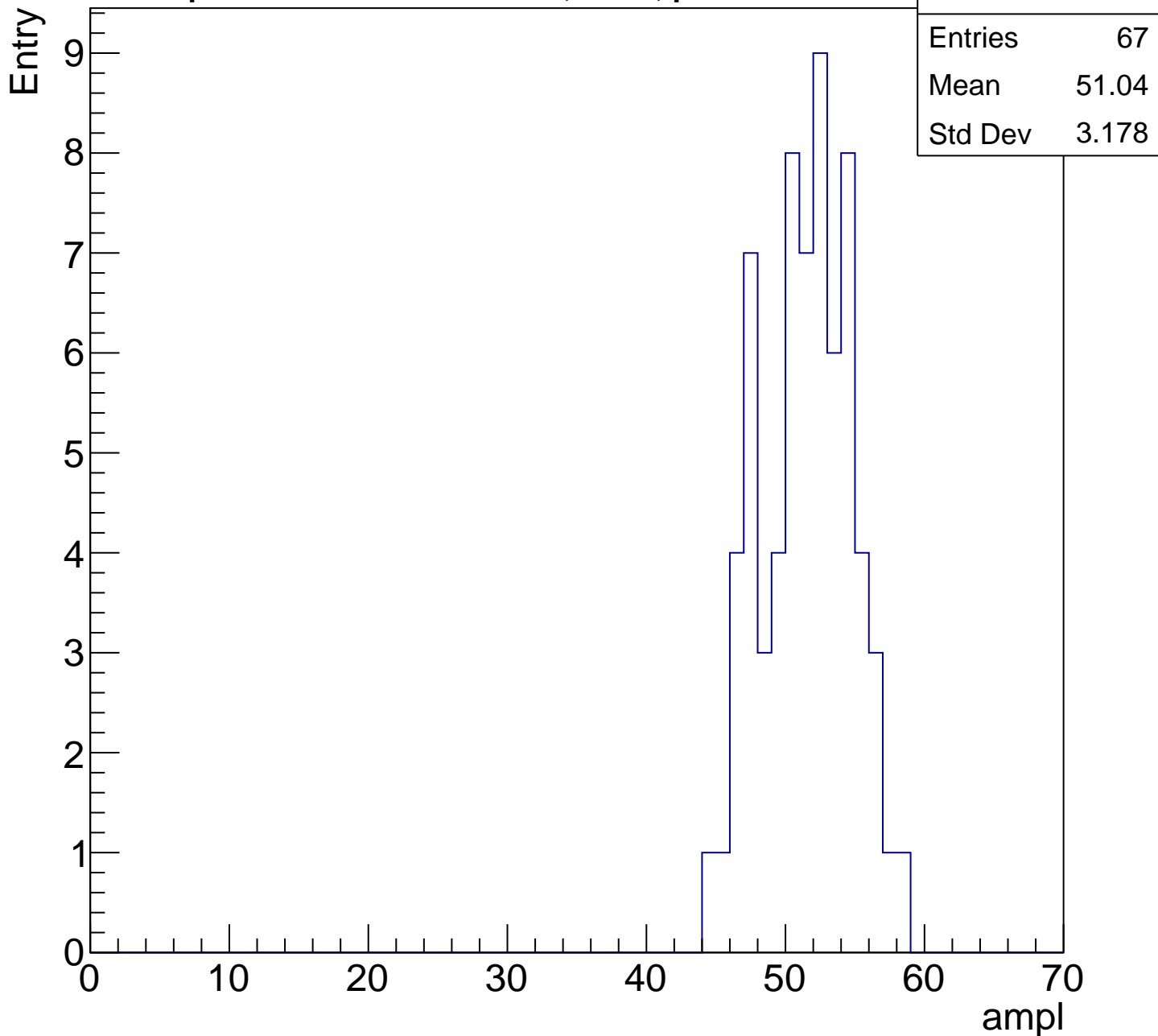
Entry



Entries	51
Mean	45.41
Std Dev	3.088

# B1L103S, U3-ch79, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U3-ch79, adc5

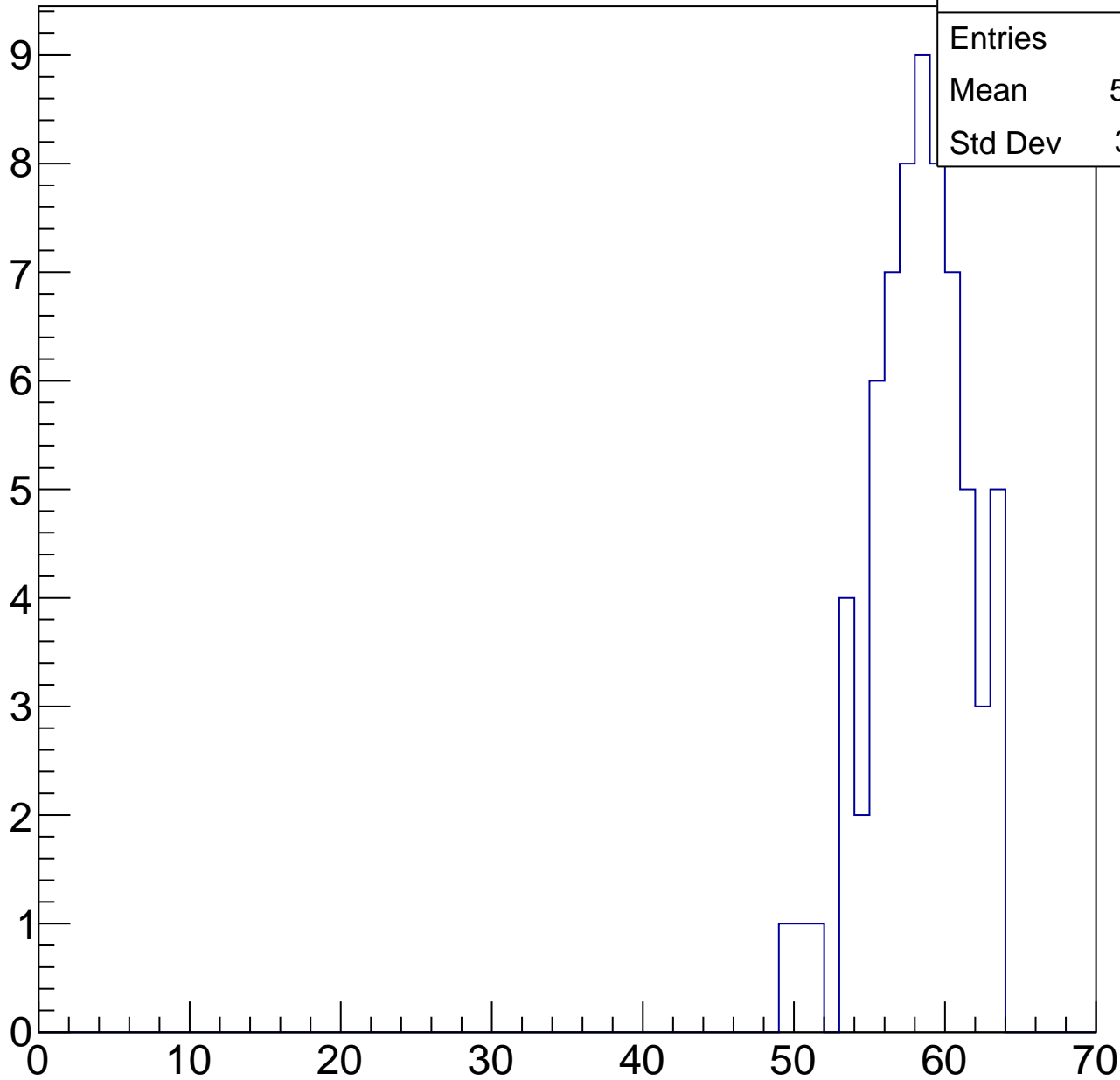
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	67
Mean	57.73
Std Dev	3.151

ampl

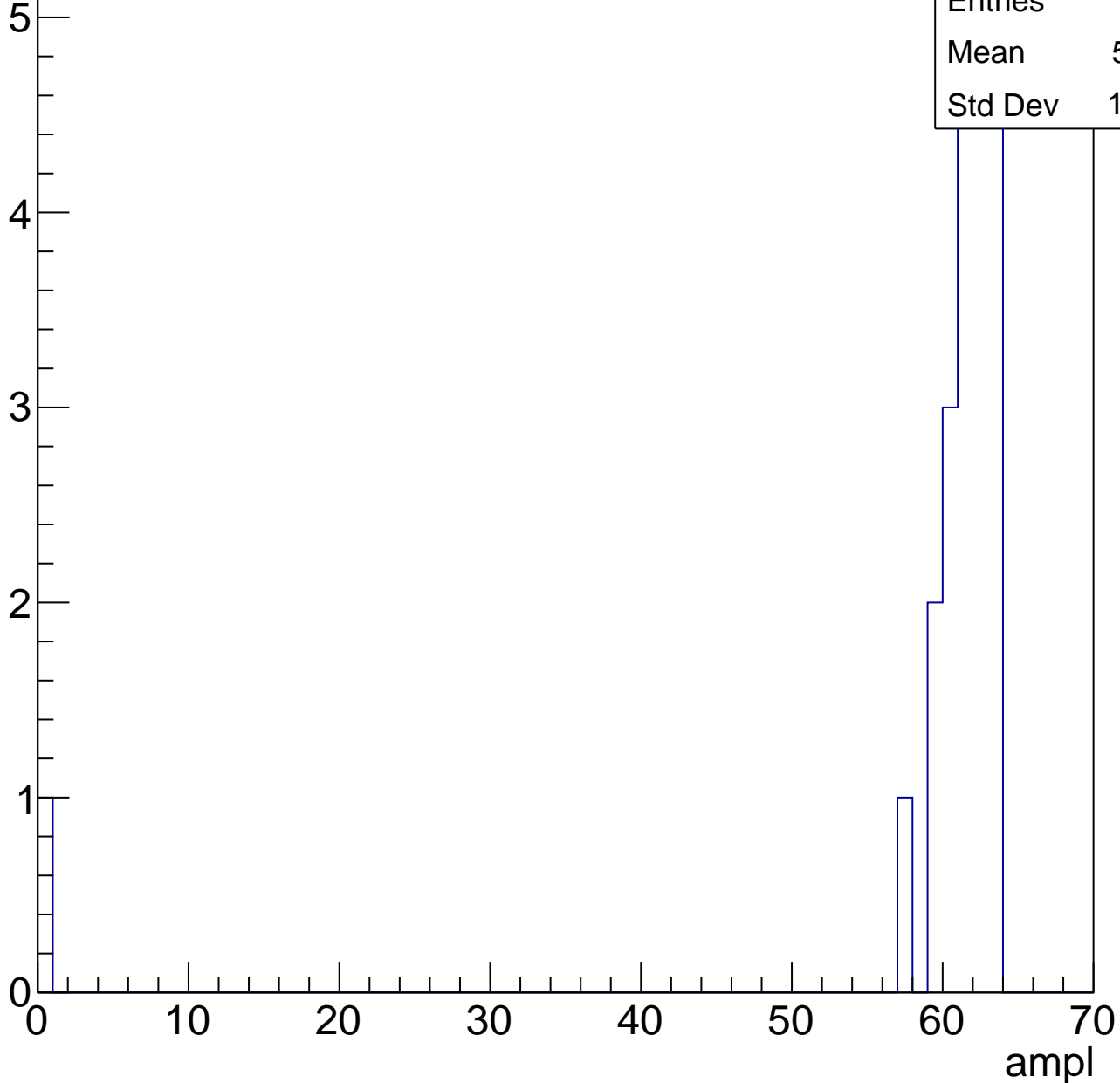


# B1L103S, U3-ch79, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	22
Mean	58.41
Std Dev	12.84





# B1L103S, U3-ch79, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	41.33
Std Dev	29.23

0 10 20 30 40 50 60 70

ampl

# B1L103S, U3-ch80, adc0

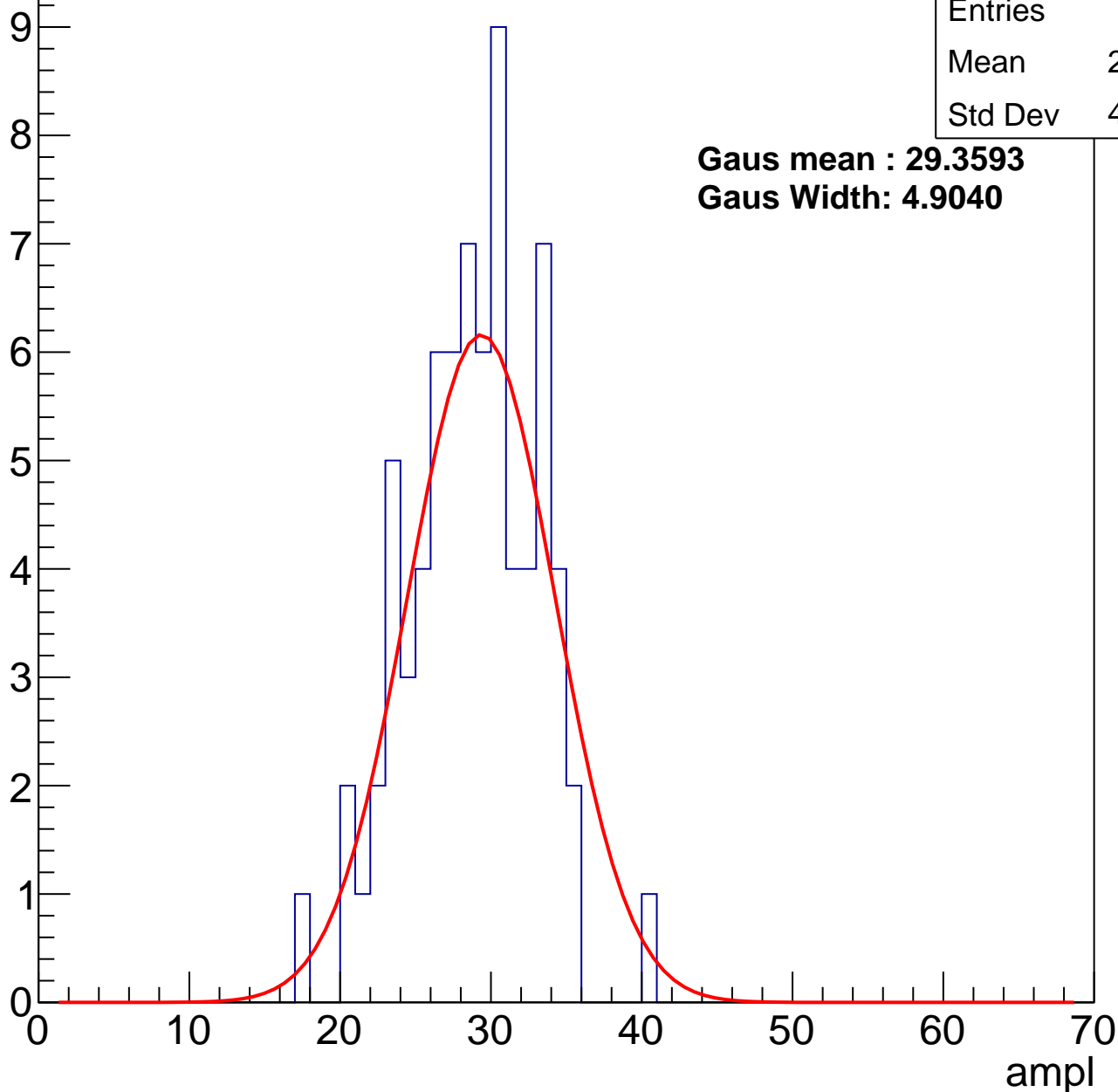
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	28.32
Std Dev	4.198

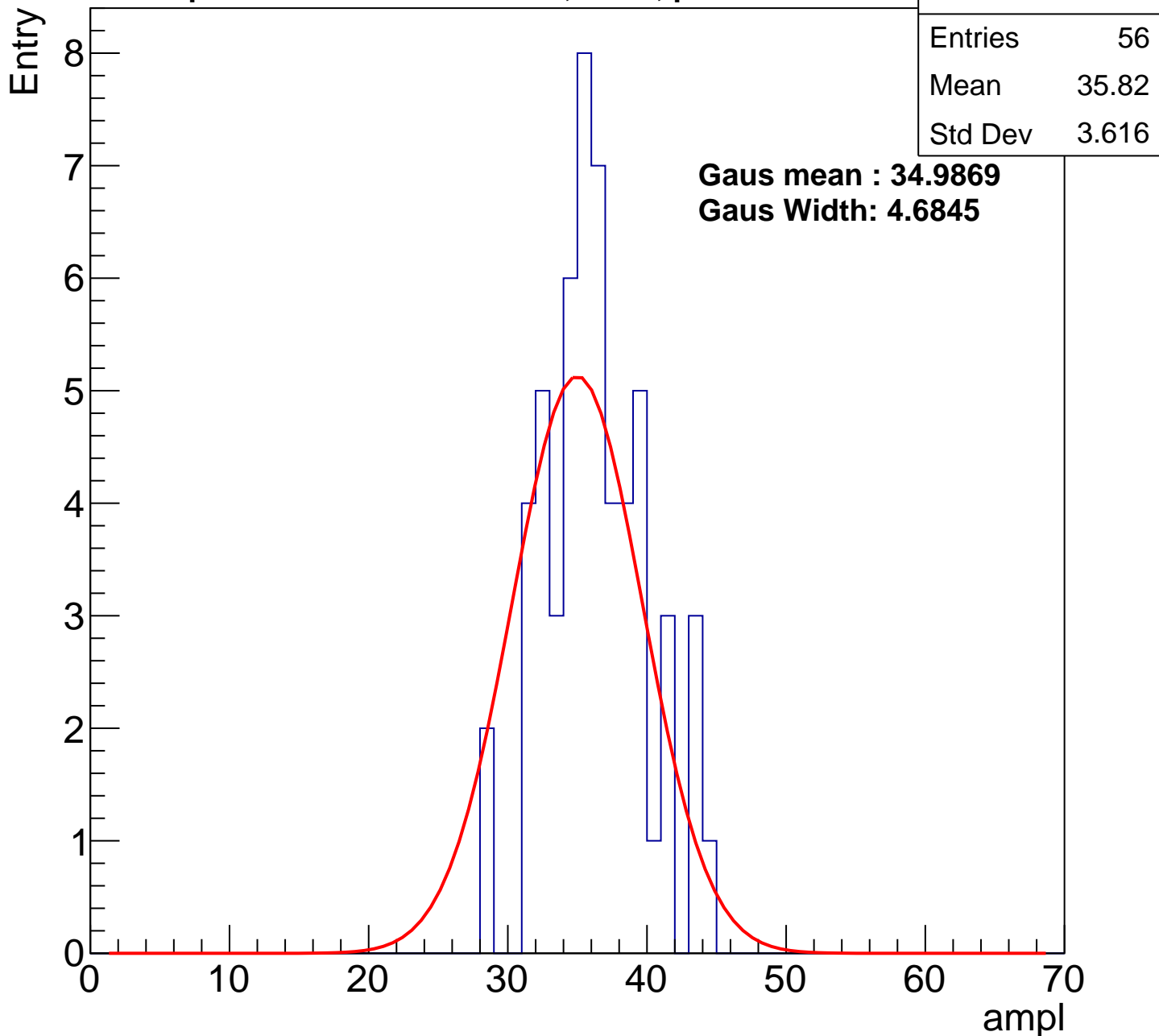
**Gaus mean : 29.3593**

**Gaus Width: 4.9040**



# B1L103S, U3-ch80, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U3-ch80, adc2

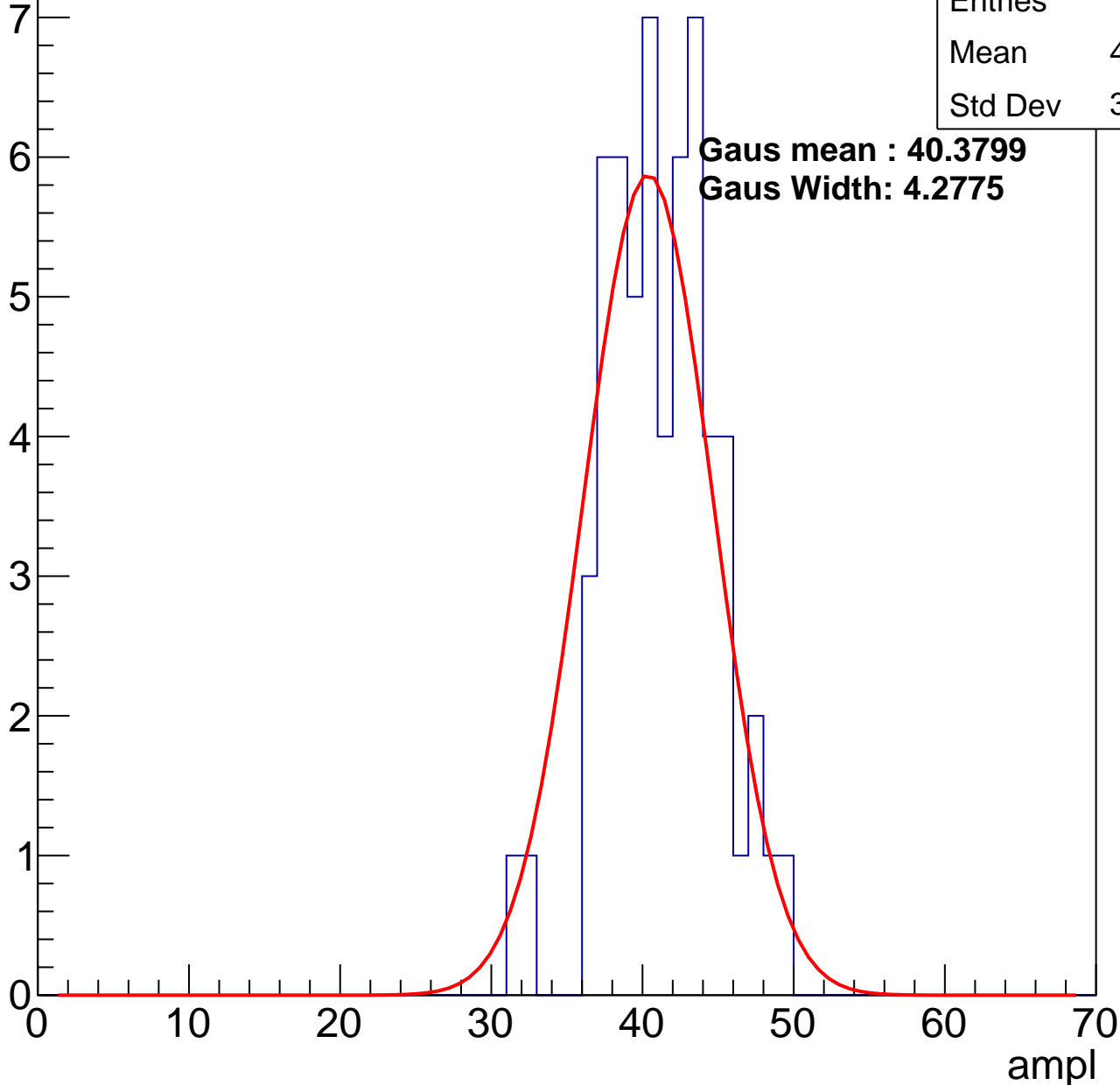
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	40.78
Std Dev	3.622

**Gaus mean : 40.3799**

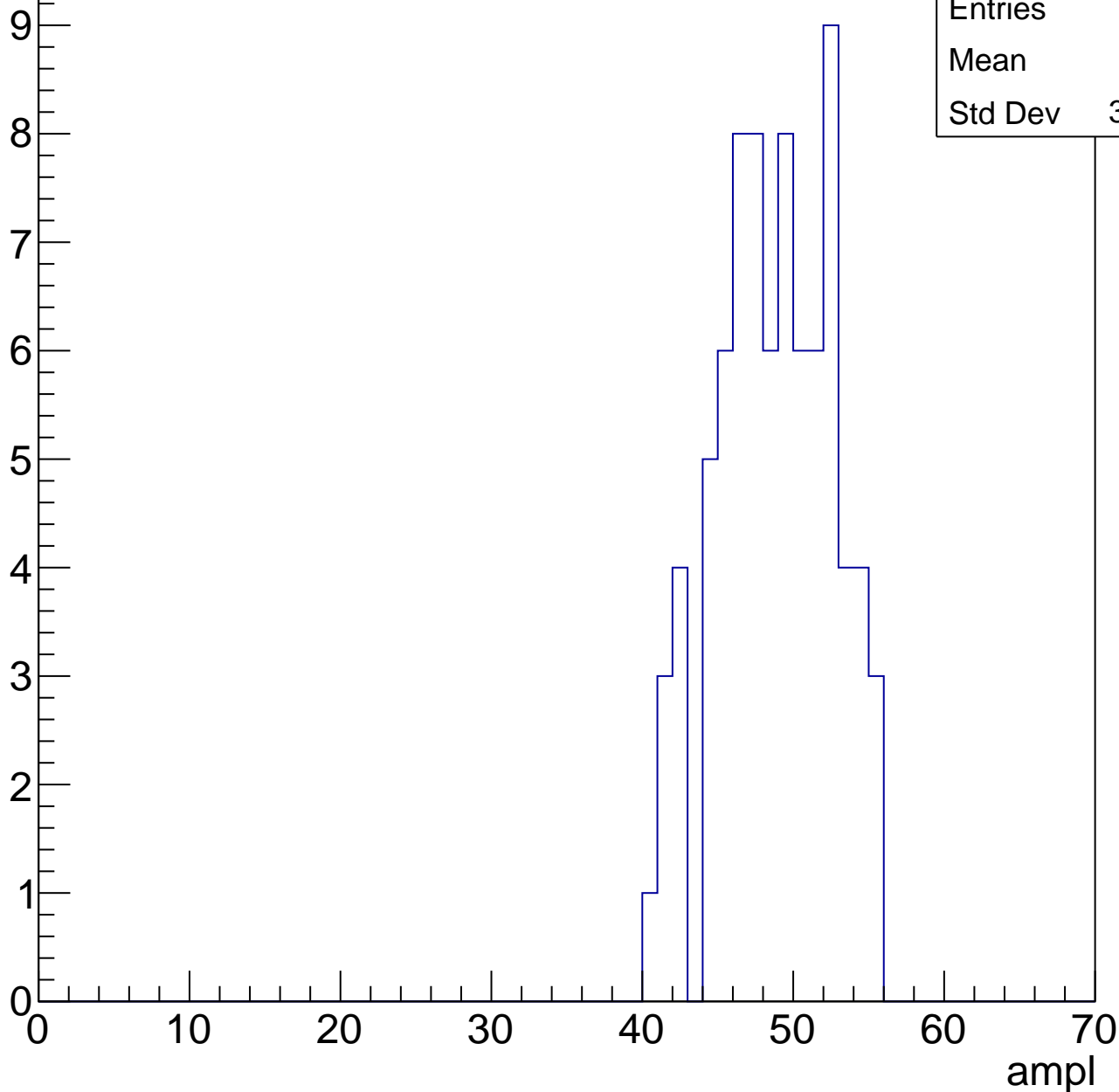
**Gaus Width: 4.2775**



# B1L103S, U3-ch80, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

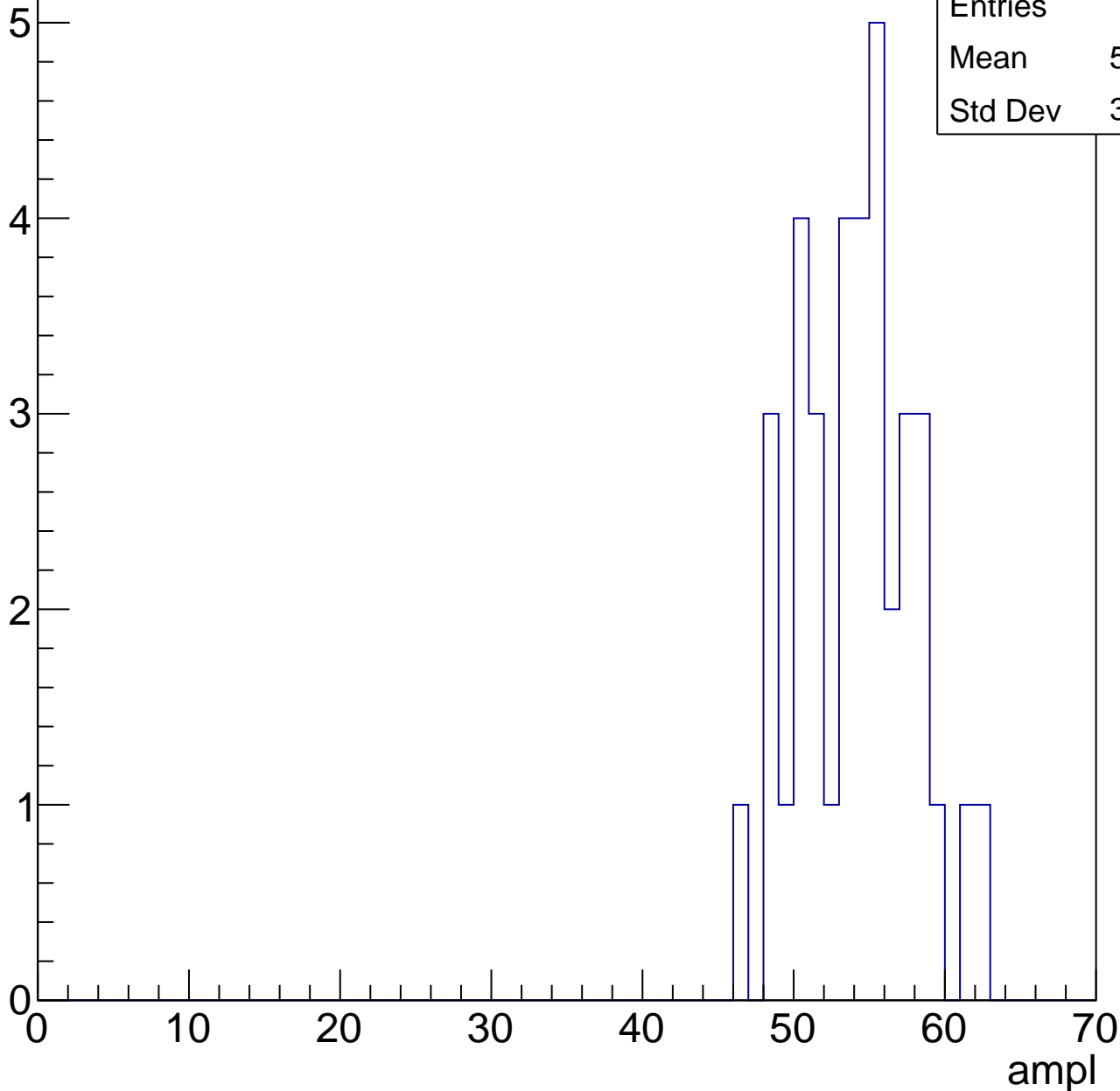


# B1L103S, U3-ch80, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	37
Mean	53.68
Std Dev	3.742

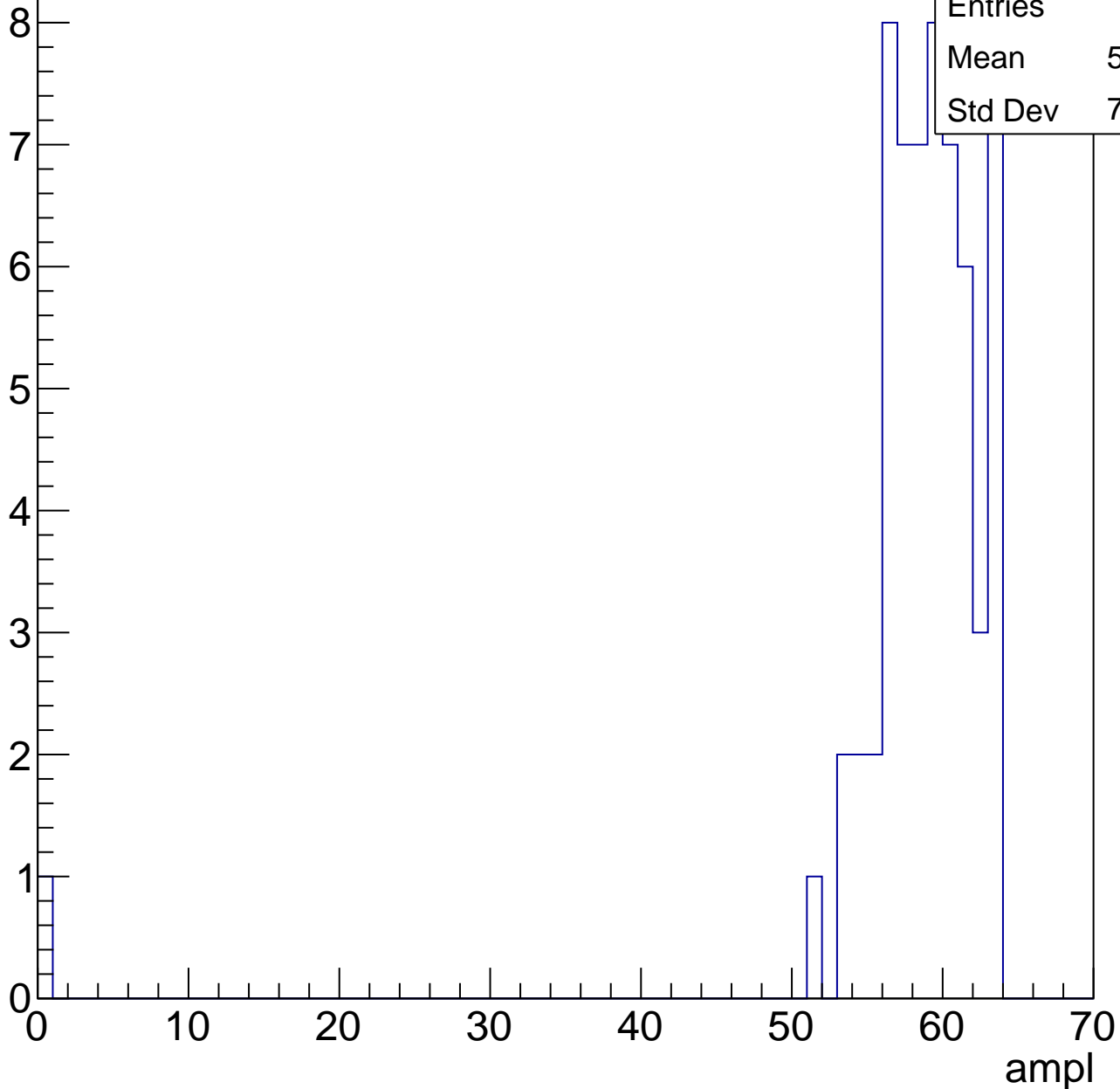


# B1L103S, U3-ch80, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	57.68
Std Dev	7.914

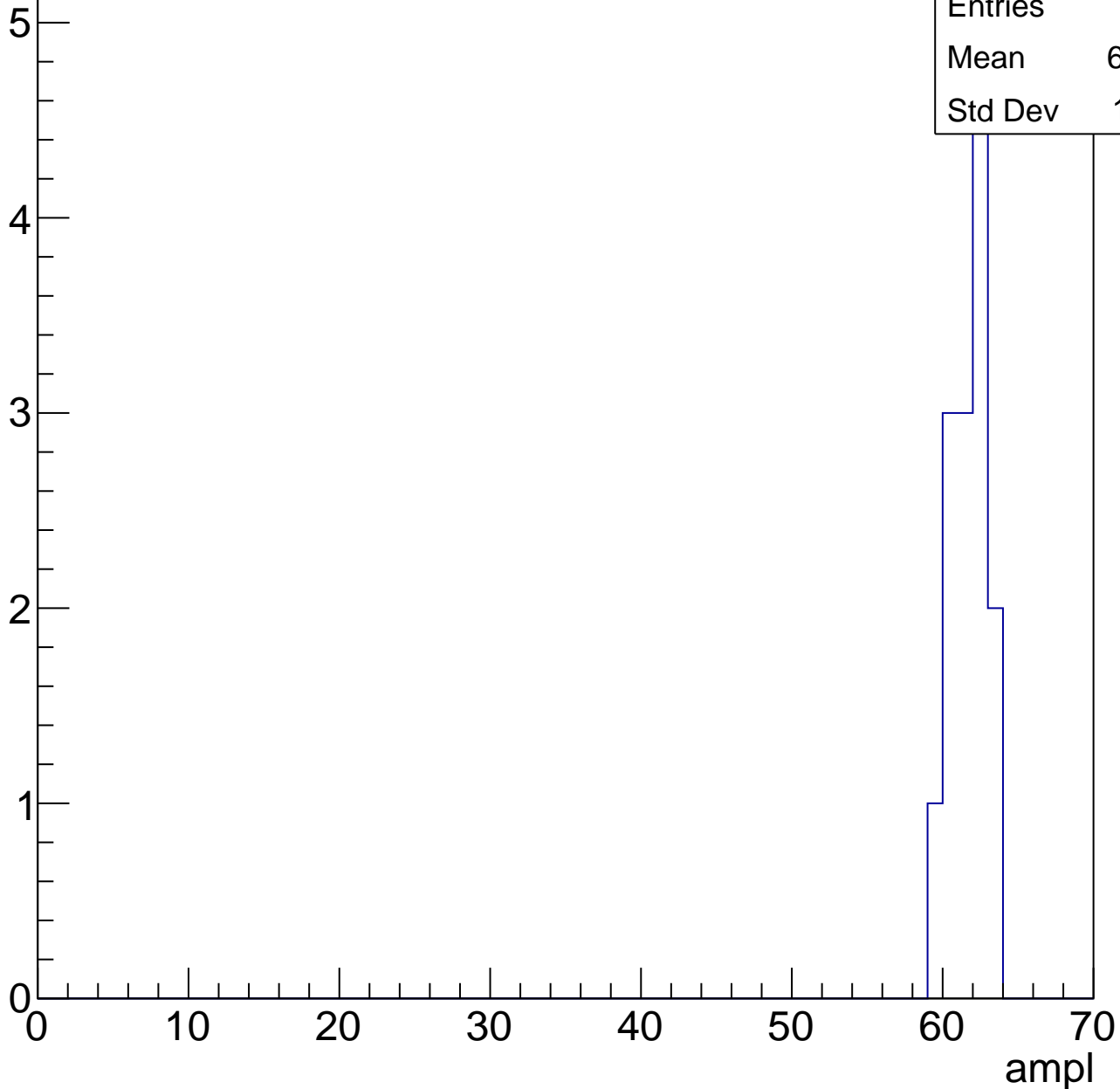


# B1L103S, U3-ch80, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	14
Mean	61.29
Std Dev	1.161





# B1L103S, U3-ch80, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch81, adc0

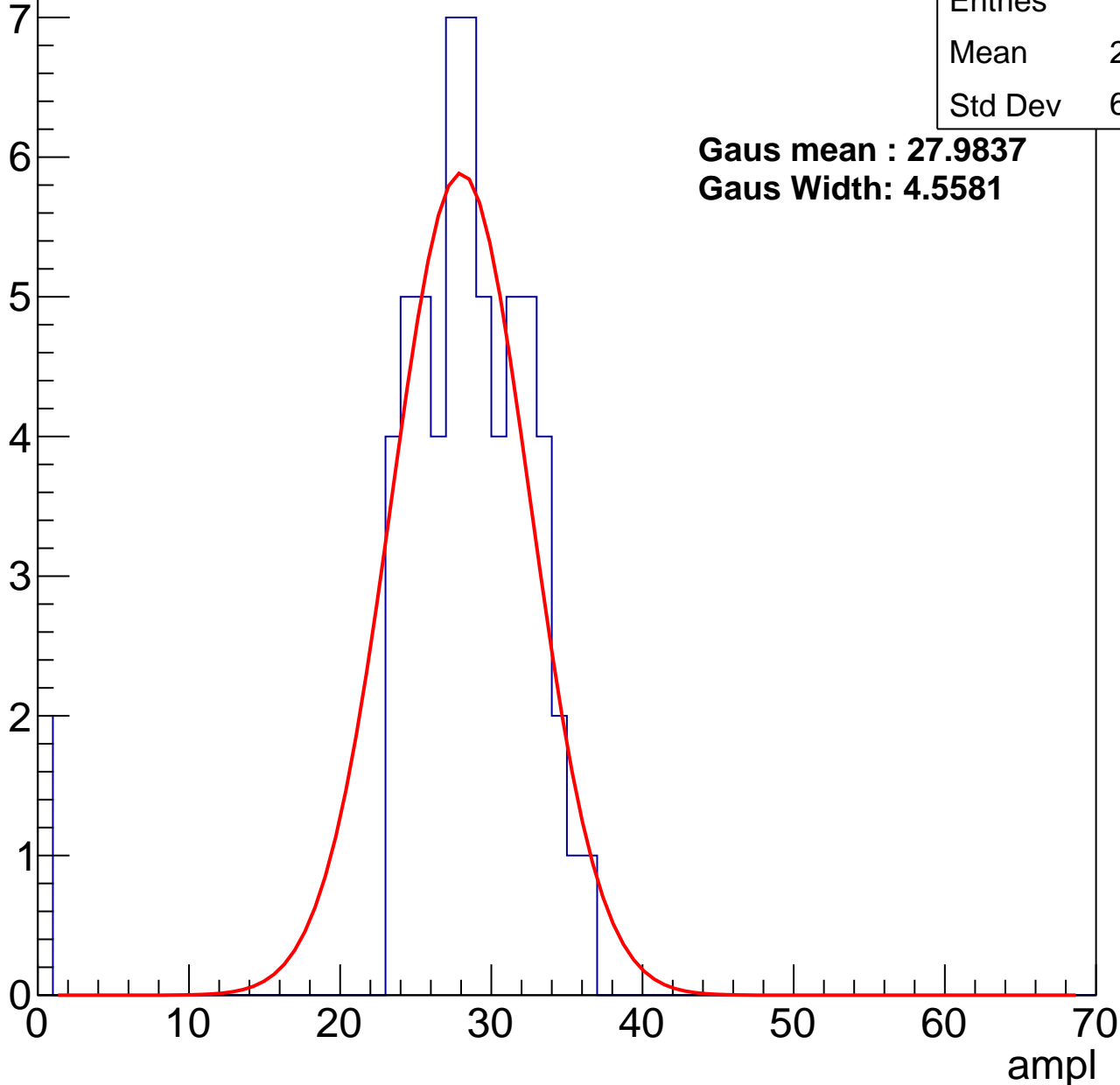
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	27.49
Std Dev	6.048

**Gaus mean : 27.9837**

**Gaus Width: 4.5581**



# B1L103S, U3-ch81, adc1

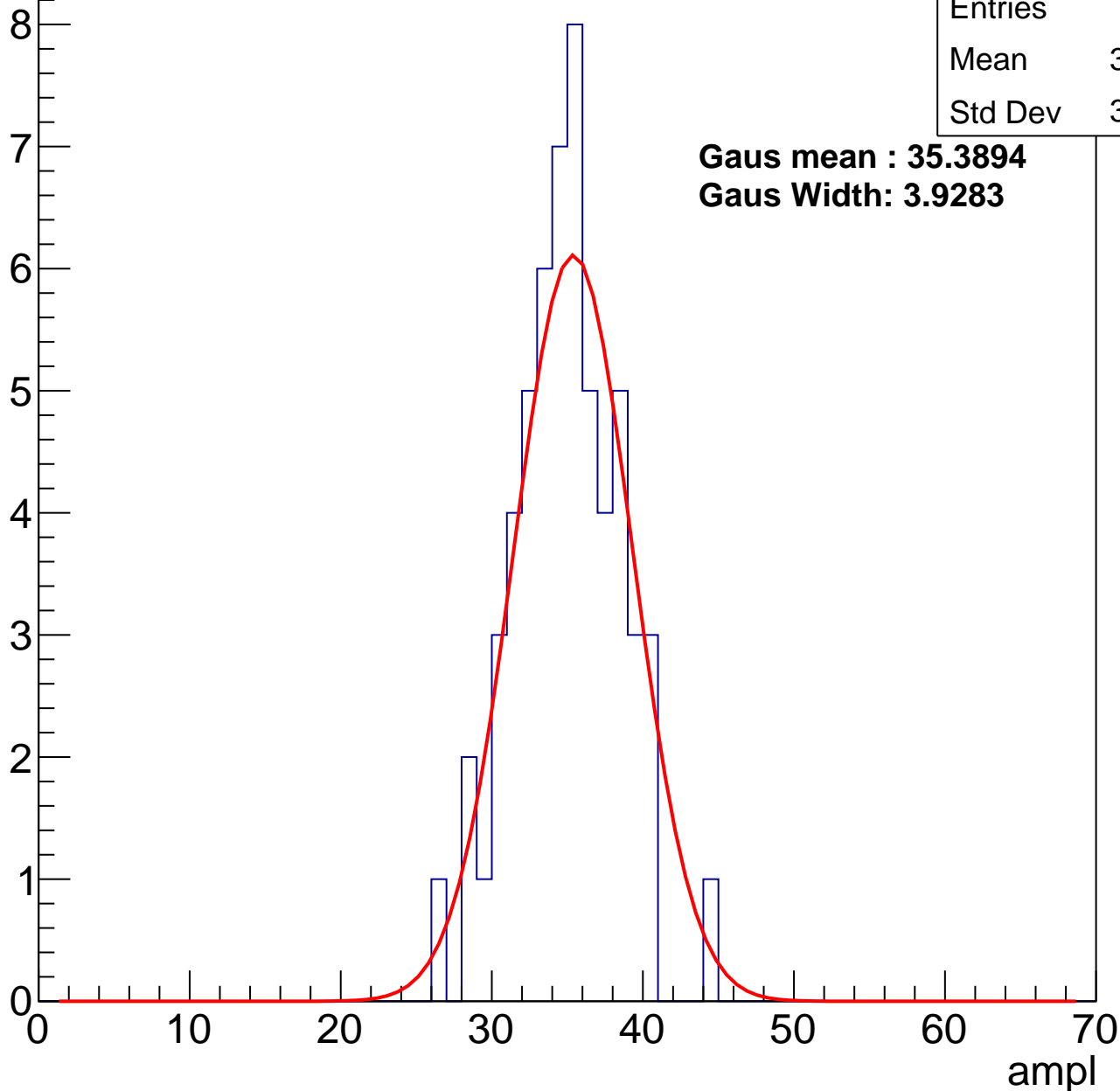
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	34.48
Std Dev	3.435

**Gaus mean : 35.3894**

**Gaus Width: 3.9283**



# B1L103S, U3-ch81, adc2

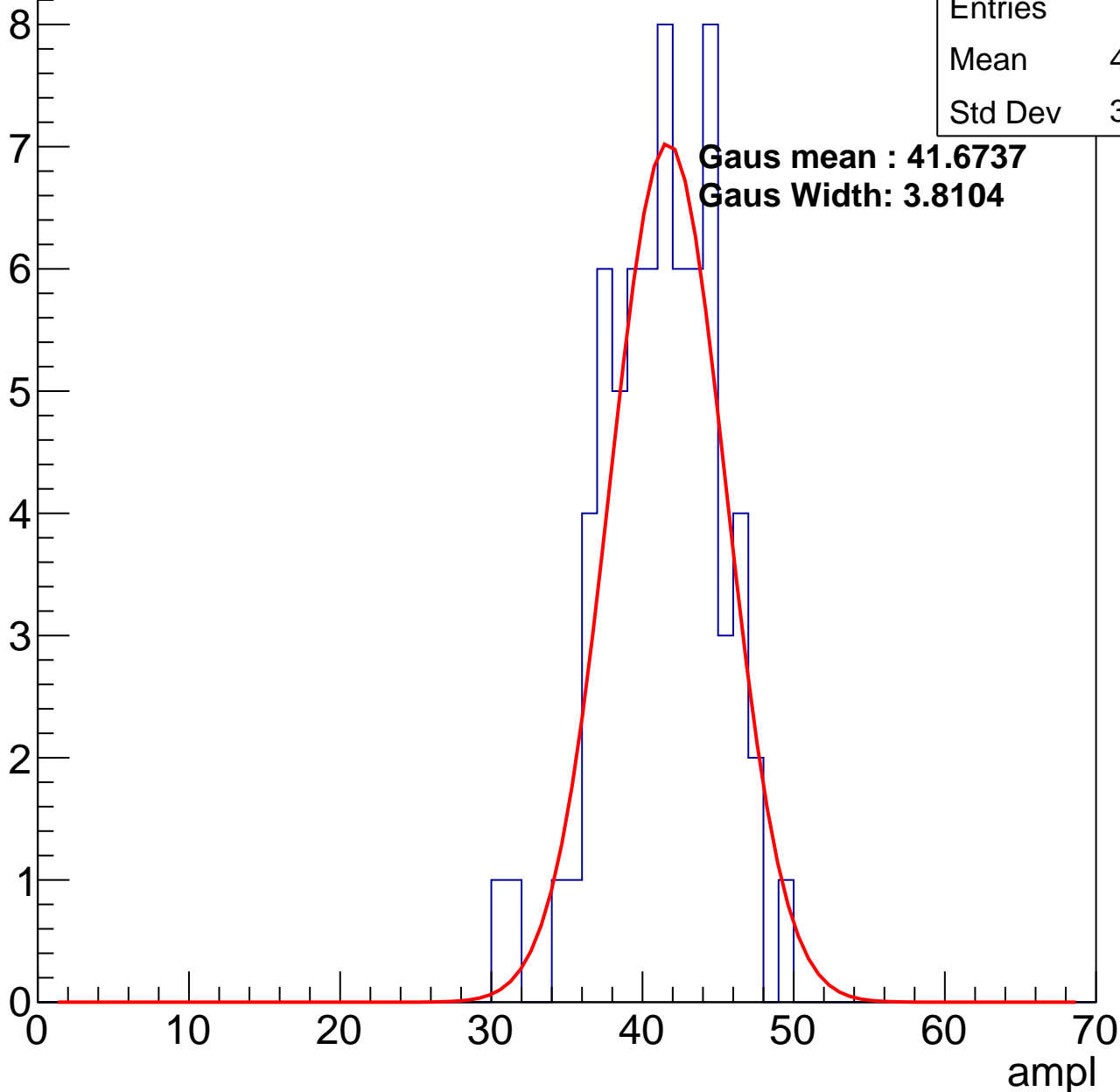
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	40.75
Std Dev	3.728

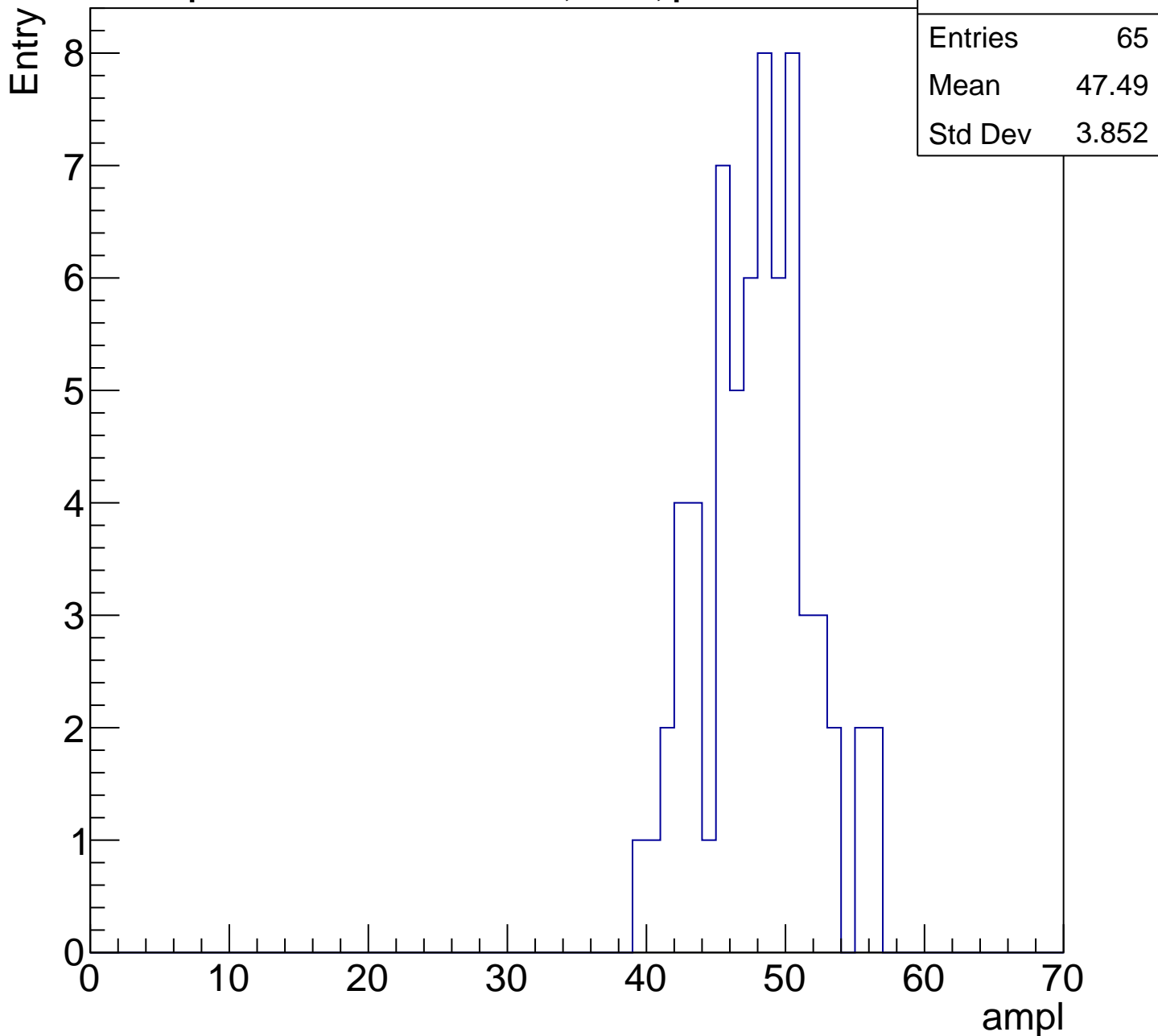
**Gaus mean : 41.6737**

**Gaus Width: 3.8104**



# B1L103S, U3-ch81, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

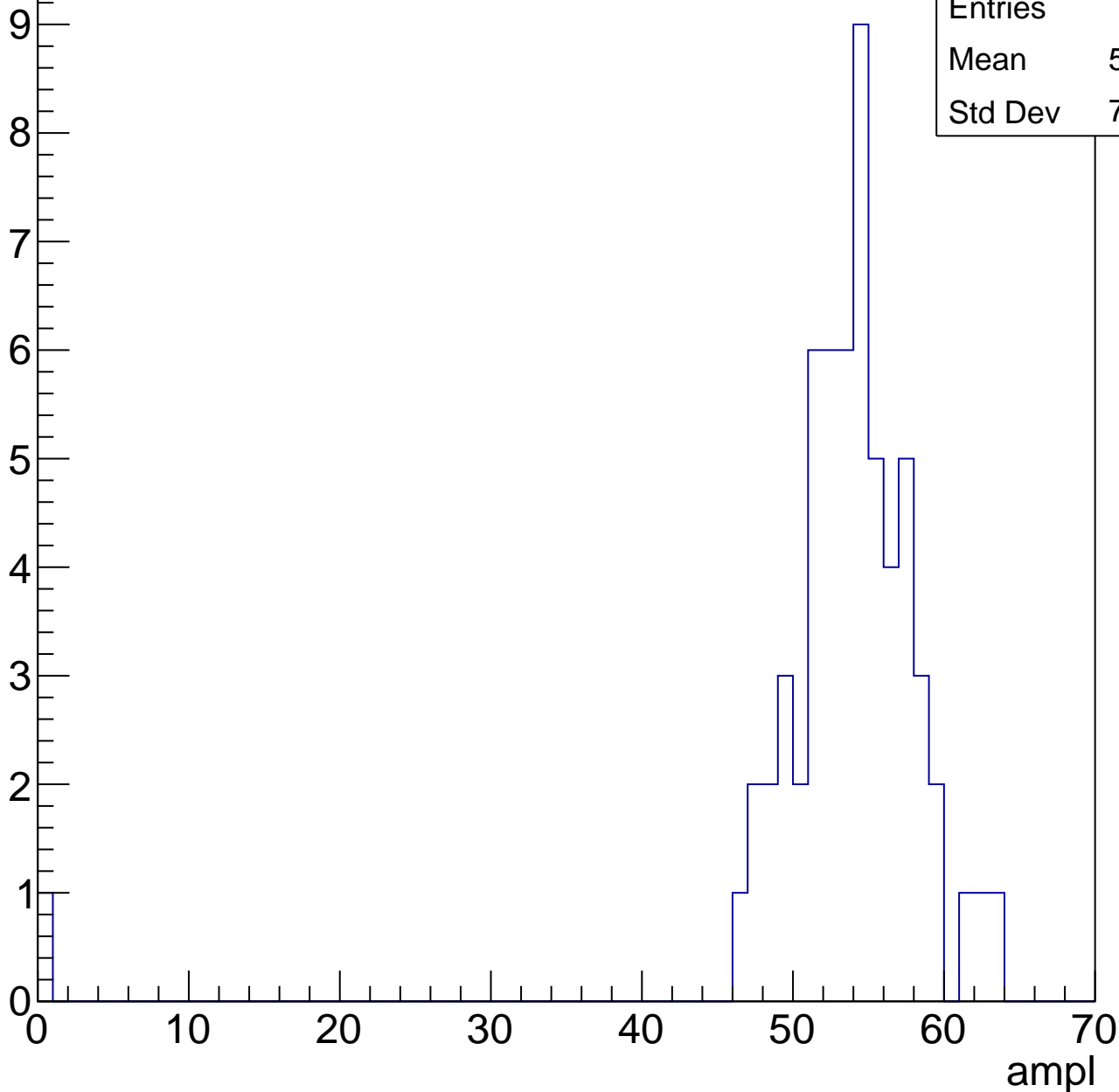


# B1L103S, U3-ch81, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

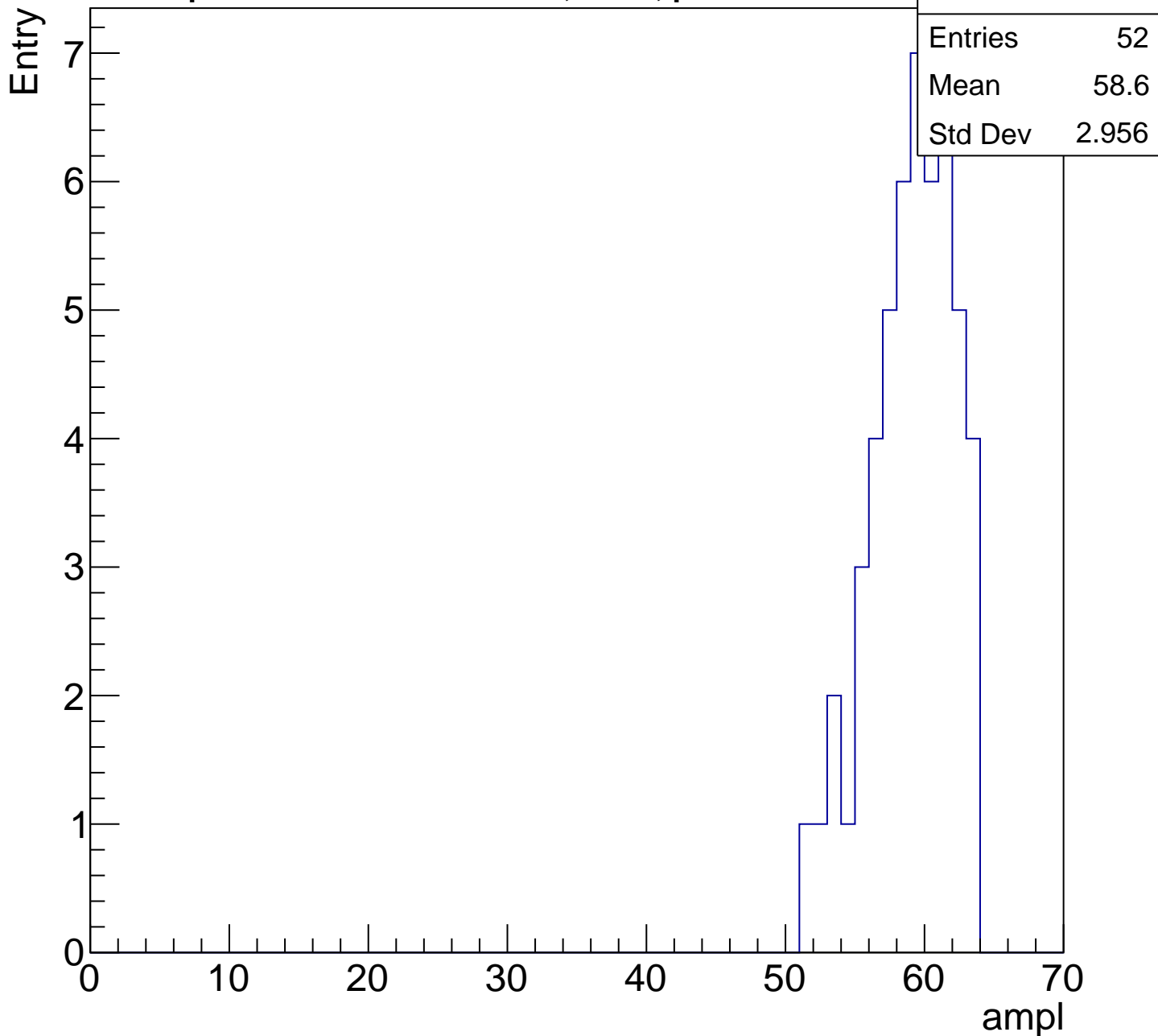
Entry

Entries	60
Mean	52.78
Std Dev	7.757



# B1L103S, U3-ch81, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

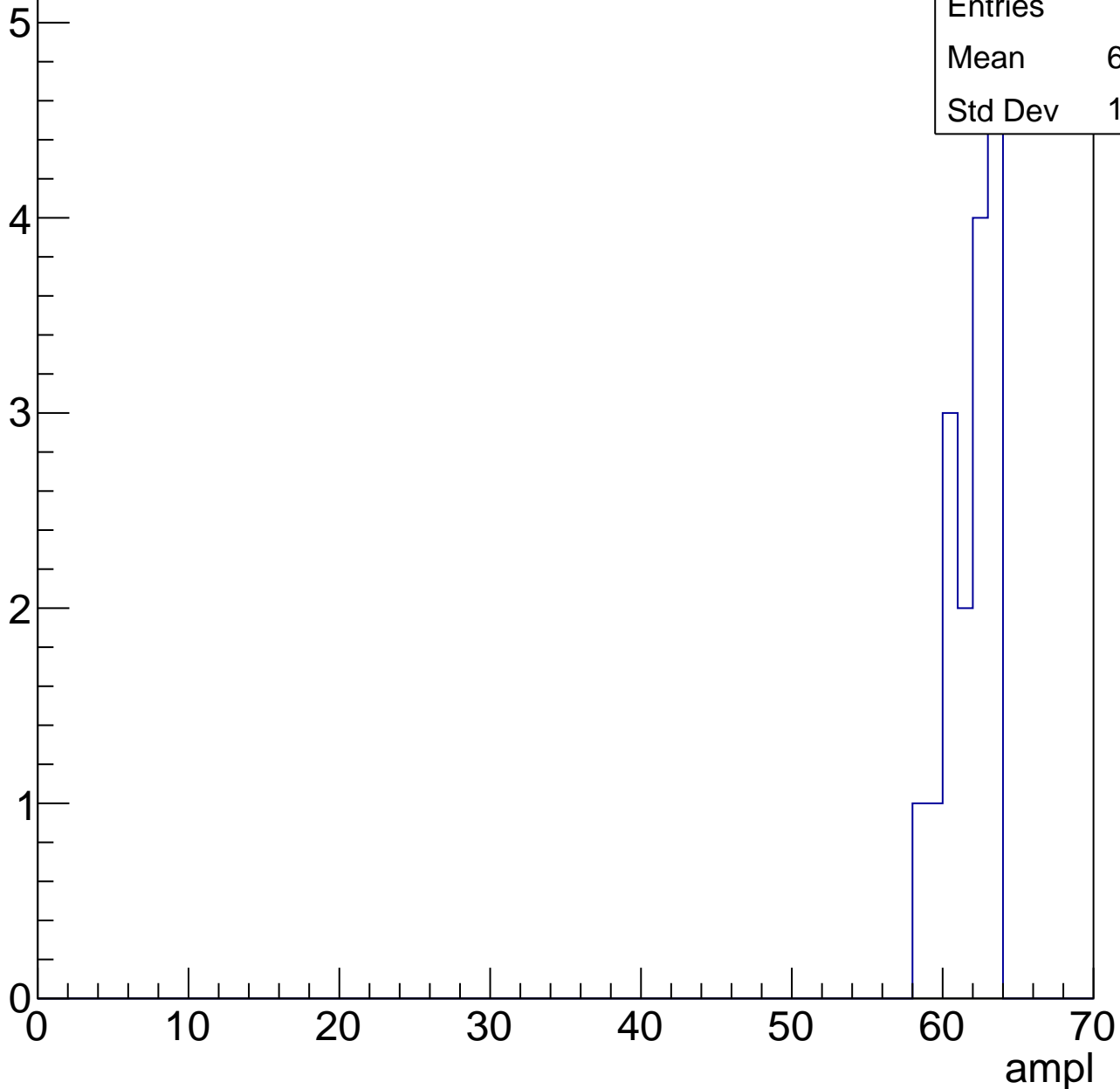


# B1L103S, U3-ch81, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	16
Mean	61.38
Std Dev	1.536

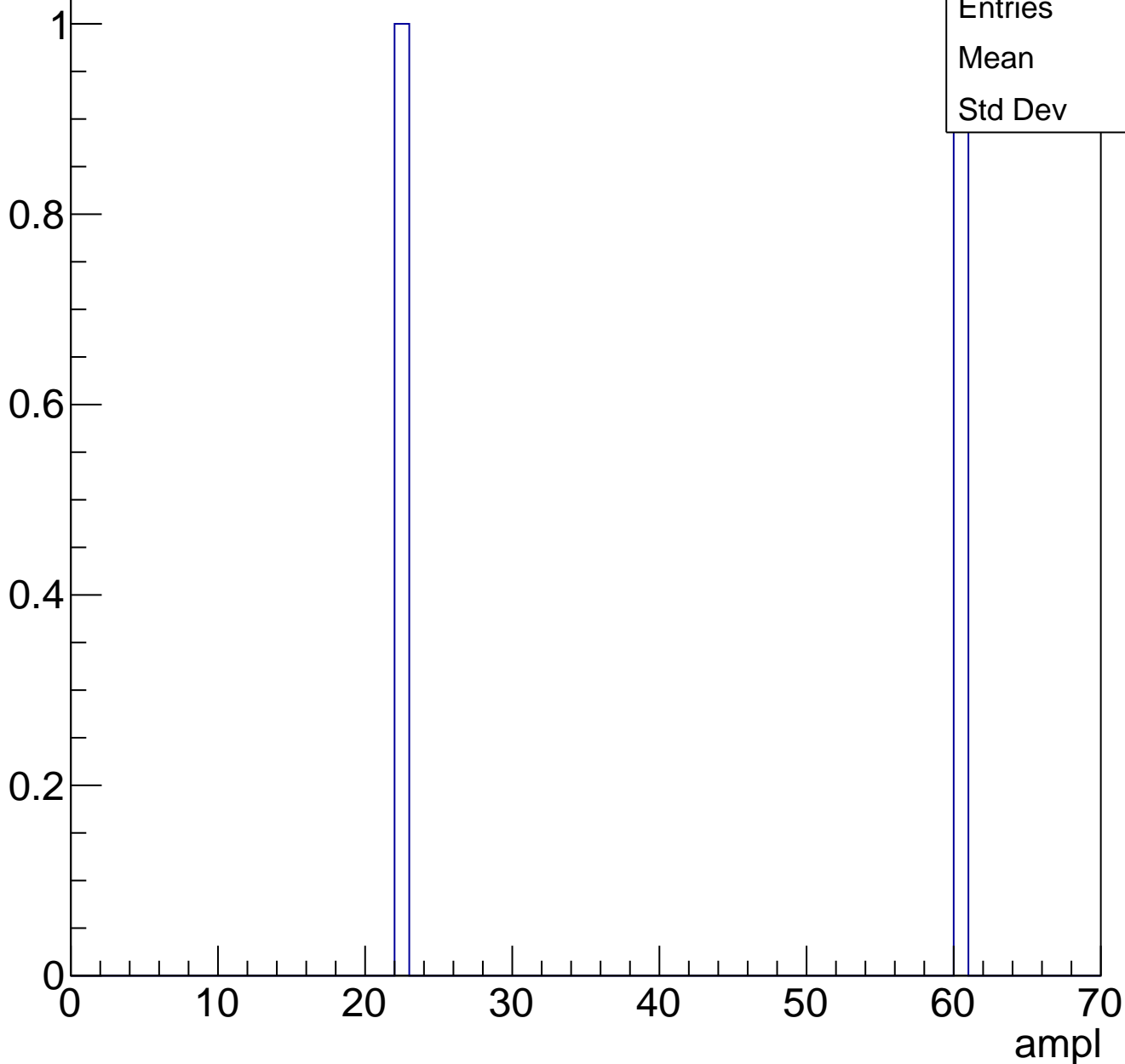




# B1L103S, U3-ch81, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch82, adc0

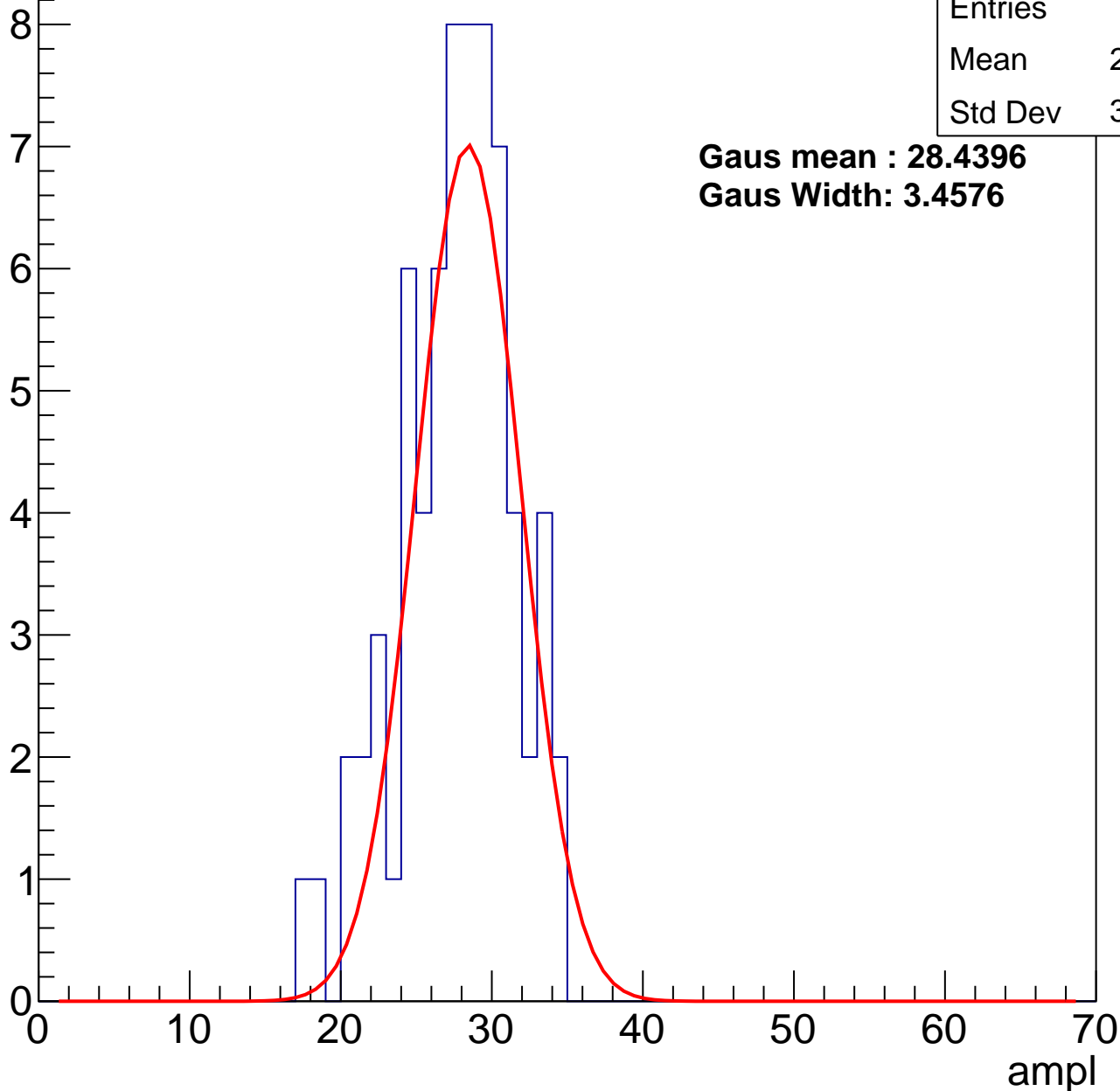
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	27.19
Std Dev	3.758

**Gaus mean : 28.4396**

**Gaus Width: 3.4576**



# B1L103S, U3-ch82, adc1

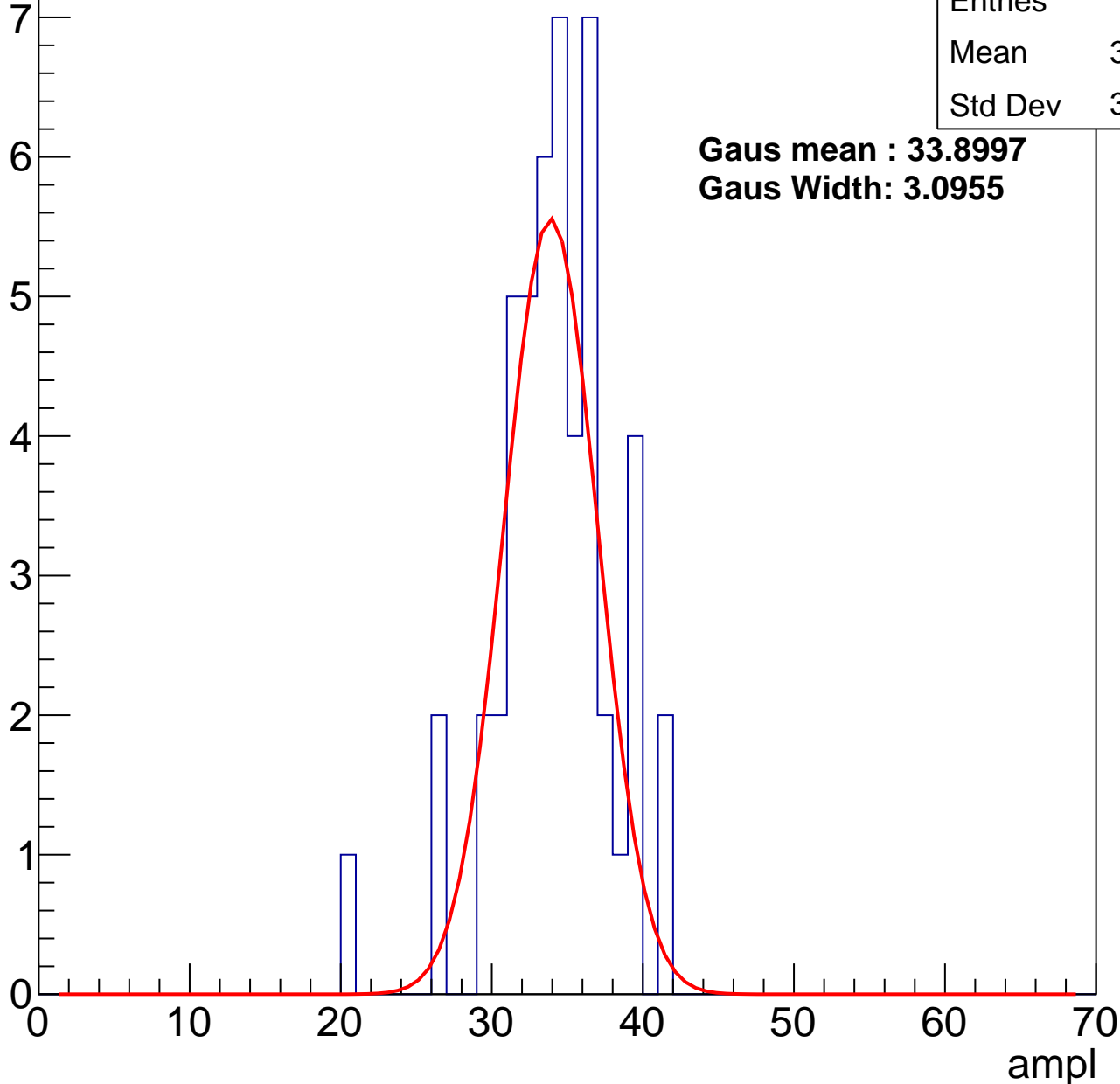
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	33.66
Std Dev	3.835

**Gaus mean : 33.8997**

**Gaus Width: 3.0955**



# B1L103S, U3-ch82, adc2

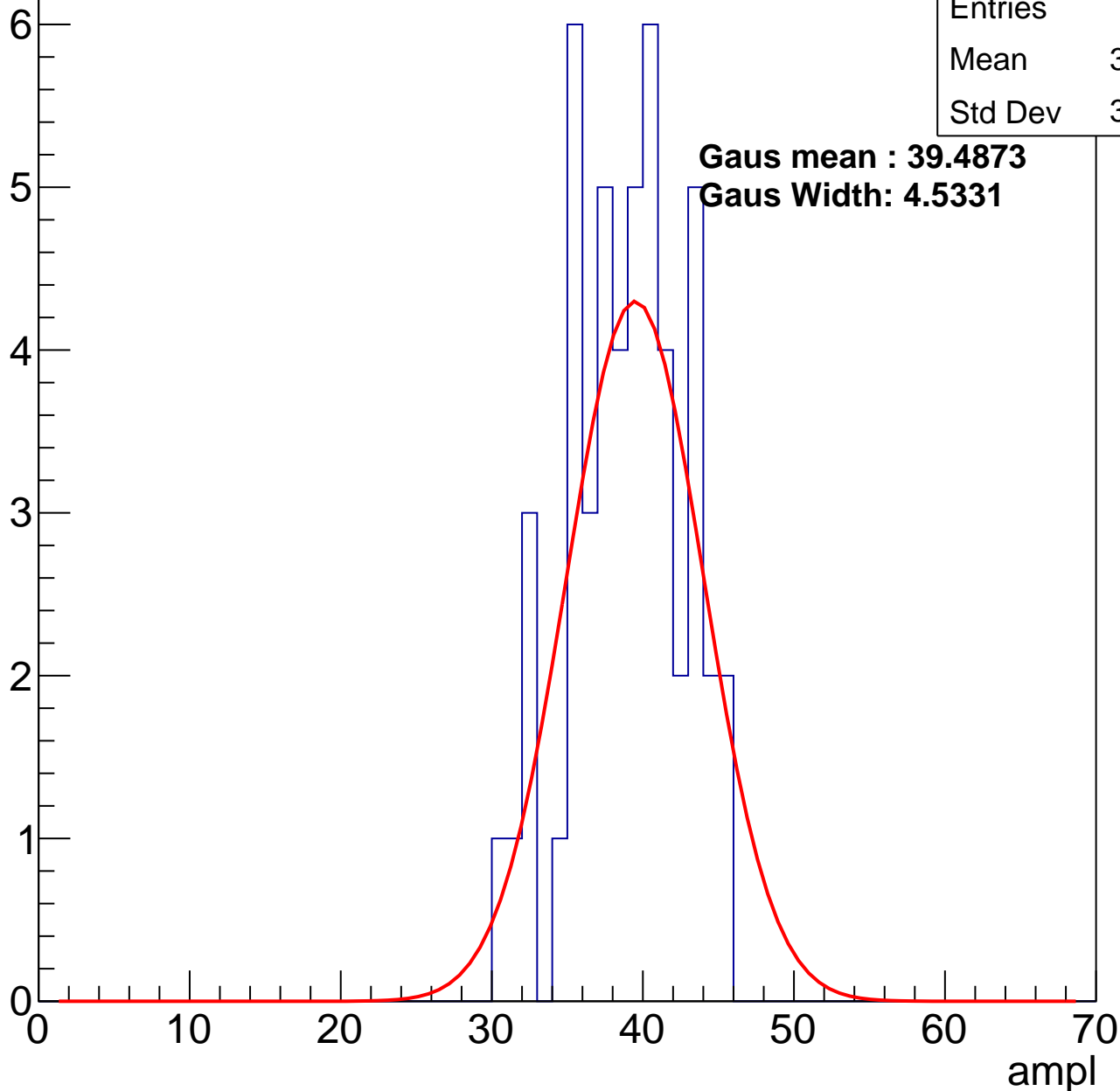
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	38.44
Std Dev	3.716

**Gaus mean : 39.4873**

**Gaus Width: 4.5331**

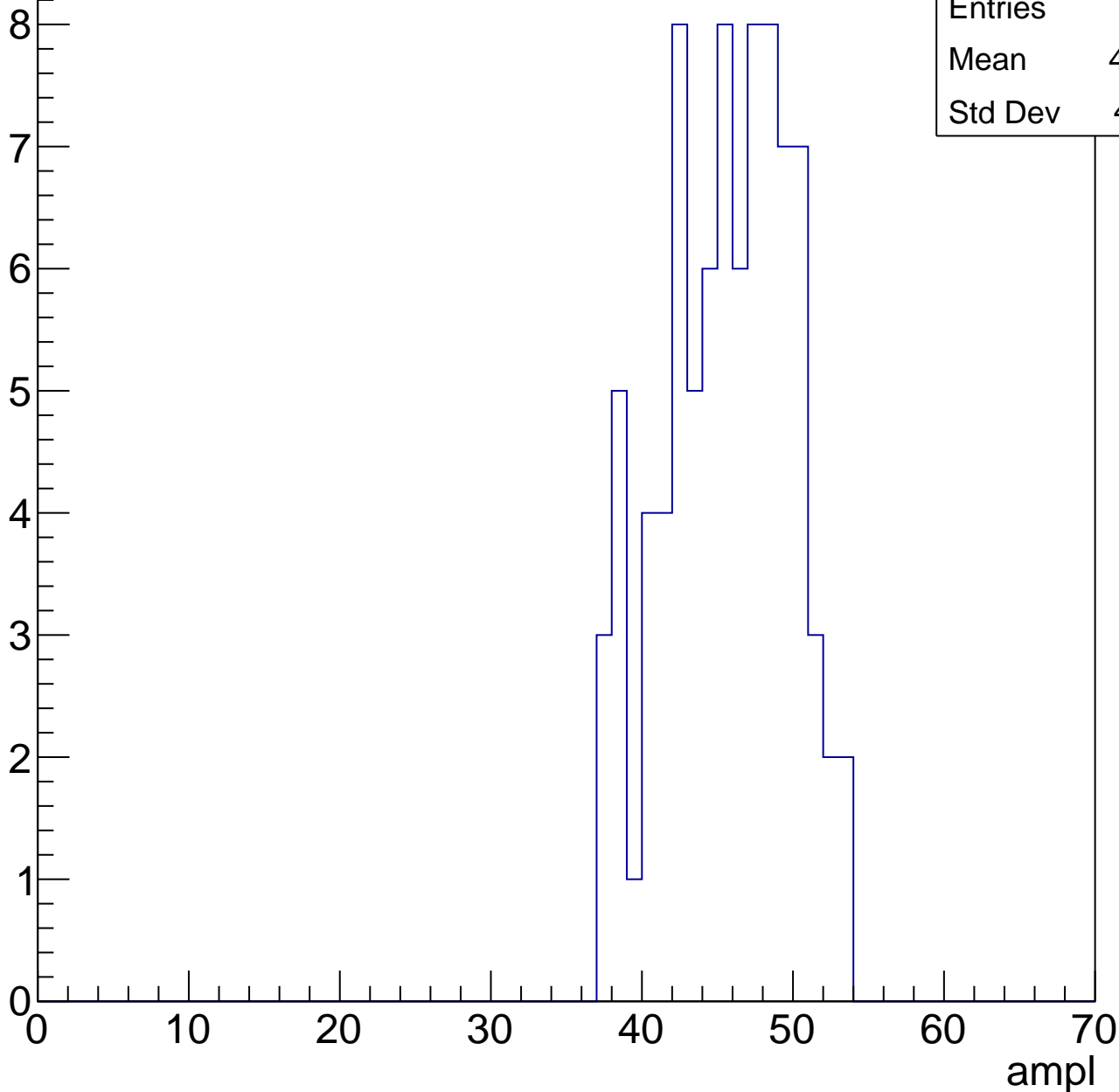


# B1L103S, U3-ch82, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

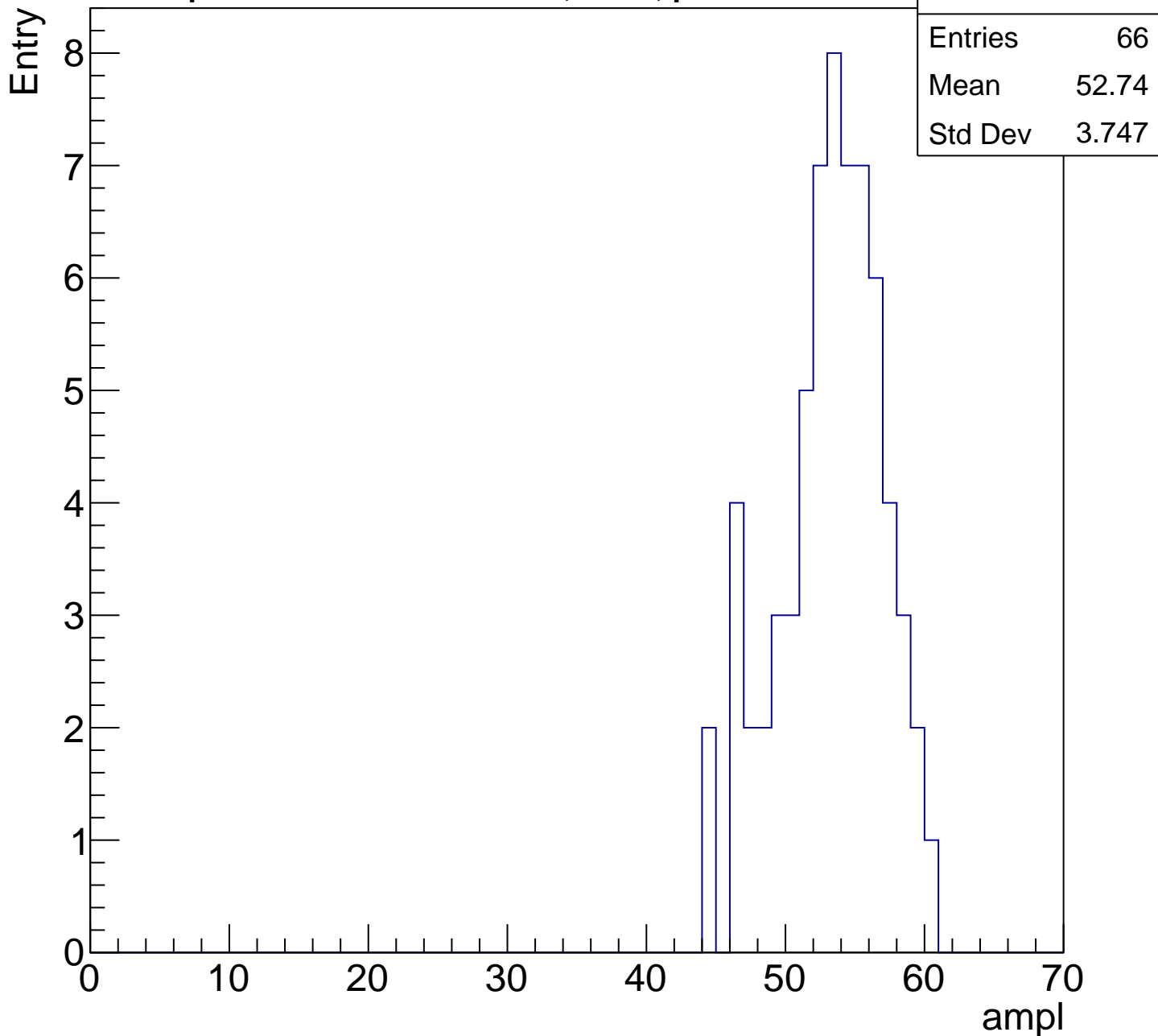
Entry

Entries	87
Mean	45.18
Std Dev	4.101



# B1L103S, U3-ch82, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U3-ch82, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

6

5

4

3

2

1

0

0

10

20

30

40

50

60

70

ampl

Entries	39
Mean	58.1
Std Dev	3.136

6

5

4

3

2

1

0

0

10

20

30

40

50

60

70

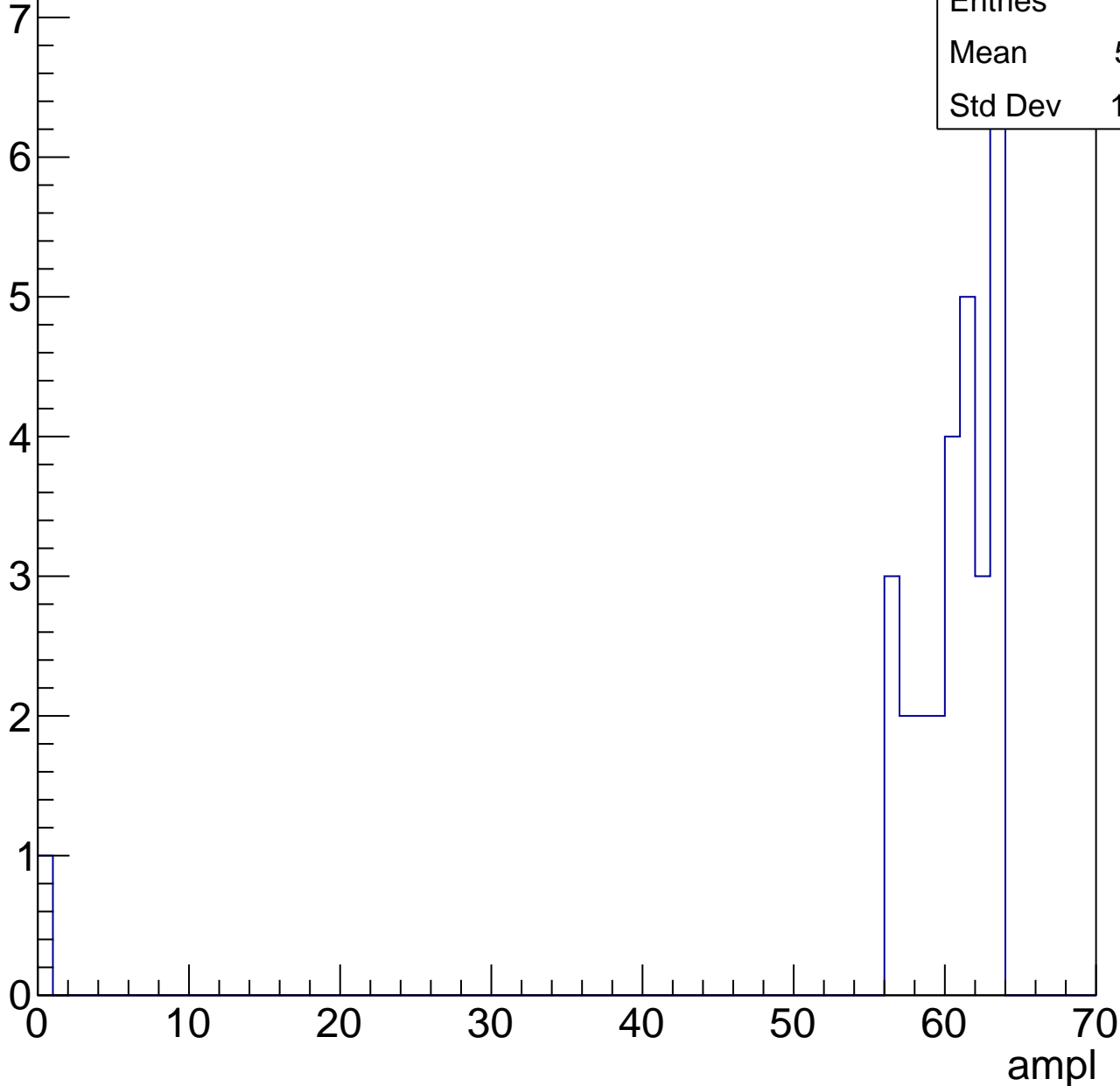
ampl

# B1L103S, U3-ch82, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	29
Mean	58.21
Std Dev	11.24

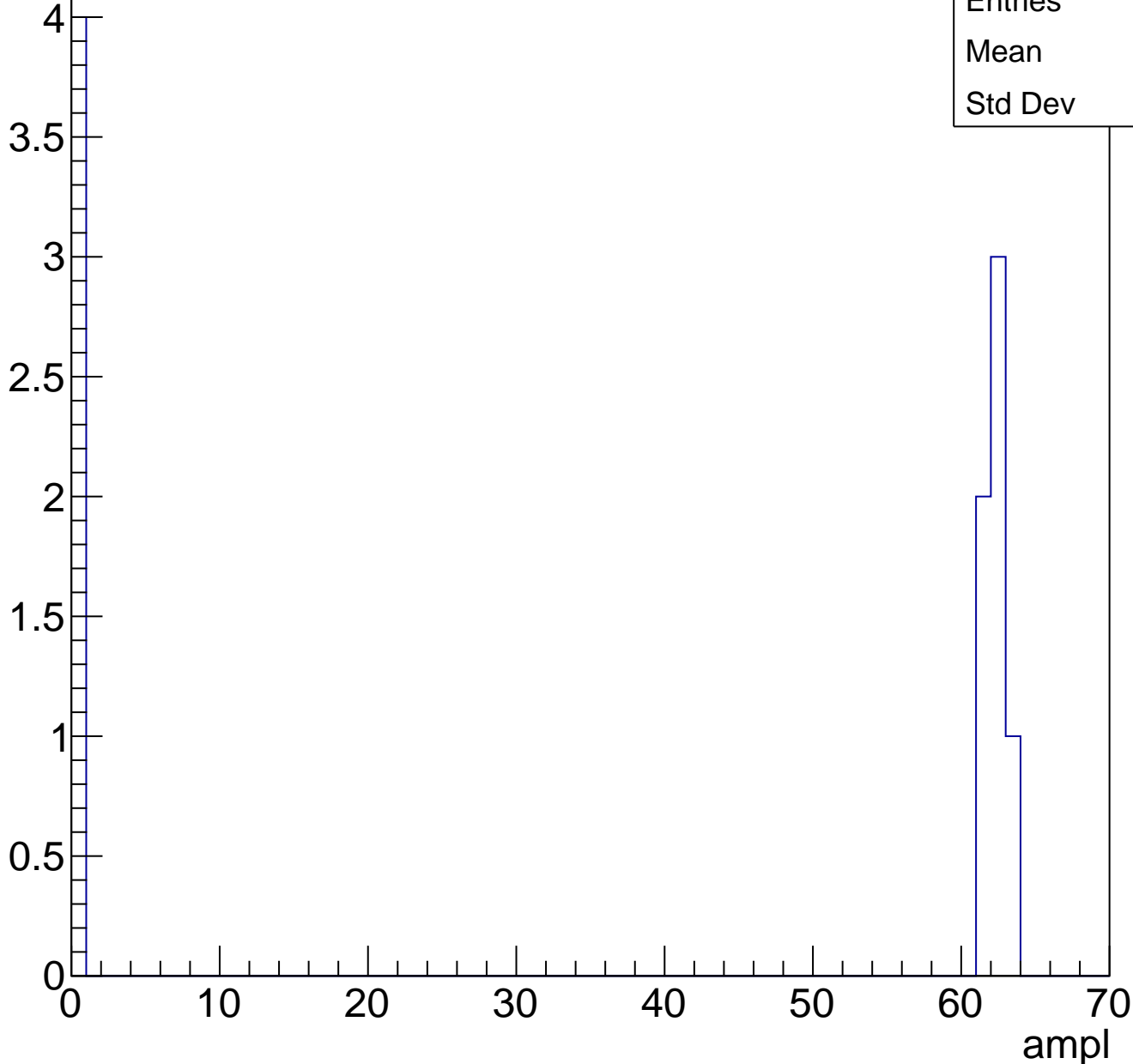




# B1L103S, U3-ch82, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	10
Mean	37.1
Std Dev	30.3

# B1L103S, U3-ch83, adc0

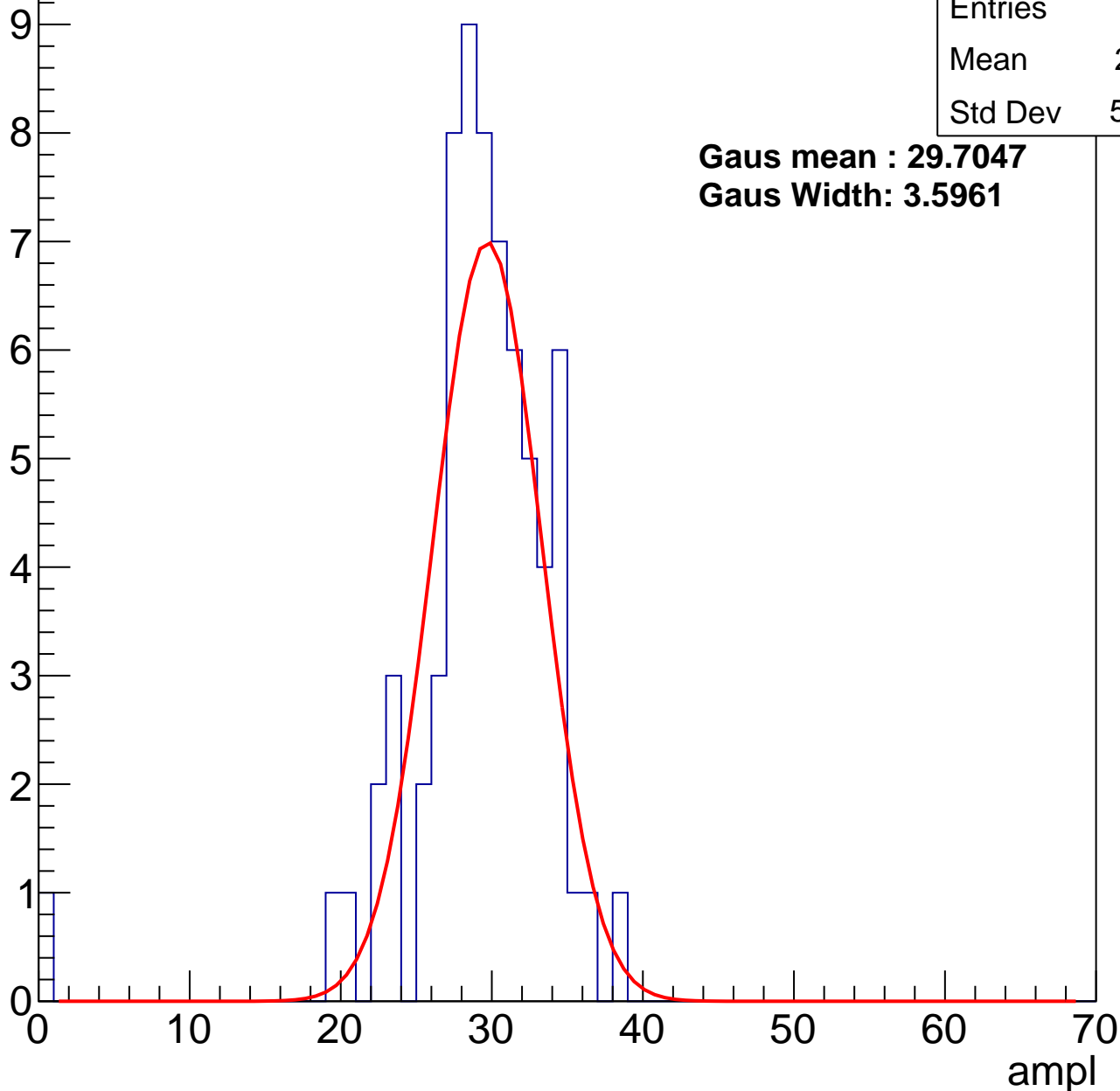
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	28.71
Std Dev	5.077

**Gaus mean : 29.7047**

**Gaus Width: 3.5961**



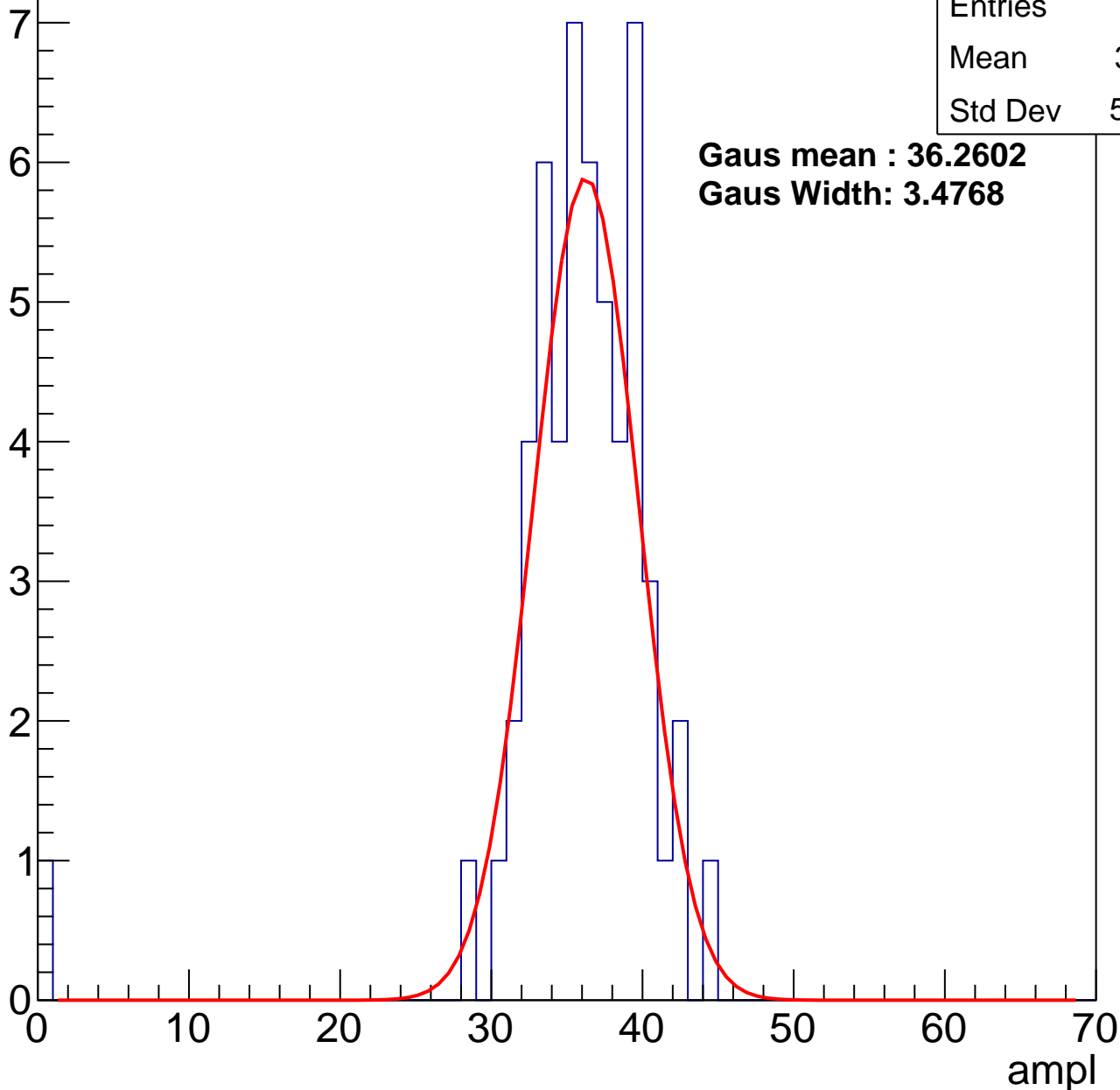
# B1L103S, U3-ch83, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

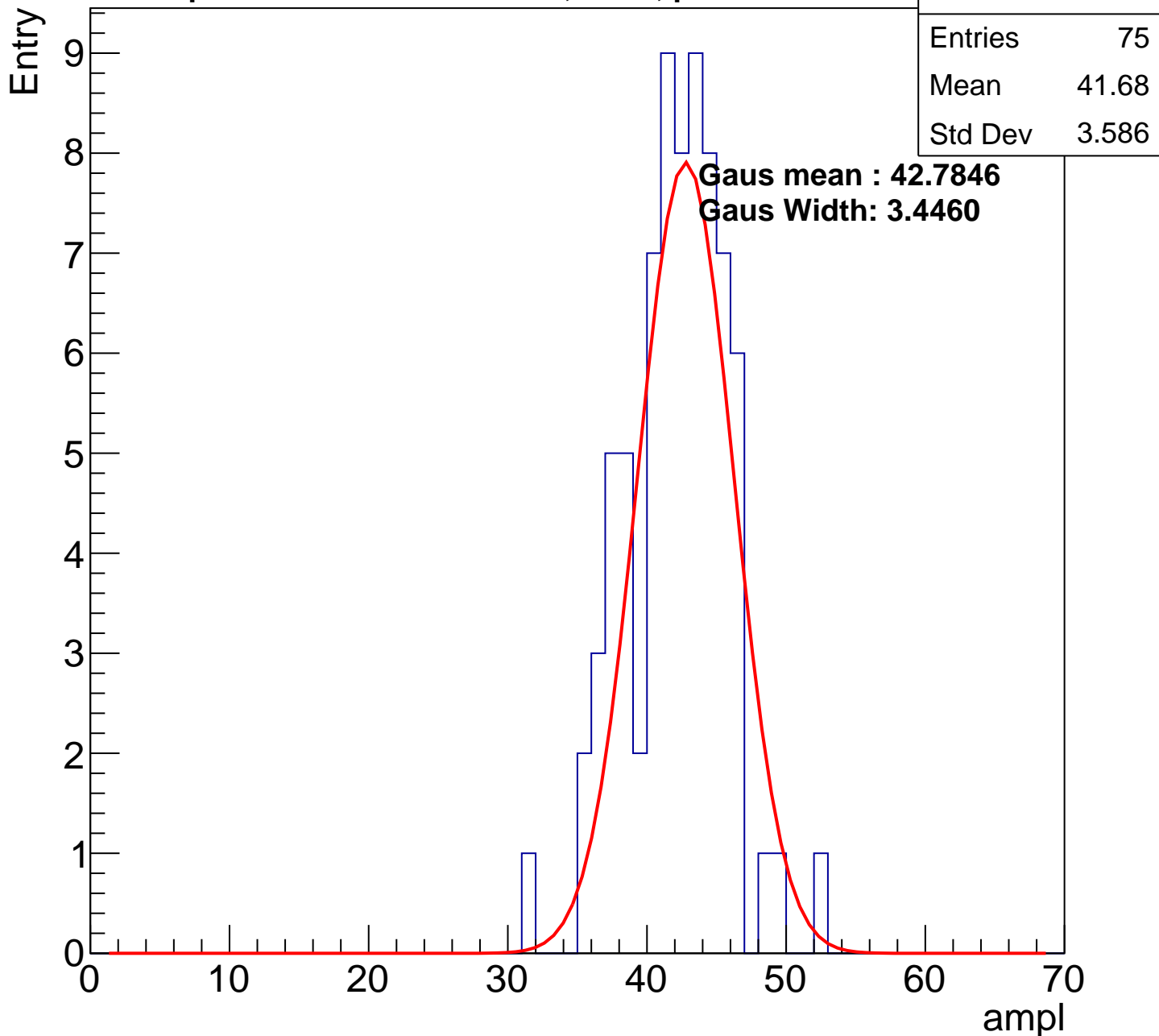
Entries	55
Mean	35.31
Std Dev	5.806

**Gaus mean : 36.2602**  
**Gaus Width: 3.4768**



# B1L103S, U3-ch83, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

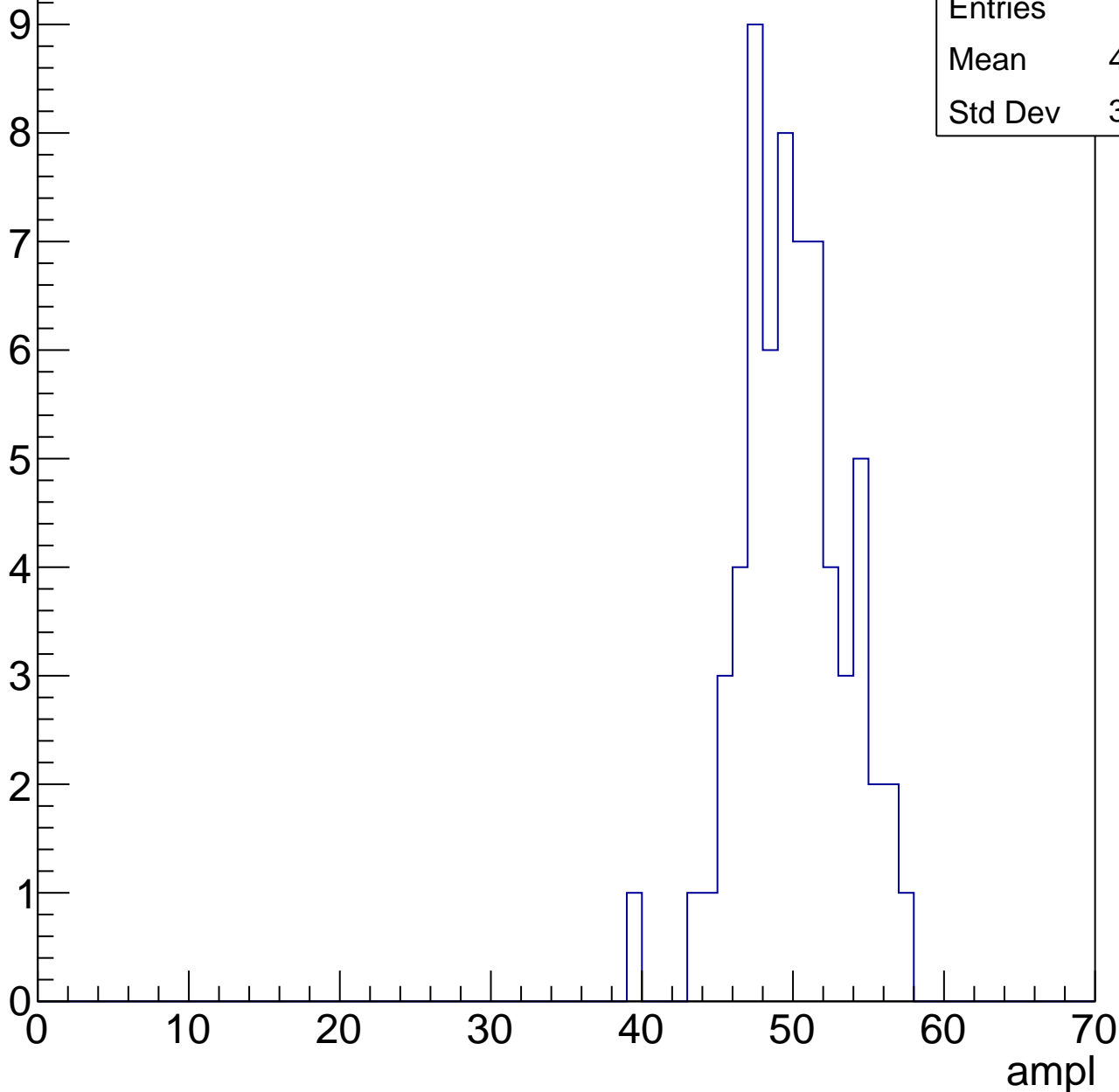


# B1L103S, U3-ch83, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

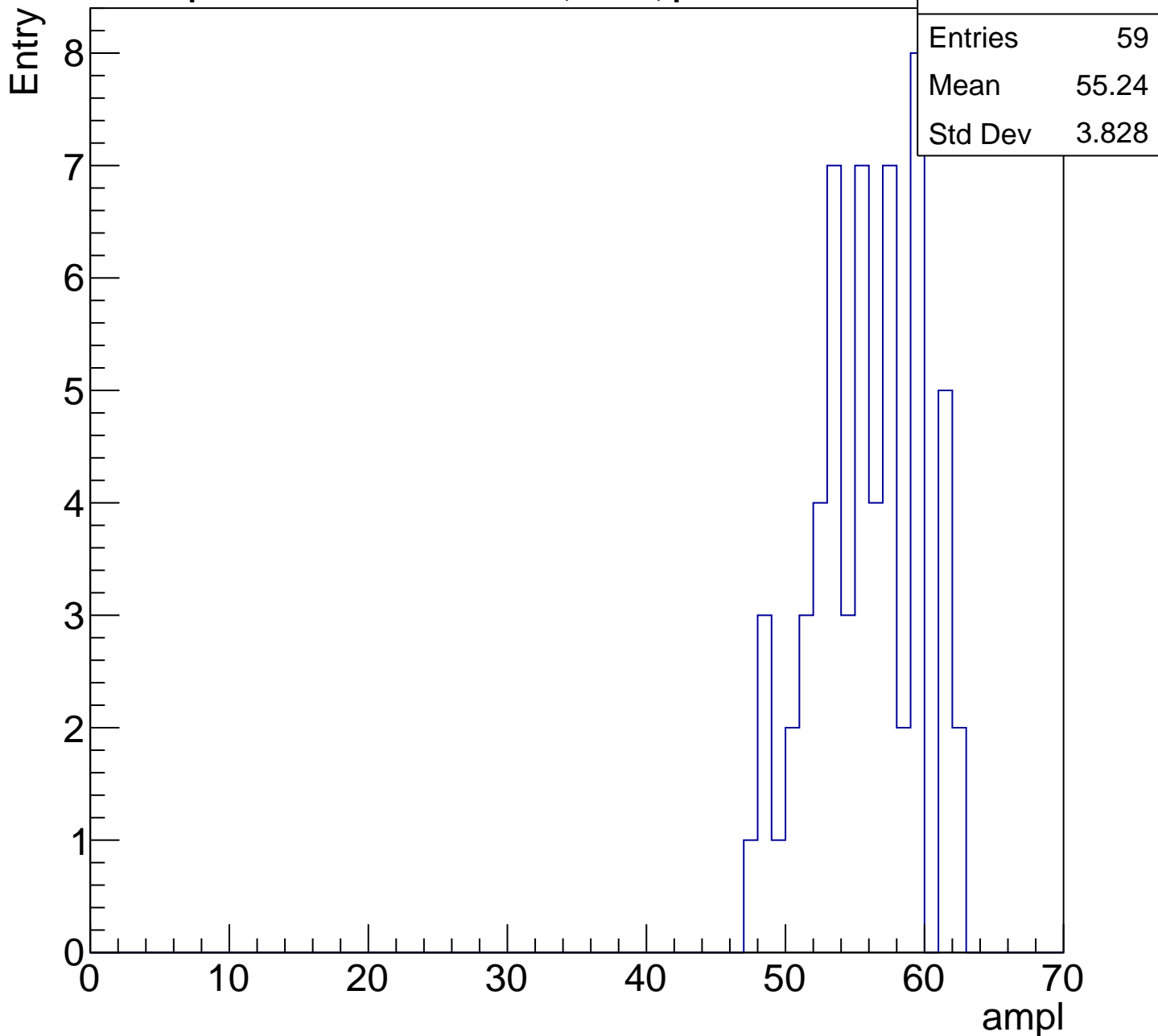
Entry

Entries	64
Mean	49.55
Std Dev	3.414



# B1L103S, U3-ch83, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

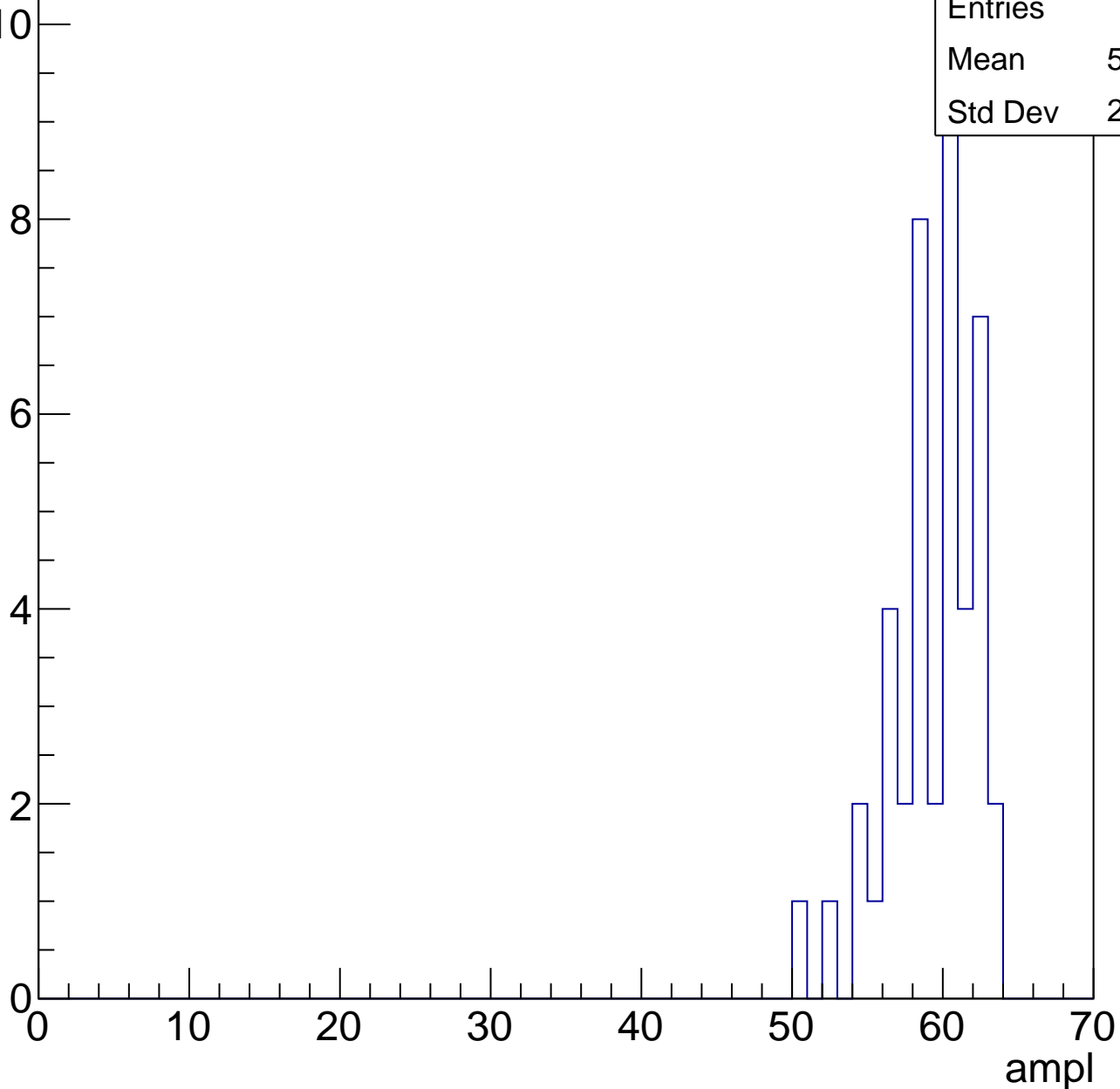


# B1L103S, U3-ch83, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	44
Mean	58.84
Std Dev	2.892

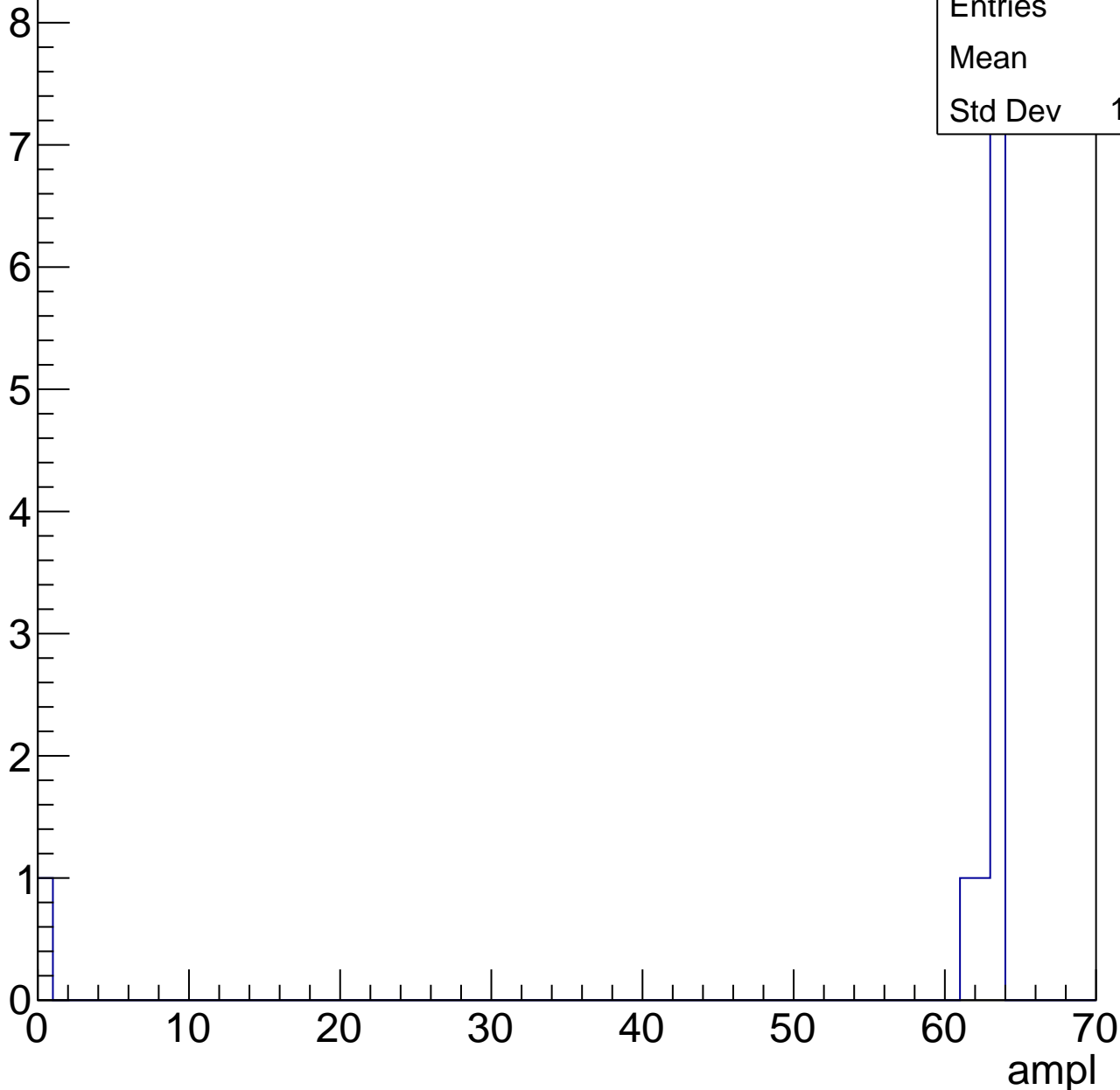


# B1L103S, U3-ch83, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	11
Mean	57
Std Dev	18.04





# B1L103S, U3-ch83, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch84, adc0

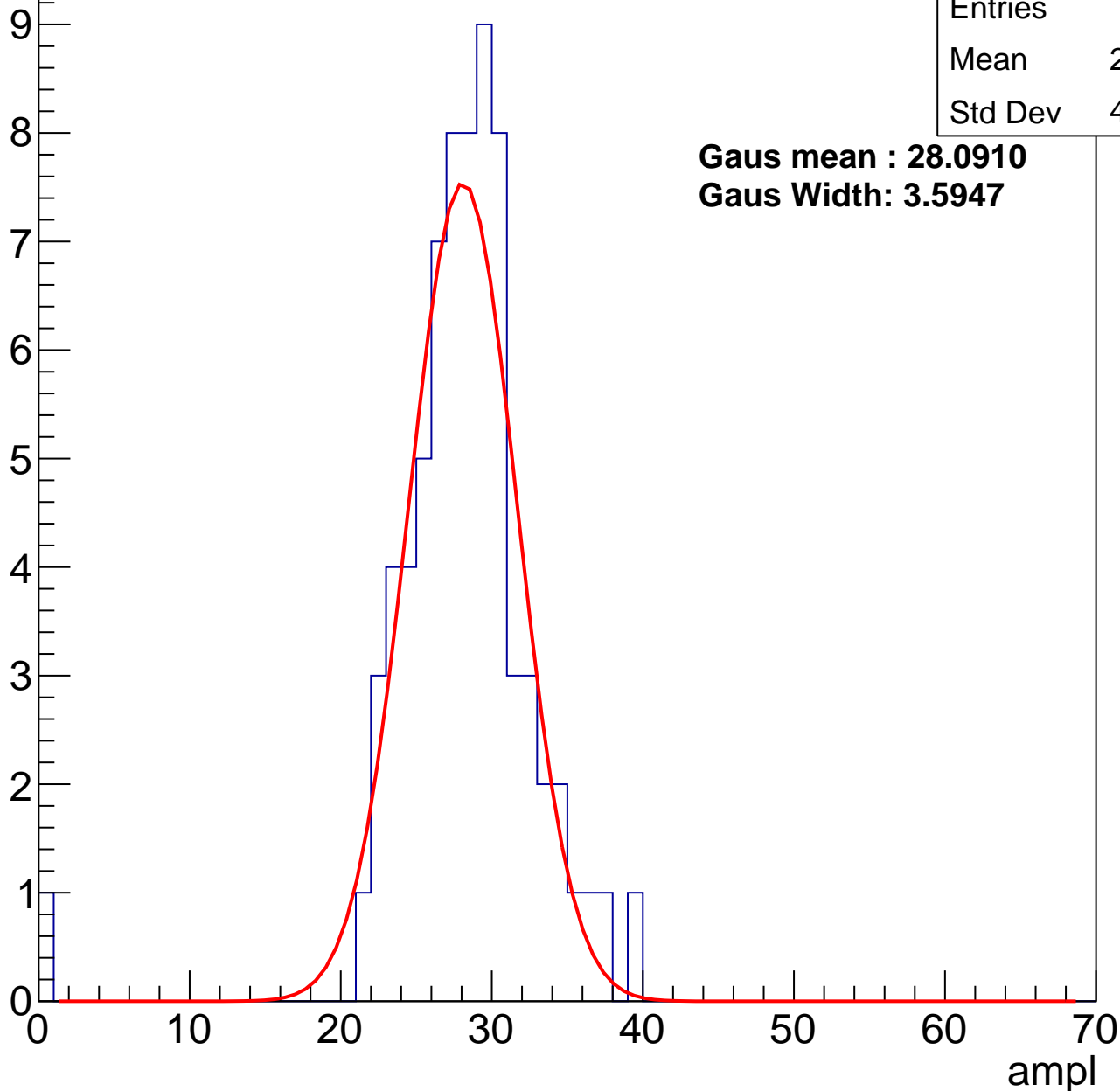
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	27.68
Std Dev	4.904

**Gaus mean : 28.0910**

**Gaus Width: 3.5947**



# B1L103S, U3-ch84, adc1

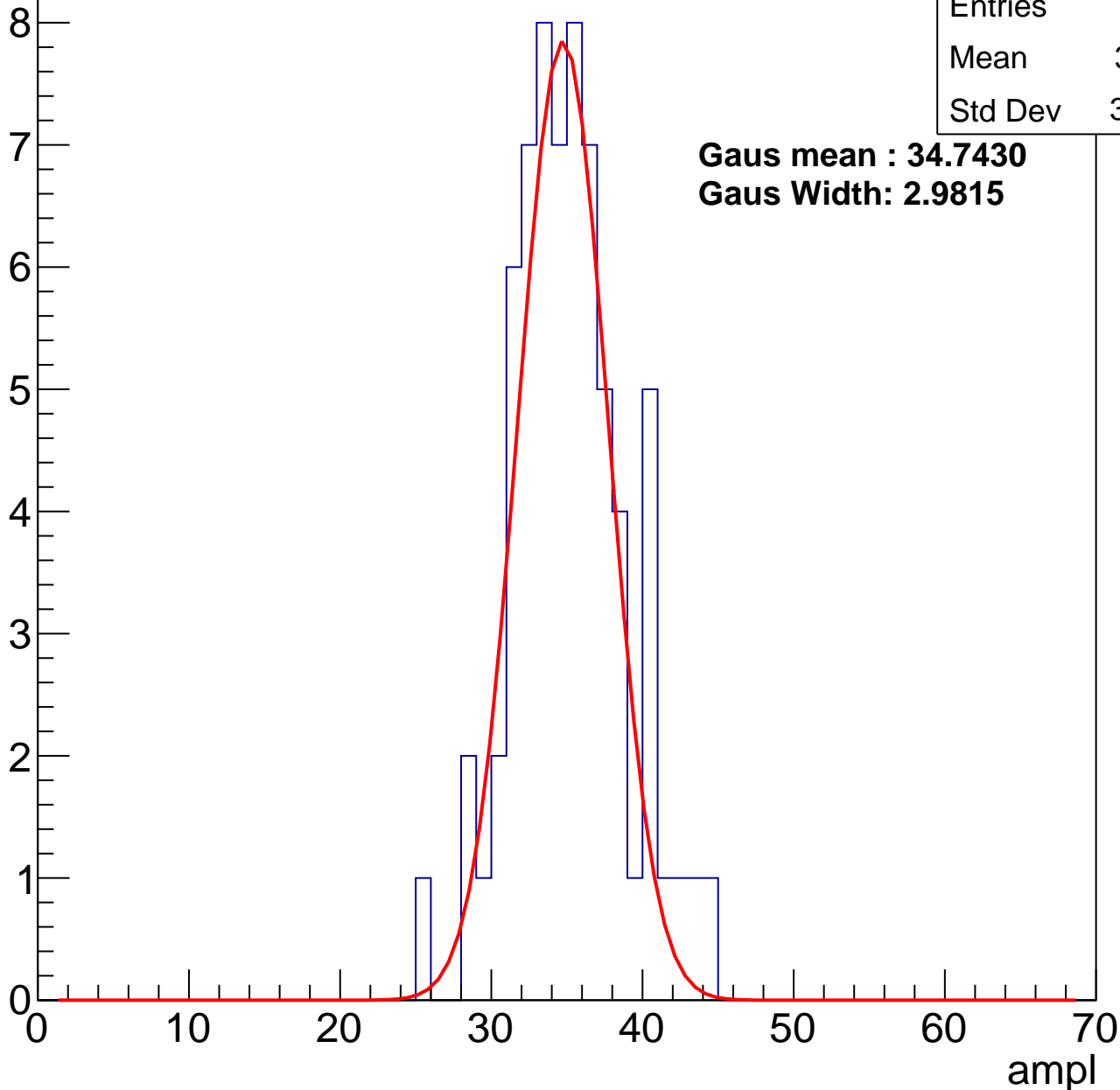
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	34.71
Std Dev	3.658

**Gaus mean : 34.7430**

**Gaus Width: 2.9815**



# B1L103S, U3-ch84, adc2

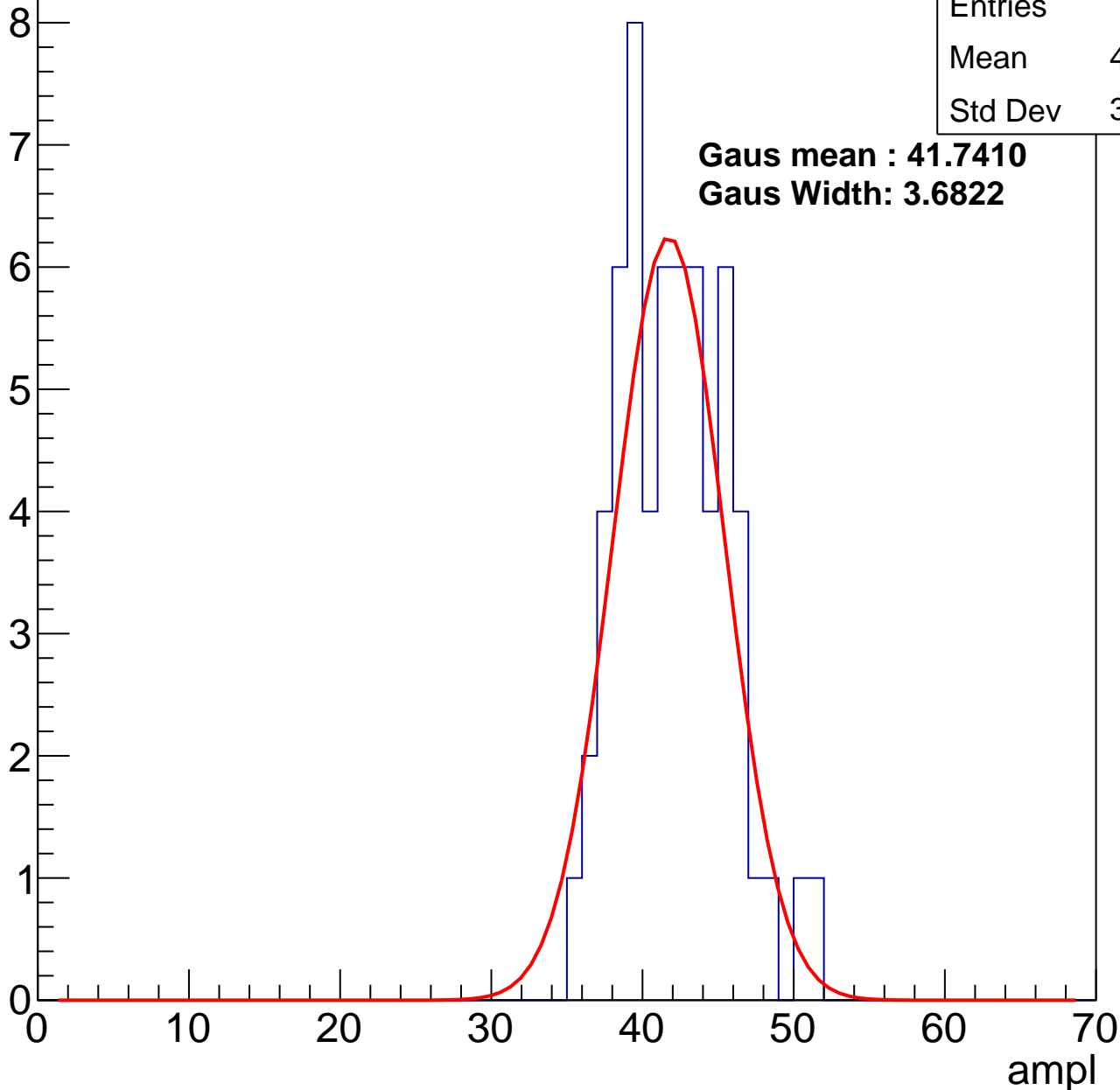
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	41.59
Std Dev	3.499

**Gaus mean : 41.7410**

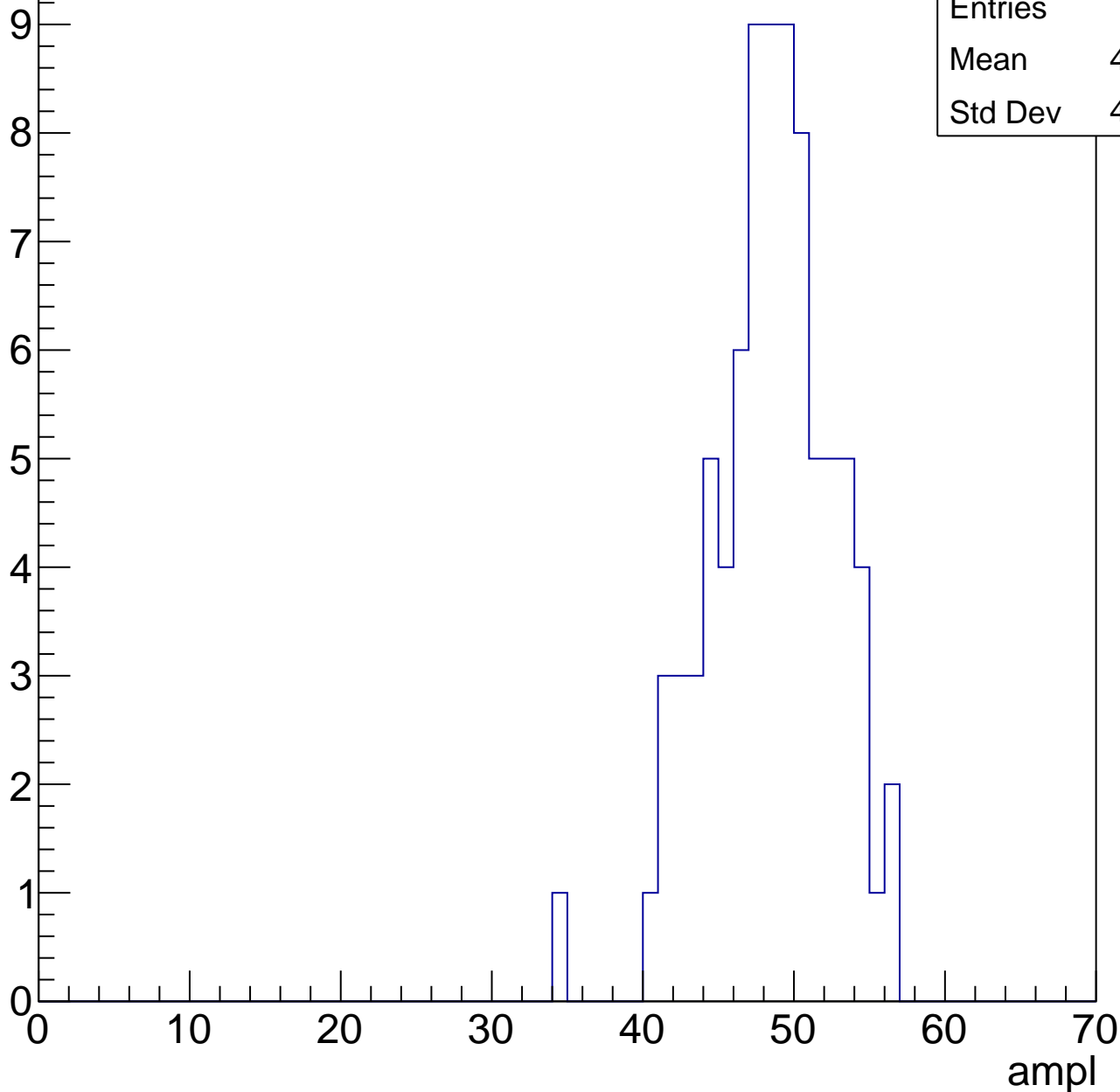
**Gaus Width: 3.6822**



# B1L103S, U3-ch84, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



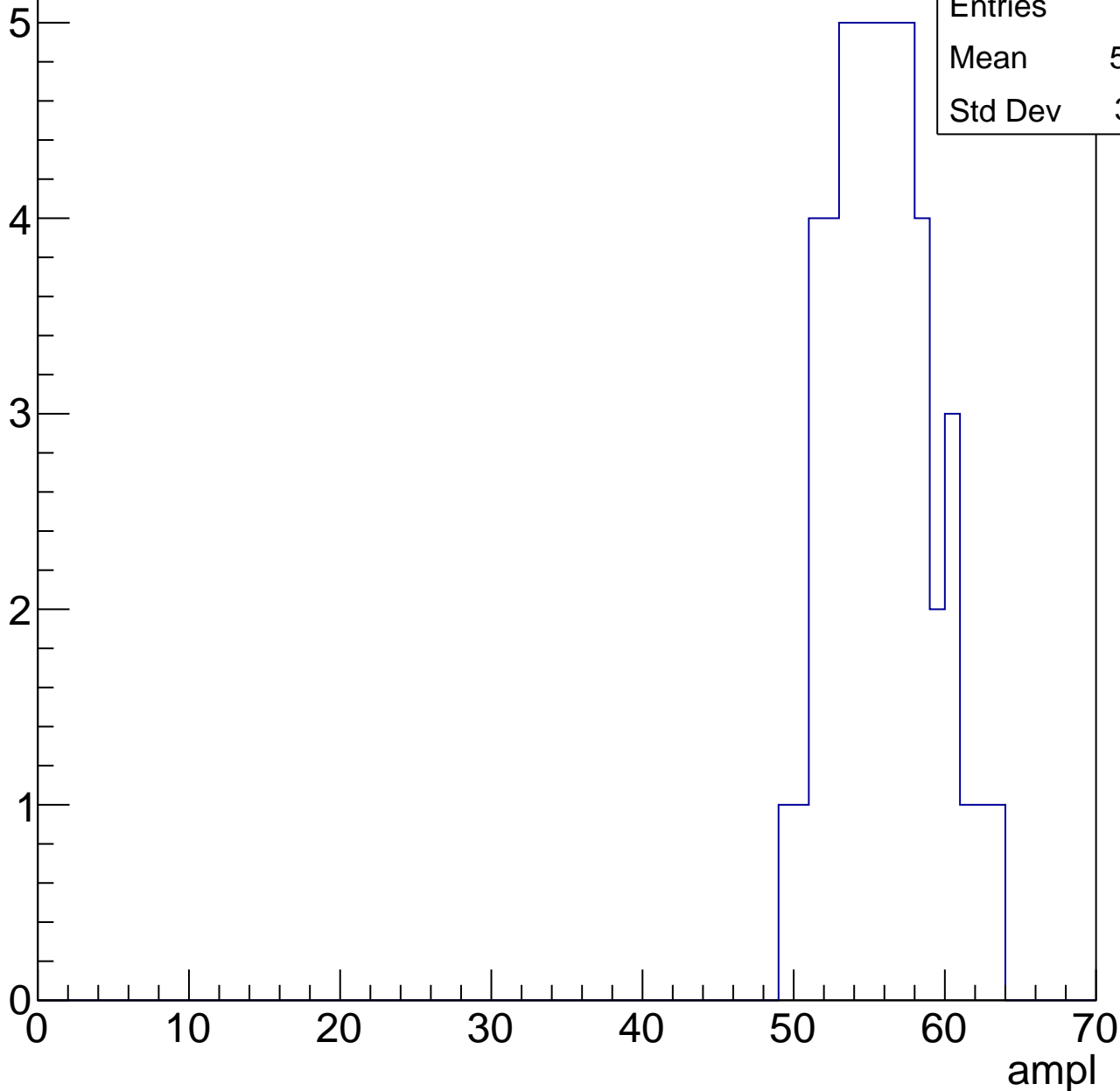
Entries	83
Mean	48.04
Std Dev	4.034

# B1L103S, U3-ch84, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	47
Mean	55.36
Std Dev	3.251

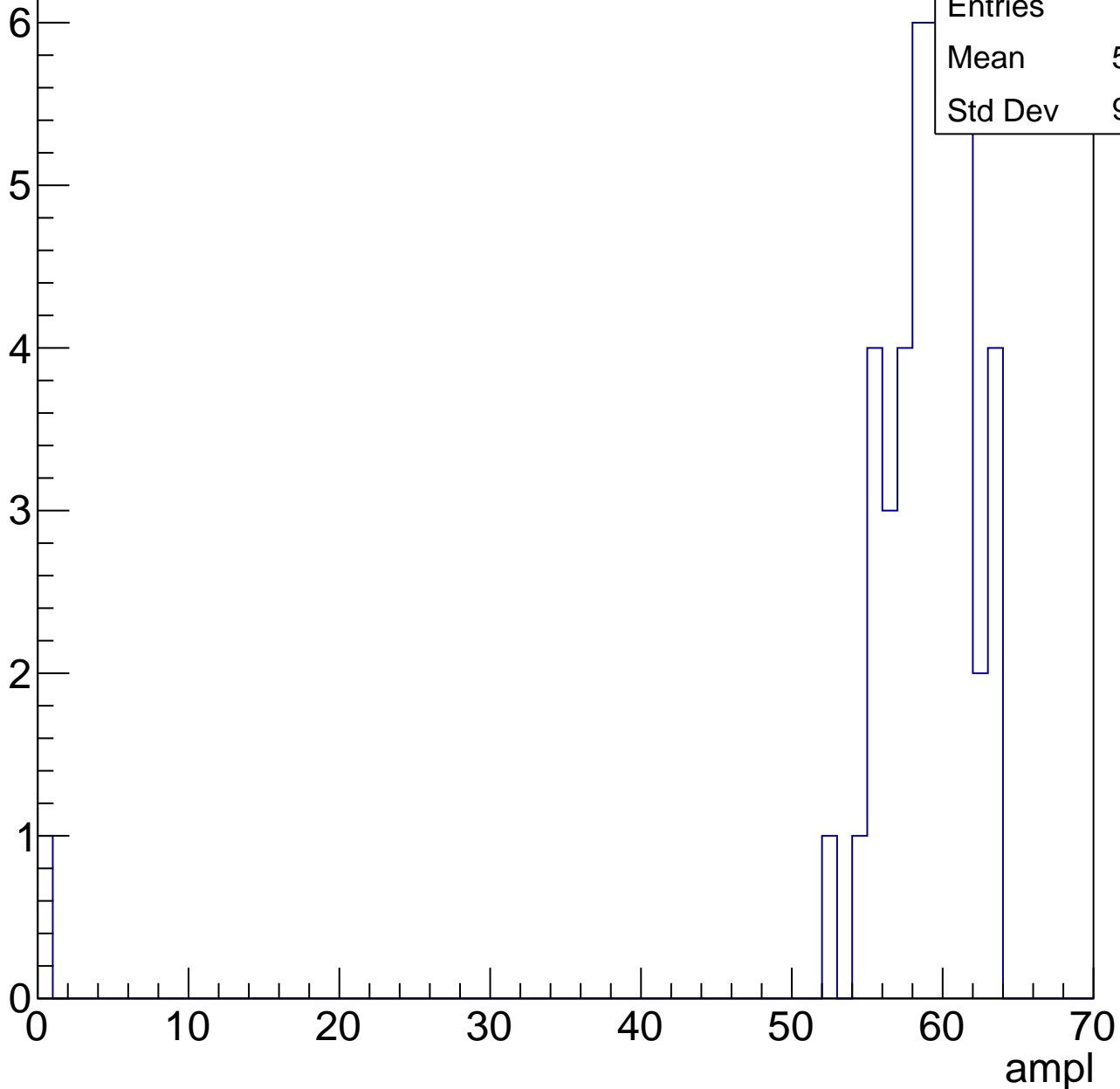


# B1L103S, U3-ch84, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	44
Mean	57.41
Std Dev	9.131

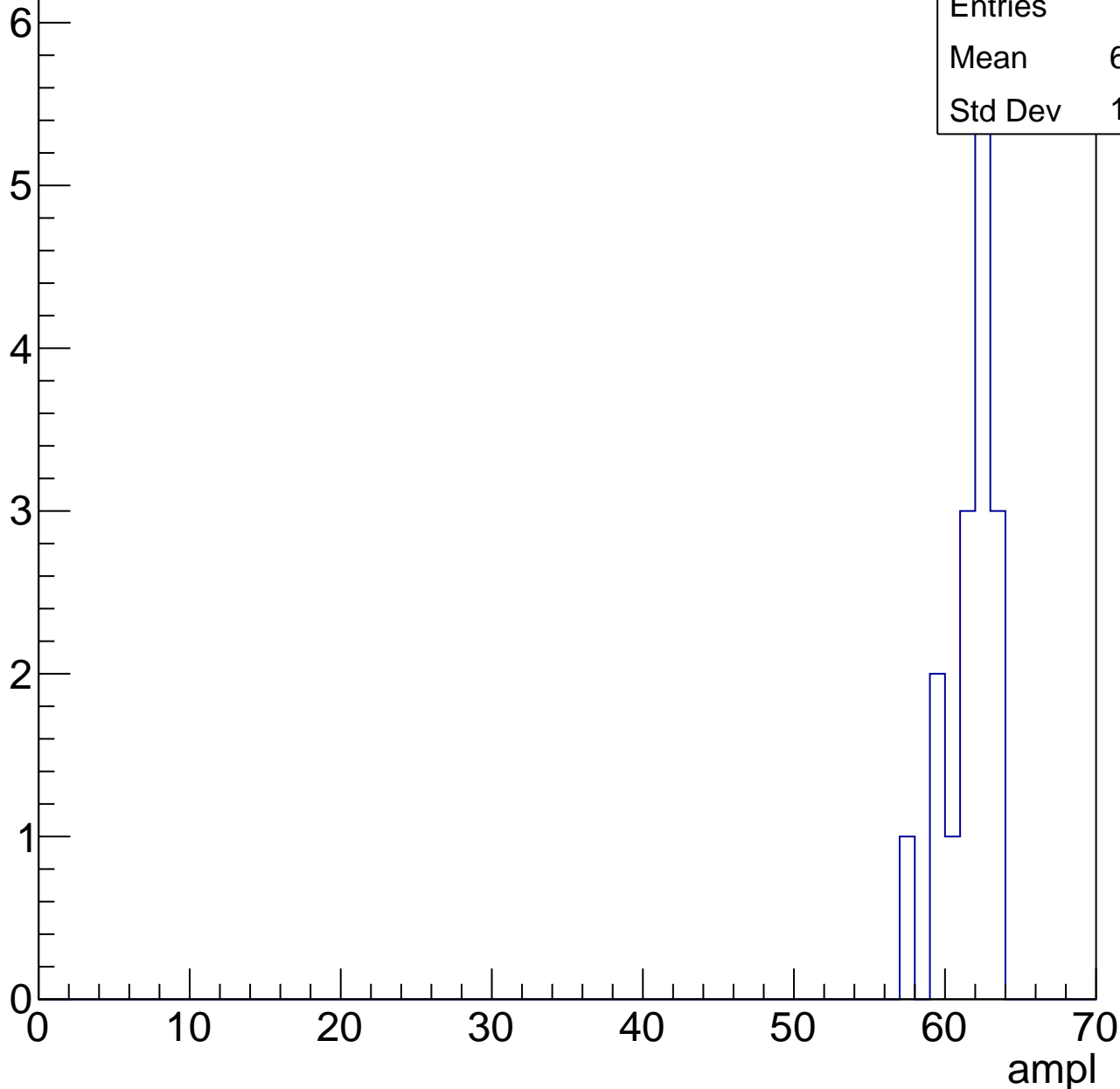


# B1L103S, U3-ch84, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	16
Mean	61.19
Std Dev	1.629

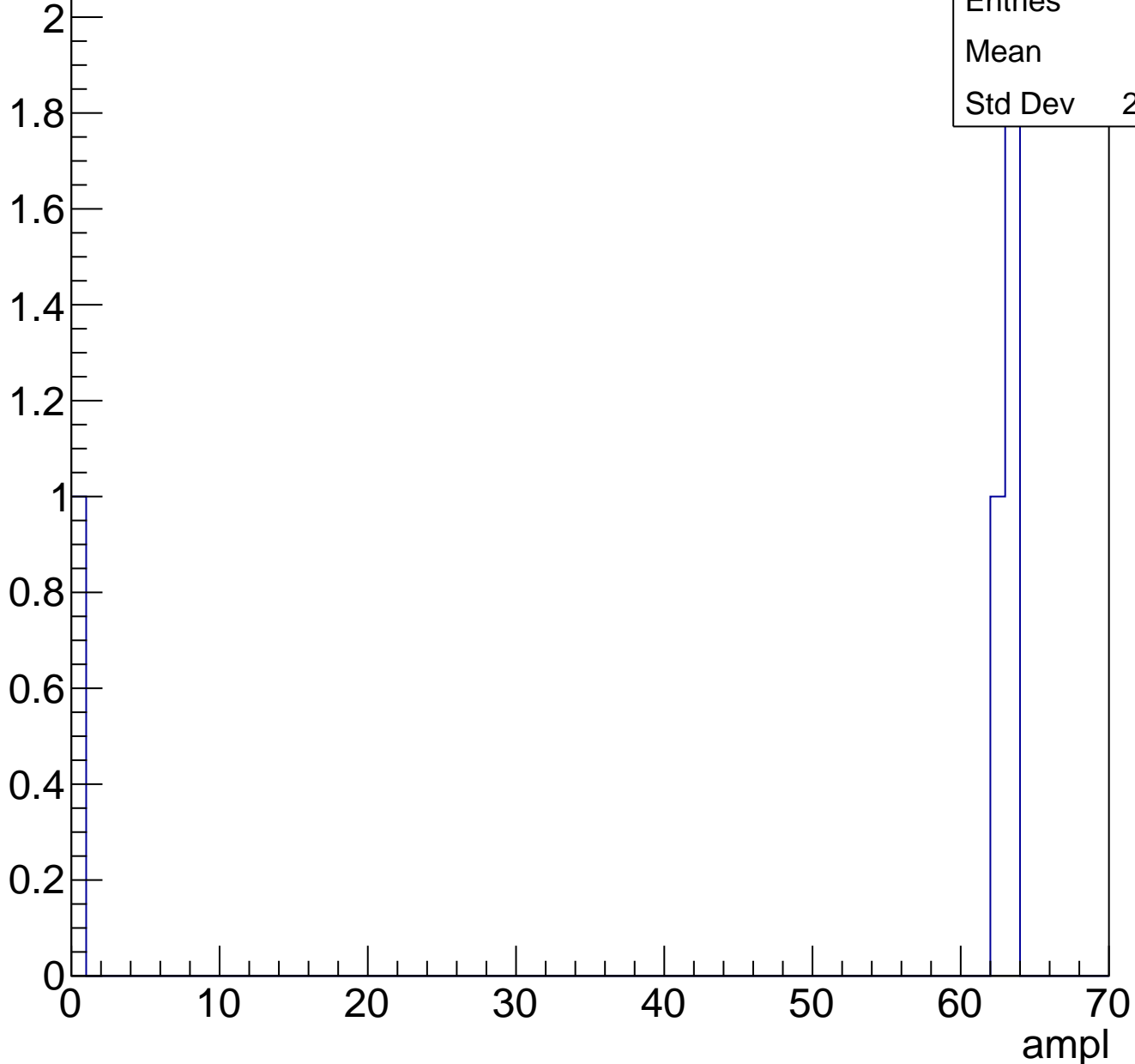




# B1L103S, U3-ch84, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch85, adc0

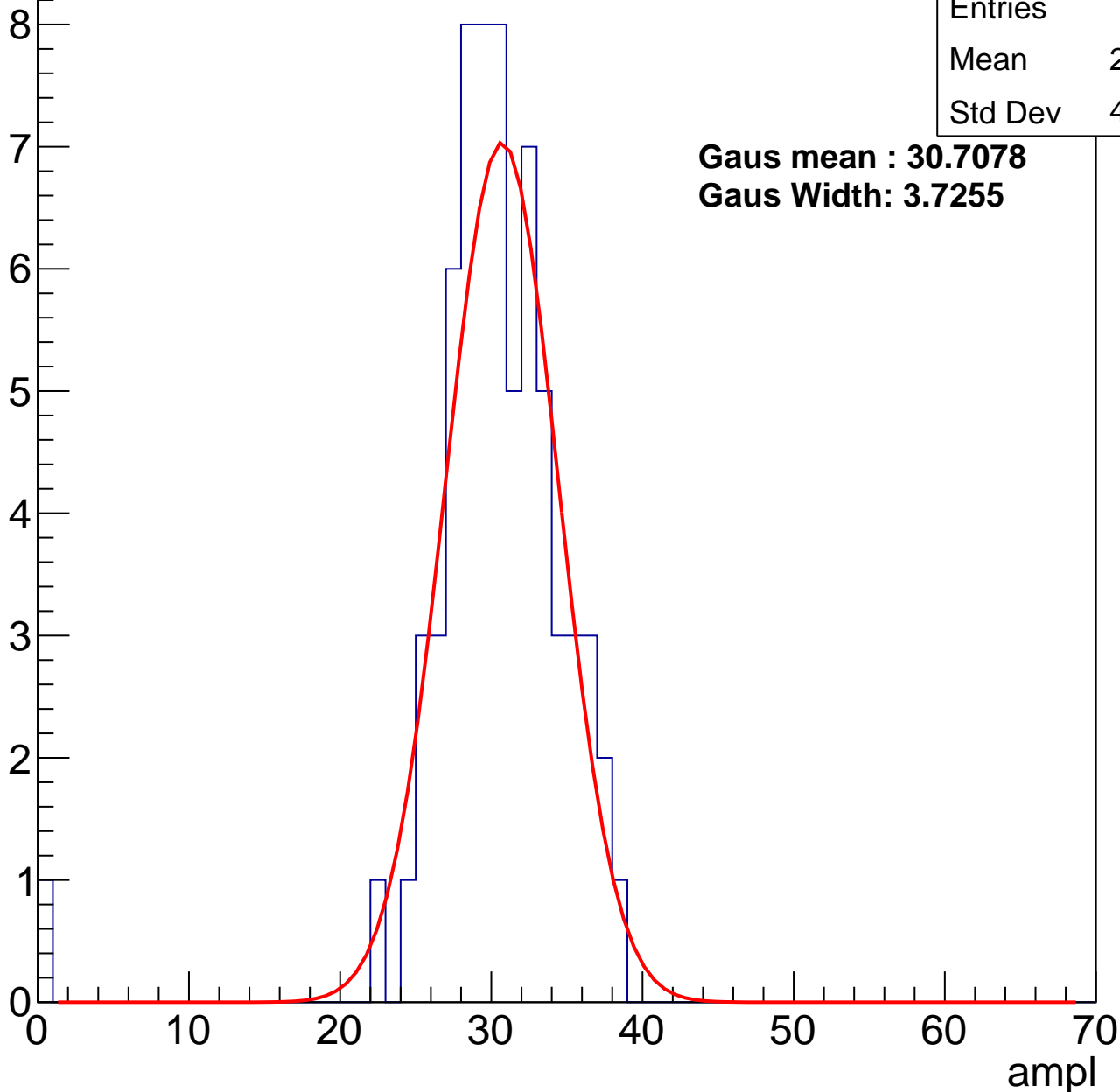
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	29.82
Std Dev	4.979

**Gaus mean : 30.7078**

**Gaus Width: 3.7255**



# B1L103S, U3-ch85, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

7

6

5

4

3

2

1

0

Entries 66

Mean 36.89

Std Dev 3.61

**Gaus mean : 36.9063**

**Gaus Width: 3.4370**

ampl

0

10

20

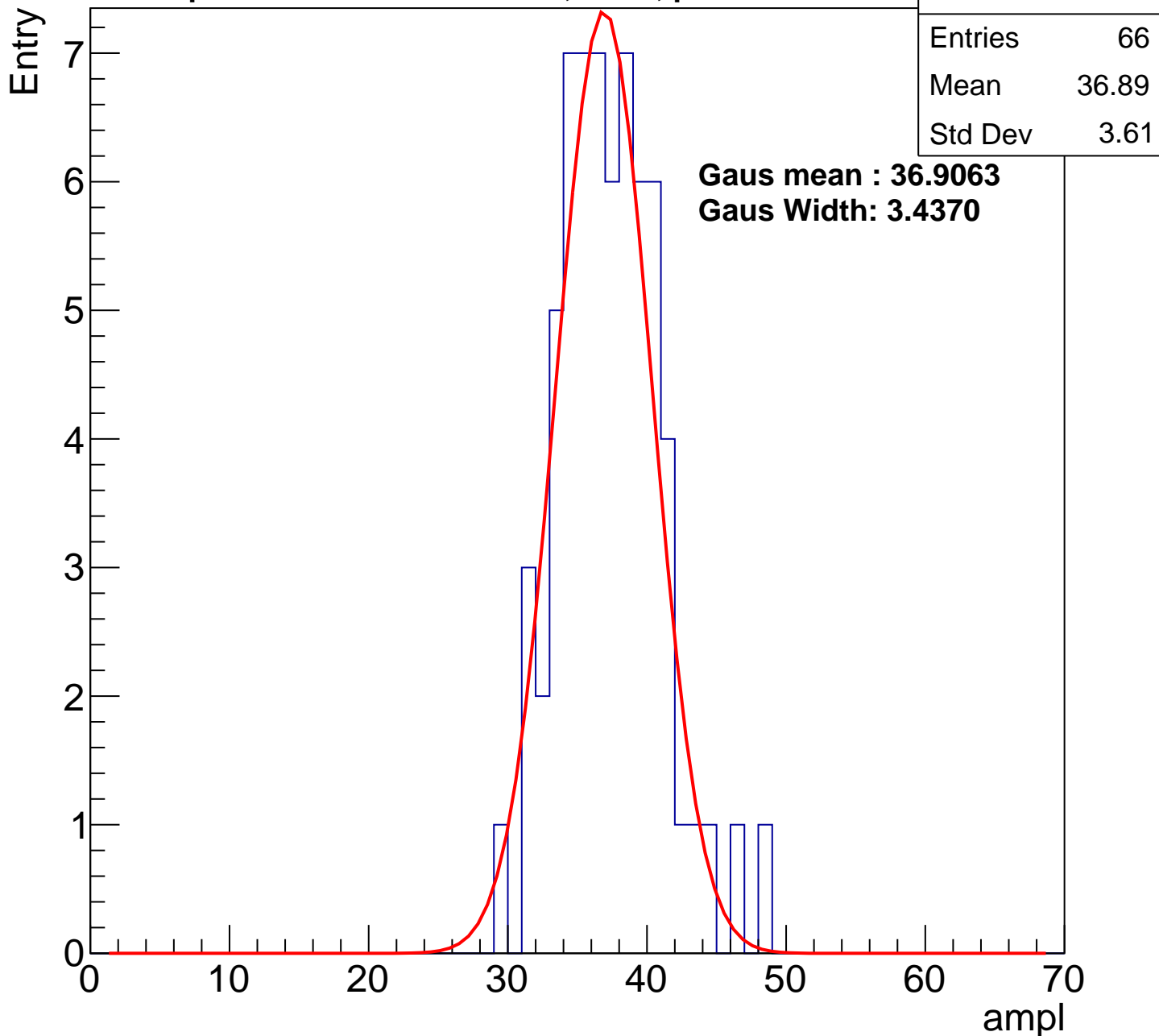
30

40

50

60

70



# B1L103S, U3-ch85, adc2

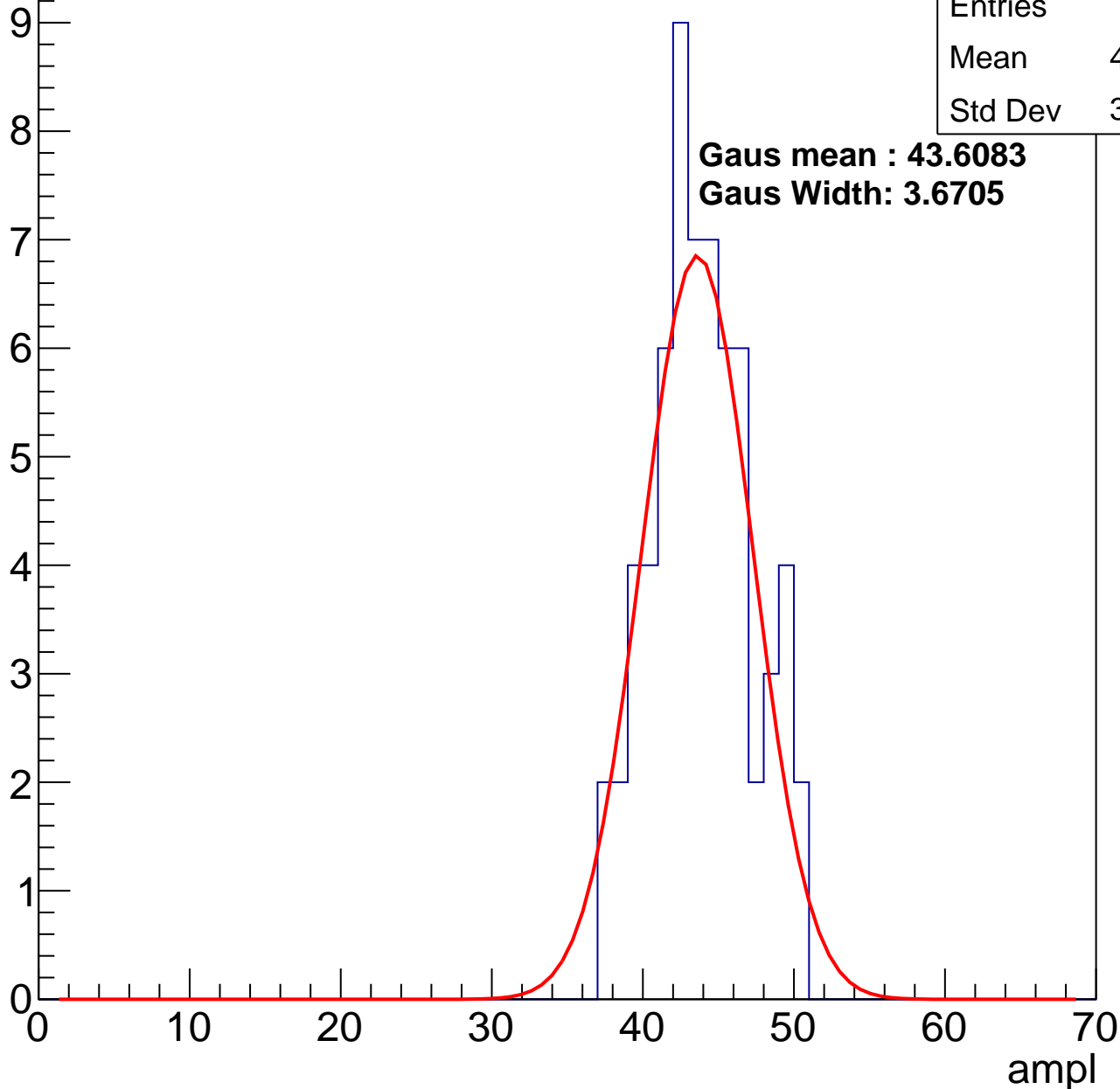
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	43.42
Std Dev	3.254

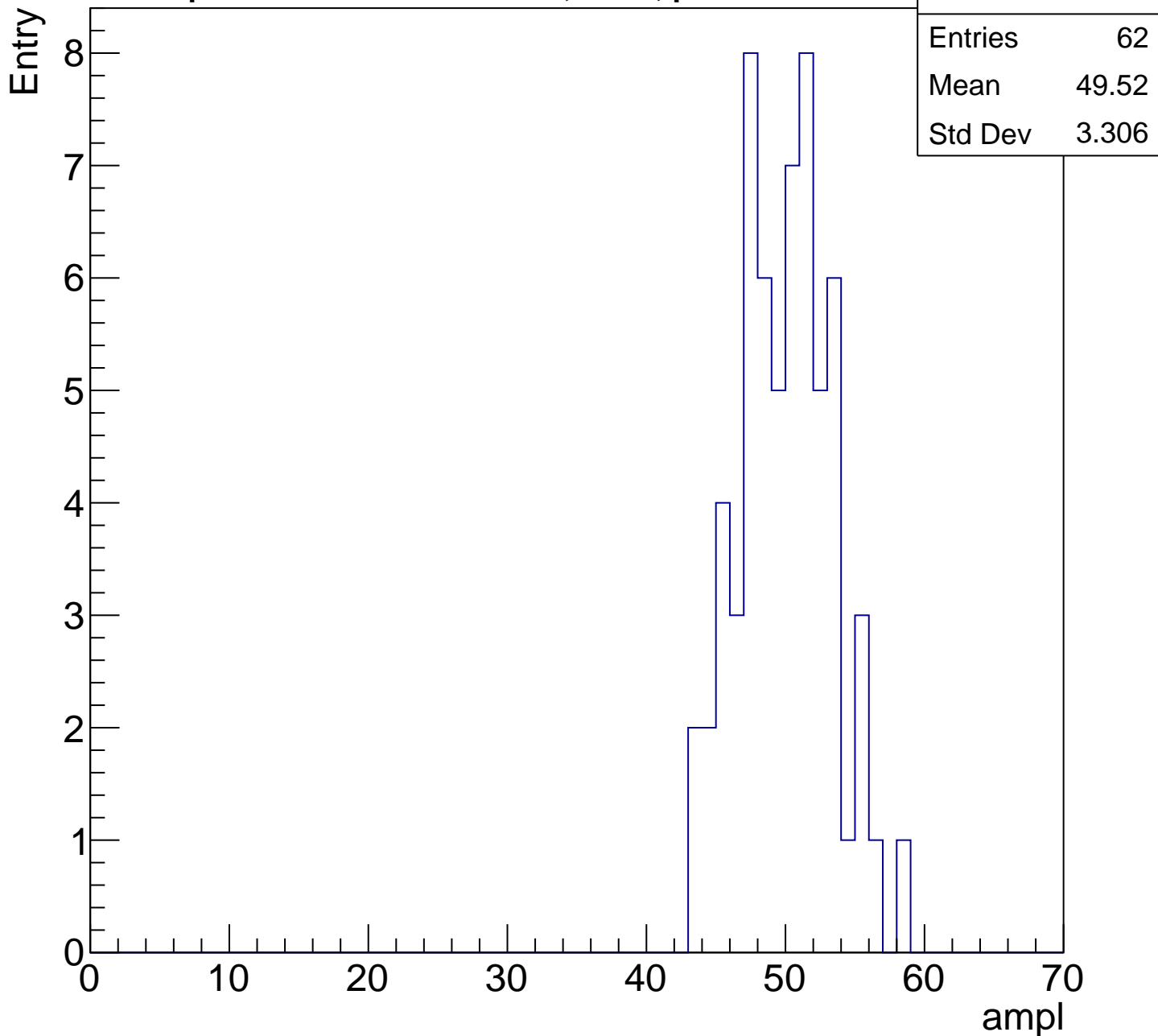
**Gaus mean : 43.6083**

**Gaus Width: 3.6705**



# B1L103S, U3-ch85, adc3

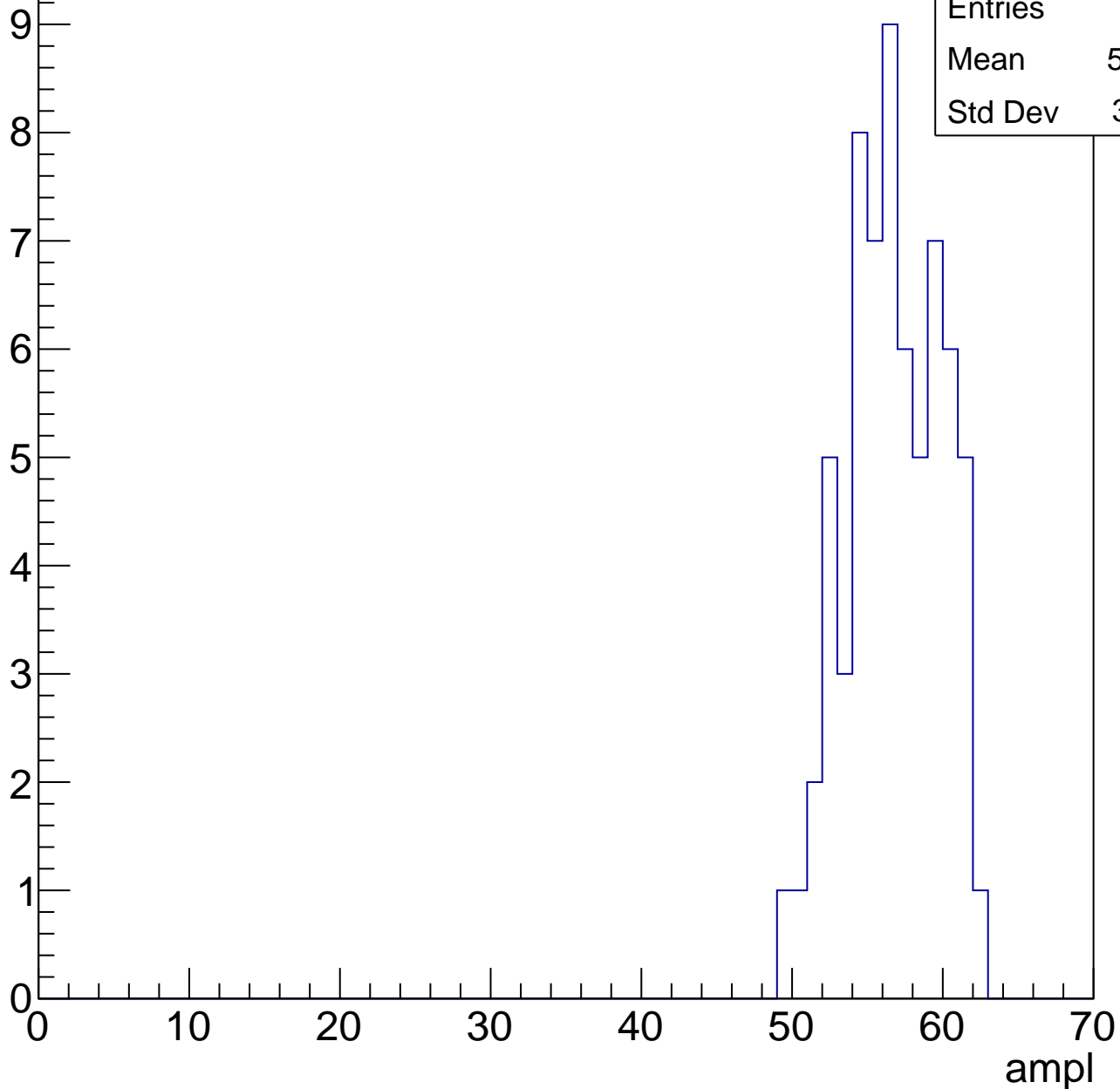
calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U3-ch85, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



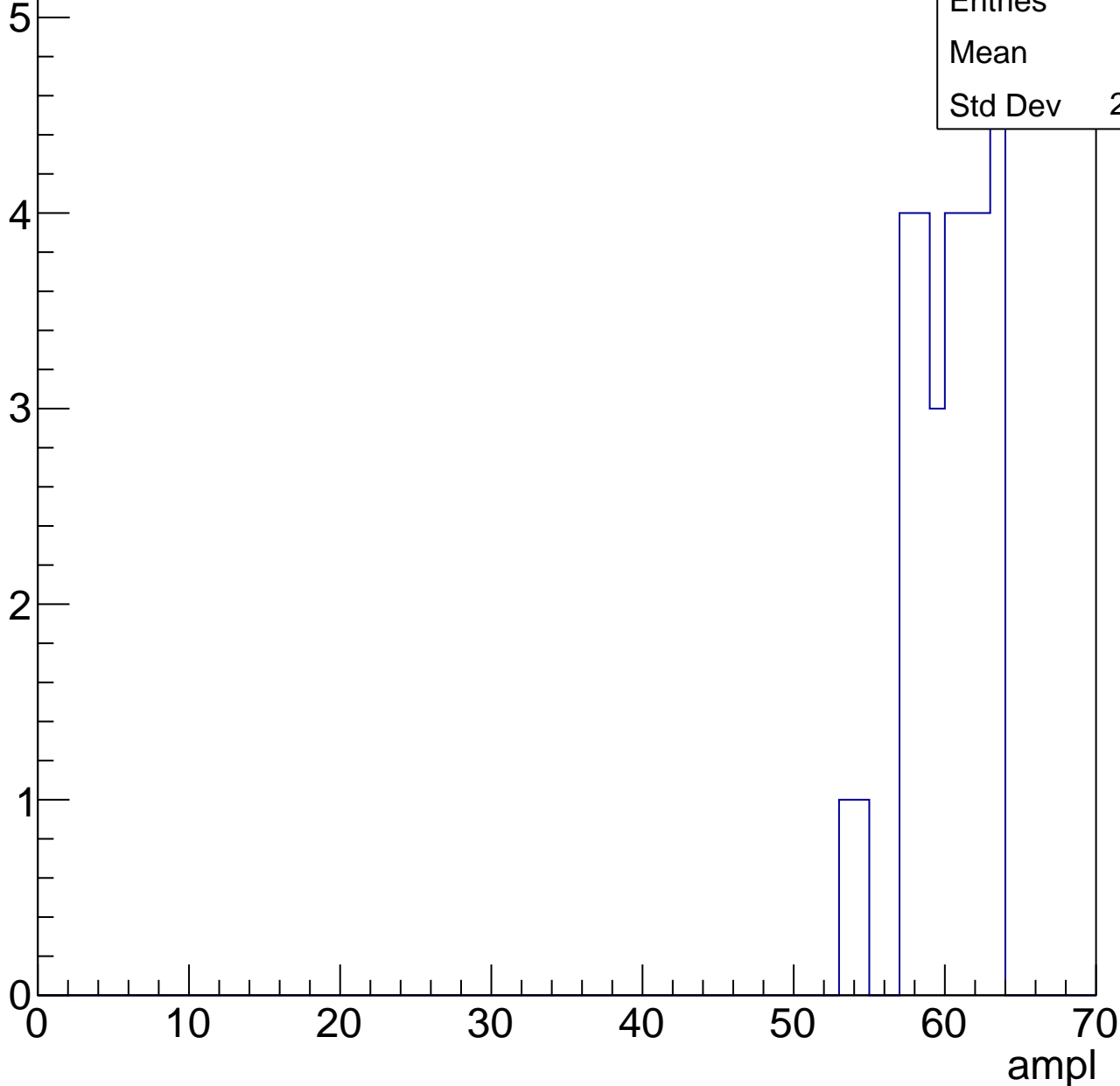
Entries	66
Mean	56.26
Std Dev	3.071

# B1L103S, U3-ch85, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	30
Mean	59.7
Std Dev	2.597

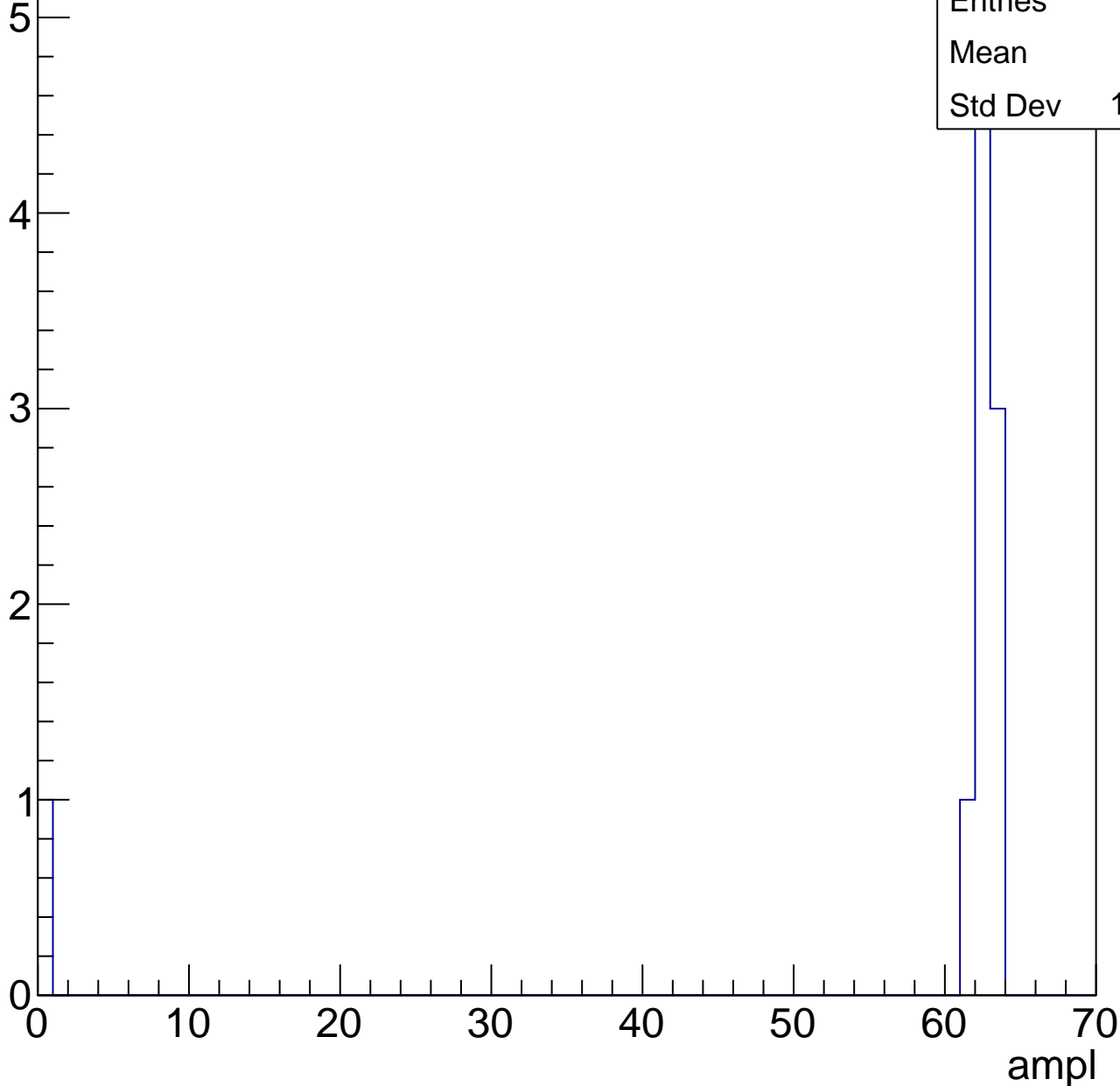


# B1L103S, U3-ch85, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	10
Mean	56
Std Dev	18.68

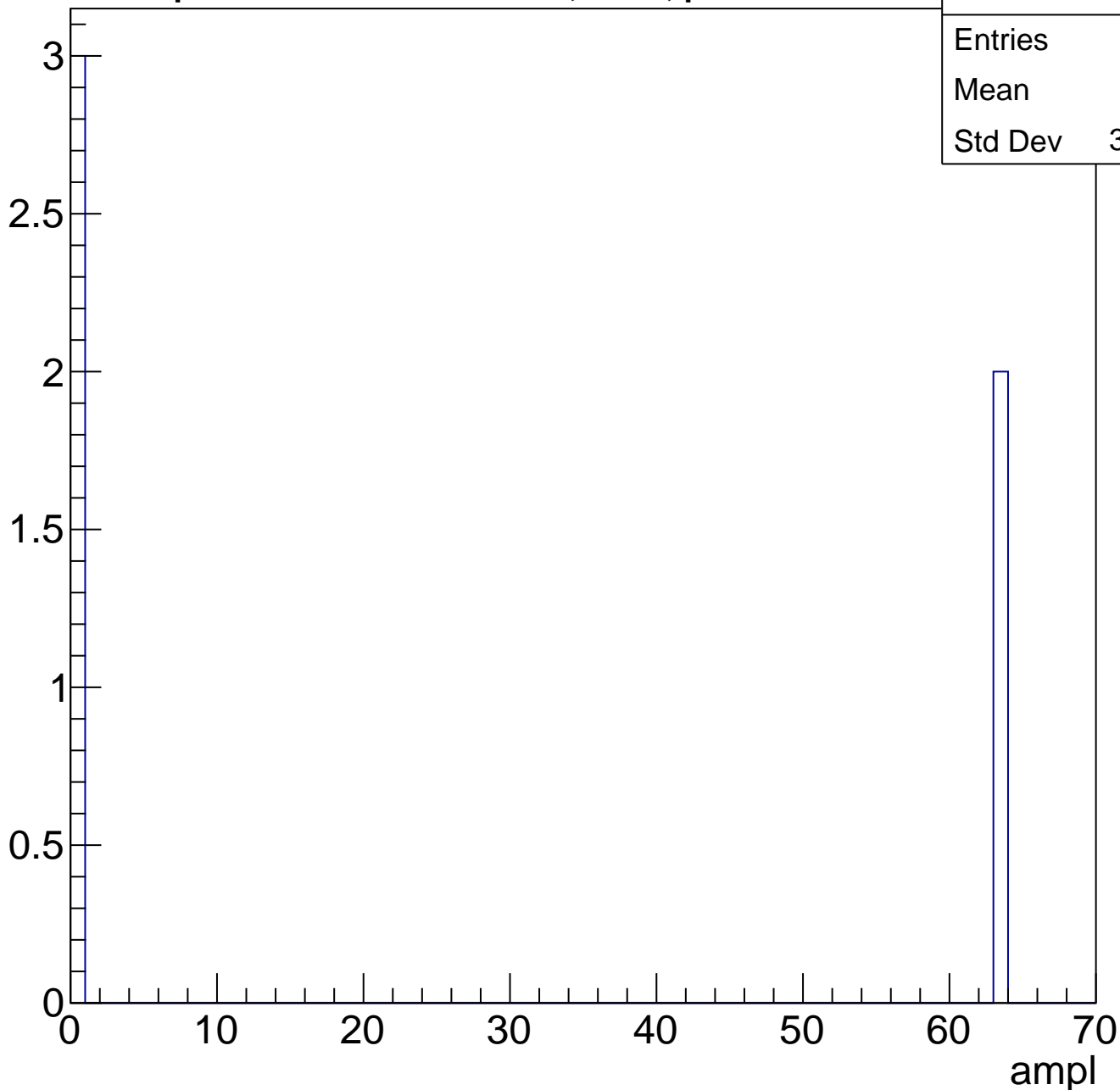




# B1L103S, U3-ch85, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	5
Mean	25.2
Std Dev	30.86

# B1L103S, U3-ch86, adc0

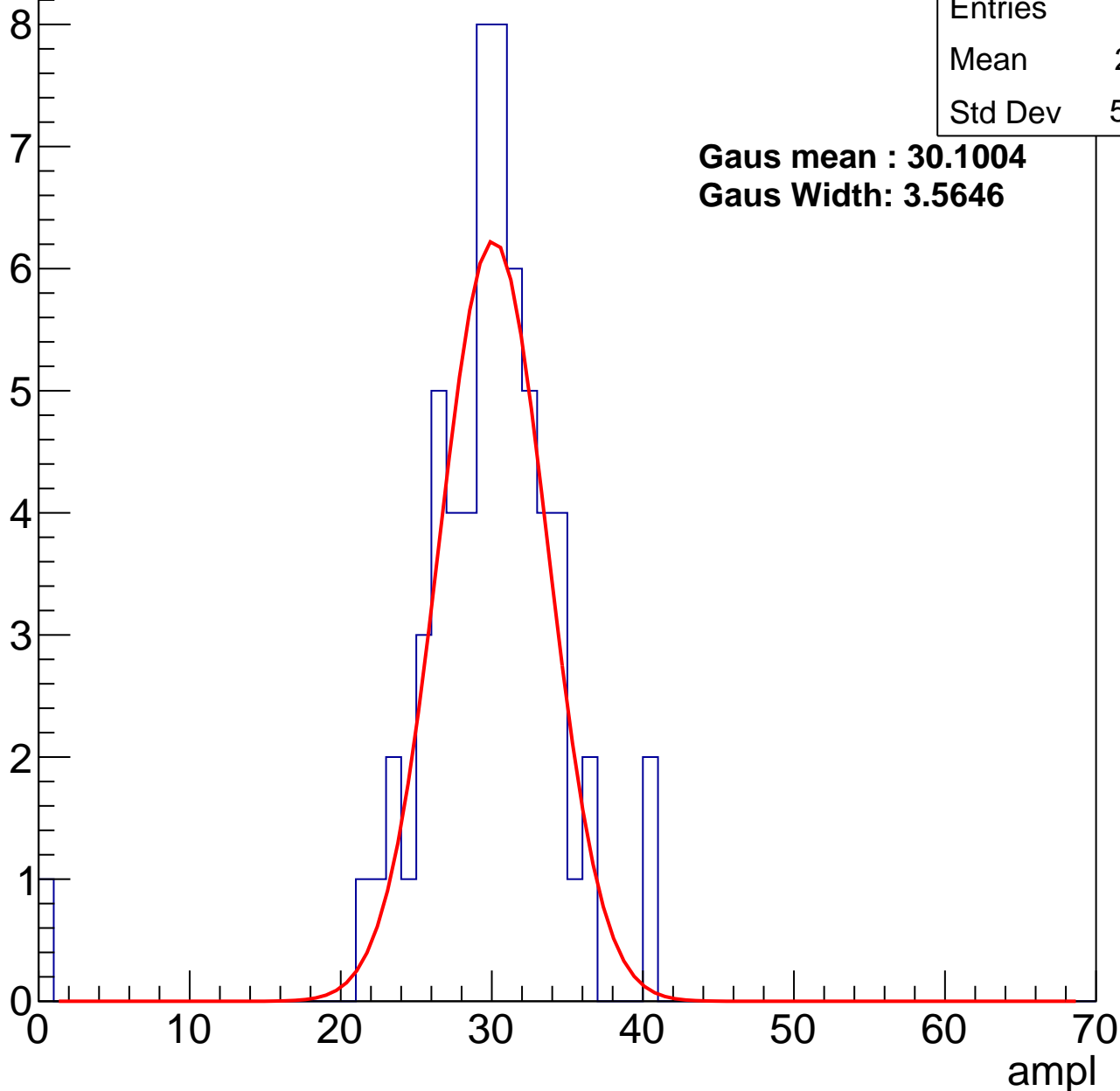
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	29.21
Std Dev	5.356

**Gaus mean : 30.1004**

**Gaus Width: 3.5646**



# B1L103S, U3-ch86, adc1

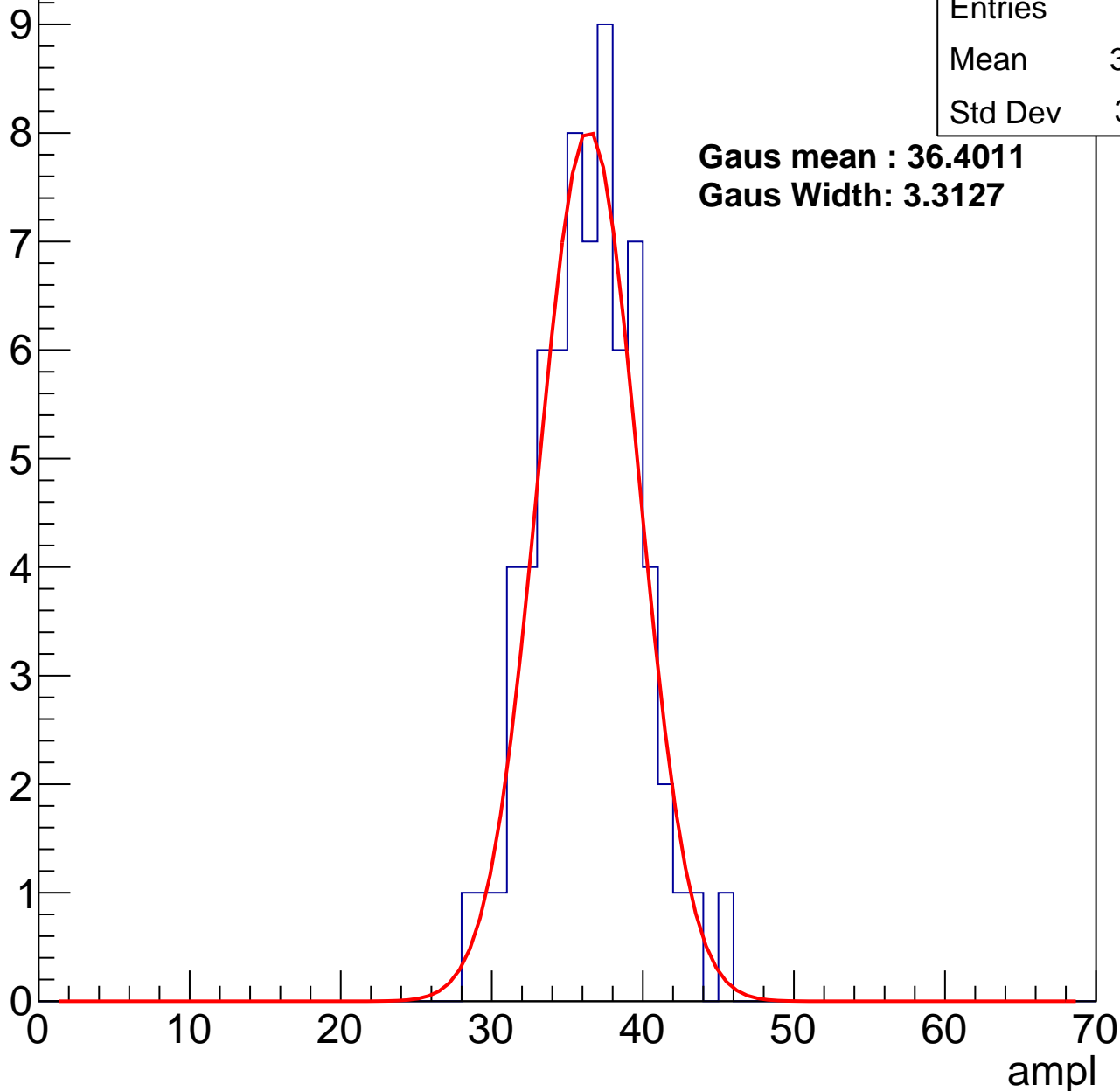
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	35.93
Std Dev	3.351

**Gaus mean : 36.4011**

**Gaus Width: 3.3127**



# B1L103S, U3-ch86, adc2

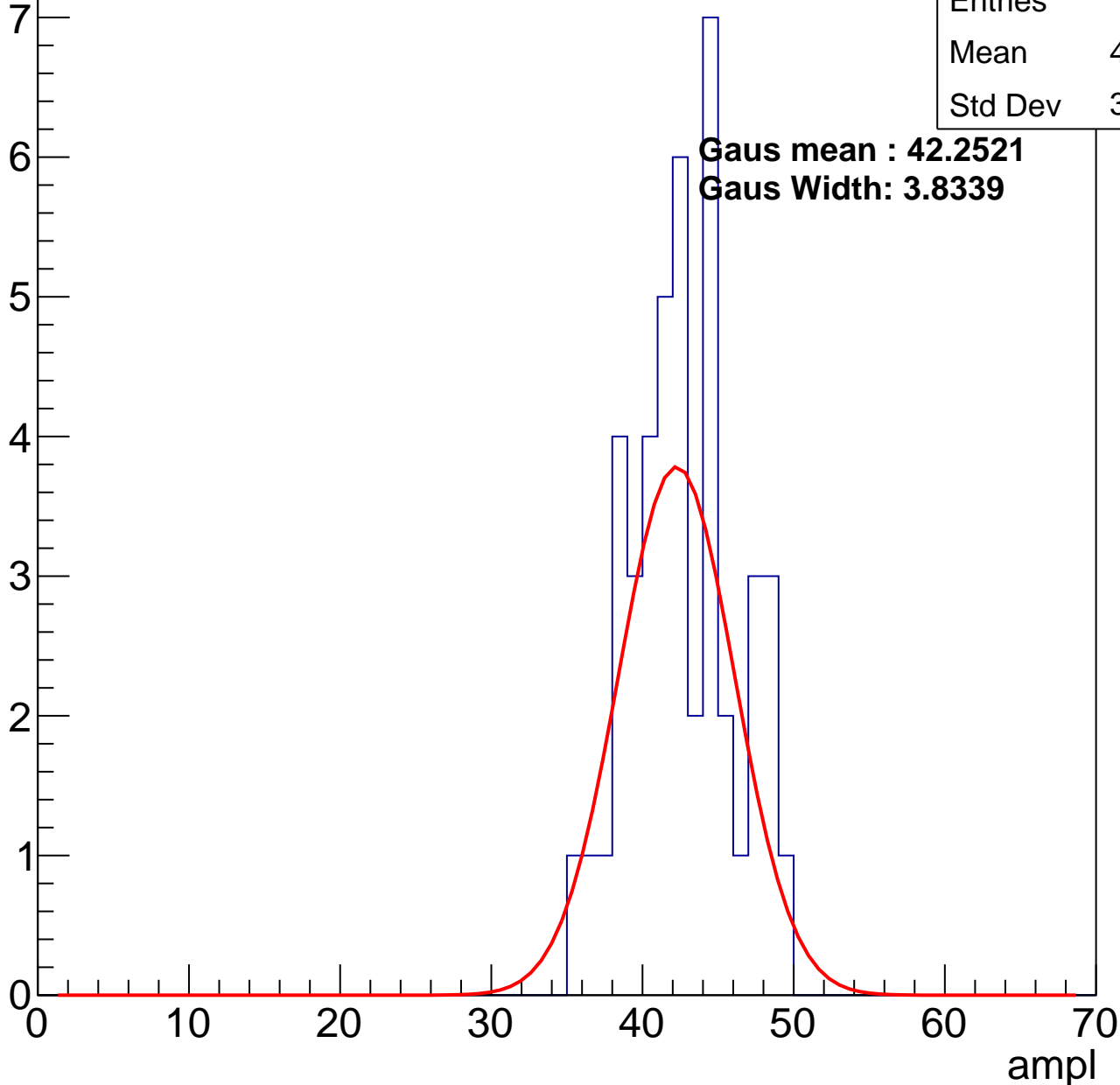
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	44
Mean	42.23
Std Dev	3.424

**Gaus mean : 42.2521**

**Gaus Width: 3.8339**

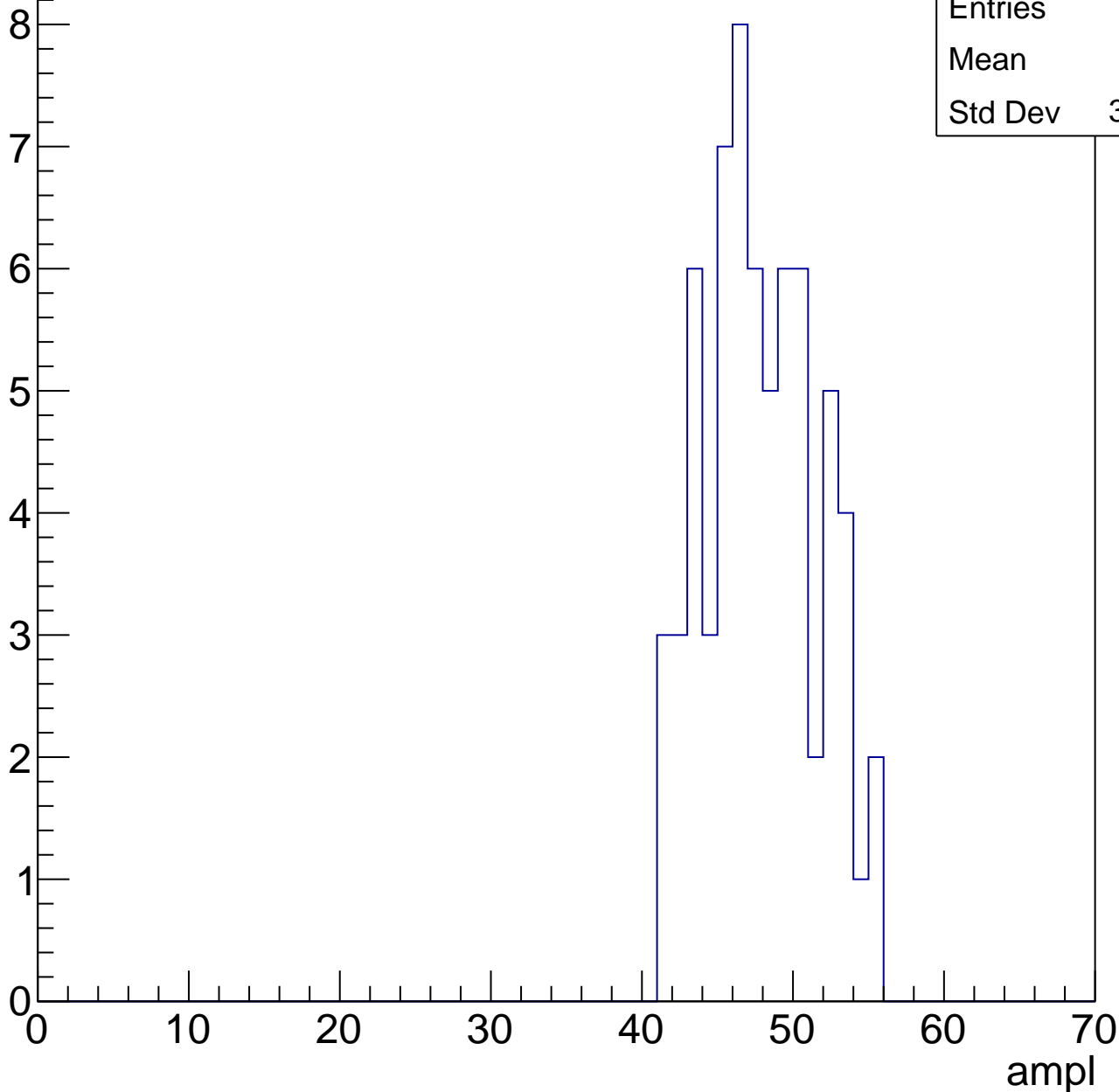


# B1L103S, U3-ch86, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

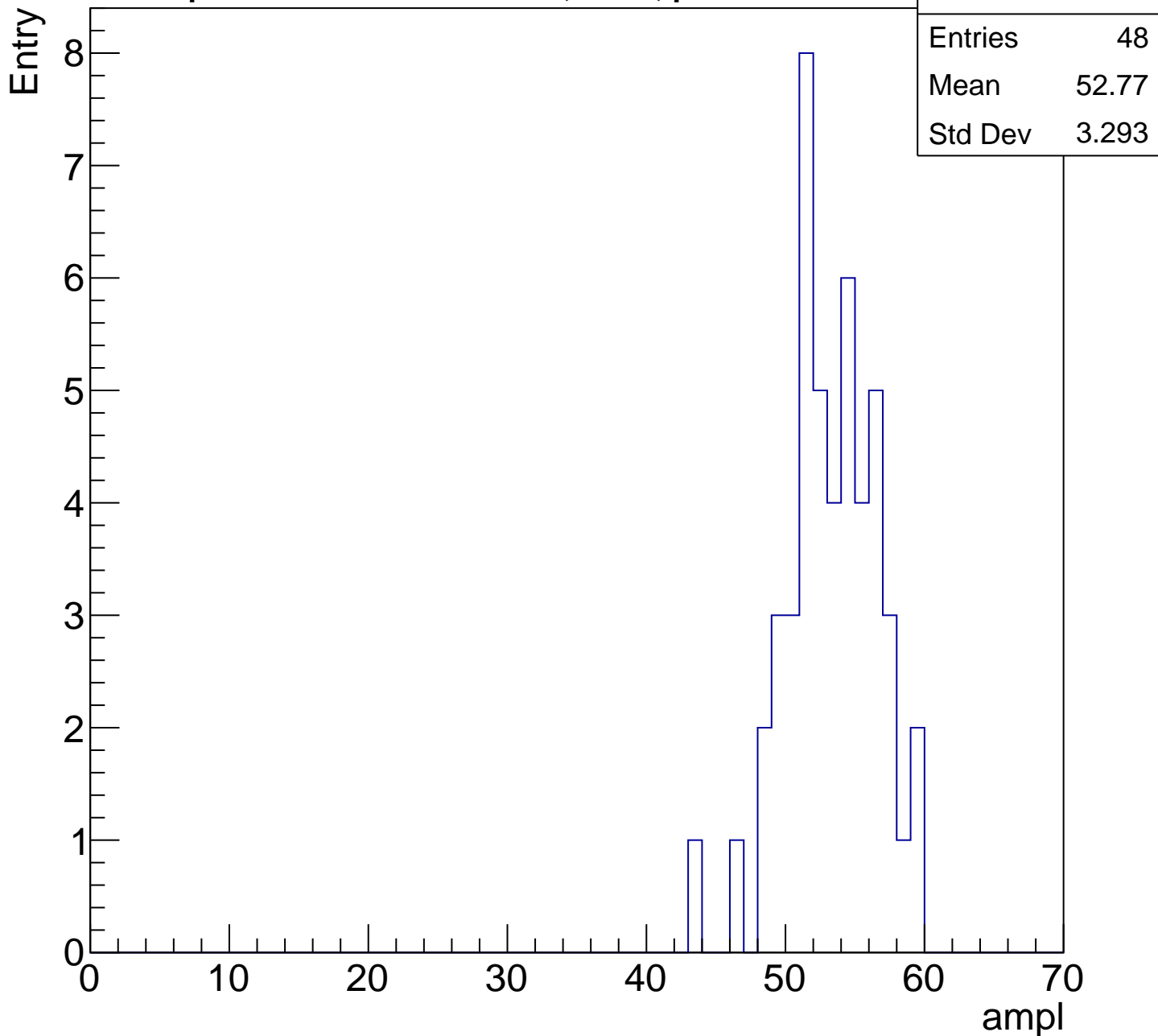
Entry

Entries	67
Mean	47.4
Std Dev	3.649



# B1L103S, U3-ch86, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

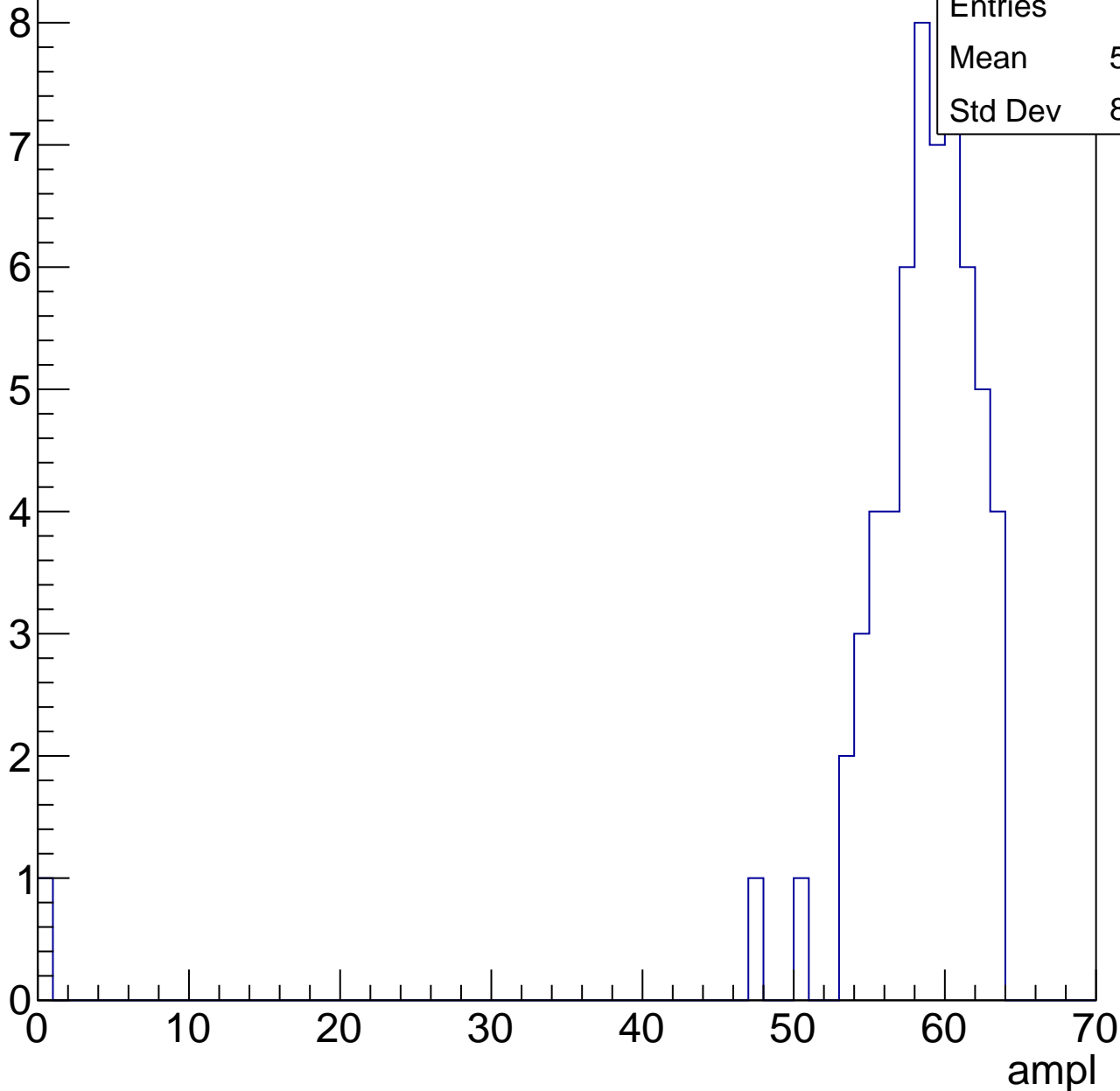


# B1L103S, U3-ch86, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	57.27
Std Dev	8.109

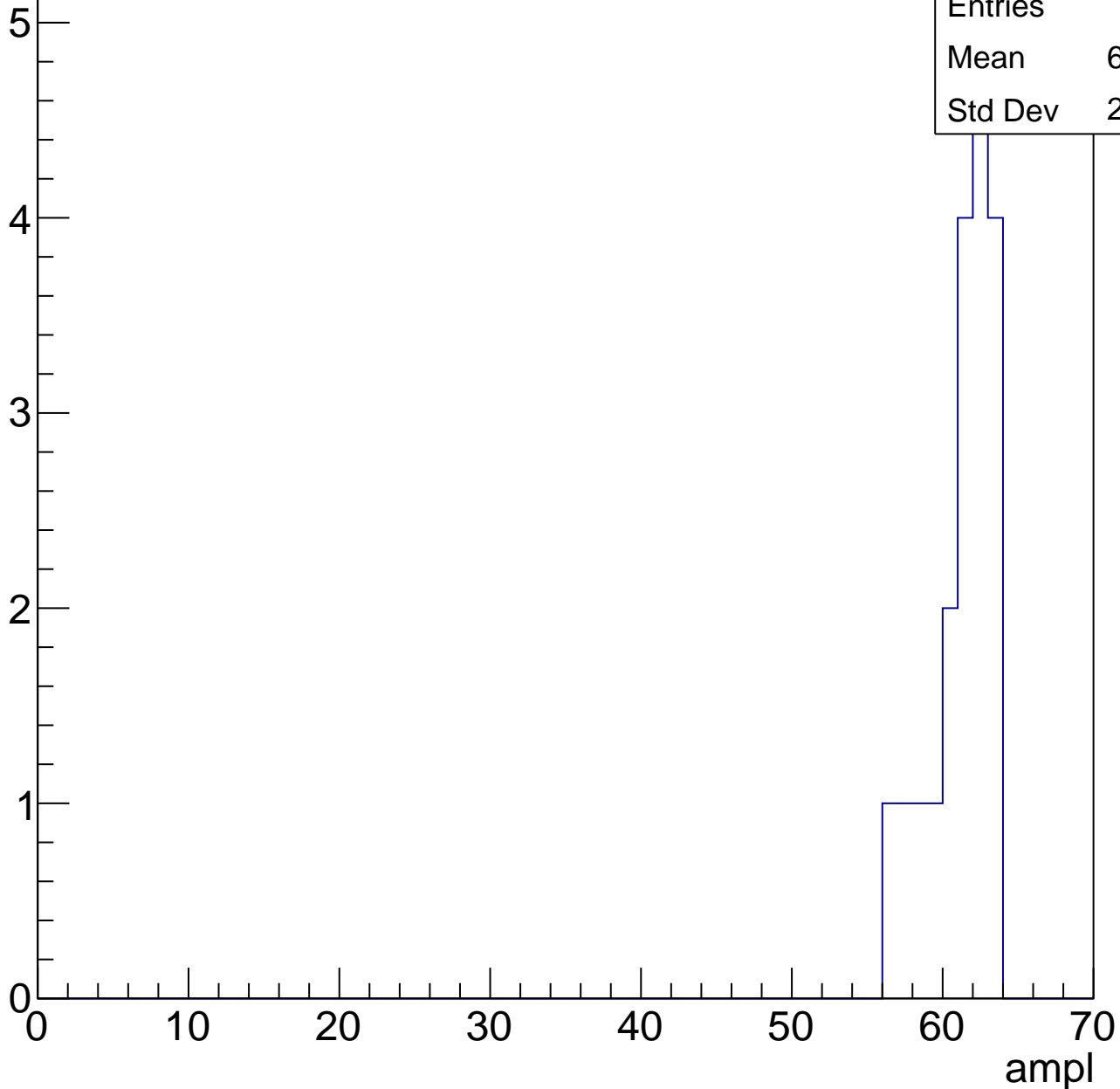


# B1L103S, U3-ch86, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	19
Mean	60.84
Std Dev	2.007

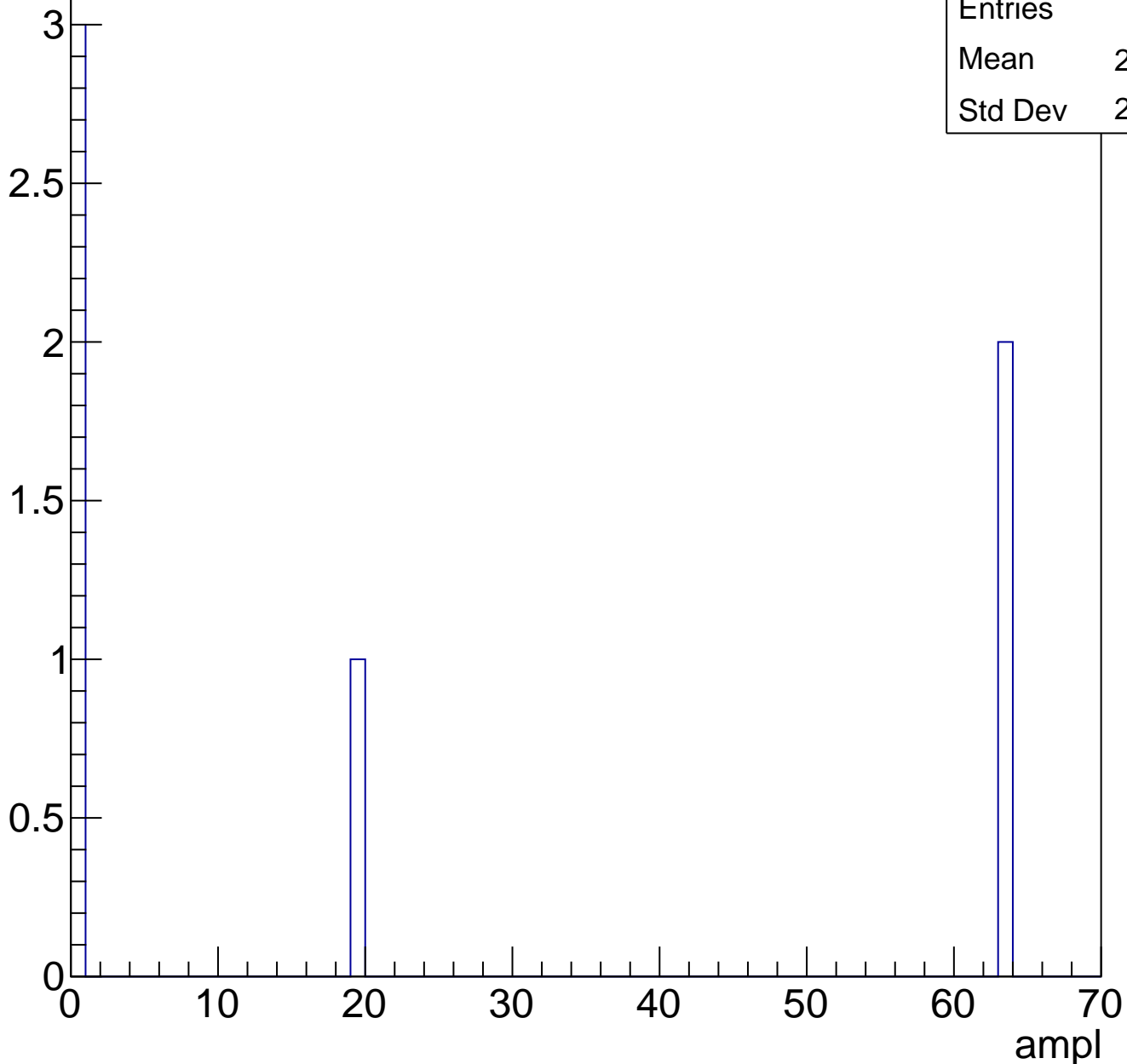




# B1L103S, U3-ch86, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	6
Mean	24.17
Std Dev	28.27

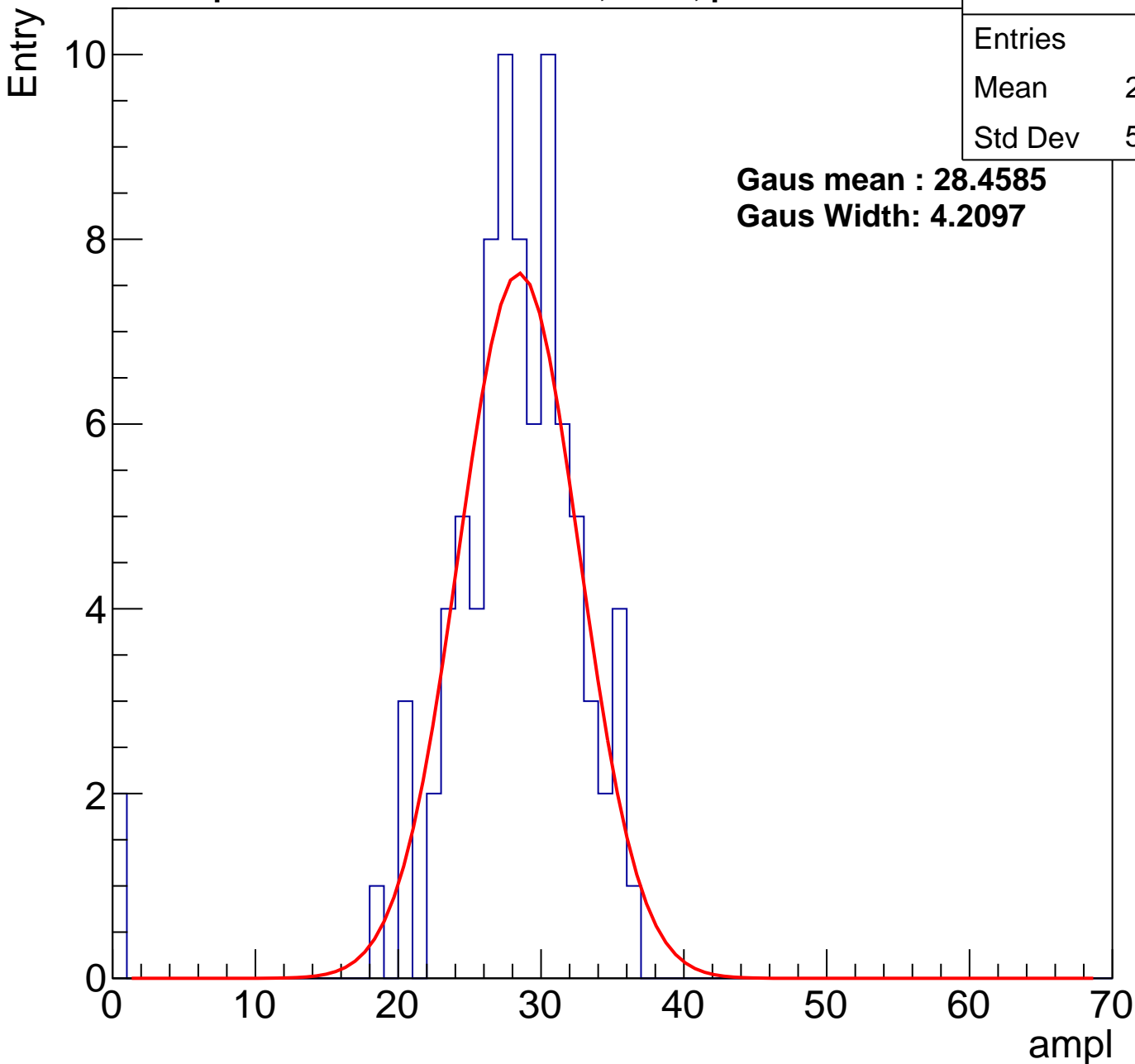
# B1L103S, U3-ch87, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	84
Mean	27.37
Std Dev	5.715

**Gaus mean : 28.4585**

**Gaus Width: 4.2097**



# B1L103S, U3-ch87, adc1

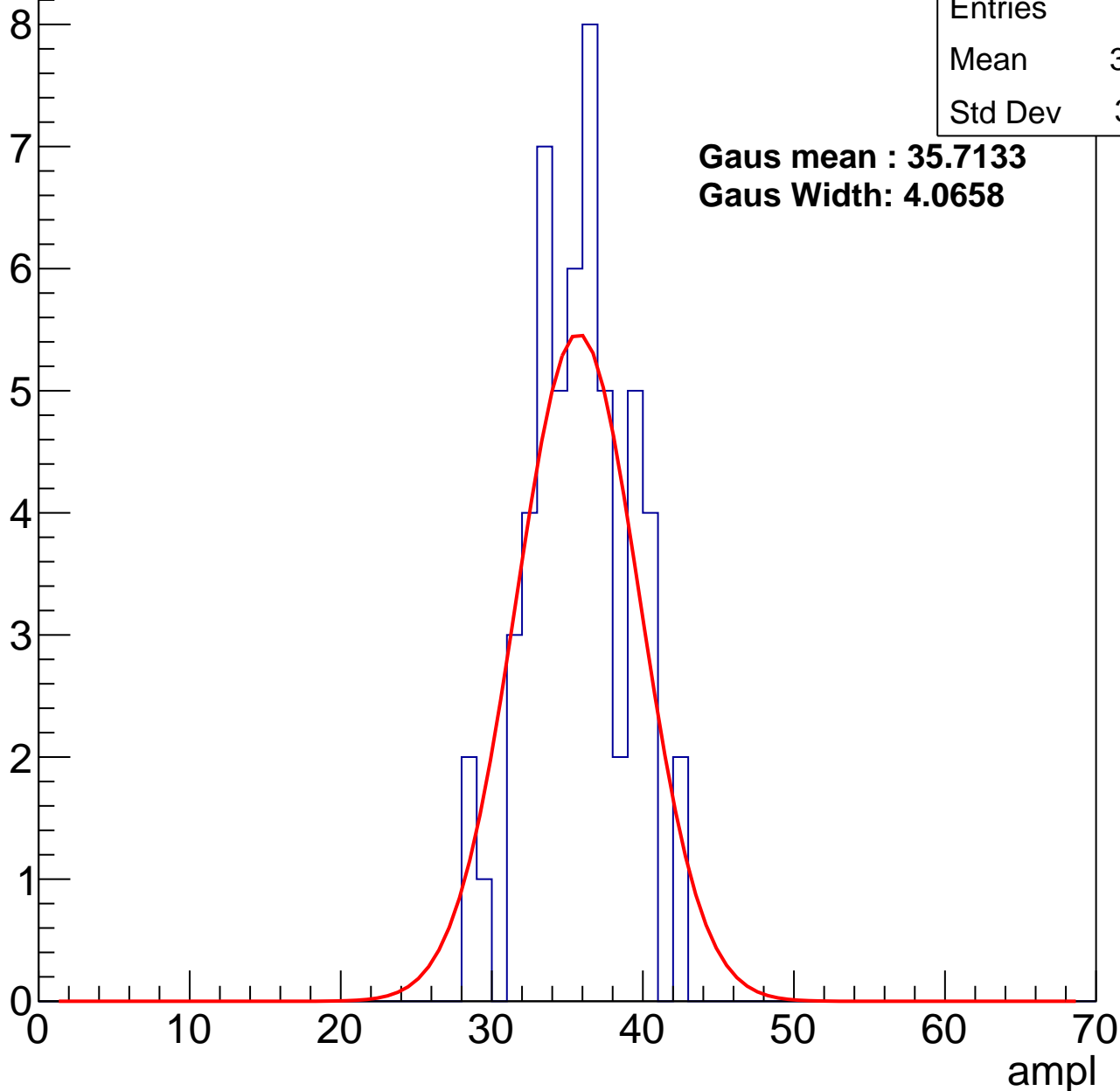
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	35.28
Std Dev	3.251

**Gaus mean : 35.7133**

**Gaus Width: 4.0658**



# B1L103S, U3-ch87, adc2

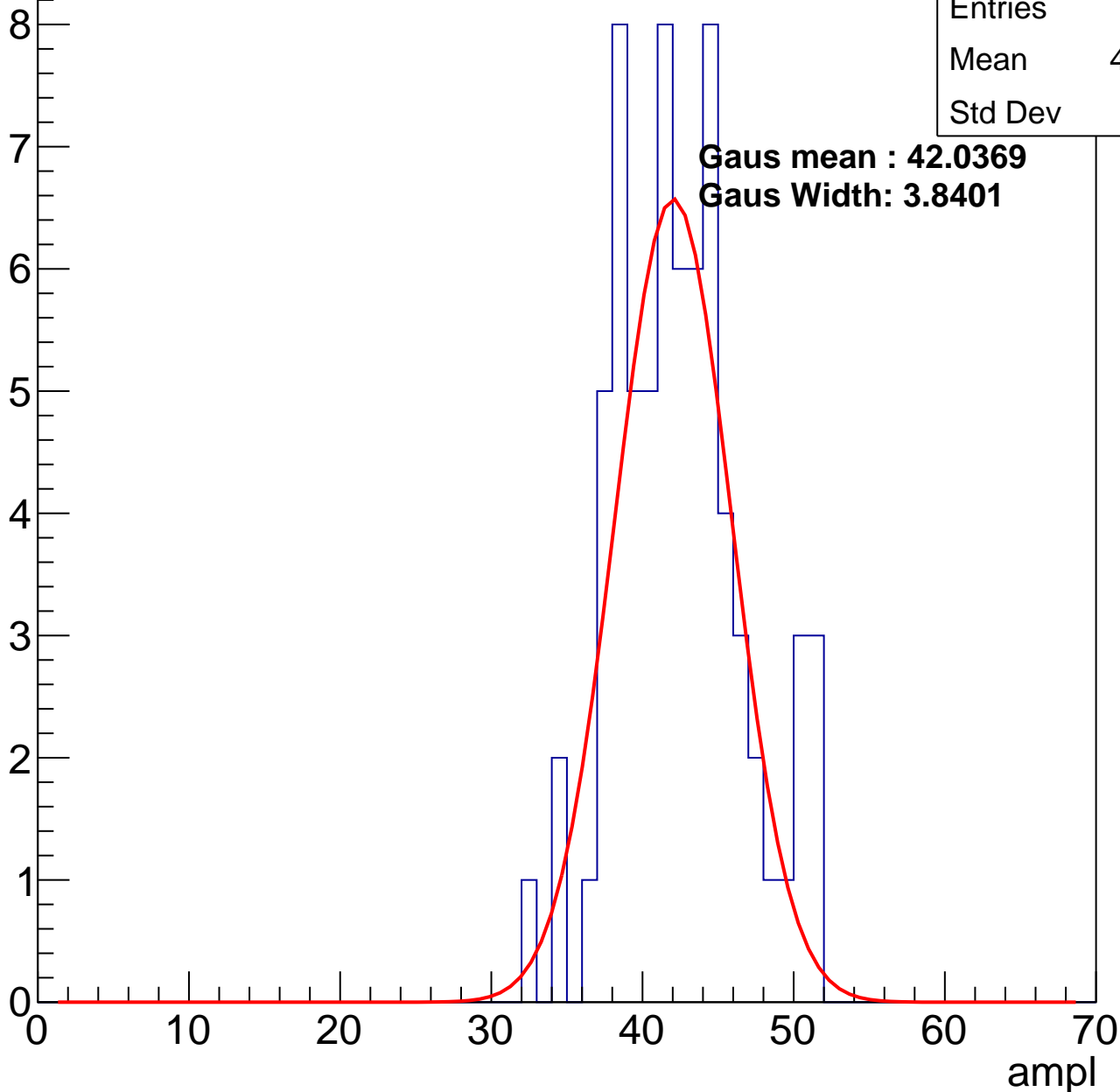
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	41.97
Std Dev	4.22

**Gaus mean : 42.0369**

**Gaus Width: 3.8401**

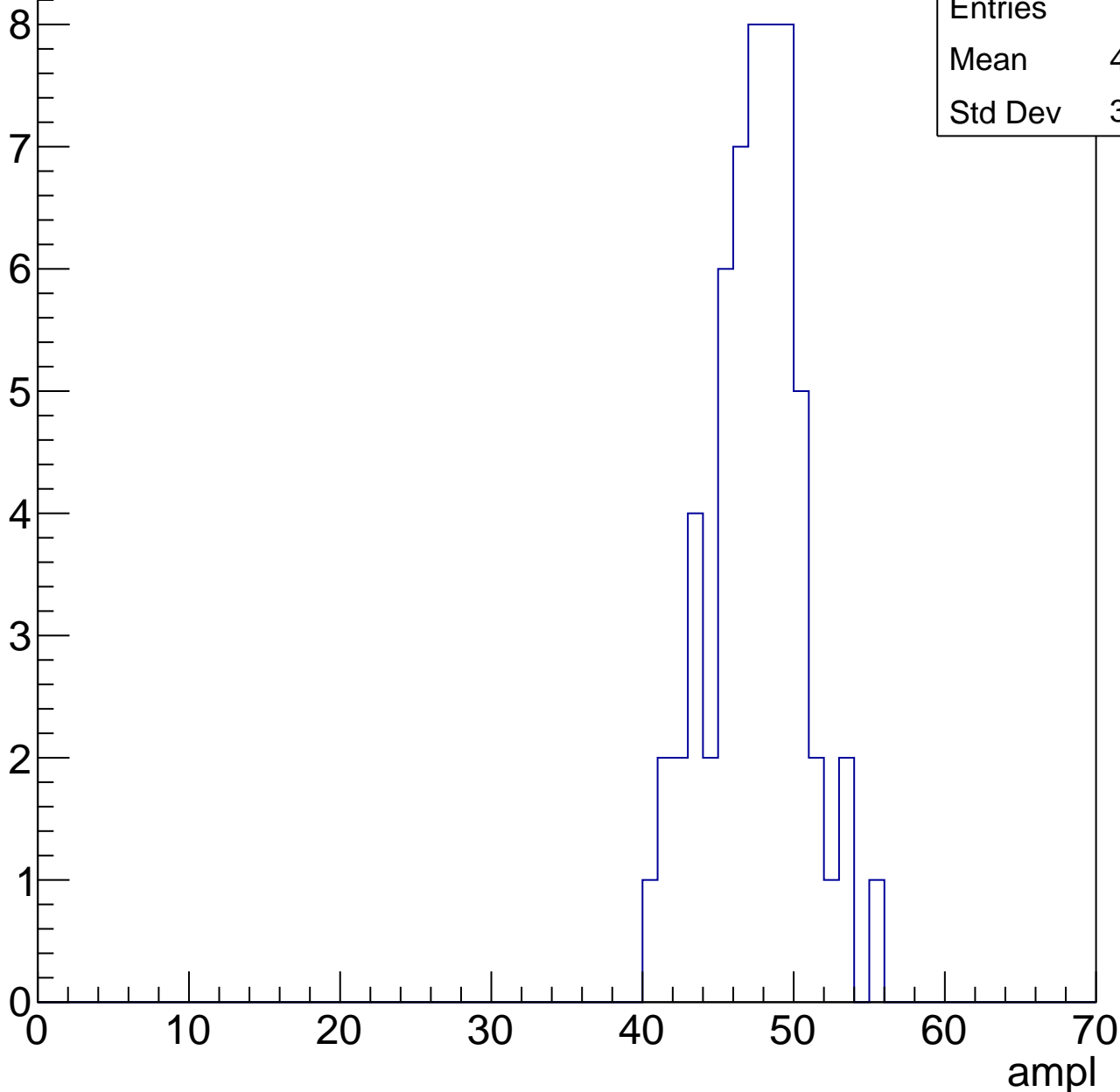


# B1L103S, U3-ch87, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

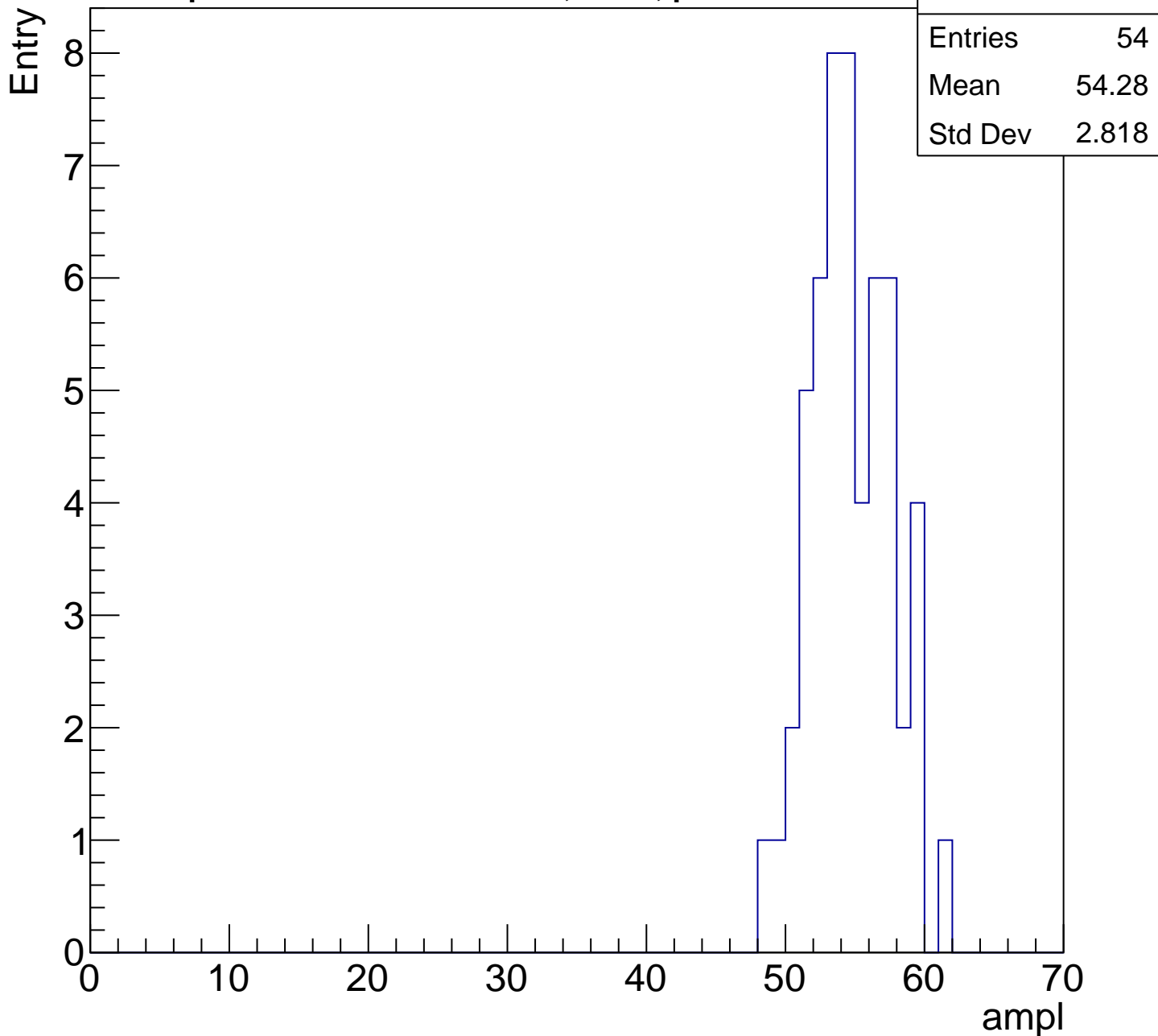
Entry

Entries	59
Mean	47.03
Std Dev	3.086



# B1L103S, U3-ch87, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

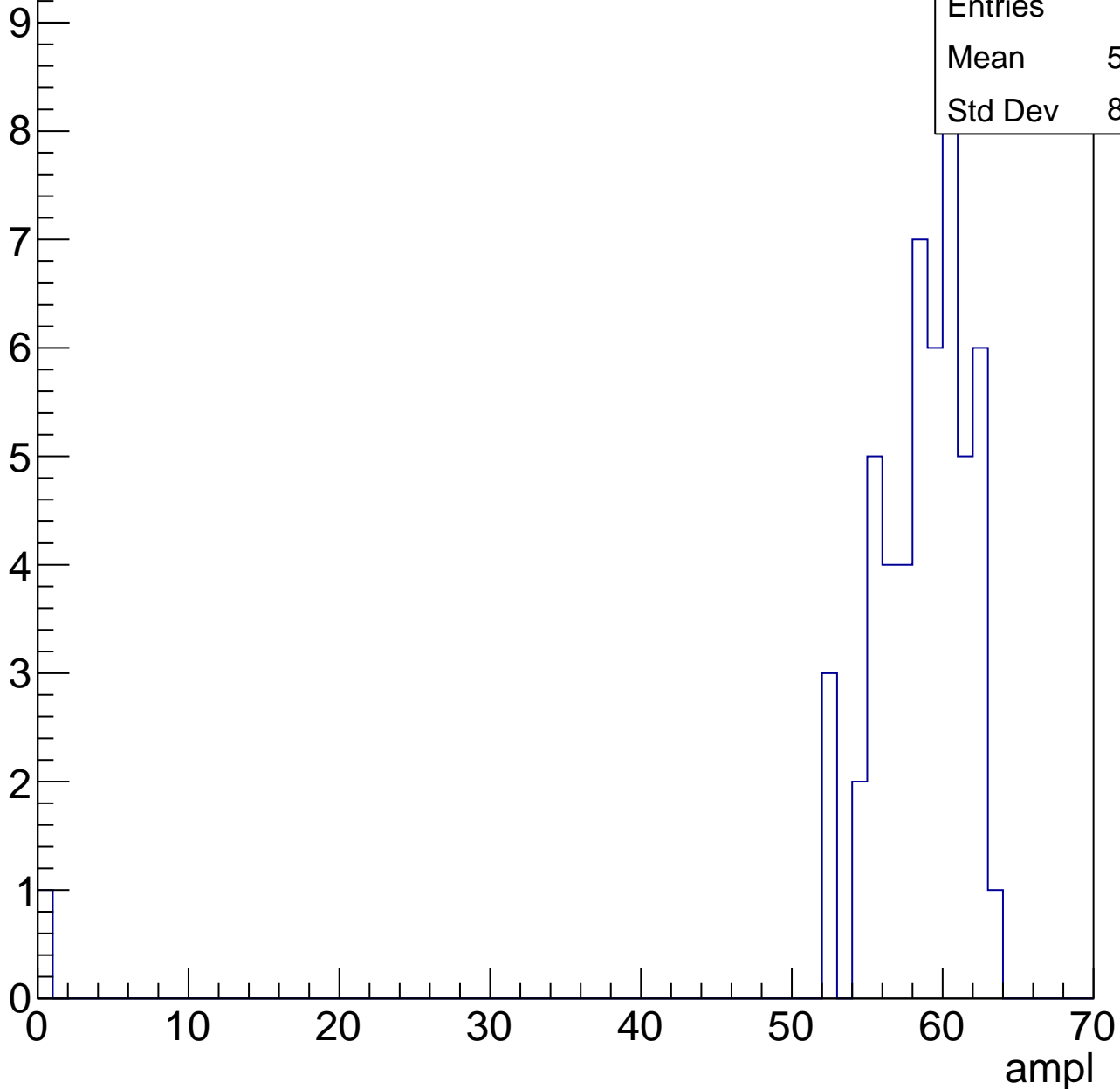


# B1L103S, U3-ch87, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	57.19
Std Dev	8.403

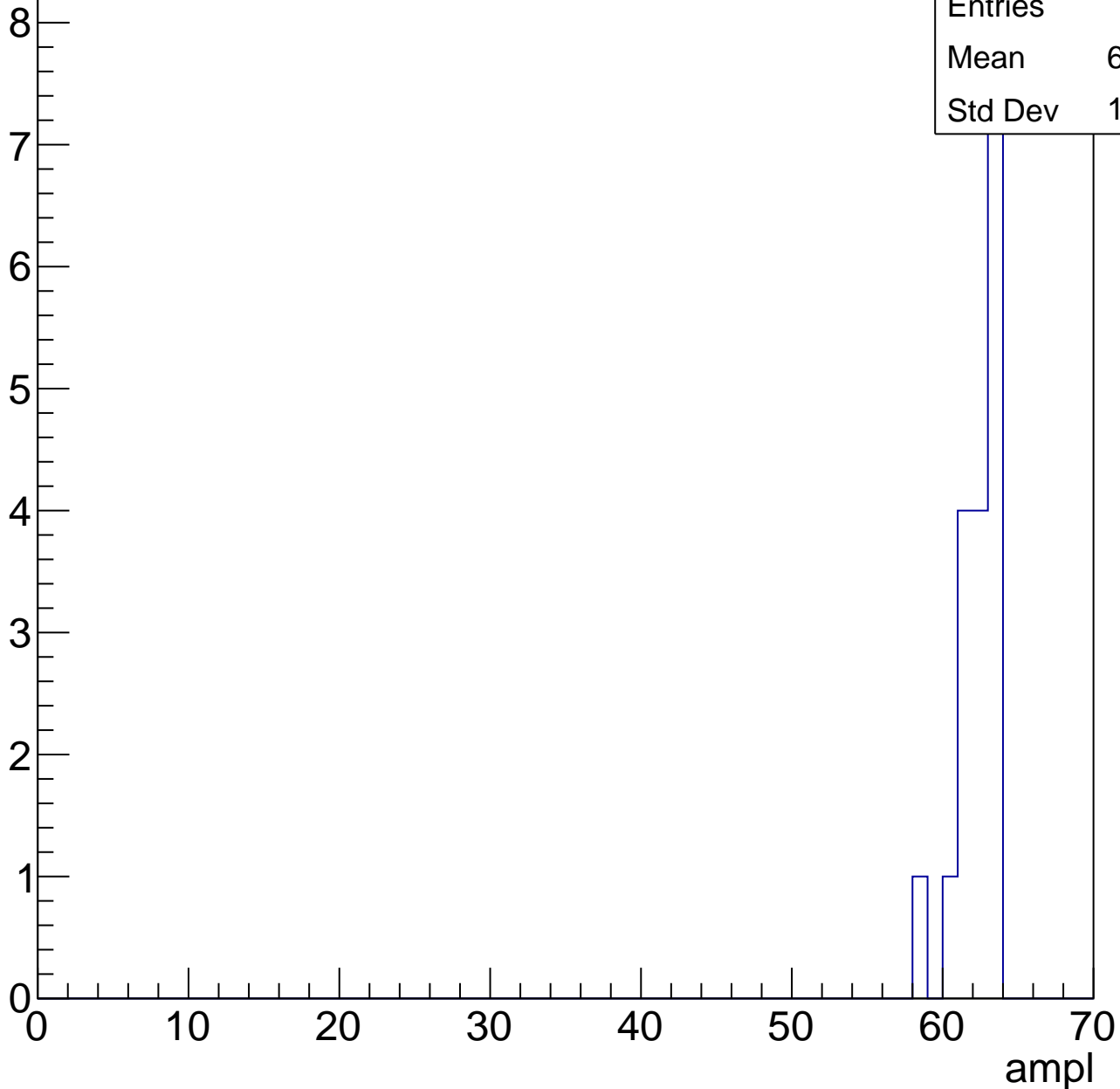


# B1L103S, U3-ch87, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	18
Mean	61.89
Std Dev	1.329

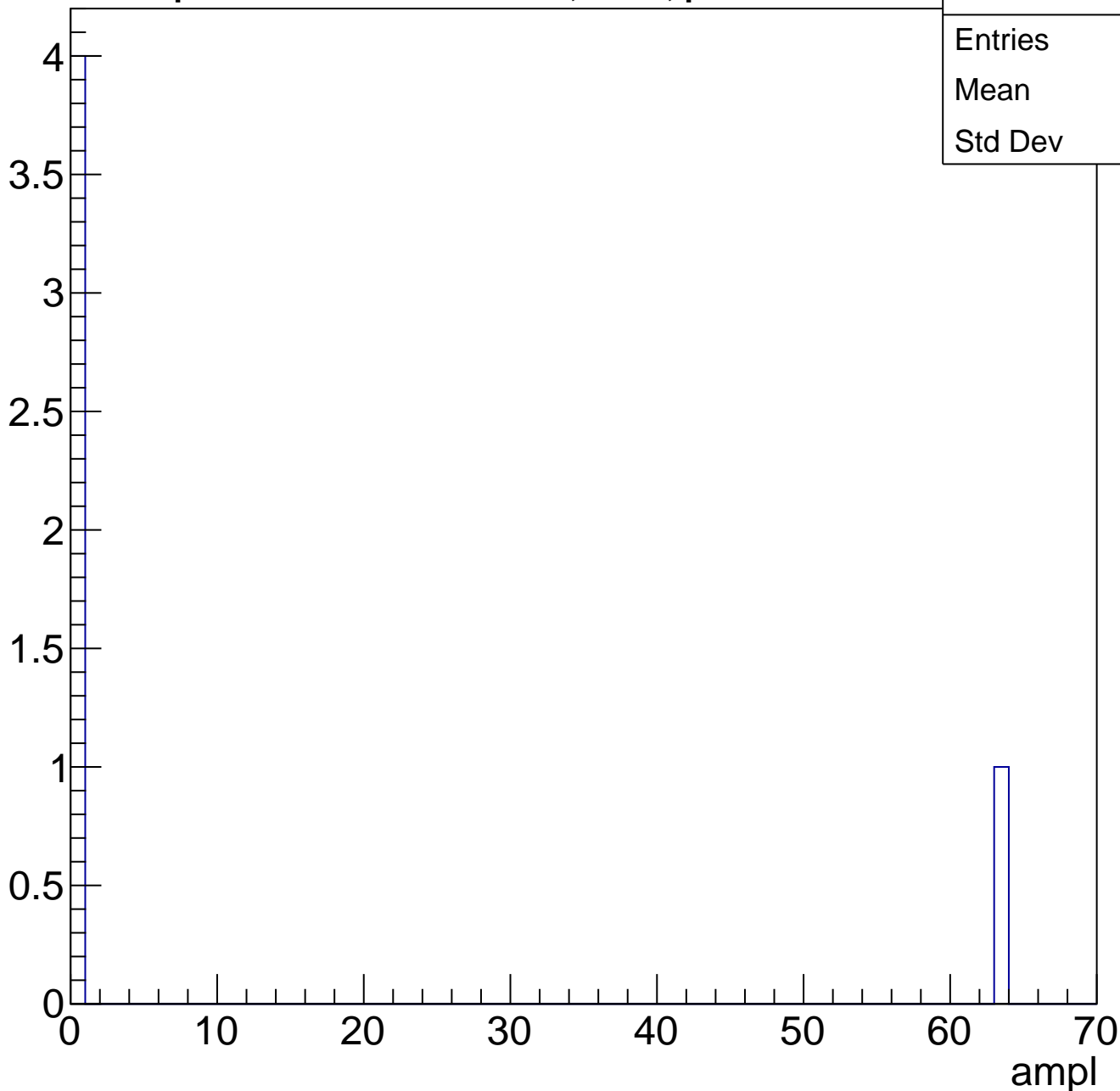




# B1L103S, U3-ch87, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch88, adc0

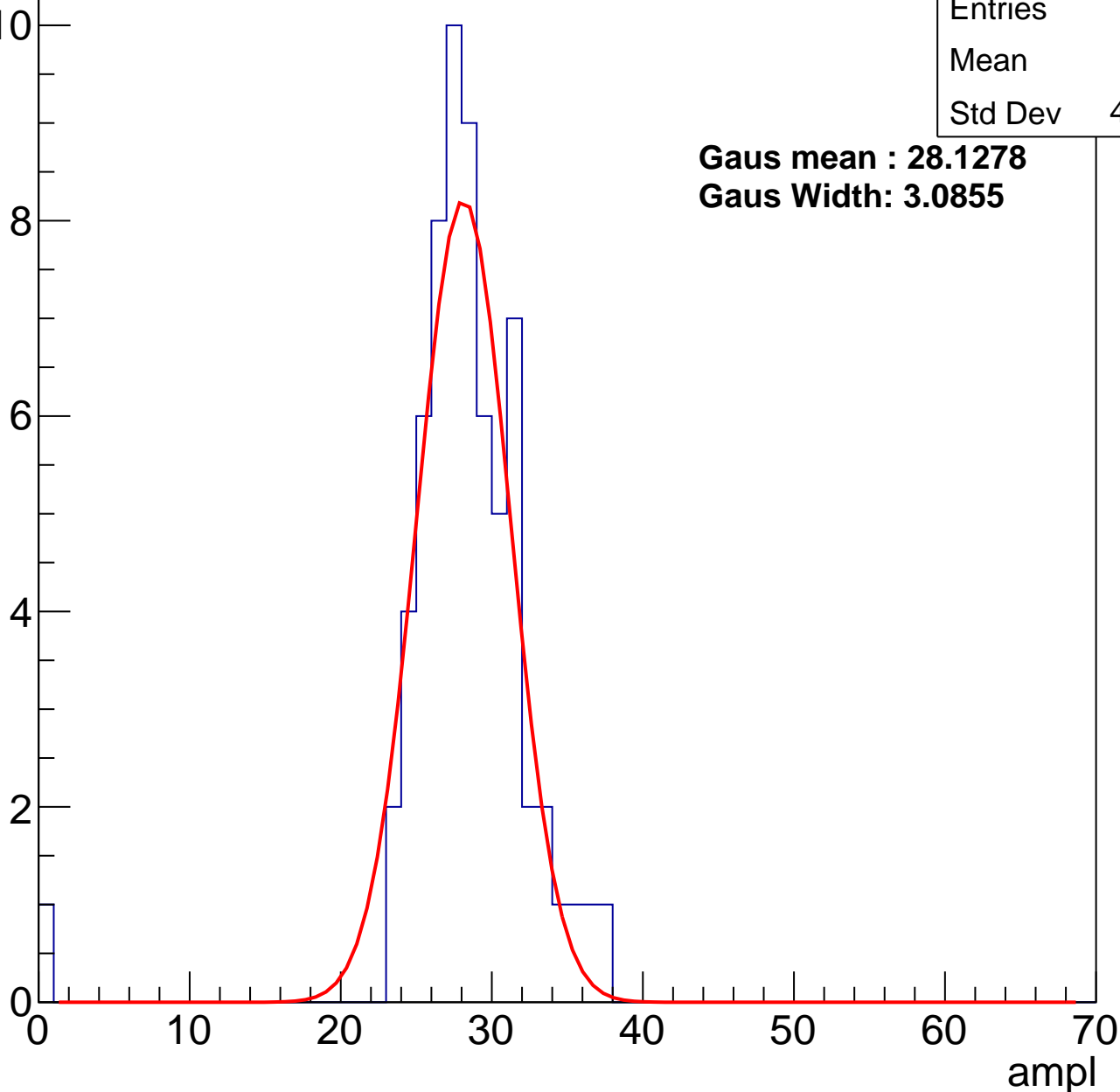
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	27.8
Std Dev	4.593

**Gaus mean : 28.1278**

**Gaus Width: 3.0855**



# B1L103S, U3-ch88, adc1

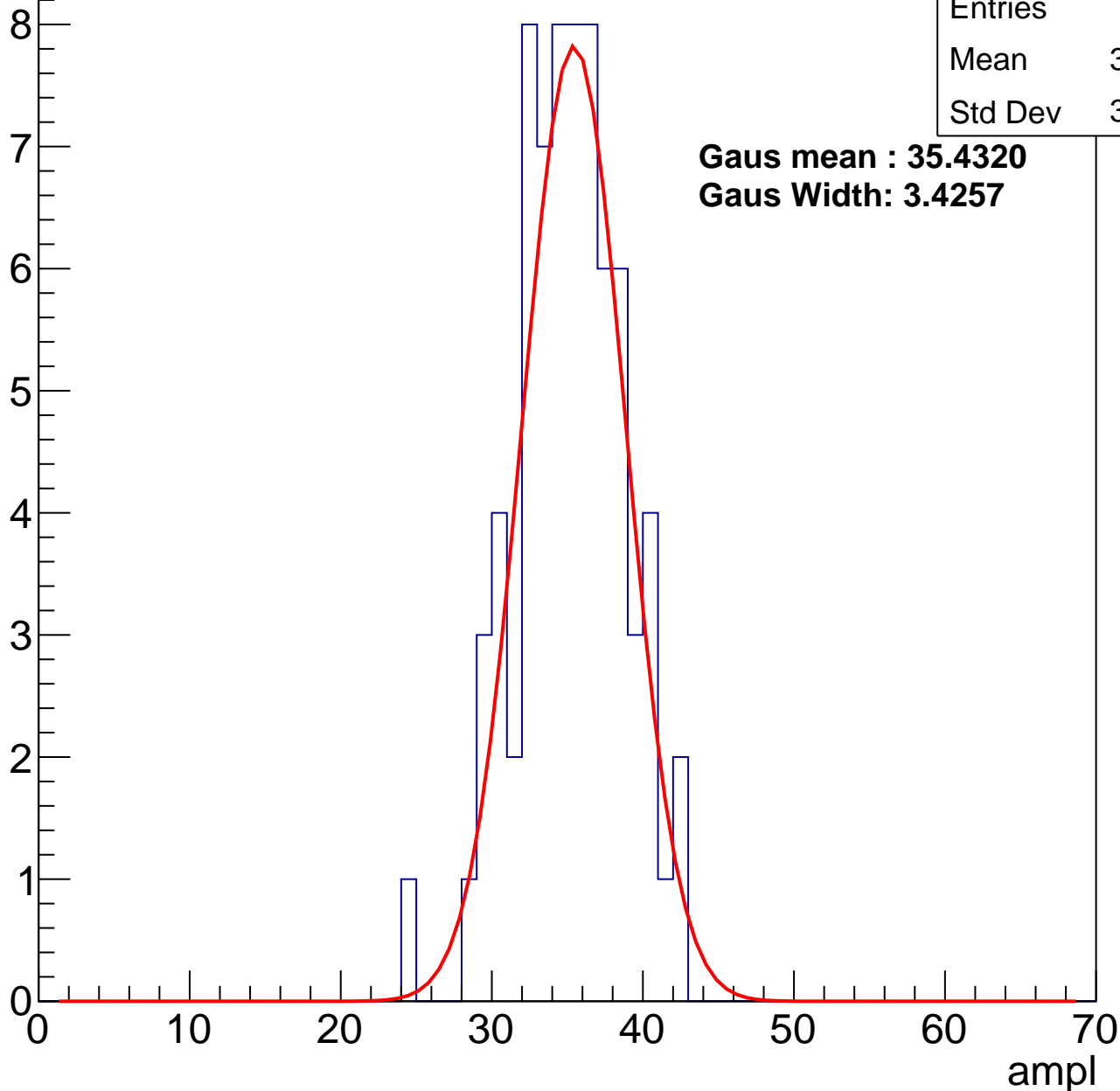
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	34.72
Std Dev	3.497

**Gaus mean : 35.4320**

**Gaus Width: 3.4257**



# B1L103S, U3-ch88, adc2

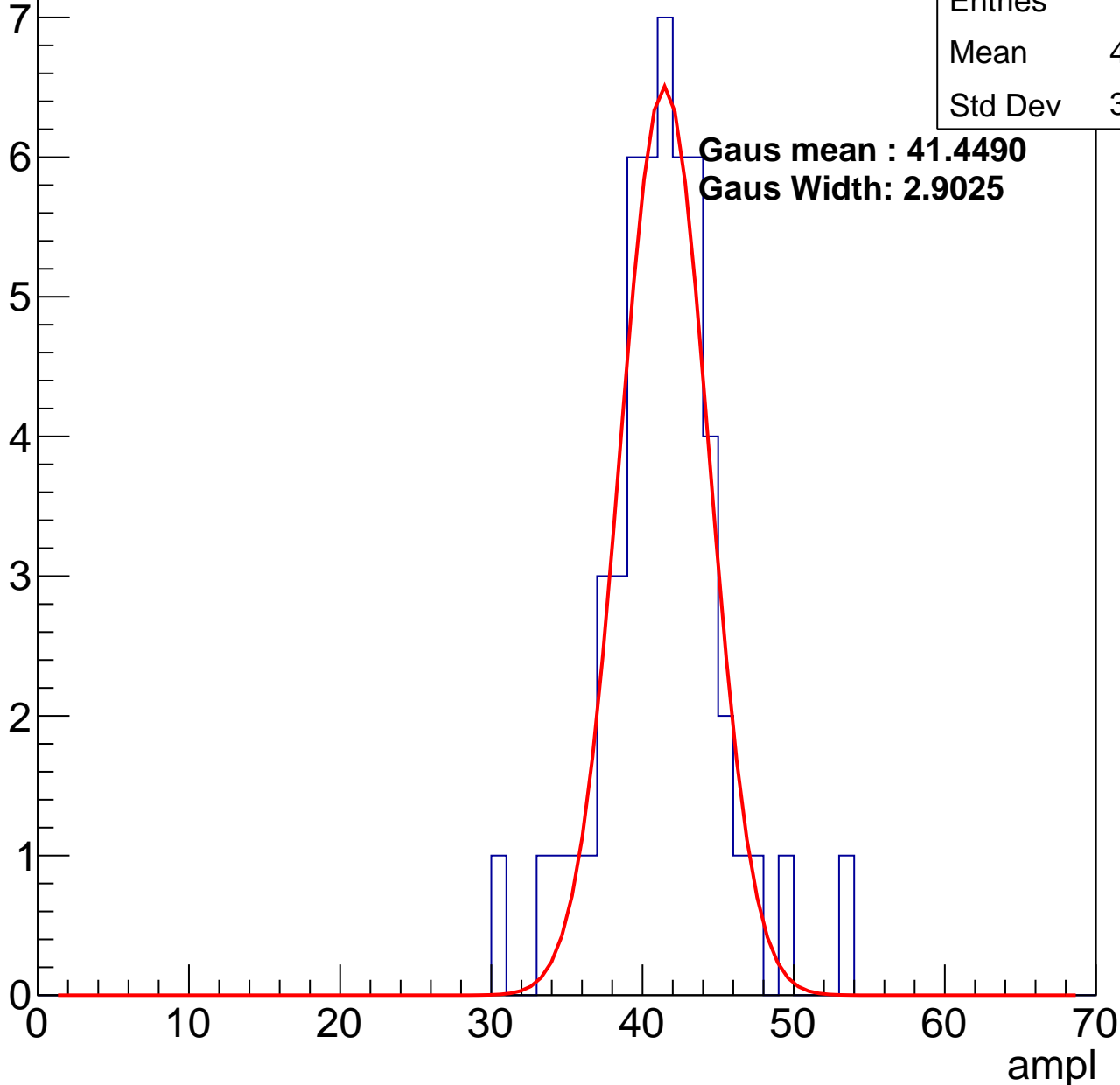
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	40.87
Std Dev	3.838

**Gaus mean : 41.4490**

**Gaus Width: 2.9025**

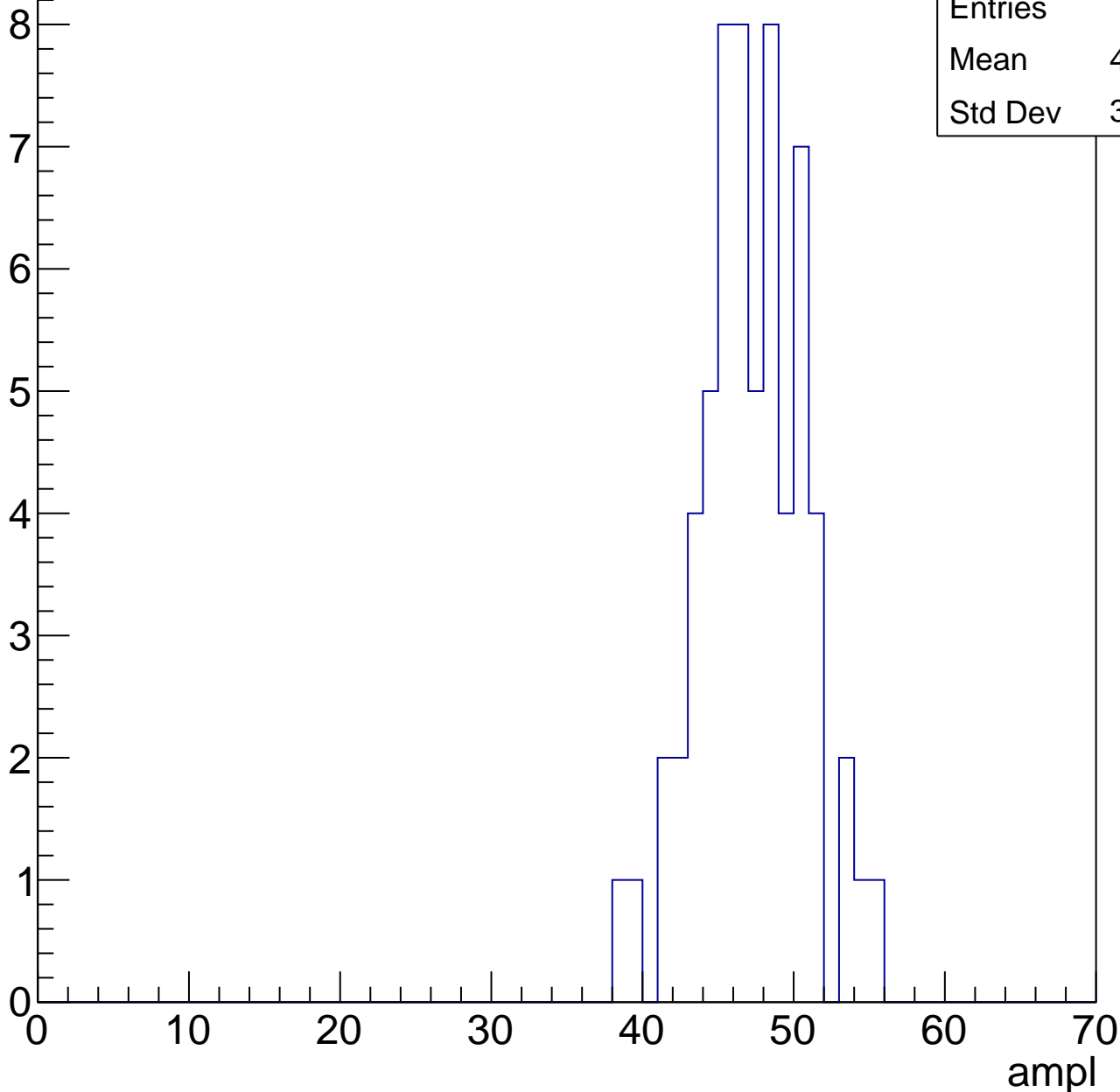


# B1L103S, U3-ch88, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	46.78
Std Dev	3.448

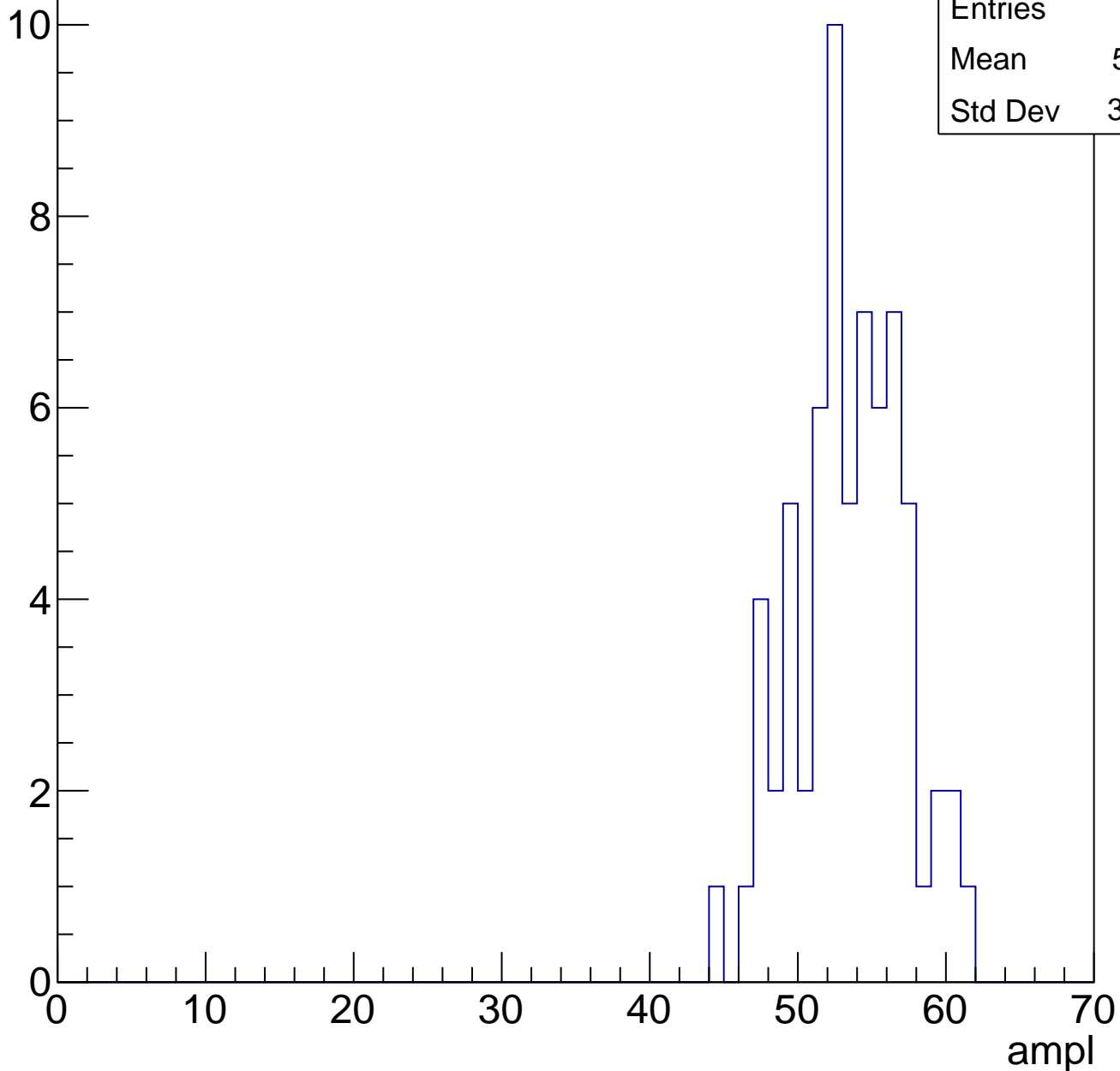


# B1L103S, U3-ch88, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	67
Mean	53.01
Std Dev	3.643

Entry



# B1L103S, U3-ch88, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

7

6

5

4

3

2

1

0

Entries 47

Mean 57.6

Std Dev 8.996

ampl

0

10

20

30

40

50

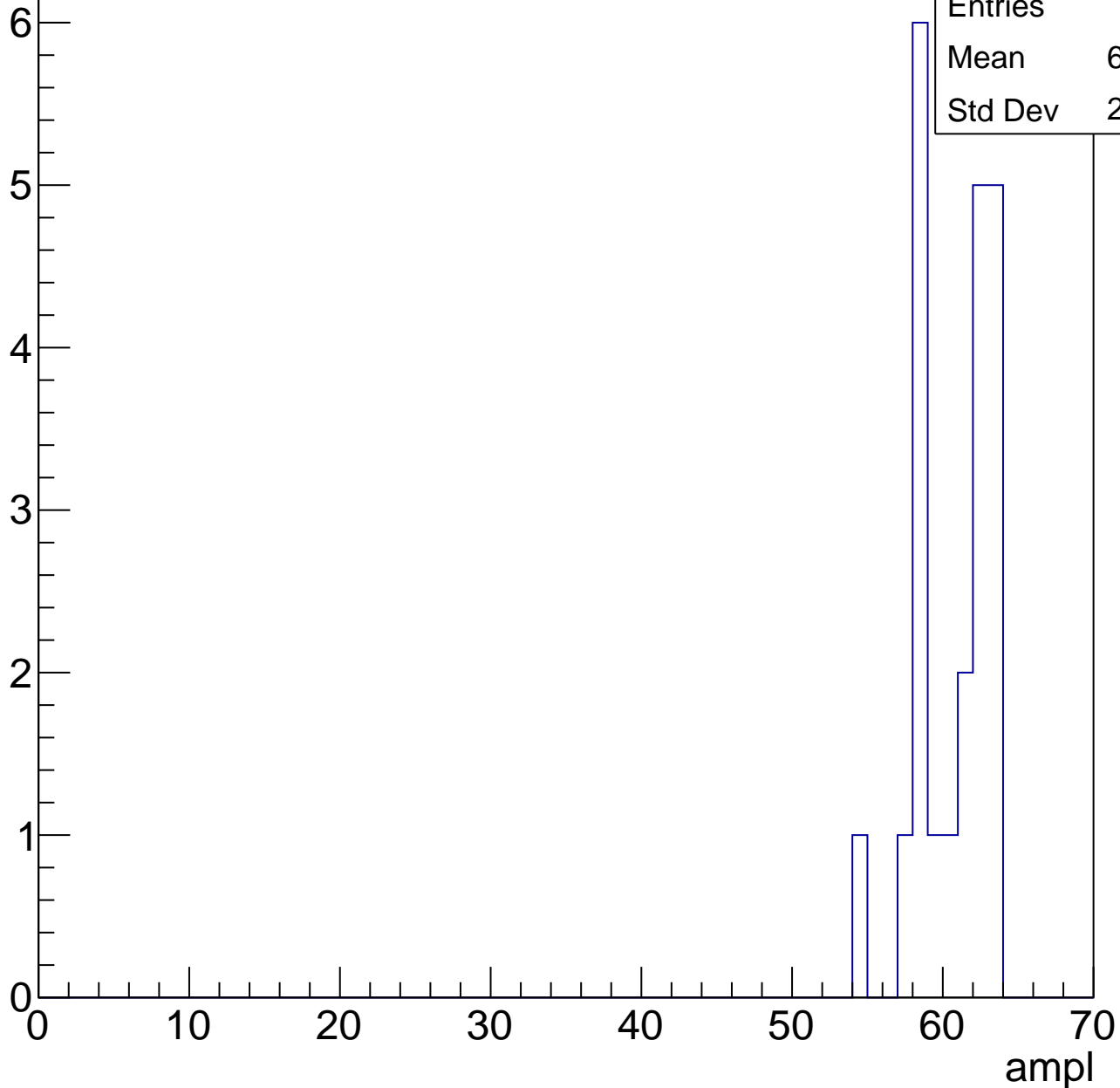
60

70

# B1L103S, U3-ch88, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

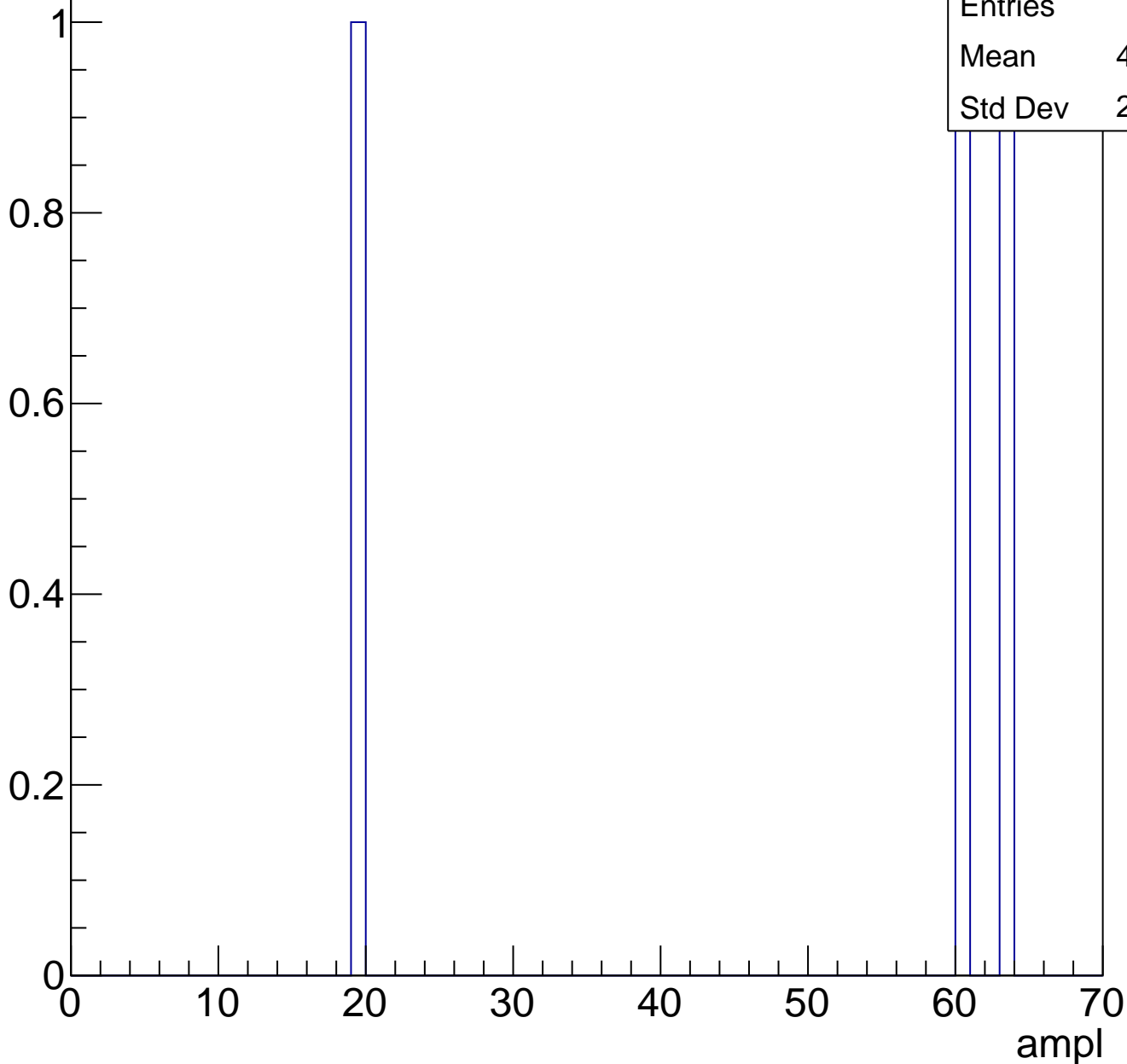




# B1L103S, U3-ch88, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch89, adc0

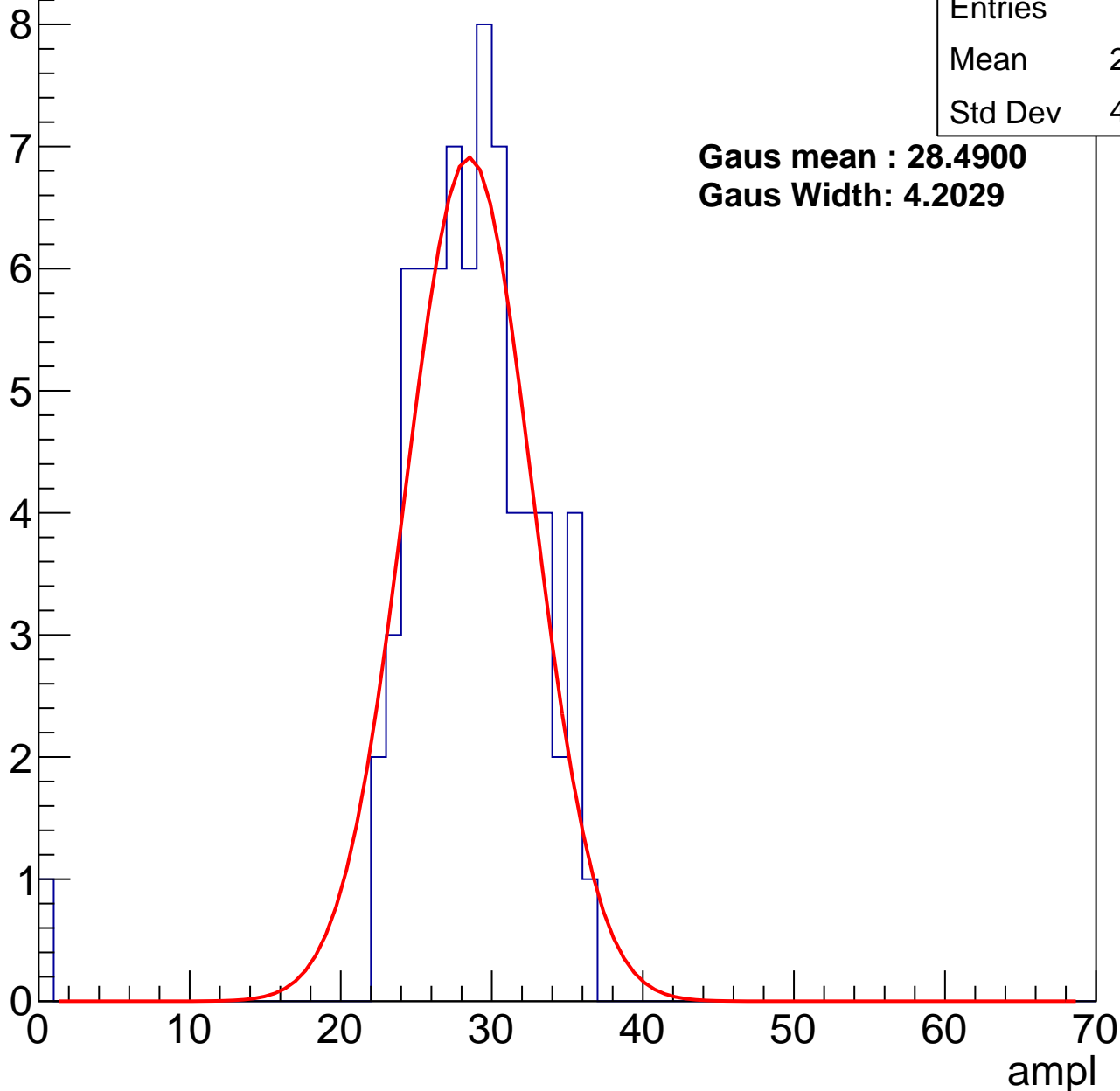
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	28.03
Std Dev	4.864

**Gaus mean : 28.4900**

**Gaus Width: 4.2029**



# B1L103S, U3-ch89, adc1

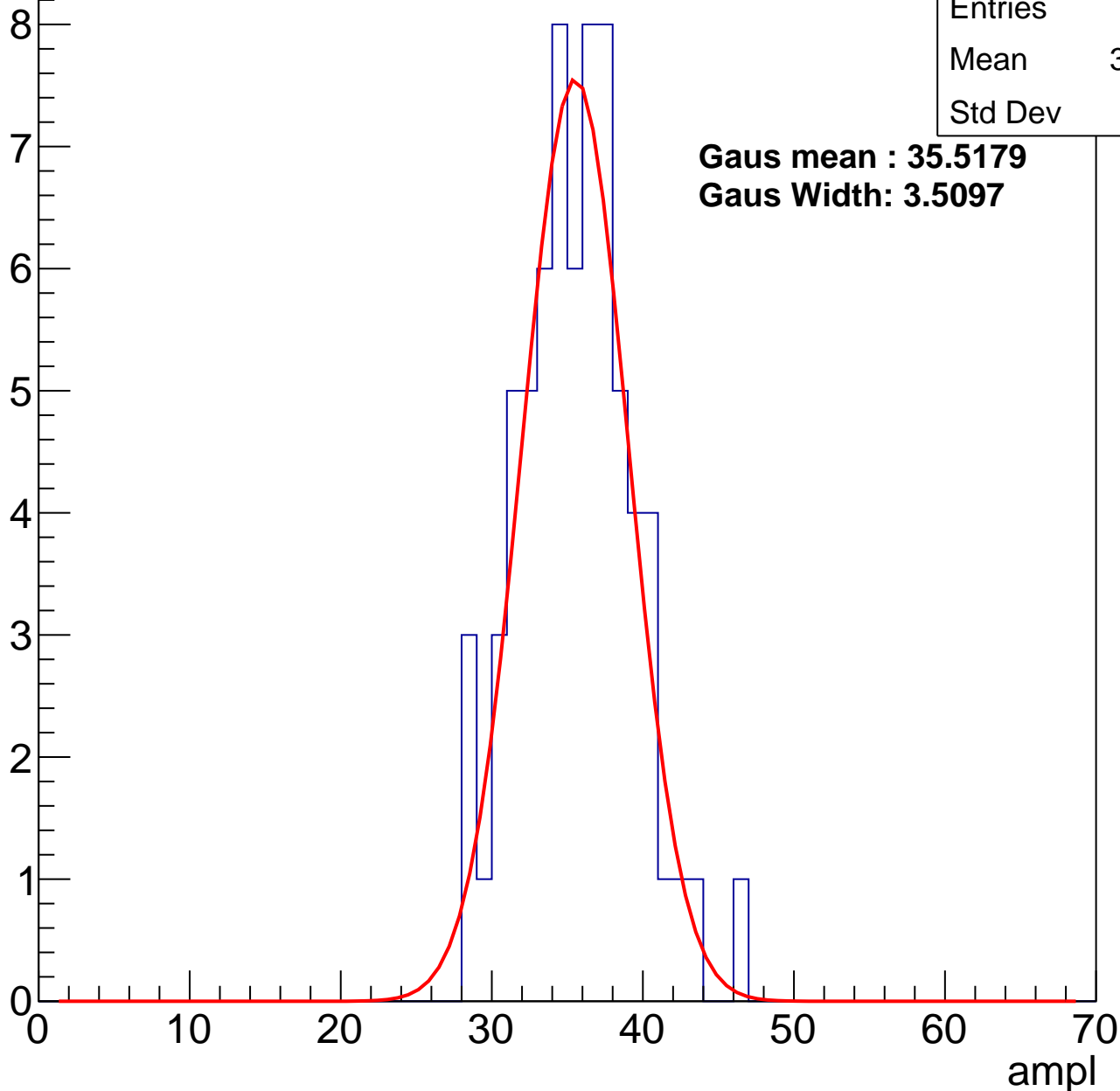
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	35.14
Std Dev	3.65

**Gaus mean : 35.5179**

**Gaus Width: 3.5097**



# B1L103S, U3-ch89, adc2

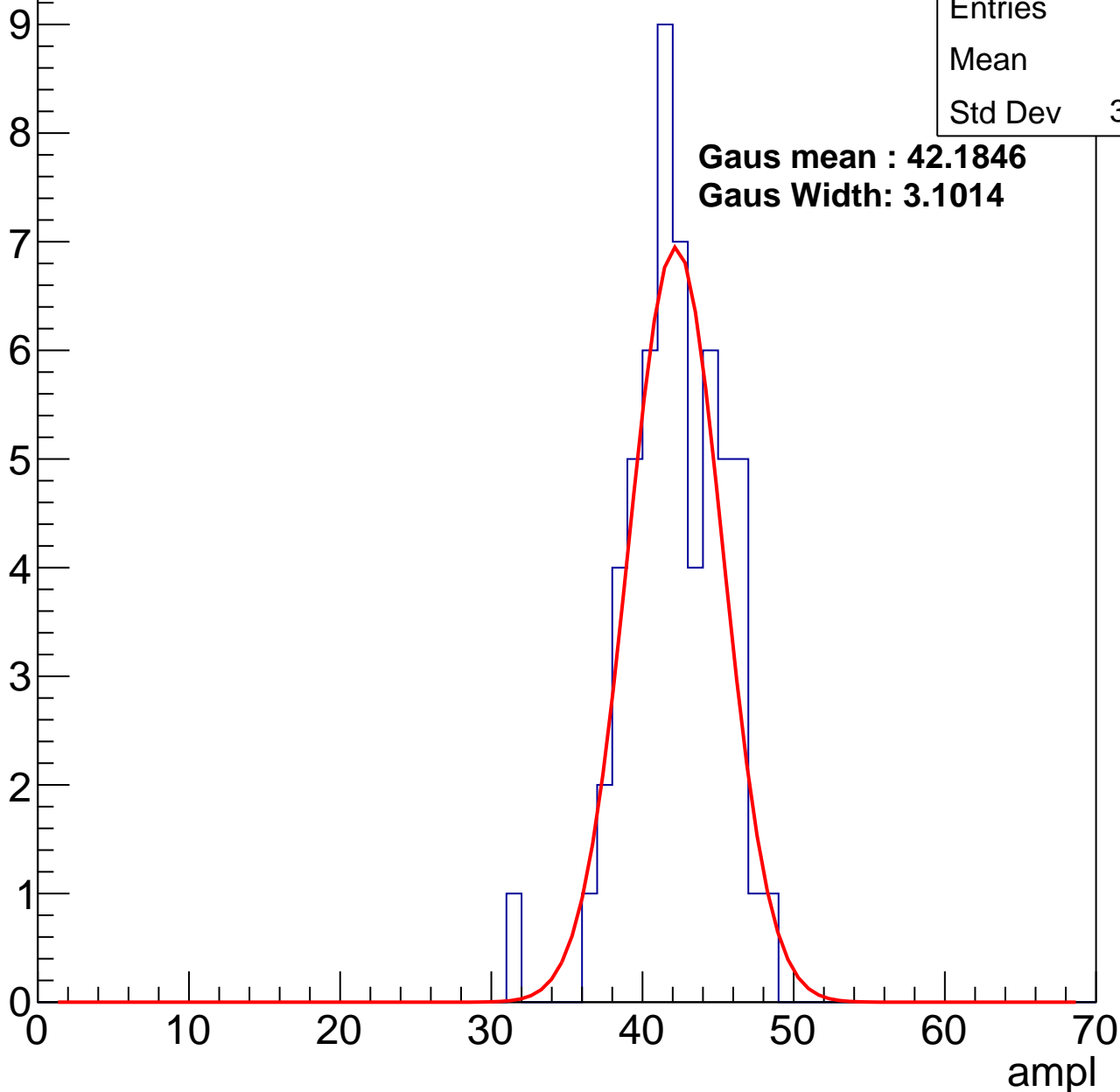
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	41.7
Std Dev	3.129

**Gaus mean : 42.1846**

**Gaus Width: 3.1014**

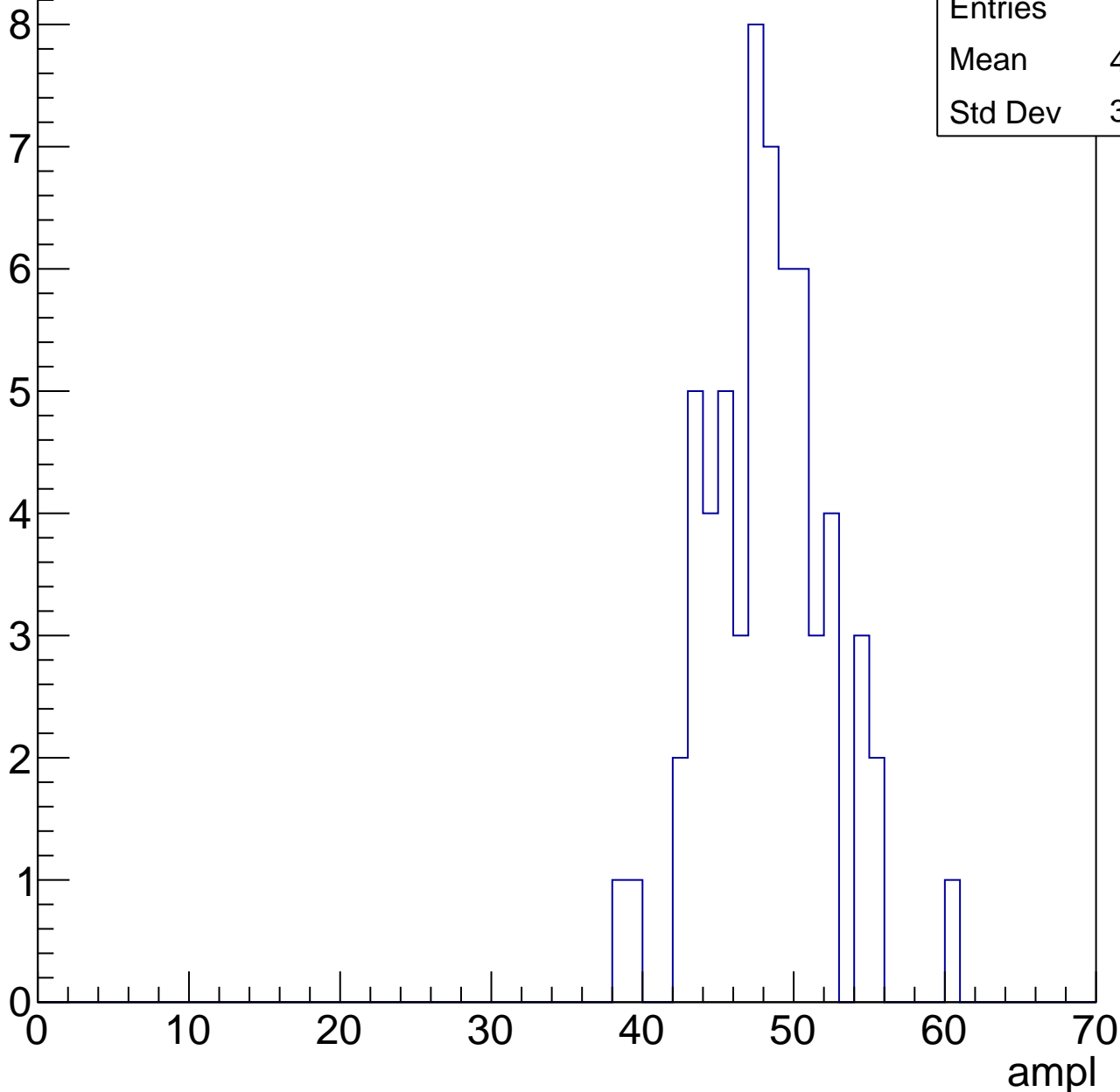


# B1L103S, U3-ch89, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

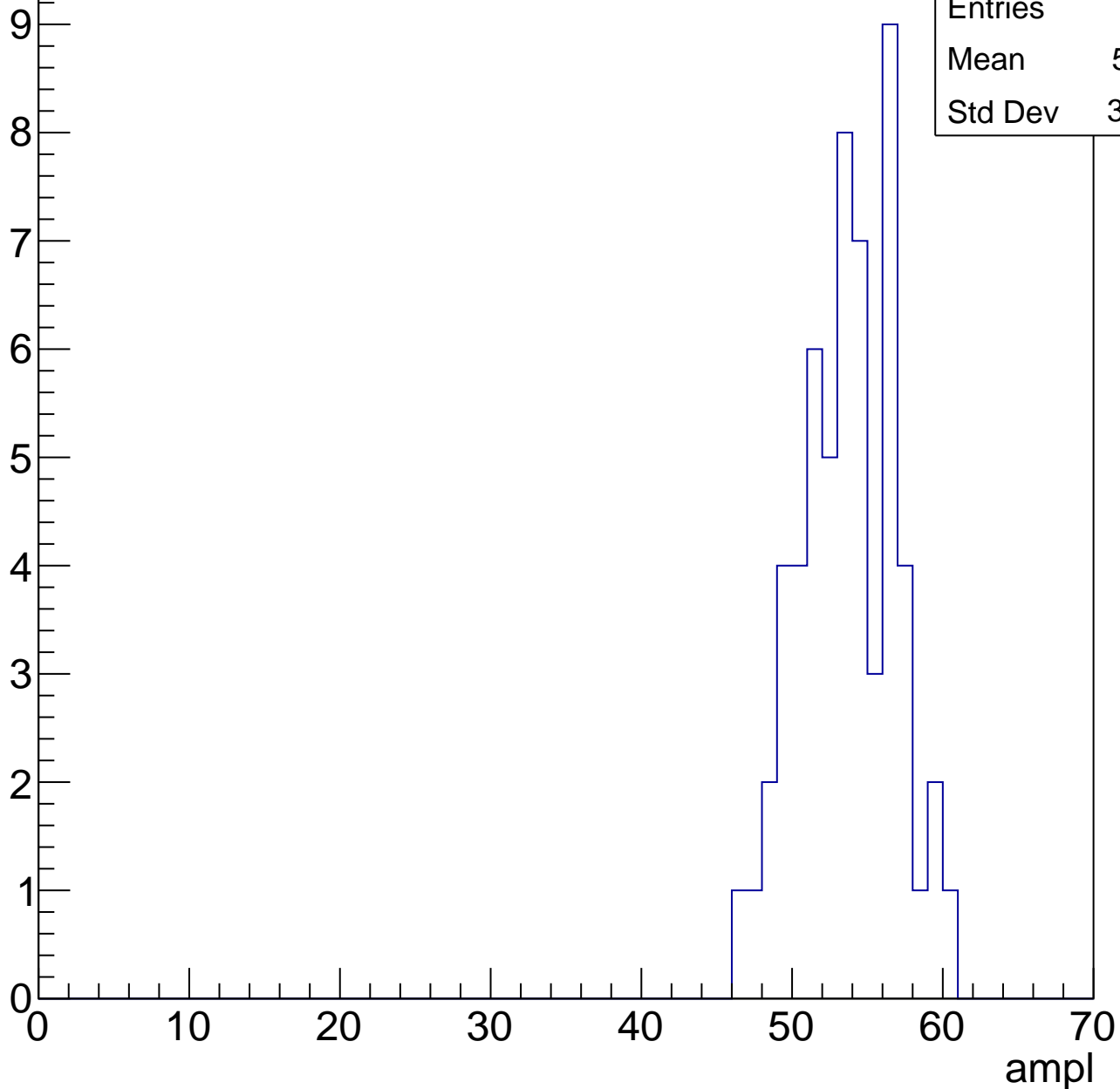
Entries	61
Mean	47.77
Std Dev	3.998



# B1L103S, U3-ch89, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

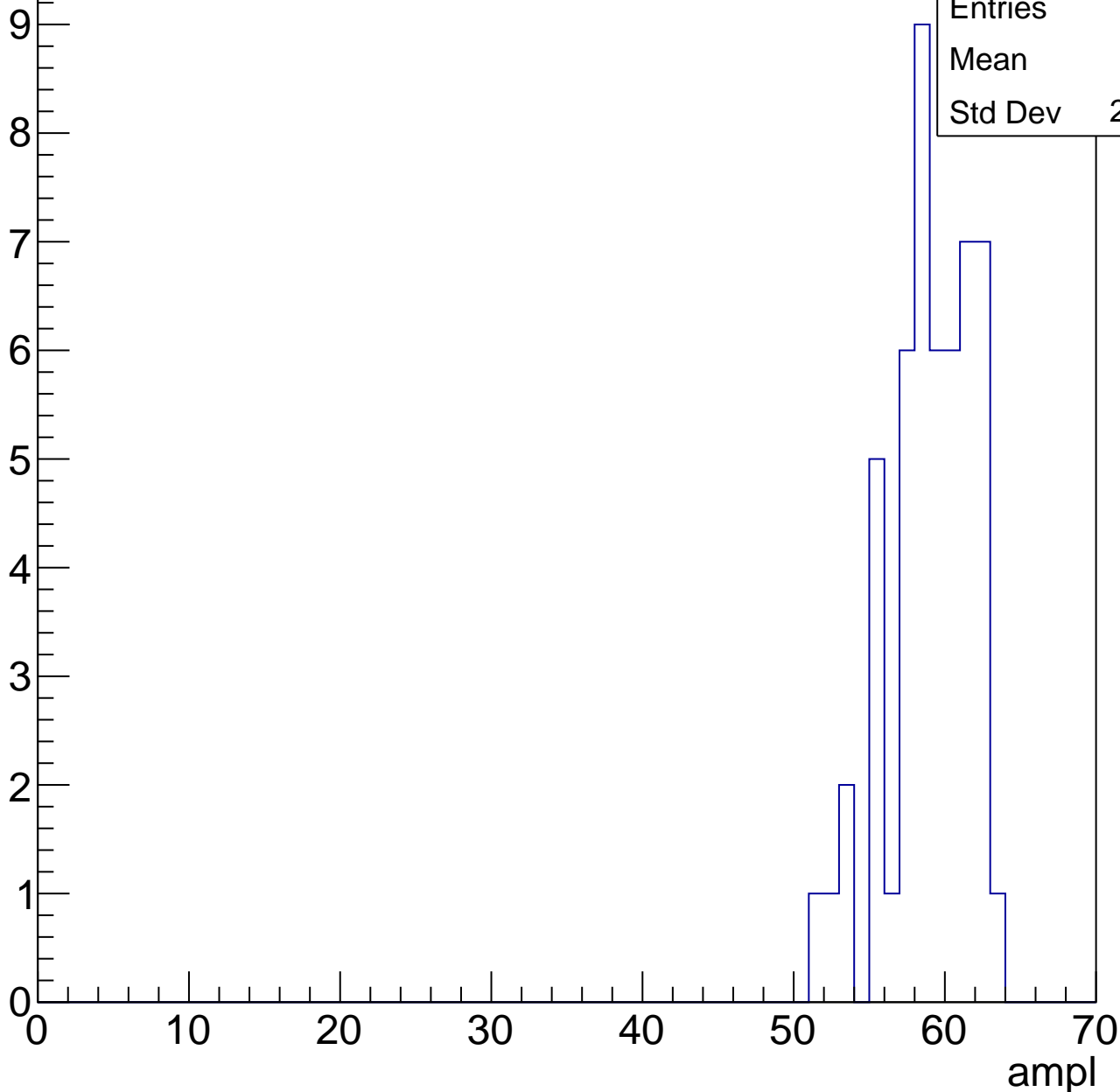


# B1L103S, U3-ch89, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	58.5
Std Dev	2.798

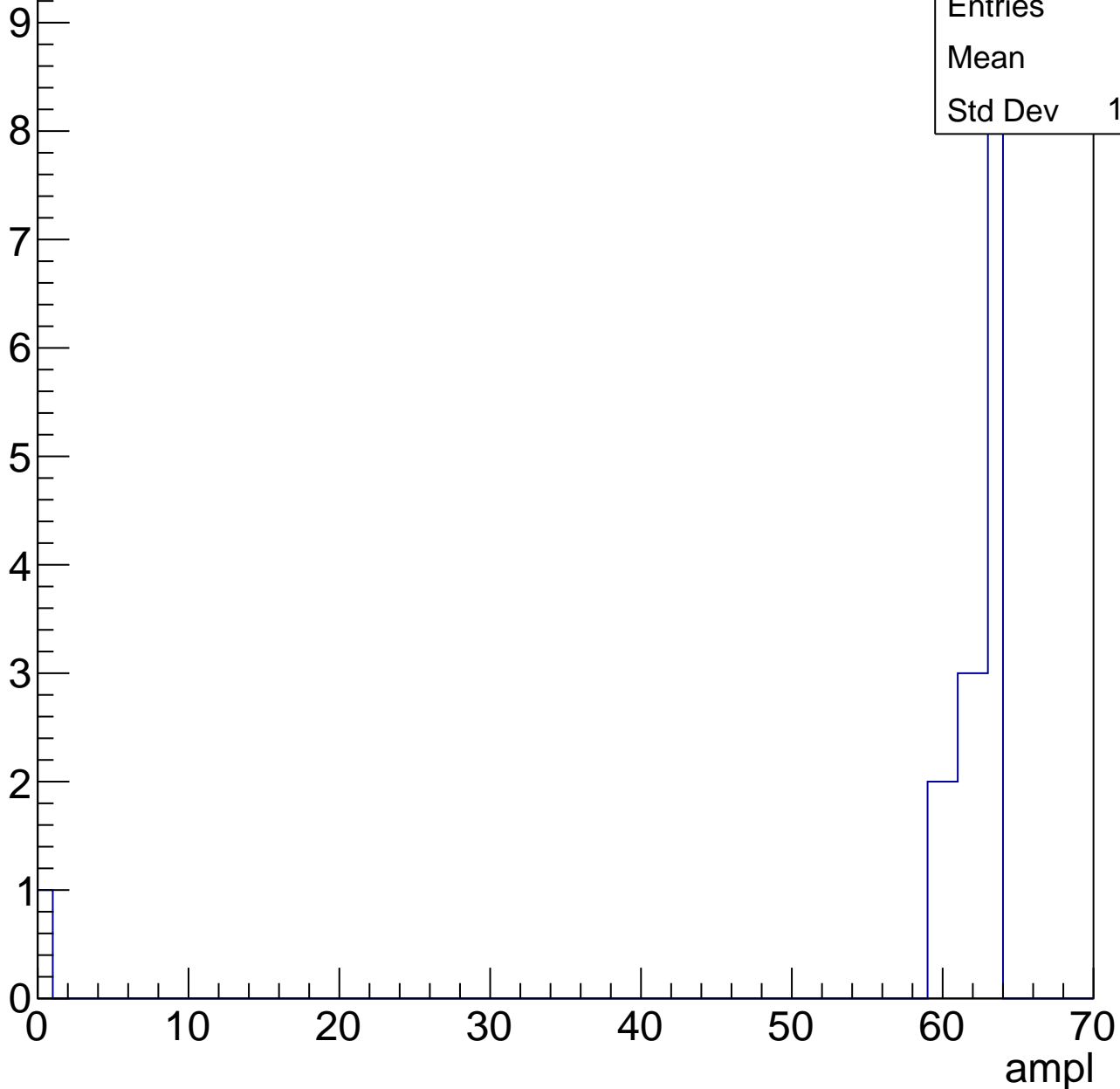


# B1L103S, U3-ch89, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	20
Mean	58.7
Std Dev	13.54





# B1L103S, U3-ch89, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch90, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	74
Mean	26.77
Std Dev	5.858

**Gaus mean : 27.9595**

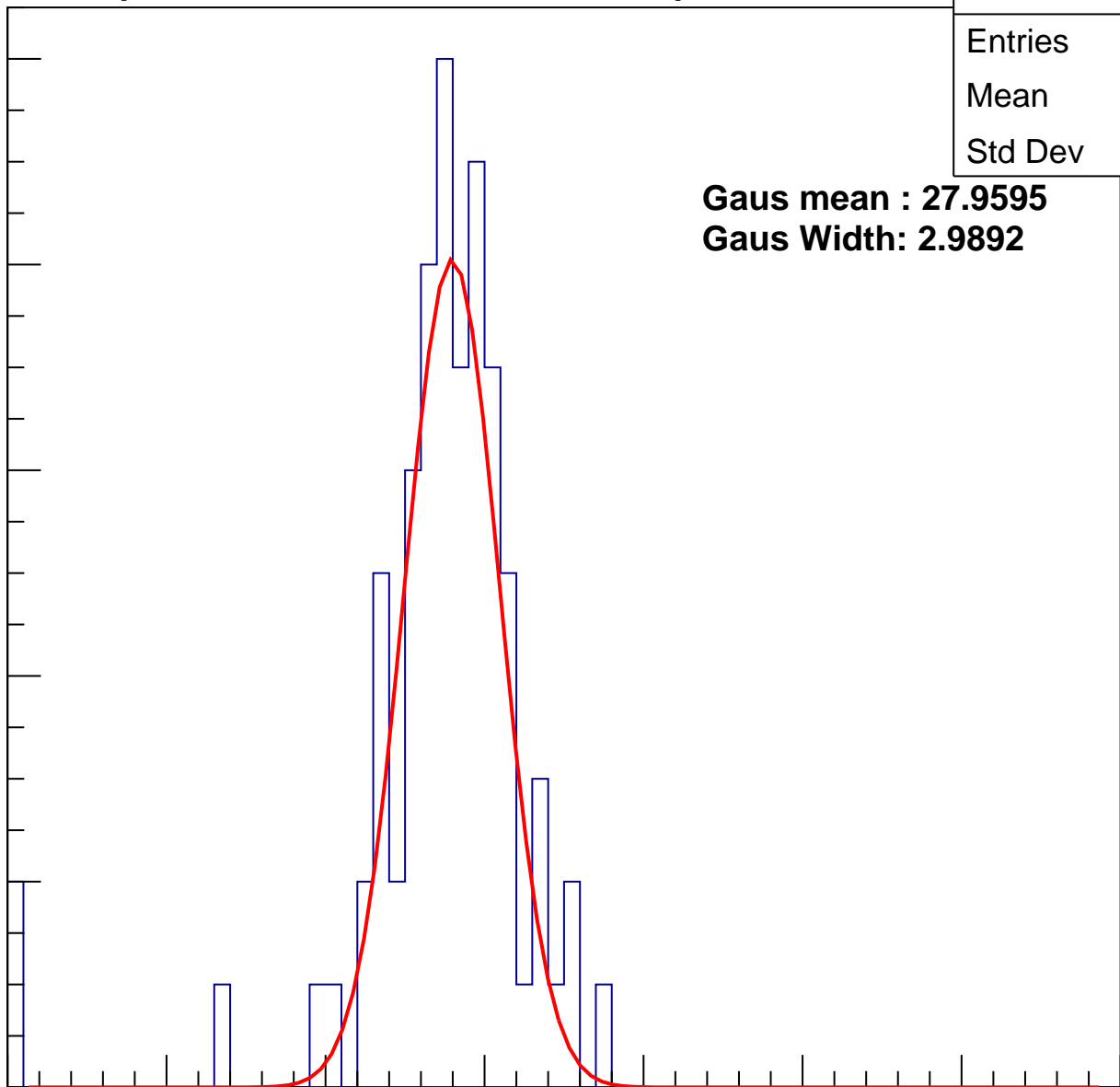
**Gaus Width: 2.9892**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U3-ch90, adc1

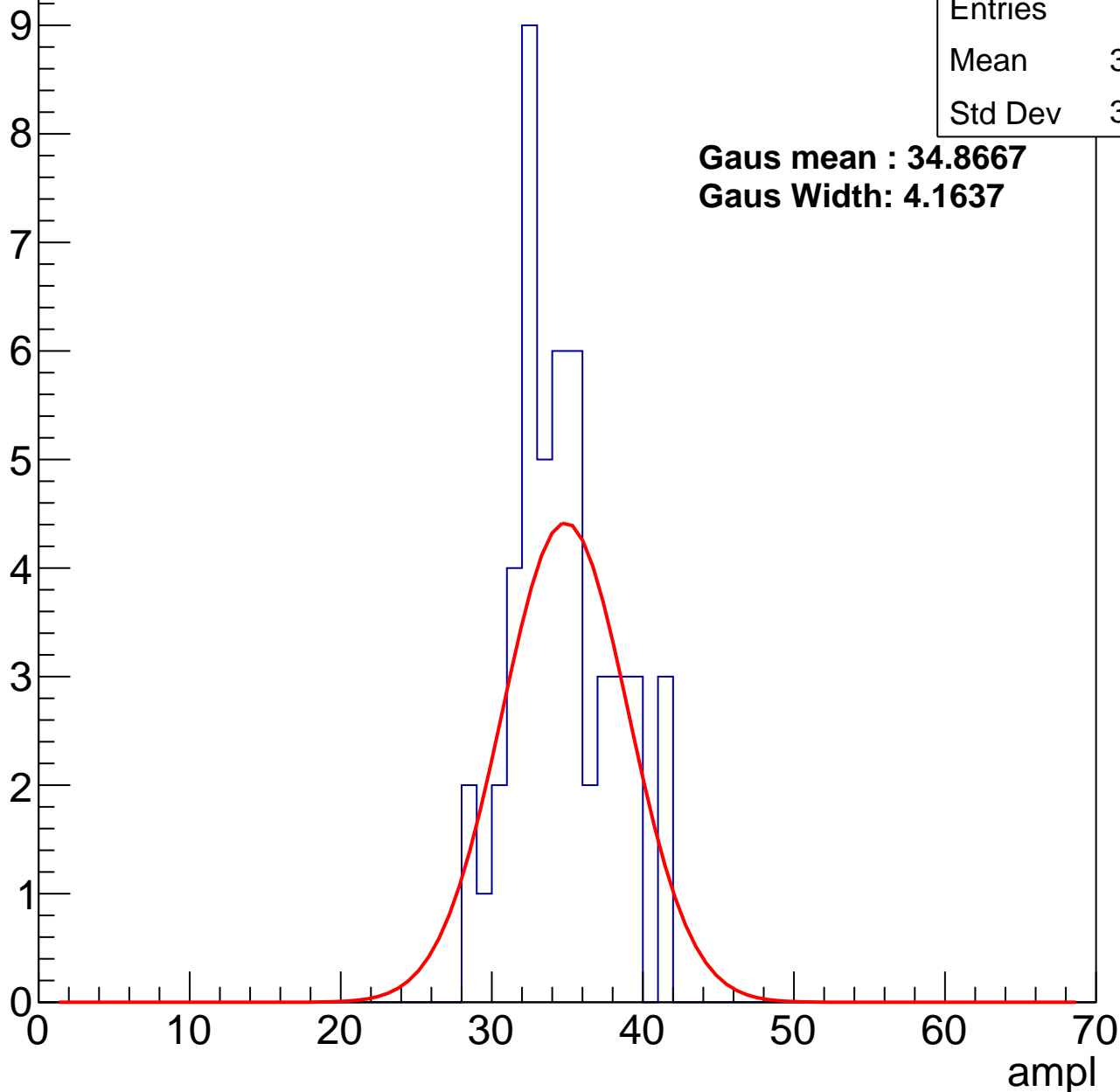
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	34.14
Std Dev	3.245

**Gaus mean : 34.8667**

**Gaus Width: 4.1637**



# B1L103S, U3-ch90, adc2

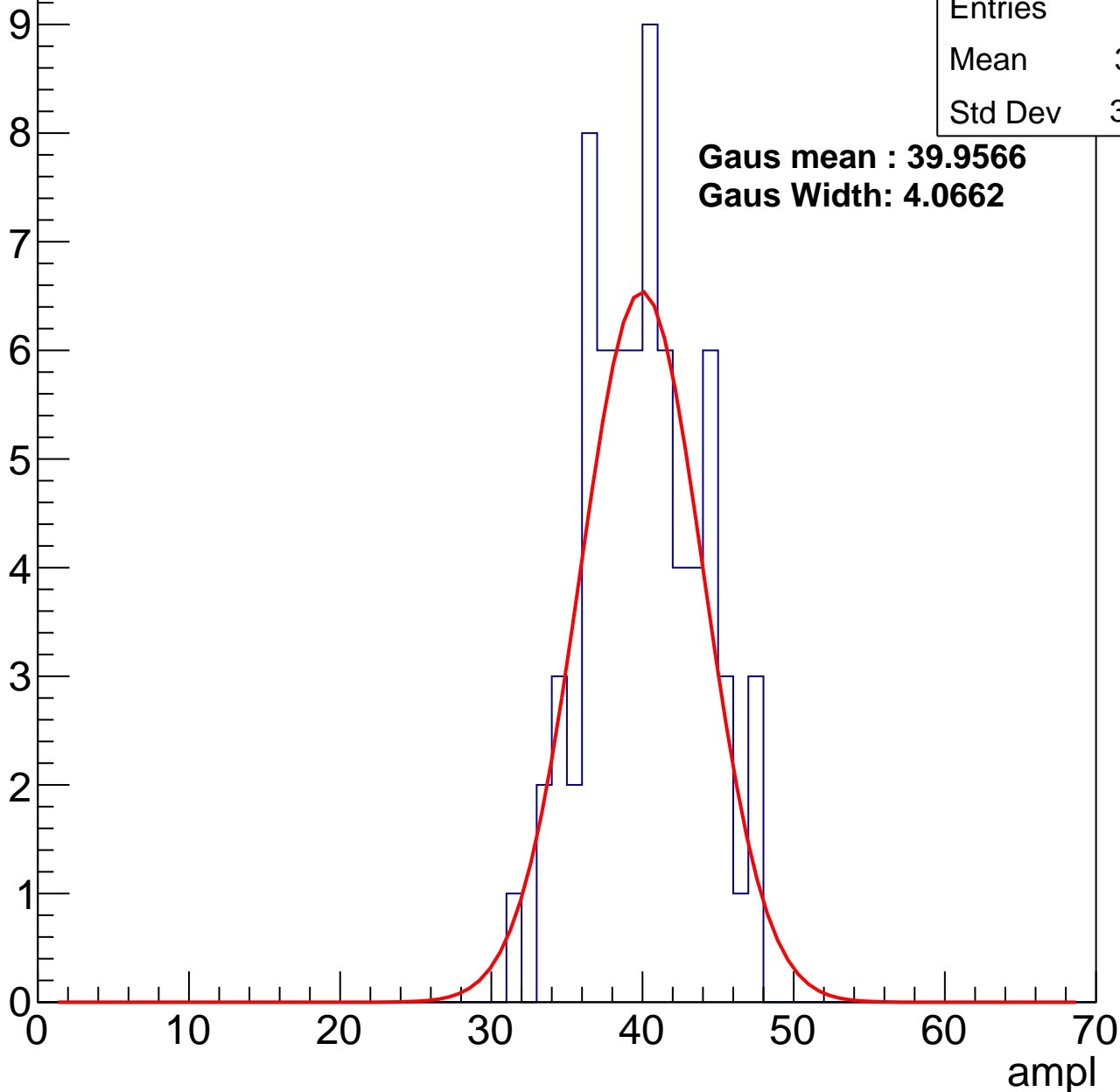
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	39.61
Std Dev	3.685

**Gaus mean : 39.9566**

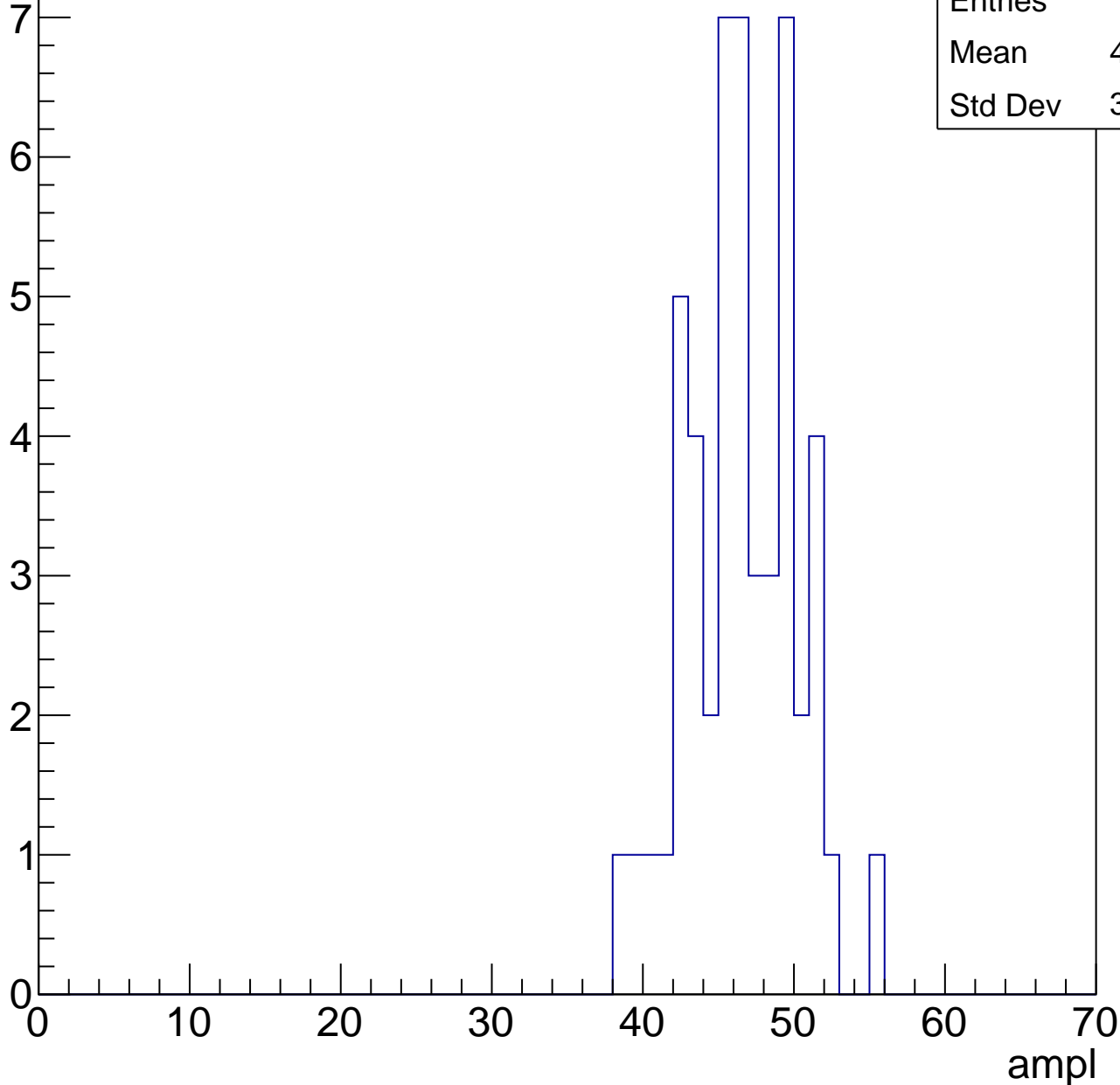
**Gaus Width: 4.0662**



# B1L103S, U3-ch90, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

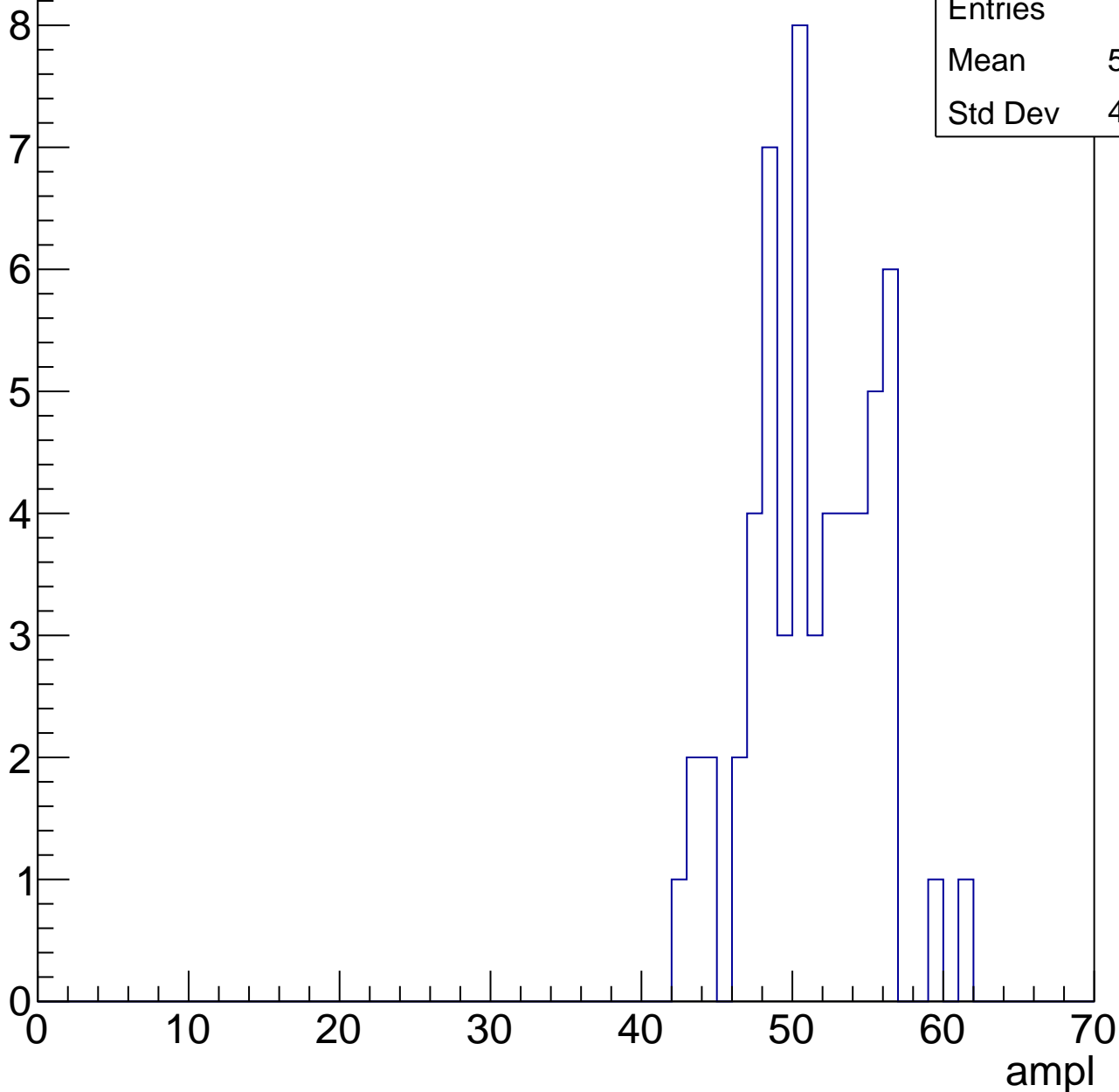


# B1L103S, U3-ch90, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

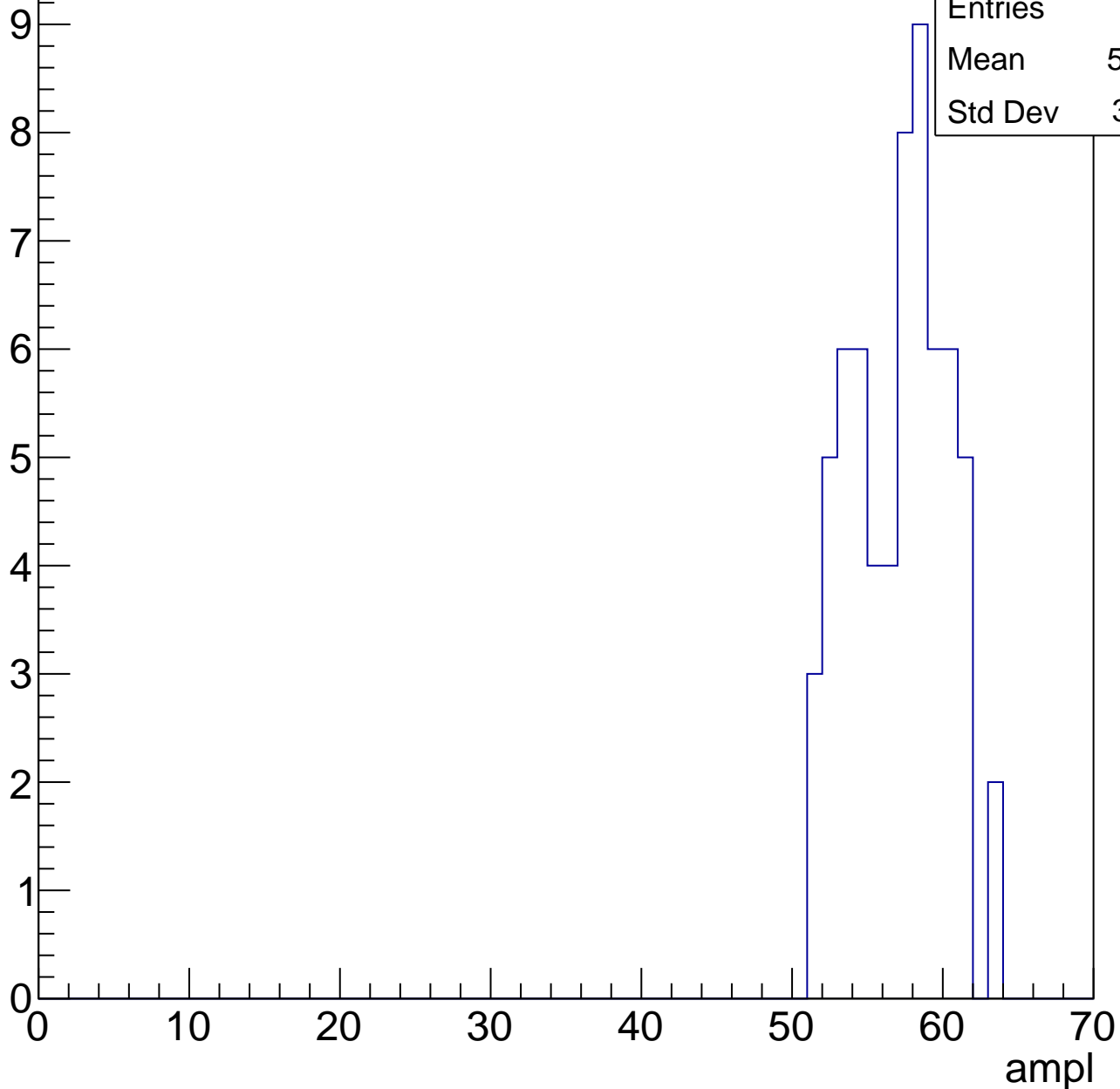
Entries	57
Mean	50.86
Std Dev	4.089



# B1L103S, U3-ch90, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

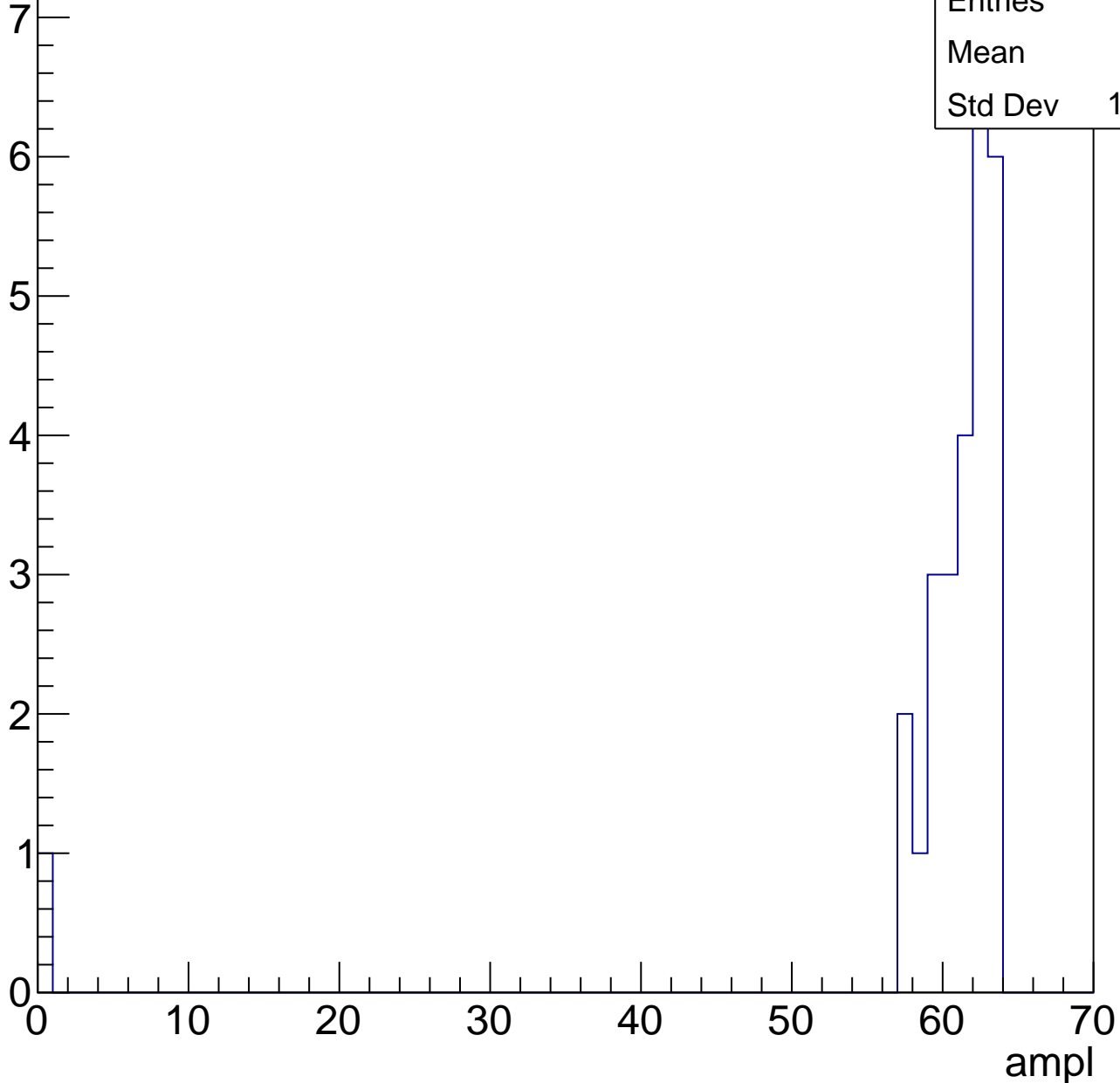


# B1L103S, U3-ch90, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	27
Mean	58.7
Std Dev	11.65





# B1L103S, U3-ch90, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

ampl

Entries

6

Mean

62

Std Dev

1

Entries	6
Mean	62
Std Dev	1

# B1L103S, U3-ch91, adc0

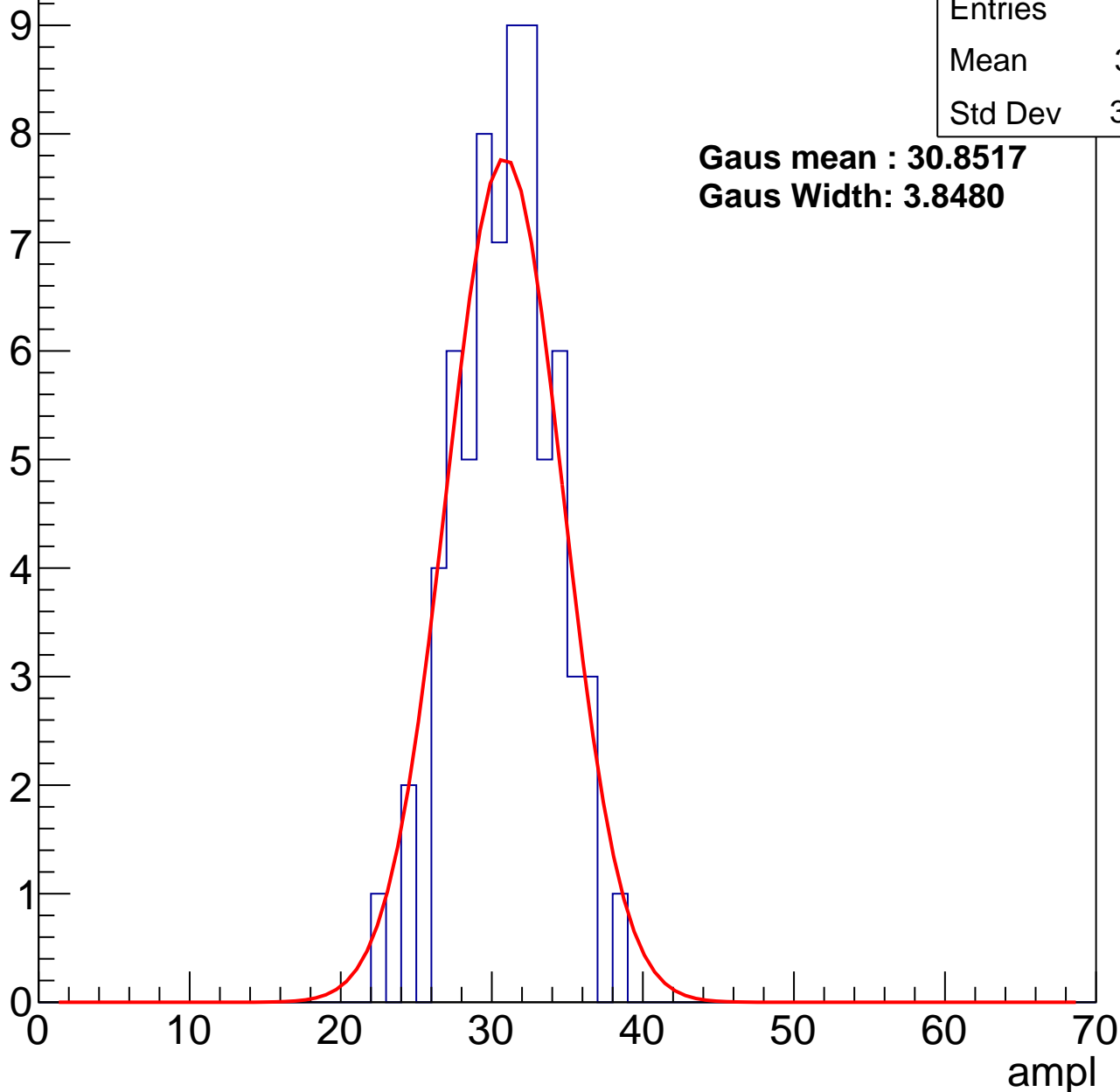
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	30.51
Std Dev	3.179

**Gaus mean : 30.8517**

**Gaus Width: 3.8480**



# B1L103S, U3-ch91, adc1

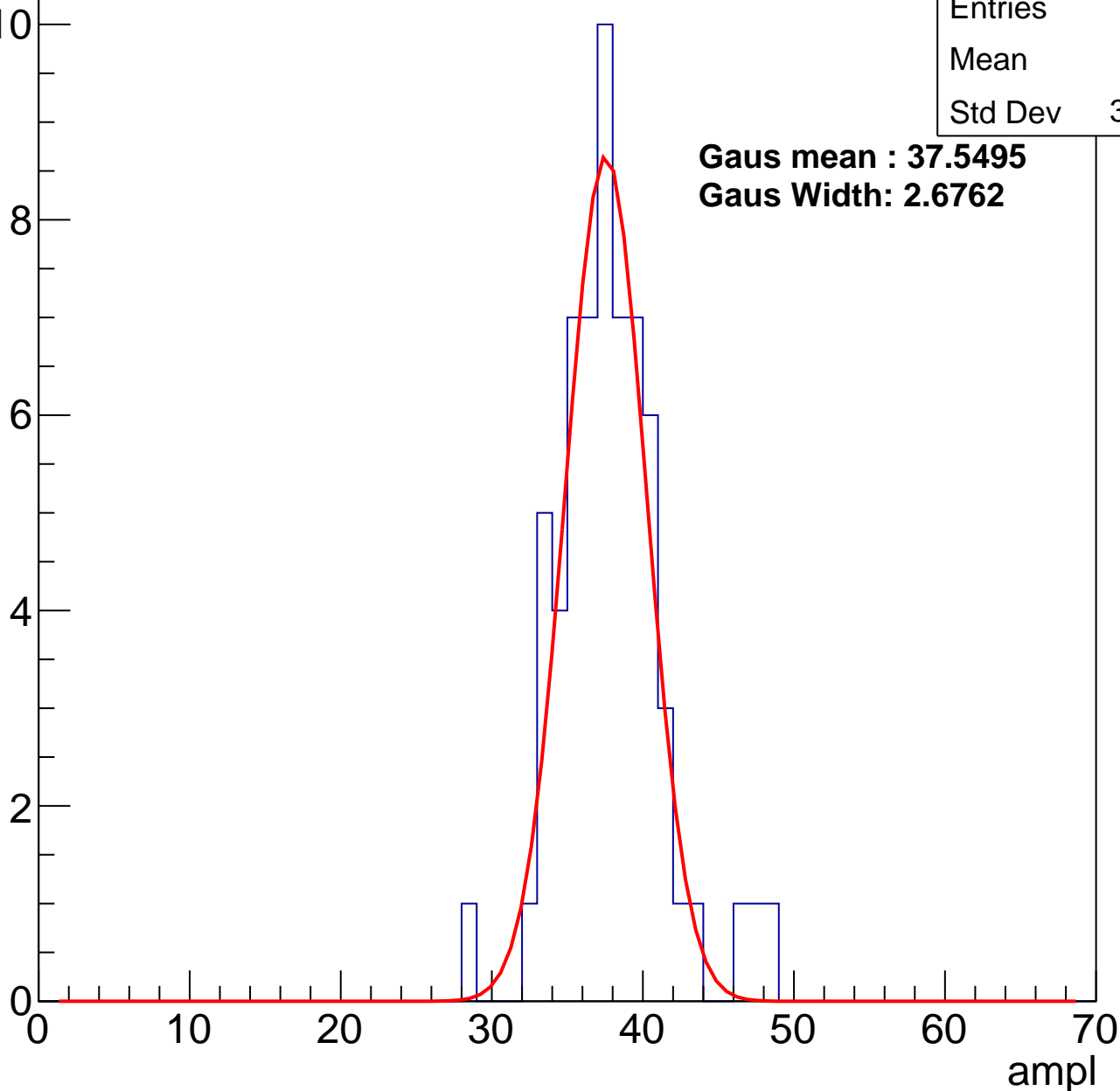
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	37.4
Std Dev	3.444

**Gaus mean : 37.5495**

**Gaus Width: 2.6762**



# B1L103S, U3-ch91, adc2

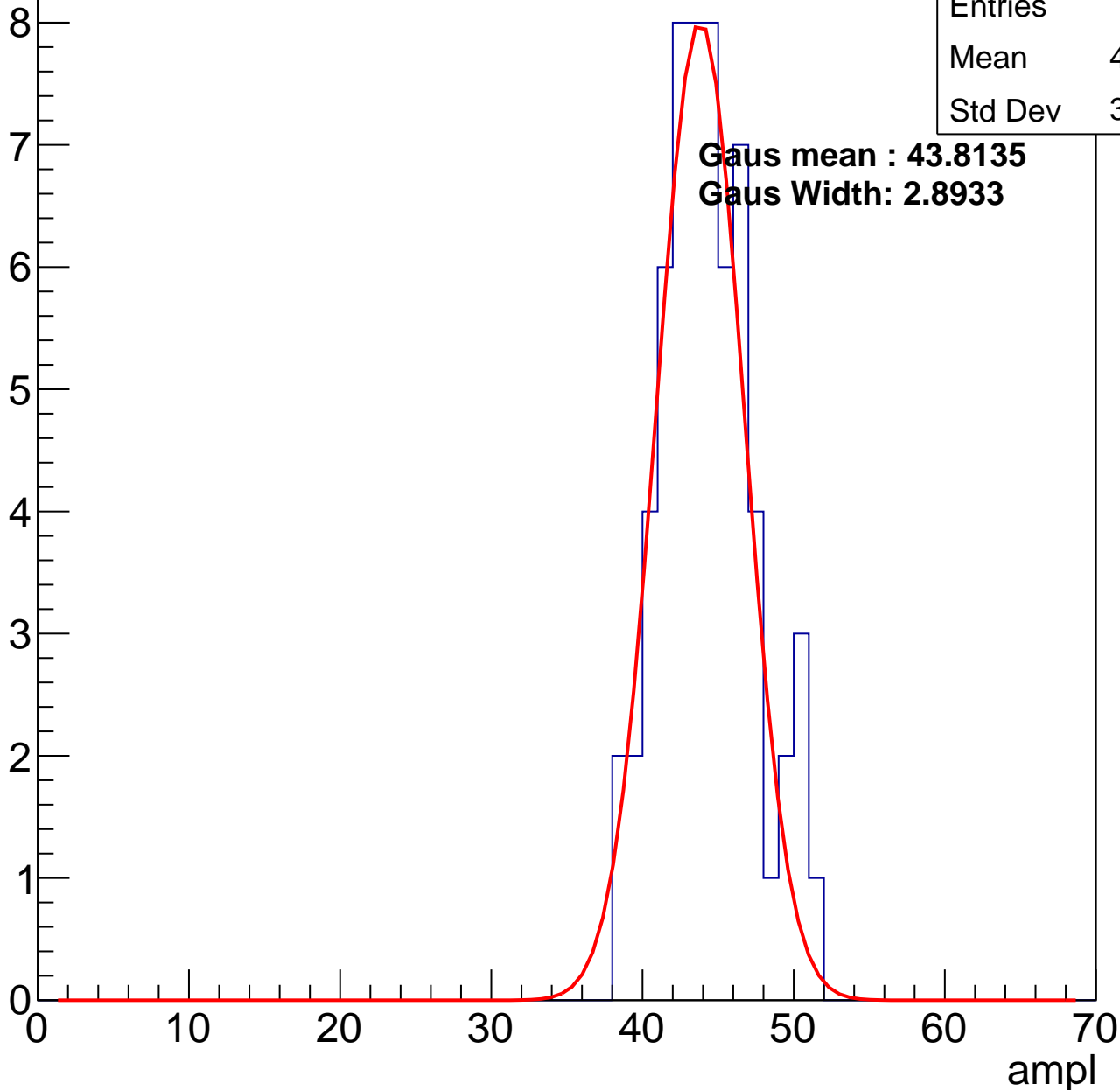
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	43.85
Std Dev	3.037

**Gaus mean : 43.8135**

**Gaus Width: 2.8933**

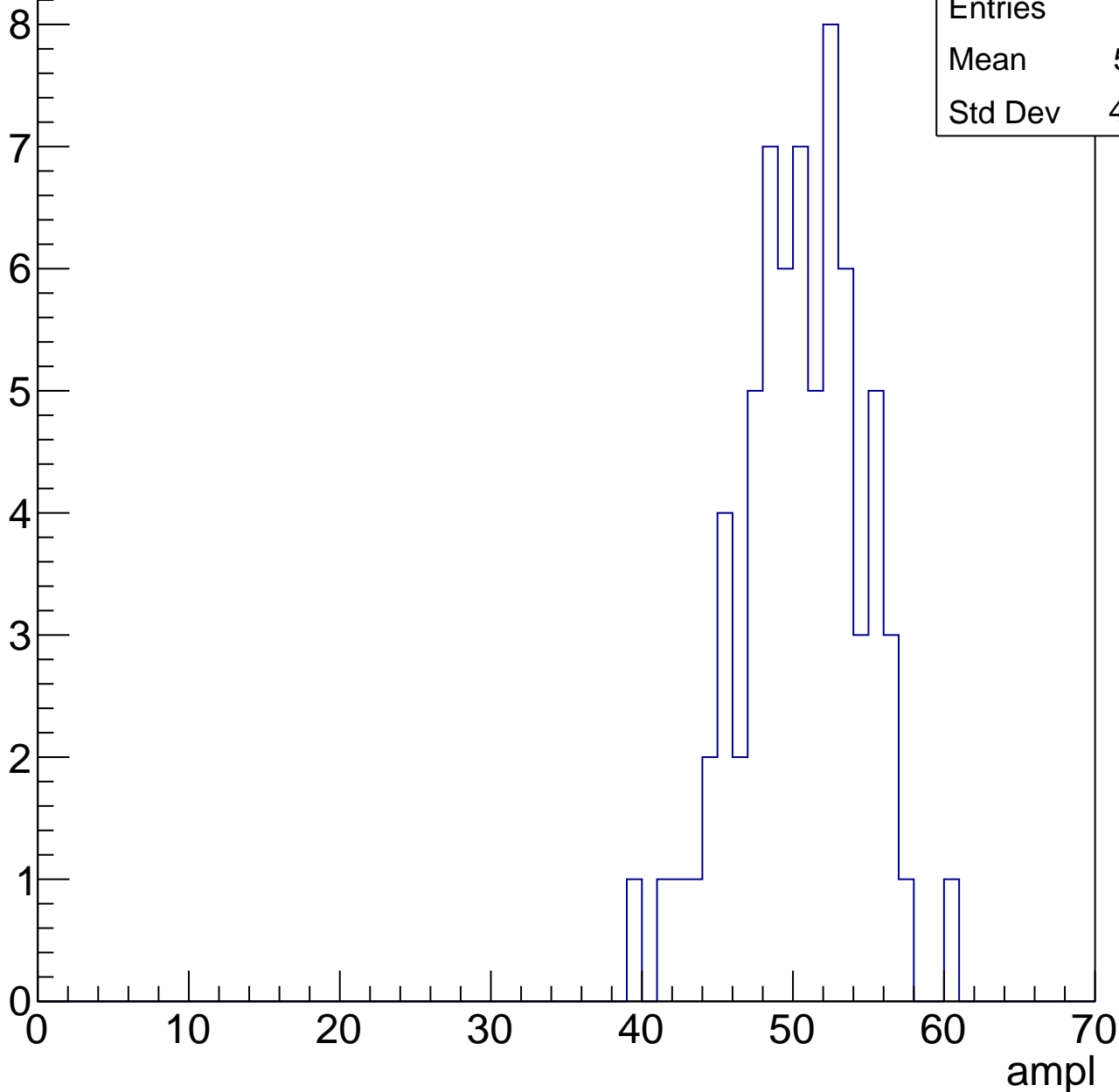


# B1L103S, U3-ch91, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	50.01
Std Dev	4.027

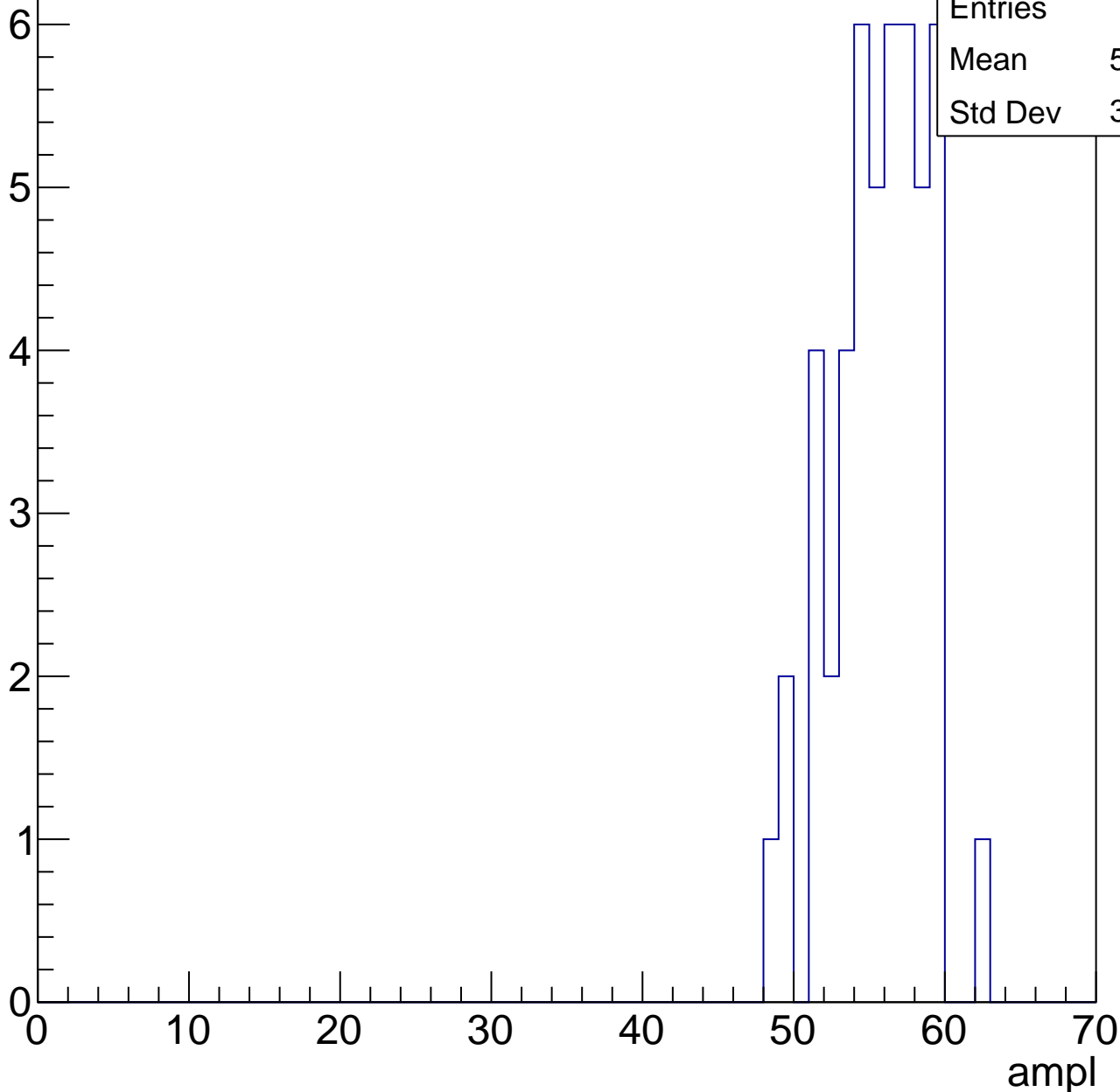


# B1L103S, U3-ch91, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	48
Mean	55.19
Std Dev	3.039



# B1L103S, U3-ch91, adc5

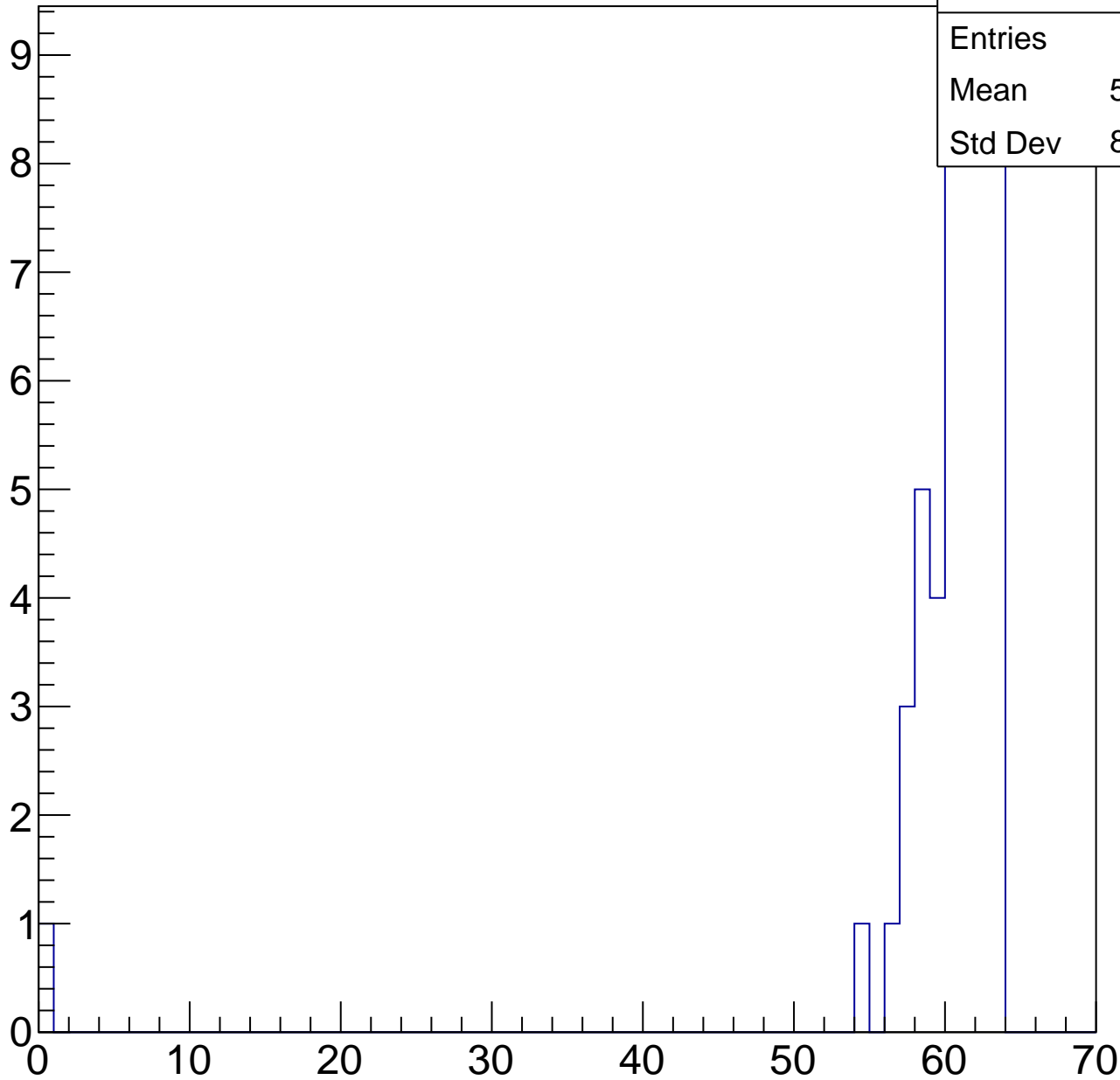
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	48
Mean	59.06
Std Dev	8.866

ampl



# B1L103S, U3-ch91, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

0 10 20 30 40 50 60 70

ampl

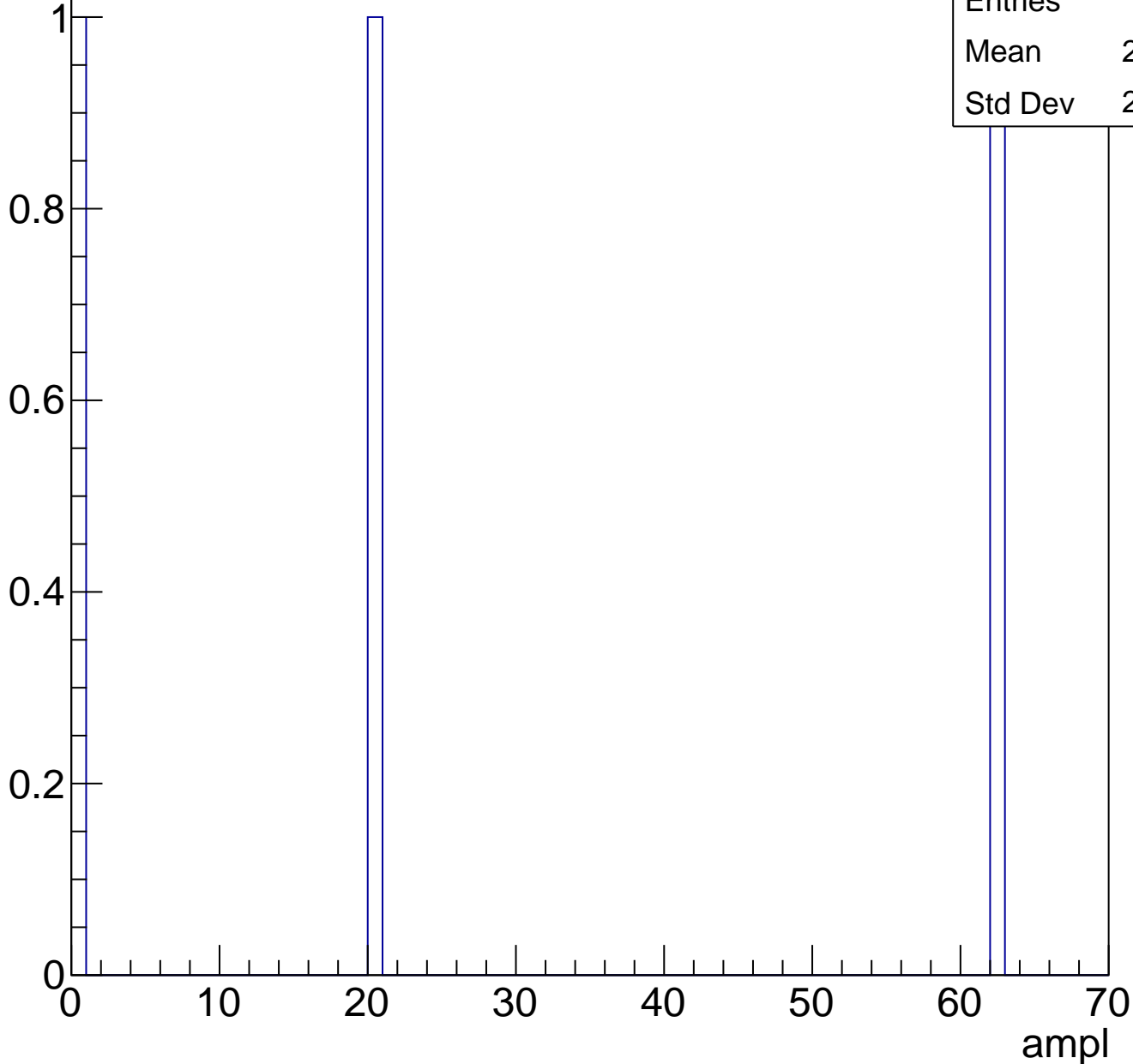
Entries	4
Mean	62
Std Dev	1



# B1L103S, U3-ch91, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	3
Mean	27.33
Std Dev	25.84

# B1L103S, U3-ch92, adc0

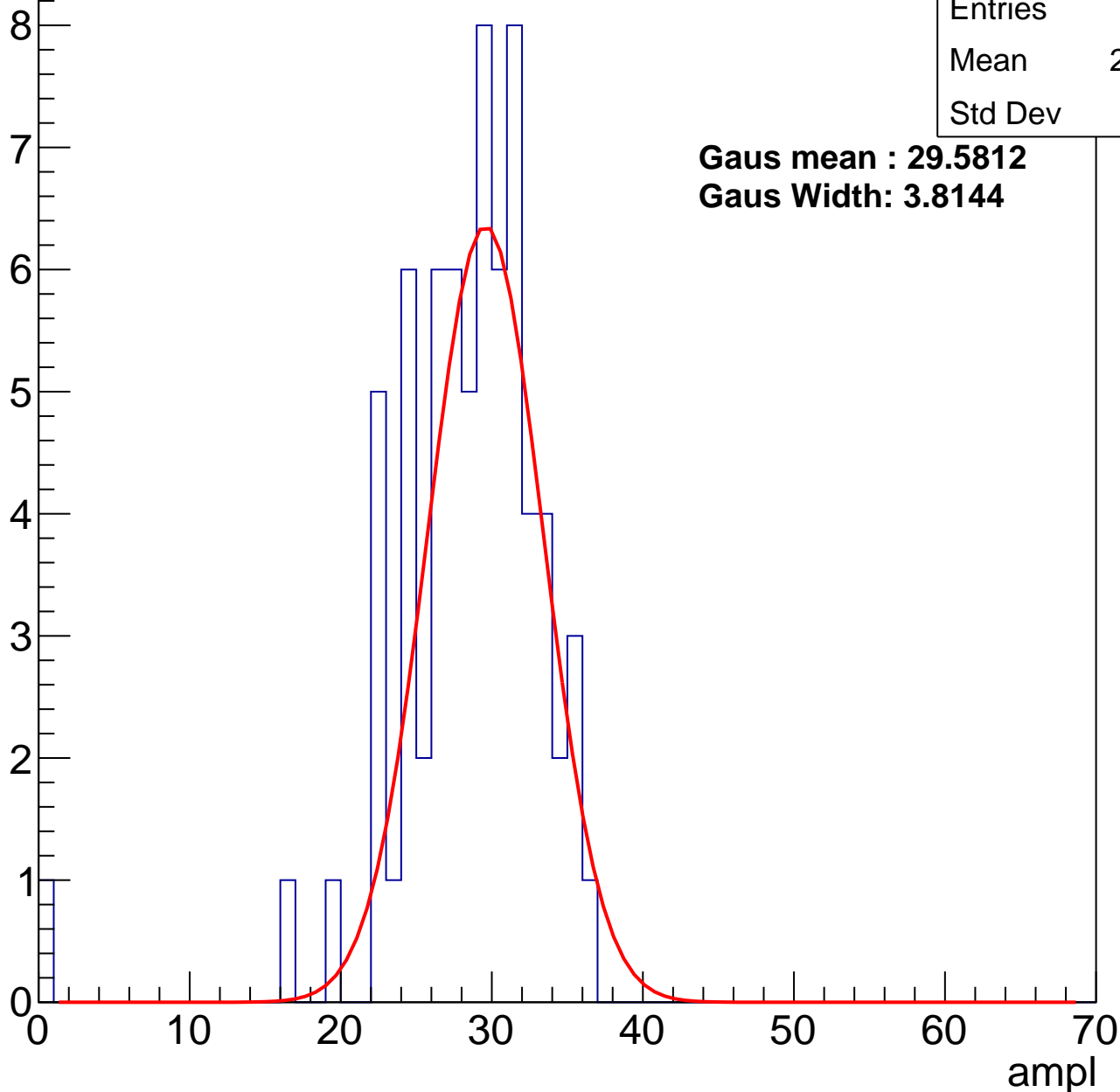
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	27.84
Std Dev	5.22

**Gaus mean : 29.5812**

**Gaus Width: 3.8144**



# B1L103S, U3-ch92, adc1

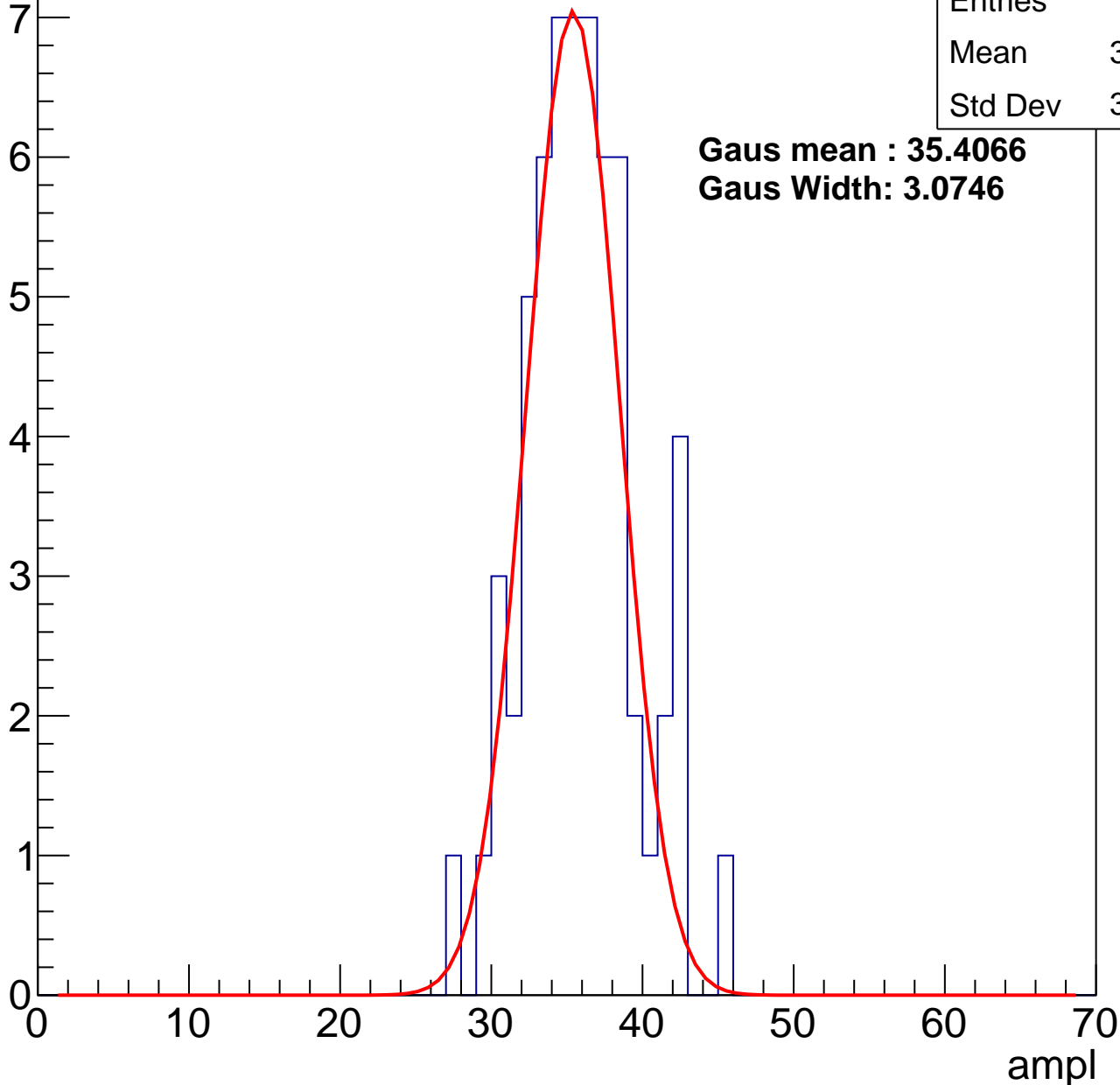
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	35.48
Std Dev	3.574

**Gaus mean : 35.4066**

**Gaus Width: 3.0746**



# B1L103S, U3-ch92, adc2

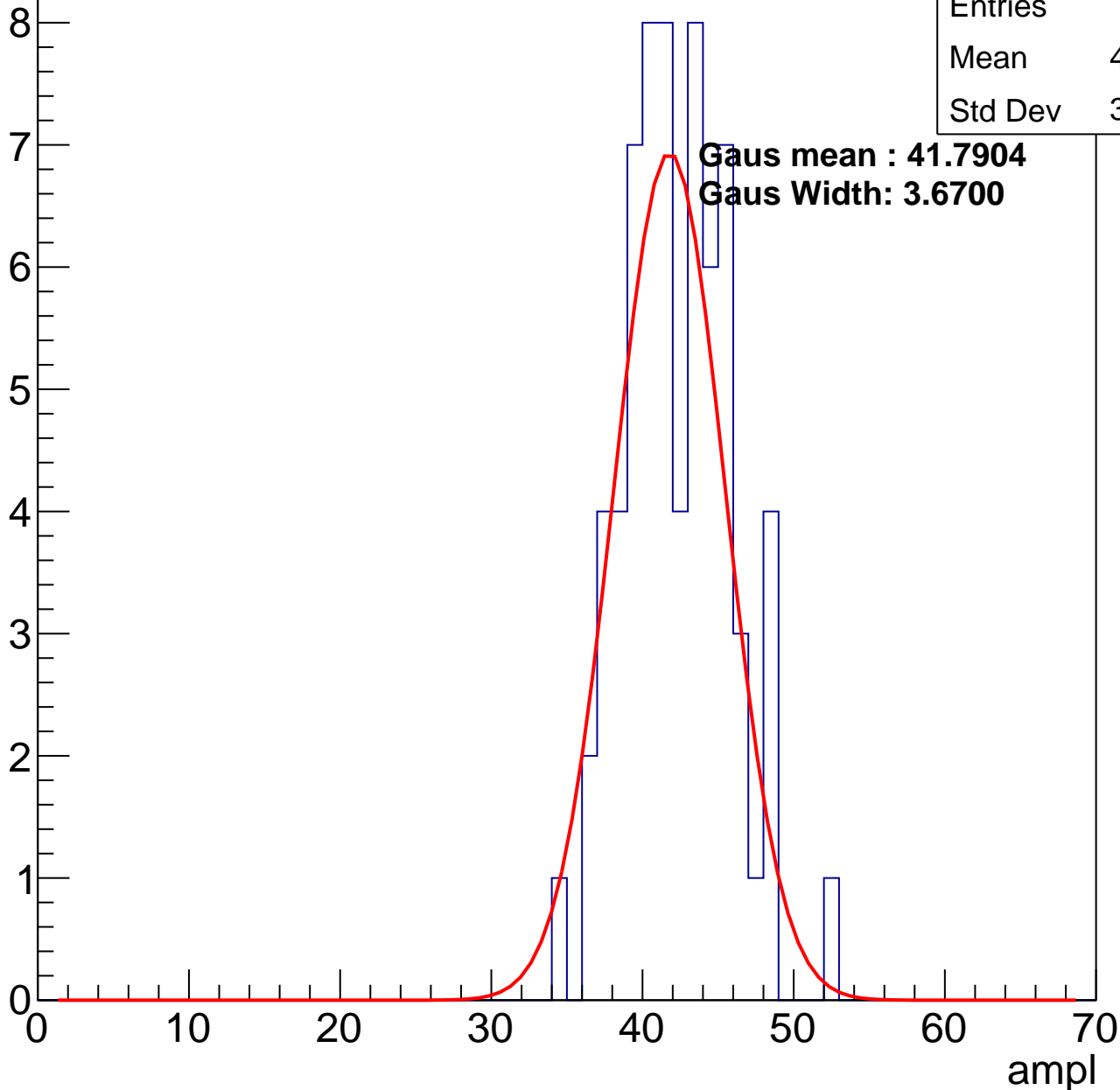
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	41.87
Std Dev	3.459

**Gaus mean : 41.7904**

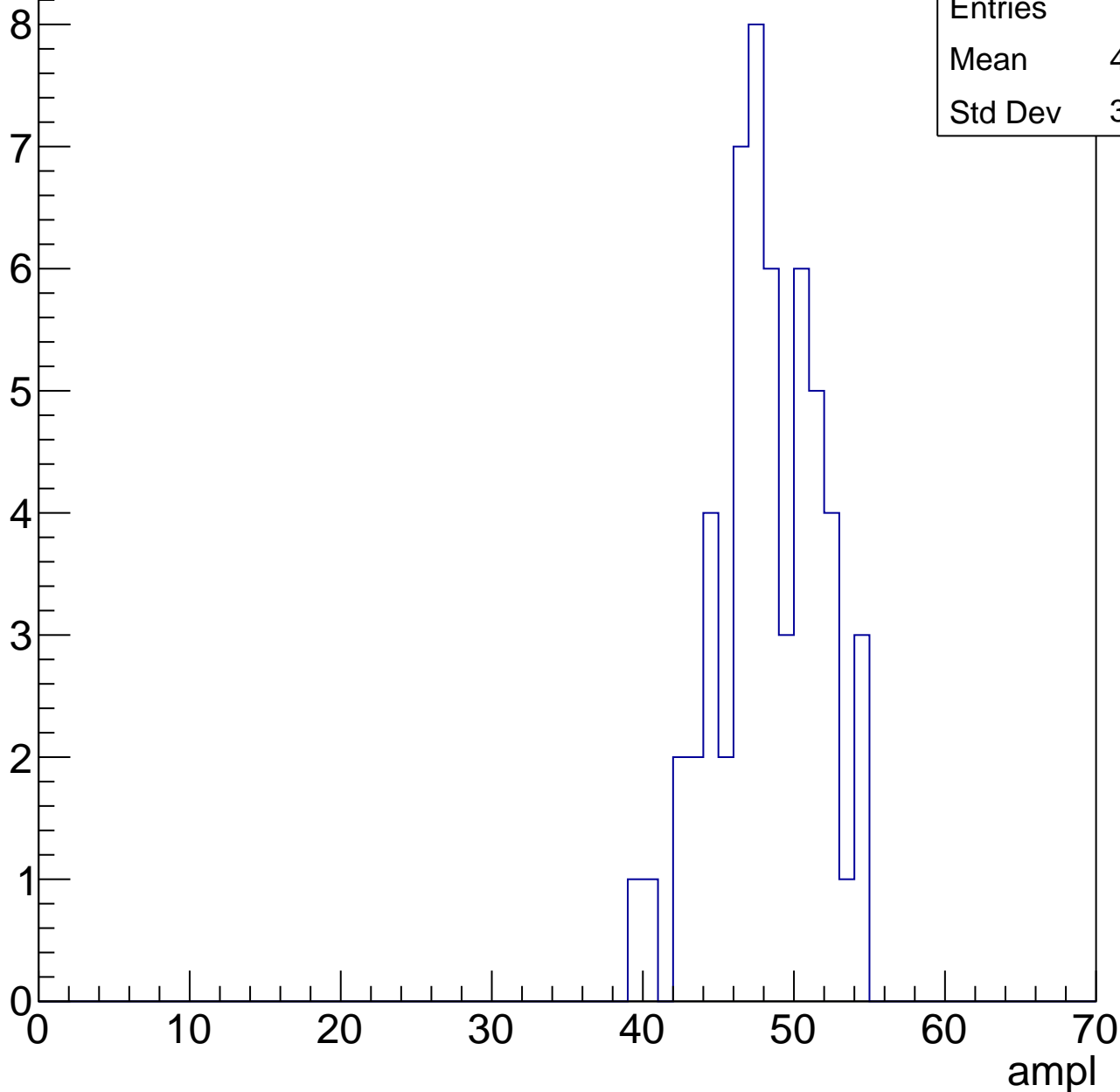
**Gaus Width: 3.6700**



# B1L103S, U3-ch92, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

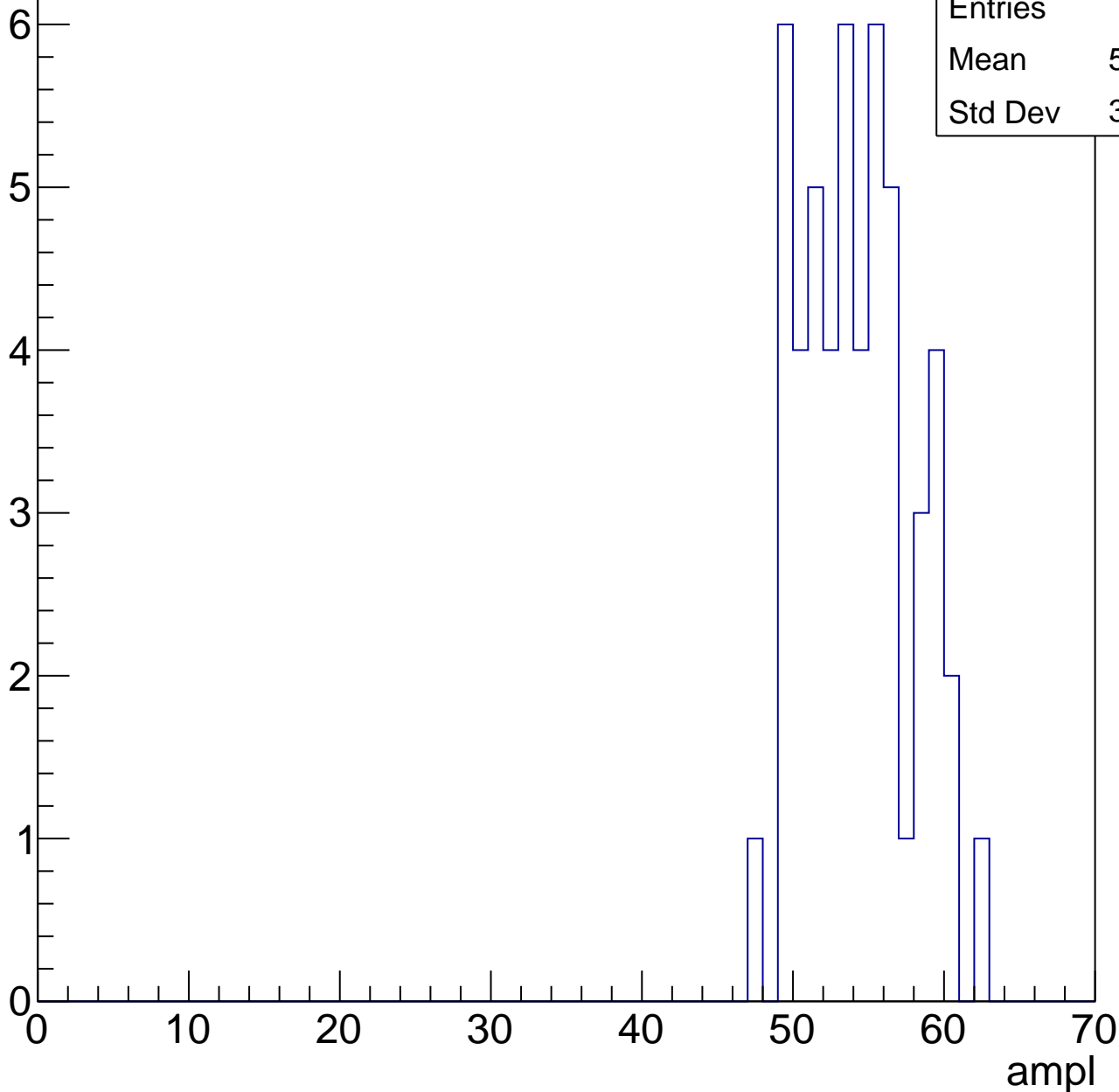


# B1L103S, U3-ch92, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

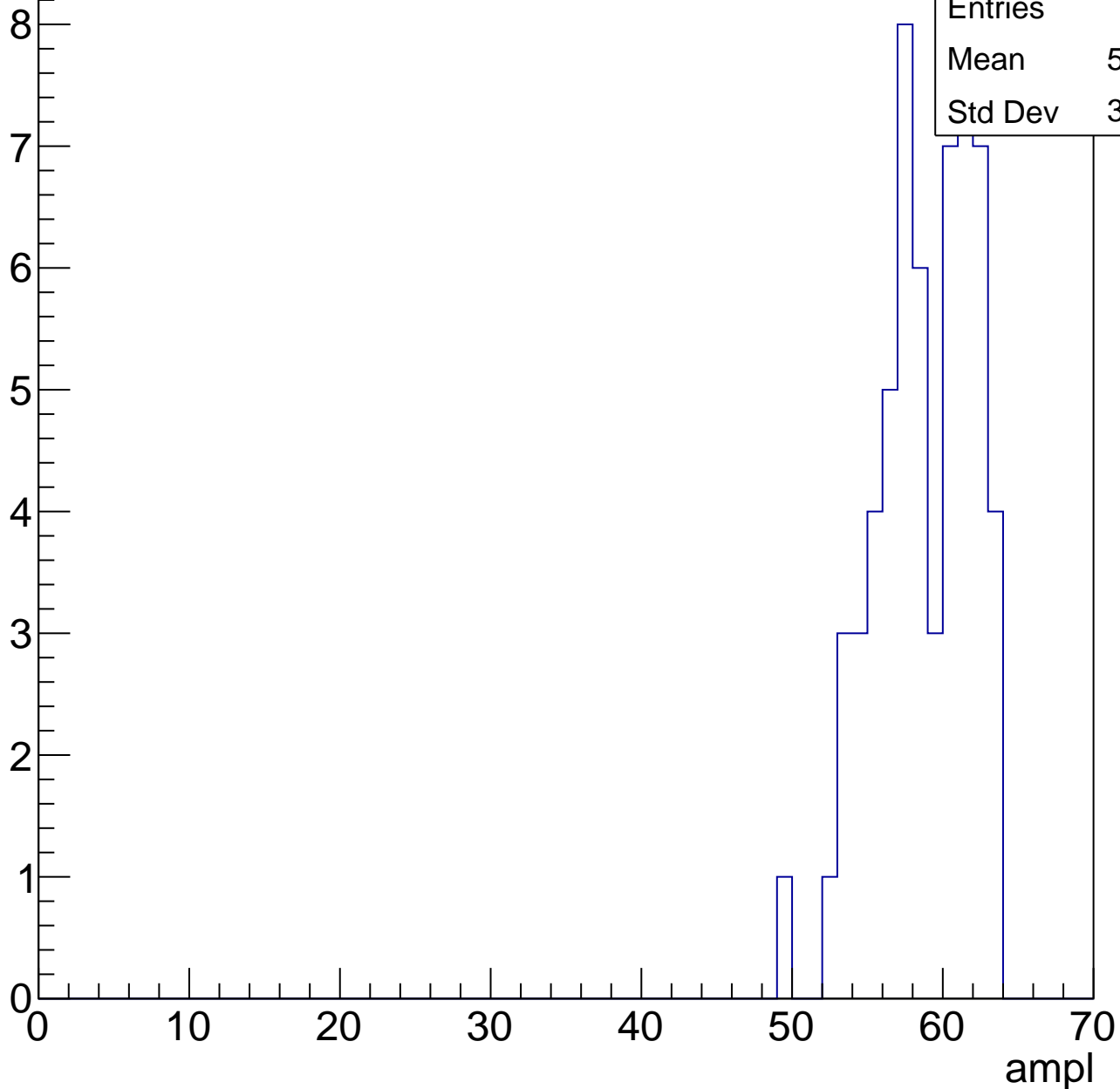
Entries	52
Mean	53.79
Std Dev	3.526



# B1L103S, U3-ch92, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



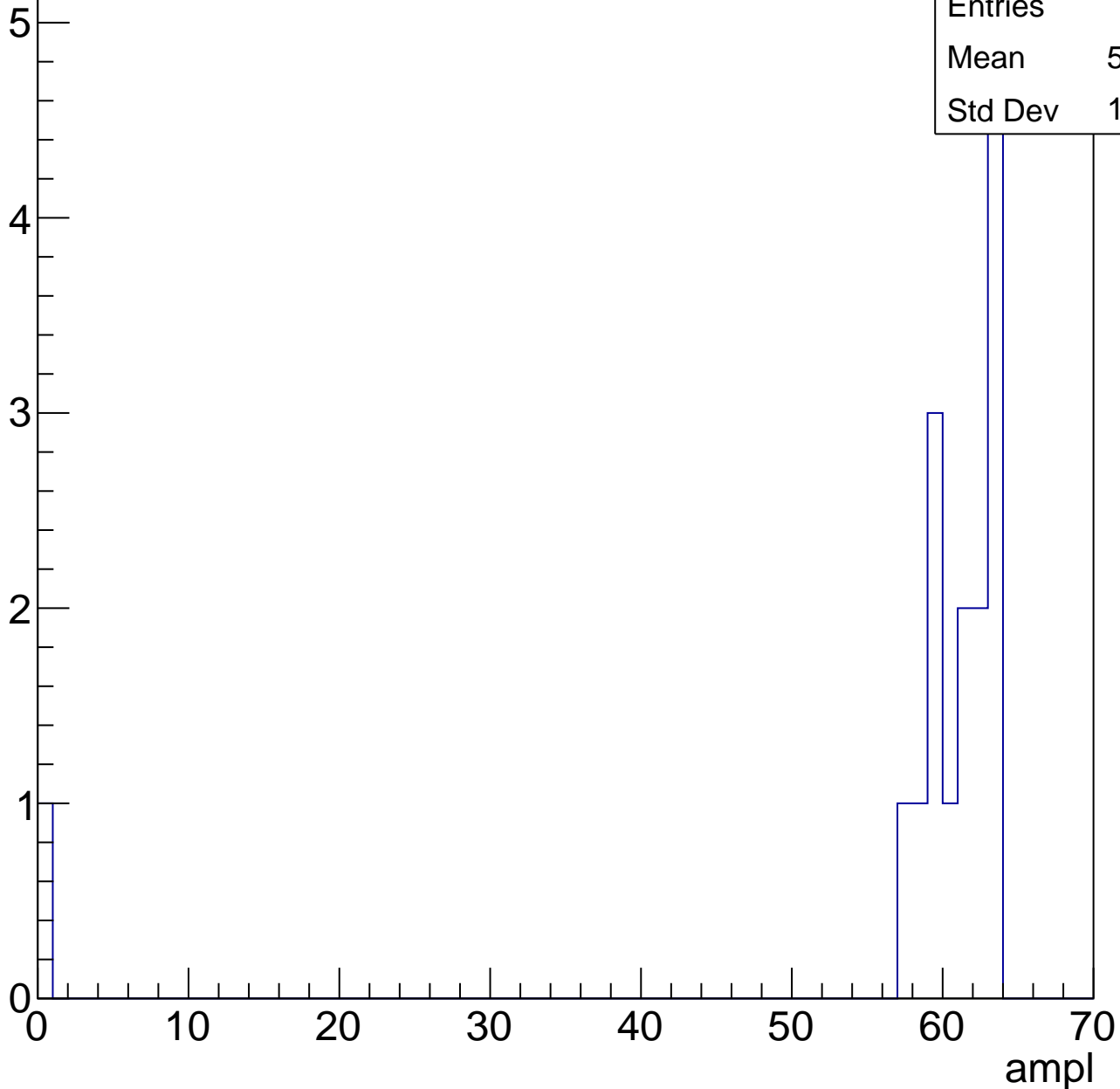
Entries	60
Mean	58.28
Std Dev	3.199

# B1L103S, U3-ch92, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	16
Mean	57.06
Std Dev	14.86





# B1L103S, U3-ch92, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch93, adc0

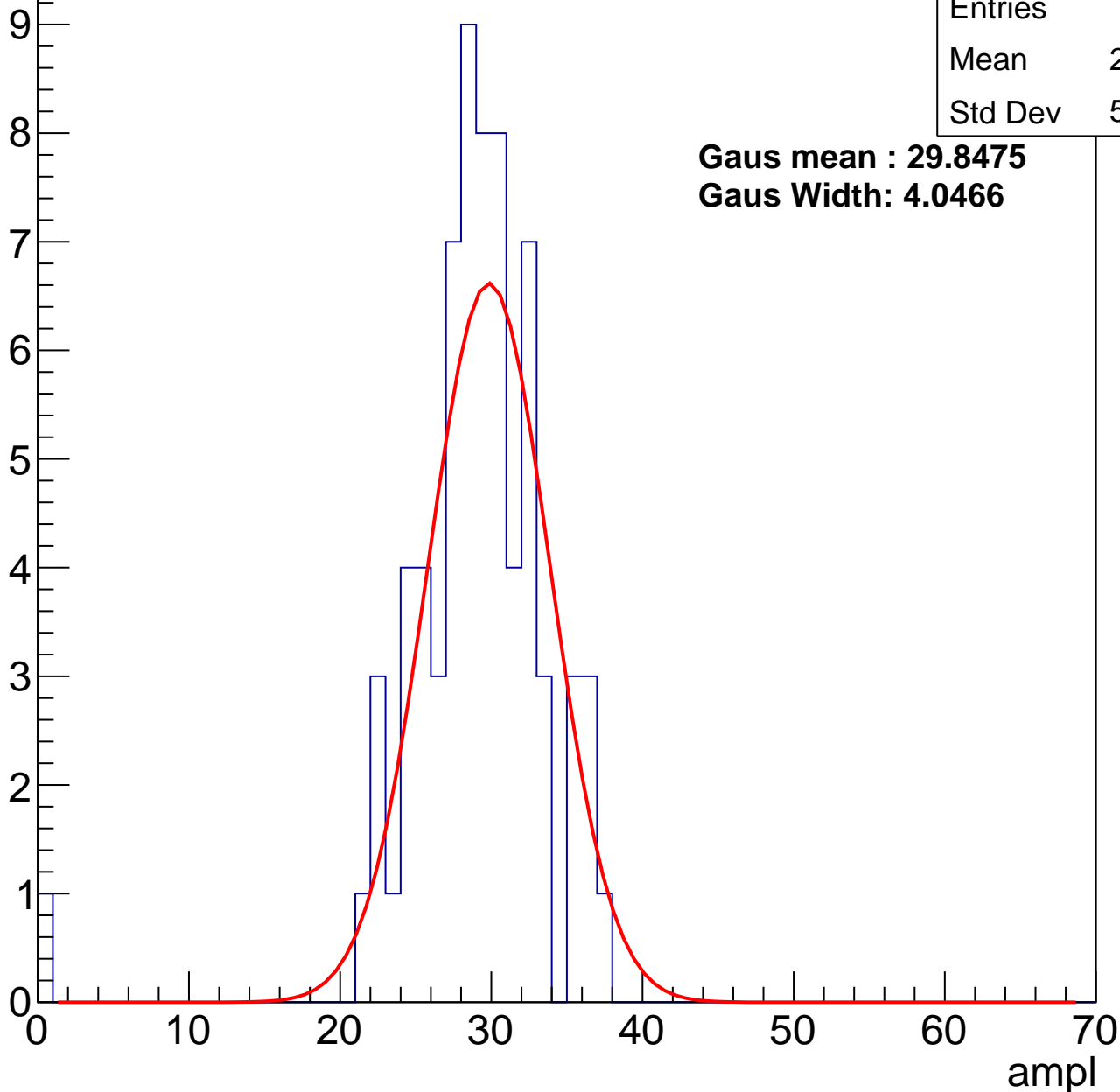
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	28.49
Std Dev	5.002

**Gaus mean : 29.8475**

**Gaus Width: 4.0466**



# B1L103S, U3-ch93, adc1

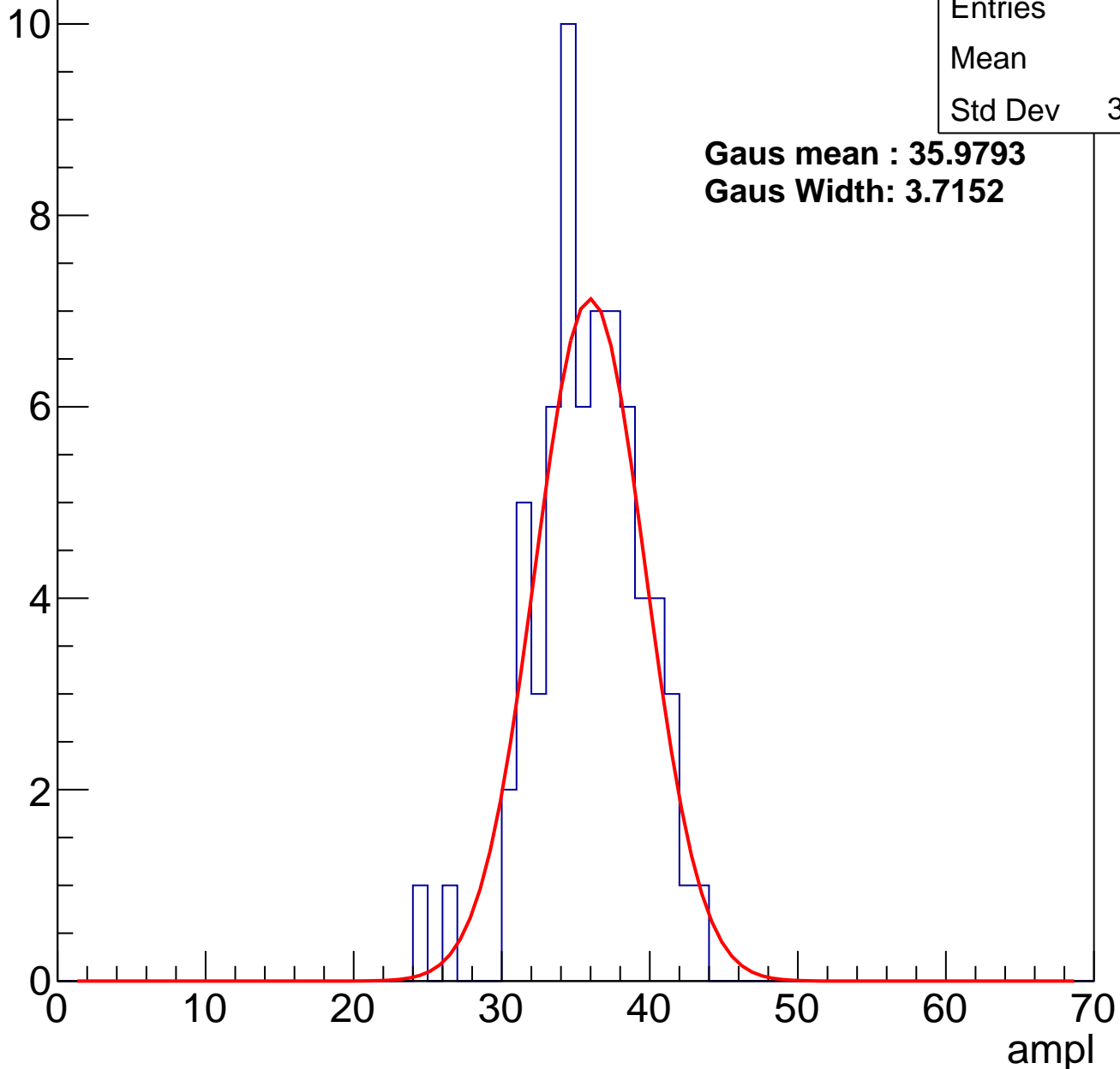
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	67
Mean	35.4
Std Dev	3.575

**Gaus mean : 35.9793**

**Gaus Width: 3.7152**

Entry



# B1L103S, U3-ch93, adc2

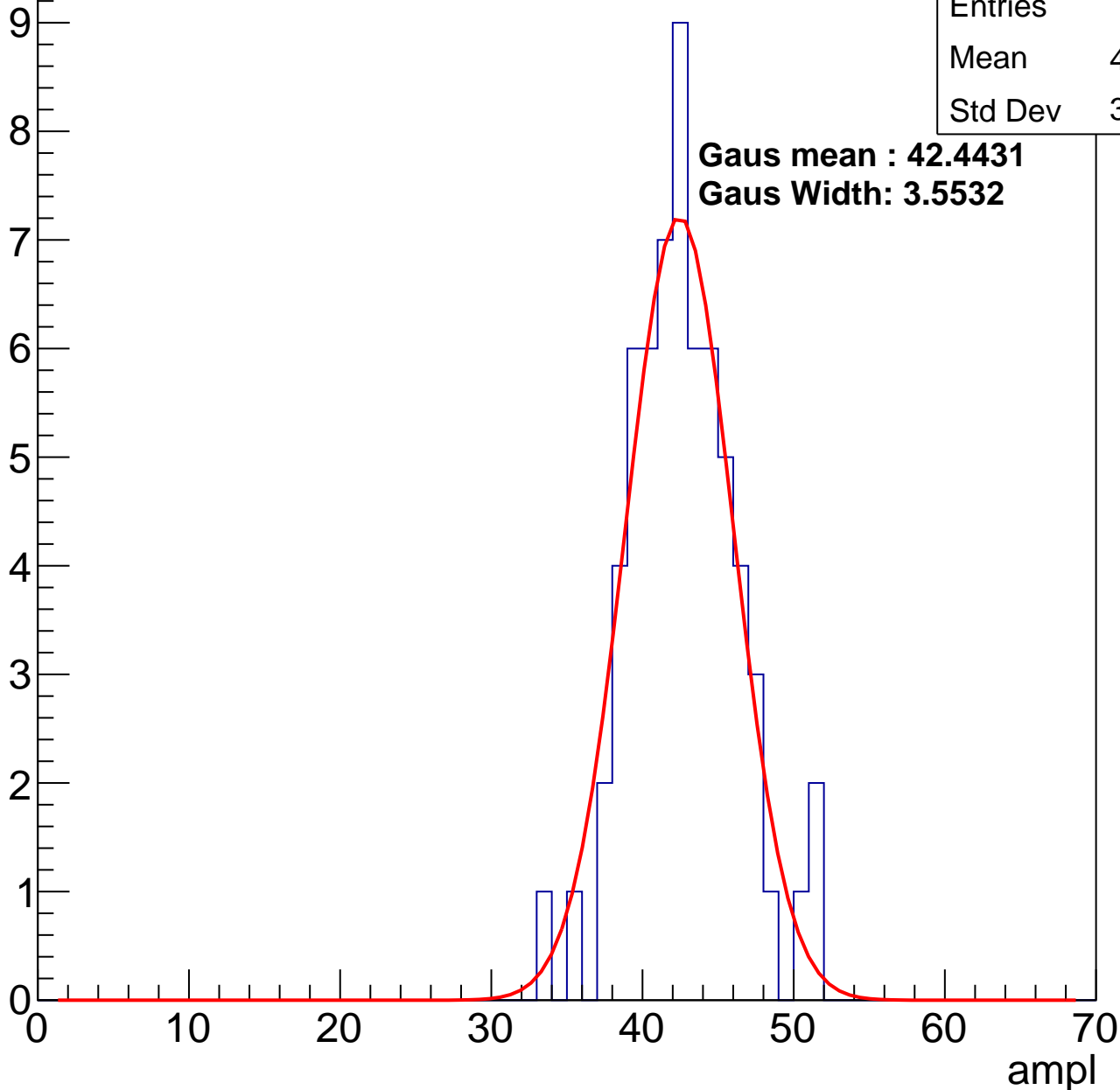
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	42.27
Std Dev	3.537

**Gaus mean : 42.4431**

**Gaus Width: 3.5532**

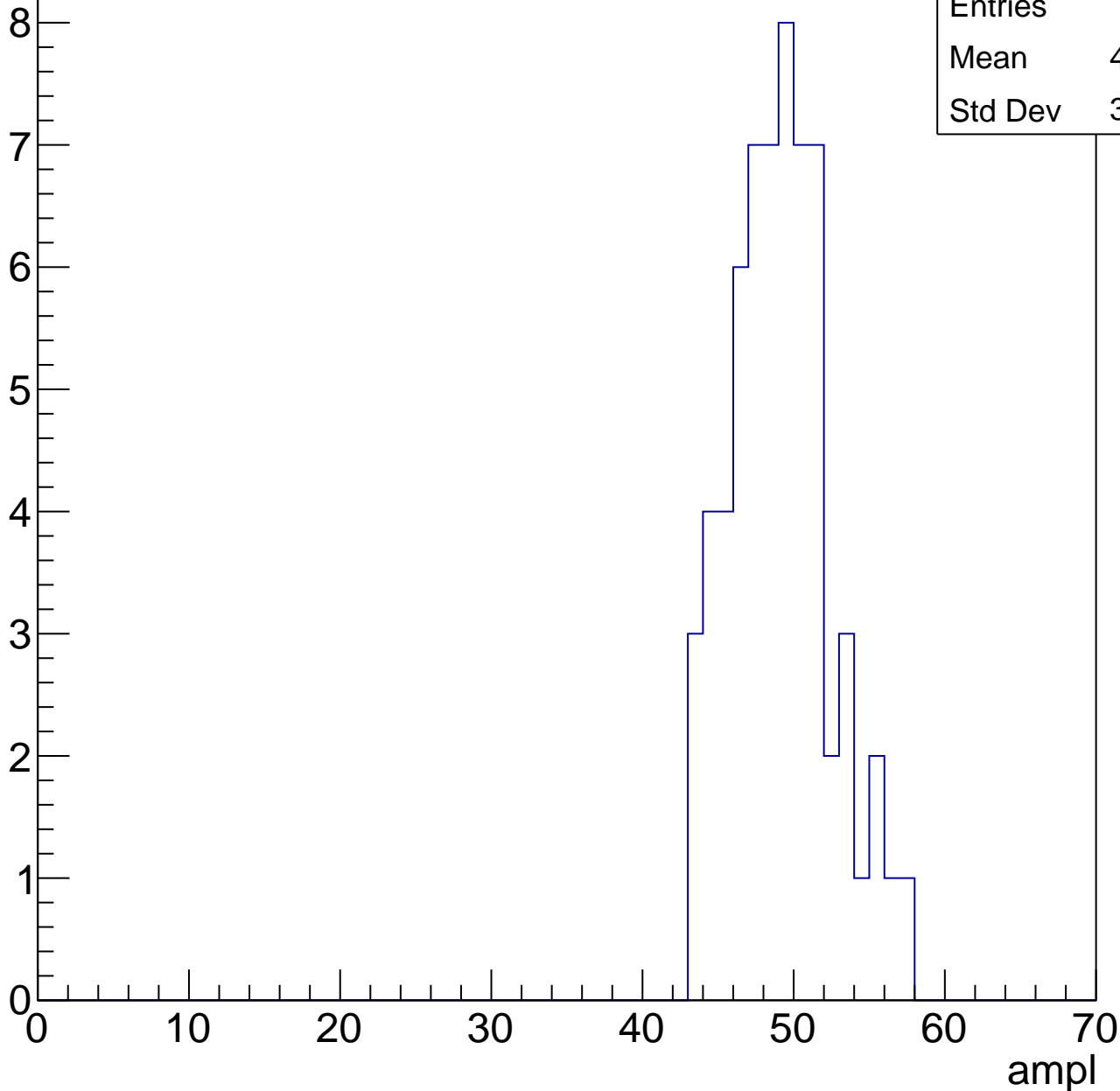


# B1L103S, U3-ch93, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

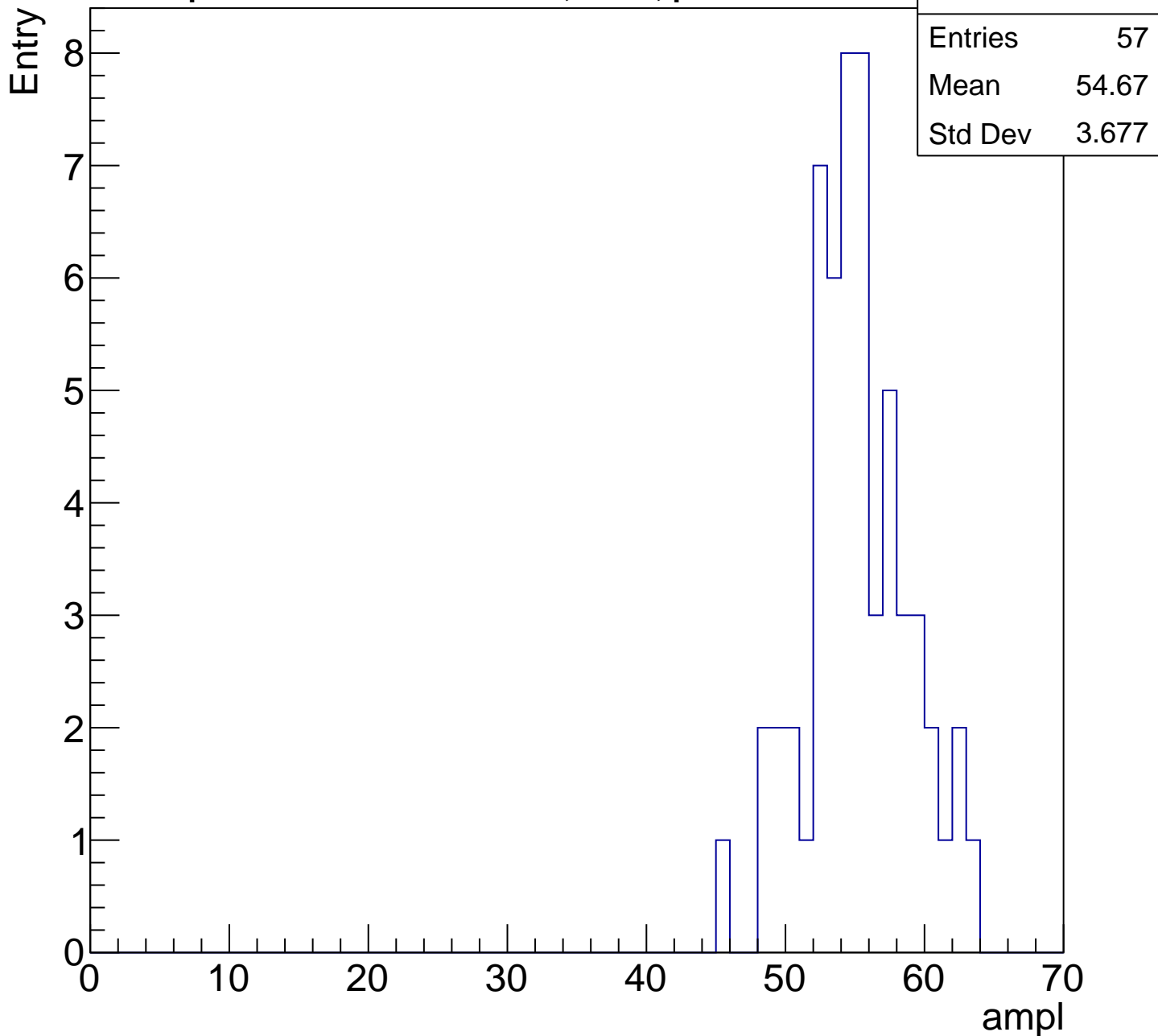
Entry

Entries	63
Mean	48.65
Std Dev	3.247



# B1L103S, U3-ch93, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

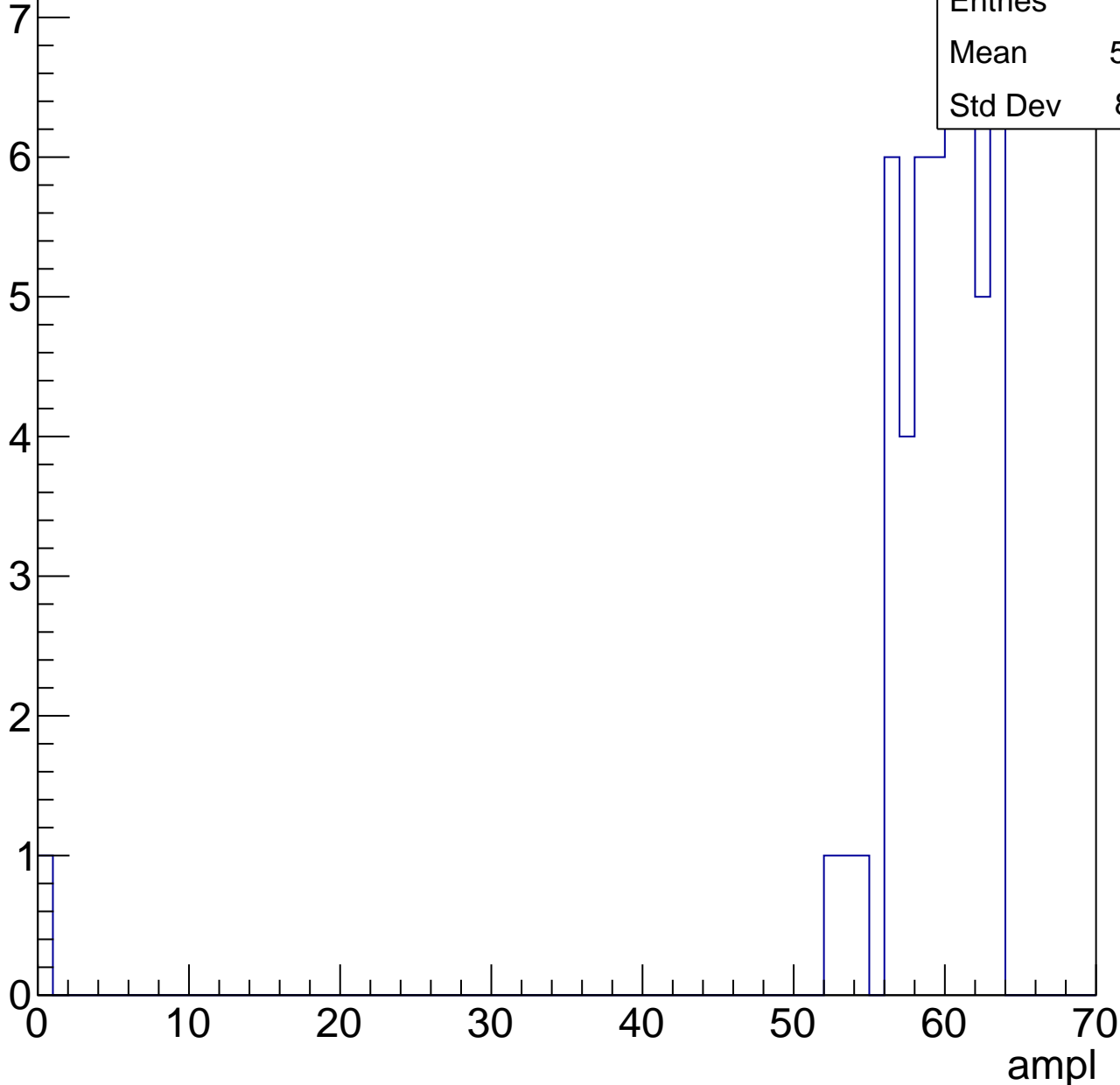


# B1L103S, U3-ch93, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

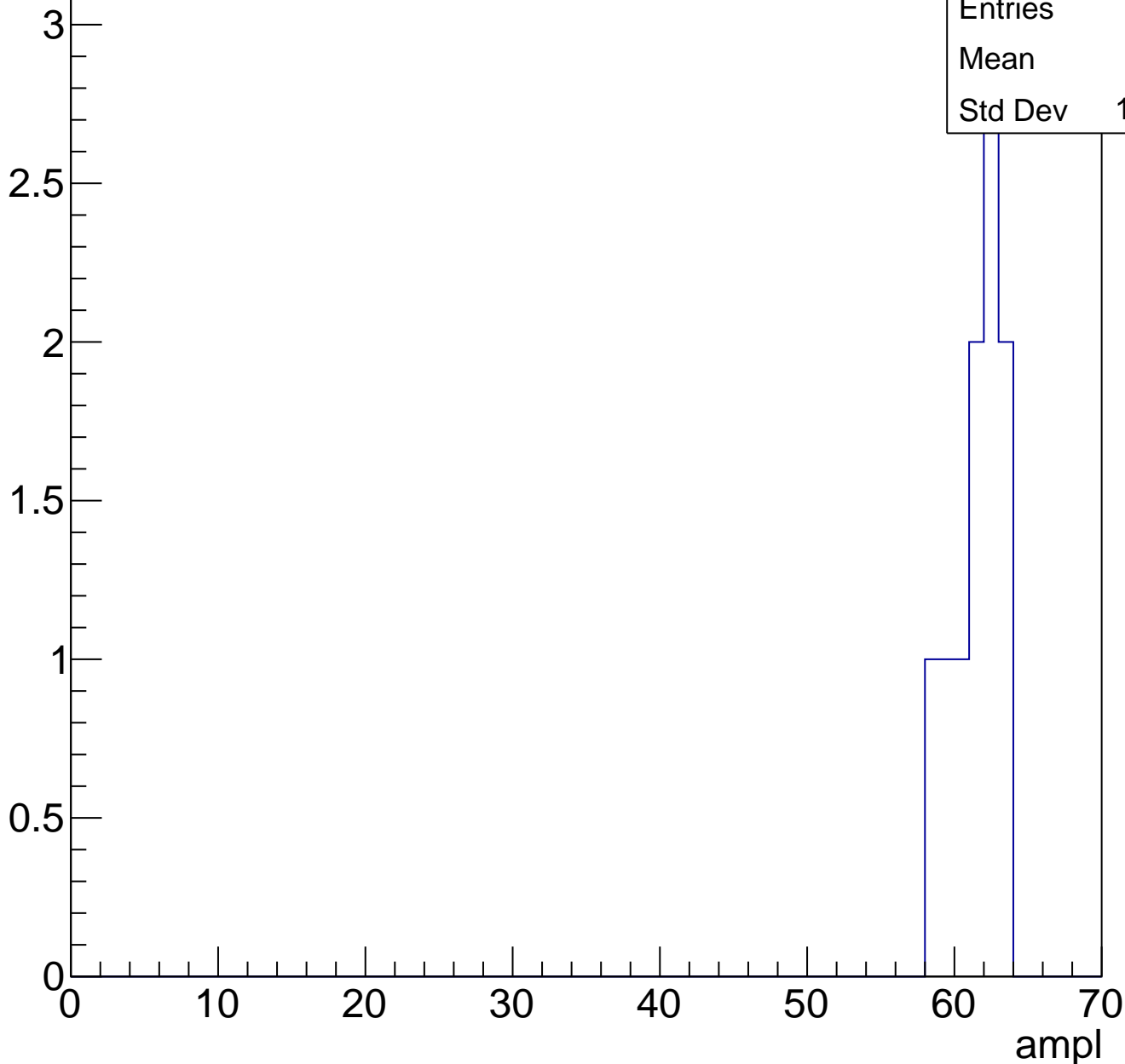
Entries	52
Mean	58.13
Std Dev	8.571



# B1L103S, U3-ch93, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U3-ch93, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U3-ch94, adc0

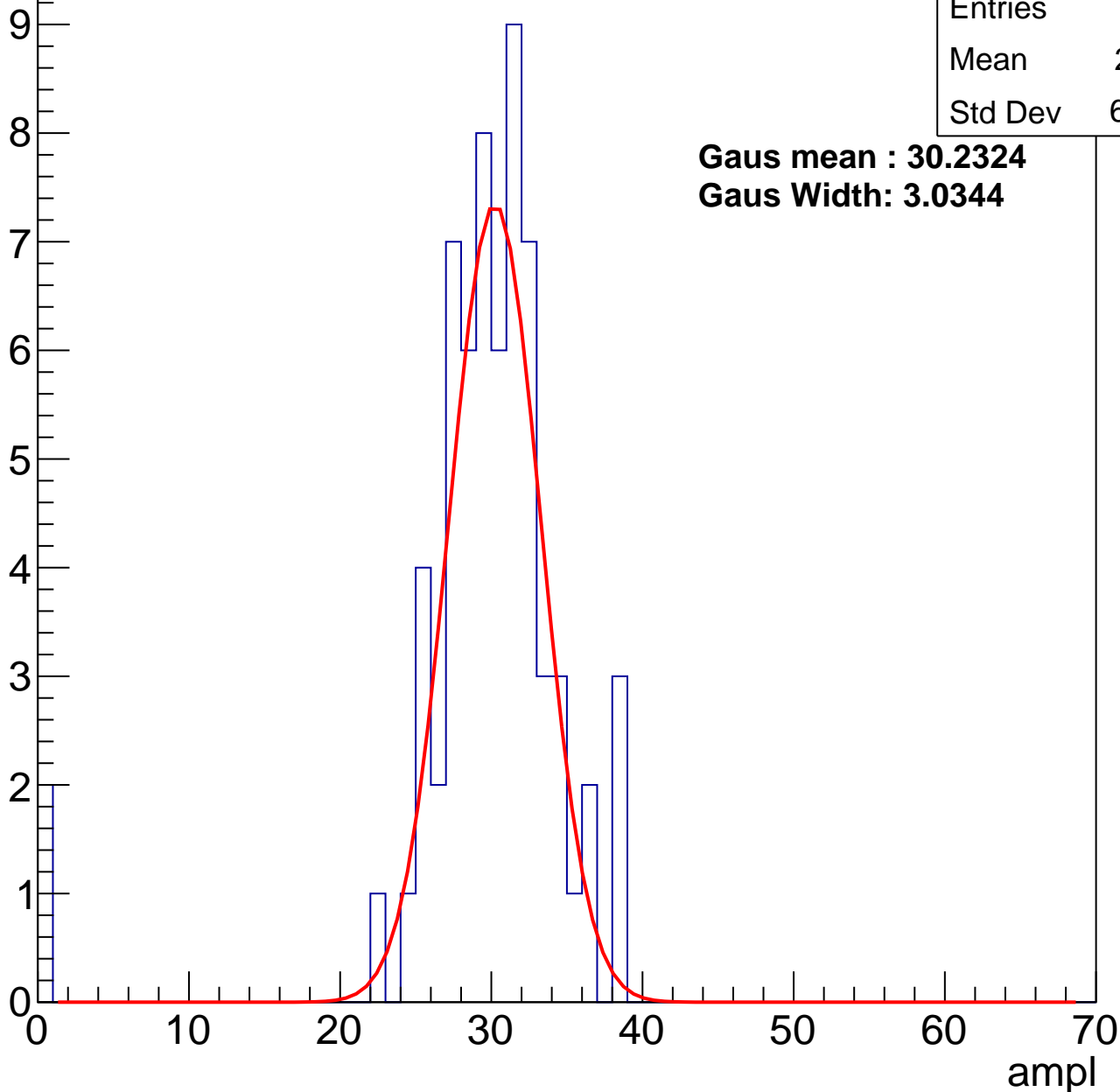
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	29.11
Std Dev	6.172

**Gaus mean : 30.2324**

**Gaus Width: 3.0344**



# B1L103S, U3-ch94, adc1

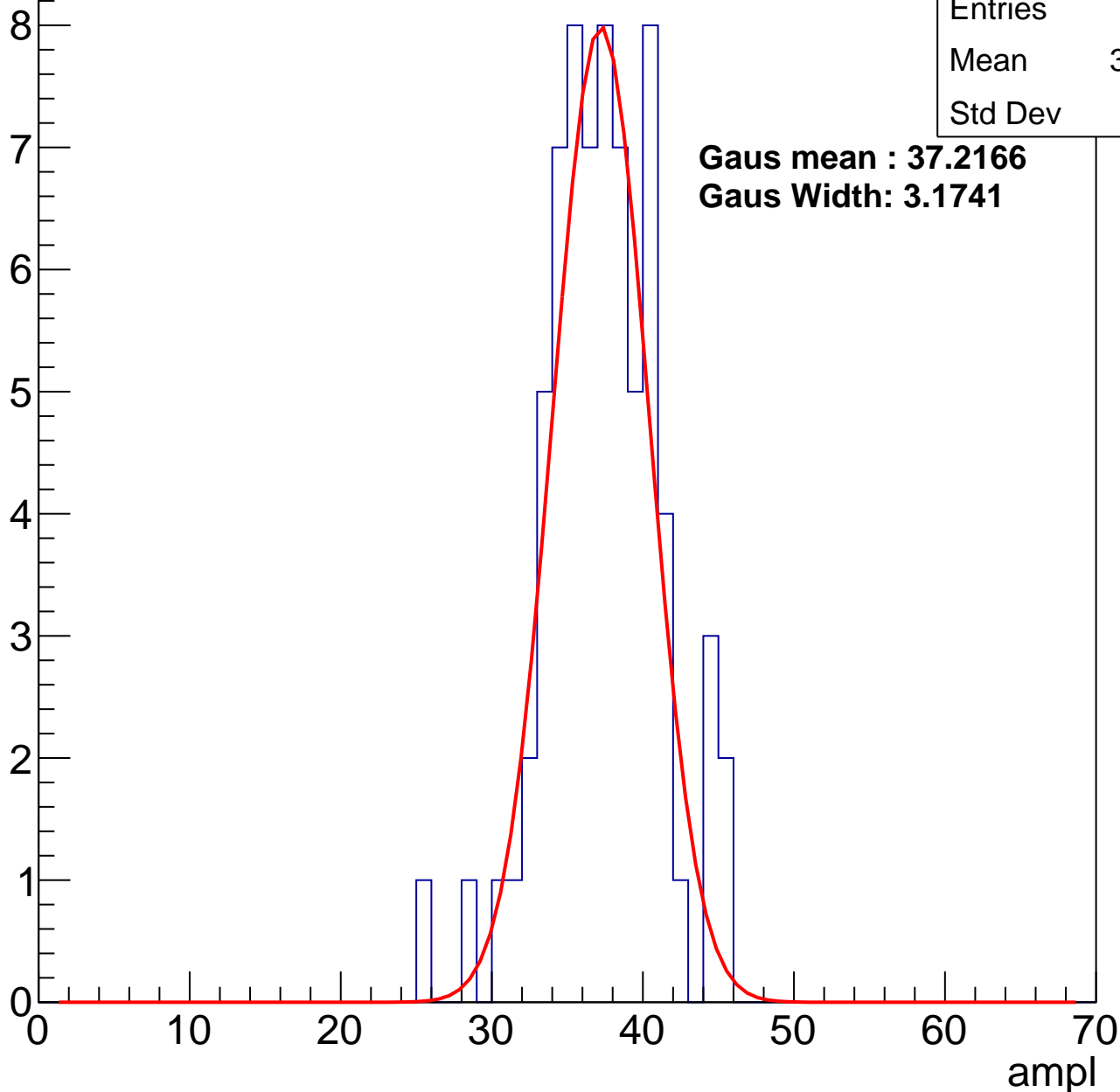
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	36.87
Std Dev	3.76

**Gaus mean : 37.2166**

**Gaus Width: 3.1741**



# B1L103S, U3-ch94, adc2

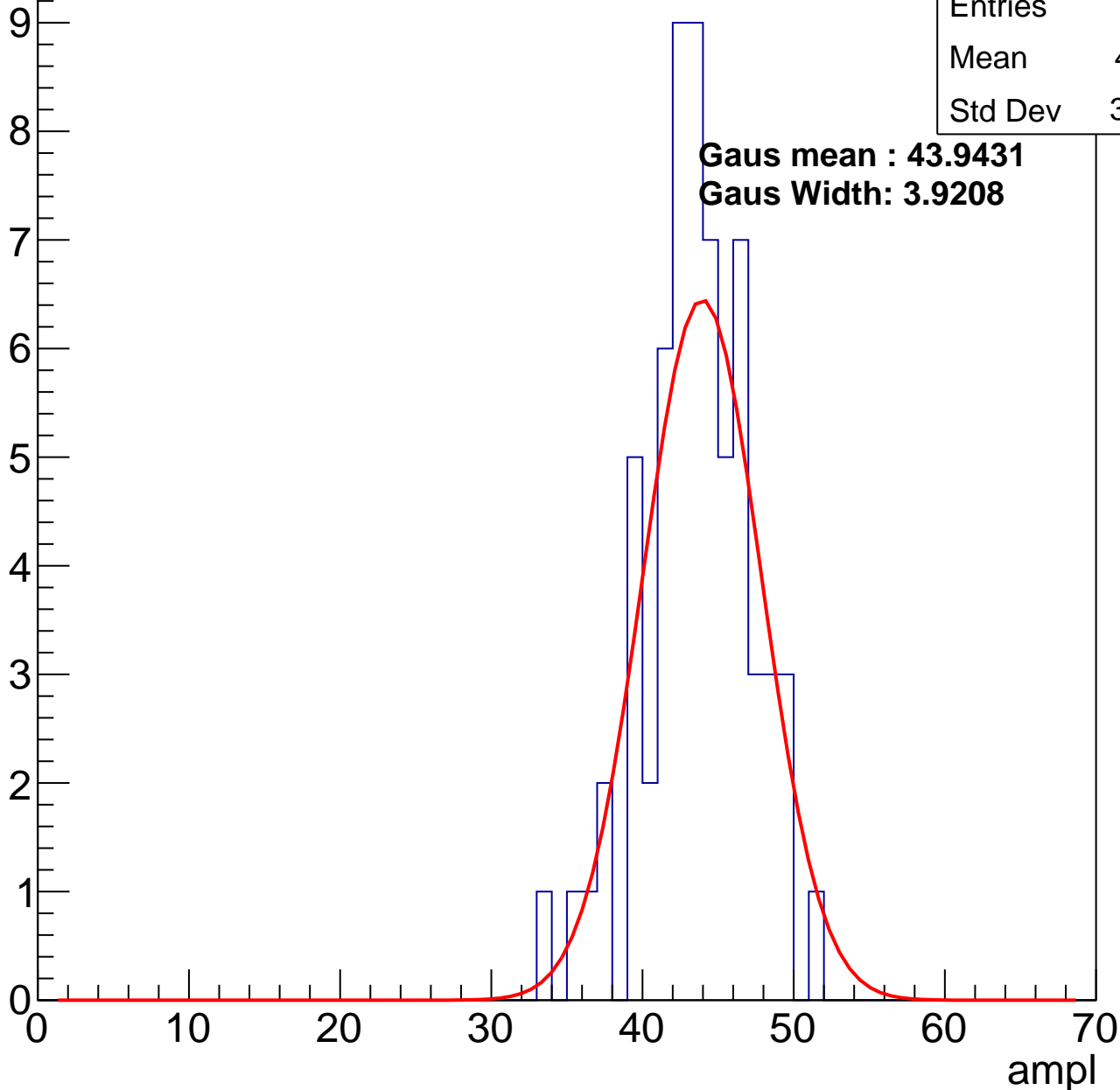
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	43.11
Std Dev	3.509

**Gaus mean : 43.9431**

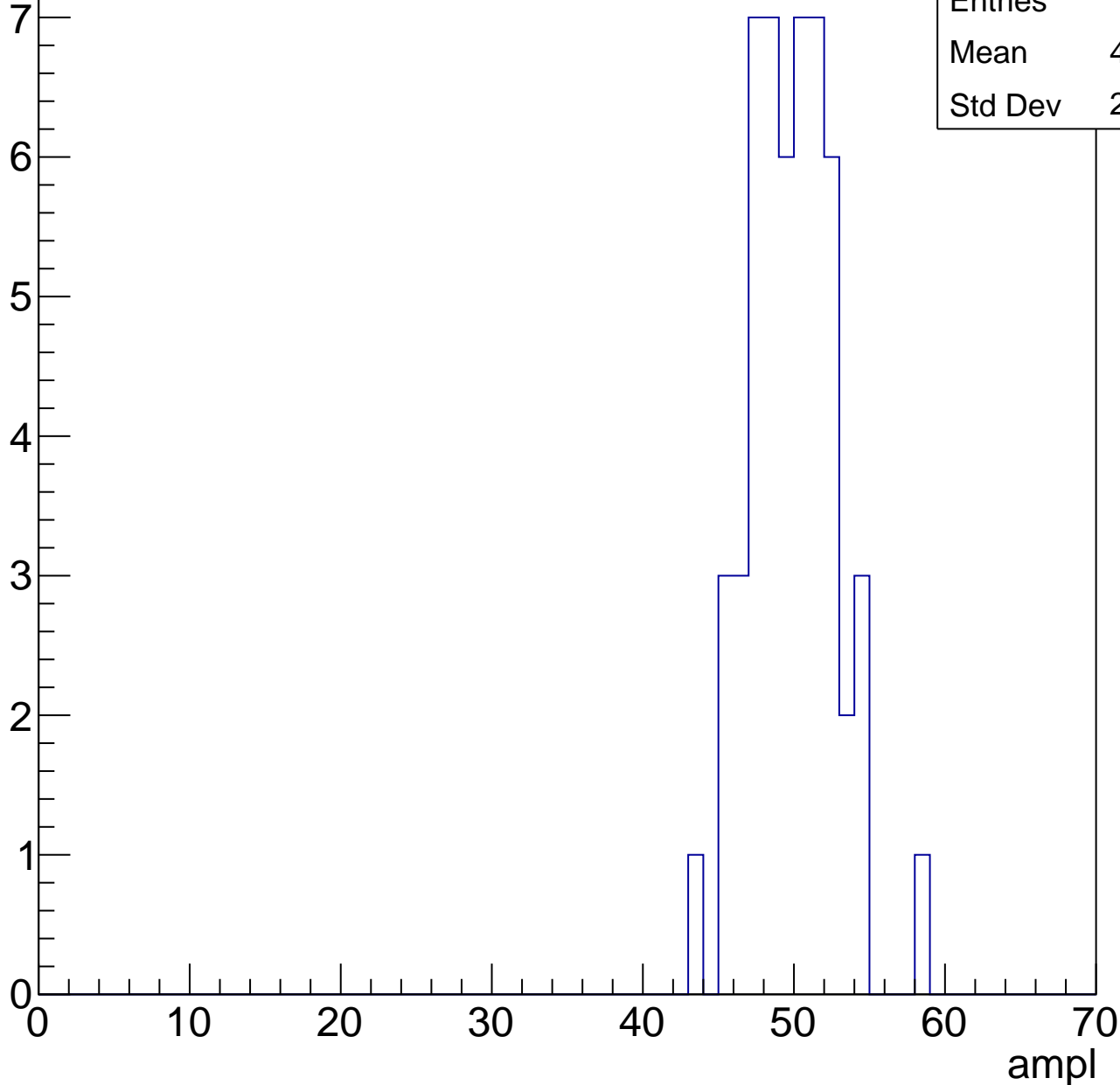
**Gaus Width: 3.9208**



# B1L103S, U3-ch94, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

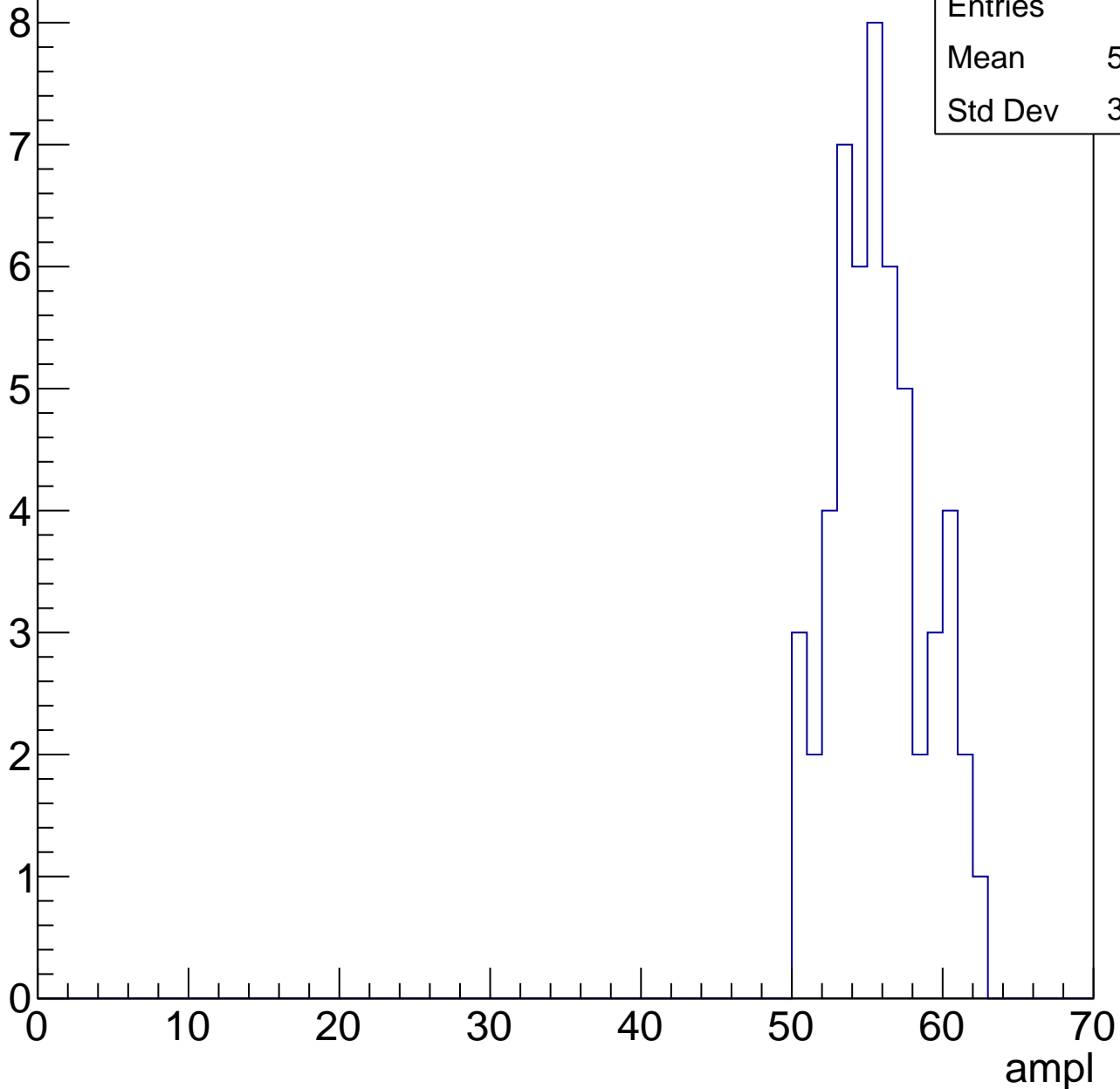


# B1L103S, U3-ch94, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

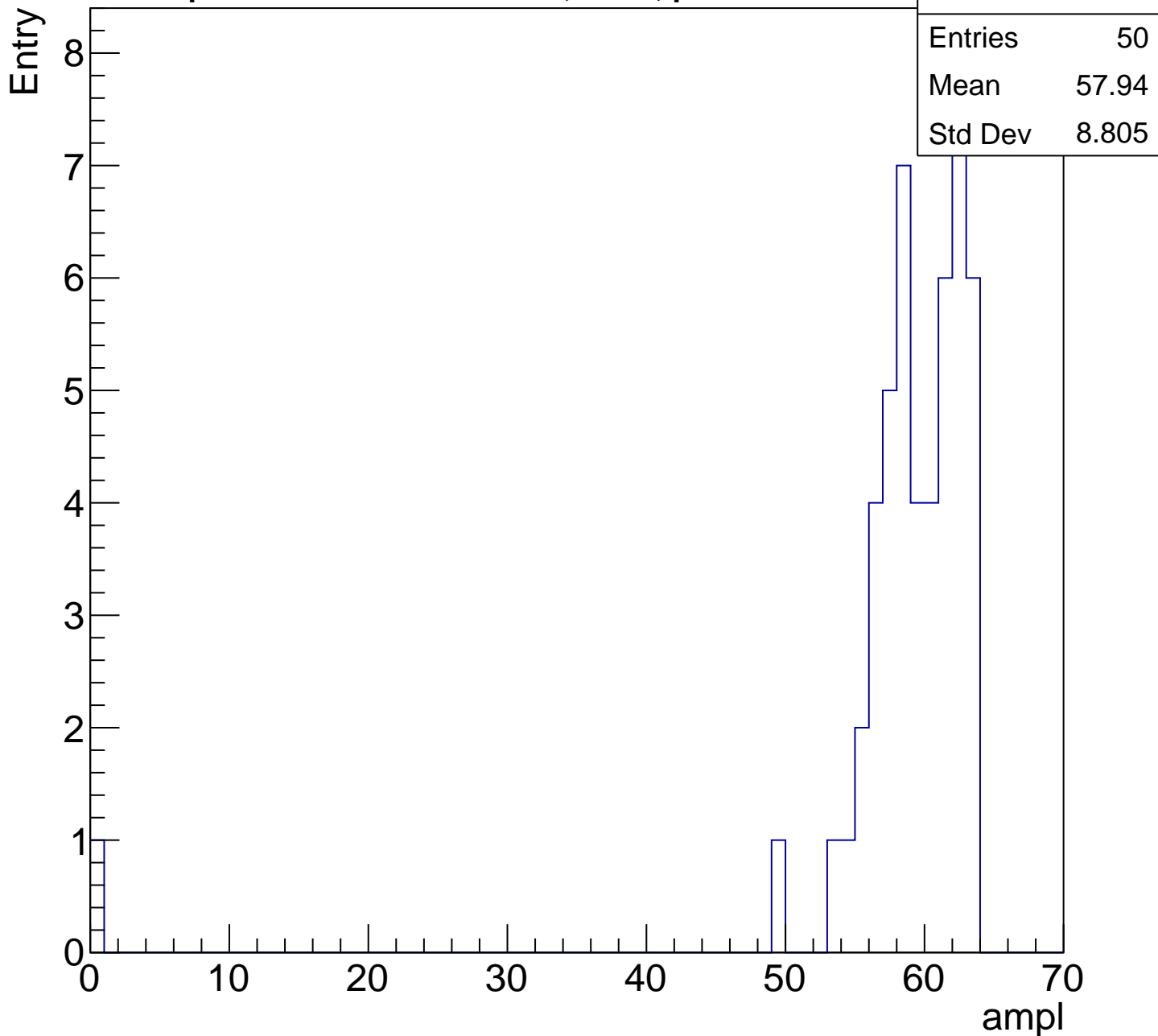
Entry

Entries	53
Mean	55.34
Std Dev	3.022



# B1L103S, U3-ch94, adc5

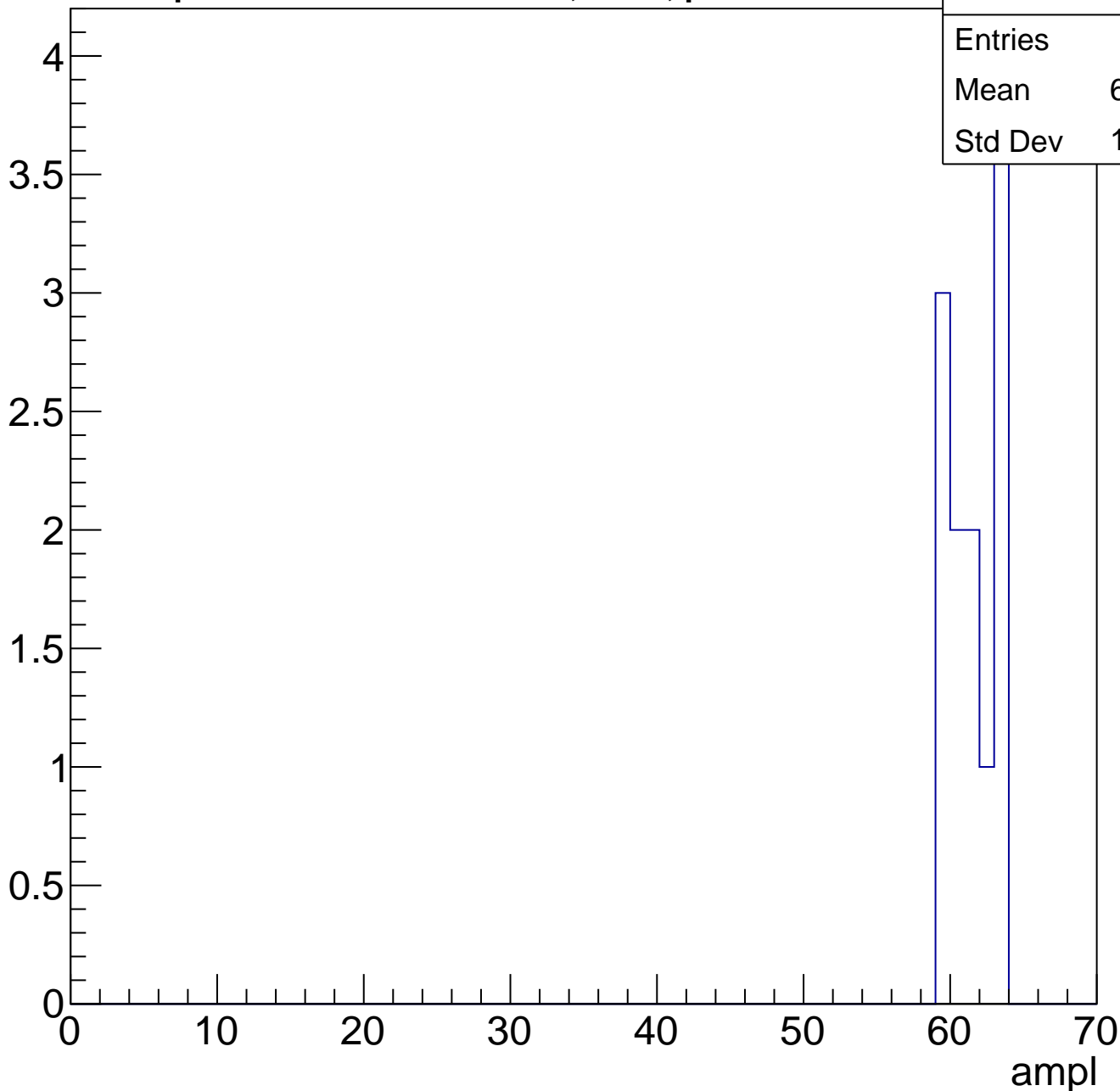
calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U3-ch94, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	12
Mean	61.08
Std Dev	1.605



# B1L103S, U3-ch94, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U3-ch95, adc0

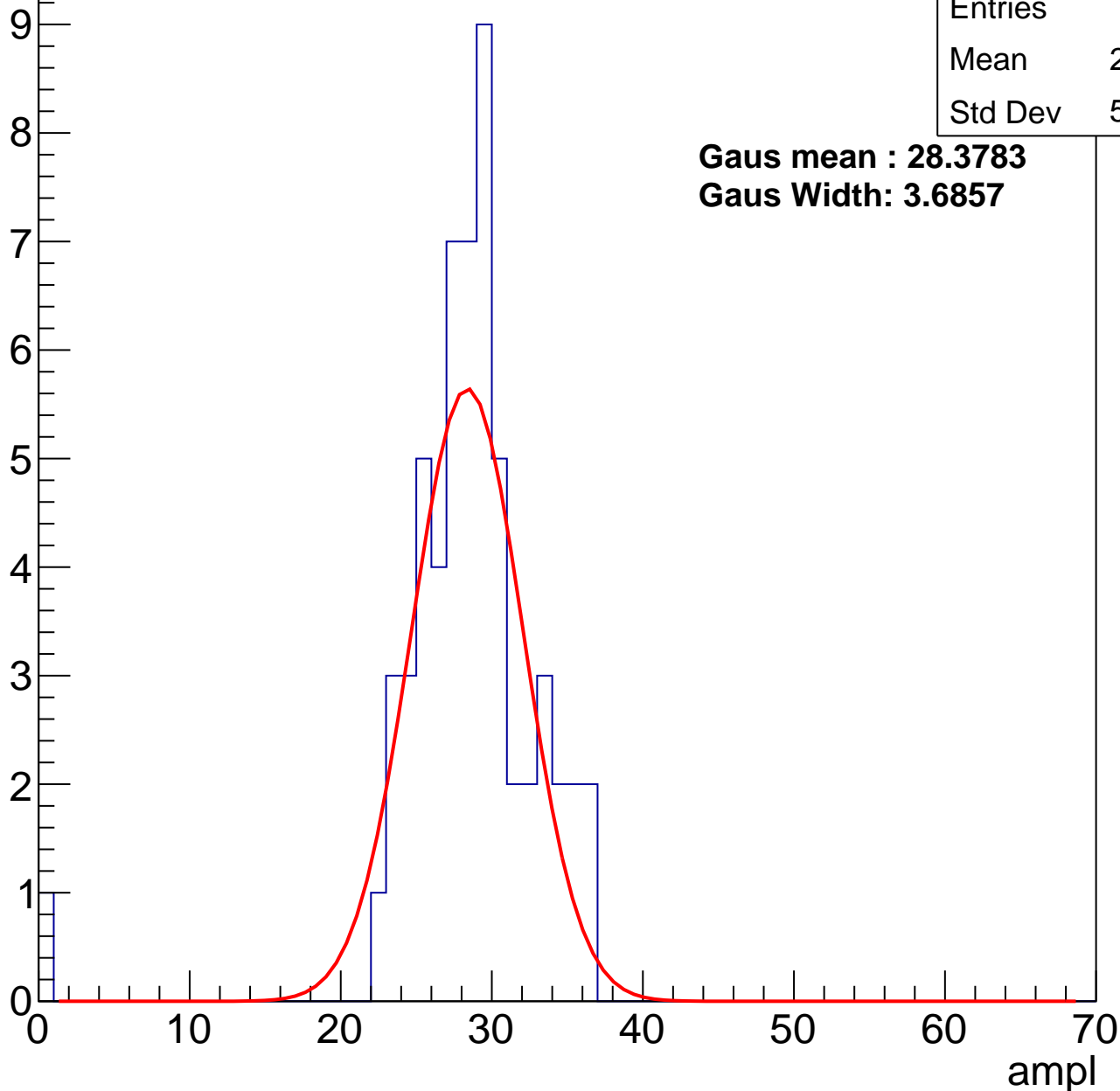
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	27.98
Std Dev	5.022

**Gaus mean : 28.3783**

**Gaus Width: 3.6857**



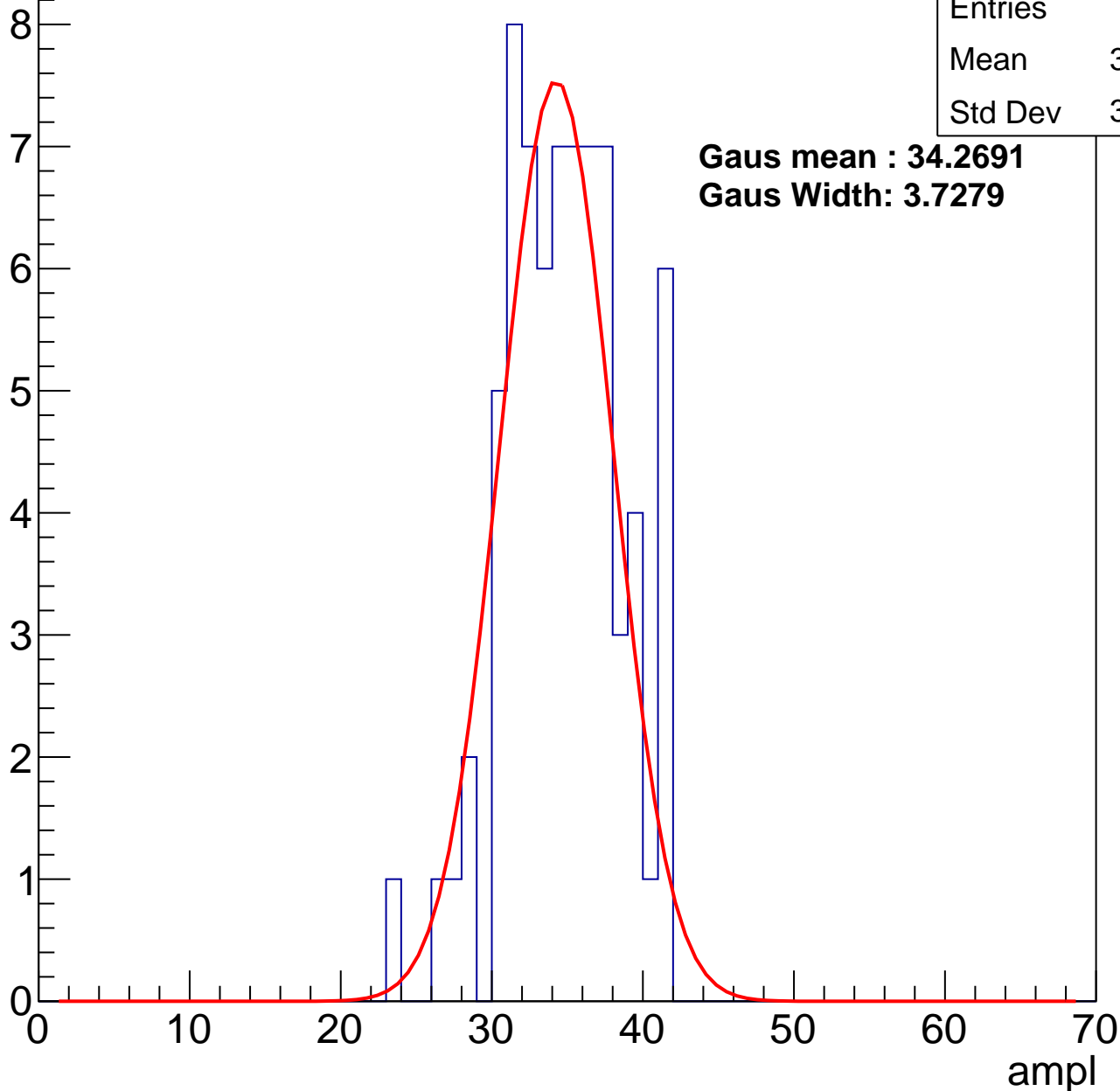
# B1L103S, U3-ch95, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	34.27
Std Dev	3.815

**Gaus mean : 34.2691**  
**Gaus Width: 3.7279**



# B1L103S, U3-ch95, adc2

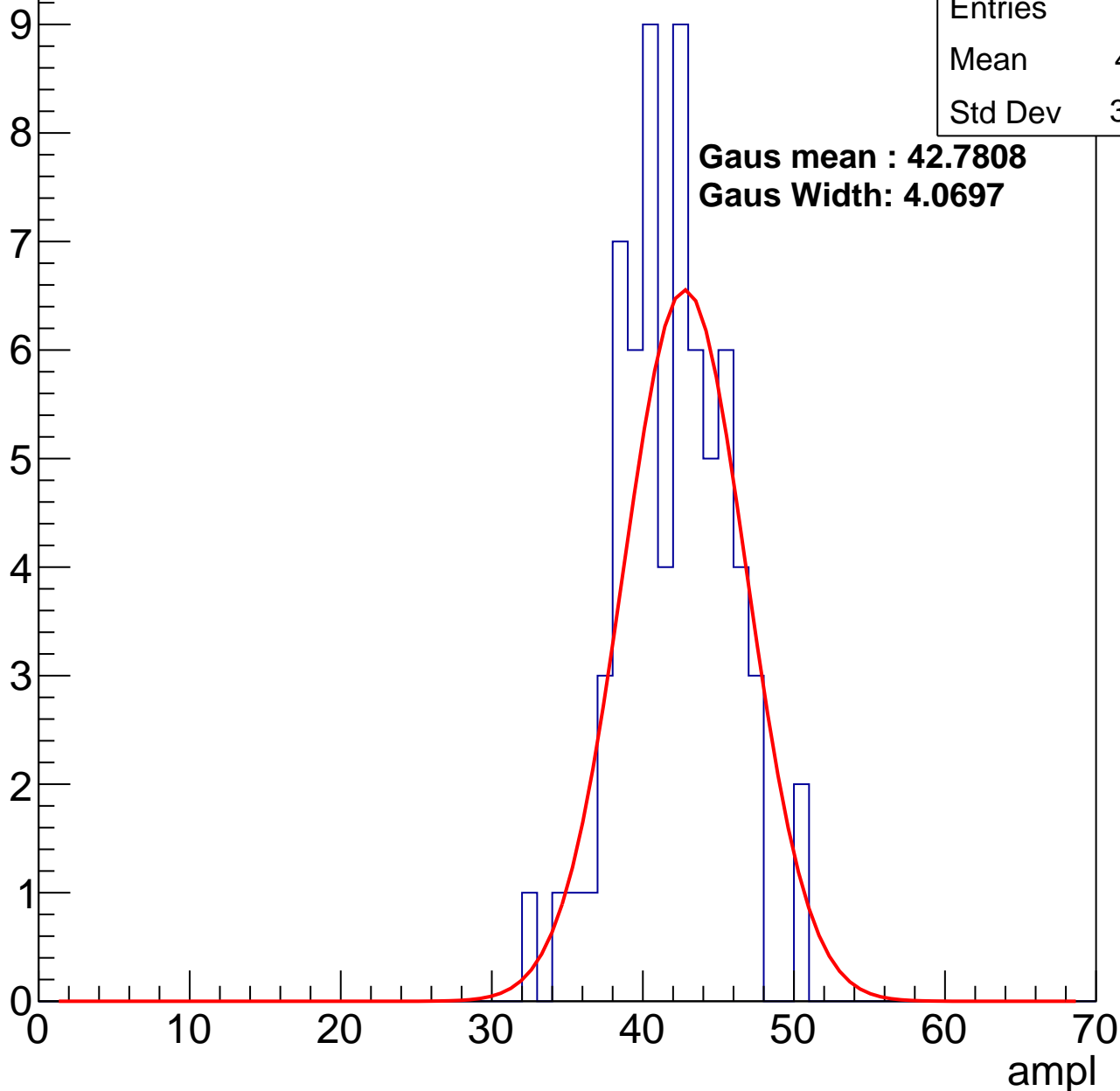
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	41.51
Std Dev	3.558

**Gaus mean : 42.7808**

**Gaus Width: 4.0697**

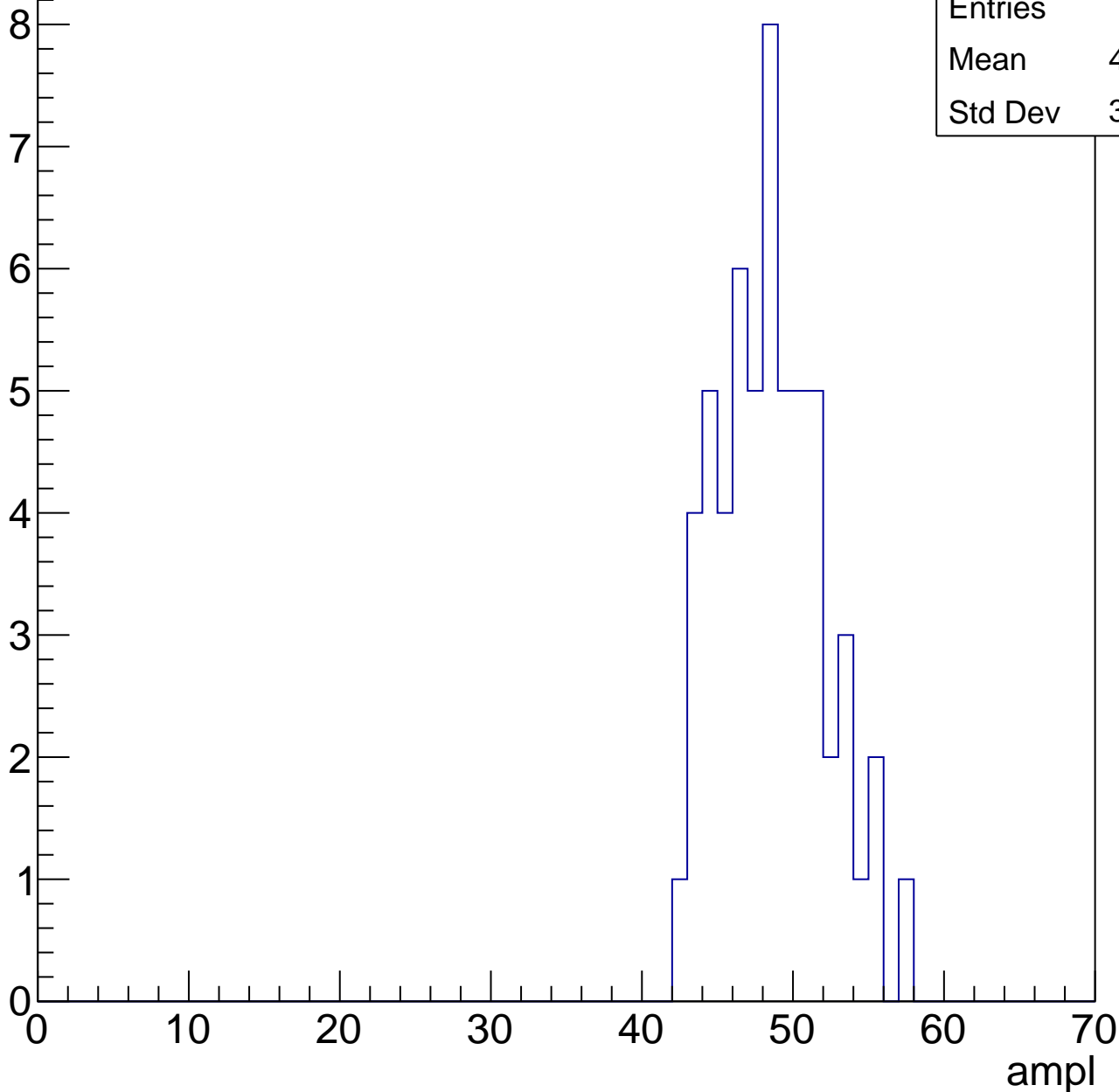


# B1L103S, U3-ch95, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

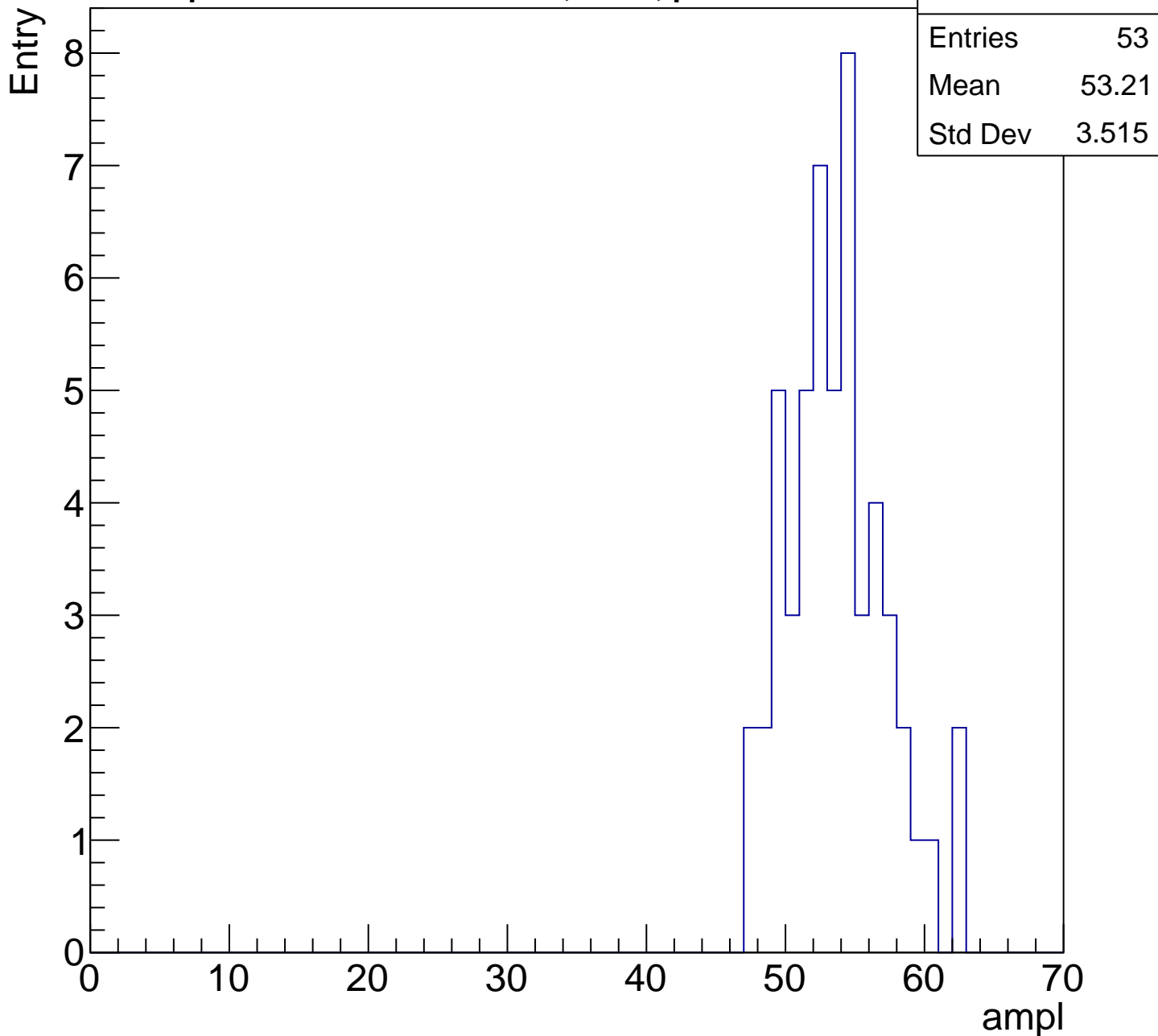
Entry

Entries	57
Mean	48.12
Std Dev	3.434



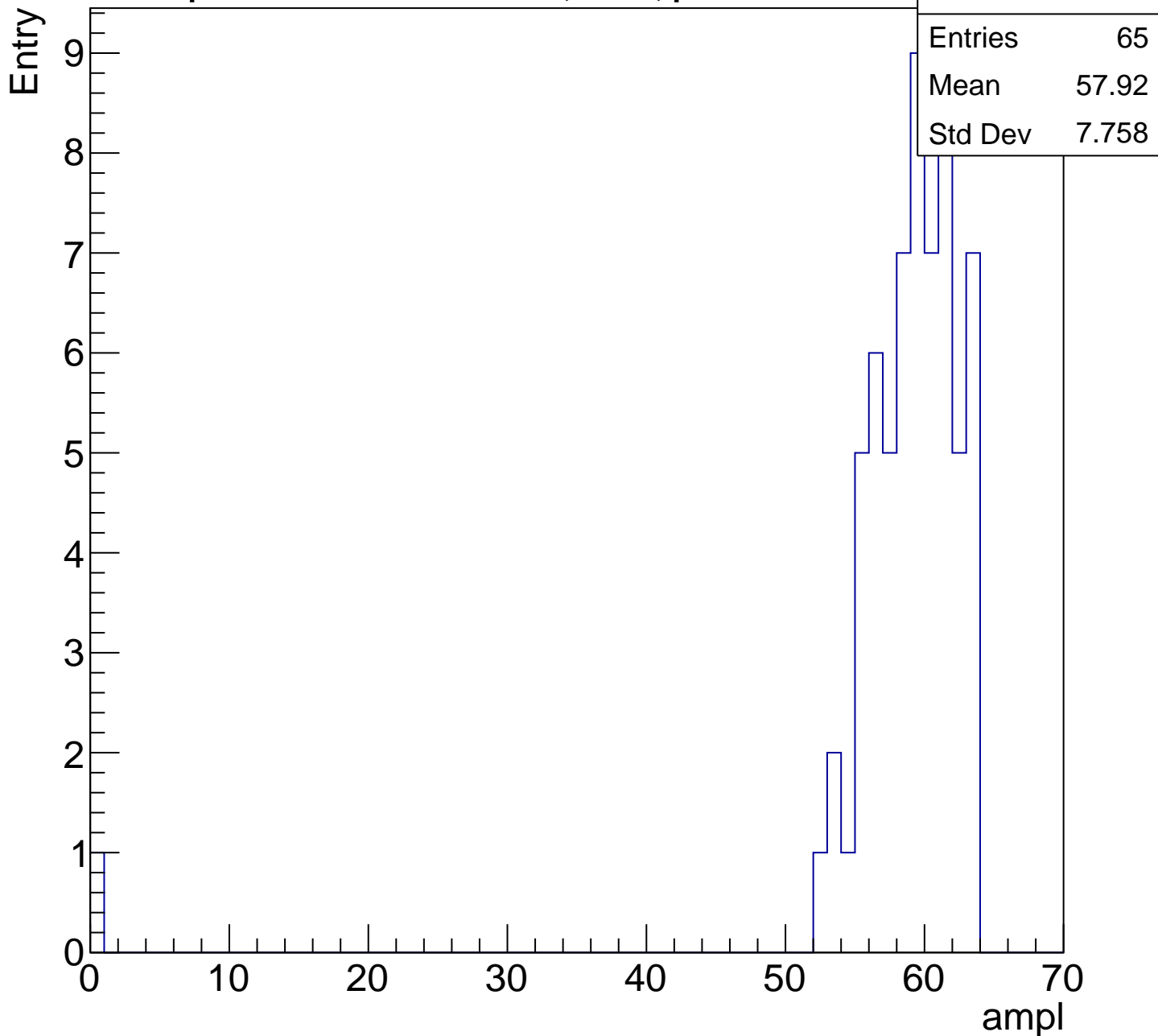
# B1L103S, U3-ch95, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U3-ch95, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U3-ch95, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries

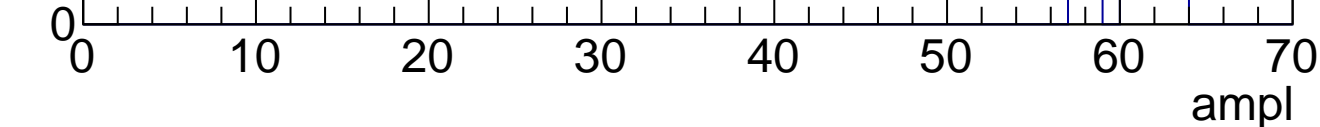
11

Mean

61

Std Dev

1.954





# B1L103S, U3-ch95, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L103S, U3-ch96, adc0

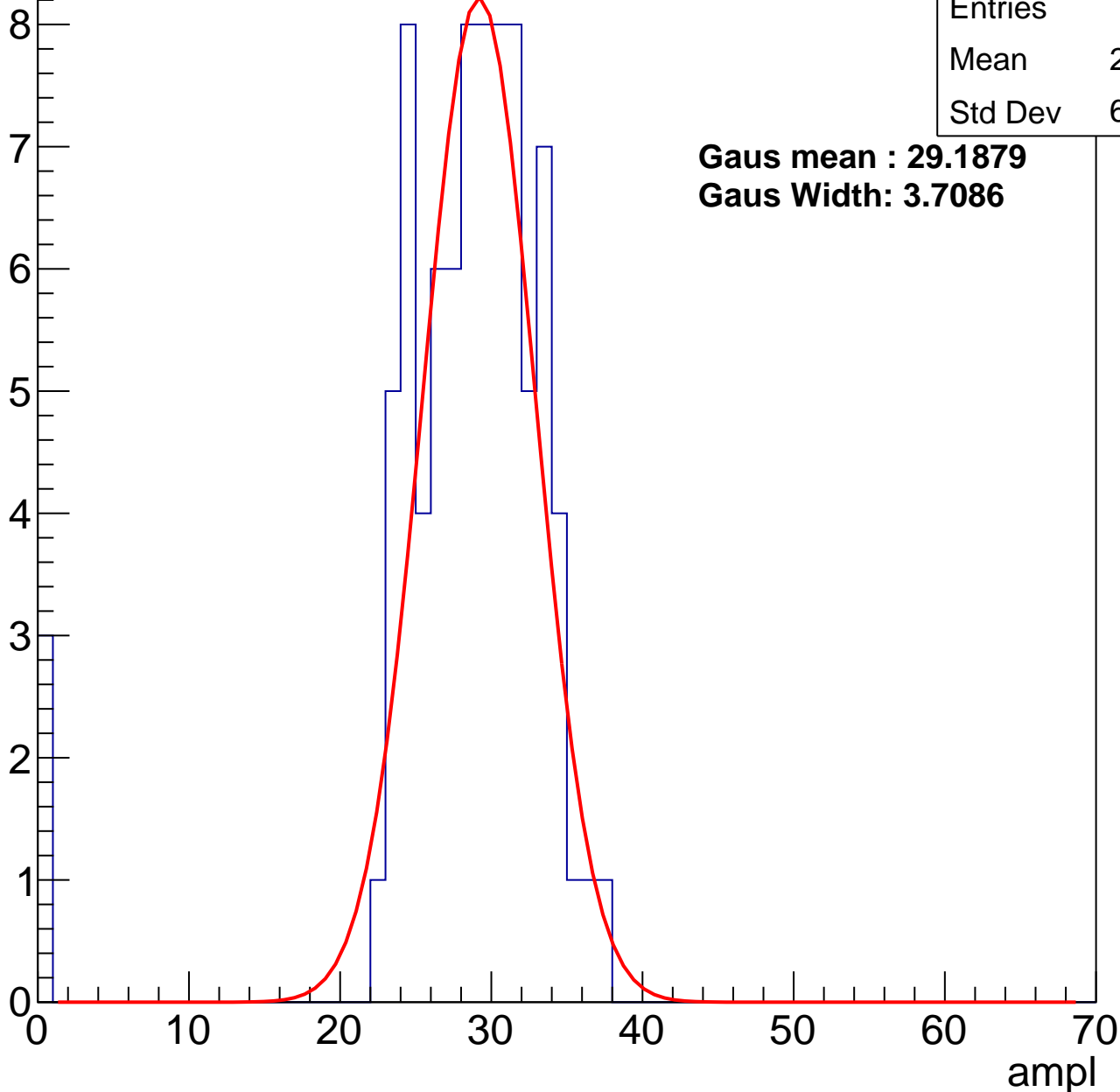
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	84
Mean	27.69
Std Dev	6.366

**Gaus mean : 29.1879**

**Gaus Width: 3.7086**



# B1L103S, U3-ch96, adc1

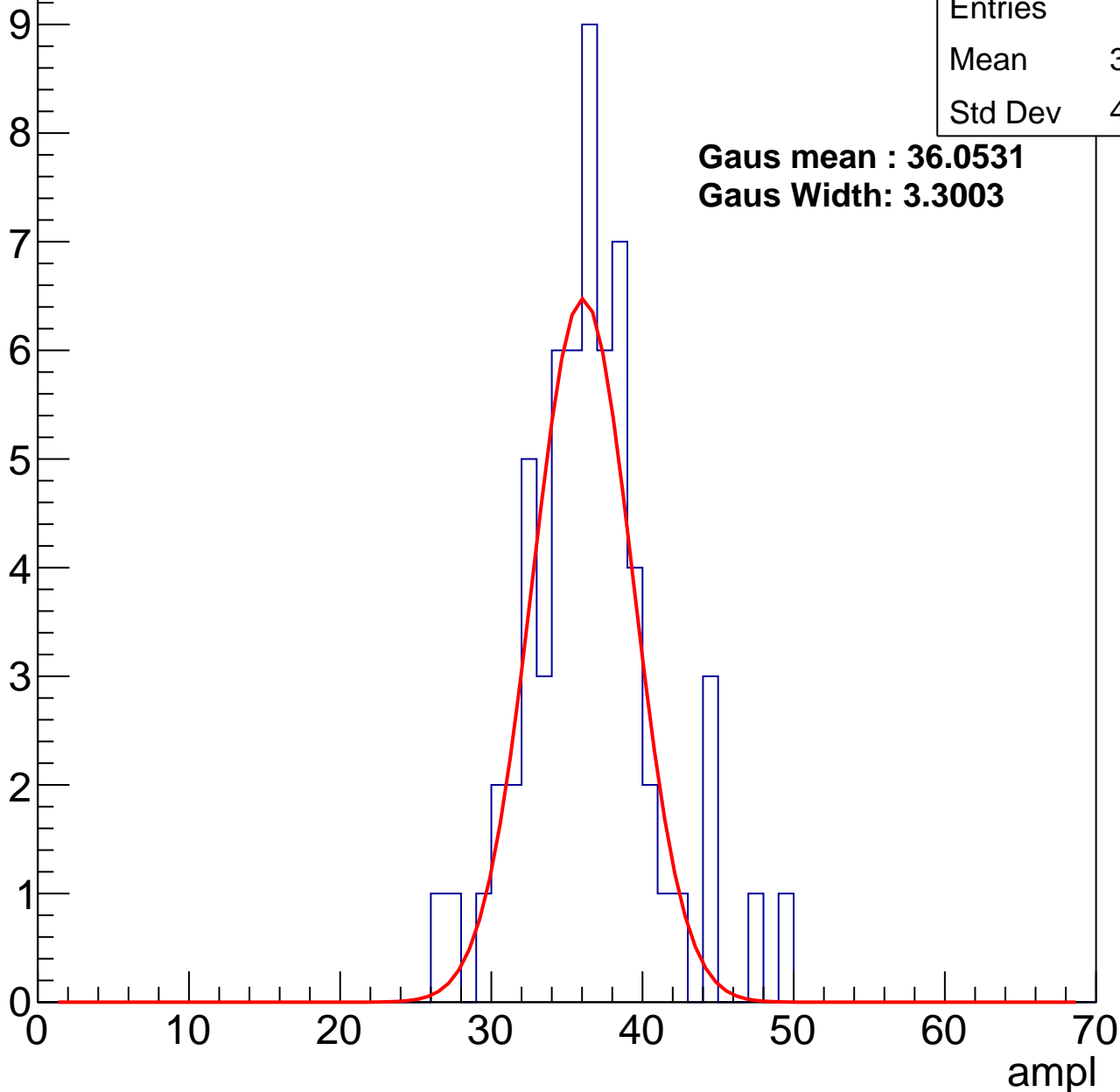
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	36.06
Std Dev	4.276

**Gaus mean : 36.0531**

**Gaus Width: 3.3003**



# B1L103S, U3-ch96, adc2

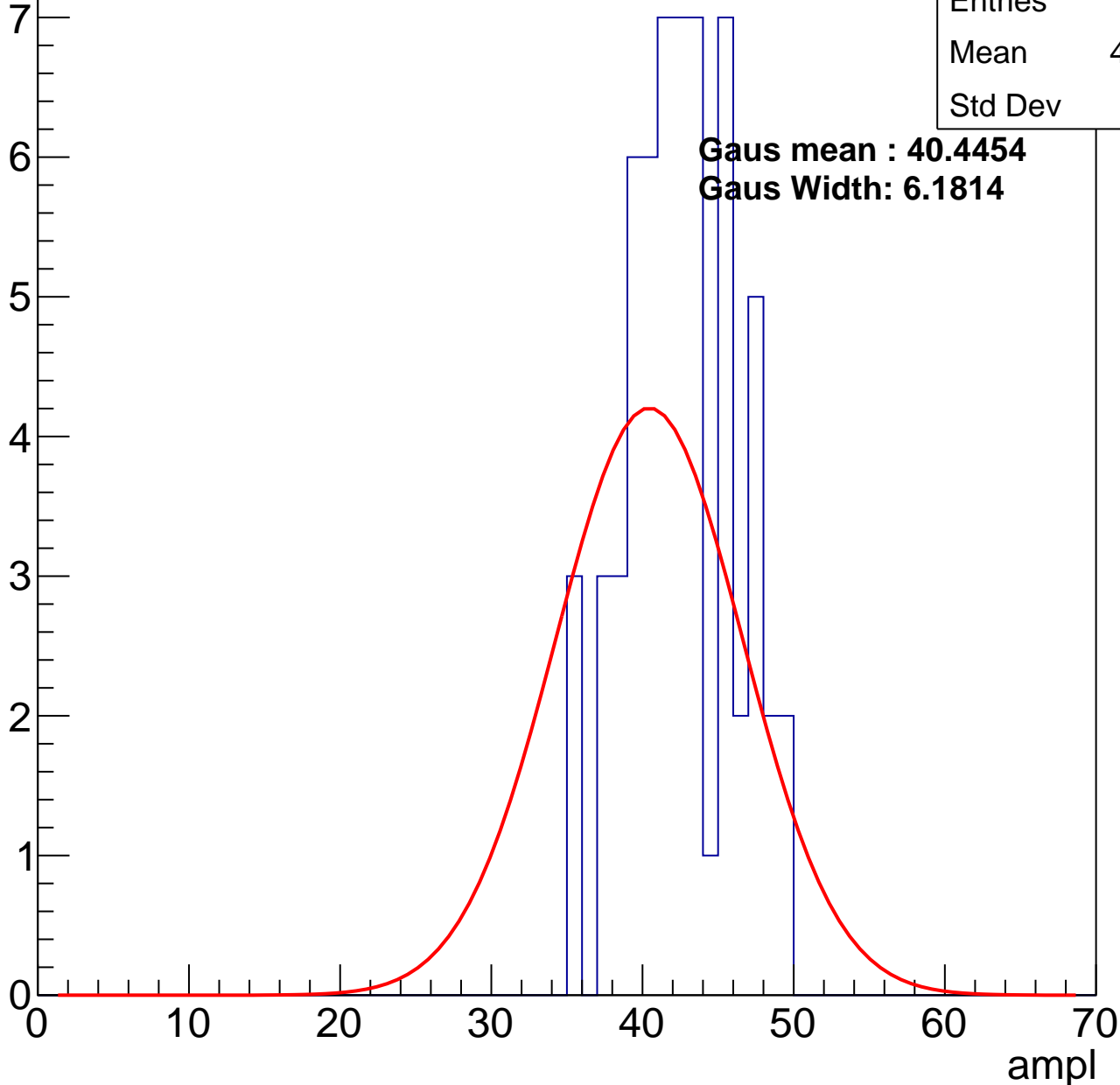
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	42.07
Std Dev	3.52

**Gaus mean : 40.4454**

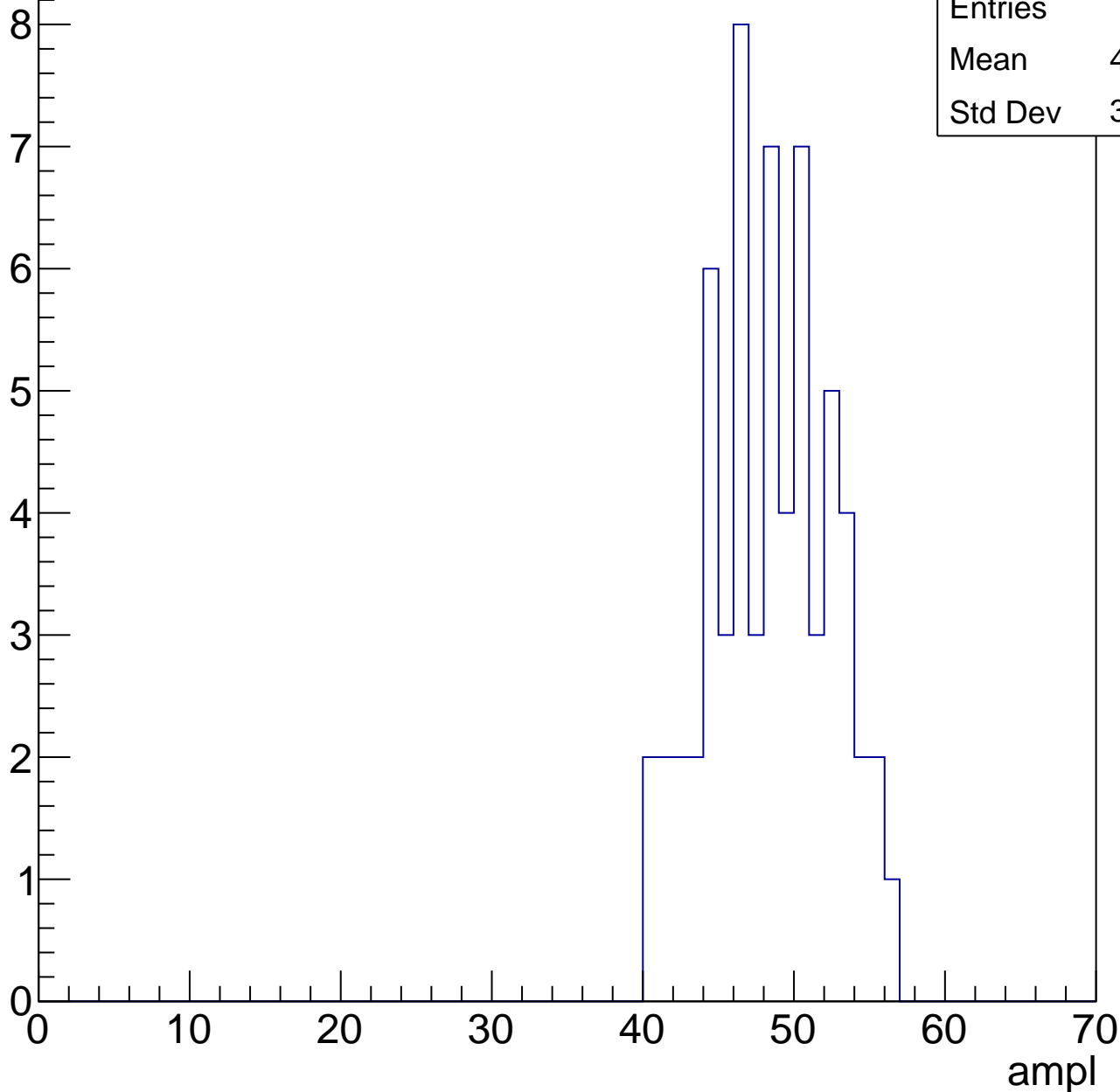
**Gaus Width: 6.1814**



# B1L103S, U3-ch96, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

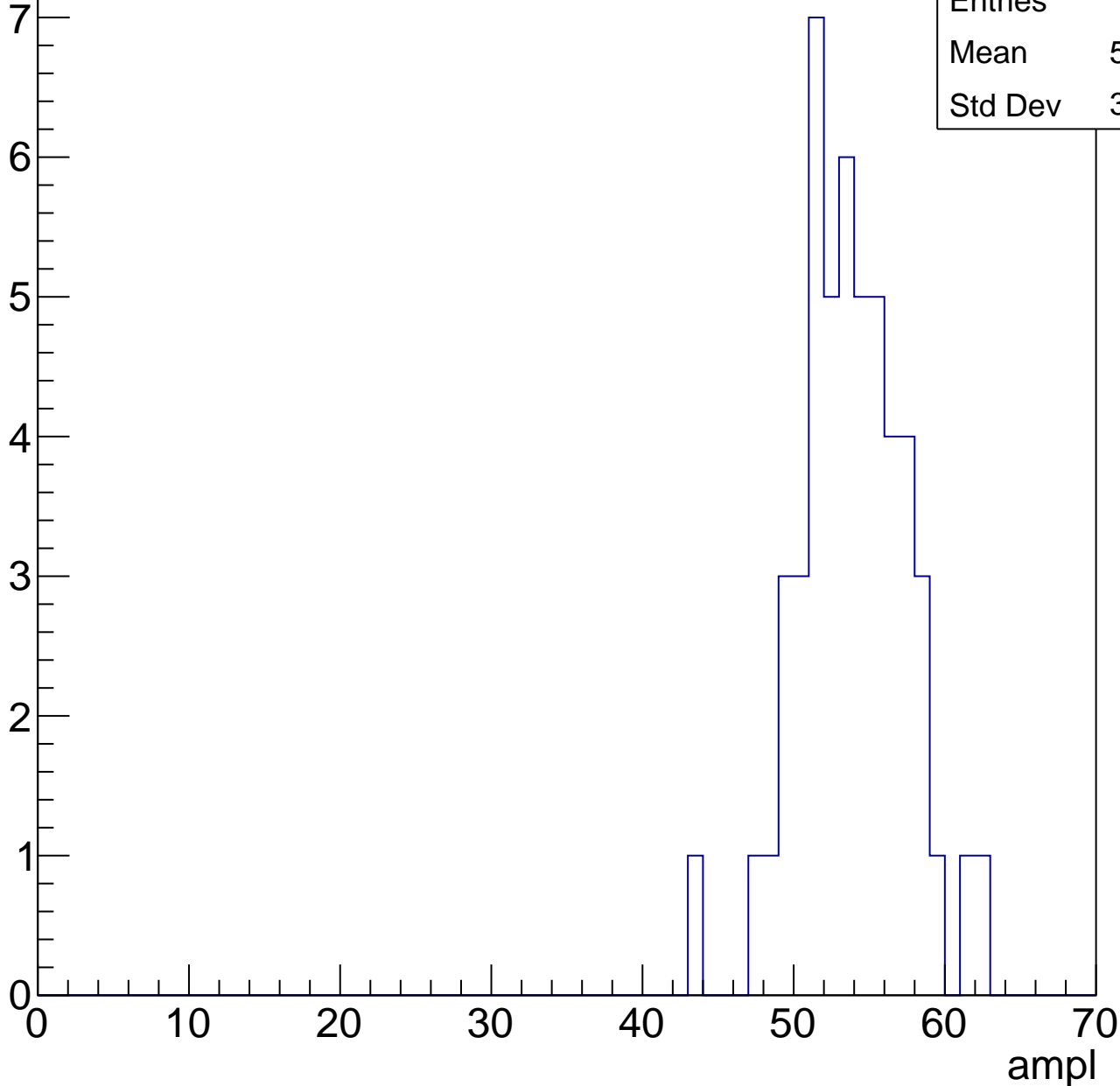


# B1L103S, U3-ch96, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	53.39
Std Dev	3.548



# B1L103S, U3-ch96, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

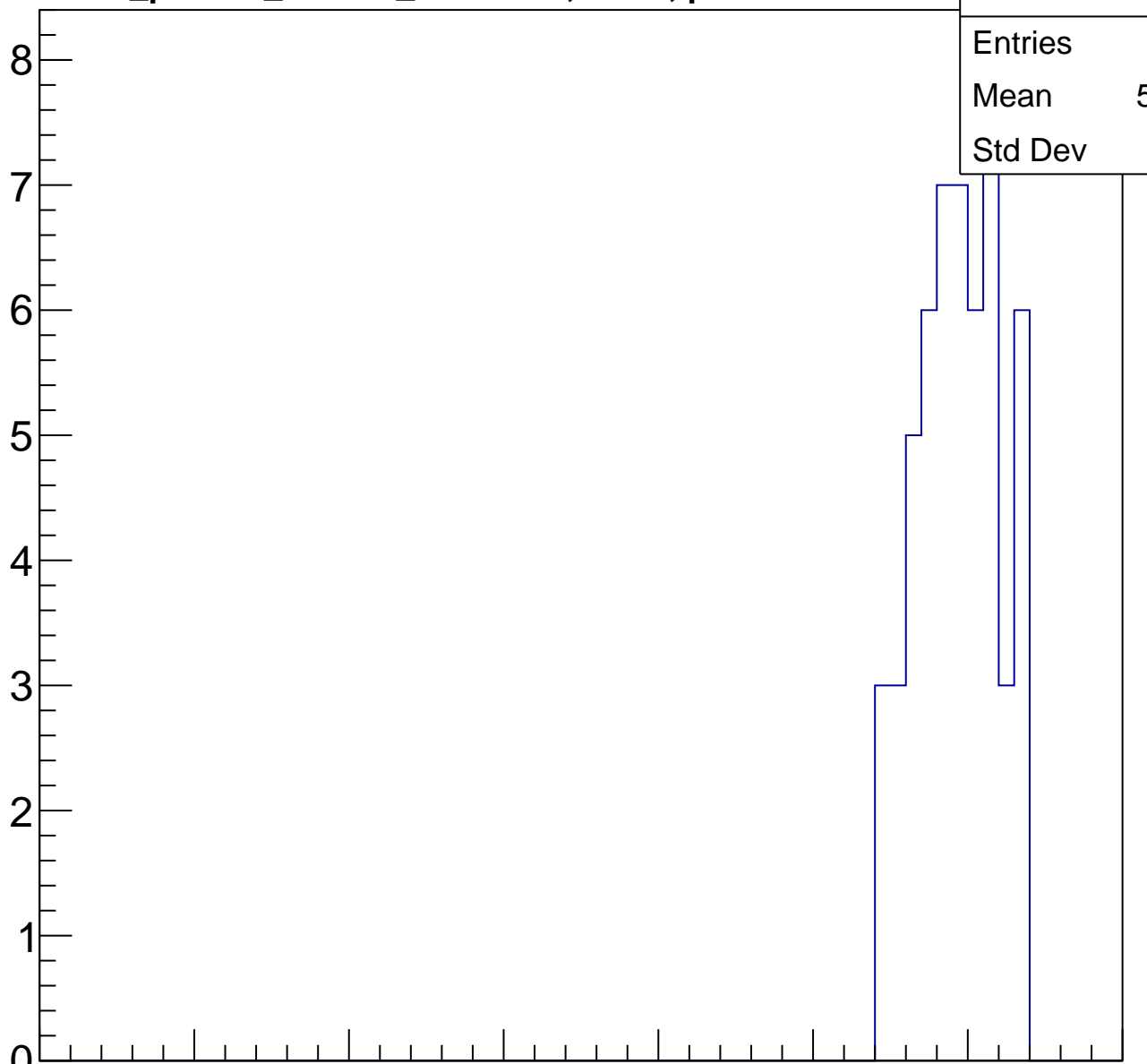
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	54
Mean	58.89
Std Dev	2.58

ampl

0 10 20 30 40 50 60 70

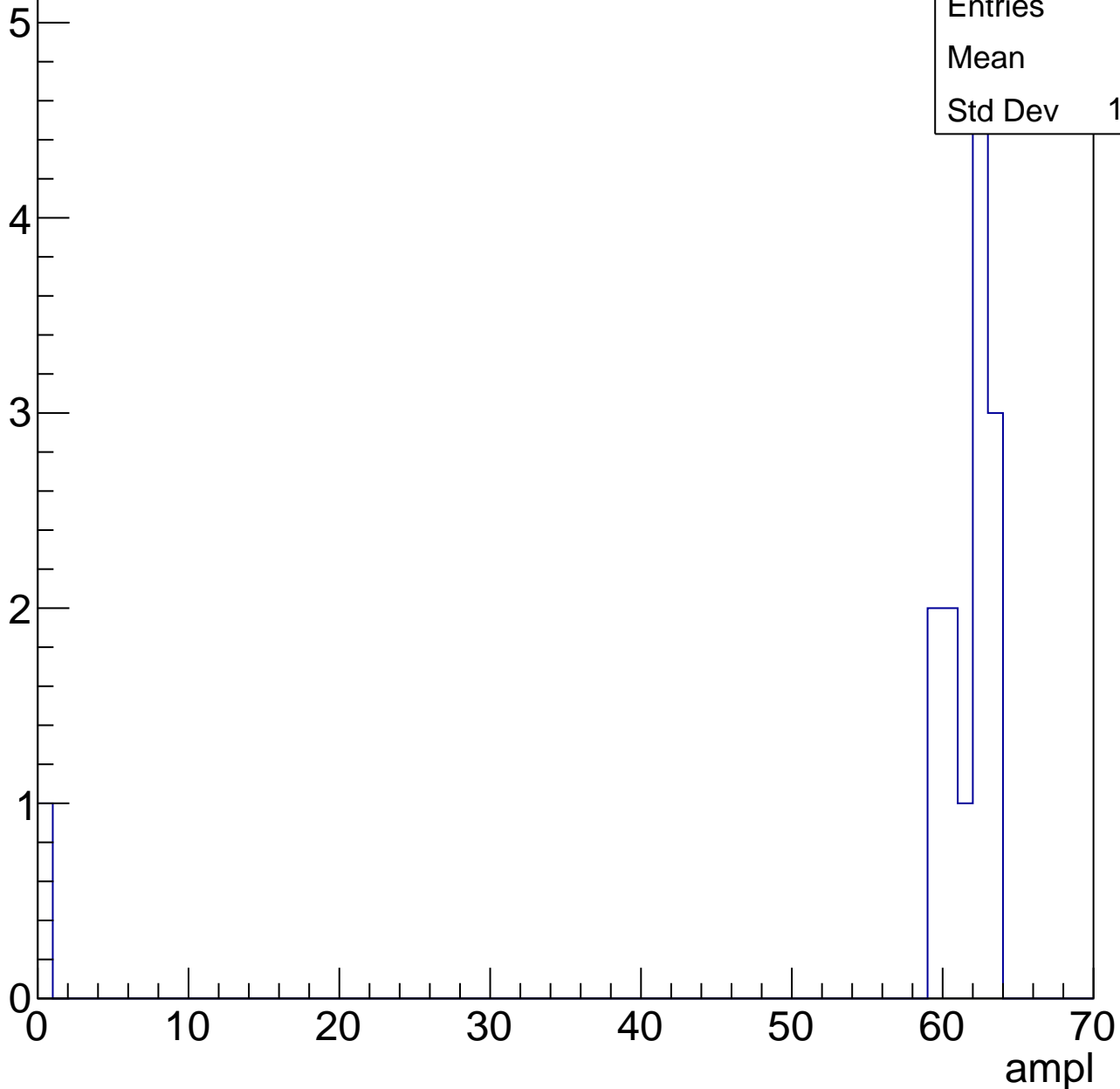


# B1L103S, U3-ch96, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	14
Mean	57
Std Dev	15.87





# B1L103S, U3-ch96, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

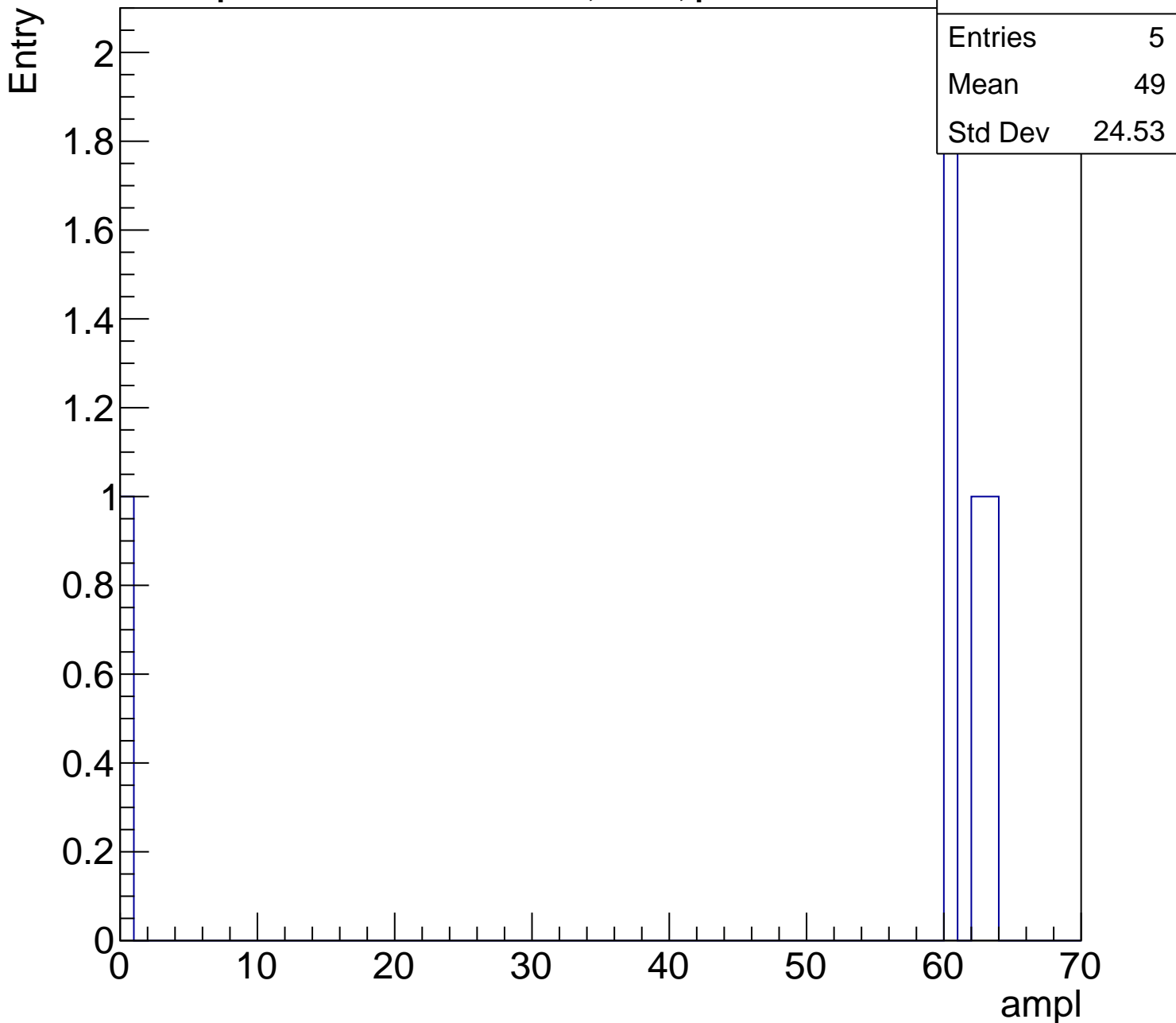
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	49
Std Dev	24.53

0 10 20 30 40 50 60 70

ampl



# B1L103S, U3-ch97, adc0

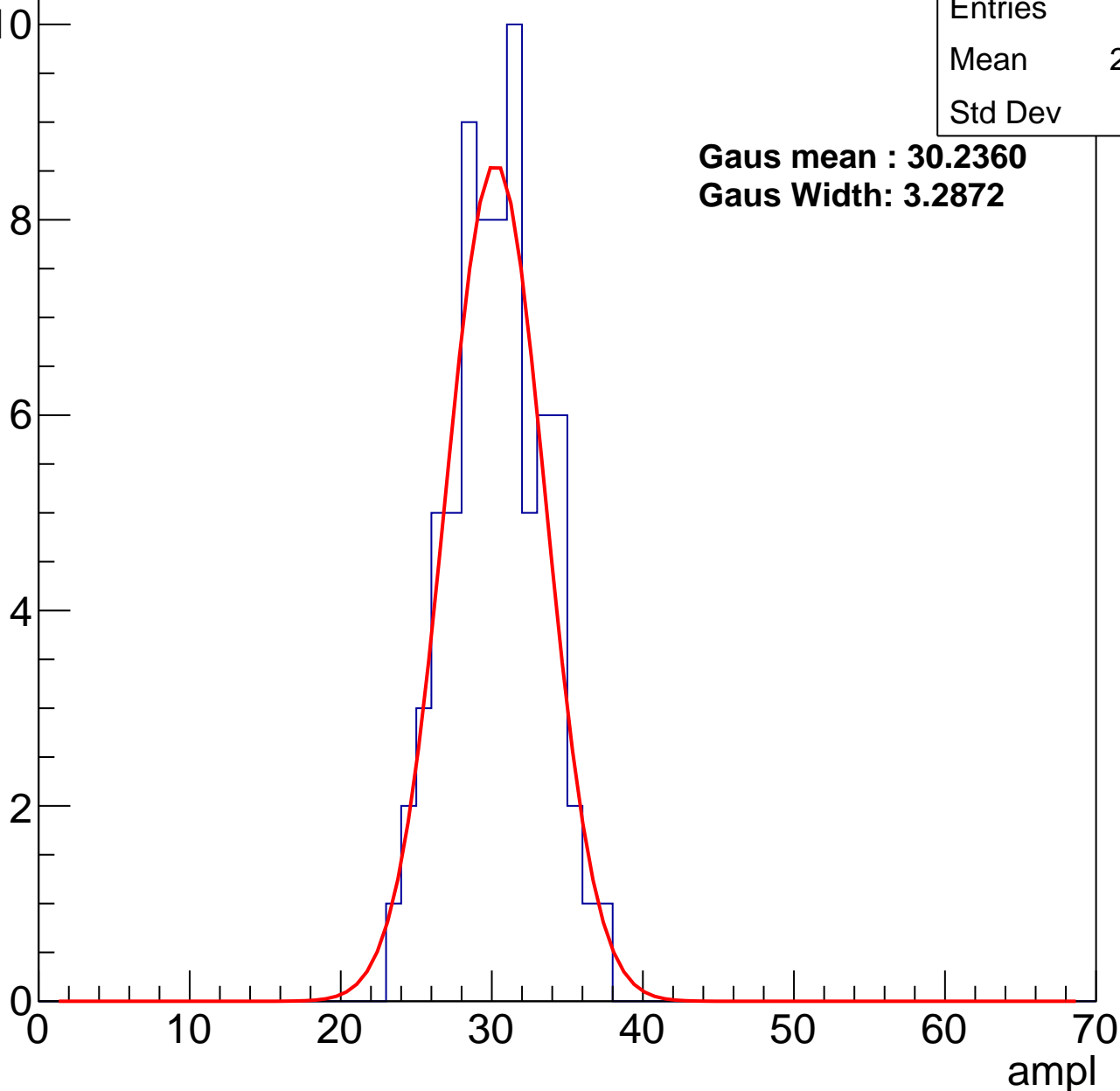
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	29.86
Std Dev	3.07

**Gaus mean : 30.2360**

**Gaus Width: 3.2872**



# B1L103S, U3-ch97, adc1

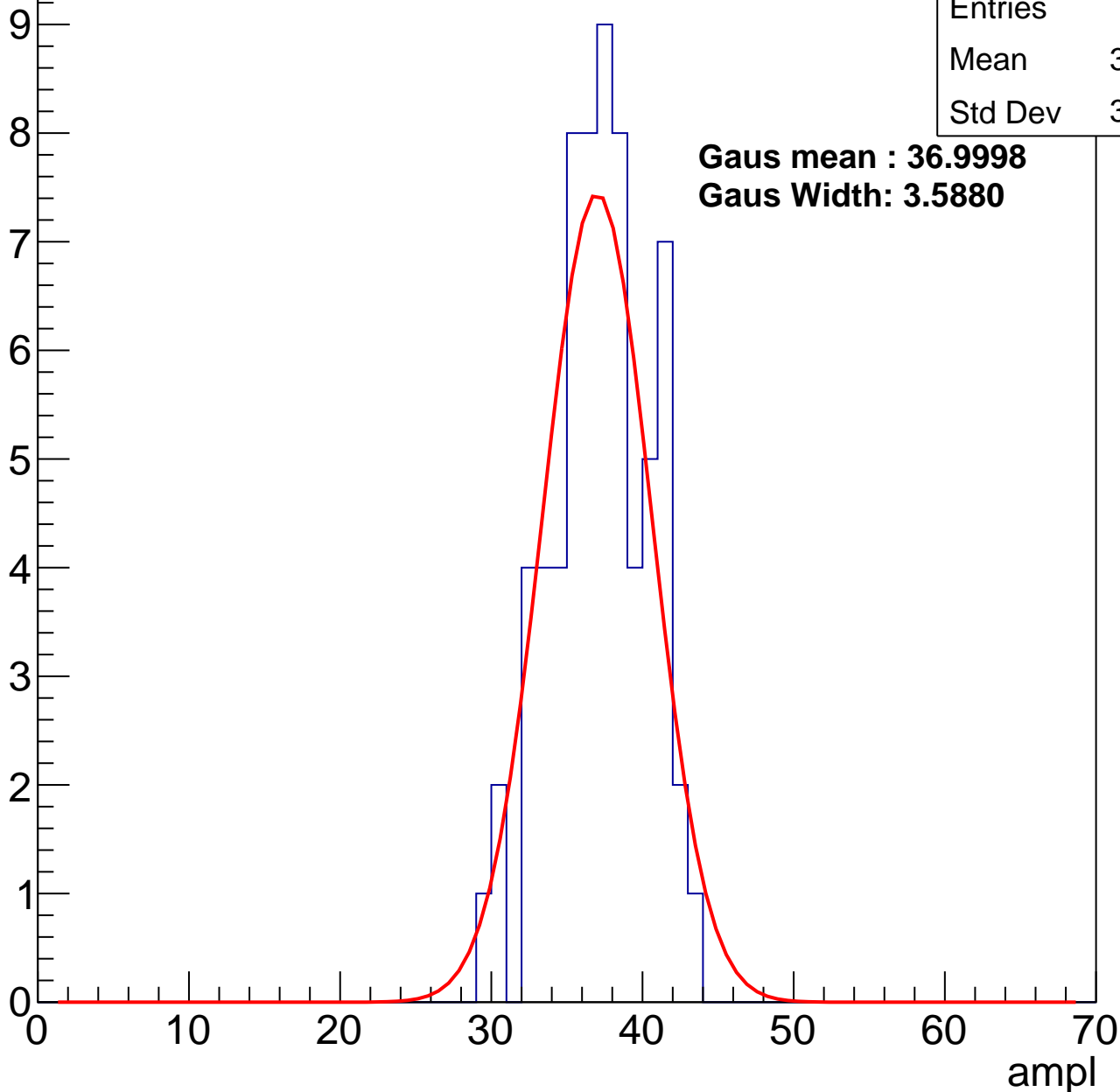
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	36.72
Std Dev	3.147

**Gaus mean : 36.9998**

**Gaus Width: 3.5880**



# B1L103S, U3-ch97, adc2

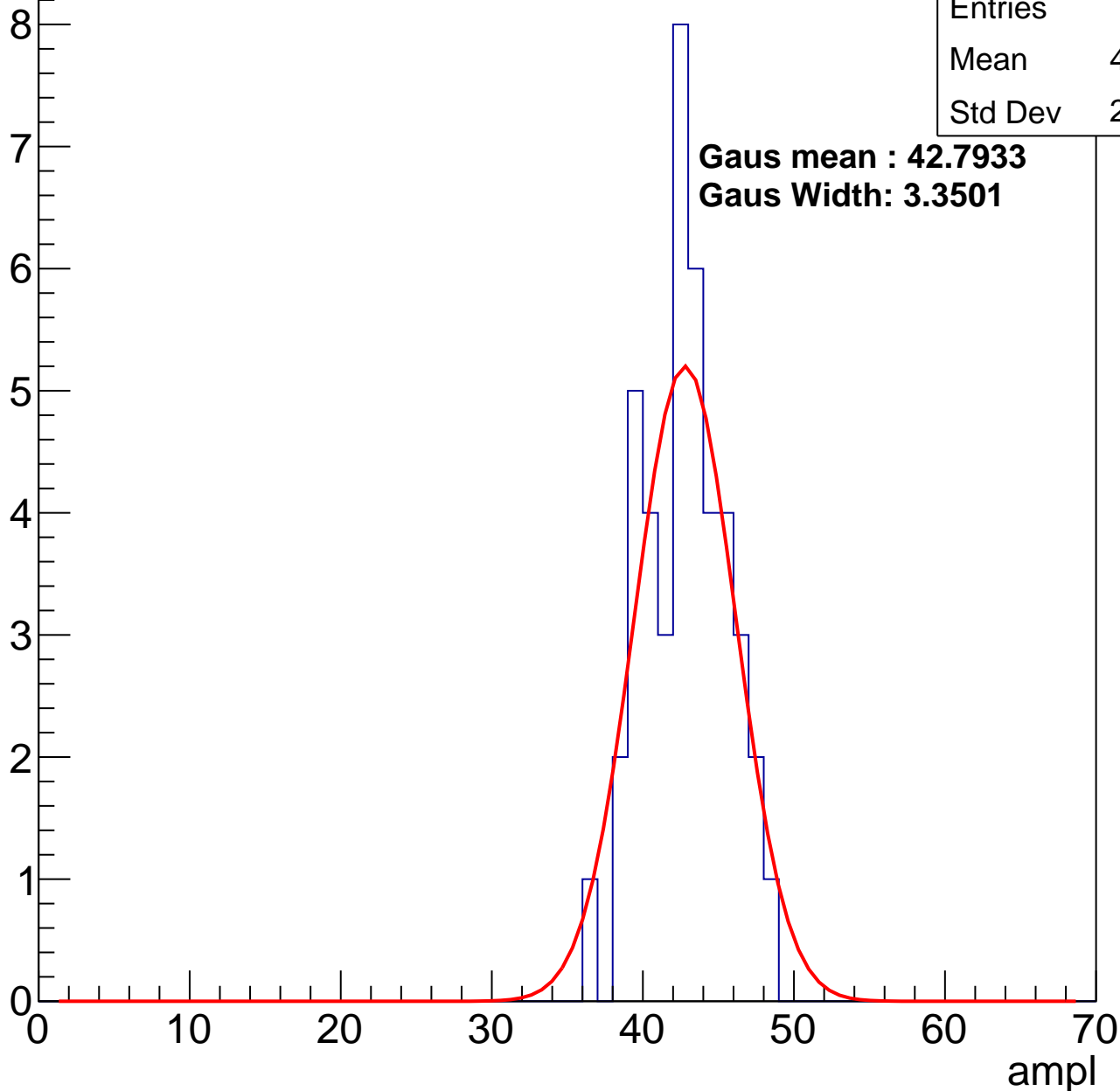
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	43
Mean	42.33
Std Dev	2.726

**Gaus mean : 42.7933**

**Gaus Width: 3.3501**

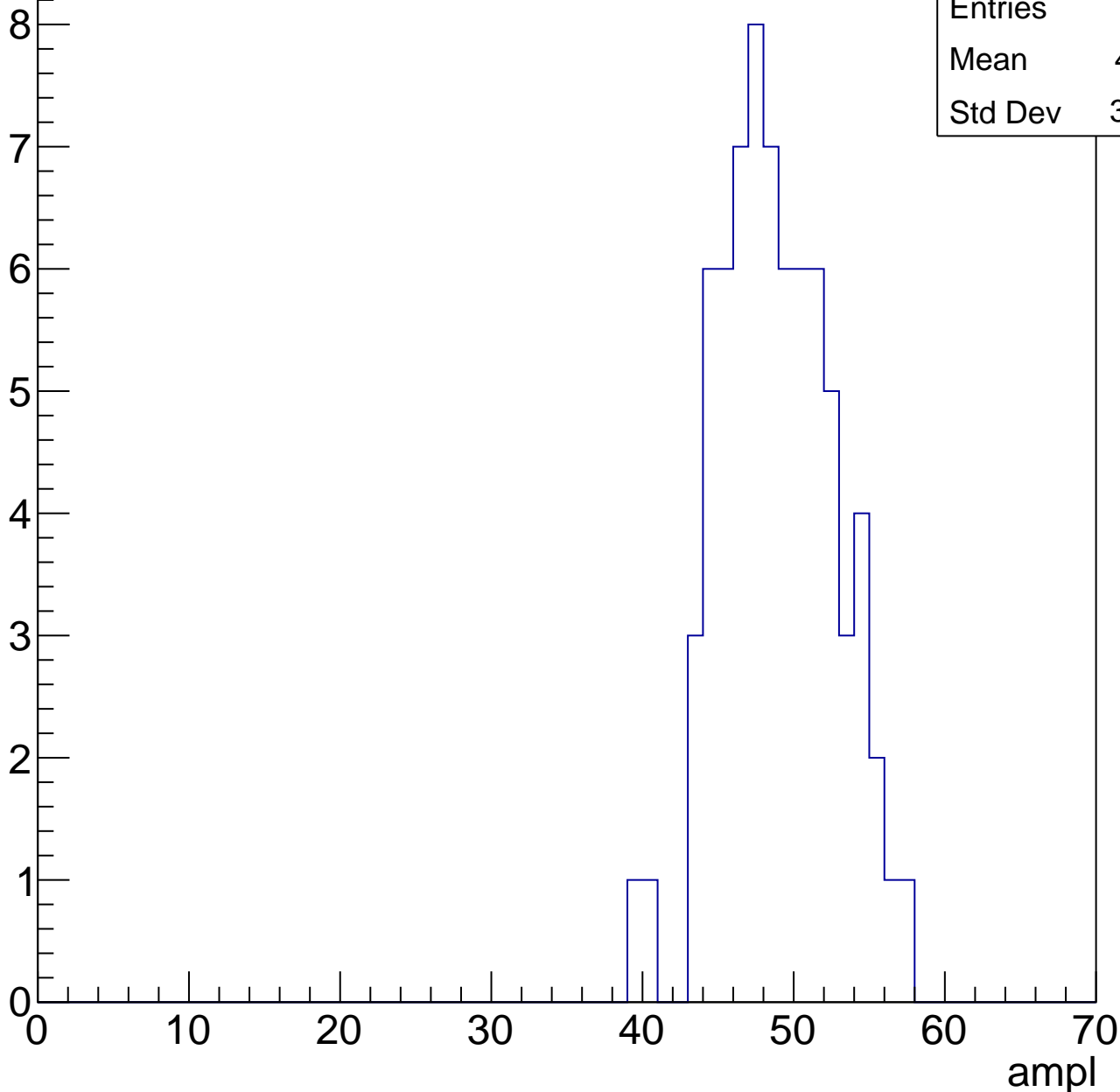


# B1L103S, U3-ch97, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

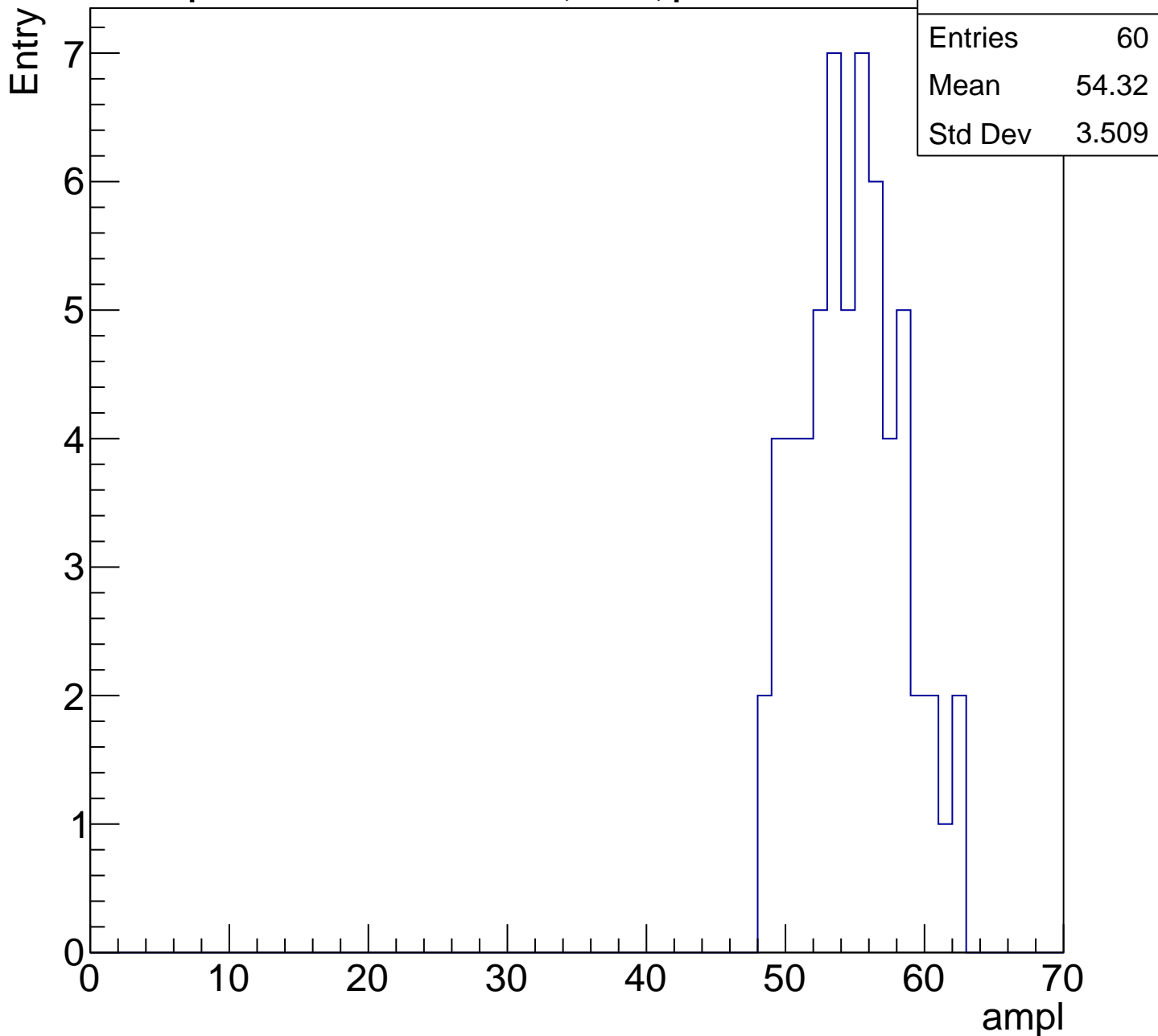
Entry

Entries	73
Mean	48.41
Std Dev	3.737



# B1L103S, U3-ch97, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

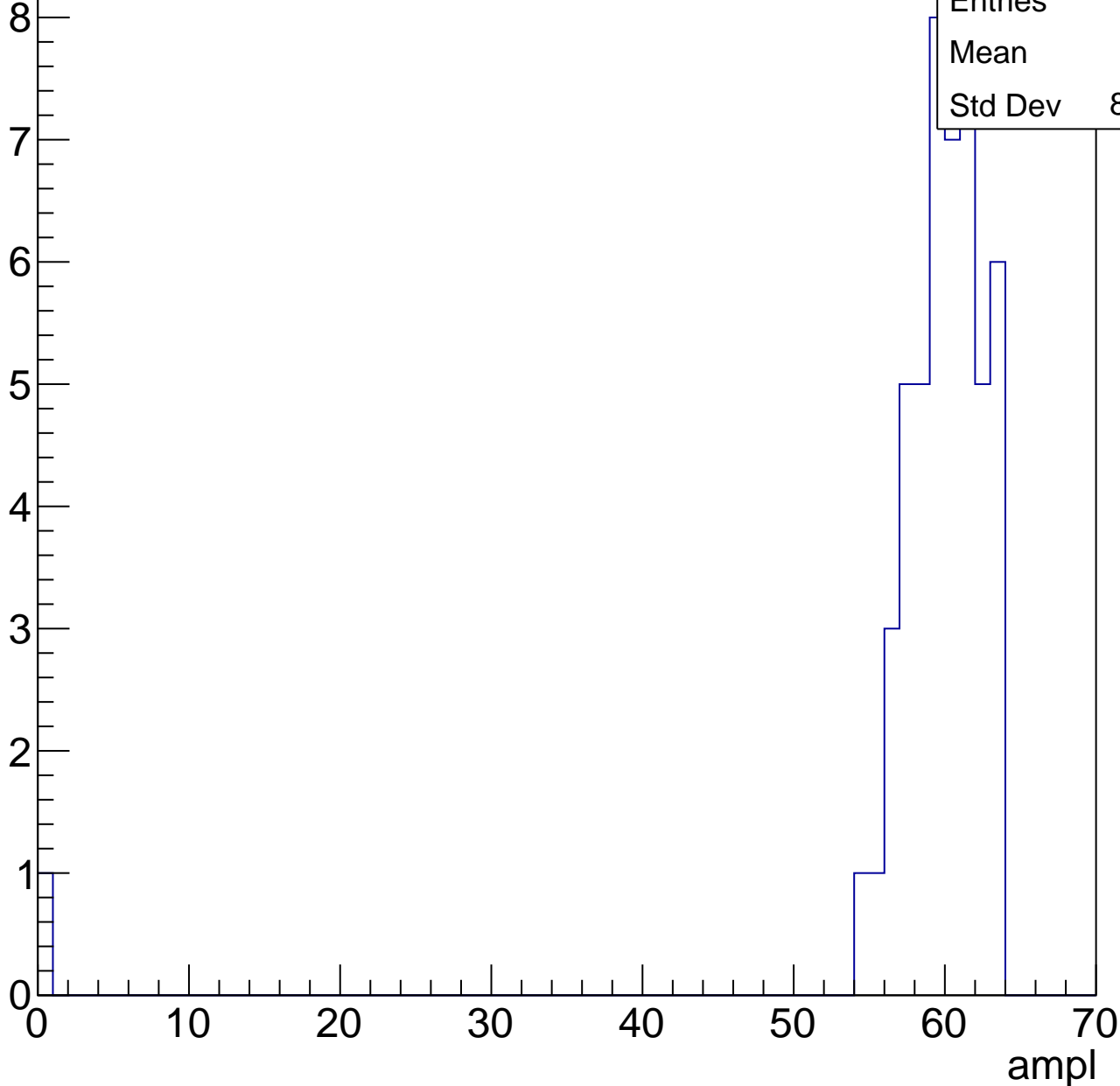


# B1L103S, U3-ch97, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	58.4
Std Dev	8.644



# B1L103S, U3-ch97, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U3-ch97, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch98, adc0

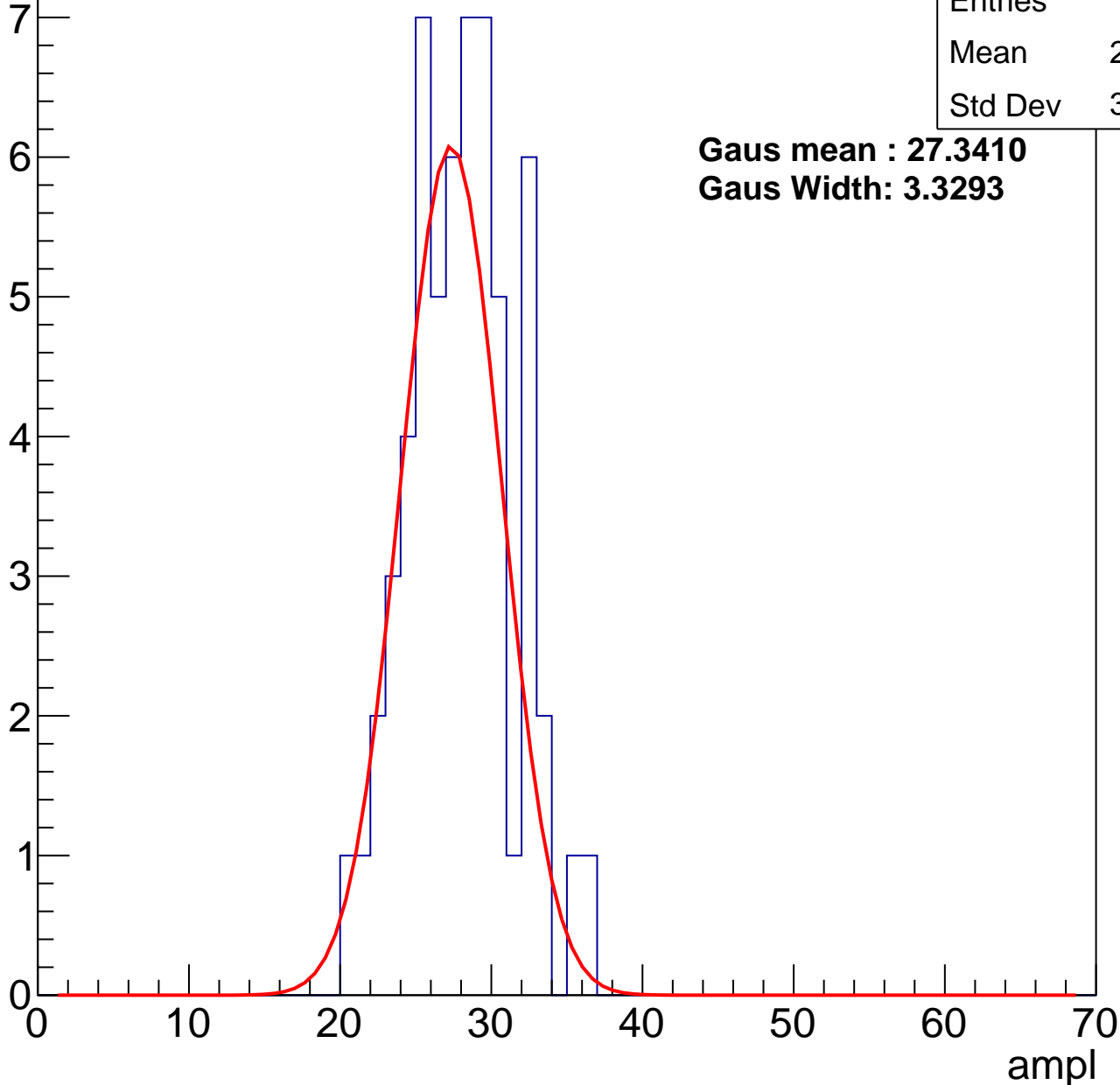
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	27.56
Std Dev	3.436

**Gaus mean : 27.3410**

**Gaus Width: 3.3293**



# B1L103S, U3-ch98, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	71
Mean	33.03
Std Dev	5.451

**Gaus mean : 34.5005**

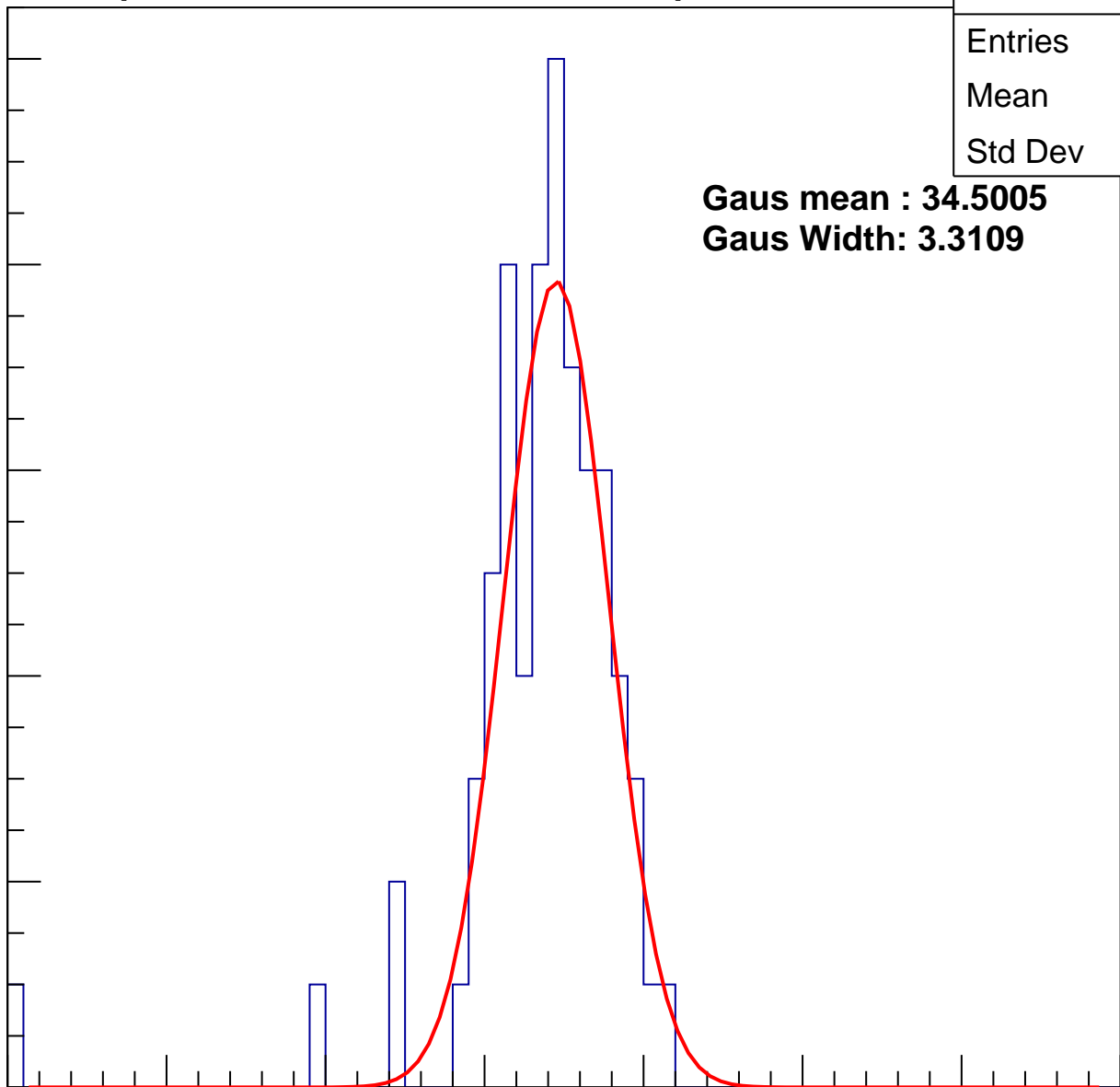
**Gaus Width: 3.3109**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U3-ch98, adc2

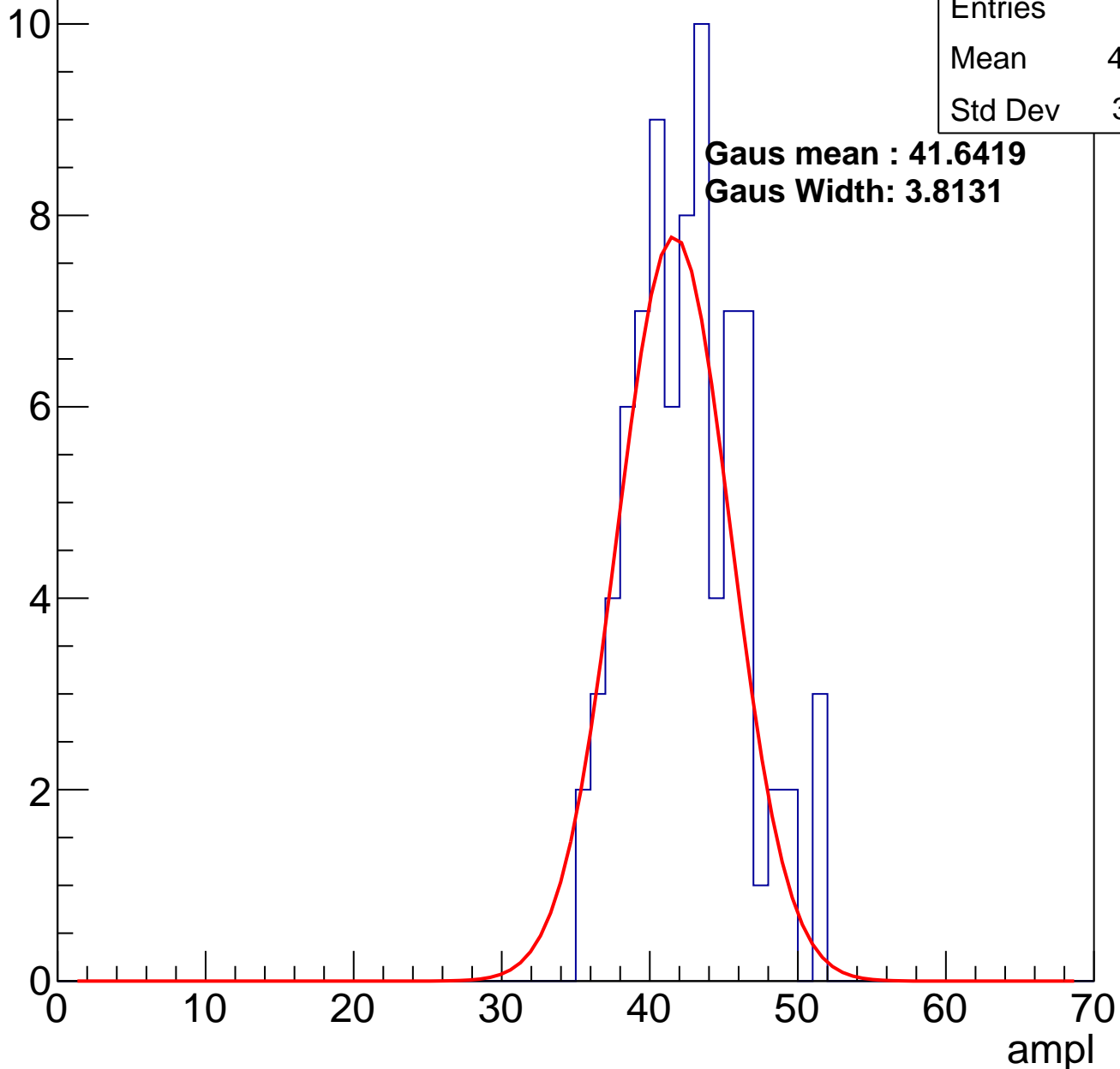
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	81
Mean	42.05
Std Dev	3.761

**Gaus mean : 41.6419**

**Gaus Width: 3.8131**

Entry

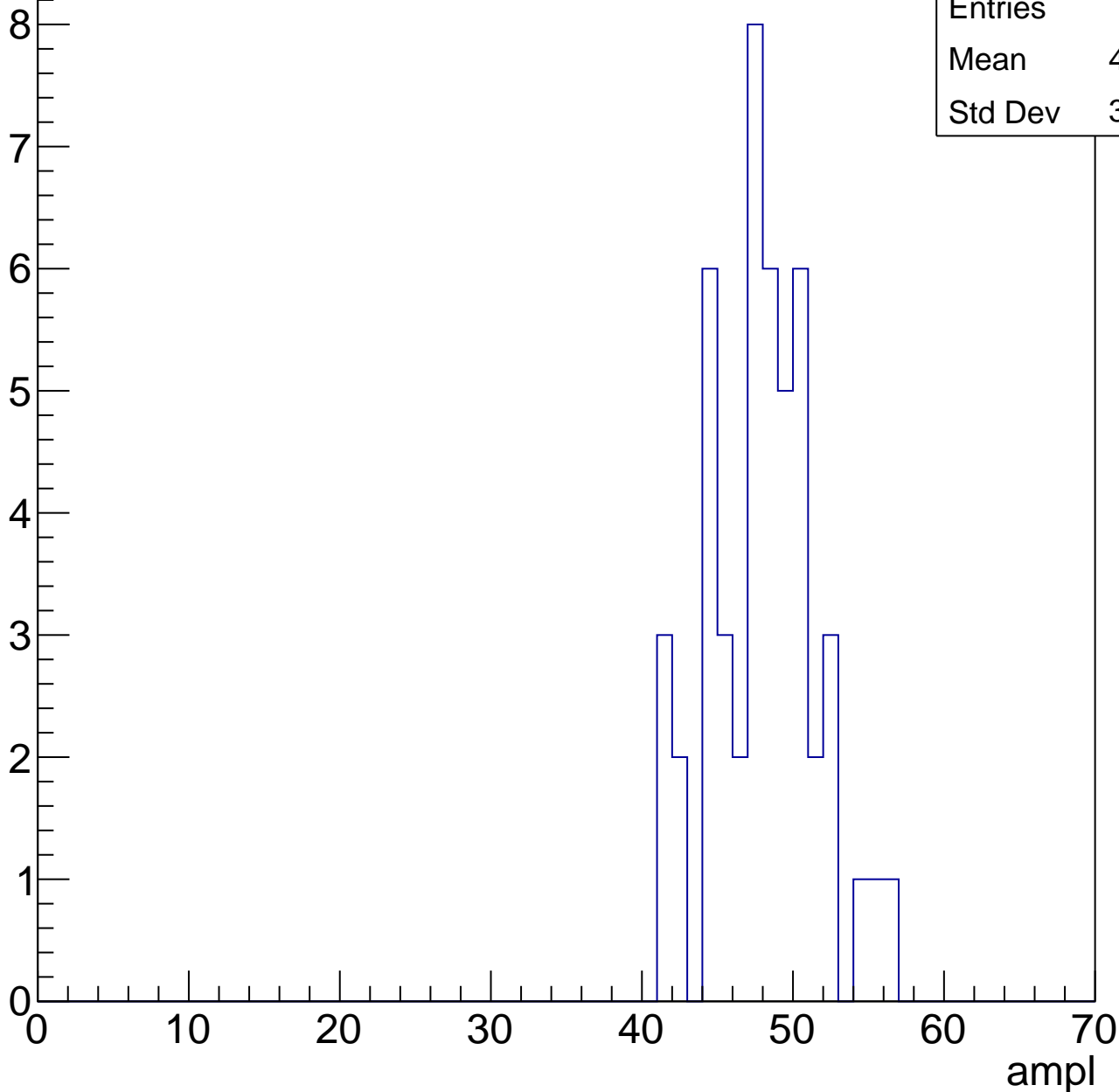


# B1L103S, U3-ch98, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	47.55
Std Dev	3.476

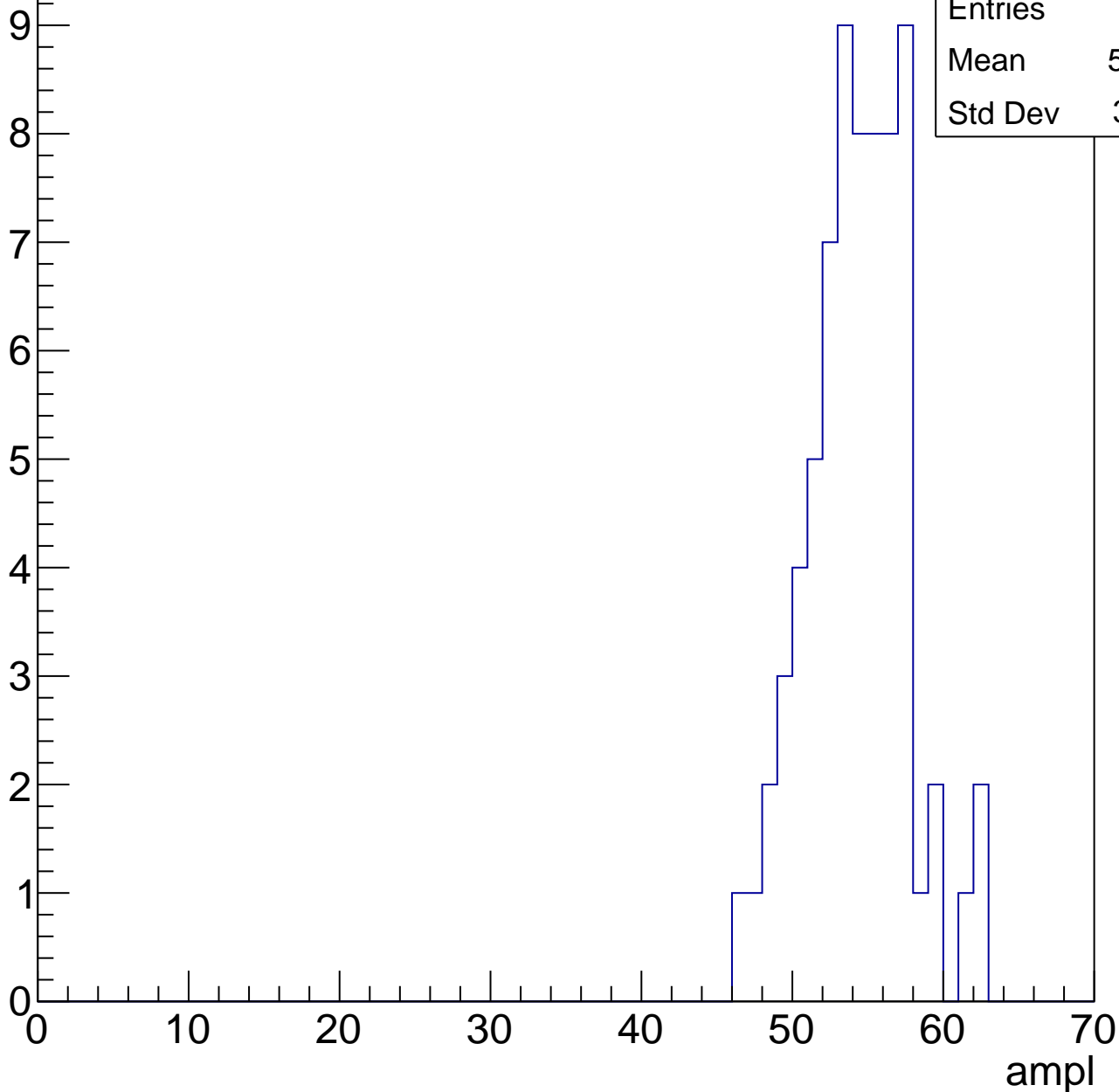


# B1L103S, U3-ch98, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	53.89
Std Dev	3.291



# B1L103S, U3-ch98, adc5

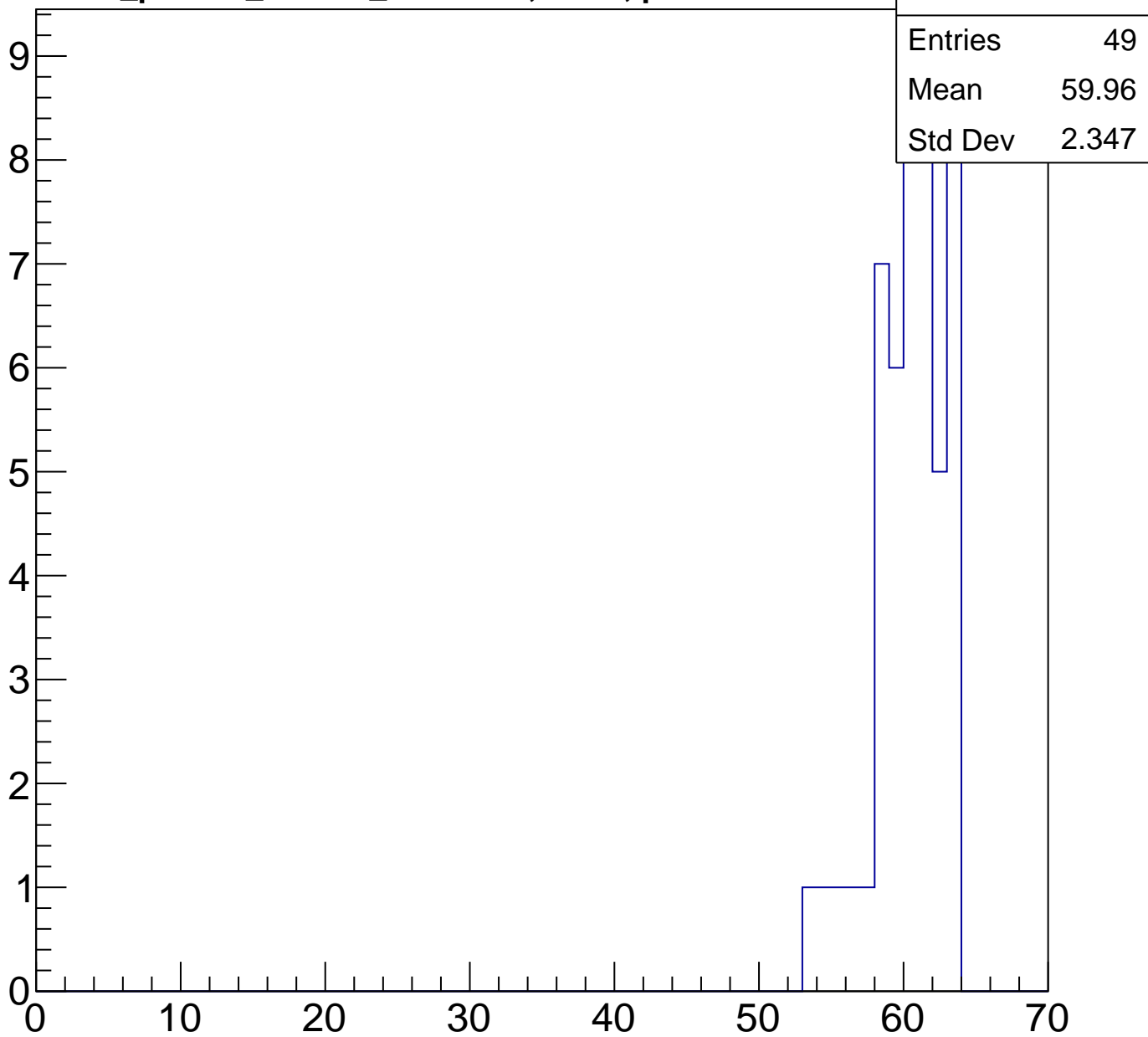
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	49
Mean	59.96
Std Dev	2.347

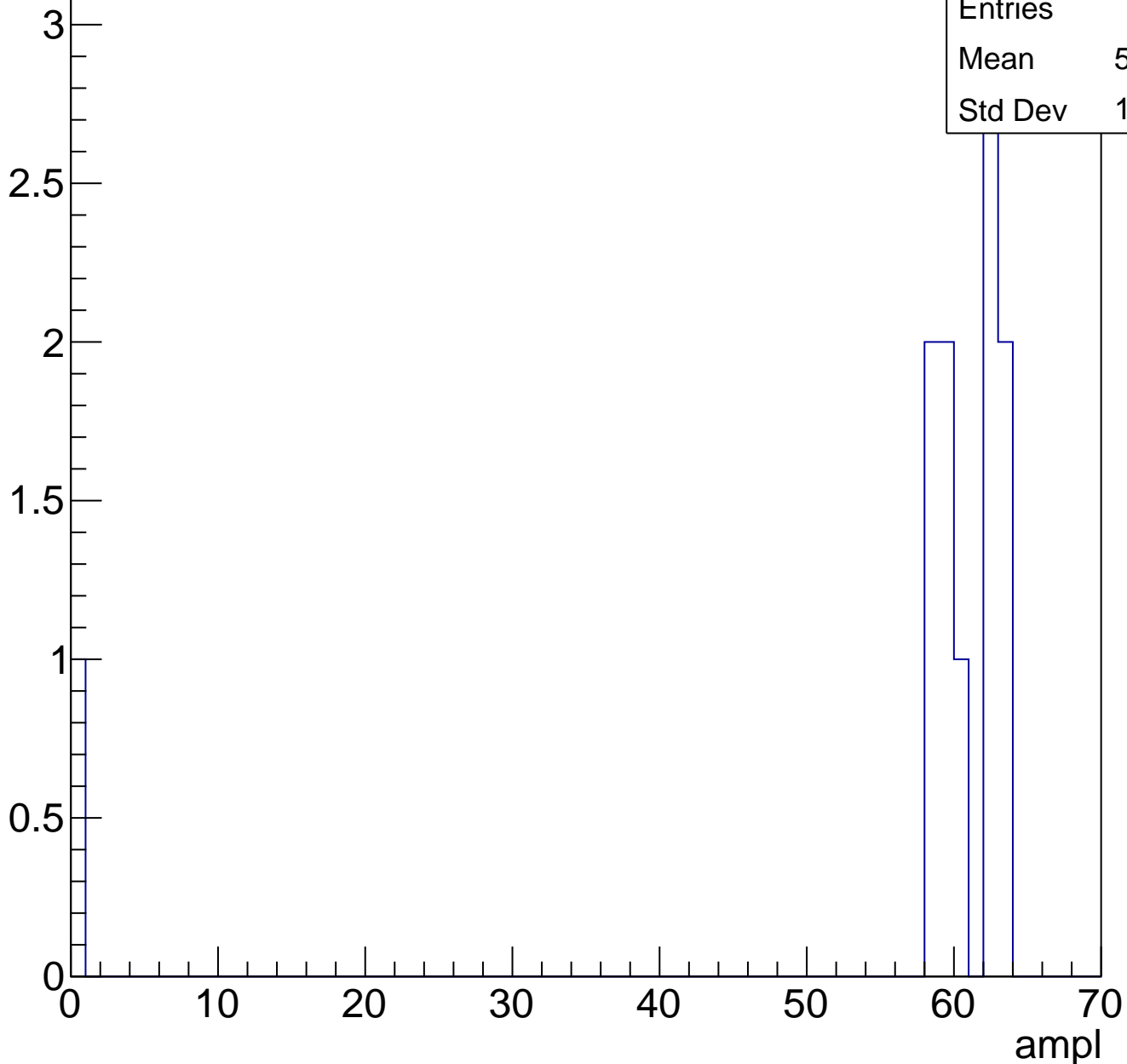
ampl



# B1L103S, U3-ch98, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U3-ch98, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch99, adc0

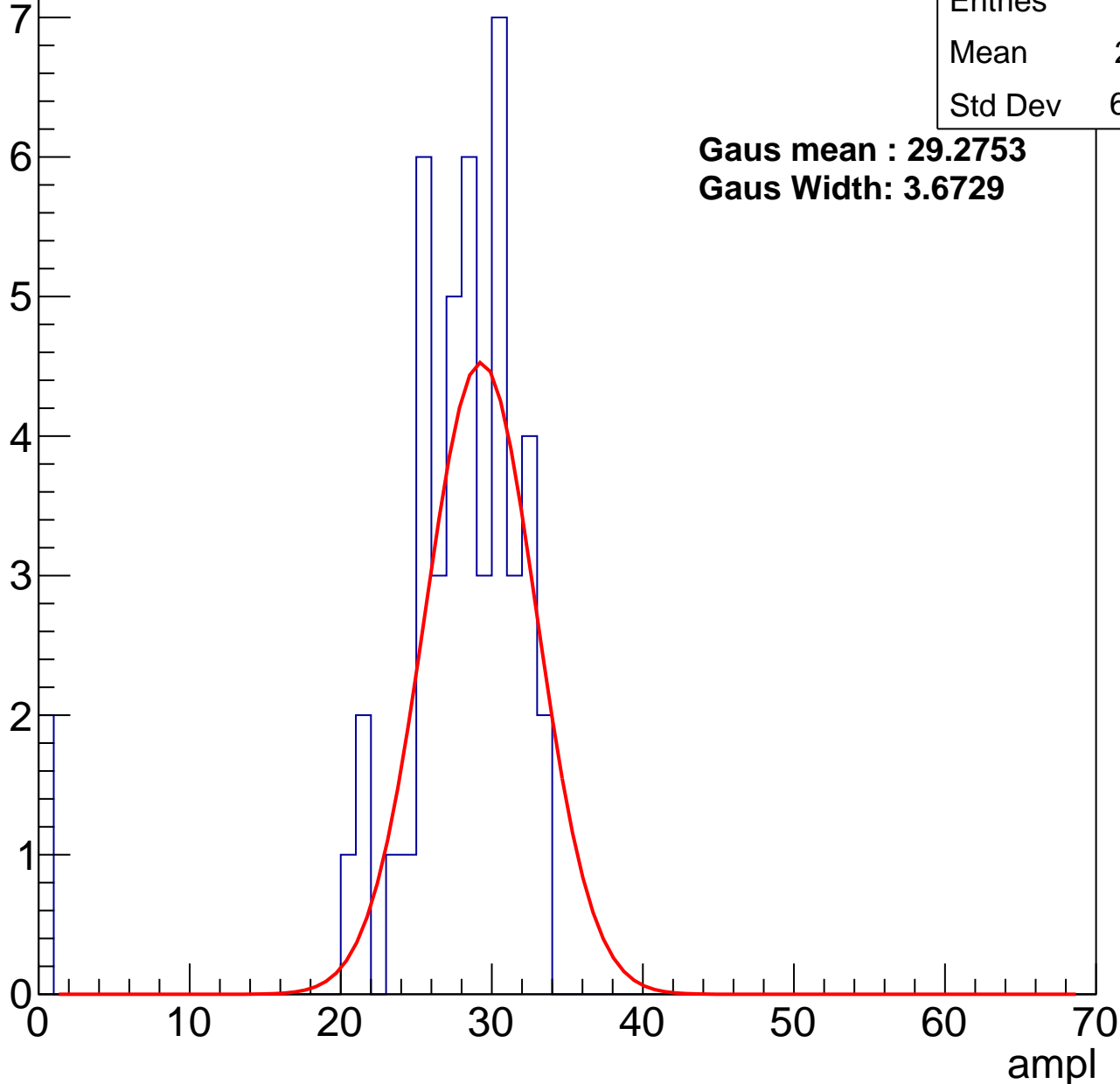
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	46
Mean	26.61
Std Dev	6.469

**Gaus mean : 29.2753**

**Gaus Width: 3.6729**



# B1L103S, U3-ch99, adc1

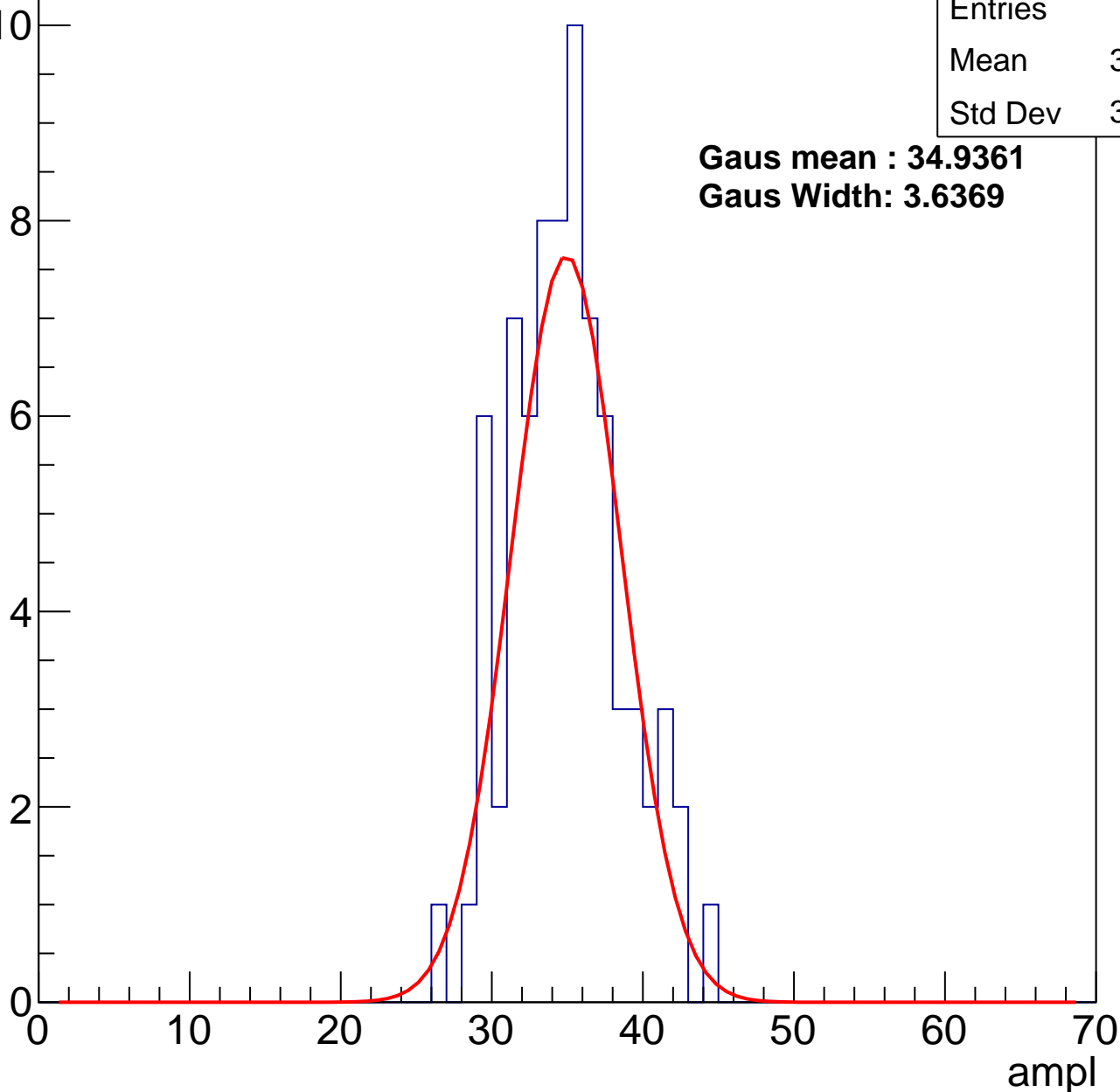
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	34.46
Std Dev	3.669

**Gaus mean : 34.9361**

**Gaus Width: 3.6369**



# B1L103S, U3-ch99, adc2

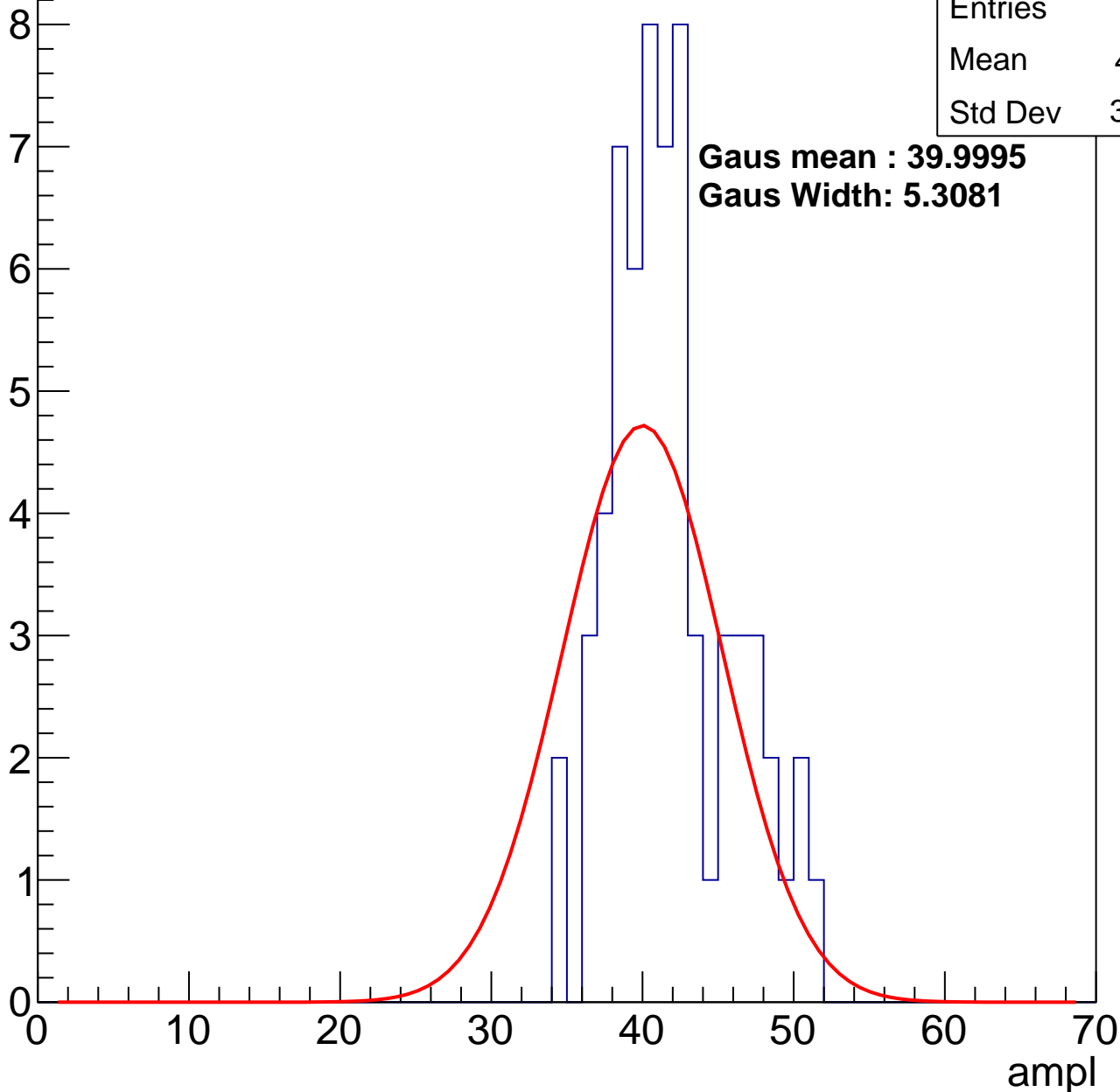
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	41.41
Std Dev	3.964

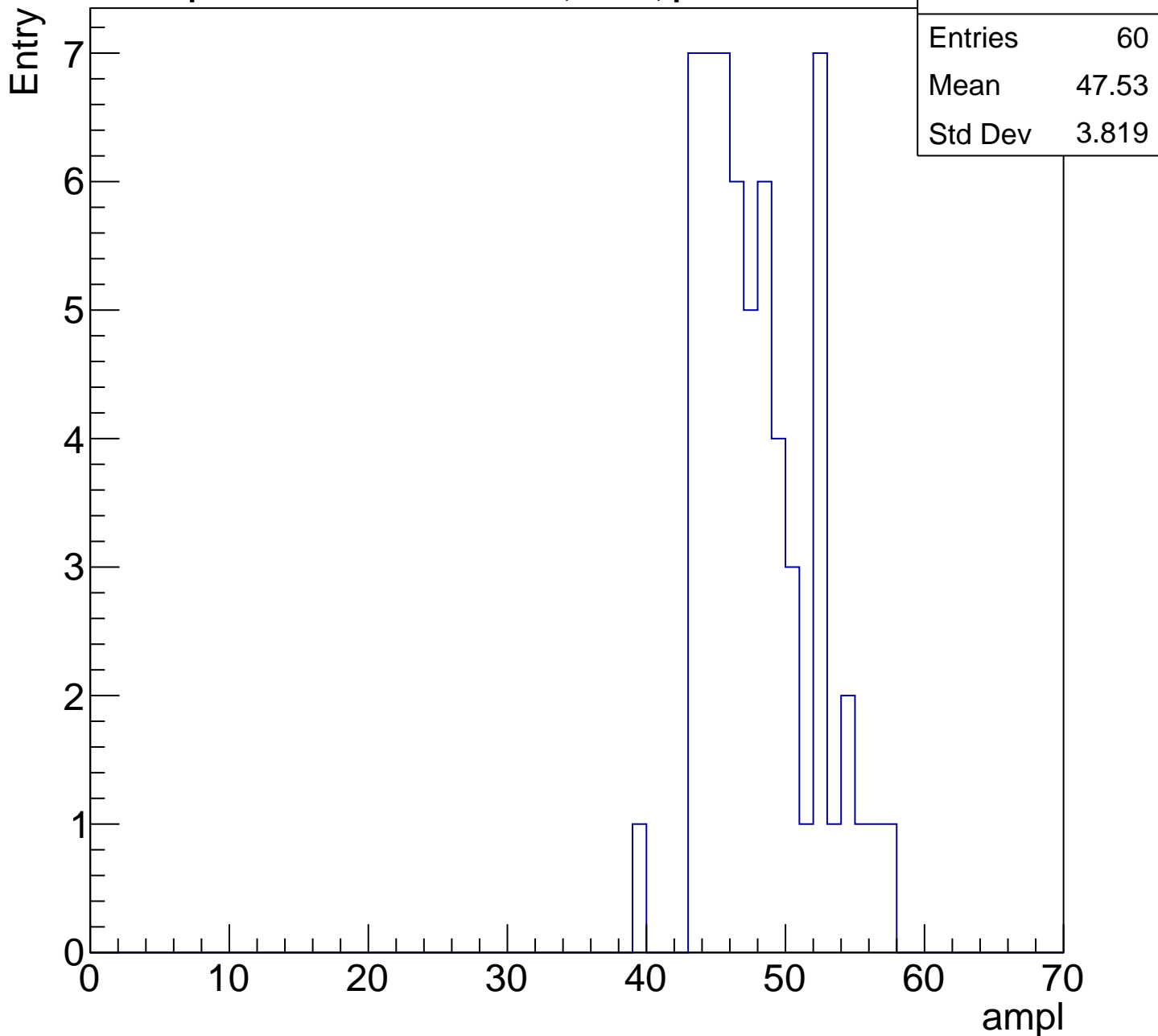
**Gaus mean : 39.9995**

**Gaus Width: 5.3081**



# B1L103S, U3-ch99, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

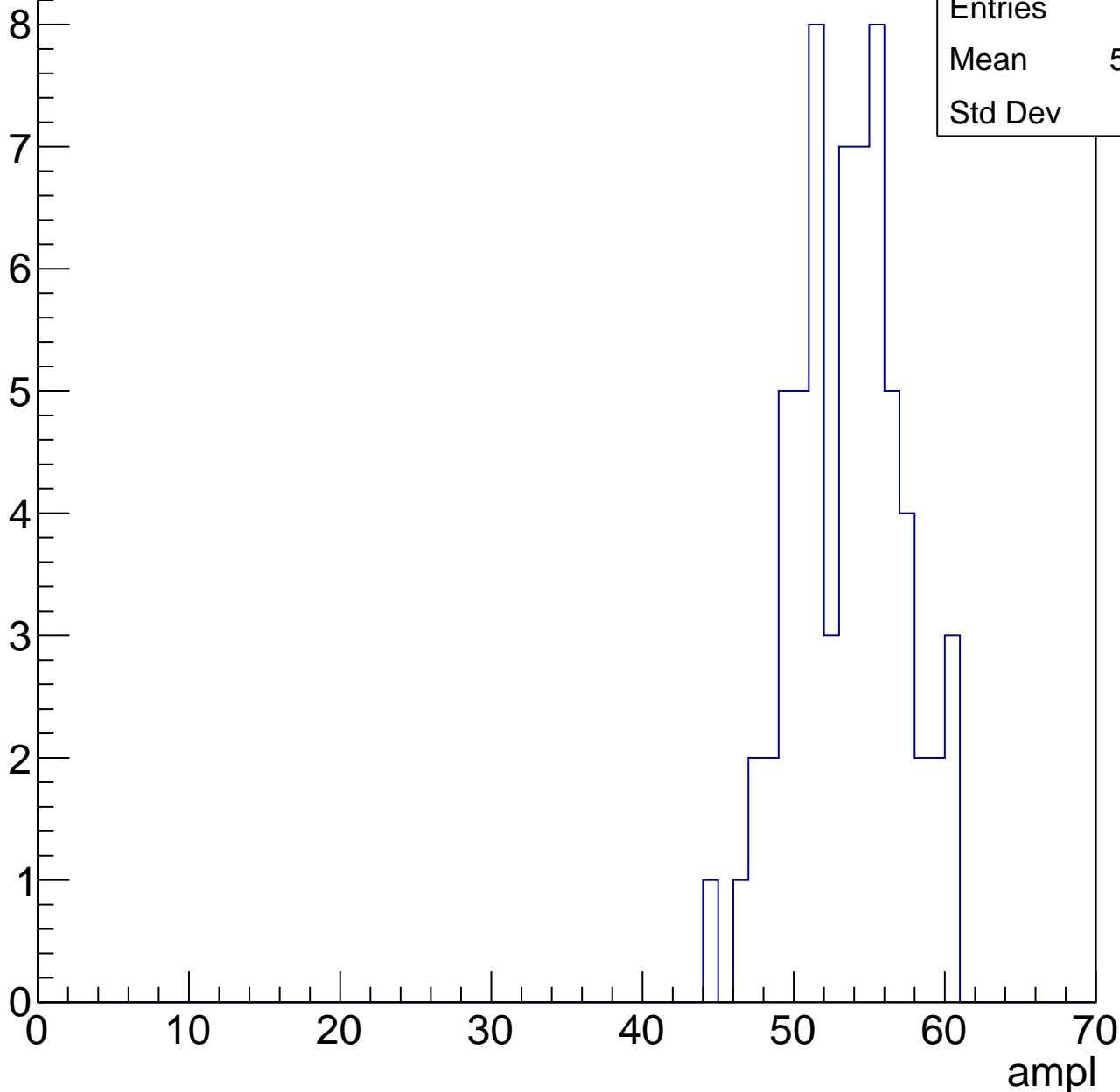


# B1L103S, U3-ch99, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	53.08
Std Dev	3.57



# B1L103S, U3-ch99, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

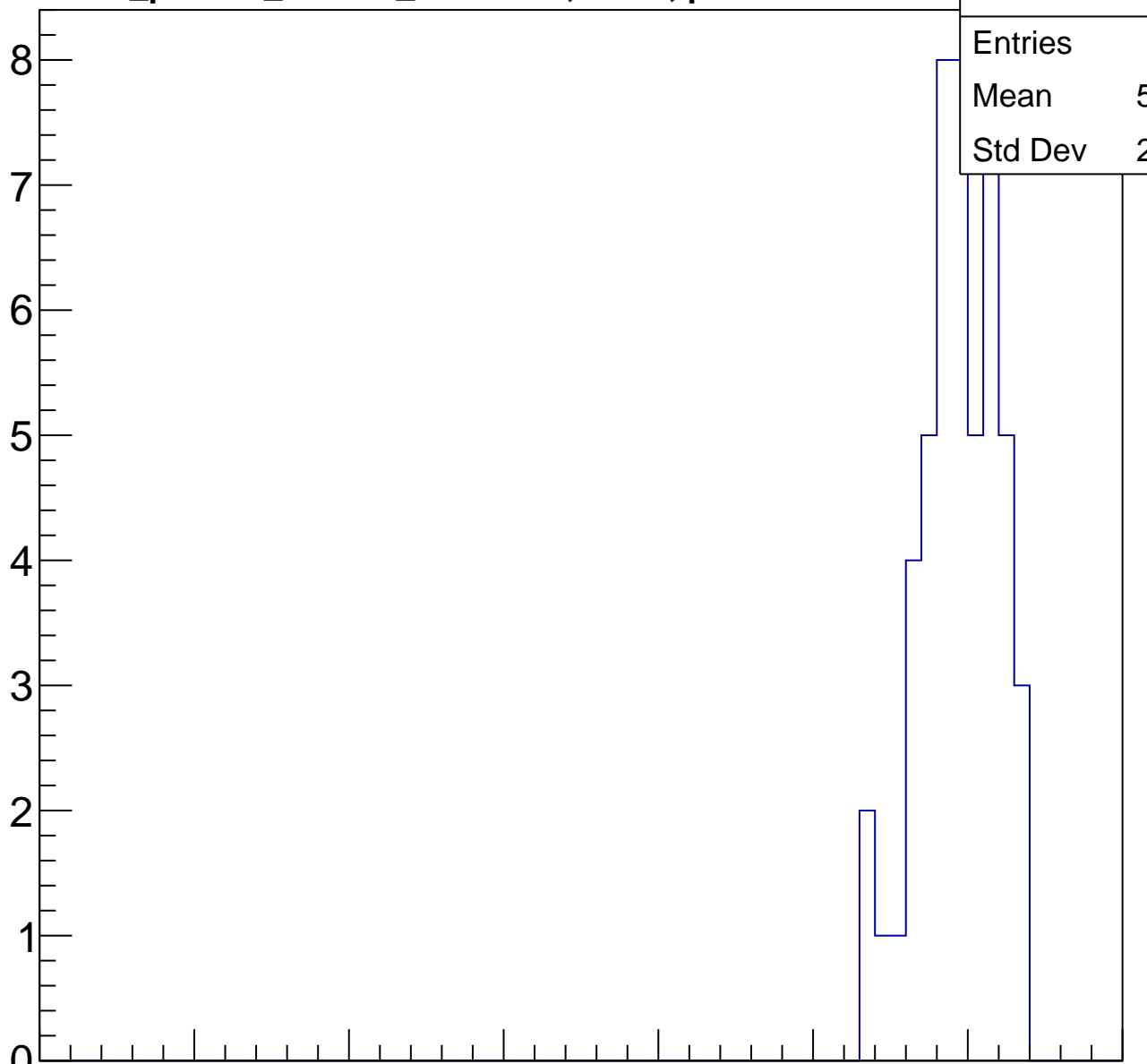
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	50
Mean	58.94
Std Dev	2.477

ampl

0 10 20 30 40 50 60 70

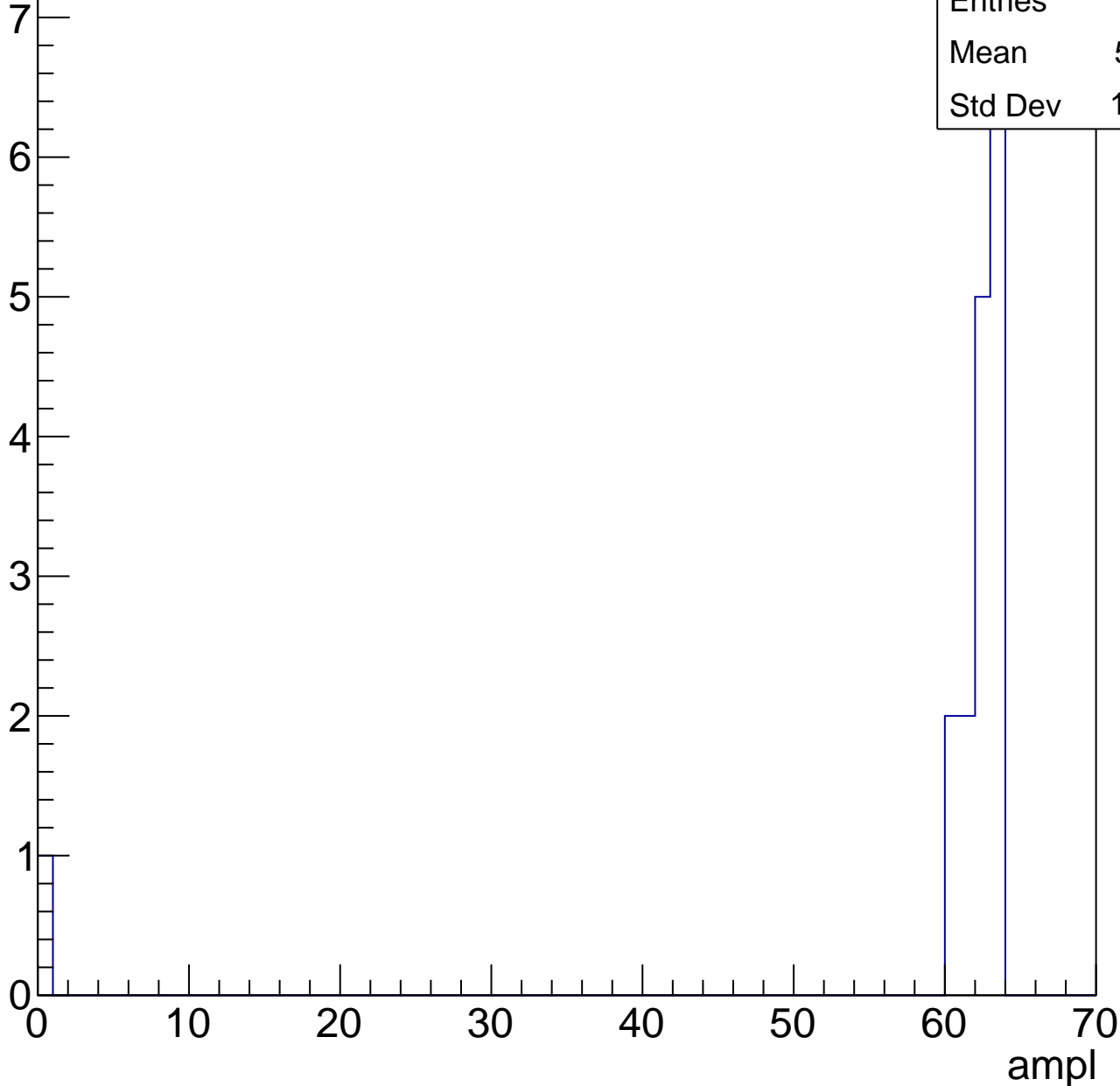


# B1L103S, U3-ch99, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	17
Mean	58.41
Std Dev	14.64





# B1L103S, U3-ch99, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U3-ch100, adc0

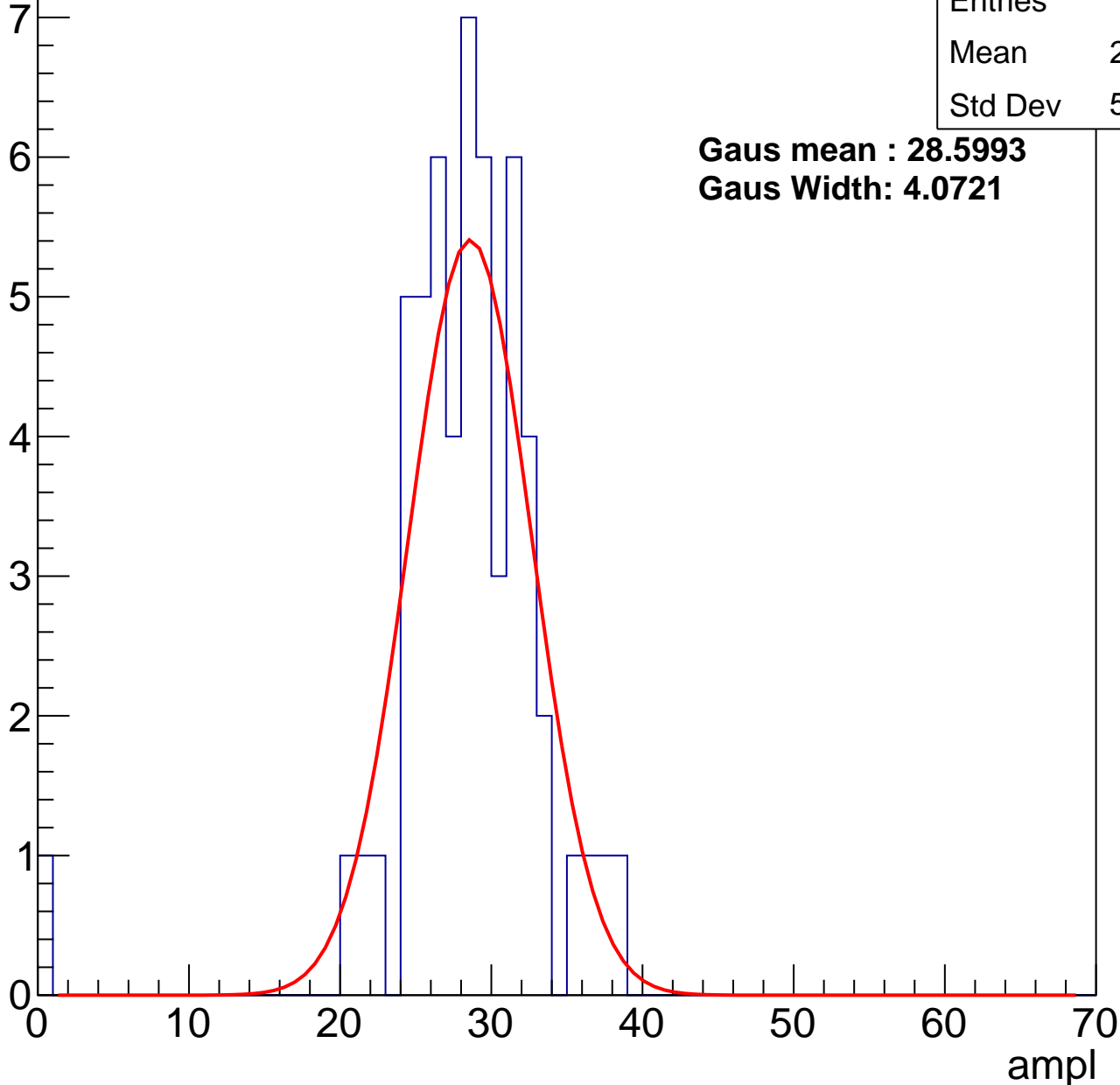
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	27.82
Std Dev	5.285

**Gaus mean : 28.5993**

**Gaus Width: 4.0721**



# B1L103S, U3-ch100, adc1

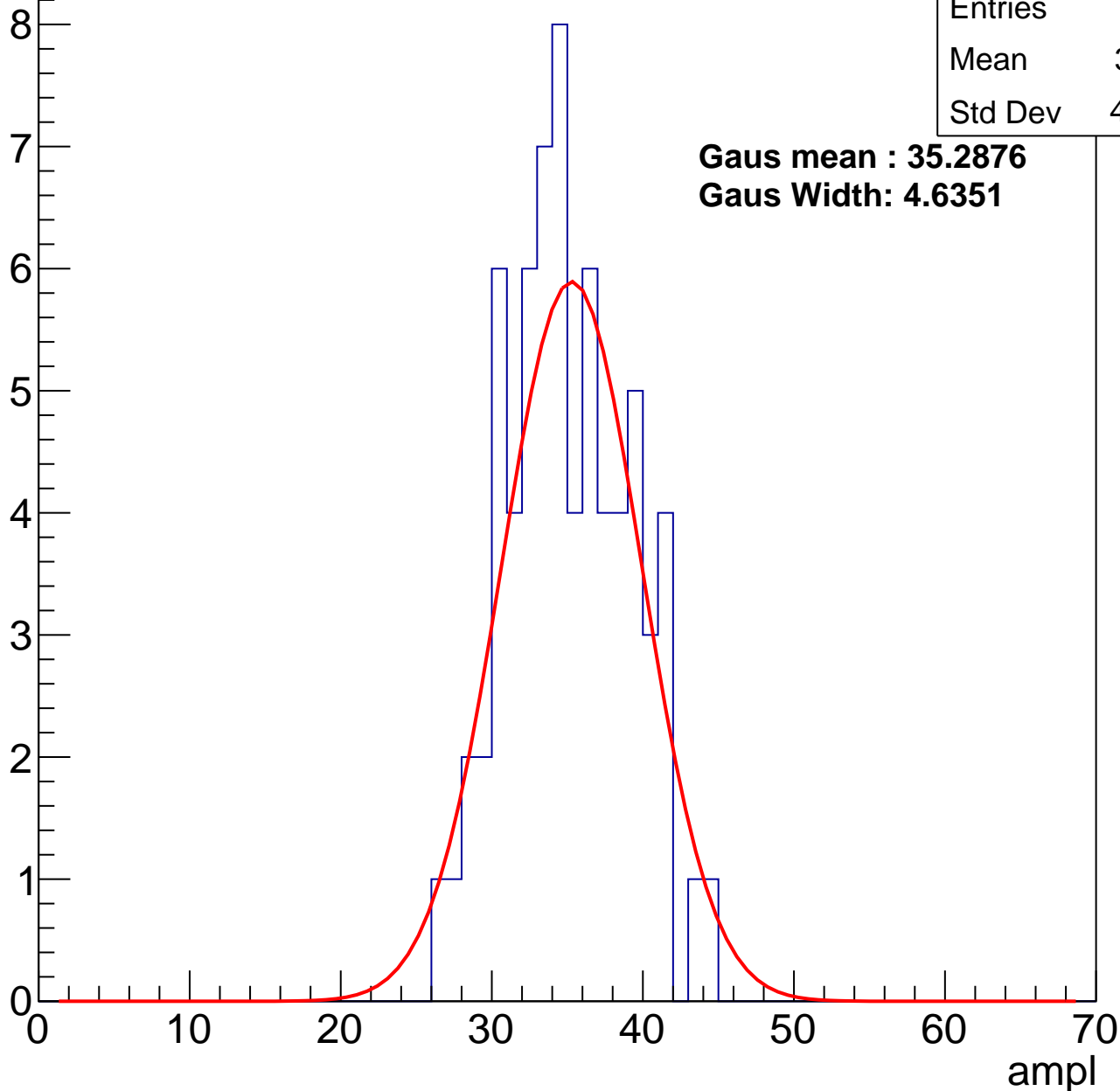
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	34.61
Std Dev	4.012

**Gaus mean : 35.2876**

**Gaus Width: 4.6351**



# B1L103S, U3-ch100, adc2

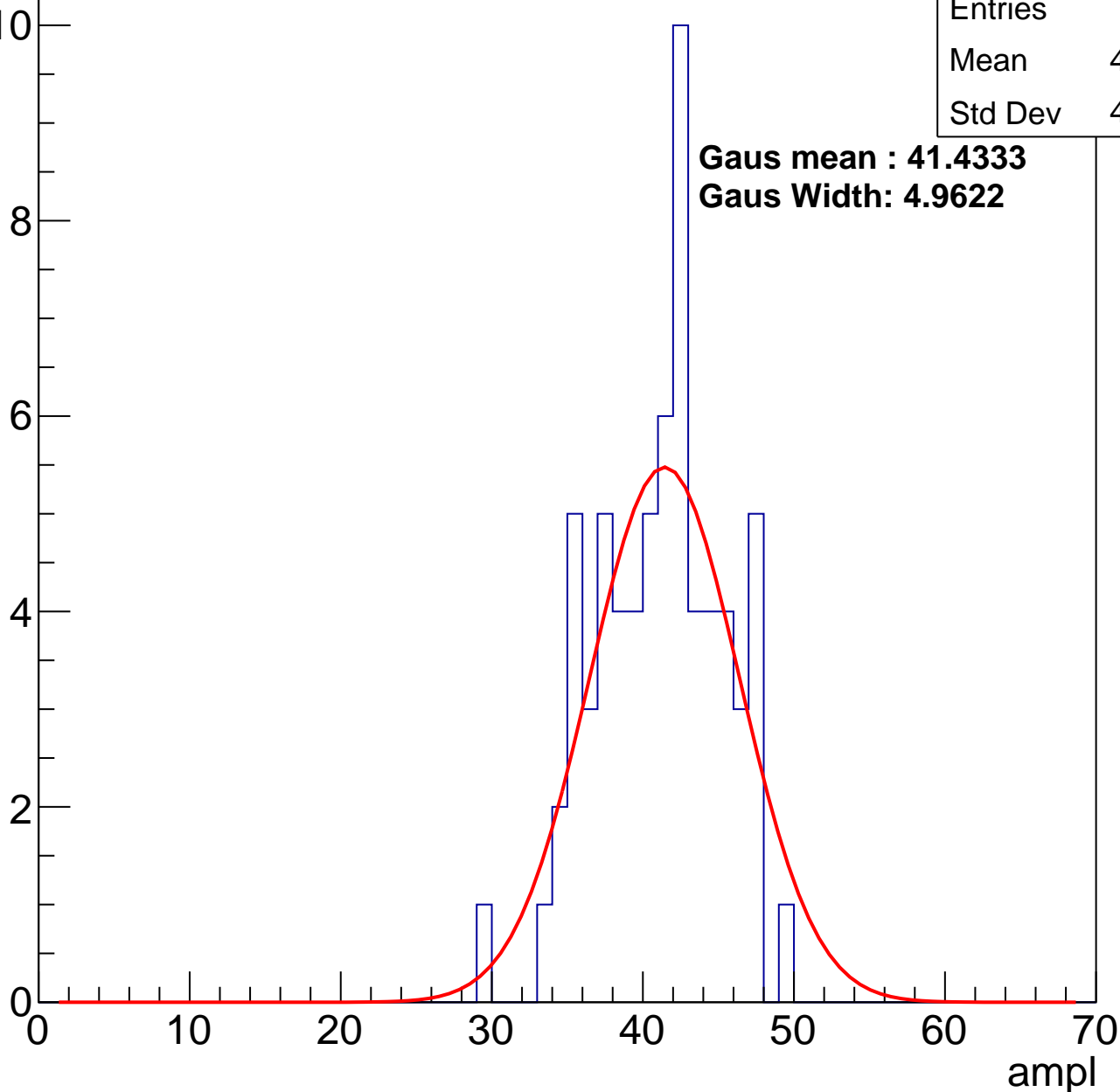
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	40.63
Std Dev	4.113

**Gaus mean : 41.4333**

**Gaus Width: 4.9622**

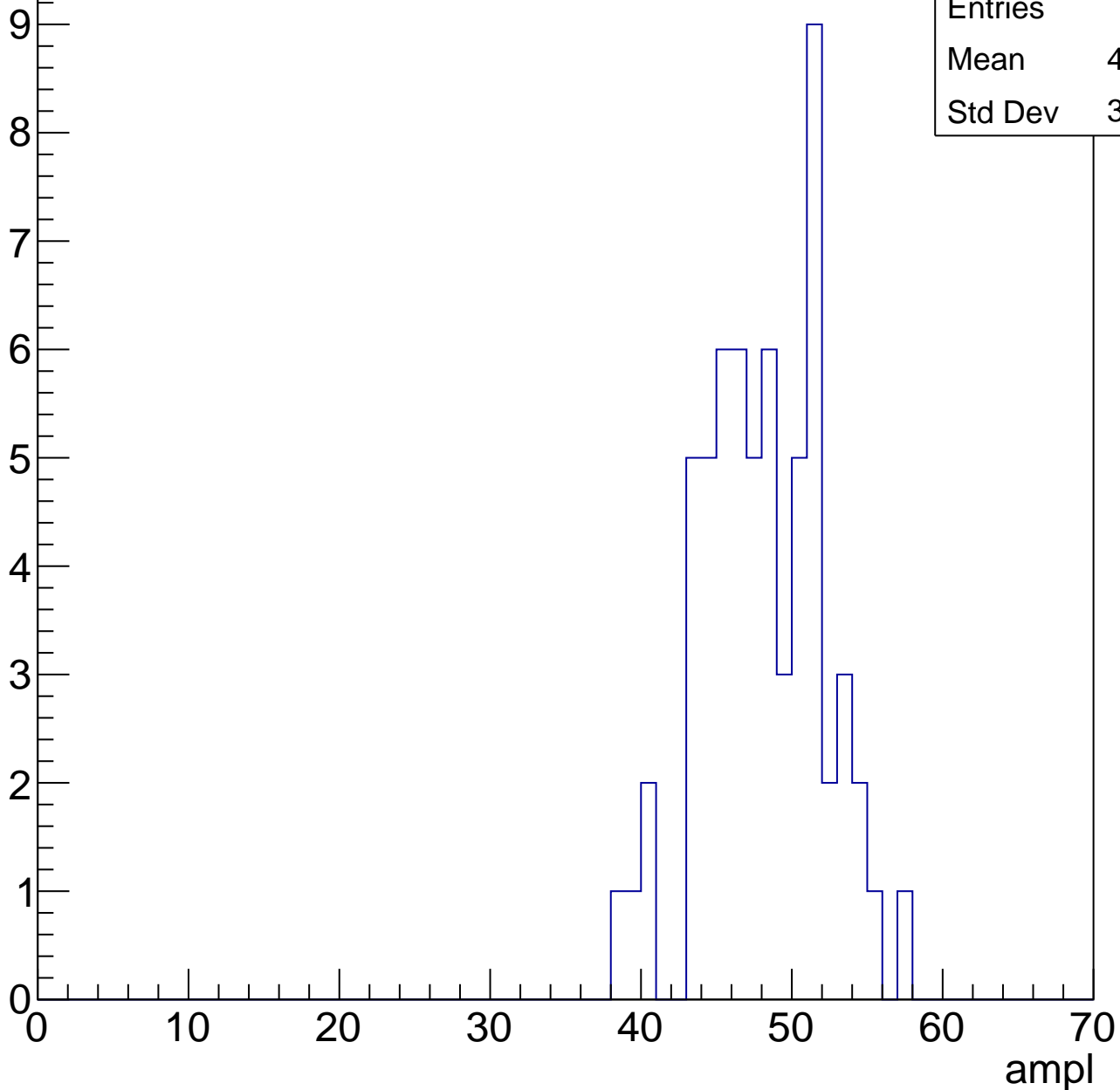


# B1L103S, U3-ch100, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	47.62
Std Dev	3.986

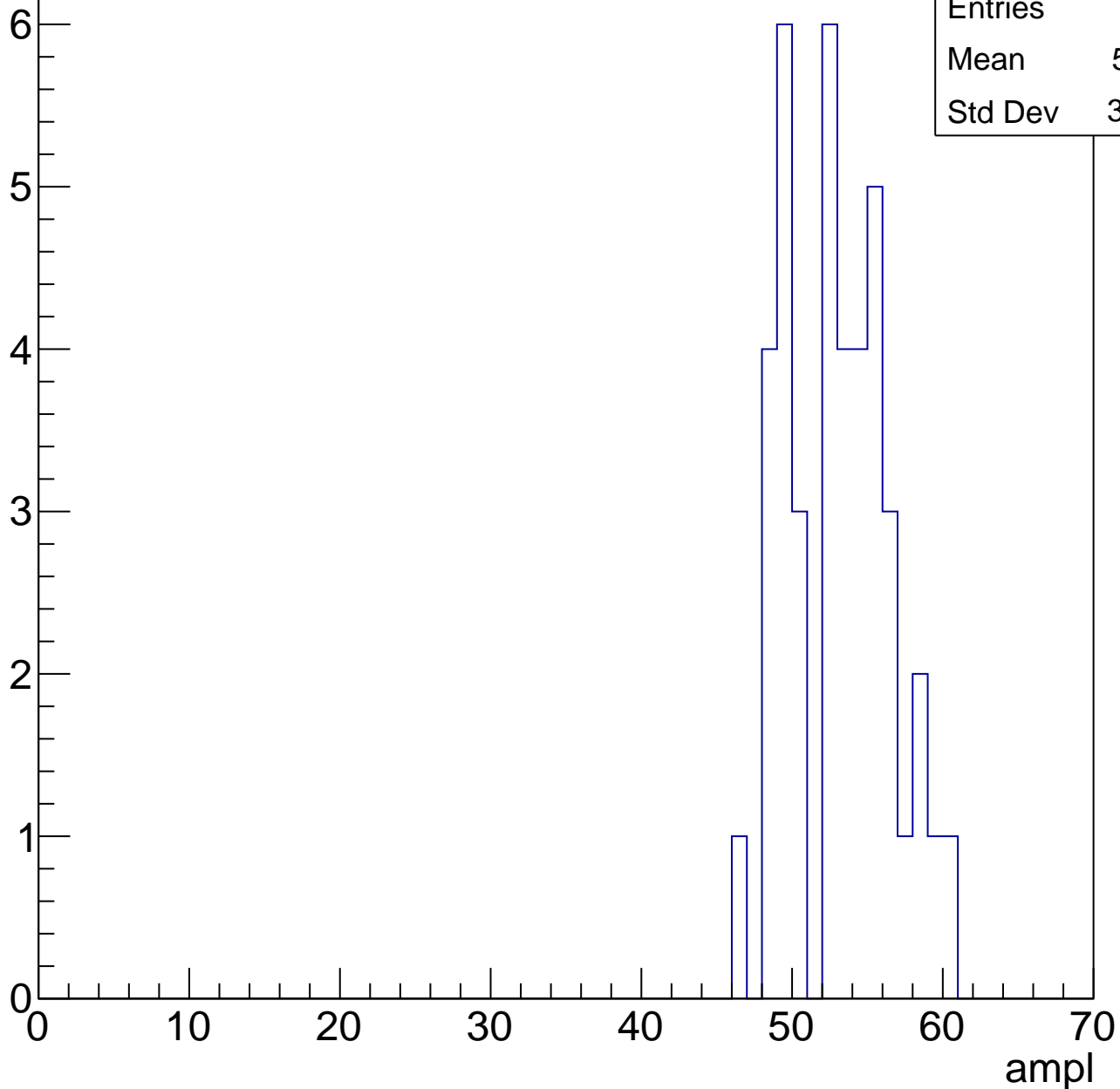


# B1L103S, U3-ch100, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

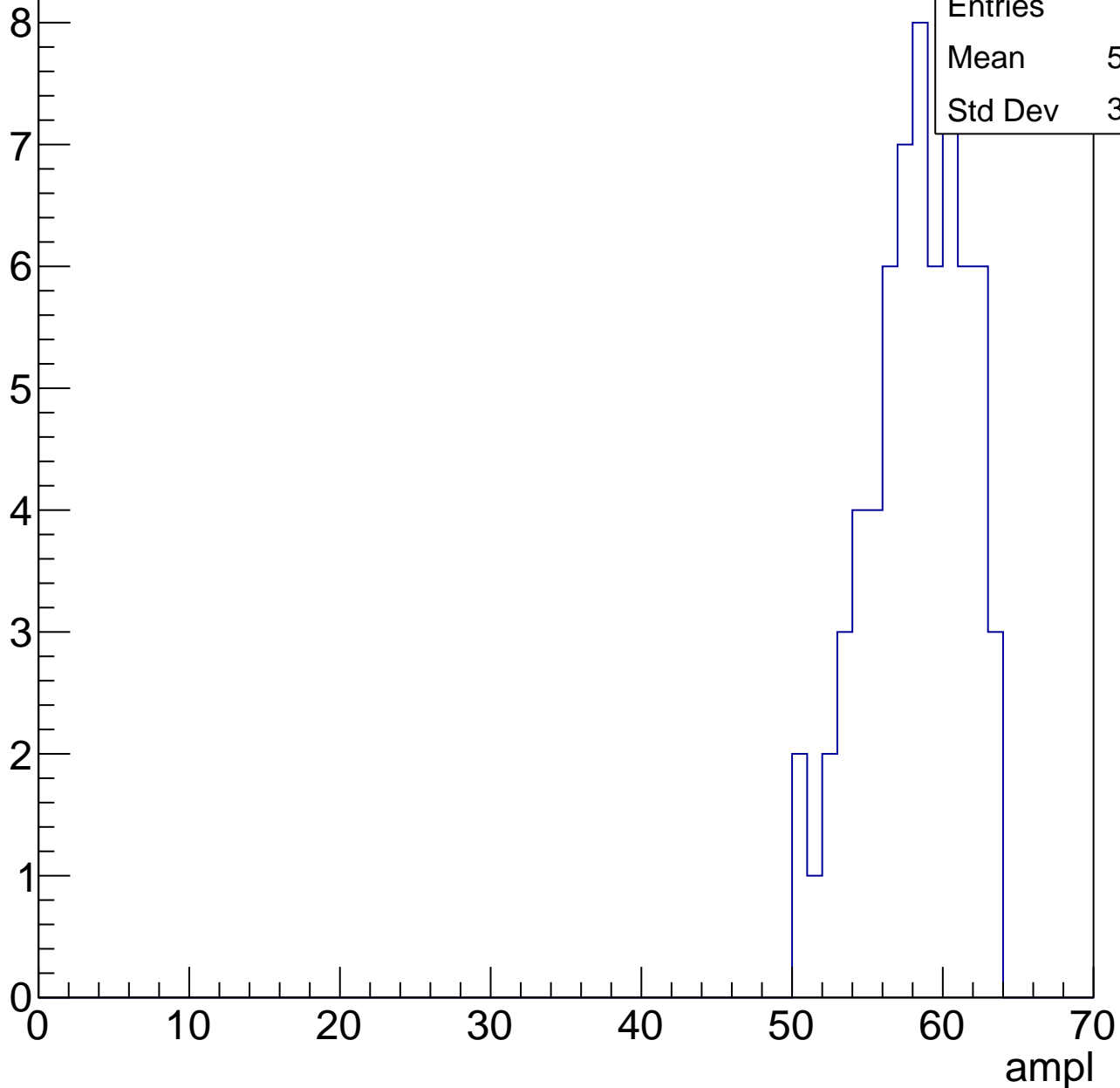
Entries	41
Mean	52.61
Std Dev	3.399



# B1L103S, U3-ch100, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



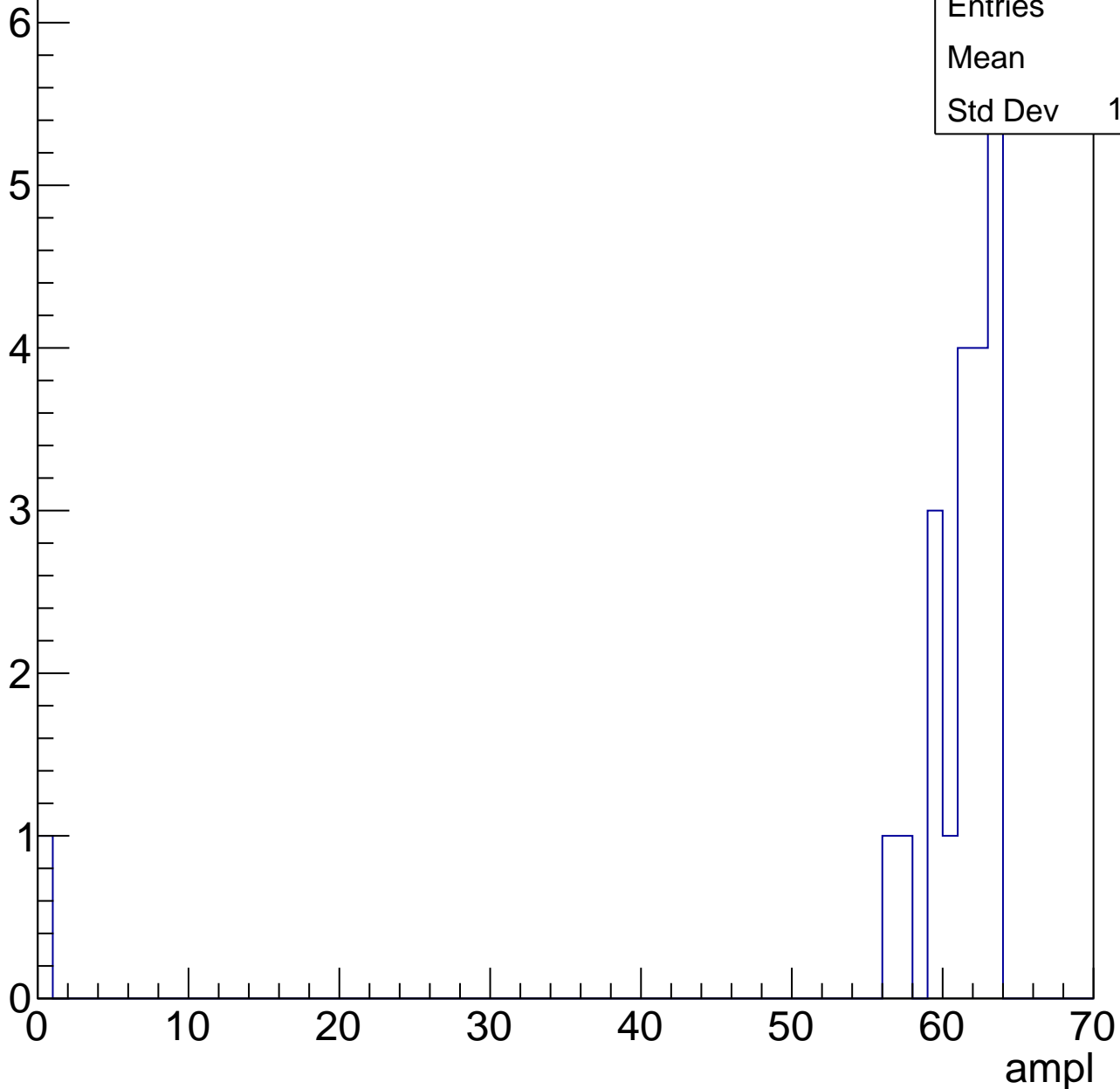
Entries	66
Mean	57.73
Std Dev	3.287

# B1L103S, U3-ch100, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	21
Mean	58.1
Std Dev	13.14





# B1L103S, U3-ch100, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch101, adc0

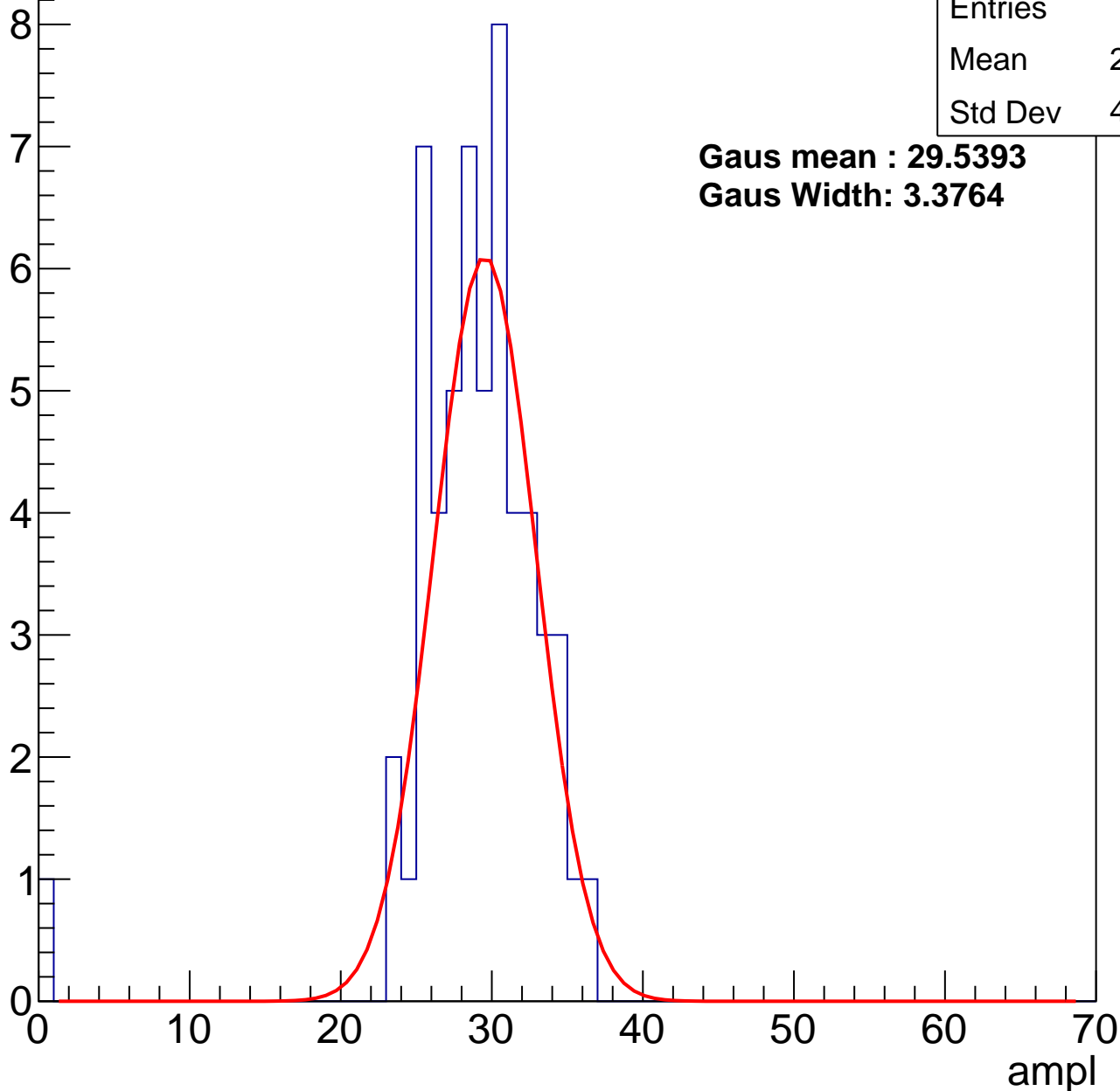
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	28.38
Std Dev	4.926

**Gaus mean : 29.5393**

**Gaus Width: 3.3764**



# B1L103S, U3-ch101, adc1

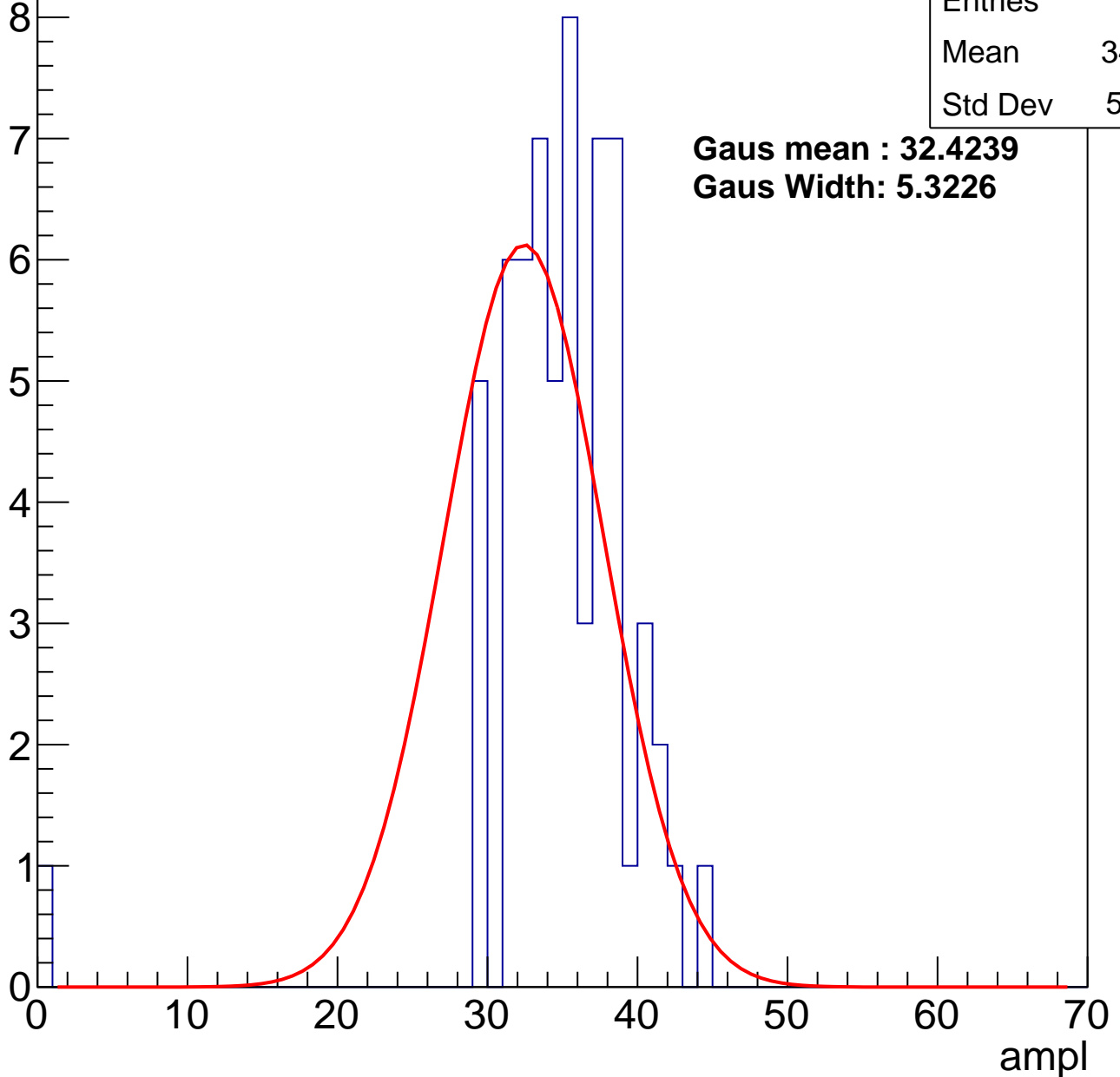
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	34.35
Std Dev	5.561

**Gaus mean : 32.4239**

**Gaus Width: 5.3226**



# B1L103S, U3-ch101, adc2

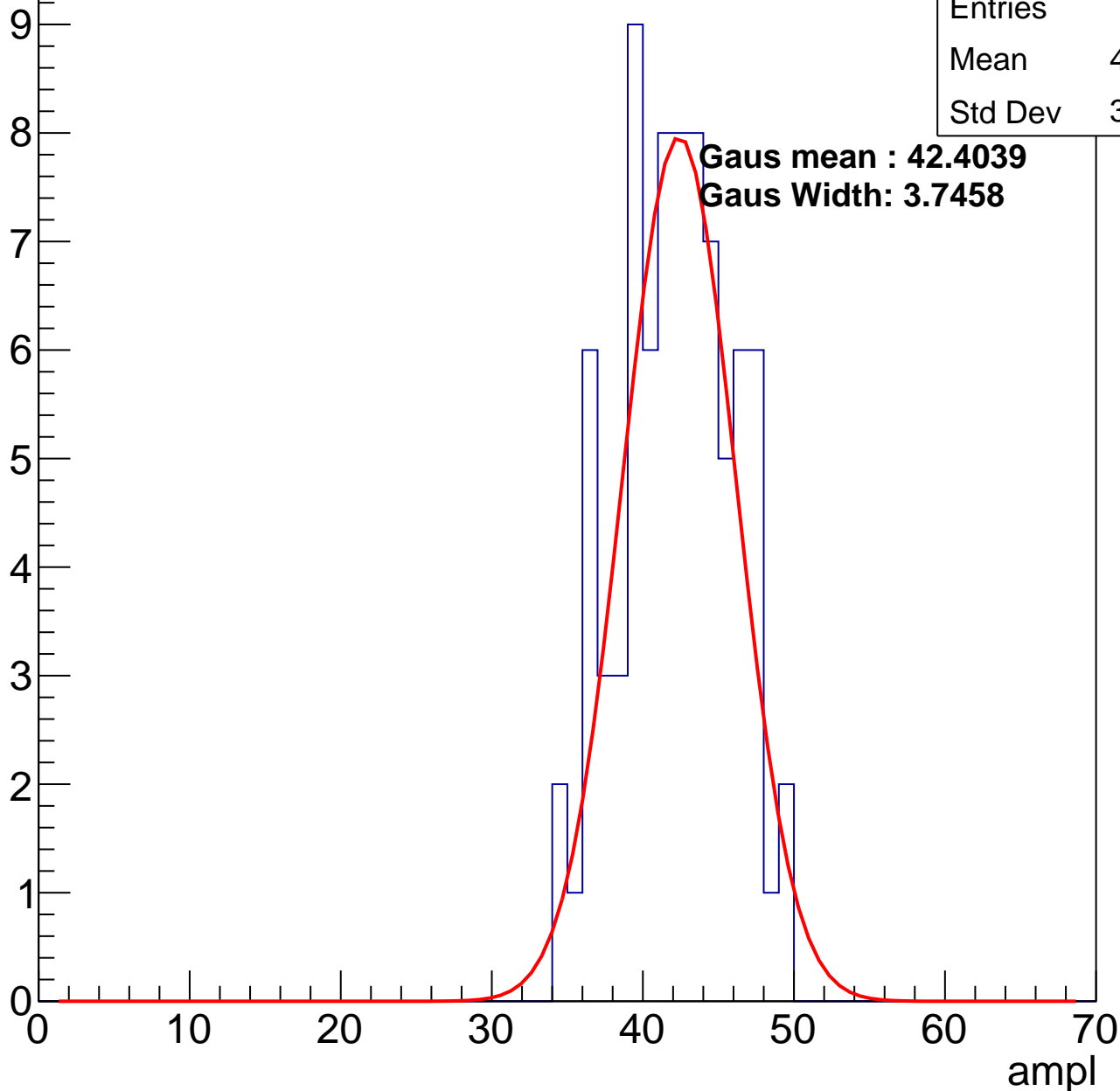
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	81
Mean	41.73
Std Dev	3.658

**Gaus mean : 42.4039**

**Gaus Width: 3.7458**

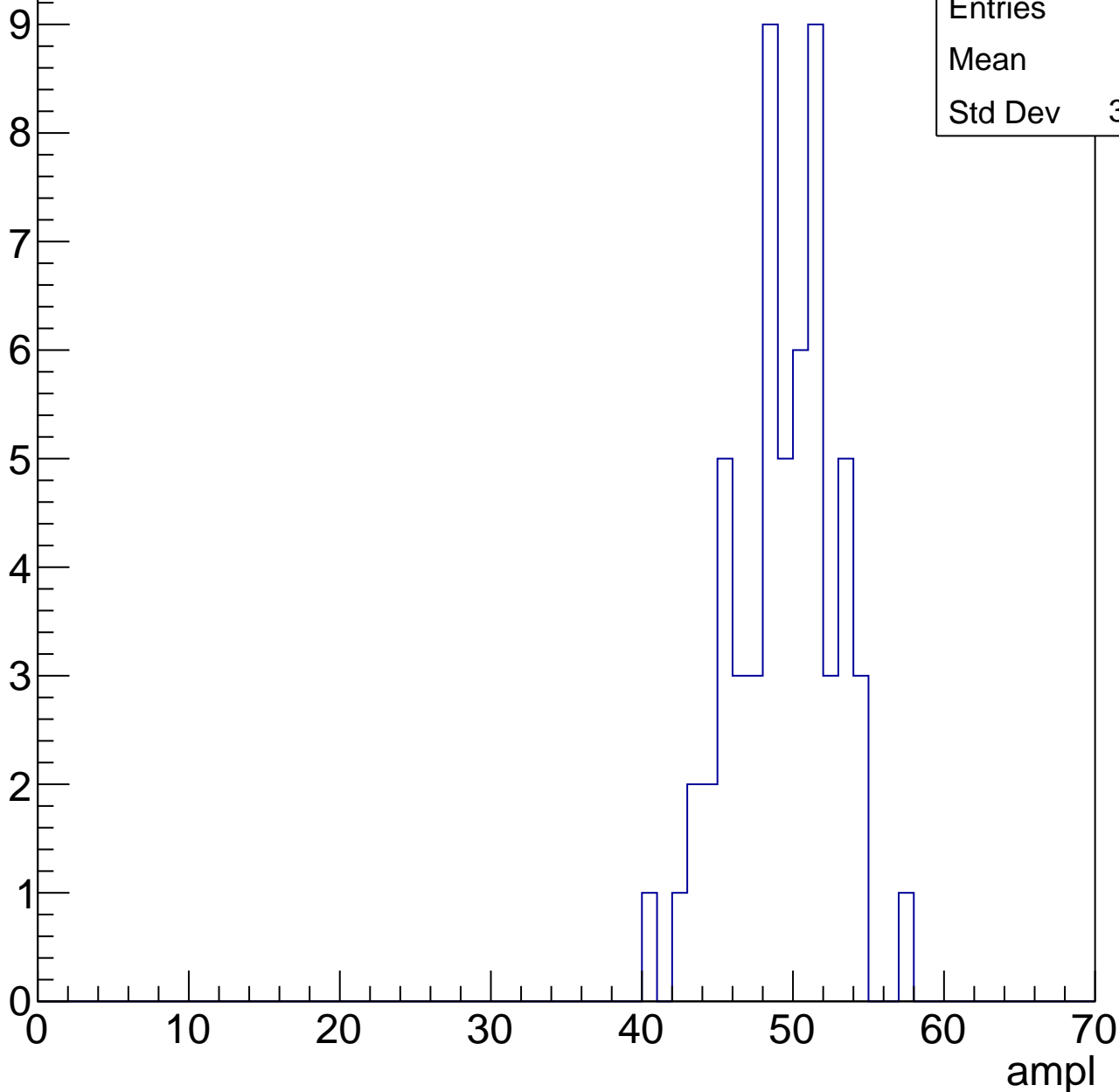


# B1L103S, U3-ch101, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	48.9
Std Dev	3.392

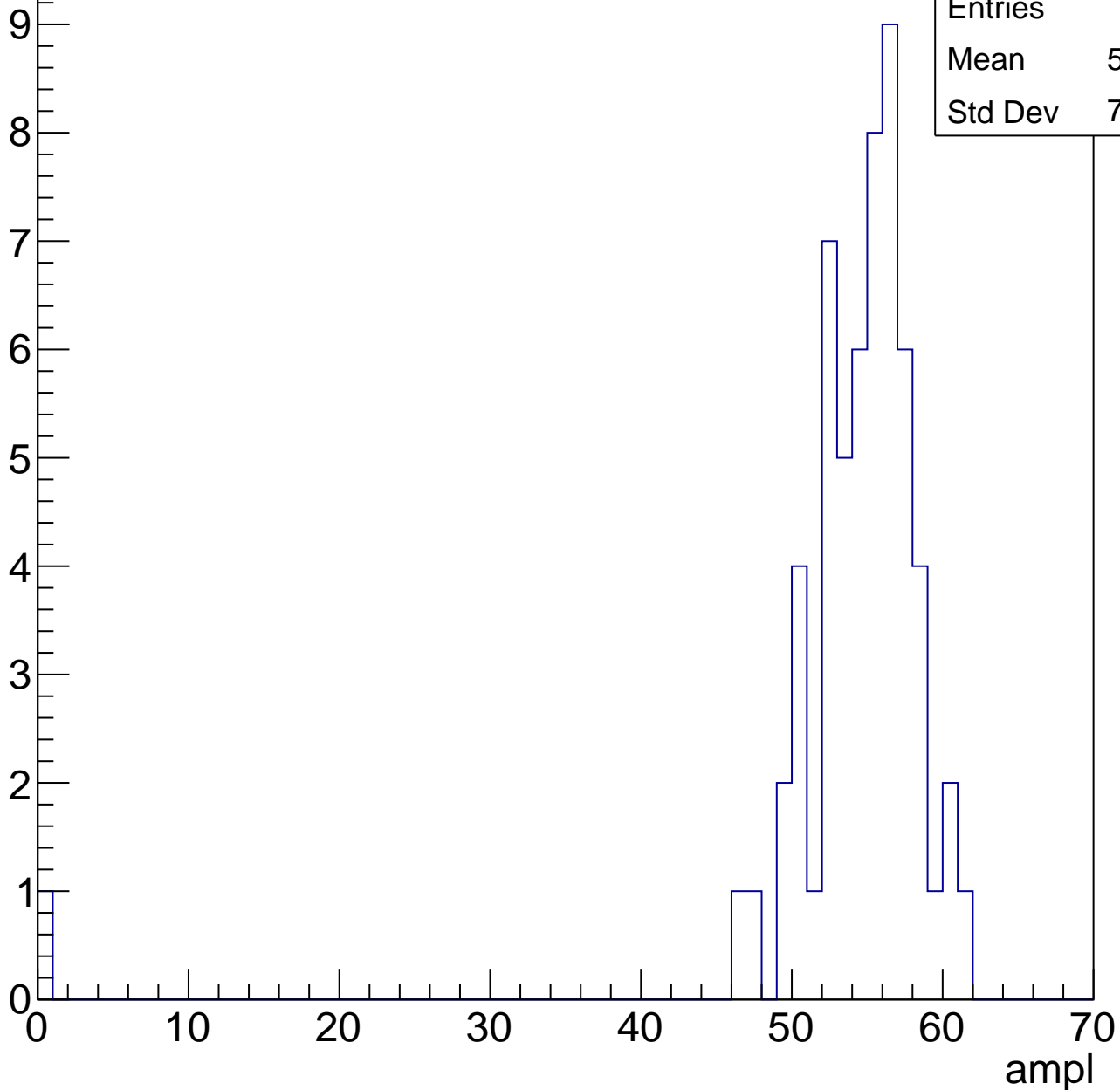


# B1L103S, U3-ch101, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

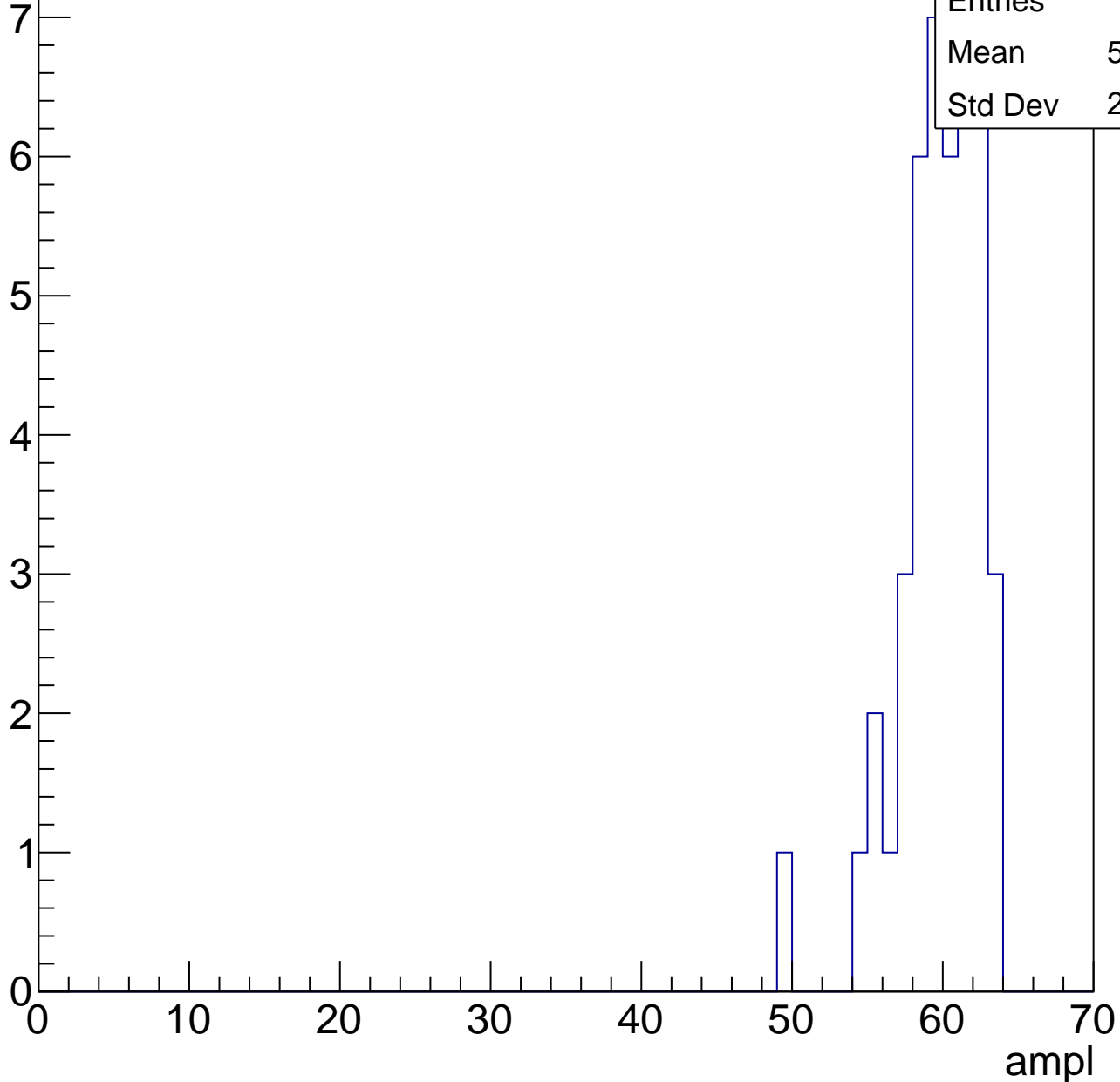
Entries	59
Mean	53.44
Std Dev	7.674



# B1L103S, U3-ch101, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

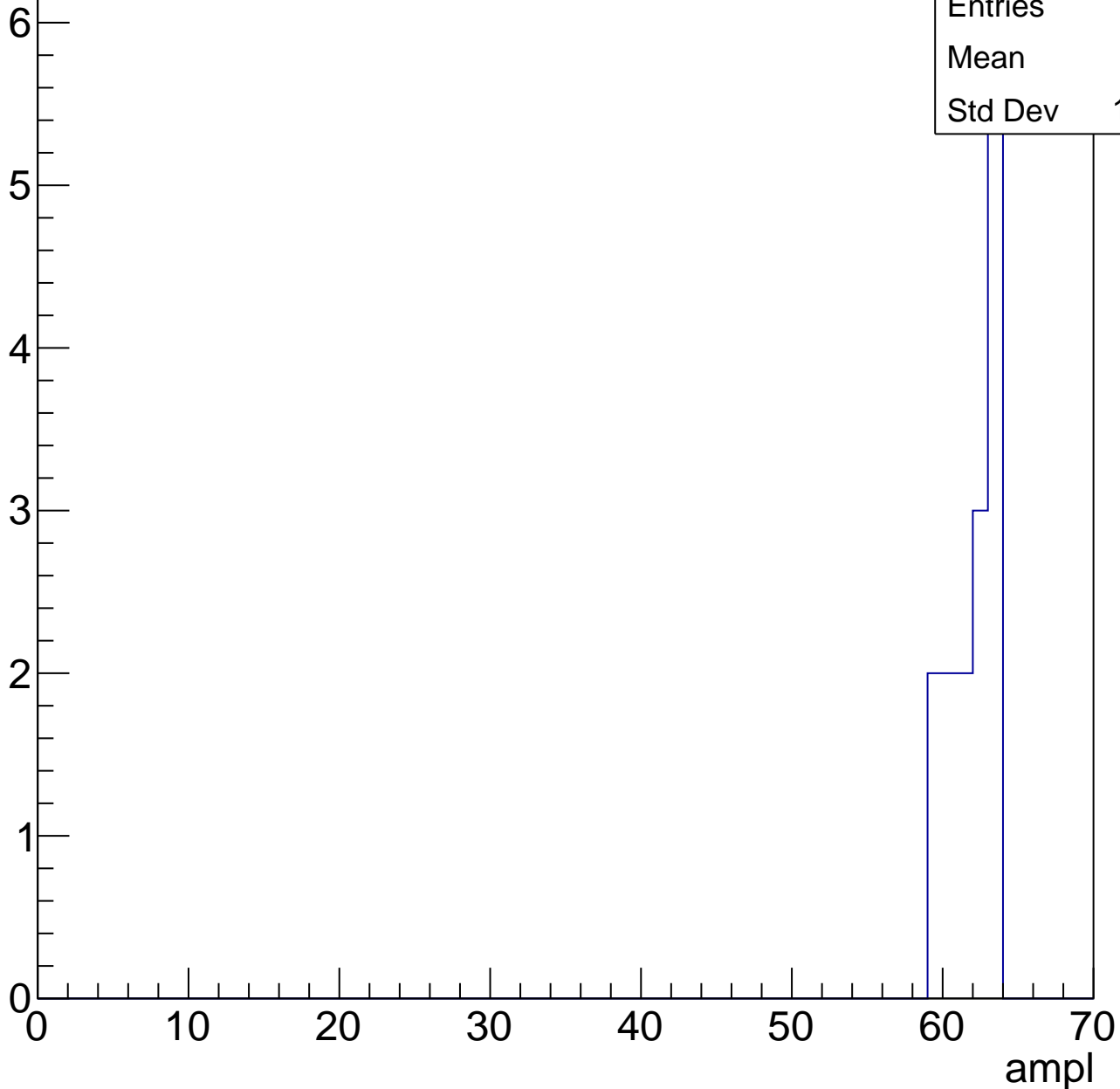


# B1L103S, U3-ch101, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	15
Mean	61.6
Std Dev	1.451

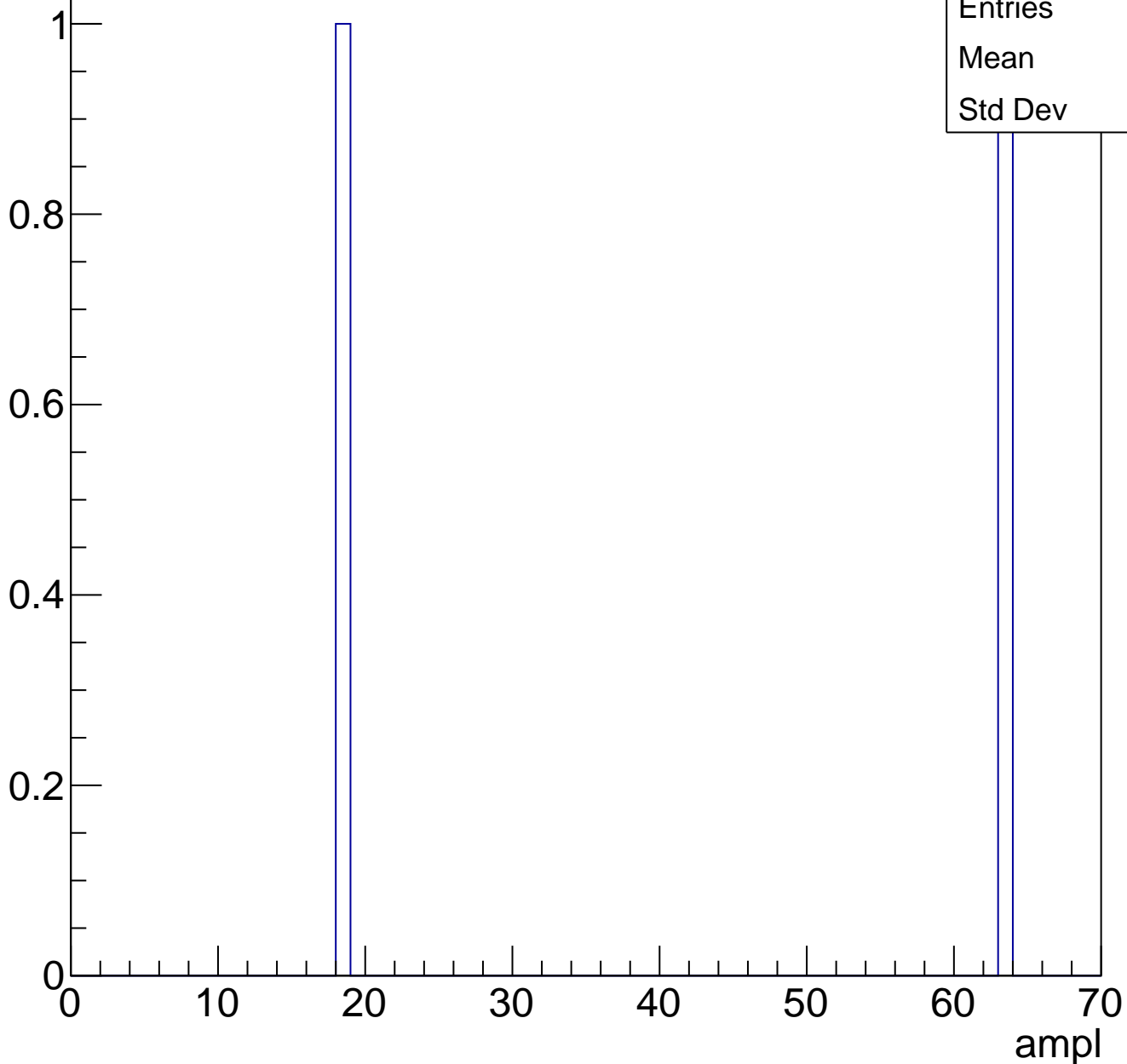




# B1L103S, U3-ch101, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch102, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	86
Mean	25.86
Std Dev	6.994

**Gaus mean : 27.7614**

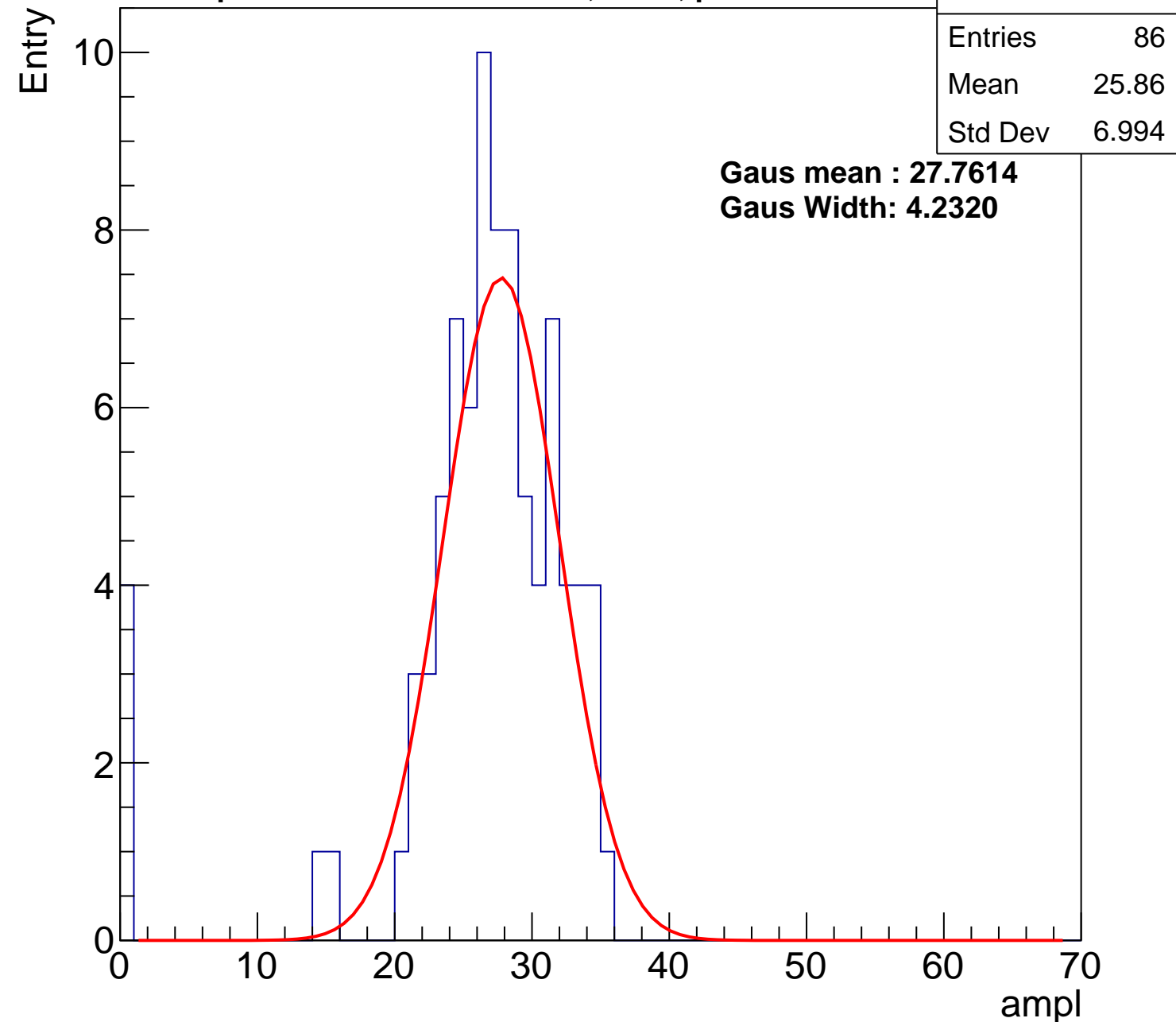
**Gaus Width: 4.2320**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U3-ch102, adc1

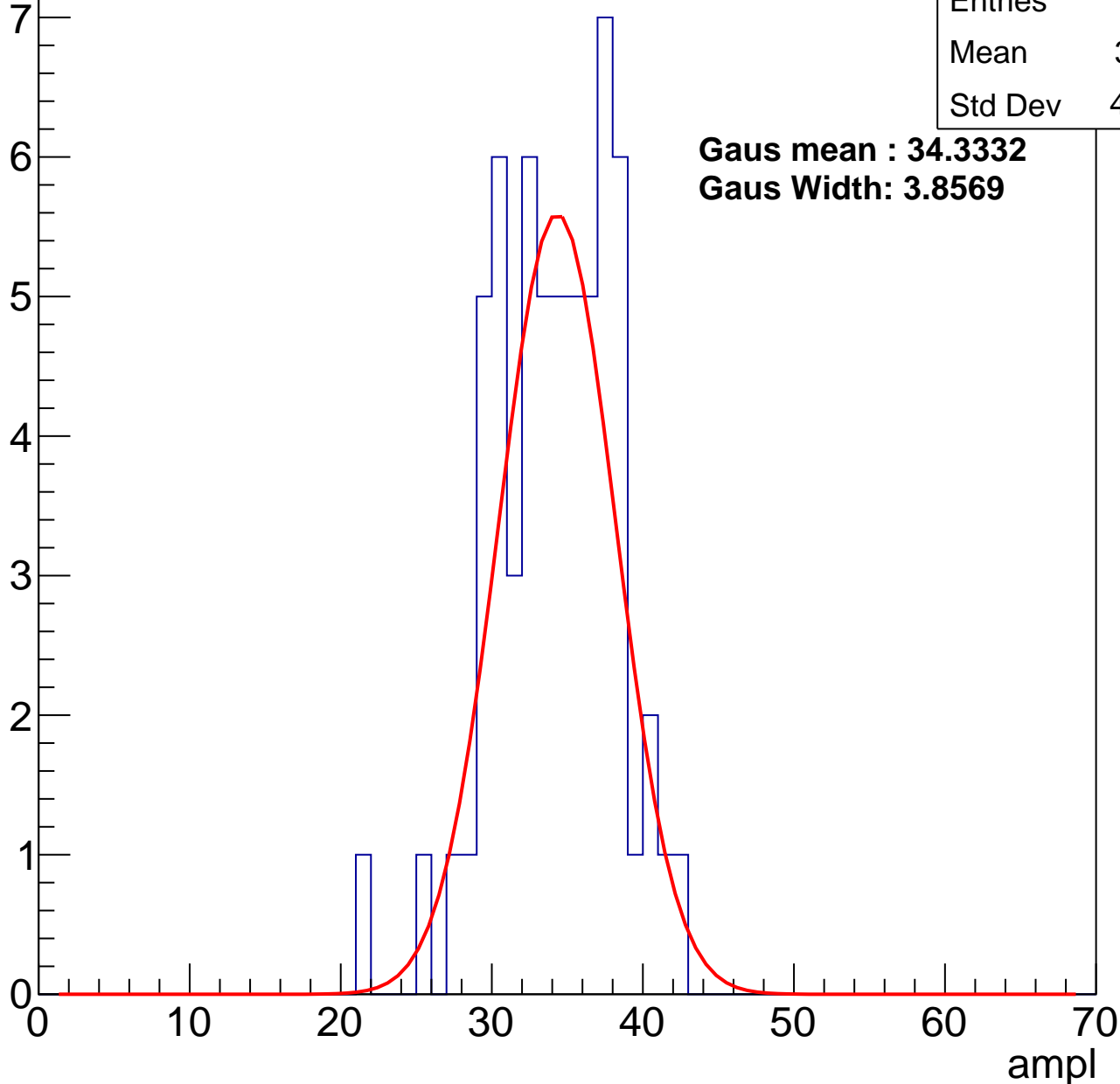
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	33.71
Std Dev	4.018

**Gaus mean : 34.3332**

**Gaus Width: 3.8569**



# B1L103S, U3-ch102, adc2

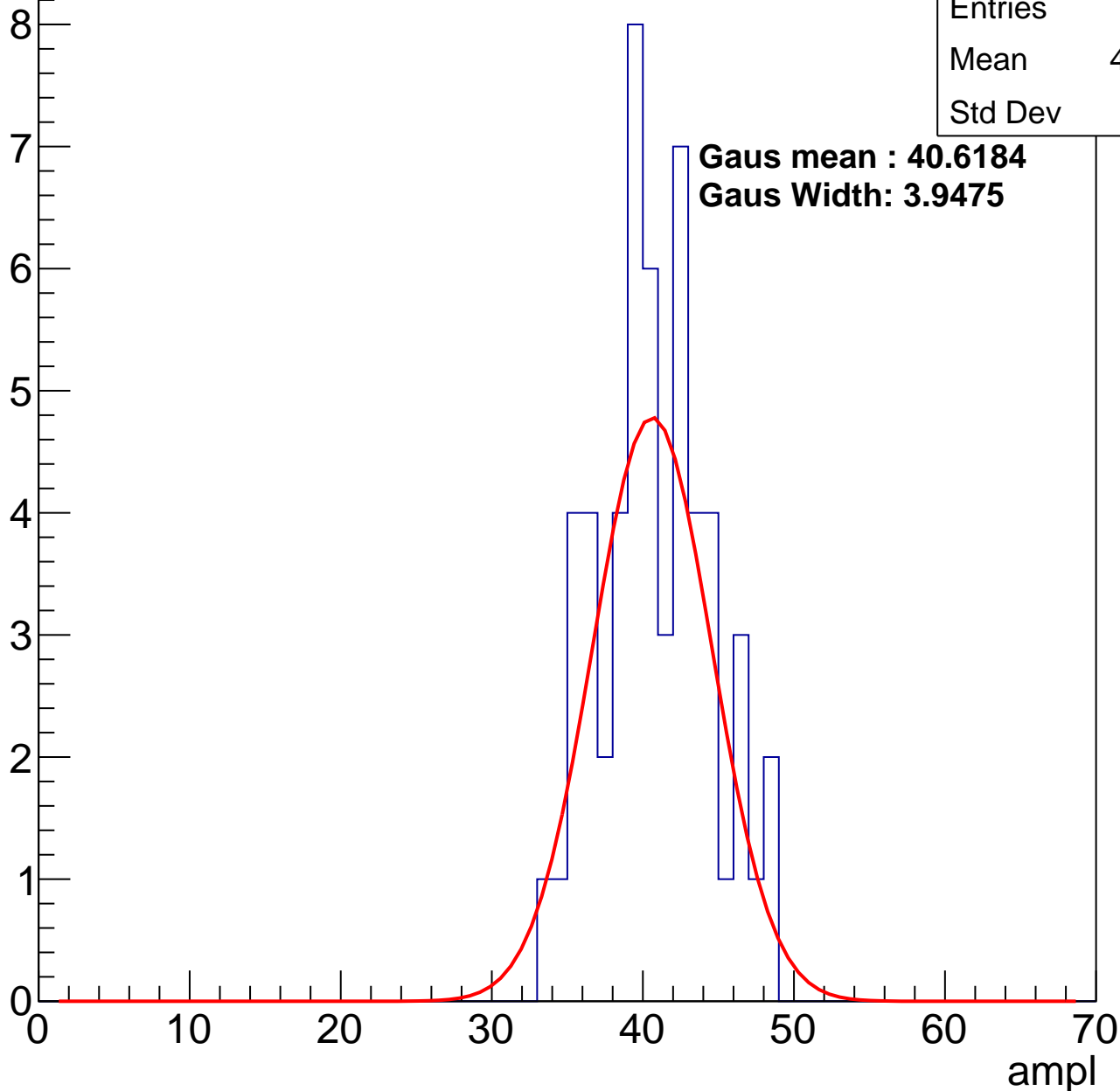
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	40.36
Std Dev	3.63

**Gaus mean : 40.6184**

**Gaus Width: 3.9475**

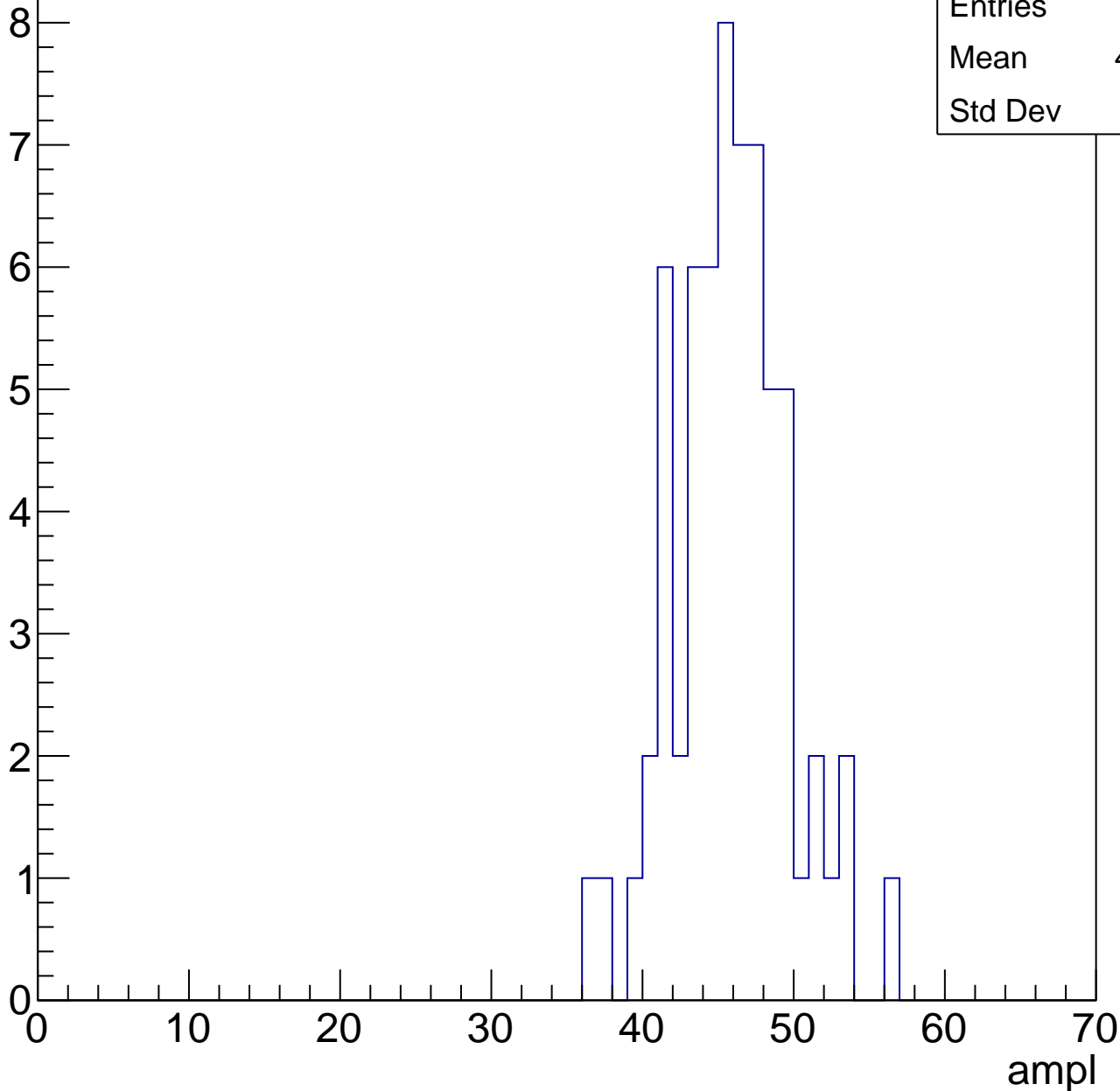


# B1L103S, U3-ch102, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	45.41
Std Dev	3.79

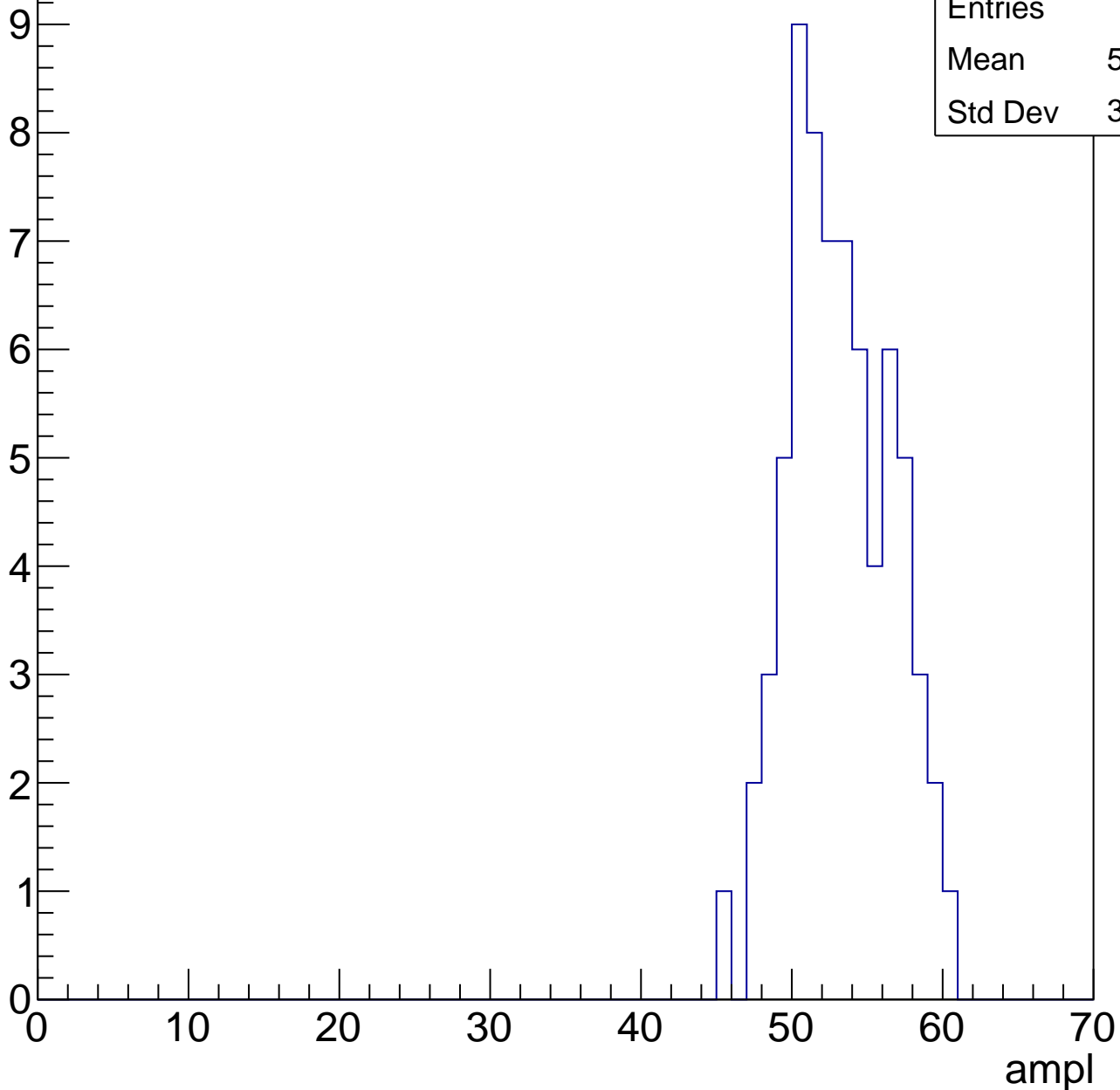


# B1L103S, U3-ch102, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

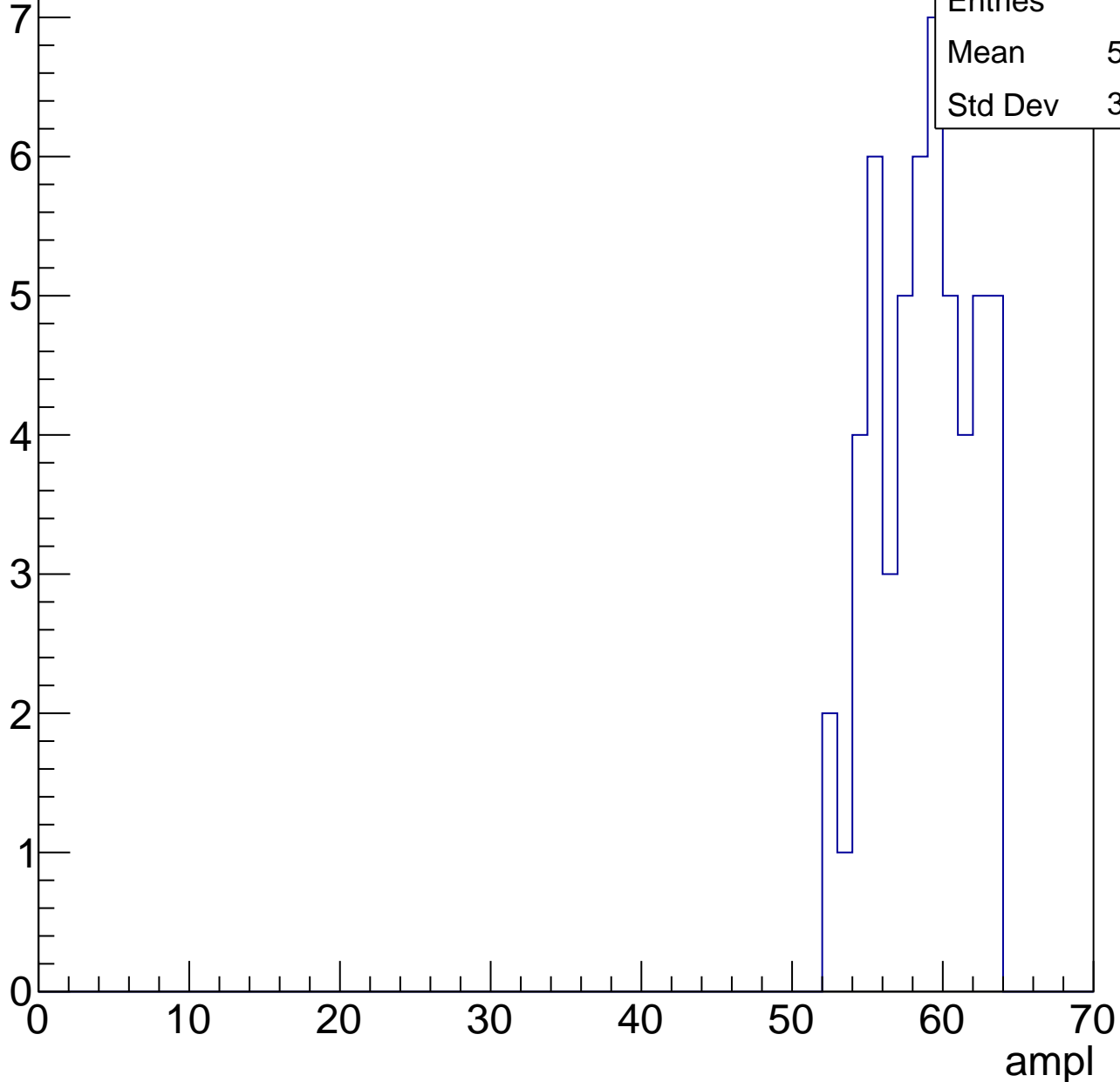
Entries	69
Mean	52.72
Std Dev	3.314



# B1L103S, U3-ch102, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



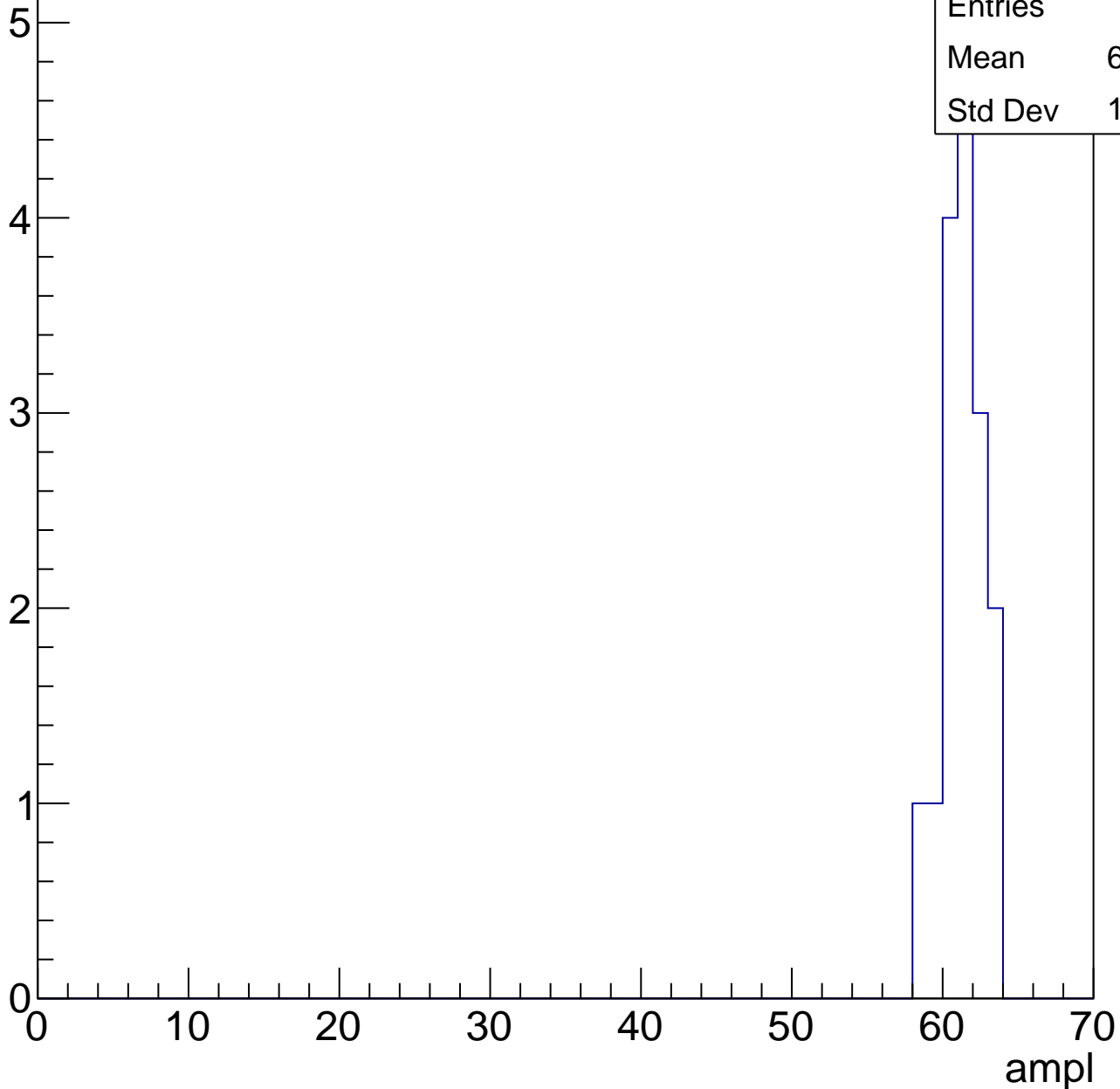
Entries	53
Mean	58.23
Std Dev	3.063

# B1L103S, U3-ch102, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	16
Mean	60.88
Std Dev	1.317

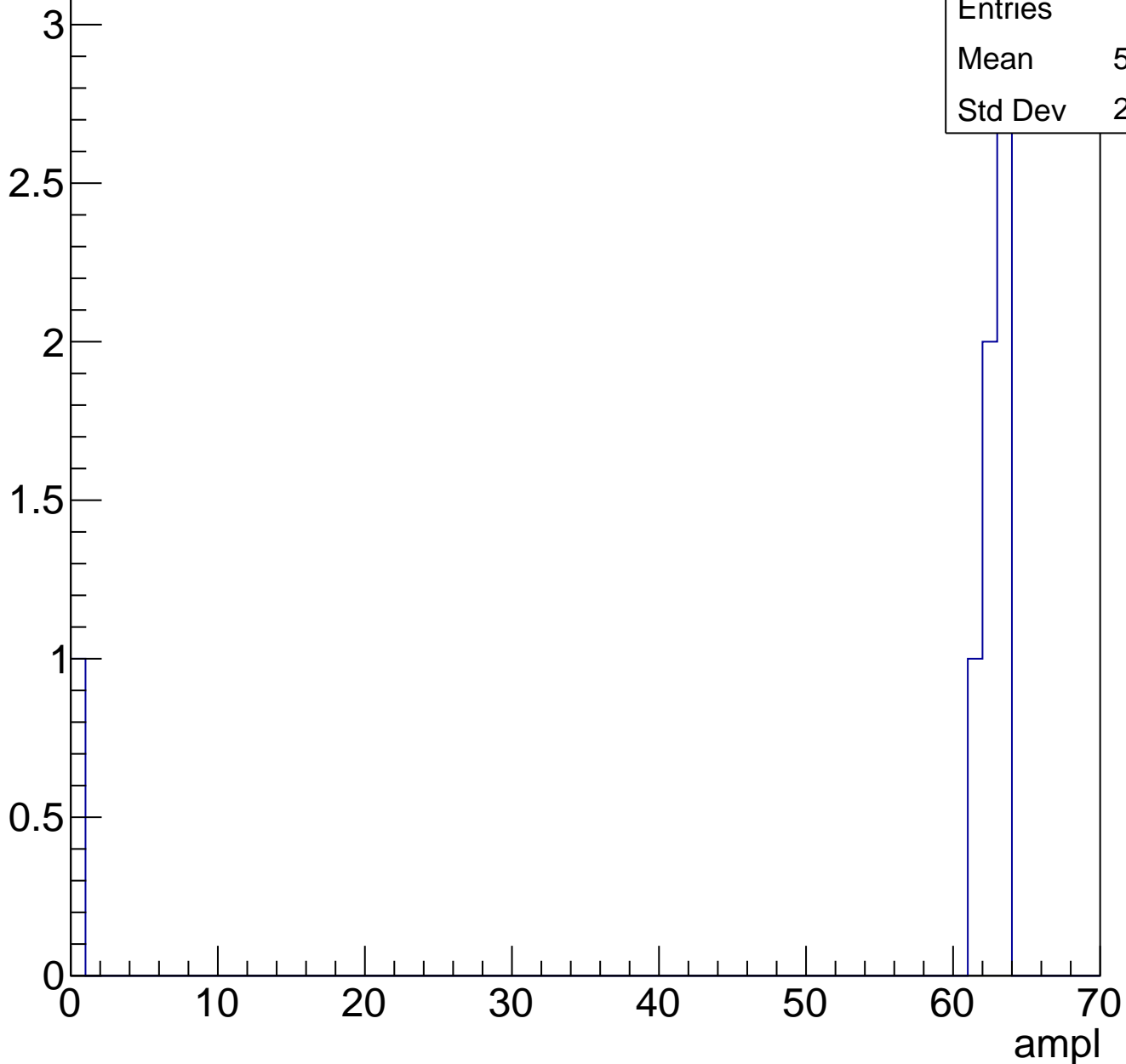




# B1L103S, U3-ch102, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch103, adc0

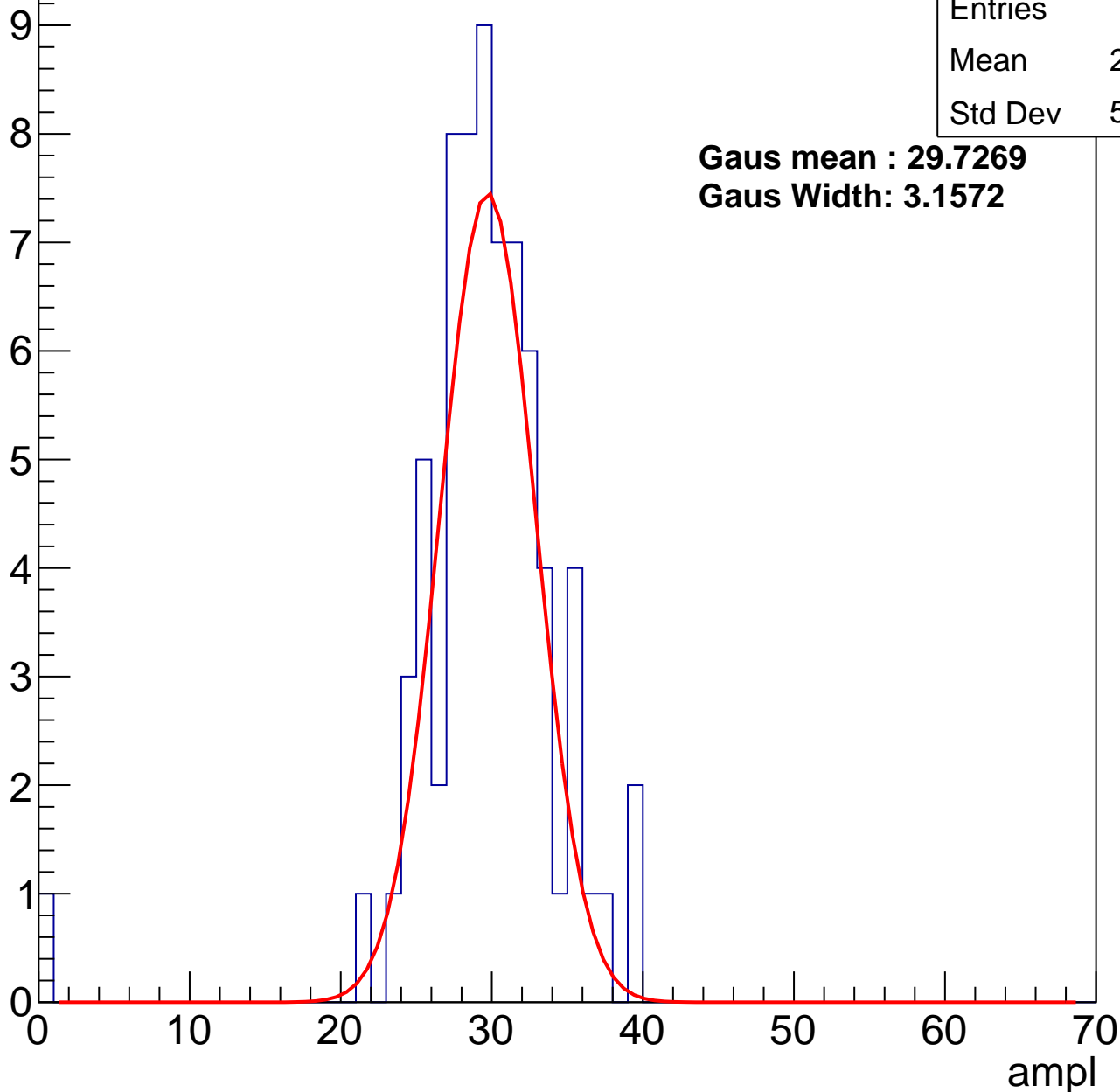
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	29.15
Std Dev	5.017

**Gaus mean : 29.7269**

**Gaus Width: 3.1572**



# B1L103S, U3-ch103, adc1

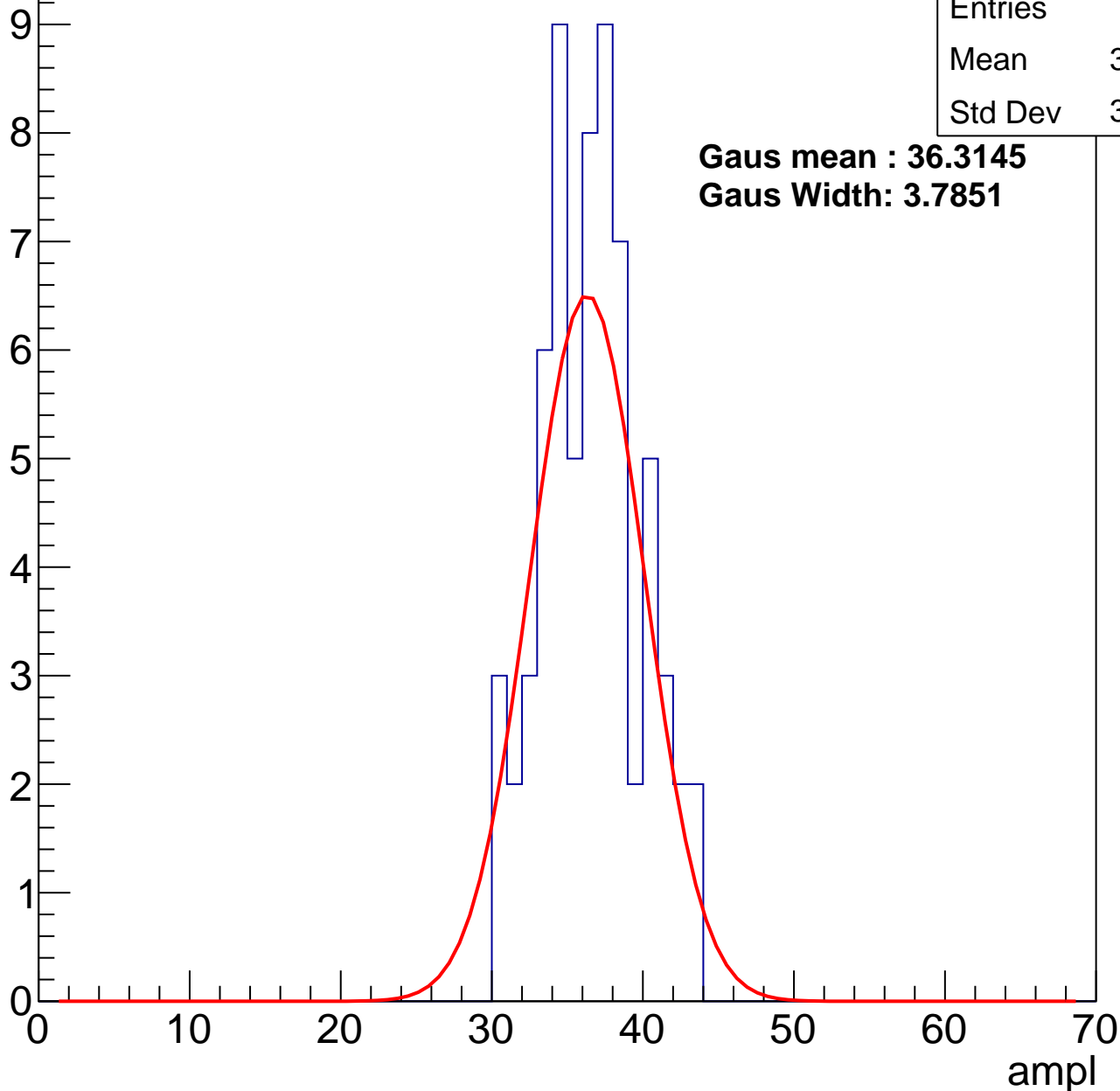
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	36.14
Std Dev	3.209

**Gaus mean : 36.3145**

**Gaus Width: 3.7851**



# B1L103S, U3-ch103, adc2

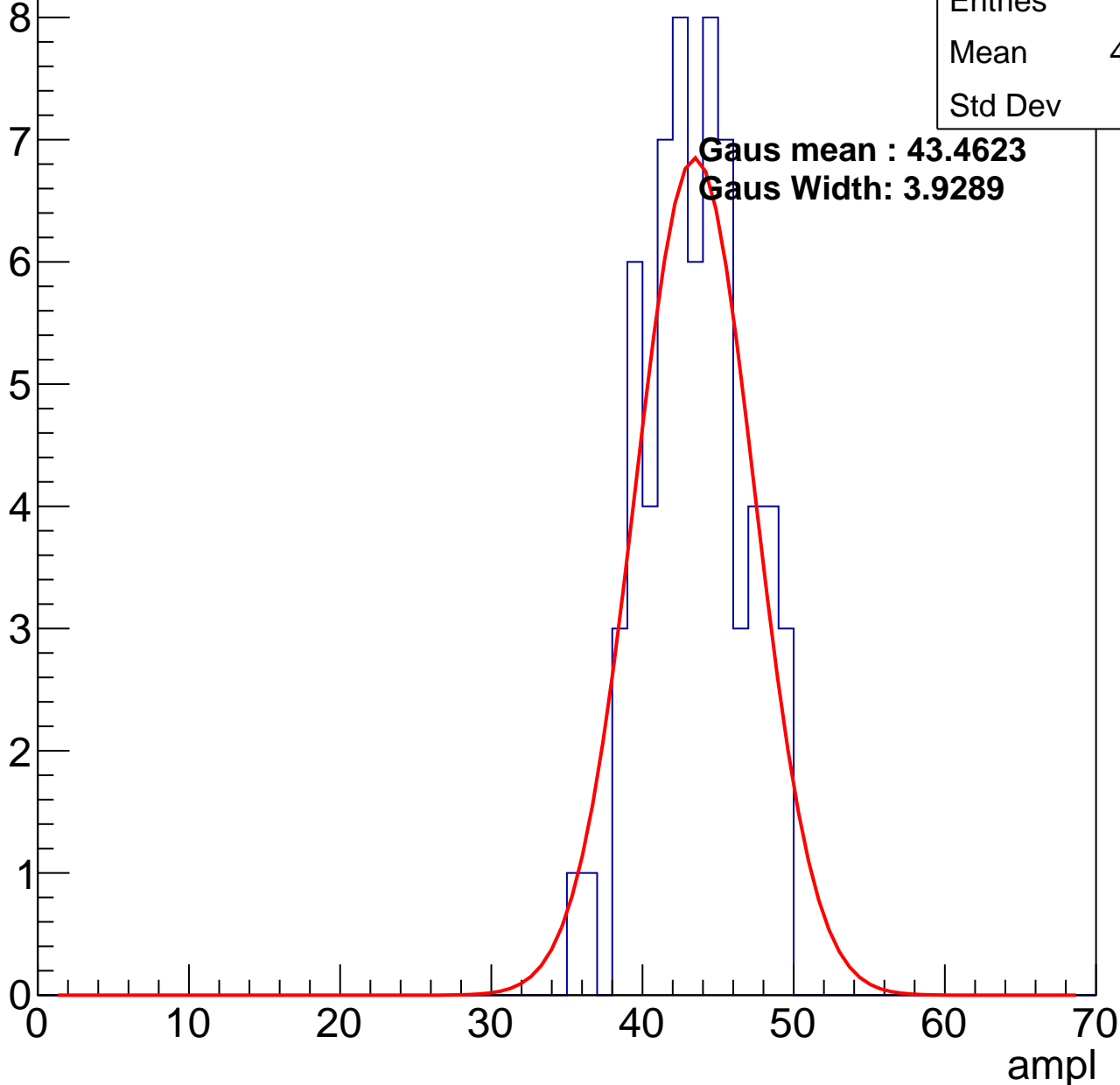
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	42.95
Std Dev	3.26

**Gaus mean : 43.4623**

**Gaus Width: 3.9289**

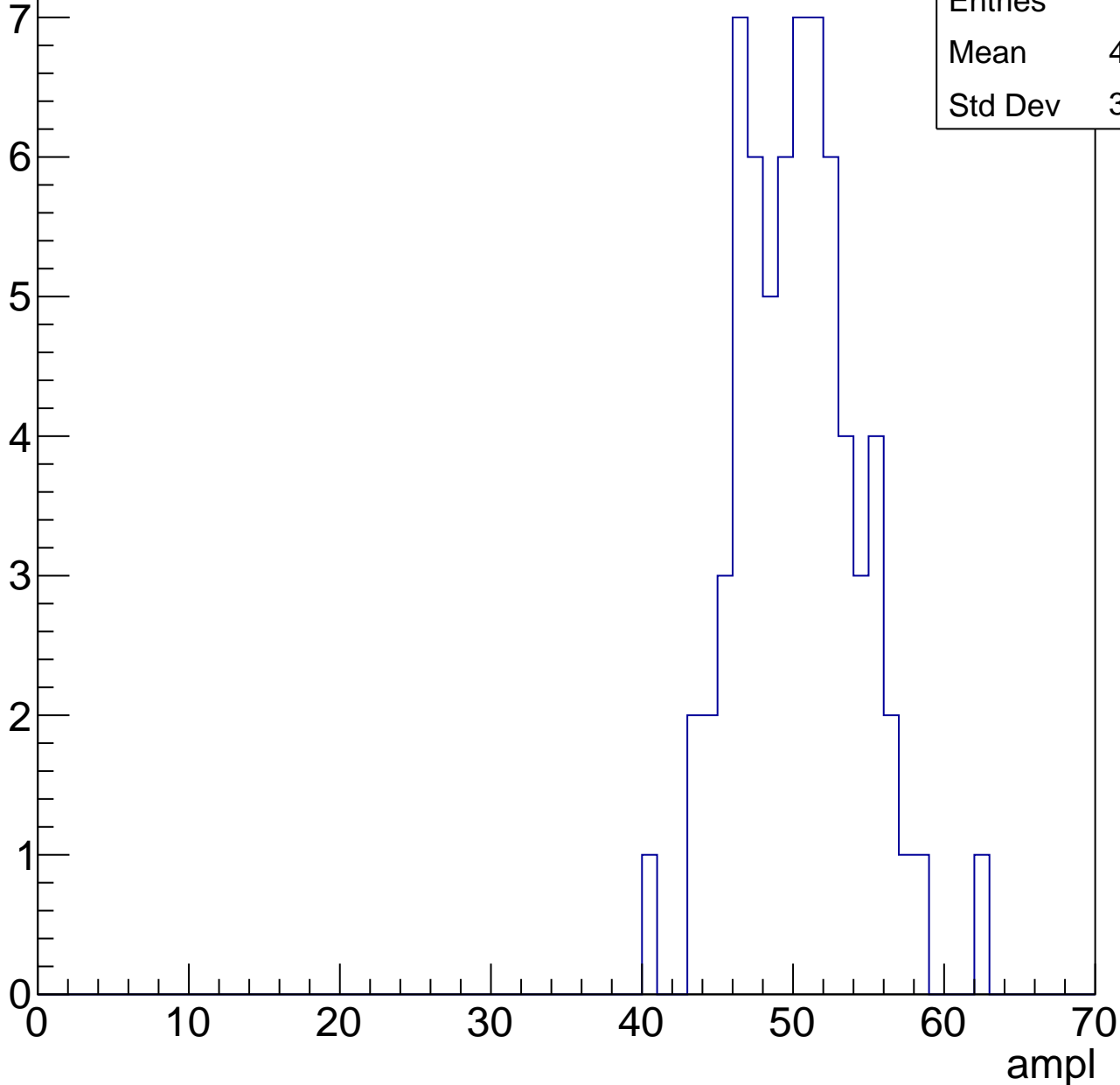


# B1L103S, U3-ch103, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	49.84
Std Dev	3.984

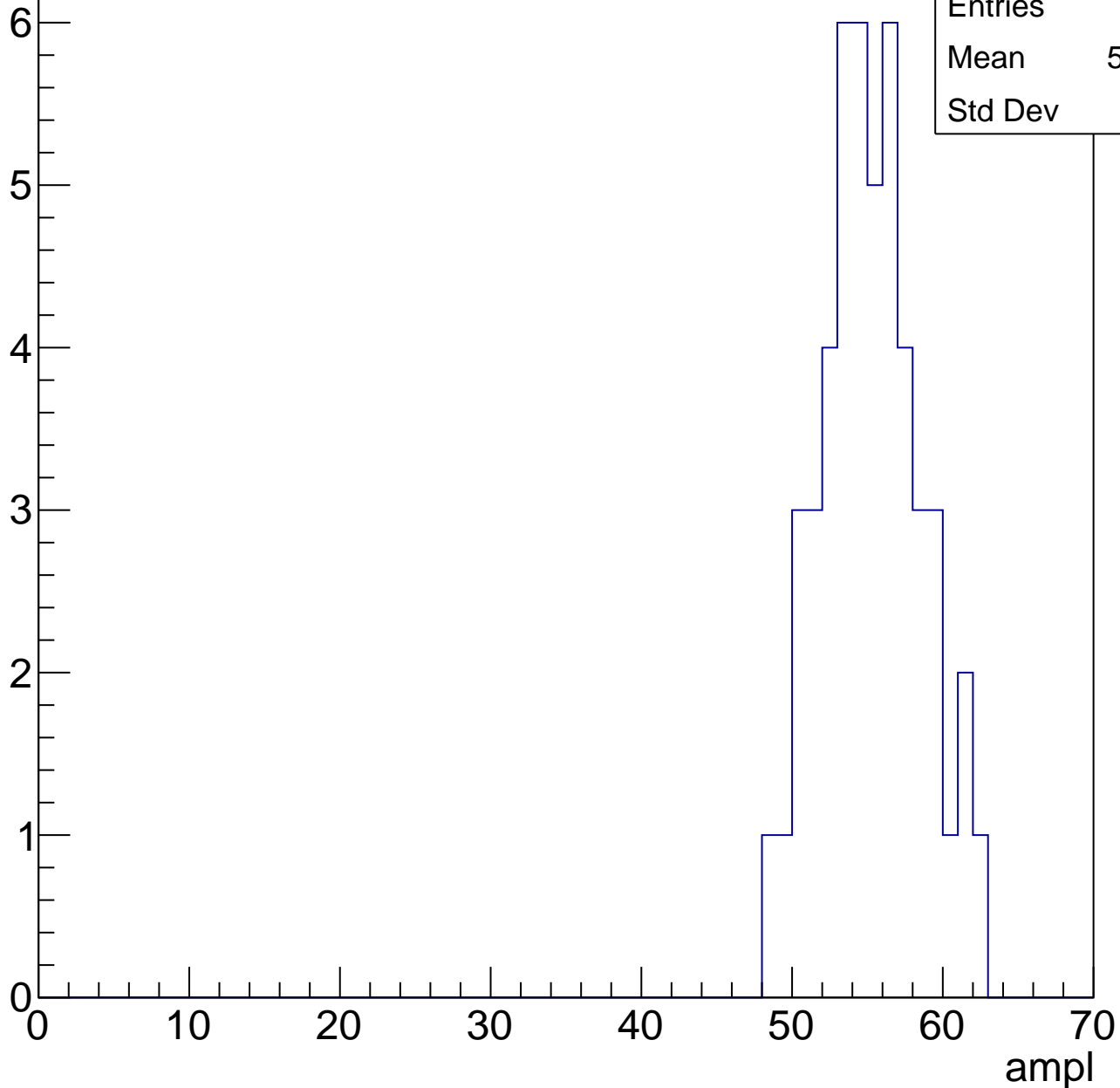


# B1L103S, U3-ch103, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	54.78
Std Dev	3.24



# B1L103S, U3-ch103, adc5

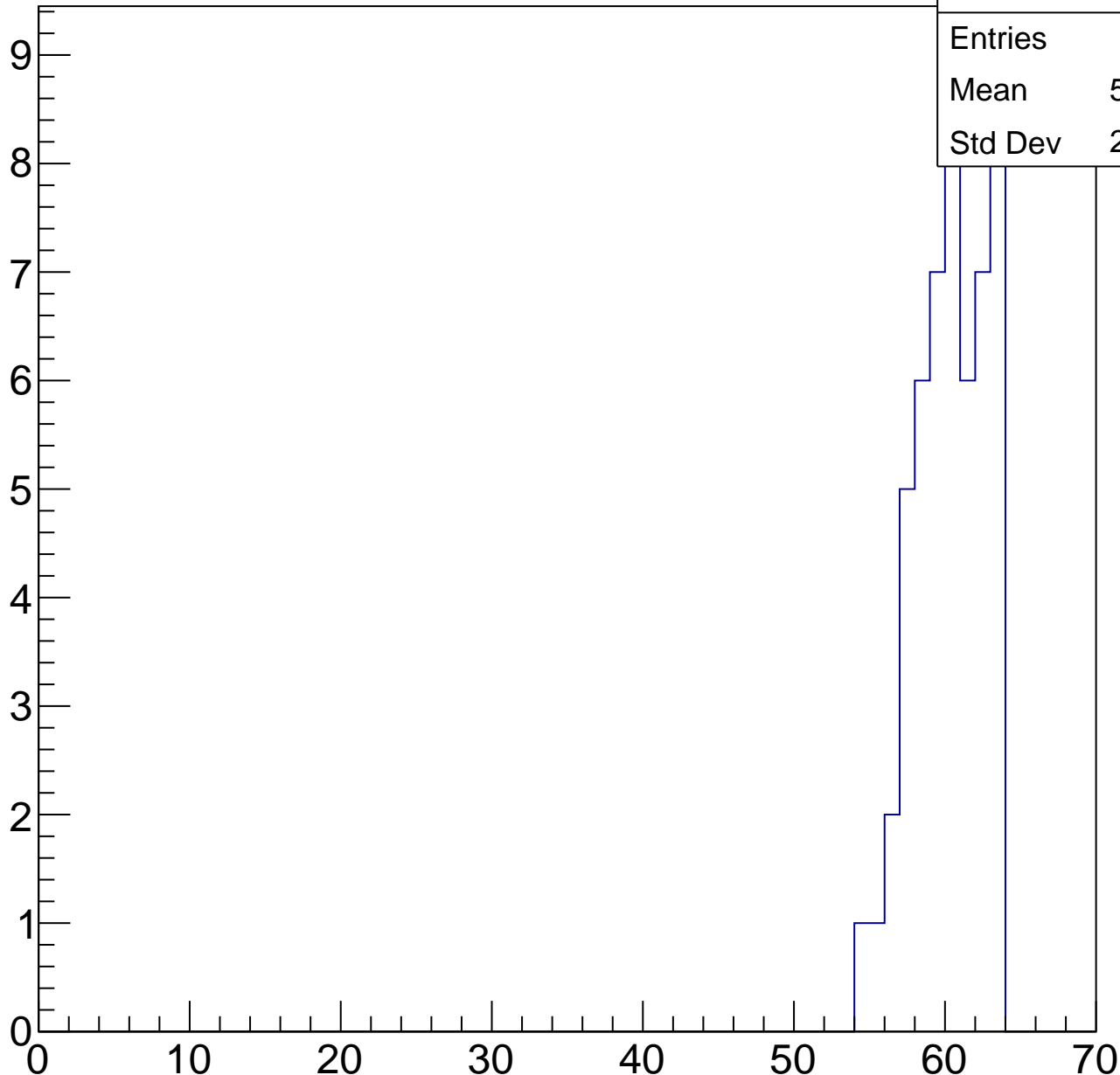
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	52
Mean	59.83
Std Dev	2.293

ampl



# B1L103S, U3-ch103, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

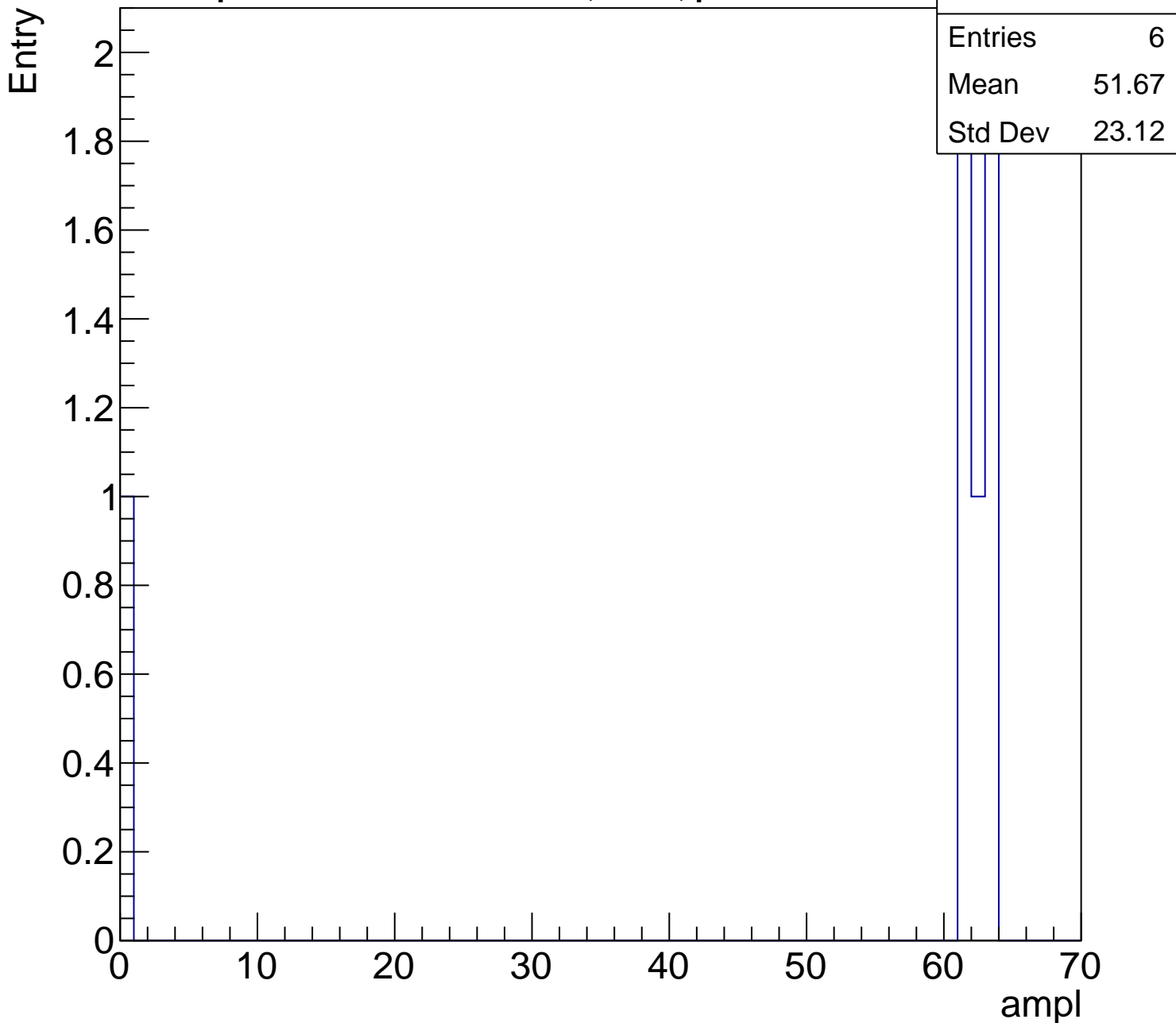
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	51.67
Std Dev	23.12

0 10 20 30 40 50 60 70

ampl





# B1L103S, U3-ch103, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U3-ch104, adc0

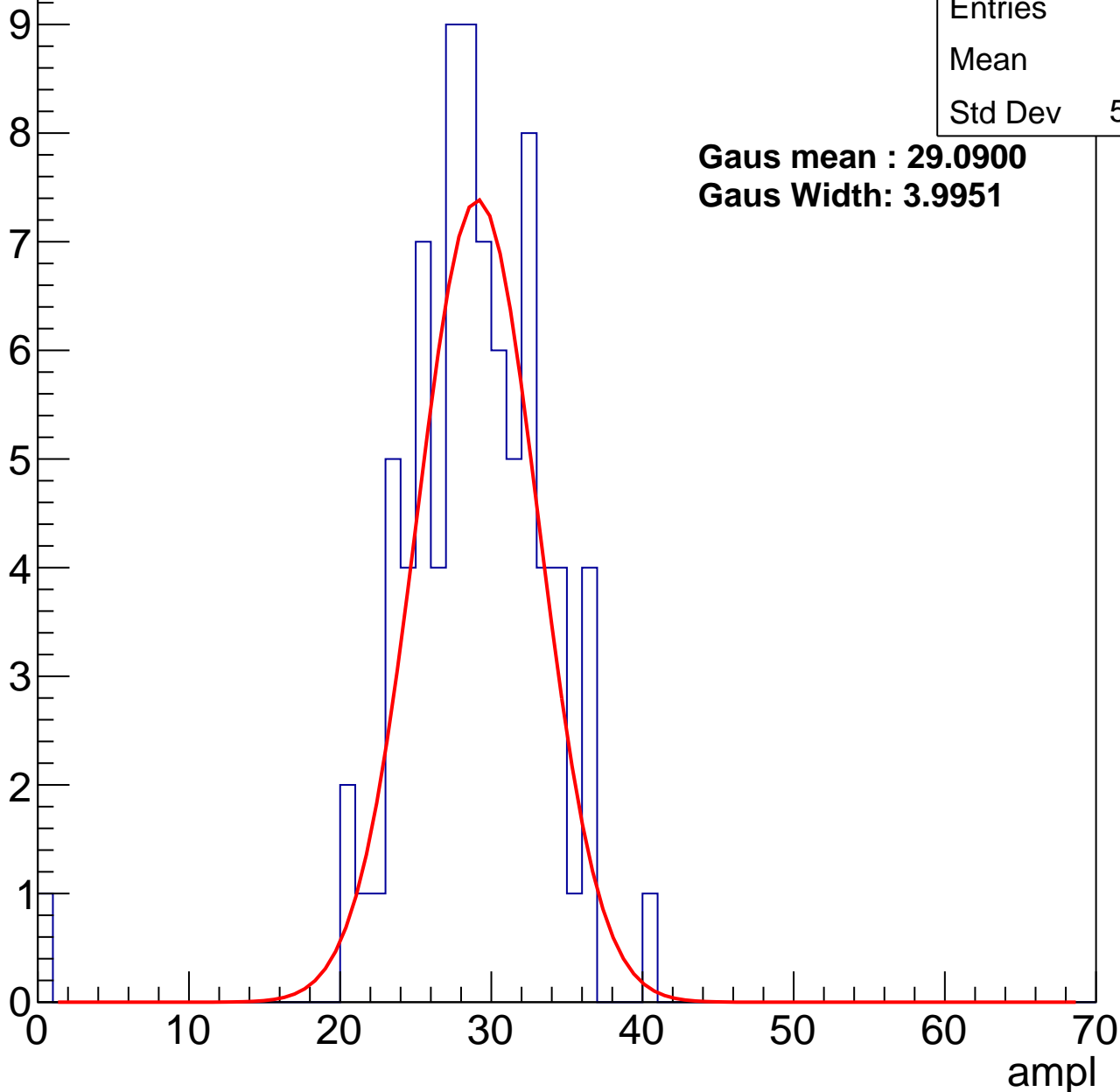
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	83
Mean	28.3
Std Dev	5.105

**Gaus mean : 29.0900**

**Gaus Width: 3.9951**



# B1L103S, U3-ch104, adc1

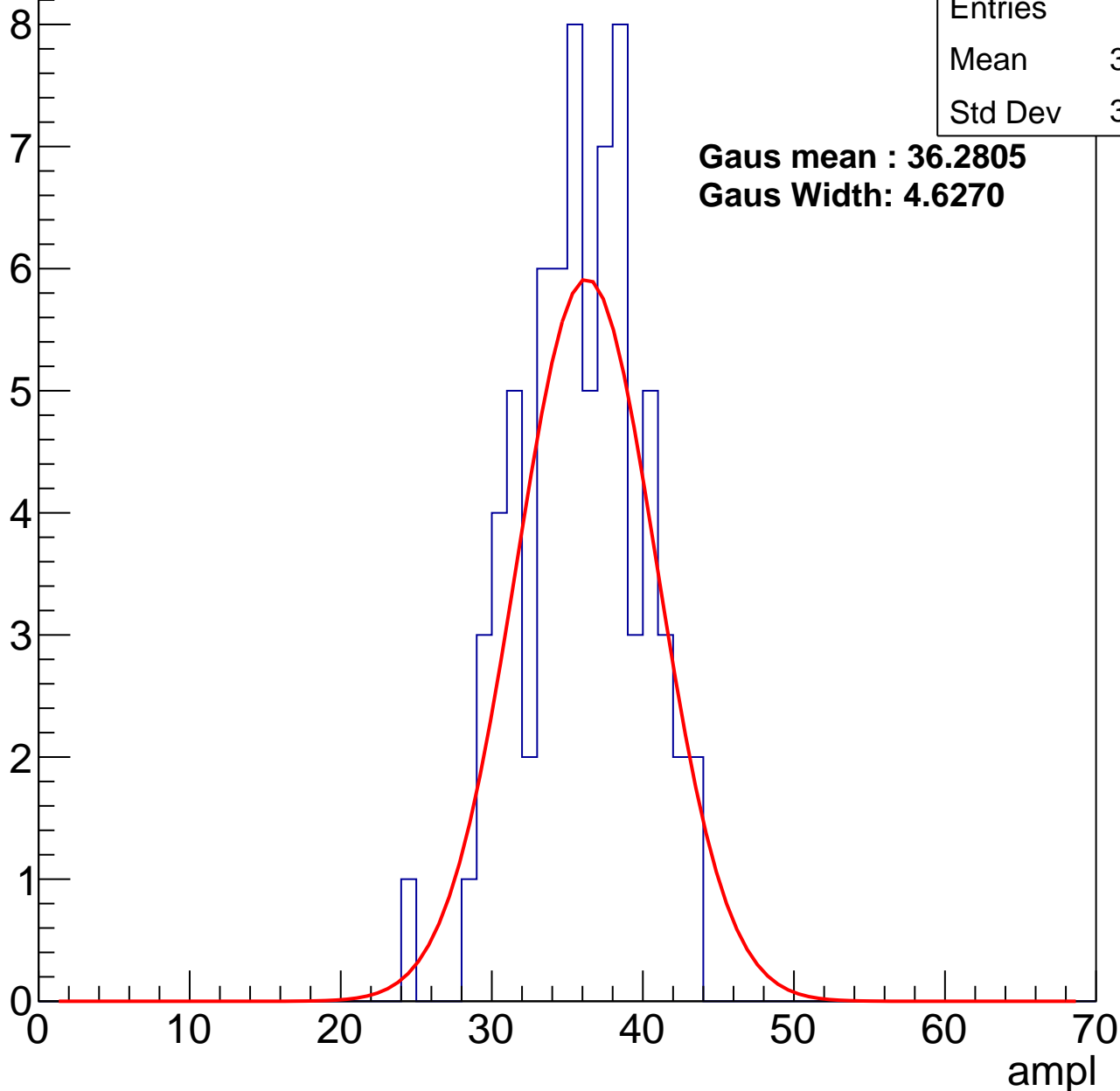
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	35.39
Std Dev	3.949

**Gaus mean : 36.2805**

**Gaus Width: 4.6270**



# B1L103S, U3-ch104, adc2

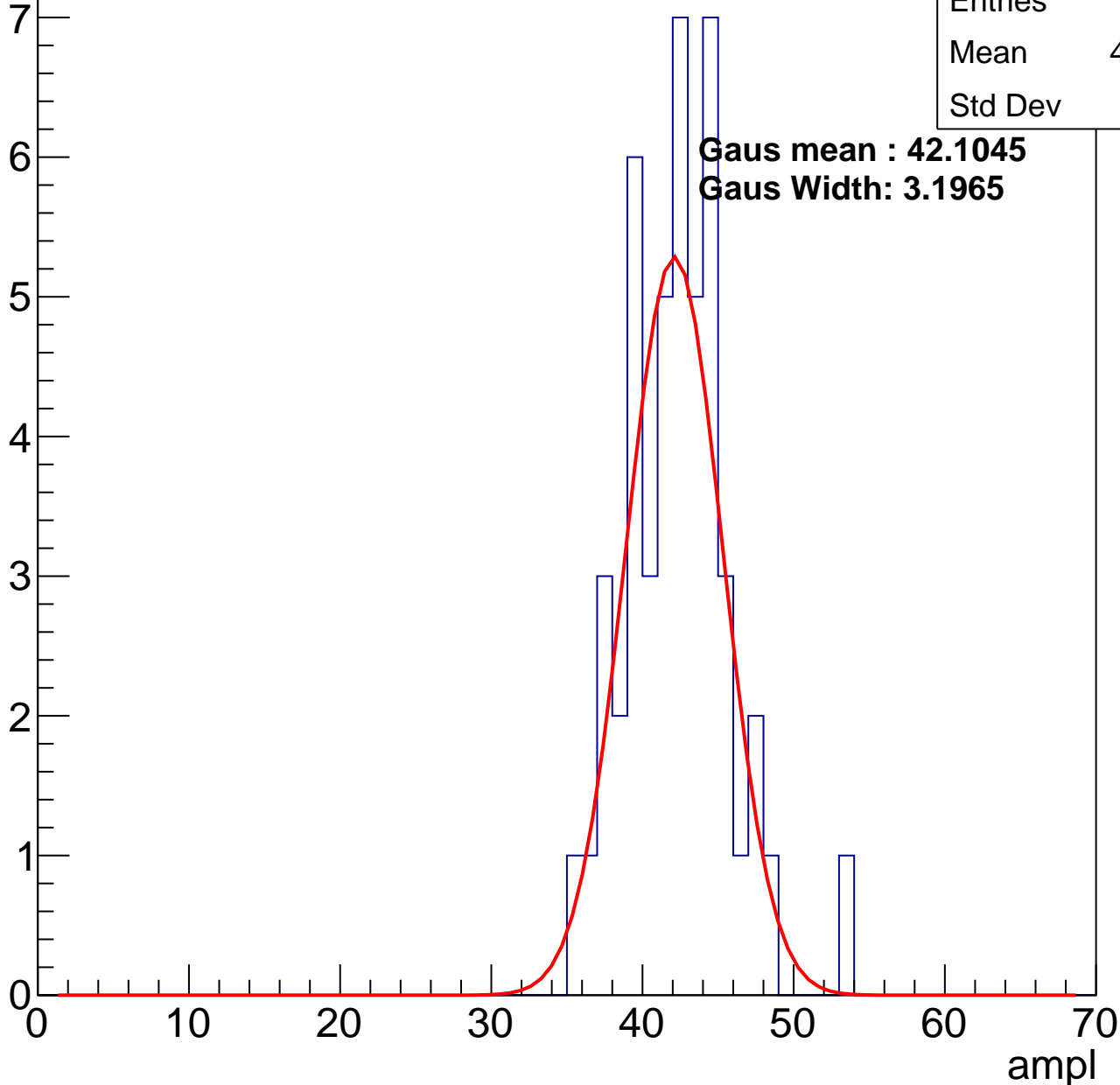
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	48
Mean	41.88
Std Dev	3.37

**Gaus mean : 42.1045**

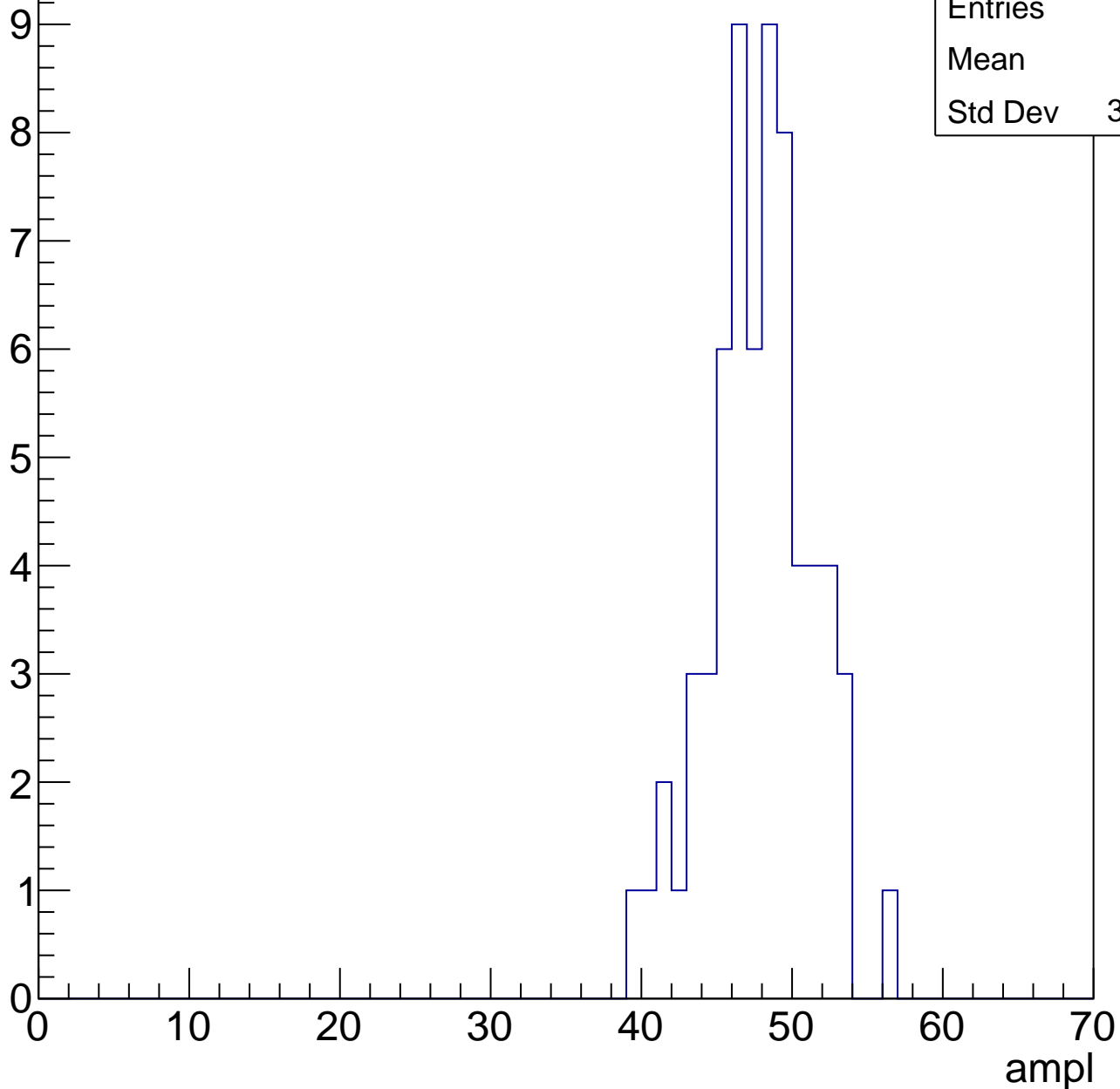
**Gaus Width: 3.1965**



# B1L103S, U3-ch104, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



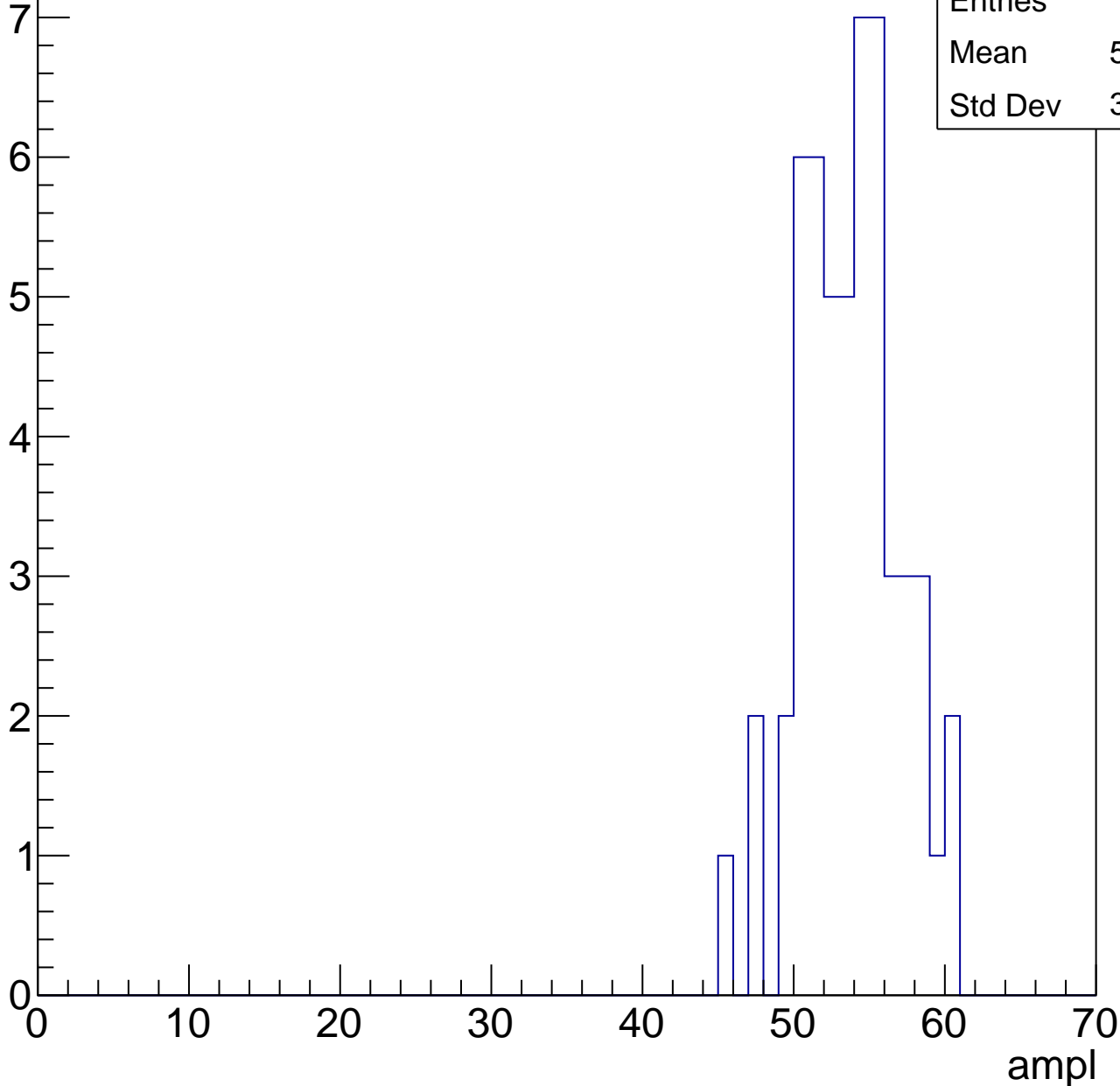
Entries	65
Mean	47.4
Std Dev	3.369

# B1L103S, U3-ch104, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	53.26
Std Dev	3.269

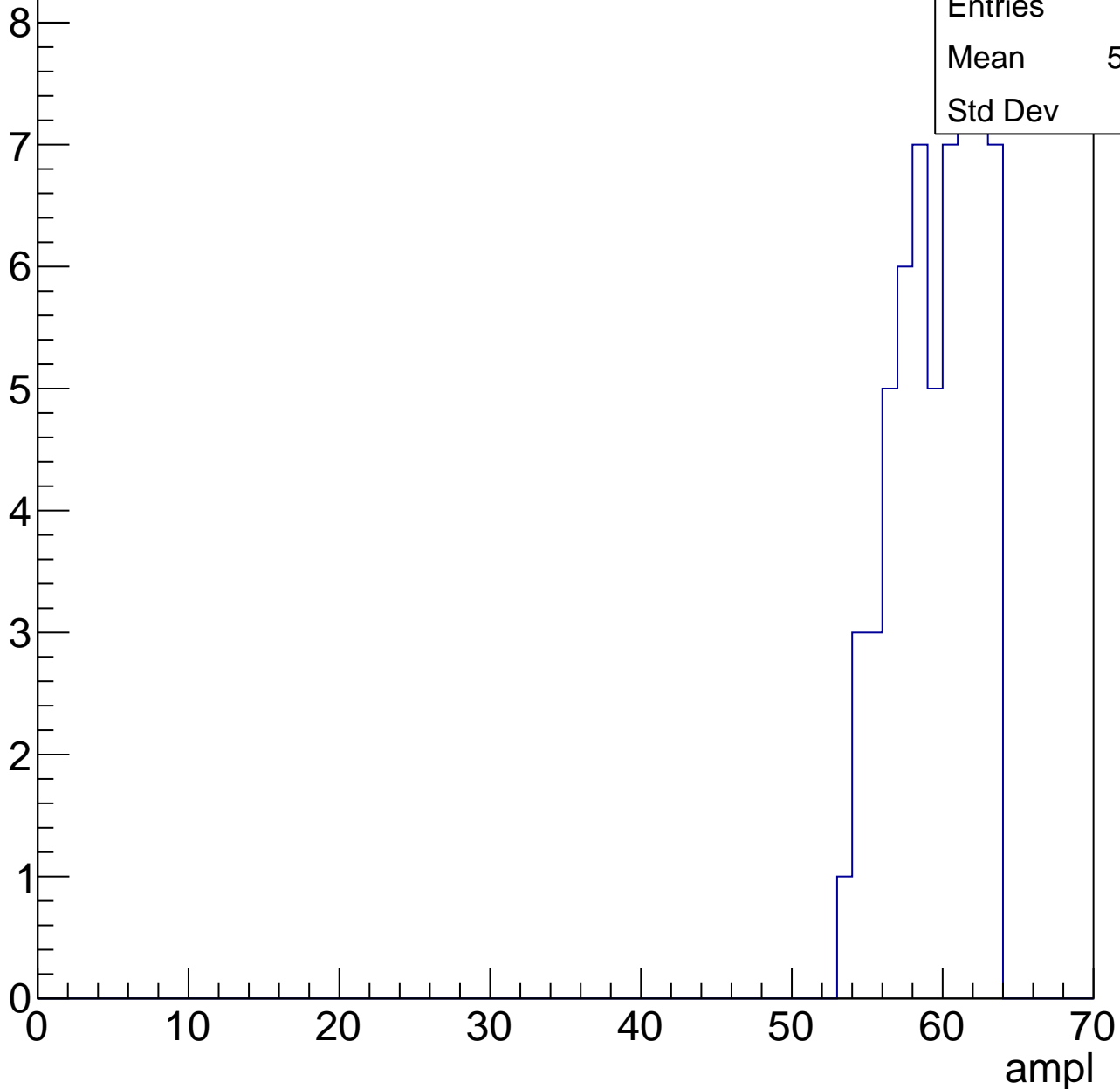


# B1L103S, U3-ch104, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

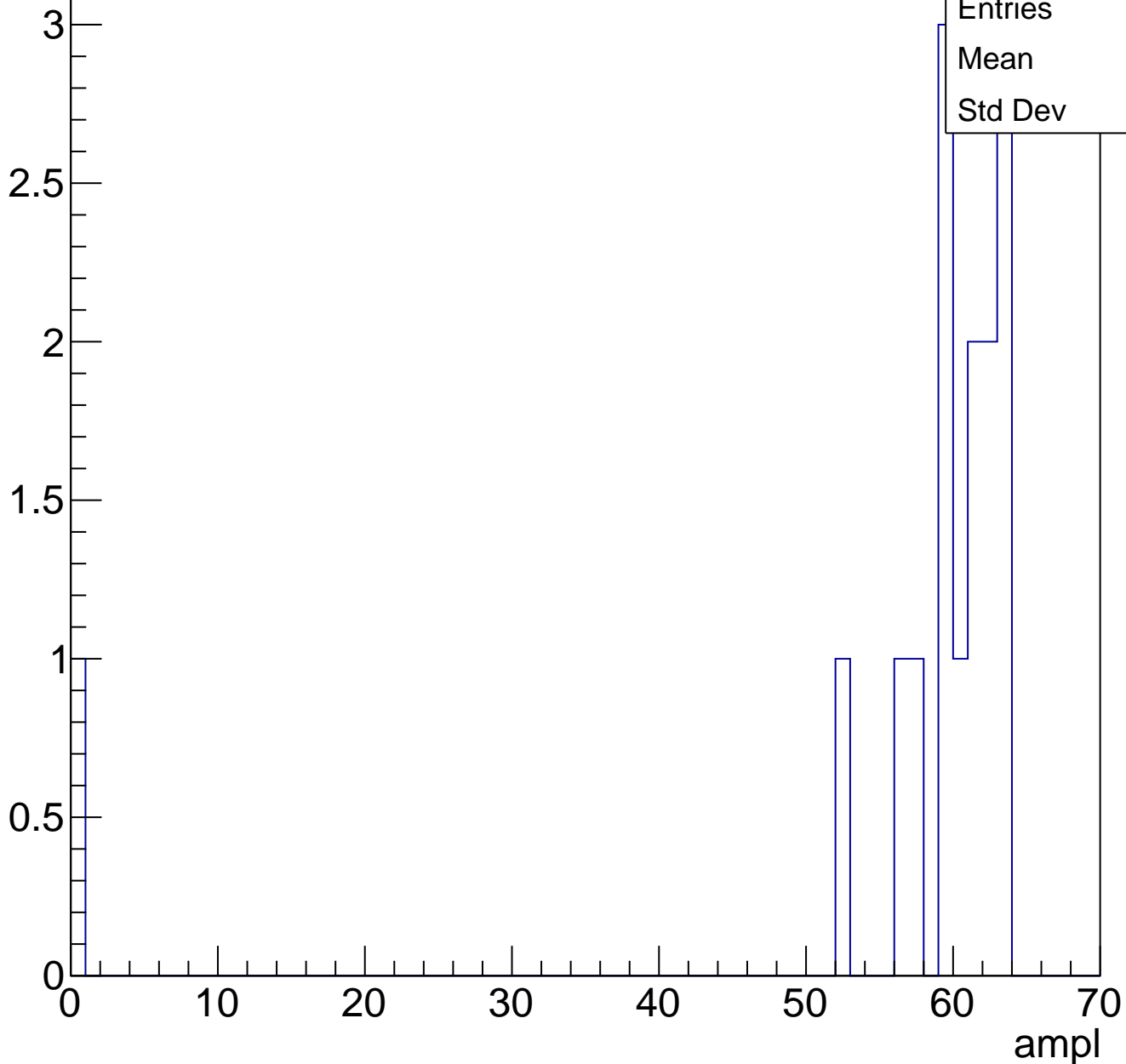
Entries	60
Mean	59.13
Std Dev	2.76



# B1L103S, U3-ch104, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

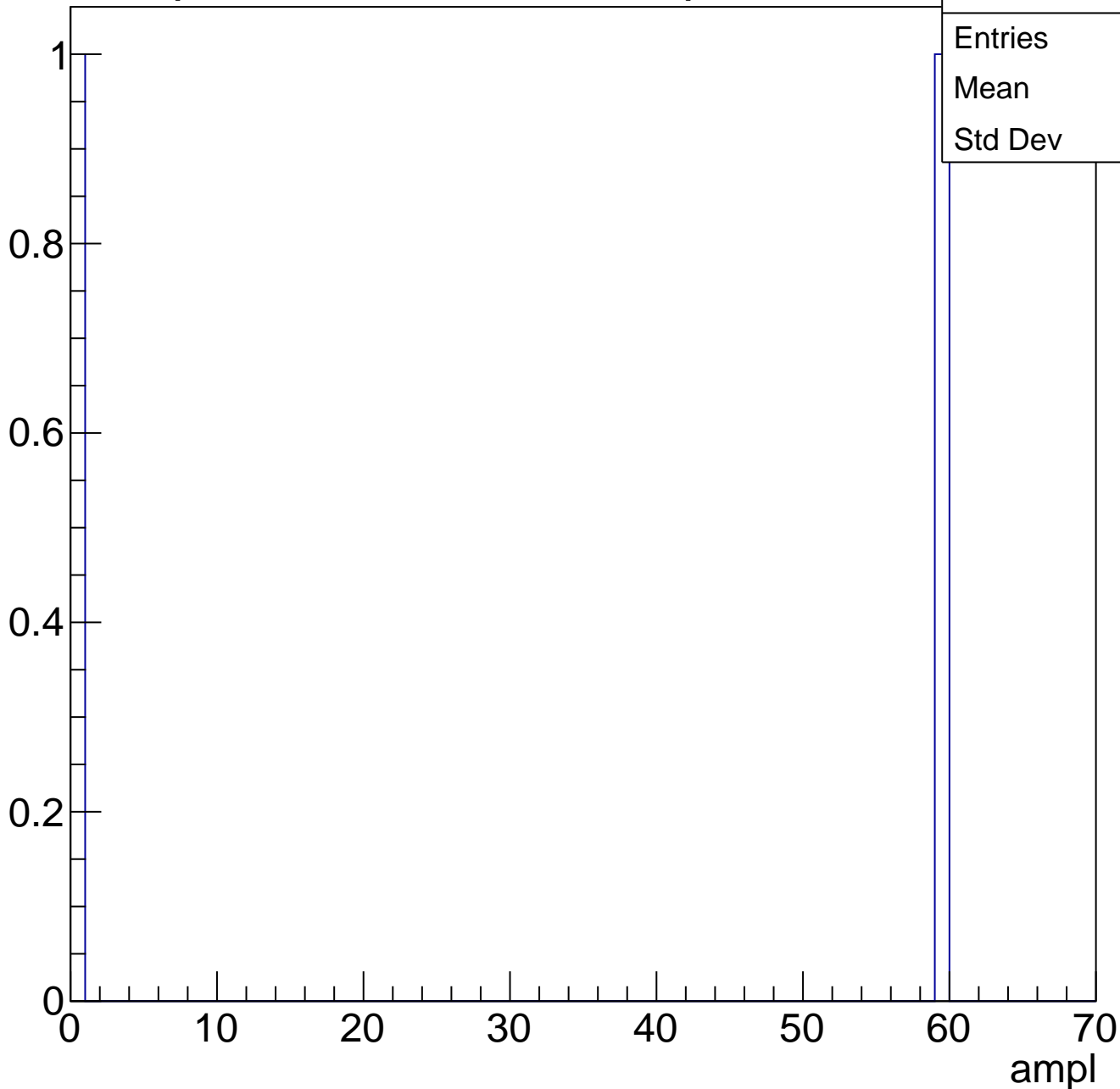




# B1L103S, U3-ch104, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch105, adc0

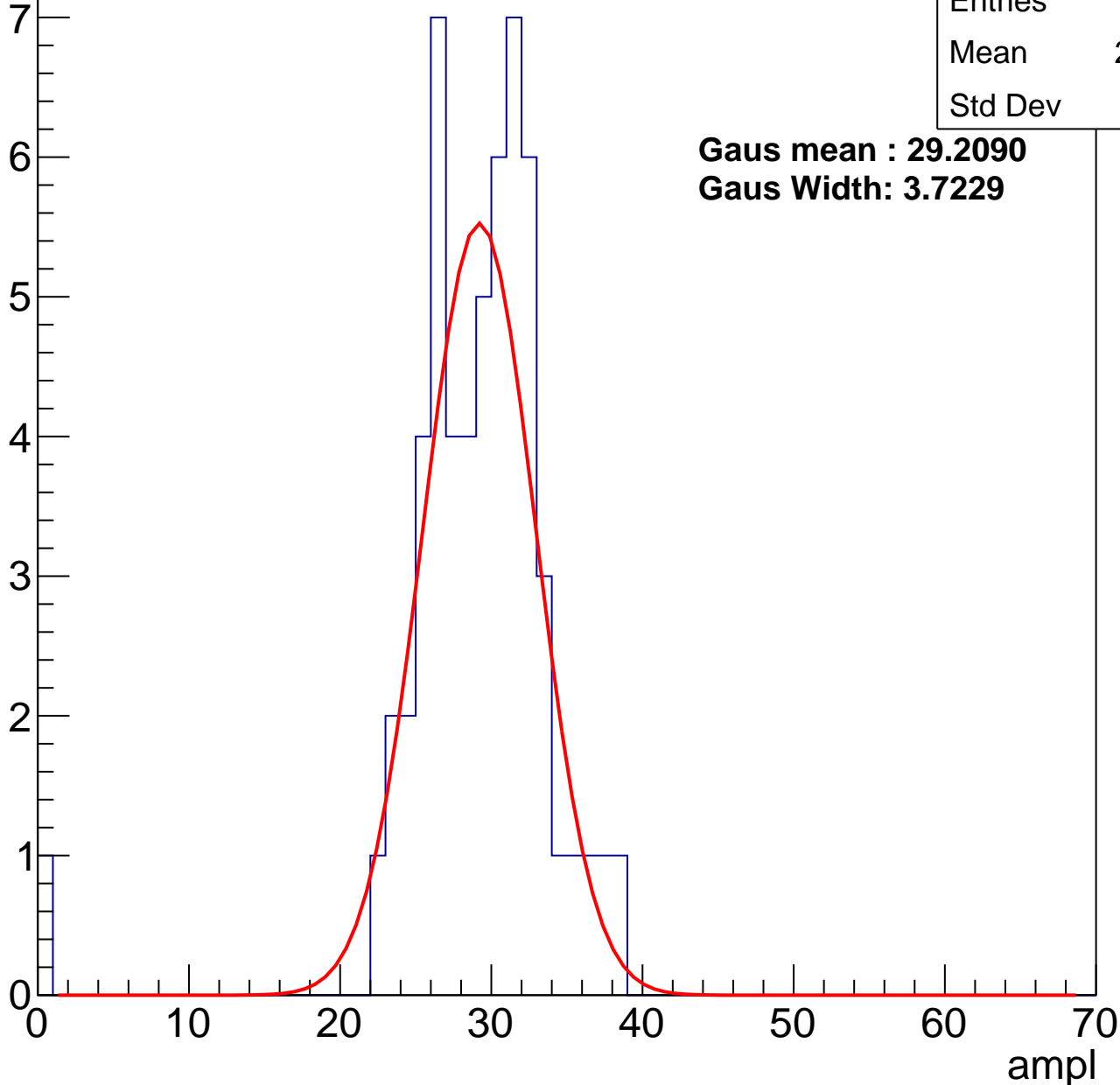
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	28.61
Std Dev	5.2

**Gaus mean : 29.2090**

**Gaus Width: 3.7229**



# B1L103S, U3-ch105, adc1

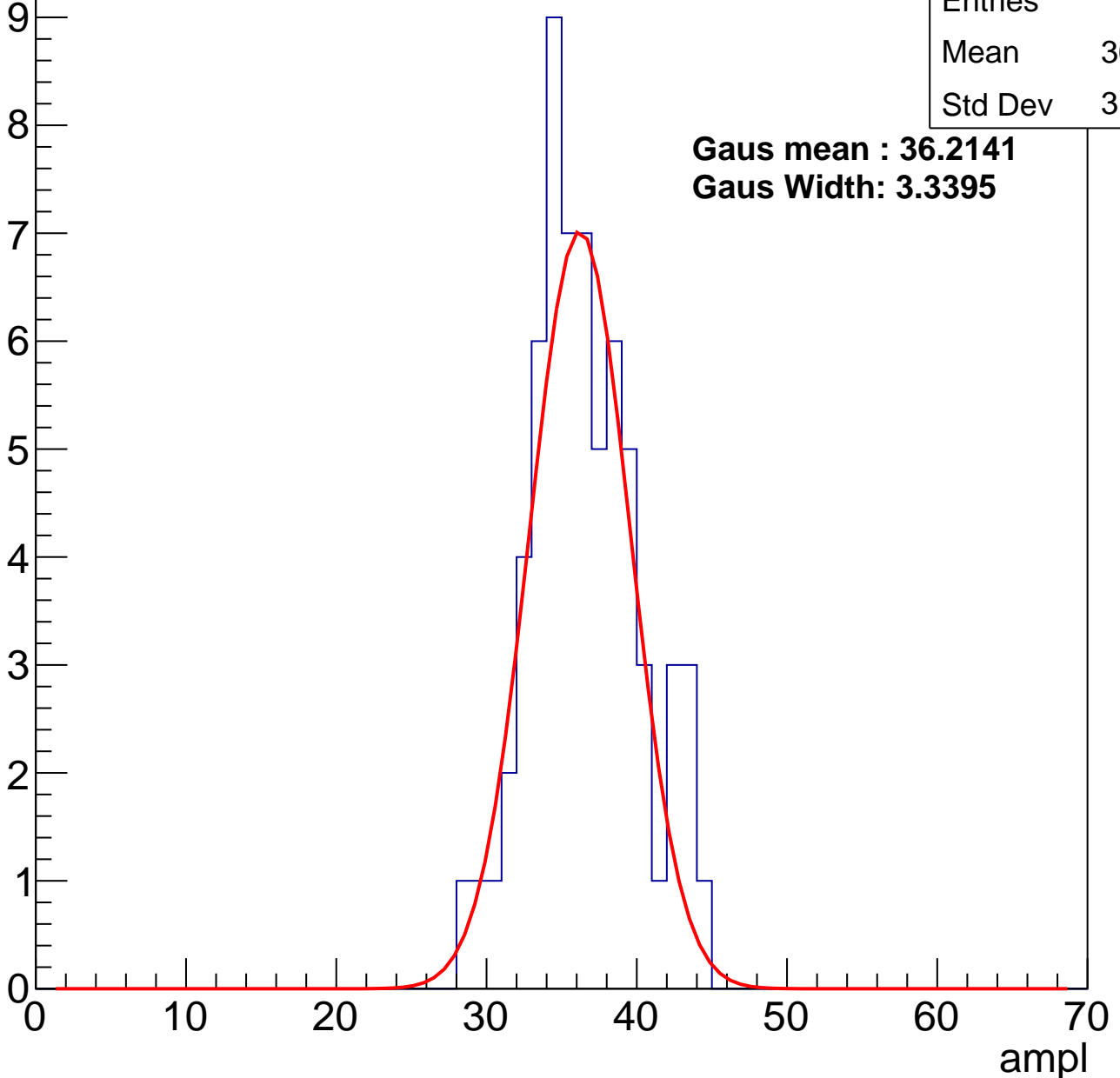
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	36.09
Std Dev	3.564

**Gaus mean : 36.2141**

**Gaus Width: 3.3395**



# B1L103S, U3-ch105, adc2

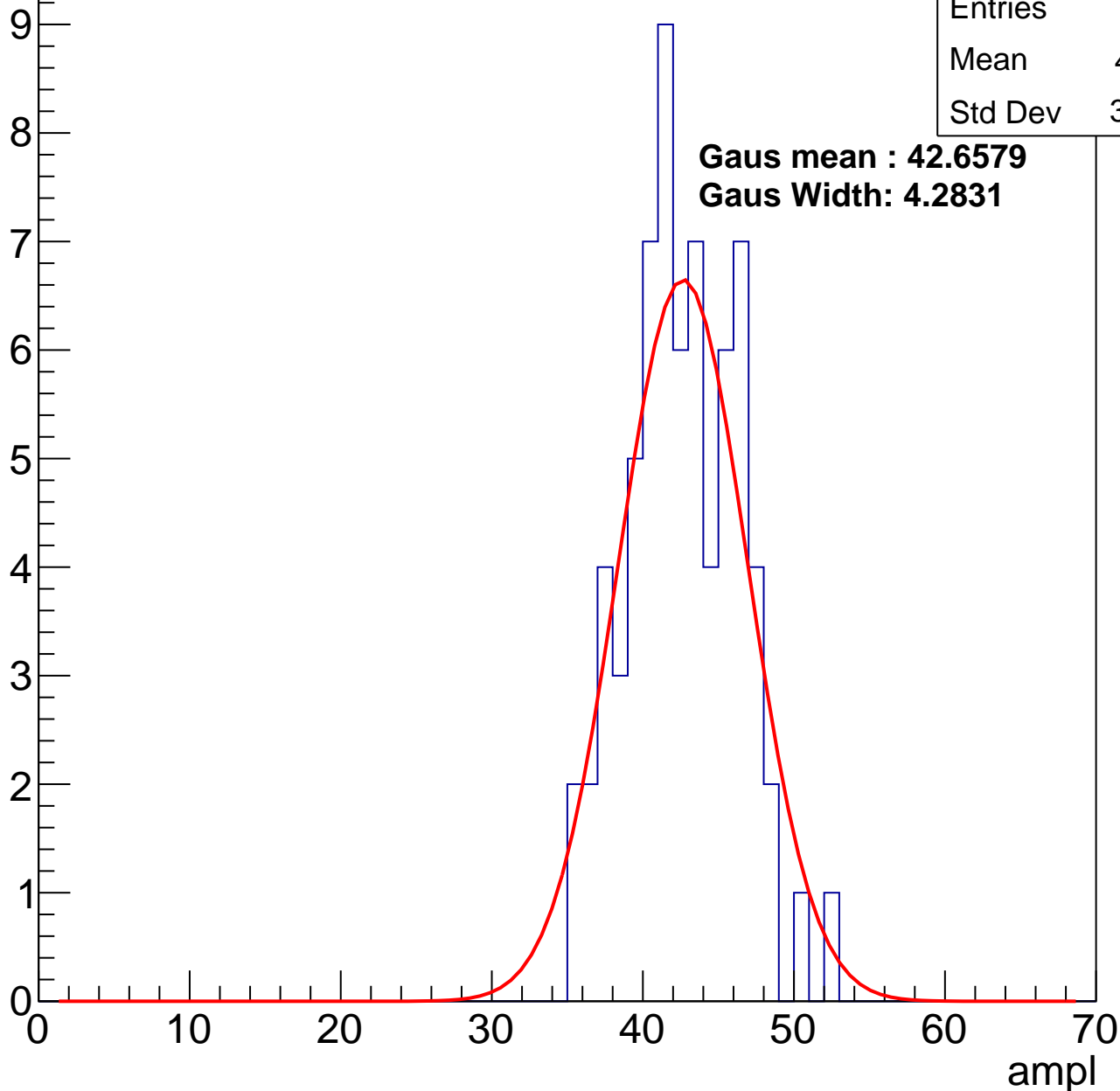
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	42.21
Std Dev	3.629

**Gaus mean : 42.6579**

**Gaus Width: 4.2831**



# B1L103S, U3-ch105, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	63
Mean	48.9
Std Dev	2.937

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

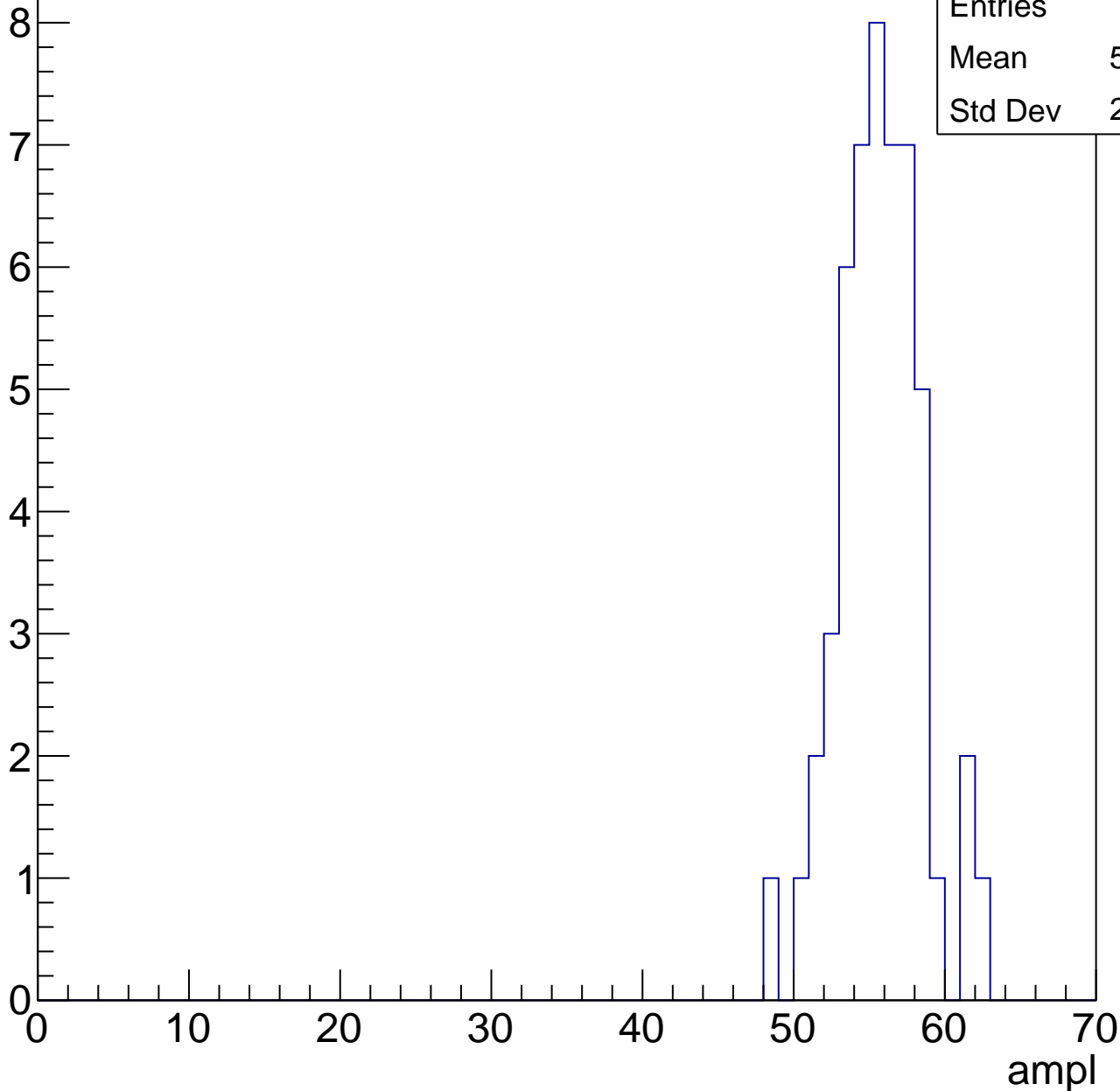
42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57

# B1L103S, U3-ch105, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	55.22
Std Dev	2.725

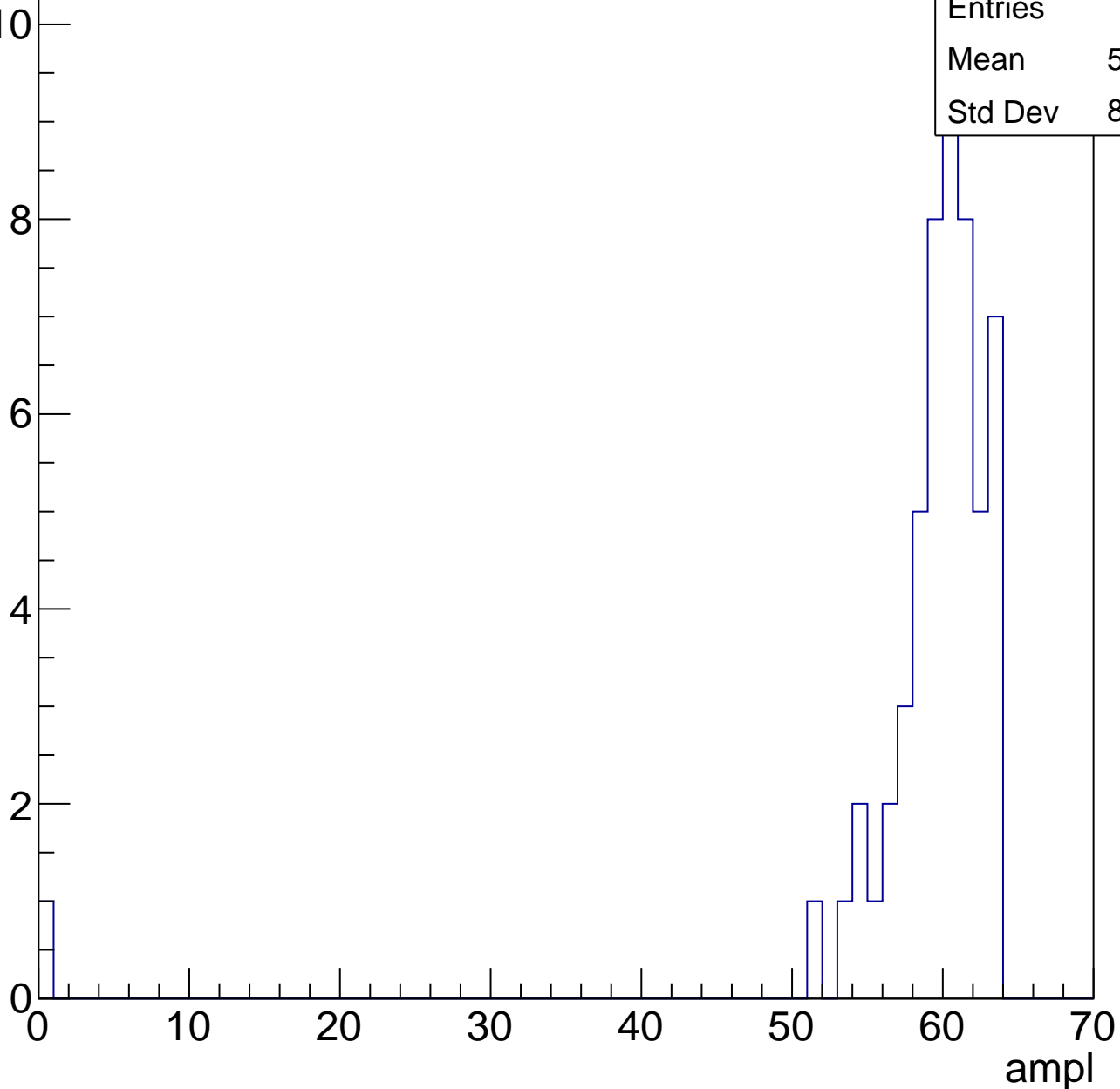


# B1L103S, U3-ch105, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

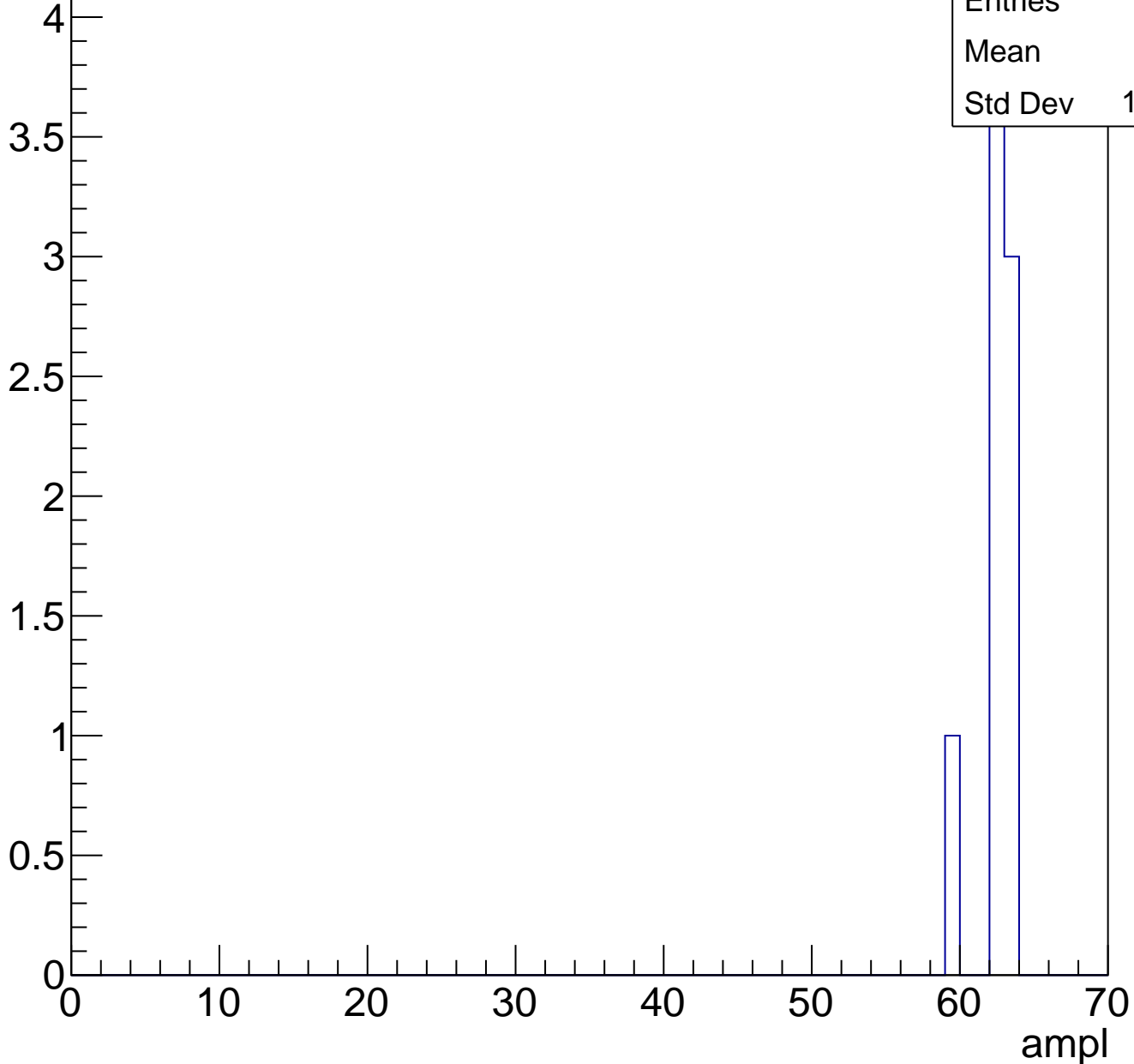
Entries	54
Mean	58.35
Std Dev	8.453



# B1L103S, U3-ch105, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

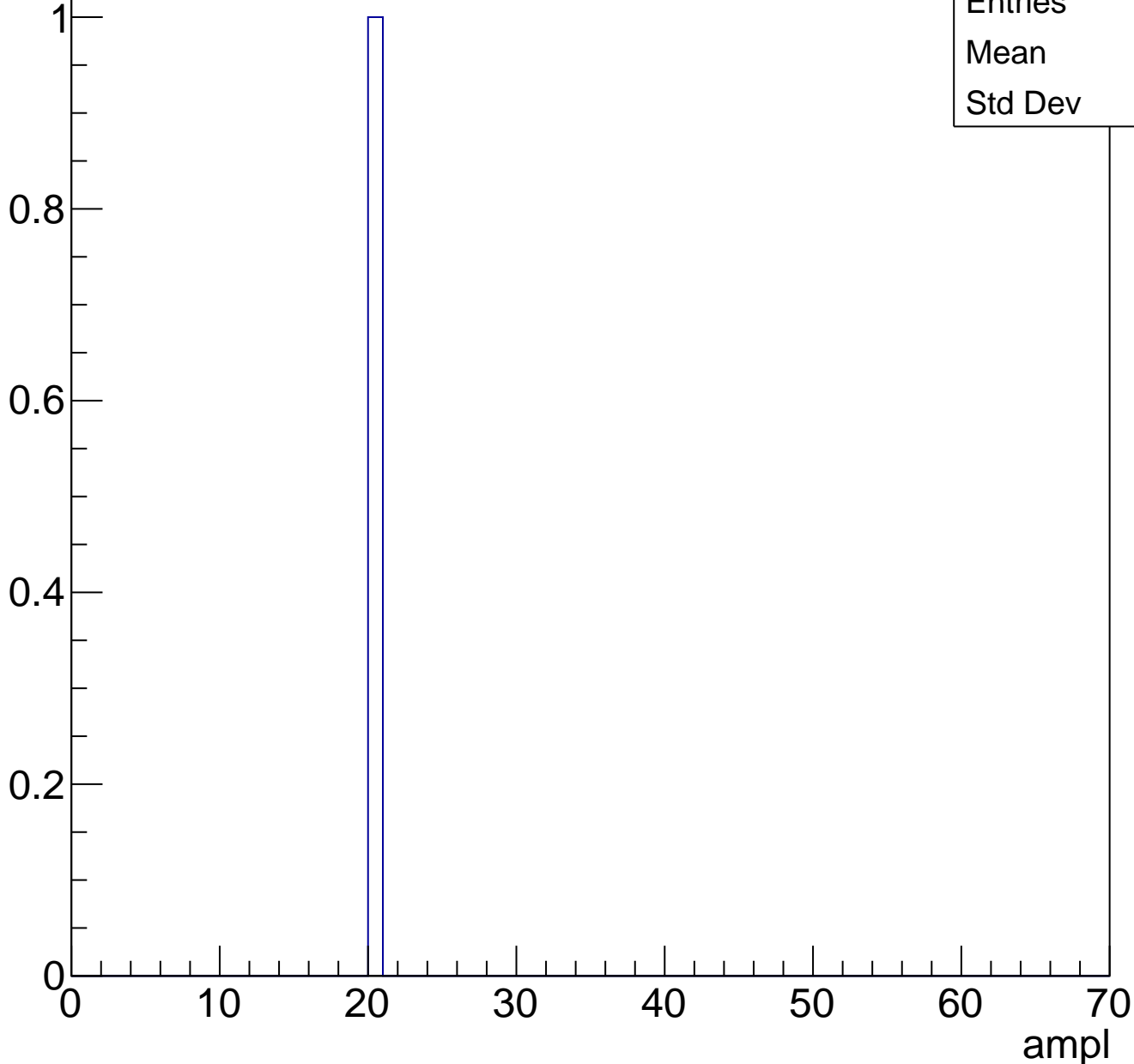




# B1L103S, U3-ch105, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	20
Std Dev	0

# B1L103S, U3-ch106, adc0

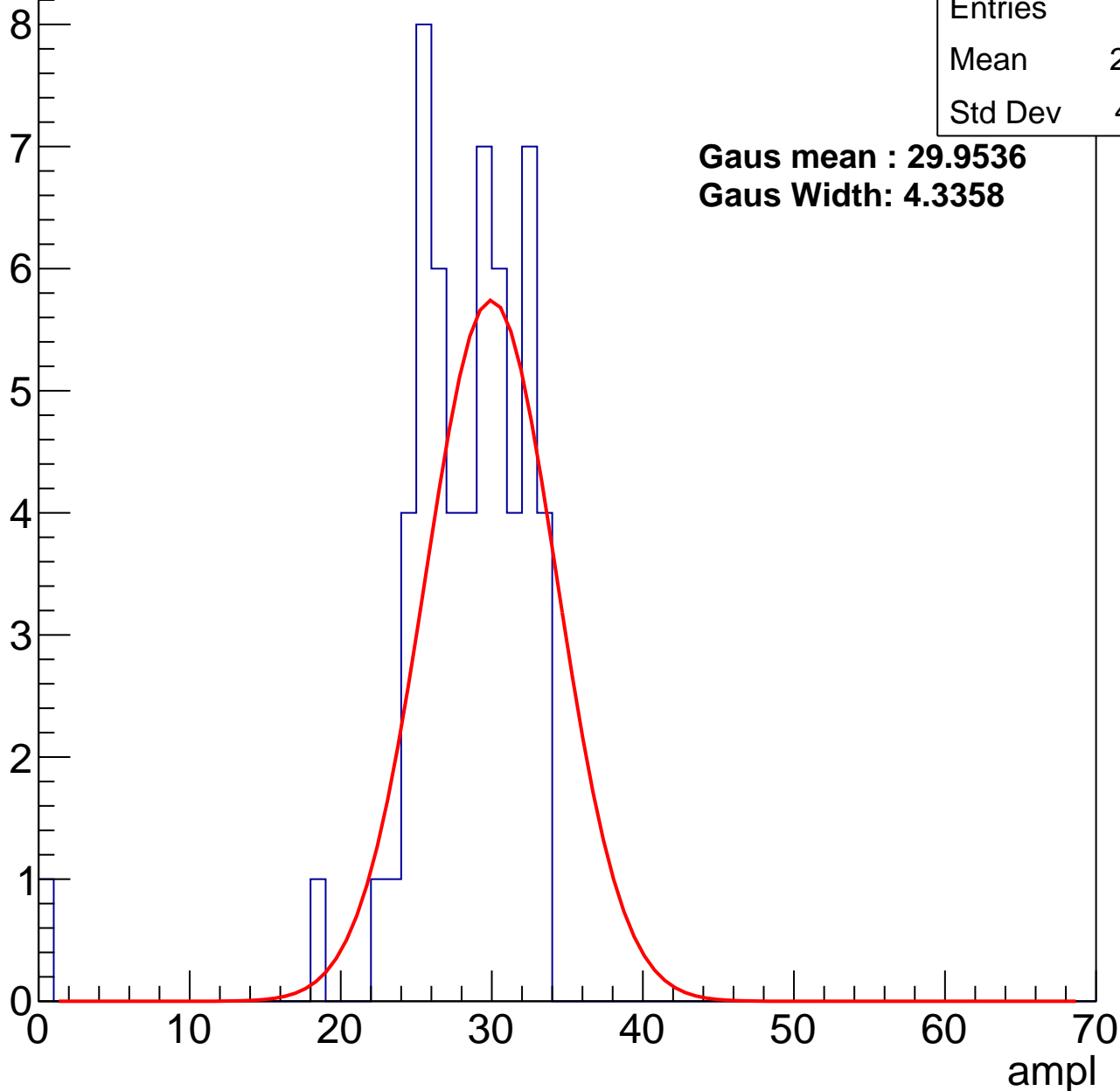
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	27.55
Std Dev	4.871

**Gaus mean : 29.9536**

**Gaus Width: 4.3358**



# B1L103S, U3-ch106, adc1

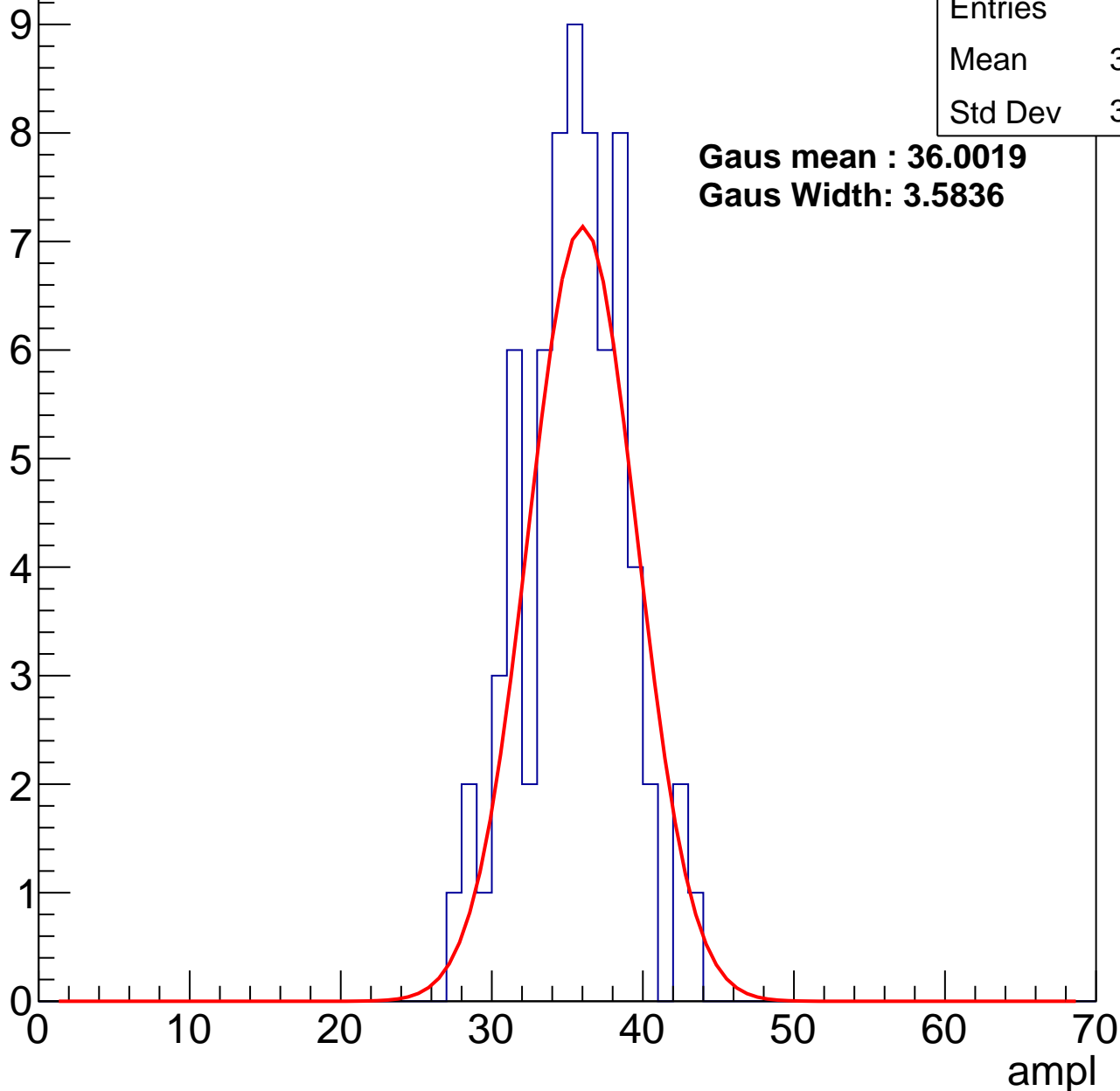
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	34.99
Std Dev	3.403

**Gaus mean : 36.0019**

**Gaus Width: 3.5836**



# B1L103S, U3-ch106, adc2

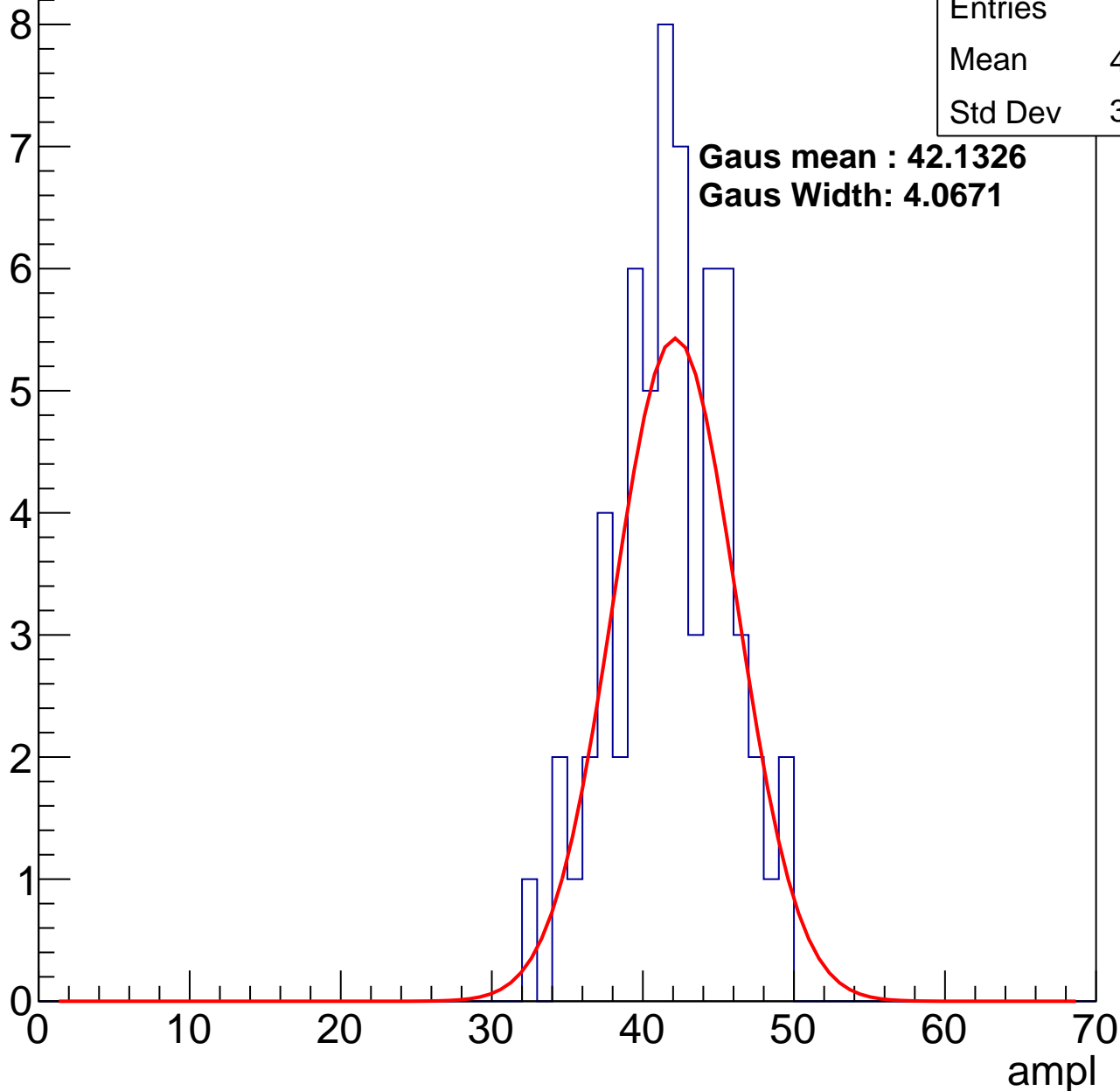
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	41.44
Std Dev	3.748

**Gaus mean : 42.1326**

**Gaus Width: 4.0671**

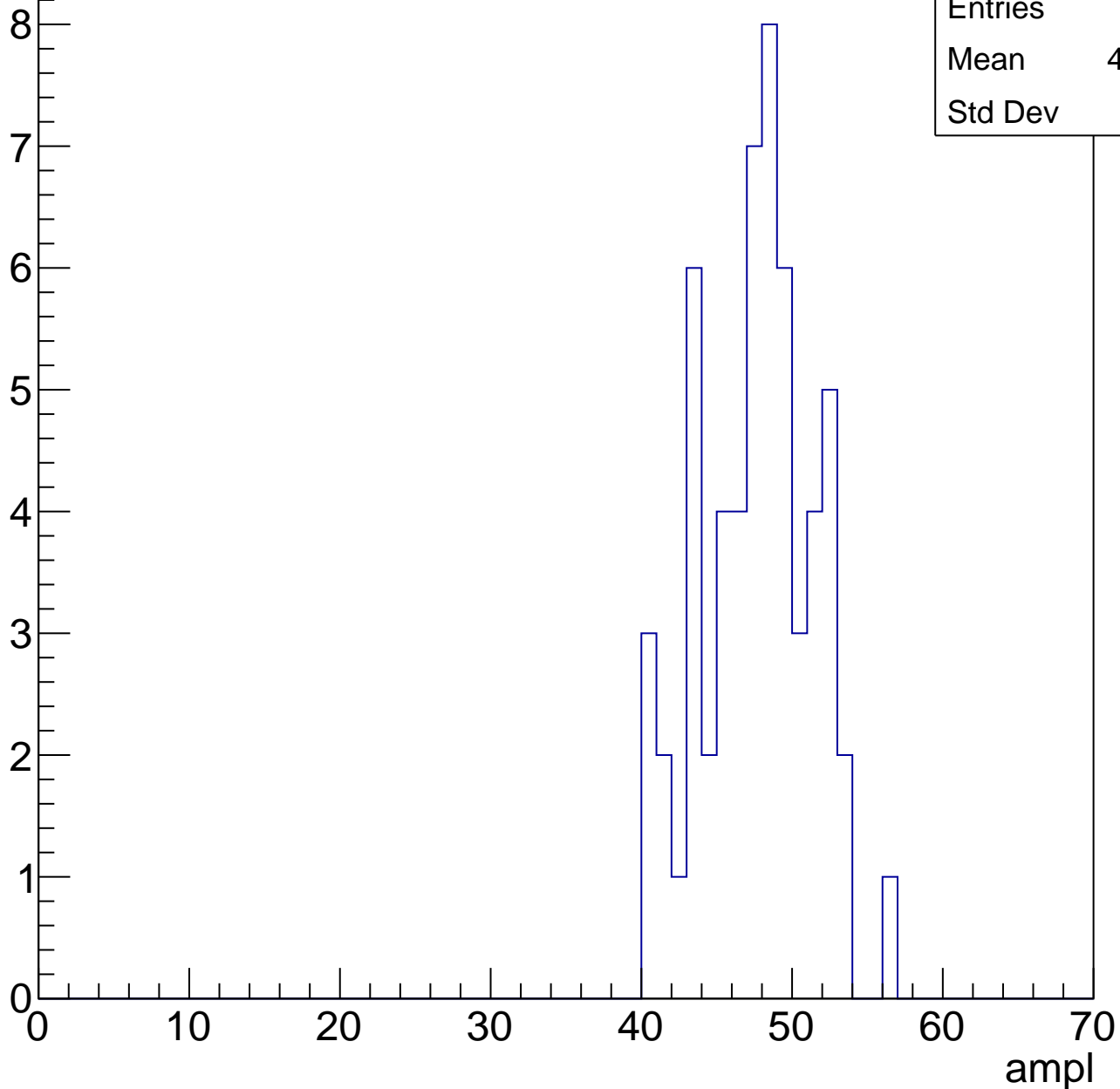


# B1L103S, U3-ch106, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	47.19
Std Dev	3.66

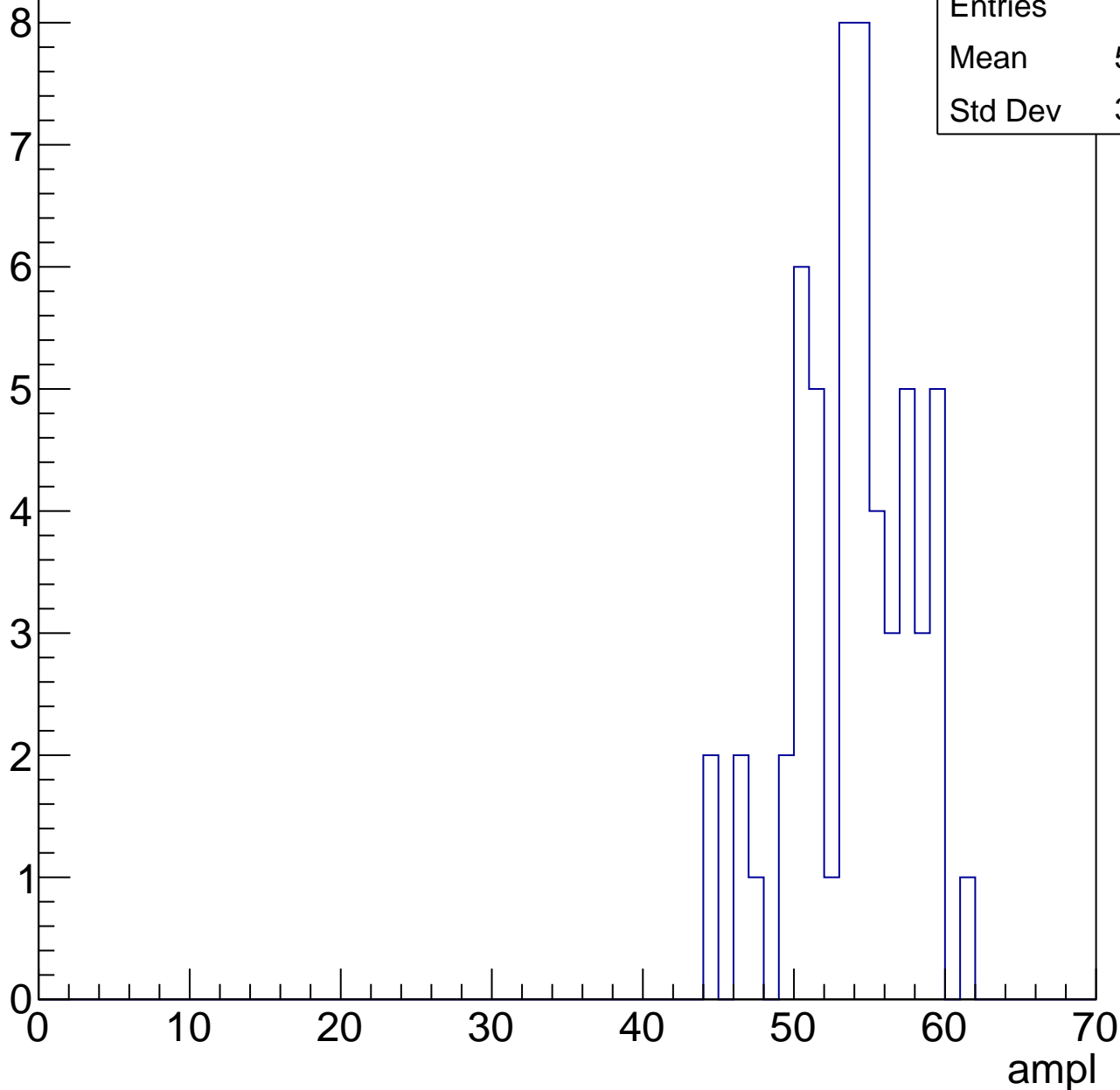


# B1L103S, U3-ch106, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	53.41
Std Dev	3.881

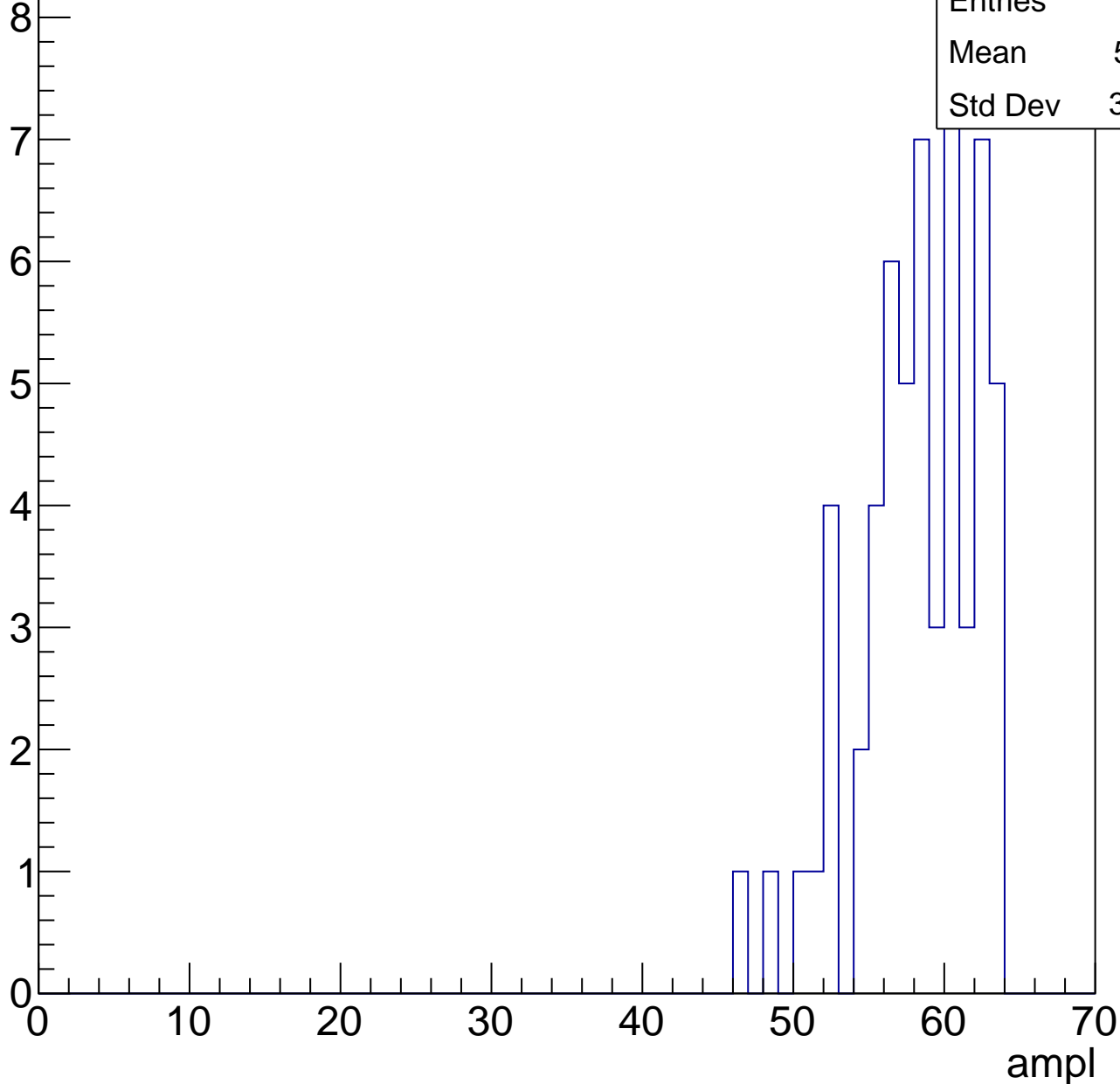


# B1L103S, U3-ch106, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	57.71
Std Dev	3.922

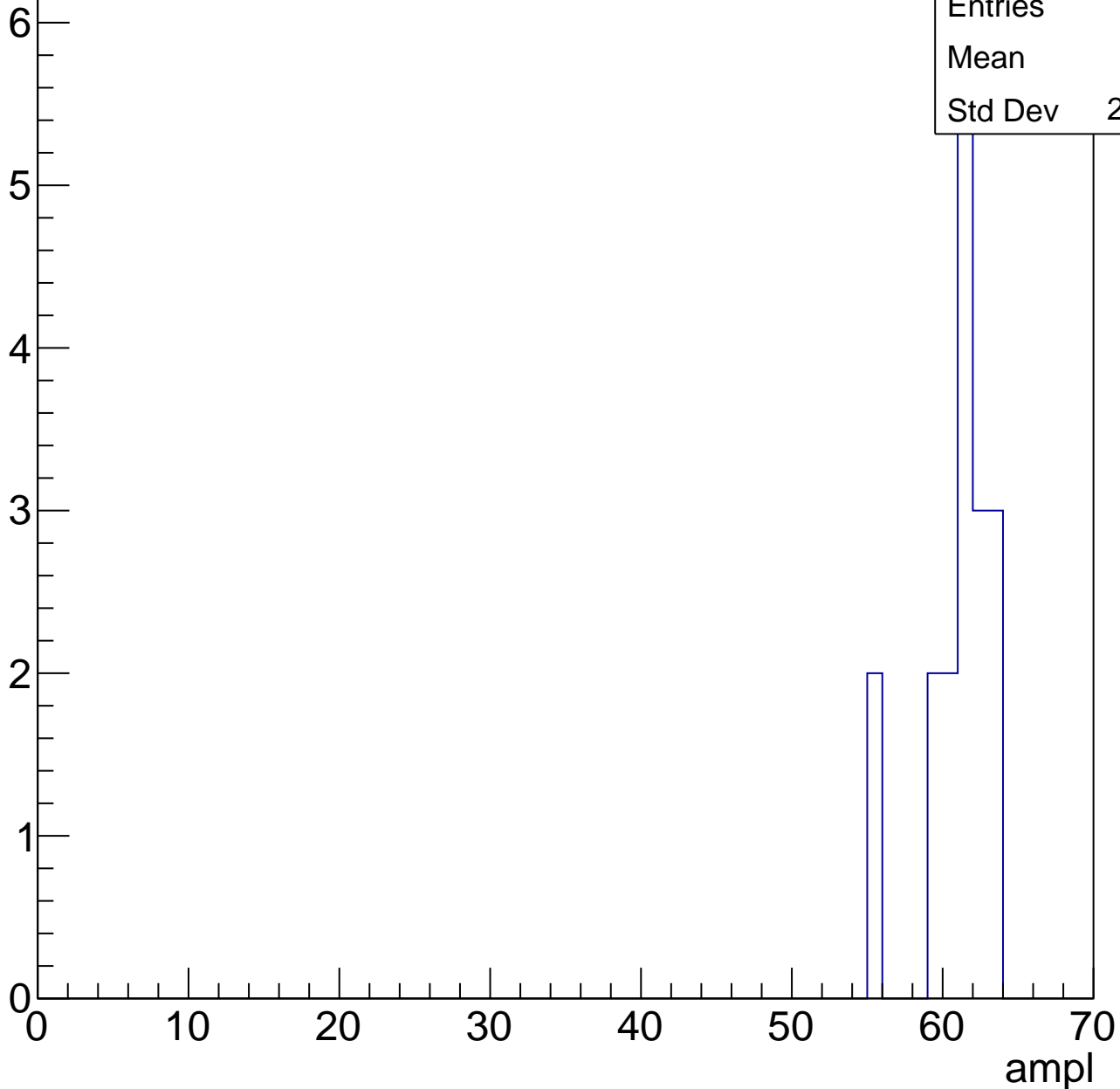


# B1L103S, U3-ch106, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	18
Mean	60.5
Std Dev	2.267

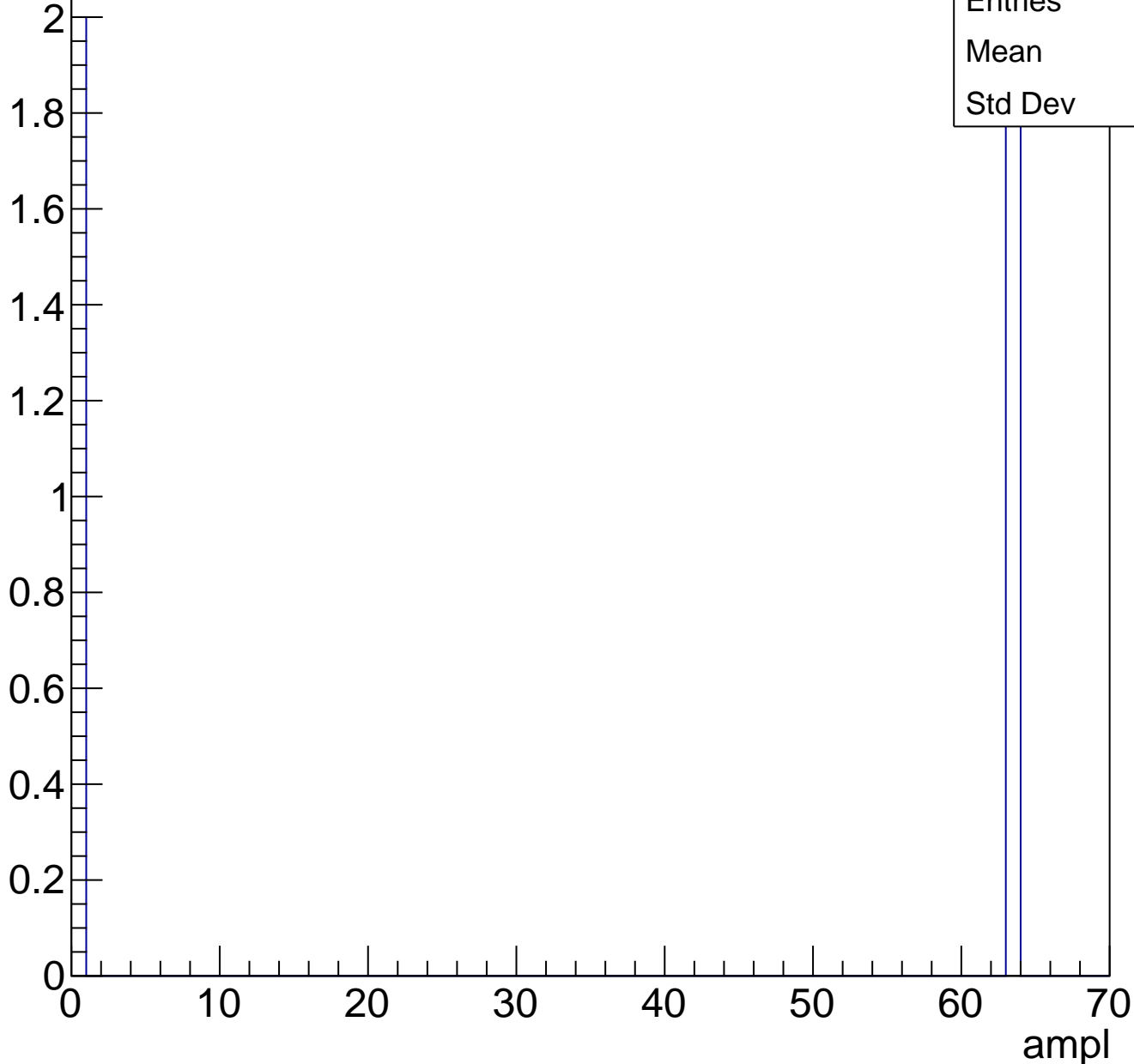




# B1L103S, U3-ch106, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch107, adc0

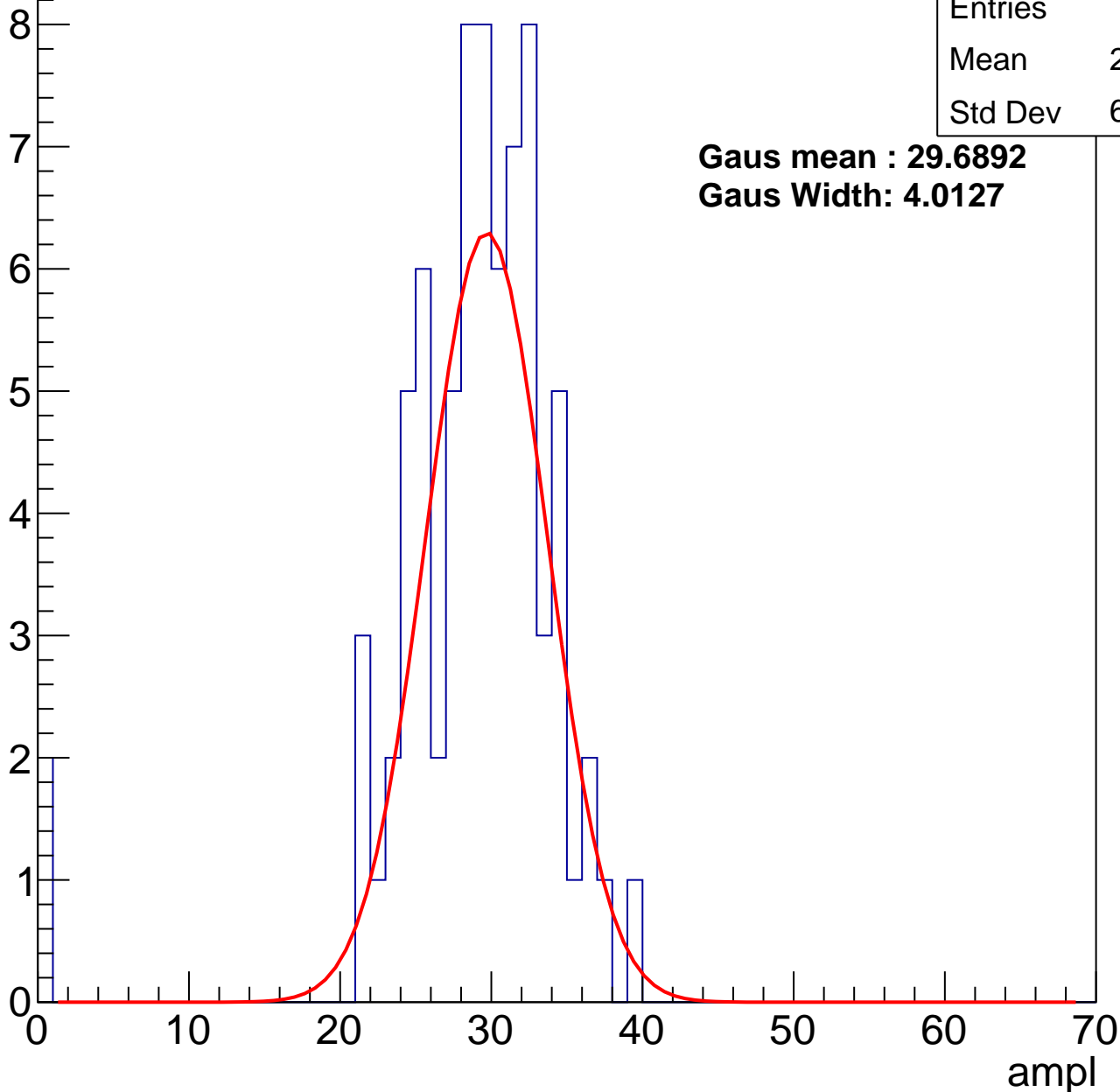
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	28.28
Std Dev	6.069

**Gaus mean : 29.6892**

**Gaus Width: 4.0127**



# B1L103S, U3-ch107, adc1

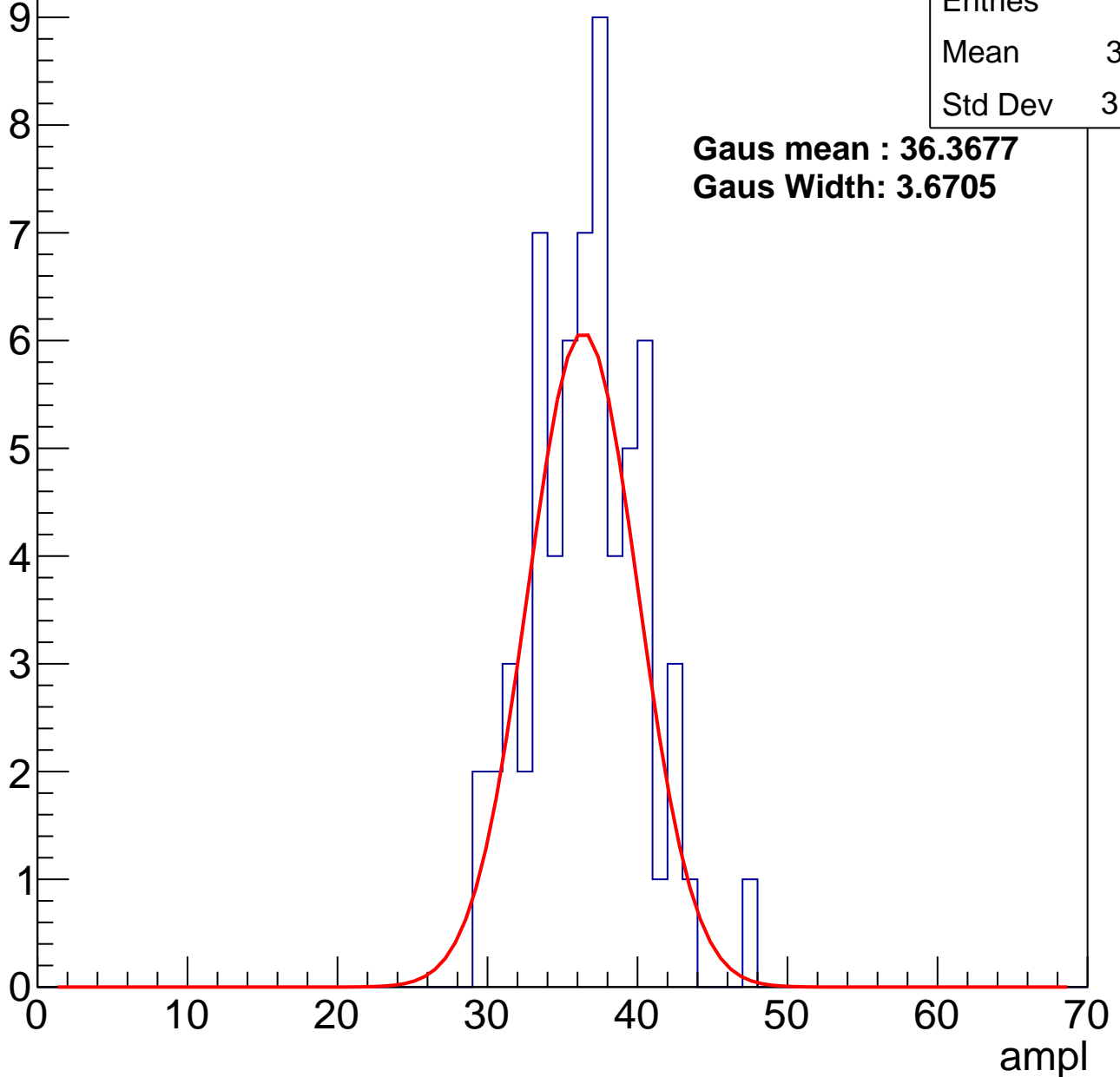
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	36.21
Std Dev	3.626

**Gaus mean : 36.3677**

**Gaus Width: 3.6705**



# B1L103S, U3-ch107, adc2

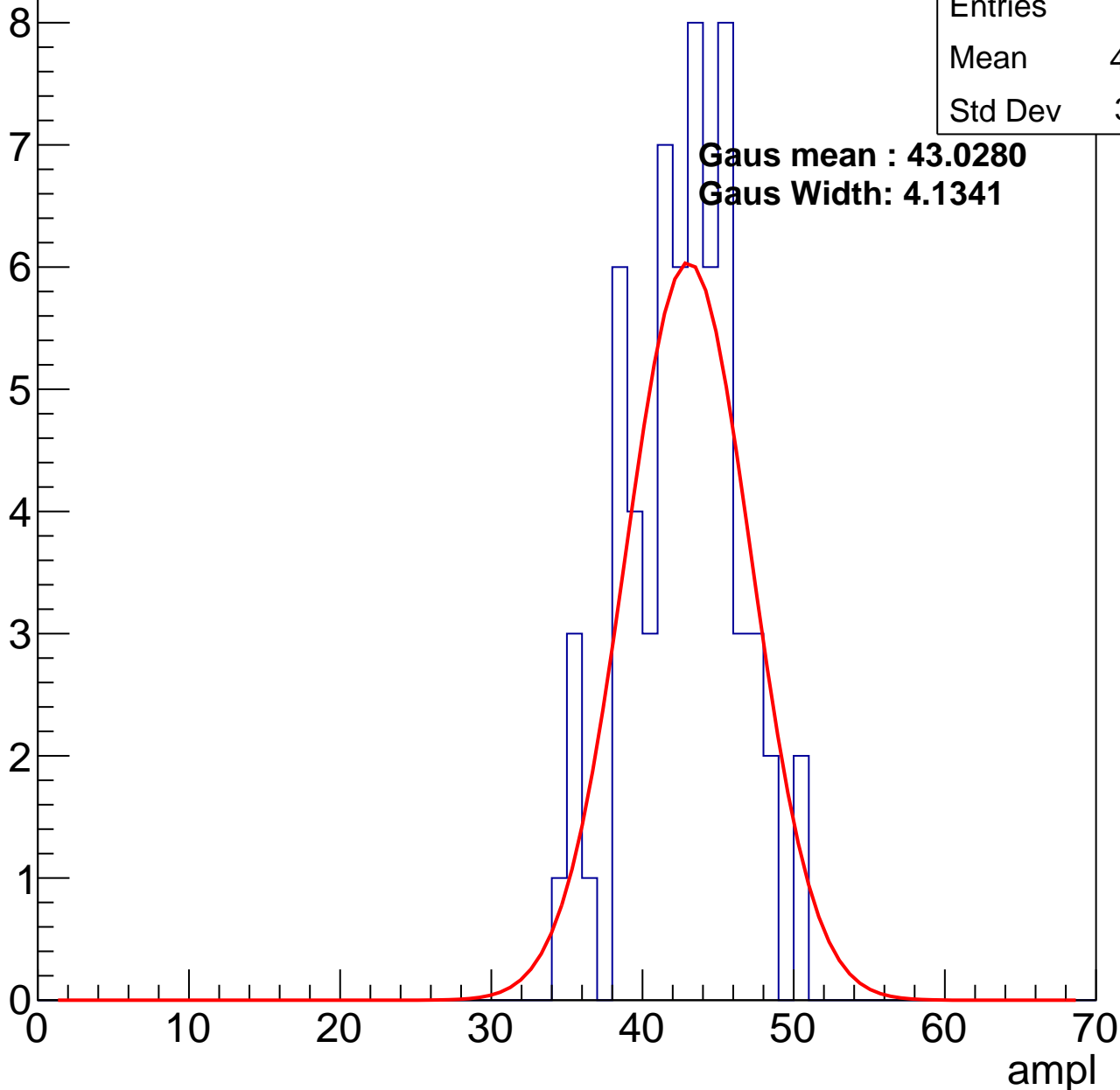
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	42.24
Std Dev	3.611

**Gaus mean : 43.0280**

**Gaus Width: 4.1341**

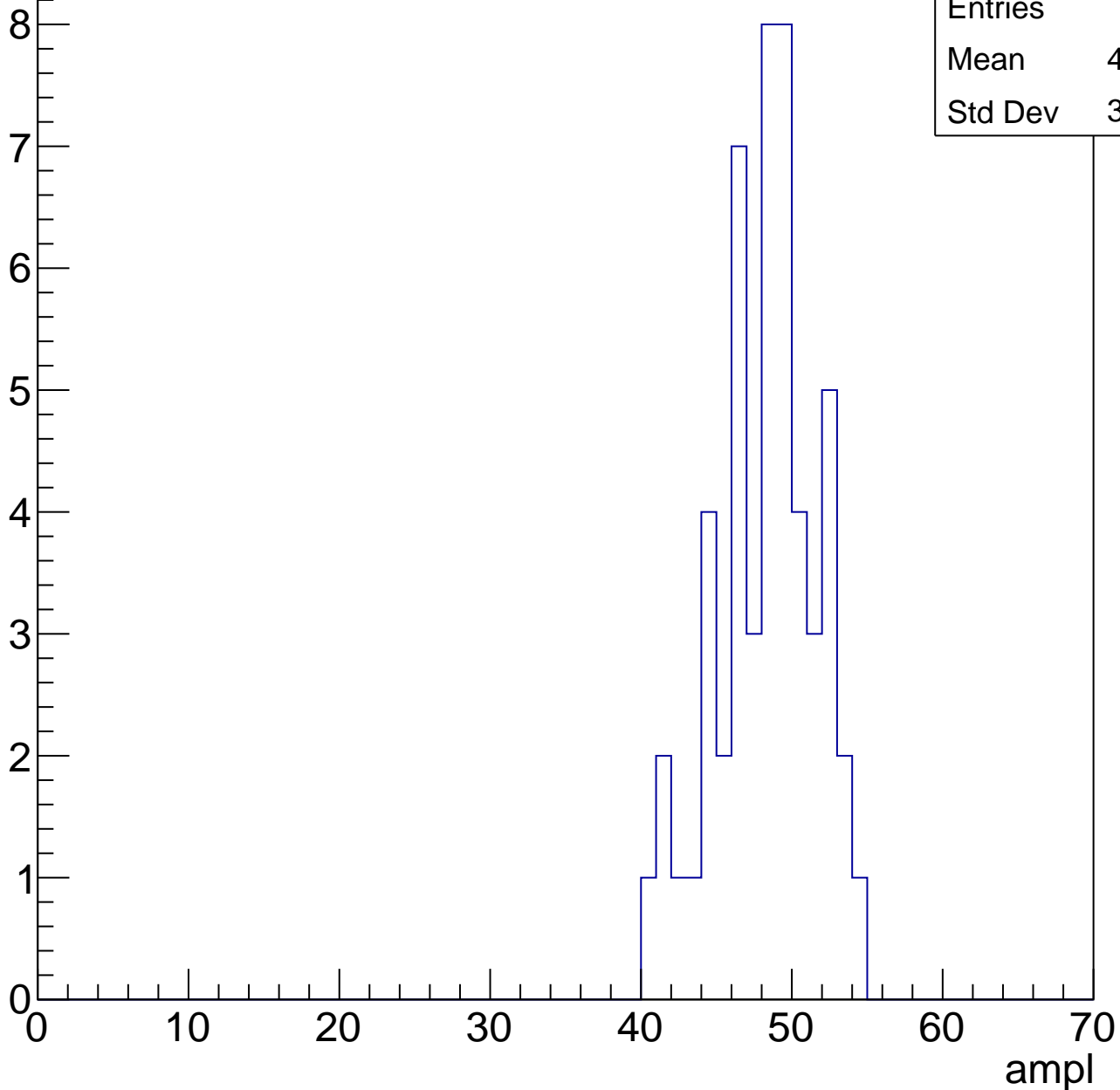


# B1L103S, U3-ch107, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	47.79
Std Dev	3.254

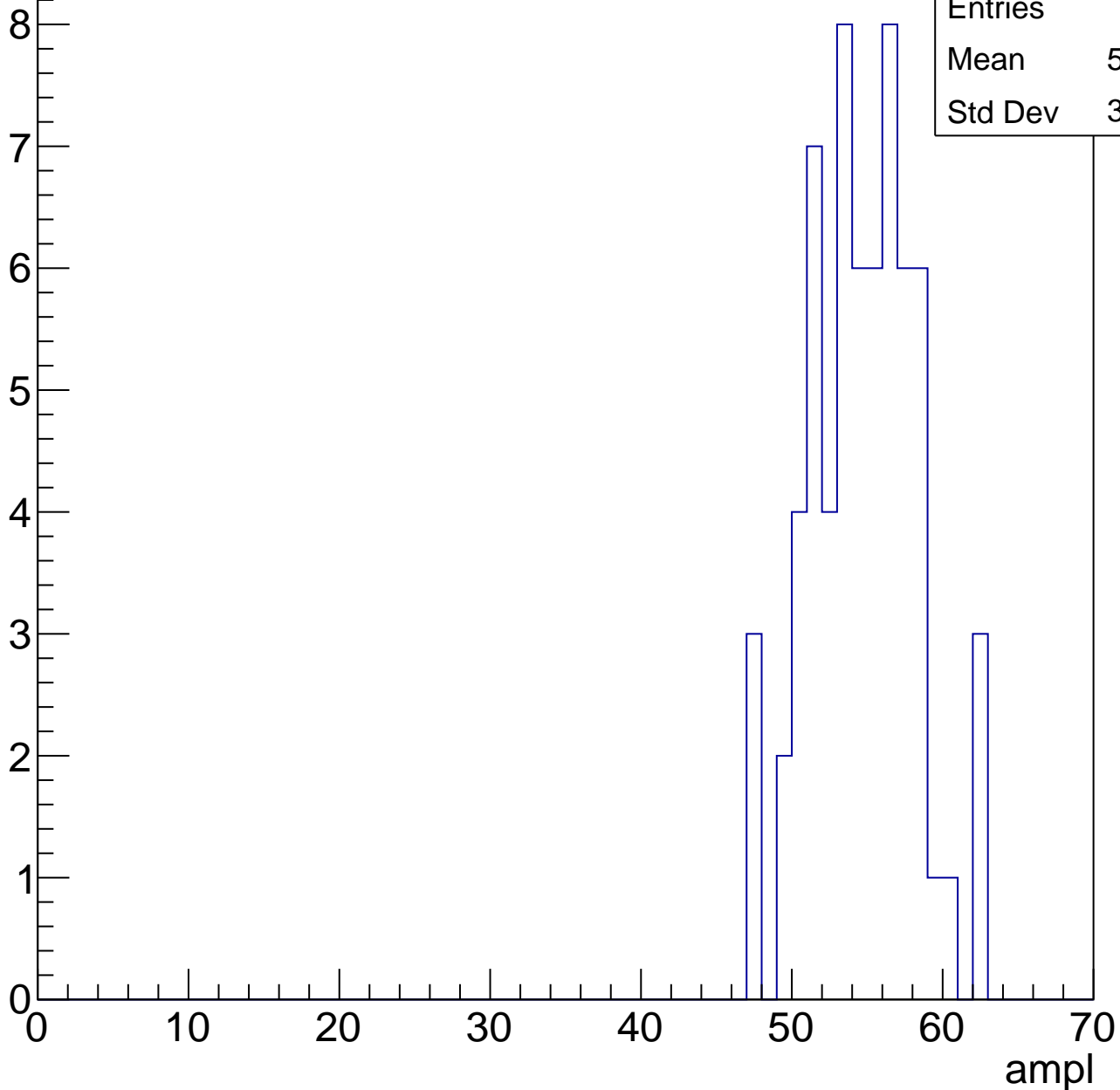


# B1L103S, U3-ch107, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	54.23
Std Dev	3.476



# B1L103S, U3-ch107, adc5

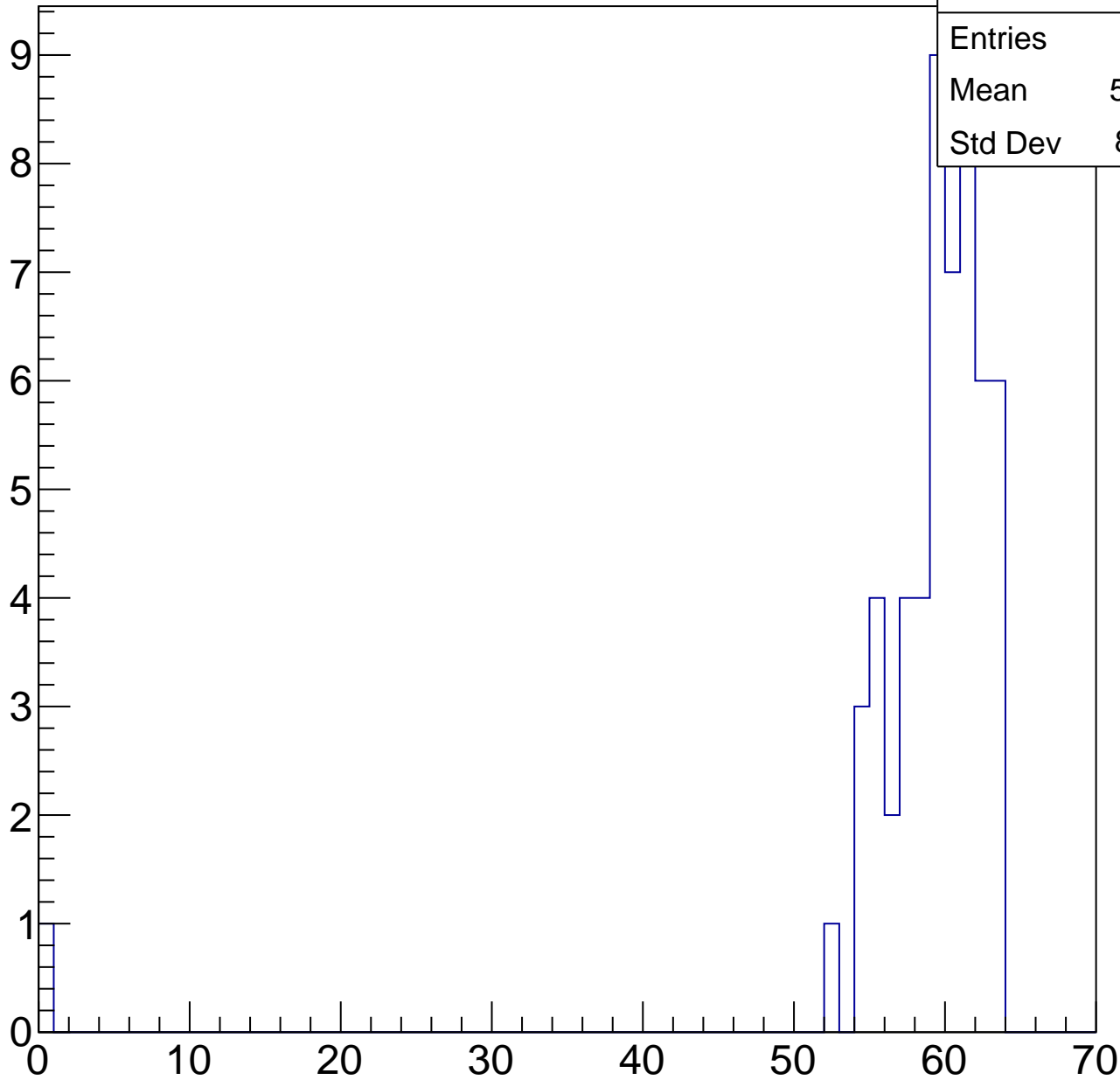
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	56
Mean	58.14
Std Dev	8.301

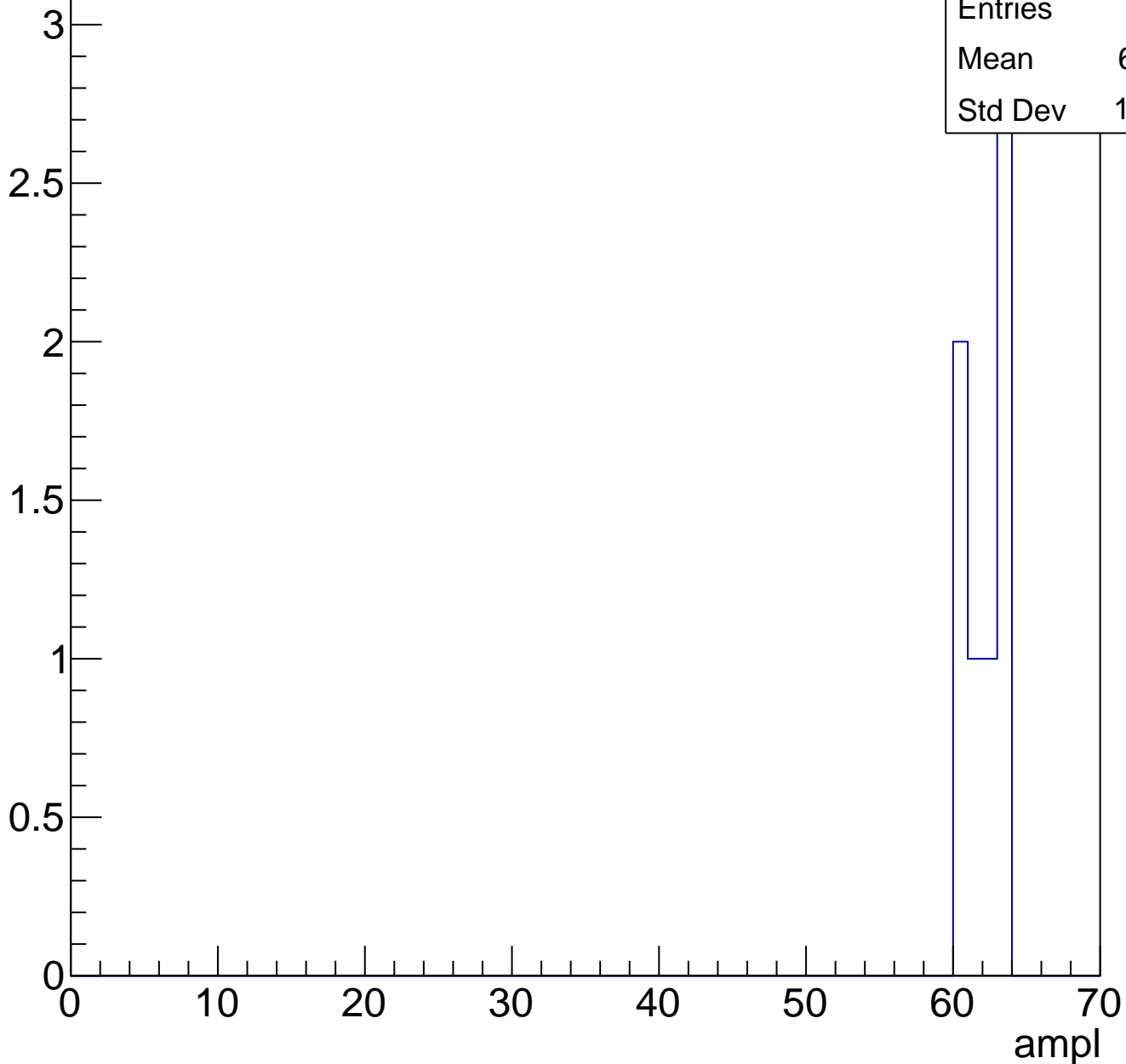
ampl



# B1L103S, U3-ch107, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U3-ch107, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch108, adc0

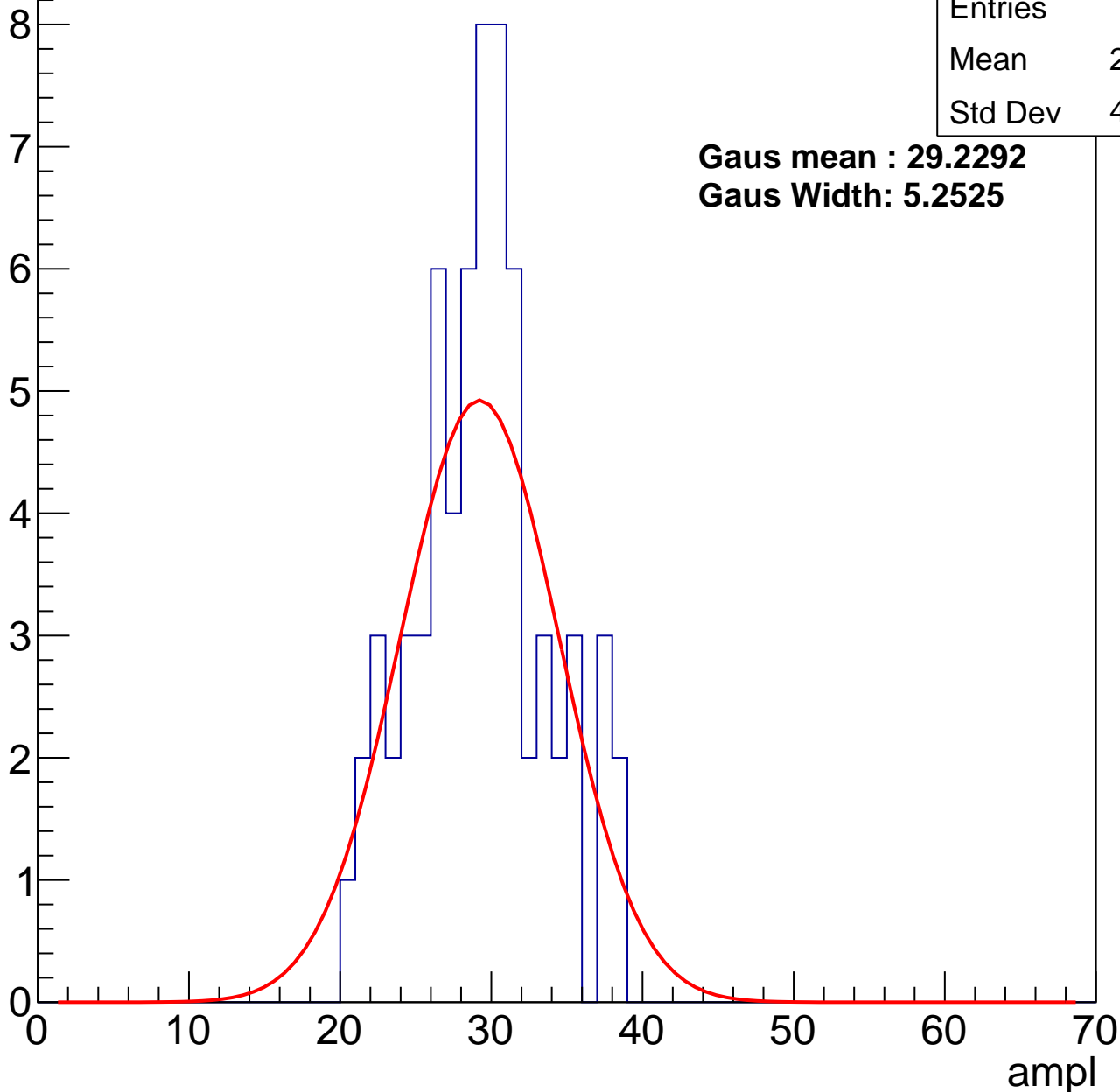
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	28.87
Std Dev	4.295

**Gaus mean : 29.2292**

**Gaus Width: 5.2525**



# B1L103S, U3-ch108, adc1

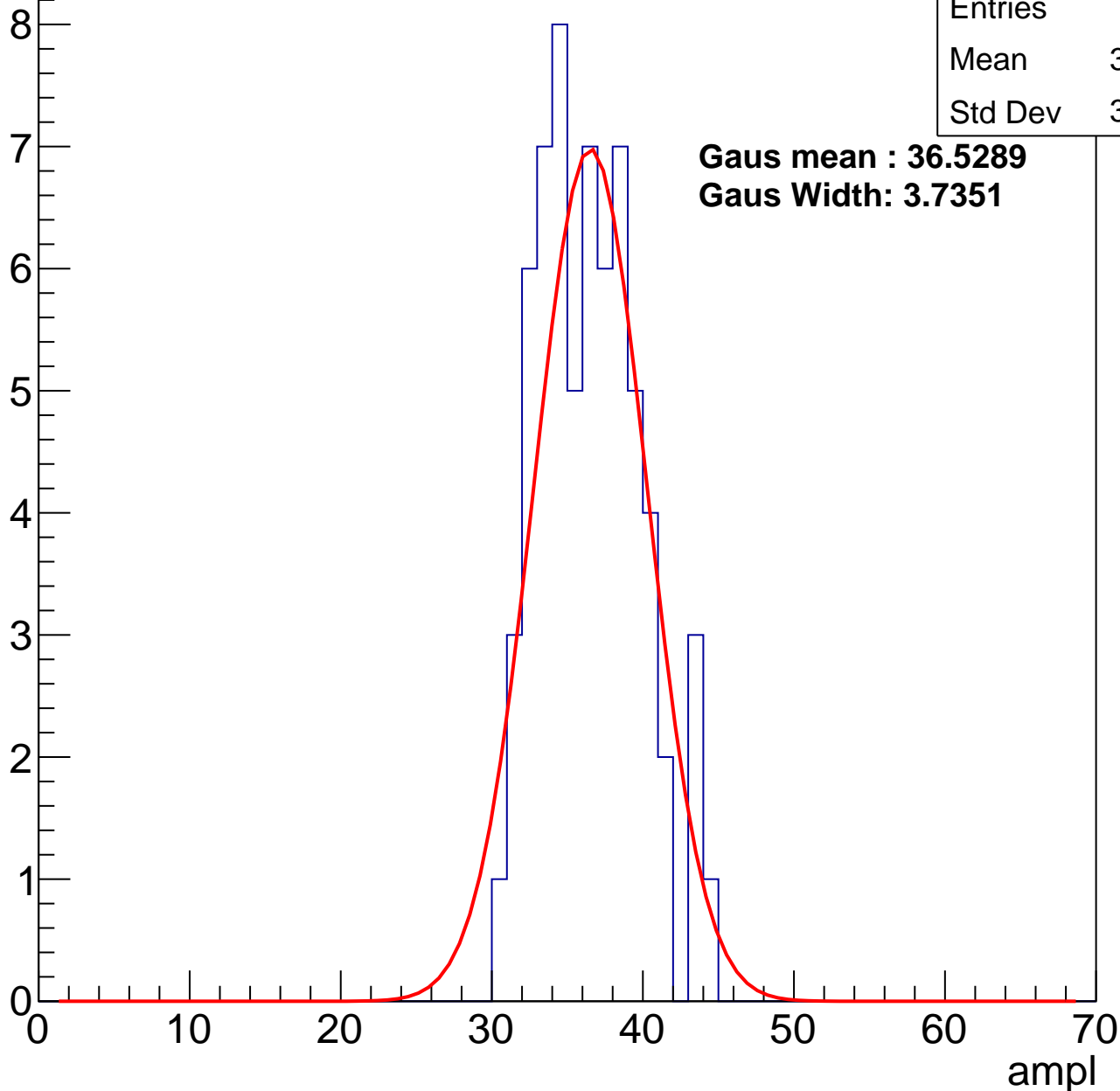
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	36.05
Std Dev	3.307

**Gaus mean : 36.5289**

**Gaus Width: 3.7351**



# B1L103S, U3-ch108, adc2

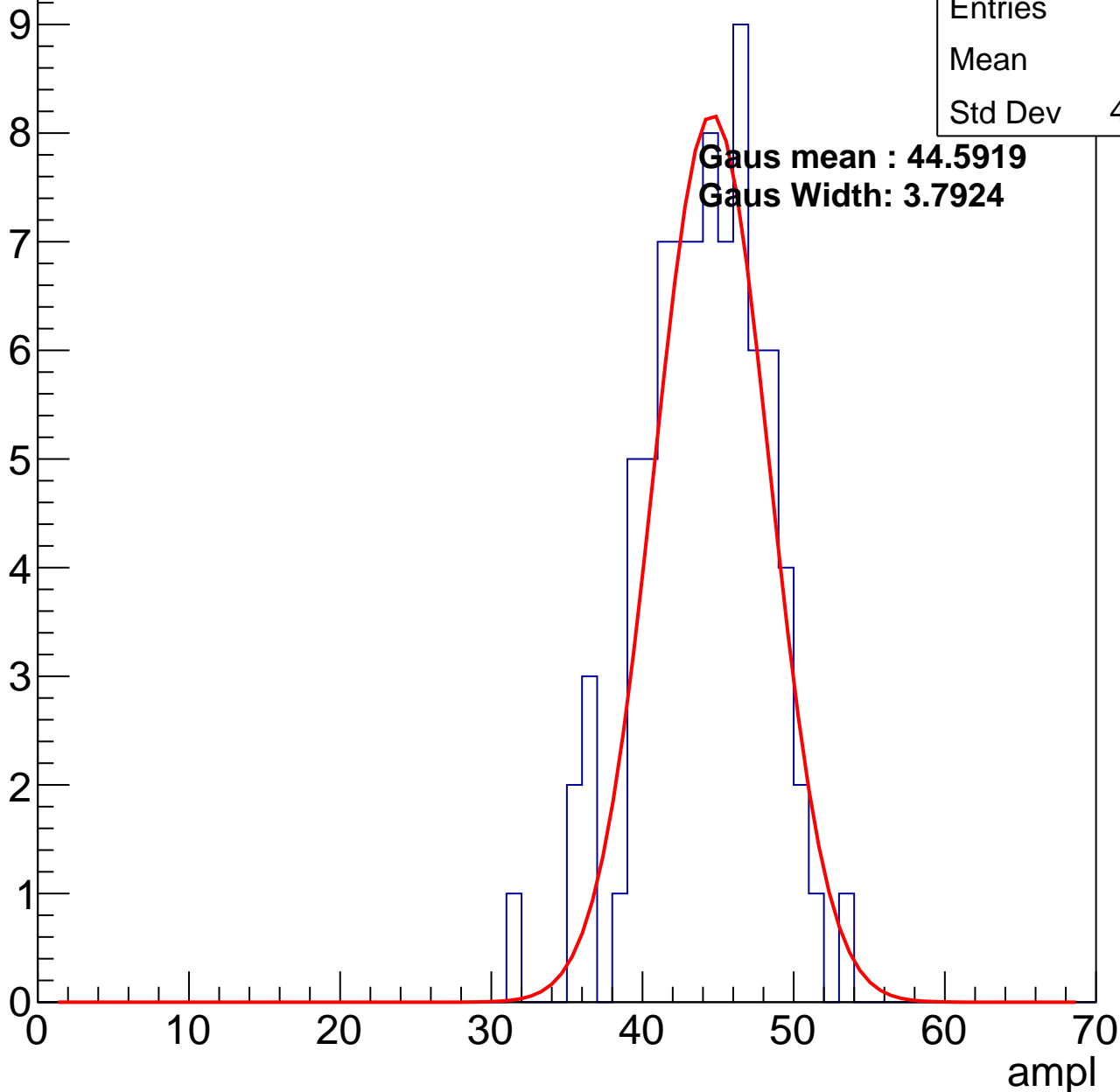
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	82
Mean	43.6
Std Dev	4.048

**Gaus mean : 44.5919**

**Gaus Width: 3.7924**

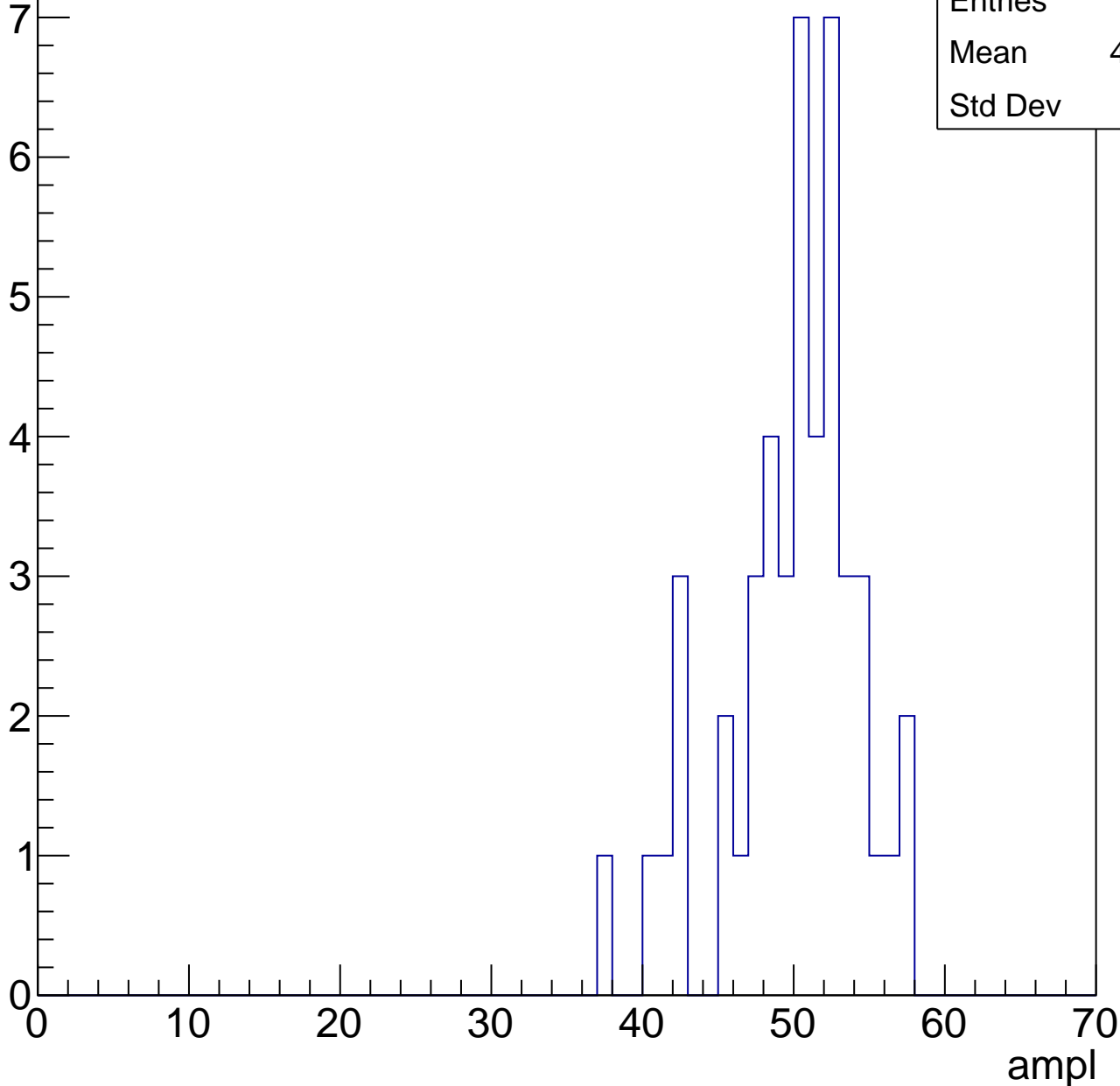


# B1L103S, U3-ch108, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

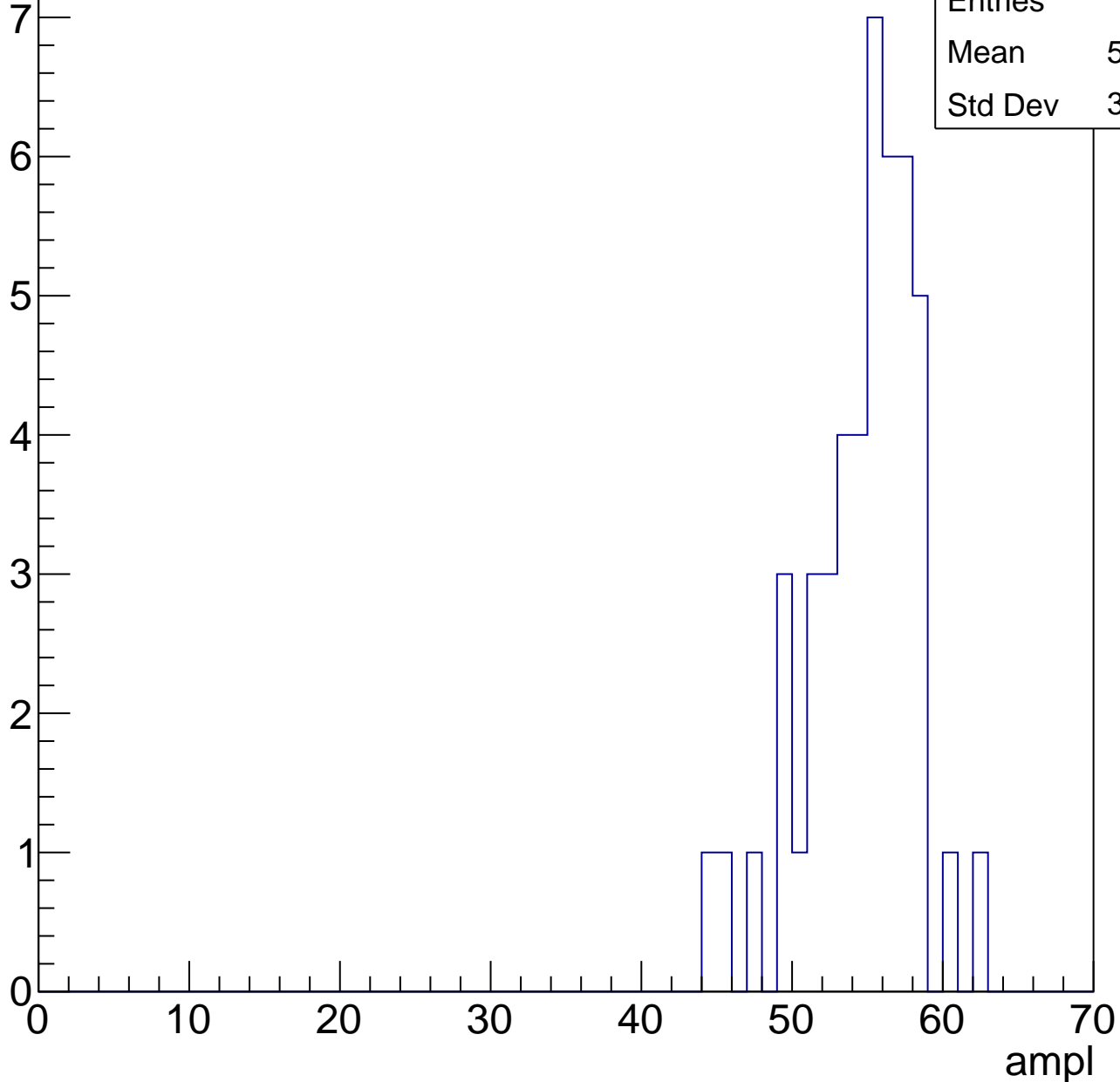
Entries	47
Mean	49.45
Std Dev	4.39



# B1L103S, U3-ch108, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch108, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	63
Mean	58.27
Std Dev	8.01

Entry

10

8

6

4

2

0

0

10

20

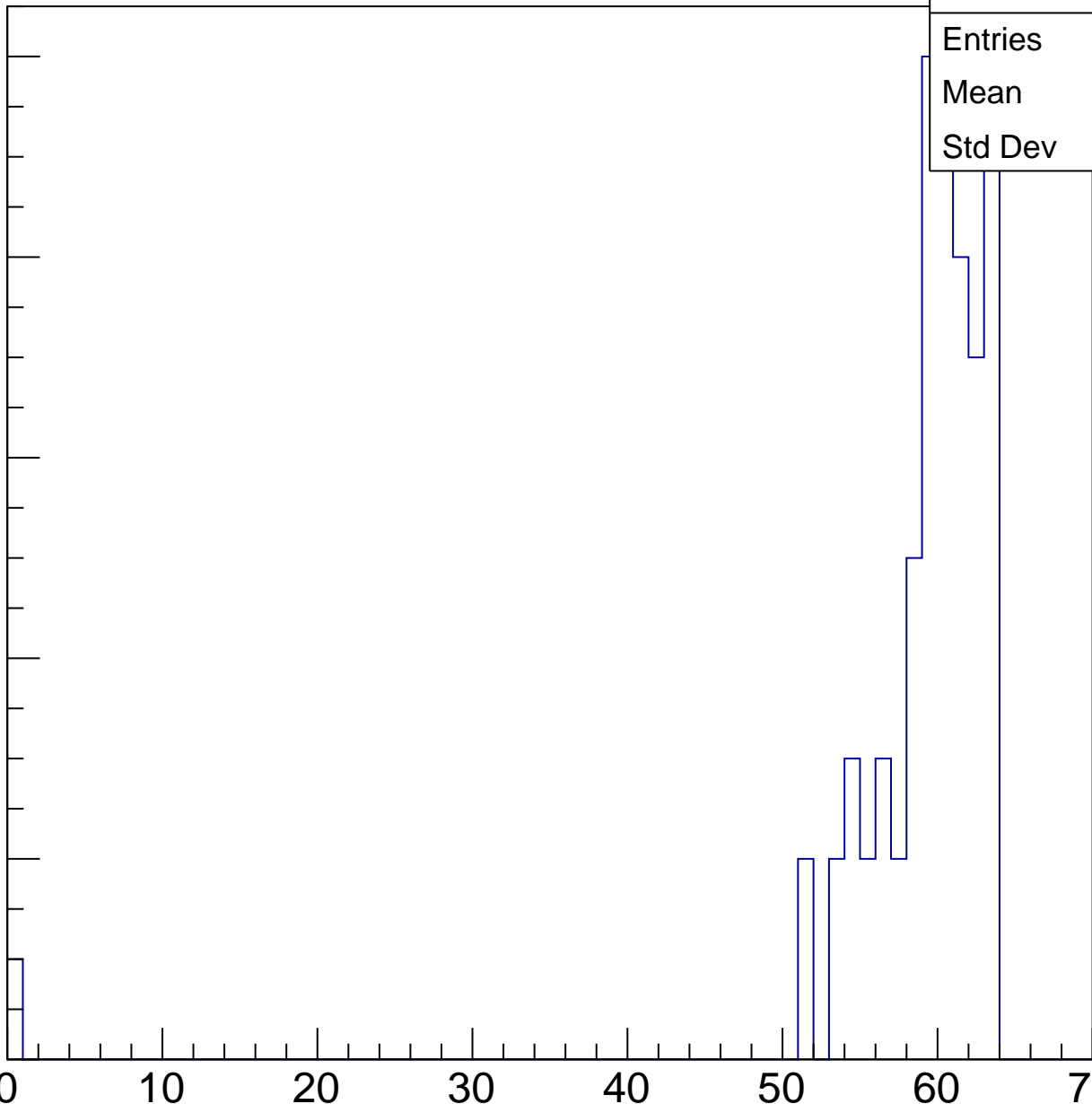
30

40

50

60

ampl



# B1L103S, U3-ch108, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	61.8
Std Dev	0.7483

ampl

0 10 20 30 40 50 60 70



# B1L103S, U3-ch108, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U3-ch109, adc0

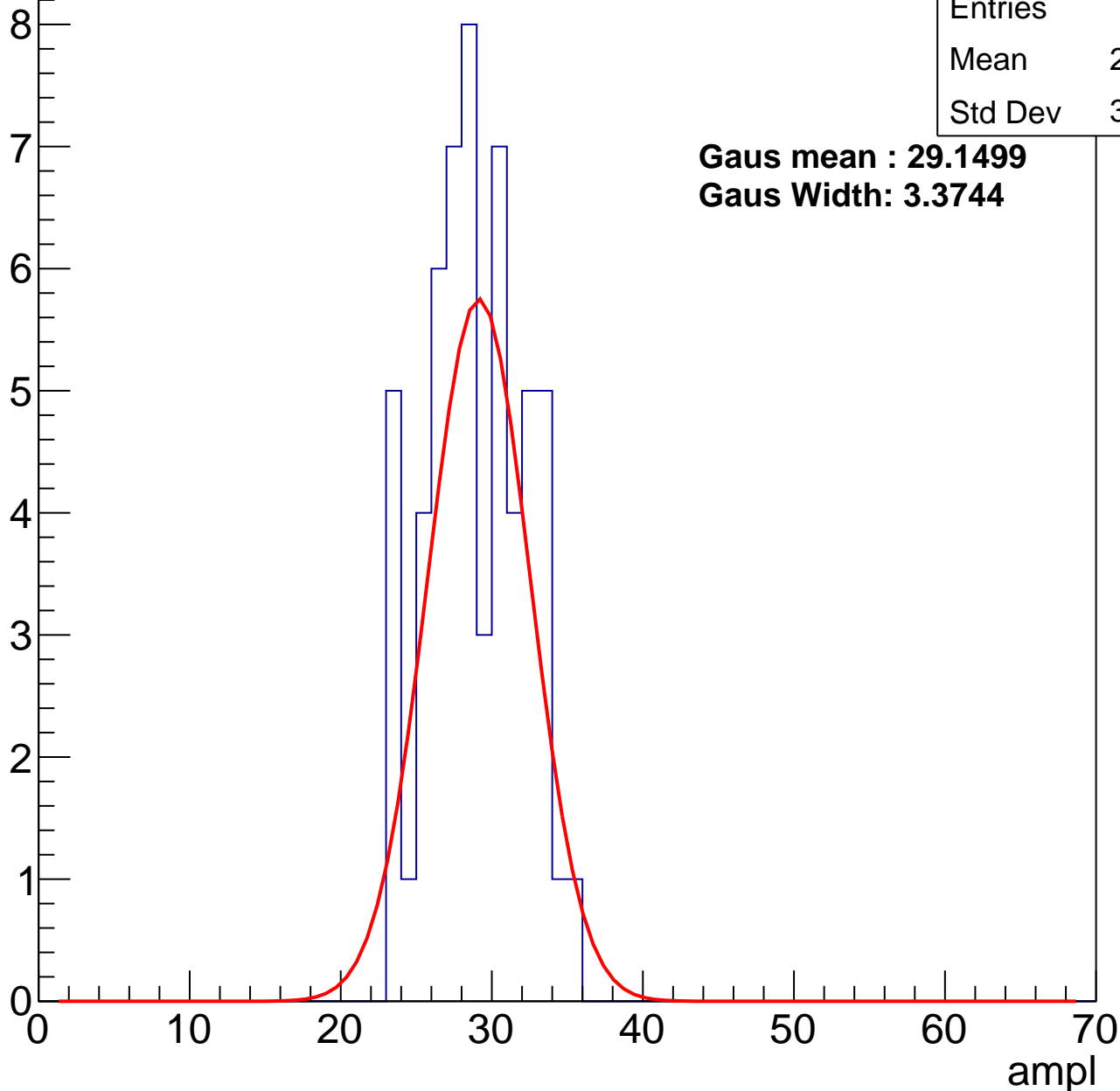
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	28.47
Std Dev	3.113

**Gaus mean : 29.1499**

**Gaus Width: 3.3744**



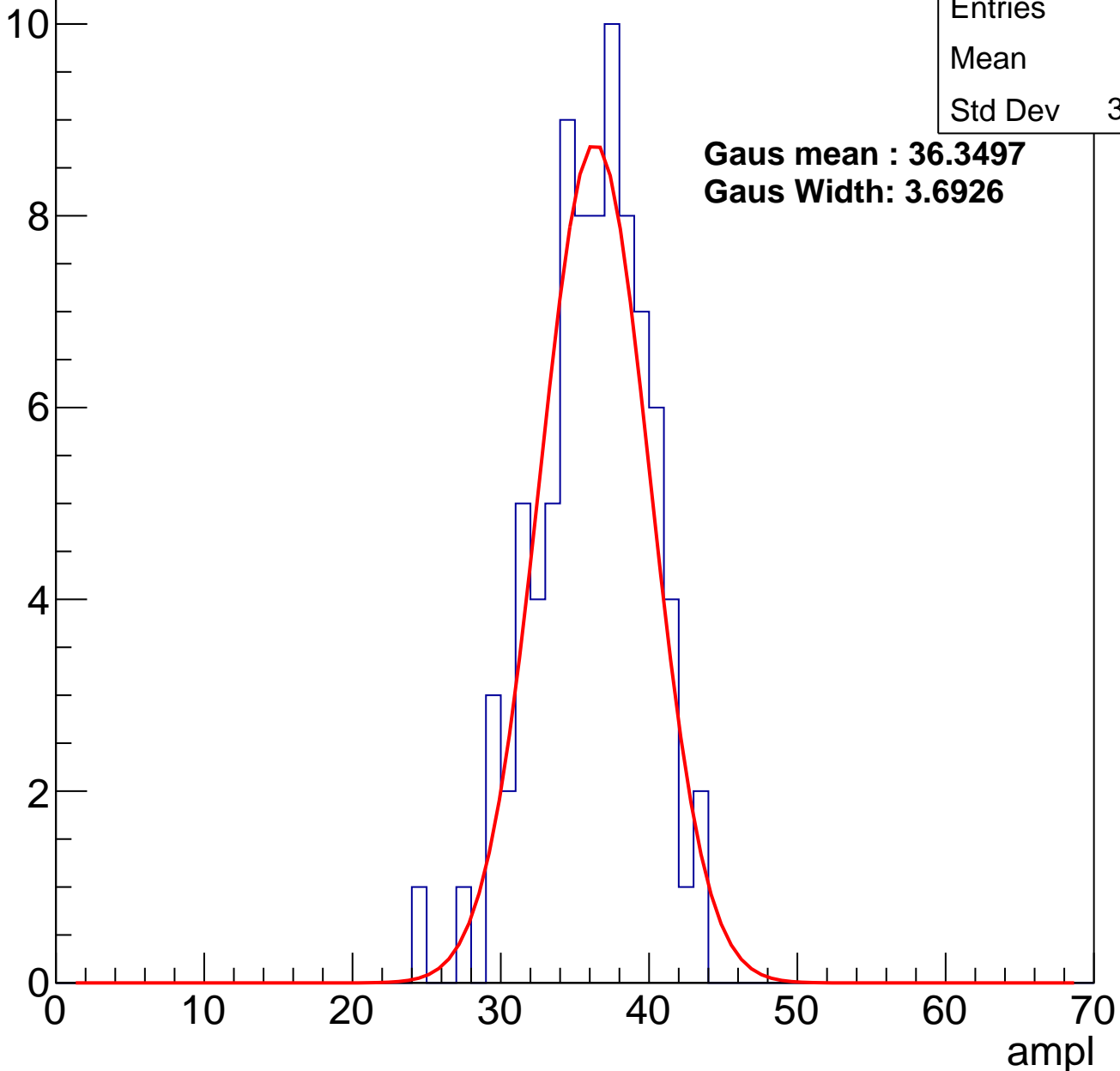
# B1L103S, U3-ch109, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	84
Mean	35.7
Std Dev	3.699

**Gaus mean : 36.3497**  
**Gaus Width: 3.6926**

Entry



# B1L103S, U3-ch109, adc2

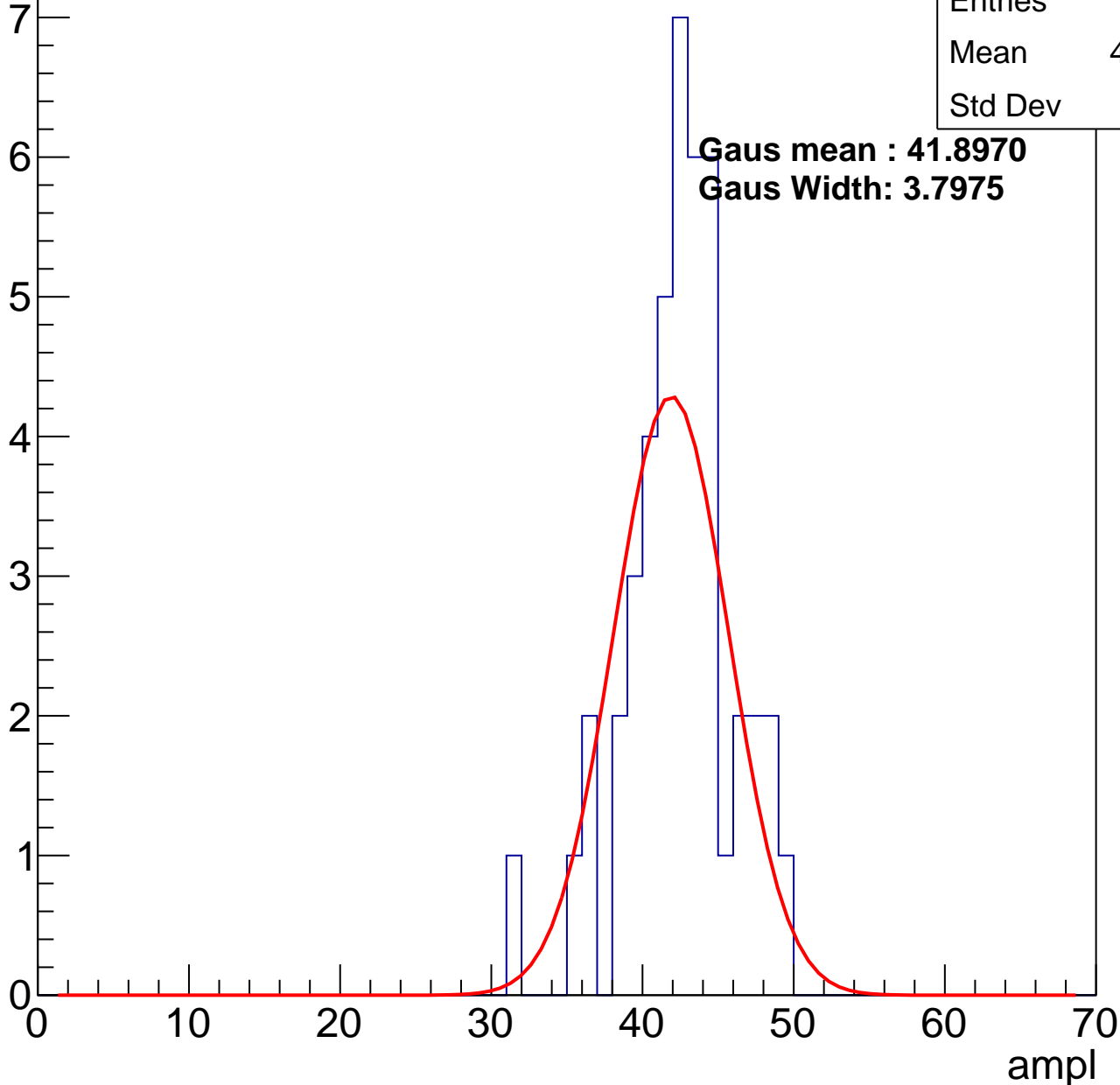
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	45
Mean	41.96
Std Dev	3.54

**Gaus mean : 41.8970**

**Gaus Width: 3.7975**

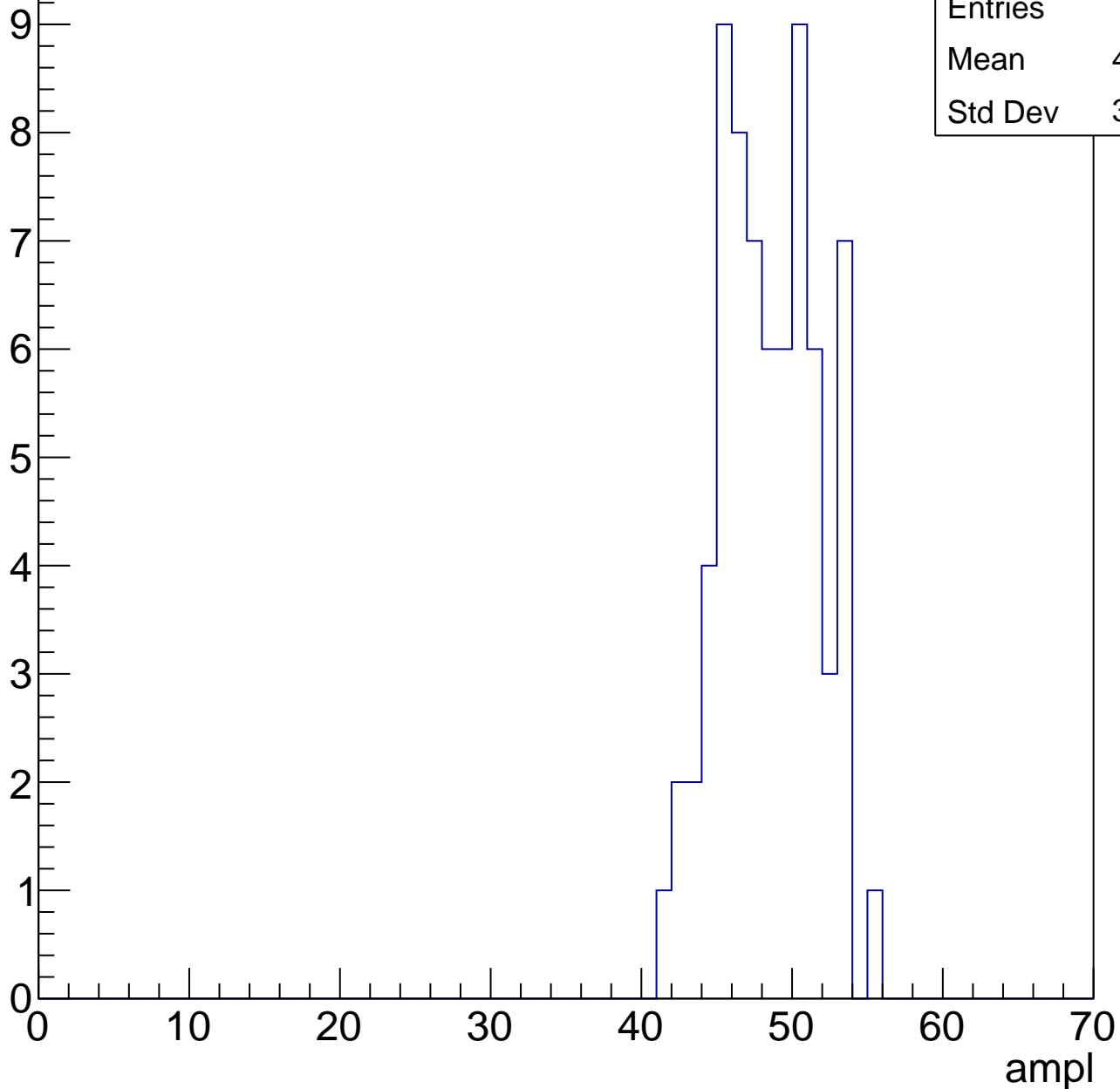


# B1L103S, U3-ch109, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	48.01
Std Dev	3.191

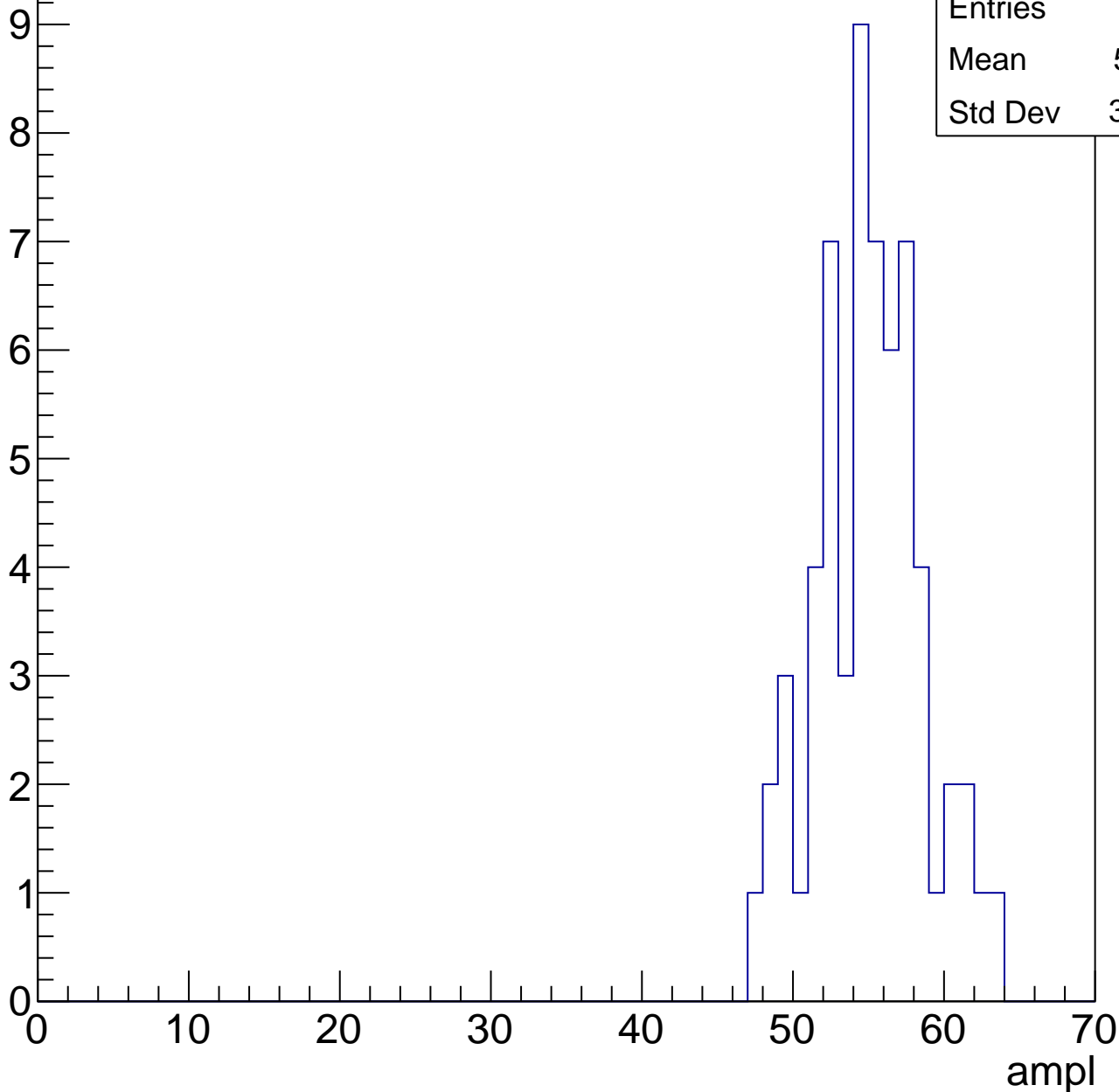


# B1L103S, U3-ch109, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	54.61
Std Dev	3.517

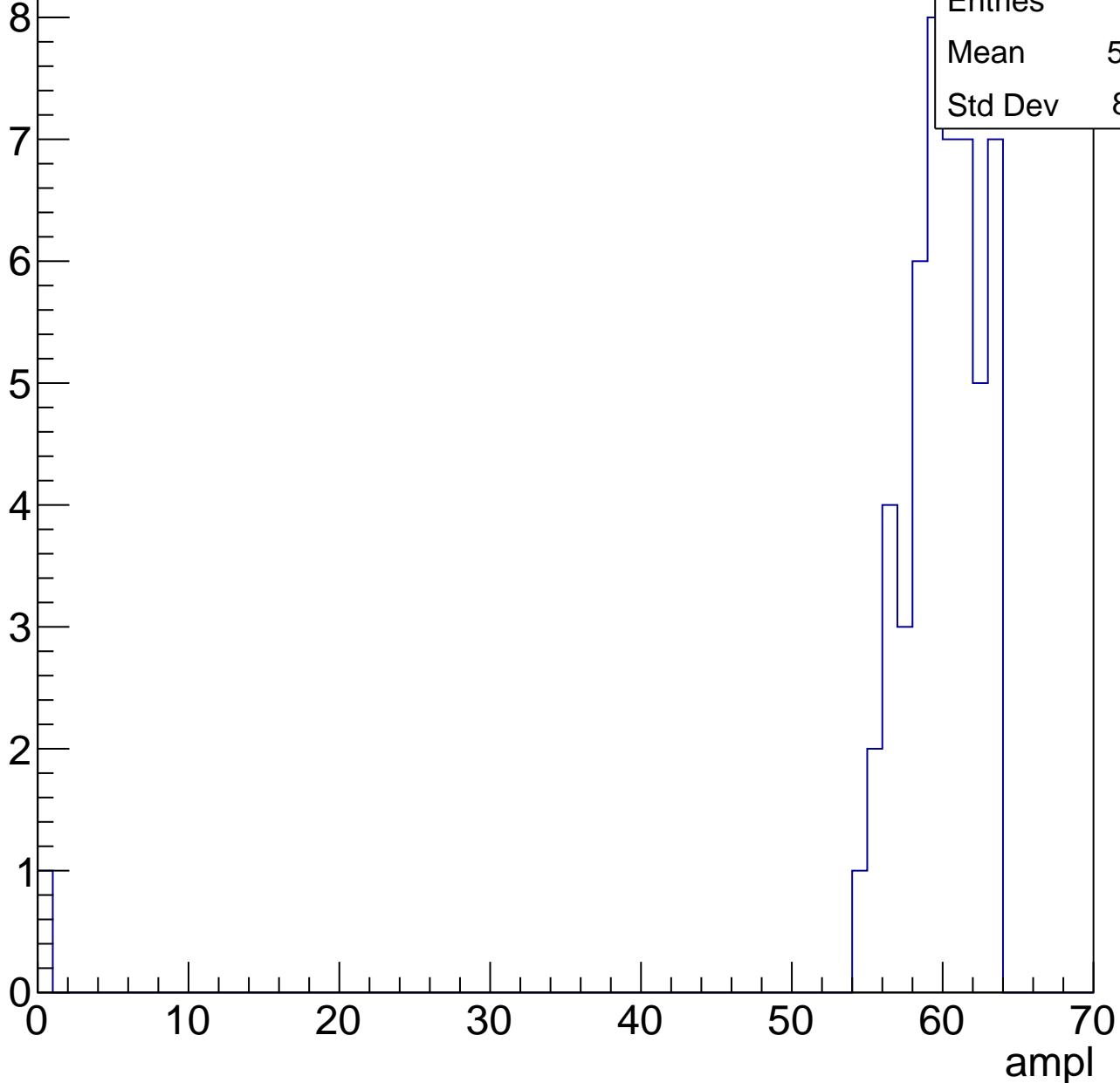


# B1L103S, U3-ch109, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

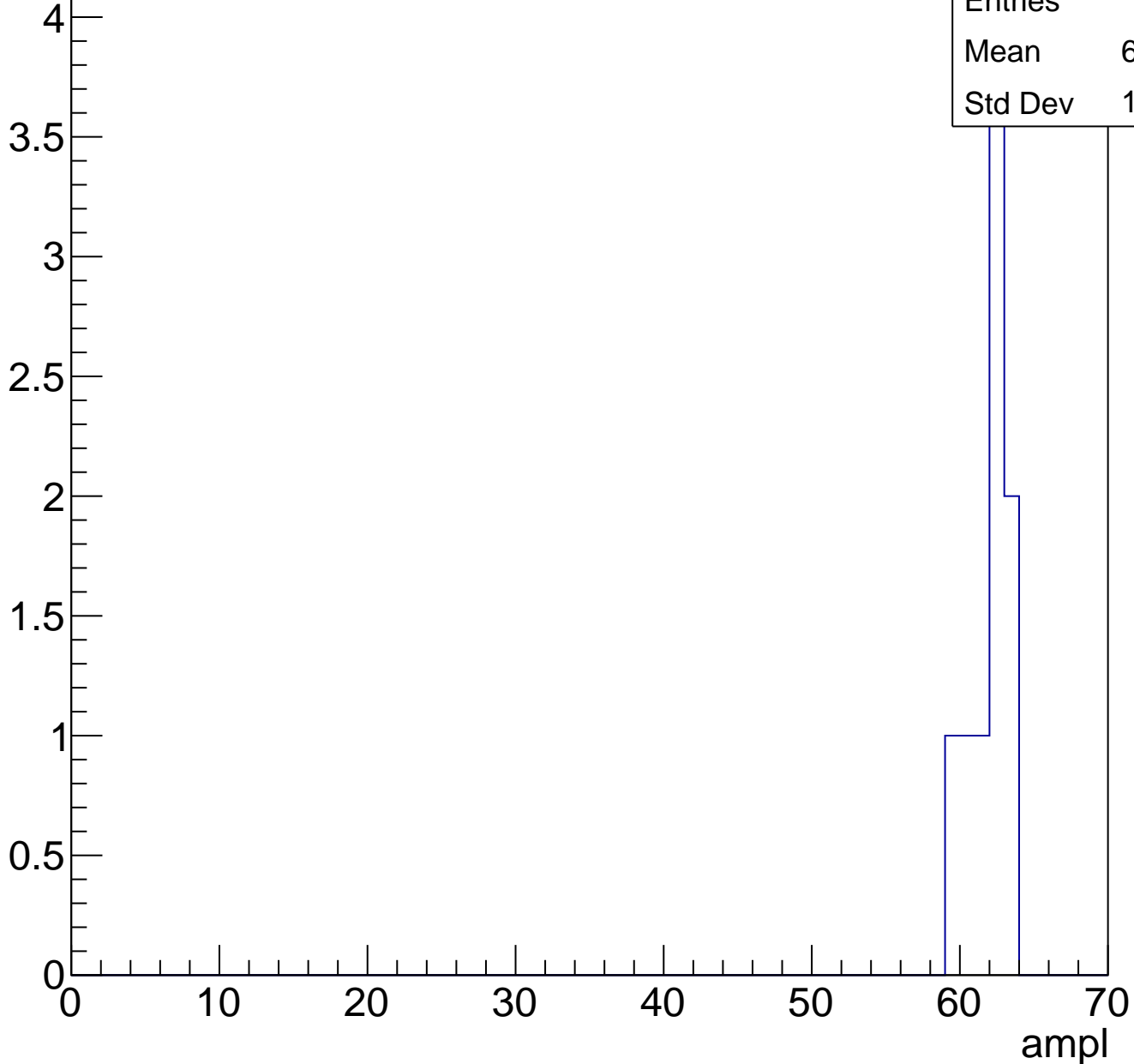
Entries	51
Mean	58.37
Std Dev	8.591



# B1L103S, U3-ch109, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U3-ch109, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U3-ch110, adc0

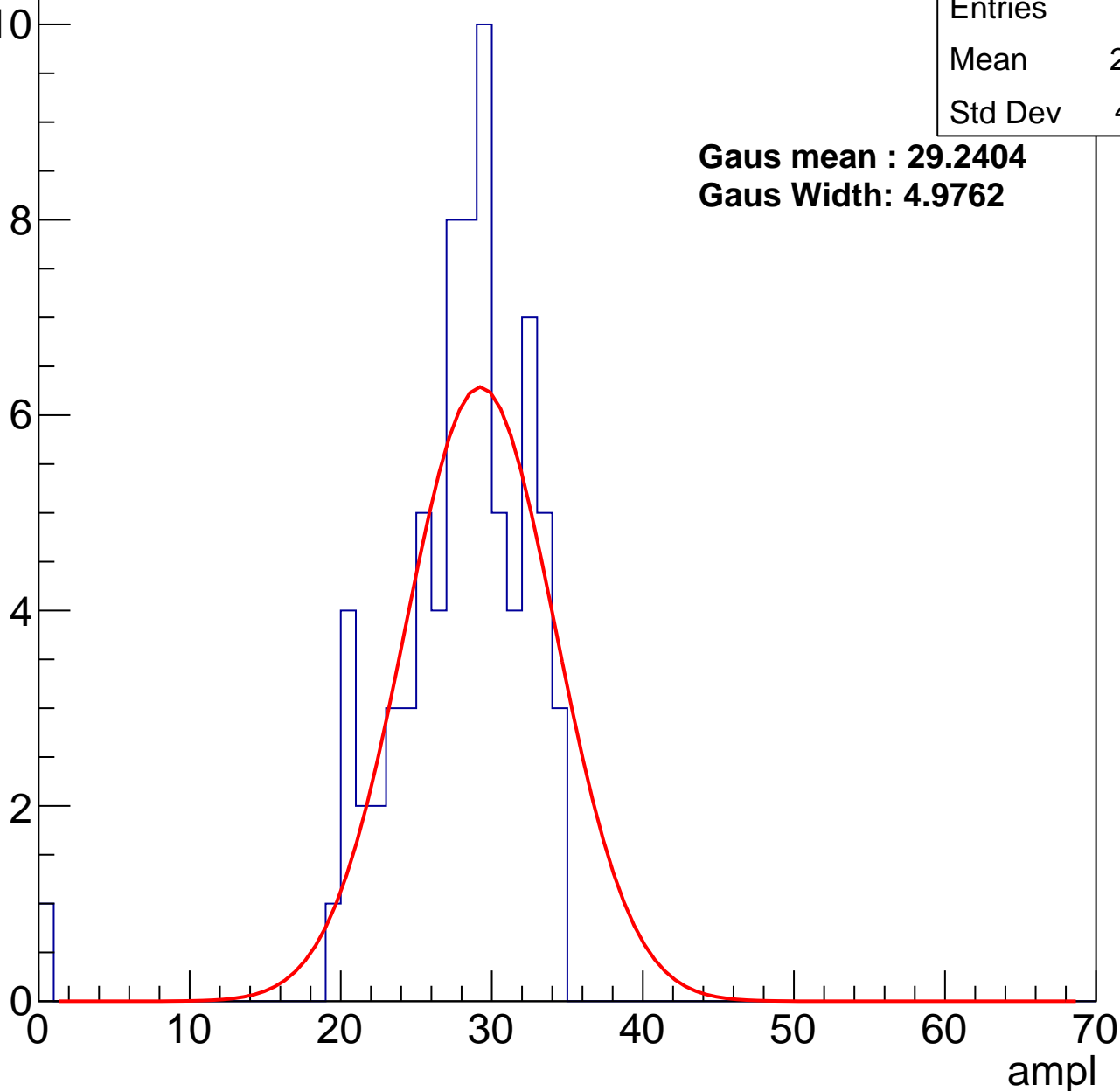
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	27.33
Std Dev	4.981

**Gaus mean : 29.2404**

**Gaus Width: 4.9762**



# B1L103S, U3-ch110, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	66
Mean	34.97
Std Dev	3.845

**Gaus mean : 35.0504**

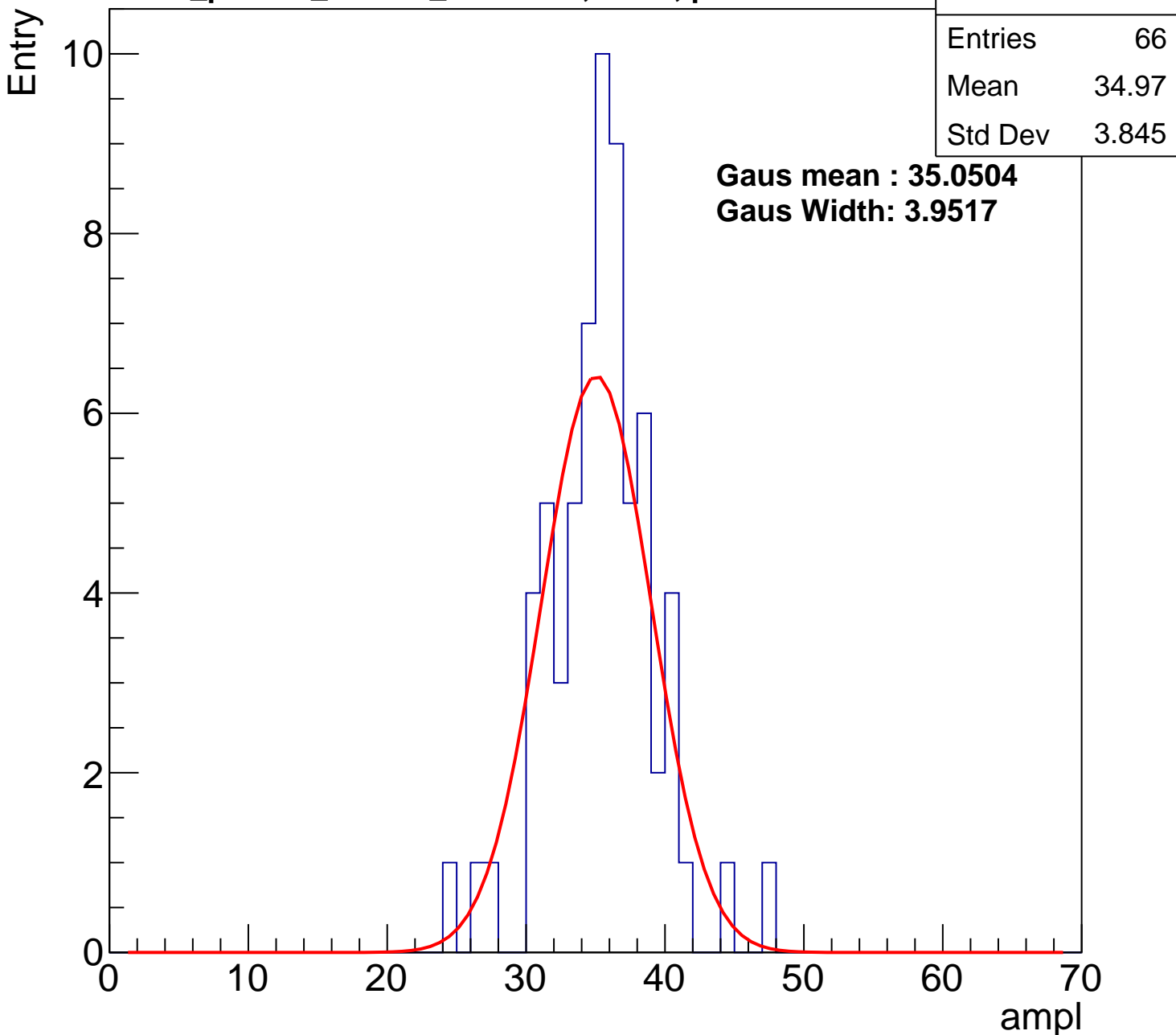
**Gaus Width: 3.9517**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U3-ch110, adc2

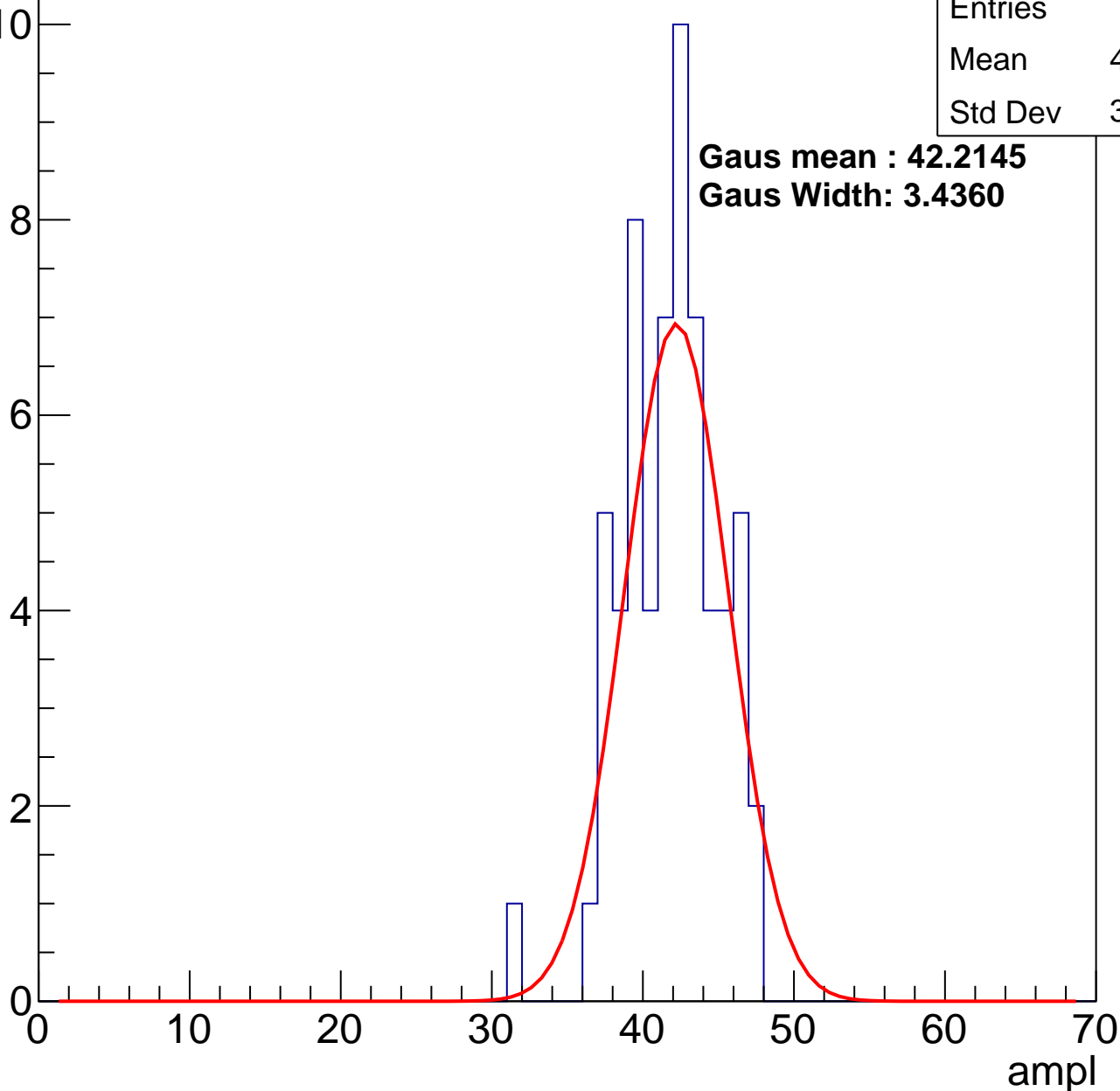
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	41.35
Std Dev	3.122

**Gaus mean : 42.2145**

**Gaus Width: 3.4360**

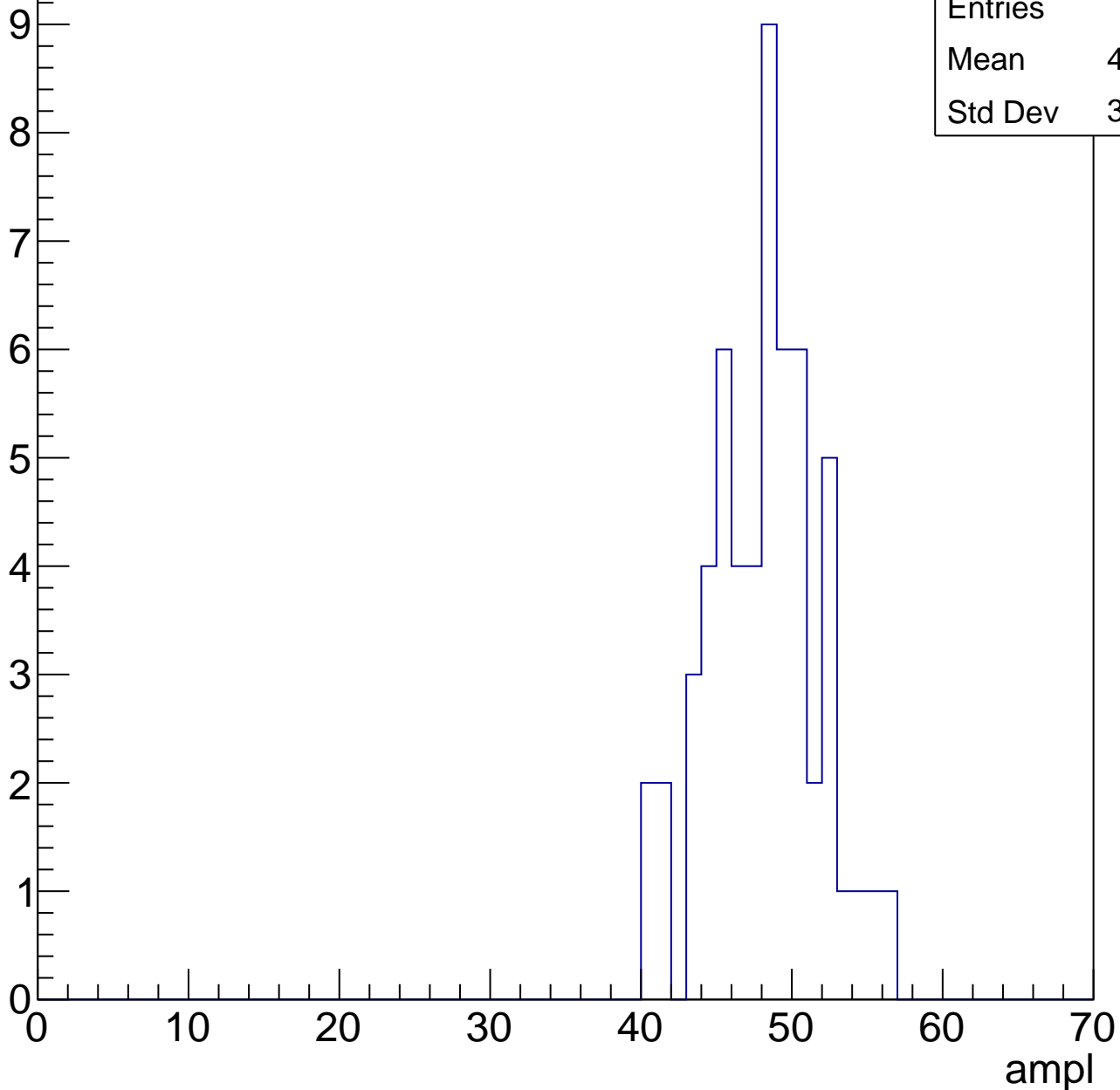


# B1L103S, U3-ch110, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	47.63
Std Dev	3.587

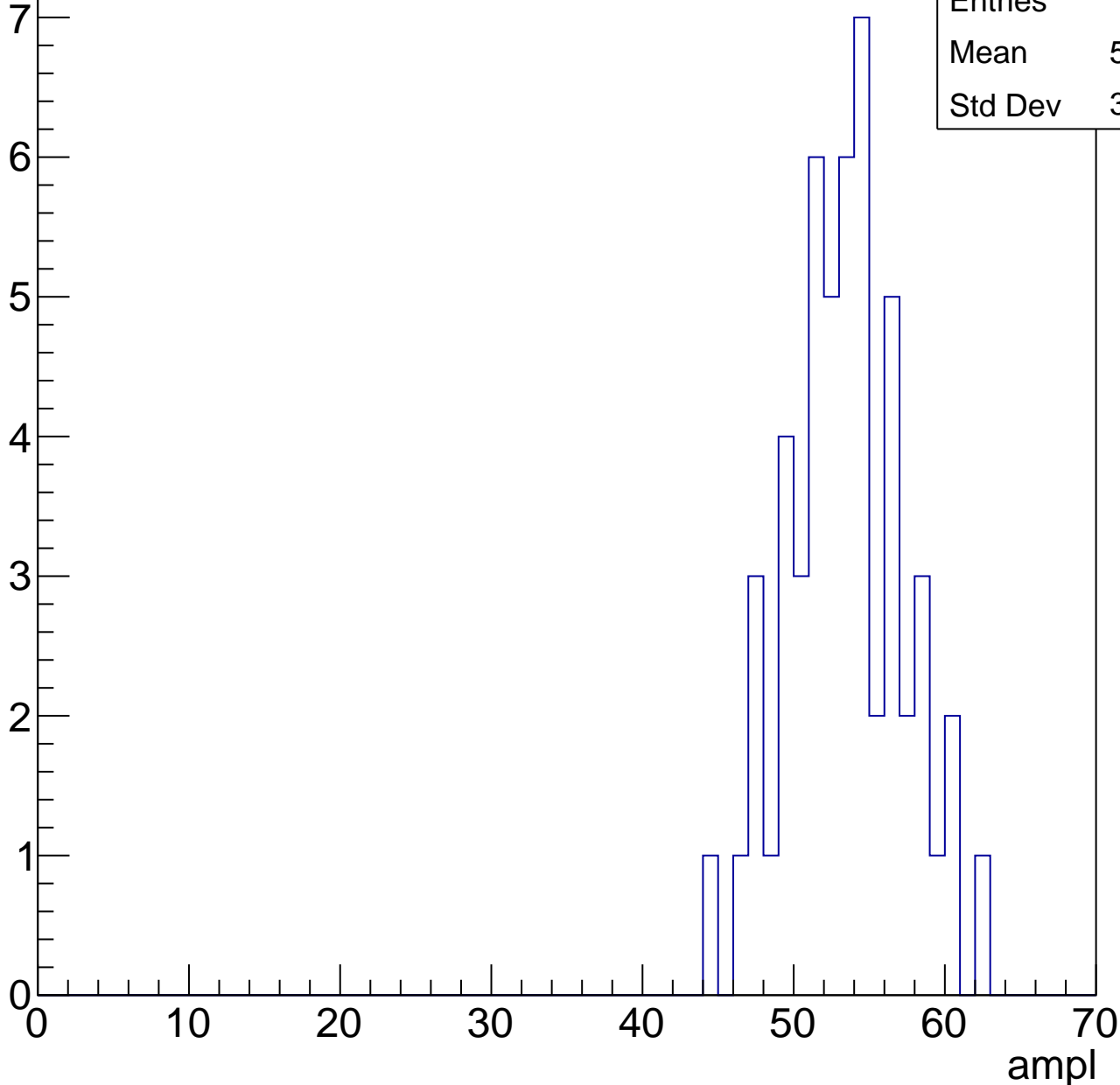


# B1L103S, U3-ch110, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	52.94
Std Dev	3.799

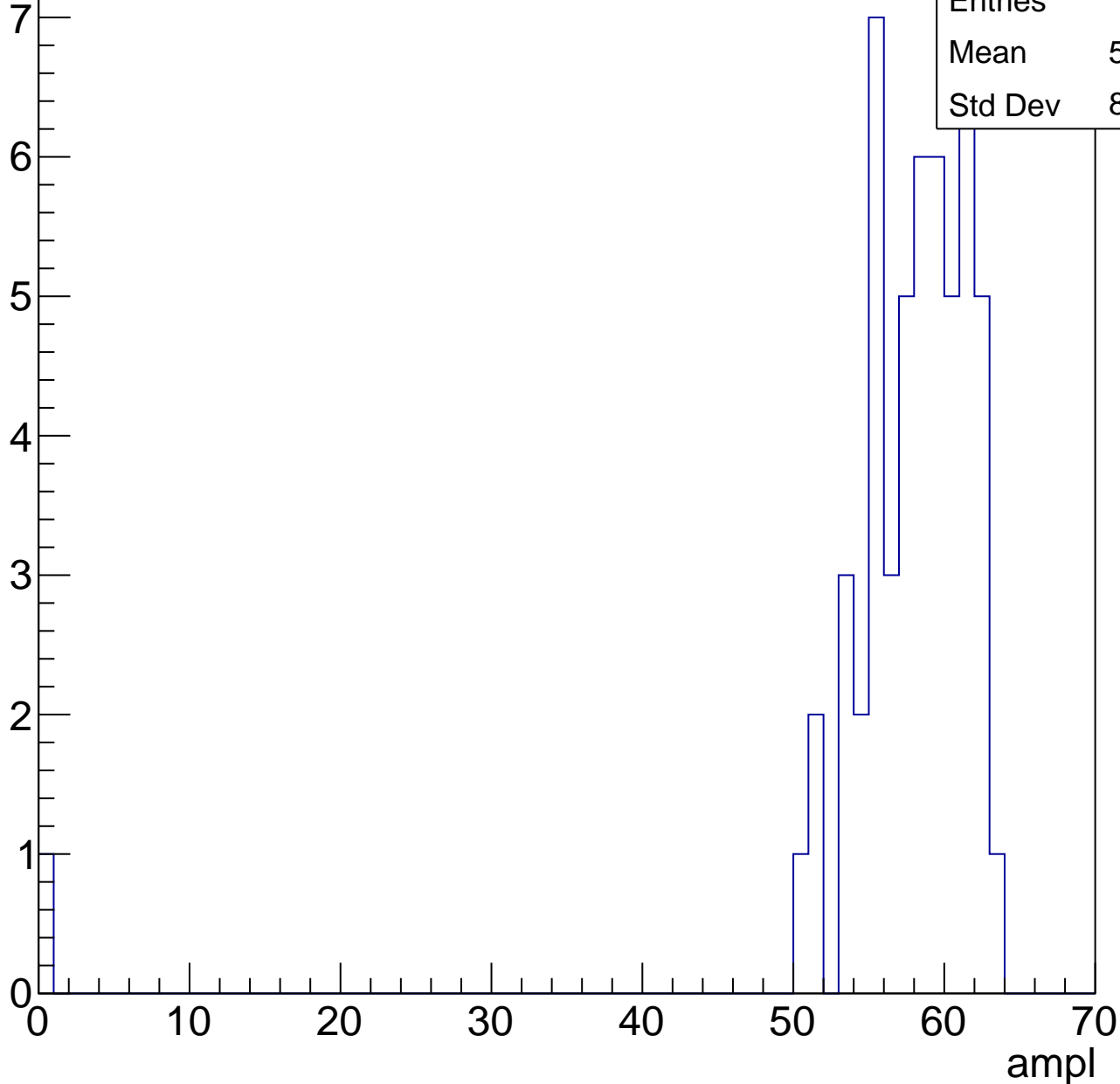


# B1L103S, U3-ch110, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	56.65
Std Dev	8.398

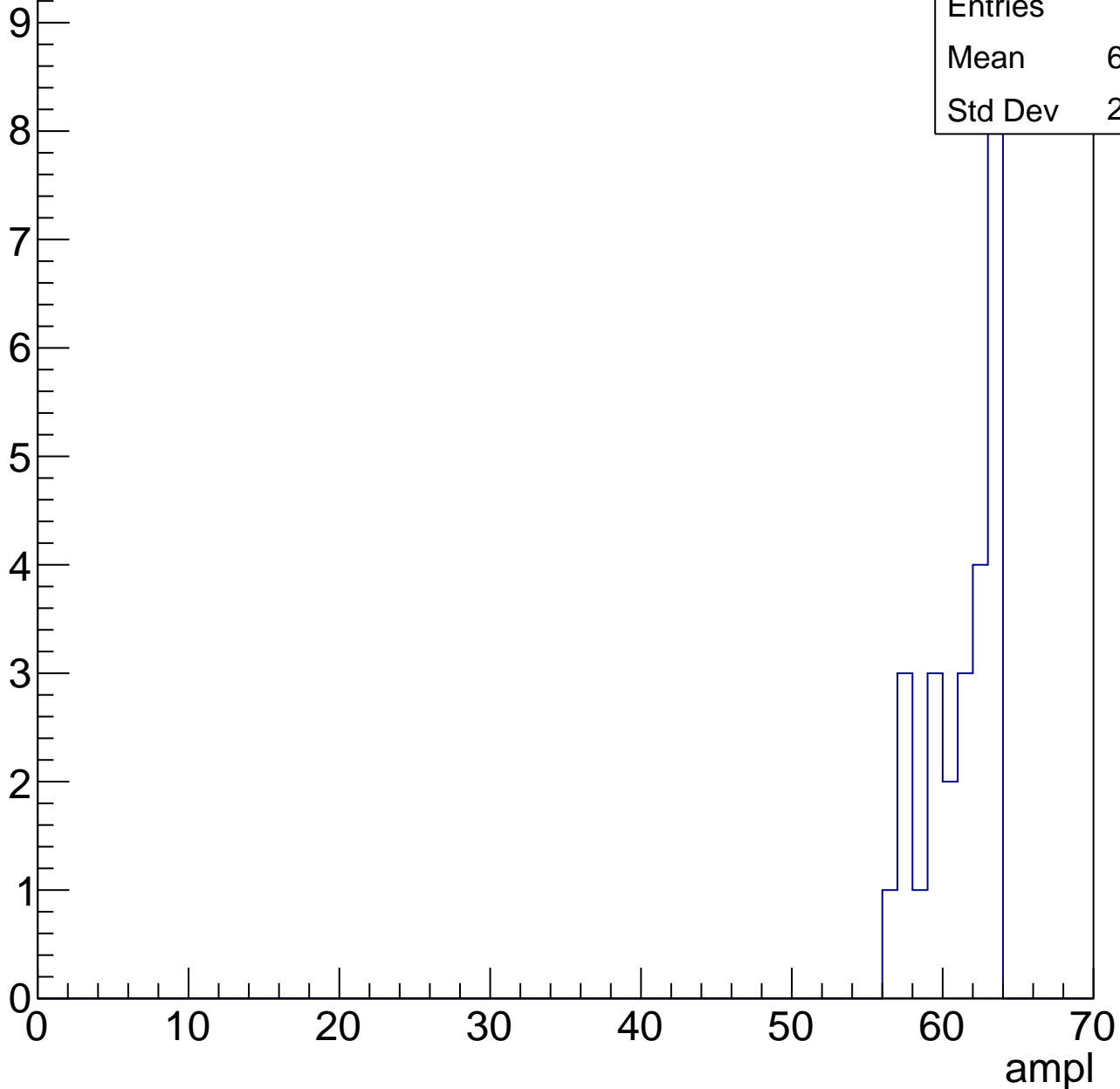


# B1L103S, U3-ch110, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	26
Mean	60.77
Std Dev	2.275

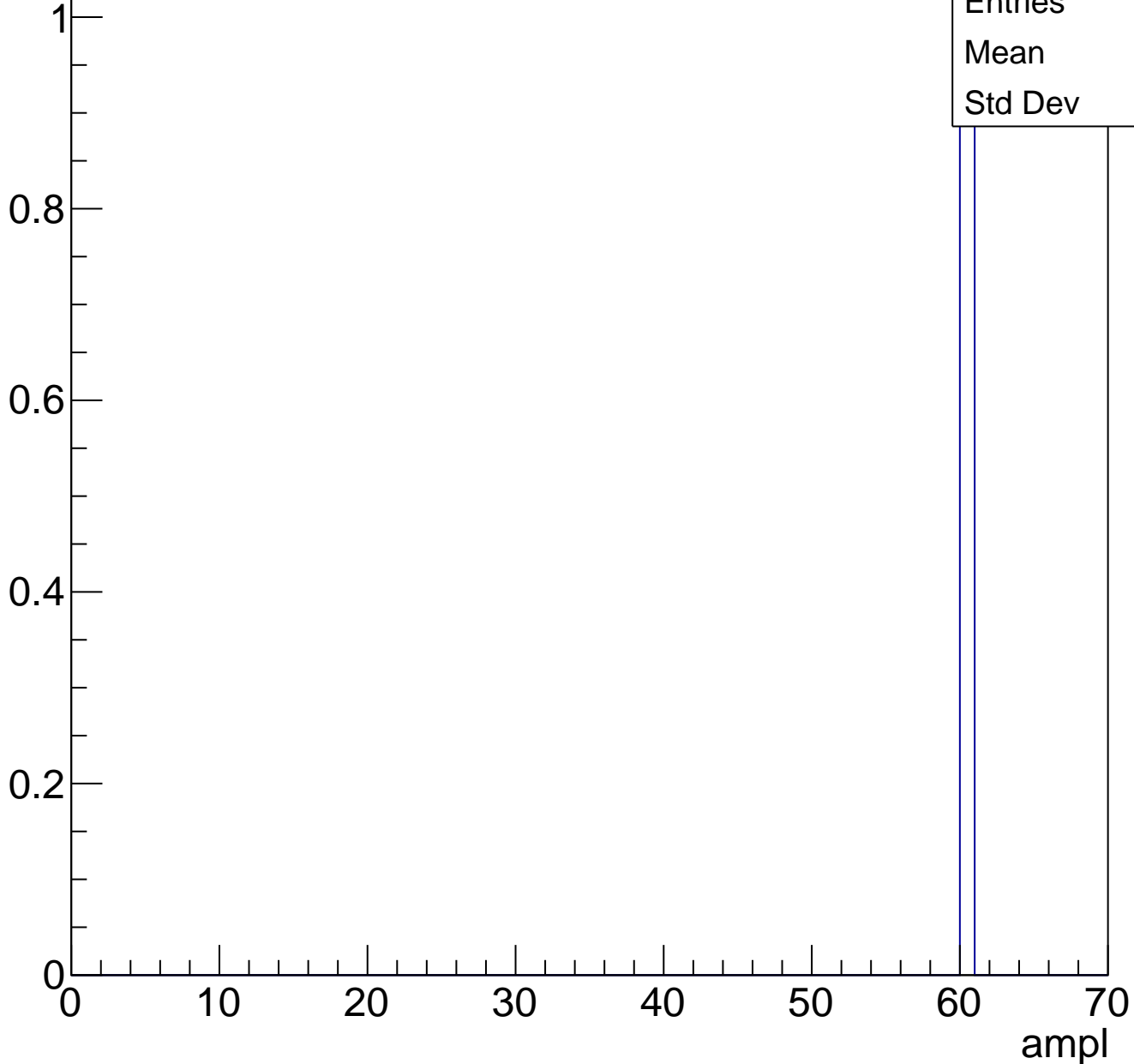




# B1L103S, U3-ch110, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch111, adc0

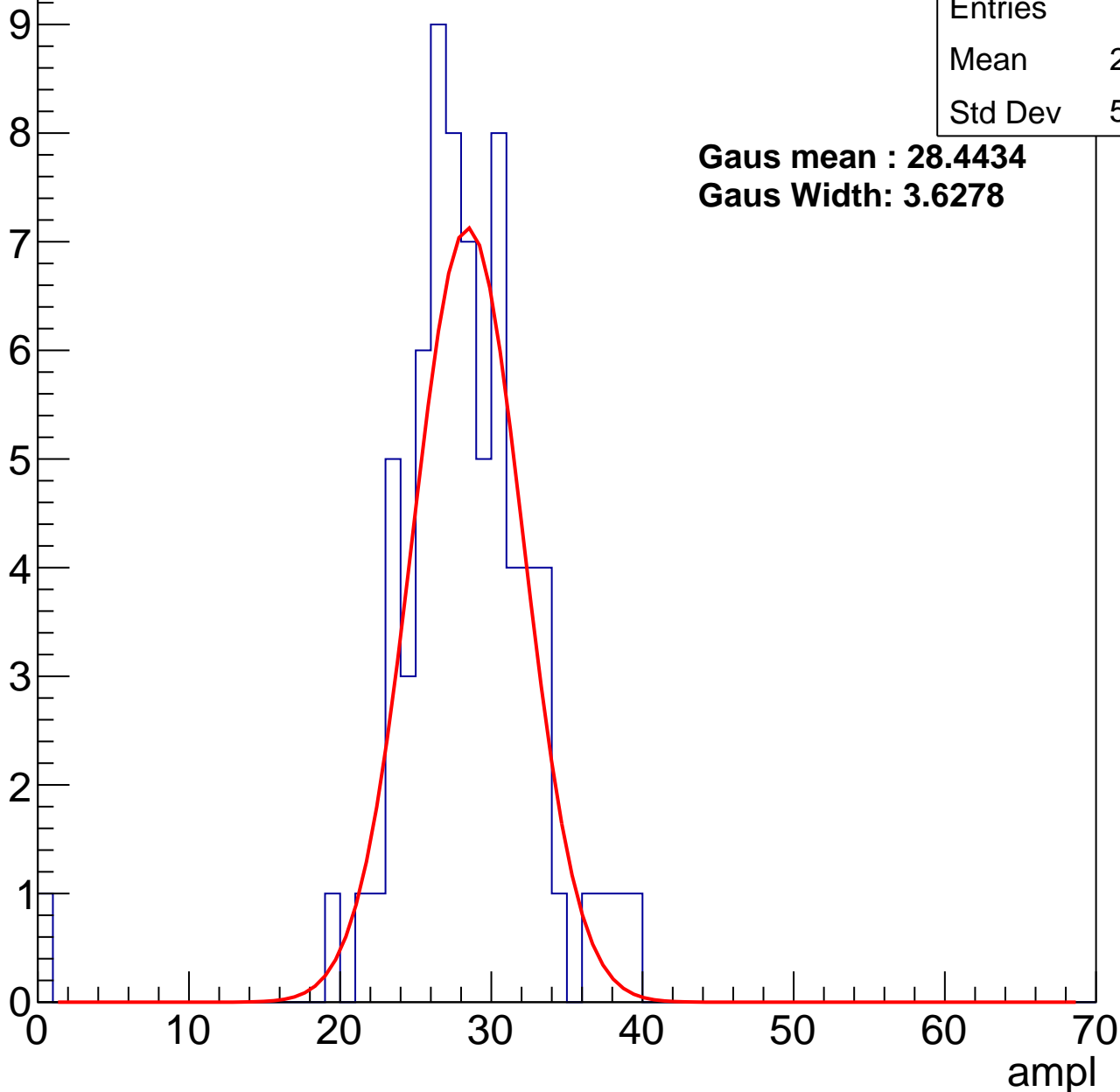
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	27.75
Std Dev	5.076

**Gaus mean : 28.4434**

**Gaus Width: 3.6278**



# B1L103S, U3-ch111, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	73
Mean	35.45
Std Dev	3.634

**Gaus mean : 35.9979**

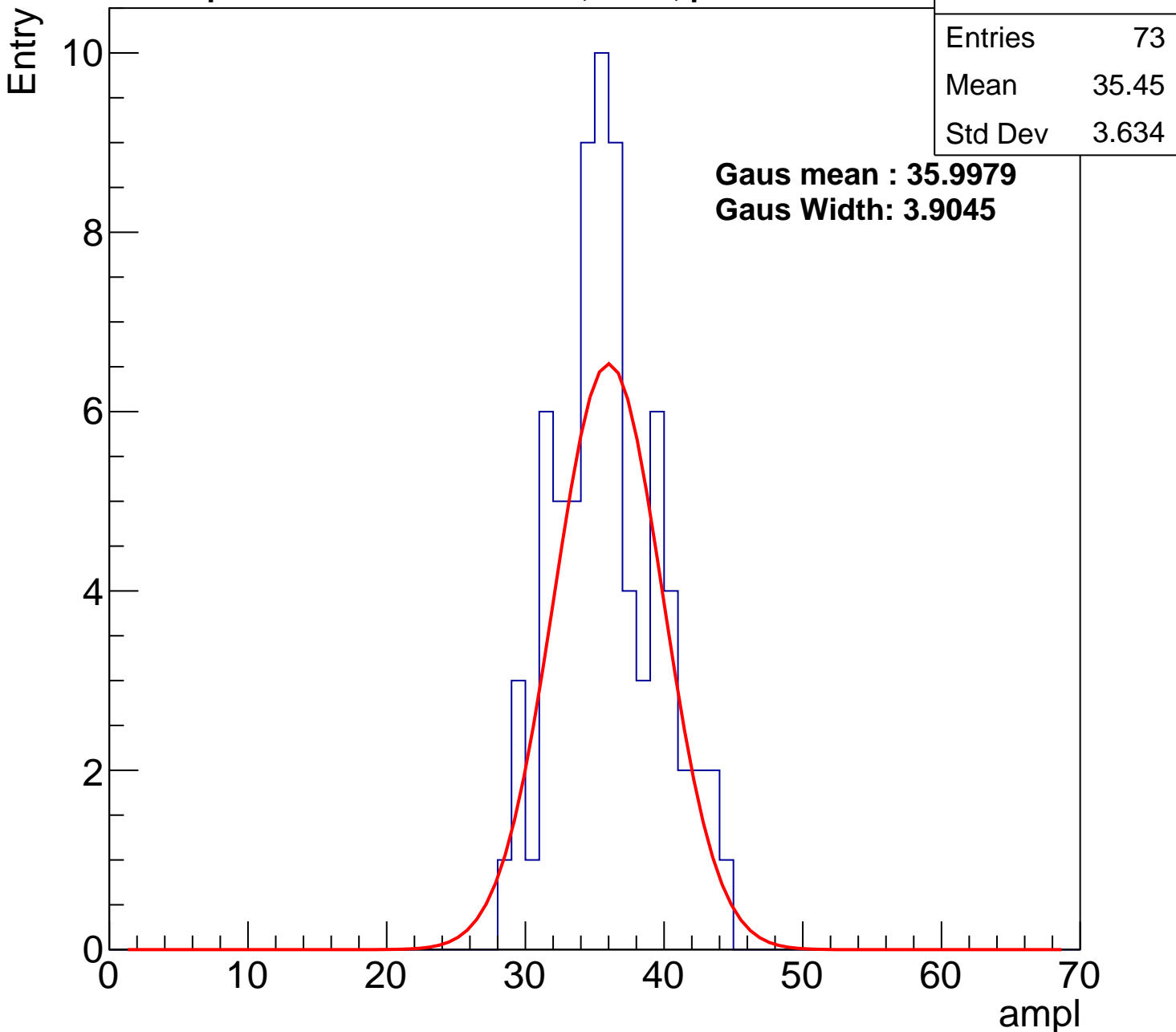
**Gaus Width: 3.9045**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U3-ch111, adc2

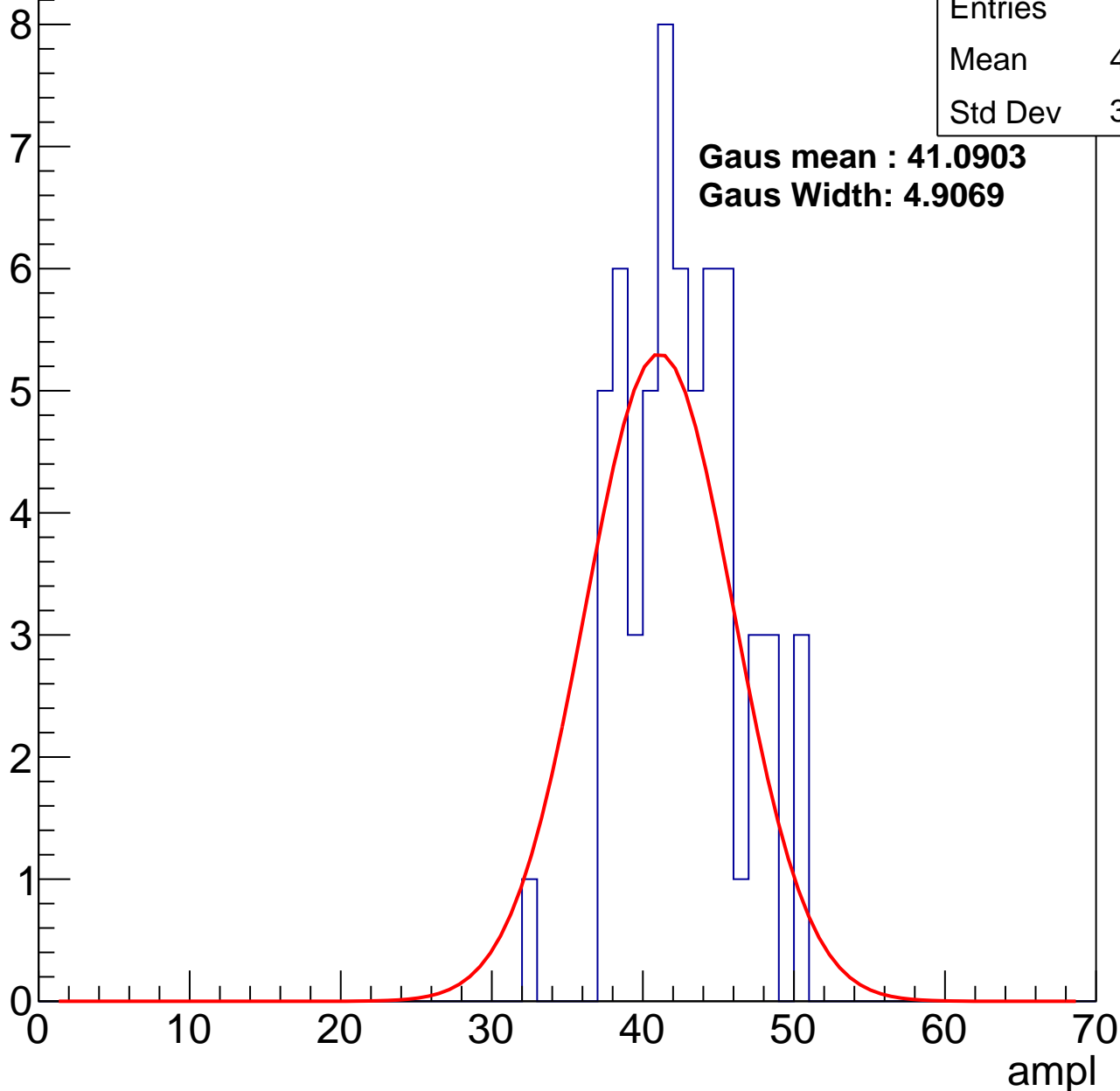
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	42.16
Std Dev	3.729

**Gaus mean : 41.0903**

**Gaus Width: 4.9069**

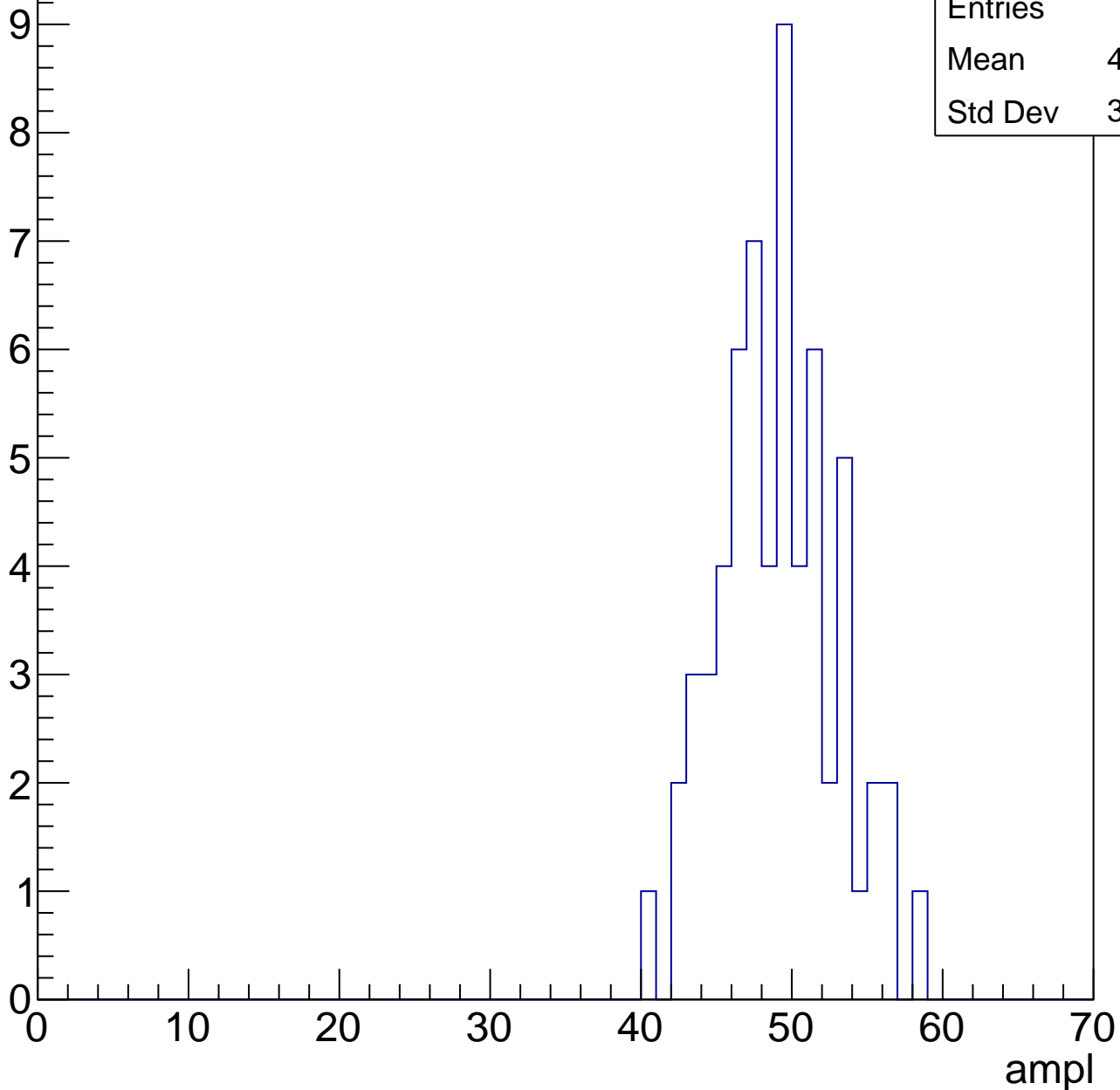


# B1L103S, U3-ch111, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	48.58
Std Dev	3.817

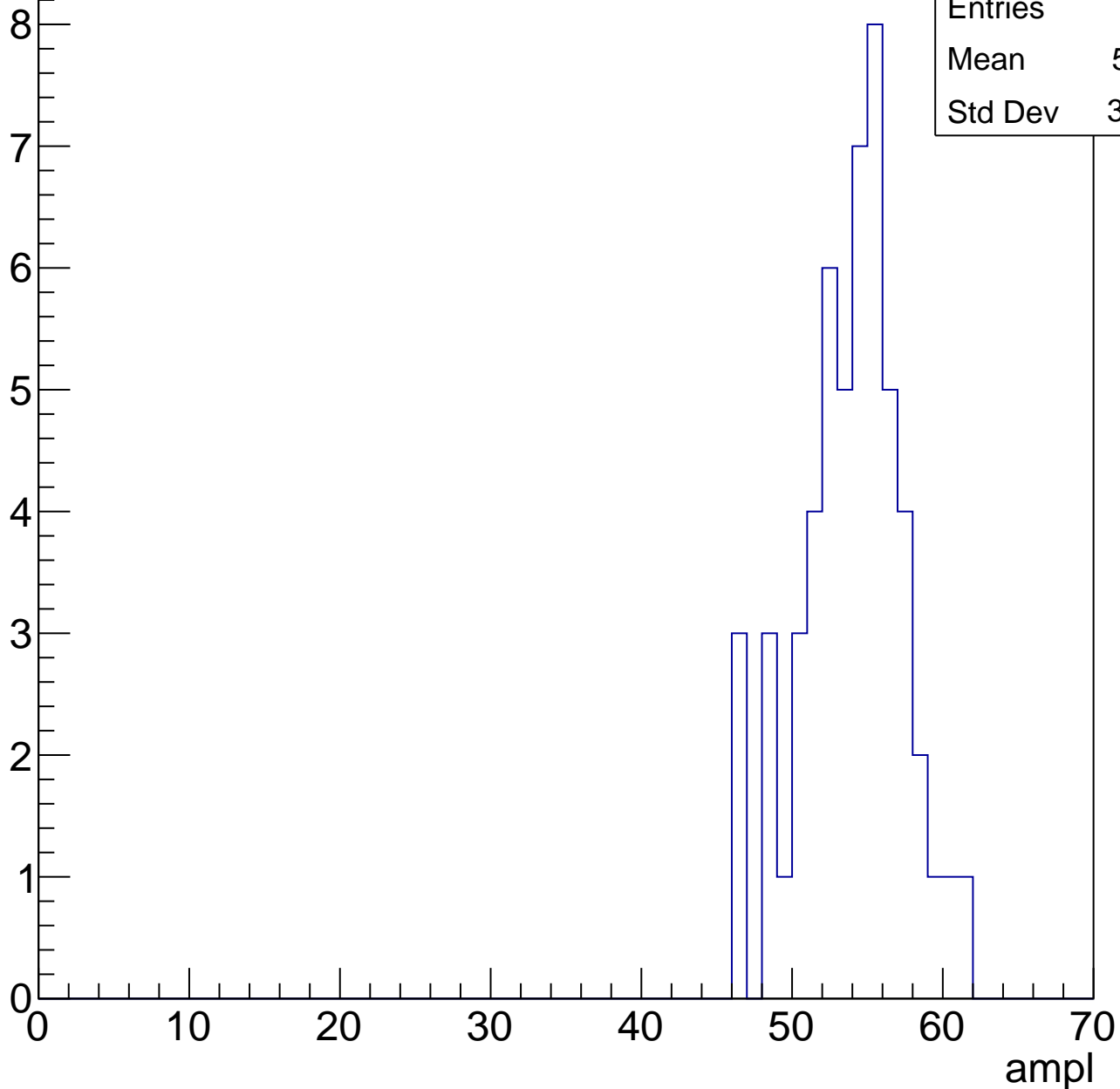


# B1L103S, U3-ch111, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	53.41
Std Dev	3.402

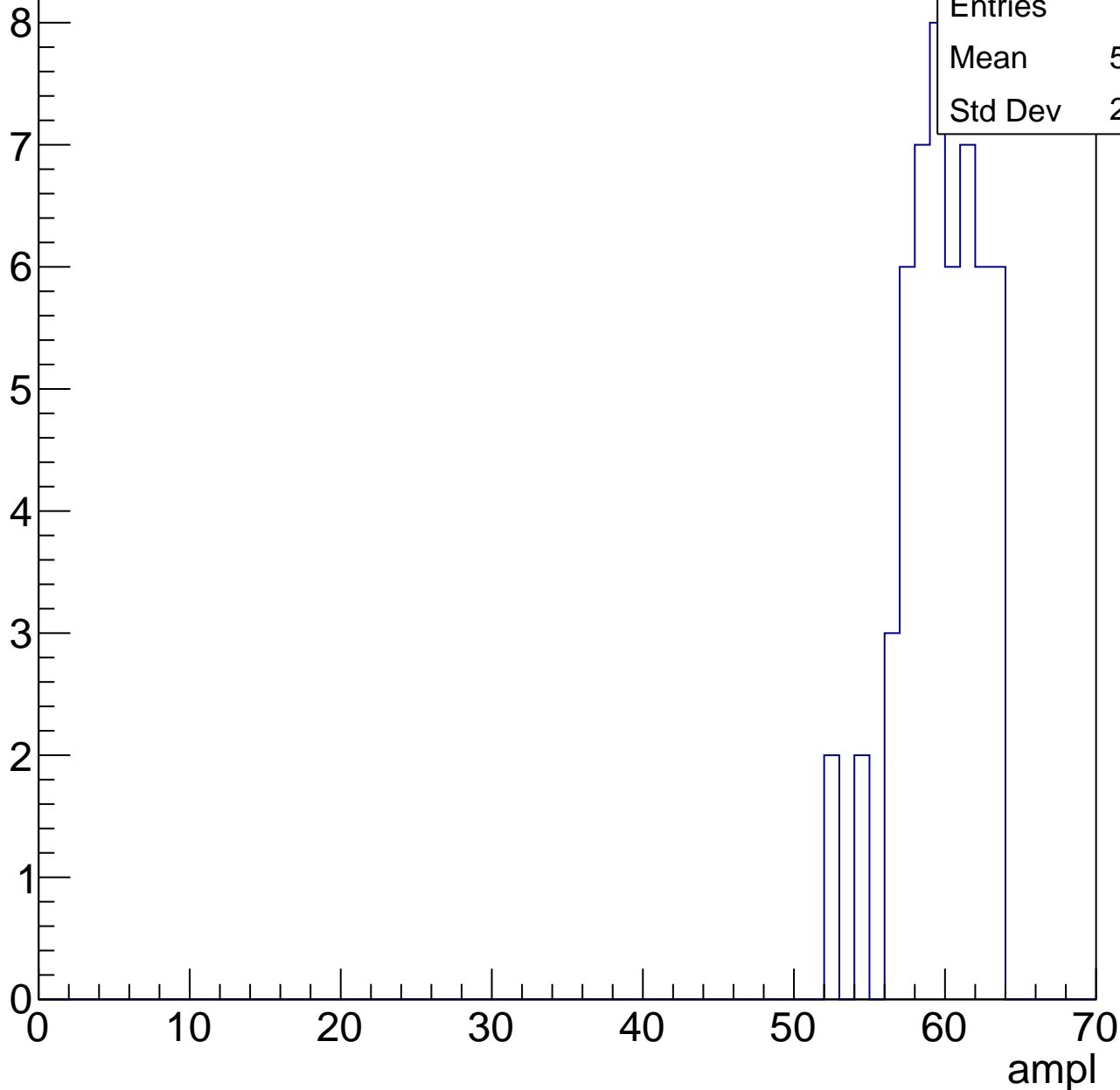


# B1L103S, U3-ch111, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

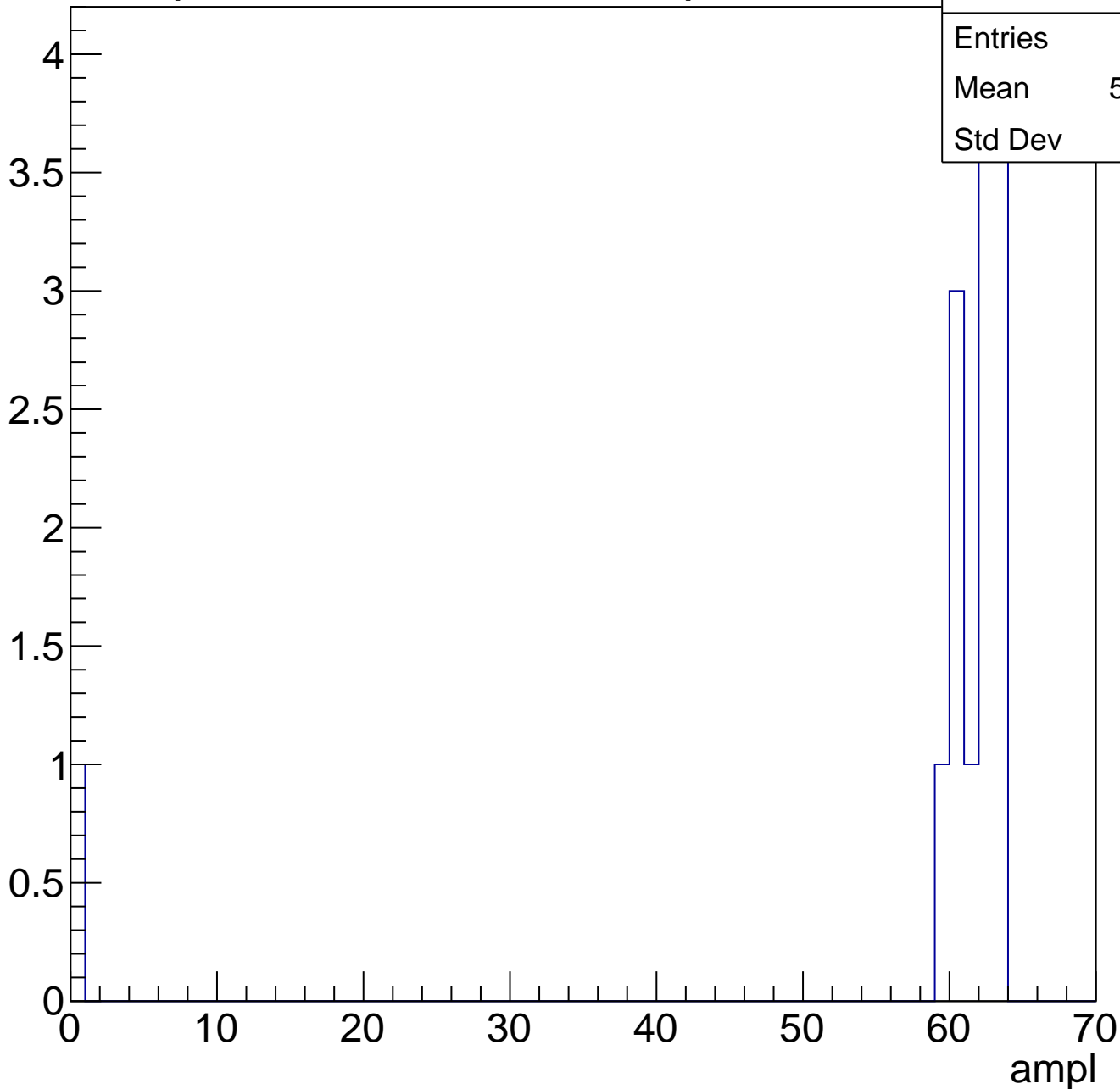
Entries	53
Mean	59.19
Std Dev	2.706



# B1L103S, U3-ch111, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

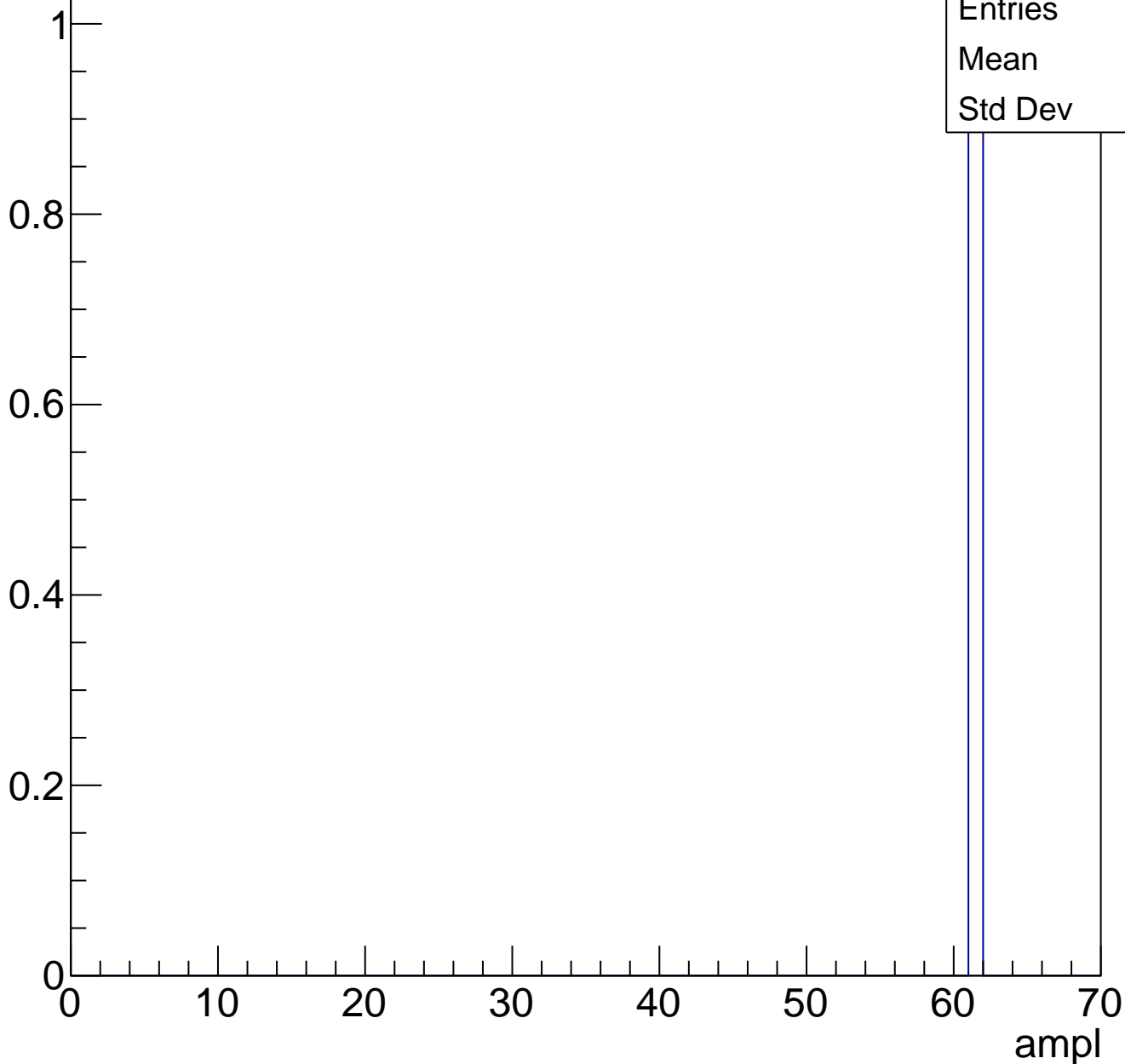




# B1L103S, U3-ch111, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch112, adc0

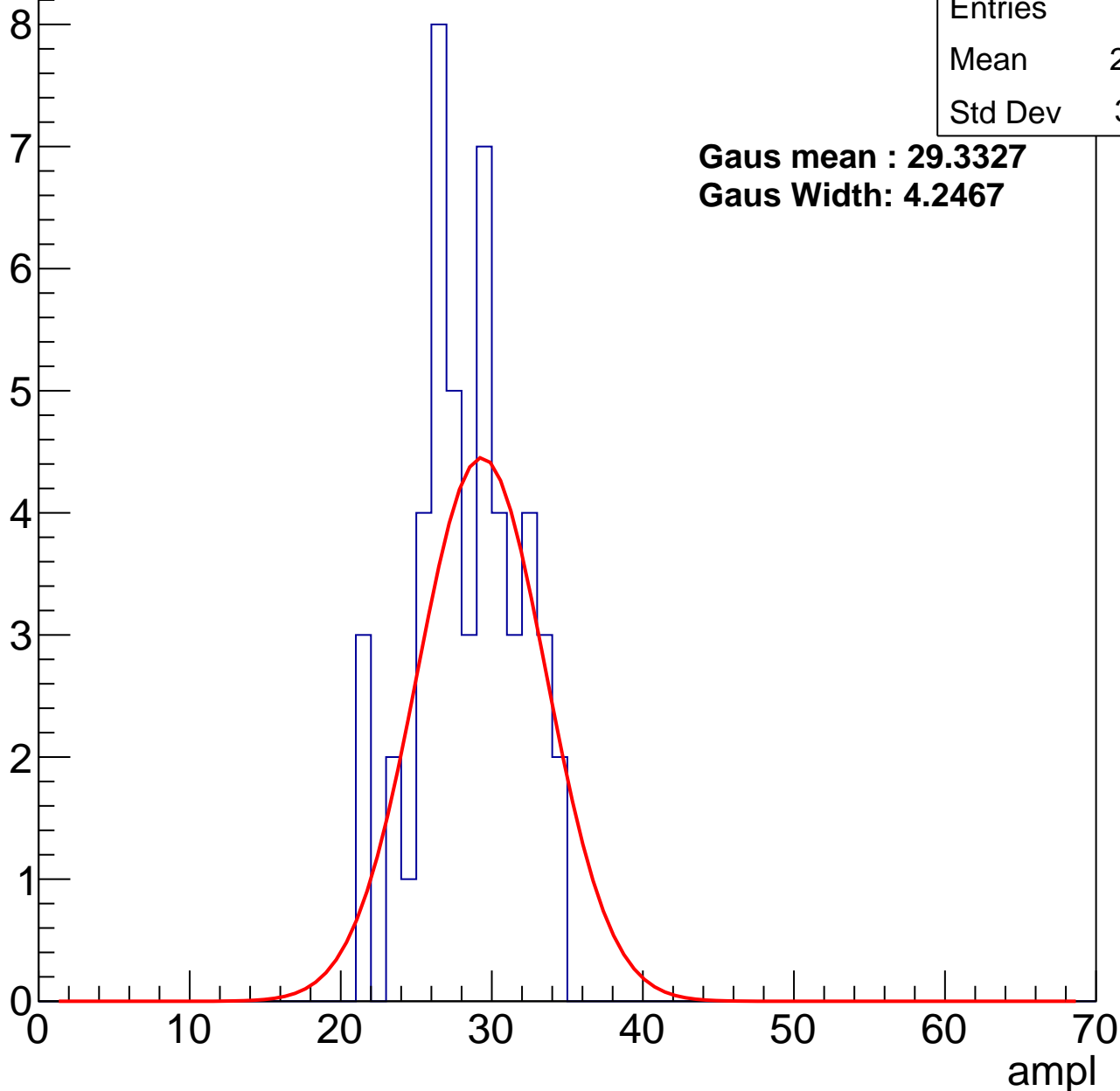
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	27.98
Std Dev	3.341

**Gaus mean : 29.3327**

**Gaus Width: 4.2467**



# B1L103S, U3-ch112, adc1

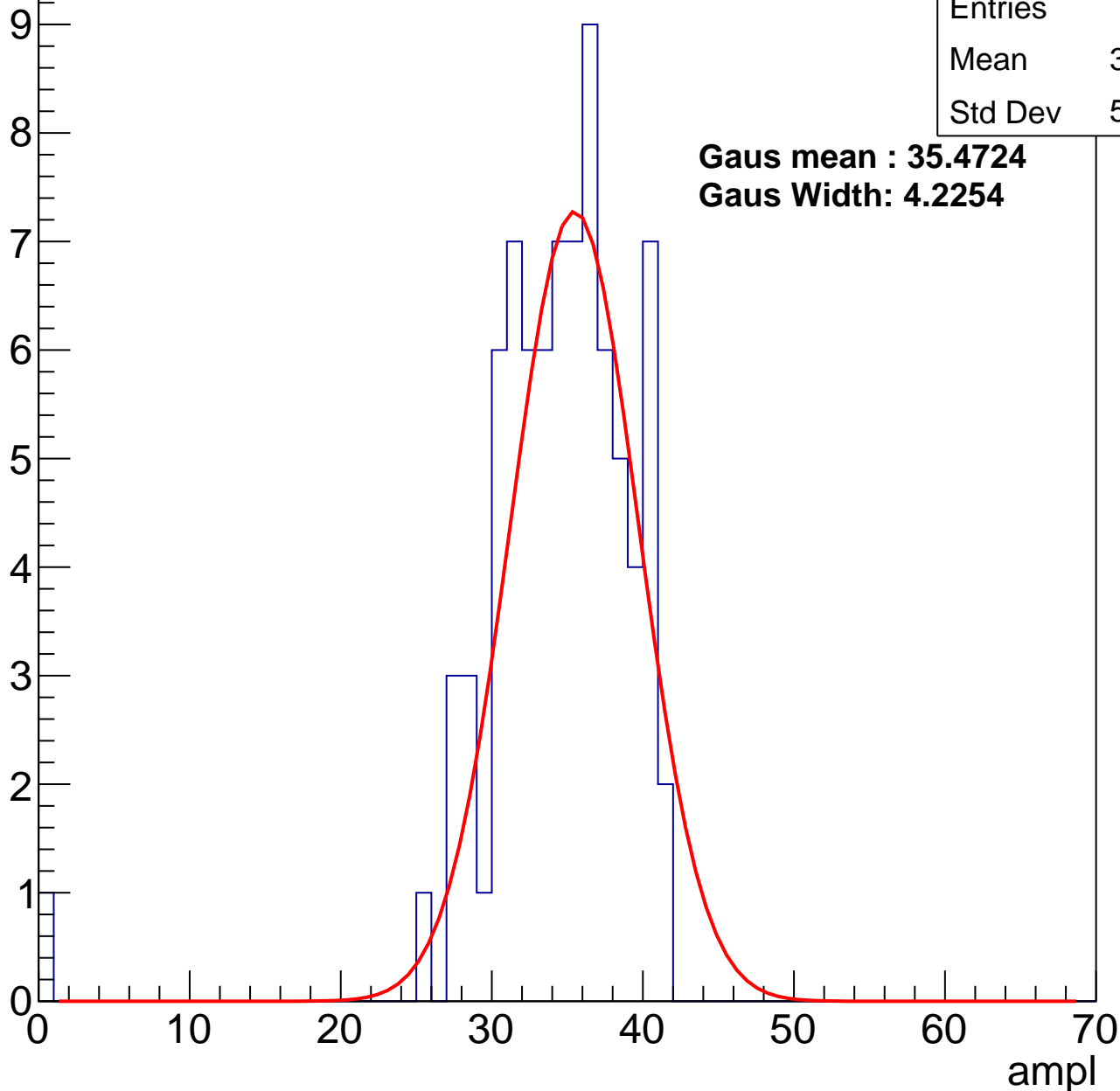
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	81
Mean	33.86
Std Dev	5.365

**Gaus mean : 35.4724**

**Gaus Width: 4.2254**



# B1L103S, U3-ch112, adc2

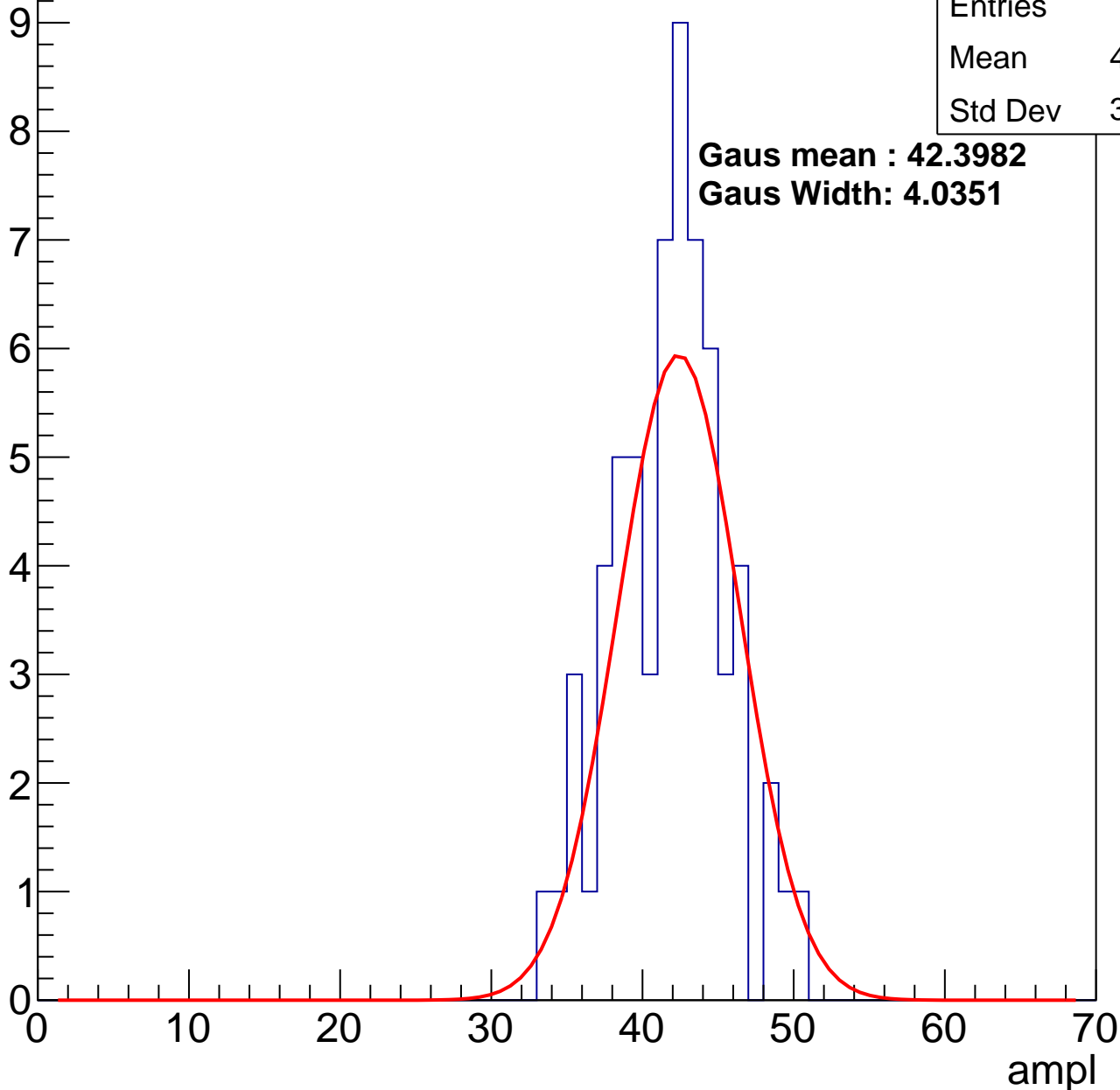
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	41.35
Std Dev	3.678

**Gaus mean : 42.3982**

**Gaus Width: 4.0351**

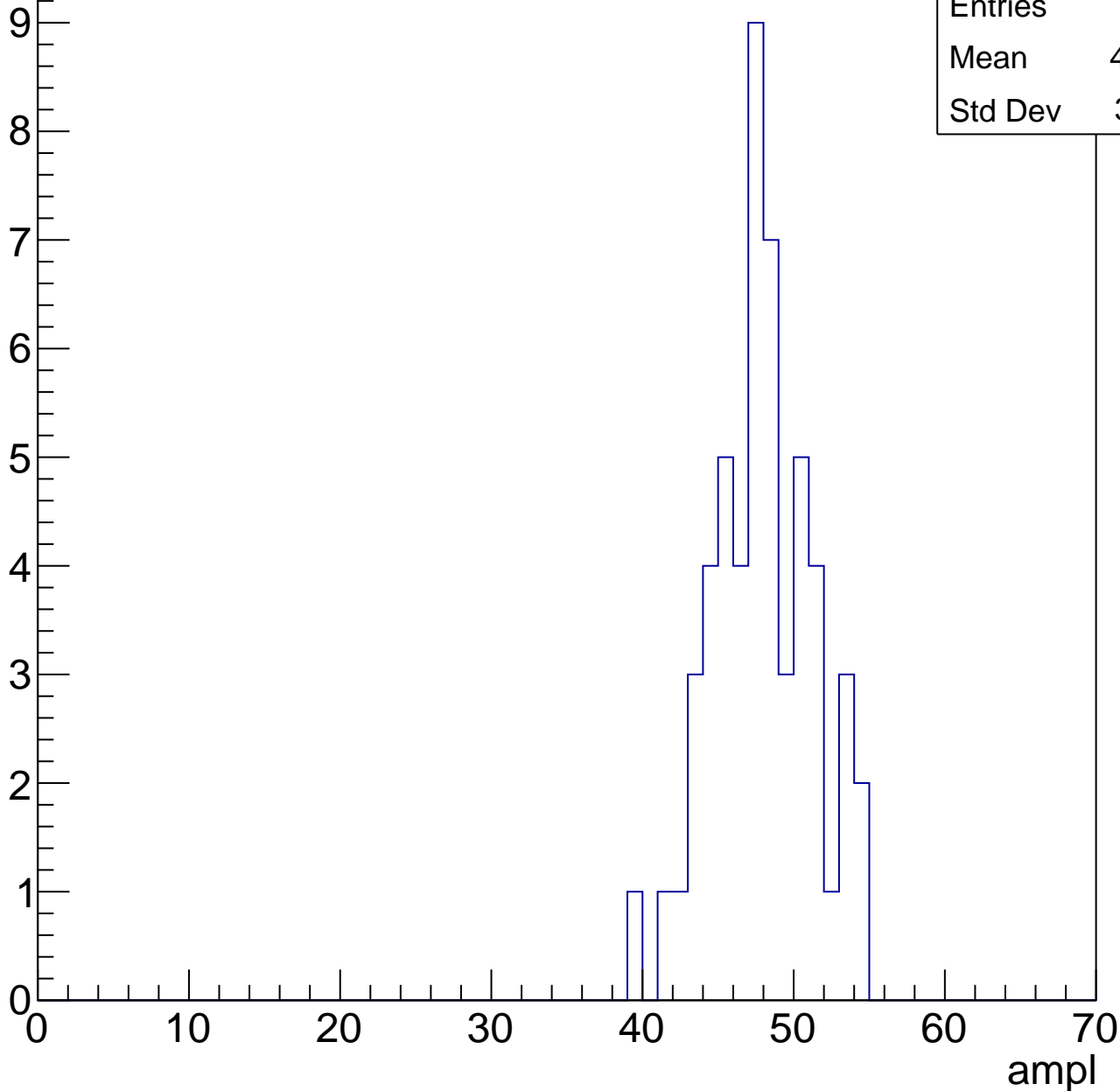


# B1L103S, U3-ch112, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

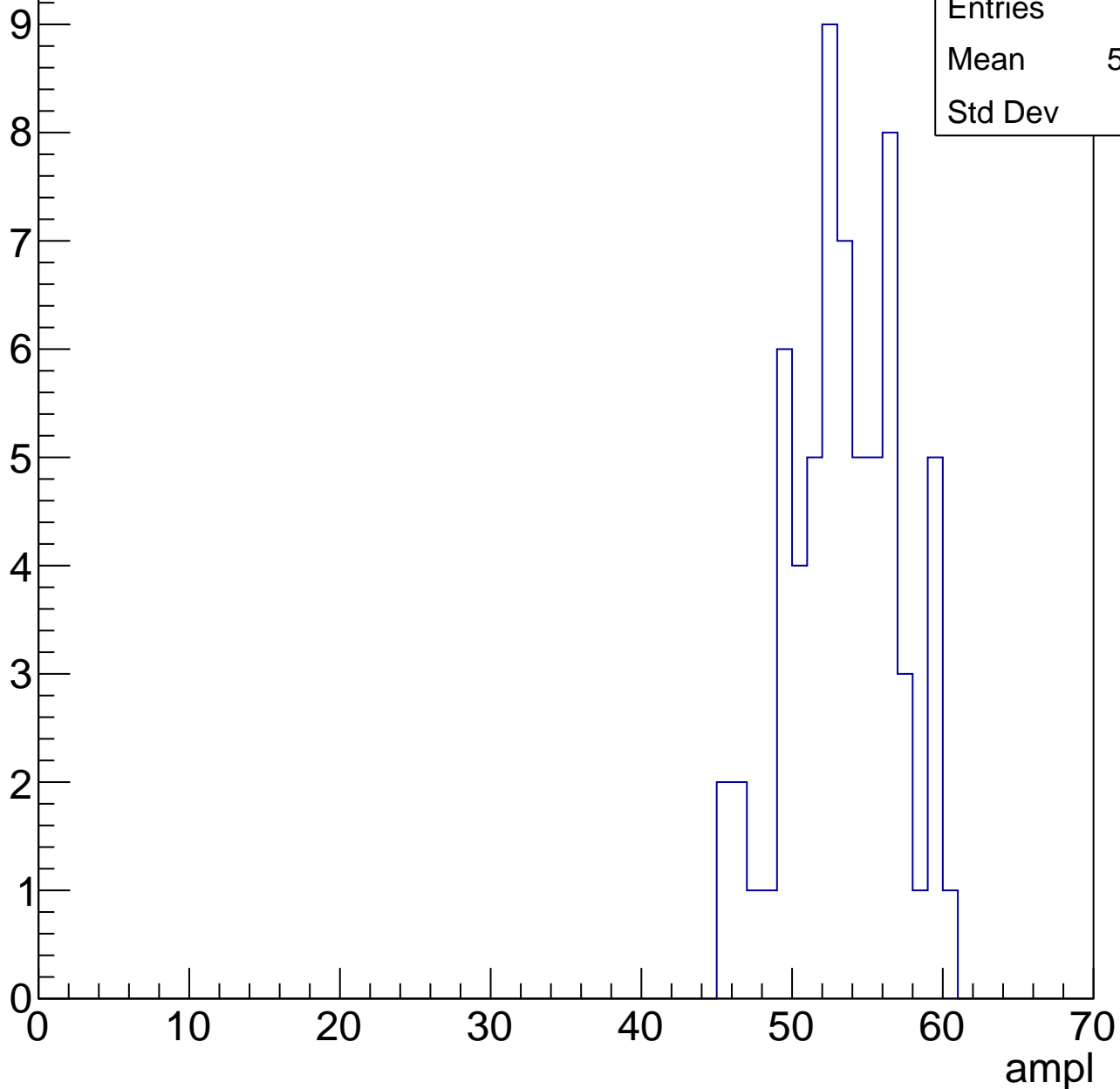
Entries	53
Mean	47.45
Std Dev	3.311



# B1L103S, U3-ch112, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



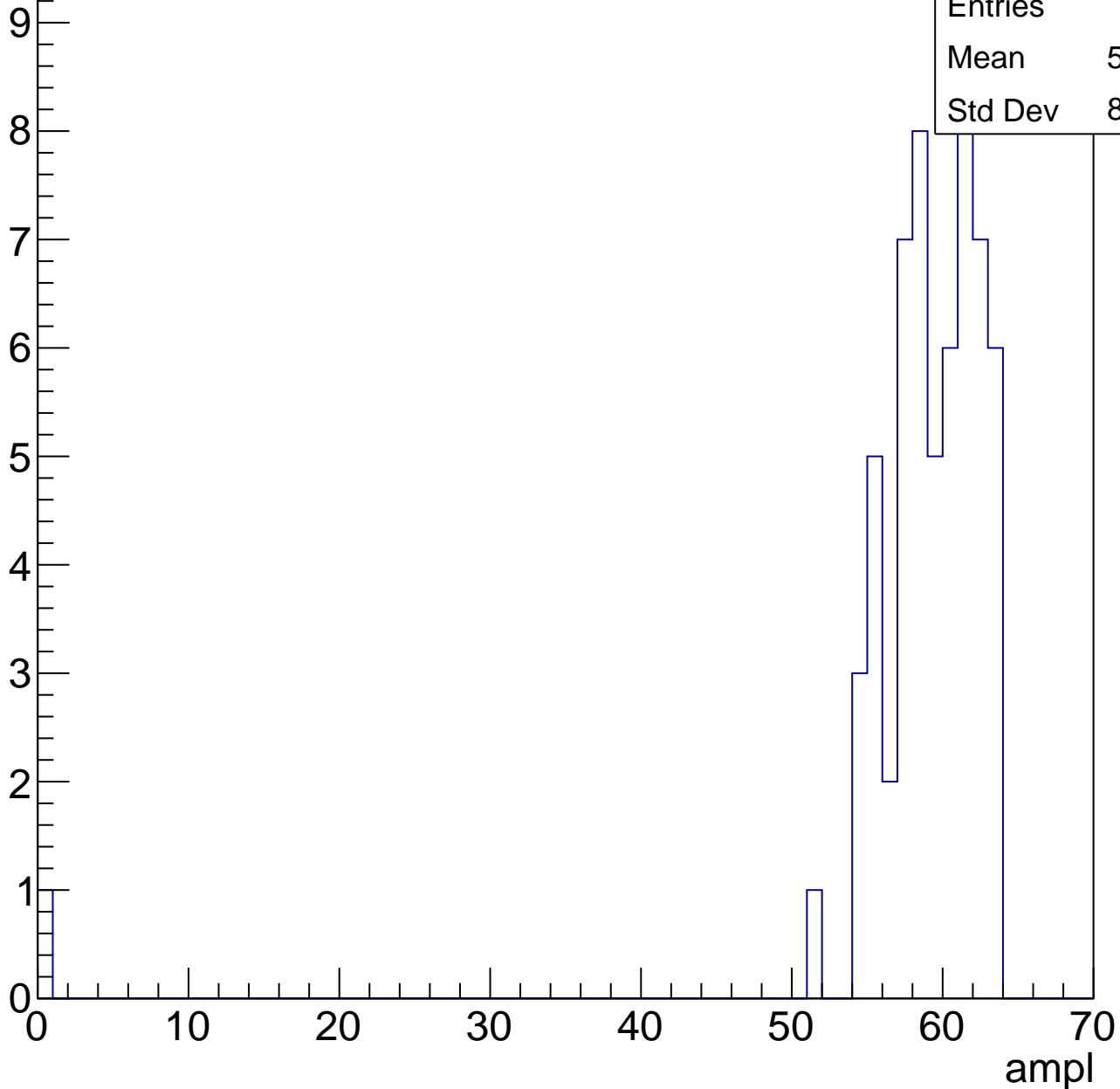
Entries	65
Mean	52.95
Std Dev	3.61

# B1L103S, U3-ch112, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	57.98
Std Dev	8.055



# B1L103S, U3-ch112, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

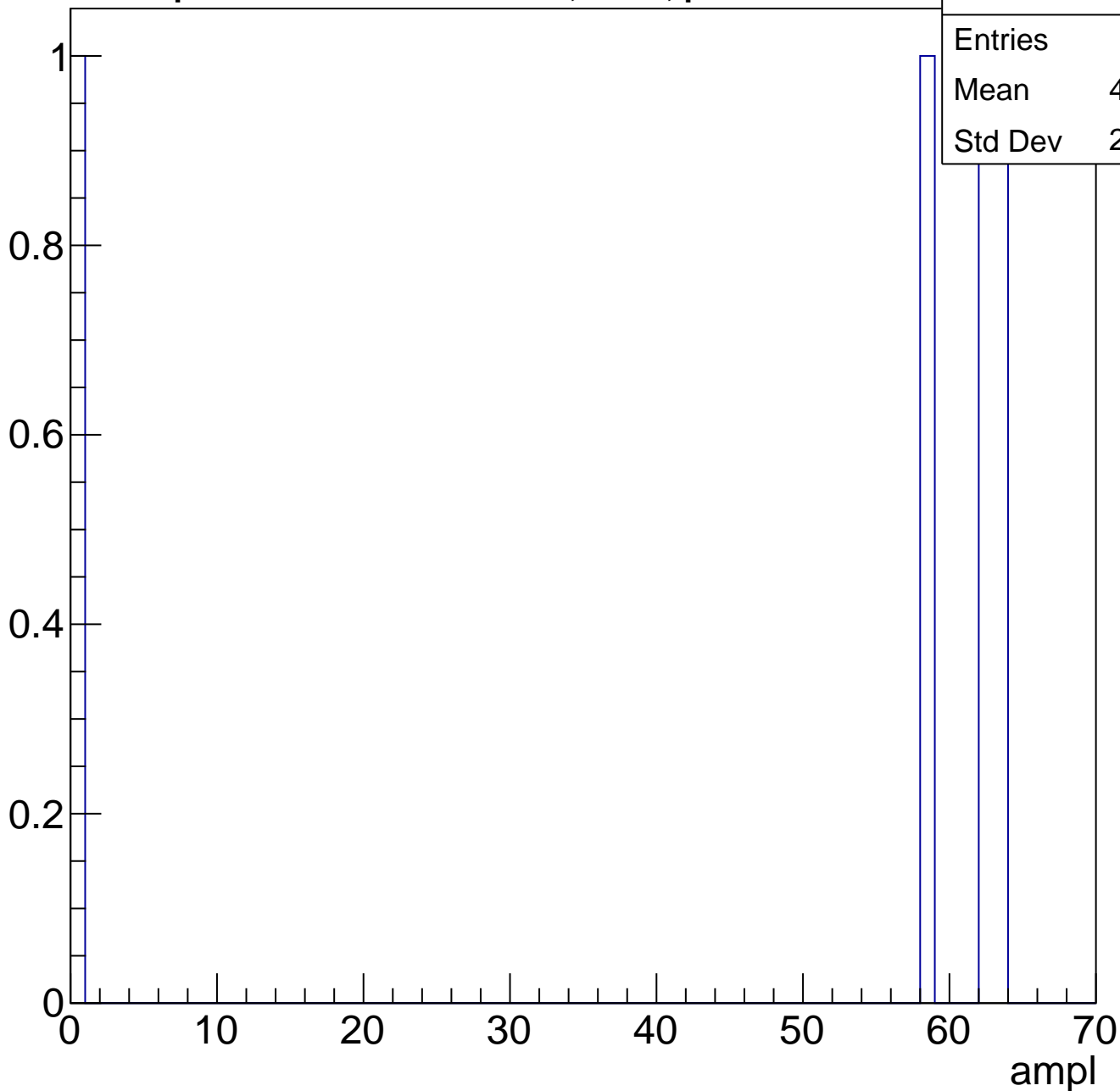
Entries	9
Mean	61.56
Std Dev	1.257



# B1L103S, U3-ch112, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch113, adc0

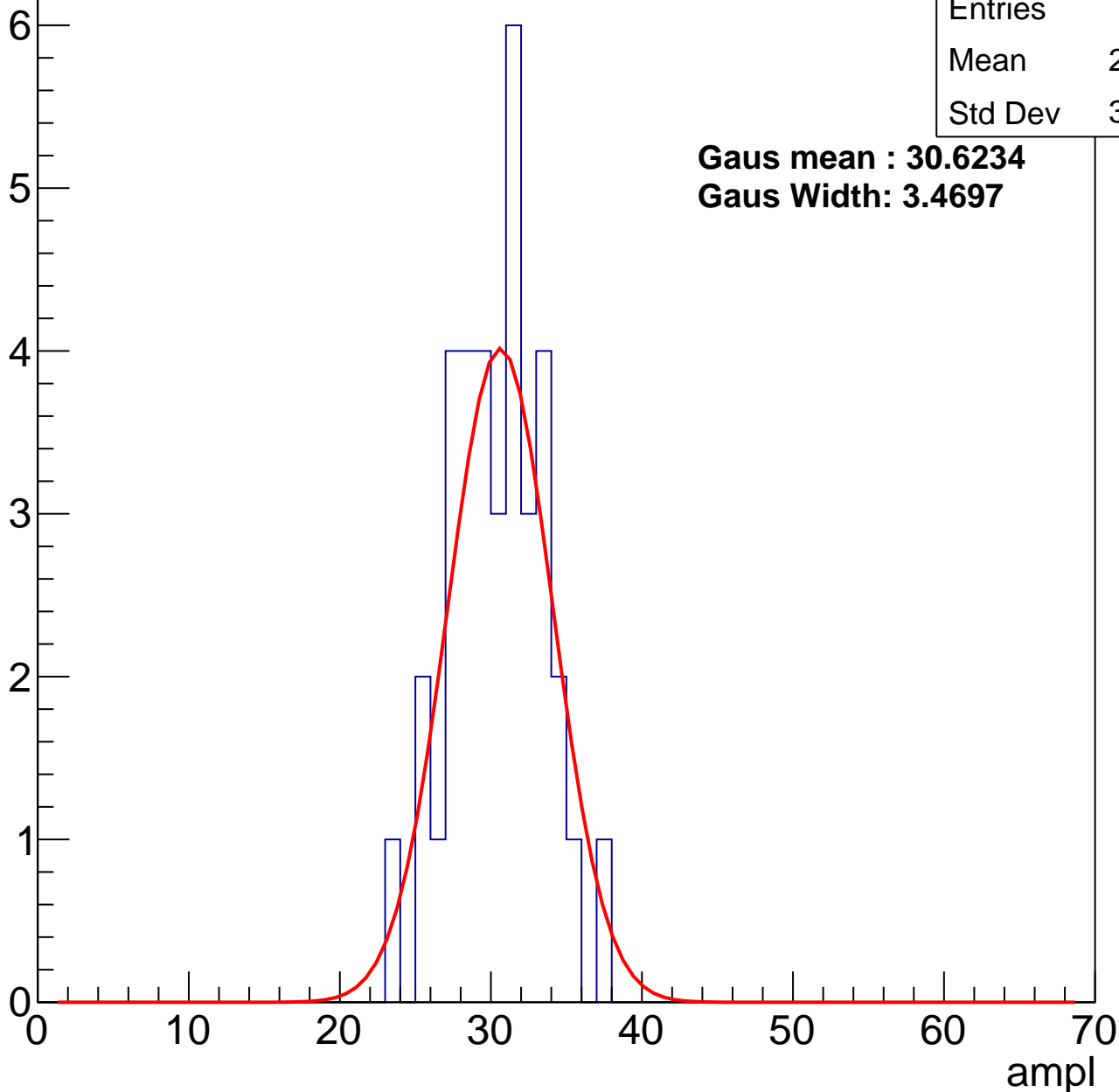
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	36
Mean	29.97
Std Dev	3.032

**Gaus mean : 30.6234**

**Gaus Width: 3.4697**



# B1L103S, U3-ch113, adc1

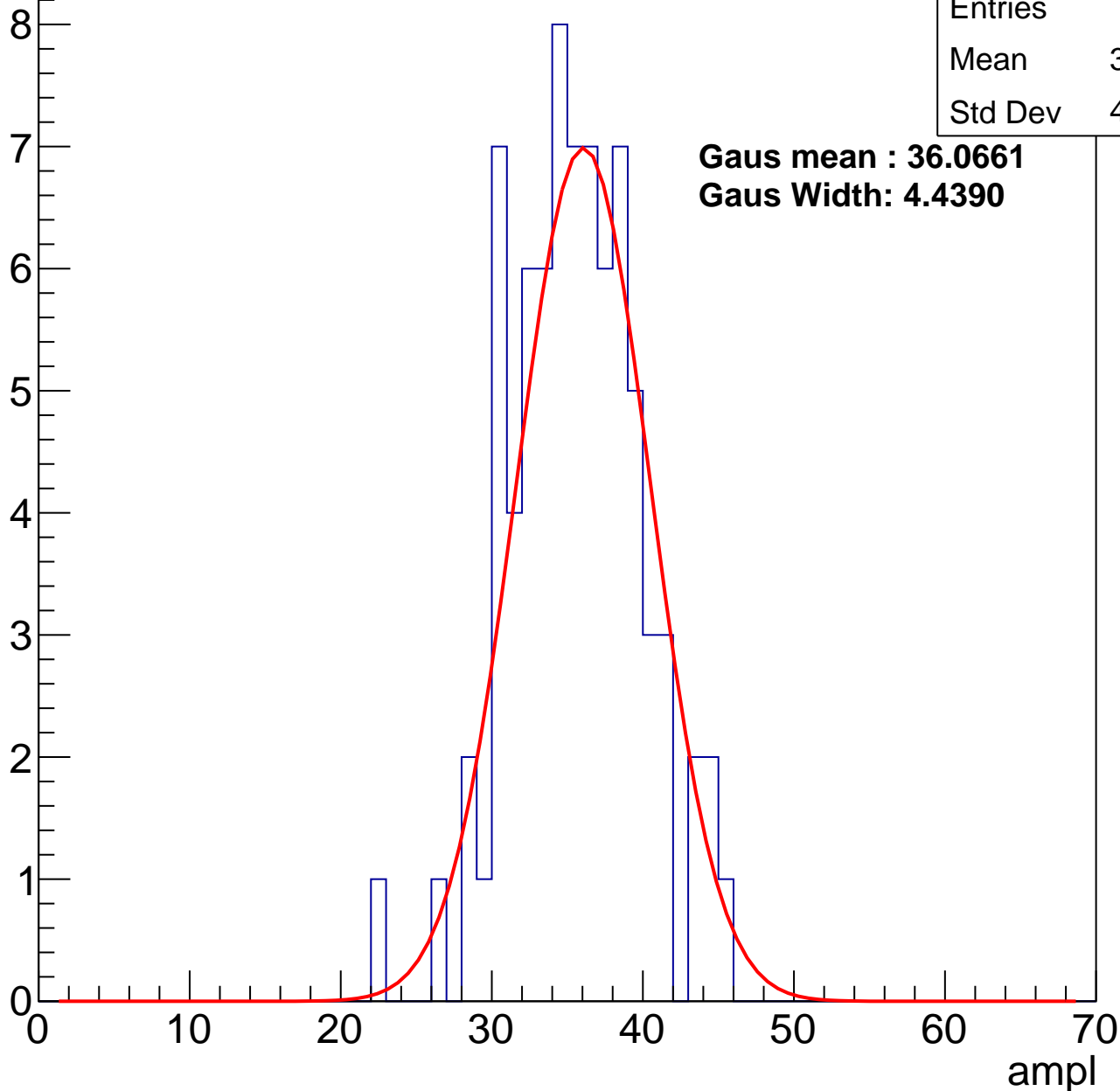
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	79
Mean	35.08
Std Dev	4.292

**Gaus mean : 36.0661**

**Gaus Width: 4.4390**



# B1L103S, U3-ch113, adc2

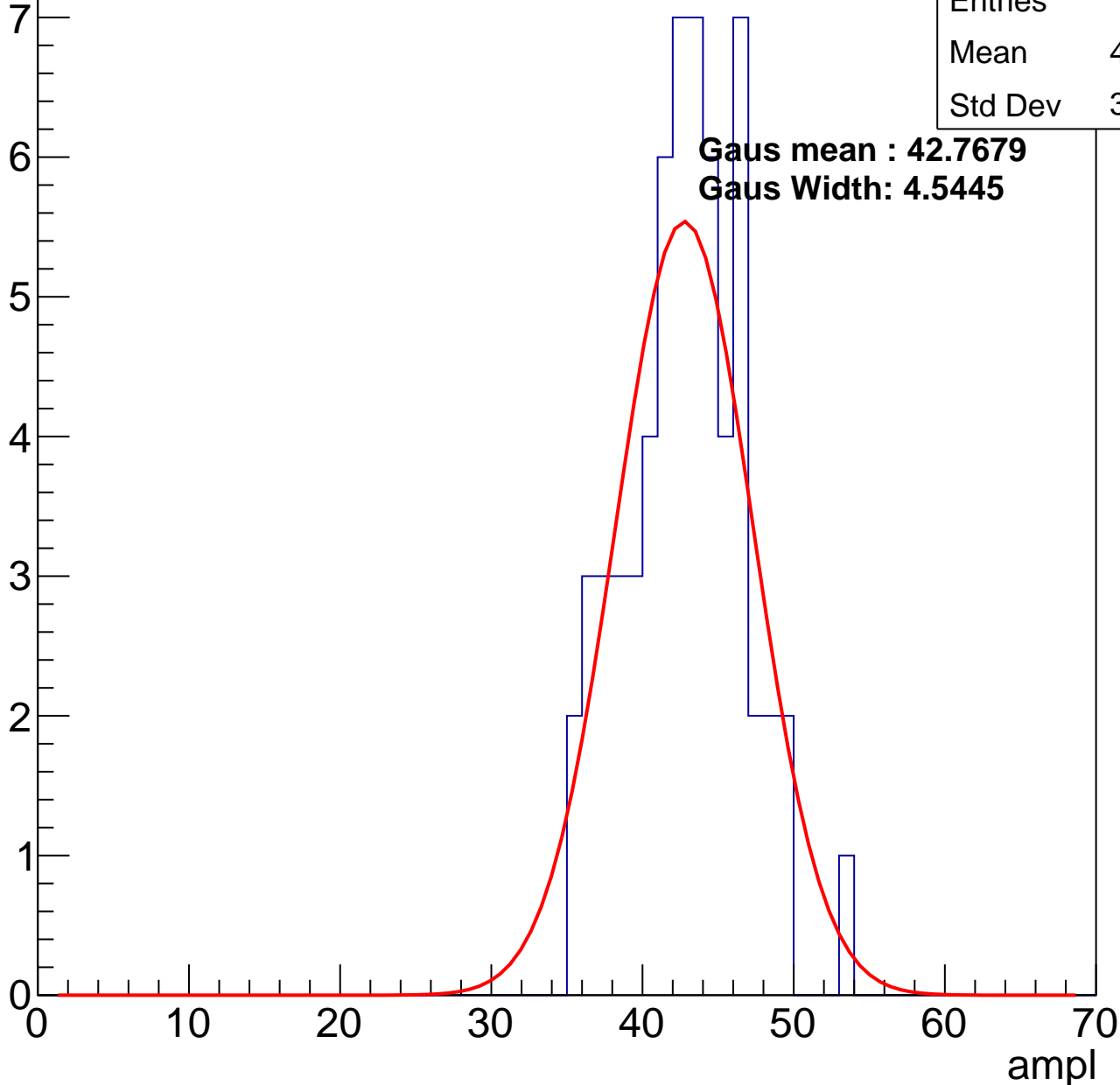
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	42.39
Std Dev	3.786

**Gaus mean : 42.7679**

**Gaus Width: 4.5445**

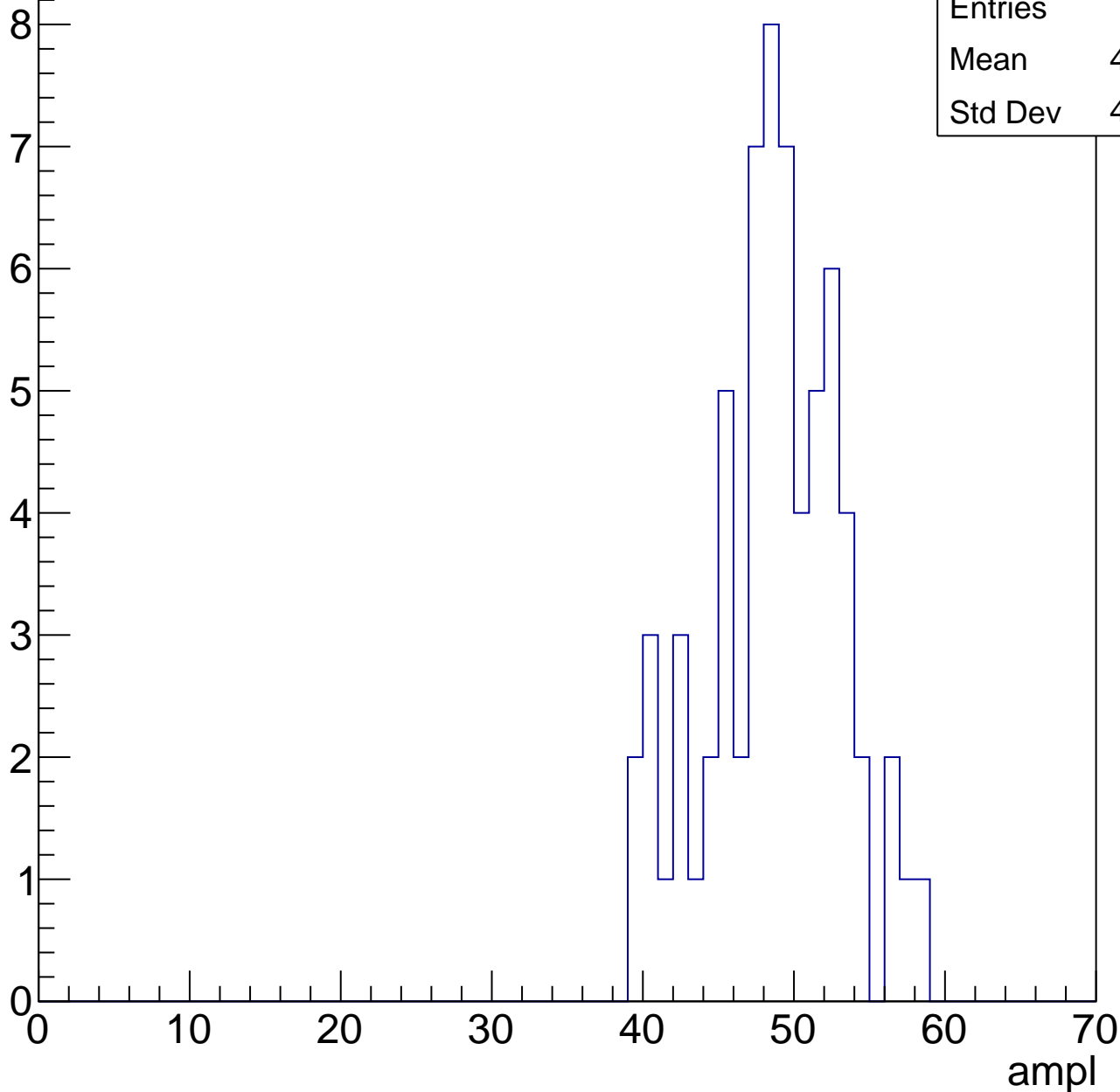


# B1L103S, U3-ch113, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	48.23
Std Dev	4.386

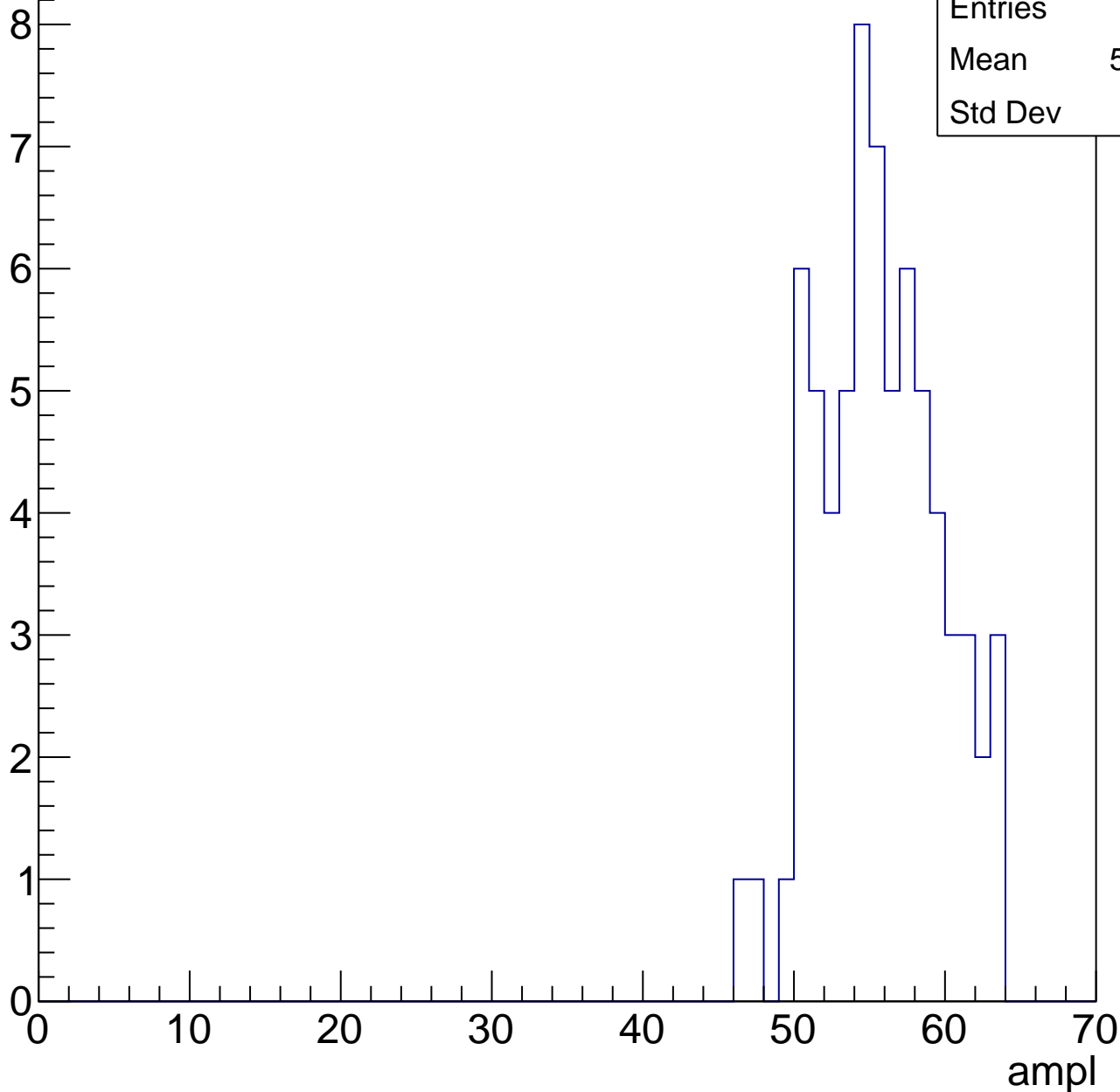


# B1L103S, U3-ch113, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	55.23
Std Dev	3.96

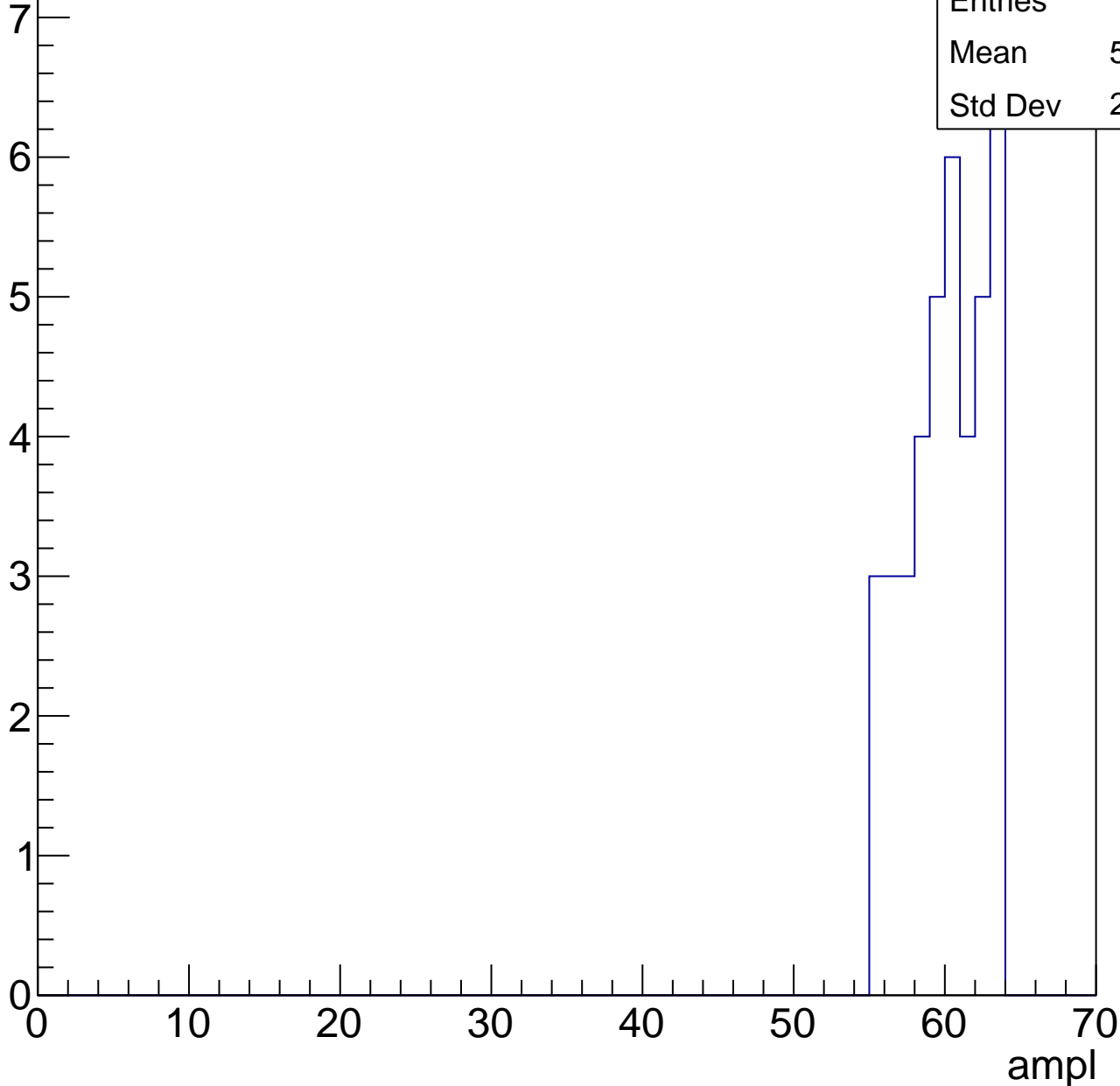


# B1L103S, U3-ch113, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	40
Mean	59.65
Std Dev	2.515



# B1L103S, U3-ch113, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

3

2.5

2

1.5

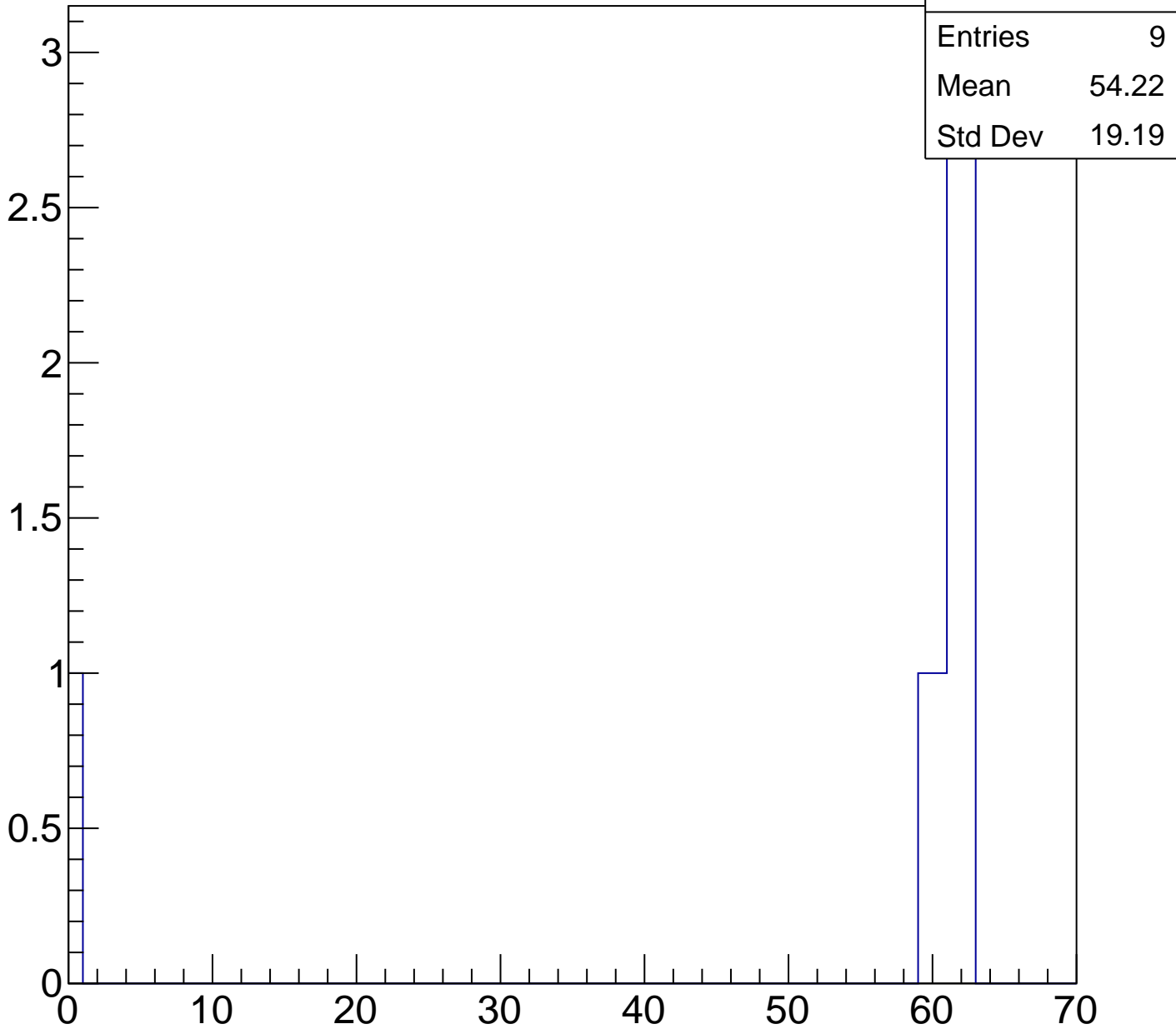
1

0.5

0

ampl

Entries	9
Mean	54.22
Std Dev	19.19





# B1L103S, U3-ch113, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U3-ch114, adc0

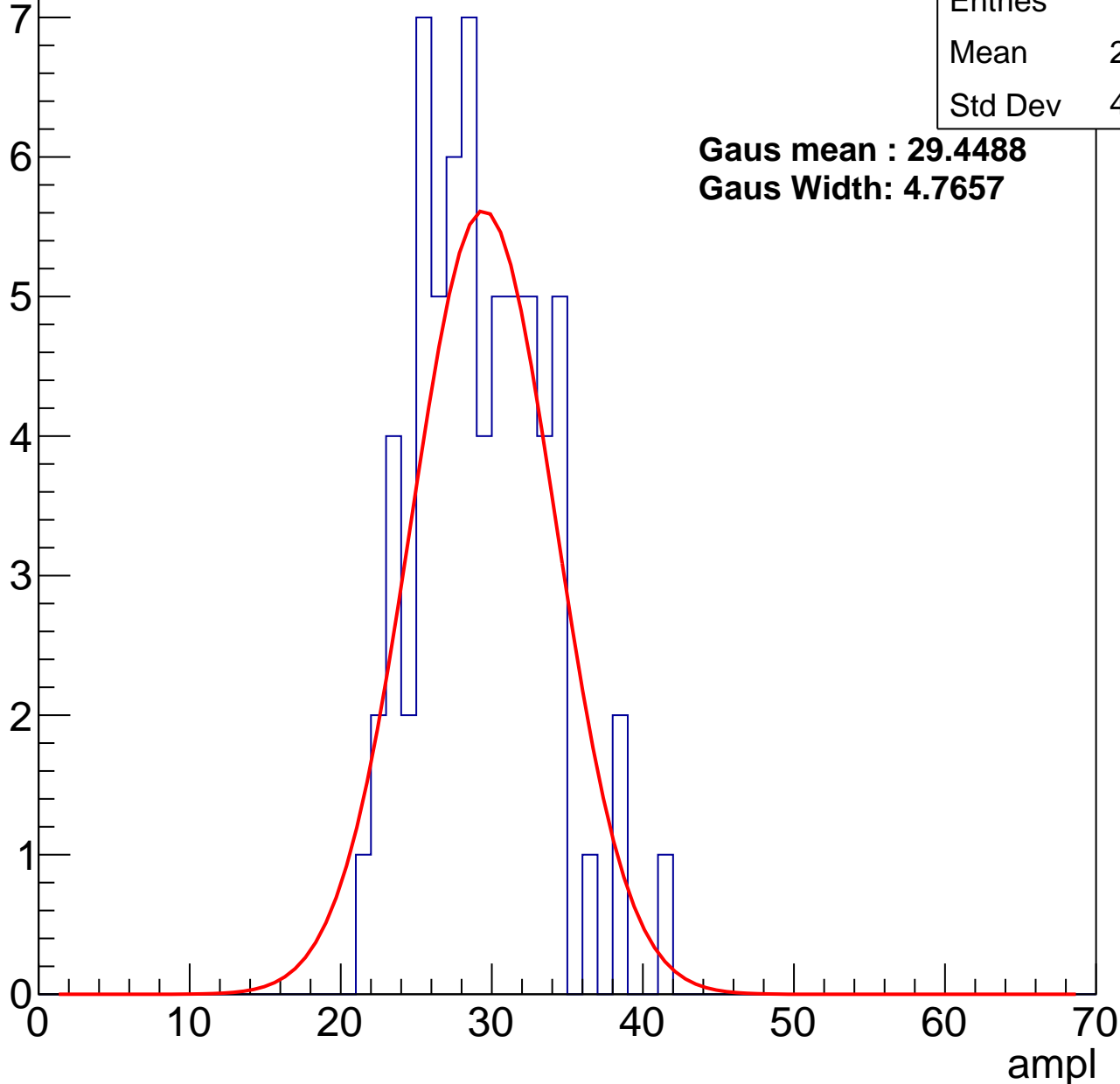
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	28.85
Std Dev	4.186

**Gaus mean : 29.4488**

**Gaus Width: 4.7657**



# B1L103S, U3-ch114, adc1

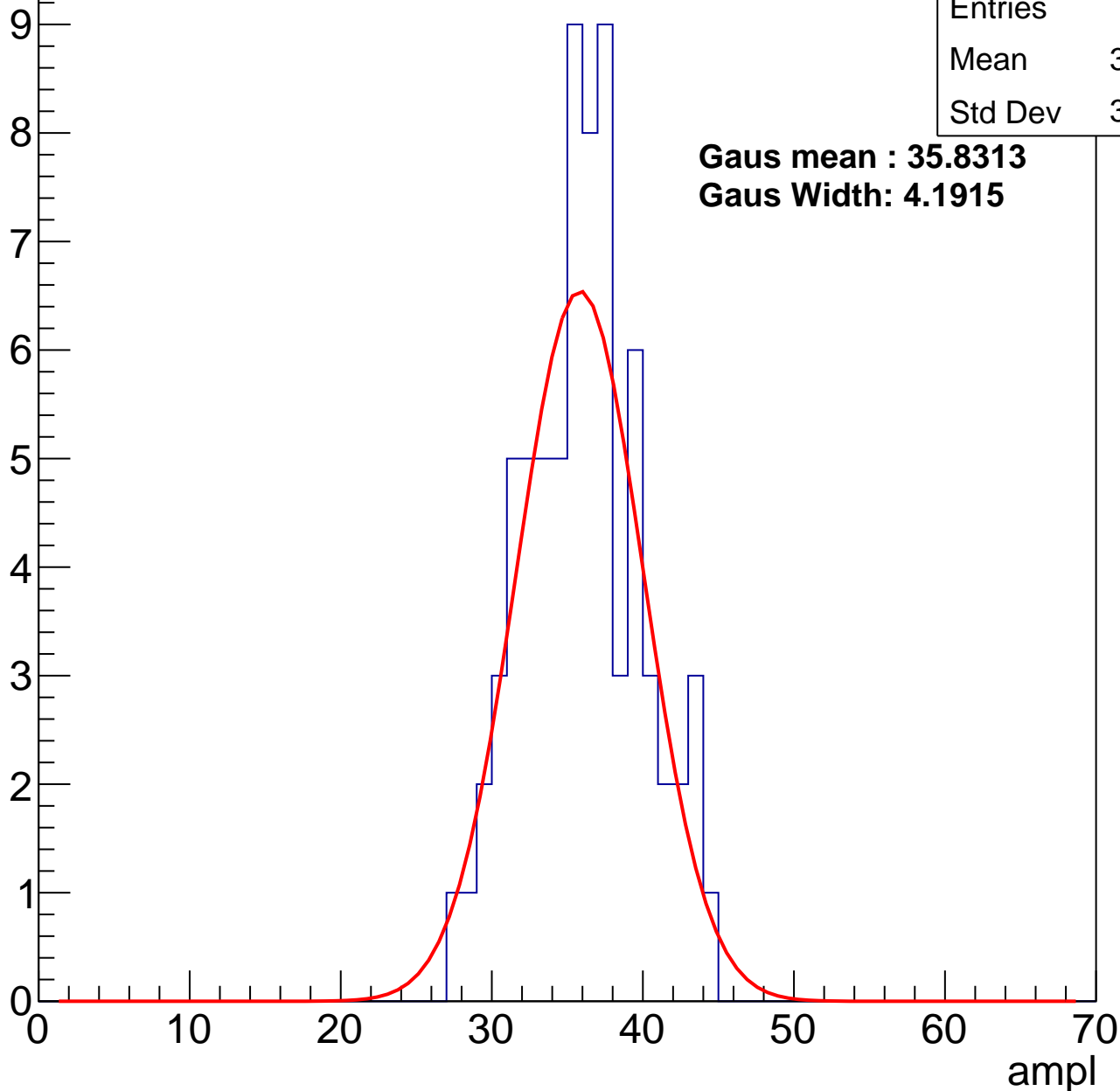
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	35.56
Std Dev	3.832

**Gaus mean : 35.8313**

**Gaus Width: 4.1915**



# B1L103S, U3-ch114, adc2

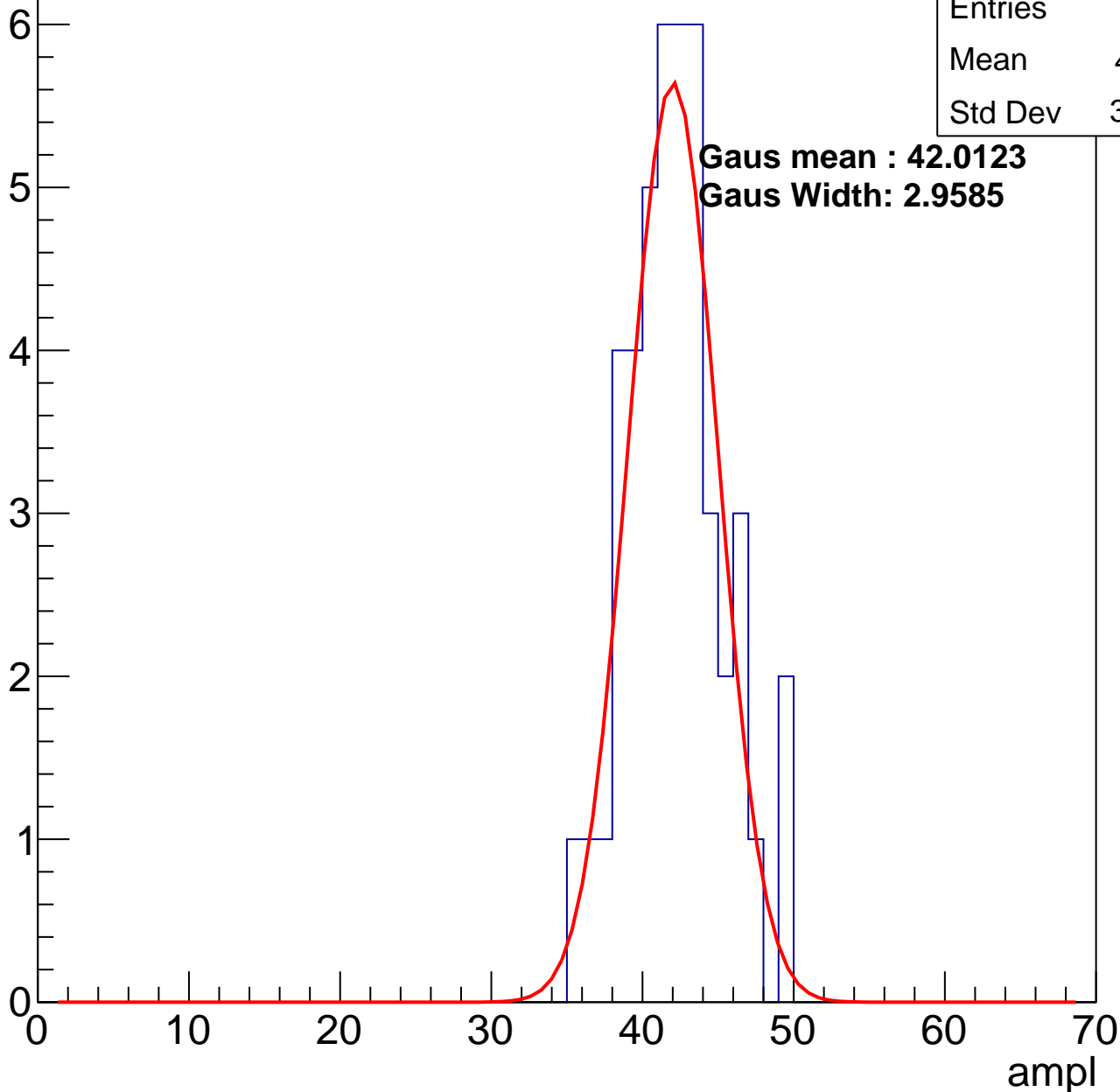
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	45
Mean	41.71
Std Dev	3.124

**Gaus mean : 42.0123**

**Gaus Width: 2.9585**

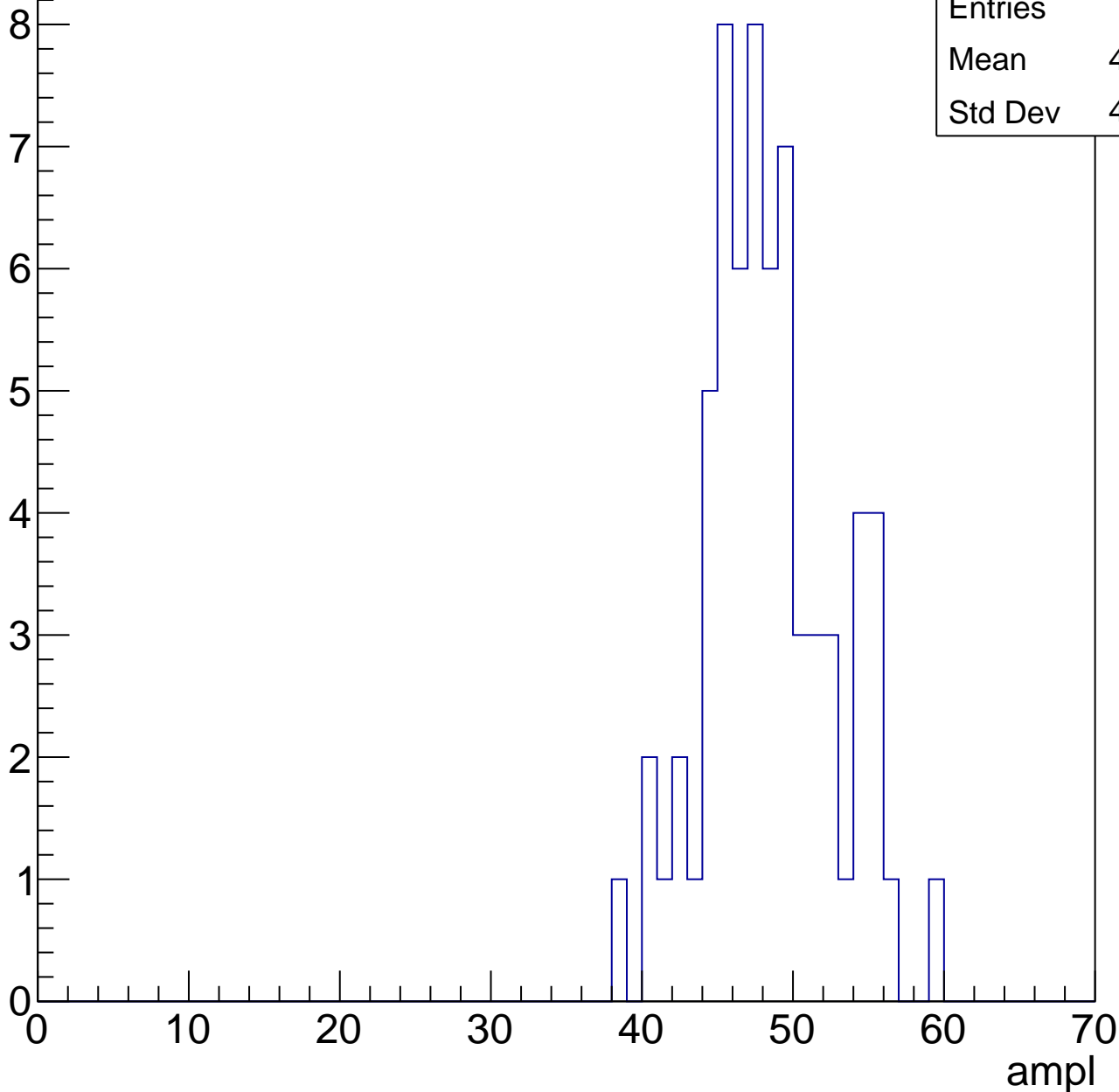


# B1L103S, U3-ch114, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	47.94
Std Dev	4.235

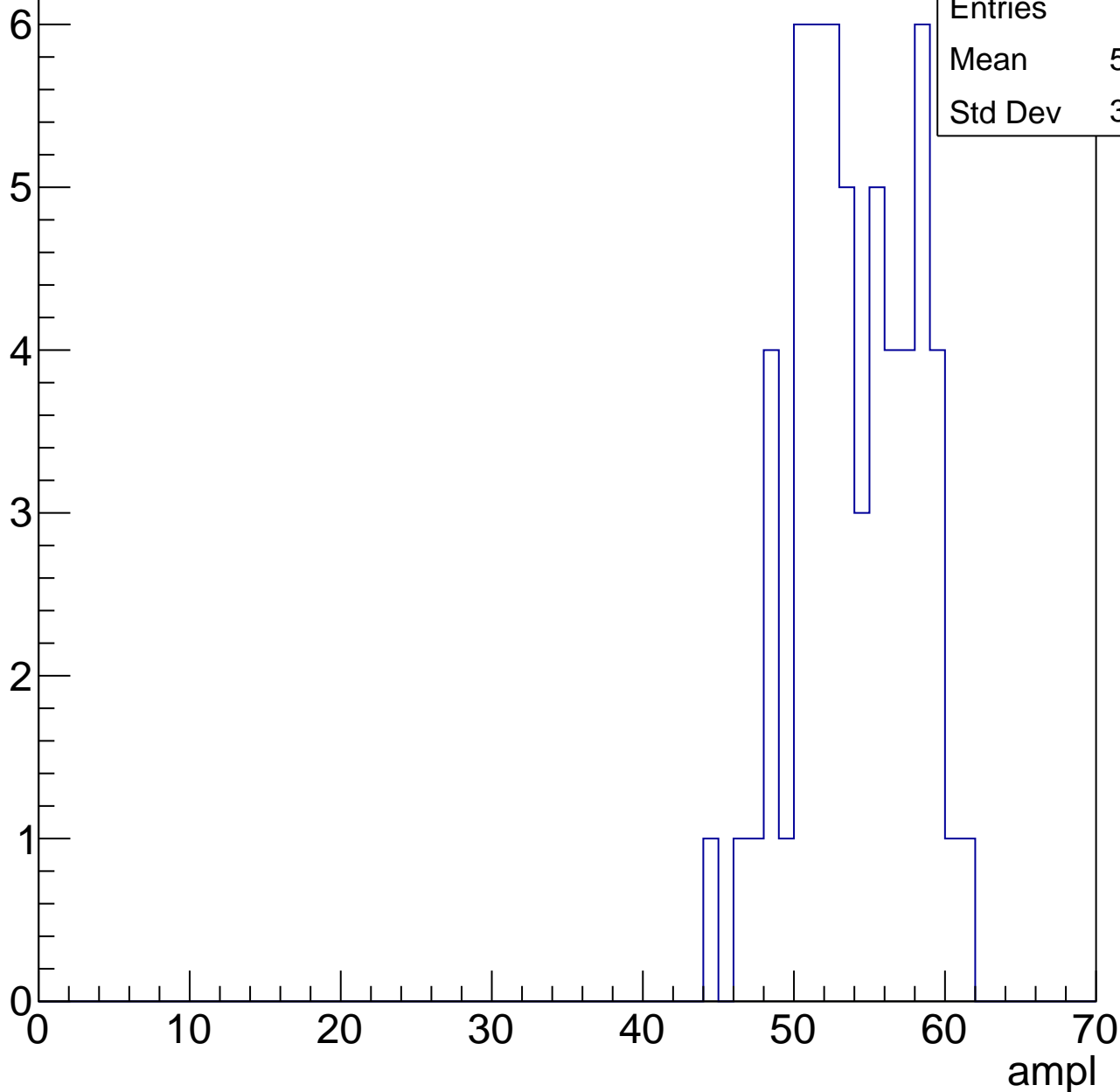


# B1L103S, U3-ch114, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	53.47
Std Dev	3.868

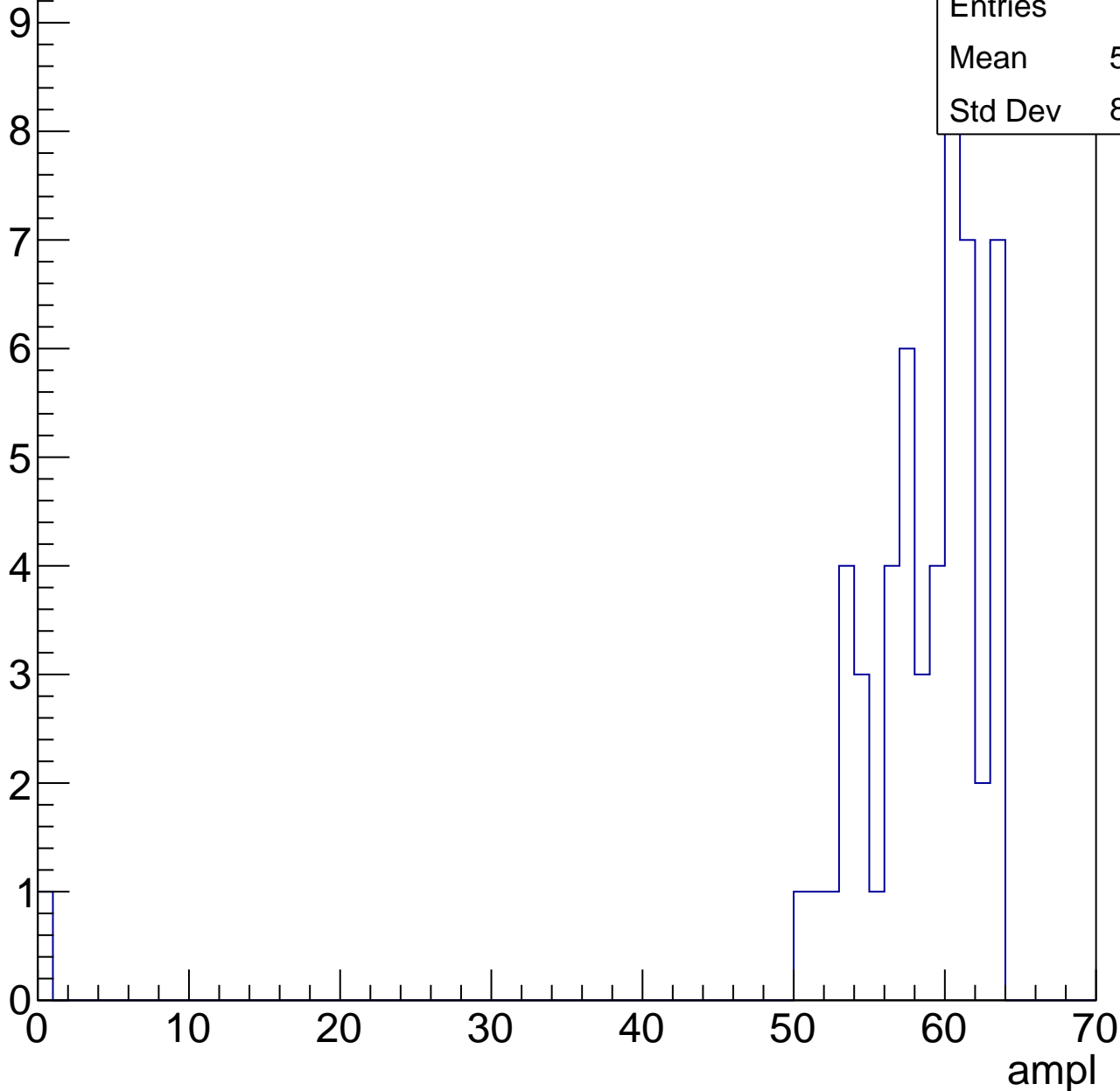


# B1L103S, U3-ch114, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	57.22
Std Dev	8.574

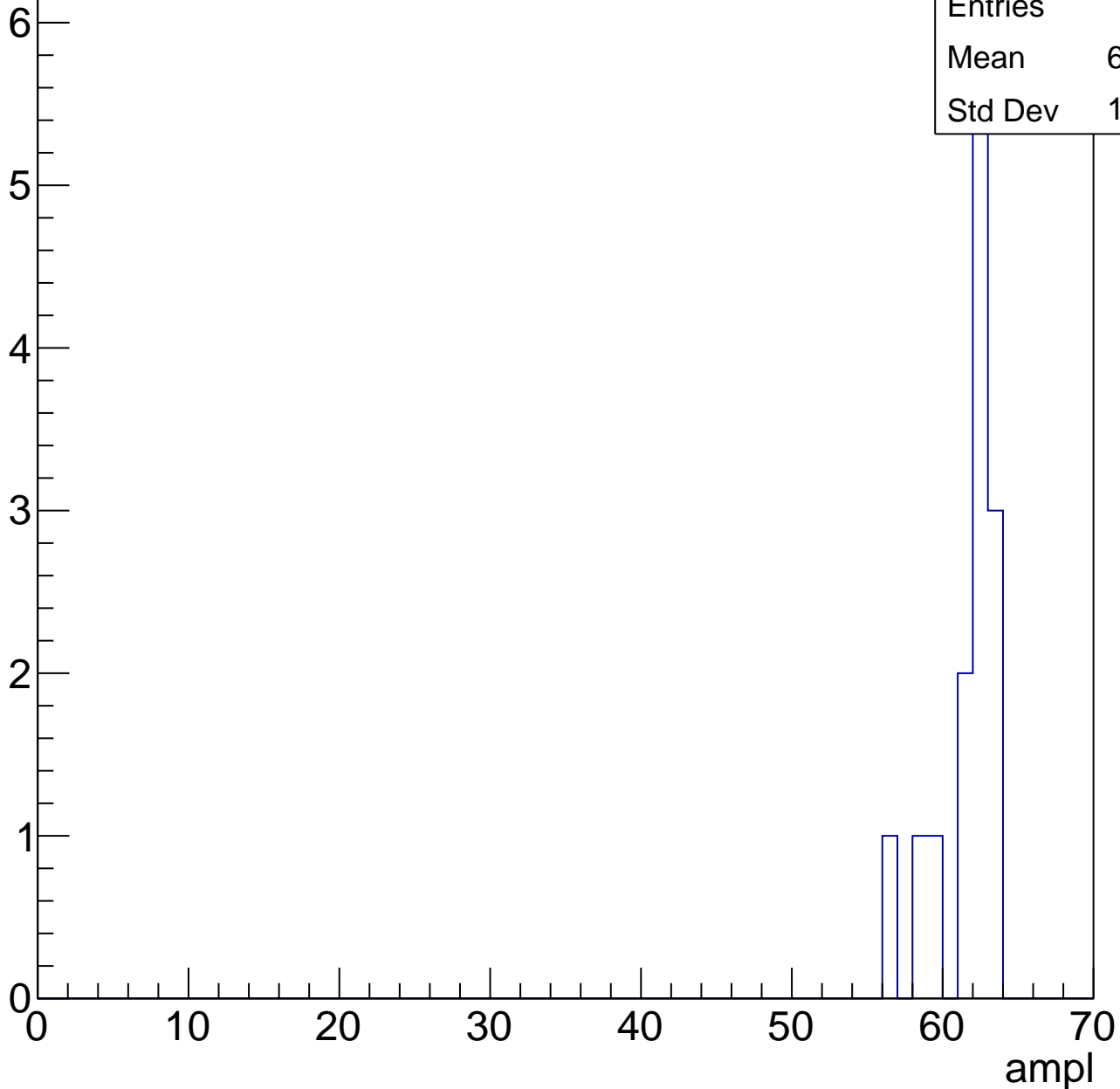


# B1L103S, U3-ch114, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	14
Mean	61.14
Std Dev	1.995

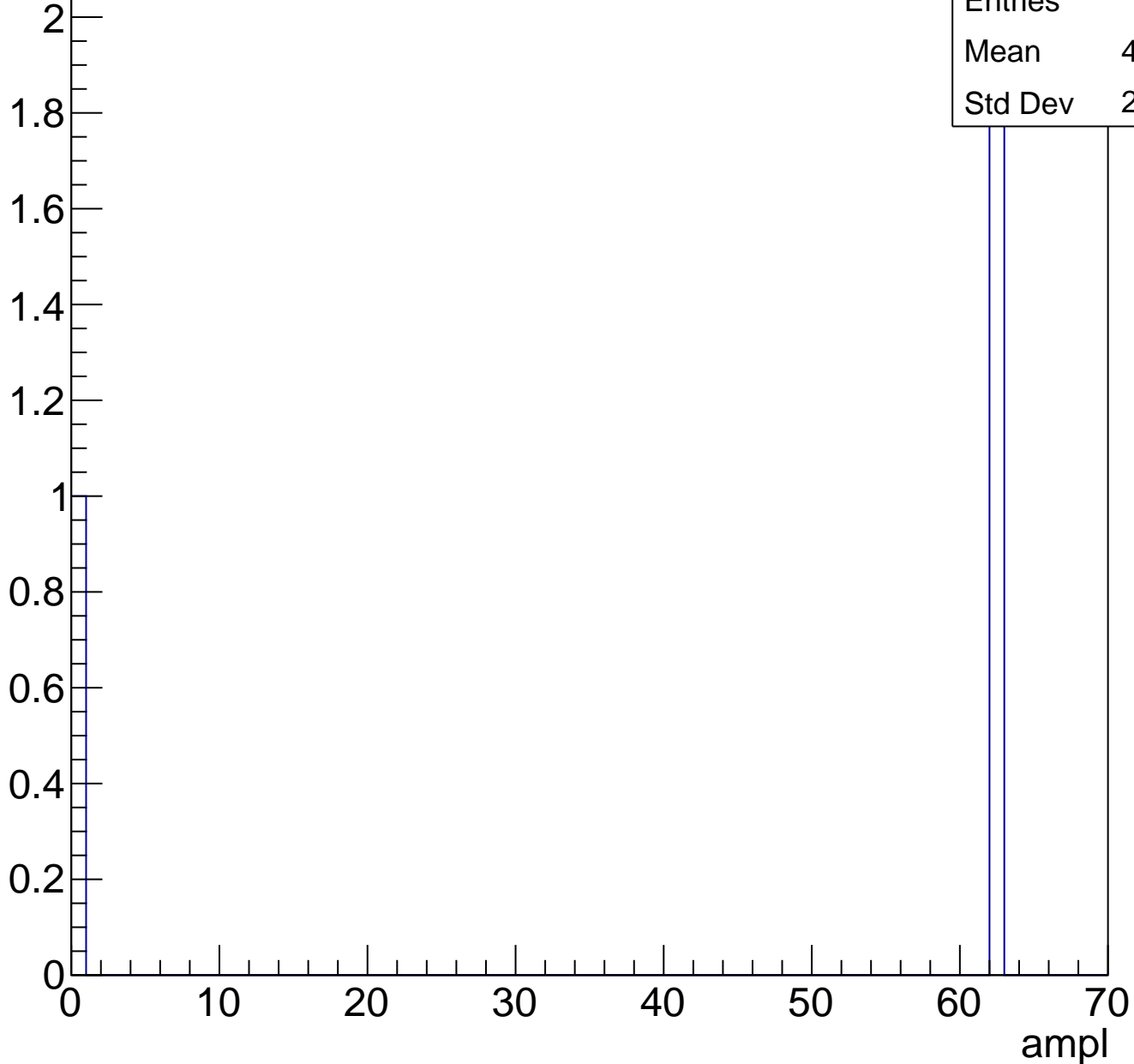




# B1L103S, U3-ch114, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch115, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	83
Mean	28.39
Std Dev	4.889

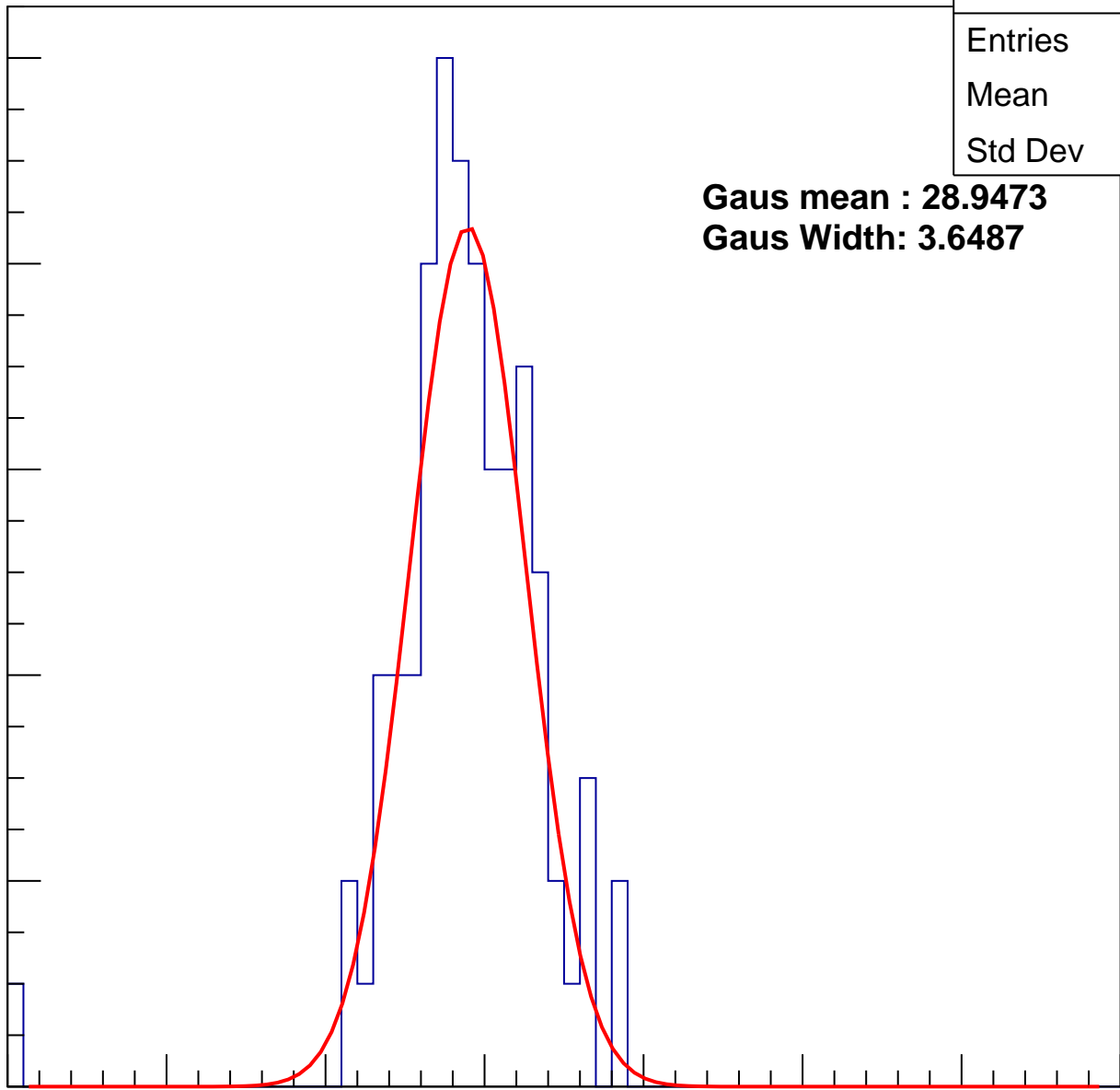
**Gaus mean : 28.9473**

**Gaus Width: 3.6487**

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U3-ch115, adc1

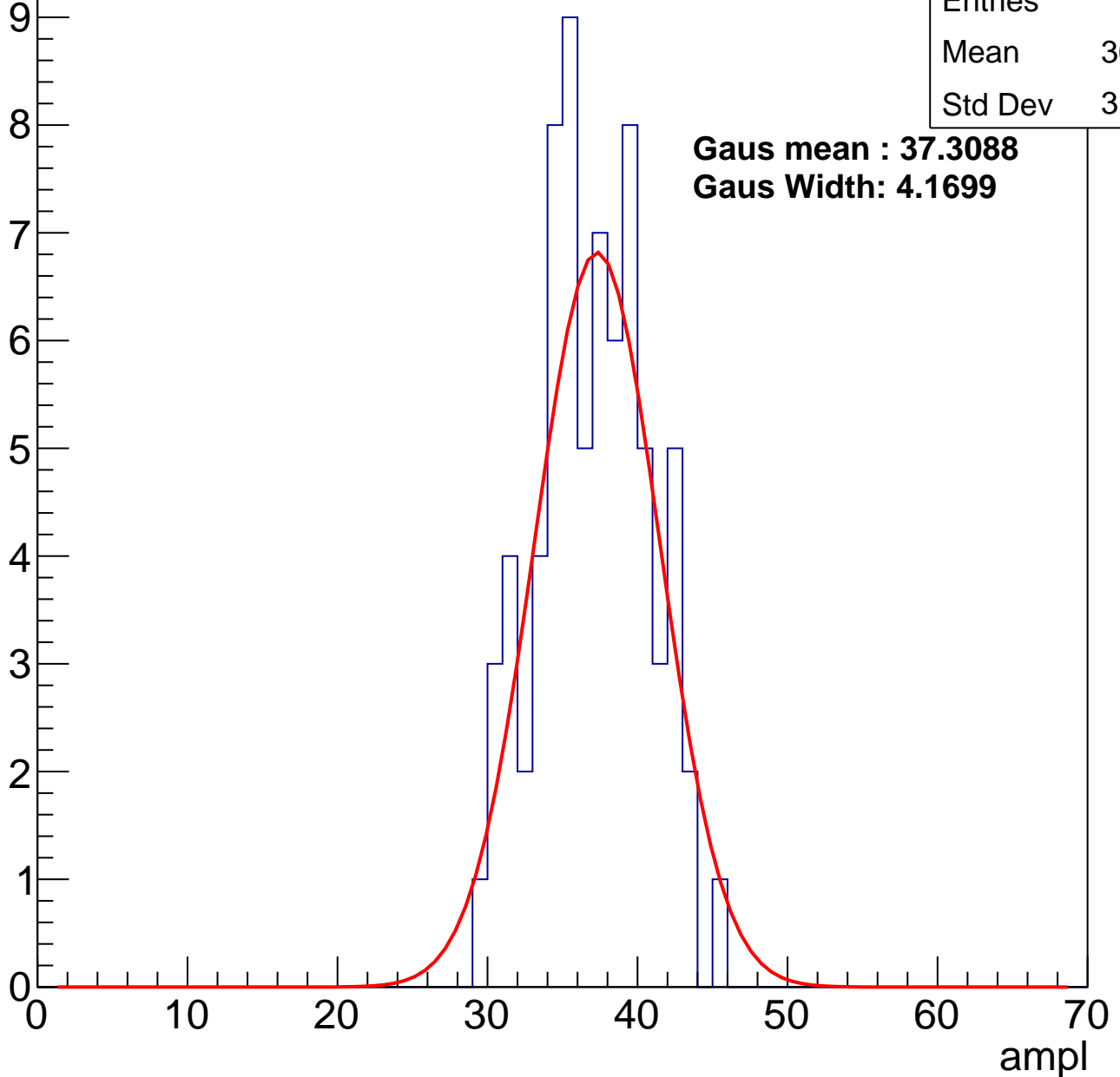
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	36.56
Std Dev	3.626

**Gaus mean : 37.3088**

**Gaus Width: 4.1699**



# B1L103S, U3-ch115, adc2

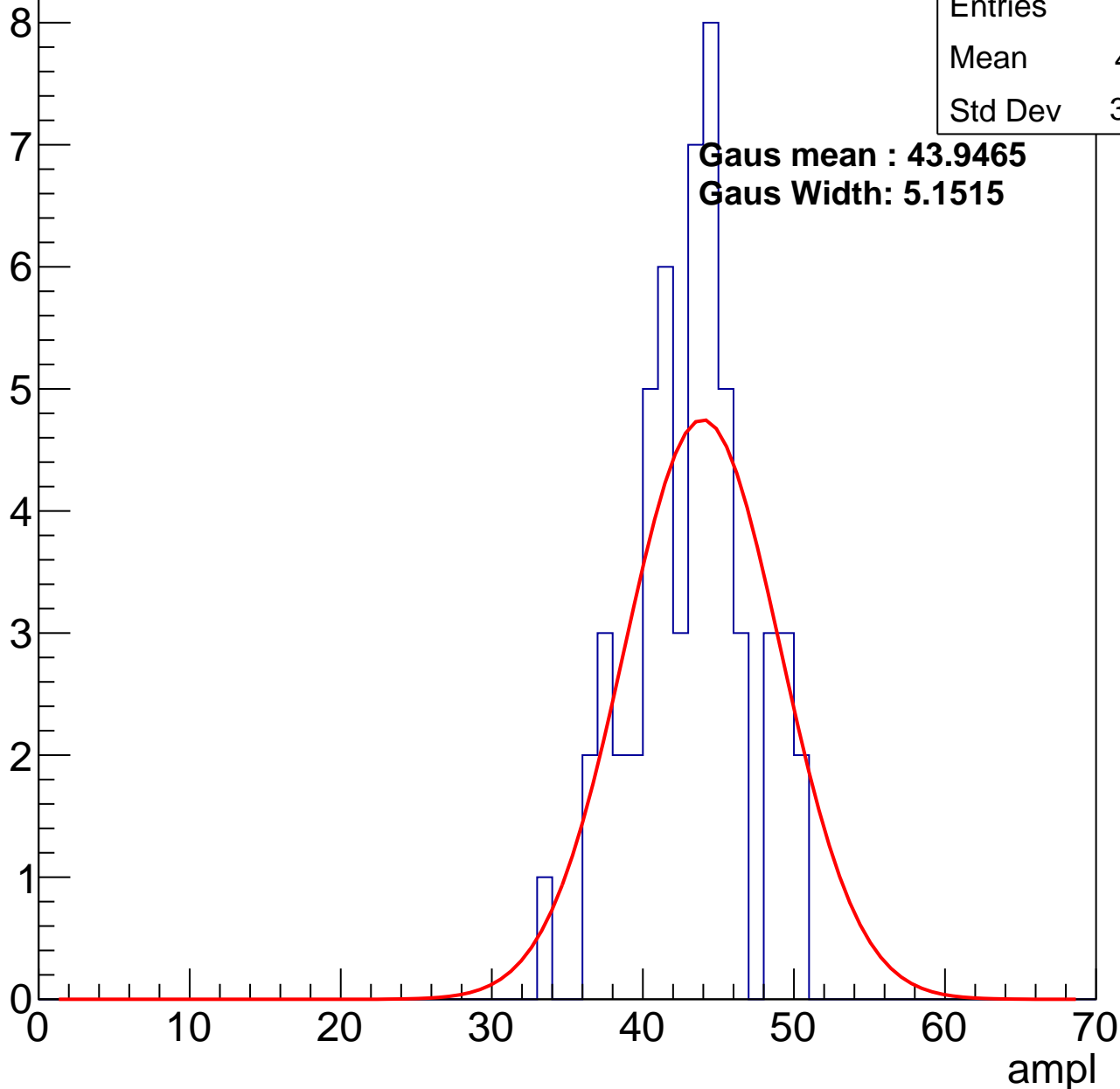
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	42.71
Std Dev	3.793

**Gaus mean : 43.9465**

**Gaus Width: 5.1515**

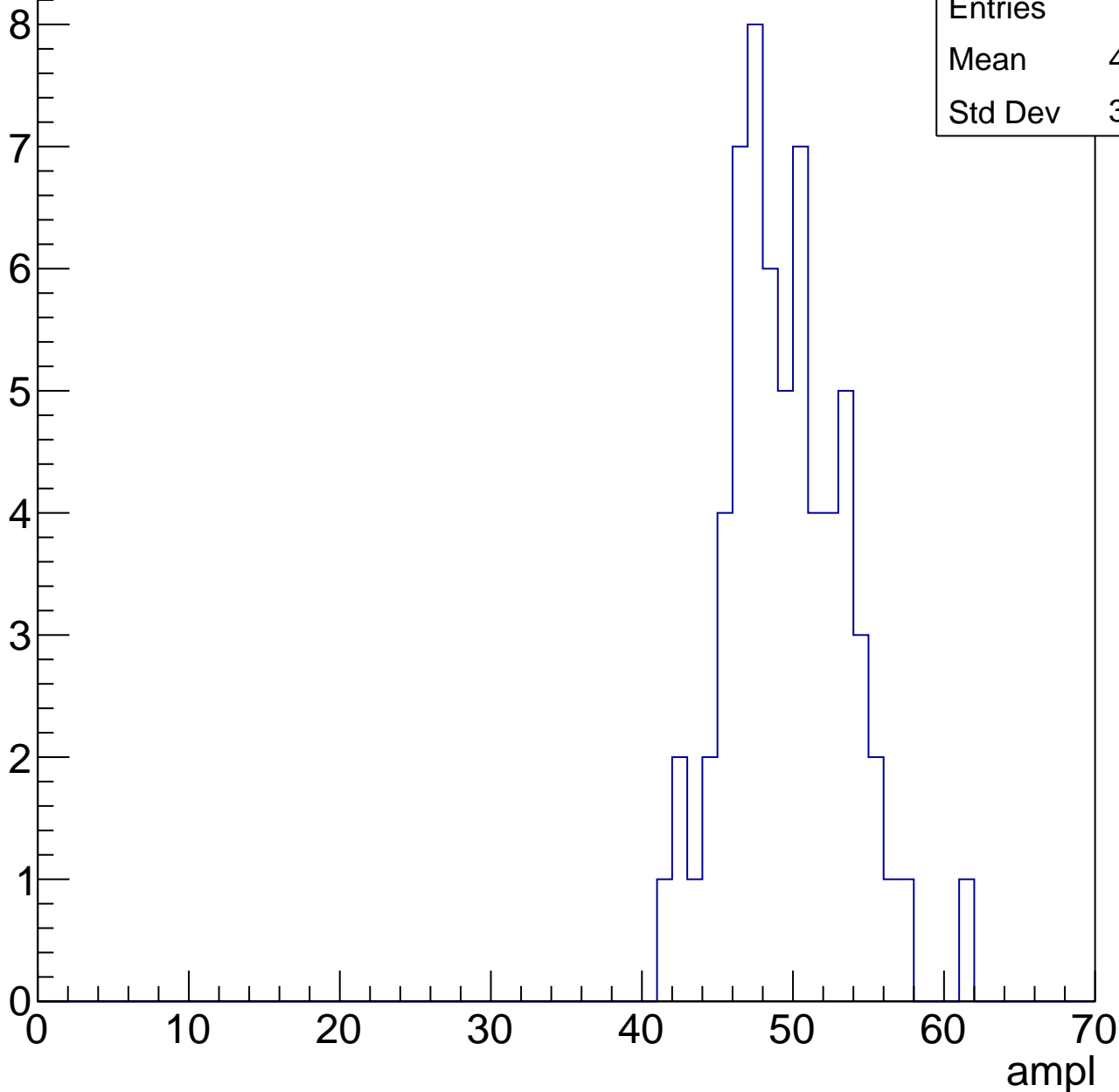


# B1L103S, U3-ch115, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	49.06
Std Dev	3.864

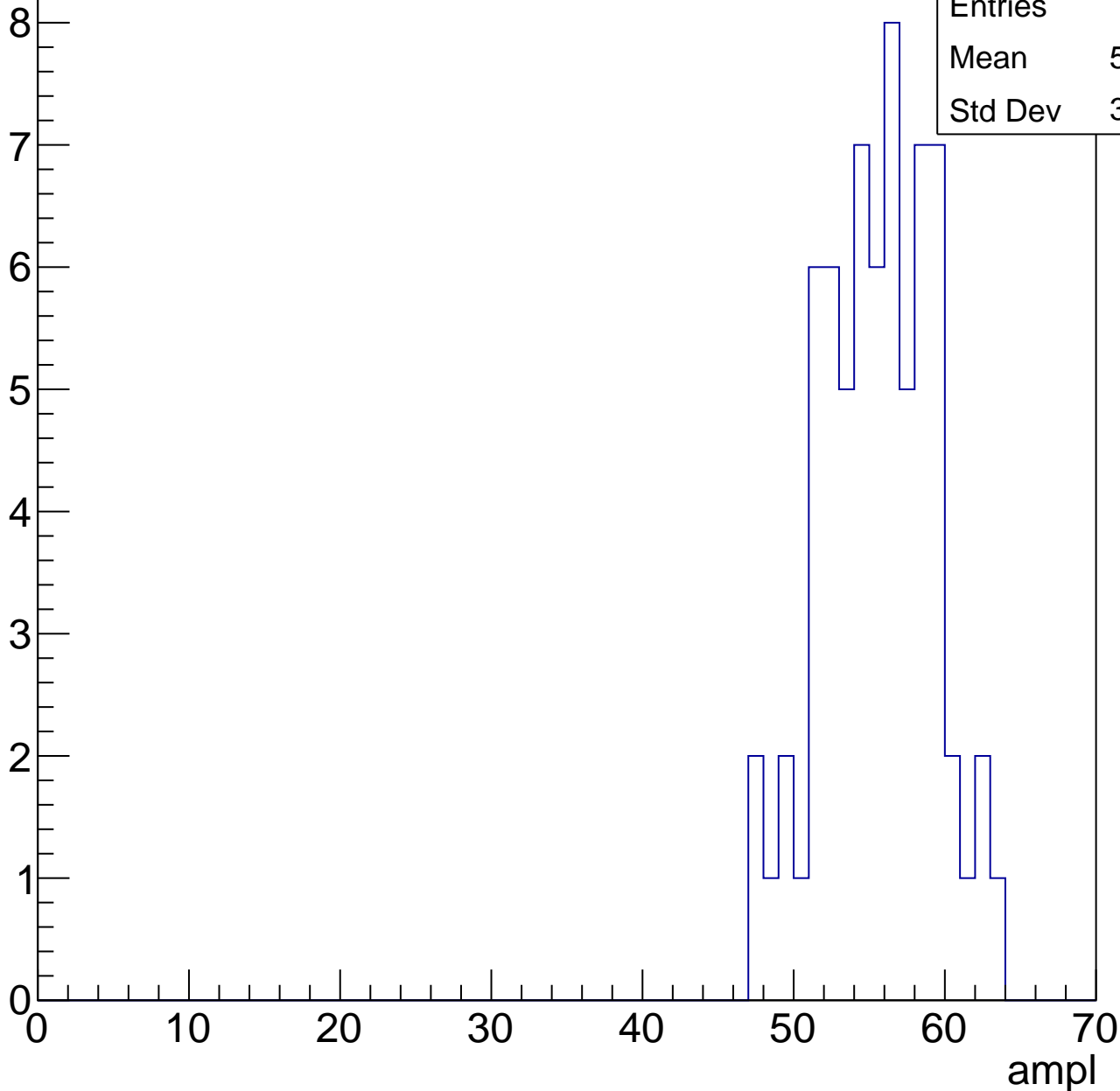


# B1L103S, U3-ch115, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	55.09
Std Dev	3.615

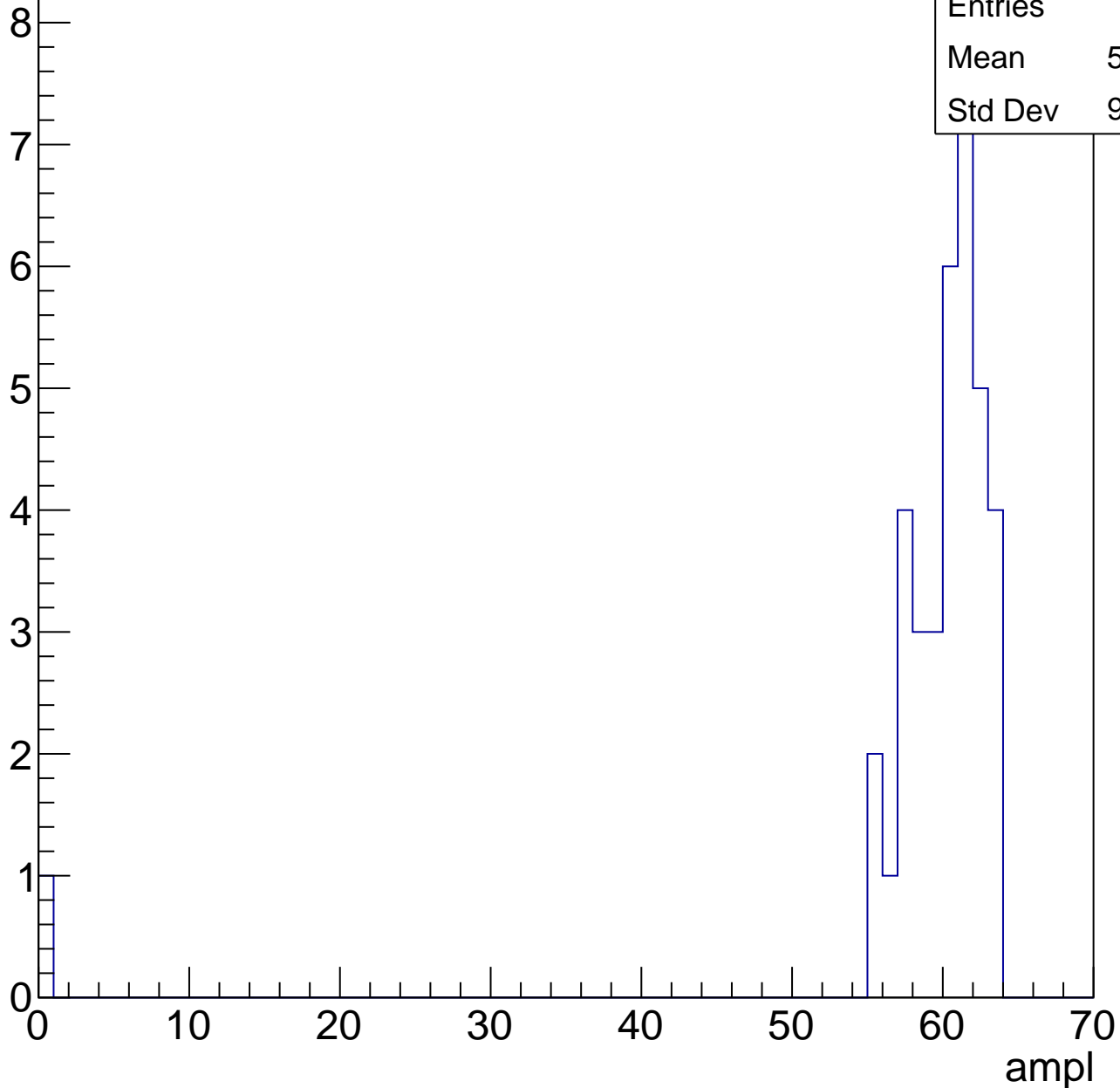


# B1L103S, U3-ch115, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	37
Mean	58.24
Std Dev	9.955

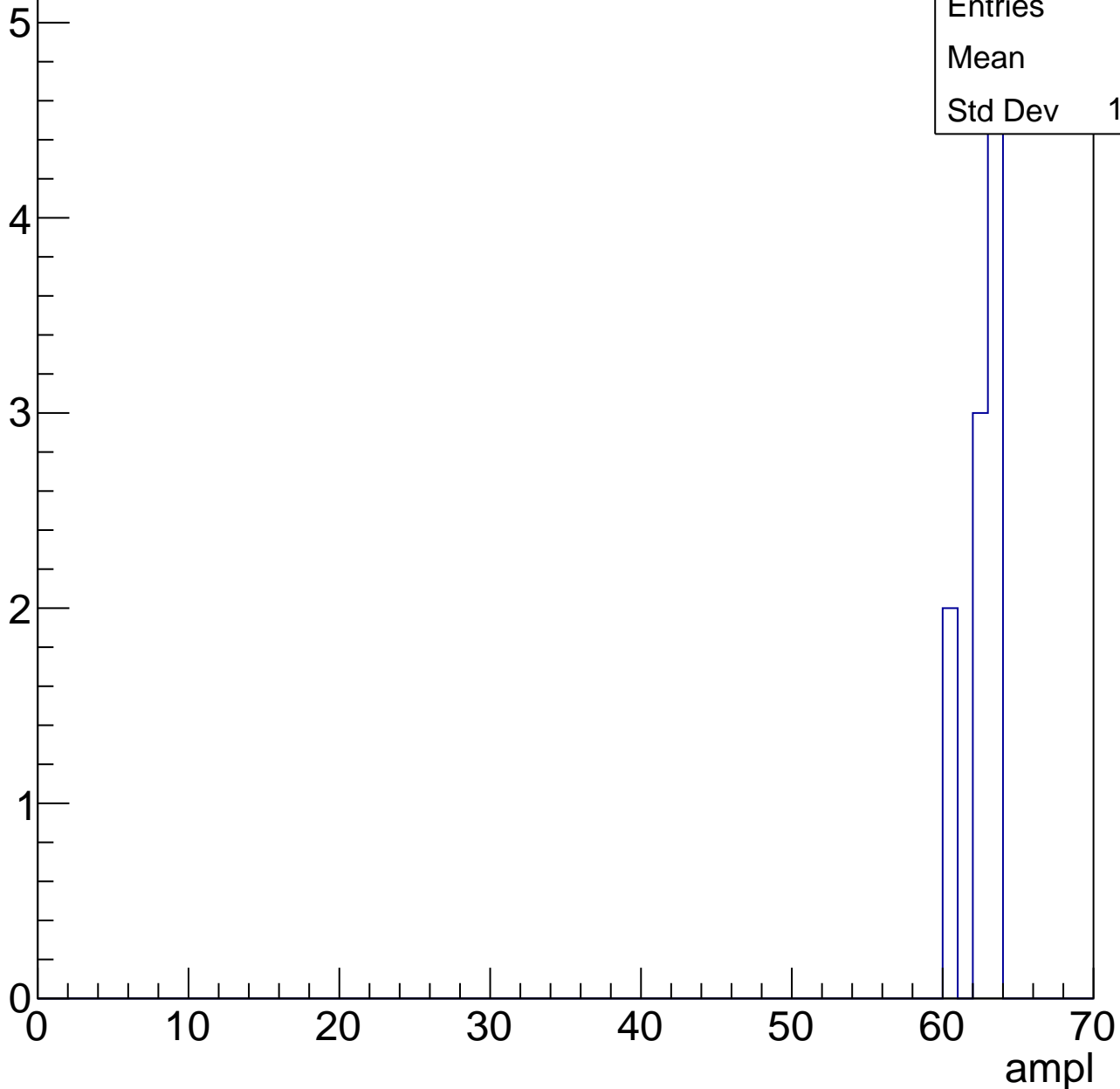


# B1L103S, U3-ch115, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	10
Mean	62.1
Std Dev	1.136





# B1L103S, U3-ch115, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U3-ch116, adc0

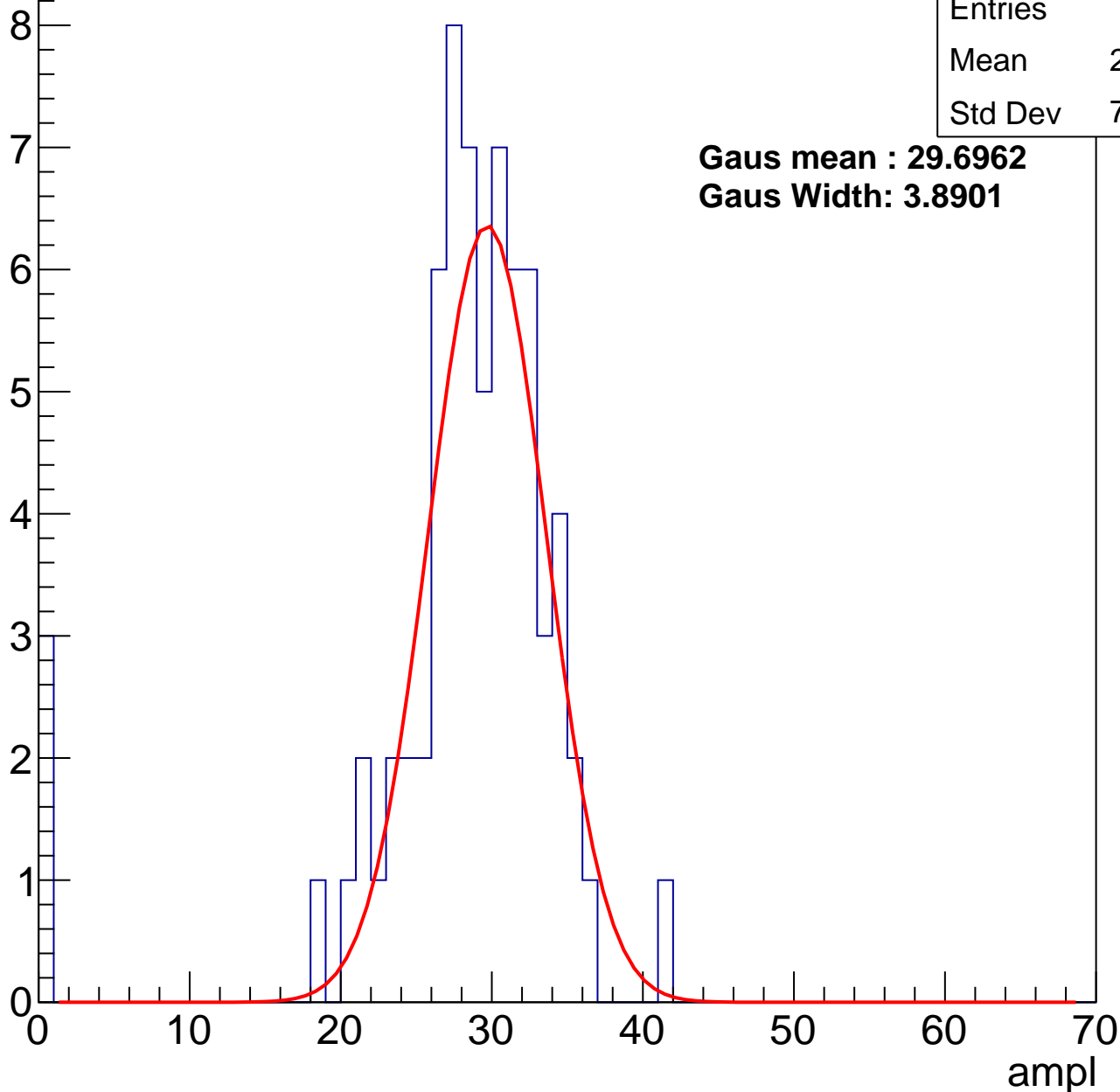
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	27.56
Std Dev	7.072

**Gaus mean : 29.6962**

**Gaus Width: 3.8901**



# B1L103S, U3-ch116, adc1

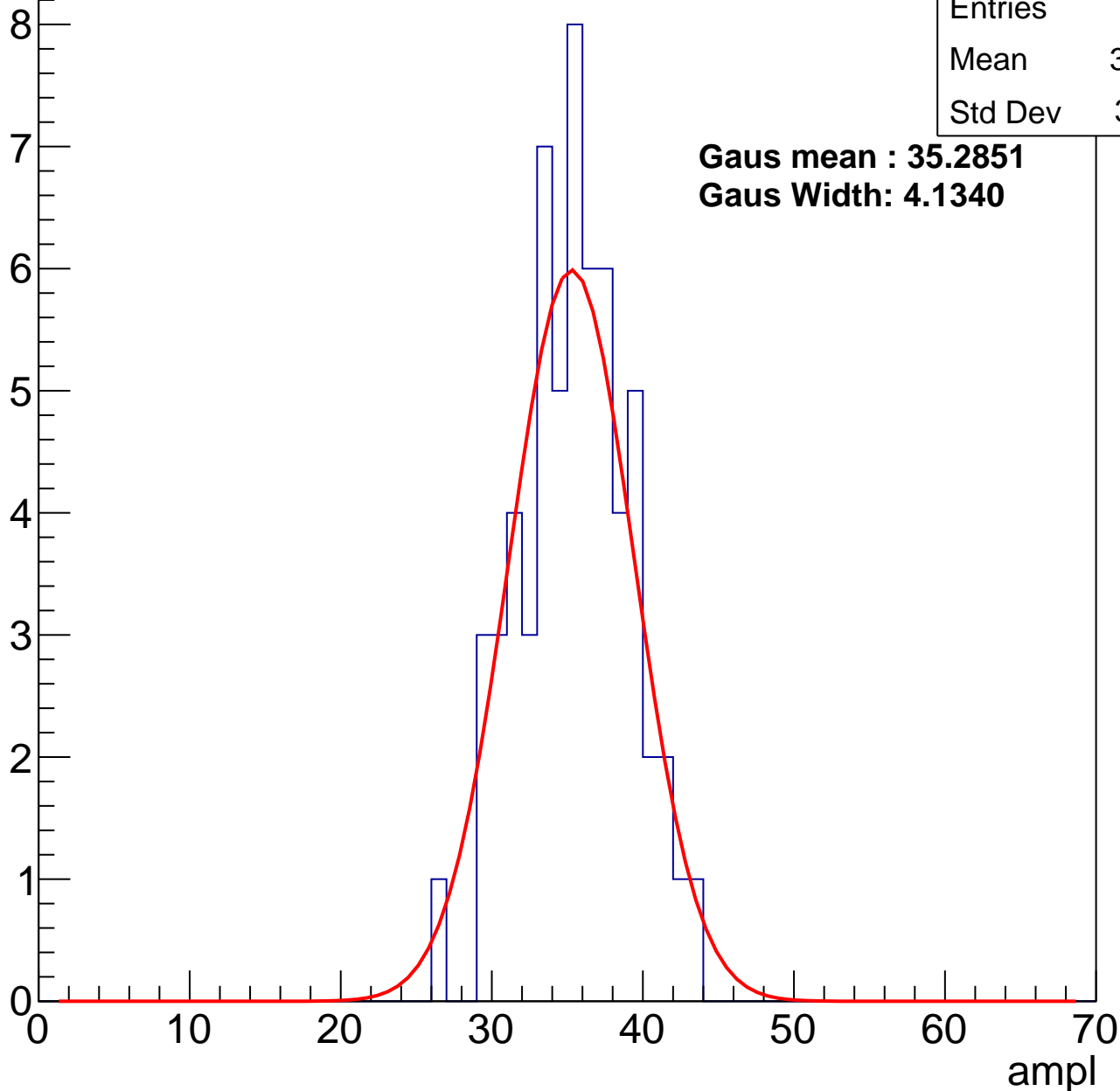
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	35.02
Std Dev	3.551

**Gaus mean : 35.2851**

**Gaus Width: 4.1340**



# B1L103S, U3-ch116, adc2

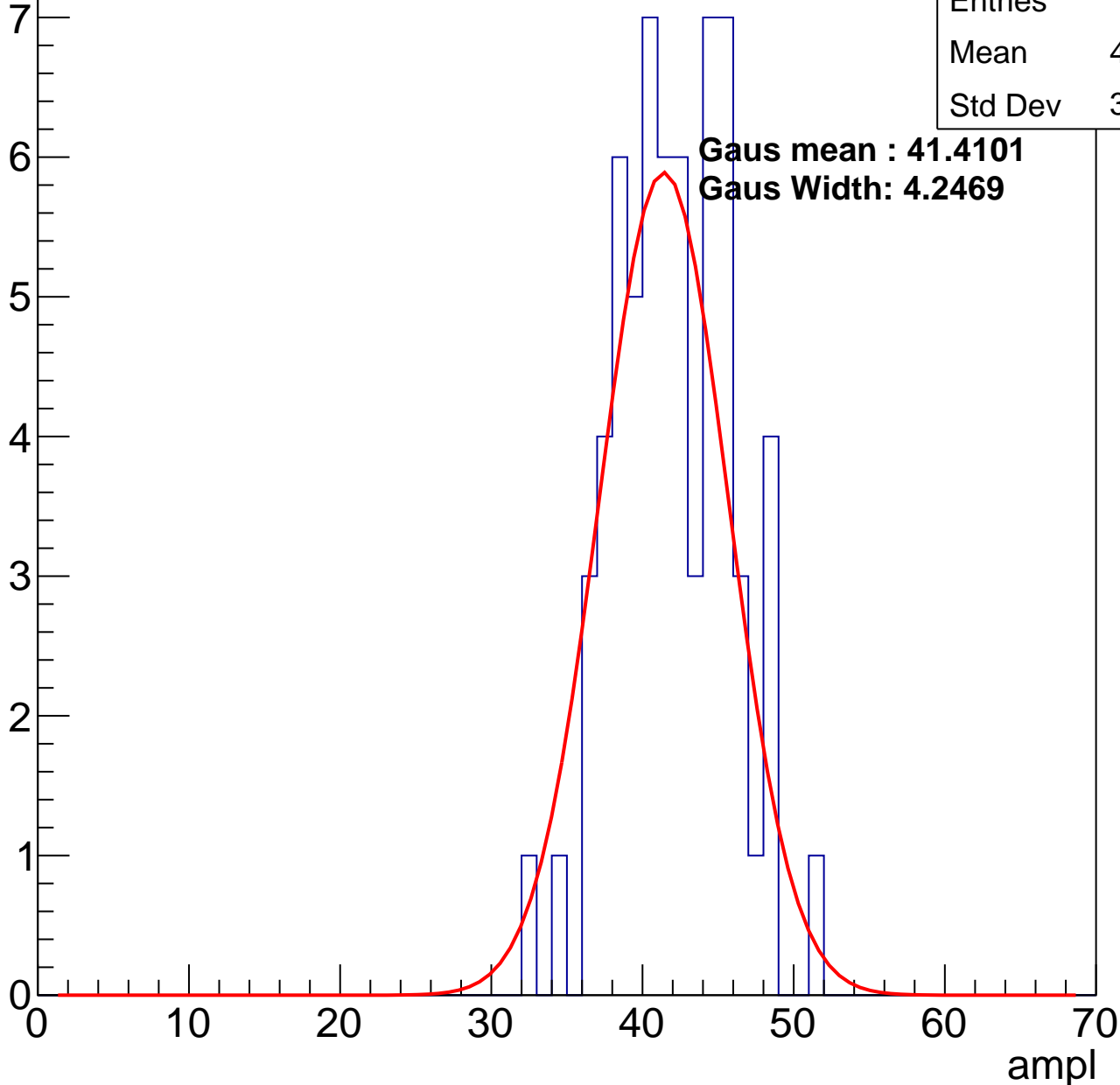
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	41.58
Std Dev	3.778

**Gaus mean : 41.4101**

**Gaus Width: 4.2469**

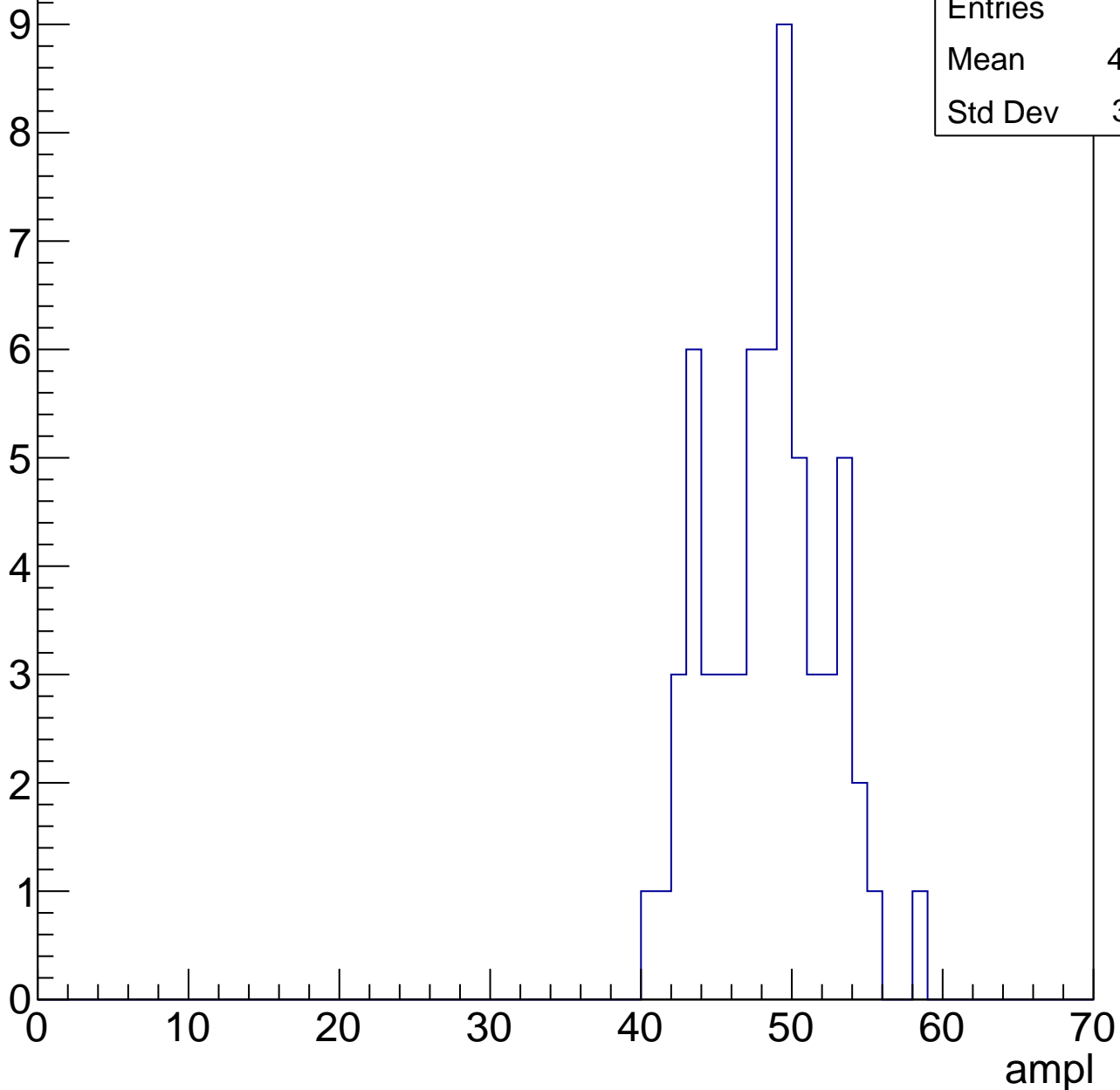


# B1L103S, U3-ch116, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	47.97
Std Dev	3.871

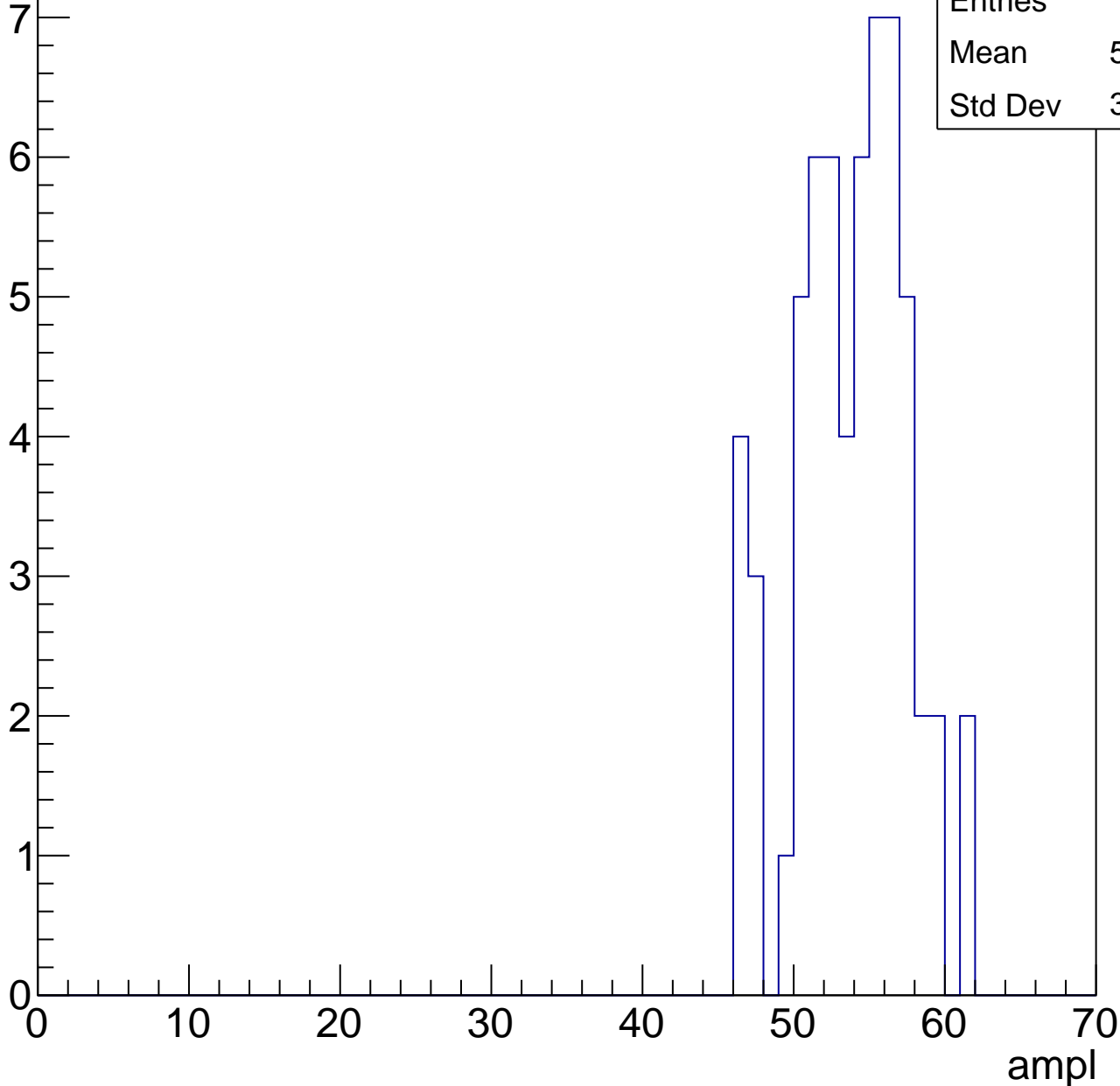


# B1L103S, U3-ch116, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	53.27
Std Dev	3.692

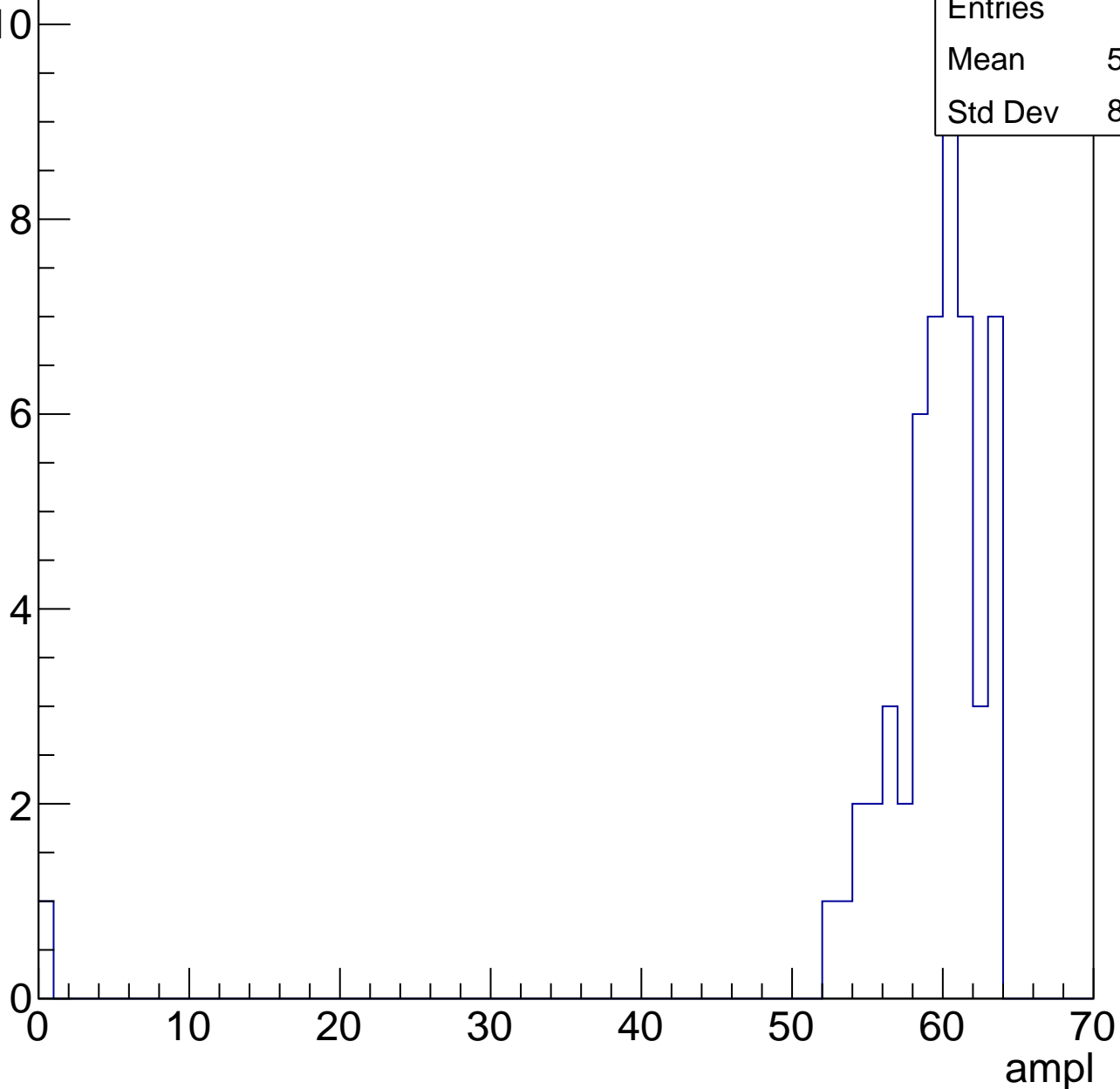


# B1L103S, U3-ch116, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	58.08
Std Dev	8.573

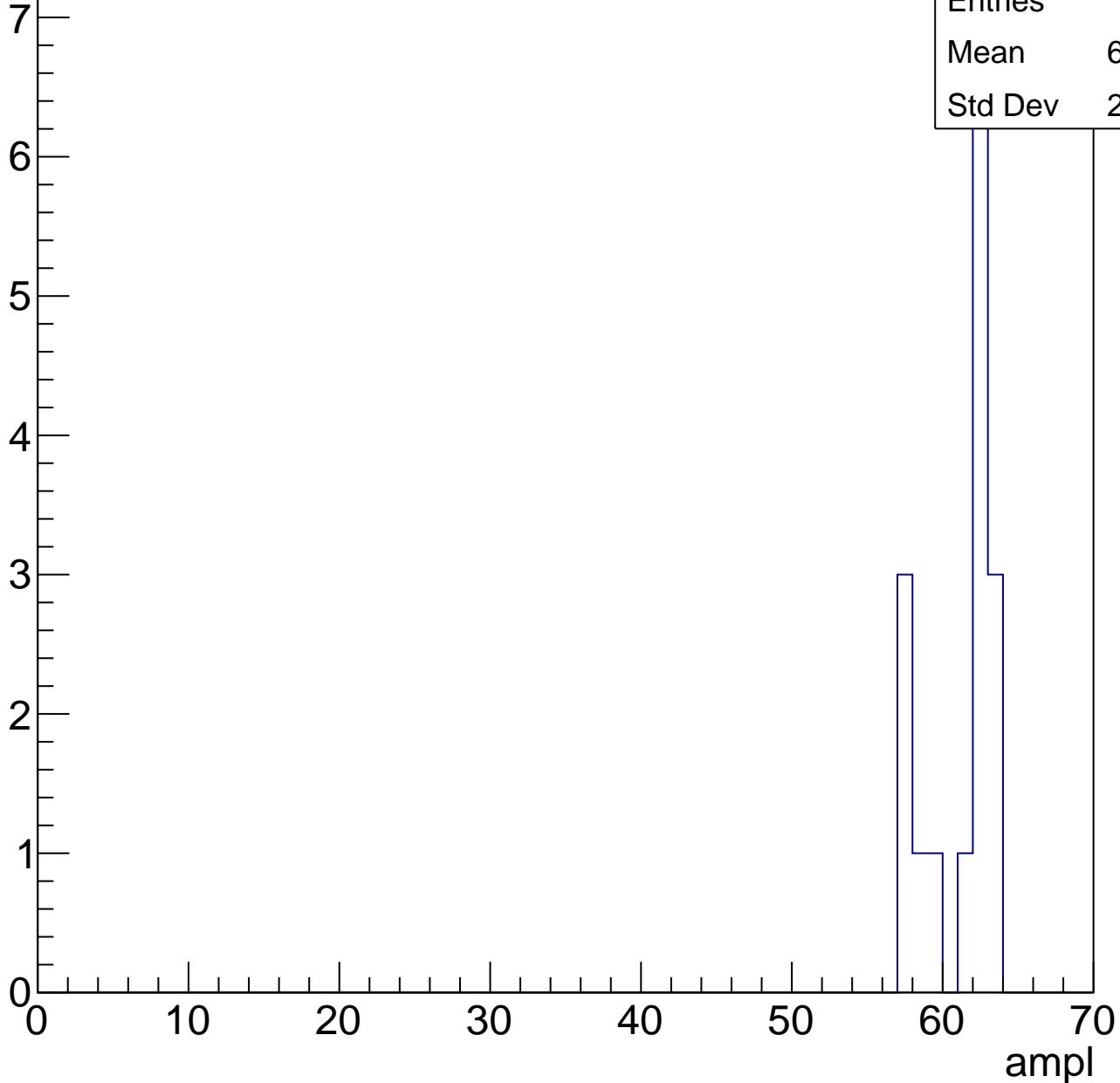


# B1L103S, U3-ch116, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	16
Mean	60.75
Std Dev	2.222





# B1L103S, U3-ch116, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U3-ch117, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	66
Mean	26.88
Std Dev	5.783

**Gaus mean : 27.9617**

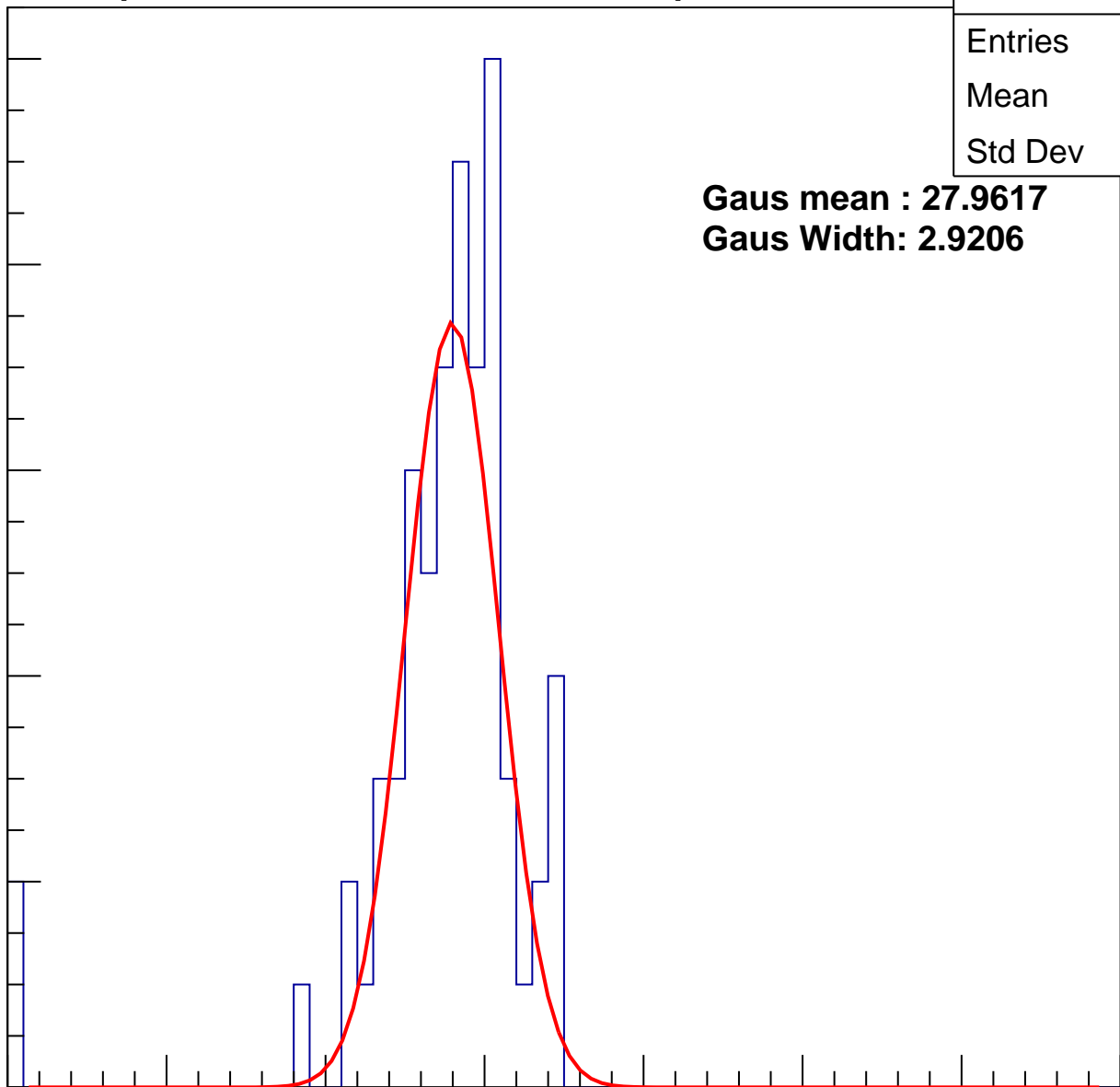
**Gaus Width: 2.9206**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

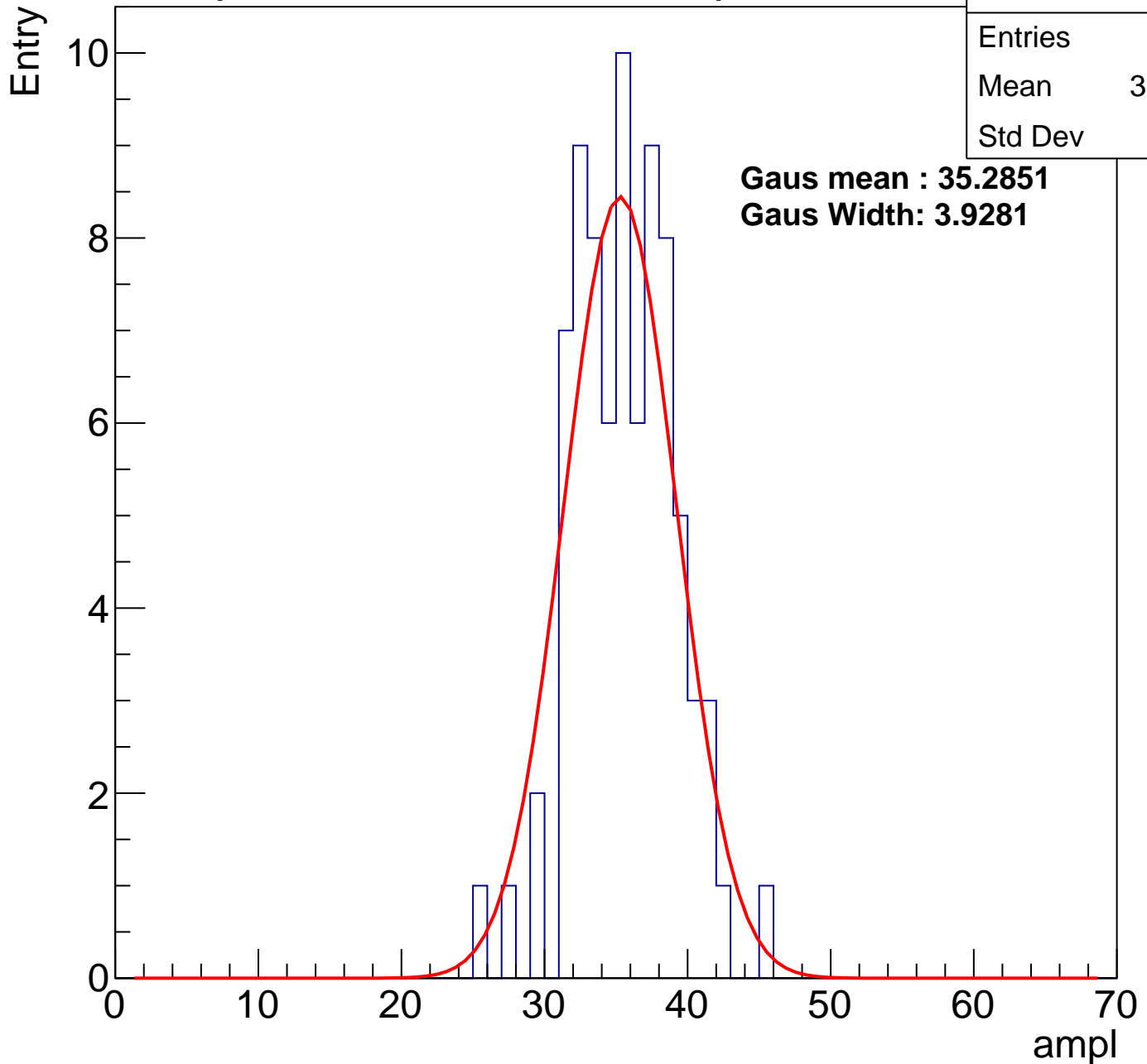


# B1L103S, U3-ch117, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	80
Mean	35.14
Std Dev	3.52

**Gaus mean : 35.2851**  
**Gaus Width: 3.9281**



# B1L103S, U3-ch117, adc2

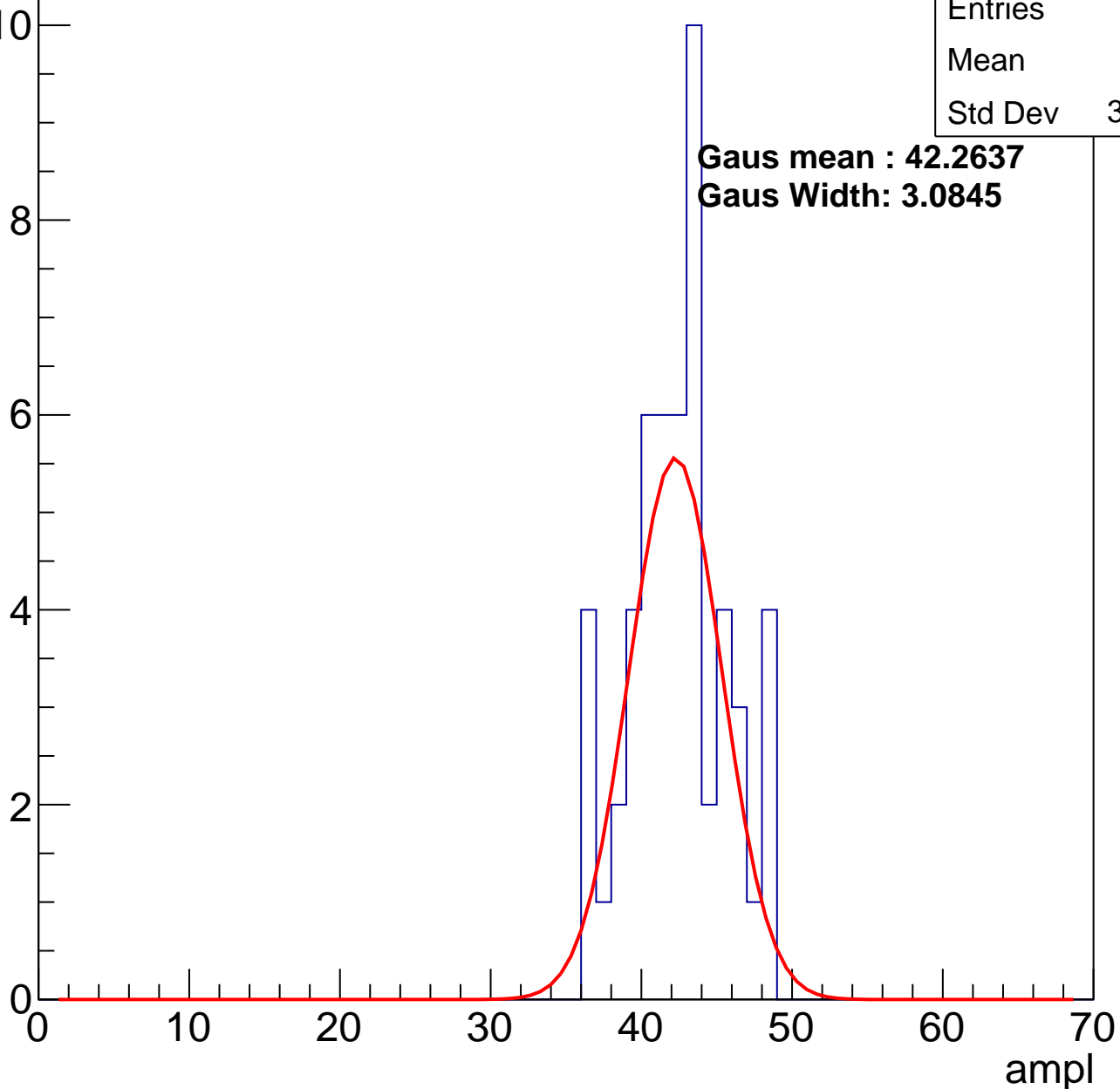
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	42
Std Dev	3.186

**Gaus mean : 42.2637**

**Gaus Width: 3.0845**

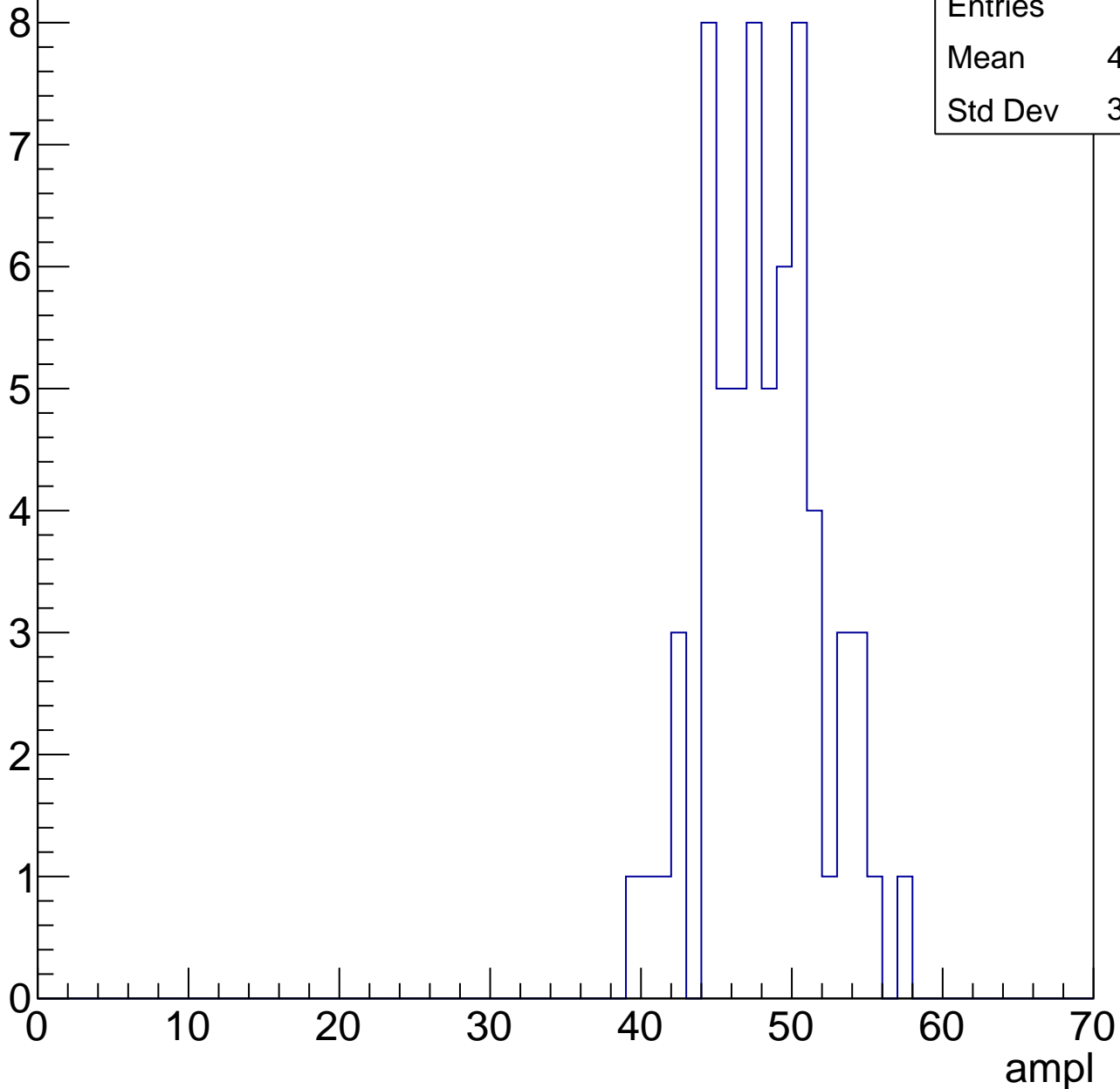


# B1L103S, U3-ch117, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	47.69
Std Dev	3.749

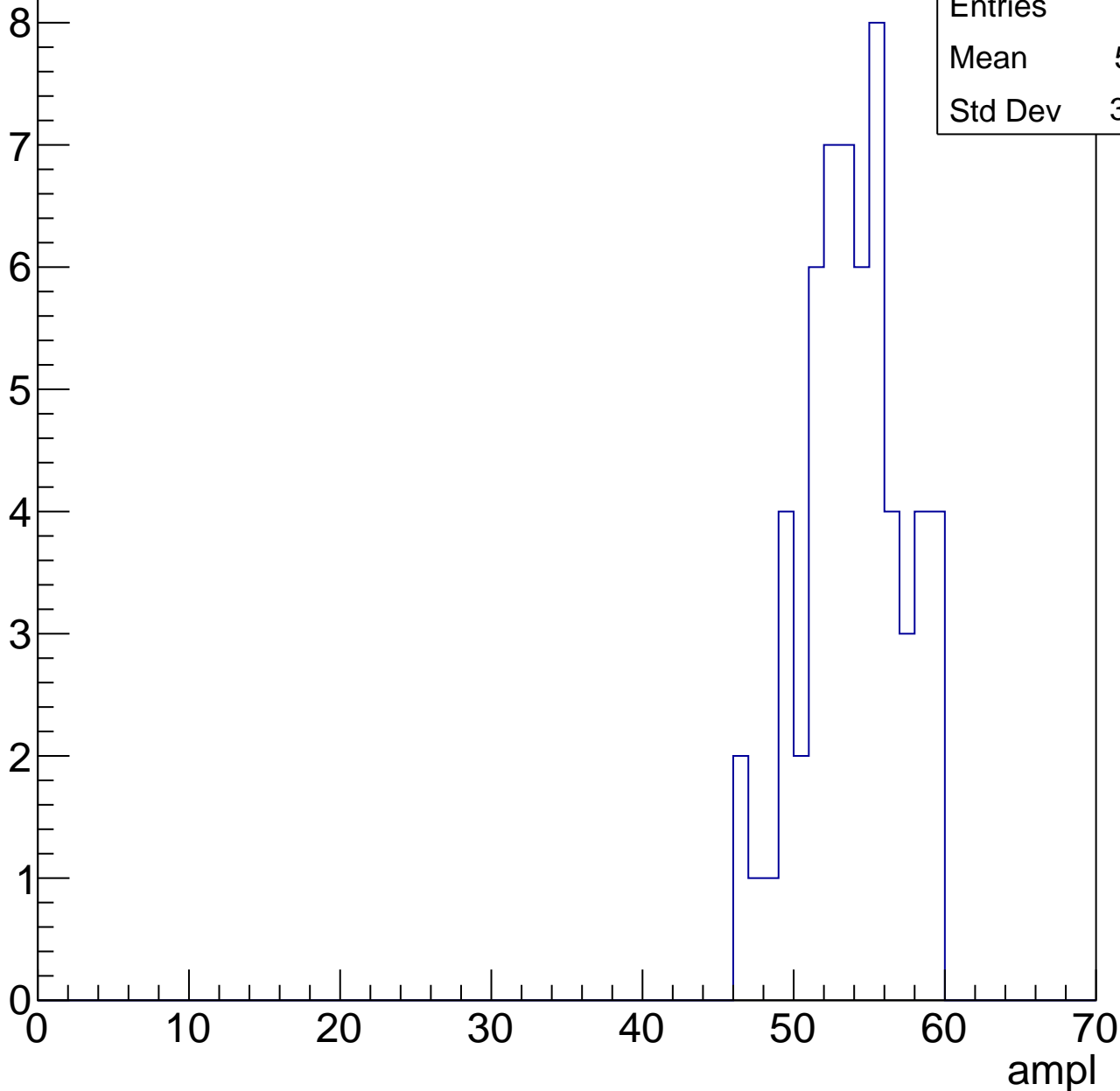


# B1L103S, U3-ch117, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	53.41
Std Dev	3.263



# B1L103S, U3-ch117, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

7

6

5

4

3

2

1

0

Entries

41

Mean

58.71

Std Dev

2.873

0

0

10

20

30

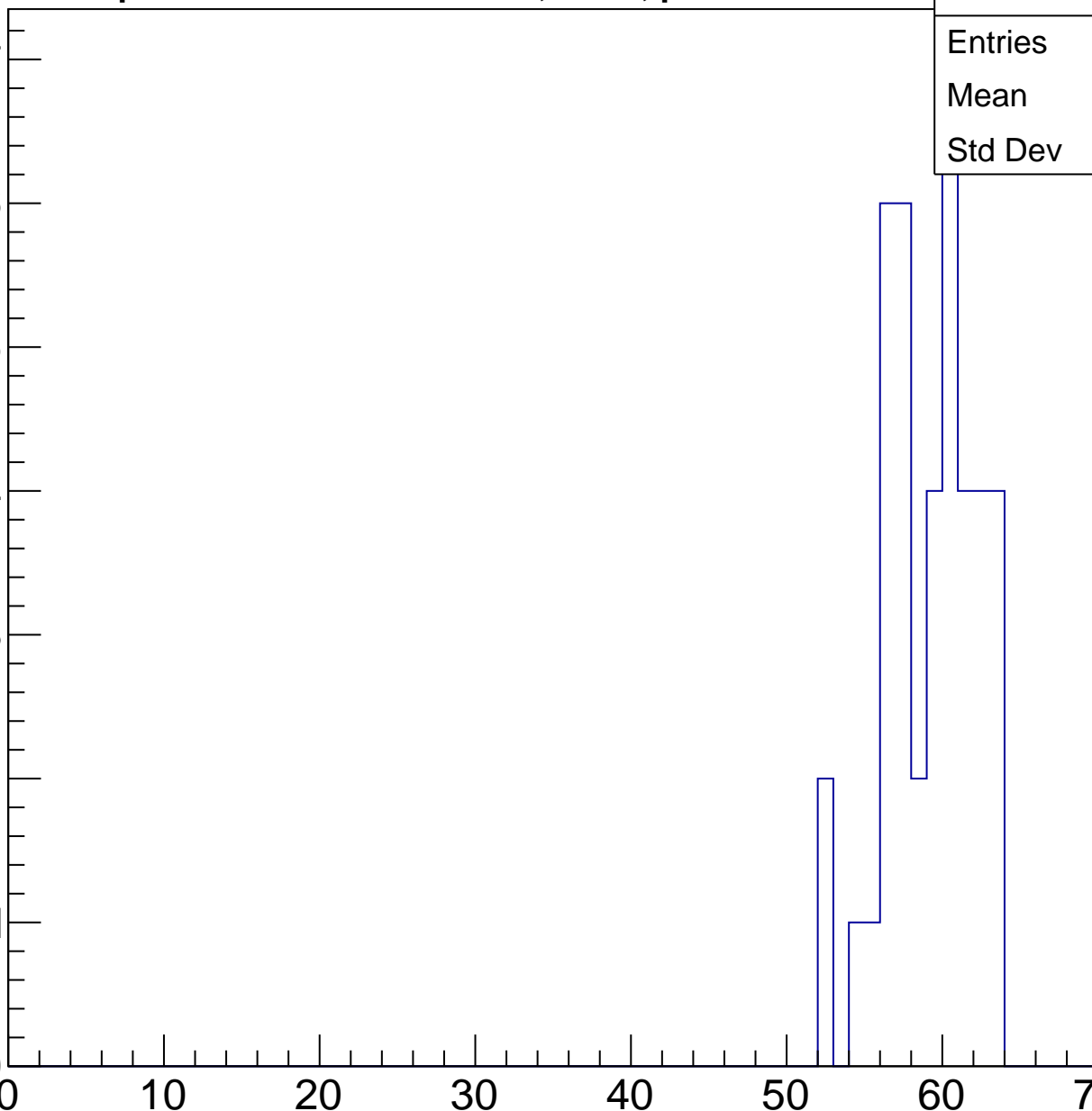
40

50

60

70

ampl

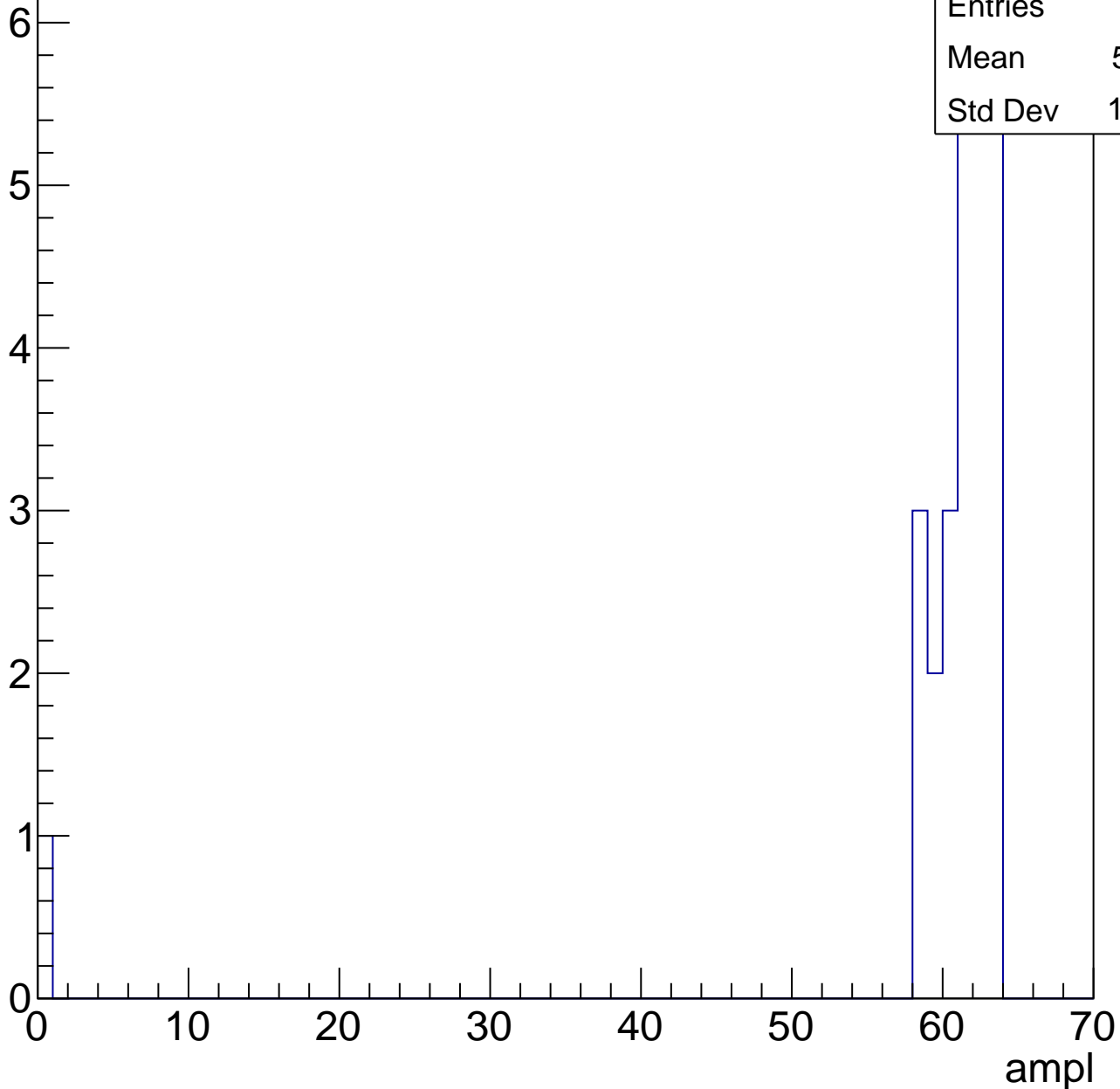


# B1L103S, U3-ch117, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	27
Mean	58.81
Std Dev	11.64





# B1L103S, U3-ch117, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U3-ch118, adc0

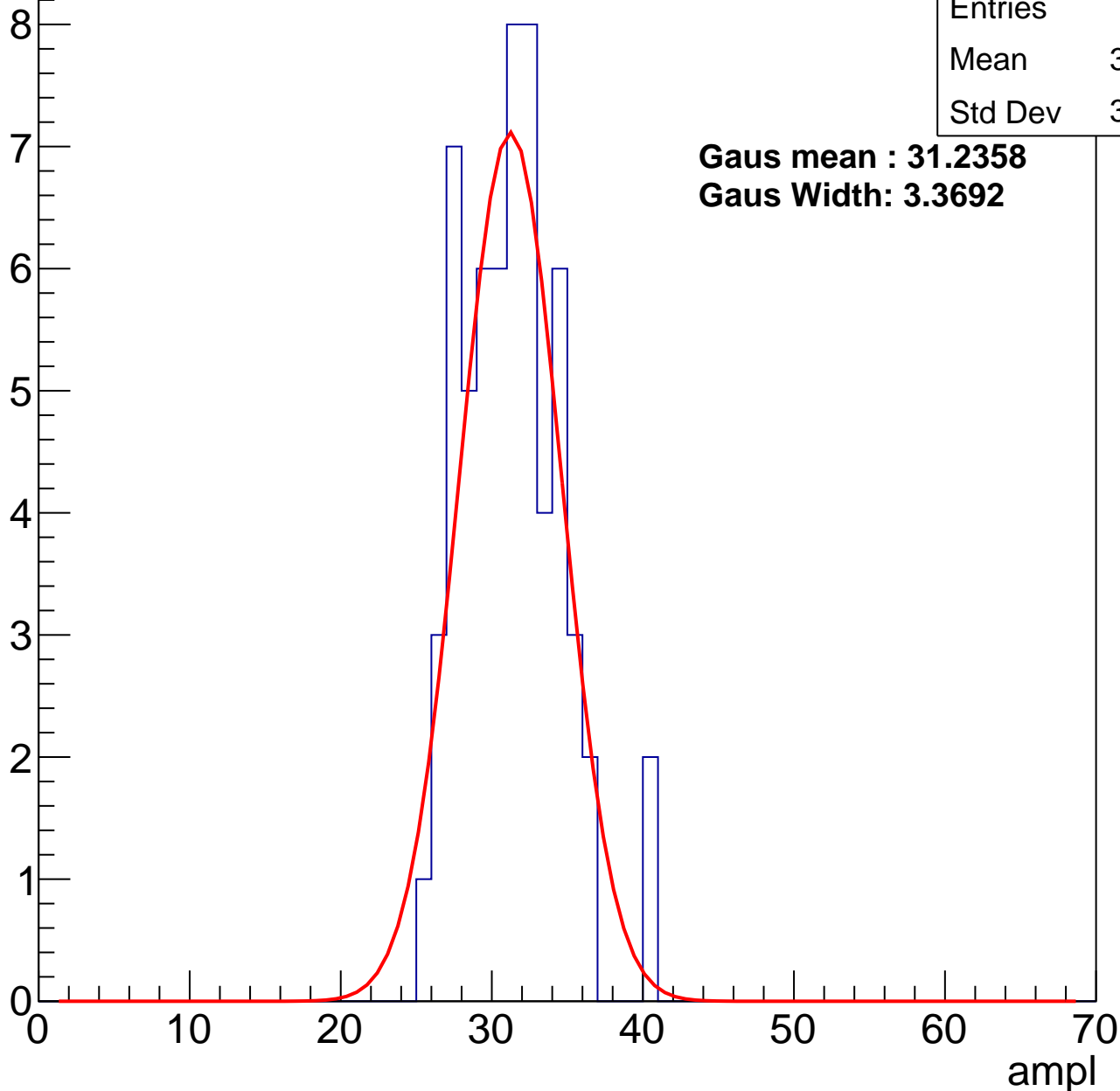
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	30.87
Std Dev	3.226

**Gaus mean : 31.2358**

**Gaus Width: 3.3692**



# B1L103S, U3-ch118, adc1

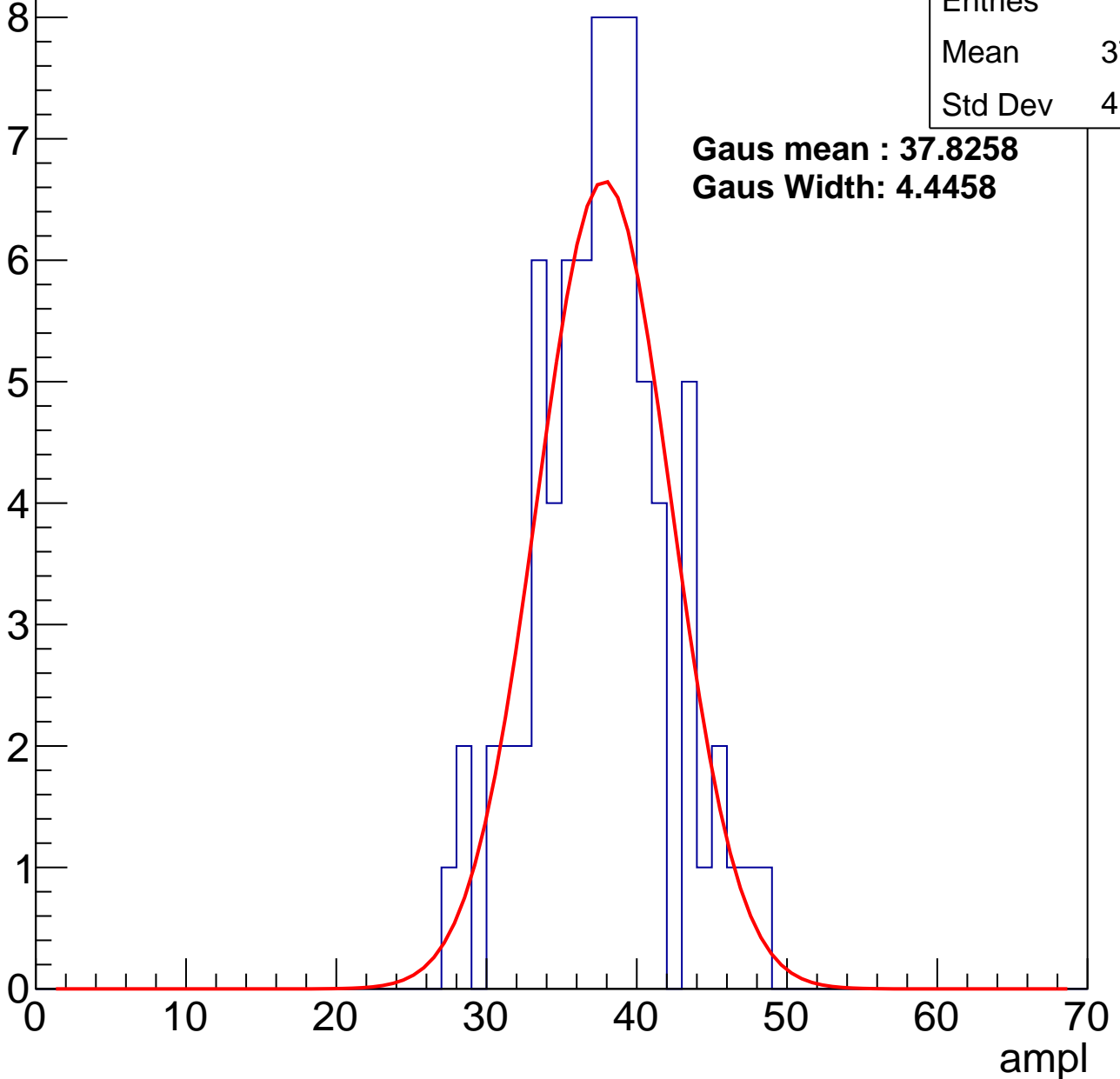
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	37.27
Std Dev	4.392

**Gaus mean : 37.8258**

**Gaus Width: 4.4458**



# B1L103S, U3-ch118, adc2

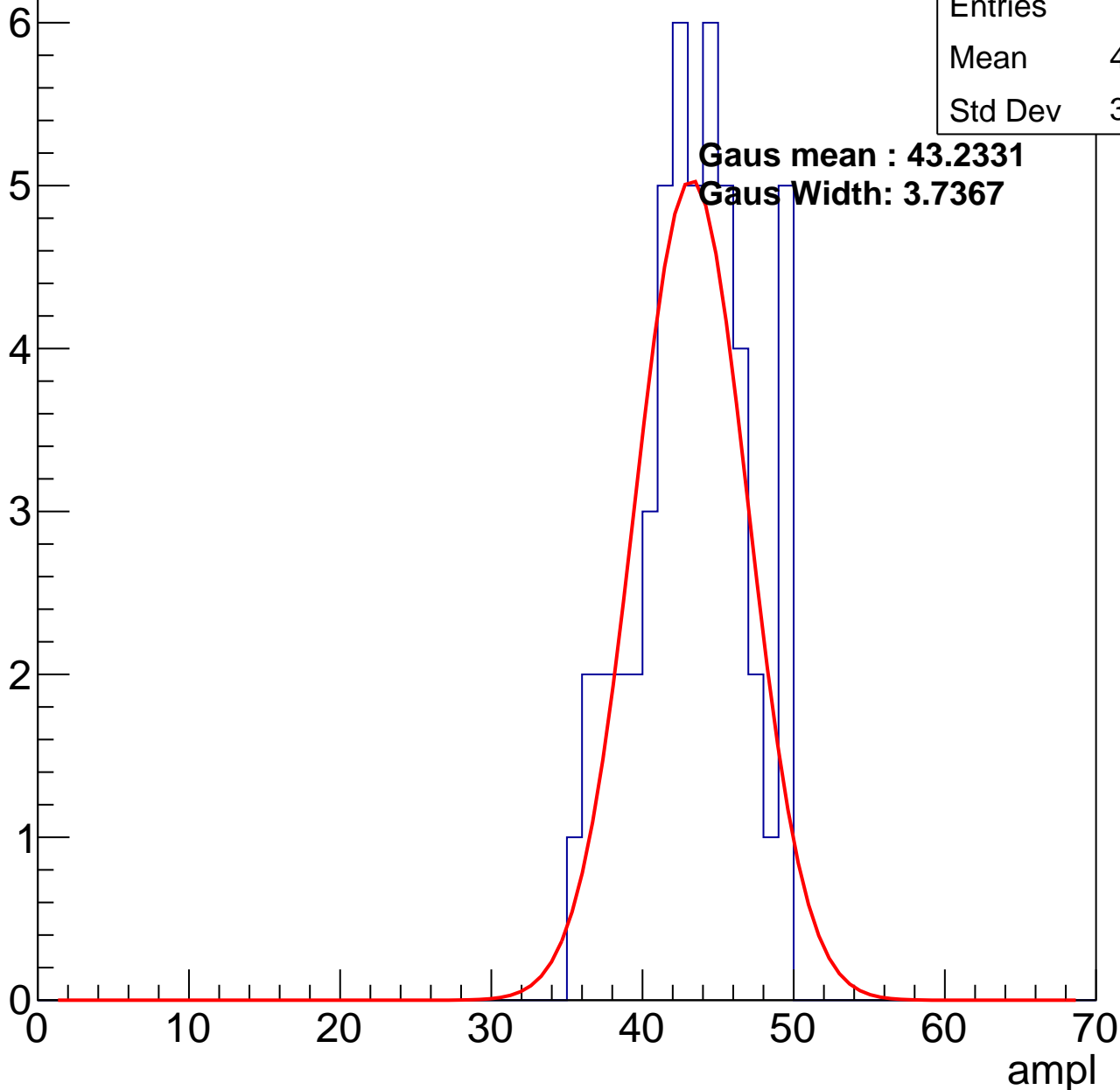
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	42.88
Std Dev	3.617

Gaus mean : 43.2331

Gaus Width: 3.7367

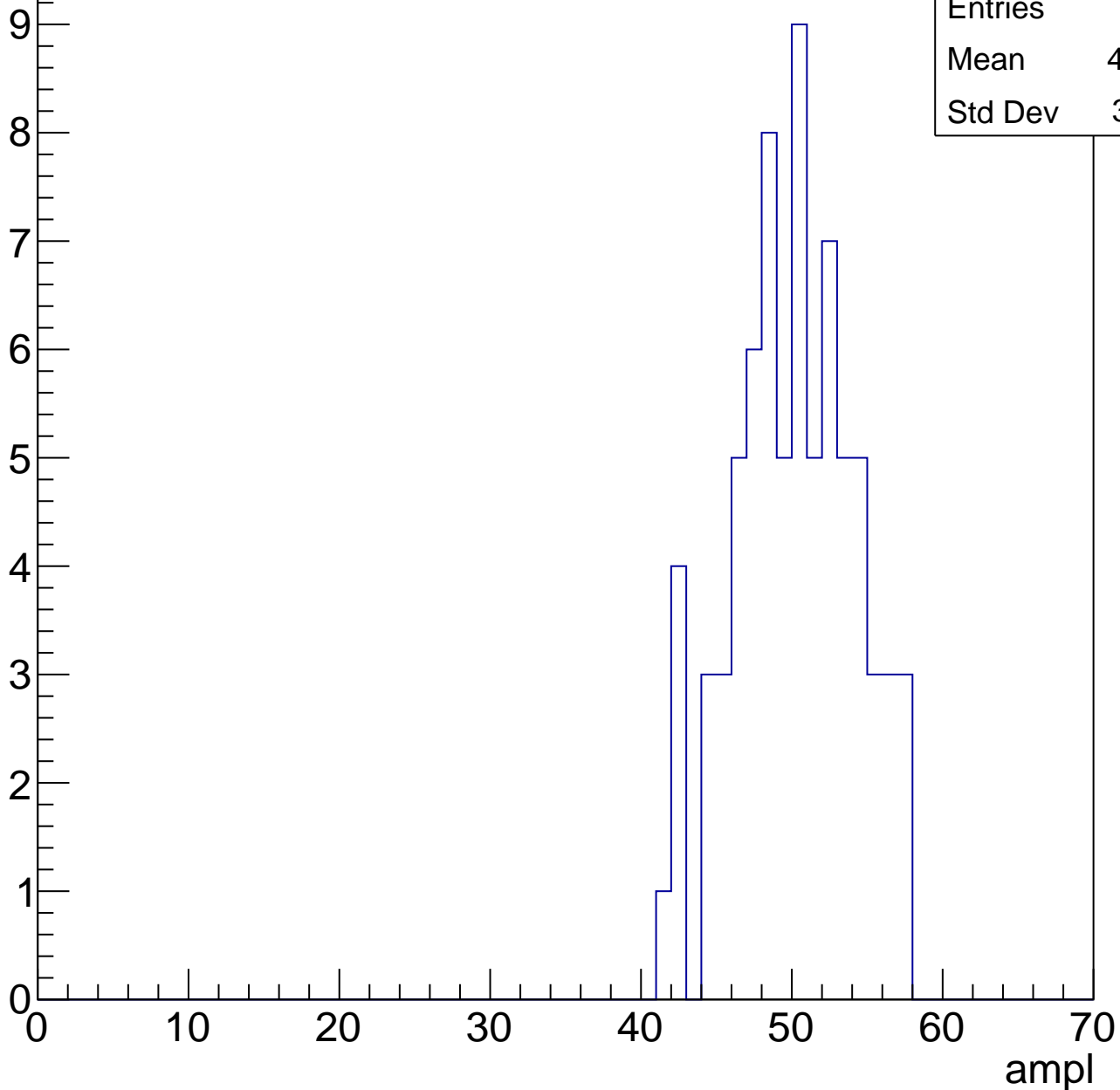


# B1L103S, U3-ch118, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	49.67
Std Dev	3.951

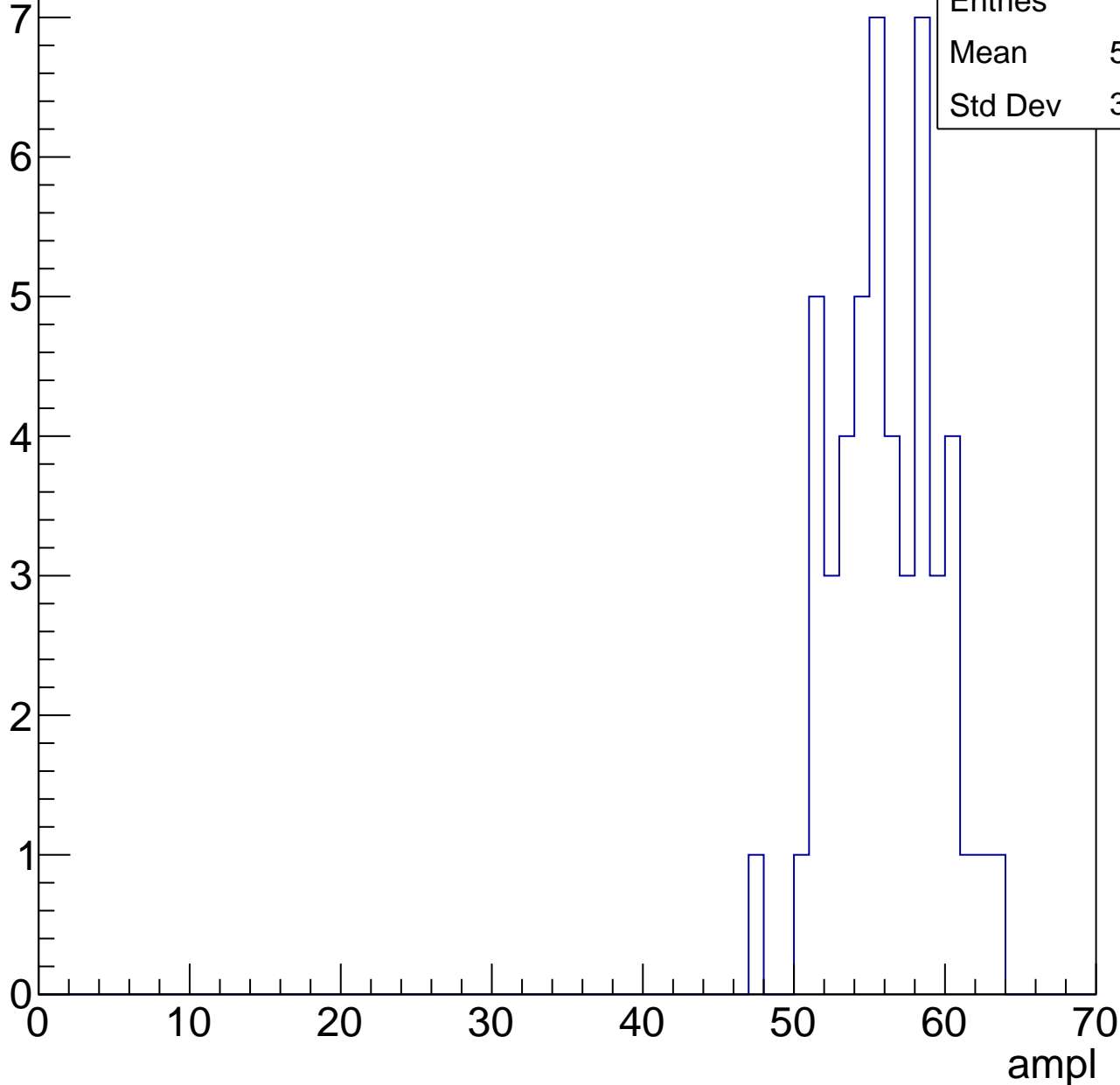


# B1L103S, U3-ch118, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	55.58
Std Dev	3.395

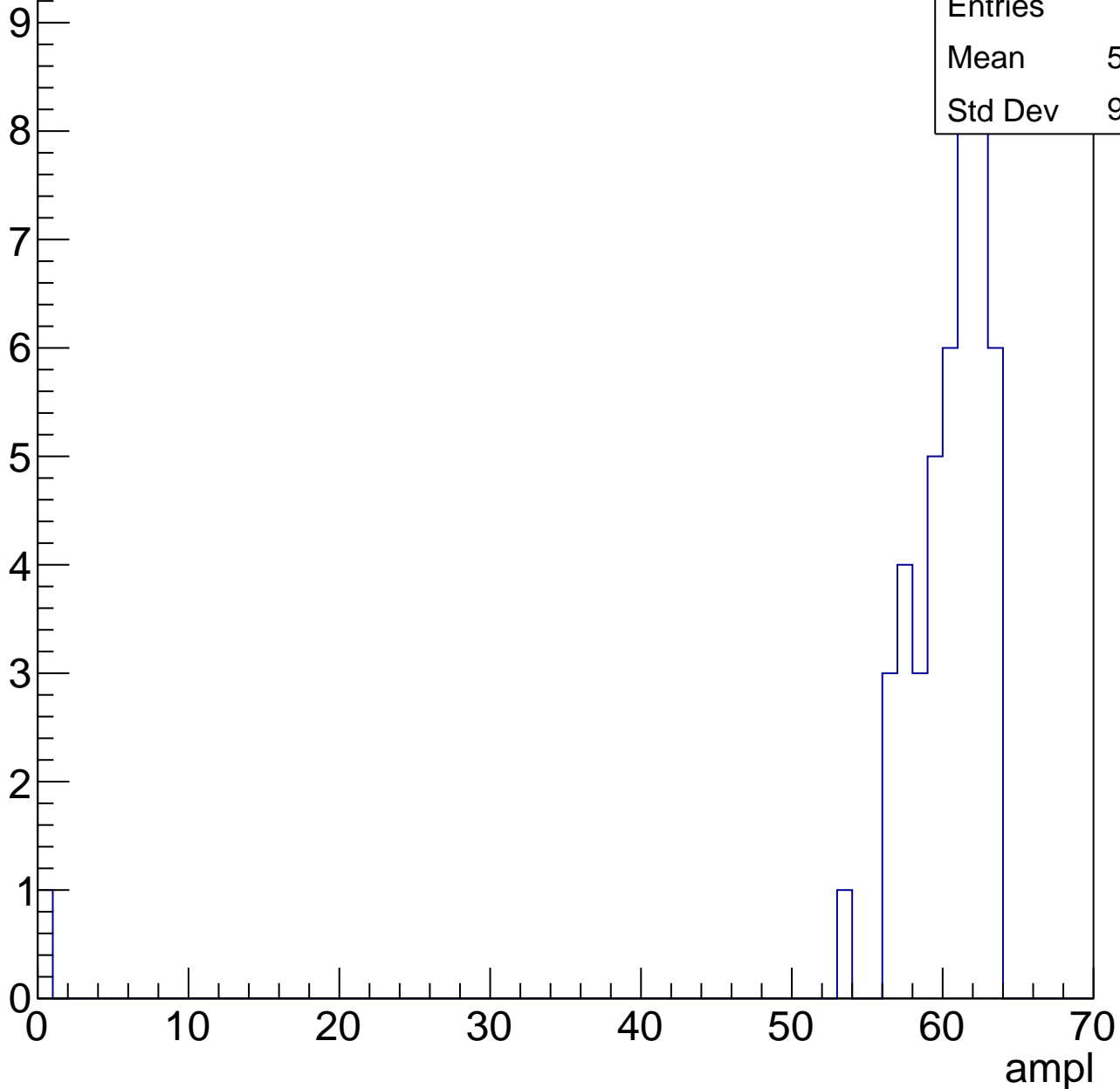


# B1L103S, U3-ch118, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

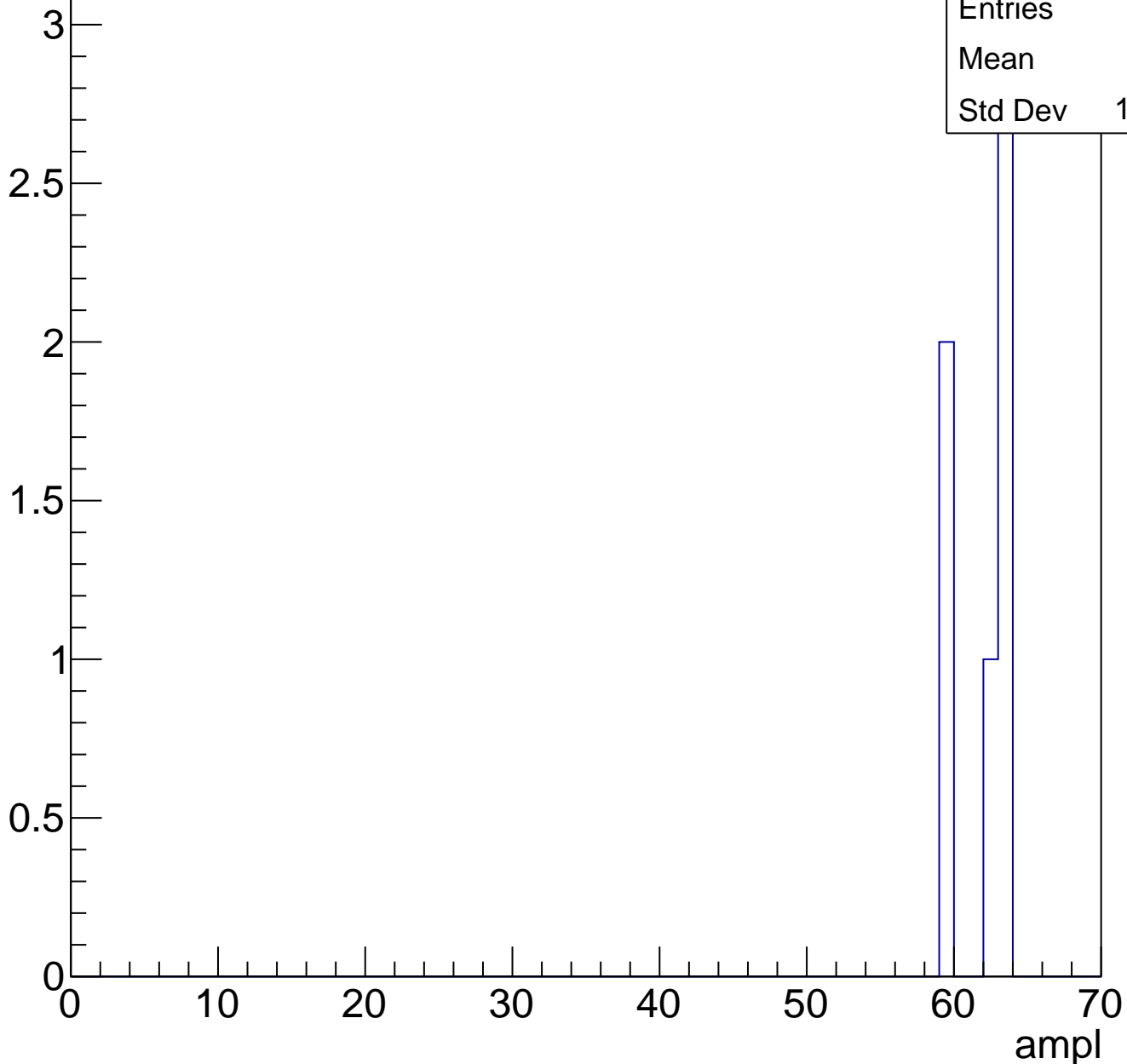
Entries	46
Mean	58.72
Std Dev	9.052



# B1L103S, U3-ch118, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U3-ch118, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	22
Std Dev	0

ampl

# B1L103S, U3-ch119, adc0

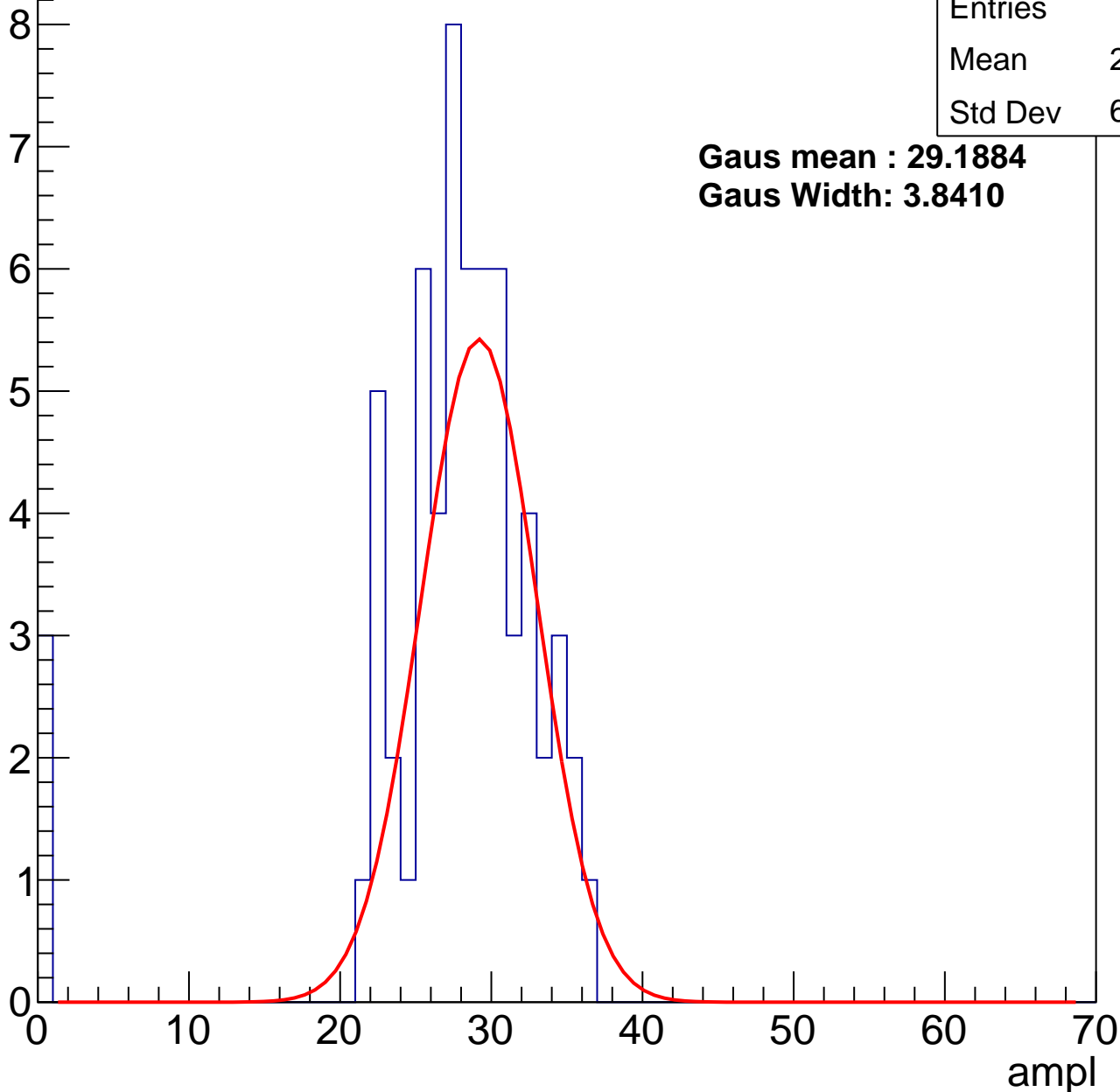
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	26.79
Std Dev	6.986

**Gaus mean : 29.1884**

**Gaus Width: 3.8410**



# B1L103S, U3-ch119, adc1

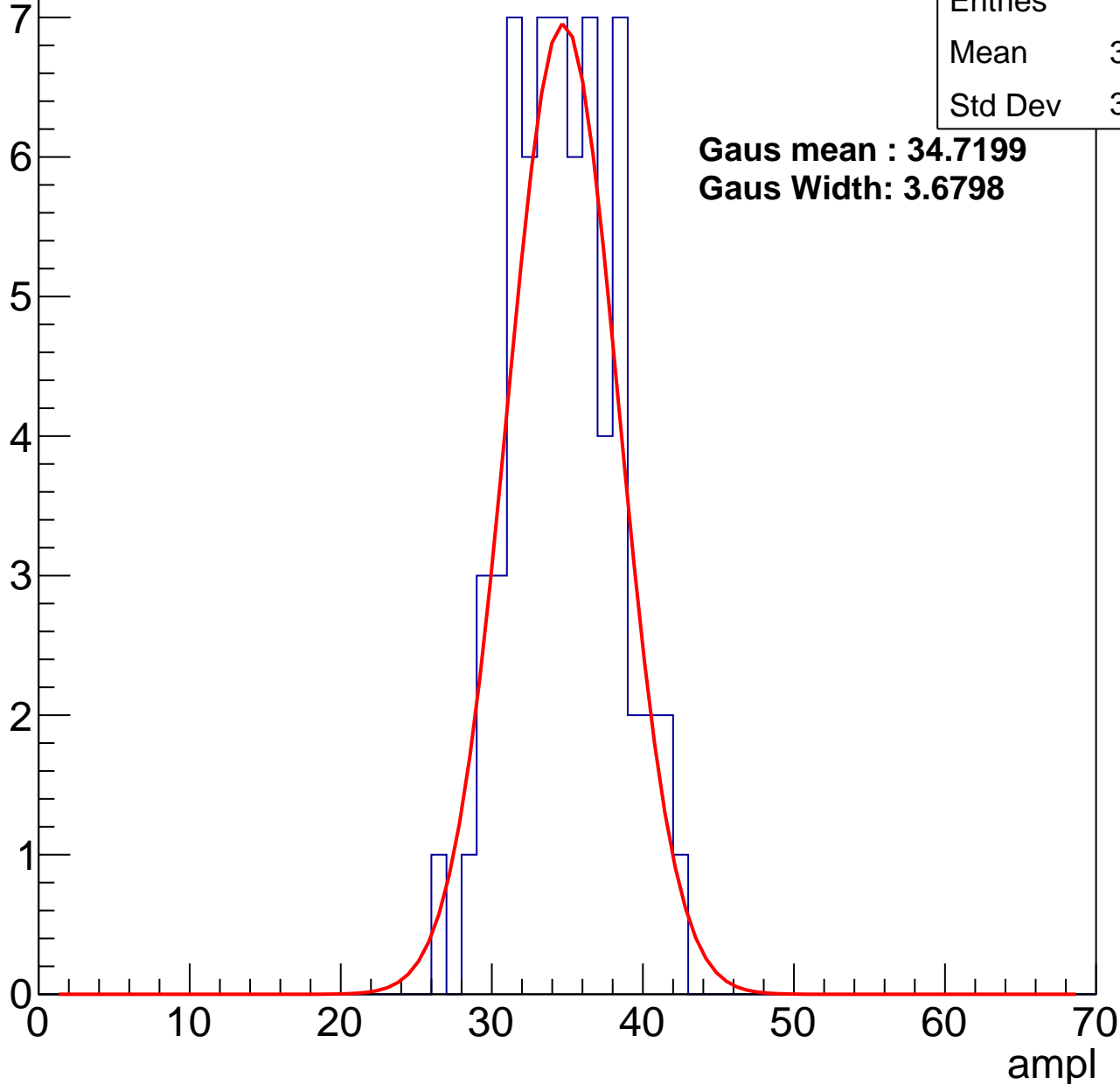
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	34.35
Std Dev	3.427

**Gaus mean : 34.7199**

**Gaus Width: 3.6798**



# B1L103S, U3-ch119, adc2

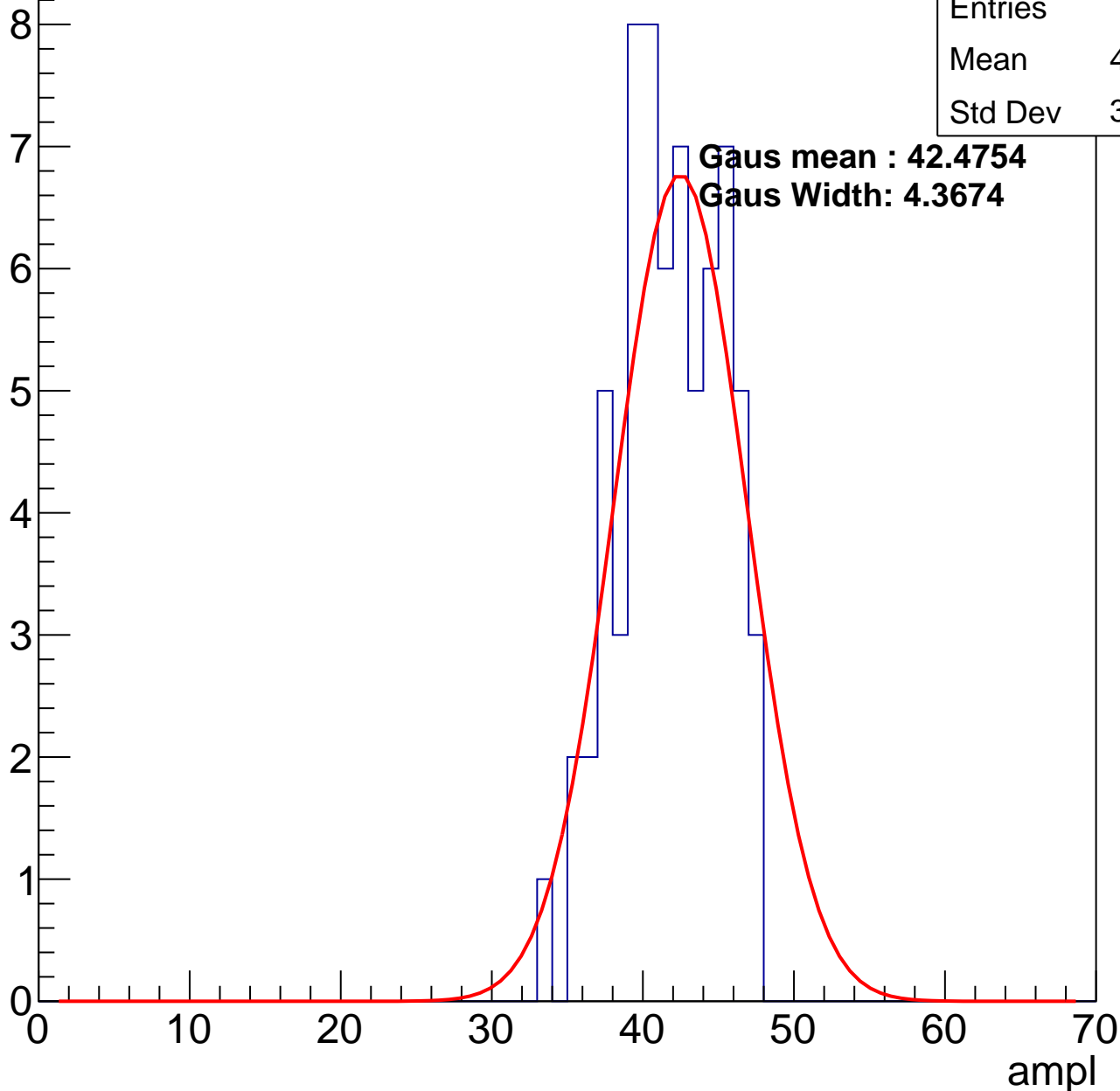
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	41.34
Std Dev	3.324

**Gaus mean : 42.4754**

**Gaus Width: 4.3674**

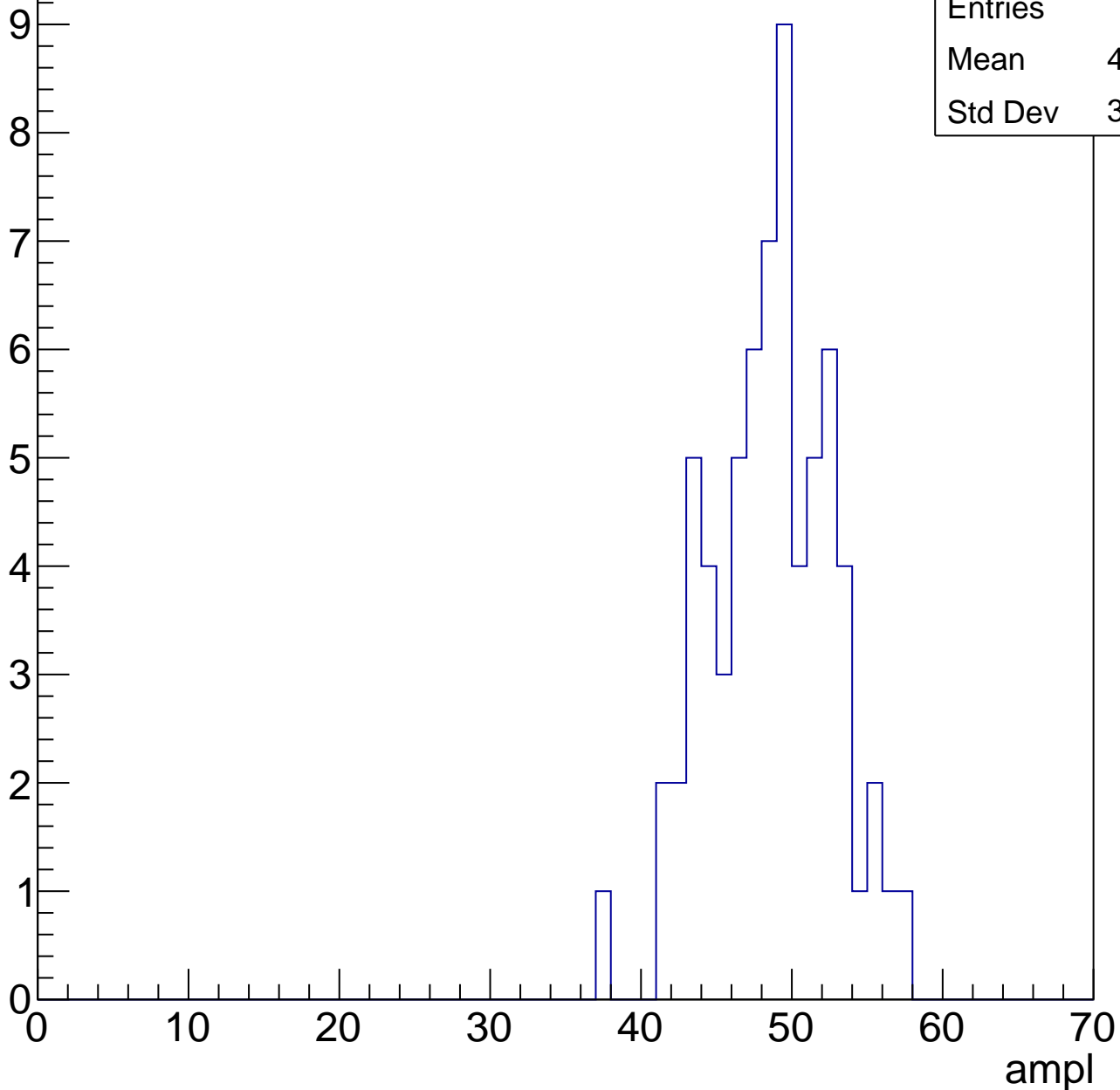


# B1L103S, U3-ch119, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	48.15
Std Dev	3.979

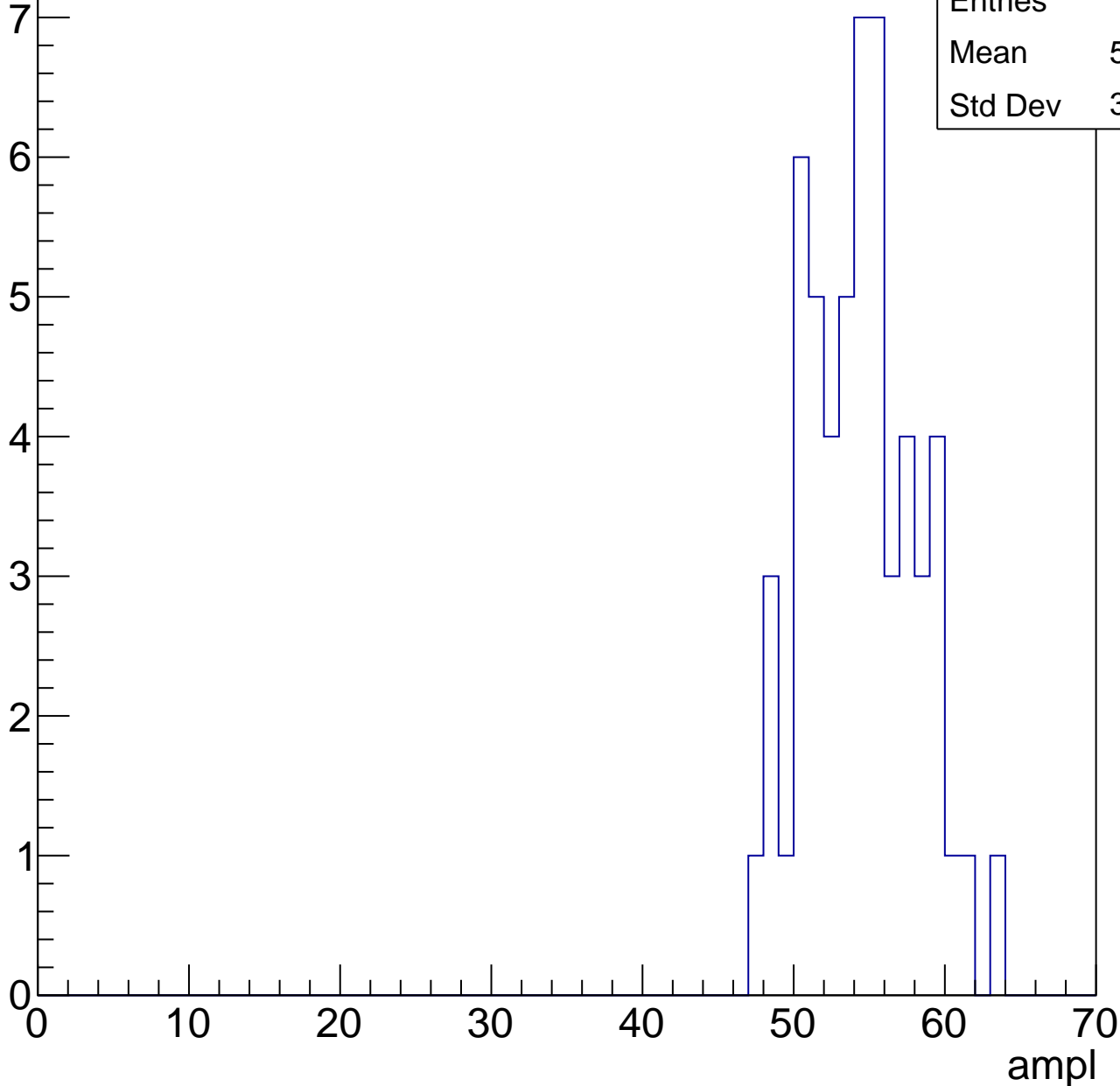


# B1L103S, U3-ch119, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	53.95
Std Dev	3.568

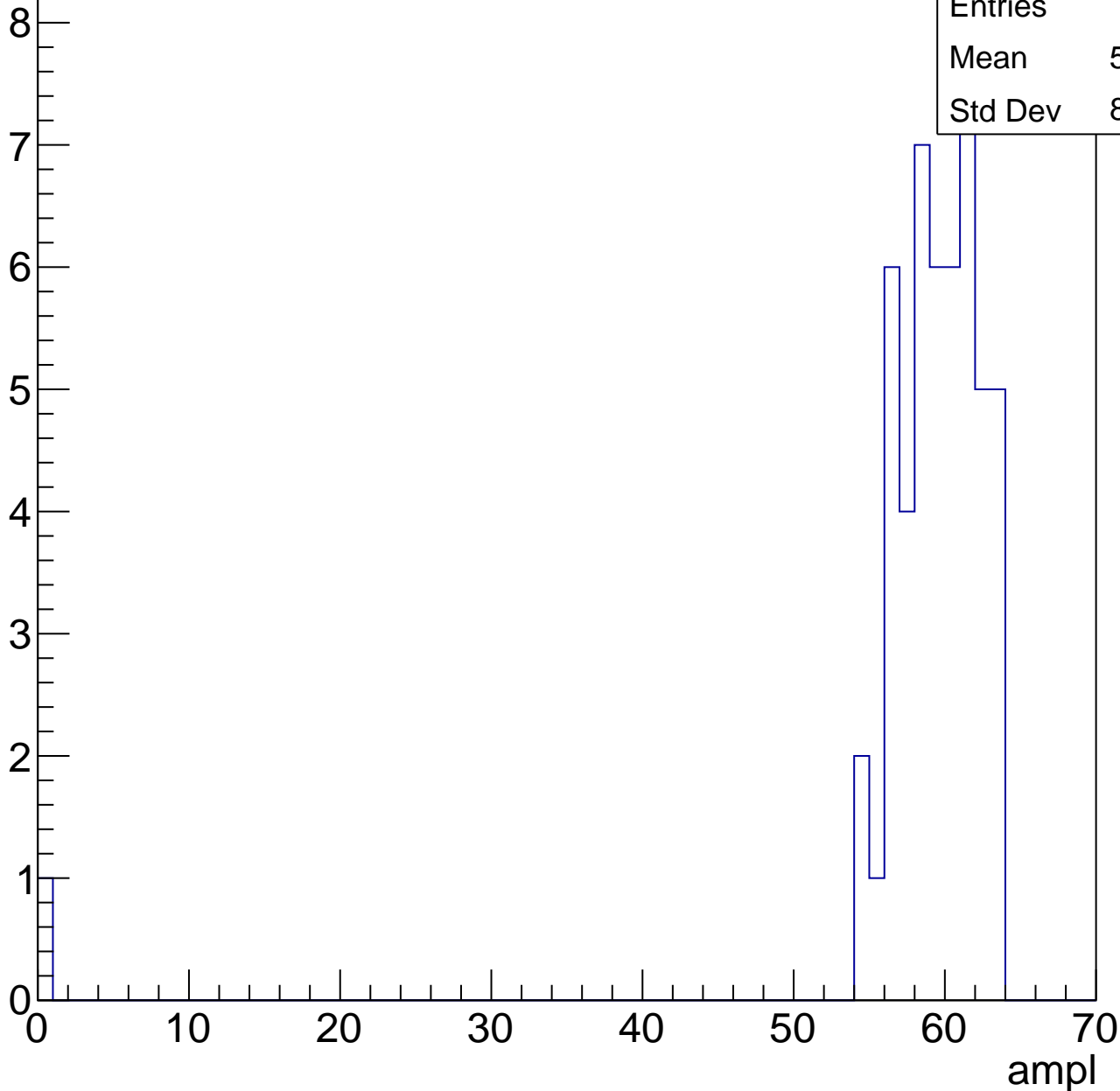


# B1L103S, U3-ch119, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	58.04
Std Dev	8.563

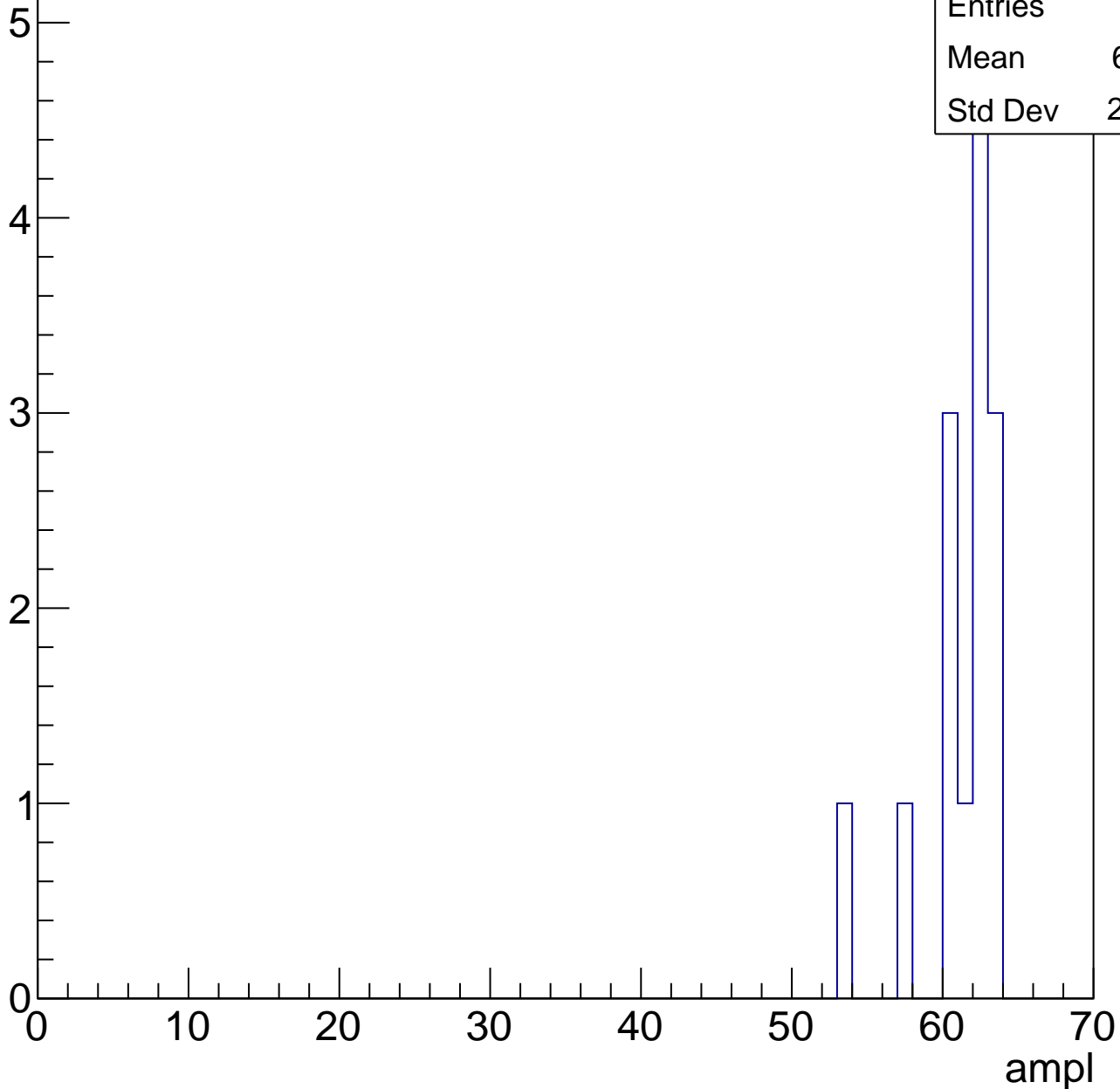


# B1L103S, U3-ch119, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	14
Mean	60.71
Std Dev	2.657





# B1L103S, U3-ch119, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch120, adc0

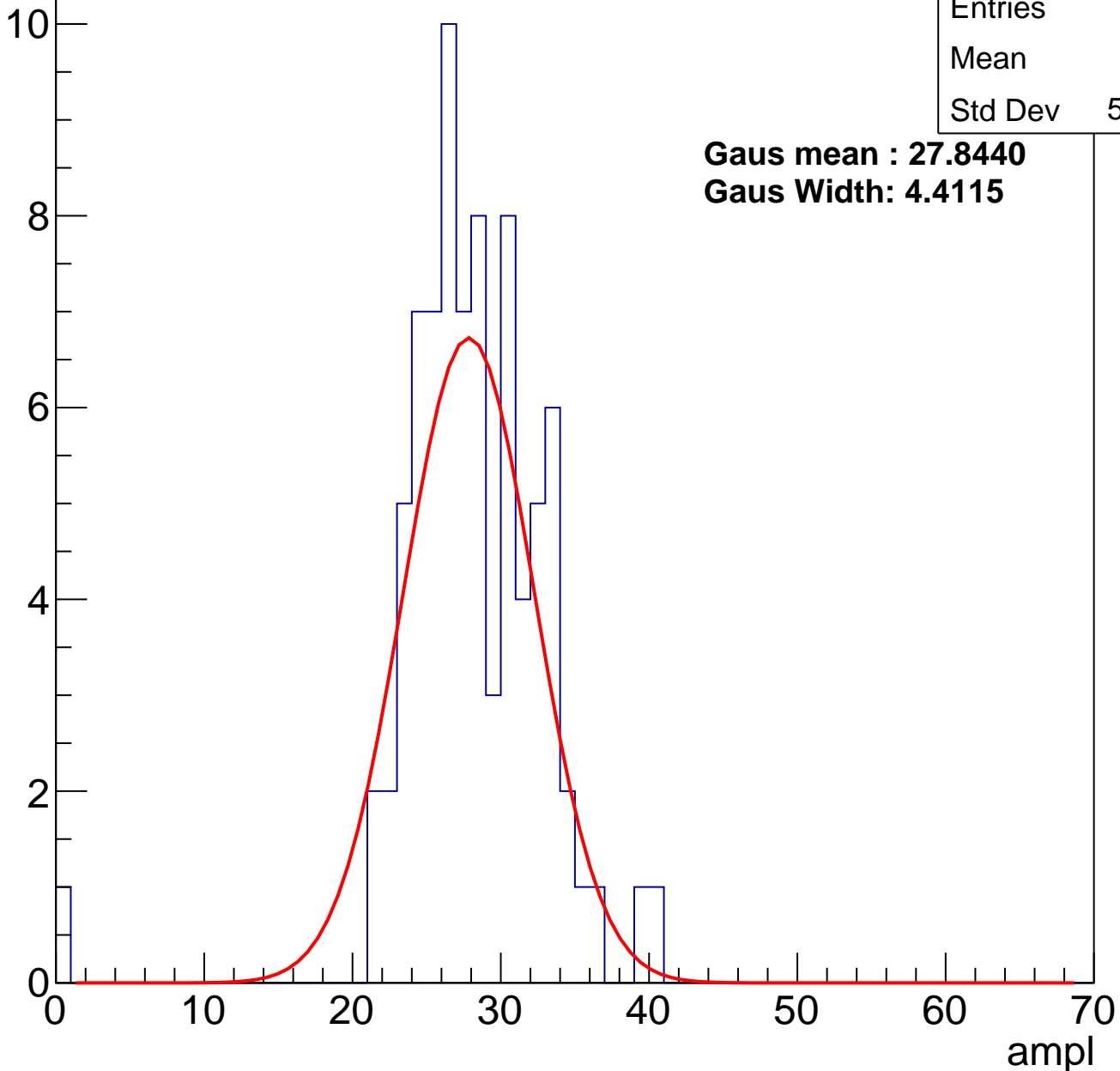
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	81
Mean	27.7
Std Dev	5.024

**Gaus mean : 27.8440**

**Gaus Width: 4.4115**

Entry



# B1L103S, U3-ch120, adc1

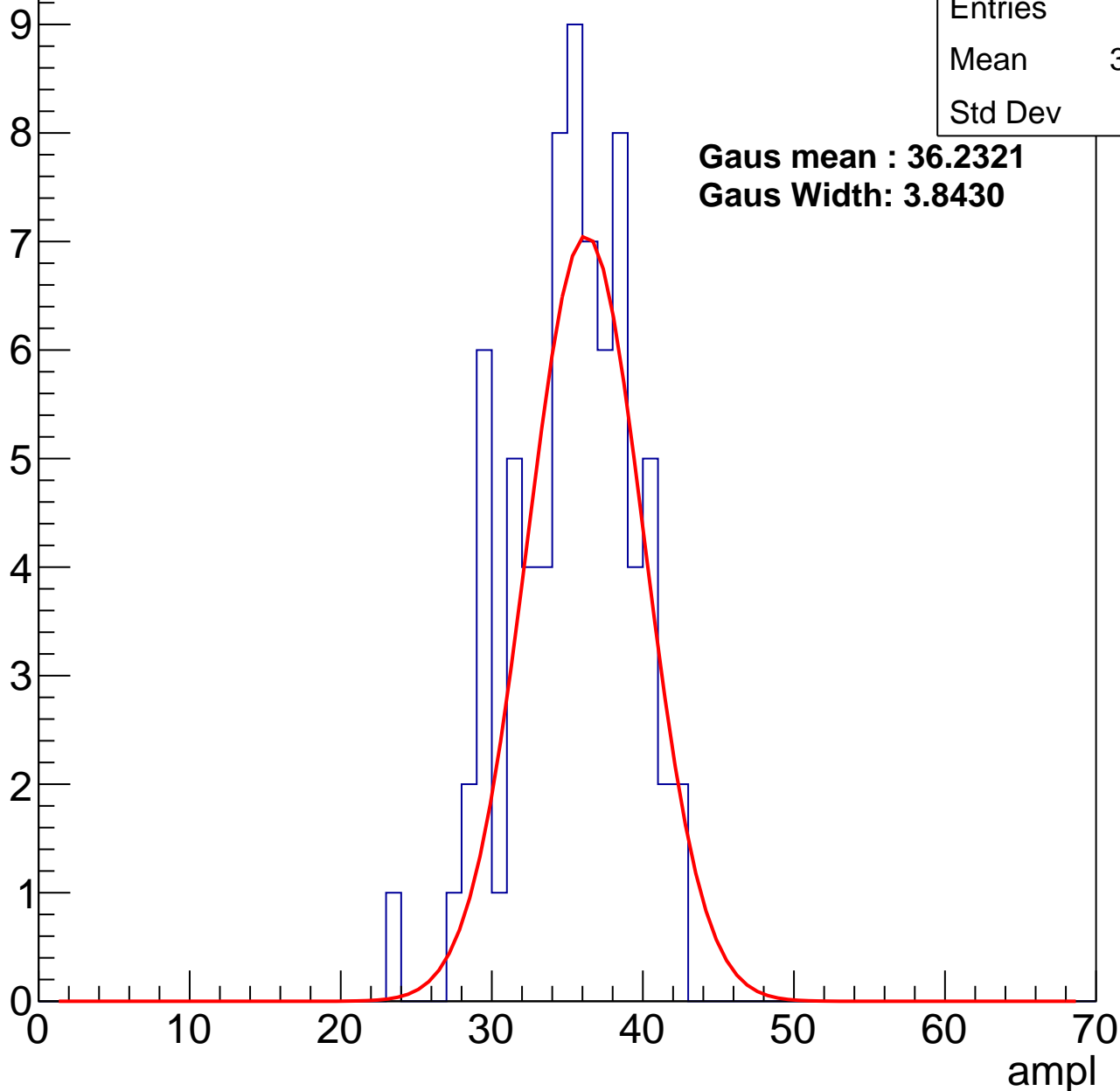
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	34.83
Std Dev	3.91

**Gaus mean : 36.2321**

**Gaus Width: 3.8430**



# B1L103S, U3-ch120, adc2

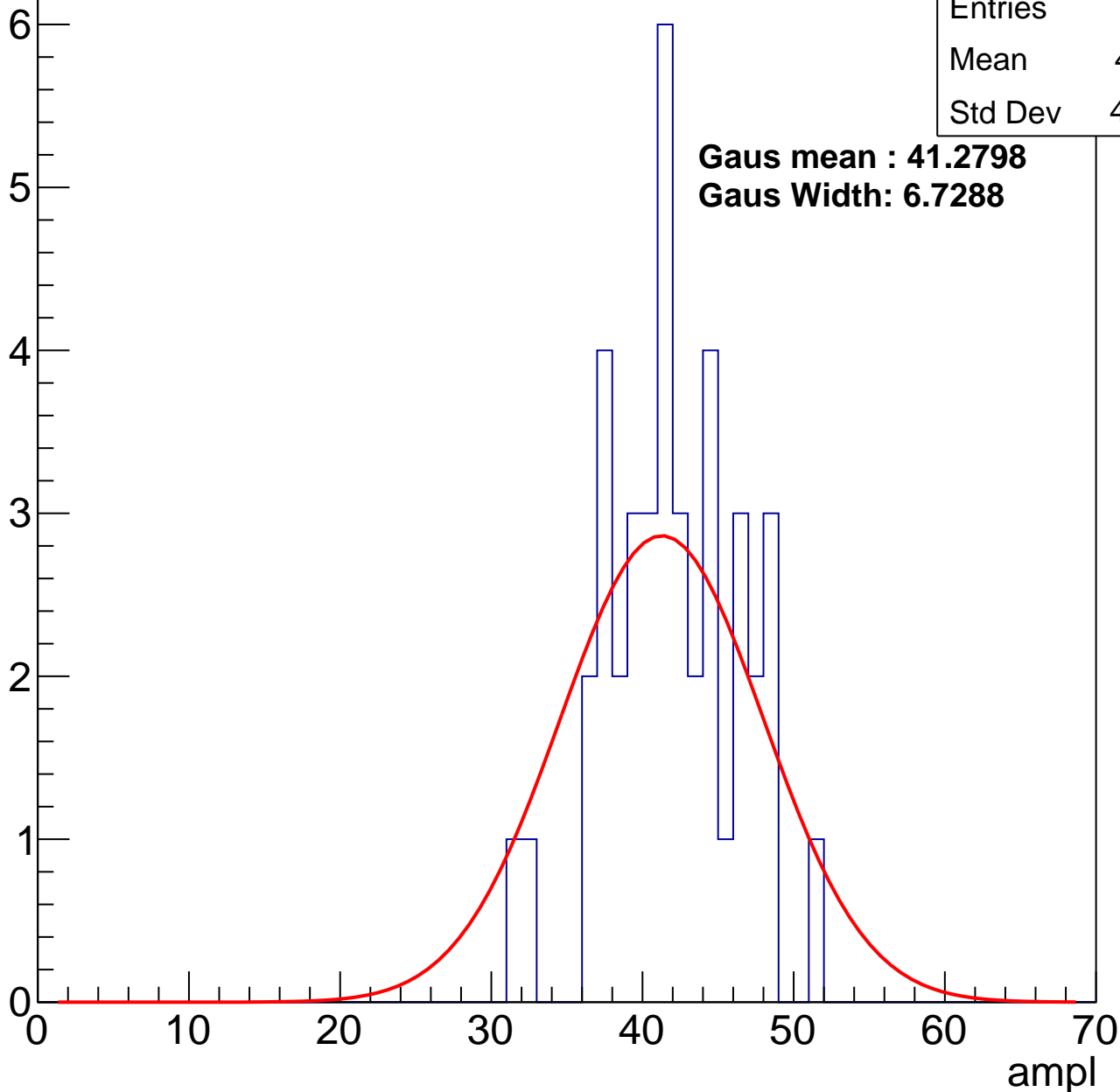
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	41
Mean	41.51
Std Dev	4.346

**Gaus mean : 41.2798**

**Gaus Width: 6.7288**

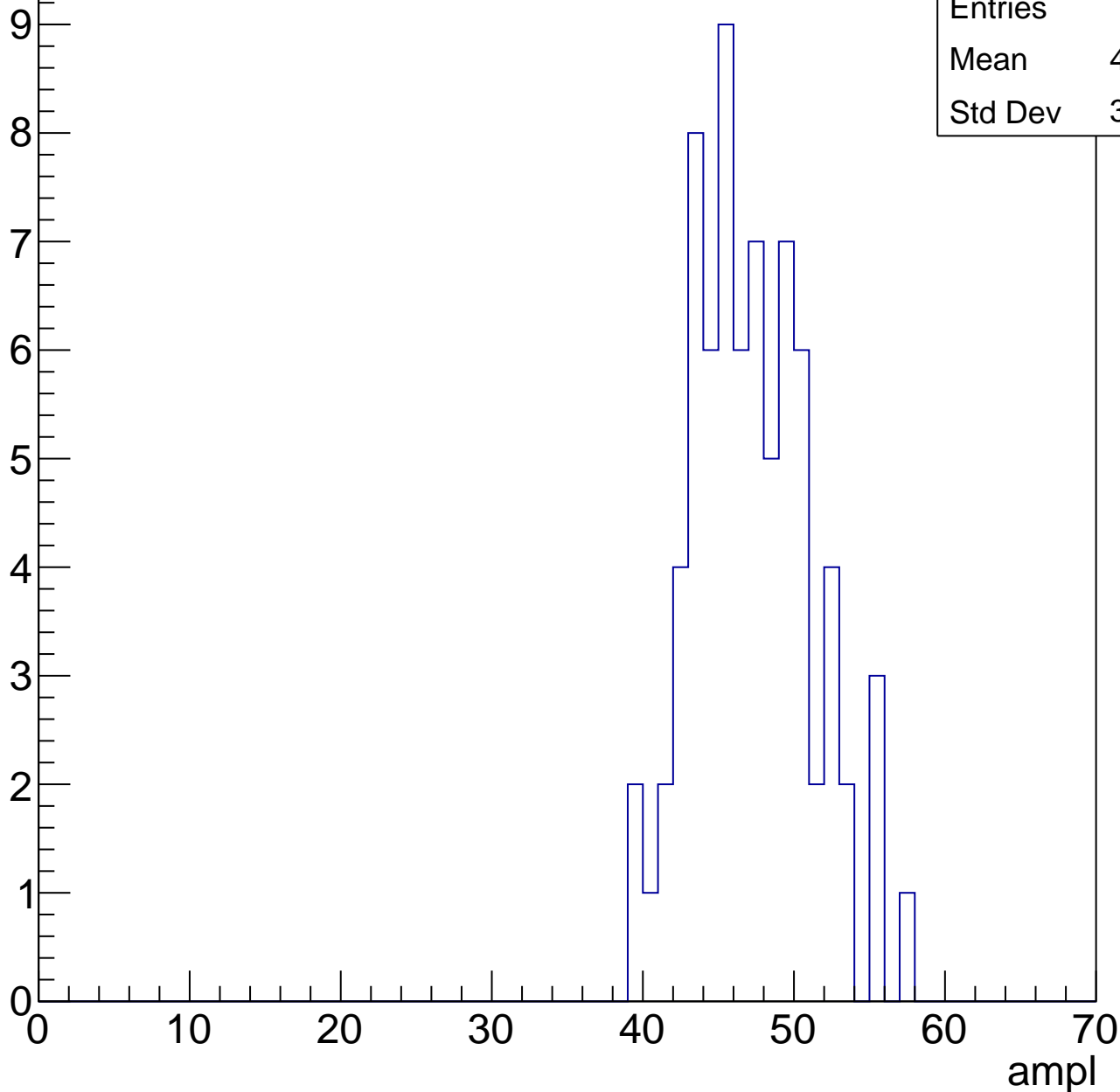


# B1L103S, U3-ch120, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	46.76
Std Dev	3.919

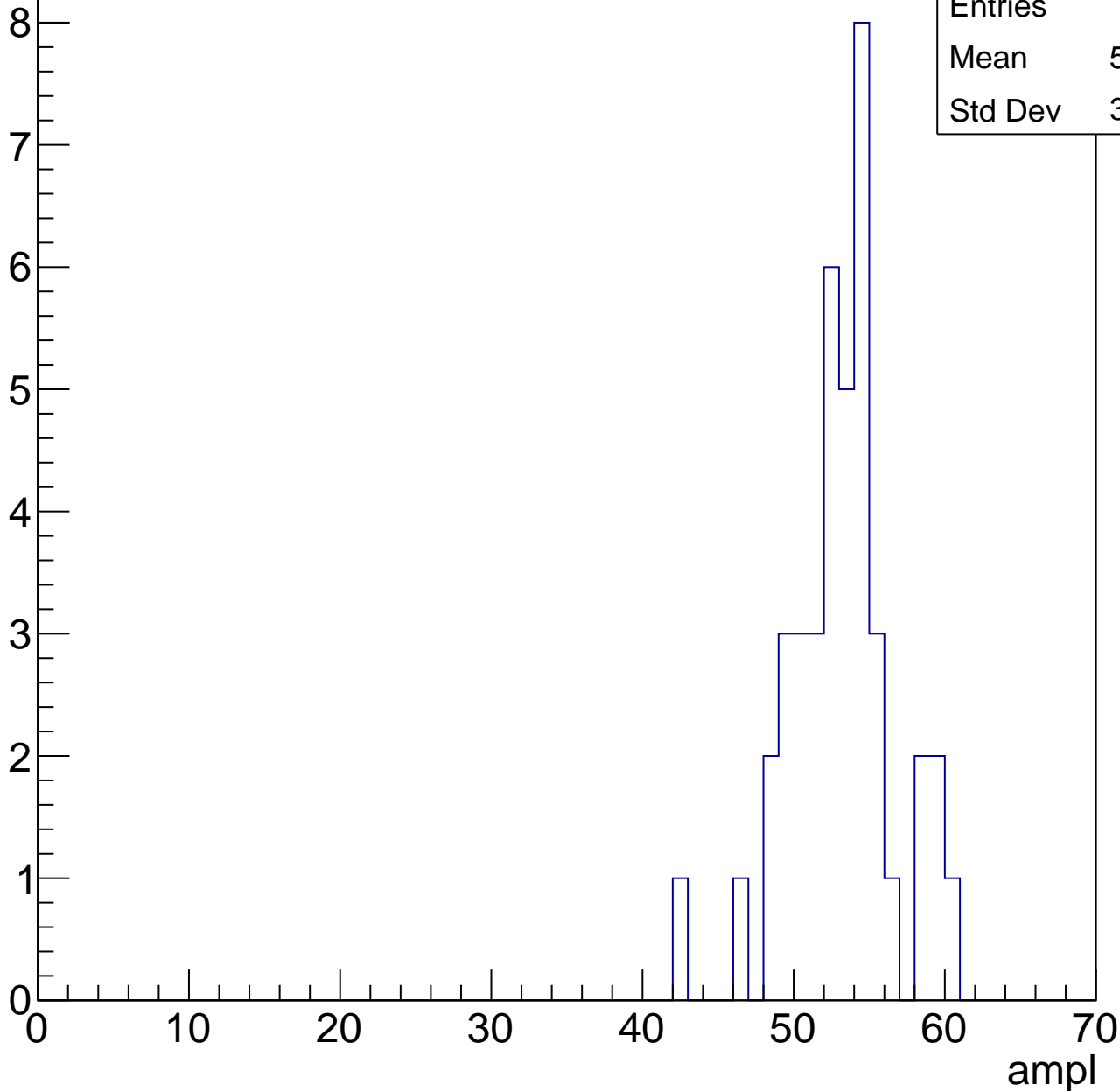


# B1L103S, U3-ch120, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	41
Mean	52.63
Std Dev	3.518

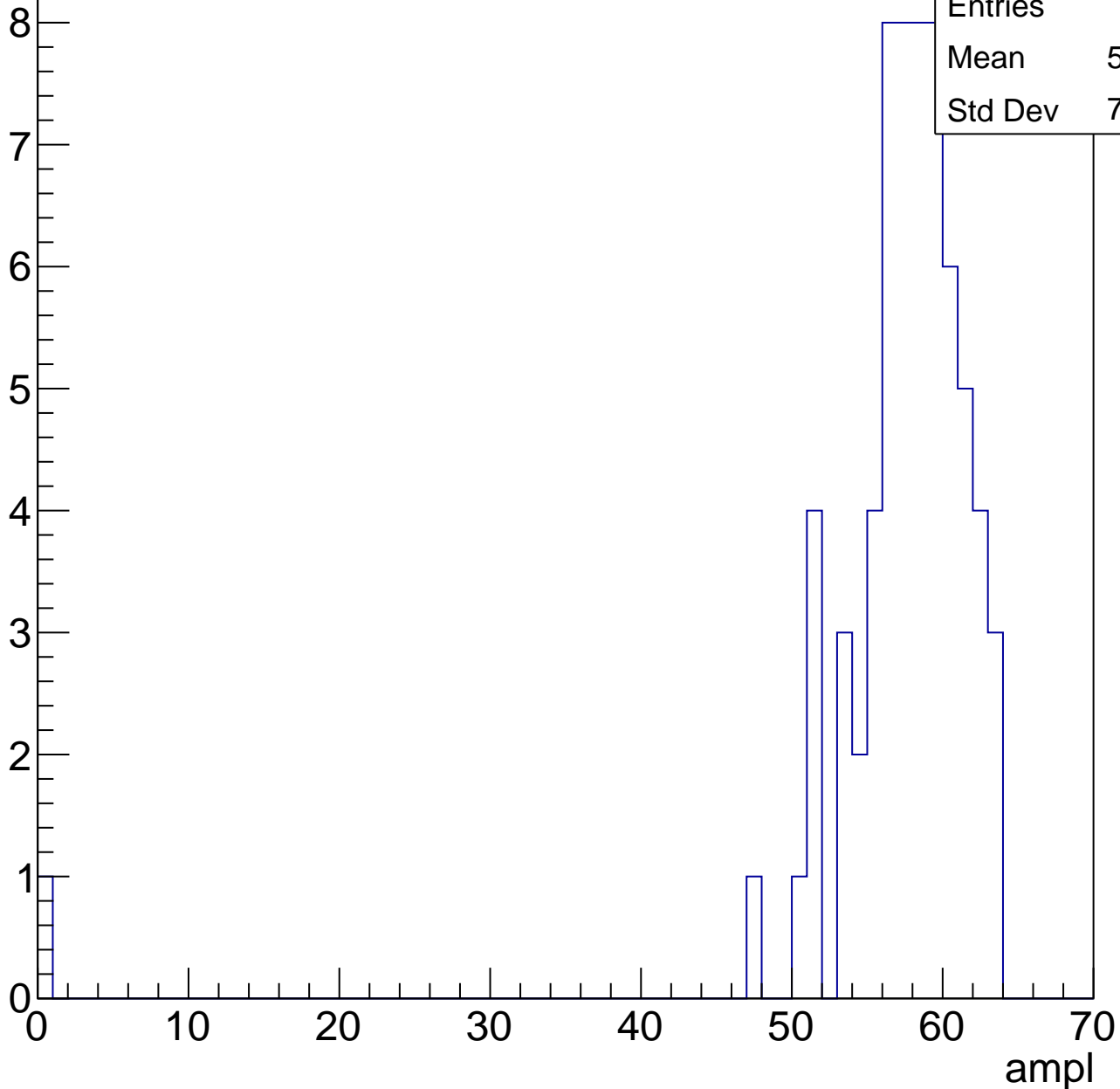


# B1L103S, U3-ch120, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	56.52
Std Dev	7.784

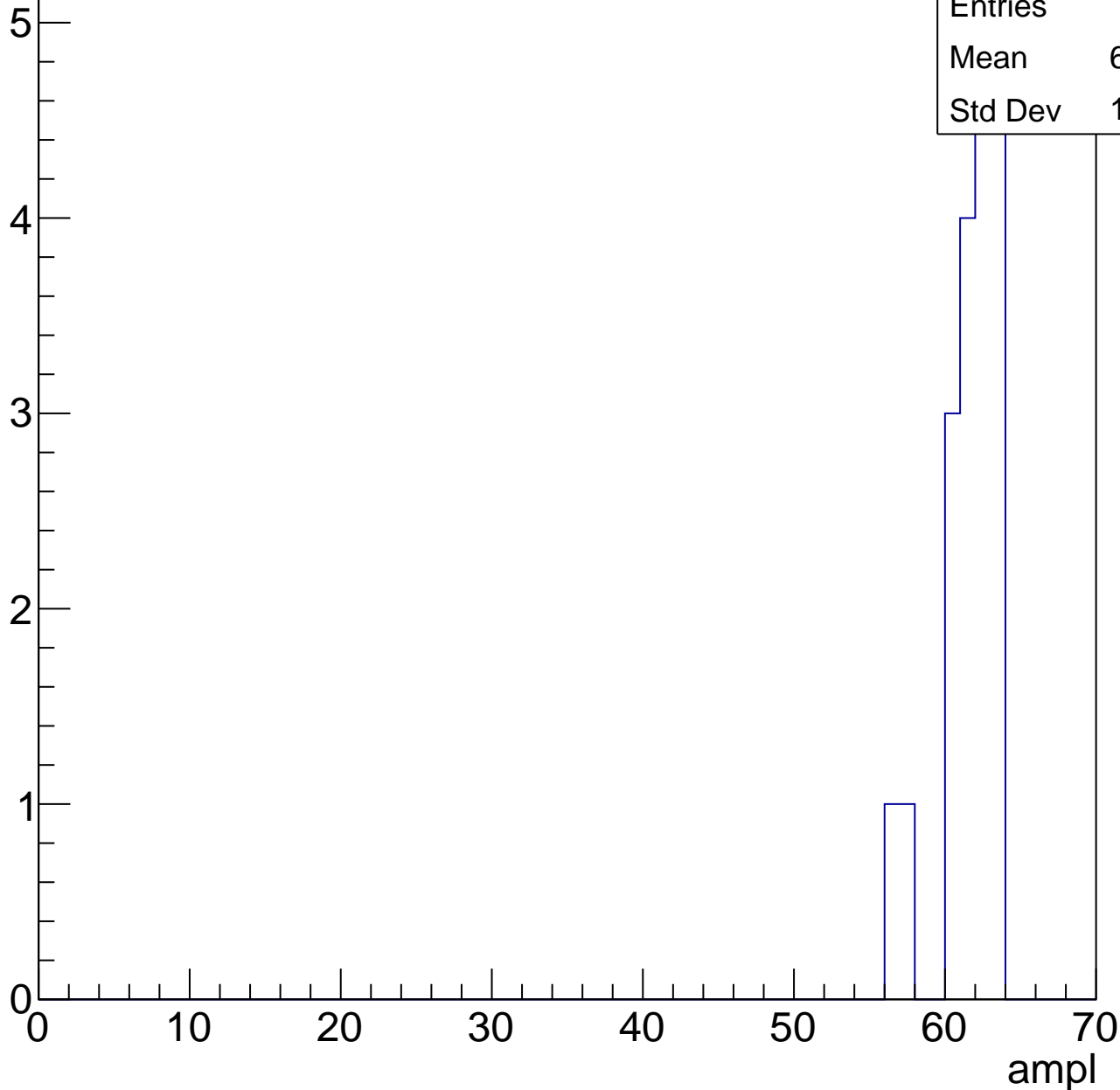


# B1L103S, U3-ch120, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	19
Mean	61.16
Std Dev	1.899

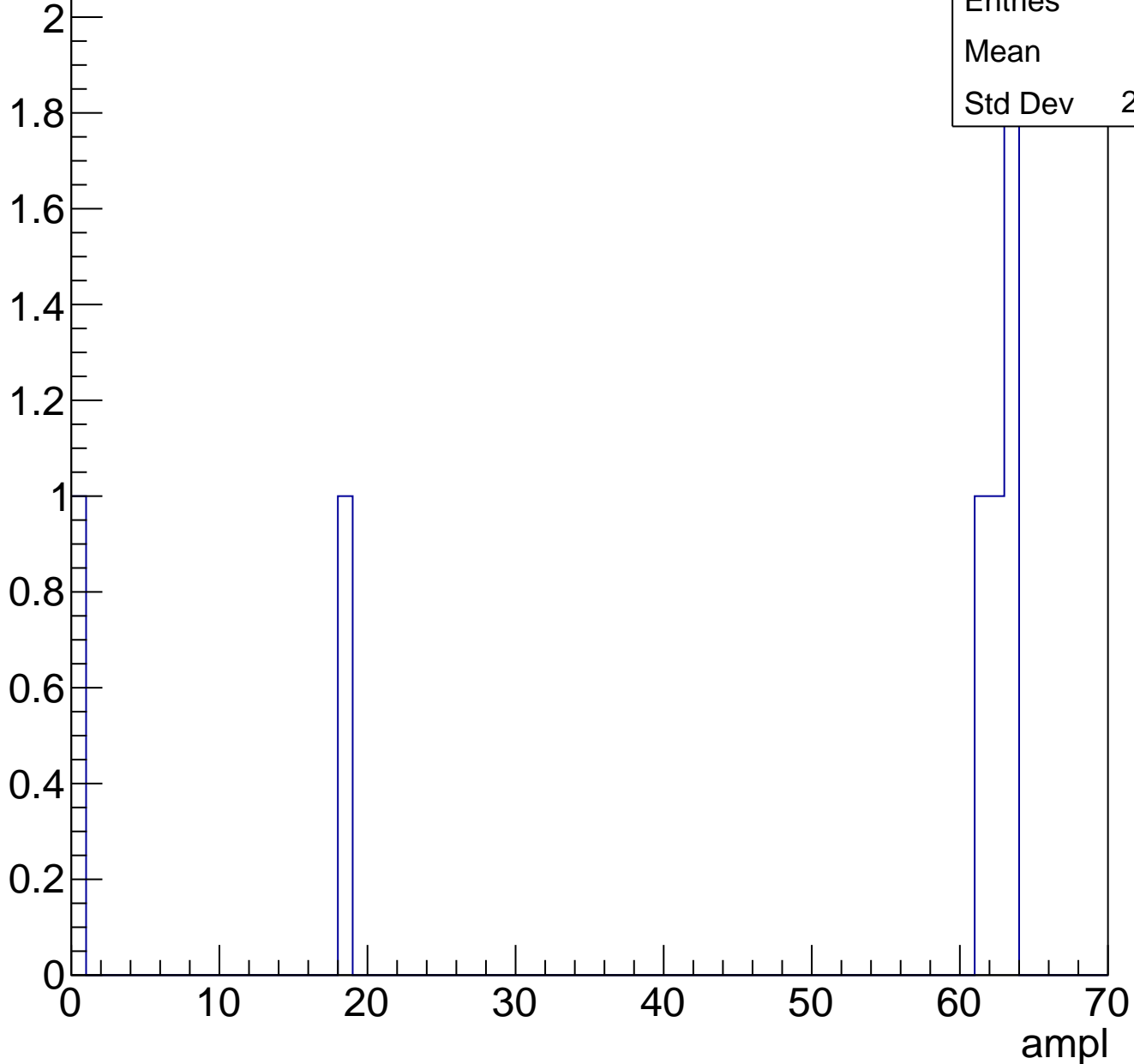




# B1L103S, U3-ch120, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch121, adc0

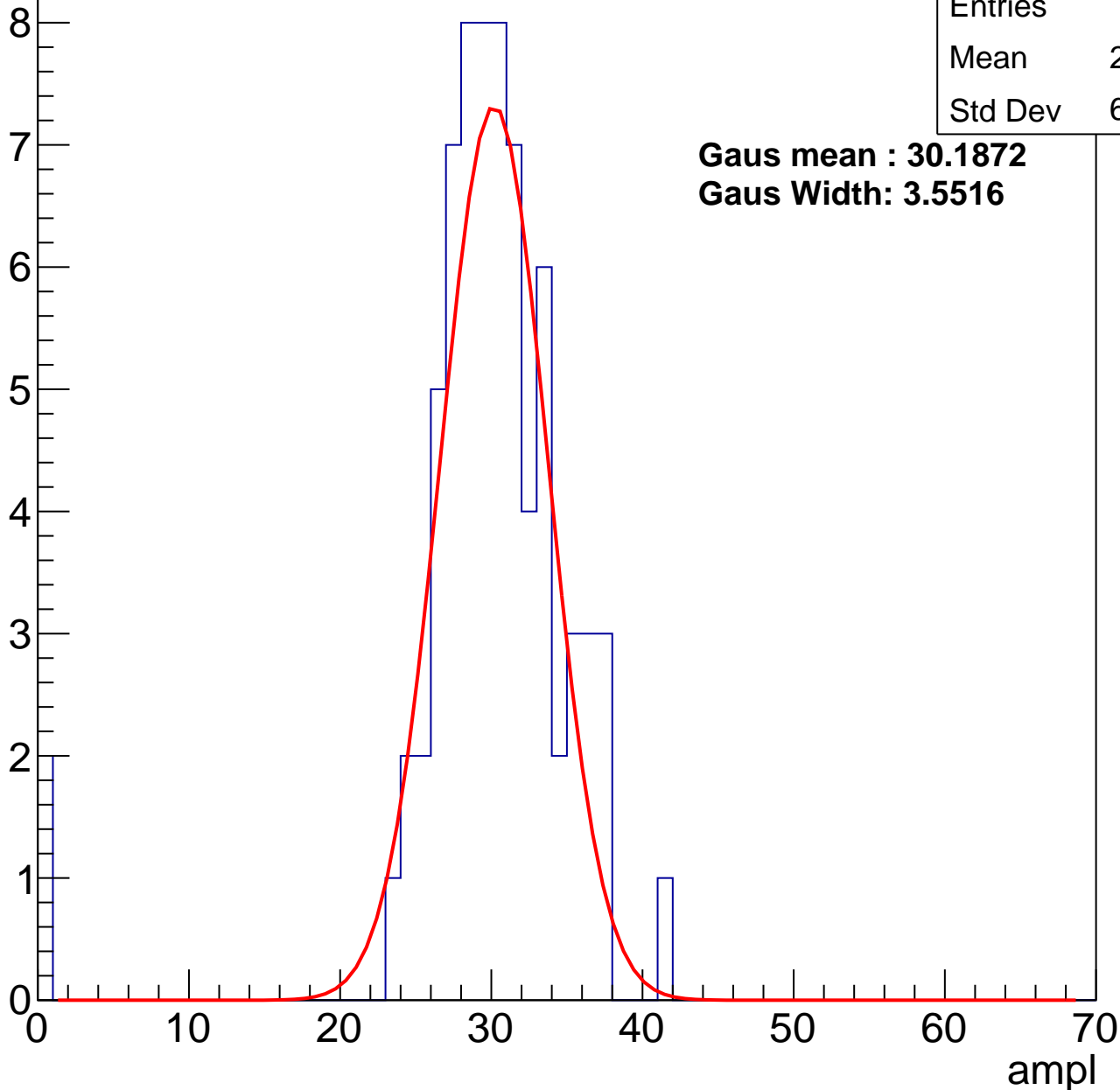
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	29.33
Std Dev	6.103

**Gaus mean : 30.1872**

**Gaus Width: 3.5516**



# B1L103S, U3-ch121, adc1

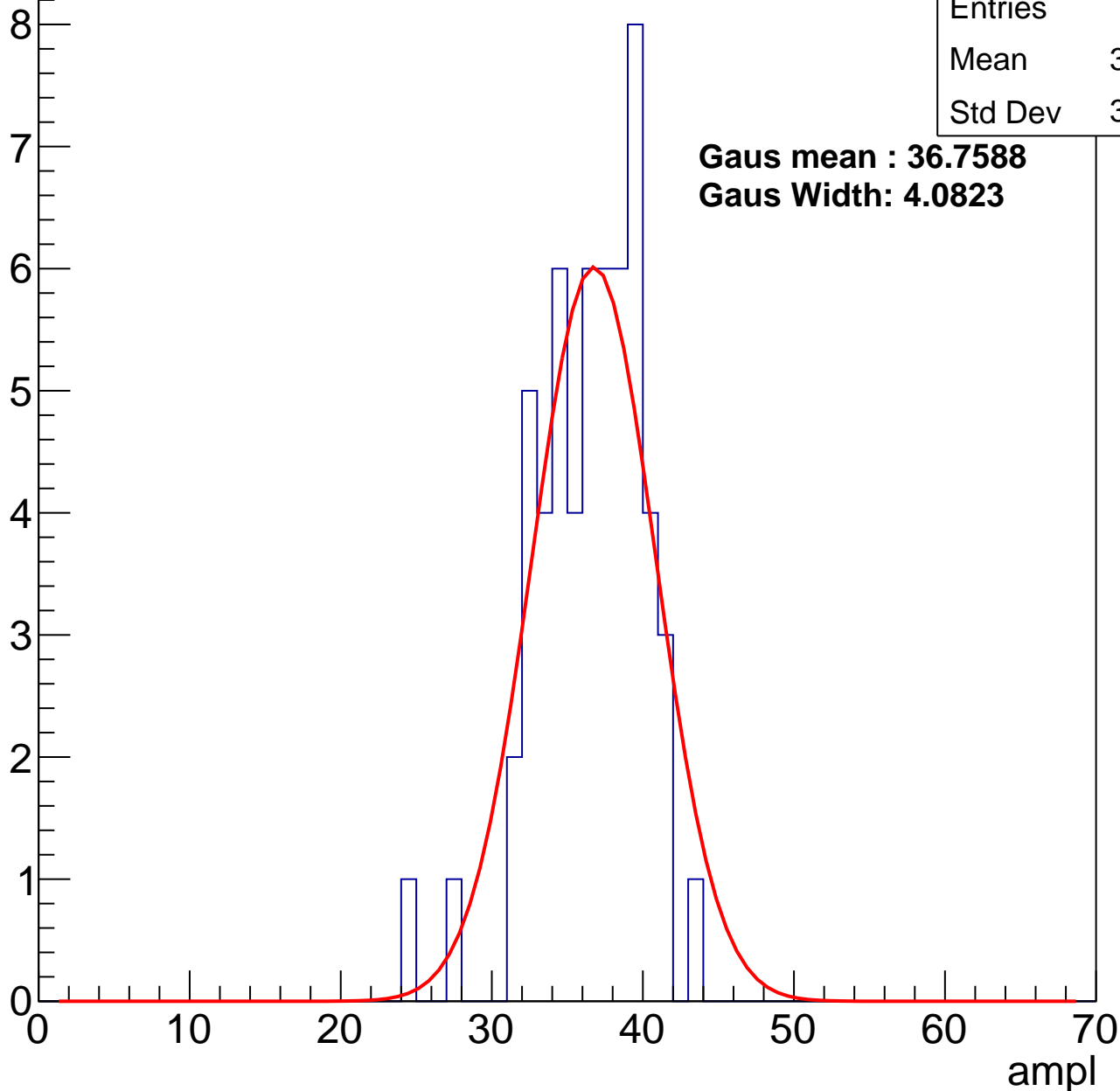
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	36.02
Std Dev	3.527

**Gaus mean : 36.7588**

**Gaus Width: 4.0823**



# B1L103S, U3-ch121, adc2

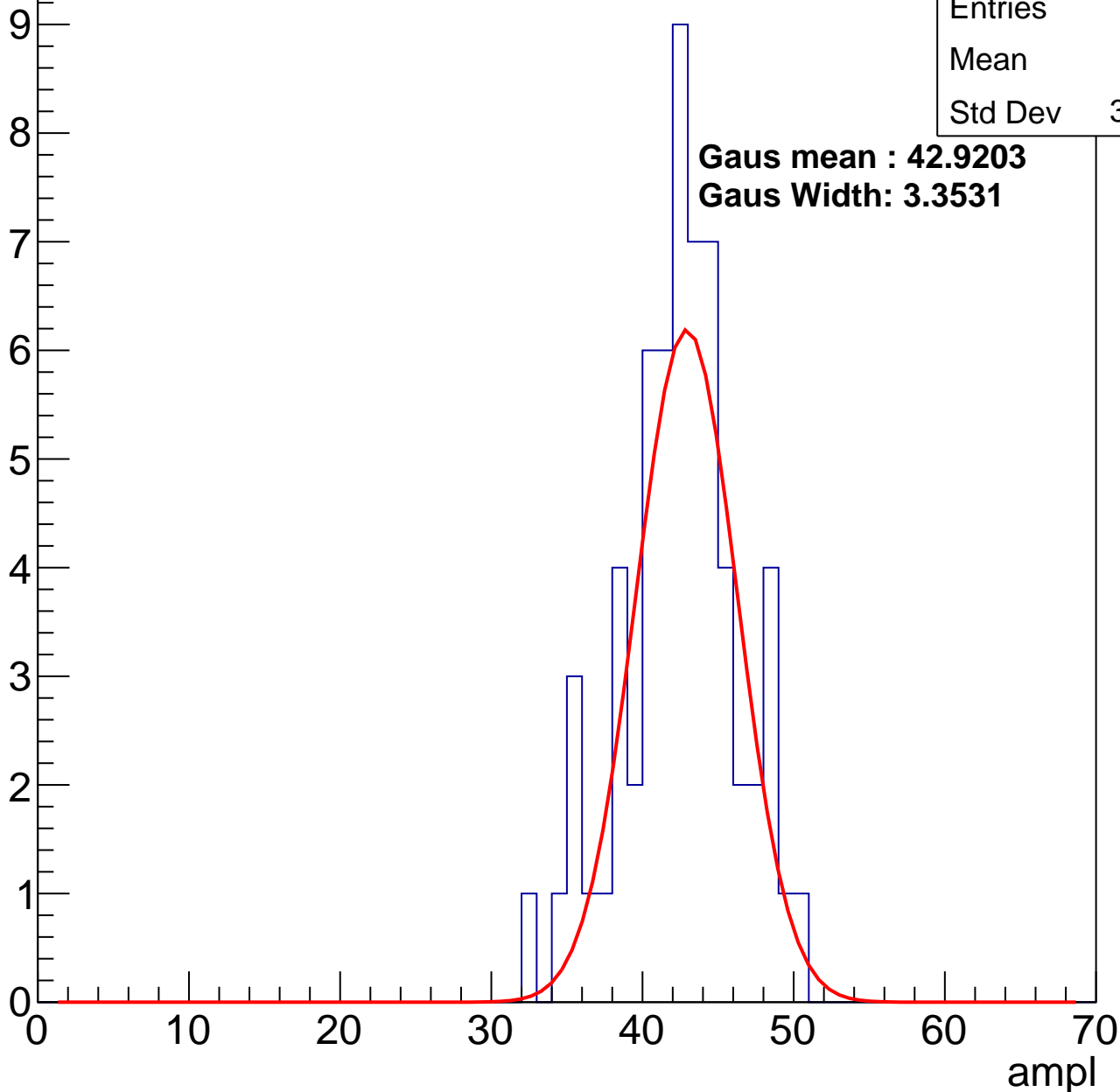
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	42
Std Dev	3.797

**Gaus mean : 42.9203**

**Gaus Width: 3.3531**

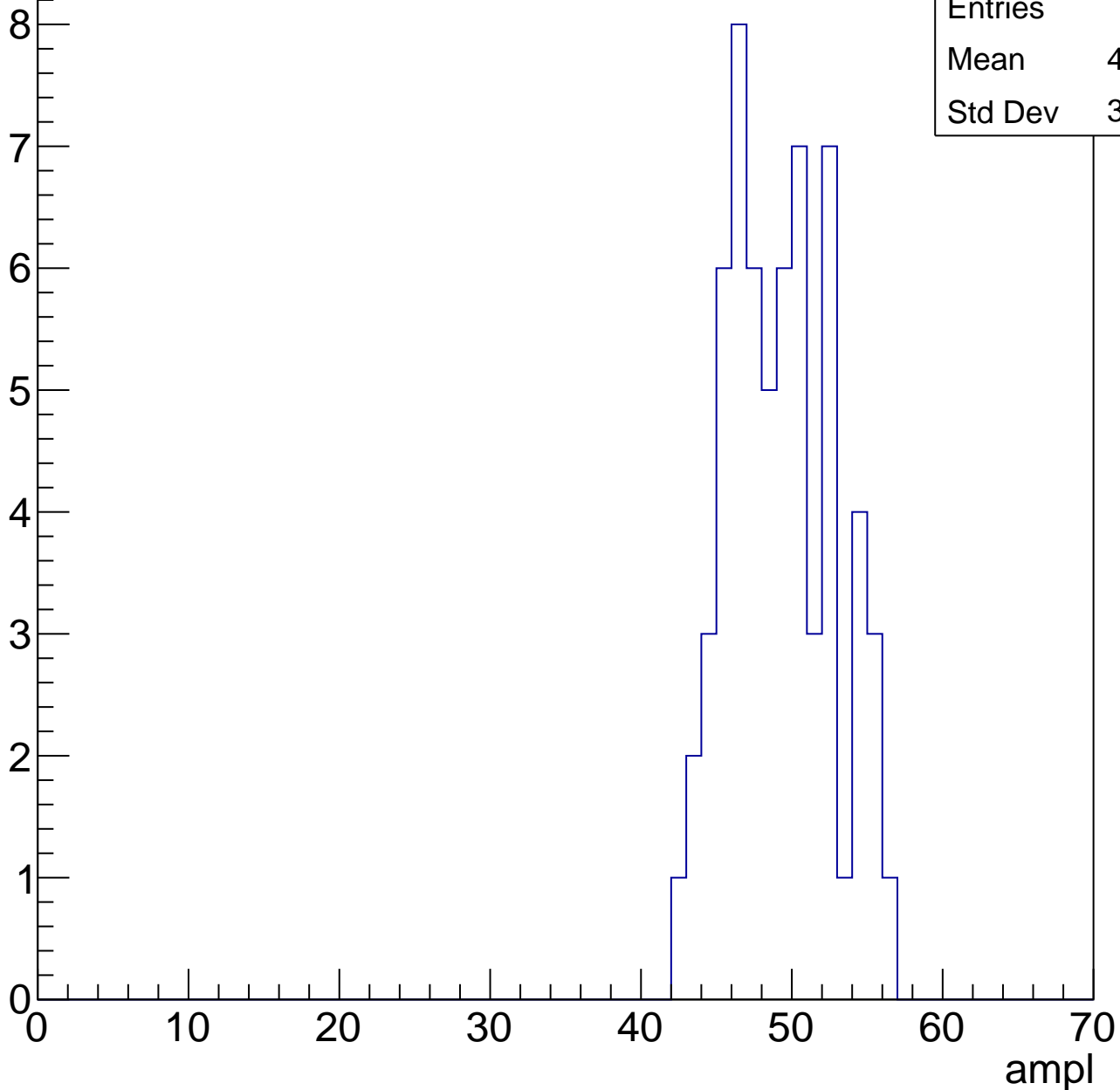


# B1L103S, U3-ch121, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	48.75
Std Dev	3.436

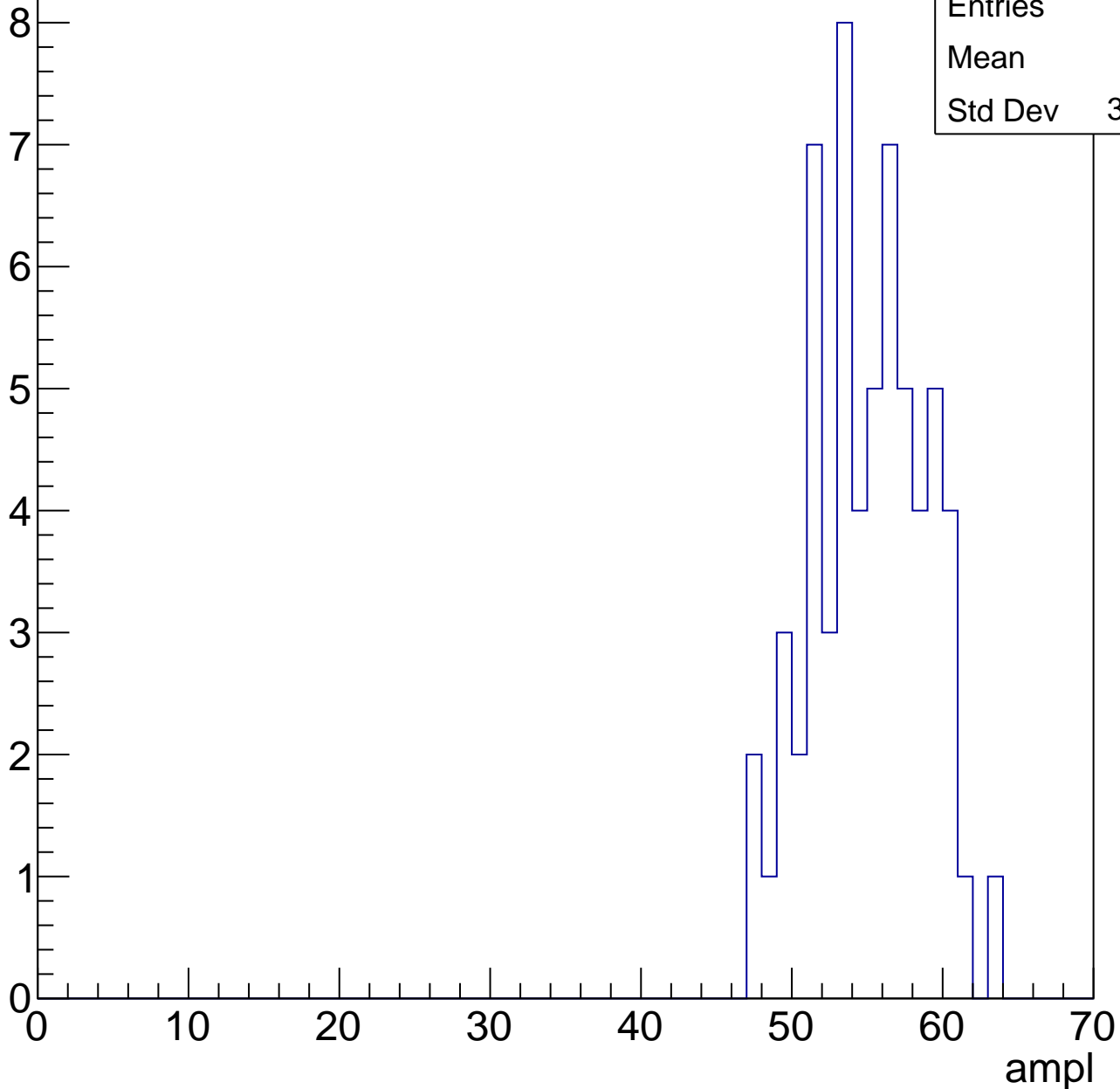


# B1L103S, U3-ch121, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	54.6
Std Dev	3.687

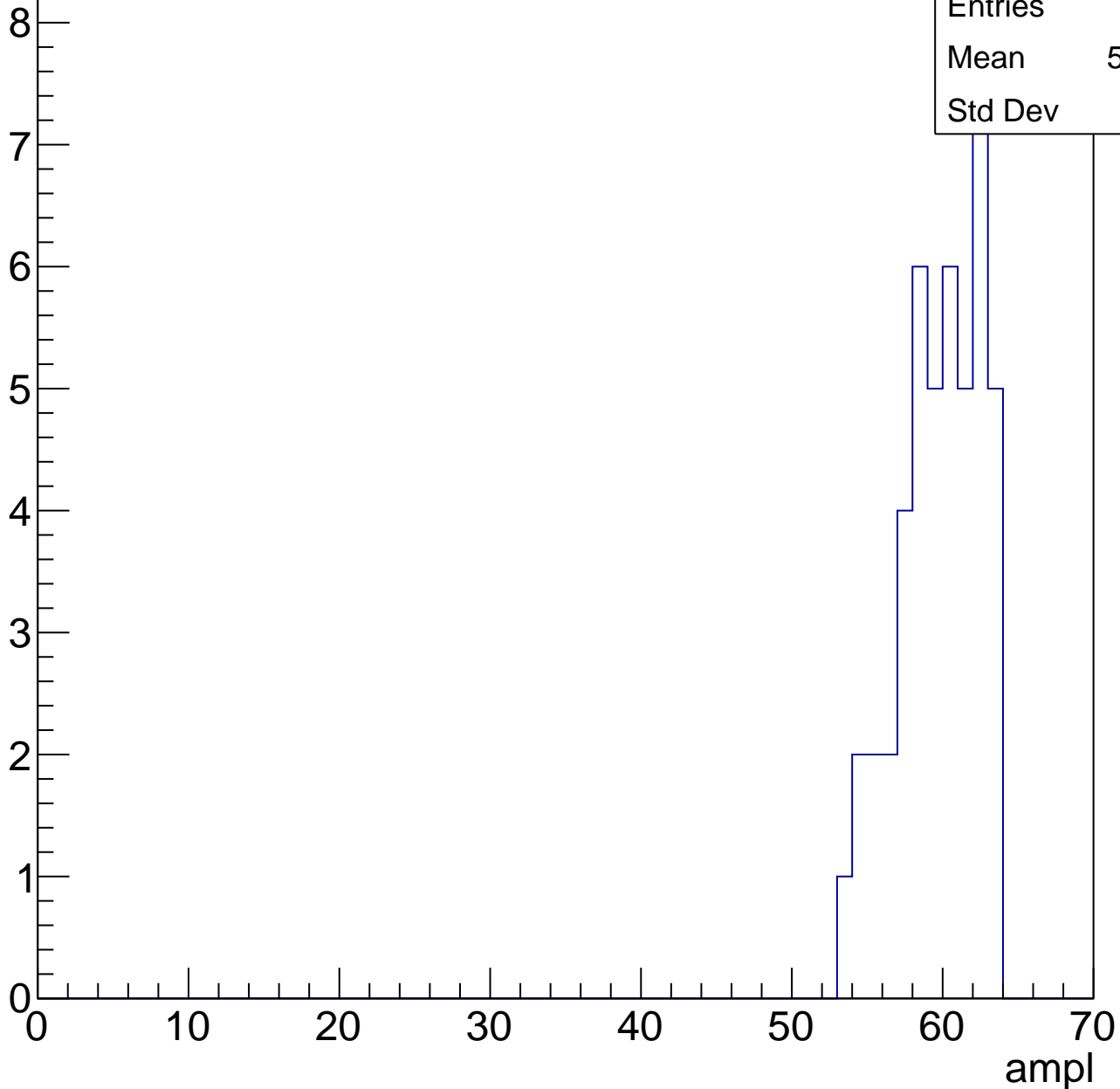


# B1L103S, U3-ch121, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

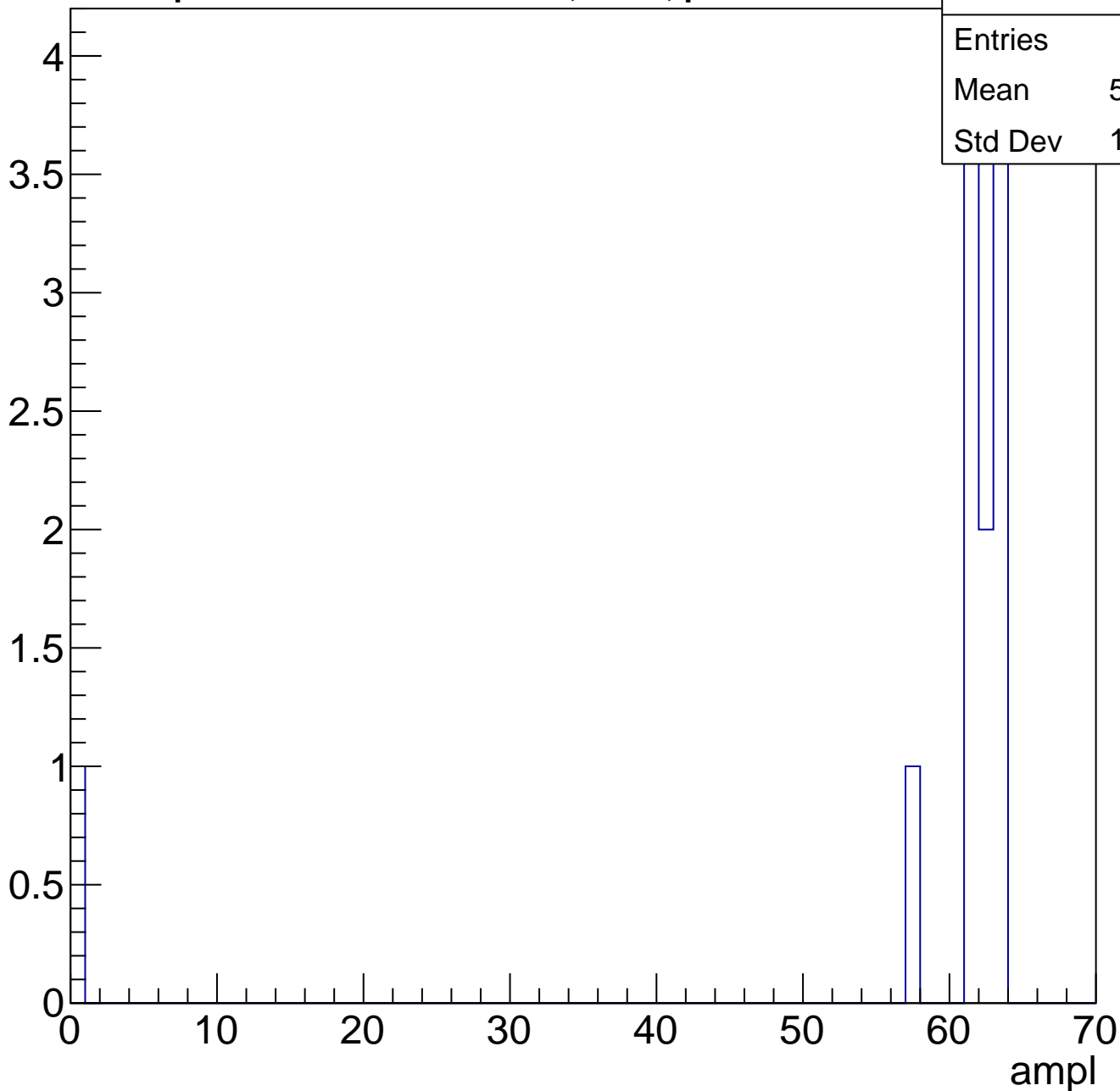
Entries	46
Mean	59.35
Std Dev	2.68



# B1L103S, U3-ch121, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U3-ch121, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch122, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	72
Mean	29.9
Std Dev	5.94

**Gaus mean : 30.7557**

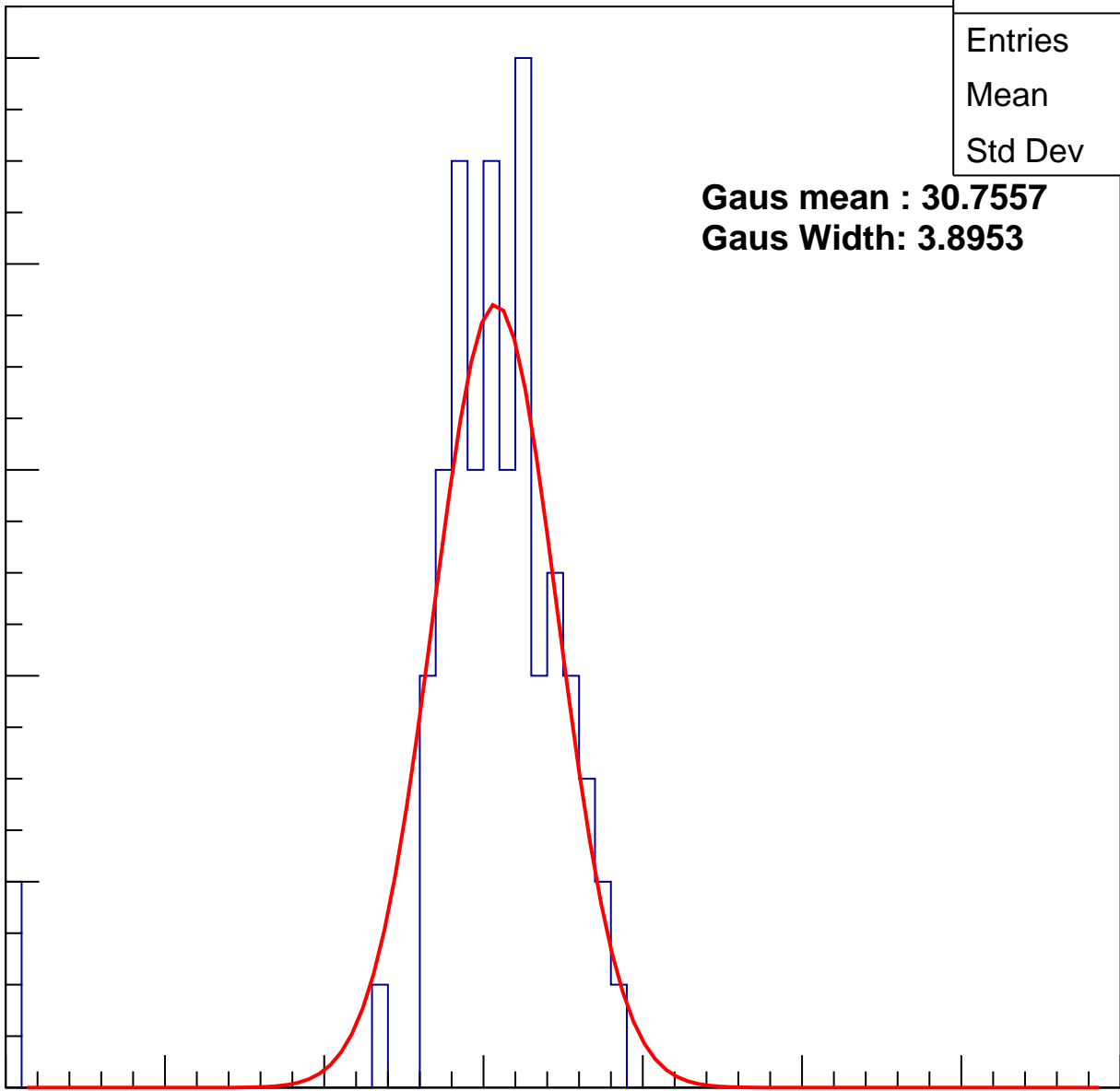
**Gaus Width: 3.8953**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U3-ch122, adc1

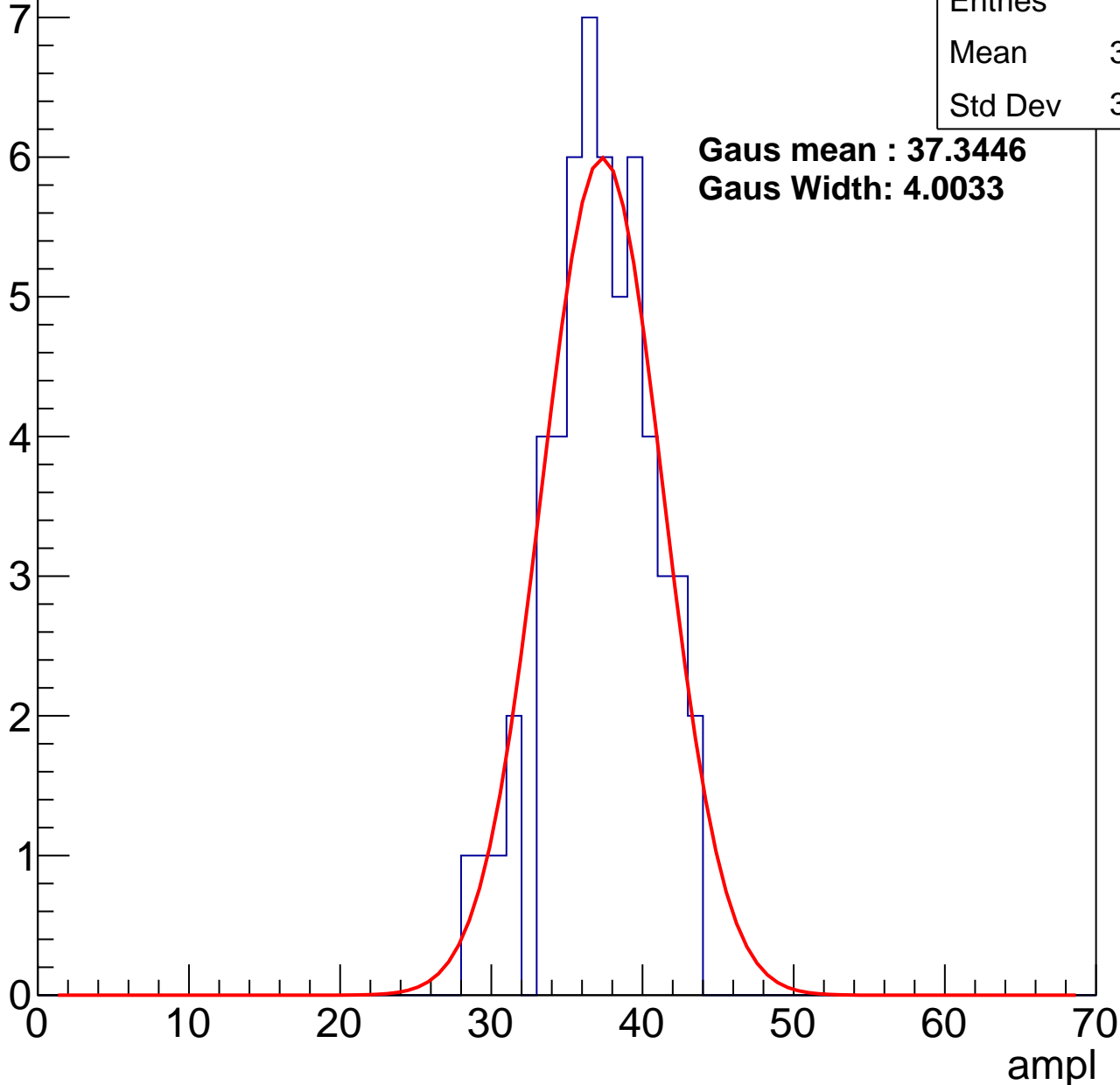
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	36.73
Std Dev	3.445

**Gaus mean : 37.3446**

**Gaus Width: 4.0033**



# B1L103S, U3-ch122, adc2

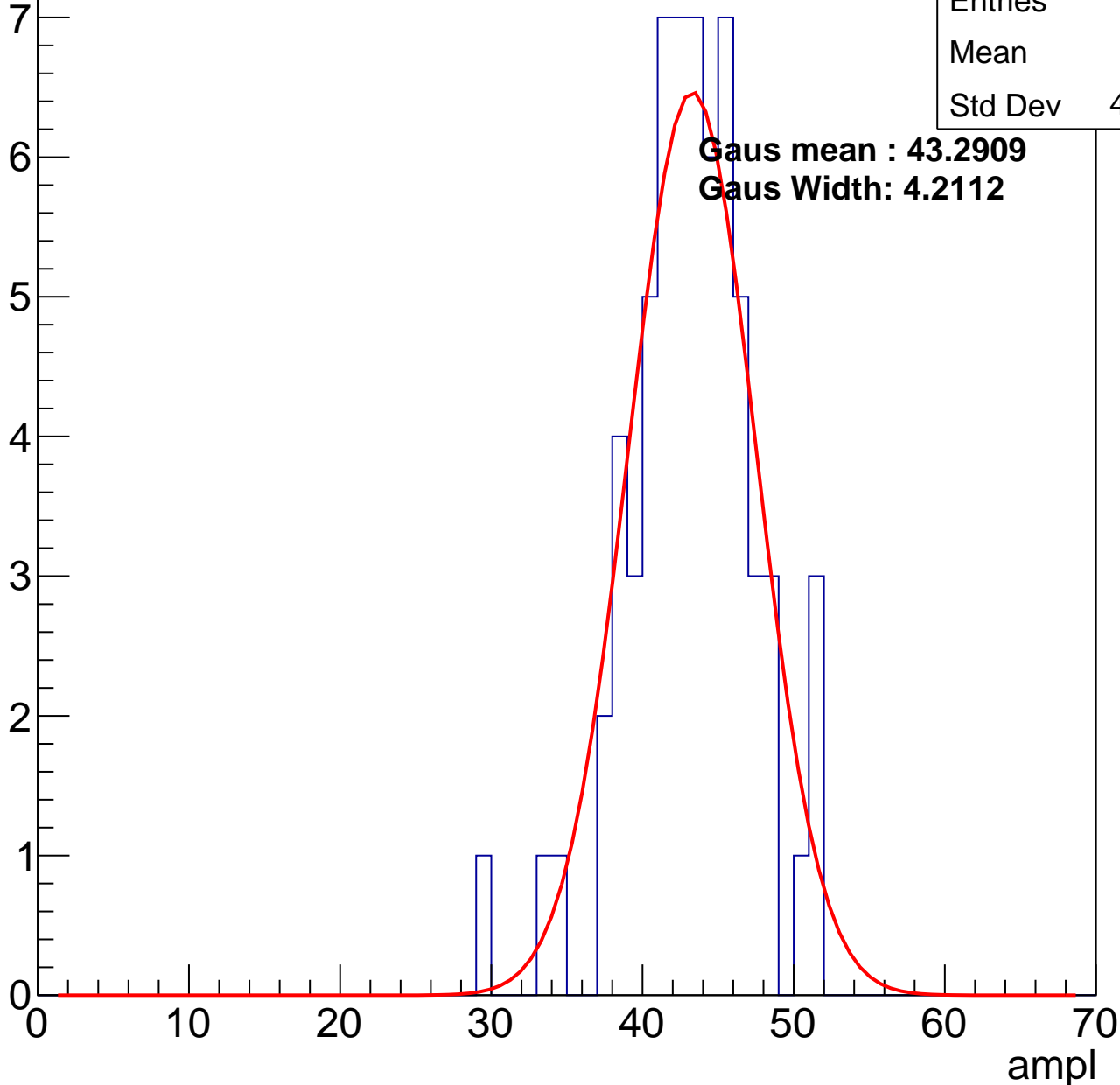
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	42.7
Std Dev	4.108

**Gaus mean : 43.2909**

**Gaus Width: 4.2112**

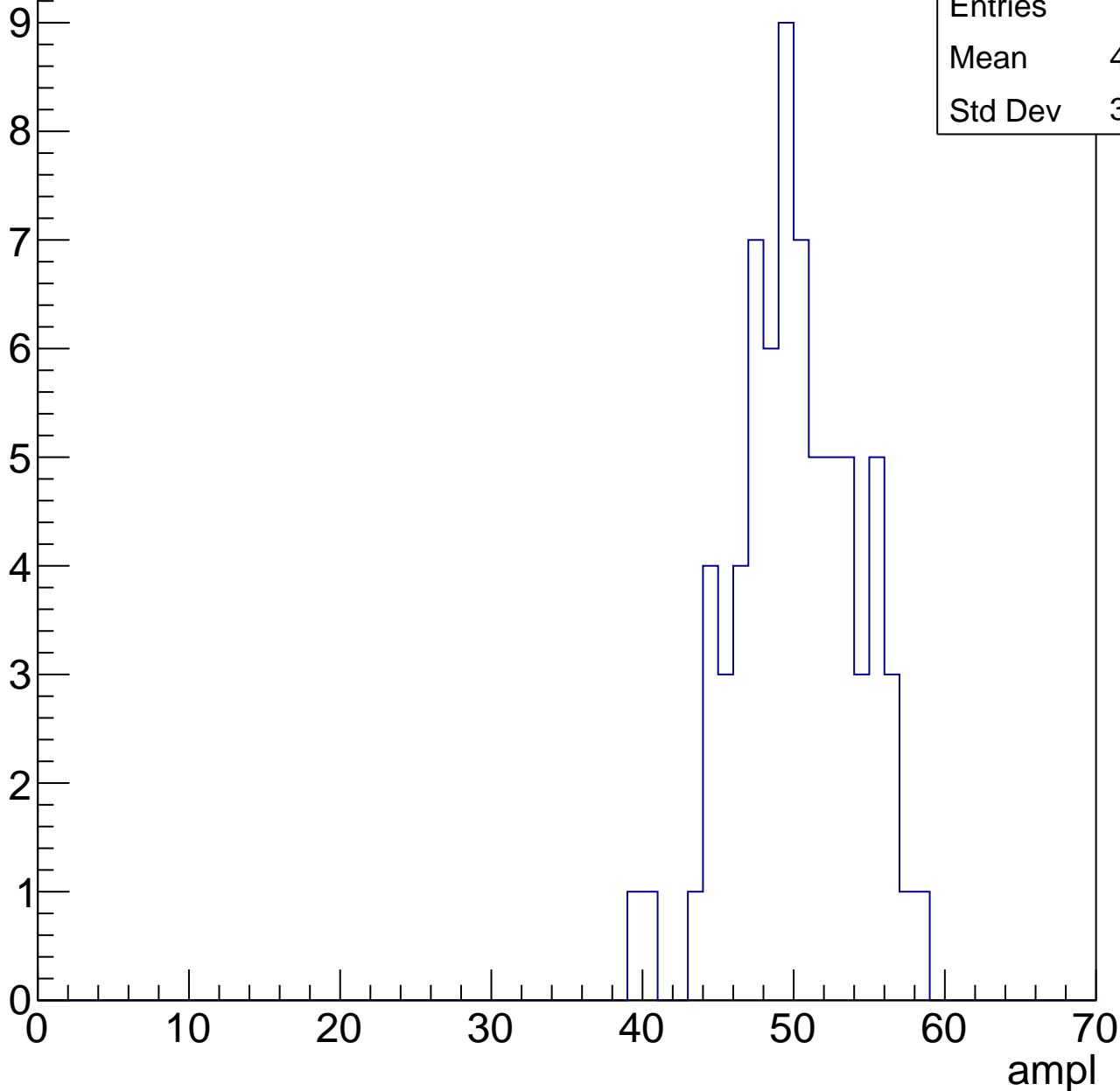


# B1L103S, U3-ch122, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	49.65
Std Dev	3.944

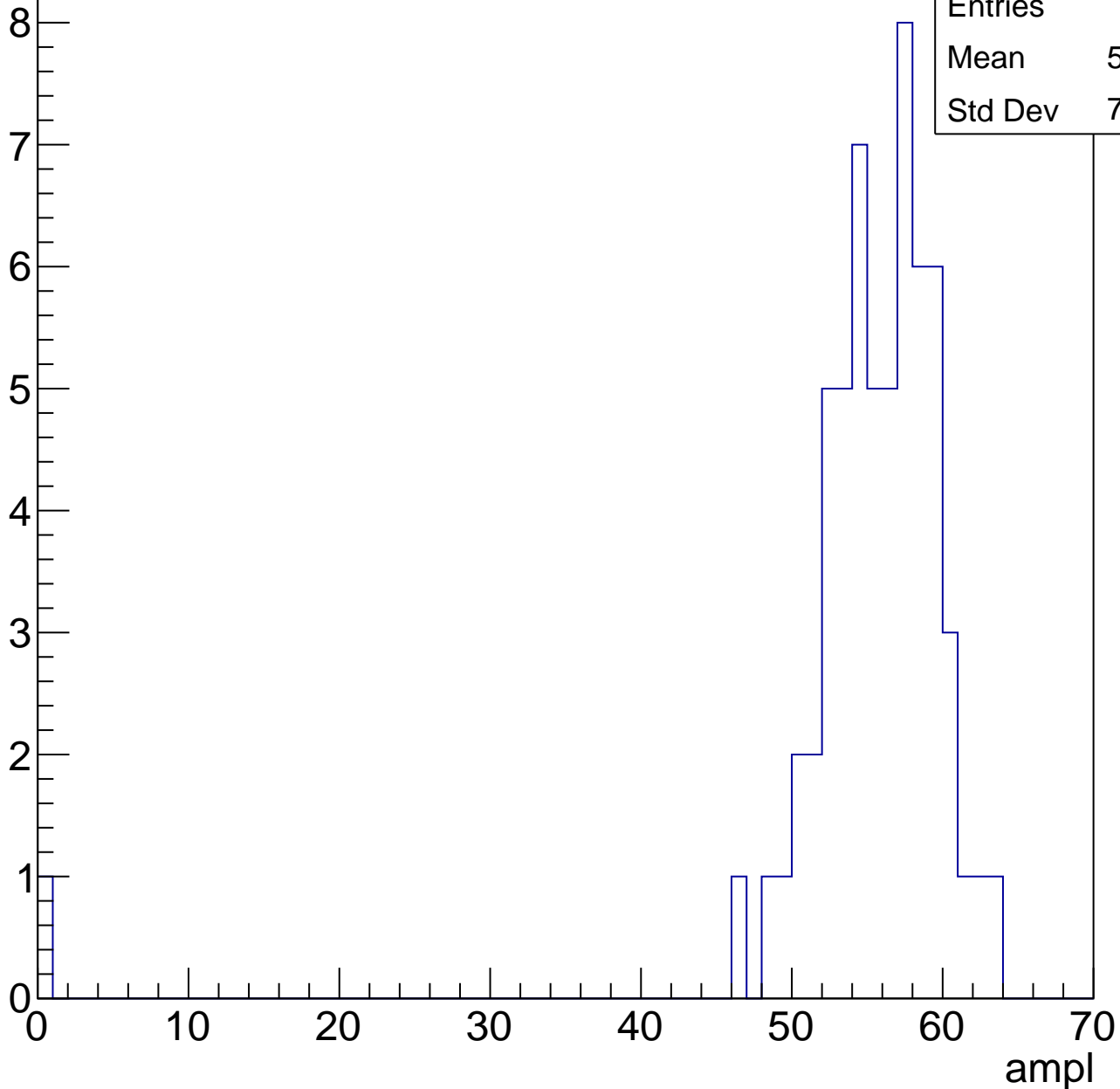


# B1L103S, U3-ch122, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

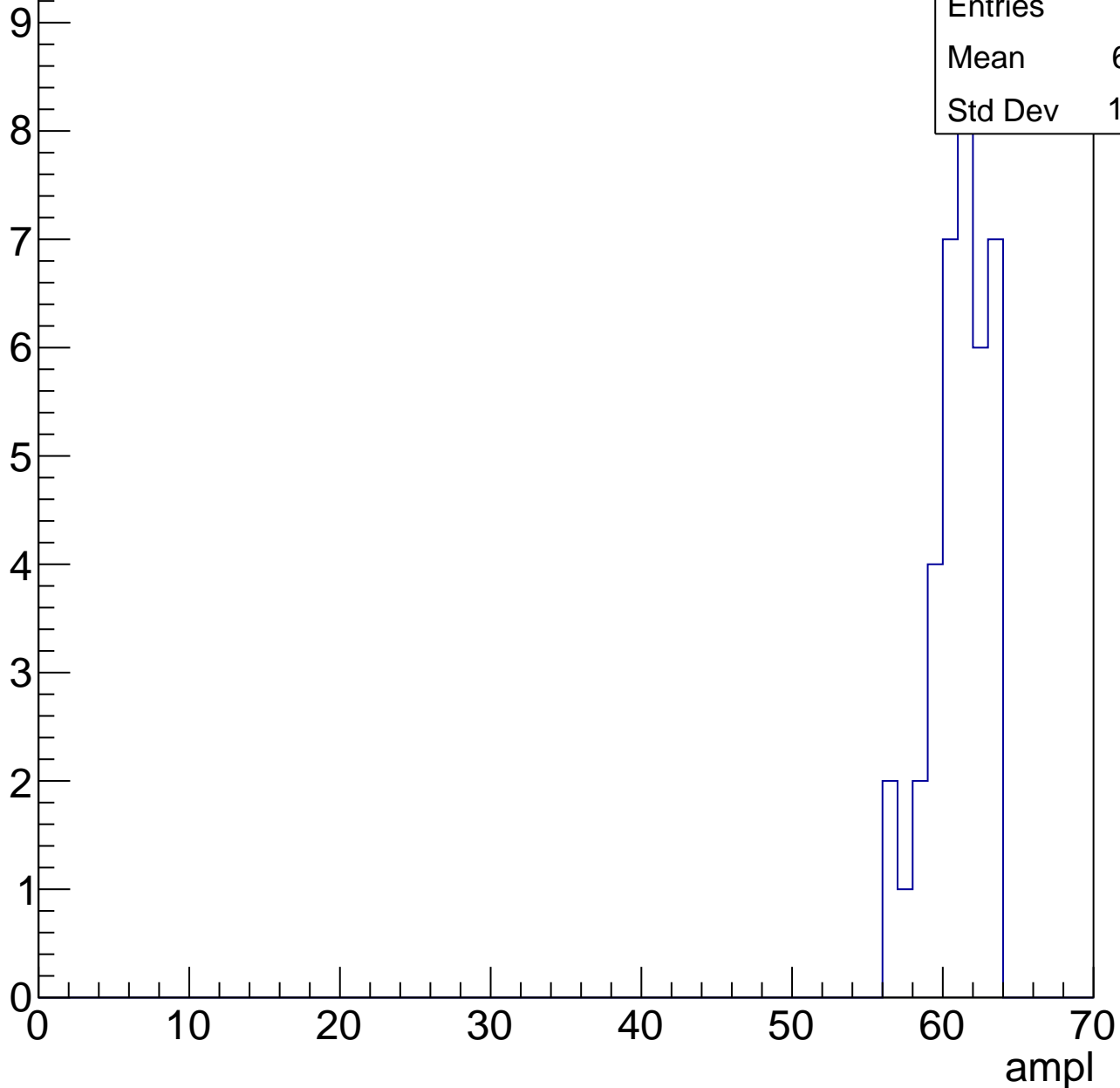
Entries	61
Mean	54.54
Std Dev	7.833



# B1L103S, U3-ch122, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

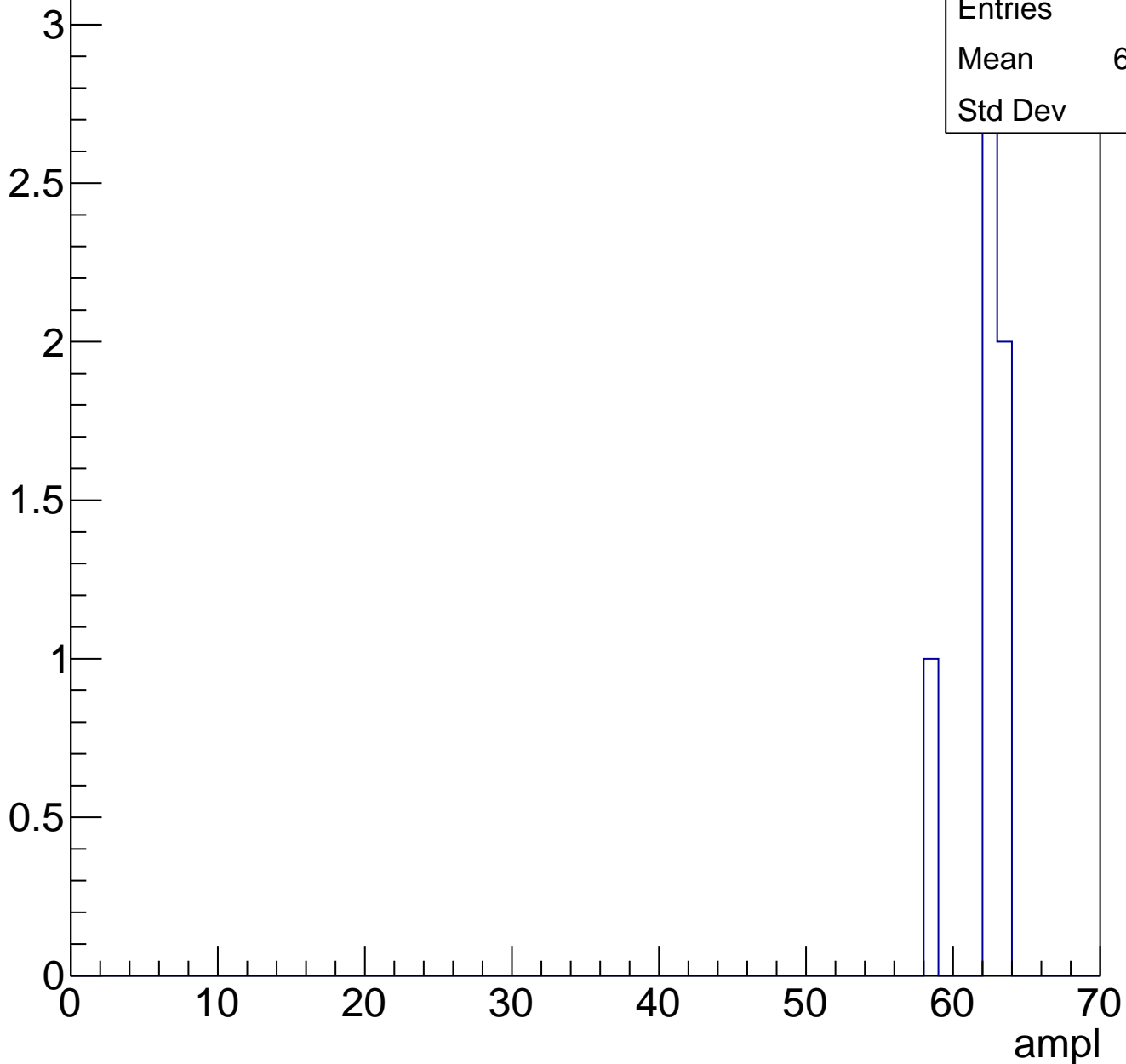


Entries	38
Mean	60.61
Std Dev	1.885

# B1L103S, U3-ch122, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U3-ch122, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U3-ch123, adc0

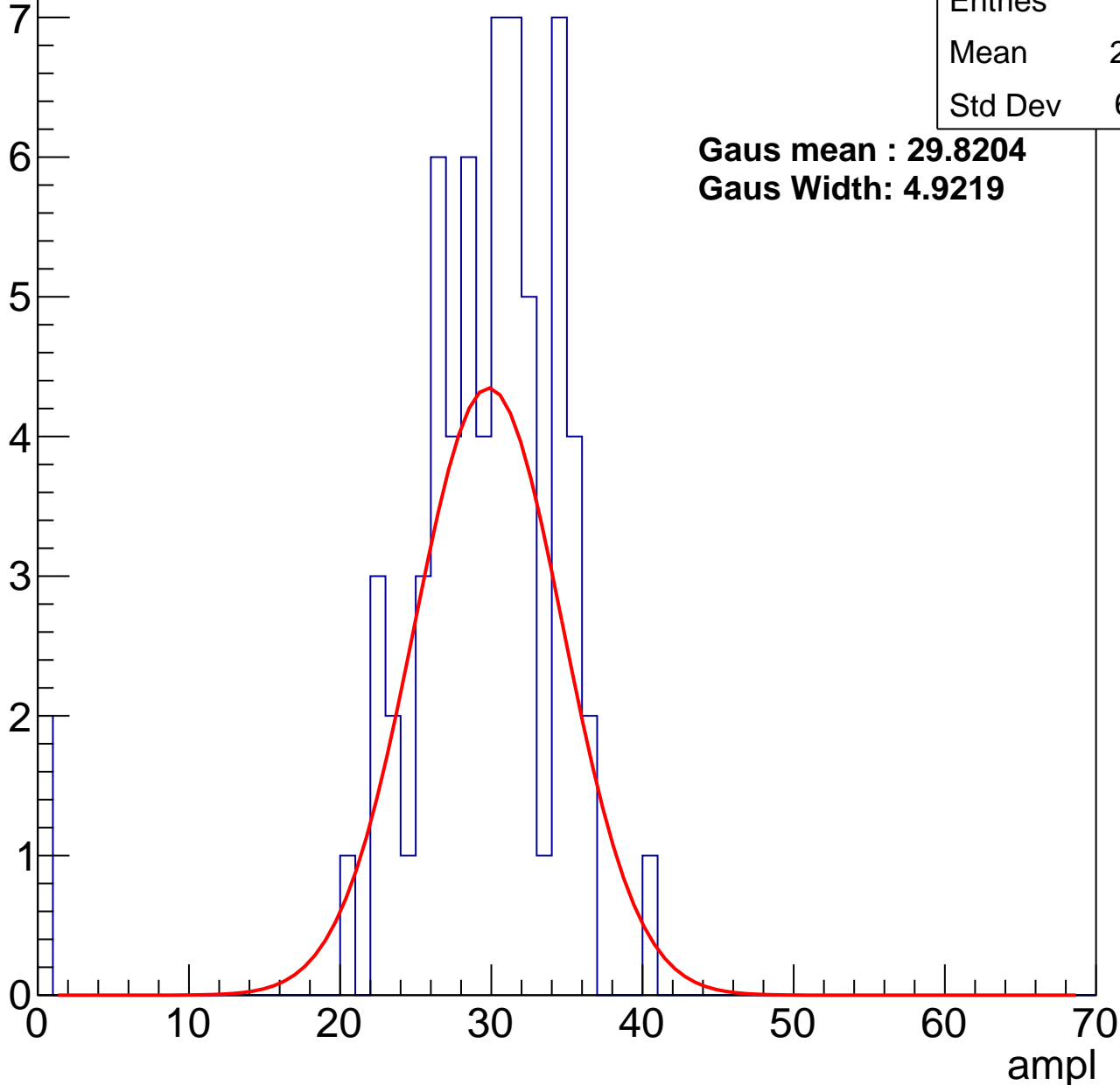
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	28.62
Std Dev	6.461

**Gaus mean : 29.8204**

**Gaus Width: 4.9219**



# B1L103S, U3-ch123, adc1

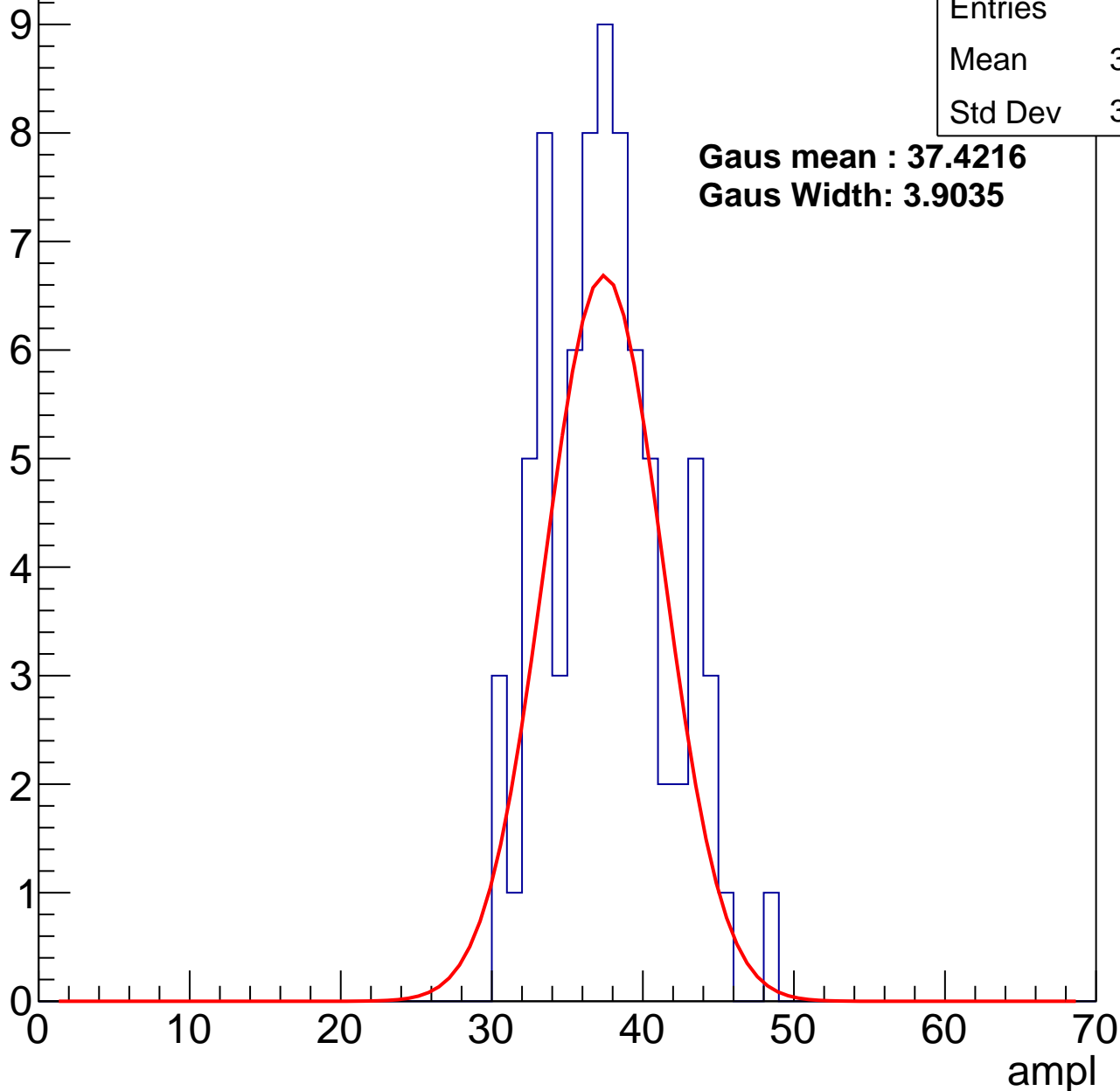
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	37.13
Std Dev	3.915

**Gaus mean : 37.4216**

**Gaus Width: 3.9035**



# B1L103S, U3-ch123, adc2

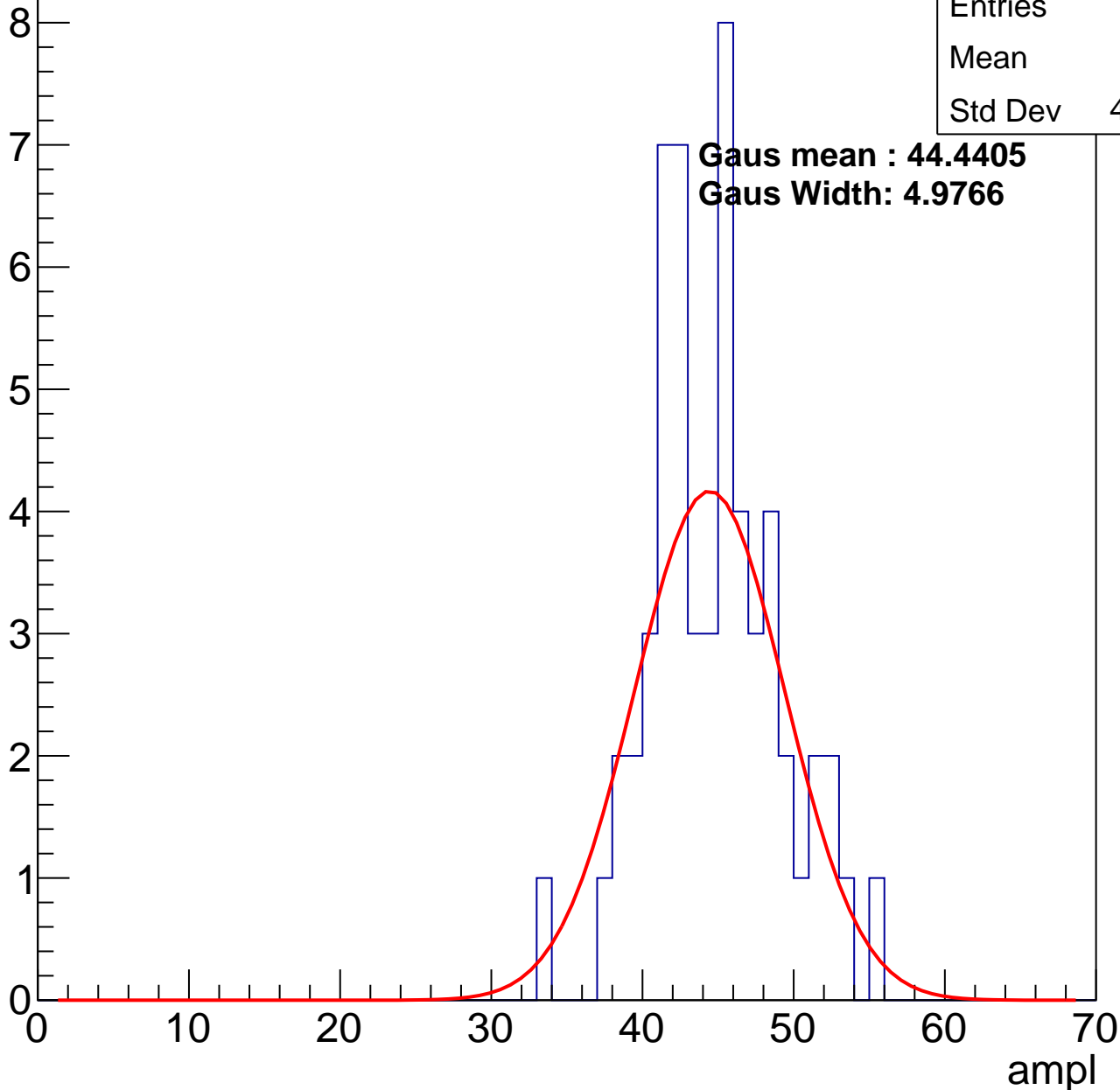
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	44.3
Std Dev	4.308

**Gaus mean : 44.4405**

**Gaus Width: 4.9766**

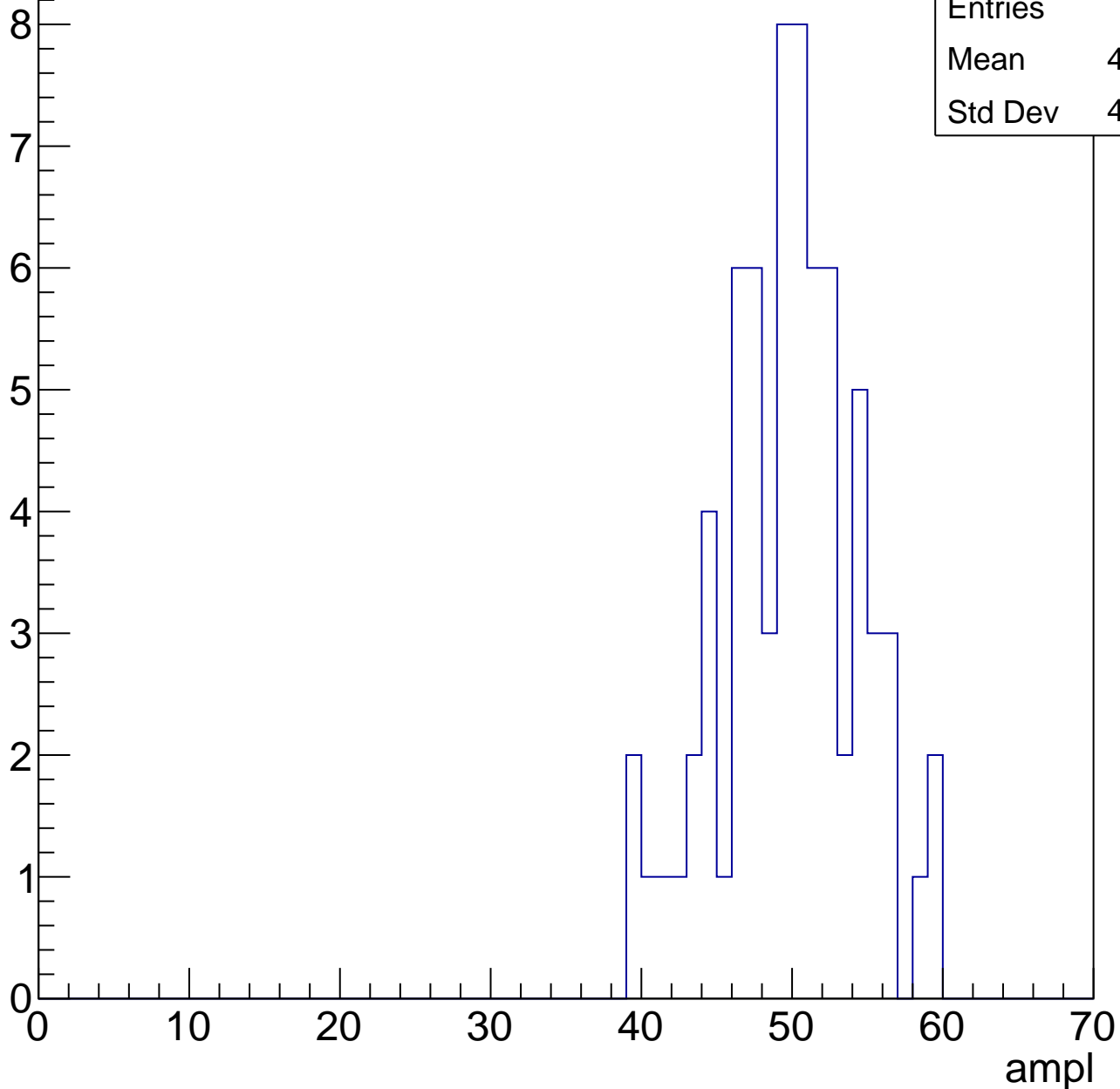


# B1L103S, U3-ch123, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	49.37
Std Dev	4.492

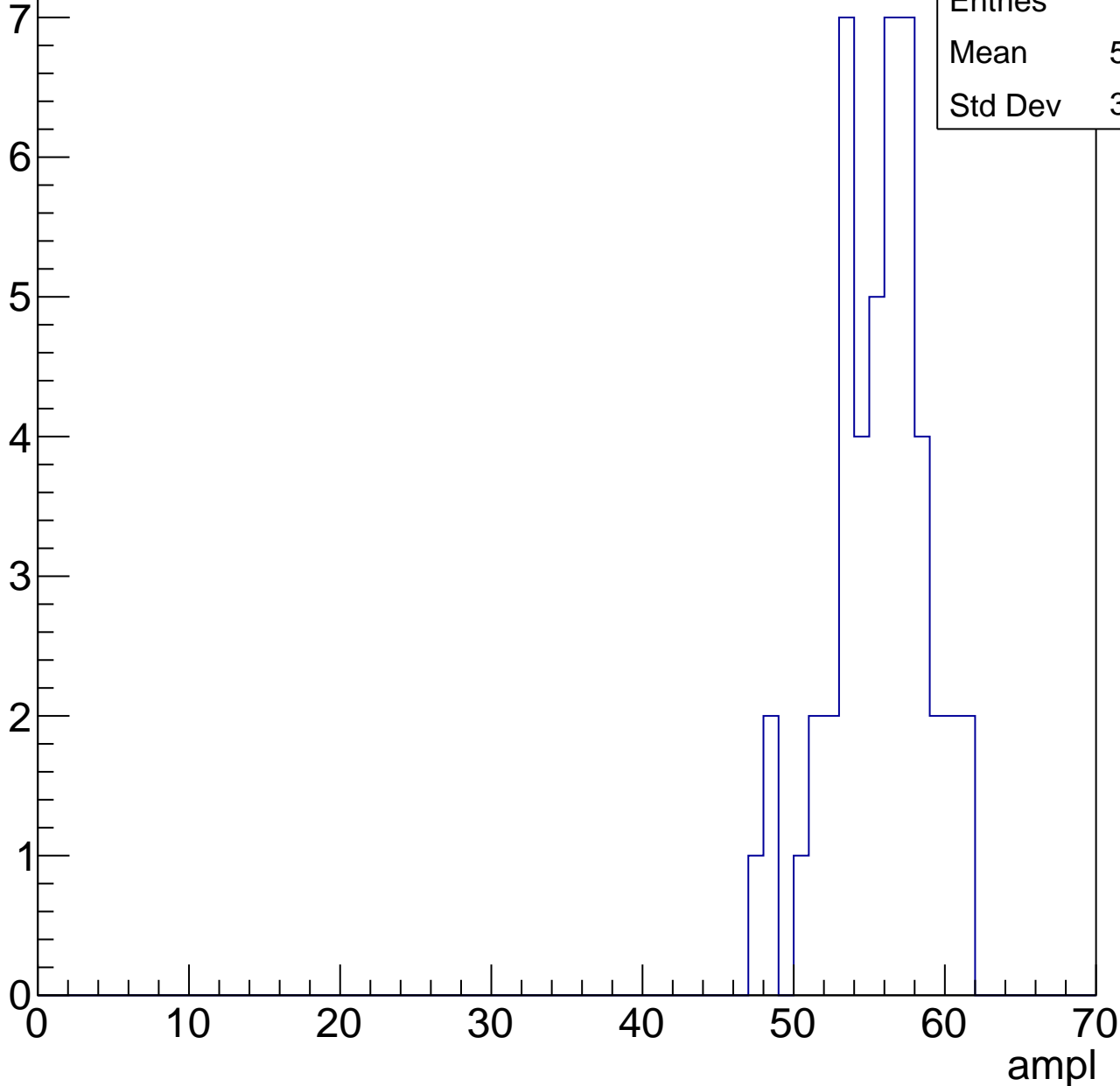


# B1L103S, U3-ch123, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	48
Mean	55.08
Std Dev	3.207

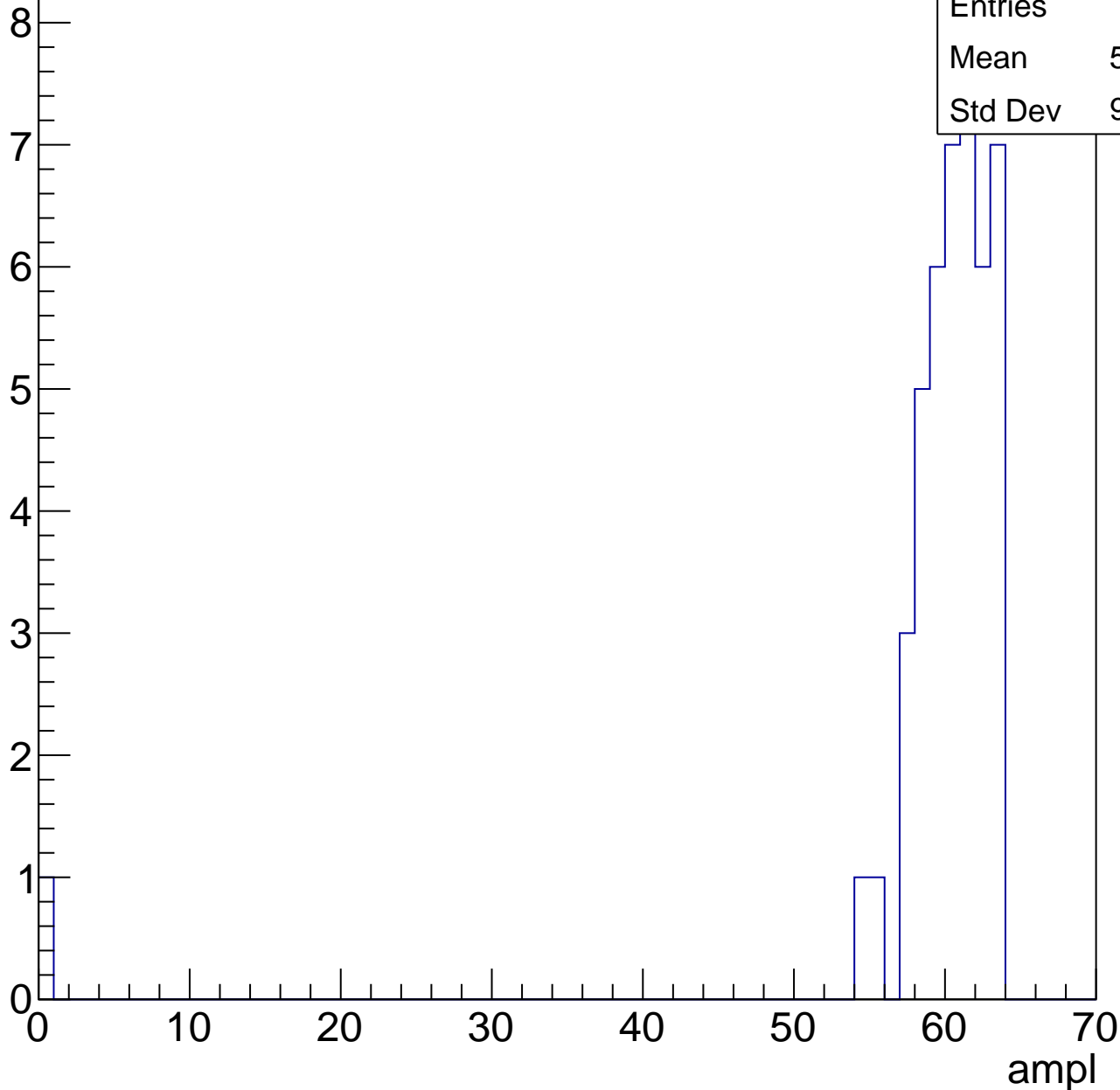


# B1L103S, U3-ch123, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

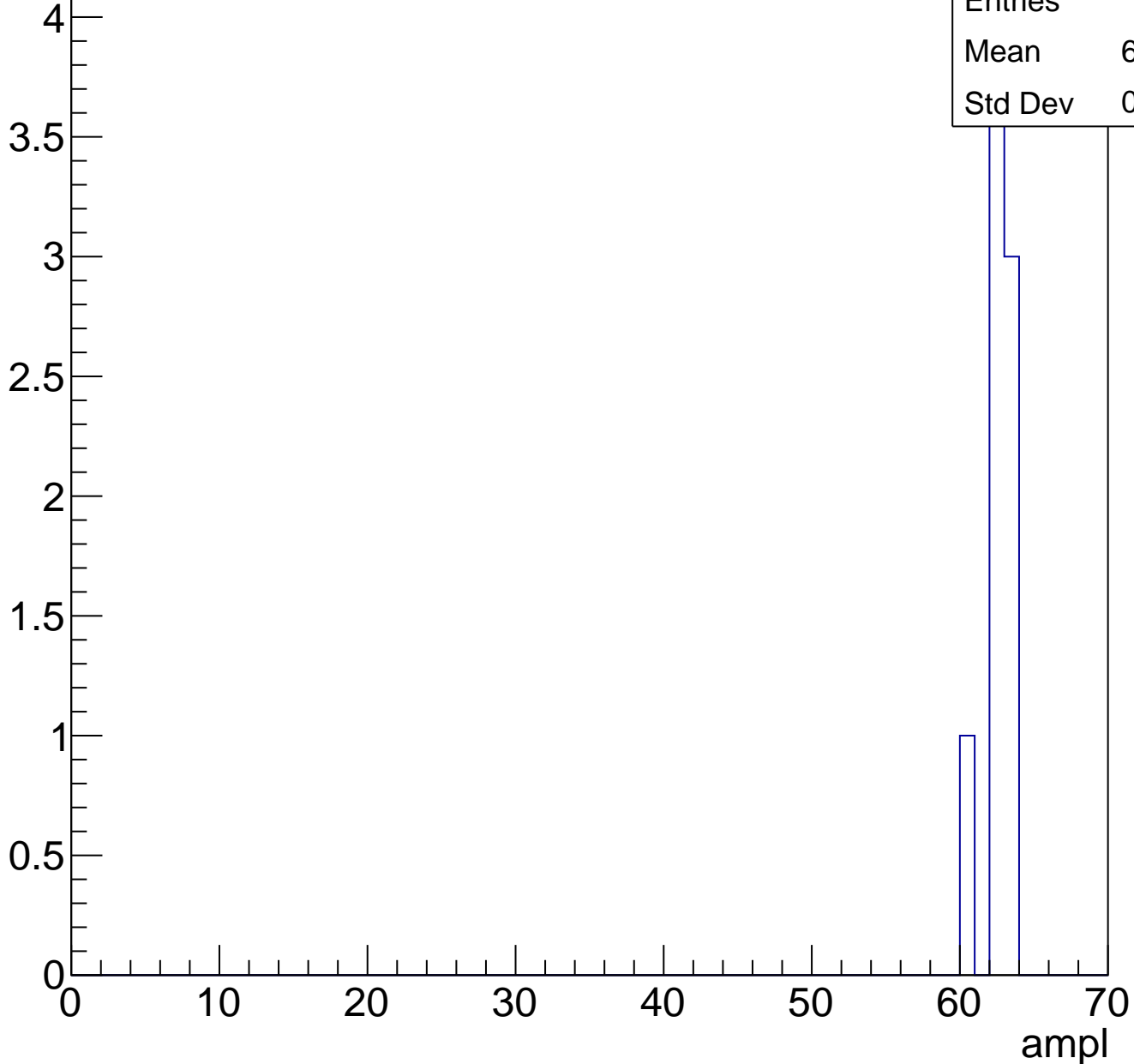
Entries	45
Mean	58.78
Std Dev	9.119



# B1L103S, U3-ch123, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U3-ch123, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

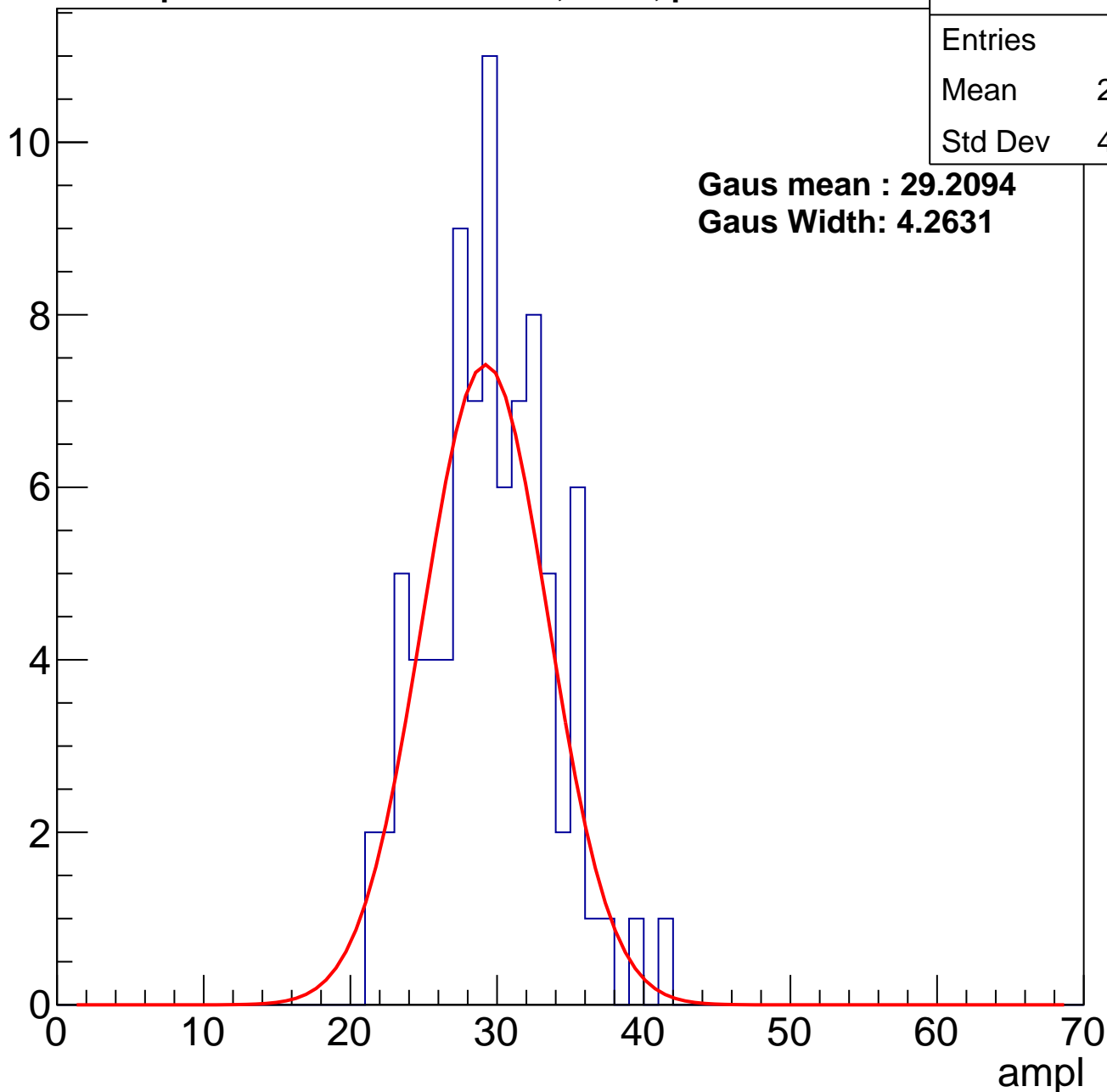
Entry



# B1L103S, U3-ch124, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch124, adc1

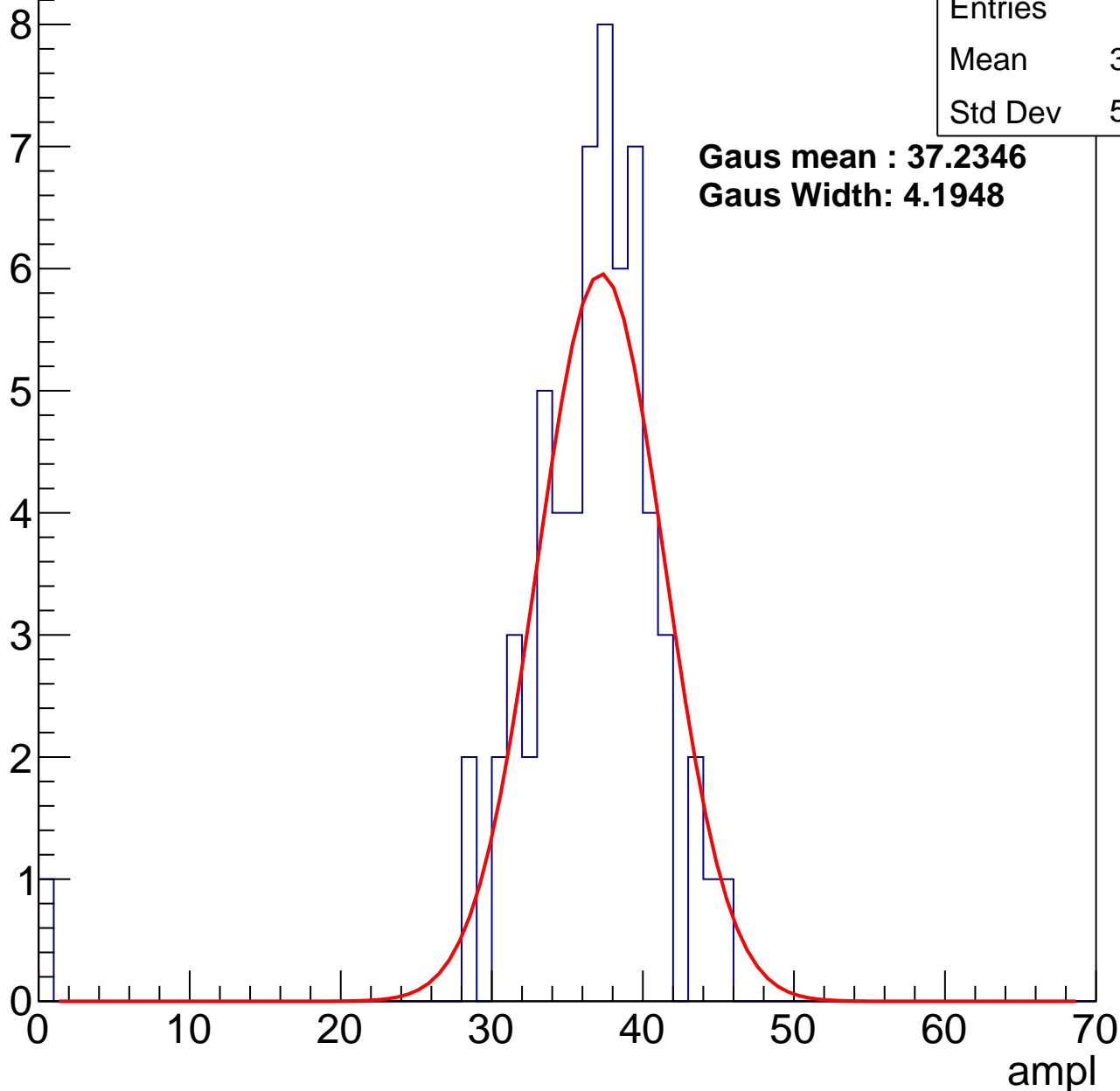
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	35.82
Std Dev	5.879

**Gaus mean : 37.2346**

**Gaus Width: 4.1948**



# B1L103S, U3-ch124, adc2

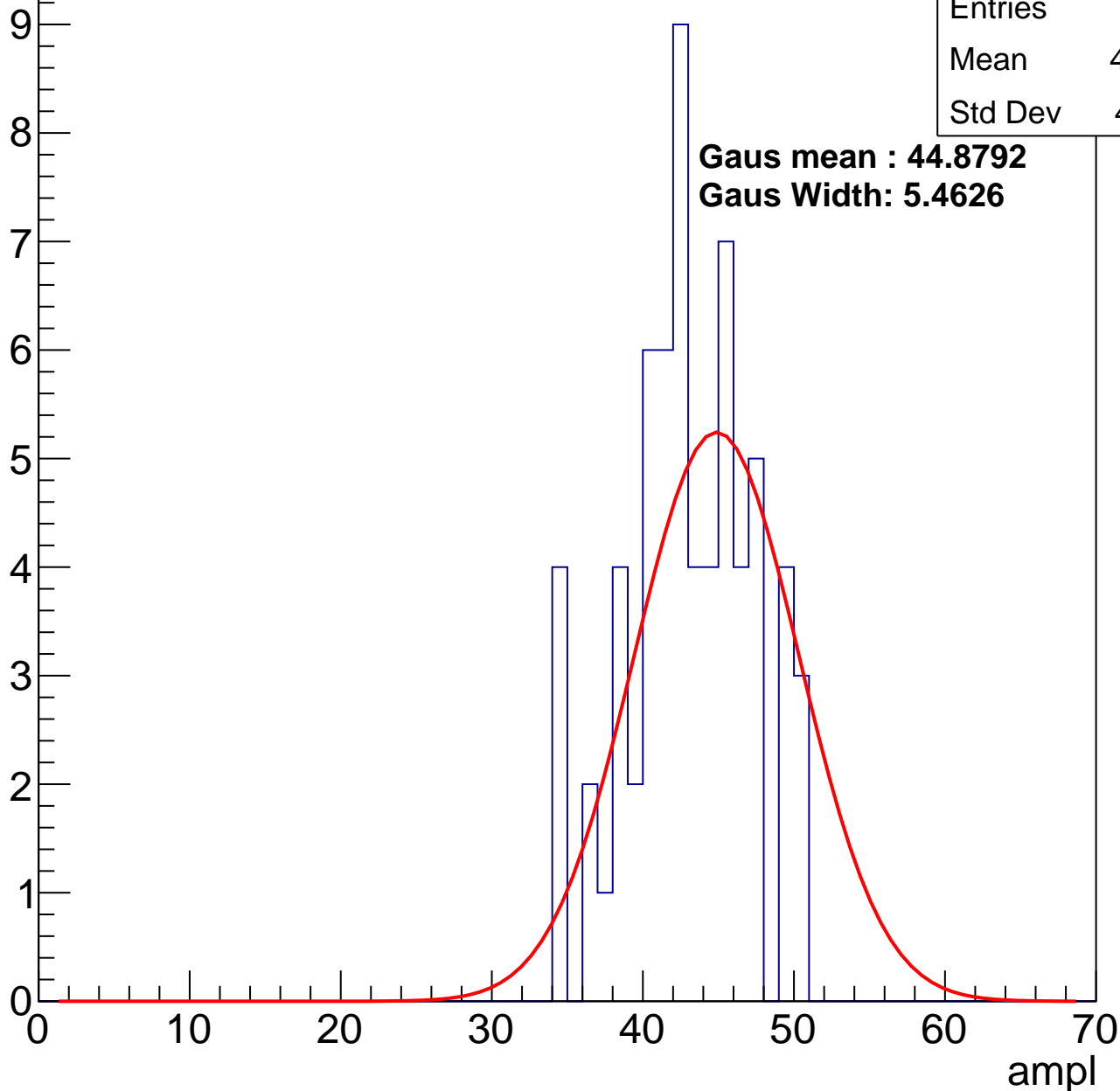
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	42.57
Std Dev	4.121

**Gaus mean : 44.8792**

**Gaus Width: 5.4626**

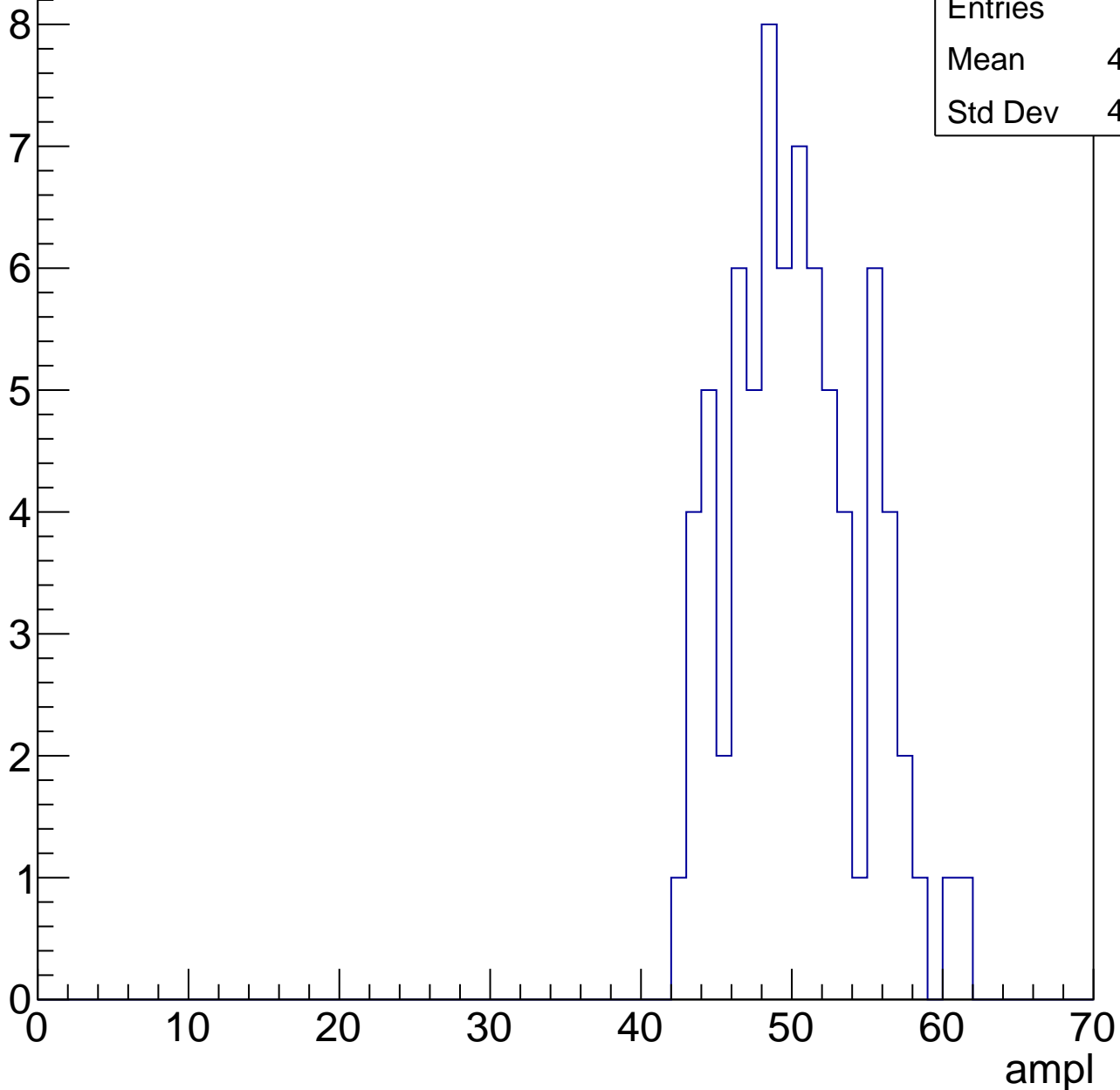


# B1L103S, U3-ch124, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	49.89
Std Dev	4.356

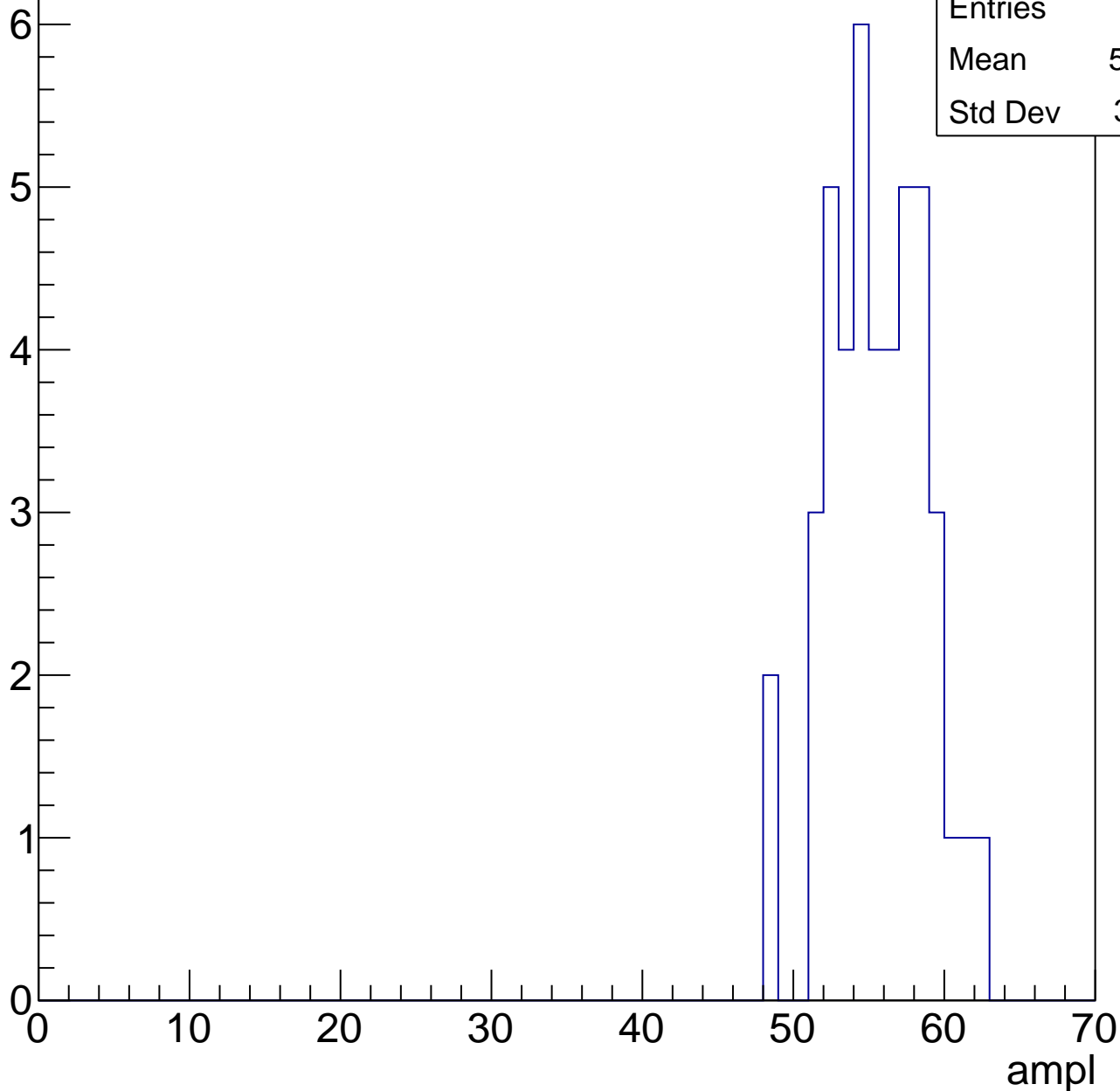


# B1L103S, U3-ch124, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	44
Mean	55.09
Std Dev	3.161

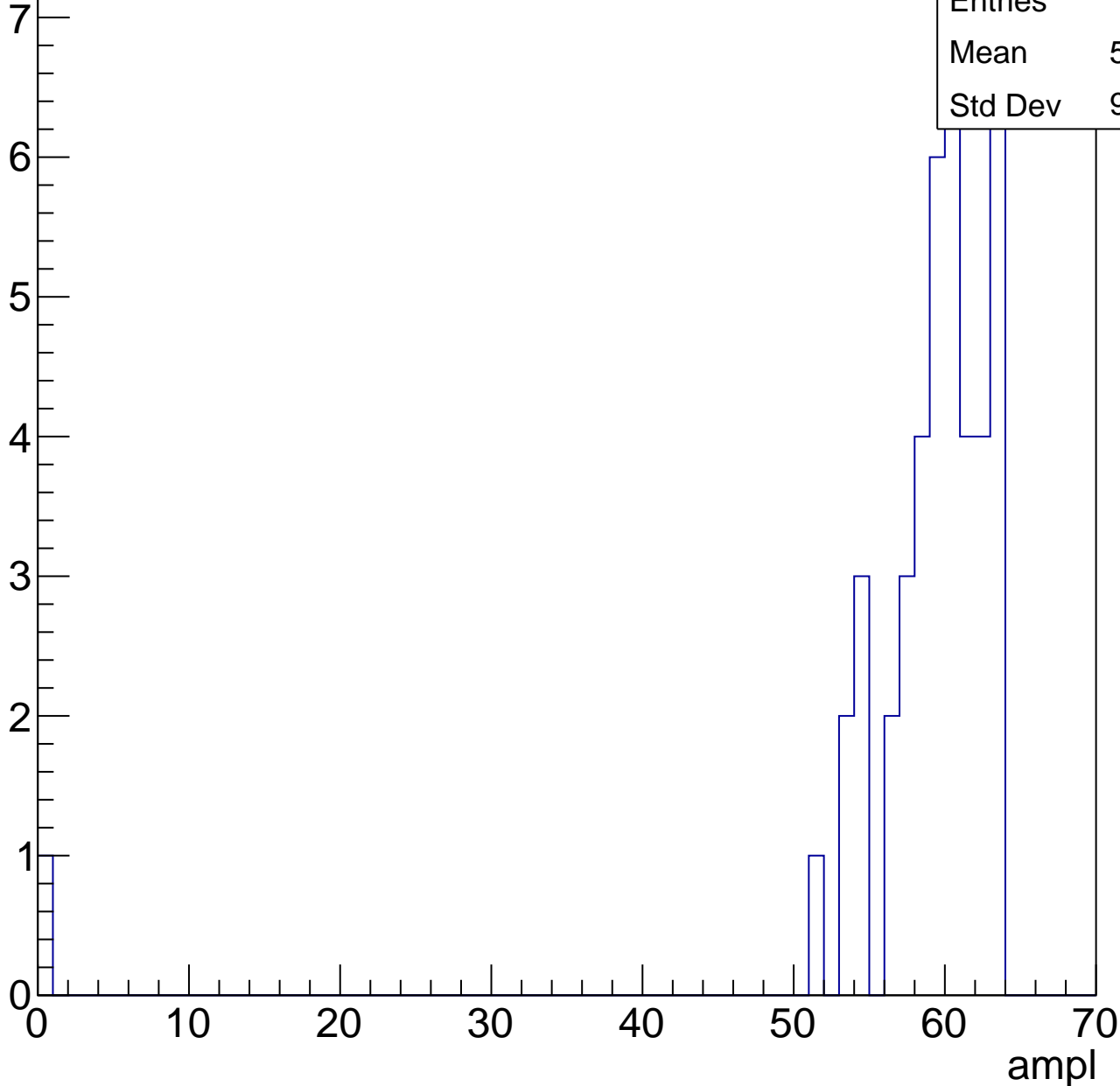


# B1L103S, U3-ch124, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

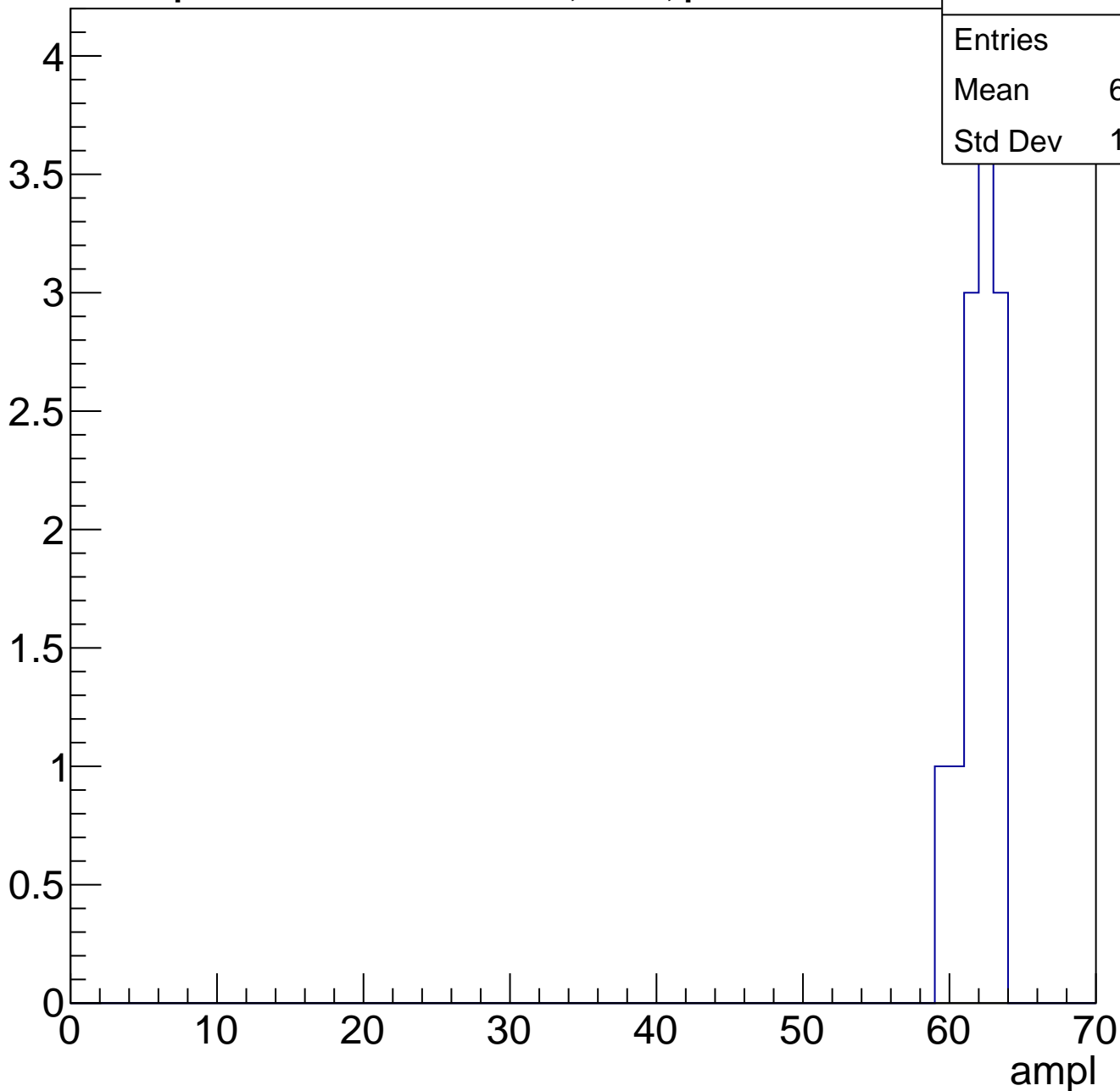
Entries	44
Mean	57.75
Std Dev	9.328



# B1L103S, U3-ch124, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

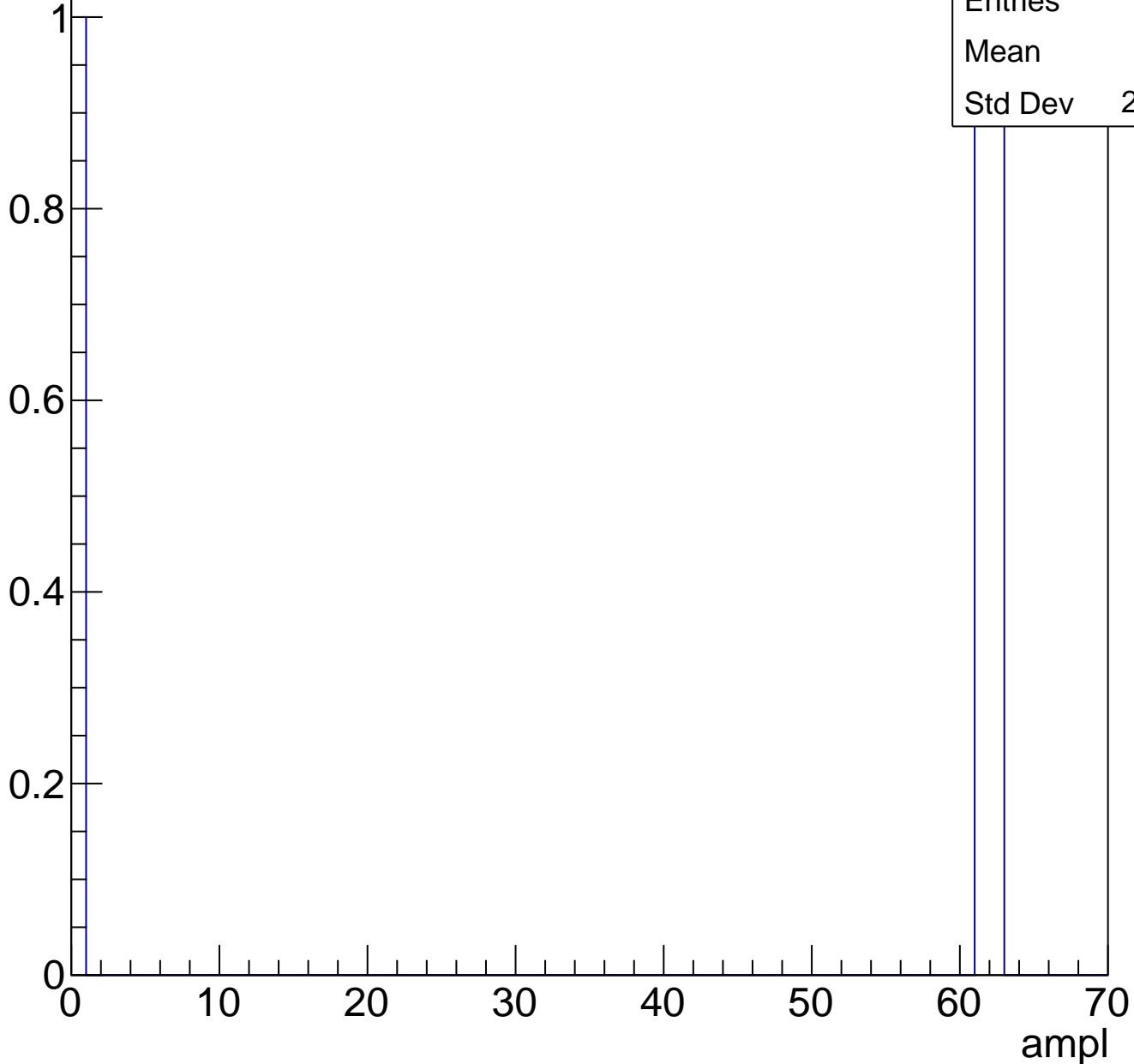




# B1L103S, U3-ch124, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch125, adc0

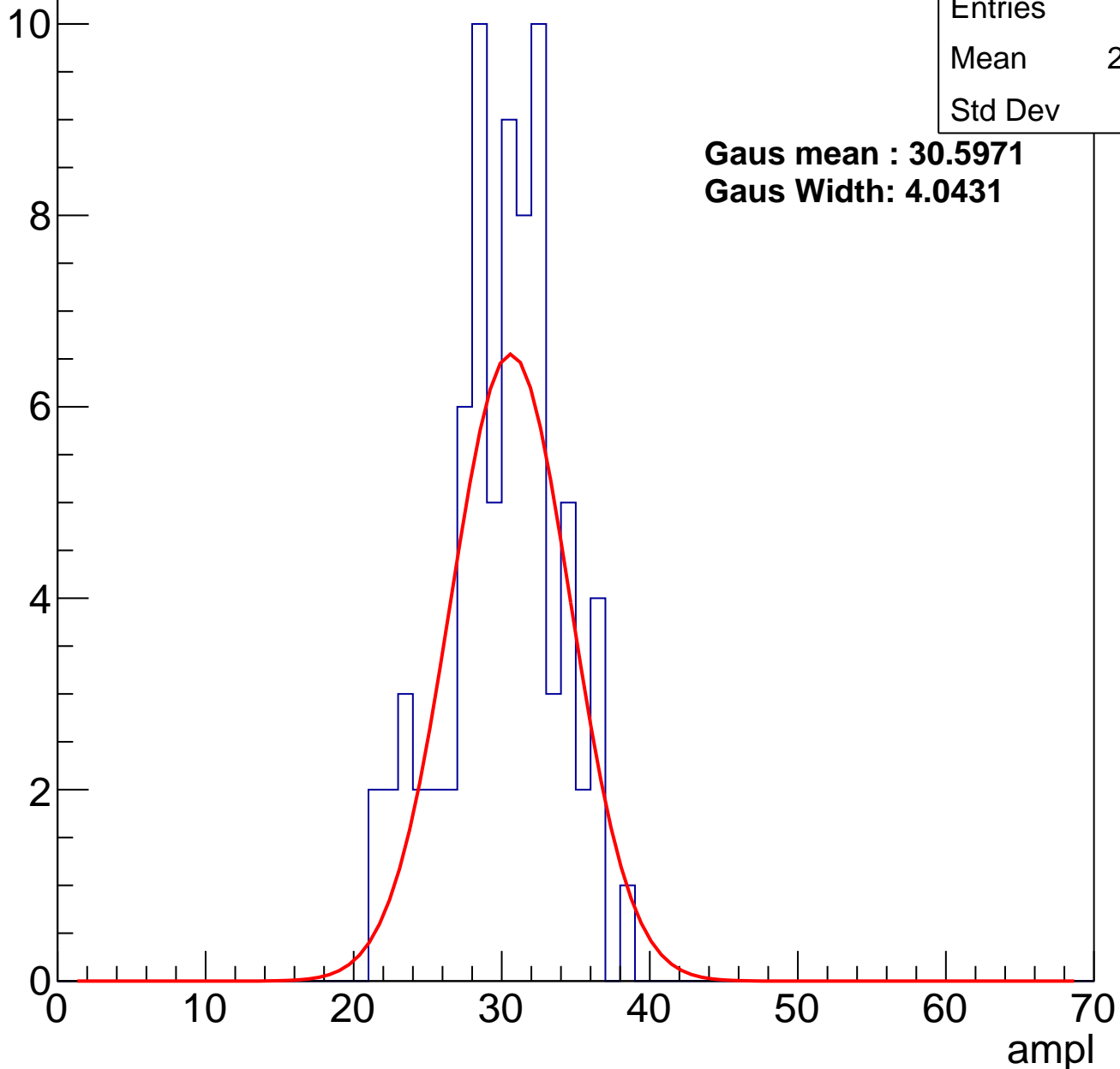
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	76
Mean	29.62
Std Dev	3.79

**Gaus mean : 30.5971**

**Gaus Width: 4.0431**

Entry



# B1L103S, U3-ch125, adc1

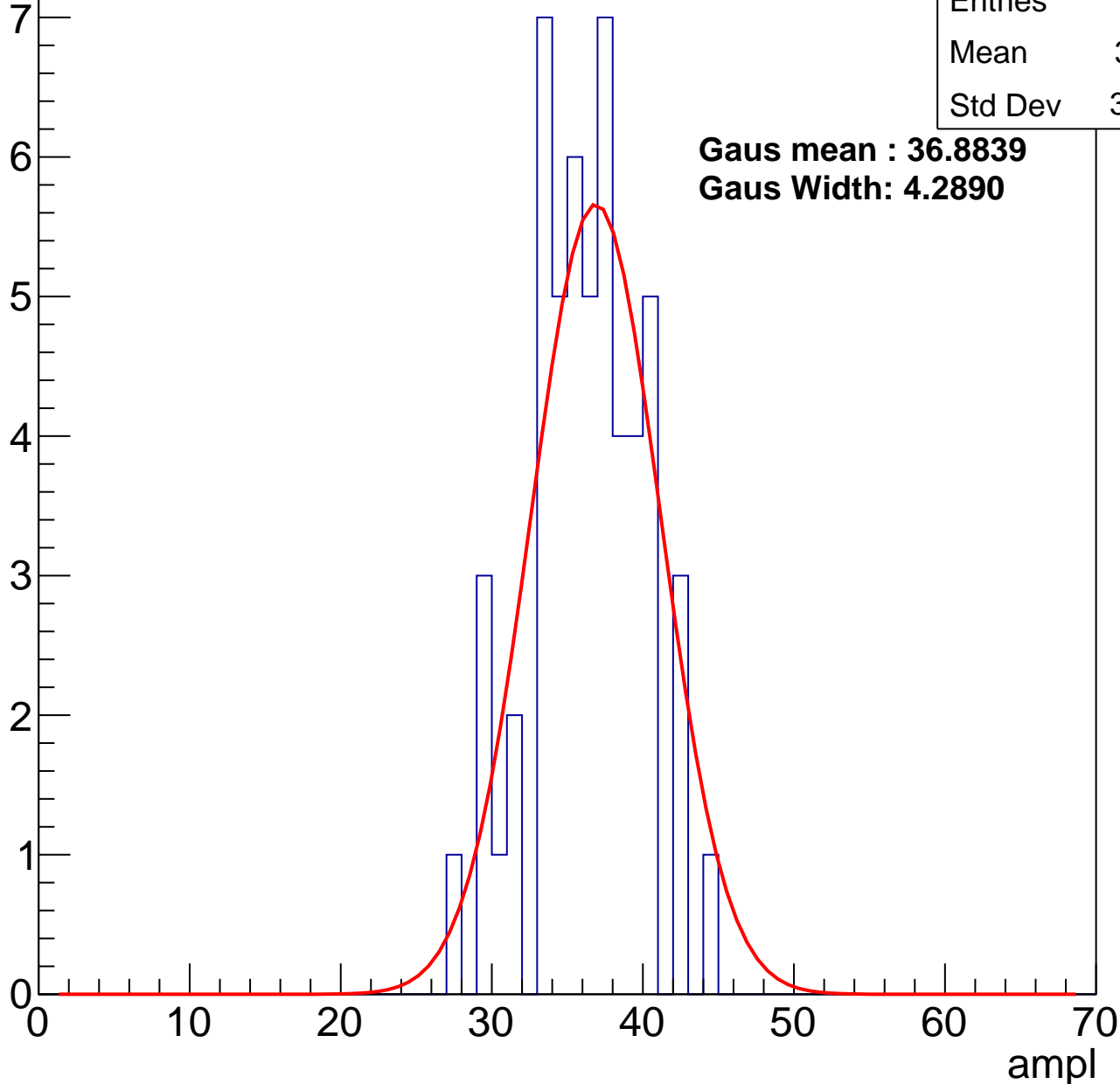
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	35.81
Std Dev	3.632

**Gaus mean : 36.8839**

**Gaus Width: 4.2890**



# B1L103S, U3-ch125, adc2

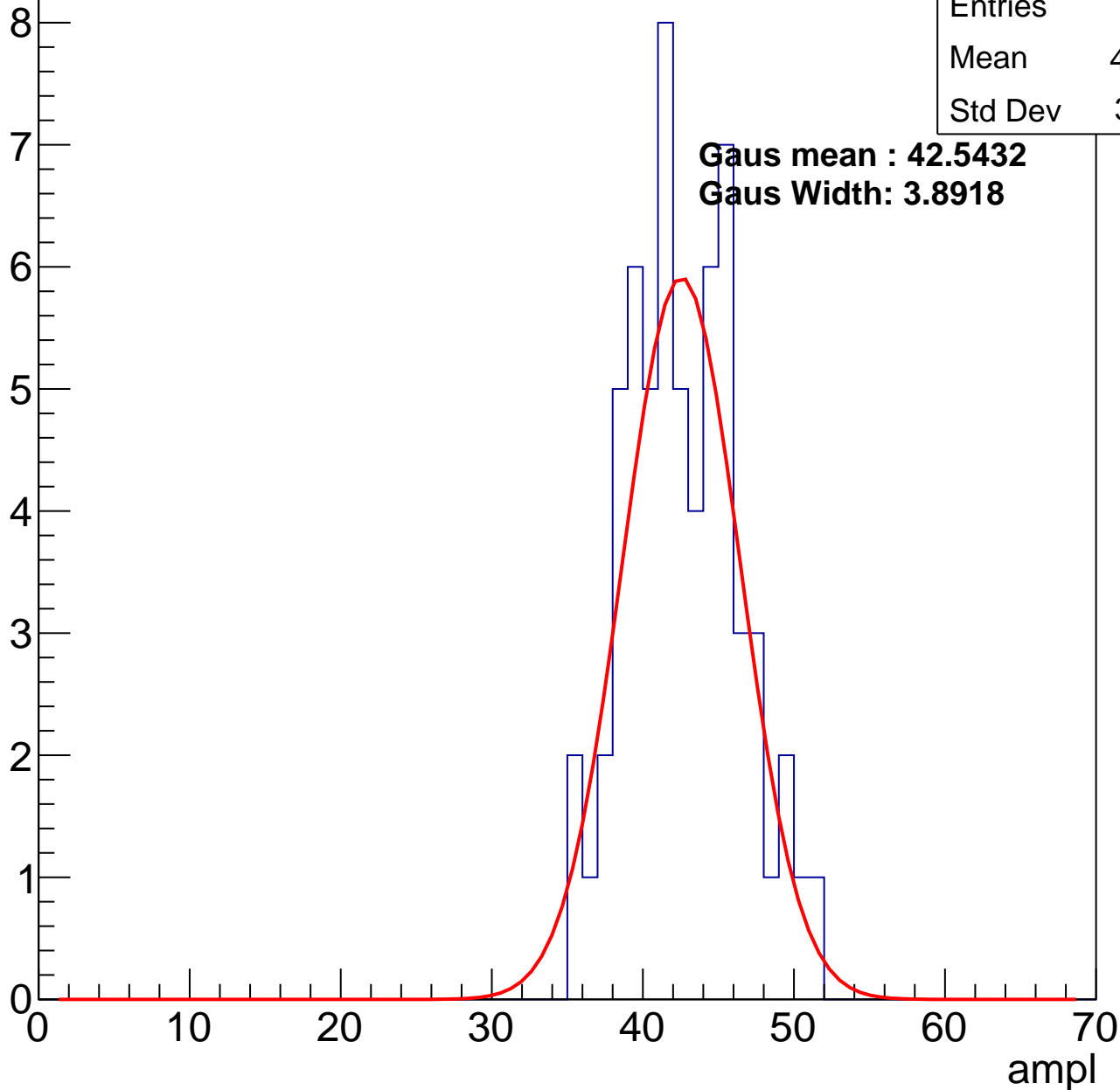
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	42.24
Std Dev	3.671

**Gaus mean : 42.5432**

**Gaus Width: 3.8918**

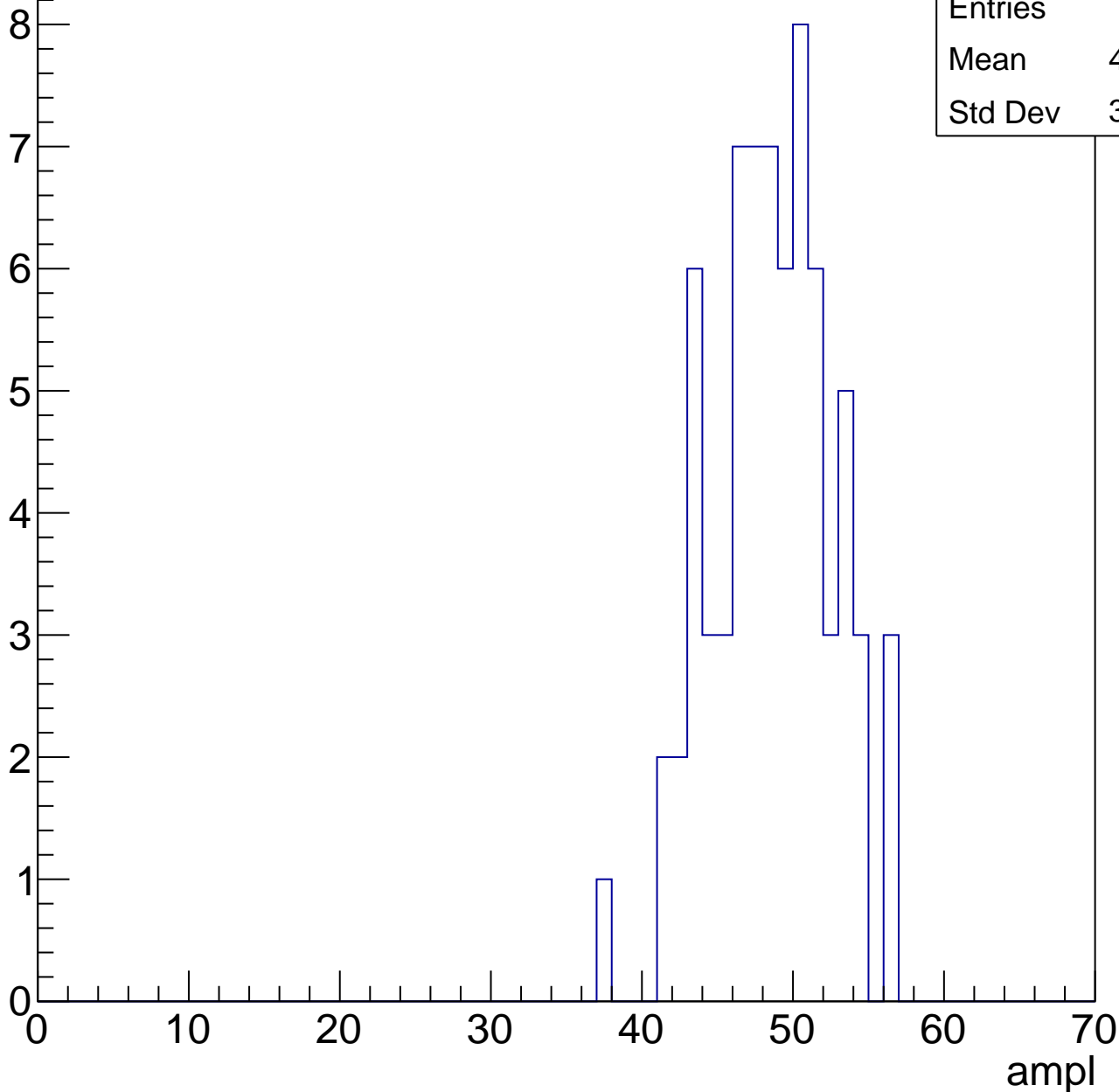


# B1L103S, U3-ch125, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	48.14
Std Dev	3.935

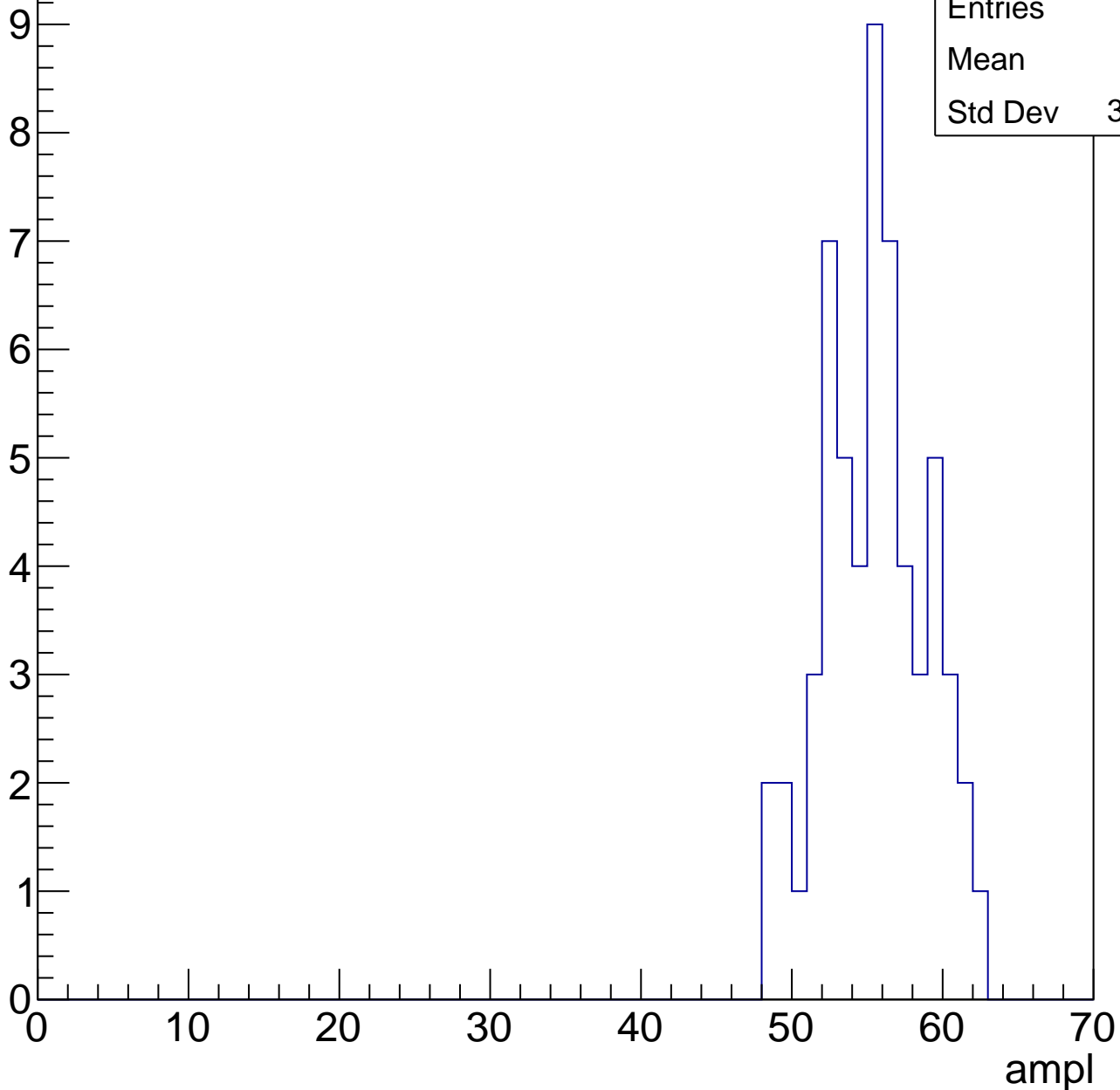


# B1L103S, U3-ch125, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	55
Std Dev	3.363

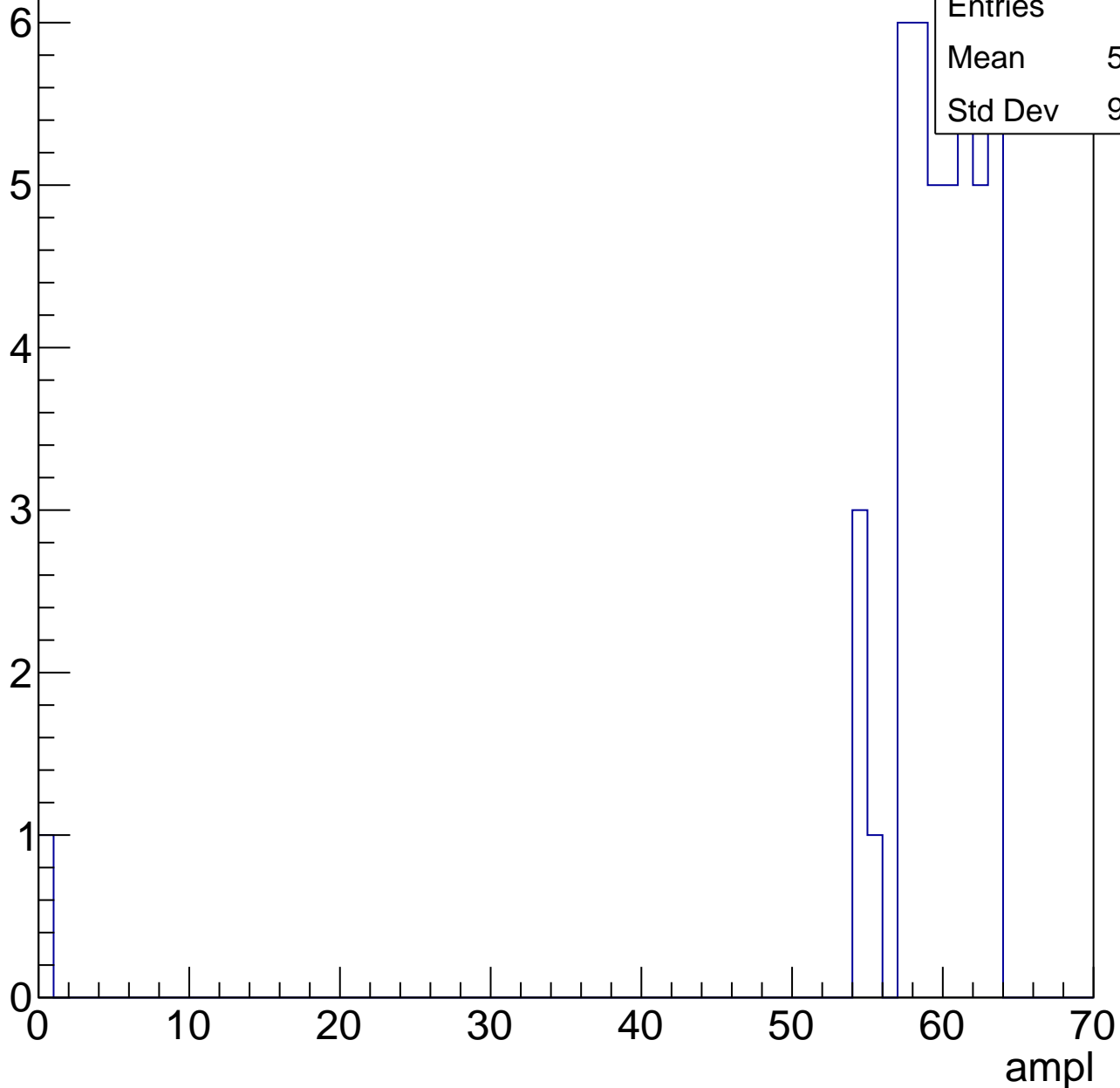


# B1L103S, U3-ch125, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

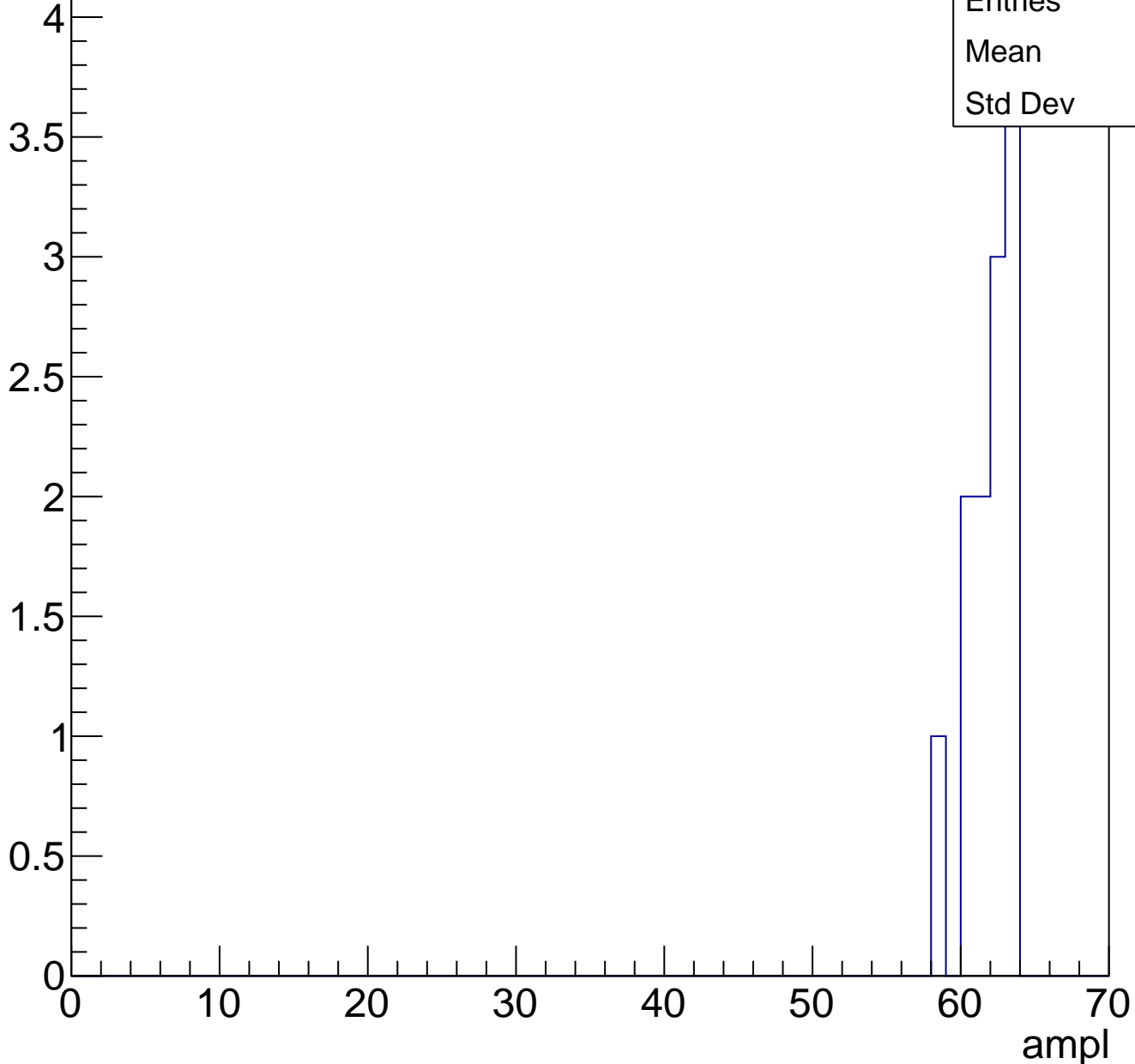
Entries	44
Mean	58.09
Std Dev	9.214



# B1L103S, U3-ch125, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

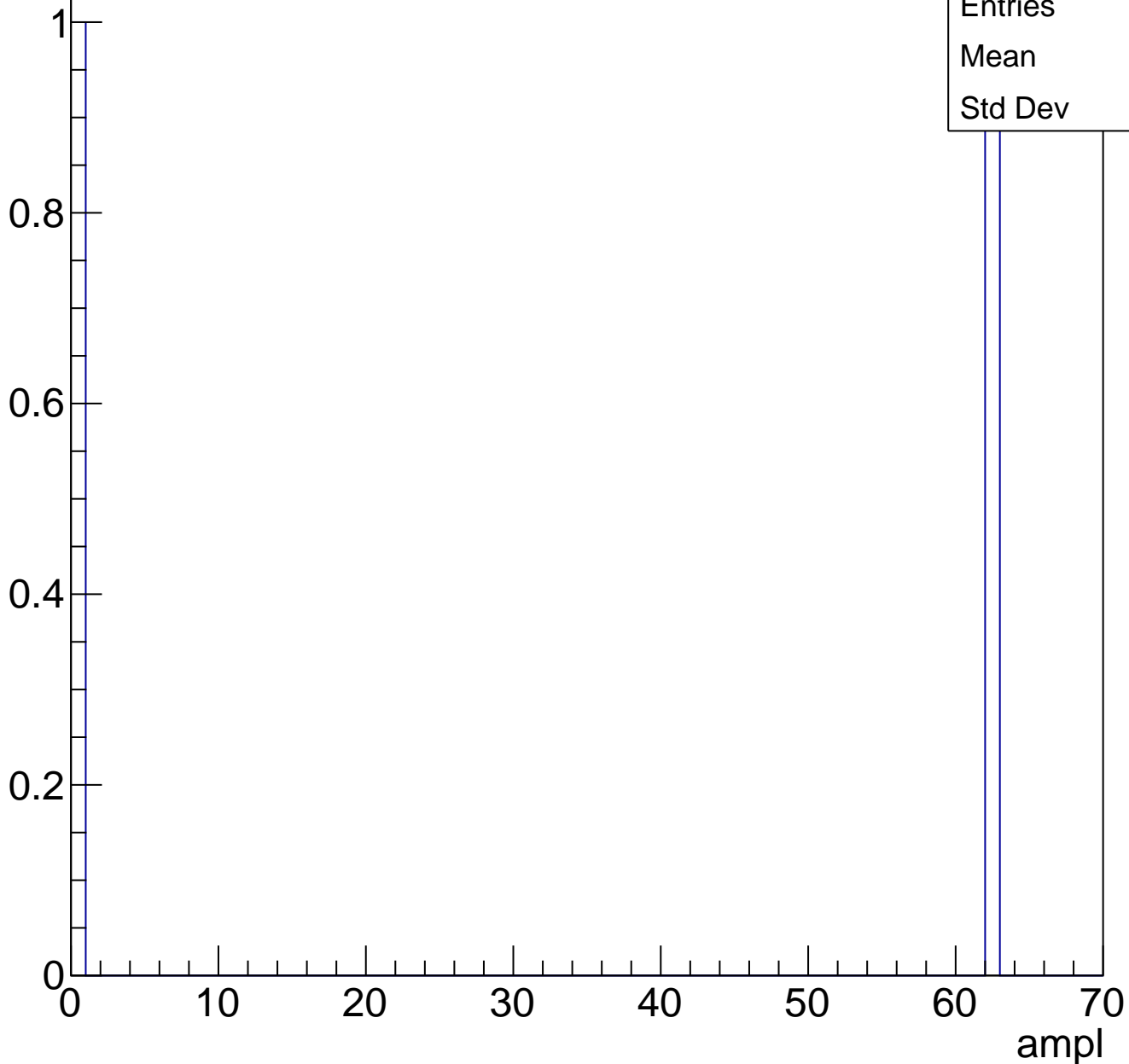




# B1L103S, U3-ch125, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch126, adc0

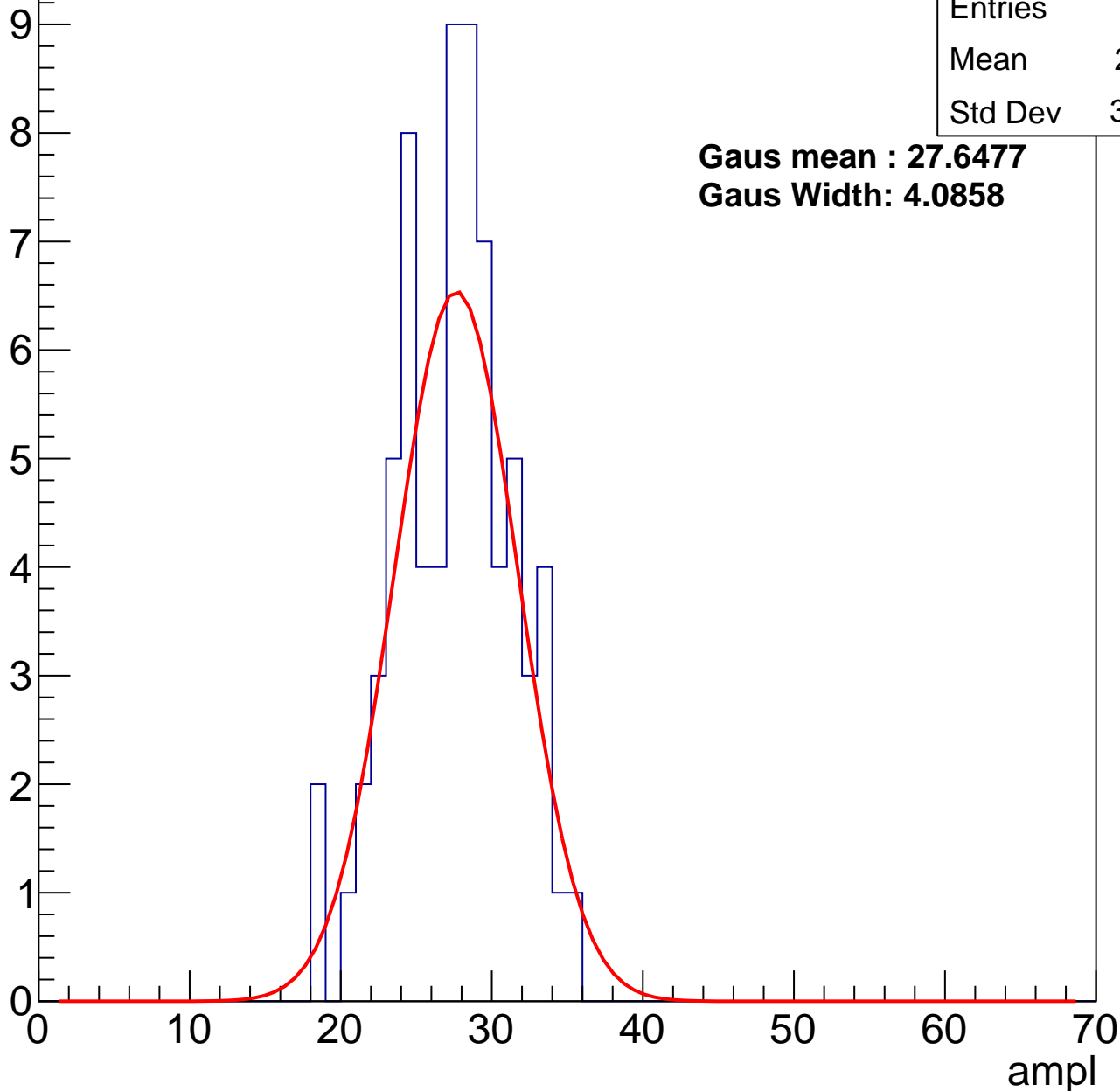
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	27.01
Std Dev	3.755

**Gaus mean : 27.6477**

**Gaus Width: 4.0858**



# B1L103S, U3-ch126, adc1

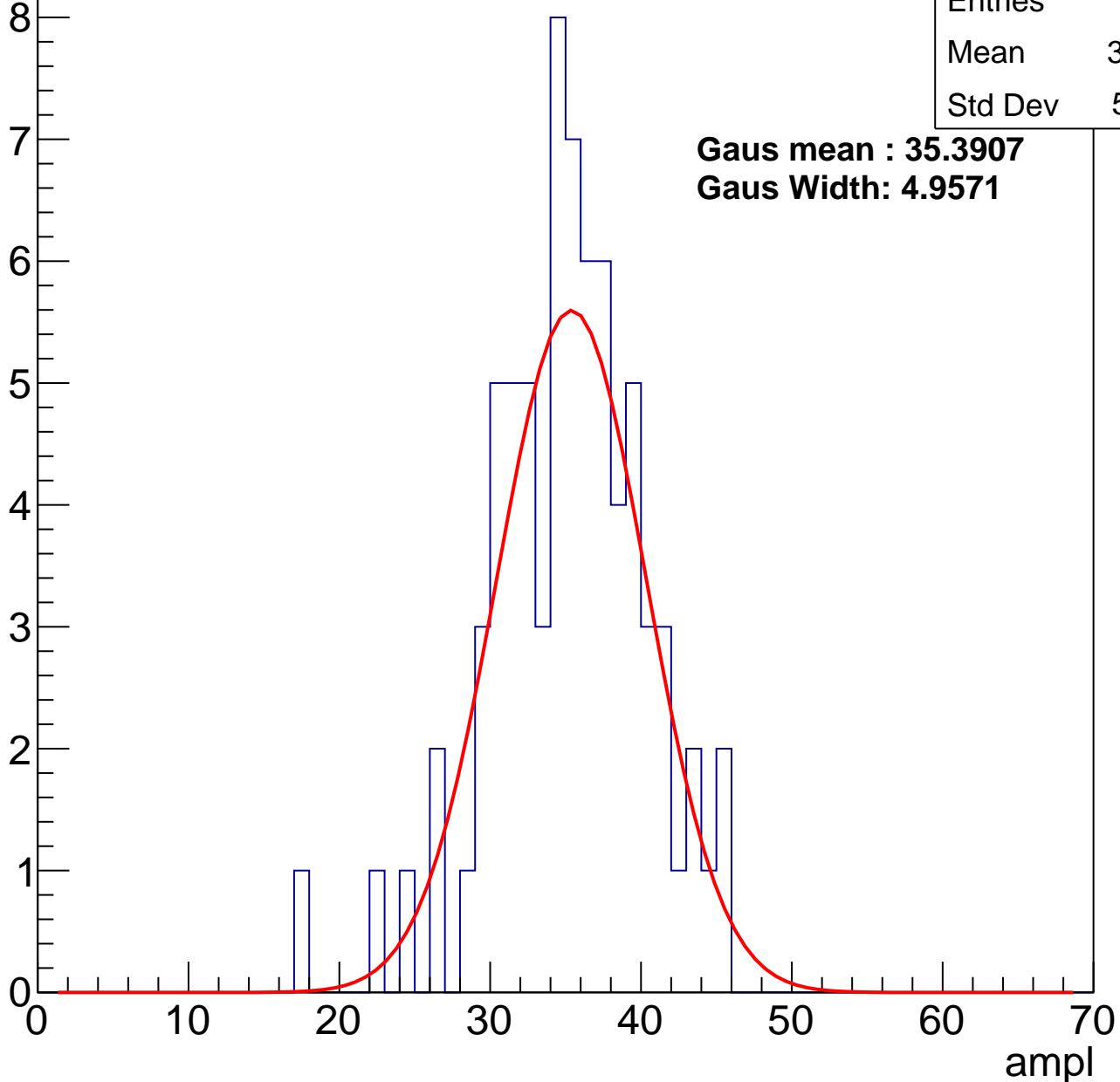
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	34.68
Std Dev	5.141

**Gaus mean : 35.3907**

**Gaus Width: 4.9571**



# B1L103S, U3-ch126, adc2

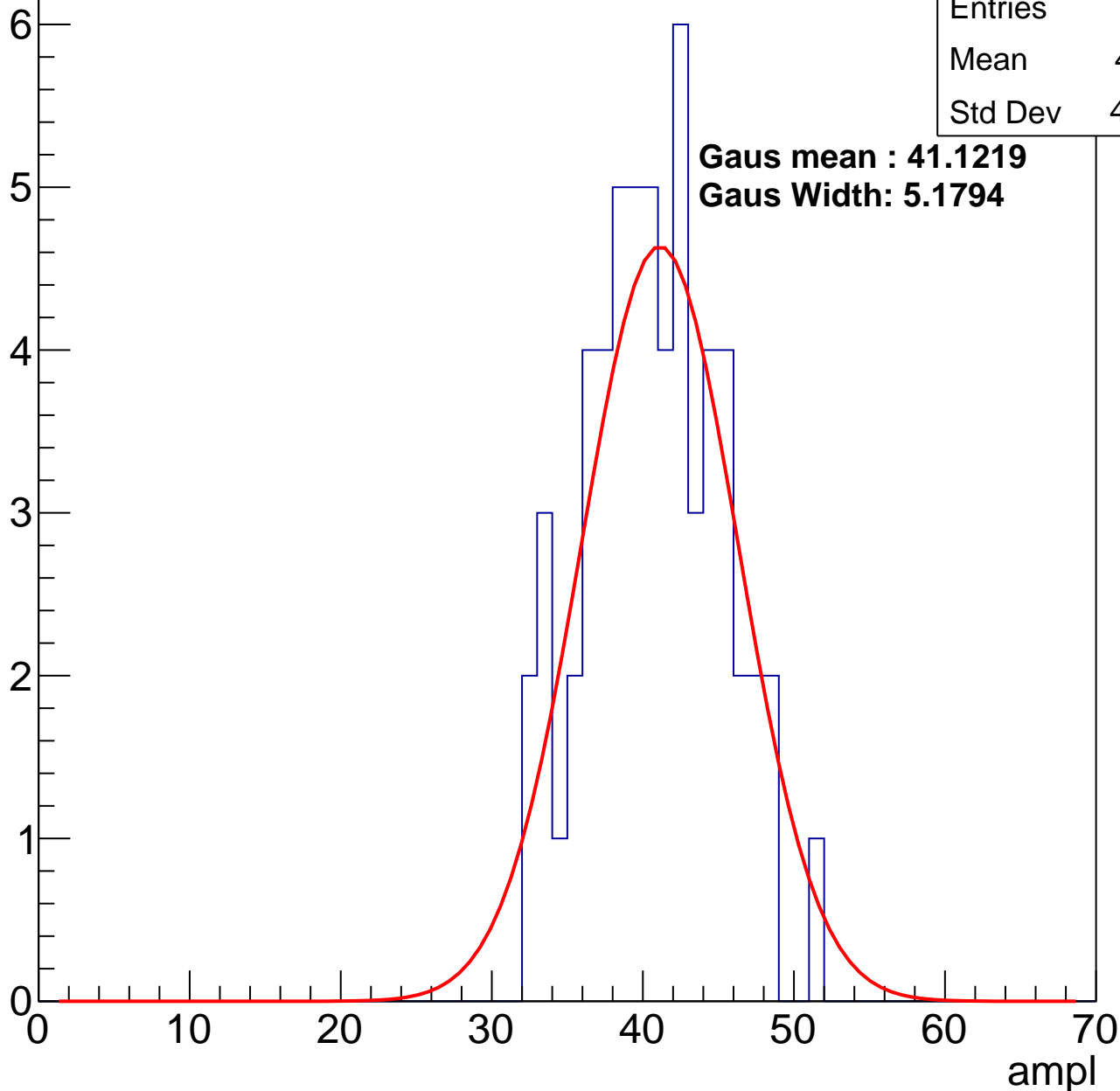
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	40.31
Std Dev	4.354

**Gaus mean : 41.1219**

**Gaus Width: 5.1794**

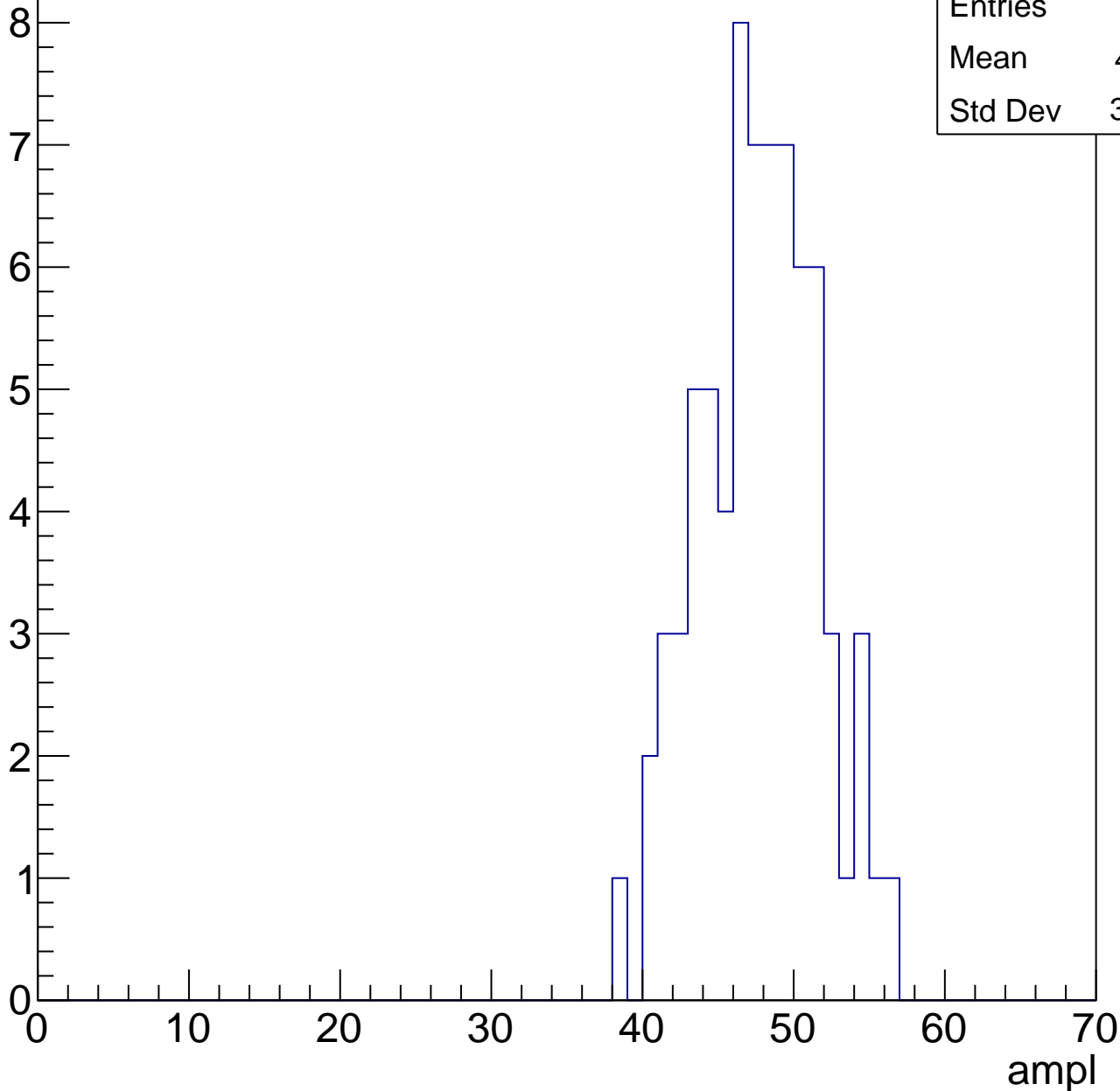


# B1L103S, U3-ch126, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

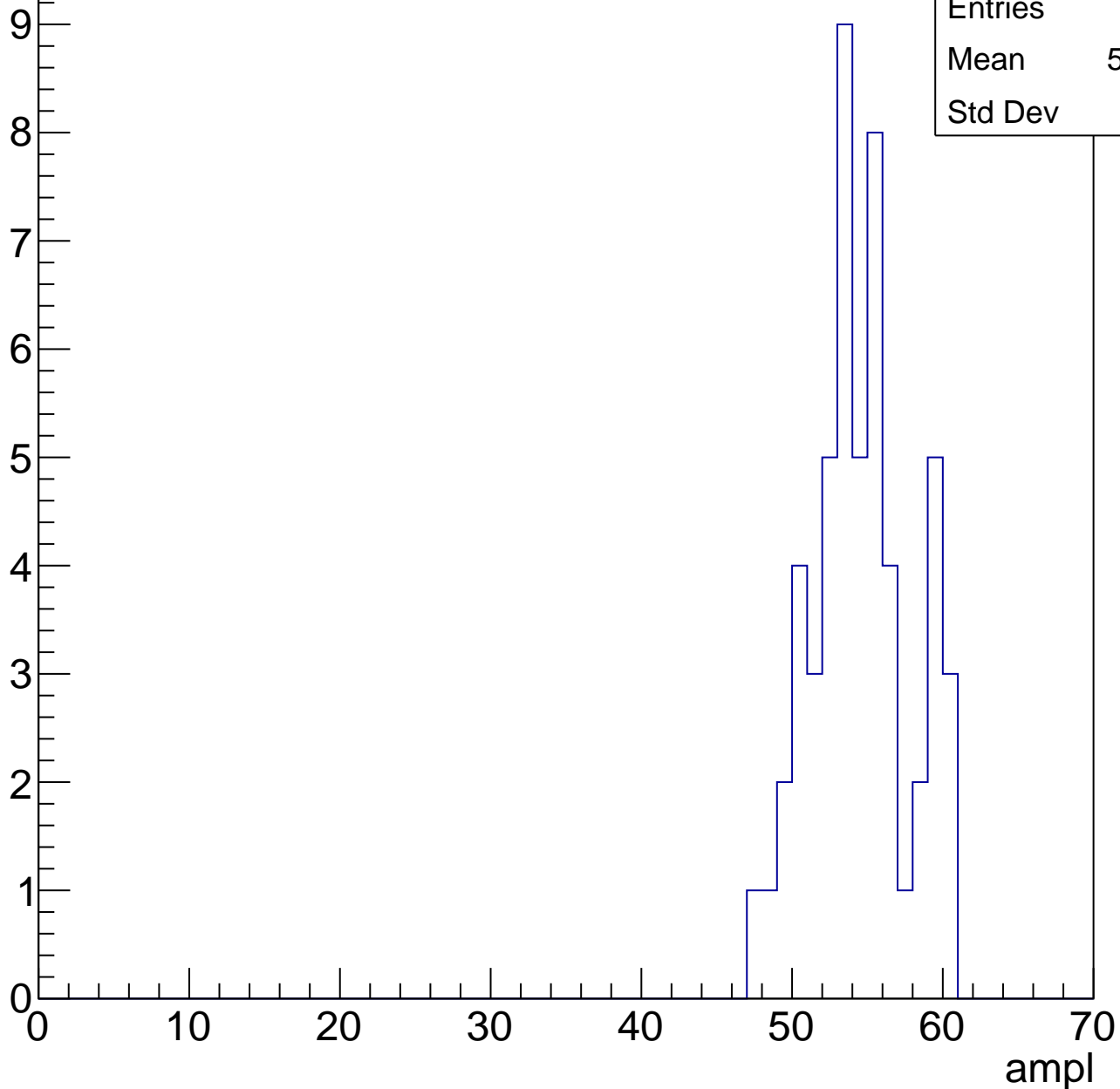
Entries	73
Mean	47.21
Std Dev	3.875



# B1L103S, U3-ch126, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



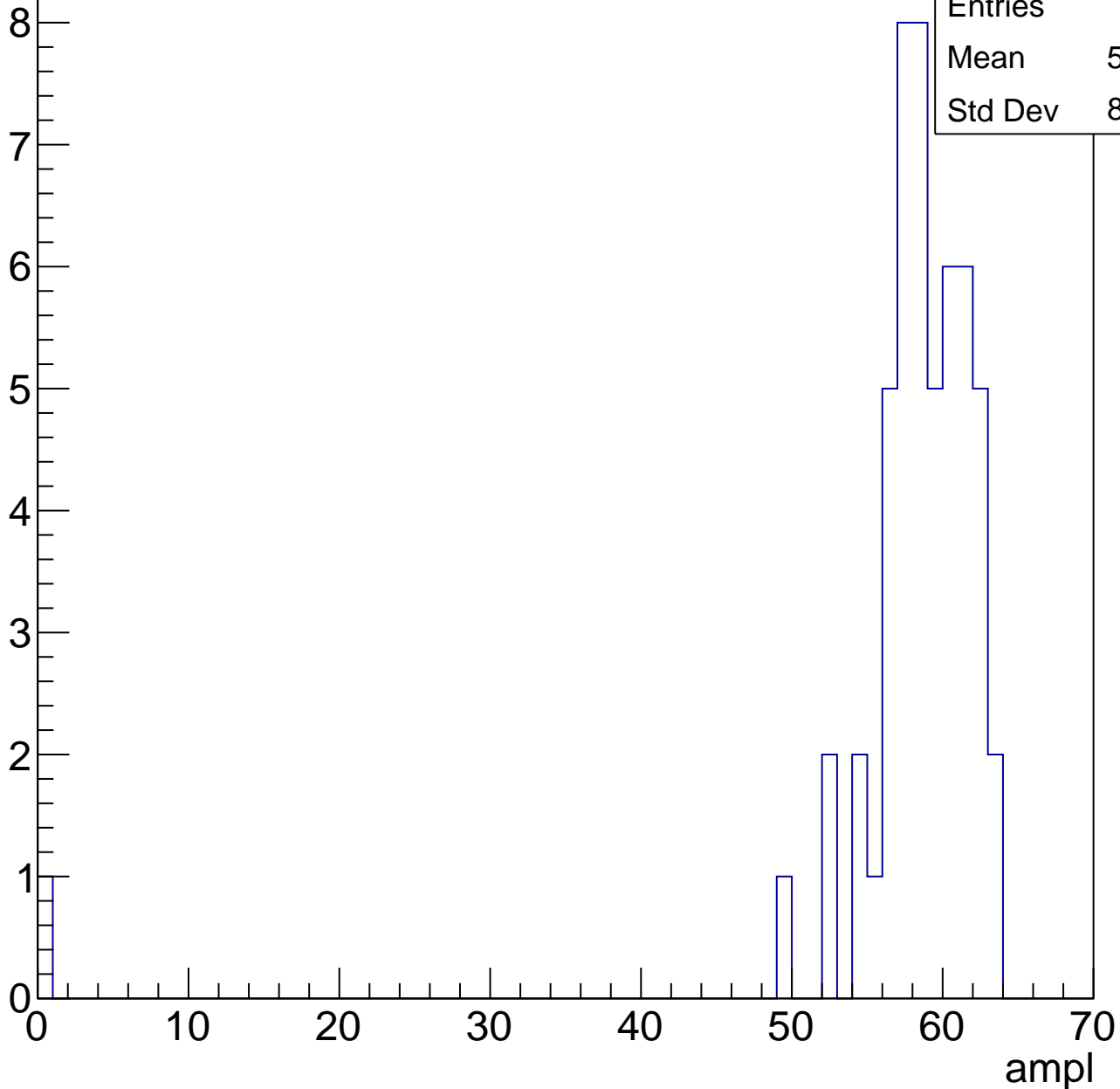
Entries	53
Mean	54.06
Std Dev	3.23

# B1L103S, U3-ch126, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	57.17
Std Dev	8.507

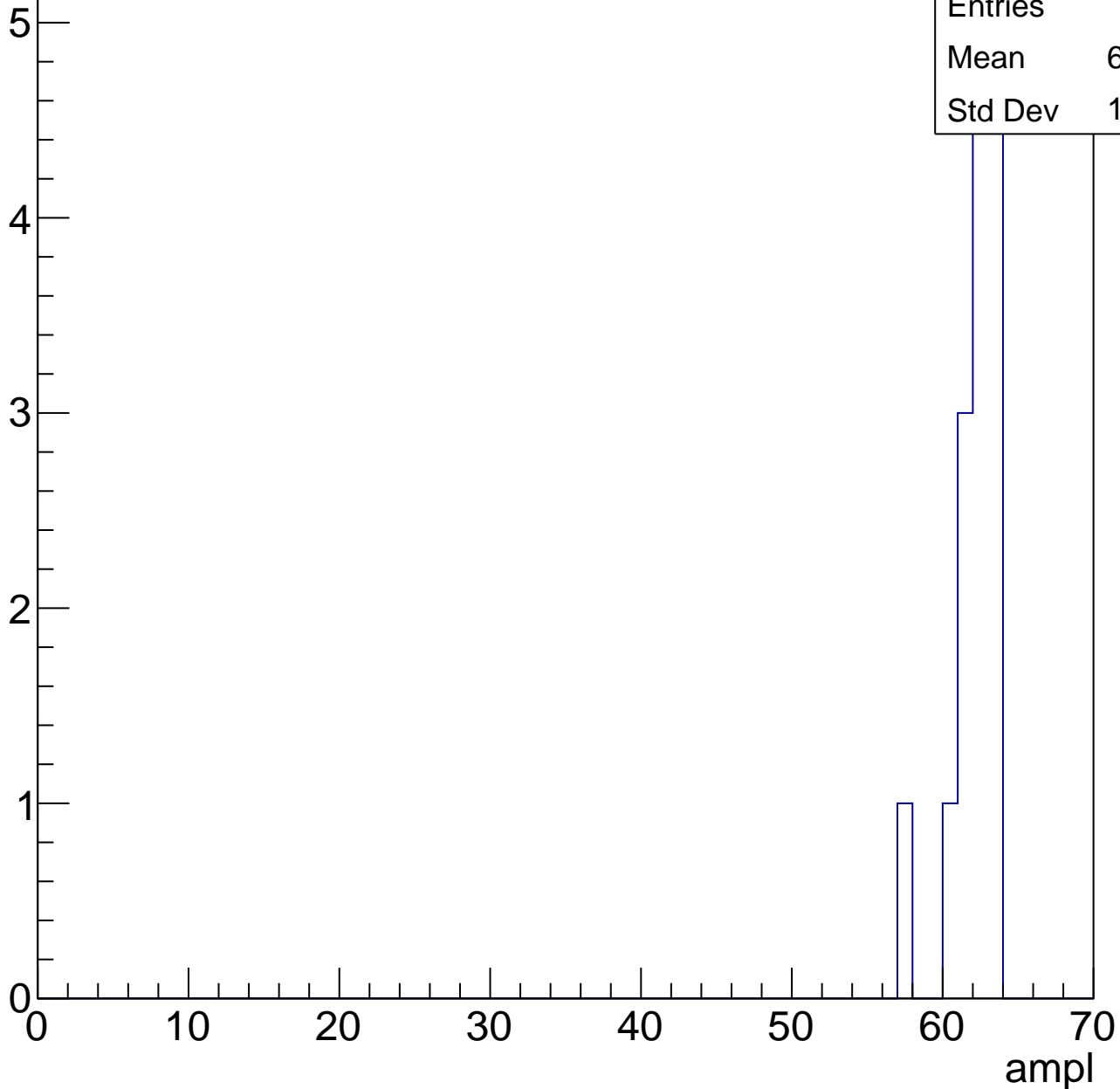


# B1L103S, U3-ch126, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	15
Mean	61.67
Std Dev	1.535

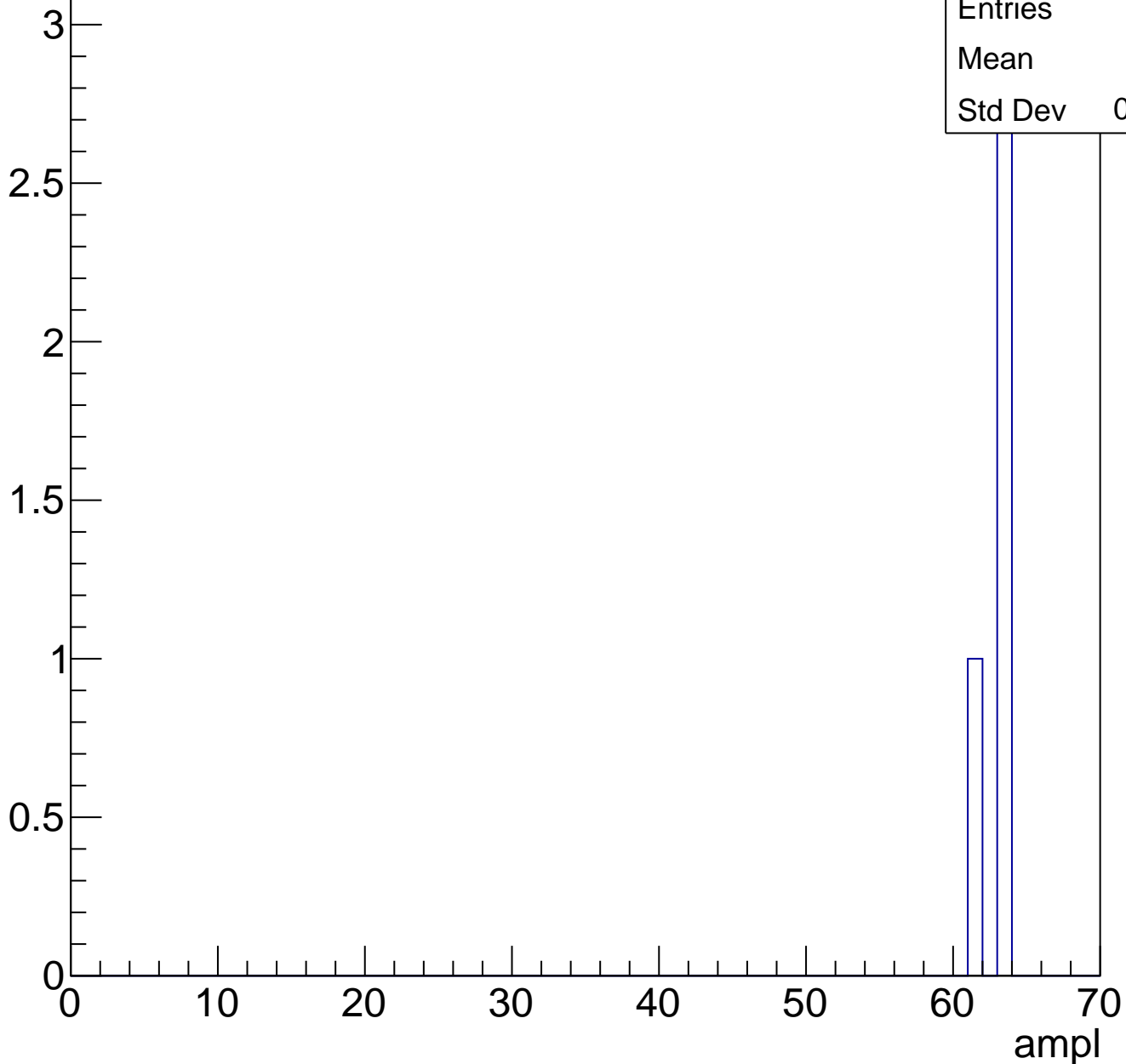




# B1L103S, U3-ch126, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U3-ch127, adc0

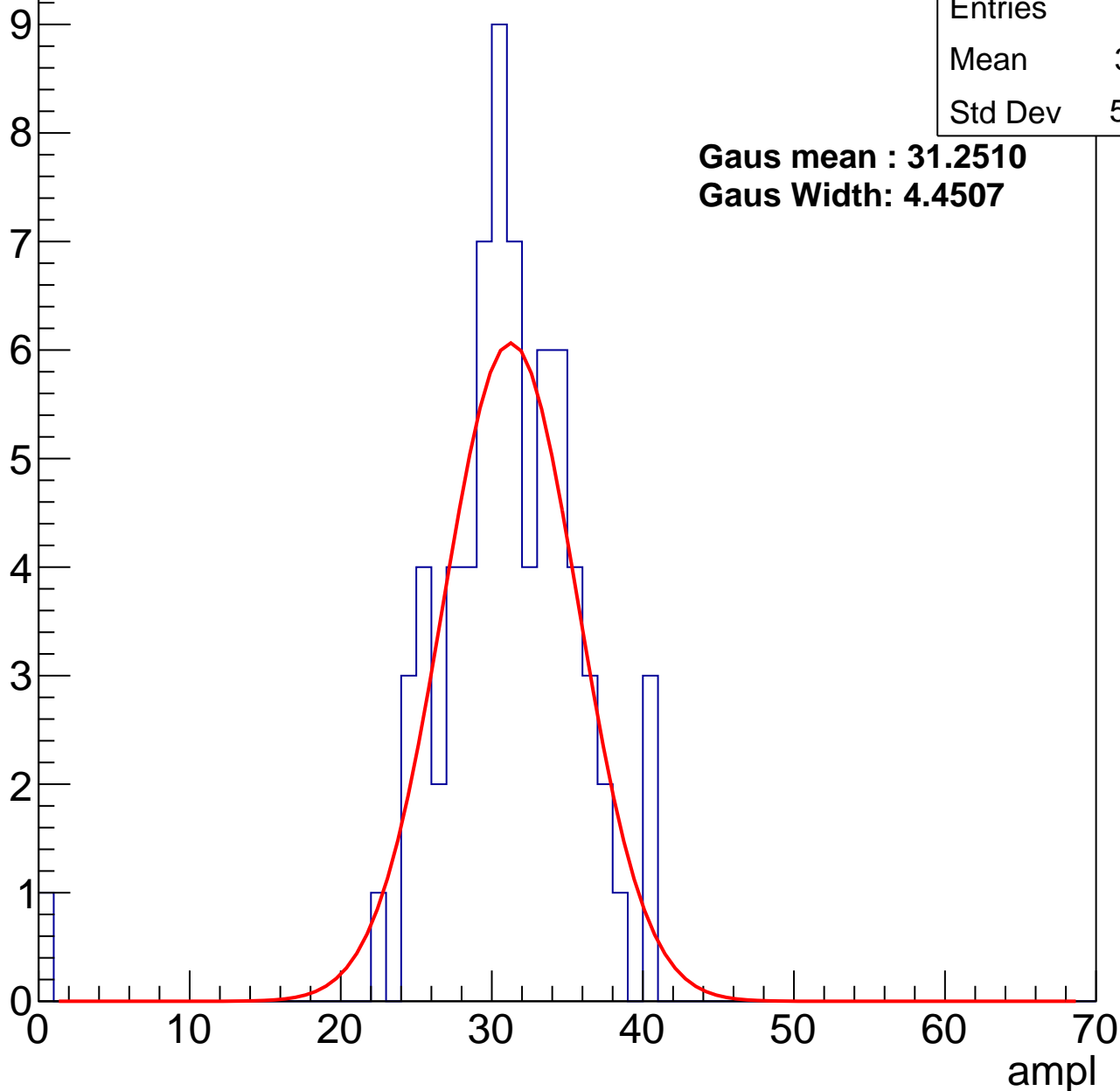
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	30.51
Std Dev	5.423

**Gaus mean : 31.2510**

**Gaus Width: 4.4507**



# B1L103S, U3-ch127, adc1

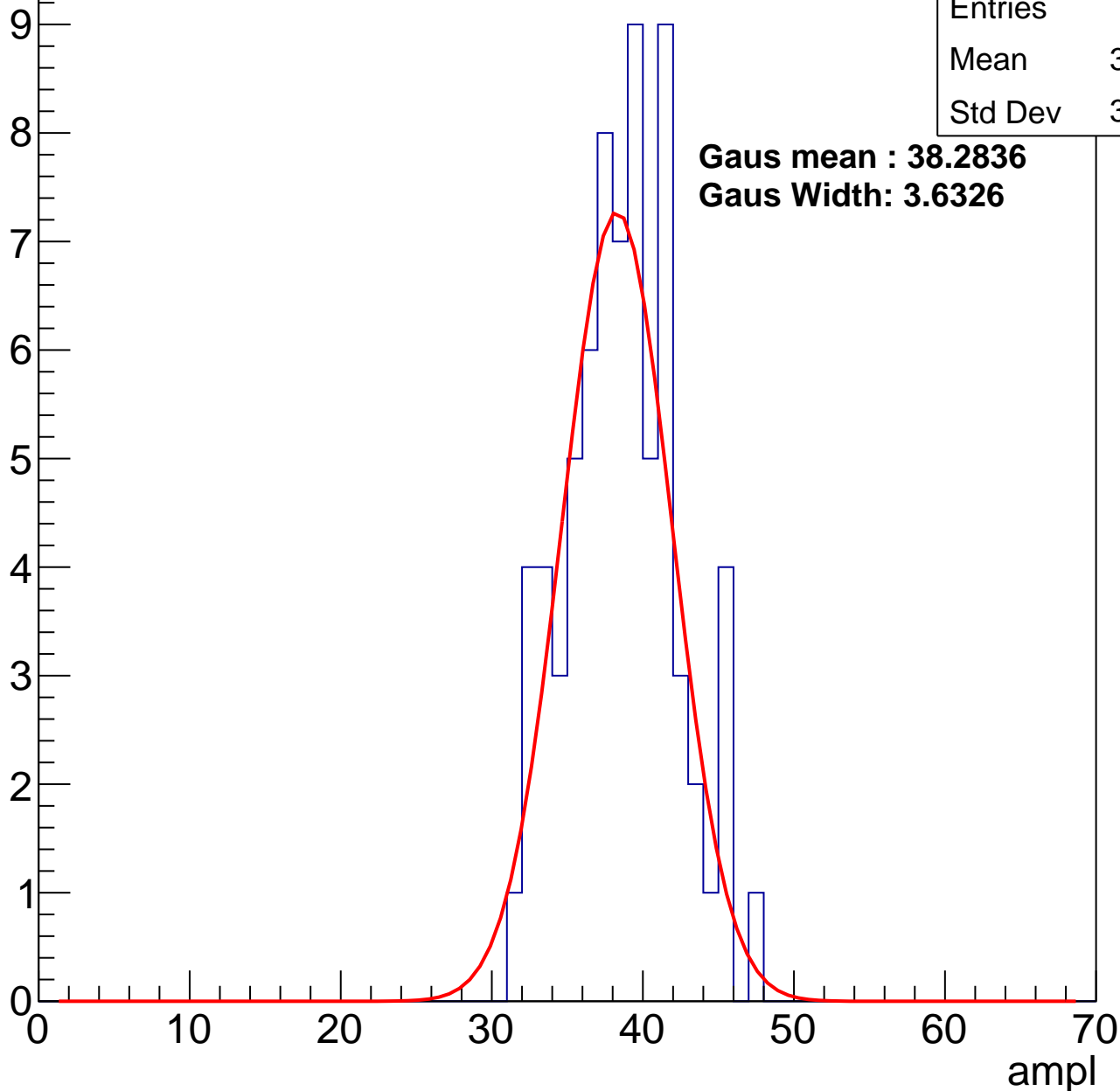
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	38.18
Std Dev	3.607

**Gaus mean : 38.2836**

**Gaus Width: 3.6326**



# B1L103S, U3-ch127, adc2

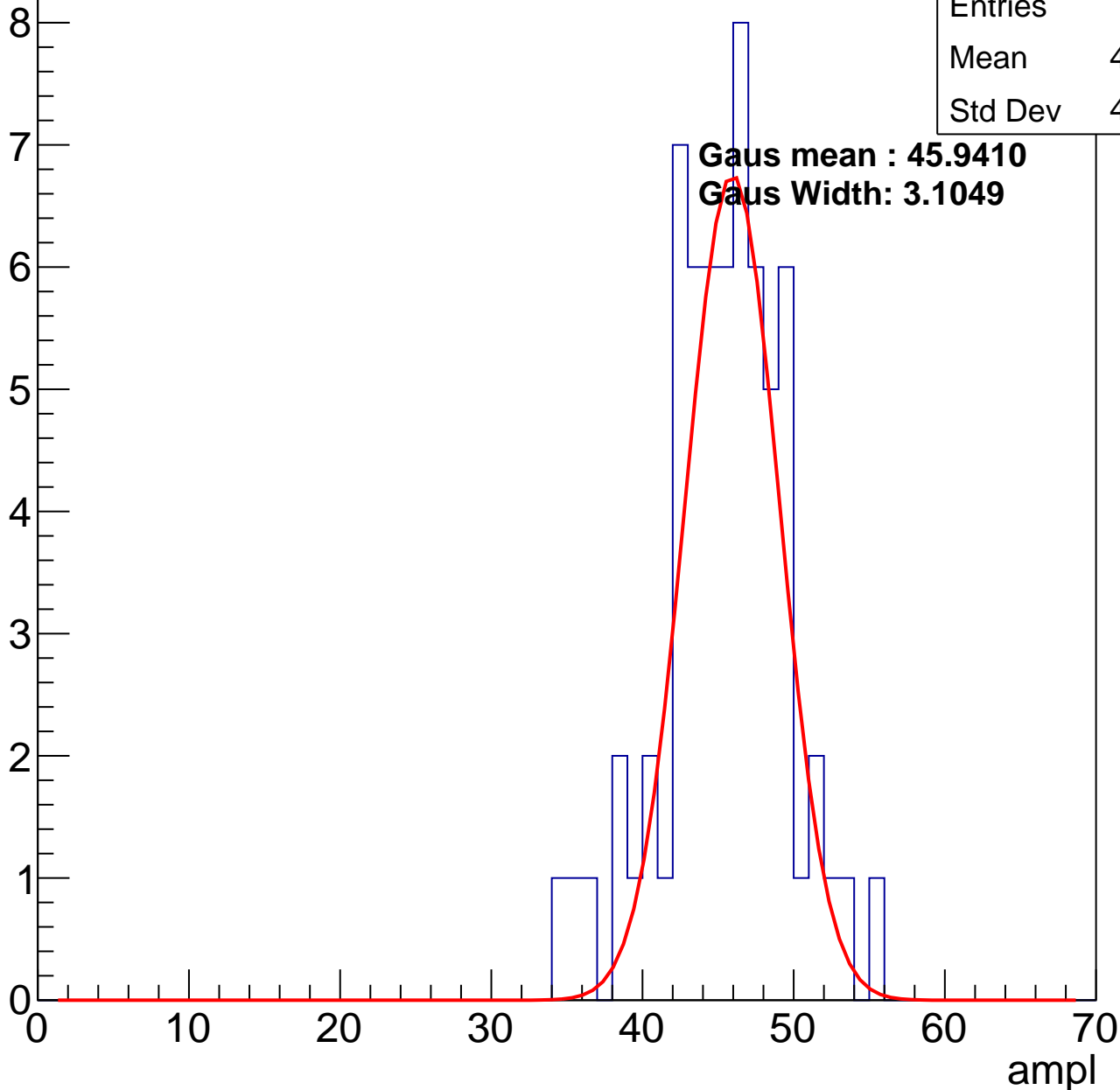
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	44.97
Std Dev	4.072

**Gaus mean : 45.9410**

**Gaus Width: 3.1049**

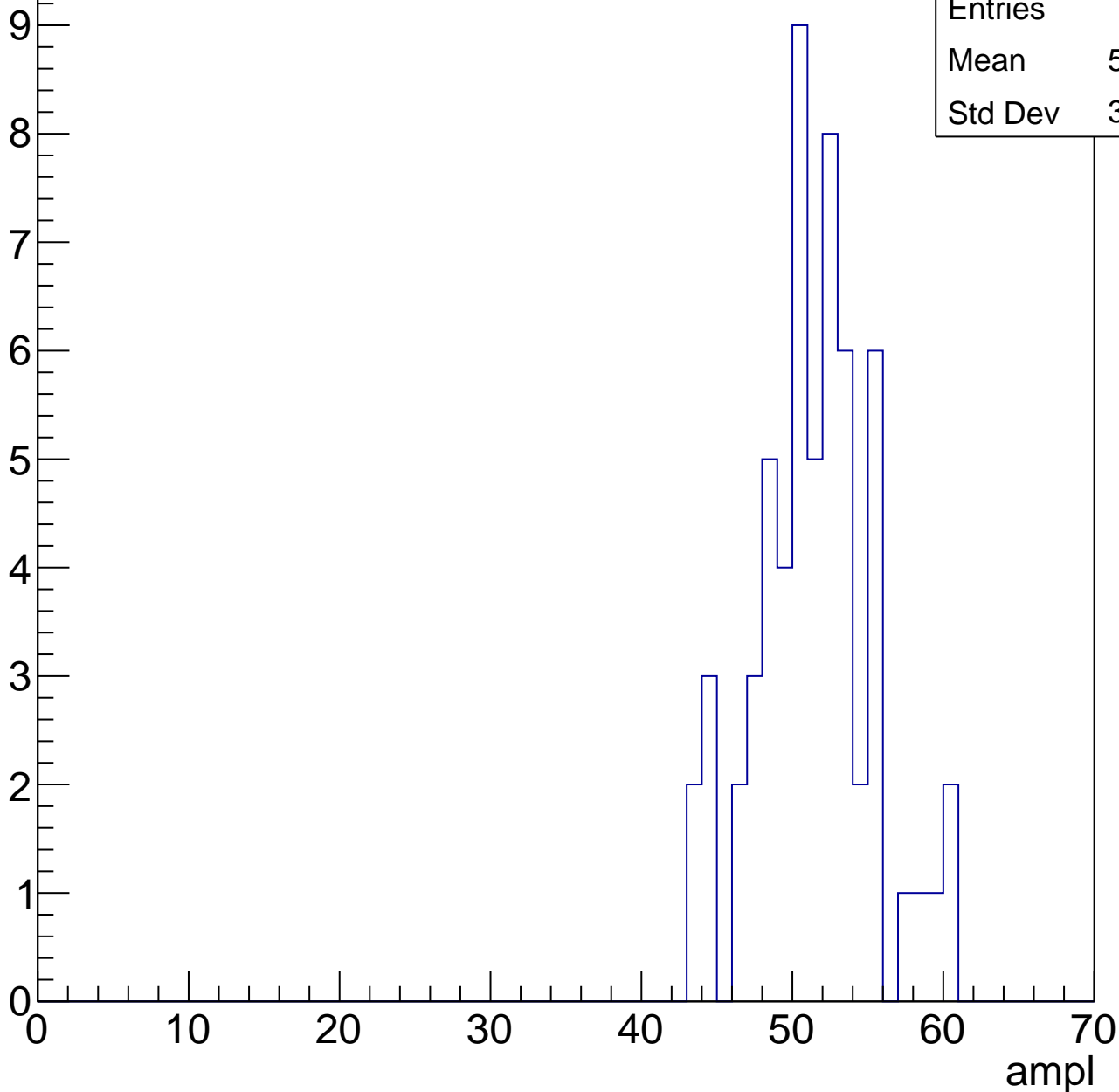


# B1L103S, U3-ch127, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

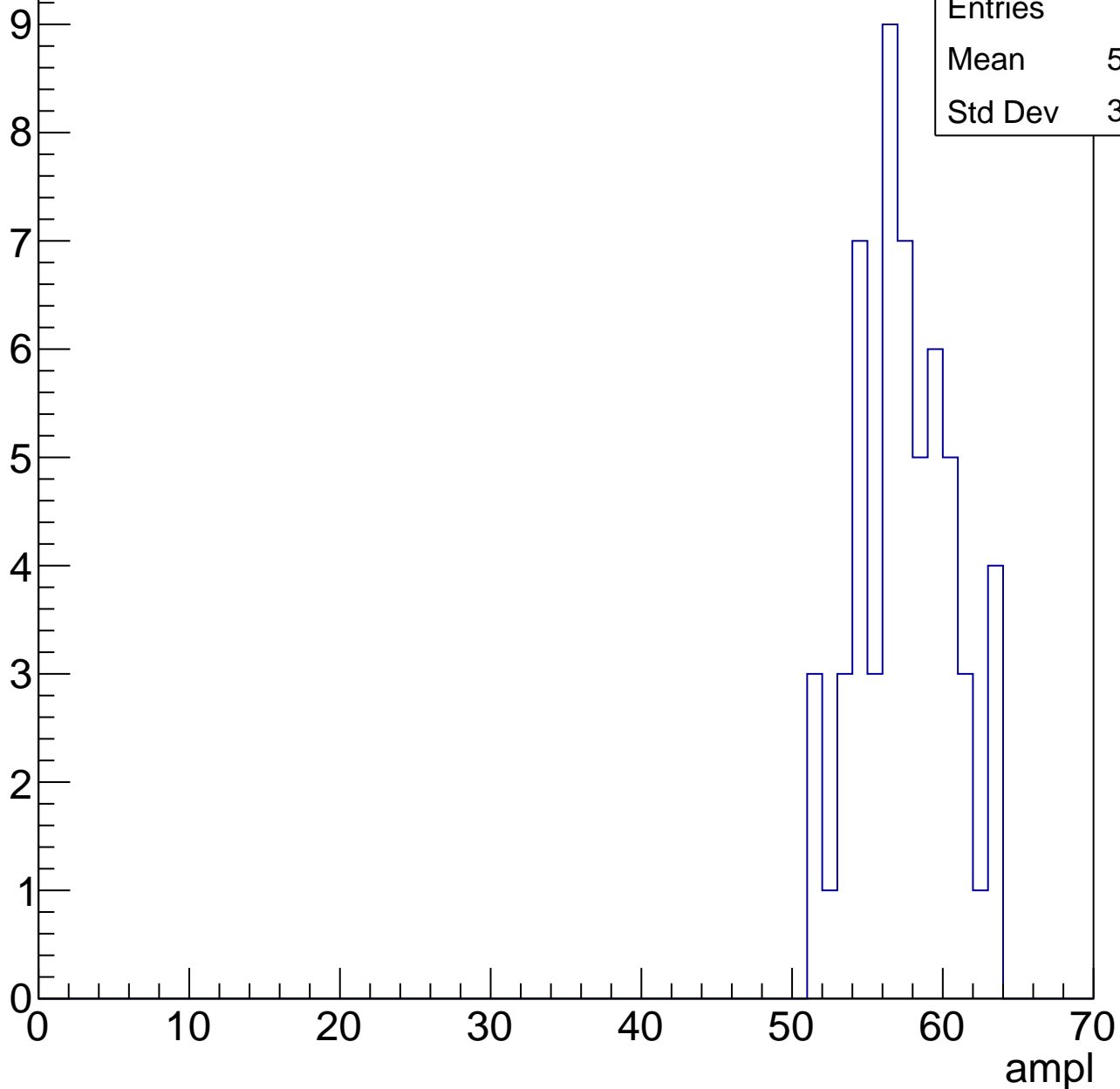
Entries	60
Mean	50.97
Std Dev	3.873



# B1L103S, U3-ch127, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



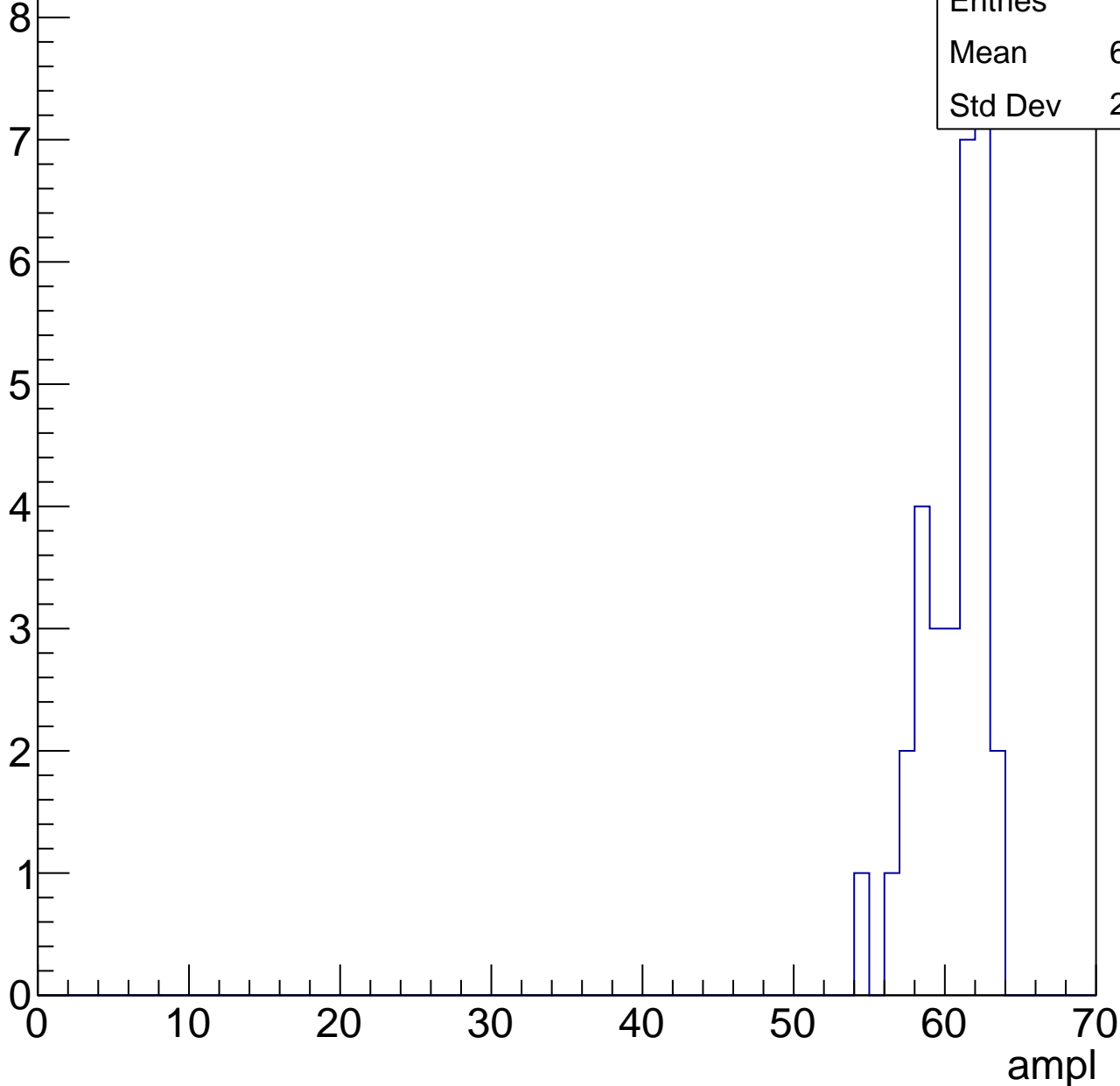
Entries	57
Mean	57.04
Std Dev	3.123

# B1L103S, U3-ch127, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

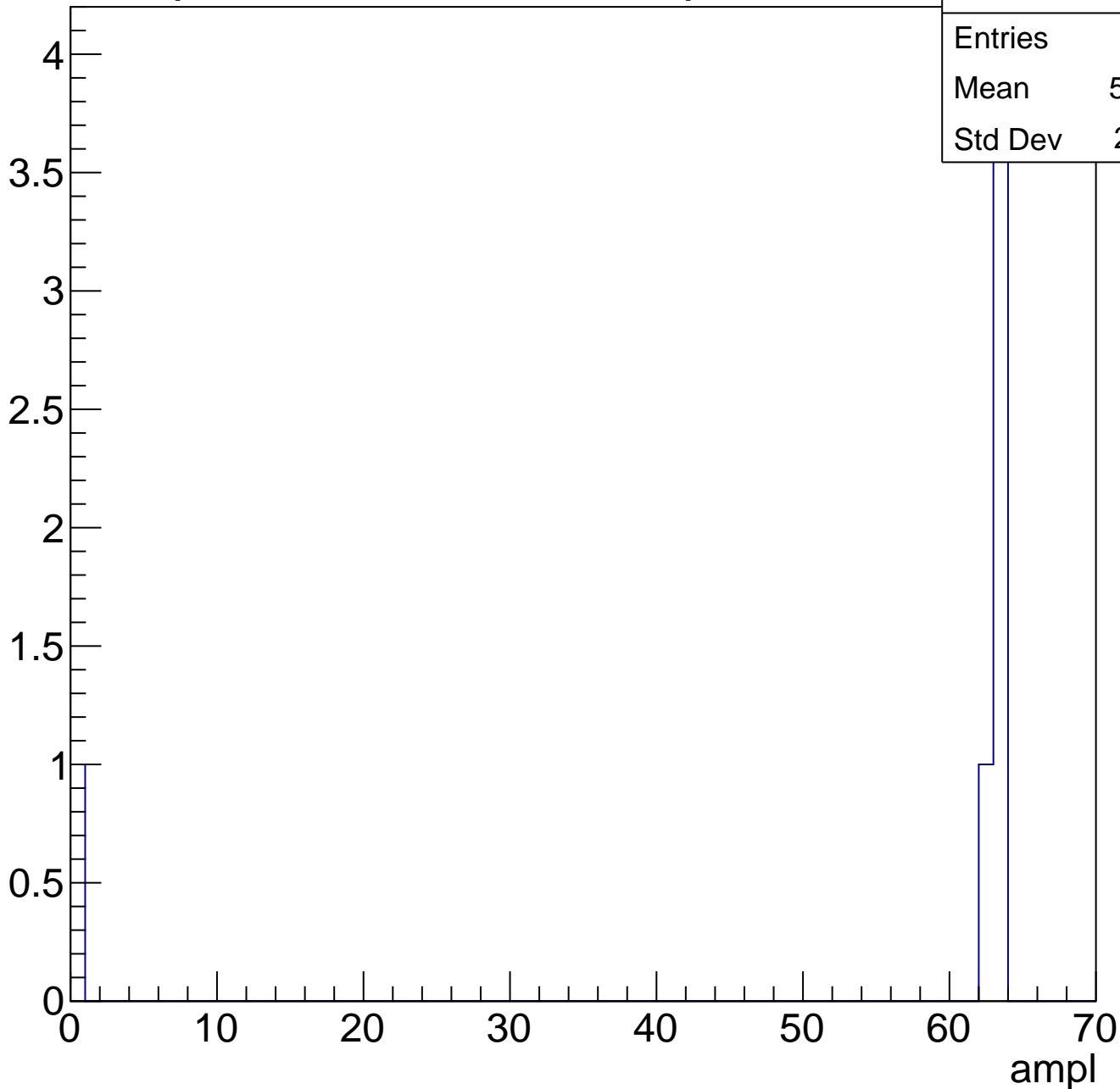
Entries	31
Mean	60.06
Std Dev	2.169



# B1L103S, U3-ch127, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U3-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U3-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

