

B0L100S, U8-ch0

calib_packv5_042523_0143.root, FC#6, port A1

Entry

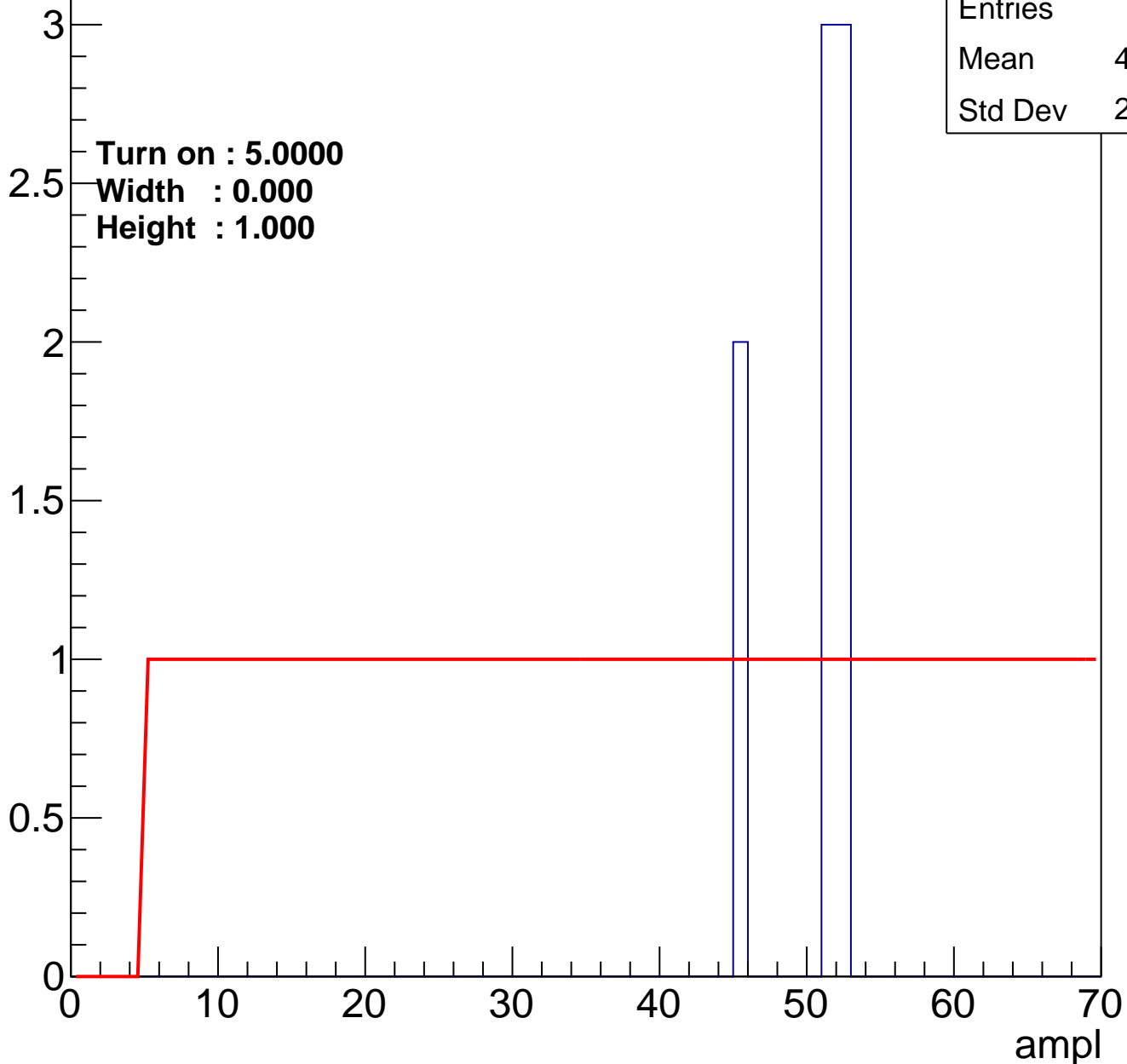


Entries	0
Mean	0
Std Dev	0

B0L100S, U8-ch1

calib_packv5_042523_0143.root, FC#6, port A1

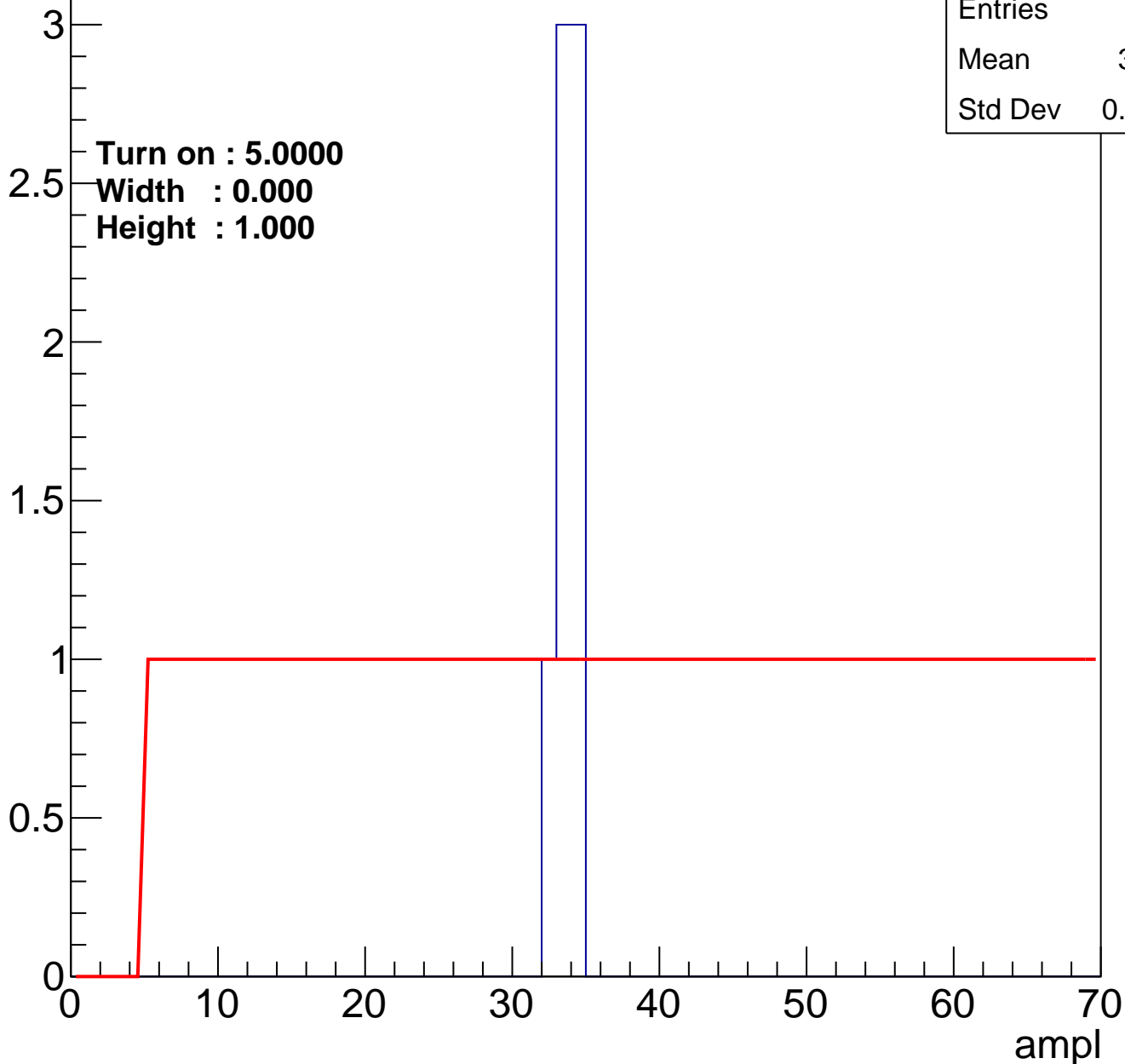
Entry



B0L100S, U8-ch2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U8-ch3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U8-ch4

calib_packv5_042523_0143.root, FC#6, port A1

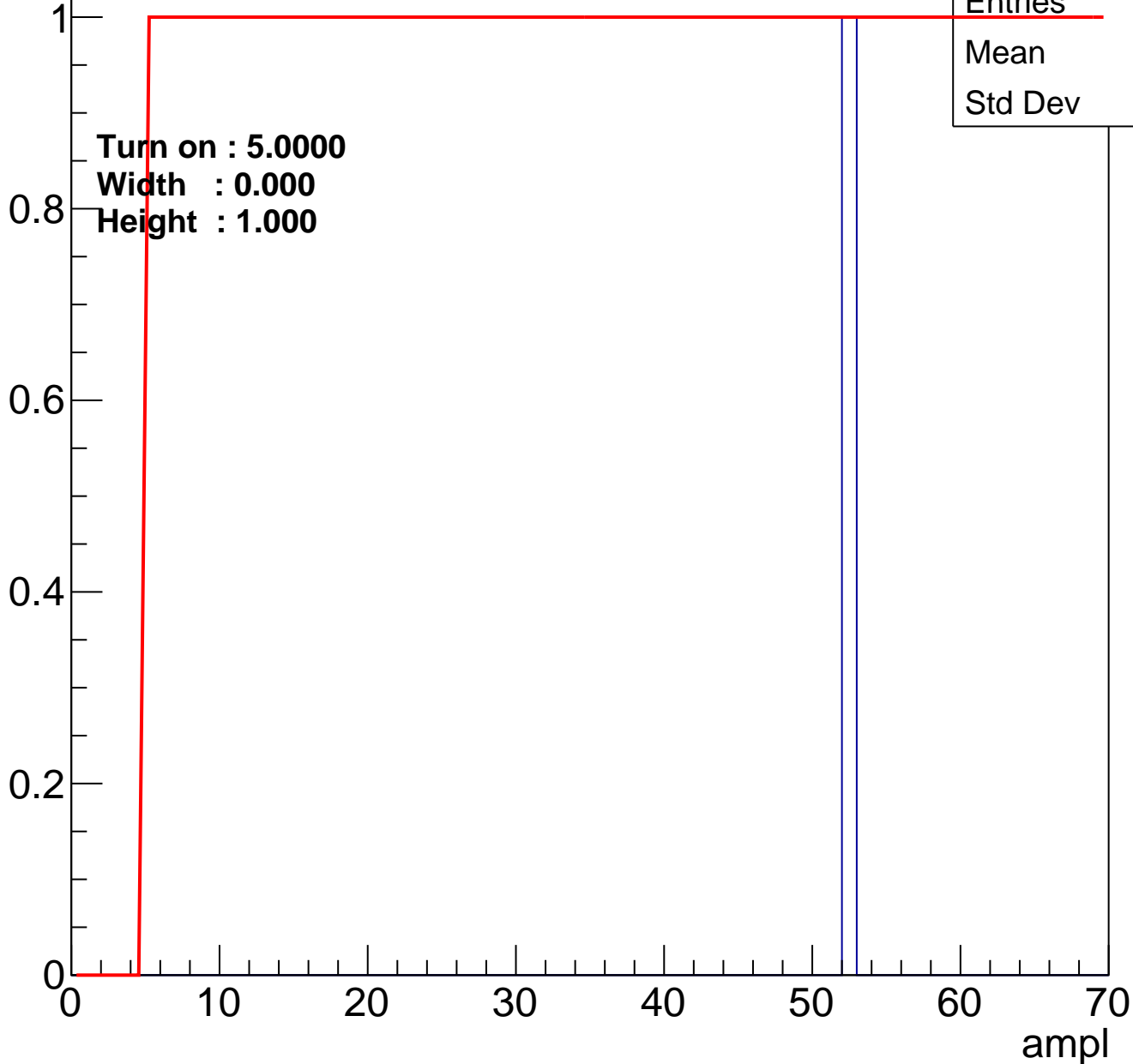
Entry



B0L100S, U8-ch5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U8-ch6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U8-ch7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U8-ch8

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U8-ch9

calib_packv5_042523_0143.root, FC#6, port A1

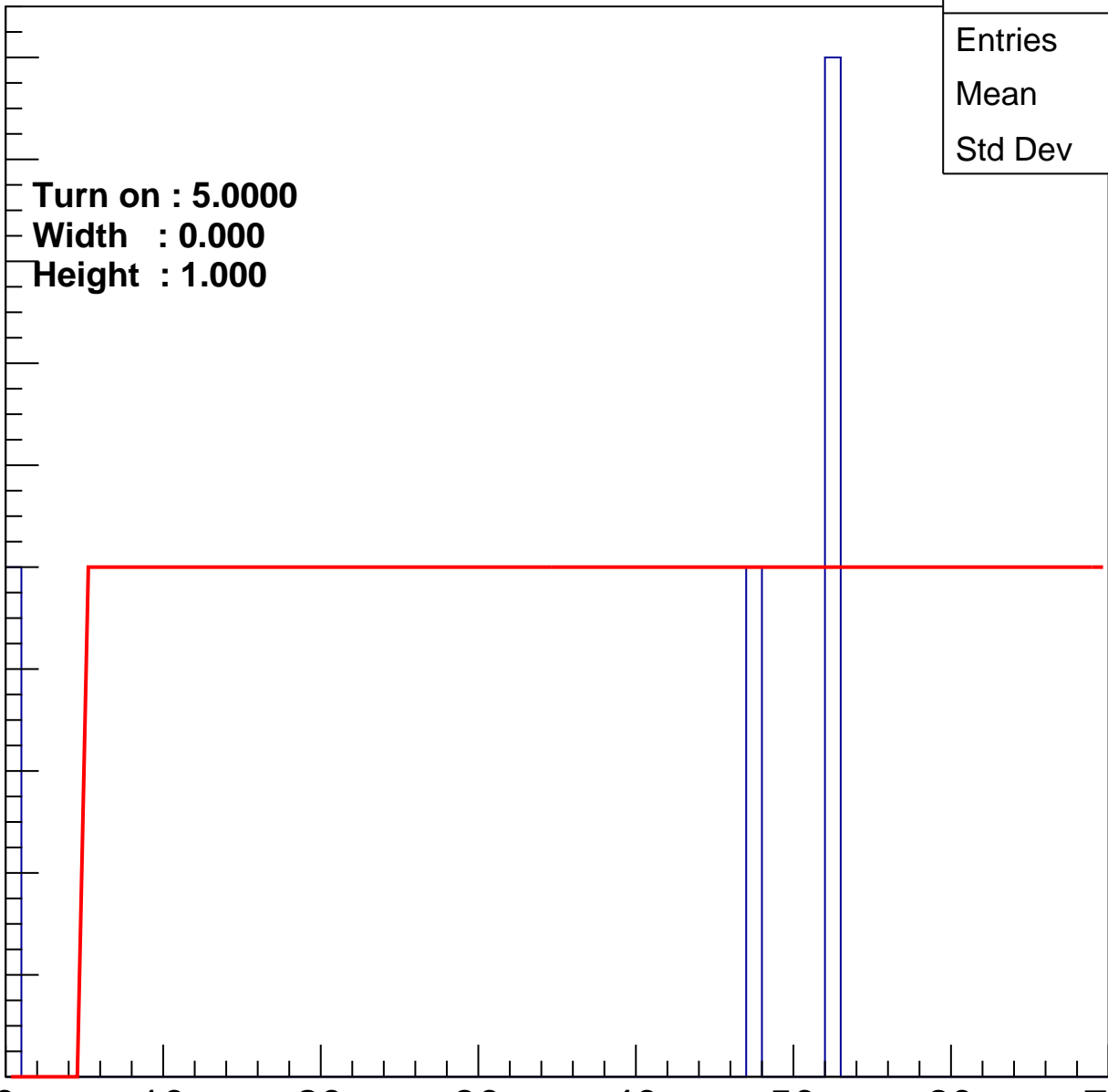
Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Turn on : 5.0000
Width : 0.000
Height : 1.000

Entries	4
Mean	37.75
Std Dev	21.89

0 10 20 30 40 50 60 70
ampl



B0L100S, U8-ch10

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U8-ch11

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U8-ch12

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U8-ch13

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U8-ch14

calib_packv5_042523_0143.root, FC#6, port A1

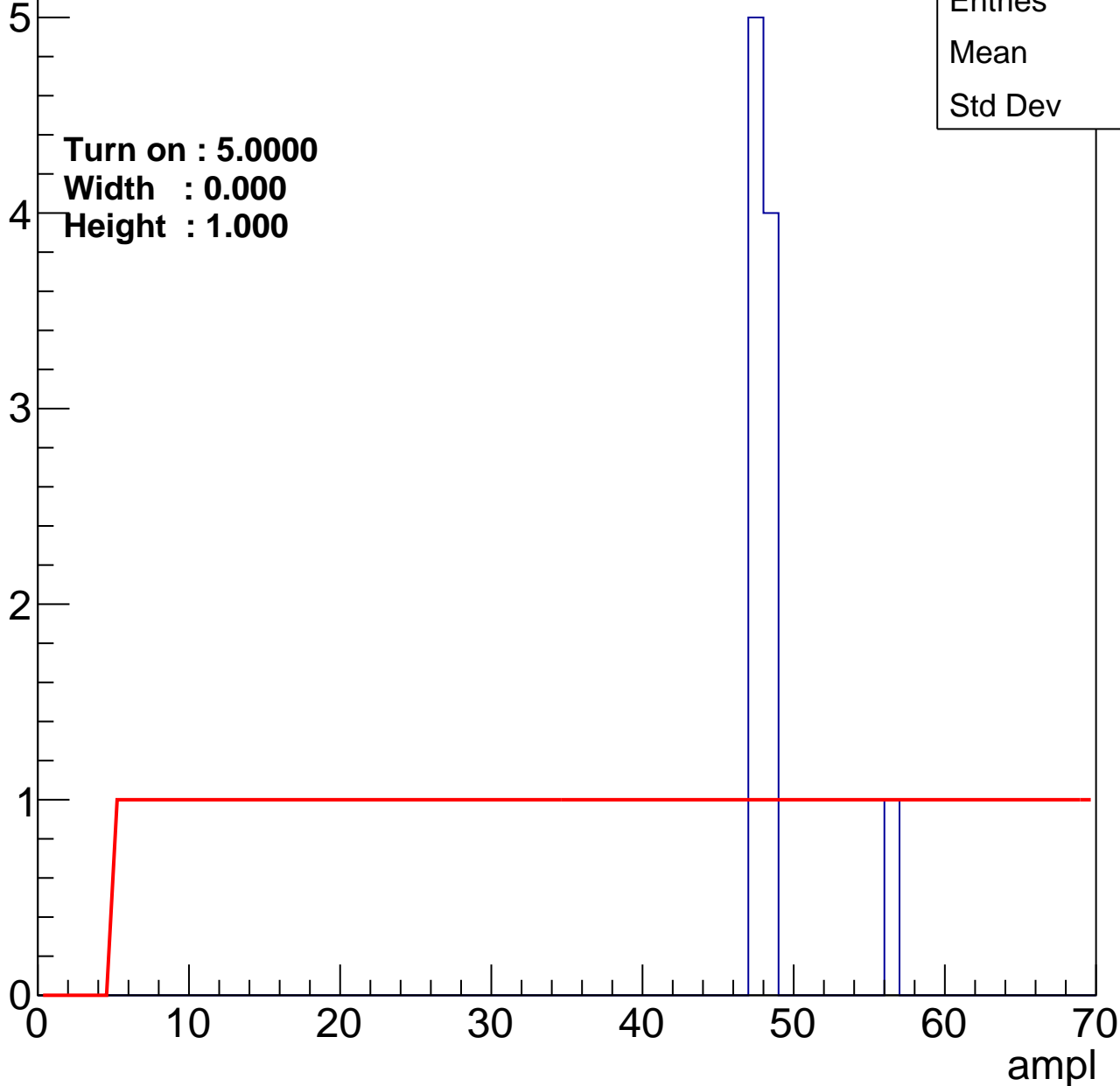
Entry

Entries	10
Mean	48.3
Std Dev	2.61

Turn on : 5.0000

Width : 0.000

Height : 1.000



B0L100S, U8-ch15

calib_packv5_042523_0143.root, FC#6, port A1

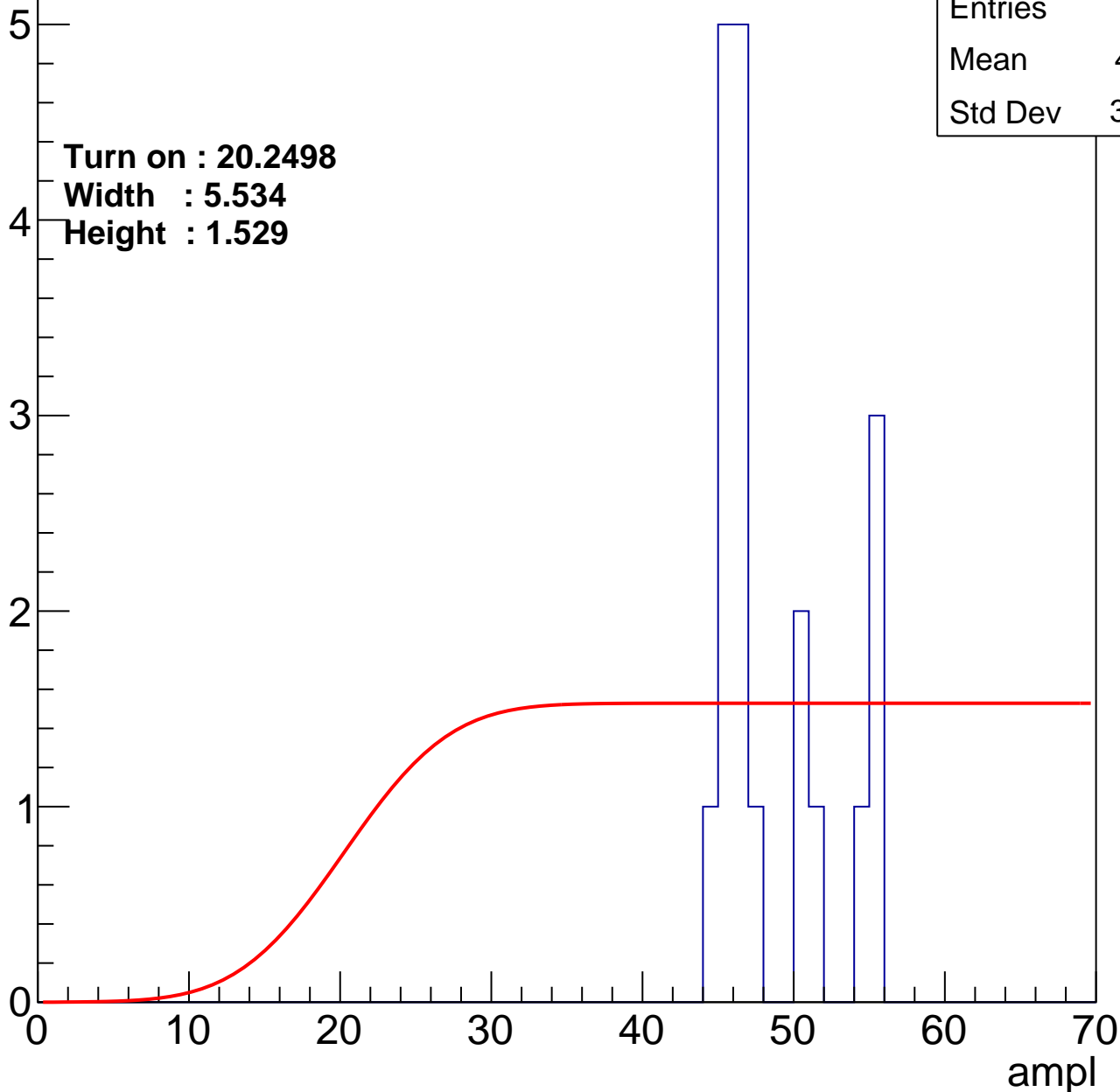
Entry

Entries	19
Mean	48.21
Std Dev	3.847

Turn on : 20.2498

Width : 5.534

Height : 1.529



B0L100S, U8-ch16

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U8-ch17

calib_packv5_042523_0143.root, FC#6, port A1

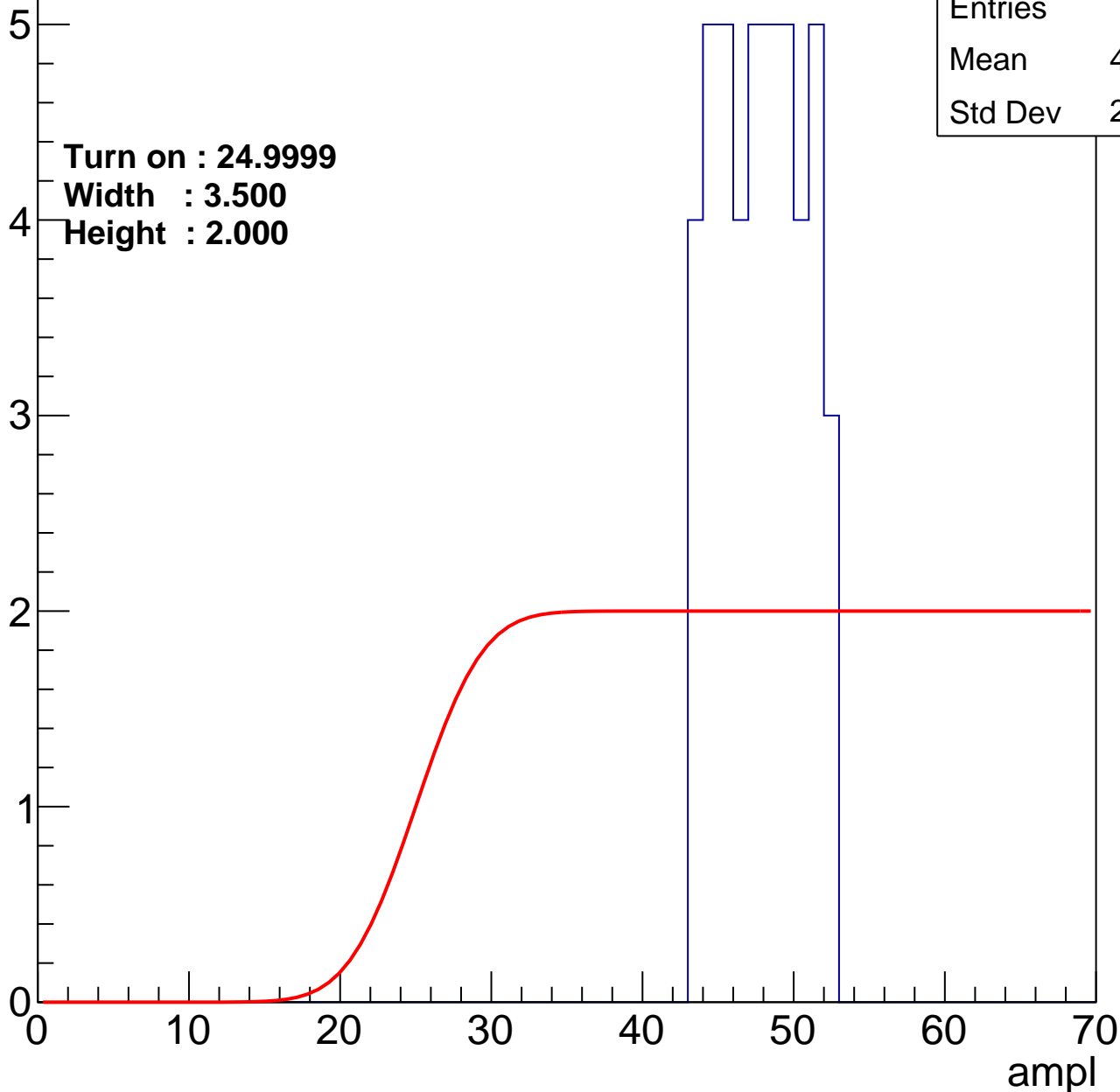
Entry

Entries	45
Mean	47.38
Std Dev	2.759

Turn on : 24.9999

Width : 3.500

Height : 2.000



B0L100S, U8-ch18

calib_packv5_042523_0143.root, FC#6, port A1

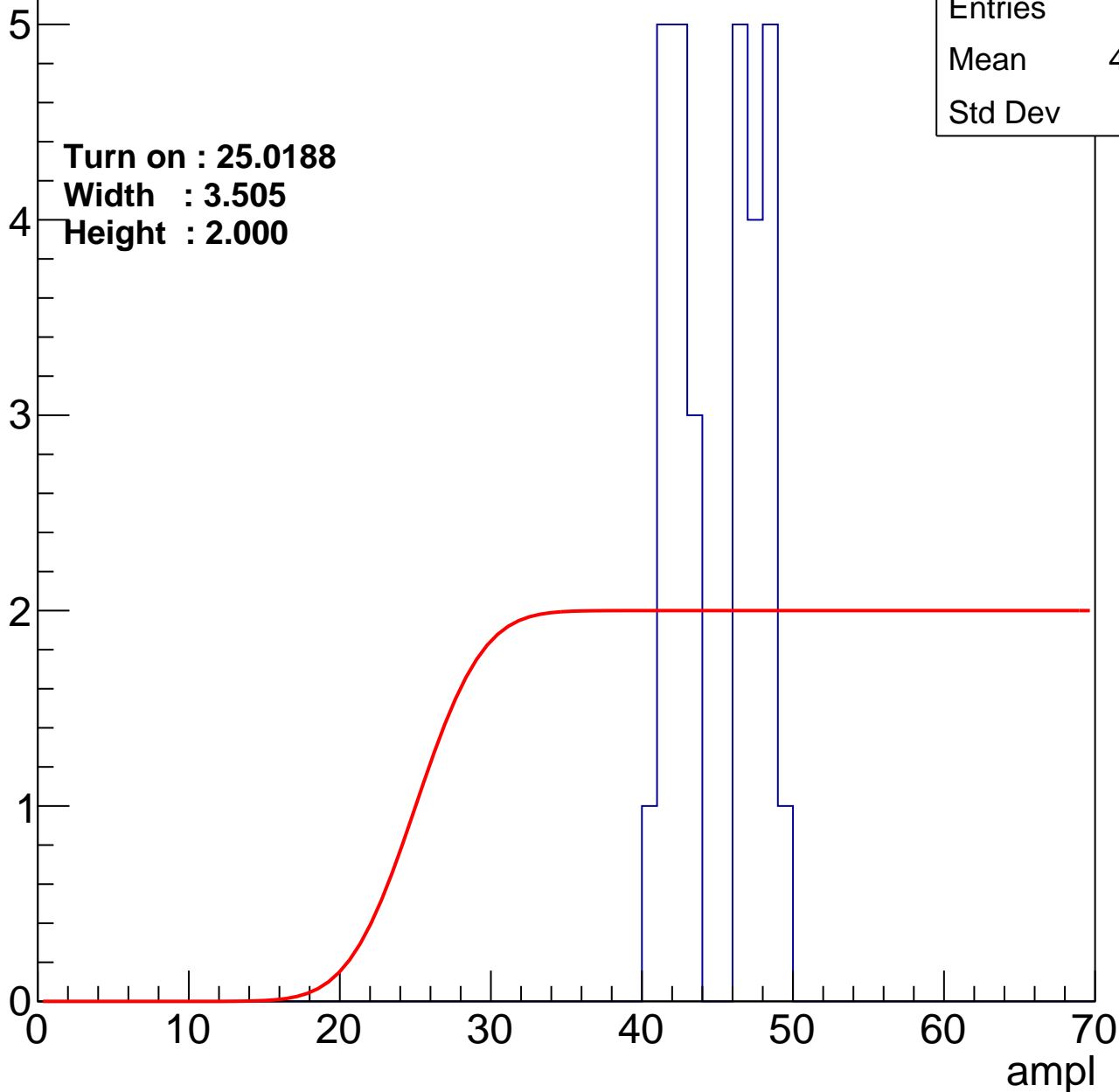
Entry

Entries	29
Mean	44.52
Std Dev	2.86

Turn on : 25.0188

Width : 3.505

Height : 2.000



B0L100S, U8-ch19

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U8-ch20

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U8-ch21

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U8-ch22

calib_packv5_042523_0143.root, FC#6, port A1

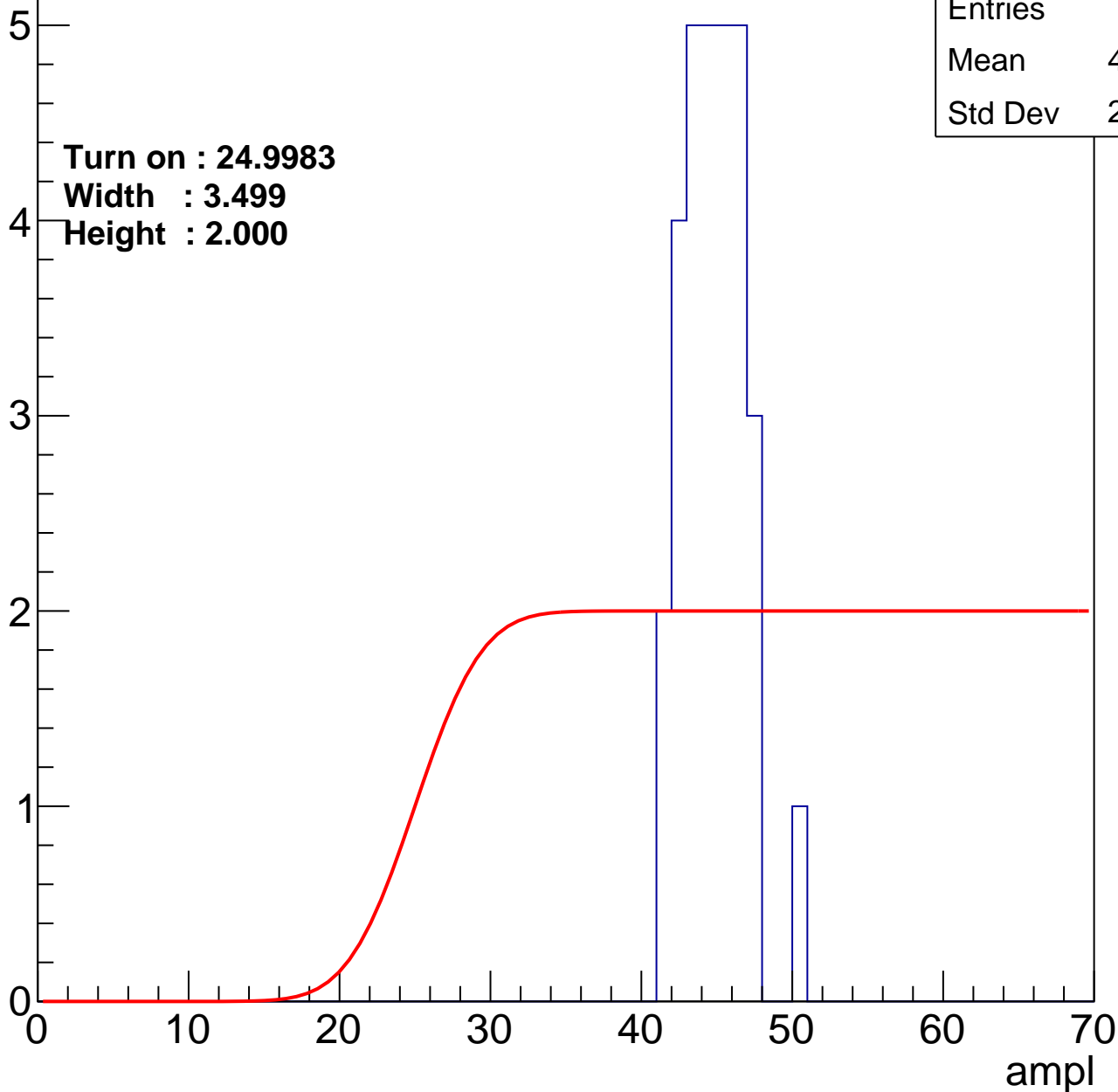
Entry

Entries	30
Mean	44.37
Std Dev	2.025

Turn on : 24.9983

Width : 3.499

Height : 2.000



B0L100S, U8-ch23

calib_packv5_042523_0143.root, FC#6, port A1

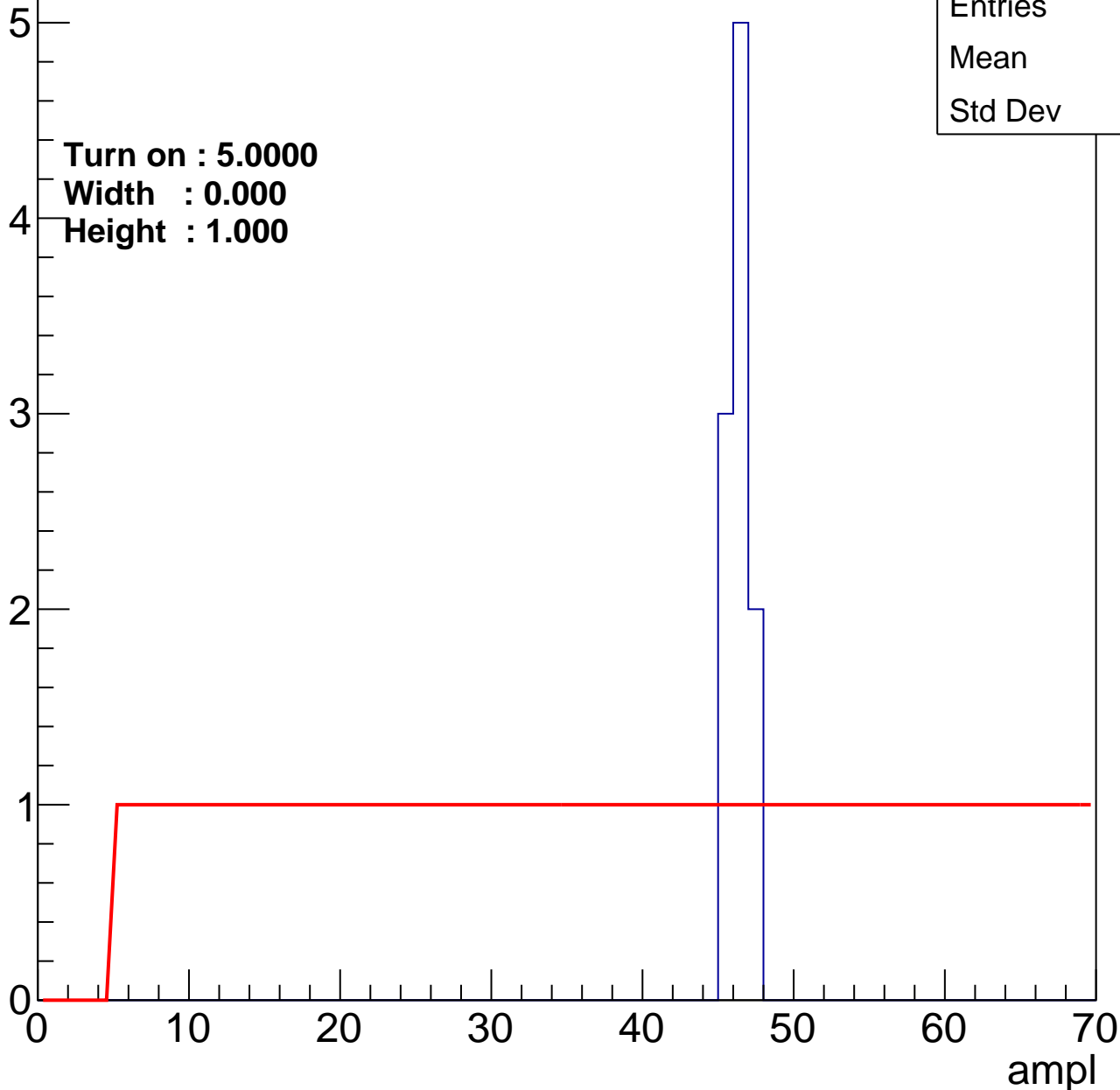
Entry

Entries	10
Mean	45.9
Std Dev	0.7

Turn on : 5.0000

Width : 0.000

Height : 1.000



B0L100S, U8-ch24

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U8-ch25

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U8-ch26

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U8-ch27

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U8-ch28

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U8-ch29

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U8-ch30

calib_packv5_042523_0143.root, FC#6, port A1

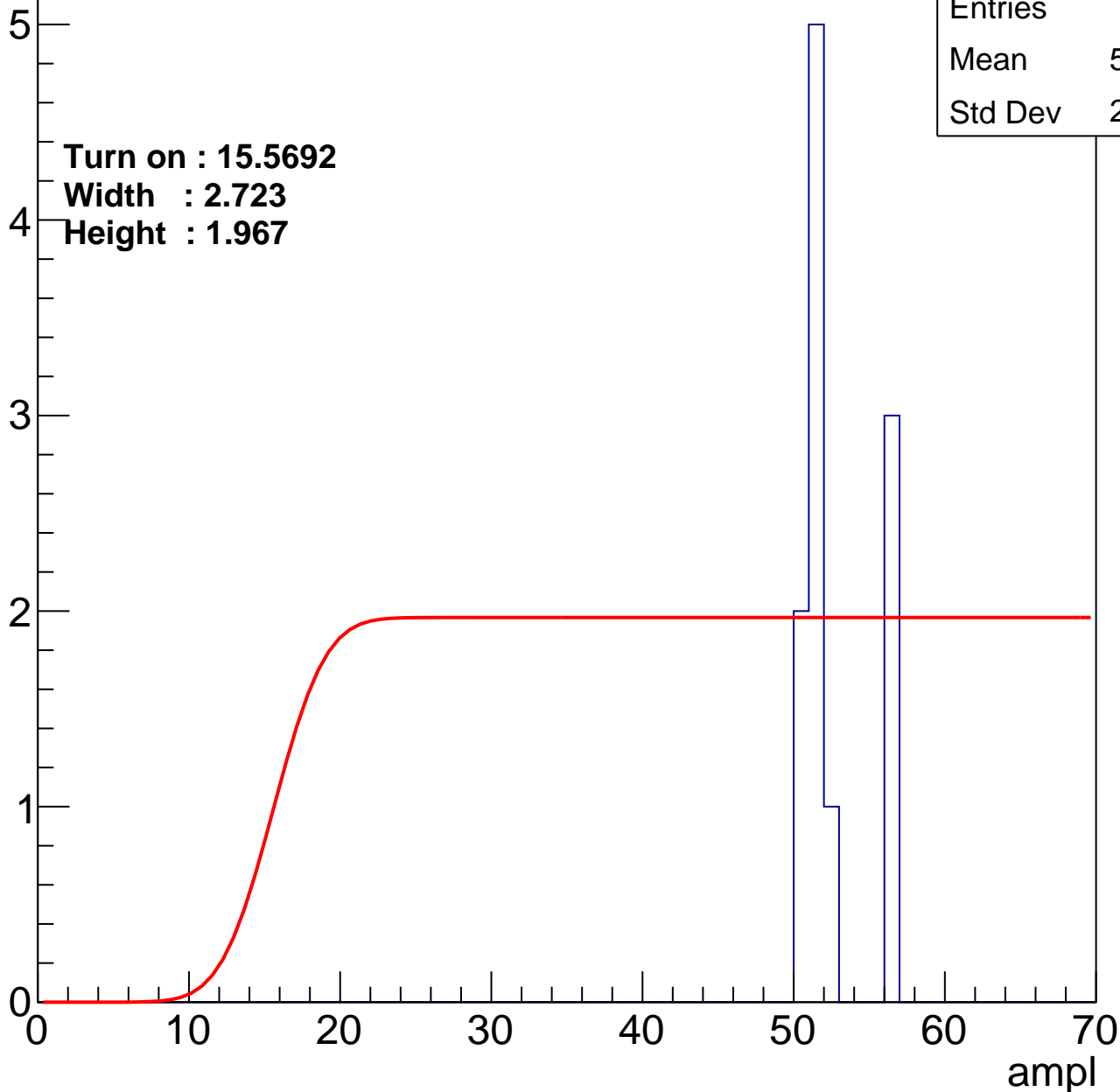
Entry

Entries	11
Mean	52.27
Std Dev	2.339

Turn on : 15.5692

Width : 2.723

Height : 1.967



B0L100S, U8-ch31

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U8-ch32

calib_packv5_042523_0143.root, FC#6, port A1

Entry

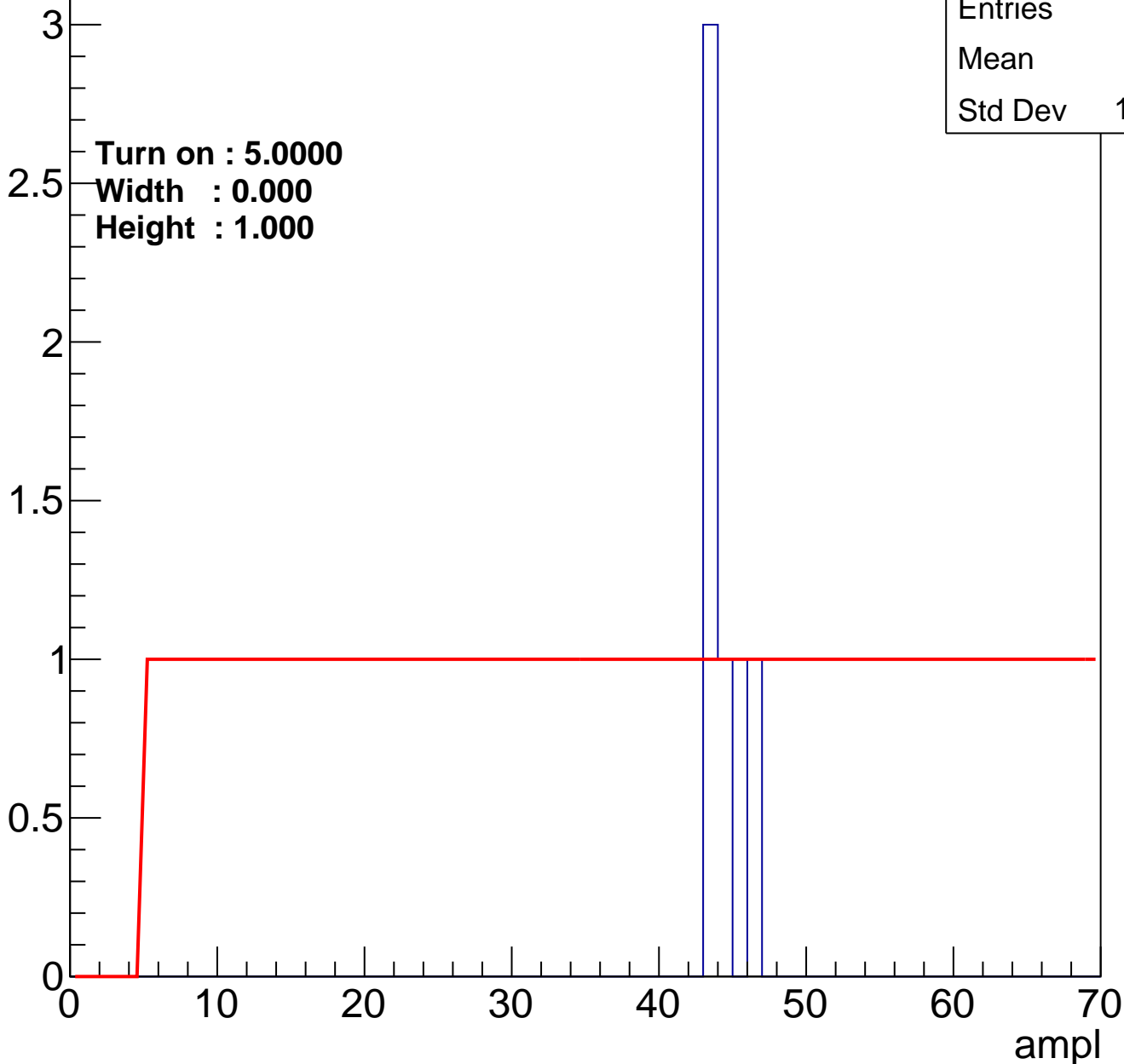


Entries	0
Mean	0
Std Dev	0

B0L100S, U8-ch33

calib_packv5_042523_0143.root, FC#6, port A1

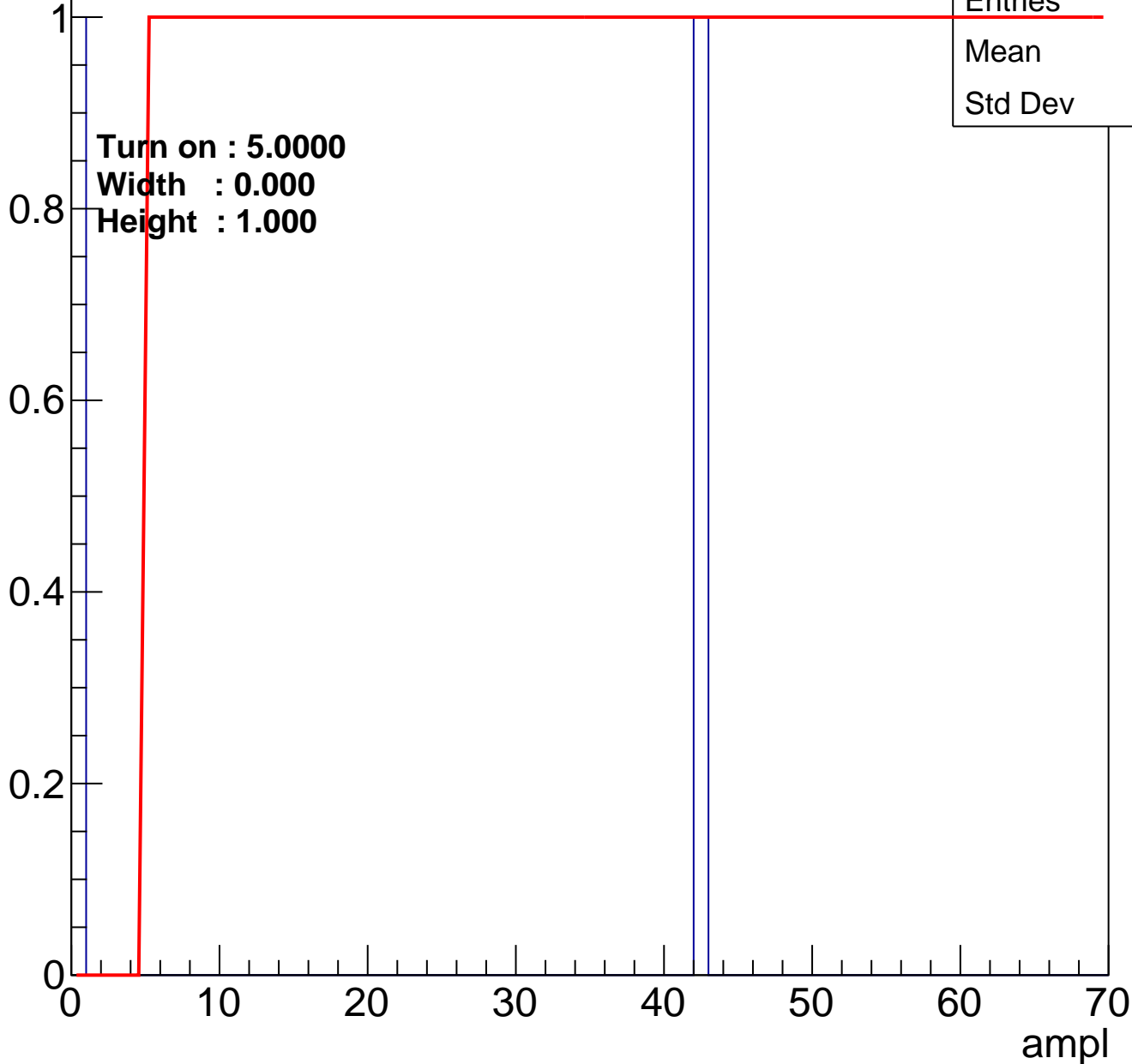
Entry



B0L100S, U8-ch34

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	2
Mean	21
Std Dev	21

B0L100S, U8-ch35

calib_packv5_042523_0143.root, FC#6, port A1

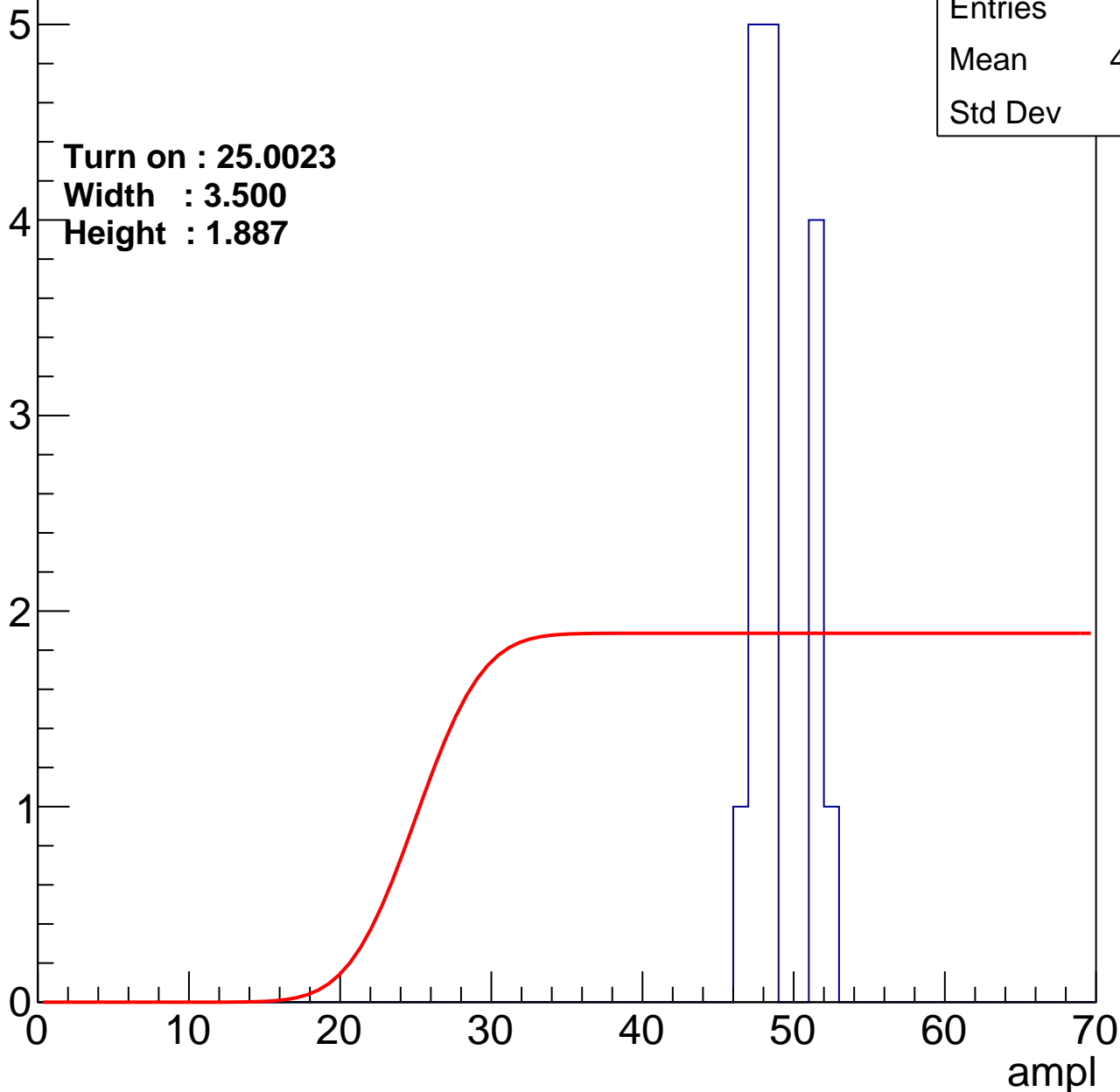
Entry

Entries	16
Mean	48.56
Std Dev	1.87

Turn on : 25.0023

Width : 3.500

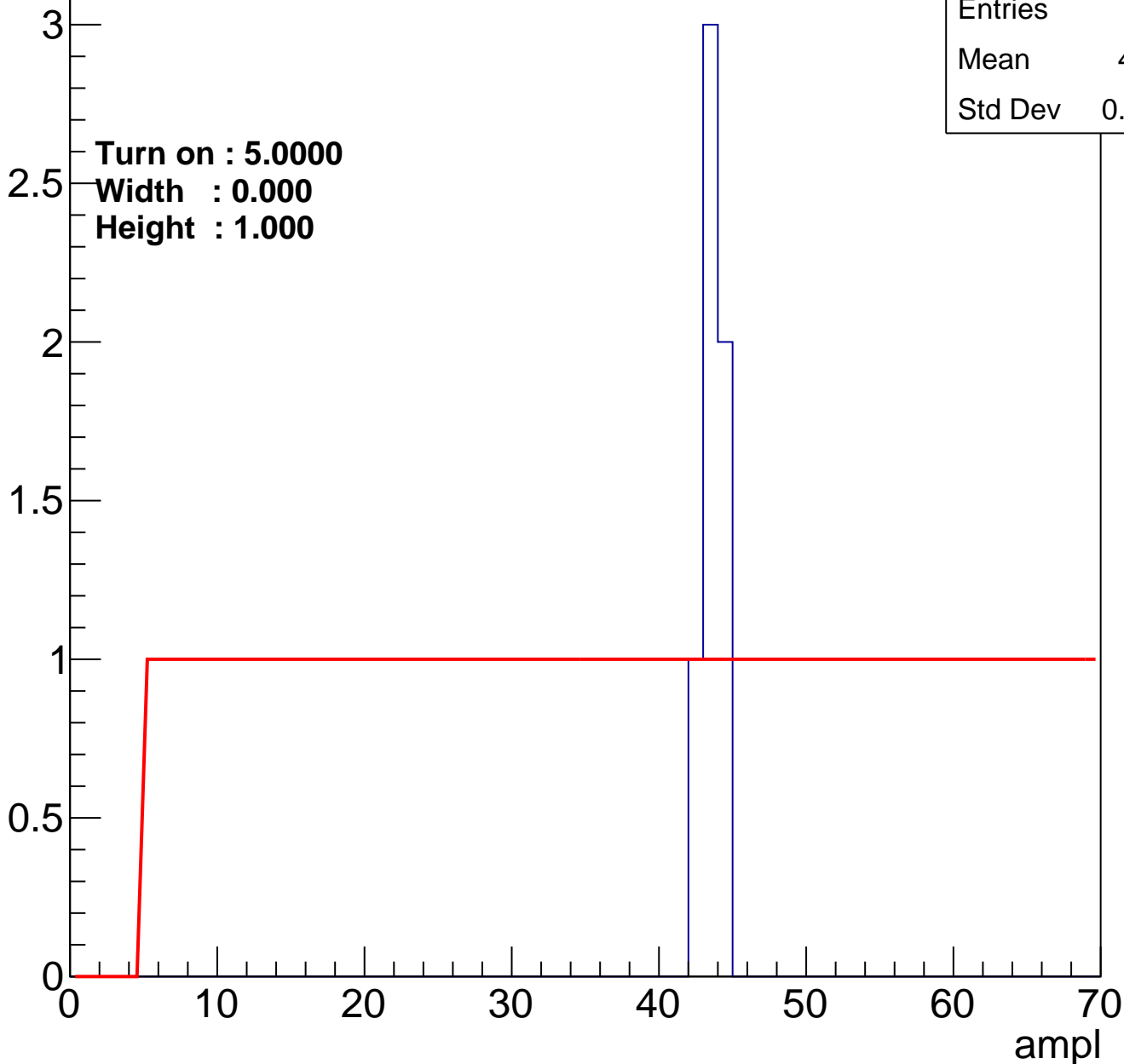
Height : 1.887



B0L100S, U8-ch36

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	6
Mean	43.17
Std Dev	0.6872

B0L100S, U8-ch37

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U8-ch38

calib_packv5_042523_0143.root, FC#6, port A1

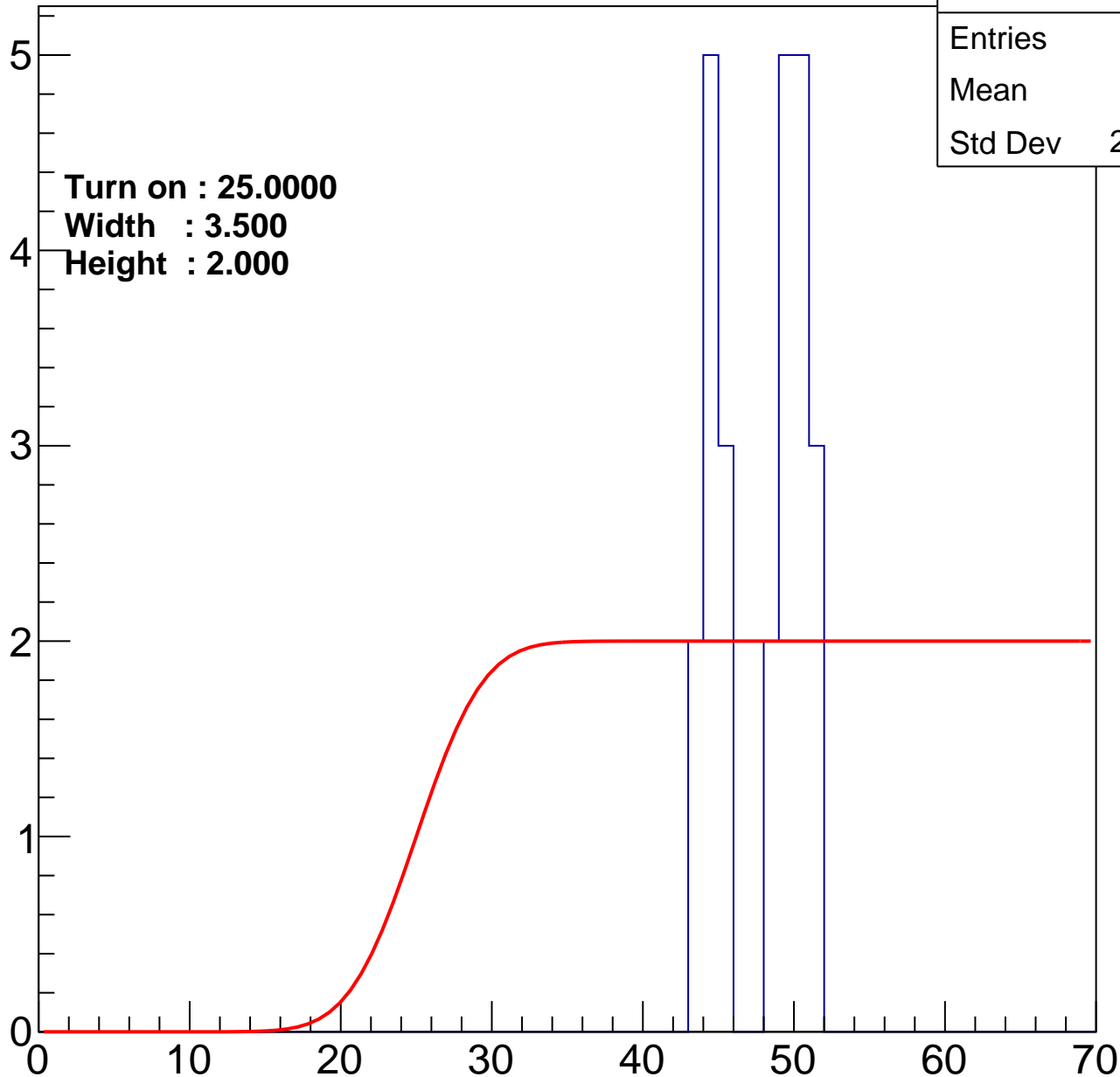
Entry

5
4
3
2
1
0

Turn on : 25.0000
Width : 3.500
Height : 2.000

Entries	25
Mean	47.4
Std Dev	2.828

ampl



B0L100S, U8-ch39

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U8-ch40

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U8-ch41

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U8-ch42

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U8-ch43

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U8-ch44

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U8-ch45

calib_packv5_042523_0143.root, FC#6, port A1

Entry

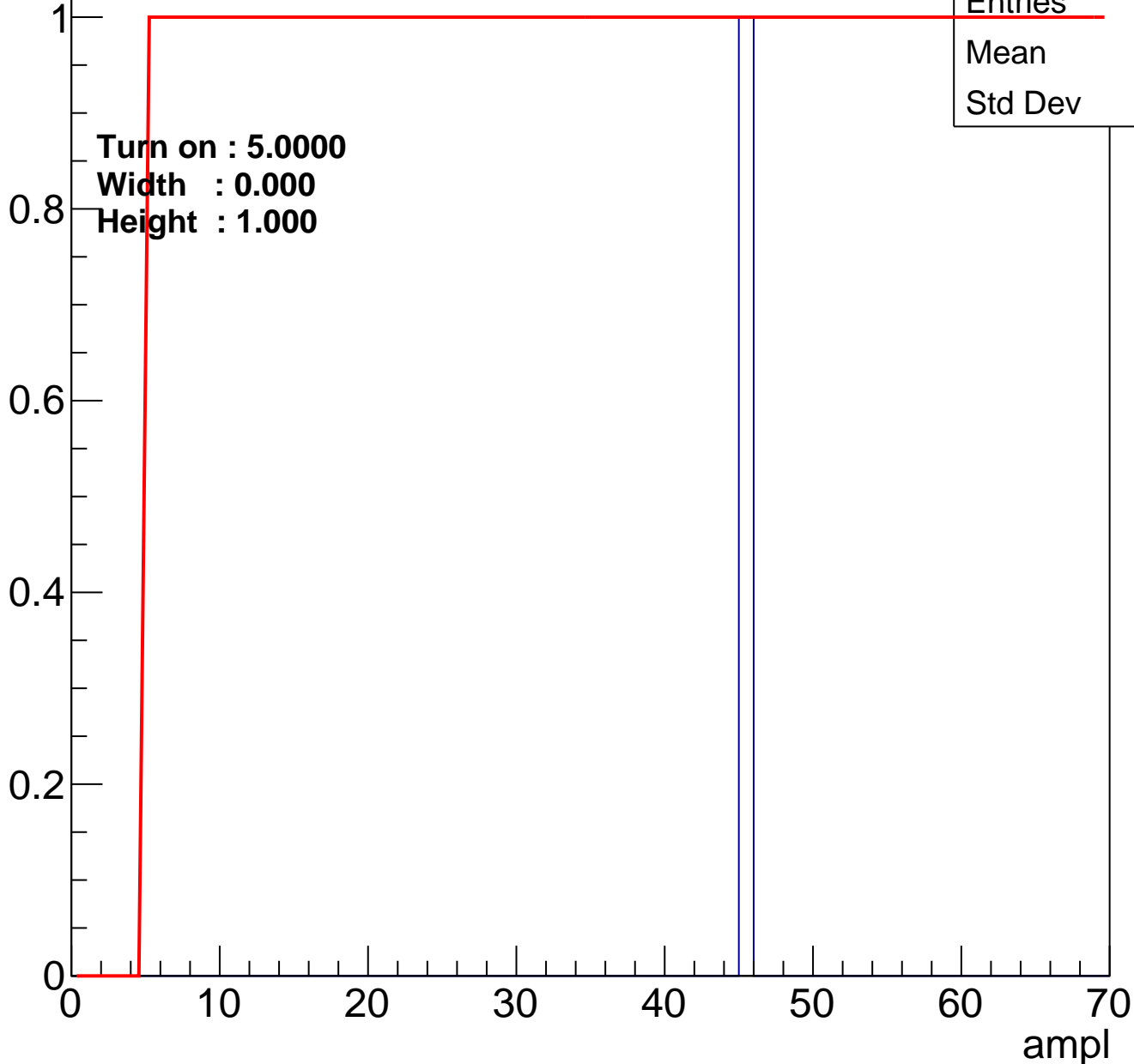


Entries	0
Mean	0
Std Dev	0

B0L100S, U8-ch46

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U8-ch47

calib_packv5_042523_0143.root, FC#6, port A1

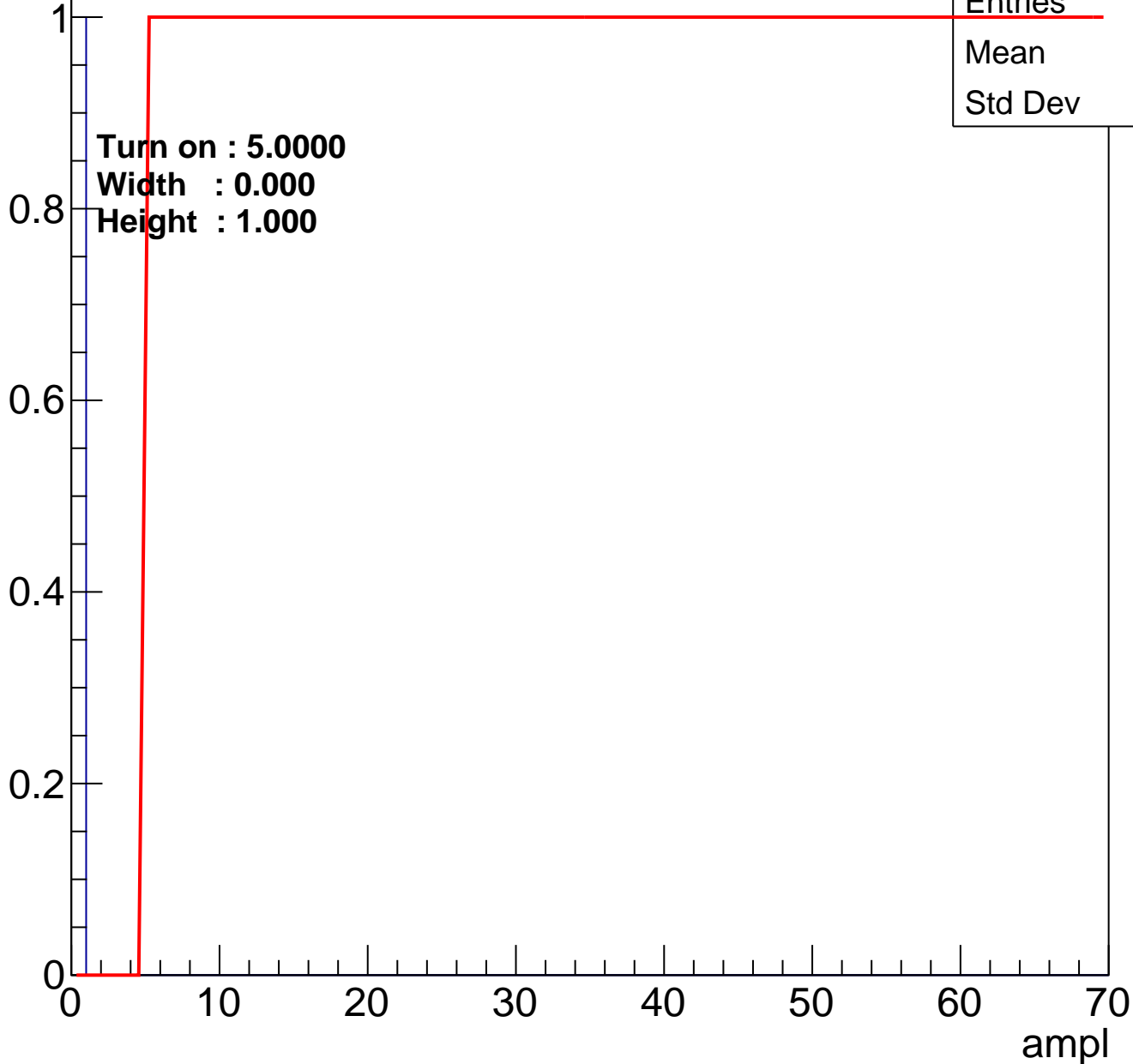
Entry



B0L100S, U8-ch48

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U8-ch49

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U8-ch50

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U8-ch51

calib_packv5_042523_0143.root, FC#6, port A1

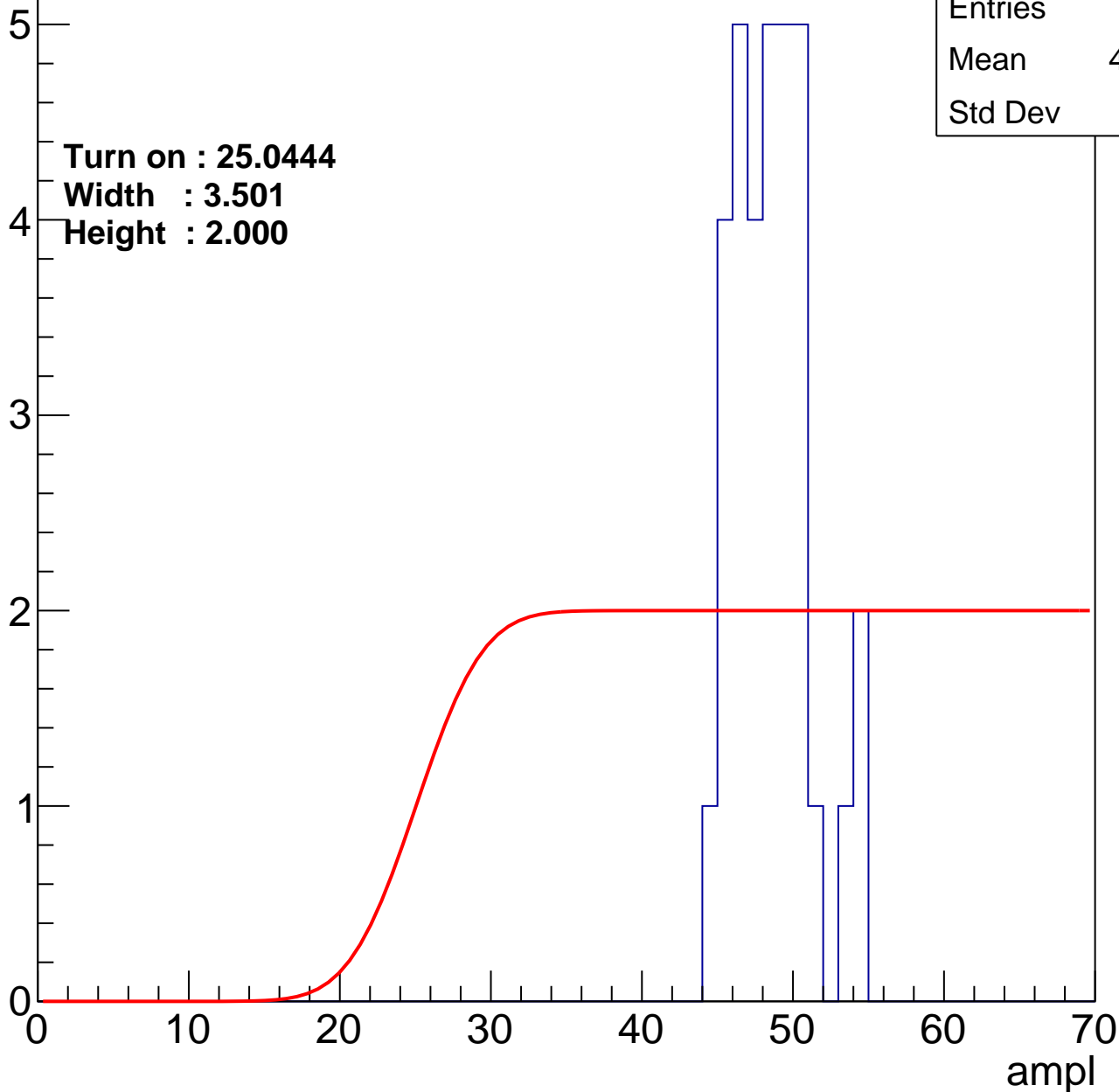
Entry

Entries	33
Mean	48.15
Std Dev	2.5

Turn on : 25.0444

Width : 3.501

Height : 2.000



B0L100S, U8-ch52

calib_packv5_042523_0143.root, FC#6, port A1

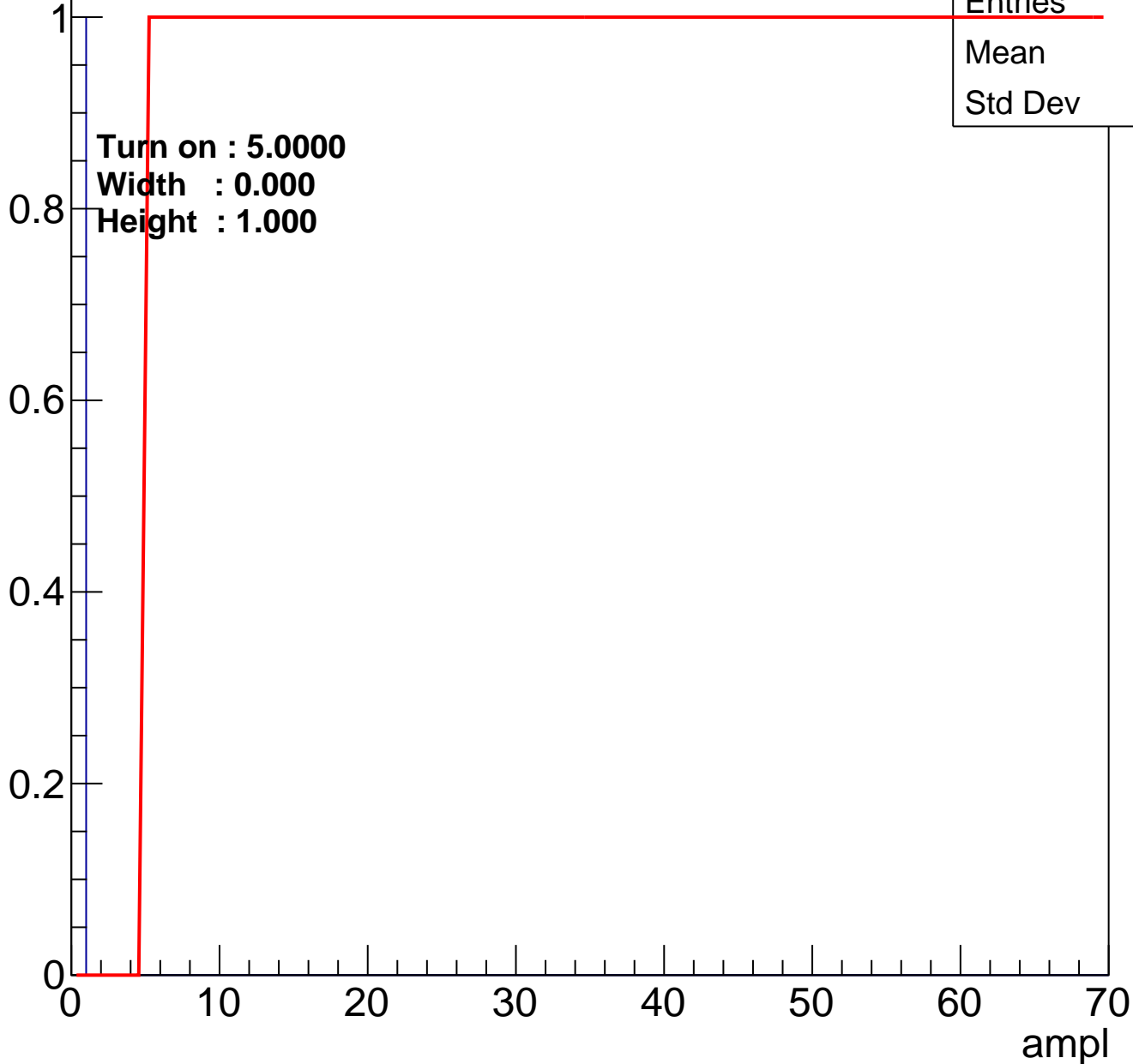
Entry



B0L100S, U8-ch53

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U8-ch54

calib_packv5_042523_0143.root, FC#6, port A1

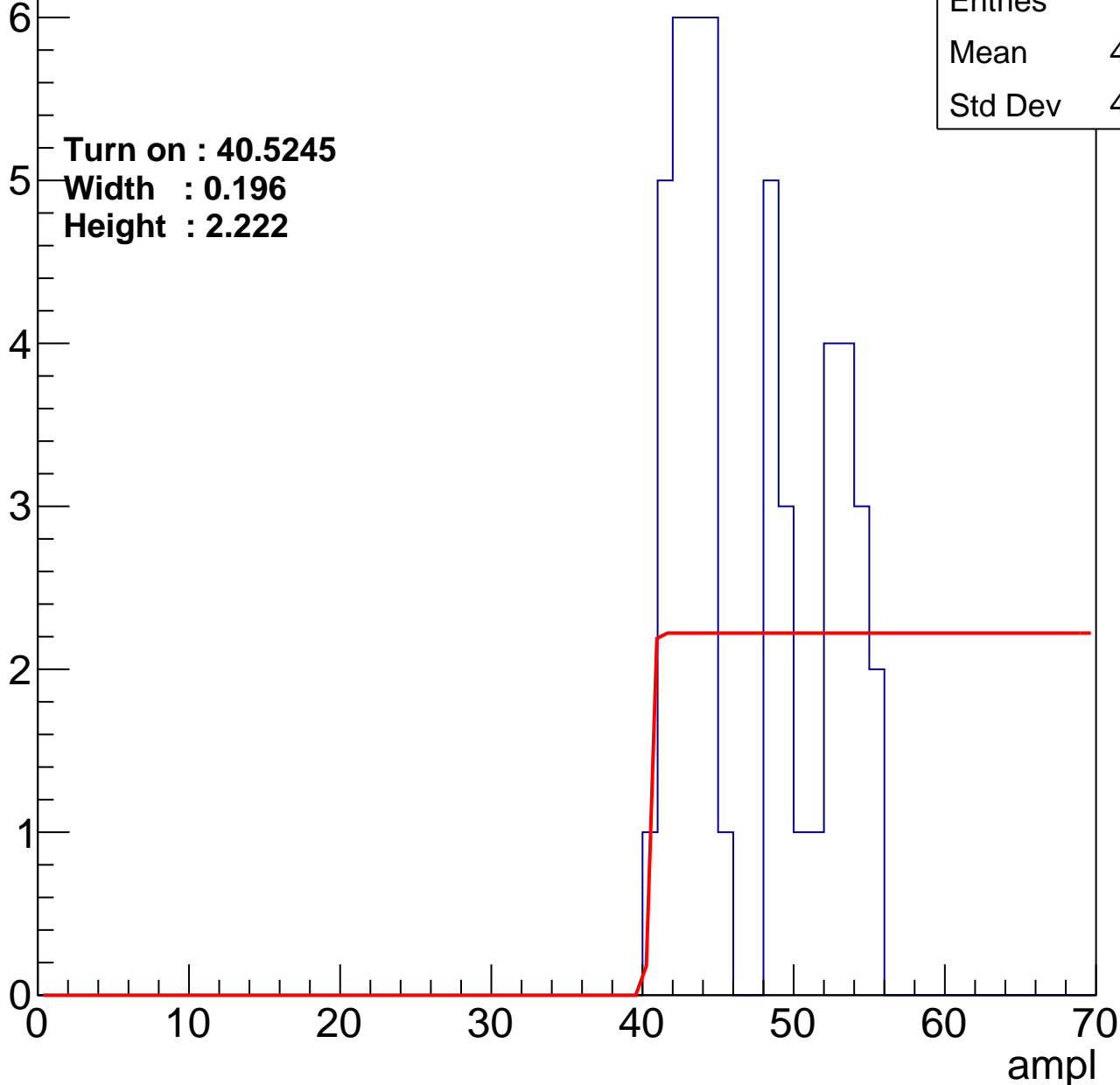
Entry

Entries	48
Mean	46.75
Std Dev	4.768

Turn on : 40.5245

Width : 0.196

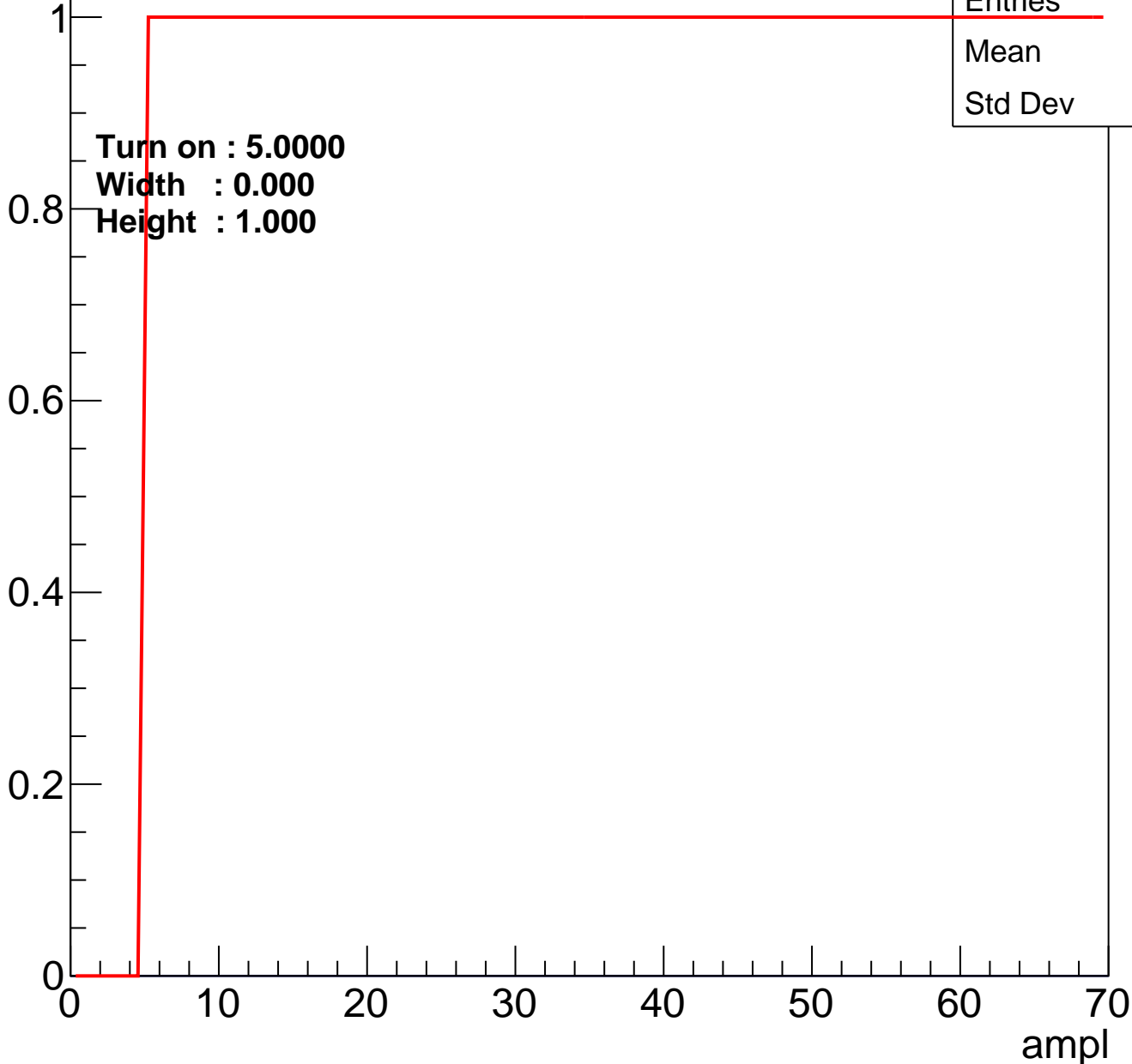
Height : 2.222



B0L100S, U8-ch55

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U8-ch56

calib_packv5_042523_0143.root, FC#6, port A1

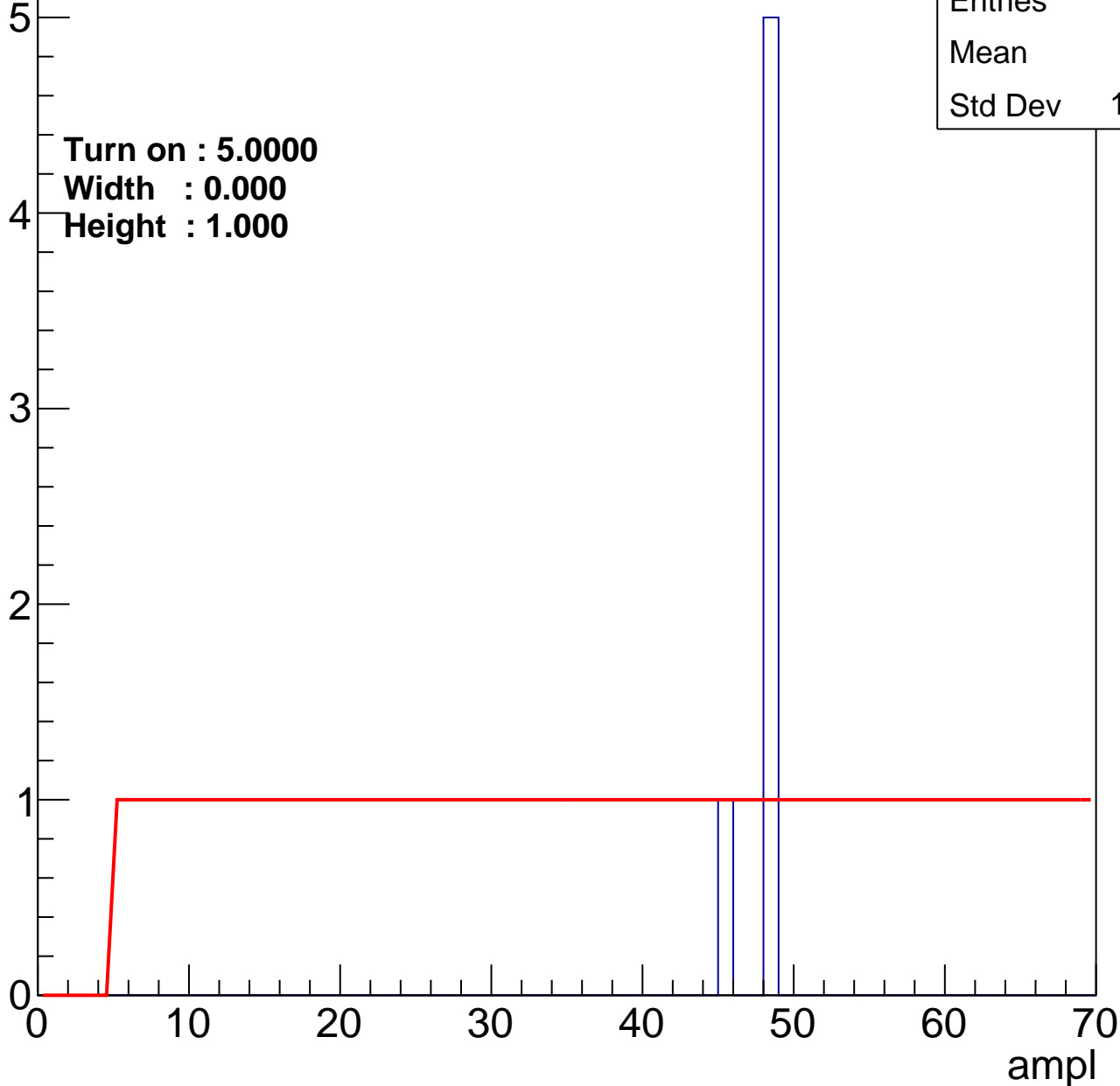
Entry

Entries	6
Mean	47.5
Std Dev	1.118

Turn on : 5.0000

Width : 0.000

Height : 1.000



B0L100S, U8-ch57

calib_packv5_042523_0143.root, FC#6, port A1

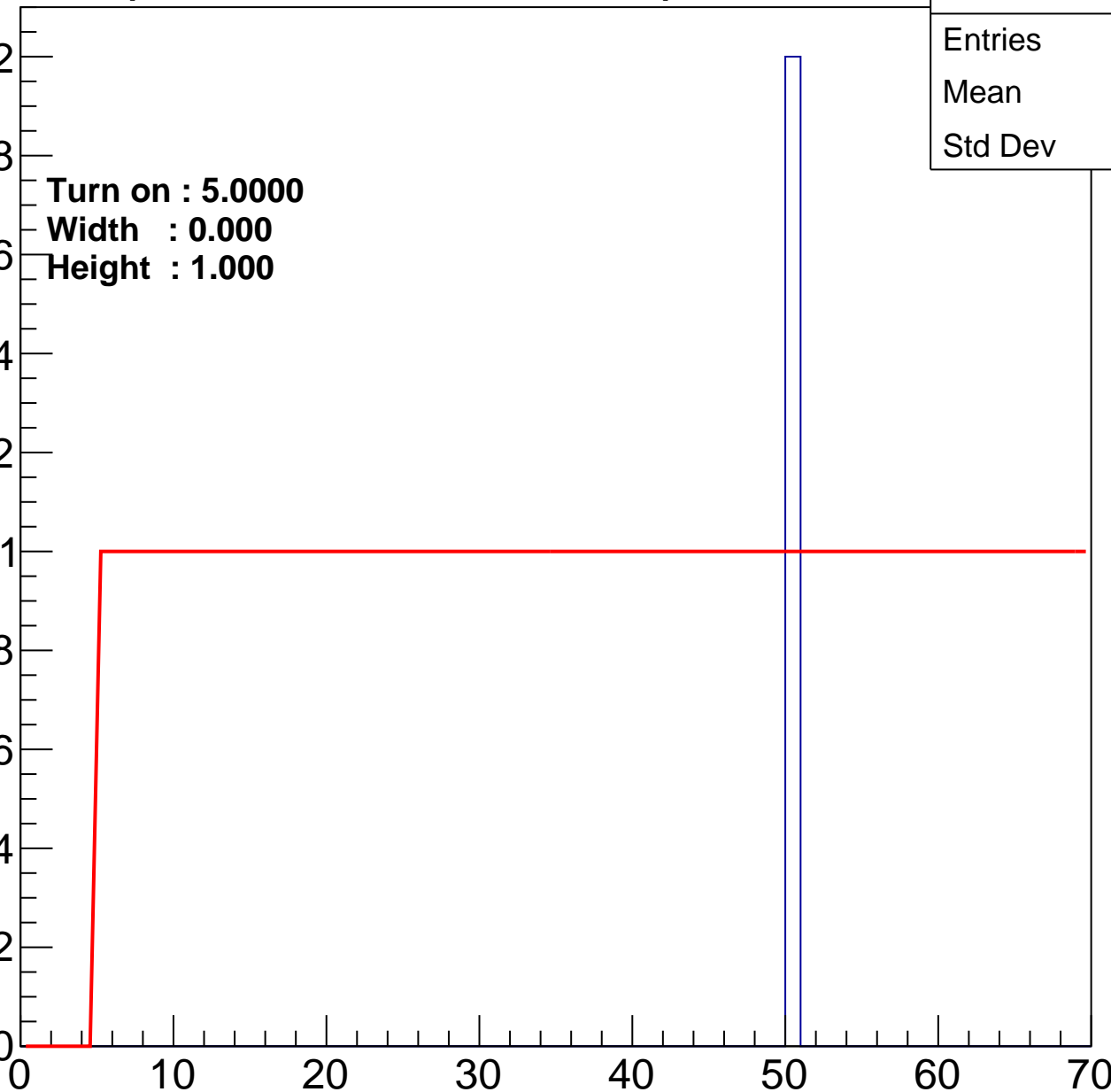
Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Turn on : 5.0000
Width : 0.000
Height : 1.000

Entries	2
Mean	50
Std Dev	0

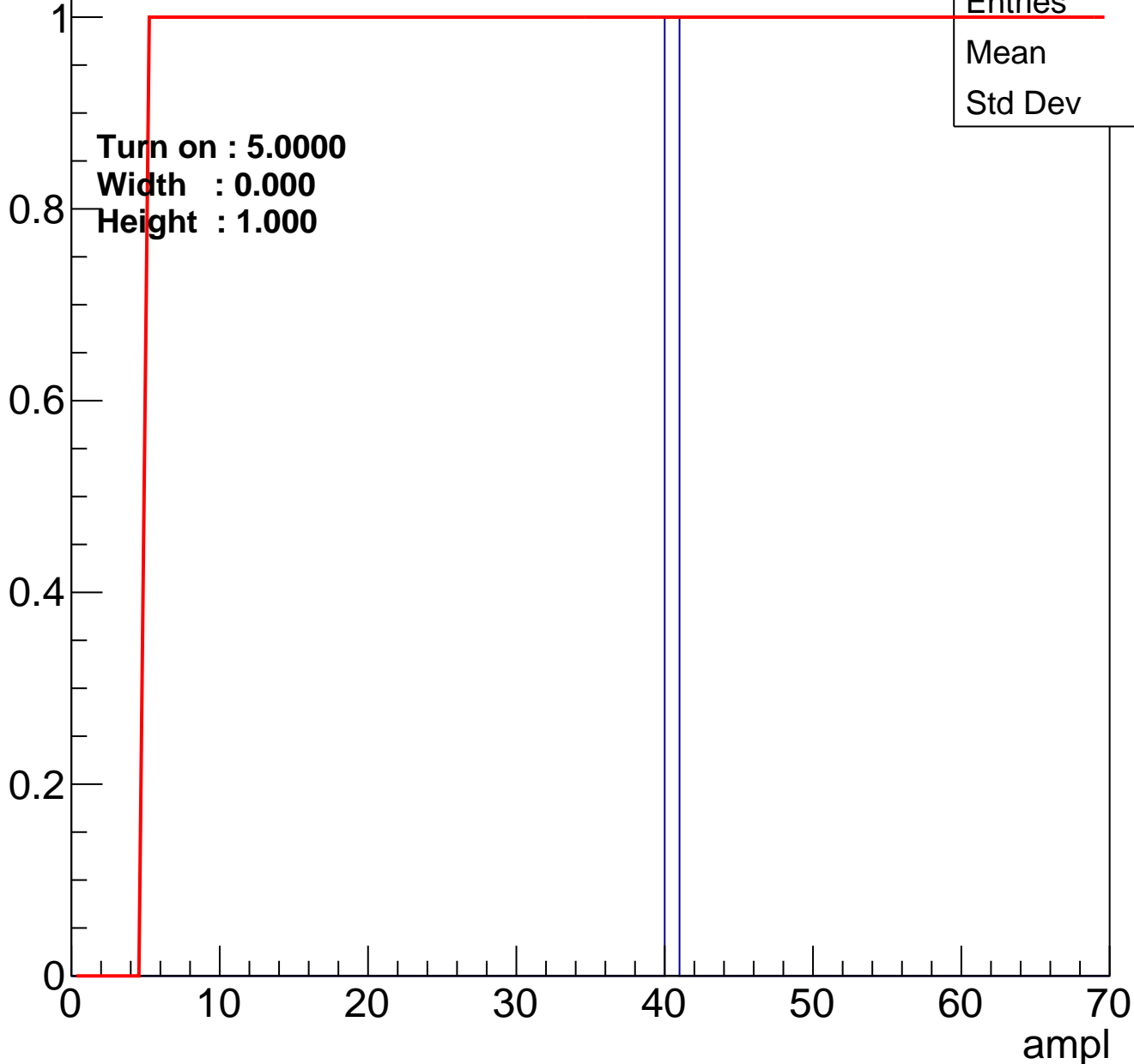
ampl



B0L100S, U8-ch58

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U8-ch59

calib_packv5_042523_0143.root, FC#6, port A1

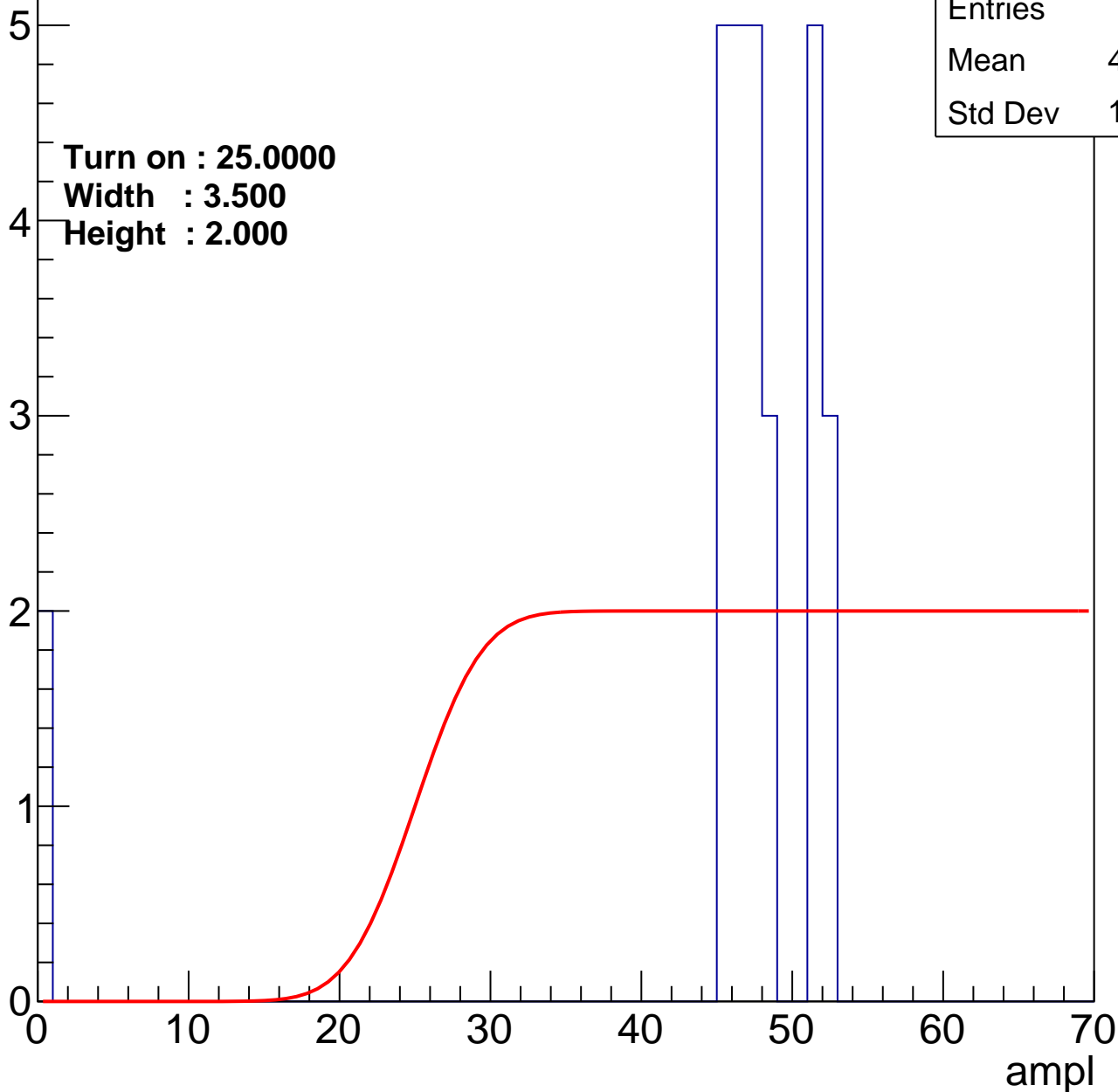
Entry

Entries	28
Mean	44.46
Std Dev	12.57

Turn on : 25.0000

Width : 3.500

Height : 2.000



B0L100S, U8-ch60

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U8-ch61

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U8-ch62

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U8-ch63

calib_packv5_042523_0143.root, FC#6, port A1

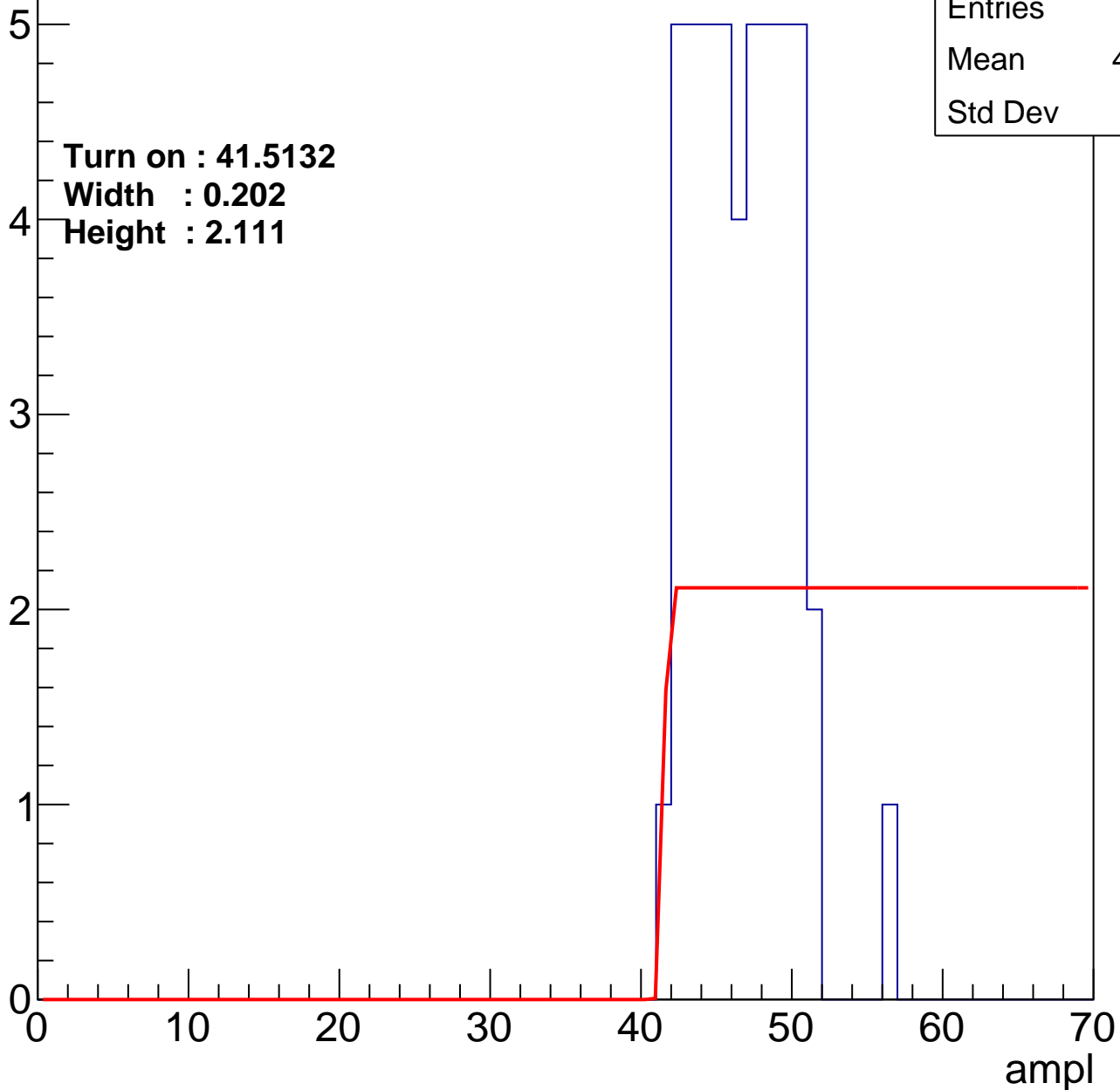
Entry

Entries	48
Mean	46.31
Std Dev	3.13

Turn on : 41.5132

Width : 0.202

Height : 2.111



B0L100S, U8-ch64

calib_packv5_042523_0143.root, FC#6, port A1

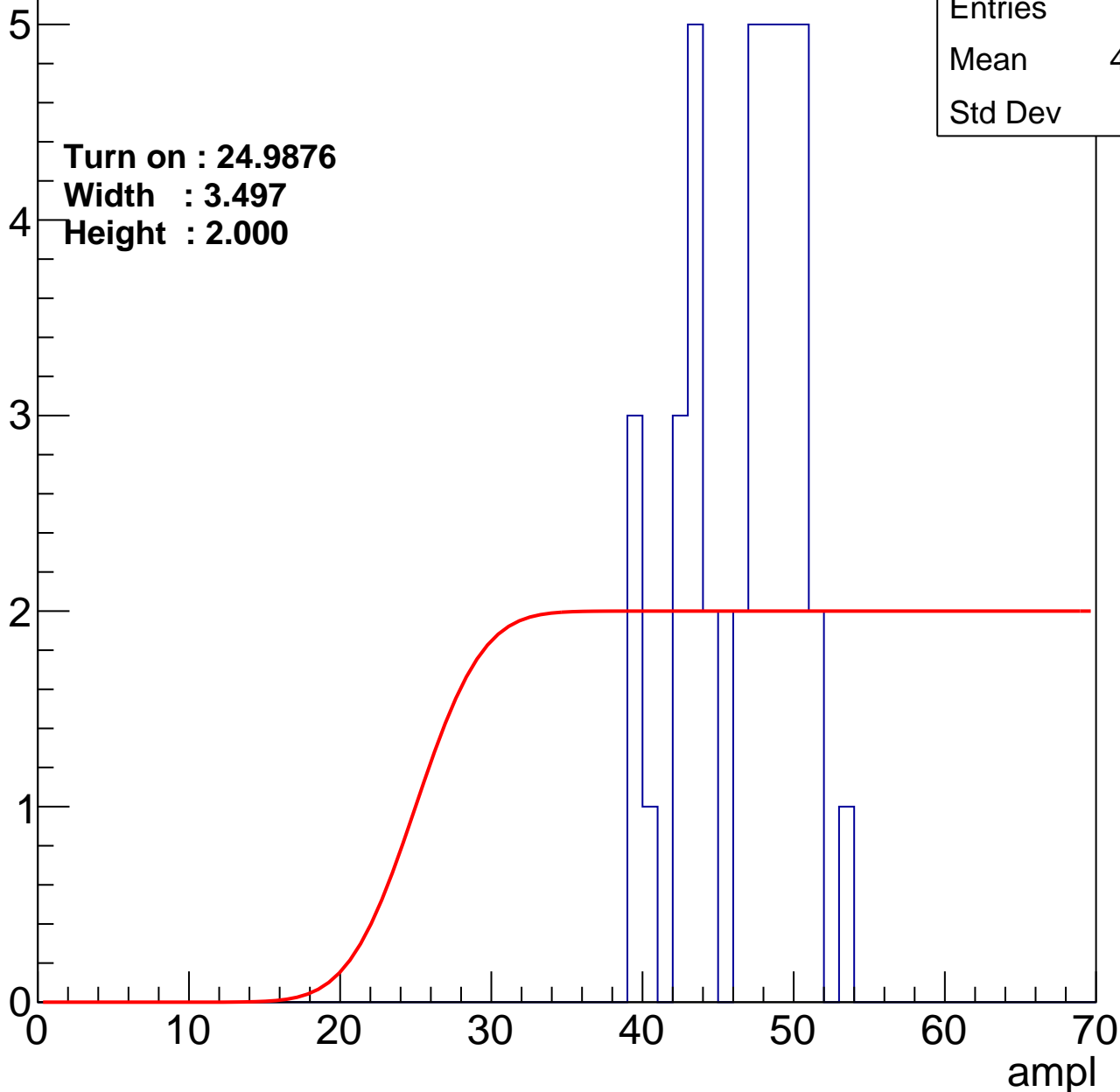
Entry

Entries	39
Mean	46.23
Std Dev	3.69

Turn on : 24.9876

Width : 3.497

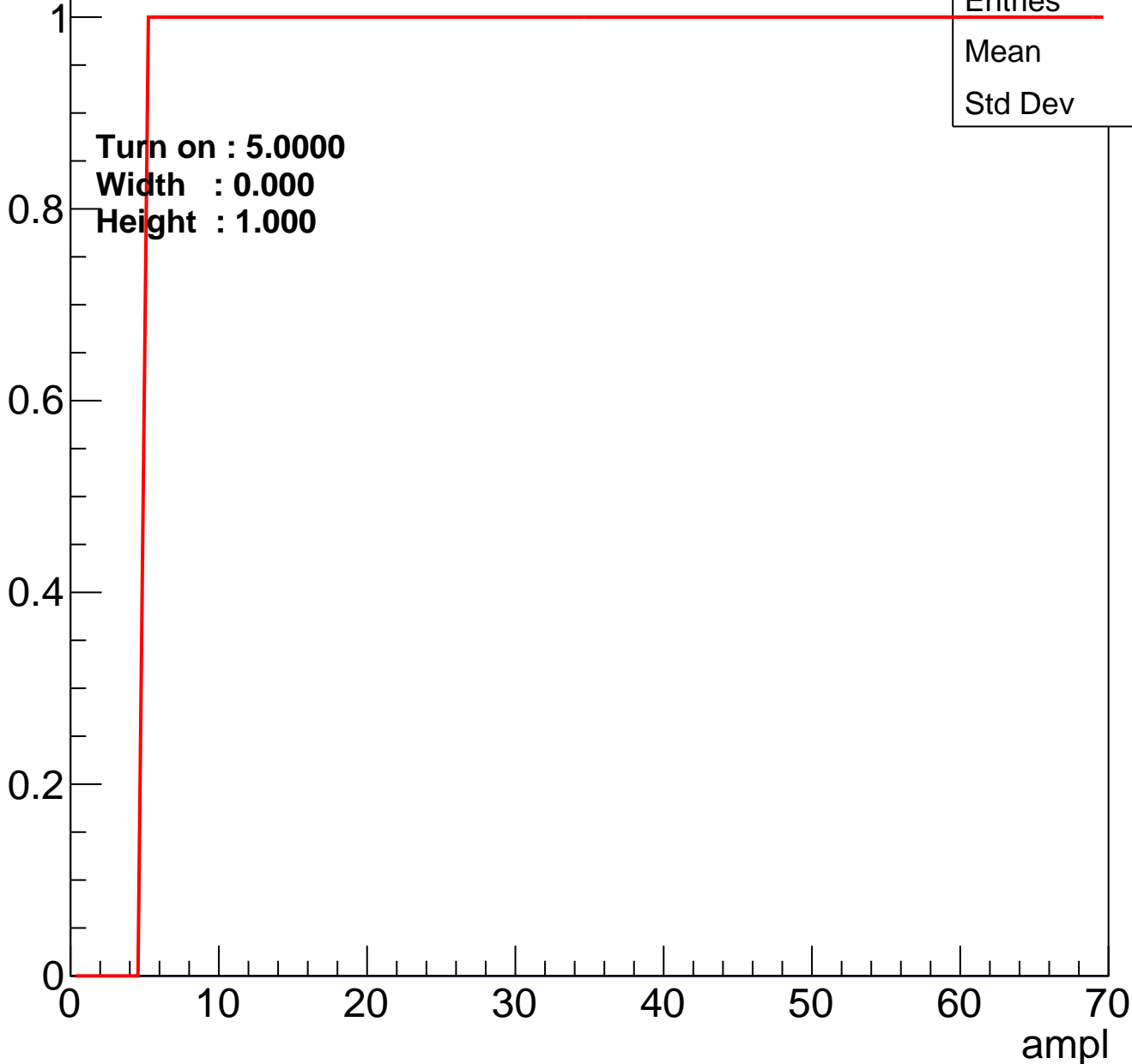
Height : 2.000



B0L100S, U8-ch65

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U8-ch66

calib_packv5_042523_0143.root, FC#6, port A1

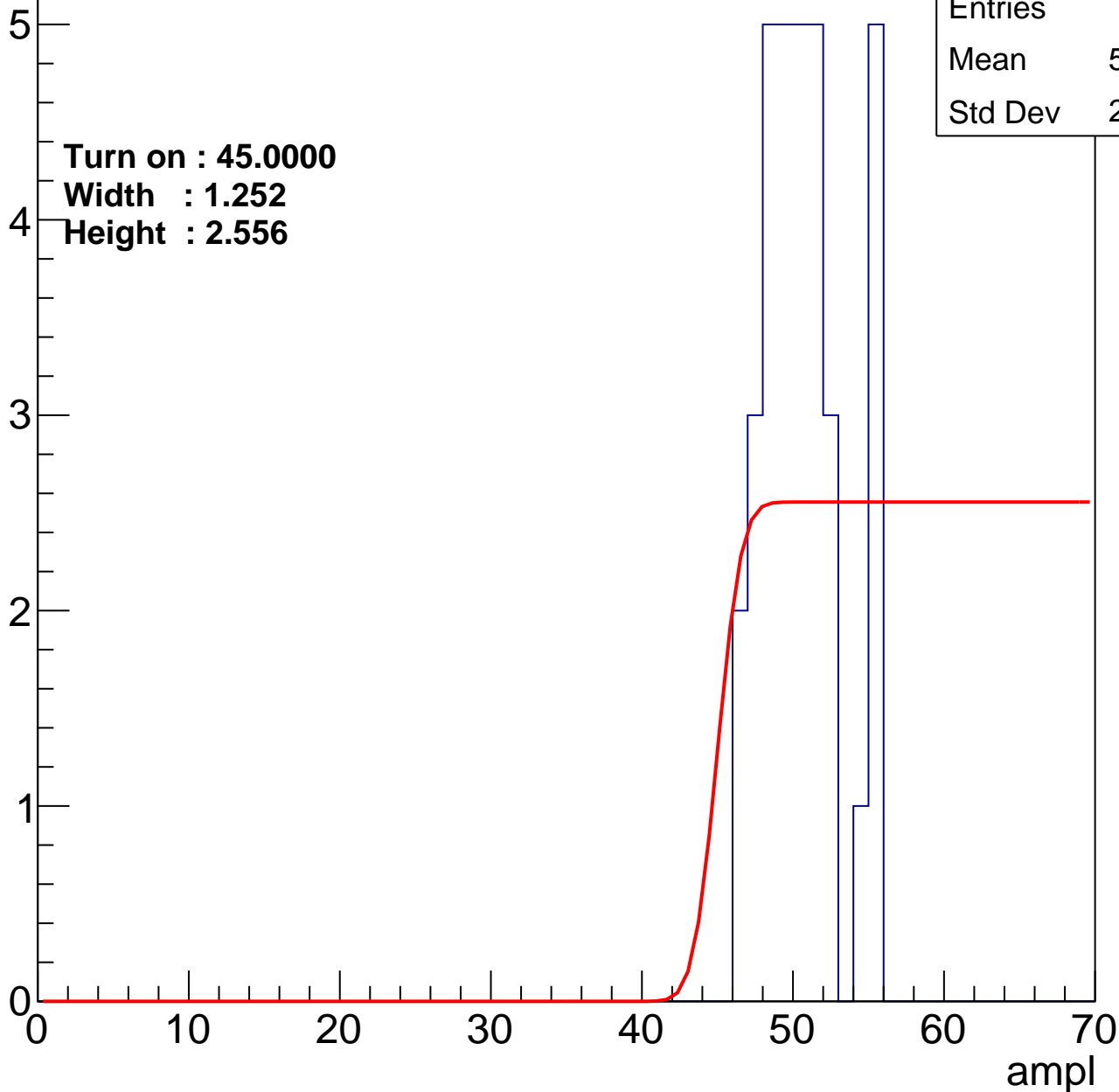
Entry

Entries	34
Mean	50.24
Std Dev	2.657

Turn on : 45.0000

Width : 1.252

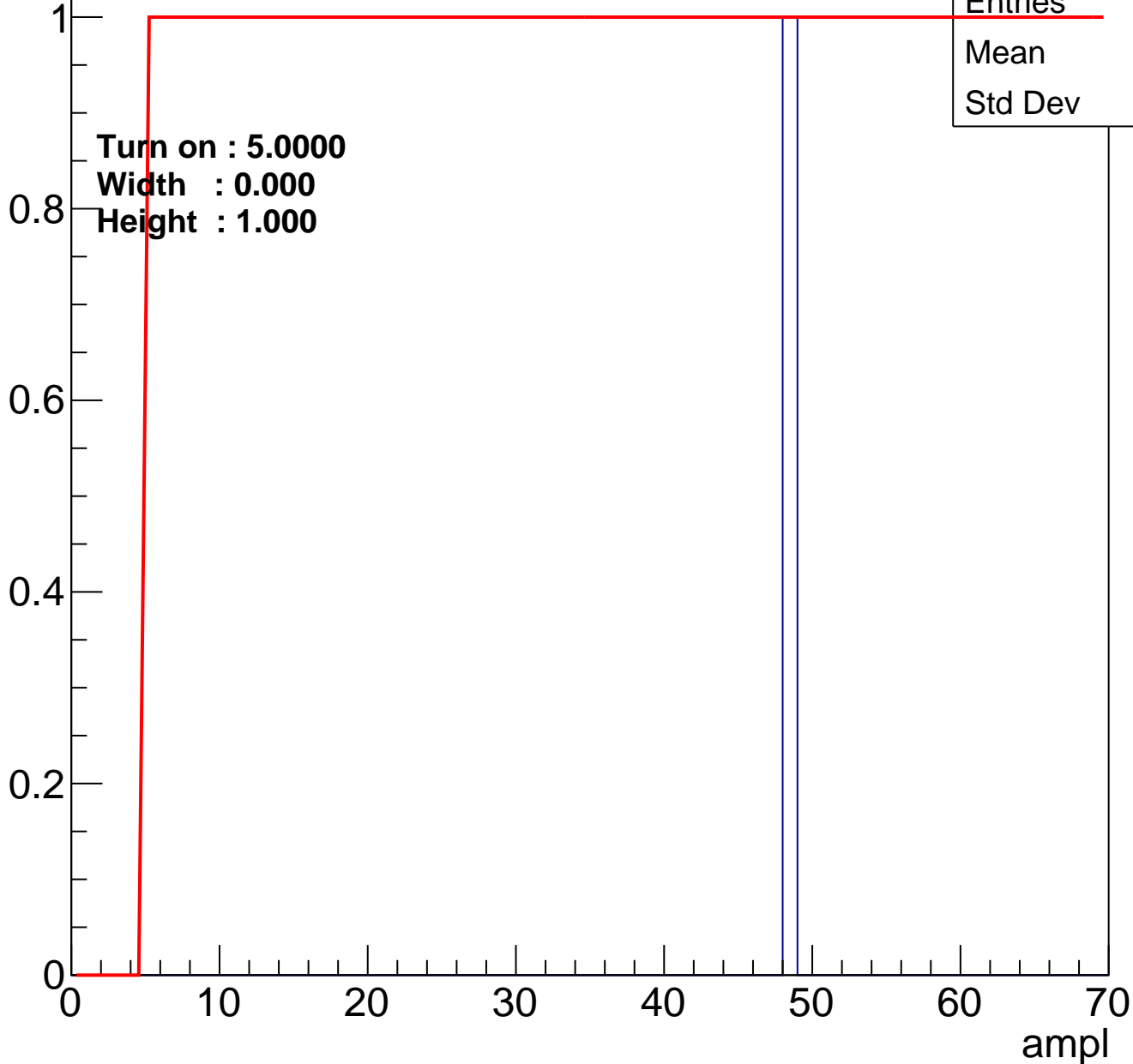
Height : 2.556



B0L100S, U8-ch67

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U8-ch68

calib_packv5_042523_0143.root, FC#6, port A1

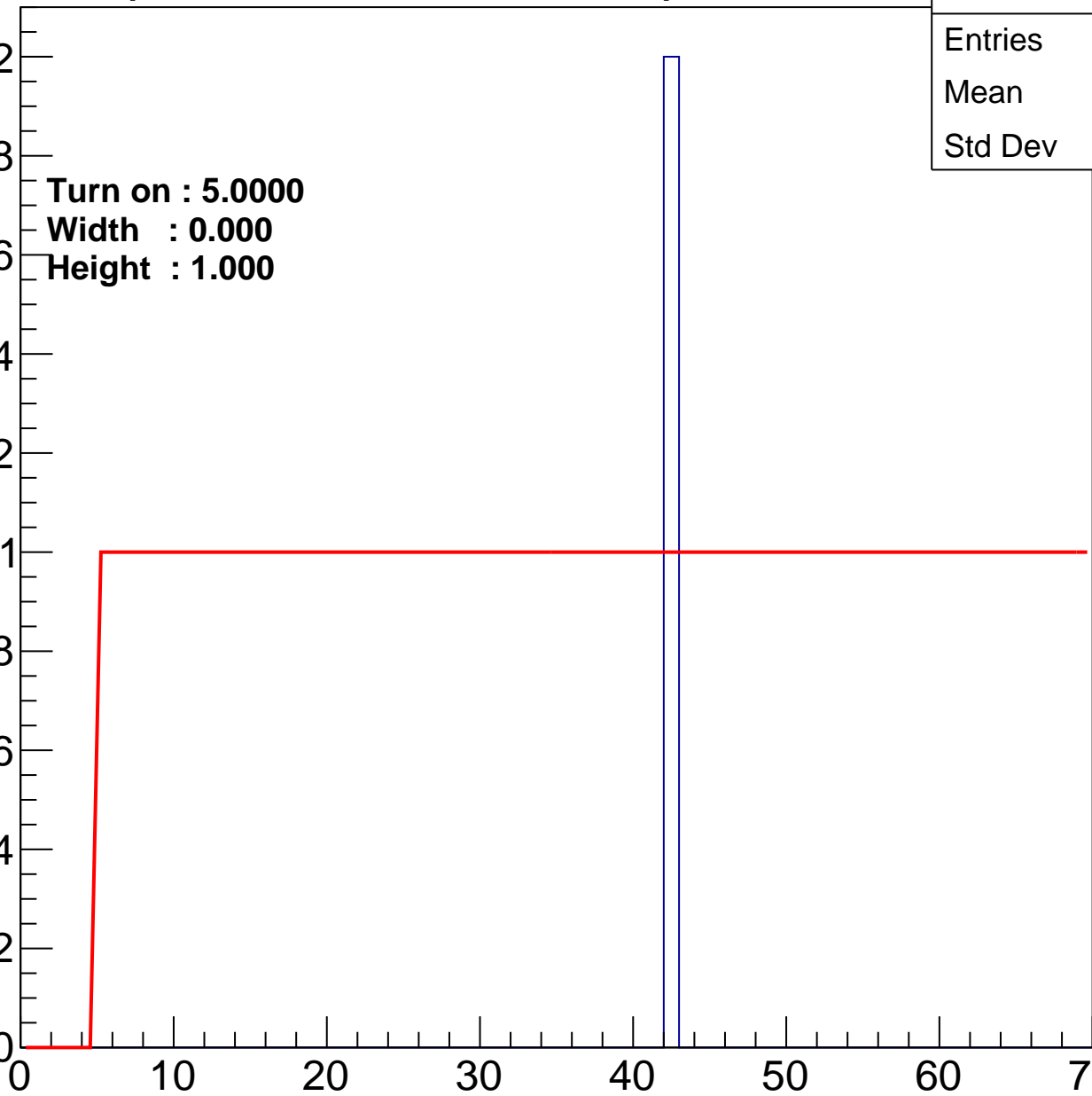
Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Turn on : 5.0000
Width : 0.000
Height : 1.000

Entries	2
Mean	42
Std Dev	0

ampl



B0L100S, U8-ch69

calib_packv5_042523_0143.root, FC#6, port A1

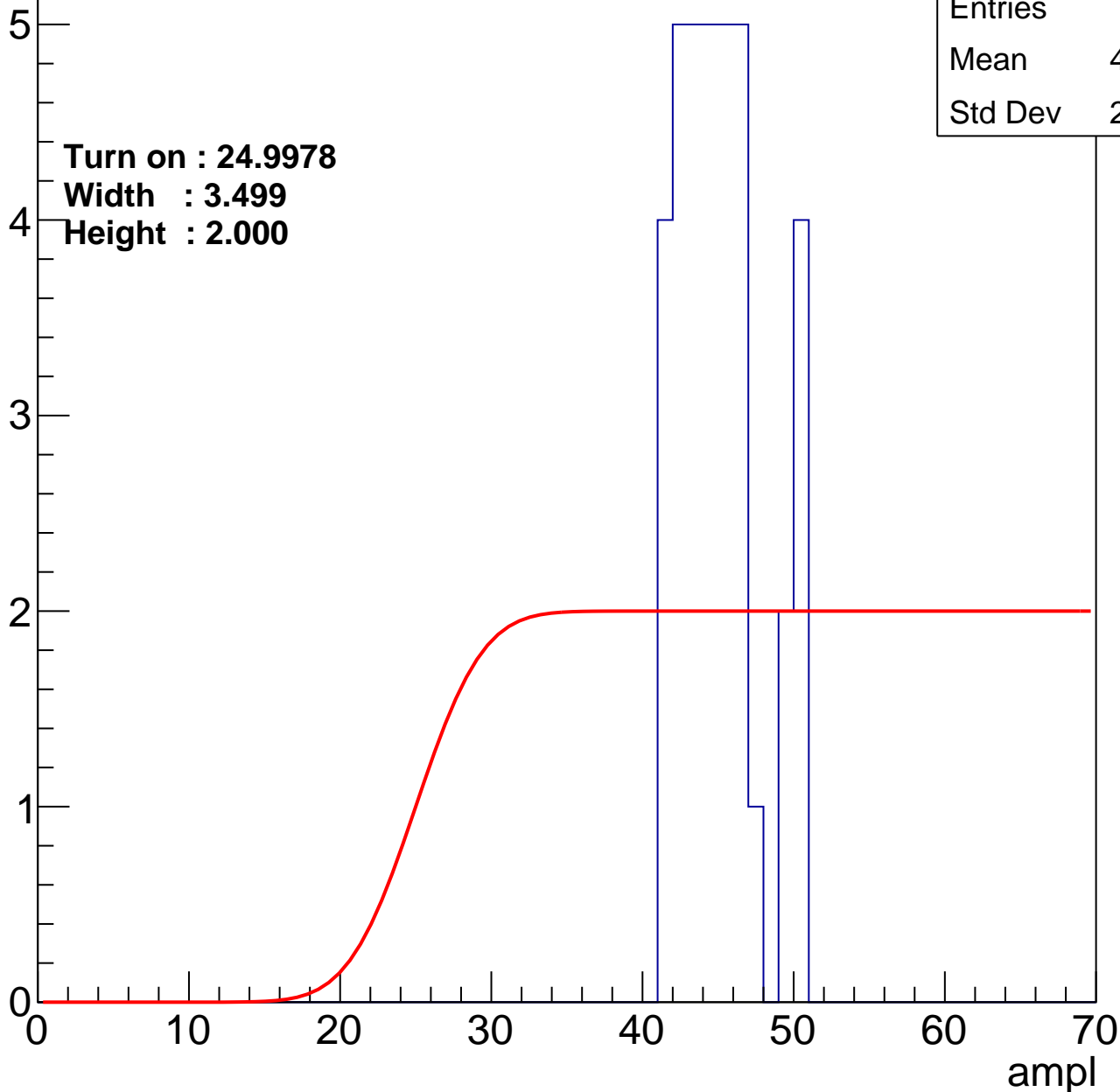
Entry

Entries	36
Mean	44.69
Std Dev	2.747

Turn on : 24.9978

Width : 3.499

Height : 2.000



B0L100S, U8-ch70

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U8-ch71

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U8-ch72

calib_packv5_042523_0143.root, FC#6, port A1

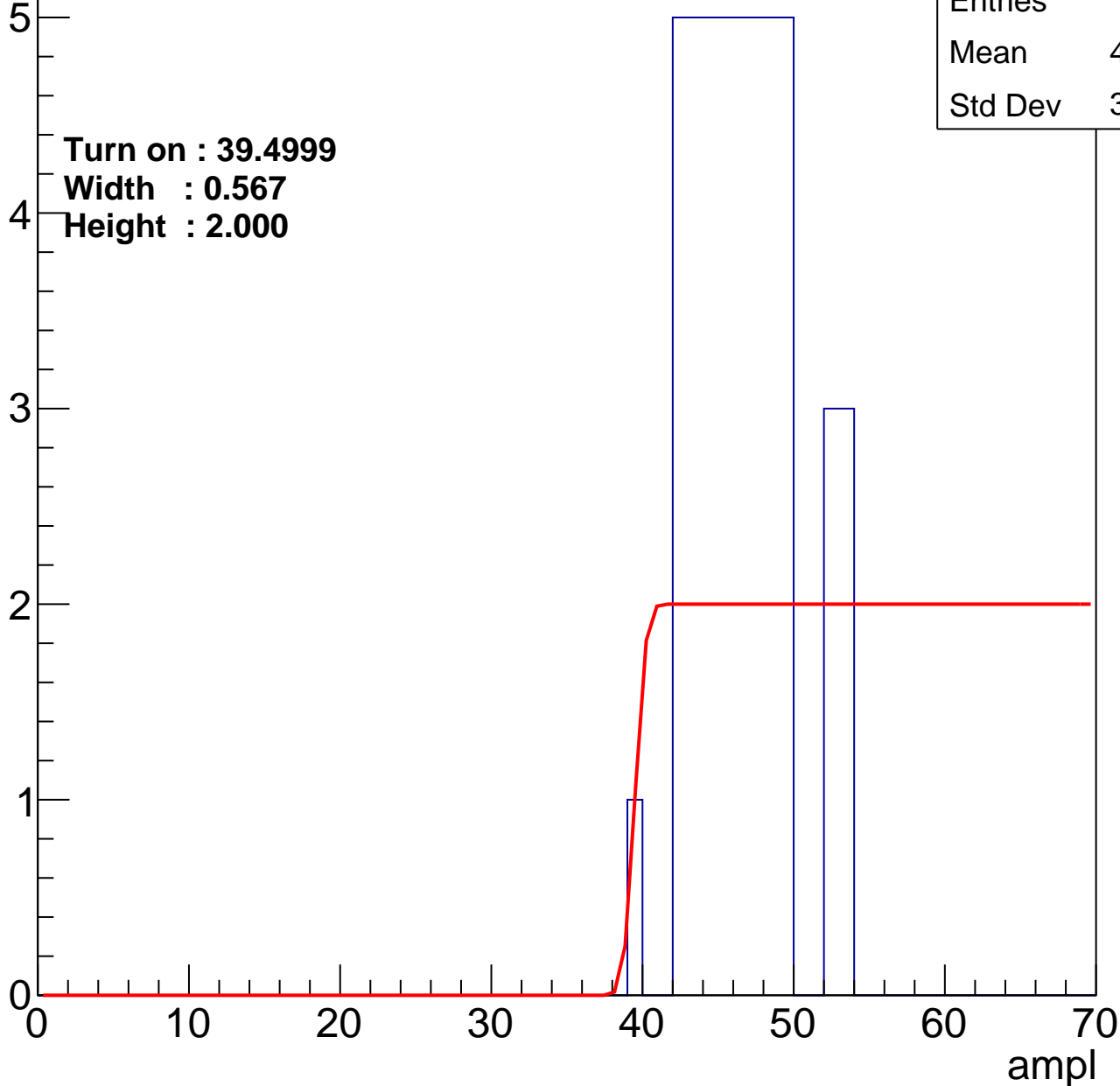
Entry

Entries	47
Mean	46.26
Std Dev	3.329

Turn on : 39.4999

Width : 0.567

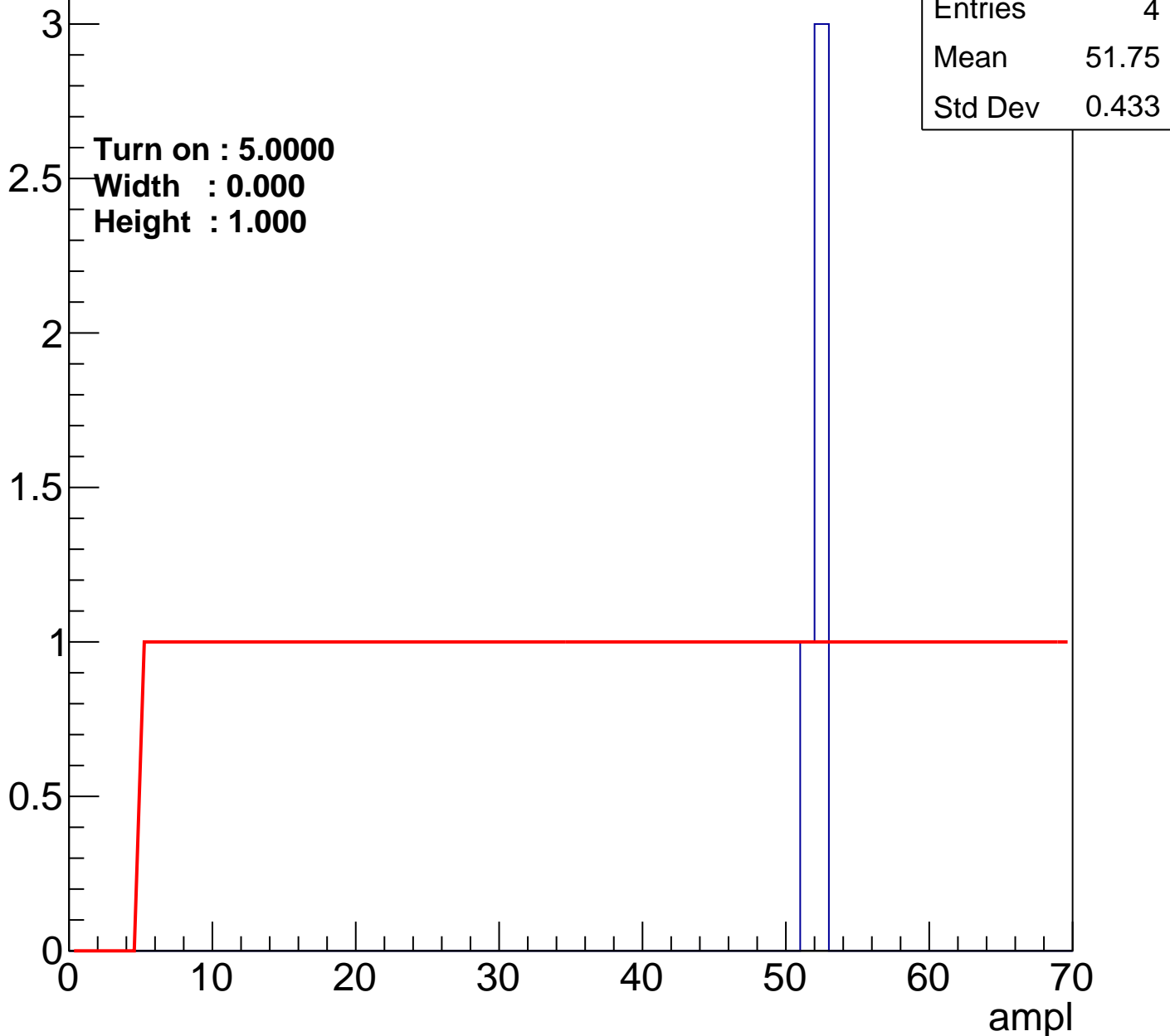
Height : 2.000



B0L100S, U8-ch73

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U8-ch74

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U8-ch75

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U8-ch76

calib_packv5_042523_0143.root, FC#6, port A1

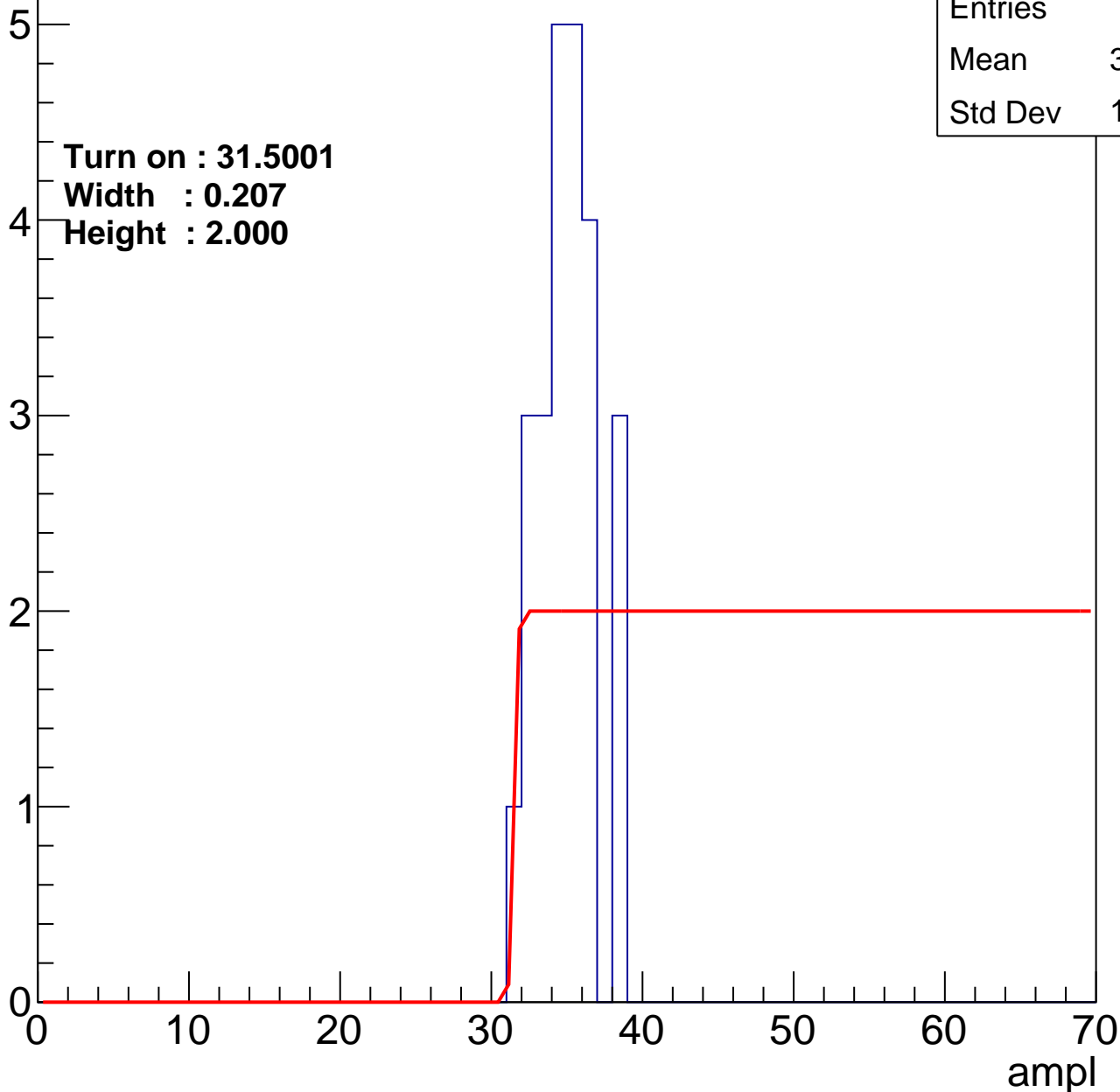
Entry

Entries	24
Mean	34.54
Std Dev	1.893

Turn on : 31.5001

Width : 0.207

Height : 2.000



B0L100S, U8-ch77

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U8-ch78

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U8-ch79

calib_packv5_042523_0143.root, FC#6, port A1

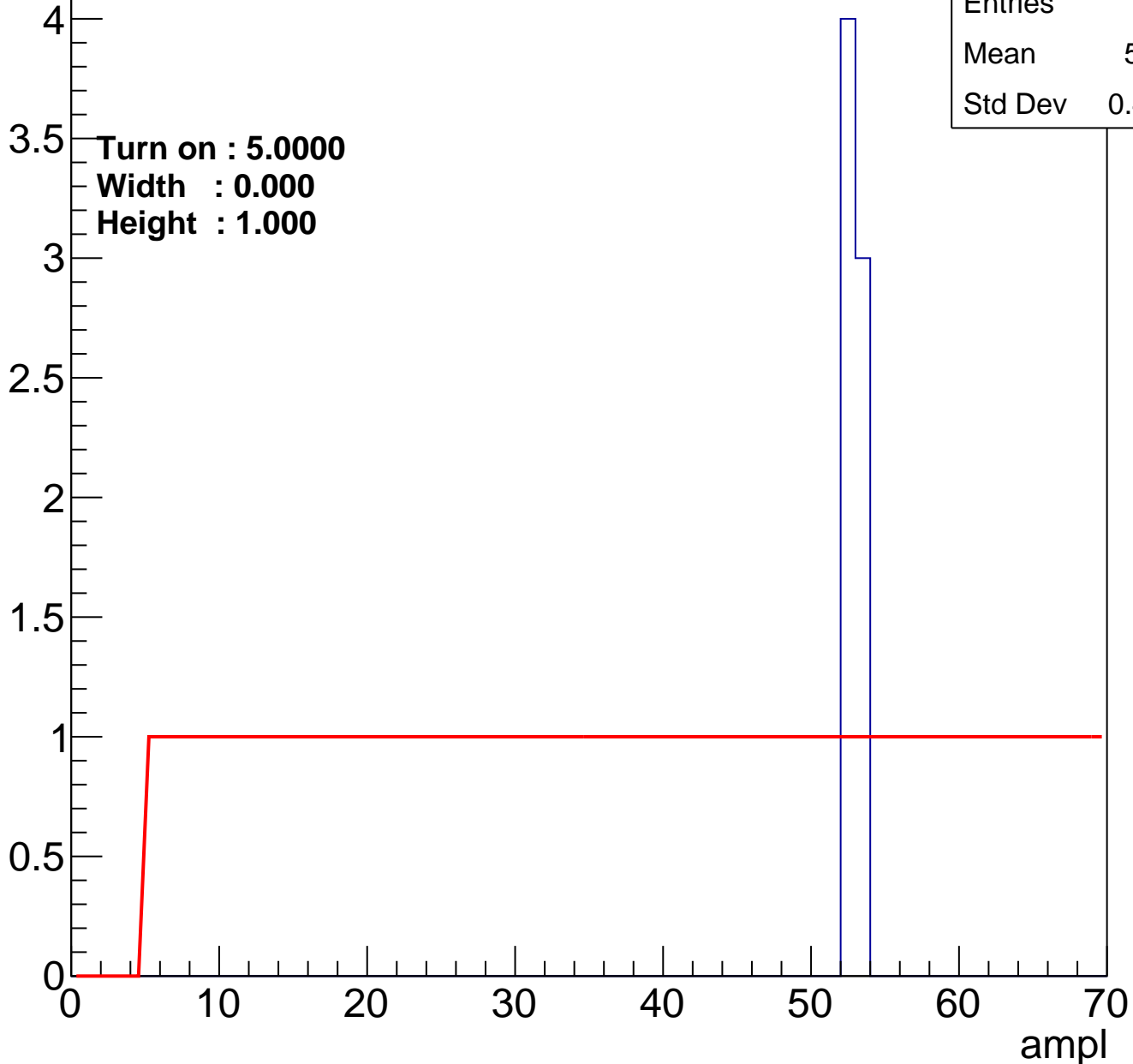
Entry



B0L100S, U8-ch80

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U8-ch81

calib_packv5_042523_0143.root, FC#6, port A1

Entry

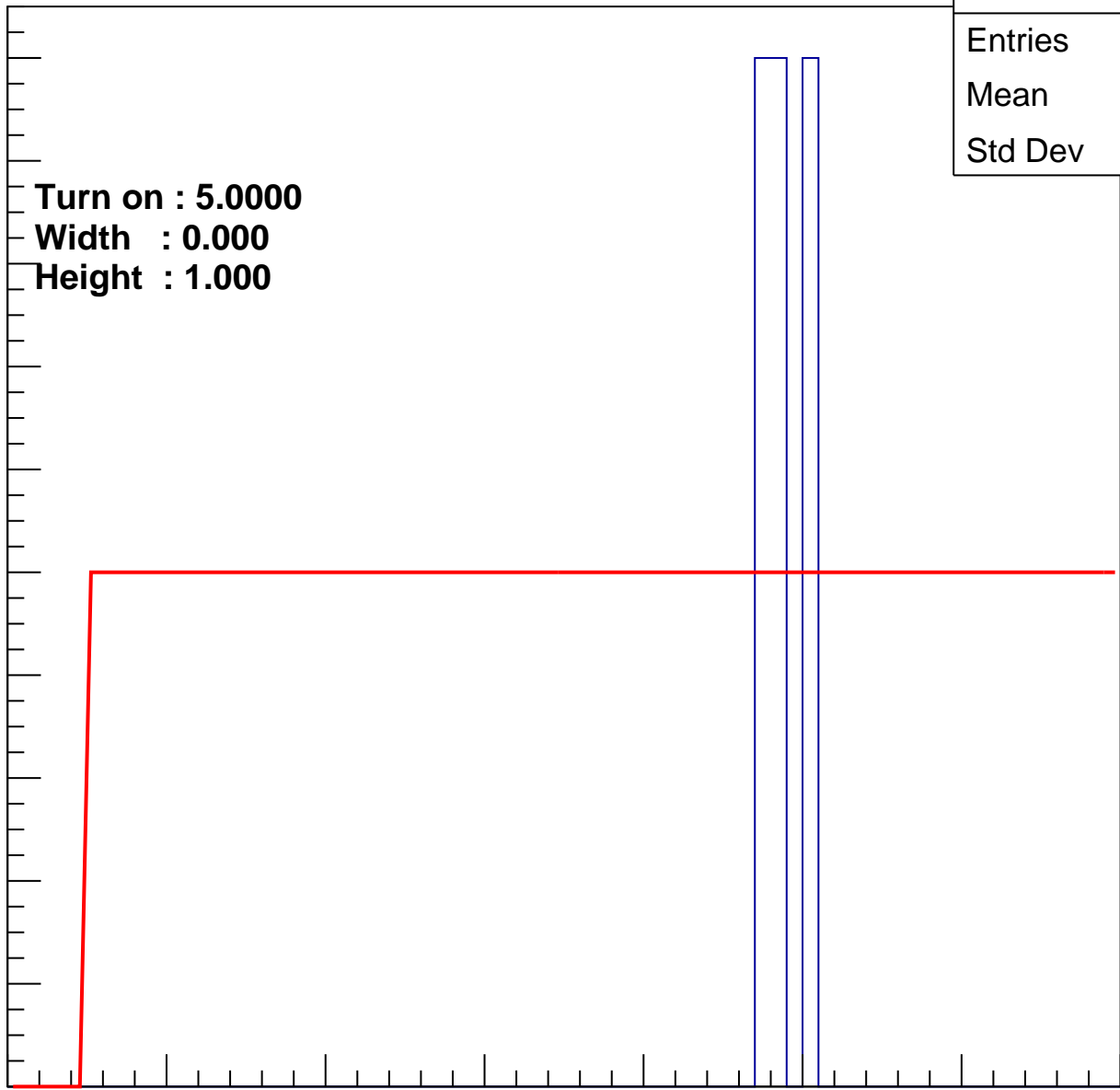
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Turn on : 5.0000
Width : 0.000
Height : 1.000

Entries	6
Mean	48.33
Std Dev	1.247

0 10 20 30 40 50 60 70

ampl



B0L100S, U8-ch82

calib_packv5_042523_0143.root, FC#6, port A1

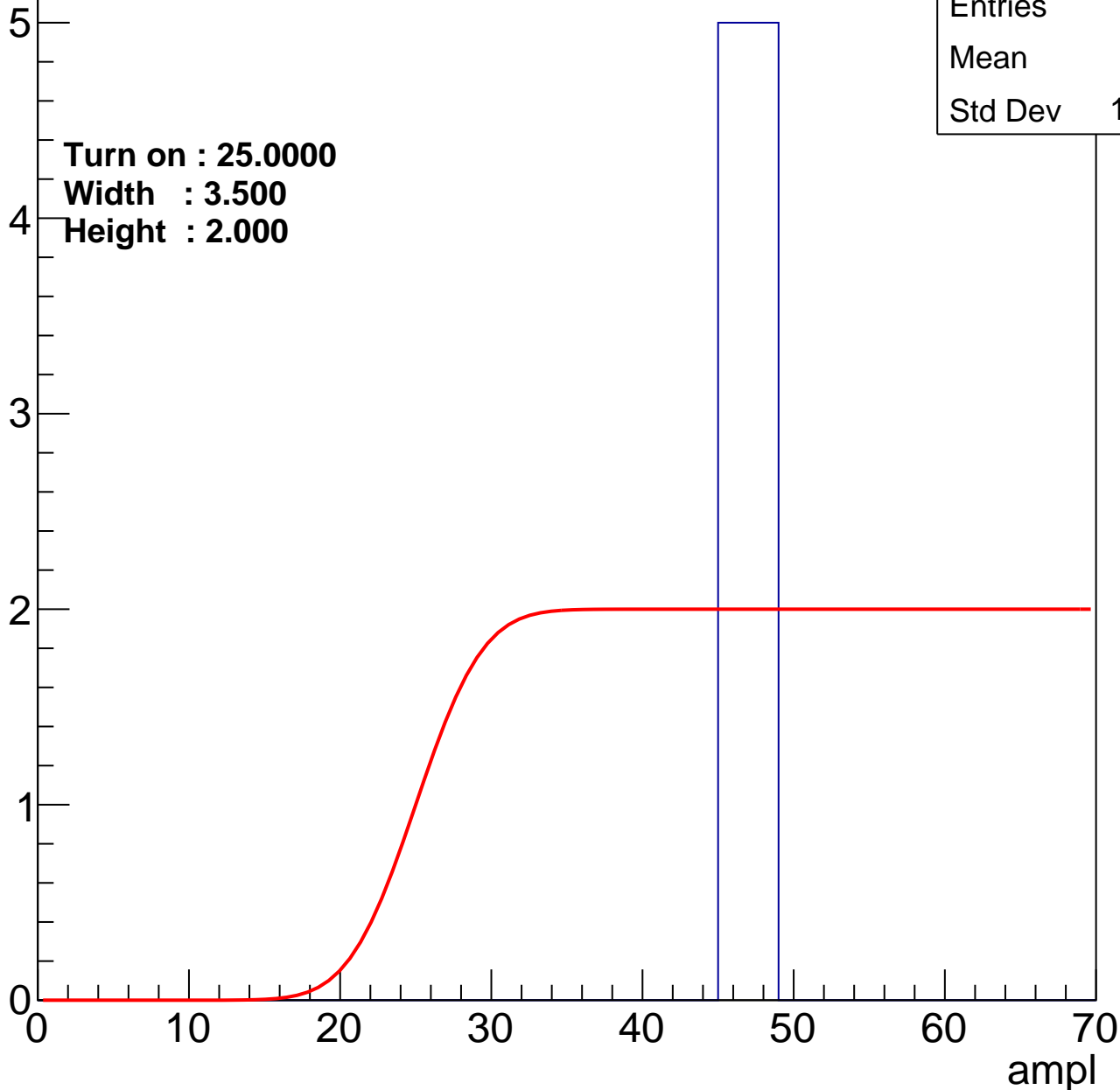
Entry

Entries	20
Mean	46.5
Std Dev	1.118

Turn on : 25.0000

Width : 3.500

Height : 2.000



B0L100S, U8-ch83

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U8-ch84

calib_packv5_042523_0143.root, FC#6, port A1

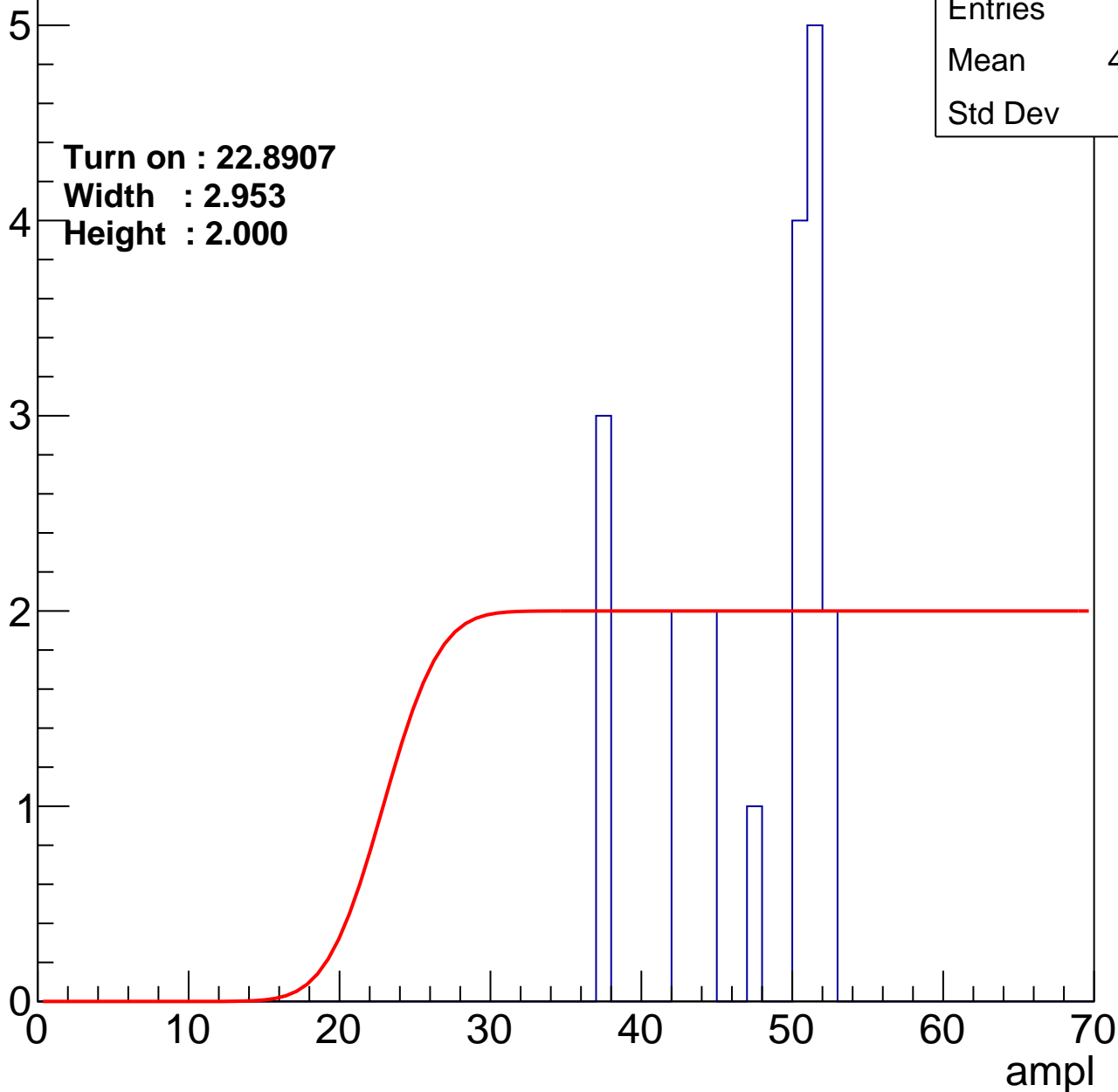
Entry

Entries	21
Mean	46.43
Std Dev	5.16

Turn on : 22.8907

Width : 2.953

Height : 2.000



B0L100S, U8-ch85

calib_packv5_042523_0143.root, FC#6, port A1

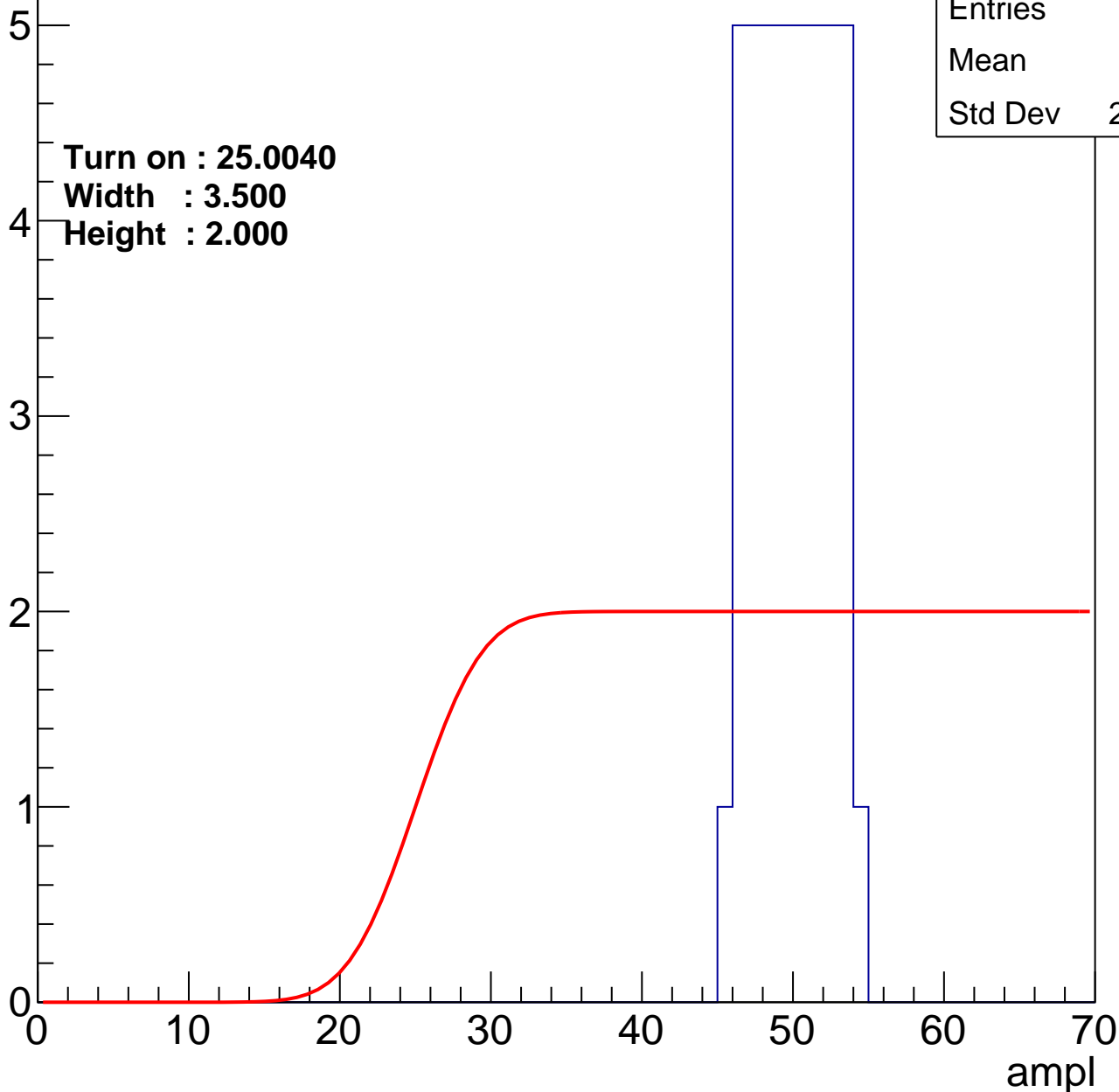
Entry

Entries	42
Mean	49.5
Std Dev	2.442

Turn on : 25.0040

Width : 3.500

Height : 2.000



B0L100S, U8-ch86

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U8-ch87

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U8-ch88

calib_packv5_042523_0143.root, FC#6, port A1

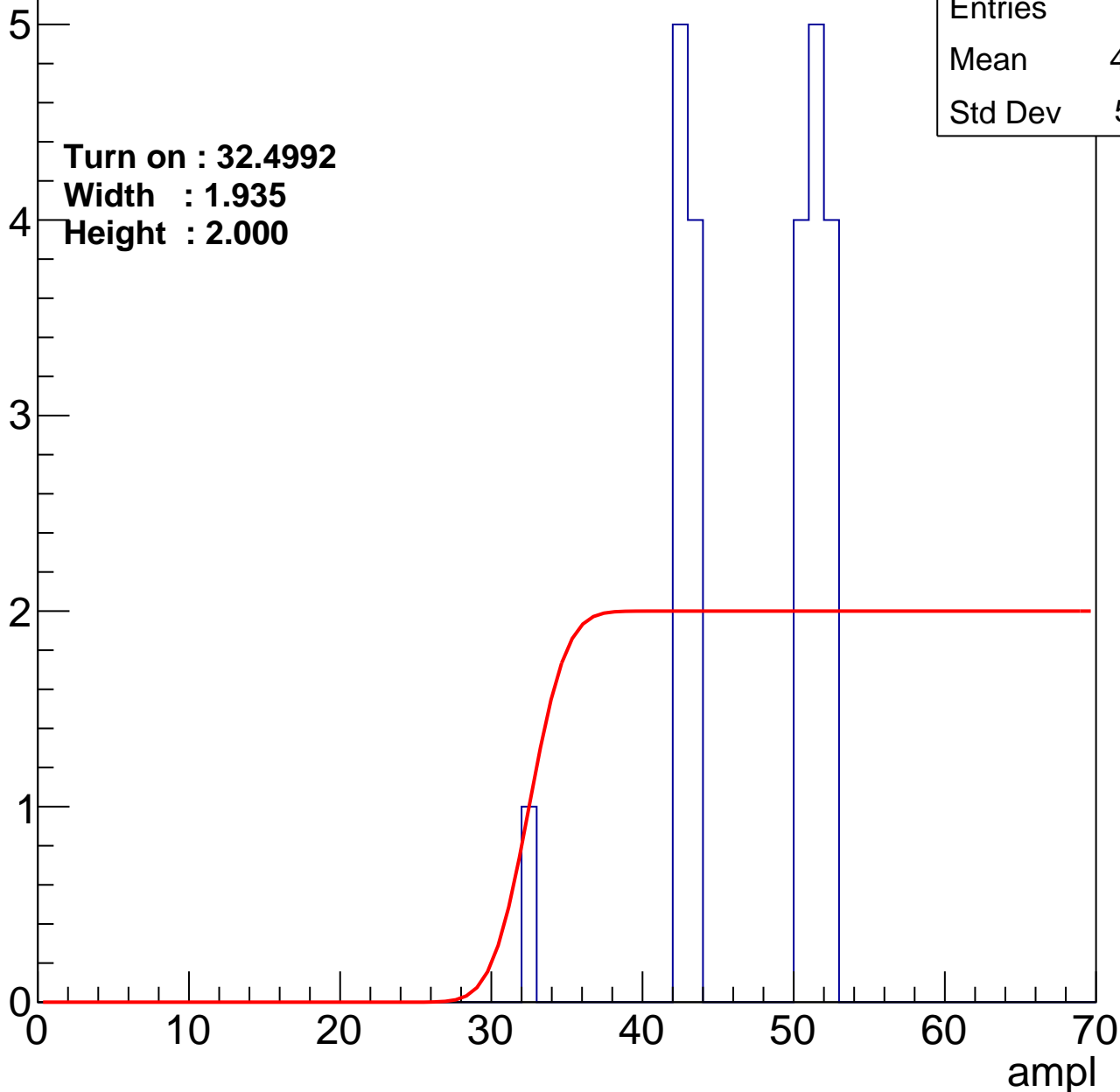
Entry

Entries	23
Mean	46.83
Std Dev	5.231

Turn on : 32.4992

Width : 1.935

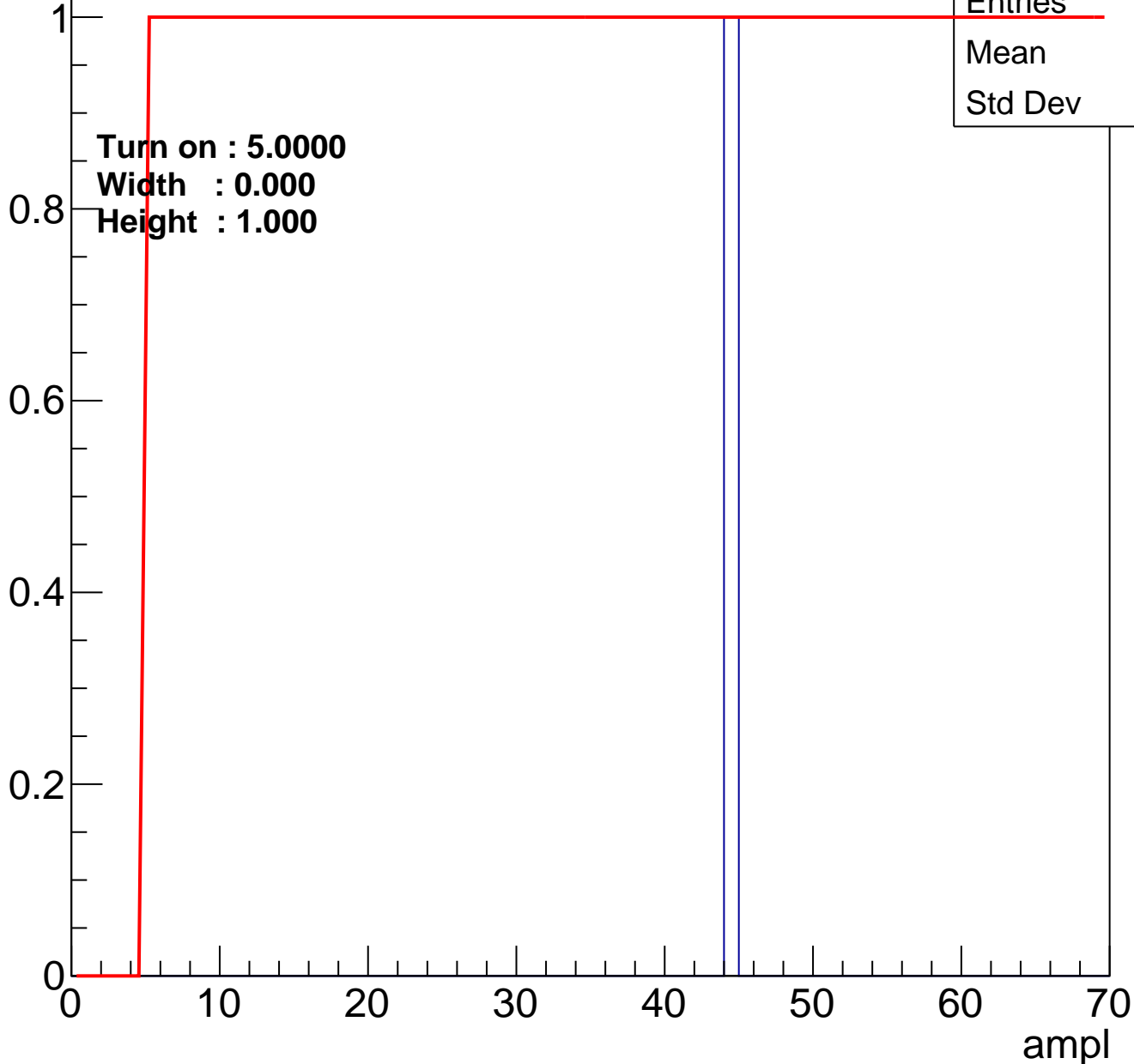
Height : 2.000



B0L100S, U8-ch89

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U8-ch90

calib_packv5_042523_0143.root, FC#6, port A1

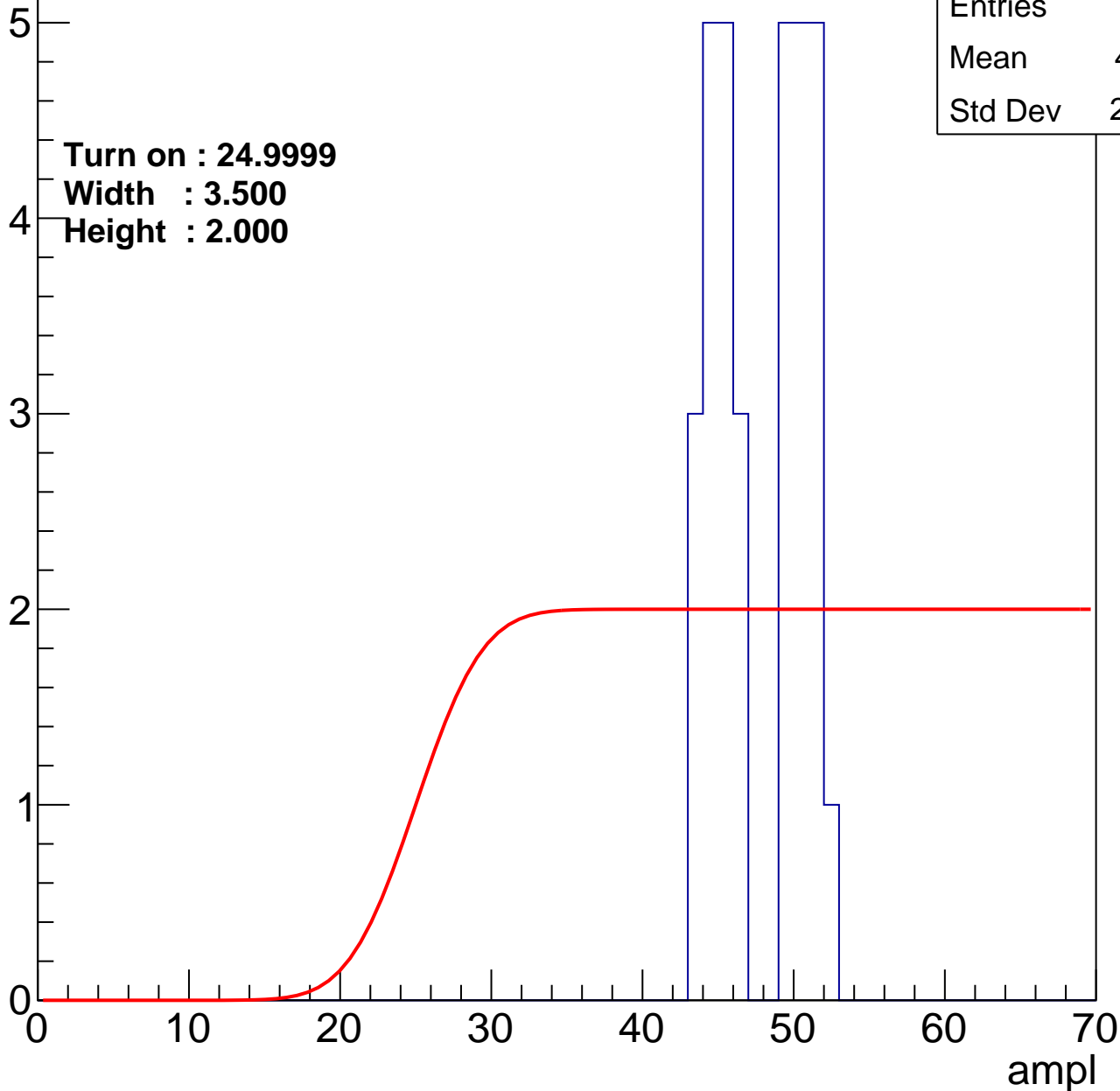
Entry

Entries	32
Mean	47.31
Std Dev	2.973

Turn on : 24.9999

Width : 3.500

Height : 2.000



B0L100S, U8-ch91

calib_packv5_042523_0143.root, FC#6, port A1

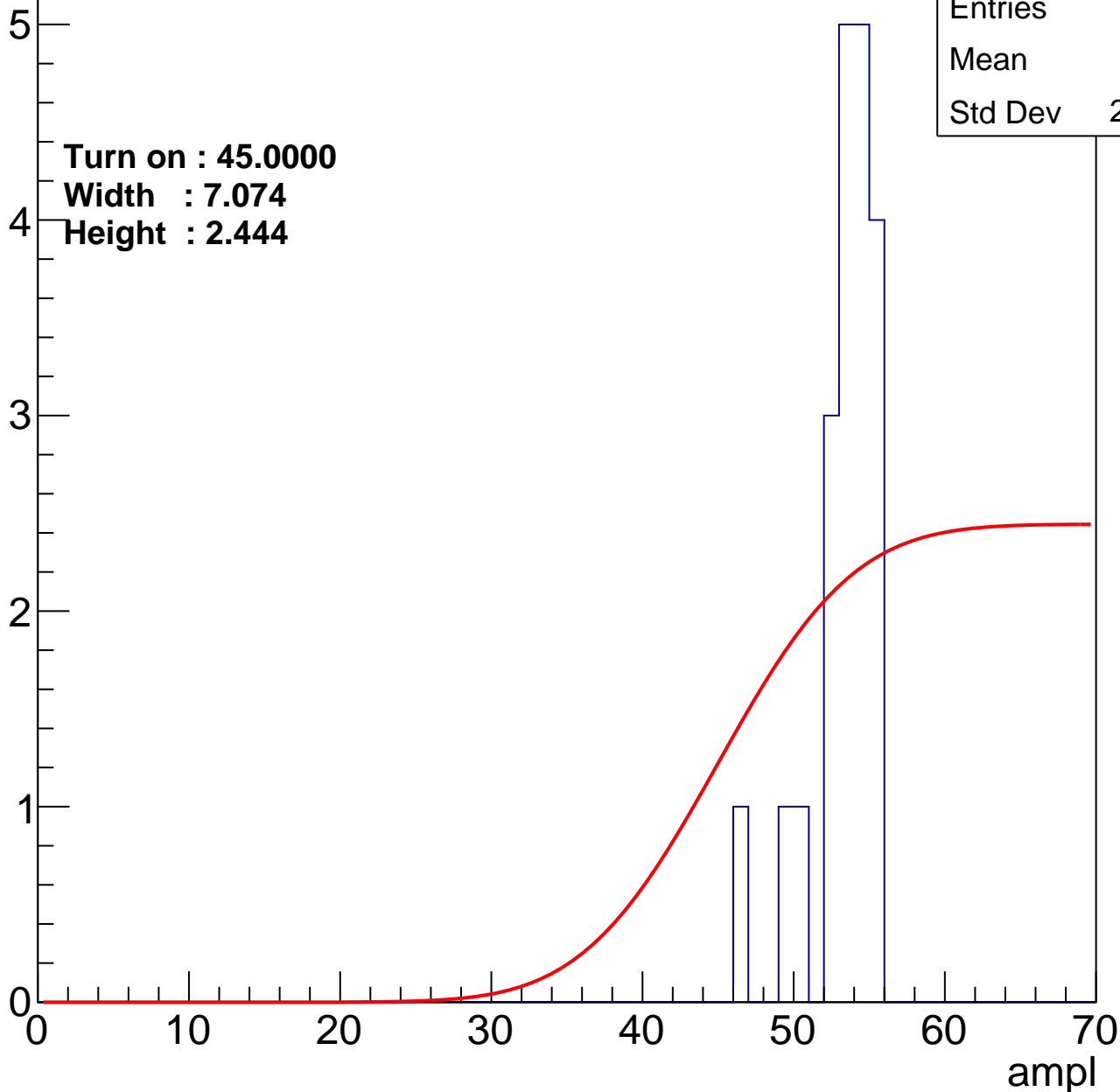
Entry

Entries	20
Mean	52.8
Std Dev	2.205

Turn on : 45.0000

Width : 7.074

Height : 2.444



B0L100S, U8-ch92

calib_packv5_042523_0143.root, FC#6, port A1

Entry

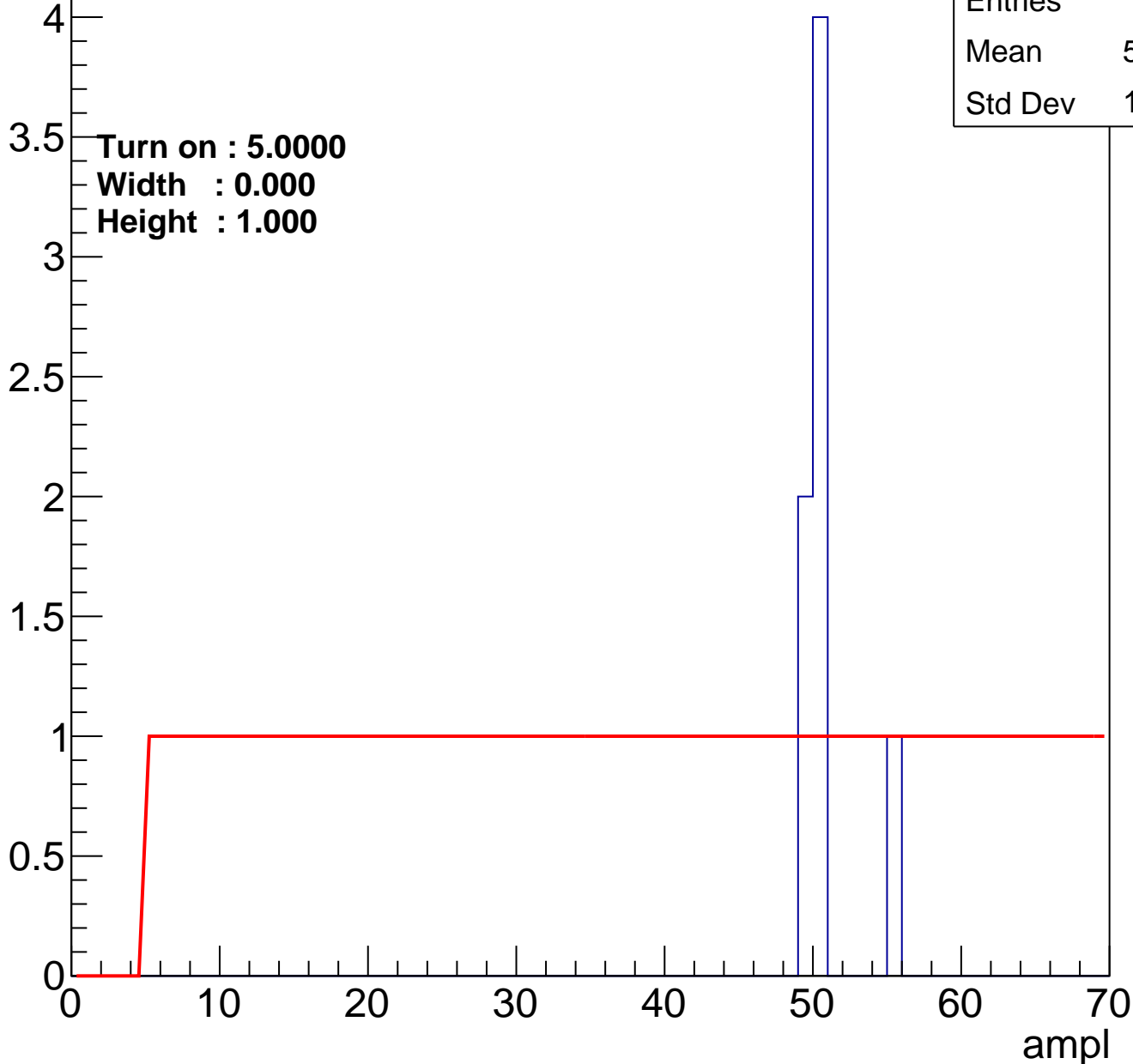


Entries	0
Mean	0
Std Dev	0

B0L100S, U8-ch93

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	7
Mean	50.43
Std Dev	1.917

B0L100S, U8-ch94

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U8-ch95

calib_packv5_042523_0143.root, FC#6, port A1

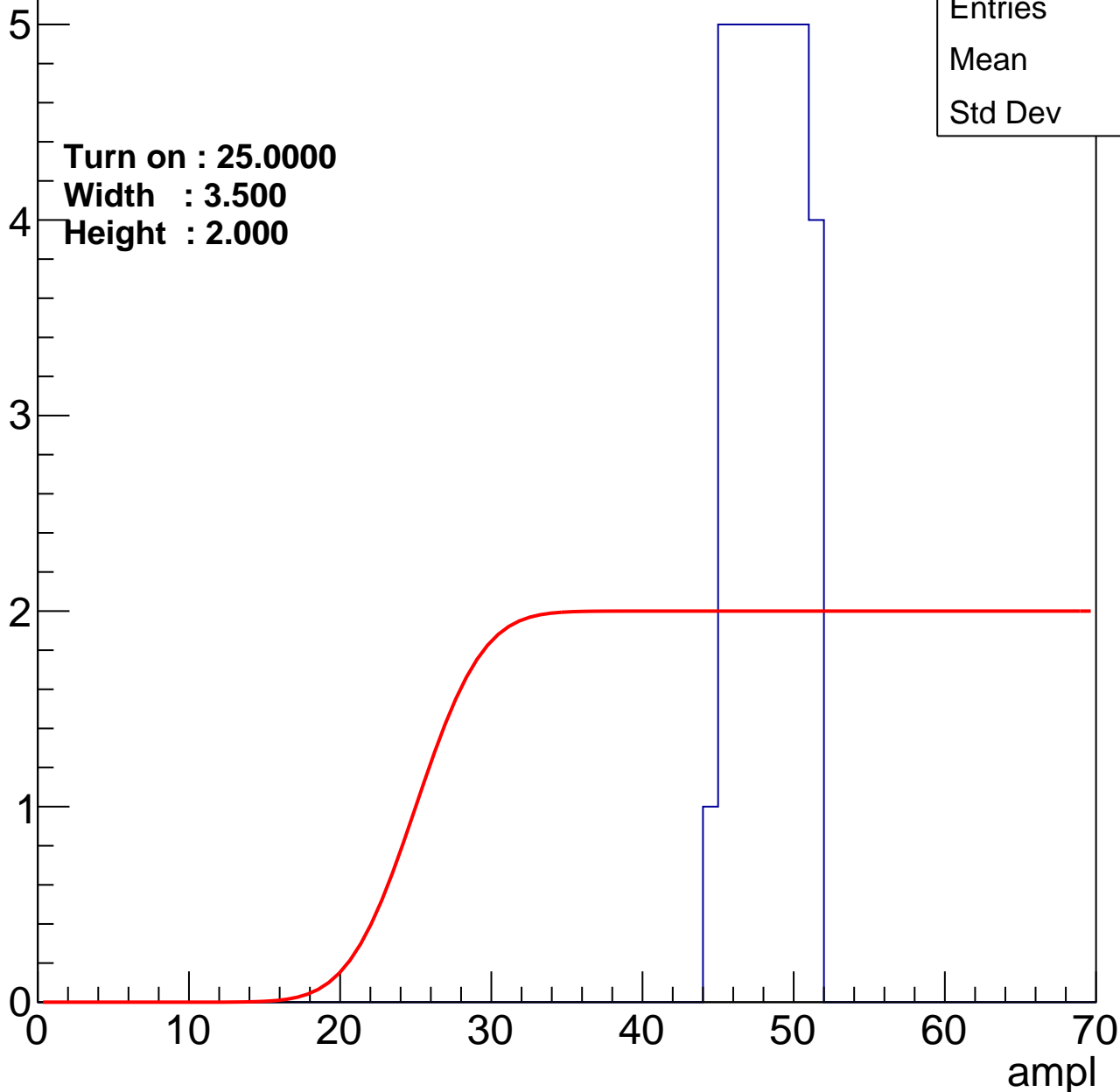
Entry

Entries	35
Mean	47.8
Std Dev	2.04

Turn on : 25.0000

Width : 3.500

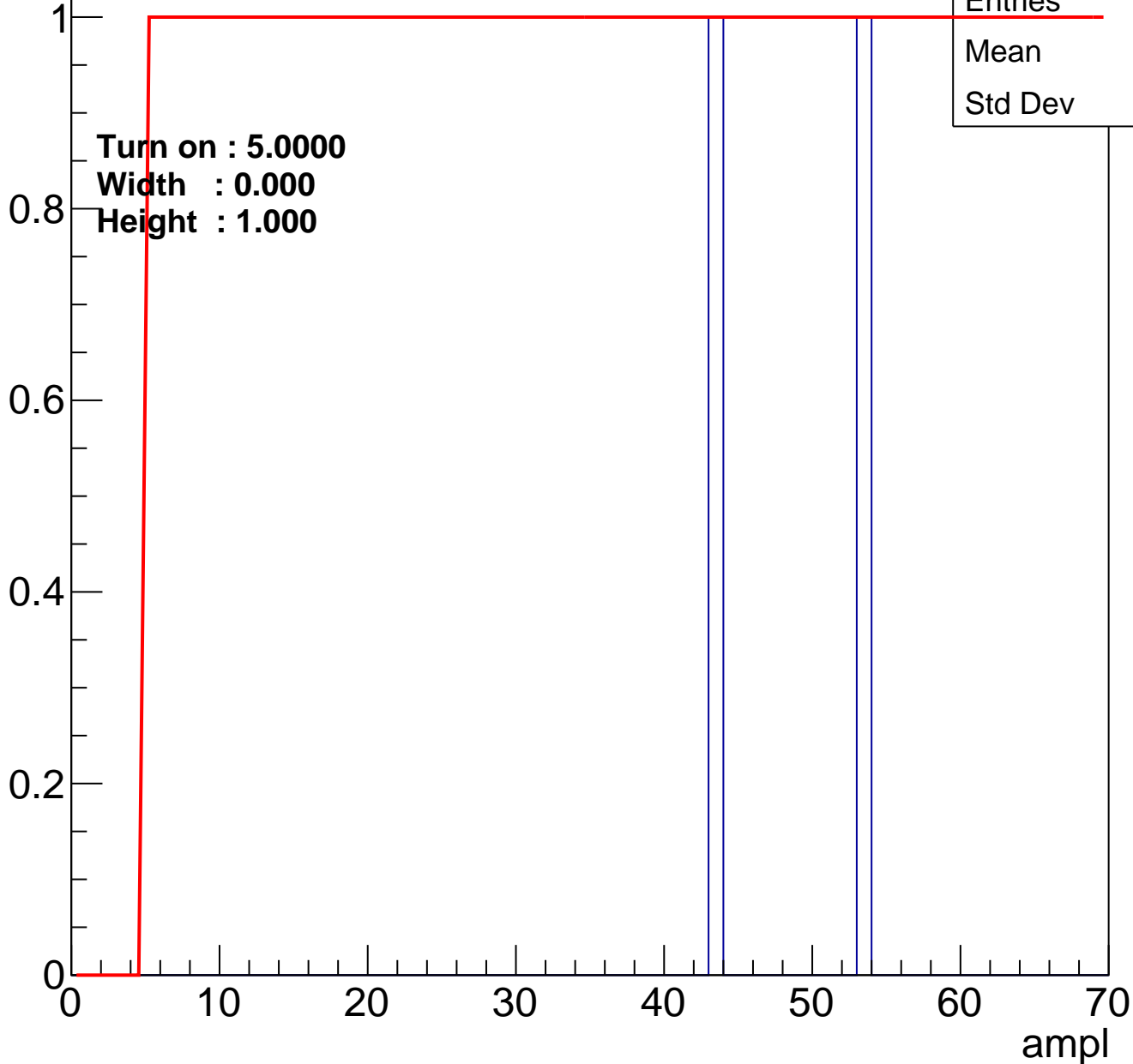
Height : 2.000



B0L100S, U8-ch96

calib_packv5_042523_0143.root, FC#6, port A1

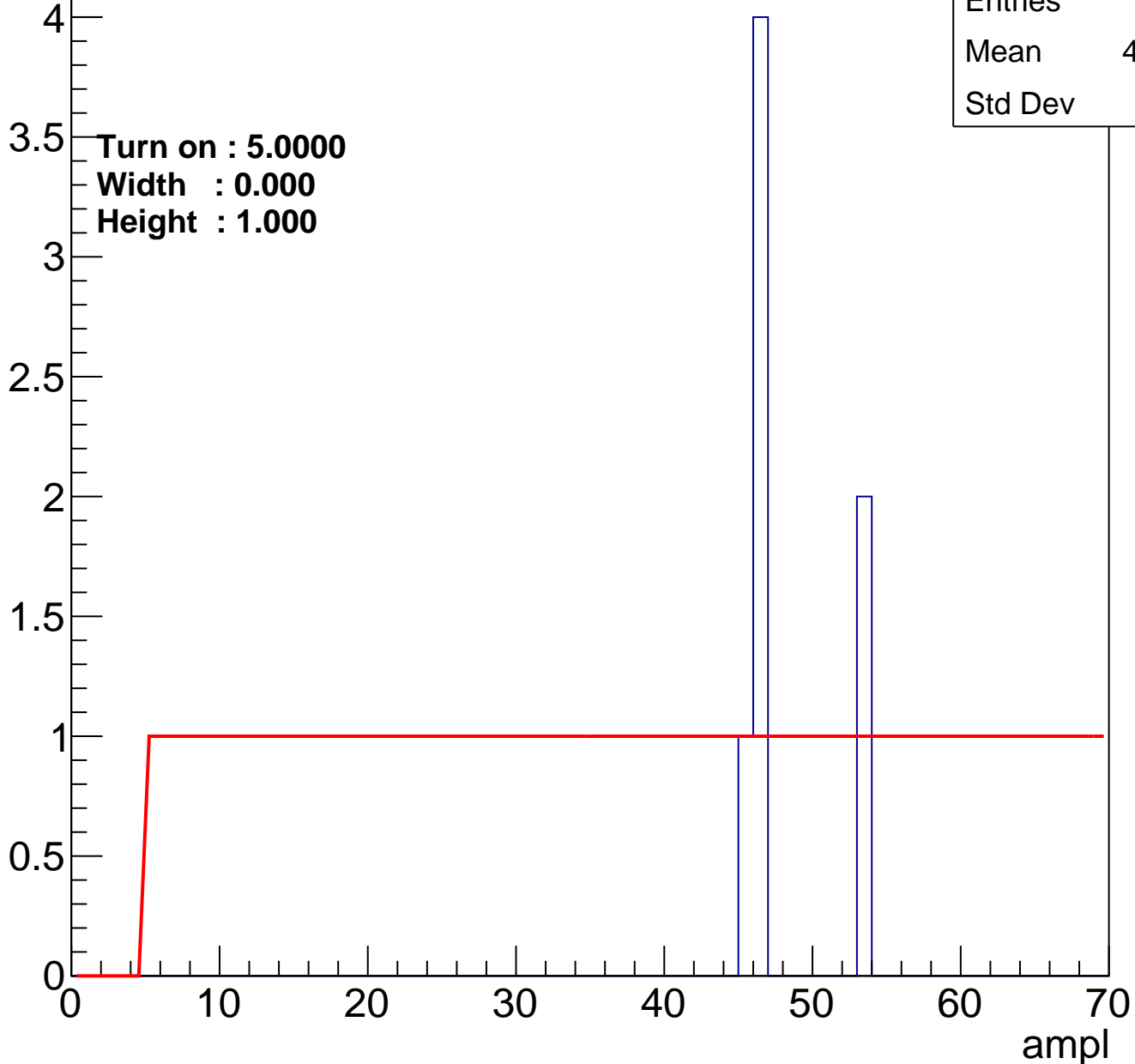
Entry



B0L100S, U8-ch97

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	7
Mean	47.86
Std Dev	3.27

Turn on : 5.0000
Width : 0.000
Height : 1.000

B0L100S, U8-ch98

calib_packv5_042523_0143.root, FC#6, port A1

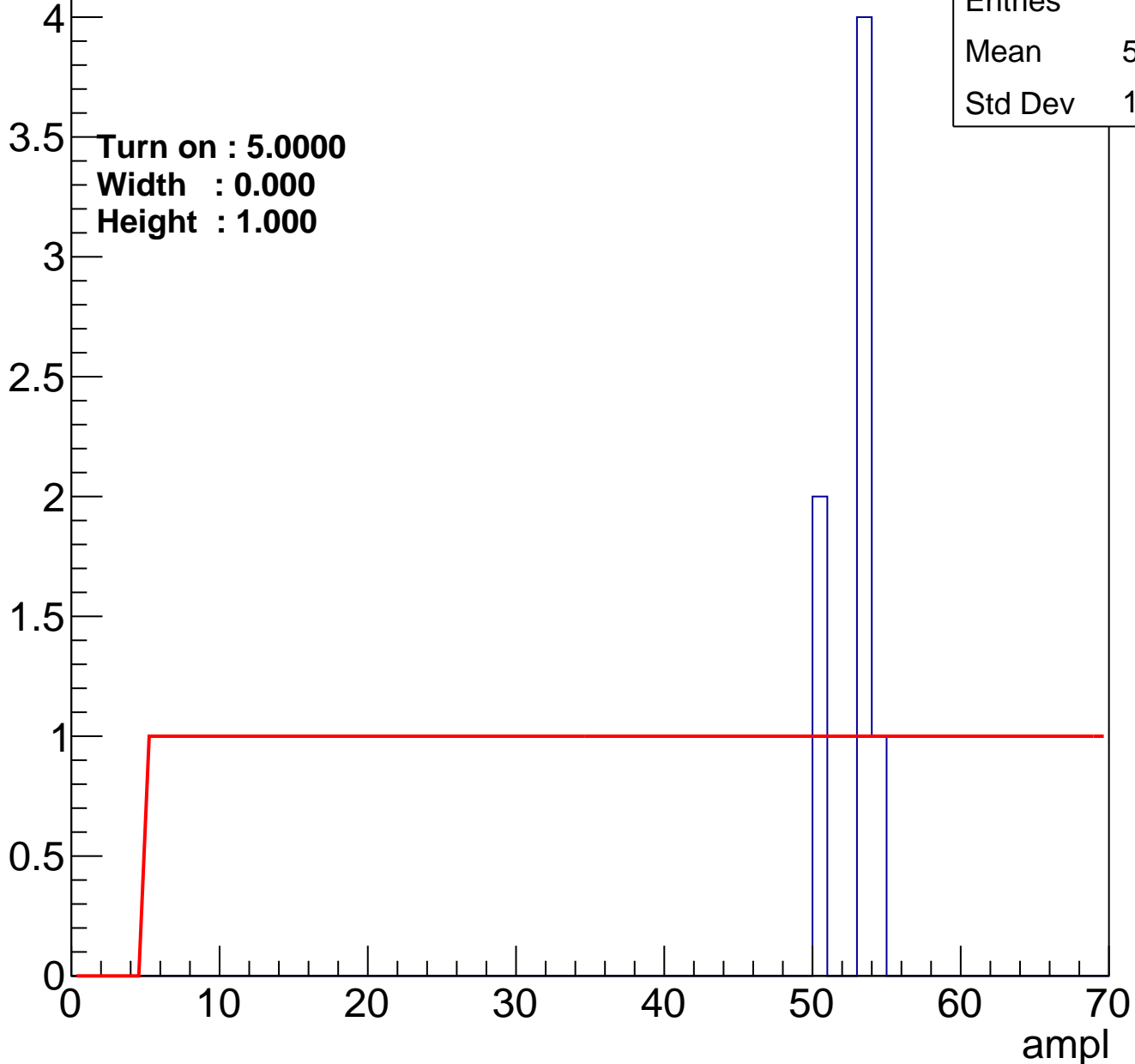
Entry



B0L100S, U8-ch99

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	7
Mean	52.29
Std Dev	1.485

B0L100S, U8-ch100

calib_packv5_042523_0143.root, FC#6, port A1

Entry

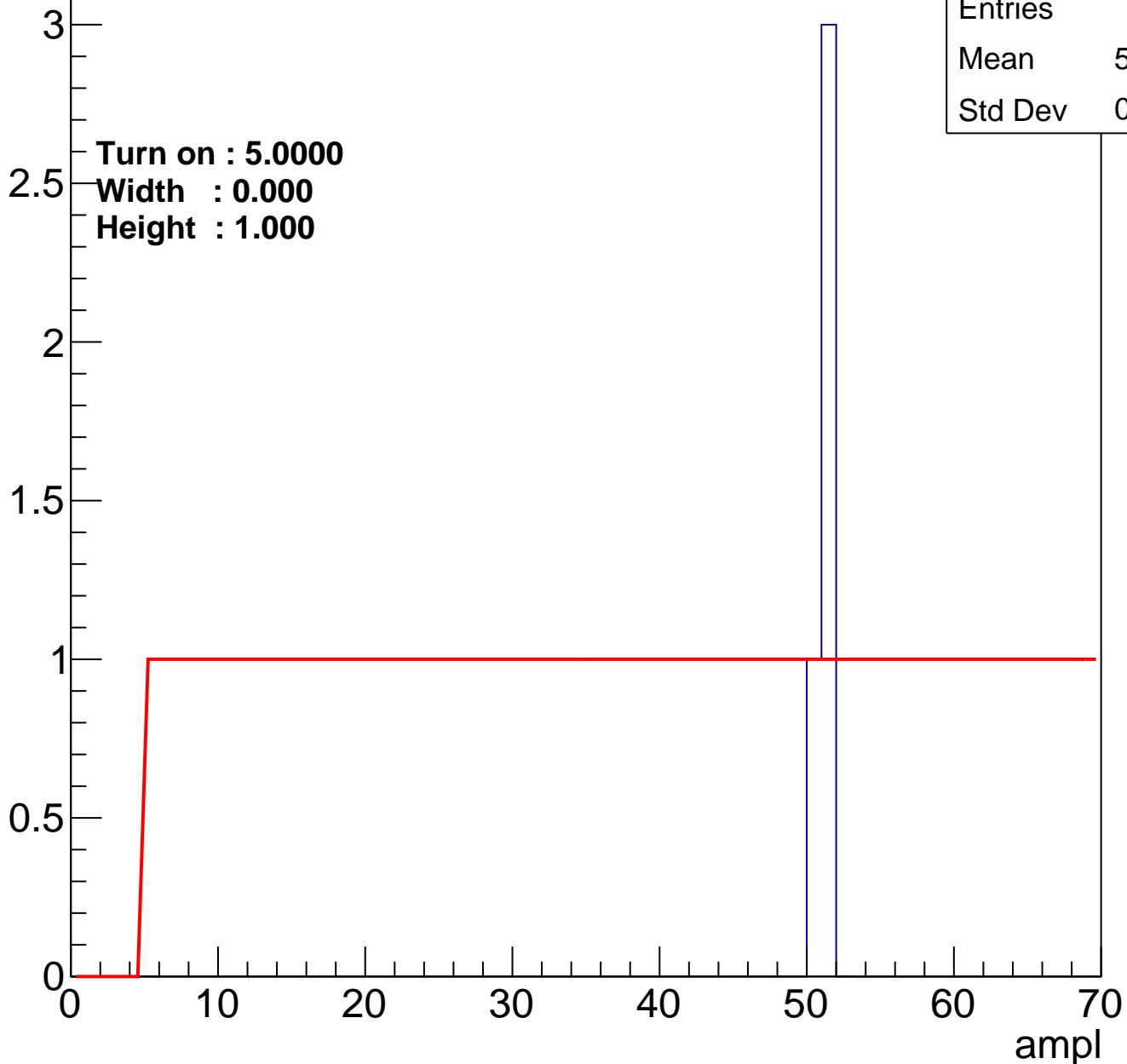


Entries	0
Mean	0
Std Dev	0

B0L100S, U8-ch101

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U8-ch102

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U8-ch103

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	1
Mean	0
Std Dev	0

B0L100S, U8-ch104

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U8-ch105

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U8-ch106

calib_packv5_042523_0143.root, FC#6, port A1

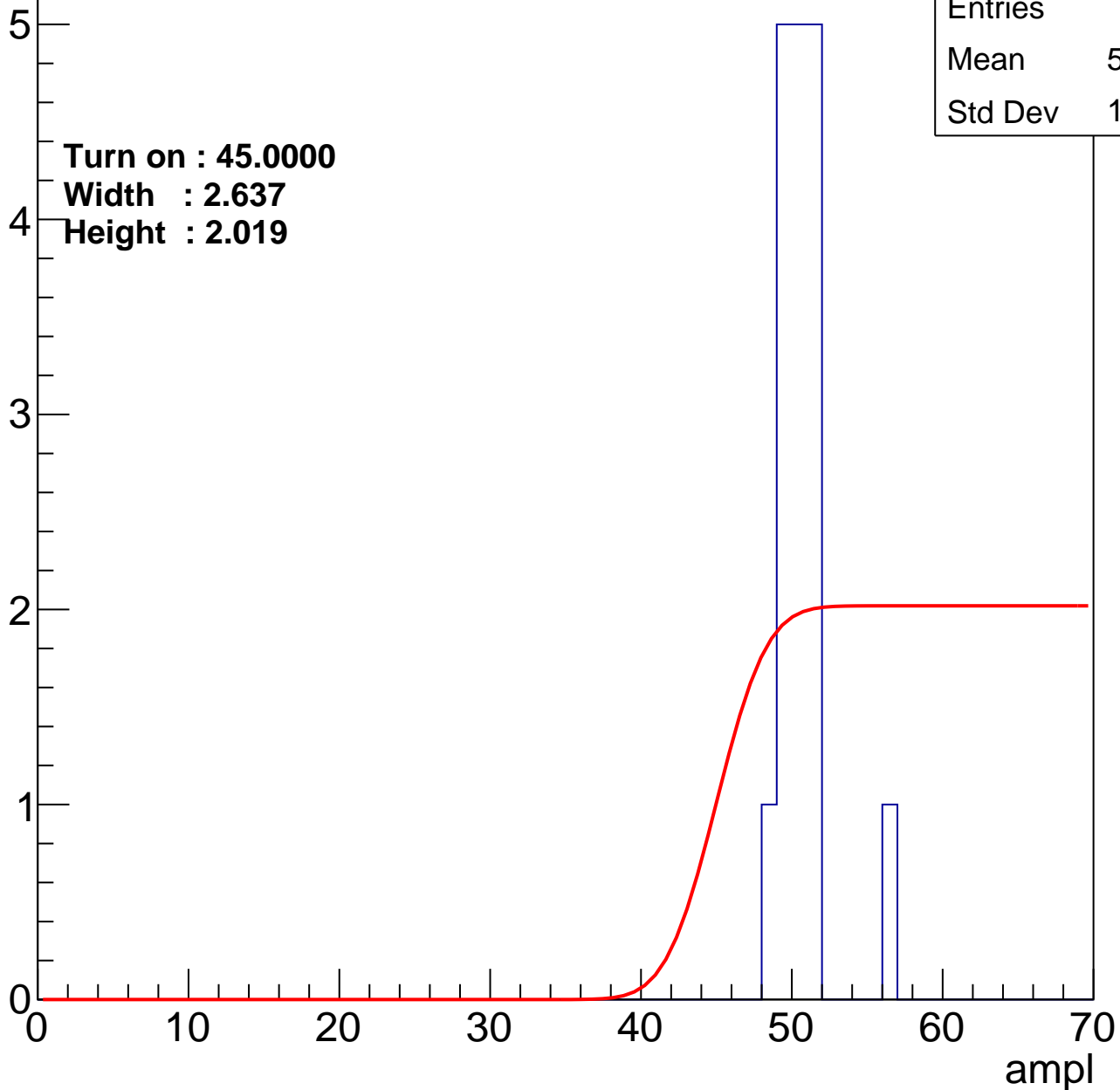
Entry

Entries	17
Mean	50.24
Std Dev	1.699

Turn on : 45.0000

Width : 2.637

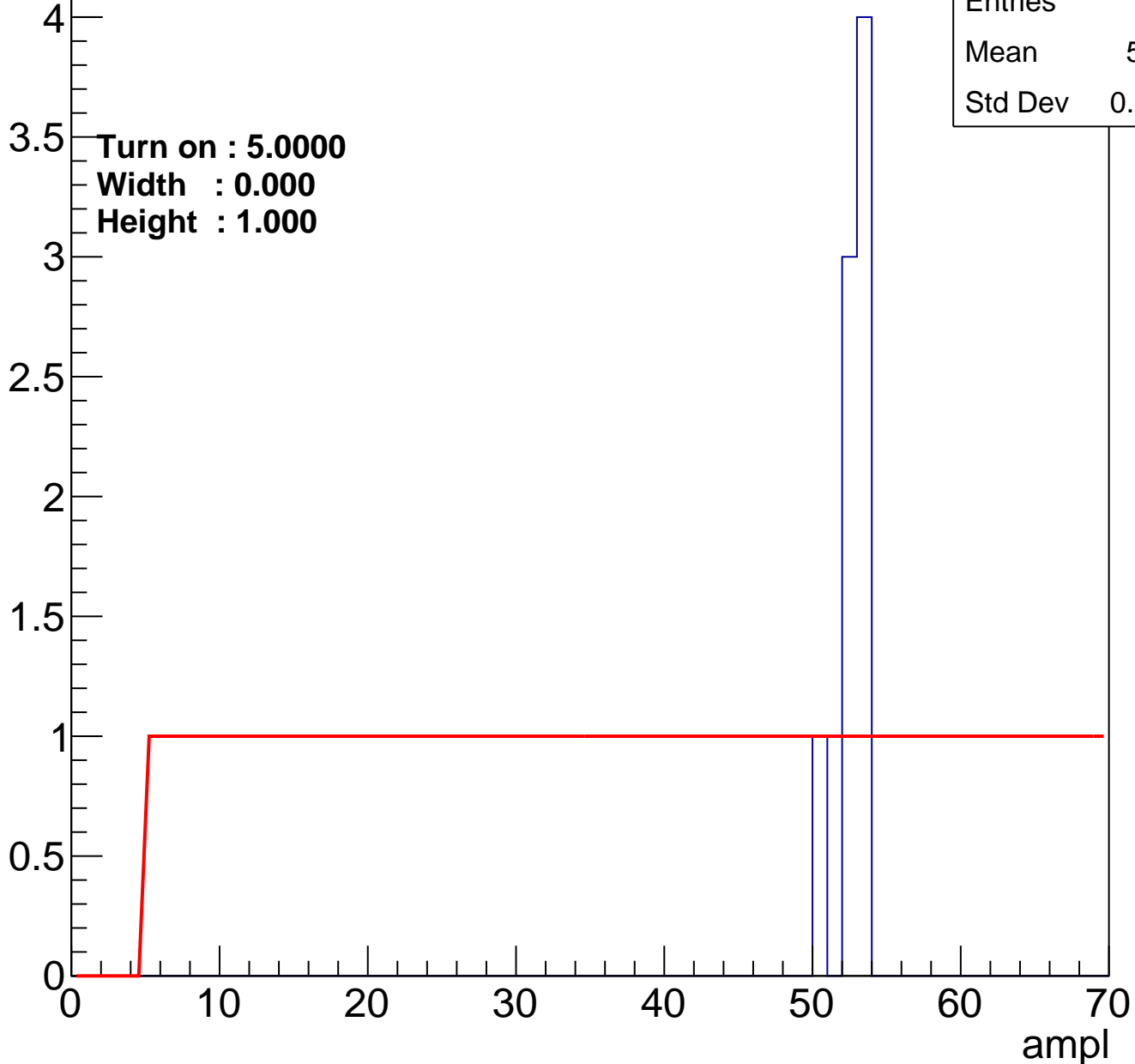
Height : 2.019



B0L100S, U8-ch107

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U8-ch108

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U8-ch109

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	1
Mean	0
Std Dev	0

B0L100S, U8-ch110

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U8-ch111

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U8-ch112

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U8-ch113

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	1
Mean	0
Std Dev	0

B0L100S, U8-ch114

calib_packv5_042523_0143.root, FC#6, port A1

Entry

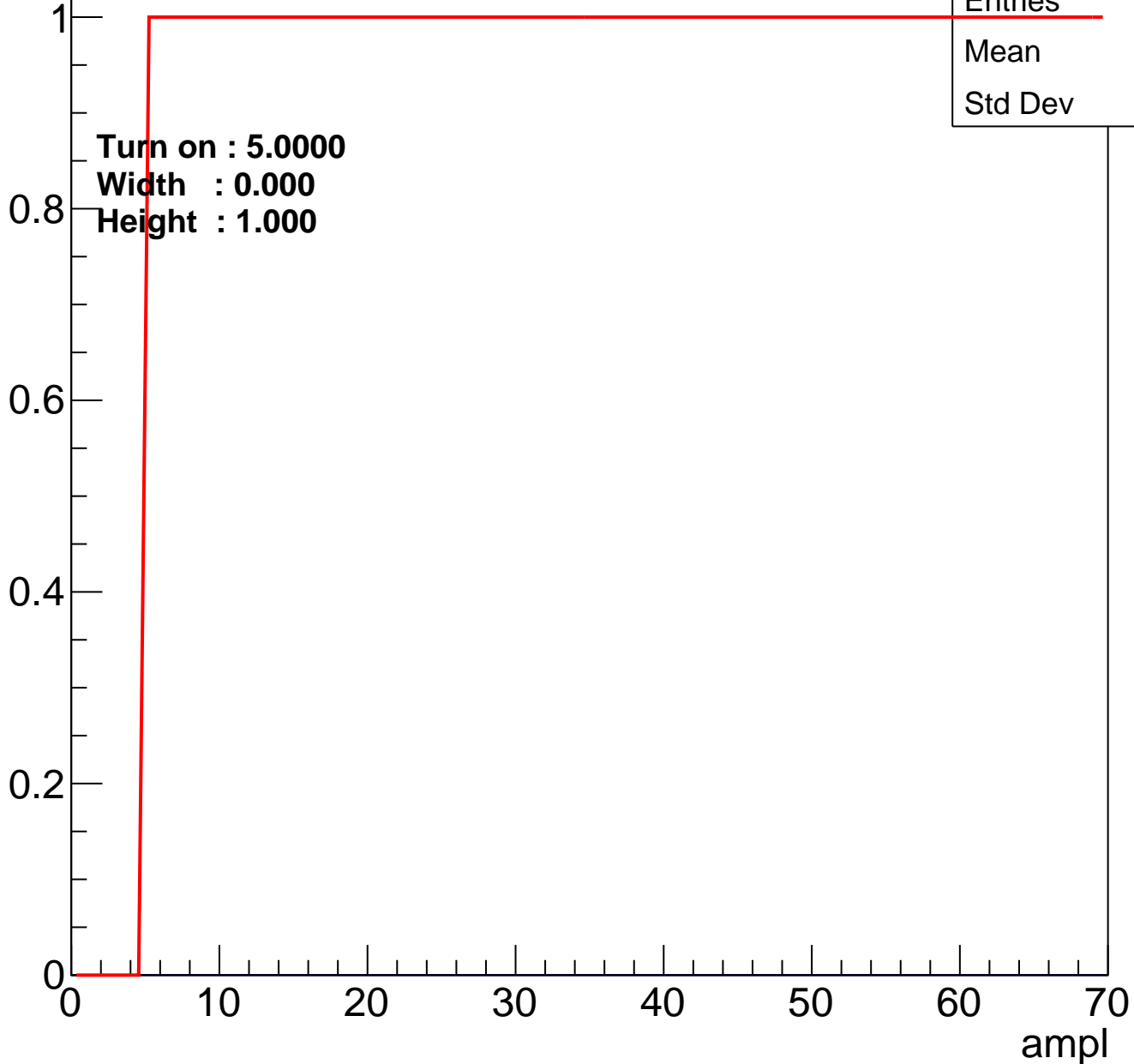


Entries	0
Mean	0
Std Dev	0

B0L100S, U8-ch115

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U8-ch116

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	1
Mean	0
Std Dev	0

B0L100S, U8-ch117

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	1
Mean	0
Std Dev	0

B0L100S, U8-ch118

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U8-ch119

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U8-ch120

calib_packv5_042523_0143.root, FC#6, port A1

Entry

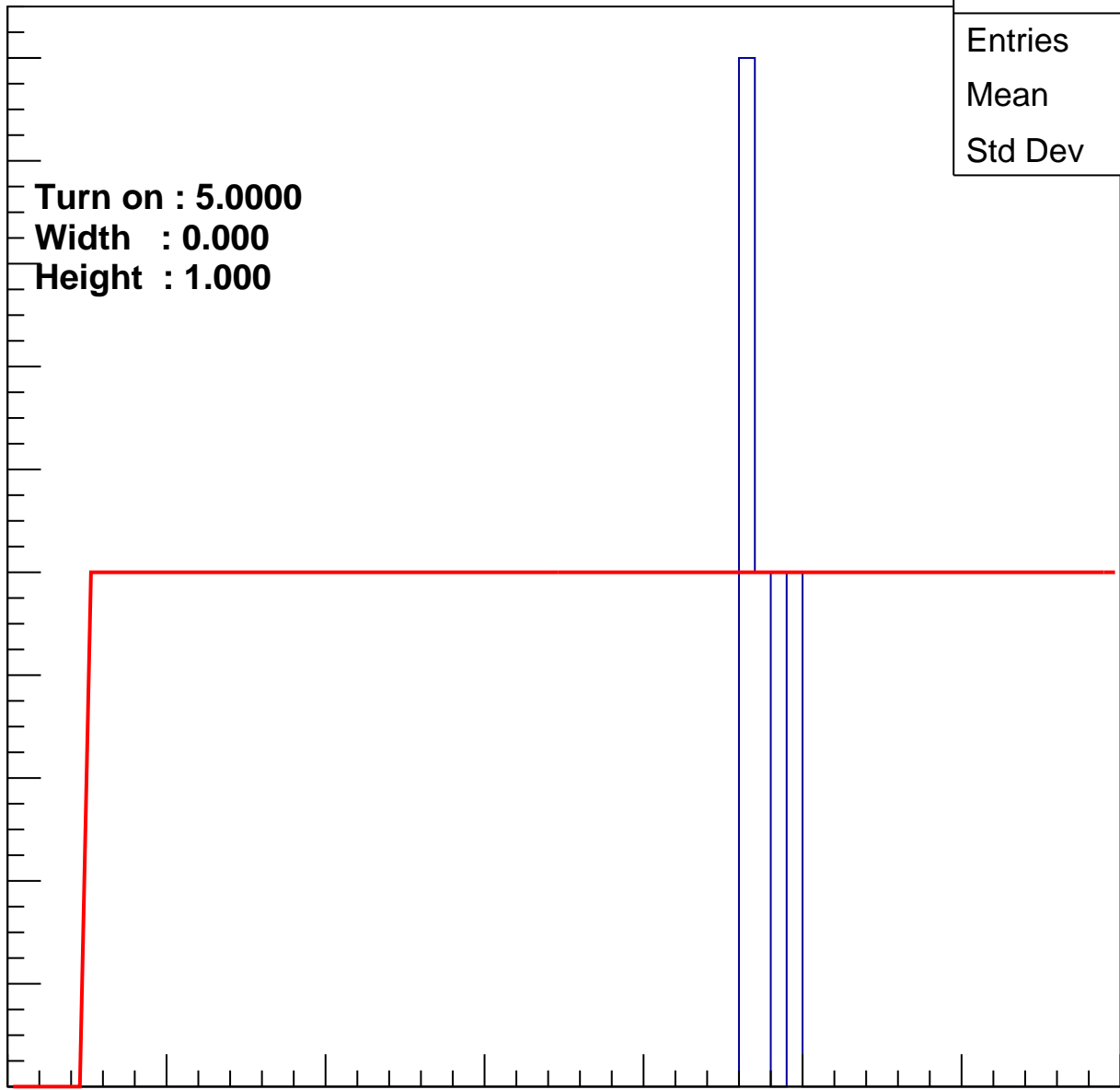
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Turn on : 5.0000
Width : 0.000
Height : 1.000

Entries	4
Mean	47
Std Dev	1.225

0 10 20 30 40 50 60 70

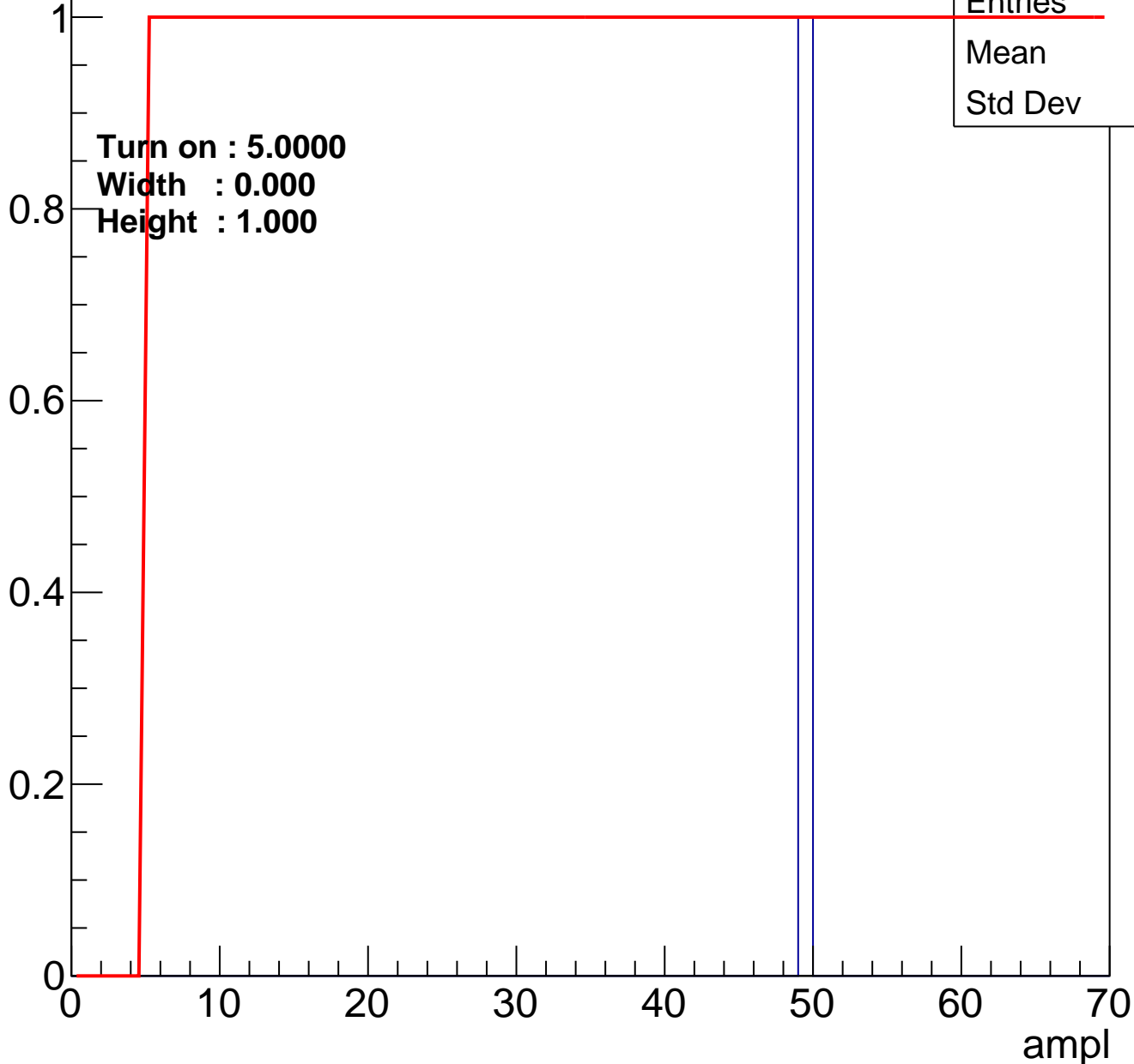
ampl



B0L100S, U8-ch121

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U8-ch122

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U8-ch123

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	2
Mean	0
Std Dev	0

B0L100S, U8-ch124

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U8-ch125

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U8-ch126

calib_packv5_042523_0143.root, FC#6, port A1

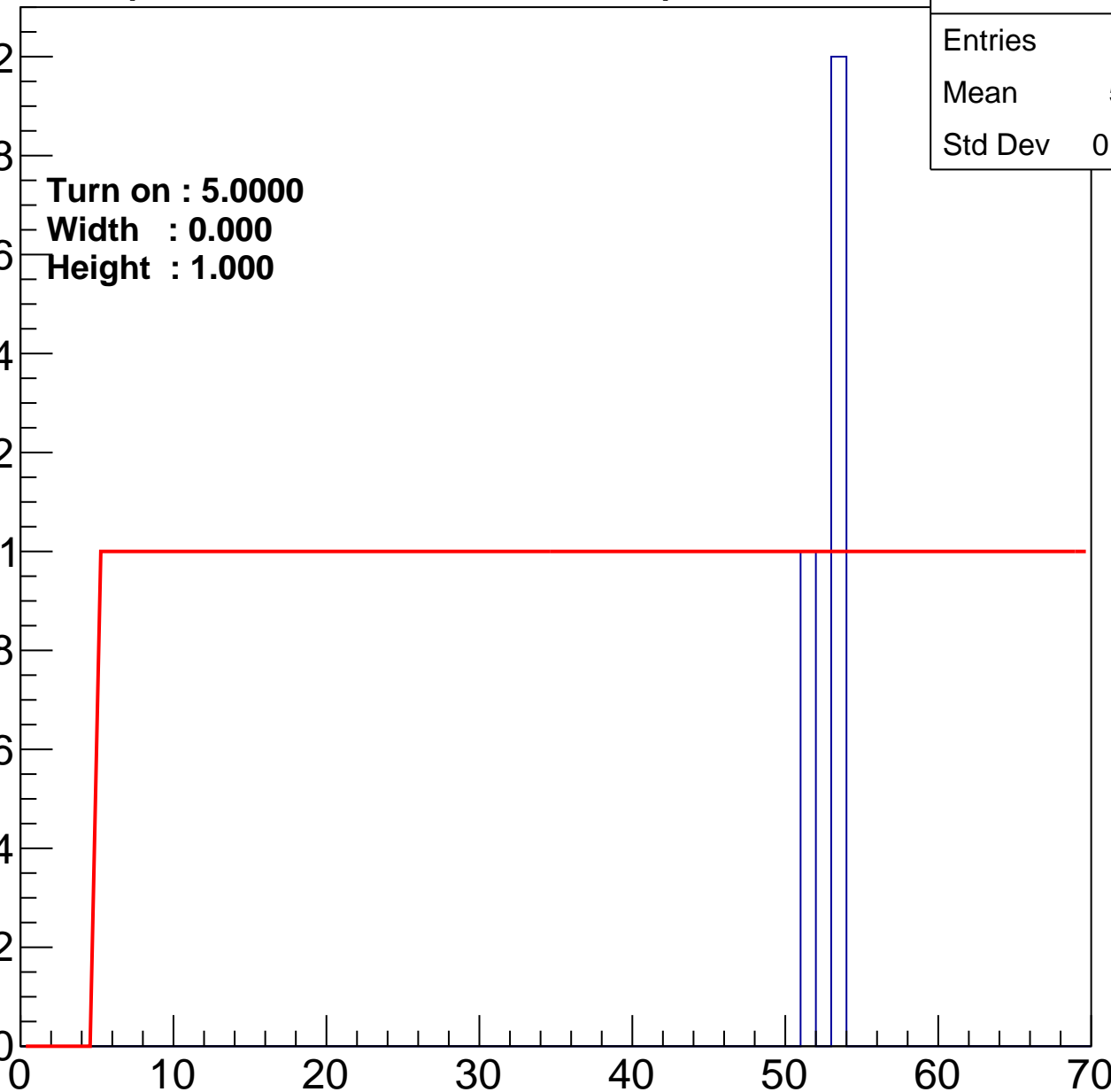
Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Turn on : 5.0000
Width : 0.000
Height : 1.000

Entries	3
Mean	52.33
Std Dev	0.9428

ampl



B0L100S, U8-ch127

calib_packv5_042523_0143.root, FC#6, port A1

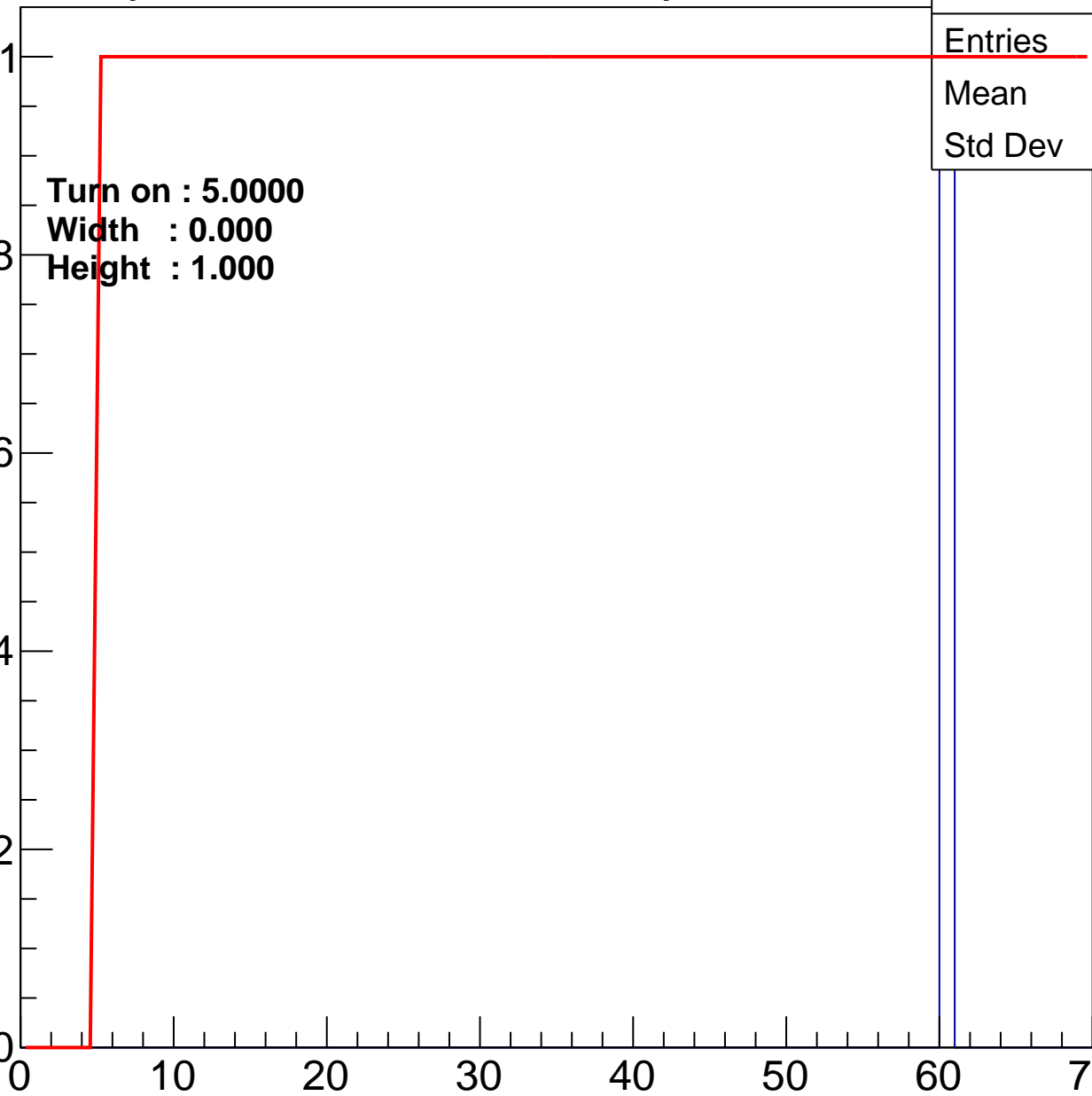
Entry

1
0.8
0.6
0.4
0.2
0

Turn on : 5.0000
Width : 0.000
Height : 1.000

Entries	1
Mean	60
Std Dev	0

ampl



B0L100S, U8-ch127

calib_packv5_042523_0143.root, FC#6, port A1

Entry

