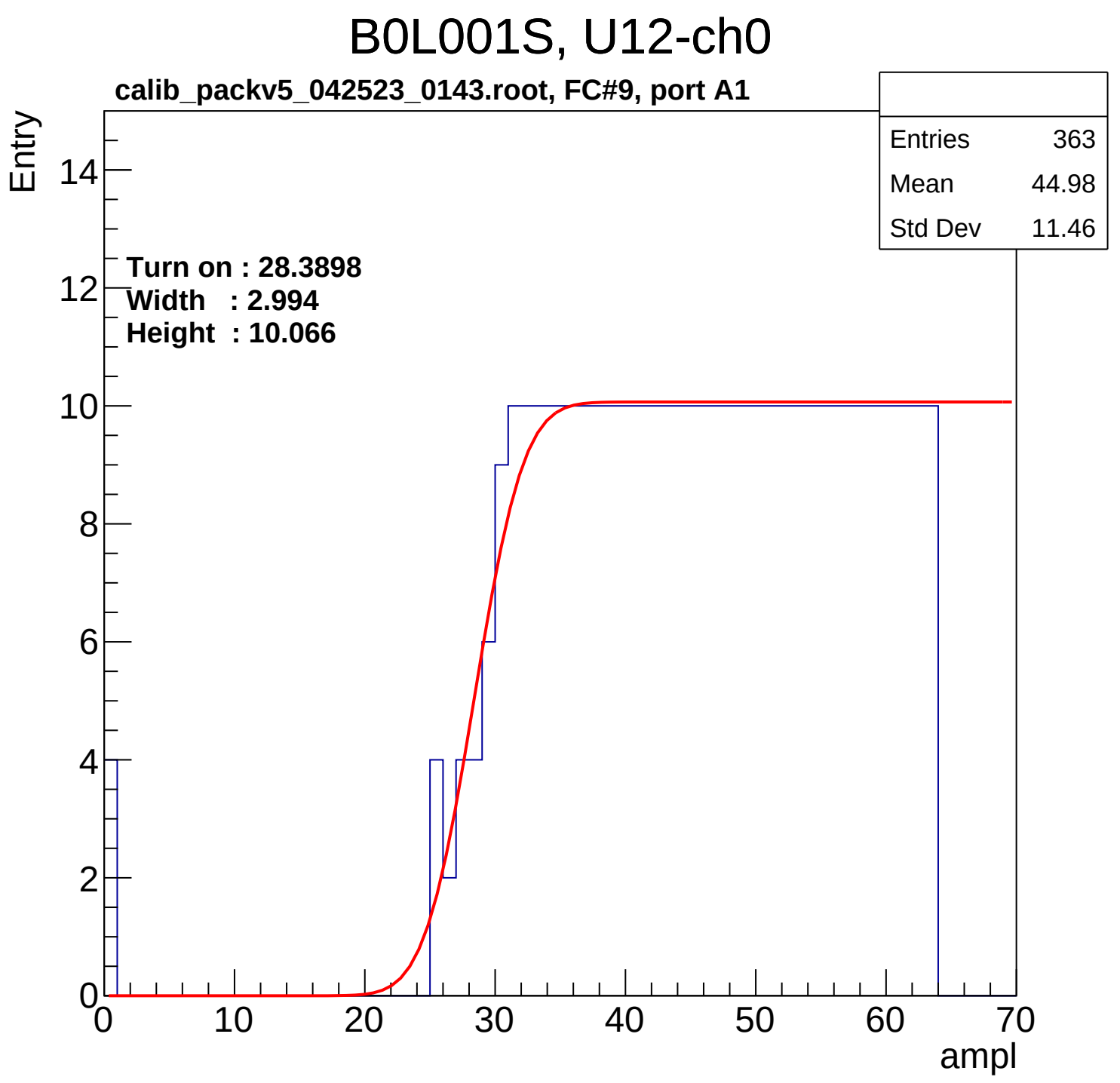
B0L001S, U12-ch0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 44.98
Std Dev 11.46
Turn on : 28.3898
Width : 2.994
Height : 10.066
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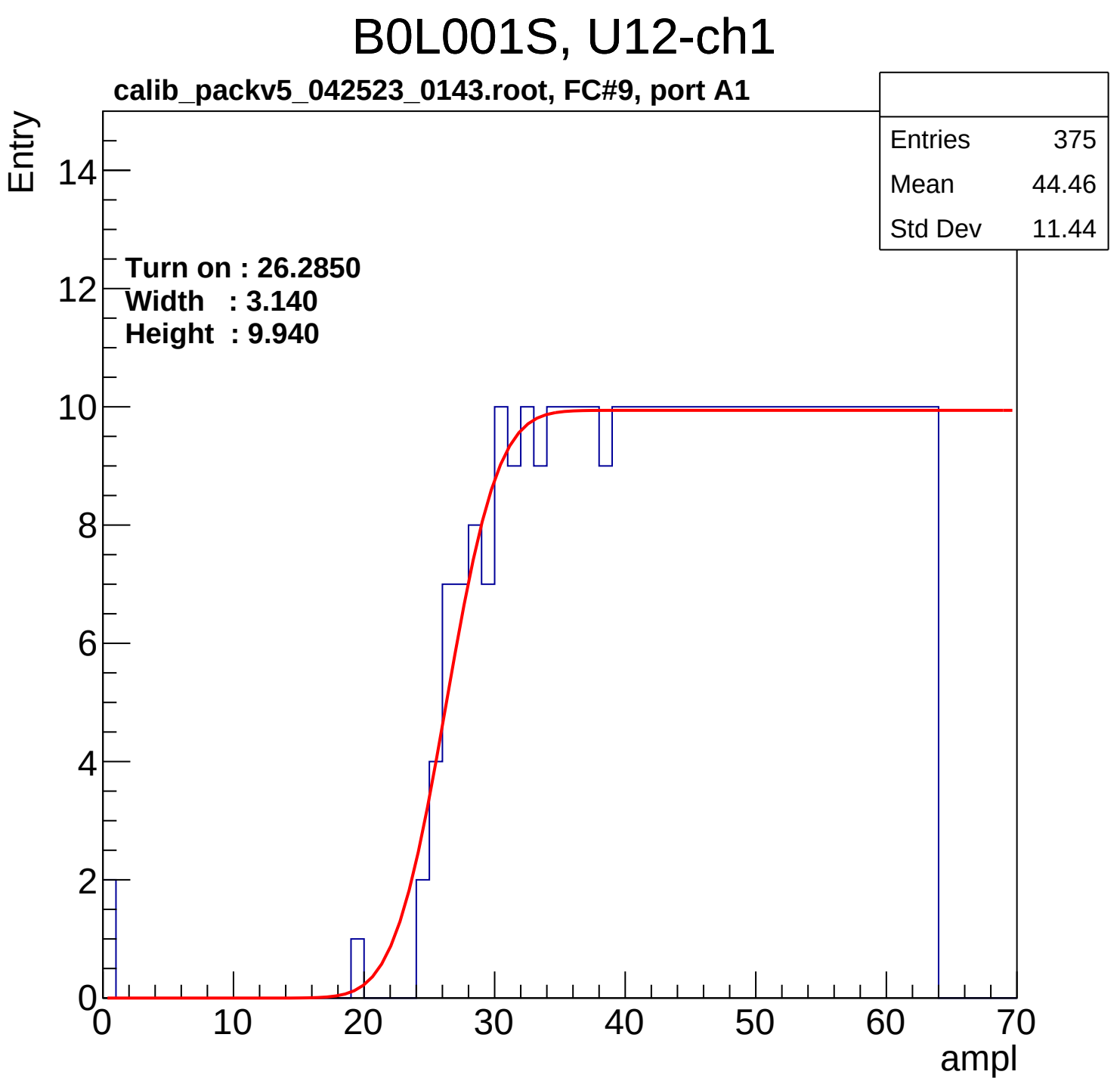
B0L001S, U12-ch1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 375
Mean 44.46
Std Dev 11.44
Turn on : 26.2850
Width : 3.140
Height : 9.940
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ampl
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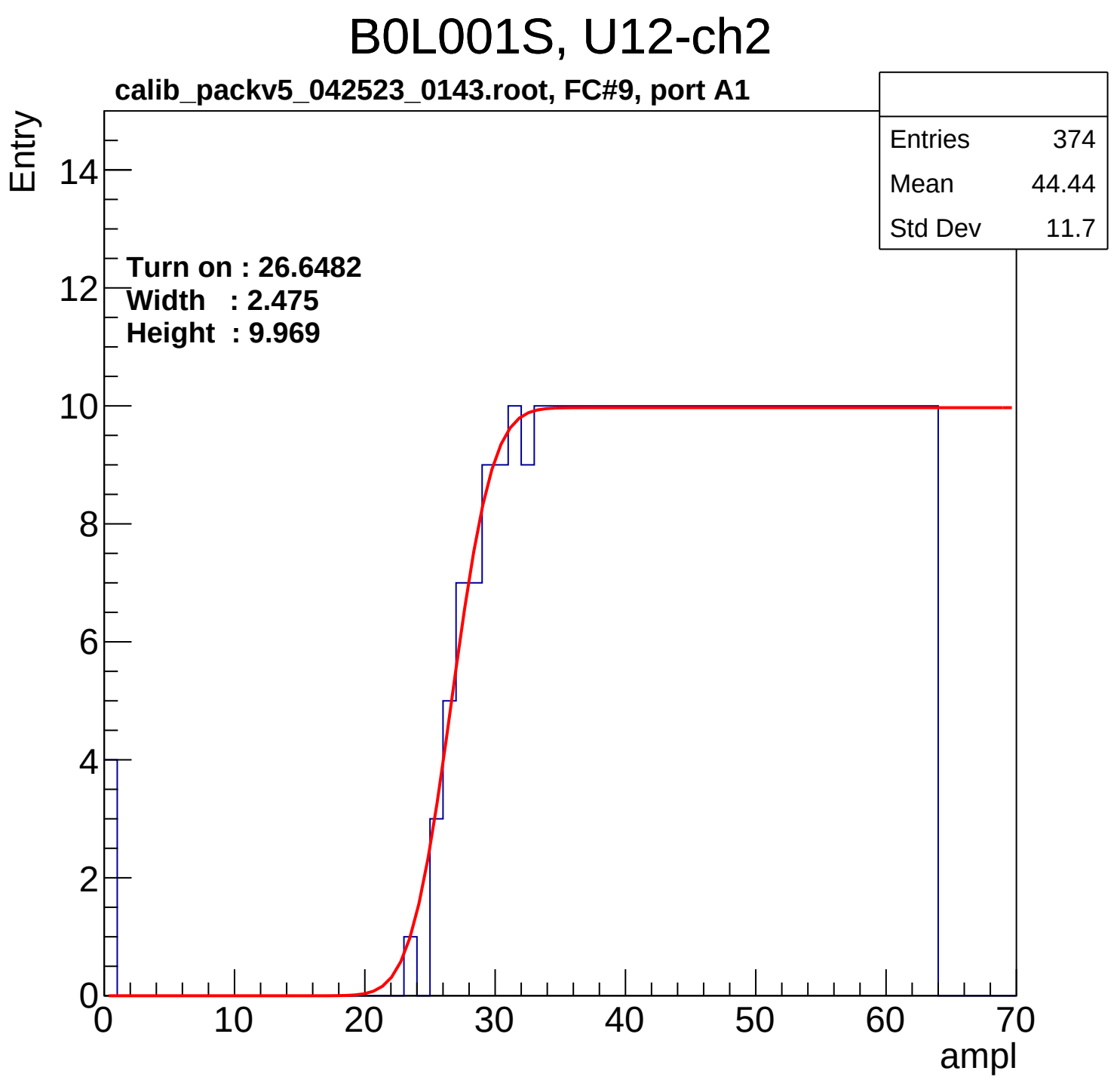
B0L001S, U12-ch2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 374
Mean 44.44
Std Dev 11.7
Turn on : 26.6482
Width : 2.475
Height : 9.969
Entry
ampl
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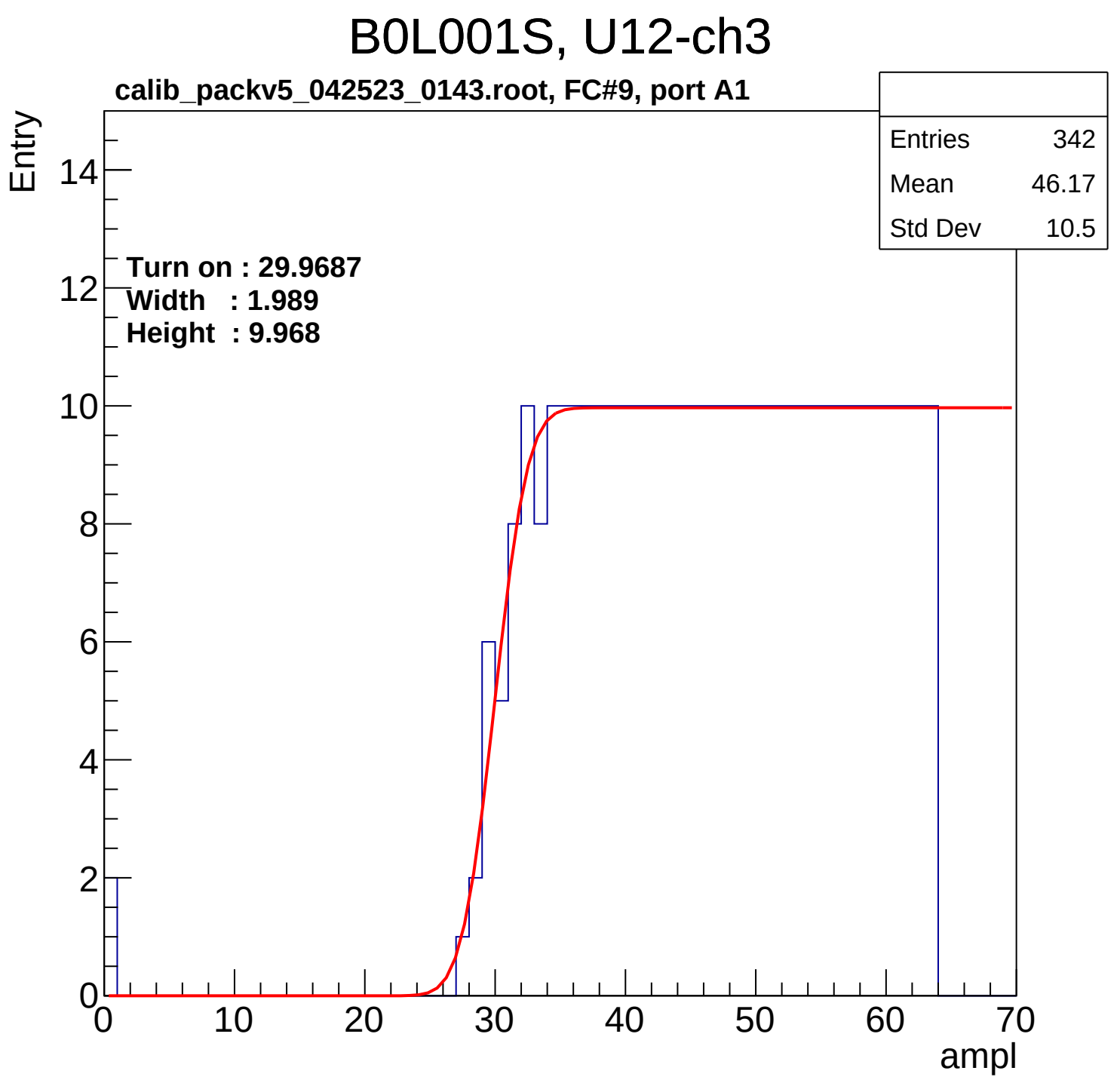
B0L001S, U12-ch3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 342
Mean 46.17
Std Dev 10.5
Turn on : 29.9687
Width : 1.989
Height : 9.968
Entry
ampl
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8
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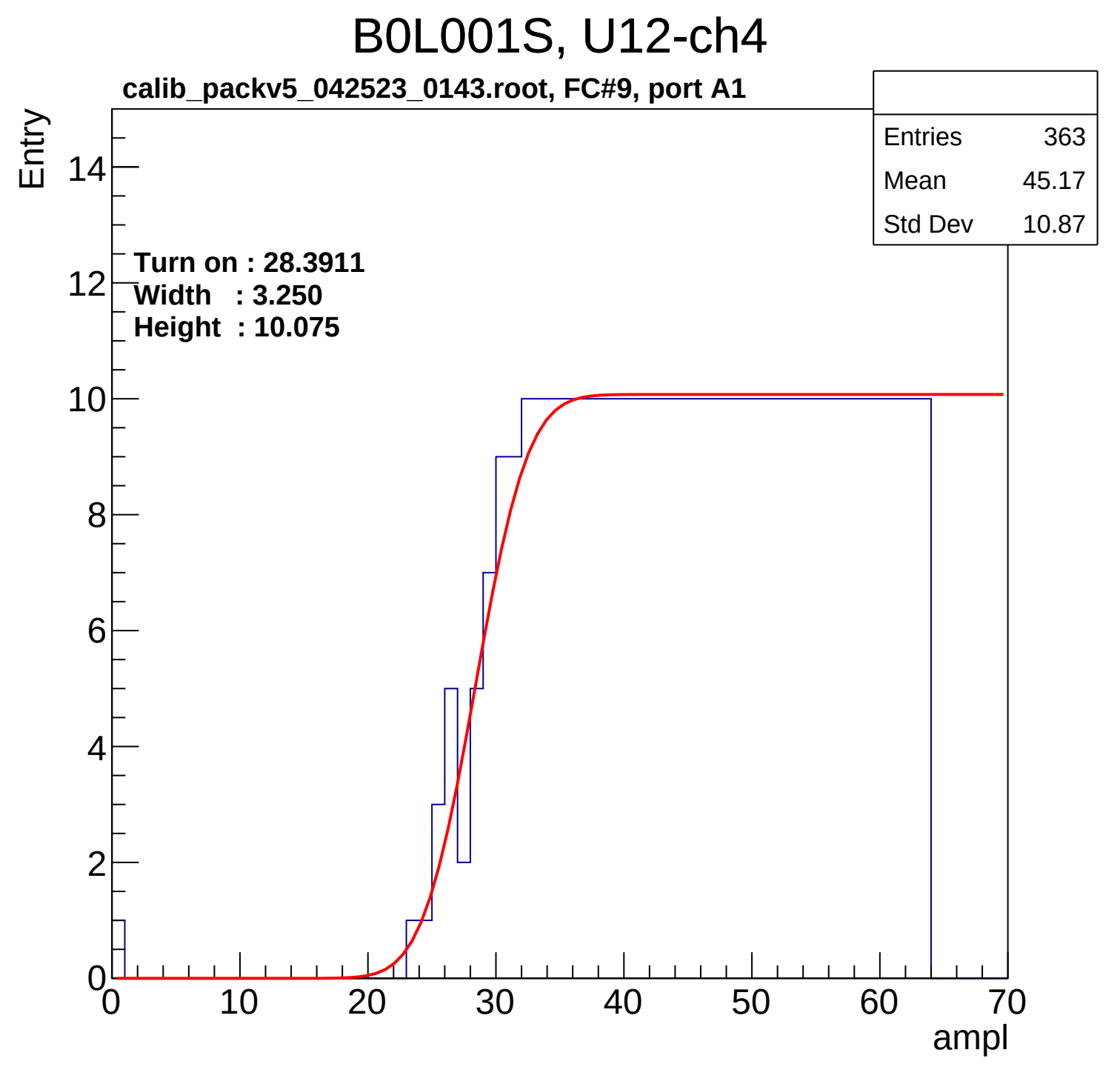
B0L001S, U12-ch4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 45.17
Std Dev 10.87
Turn on : 28.3911
Width : 3.250
Height : 10.075
Entry
ampl
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2
4
6
8
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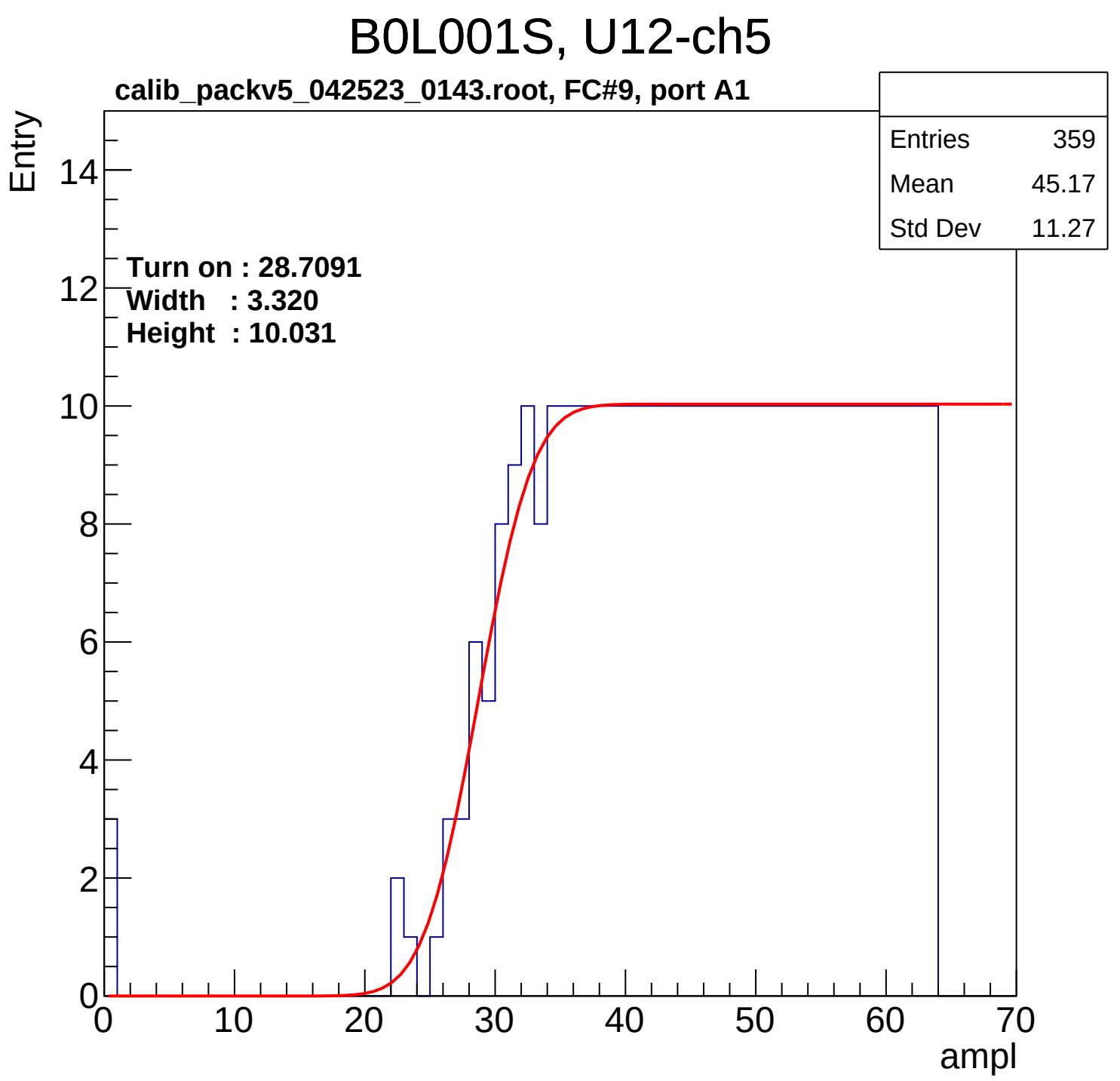
B0L001S, U12-ch5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 45.17
Std Dev 11.27
Turn on : 28.7091
Width : 3.320
Height : 10.031
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ampl
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6
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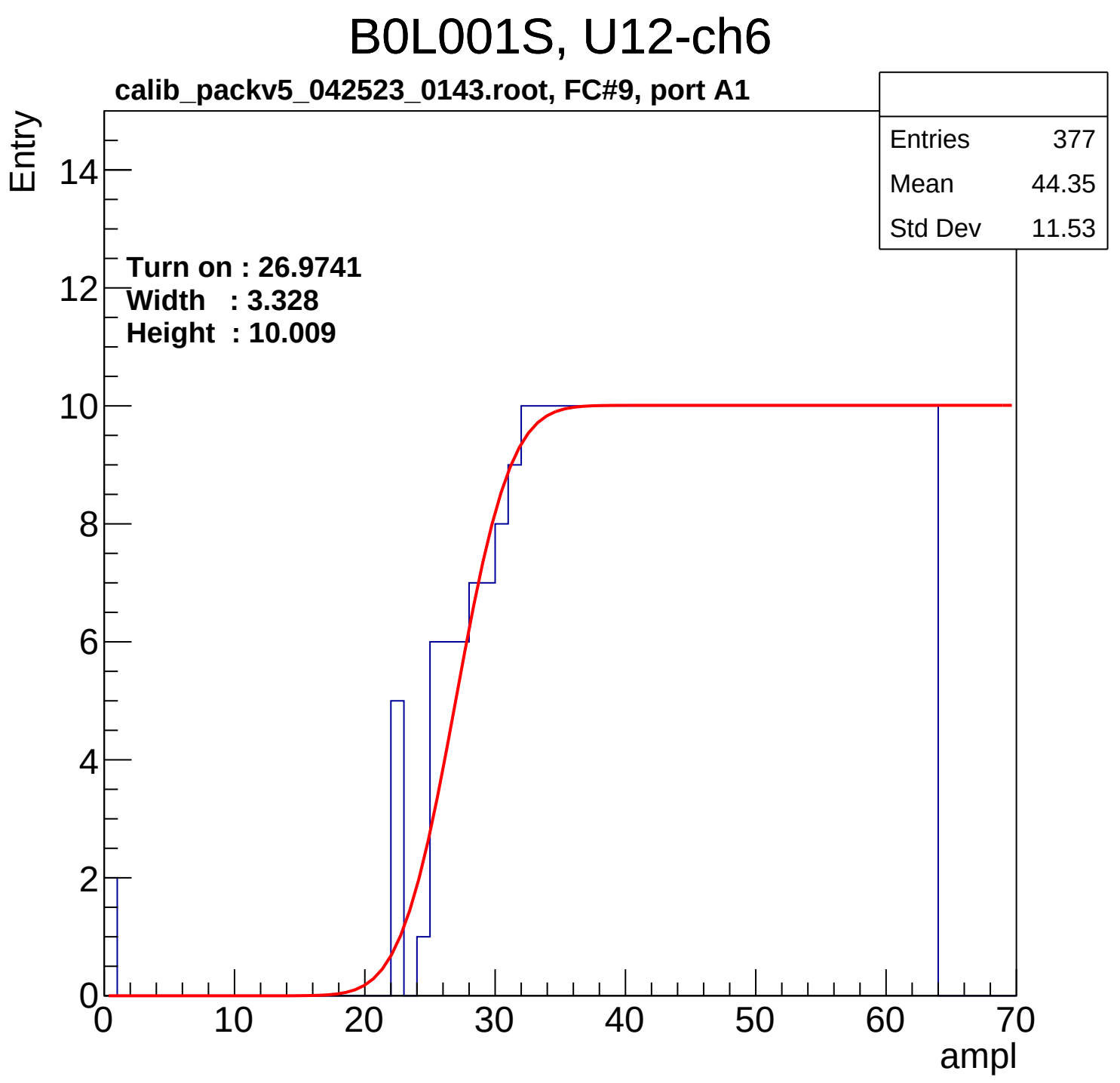
B0L001S, U12-ch6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 377
Mean 44.35
Std Dev 11.53
Turn on : 26.9741
Width : 3.328
Height : 10.009
Entry
ampl
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4
6
8
10
12
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0
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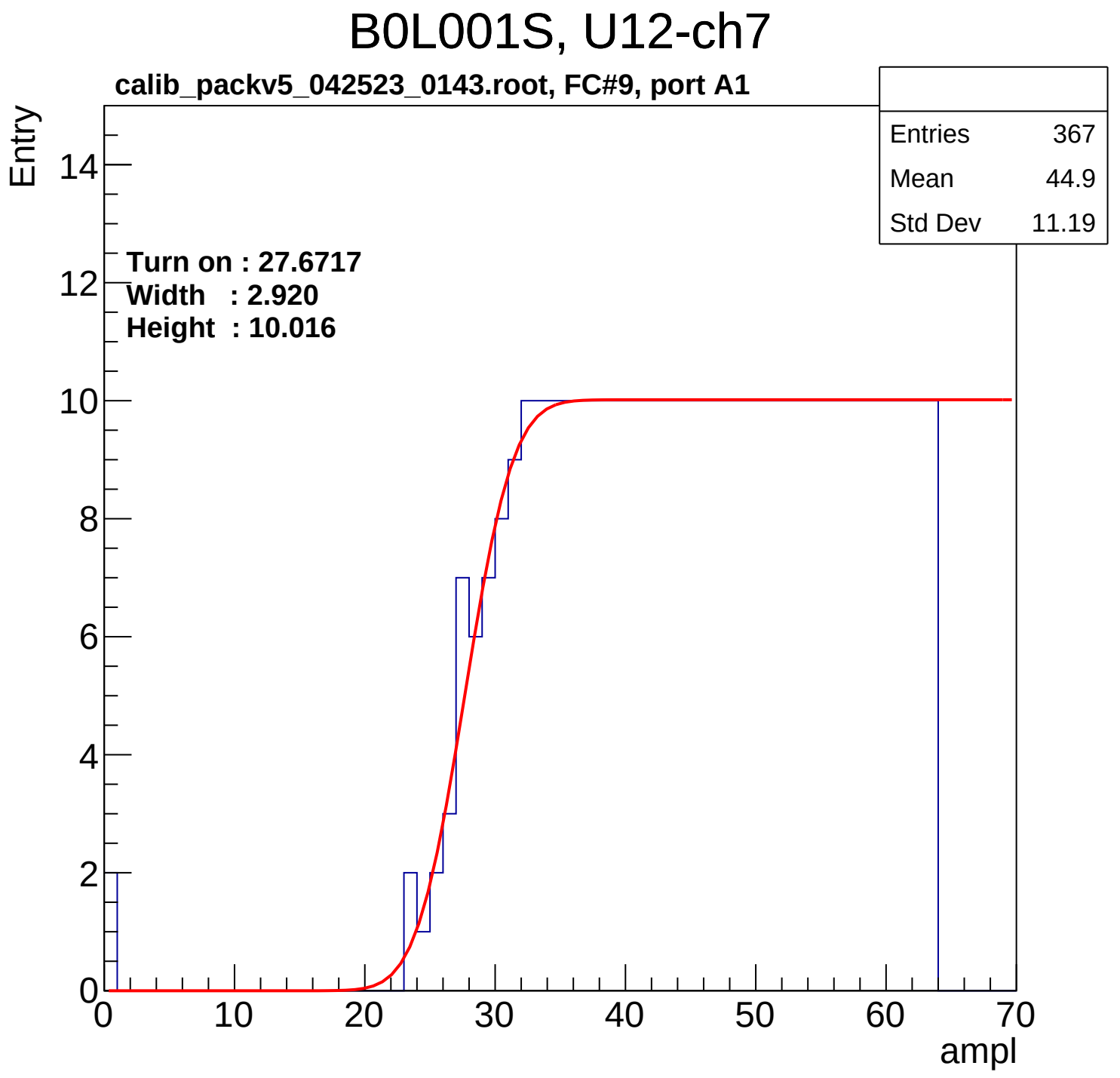
B0L001S, U12-ch7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.9
Std Dev 11.19
Turn on : 27.6717
Width : 2.920
Height : 10.016
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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60
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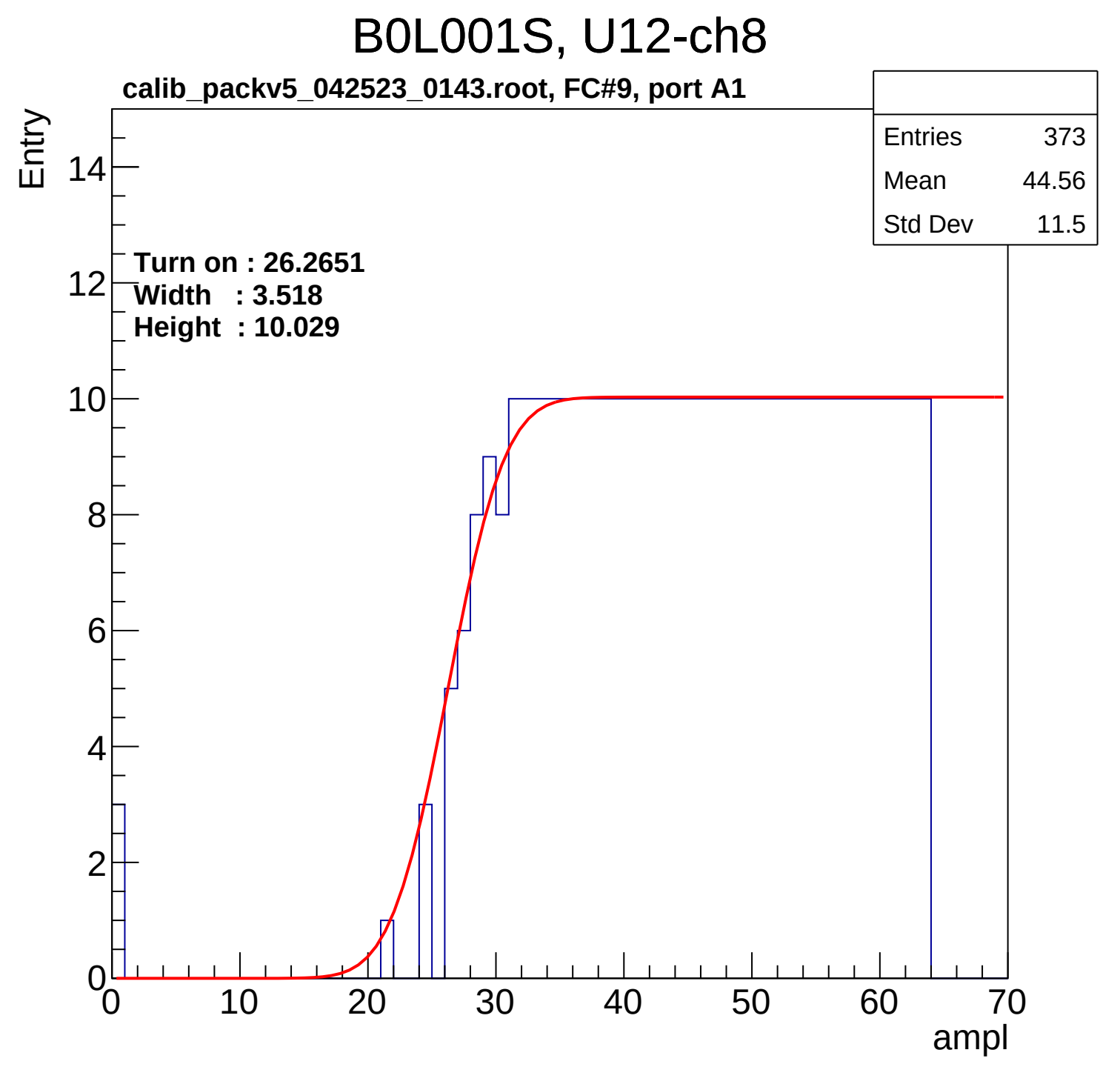
B0L001S, U12-ch8
calib_packv5_042523_0143.root, FC#9, port A1
Entries 373
Mean 44.56
Std Dev 11.5
Turn on : 26.2651
Width : 3.518
Height : 10.029
Entry
ampl
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6
8
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0
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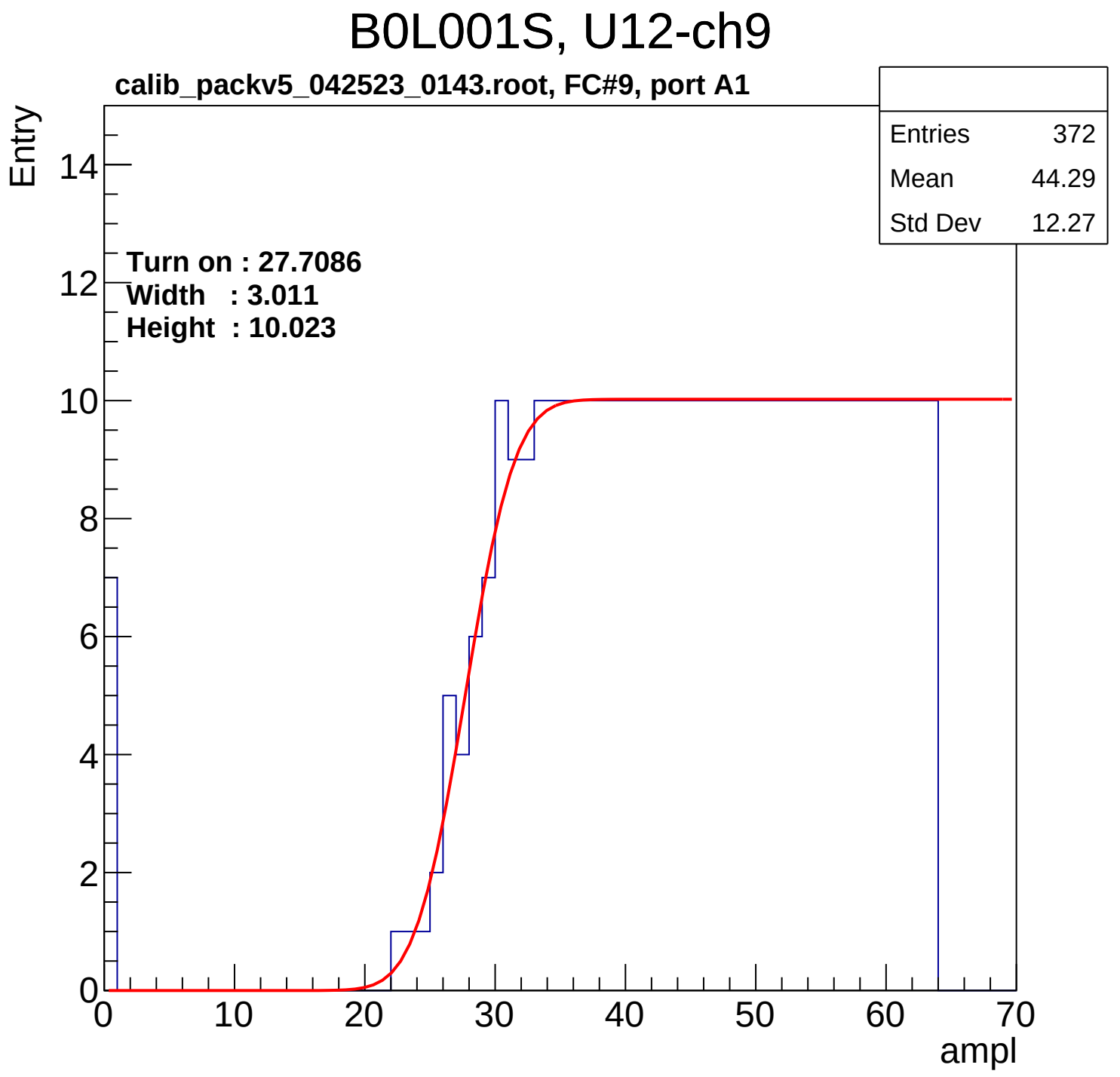
B0L001S, U12-ch9
calib_packv5_042523_0143.root, FC#9, port A1
Entries 372
Mean 44.29
Std Dev 12.27
Turn on : 27.7086
Width : 3.011
Height : 10.023
Entry
ampl
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6
8
10
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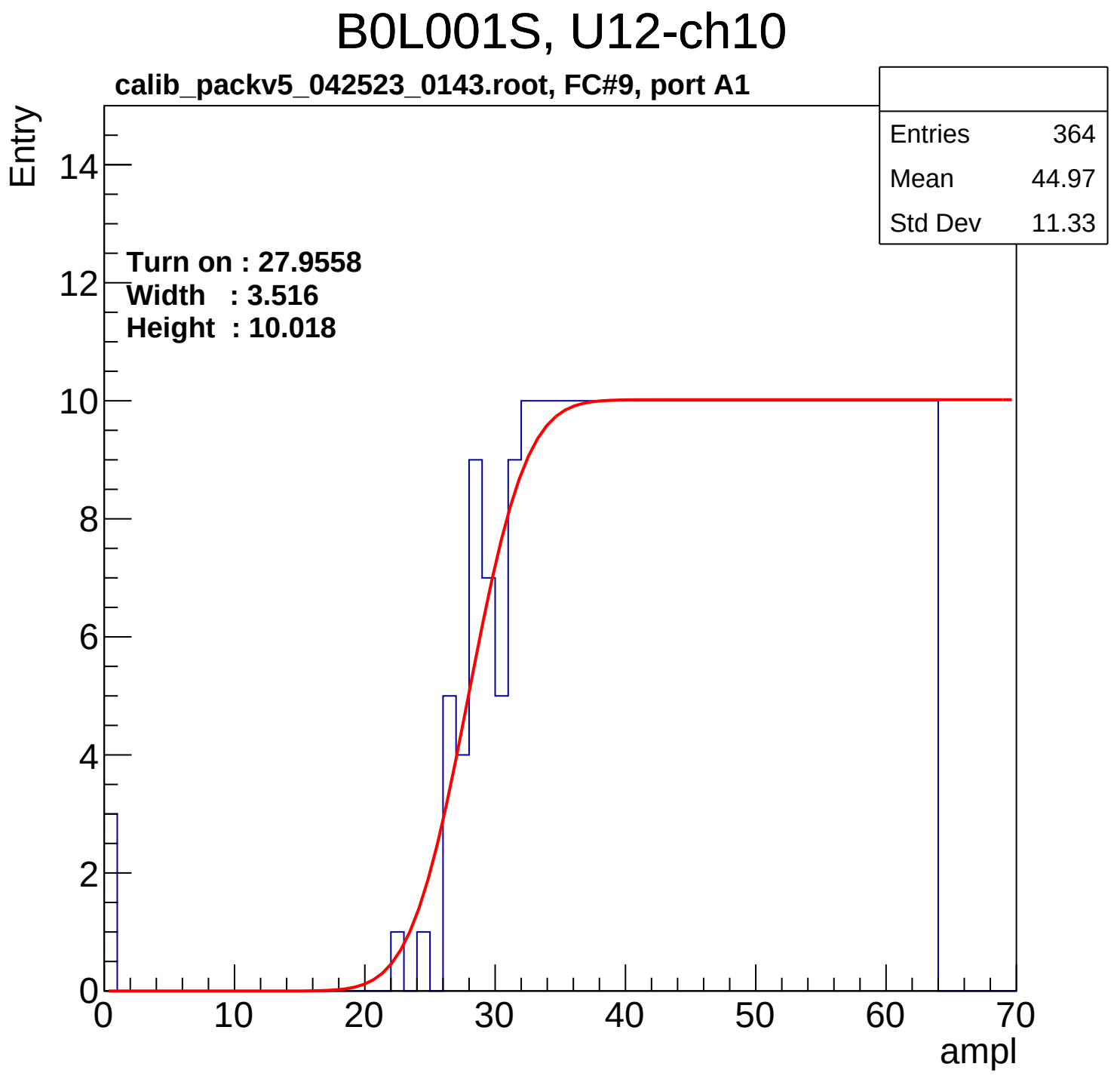
B0L001S, U12-ch10
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 44.97
Std Dev 11.33
Turn on : 27.9558
Width : 3.516
Height : 10.018
Entry
ampl
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6
8
10
12
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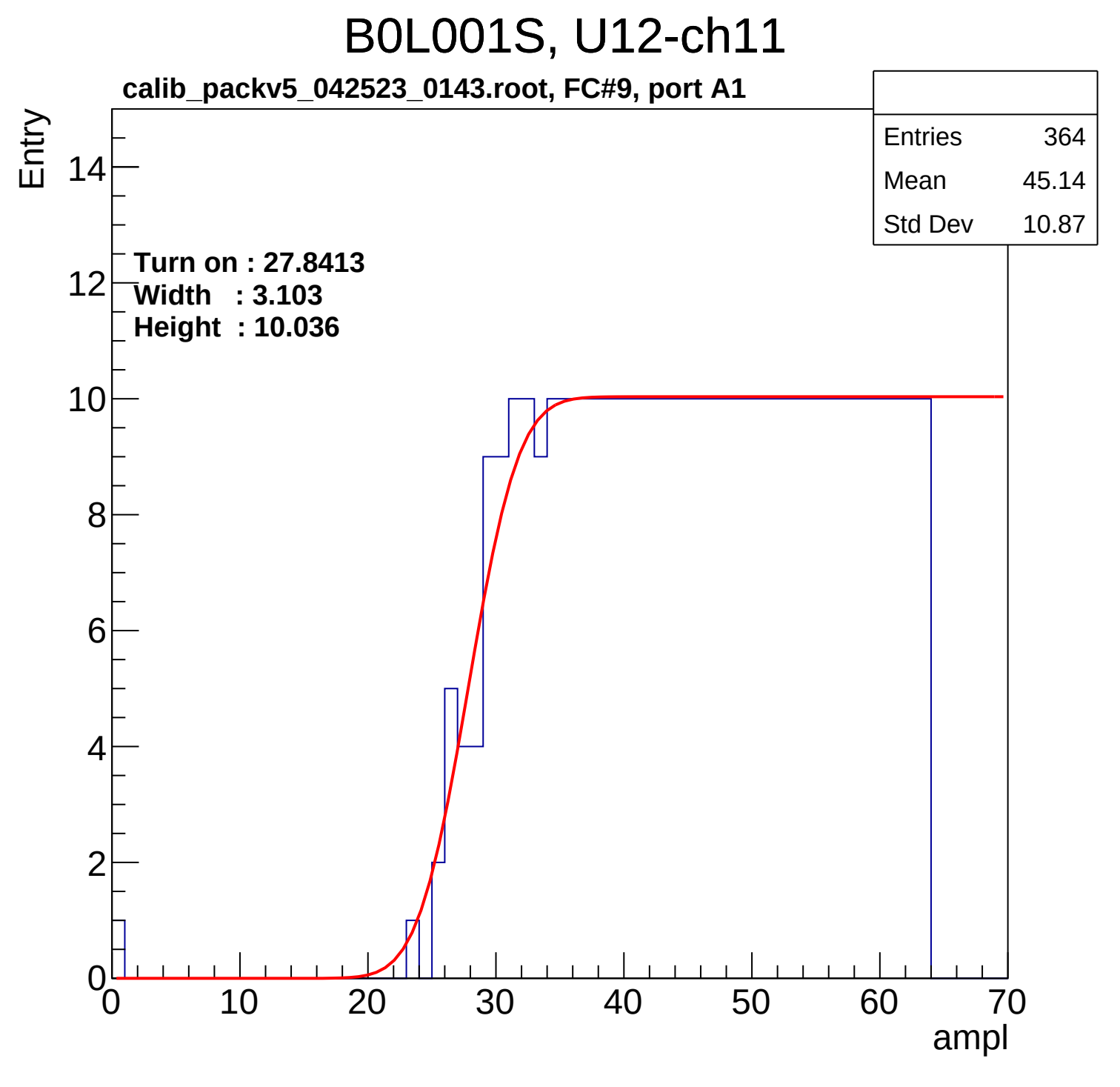
B0L001S, U12-ch11
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 45.14
Std Dev 10.87
Turn on : 27.8413
Width : 3.103
Height : 10.036
Entry
ampl
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6
8
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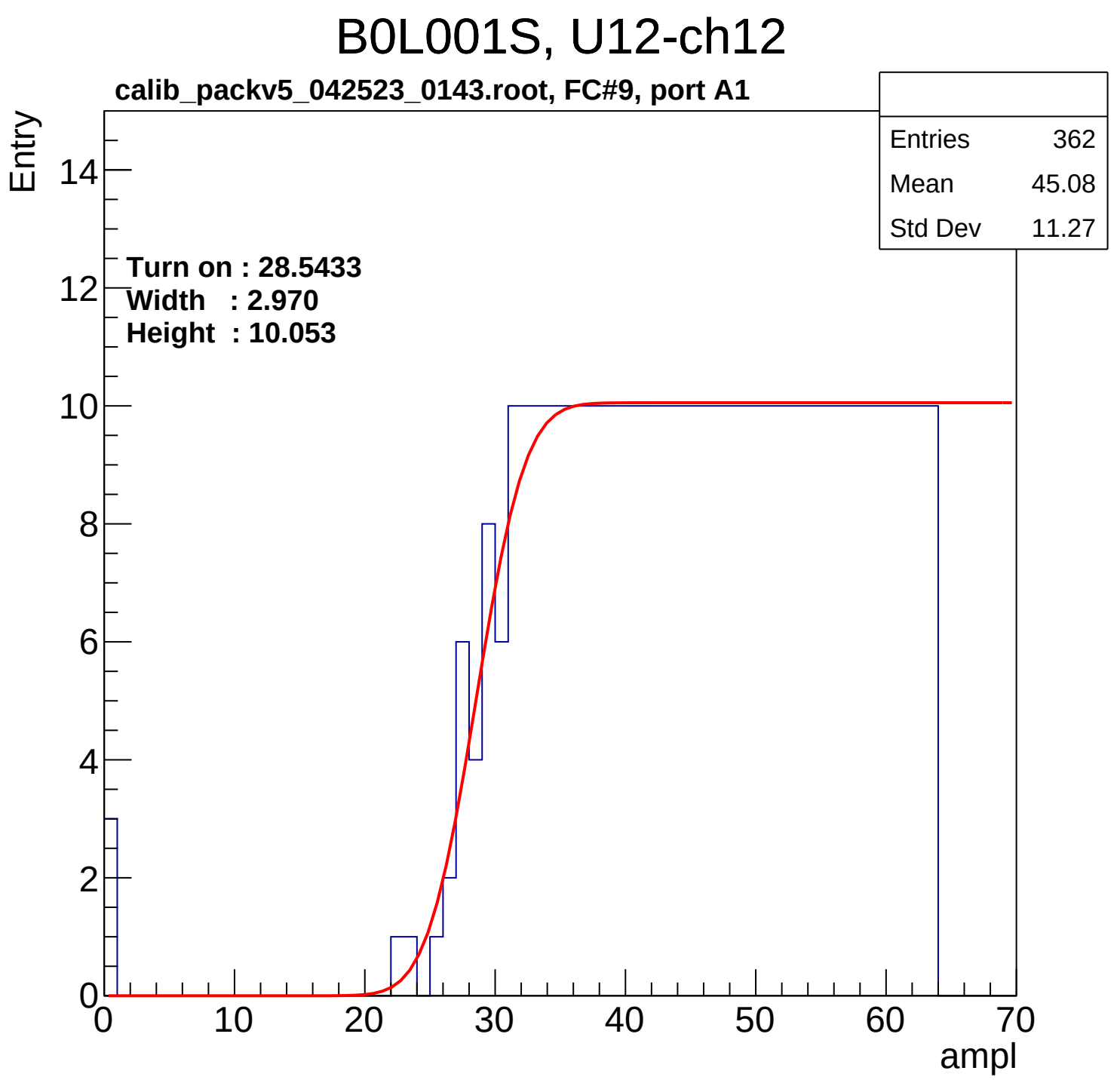
B0L001S, U12-ch12
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 45.08
Std Dev 11.27
Turn on : 28.5433
Width : 2.970
Height : 10.053
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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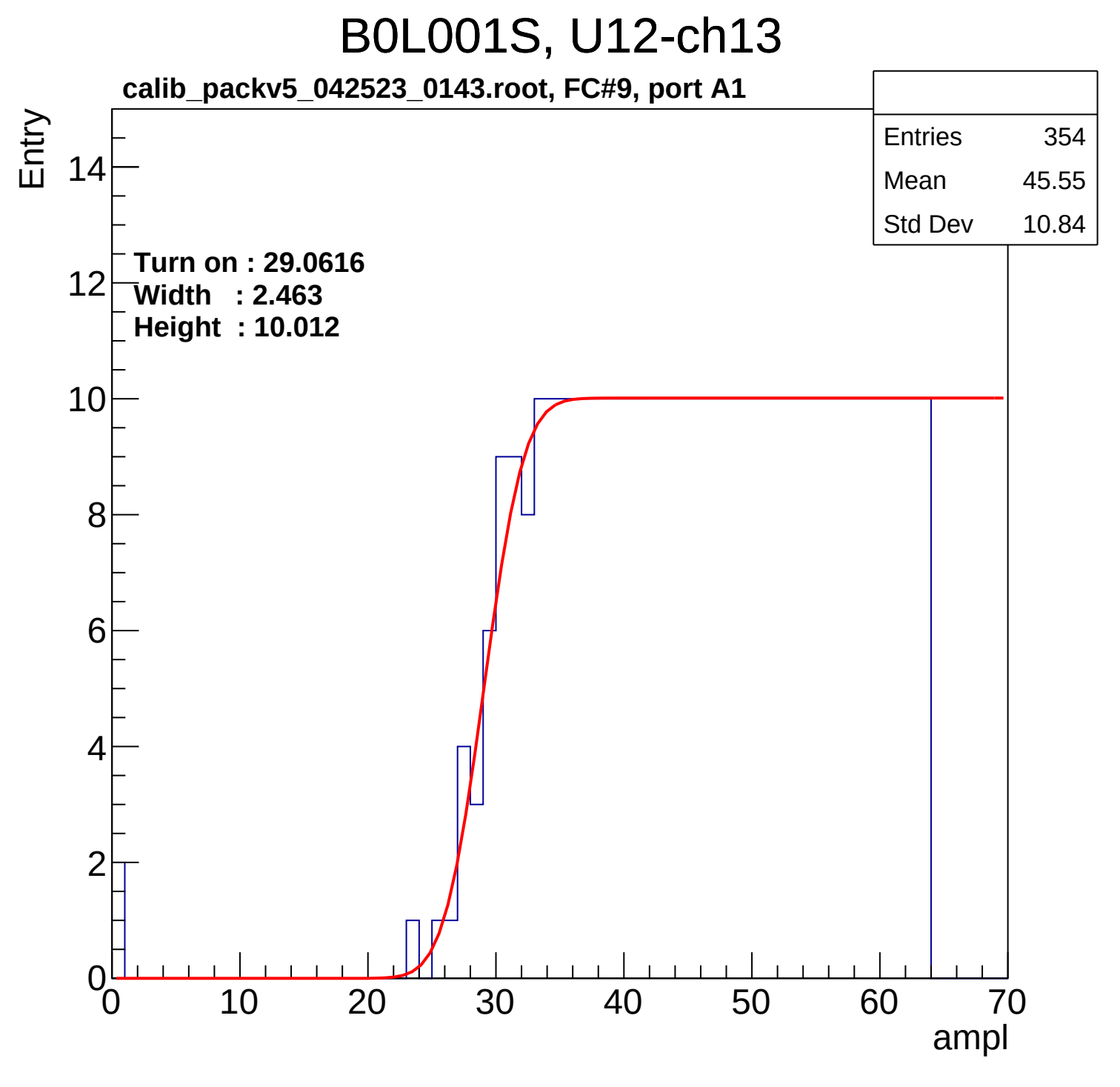
B0L001S, U12-ch13
calib_packv5_042523_0143.root, FC#9, port A1
Entries 354
Mean 45.55
Std Dev 10.84
Turn on : 29.0616
Width : 2.463
Height : 10.012
Entry
ampl
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6
8
10
12
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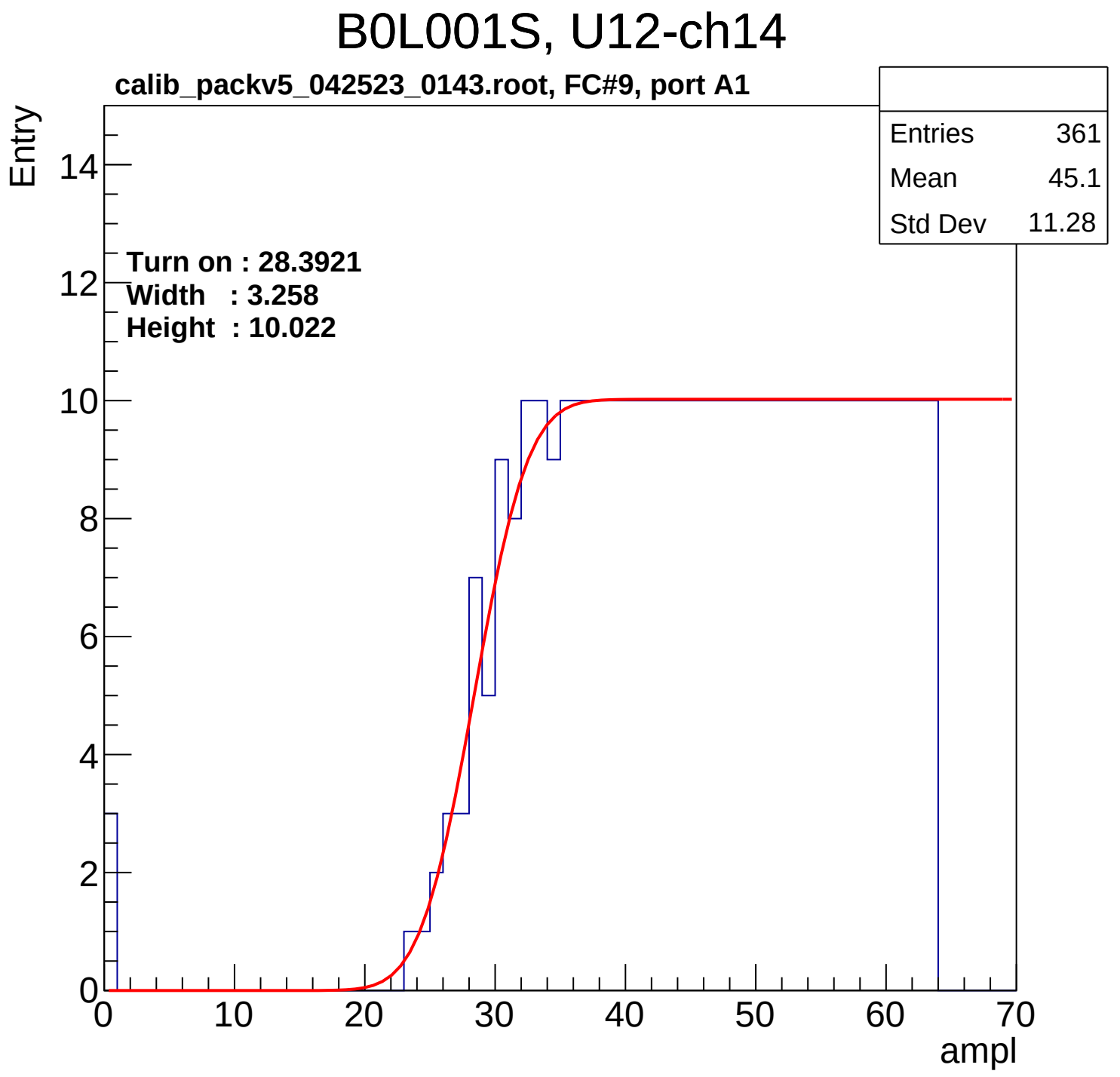
B0L001S, U12-ch14
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 45.1
Std Dev 11.28
Turn on : 28.3921
Width : 3.258
Height : 10.022
Entry
ampl
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6
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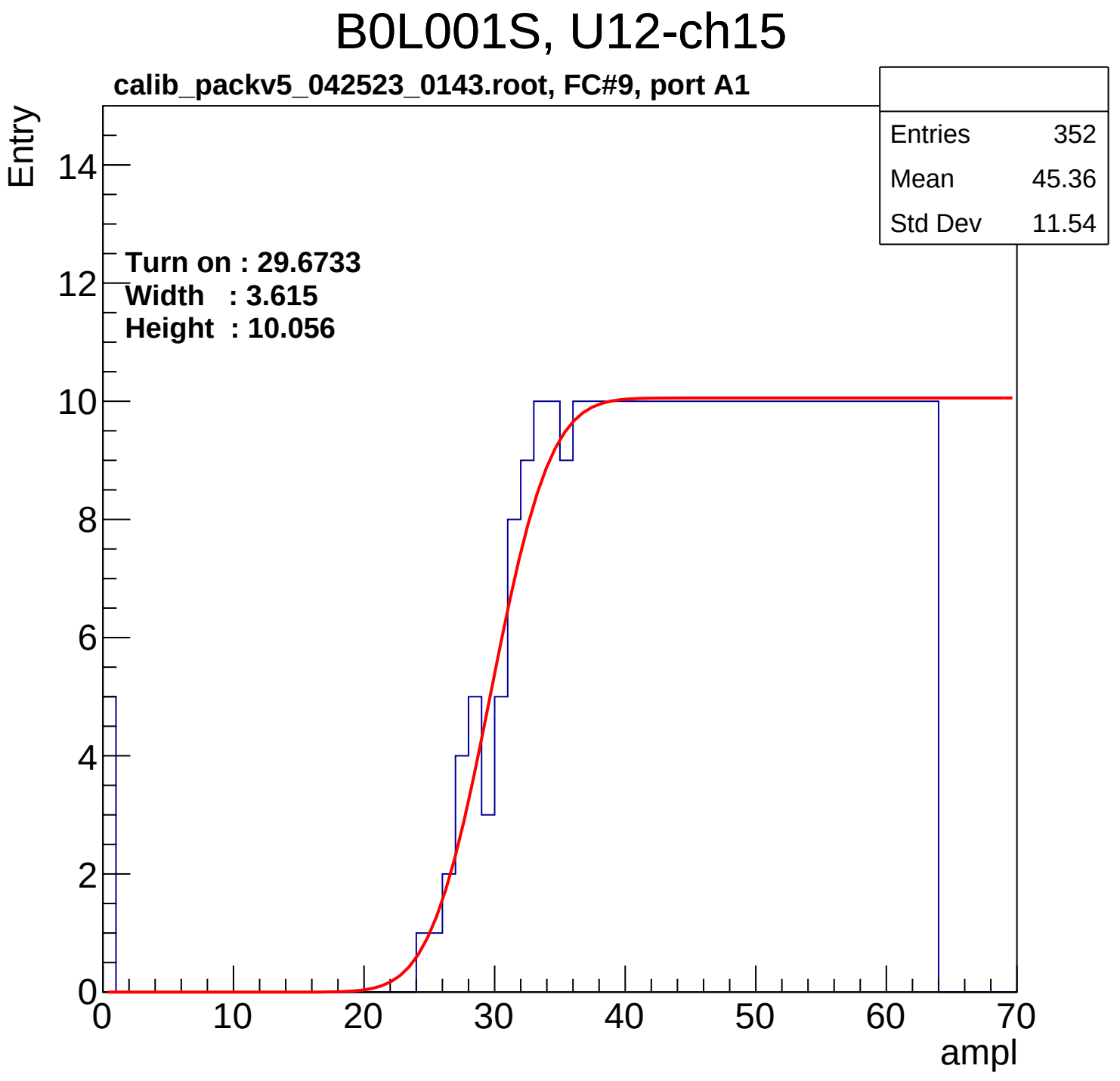
B0L001S, U12-ch15
calib_packv5_042523_0143.root, FC#9, port A1
Entries 352
Mean 45.36
Std Dev 11.54
Turn on : 29.6733
Width : 3.615
Height : 10.056
Entry
ampl
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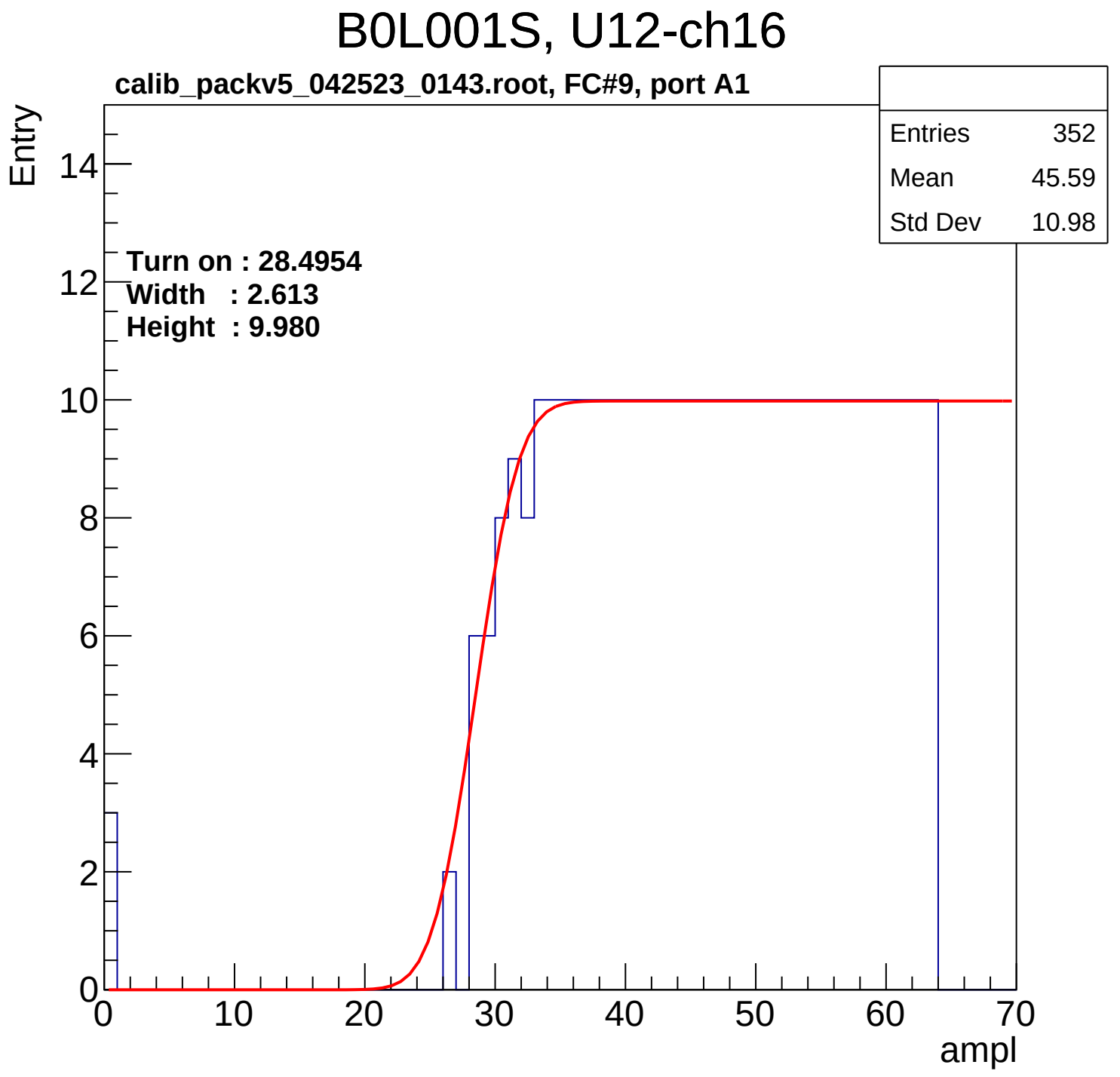
B0L001S, U12-ch16
calib_packv5_042523_0143.root, FC#9, port A1
Entries 352
Mean 45.59
Std Dev 10.98
Turn on : 28.4954
Width : 2.613
Height : 9.980
Entry
ampl
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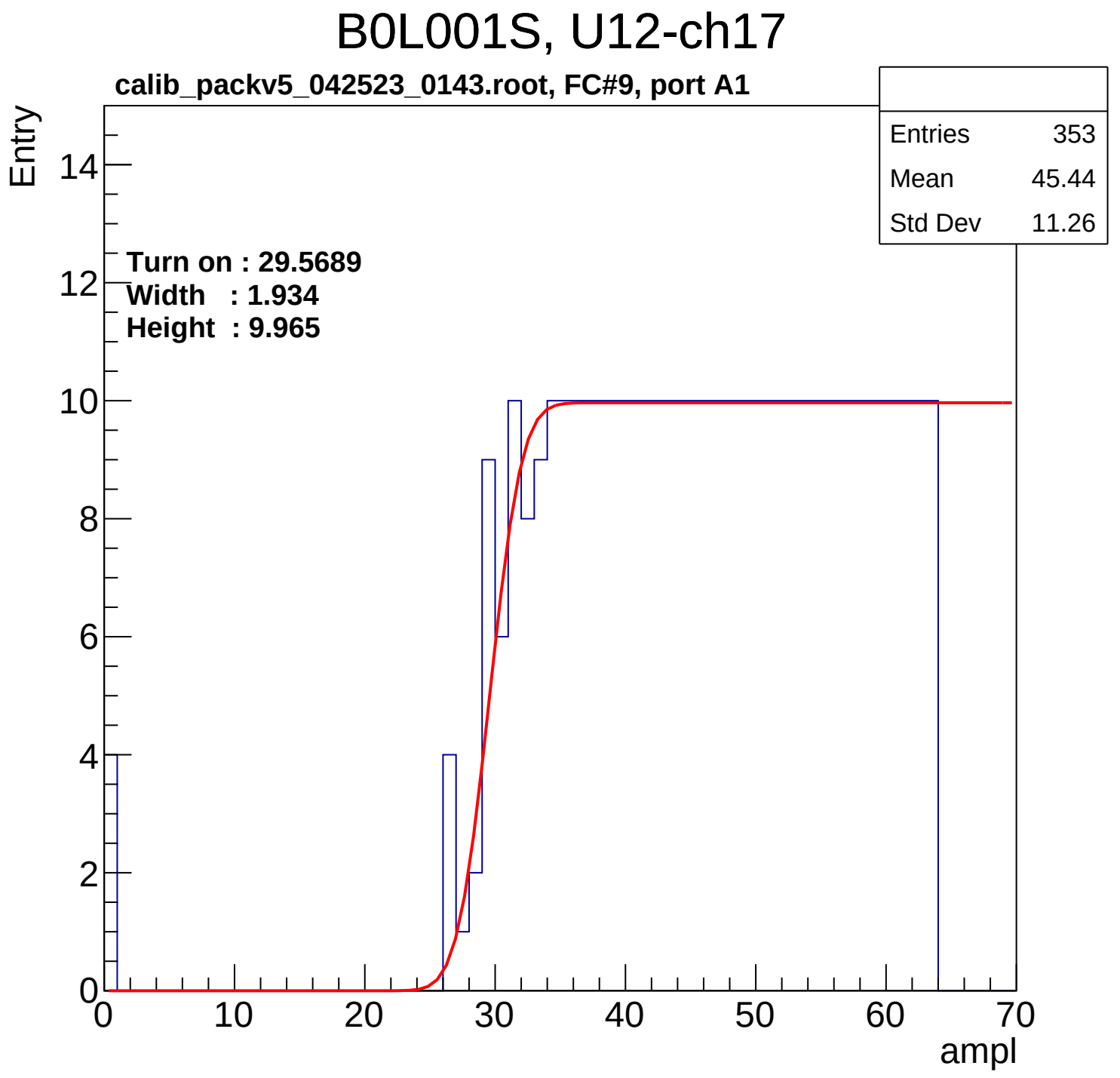
B0L001S, U12-ch17
calib_packv5_042523_0143.root, FC#9, port A1
Entries 353
Mean 45.44
Std Dev 11.26
Turn on : 29.5689
Width : 1.934
Height : 9.965
Entry
ampl
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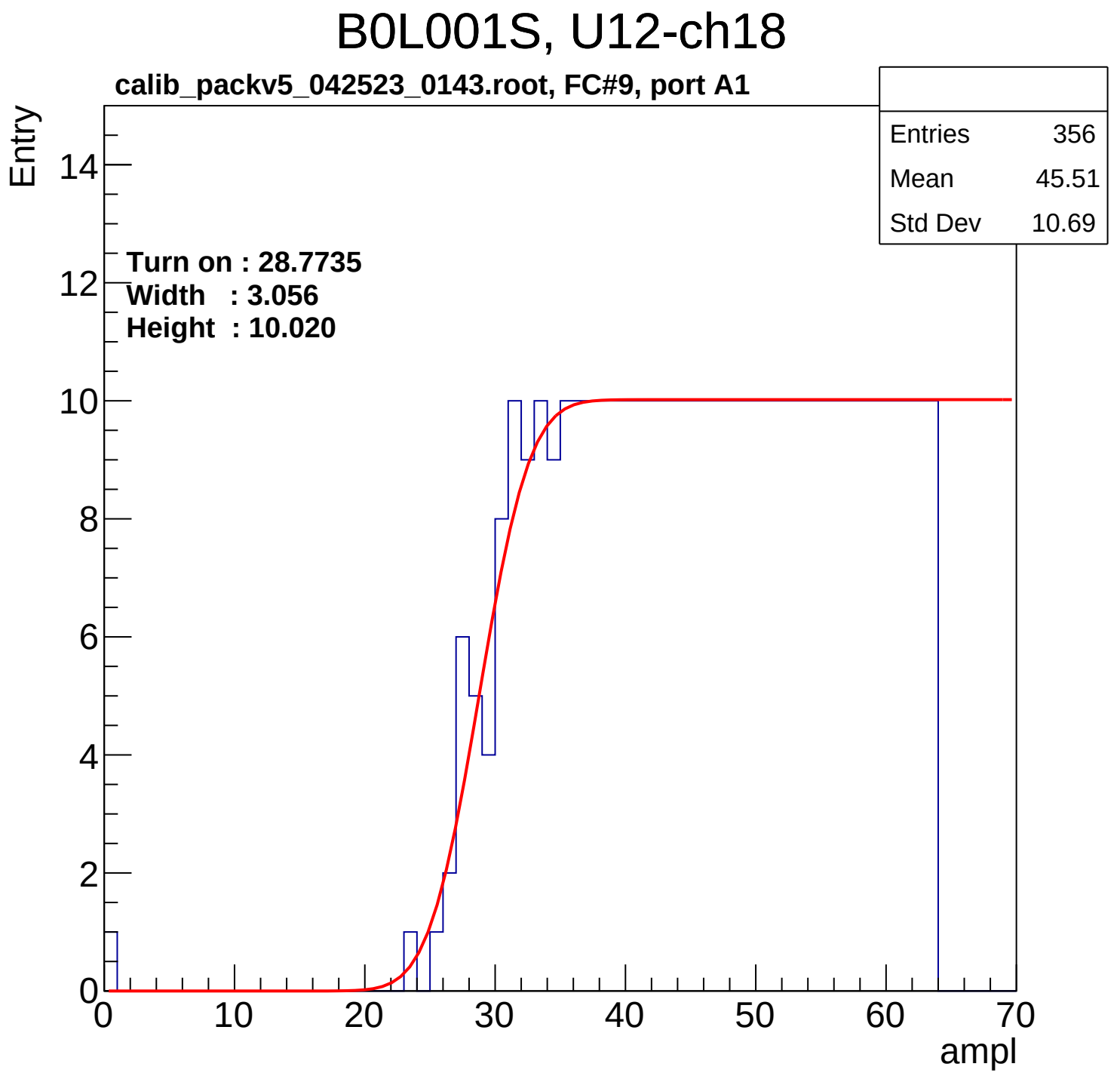
B0L001S, U12-ch18
calib_packv5_042523_0143.root, FC#9, port A1
Entries 356
Mean 45.51
Std Dev 10.69
Turn on : 28.7735
Width : 3.056
Height : 10.020
Entry
ampl
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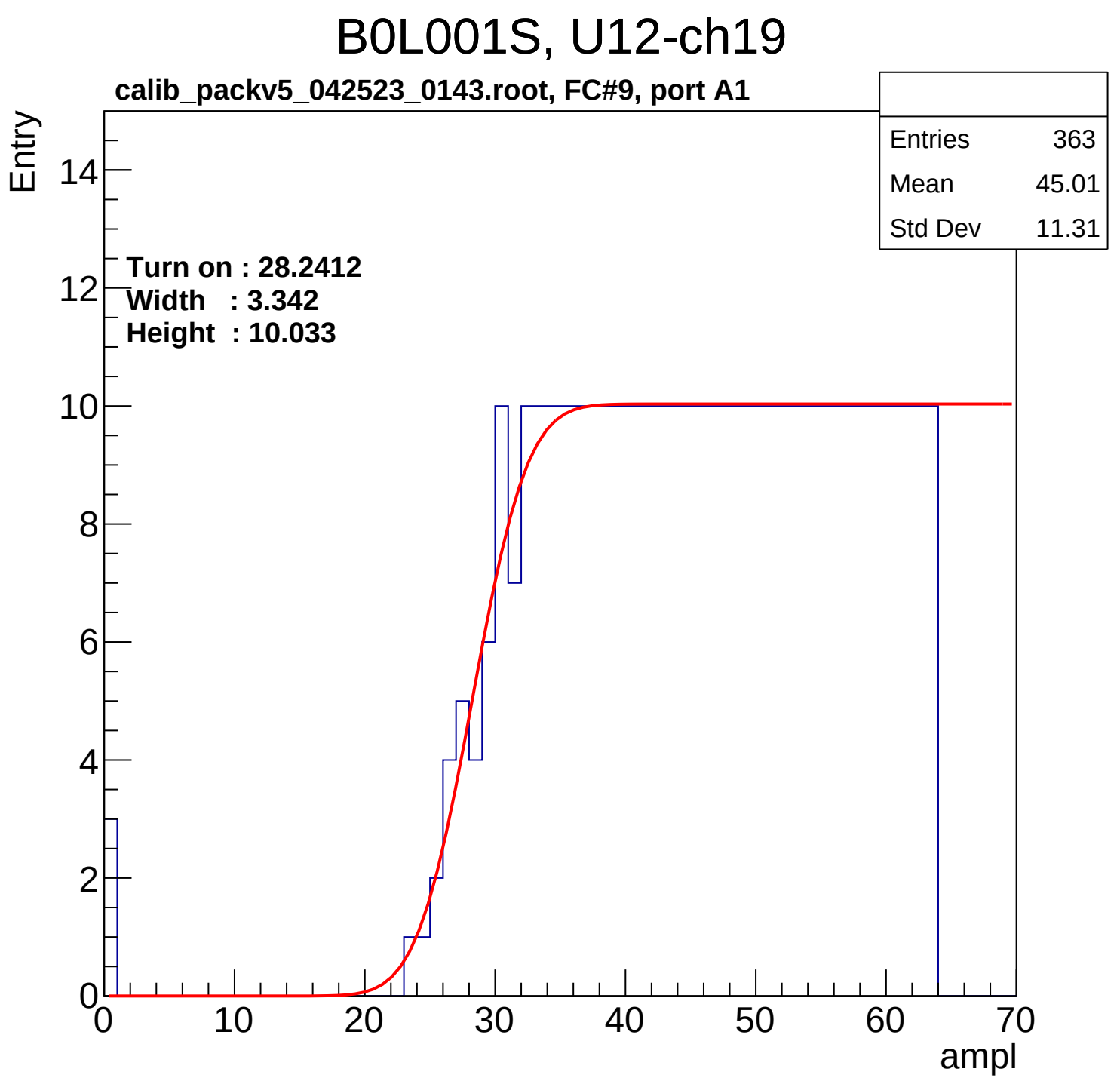
B0L001S, U12-ch19
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 45.01
Std Dev 11.31
Turn on : 28.2412
Width : 3.342
Height : 10.033
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ampl
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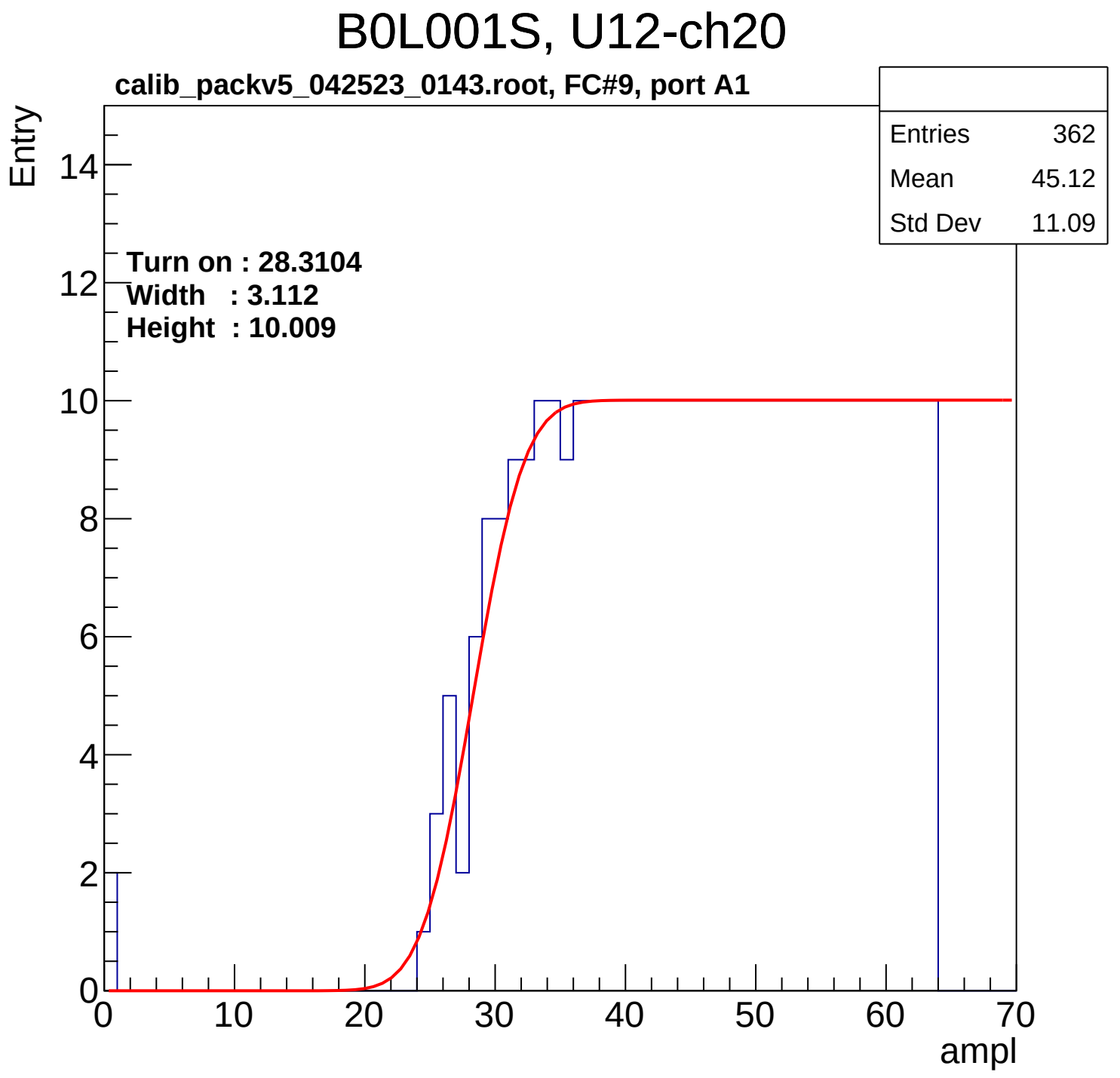
B0L001S, U12-ch20
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 45.12
Std Dev 11.09
Turn on : 28.3104
Width : 3.112
Height : 10.009
Entry
ampl
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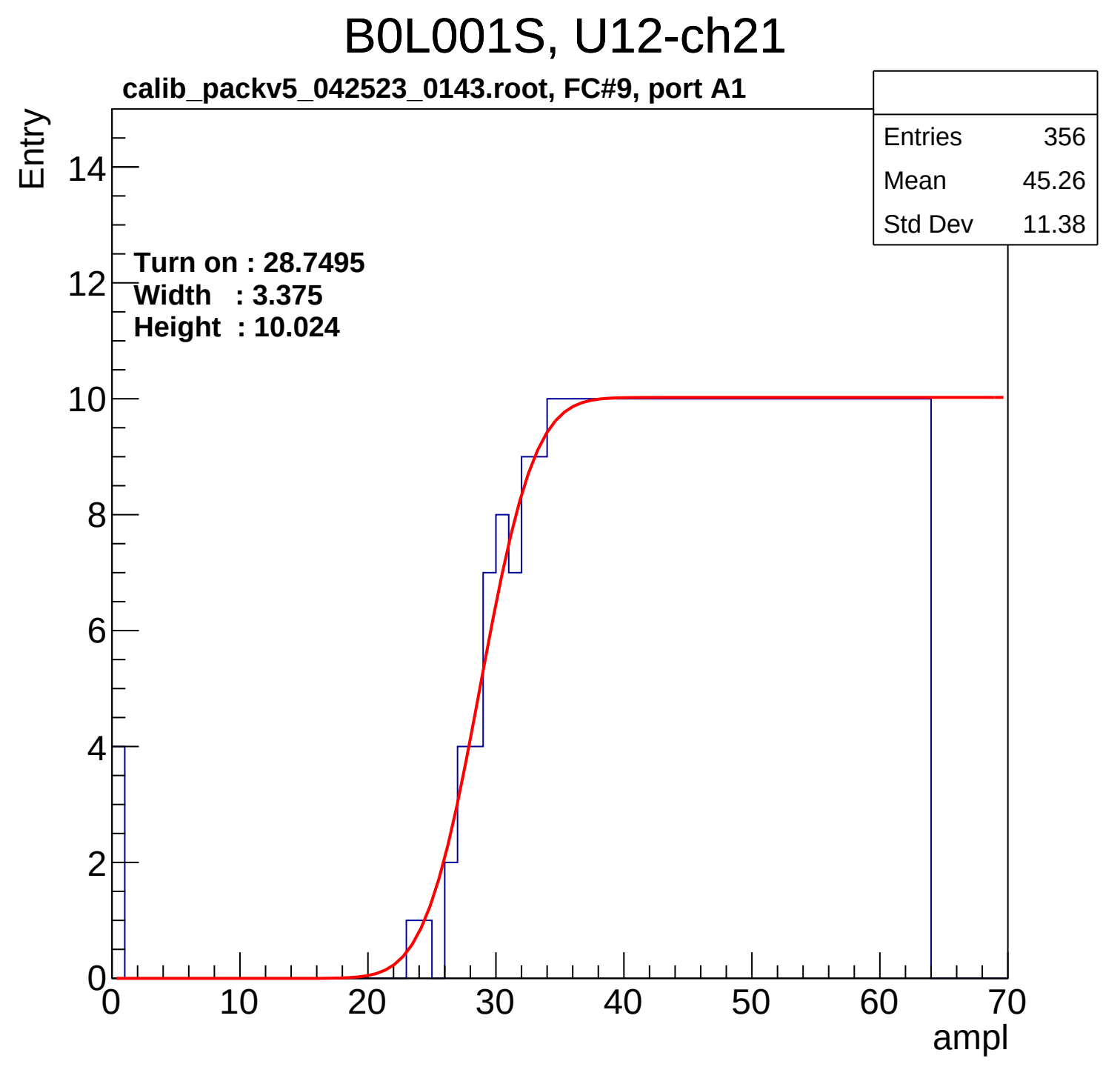
B0L001S, U12-ch21
calib_packv5_042523_0143.root, FC#9, port A1
Entries 356
Mean 45.26
Std Dev 11.38
Turn on : 28.7495
Width : 3.375
Height : 10.024
Entry
ampl
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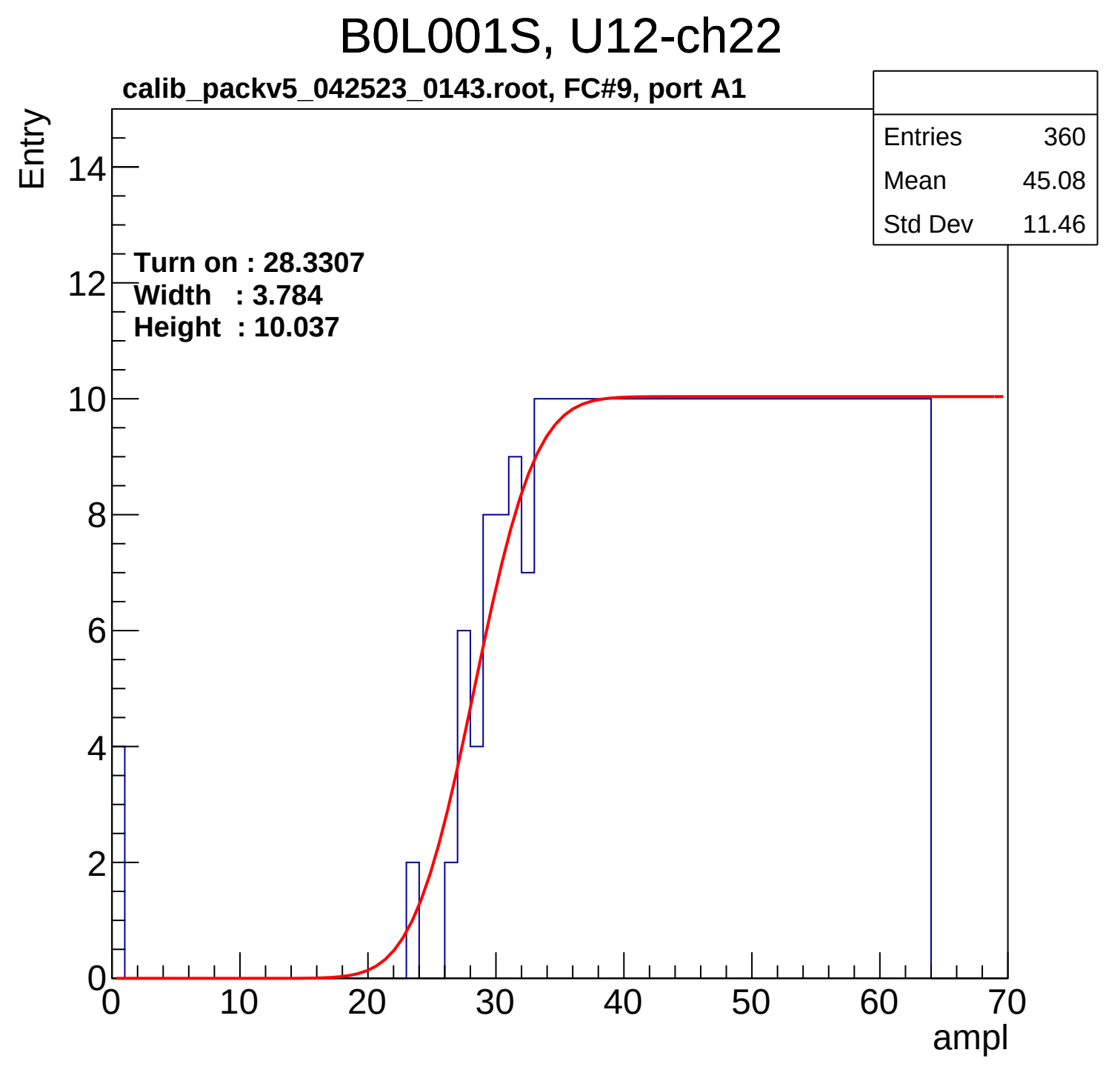
B0L001S, U12-ch22
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 45.08
Std Dev 11.46
Turn on : 28.3307
Width : 3.784
Height : 10.037
Entry
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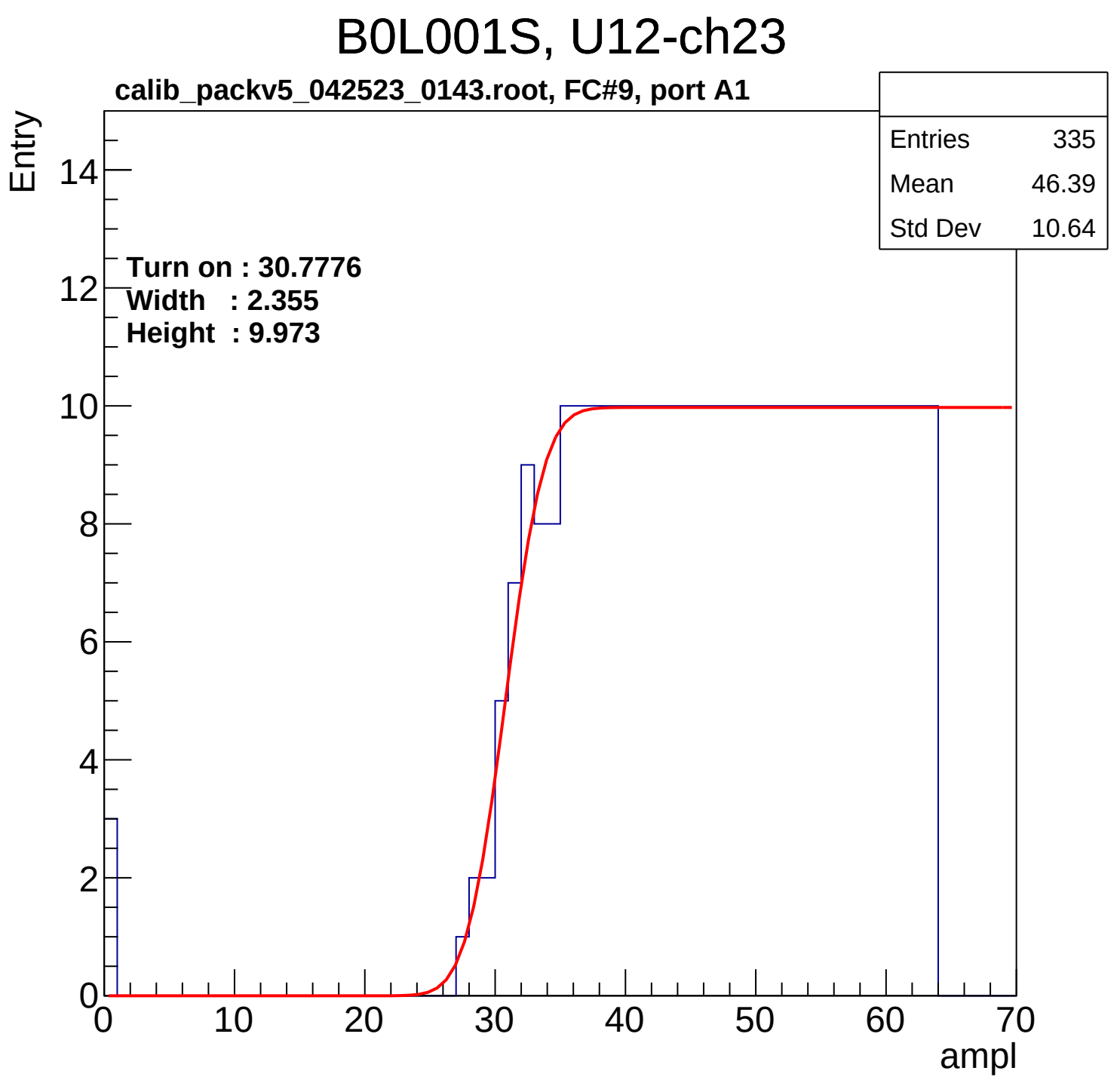
B0L001S, U12-ch23
calib_packv5_042523_0143.root, FC#9, port A1
Entries 335
Mean 46.39
Std Dev 10.64
Turn on : 30.7776
Width : 2.355
Height : 9.973
Entry
ampl
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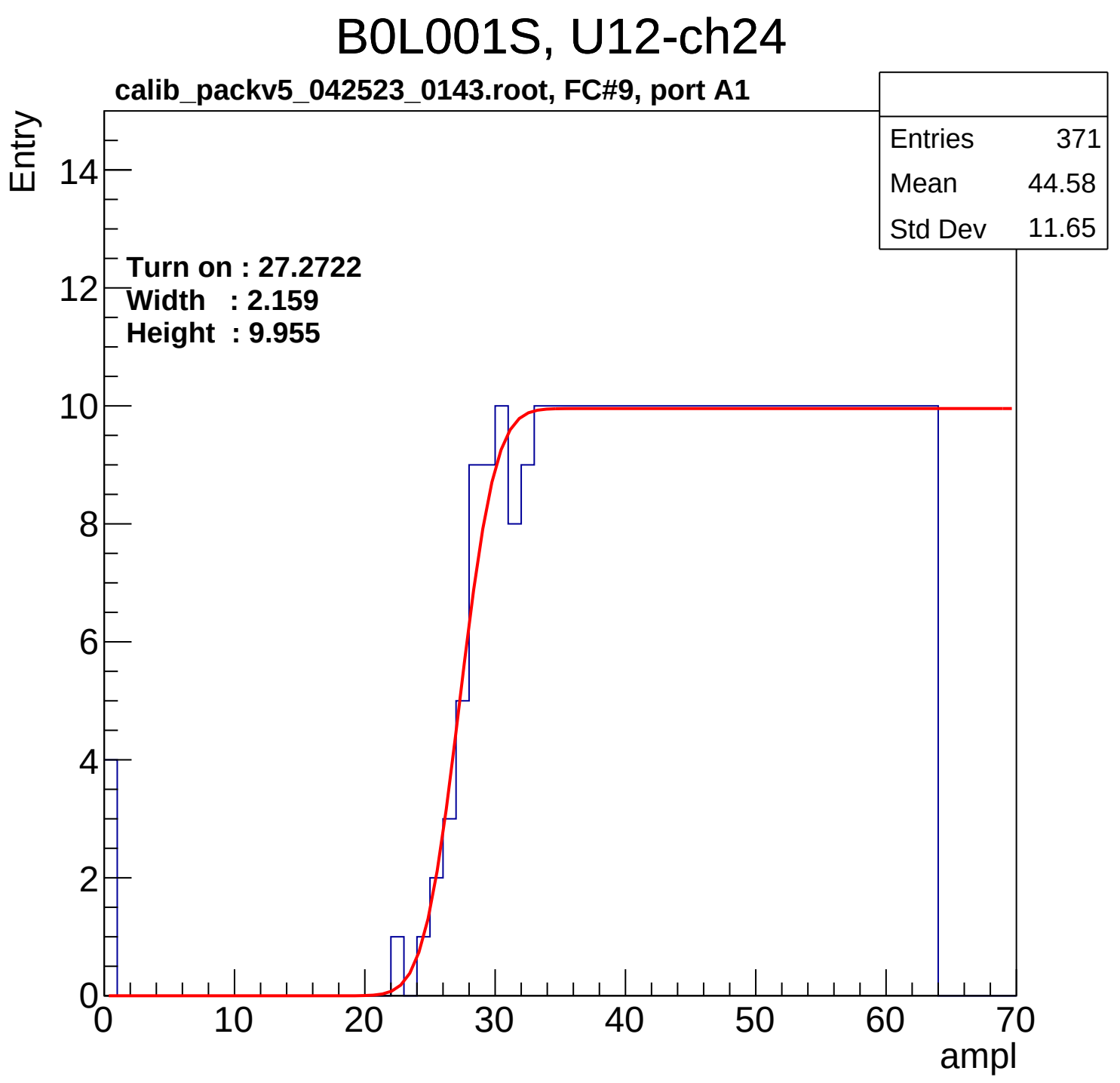
B0L001S, U12-ch24
calib_packv5_042523_0143.root, FC#9, port A1
Entries 371
Mean 44.58
Std Dev 11.65
Turn on : 27.2722
Width : 2.159
Height : 9.955
Entry
ampl
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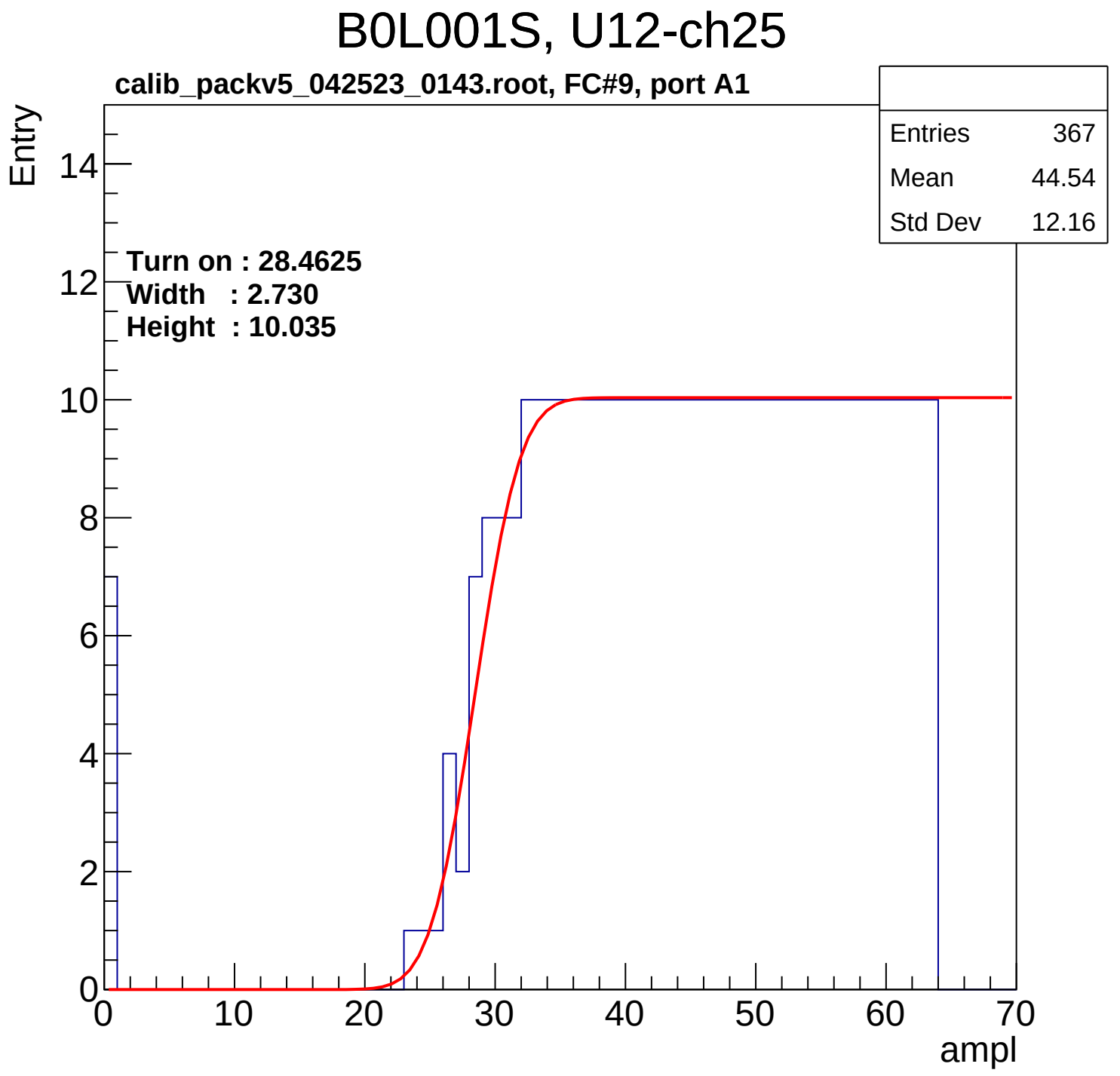
B0L001S, U12-ch25
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.54
Std Dev 12.16
Turn on : 28.4625
Width : 2.730
Height : 10.035
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ampl
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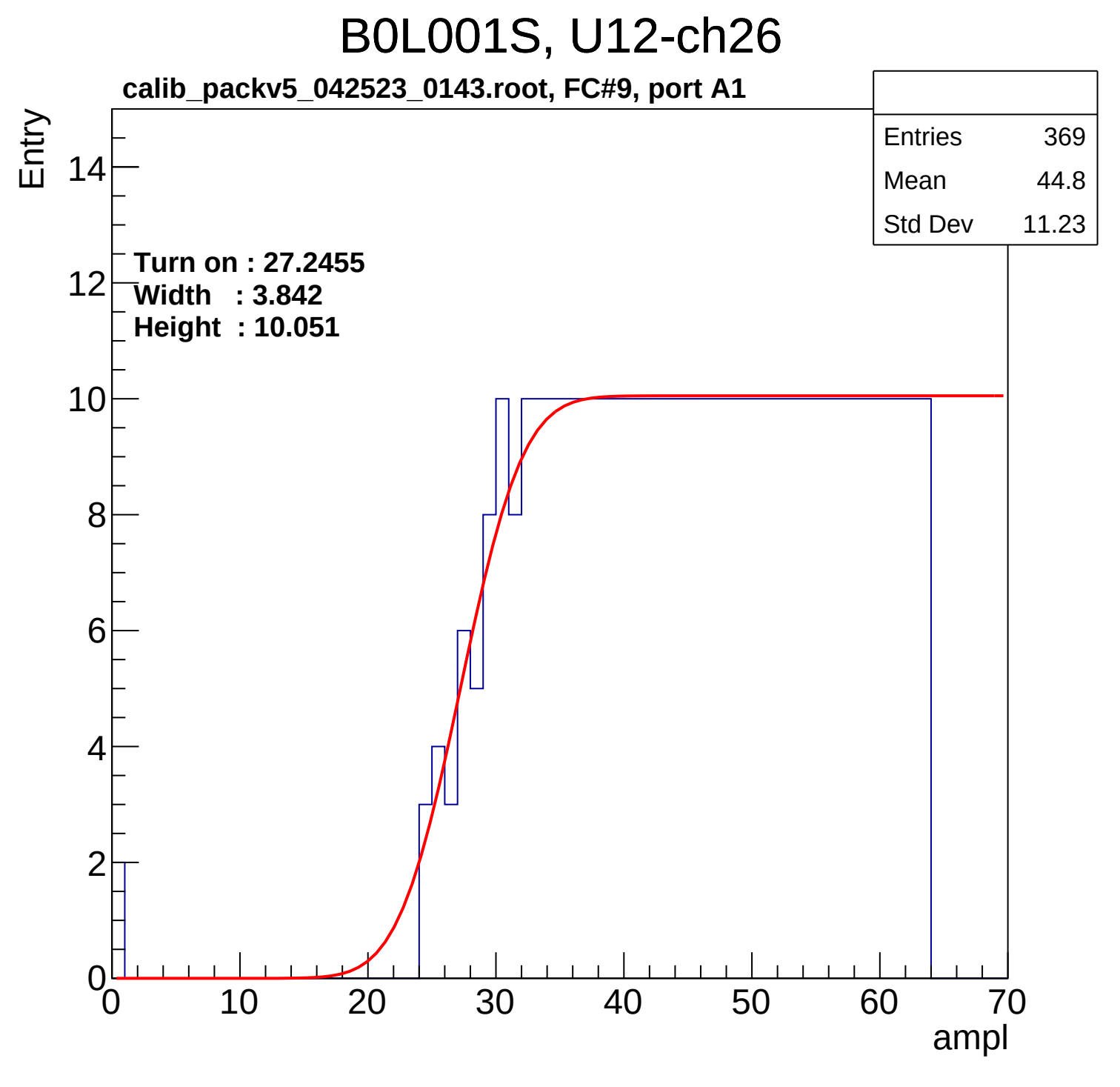
B0L001S, U12-ch26
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.8
Std Dev 11.23
Turn on : 27.2455
Width : 3.842
Height : 10.051
Entry
ampl
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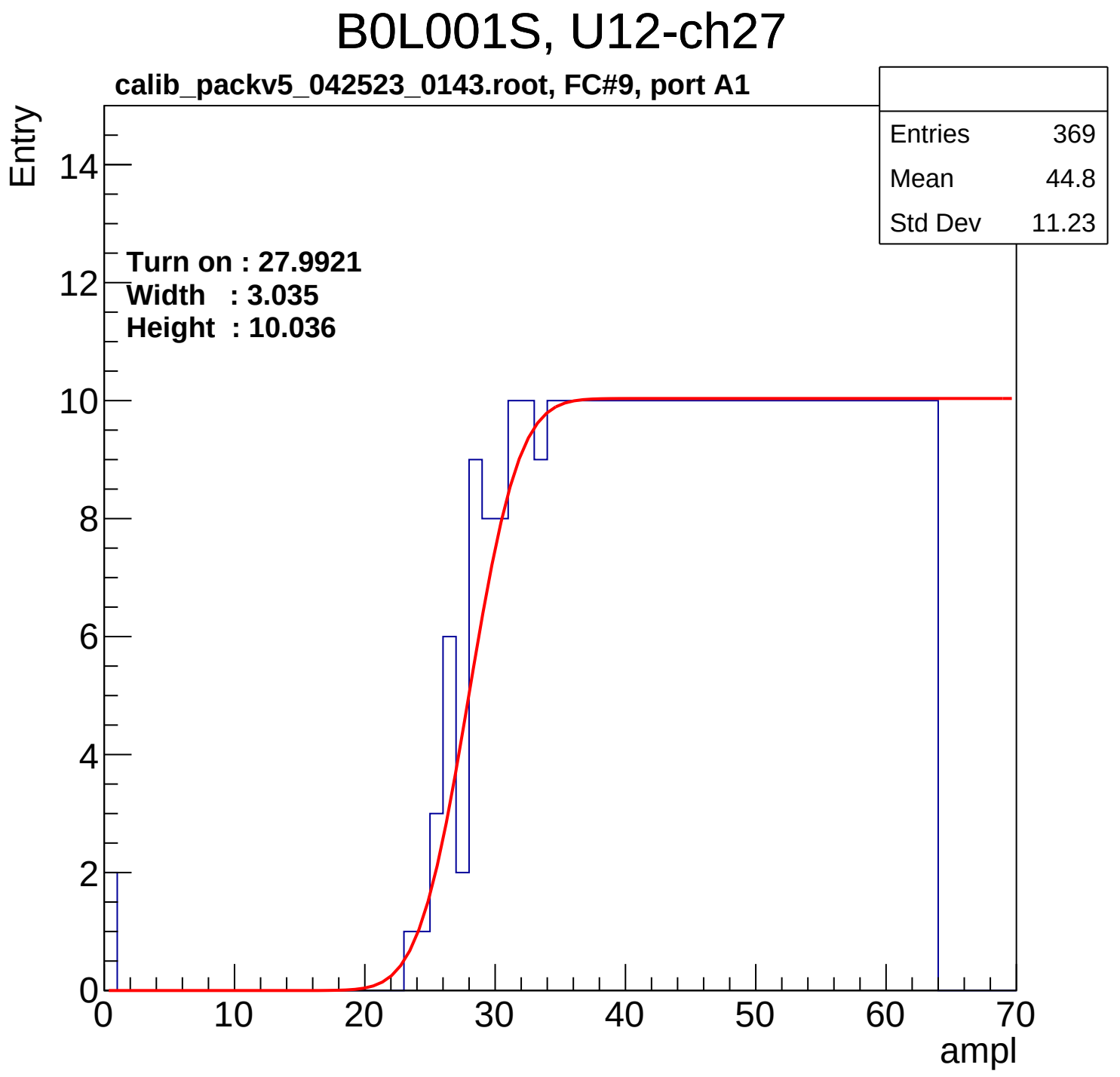
B0L001S, U12-ch27
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.8
Std Dev 11.23
Turn on : 27.9921
Width : 3.035
Height : 10.036
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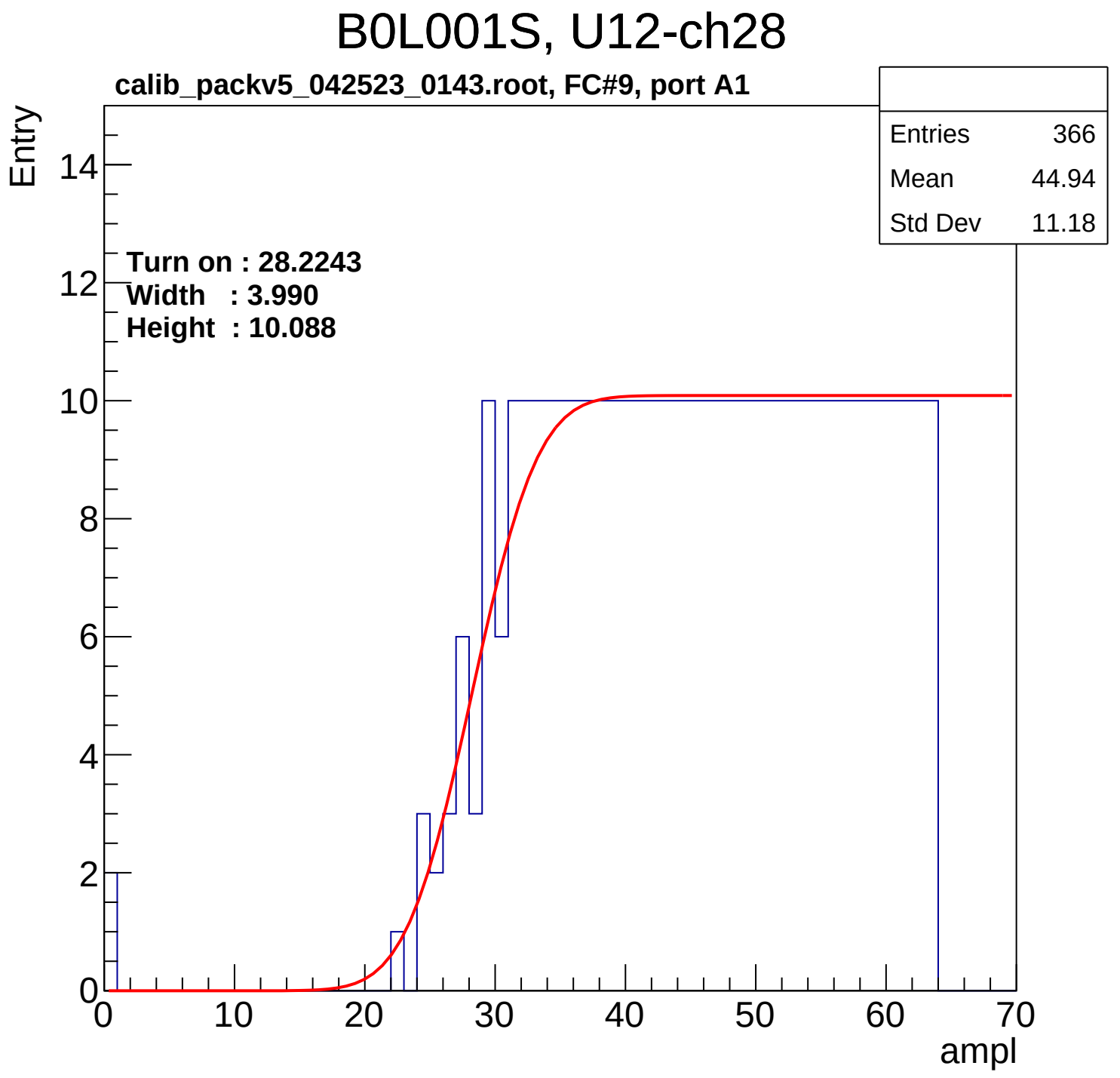
B0L001S, U12-ch28
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.94
Std Dev 11.18
Turn on : 28.2243
Width : 3.990
Height : 10.088
Entry
ampl
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20
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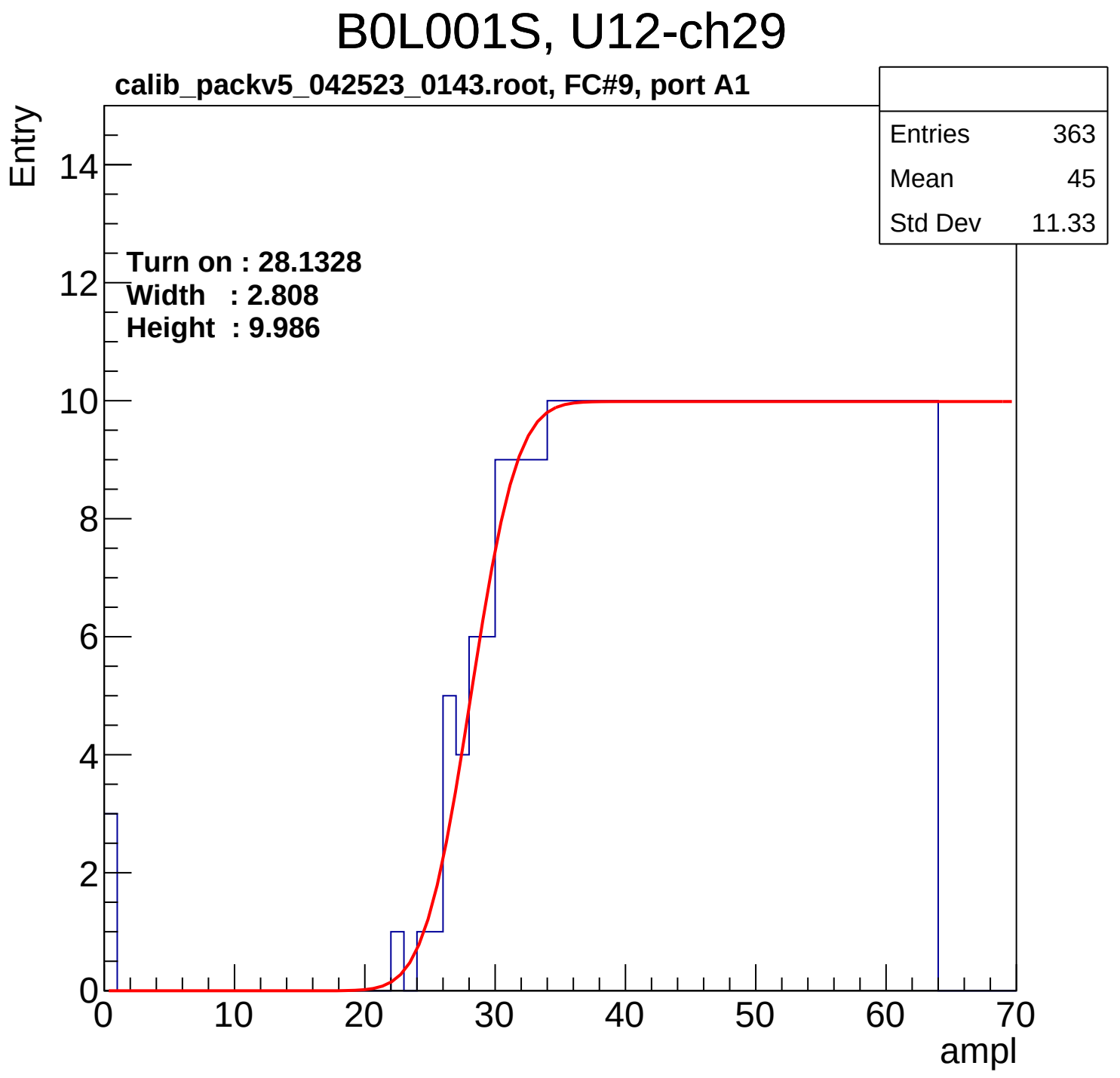
B0L001S, U12-ch29
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 45
Std Dev 11.33
Turn on : 28.1328
Width : 2.808
Height : 9.986
Entry
ampl
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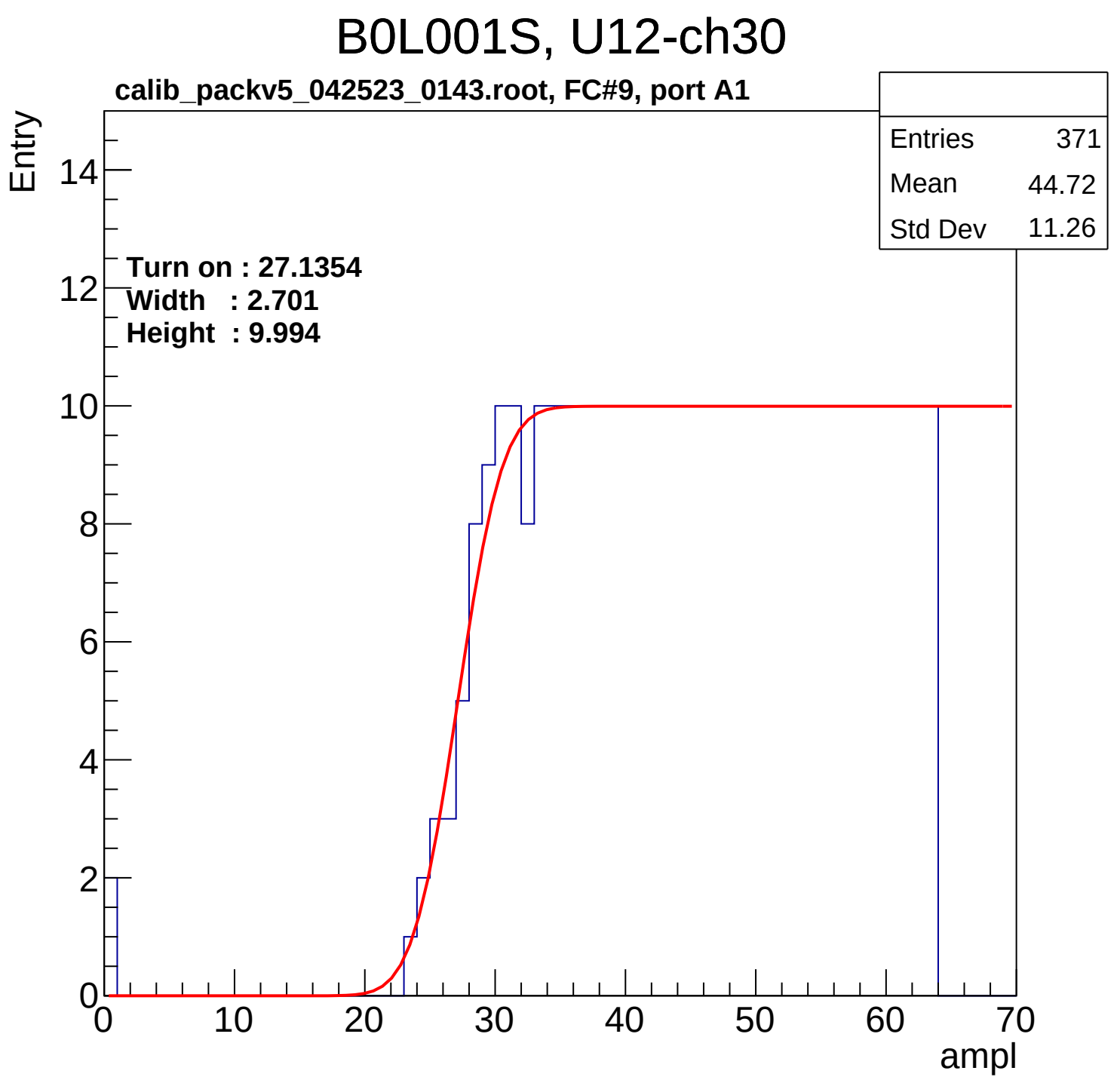
B0L001S, U12-ch30
calib_packv5_042523_0143.root, FC#9, port A1
Entries 371
Mean 44.72
Std Dev 11.26
Turn on : 27.1354
Width : 2.701
Height : 9.994
Entry
ampl
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2
4
6
8
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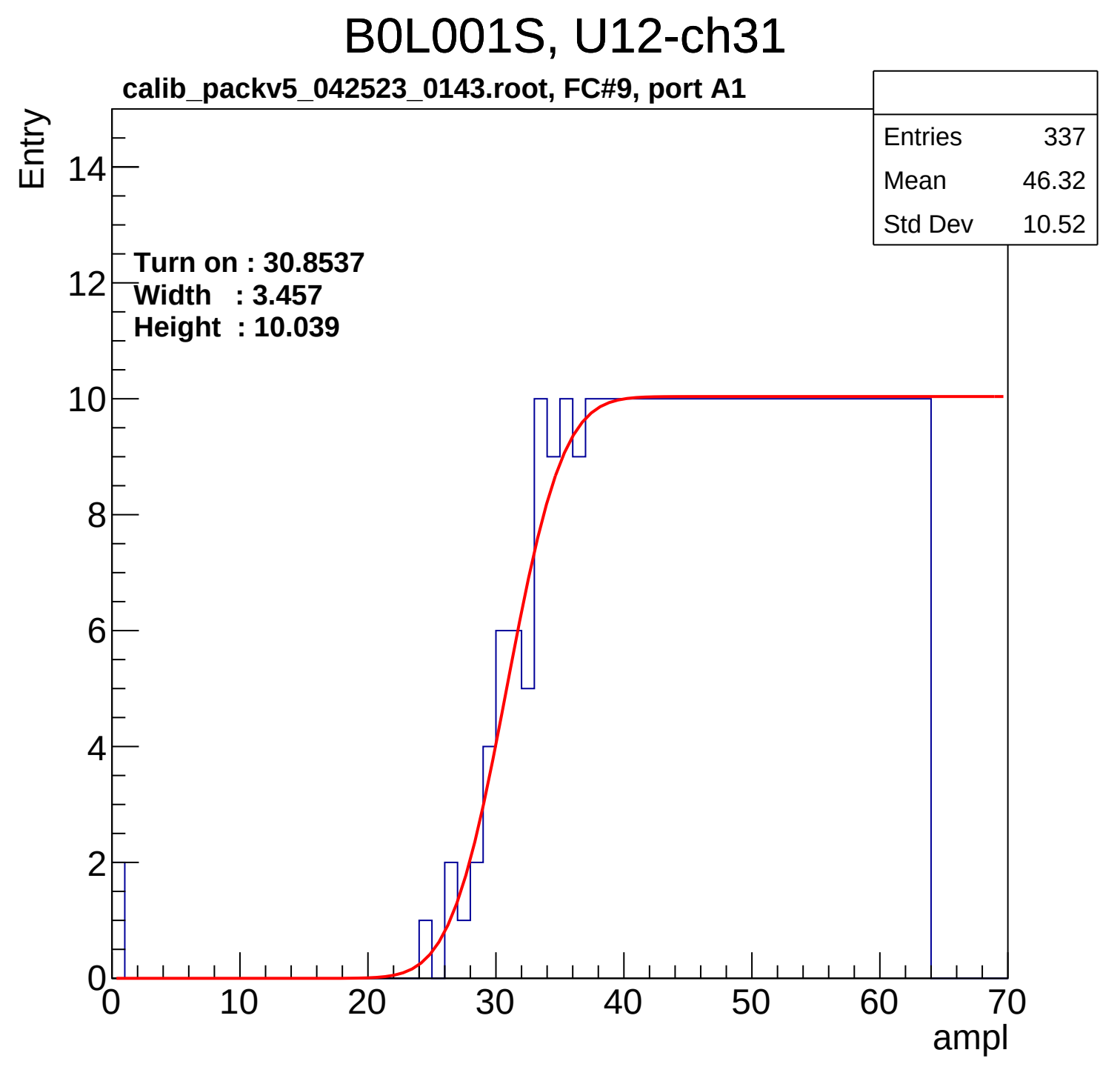
B0L001S, U12-ch31
calib_packv5_042523_0143.root, FC#9, port A1
Entries 337
Mean 46.32
Std Dev 10.52
Turn on : 30.8537
Width : 3.457
Height : 10.039
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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60
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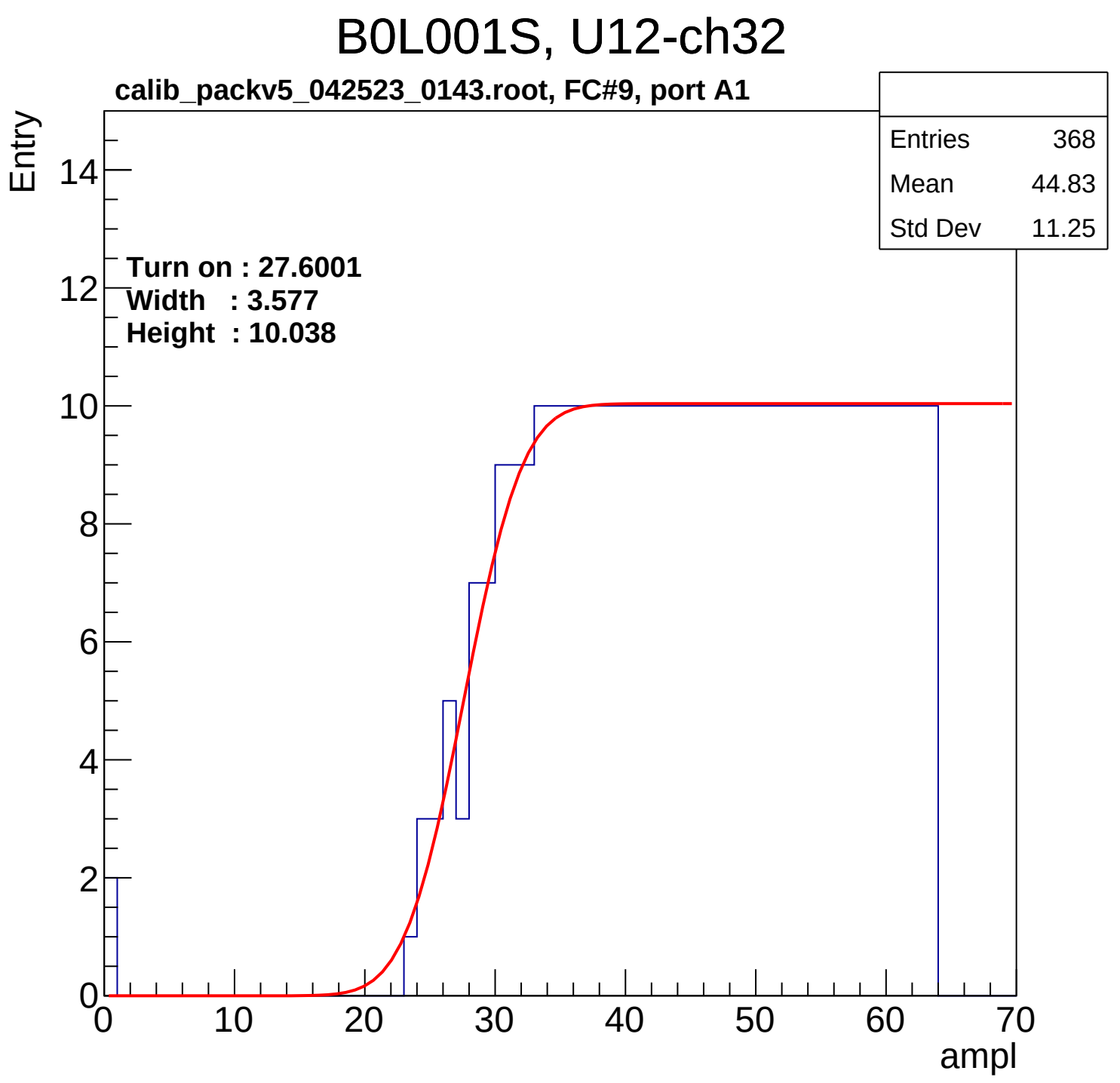
B0L001S, U12-ch32
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.83
Std Dev 11.25
Turn on : 27.6001
Width : 3.577
Height : 10.038
Entry
ampl
0
2
4
6
8
10
12
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0
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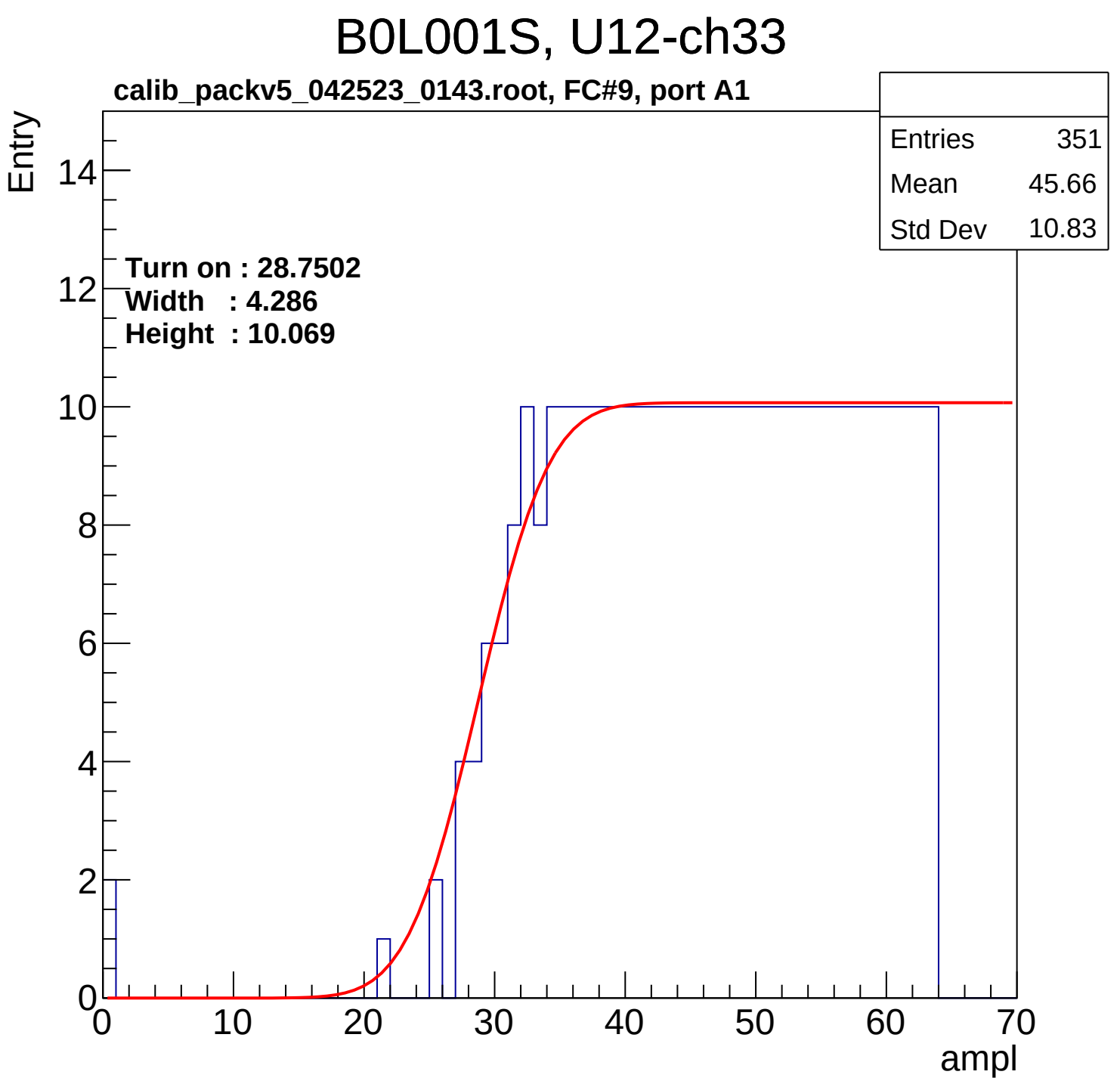
B0L001S, U12-ch33
calib_packv5_042523_0143.root, FC#9, port A1
Entries 351
Mean 45.66
Std Dev 10.83
Turn on : 28.7502
Width : 4.286
Height : 10.069
Entry
ampl
0
2
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6
8
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12
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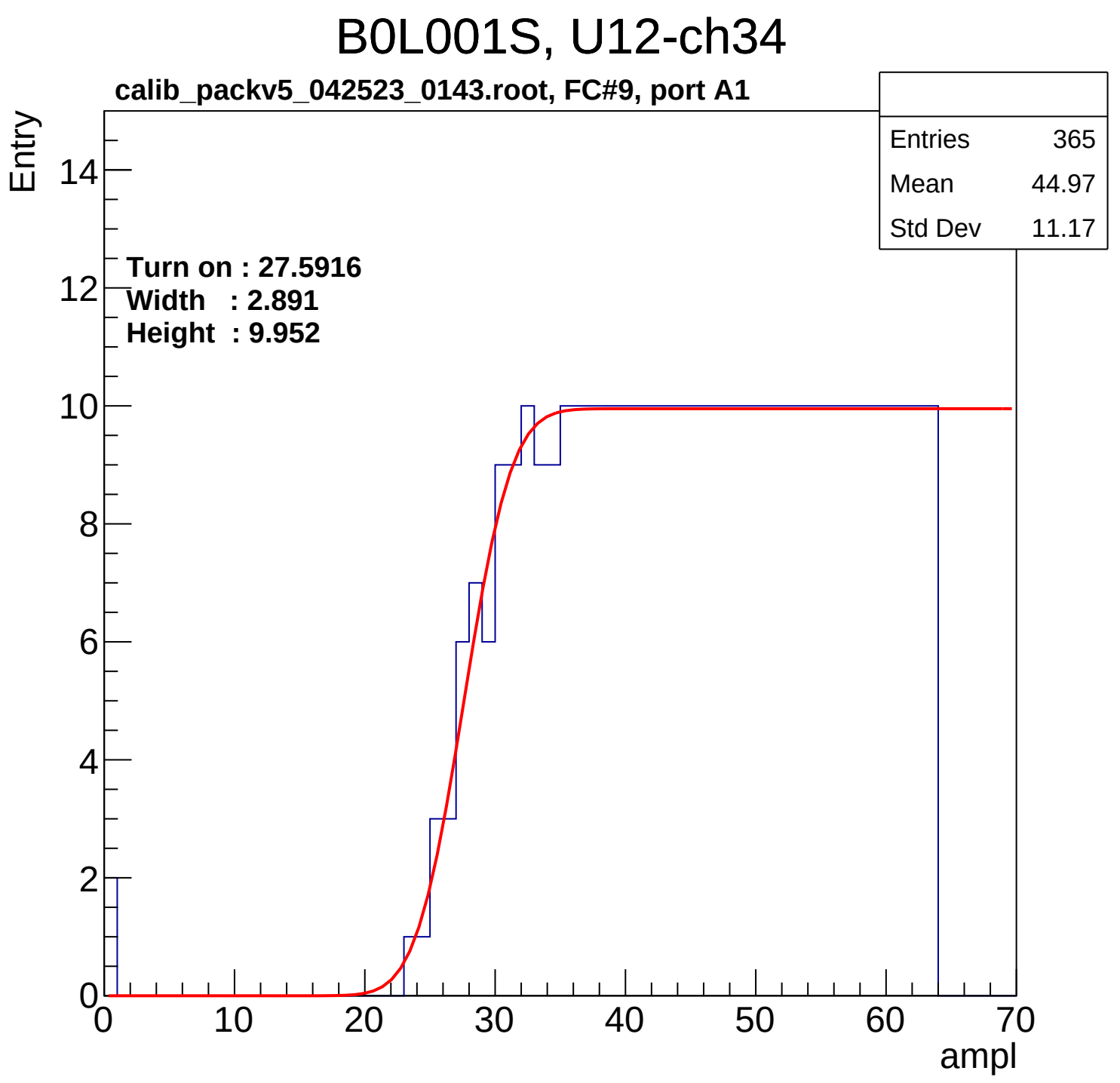
B0L001S, U12-ch34
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 44.97
Std Dev 11.17
Turn on : 27.5916
Width : 2.891
Height : 9.952
Entry
ampl
0
2
4
6
8
10
12
14
0
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40
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60
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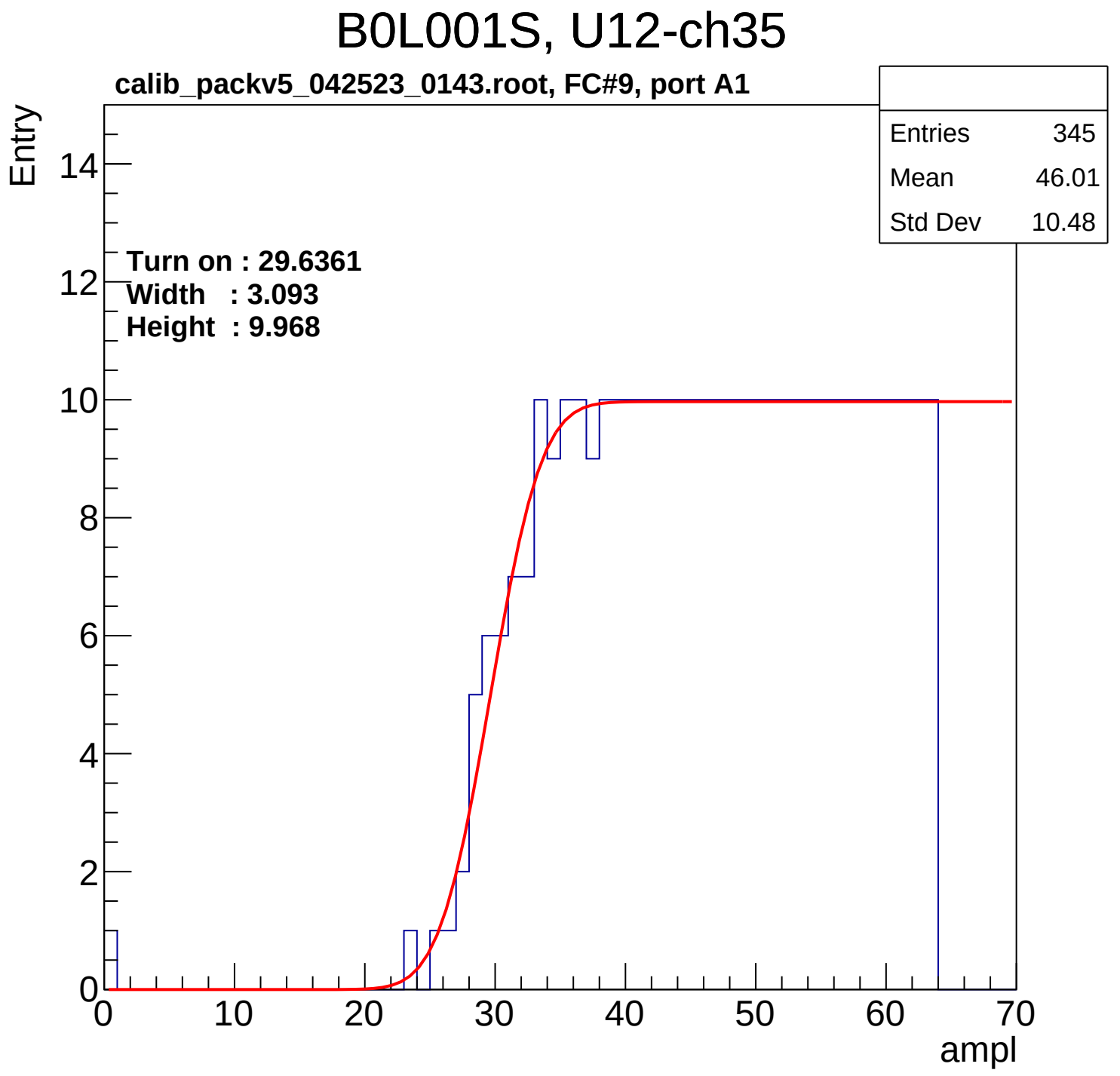
B0L001S, U12-ch35
calib_packv5_042523_0143.root, FC#9, port A1
Entries 345
Mean 46.01
Std Dev 10.48
Turn on : 29.6361
Width : 3.093
Height : 9.968
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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60
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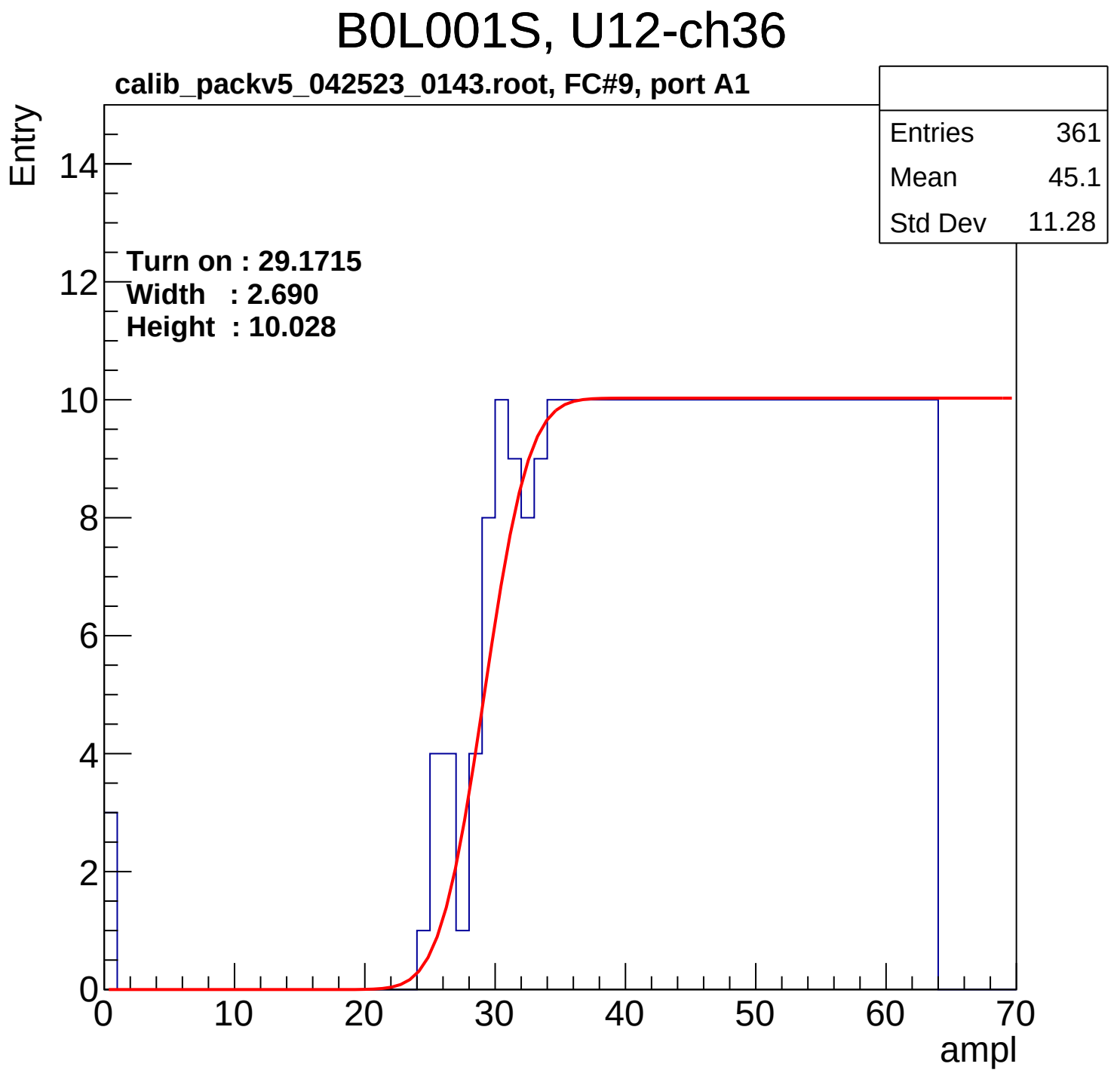
B0L001S, U12-ch36
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 45.1
Std Dev 11.28
Turn on : 29.1715
Width : 2.690
Height : 10.028
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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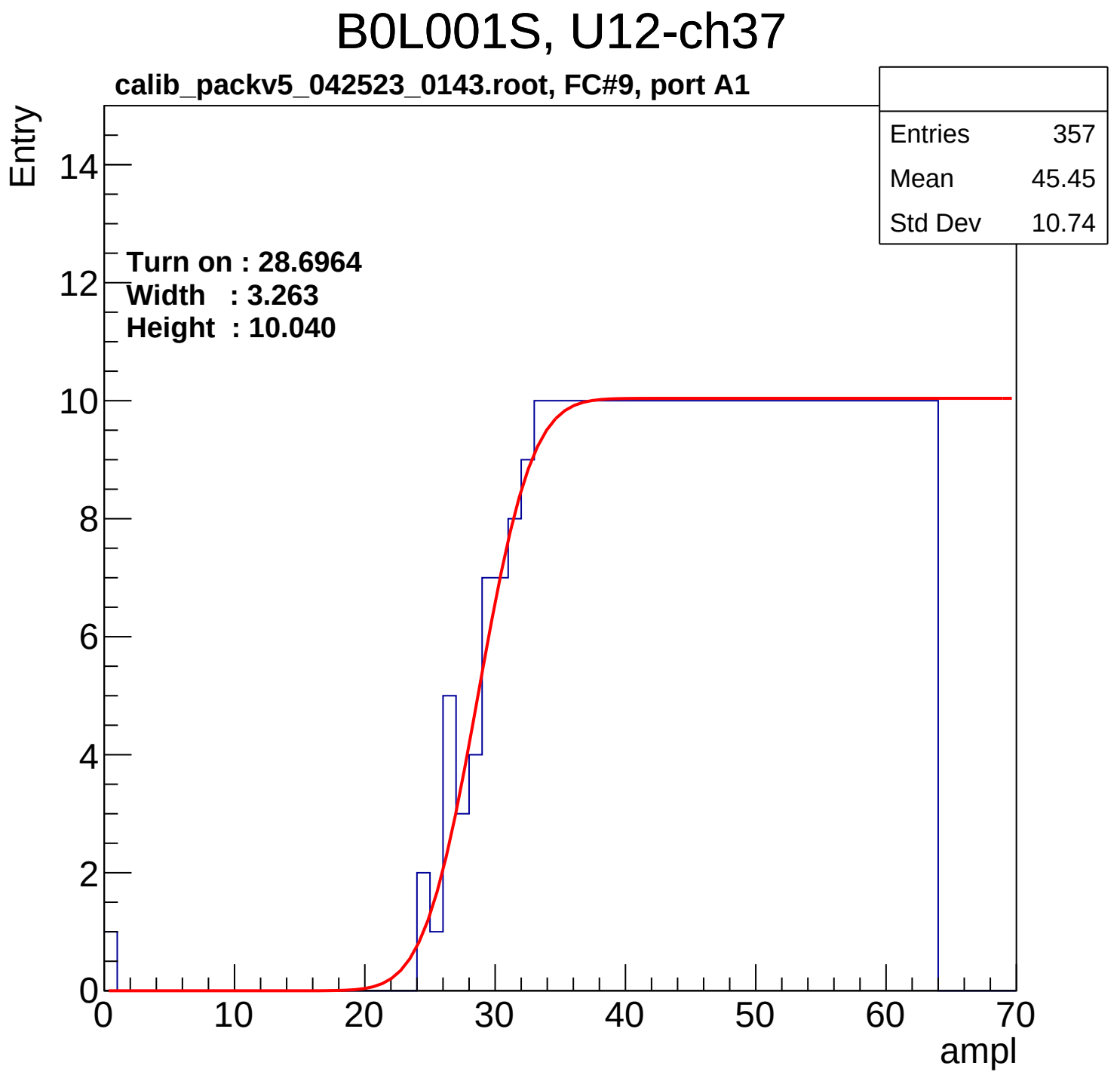
40
50
60
70


B0L001S, U12-ch37
calib_packv5_042523_0143.root, FC#9, port A1
Entries 357
Mean 45.45
Std Dev 10.74
Turn on : 28.6964
Width : 3.263
Height : 10.040
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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40
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60
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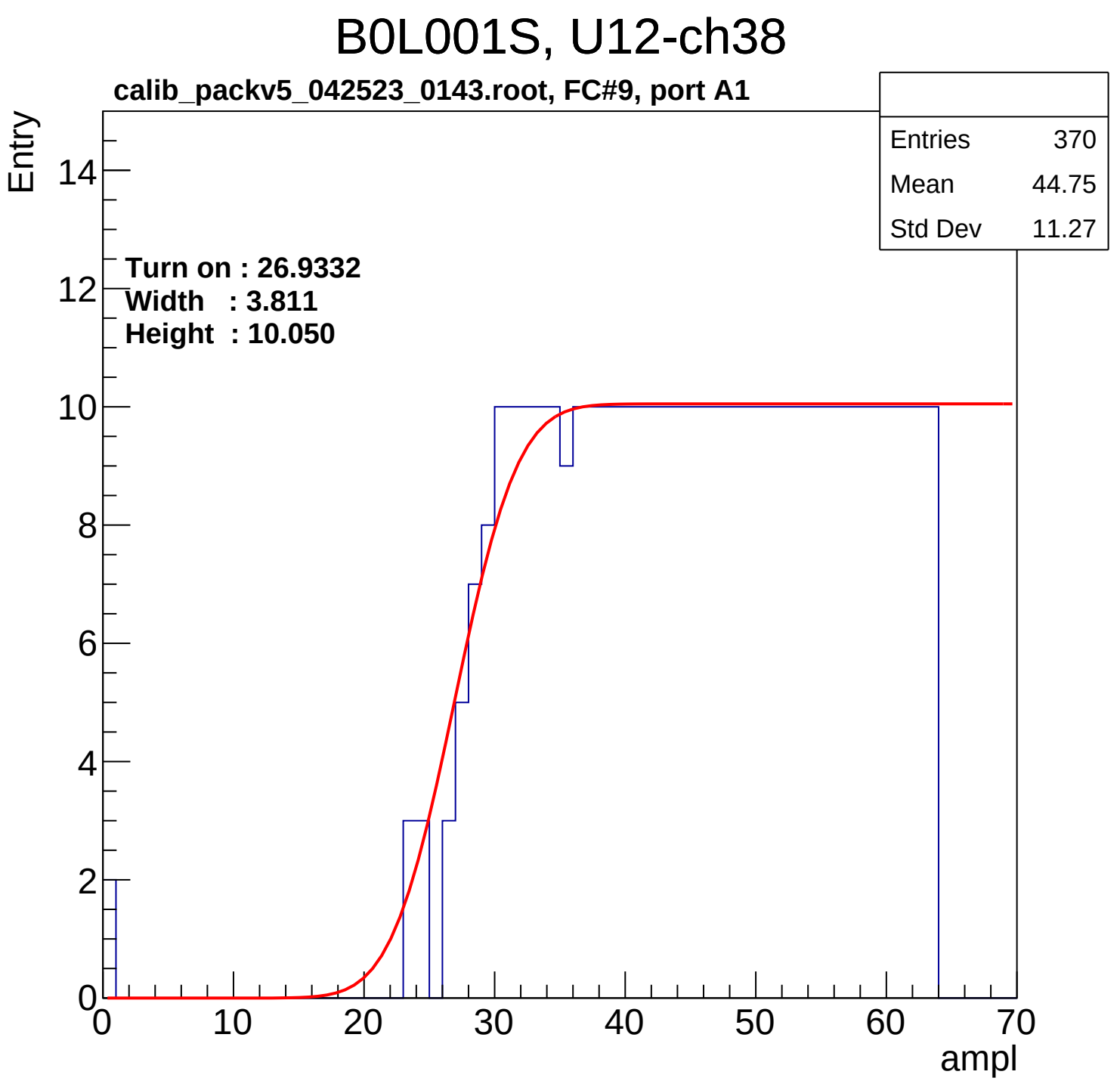
B0L001S, U12-ch38
calib_packv5_042523_0143.root, FC#9, port A1
Entries 370
Mean 44.75
Std Dev 11.27
Turn on : 26.9332
Width : 3.811
Height : 10.050
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
50
60
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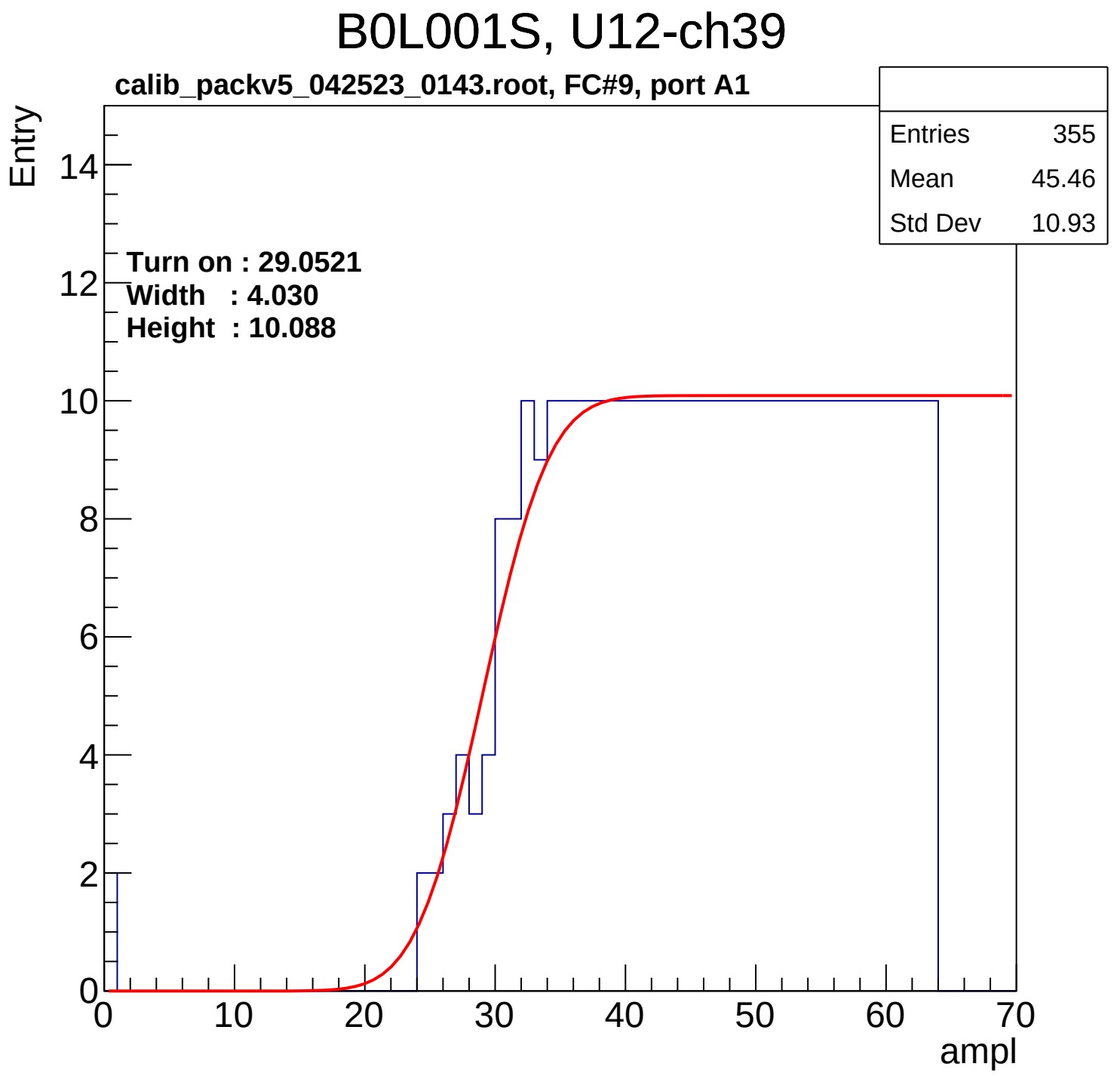
B0L001S, U12-ch39
calib_packv5_042523_0143.root, FC#9, port A1
Entries 355
Mean 45.46
Std Dev 10.93
Turn on : 29.0521
Width : 4.030
Height : 10.088
Entry
ampl
0
2
4
6
8
10
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0
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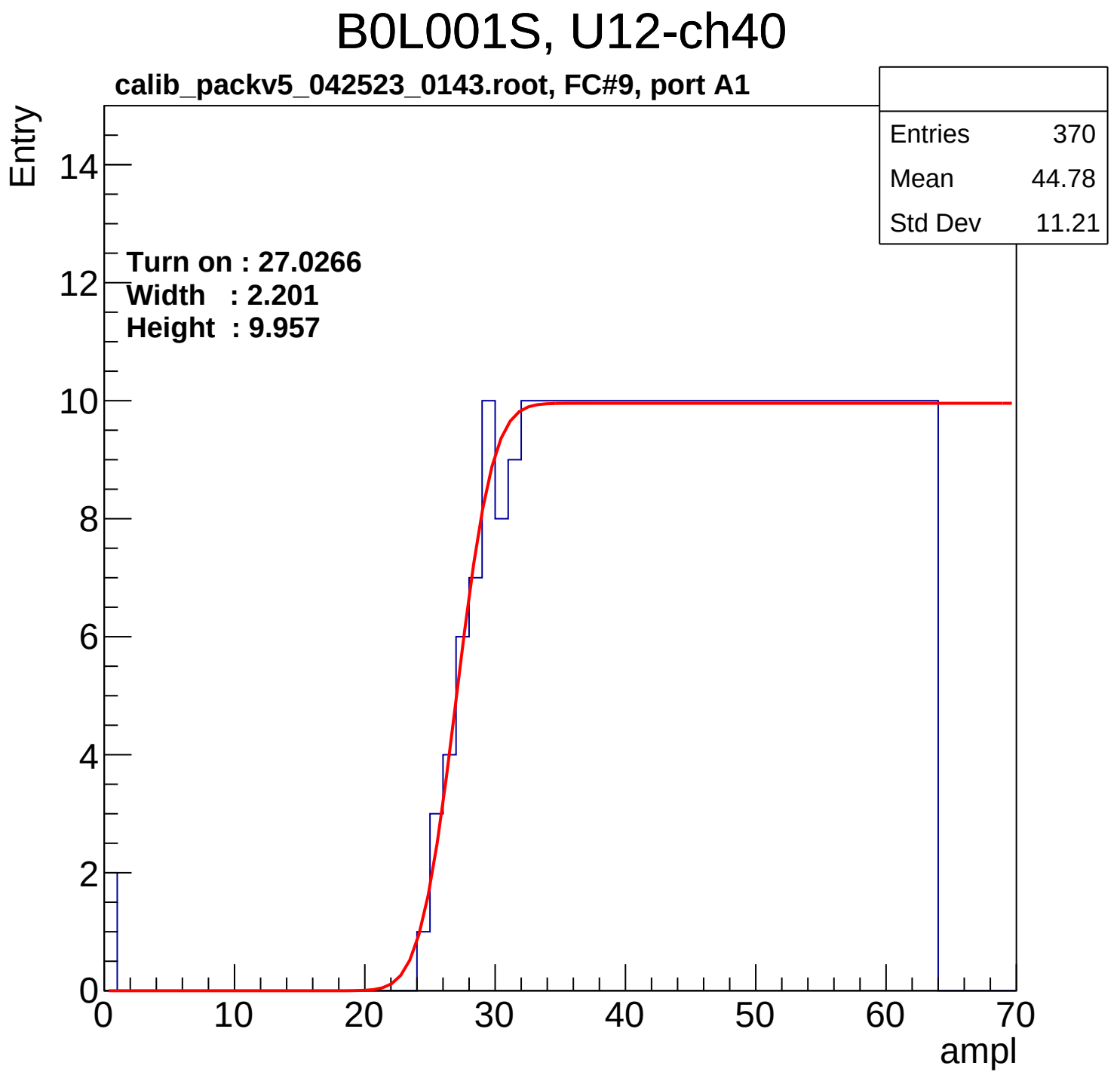
B0L001S, U12-ch40
calib_packv5_042523_0143.root, FC#9, port A1
Entries 370
Mean 44.78
Std Dev 11.21
Turn on : 27.0266
Width : 2.201
Height : 9.957
Entry
ampl
0
2
4
6
8
10
12
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0
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20
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60
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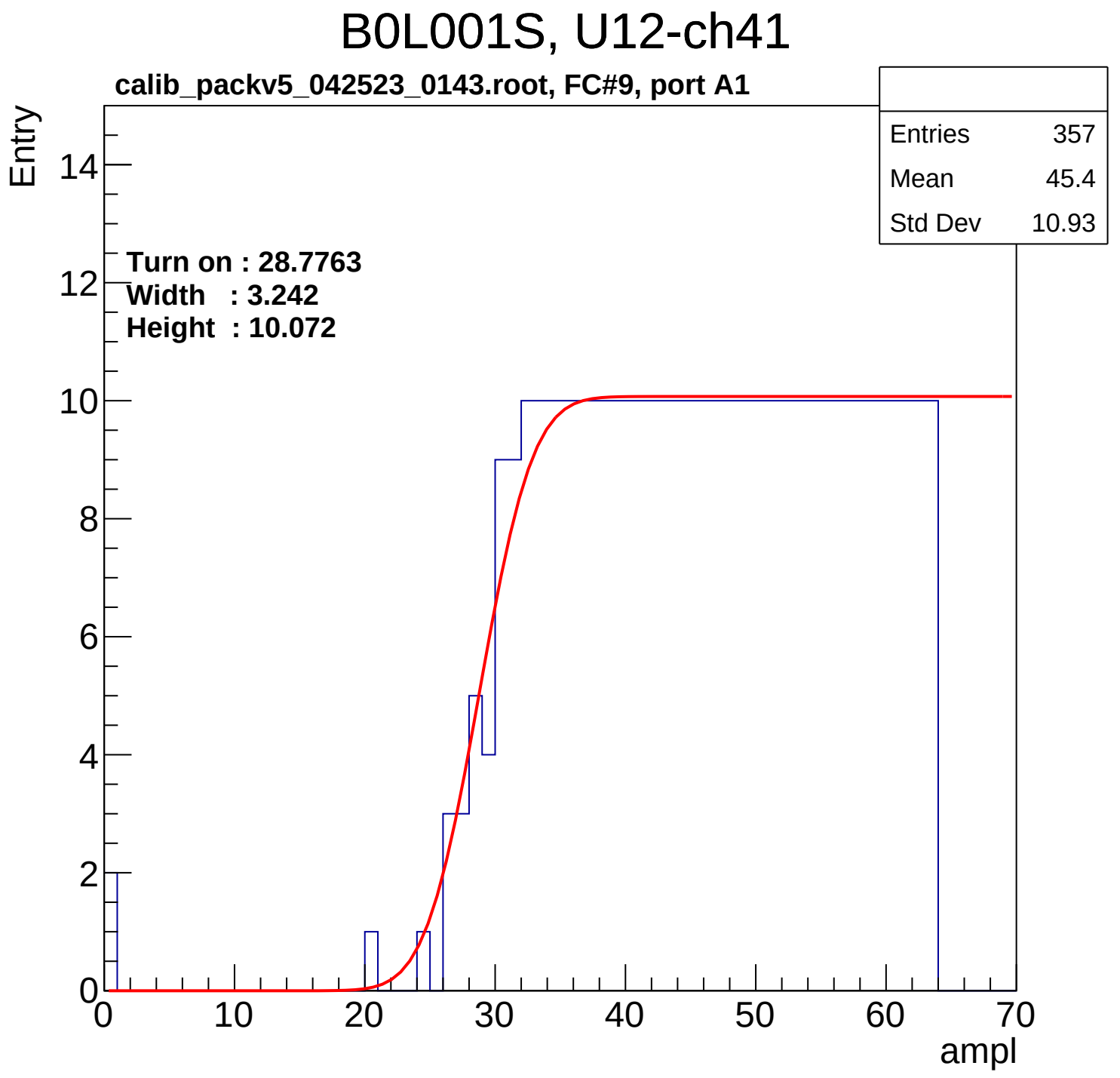
B0L001S, U12-ch41
calib_packv5_042523_0143.root, FC#9, port A1
Entries 357
Mean 45.4
Std Dev 10.93
Turn on : 28.7763
Width : 3.242
Height : 10.072
Entry
ampl
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4
6
8
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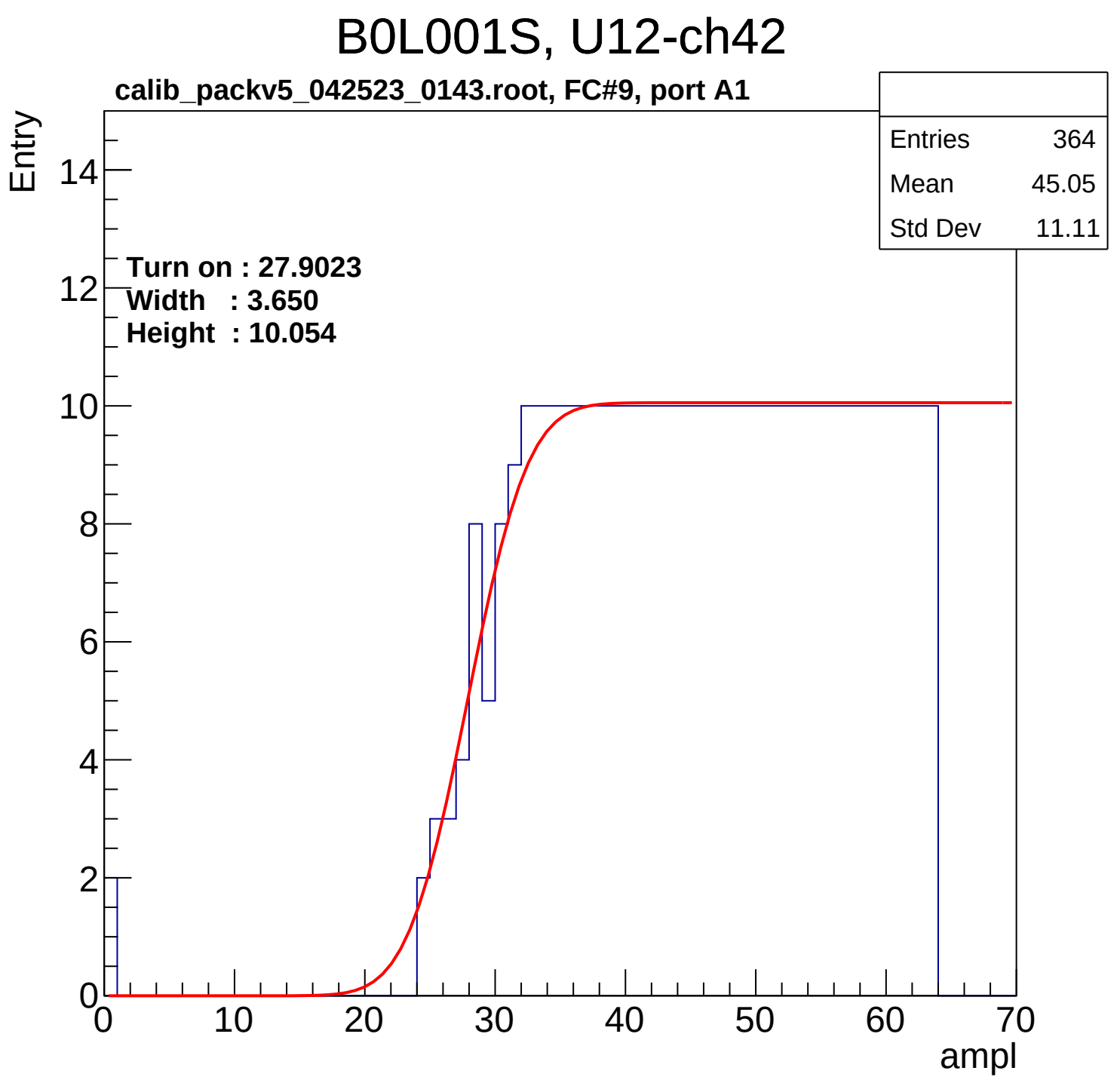
B0L001S, U12-ch42
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 45.05
Std Dev 11.11
Turn on : 27.9023
Width : 3.650
Height : 10.054
Entry
ampl
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4
6
8
10
12
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0
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20
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60
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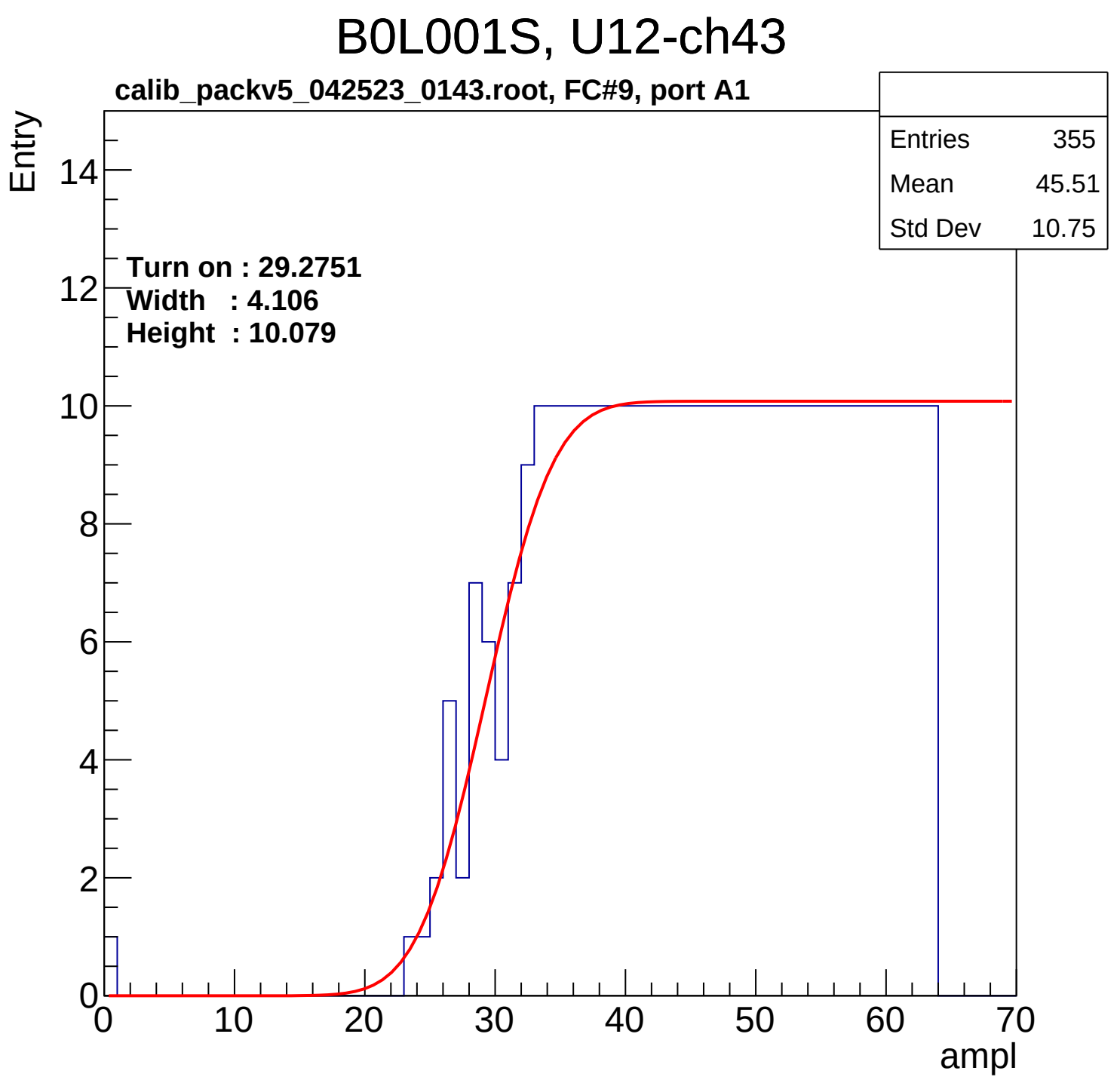
B0L001S, U12-ch43
calib_packv5_042523_0143.root, FC#9, port A1
Entries 355
Mean 45.51
Std Dev 10.75
Turn on : 29.2751
Width : 4.106
Height : 10.079
Entry
ampl
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6
8
10
12
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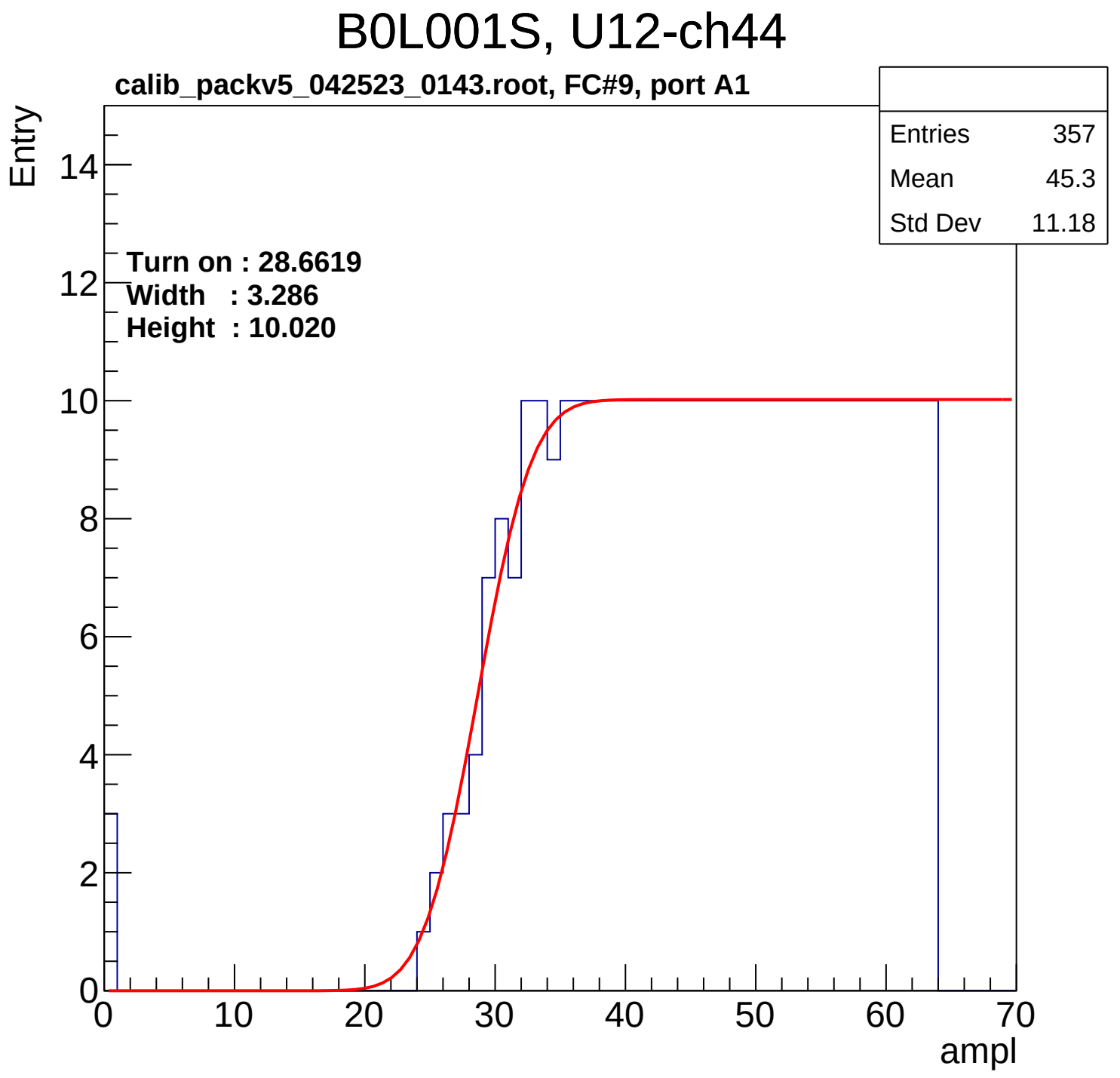
B0L001S, U12-ch44
calib_packv5_042523_0143.root, FC#9, port A1
Entries 357
Mean 45.3
Std Dev 11.18
Turn on : 28.6619
Width : 3.286
Height : 10.020
Entry
ampl
0
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6
8
10
12
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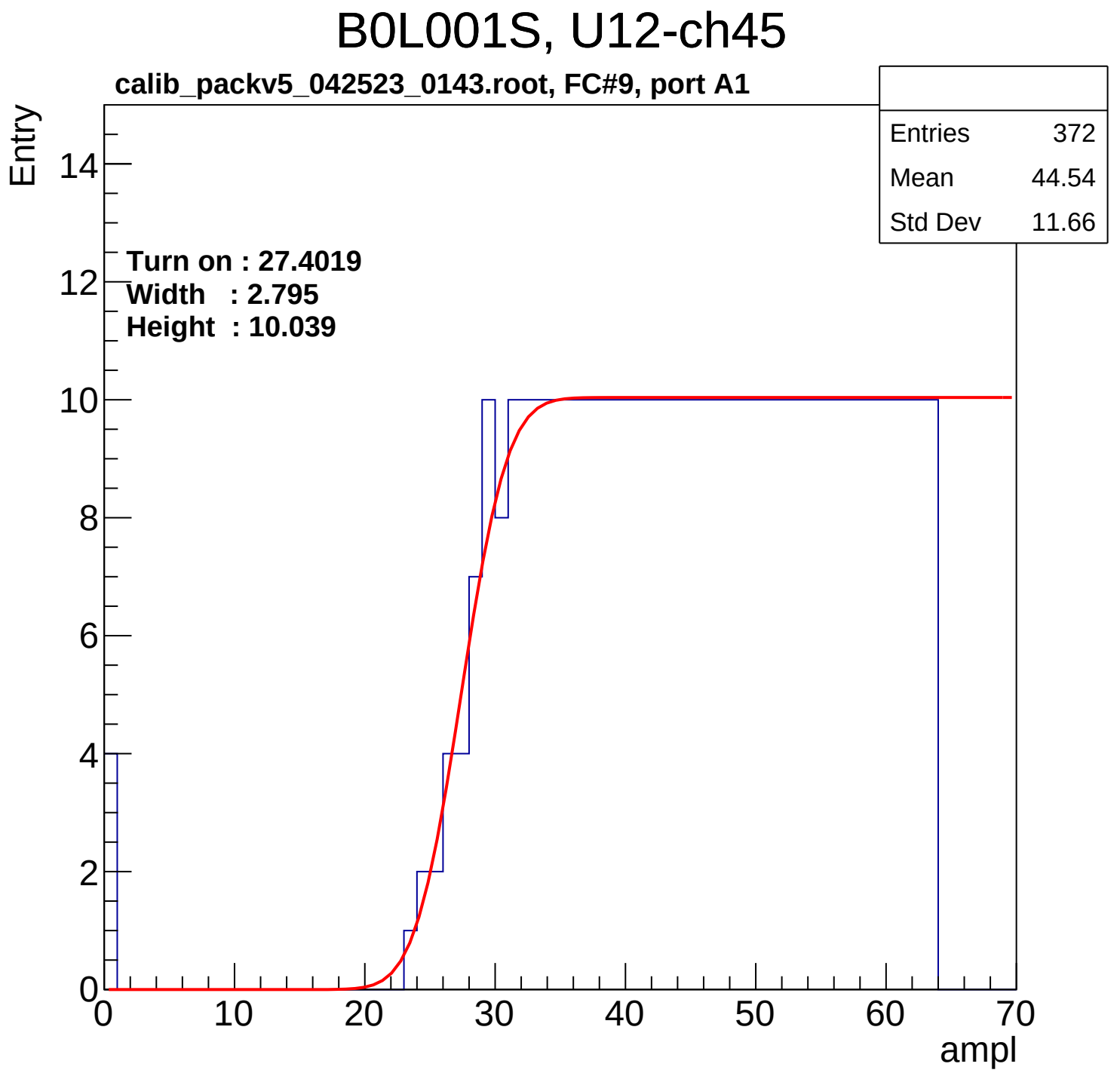
B0L001S, U12-ch45
calib_packv5_042523_0143.root, FC#9, port A1
Entries 372
Mean 44.54
Std Dev 11.66
Turn on : 27.4019
Width : 2.795
Height : 10.039
Entry
ampl
0
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6
8
10
12
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0
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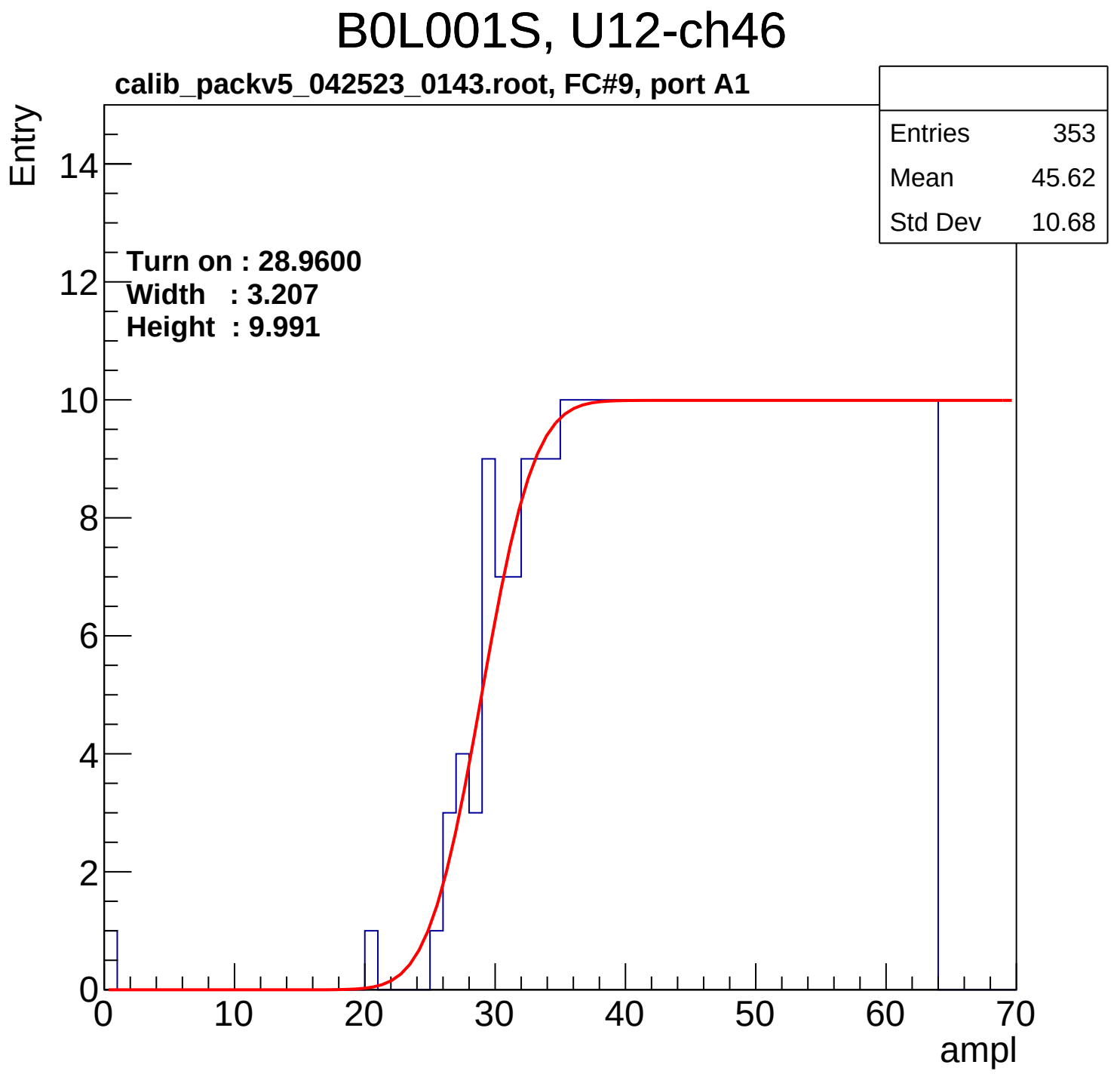
B0L001S, U12-ch46
calib_packv5_042523_0143.root, FC#9, port A1
Entries 353
Mean 45.62
Std Dev 10.68
Turn on : 28.9600
Width : 3.207
Height : 9.991
Entry
ampl
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2
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6
8
10
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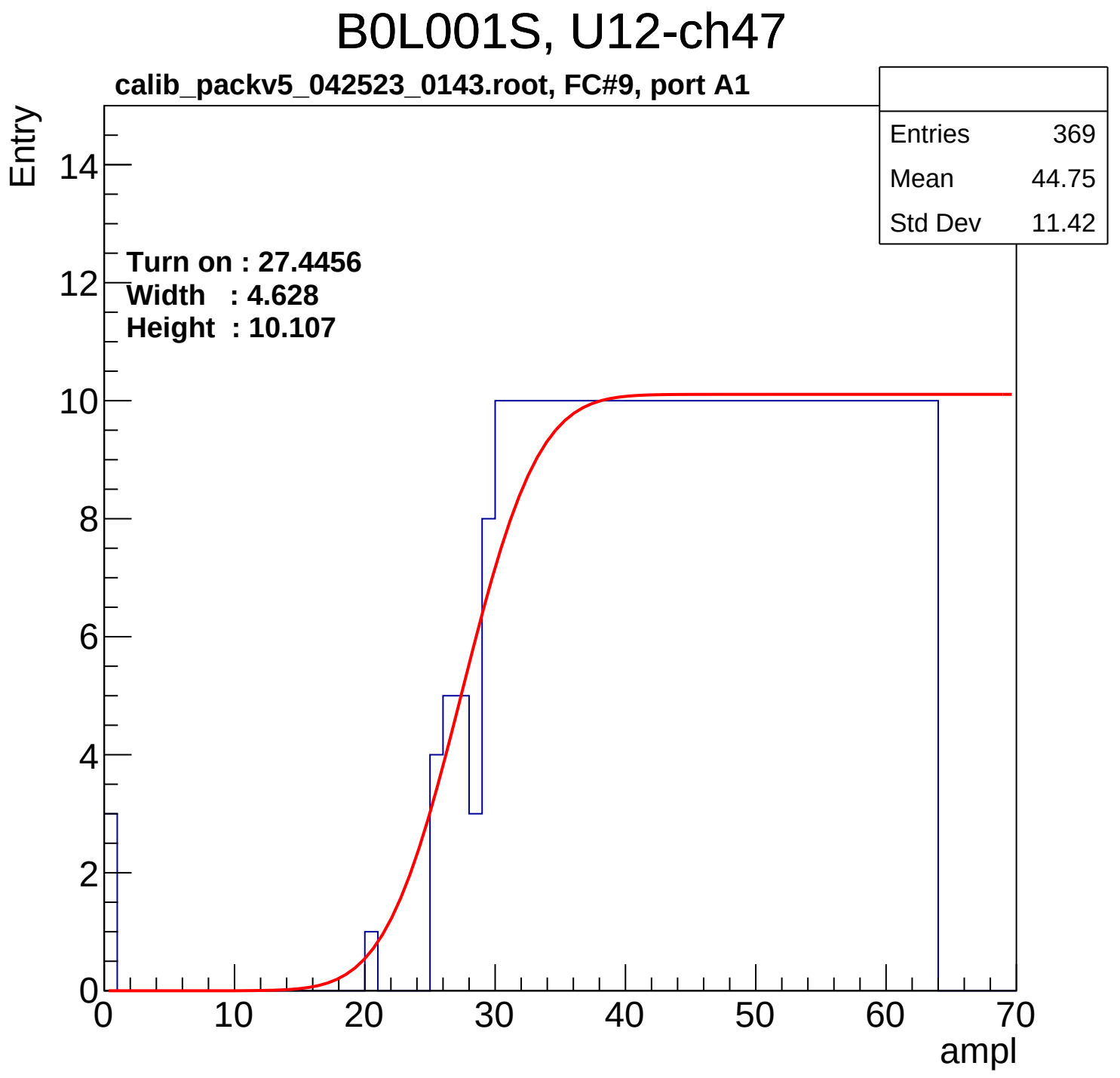
B0L001S, U12-ch47
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.75
Std Dev 11.42
Turn on : 27.4456
Width : 4.628
Height : 10.107
Entry
ampl
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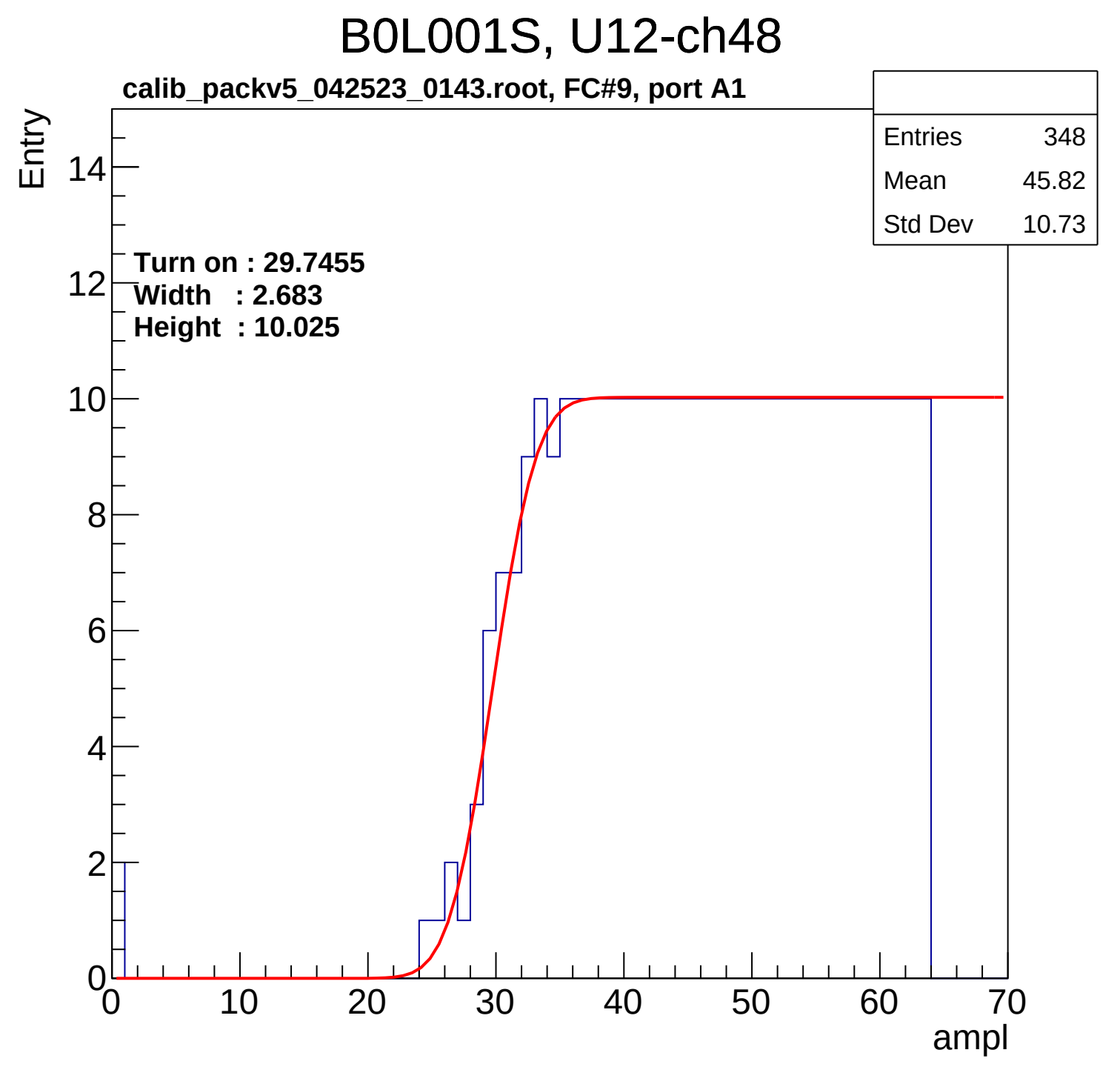
B0L001S, U12-ch48
calib_packv5_042523_0143.root, FC#9, port A1
Entries 348
Mean 45.82
Std Dev 10.73
Turn on : 29.7455
Width : 2.683
Height : 10.025
Entry
ampl
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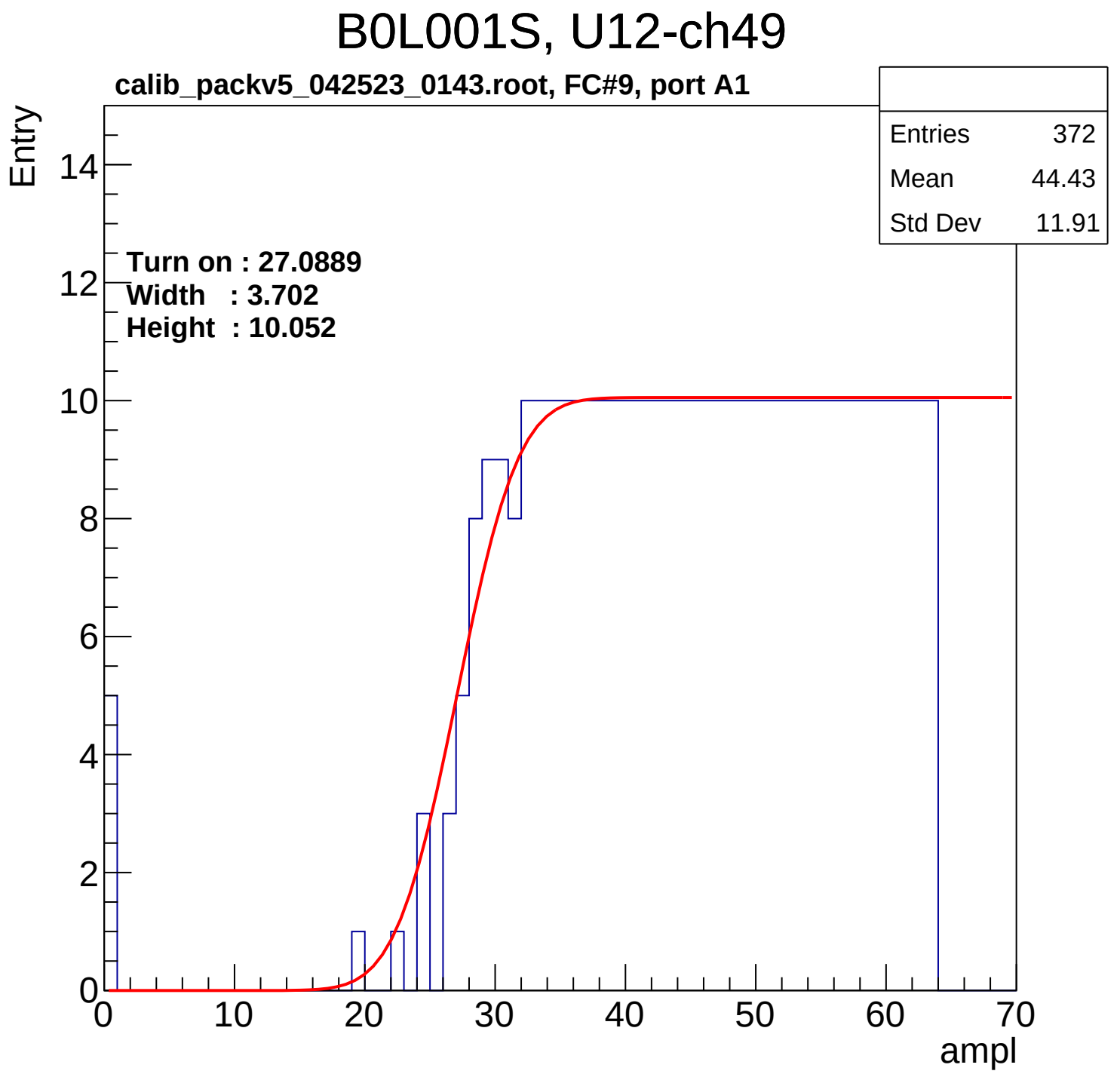
B0L001S, U12-ch49
calib_packv5_042523_0143.root, FC#9, port A1
Entries 372
Mean 44.43
Std Dev 11.91
Turn on : 27.0889
Width : 3.702
Height : 10.052
Entry
ampl
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2
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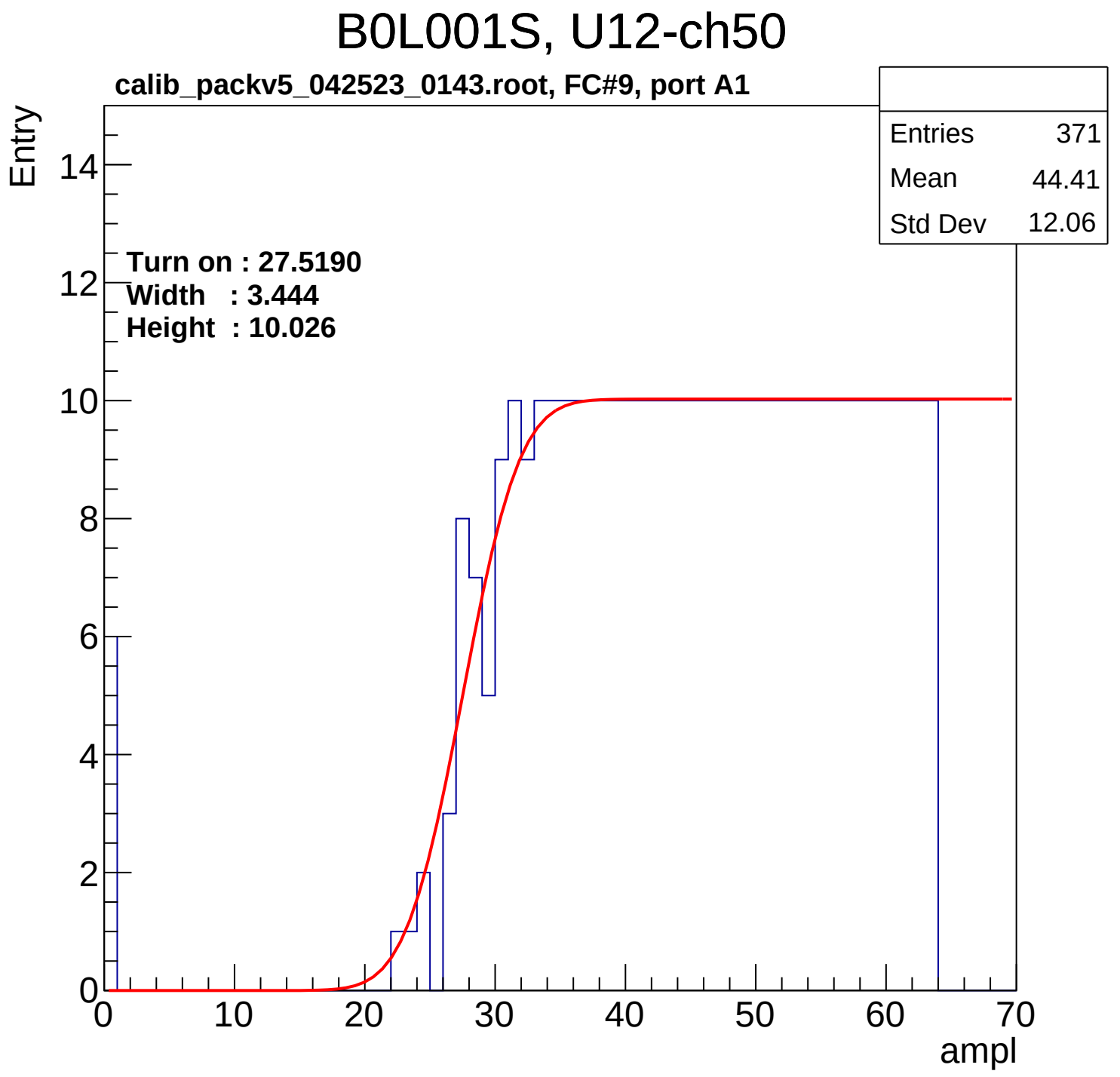
B0L001S, U12-ch50
calib_packv5_042523_0143.root, FC#9, port A1
Entries 371
Mean 44.41
Std Dev 12.06
Turn on : 27.5190
Width : 3.444
Height : 10.026
Entry
ampl
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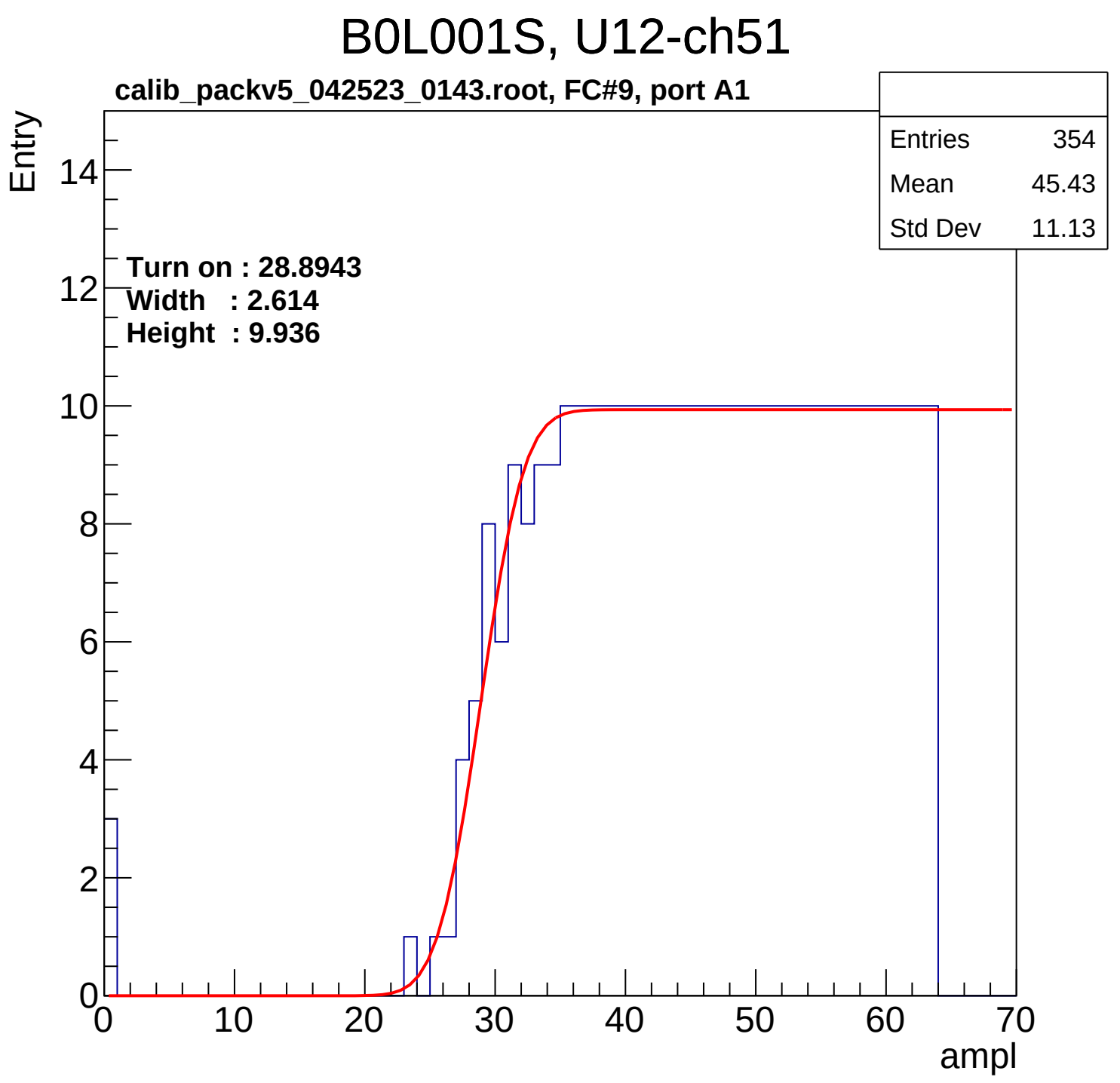
B0L001S, U12-ch51
calib_packv5_042523_0143.root, FC#9, port A1
Entries 354
Mean 45.43
Std Dev 11.13
Turn on : 28.8943
Width : 2.614
Height : 9.936
Entry
ampl
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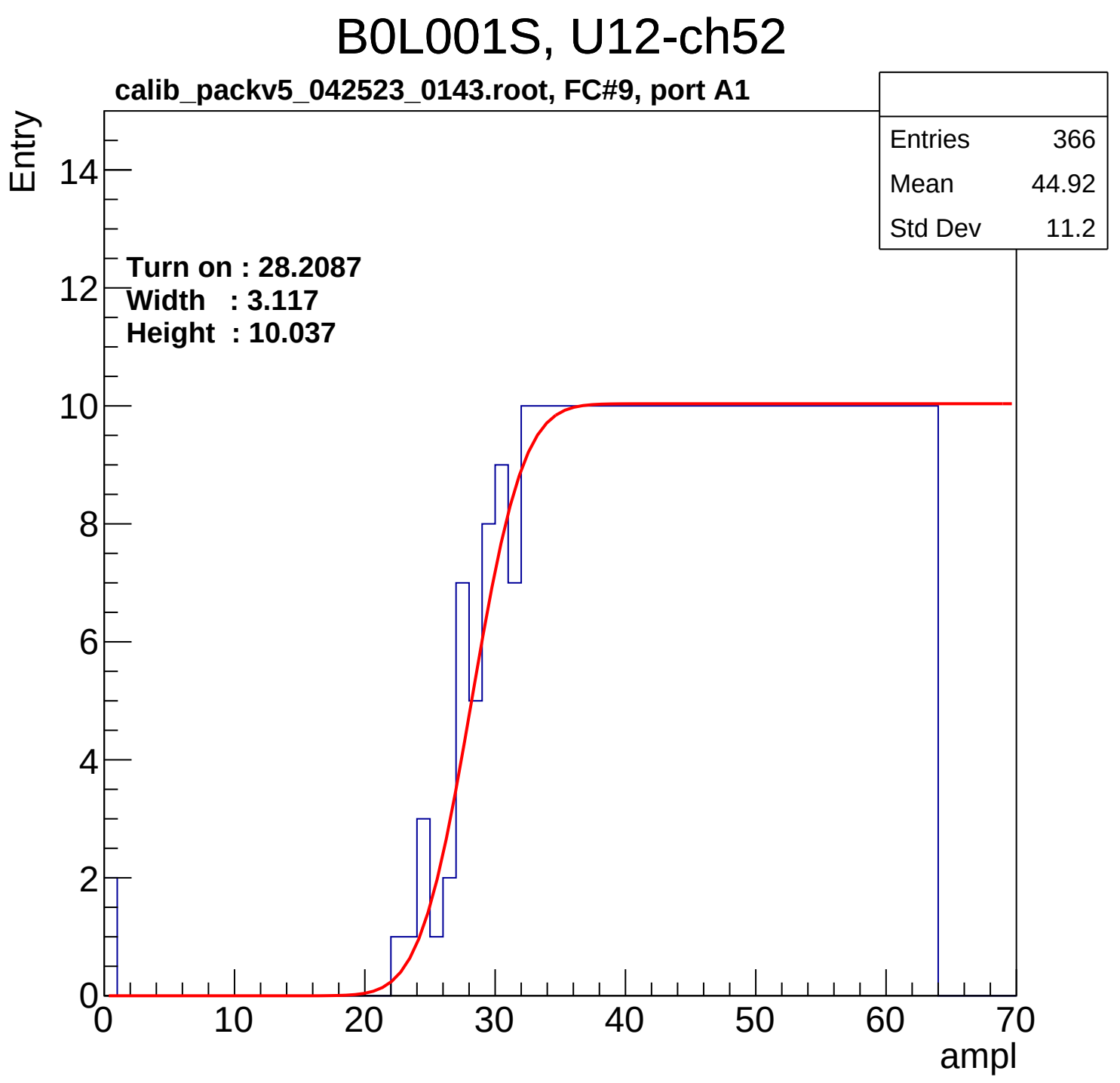
B0L001S, U12-ch52
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.92
Std Dev 11.2
Turn on : 28.2087
Width : 3.117
Height : 10.037
Entry
ampl
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6
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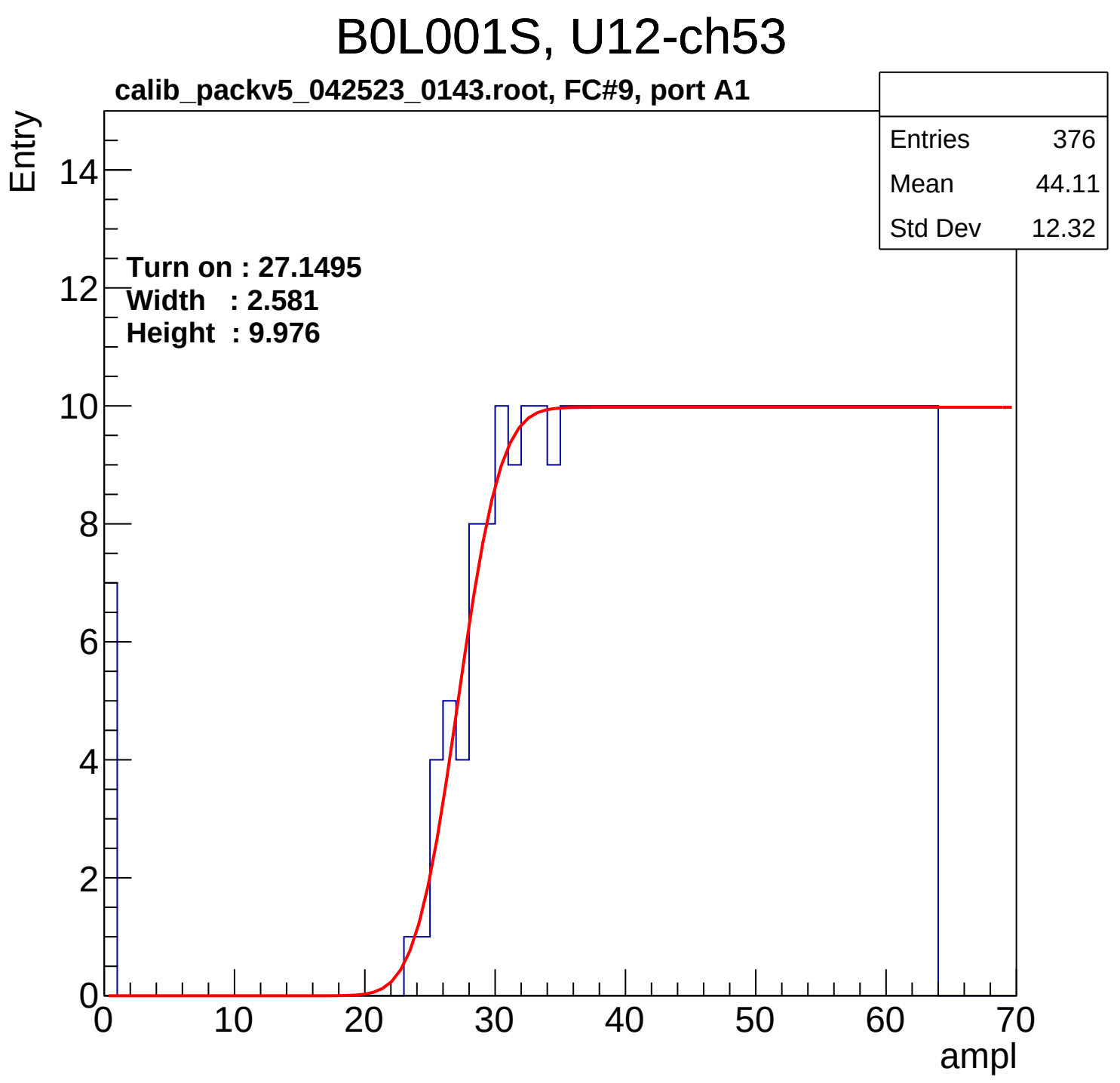
B0L001S, U12-ch53
calib_packv5_042523_0143.root, FC#9, port A1
Entries 376
Mean 44.11
Std Dev 12.32
Turn on : 27.1495
Width : 2.581
Height : 9.976
Entry
ampl
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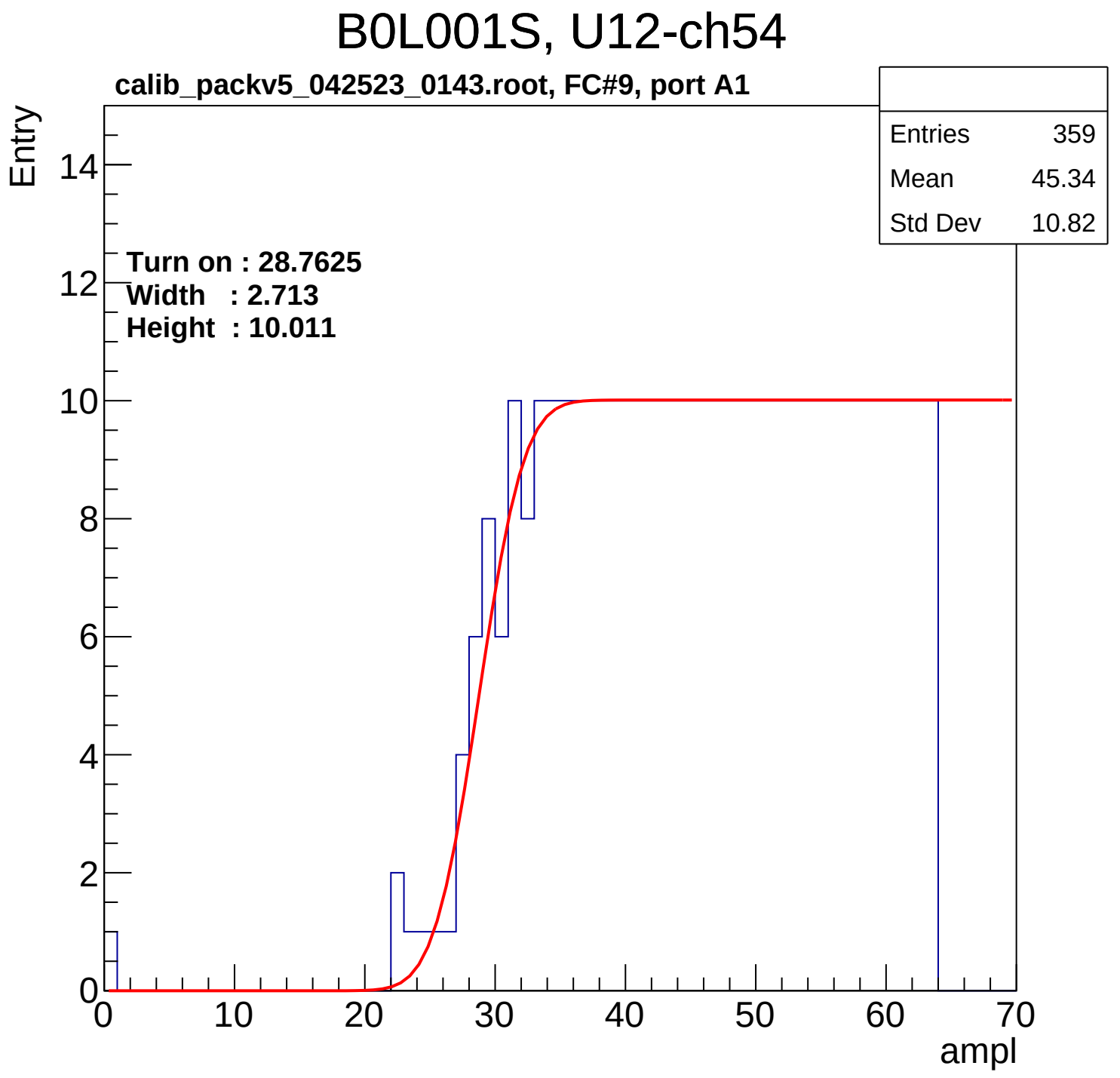
B0L001S, U12-ch54
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 45.34
Std Dev 10.82
Turn on : 28.7625
Width : 2.713
Height : 10.011
Entry
ampl
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2
4
6
8
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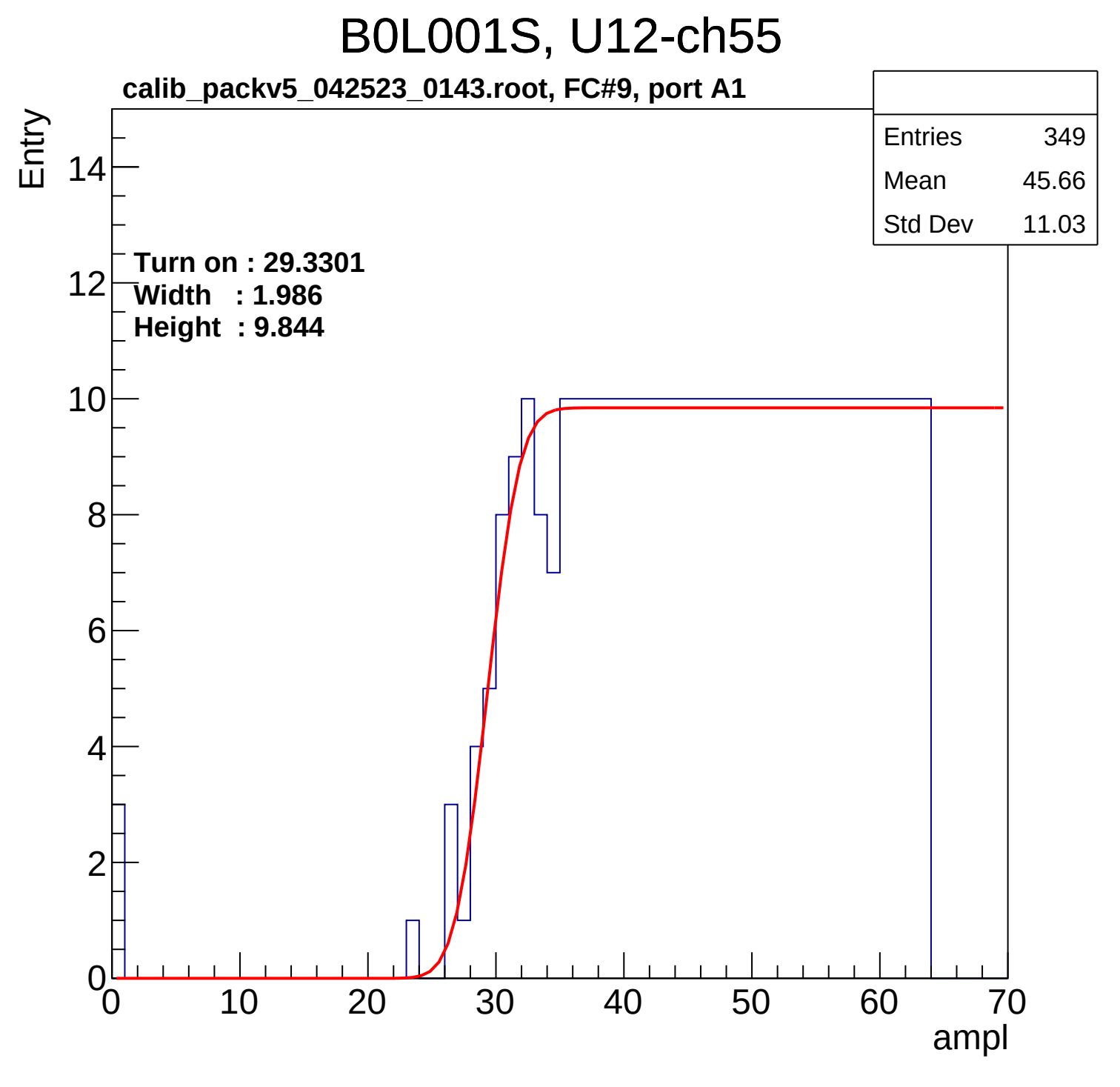
B0L001S, U12-ch55
calib_packv5_042523_0143.root, FC#9, port A1
Entries 349
Mean 45.66
Std Dev 11.03
Turn on : 29.3301
Width : 1.986
Height : 9.844
Entry
ampl
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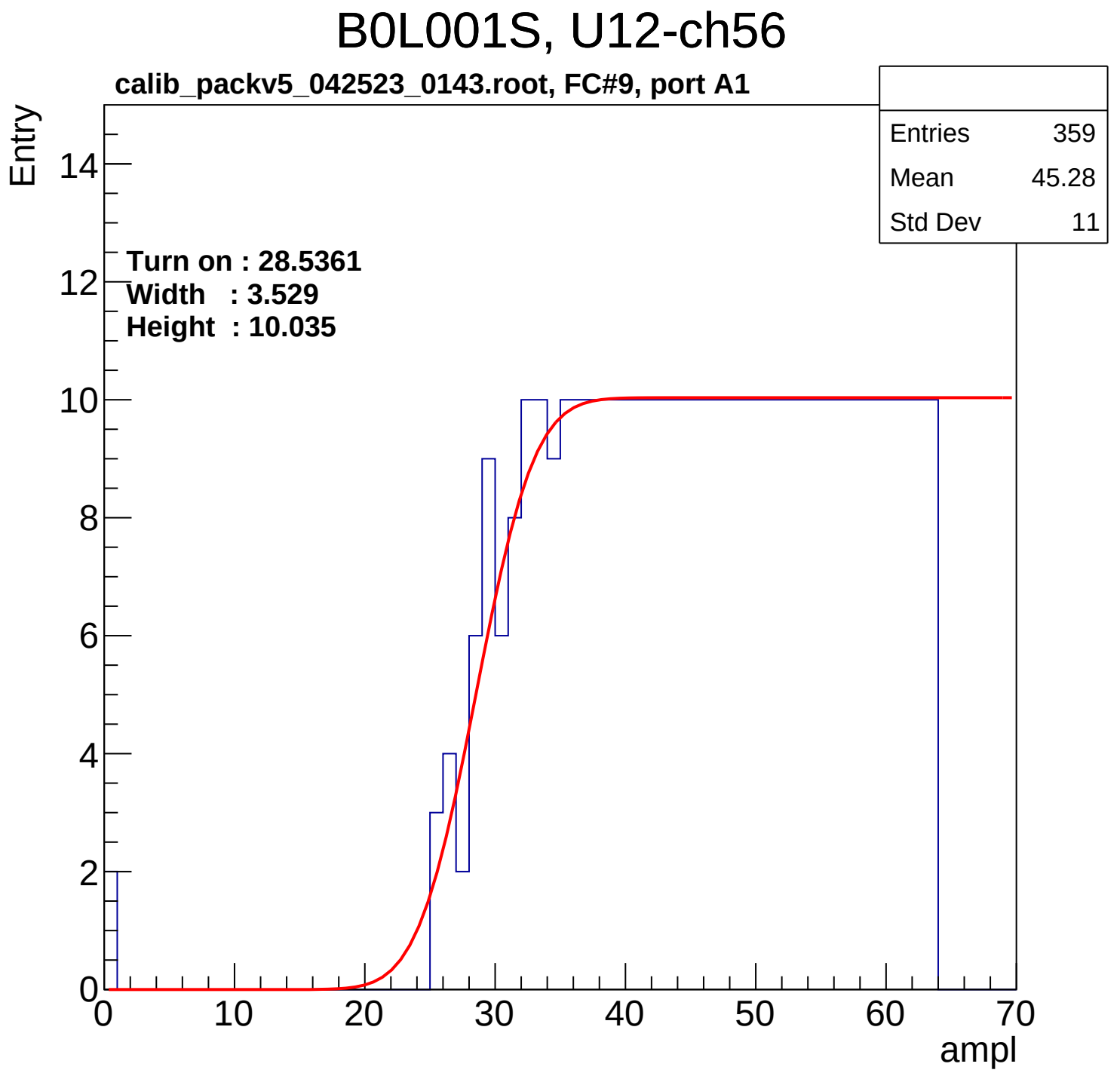
B0L001S, U12-ch56
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 45.28
Std Dev 11
Turn on : 28.5361
Width : 3.529
Height : 10.035
Entry
ampl
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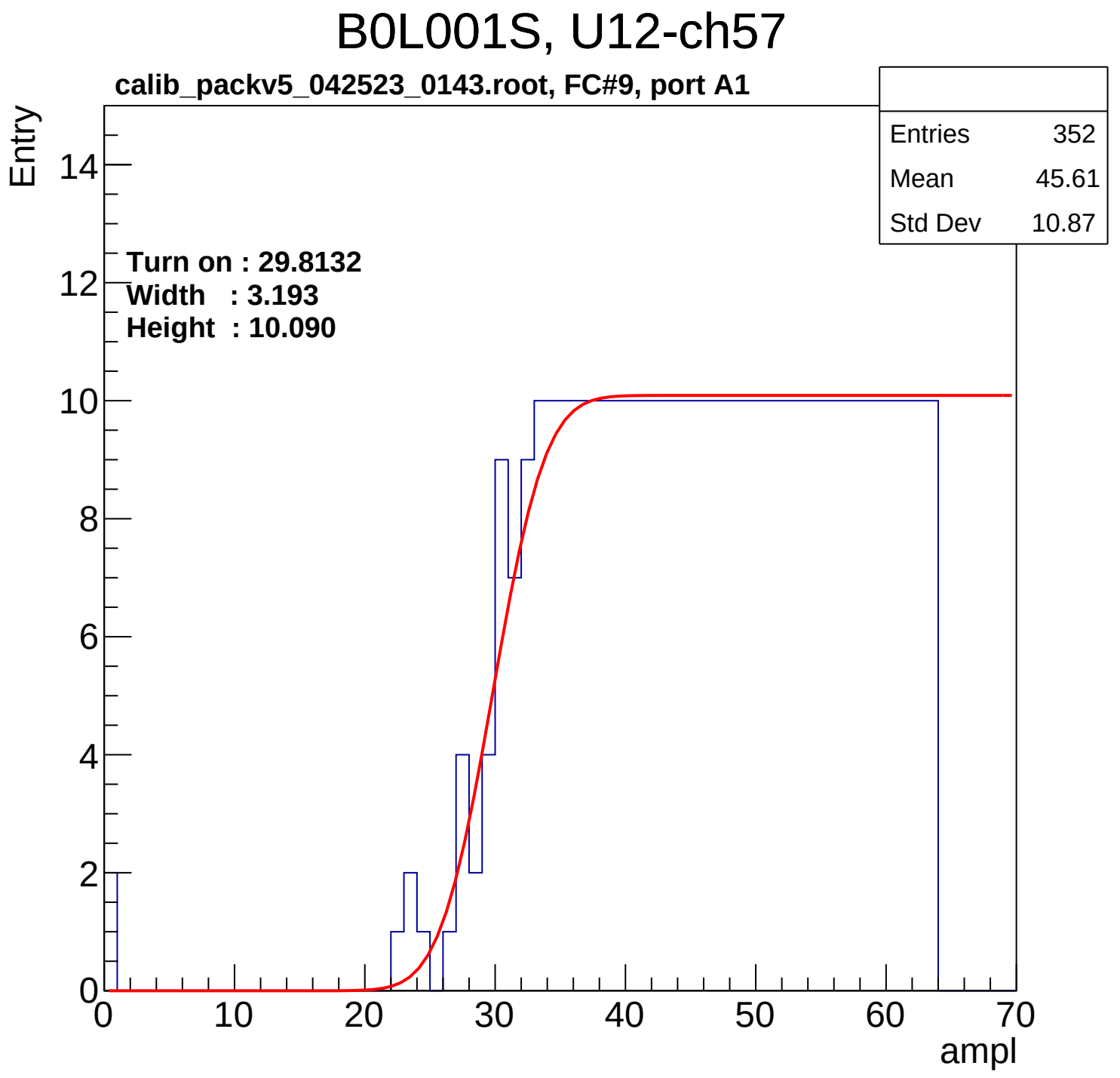
B0L001S, U12-ch57
calib_packv5_042523_0143.root, FC#9, port A1
Entries 352
Mean 45.61
Std Dev 10.87
Turn on : 29.8132
Width : 3.193
Height : 10.090
Entry
ampl
0
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4
6
8
10
12
14
0
10
20
30
40
50
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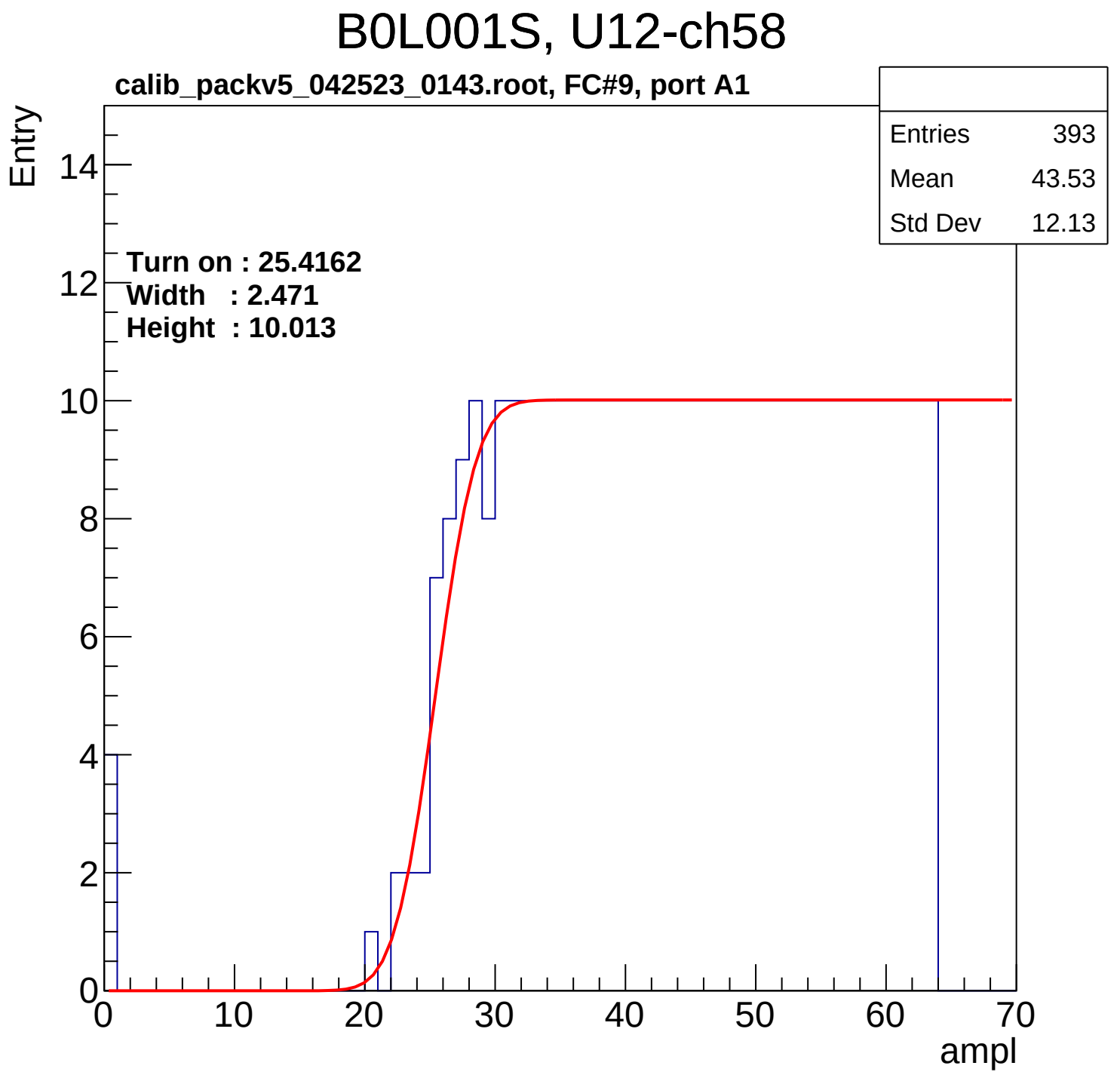
B0L001S, U12-ch58
calib_packv5_042523_0143.root, FC#9, port A1
Entries 393
Mean 43.53
Std Dev 12.13
Turn on : 25.4162
Width : 2.471
Height : 10.013
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ampl
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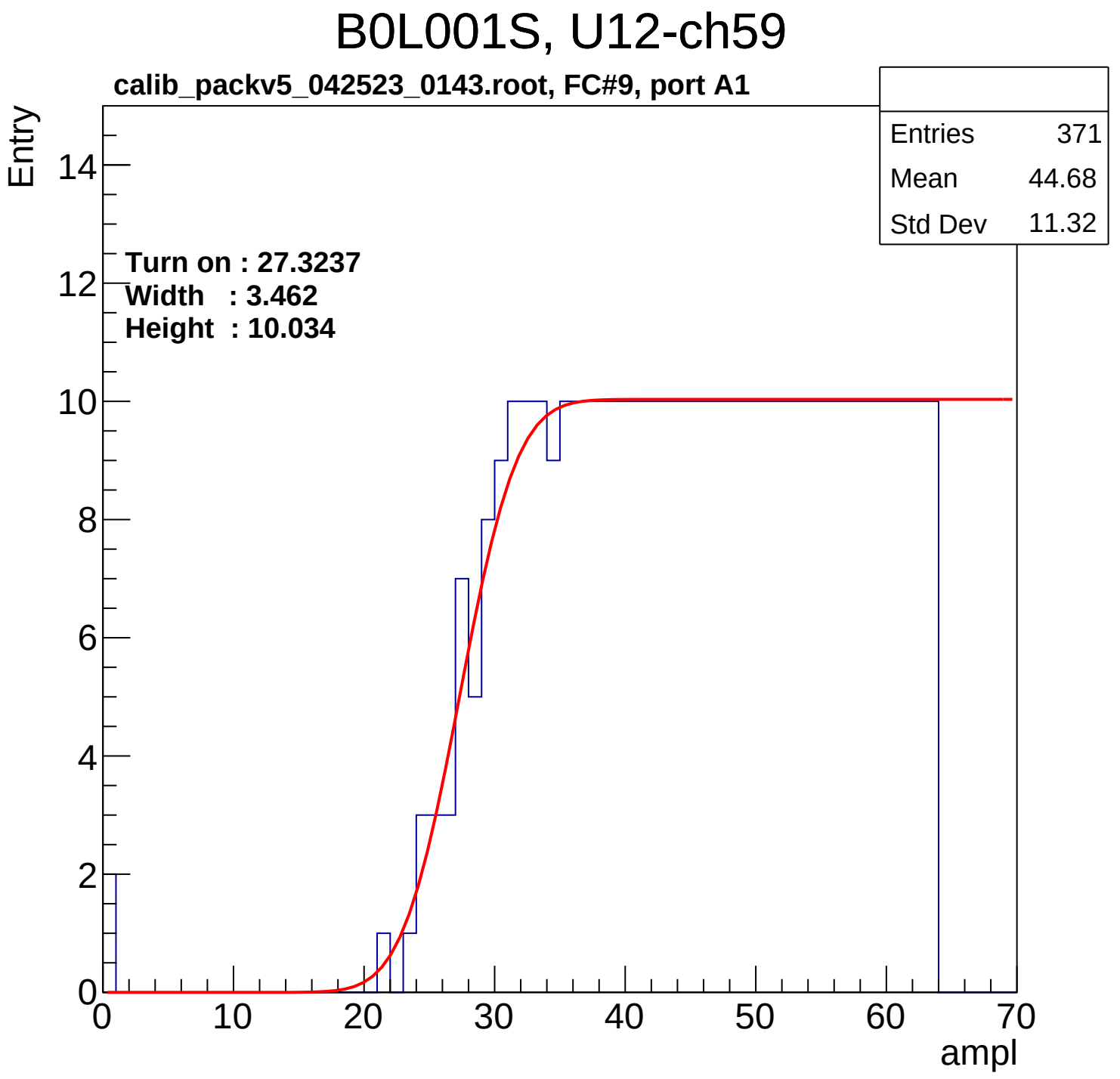
B0L001S, U12-ch59
calib_packv5_042523_0143.root, FC#9, port A1
Entries 371
Mean 44.68
Std Dev 11.32
Turn on : 27.3237
Width : 3.462
Height : 10.034
Entry
ampl
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2
4
6
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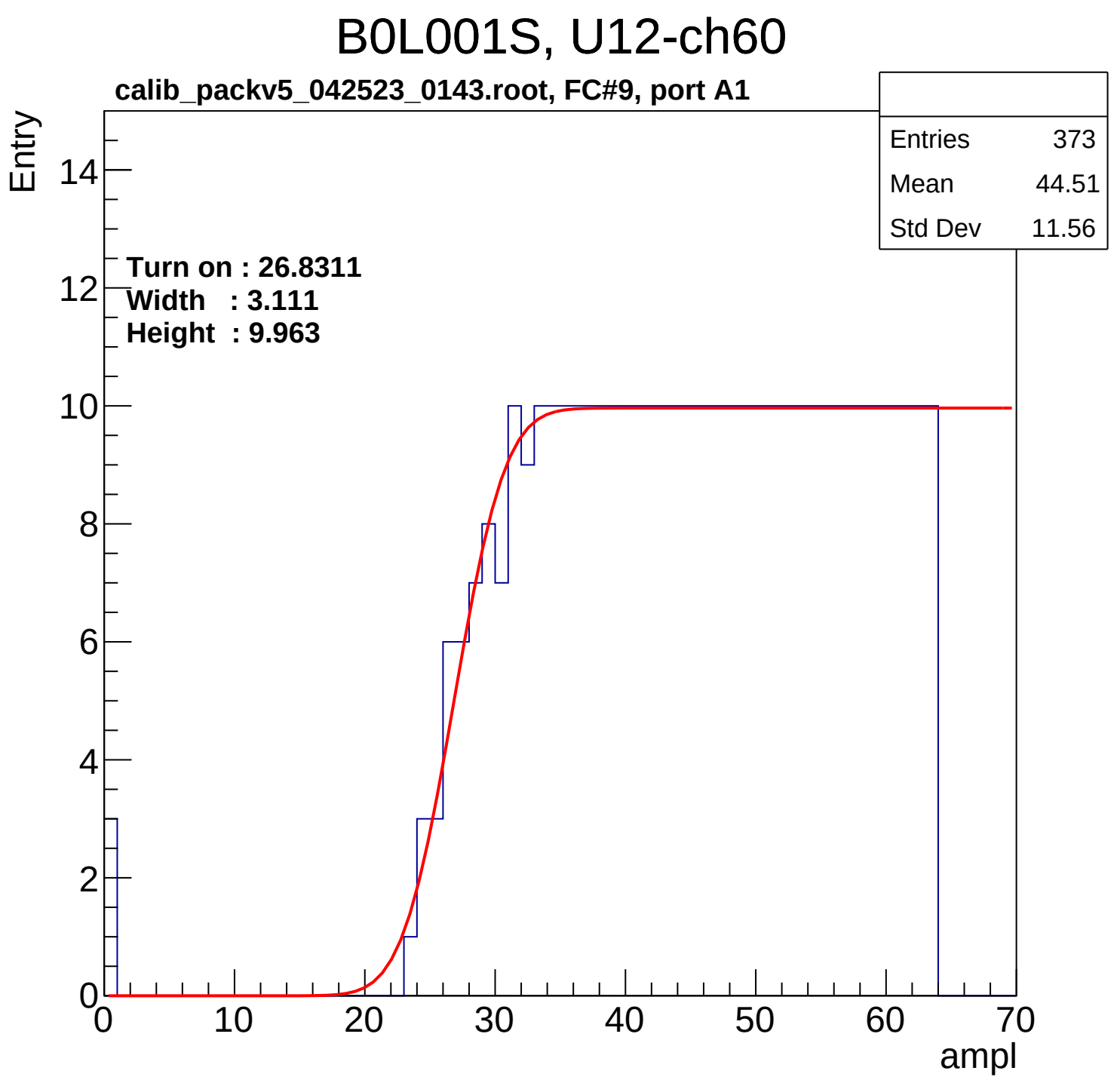
B0L001S, U12-ch60
calib_packv5_042523_0143.root, FC#9, port A1
Entries 373
Mean 44.51
Std Dev 11.56
Turn on : 26.8311
Width : 3.111
Height : 9.963
Entry
ampl
0
2
4
6
8
10
12
14
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60
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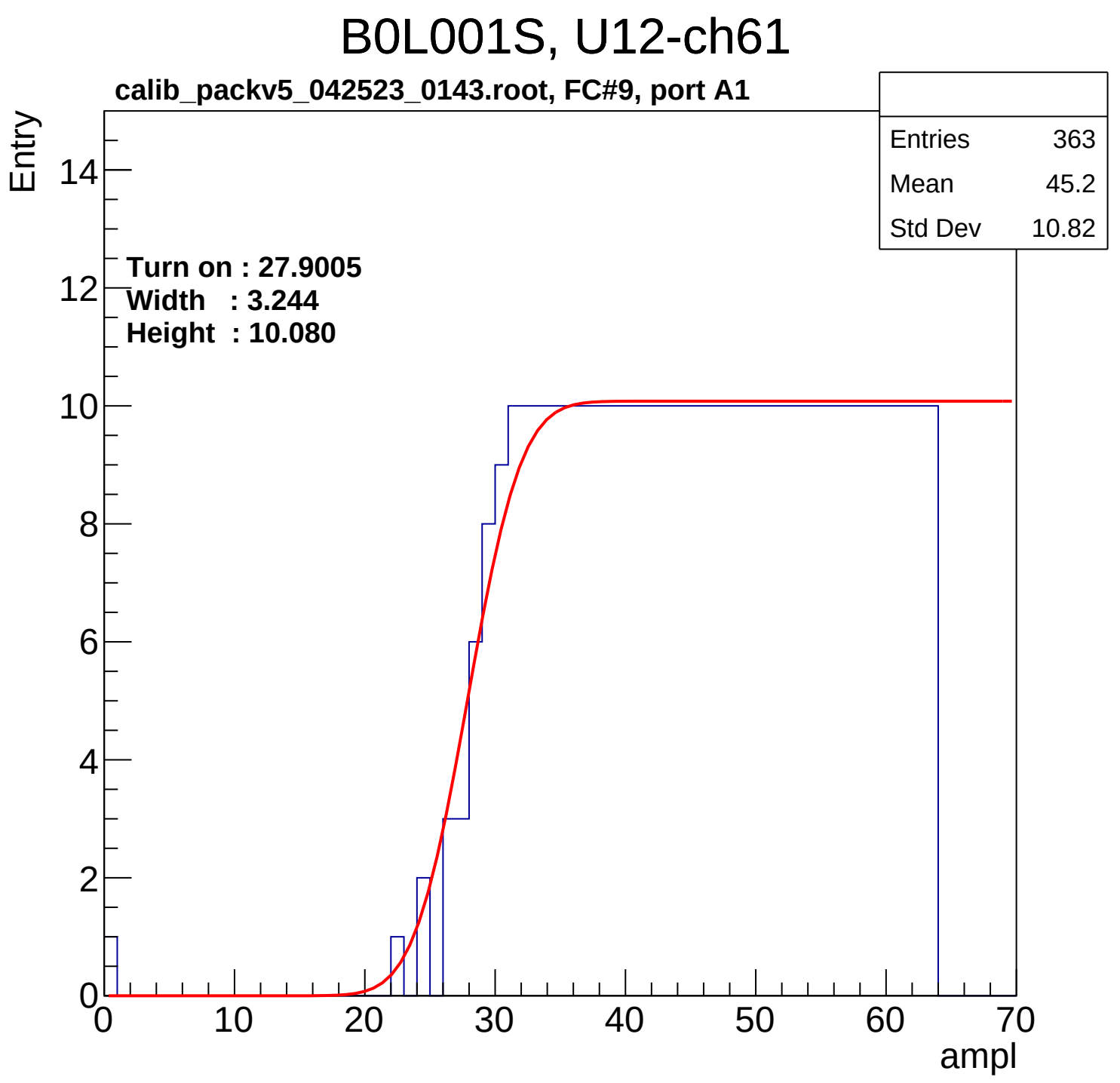
B0L001S, U12-ch61
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 45.2
Std Dev 10.82
Turn on : 27.9005
Width : 3.244
Height : 10.080
Entry
ampl
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2
4
6
8
10
12
14
0
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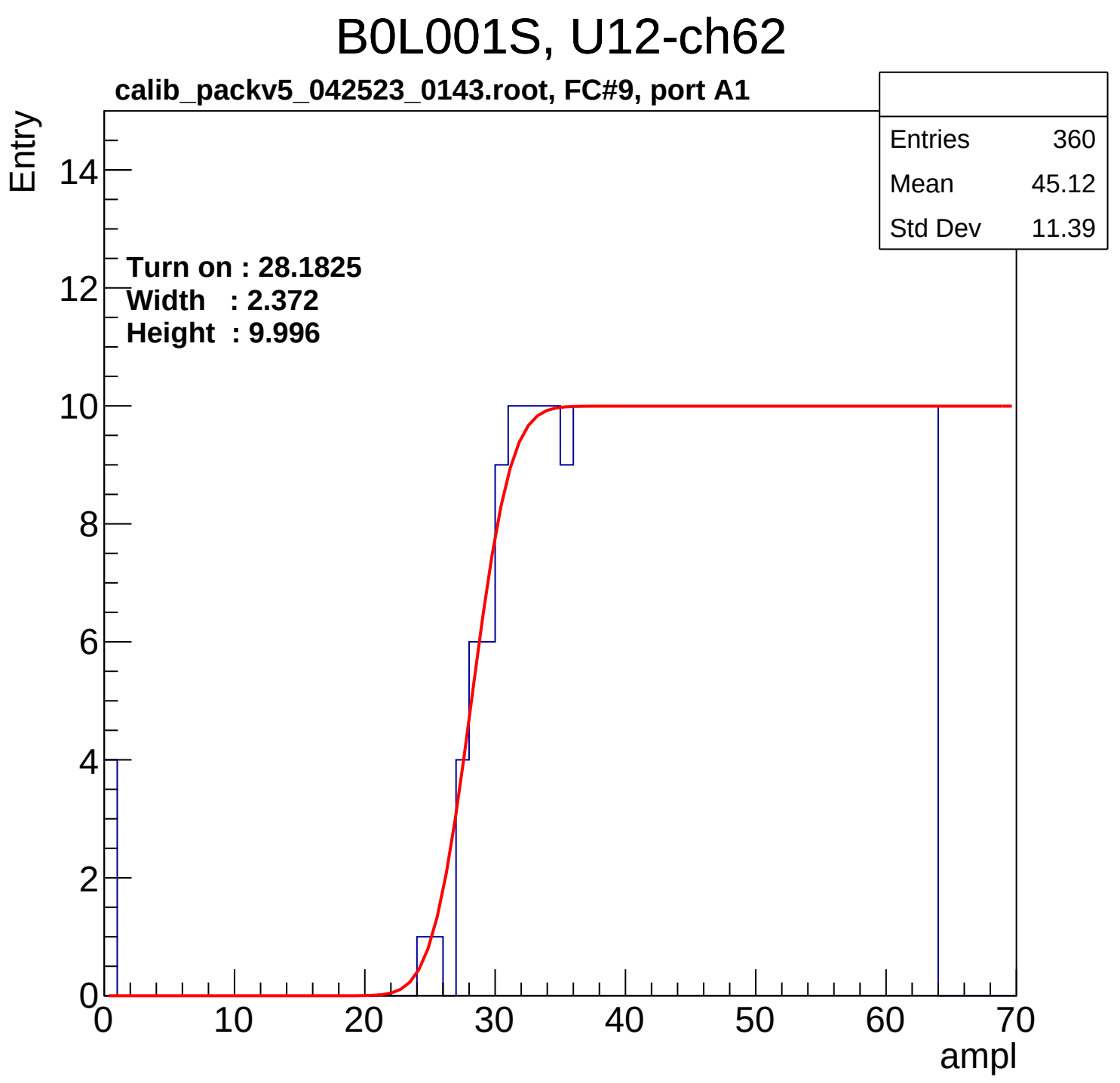
B0L001S, U12-ch62
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 45.12
Std Dev 11.39
Turn on : 28.1825
Width : 2.372
Height : 9.996
Entry
ampl
0
2
4
6
8
10
12
14
0
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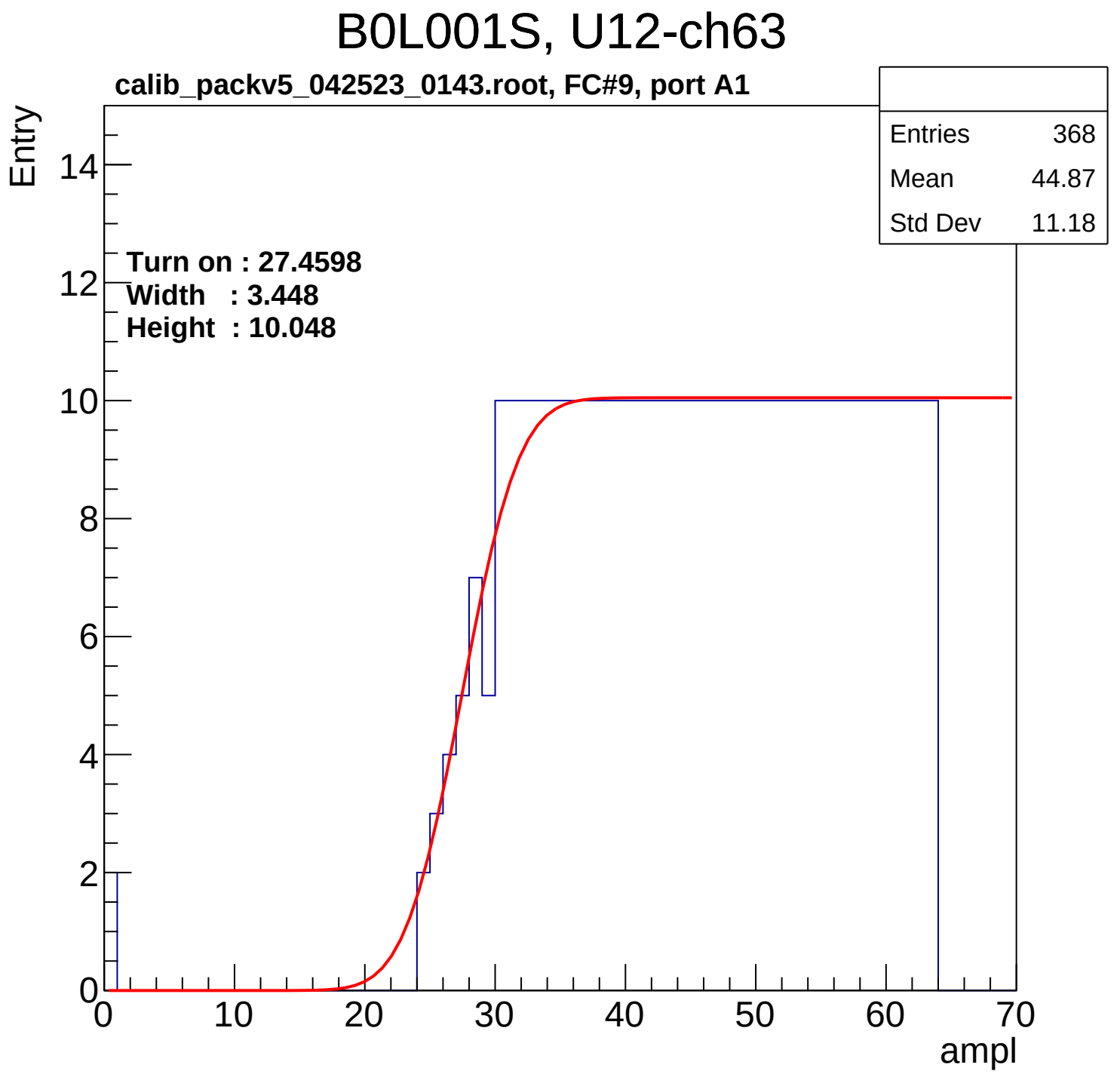
B0L001S, U12-ch63
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.87
Std Dev 11.18
Turn on : 27.4598
Width : 3.448
Height : 10.048
Entry
ampl
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2
4
6
8
10
12
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0
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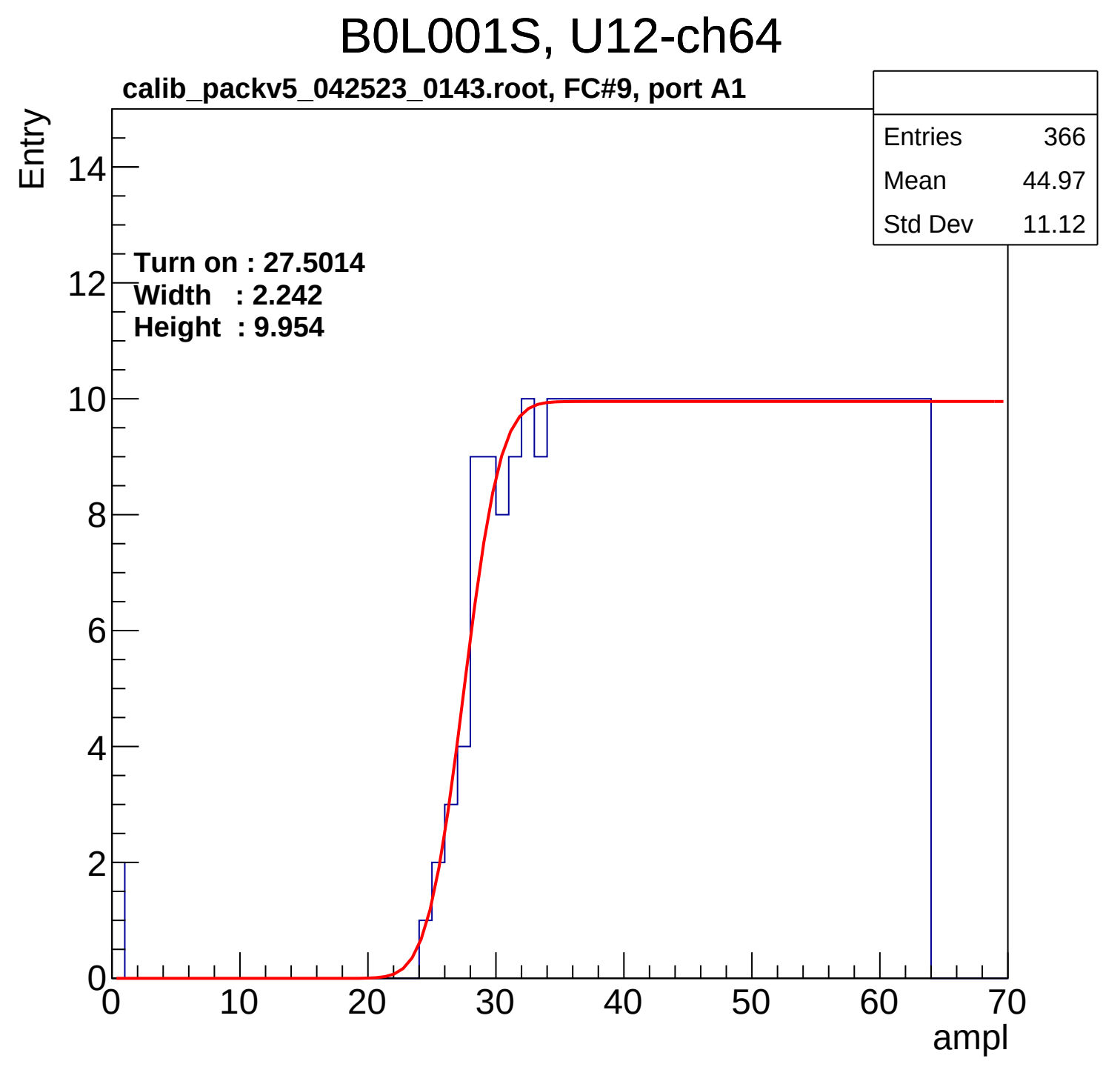
B0L001S, U12-ch64
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.97
Std Dev 11.12
Turn on : 27.5014
Width : 2.242
Height : 9.954
Entry
ampl
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2
4
6
8
10
12
14
0
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60
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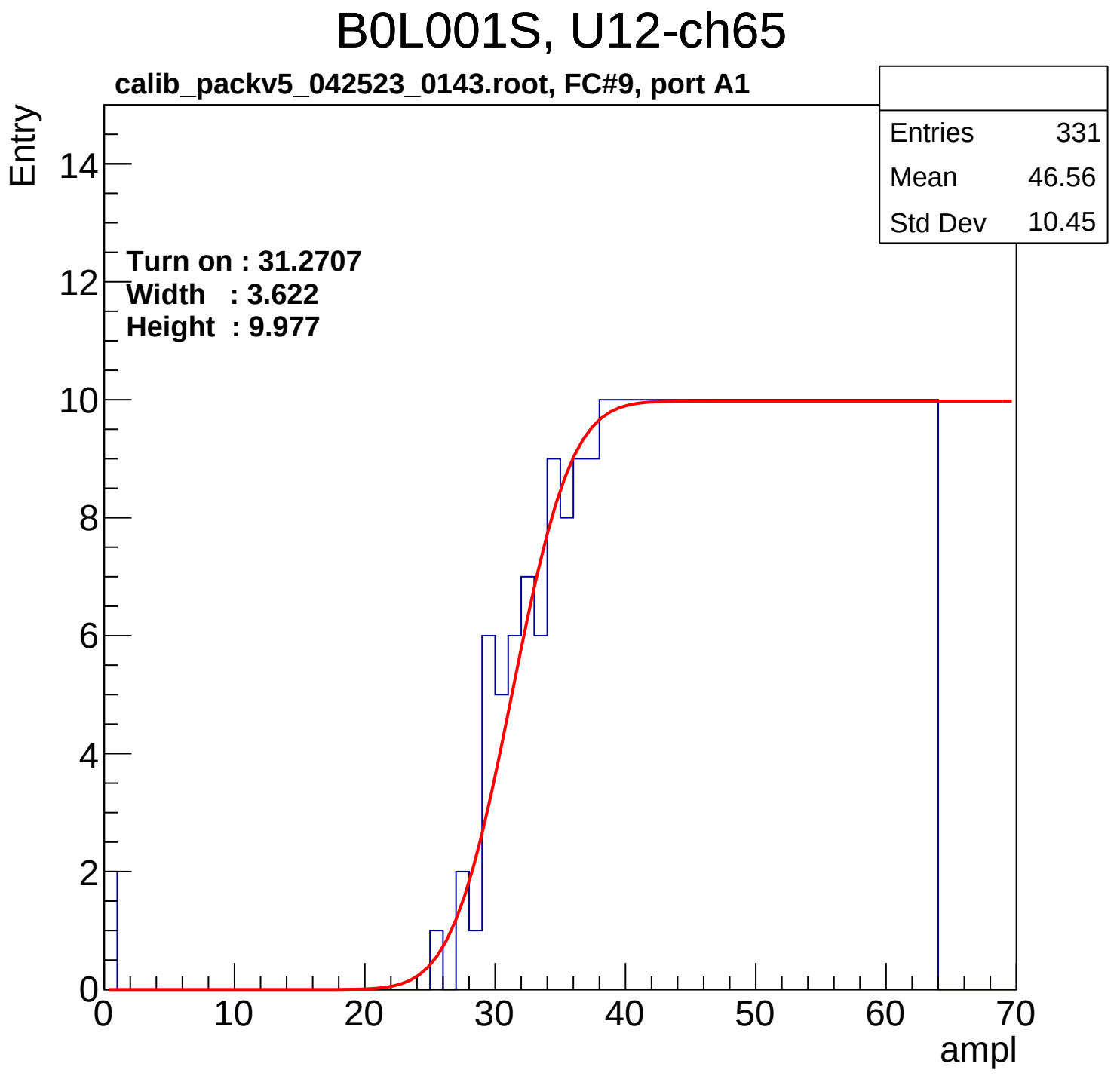
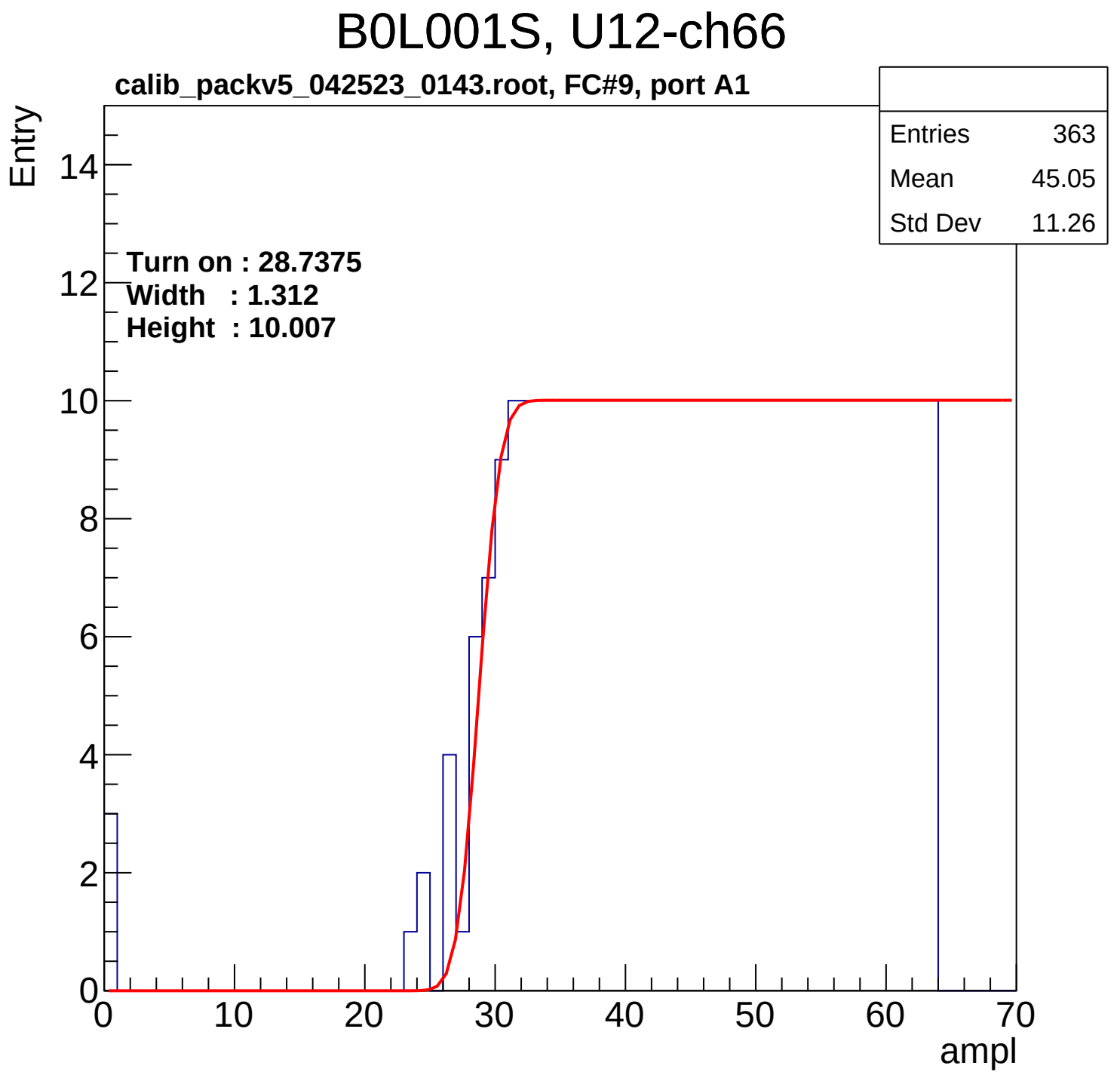

B0L001S, U12-ch65
calib_packv5_042523_0143.root, FC#9, port A1
Entries 331
Mean 46.56
Std Dev 10.45
Turn on : 31.2707
Width : 3.622
Height : 9.977
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U12-ch66
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 45.05
Std Dev 11.26
Turn on : 28.7375
Width : 1.312
Height : 10.007
Entry
ampl
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2
4
6
8
10
12
14
0
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20
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60
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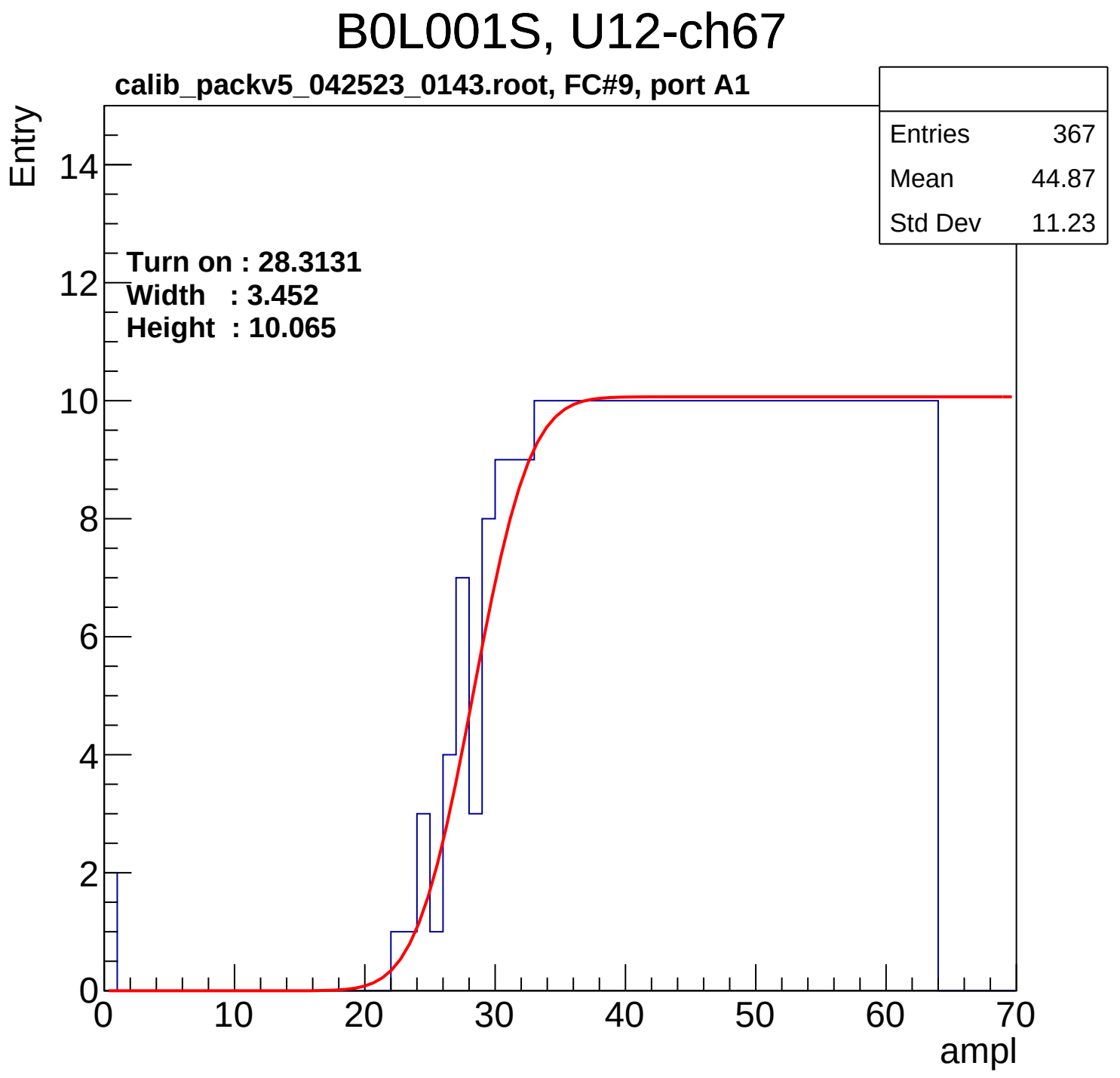
B0L001S, U12-ch67
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.87
Std Dev 11.23
Turn on : 28.3131
Width : 3.452
Height : 10.065
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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60
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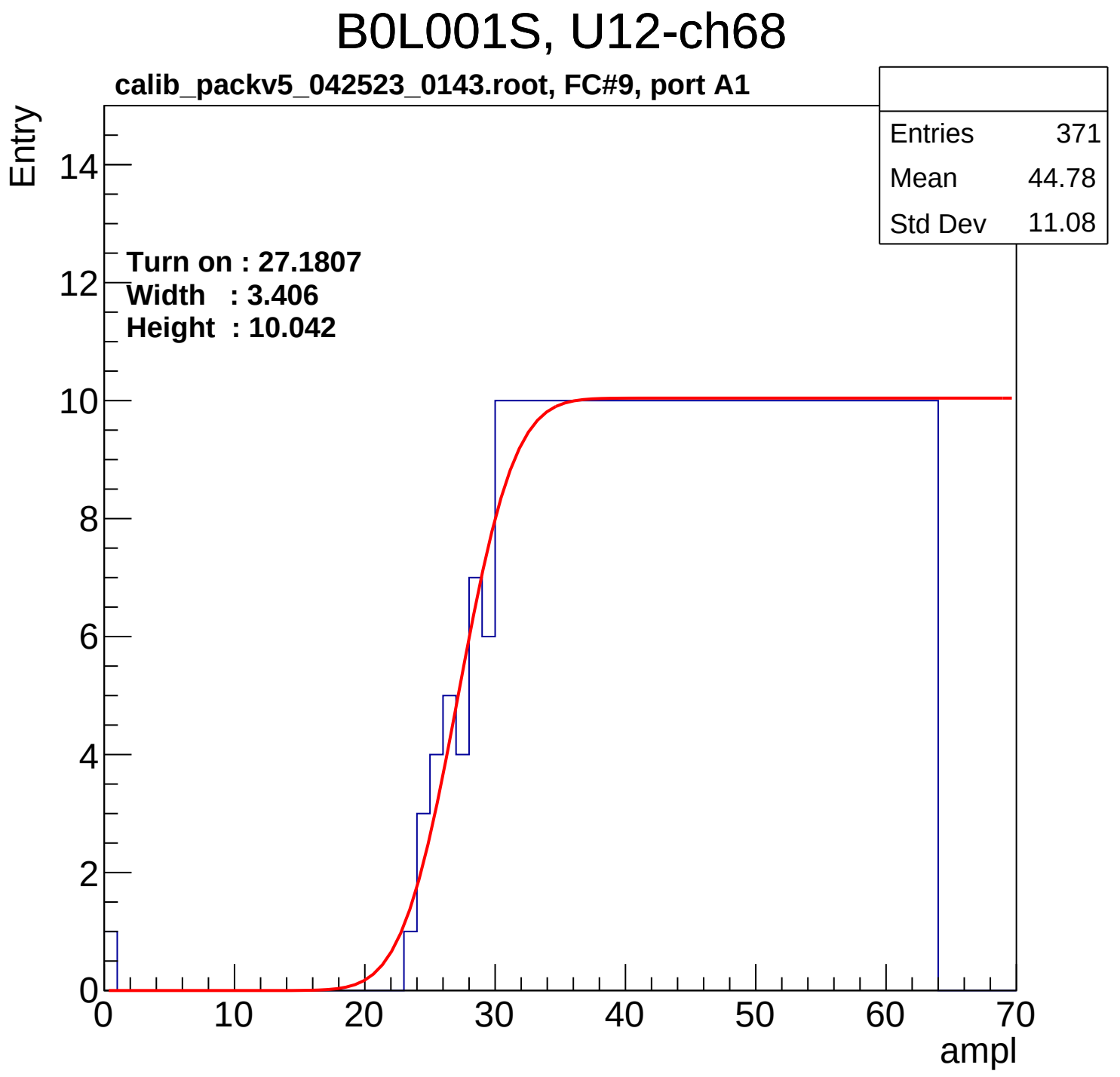
B0L001S, U12-ch68
calib_packv5_042523_0143.root, FC#9, port A1
Entries 371
Mean 44.78
Std Dev 11.08
Turn on : 27.1807
Width : 3.406
Height : 10.042
Entry
ampl
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6
8
10
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0
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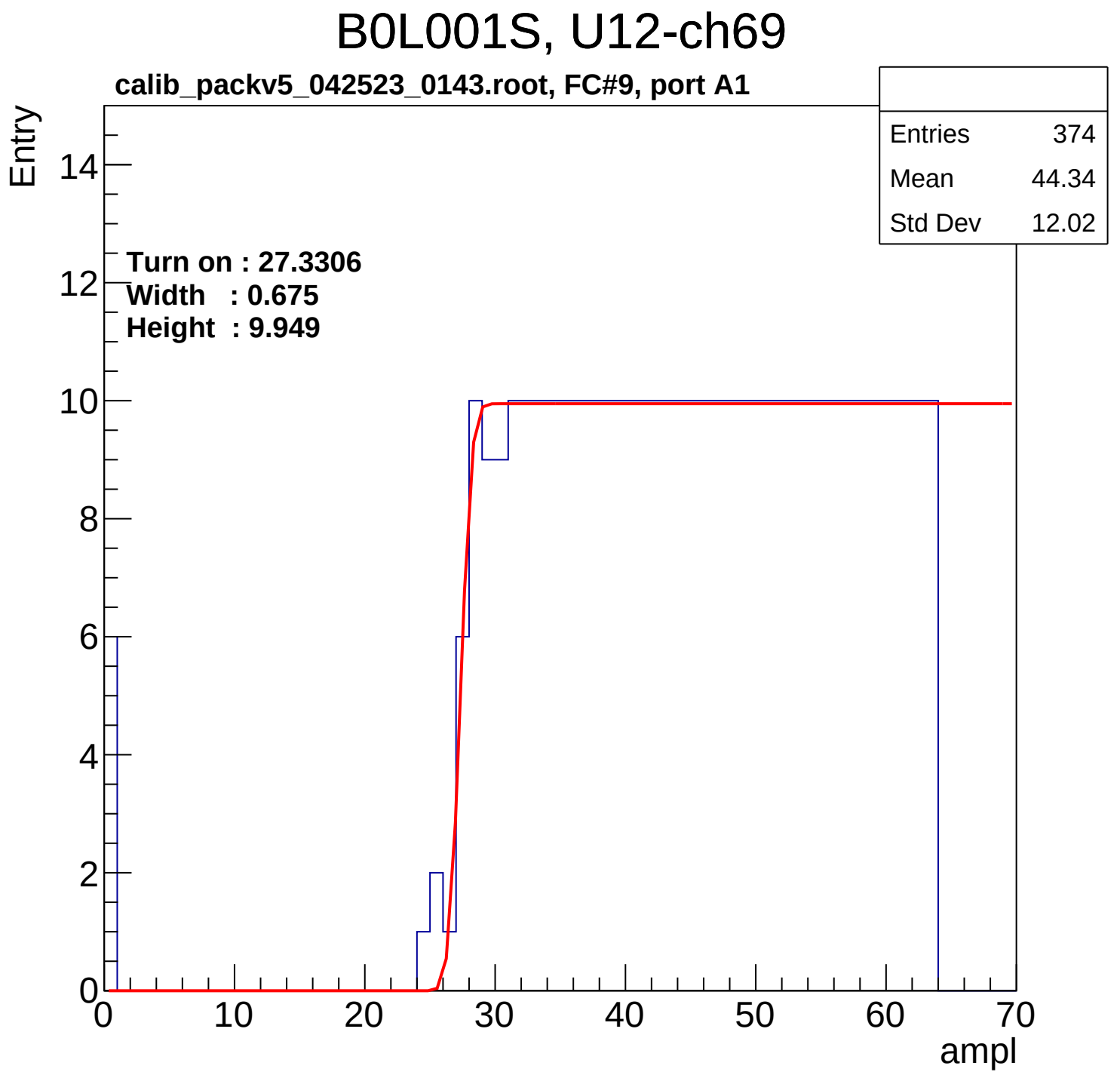
B0L001S, U12-ch69
calib_packv5_042523_0143.root, FC#9, port A1
Entries 374
Mean 44.34
Std Dev 12.02
Turn on : 27.3306
Width : 0.675
Height : 9.949
Entry
ampl
0
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6
8
10
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0
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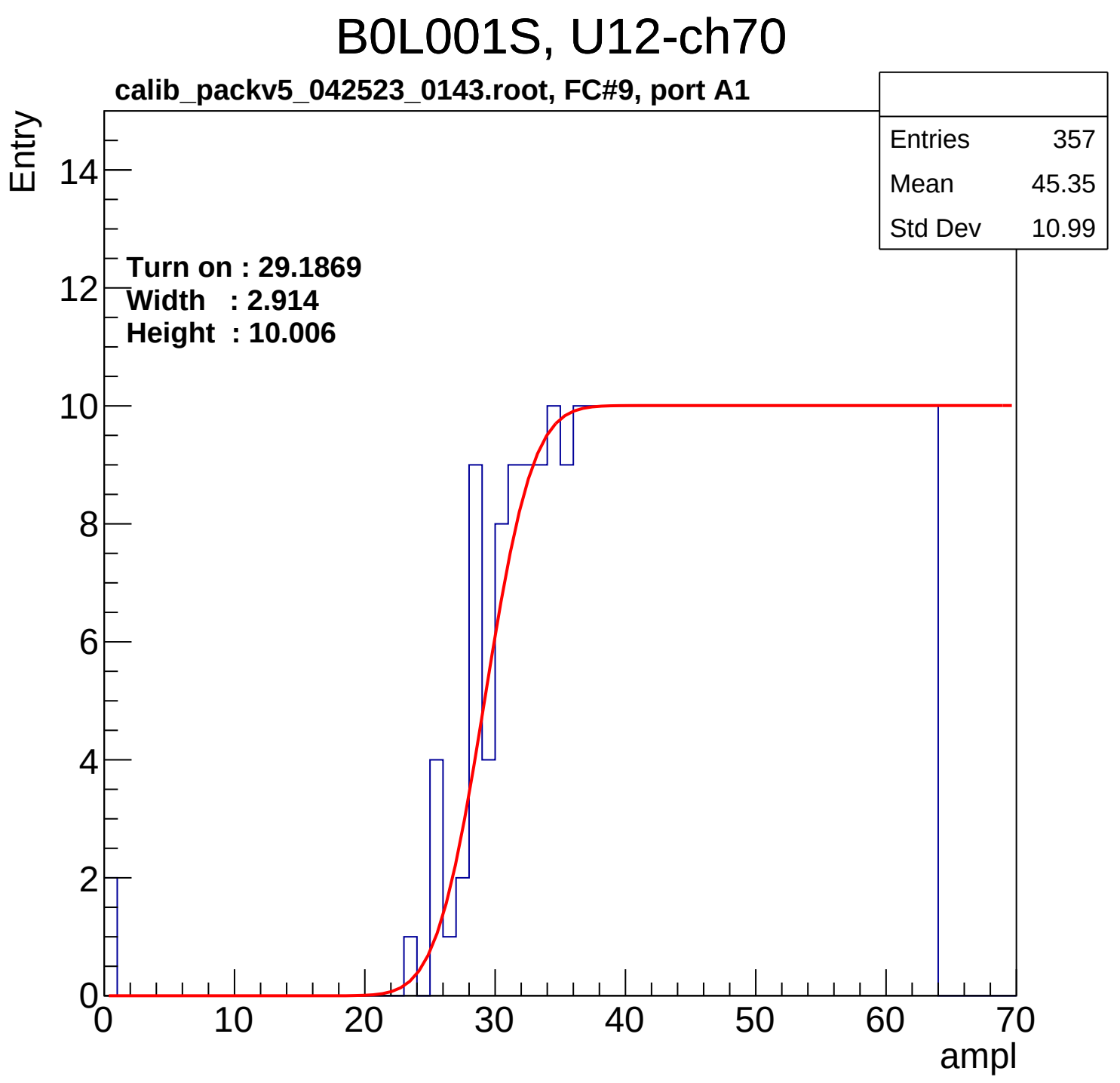
B0L001S, U12-ch70
calib_packv5_042523_0143.root, FC#9, port A1
Entries 357
Mean 45.35
Std Dev 10.99
Turn on : 29.1869
Width : 2.914
Height : 10.006
Entry
ampl
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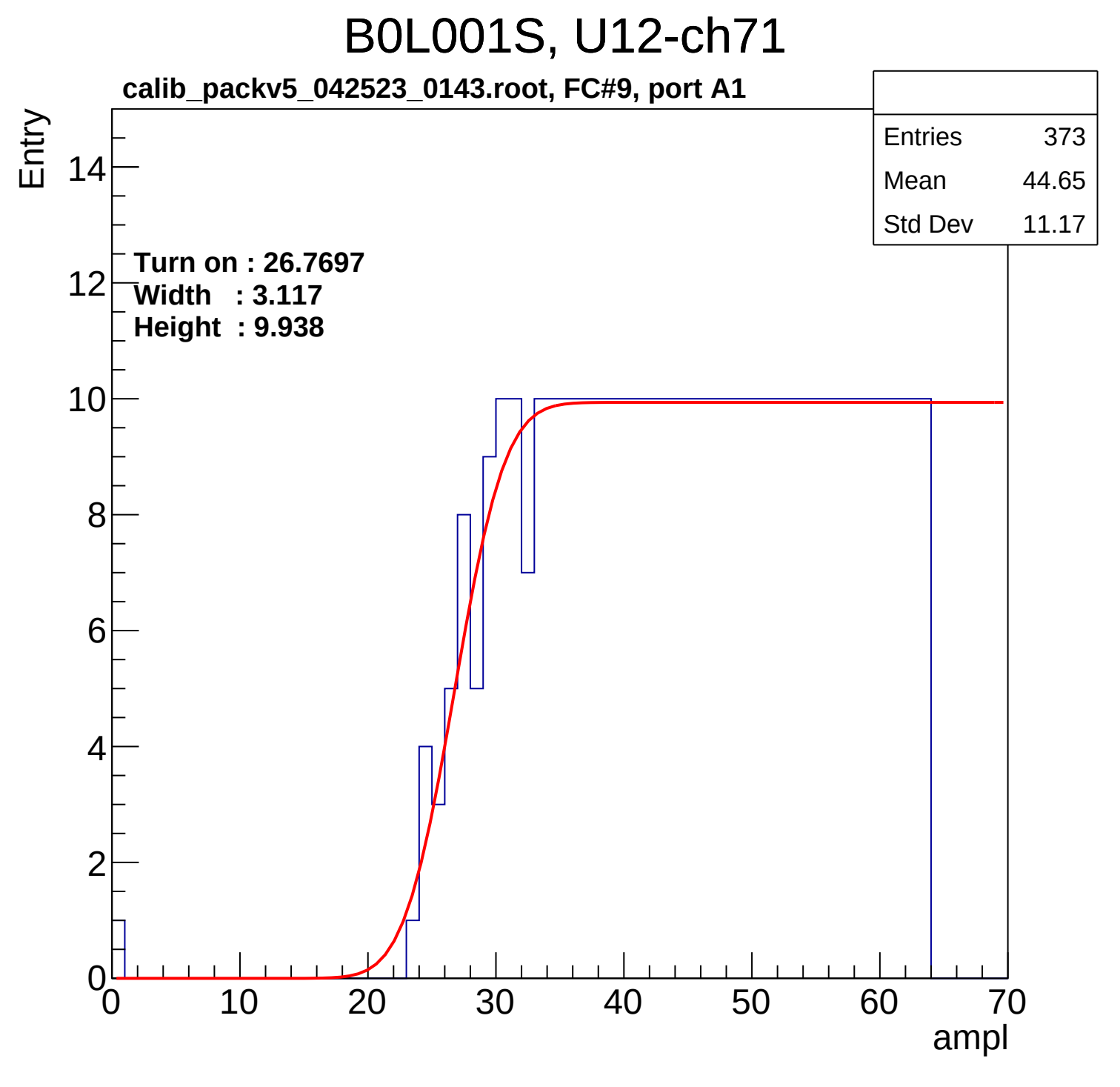
B0L001S, U12-ch71
calib_packv5_042523_0143.root, FC#9, port A1
Entries 373
Mean 44.65
Std Dev 11.17
Turn on : 26.7697
Width : 3.117
Height : 9.938
Entry
ampl
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6
8
10
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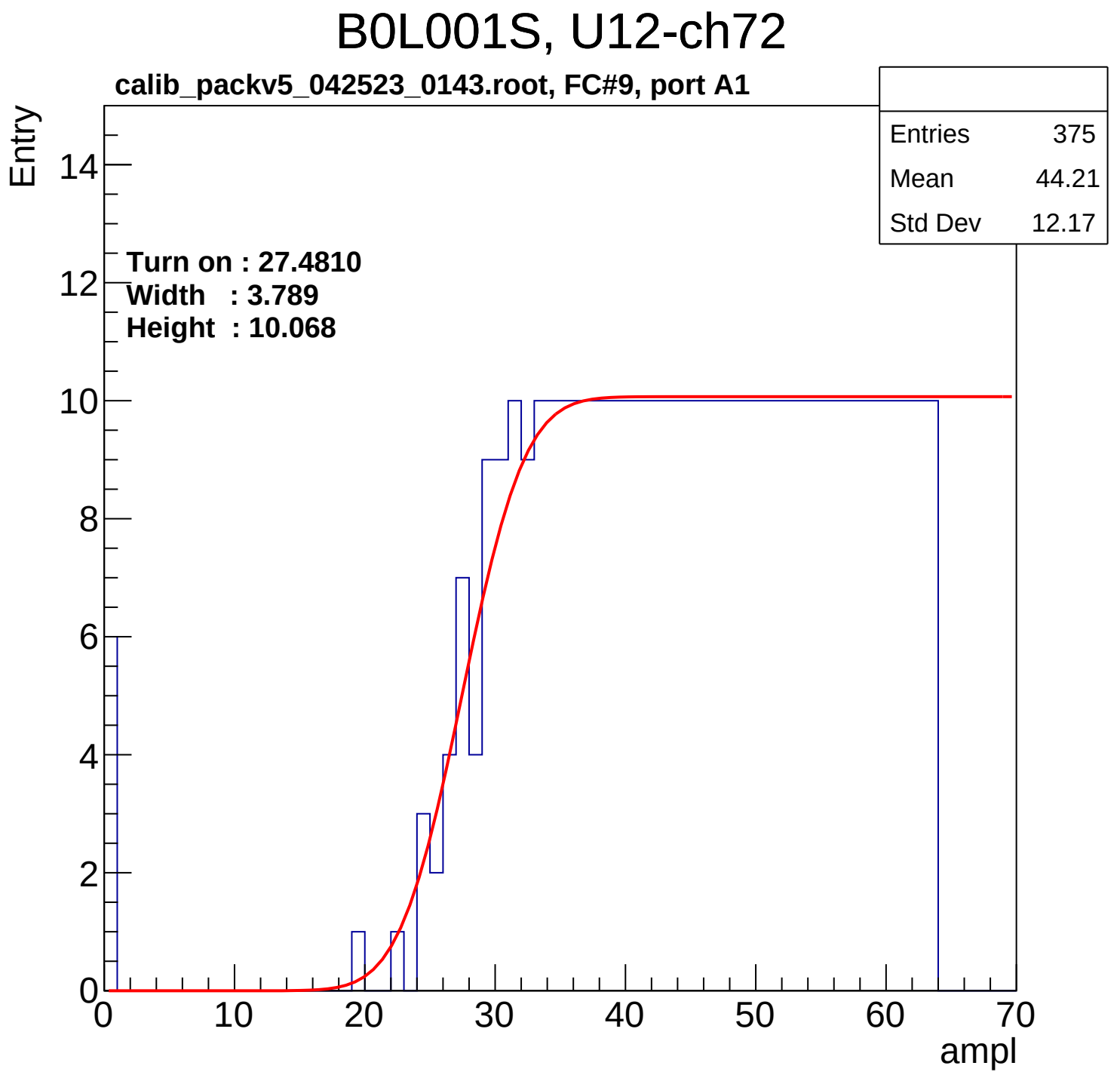
B0L001S, U12-ch72
calib_packv5_042523_0143.root, FC#9, port A1
Entries 375
Mean 44.21
Std Dev 12.17
Turn on : 27.4810
Width : 3.789
Height : 10.068
Entry
ampl
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6
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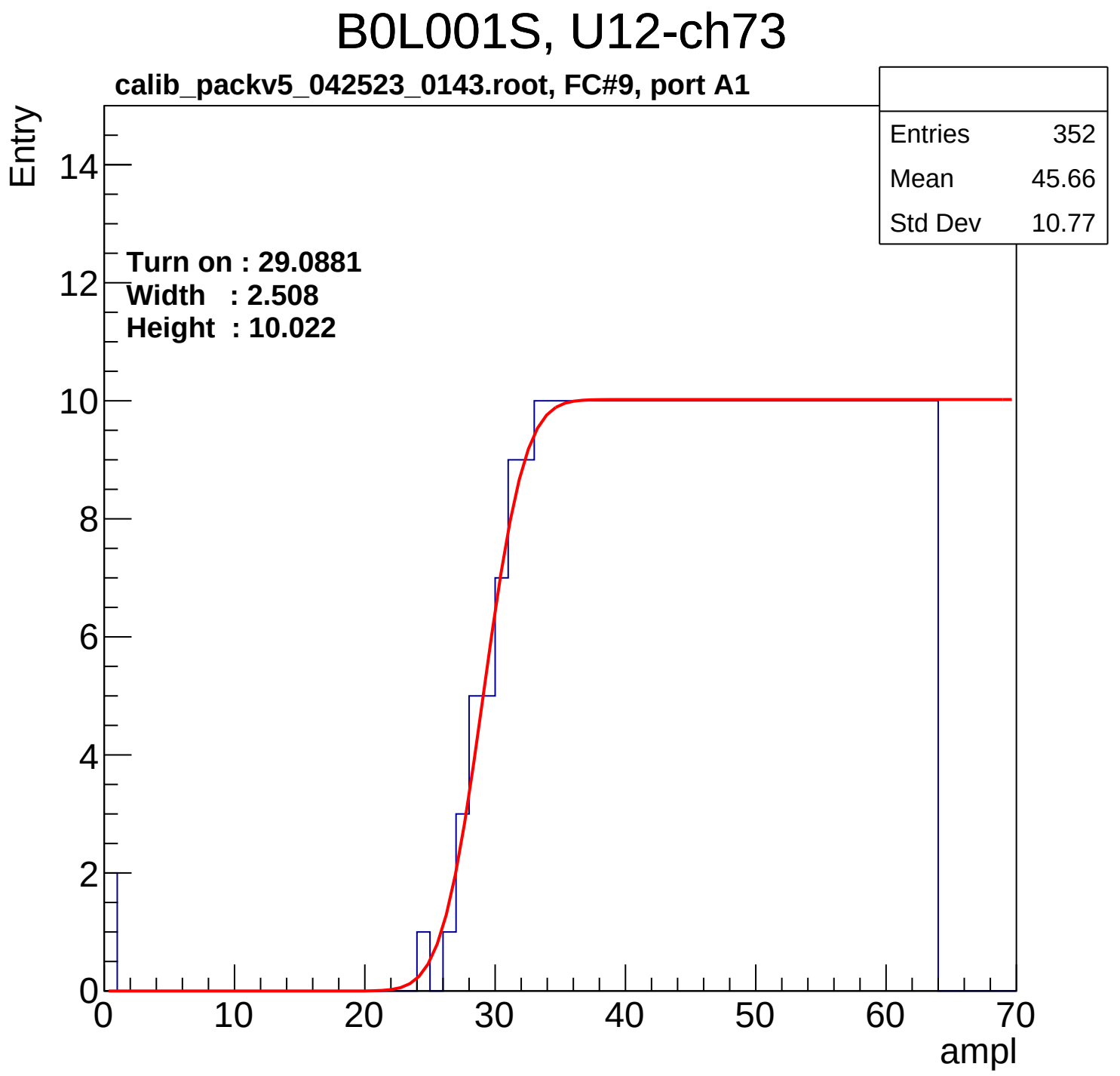
B0L001S, U12-ch73
calib_packv5_042523_0143.root, FC#9, port A1
Entries 352
Mean 45.66
Std Dev 10.77
Turn on : 29.0881
Width : 2.508
Height : 10.022
Entry
ampl
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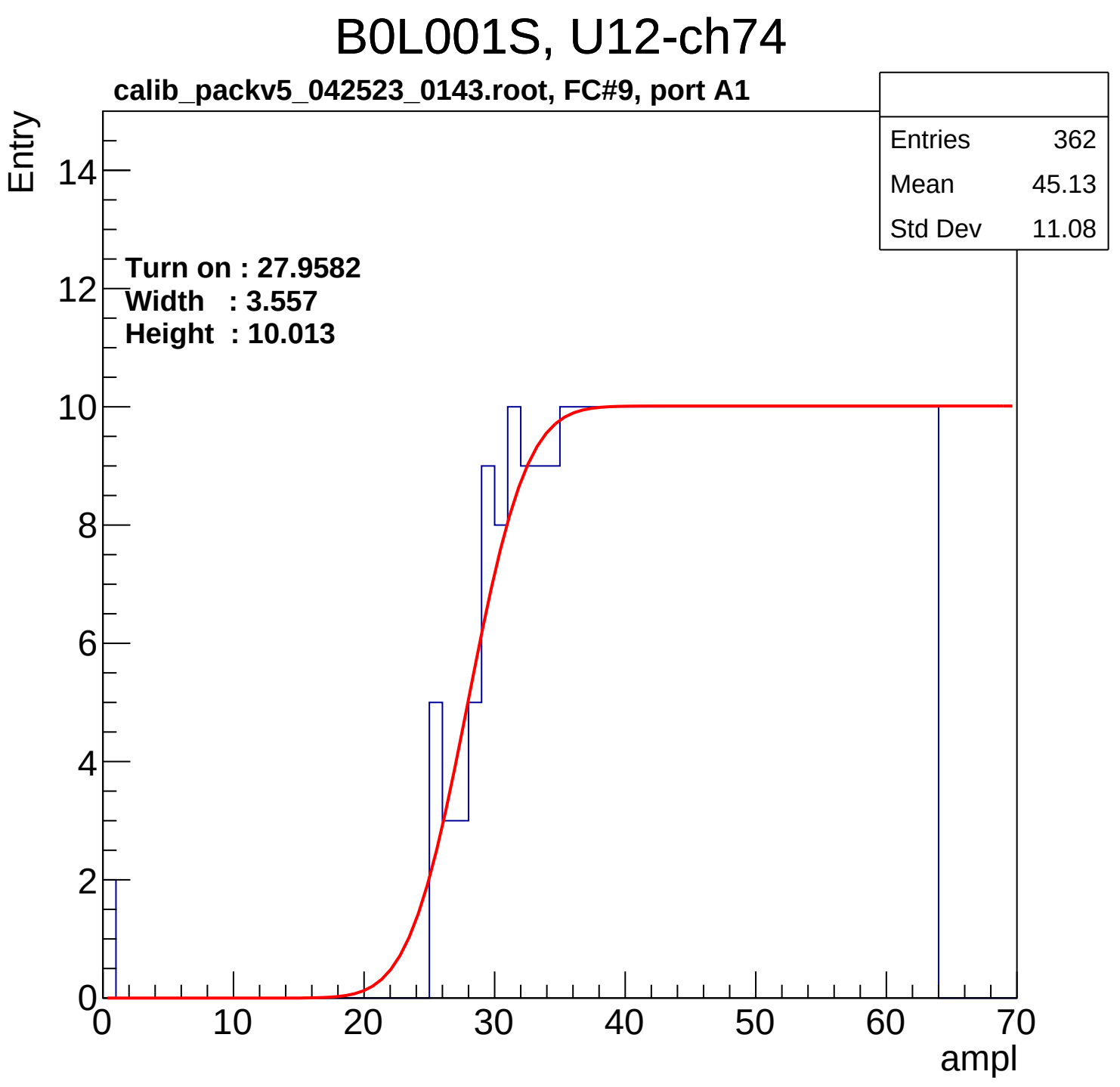
B0L001S, U12-ch74
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 45.13
Std Dev 11.08
Turn on : 27.9582
Width : 3.557
Height : 10.013
Entry
ampl
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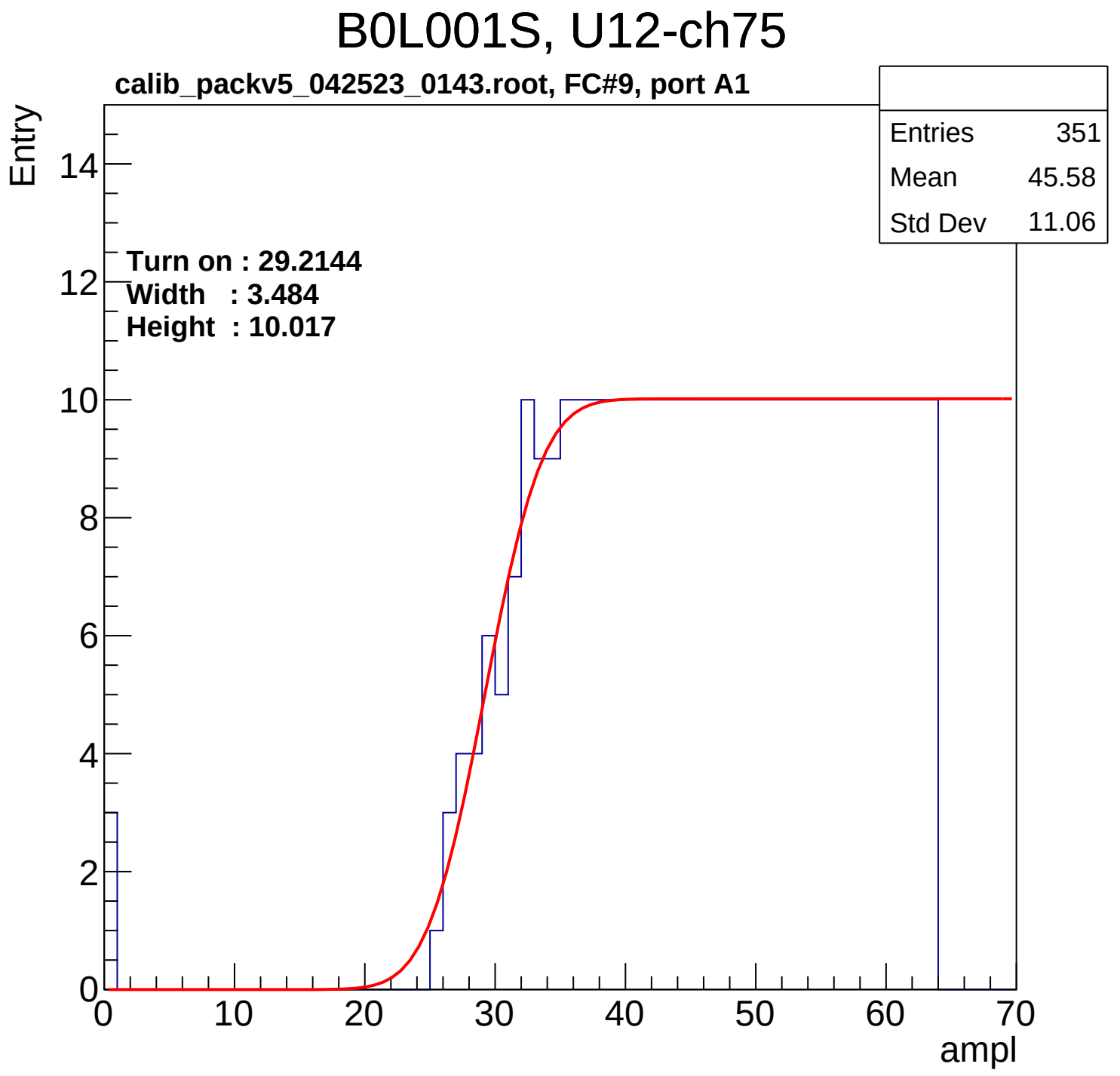
B0L001S, U12-ch75
calib_packv5_042523_0143.root, FC#9, port A1
Entries 351
Mean 45.58
Std Dev 11.06
Turn on : 29.2144
Width : 3.484
Height : 10.017
Entry
ampl
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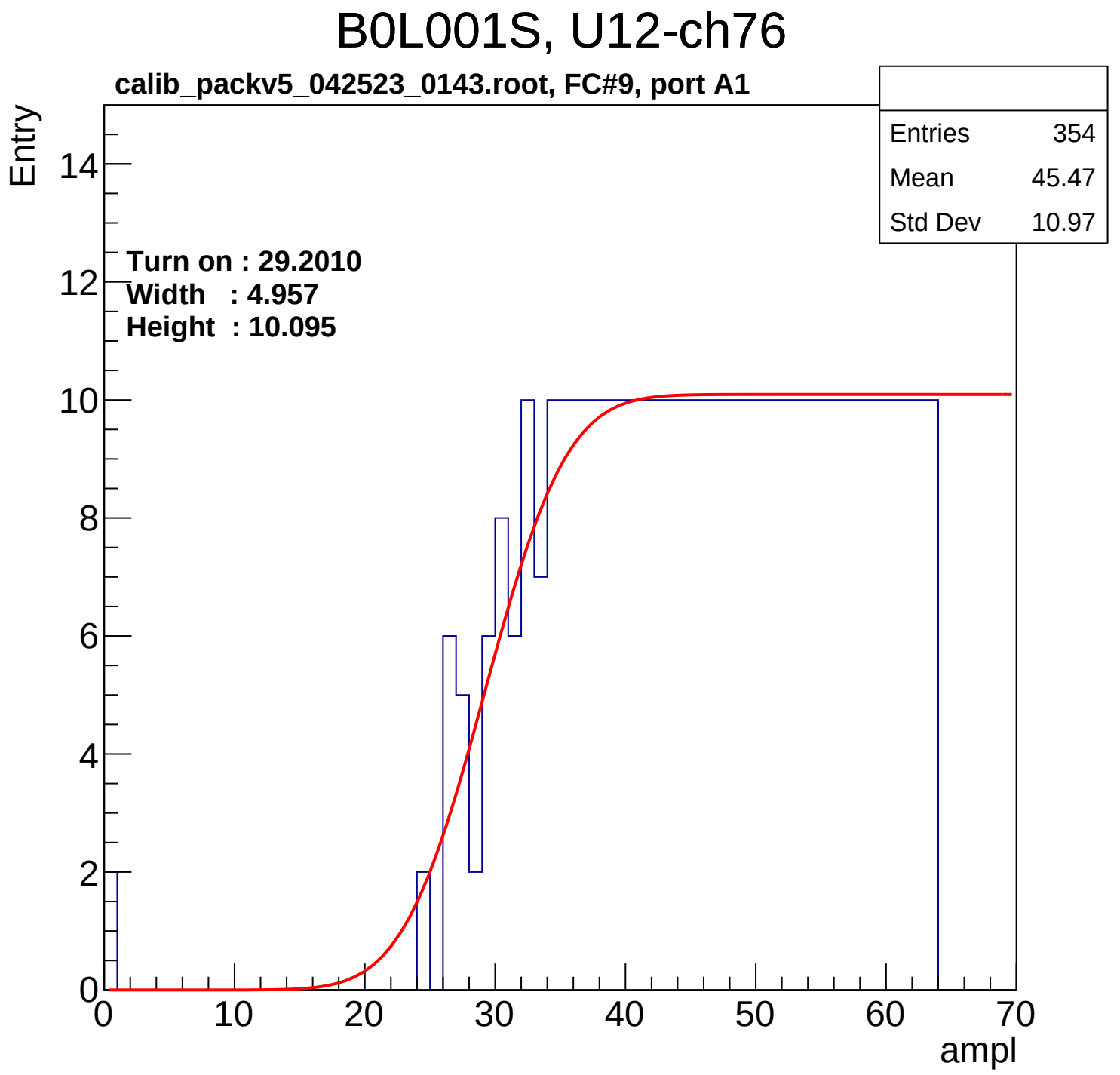
B0L001S, U12-ch76
calib_packv5_042523_0143.root, FC#9, port A1
Entries 354
Mean 45.47
Std Dev 10.97
Turn on : 29.2010
Width : 4.957
Height : 10.095
Entry
ampl
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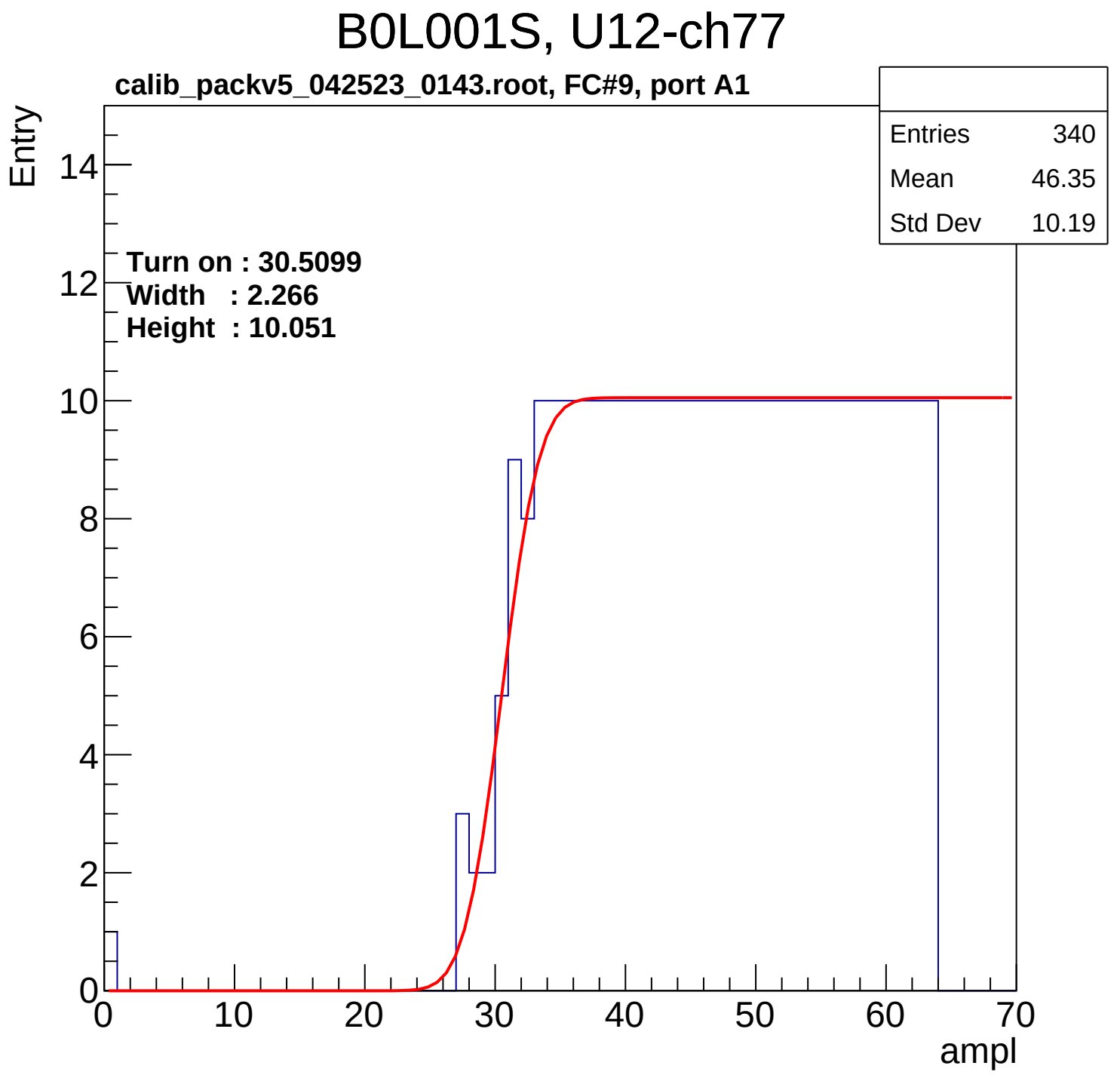
B0L001S, U12-ch77
calib_packv5_042523_0143.root, FC#9, port A1
Entries 340
Mean 46.35
Std Dev 10.19
Turn on : 30.5099
Width : 2.266
Height : 10.051
Entry
ampl
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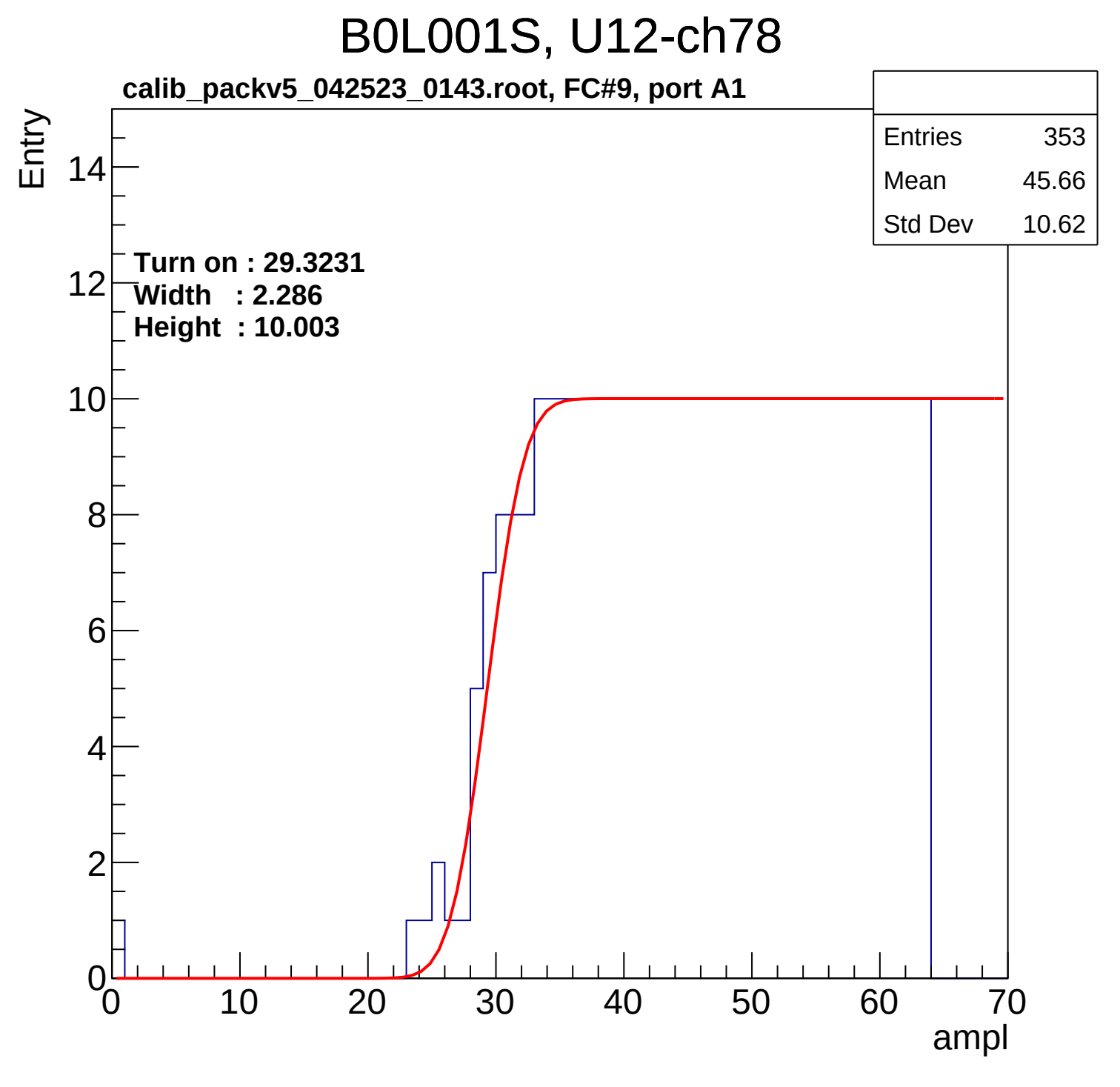
B0L001S, U12-ch78
calib_packv5_042523_0143.root, FC#9, port A1
Entries 353
Mean 45.66
Std Dev 10.62
Turn on : 29.3231
Width : 2.286
Height : 10.003
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ampl
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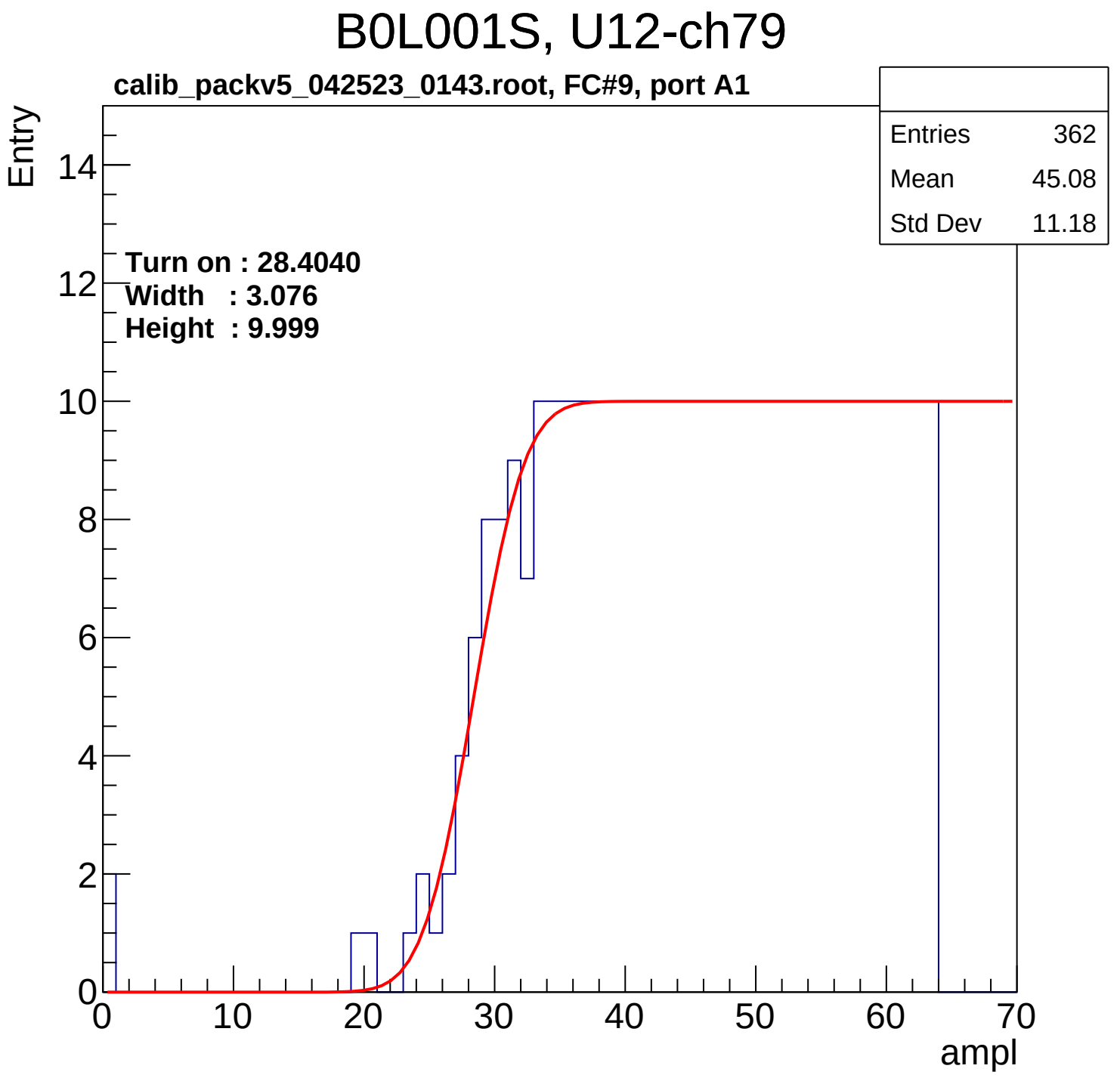
B0L001S, U12-ch79
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 45.08
Std Dev 11.18
Turn on : 28.4040
Width : 3.076
Height : 9.999
Entry
ampl
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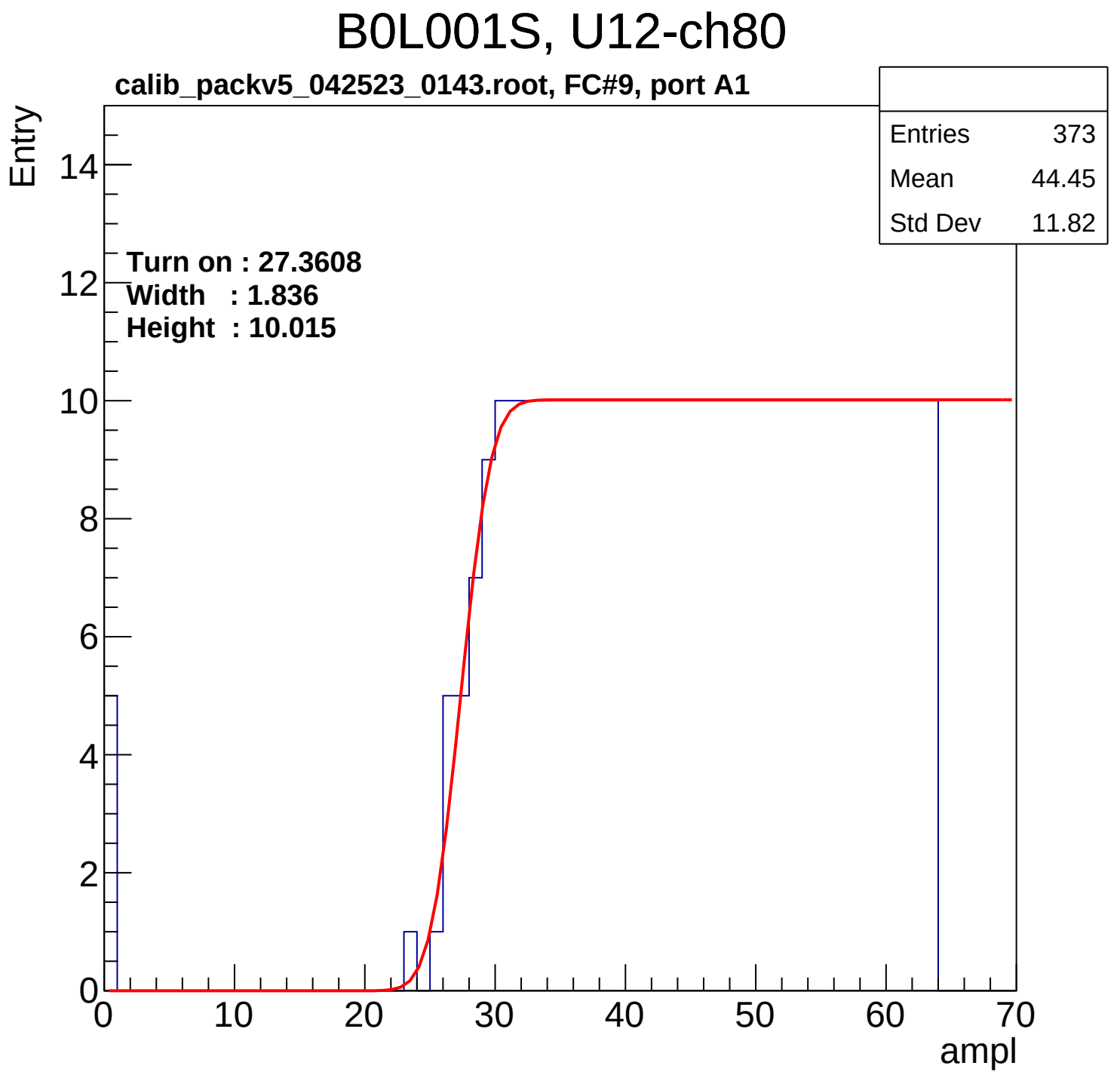
B0L001S, U12-ch80
calib_packv5_042523_0143.root, FC#9, port A1
Entries 373
Mean 44.45
Std Dev 11.82
Turn on : 27.3608
Width : 1.836
Height : 10.015
Entry
ampl
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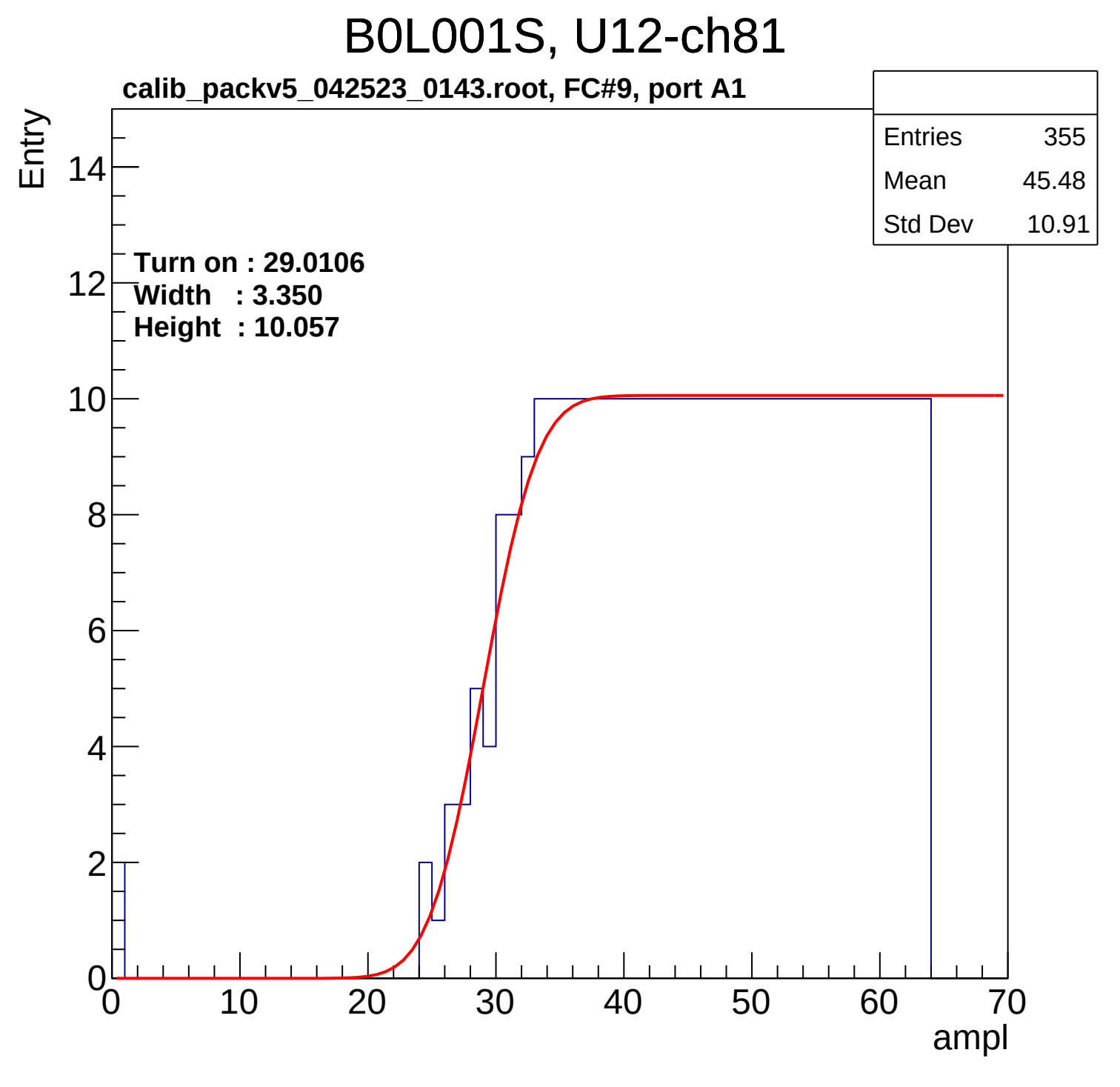
B0L001S, U12-ch81
calib_packv5_042523_0143.root, FC#9, port A1
Entries 355
Mean 45.48
Std Dev 10.91
Turn on : 29.0106
Width : 3.350
Height : 10.057
Entry
ampl
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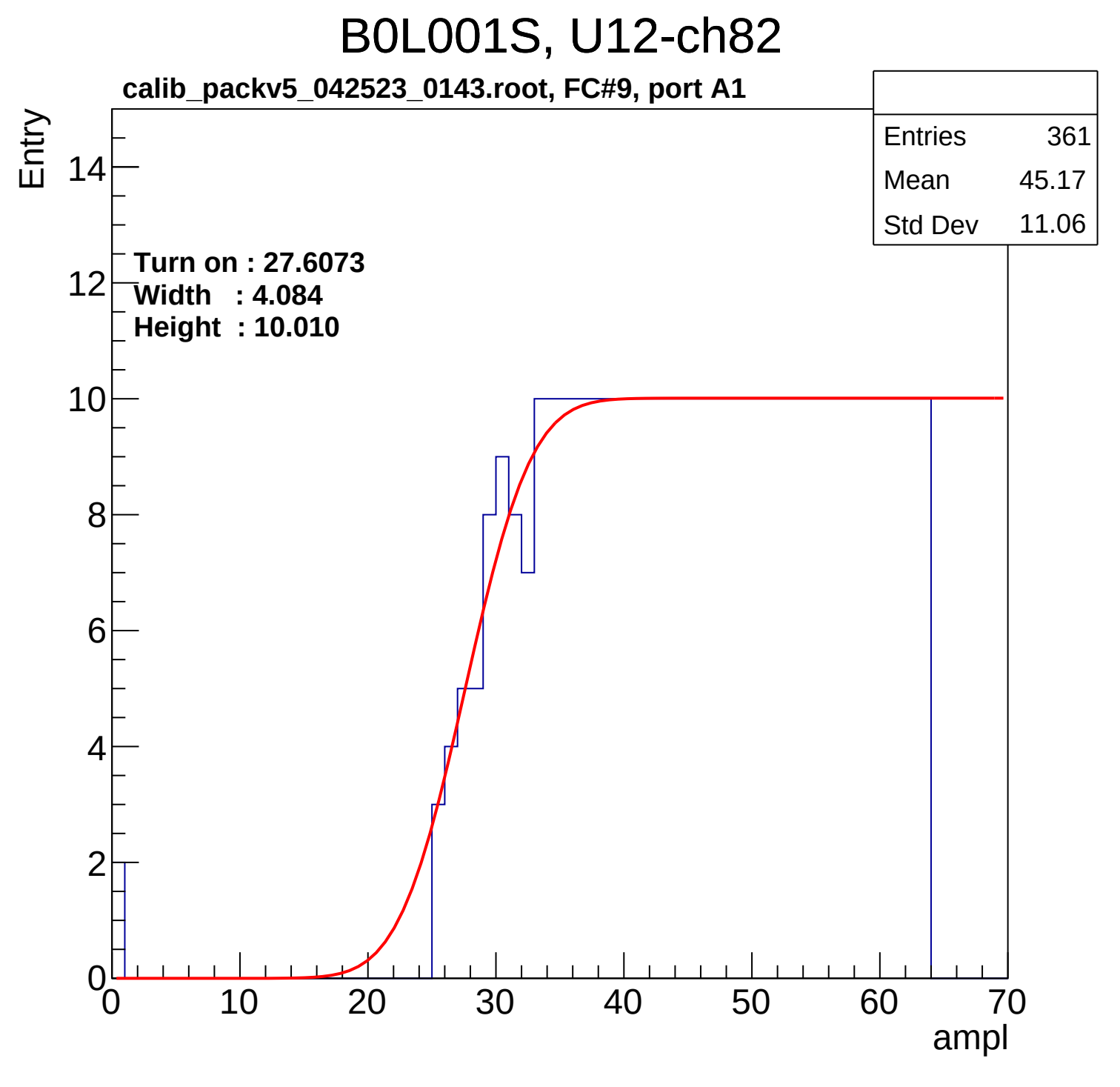
B0L001S, U12-ch82
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 45.17
Std Dev 11.06
Turn on : 27.6073
Width : 4.084
Height : 10.010
Entry
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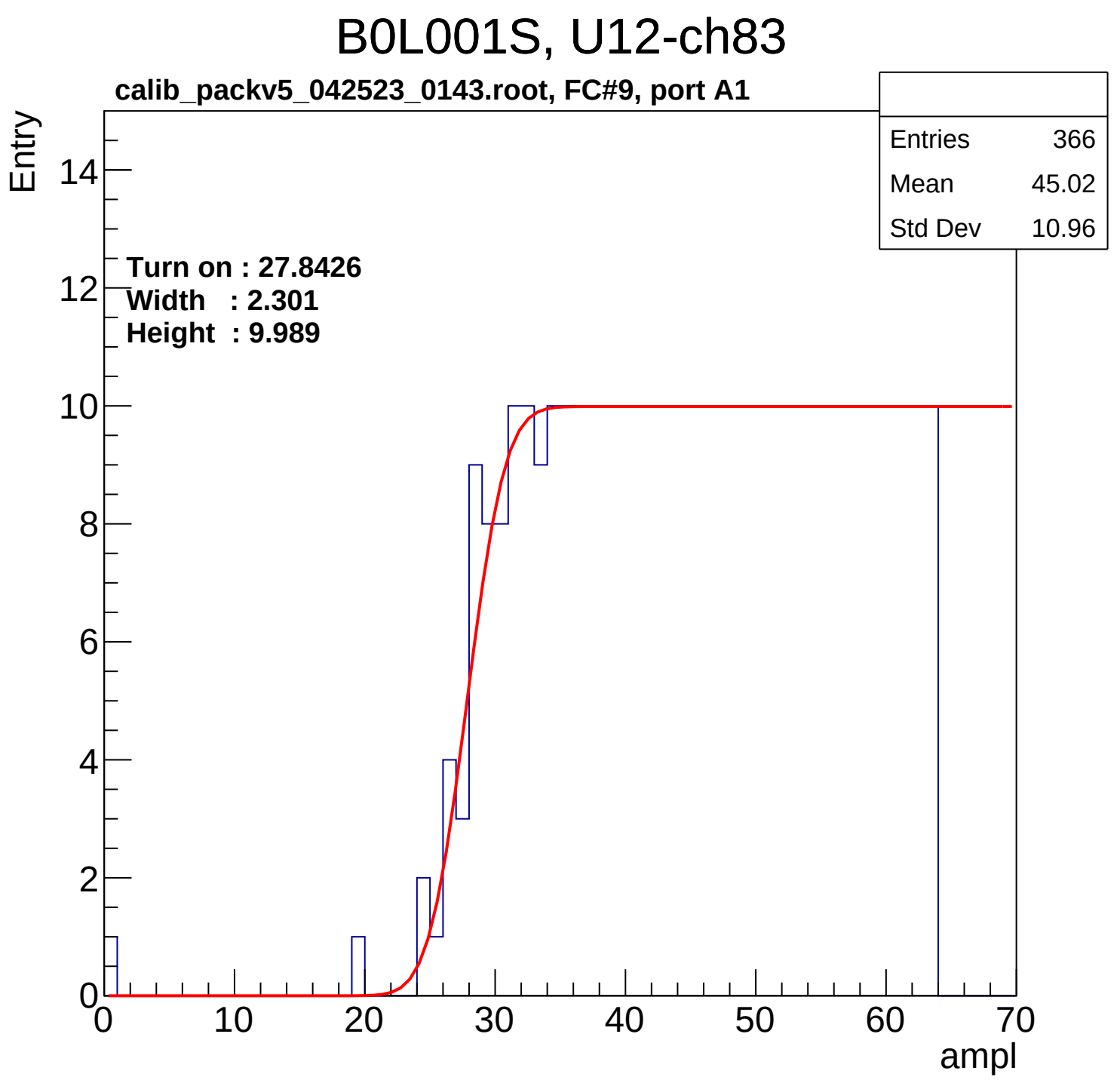
B0L001S, U12-ch83
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 45.02
Std Dev 10.96
Turn on : 27.8426
Width : 2.301
Height : 9.989
Entry
ampl
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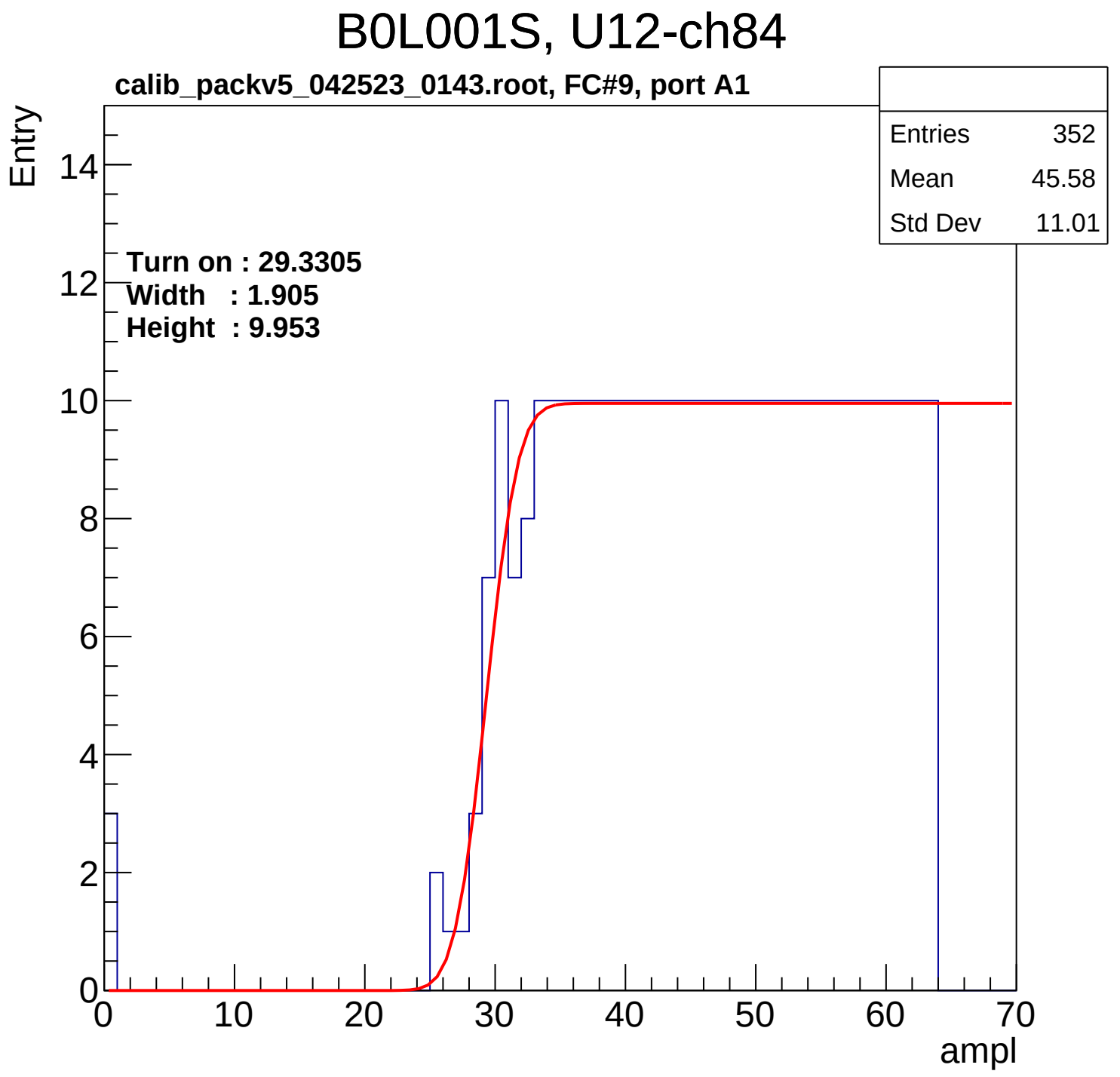
B0L001S, U12-ch84
calib_packv5_042523_0143.root, FC#9, port A1
Entries 352
Mean 45.58
Std Dev 11.01
Turn on : 29.3305
Width : 1.905
Height : 9.953
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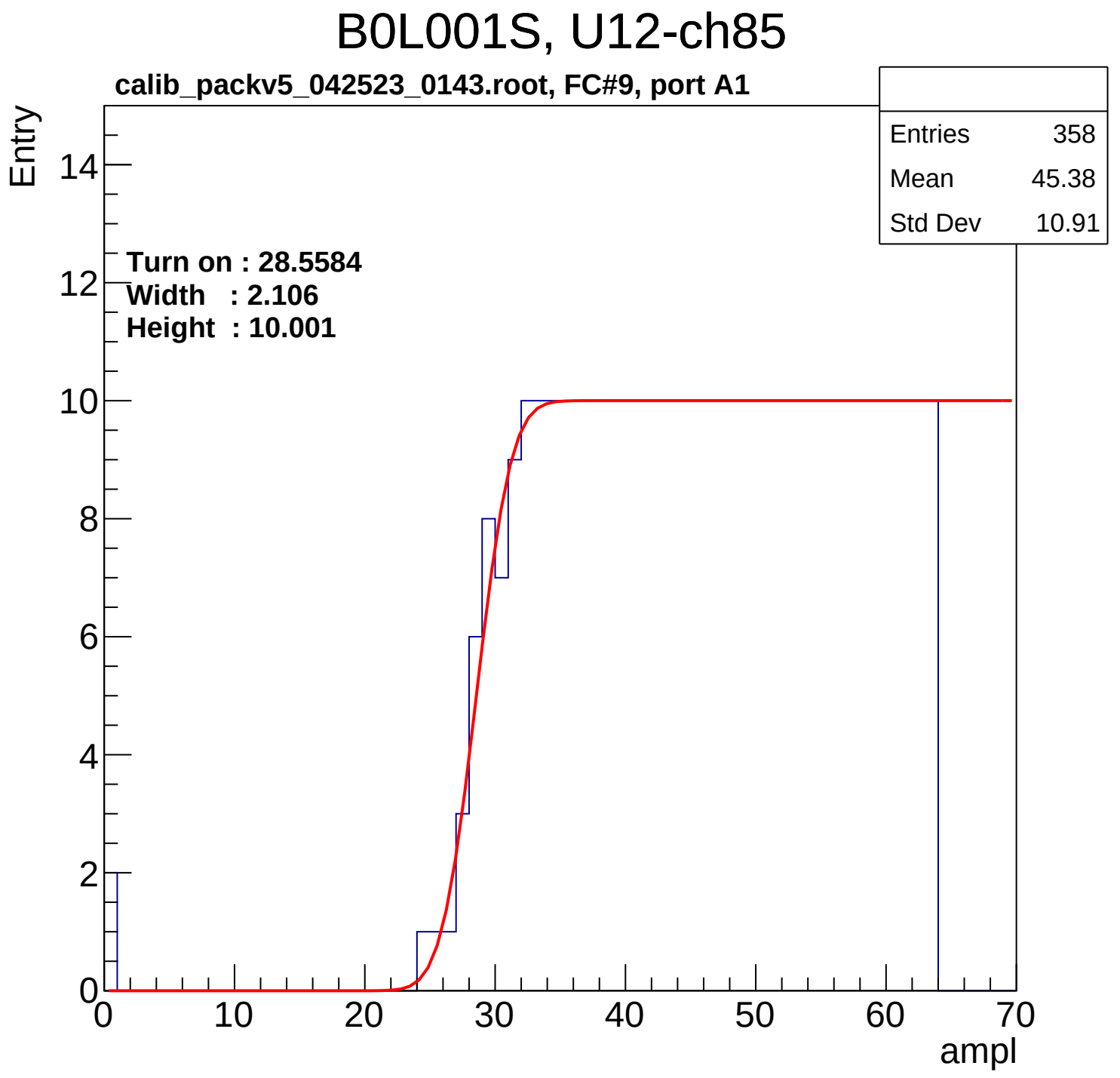
B0L001S, U12-ch85
calib_packv5_042523_0143.root, FC#9, port A1
Entries 358
Mean 45.38
Std Dev 10.91
Turn on : 28.5584
Width : 2.106
Height : 10.001
Entry
ampl
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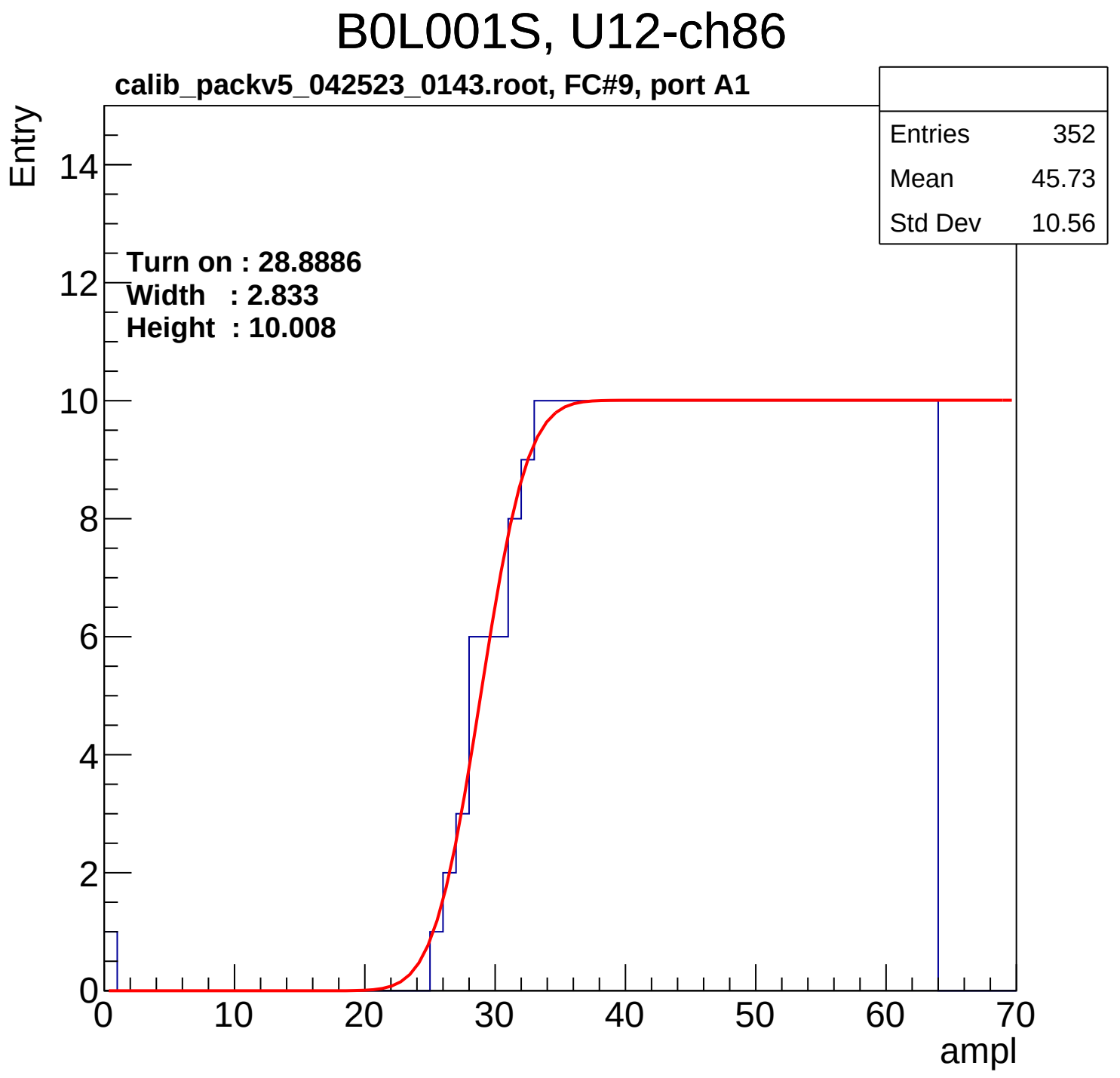
B0L001S, U12-ch86
calib_packv5_042523_0143.root, FC#9, port A1
Entries 352
Mean 45.73
Std Dev 10.56
Turn on : 28.8886
Width : 2.833
Height : 10.008
Entry
ampl
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4
6
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10
20
30
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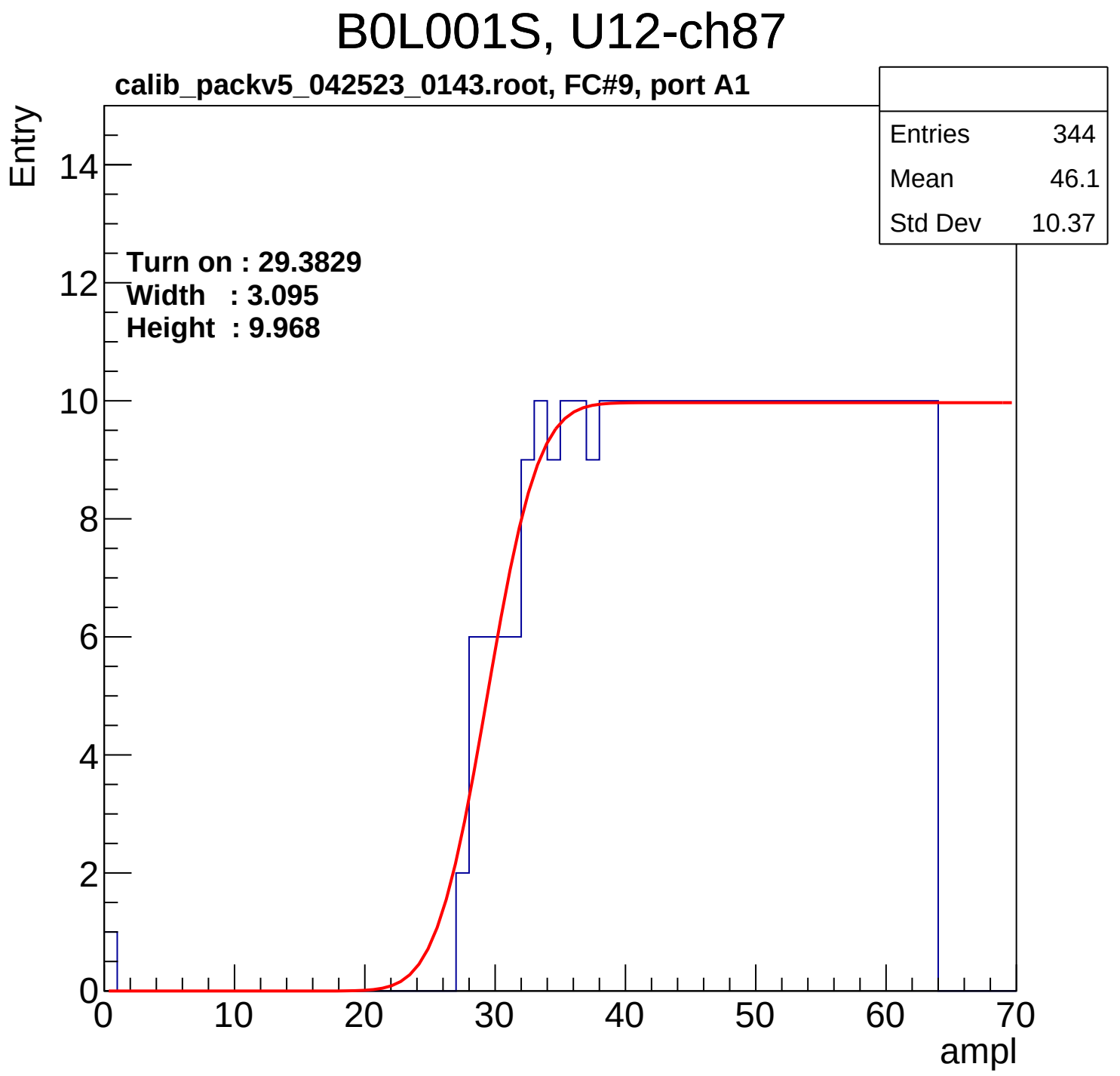
B0L001S, U12-ch87
calib_packv5_042523_0143.root, FC#9, port A1
Entries 344
Mean 46.1
Std Dev 10.37
Turn on : 29.3829
Width : 3.095
Height : 9.968
Entry
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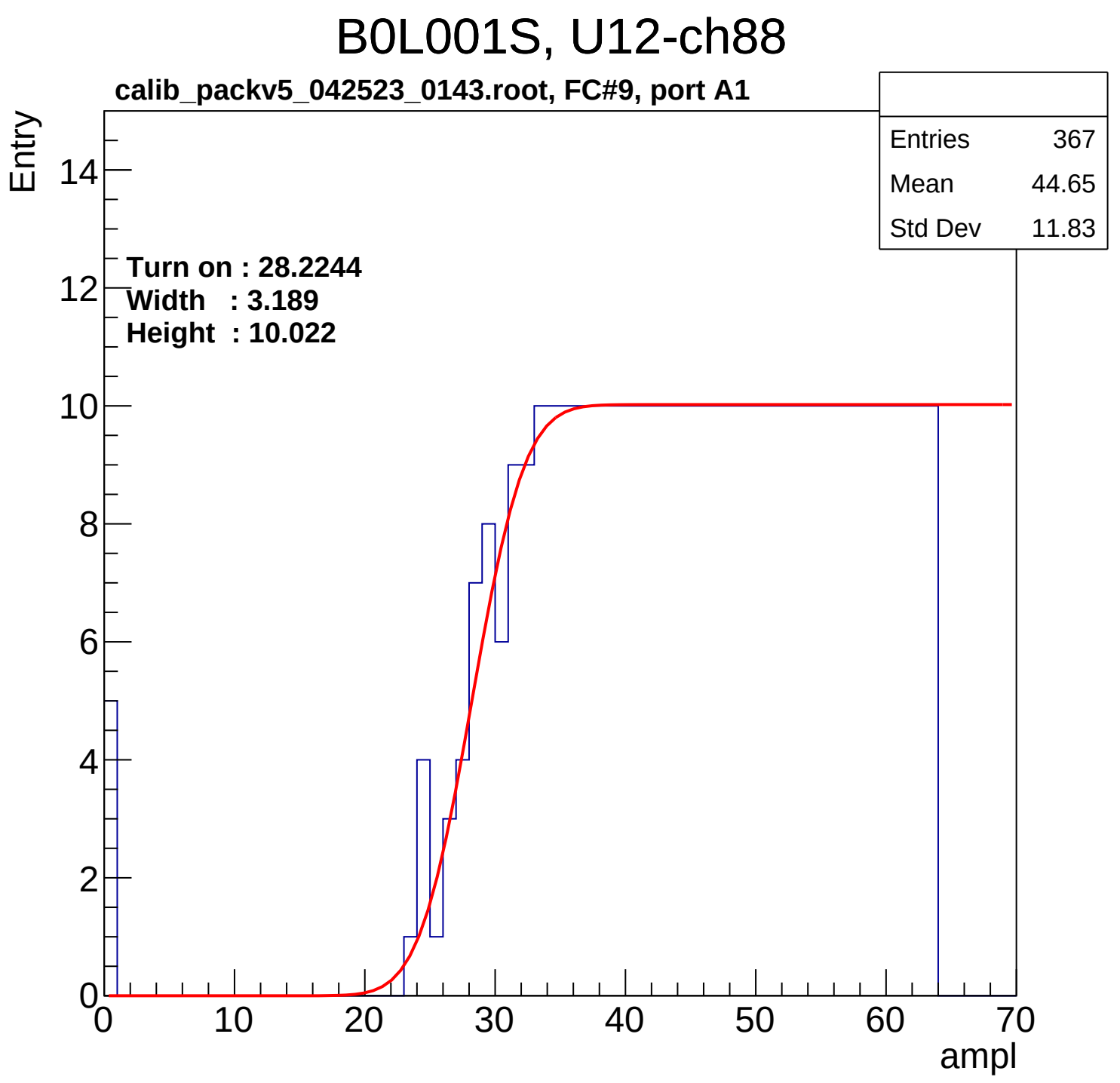
B0L001S, U12-ch88
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.65
Std Dev 11.83
Turn on : 28.2244
Width : 3.189
Height : 10.022
Entry
ampl
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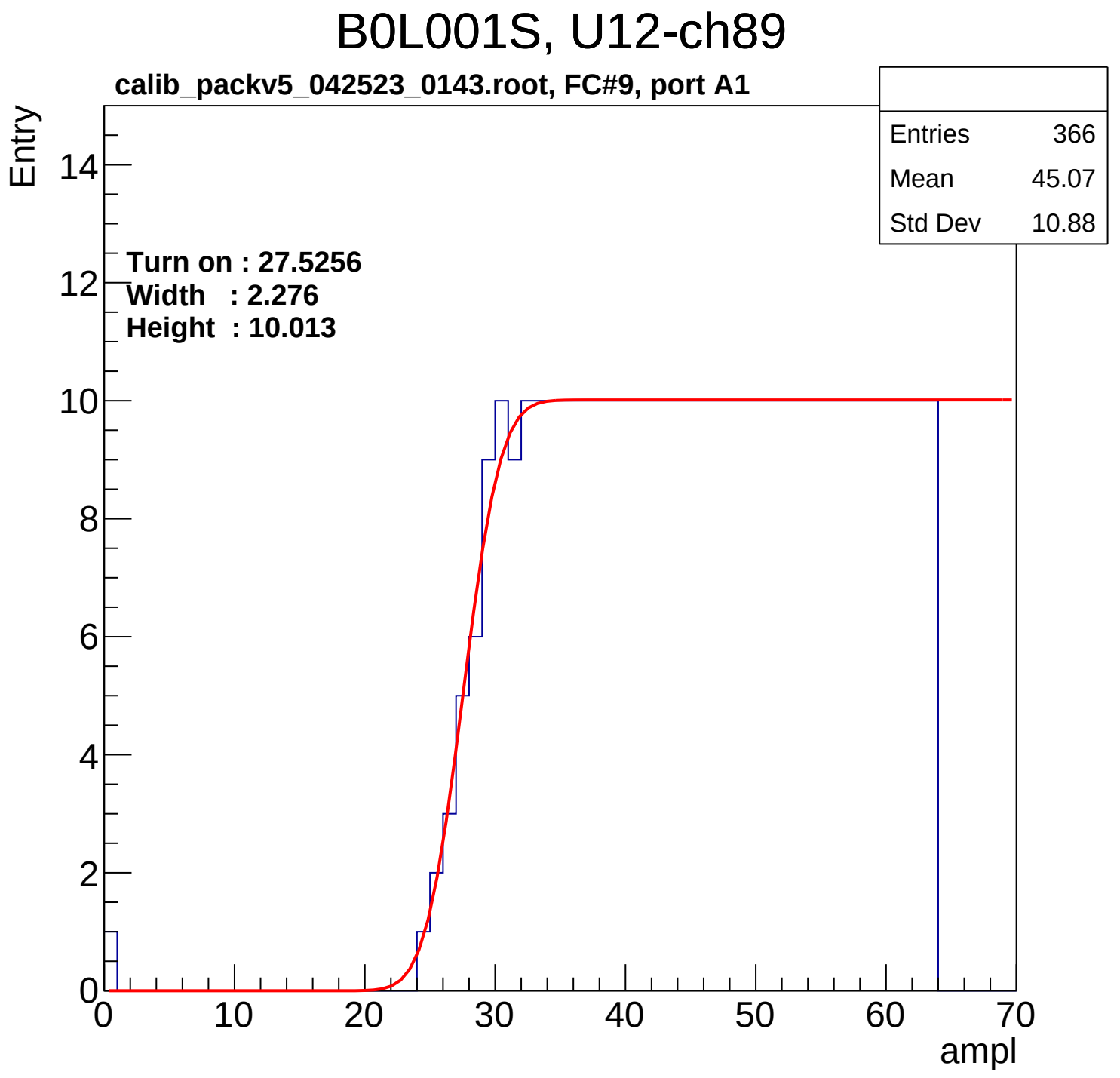
B0L001S, U12-ch89
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 45.07
Std Dev 10.88
Turn on : 27.5256
Width : 2.276
Height : 10.013
Entry
ampl
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2
4
6
8
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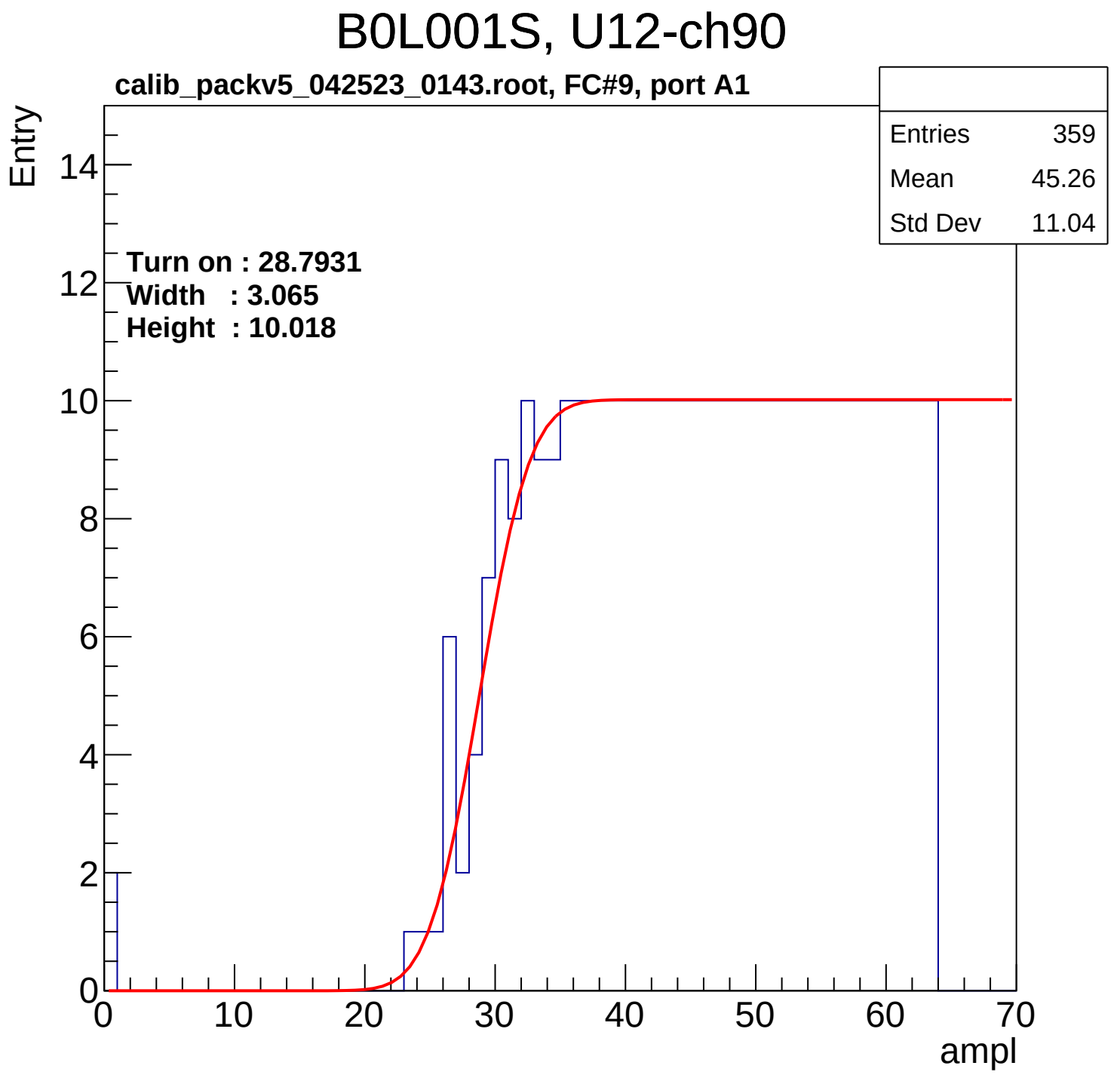
B0L001S, U12-ch90
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 45.26
Std Dev 11.04
Turn on : 28.7931
Width : 3.065
Height : 10.018
Entry
ampl
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2
4
6
8
10
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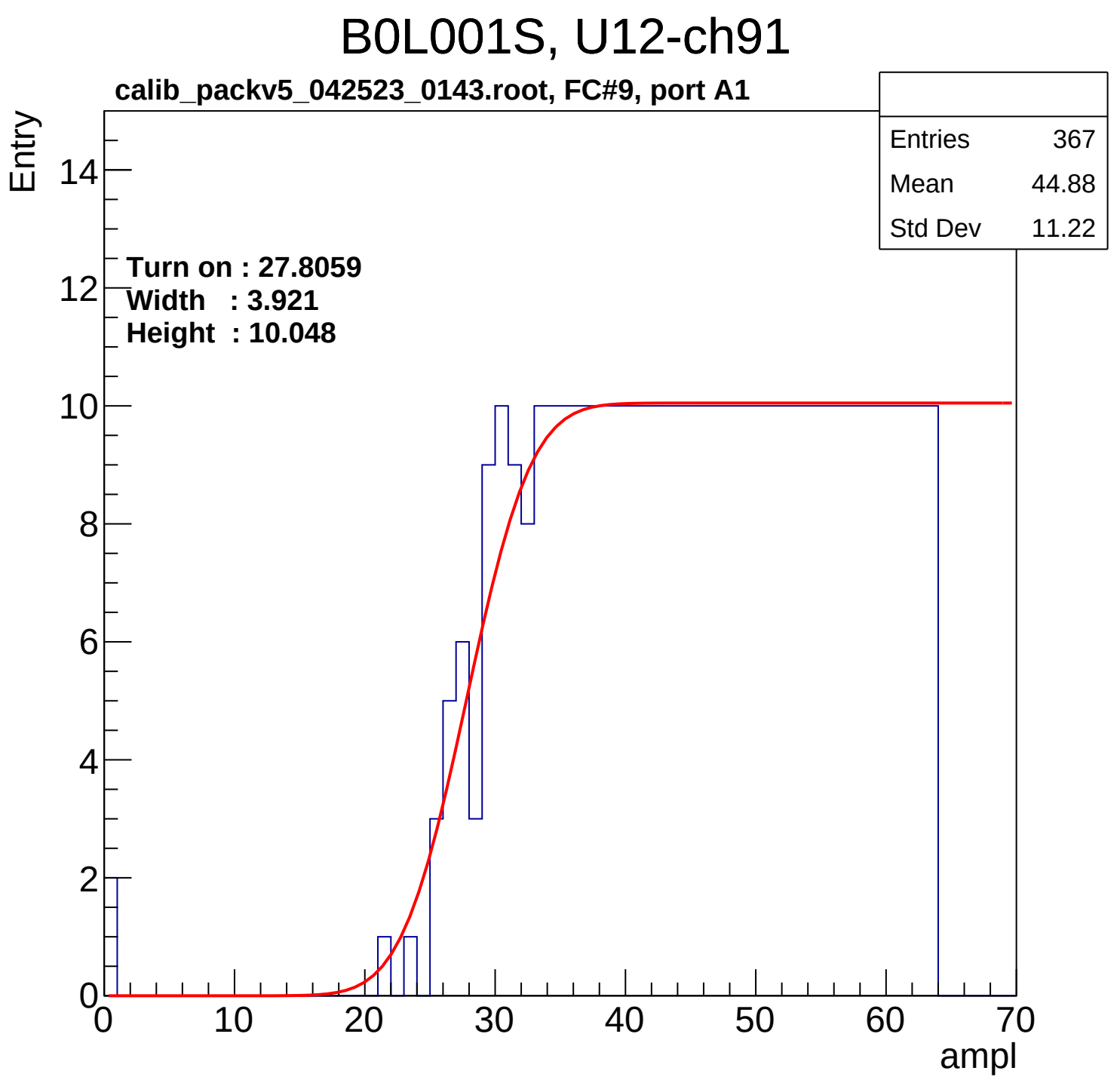
B0L001S, U12-ch91
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.88
Std Dev 11.22
Turn on : 27.8059
Width : 3.921
Height : 10.048
Entry
ampl
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2
4
6
8
10
12
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0
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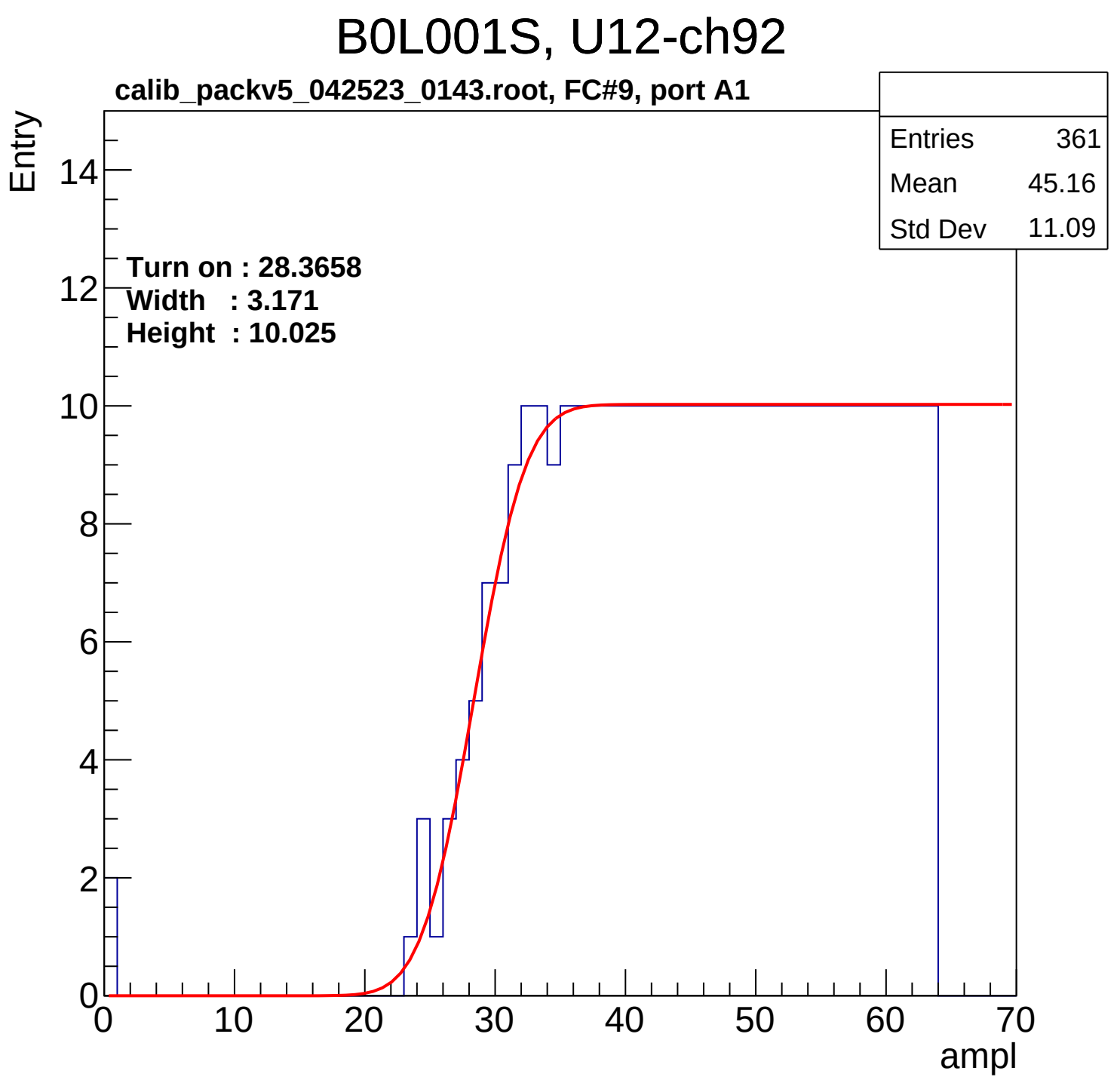
B0L001S, U12-ch92
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 45.16
Std Dev 11.09
Turn on : 28.3658
Width : 3.171
Height : 10.025
Entry
ampl
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2
4
6
8
10
12
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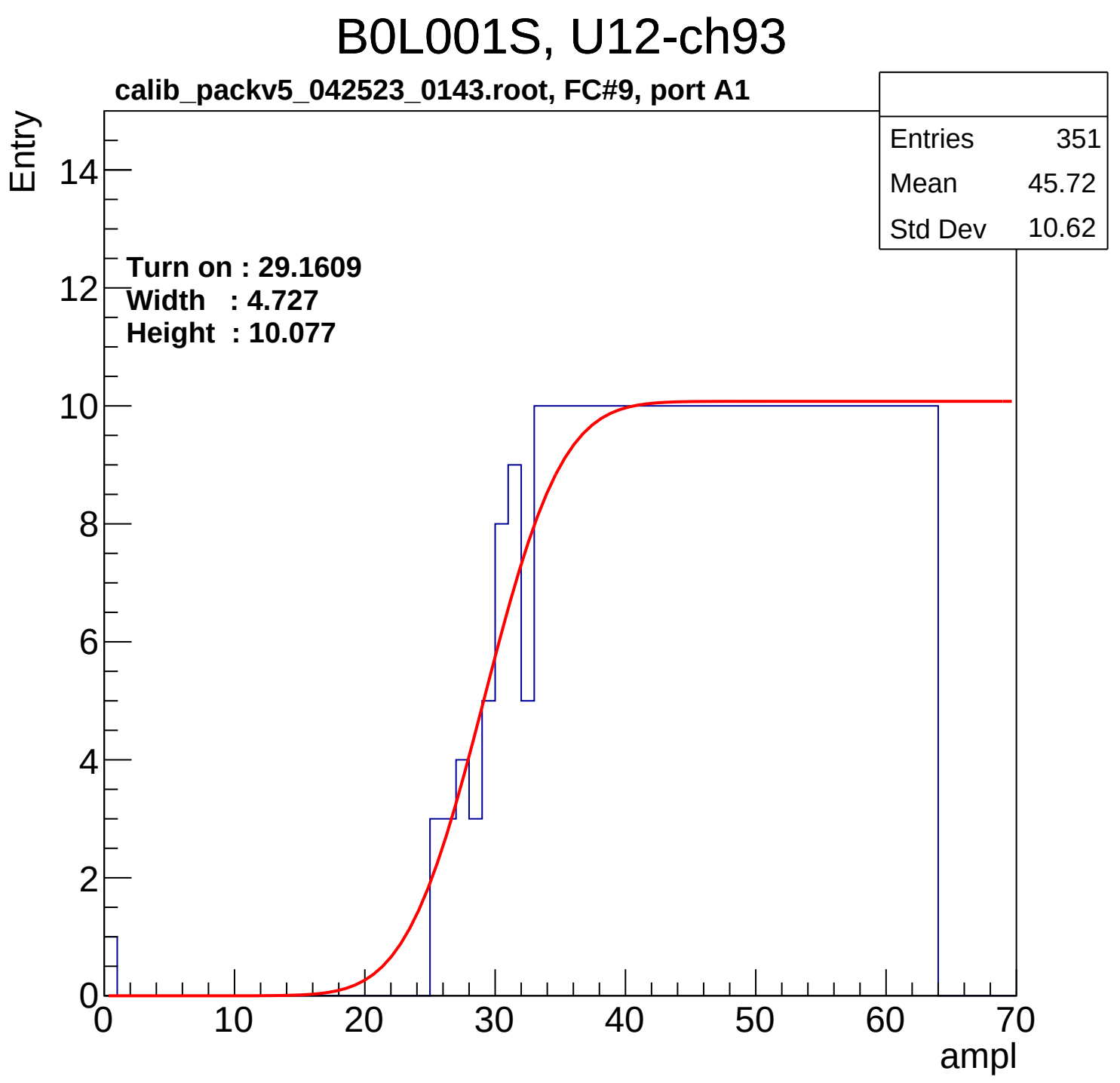
B0L001S, U12-ch93
calib_packv5_042523_0143.root, FC#9, port A1
Entries 351
Mean 45.72
Std Dev 10.62
Turn on : 29.1609
Width : 4.727
Height : 10.077
Entry
ampl
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4
6
8
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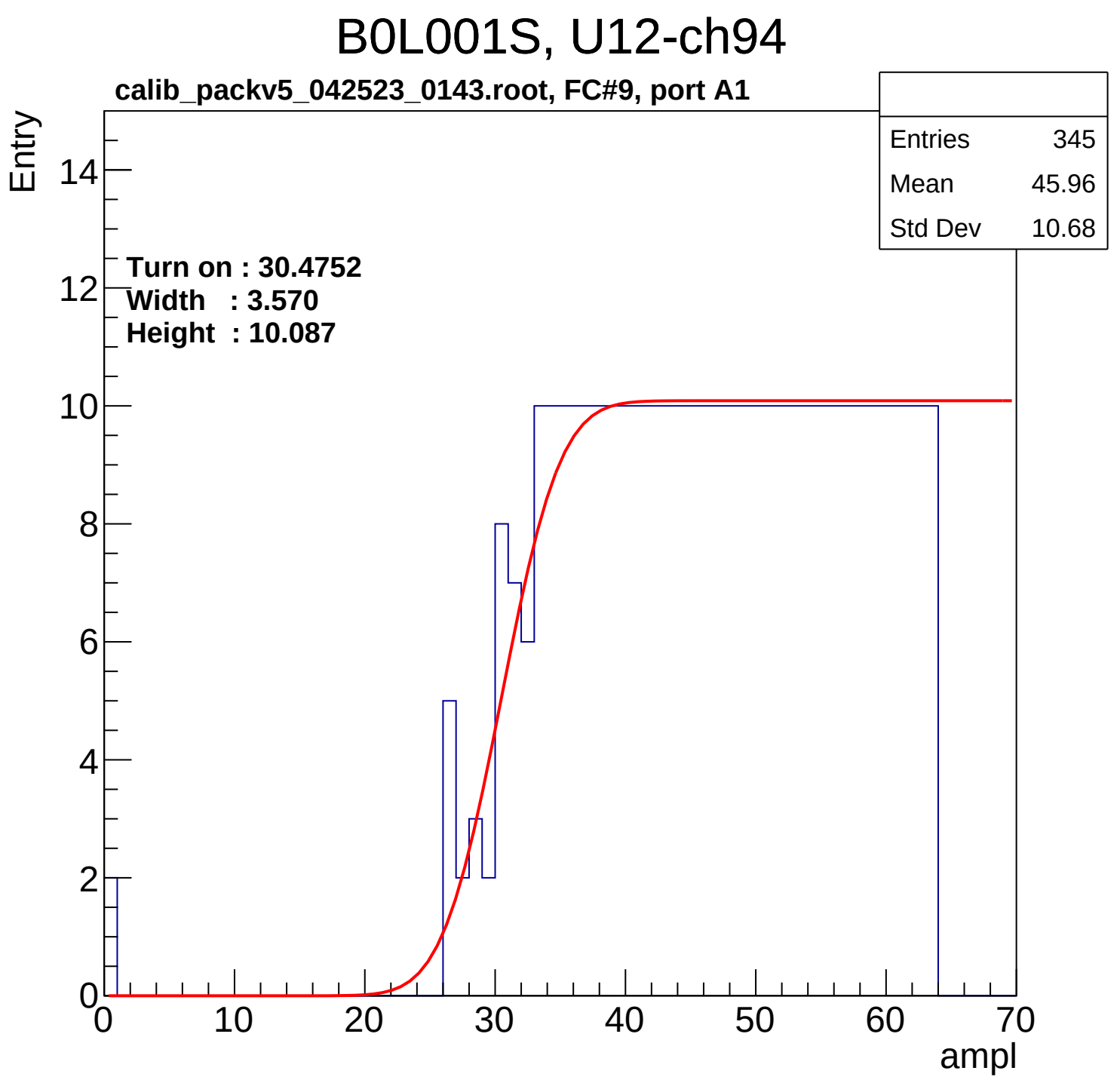
B0L001S, U12-ch94
calib_packv5_042523_0143.root, FC#9, port A1
Entries 345
Mean 45.96
Std Dev 10.68
Turn on : 30.4752
Width : 3.570
Height : 10.087
Entry
ampl
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2
4
6
8
10
12
14
0
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20
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40
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60
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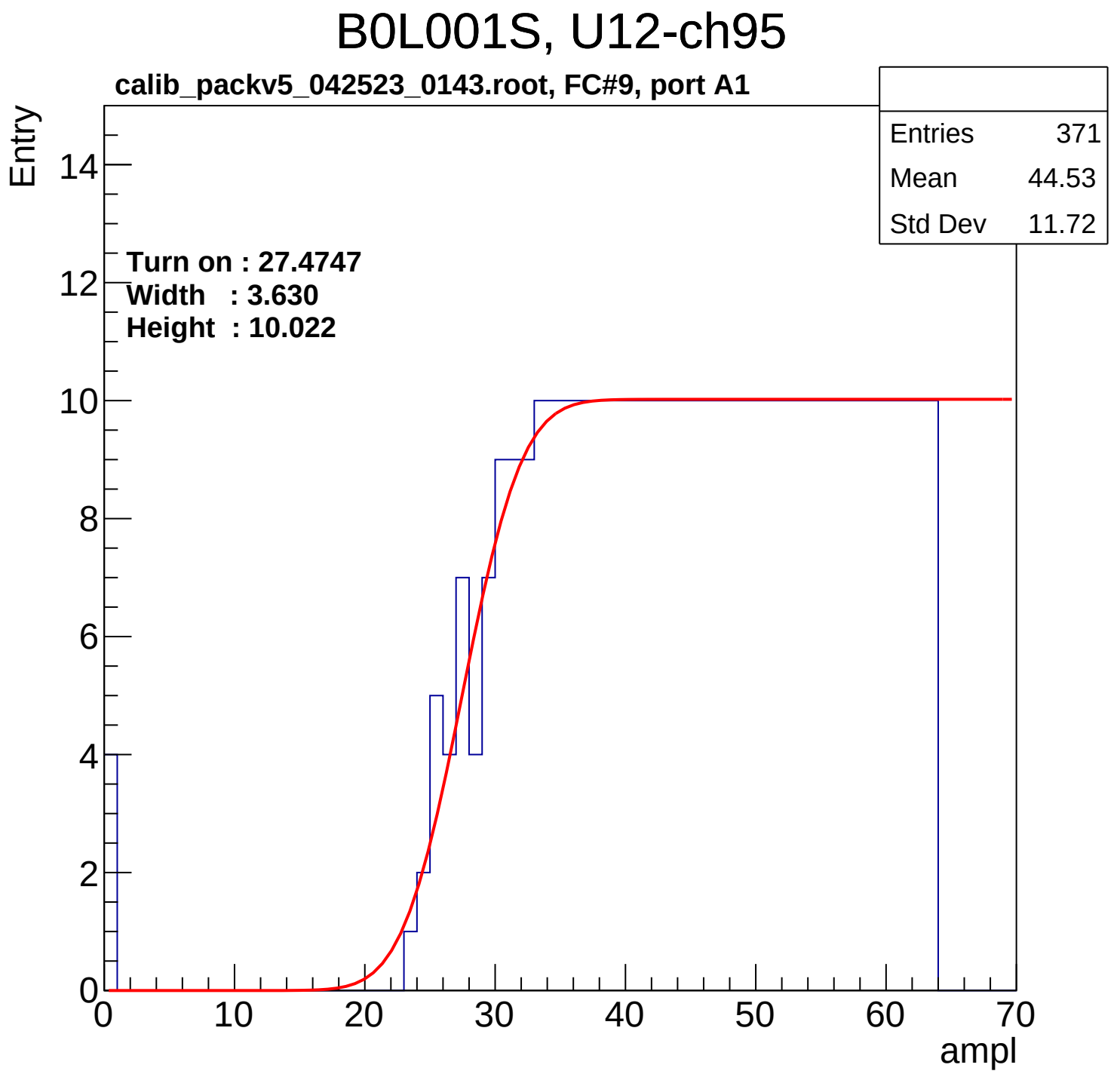
B0L001S, U12-ch95
calib_packv5_042523_0143.root, FC#9, port A1
Entries 371
Mean 44.53
Std Dev 11.72
Turn on : 27.4747
Width : 3.630
Height : 10.022
Entry
ampl
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4
6
8
10
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0
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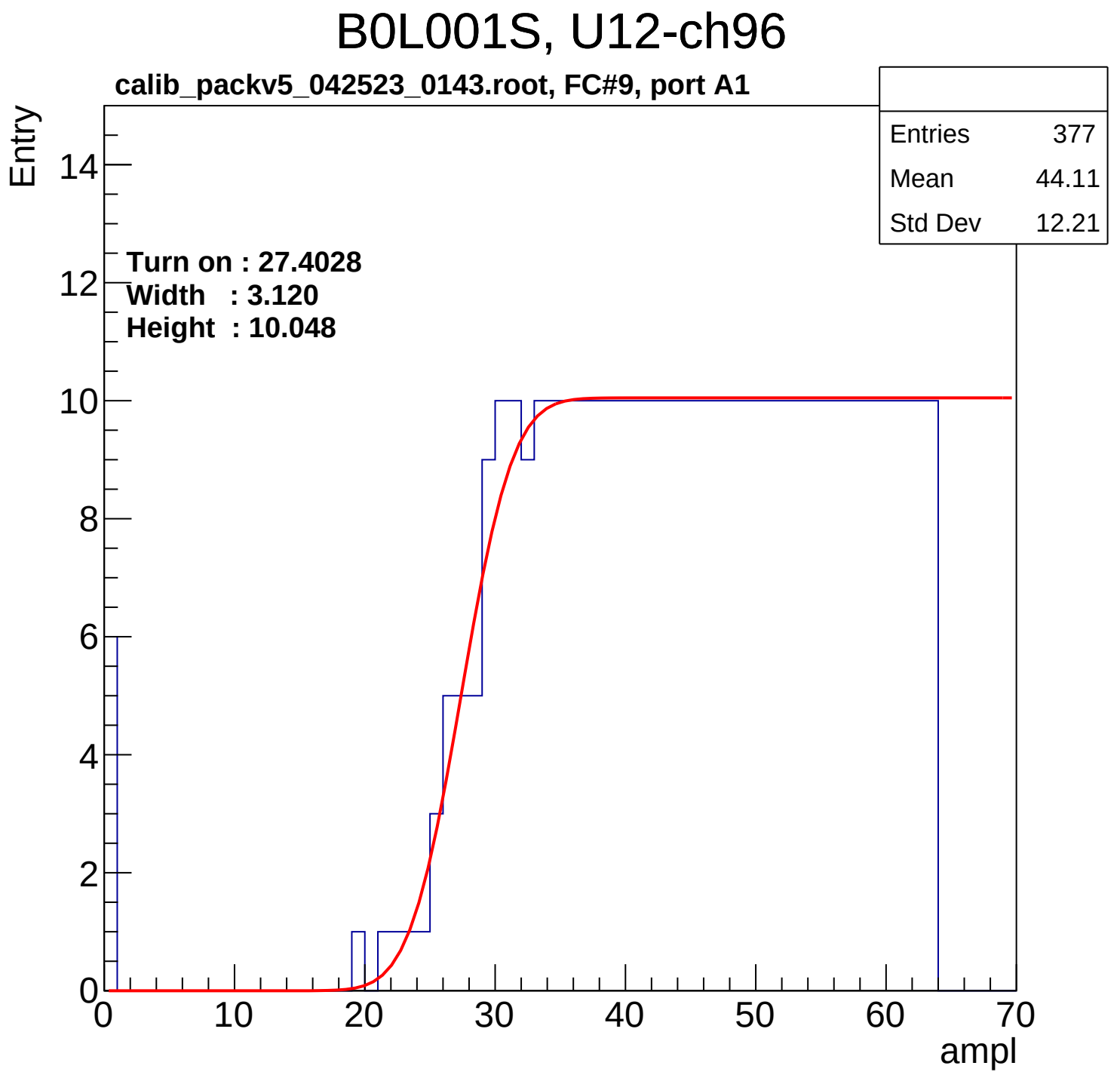
B0L001S, U12-ch96
calib_packv5_042523_0143.root, FC#9, port A1
Entries 377
Mean 44.11
Std Dev 12.21
Turn on : 27.4028
Width : 3.120
Height : 10.048
Entry
ampl
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2
4
6
8
10
12
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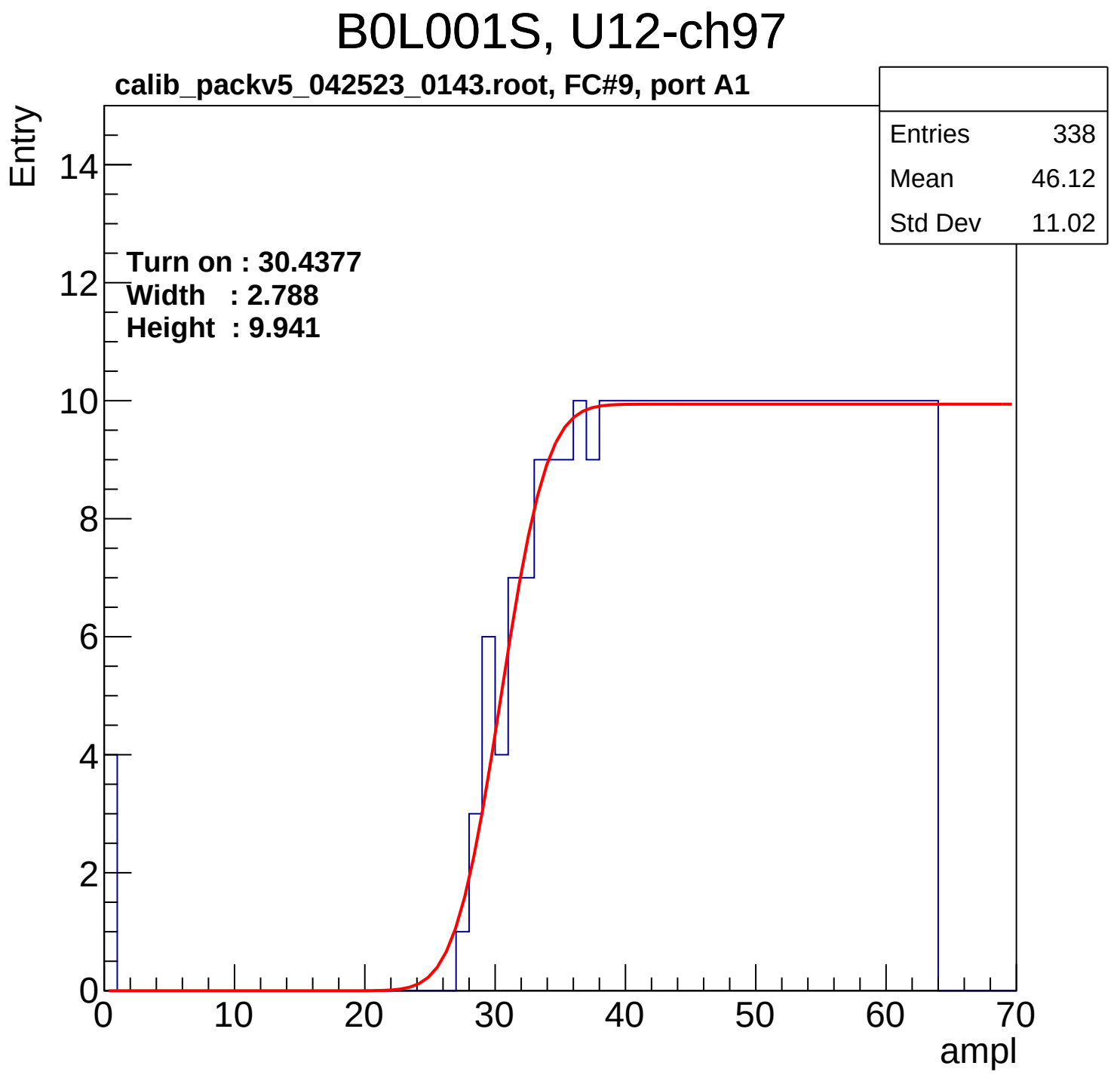
B0L001S, U12-ch97
calib_packv5_042523_0143.root, FC#9, port A1
Entries 338
Mean 46.12
Std Dev 11.02
Turn on : 30.4377
Width : 2.788
Height : 9.941
Entry
ampl
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2
4
6
8
10
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0
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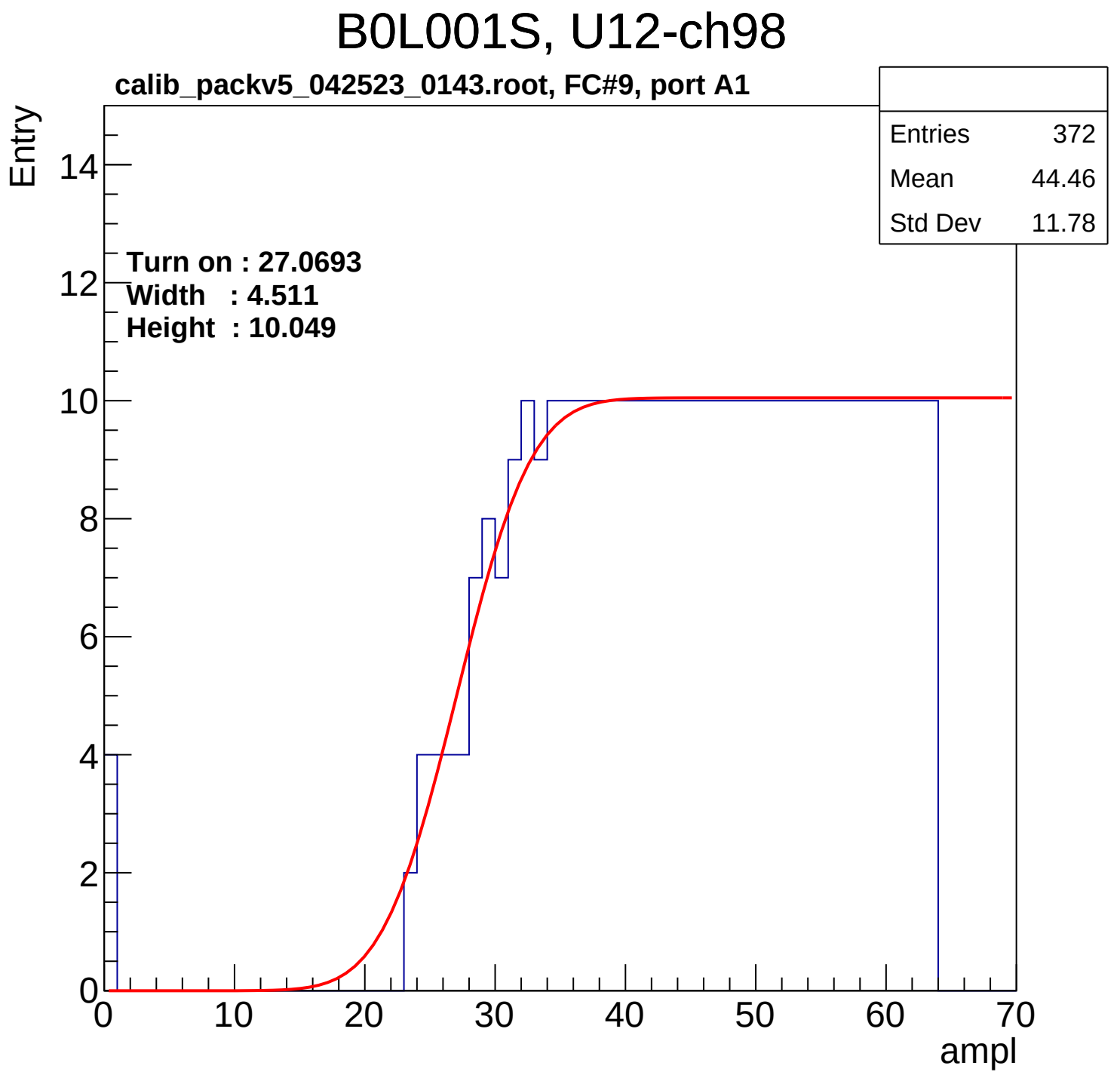
B0L001S, U12-ch98
calib_packv5_042523_0143.root, FC#9, port A1
Entries 372
Mean 44.46
Std Dev 11.78
Turn on : 27.0693
Width : 4.511
Height : 10.049
Entry
ampl
0
2
4
6
8
10
12
14
0
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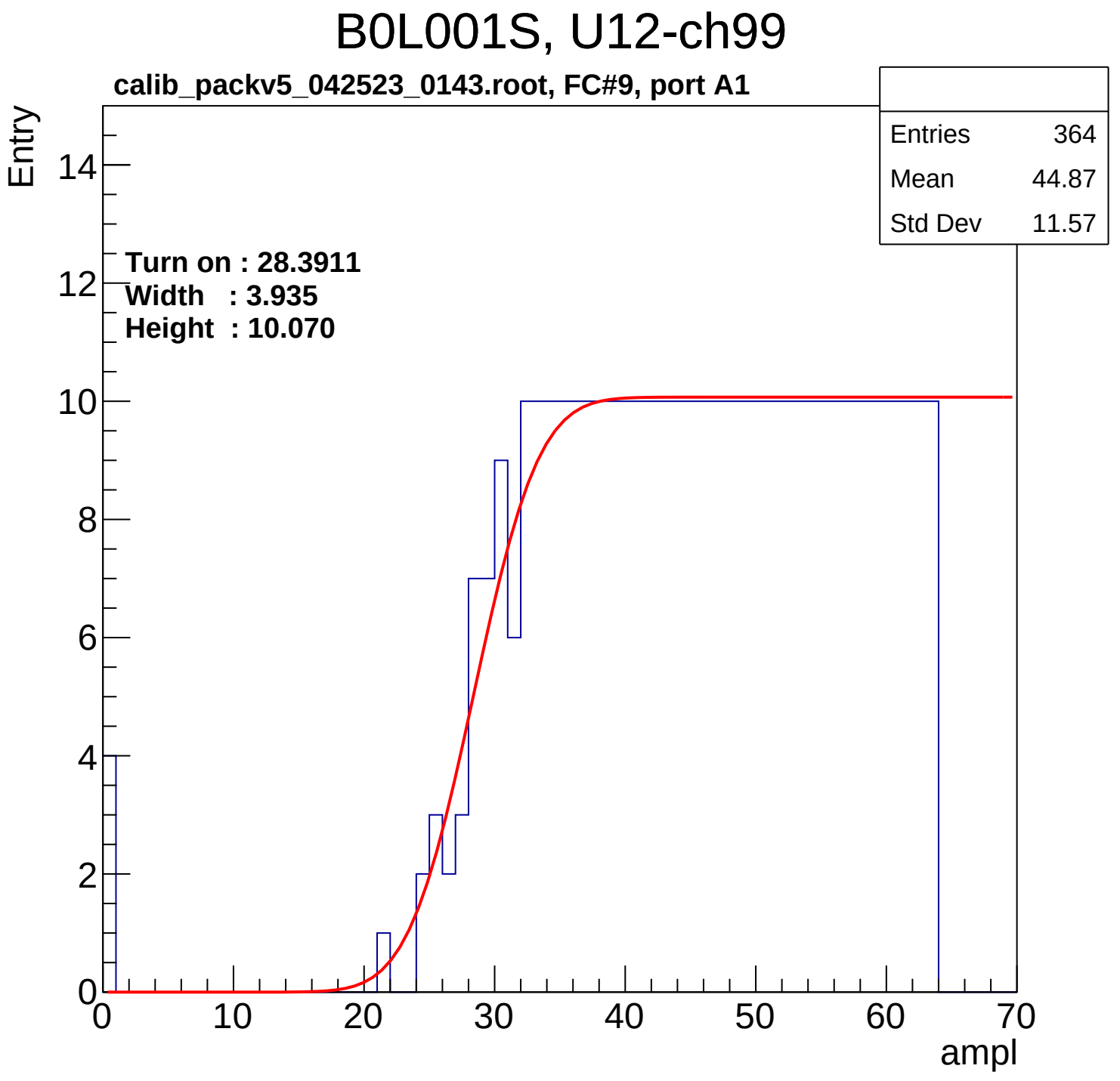
B0L001S, U12-ch99
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 44.87
Std Dev 11.57
Turn on : 28.3911
Width : 3.935
Height : 10.070
Entry
ampl
0
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4
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8
10
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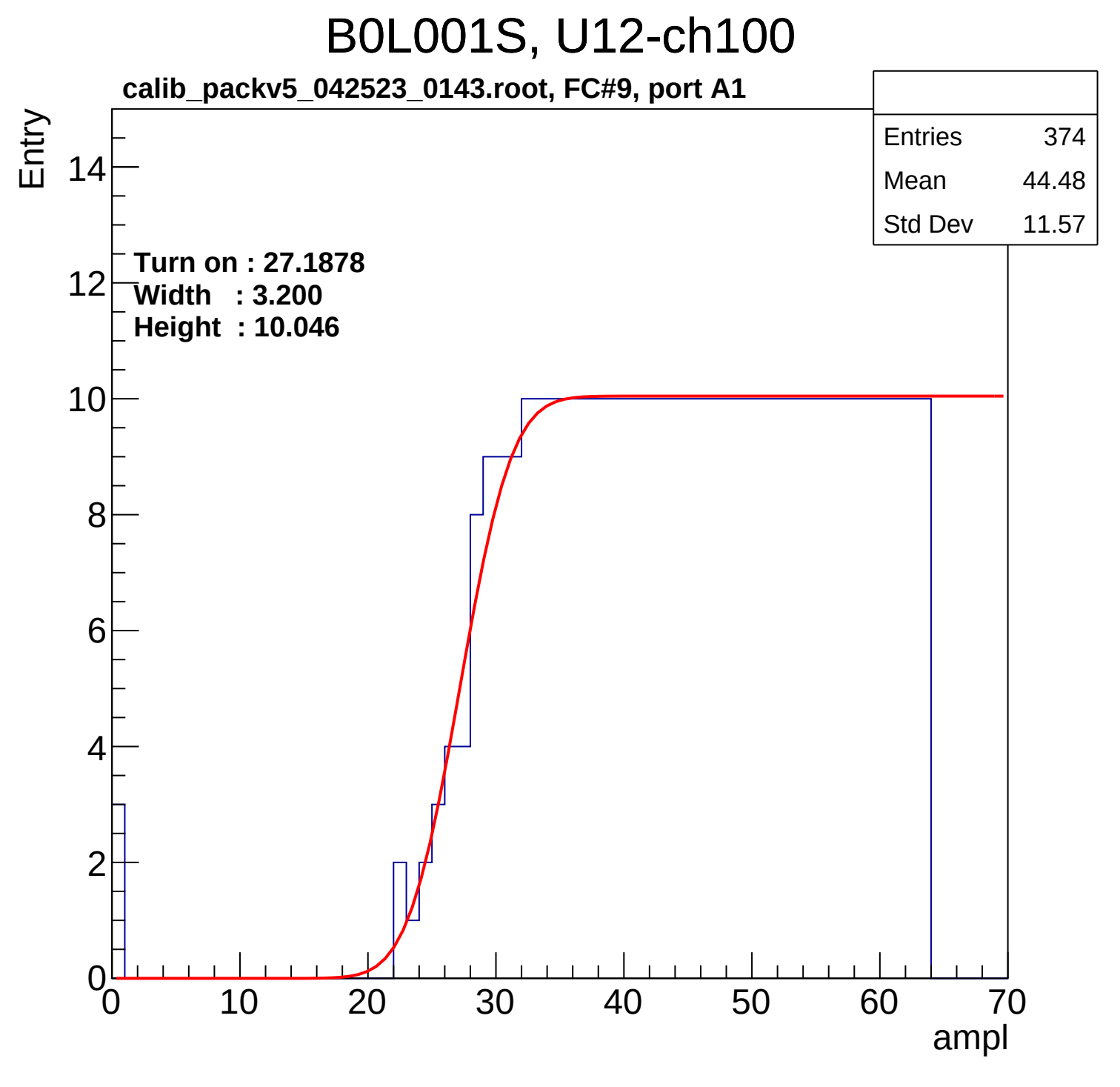
B0L001S, U12-ch100
calib_packv5_042523_0143.root, FC#9, port A1
Entries 374
Mean 44.48
Std Dev 11.57
Turn on : 27.1878
Width : 3.200
Height : 10.046
Entry
ampl
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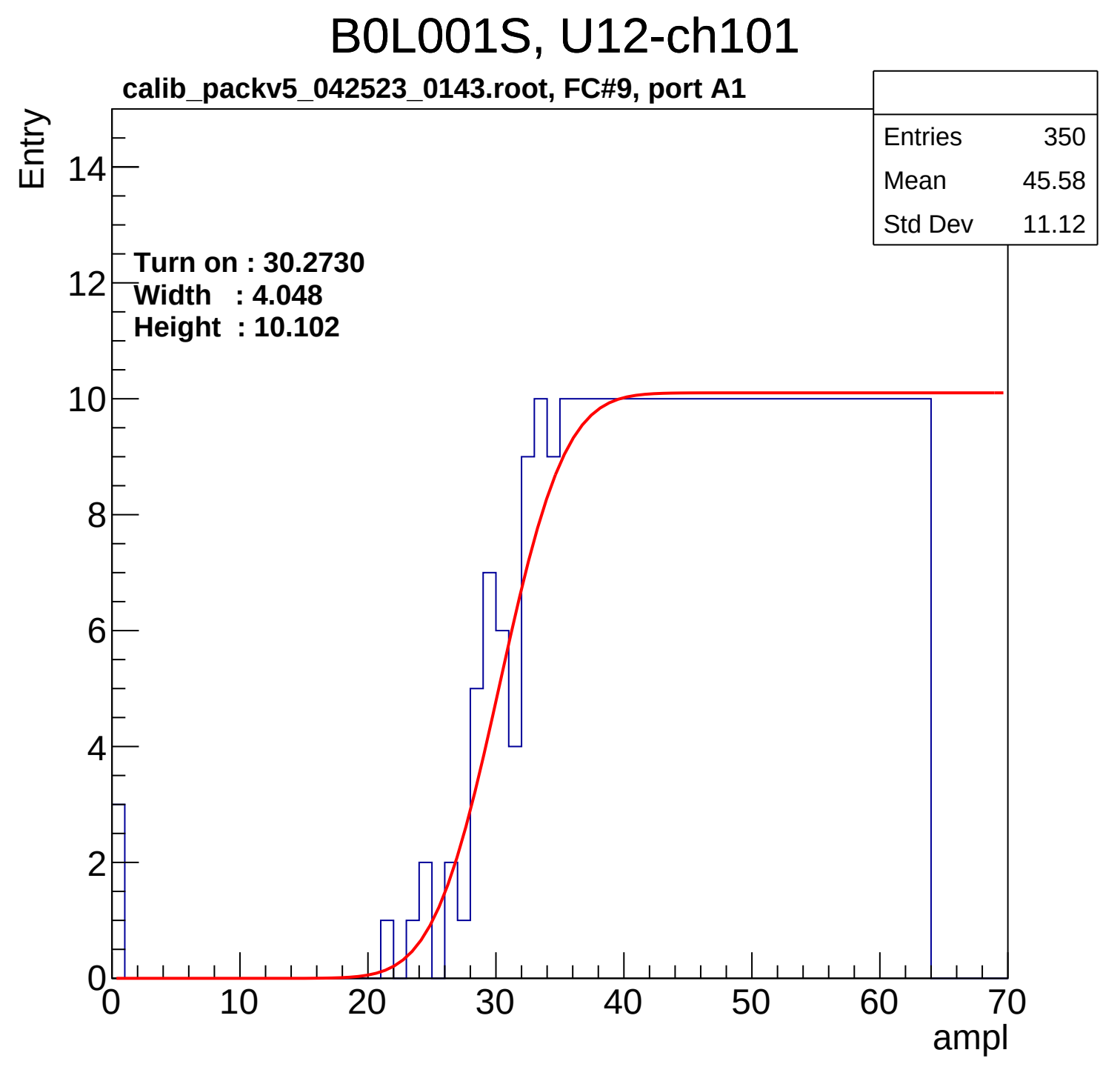
B0L001S, U12-ch101
calib_packv5_042523_0143.root, FC#9, port A1
Entries 350
Mean 45.58
Std Dev 11.12
Turn on : 30.2730
Width : 4.048
Height : 10.102
Entry
ampl
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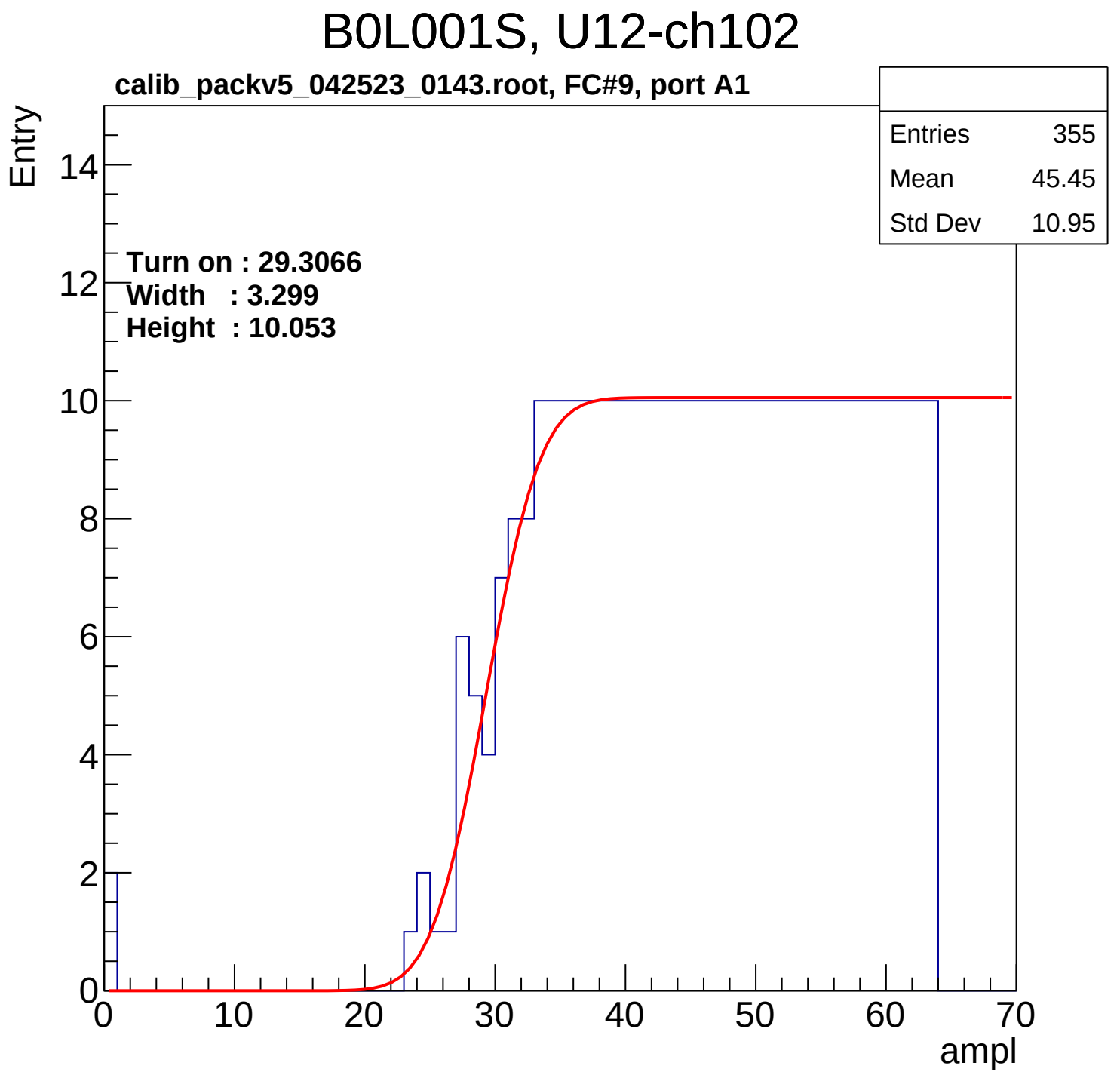
B0L001S, U12-ch102
calib_packv5_042523_0143.root, FC#9, port A1
Entries 355
Mean 45.45
Std Dev 10.95
Turn on : 29.3066
Width : 3.299
Height : 10.053
Entry
ampl
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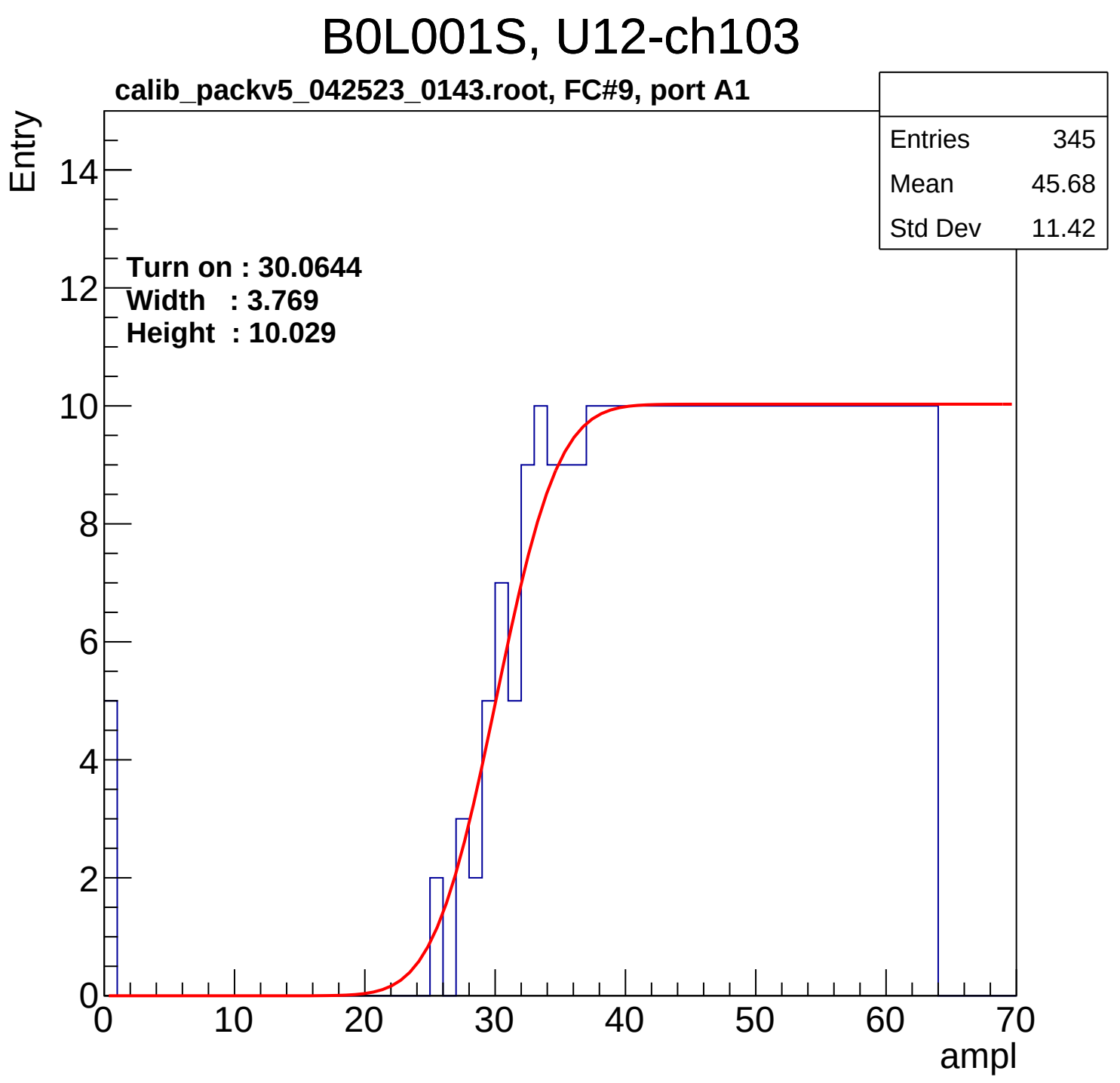
B0L001S, U12-ch103
calib_packv5_042523_0143.root, FC#9, port A1
Entries 345
Mean 45.68
Std Dev 11.42
Turn on : 30.0644
Width : 3.769
Height : 10.029
Entry
ampl
0
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6
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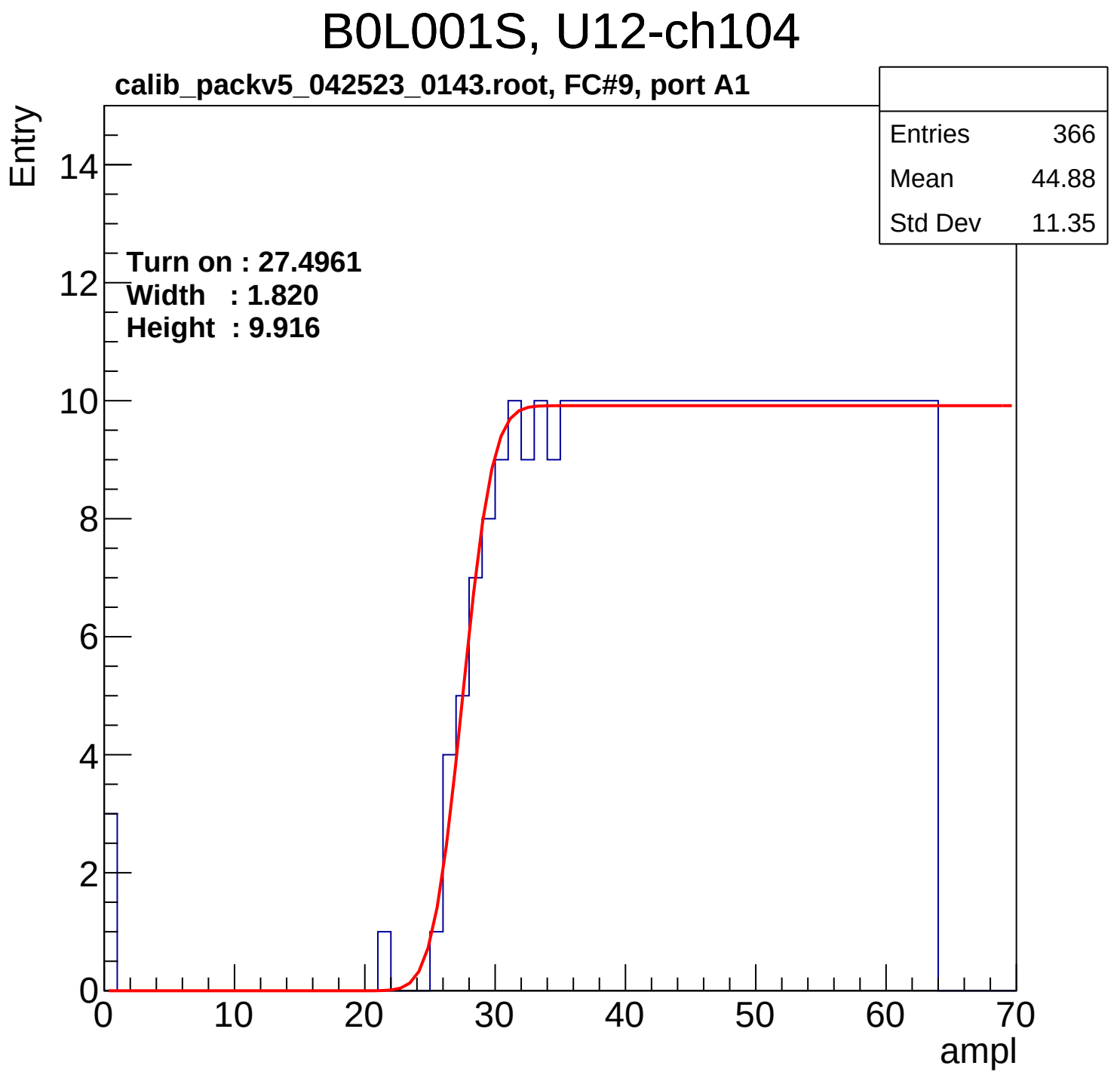
B0L001S, U12-ch104
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.88
Std Dev 11.35
Turn on : 27.4961
Width : 1.820
Height : 9.916
Entry
ampl
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8
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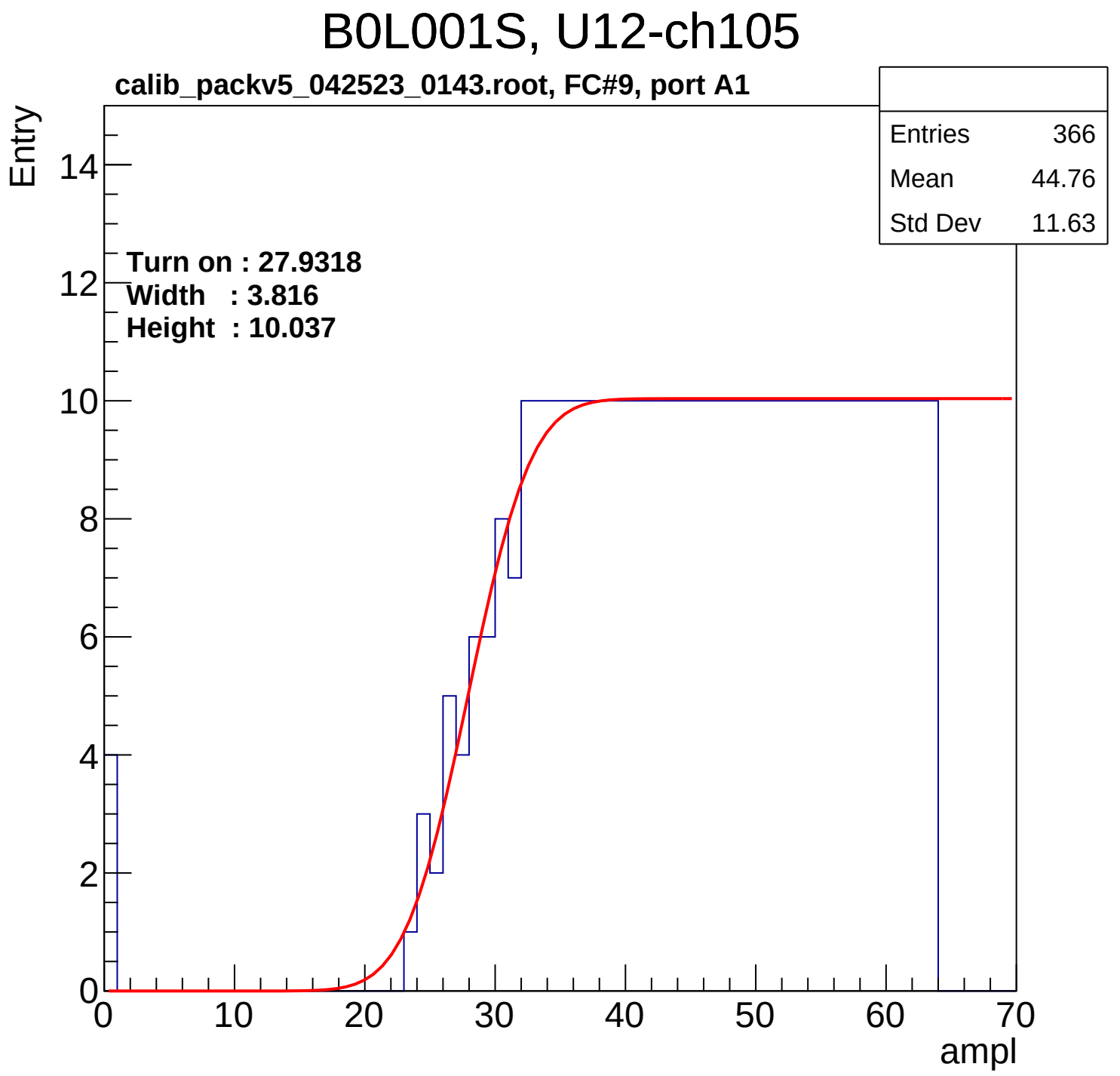
B0L001S, U12-ch105
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.76
Std Dev 11.63
Turn on : 27.9318
Width : 3.816
Height : 10.037
Entry
ampl
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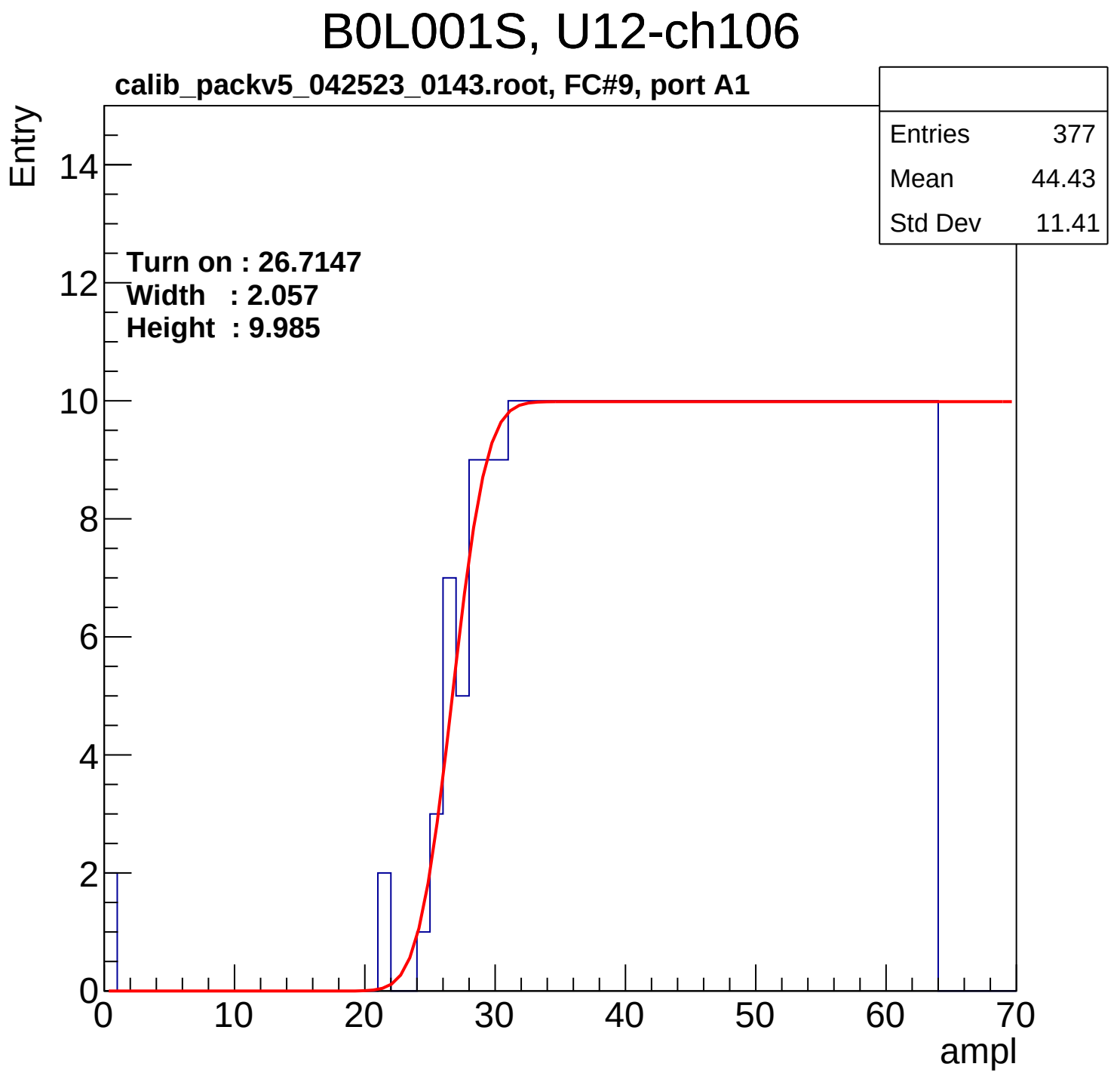
B0L001S, U12-ch106
calib_packv5_042523_0143.root, FC#9, port A1
Entries 377
Mean 44.43
Std Dev 11.41
Turn on : 26.7147
Width : 2.057
Height : 9.985
Entry
ampl
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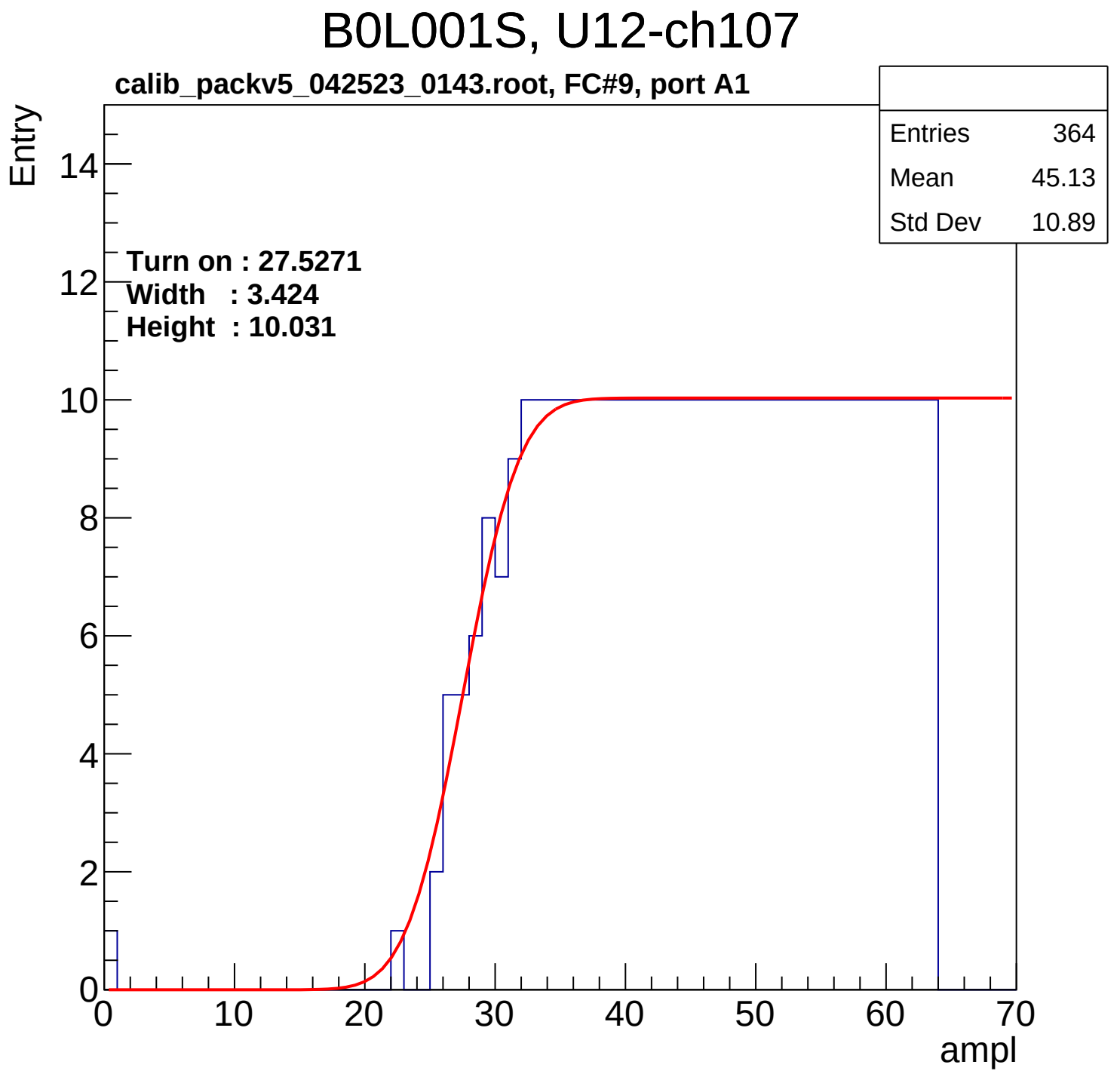
B0L001S, U12-ch107
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 45.13
Std Dev 10.89
Turn on : 27.5271
Width : 3.424
Height : 10.031
Entry
ampl
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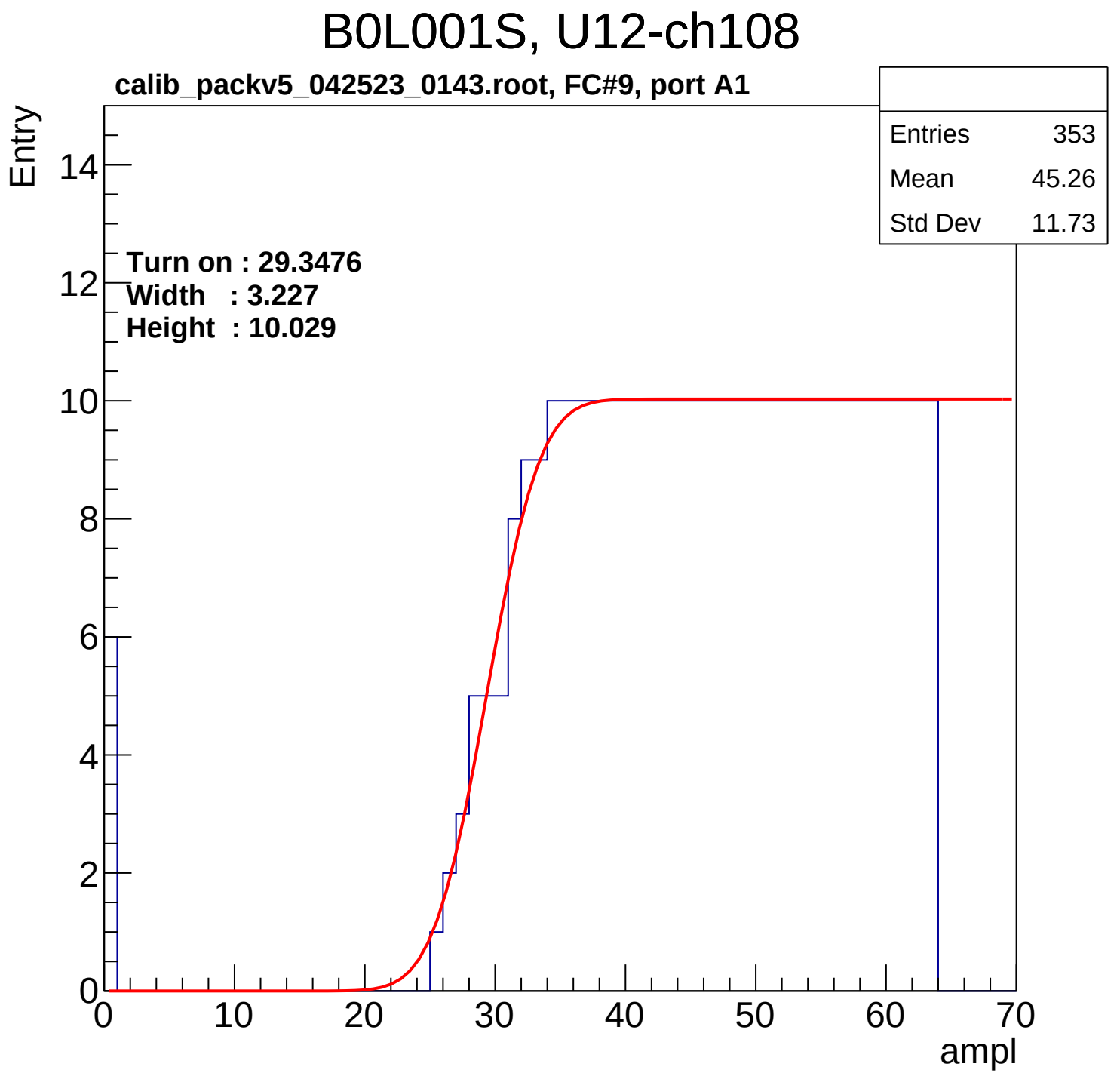
B0L001S, U12-ch108
calib_packv5_042523_0143.root, FC#9, port A1
Entries 353
Mean 45.26
Std Dev 11.73
Turn on : 29.3476
Width : 3.227
Height : 10.029
Entry
ampl
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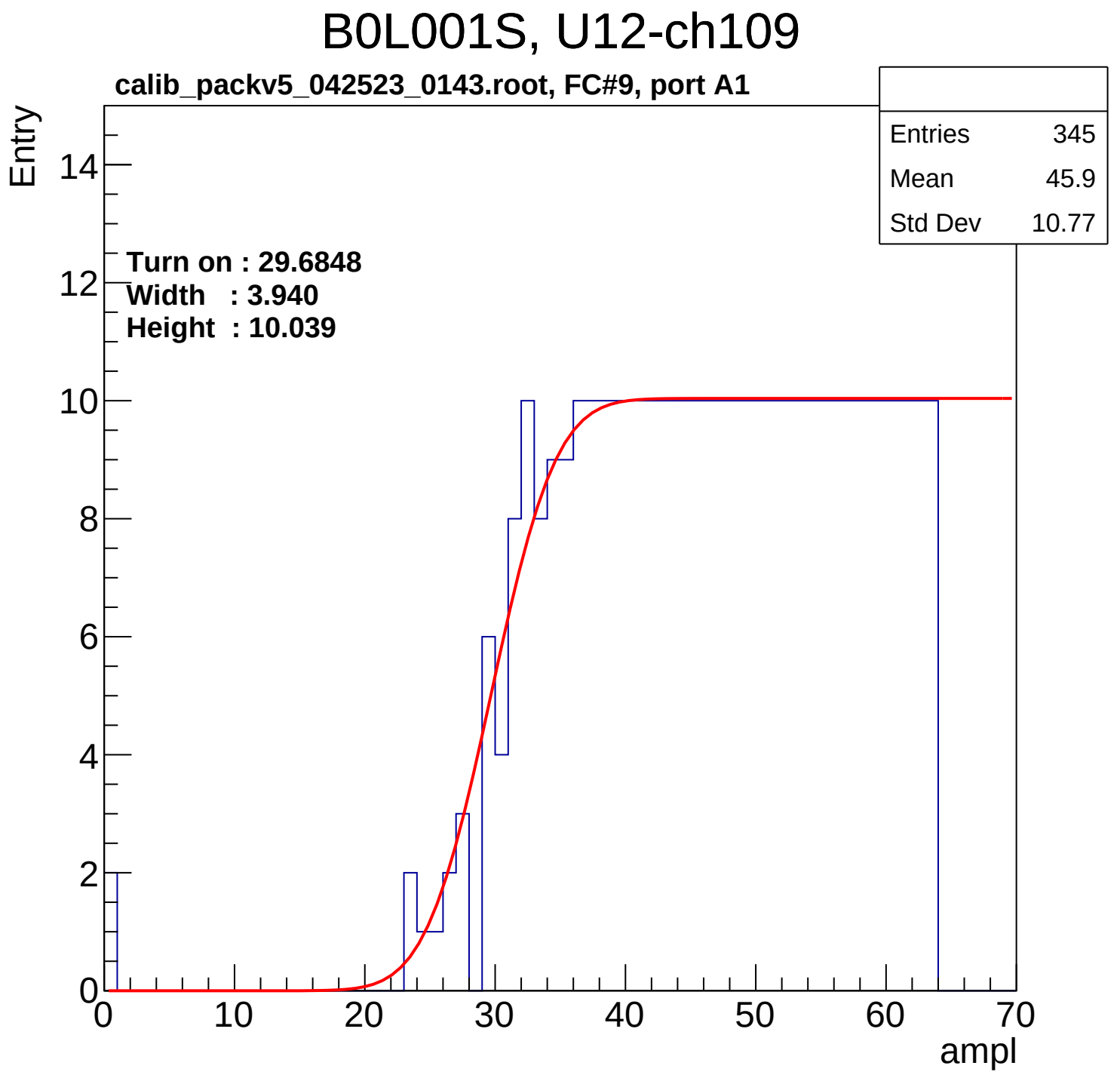
B0L001S, U12-ch109
calib_packv5_042523_0143.root, FC#9, port A1
Entries 345
Mean 45.9
Std Dev 10.77
Turn on : 29.6848
Width : 3.940
Height : 10.039
Entry
ampl
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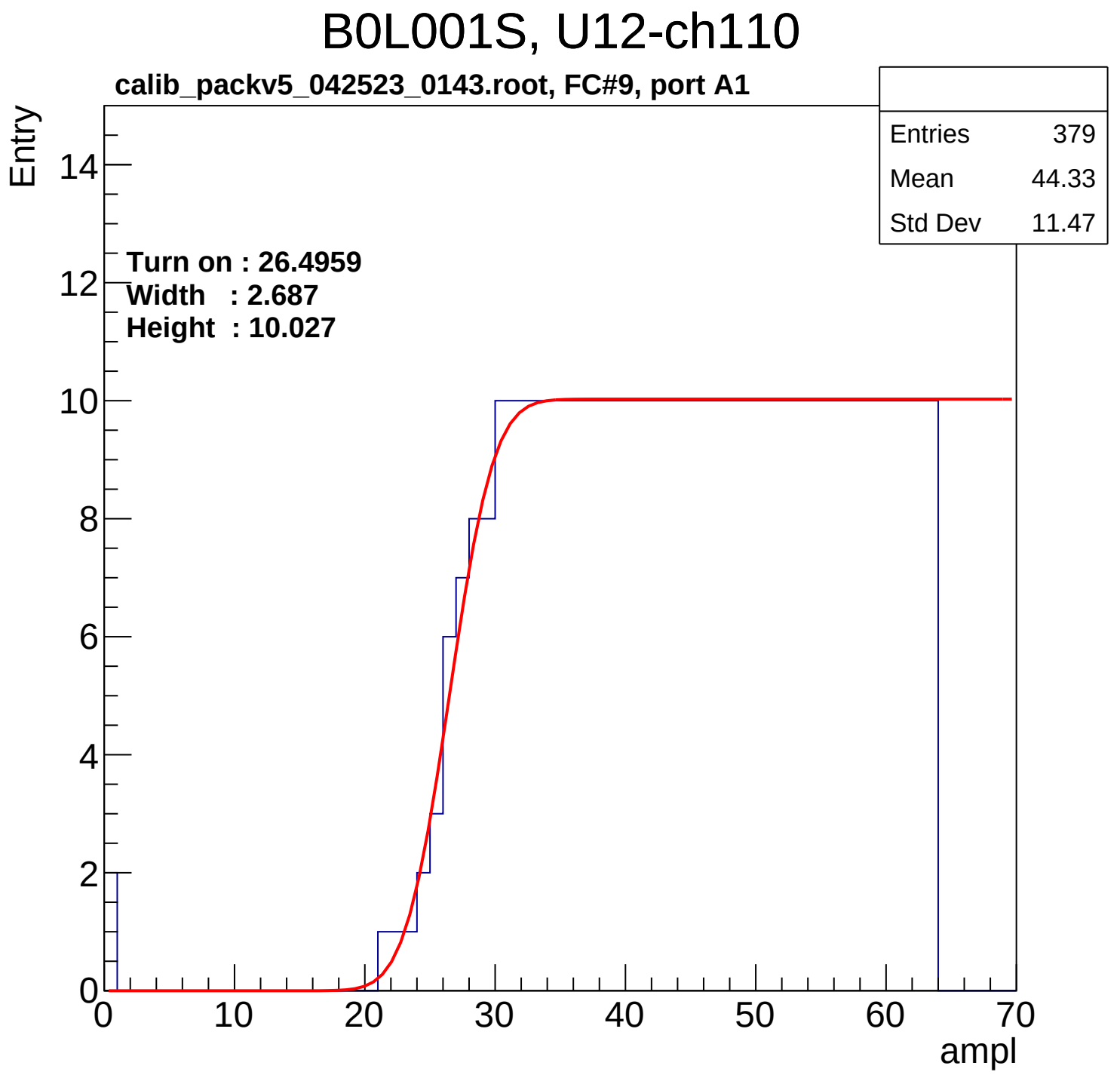
B0L001S, U12-ch110
calib_packv5_042523_0143.root, FC#9, port A1
Entries 379
Mean 44.33
Std Dev 11.47
Turn on : 26.4959
Width : 2.687
Height : 10.027
Entry
ampl
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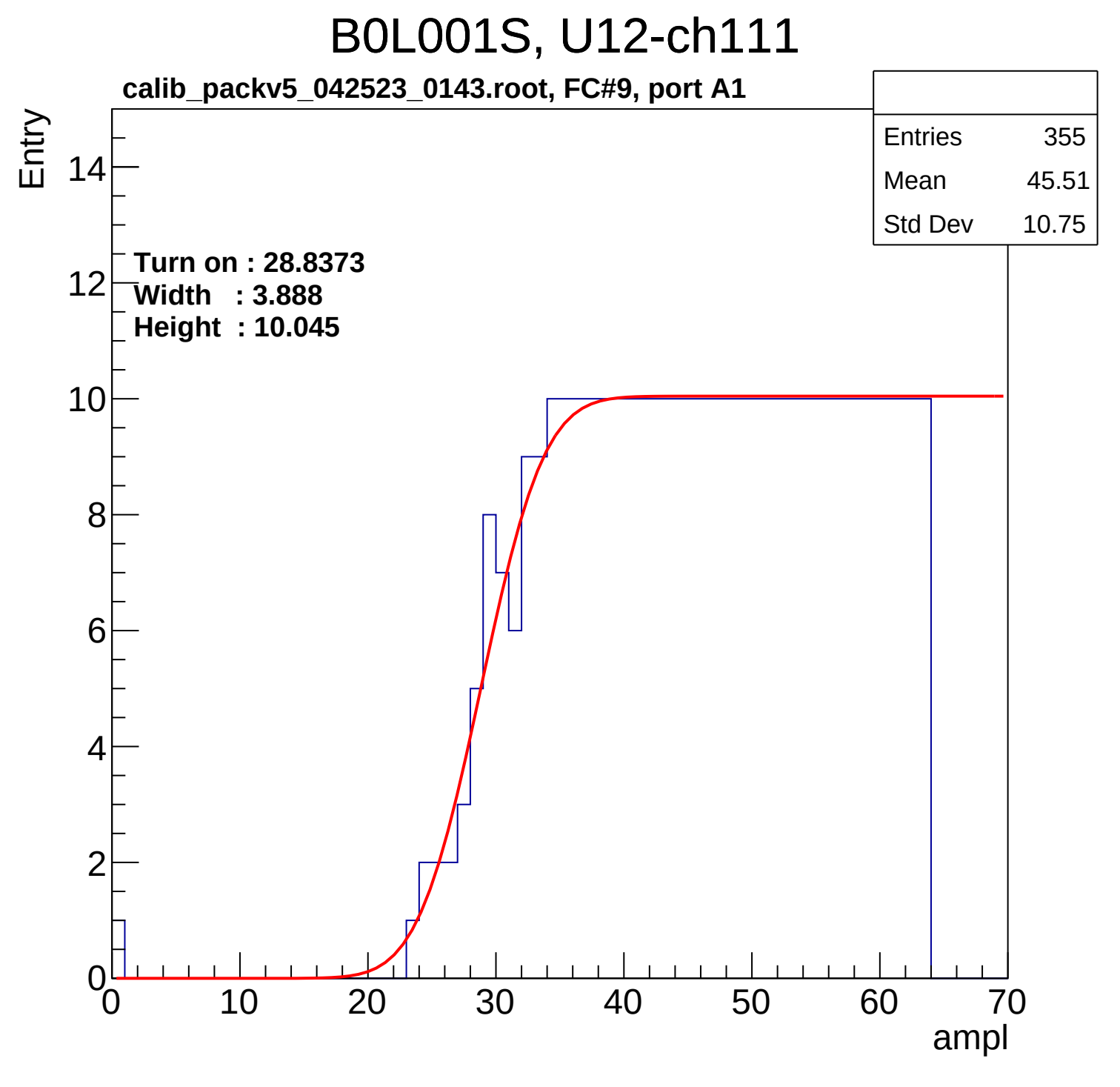
B0L001S, U12-ch111
calib_packv5_042523_0143.root, FC#9, port A1
Entries 355
Mean 45.51
Std Dev 10.75
Turn on : 28.8373
Width : 3.888
Height : 10.045
Entry
ampl
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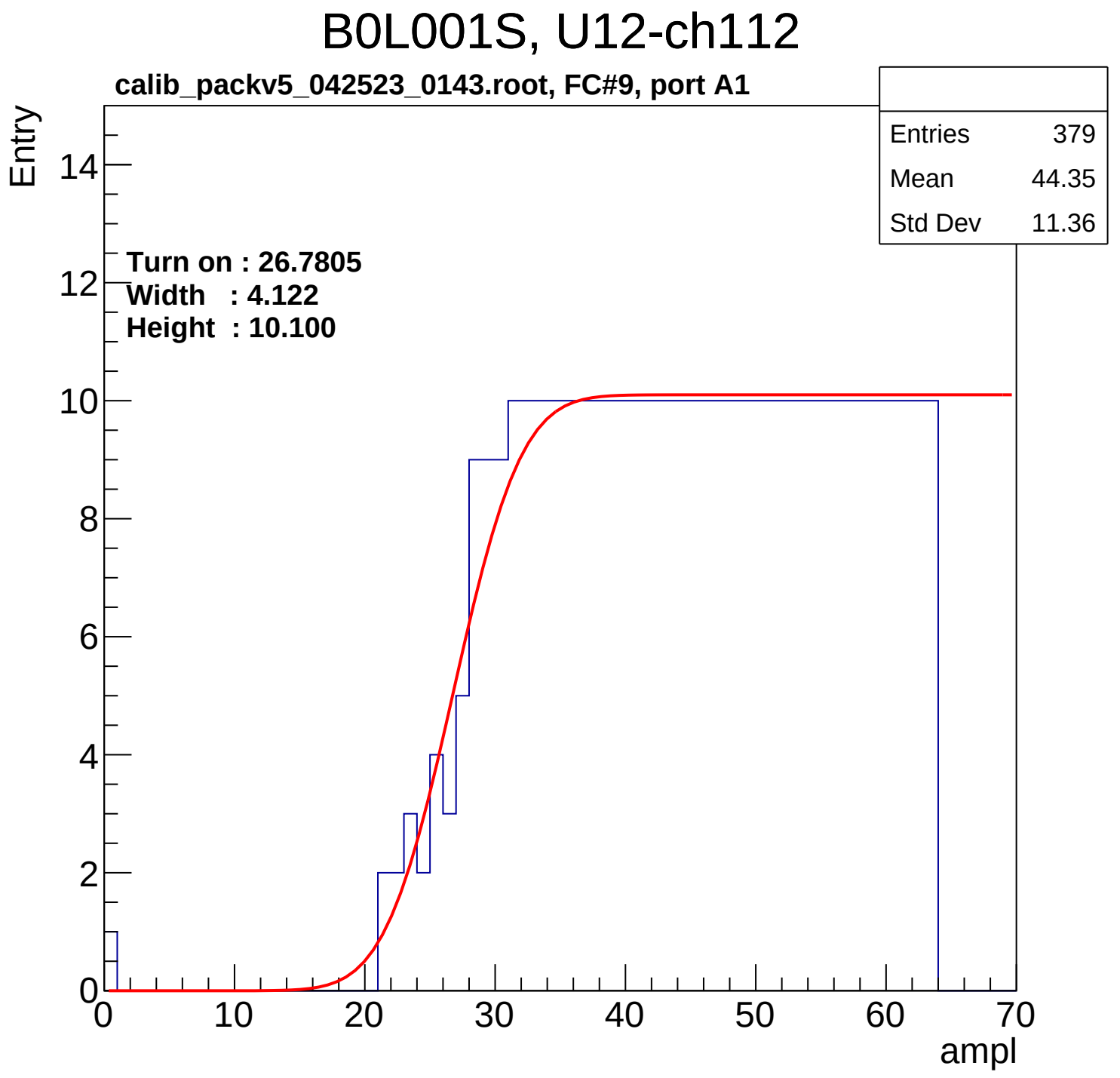
B0L001S, U12-ch112
calib_packv5_042523_0143.root, FC#9, port A1
Entries 379
Mean 44.35
Std Dev 11.36
Turn on : 26.7805
Width : 4.122
Height : 10.100
Entry
ampl
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6
8
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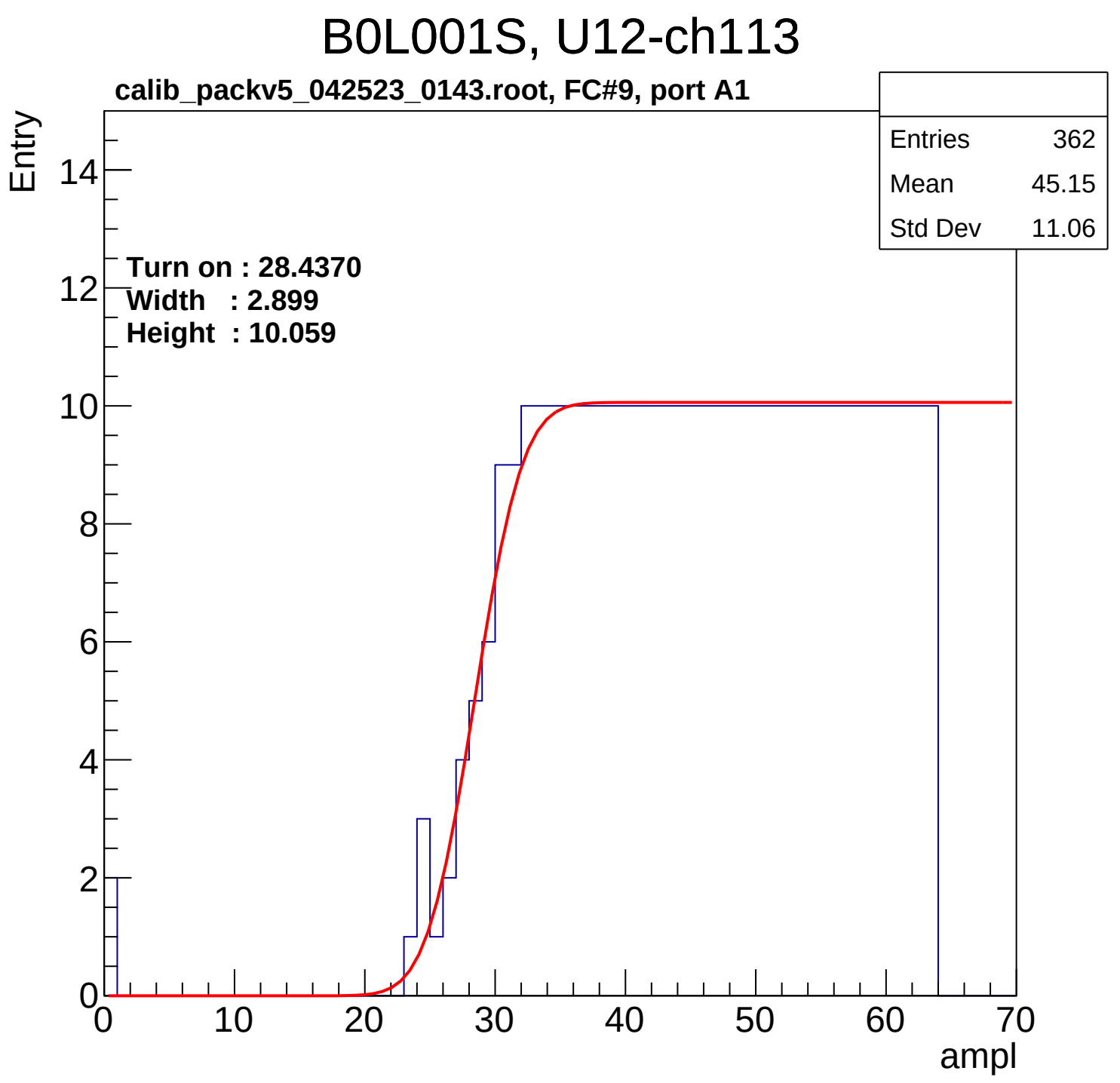
B0L001S, U12-ch113
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 45.15
Std Dev 11.06
Turn on : 28.4370
Width : 2.899
Height : 10.059
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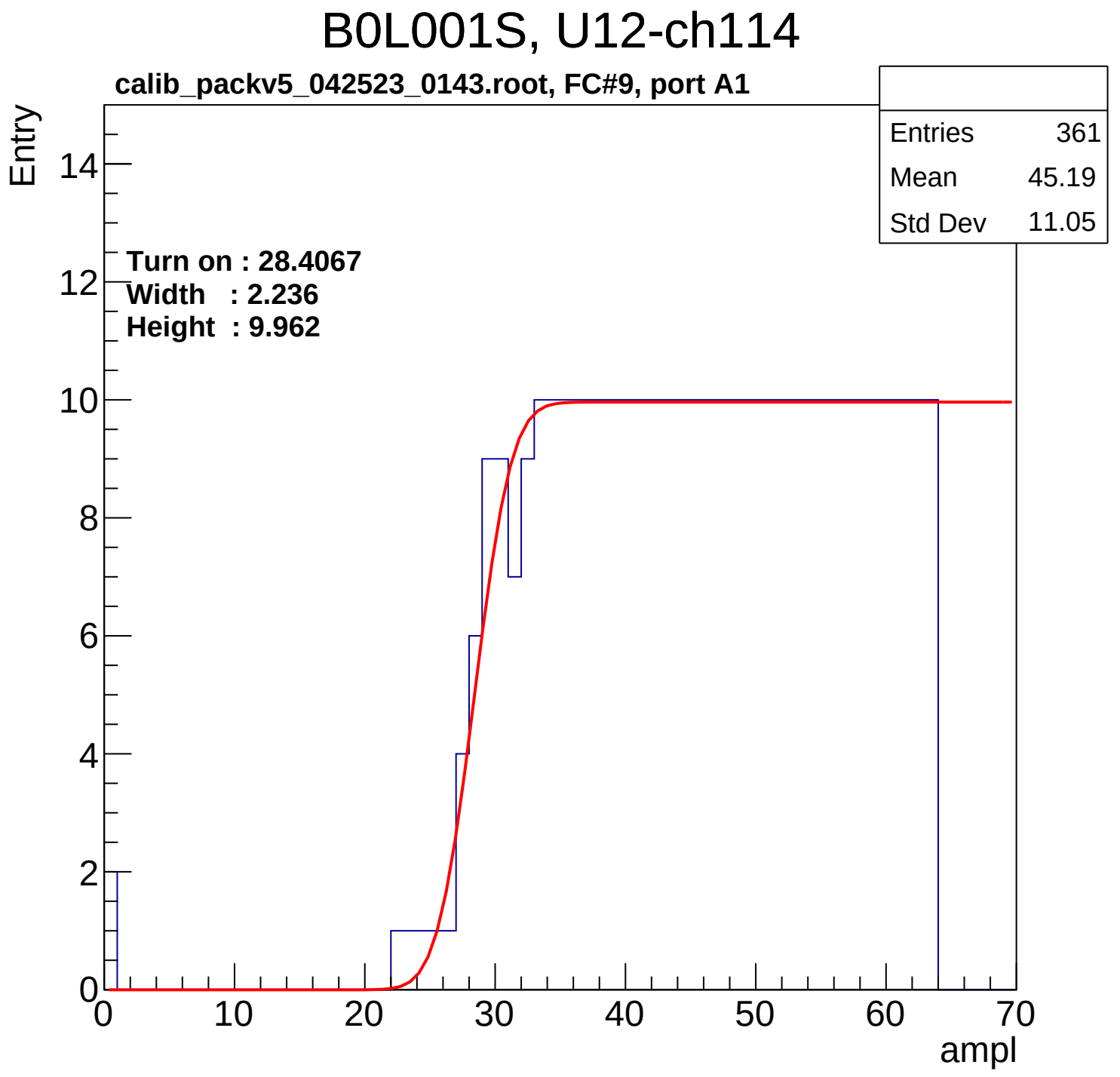
B0L001S, U12-ch114
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 45.19
Std Dev 11.05
Turn on : 28.4067
Width : 2.236
Height : 9.962
Entry
ampl
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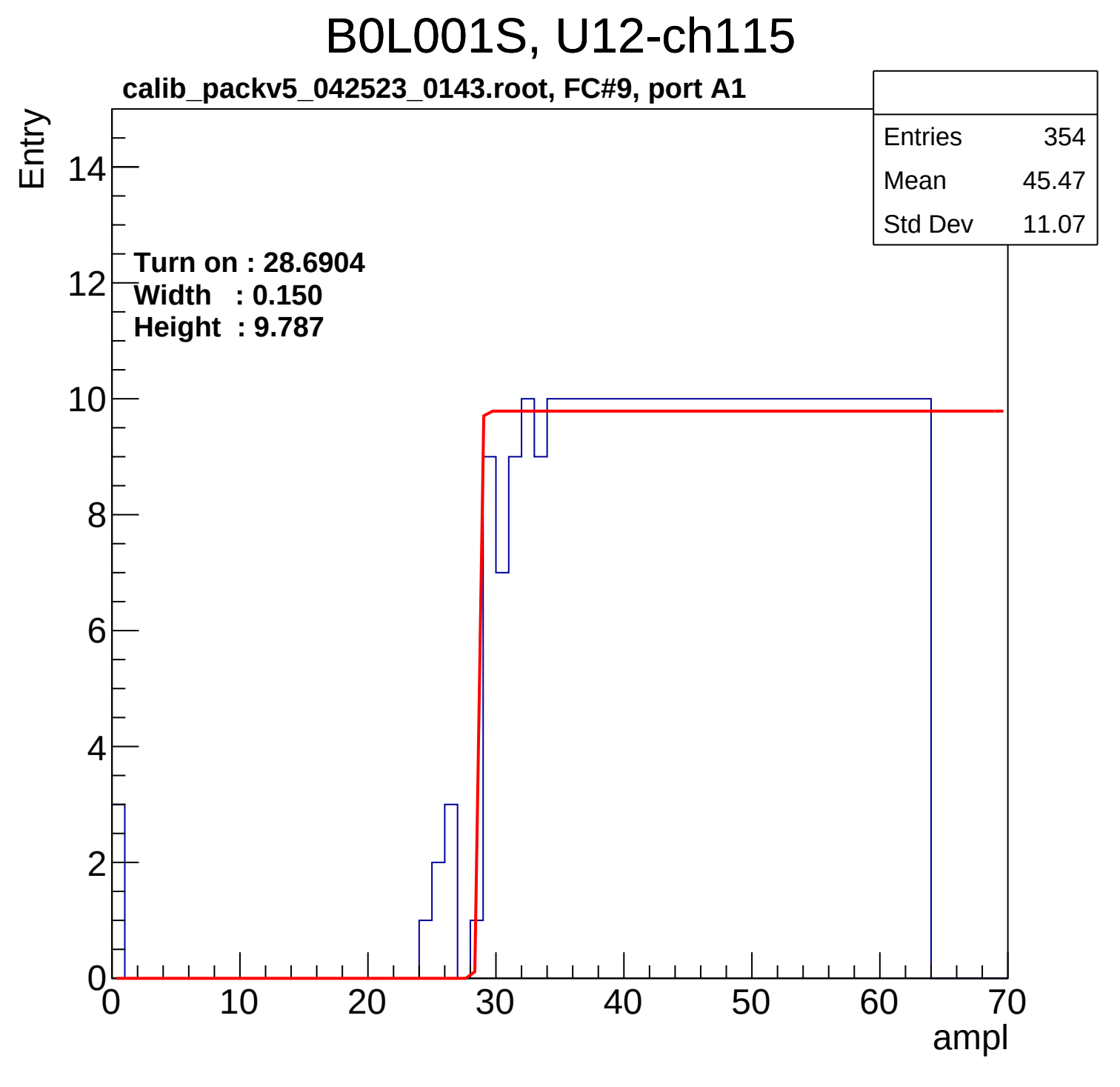
B0L001S, U12-ch115
calib_packv5_042523_0143.root, FC#9, port A1
Entries 354
Mean 45.47
Std Dev 11.07
Turn on : 28.6904
Width : 0.150
Height : 9.787
Entry
ampl
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20
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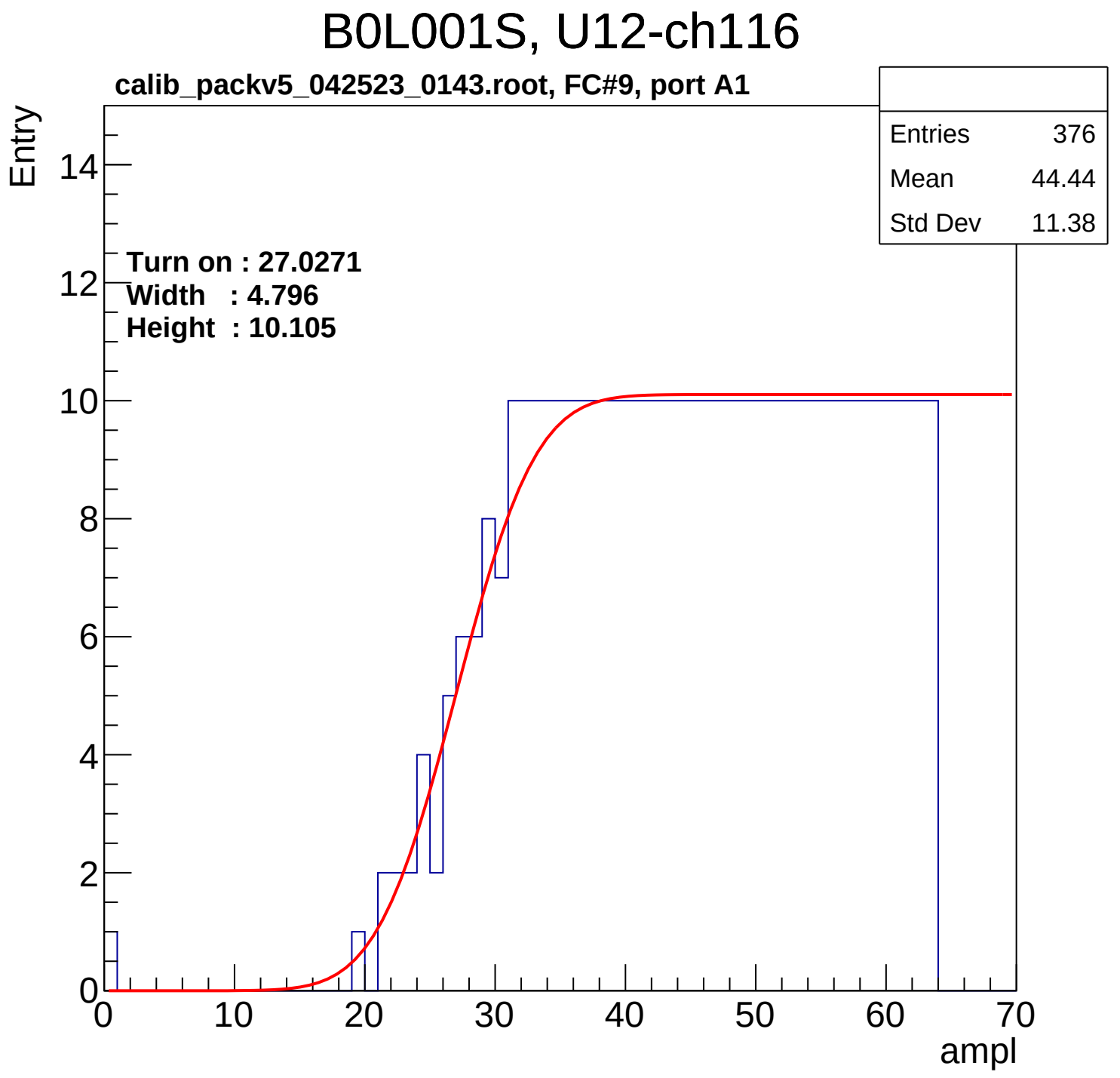
B0L001S, U12-ch116
calib_packv5_042523_0143.root, FC#9, port A1
Entries 376
Mean 44.44
Std Dev 11.38
Turn on : 27.0271
Width : 4.796
Height : 10.105
Entry
ampl
0
2
4
6
8
10
12
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0
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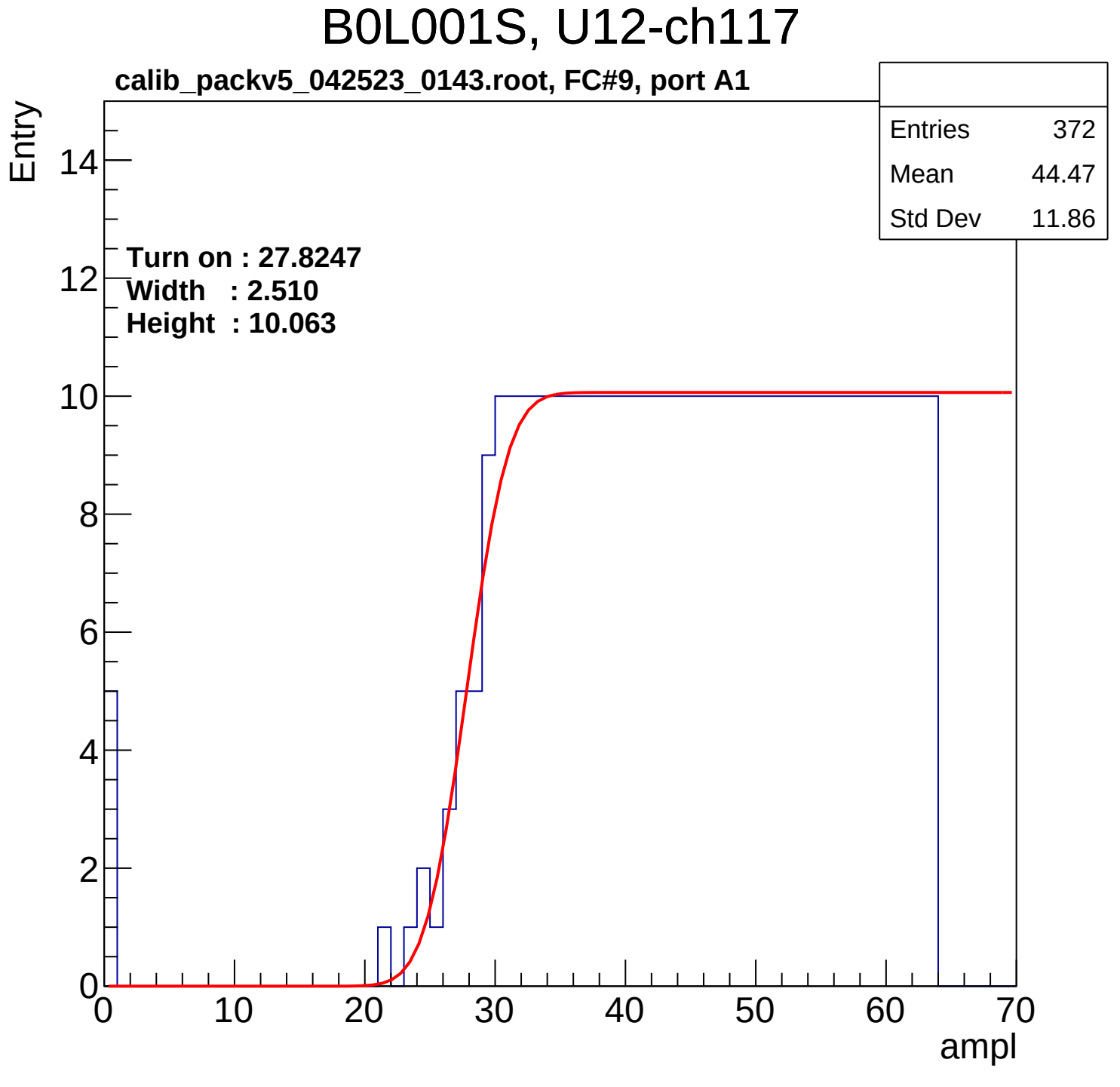
B0L001S, U12-ch117
calib_packv5_042523_0143.root, FC#9, port A1
Entries 372
Mean 44.47
Std Dev 11.86
Turn on : 27.8247
Width : 2.510
Height : 10.063
Entry
ampl
0
2
4
6
8
10
12
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0
10
20
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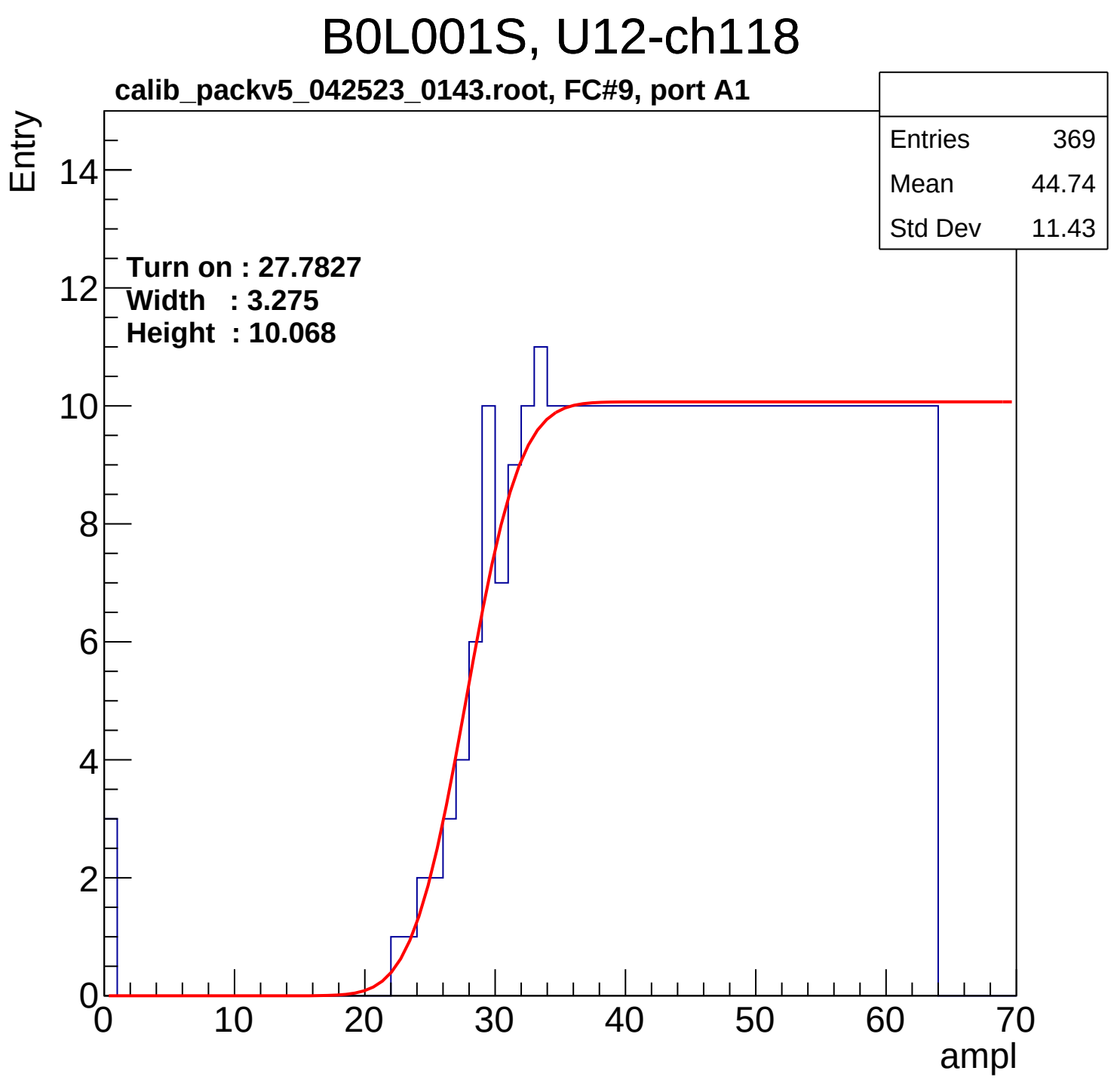
B0L001S, U12-ch118
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.74
Std Dev 11.43
Turn on : 27.7827
Width : 3.275
Height : 10.068
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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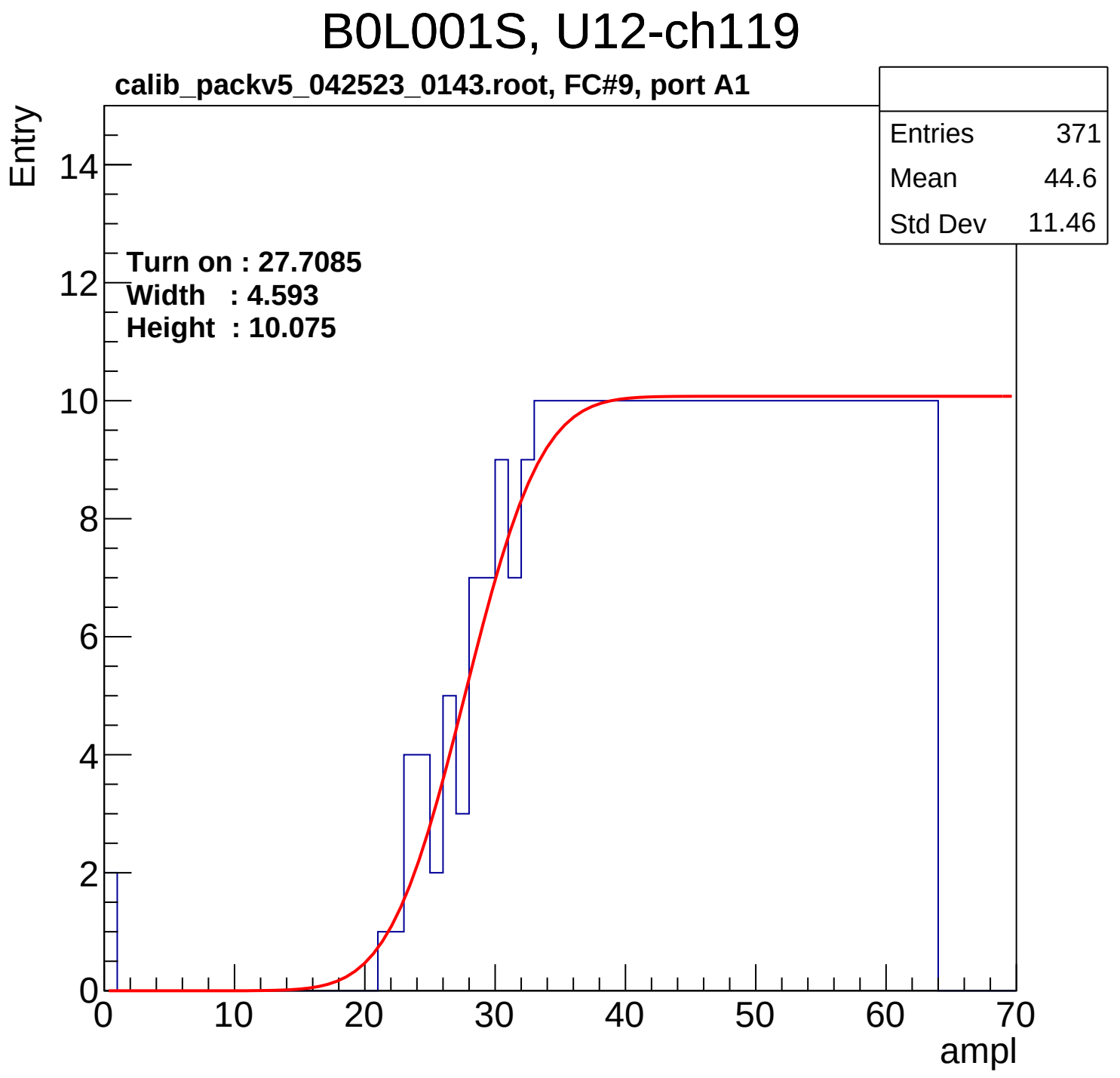
B0L001S, U12-ch119
calib_packv5_042523_0143.root, FC#9, port A1
Entries 371
Mean 44.6
Std Dev 11.46
Turn on : 27.7085
Width : 4.593
Height : 10.075
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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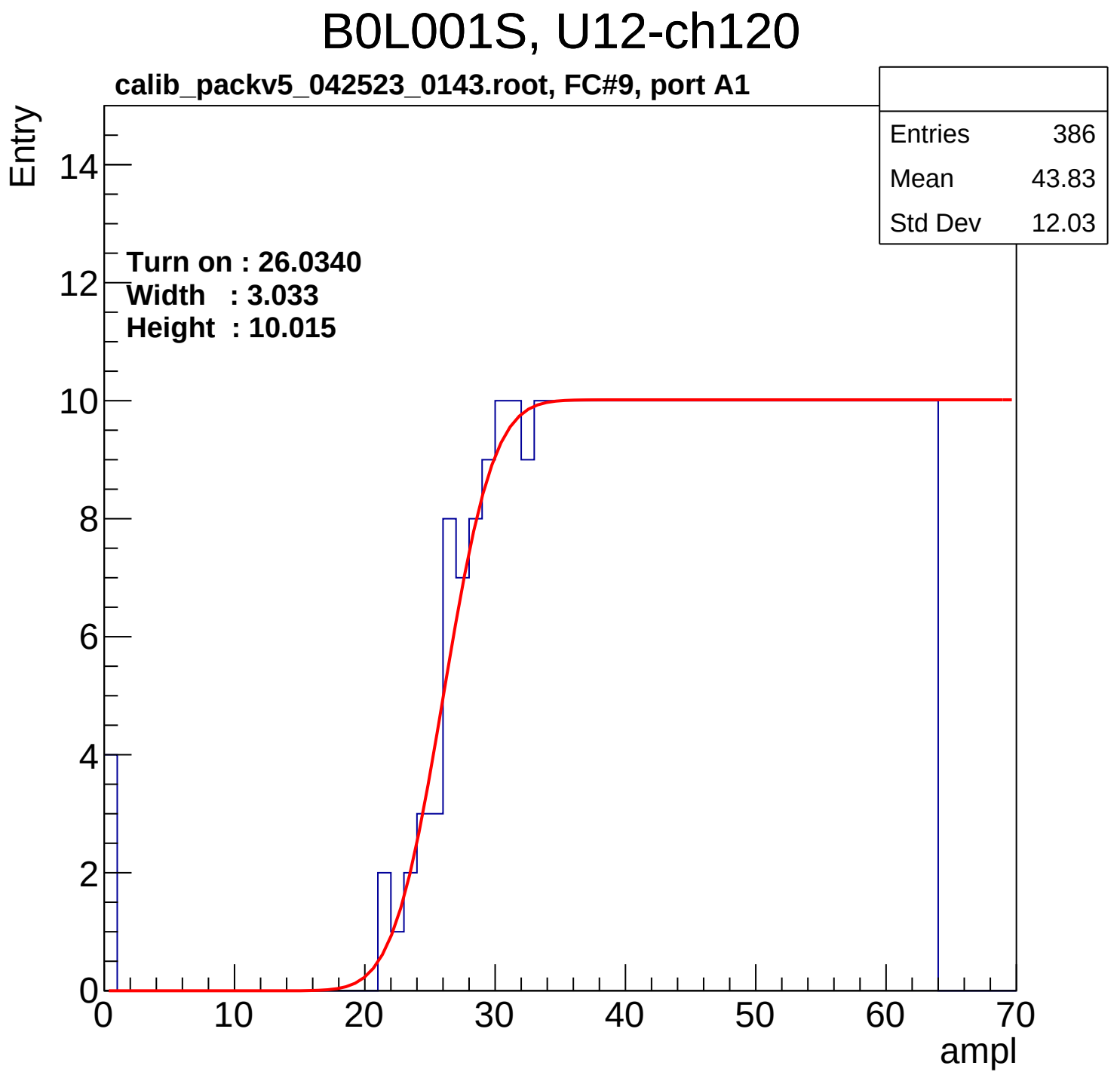
B0L001S, U12-ch120
calib_packv5_042523_0143.root, FC#9, port A1
Entries 386
Mean 43.83
Std Dev 12.03
Turn on : 26.0340
Width : 3.033
Height : 10.015
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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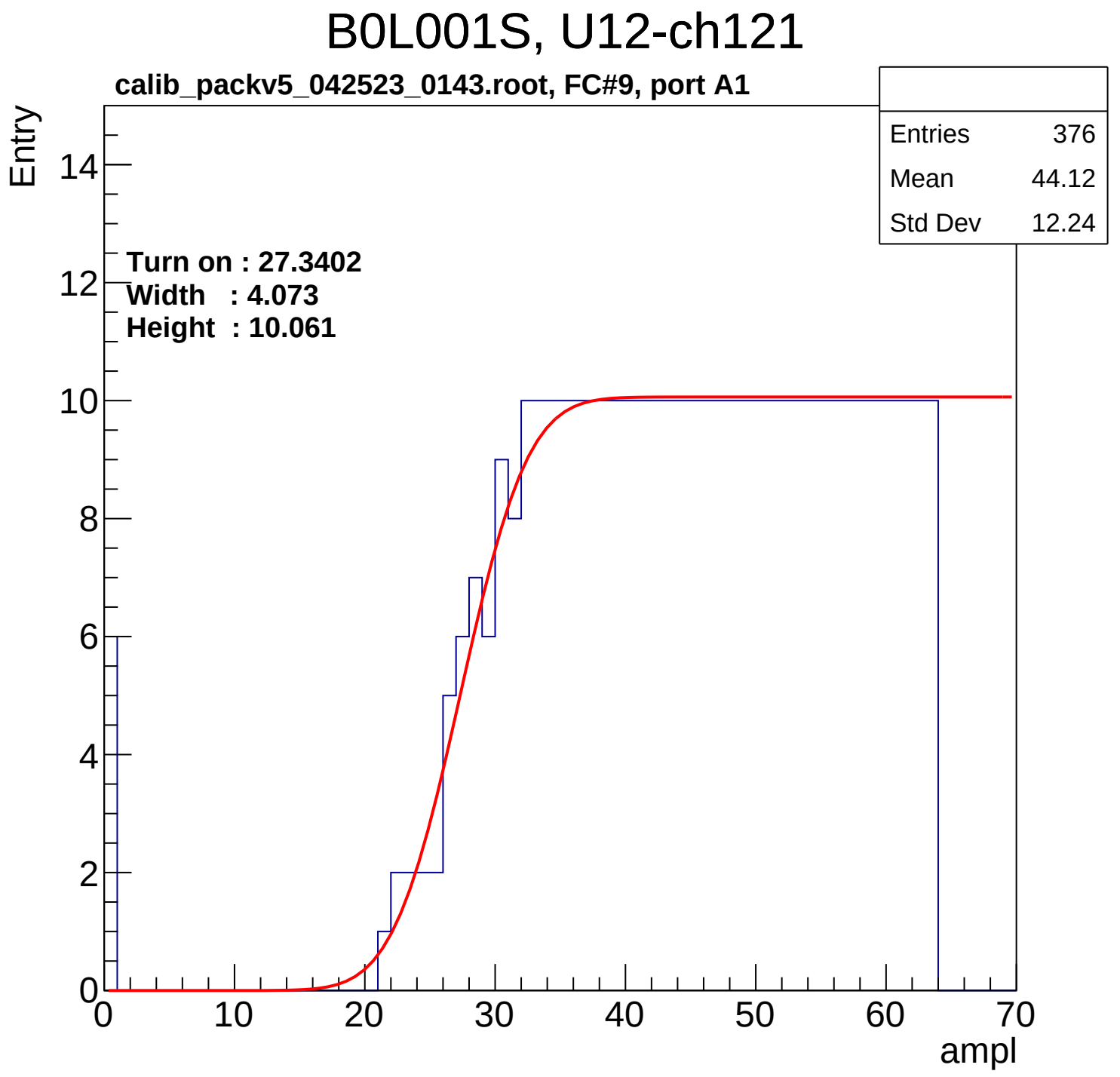
B0L001S, U12-ch121
calib_packv5_042523_0143.root, FC#9, port A1
Entries 376
Mean 44.12
Std Dev 12.24
Turn on : 27.3402
Width : 4.073
Height : 10.061
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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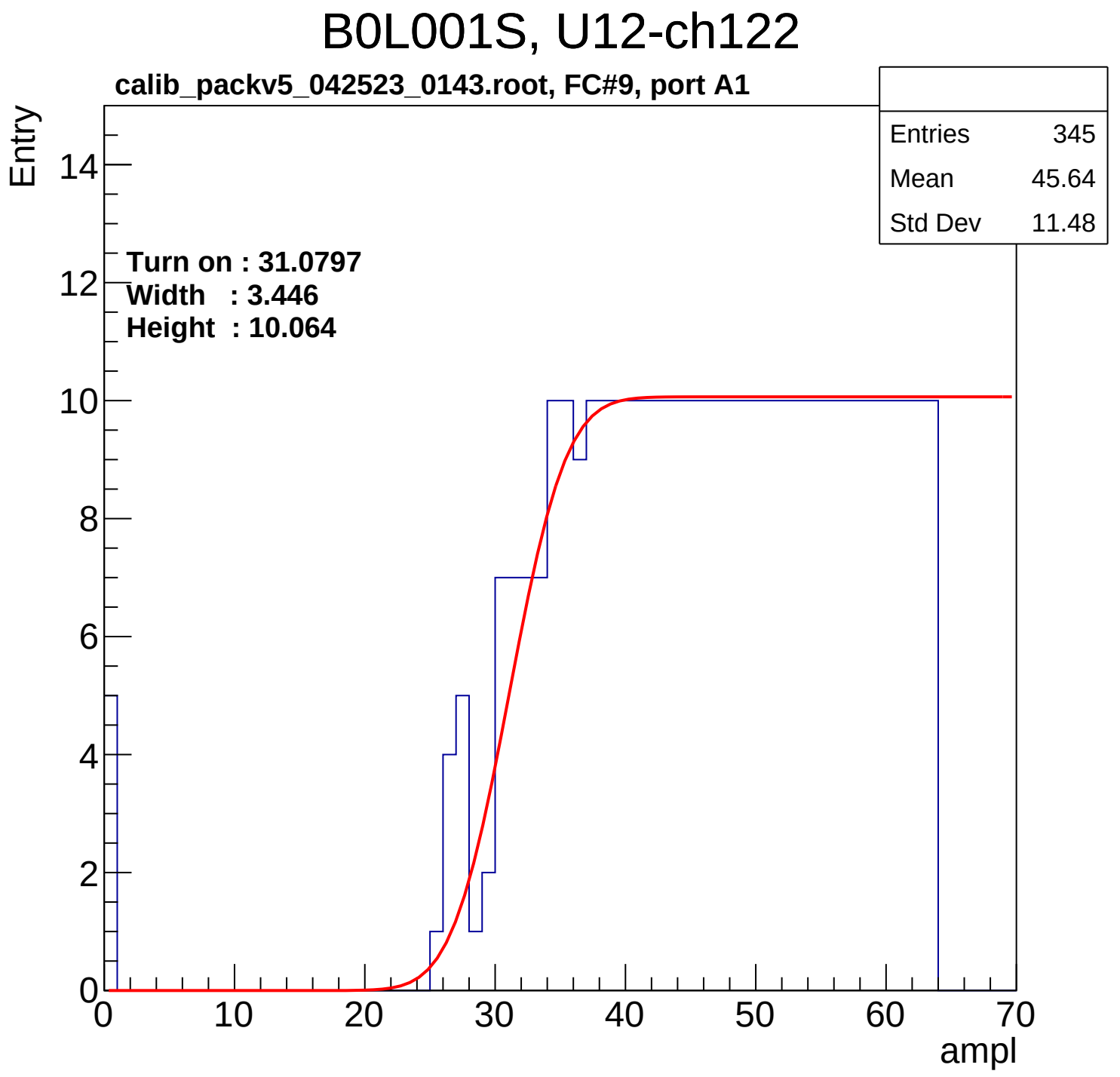
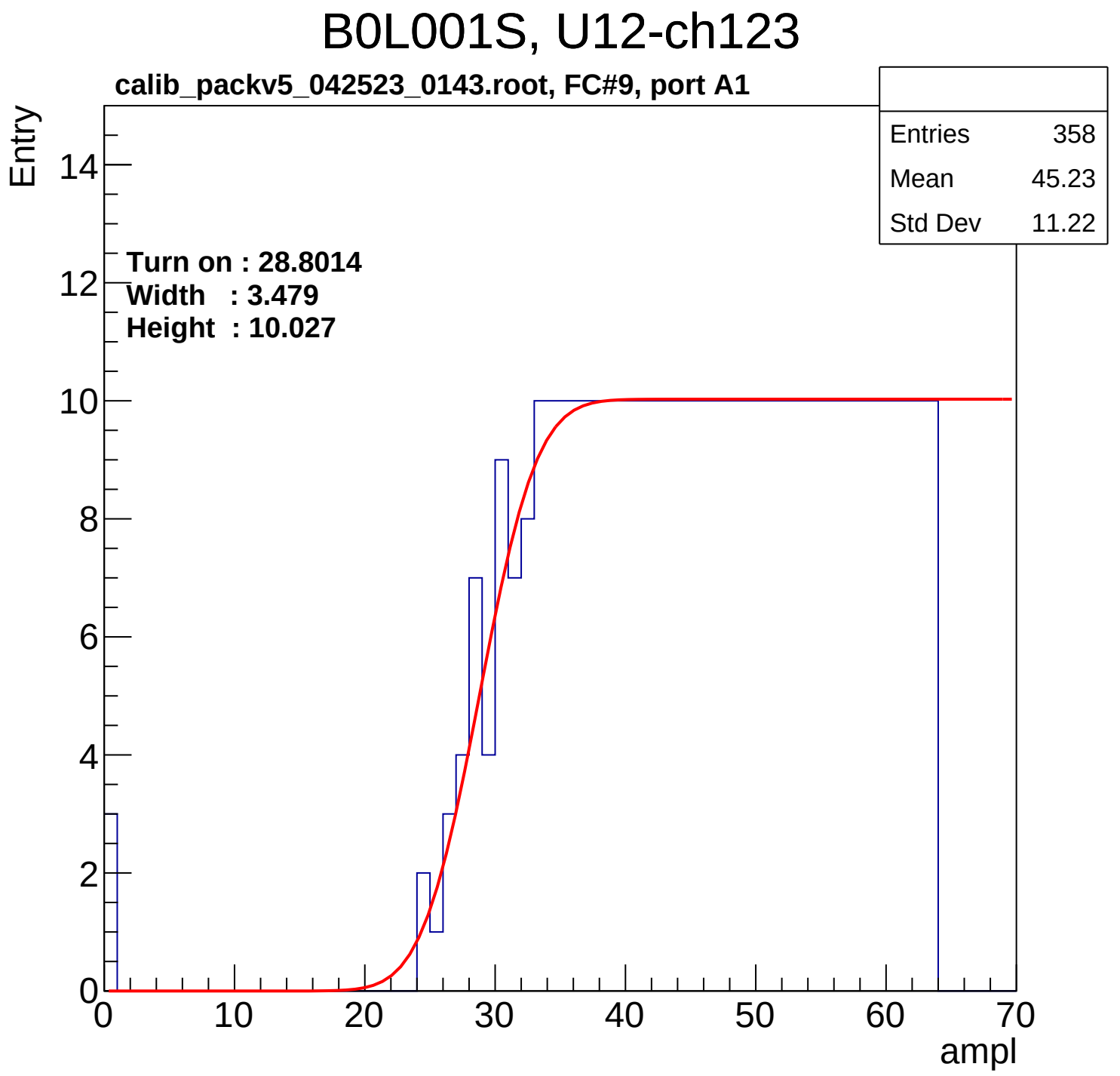

B0L001S, U12-ch122
calib_packv5_042523_0143.root, FC#9, port A1
Entries 345
Mean 45.64
Std Dev 11.48
Turn on : 31.0797
Width : 3.446
Height : 10.064
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U12-ch123
calib_packv5_042523_0143.root, FC#9, port A1
Entries 358
Mean 45.23
Std Dev 11.22
Turn on : 28.8014
Width : 3.479
Height : 10.027
Entry
ampl
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2
4
6
8
10
12
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10
20
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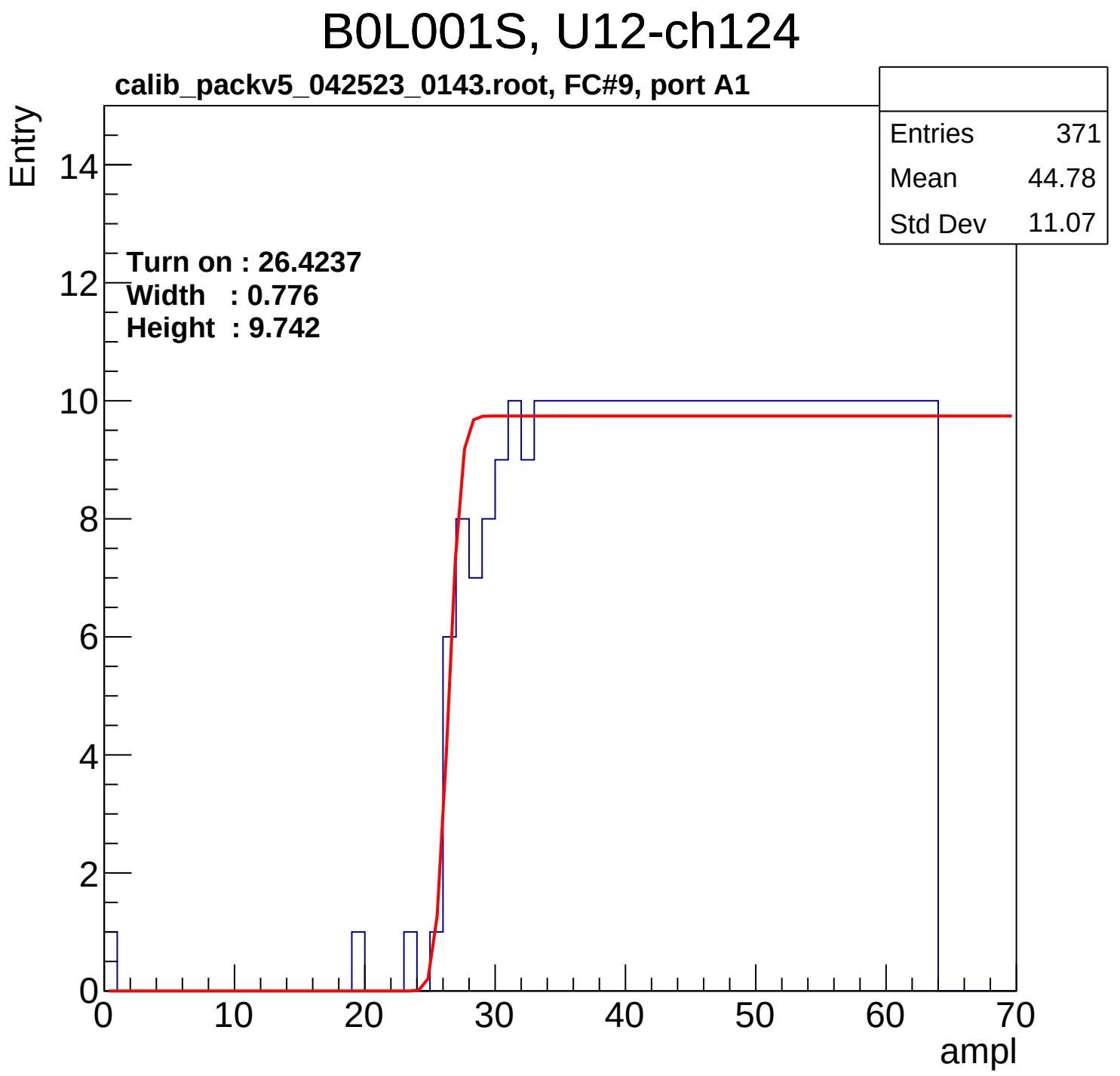
40
50
60
70


B0L001S, U12-ch124
calib_packv5_042523_0143.root, FC#9, port A1
Entries 371
Mean 44.78
Std Dev 11.07
Turn on : 26.4237
Width : 0.776
Height : 9.742
Entry
ampl
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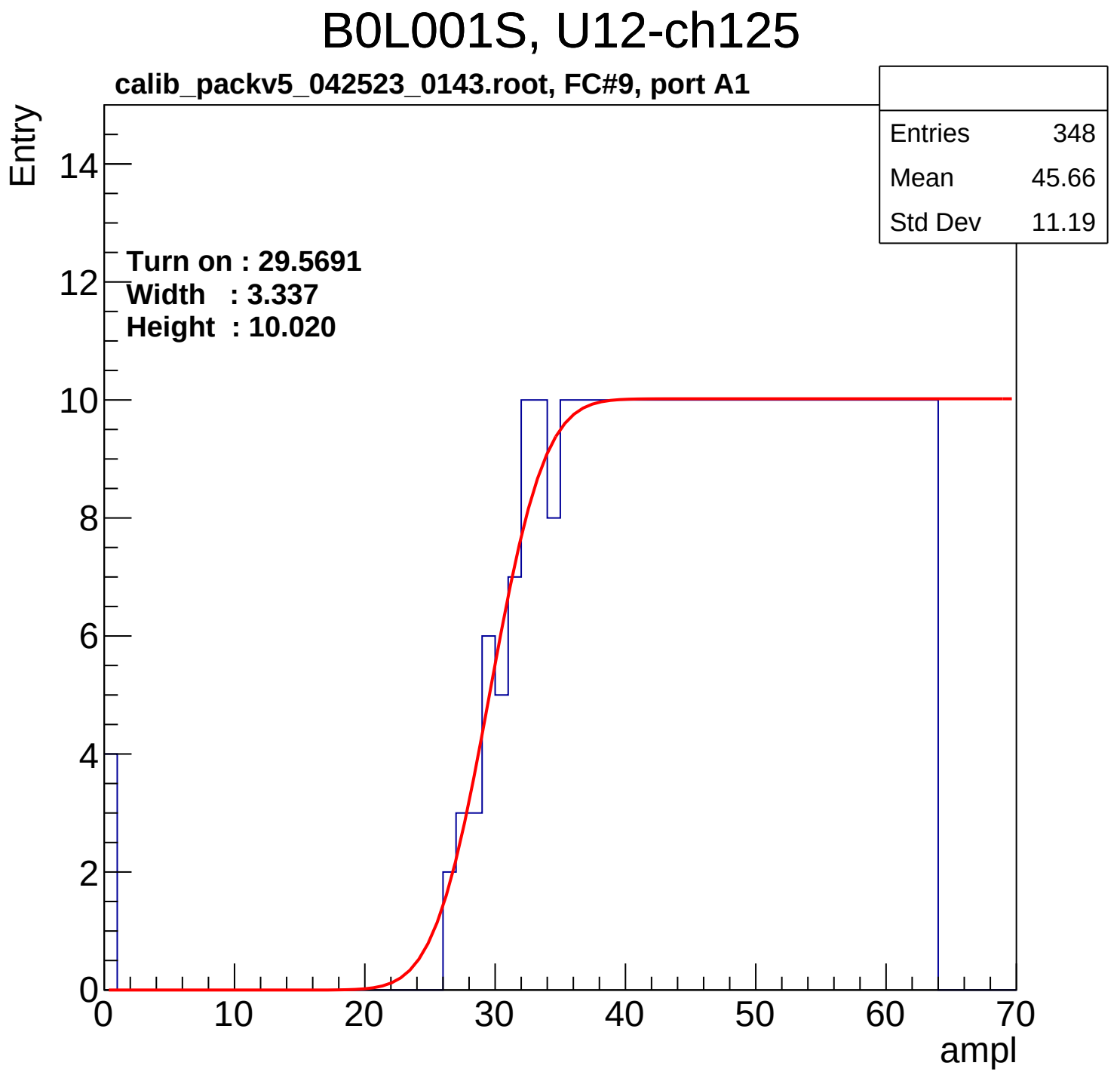
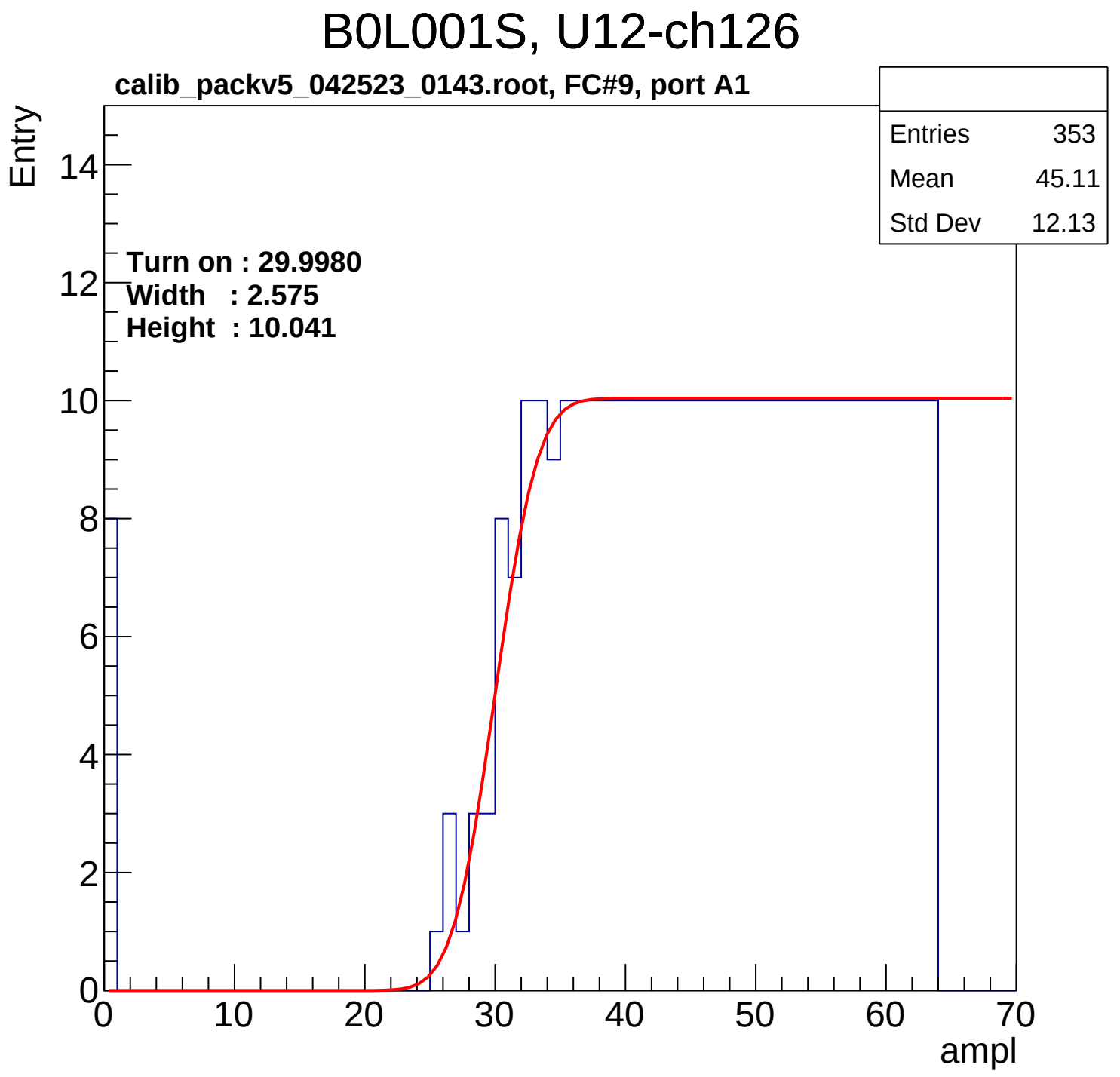
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U12-ch125
calib_packv5_042523_0143.root, FC#9, port A1
Entries 348
Mean 45.66
Std Dev 11.19
Turn on : 29.5691
Width : 3.337
Height : 10.020
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U12-ch126
calib_packv5_042523_0143.root, FC#9, port A1
Entries 353
Mean 45.11
Std Dev 12.13
Turn on : 29.9980
Width : 2.575
Height : 10.041
Entry
ampl
0
2
4
6
8
10
12
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0
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20
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40
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60
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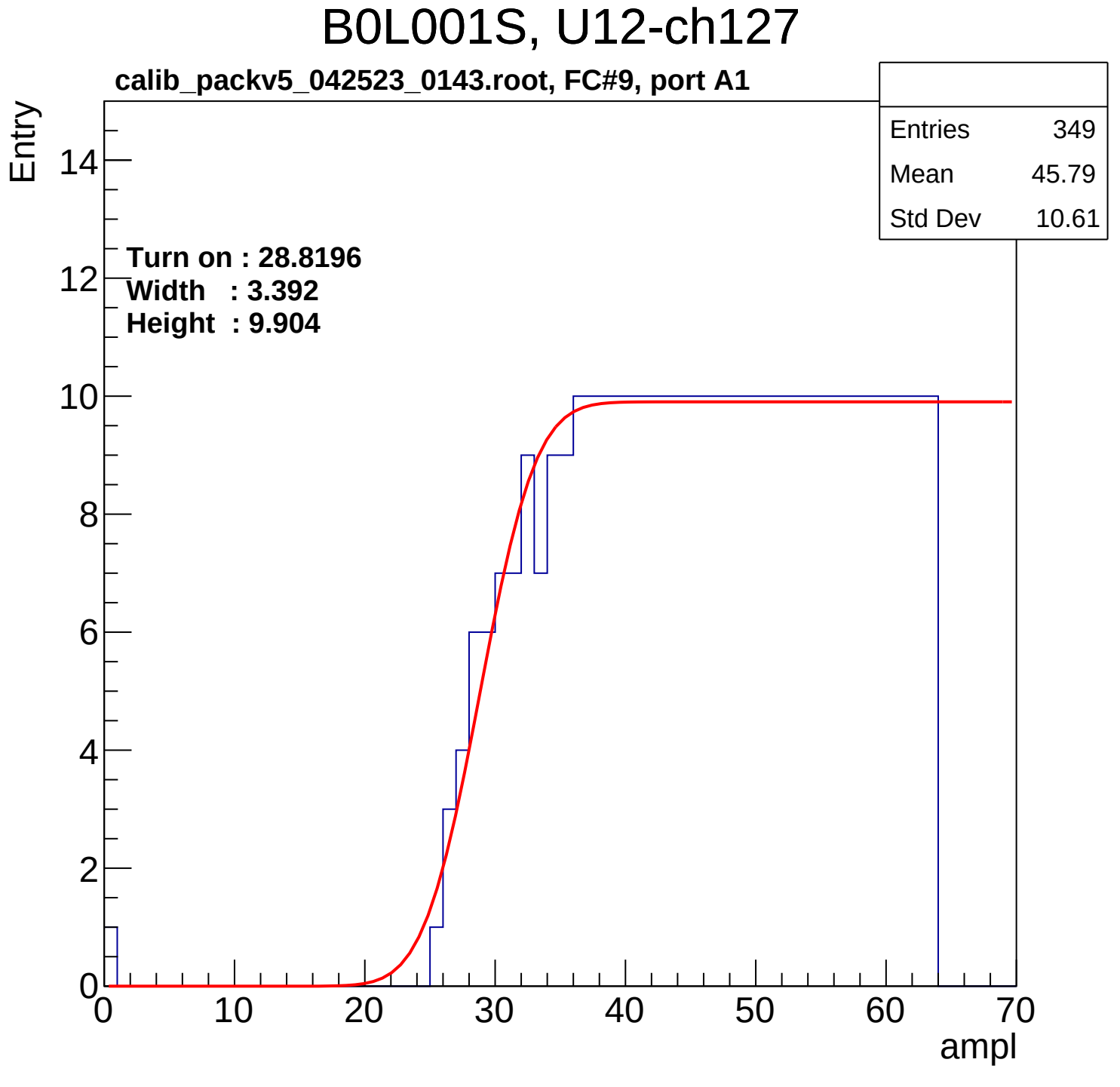
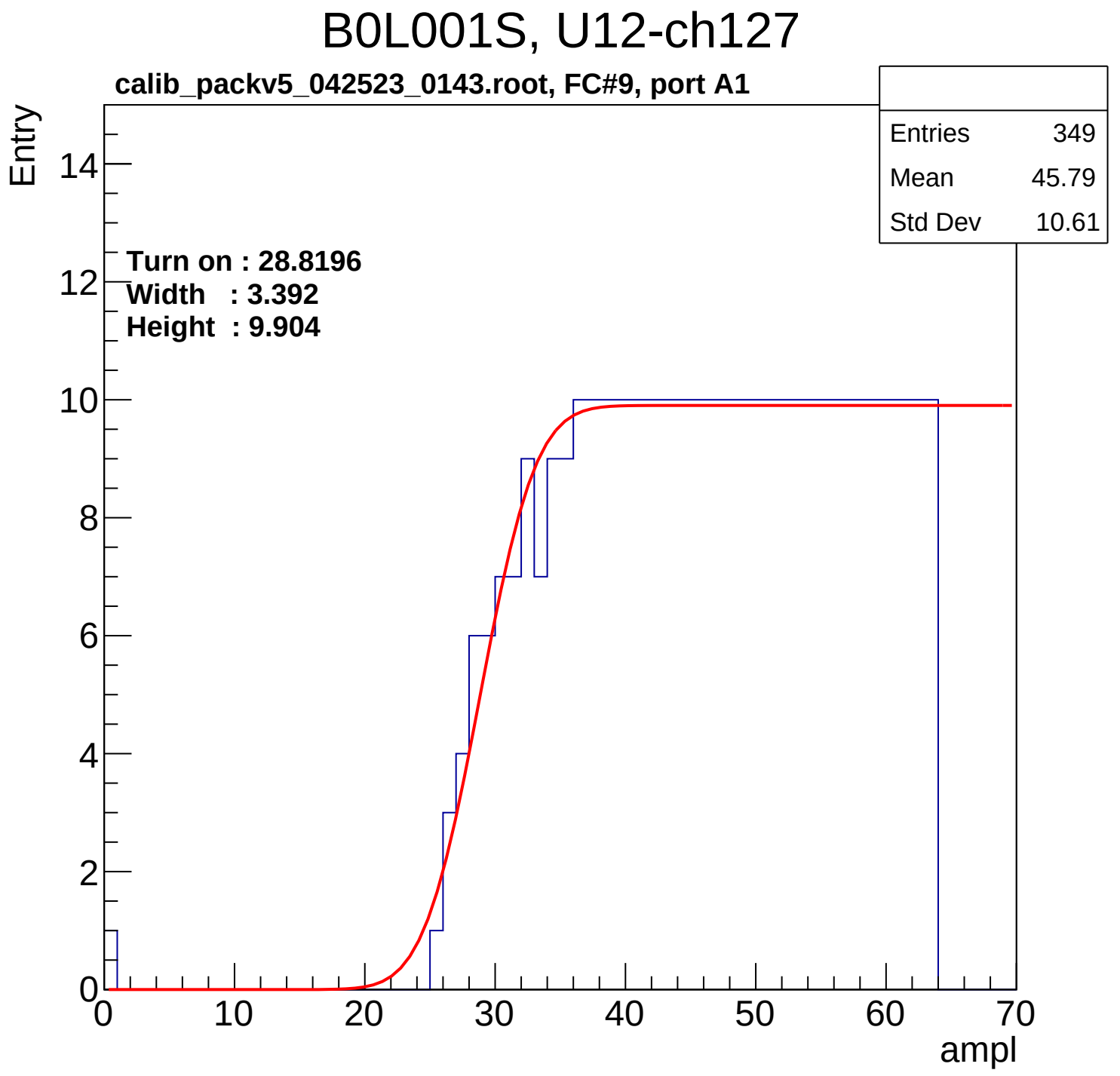

B0L001S, U12-ch127
calib_packv5_042523_0143.root, FC#9, port A1
Entries 349
Mean 45.79
Std Dev 10.61
Turn on : 28.8196
Width : 3.392
Height : 9.904
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U12-ch127
calib_packv5_042523_0143.root, FC#9, port A1
Entries 349
Mean 45.79
Std Dev 10.61
Turn on : 28.8196
Width : 3.392
Height : 9.904
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70