



# B1L102S, U2-ch0

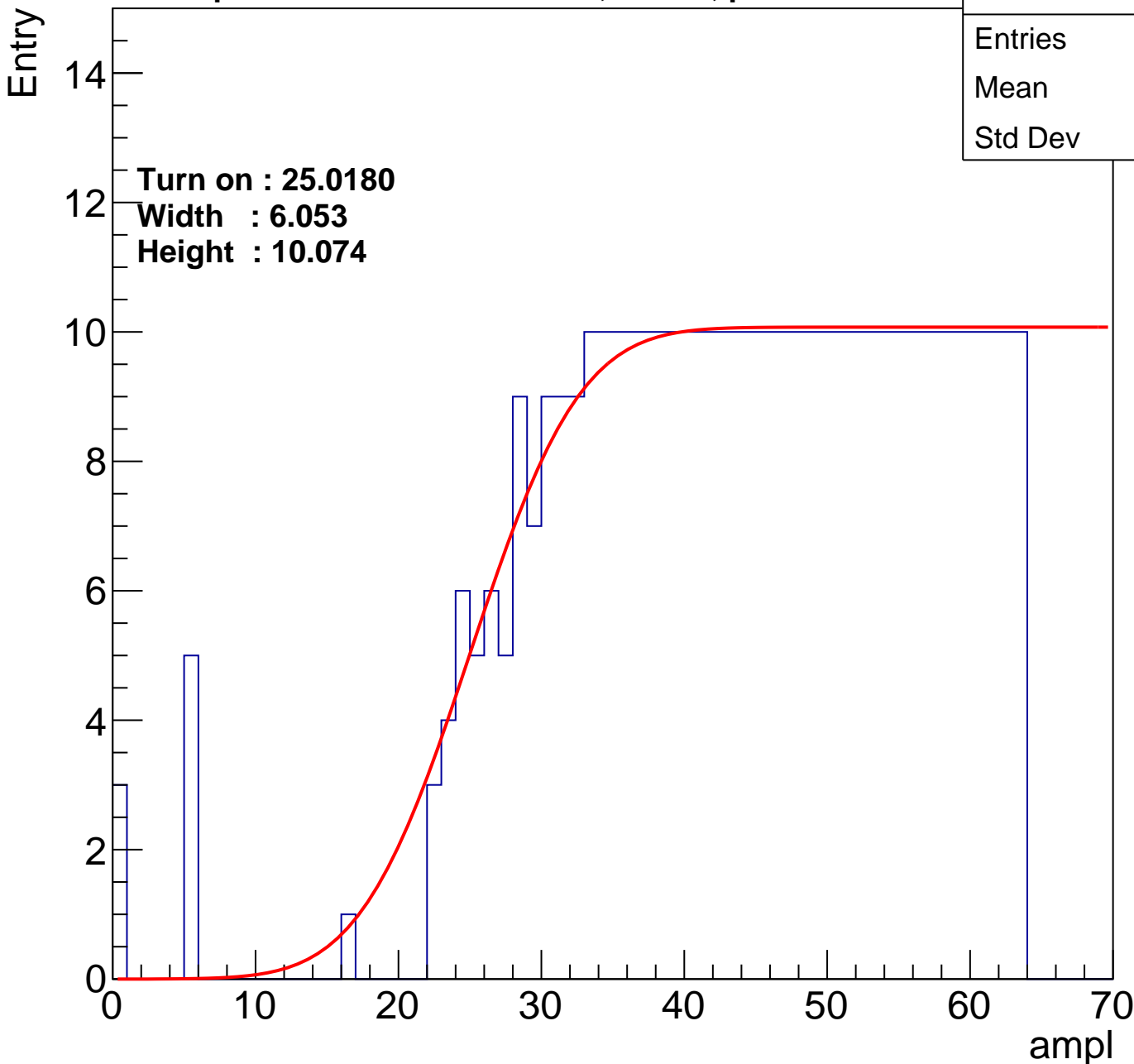
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	391
Mean	43.3
Std Dev	12.7

Turn on : 25.0180

Width : 6.053

Height : 10.074



# B1L102S, U2-ch1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	380
Mean	44.31
Std Dev	11.37

Turn on : 26.5599

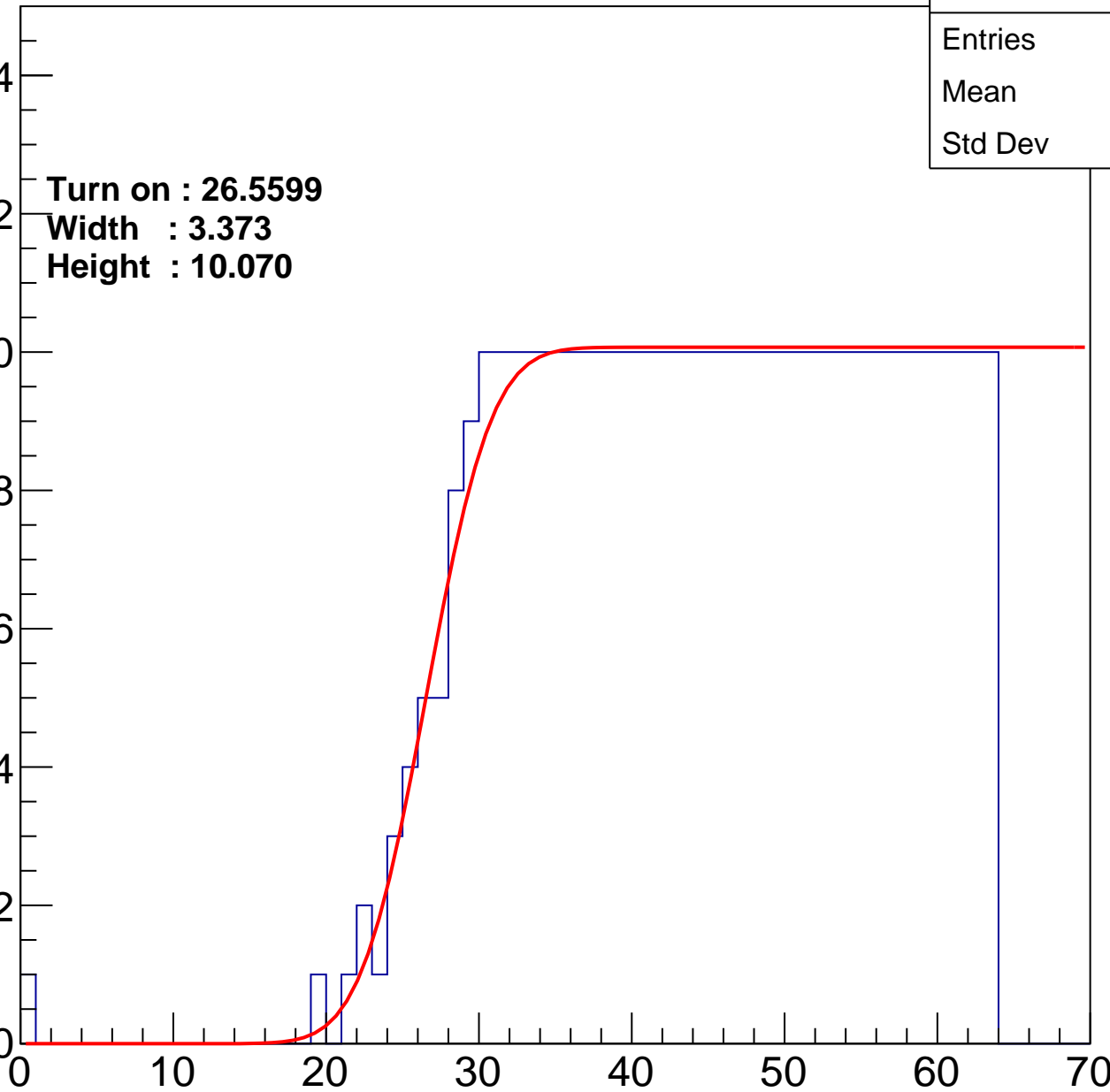
Width : 3.373

Height : 10.070

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch2

calib\_packv5\_042523\_0143.root, FC#11, port A2

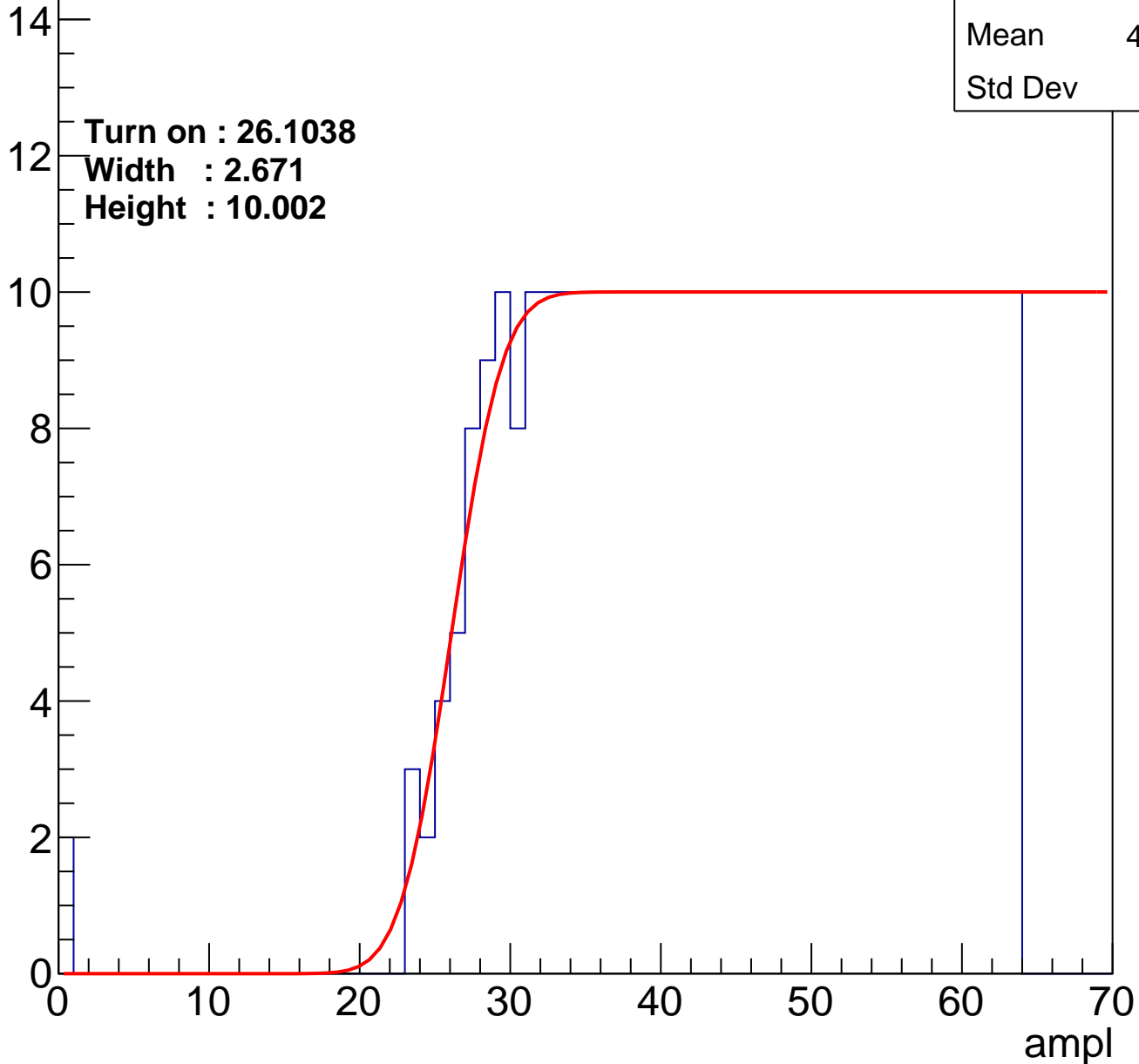
Entries	381
Mean	44.24
Std Dev	11.5

Turn on : 26.1038

Width : 2.671

Height : 10.002

Entry



# B1L102S, U2-ch3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	383
Mean	44.02
Std Dev	11.8

Turn on : 25.8608

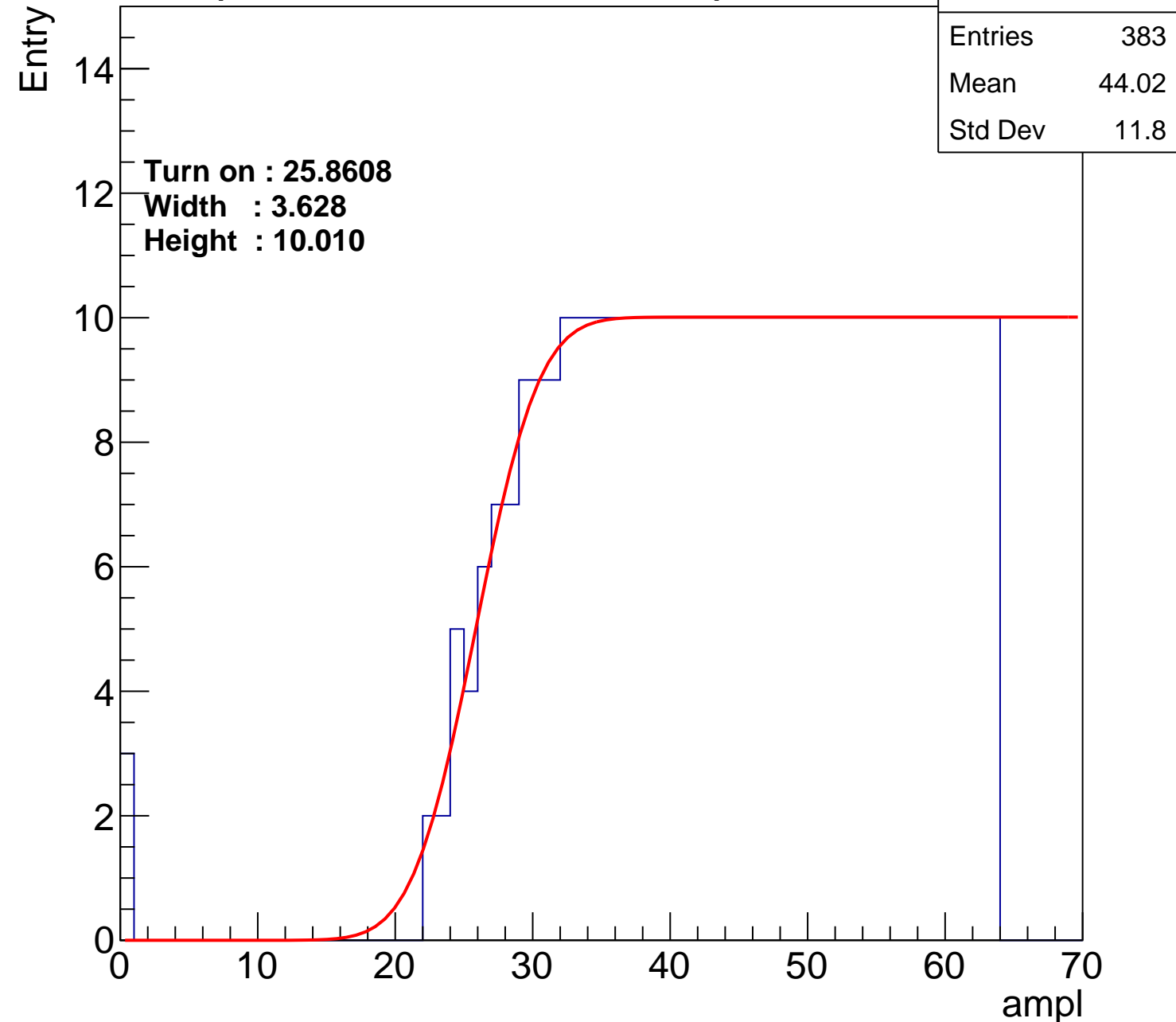
Width : 3.628

Height : 10.010

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	376
Mean	44.44
Std Dev	11.45

Turn on : 27.0997

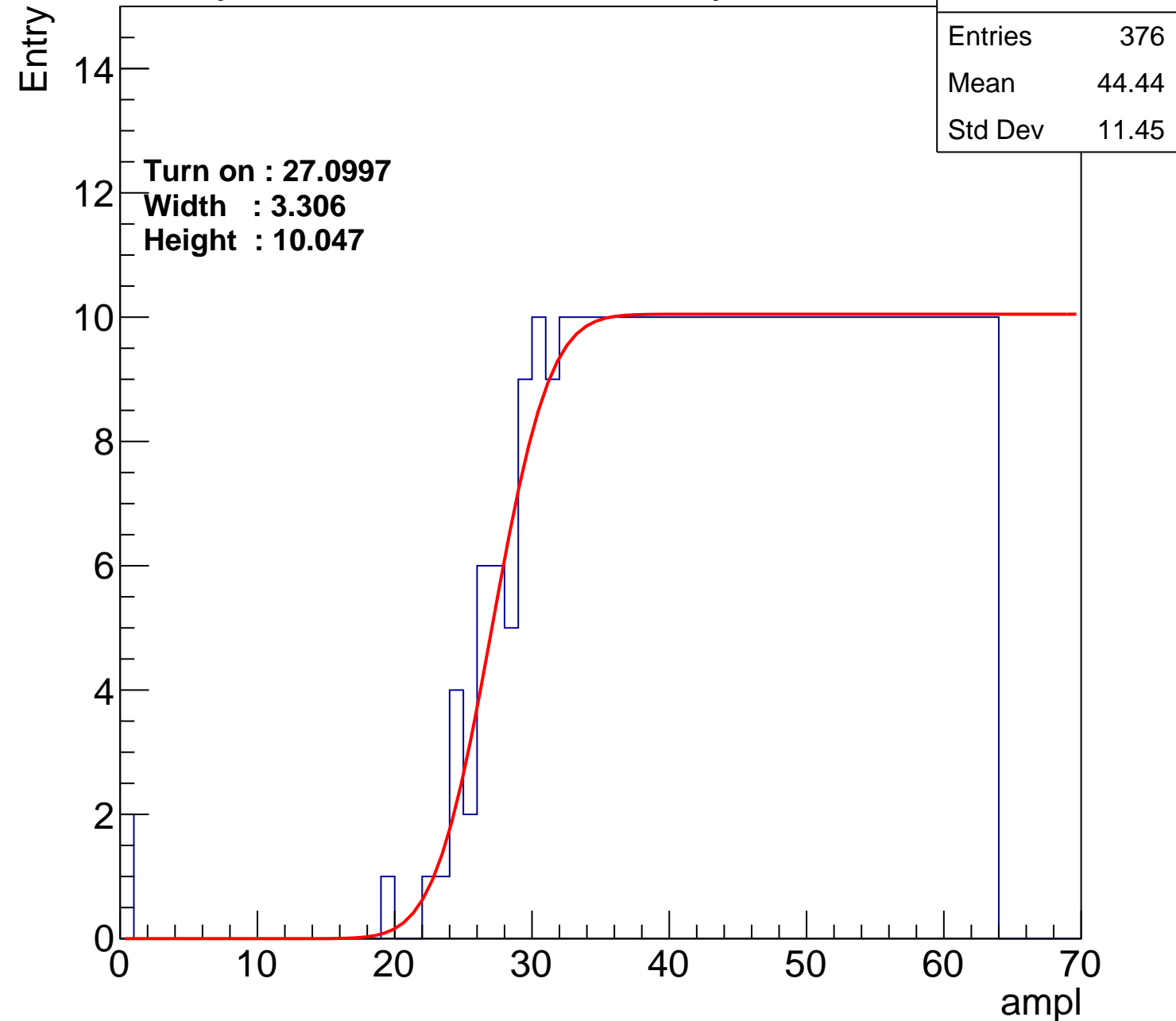
Width : 3.306

Height : 10.047

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	373
Mean	44.56
Std Dev	11.42

Turn on : 27.5548

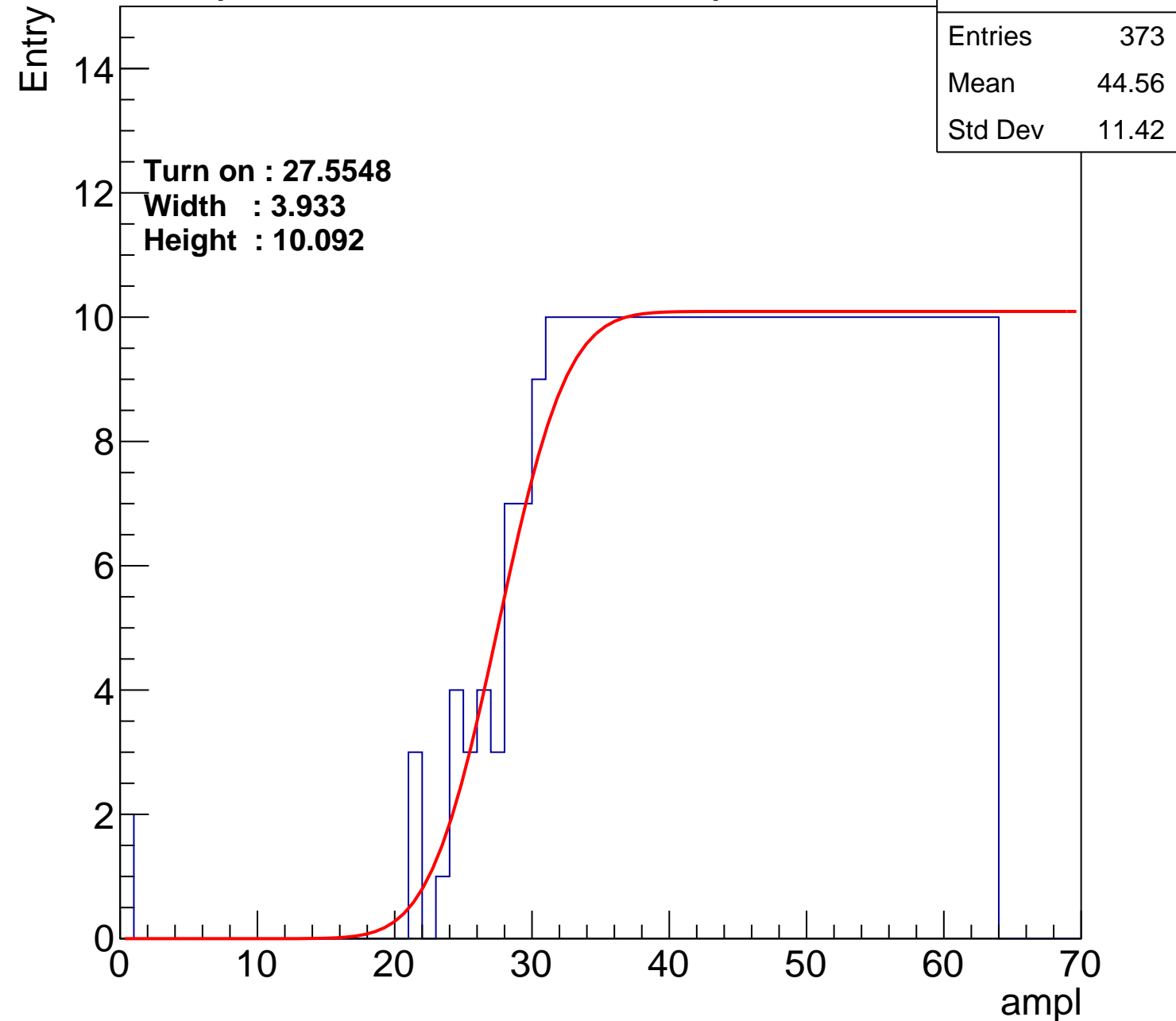
Width : 3.933

Height : 10.092

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	380
Mean	44.25
Std Dev	11.54

Turn on : 25.9886

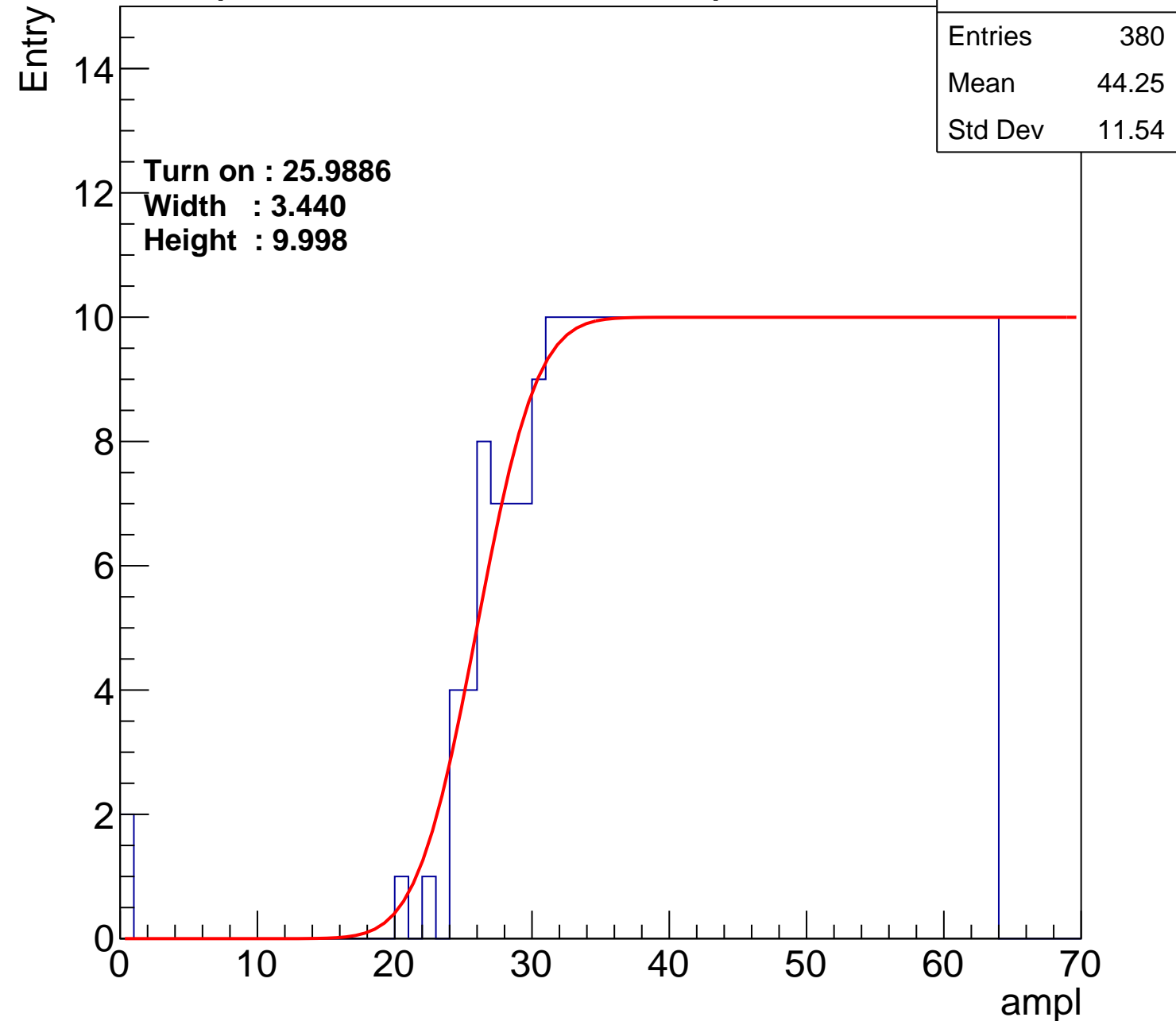
Width : 3.440

Height : 9.998

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L102S, U2-ch7

calib\_packv5\_042523\_0143.root, FC#11, port A2

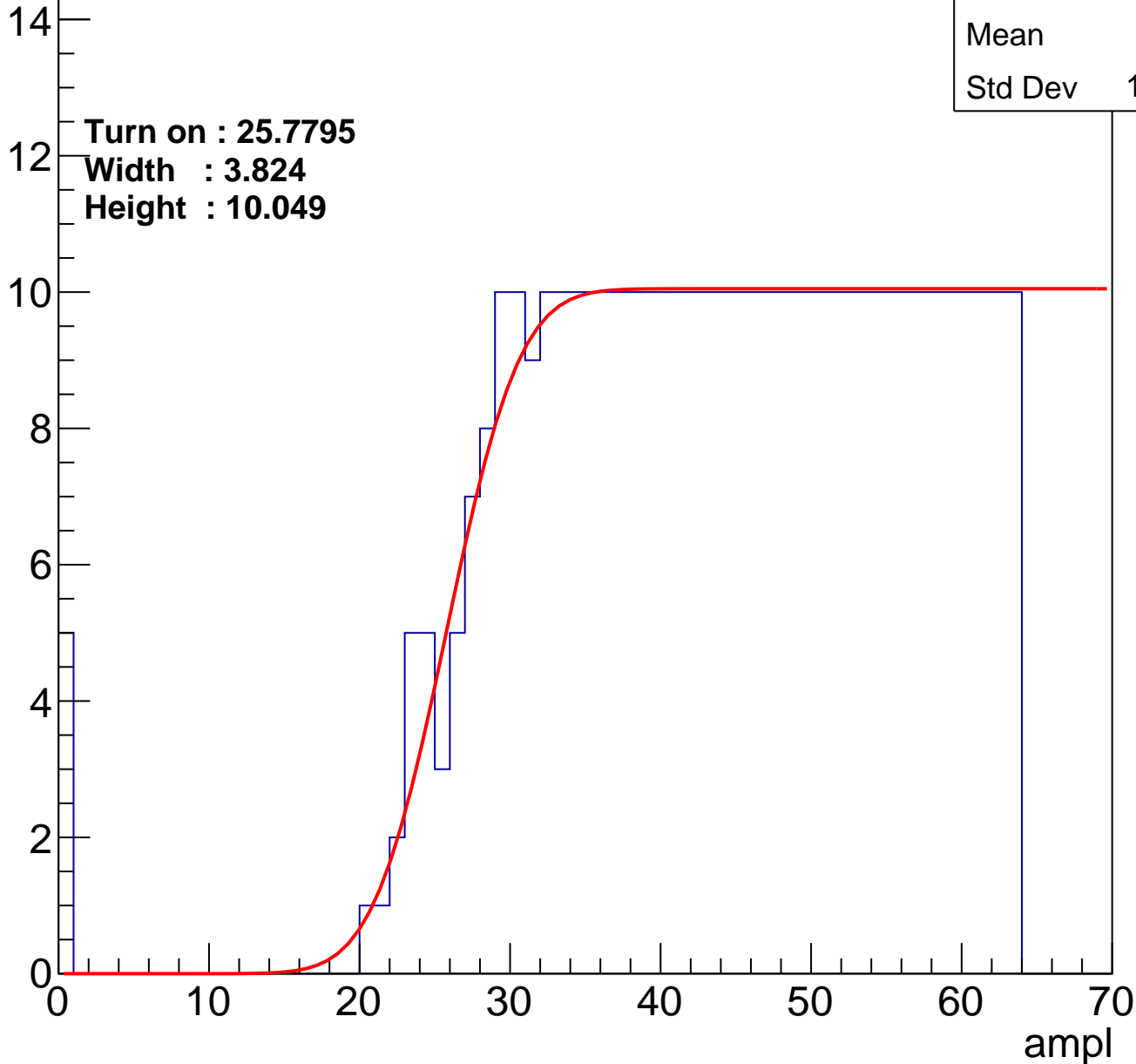
Entries	391
Mean	43.5
Std Dev	12.34

Turn on : 25.7795

Width : 3.824

Height : 10.049

Entry



# B1L102S, U2-ch8

calib\_packv5\_042523\_0143.root, FC#11, port A2

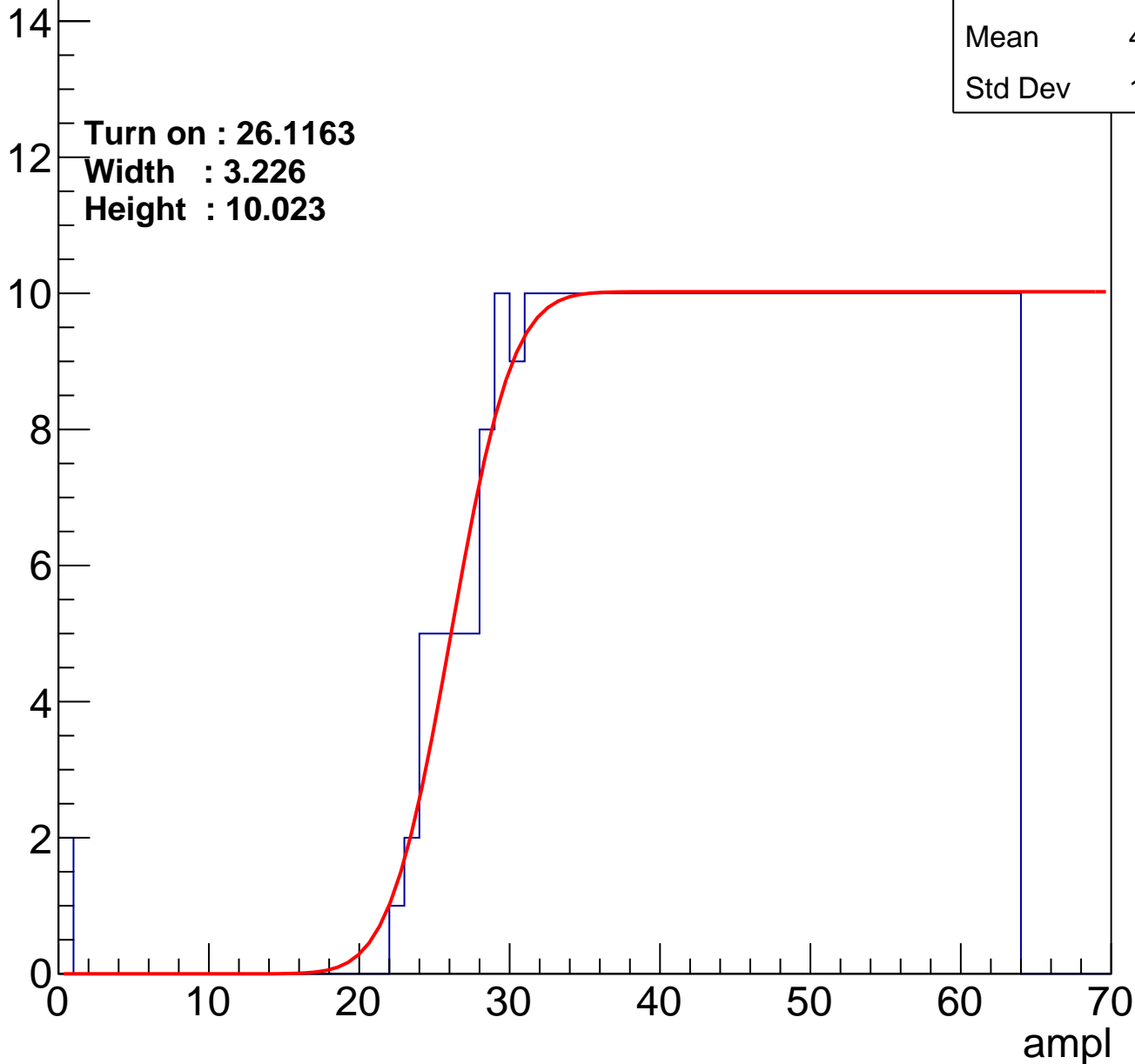
Entry

Entries	382
Mean	44.17
Std Dev	11.56

Turn on : 26.1163

Width : 3.226

Height : 10.023



# B1L102S, U2-ch9

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	383
Mean	44.08
Std Dev	11.66

Turn on : 26.1546

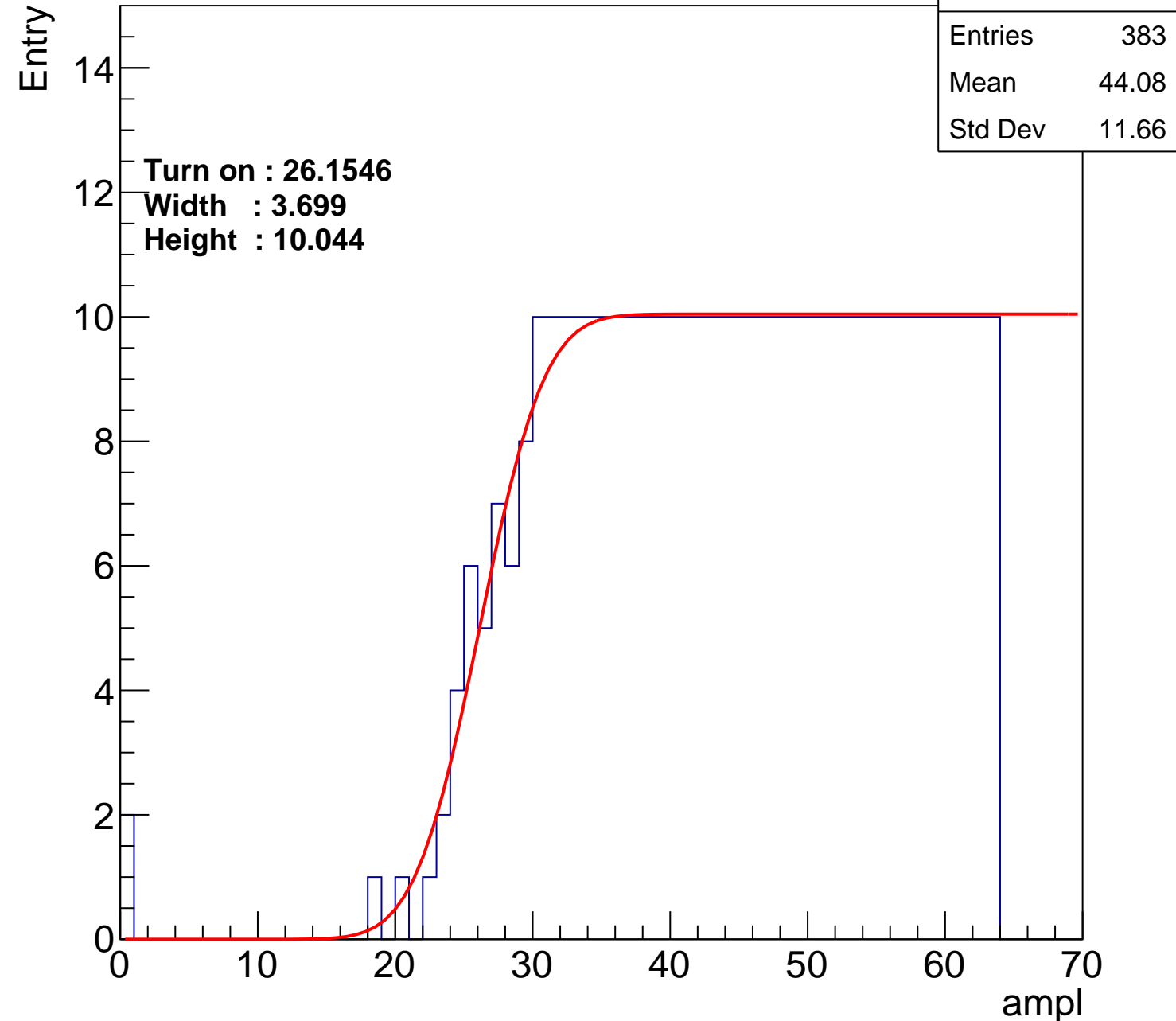
Width : 3.699

Height : 10.044

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch10

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	378
Mean	44.26
Std Dev	11.7

Turn on : 27.3513

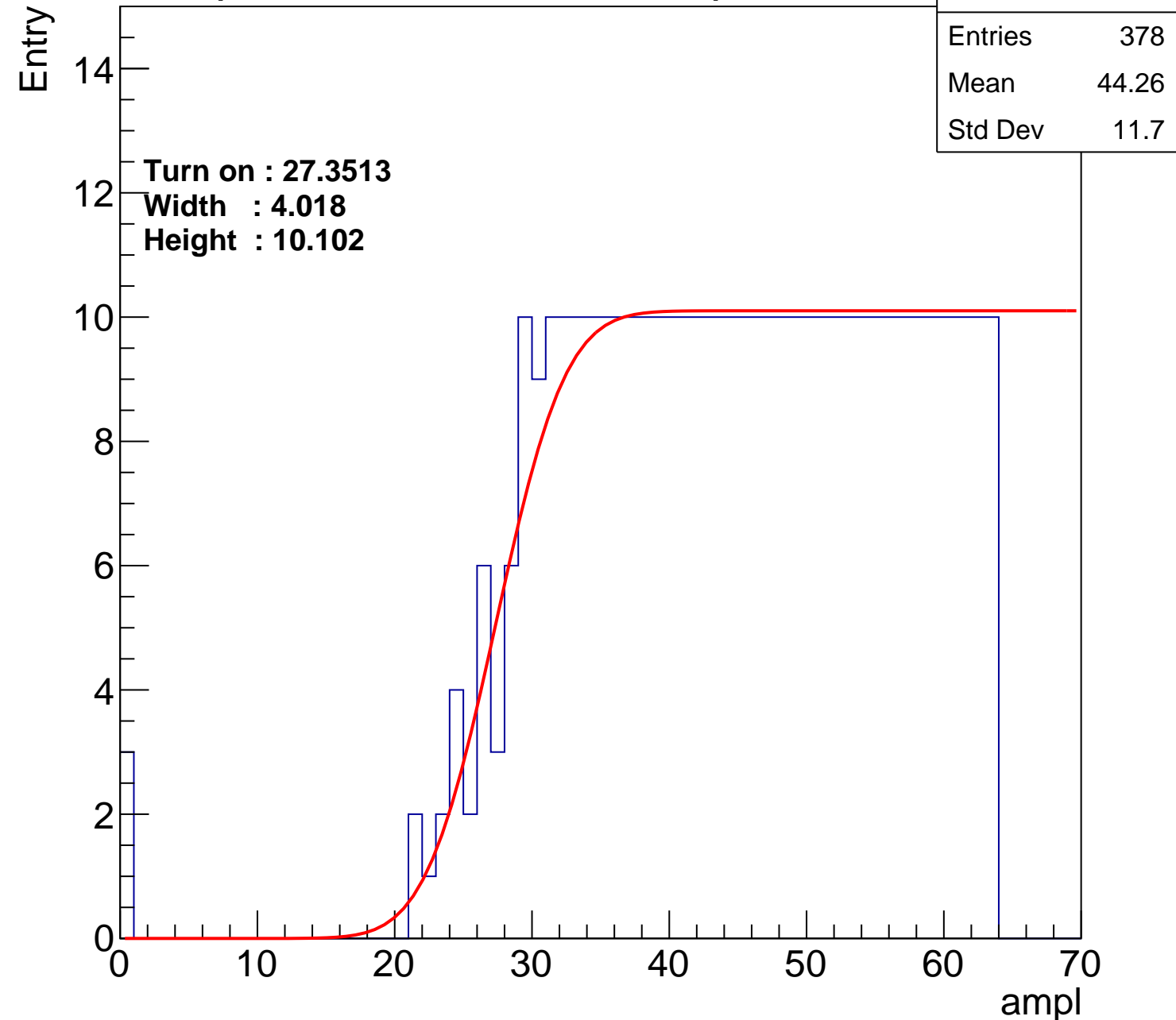
Width : 4.018

Height : 10.102

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch11

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	390
Mean	43.79
Std Dev	11.74

Turn on : 25.3990

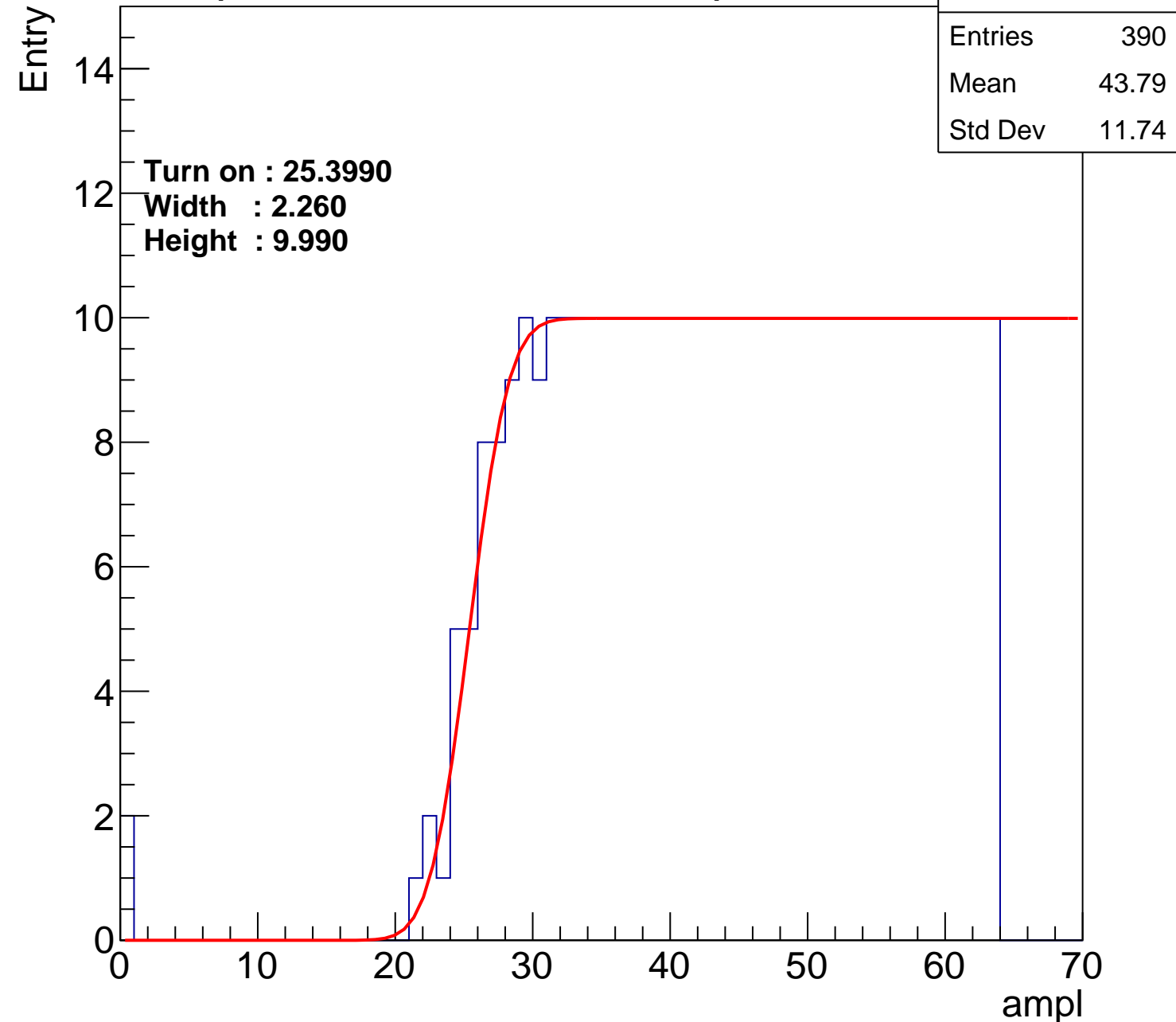
Width : 2.260

Height : 9.990

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch12

calib\_packv5\_042523\_0143.root, FC#11, port A2

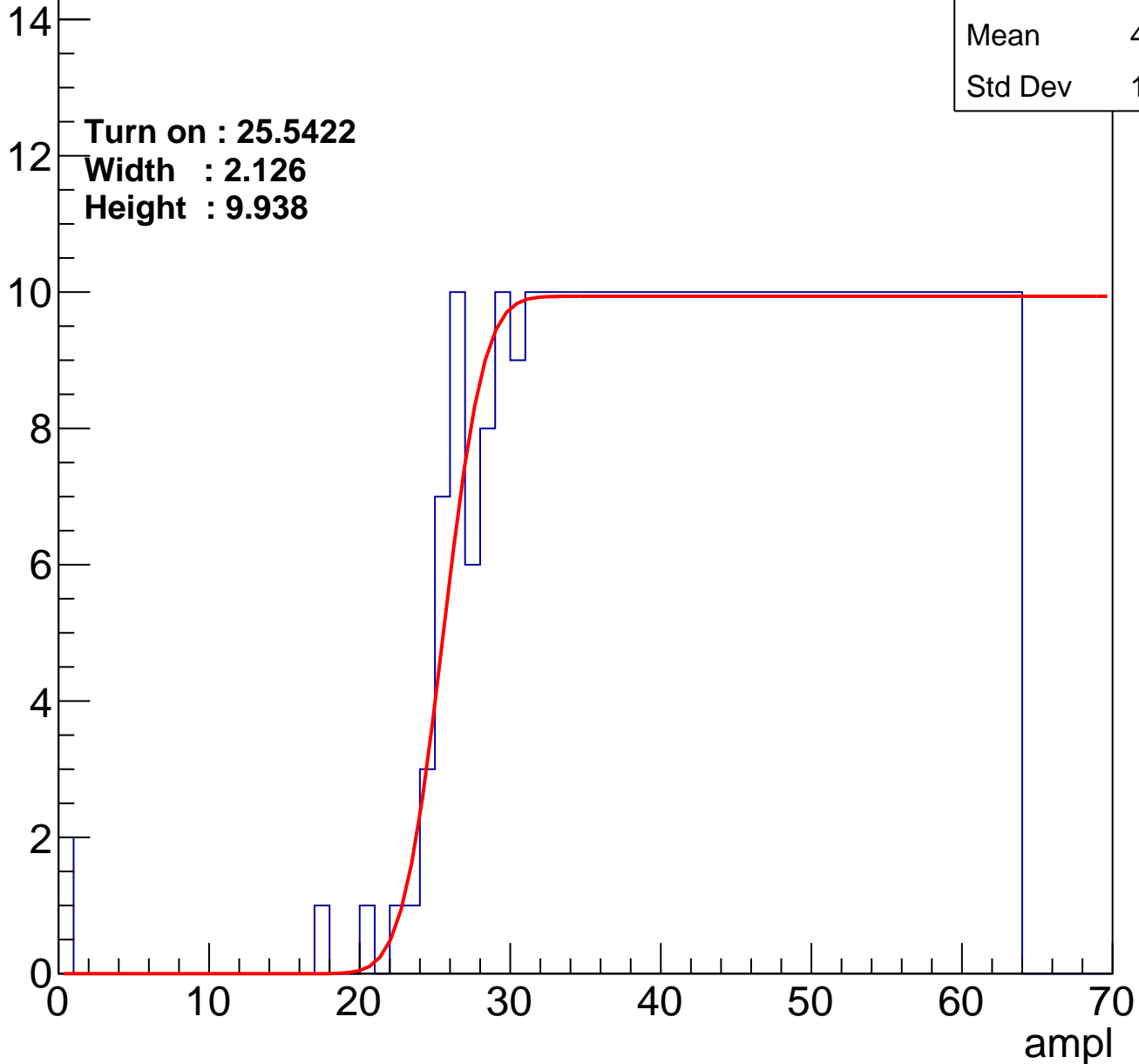
Entries	389
Mean	43.82
Std Dev	11.75

Turn on : 25.5422

Width : 2.126

Height : 9.938

Entry



# B1L102S, U2-ch13

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	378
Mean	44.27
Std Dev	11.68

**Turn on : 26.1107**

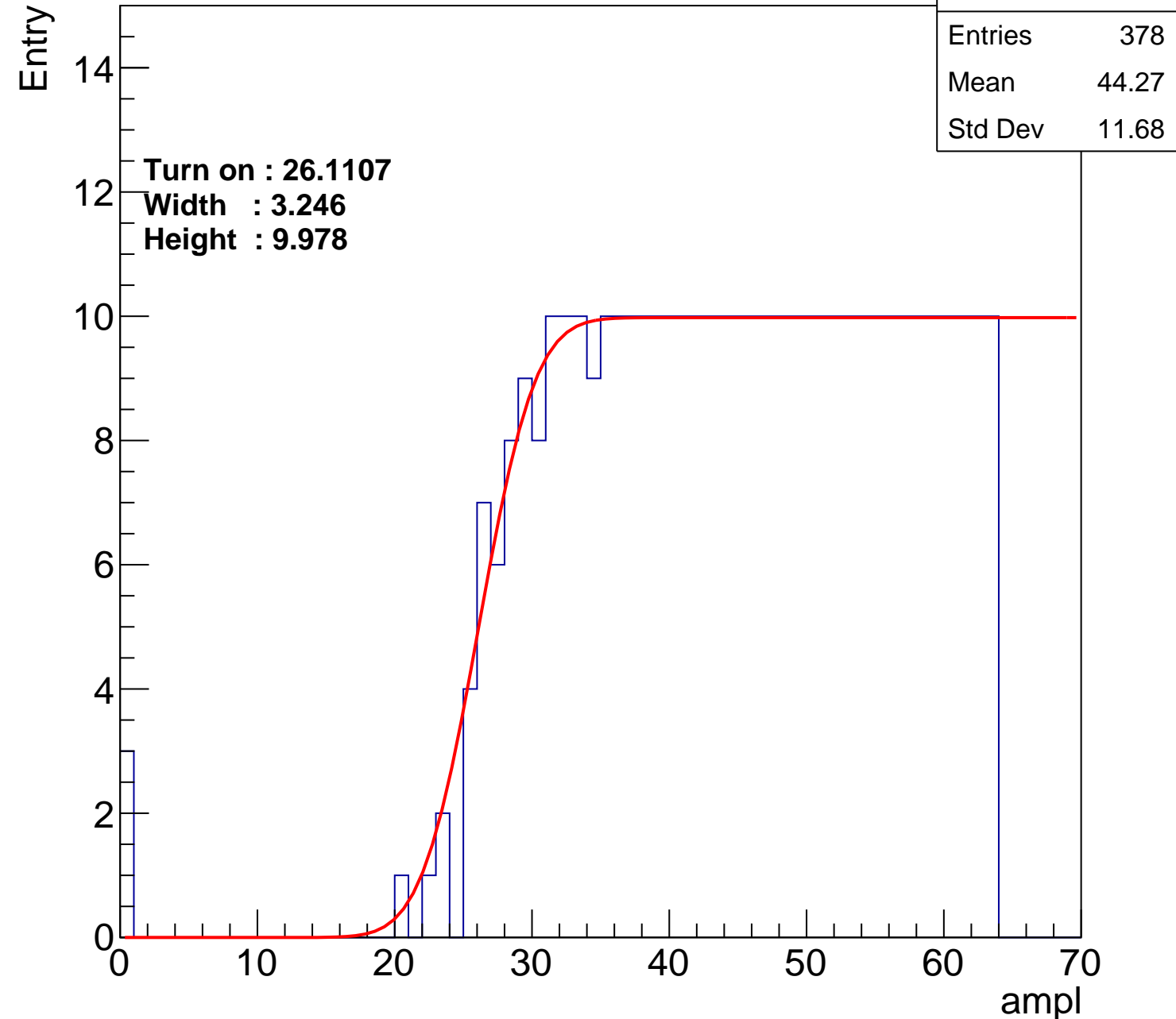
**Width : 3.246**

**Height : 9.978**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch14

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	379
Mean	44.39
Std Dev	11.28

**Turn on : 26.2963**

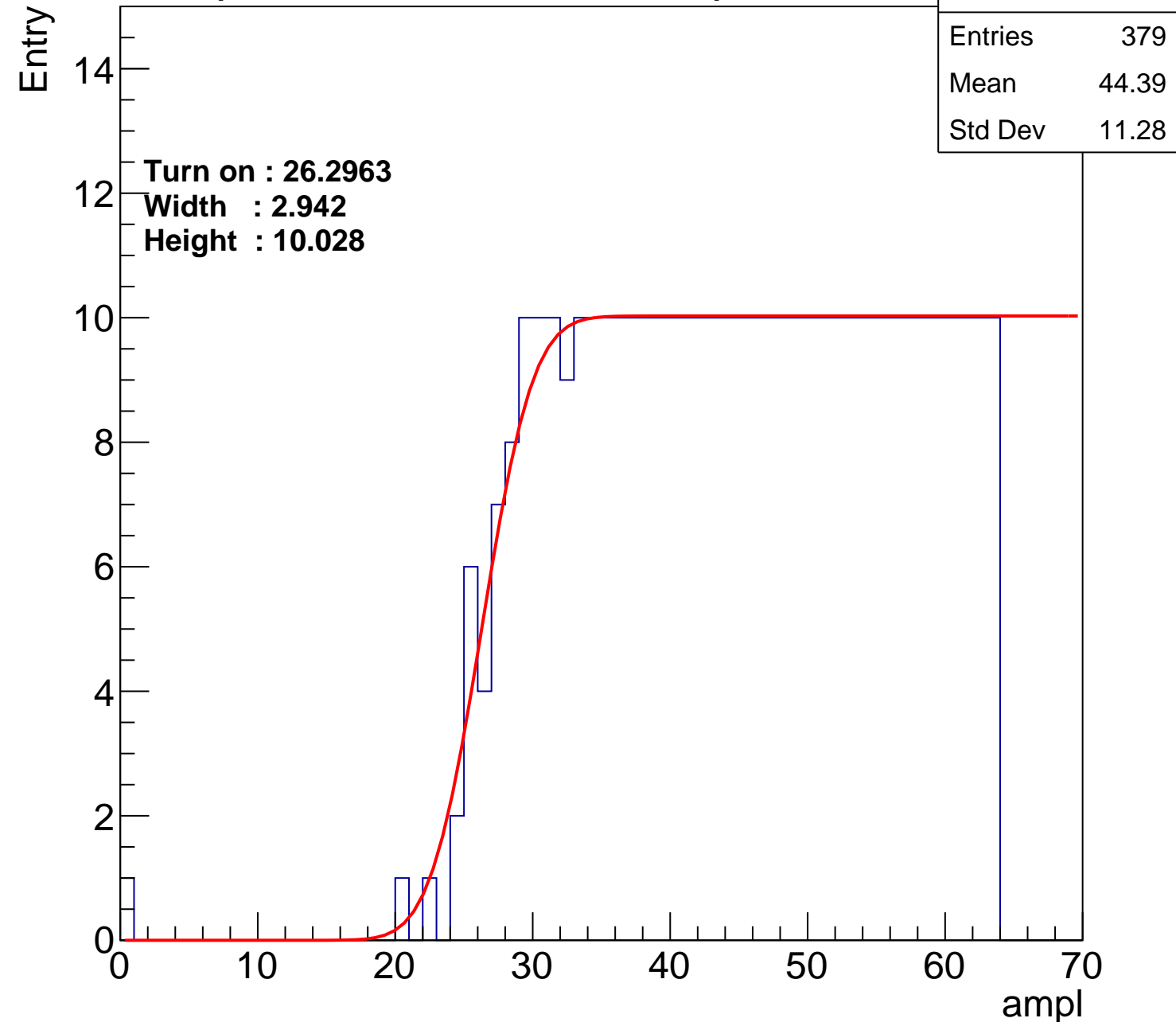
**Width : 2.942**

**Height : 10.028**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L102S, U2-ch15

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	387
Mean	43.81
Std Dev	12.01

Turn on : 25.8875

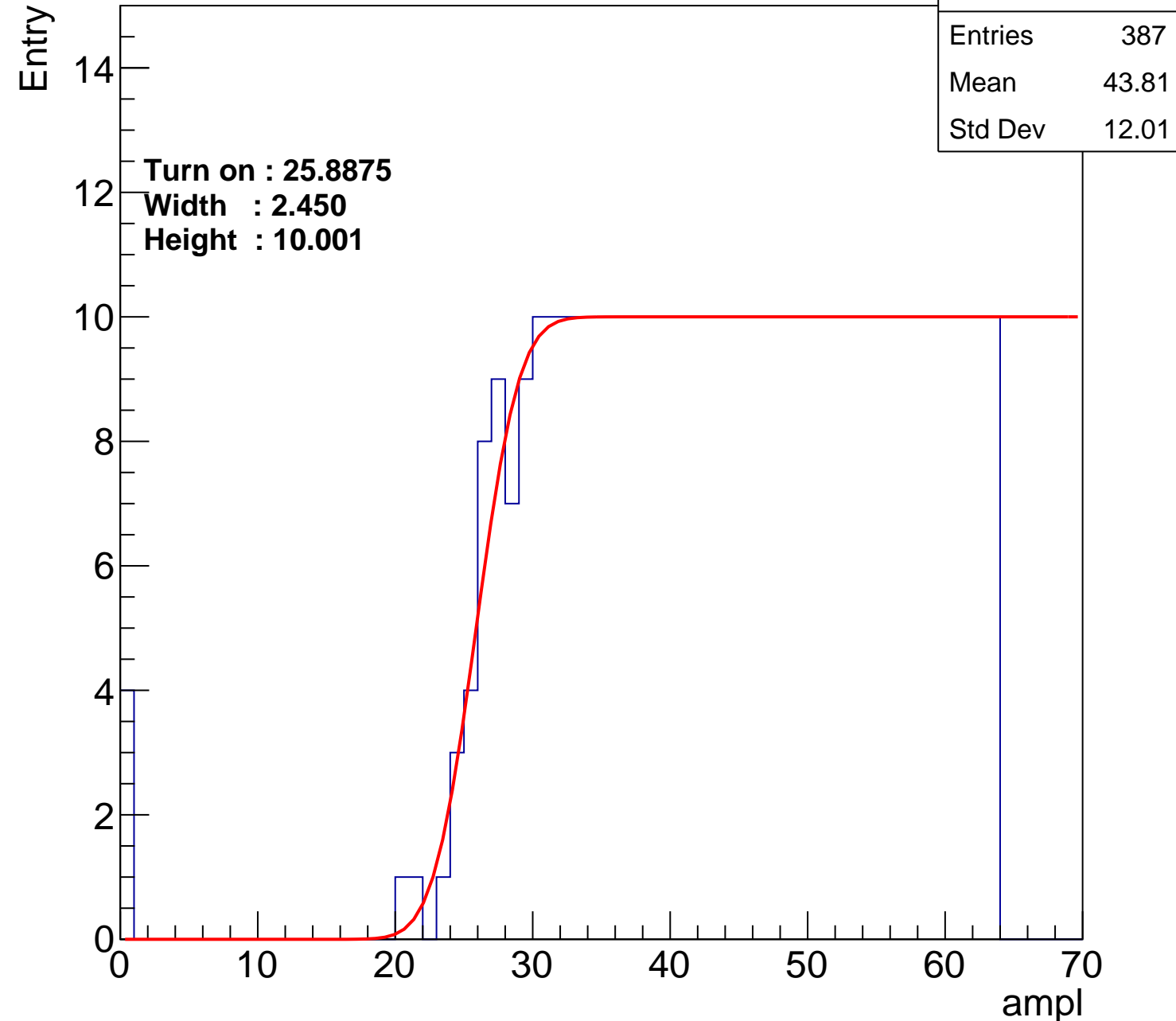
Width : 2.450

Height : 10.001

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch16

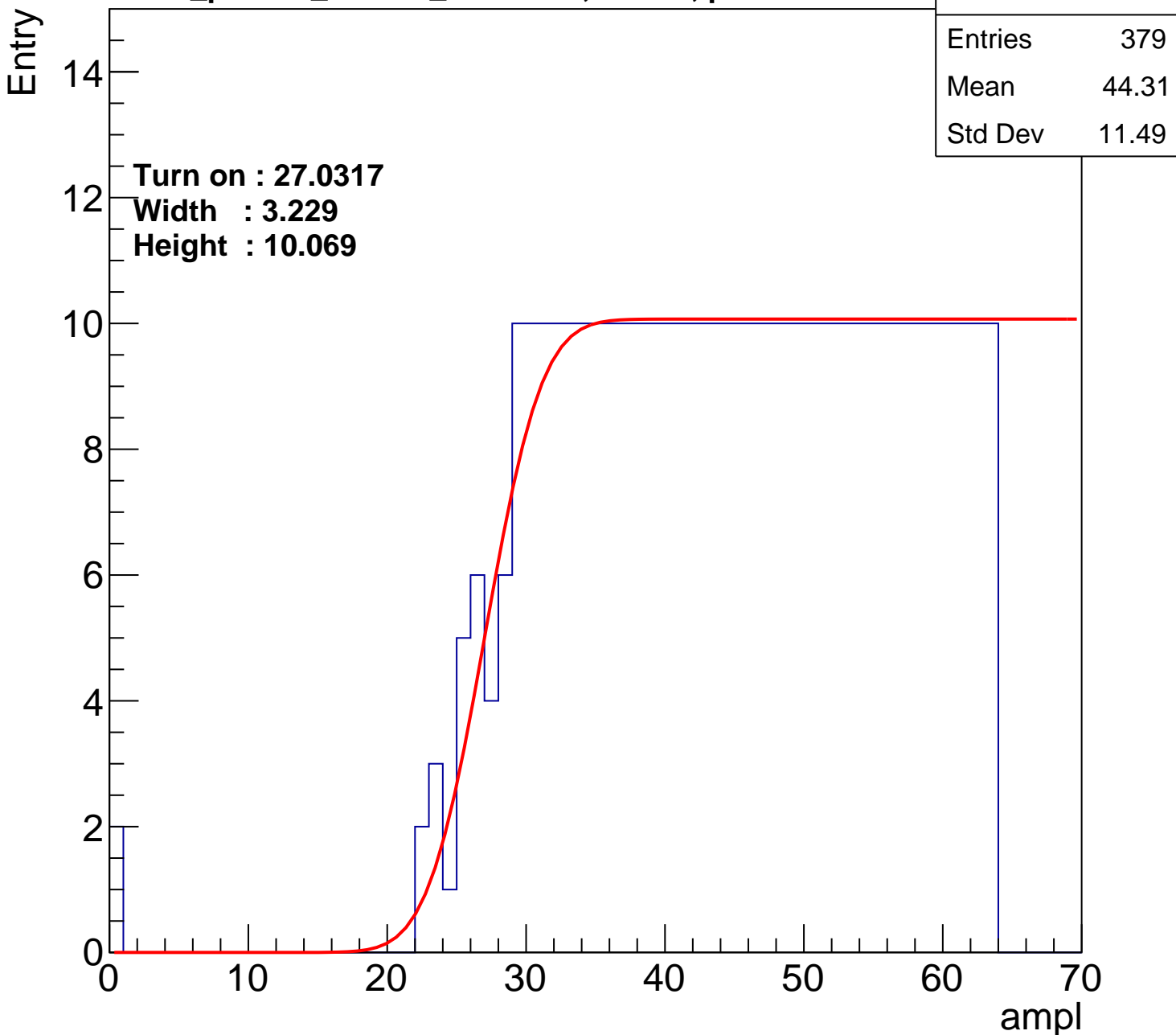
**calib\_packv5\_042523\_0143.root, FC#11, port A2**

**Turn on : 27.0317**

**Width : 3.229**

**Height : 10.069**

Entries	379
Mean	44.31
Std Dev	11.49



# B1L102S, U2-ch17

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	366
Mean	44.93
Std Dev	11.18

Turn on : 27.5285

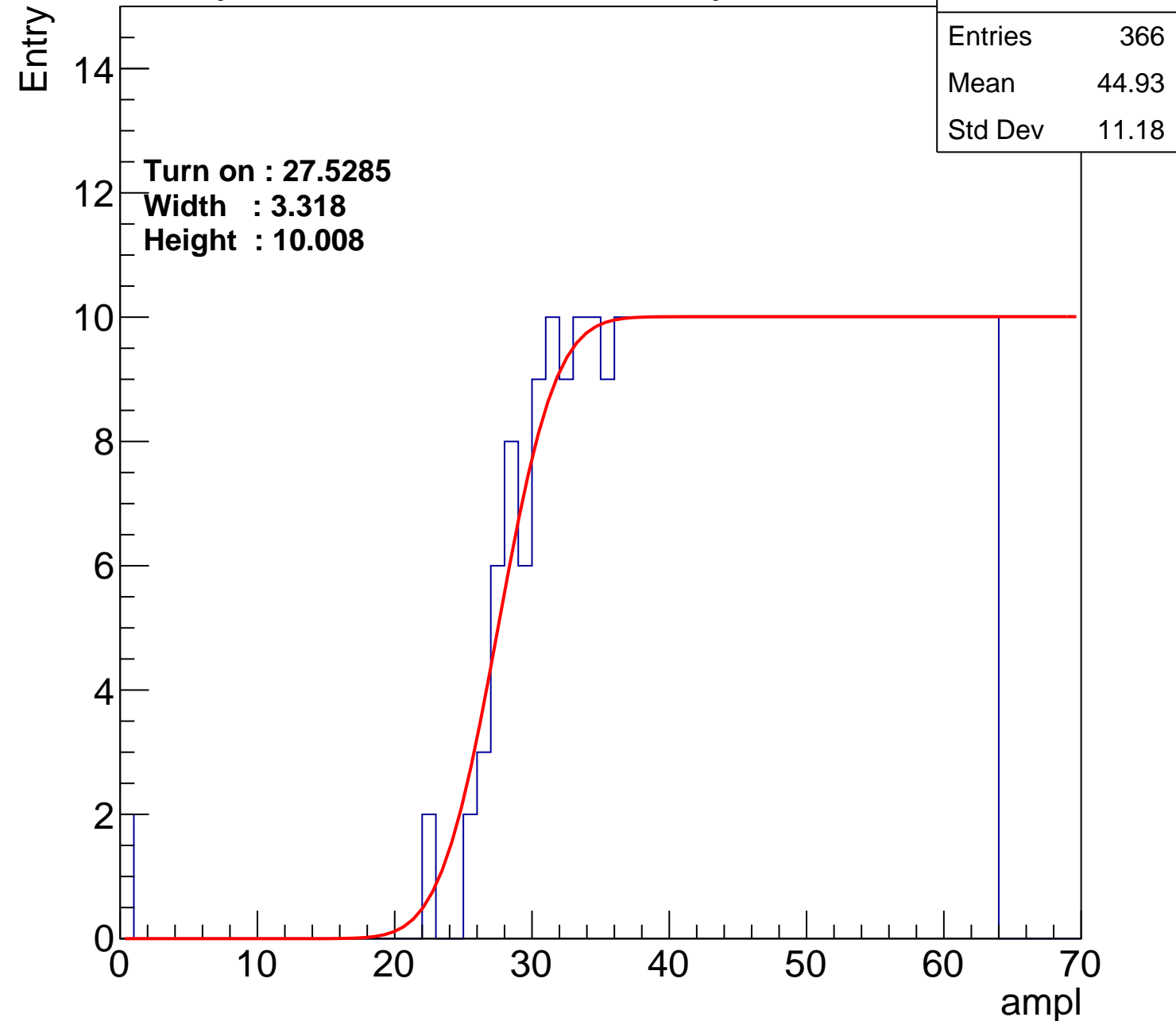
Width : 3.318

Height : 10.008

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch18

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	367
Mean	44.98
Std Dev	10.96

Turn on : 26.9514

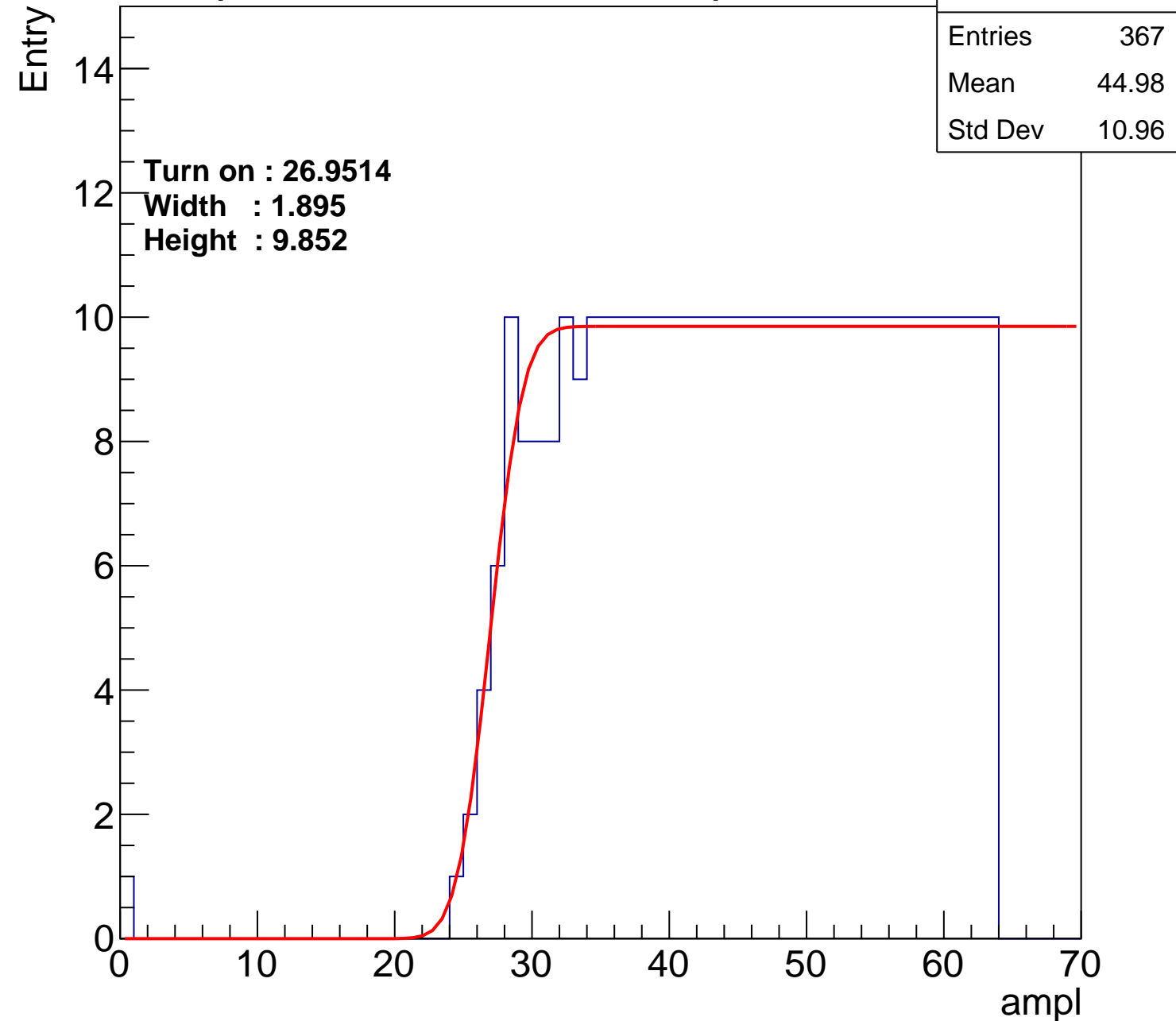
Width : 1.895

Height : 9.852

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch19

calib\_packv5\_042523\_0143.root, FC#11, port A2

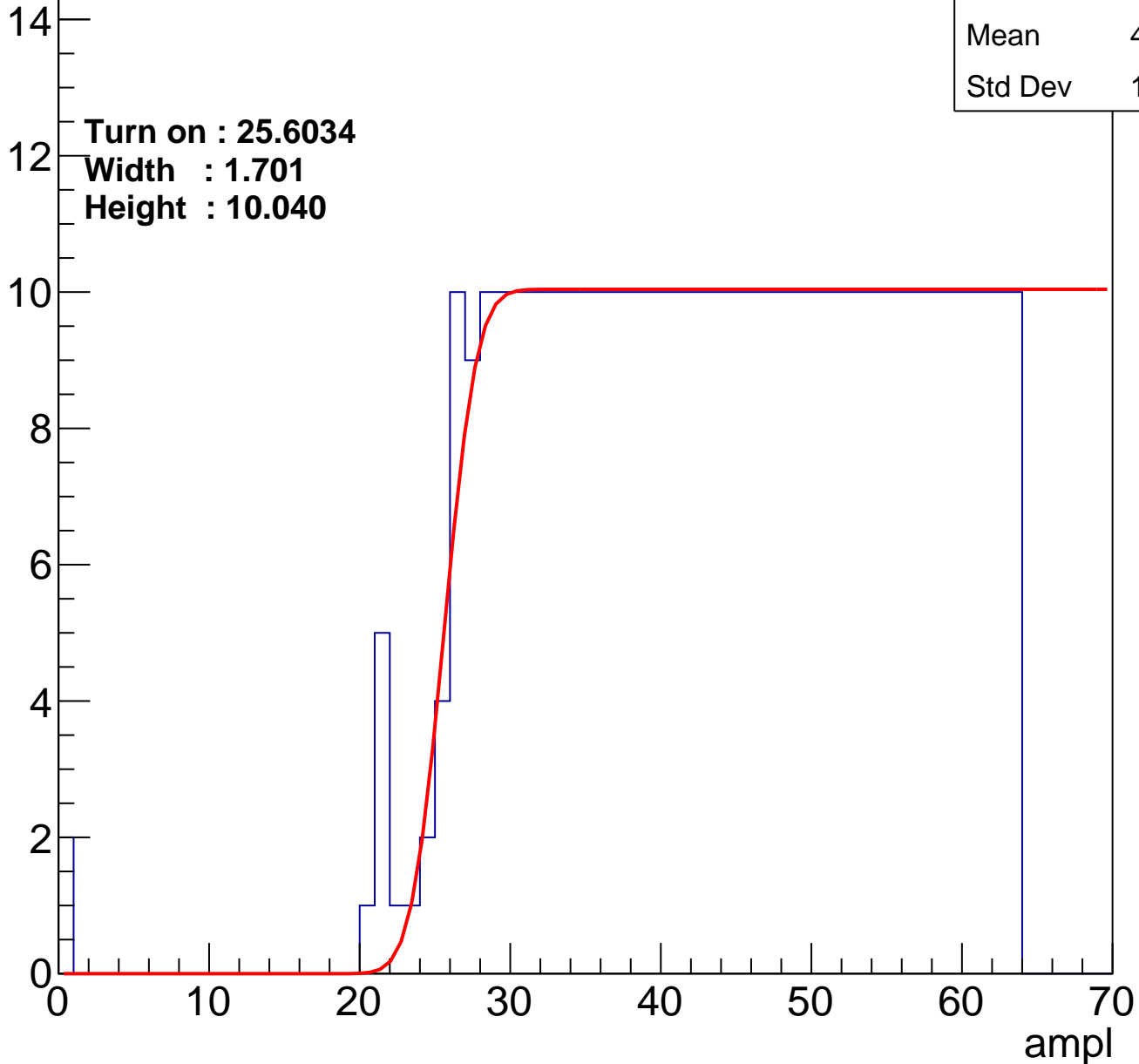
Entries	395
Mean	43.55
Std Dev	11.87

Turn on : 25.6034

Width : 1.701

Height : 10.040

Entry



# B1L102S, U2-ch20

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	394
Mean	43.33
Std Dev	12.44

Turn on : 25.2666

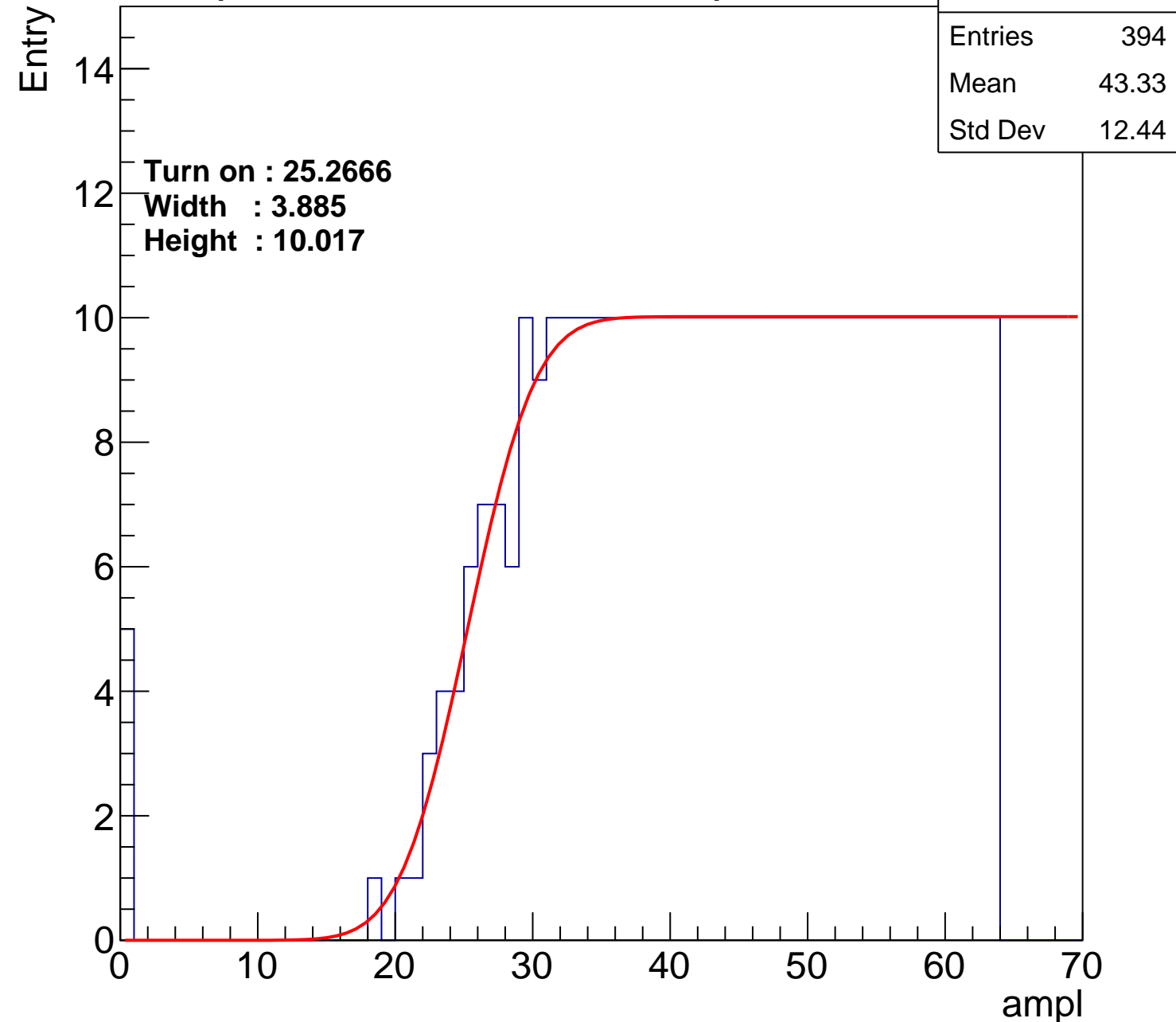
Width : 3.885

Height : 10.017

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch21

calib\_packv5\_042523\_0143.root, FC#11, port A2

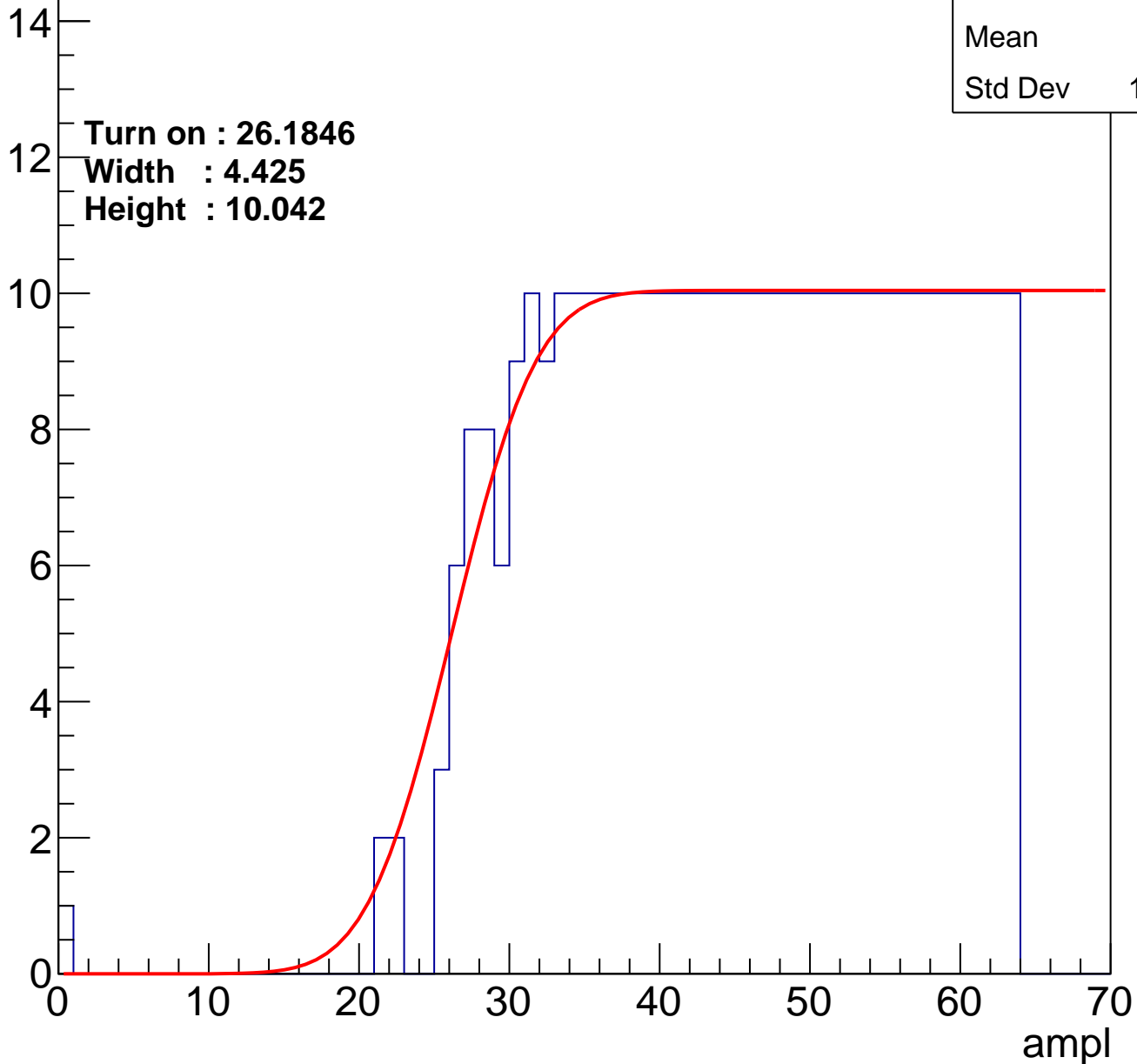
Entries	374
Mean	44.6
Std Dev	11.22

Turn on : 26.1846

Width : 4.425

Height : 10.042

Entry



# B1L102S, U2-ch22

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	375
Mean	44.56
Std Dev	11.22

**Turn on : 26.9109**

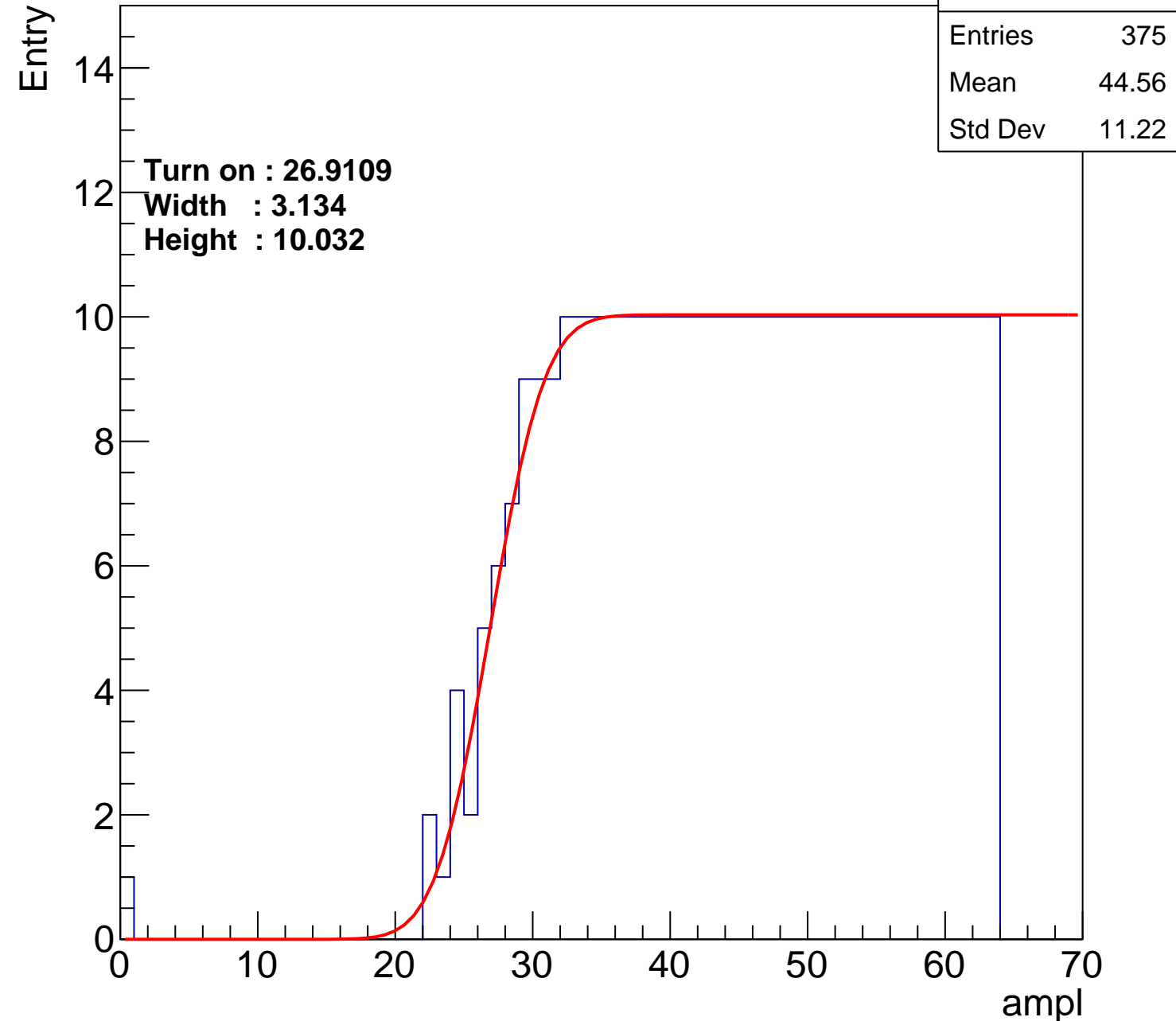
**Width : 3.134**

**Height : 10.032**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L102S, U2-ch23

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	383
Mean	44.01
Std Dev	11.83

Turn on : 27.2799

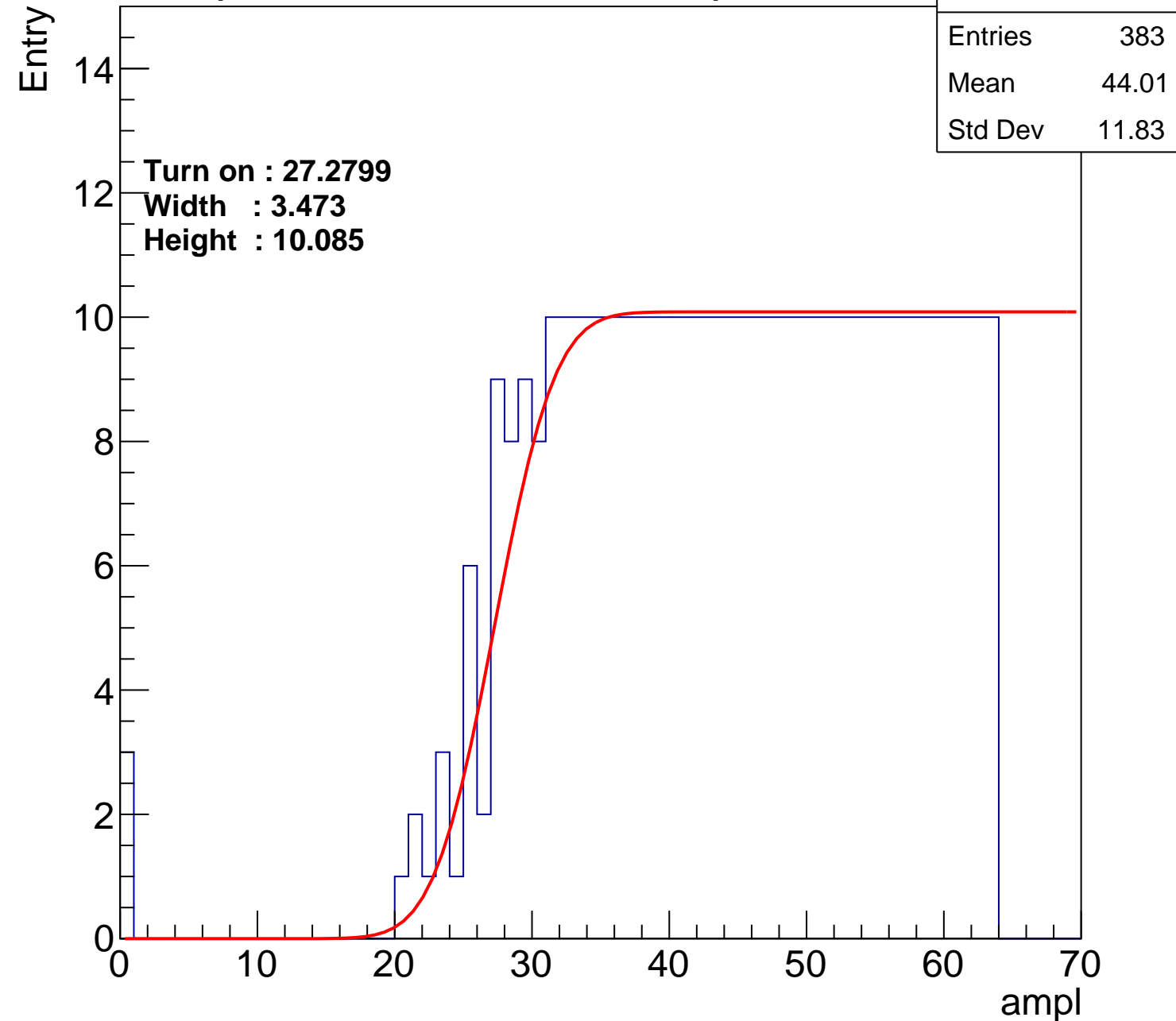
Width : 3.473

Height : 10.085

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch24

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	400
Mean	43.12
Std Dev	12.45

Turn on : 24.8118

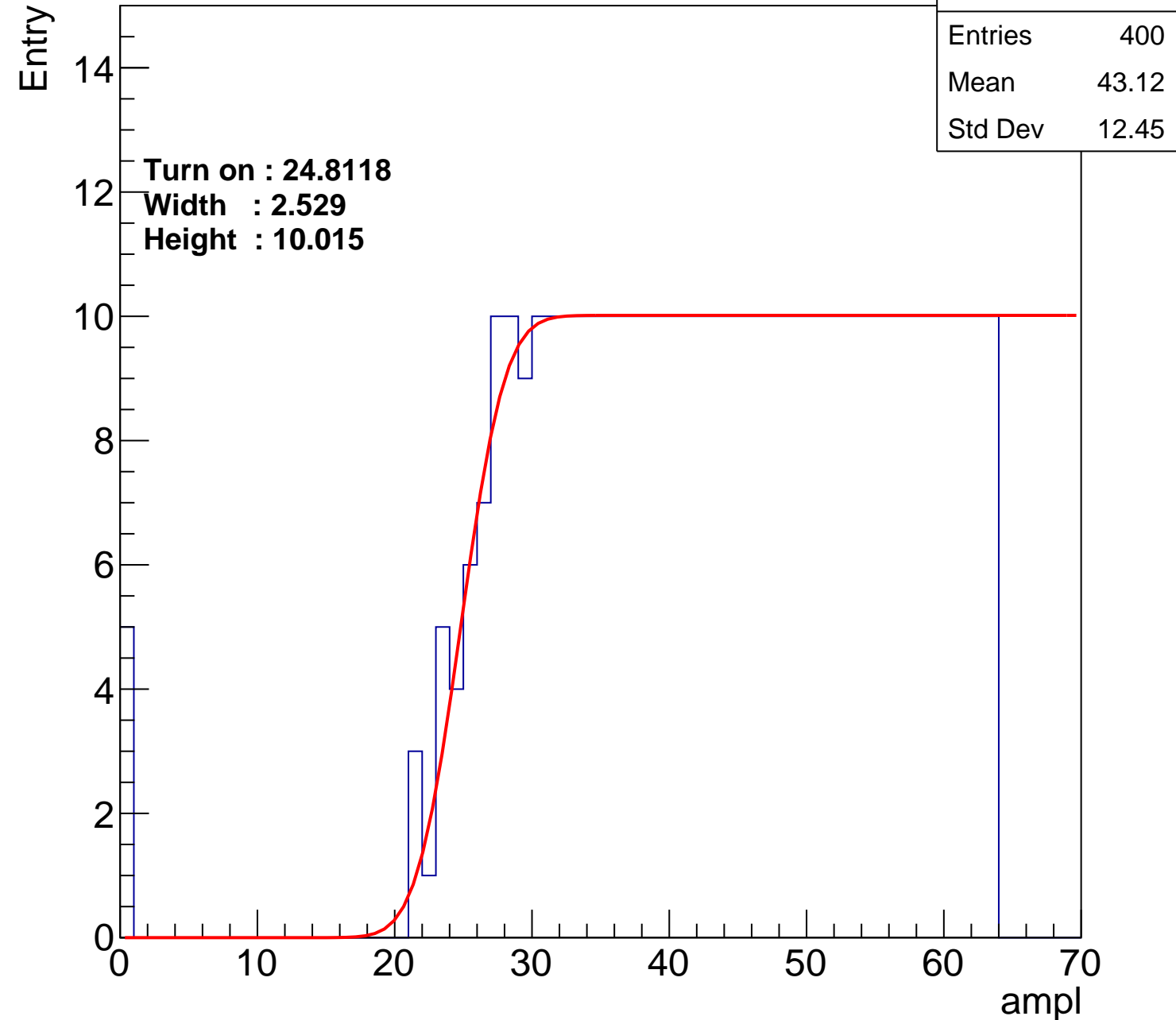
Width : 2.529

Height : 10.015

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch25

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	377
Mean	44.37
Std Dev	11.59

Turn on : 27.0901

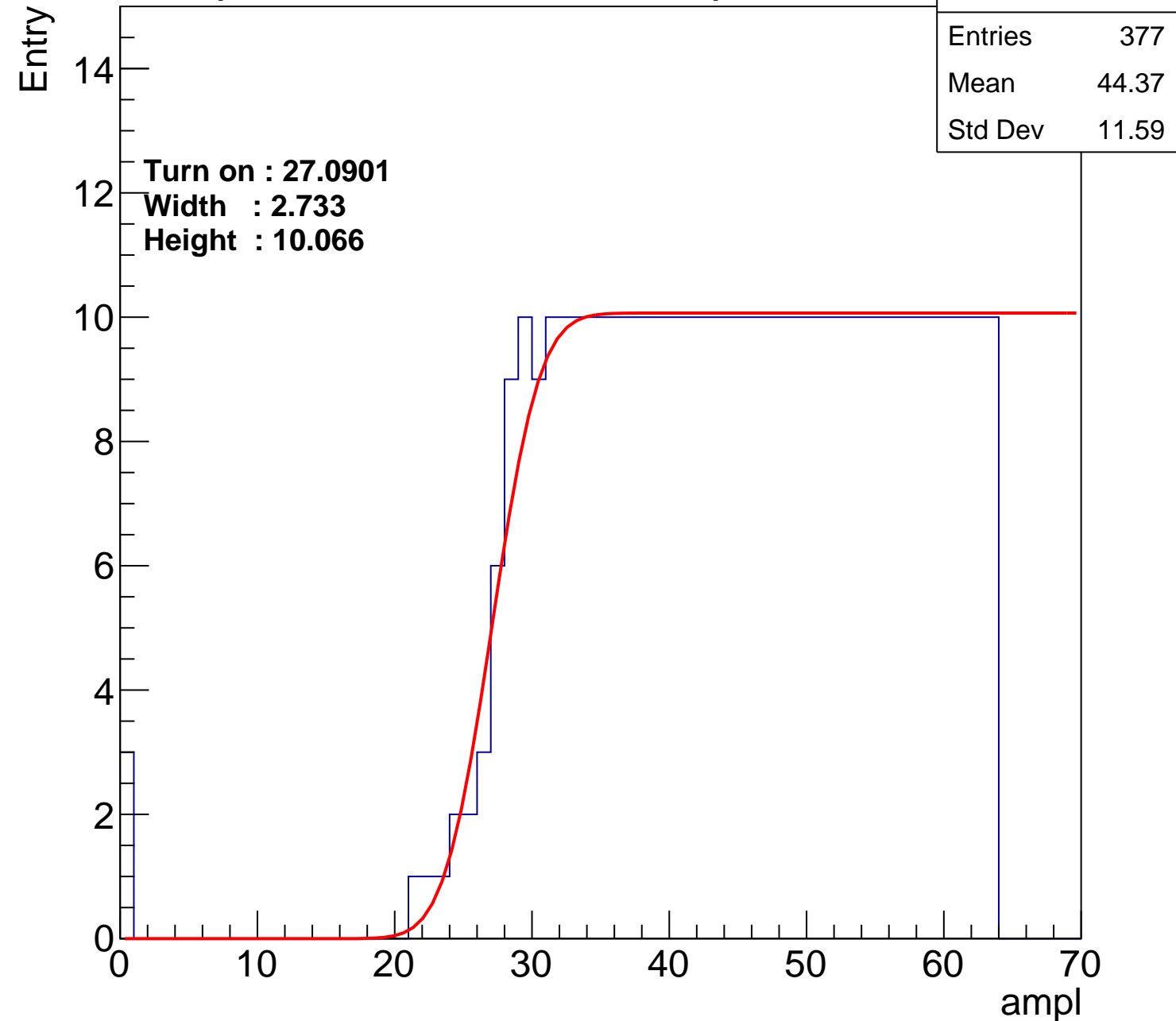
Width : 2.733

Height : 10.066

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch26

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	382
Mean	44.04
Std Dev	11.9

**Turn on : 26.3946**

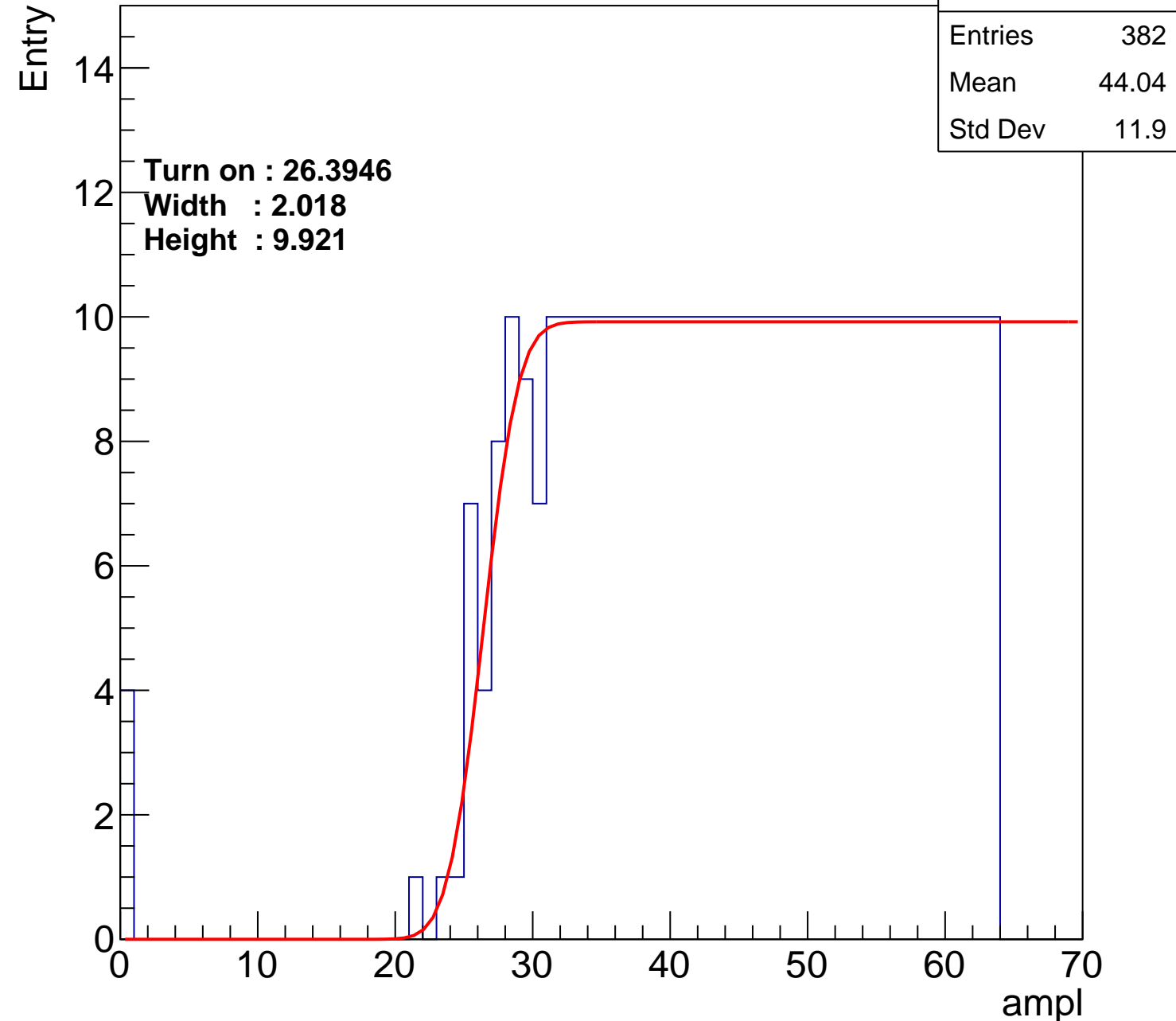
**Width : 2.018**

**Height : 9.921**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch27

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	387
Mean	43.86
Std Dev	11.86

Turn on : 25.6704

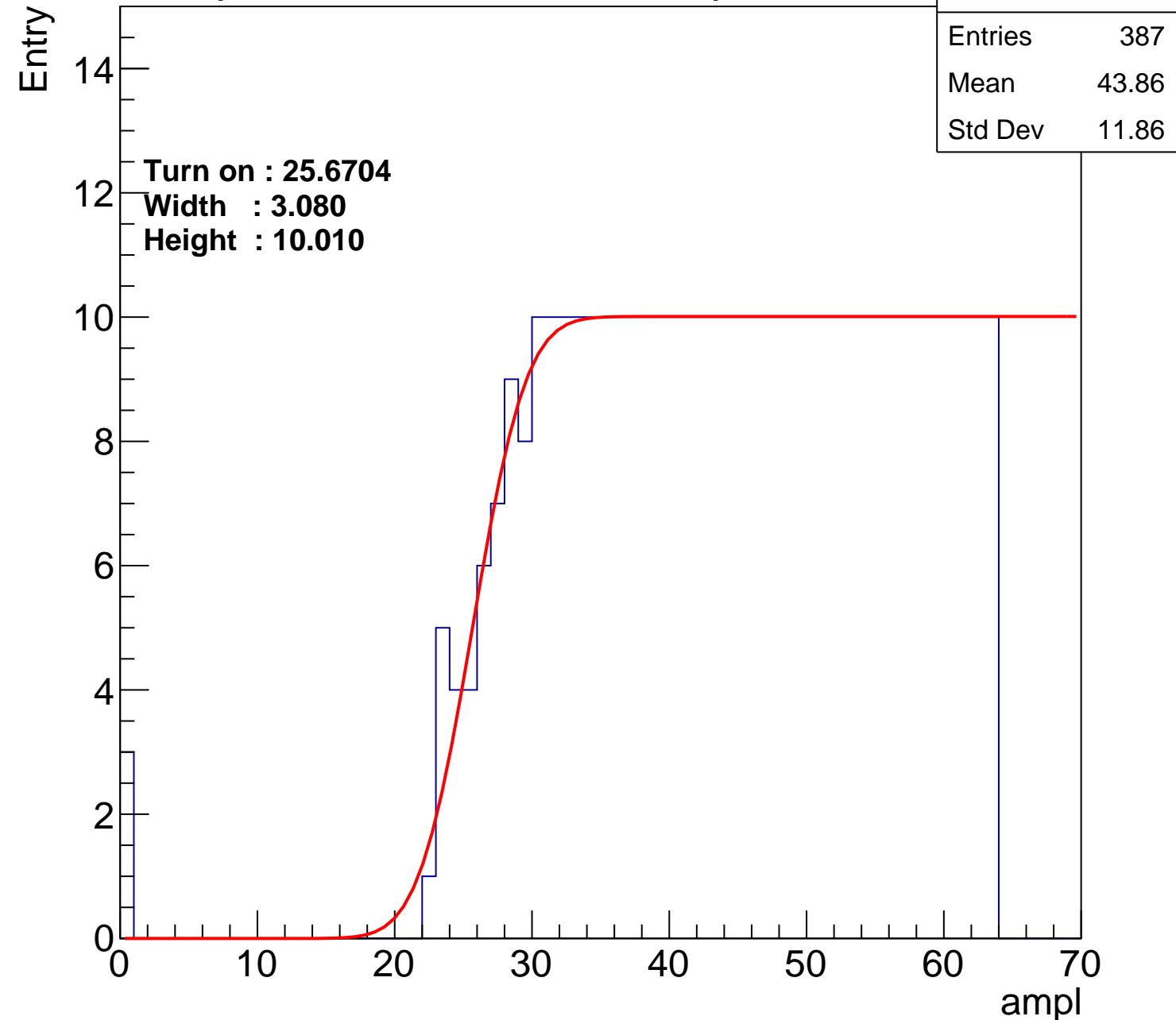
Width : 3.080

Height : 10.010

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch28

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	389
Mean	43.92
Std Dev	11.52

Turn on : 25.9524

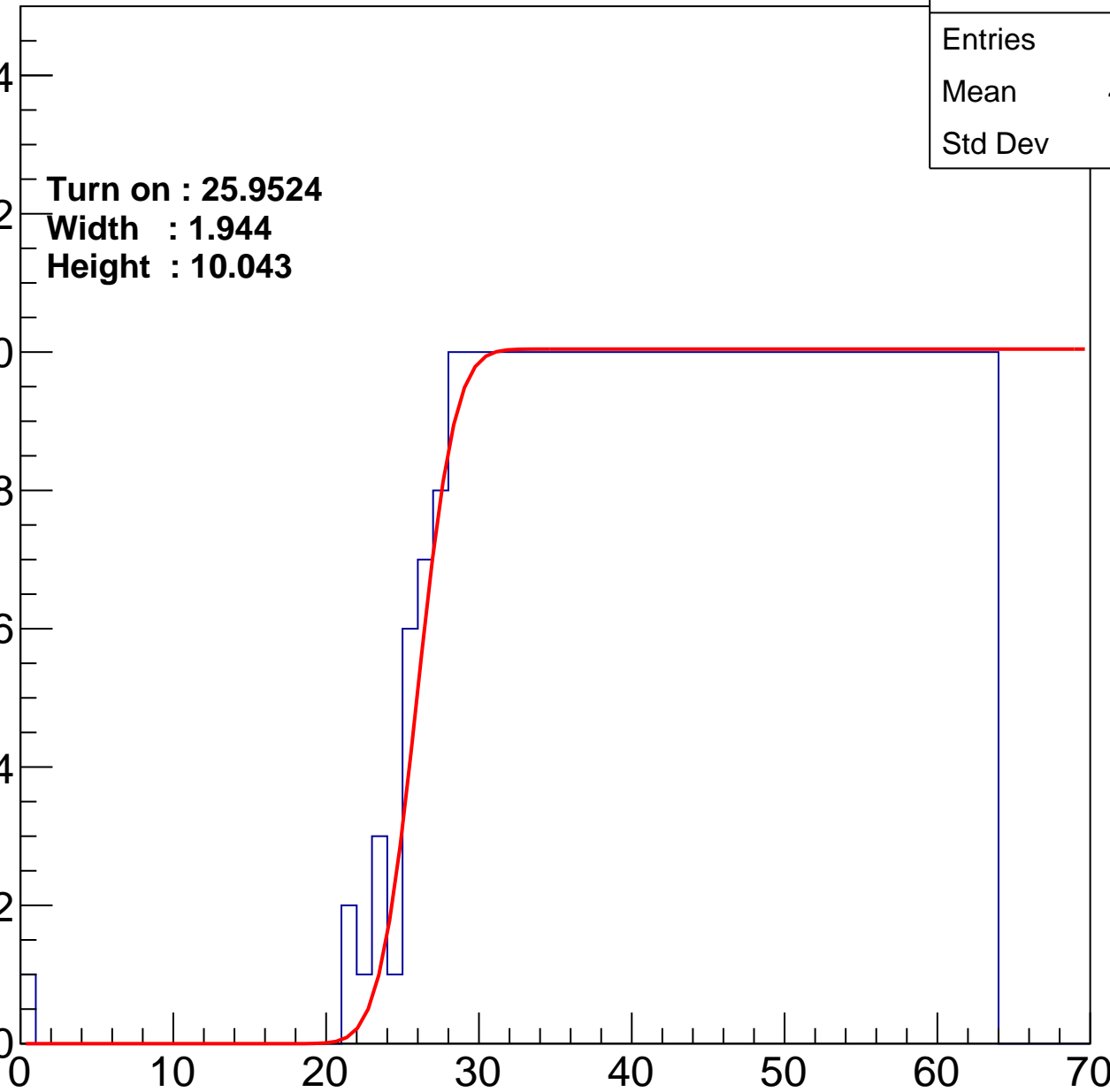
Width : 1.944

Height : 10.043

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch29

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	397
Mean	43.42
Std Dev	11.97

**Turn on : 24.8757**

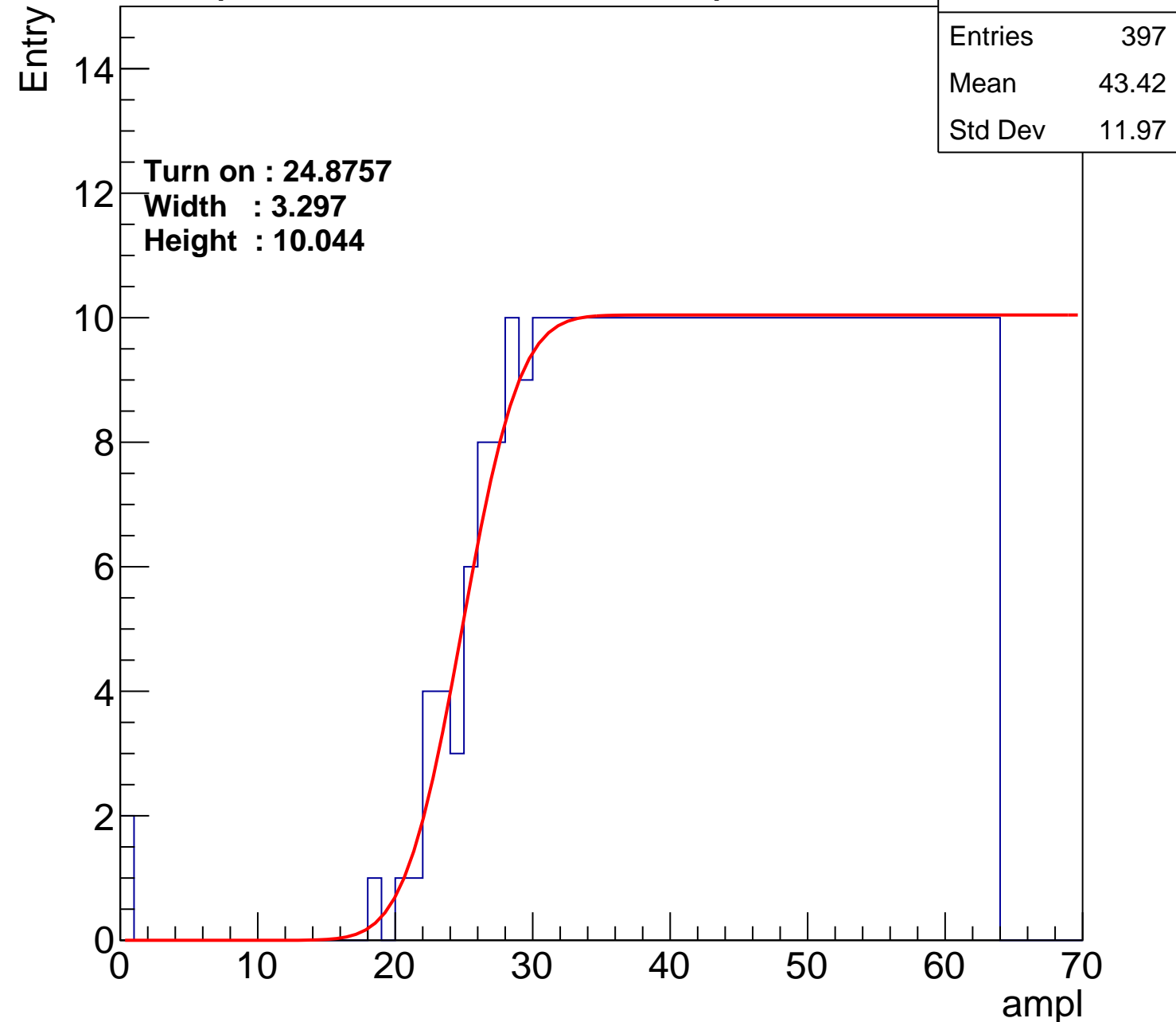
**Width : 3.297**

**Height : 10.044**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch30

calib\_packv5\_042523\_0143.root, FC#11, port A2

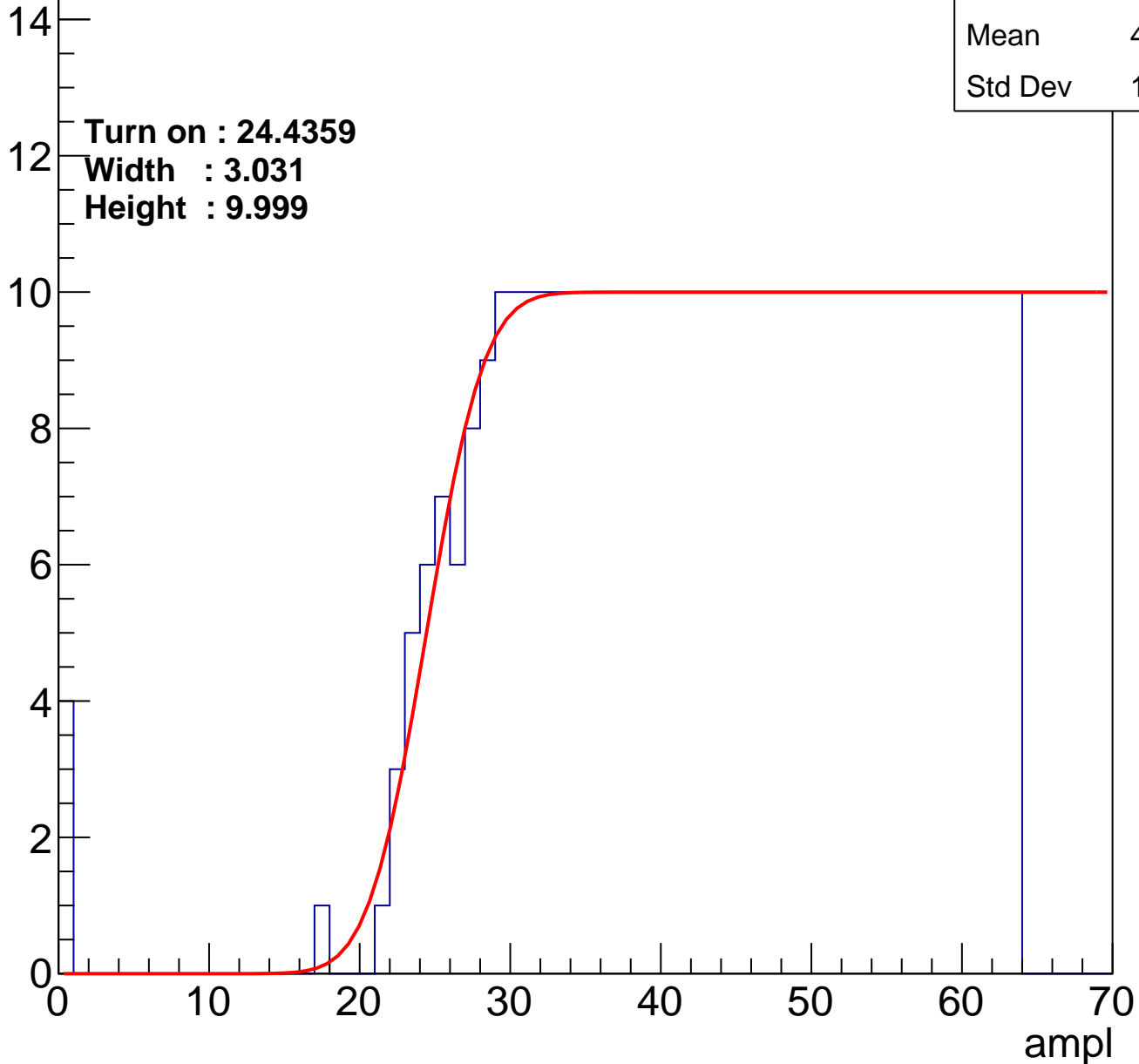
Entries	400
Mean	43.16
Std Dev	12.35

Turn on : 24.4359

Width : 3.031

Height : 9.999

Entry





# B1L102S, U2-ch31

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	400
Mean	43.13
Std Dev	12.38

Turn on : 24.0646

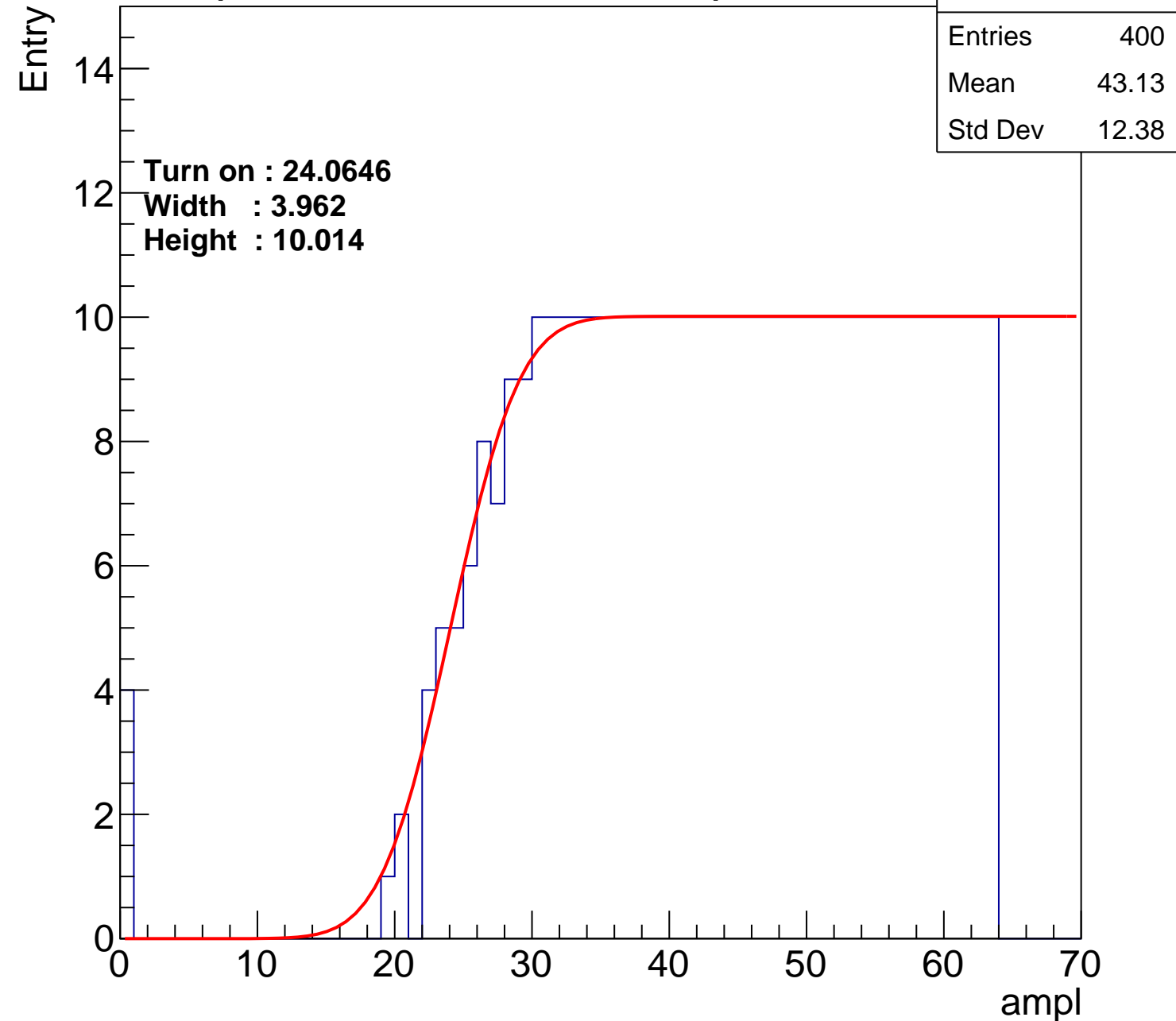
Width : 3.962

Height : 10.014

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch32

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	388
Mean	43.87
Std Dev	11.72

Turn on : 25.5756

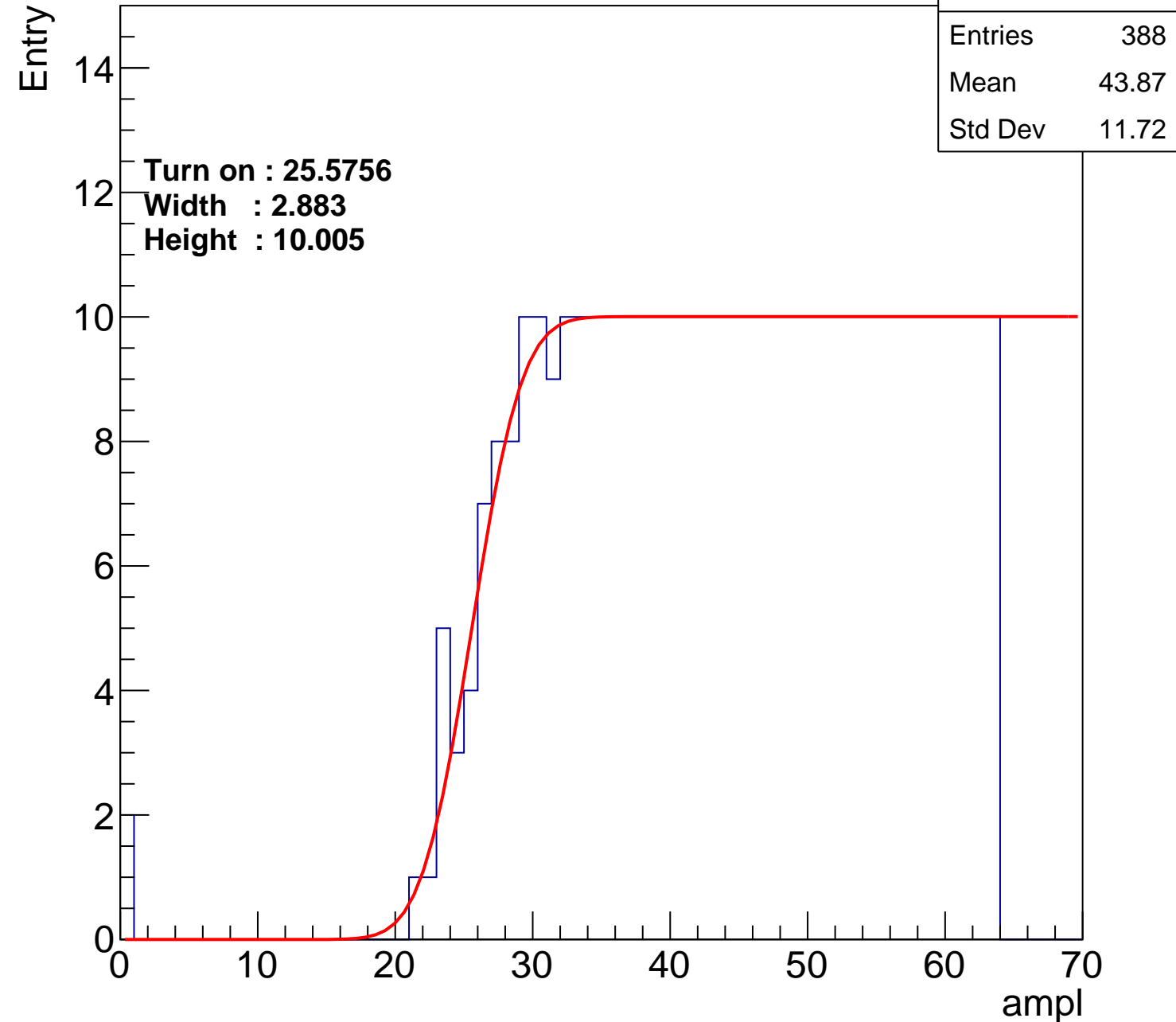
Width : 2.883

Height : 10.005

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch33

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	392
Mean	43.67
Std Dev	11.83

Turn on : 25.3710

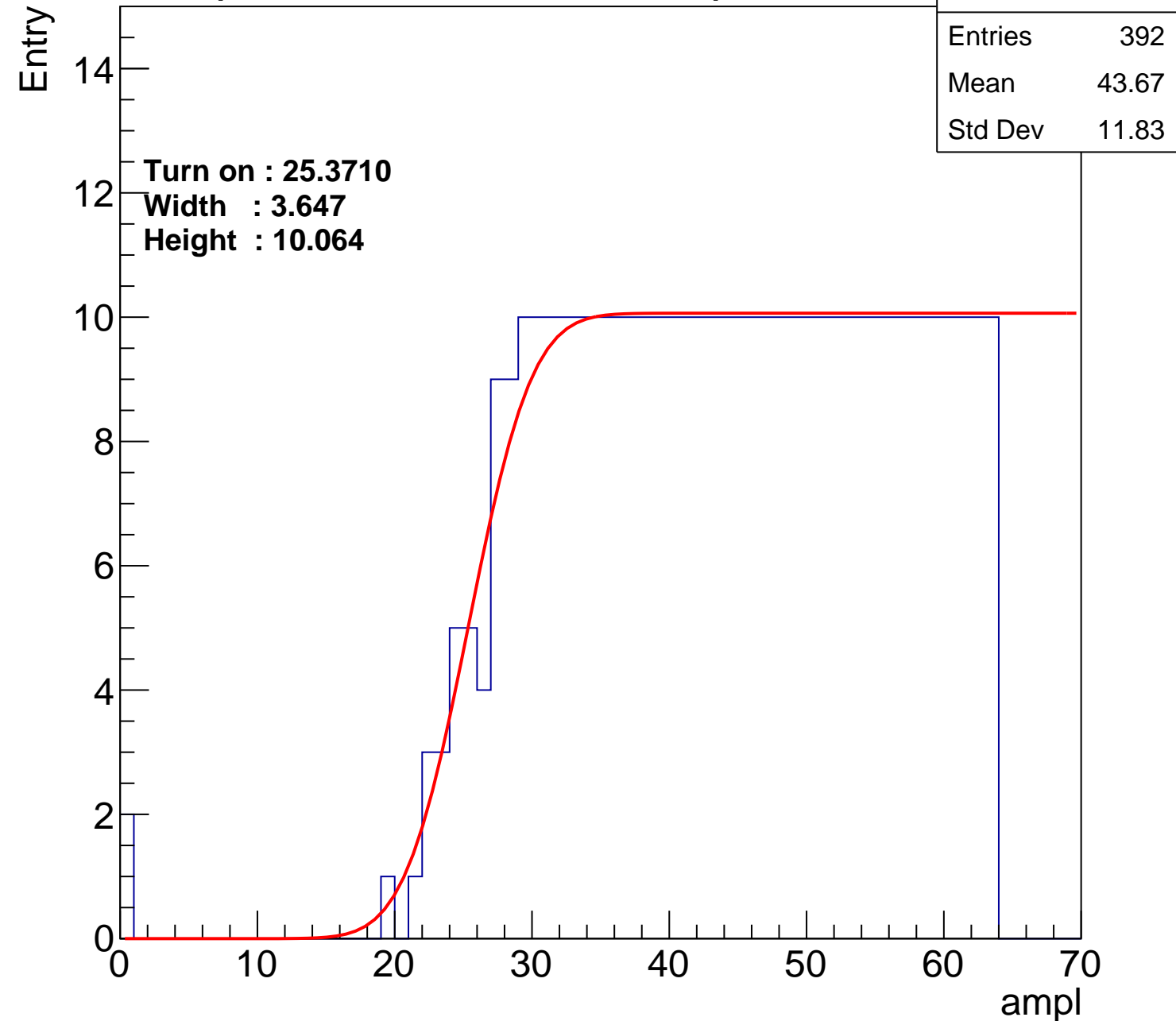
Width : 3.647

Height : 10.064

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch34

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	385
Mean	44.06
Std Dev	11.5

Turn on : 25.8096

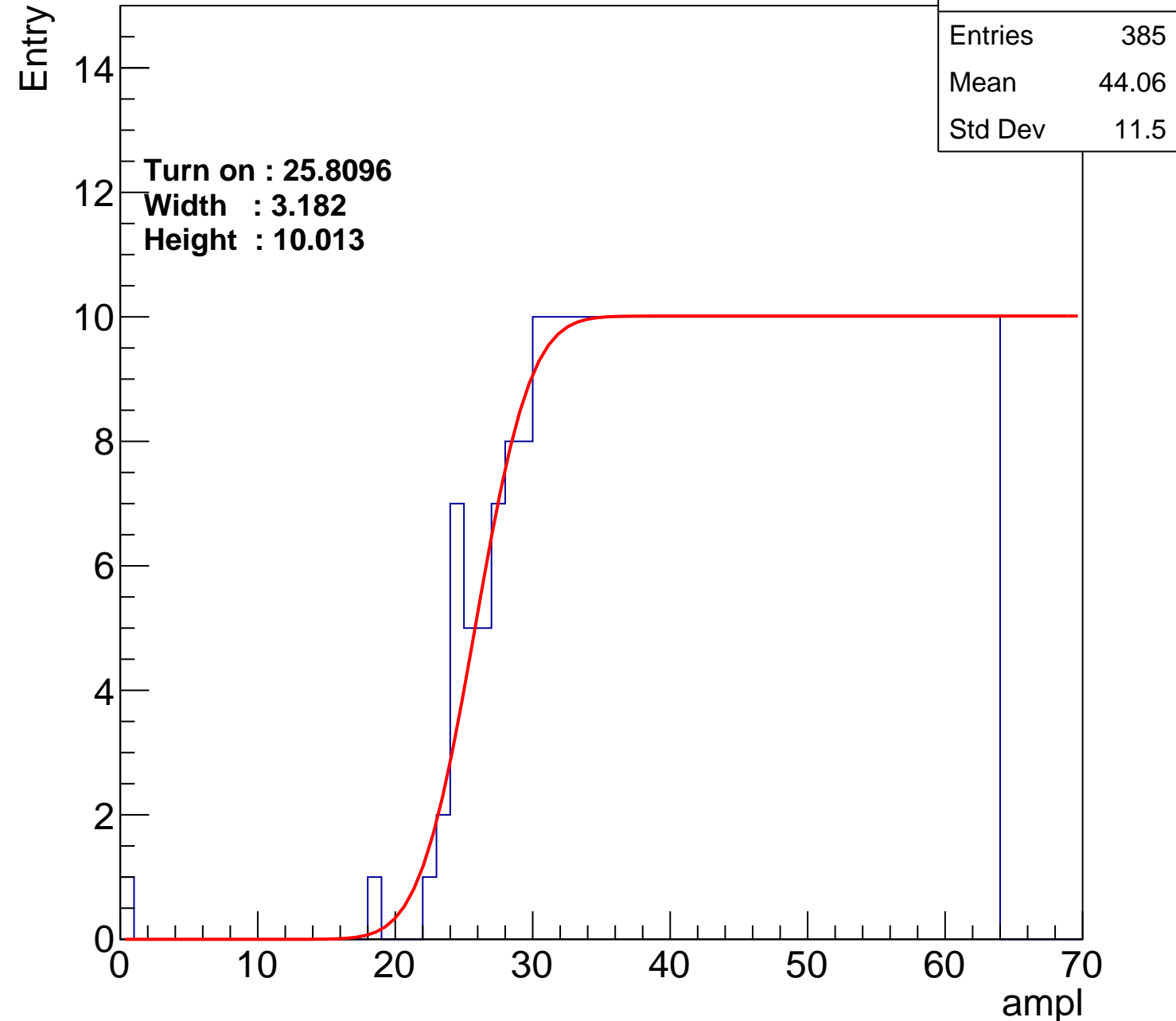
Width : 3.182

Height : 10.013

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch35

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	370
Mean	44.83
Std Dev	11.06

Turn on : 27.3583

Width : 2.972

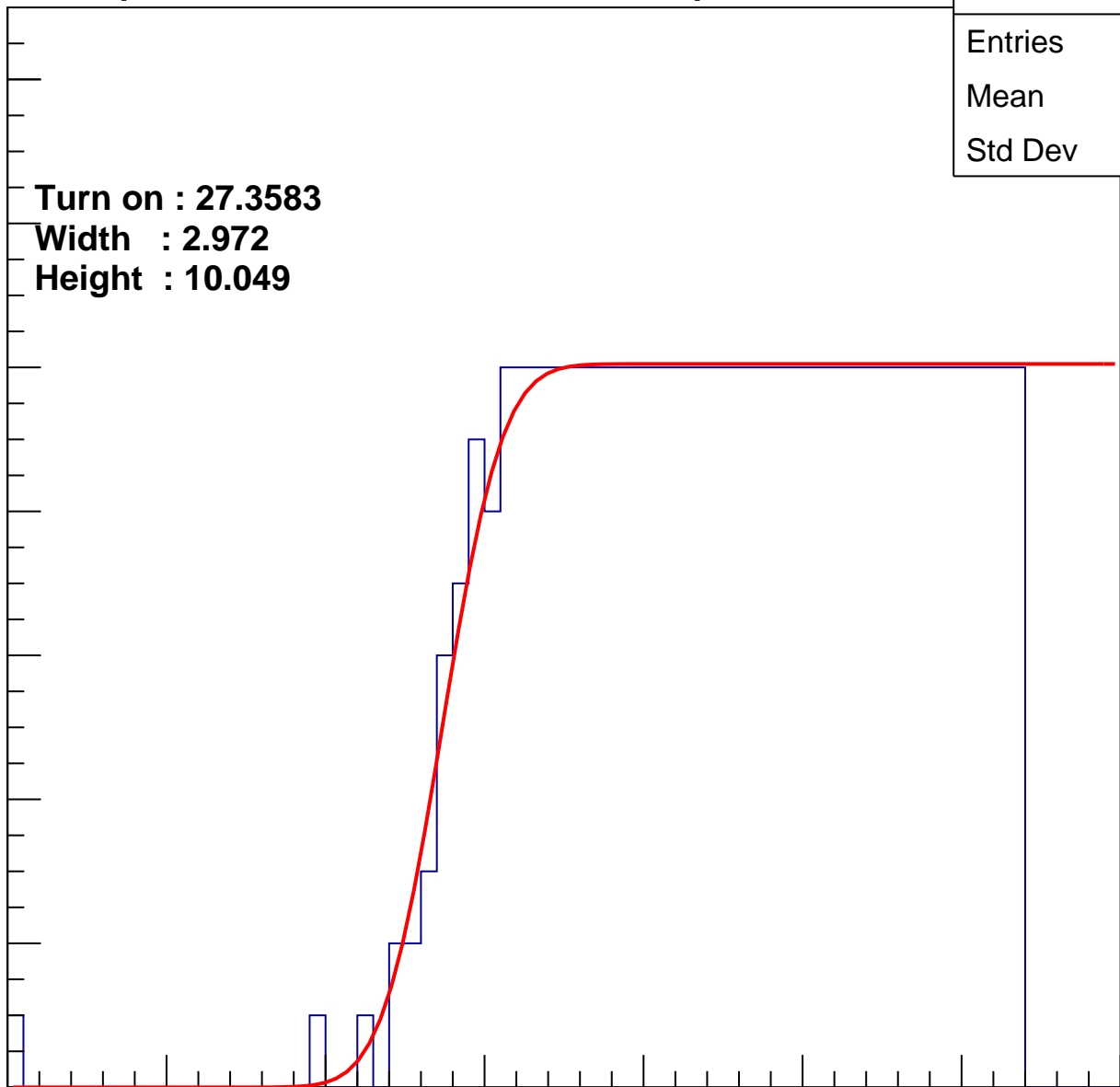
Height : 10.049

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U2-ch36

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	387
Mean	43.85
Std Dev	11.87

Turn on : 25.7546

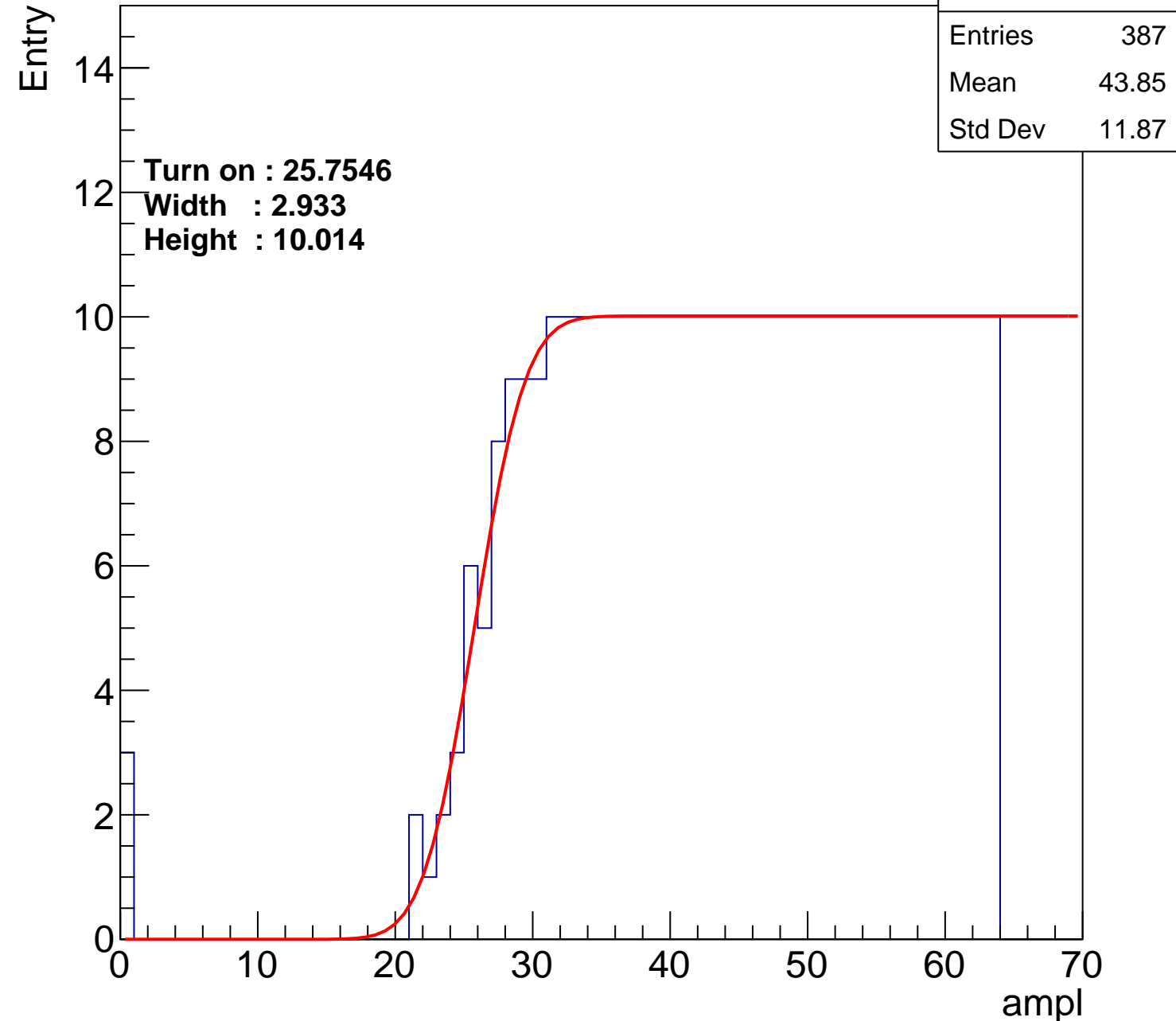
Width : 2.933

Height : 10.014

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch37

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	373
Mean	44.47
Std Dev	11.71

Turn on : 27.8255

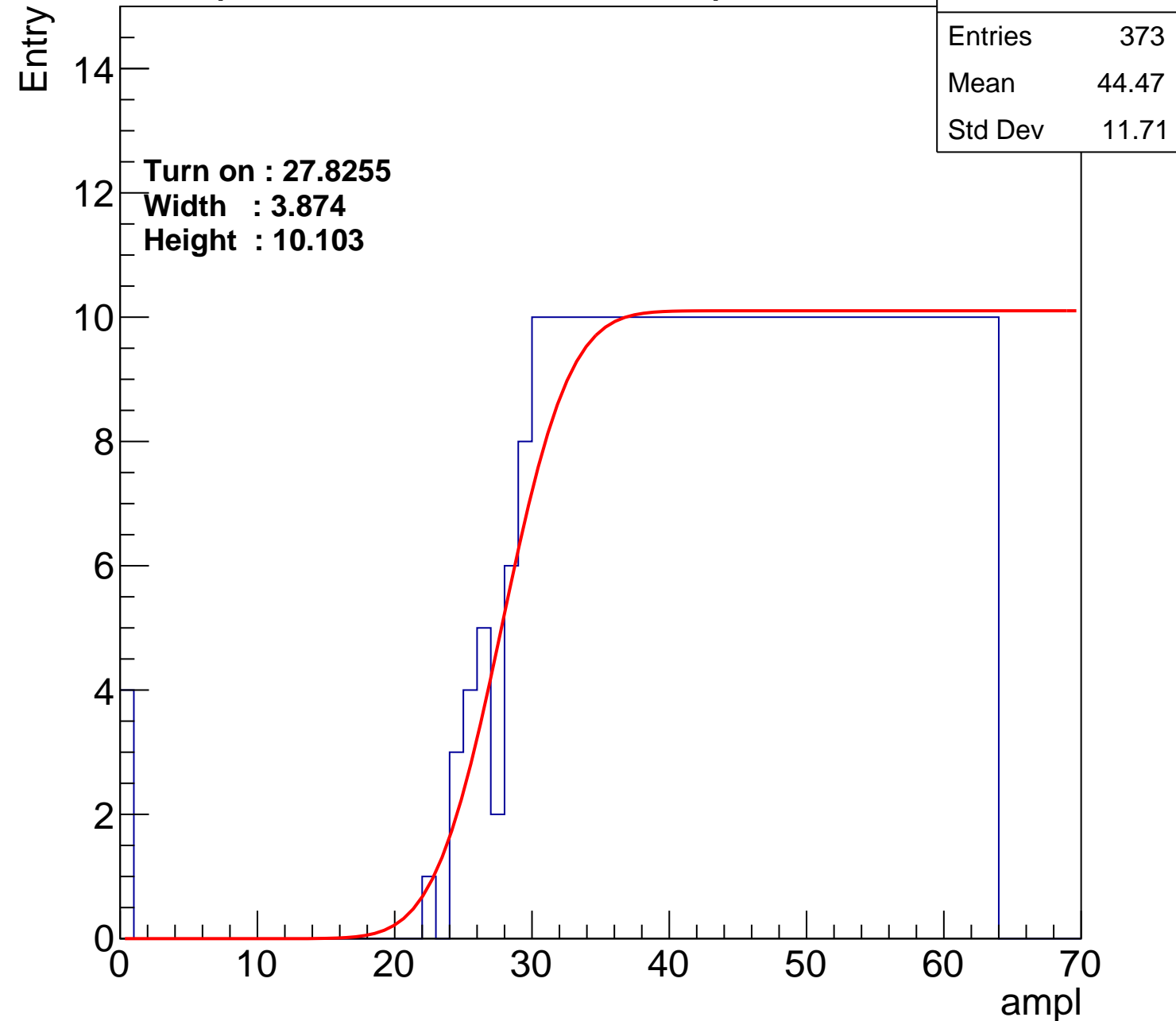
Width : 3.874

Height : 10.103

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch38

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	393
Mean	43.62
Std Dev	11.86

**Turn on : 24.9307**

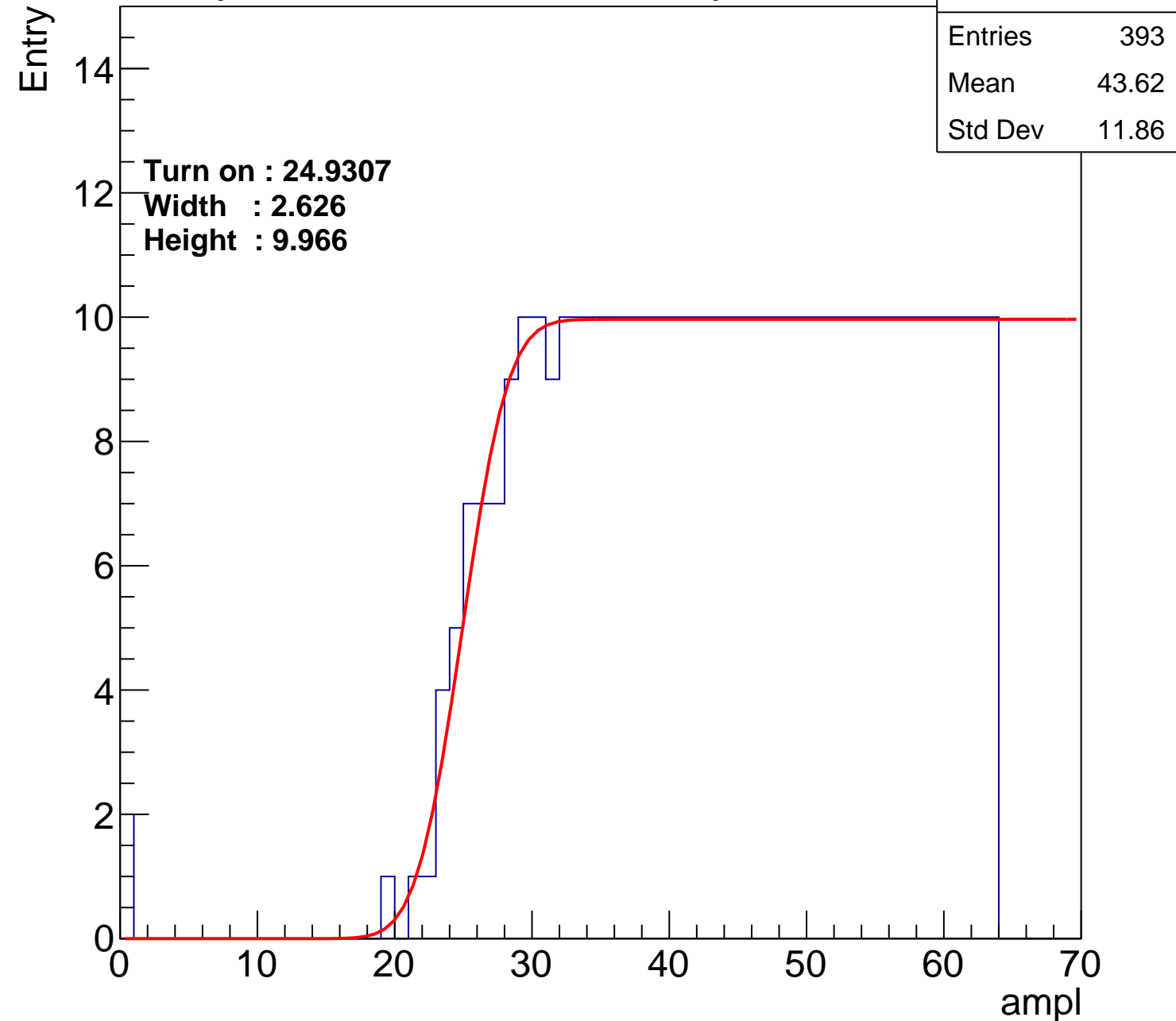
**Width : 2.626**

**Height : 9.966**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L102S, U2-ch39

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	393
Mean	43.45
Std Dev	12.32

Turn on : 25.3829

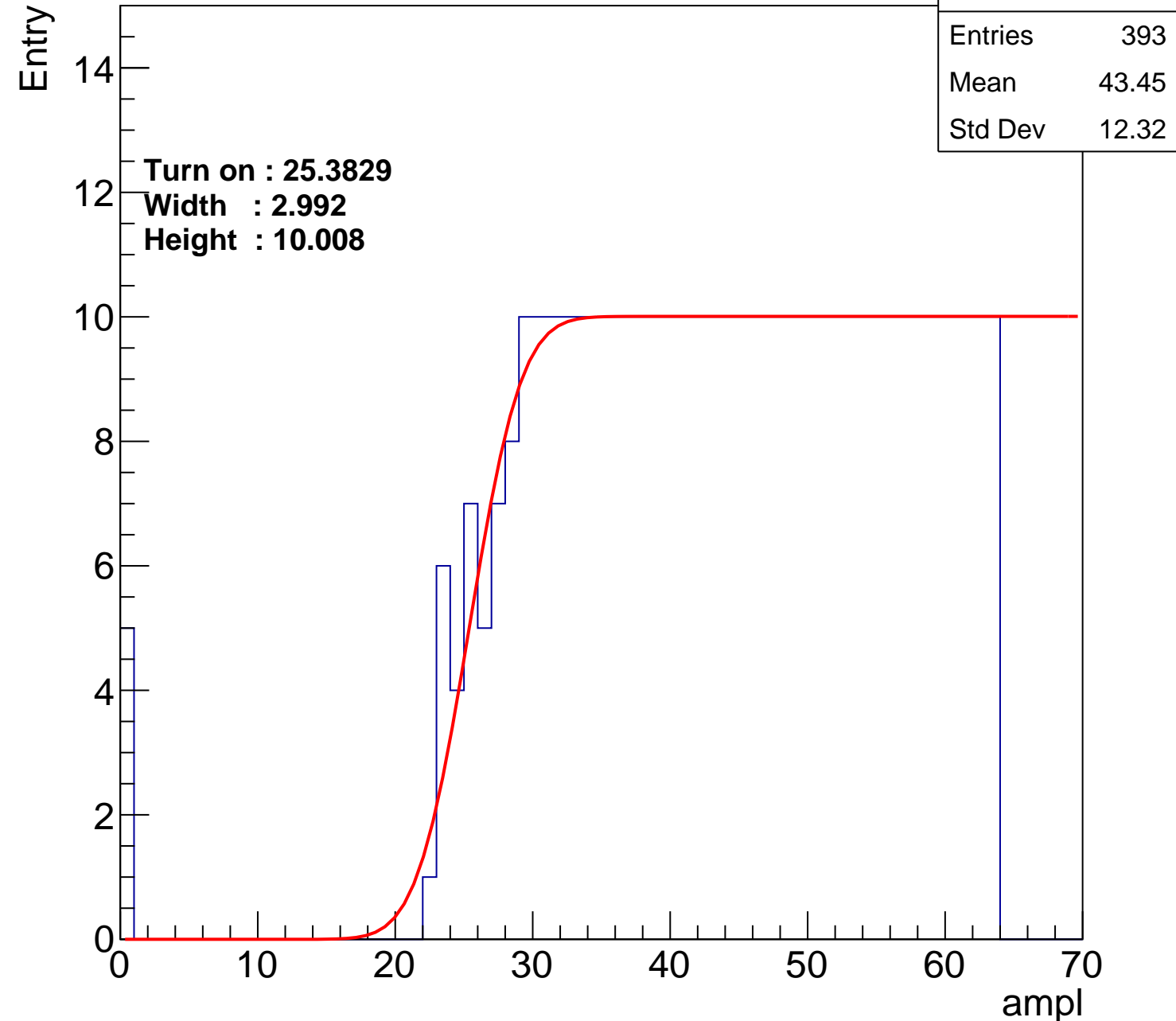
Width : 2.992

Height : 10.008

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch40

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	391
Mean	43.62
Std Dev	12.03

Turn on : 25.0472

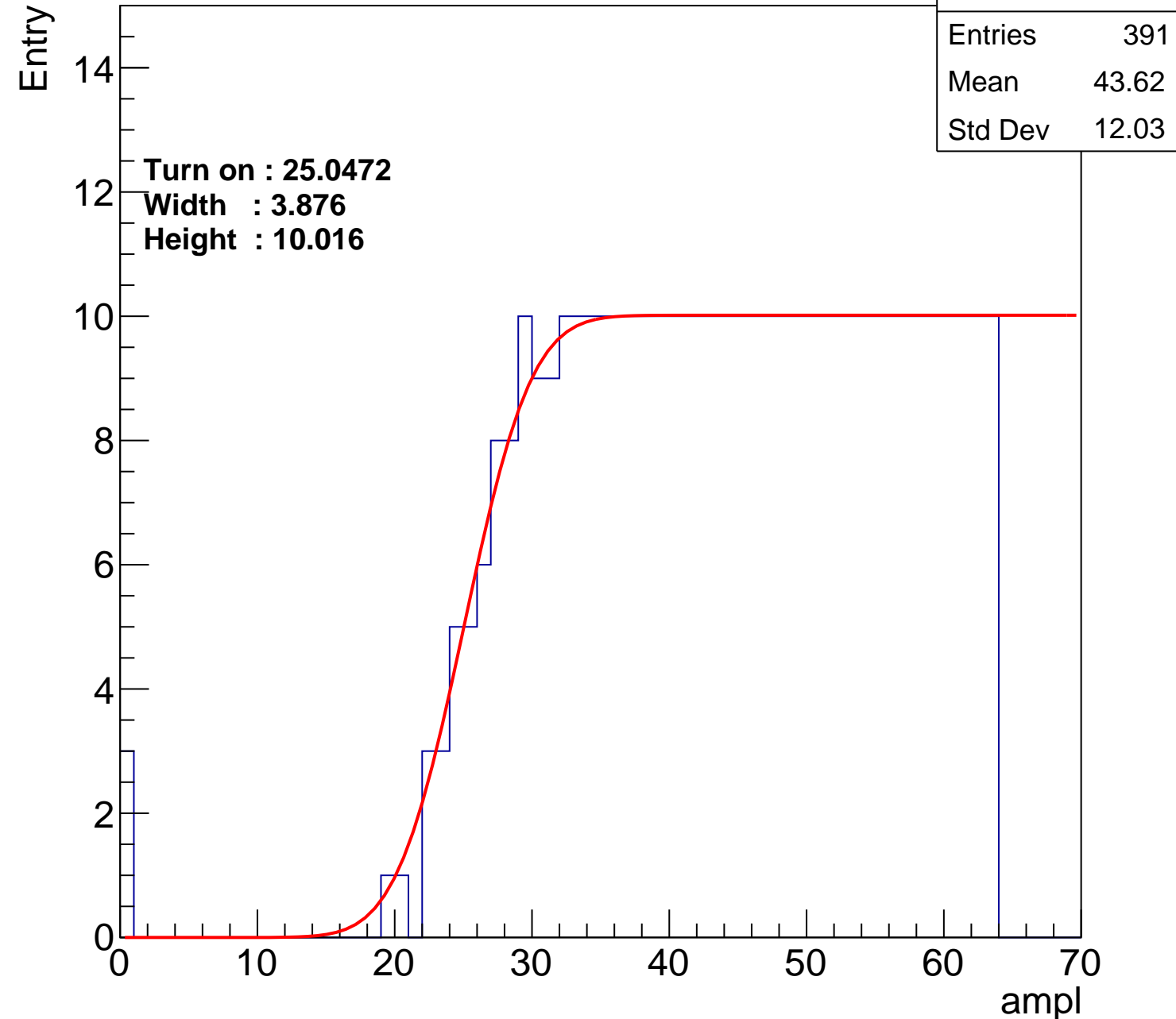
Width : 3.876

Height : 10.016

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch41

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	383
Mean	44.02
Std Dev	11.82

**Turn on : 26.1080**

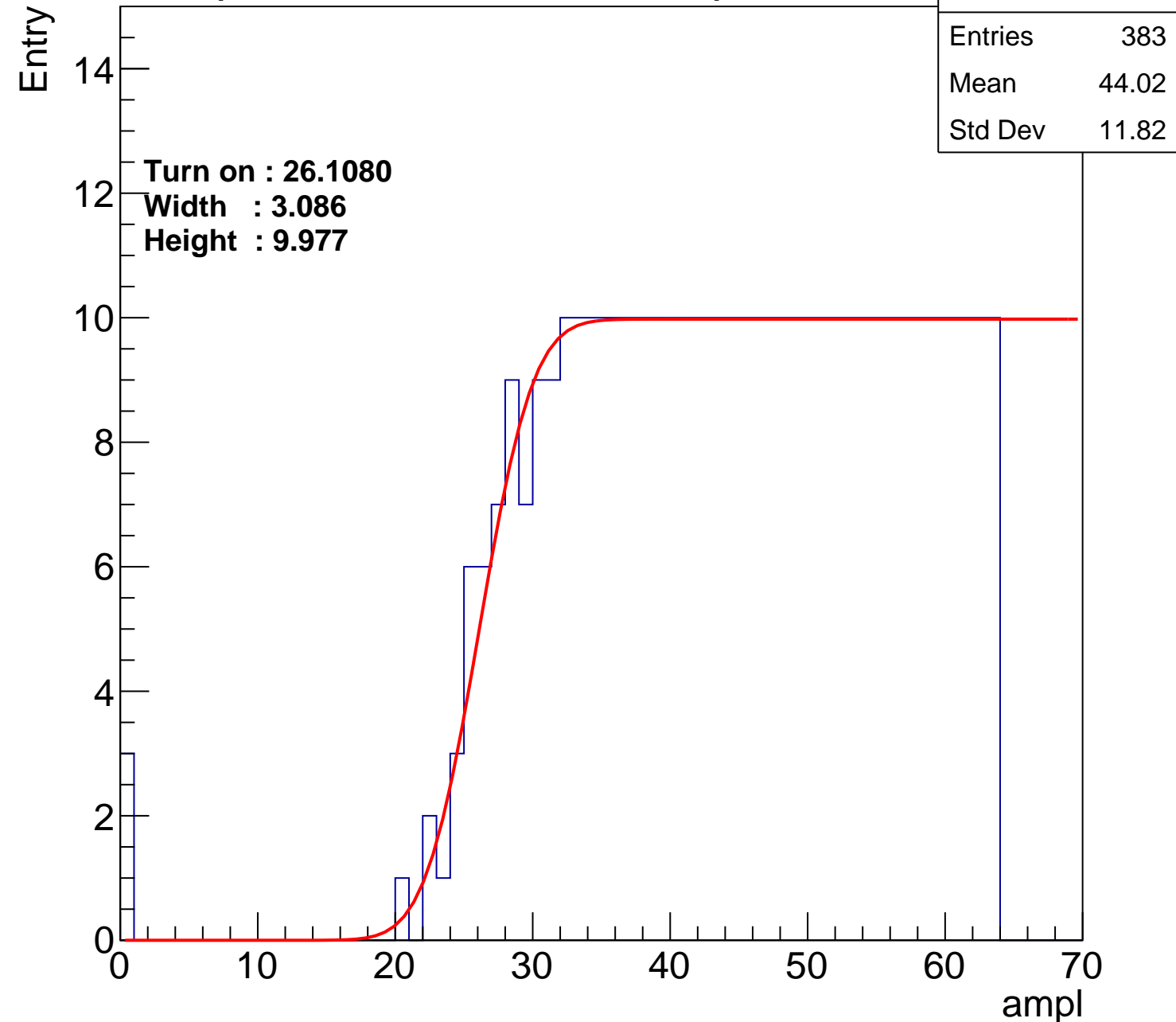
**Width : 3.086**

**Height : 9.977**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch42

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	389
Mean	43.79
Std Dev	11.78

Turn on : 25.3640

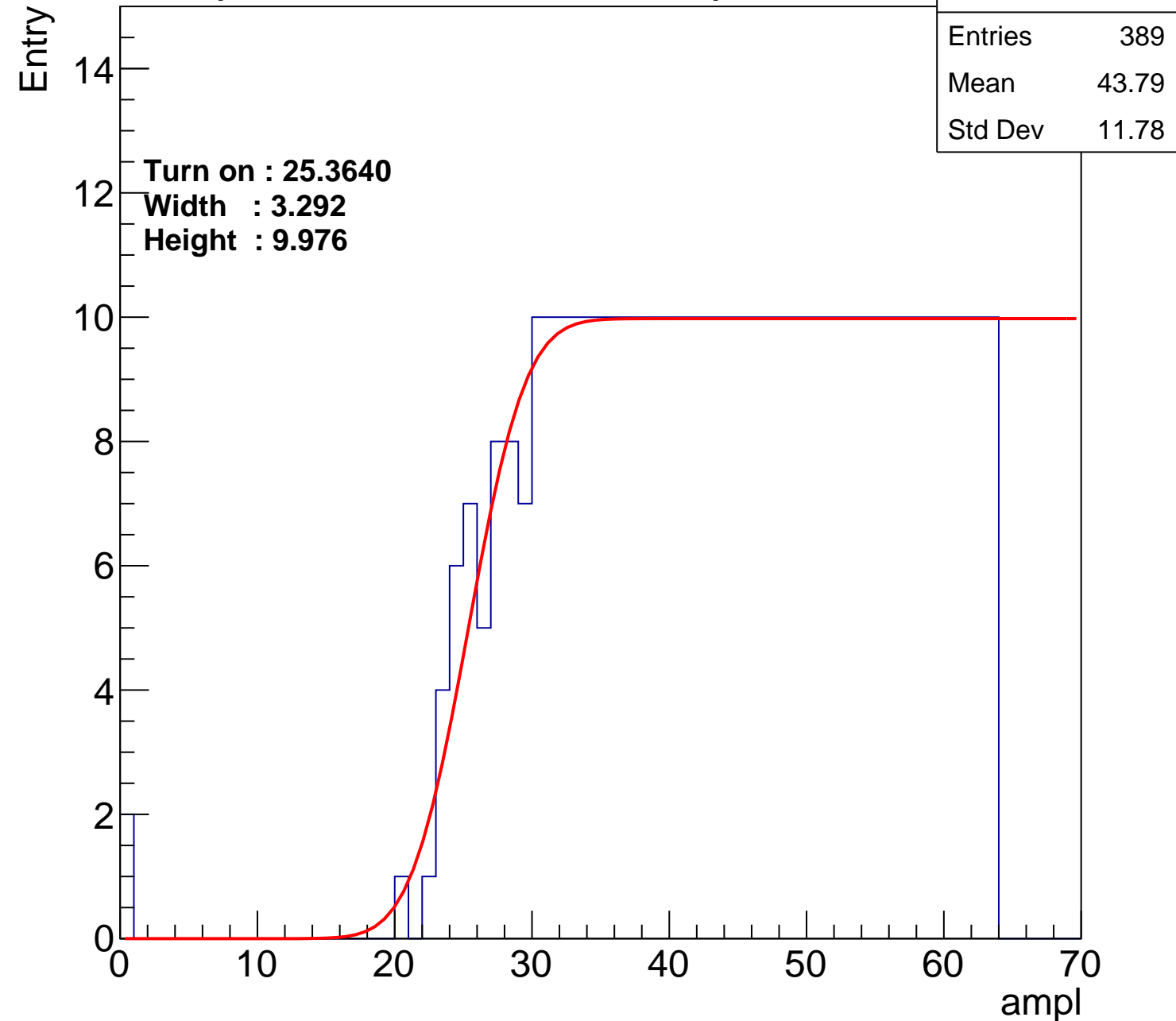
Width : 3.292

Height : 9.976

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch43

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	379
Mean	44.32
Std Dev	11.48

**Turn on : 26.3544**

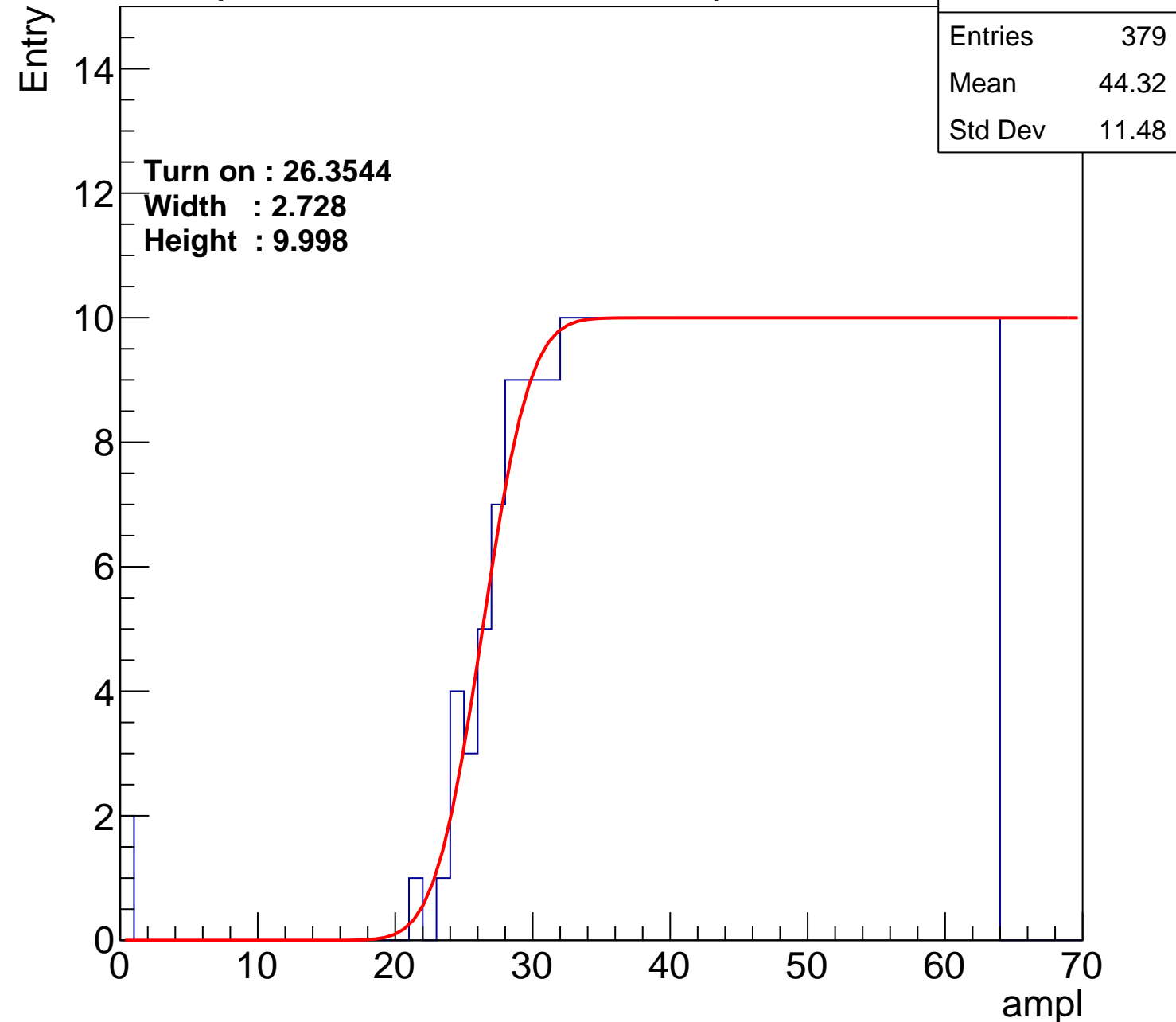
**Width : 2.728**

**Height : 9.998**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch44

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	409
Mean	42.81
Std Dev	12.31

**Turn on : 23.8573**

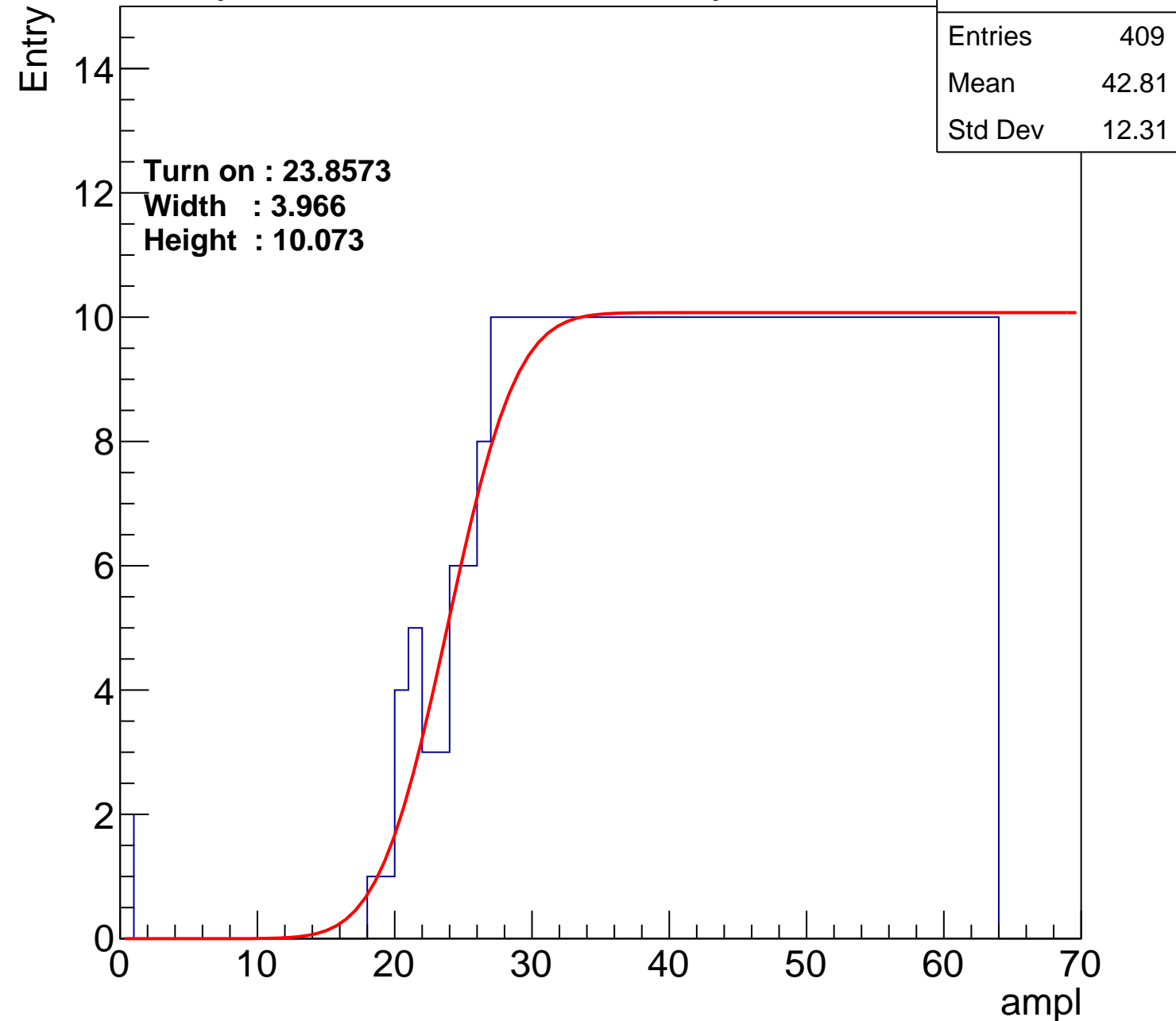
**Width : 3.966**

**Height : 10.073**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch45

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	374
Mean	44.48
Std Dev	11.58

Turn on : 27.2331

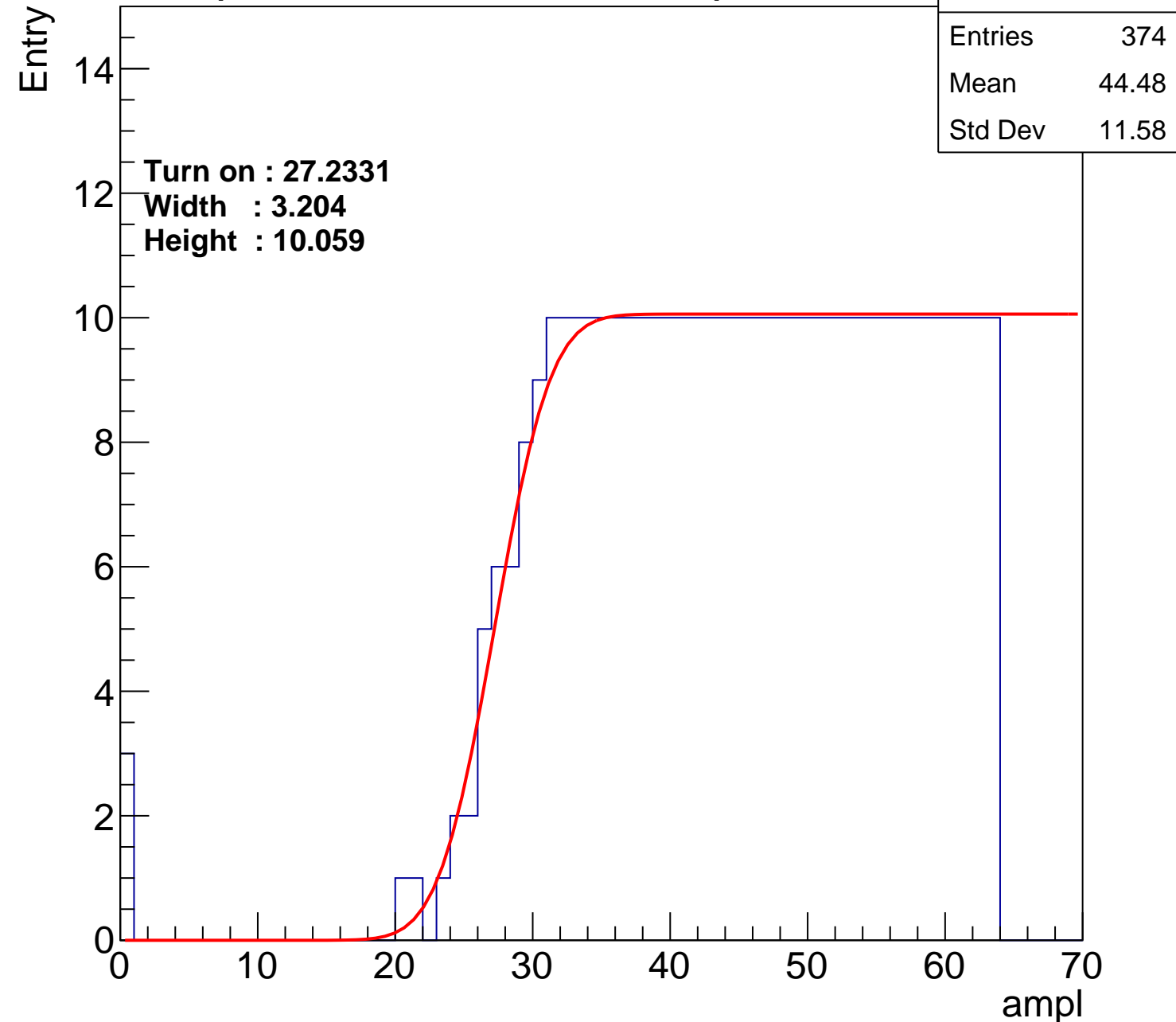
Width : 3.204

Height : 10.059

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch46

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	394
Mean	43.57
Std Dev	11.87

Turn on : 25.0035

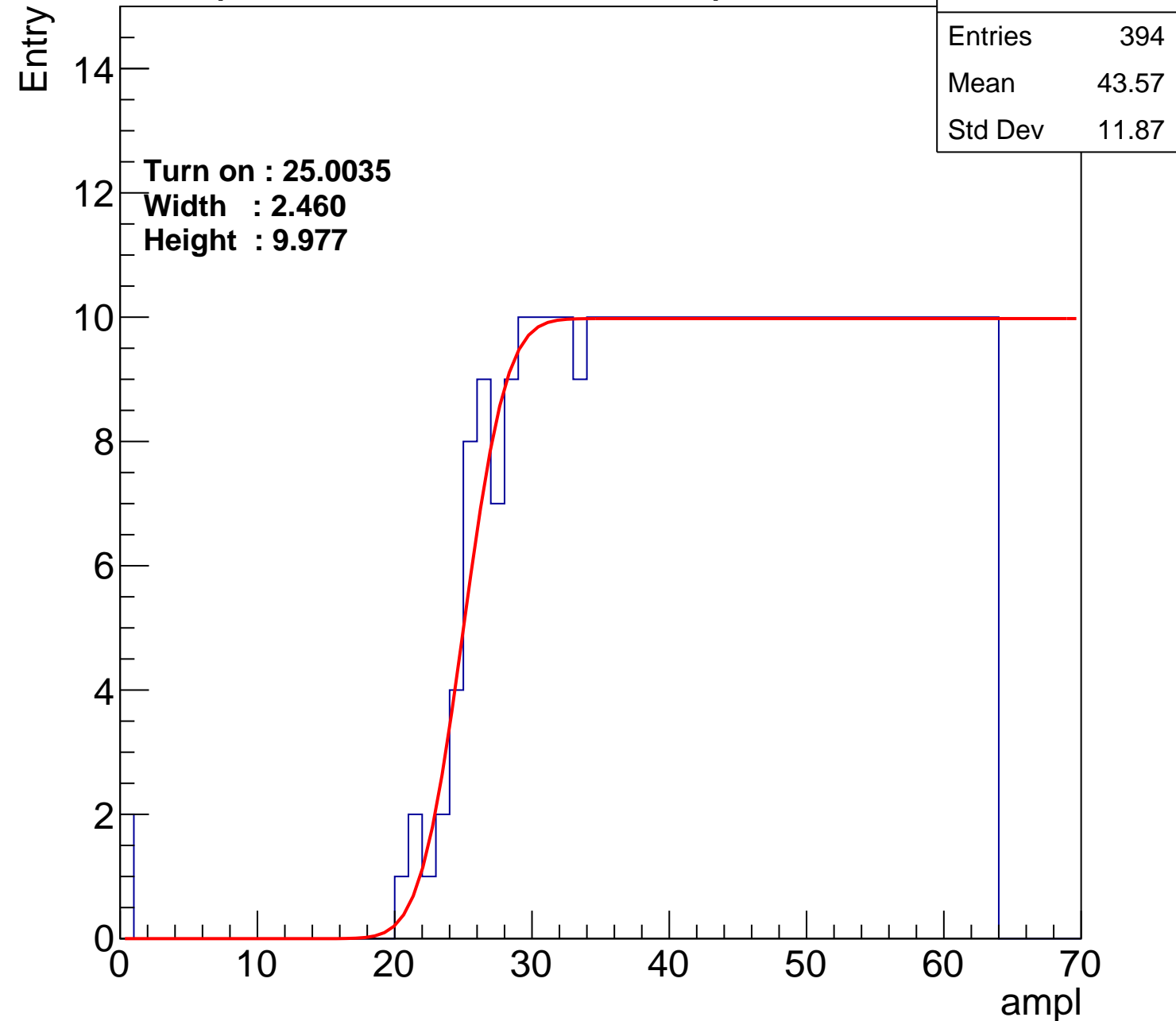
Width : 2.460

Height : 9.977

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L102S, U2-ch47

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	385
Mean	44.03
Std Dev	11.62

Turn on : 25.9183

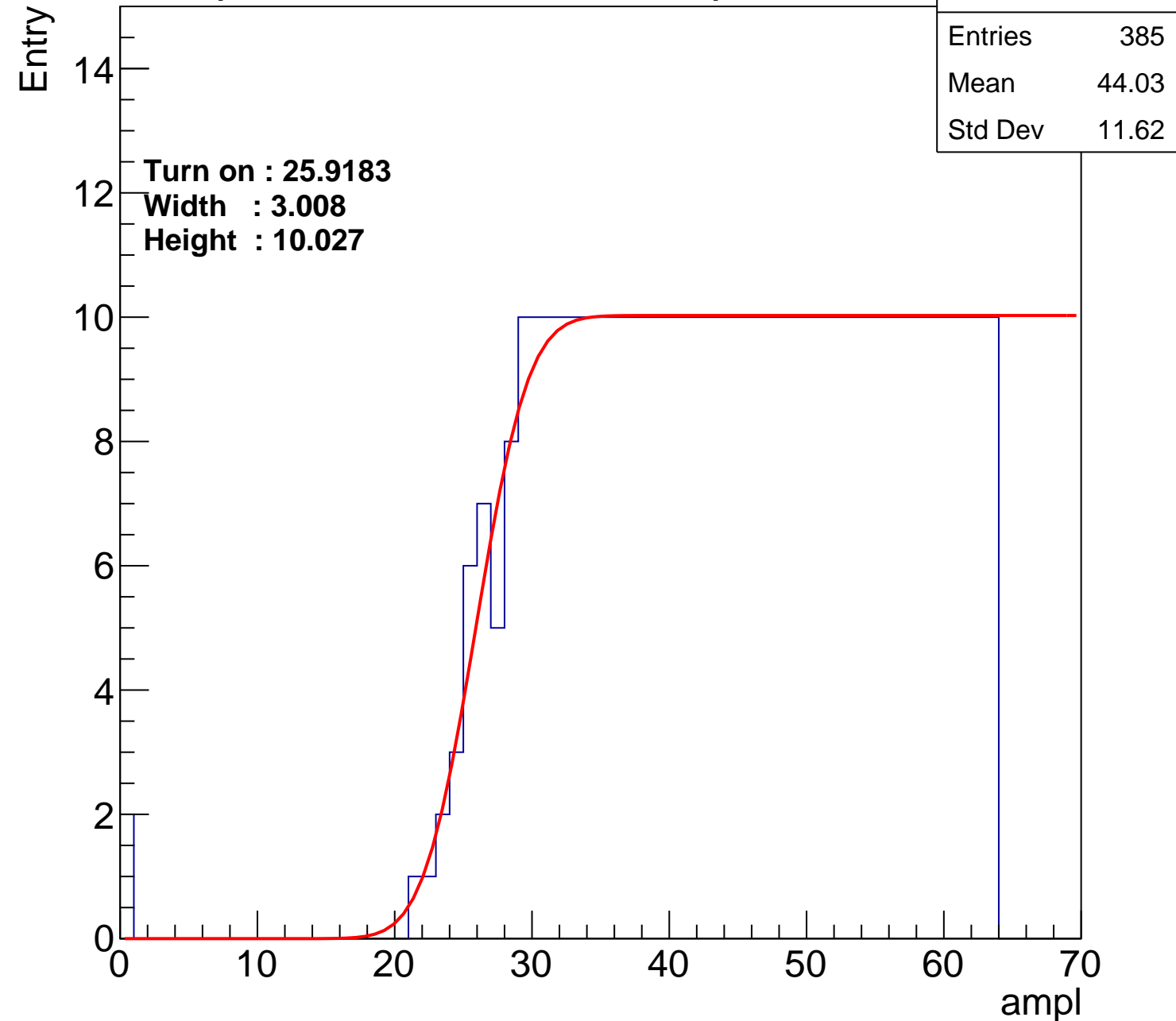
Width : 3.008

Height : 10.027

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch48

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	390
Mean	43.63
Std Dev	12.05

Turn on : 25.9344

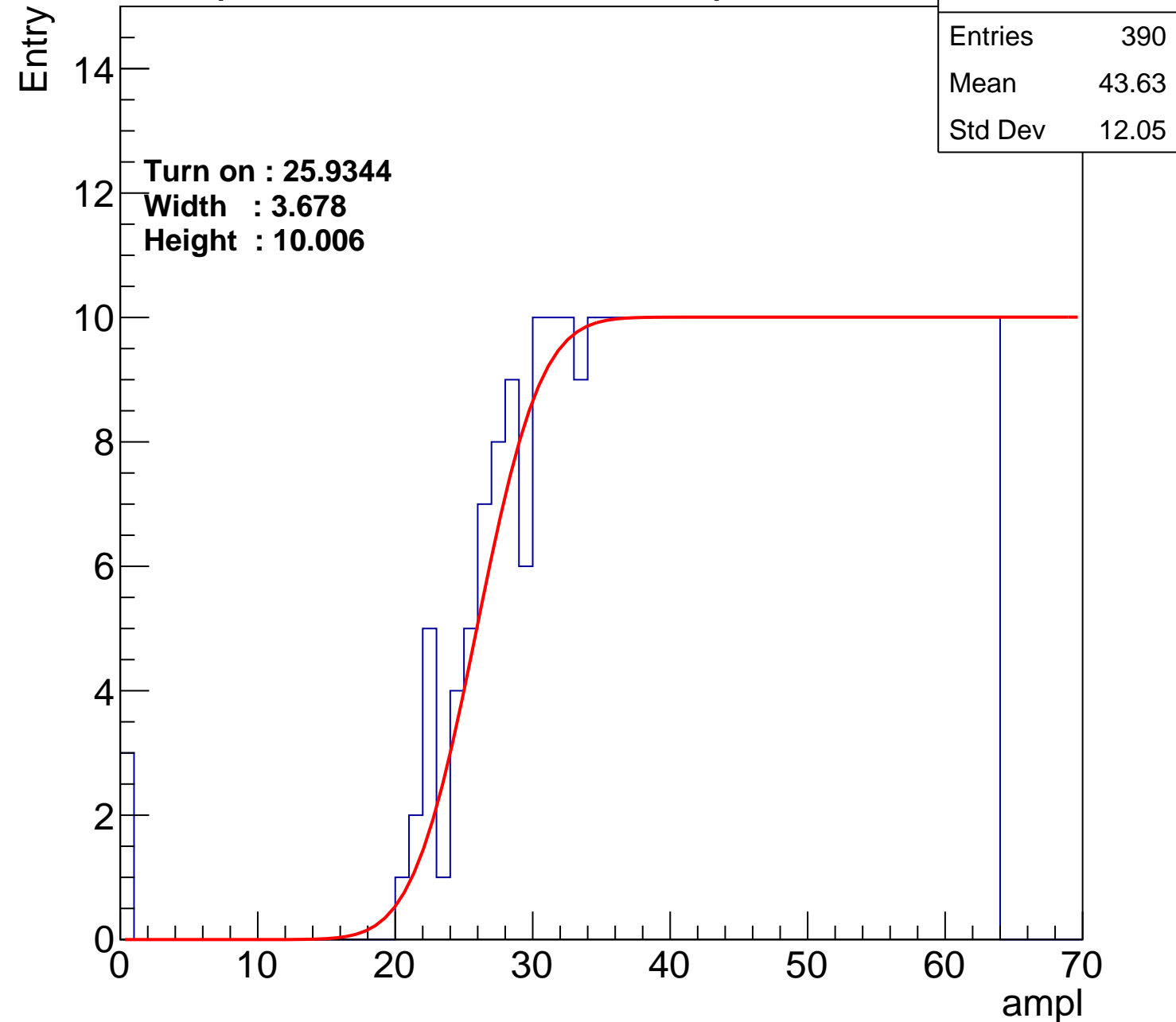
Width : 3.678

Height : 10.006

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch49

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	367
Mean	44.87
Std Dev	11.24

Turn on : 27.7999

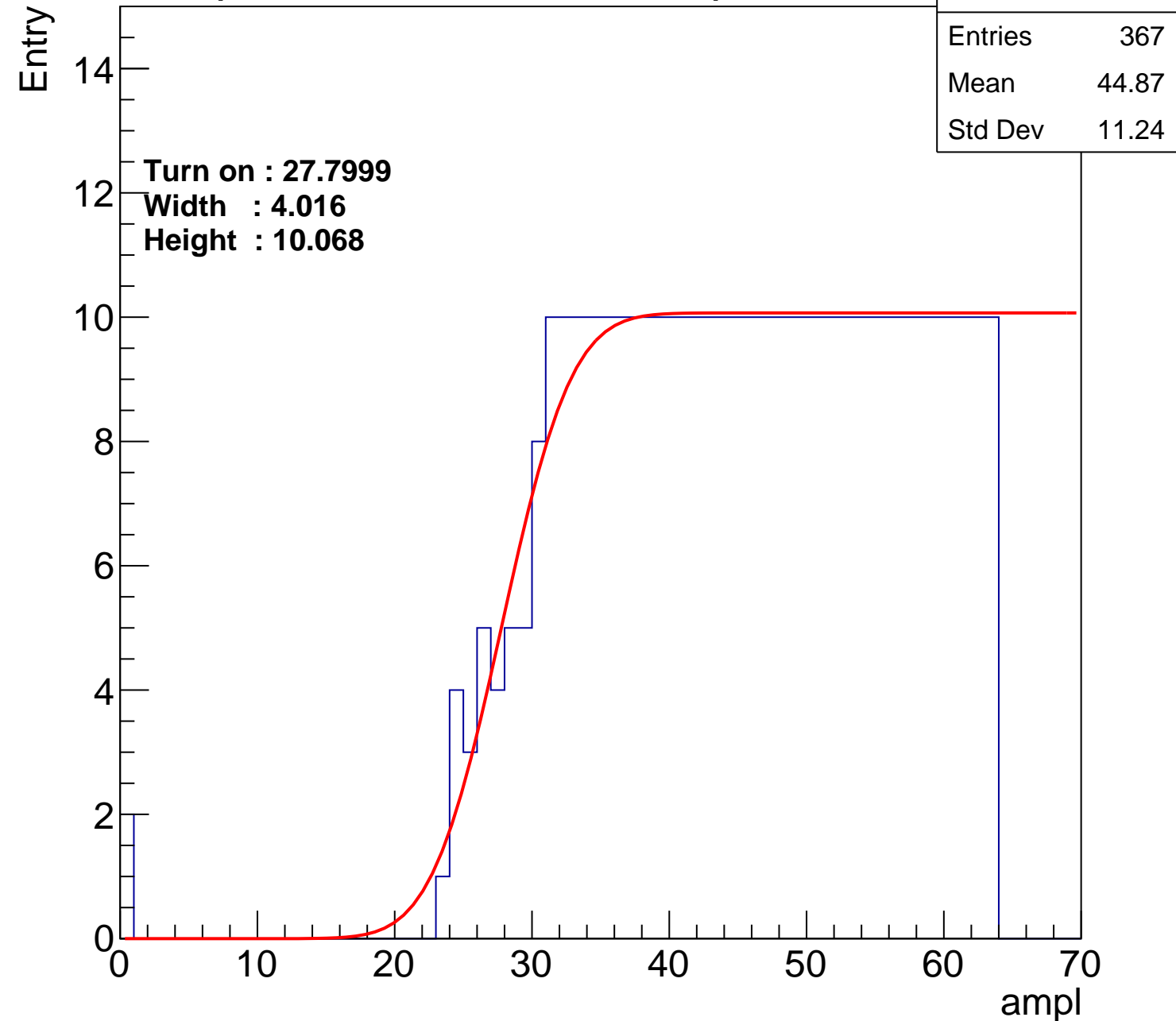
Width : 4.016

Height : 10.068

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch50

calib\_packv5\_042523\_0143.root, FC#11, port A2

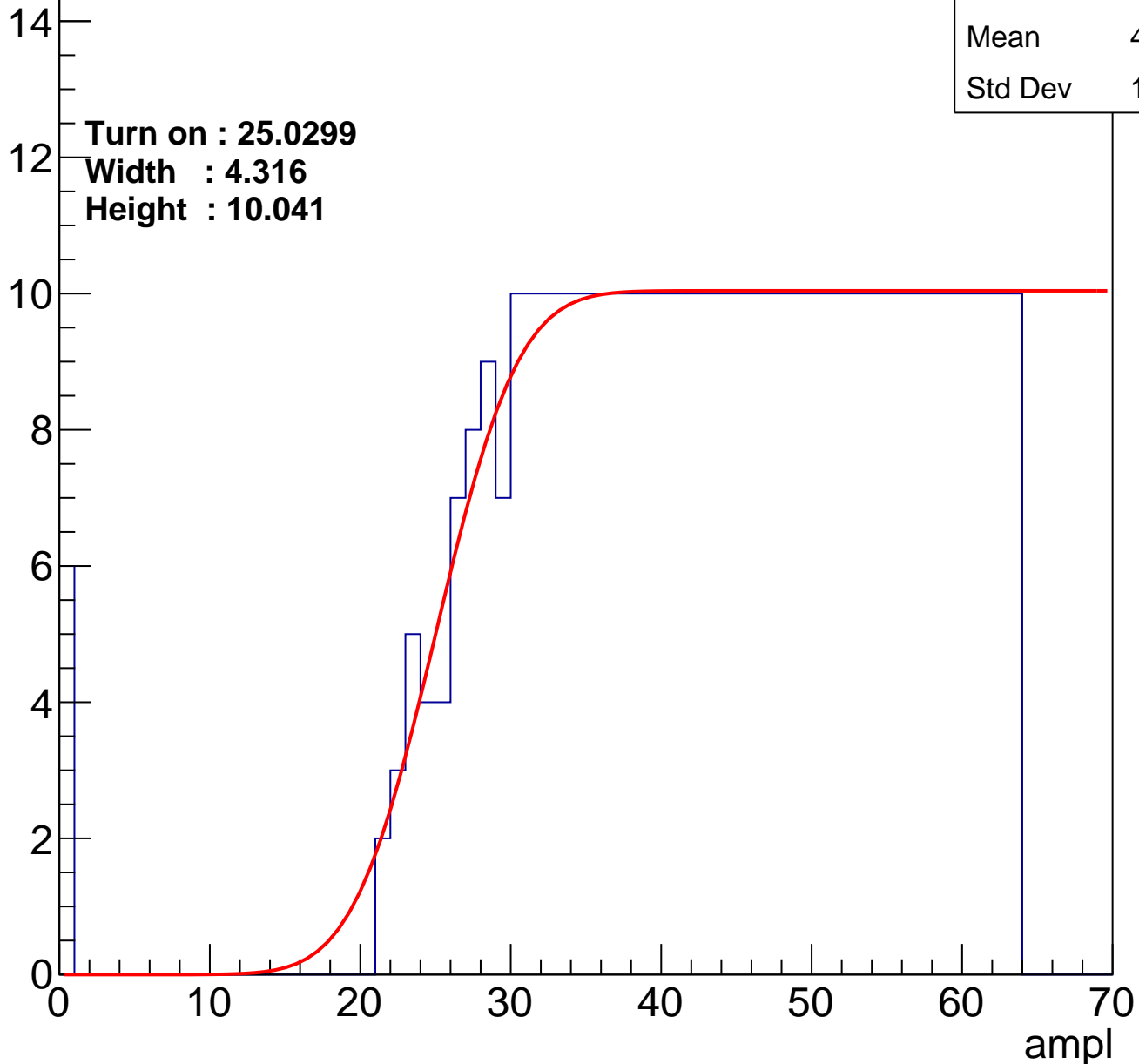
Entries	395
Mean	43.25
Std Dev	12.57

Turn on : 25.0299

Width : 4.316

Height : 10.041

Entry



# B1L102S, U2-ch51

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	407
Mean	42.89
Std Dev	12.33

Turn on : 23.6421

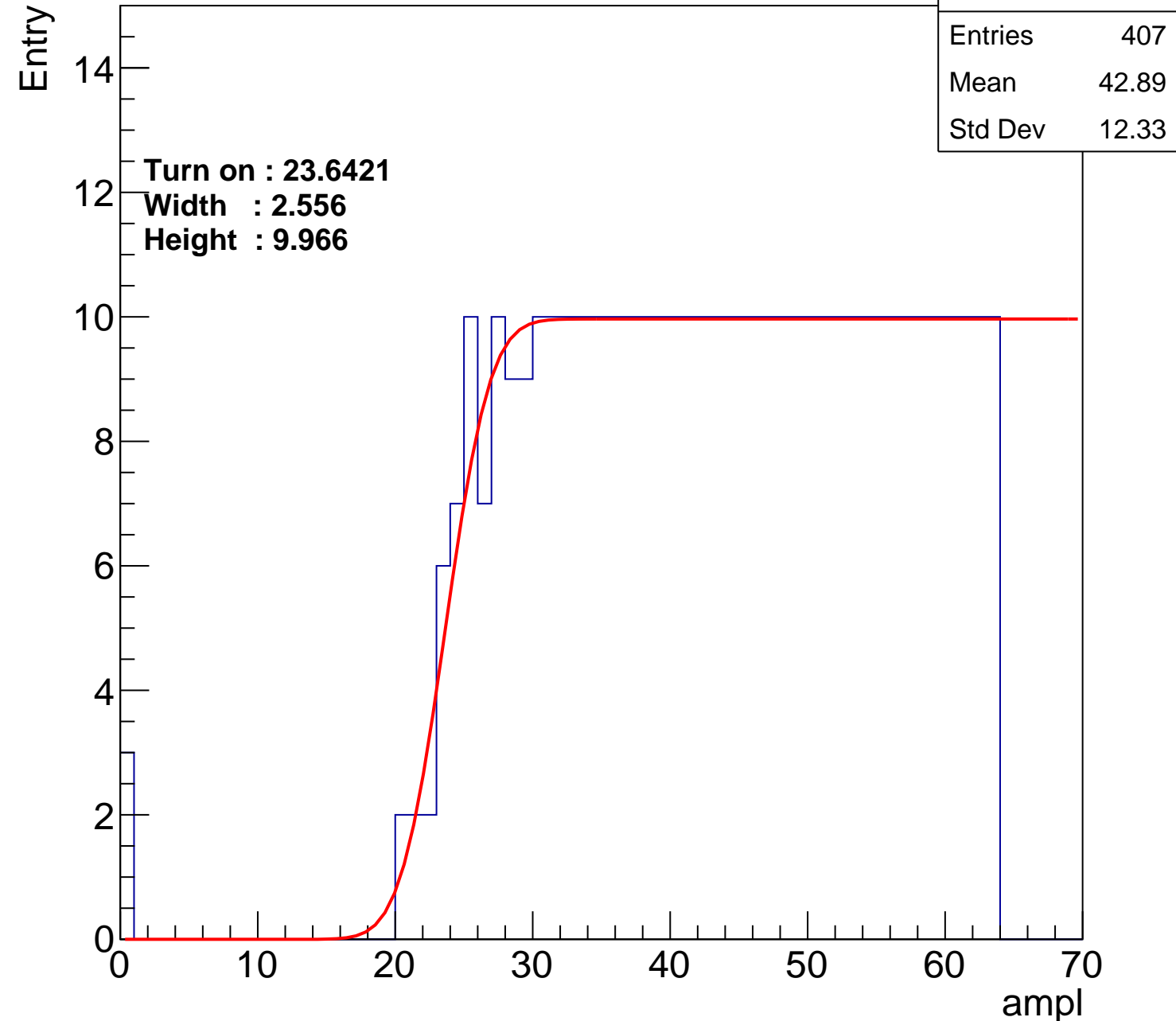
Width : 2.556

Height : 9.966

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch52

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	393
Mean	43.54
Std Dev	12.04

Turn on : 25.2285

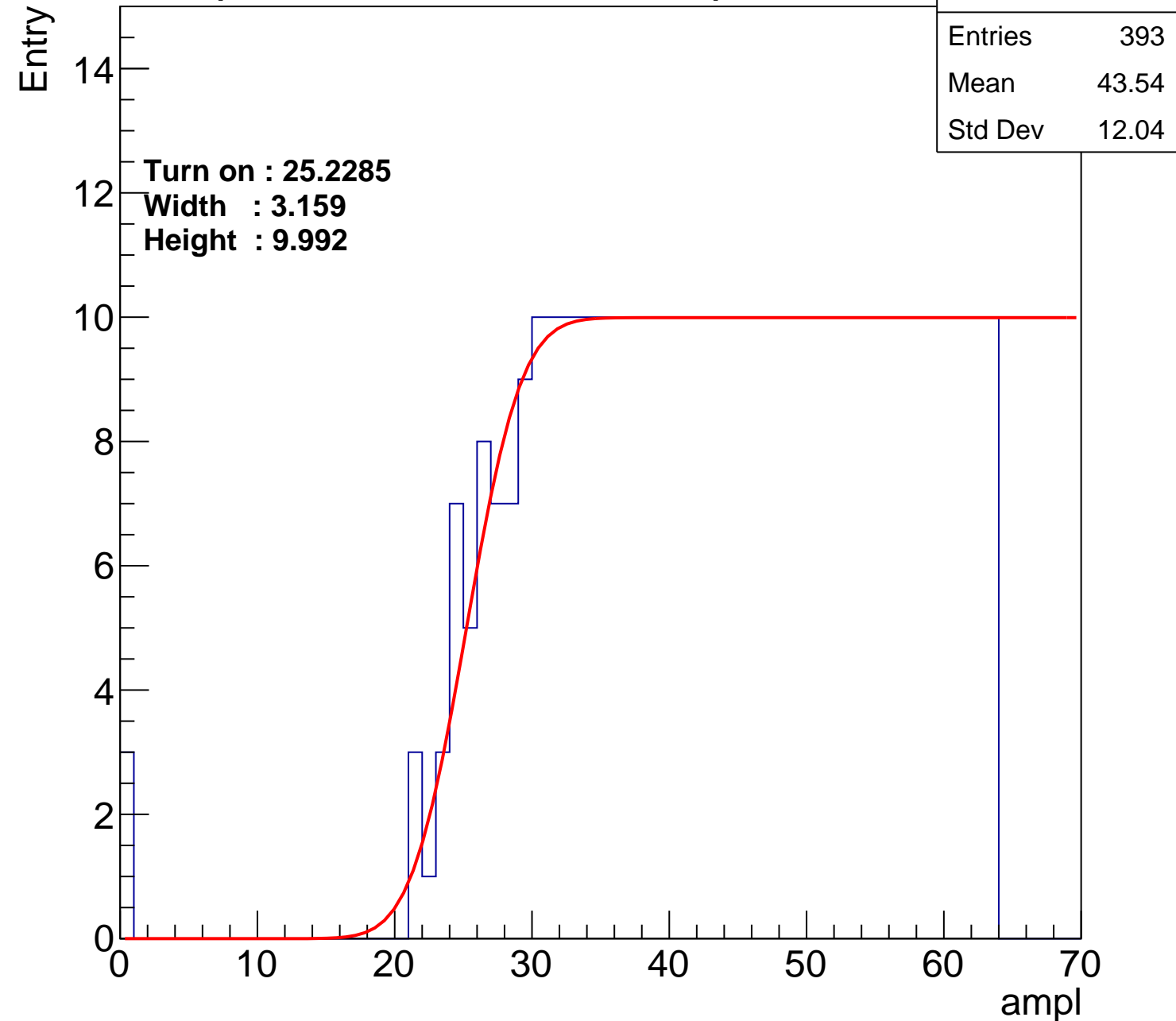
Width : 3.159

Height : 9.992

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch53

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	371
Mean	44.78
Std Dev	11.09

Turn on : 27.3274

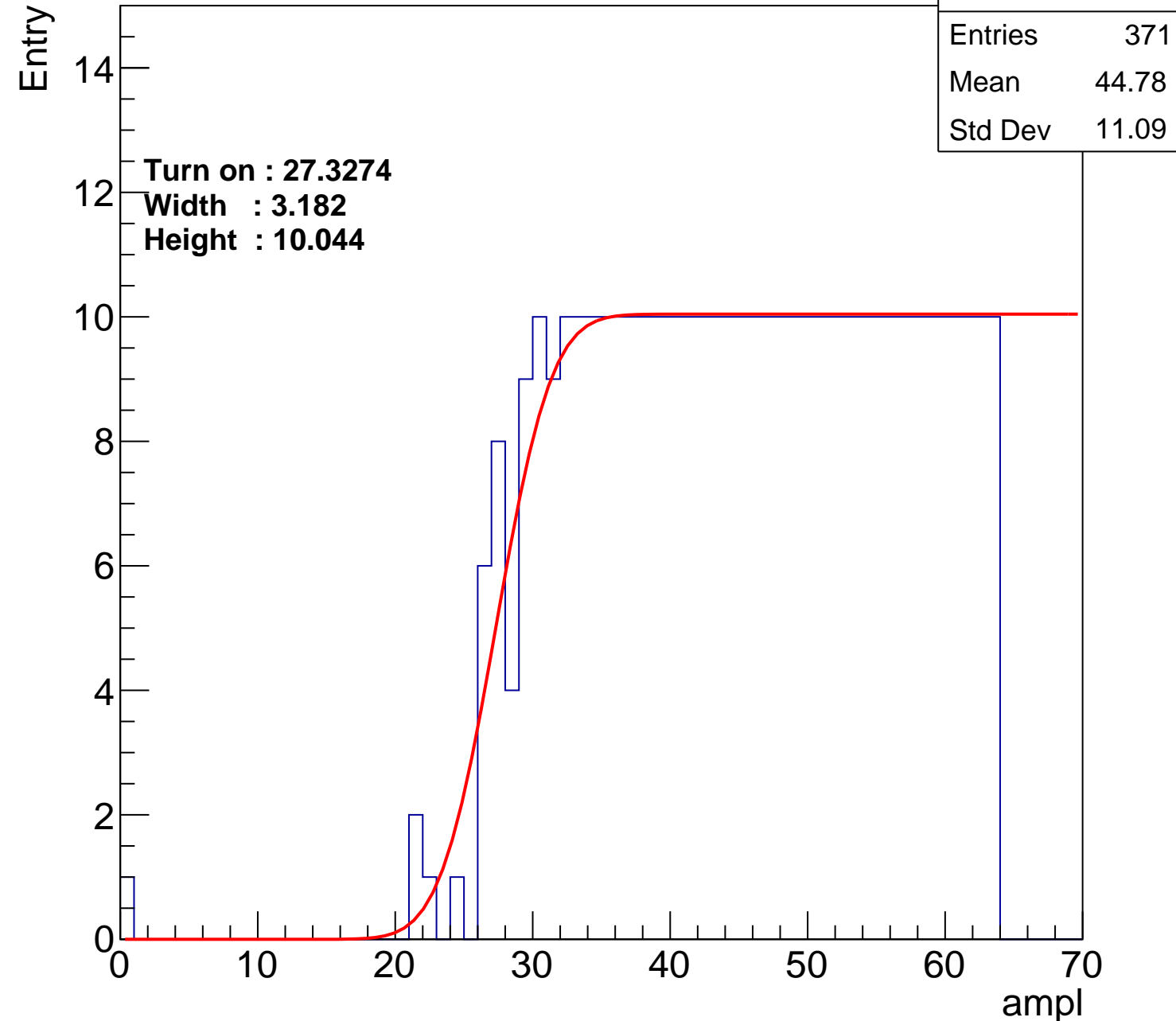
Width : 3.182

Height : 10.044

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch54

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	413
Mean	42.65
Std Dev	12.34

Turn on : 22.3742

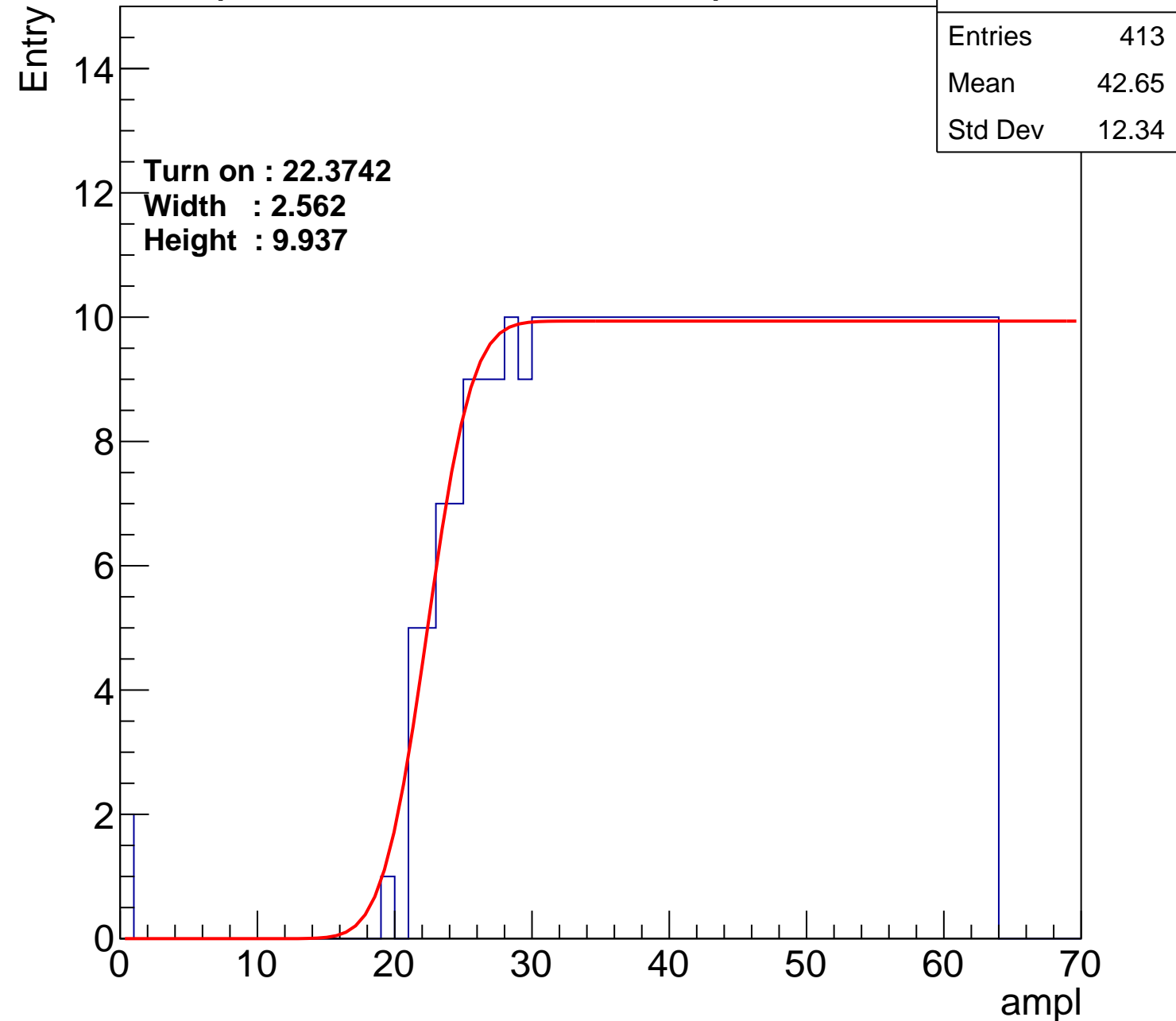
Width : 2.562

Height : 9.937

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L102S, U2-ch55

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	397
Mean	43.38
Std Dev	12.09

**Turn on : 24.5757**

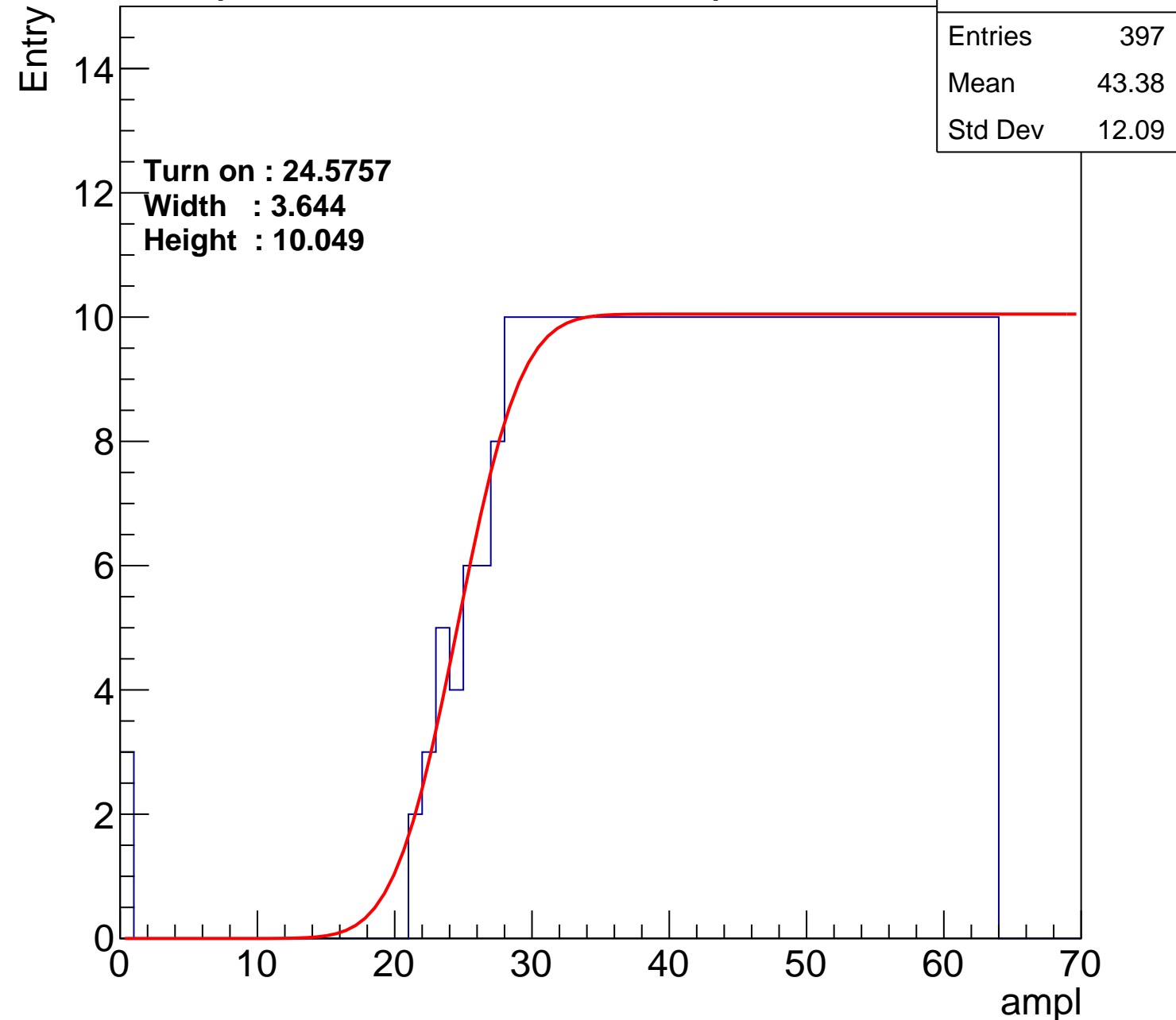
**Width : 3.644**

**Height : 10.049**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch56

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	419
Mean	42.13
Std Dev	13

Turn on : 22.7315

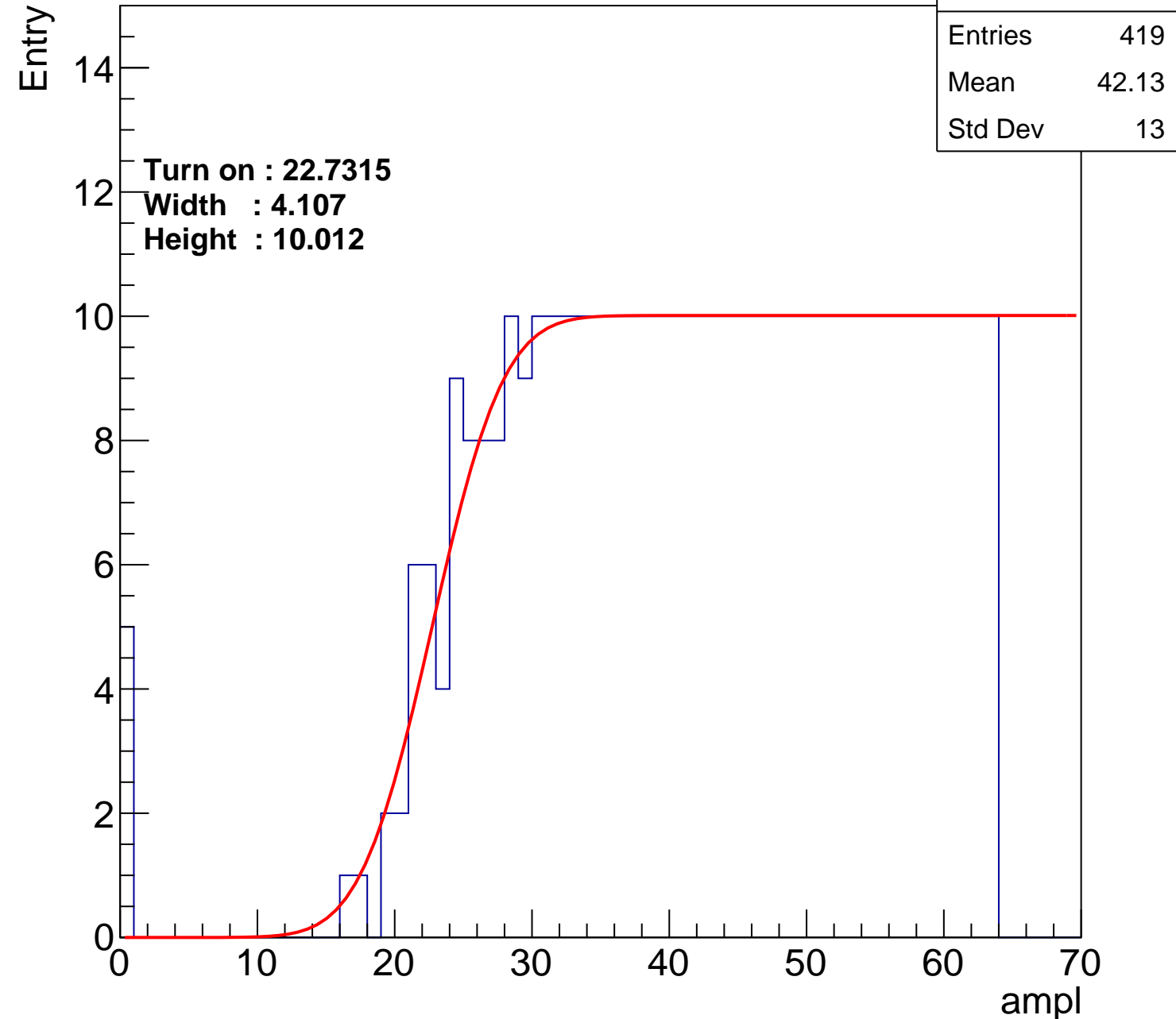
Width : 4.107

Height : 10.012

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch57

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	386
Mean	44.15
Std Dev	11.45

Turn on : 25.8868

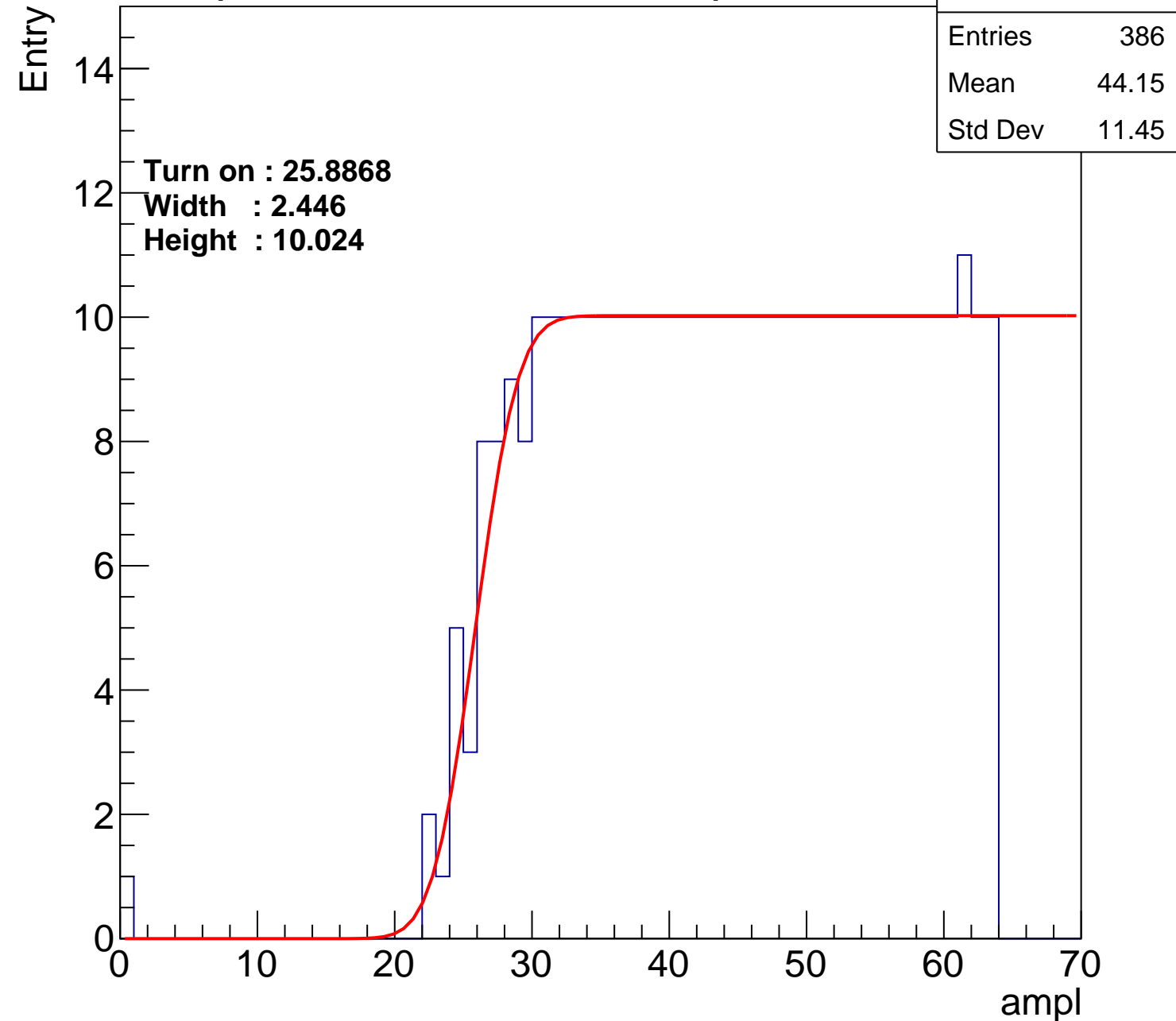
Width : 2.446

Height : 10.024

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch58

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	384
Mean	43.97
Std Dev	11.83

Turn on : 25.6461

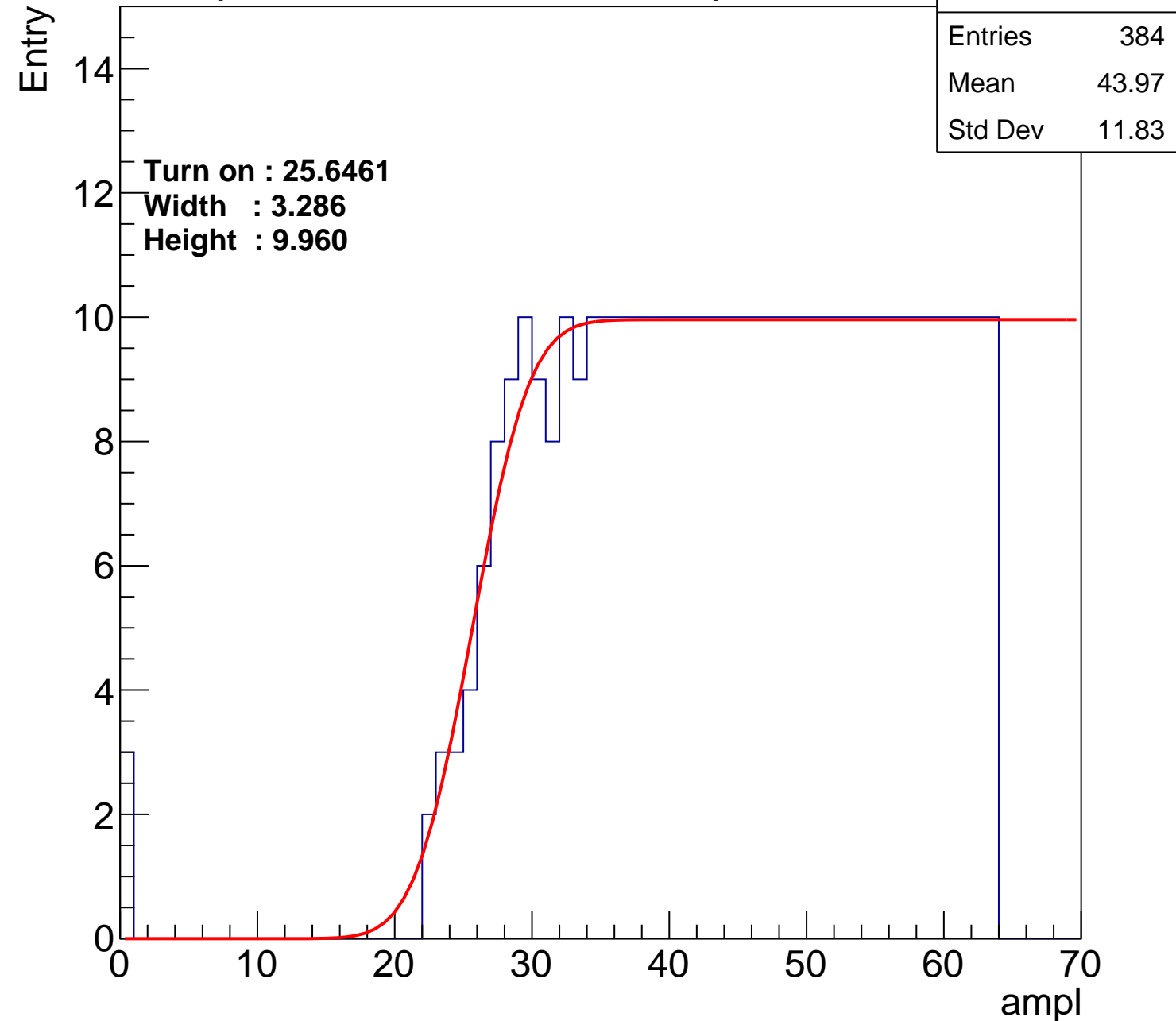
Width : 3.286

Height : 9.960

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch59

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	411
Mean	42.67
Std Dev	12.47

Turn on : 23.4097

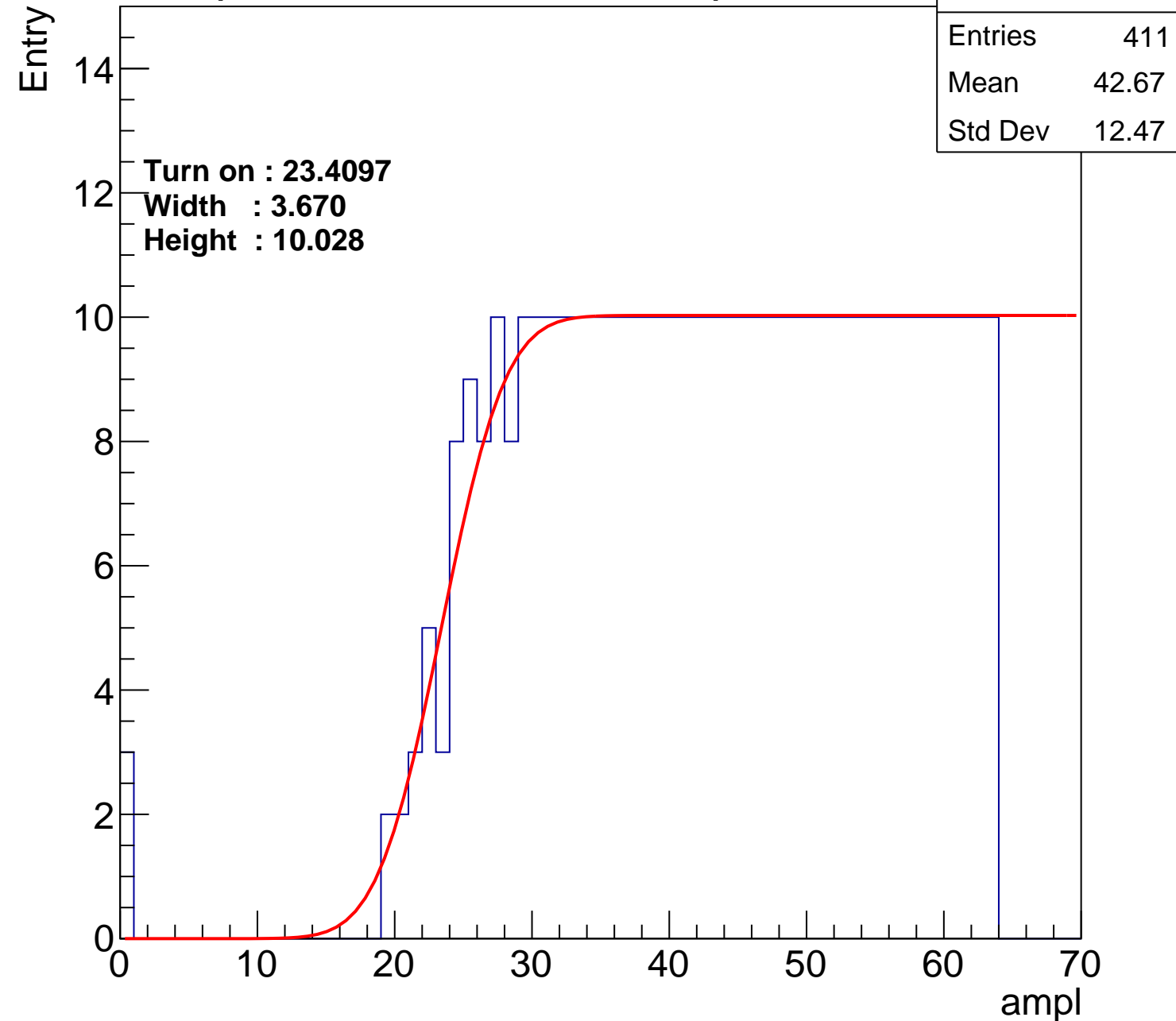
Width : 3.670

Height : 10.028

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch60

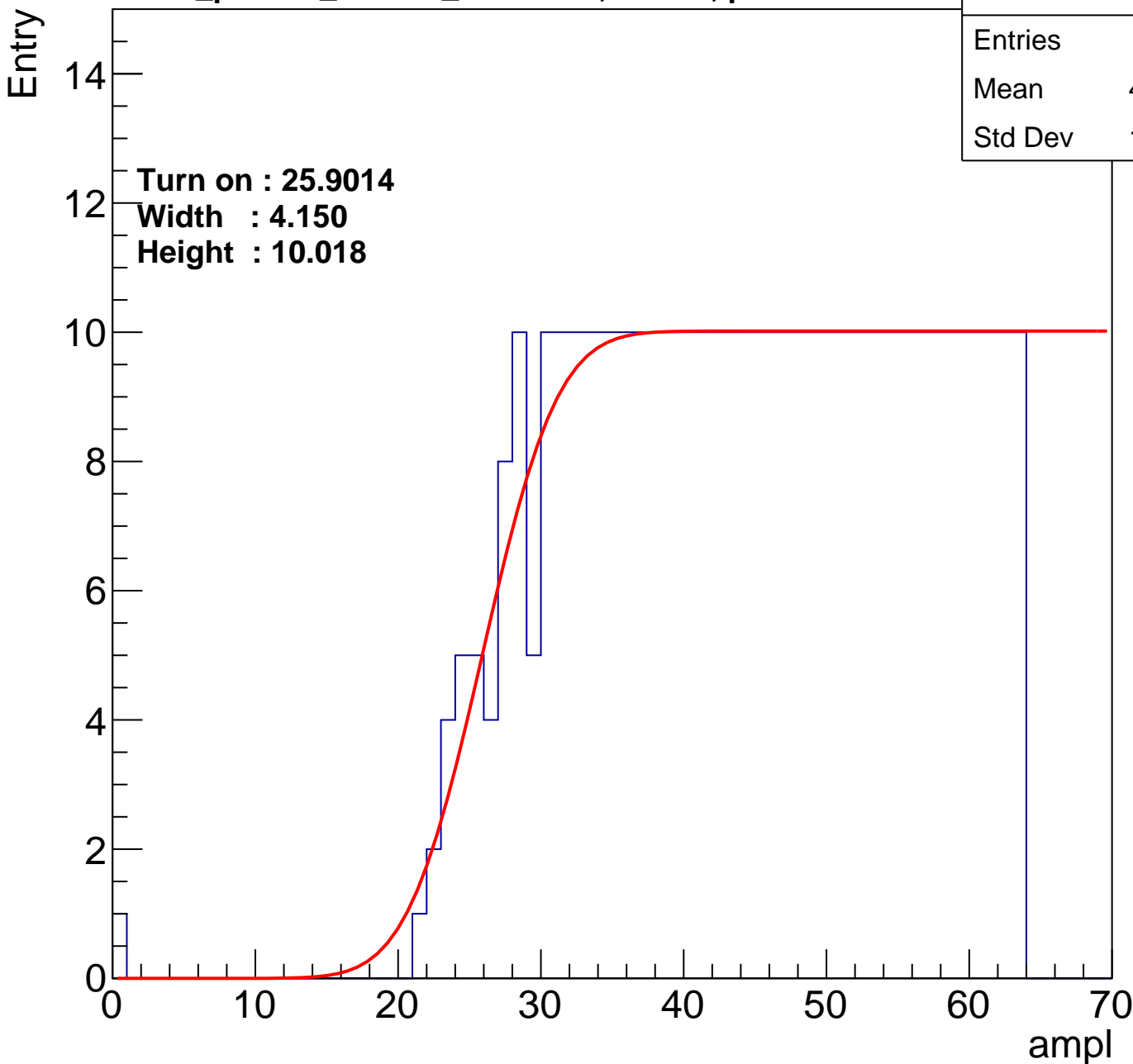
**calib\_packv5\_042523\_0143.root, FC#11, port A2**

**Turn on : 25.9014**

**Width : 4.150**

**Height : 10.018**

Entries	385
Mean	44.04
Std Dev	11.53



# B1L102S, U2-ch61

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	401
Mean	43.26
Std Dev	12.01

Turn on : 24.2613

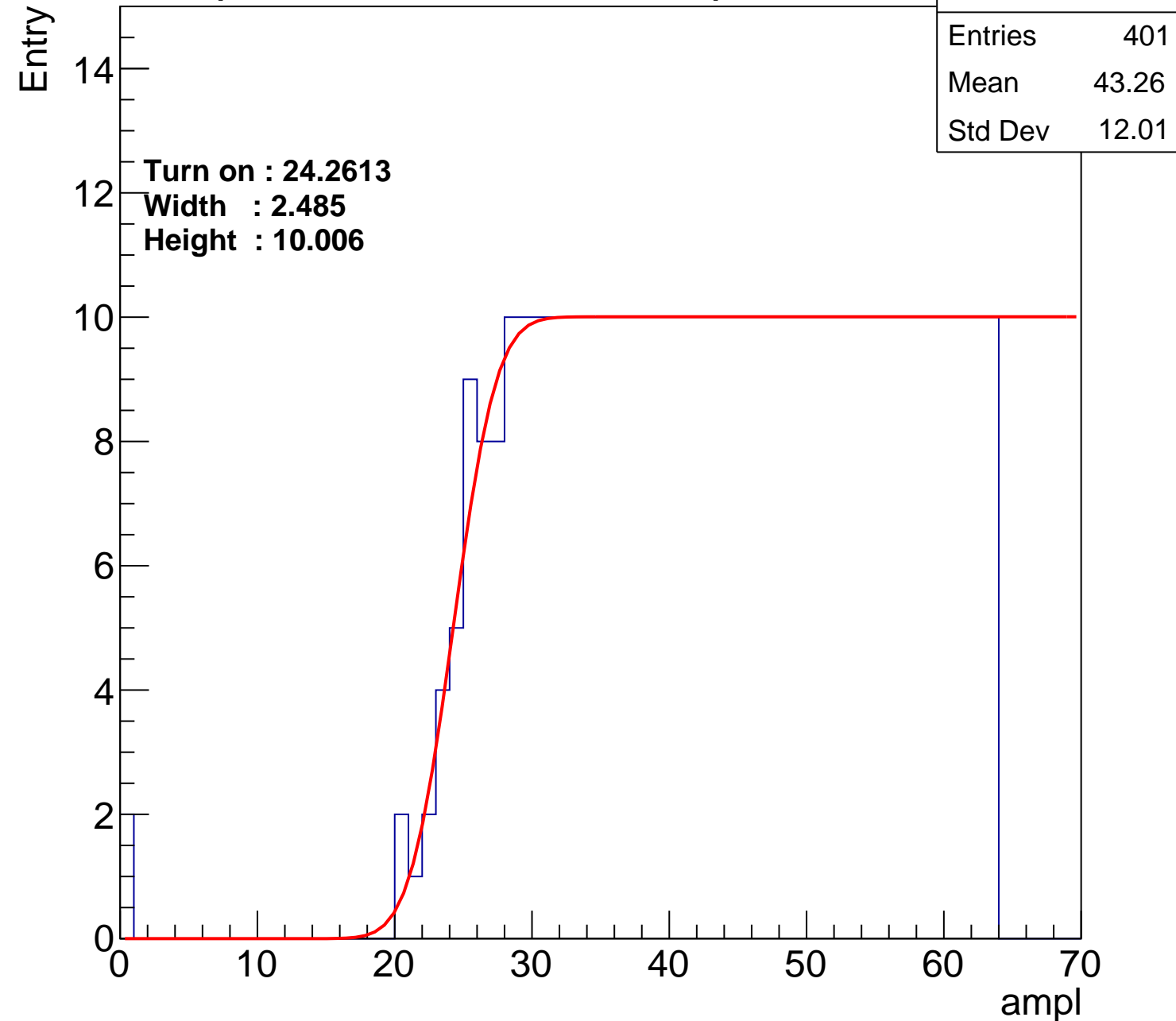
Width : 2.485

Height : 10.006

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch62

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	382
Mean	43.9
Std Dev	12.2

Turn on : 27.9116

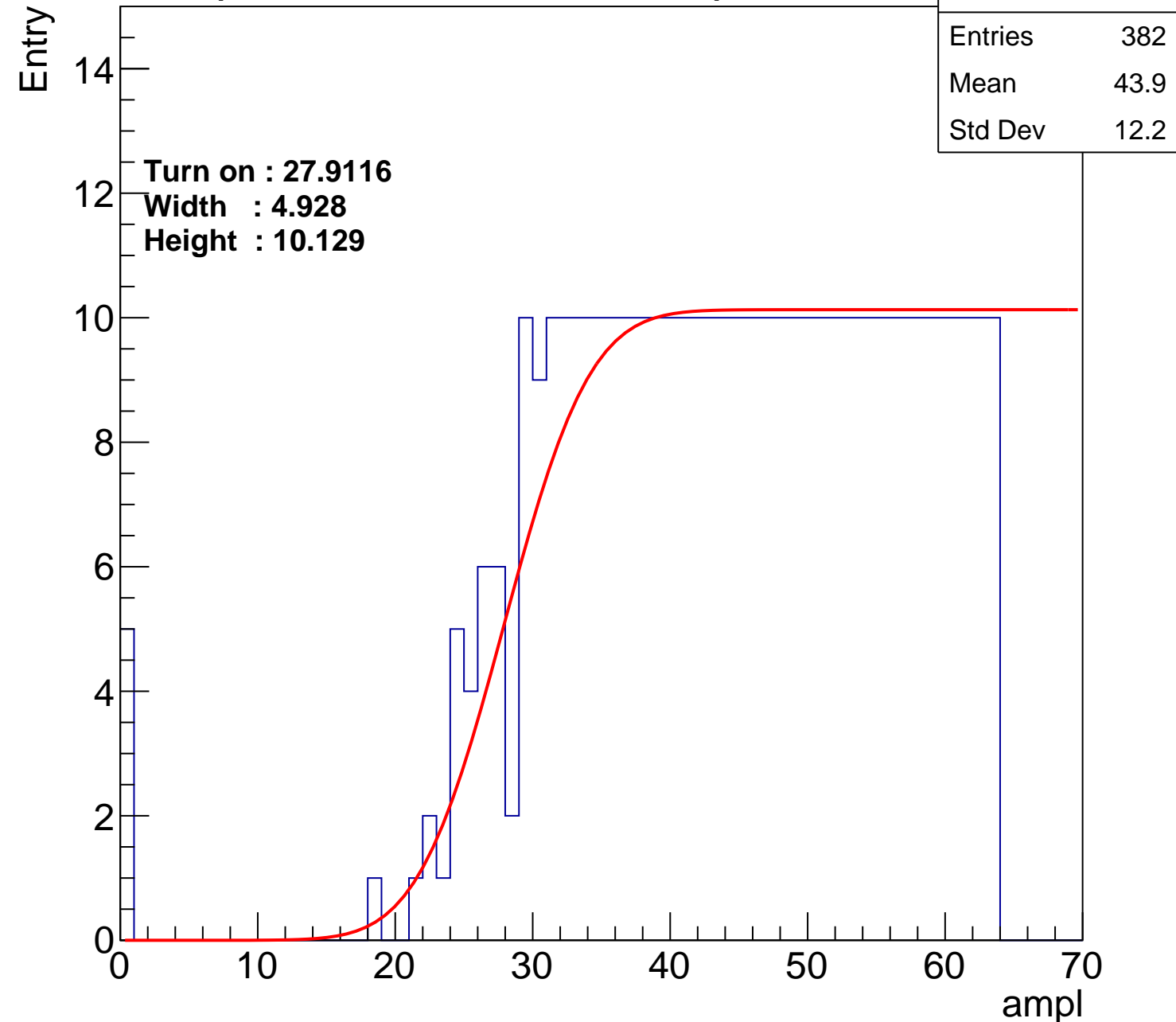
Width : 4.928

Height : 10.129

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L102S, U2-ch63

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	367
Mean	44.86
Std Dev	11.25

Turn on : 27.8168

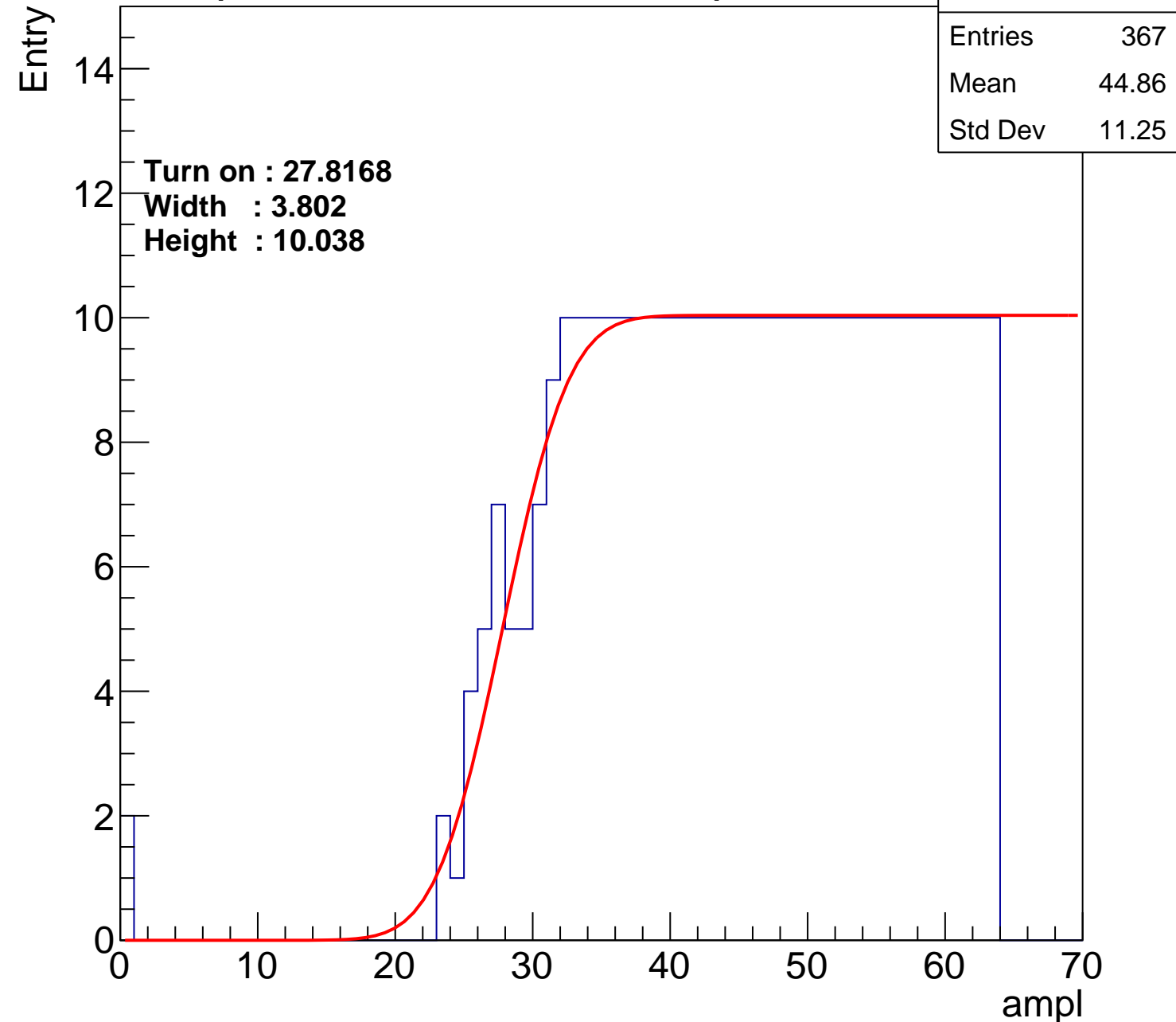
Width : 3.802

Height : 10.038

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch64

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	388
Mean	43.54
Std Dev	12.45

Turn on : 26.4798

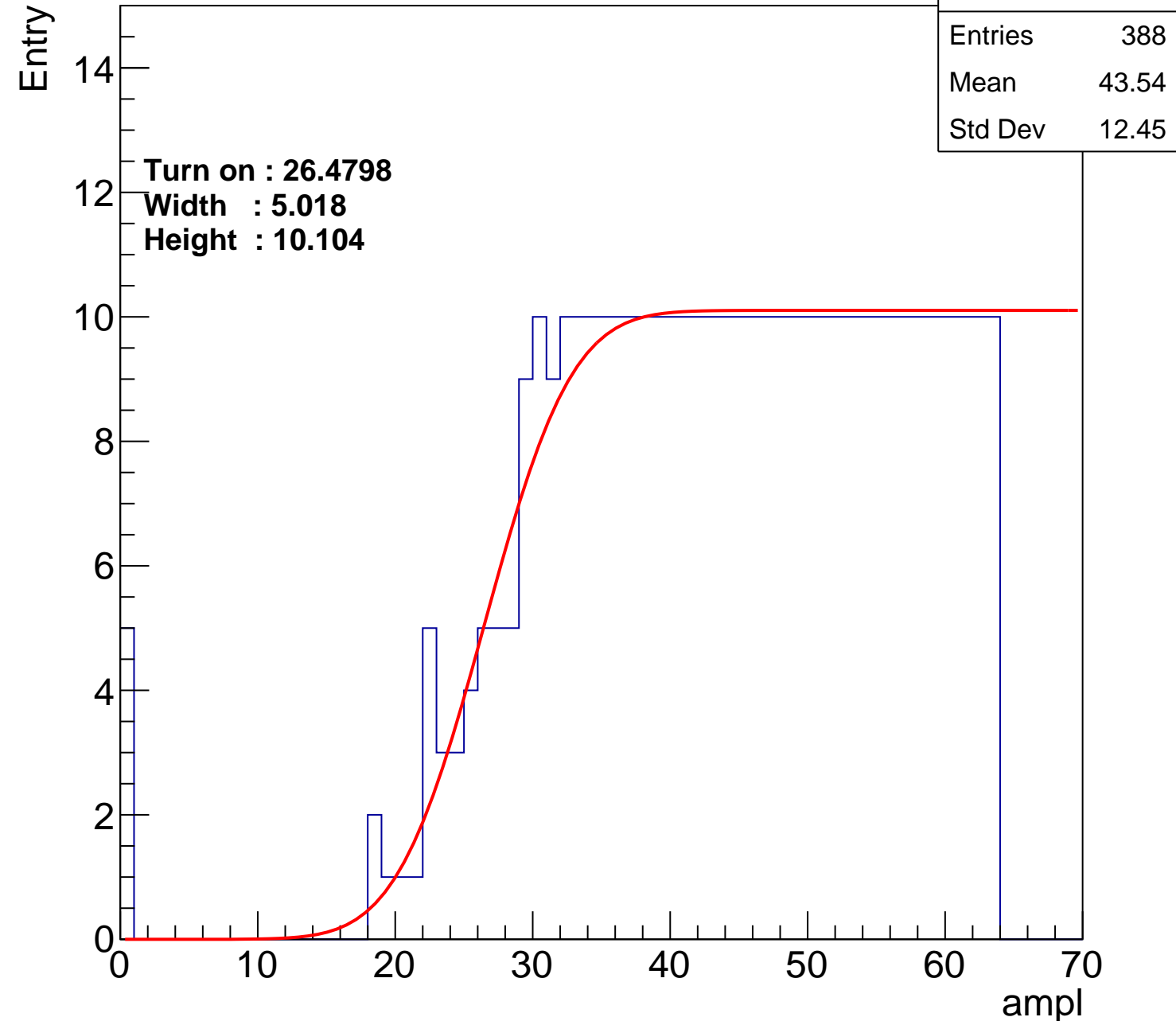
Width : 5.018

Height : 10.104

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch65

calib\_packv5\_042523\_0143.root, FC#11, port A2

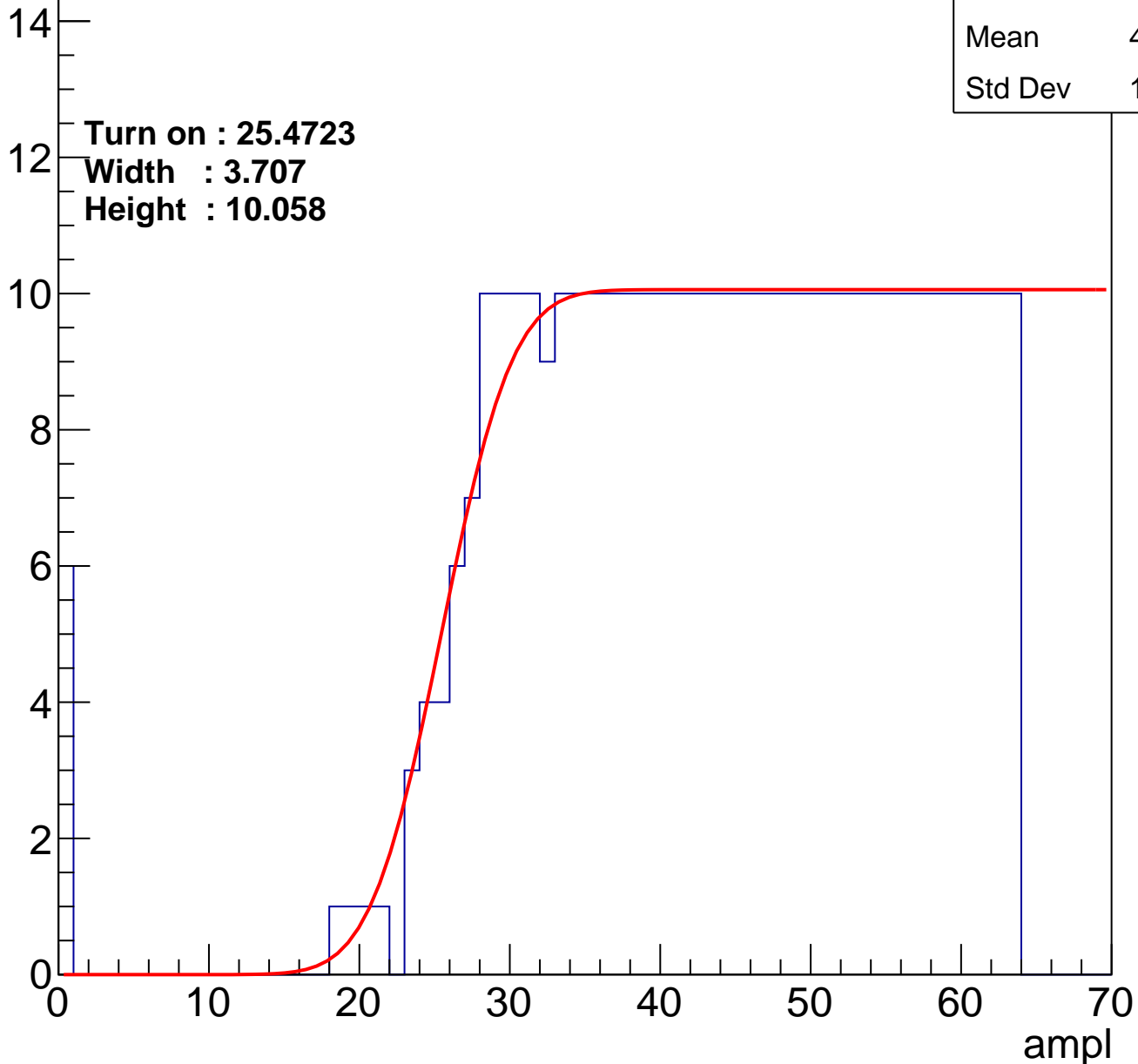
Entries	393
Mean	43.35
Std Dev	12.53

Turn on : 25.4723

Width : 3.707

Height : 10.058

Entry



# B1L102S, U2-ch66

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	391
Mean	43.64
Std Dev	12

**Turn on : 25.9183**

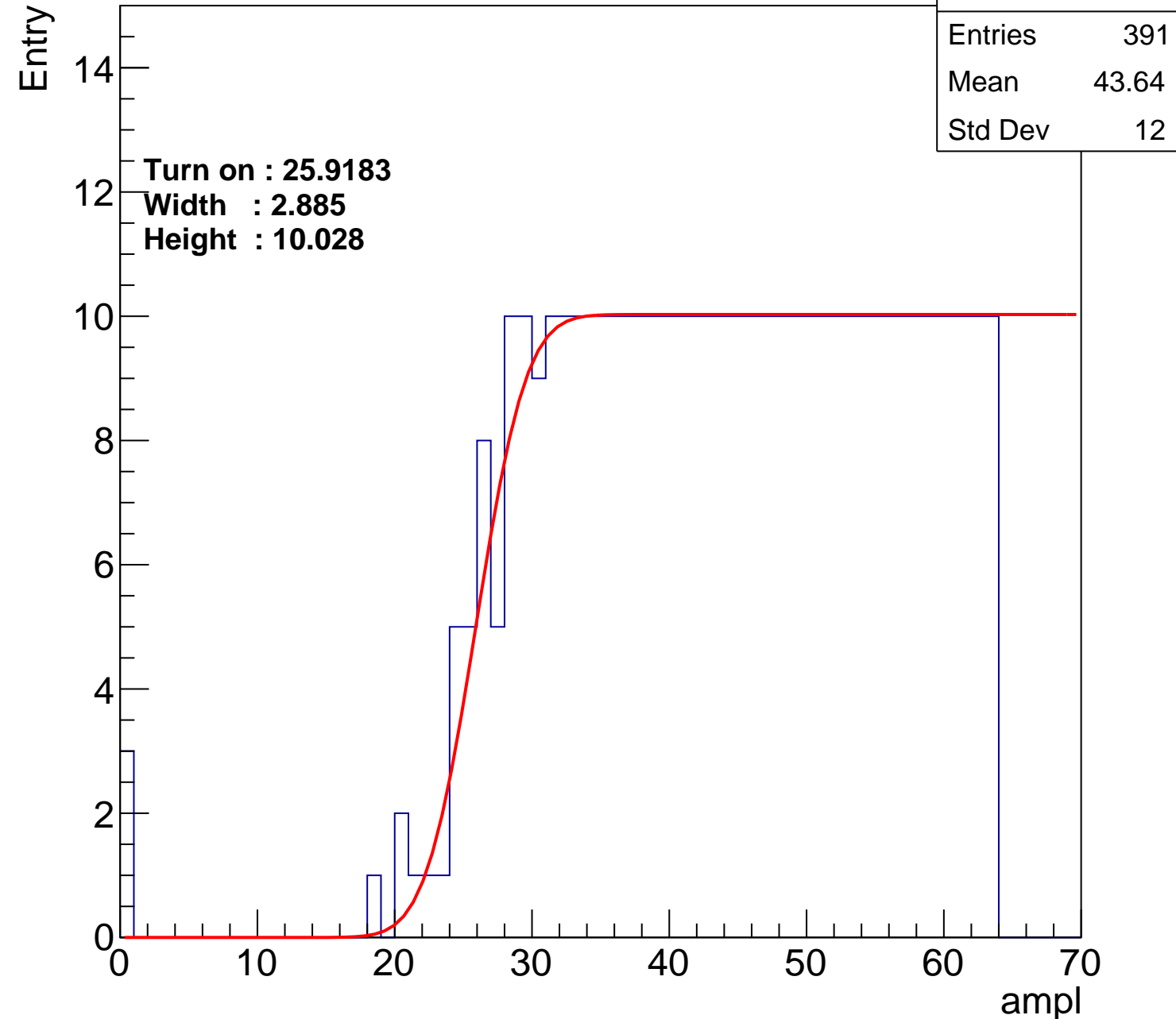
**Width : 2.885**

**Height : 10.028**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch67

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	383
Mean	44.09
Std Dev	11.62

Turn on : 25.8315

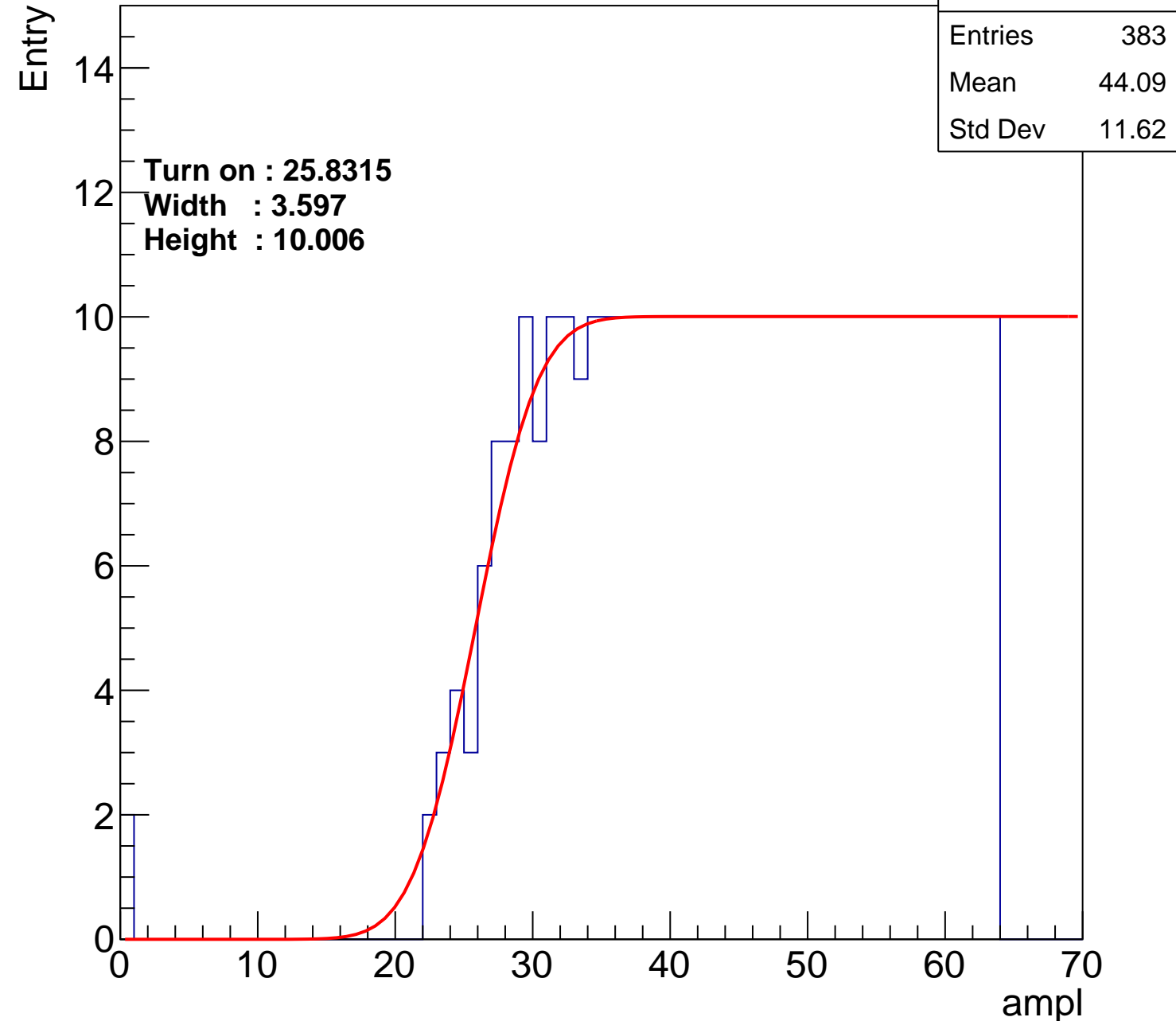
Width : 3.597

Height : 10.006

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch68

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	392
Mean	43.38
Std Dev	12.53

Turn on : 25.5070

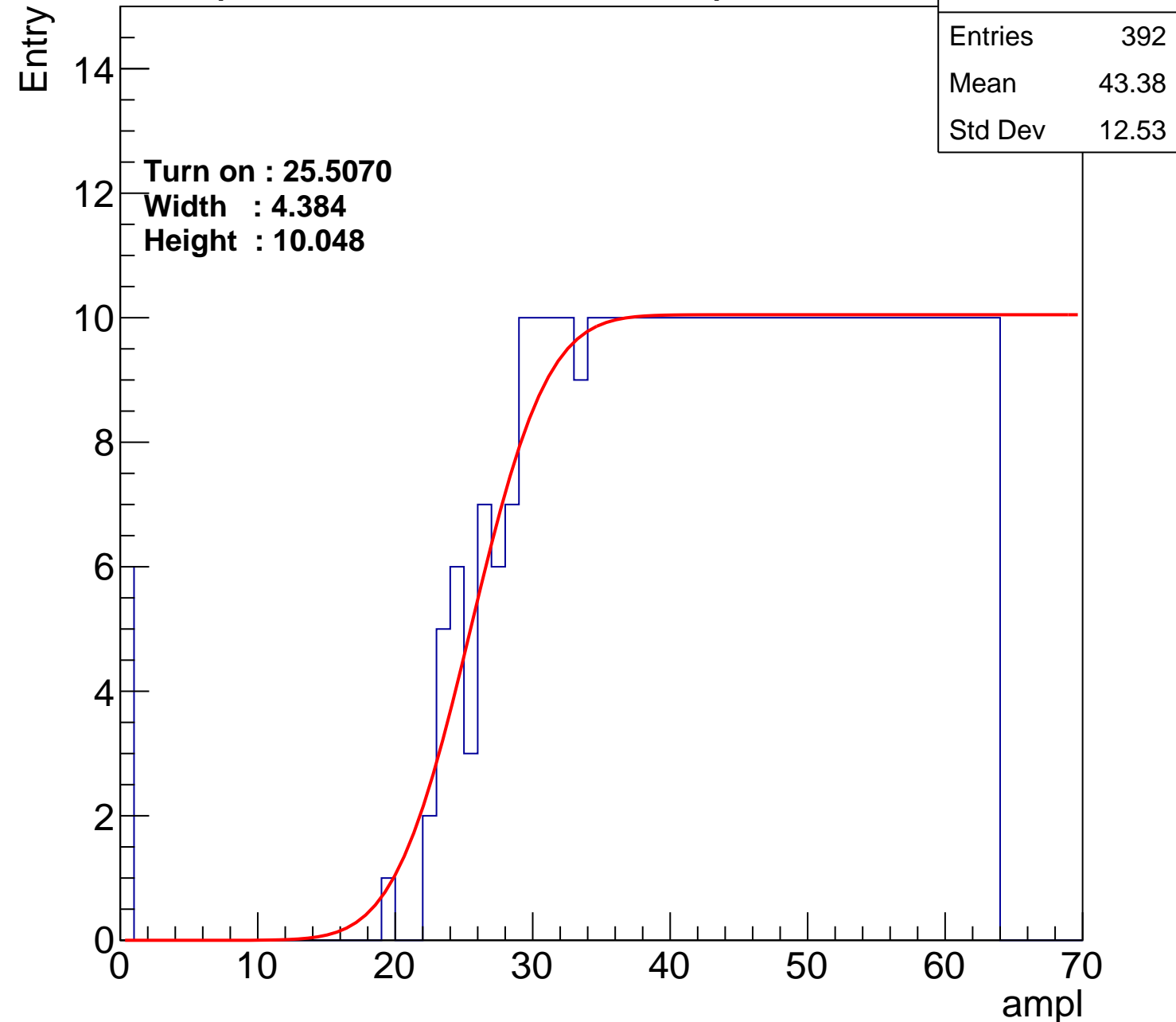
Width : 4.384

Height : 10.048

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch69

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	386
Mean	43.94
Std Dev	11.72

Turn on : 26.0112

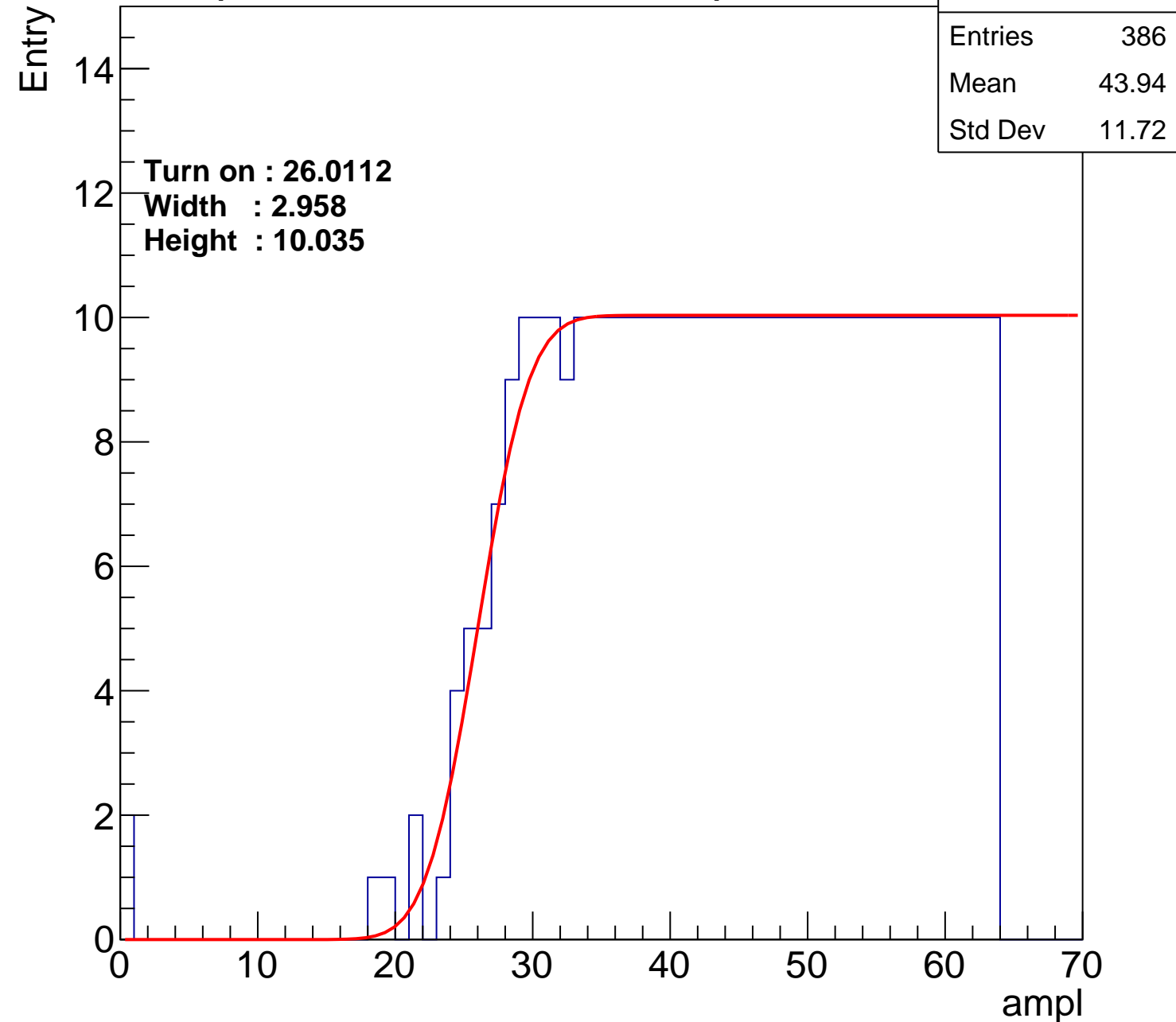
Width : 2.958

Height : 10.035

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch70

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	373
Mean	44.25
Std Dev	12.19

Turn on : 28.4412

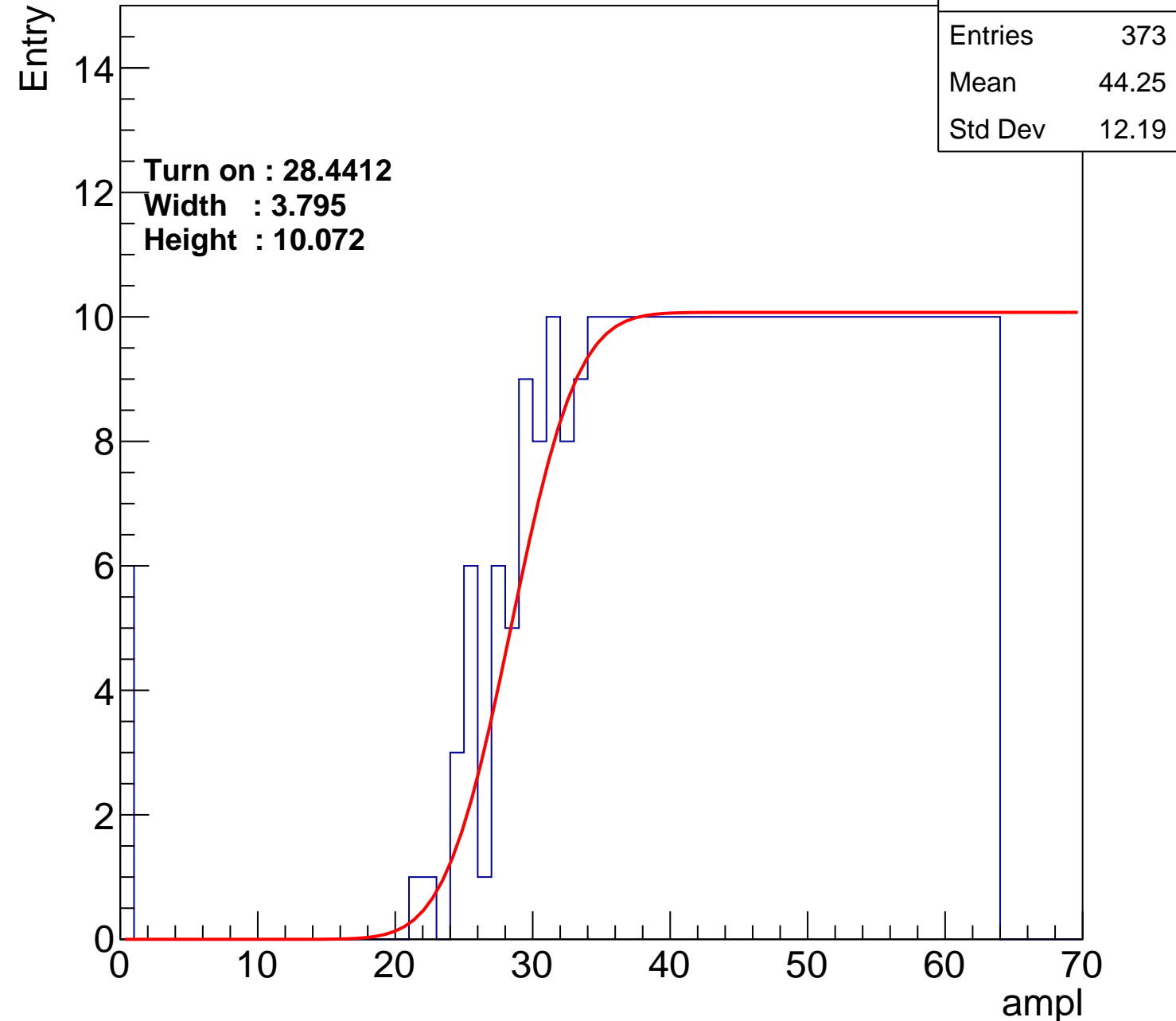
Width : 3.795

Height : 10.072

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L102S, U2-ch71

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	392
Mean	43.56
Std Dev	12.05

Turn on : 25.1191

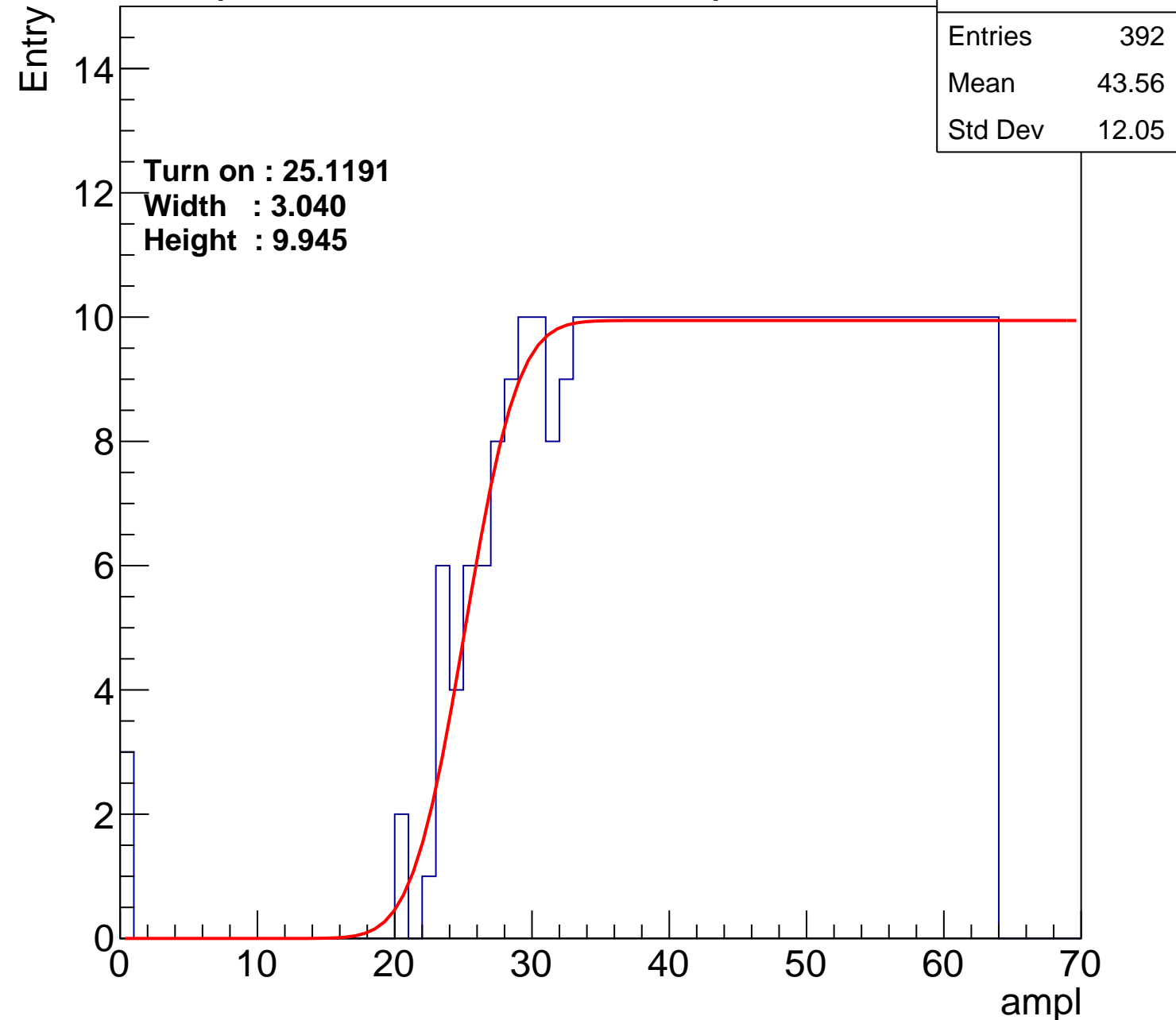
Width : 3.040

Height : 9.945

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch72

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	393
Mean	43.39
Std Dev	12.4

Turn on : 25.5500

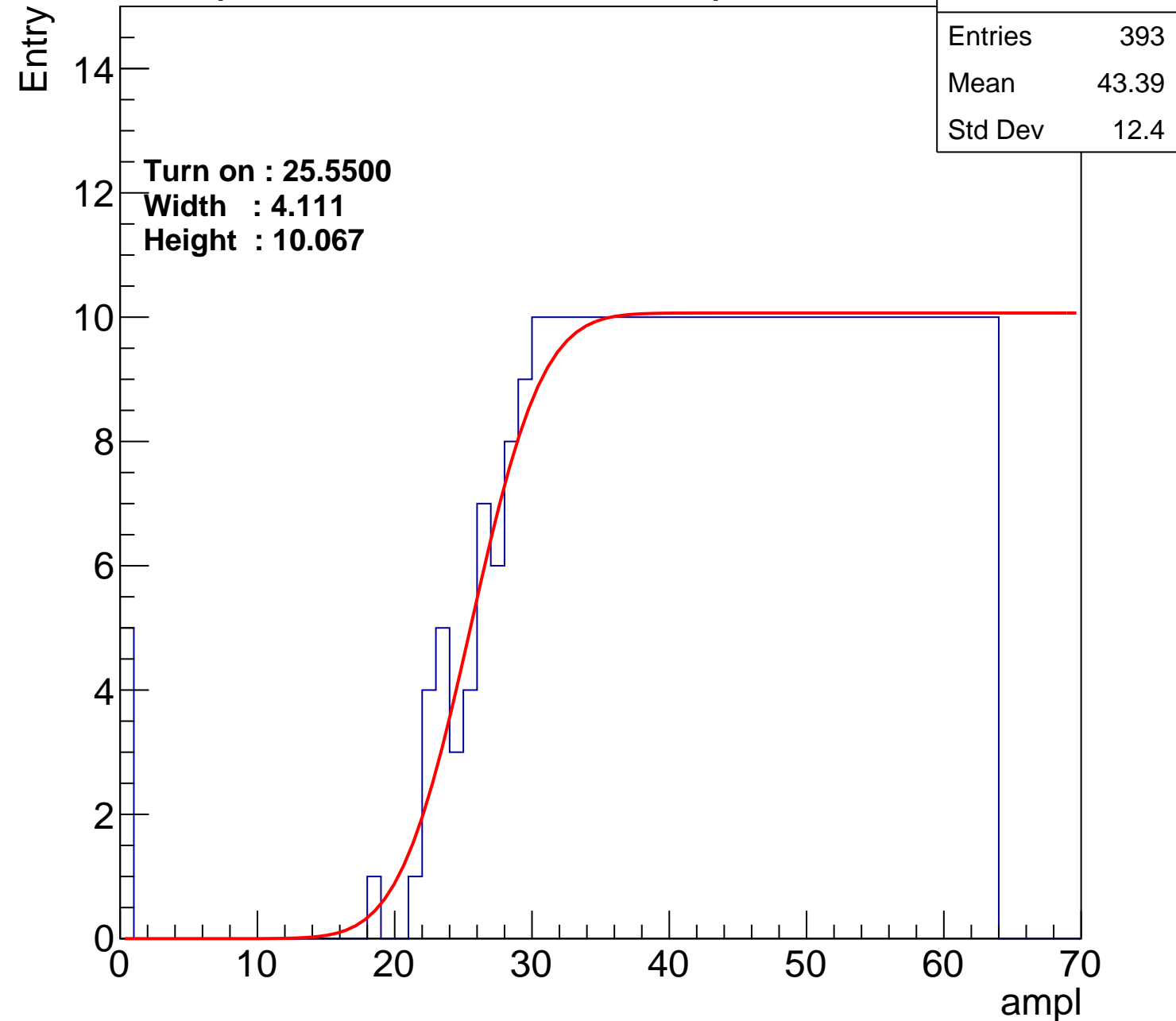
Width : 4.111

Height : 10.067

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch73

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	383
Mean	43.96
Std Dev	11.97

Turn on : 26.3395

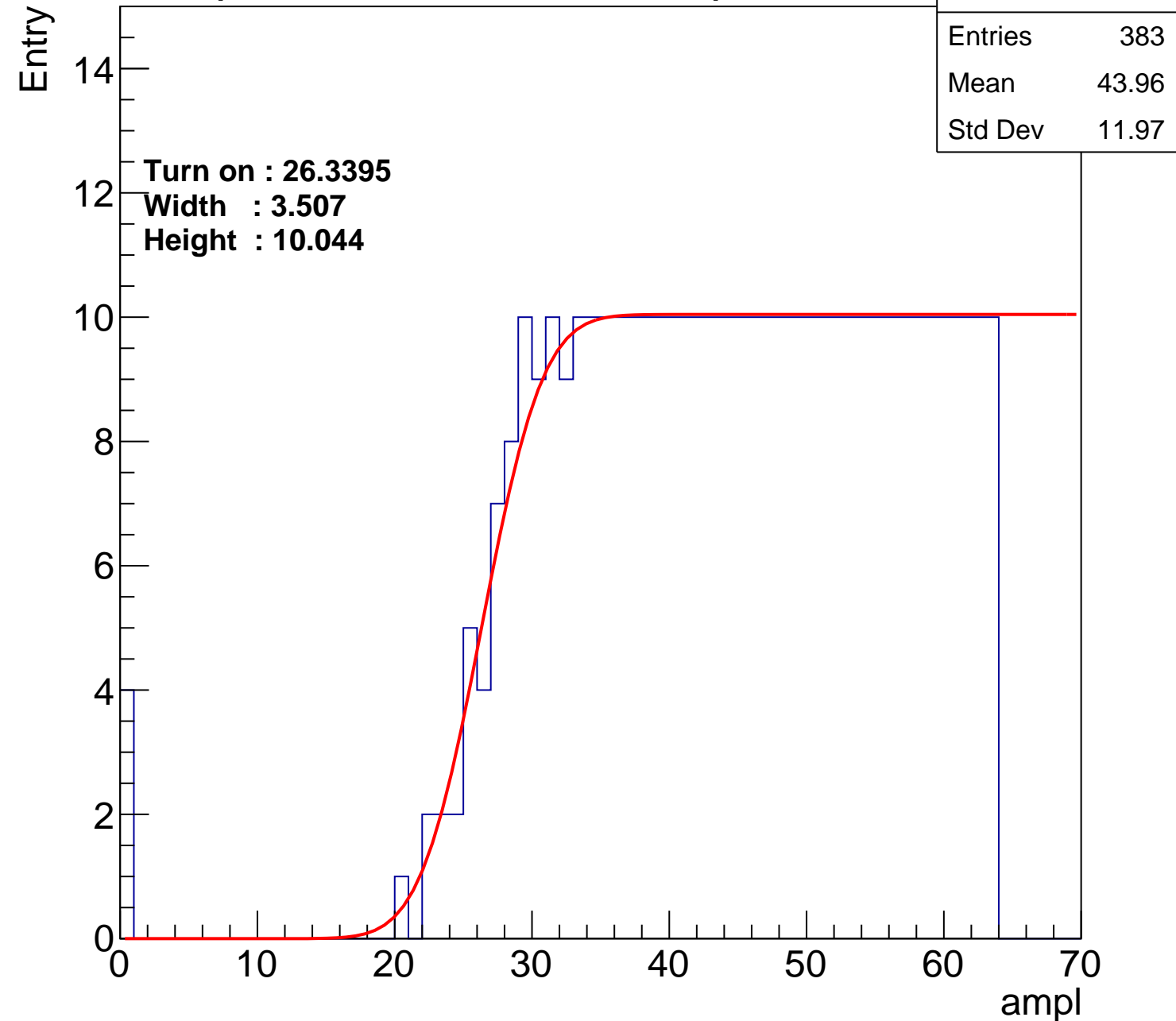
Width : 3.507

Height : 10.044

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch74

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	387
Mean	43.75
Std Dev	12.09

Turn on : 26.5591

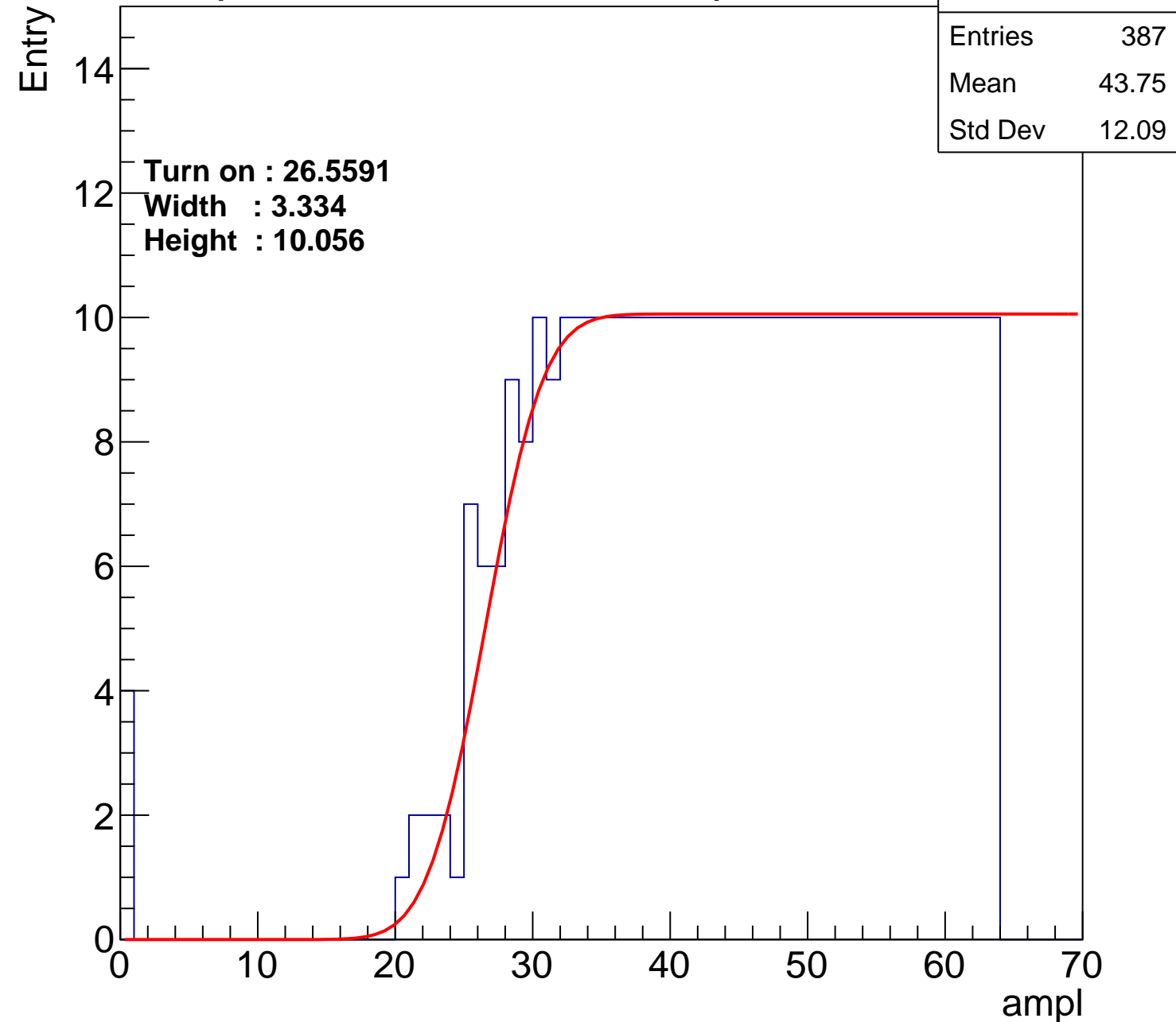
Width : 3.334

Height : 10.056

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch75

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	391
Mean	43.63
Std Dev	12

Turn on : 25.5981

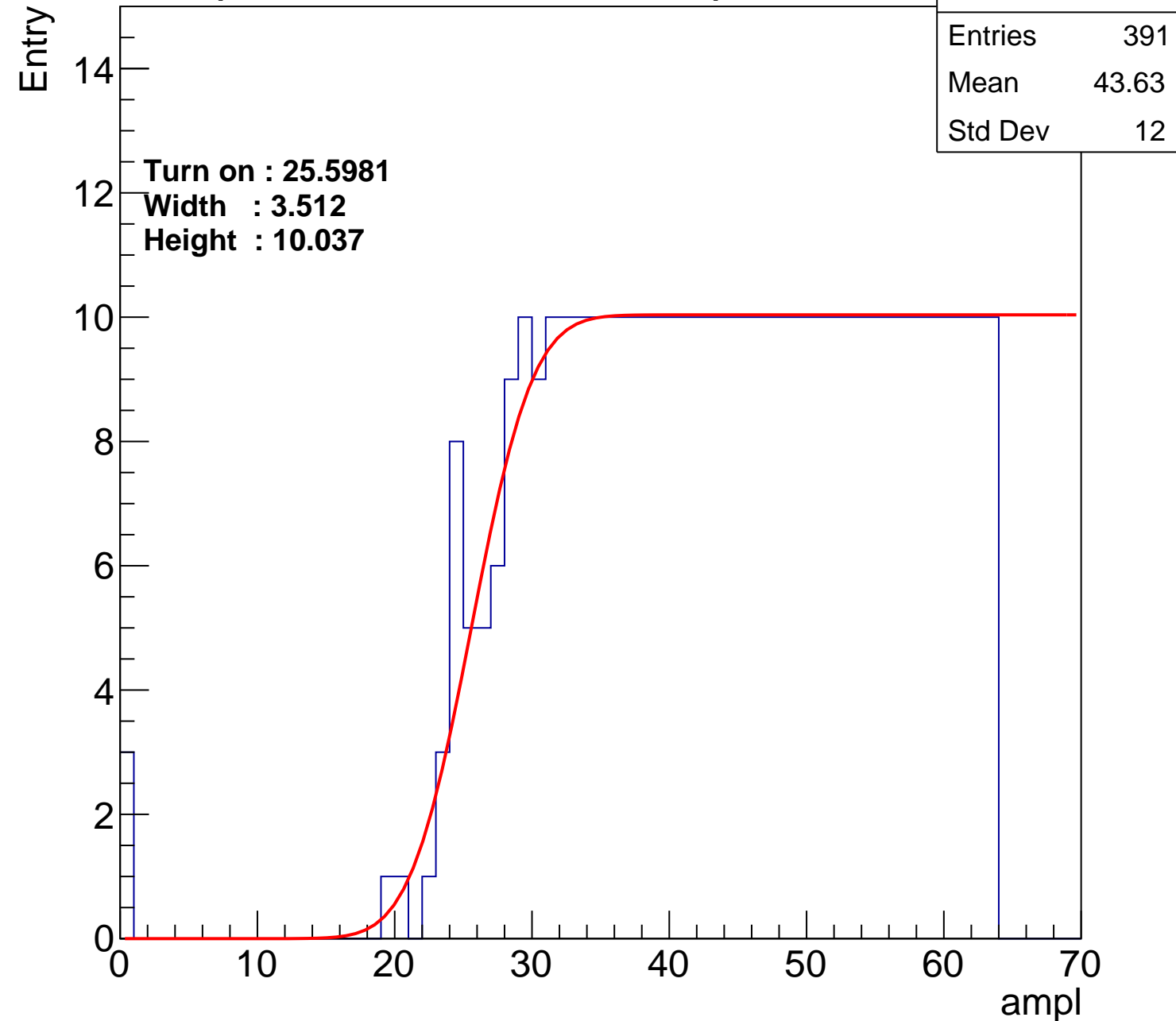
Width : 3.512

Height : 10.037

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch76

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	379
Mean	44.3
Std Dev	11.51

Turn on : 26.5132

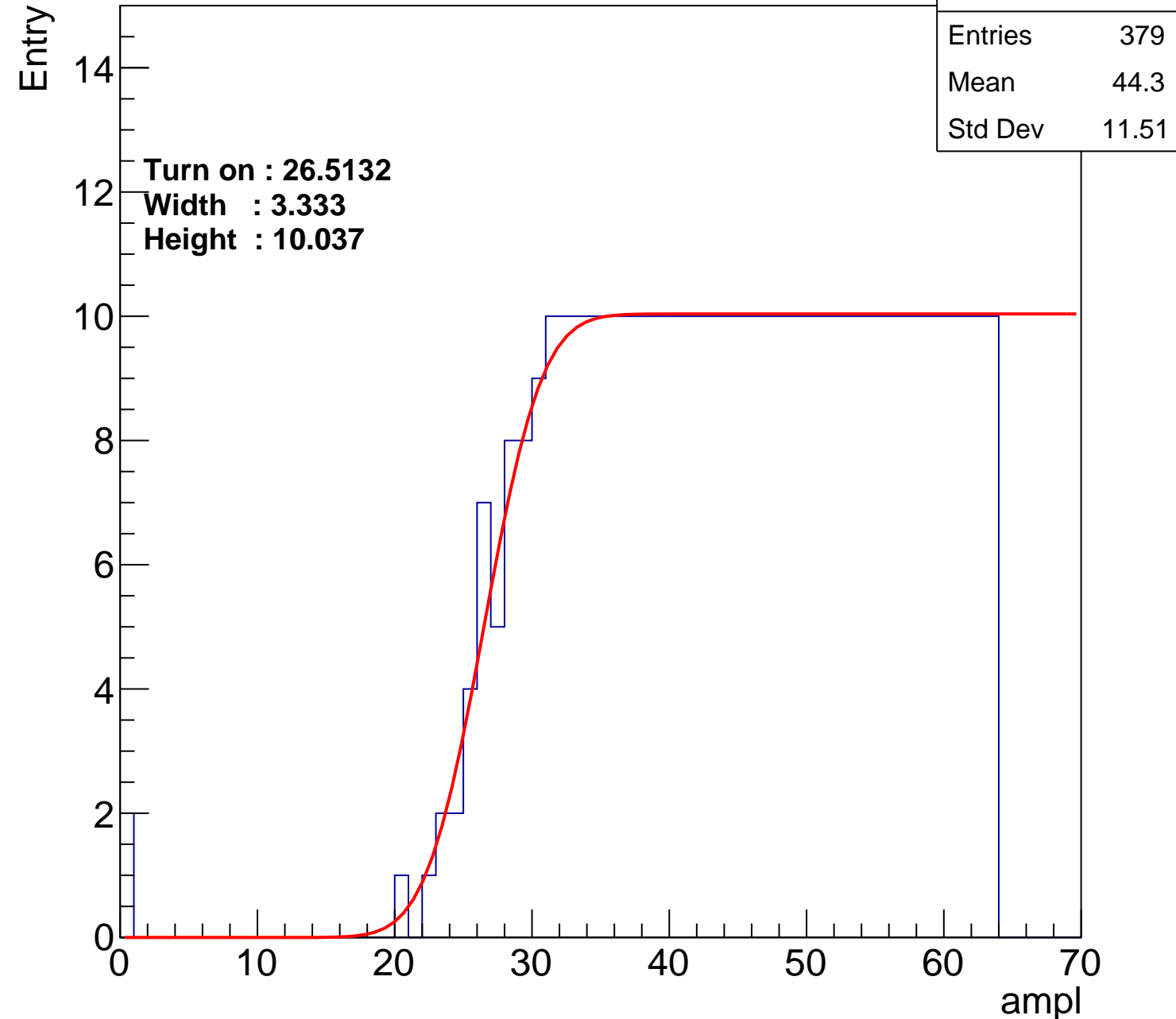
Width : 3.333

Height : 10.037

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch77

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	386
Mean	43.97
Std Dev	11.67

Turn on : 25.9490

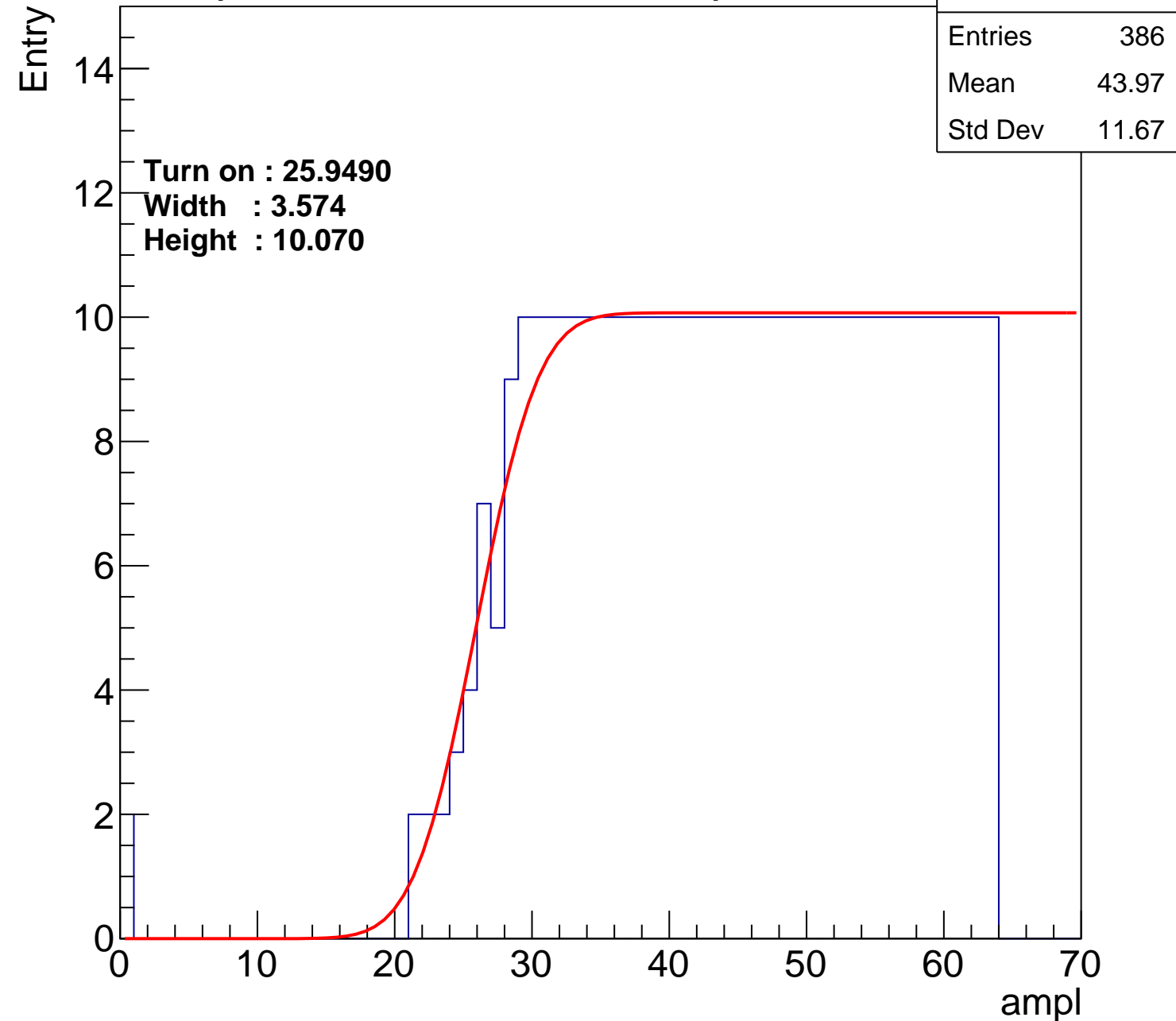
Width : 3.574

Height : 10.070

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch78

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	387
Mean	43.94
Std Dev	11.6

Turn on : 25.6465

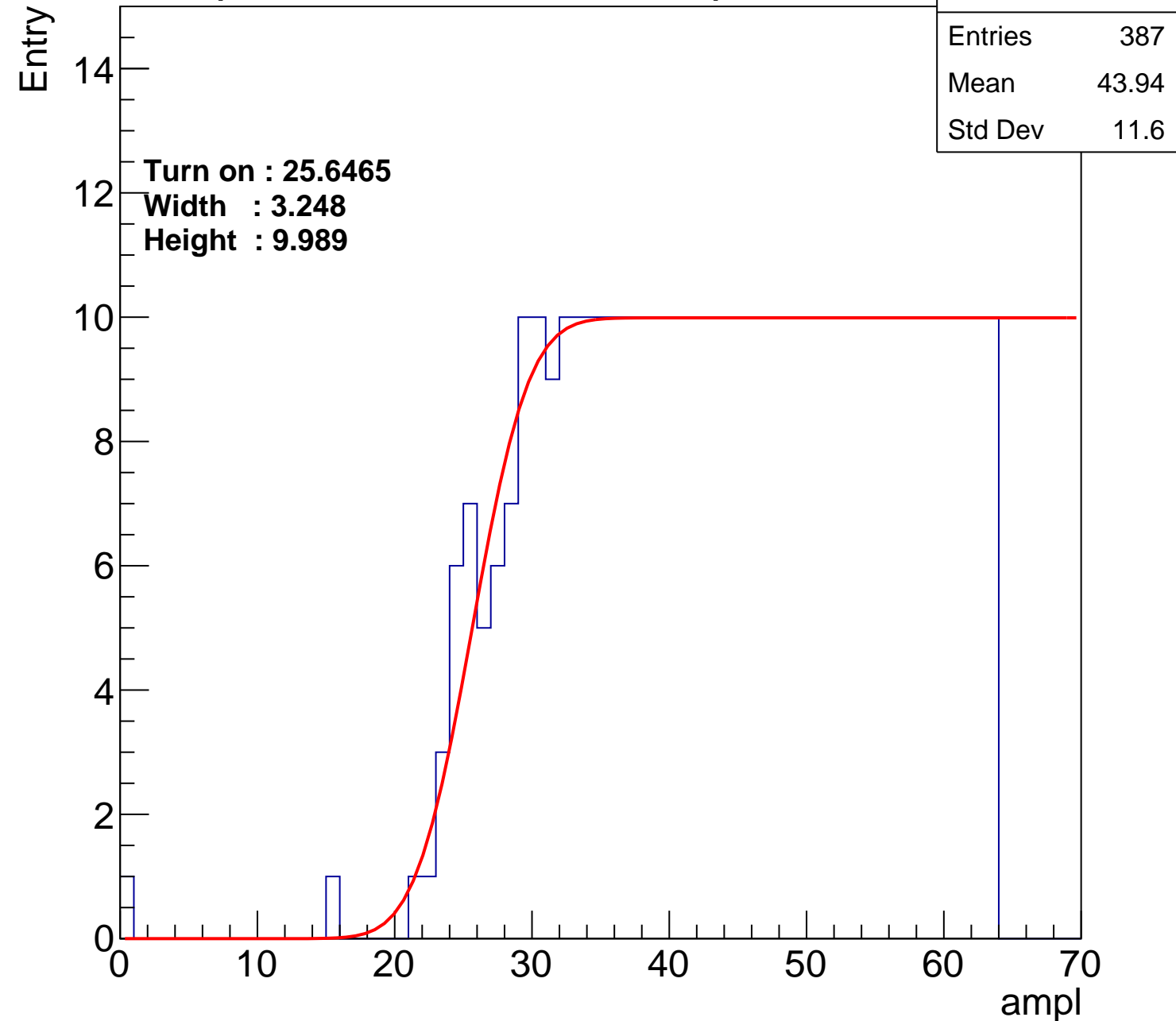
Width : 3.248

Height : 9.989

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L102S, U2-ch79

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	384
Mean	44.02
Std Dev	11.68

Turn on : 25.7766

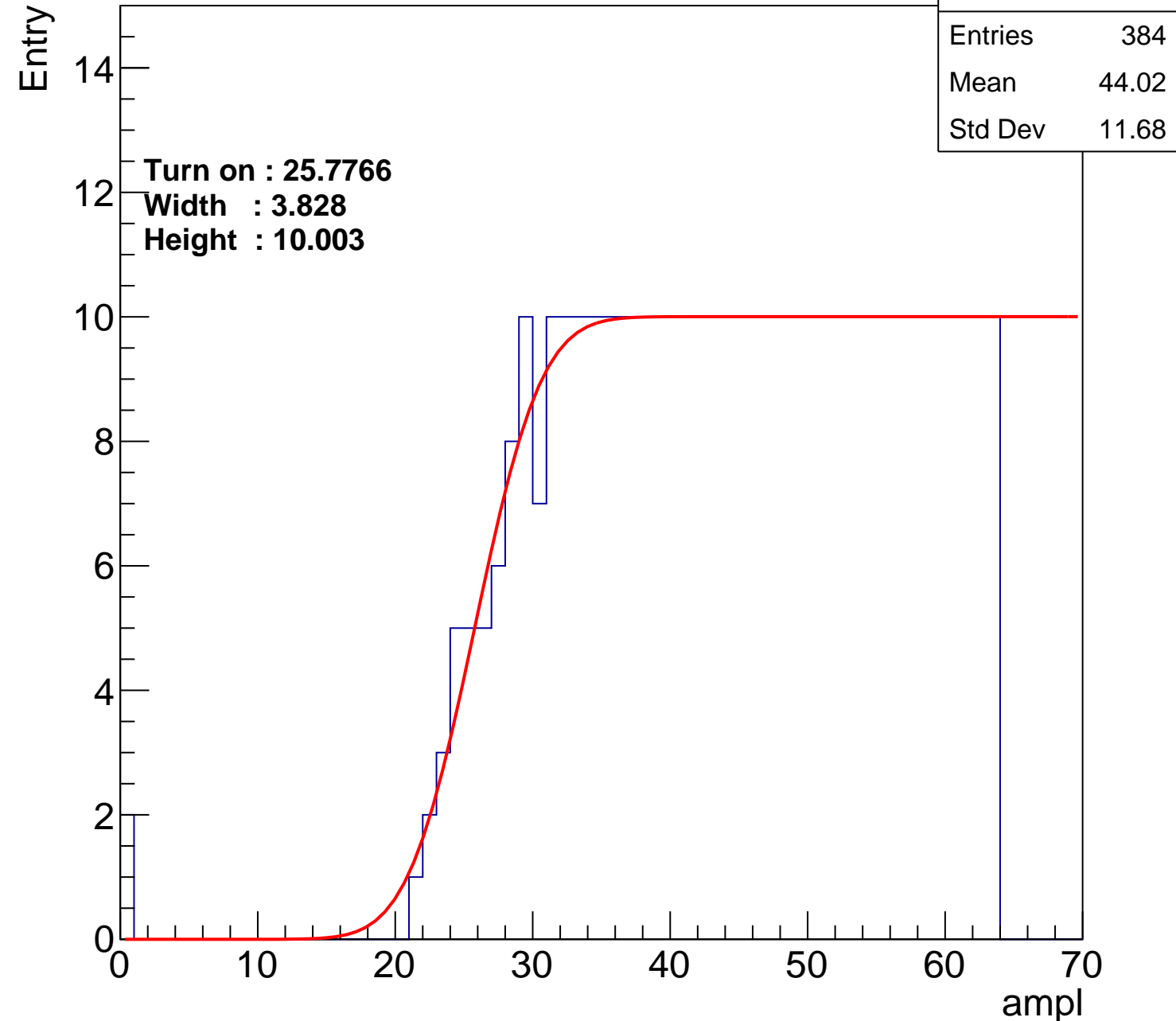
Width : 3.828

Height : 10.003

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch80

calib\_packv5\_042523\_0143.root, FC#11, port A2

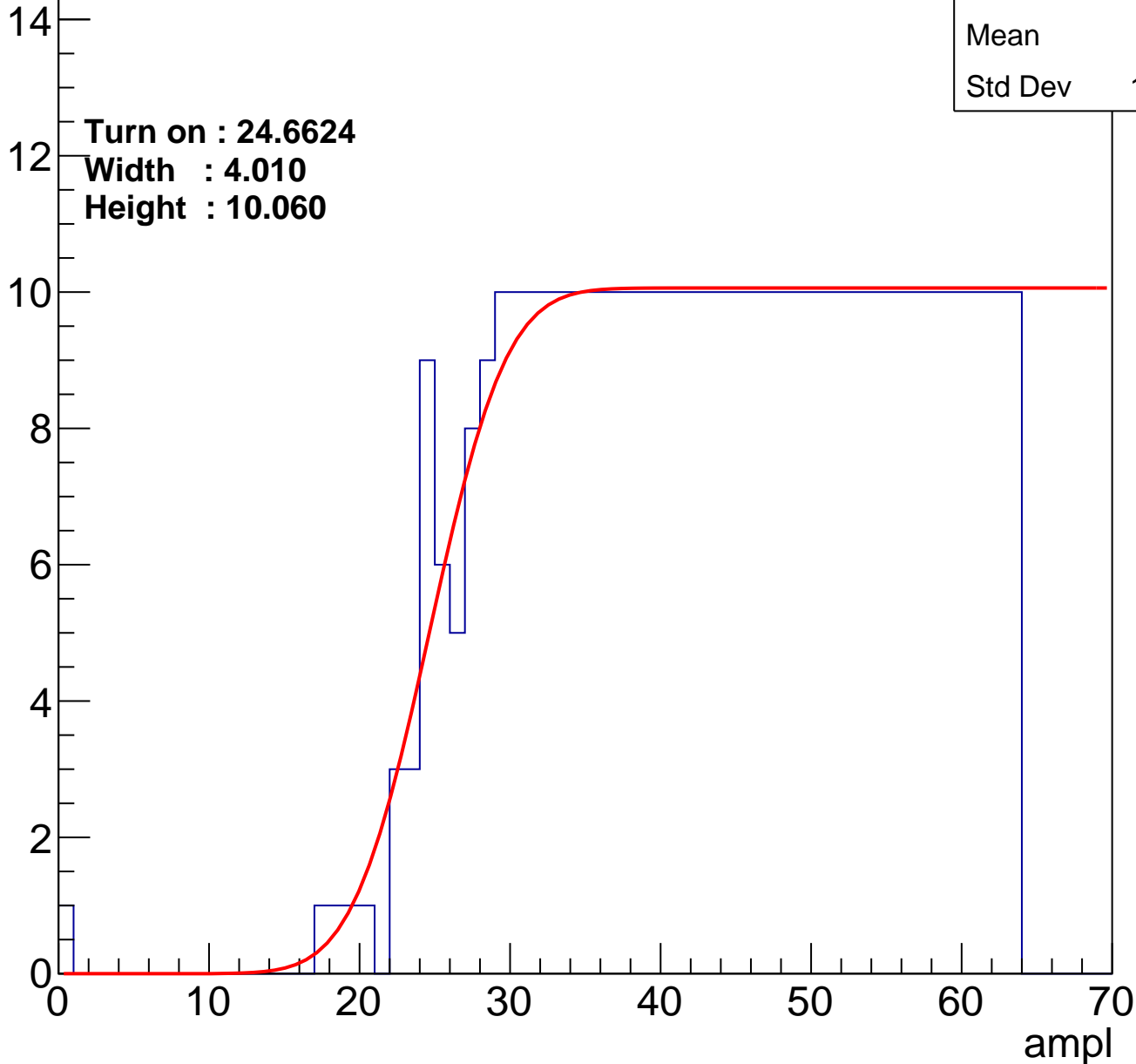
Entries	398
Mean	43.4
Std Dev	11.89

**Turn on : 24.6624**

**Width : 4.010**

**Height : 10.060**

Entry



# B1L102S, U2-ch81

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	383
Mean	44.11
Std Dev	11.6

Turn on : 26.0373

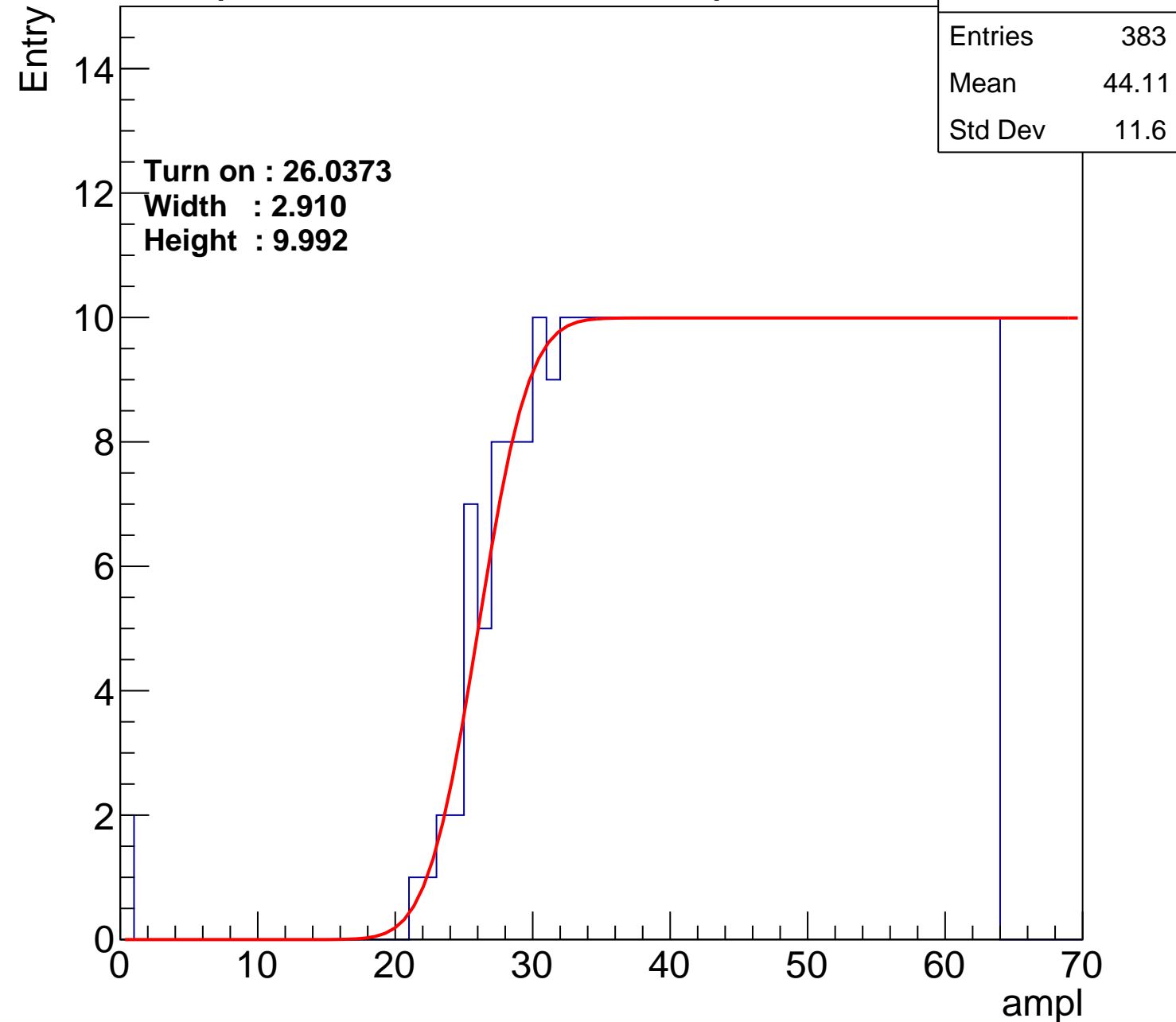
Width : 2.910

Height : 9.992

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch82

calib\_packv5\_042523\_0143.root, FC#11, port A2

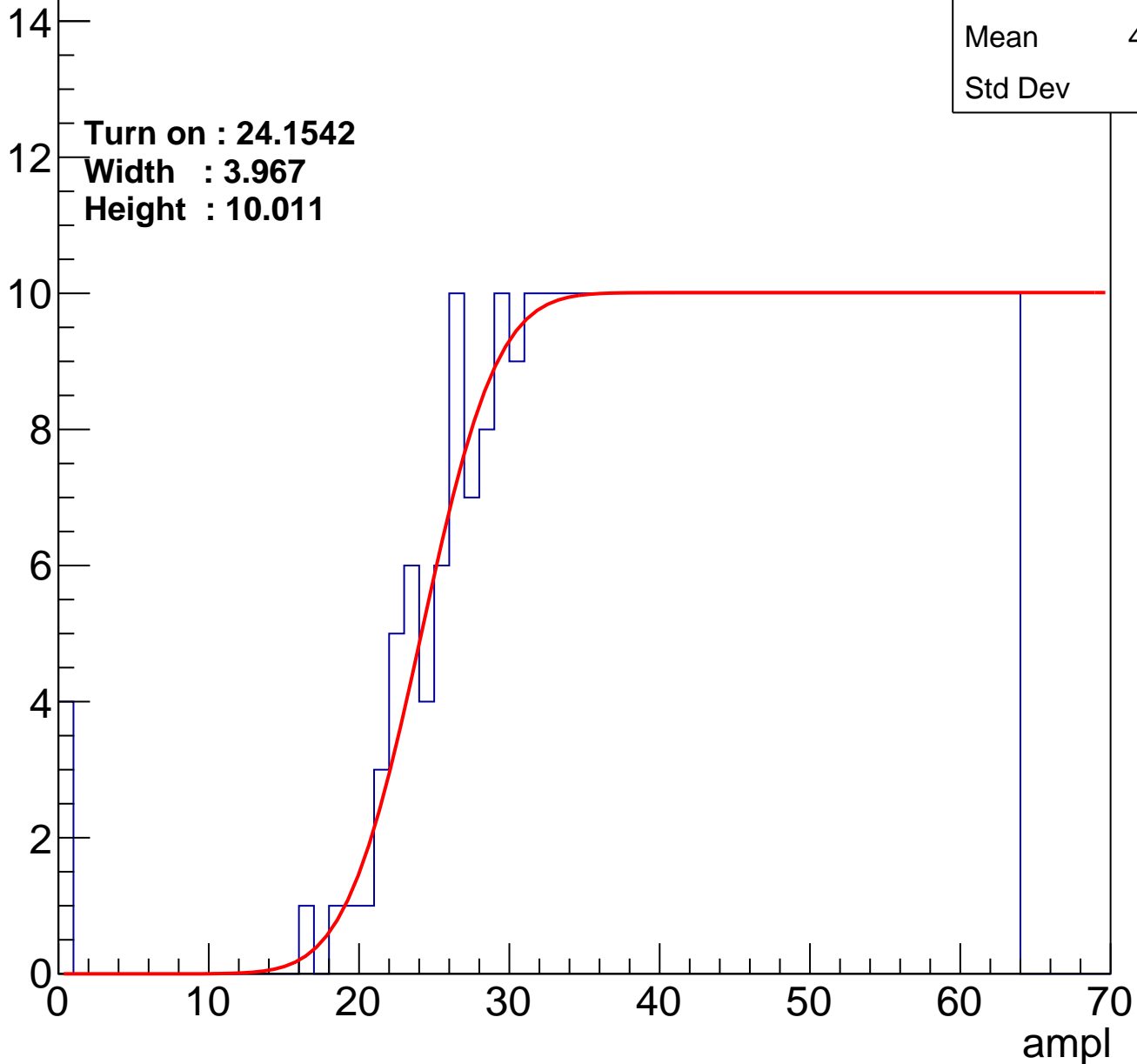
Entries	406
Mean	42.79
Std Dev	12.6

Turn on : 24.1542

Width : 3.967

Height : 10.011

Entry



# B1L102S, U2-ch83

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	367
Mean	44.84
Std Dev	11.36

Turn on : 27.4774

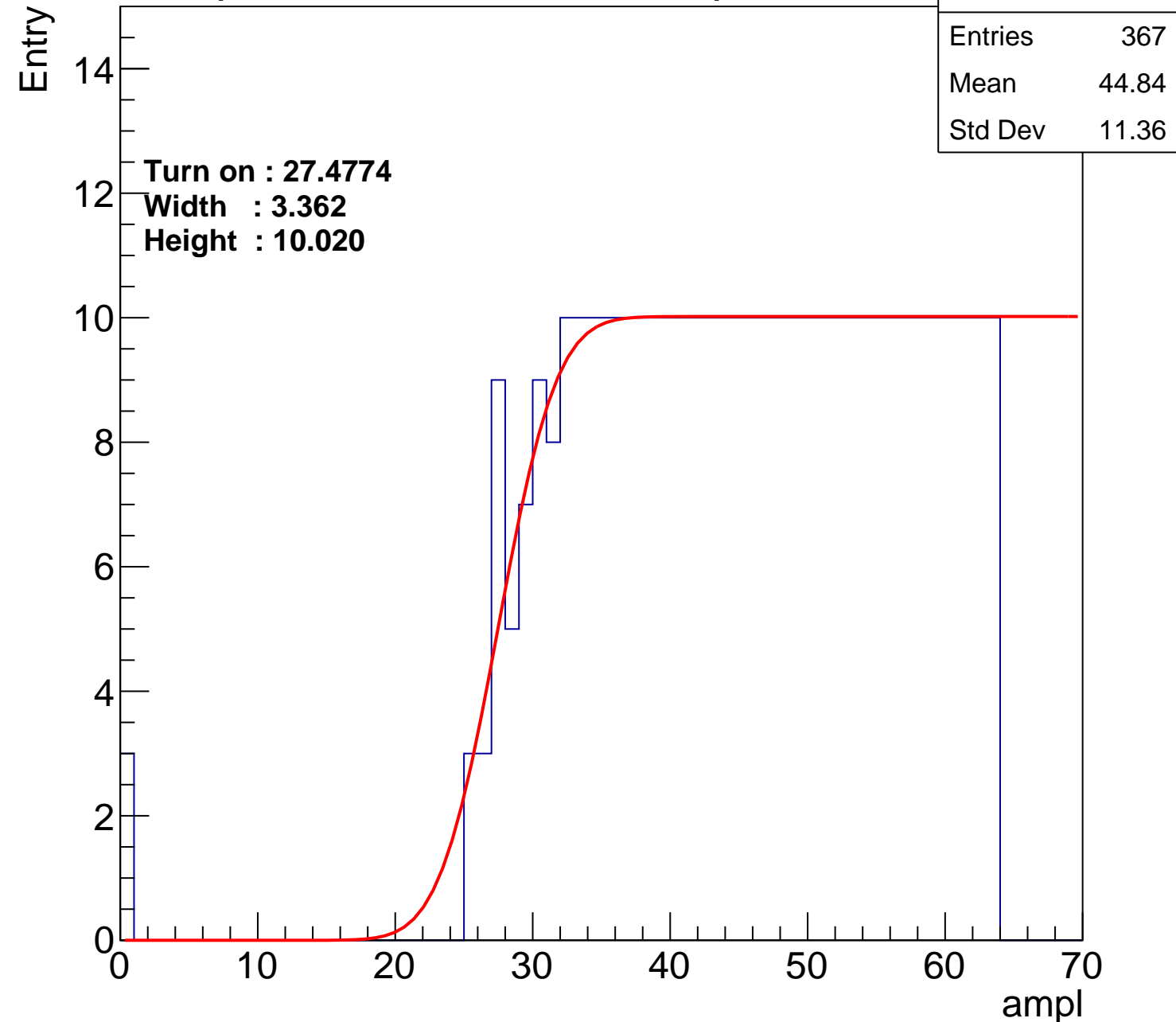
Width : 3.362

Height : 10.020

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch84

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	389
Mean	43.81
Std Dev	11.76

Turn on : 25.4636

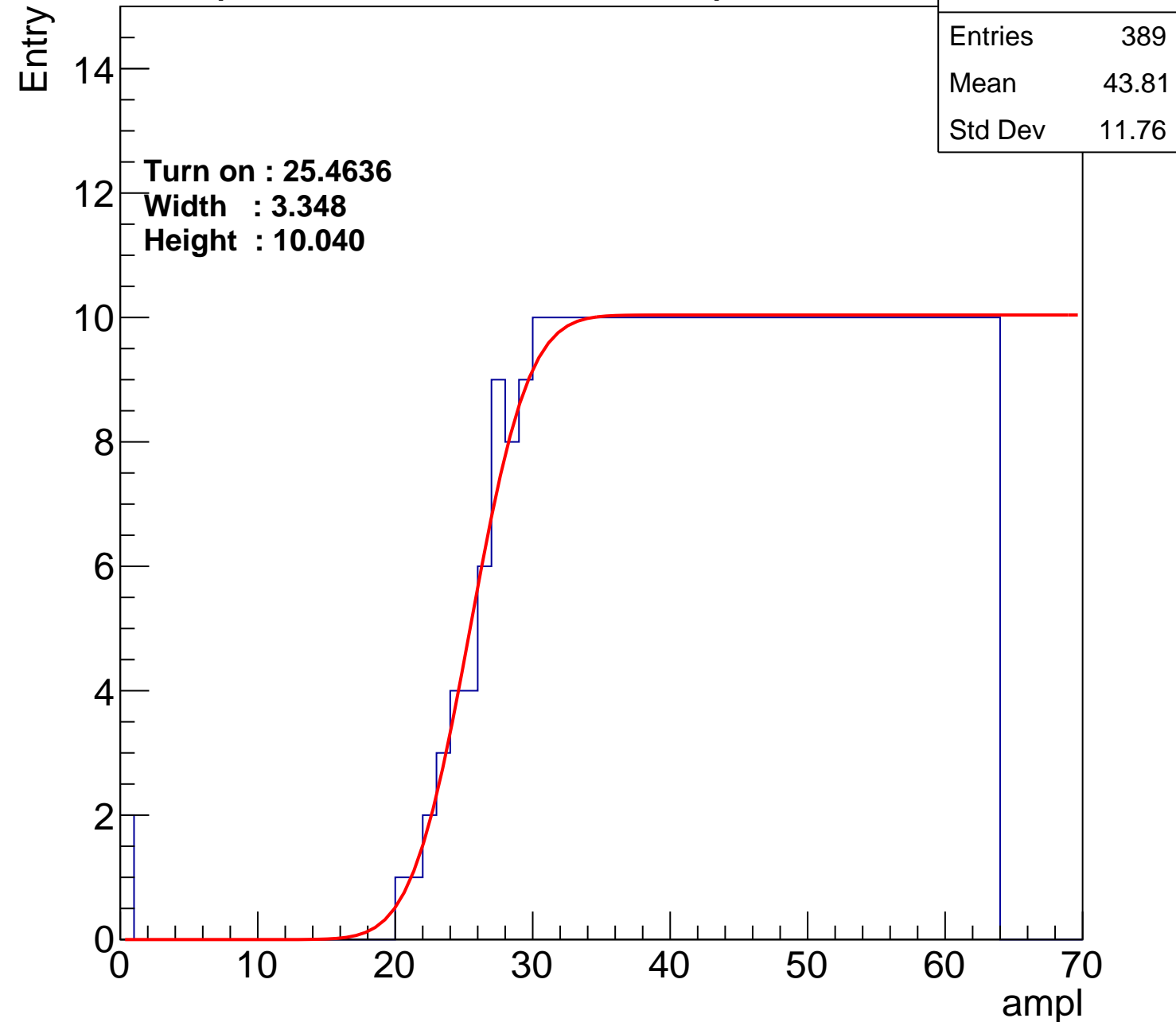
Width : 3.348

Height : 10.040

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch85

calib\_packv5\_042523\_0143.root, FC#11, port A2

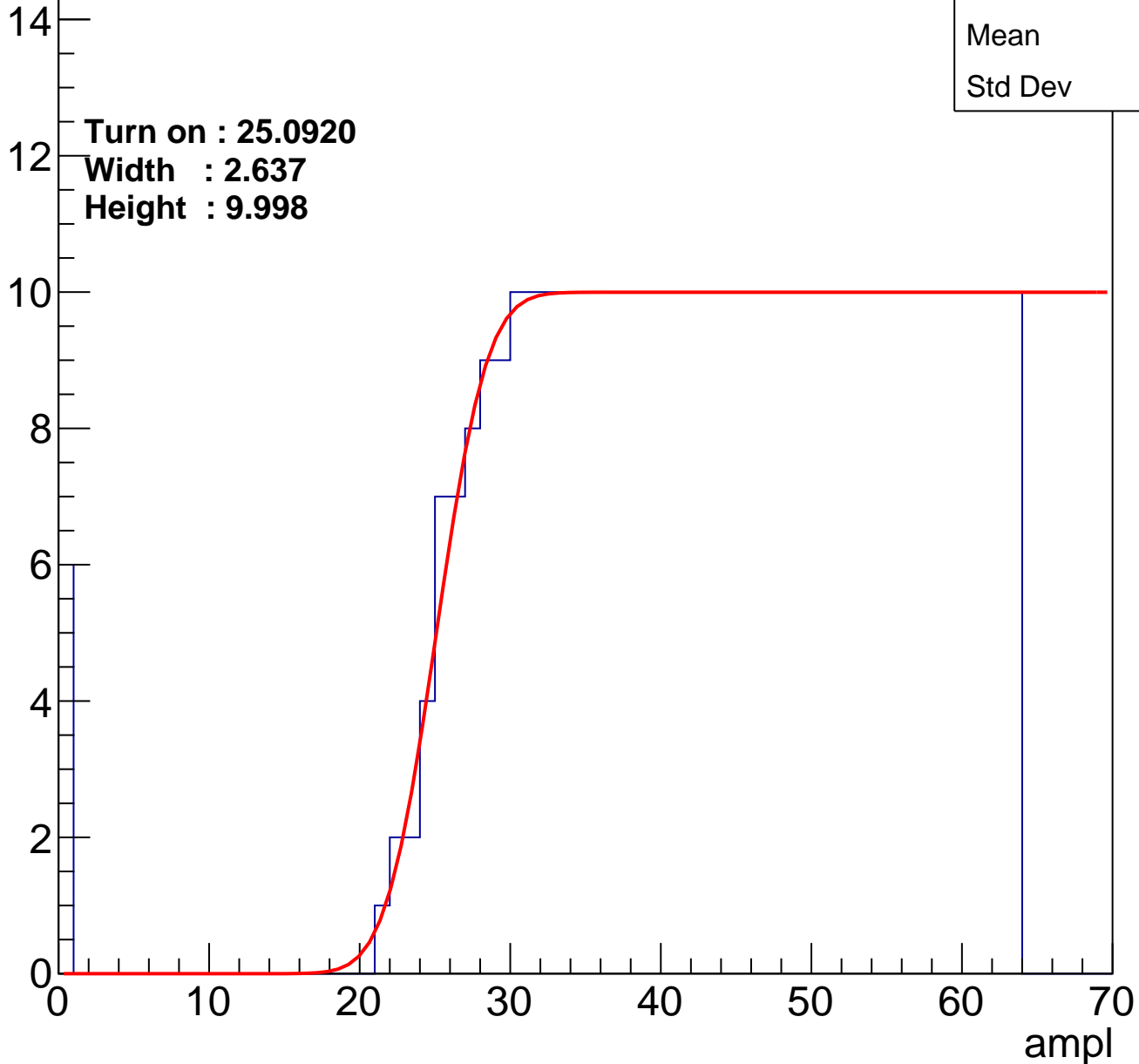
Entries	395
Mean	43.3
Std Dev	12.5

Turn on : 25.0920

Width : 2.637

Height : 9.998

Entry



# B1L102S, U2-ch86

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	378
Mean	44.29
Std Dev	11.58

Turn on : 26.8396

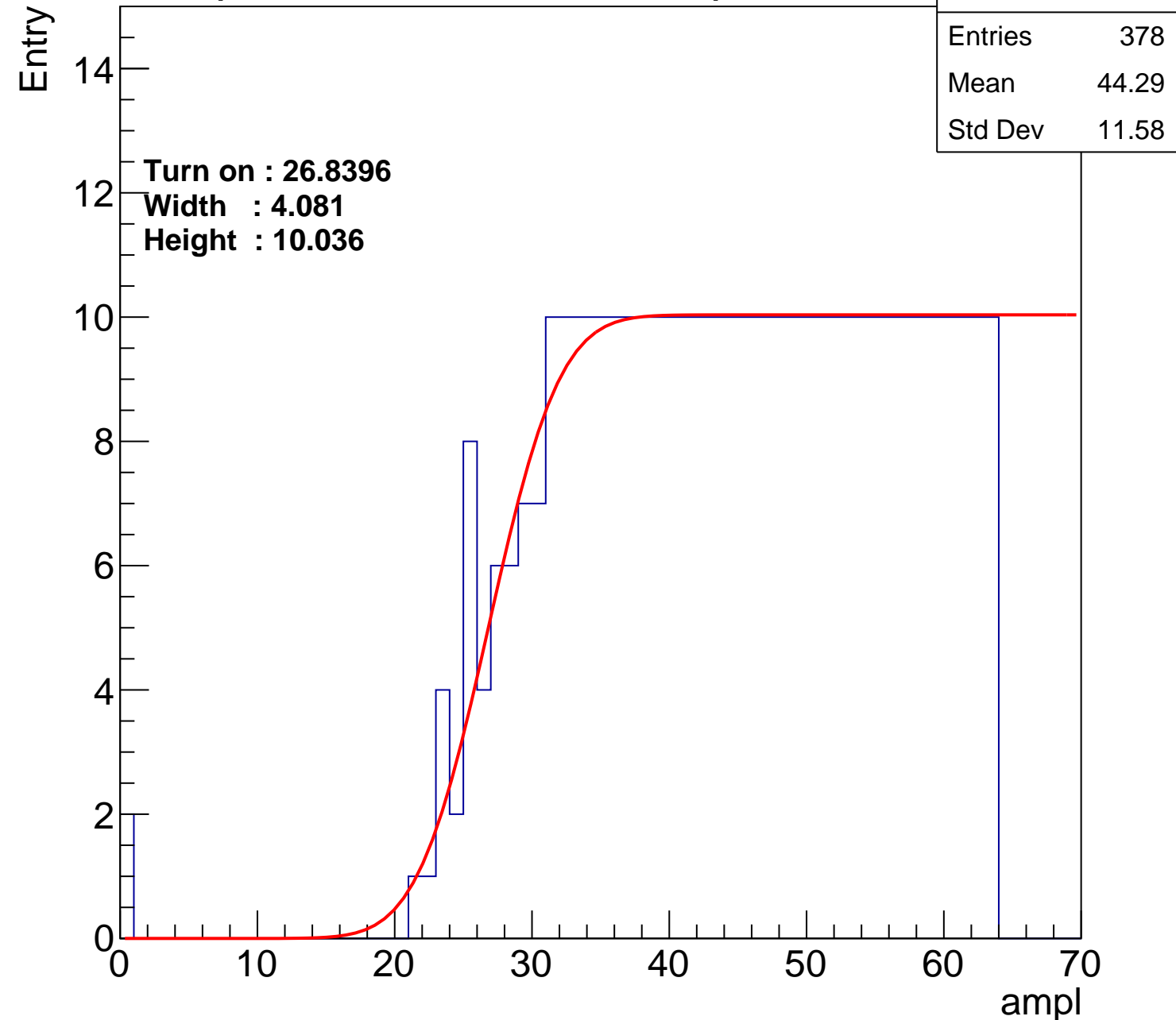
Width : 4.081

Height : 10.036

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L102S, U2-ch87

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	379
Mean	44.25
Std Dev	11.94

Turn on : 27.2691

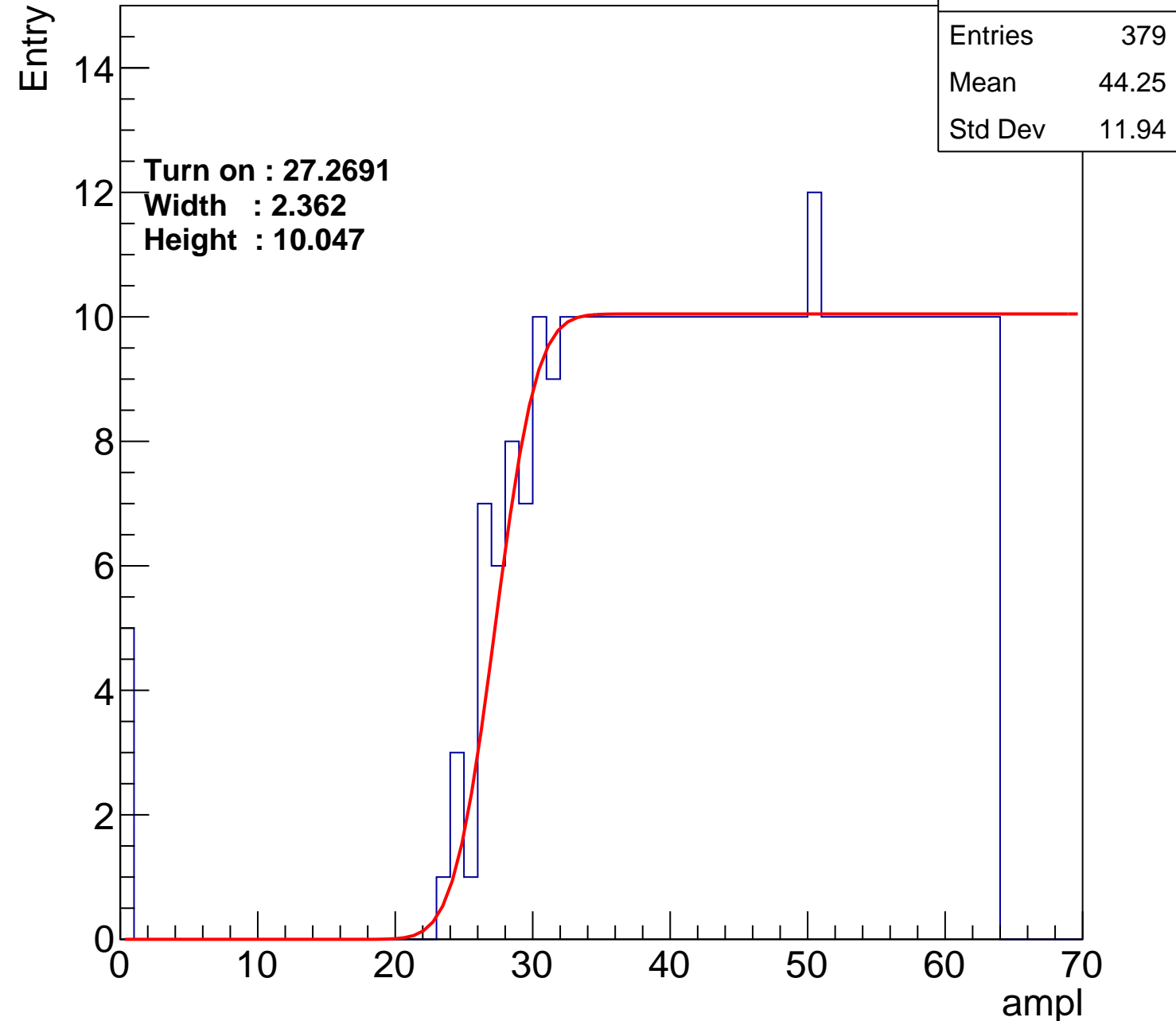
Width : 2.362

Height : 10.047

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch88

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	395
Mean	43.48
Std Dev	12.04

Turn on : 25.3434

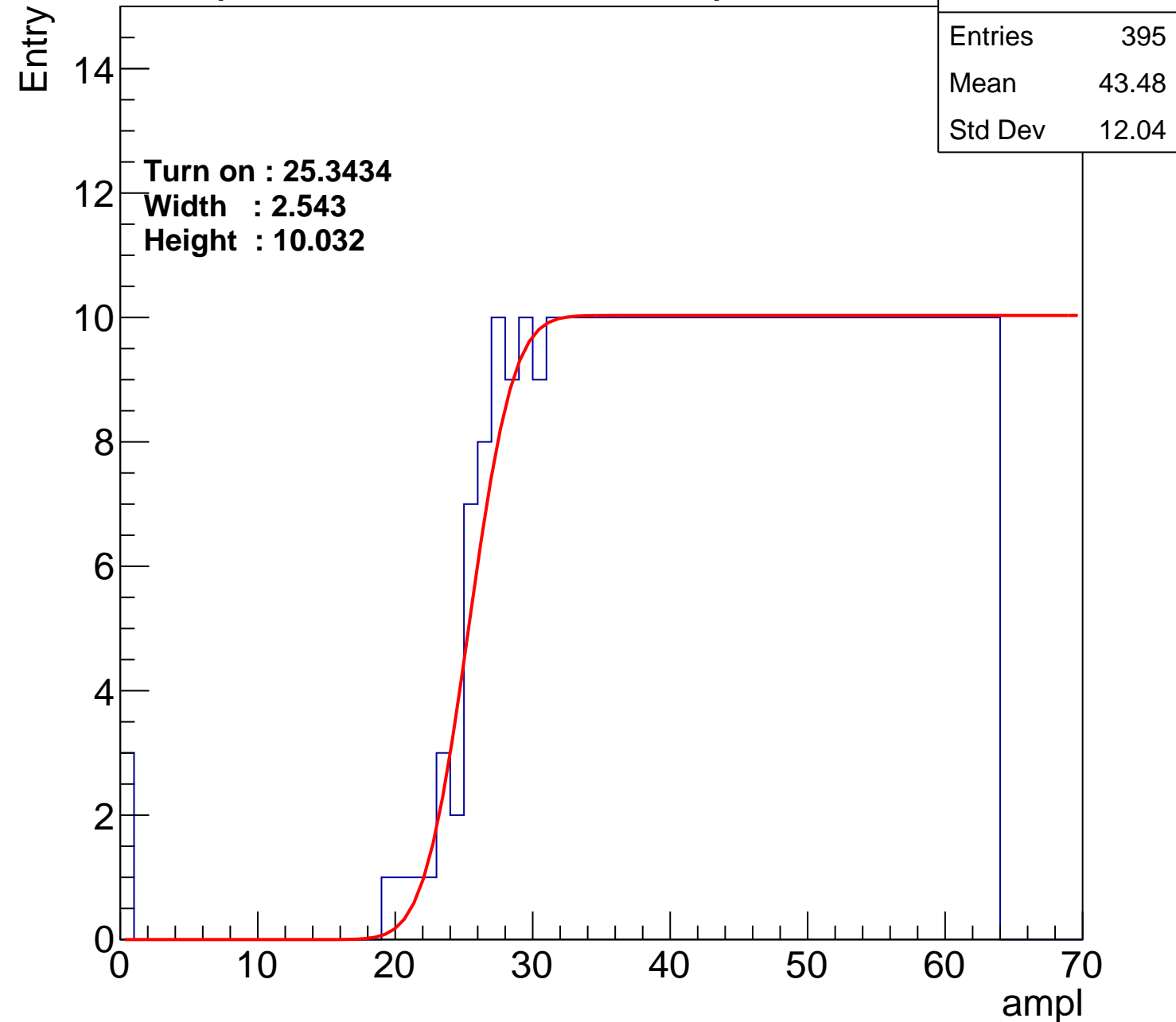
Width : 2.543

Height : 10.032

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch89

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	400
Mean	43.09
Std Dev	12.51

**Turn on : 24.9626**

**Width : 3.643**

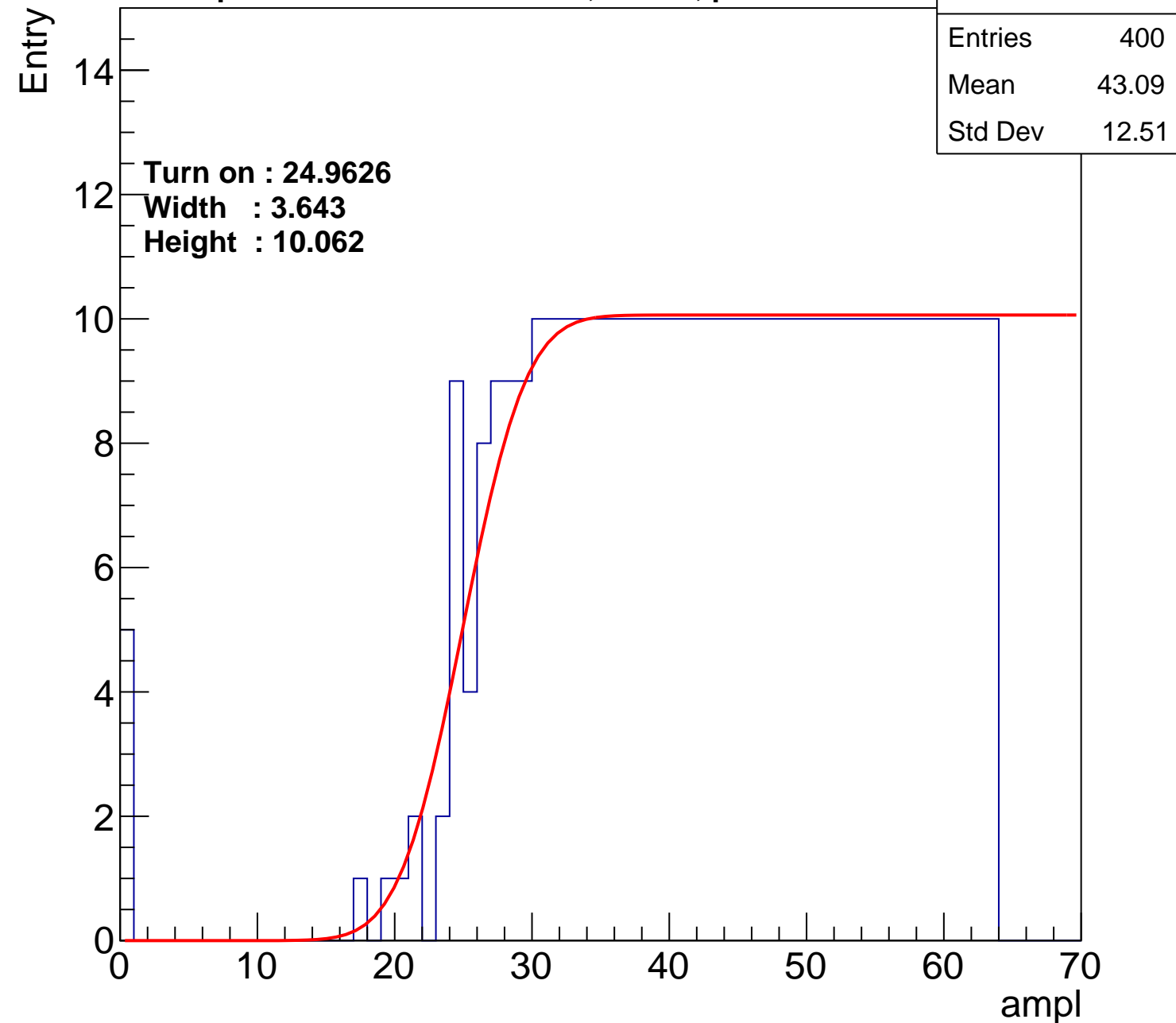
**Height : 10.062**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U2-ch90

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	383
Mean	44.06
Std Dev	11.74

Turn on : 25.7520

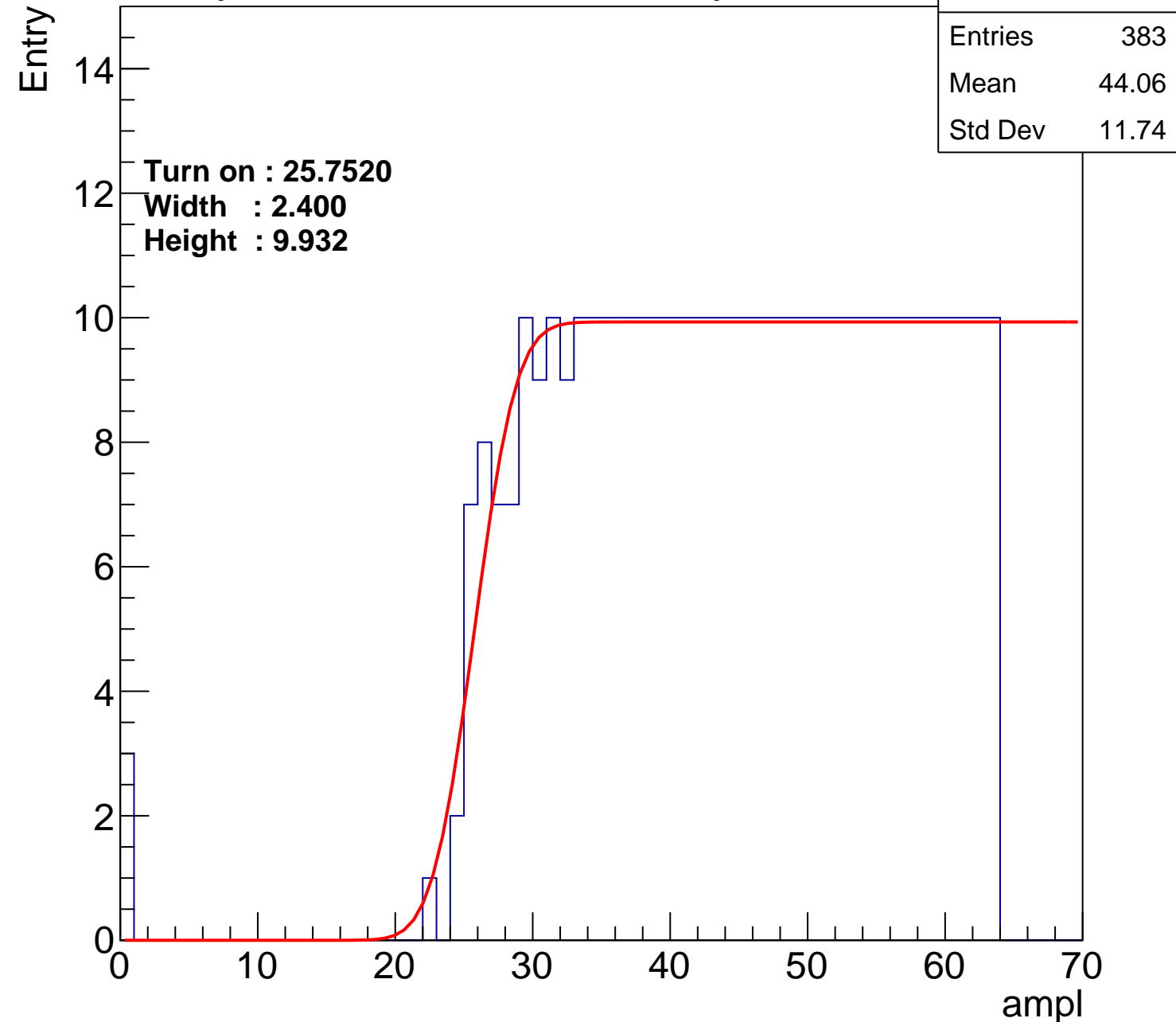
Width : 2.400

Height : 9.932

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch91

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	381
Mean	44.26
Std Dev	11.4

Turn on : 25.9030

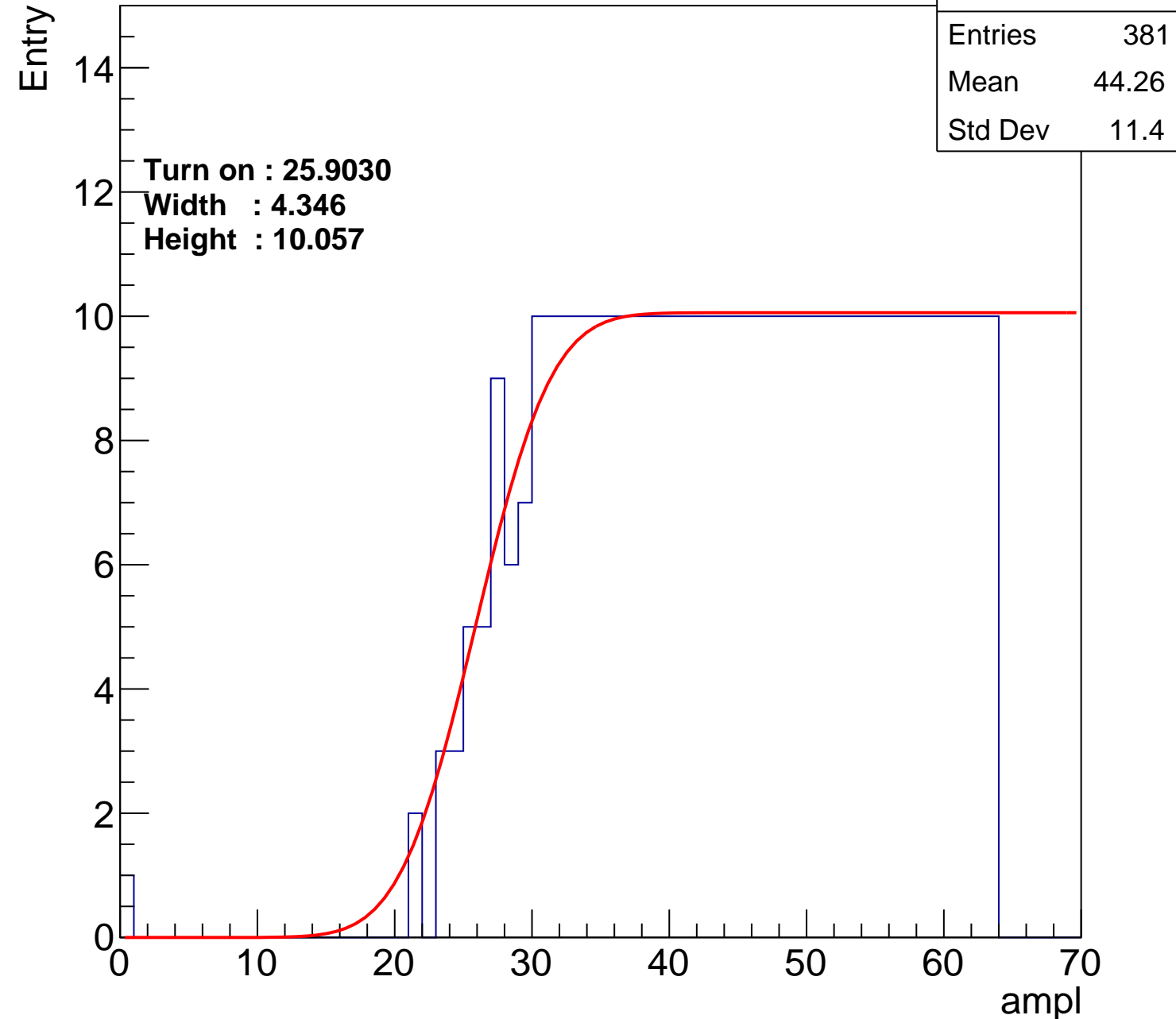
Width : 4.346

Height : 10.057

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch92

calib\_packv5\_042523\_0143.root, FC#11, port A2

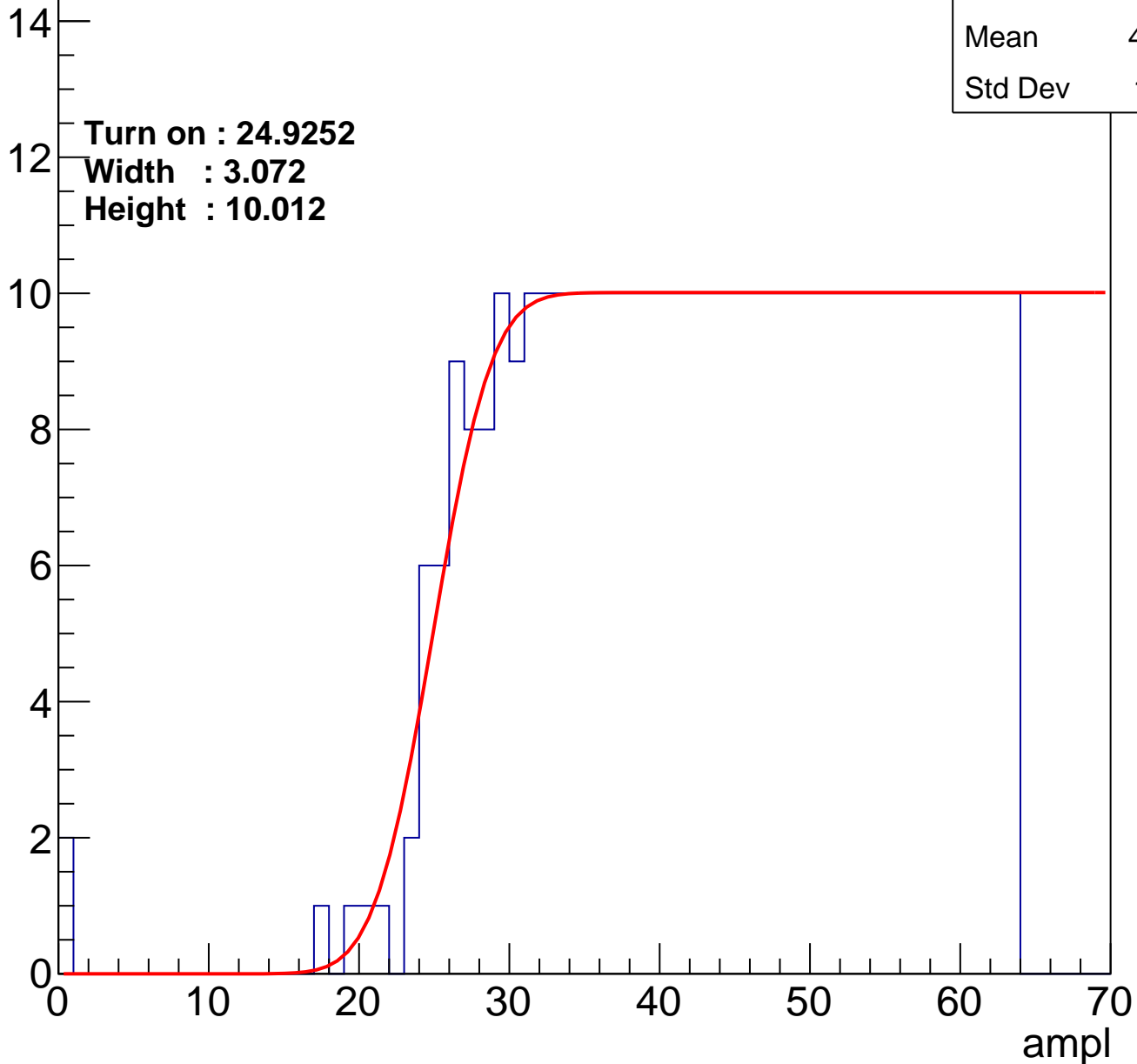
Entries	394
Mean	43.56
Std Dev	11.91

Turn on : 24.9252

Width : 3.072

Height : 10.012

Entry



# B1L102S, U2-ch93

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	392
Mean	43.68
Std Dev	11.81

Turn on : 25.2583

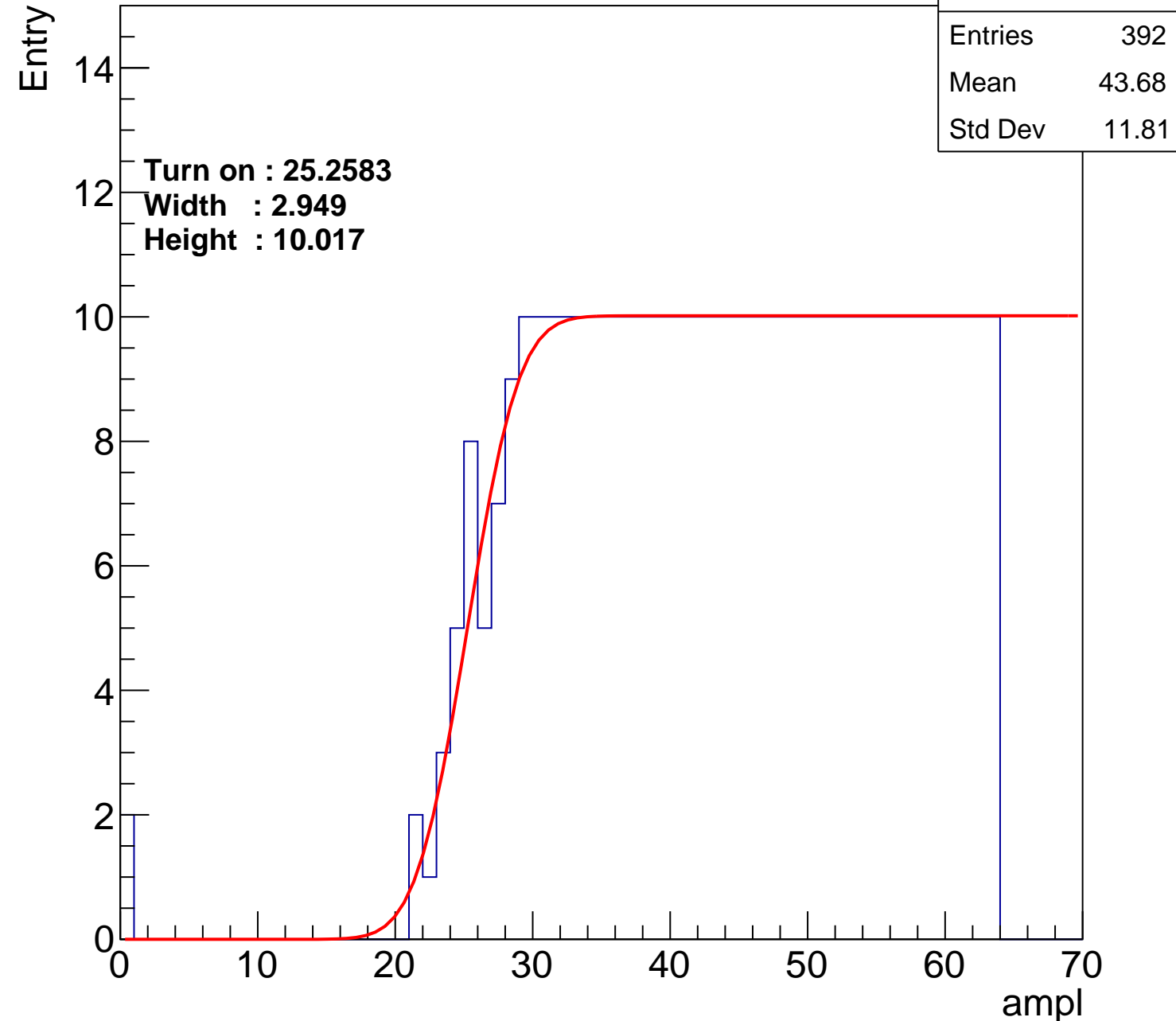
Width : 2.949

Height : 10.017

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch94

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	384
Mean	44.08
Std Dev	11.53

Turn on : 26.4595

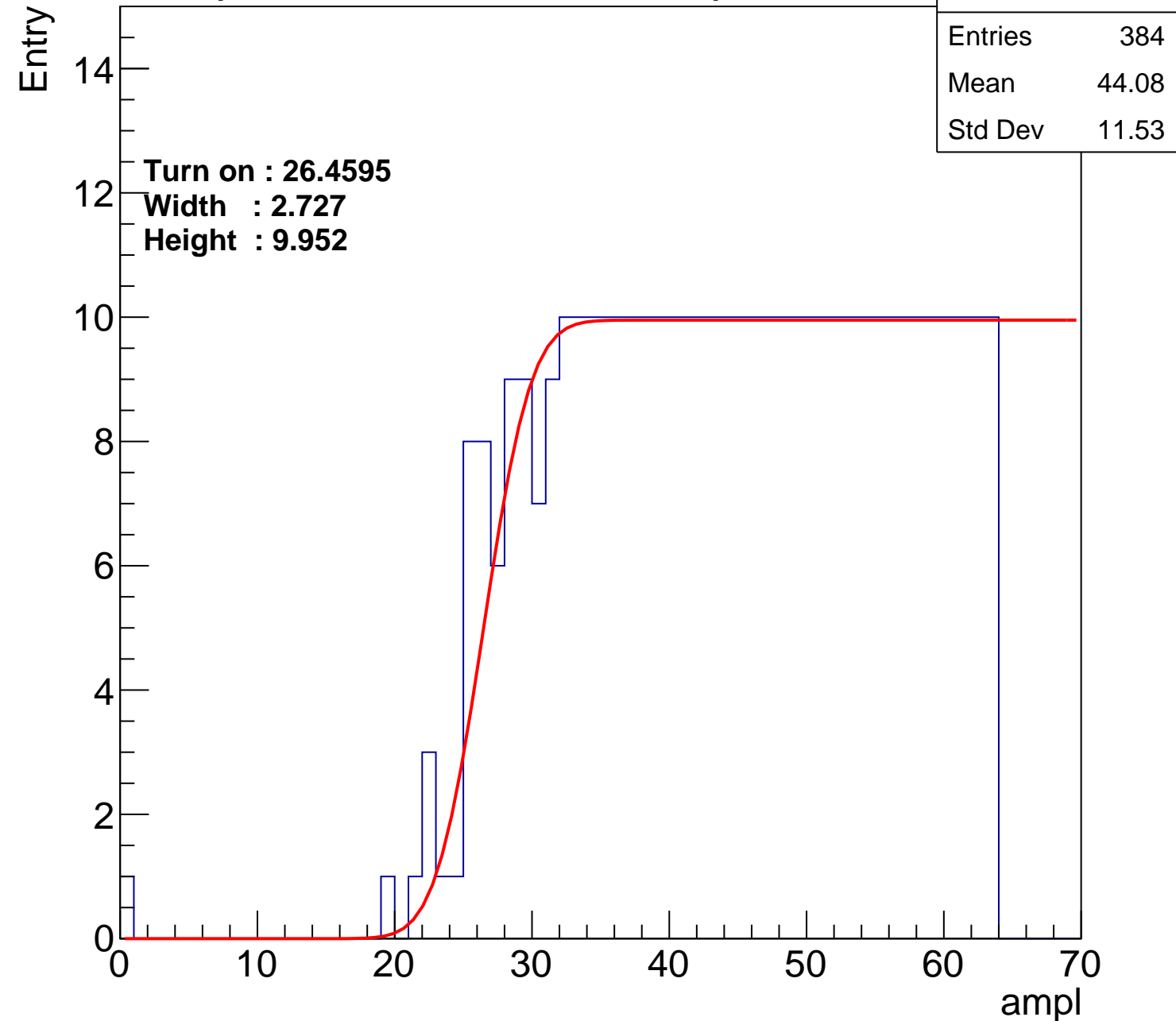
Width : 2.727

Height : 9.952

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L102S, U2-ch95

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	394
Mean	43.57
Std Dev	11.83

**Turn on : 25.3479**

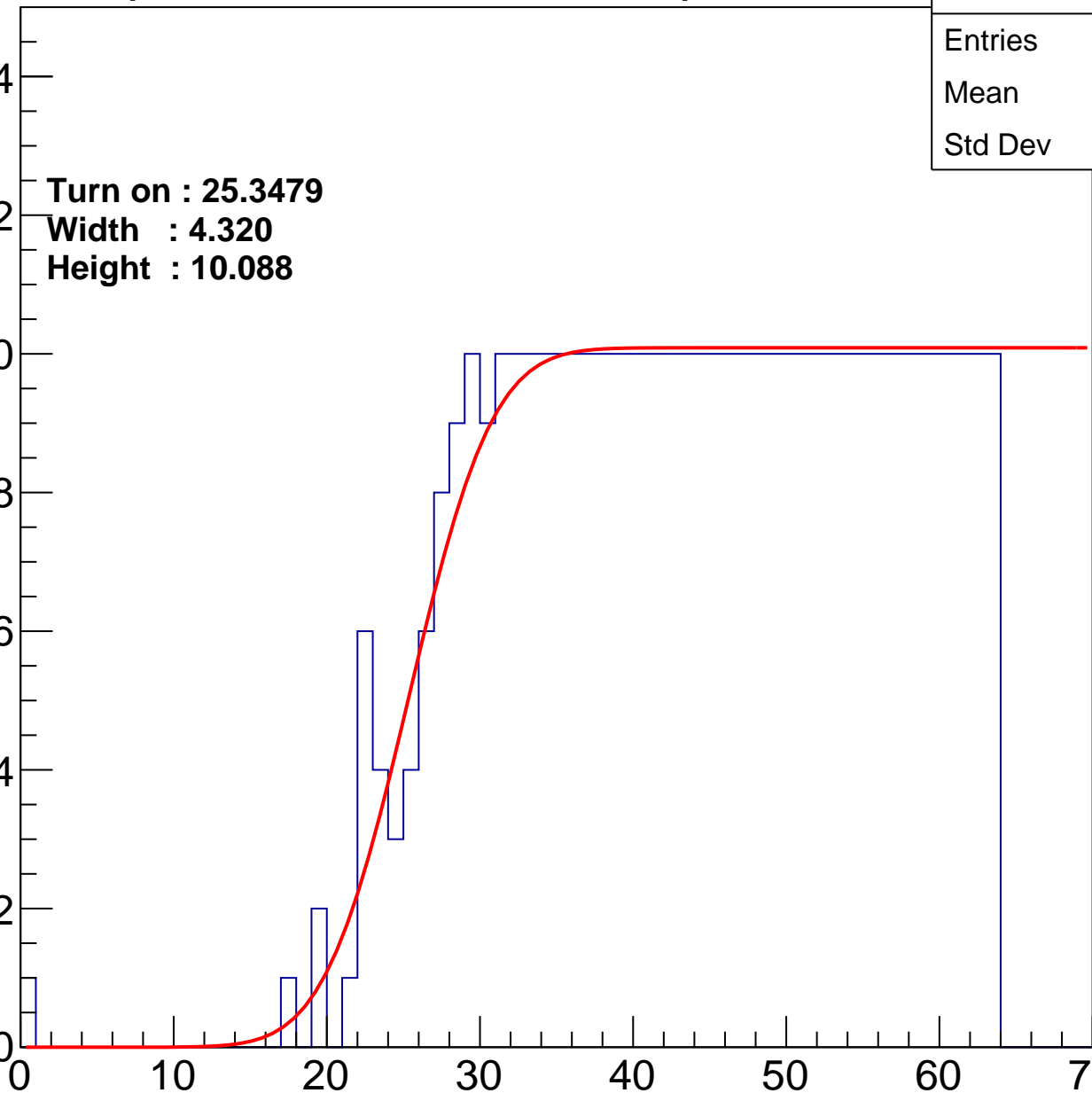
**Width : 4.320**

**Height : 10.088**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch96

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	381
Mean	44.14
Std Dev	11.73

Turn on : 26.6821

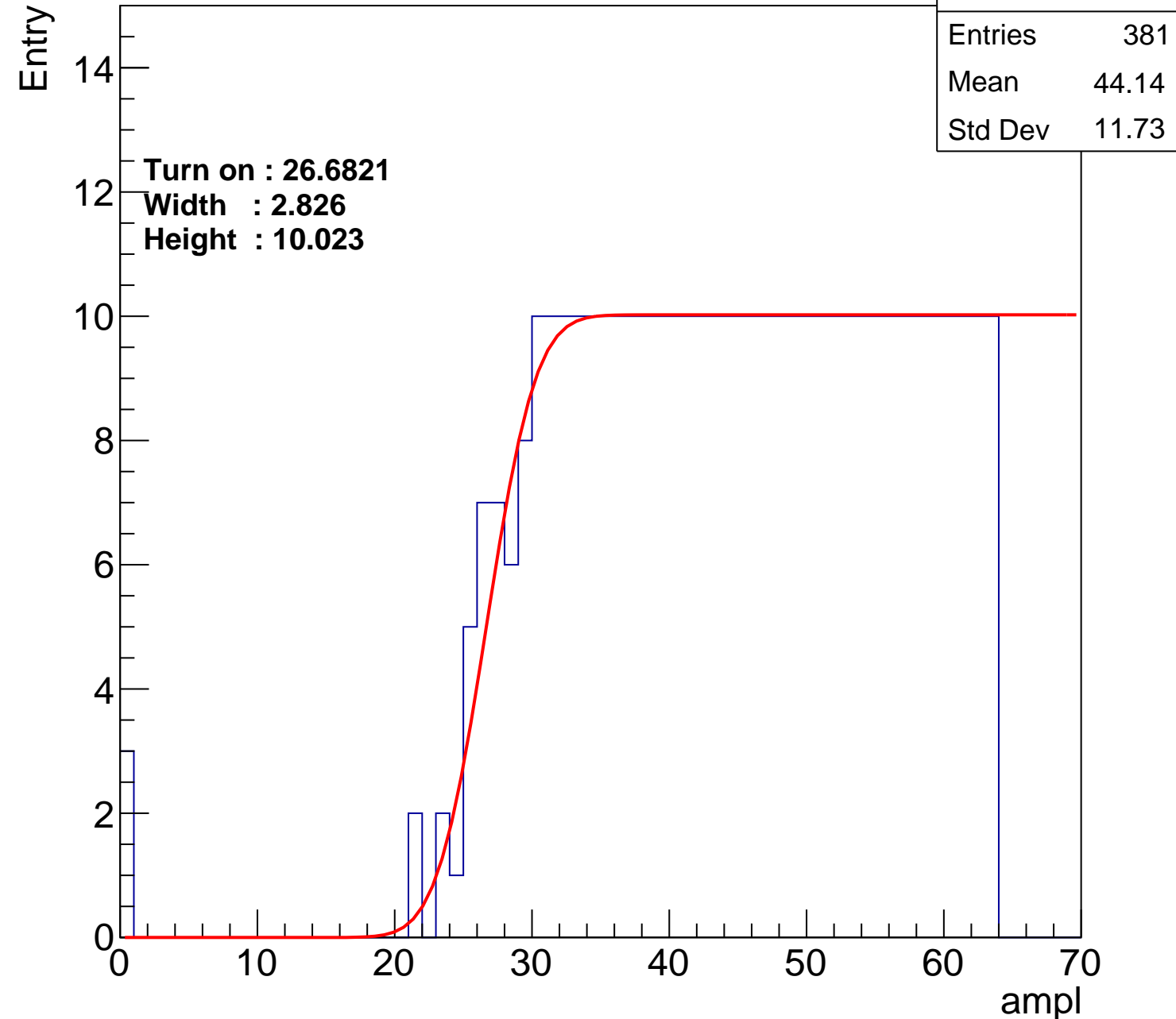
Width : 2.826

Height : 10.023

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch97

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	355
Mean	45.3
Std Dev	11.38

Turn on : 29.4585

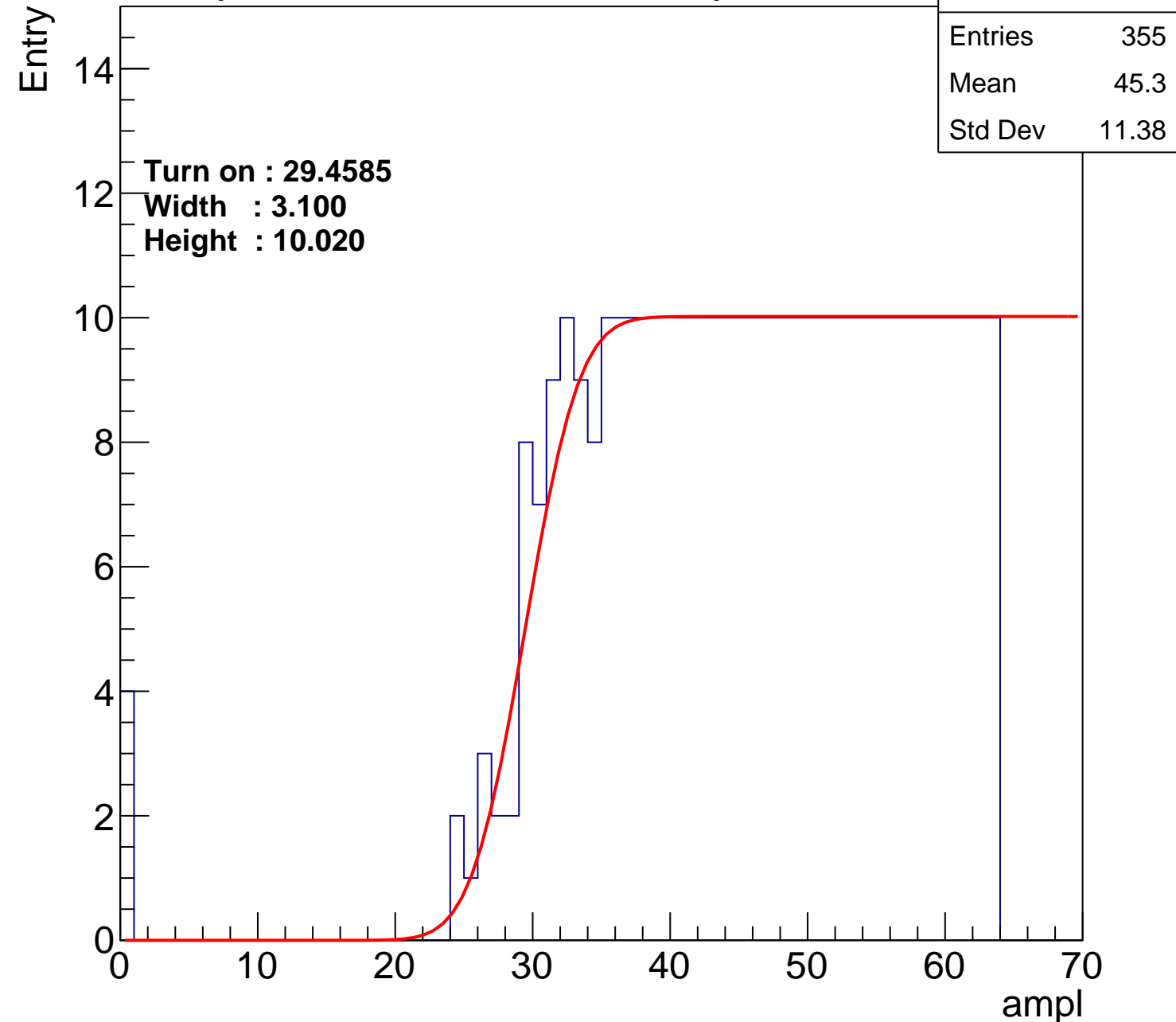
Width : 3.100

Height : 10.020

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch98

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	392
Mean	43.54
Std Dev	12.18

Turn on : 25.7459

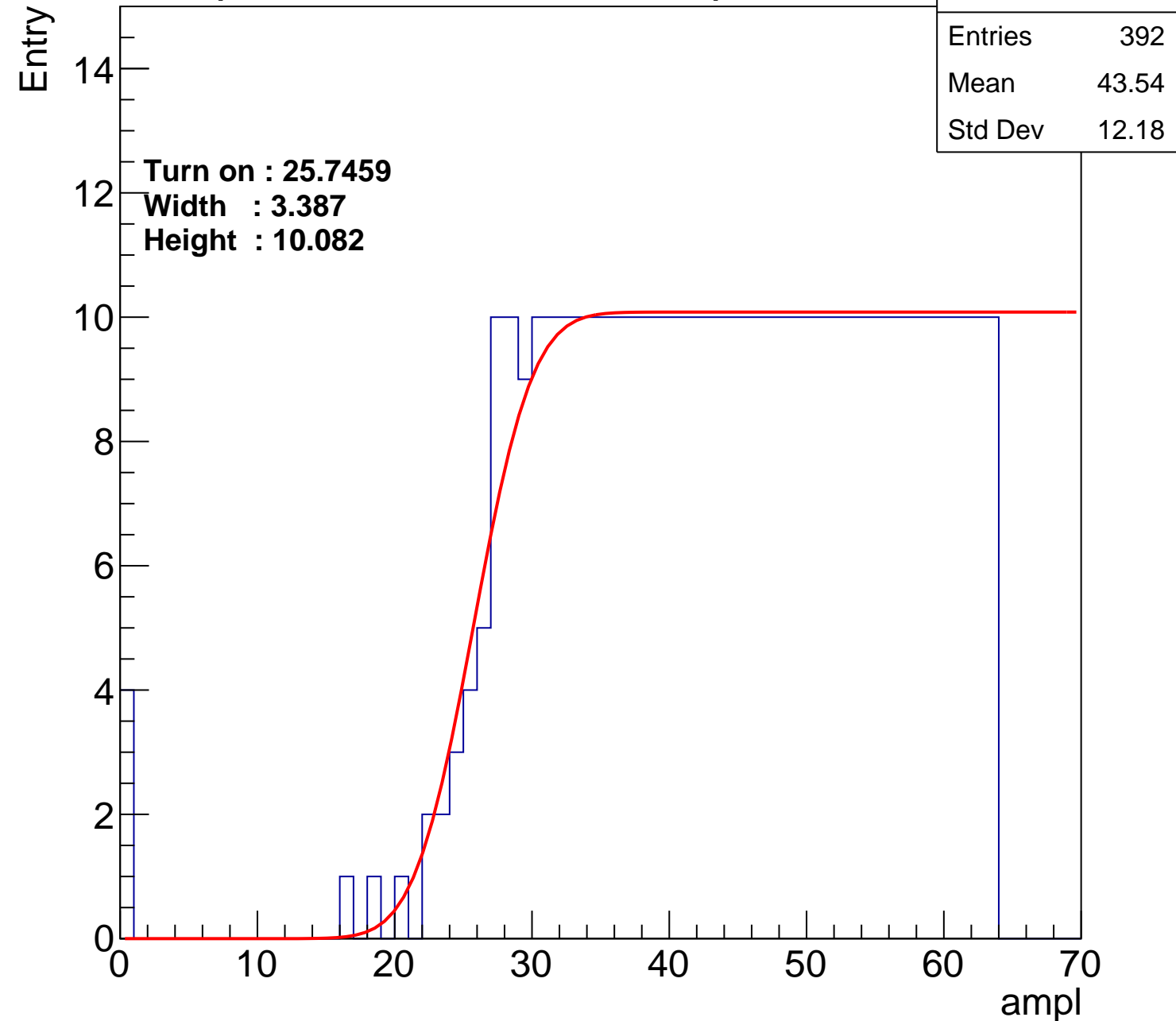
Width : 3.387

Height : 10.082

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch99

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	382
Mean	44.08
Std Dev	11.77

Turn on : 26.1186

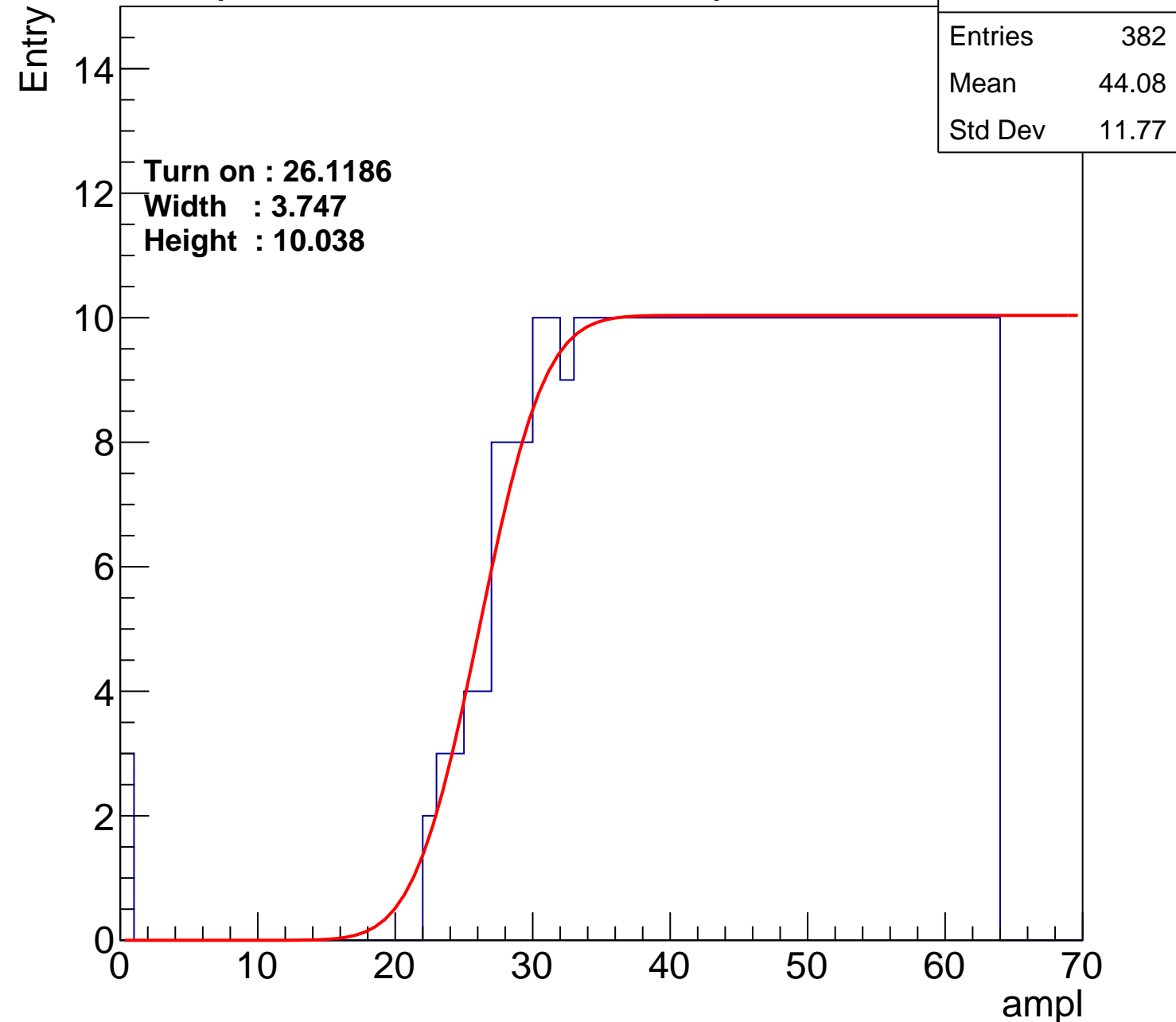
Width : 3.747

Height : 10.038

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch100

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	370
Mean	44.62
Std Dev	11.65

Turn on : 27.6940

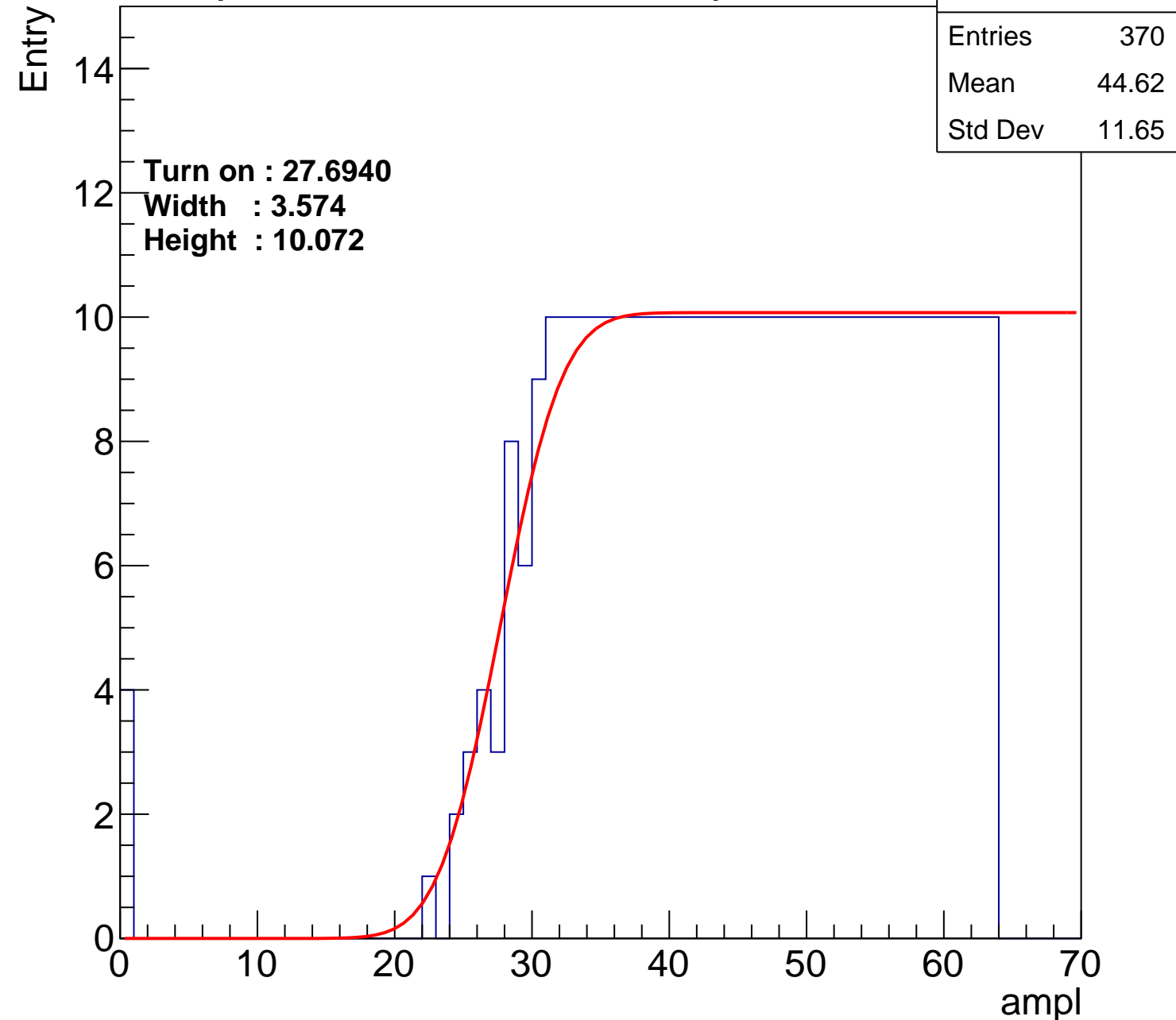
Width : 3.574

Height : 10.072

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch101

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	387
Mean	43.68
Std Dev	12.33

**Turn on : 26.0940**

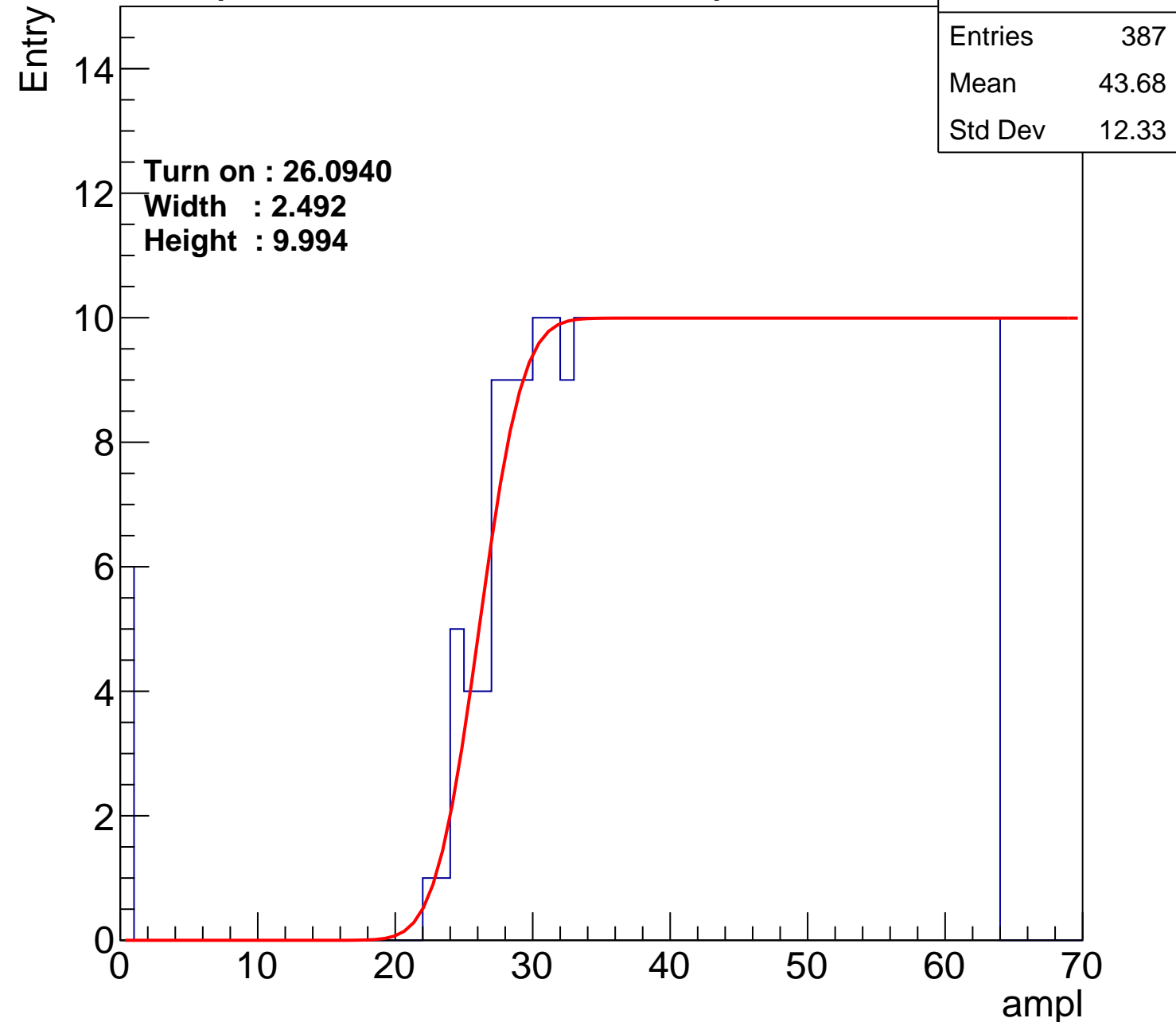
**Width : 2.492**

**Height : 9.994**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch102

calib\_packv5\_042523\_0143.root, FC#11, port A2

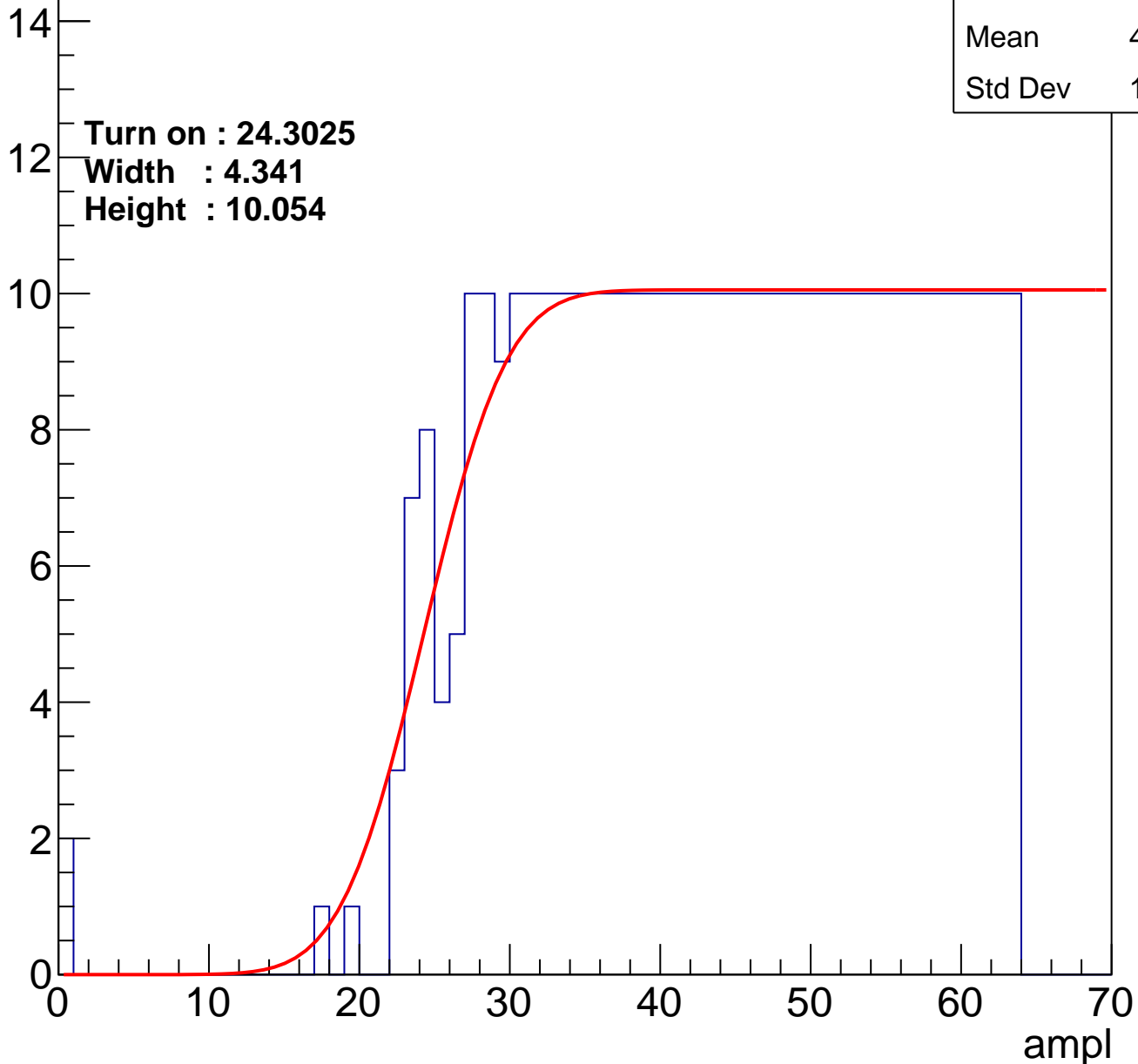
Entries	400
Mean	43.27
Std Dev	12.06

Turn on : 24.3025

Width : 4.341

Height : 10.054

Entry





# B1L102S, U2-ch103

calib\_packv5\_042523\_0143.root, FC#11, port A2

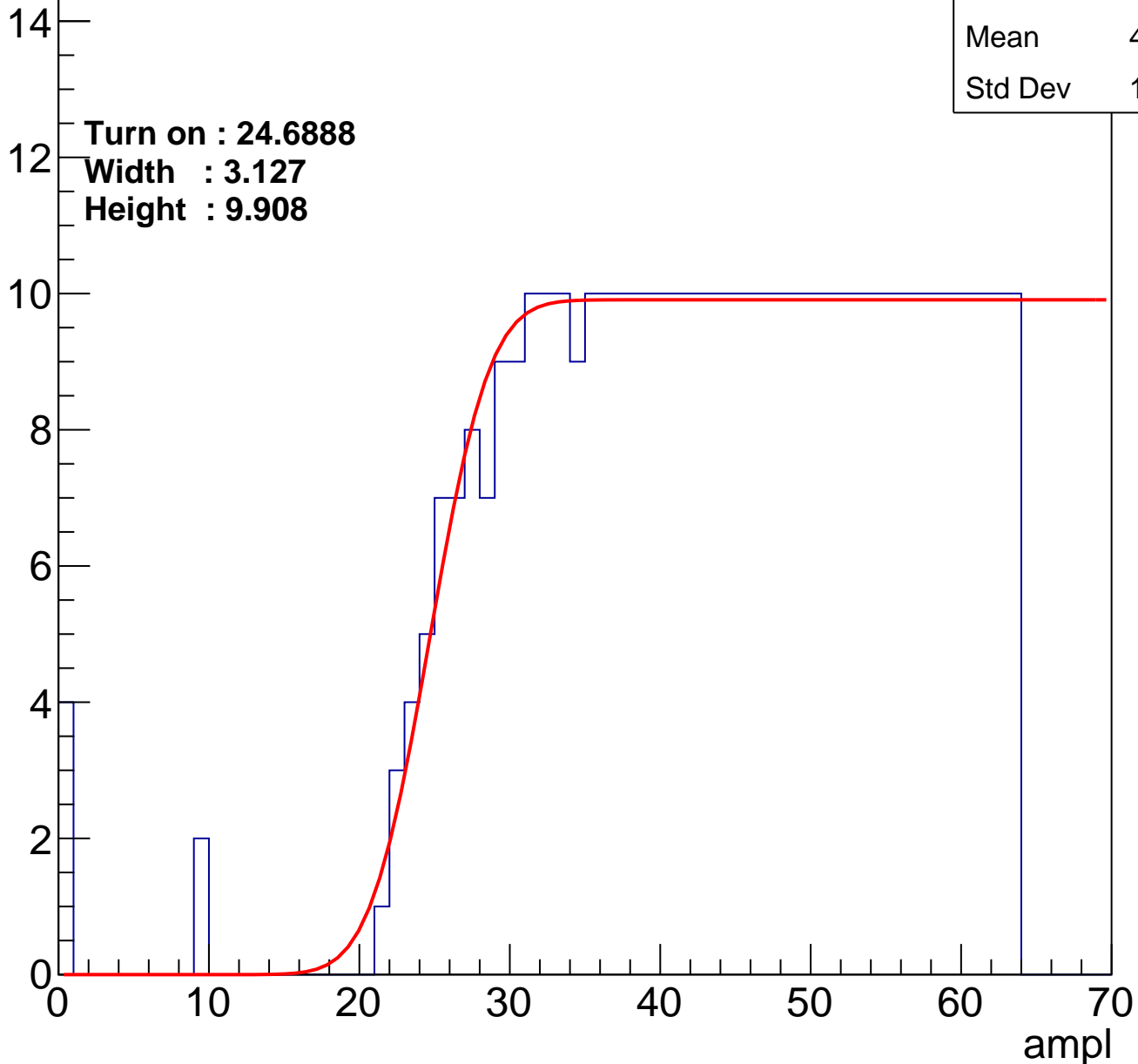
Entries	395
Mean	43.27
Std Dev	12.45

Turn on : 24.6888

Width : 3.127

Height : 9.908

Entry



# B1L102S, U2-ch104

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	393
Mean	43.42
Std Dev	12.35

Turn on : 25.4888

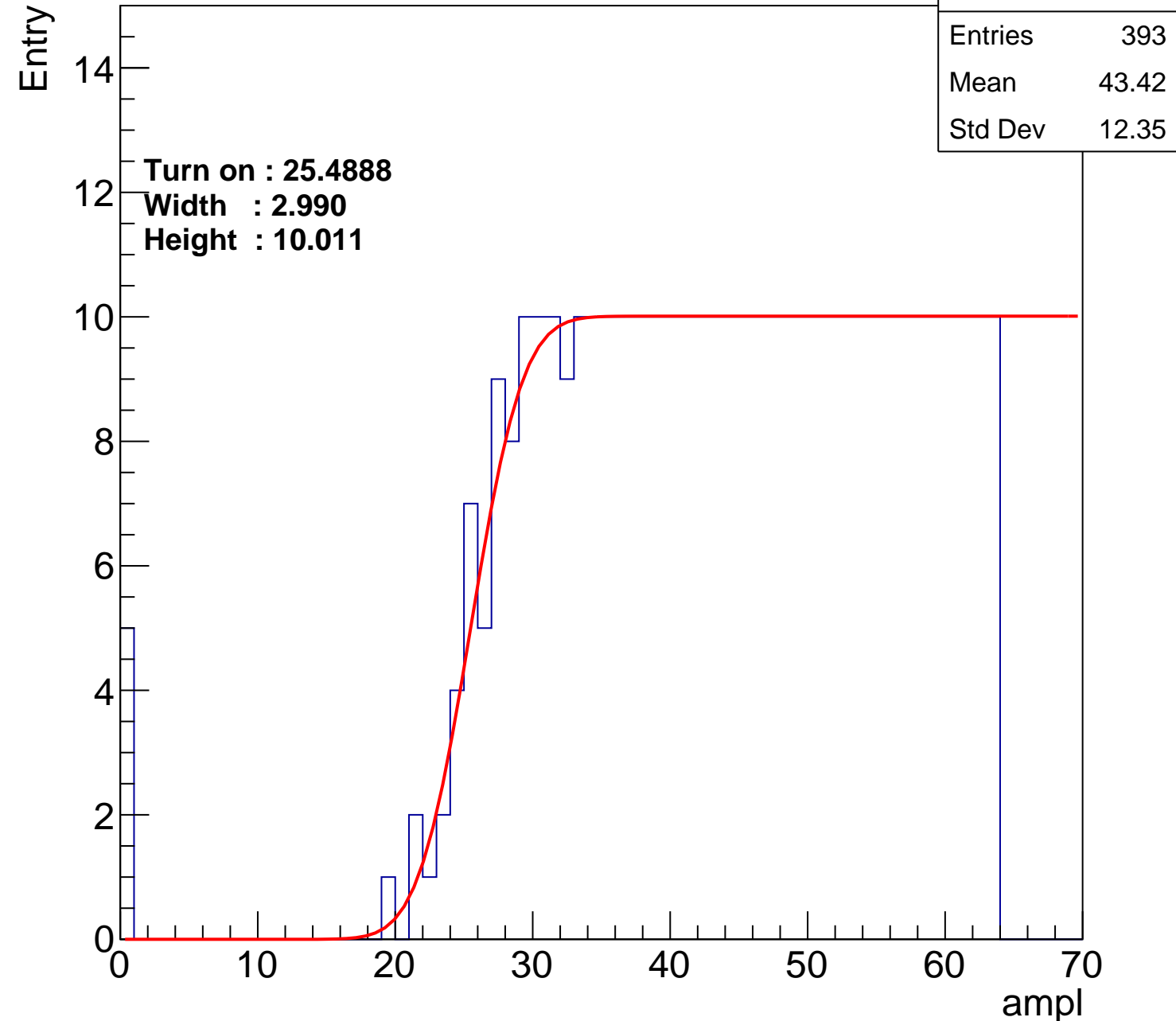
Width : 2.990

Height : 10.011

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch105

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	398
Mean	43.19
Std Dev	12.45

**Turn on : 24.7904**

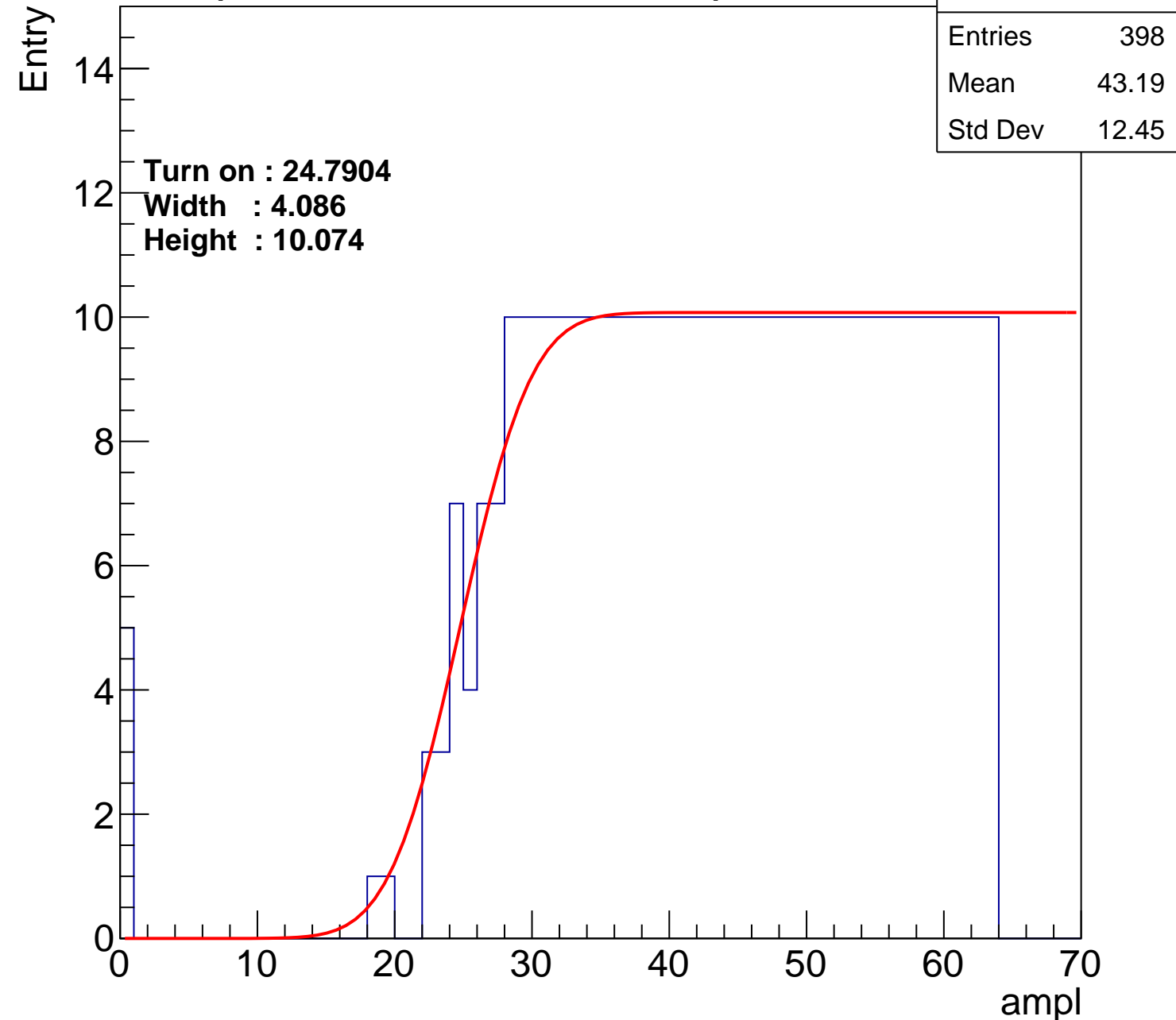
**Width : 4.086**

**Height : 10.074**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch106

calib\_packv5\_042523\_0143.root, FC#11, port A2

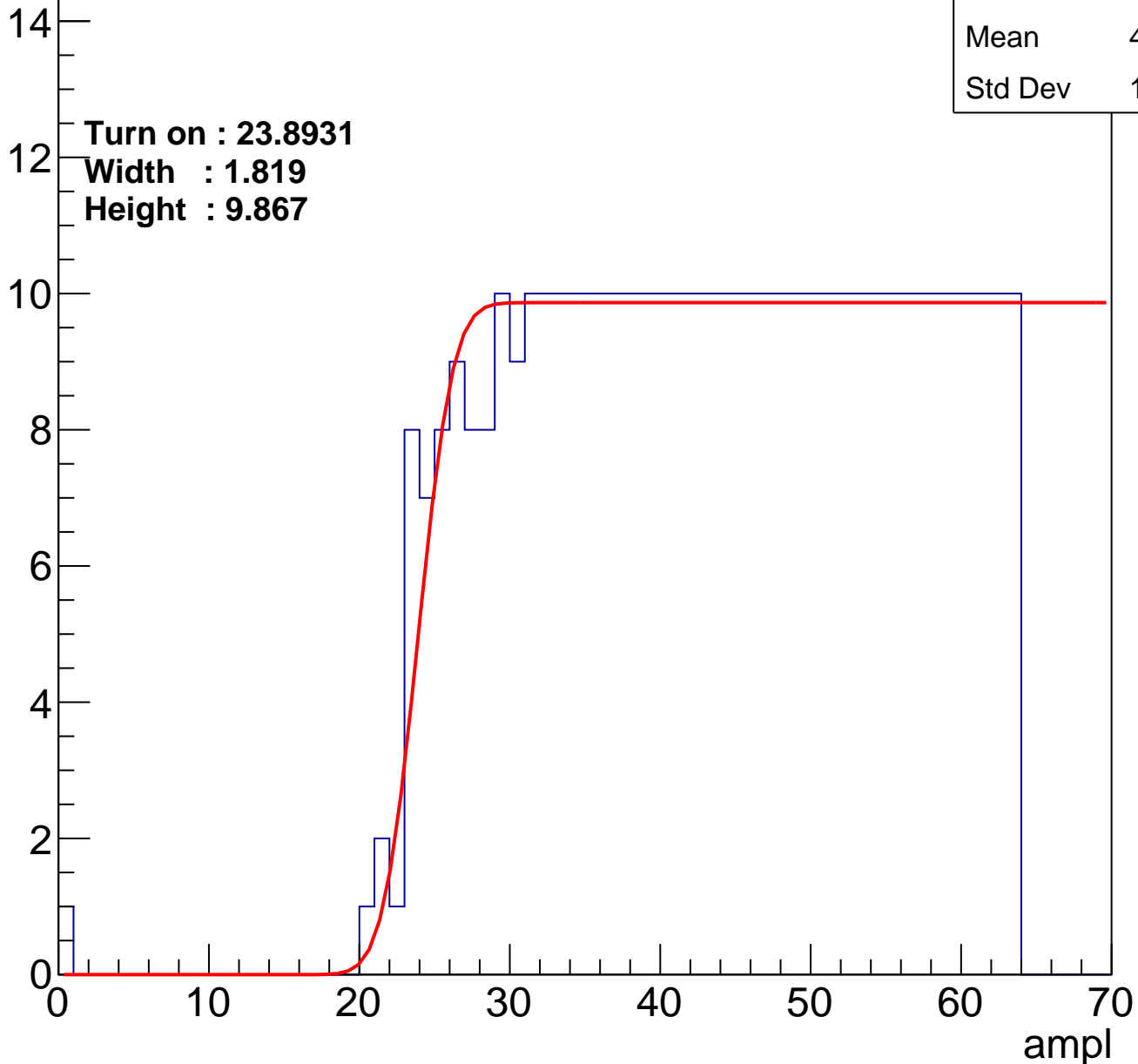
Entries	402
Mean	43.23
Std Dev	11.93

Turn on : 23.8931

Width : 1.819

Height : 9.867

Entry



# B1L102S, U2-ch107

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	379
Mean	44.16
Std Dev	11.81

Turn on : 26.3476

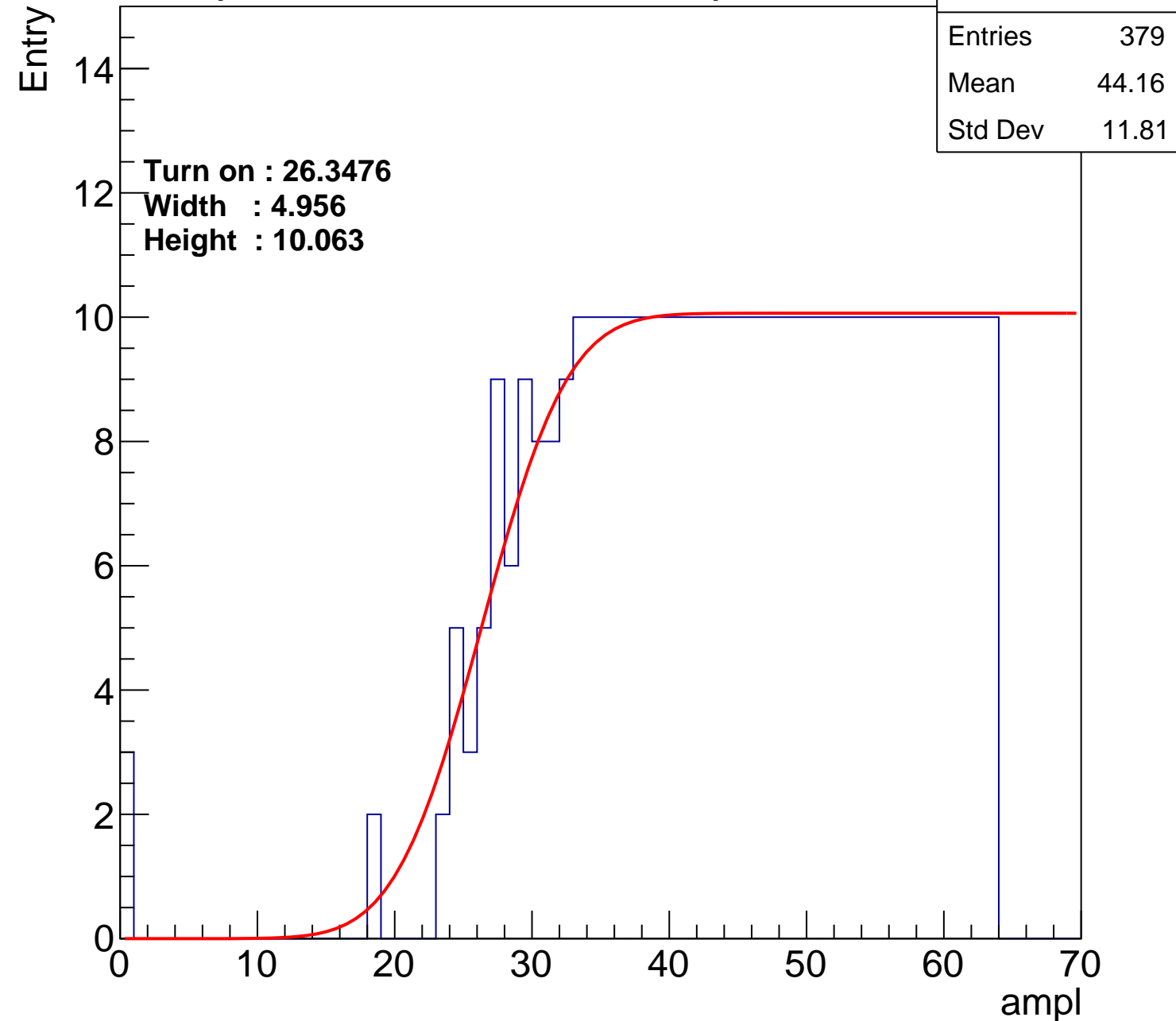
Width : 4.956

Height : 10.063

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch108

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	380
Mean	44.21
Std Dev	11.6

**Turn on : 26.3657**

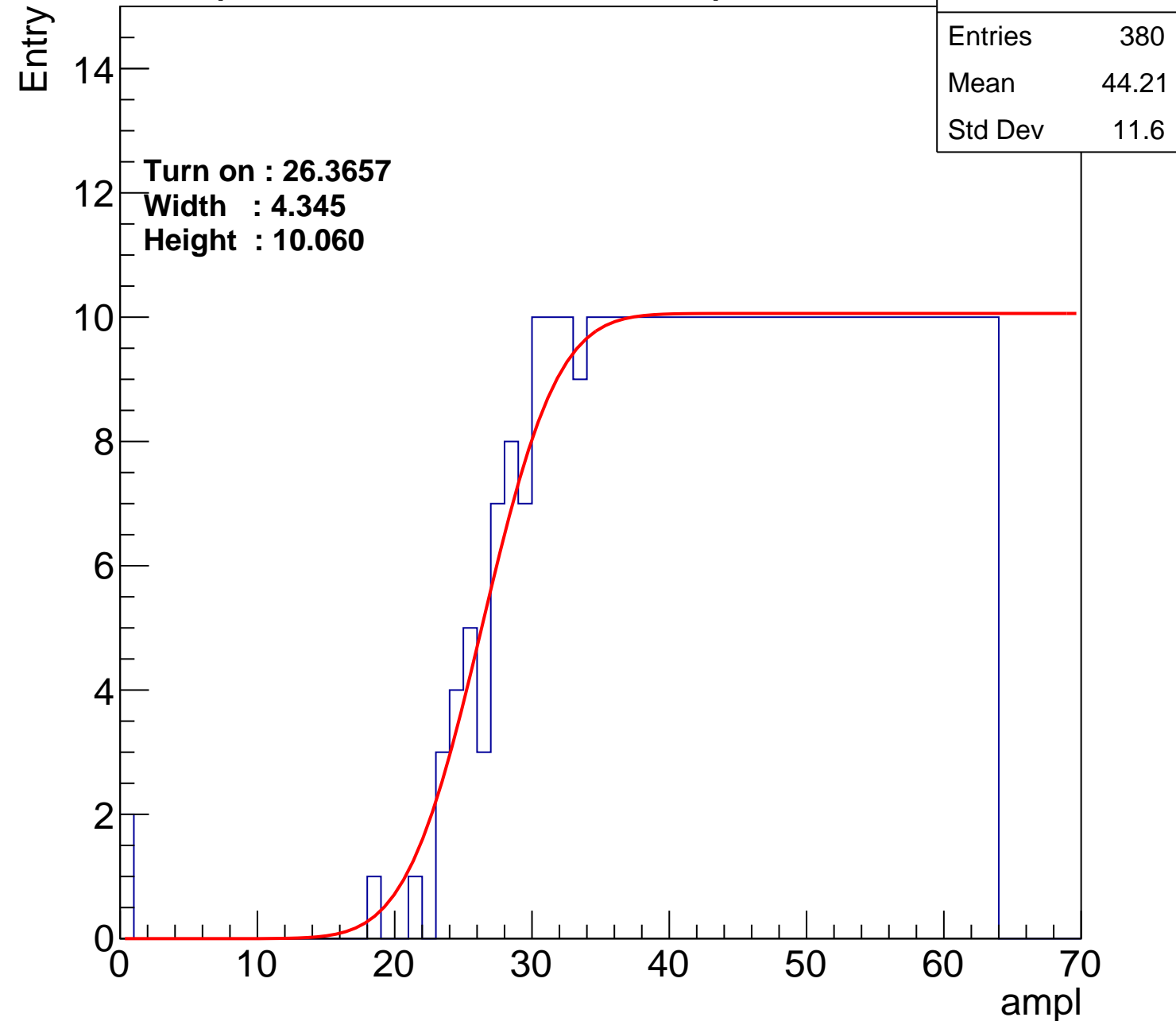
**Width : 4.345**

**Height : 10.060**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch109

calib\_packv5\_042523\_0143.root, FC#11, port A2

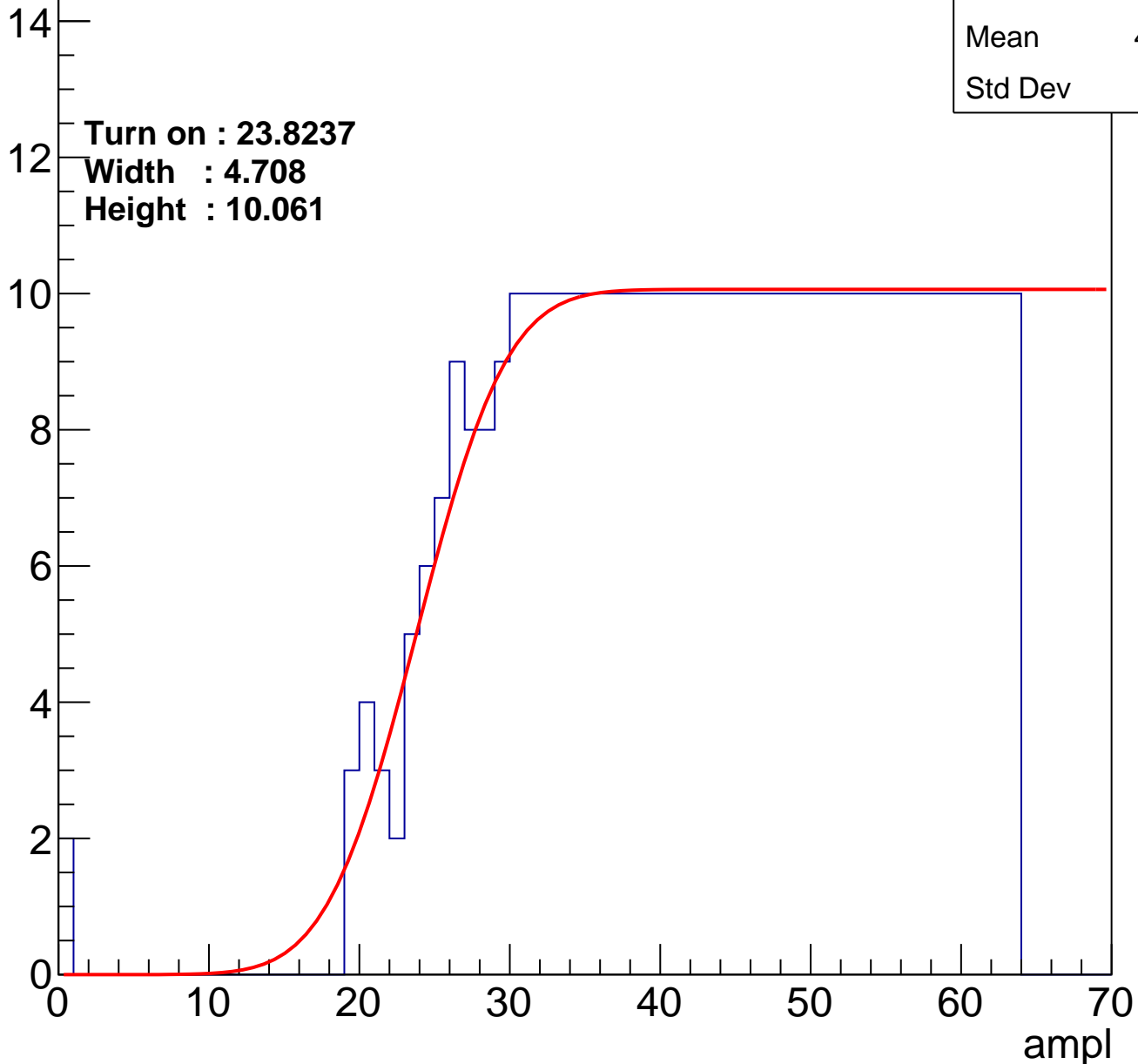
Entries	406
Mean	42.91
Std Dev	12.3

Turn on : 23.8237

Width : 4.708

Height : 10.061

Entry



# B1L102S, U2-ch110

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	398
Mean	43.28
Std Dev	12.25

Turn on : 24.9140

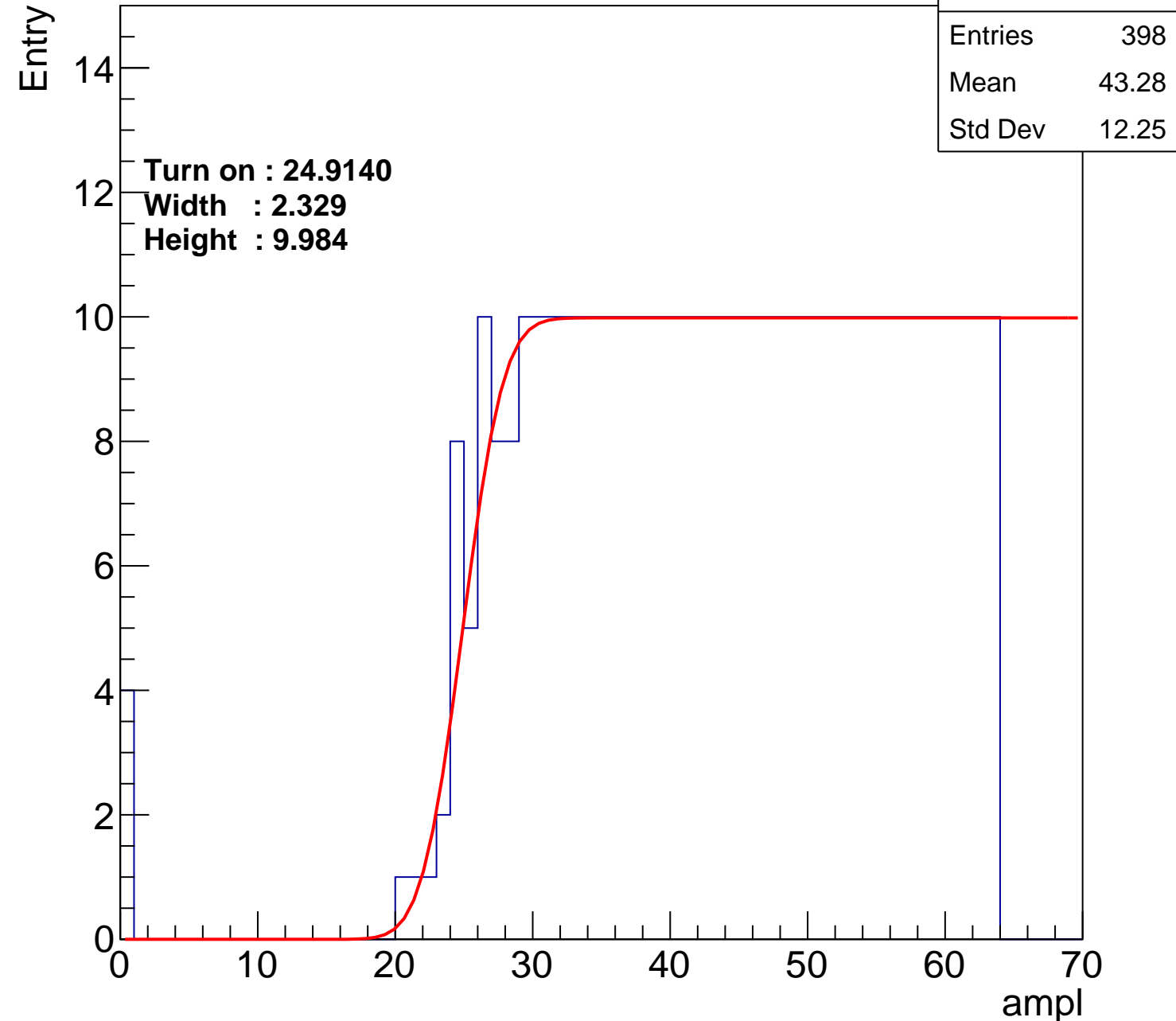
Width : 2.329

Height : 9.984

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L102S, U2-ch111

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	379
Mean	44.13
Std Dev	11.93

Turn on : 28.1672

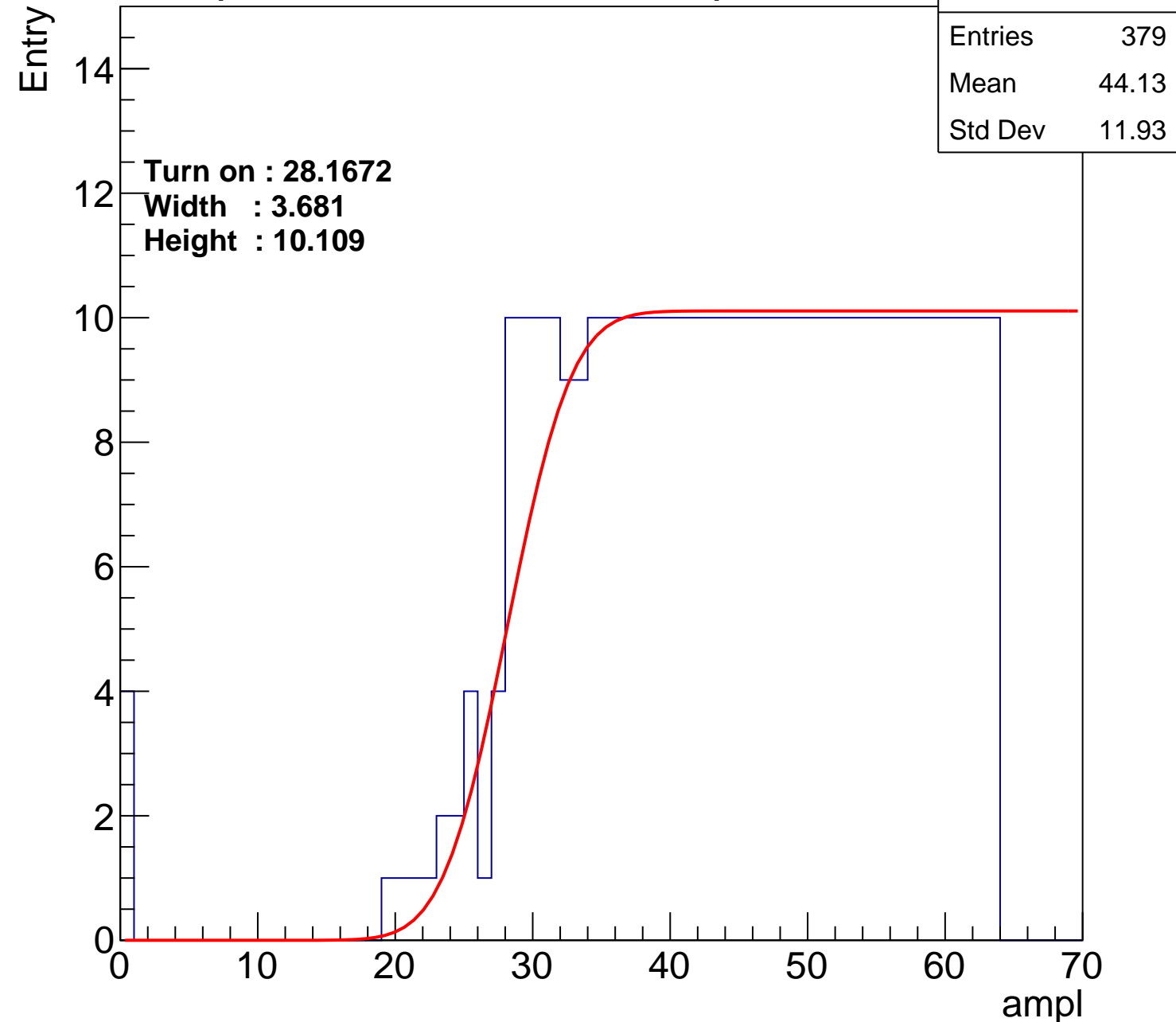
Width : 3.681

Height : 10.109

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch112

**calib\_packv5\_042523\_0143.root, FC#11, port A2**

Entries	386
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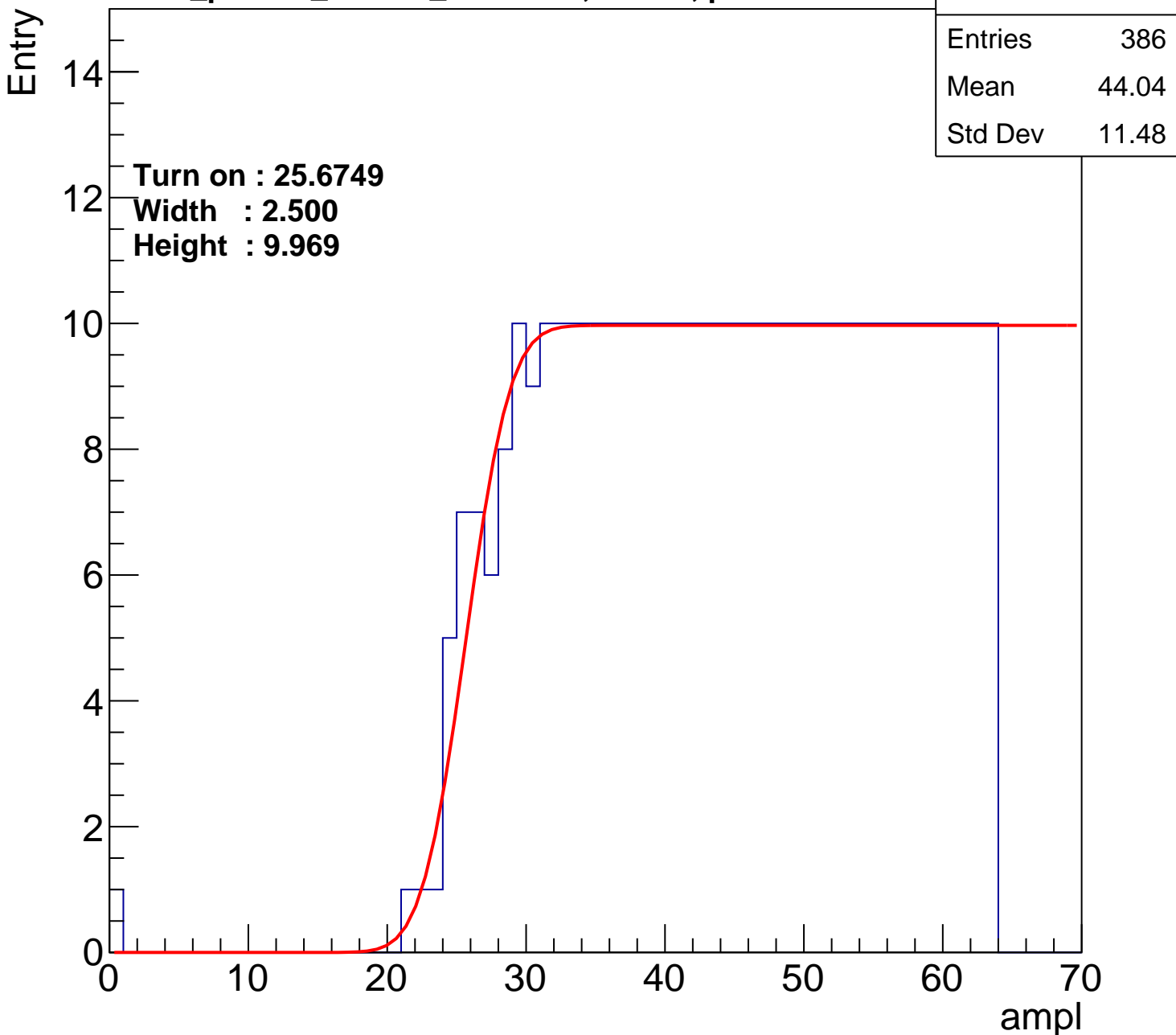
Mean	44.04
------	-------

Std Dev	11.48
---------	-------

**Turn on : 25.6749**

**Width : 2.500**

**Height : 9.969**



# B1L102S, U2-ch113

calib\_packv5\_042523\_0143.root, FC#11, port A2

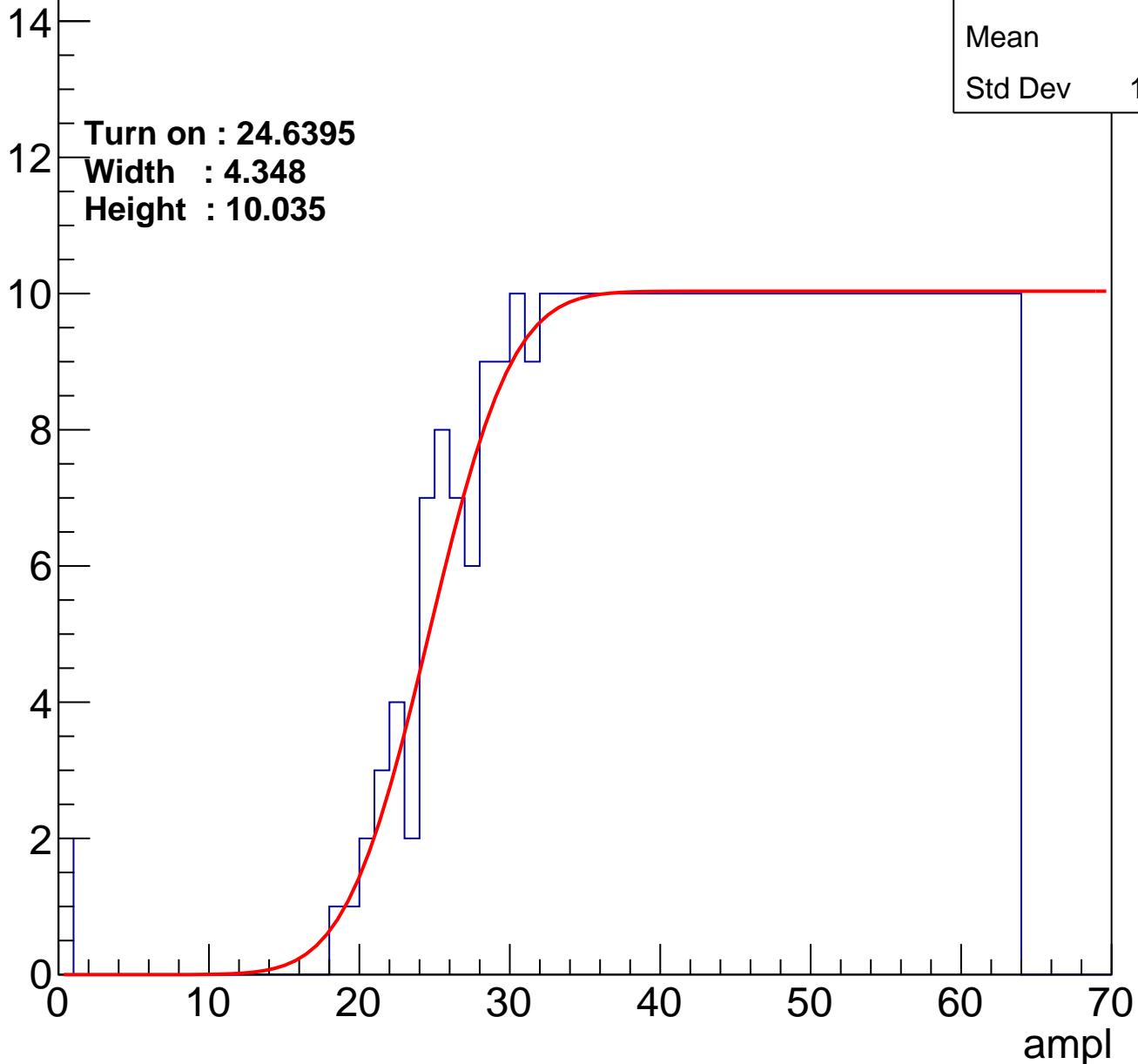
Entries	400
Mean	43.2
Std Dev	12.16

Turn on : 24.6395

Width : 4.348

Height : 10.035

Entry



# B1L102S, U2-ch114

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	390
Mean	43.74
Std Dev	11.9

Turn on : 25.6418

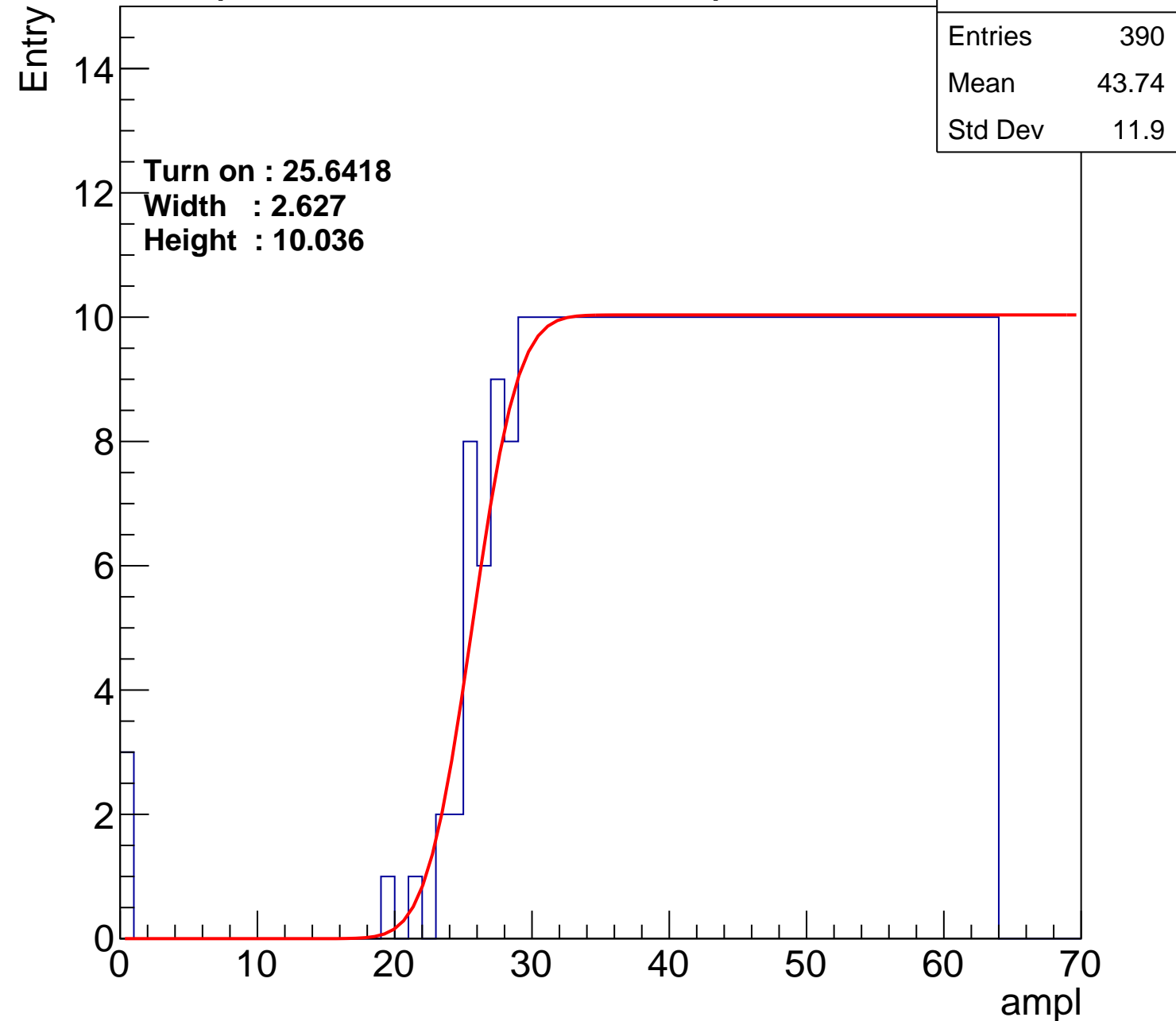
Width : 2.627

Height : 10.036

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch115

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	393
Mean	43.65
Std Dev	11.73

Turn on : 25.2954

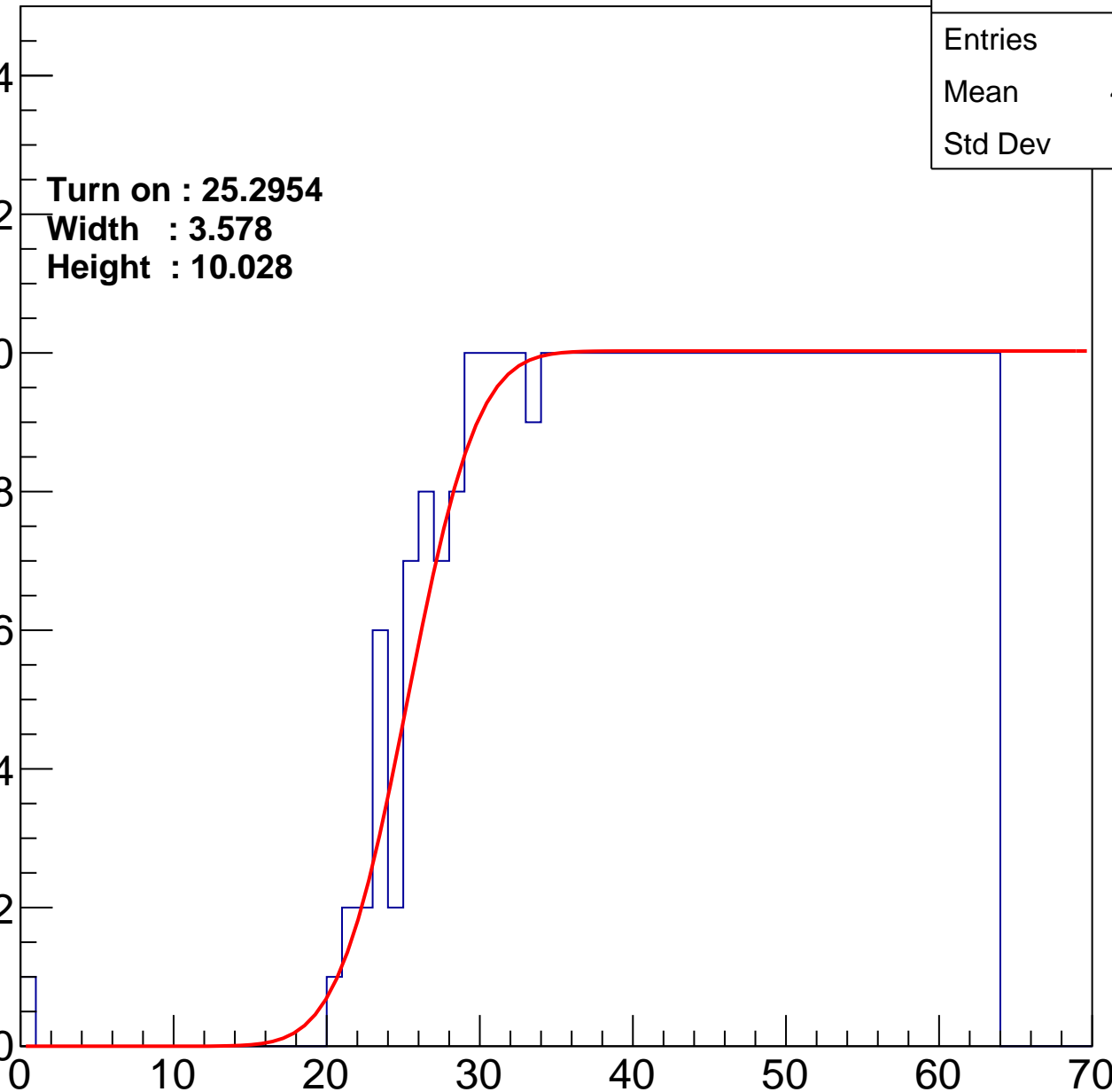
Width : 3.578

Height : 10.028

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch116

calib\_packv5\_042523\_0143.root, FC#11, port A2

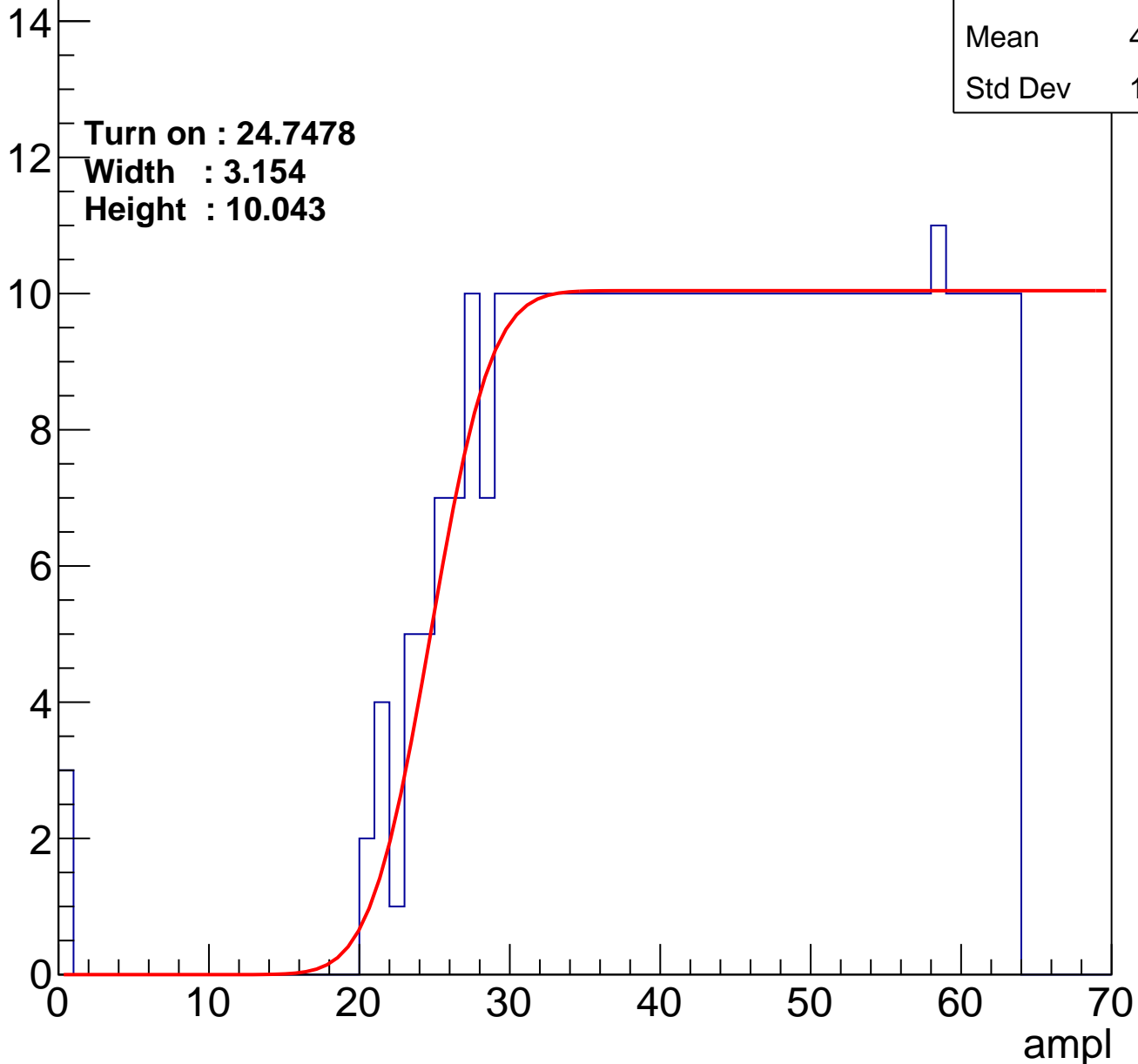
Entries	402
Mean	43.19
Std Dev	12.24

Turn on : 24.7478

Width : 3.154

Height : 10.043

Entry



# B1L102S, U2-ch117

calib\_packv5\_042523\_0143.root, FC#11, port A2

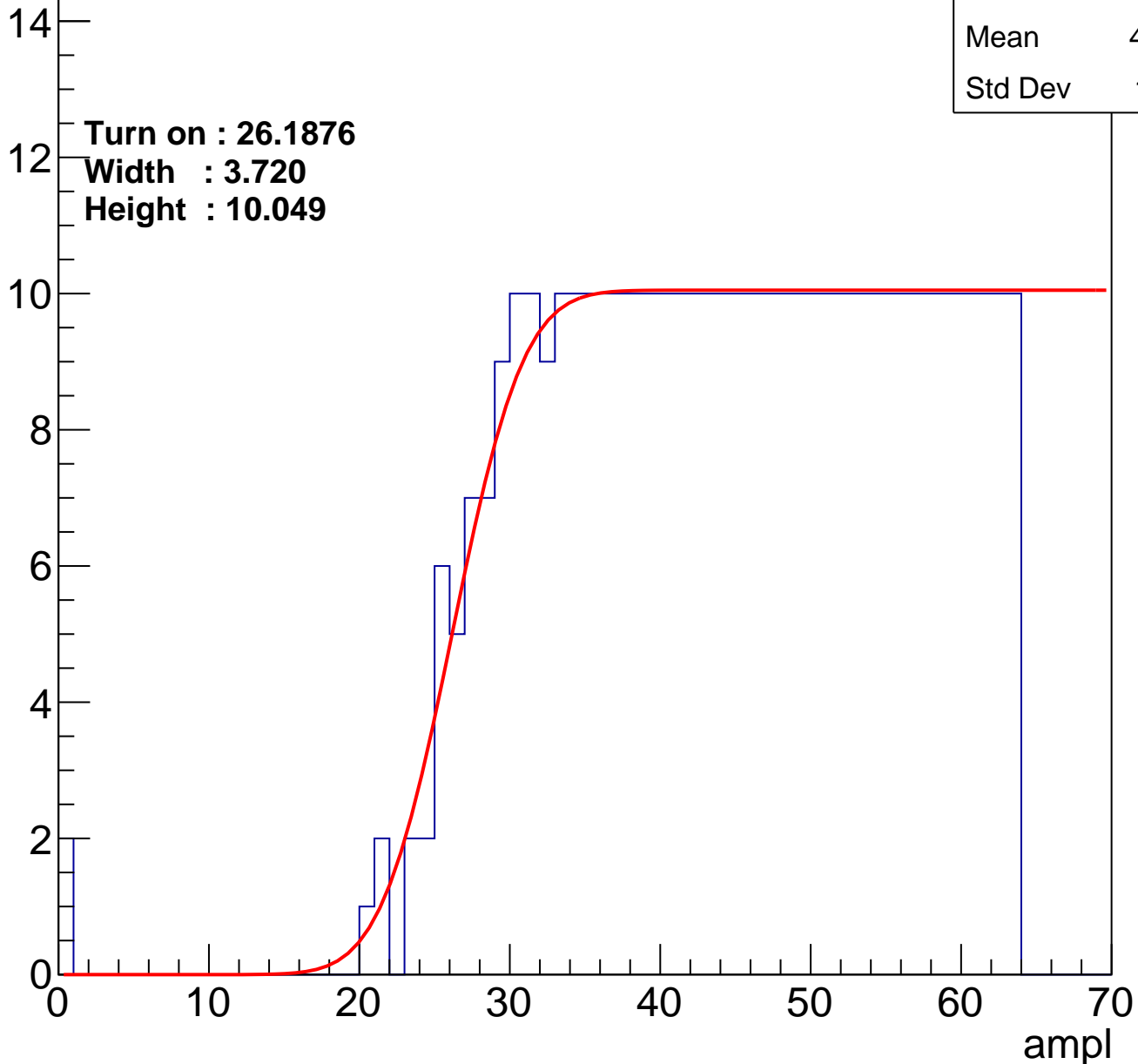
Entries	382
Mean	44.14
Std Dev	11.61

Turn on : 26.1876

Width : 3.720

Height : 10.049

Entry



# B1L102S, U2-ch118

calib\_packv5\_042523\_0143.root, FC#11, port A2

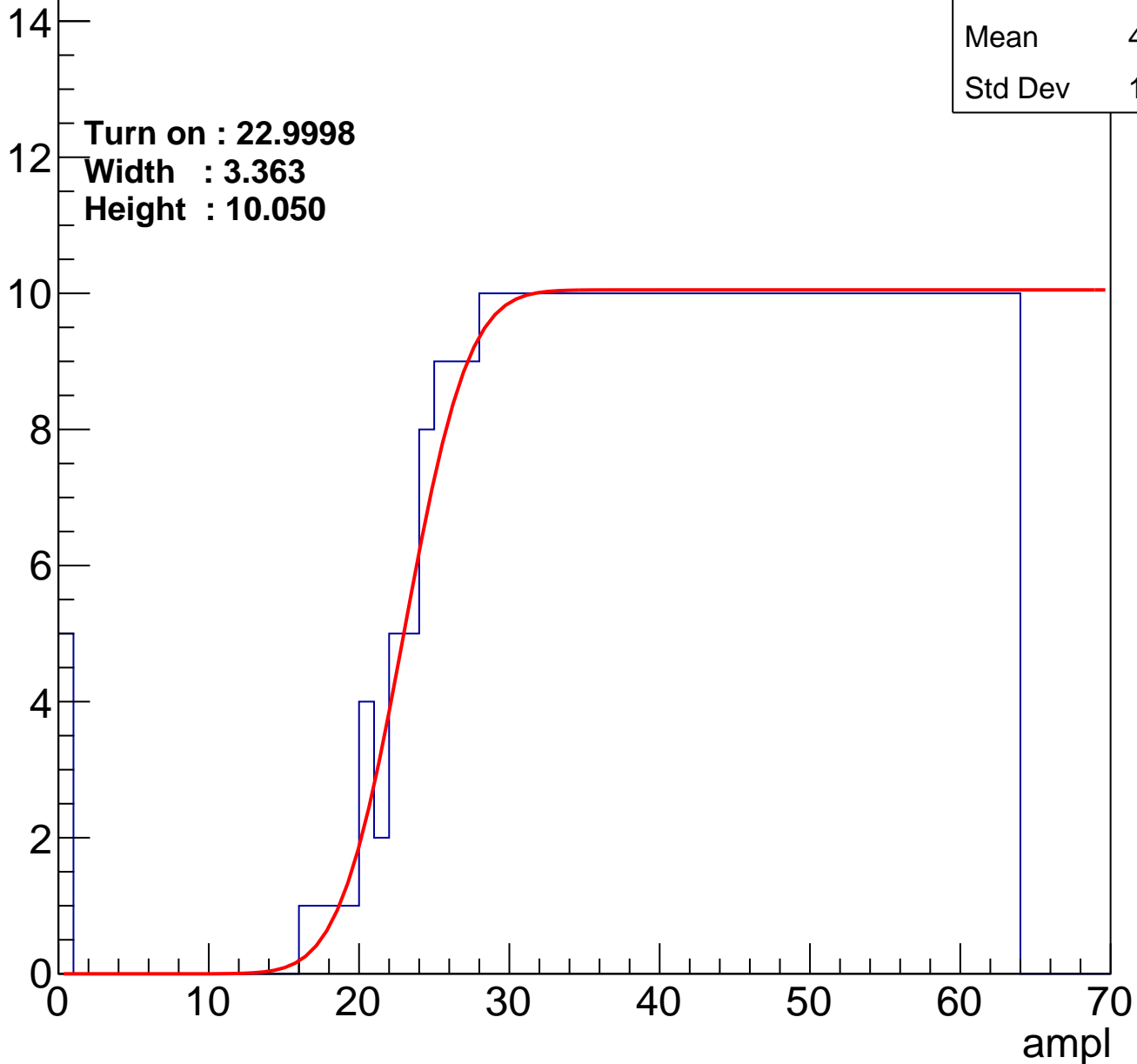
Entries	420
Mean	42.12
Std Dev	12.97

**Turn on : 22.9998**

**Width : 3.363**

**Height : 10.050**

Entry





# B1L102S, U2-ch119

calib\_packv5\_042523\_0143.root, FC#11, port A2

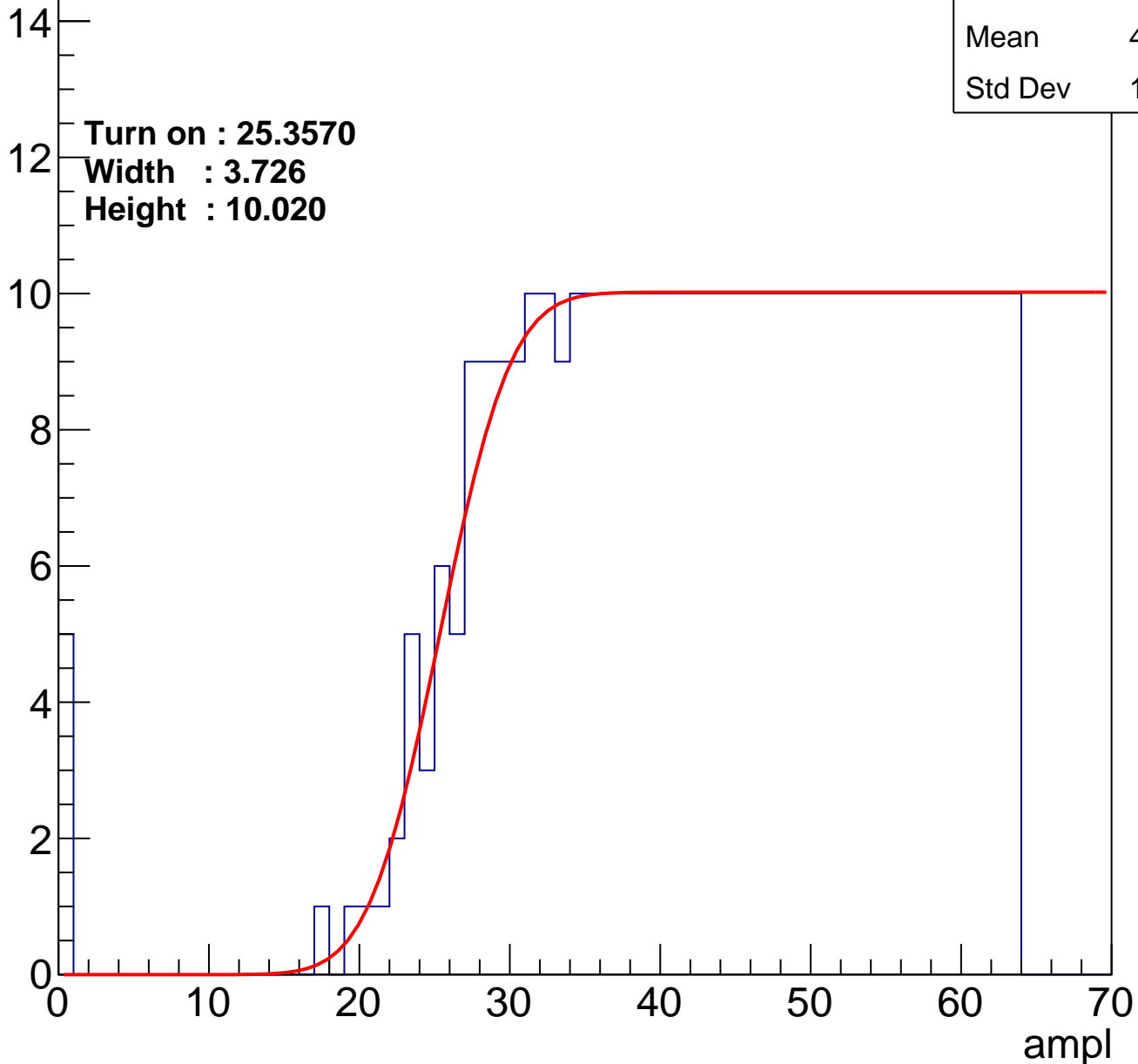
Entries	395
Mean	43.27
Std Dev	12.48

Turn on : 25.3570

Width : 3.726

Height : 10.020

Entry



# B1L102S, U2-ch120

calib\_packv5\_042523\_0143.root, FC#11, port A2

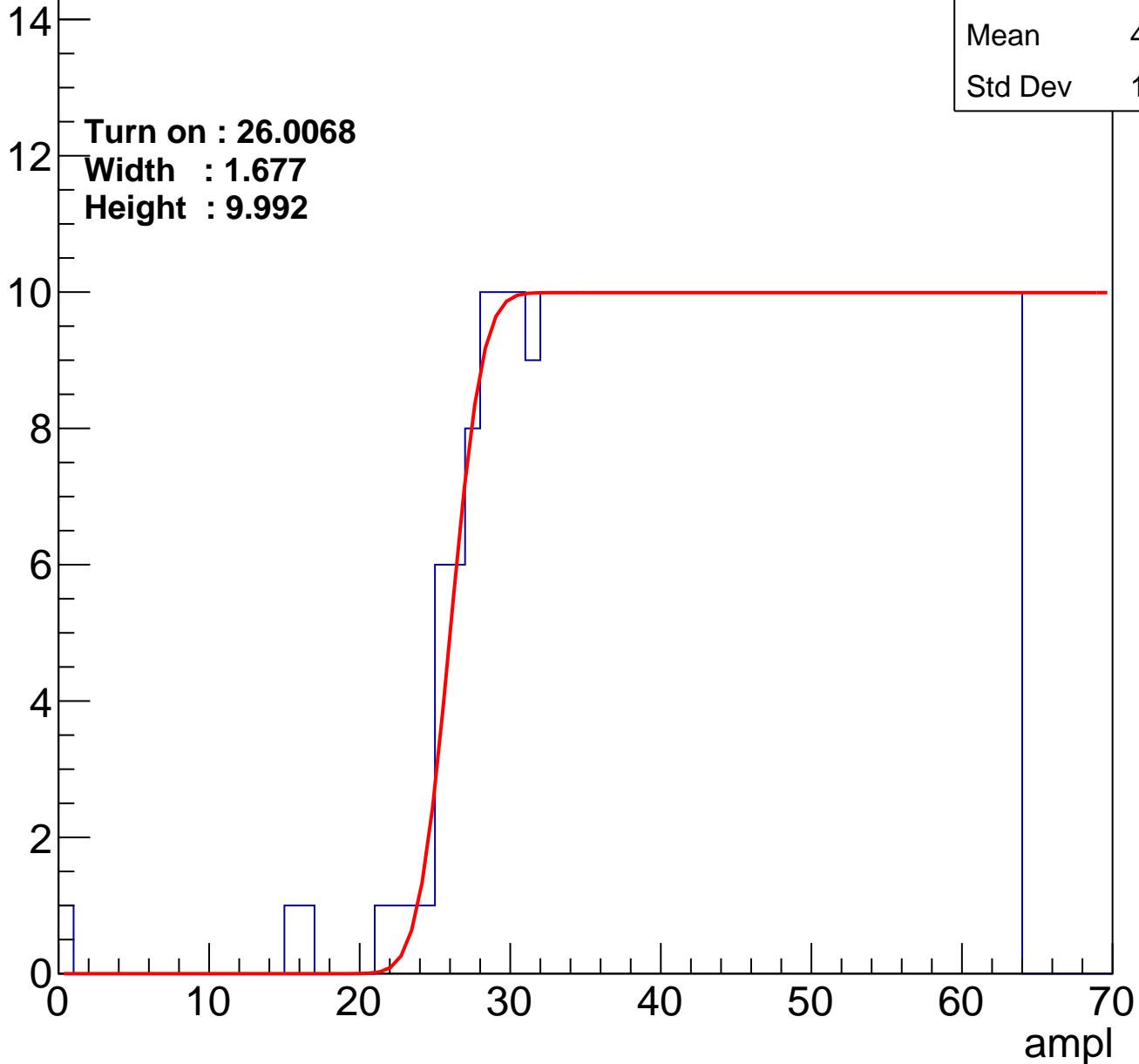
Entries	386
Mean	44.02
Std Dev	11.53

Turn on : 26.0068

Width : 1.677

Height : 9.992

Entry



# B1L102S, U2-ch121

calib\_packv5\_042523\_0143.root, FC#11, port A2

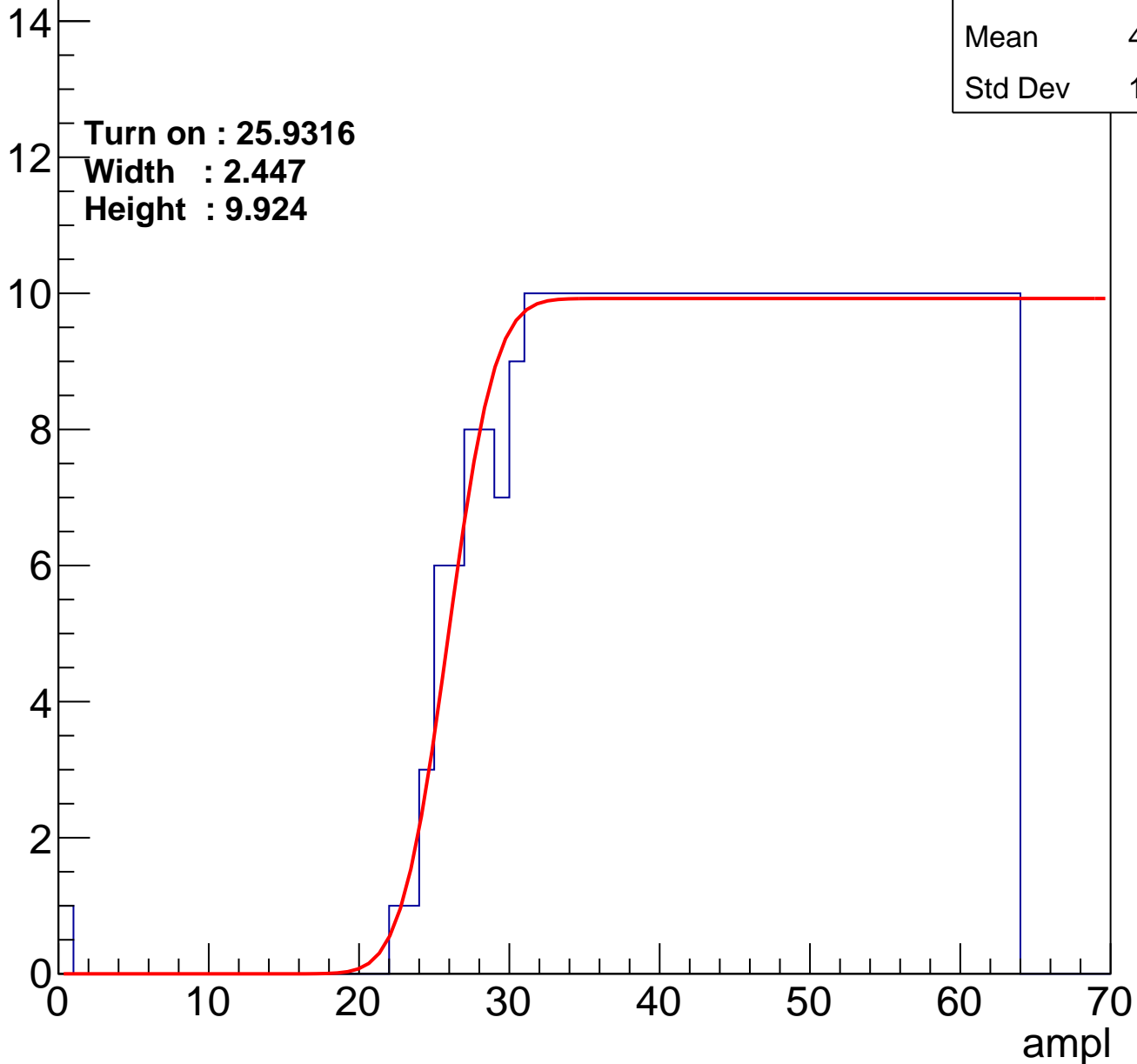
Entries	380
Mean	44.33
Std Dev	11.32

Turn on : 25.9316

Width : 2.447

Height : 9.924

Entry



# B1L102S, U2-ch122

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	391
Mean	43.63
Std Dev	12.01

Turn on : 25.8354

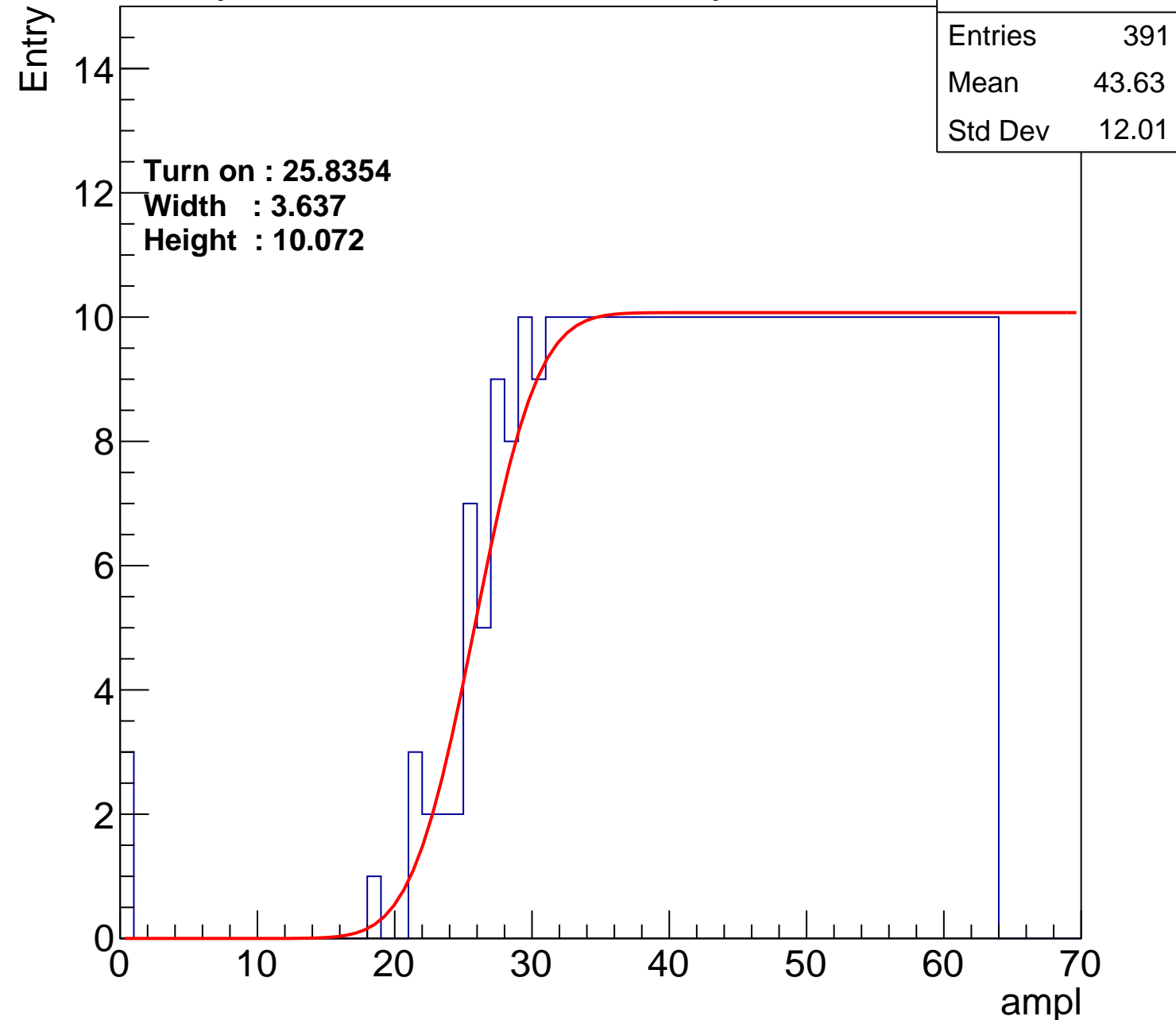
Width : 3.637

Height : 10.072

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch123

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	399
Mean	43.07
Std Dev	12.64

Turn on : 25.0528

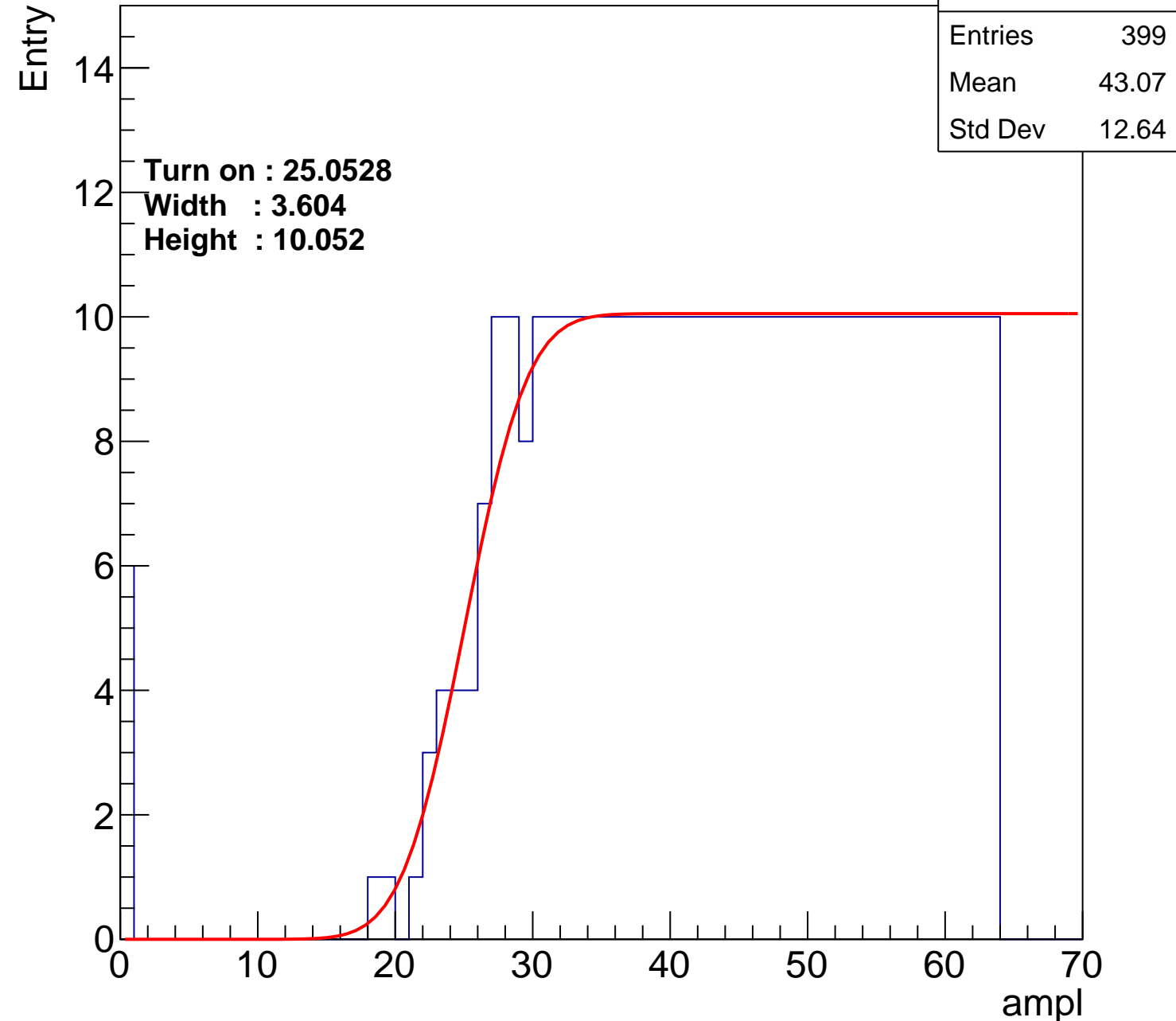
Width : 3.604

Height : 10.052

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch124

calib\_packv5\_042523\_0143.root, FC#11, port A2

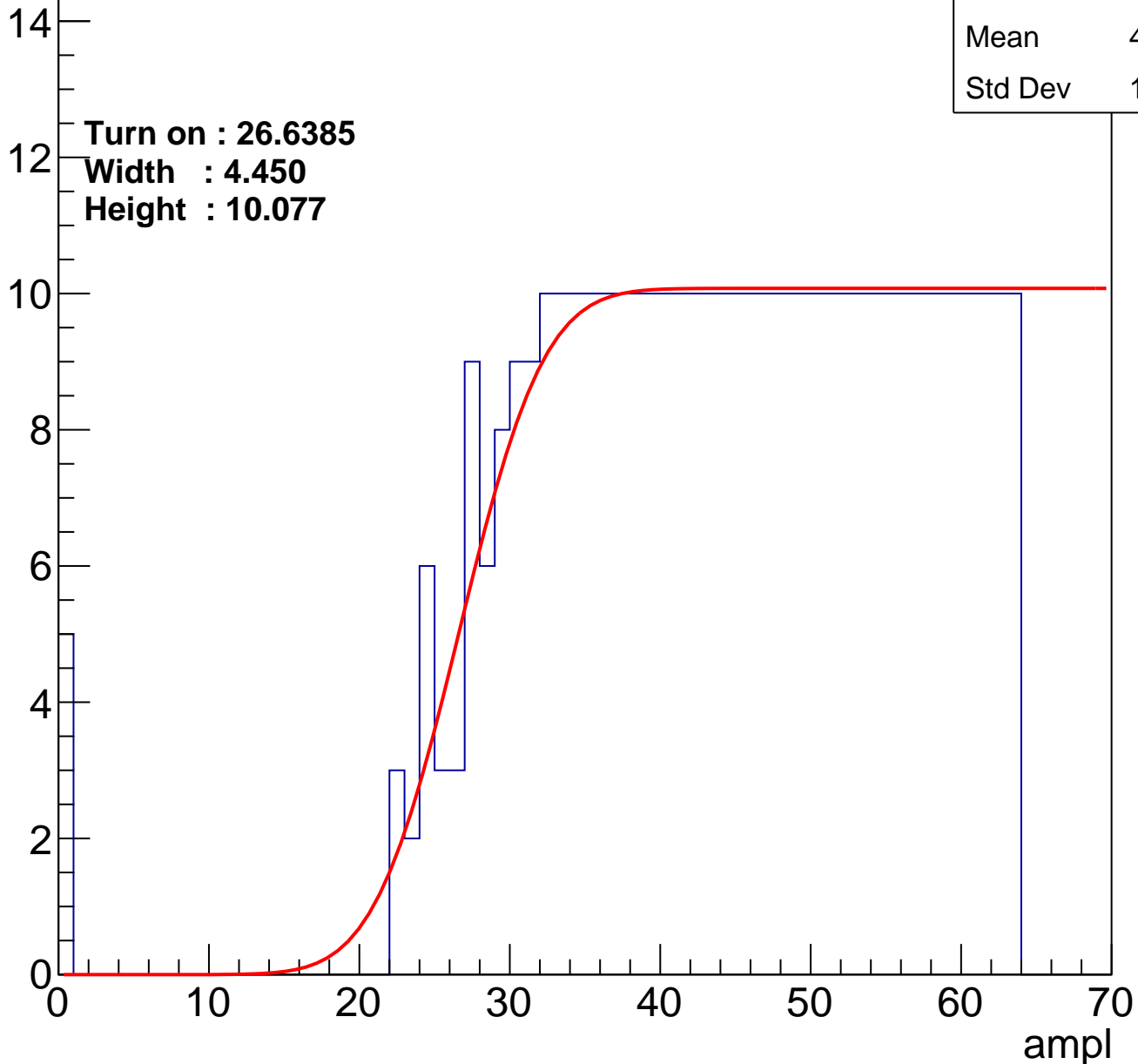
Entries	383
Mean	43.87
Std Dev	12.19

Turn on : 26.6385

Width : 4.450

Height : 10.077

Entry



# B1L102S, U2-ch125

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	388
Mean	43.89
Std Dev	11.61

Turn on : 25.3402

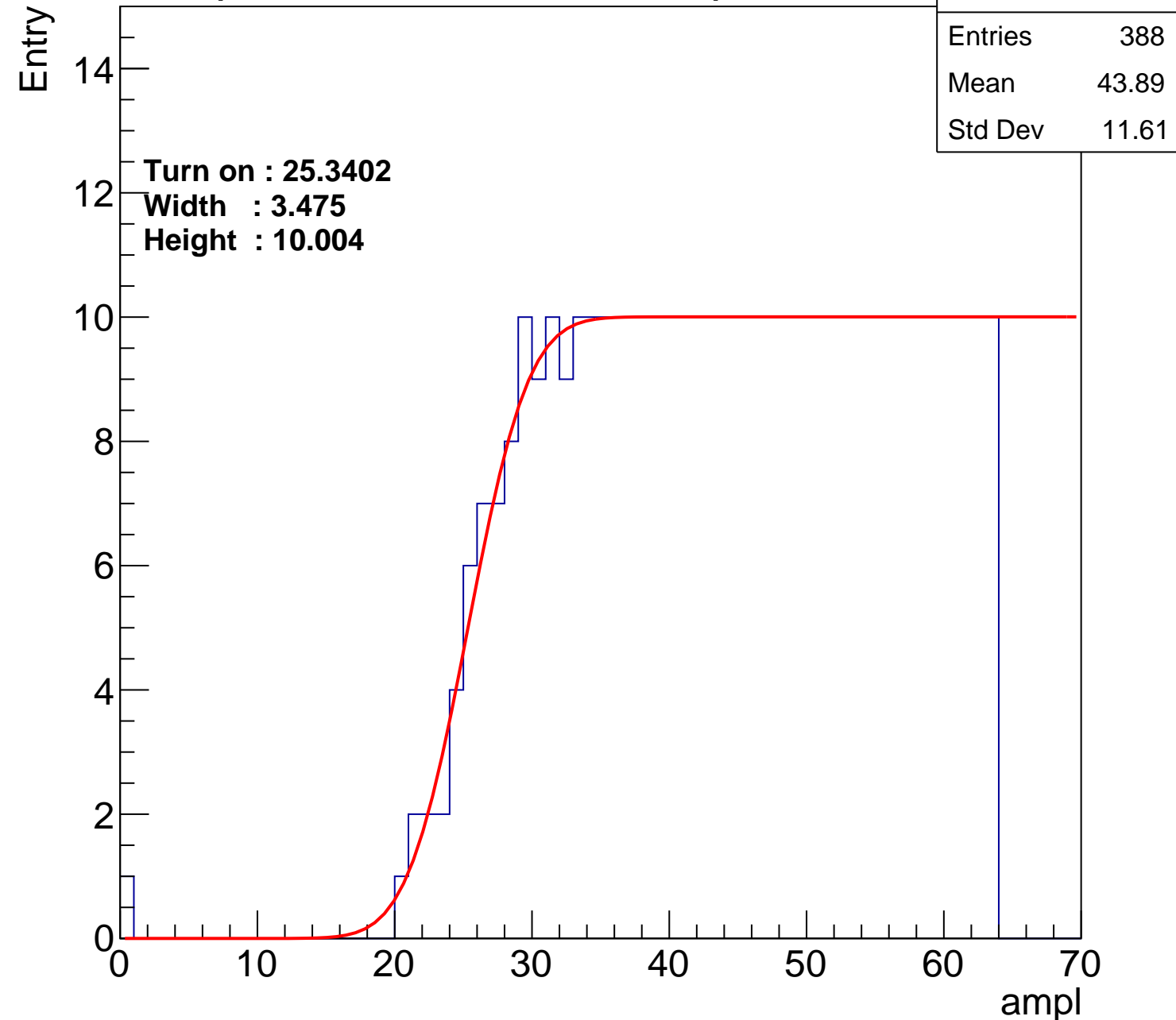
Width : 3.475

Height : 10.004

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch126

calib\_packv5\_042523\_0143.root, FC#11, port A2

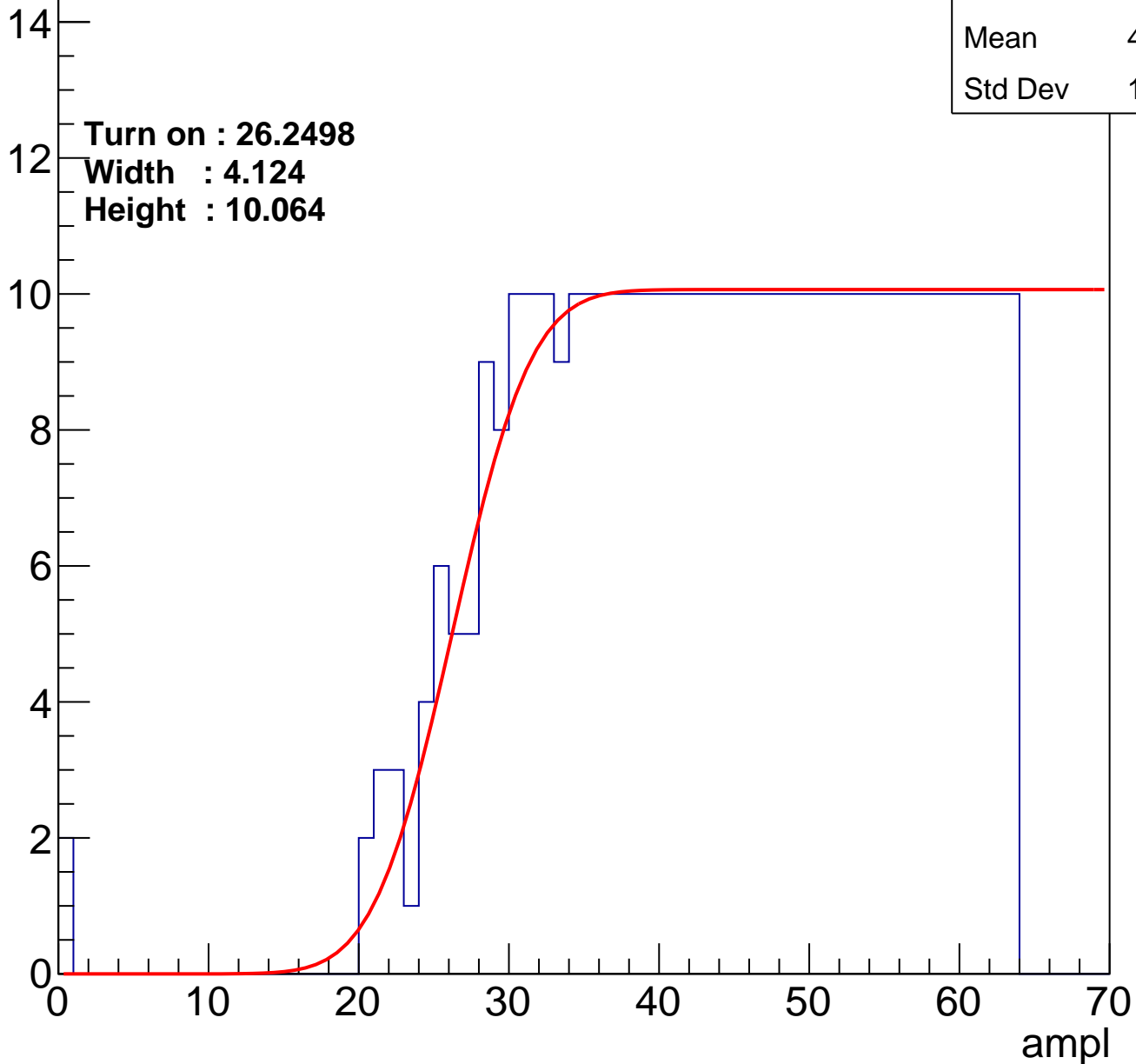
Entries	387
Mean	43.83
Std Dev	11.83

Turn on : 26.2498

Width : 4.124

Height : 10.064

Entry





# B1L102S, U2-ch127

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	389
Mean	43.68
Std Dev	12.1

Turn on : 25.8796

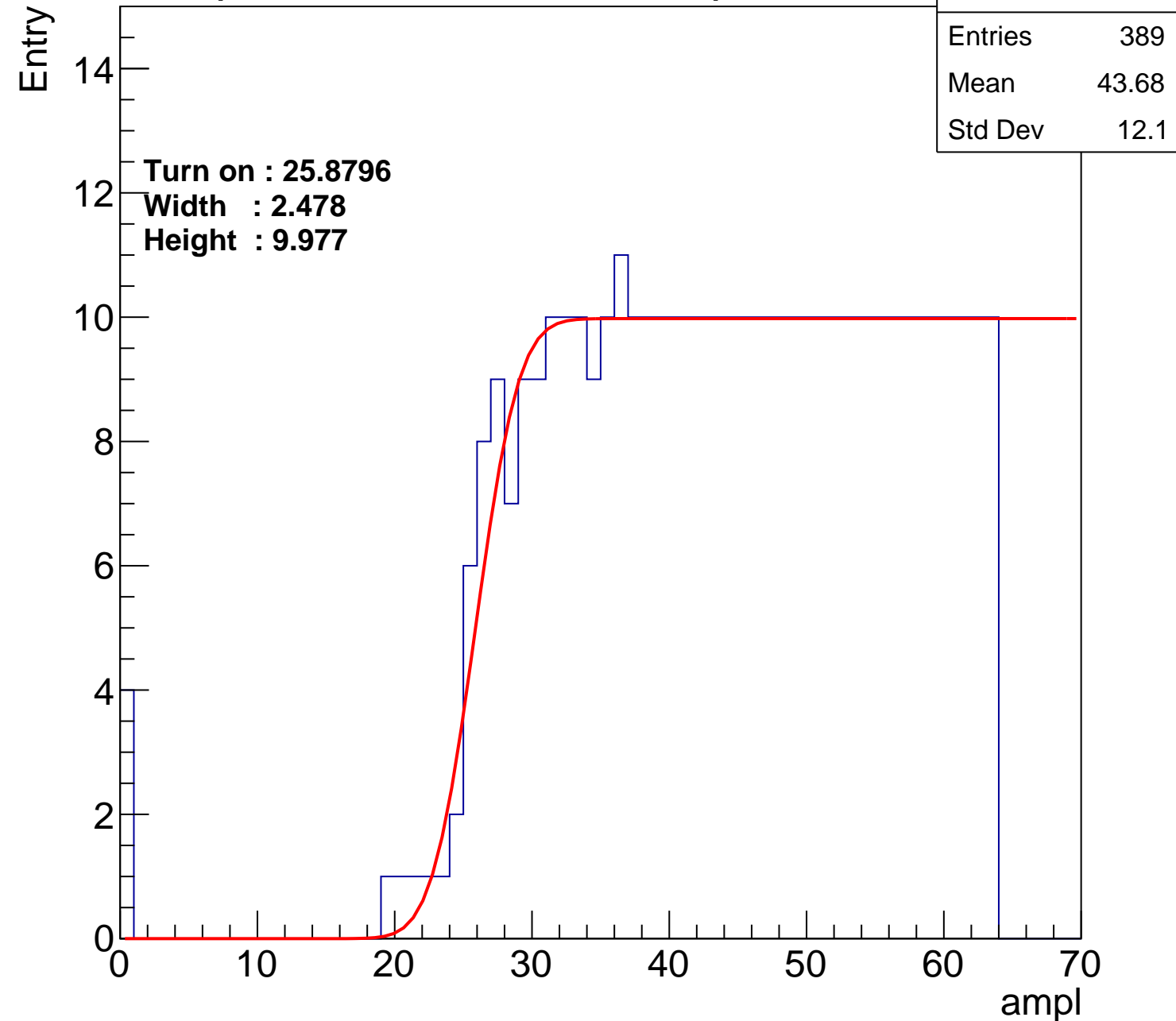
Width : 2.478

Height : 9.977

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L102S, U2-ch127

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	389
Mean	43.68
Std Dev	12.1

Turn on : 25.8796

Width : 2.478

Height : 9.977

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl

