



# B1L002S, U2-ch0

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	397
Mean	43.49
Std Dev	11.78

Turn on : 24.4719

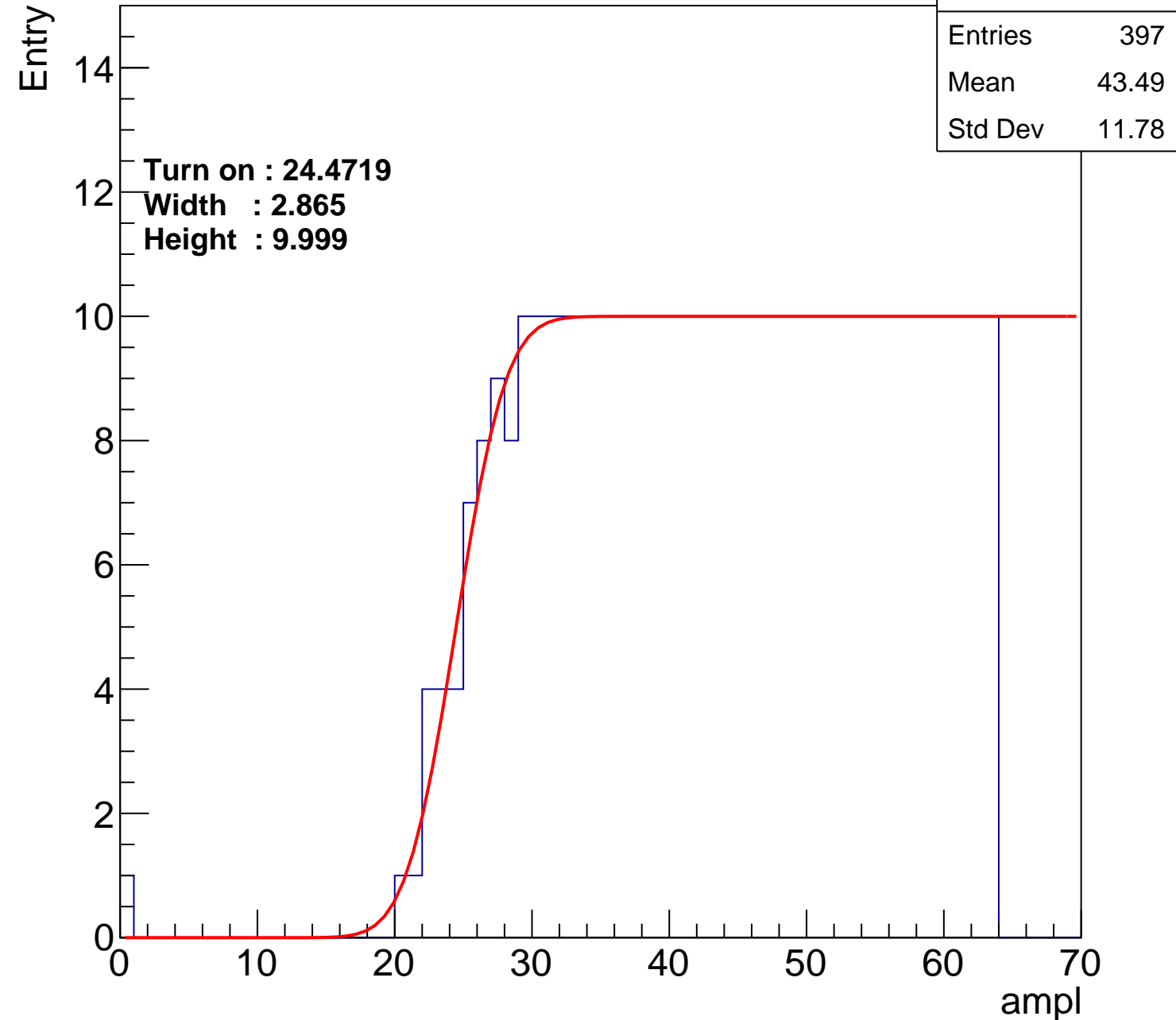
Width : 2.865

Height : 9.999

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch1

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	393
Mean	43.66
Std Dev	11.79

Turn on : 24.6269

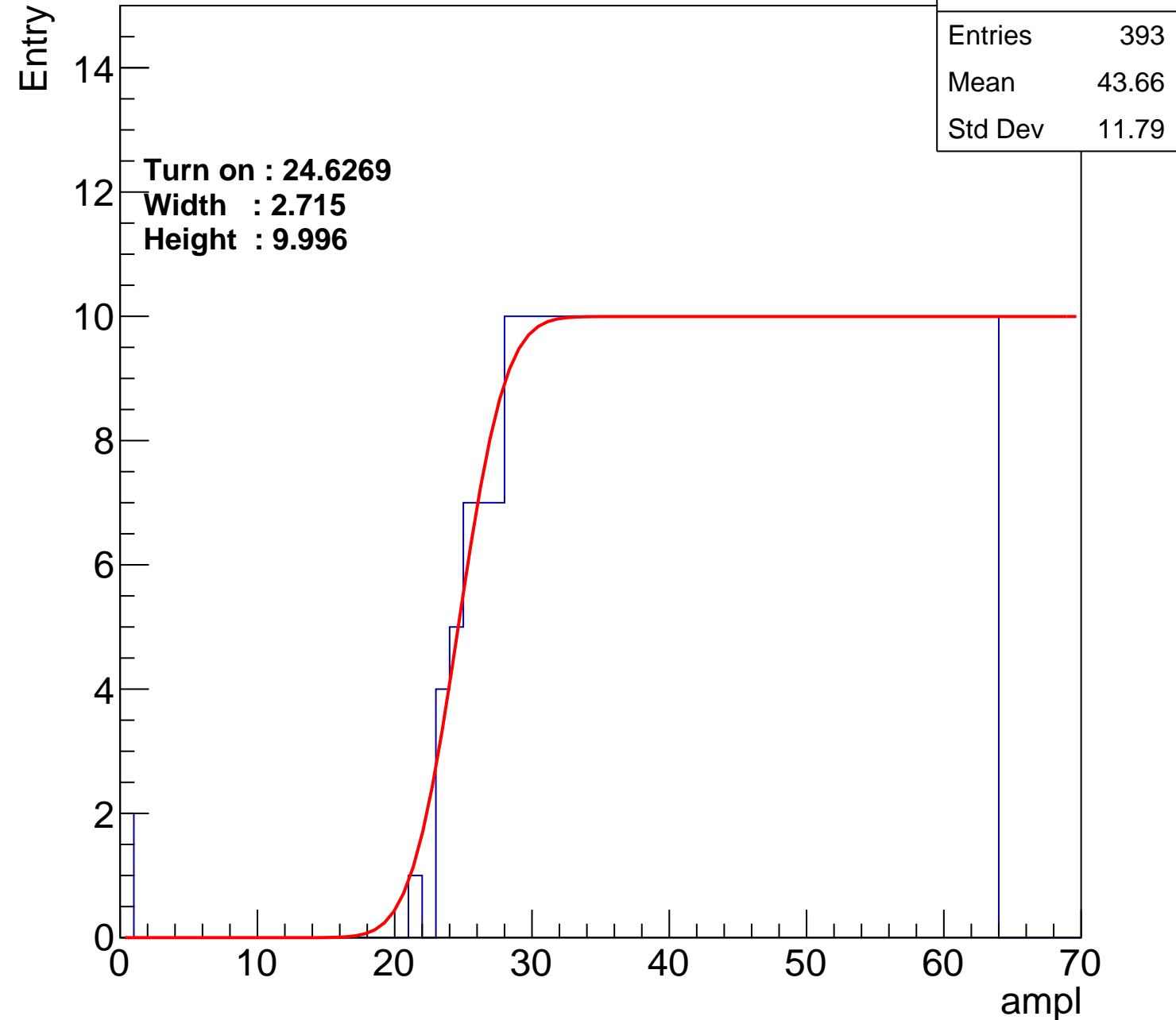
Width : 2.715

Height : 9.996

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch2

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	388
Mean	43.76
Std Dev	12.03

Turn on : 26.0047

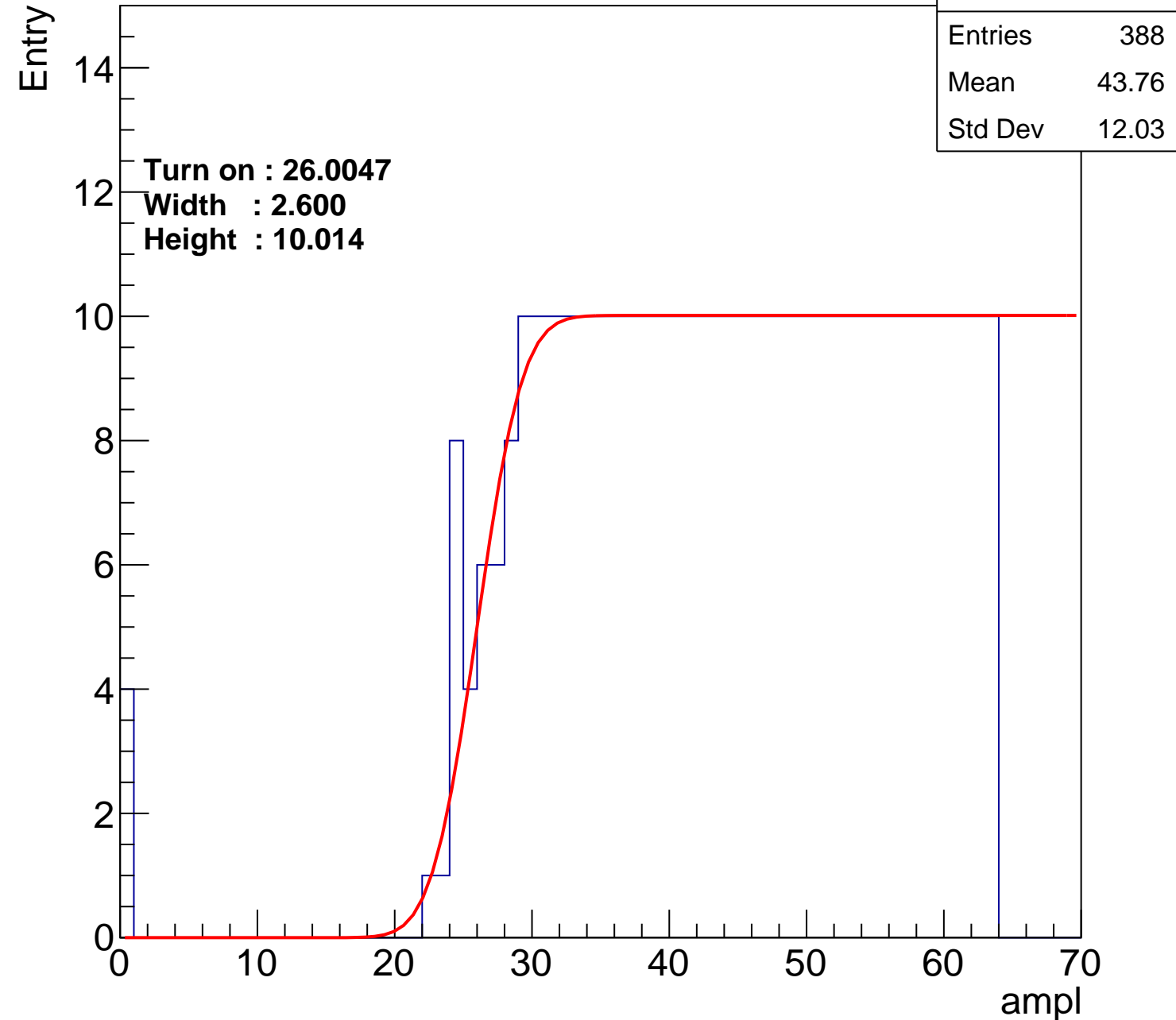
Width : 2.600

Height : 10.014

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch3

**calib\_packv5\_042523\_0143.root, FC#10, port B3**

Entries	396
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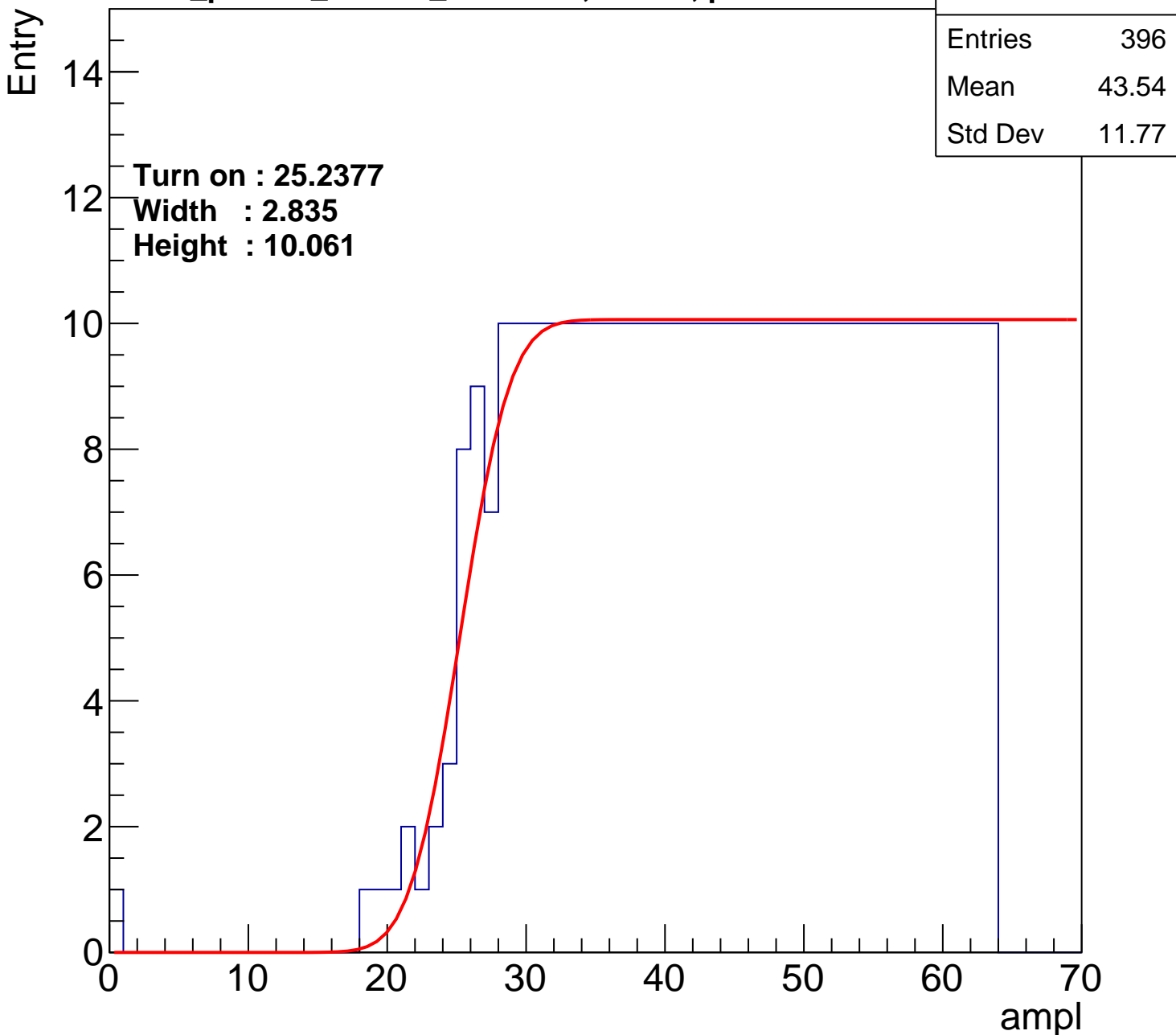
Mean	43.54
------	-------

Std Dev	11.77
---------	-------

**Turn on : 25.2377**

**Width : 2.835**

**Height : 10.061**



# B1L002S, U2-ch4

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	397
Mean	43.43
Std Dev	11.95

Turn on : 25.0181

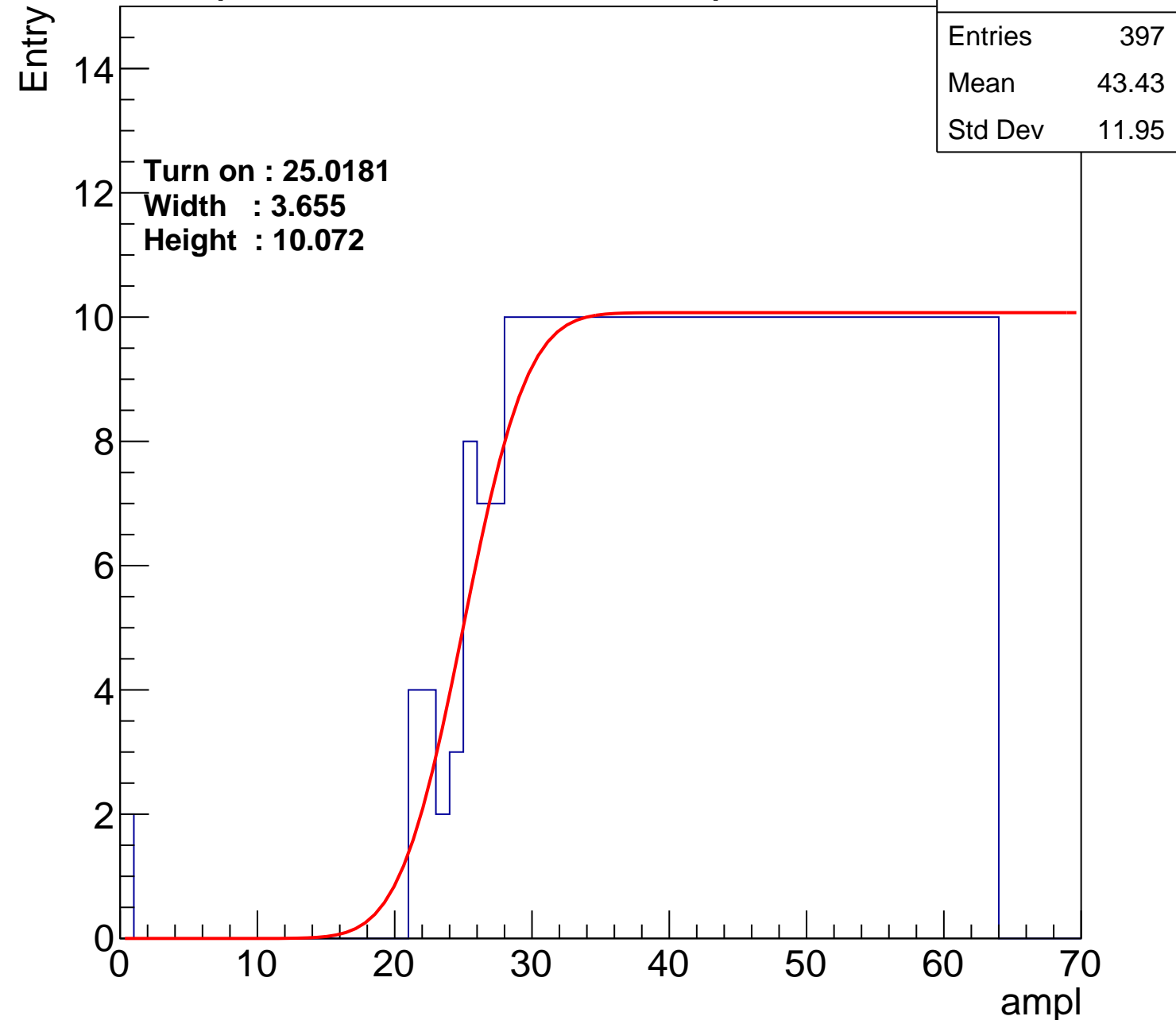
Width : 3.655

Height : 10.072

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch5

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	383
Mean	43.96
Std Dev	12.05

Turn on : 26.3578

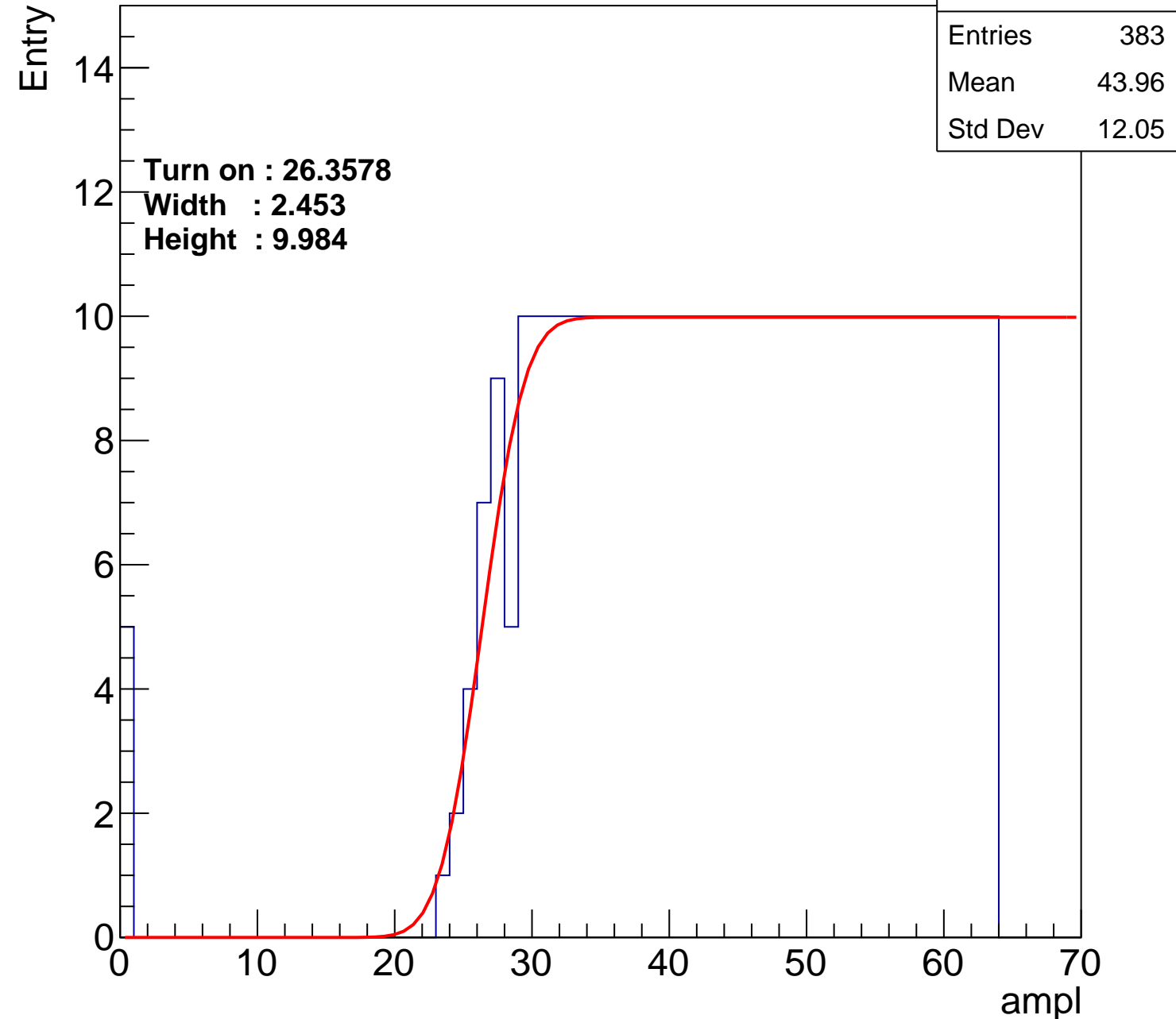
Width : 2.453

Height : 9.984

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch6

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	395
Mean	43.51
Std Dev	11.99

Turn on : 24.8378

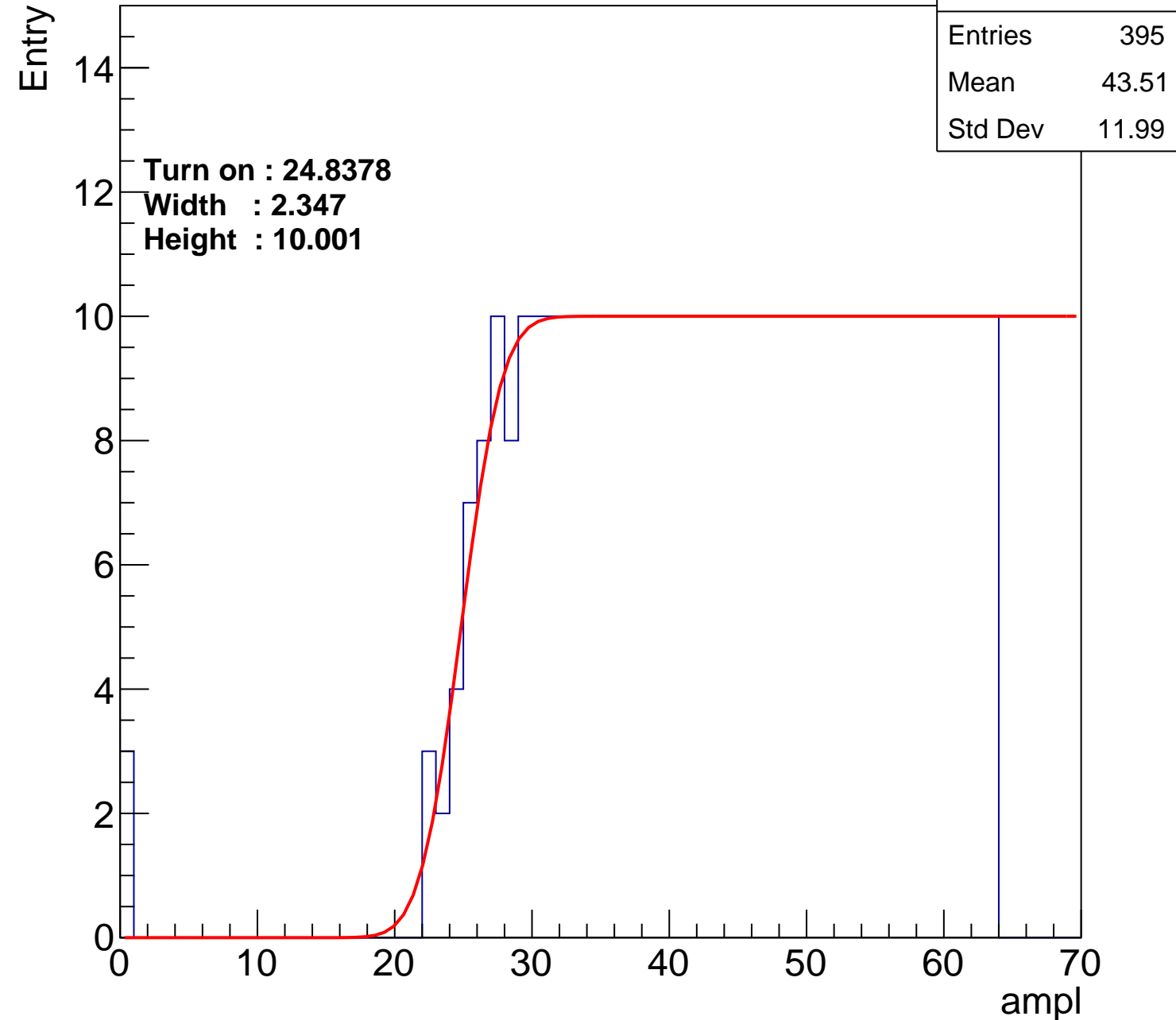
Width : 2.347

Height : 10.001

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L002S, U2-ch7

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	391
Mean	43.74
Std Dev	11.77

Turn on : 24.5461

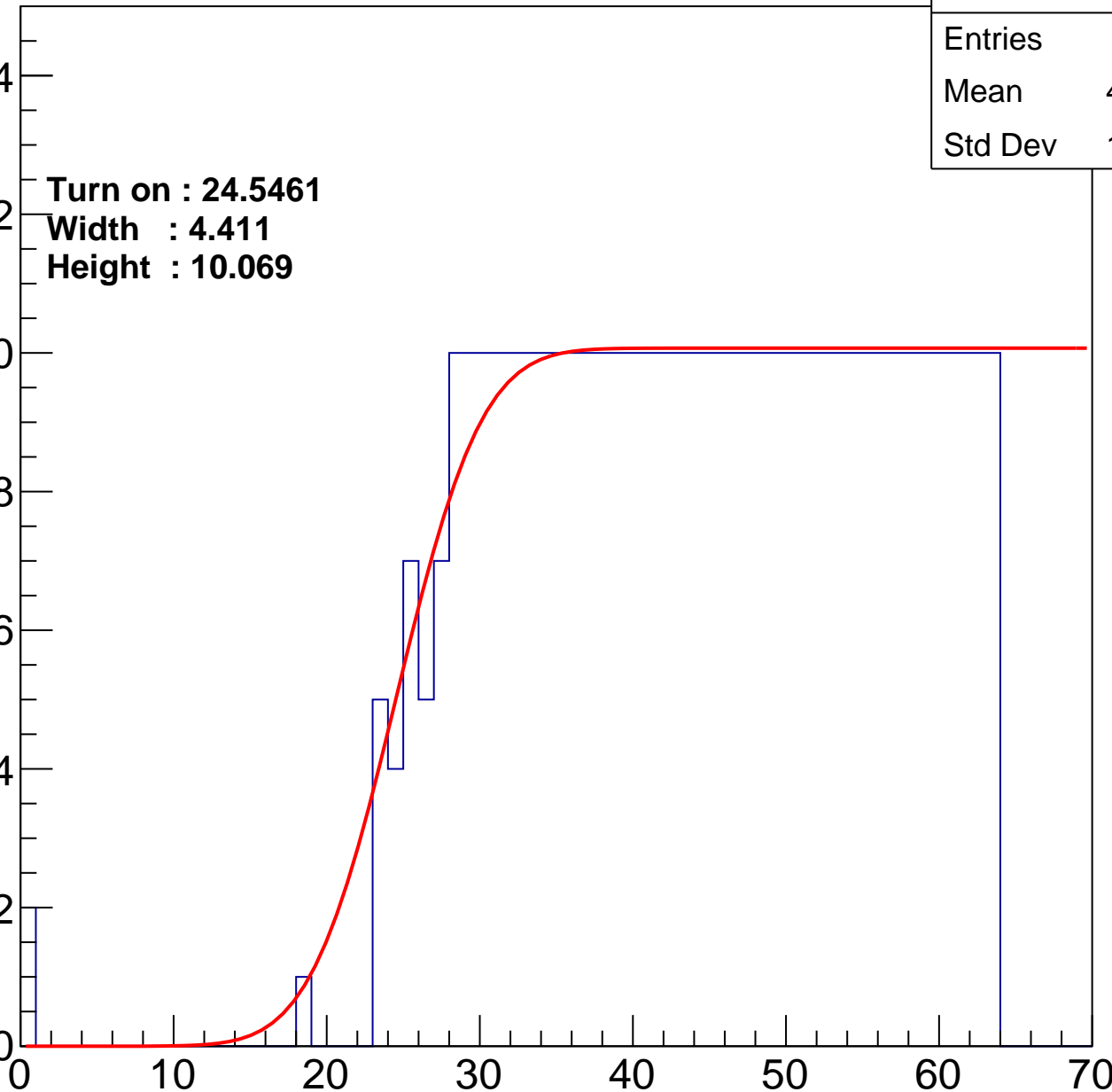
Width : 4.411

Height : 10.069

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch8

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	380
Mean	44.16
Std Dev	11.84

Turn on : 26.4273

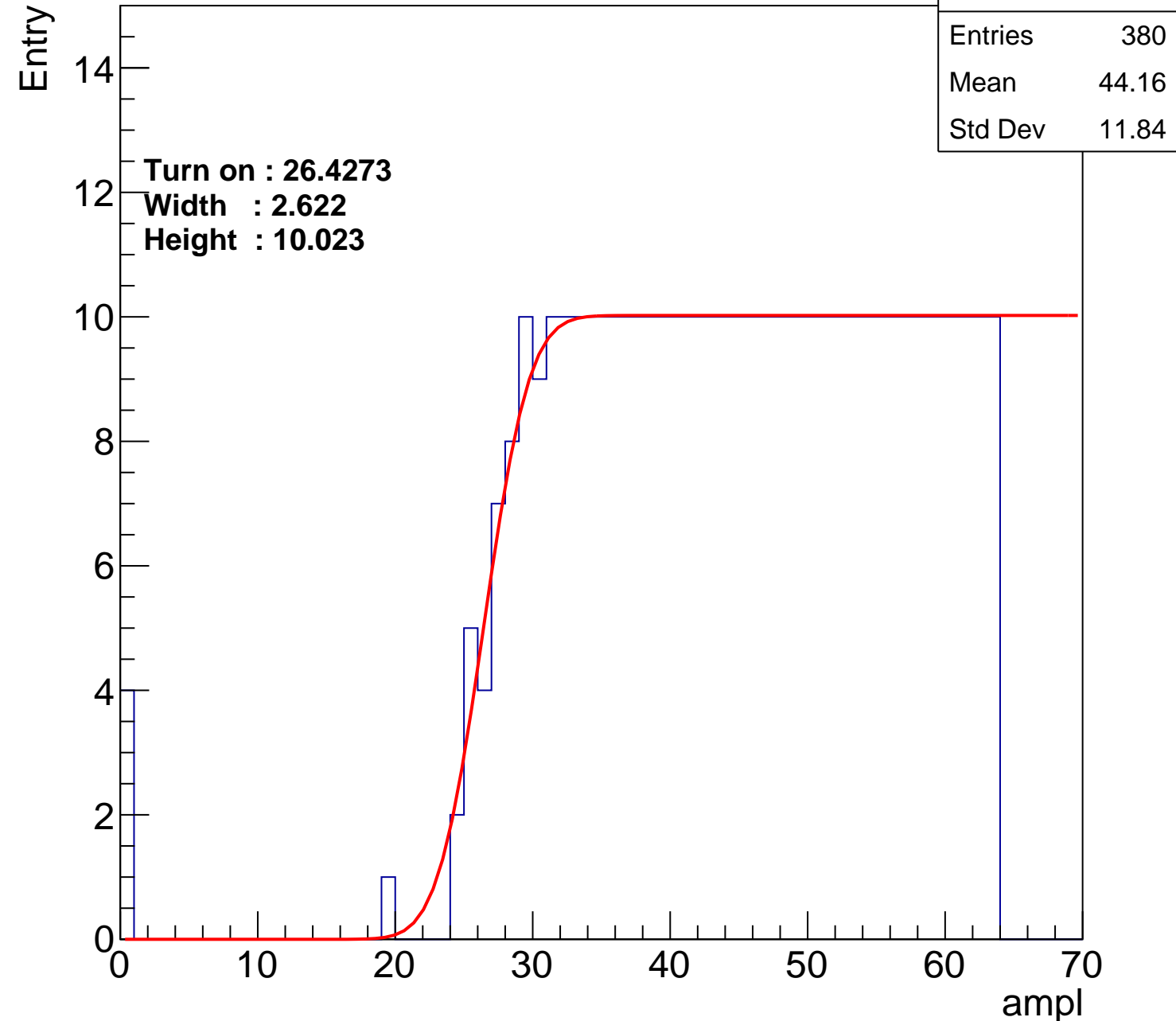
Width : 2.622

Height : 10.023

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch9

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	408
Mean	42.82
Std Dev	12.44

Turn on : 23.2263

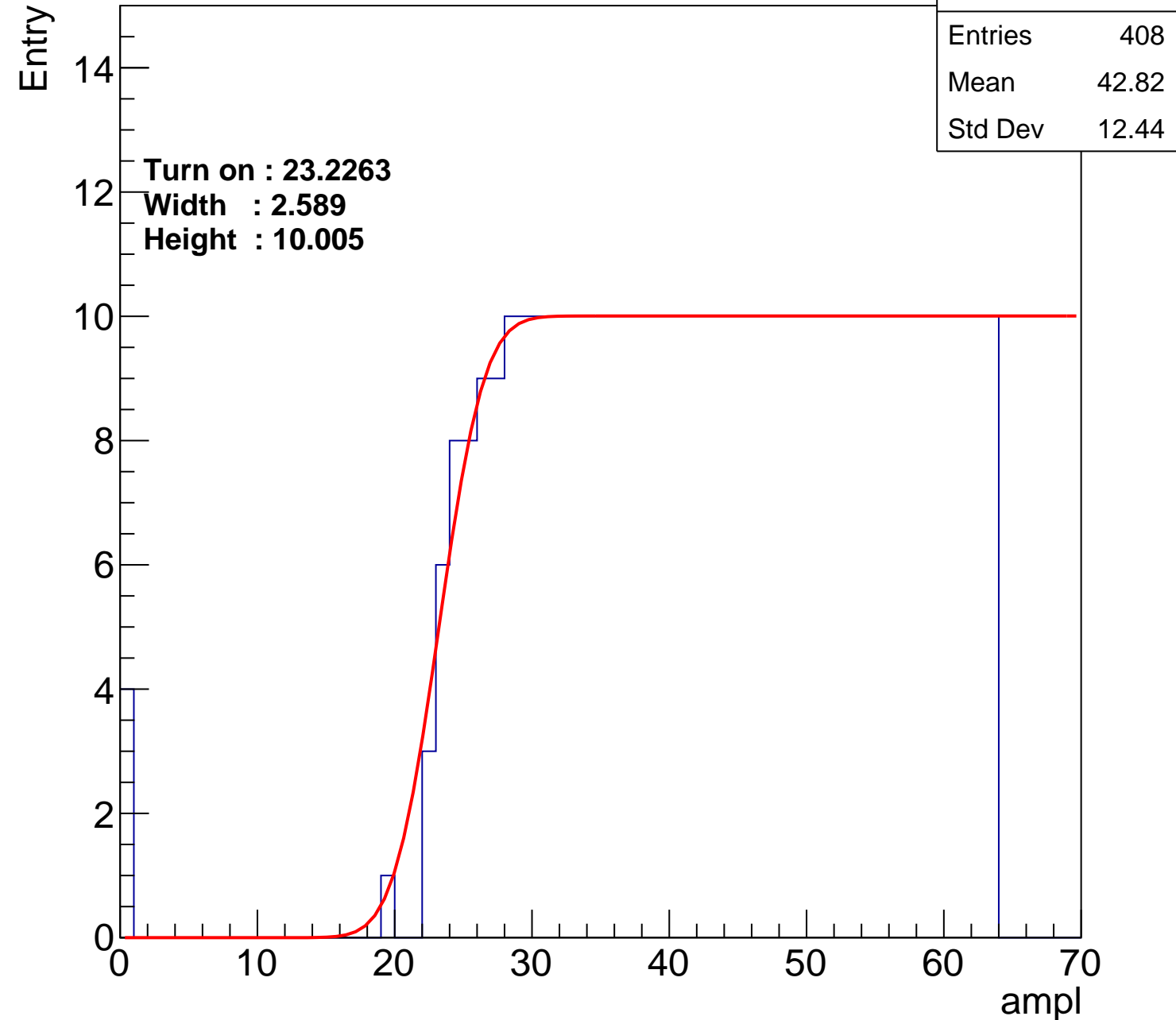
Width : 2.589

Height : 10.005

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch10

calib\_packv5\_042523\_0143.root, FC#10, port B3

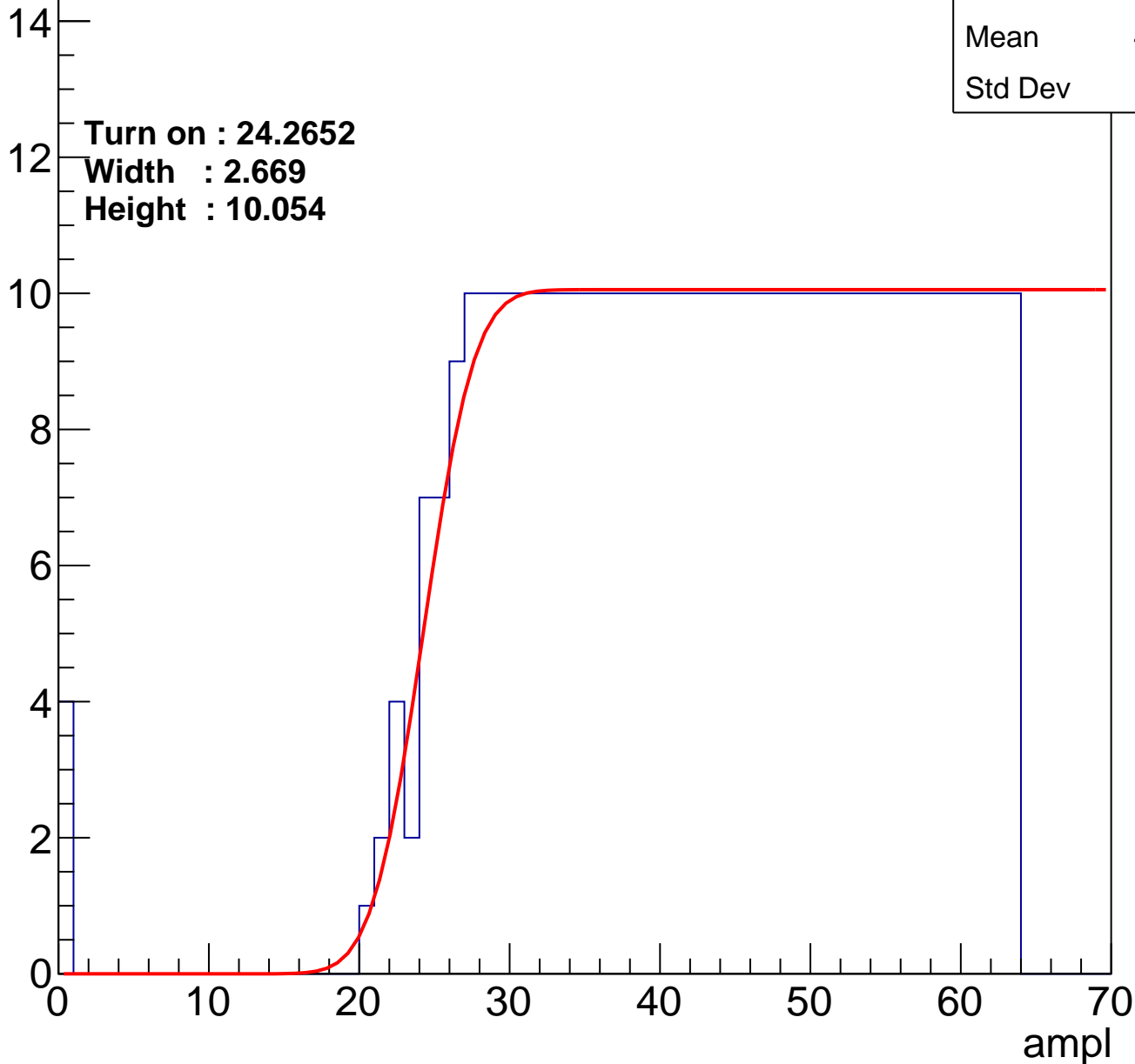
Entry

Entries	406
Mean	42.91
Std Dev	12.41

Turn on : 24.2652

Width : 2.669

Height : 10.054



# B1L002S, U2-ch11

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	379
Mean	44.27
Std Dev	11.63

Turn on : 26.8742

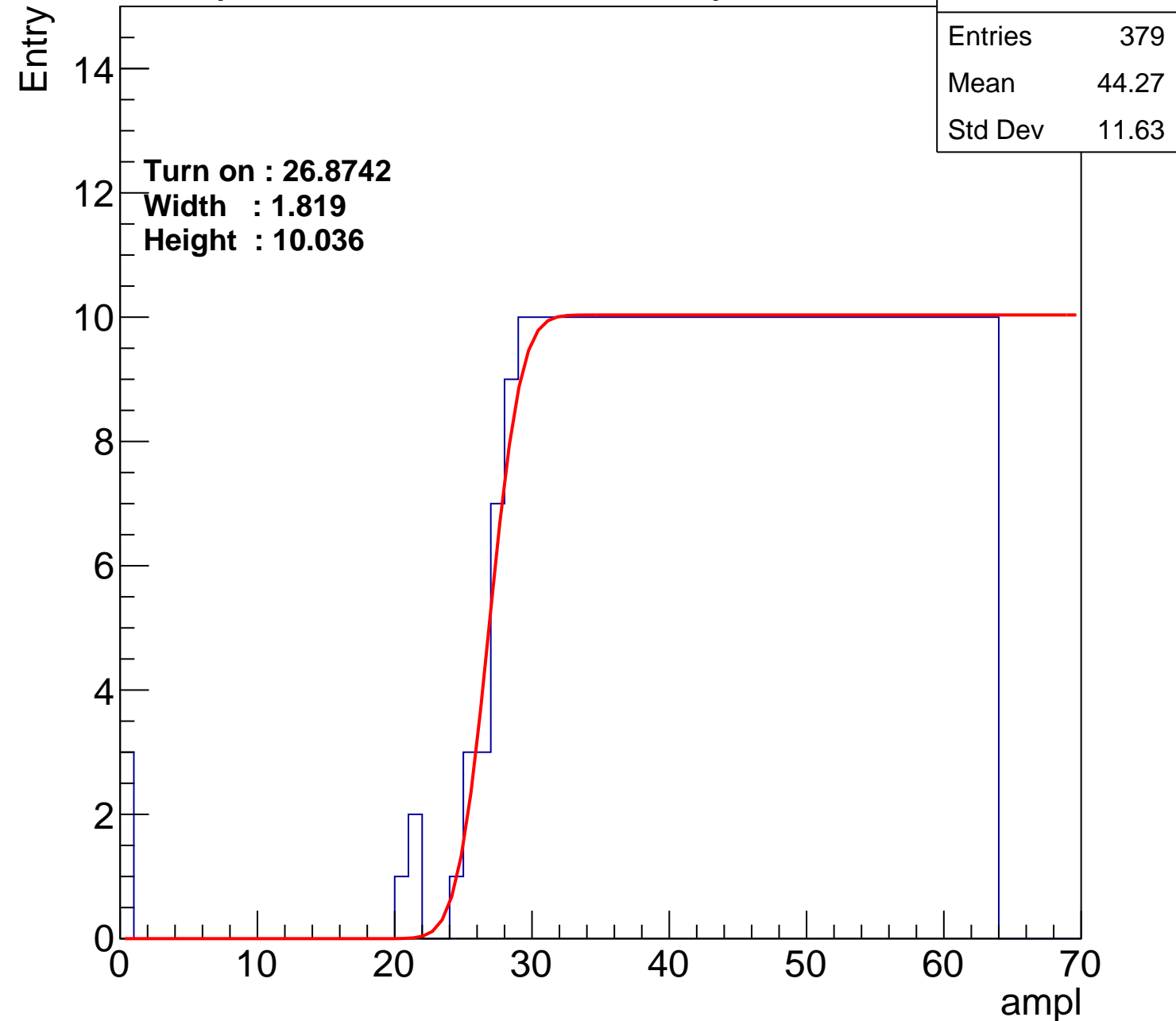
Width : 1.819

Height : 10.036

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch12

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	397
Mean	43.34
Std Dev	12.21

Turn on : 24.6007

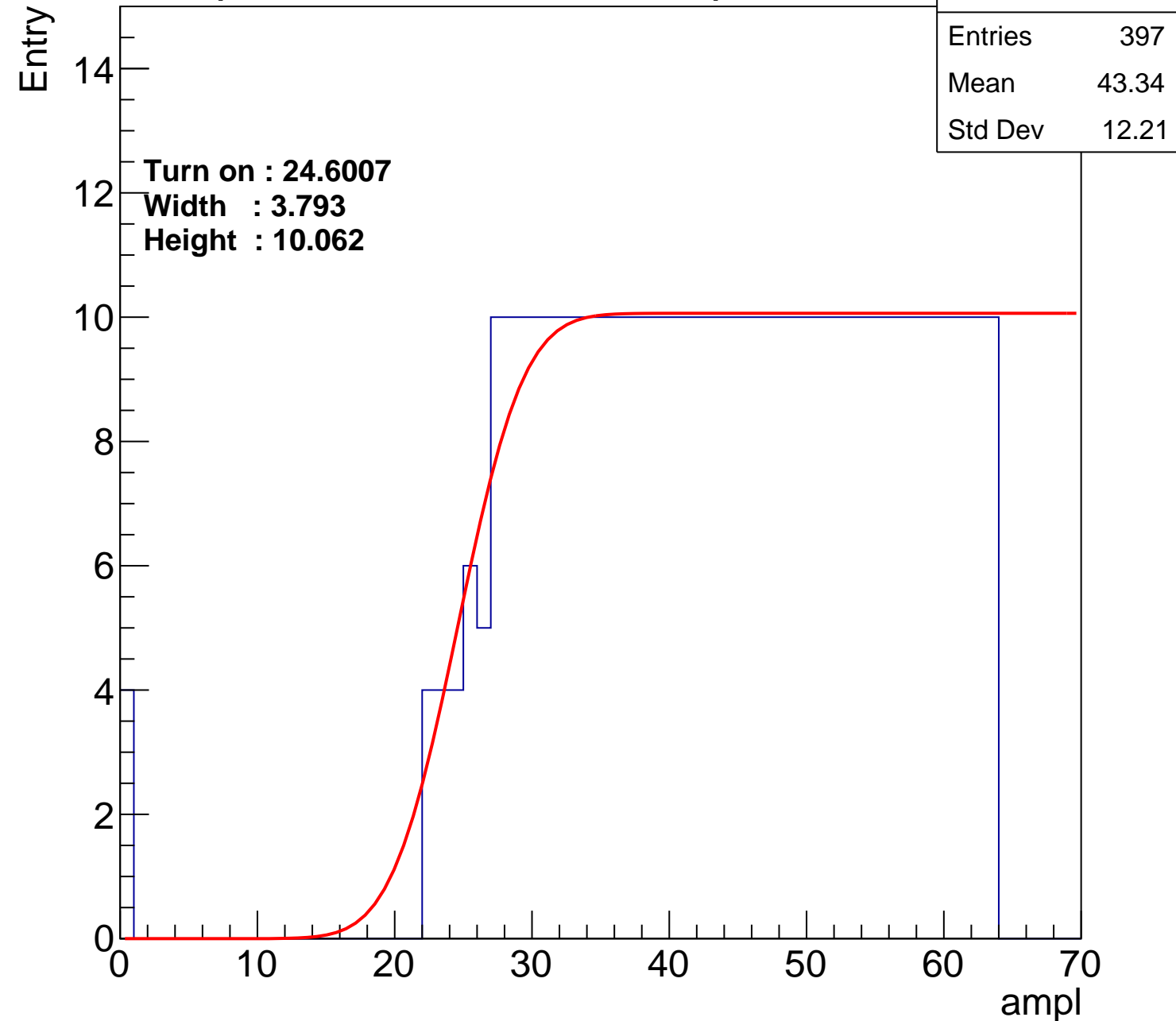
Width : 3.793

Height : 10.062

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch13

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	378
Mean	44.44
Std Dev	11.25

Turn on : 26.4858

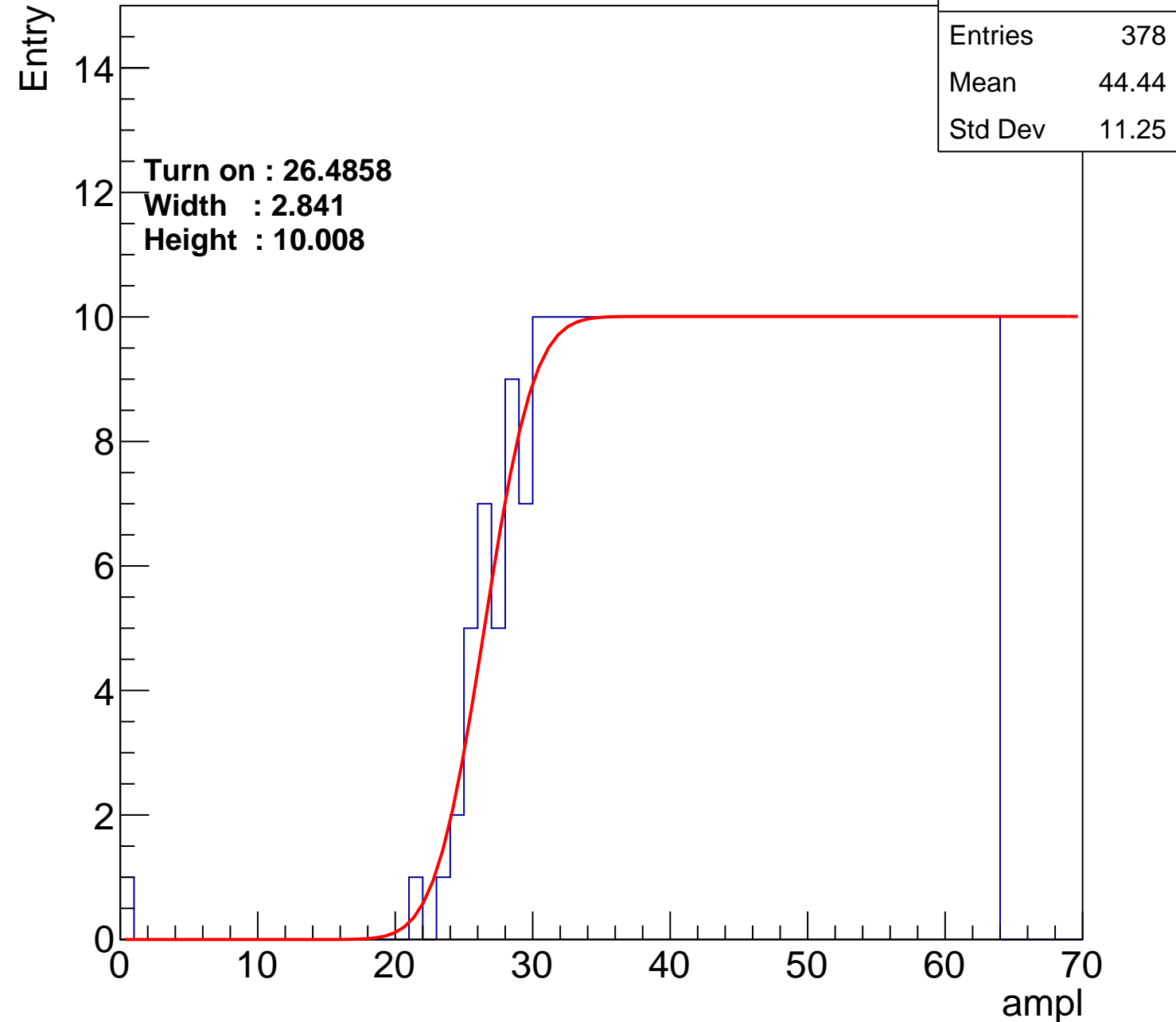
Width : 2.841

Height : 10.008

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch14

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	397
Mean	43.4
Std Dev	12.05

Turn on : 24.9107

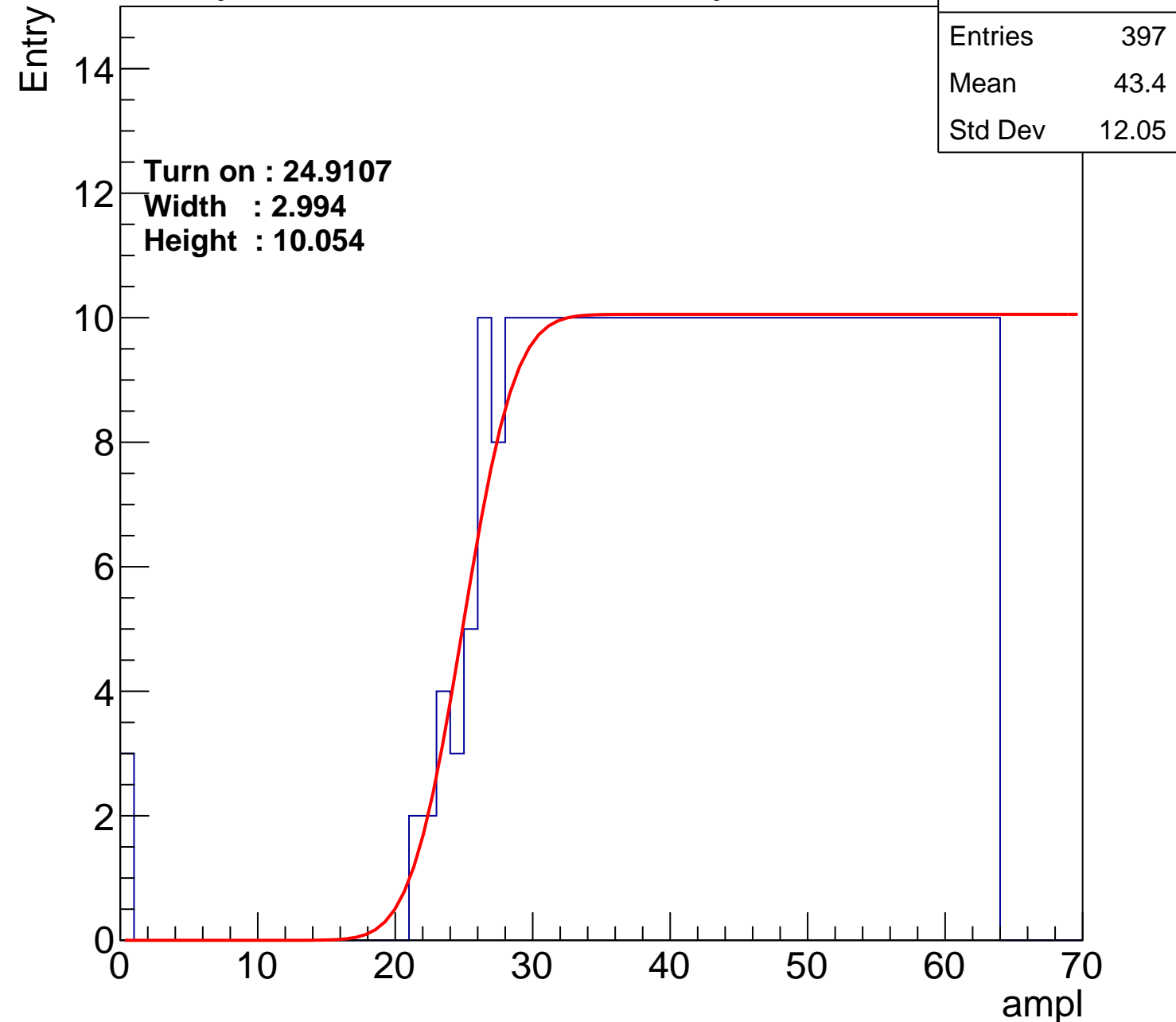
Width : 2.994

Height : 10.054

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L002S, U2-ch15

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	383
Mean	44.11
Std Dev	11.67

Turn on : 26.1771

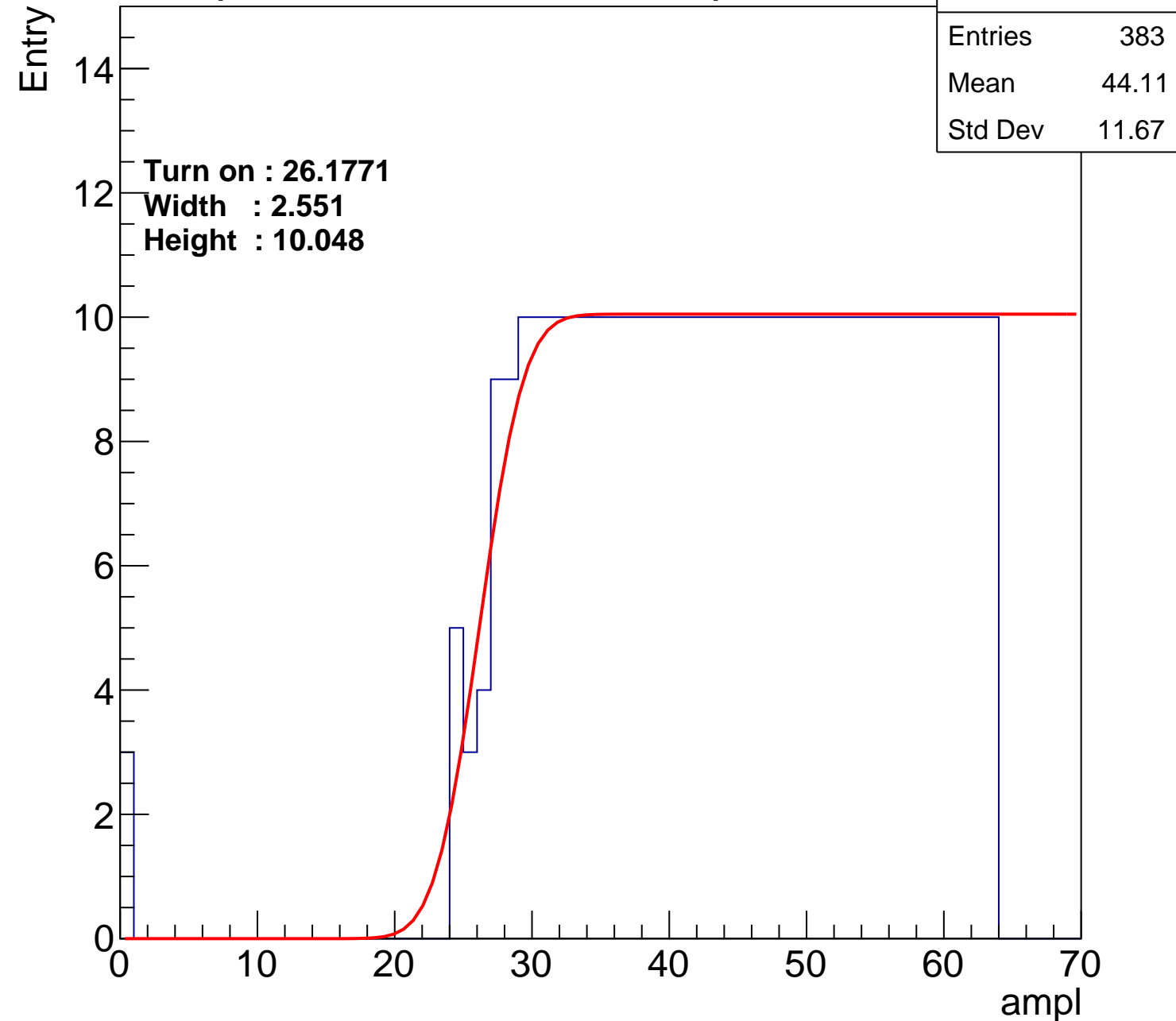
Width : 2.551

Height : 10.048

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch16

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	406
Mean	42.78
Std Dev	12.72

Turn on : 23.5131

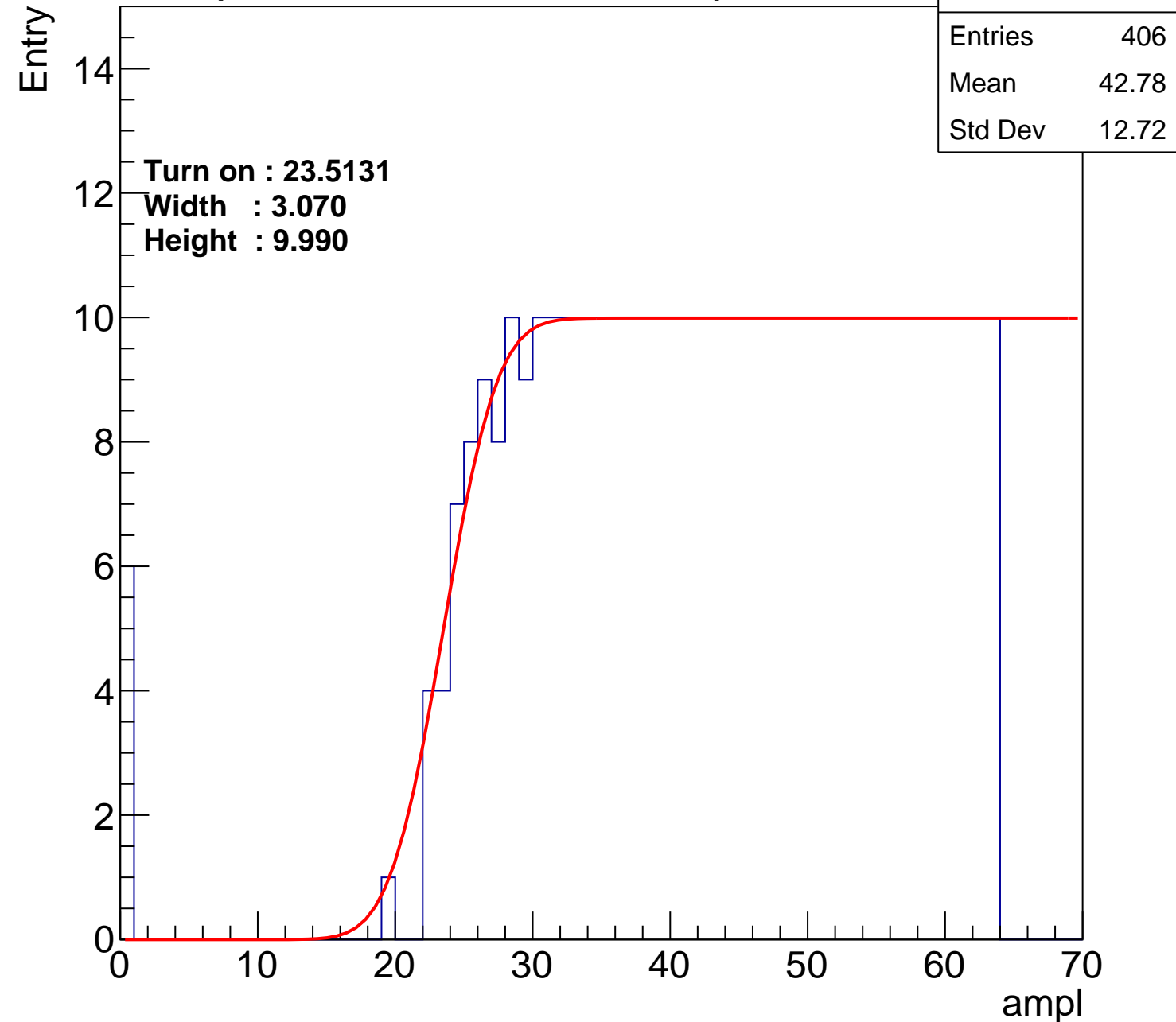
Width : 3.070

Height : 9.990

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch17

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	407
Mean	42.88
Std Dev	12.36

Turn on : 25.0006

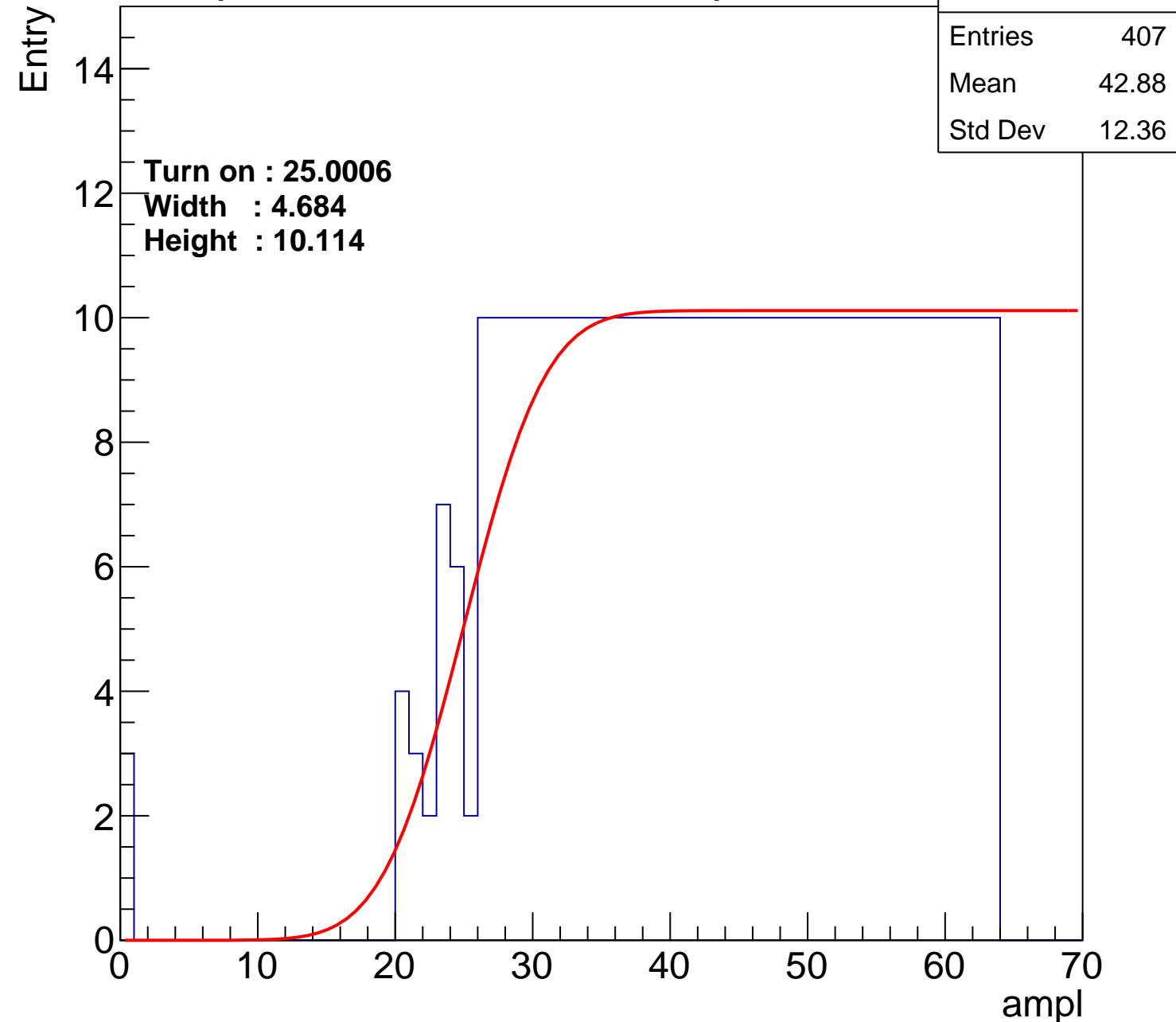
Width : 4.684

Height : 10.114

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch18

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	398
Mean	43.32
Std Dev	12.12

Turn on : 24.6524

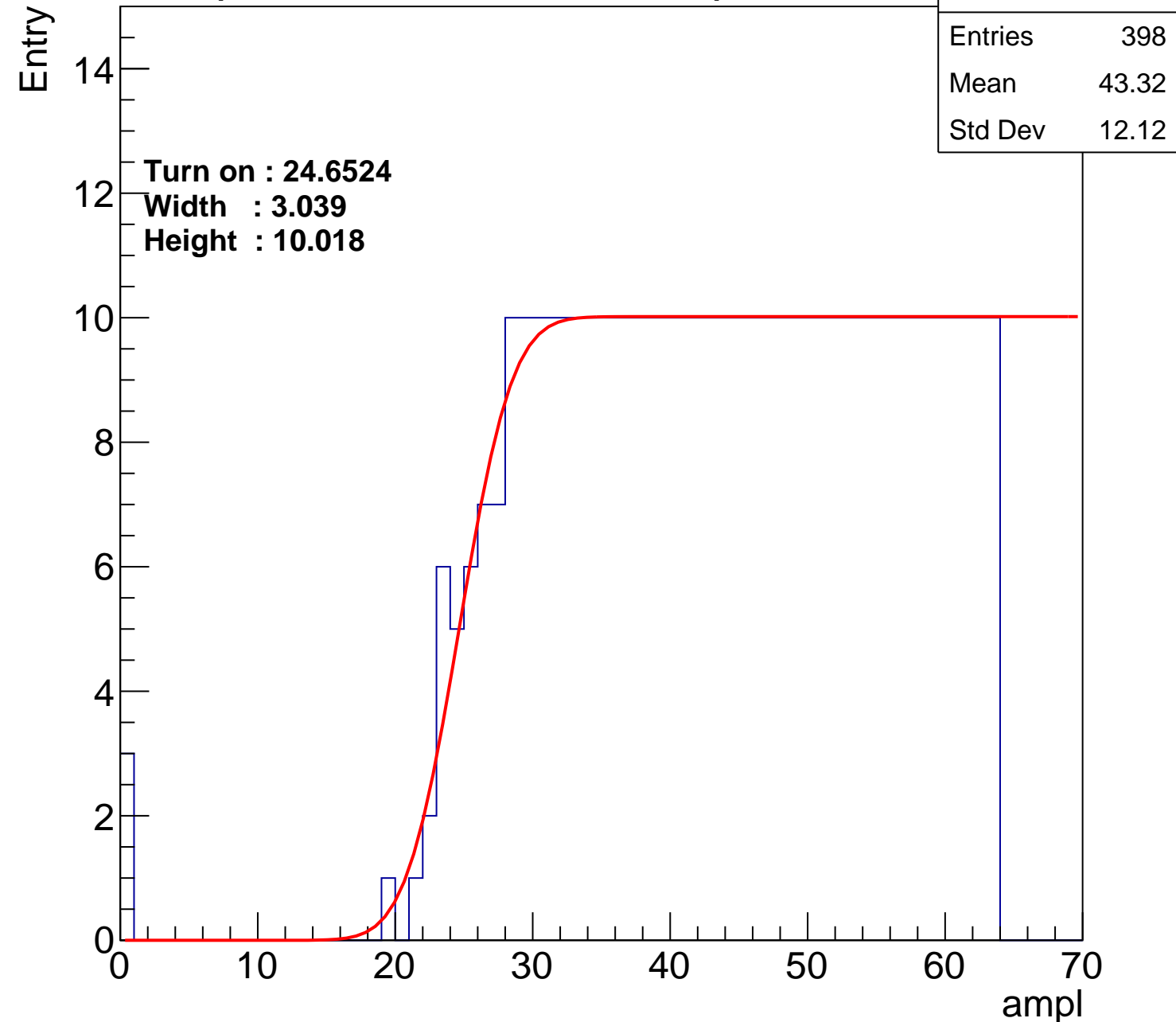
Width : 3.039

Height : 10.018

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch19

calib\_packv5\_042523\_0143.root, FC#10, port B3

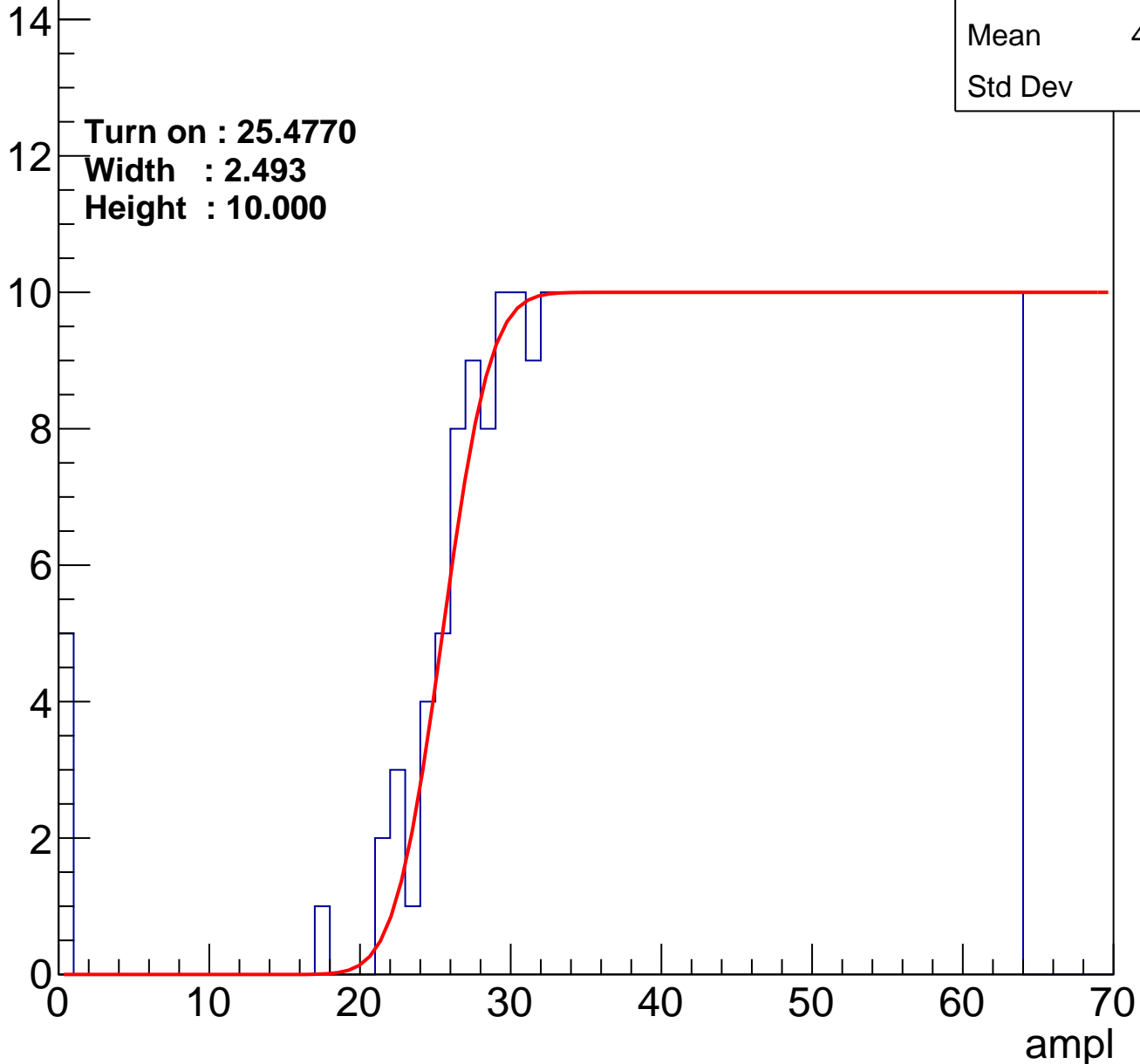
Entries	395
Mean	43.32
Std Dev	12.4

Turn on : 25.4770

Width : 2.493

Height : 10.000

Entry



# B1L002S, U2-ch20

calib\_packv5\_042523\_0143.root, FC#10, port B3

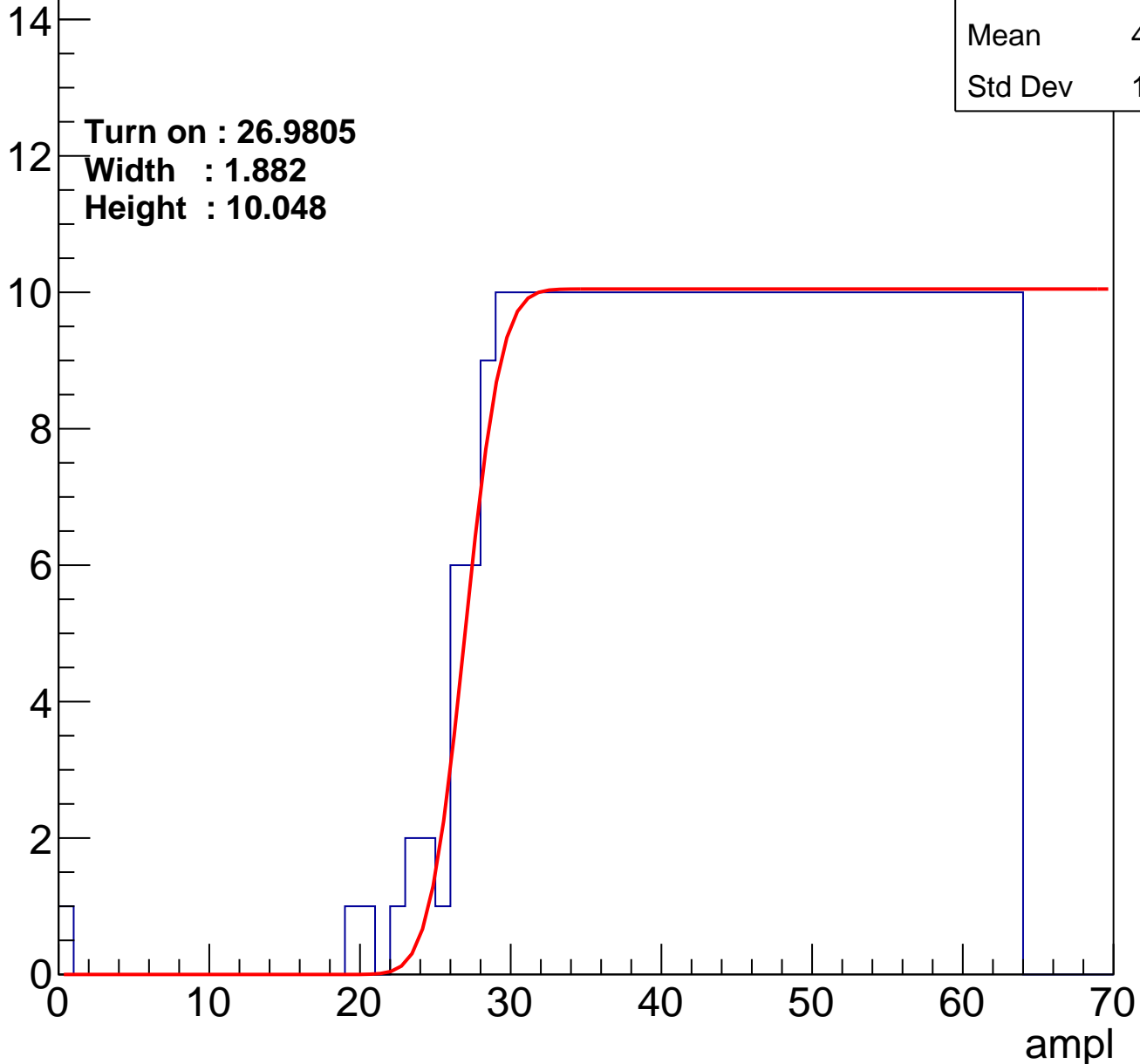
Entries	380
Mean	44.34
Std Dev	11.32

Turn on : 26.9805

Width : 1.882

Height : 10.048

Entry



# B1L002S, U2-ch21

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	393
Mean	43.54
Std Dev	12.04

Turn on : 24.9448

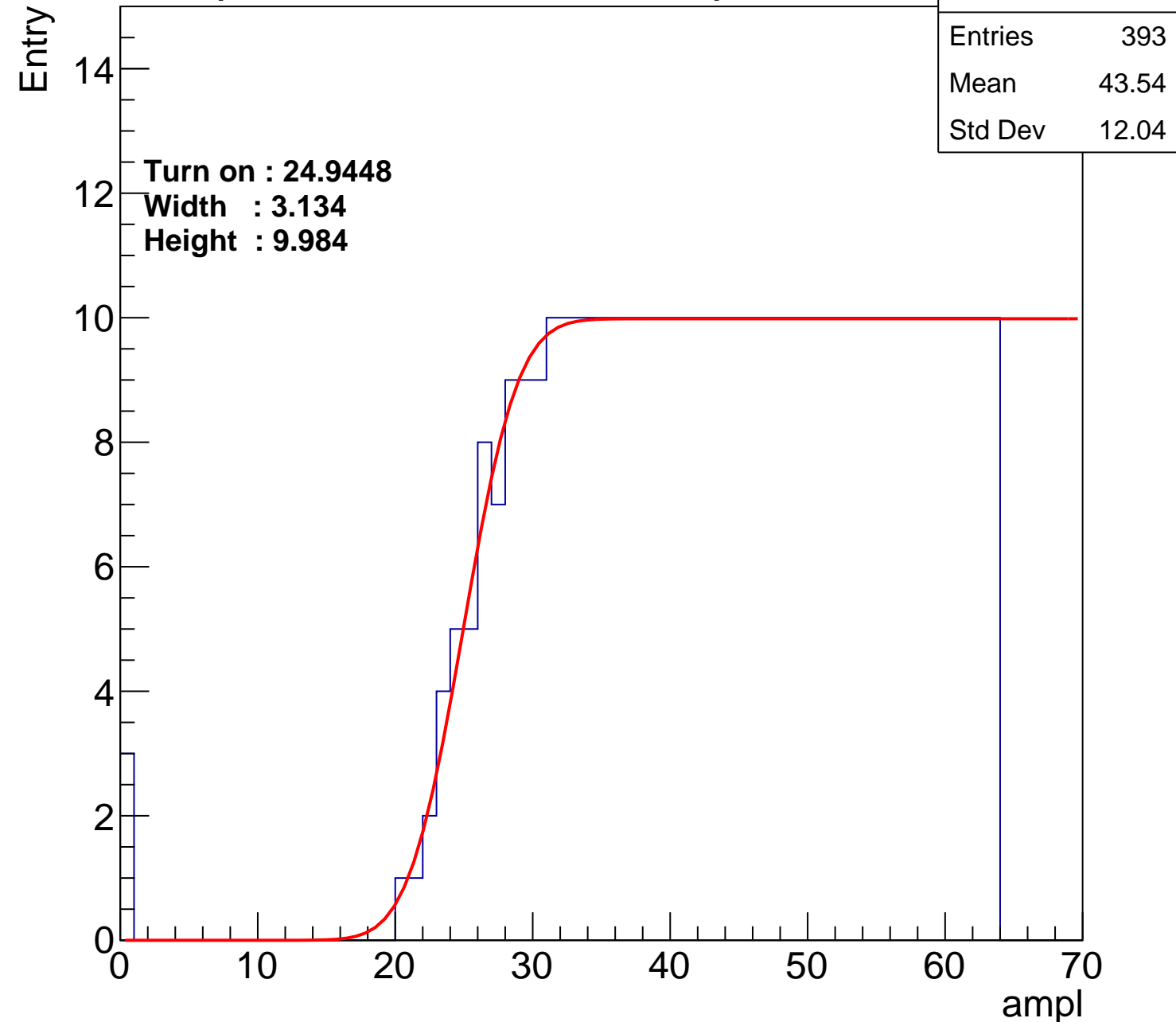
Width : 3.134

Height : 9.984

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch22

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	396
Mean	43.31
Std Dev	12.37

Turn on : 25.1032

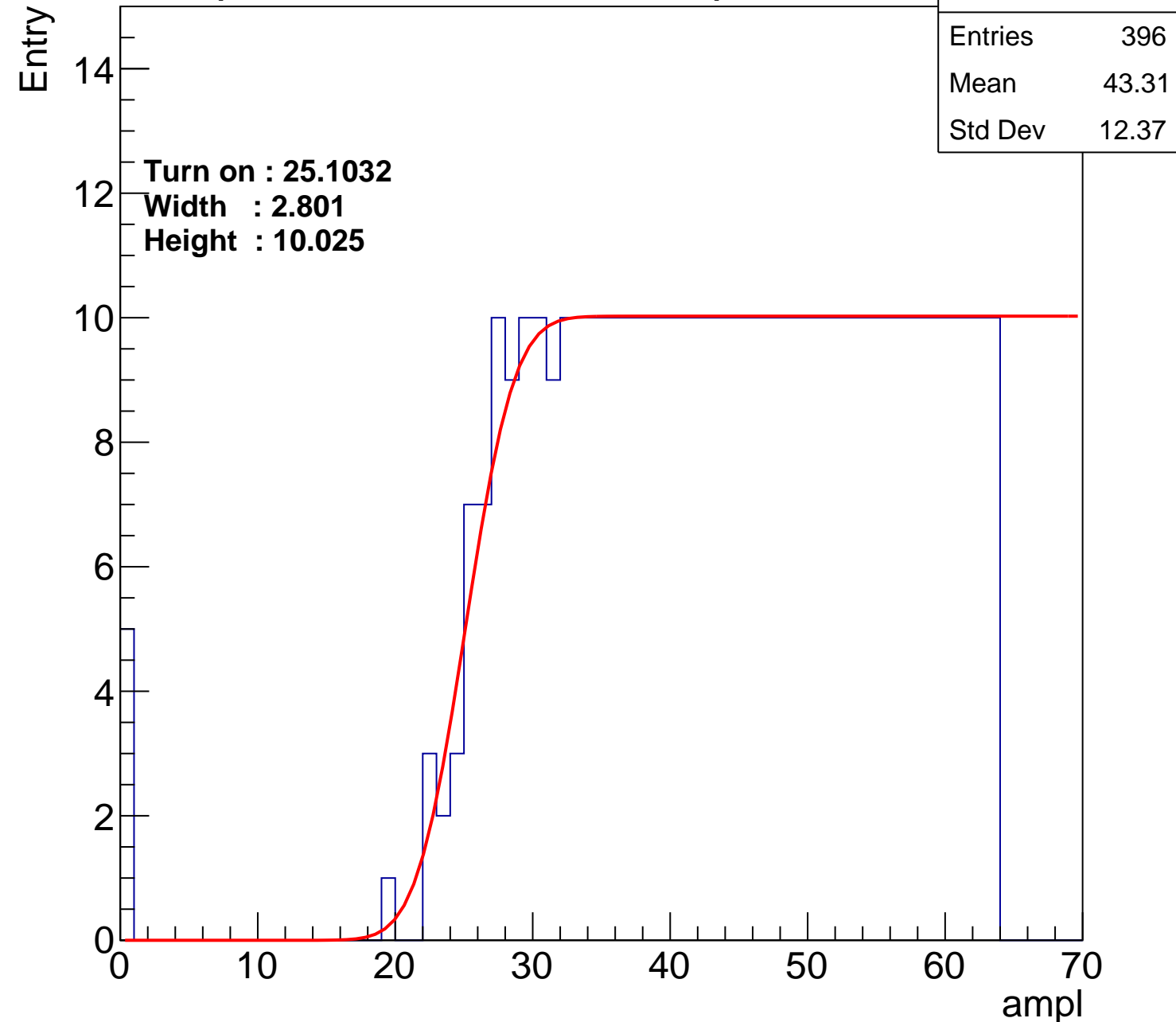
Width : 2.801

Height : 10.025

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L002S, U2-ch23

calib\_packv5\_042523\_0143.root, FC#10, port B3

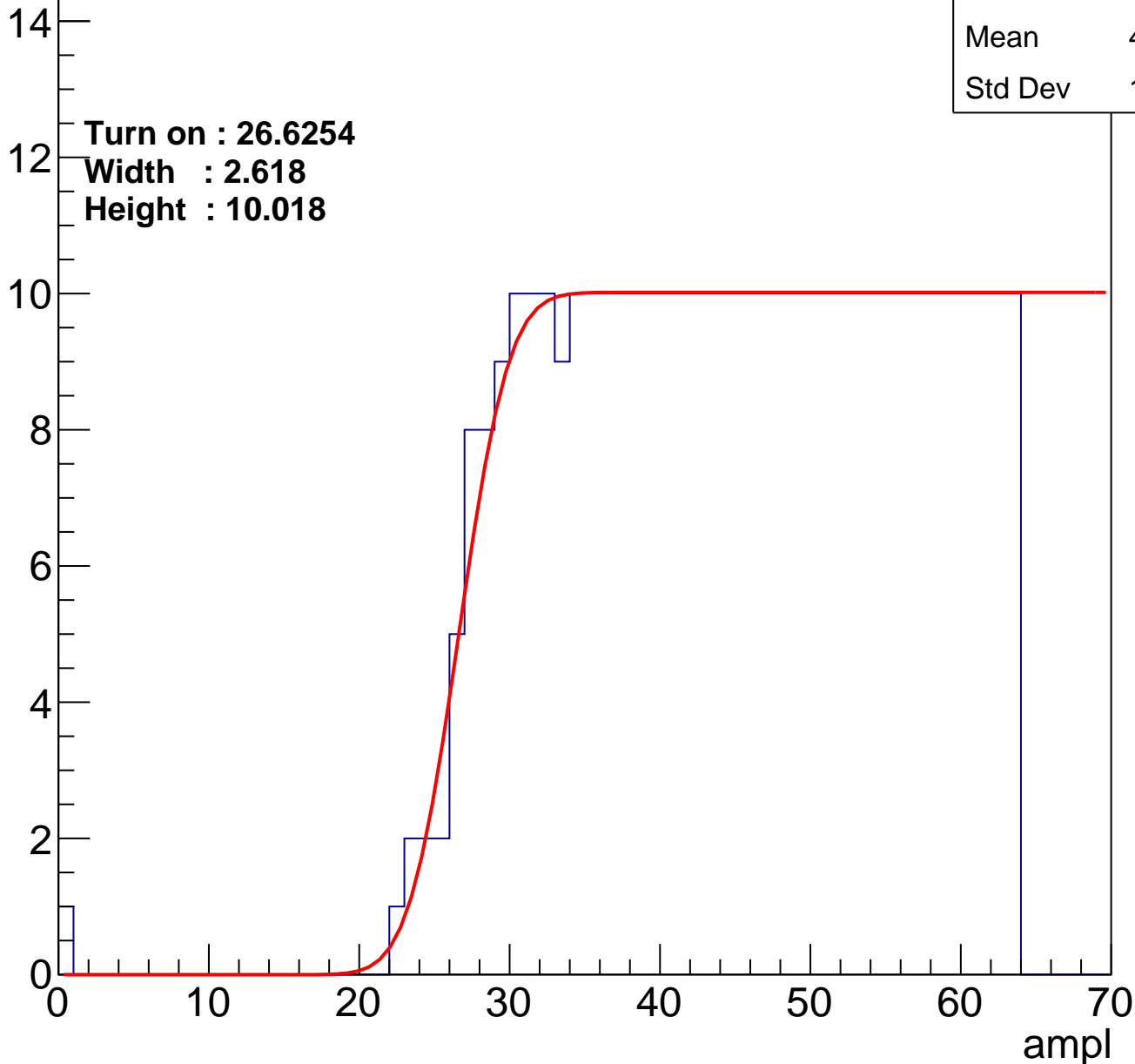
Entry

Entries	377
Mean	44.49
Std Dev	11.22

Turn on : 26.6254

Width : 2.618

Height : 10.018



# B1L002S, U2-ch24

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	388
Mean	43.77
Std Dev	12.02

Turn on : 26.0564

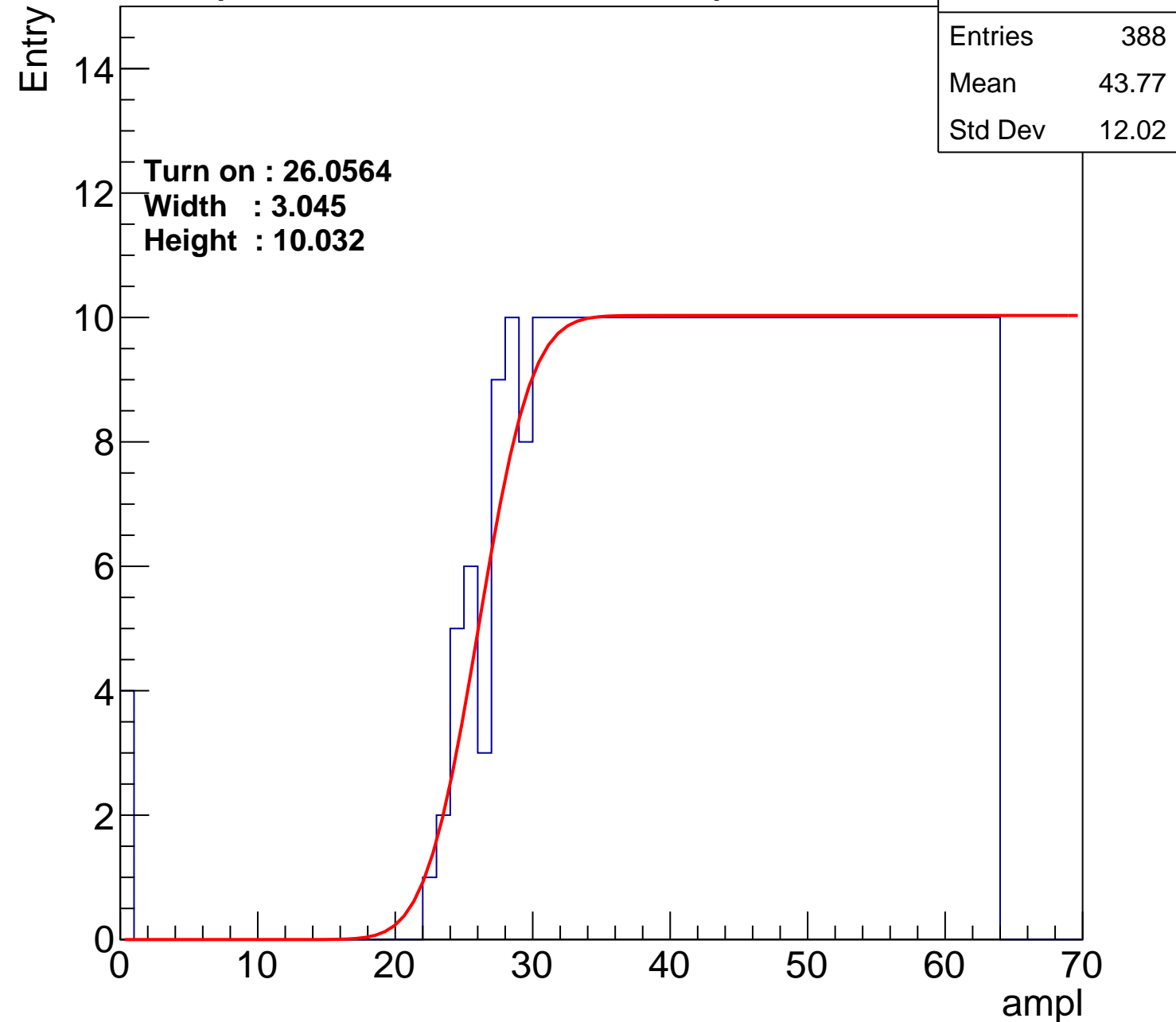
Width : 3.045

Height : 10.032

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch25

calib\_packv5\_042523\_0143.root, FC#10, port B3

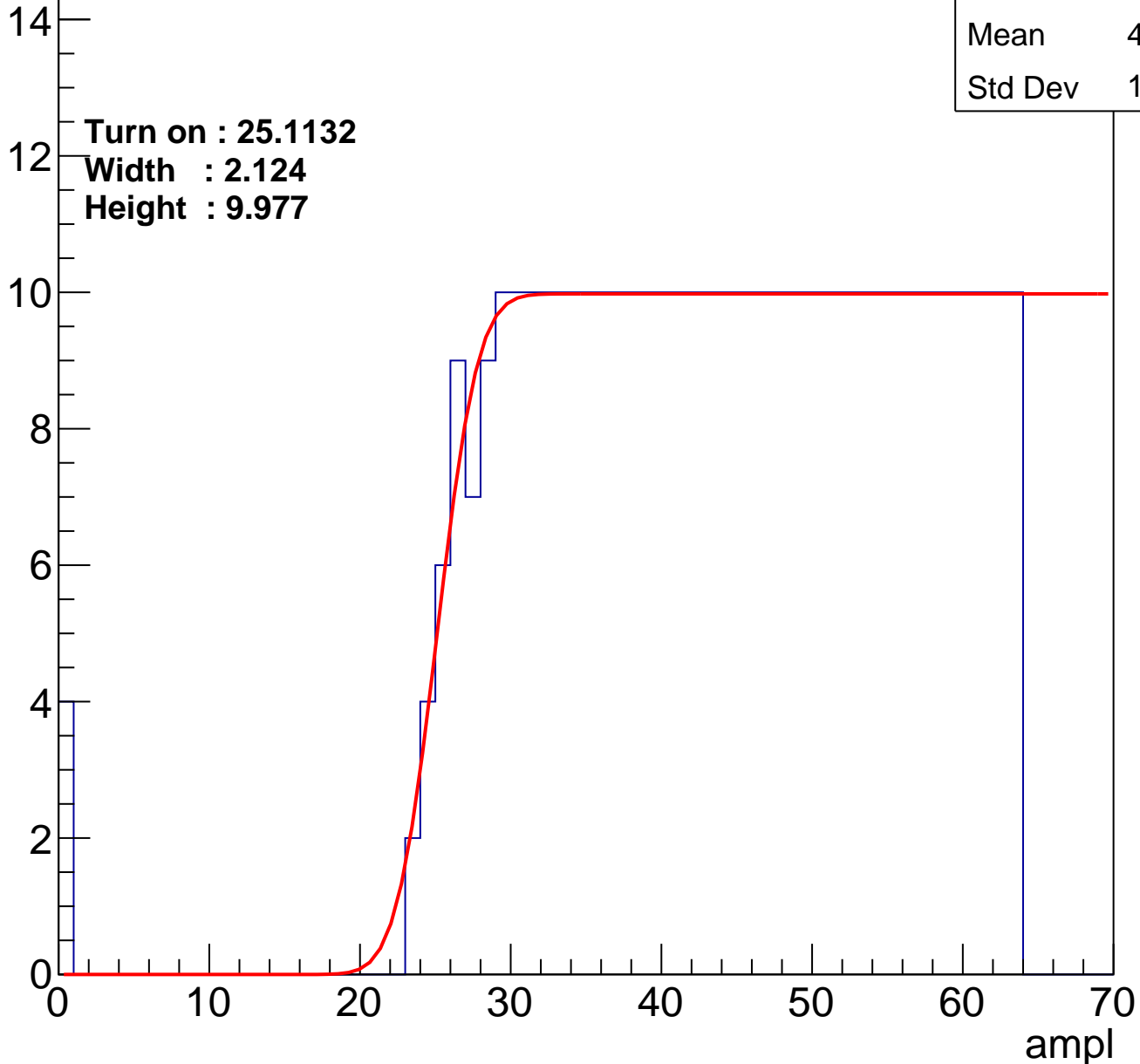
Entries	391
Mean	43.65
Std Dev	12.04

Turn on : 25.1132

Width : 2.124

Height : 9.977

Entry



# B1L002S, U2-ch26

calib\_packv5\_042523\_0143.root, FC#10, port B3

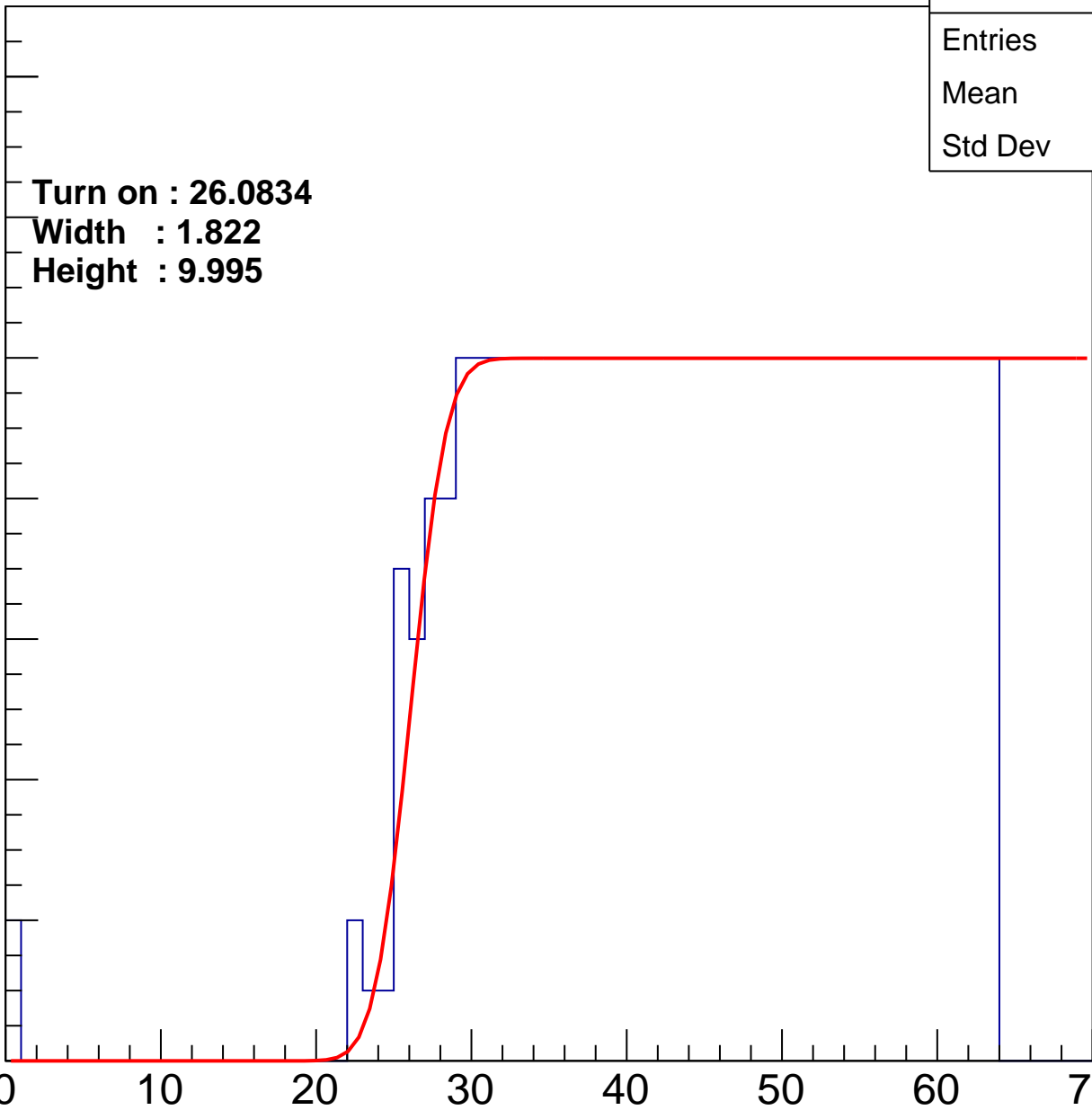
Entry

14  
12  
10  
8  
6  
4  
2  
0

Turn on : 26.0834  
Width : 1.822  
Height : 9.995

Entries	385
Mean	44.06
Std Dev	11.58

ampl



# B1L002S, U2-ch27

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	389
Mean	43.89
Std Dev	11.56

Turn on : 25.0056

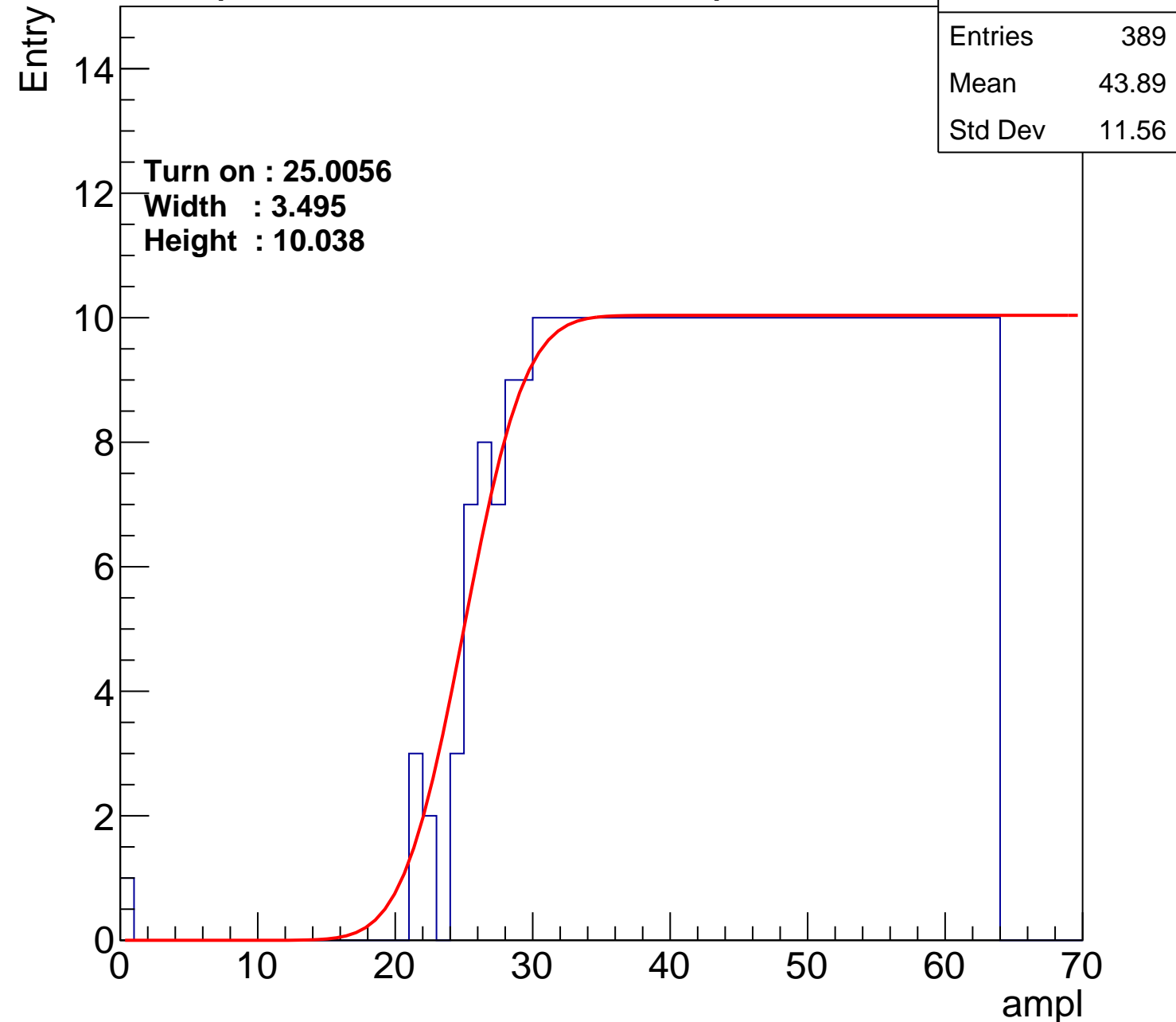
Width : 3.495

Height : 10.038

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch28

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	388
Mean	43.71
Std Dev	12.17

Turn on : 25.8701

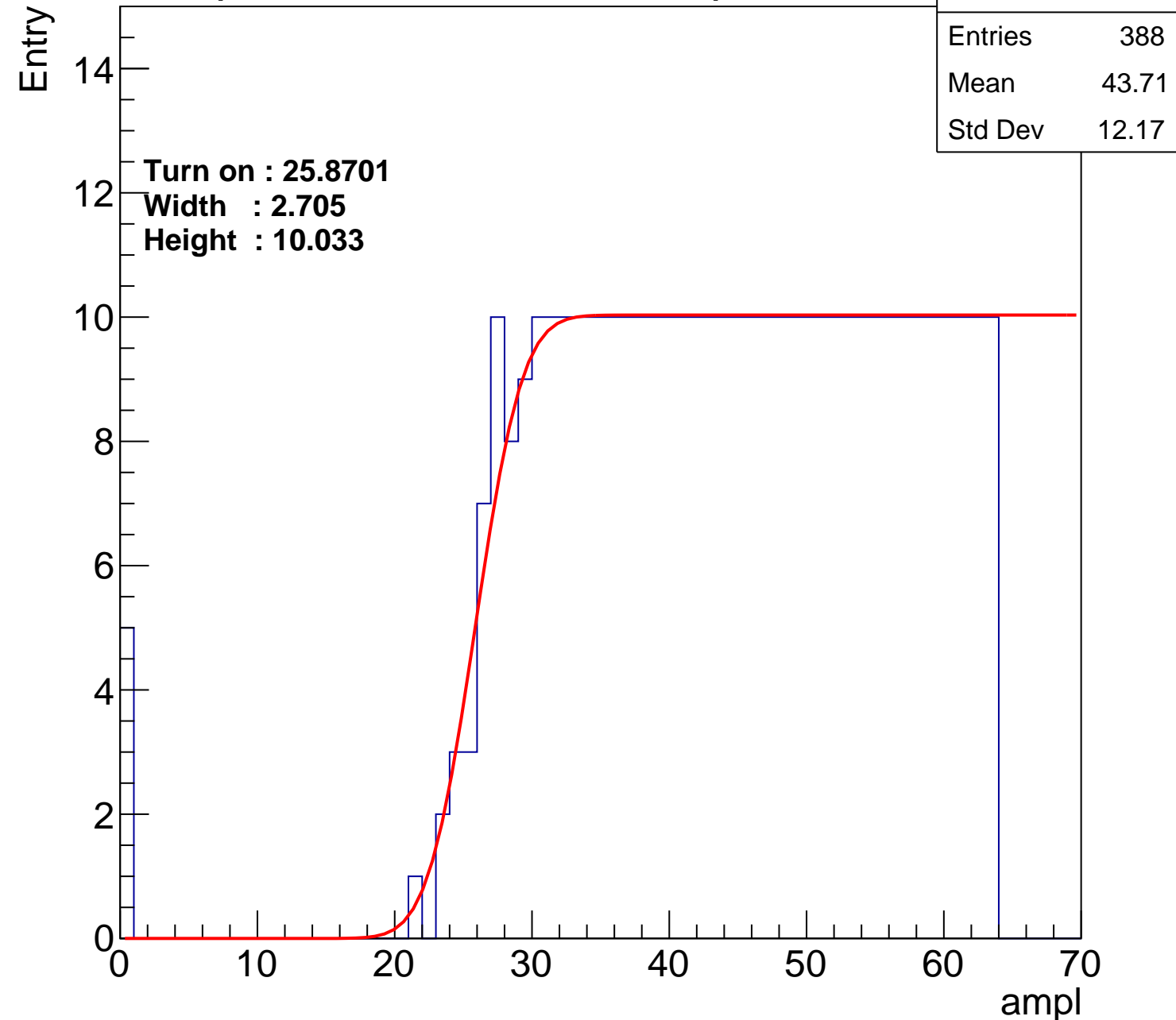
Width : 2.705

Height : 10.033

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch29

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	415
Mean	42.5
Std Dev	12.54

Turn on : 22.6115

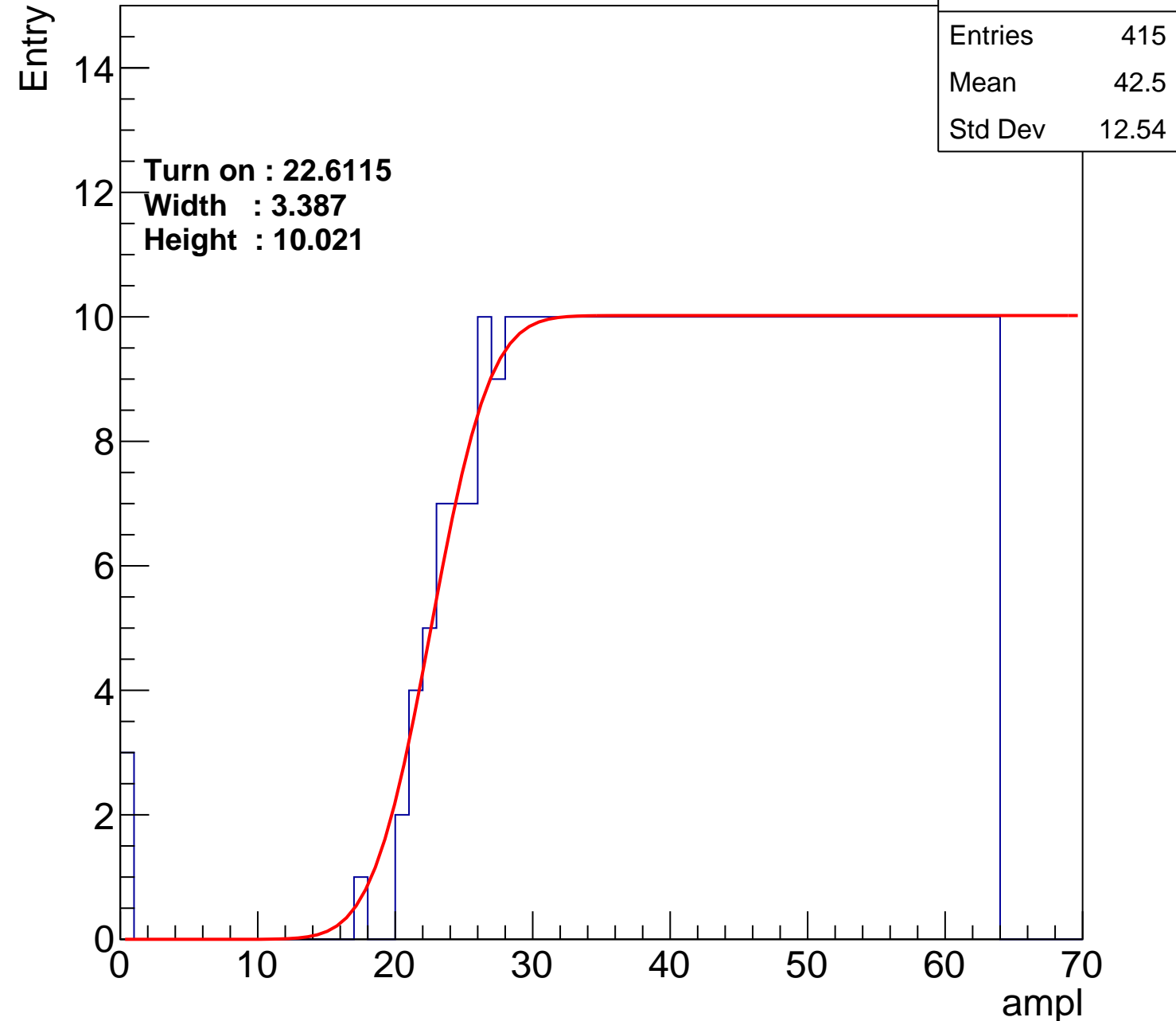
Width : 3.387

Height : 10.021

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch30

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	391
Mean	43.82
Std Dev	11.57

Turn on : 25.0965

Width : 2.326

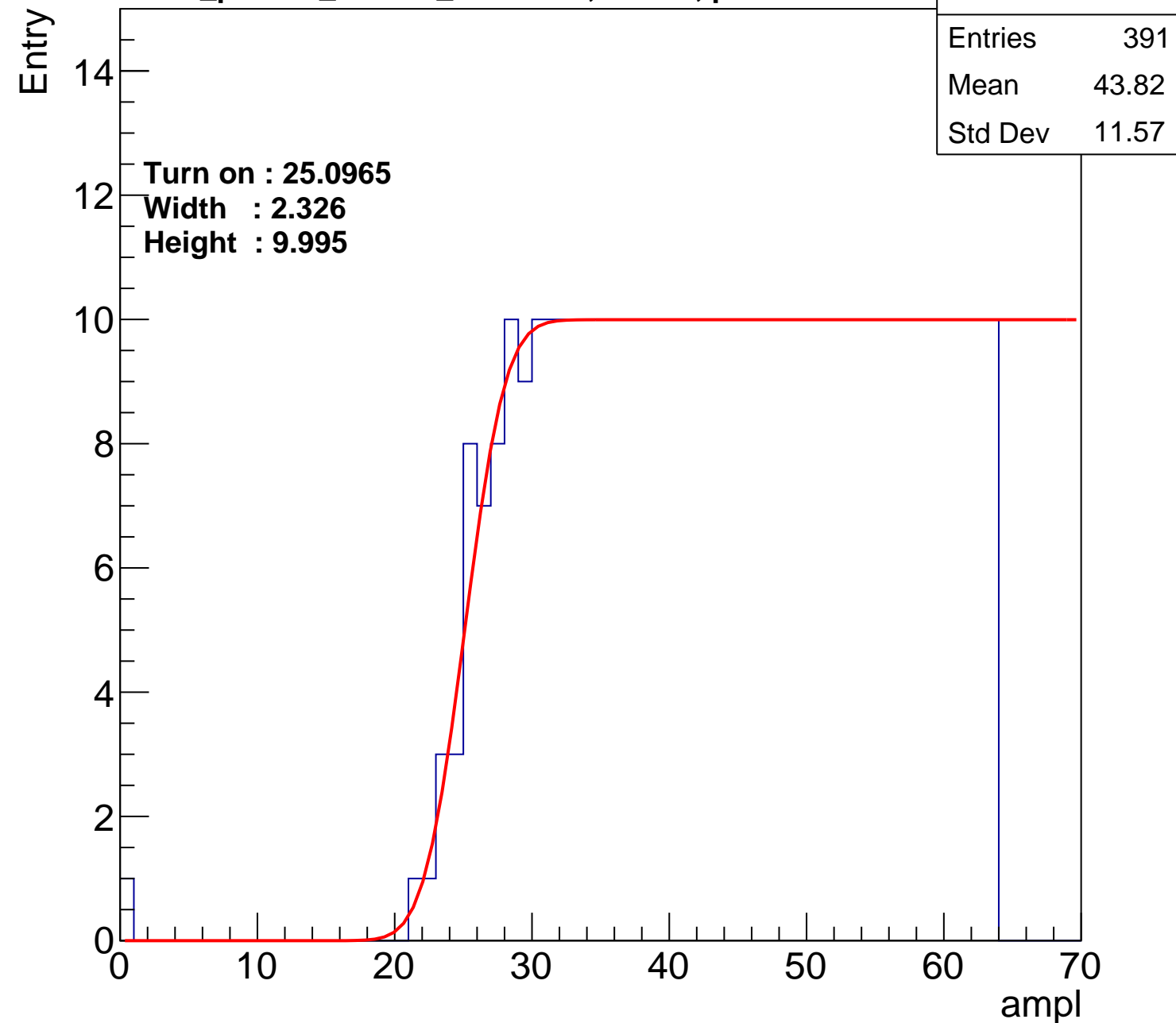
Height : 9.995

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70





# B1L002S, U2-ch31

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	402
Mean	43.15
Std Dev	12.19

Turn on : 24.4618

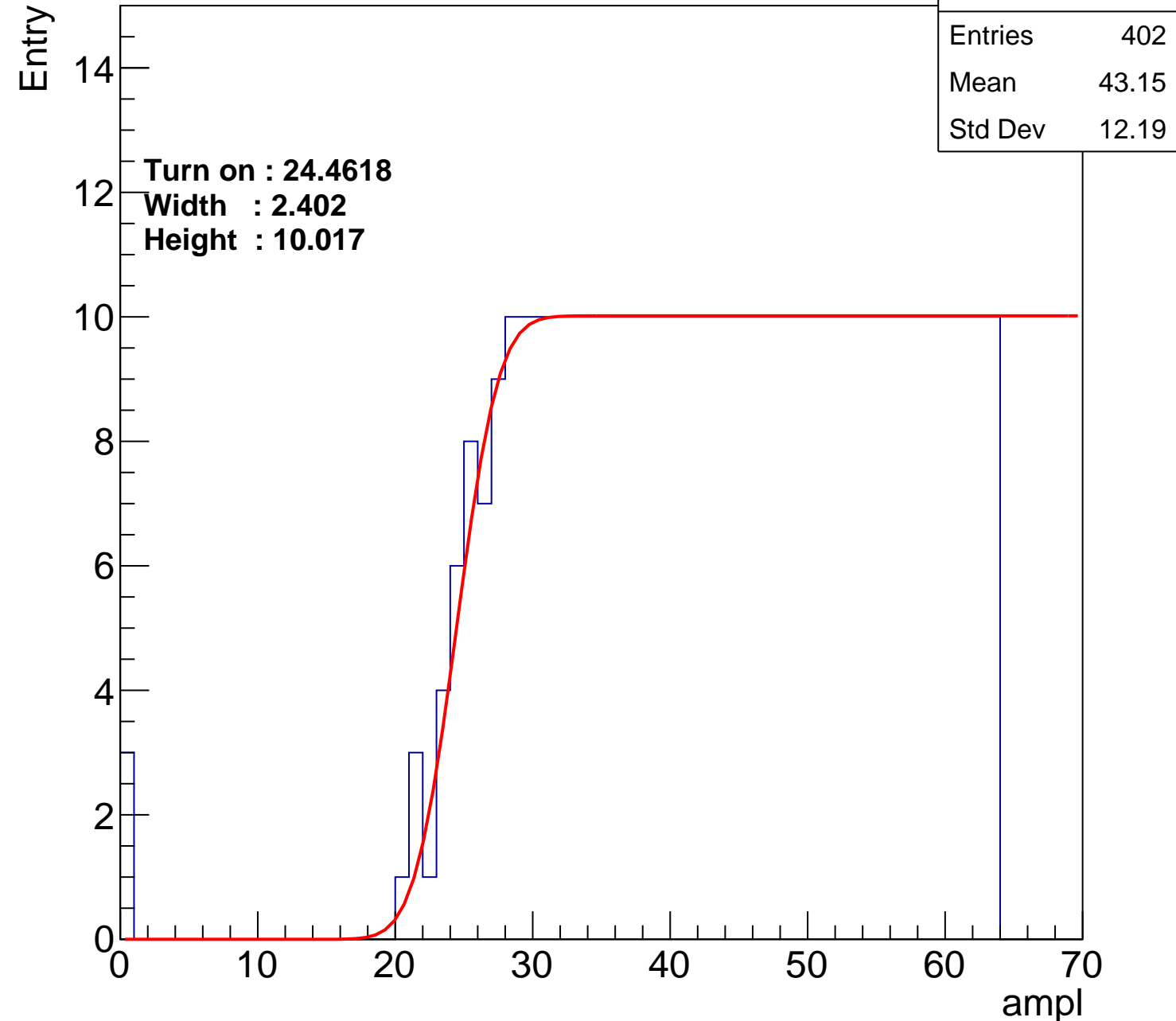
Width : 2.402

Height : 10.017

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch32

**calib\_packv5\_042523\_0143.root, FC#10, port B3**

# Entry

14

12

10

8

6

4

2

0

**Turn on : 25.6934**

**Width : 3.076**

**Height : 10.063**

Entries	390
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Mean	43.79
------	-------

Std Dev	11.75
---------	-------

ampl

# B1L002S, U2-ch33

calib\_packv5\_042523\_0143.root, FC#10, port B3

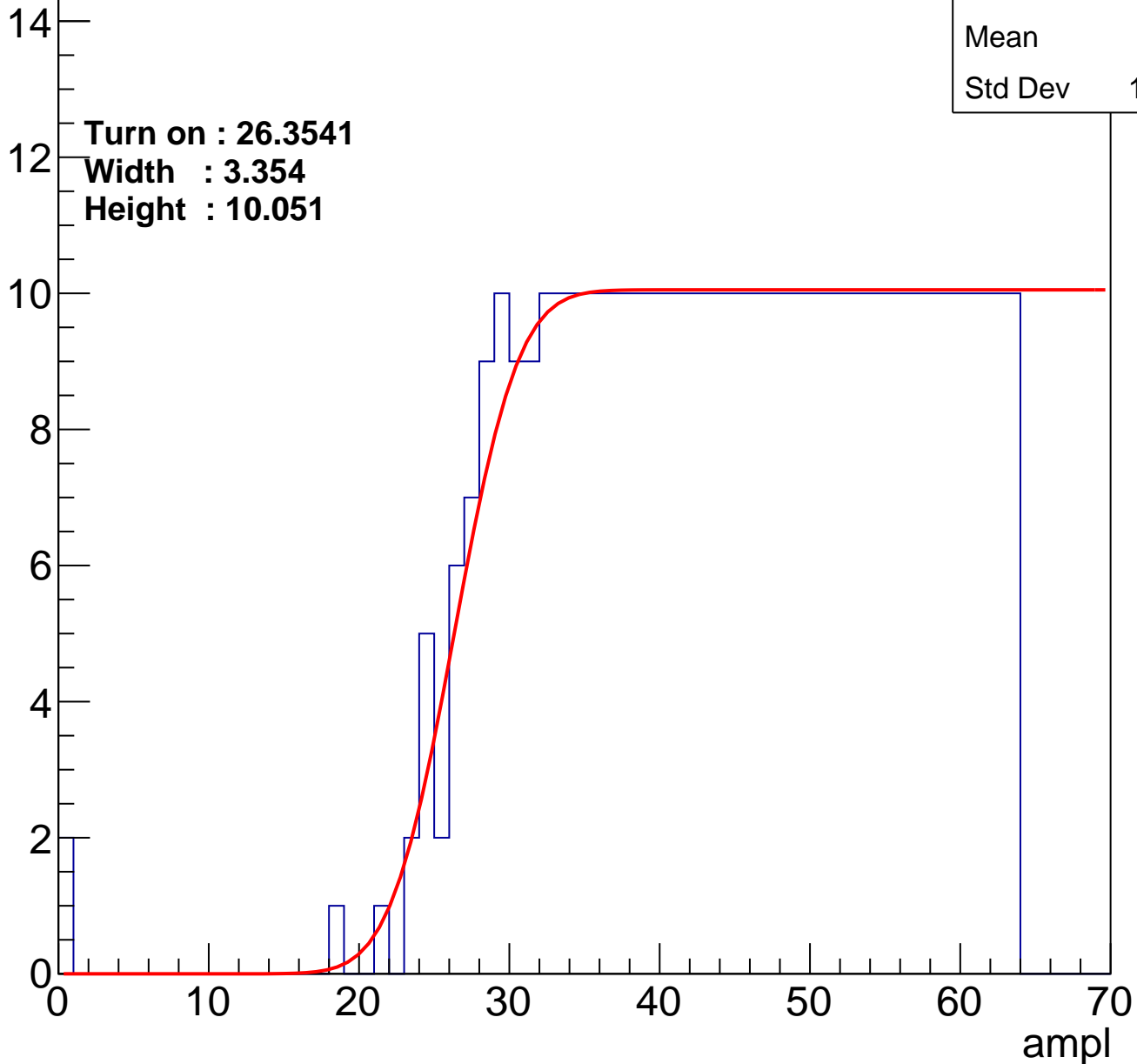
Entries	383
Mean	44.1
Std Dev	11.62

Turn on : 26.3541

Width : 3.354

Height : 10.051

Entry



# B1L002S, U2-ch34

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	392
Mean	43.61
Std Dev	11.99

Turn on : 25.7839

Width : 3.064

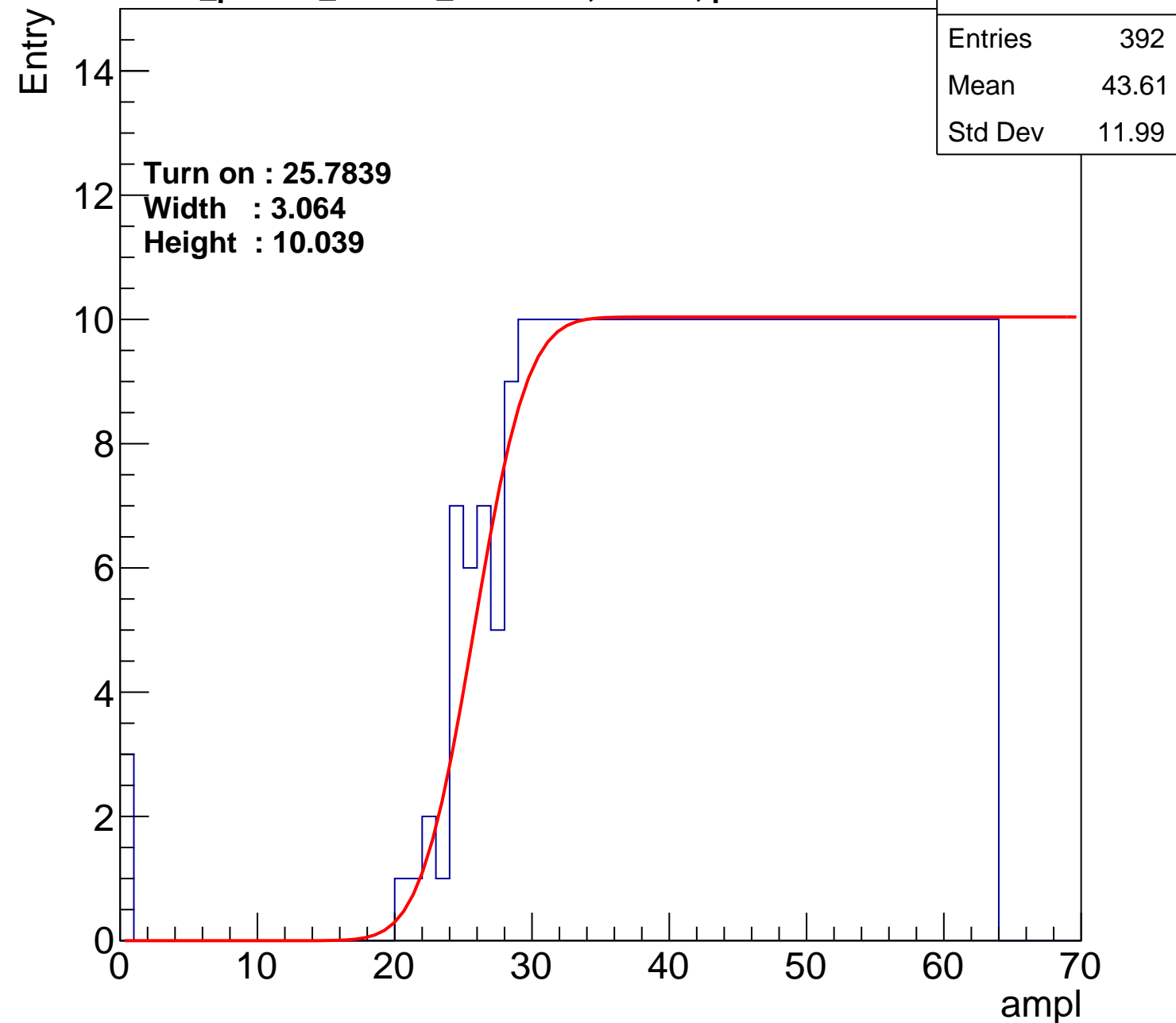
Height : 10.039

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L002S, U2-ch35

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	396
Mean	43.48
Std Dev	11.93

Turn on : 25.0435

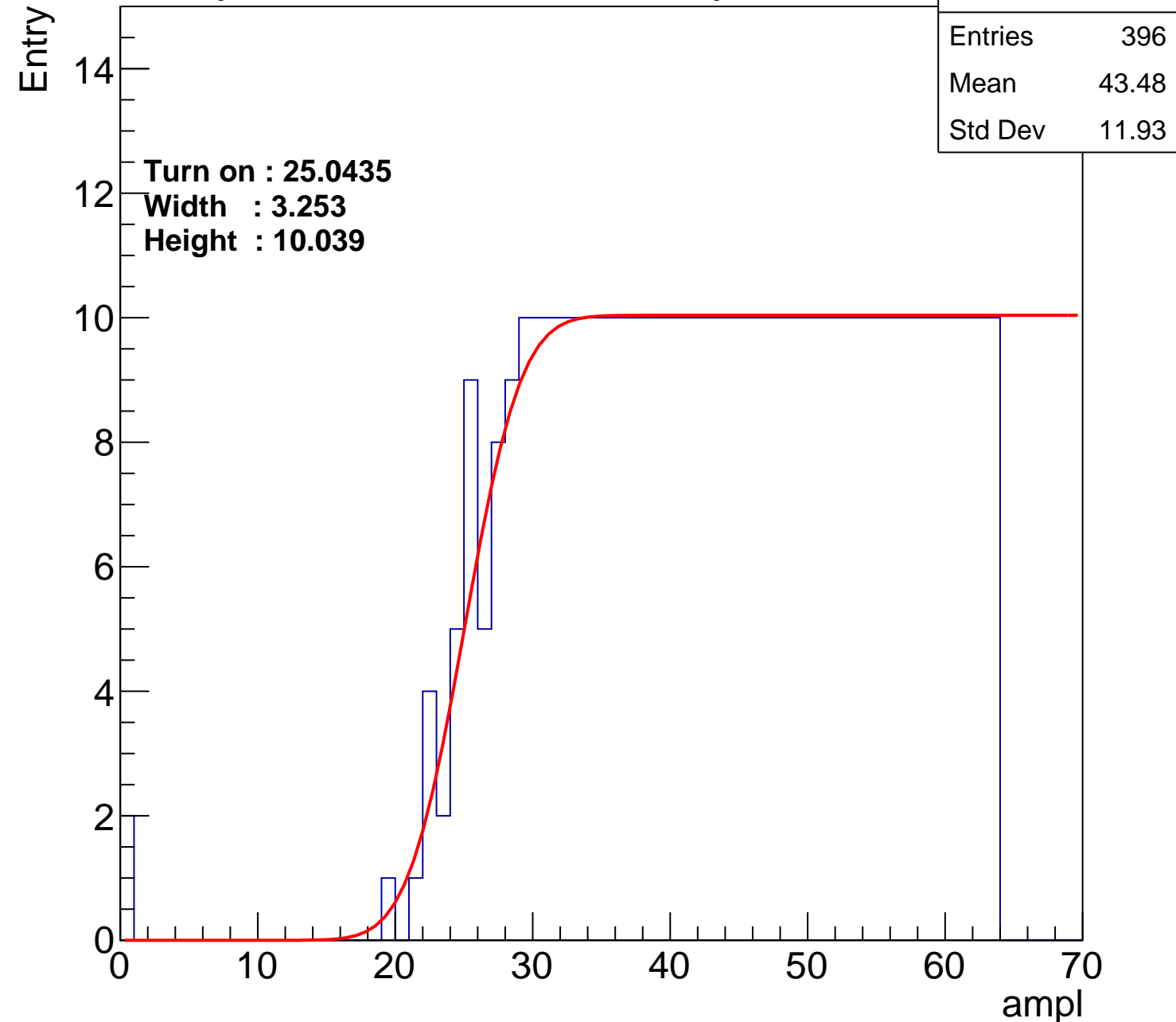
Width : 3.253

Height : 10.039

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch36

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	394
Mean	43.69
Std Dev	11.62

Turn on : 24.8165

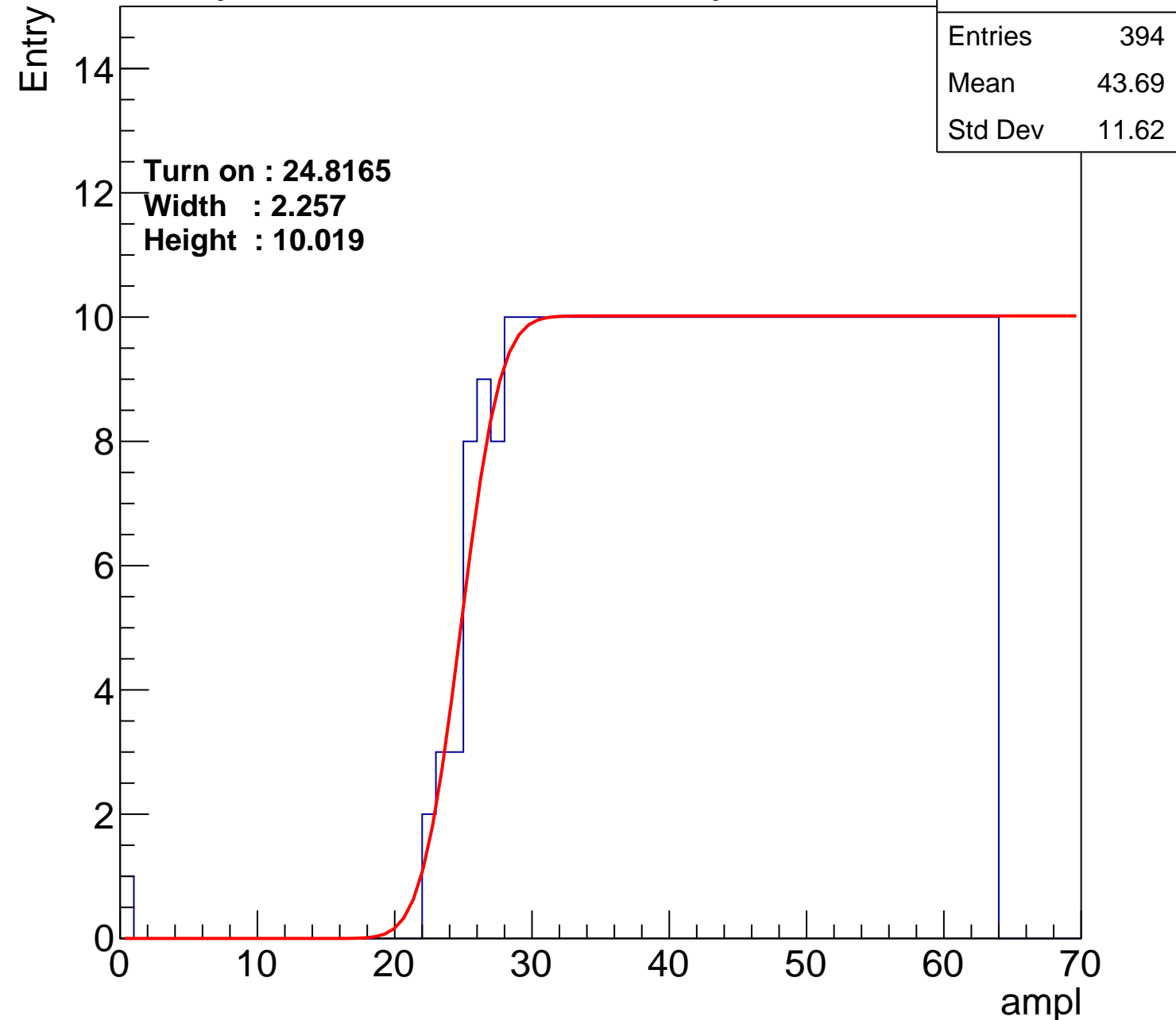
Width : 2.257

Height : 10.019

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch37

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	392
Mean	43.73
Std Dev	11.72

Turn on : 24.6857

Width : 1.357

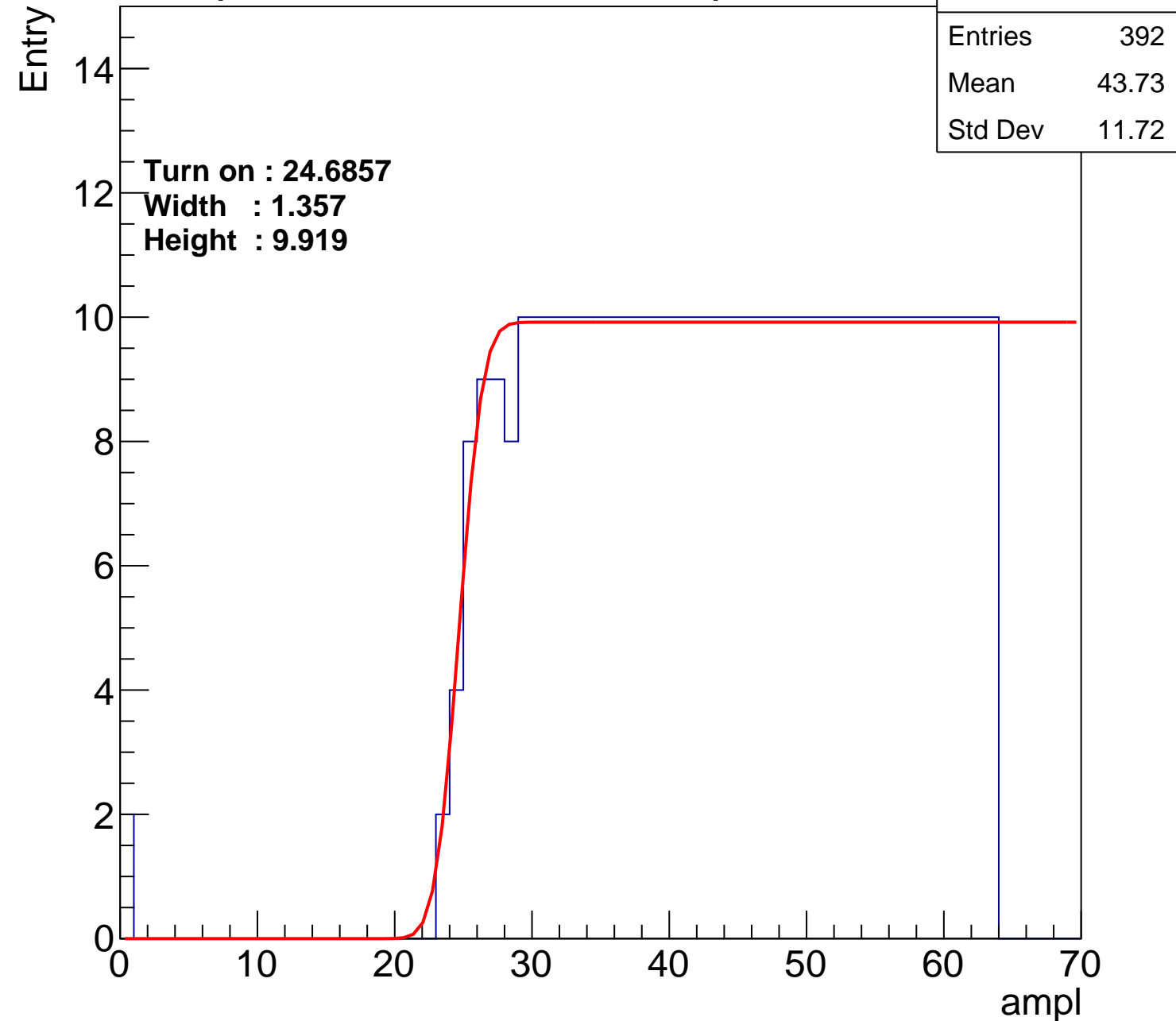
Height : 9.919

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L002S, U2-ch38

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	406
Mean	43.01
Std Dev	12.15

Turn on : 23.7533

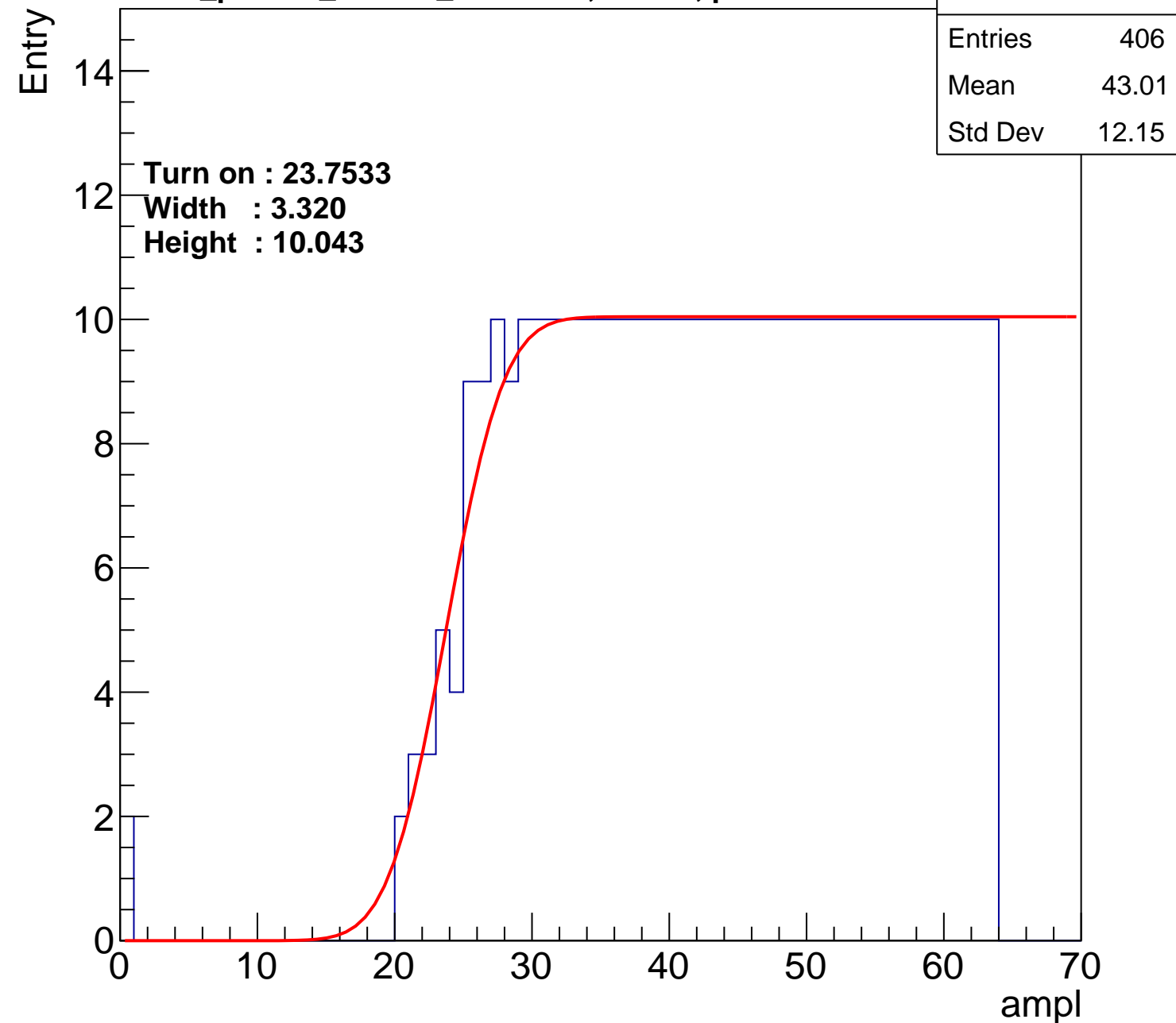
Width : 3.320

Height : 10.043

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L002S, U2-ch39

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	385
Mean	44.03
Std Dev	11.62

Turn on : 25.9697

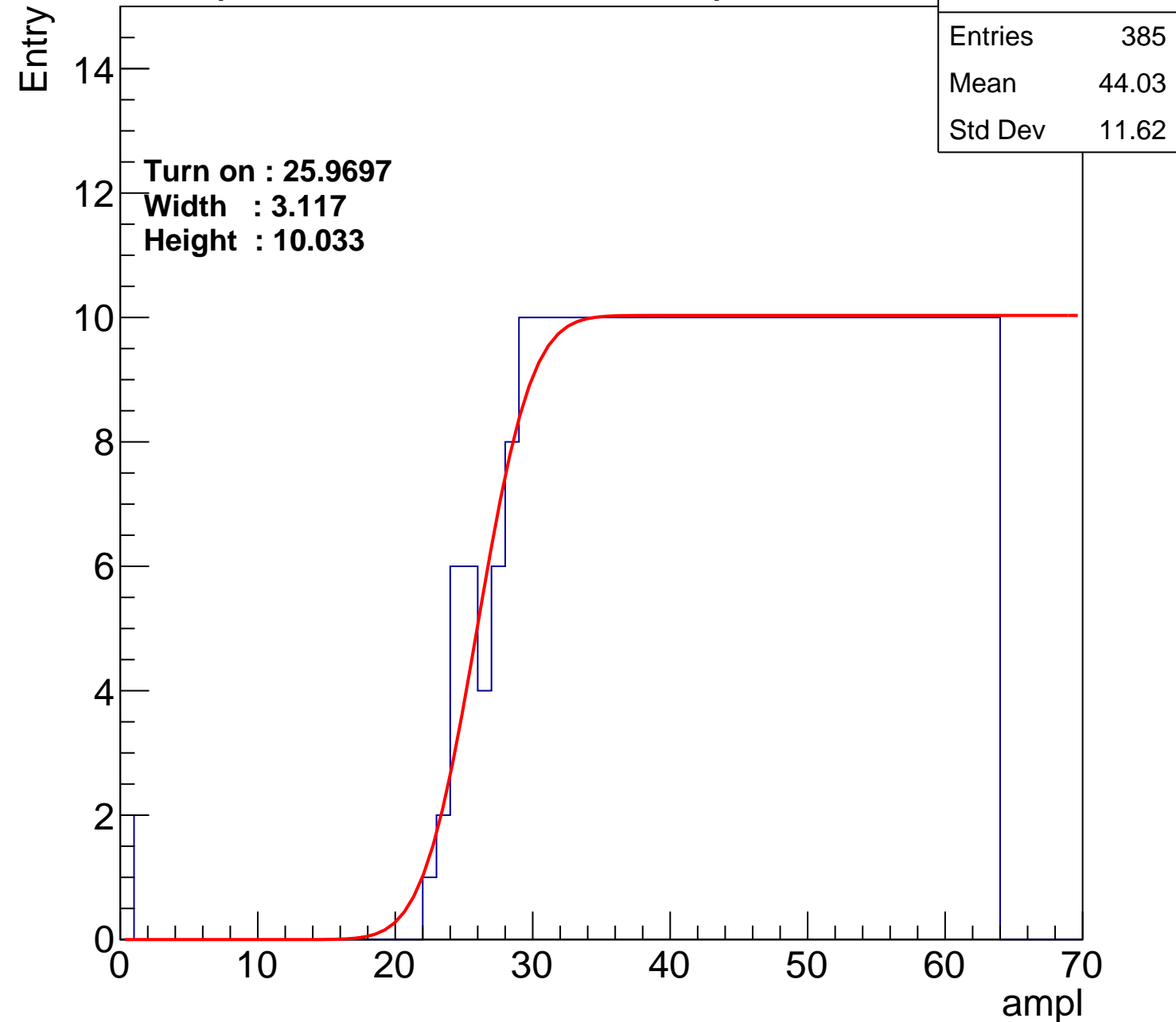
Width : 3.117

Height : 10.033

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch40

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	386
Mean	44.06
Std Dev	11.44

Turn on : 25.6950

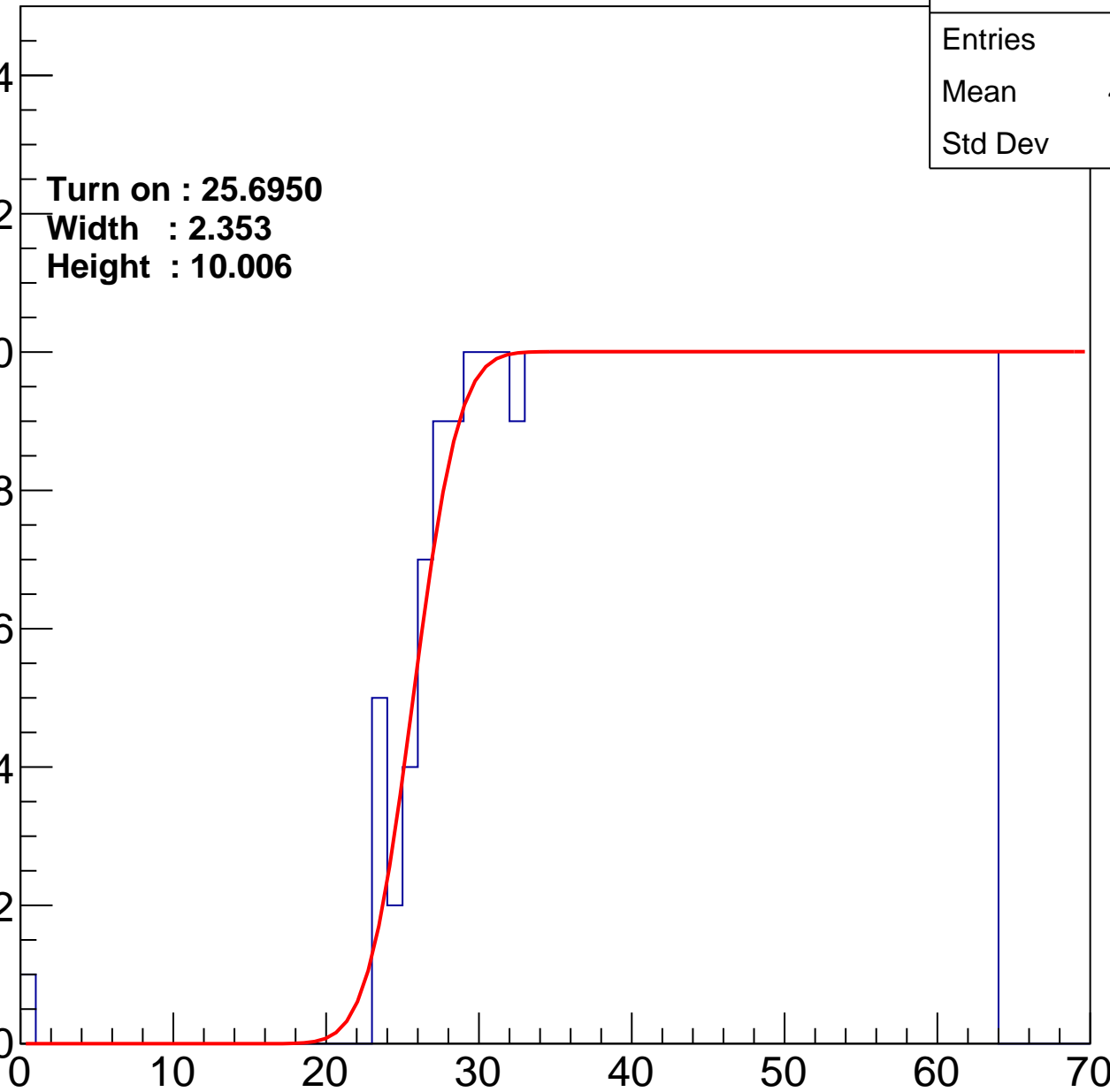
Width : 2.353

Height : 10.006

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch41

calib\_packv5\_042523\_0143.root, FC#10, port B3

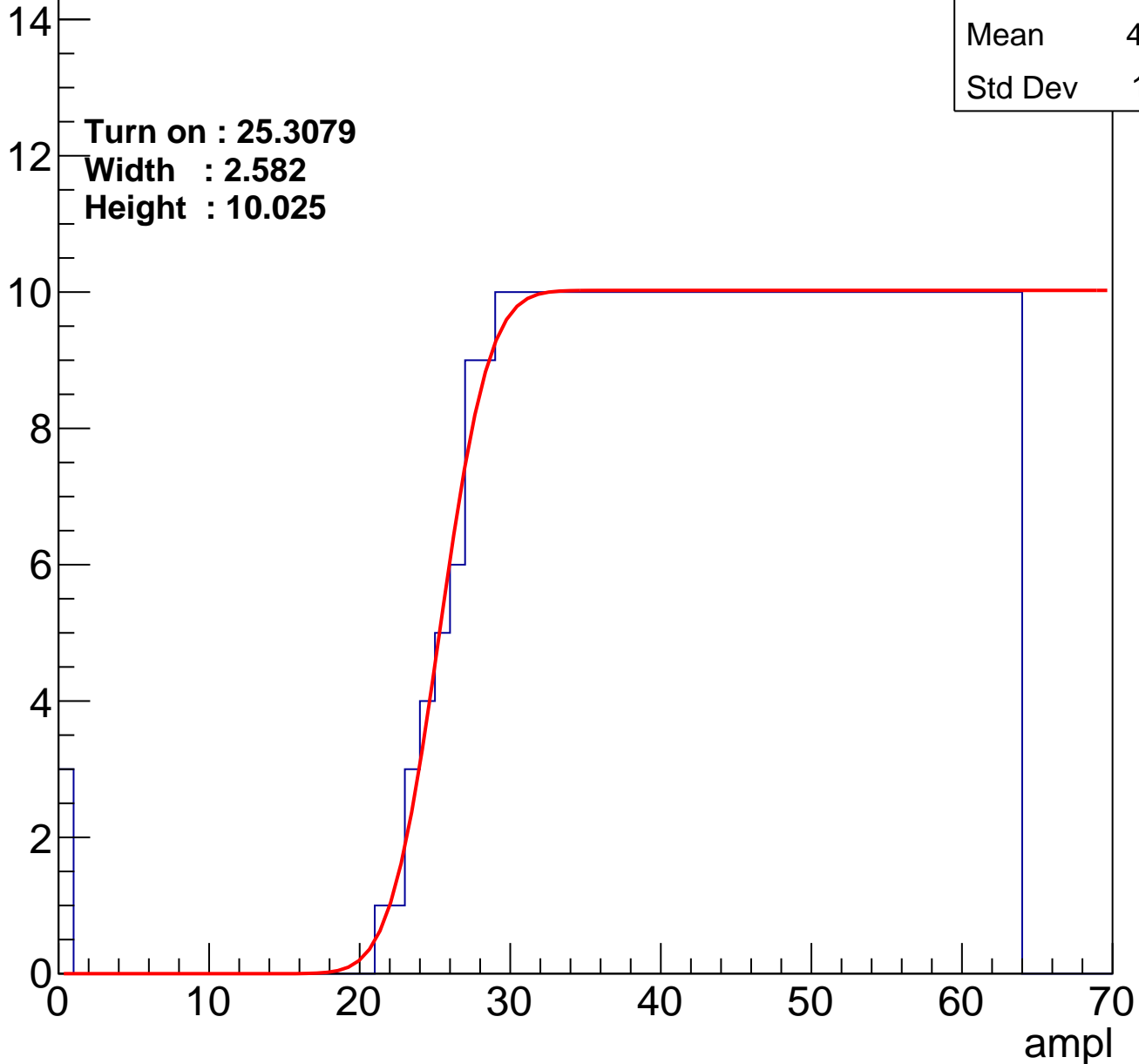
Entries	391
Mean	43.69
Std Dev	11.91

Turn on : 25.3079

Width : 2.582

Height : 10.025

Entry



# B1L002S, U2-ch42

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	387
Mean	43.93
Std Dev	11.68

Turn on : 26.3258

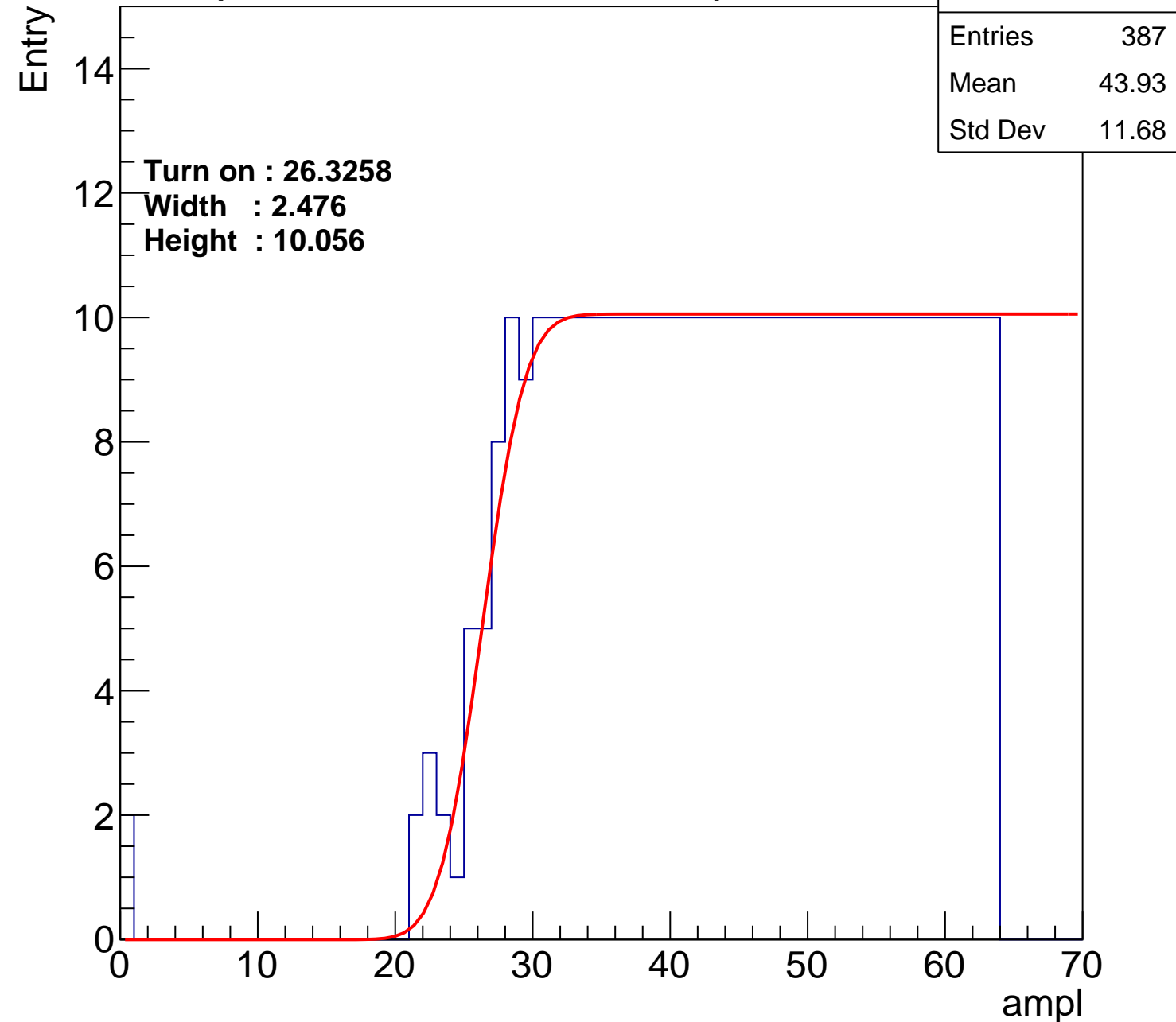
Width : 2.476

Height : 10.056

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch43

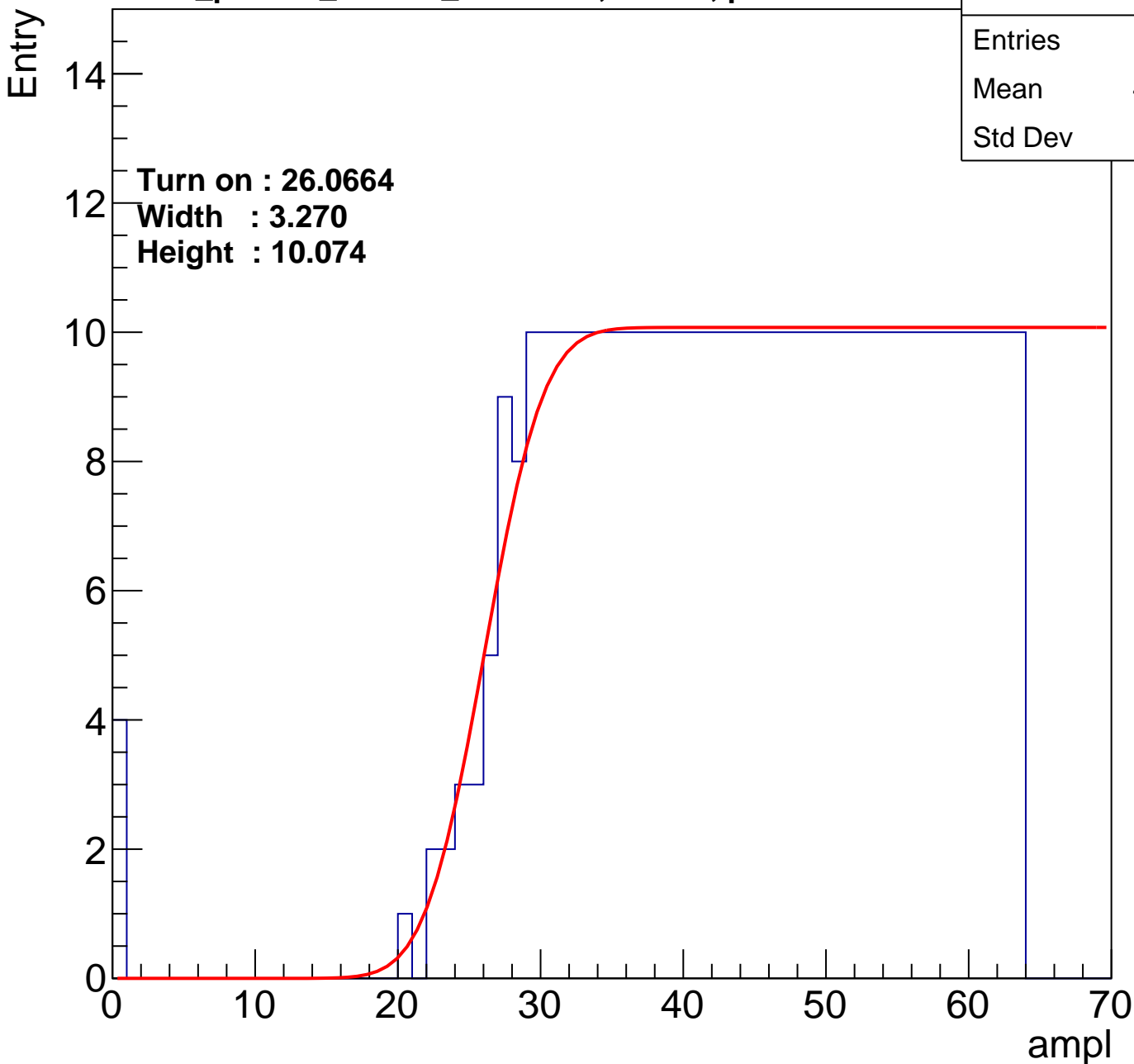
**calib\_packv5\_042523\_0143.root, FC#10, port B3**

**Turn on : 26.0664**

**Width : 3.270**

**Height : 10.074**

Entries	387
Mean	43.81
Std Dev	12.01



# B1L002S, U2-ch44

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	384
Mean	44.02
Std Dev	11.76

Turn on : 26.0320

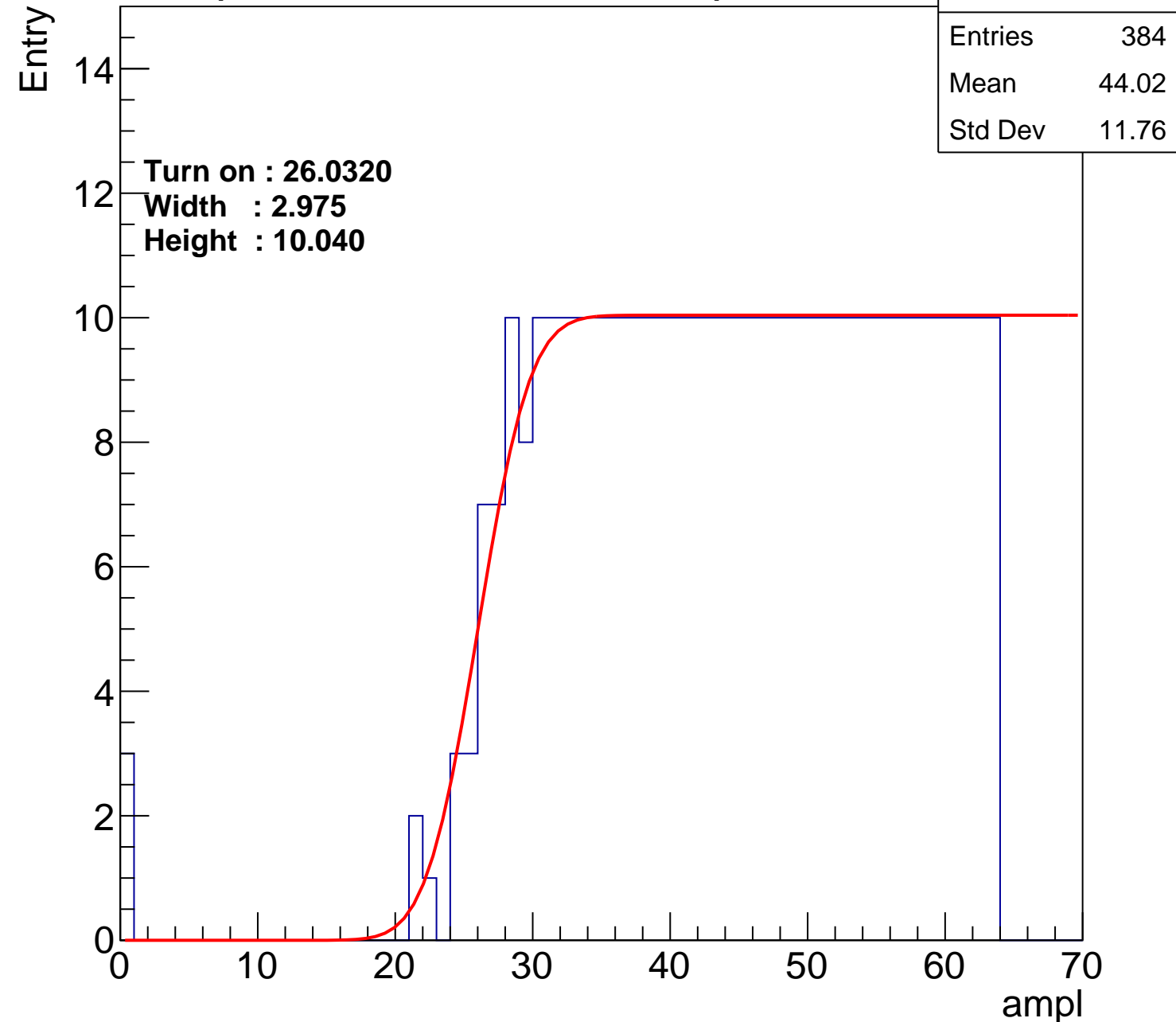
Width : 2.975

Height : 10.040

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch45

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	388
Mean	43.9
Std Dev	11.67

Turn on : 25.7550

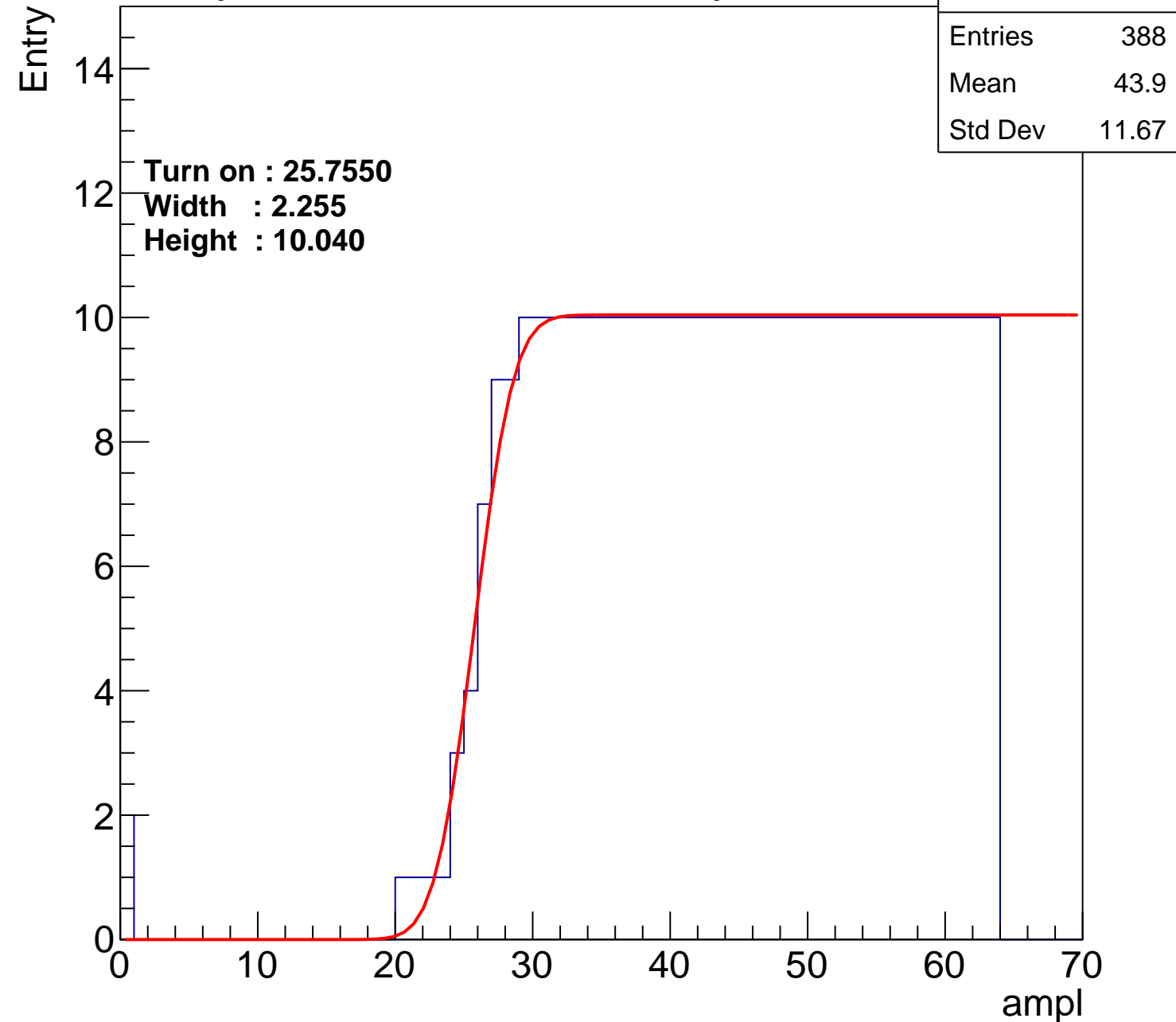
Width : 2.255

Height : 10.040

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch46

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	383
Mean	43.96
Std Dev	11.99

Turn on : 26.5299

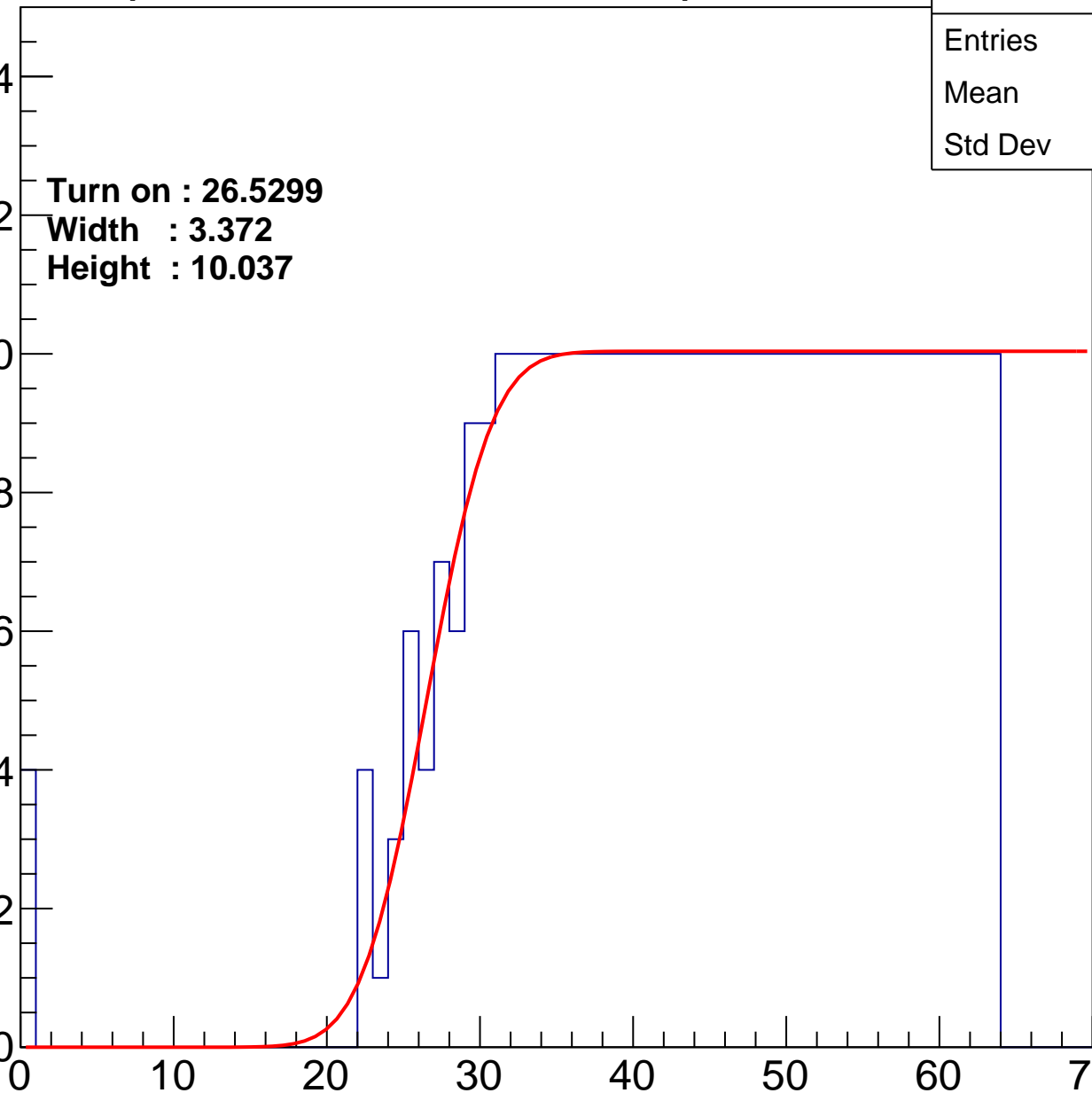
Width : 3.372

Height : 10.037

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L002S, U2-ch47

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	389
Mean	43.88
Std Dev	11.65

Turn on : 25.6259

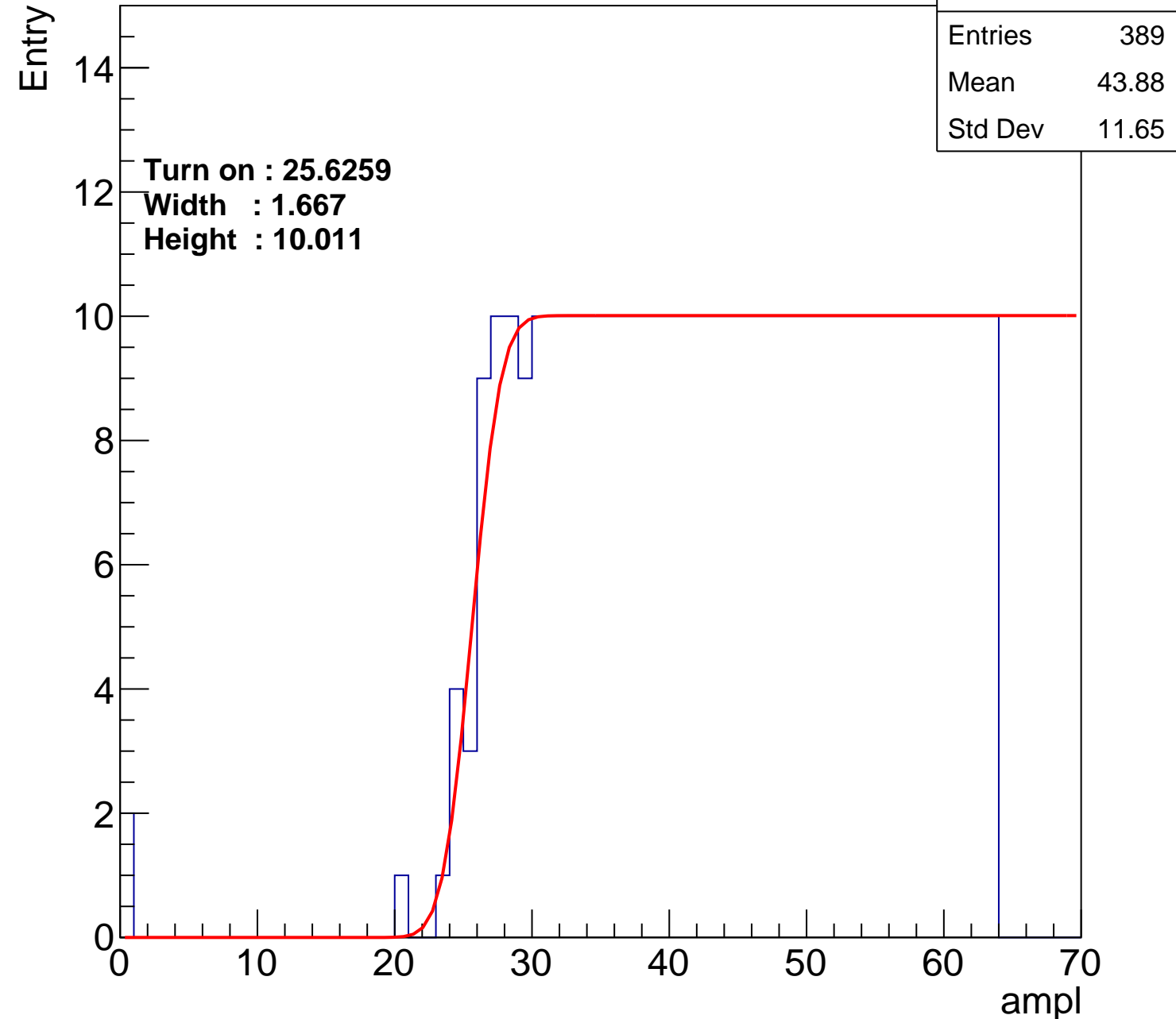
Width : 1.667

Height : 10.011

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch48

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	402
Mean	43.25
Std Dev	11.91

Turn on : 24.3018

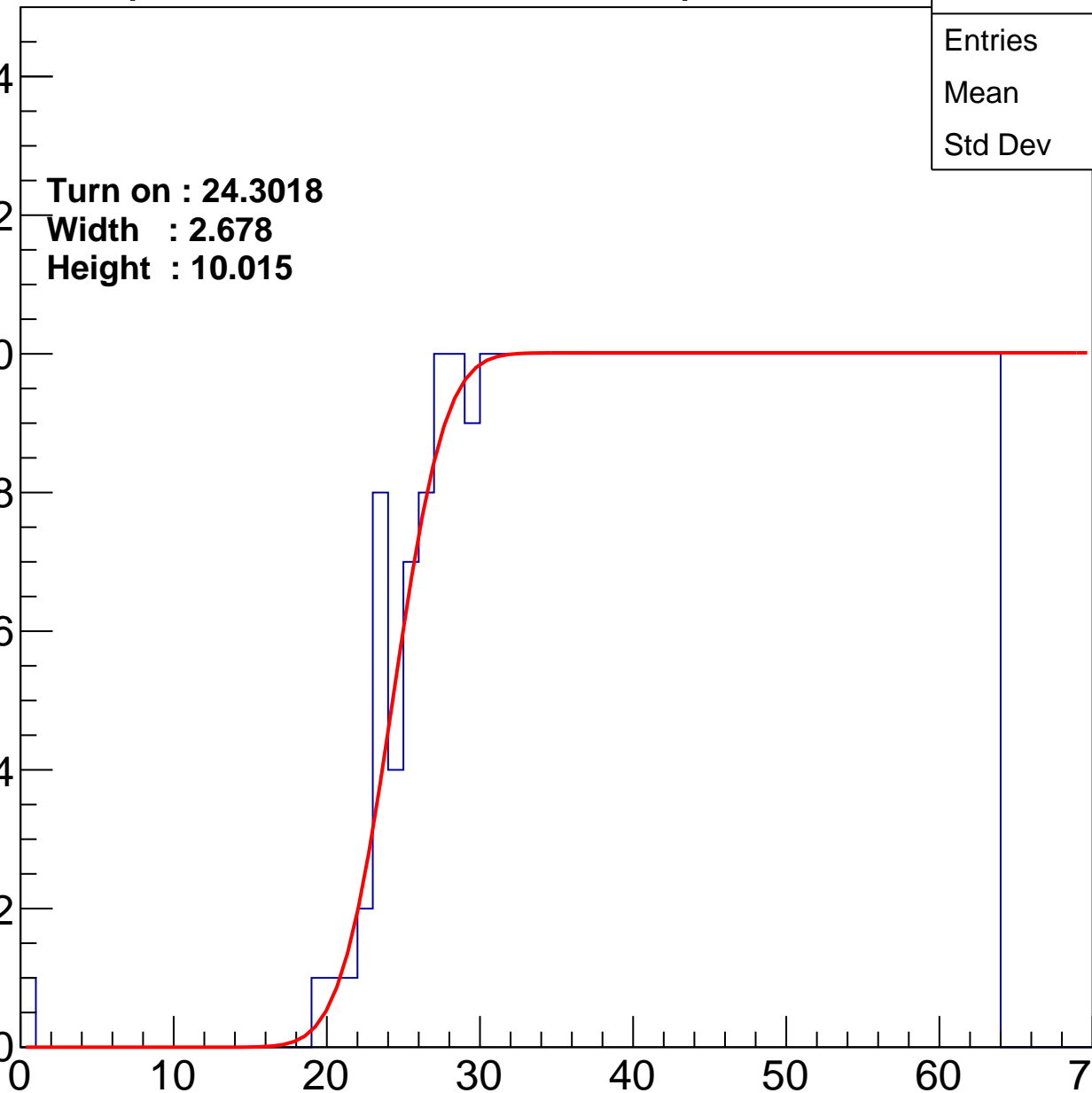
Width : 2.678

Height : 10.015

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch49

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	403
Mean	43.05
Std Dev	12.34

Turn on : 24.1218

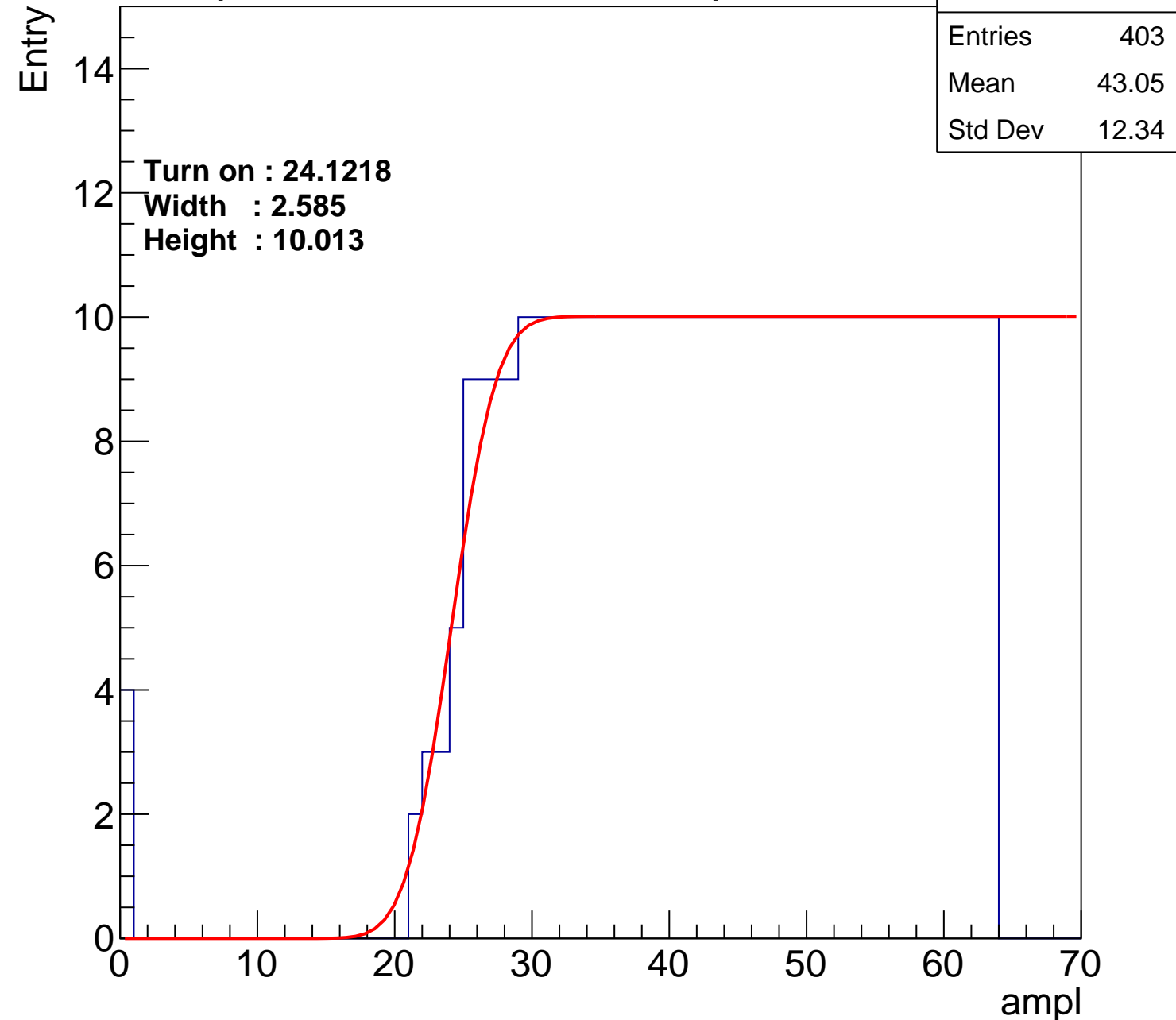
Width : 2.585

Height : 10.013

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch50

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	377
Mean	44.37
Std Dev	11.58

**Turn on : 26.8019**

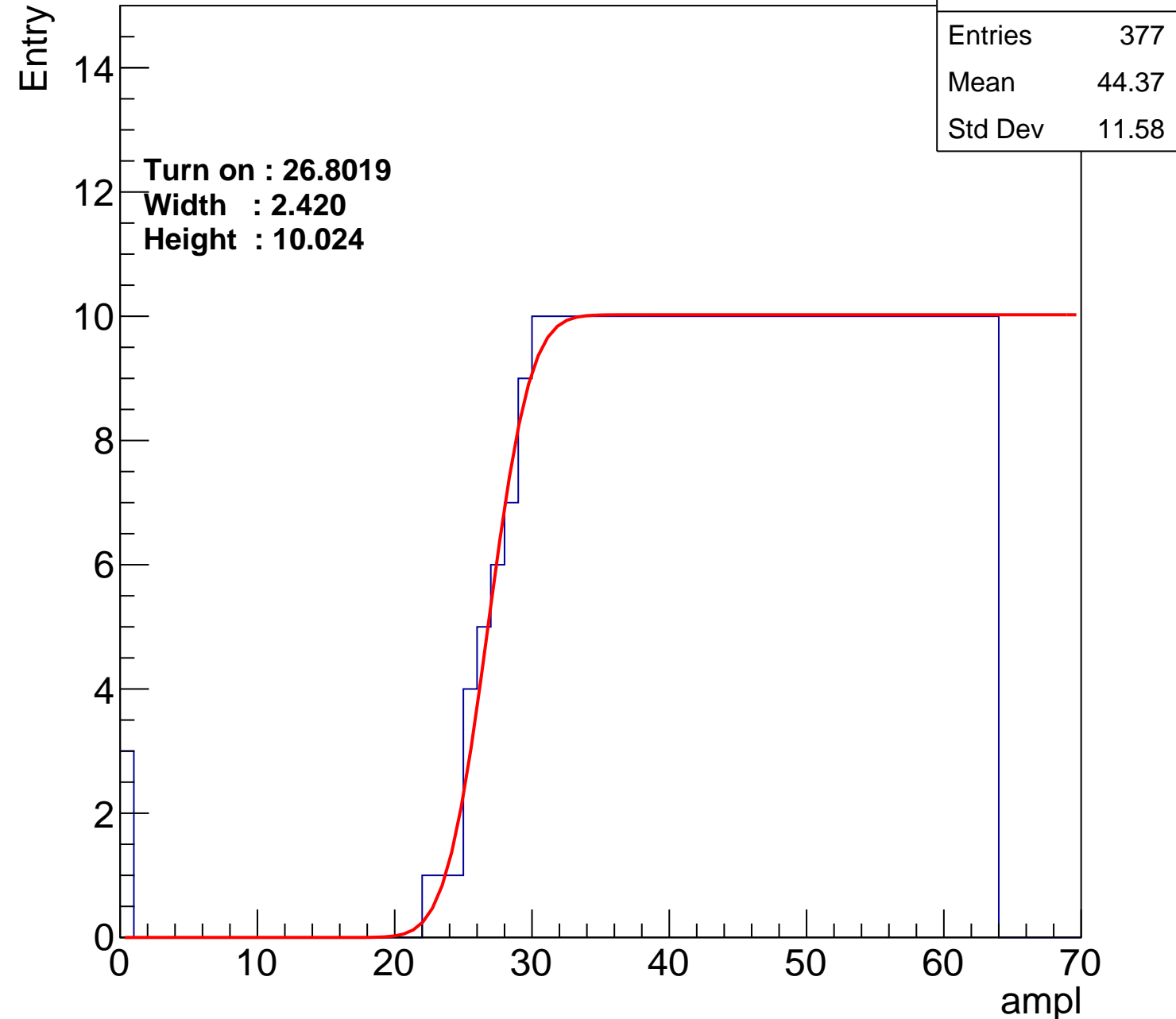
**Width : 2.420**

**Height : 10.024**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch51

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	386
Mean	43.98
Std Dev	11.64

Turn on : 26.5634

Width : 3.886

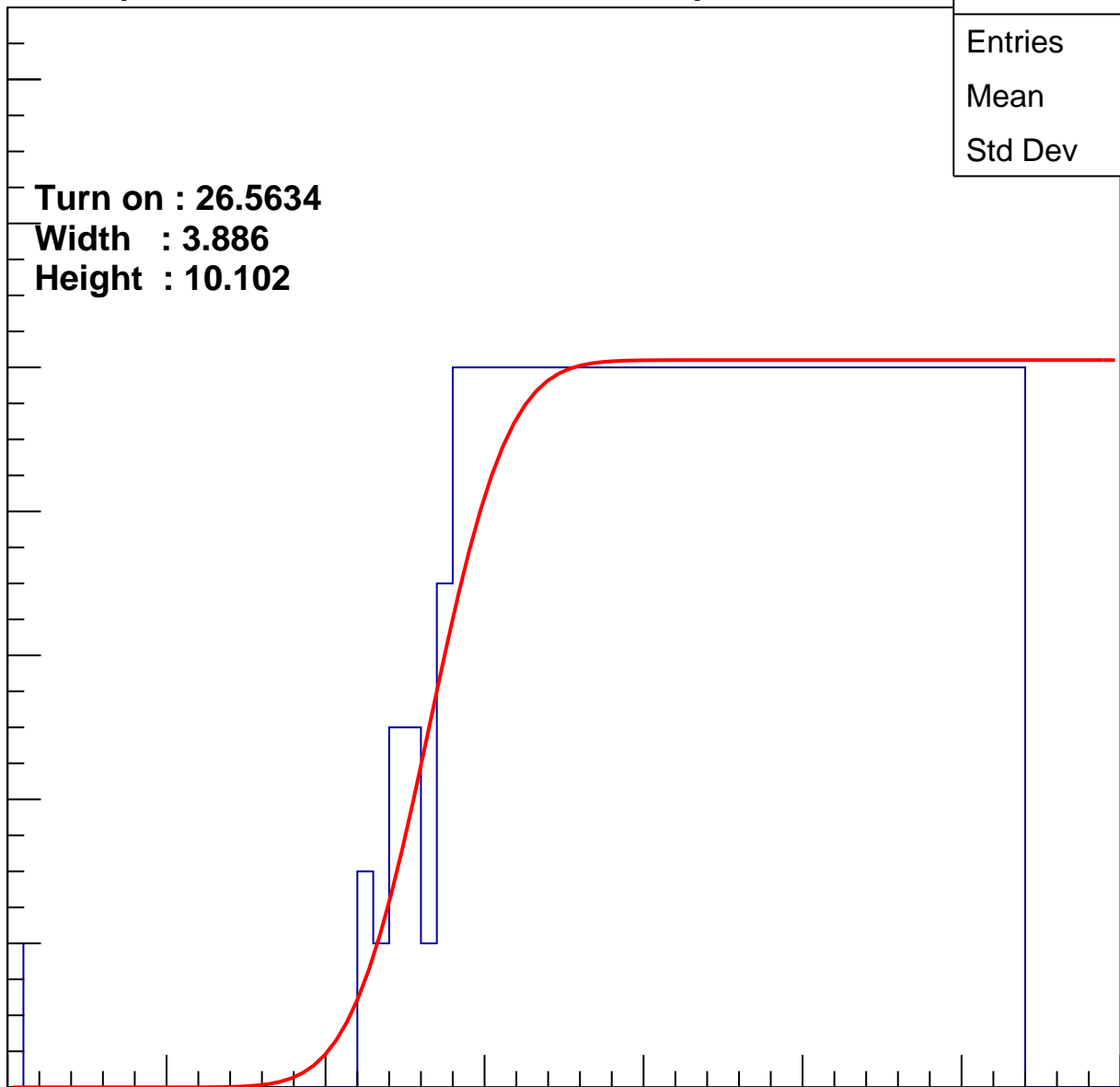
Height : 10.102

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L002S, U2-ch52

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	398
Mean	43.48
Std Dev	11.75

Turn on : 24.5271

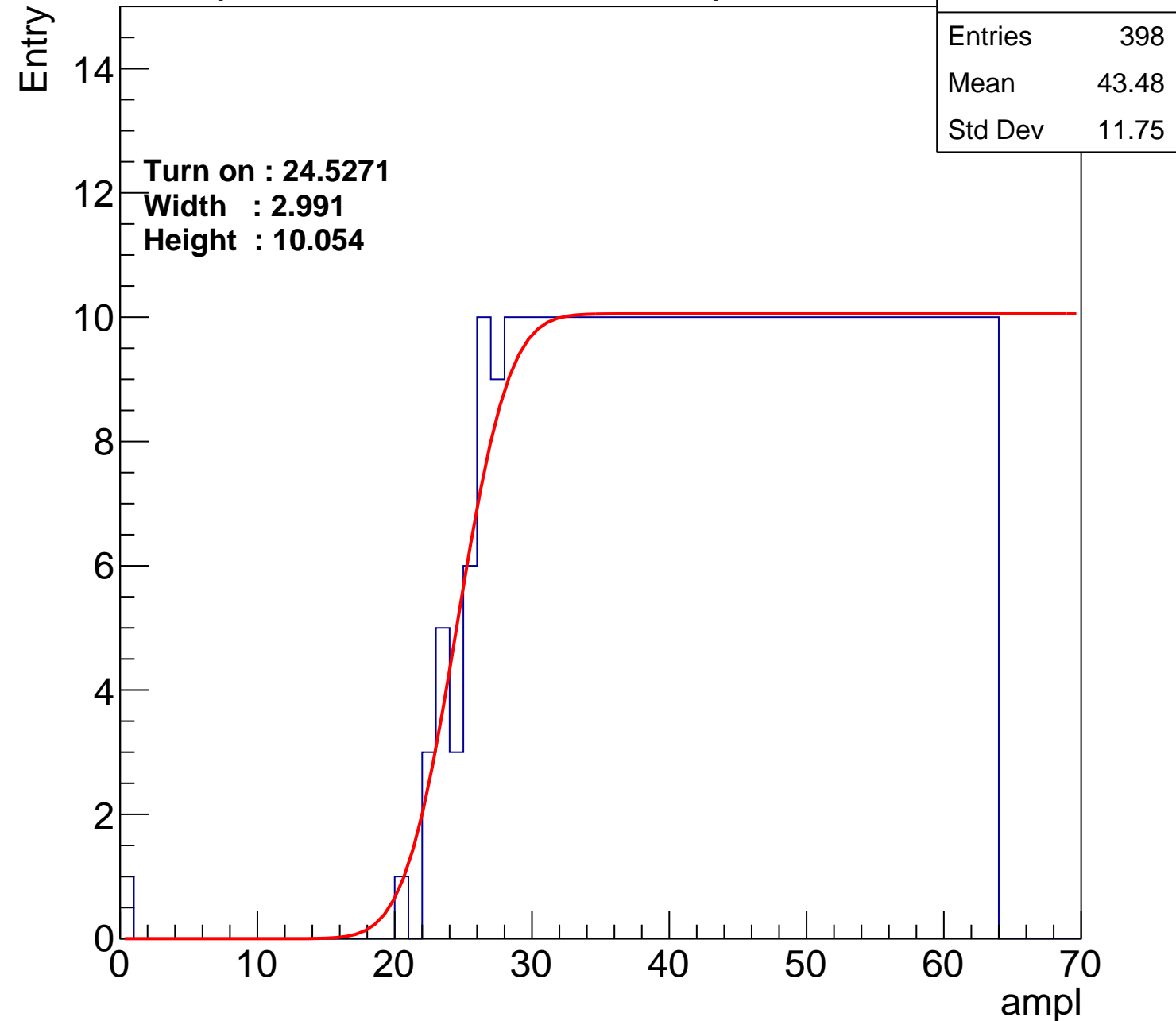
Width : 2.991

Height : 10.054

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch53

calib\_packv5\_042523\_0143.root, FC#10, port B3

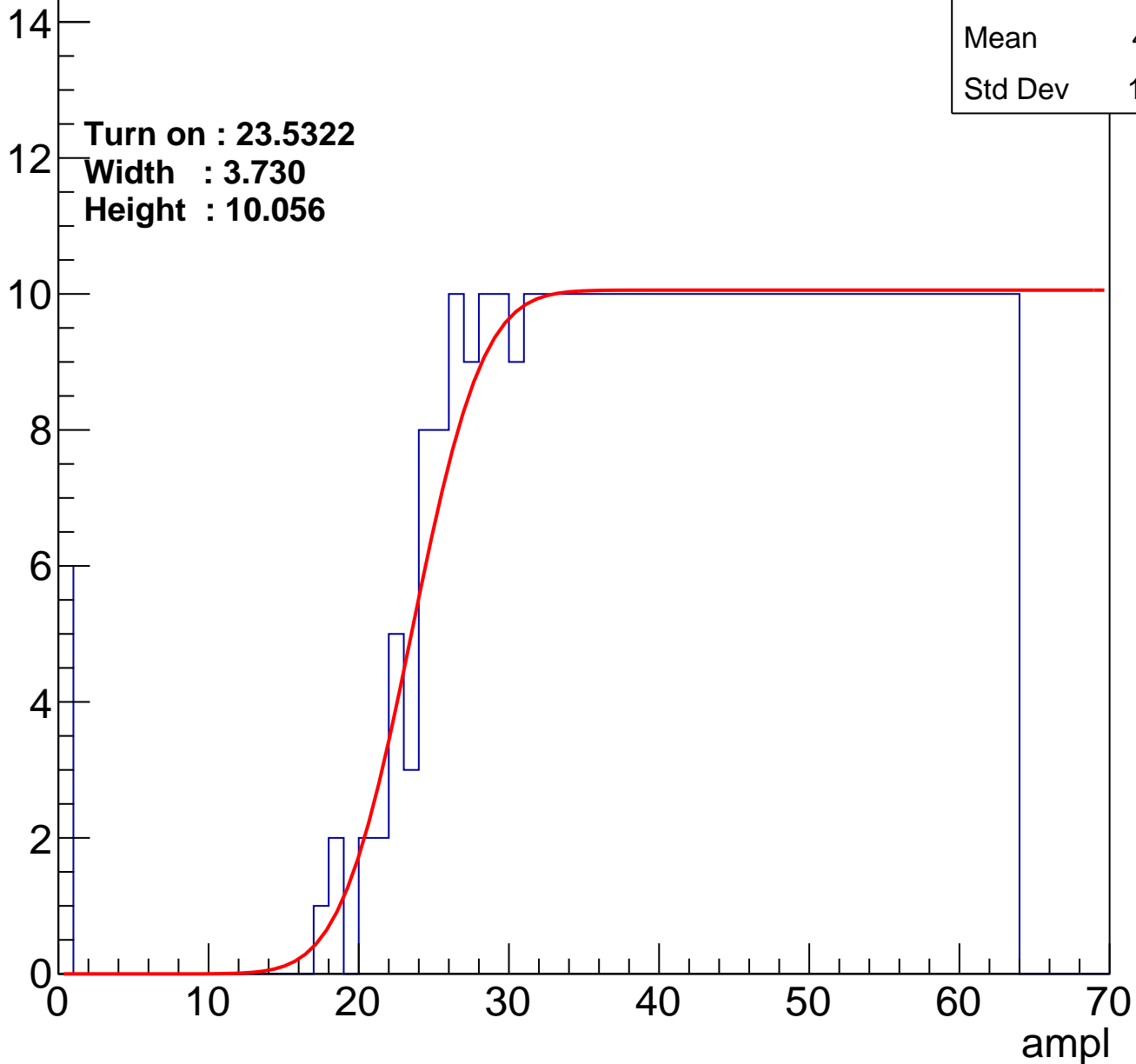
Entries	415
Mean	42.31
Std Dev	12.97

Turn on : 23.5322

Width : 3.730

Height : 10.056

Entry



# B1L002S, U2-ch54

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	396
Mean	43.47
Std Dev	11.99

Turn on : 24.5926

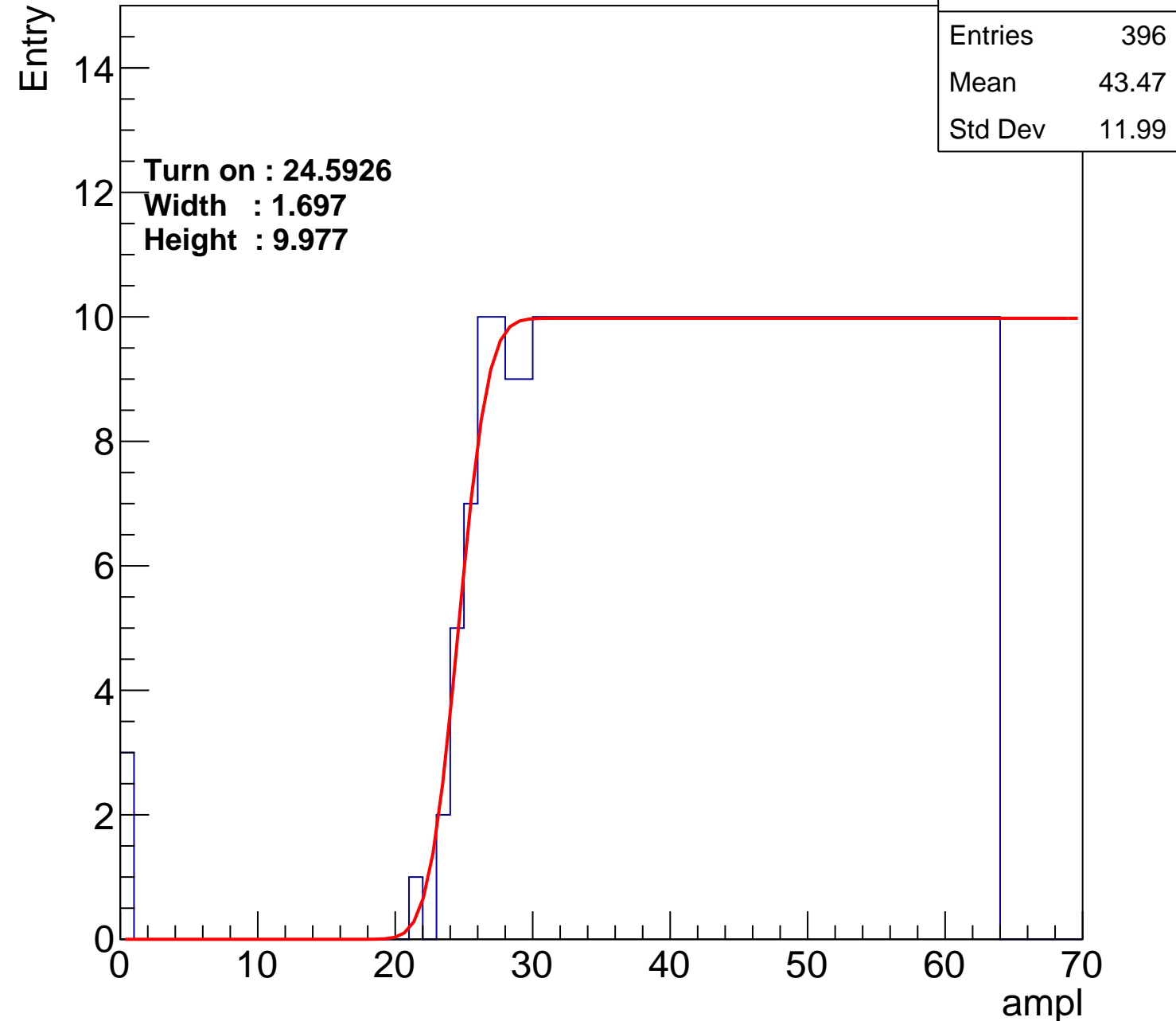
Width : 1.697

Height : 9.977

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L002S, U2-ch55

calib\_packv5\_042523\_0143.root, FC#10, port B3

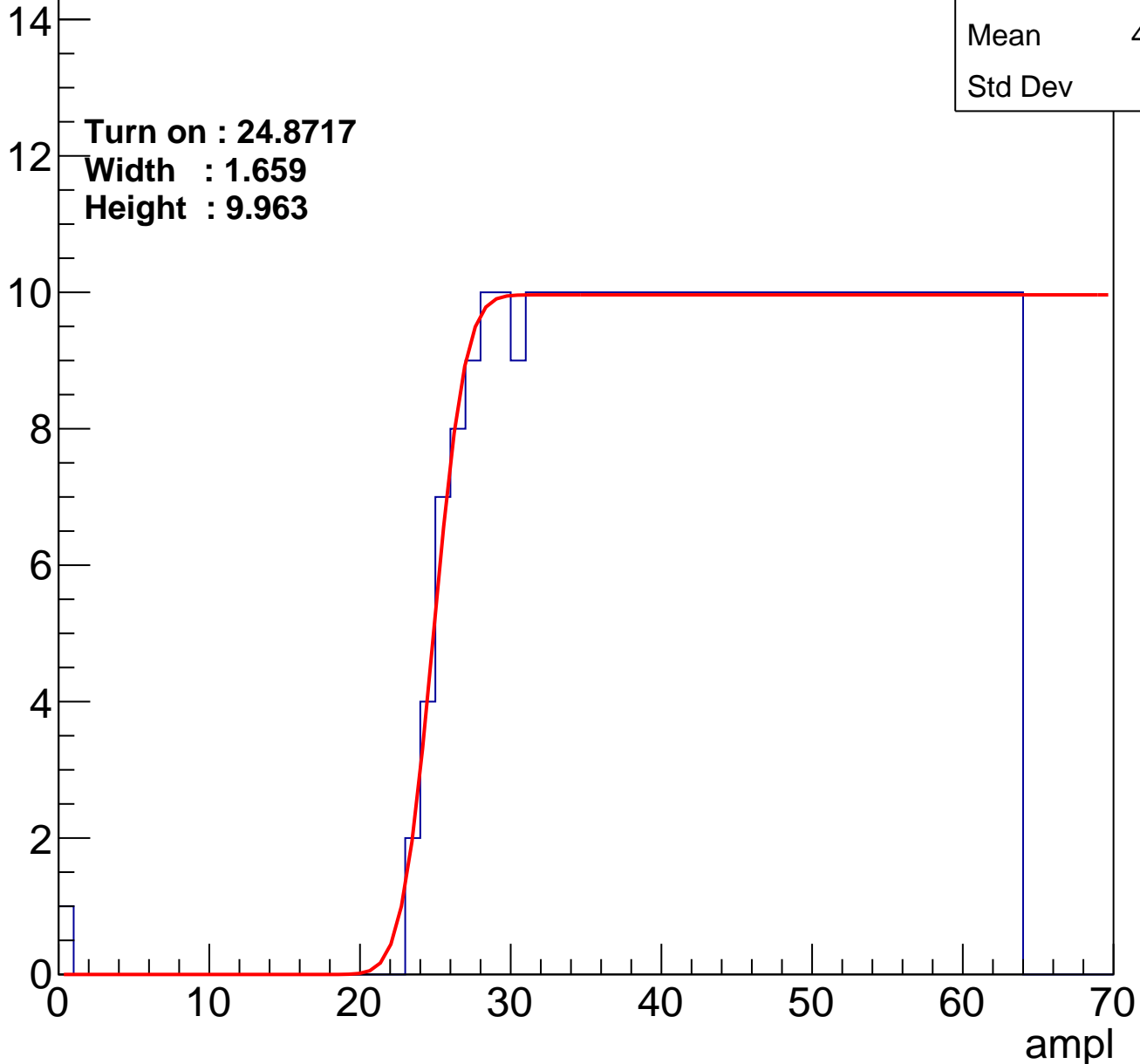
Entries	390
Mean	43.89
Std Dev	11.5

Turn on : 24.8717

Width : 1.659

Height : 9.963

Entry



# B1L002S, U2-ch56

calib\_packv5\_042523\_0143.root, FC#10, port B3

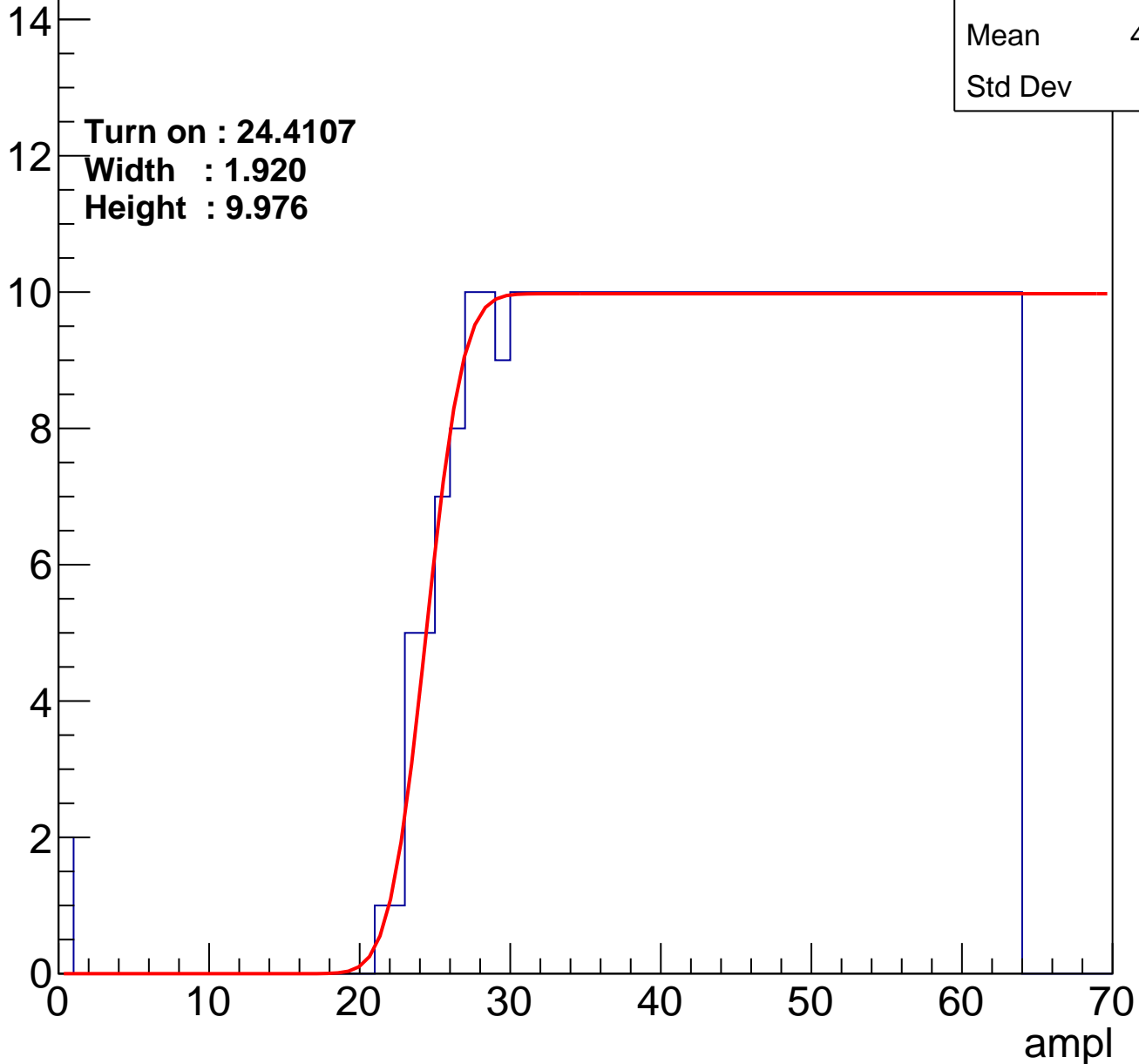
Entries	398
Mean	43.42
Std Dev	11.9

**Turn on : 24.4107**

**Width : 1.920**

**Height : 9.976**

Entry



# B1L002S, U2-ch57

calib\_packv5\_042523\_0143.root, FC#10, port B3

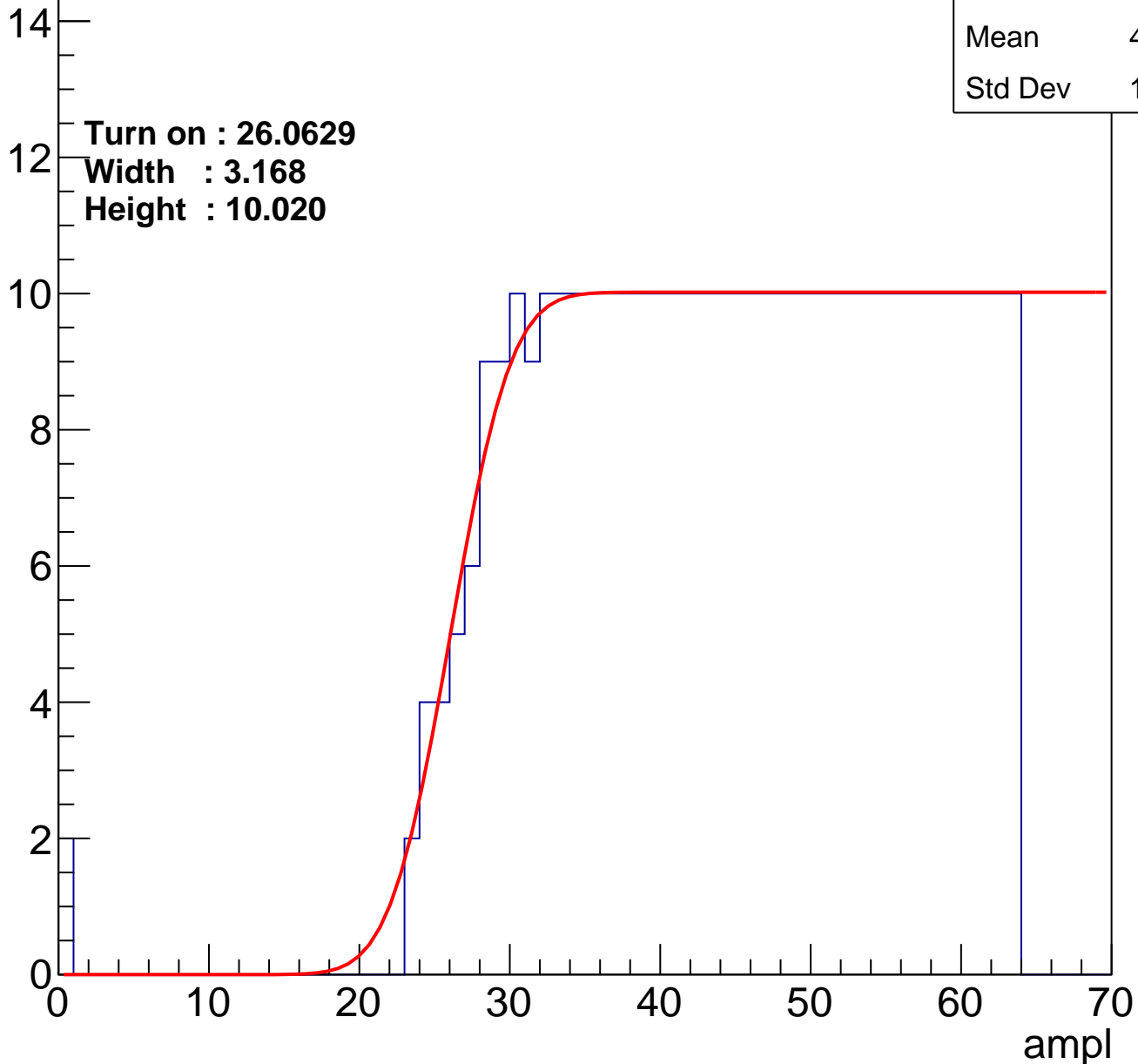
Entries	380
Mean	44.28
Std Dev	11.49

Turn on : 26.0629

Width : 3.168

Height : 10.020

Entry



# B1L002S, U2-ch58

calib\_packv5\_042523\_0143.root, FC#10, port B3

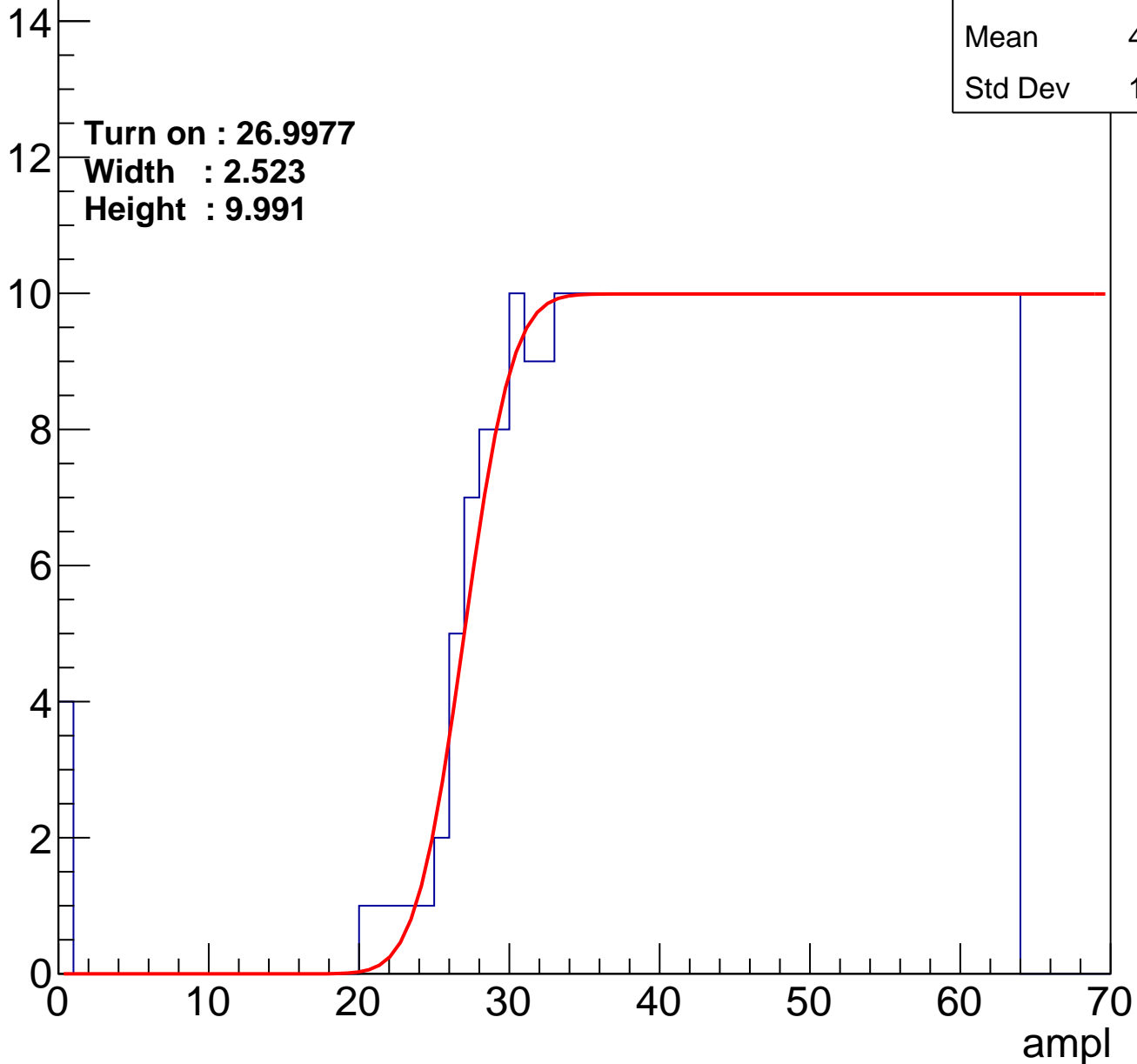
Entry

Entries	377
Mean	44.25
Std Dev	11.85

Turn on : 26.9977

Width : 2.523

Height : 9.991



# B1L002S, U2-ch59

calib\_packv5\_042523\_0143.root, FC#10, port B3

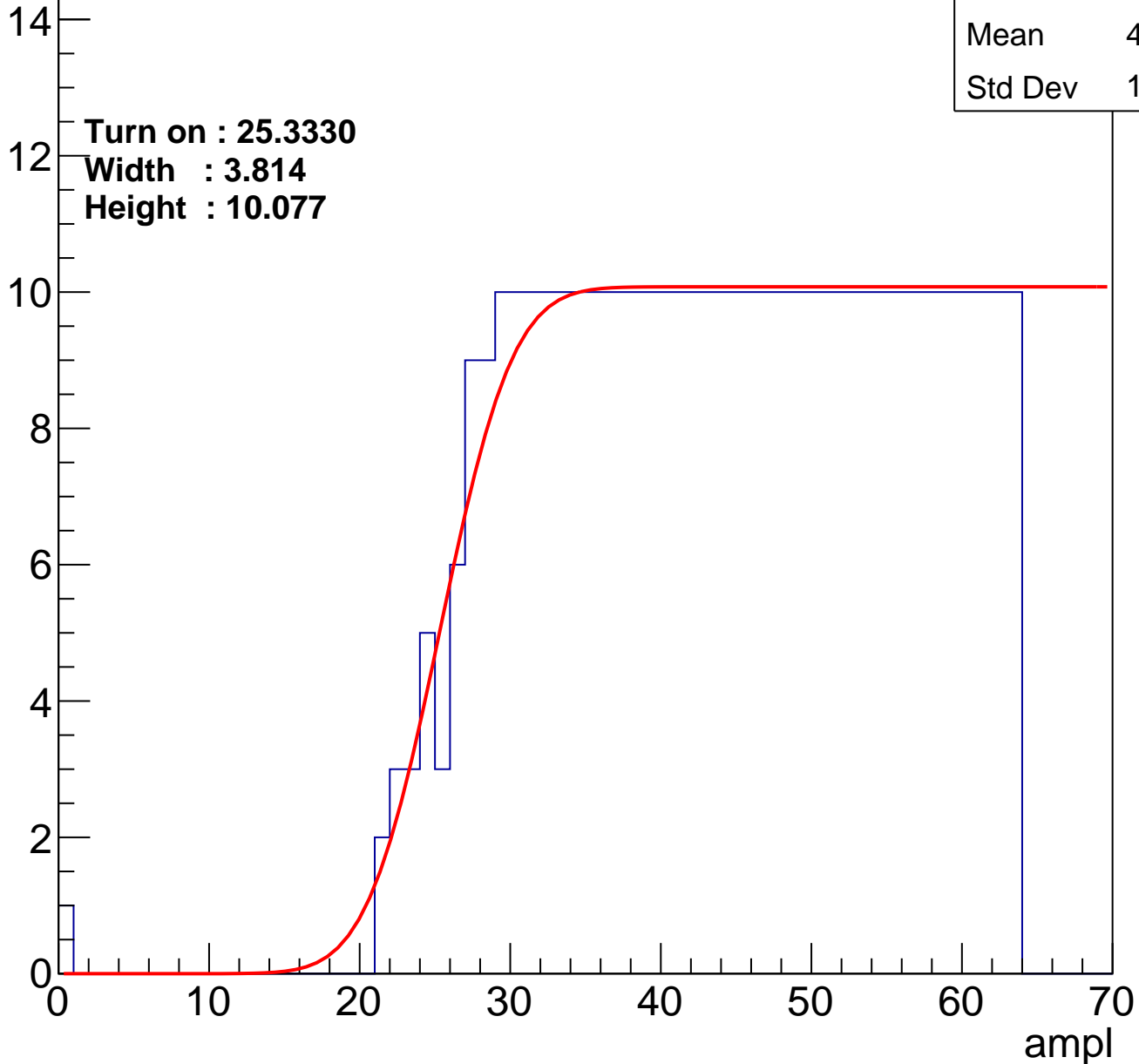
Entries	391
Mean	43.79
Std Dev	11.62

Turn on : 25.3330

Width : 3.814

Height : 10.077

Entry



# B1L002S, U2-ch60

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	408
Mean	42.87
Std Dev	12.32

Turn on : 23.3507

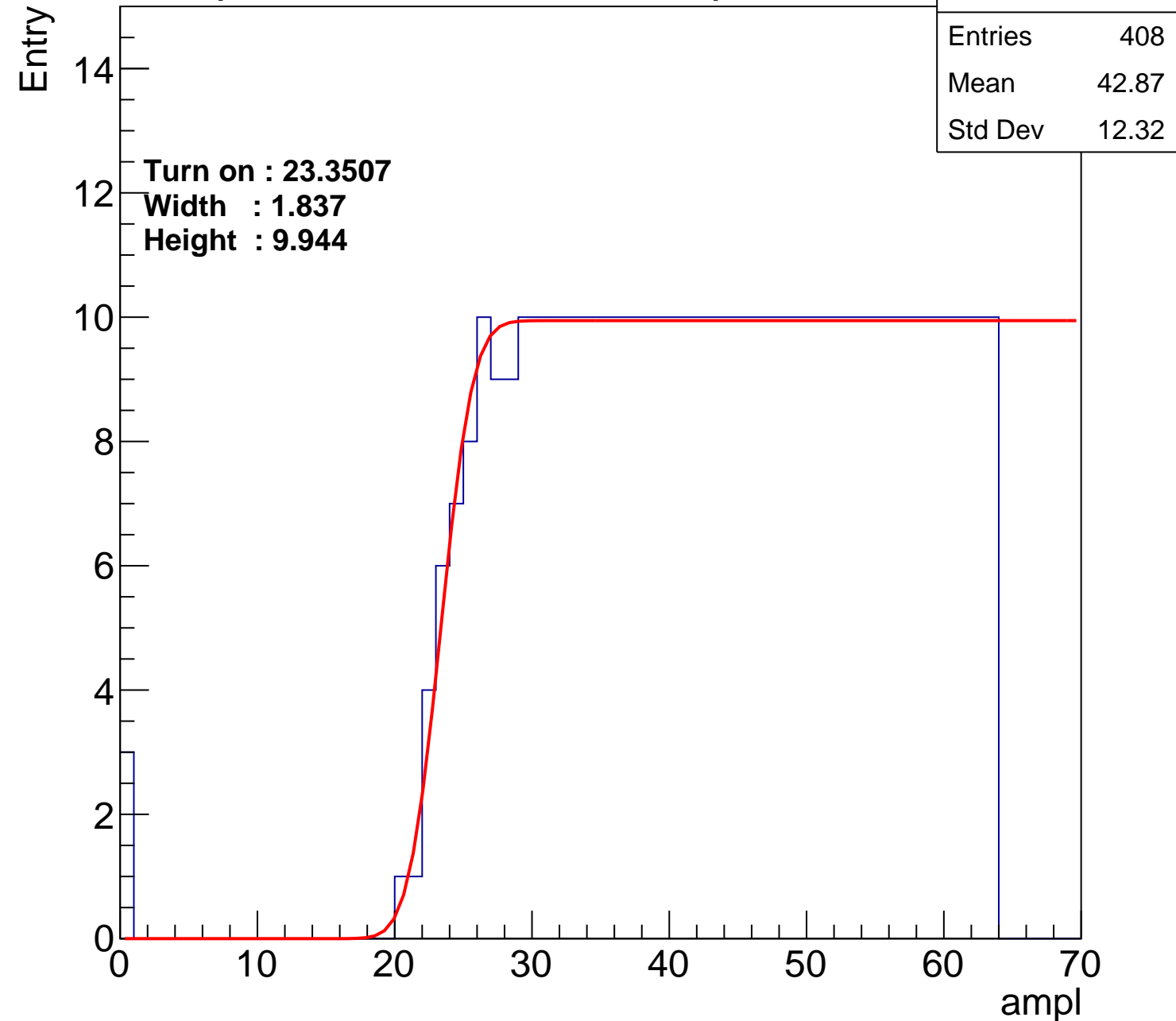
Width : 1.837

Height : 9.944

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch61

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	409
Mean	42.85
Std Dev	12.25

**Turn on : 23.1708**

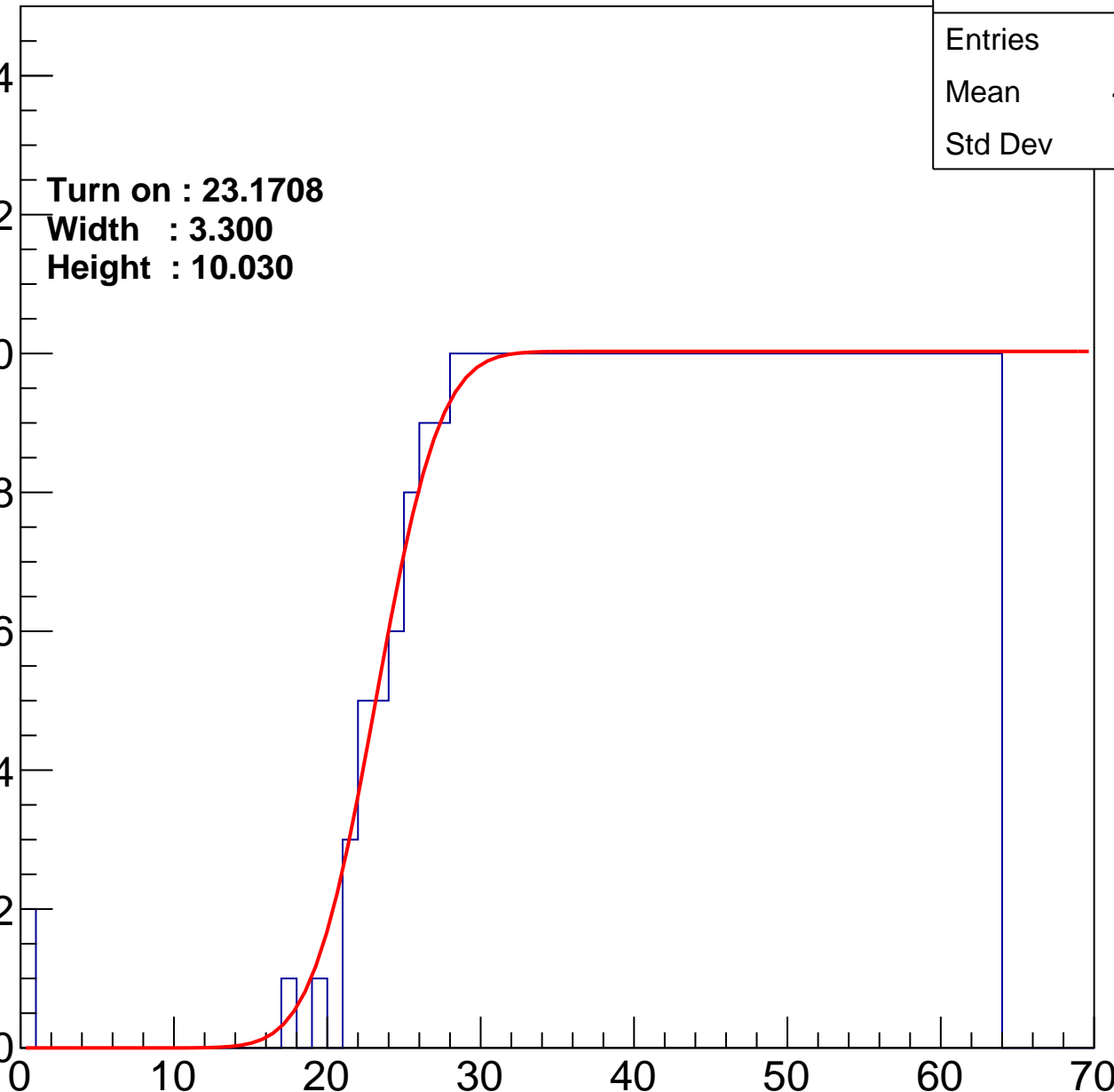
**Width : 3.300**

**Height : 10.030**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch62

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	388
Mean	43.88
Std Dev	11.7

Turn on : 25.3747

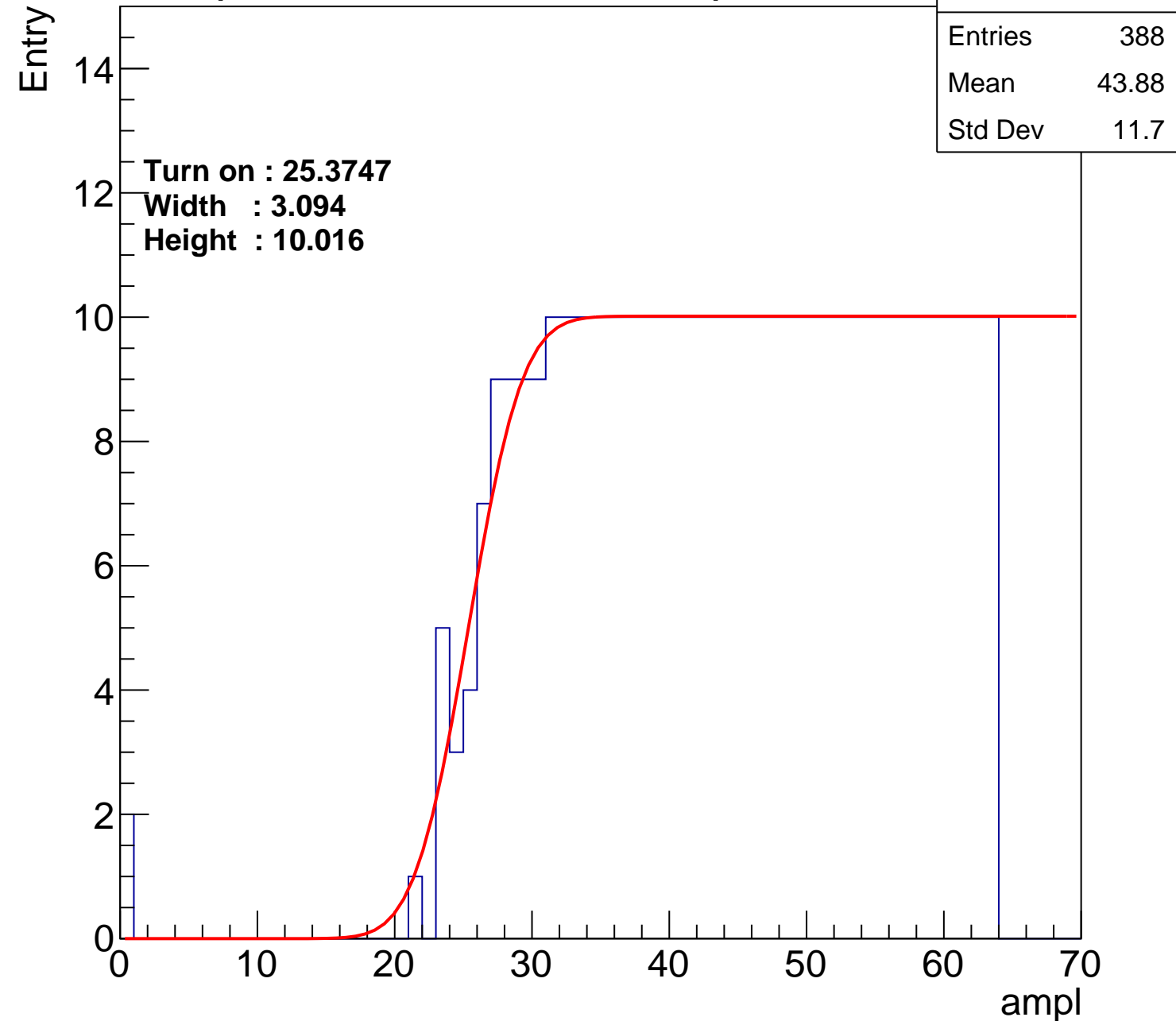
Width : 3.094

Height : 10.016

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L002S, U2-ch63

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	388
Mean	43.89
Std Dev	11.69

Turn on : 25.6196

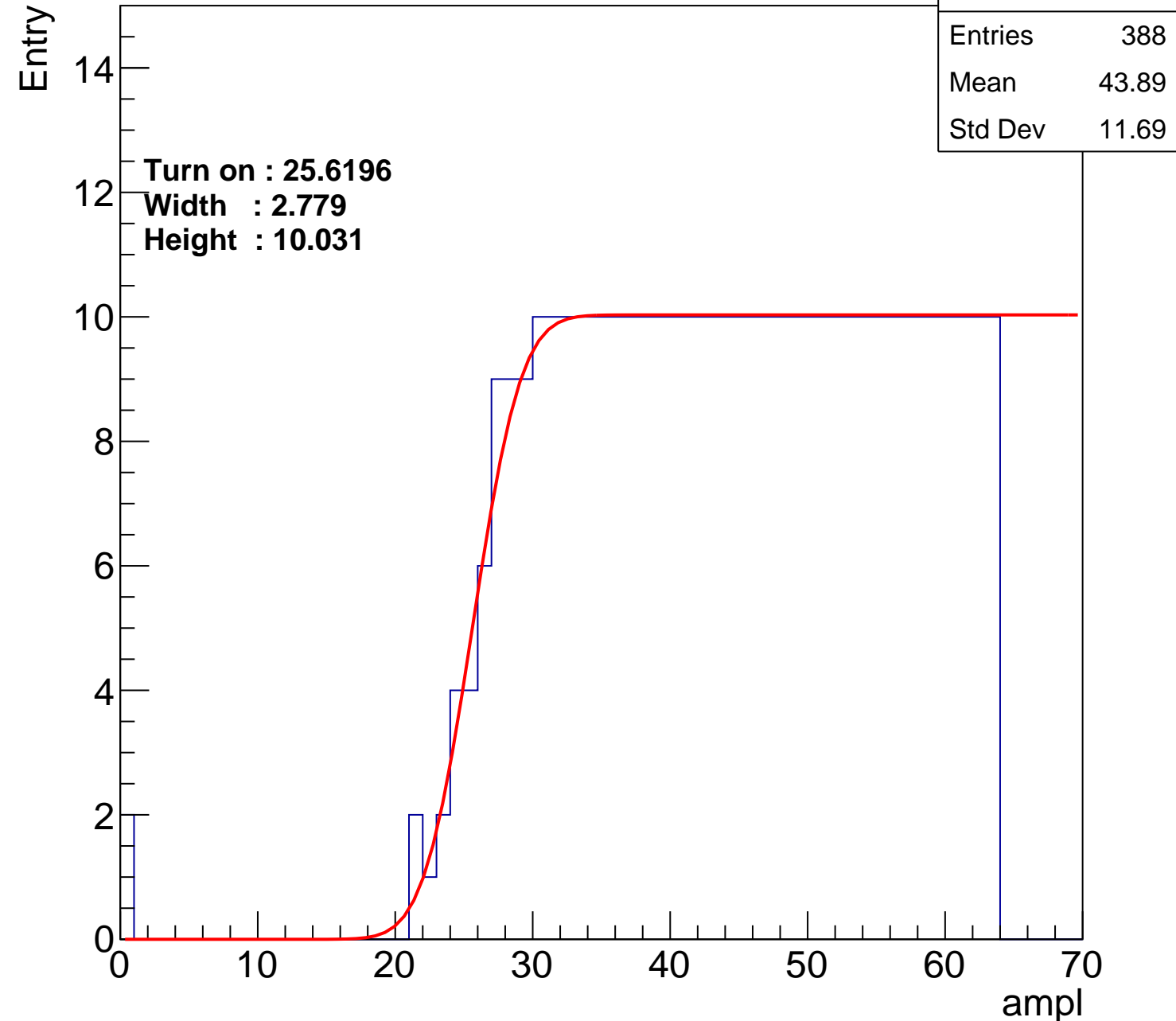
Width : 2.779

Height : 10.031

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch64

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	405
Mean	43.12
Std Dev	11.95

Turn on : 23.1615

Width : 2.420

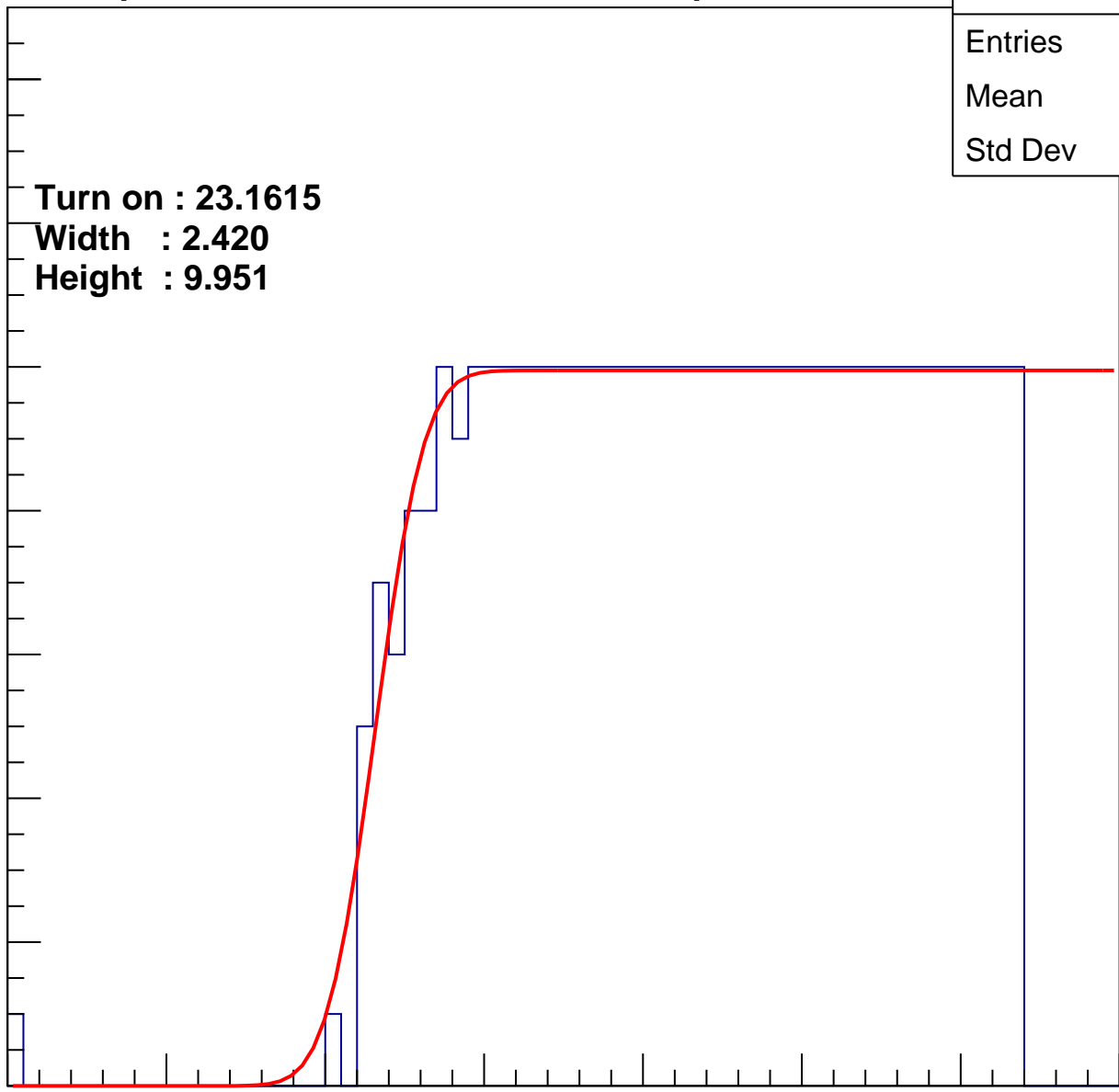
Height : 9.951

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L002S, U2-ch65

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	400
Mean	43.31
Std Dev	11.98

Turn on : 24.6173

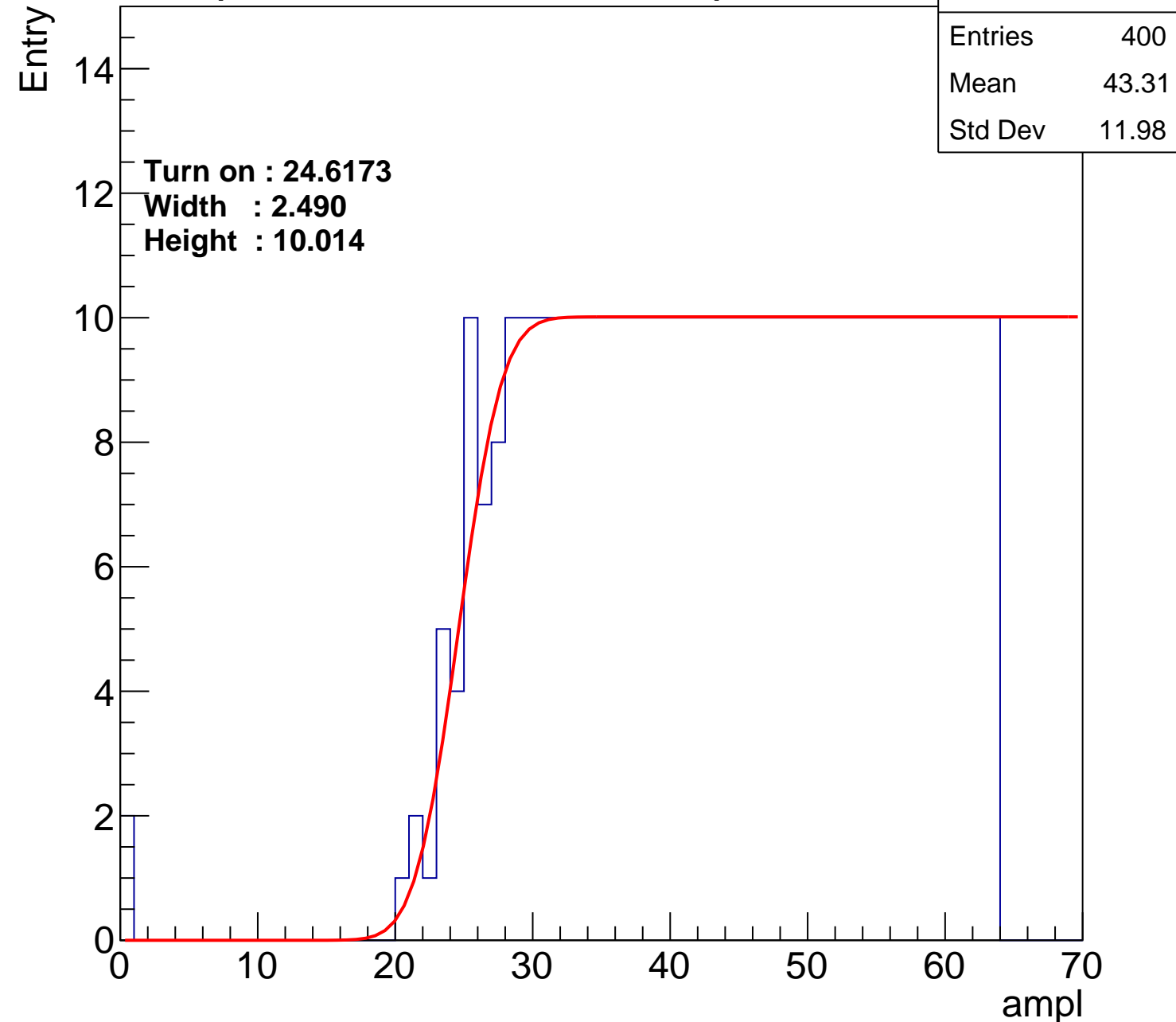
Width : 2.490

Height : 10.014

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch66

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	379
Mean	44.15
Std Dev	11.97

Turn on : 26.5022

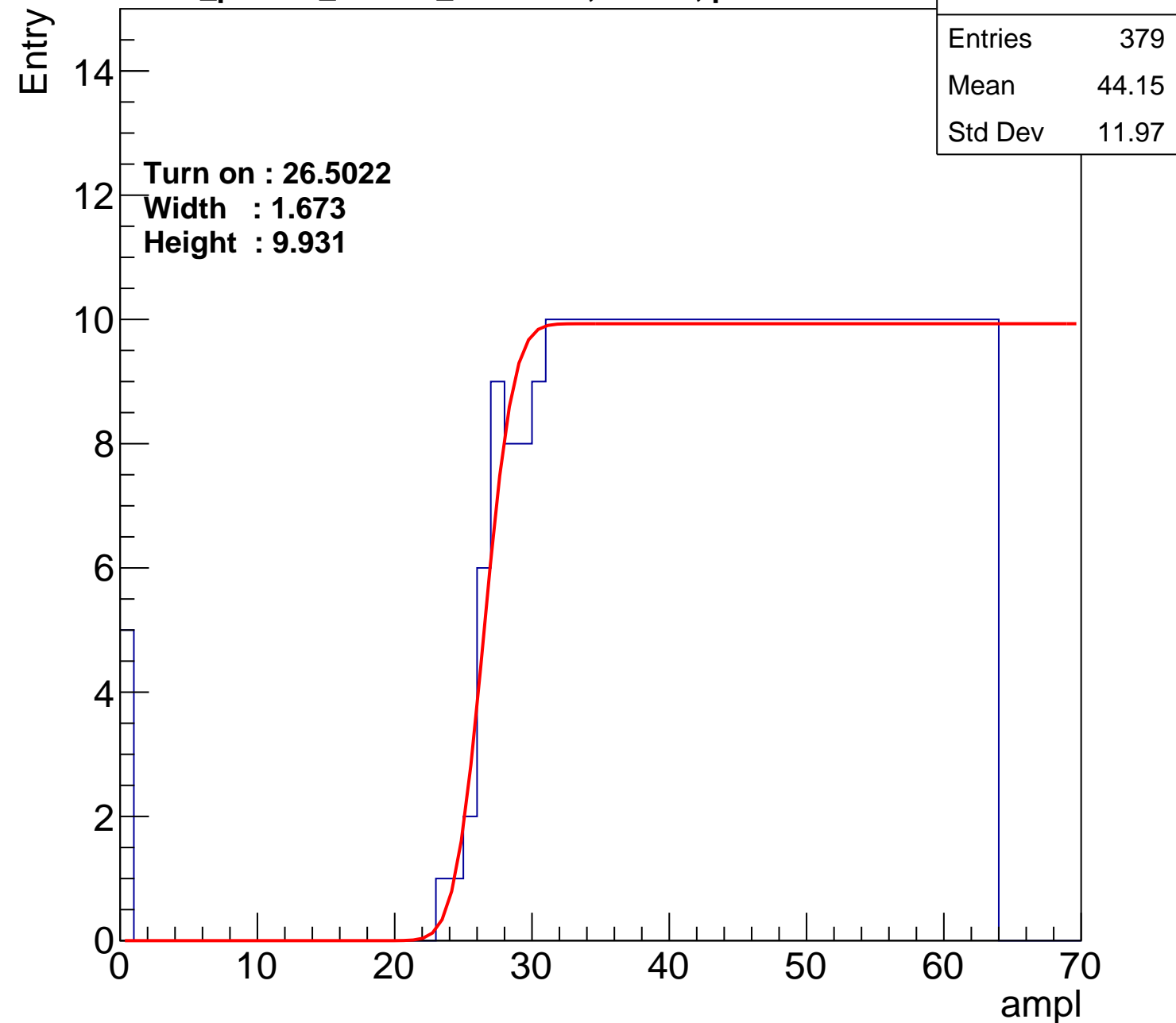
Width : 1.673

Height : 9.931

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch67

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	401
Mean	43.17
Std Dev	12.21

Turn on : 24.5420

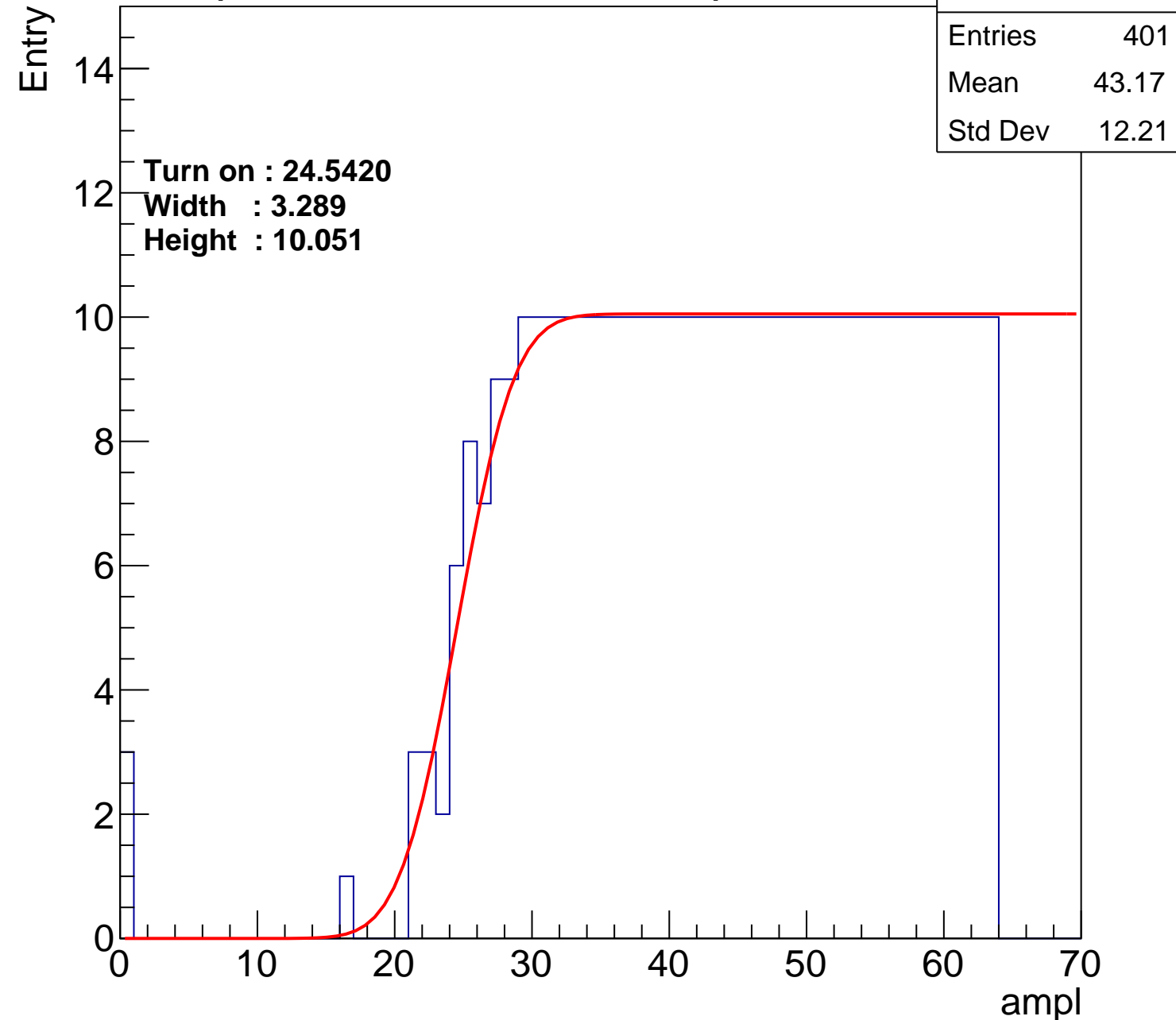
Width : 3.289

Height : 10.051

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch68

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	376
Mean	44.4
Std Dev	11.59

Turn on : 27.3090

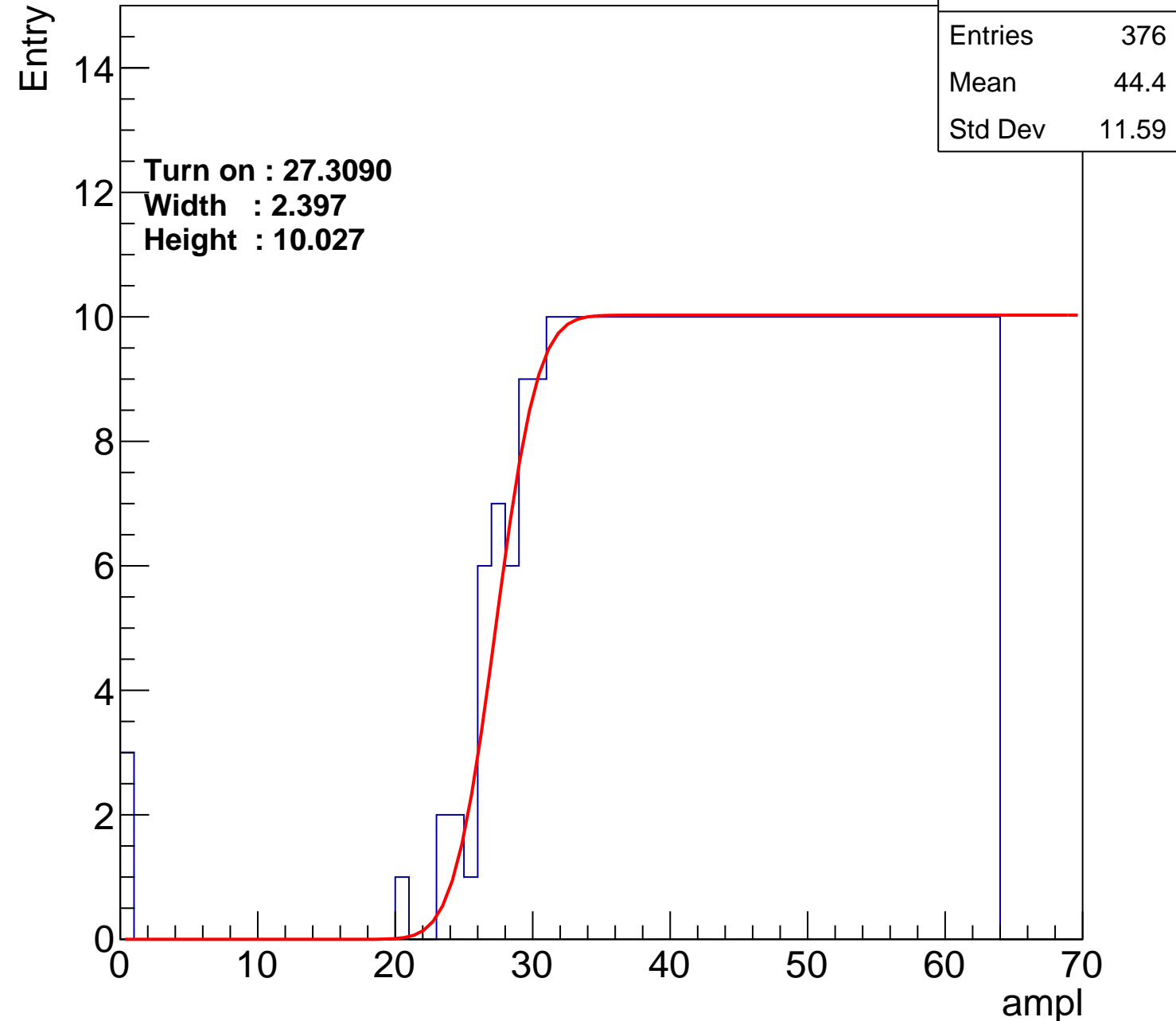
Width : 2.397

Height : 10.027

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch69

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	383
Mean	44.05
Std Dev	11.77

Turn on : 25.9188

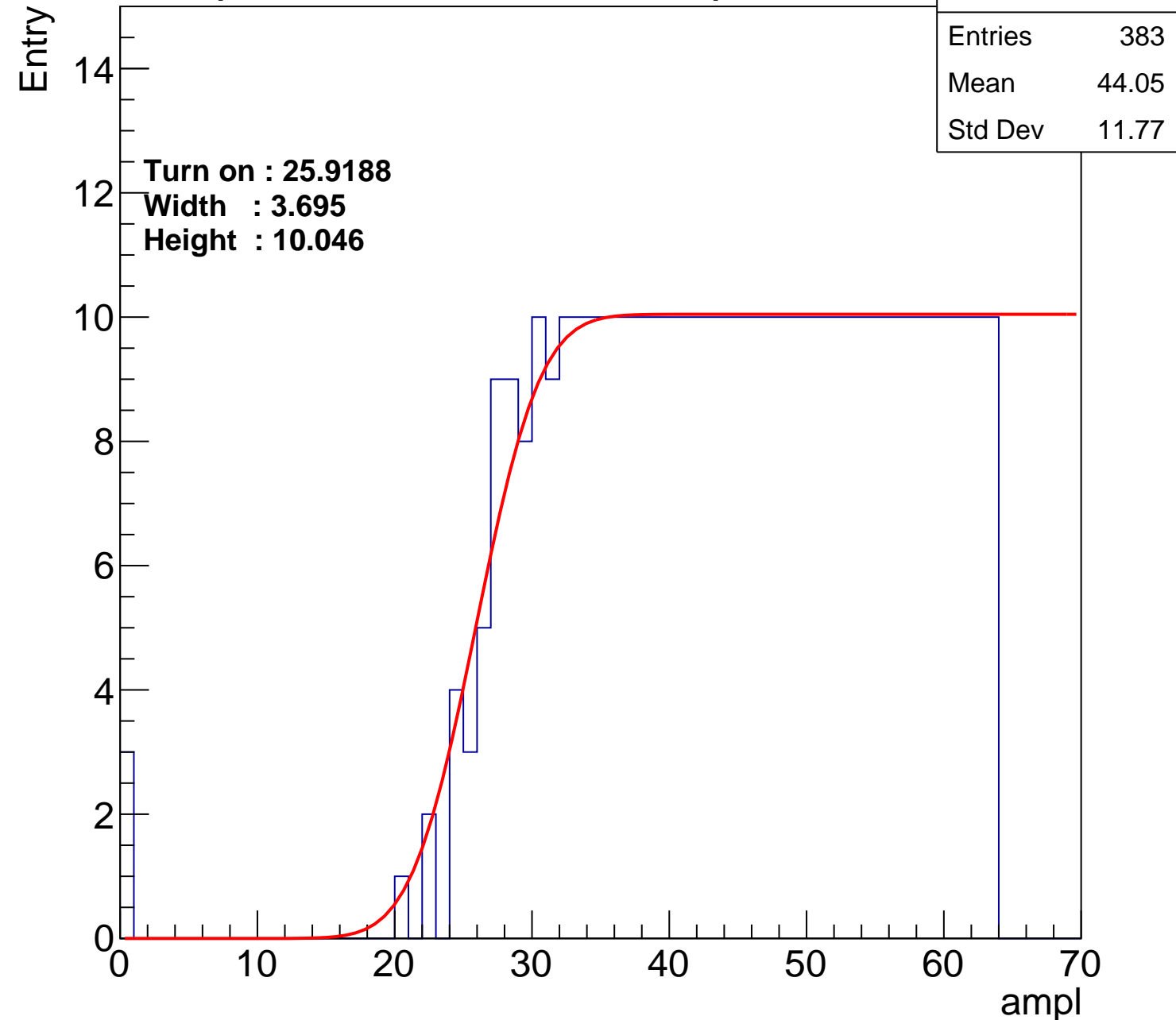
Width : 3.695

Height : 10.046

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch70

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	417
Mean	42.36
Std Dev	12.7

Turn on : 23.3032

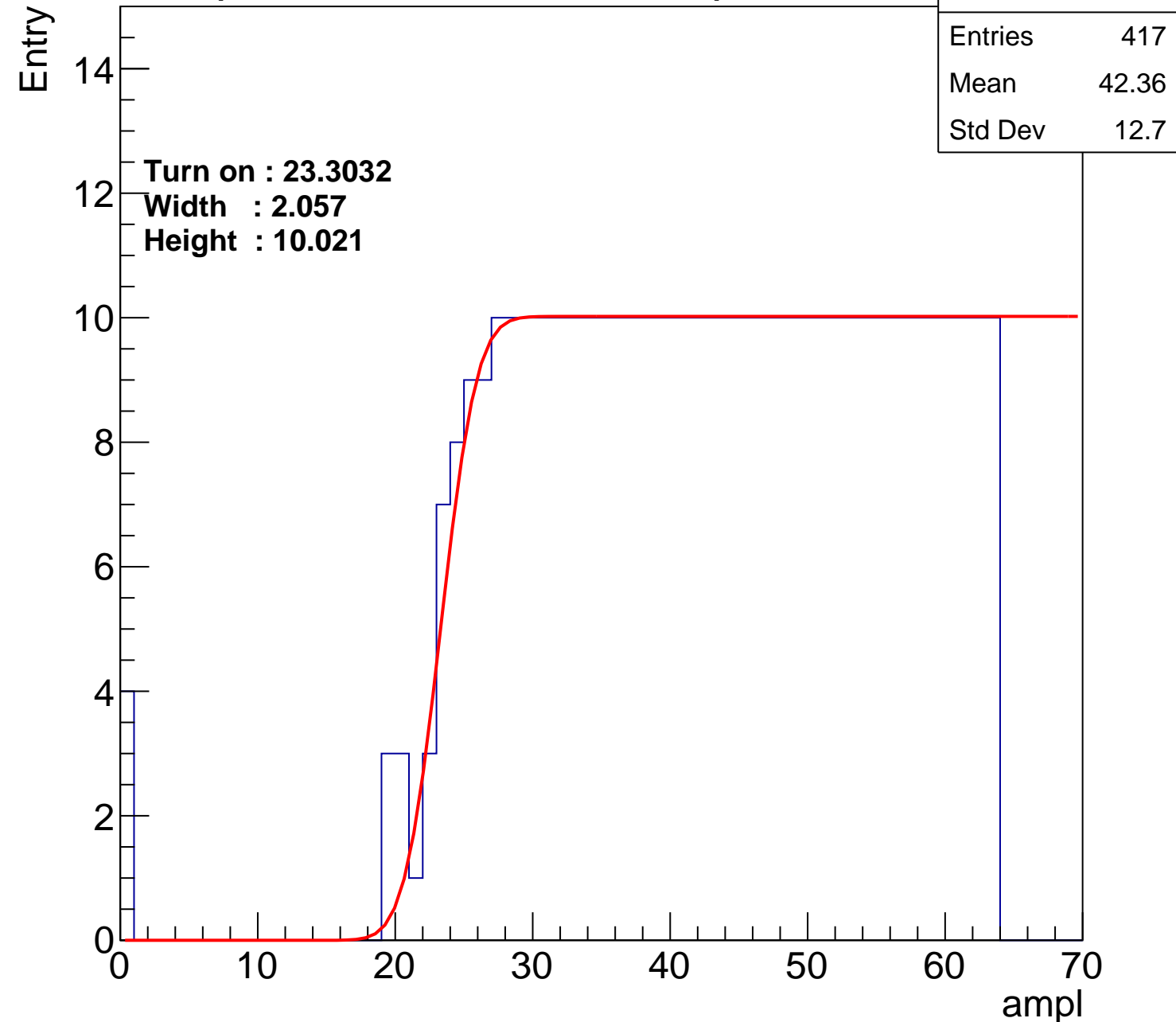
Width : 2.057

Height : 10.021

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L002S, U2-ch71

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	385
Mean	43.91
Std Dev	11.95

Turn on : 26.3926

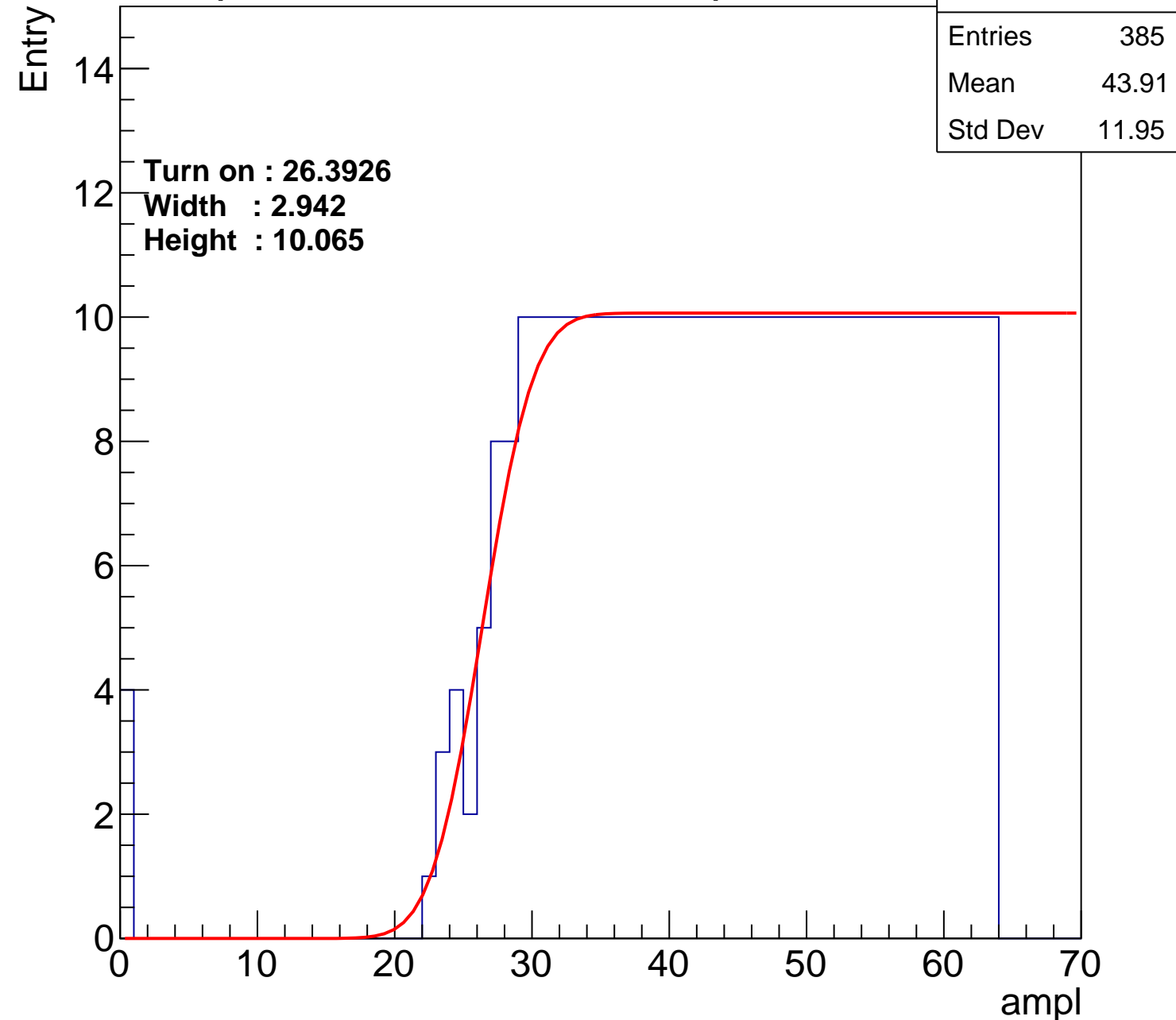
Width : 2.942

Height : 10.065

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch72

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	380
Mean	44.37
Std Dev	11.27

Turn on : 26.3110

Width : 2.505

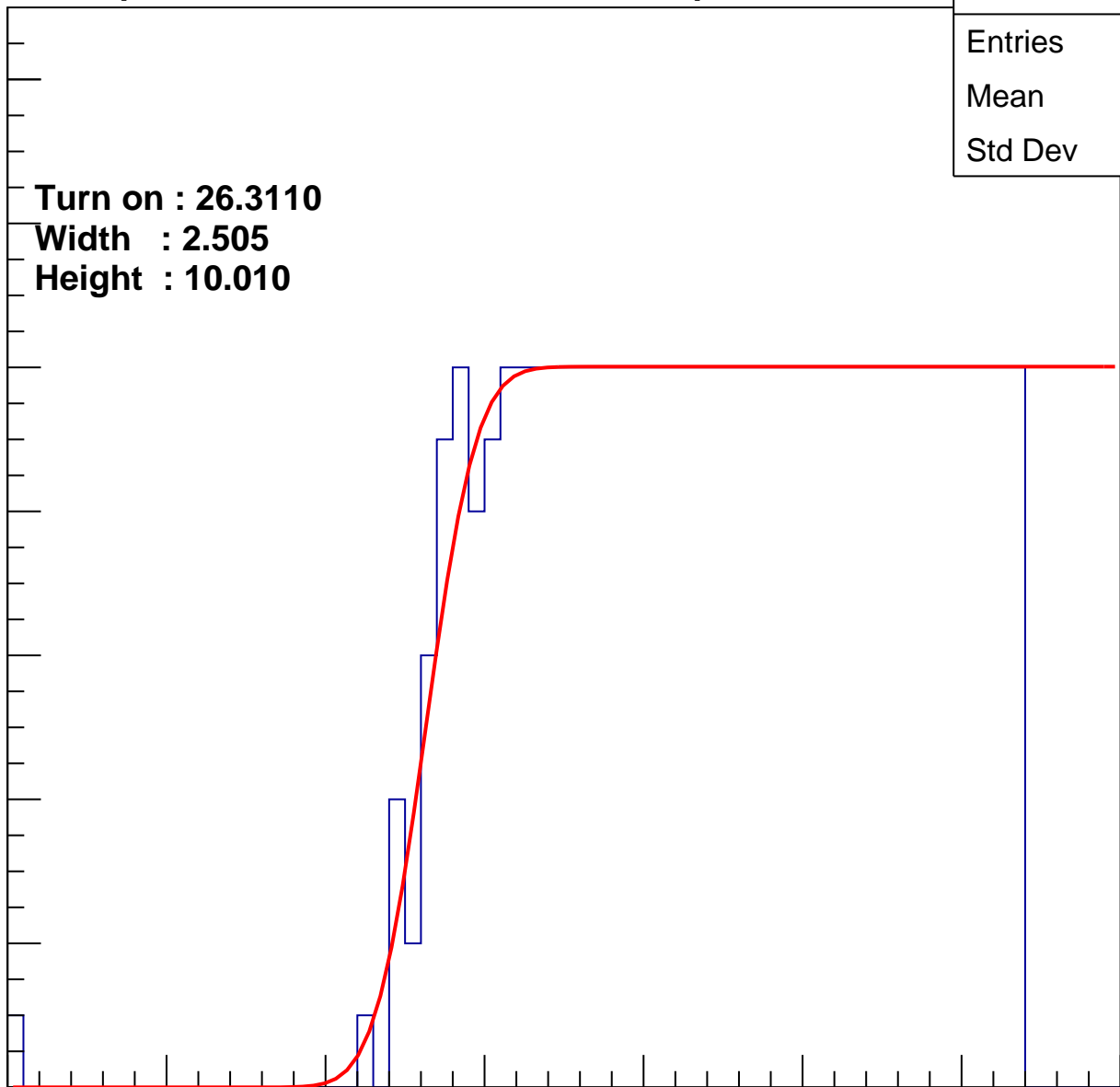
Height : 10.010

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L002S, U2-ch73

calib\_packv5\_042523\_0143.root, FC#10, port B3

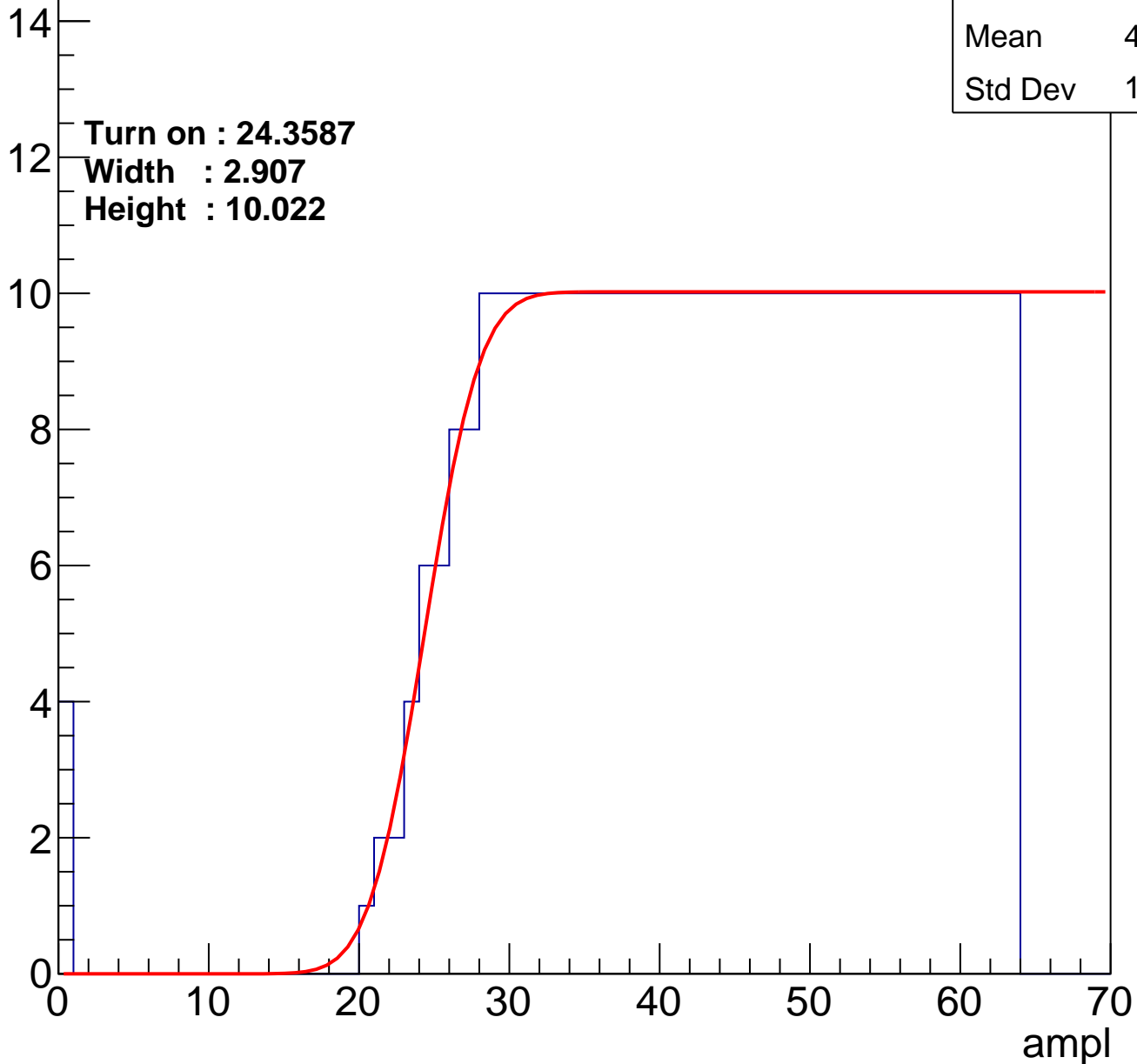
Entries	401
Mean	43.13
Std Dev	12.33

Turn on : 24.3587

Width : 2.907

Height : 10.022

Entry



# B1L002S, U2-ch74

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	387
Mean	43.93
Std Dev	11.67

Turn on : 25.5552

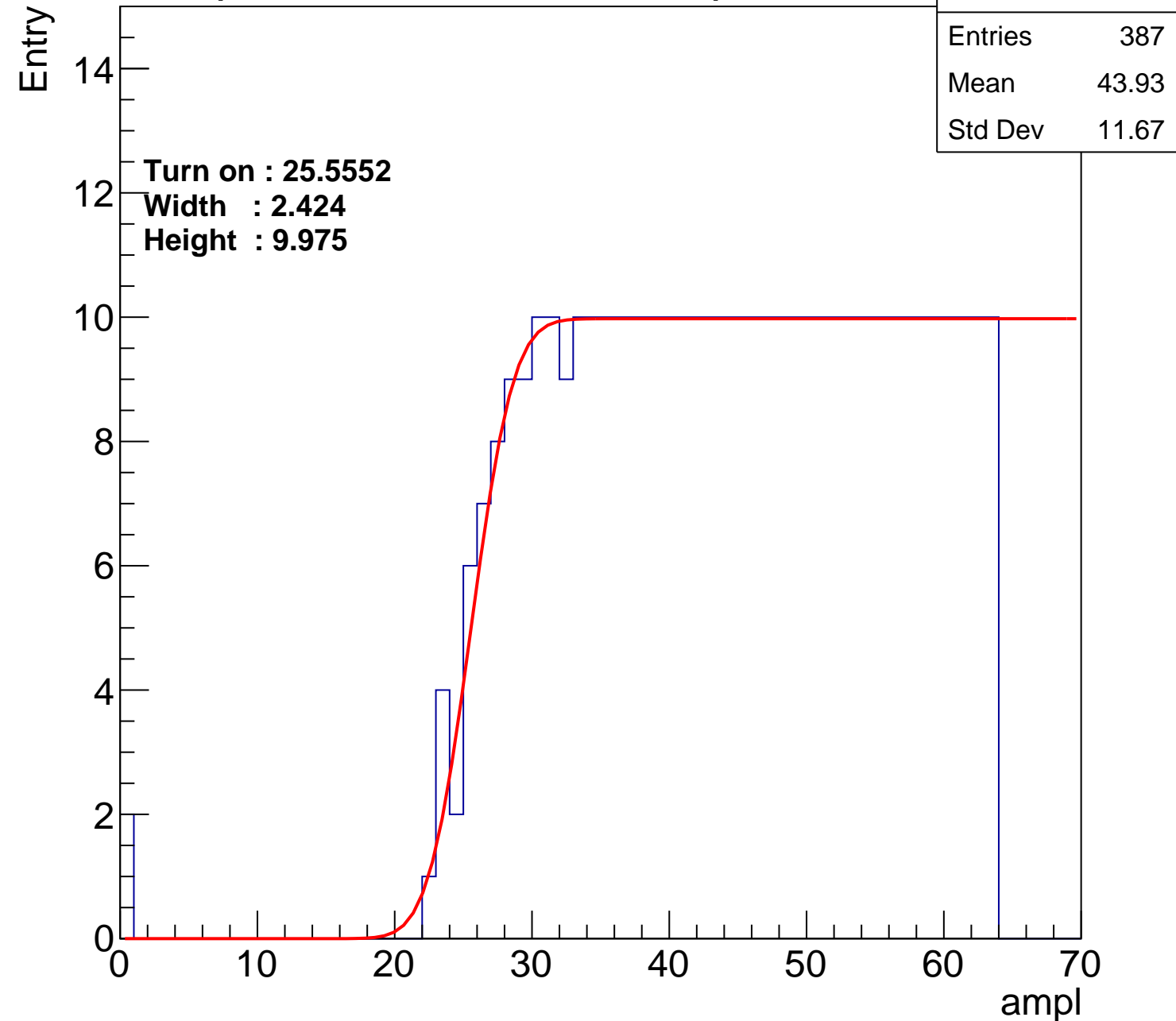
Width : 2.424

Height : 9.975

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch75

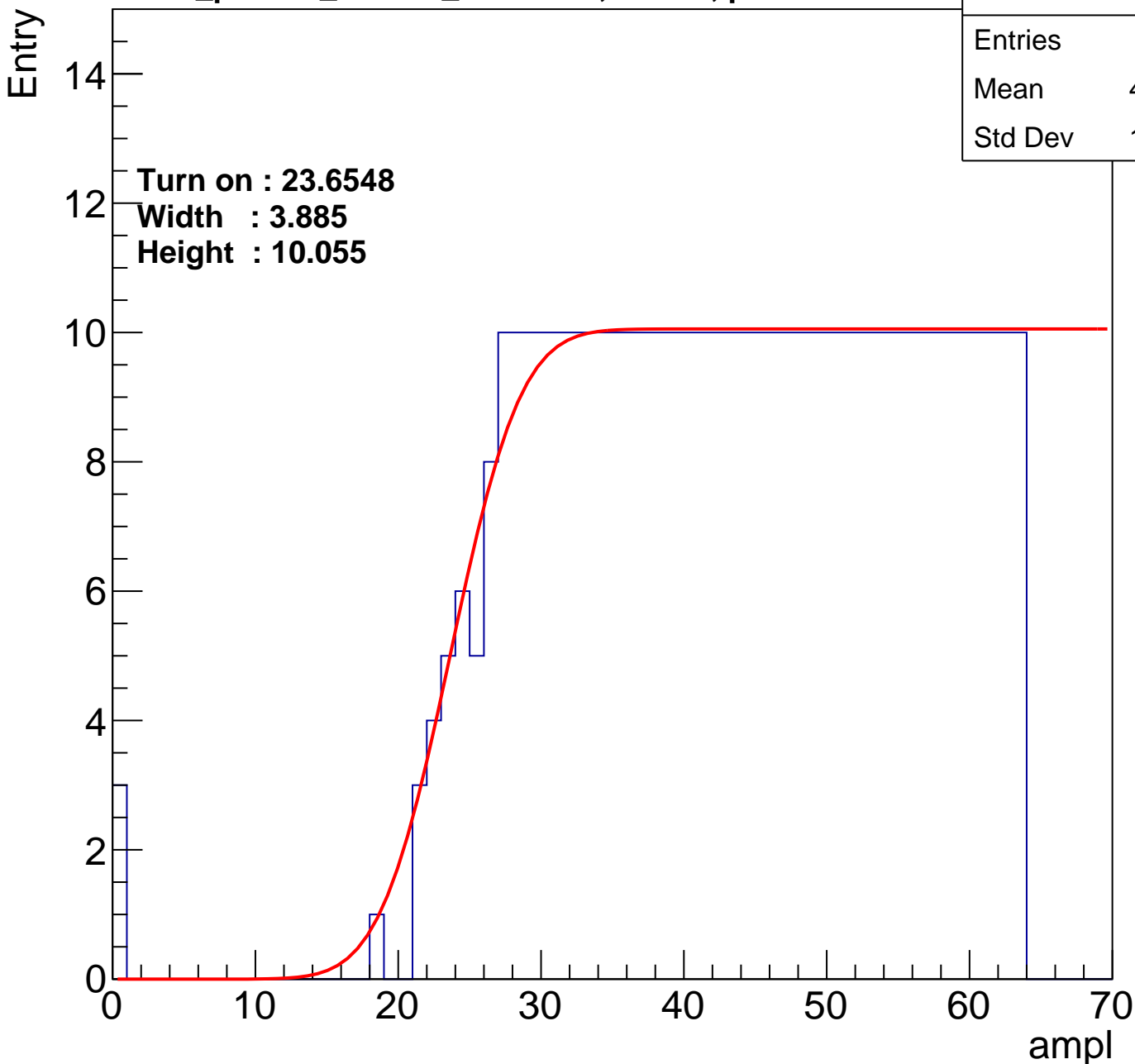
**calib\_packv5\_042523\_0143.root, FC#10, port B3**

Entries	405
Mean	42.99
Std Dev	12.29

**Turn on : 23.6548**

**Width : 3.885**

**Height : 10.055**



# B1L002S, U2-ch76

calib\_packv5\_042523\_0143.root, FC#10, port B3

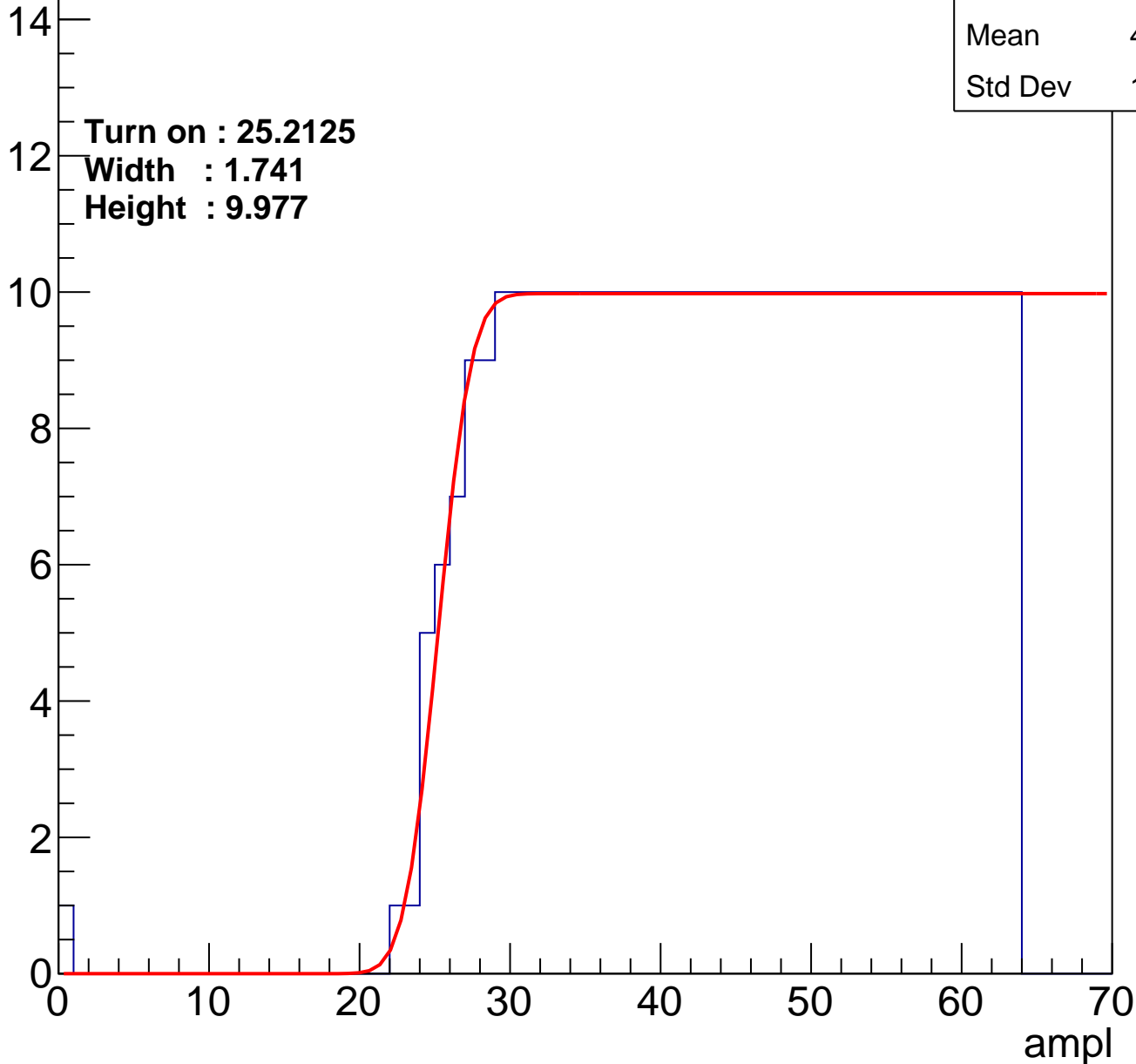
Entry

Entries	389
Mean	43.94
Std Dev	11.48

Turn on : 25.2125

Width : 1.741

Height : 9.977



# B1L002S, U2-ch77

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	378
Mean	44.32
Std Dev	11.61

Turn on : 26.3217

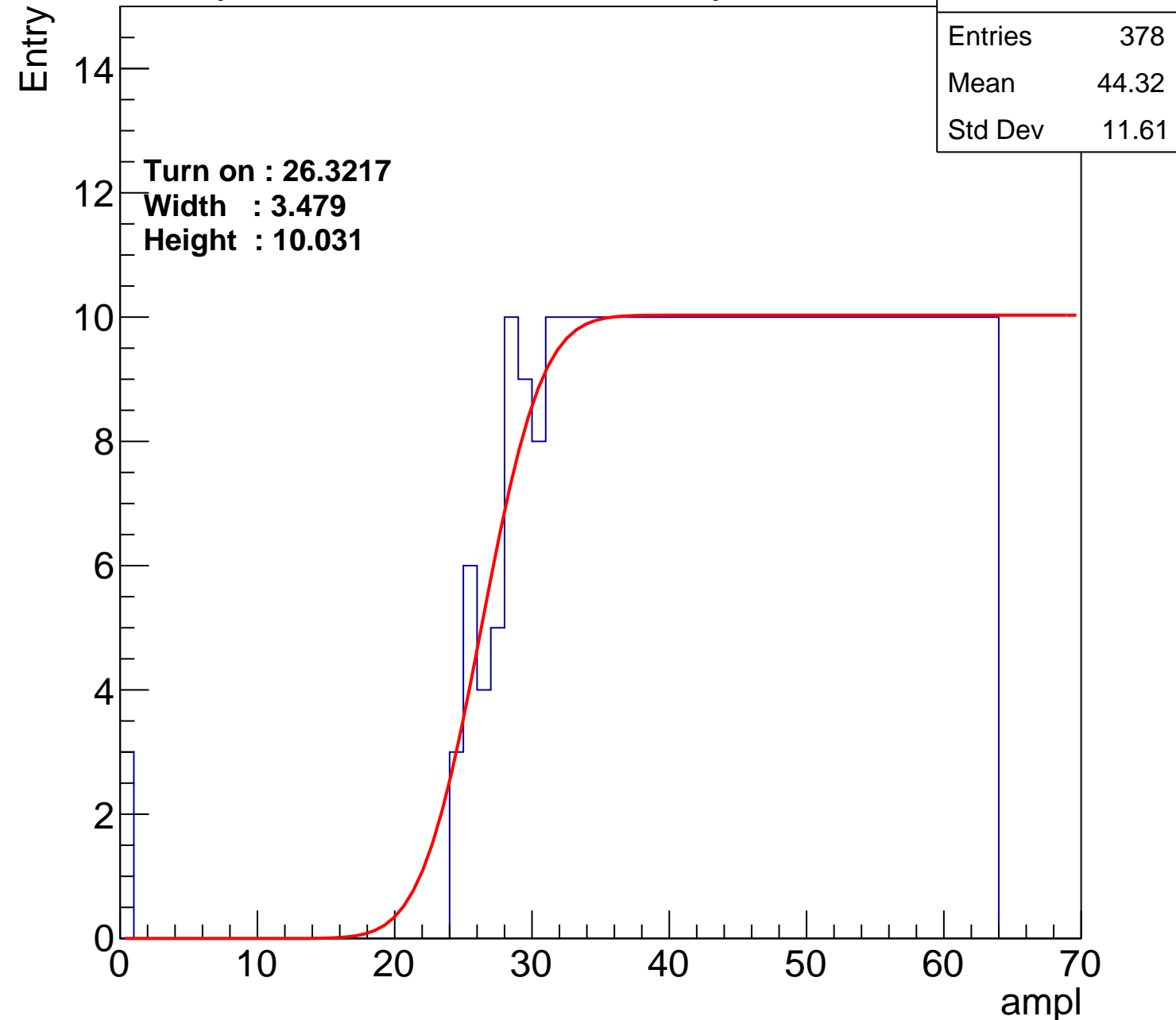
Width : 3.479

Height : 10.031

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch78

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	399
Mean	43.33
Std Dev	11.99

**Turn on : 24.5277**

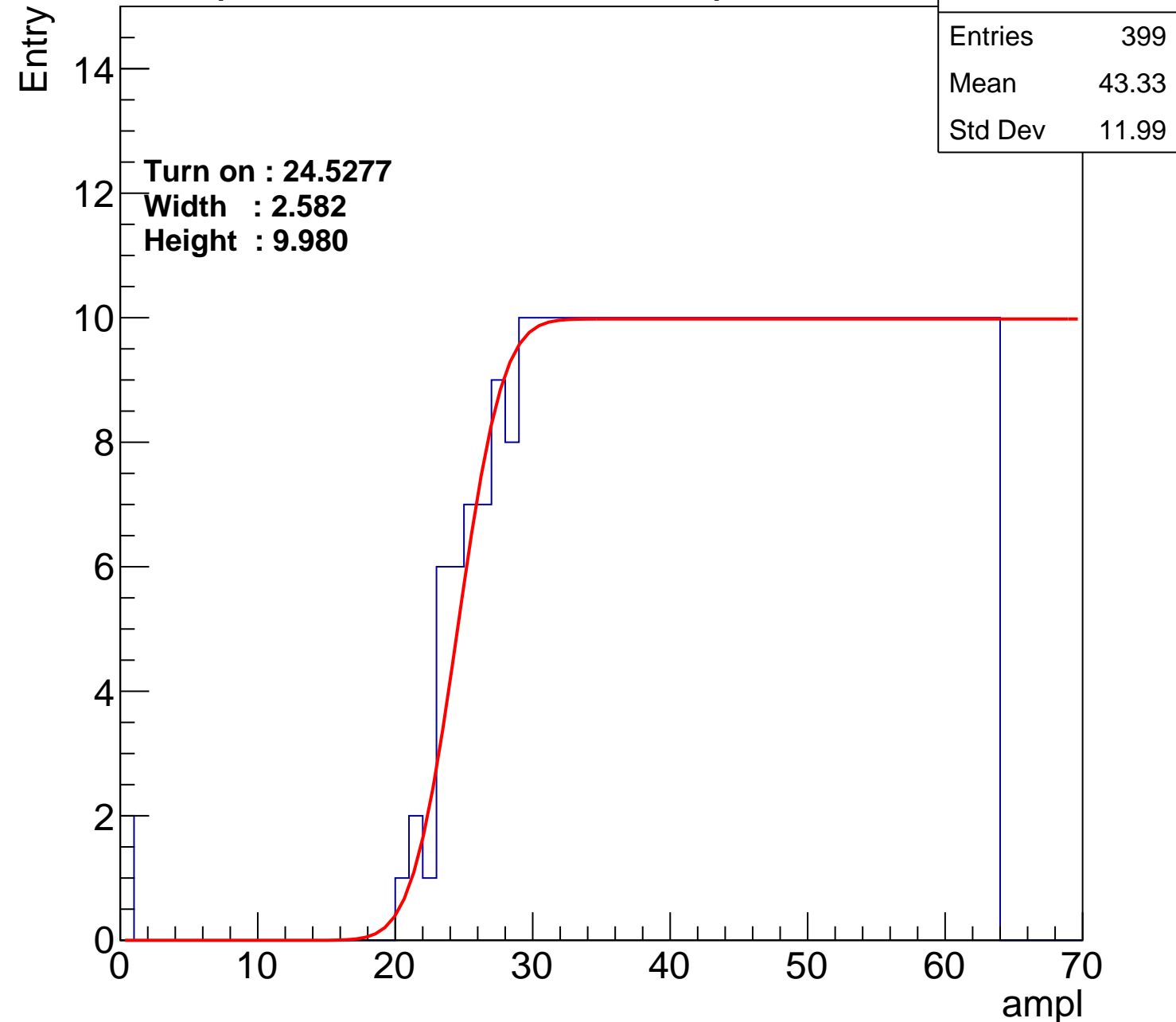
**Width : 2.582**

**Height : 9.980**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L002S, U2-ch79

calib\_packv5\_042523\_0143.root, FC#10, port B3

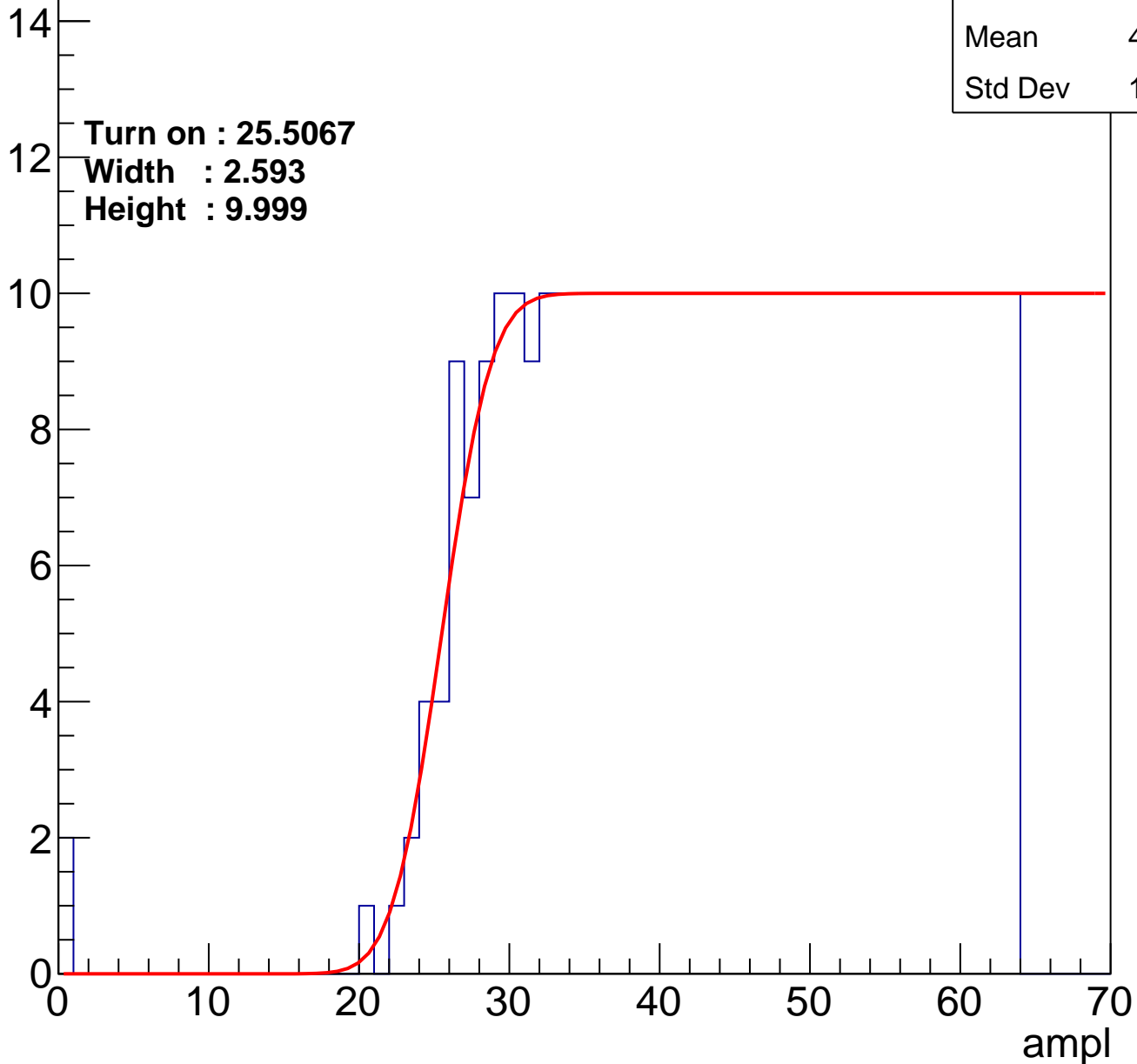
Entries	388
Mean	43.89
Std Dev	11.69

Turn on : 25.5067

Width : 2.593

Height : 9.999

Entry



# B1L002S, U2-ch80

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	403
Mean	43.1
Std Dev	12.22

Turn on : 23.9961

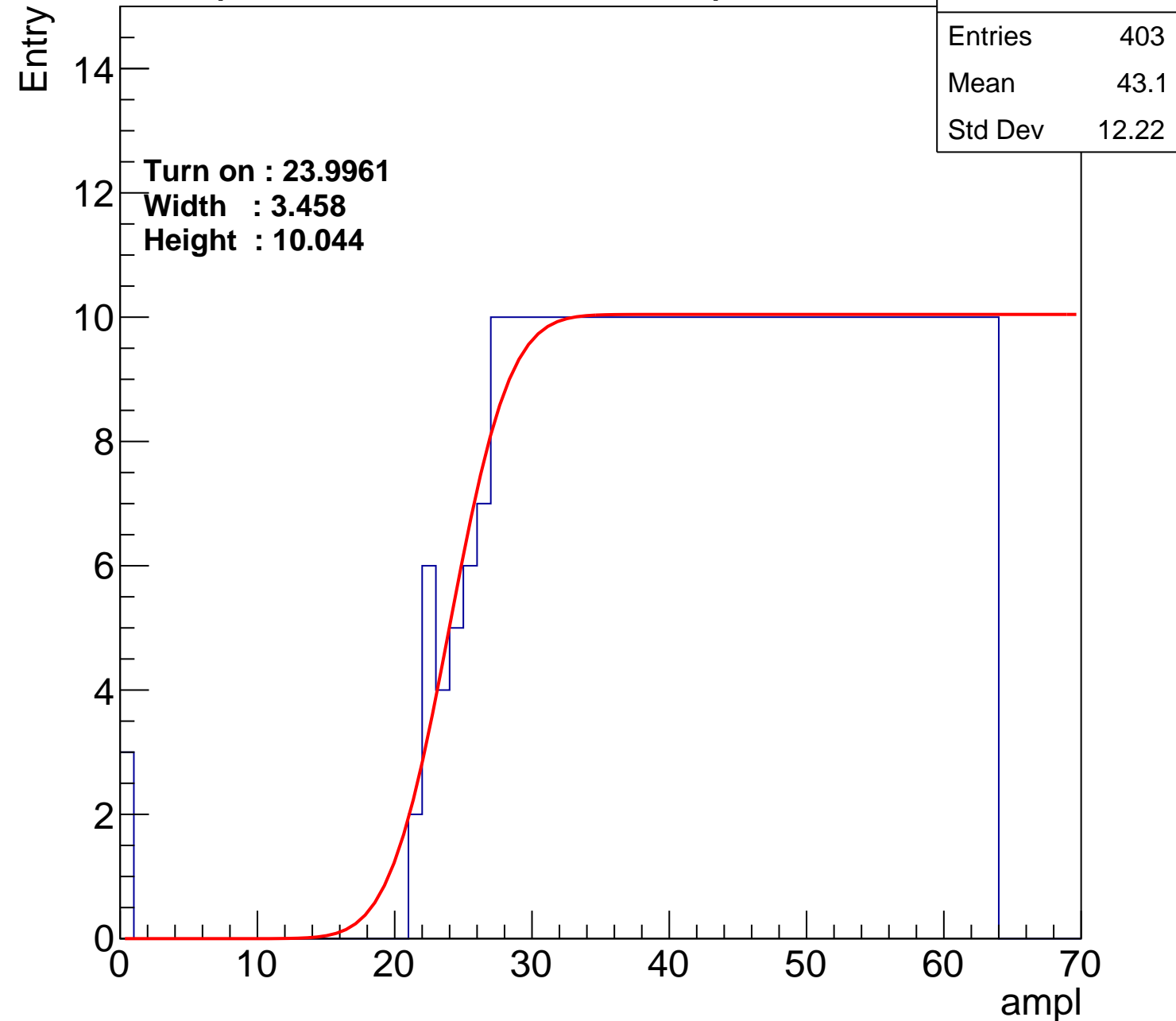
Width : 3.458

Height : 10.044

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch81

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	395
Mean	43.63
Std Dev	11.66

Turn on : 24.8381

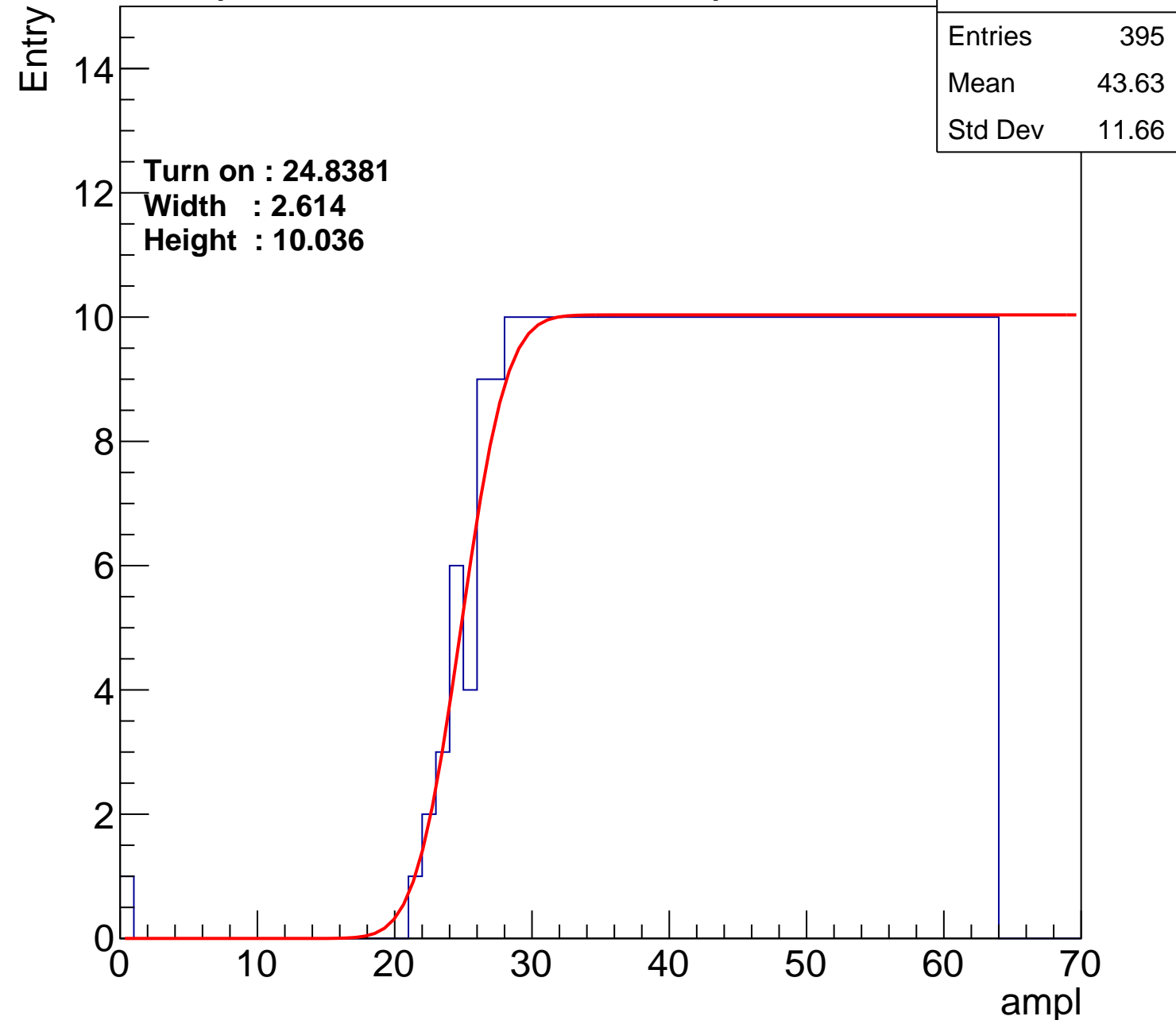
Width : 2.614

Height : 10.036

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch82

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	412
Mean	42.69
Std Dev	12.35

Turn on : 23.2390

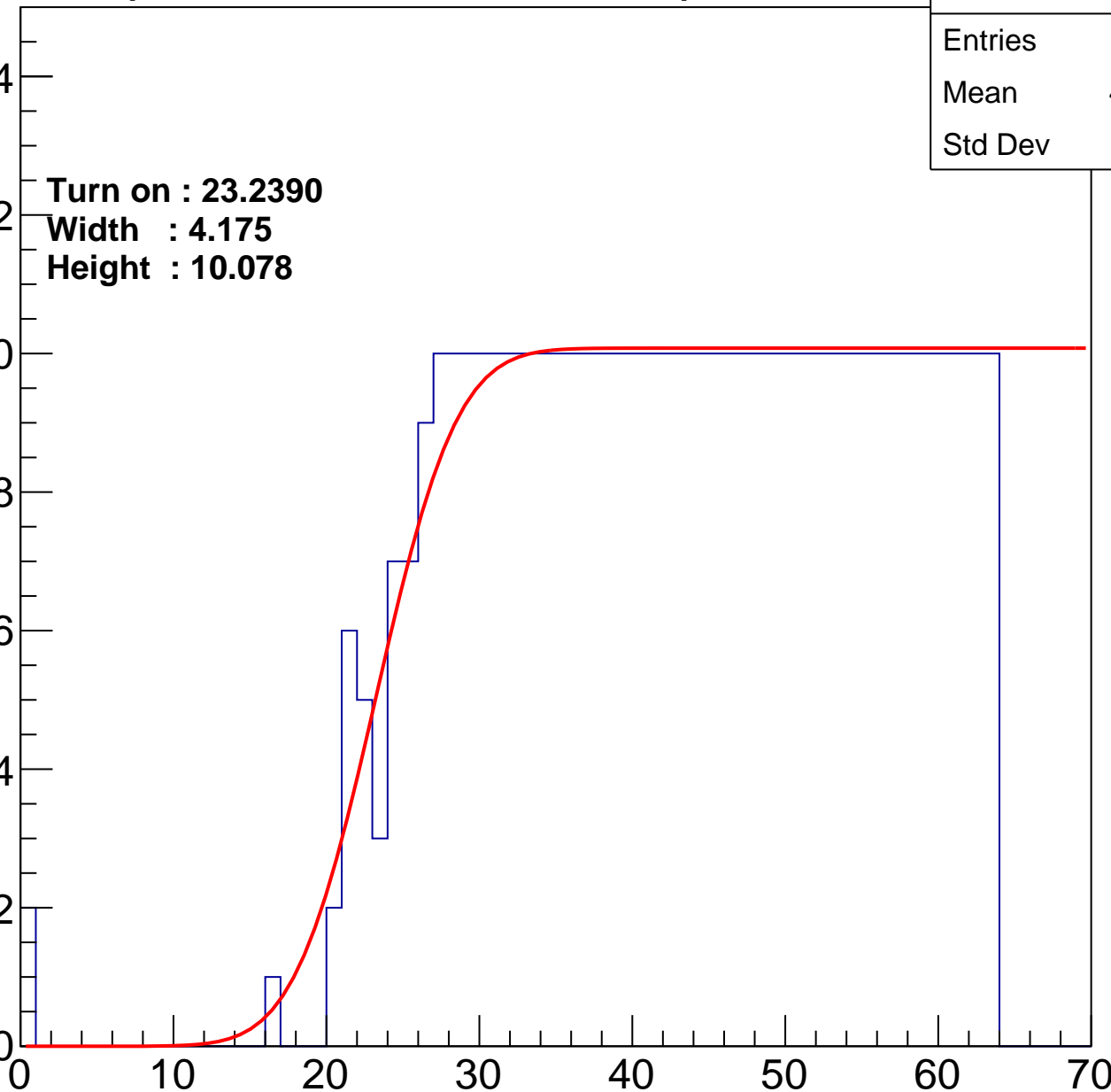
Width : 4.175

Height : 10.078

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch83

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	397
Mean	43.32
Std Dev	12.23

Turn on : 24.8613

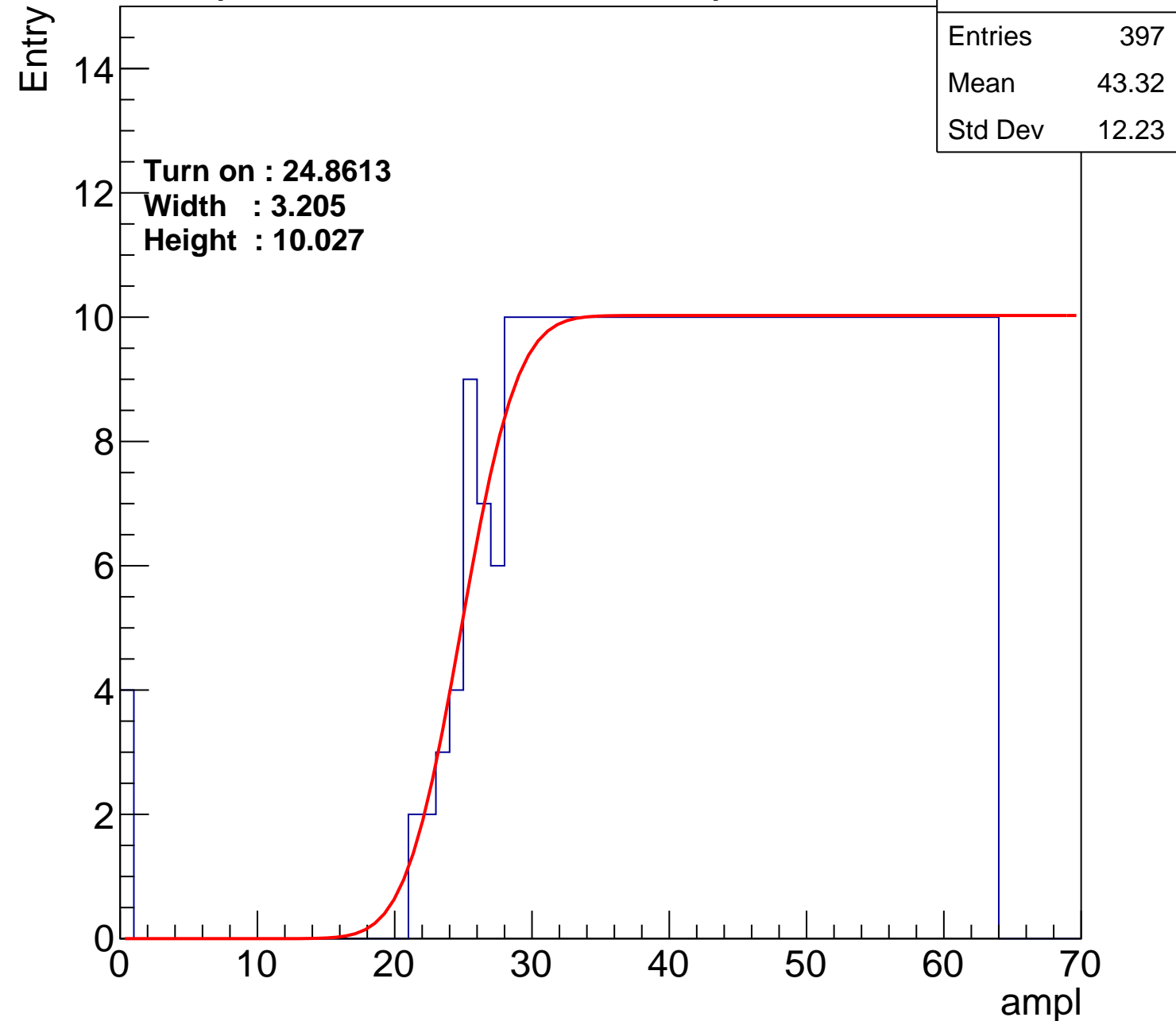
Width : 3.205

Height : 10.027

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch84

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	396
Mean	43.48
Std Dev	11.92

Turn on : 24.6946

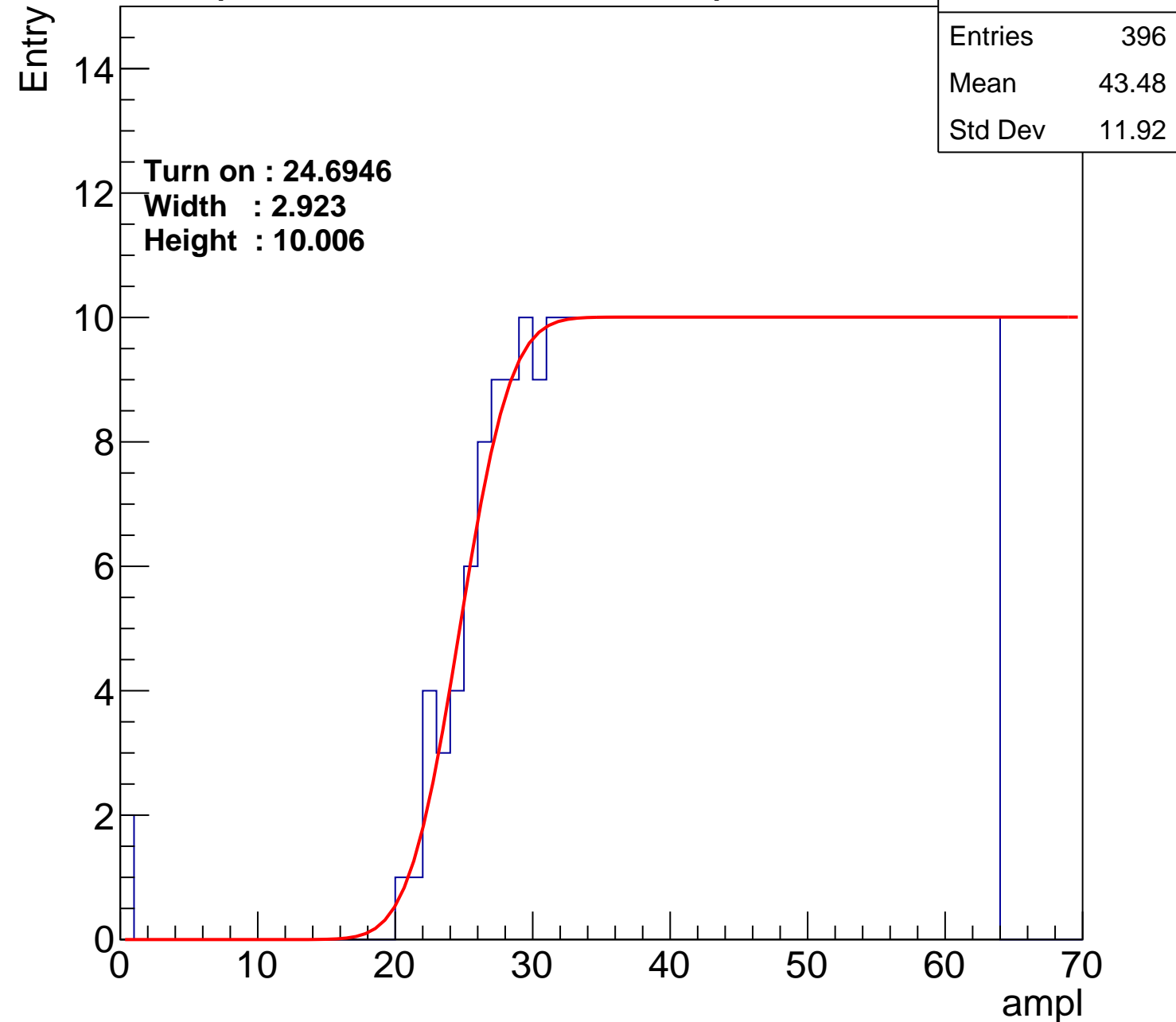
Width : 2.923

Height : 10.006

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch85

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	385
Mean	43.82
Std Dev	12.17

Turn on : 27.2228

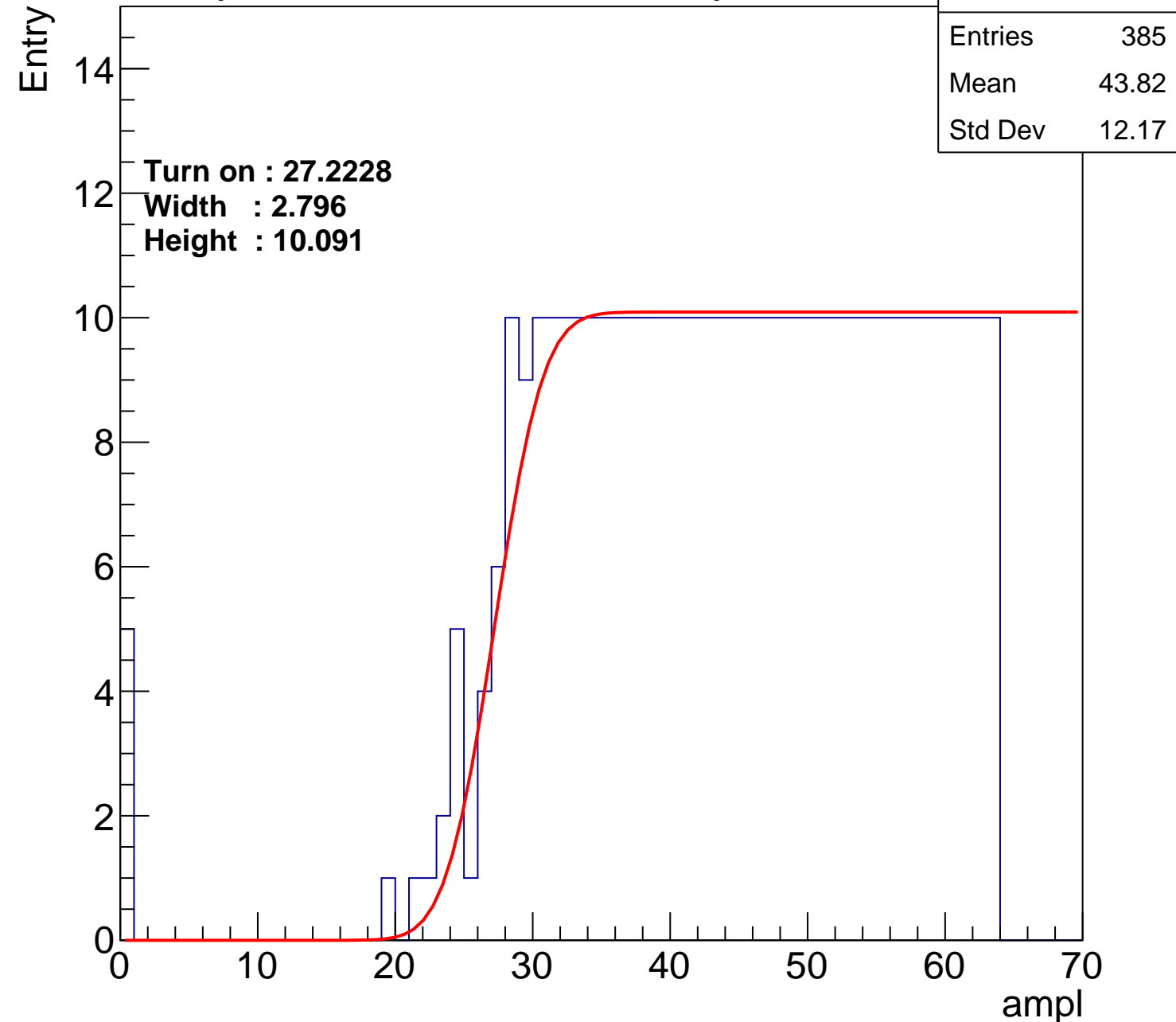
Width : 2.796

Height : 10.091

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch86

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	389
Mean	43.85
Std Dev	11.7

Turn on : 25.2896

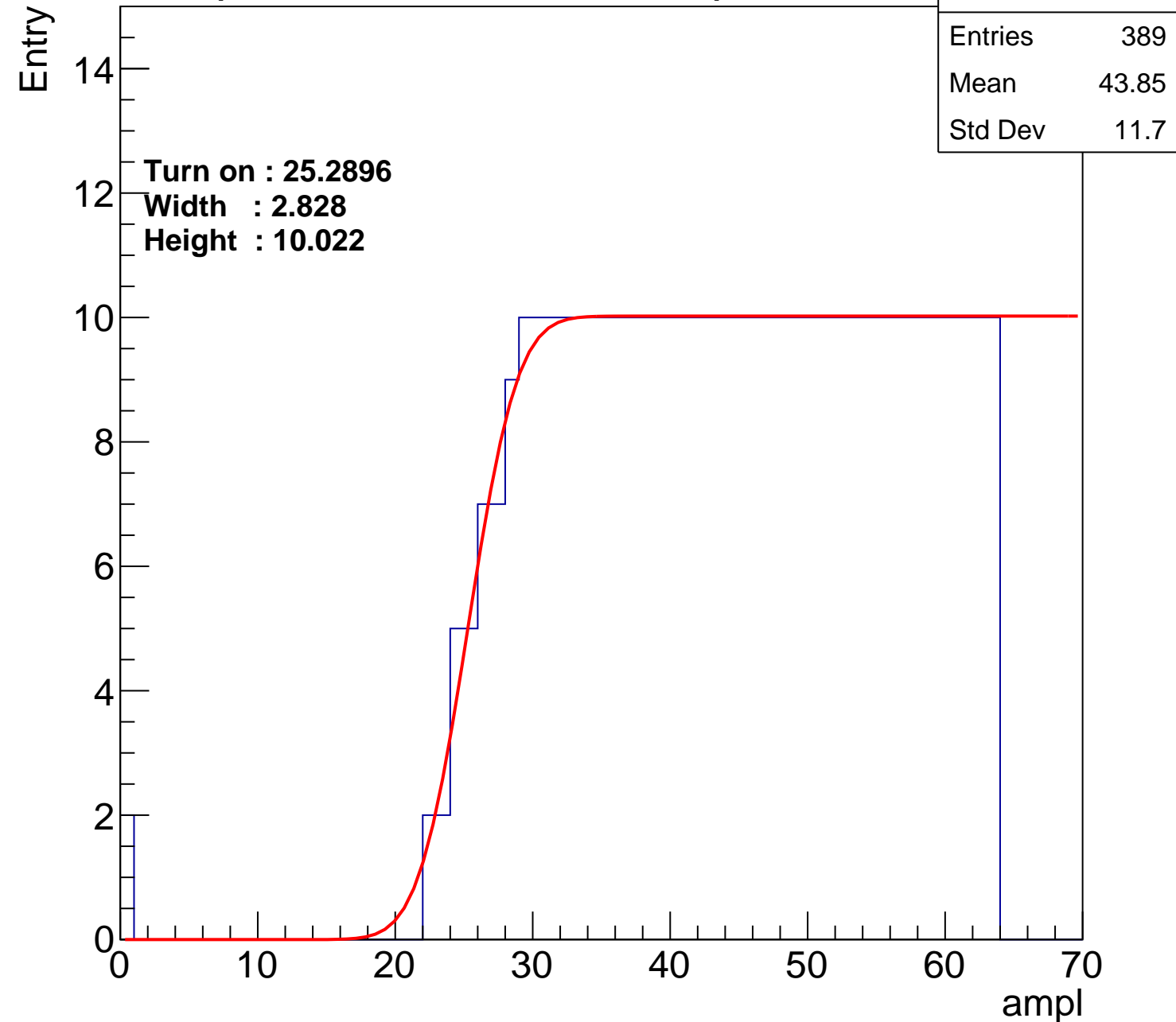
Width : 2.828

Height : 10.022

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L002S, U2-ch87

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	390
Mean	43.76
Std Dev	11.79

Turn on : 24.8156

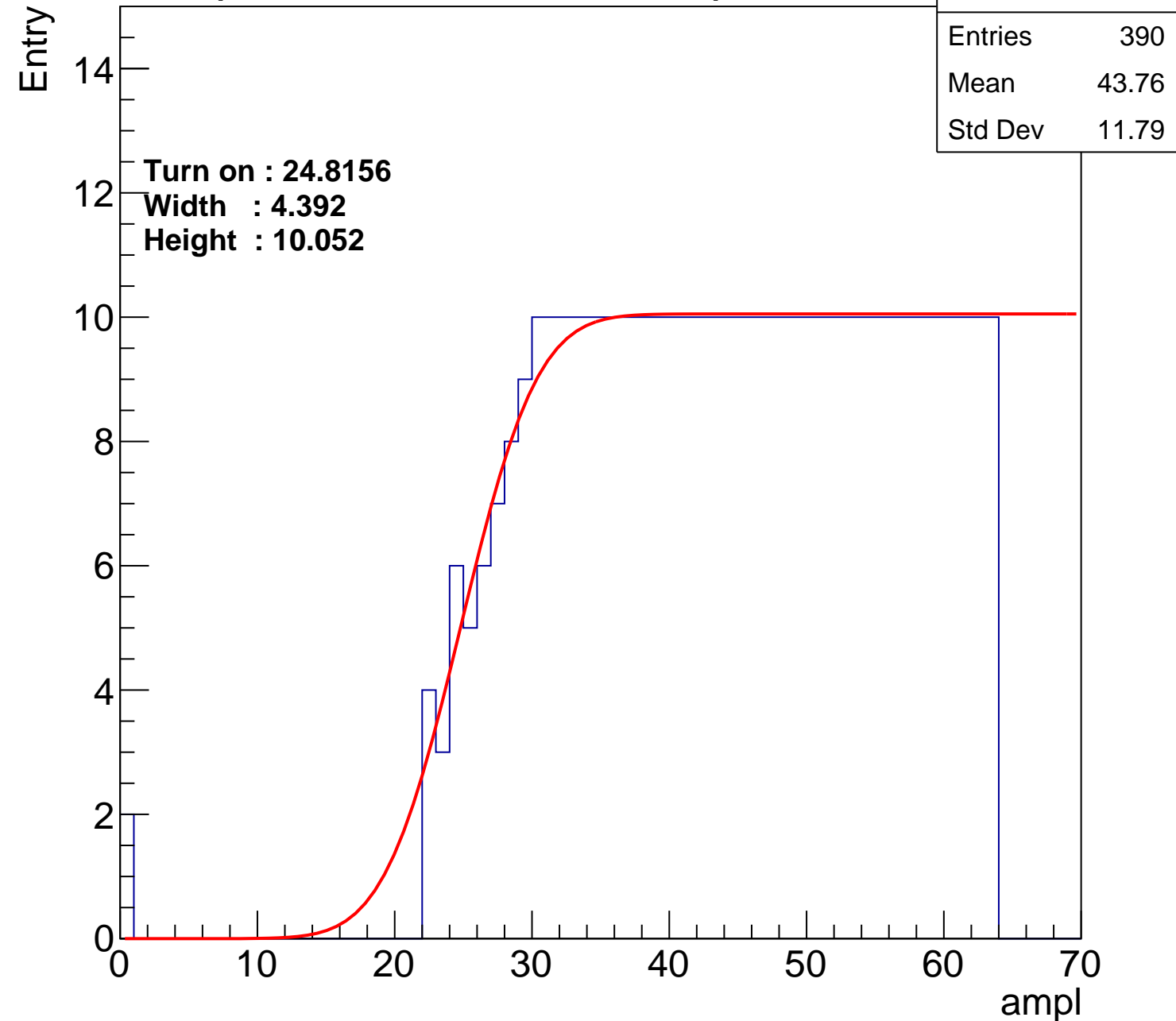
Width : 4.392

Height : 10.052

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch88

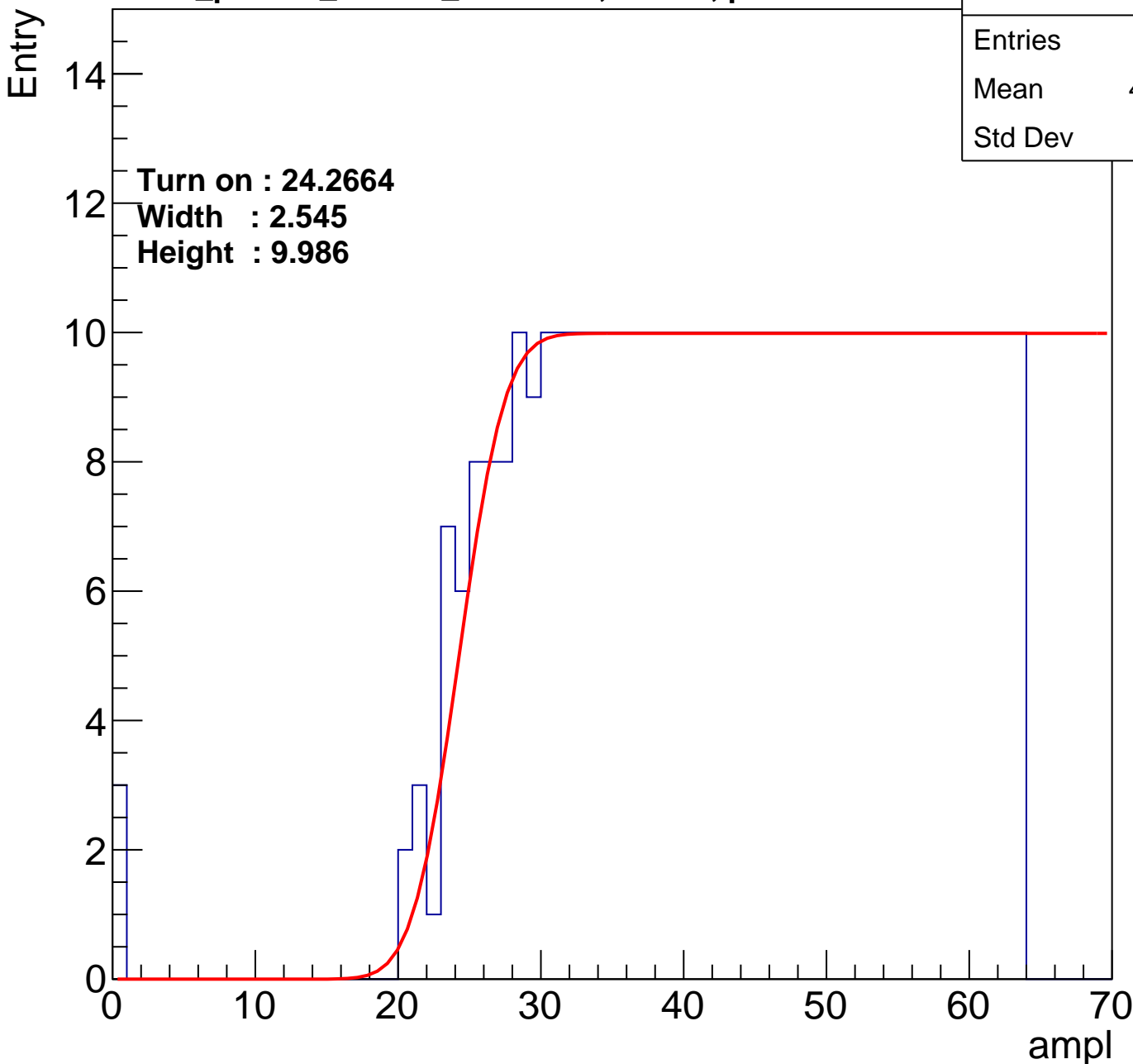
**calib\_packv5\_042523\_0143.root, FC#10, port B3**

Entries	405
Mean	42.98
Std Dev	12.3

**Turn on : 24.2664**

**Width : 2.545**

**Height : 9.986**



# B1L002S, U2-ch89

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	402
Mean	42.96
Std Dev	12.65

Turn on : 24.2202

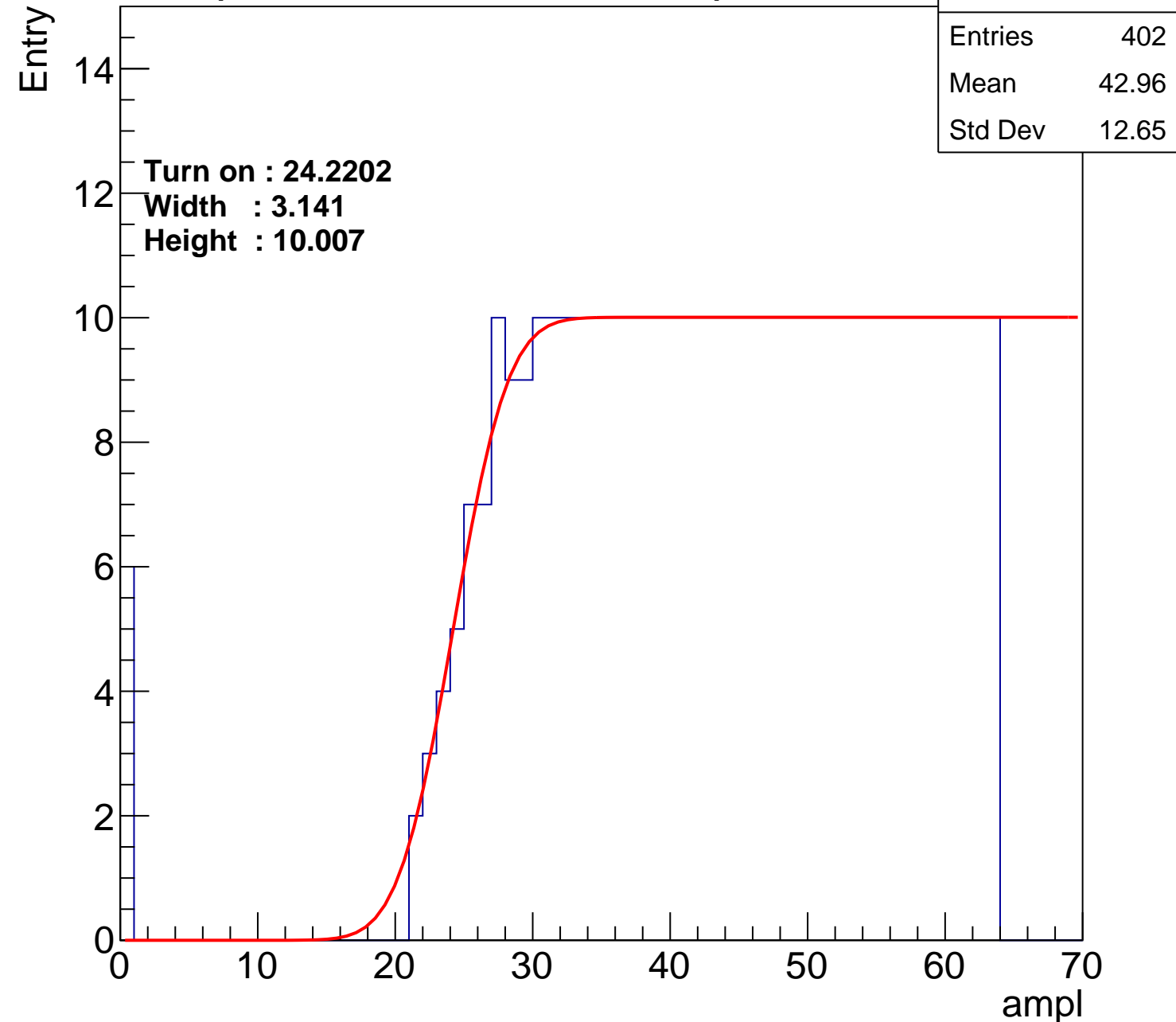
Width : 3.141

Height : 10.007

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch90

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	411
Mean	42.6
Std Dev	12.69

Turn on : 24.8359

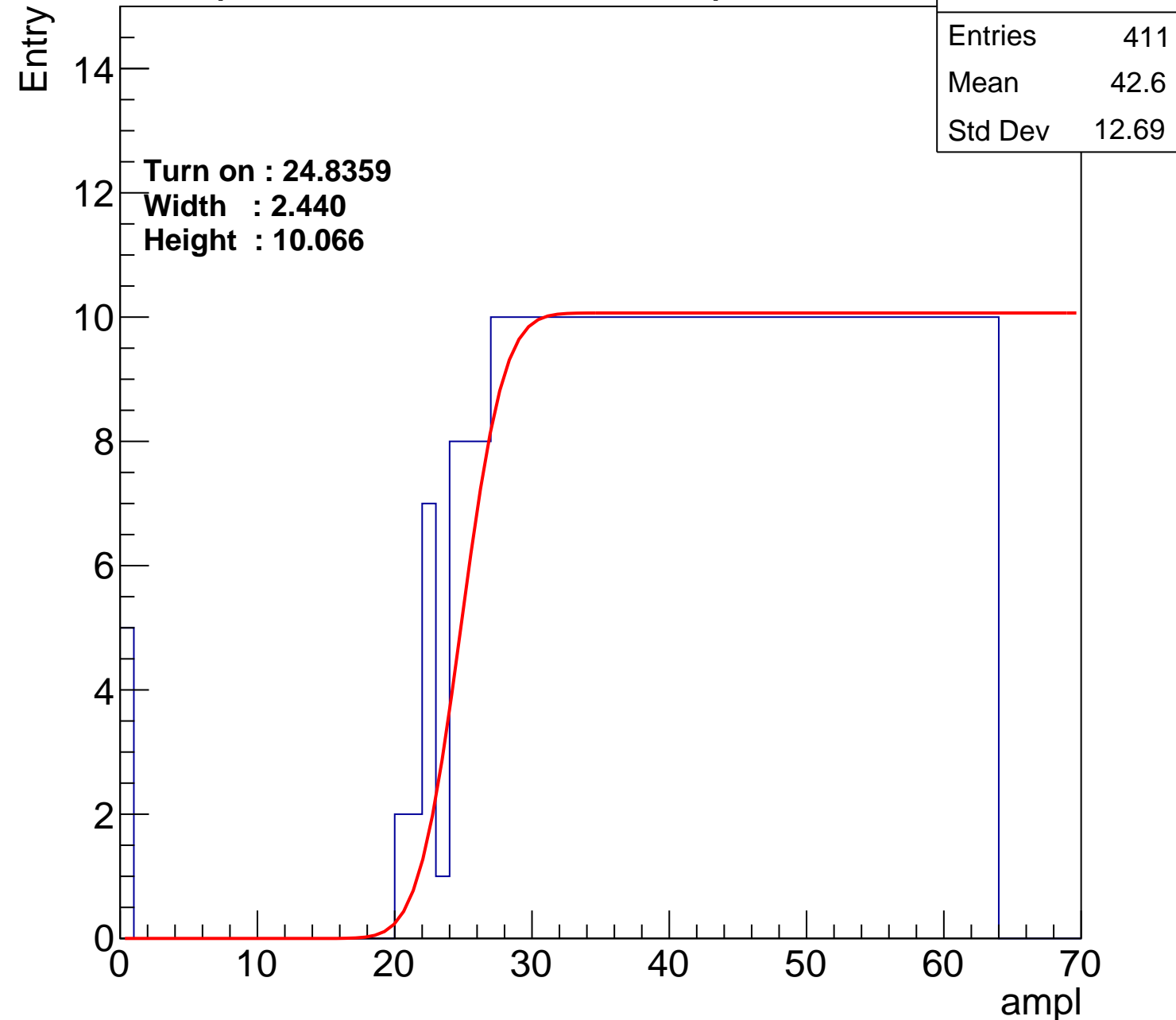
Width : 2.440

Height : 10.066

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch91

calib\_packv5\_042523\_0143.root, FC#10, port B3

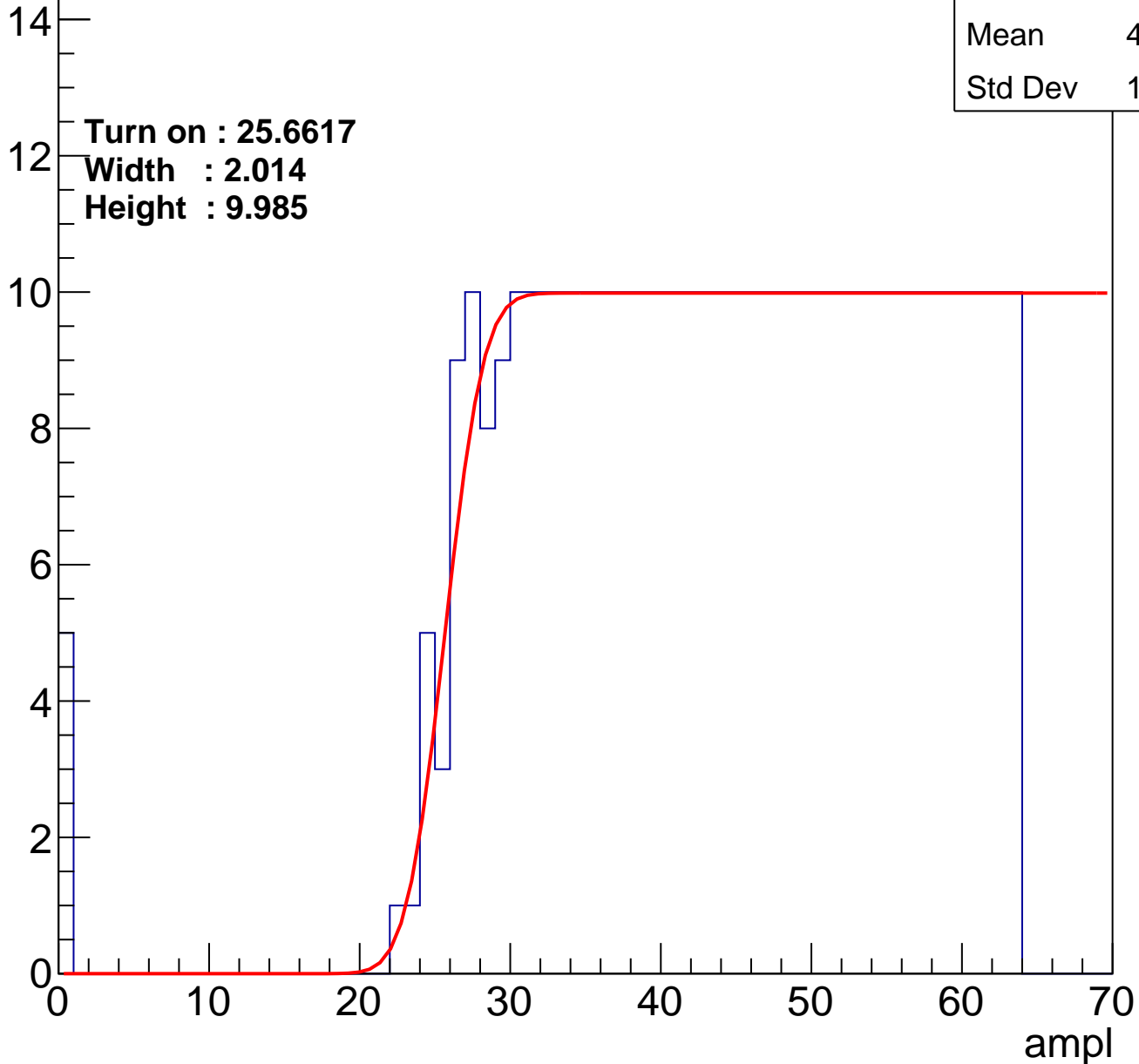
Entries	391
Mean	43.58
Std Dev	12.22

Turn on : 25.6617

Width : 2.014

Height : 9.985

Entry



# B1L002S, U2-ch92

calib\_packv5\_042523\_0143.root, FC#10, port B3

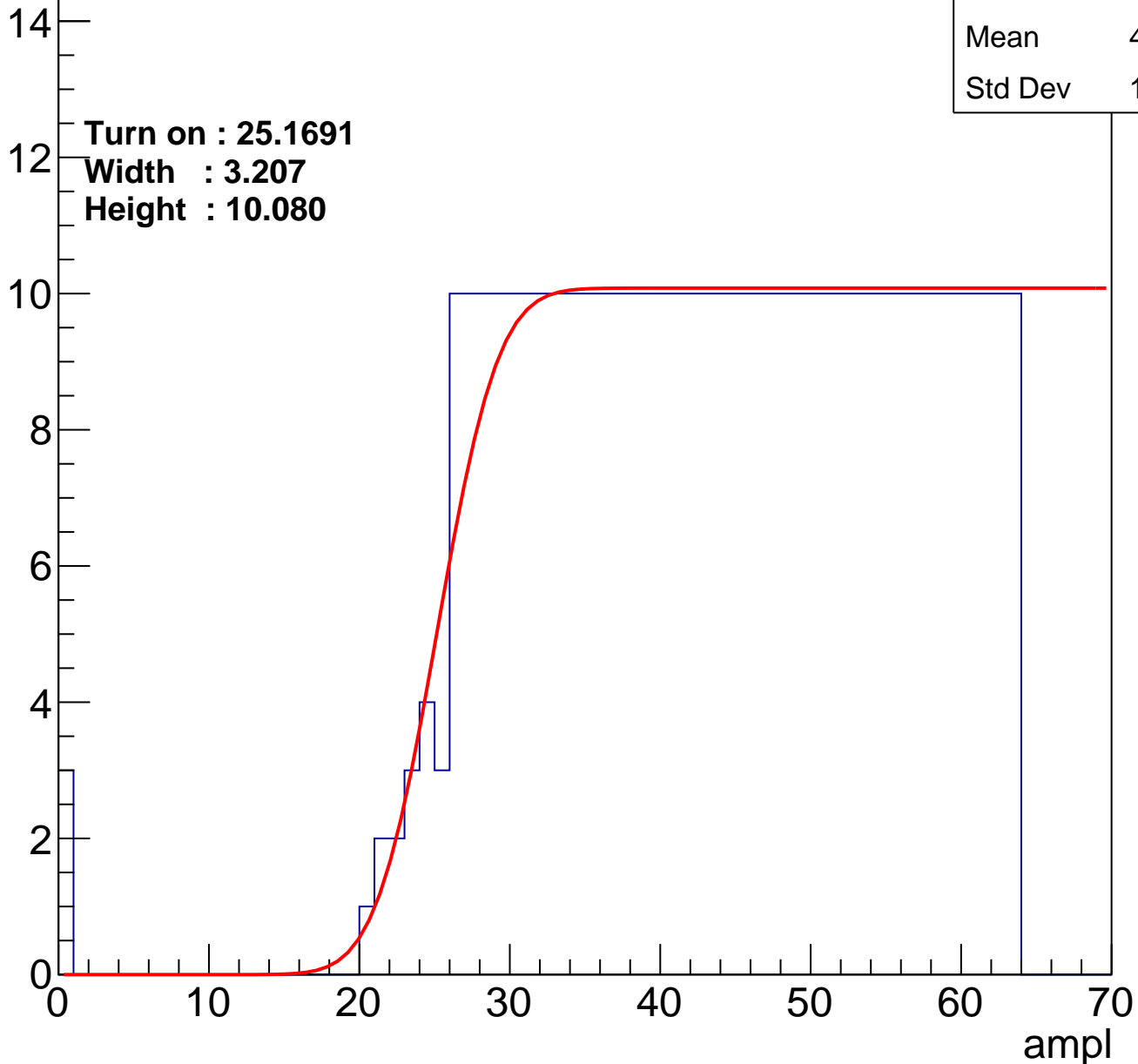
Entries	398
Mean	43.36
Std Dev	12.08

Turn on : 25.1691

Width : 3.207

Height : 10.080

Entry



# B1L002S, U2-ch93

calib\_packv5\_042523\_0143.root, FC#10, port B3

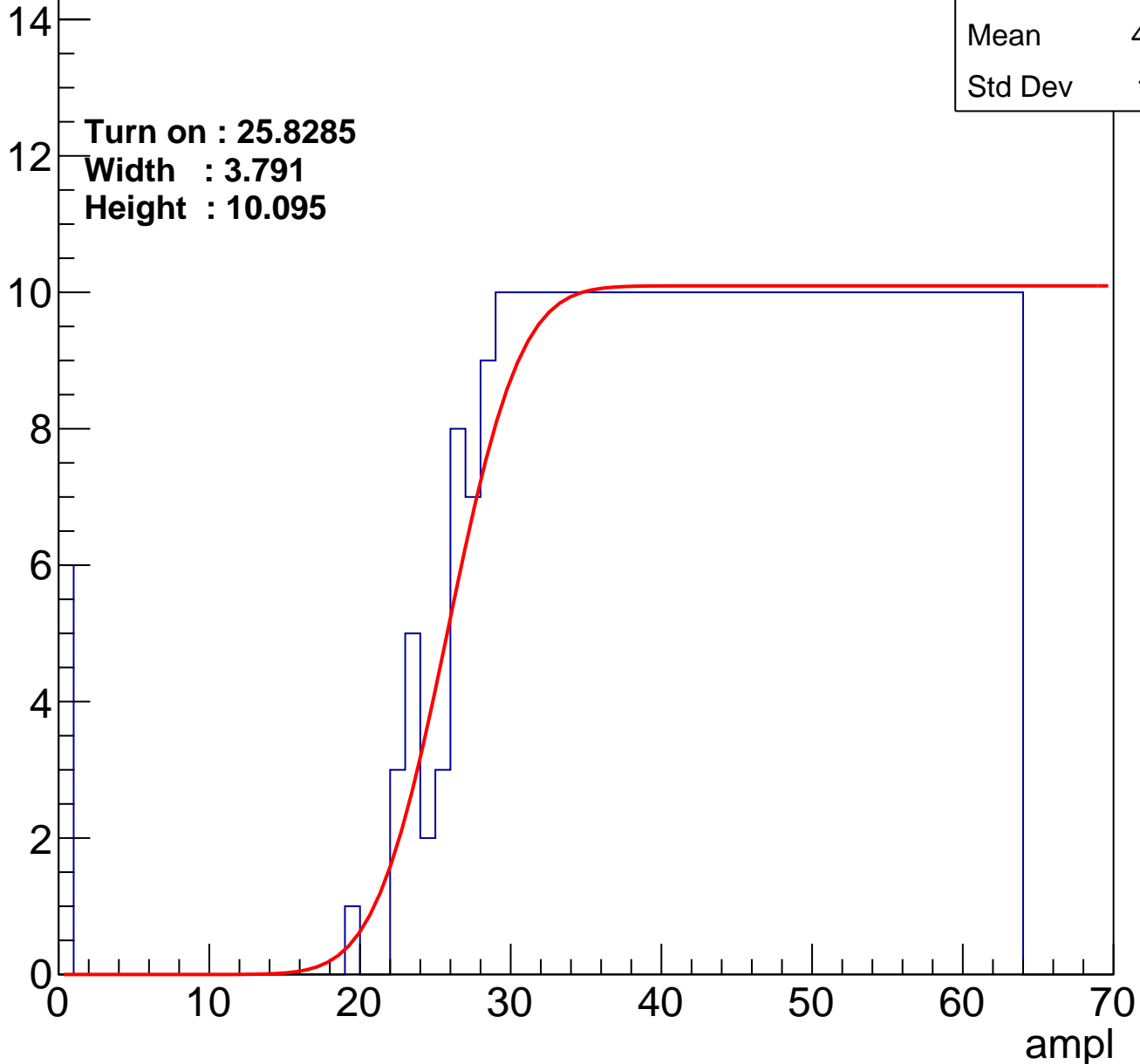
Entries	394
Mean	43.33
Std Dev	12.51

Turn on : 25.8285

Width : 3.791

Height : 10.095

Entry



B1L002S, U2-ch94

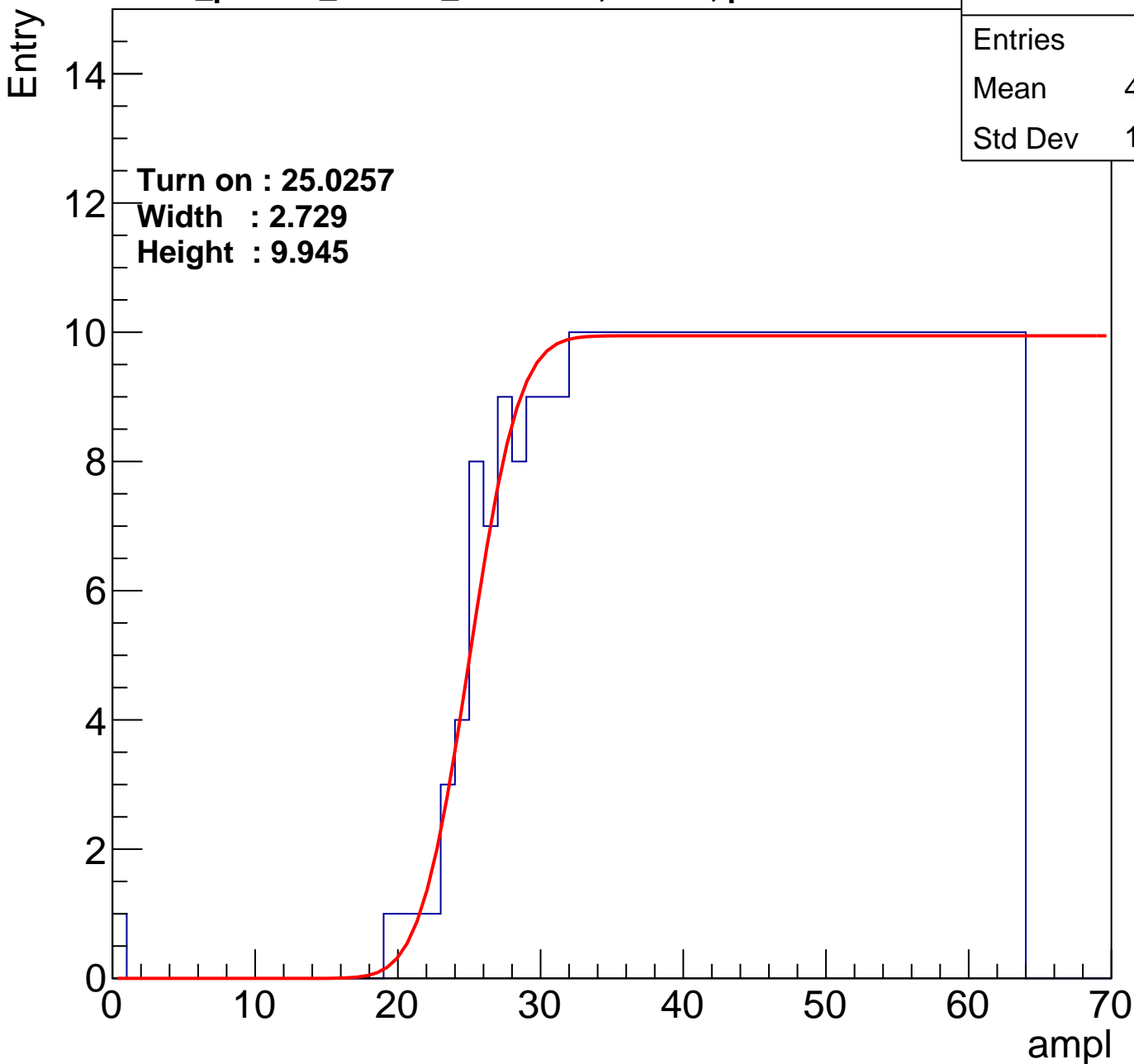
**calib\_packv5\_042523\_0143.root, FC#10, port B3**

Entries	391
Mean	43.75
Std Dev	11.68

**Turn on : 25.0257**

**Width : 2.729**

**Height : 9.945**





# B1L002S, U2-ch95

calib\_packv5\_042523\_0143.root, FC#10, port B3

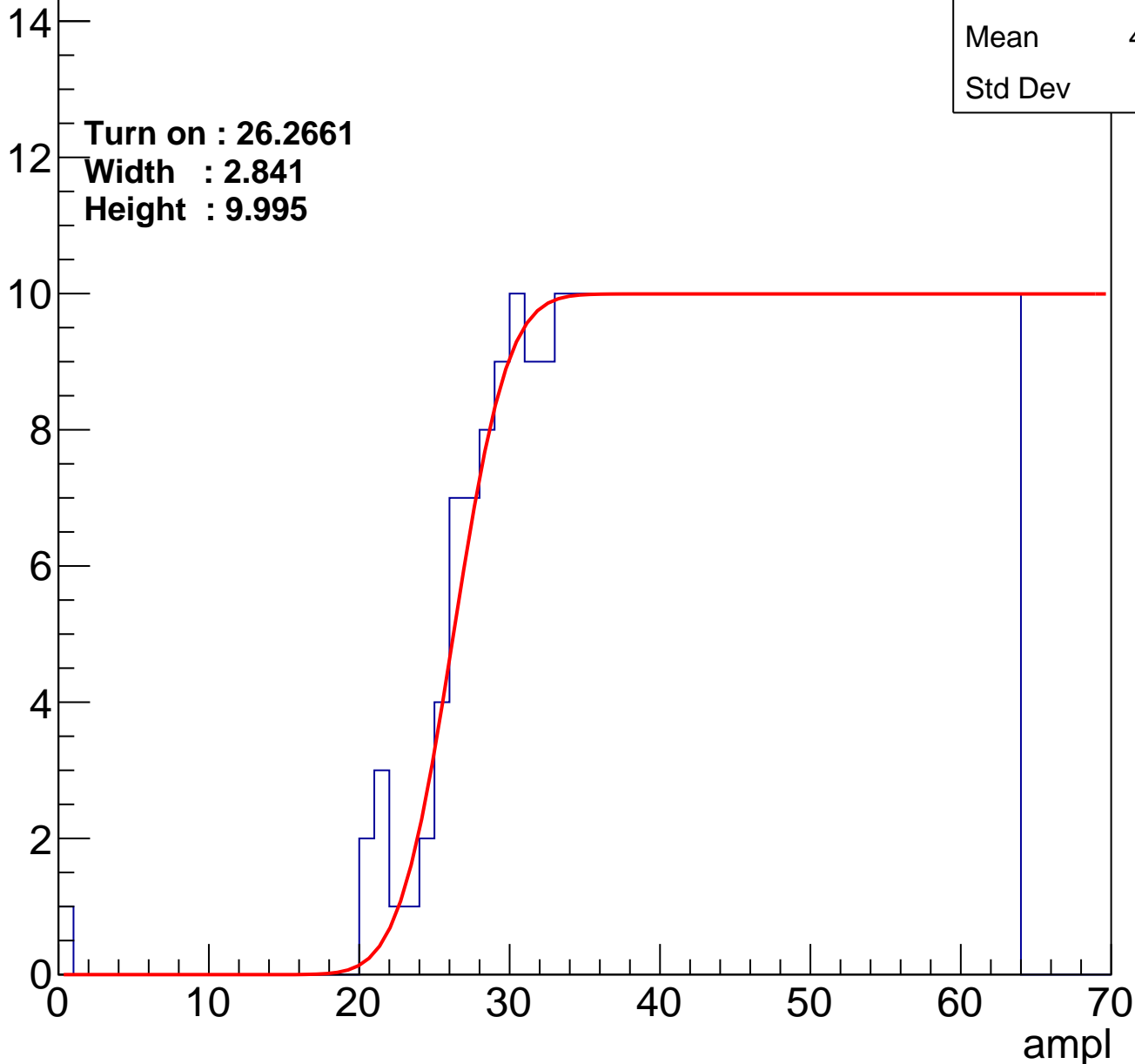
Entry

Entries	383
Mean	44.12
Std Dev	11.51

Turn on : 26.2661

Width : 2.841

Height : 9.995



# B1L002S, U2-ch96

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	383
Mean	44.14
Std Dev	11.56

Turn on : 25.4621

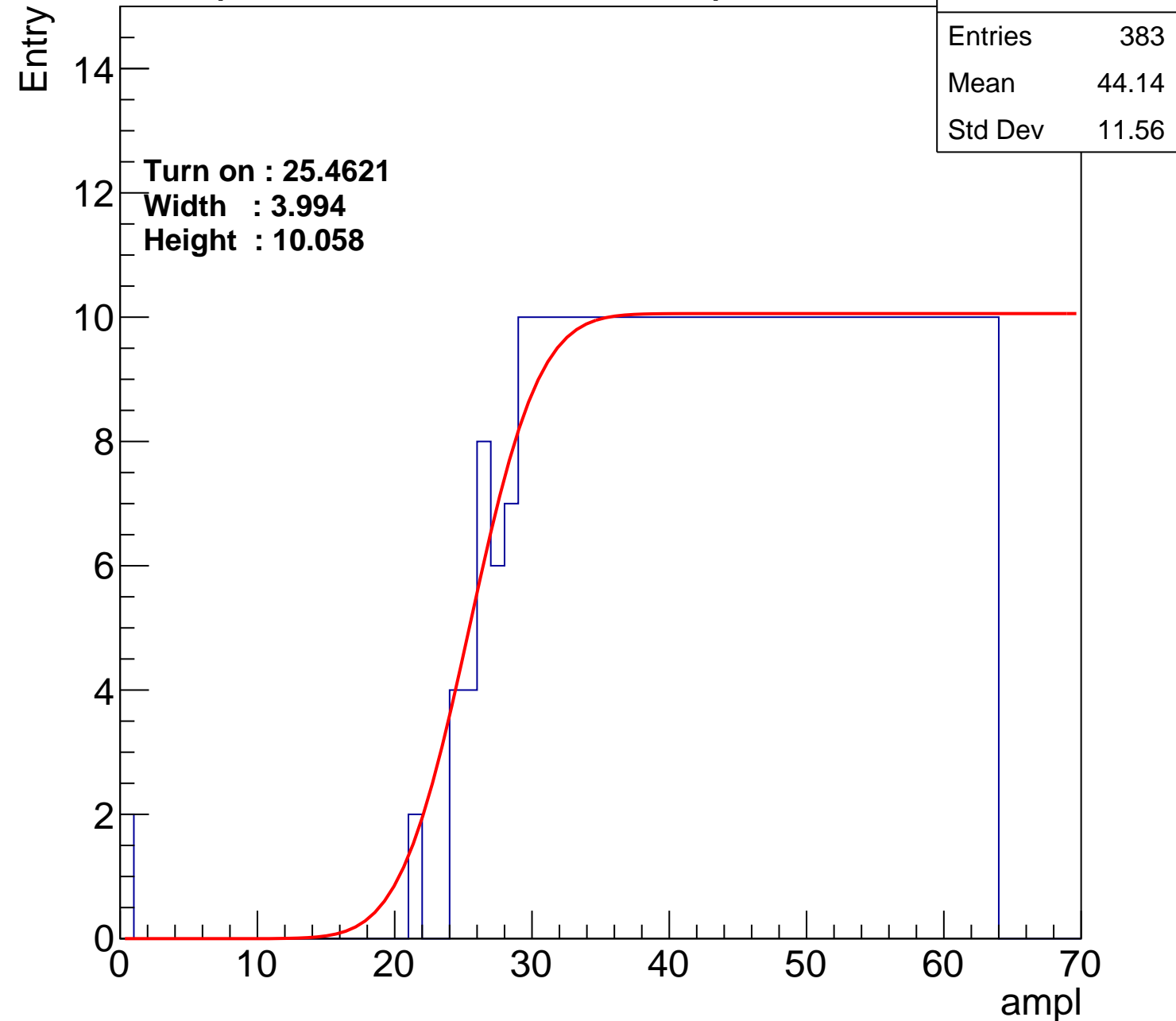
Width : 3.994

Height : 10.058

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch97

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	385
Mean	44.05
Std Dev	11.59

Turn on : 25.8745

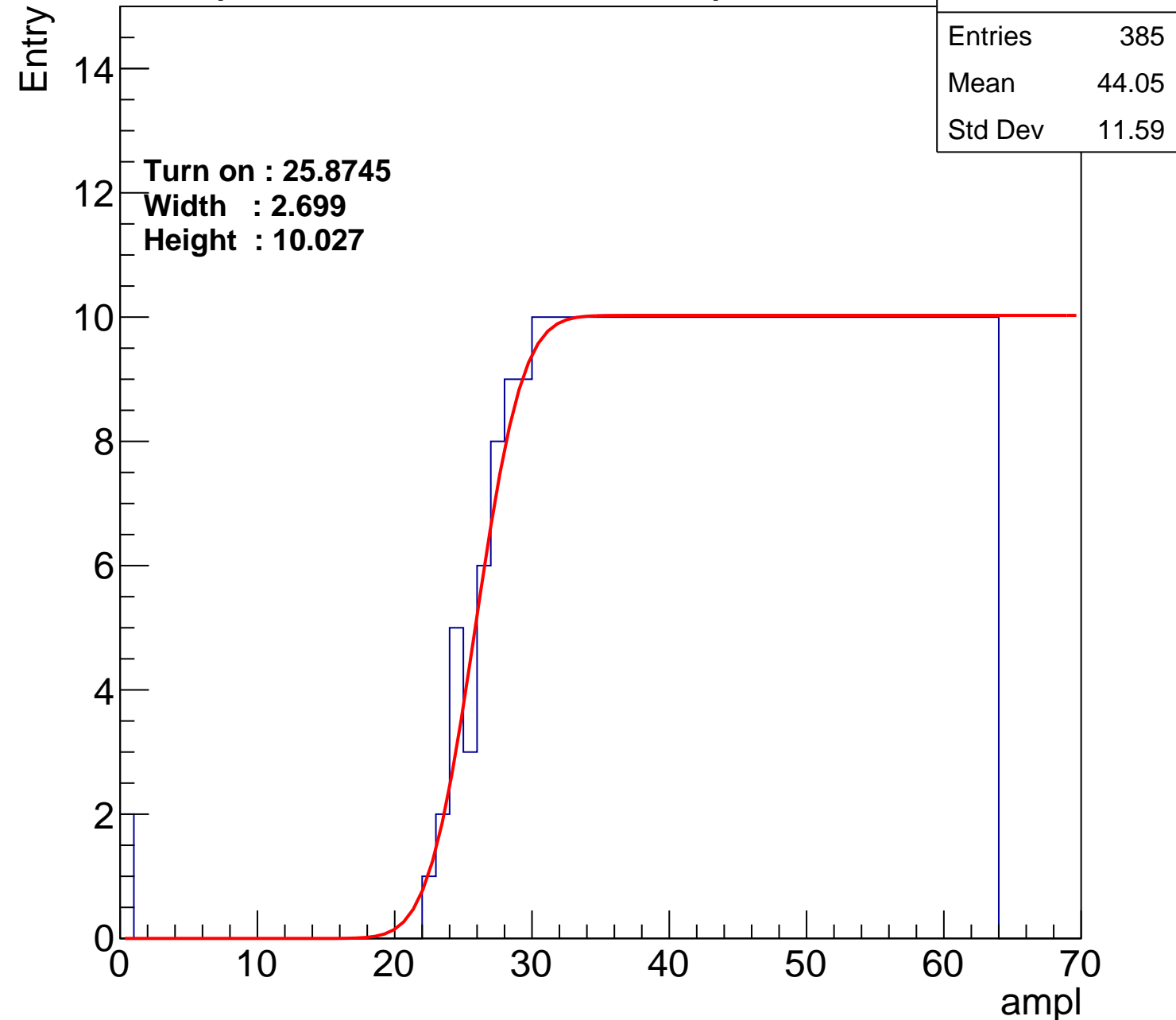
Width : 2.699

Height : 10.027

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch98

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	390
Mean	43.83
Std Dev	11.67

Turn on : 25.3035

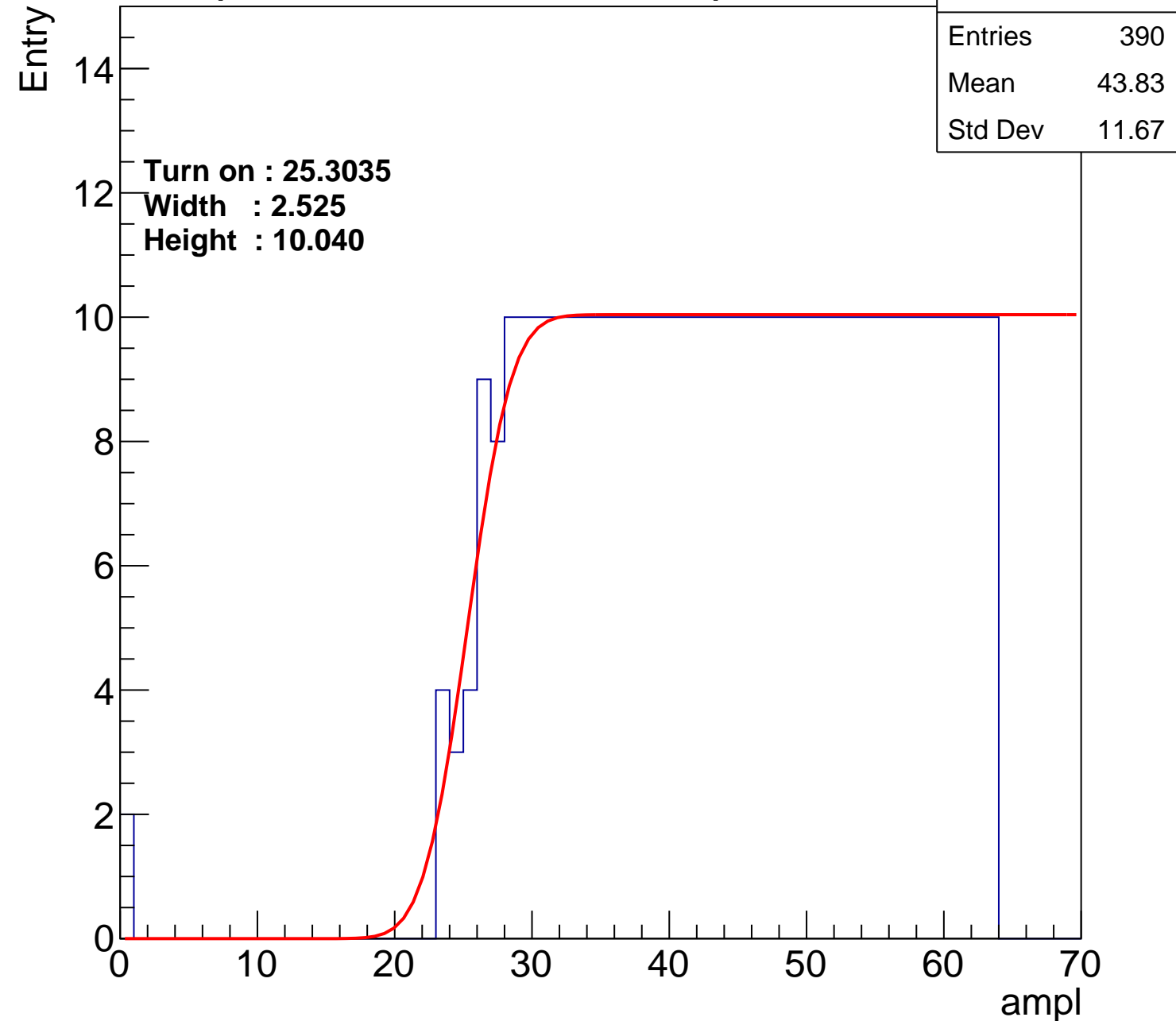
Width : 2.525

Height : 10.040

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch99

calib\_packv5\_042523\_0143.root, FC#10, port B3

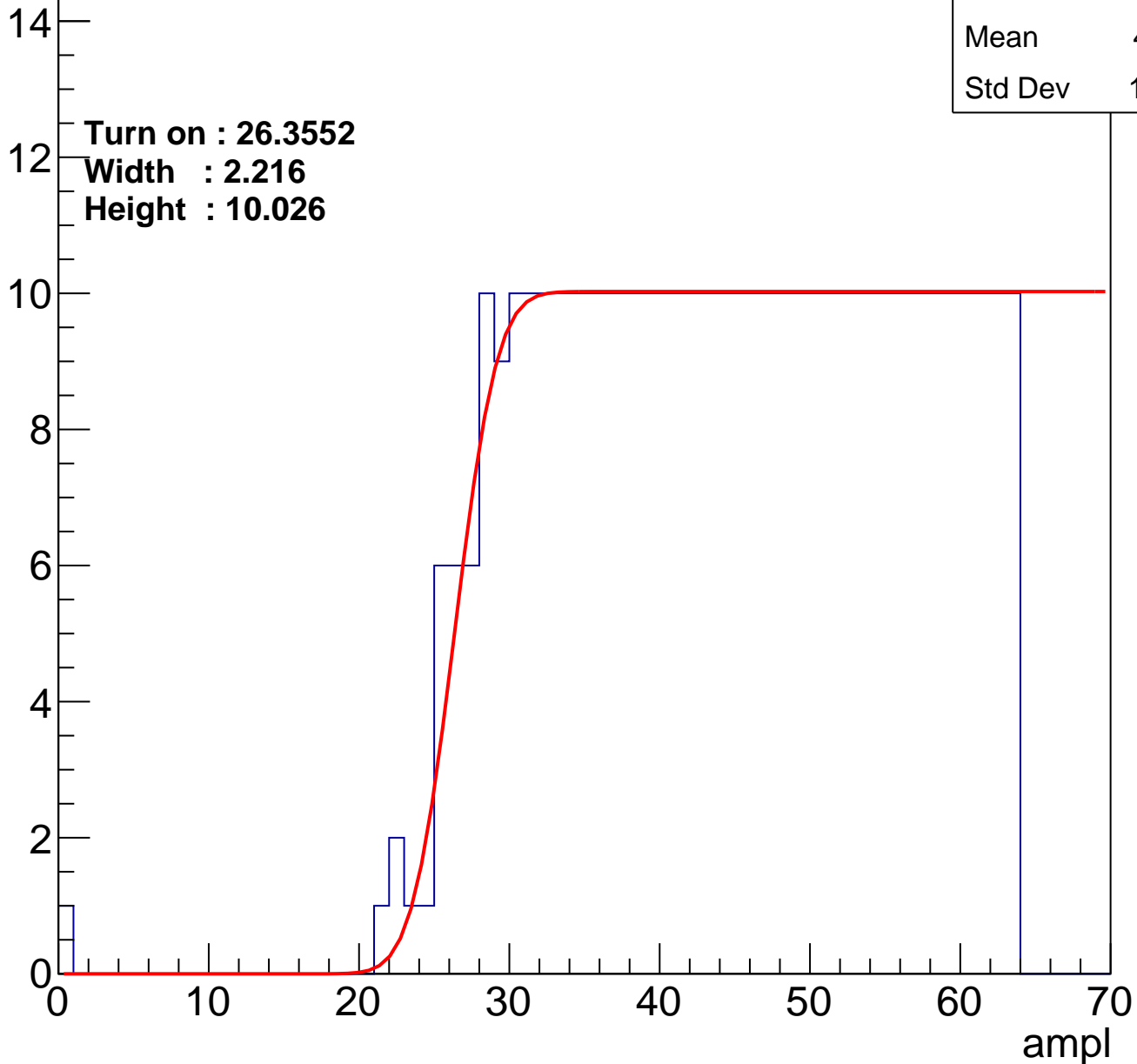
Entry

Entries	383
Mean	44.21
Std Dev	11.37

Turn on : 26.3552

Width : 2.216

Height : 10.026



# B1L002S, U2-ch100

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	394
Mean	43.46
Std Dev	12.19

Turn on : 25.4906

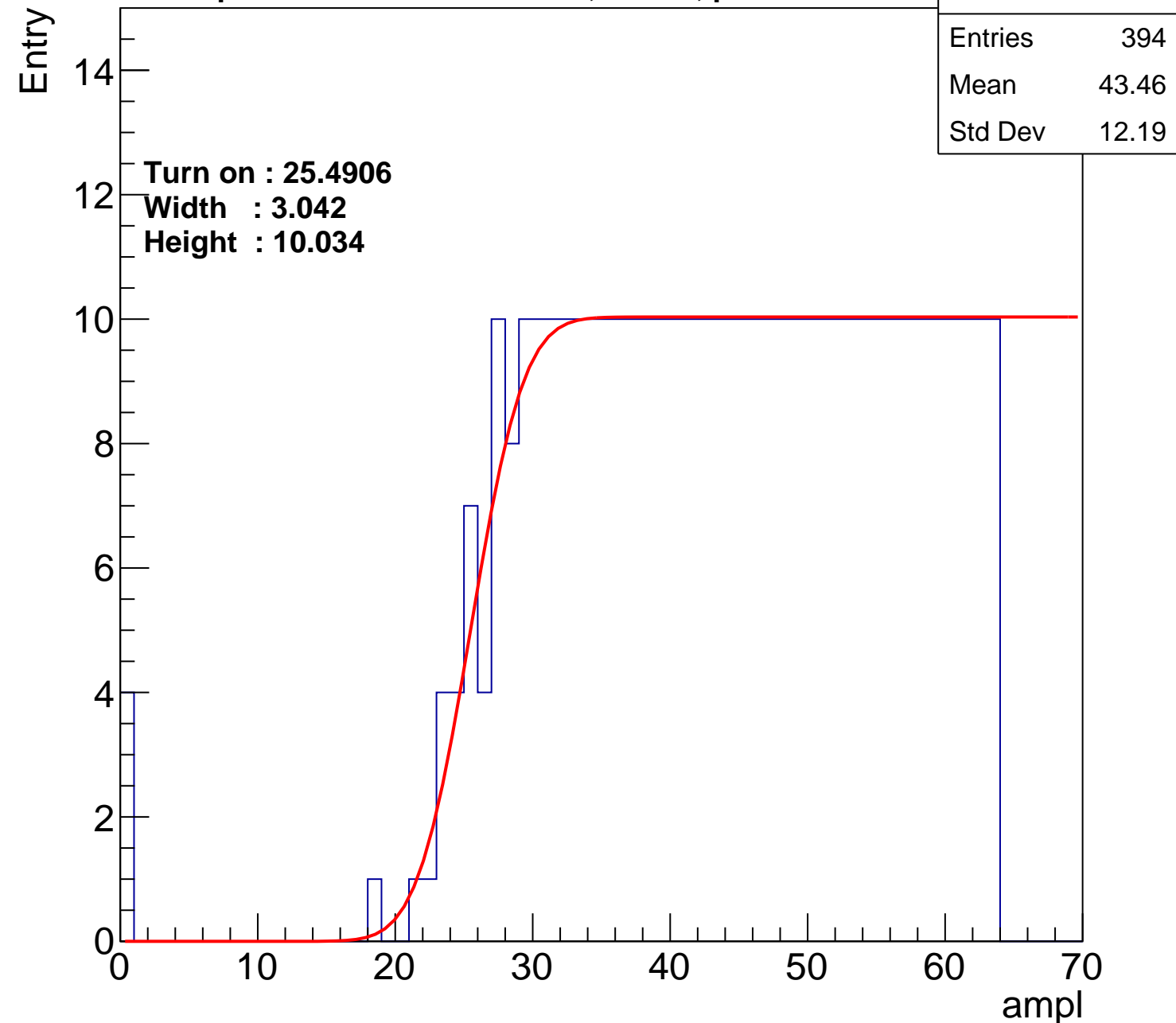
Width : 3.042

Height : 10.034

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch101

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	393
Mean	43.45
Std Dev	12.31

Turn on : 25.3761

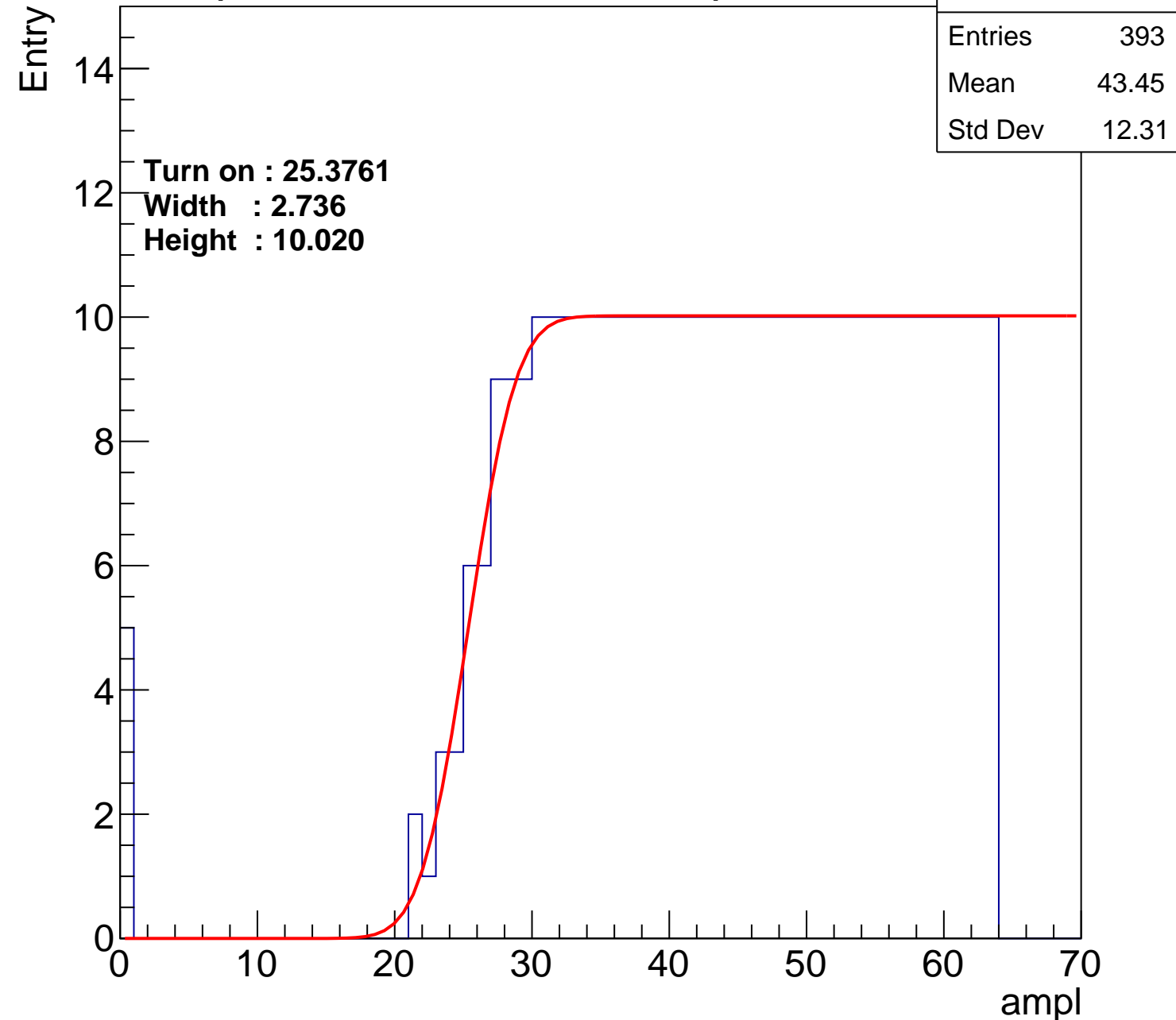
Width : 2.736

Height : 10.020

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch102

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	398
Mean	43.44
Std Dev	11.83

Turn on : 25.2467

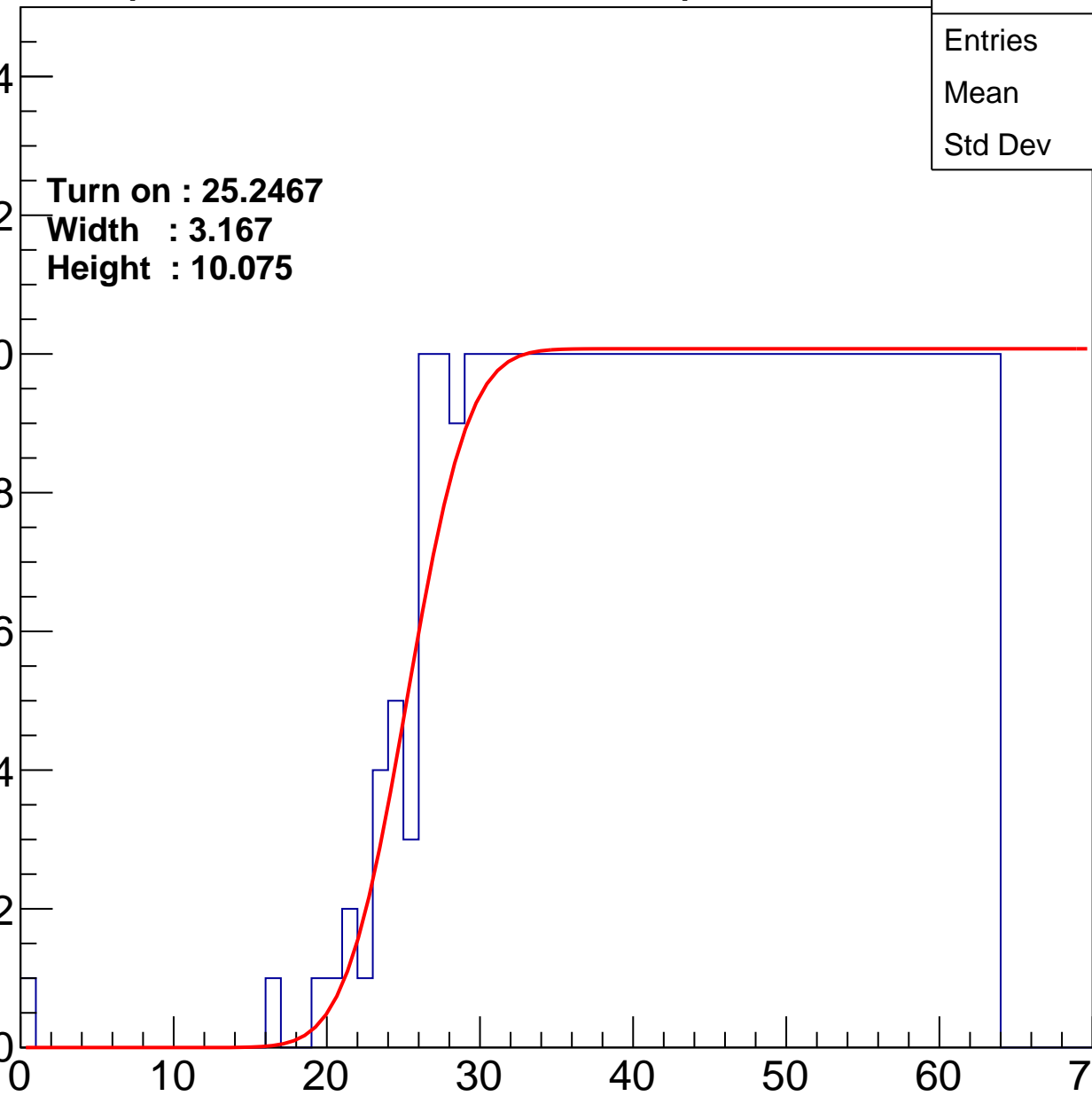
Width : 3.167

Height : 10.075

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L002S, U2-ch103

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	394
Mean	43.43
Std Dev	12.23

Turn on : 25.3908

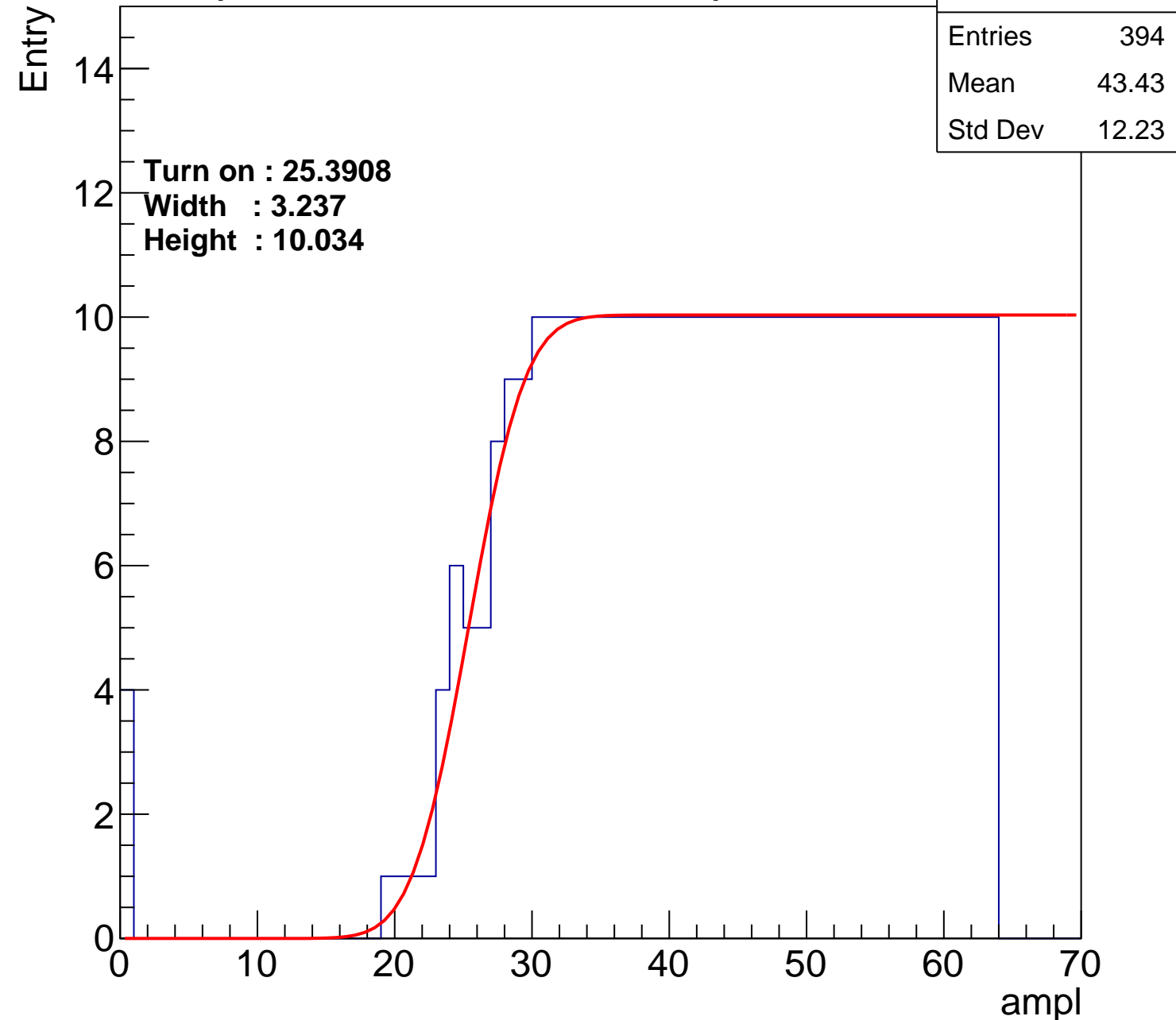
Width : 3.237

Height : 10.034

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch104

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	377
Mean	44.32
Std Dev	11.73

Turn on : 26.7846

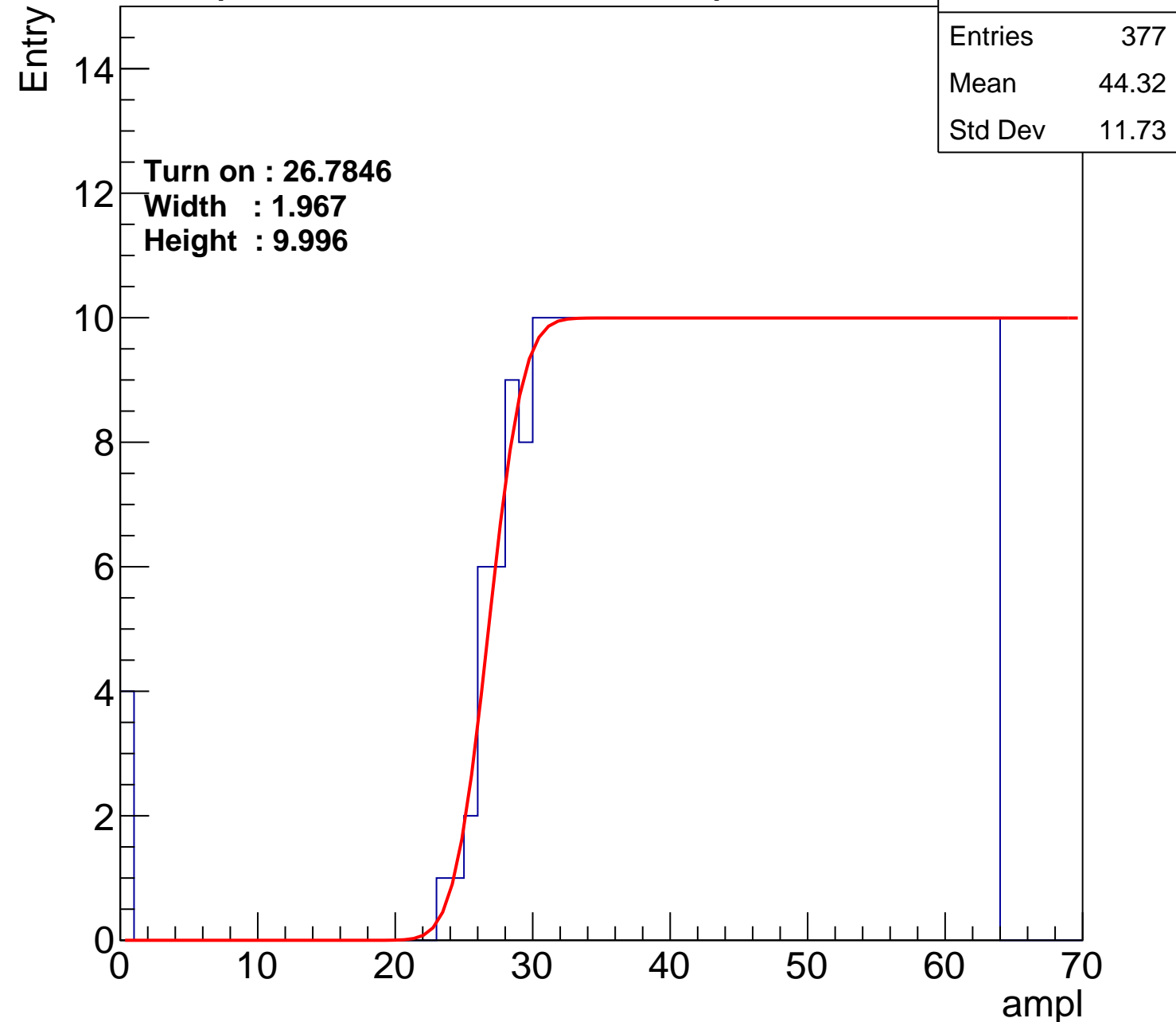
Width : 1.967

Height : 9.996

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch105

calib\_packv5\_042523\_0143.root, FC#10, port B3

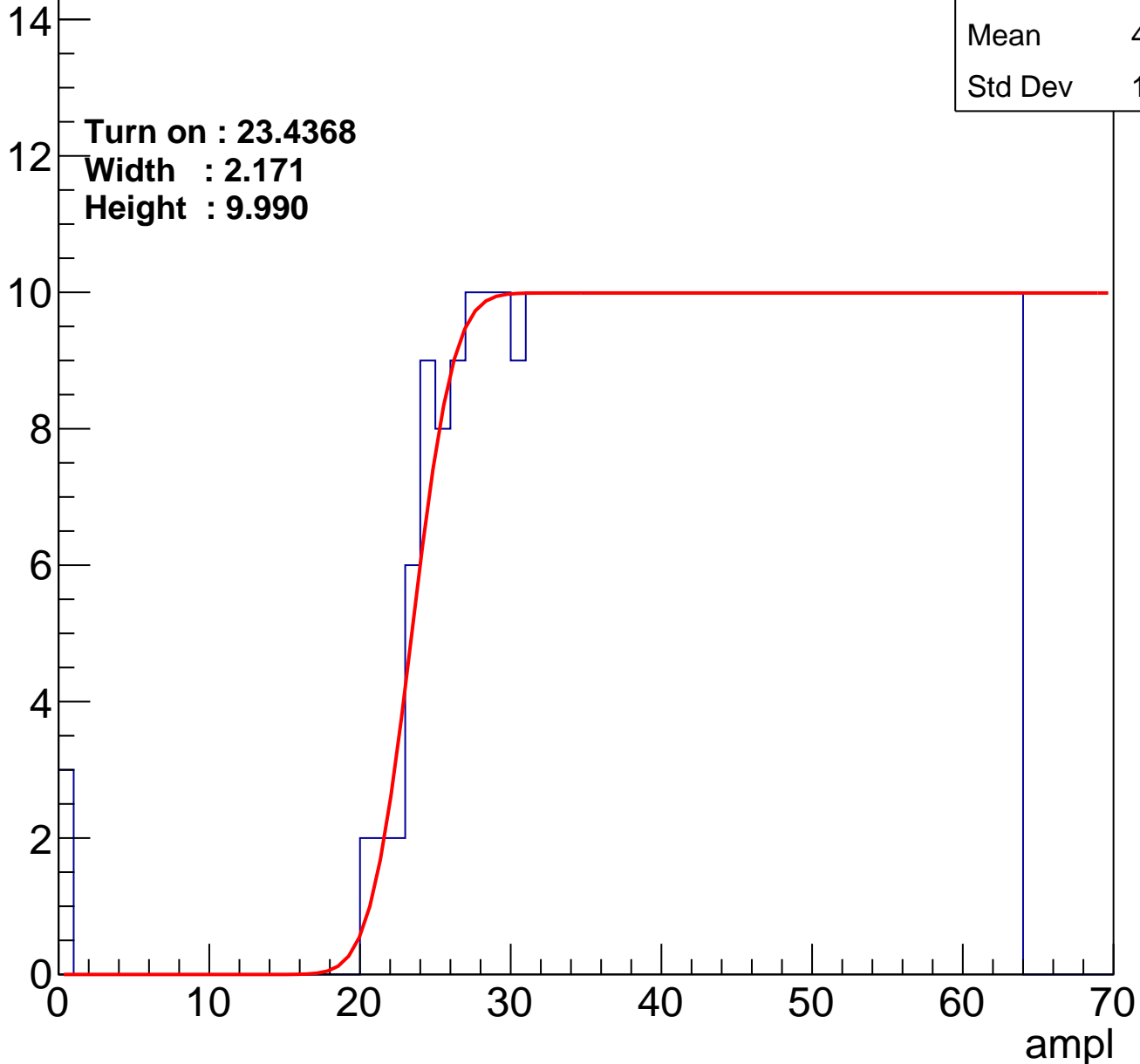
Entries	410
Mean	42.77
Std Dev	12.37

Turn on : 23.4368

Width : 2.171

Height : 9.990

Entry



# B1L002S, U2-ch106

calib\_packv5\_042523\_0143.root, FC#10, port B3

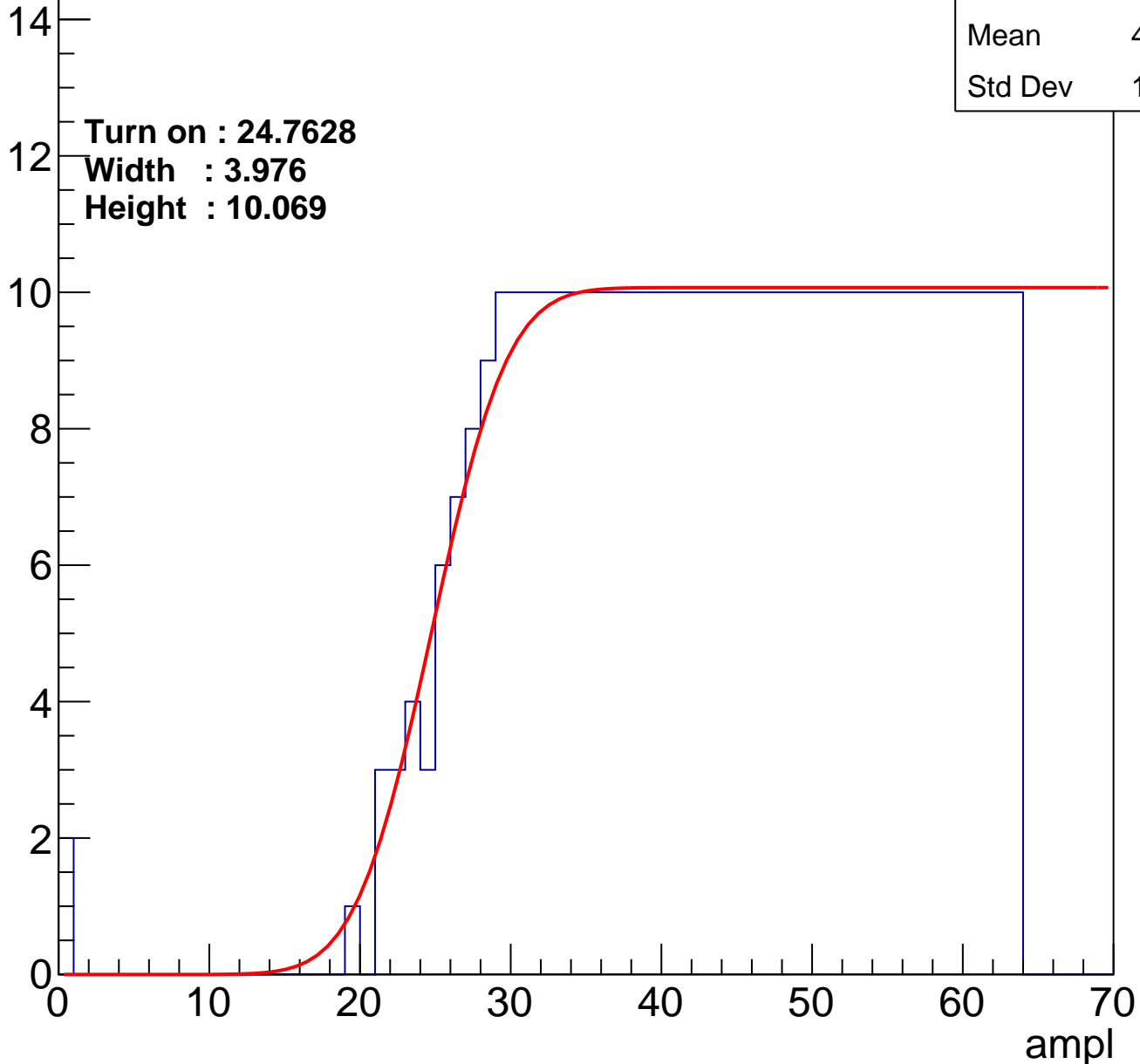
Entries	396
Mean	43.46
Std Dev	11.95

Turn on : 24.7628

Width : 3.976

Height : 10.069

Entry



# B1L002S, U2-ch107

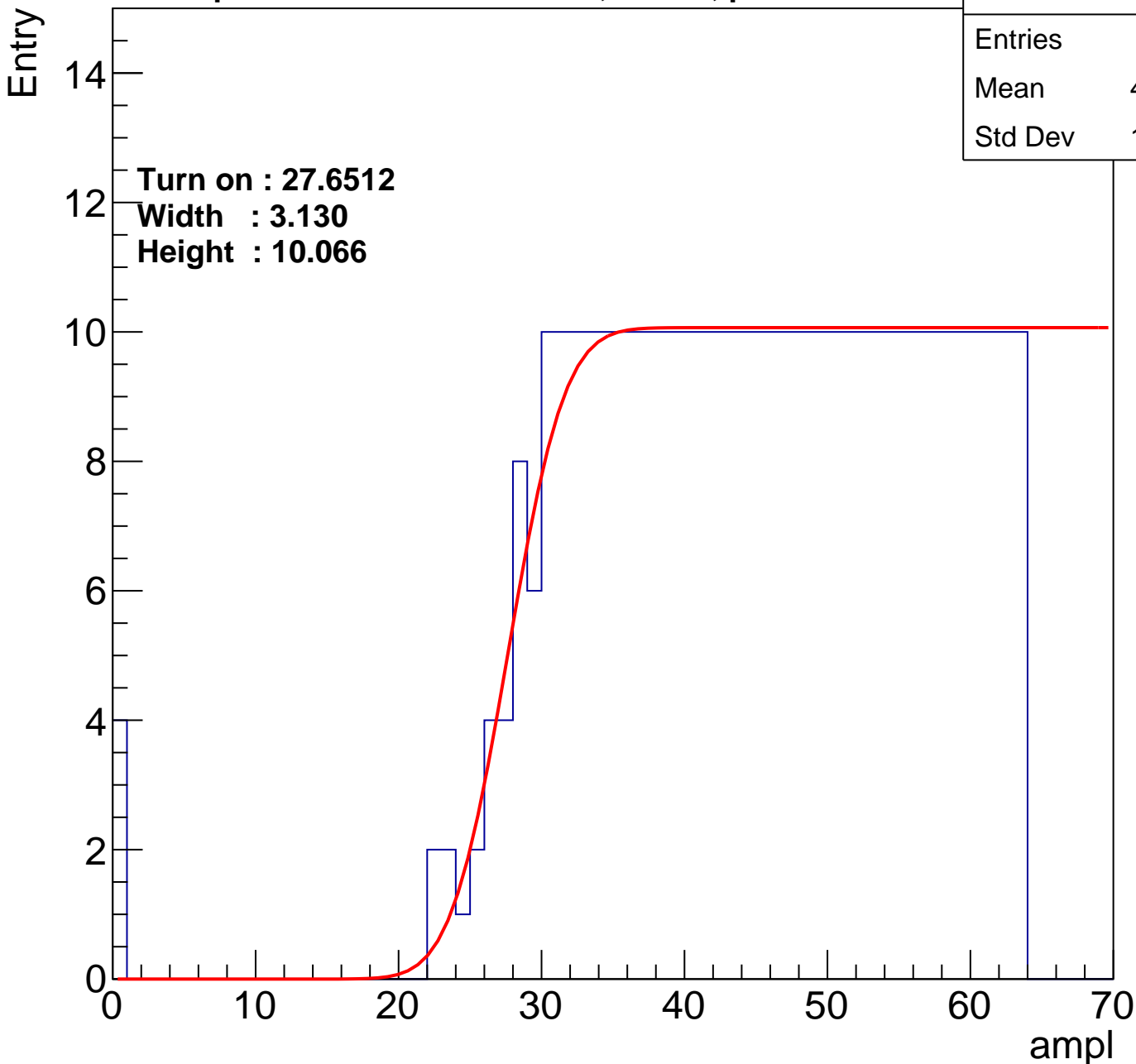
calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	373
Mean	44.46
Std Dev	11.73

Turn on : 27.6512

Width : 3.130

Height : 10.066



# B1L002S, U2-ch108

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	382
Mean	44.05
Std Dev	11.89

Turn on : 26.1606

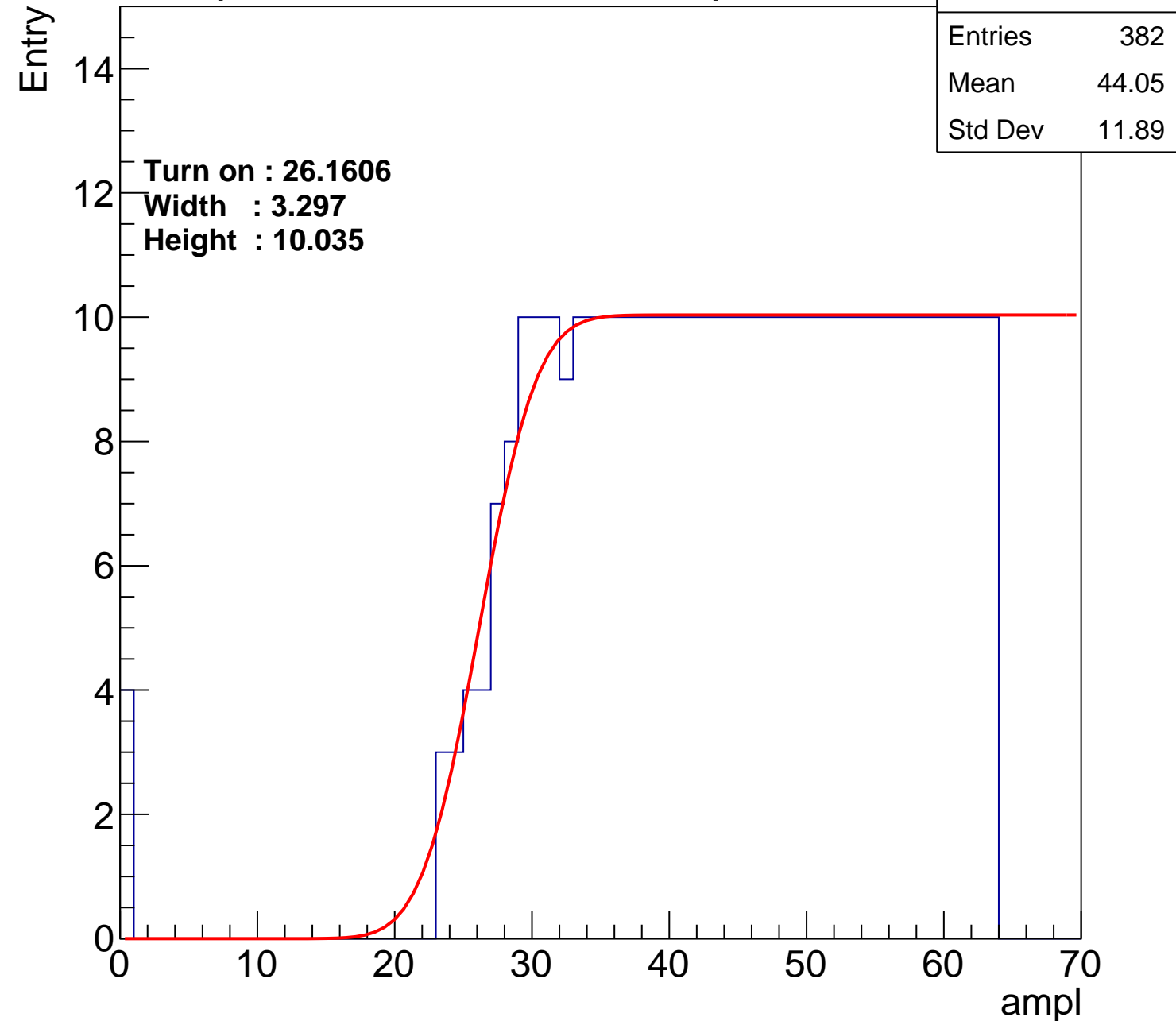
Width : 3.297

Height : 10.035

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch109

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	387
Mean	43.94
Std Dev	11.65

Turn on : 25.7144

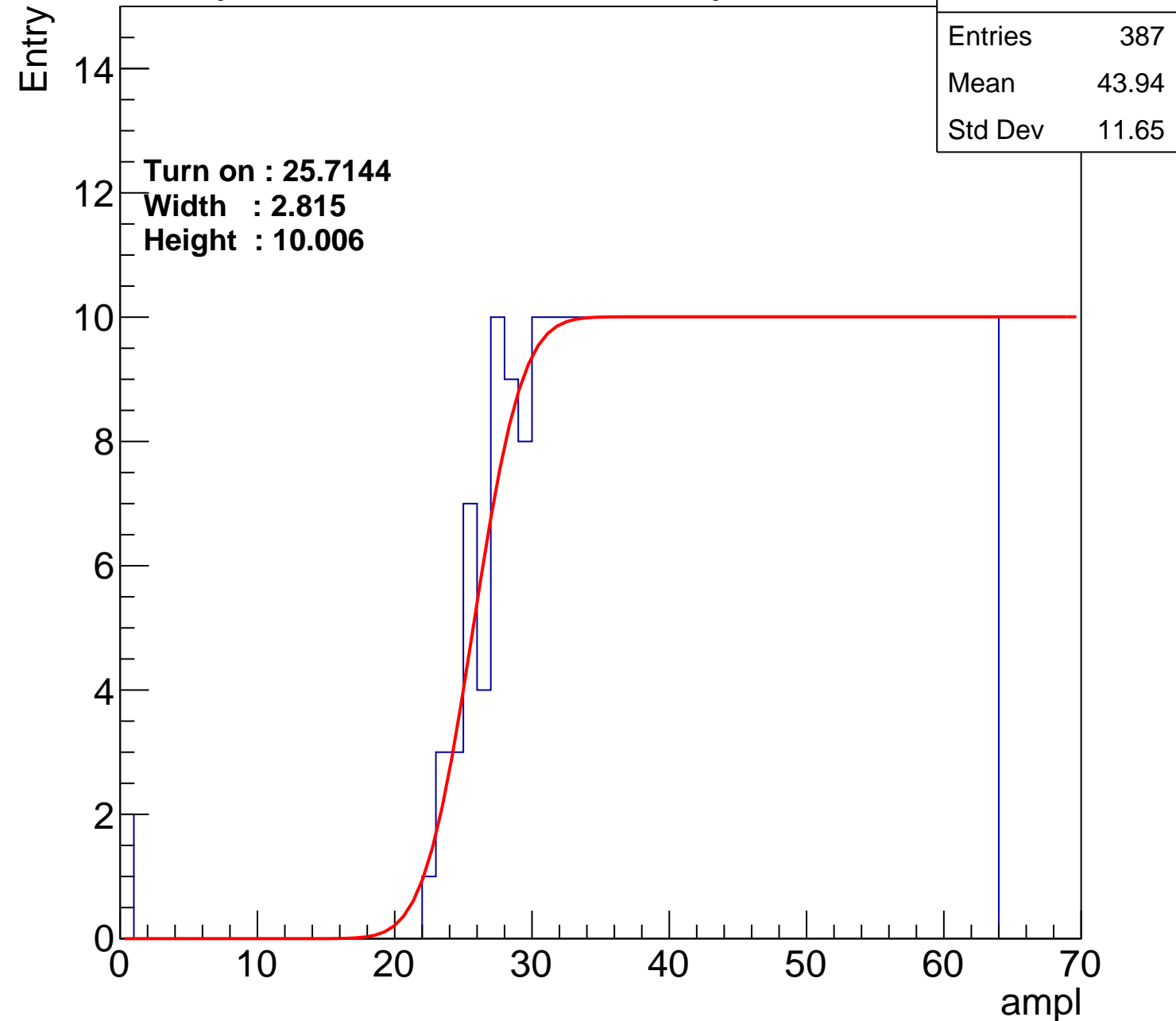
Width : 2.815

Height : 10.006

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch110

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	389
Mean	43.78
Std Dev	11.88

Turn on : 25.5585

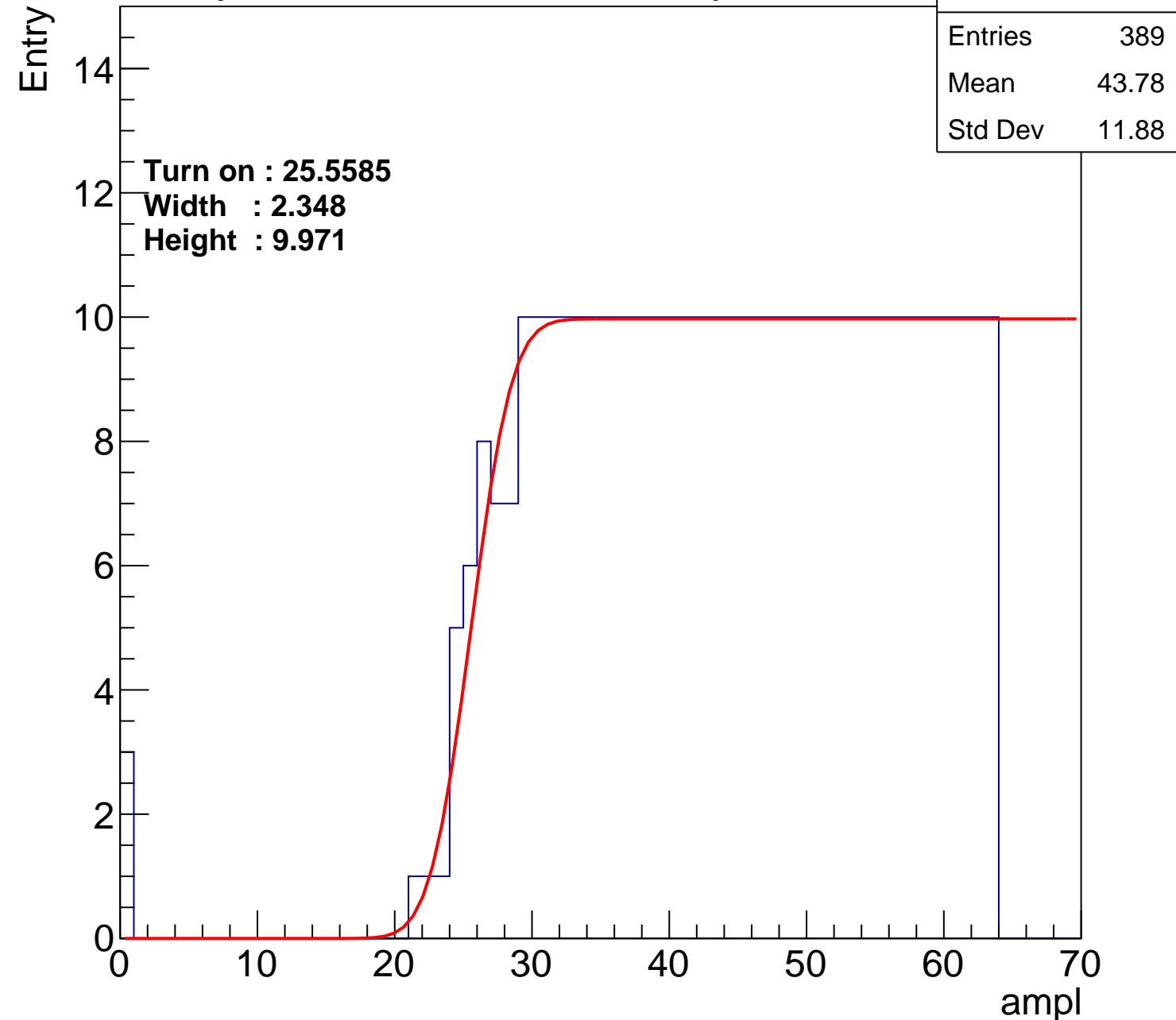
Width : 2.348

Height : 9.971

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L002S, U2-ch111

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	396
Mean	43.51
Std Dev	11.88

Turn on : 25.0149

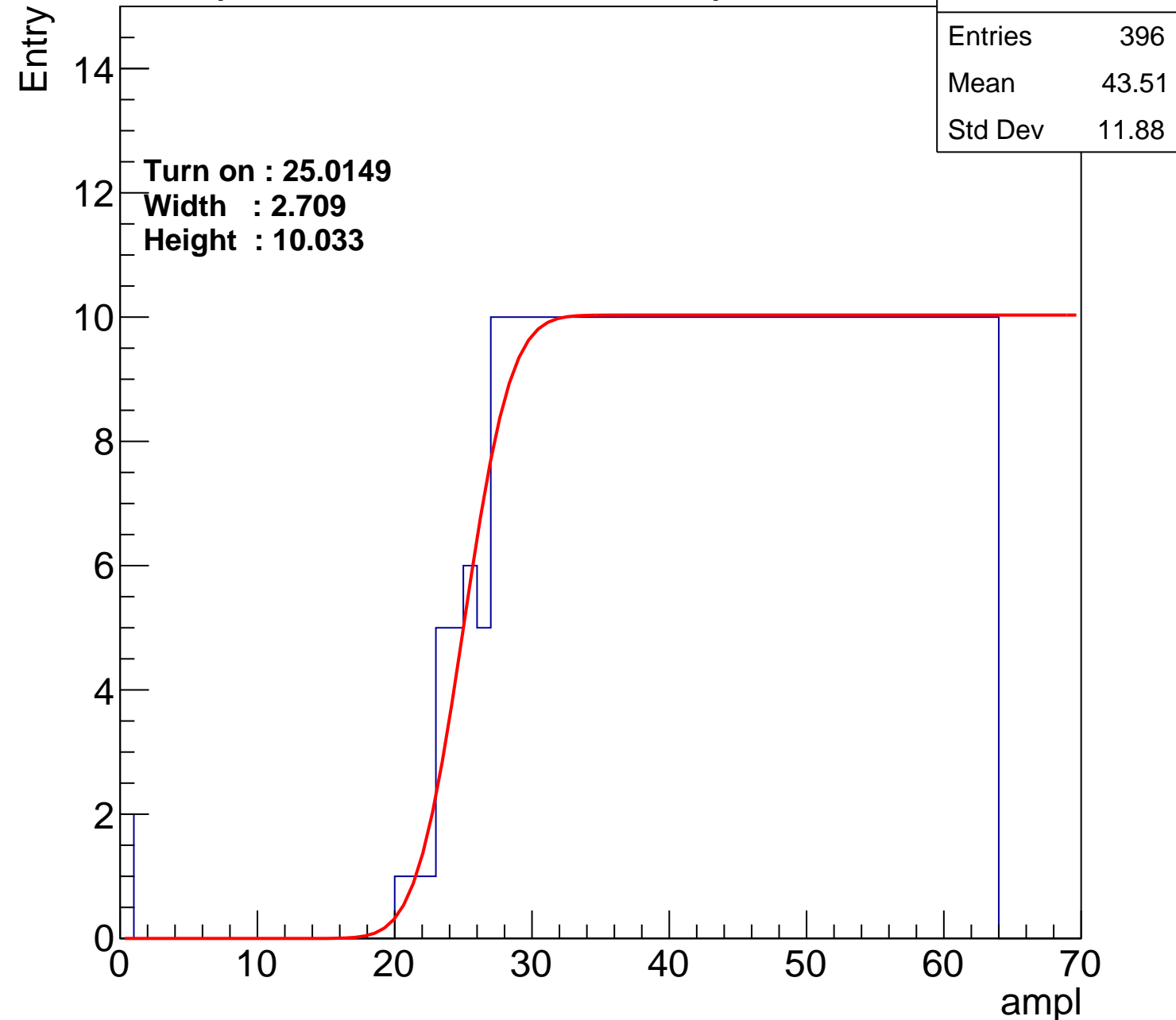
Width : 2.709

Height : 10.033

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch112

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	367
Mean	44.93
Std Dev	11.05

Turn on : 26.7734

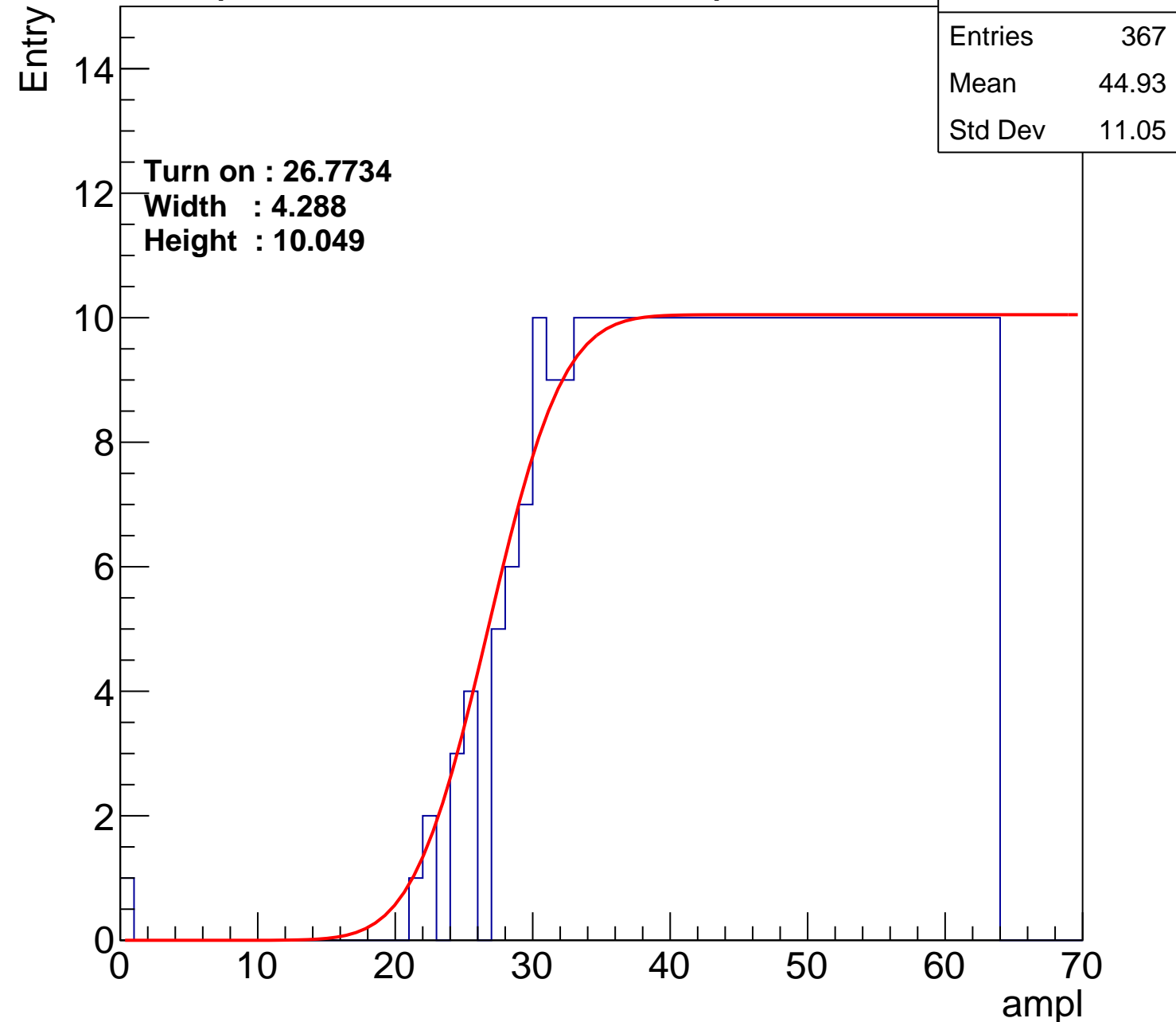
Width : 4.288

Height : 10.049

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch113

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	400
Mean	43.15
Std Dev	12.35

Turn on : 24.0751

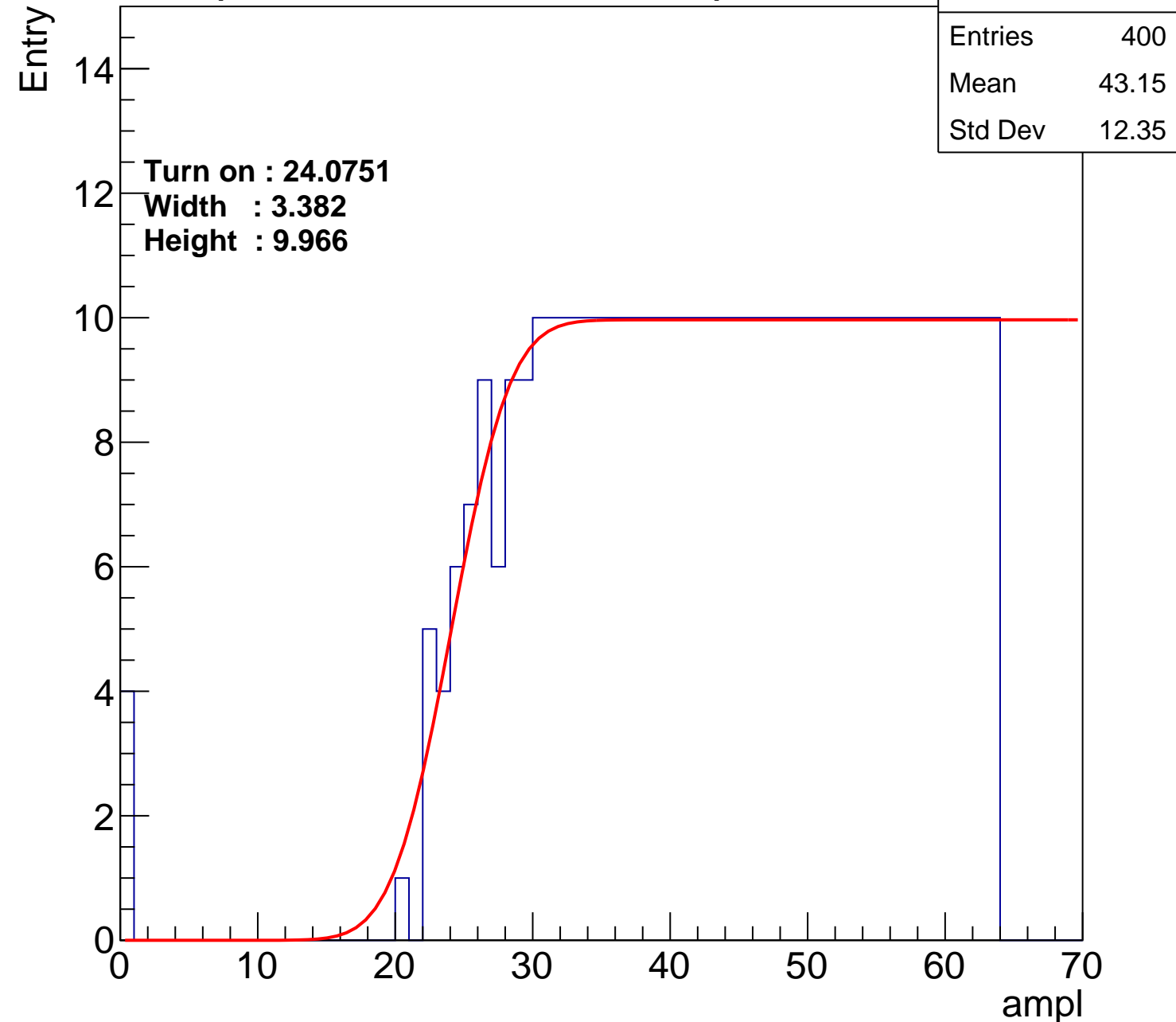
Width : 3.382

Height : 9.966

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch114

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	395
Mean	43.32
Std Dev	12.46

Turn on : 24.9071

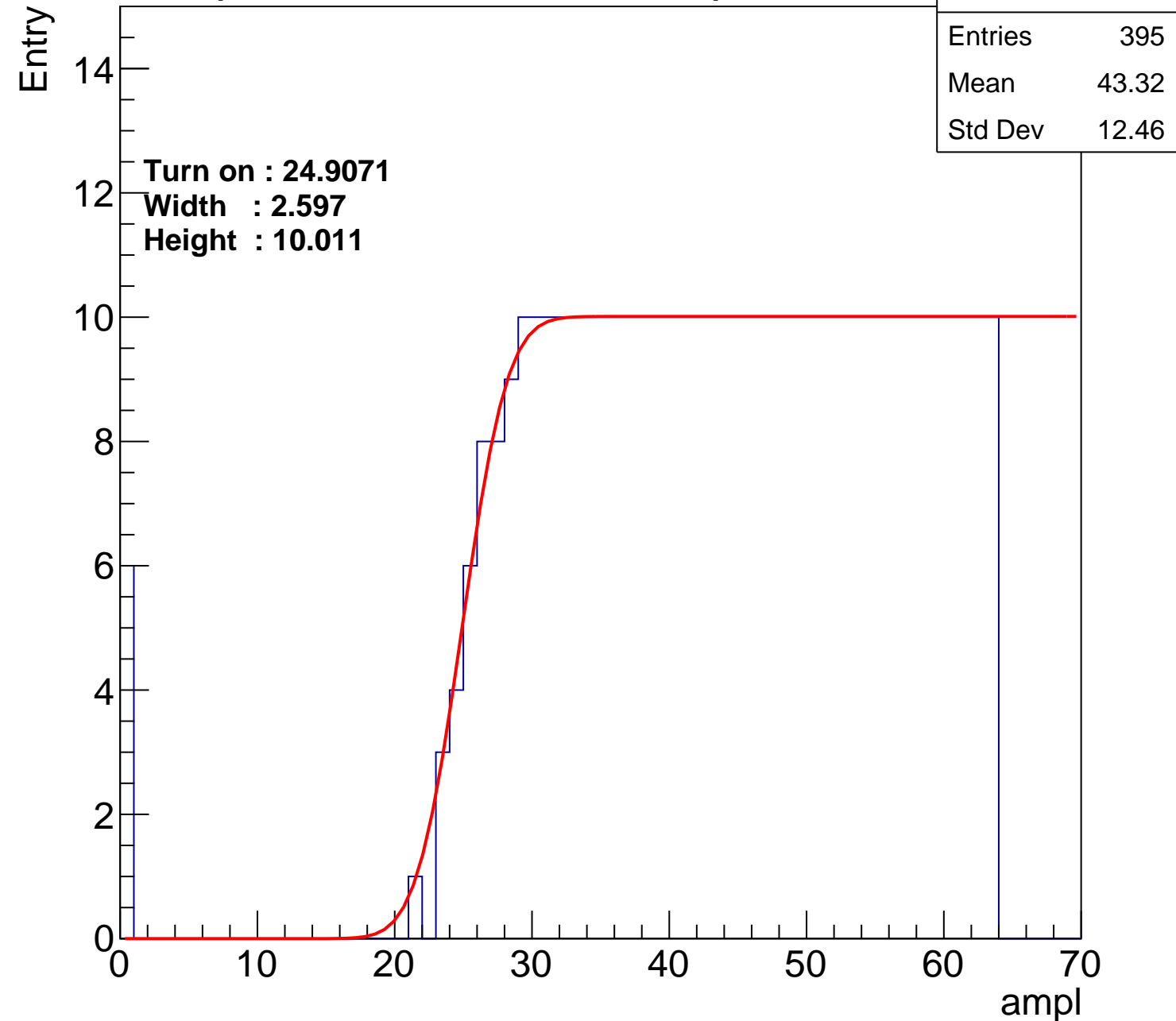
Width : 2.597

Height : 10.011

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch115

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	379
Mean	44.02
Std Dev	12.31

Turn on : 27.3343

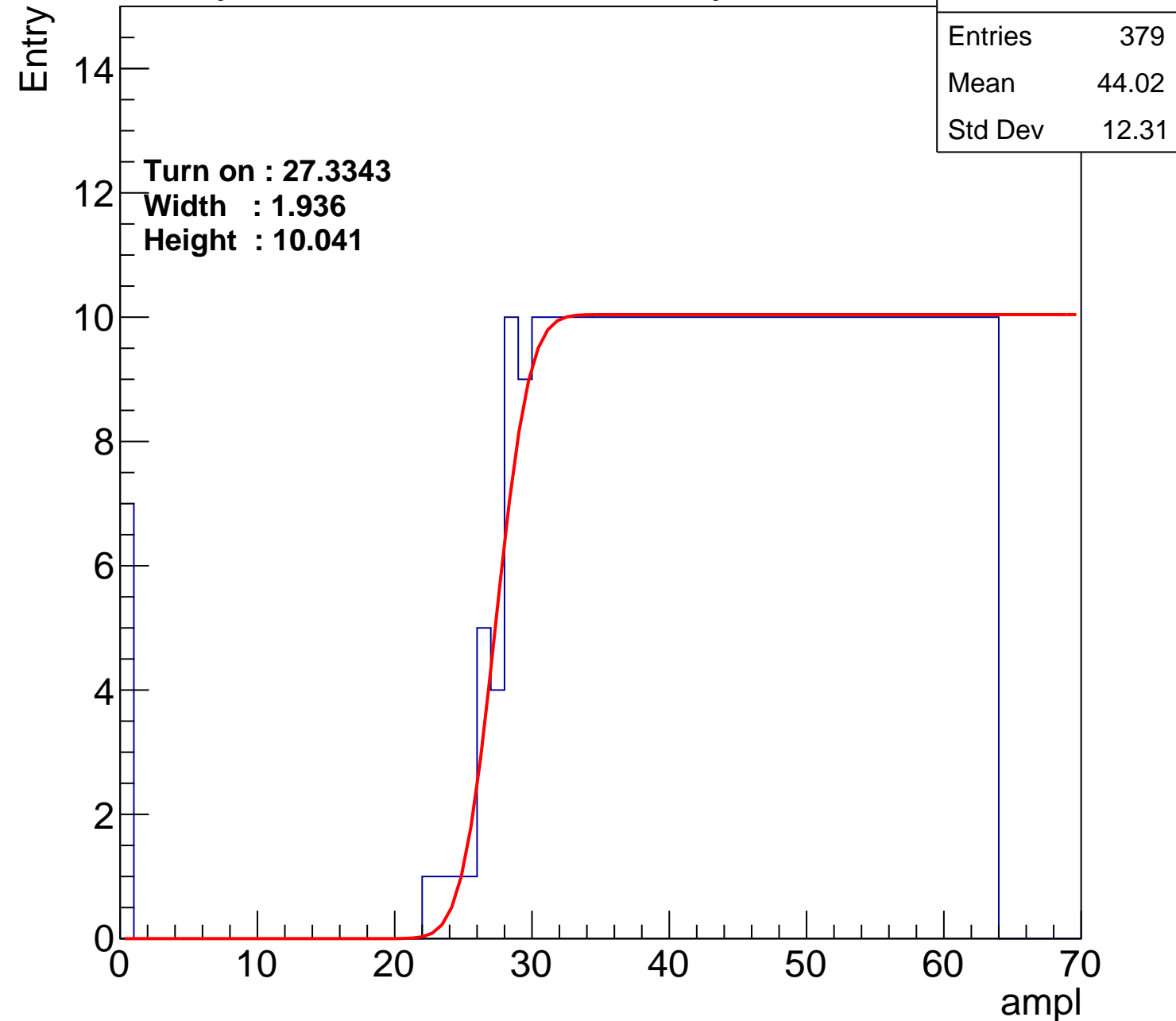
Width : 1.936

Height : 10.041

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch116

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	392
Mean	43.63
Std Dev	11.96

Turn on : 25.5488

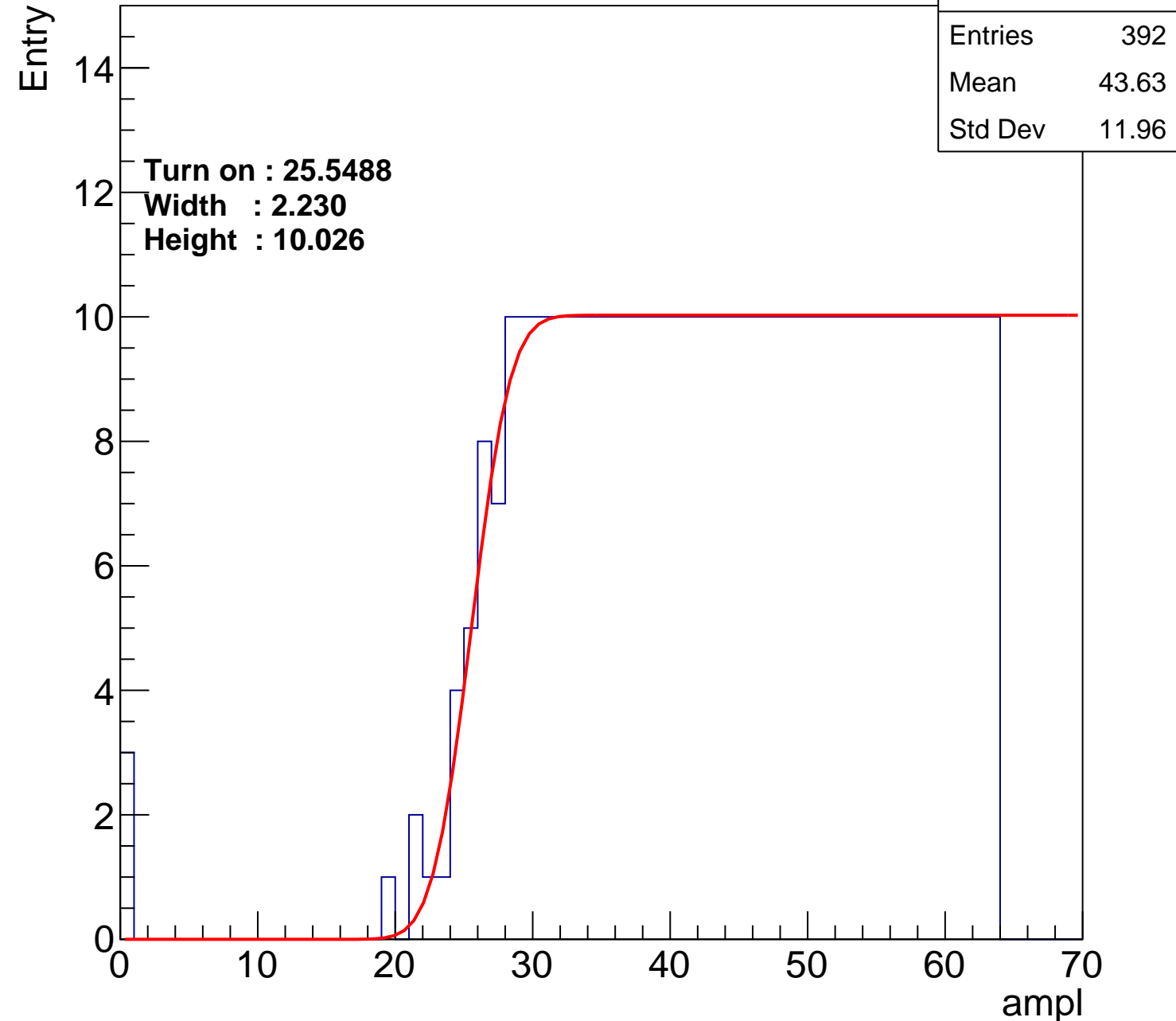
Width : 2.230

Height : 10.026

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch117

calib\_packv5\_042523\_0143.root, FC#10, port B3

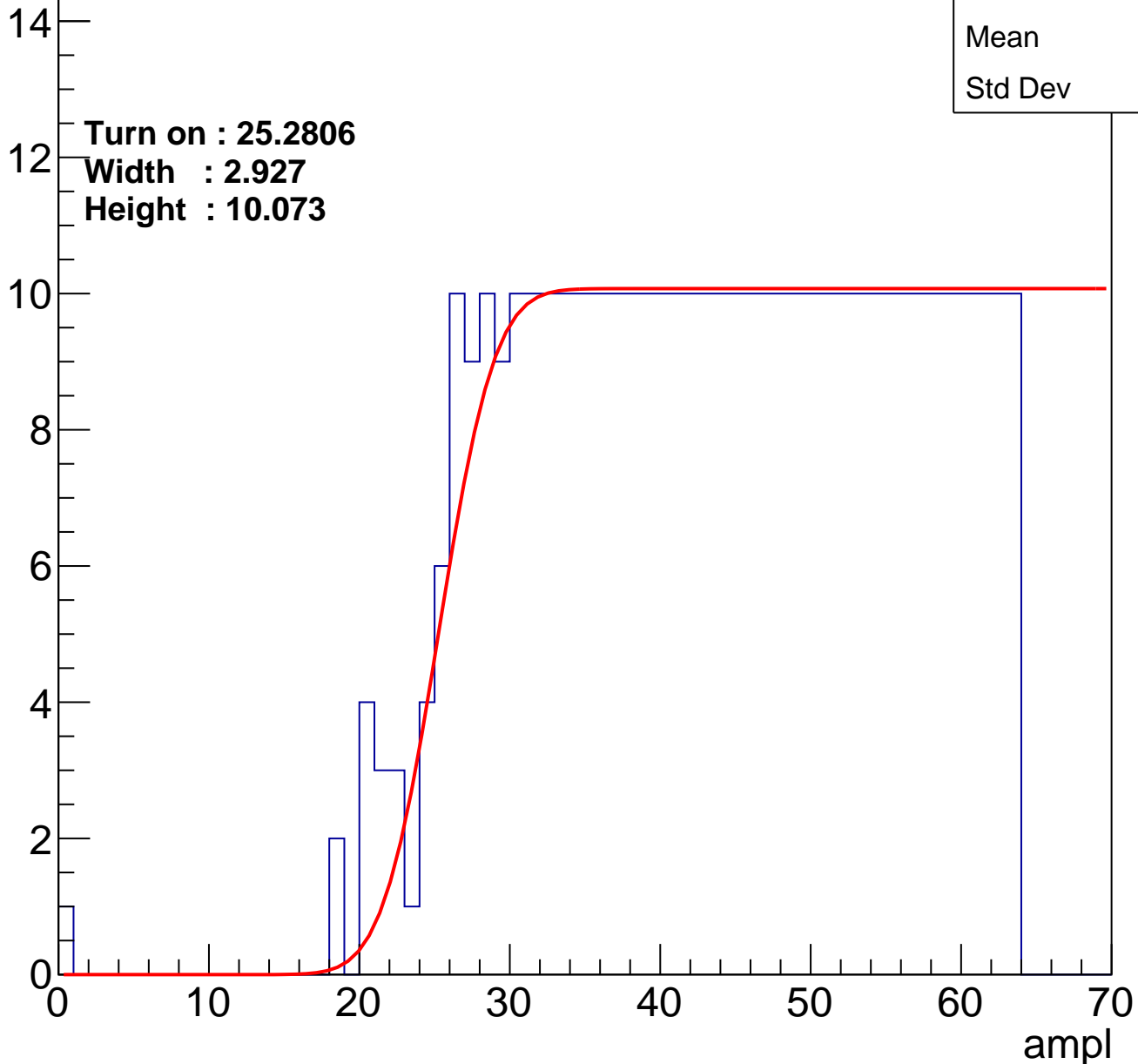
Entries	402
Mean	43.2
Std Dev	12

Turn on : 25.2806

Width : 2.927

Height : 10.073

Entry



# B1L002S, U2-ch118

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	385
Mean	44.01
Std Dev	11.73

Turn on : 25.8972

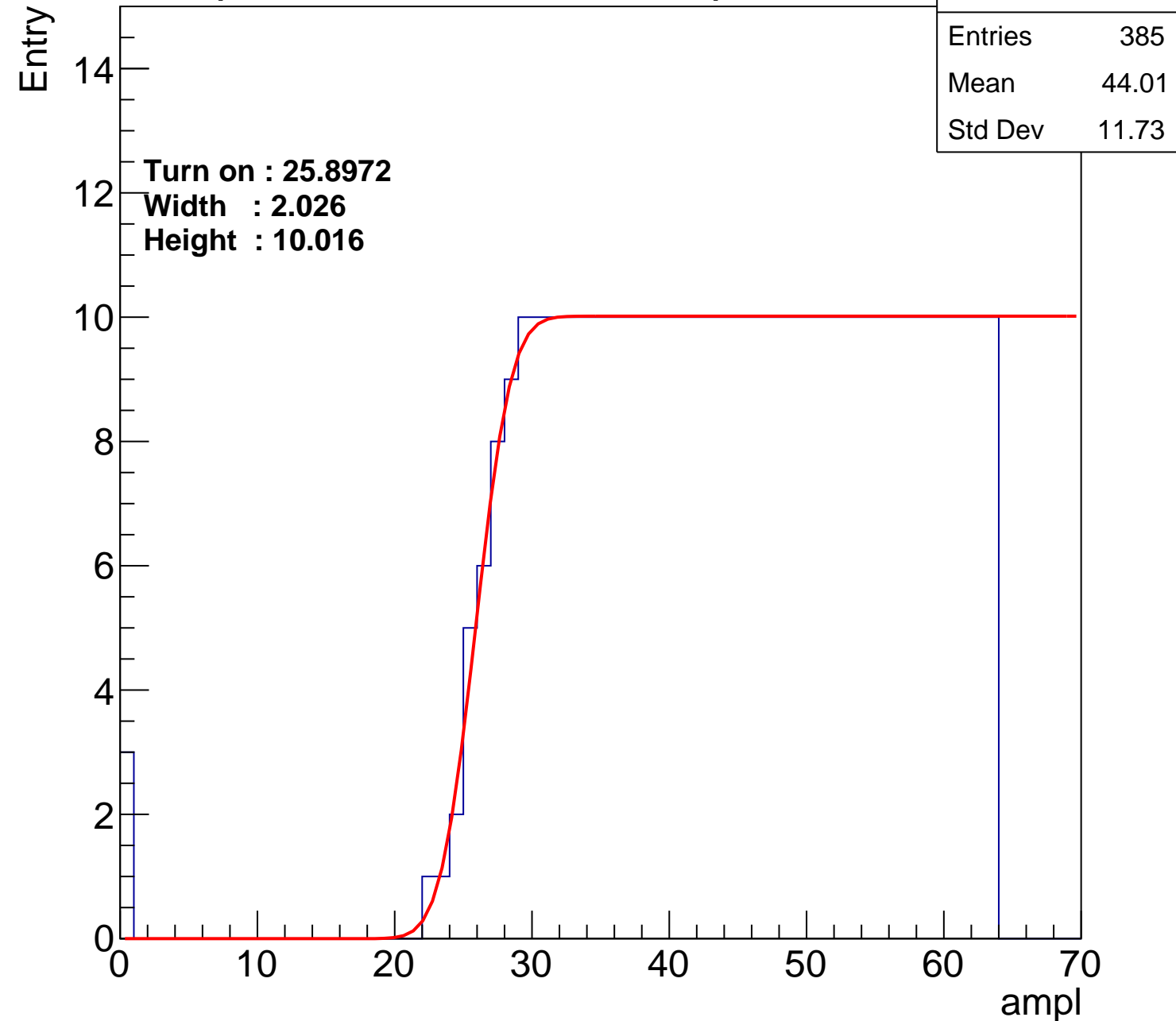
Width : 2.026

Height : 10.016

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L002S, U2-ch119

calib\_packv5\_042523\_0143.root, FC#10, port B3

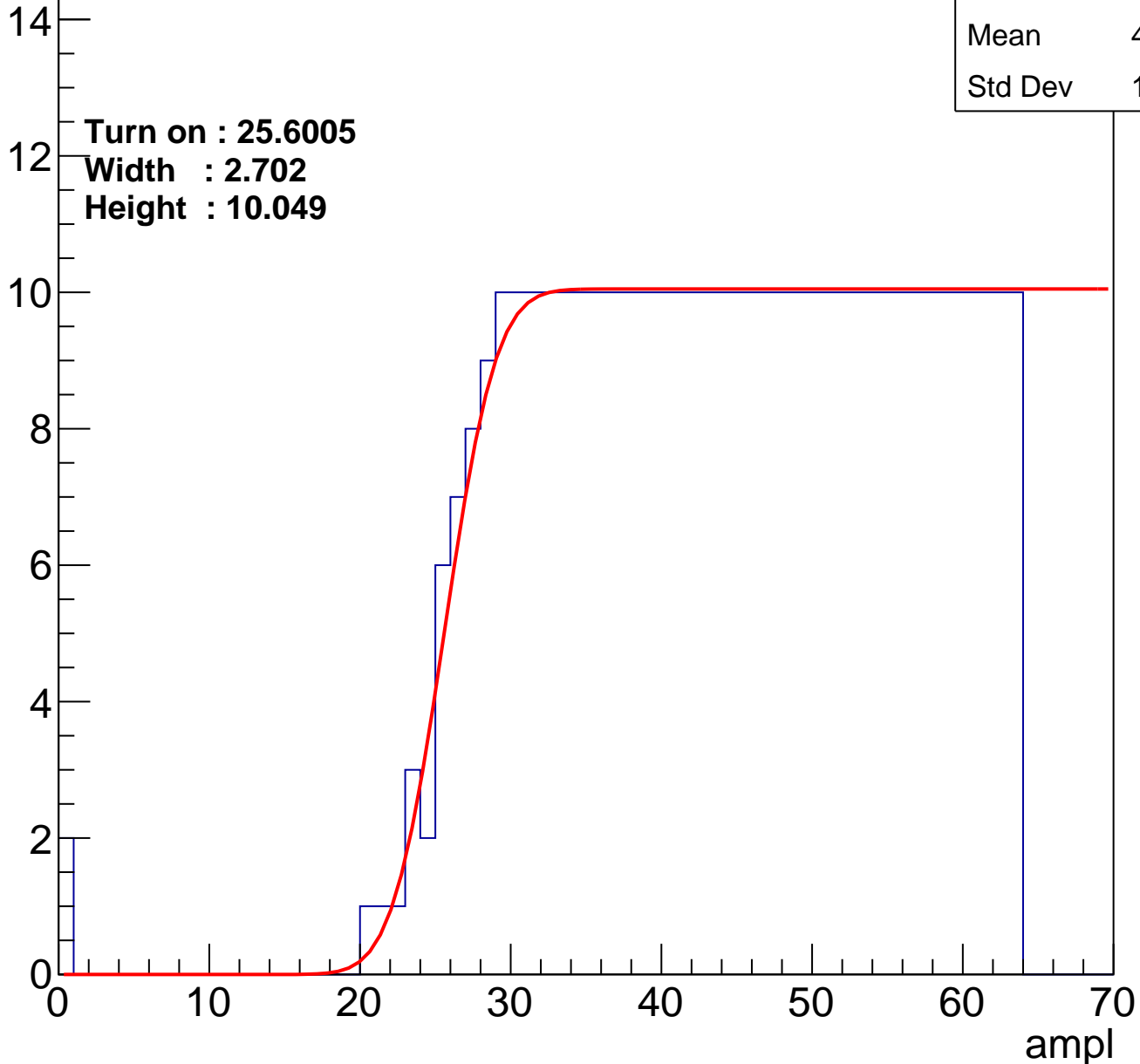
Entries	390
Mean	43.79
Std Dev	11.74

**Turn on : 25.6005**

**Width : 2.702**

**Height : 10.049**

Entry



# B1L002S, U2-ch120

calib\_packv5\_042523\_0143.root, FC#10, port B3

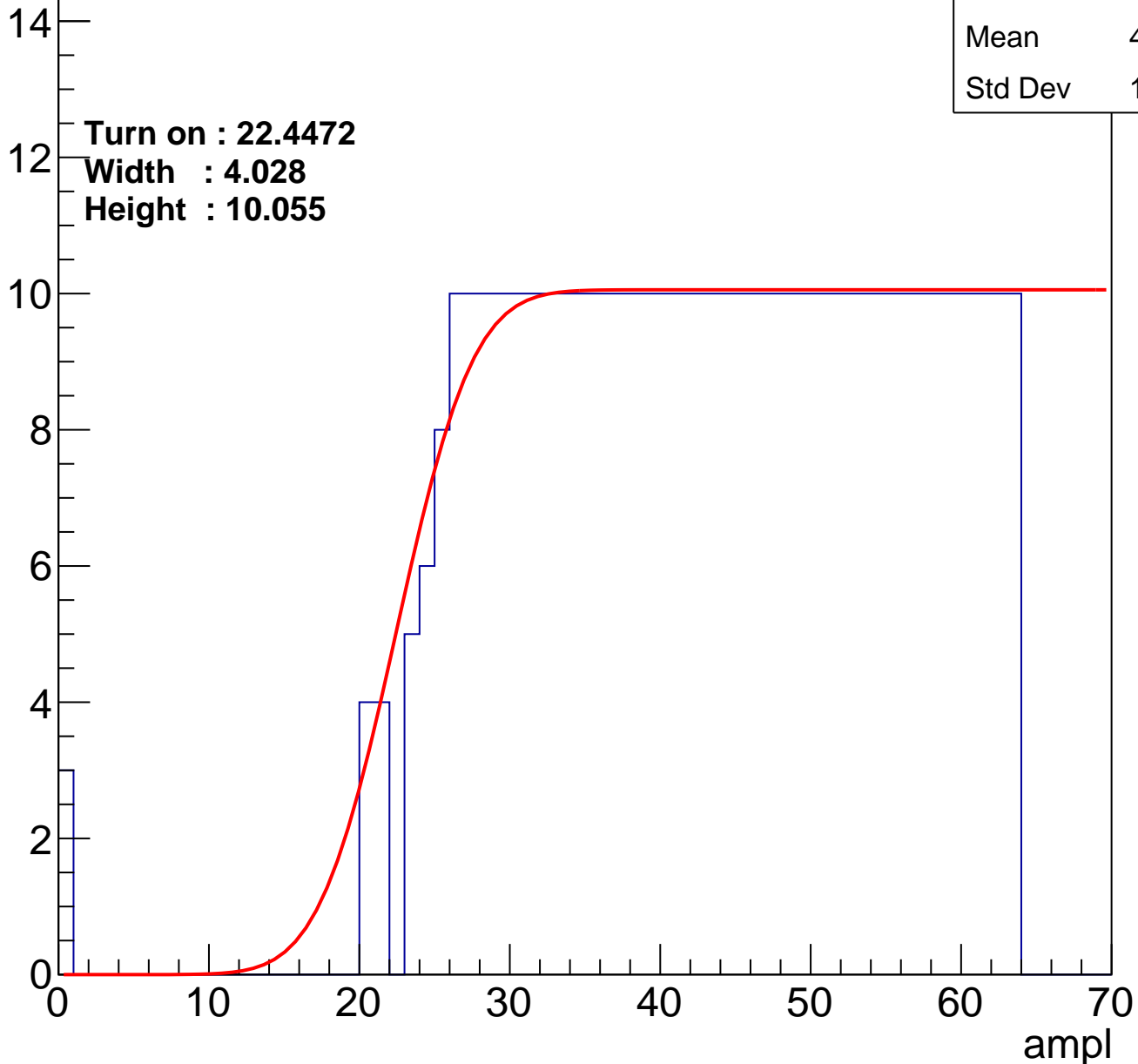
Entries	410
Mean	42.76
Std Dev	12.38

Turn on : 22.4472

Width : 4.028

Height : 10.055

Entry



# B1L002S, U2-ch121

calib\_packv5\_042523\_0143.root, FC#10, port B3

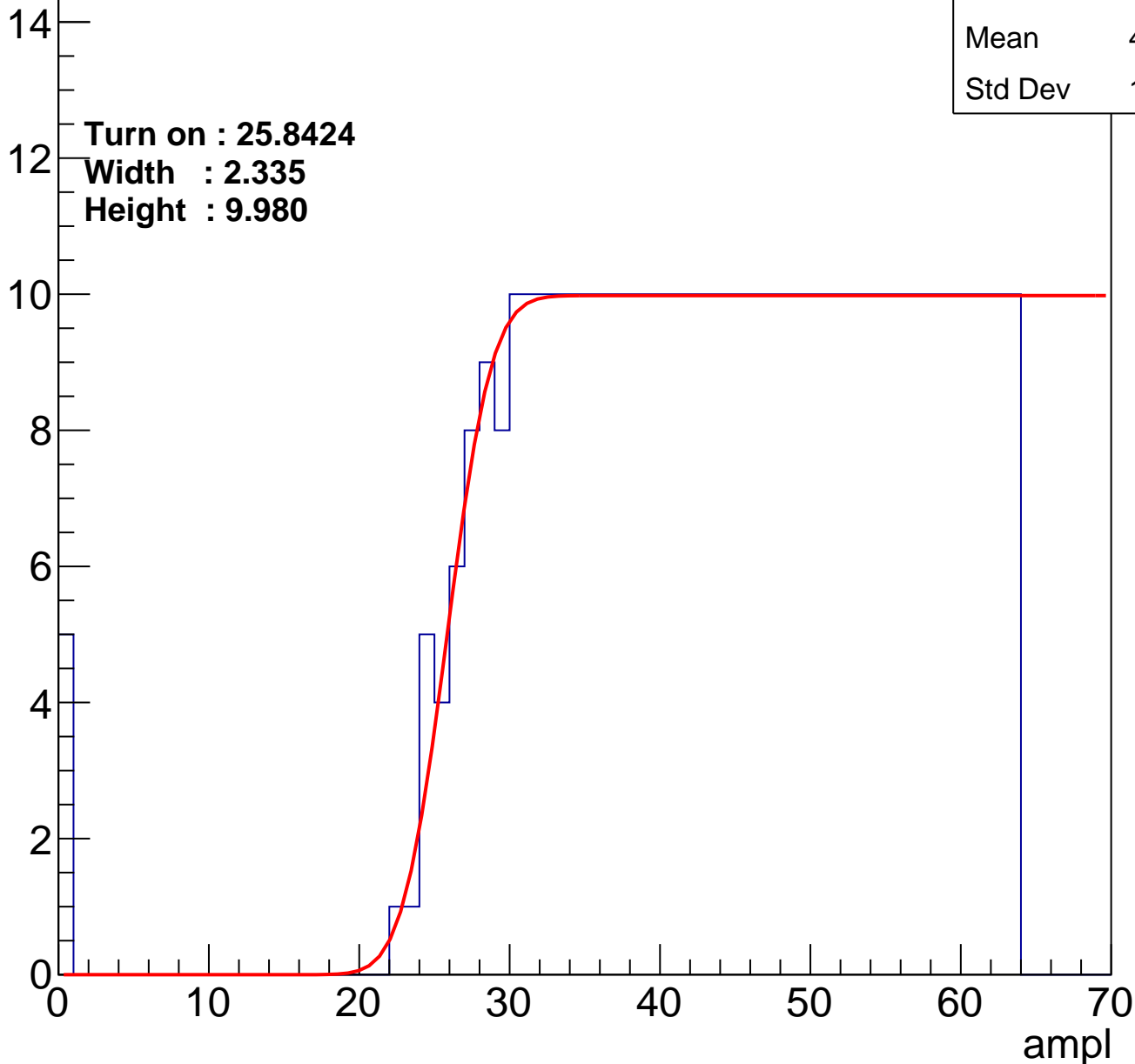
Entry

Entries	387
Mean	43.75
Std Dev	12.16

Turn on : 25.8424

Width : 2.335

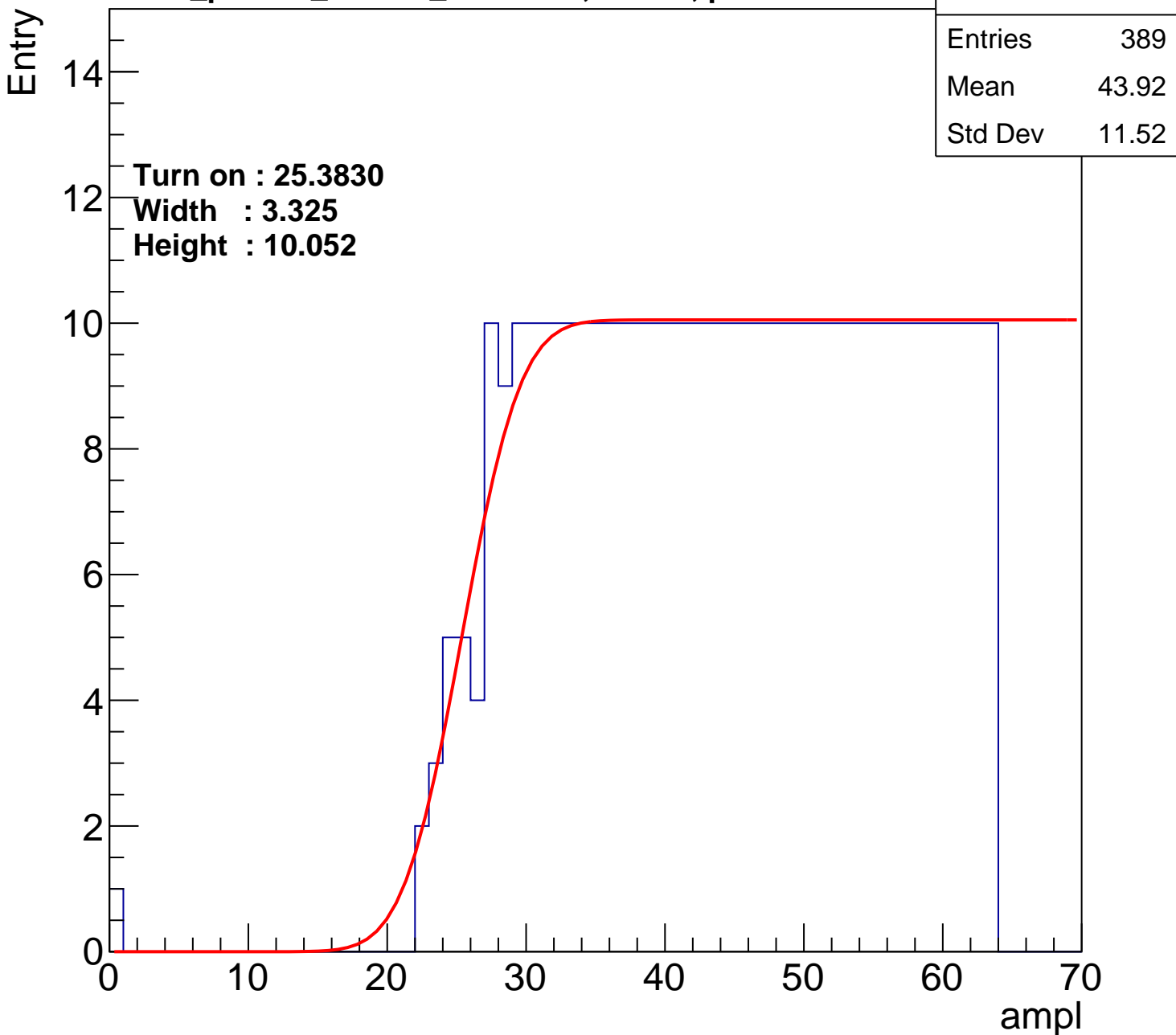
Height : 9.980



**calib\_packv5\_042523\_0143.root, FC#10, port B3**

**calib\_packv5\_042523\_0143.root, FC#10, port B3**

Turn on : 25.3830  
Width : 3.325  
Height : 10.052



# B1L002S, U2-ch123

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	386
Mean	44.04
Std Dev	11.47

Turn on : 25.2789

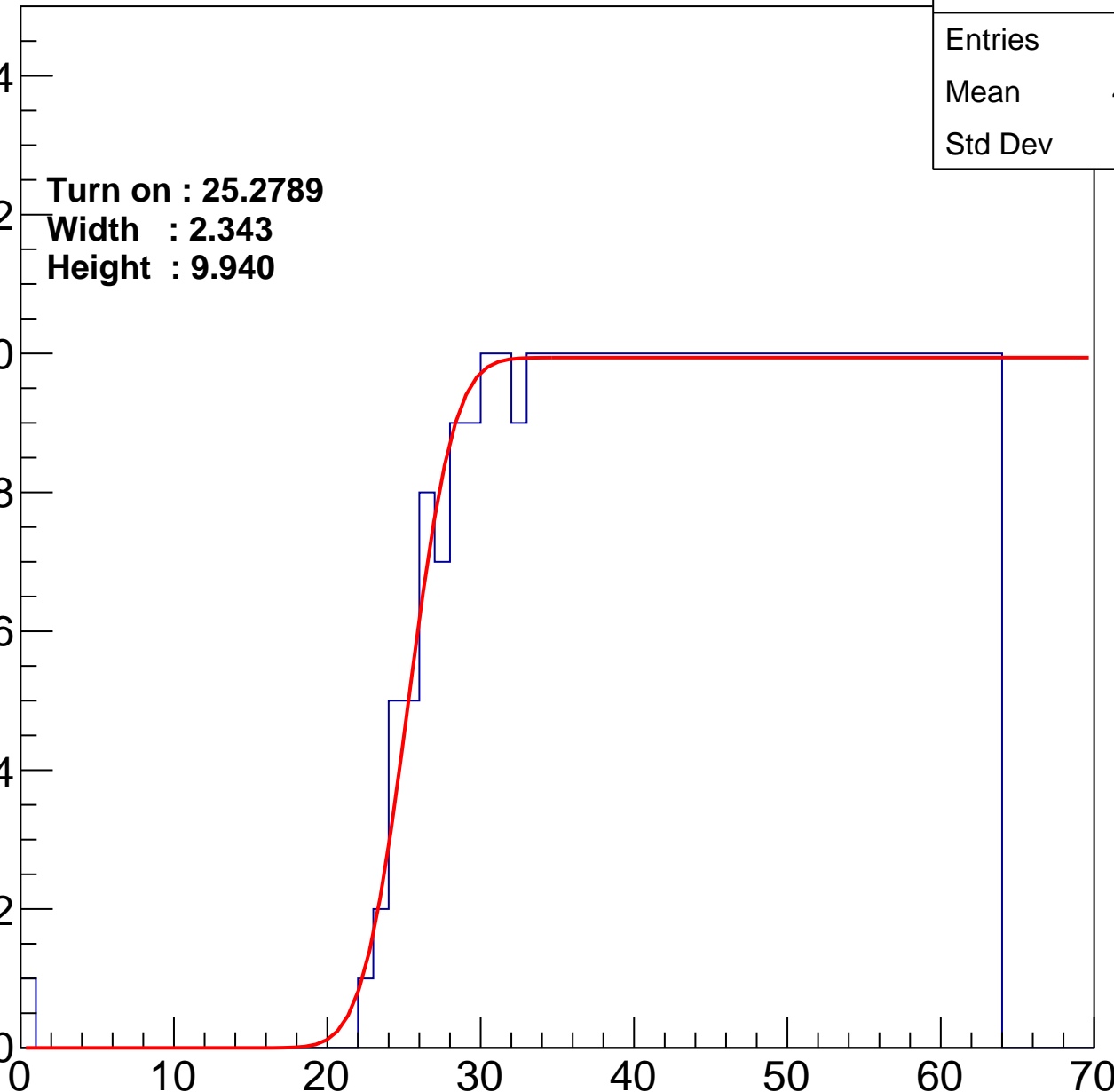
Width : 2.343

Height : 9.940

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch124

calib\_packv5\_042523\_0143.root, FC#10, port B3

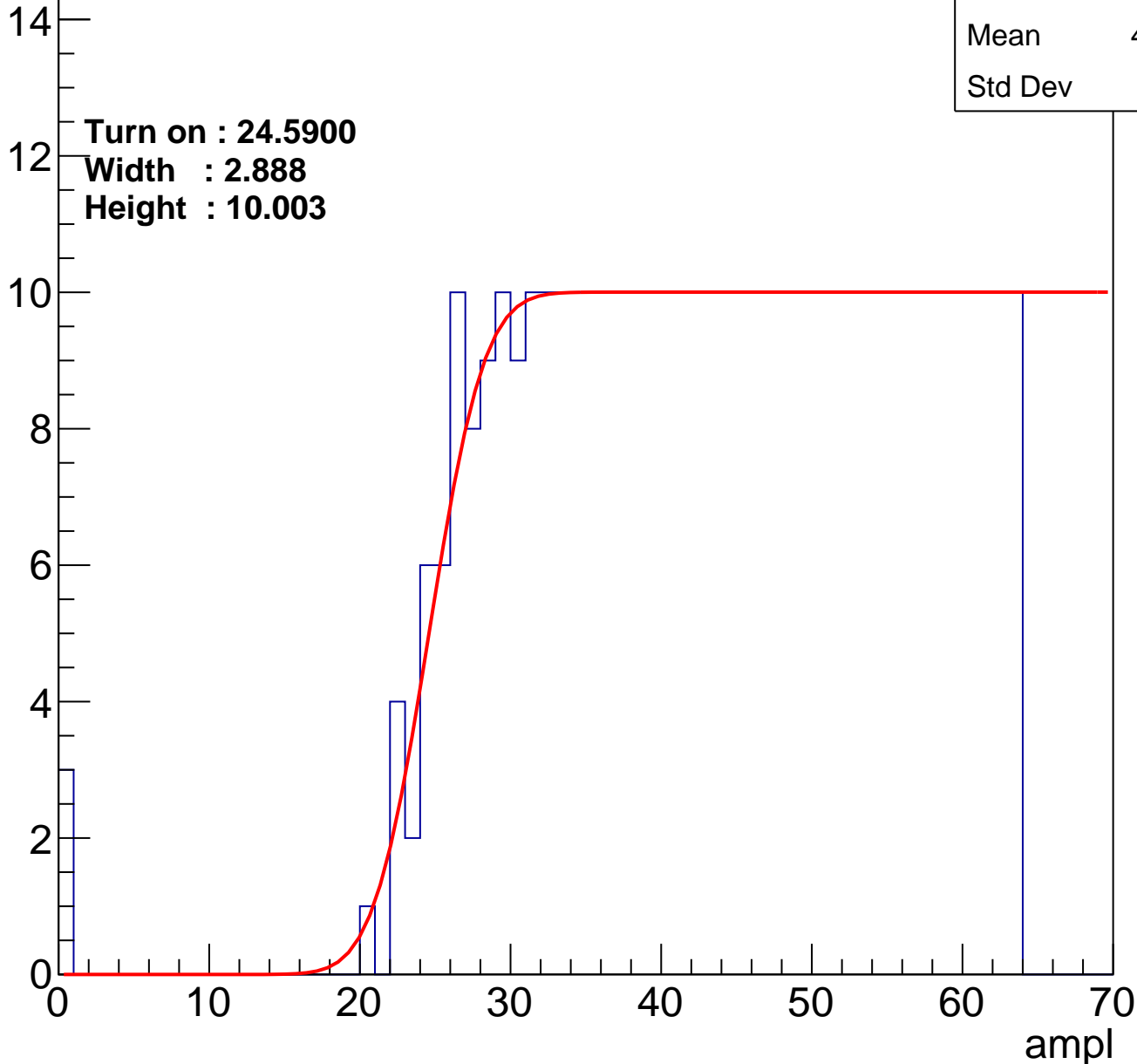
Entries	398
Mean	43.33
Std Dev	12.11

Turn on : 24.5900

Width : 2.888

Height : 10.003

Entry



# B1L002S, U2-ch125

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	389
Mean	43.8
Std Dev	11.85

Turn on : 25.3005

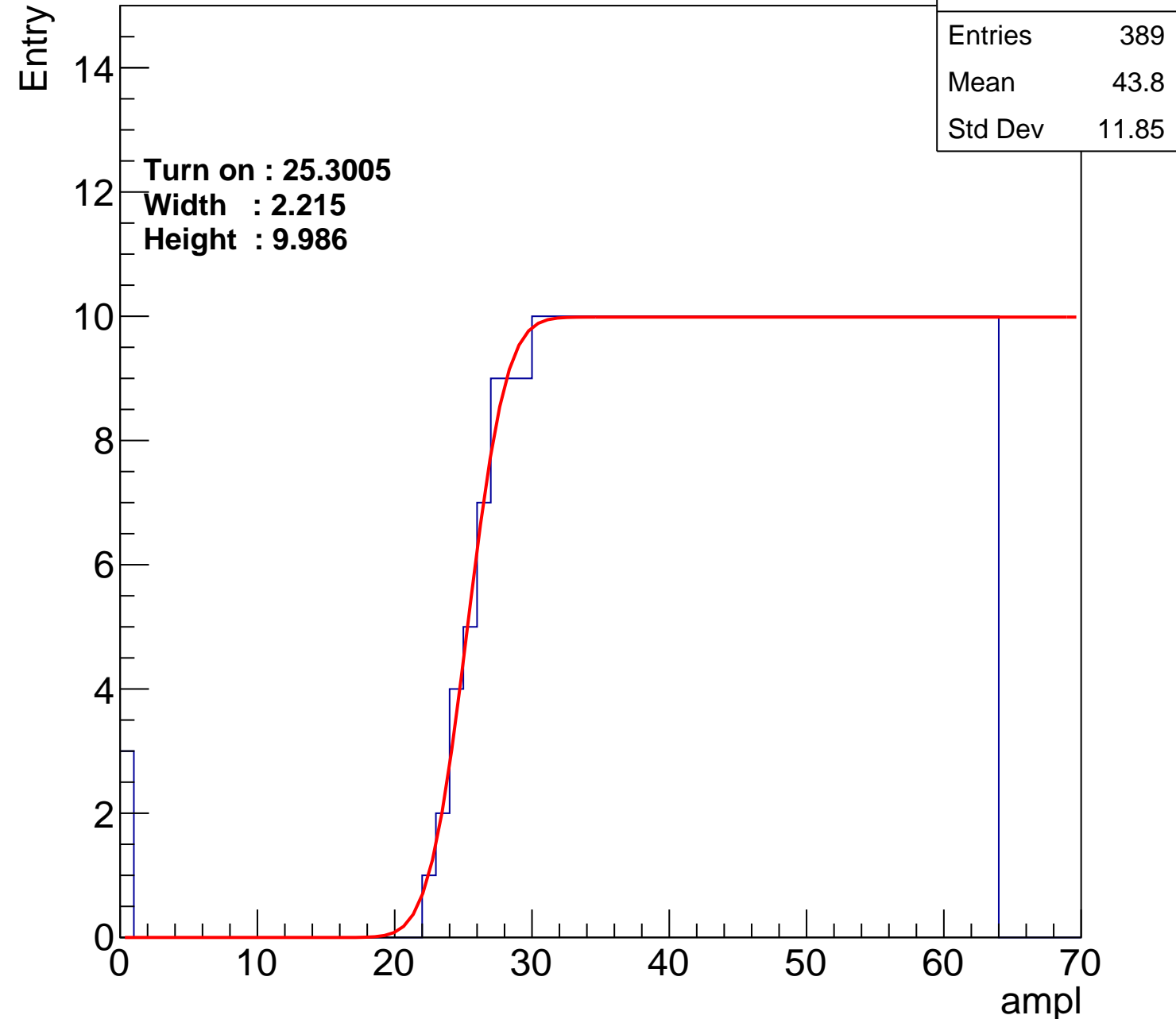
Width : 2.215

Height : 9.986

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L002S, U2-ch126

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	406
Mean	42.96
Std Dev	12.28

Turn on : 23.6179

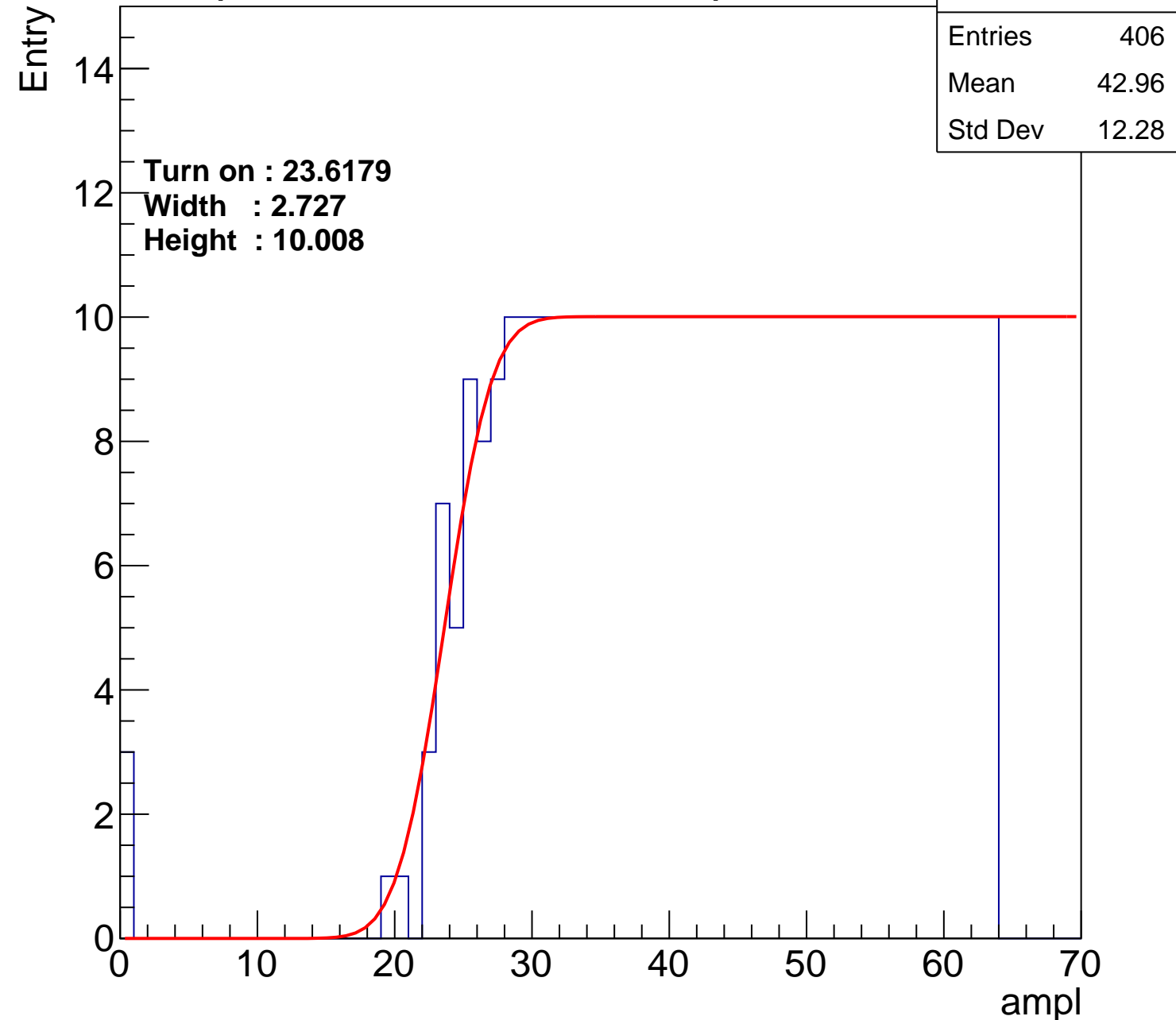
Width : 2.727

Height : 10.008

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L002S, U2-ch127

calib\_packv5\_042523\_0143.root, FC#10, port B3

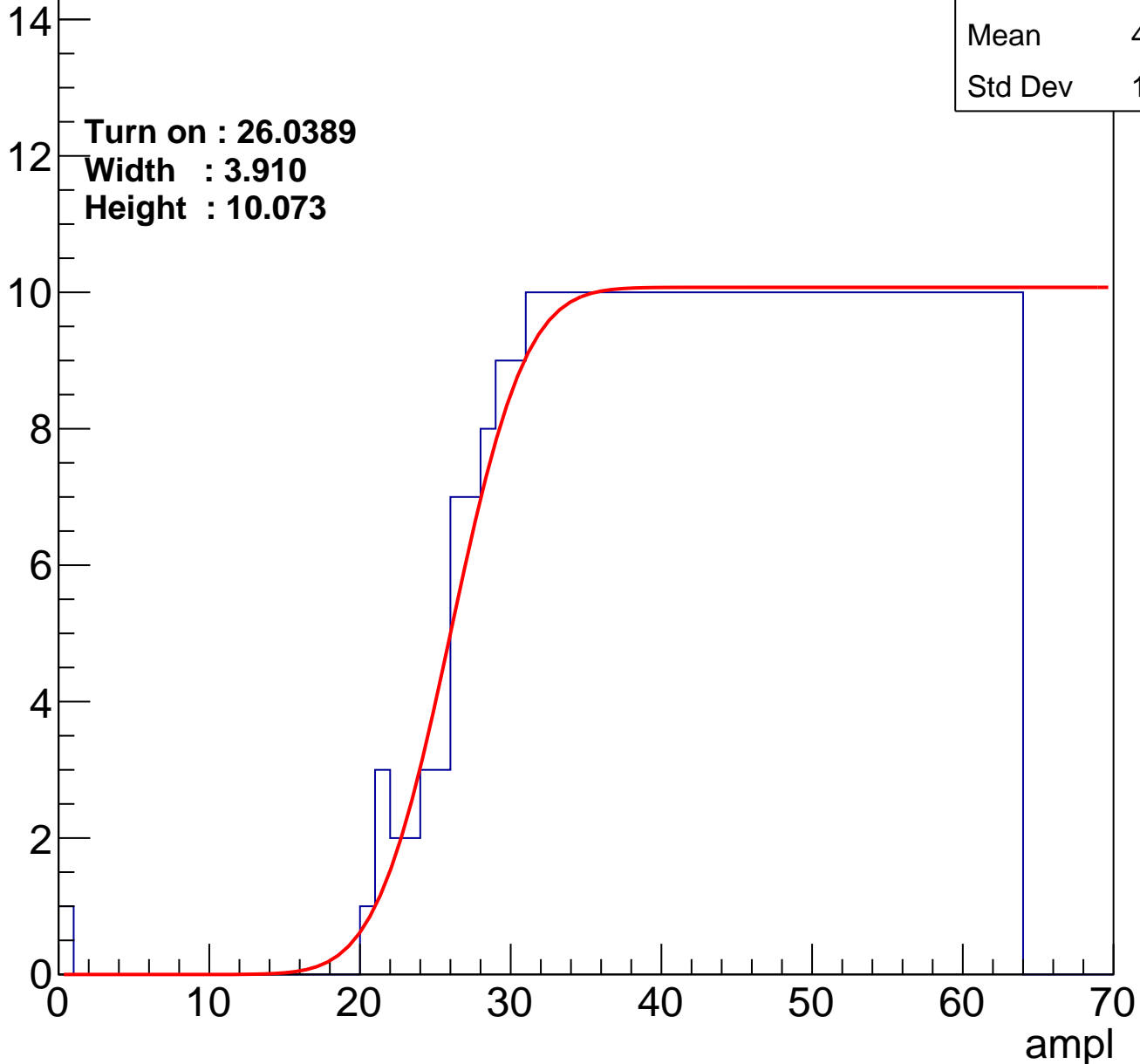
Entries	385
Mean	44.04
Std Dev	11.54

Turn on : 26.0389

Width : 3.910

Height : 10.073

Entry



# B1L002S, U2-ch127

calib\_packv5\_042523\_0143.root, FC#10, port B3

Entries	385
Mean	44.04
Std Dev	11.54

Turn on : 26.0389

Width : 3.910

Height : 10.073

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl

