

B1L103S, U23-ch0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	442
Mean	38.49
Std Dev	18.05

Turn on : 25.7367

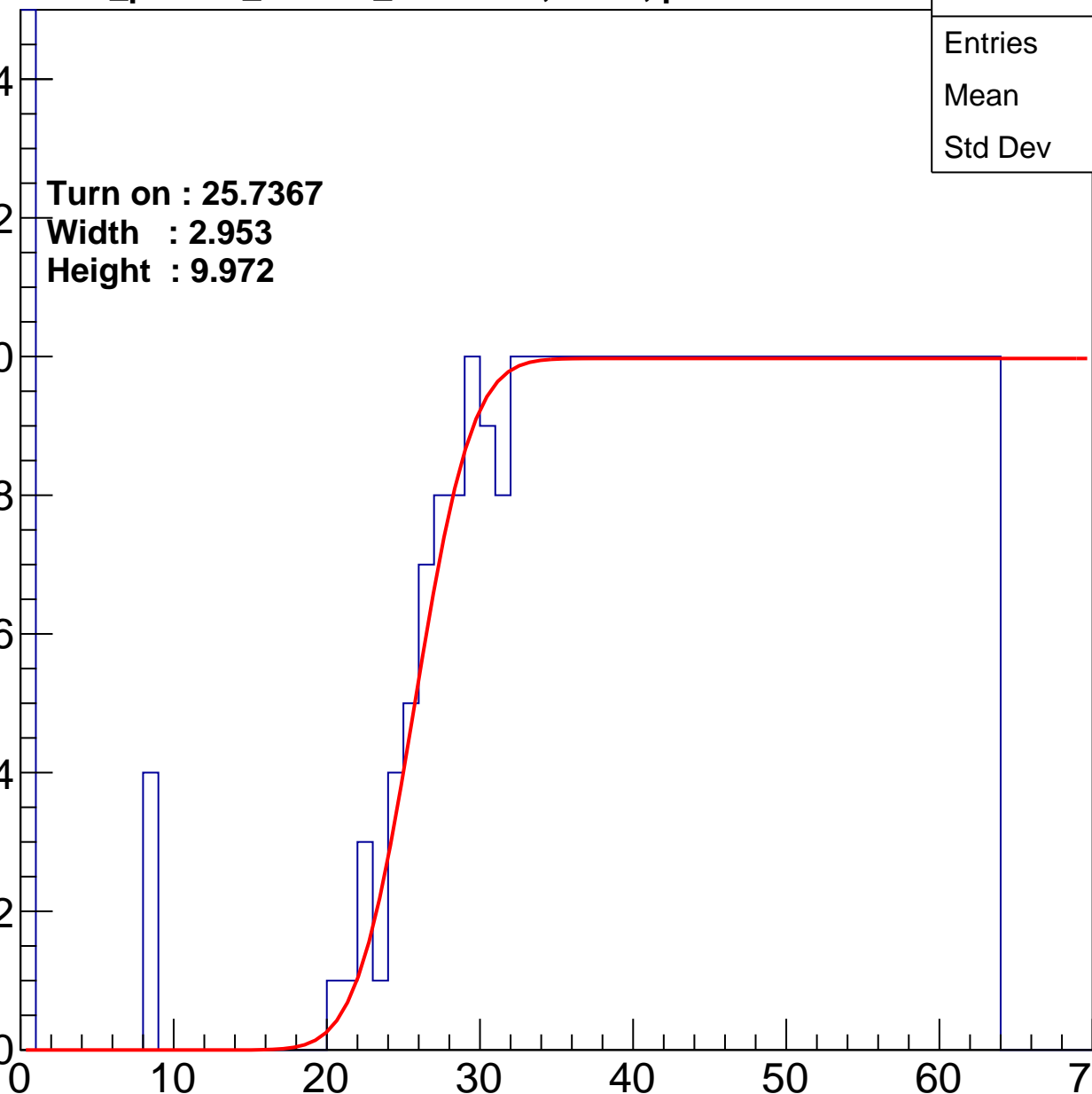
Width : 2.953

Height : 9.972

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	422
Mean	40.44
Std Dev	16.21

Turn on : 24.9606

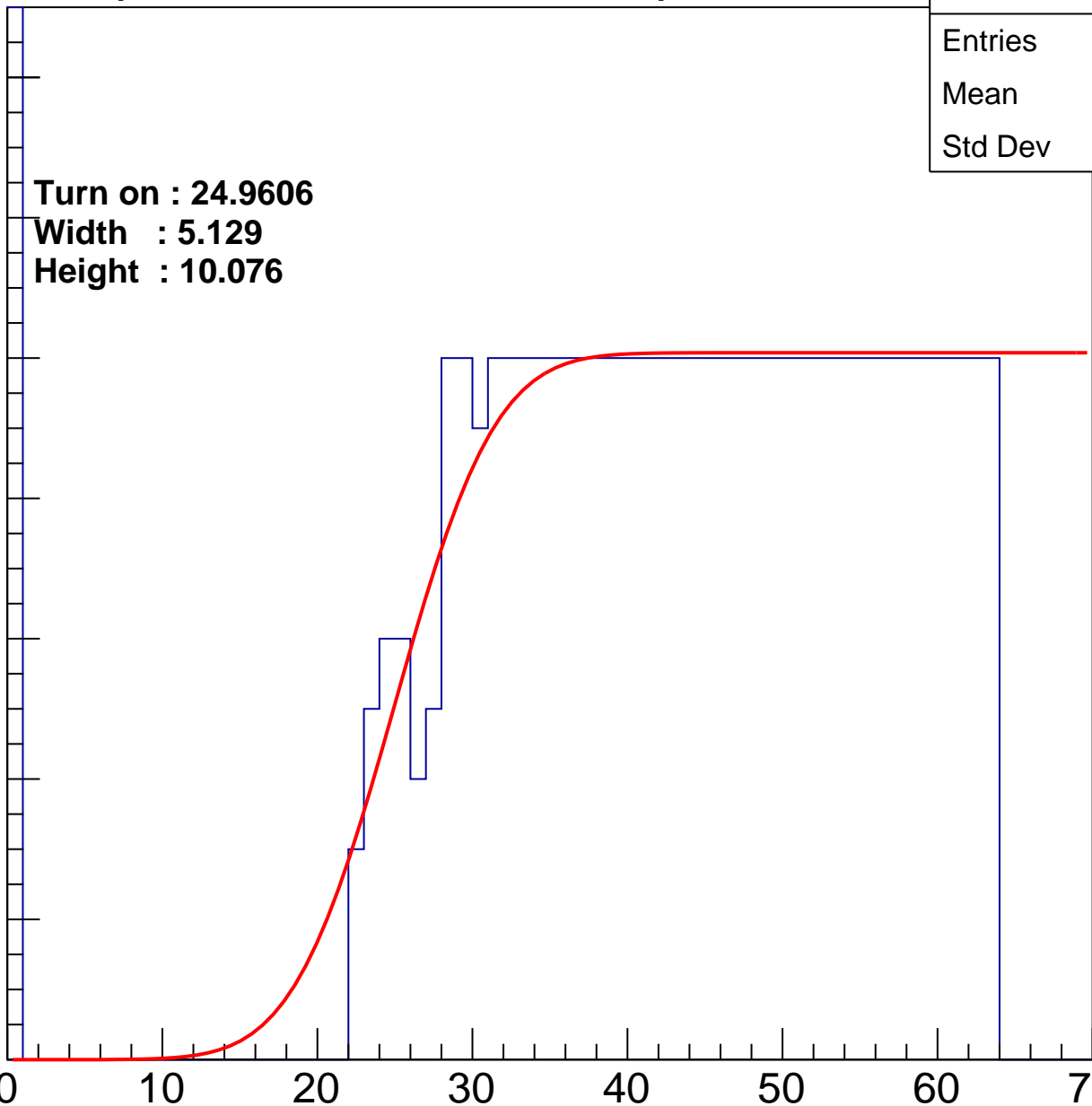
Width : 5.129

Height : 10.076

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	446
Mean	38.72
Std Dev	17.53

Turn on : 24.7603

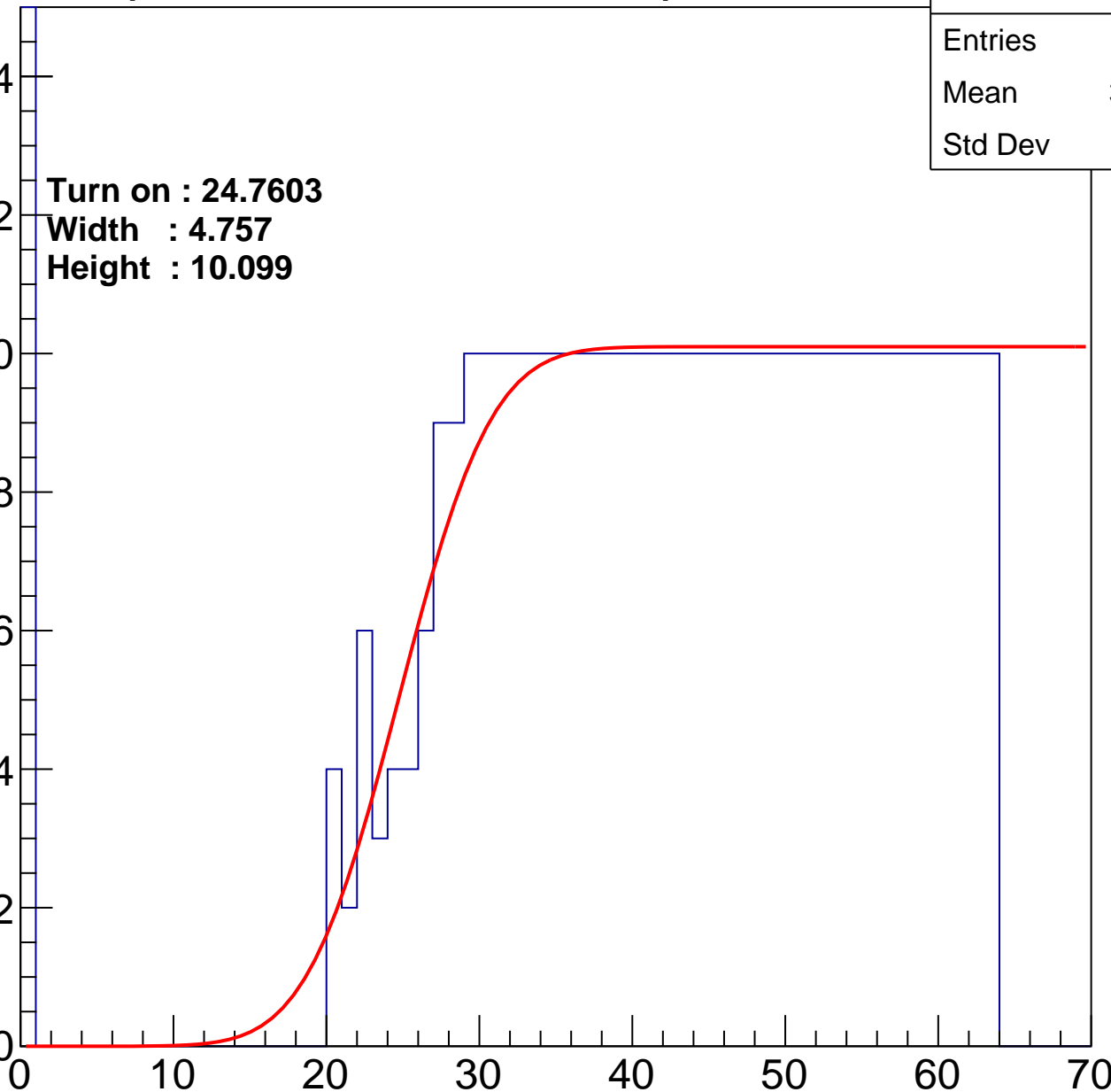
Width : 4.757

Height : 10.099

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	422
Mean	39.3
Std Dev	18.01

Turn on : 27.0509

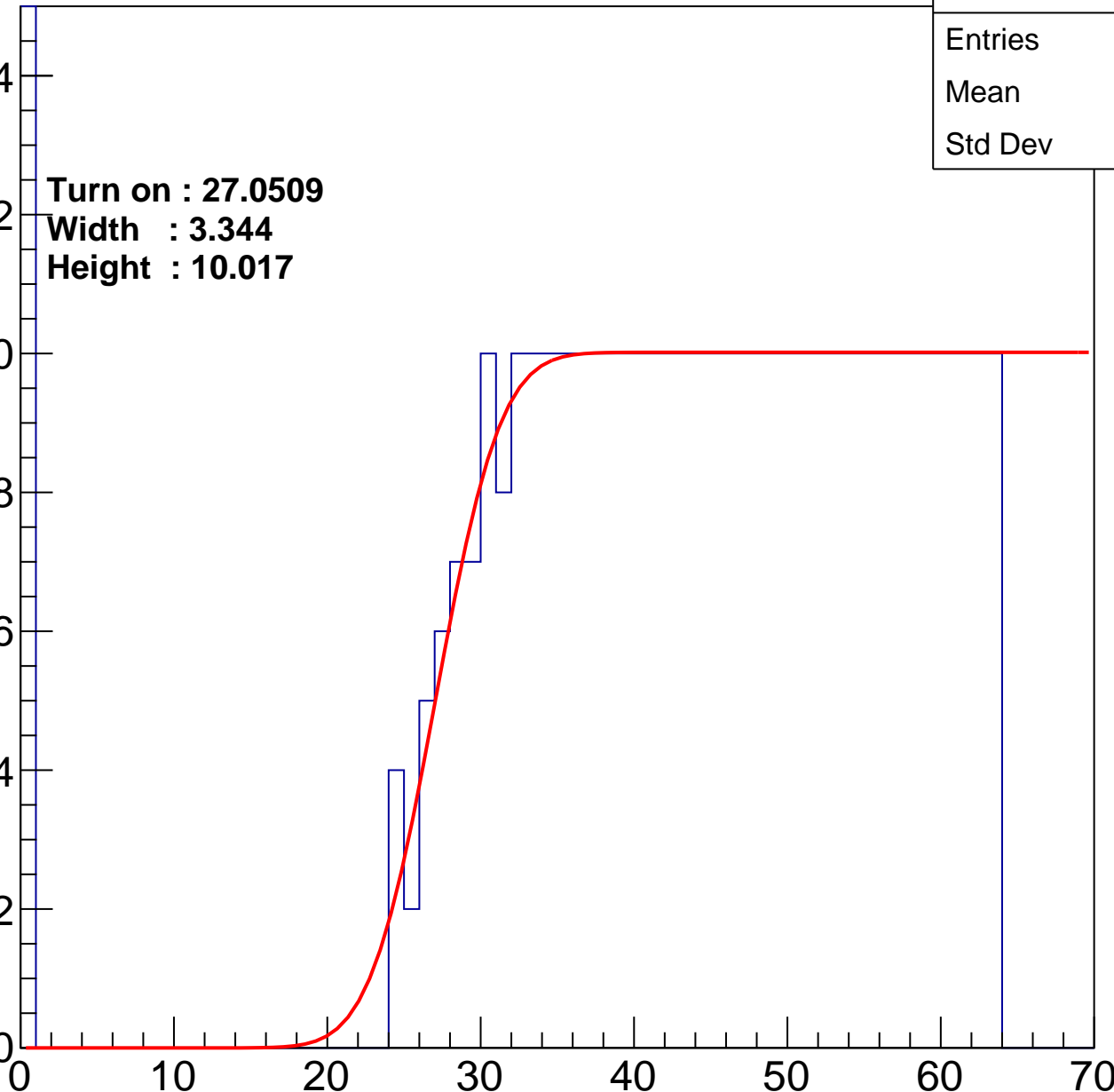
Width : 3.344

Height : 10.017

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch4

calib_packv5_041523_1651.root, FC#0, port C2

Entries	463
Mean	38.04
Std Dev	17.65

Turn on : 23.2407

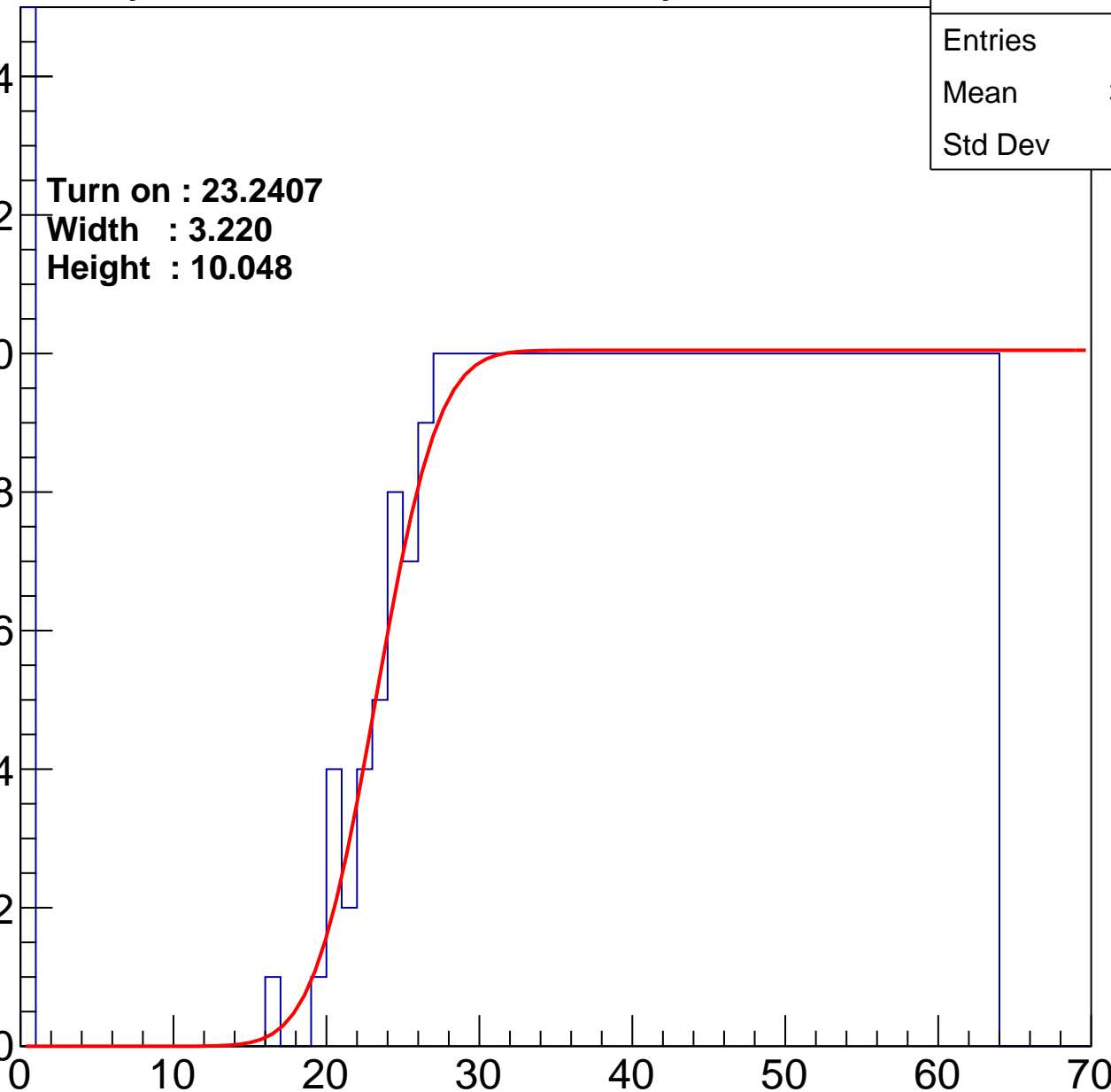
Width : 3.220

Height : 10.048

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch5

calib_packv5_041523_1651.root, FC#0, port C2

Entries	413
Mean	40.89
Std Dev	16.06

Turn on : 26.1733

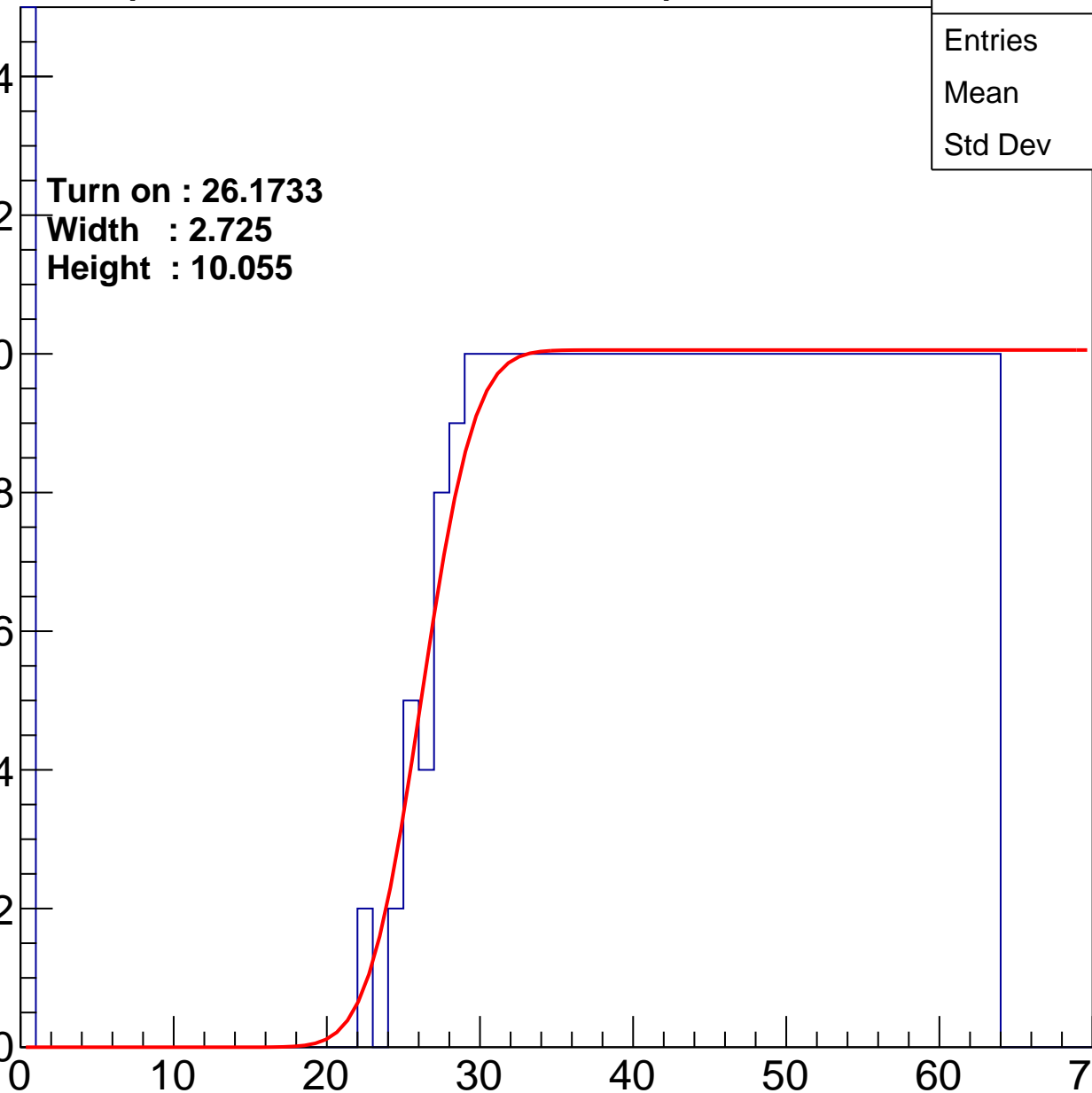
Width : 2.725

Height : 10.055

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch6

calib_packv5_041523_1651.root, FC#0, port C2

Entries	430
Mean	39.06
Std Dev	17.93

Turn on : 26.4437

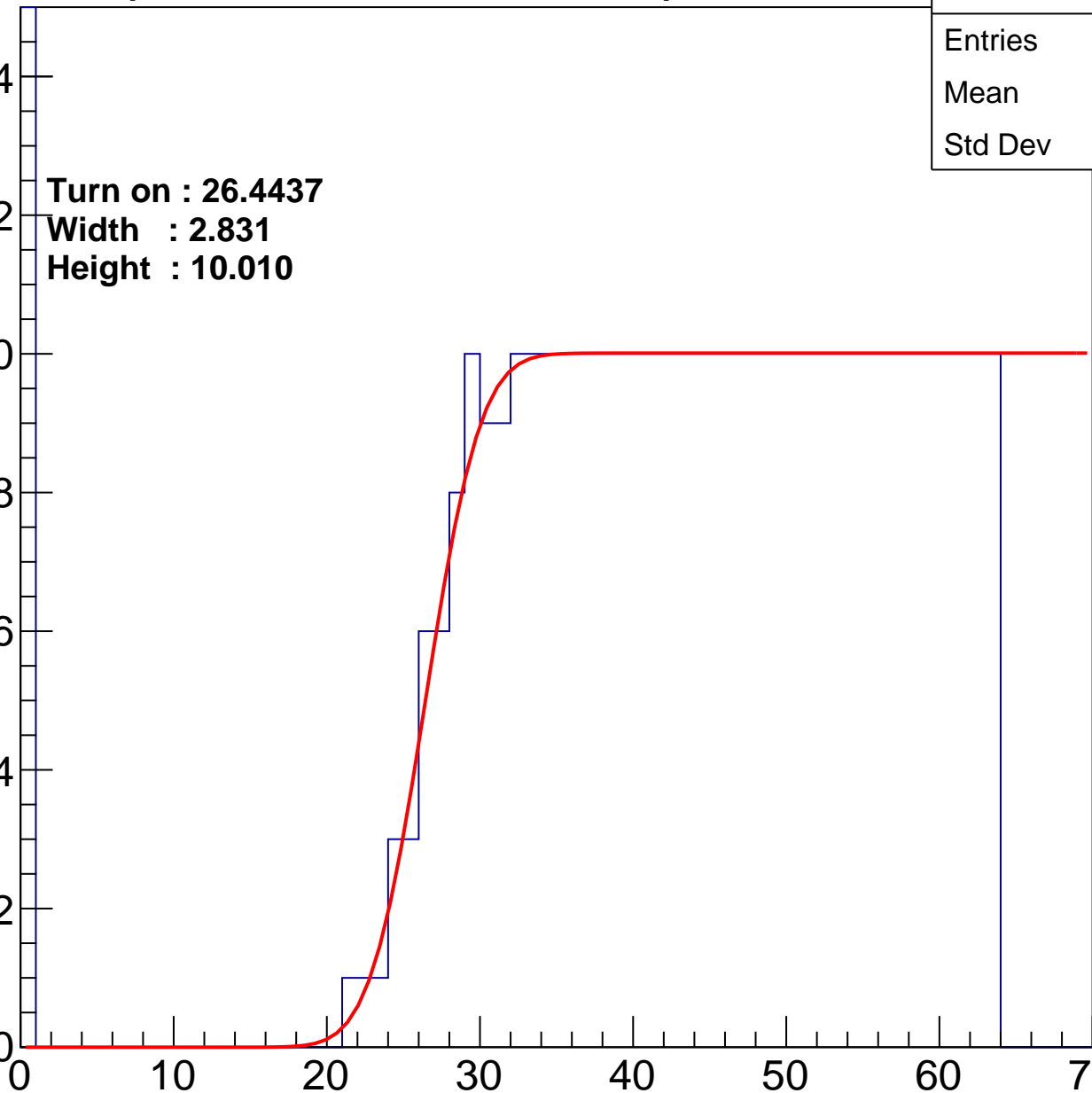
Width : 2.831

Height : 10.010

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	408
Mean	39.7
Std Dev	18.18

Turn on : 29.3882

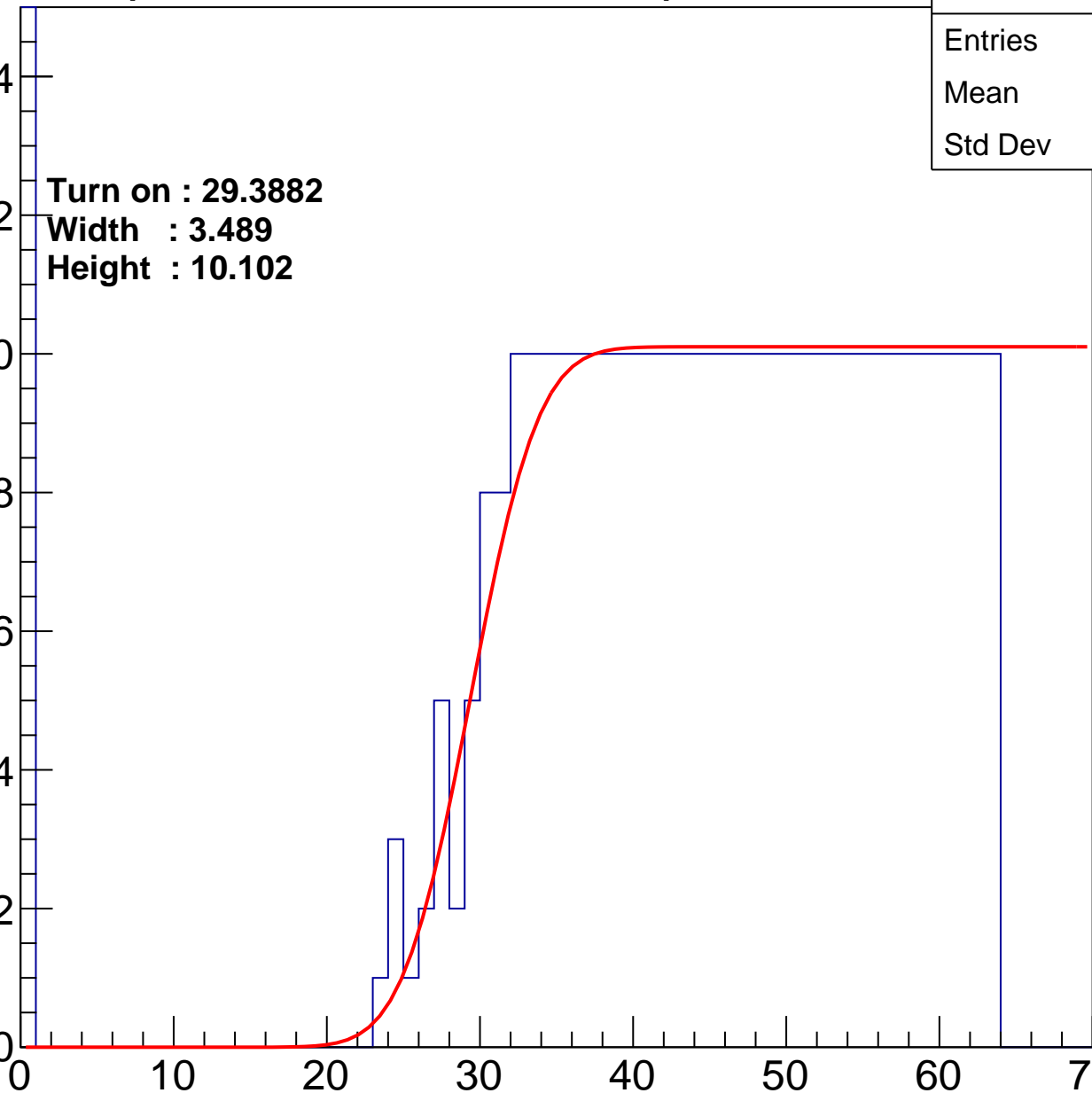
Width : 3.489

Height : 10.102

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch8

calib_packv5_041523_1651.root, FC#0, port C2

Entries	427
Mean	39.41
Std Dev	17.59

Turn on : 25.9863

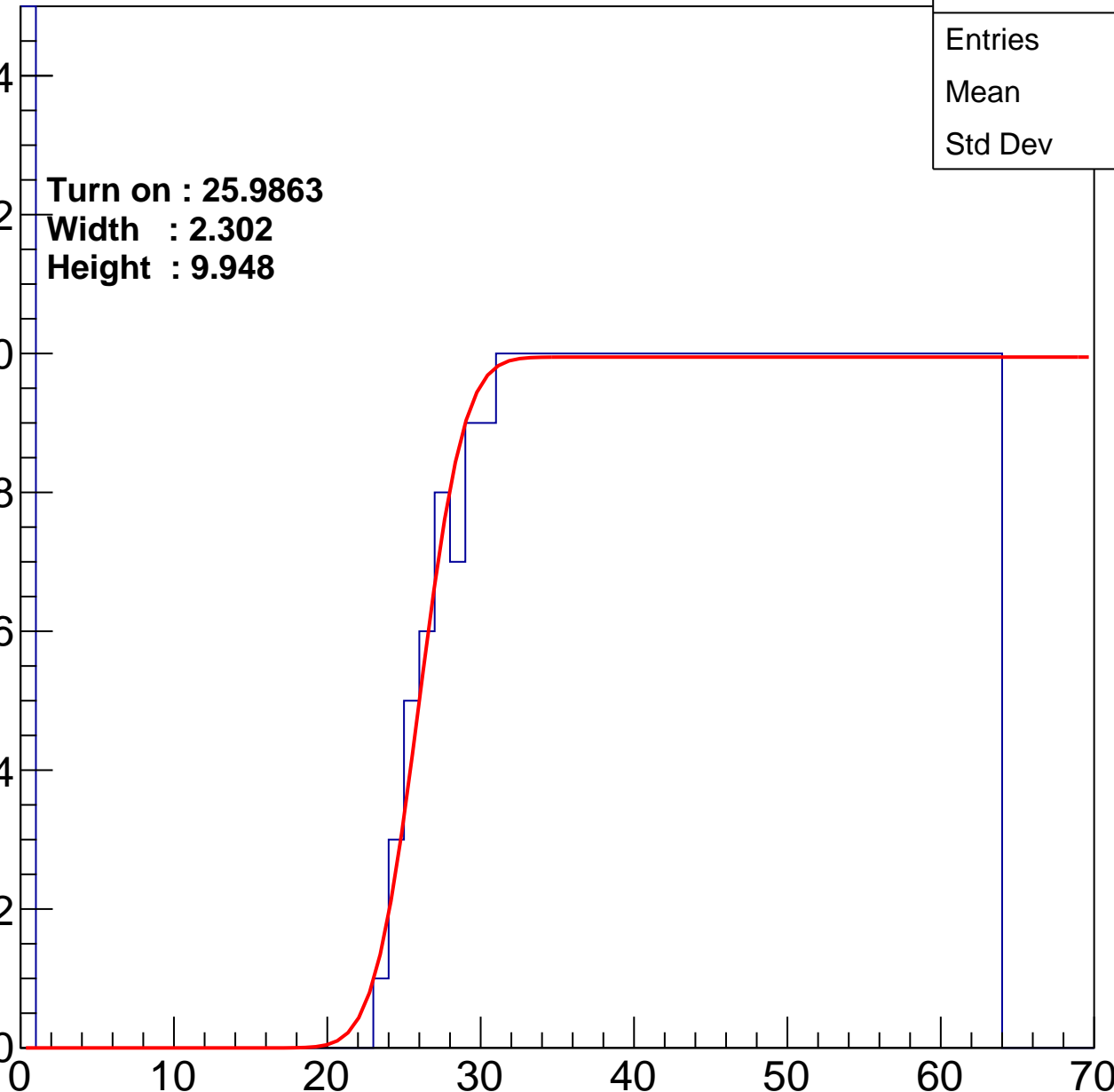
Width : 2.302

Height : 9.948

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch9

calib_packv5_041523_1651.root, FC#0, port C2

Entries	446
Mean	37.91
Std Dev	18.7

Turn on : 26.4529

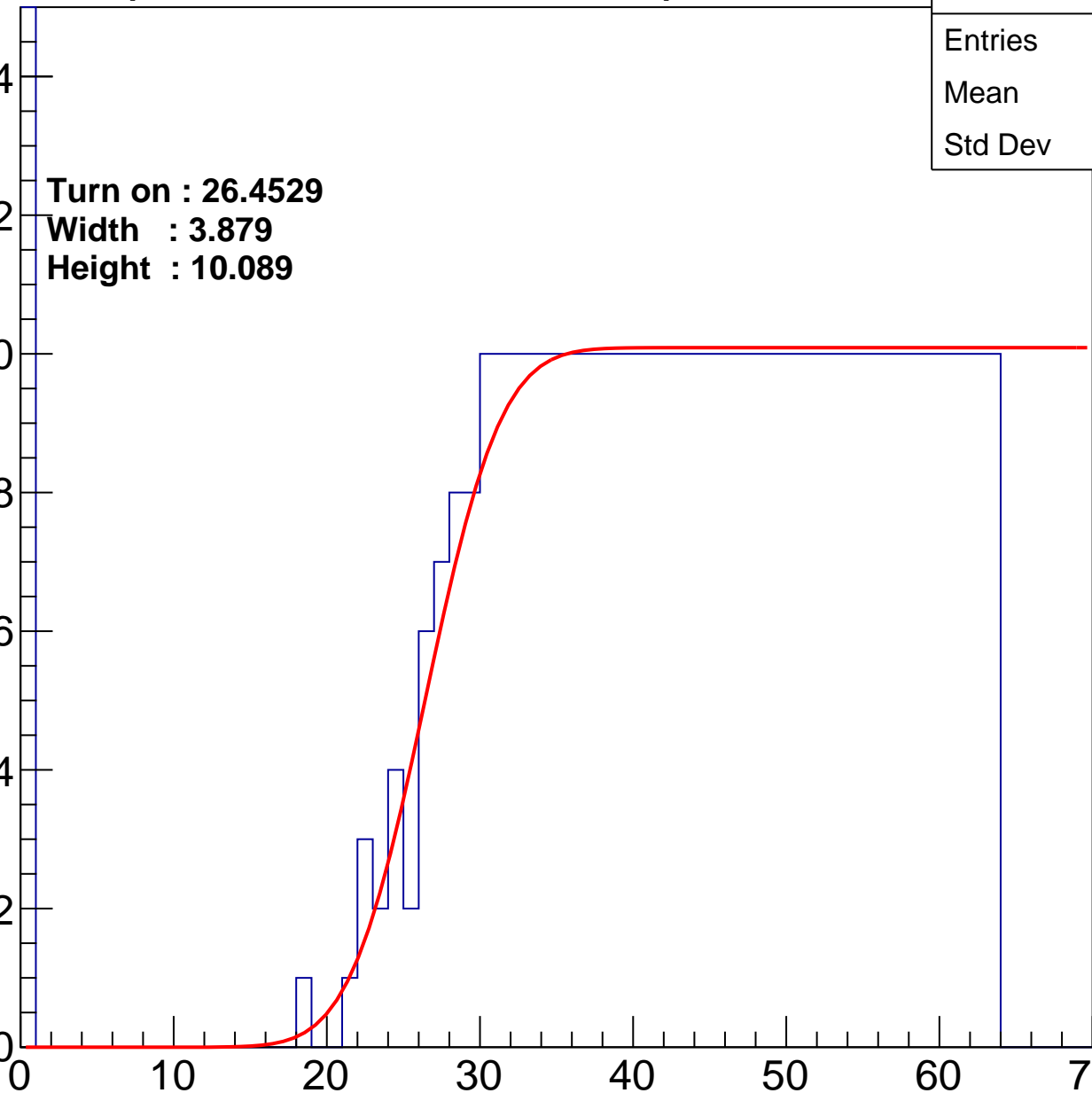
Width : 3.879

Height : 10.089

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch10

calib_packv5_041523_1651.root, FC#0, port C2

Entries	448
Mean	38.59
Std Dev	17.64

Turn on : 24.4915

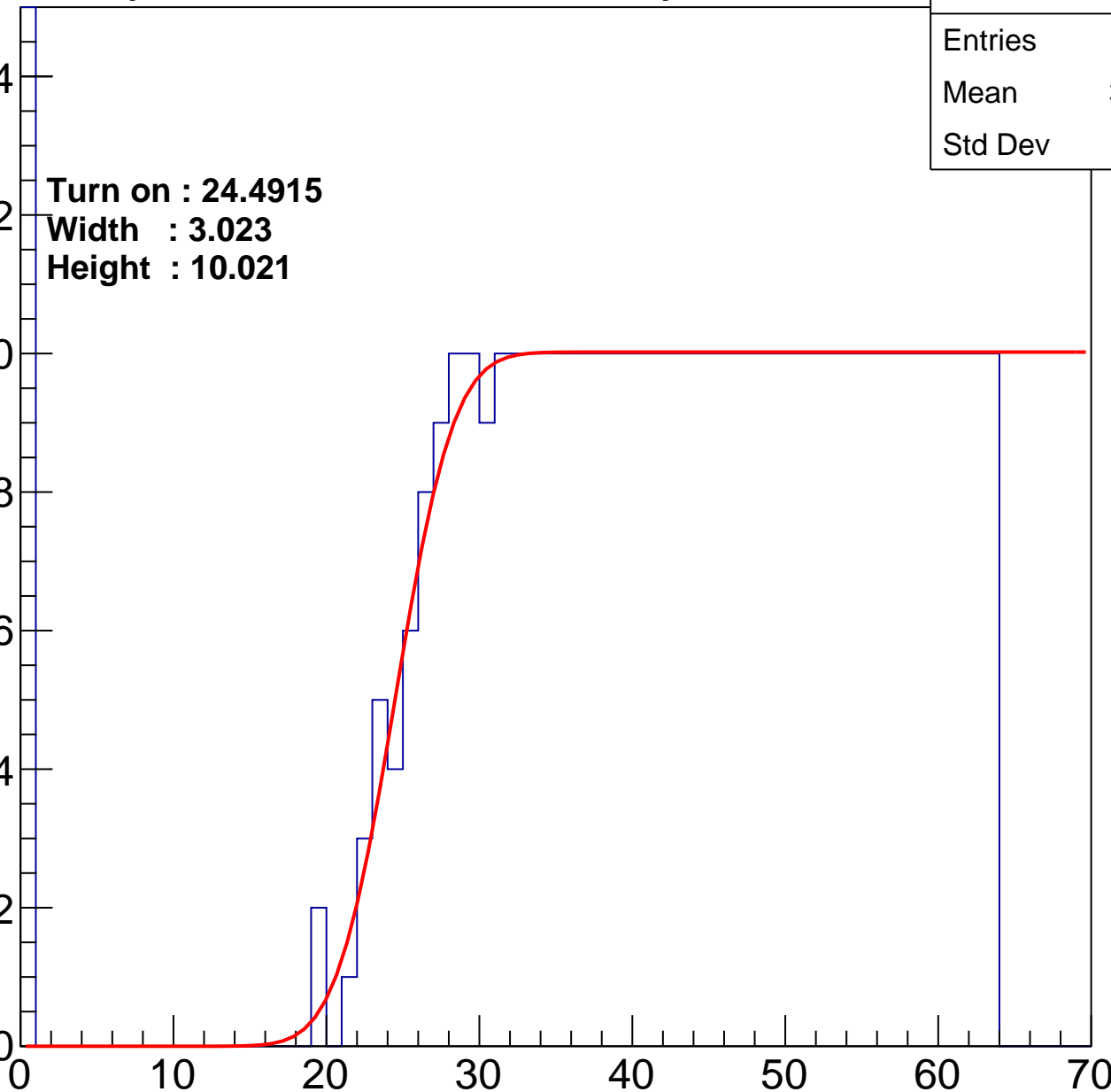
Width : 3.023

Height : 10.021

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch11

calib_packv5_041523_1651.root, FC#0, port C2

Entries	422
Mean	39.68
Std Dev	17.45

Turn on : 26.5868

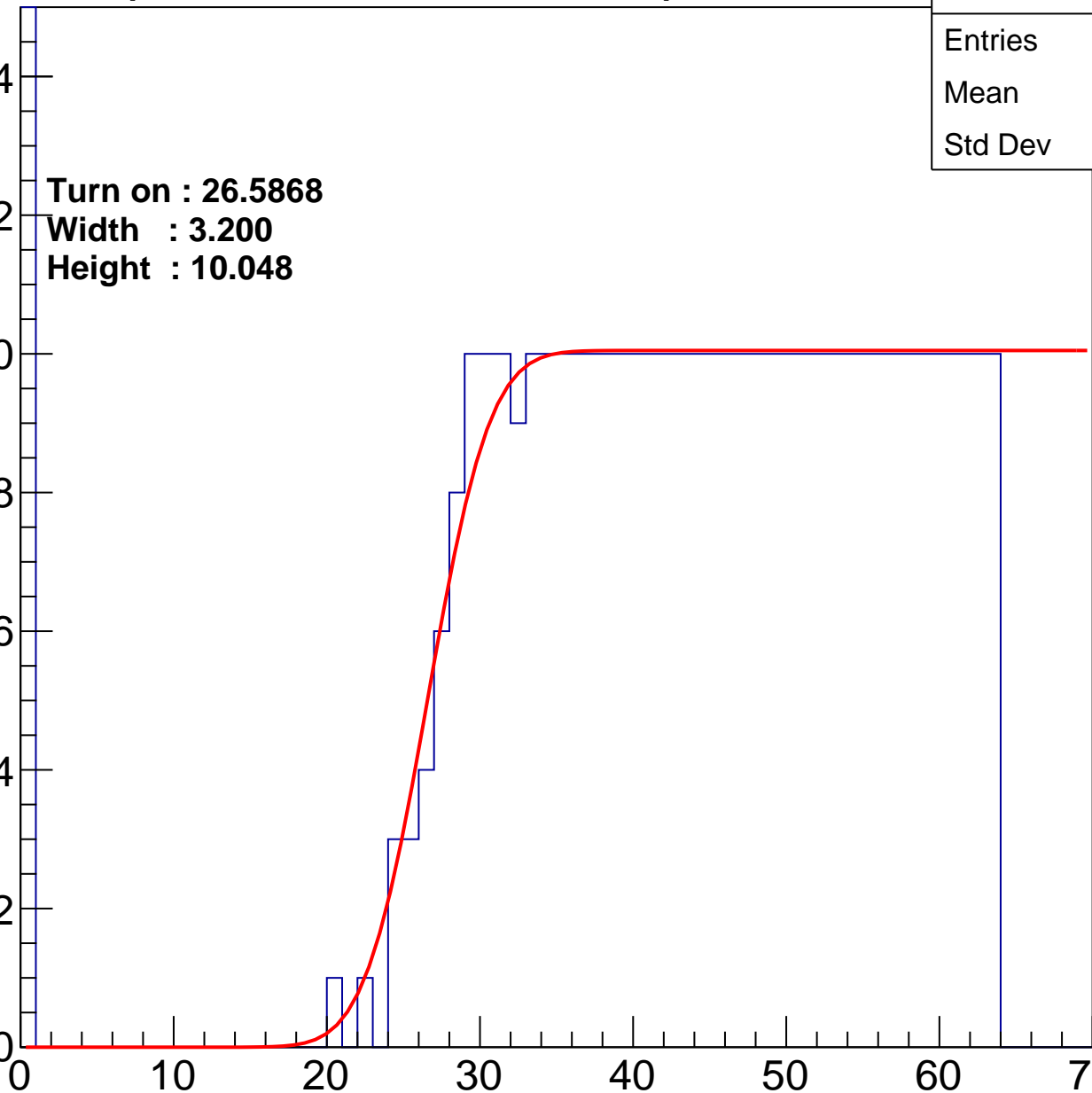
Width : 3.200

Height : 10.048

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch12

calib_packv5_041523_1651.root, FC#0, port C2

Entries	449
Mean	38
Std Dev	18.47

Turn on : 25.4900

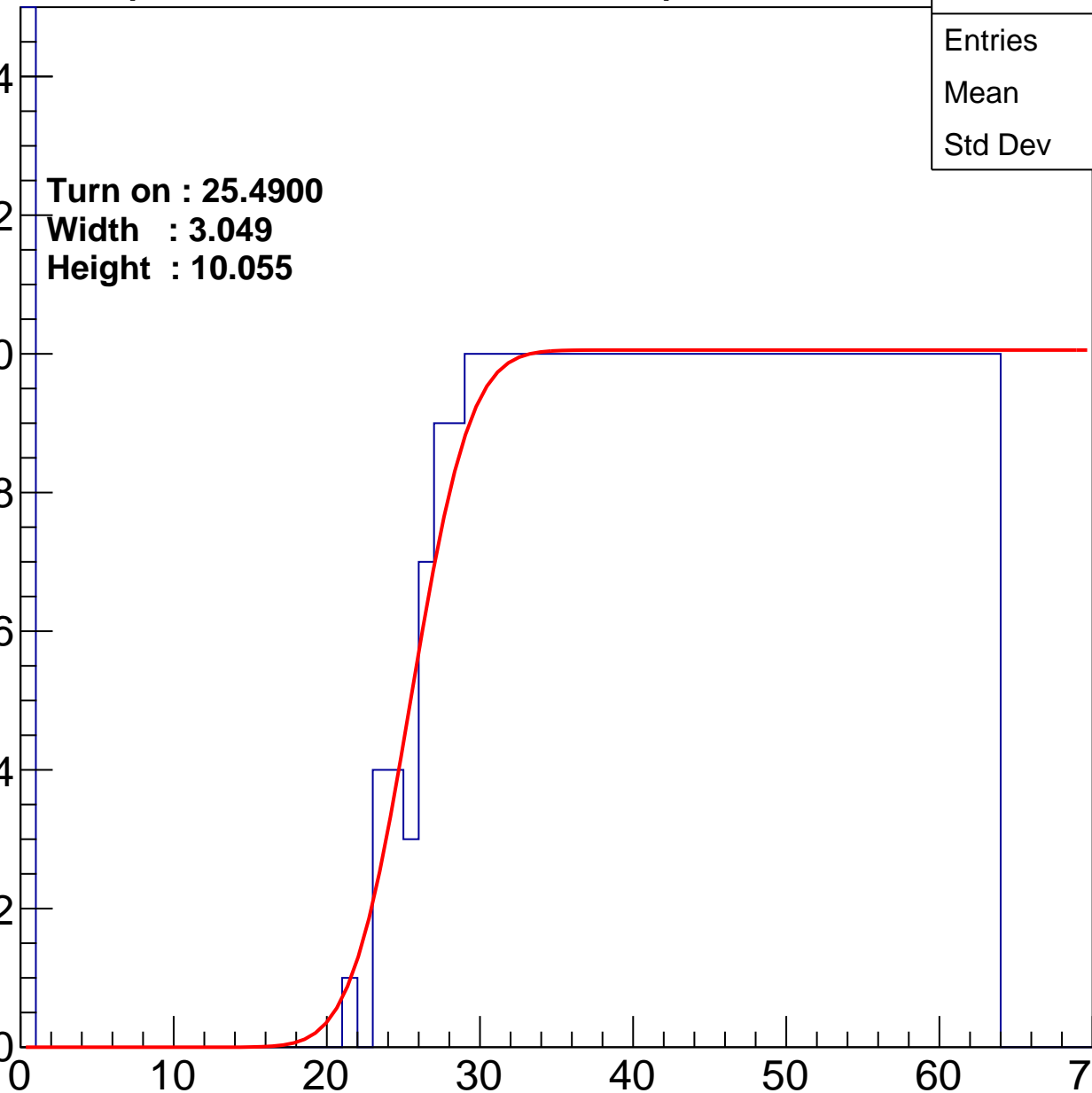
Width : 3.049

Height : 10.055

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch13

calib_packv5_041523_1651.root, FC#0, port C2

Entries	419
Mean	39.54
Std Dev	17.84

Turn on : 27.0571

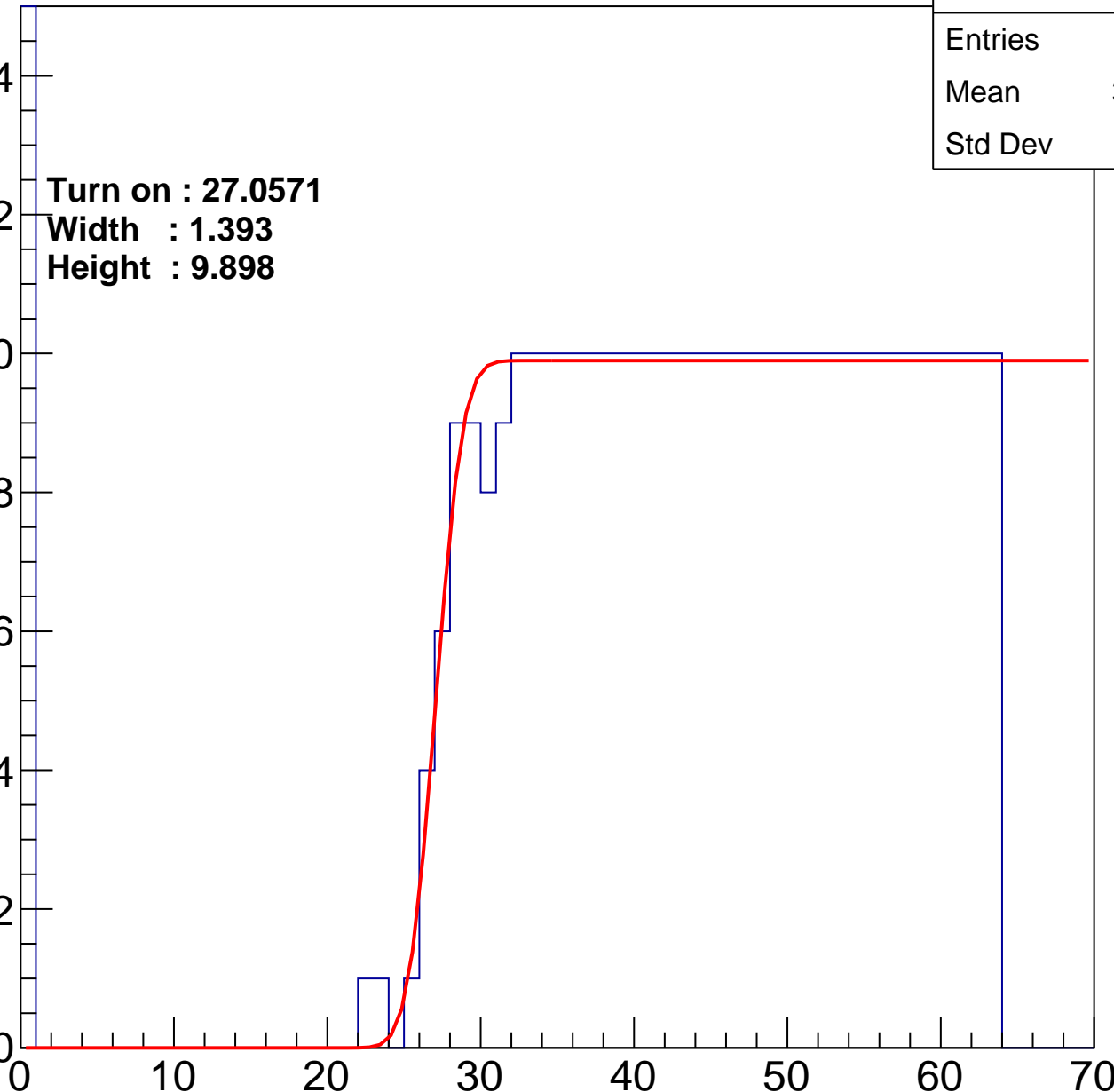
Width : 1.393

Height : 9.898

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch14

calib_packv5_041523_1651.root, FC#0, port C2

Entries	435
Mean	39.05
Std Dev	17.7

Turn on : 25.7912

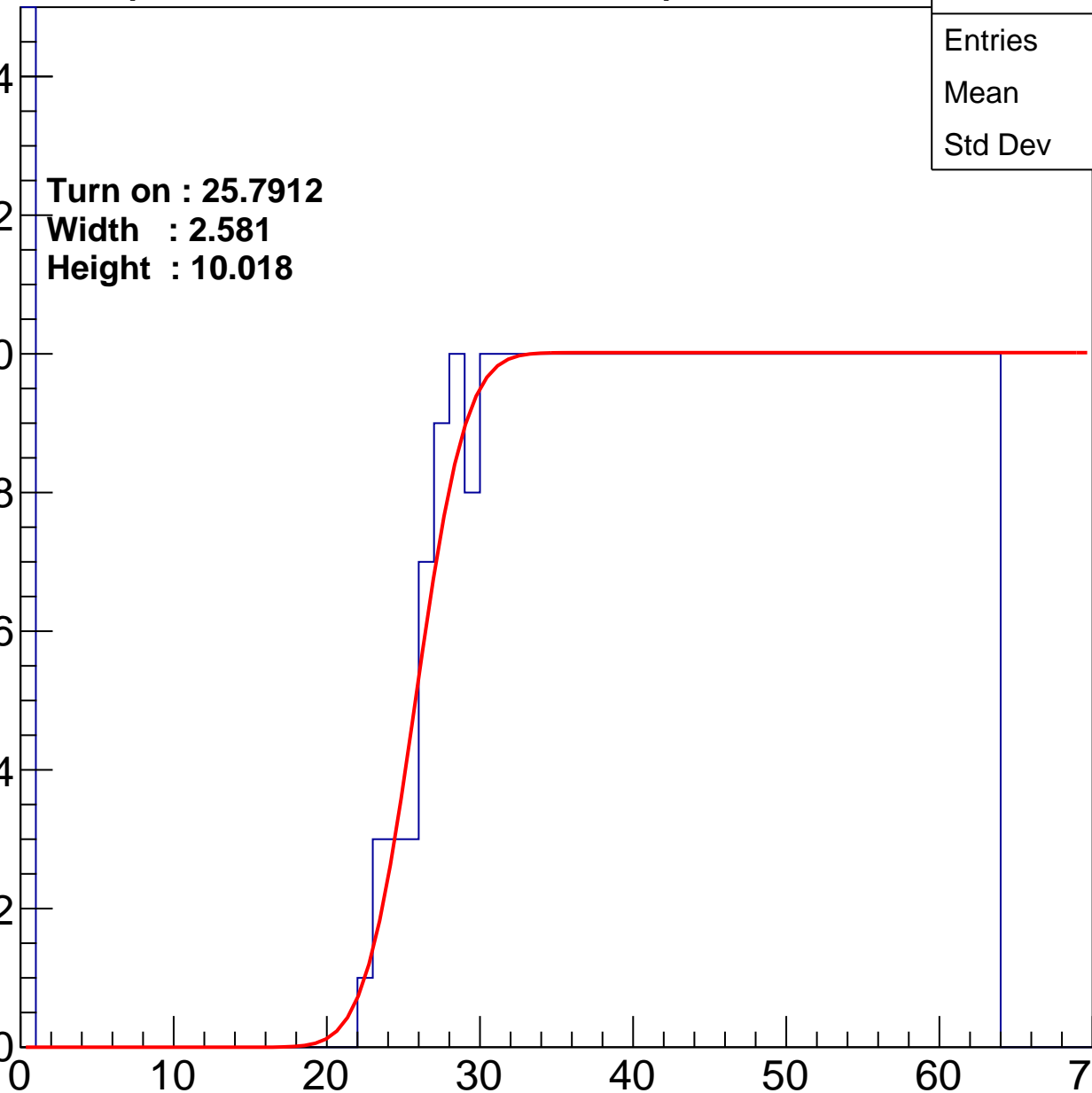
Width : 2.581

Height : 10.018

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch15

calib_packv5_041523_1651.root, FC#0, port C2

Entries	426
Mean	38.97
Std Dev	18.3

Turn on : 26.9855

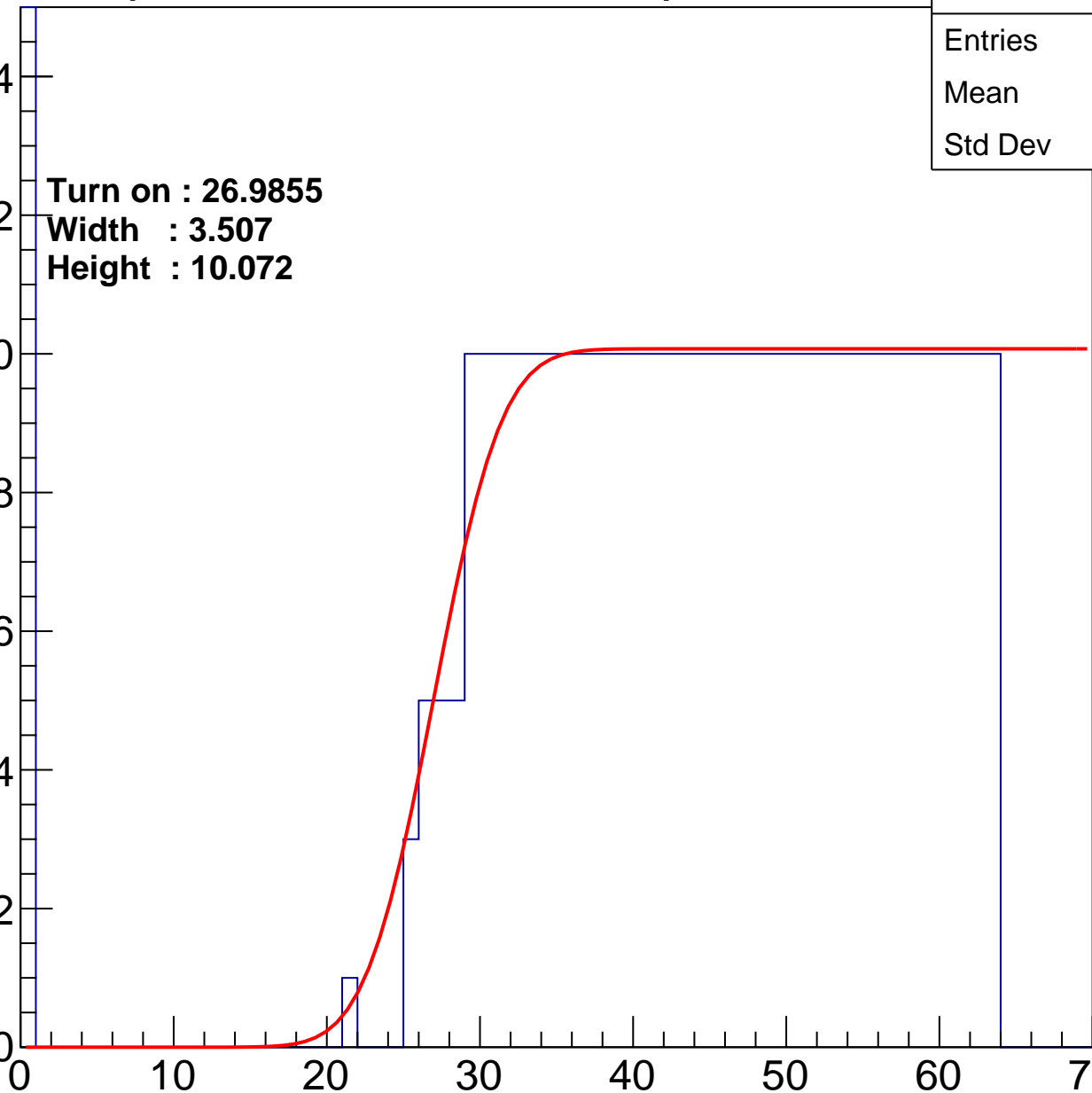
Width : 3.507

Height : 10.072

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch16

calib_packv5_041523_1651.root, FC#0, port C2

Entries	419
Mean	40.01
Std Dev	17.21

Turn on : 27.5665

Width : 2.519

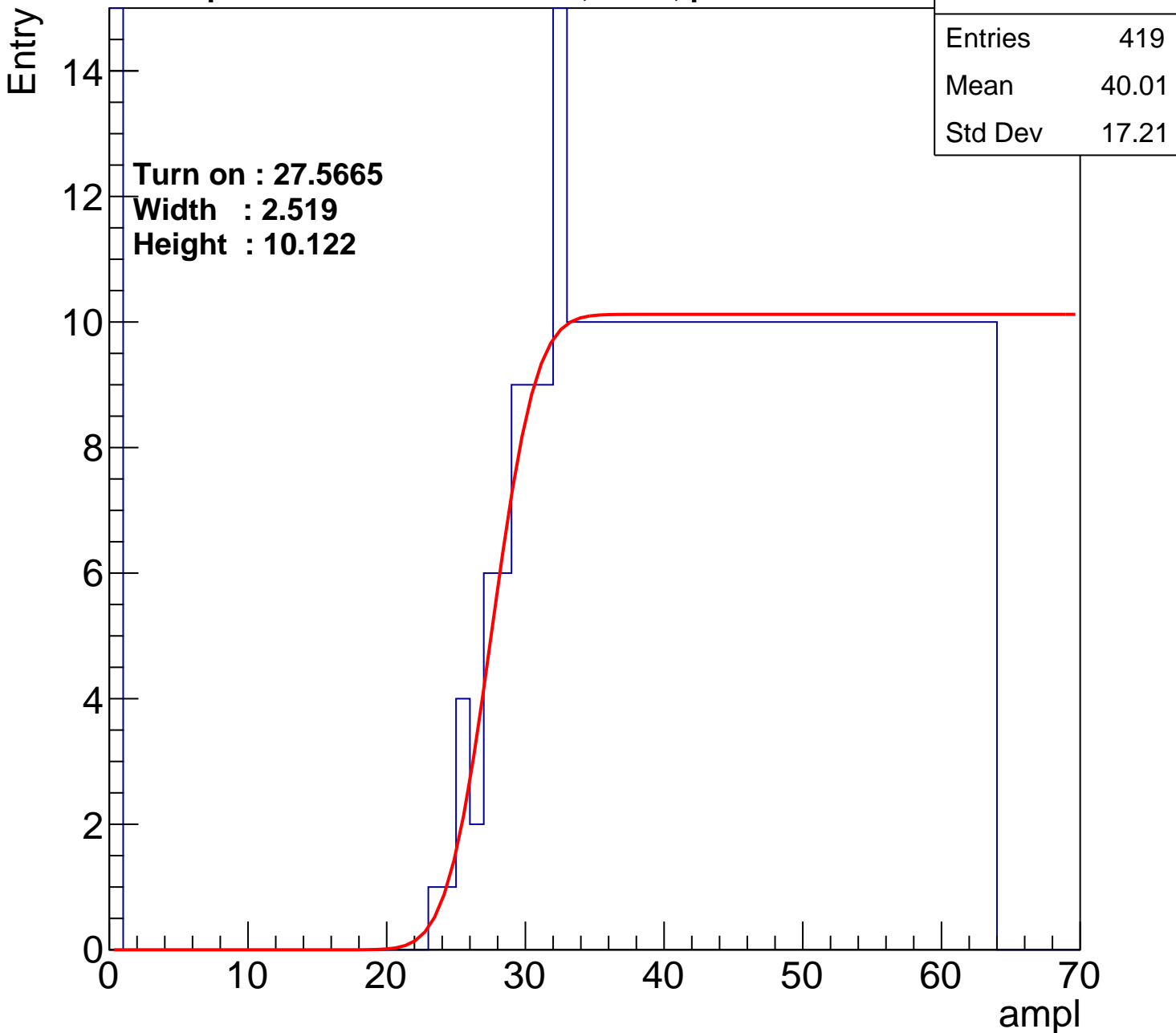
Height : 10.122

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L103S, U23-ch17

calib_packv5_041523_1651.root, FC#0, port C2

Entries	430
Mean	39.55
Std Dev	17.21

Turn on : 25.7459

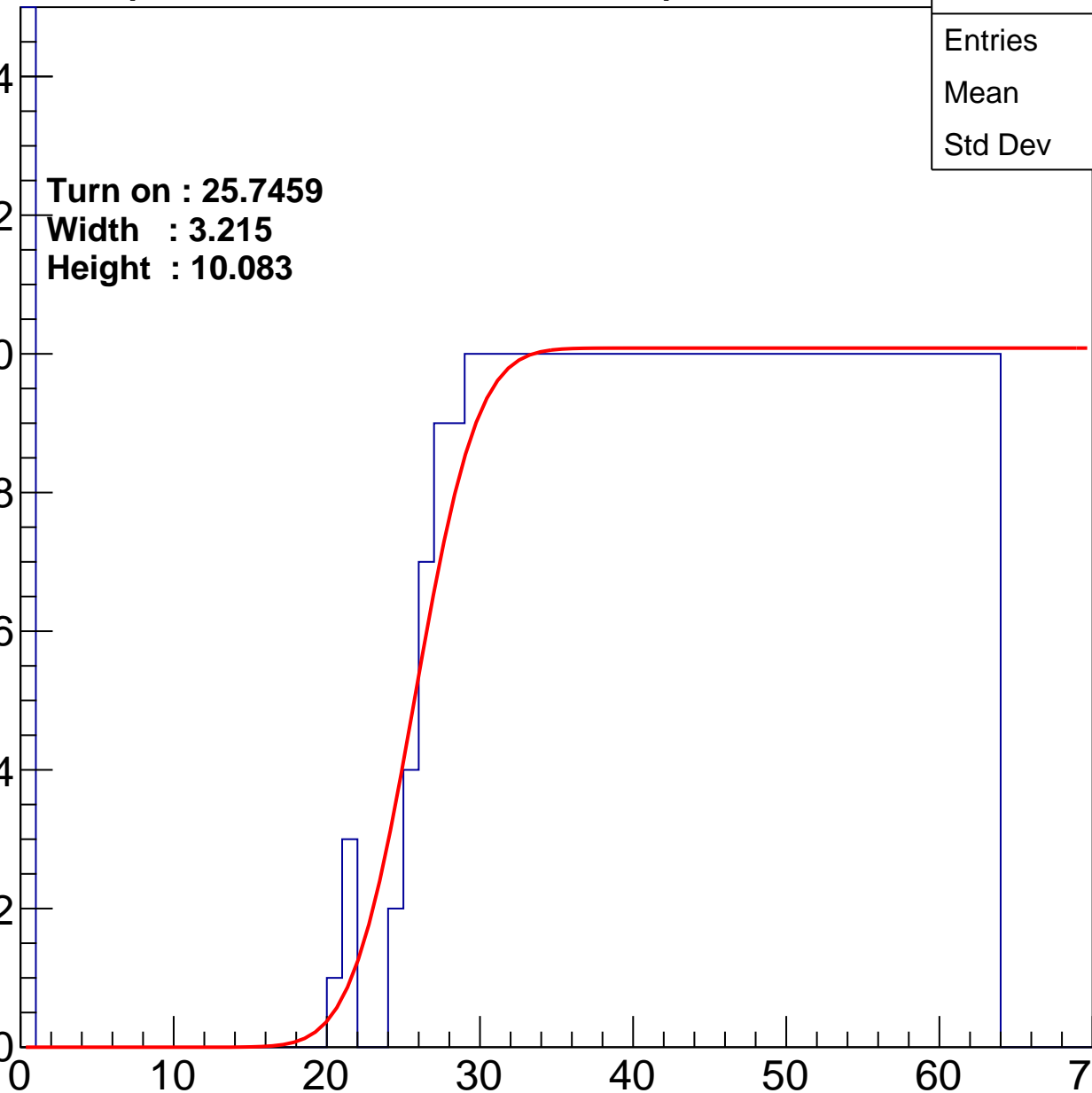
Width : 3.215

Height : 10.083

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch18

calib_packv5_041523_1651.root, FC#0, port C2

Entries	434
Mean	39.26
Std Dev	17.44

Turn on : 25.4958

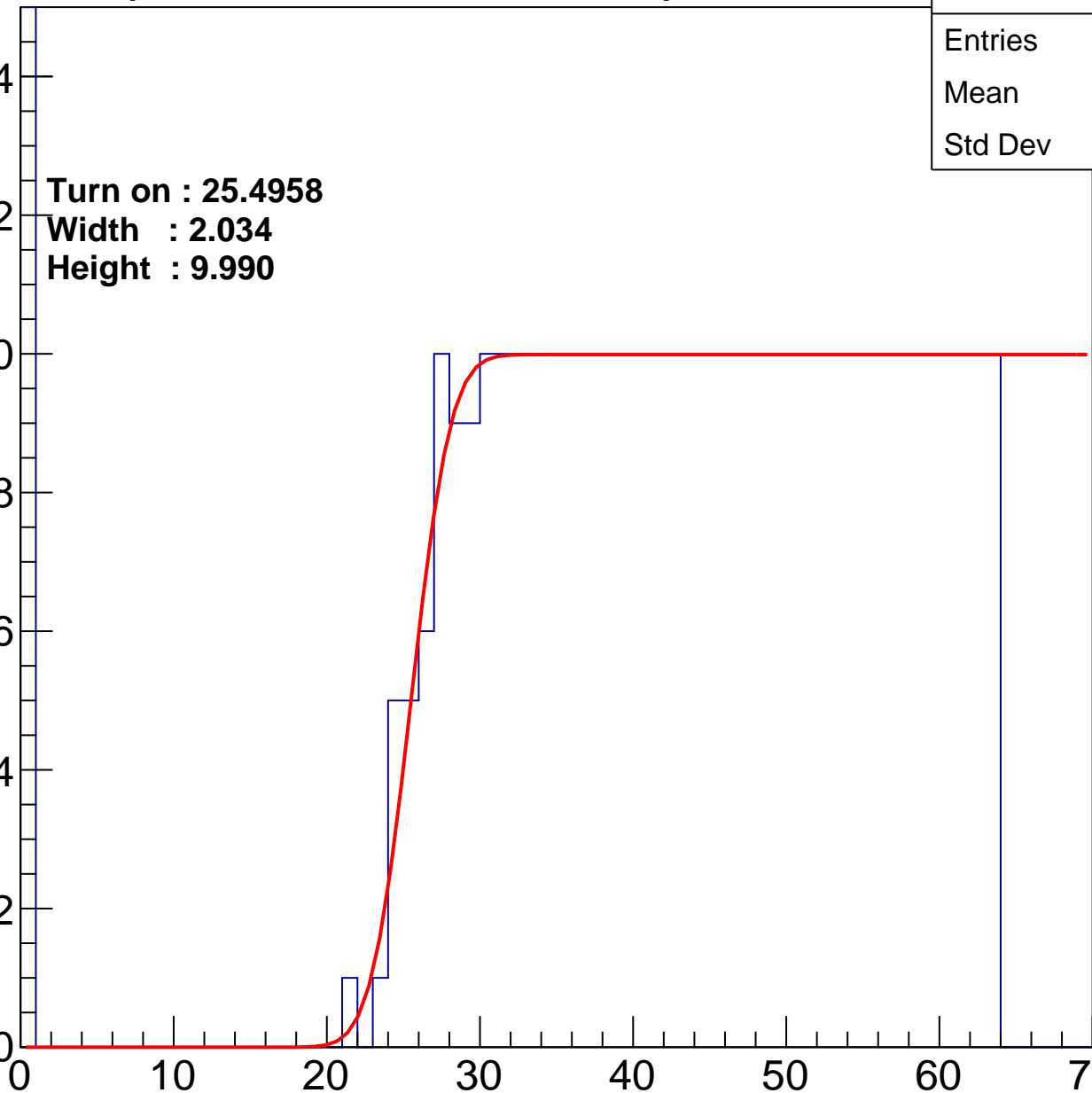
Width : 2.034

Height : 9.990

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch19

calib_packv5_041523_1651.root, FC#0, port C2

Entries	439
Mean	38.6
Std Dev	18.11

Turn on : 26.1351

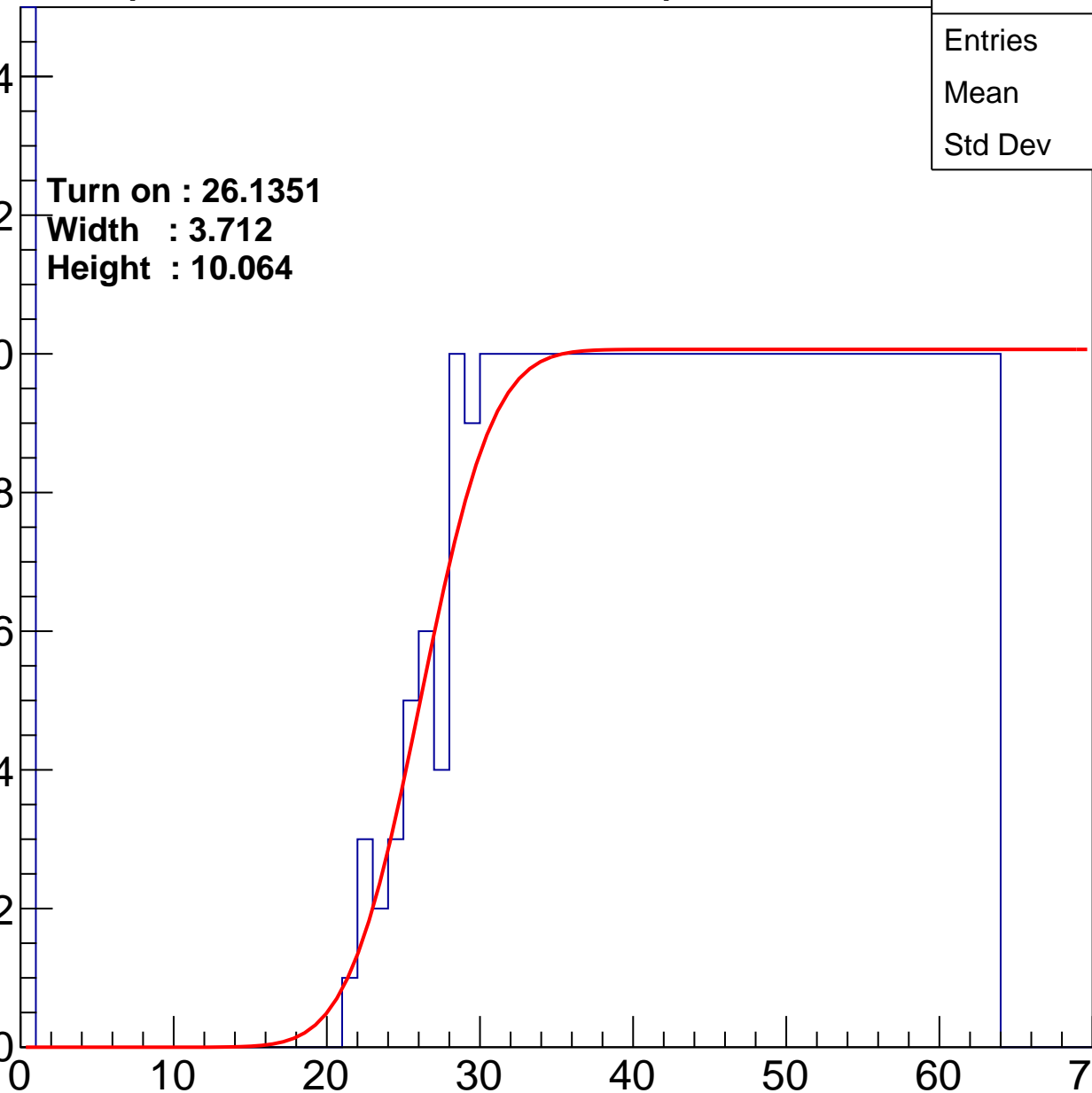
Width : 3.712

Height : 10.064

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch20

calib_packv5_041523_1651.root, FC#0, port C2

Entries	418
Mean	40.52
Std Dev	16.33

Turn on : 25.6898

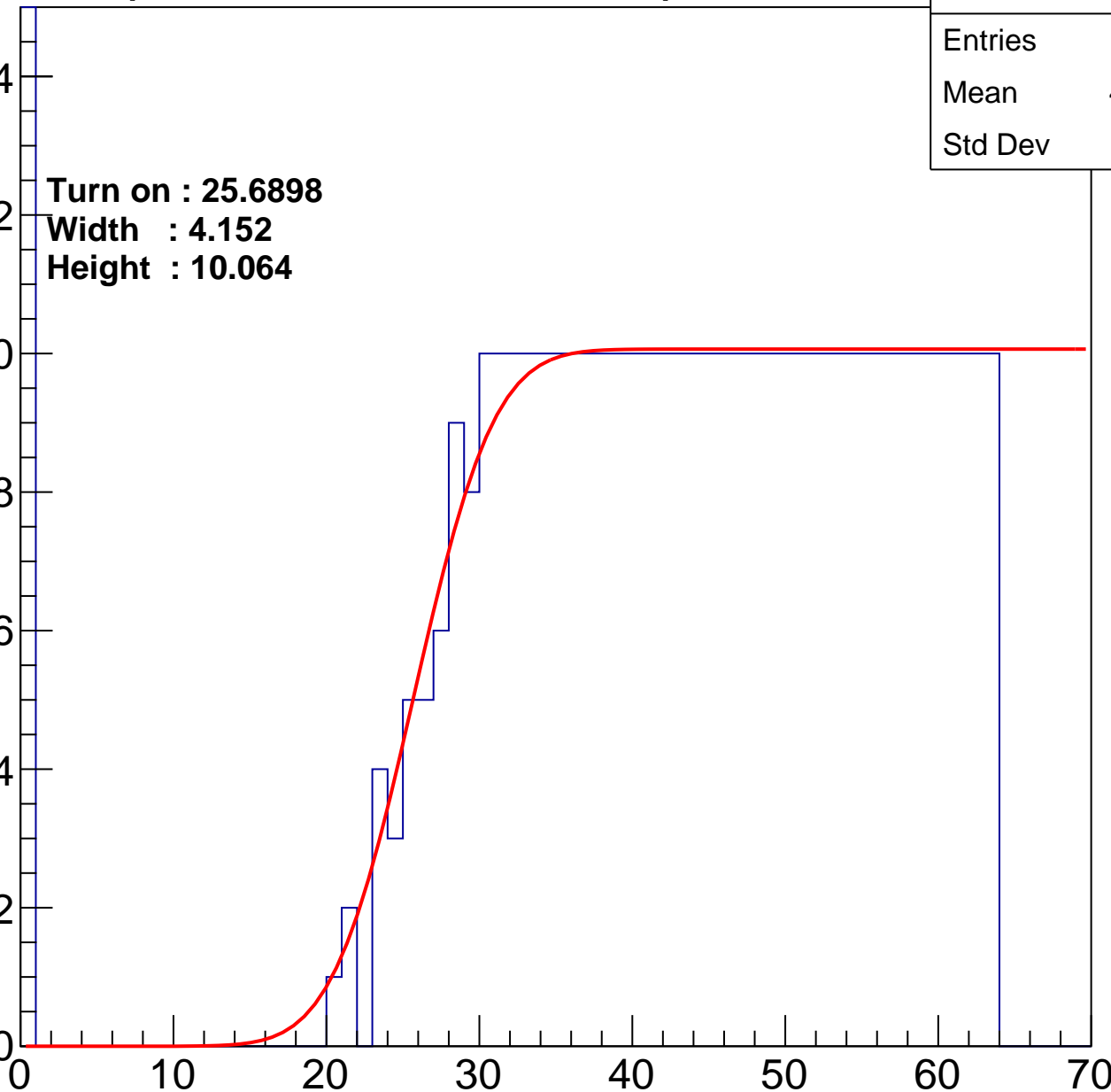
Width : 4.152

Height : 10.064

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch21

calib_packv5_041523_1651.root, FC#0, port C2

Entries	421
Mean	39.71
Std Dev	17.47

Turn on : 27.0669

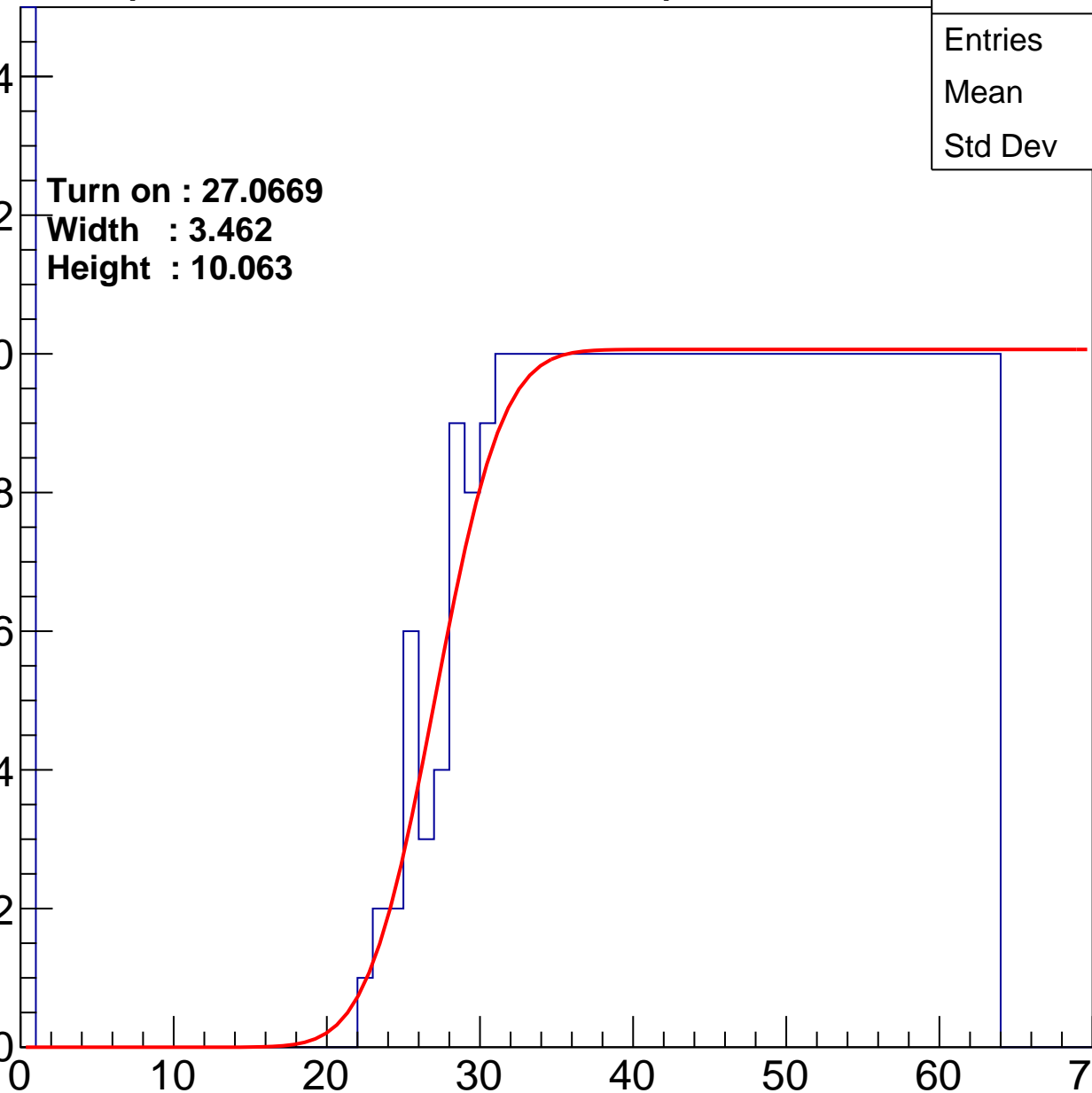
Width : 3.462

Height : 10.063

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch22

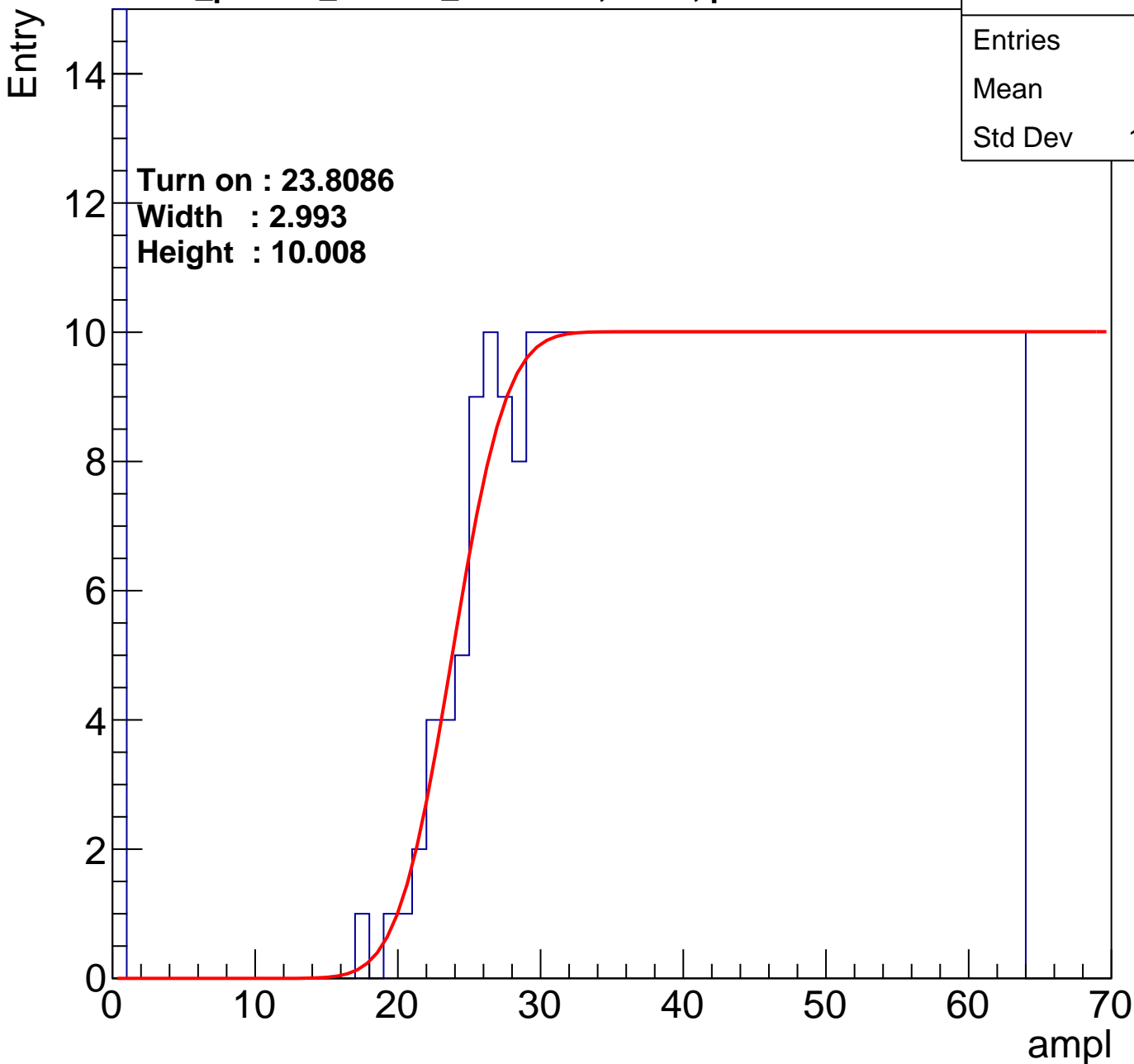
calib_packv5_041523_1651.root, FC#0, port C2

Entries	458
Mean	38.1
Std Dev	17.83

Turn on : 23.8086

Width : 2.993

Height : 10.008



B1L103S, U23-ch23

calib_packv5_041523_1651.root, FC#0, port C2

Entries	422
Mean	39.57
Std Dev	17.63

Turn on : 26.9837

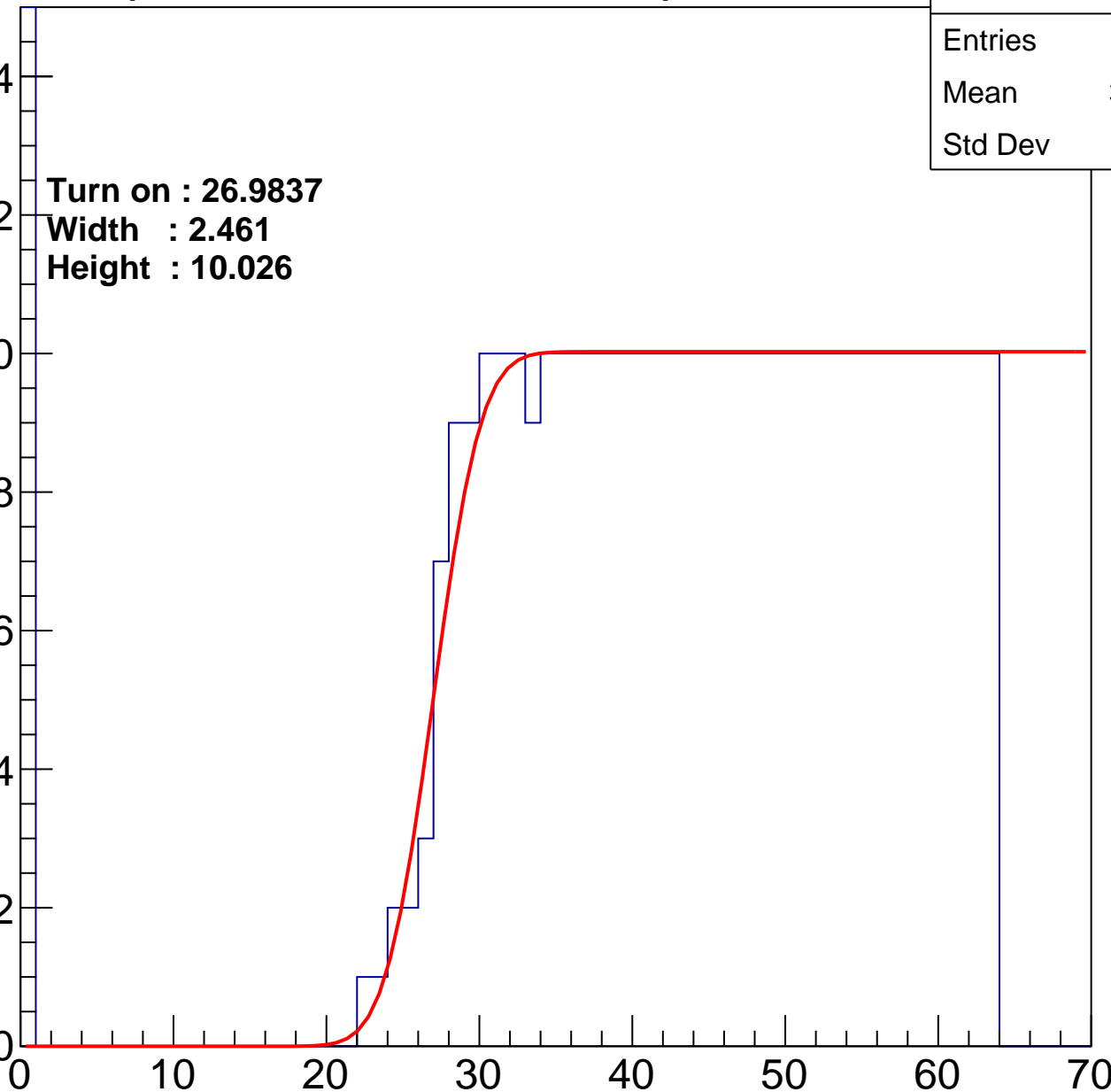
Width : 2.461

Height : 10.026

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch24

calib_packv5_041523_1651.root, FC#0, port C2

Entries	454
Mean	37.59
Std Dev	18.78

Turn on : 25.0218

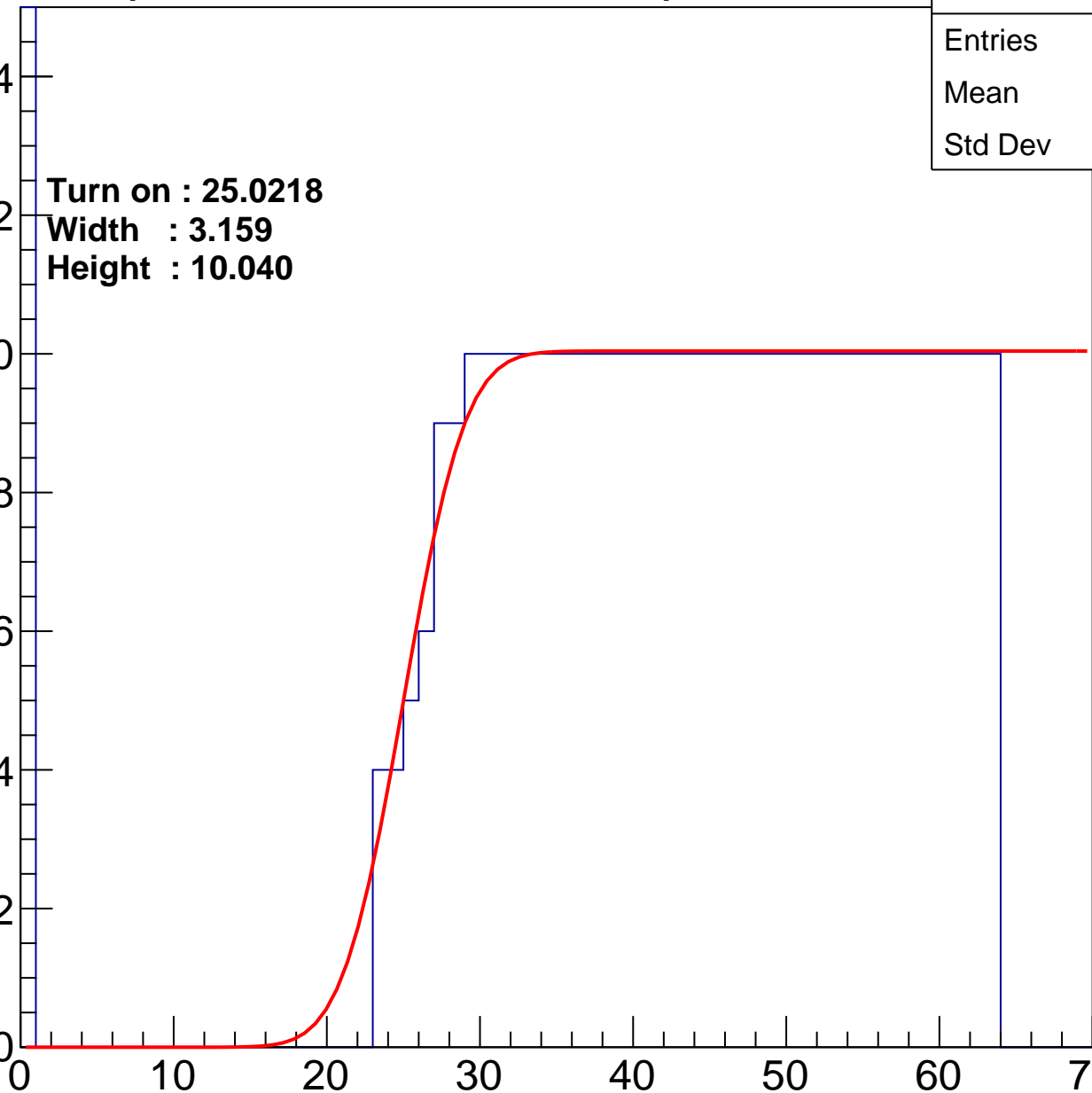
Width : 3.159

Height : 10.040

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch25

calib_packv5_041523_1651.root, FC#0, port C2

Entries	446
Mean	38.29
Std Dev	18.19

Turn on : 25.0615

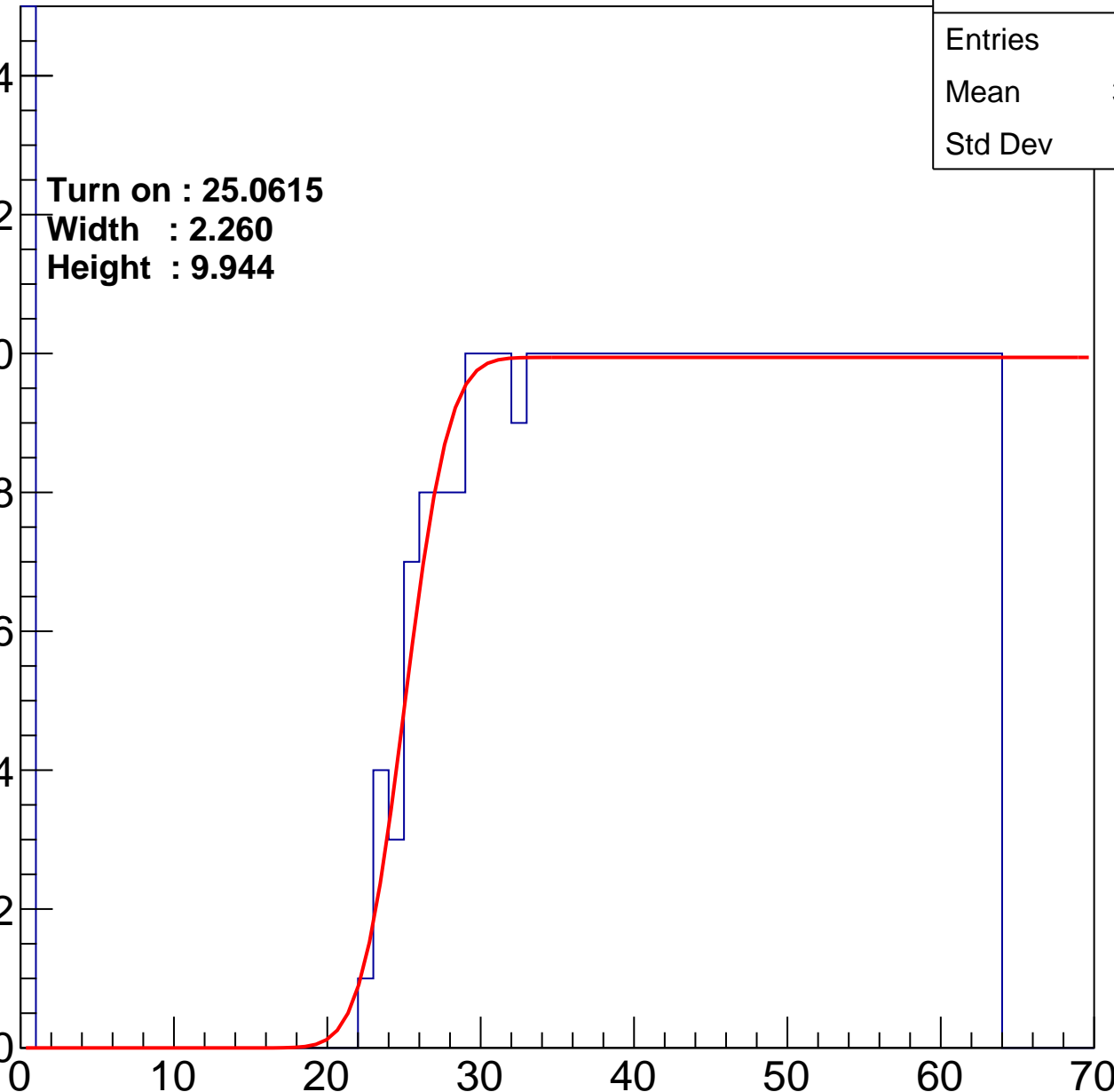
Width : 2.260

Height : 9.944

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch26

calib_packv5_041523_1651.root, FC#0, port C2

Entries	445
Mean	38.33
Std Dev	18.2

Turn on : 25.5932

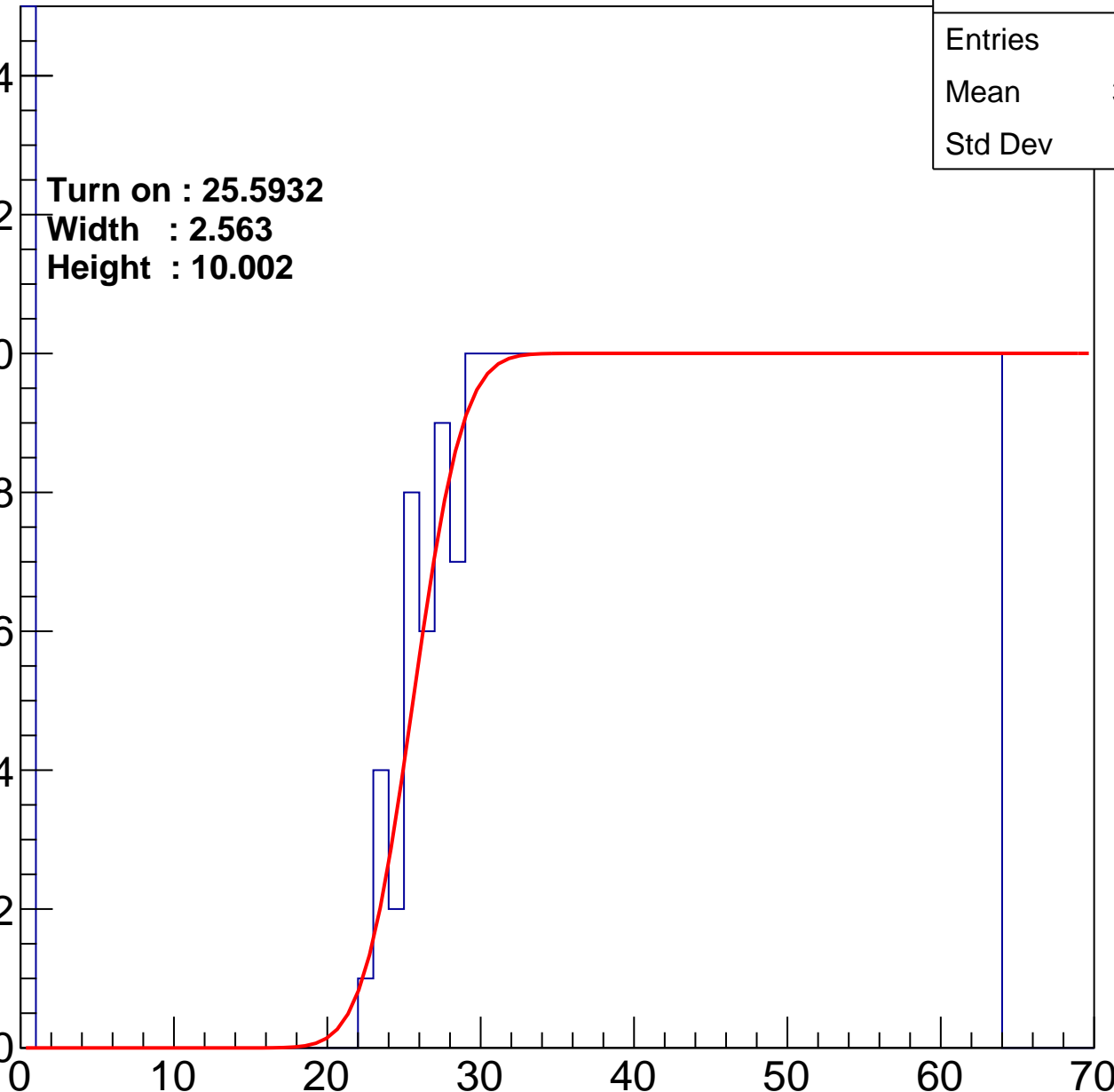
Width : 2.563

Height : 10.002

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch27

calib_packv5_041523_1651.root, FC#0, port C2

Entries	452
Mean	37.6
Std Dev	18.83

Turn on : 25.7274

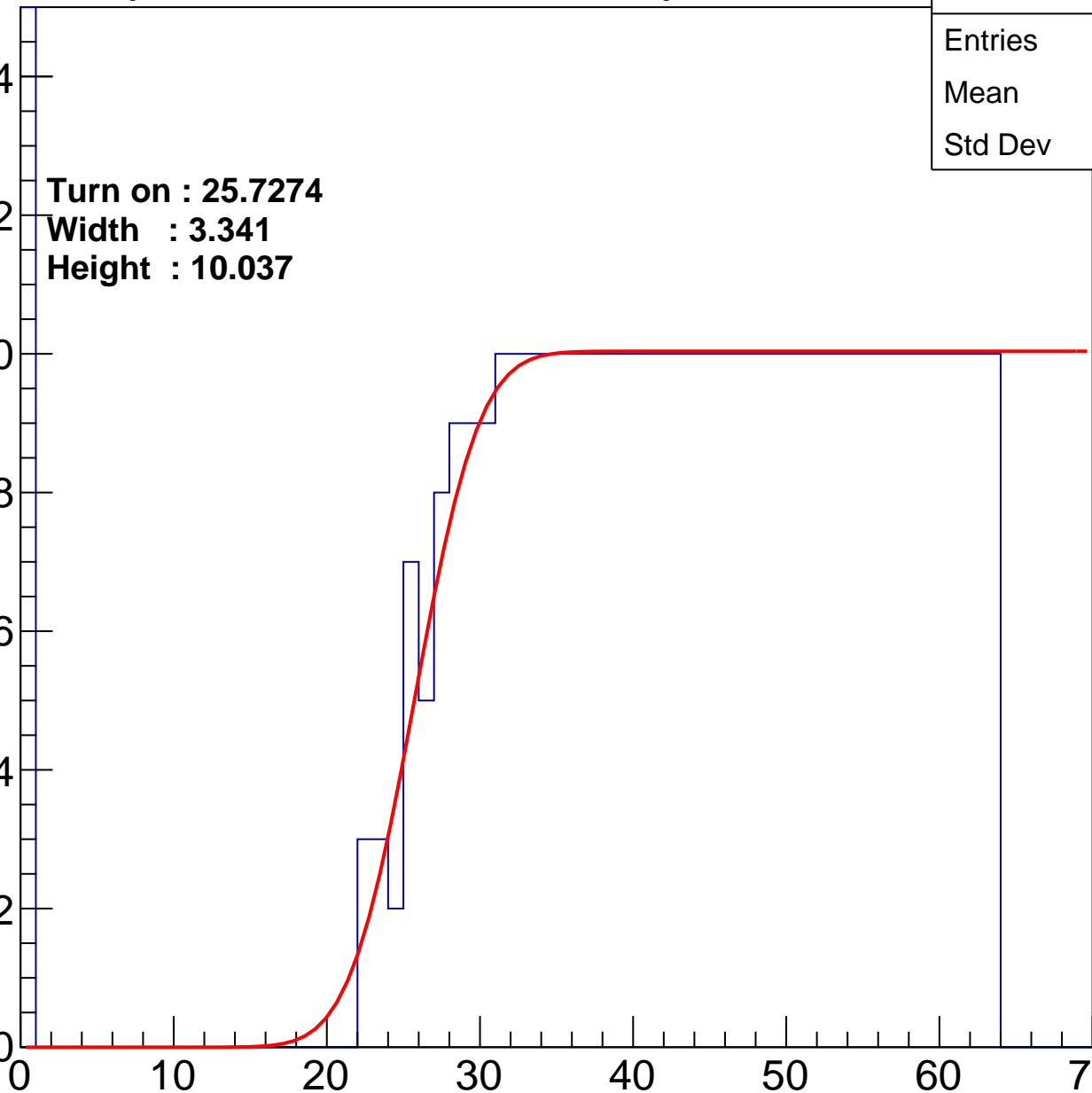
Width : 3.341

Height : 10.037

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch28

calib_packv5_041523_1651.root, FC#0, port C2

Entries	468
Mean	37.17
Std Dev	18.67

Turn on : 24.0479

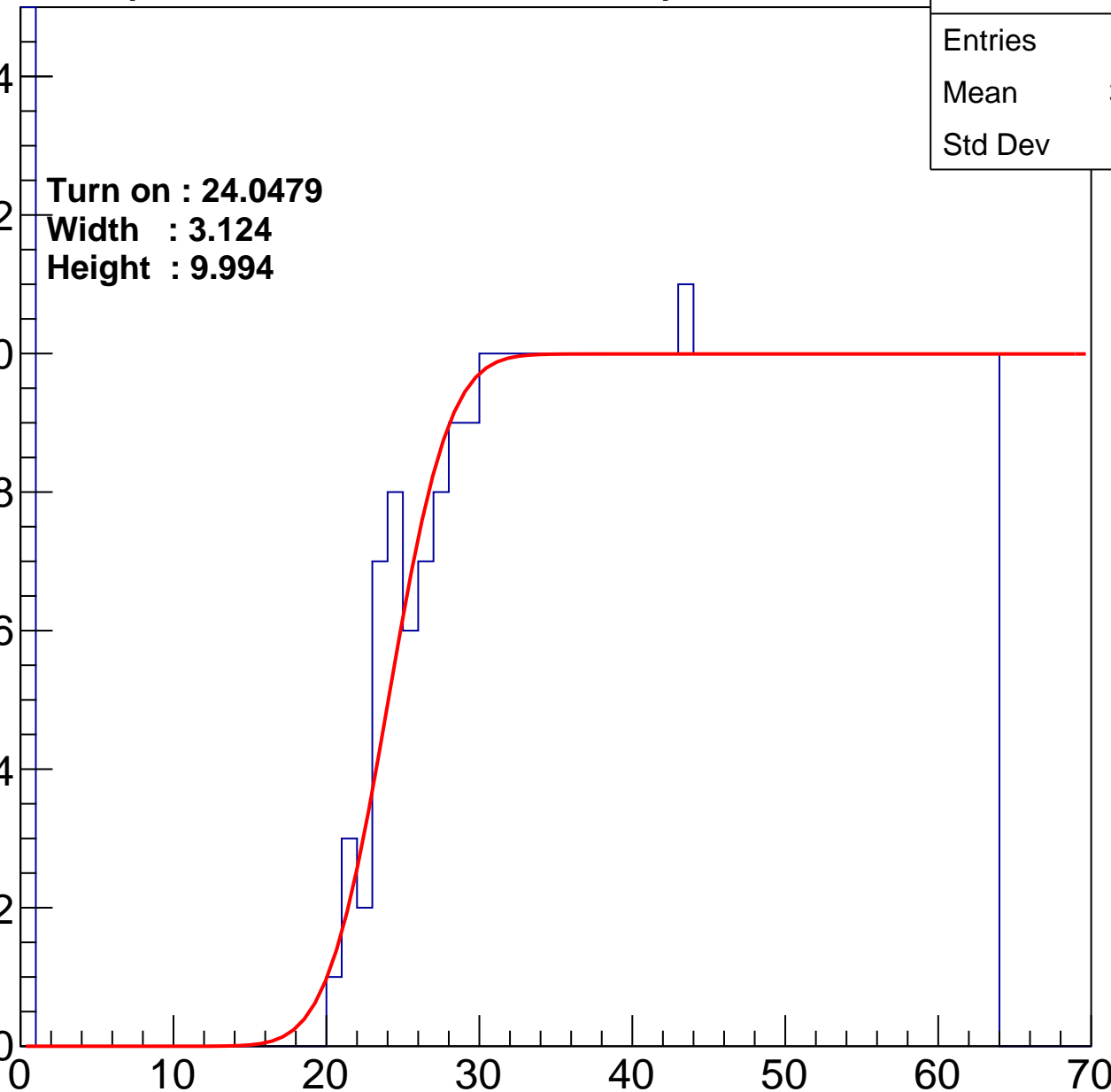
Width : 3.124

Height : 9.994

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch29

calib_packv5_041523_1651.root, FC#0, port C2

Entries	440
Mean	37.32
Std Dev	19.77

Turn on : 27.7815

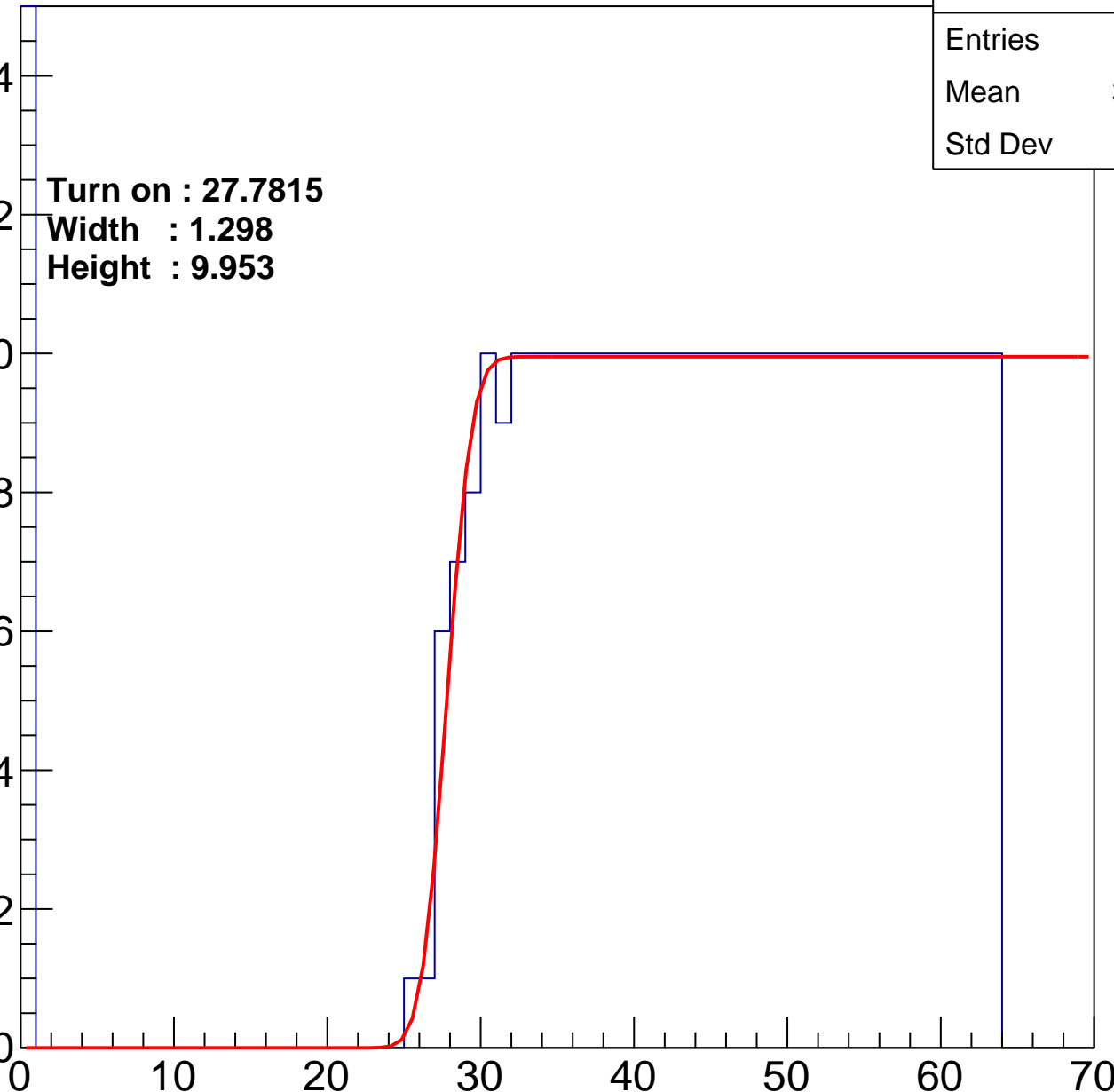
Width : 1.298

Height : 9.953

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch30

calib_packv5_041523_1651.root, FC#0, port C2

Entries	442
Mean	38.8
Std Dev	17.66

Turn on : 24.6578

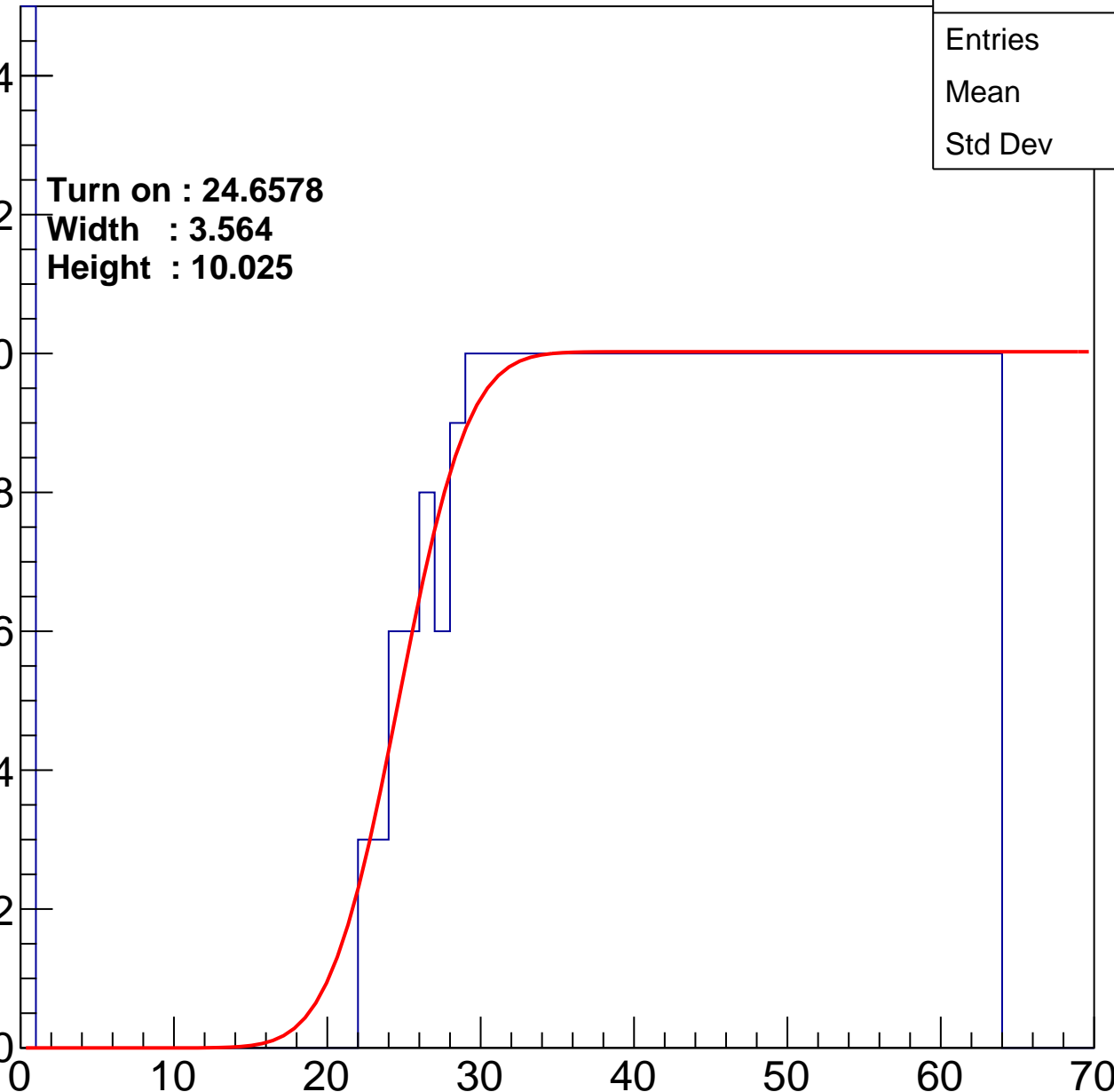
Width : 3.564

Height : 10.025

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch31

calib_packv5_041523_1651.root, FC#0, port C2

Entries	441
Mean	38.34
Std Dev	18.35

Turn on : 26.2547

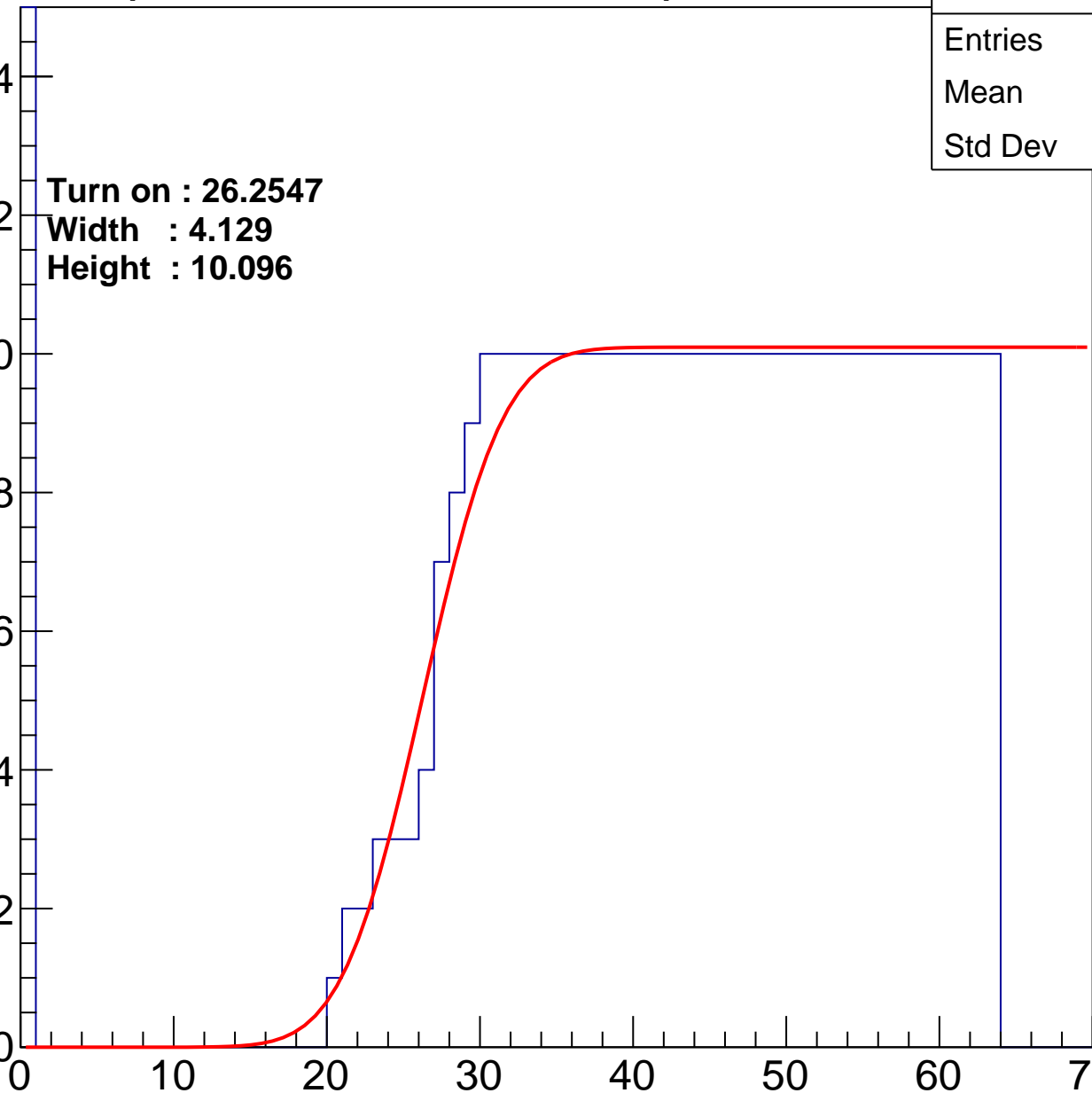
Width : 4.129

Height : 10.096

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch32

calib_packv5_041523_1651.root, FC#0, port C2

Entries	438
Mean	38.94
Std Dev	17.68

Turn on : 25.2612

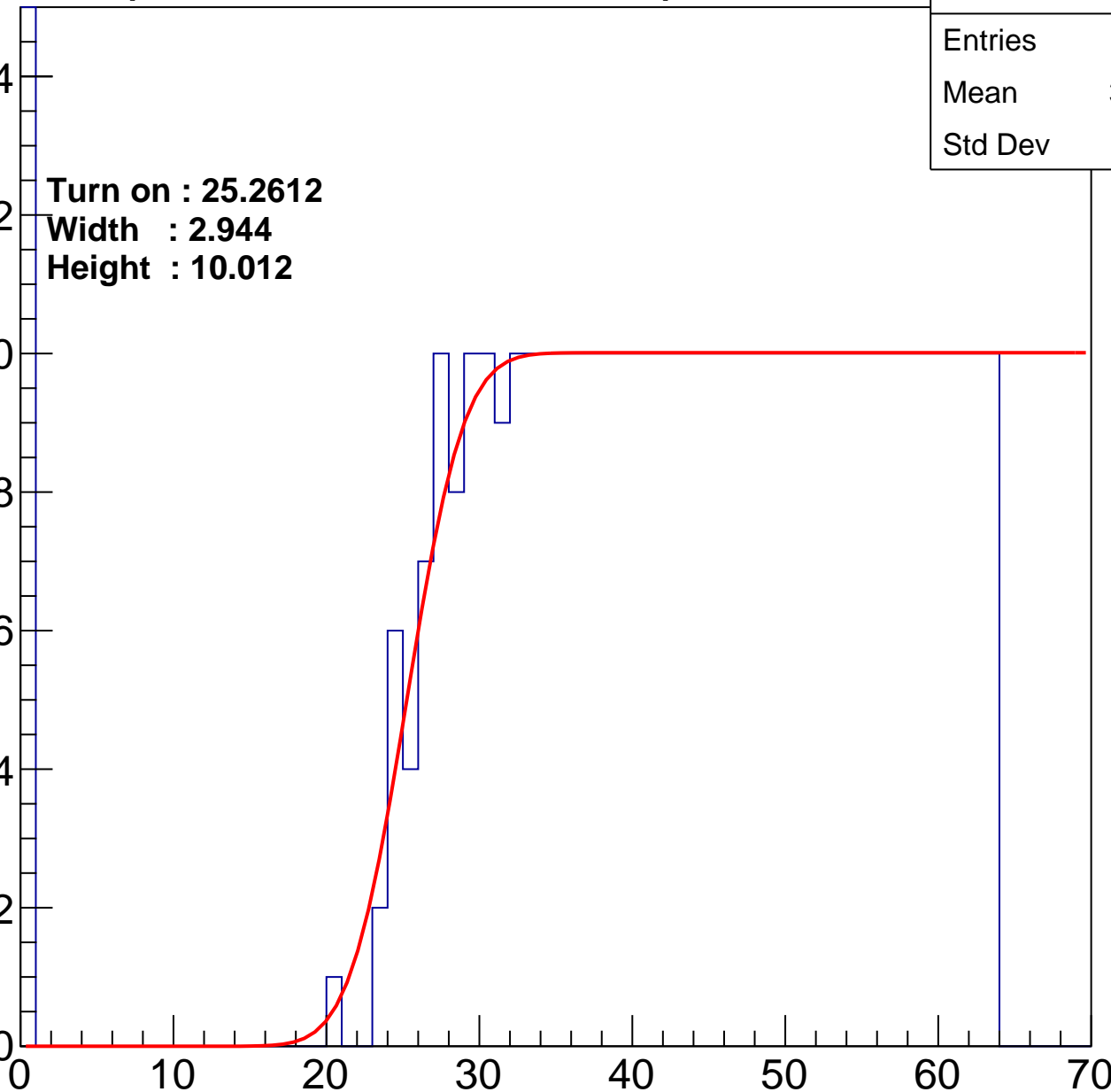
Width : 2.944

Height : 10.012

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch33

calib_packv5_041523_1651.root, FC#0, port C2

Entries	440
Mean	38.65
Std Dev	18

Turn on : 25.0806

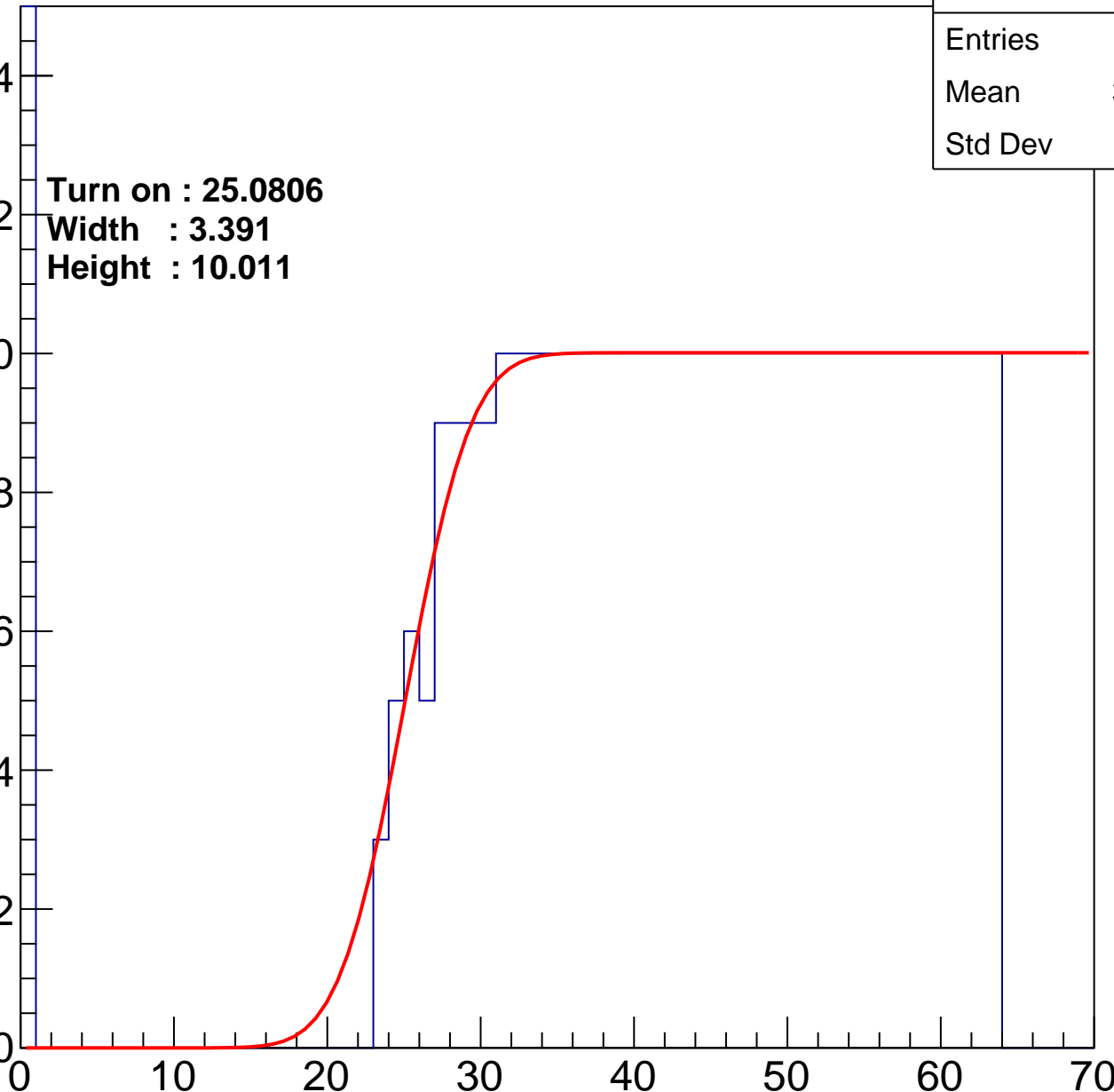
Width : 3.391

Height : 10.011

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch34

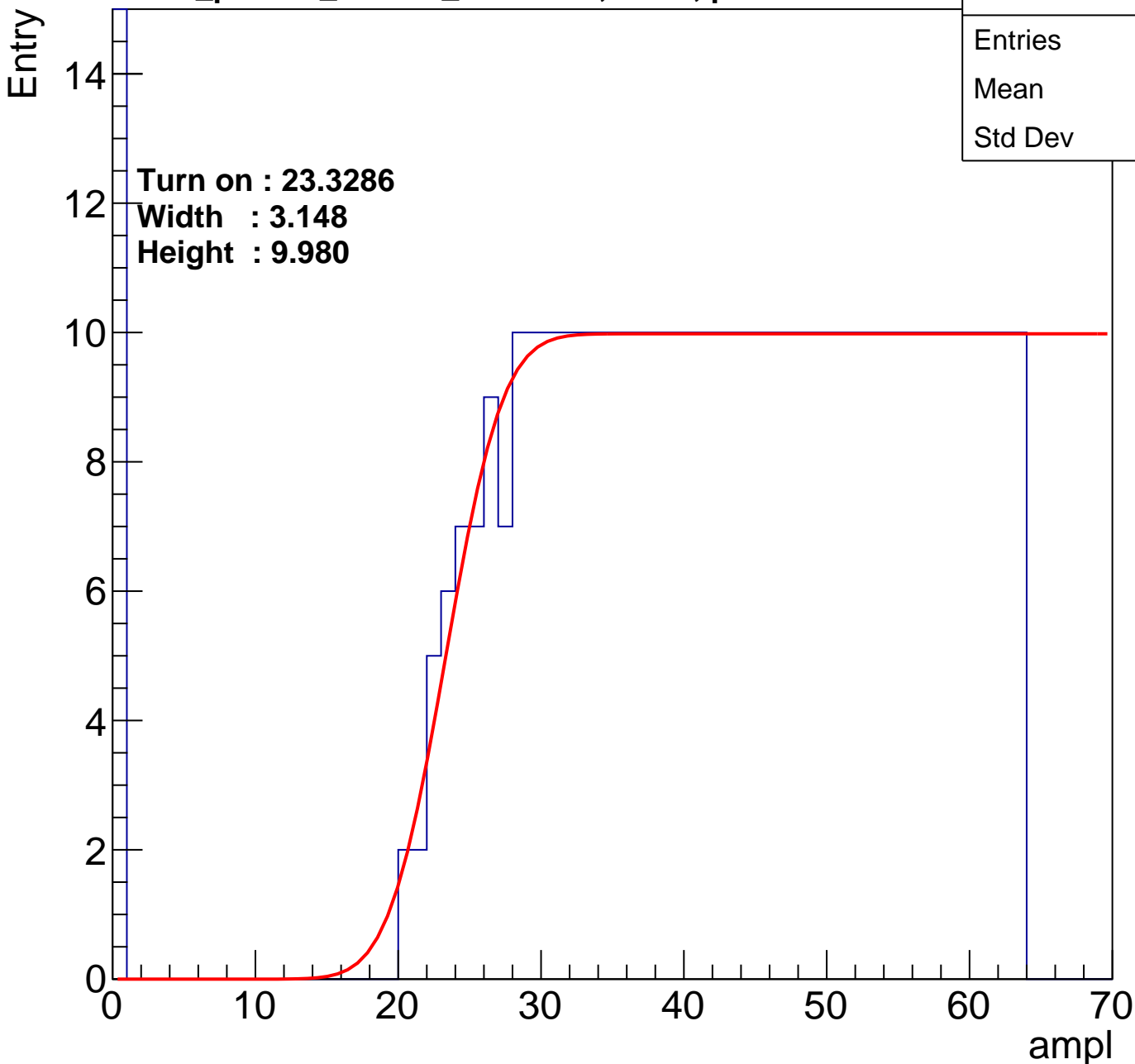
calib_packv5_041523_1651.root, FC#0, port C2

Entries	447
Mean	39.1
Std Dev	16.91

Turn on : 23.3286

Width : 3.148

Height : 9.980



B1L103S, U23-ch35

calib_packv5_041523_1651.root, FC#0, port C2

Entries	417
Mean	39.76
Std Dev	17.61

Turn on : 27.1844

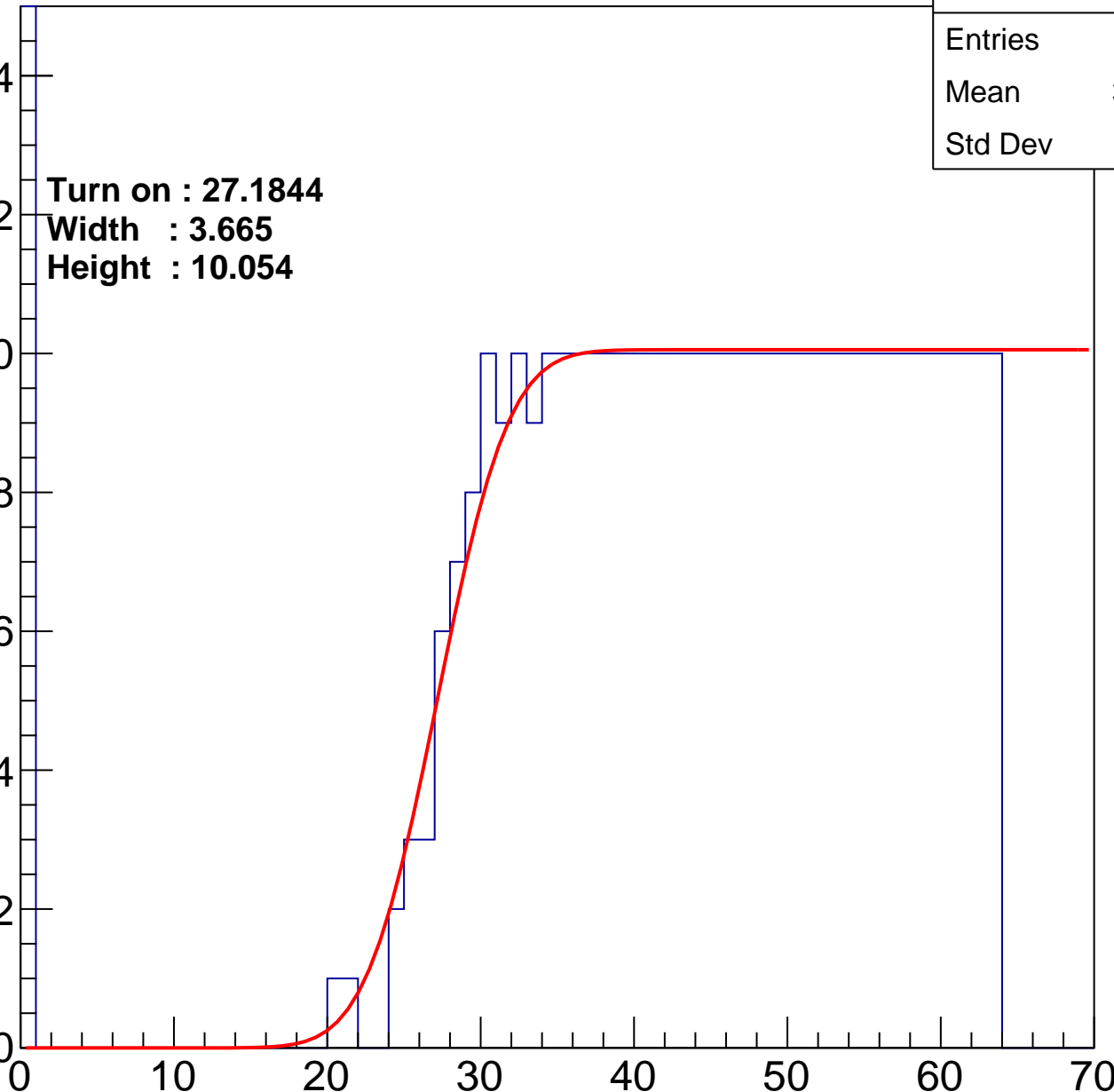
Width : 3.665

Height : 10.054

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch36

calib_packv5_041523_1651.root, FC#0, port C2

Entries	450
Mean	38
Std Dev	18.39

Turn on : 24.8658

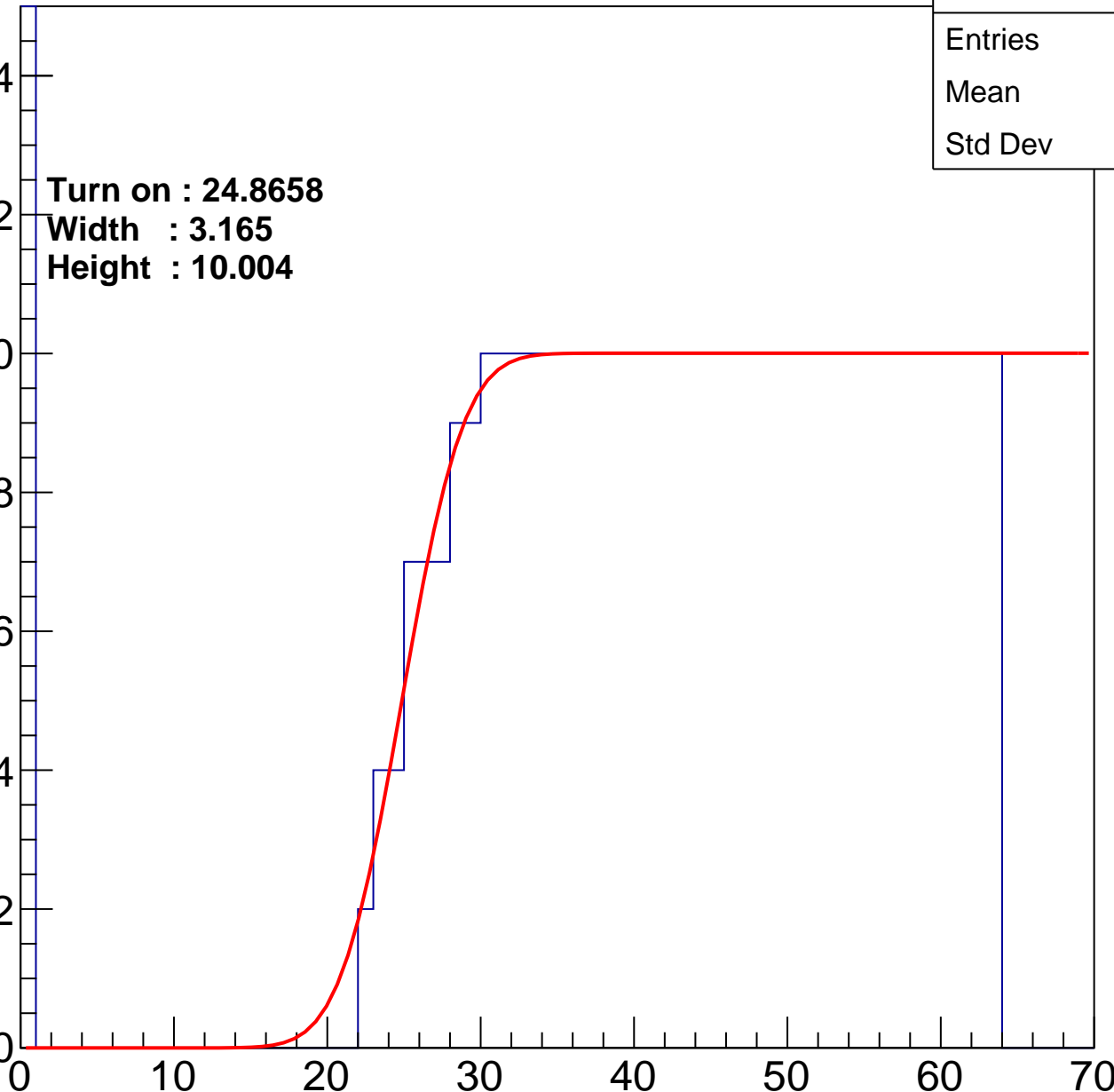
Width : 3.165

Height : 10.004

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch37

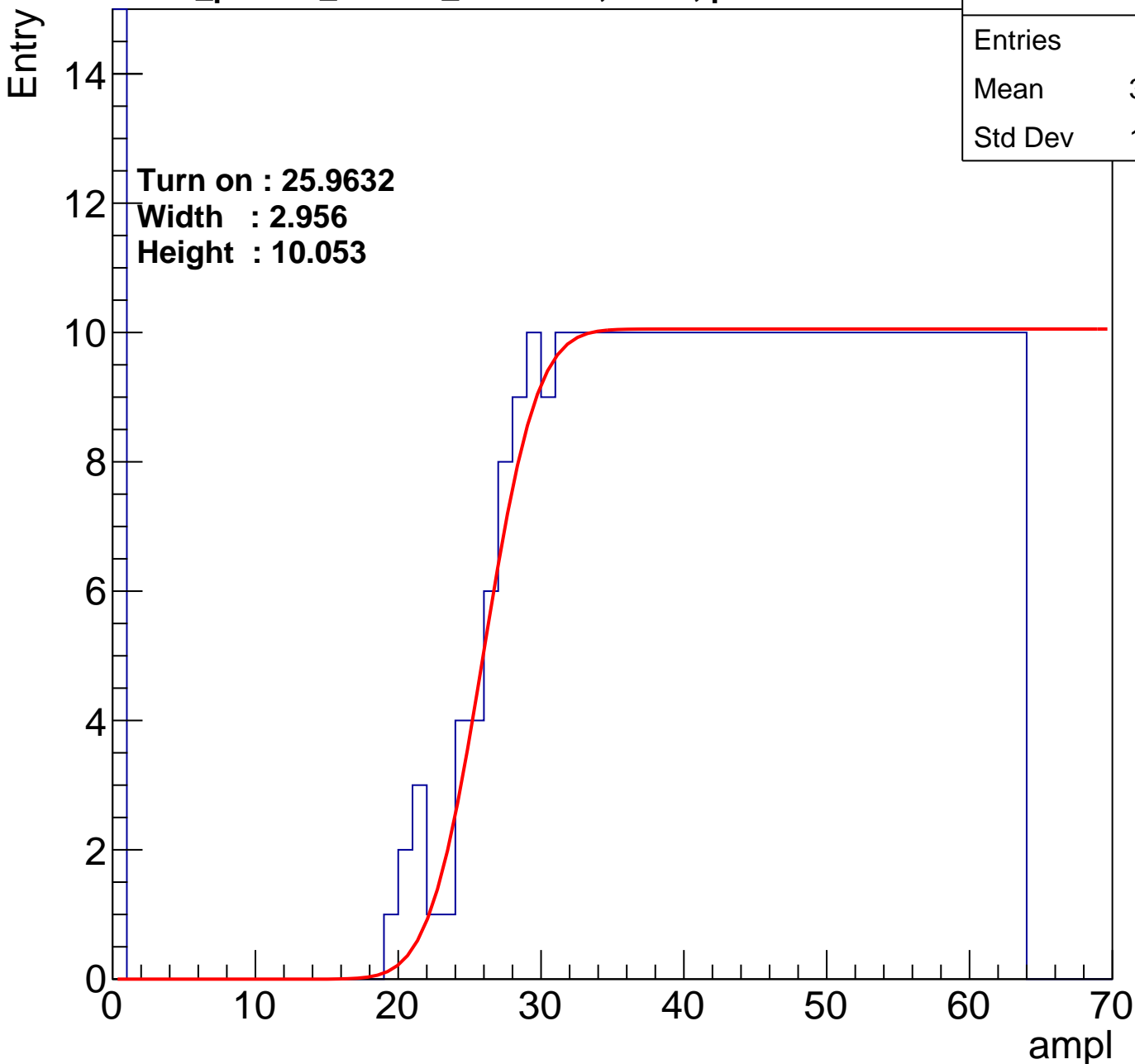
calib_packv5_041523_1651.root, FC#0, port C2

Entries	438
Mean	38.94
Std Dev	17.65

Turn on : 25.9632

Width : 2.956

Height : 10.053



B1L103S, U23-ch38

calib_packv5_041523_1651.root, FC#0, port C2

Entries	420
Mean	40.23
Std Dev	16.69

Turn on : 26.3560

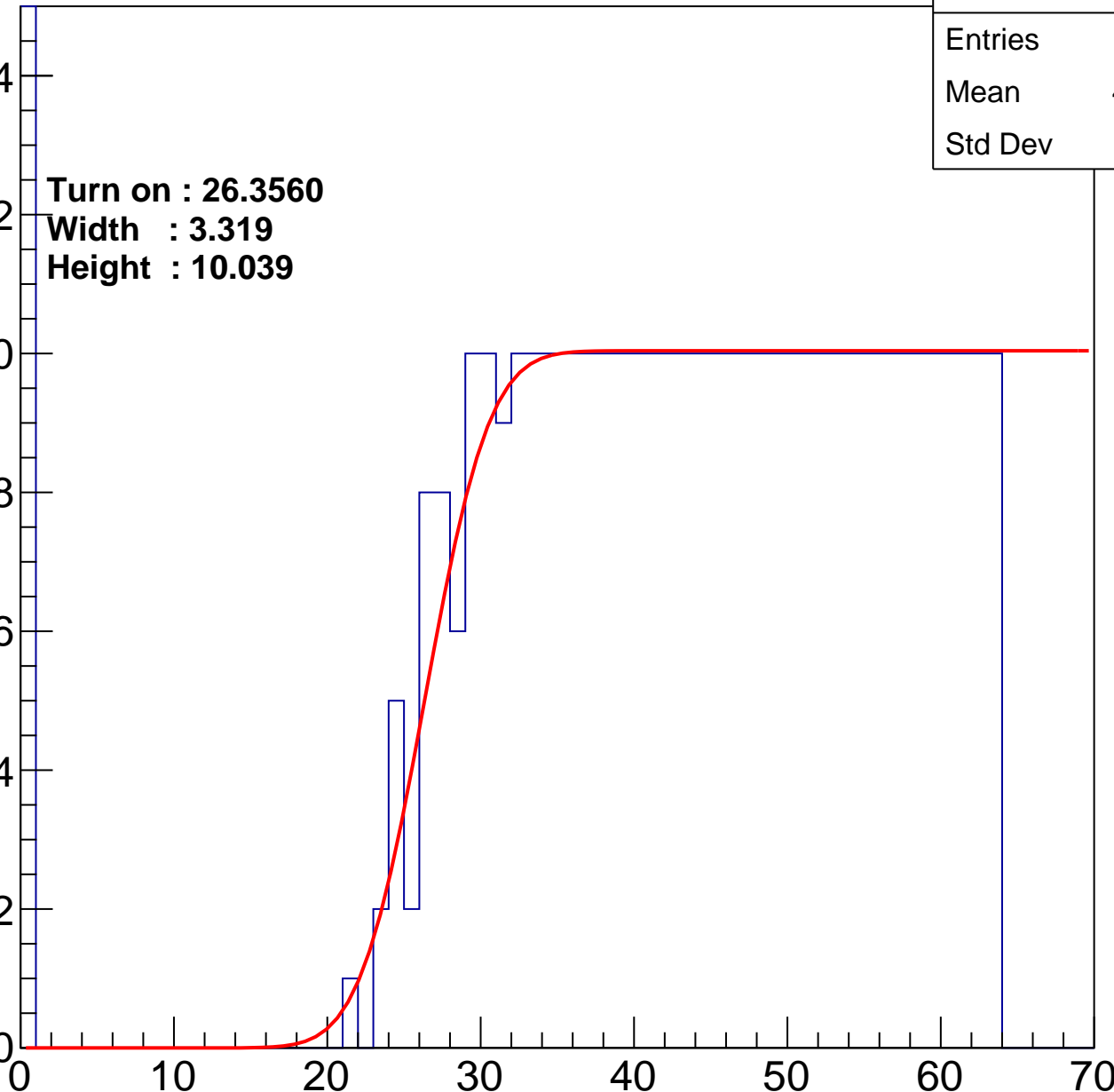
Width : 3.319

Height : 10.039

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch39

calib_packv5_041523_1651.root, FC#0, port C2

Entries	446
Mean	38.75
Std Dev	17.5

Turn on : 24.5518

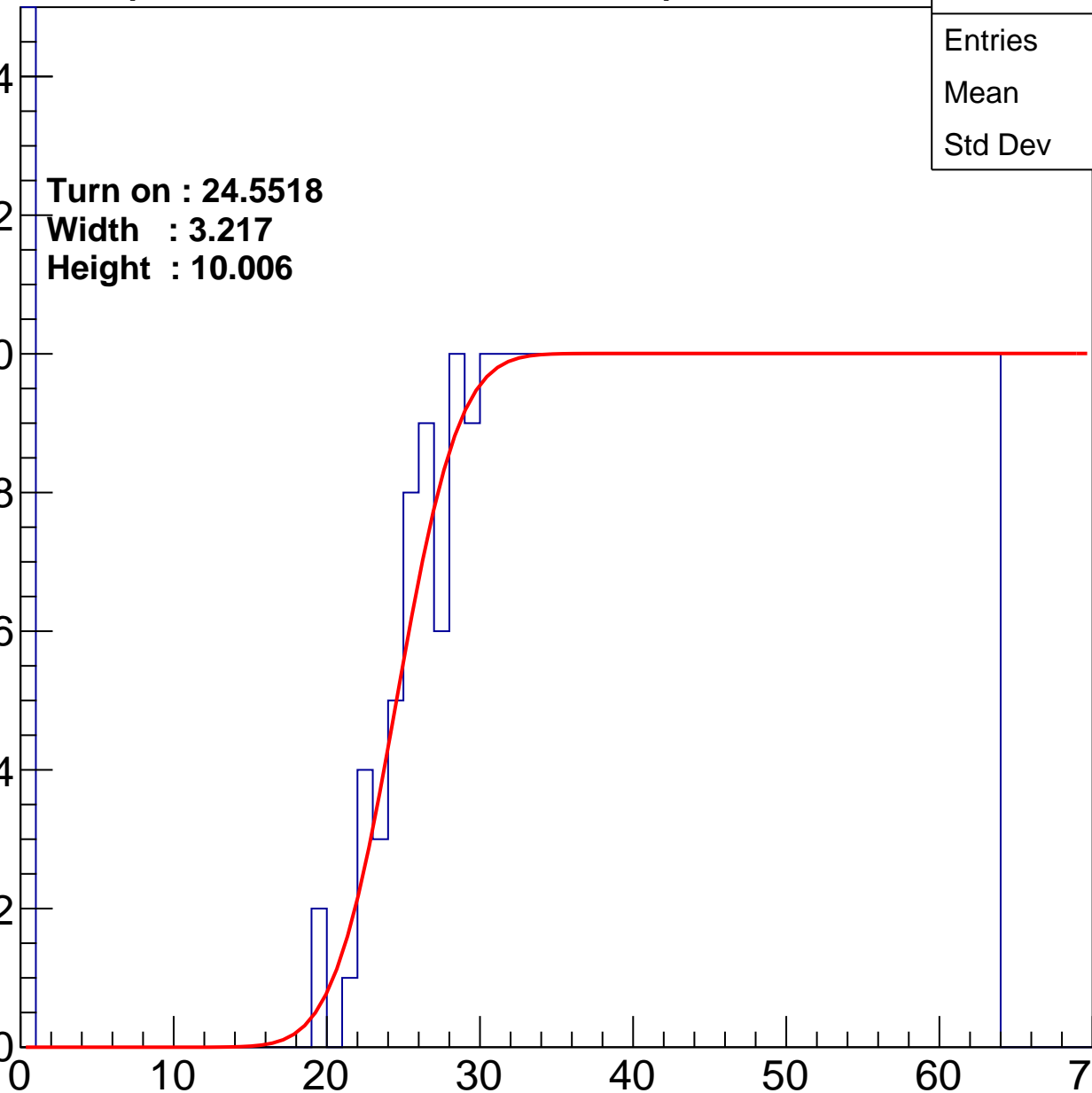
Width : 3.217

Height : 10.006

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch40

calib_packv5_041523_1651.root, FC#0, port C2

Entries	440
Mean	39.11
Std Dev	17.51

Turn on : 25.3829

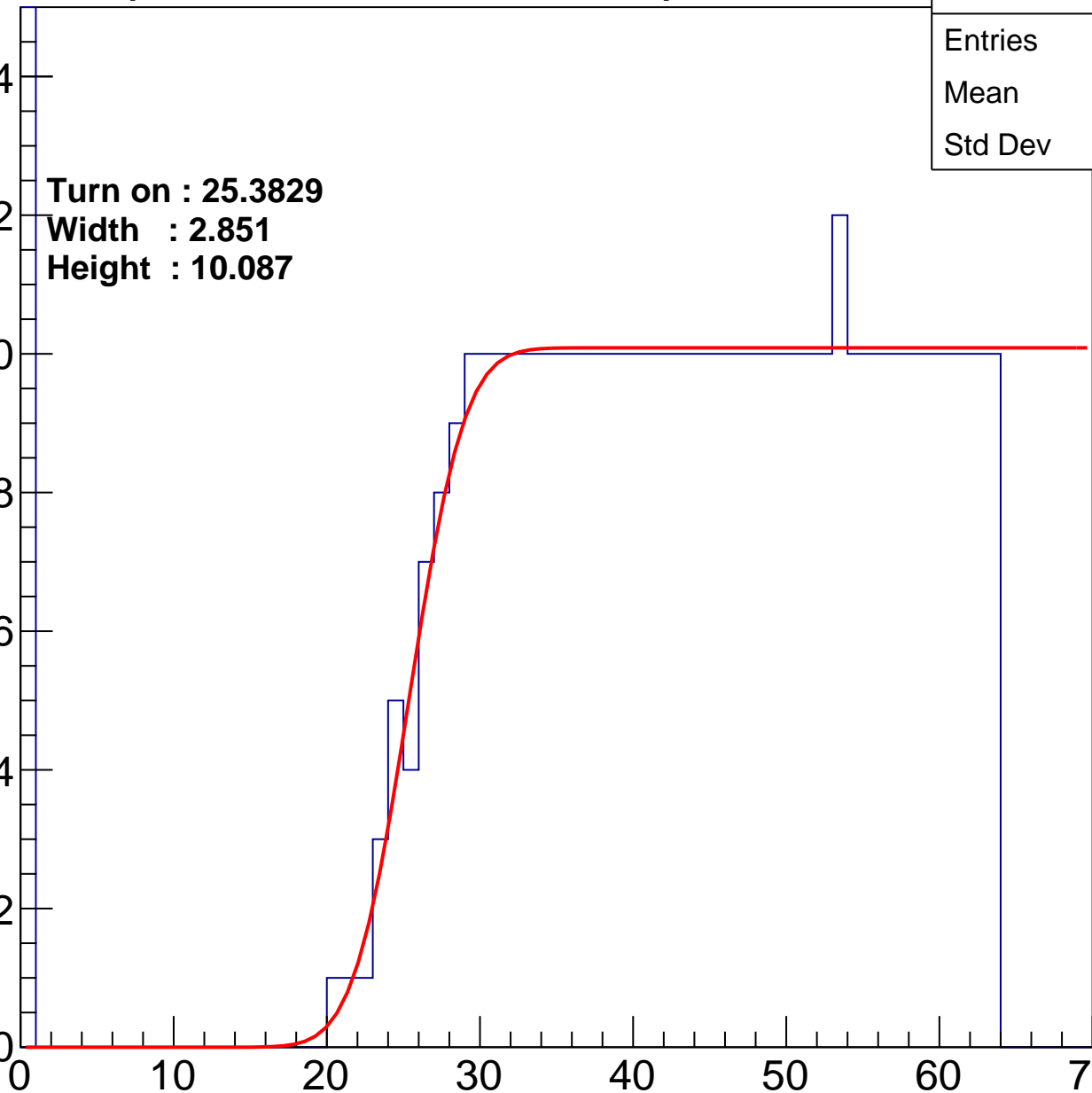
Width : 2.851

Height : 10.087

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch41

calib_packv5_041523_1651.root, FC#0, port C2

Entries	418
Mean	40.16
Std Dev	16.97

Turn on : 26.6350

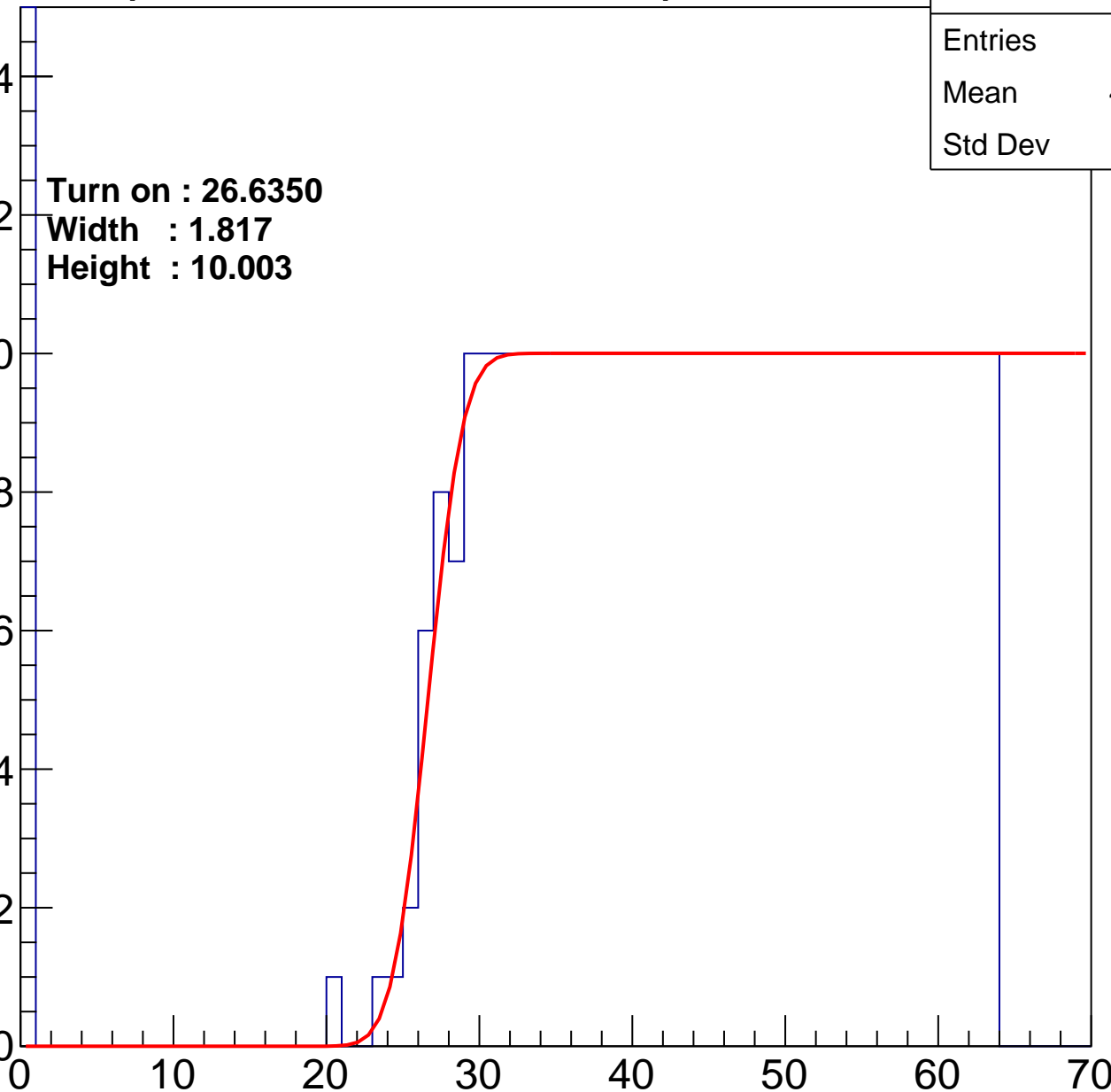
Width : 1.817

Height : 10.003

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch42

calib_packv5_041523_1651.root, FC#0, port C2

Entries	466
Mean	37.04
Std Dev	18.9

Turn on : 24.4674

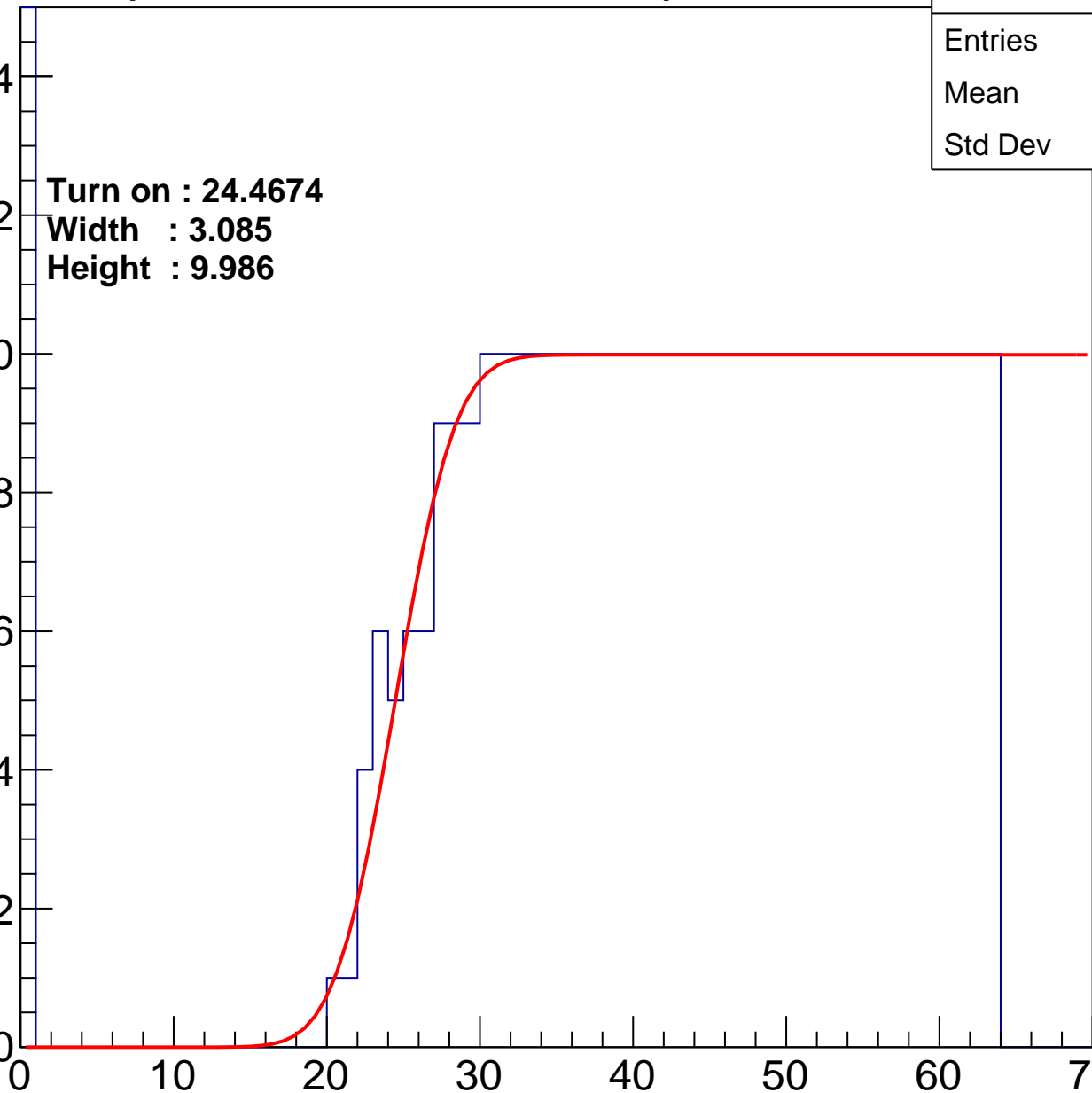
Width : 3.085

Height : 9.986

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch43

calib_packv5_041523_1651.root, FC#0, port C2

Entries	446
Mean	38.63
Std Dev	17.71

Turn on : 24.3038

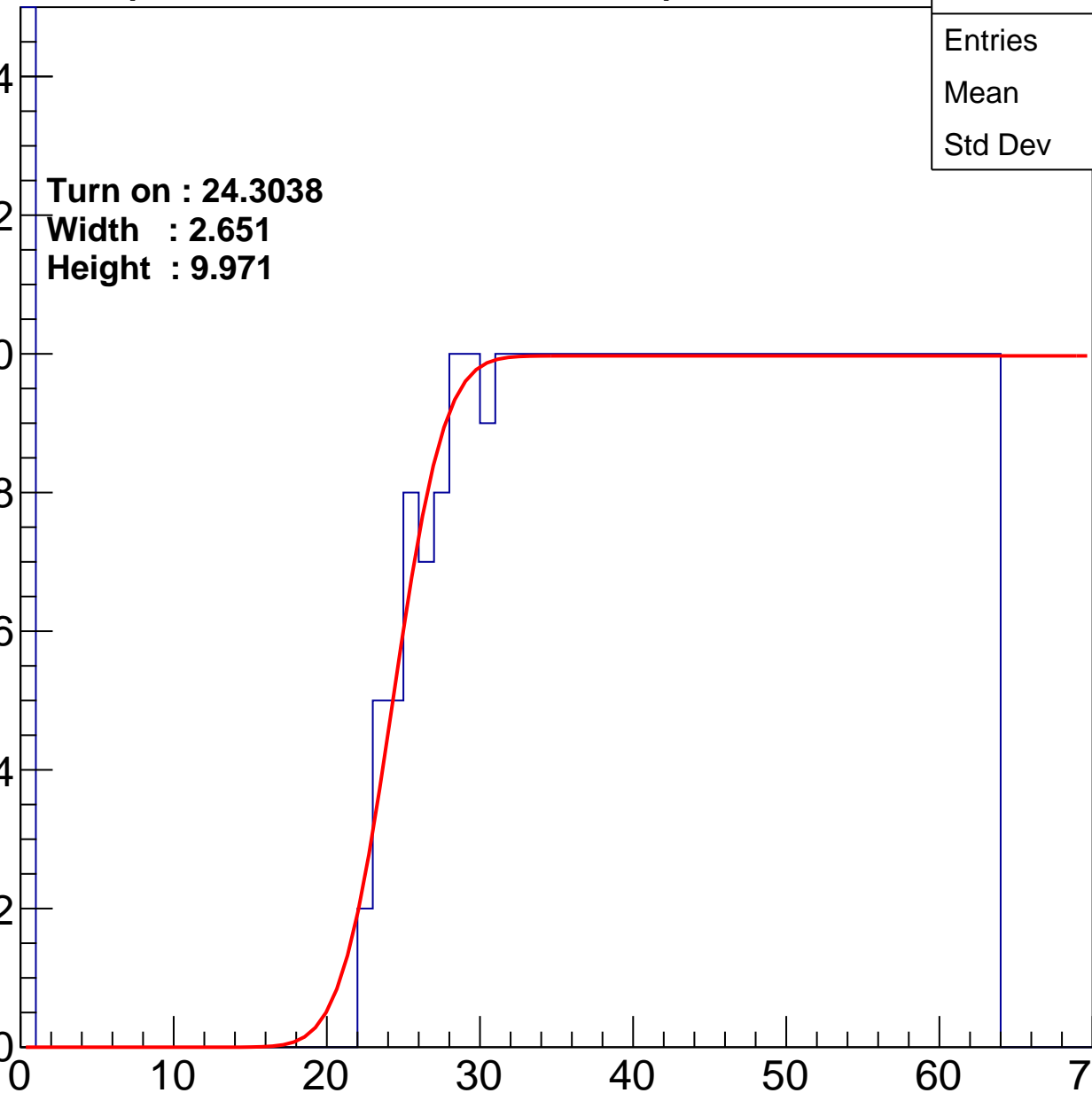
Width : 2.651

Height : 9.971

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch44

calib_packv5_041523_1651.root, FC#0, port C2

Entries	440
Mean	38.45
Std Dev	18.27

Turn on : 25.8447

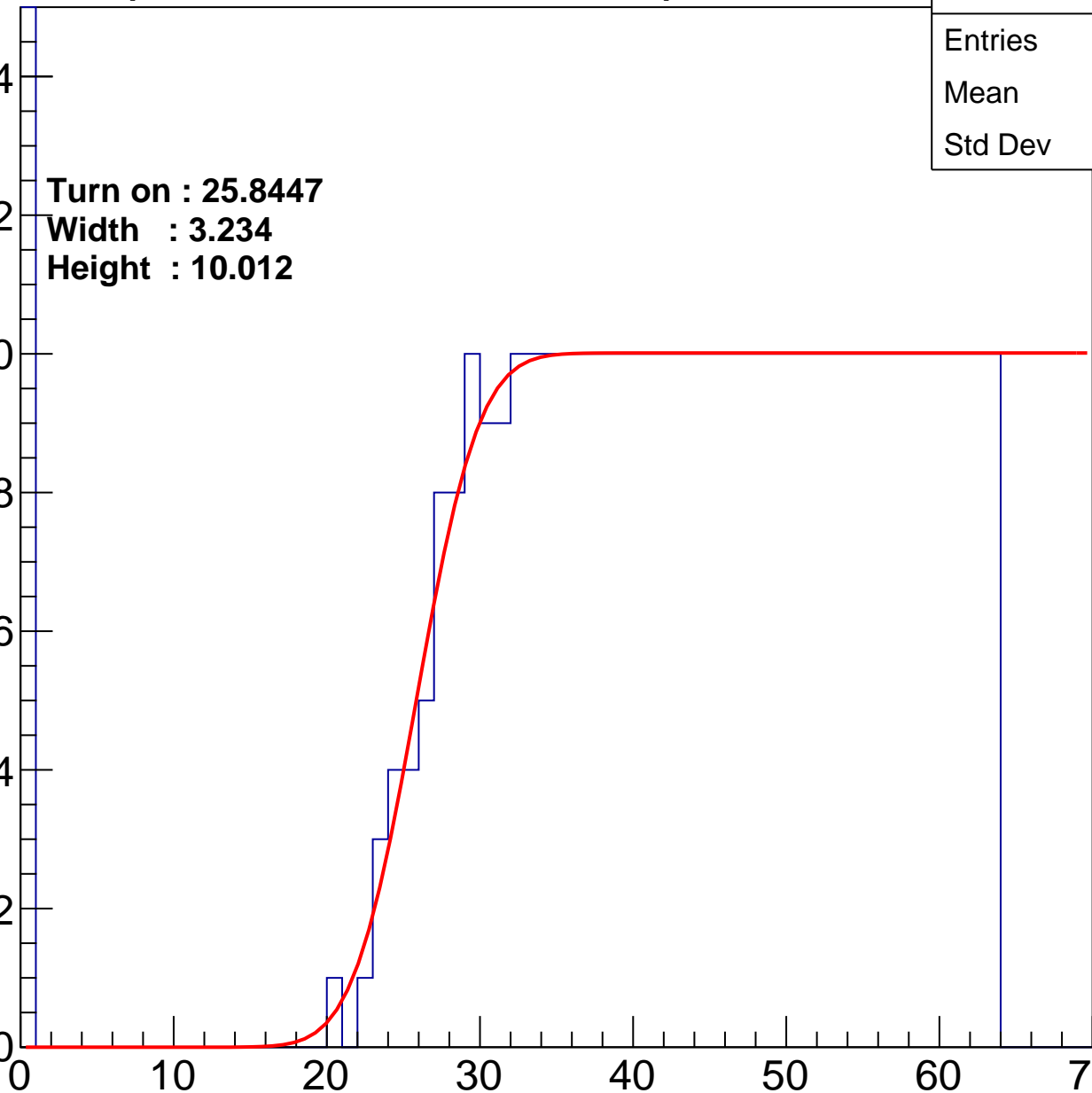
Width : 3.234

Height : 10.012

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch45

calib_packv5_041523_1651.root, FC#0, port C2

Entries	420
Mean	39.41
Std Dev	17.95

Turn on : 27.6398

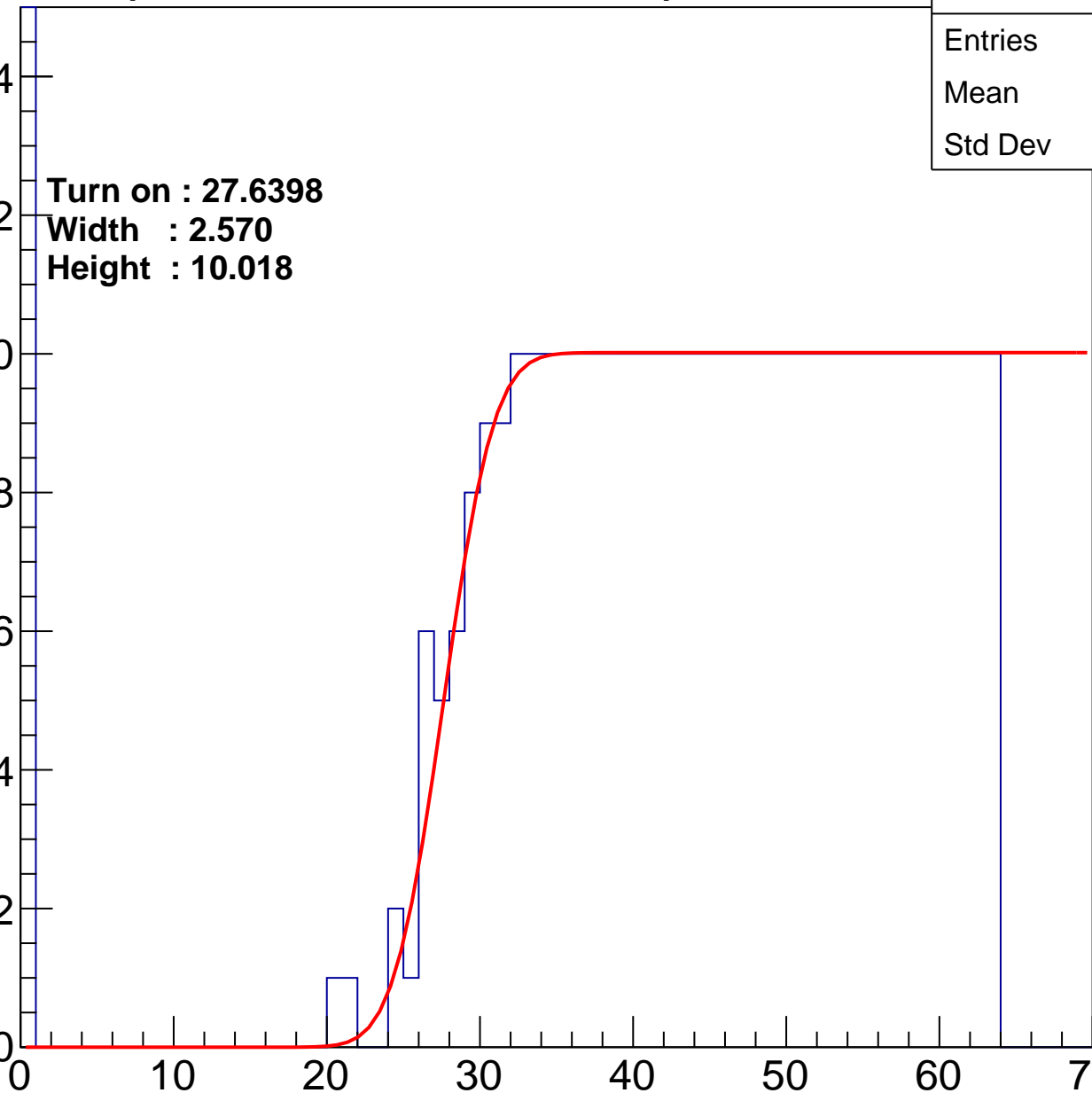
Width : 2.570

Height : 10.018

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch46

calib_packv5_041523_1651.root, FC#0, port C2

Entries	434
Mean	38.52
Std Dev	18.48

Turn on : 26.4330

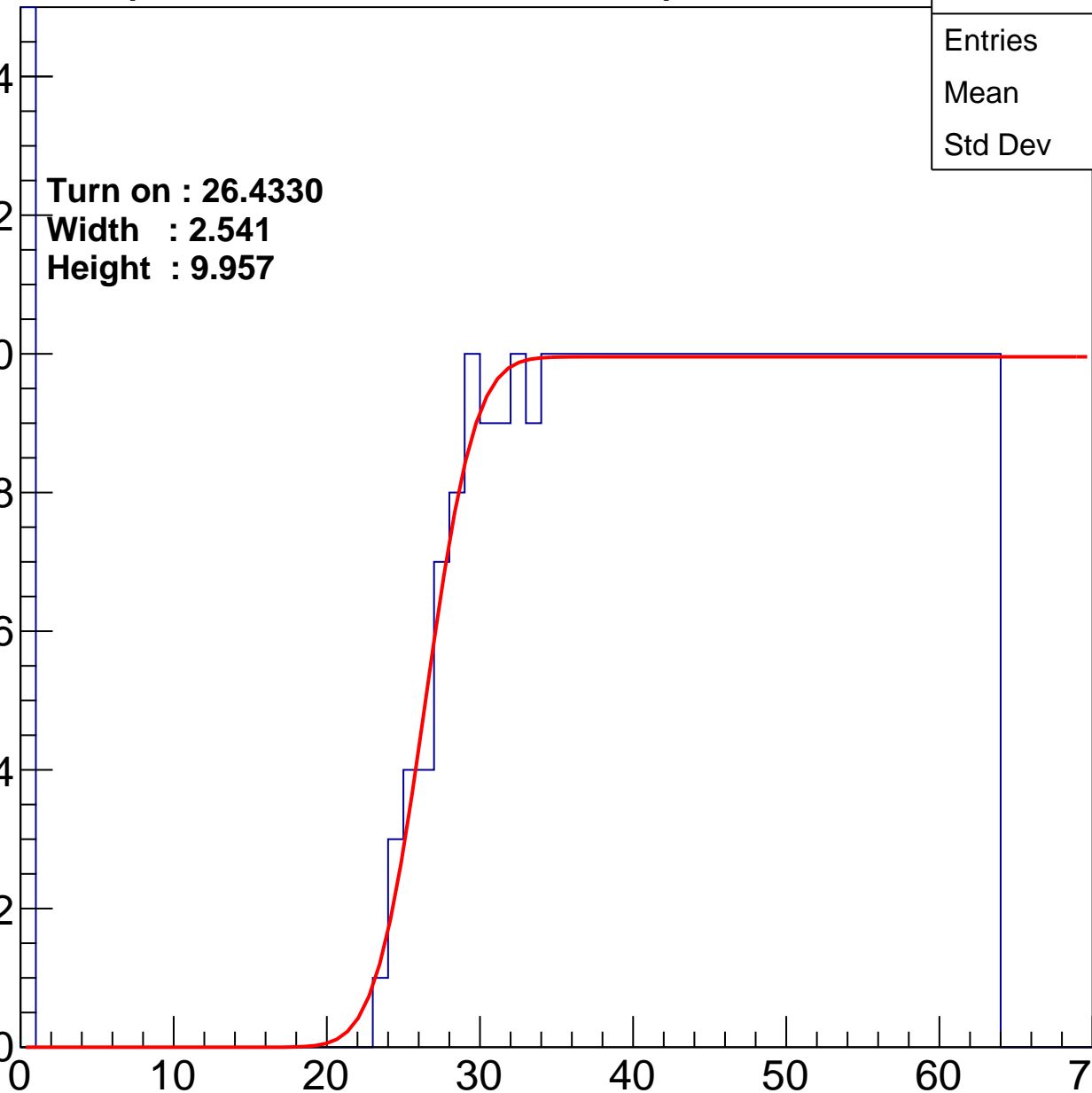
Width : 2.541

Height : 9.957

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch47

calib_packv5_041523_1651.root, FC#0, port C2

Entries	418
Mean	39.99
Std Dev	17.2

Turn on : 26.7227

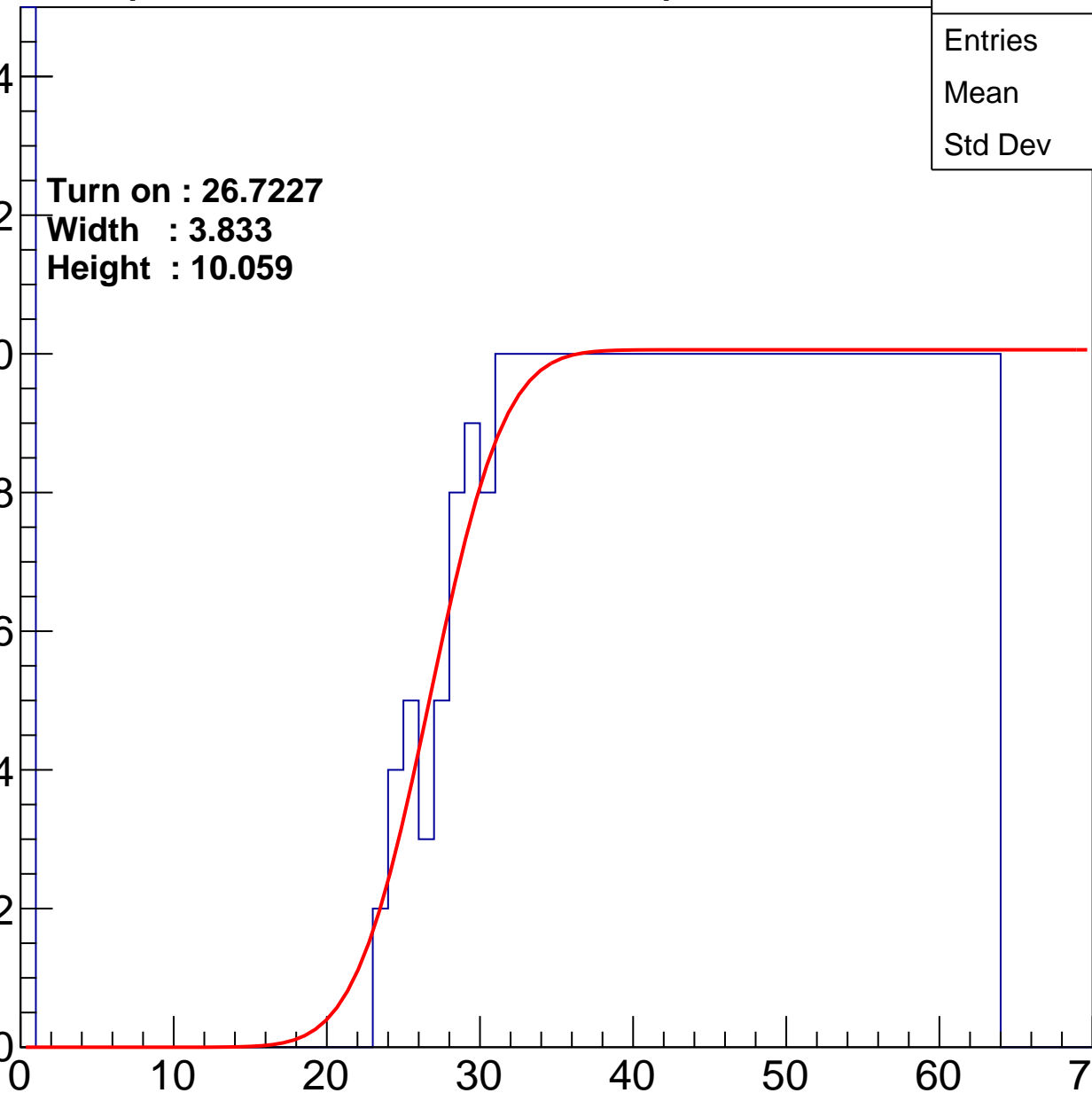
Width : 3.833

Height : 10.059

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch48

calib_packv5_041523_1651.root, FC#0, port C2

Entries	451
Mean	38.35
Std Dev	17.85

Turn on : 24.0171

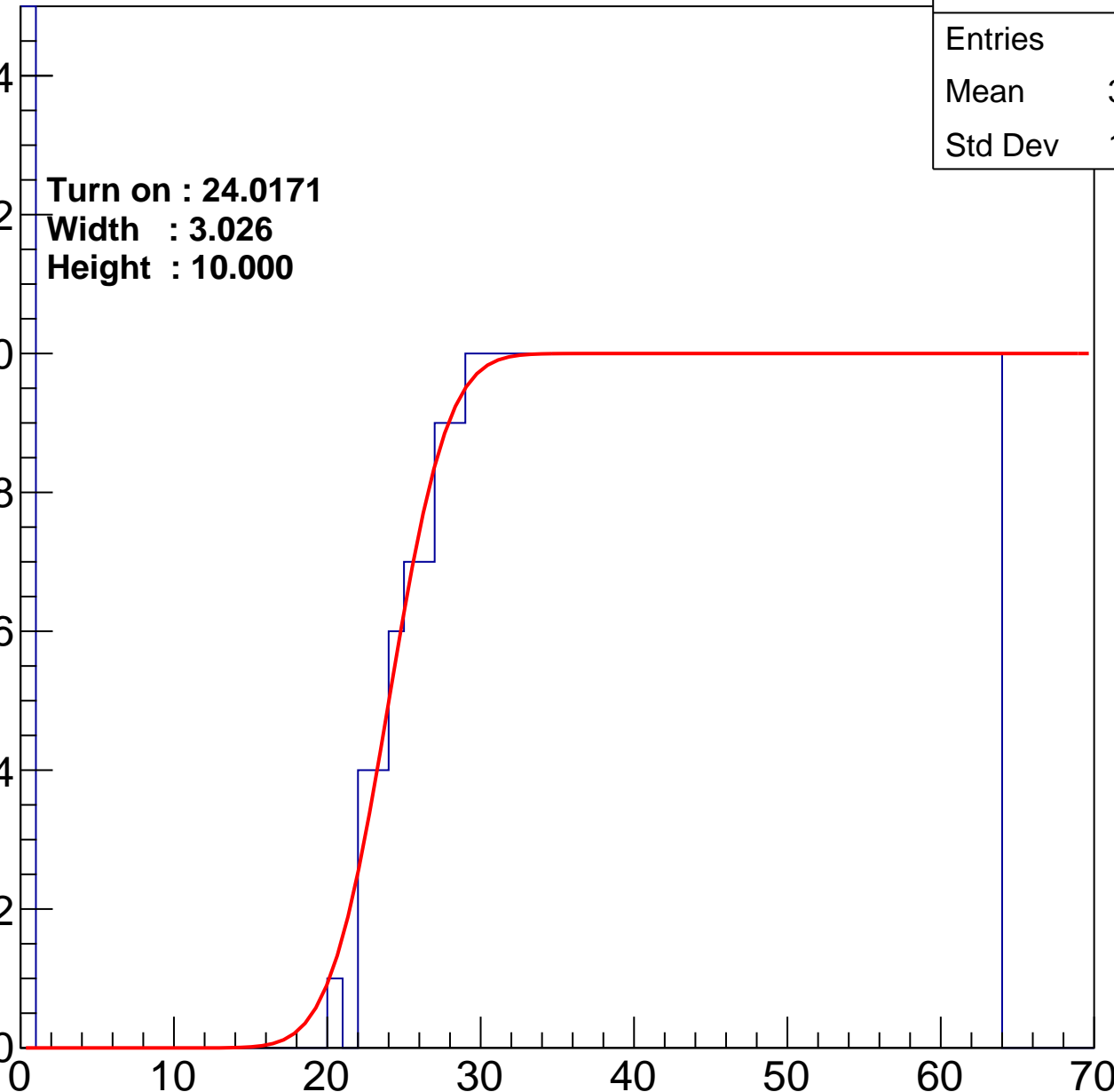
Width : 3.026

Height : 10.000

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch49

calib_packv5_041523_1651.root, FC#0, port C2

Entries	427
Mean	39.65
Std Dev	17.23

Turn on : 25.8686

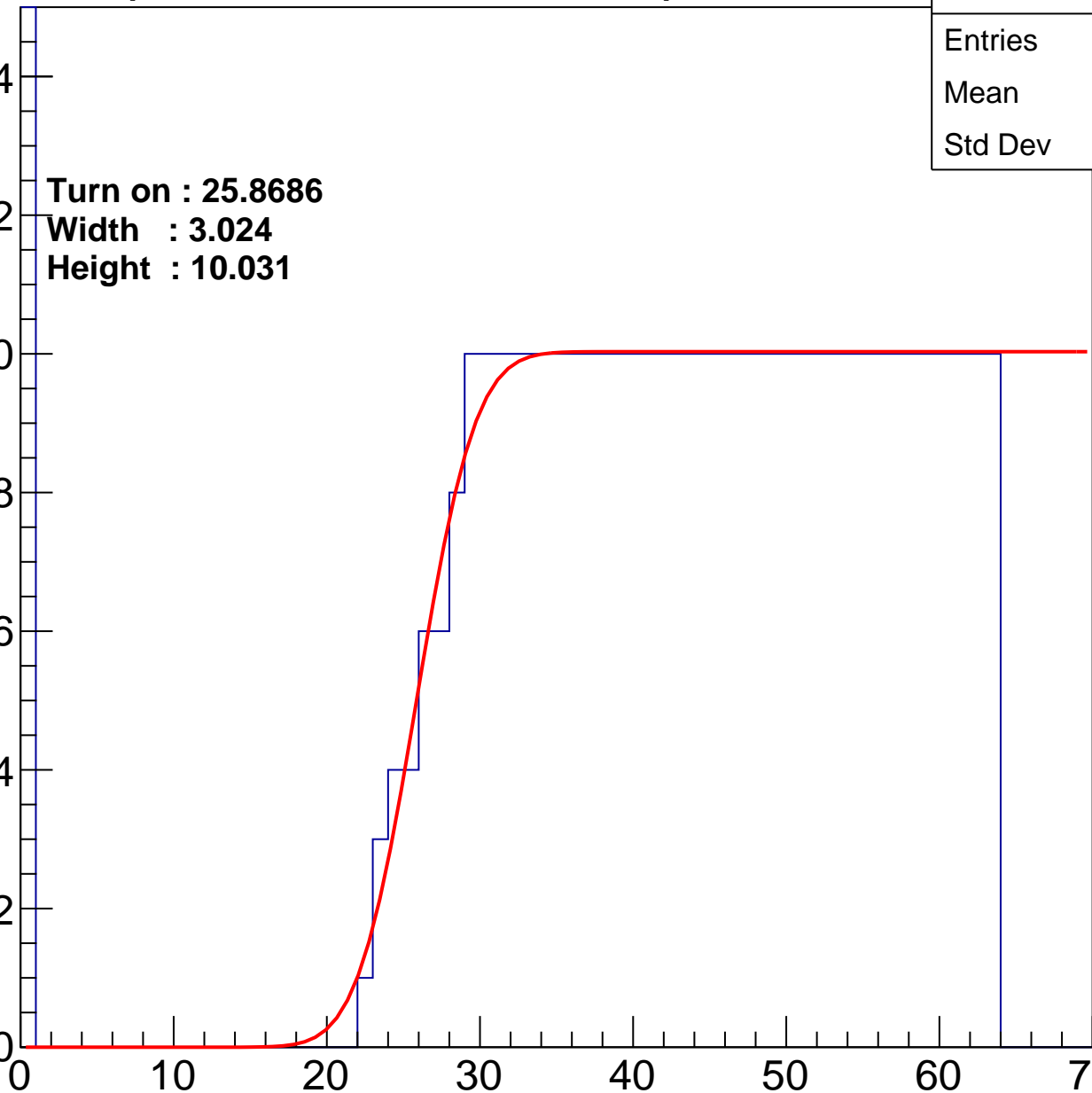
Width : 3.024

Height : 10.031

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch50

calib_packv5_041523_1651.root, FC#0, port C2

Entries	448
Mean	38.63
Std Dev	17.57

Turn on : 24.4821

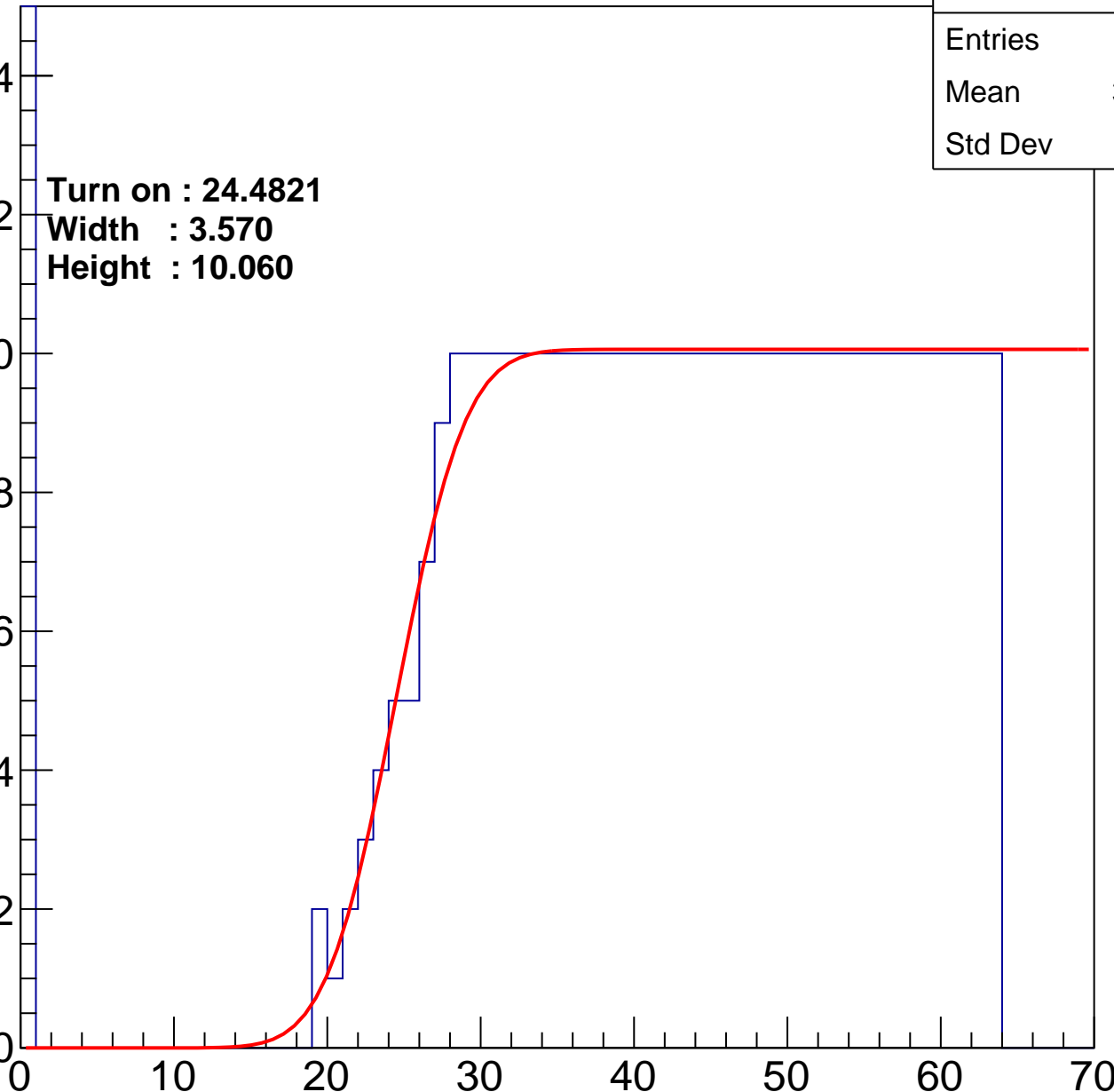
Width : 3.570

Height : 10.060

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch51

calib_packv5_041523_1651.root, FC#0, port C2

Entries	430
Mean	39.3
Std Dev	17.58

Turn on : 26.0701

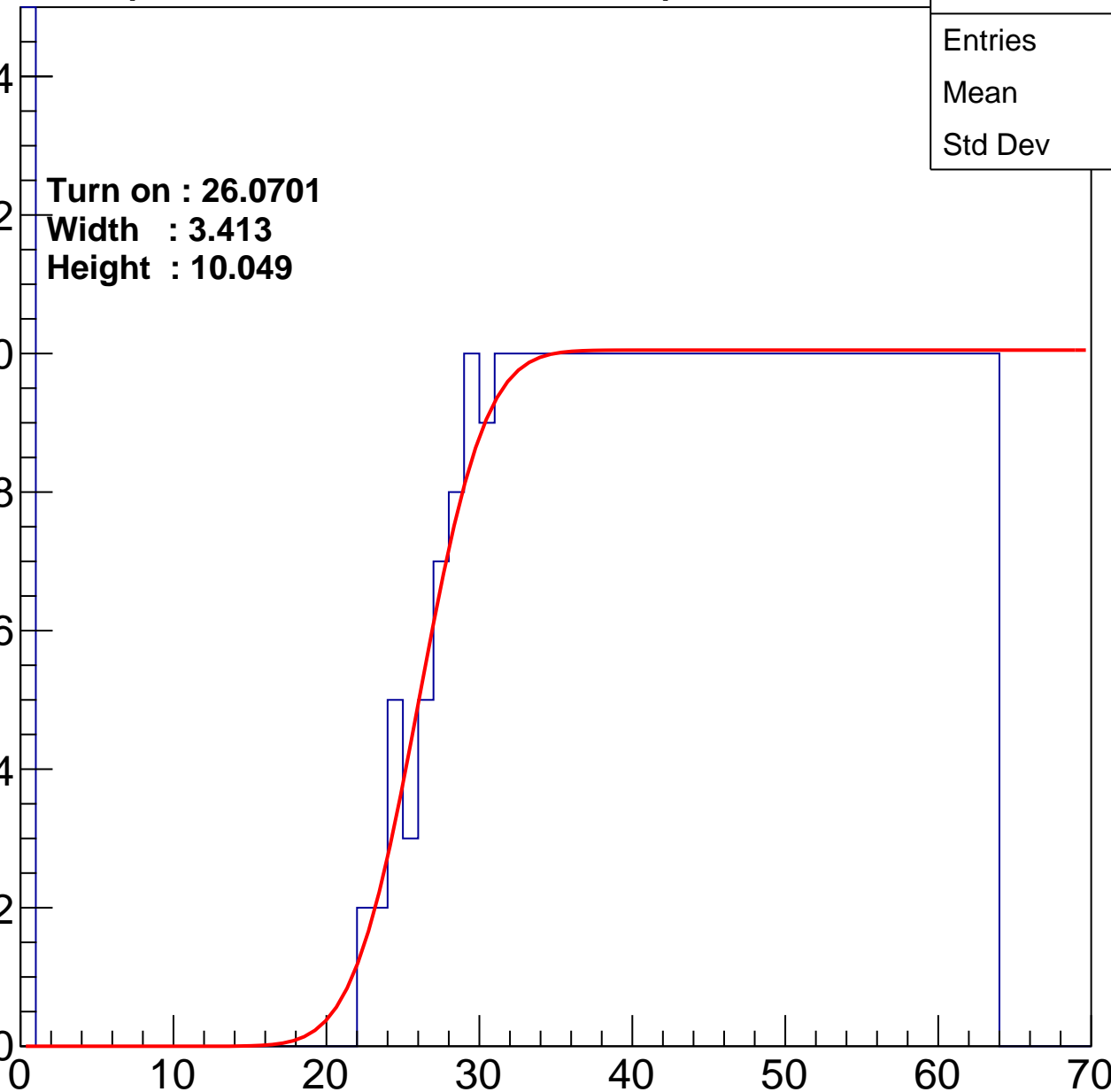
Width : 3.413

Height : 10.049

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch52

calib_packv5_041523_1651.root, FC#0, port C2

Entries	413
Mean	40.63
Std Dev	16.45

Turn on : 26.3375

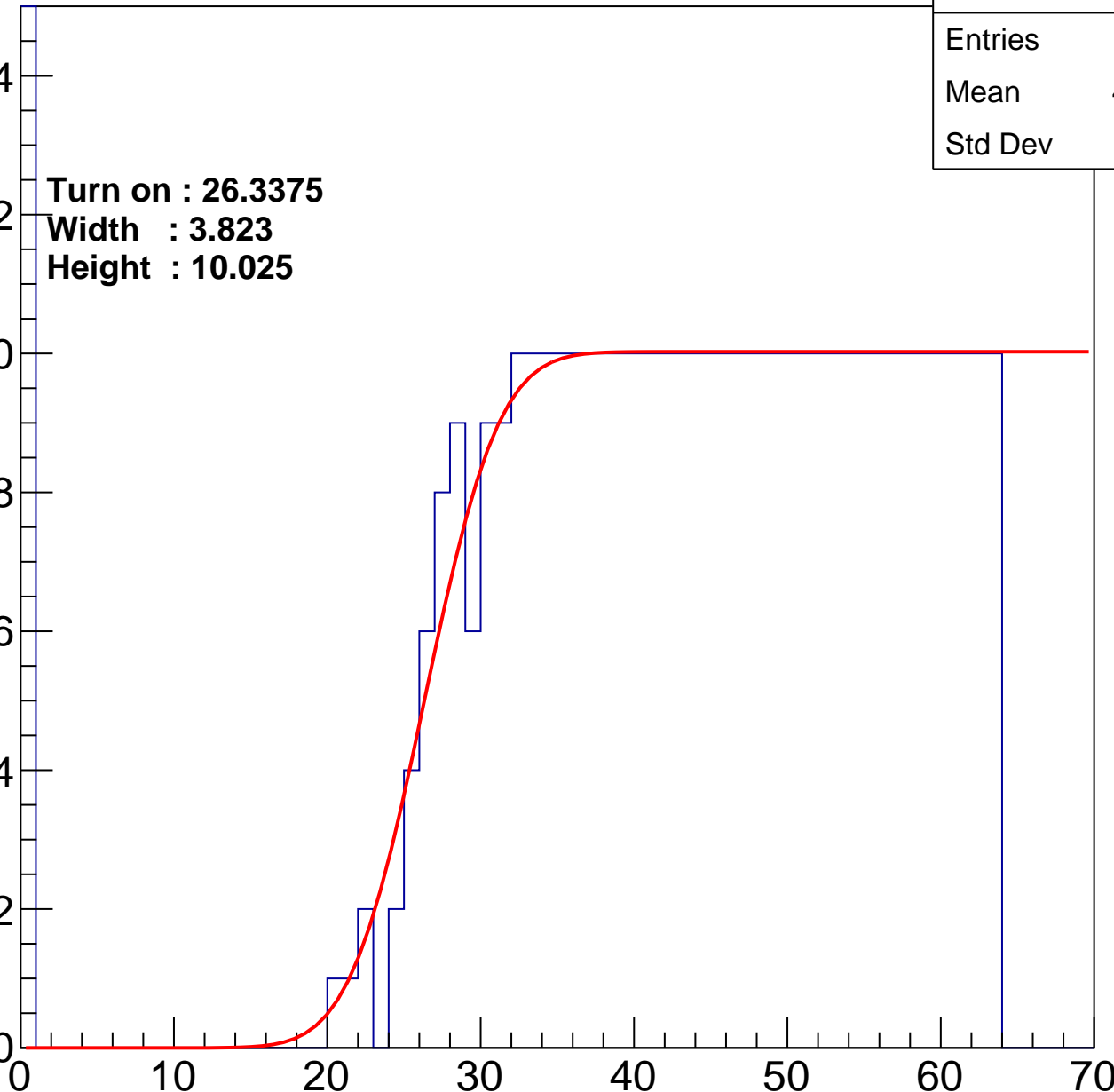
Width : 3.823

Height : 10.025

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch53

calib_packv5_041523_1651.root, FC#0, port C2

Entries	440
Mean	38.98
Std Dev	17.5

Turn on : 25.0598

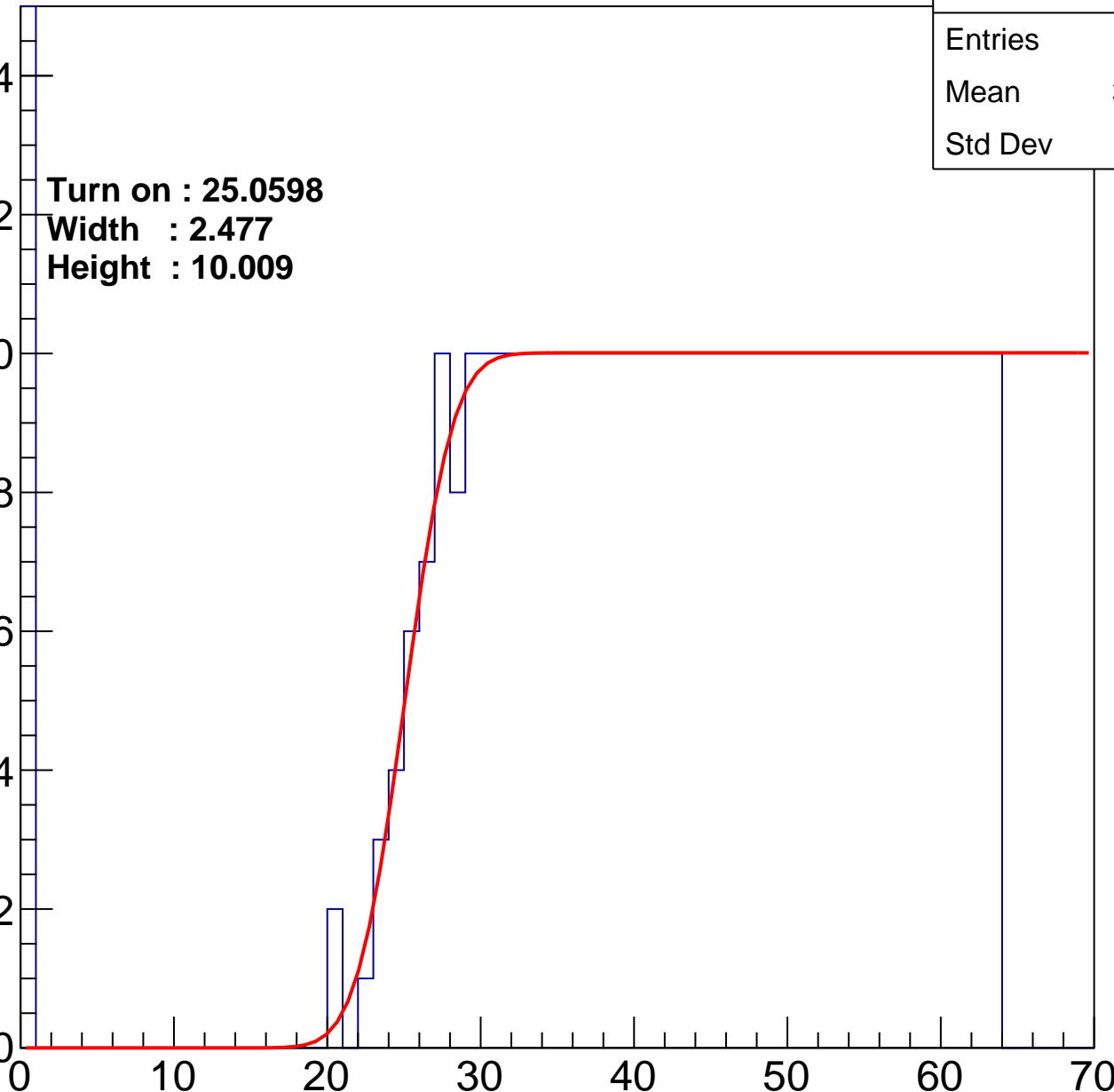
Width : 2.477

Height : 10.009

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch54

calib_packv5_041523_1651.root, FC#0, port C2

Entries	449
Mean	38.1
Std Dev	18.32

Turn on : 24.9887

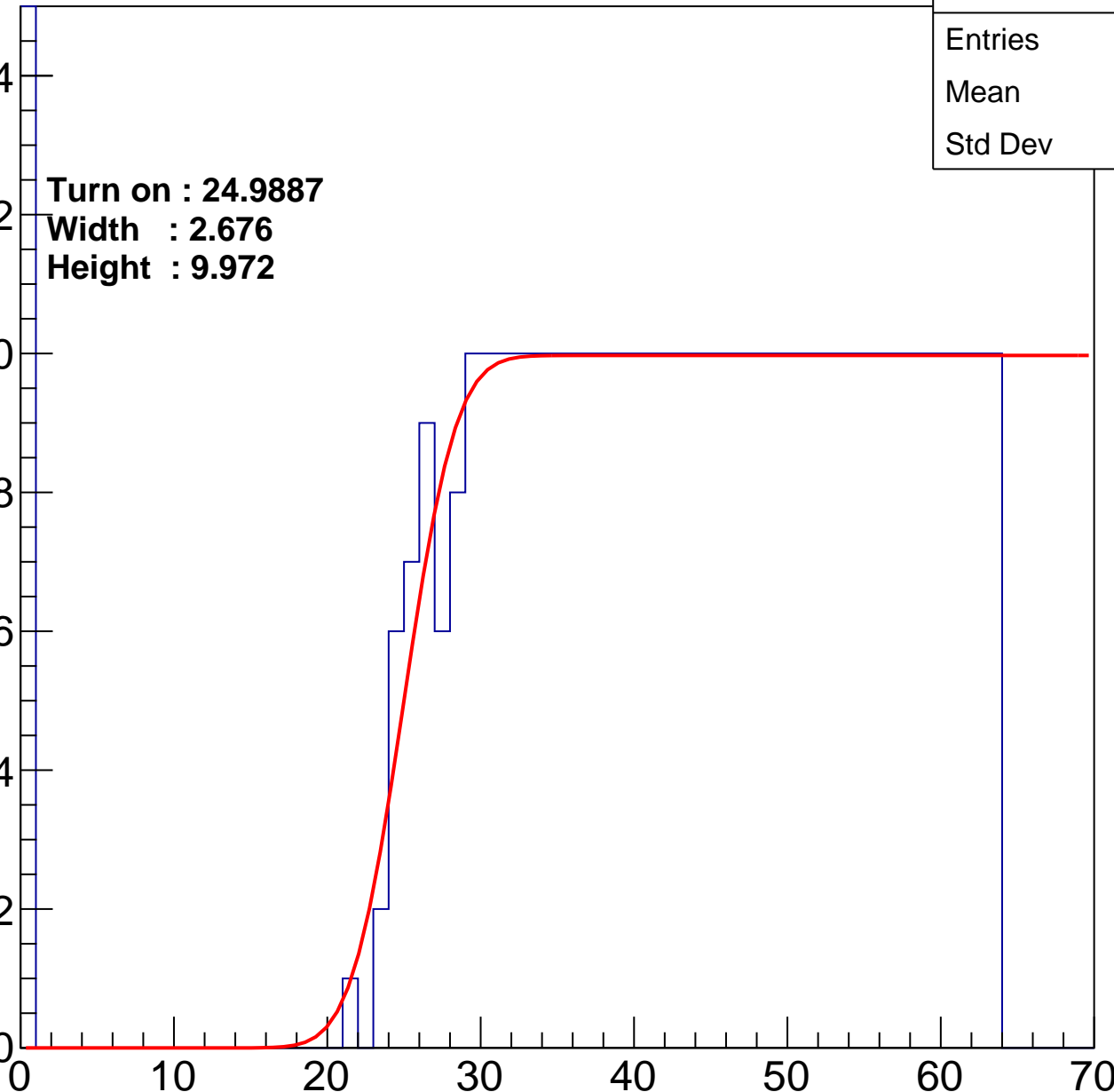
Width : 2.676

Height : 9.972

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch55

calib_packv5_041523_1651.root, FC#0, port C2

Entries	424
Mean	38.92
Std Dev	18.43

Turn on : 27.5248

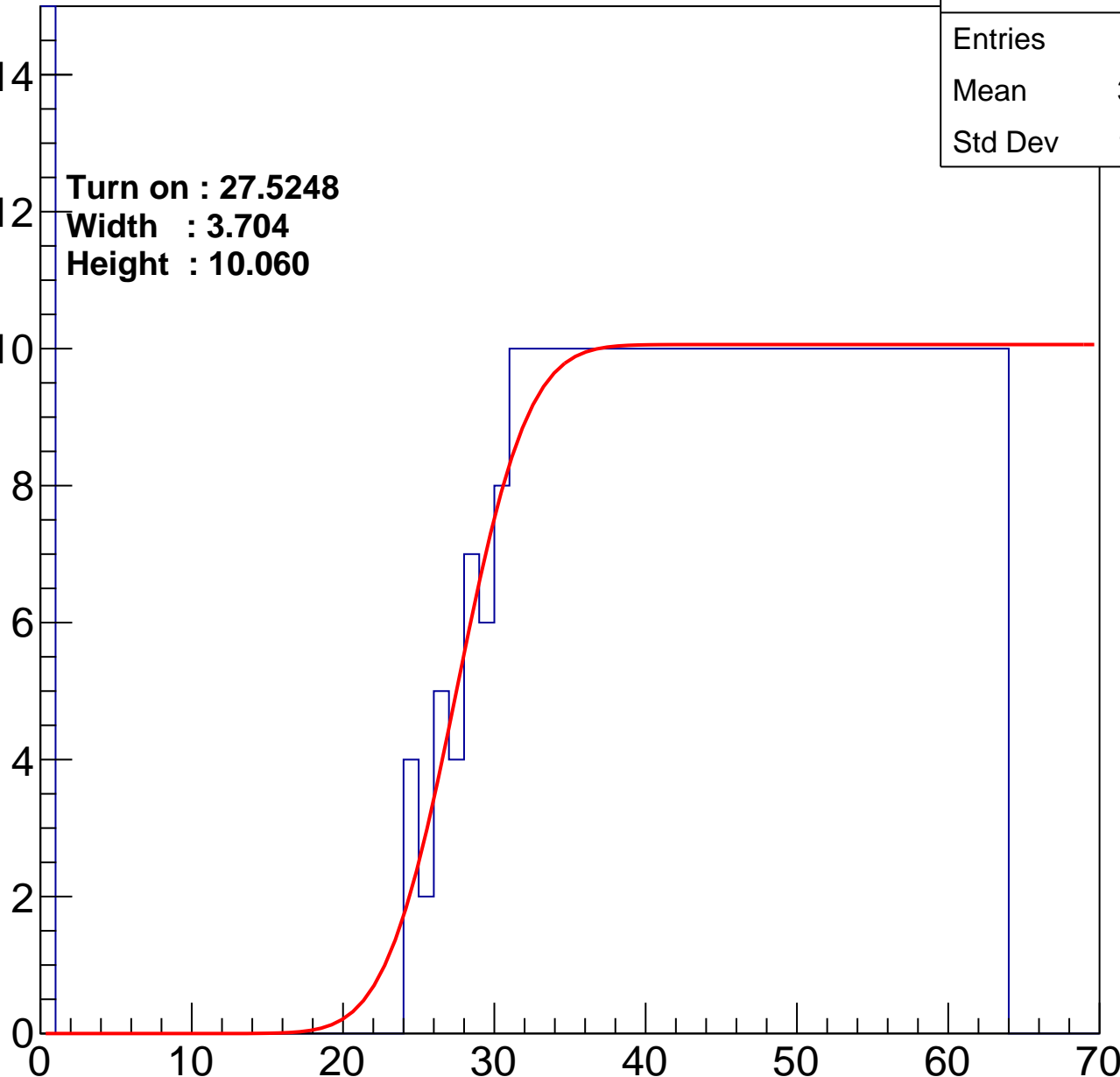
Width : 3.704

Height : 10.060

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch56

calib_packv5_041523_1651.root, FC#0, port C2

Entries	471
Mean	37.3
Std Dev	18.31

Turn on : 23.3374

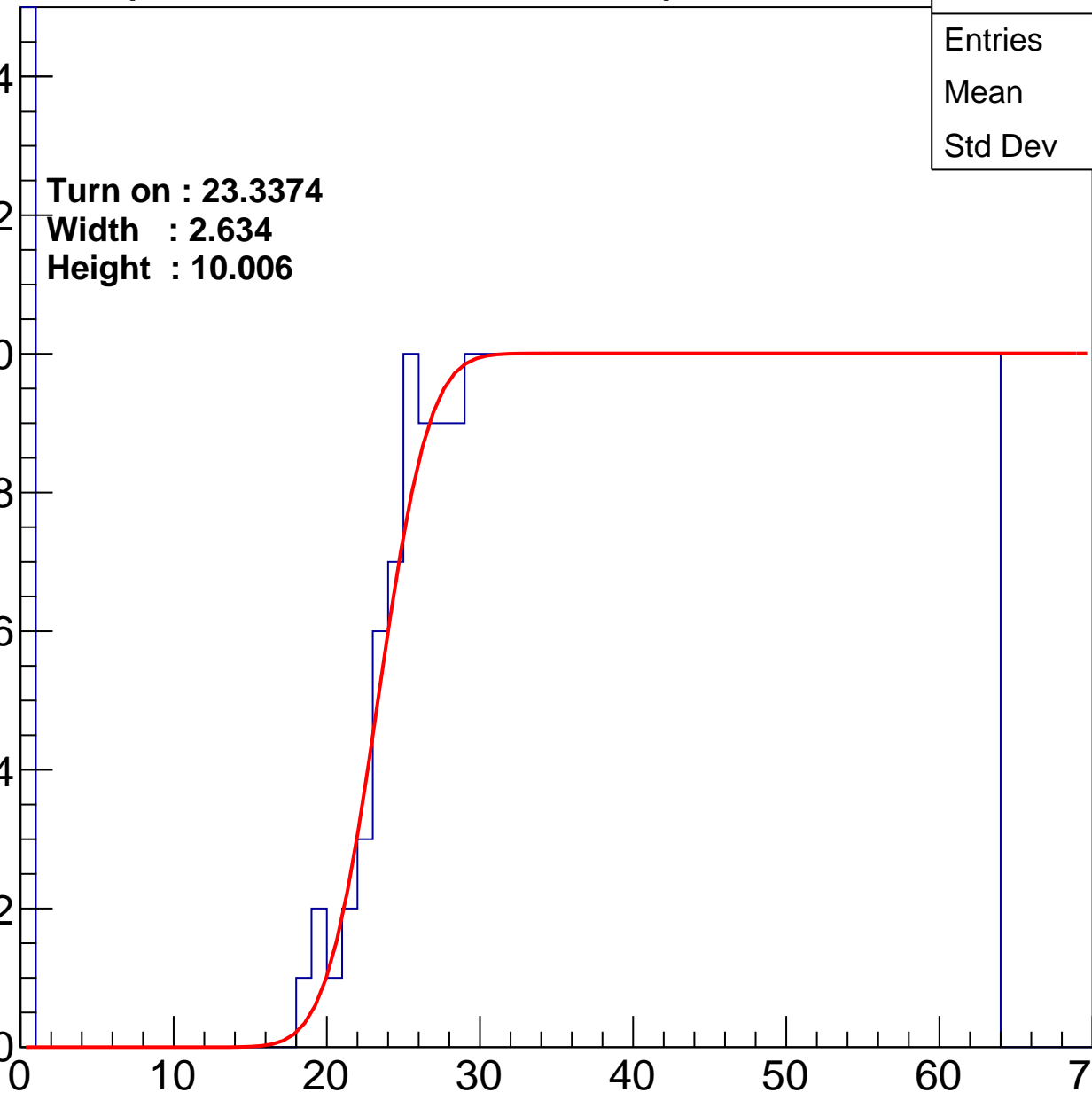
Width : 2.634

Height : 10.006

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch57

calib_packv5_041523_1651.root, FC#0, port C2

Entries	439
Mean	38.31
Std Dev	18.51

Turn on : 26.0818

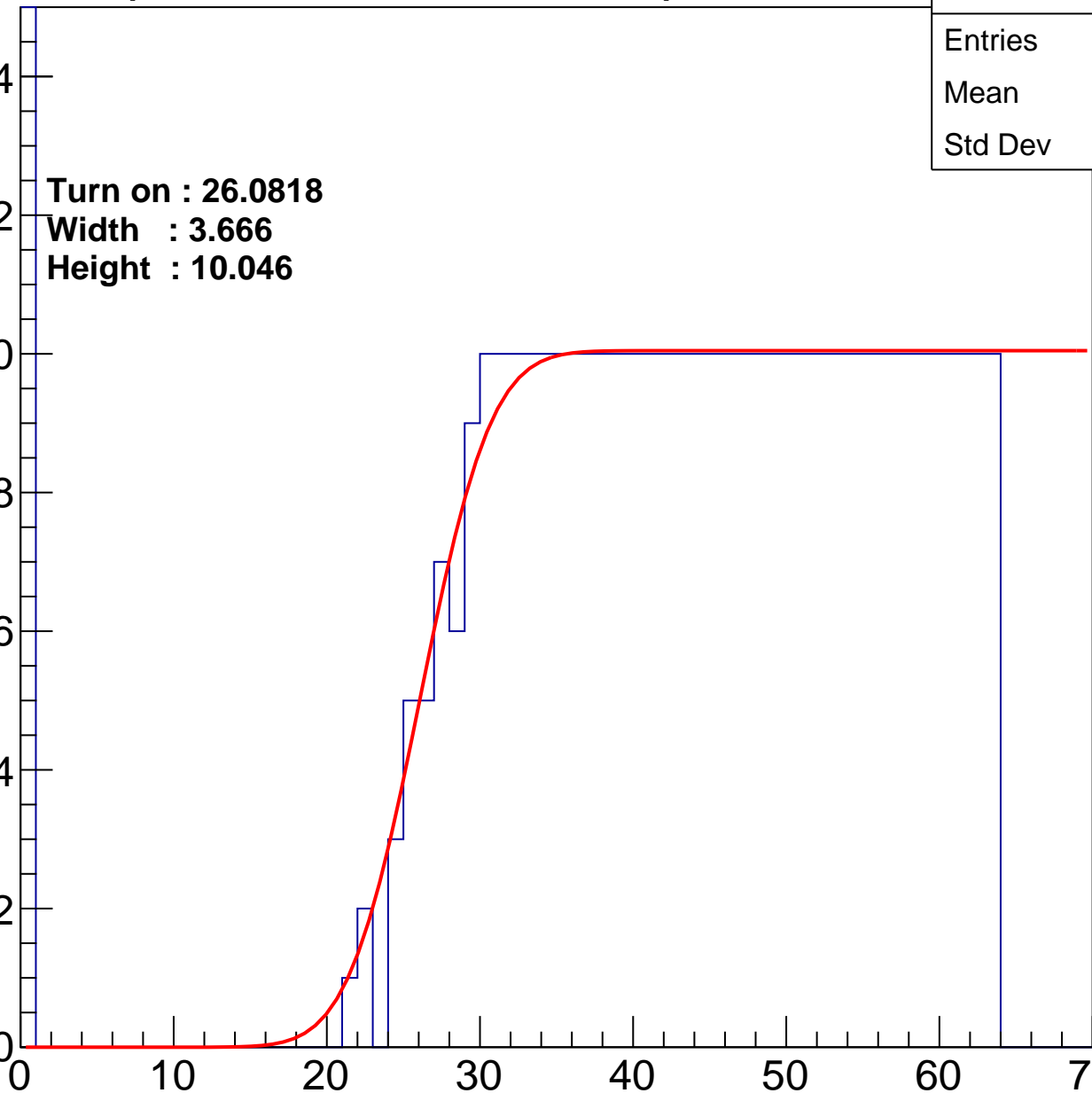
Width : 3.666

Height : 10.046

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch58

calib_packv5_041523_1651.root, FC#0, port C2

Entries	441
Mean	38.94
Std Dev	17.5

Turn on : 24.2435

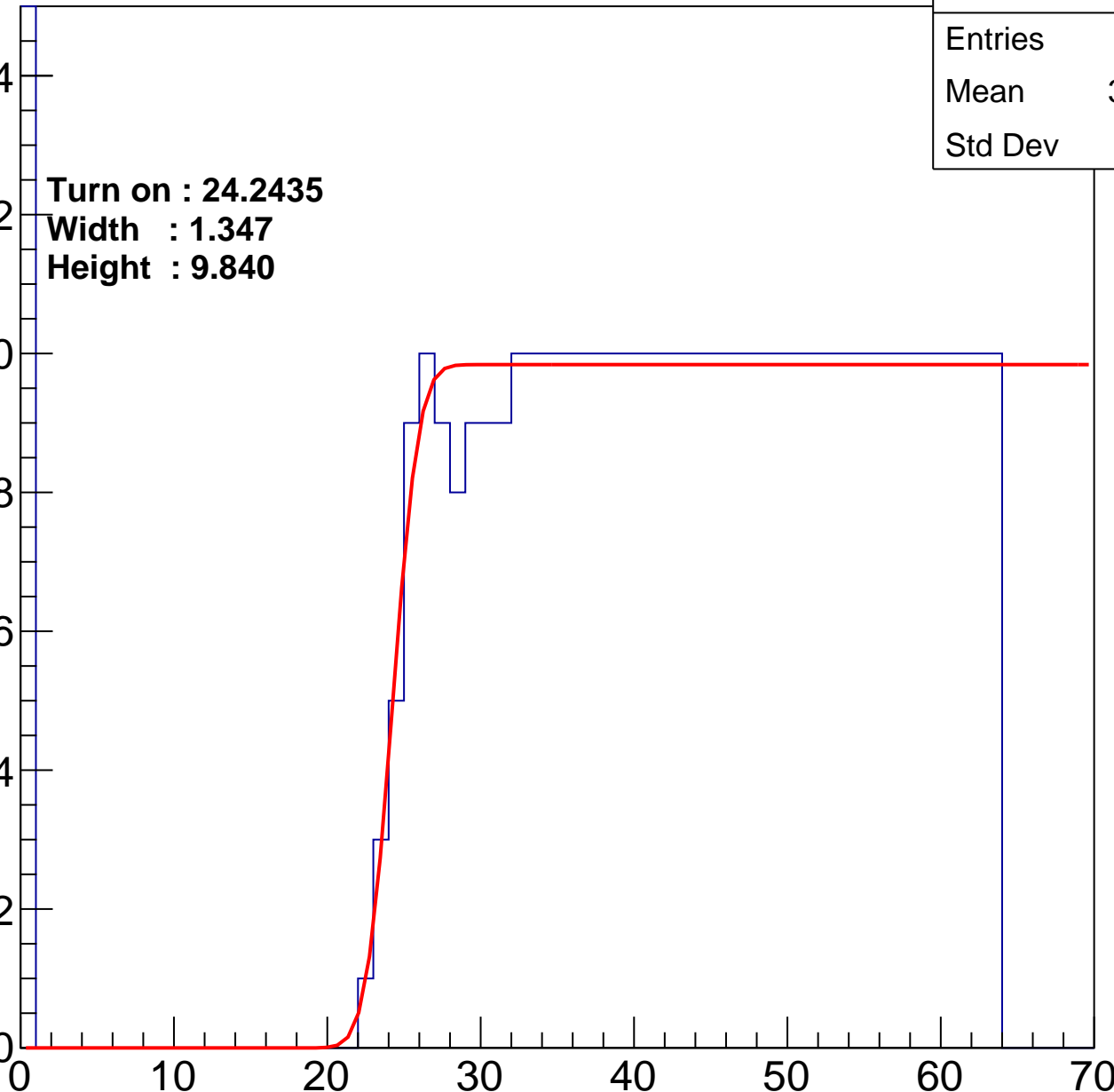
Width : 1.347

Height : 9.840

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch59

calib_packv5_041523_1651.root, FC#0, port C2

Entries	435
Mean	38.96
Std Dev	17.81

Turn on : 25.6225

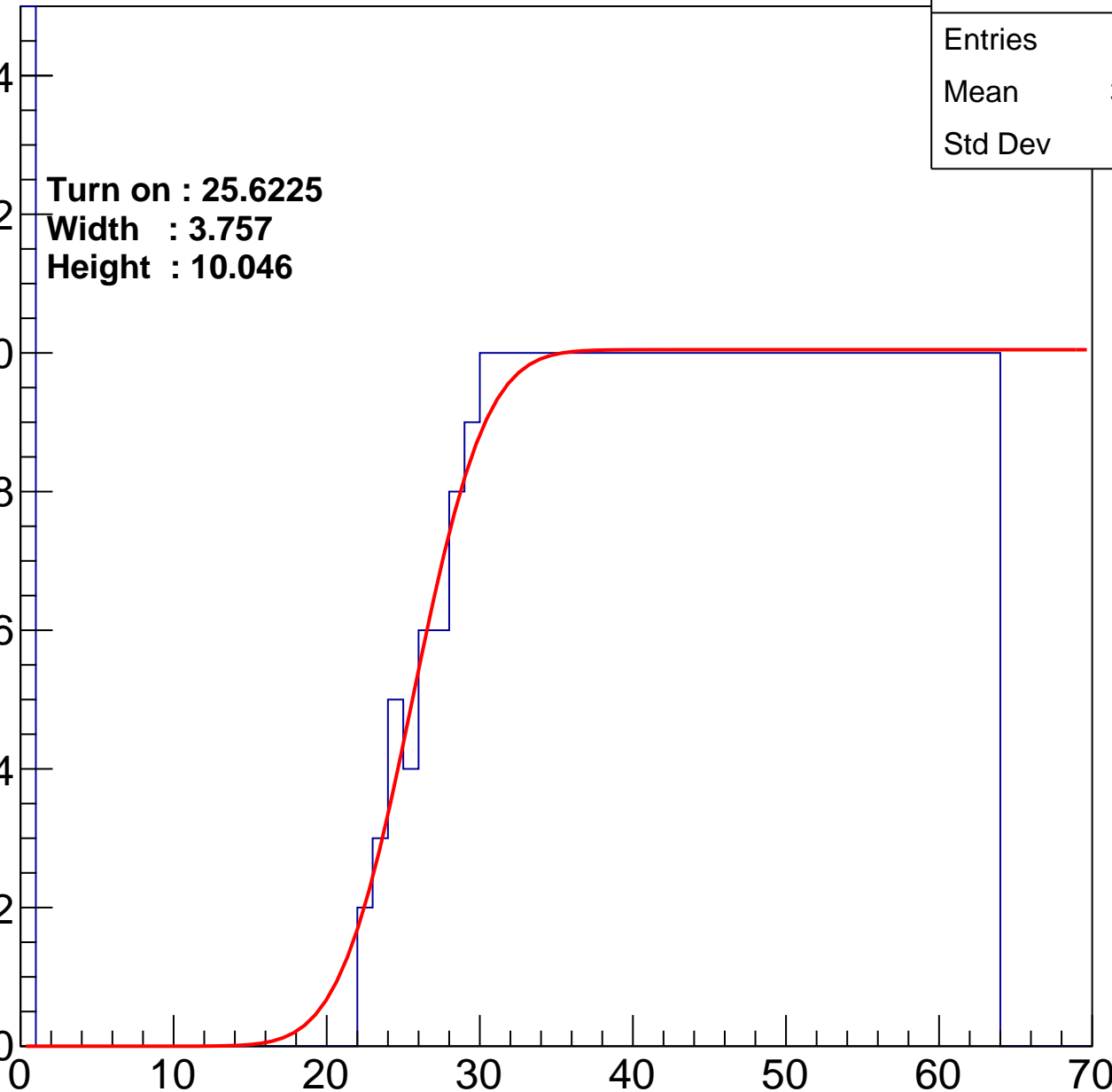
Width : 3.757

Height : 10.046

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch60

calib_packv5_041523_1651.root, FC#0, port C2

Entries	436
Mean	38.43
Std Dev	18.53

Turn on : 26.1755

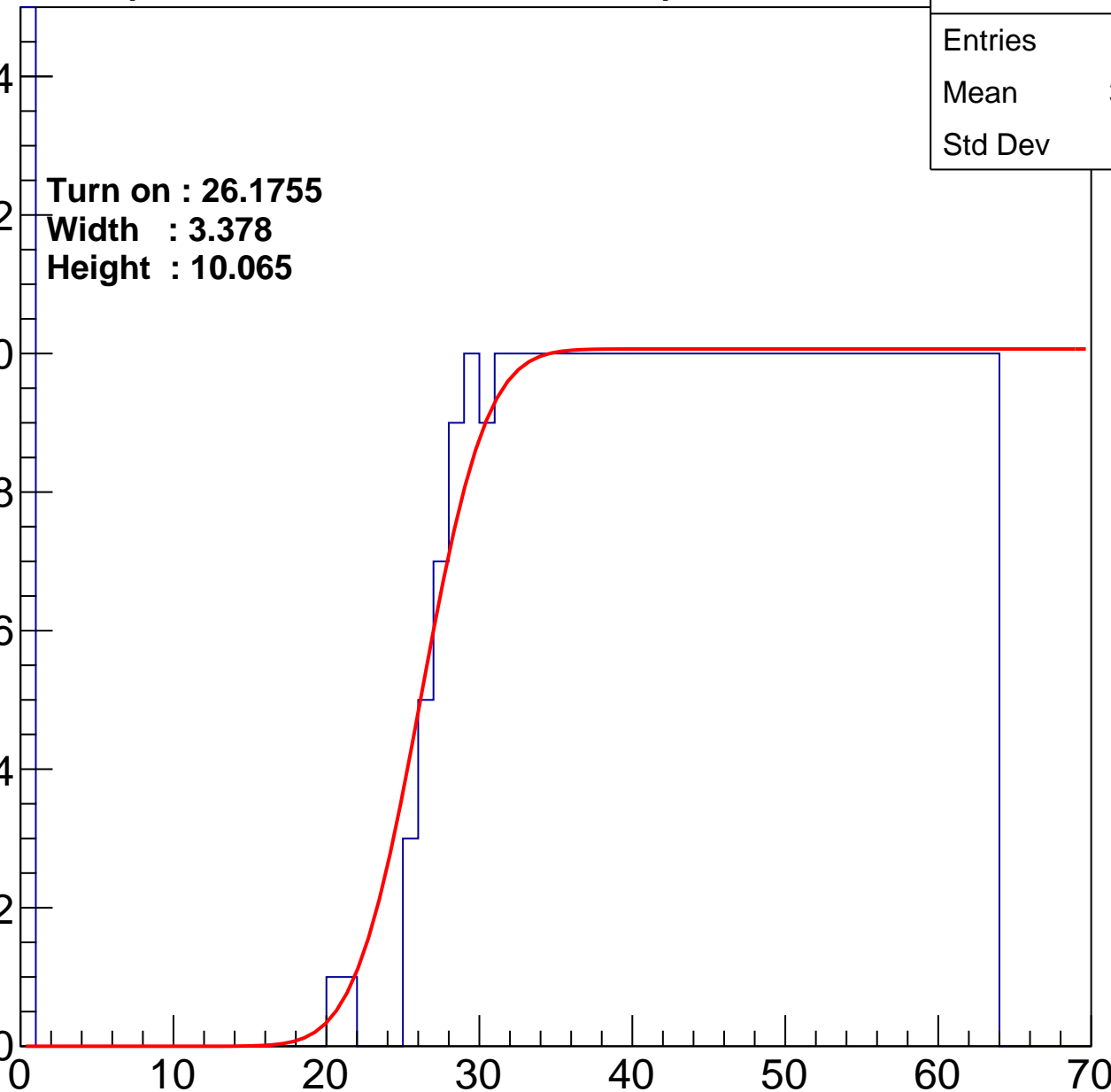
Width : 3.378

Height : 10.065

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch61

calib_packv5_041523_1651.root, FC#0, port C2

Entries	444
Mean	38.08
Std Dev	18.6

Turn on : 26.2755

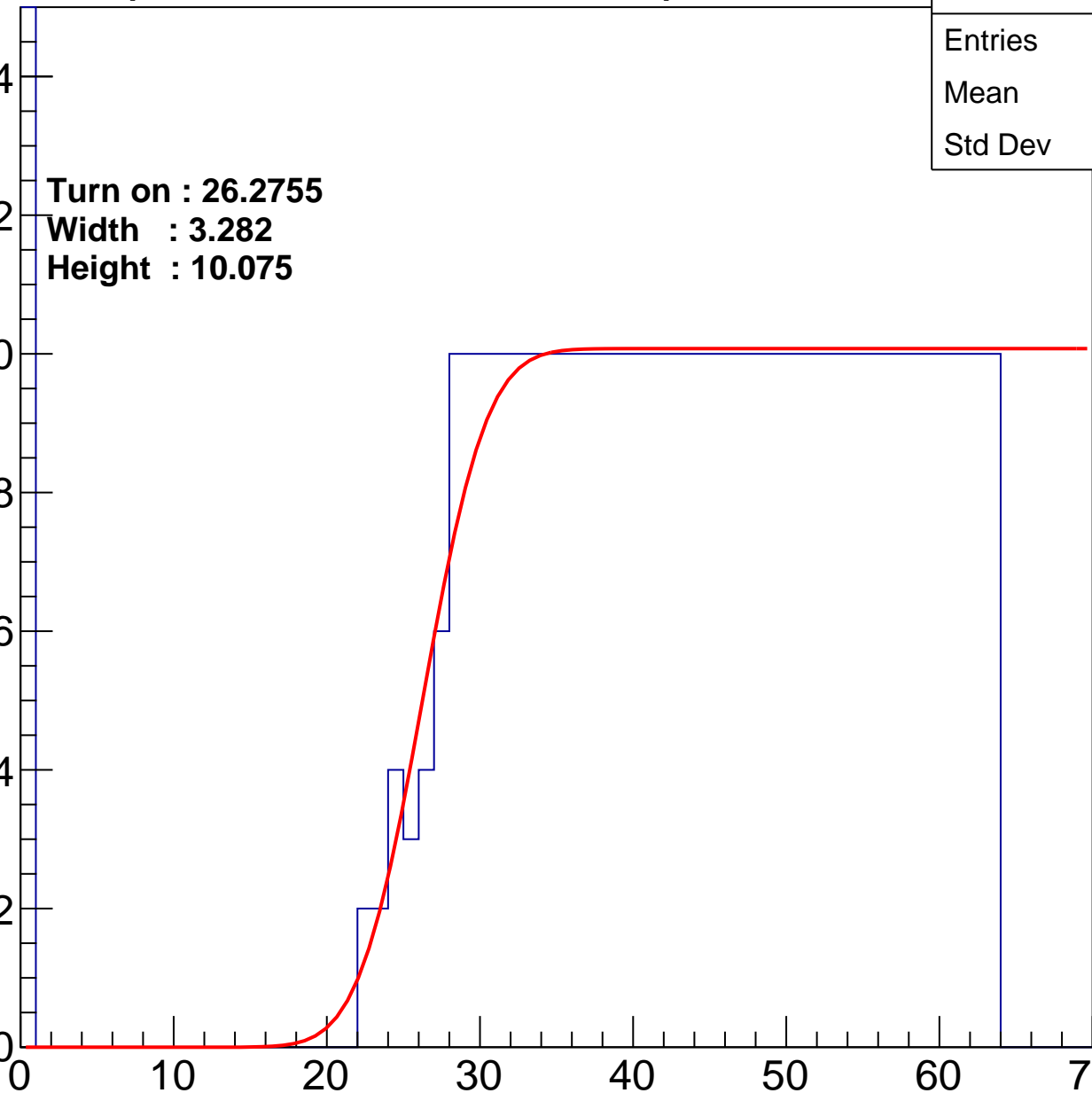
Width : 3.282

Height : 10.075

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch62

calib_packv5_041523_1651.root, FC#0, port C2

Entries	448
Mean	38.35
Std Dev	18.02

Turn on : 24.9920

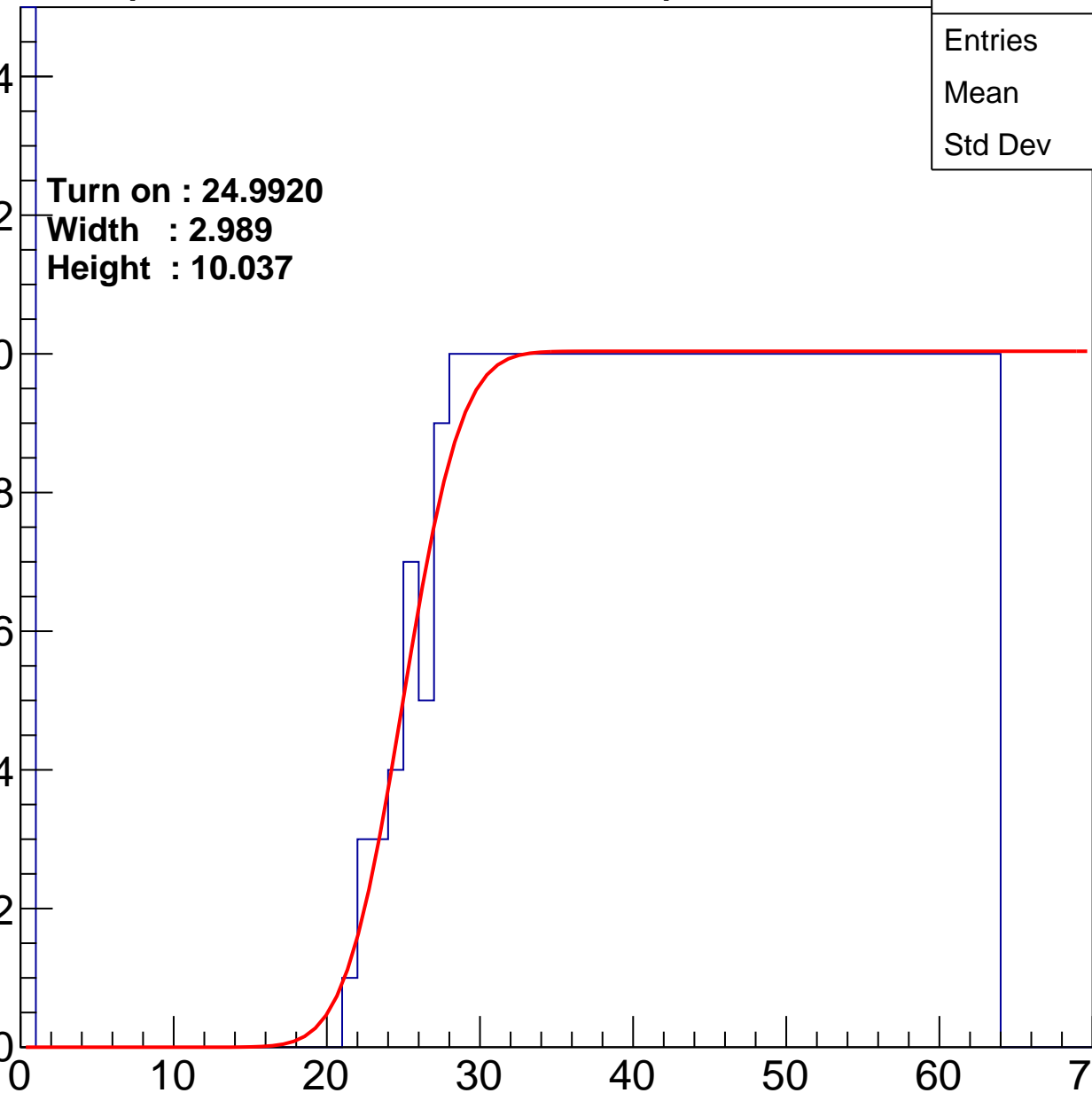
Width : 2.989

Height : 10.037

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch63

calib_packv5_041523_1651.root, FC#0, port C2

Entries	460
Mean	38.51
Std Dev	17.1

Turn on : 22.7735

Width : 1.965

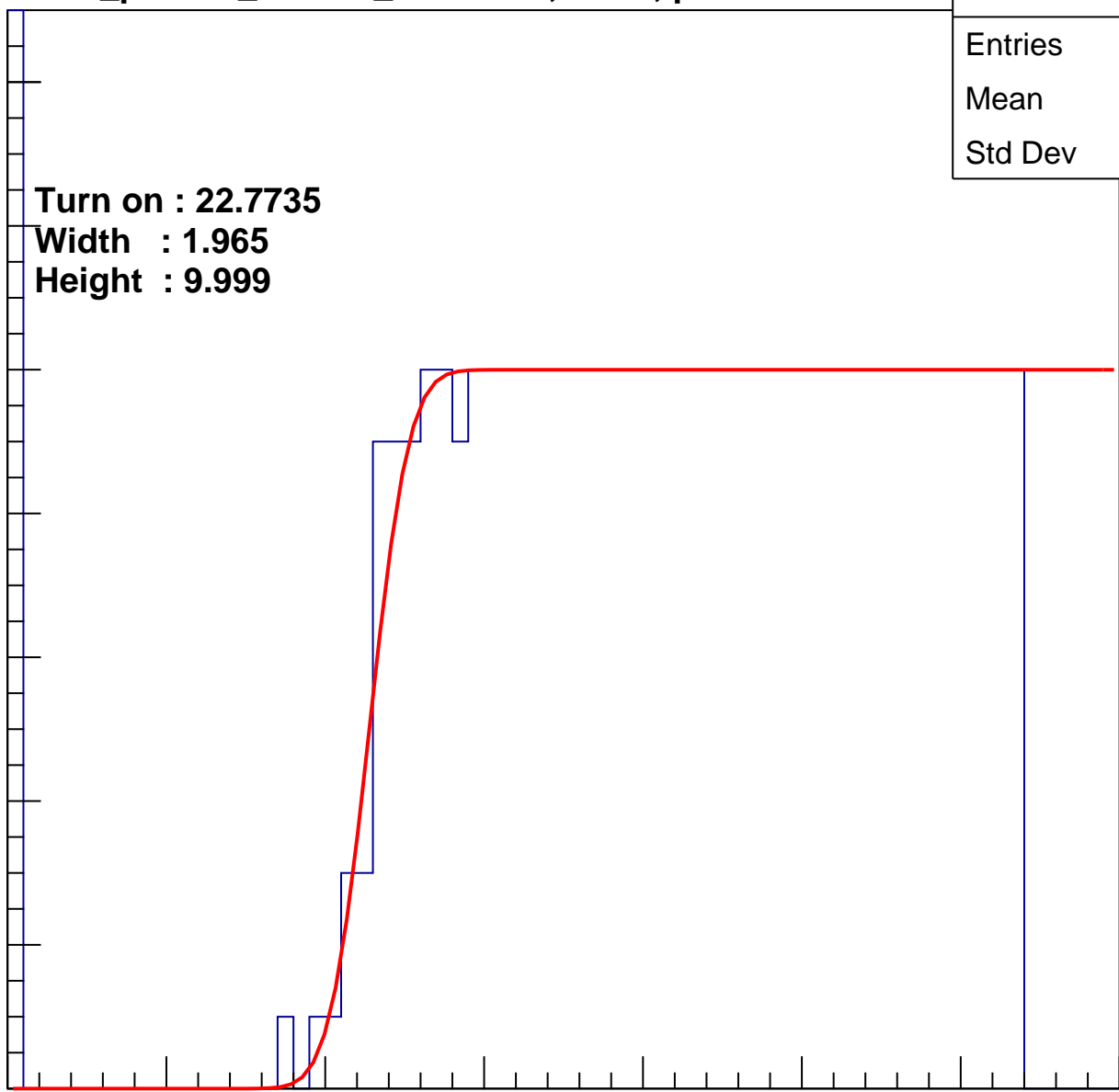
Height : 9.999

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L103S, U23-ch64

calib_packv5_041523_1651.root, FC#0, port C2

Entries	446
Mean	38.28
Std Dev	18.2

Turn on : 25.3373

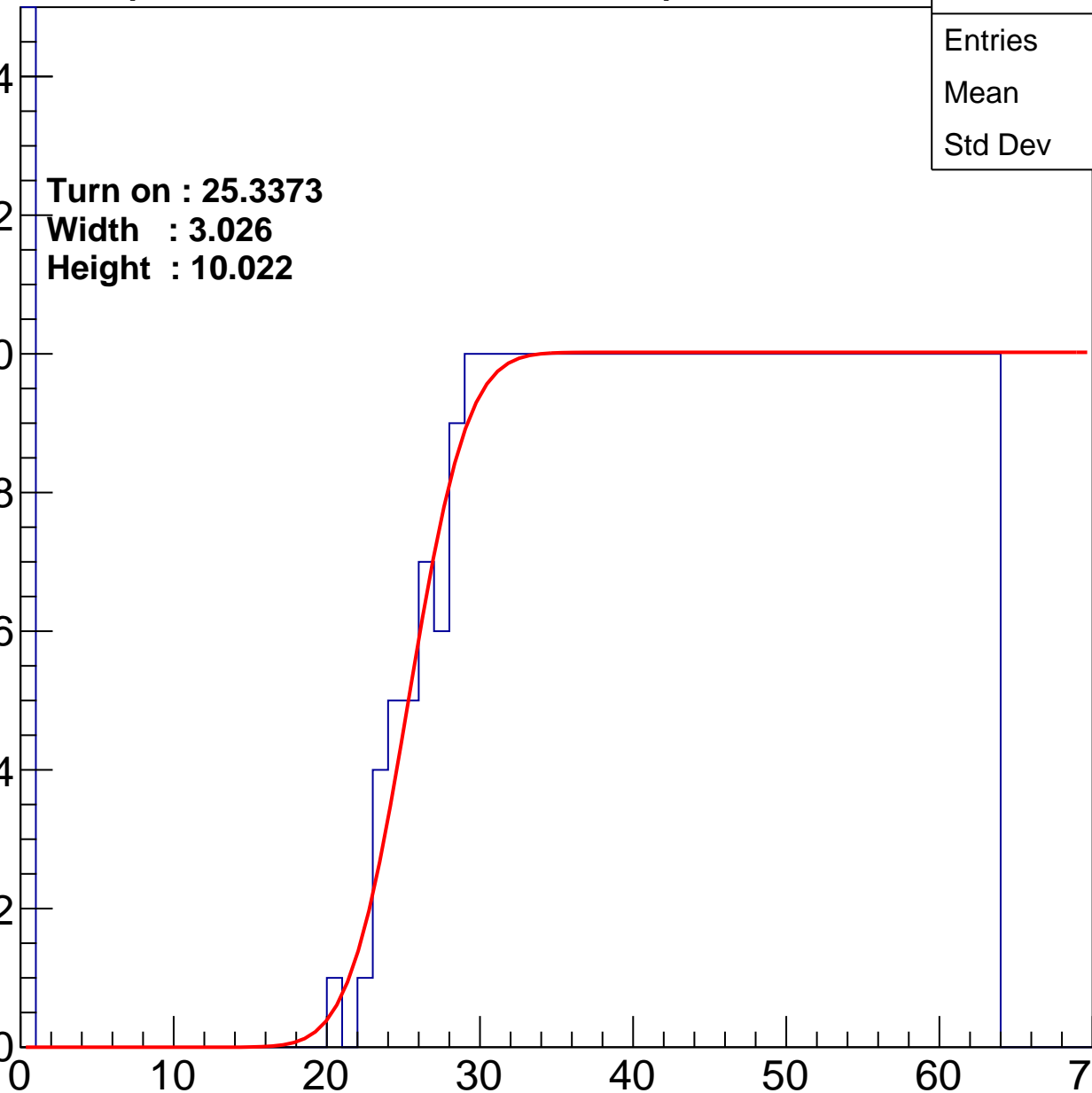
Width : 3.026

Height : 10.022

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch65

calib_packv5_041523_1651.root, FC#0, port C2

Entries	412
Mean	40.36
Std Dev	16.96

Turn on : 27.4836

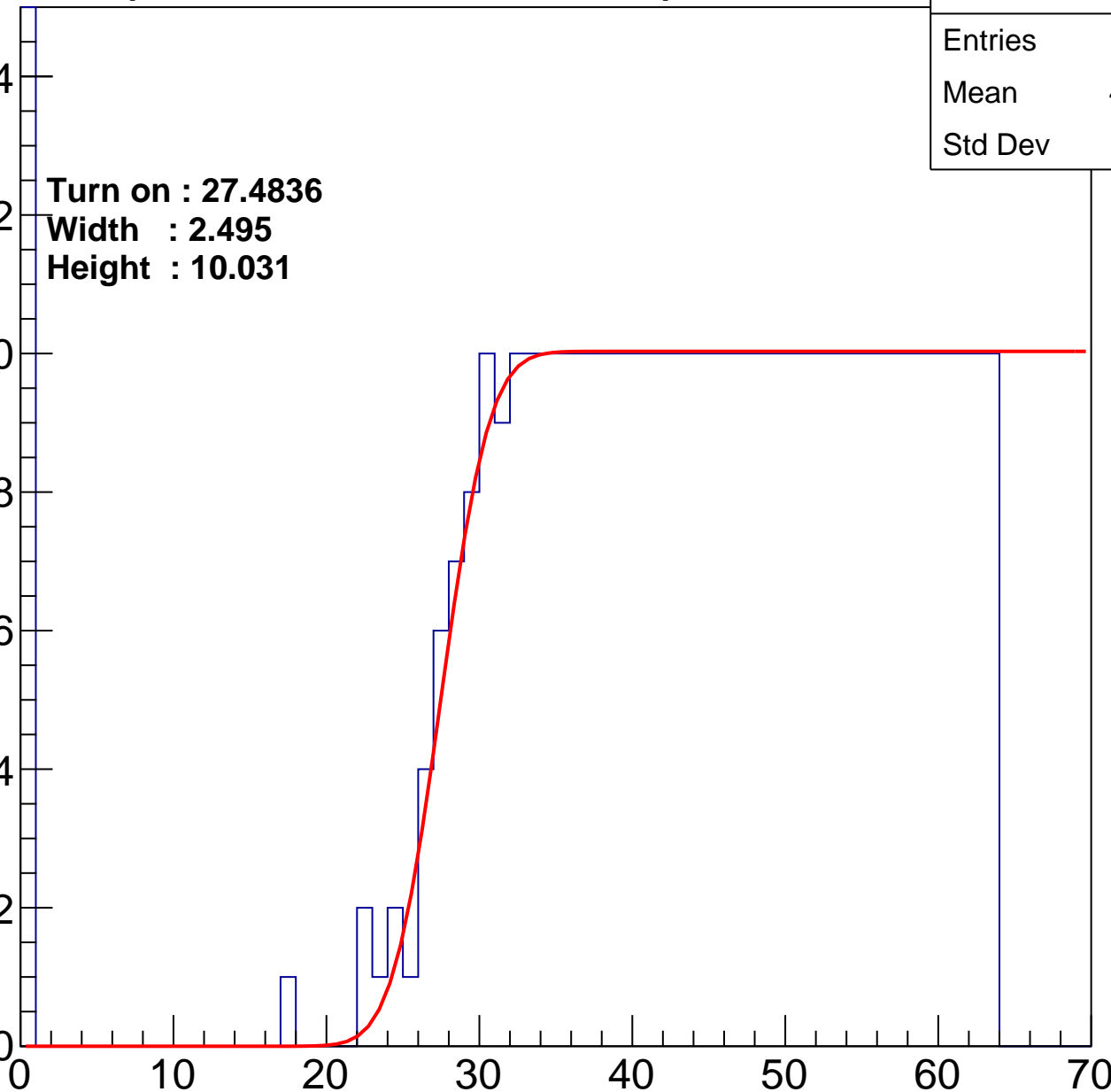
Width : 2.495

Height : 10.031

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch66

calib_packv5_041523_1651.root, FC#0, port C2

Entries	441
Mean	38.93
Std Dev	17.48

Turn on : 25.6274

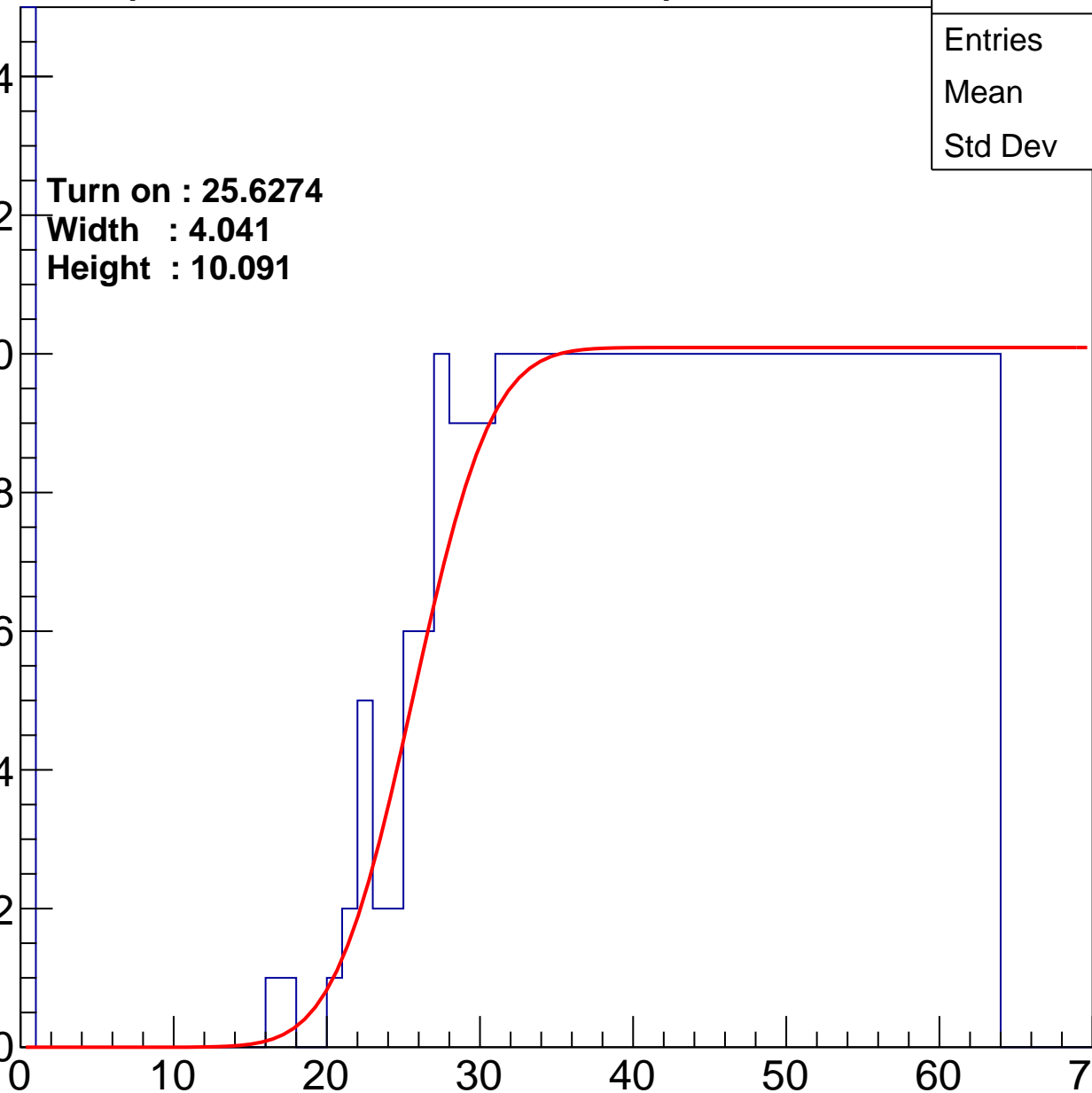
Width : 4.041

Height : 10.091

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch67

calib_packv5_041523_1651.root, FC#0, port C2

Entries	424
Mean	39.38
Std Dev	17.8

Turn on : 26.5233

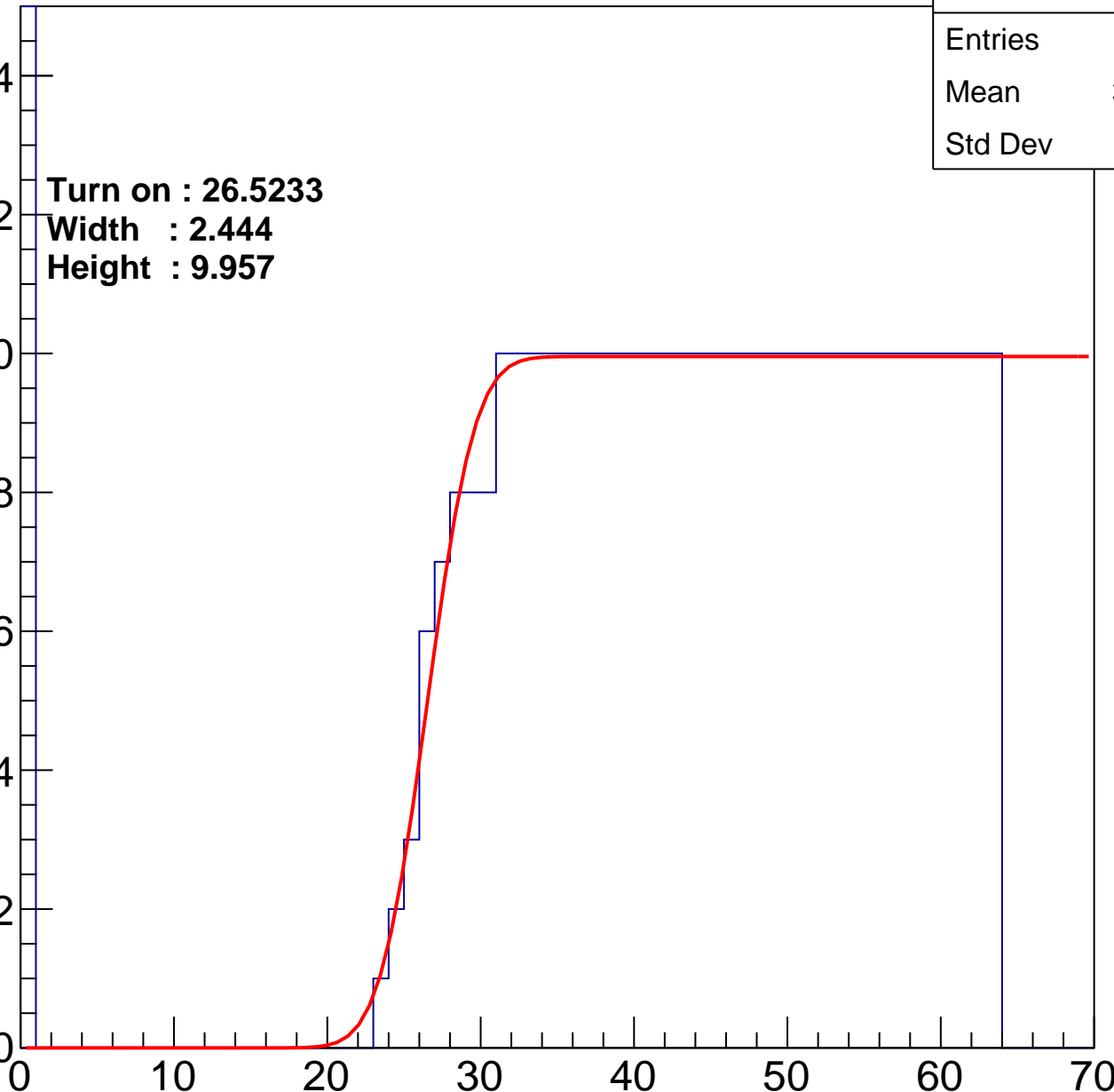
Width : 2.444

Height : 9.957

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch68

calib_packv5_041523_1651.root, FC#0, port C2

Entries	435
Mean	40.06
Std Dev	16.02

Turn on : 23.6602

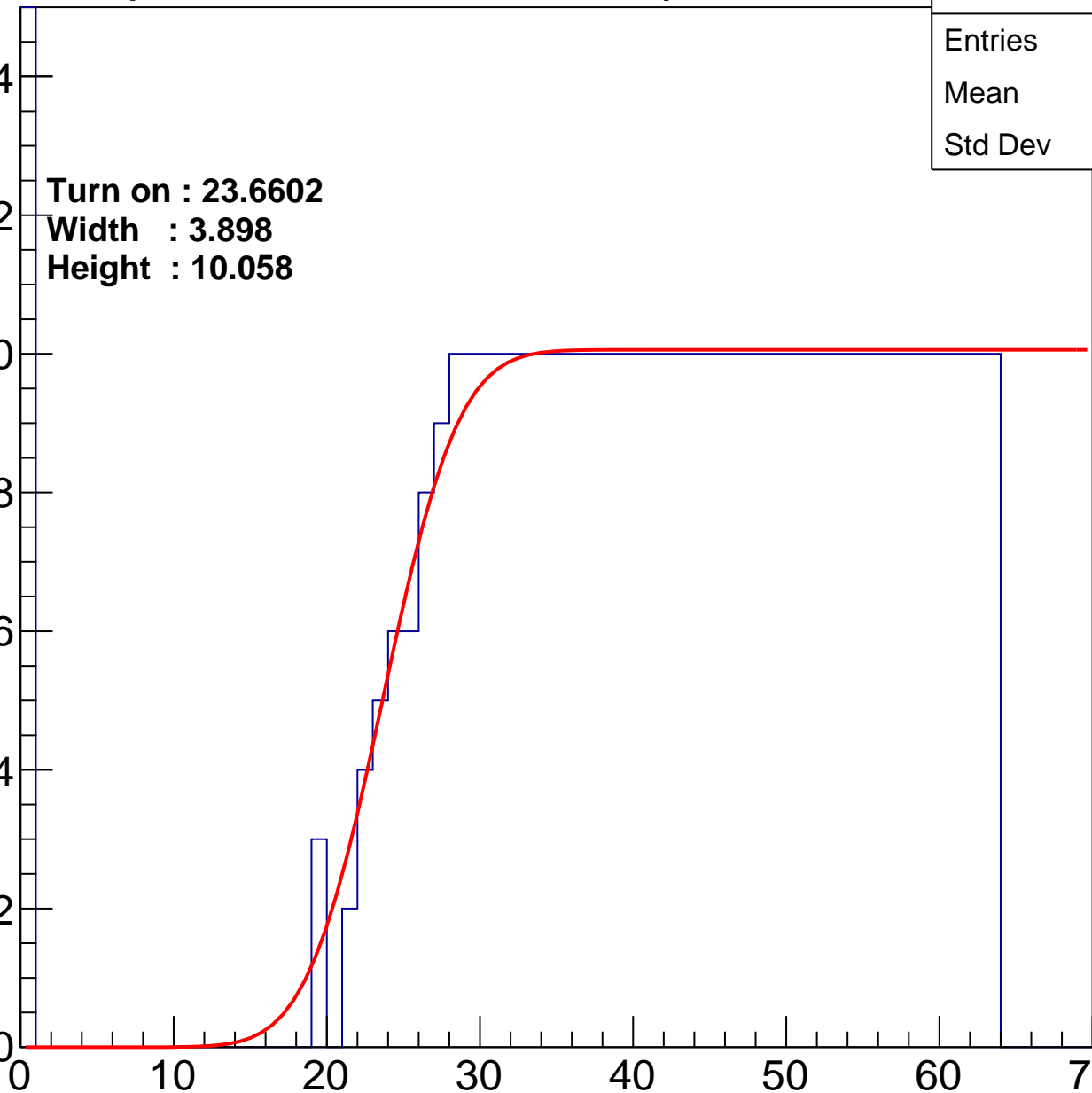
Width : 3.898

Height : 10.058

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch69

calib_packv5_041523_1651.root, FC#0, port C2

Entries	454
Mean	38.14
Std Dev	17.99

Turn on : 24.2616

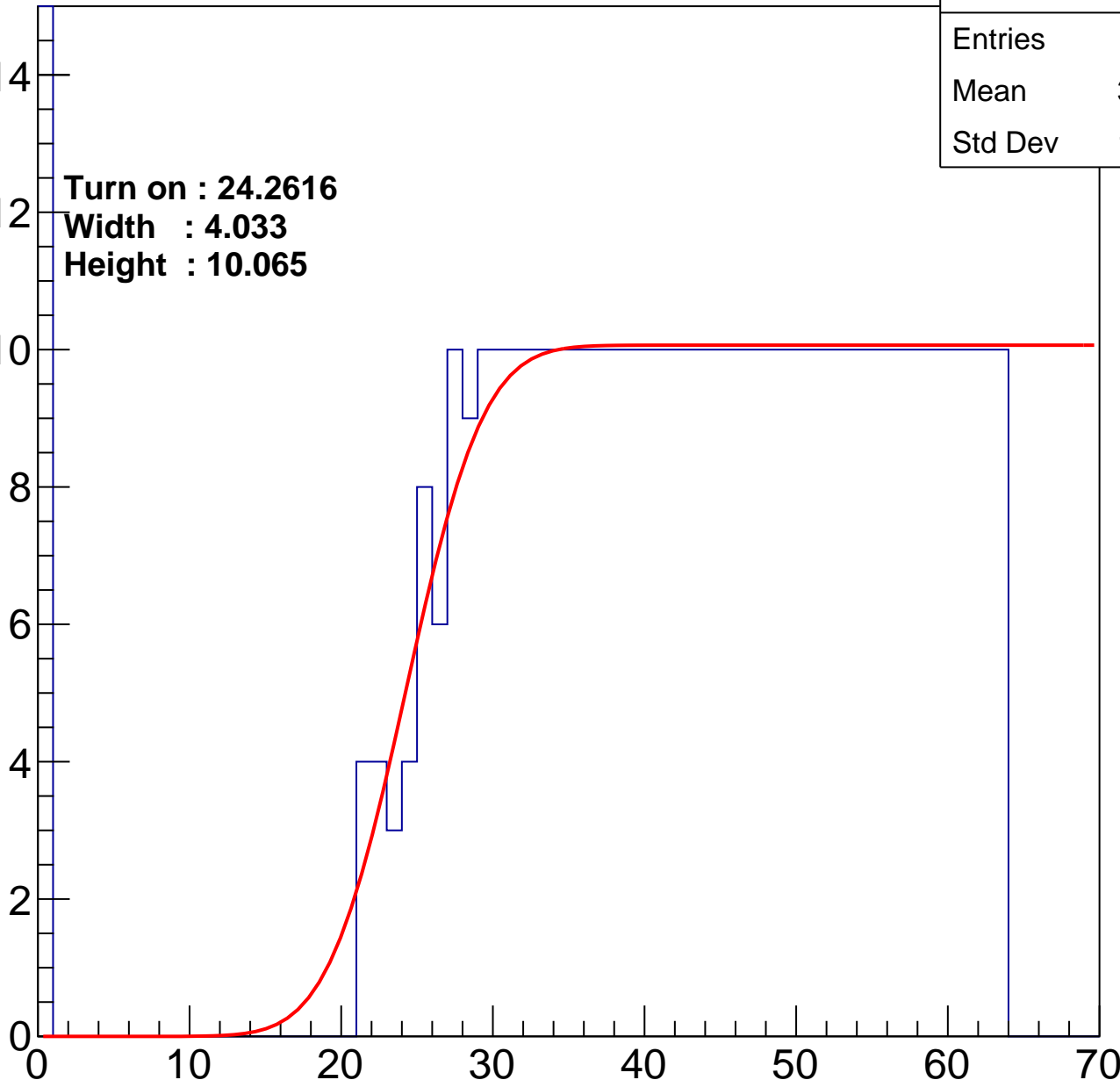
Width : 4.033

Height : 10.065

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch70

calib_packv5_041523_1651.root, FC#0, port C2

Entries	440
Mean	39.58
Std Dev	16.55

Turn on : 23.8702

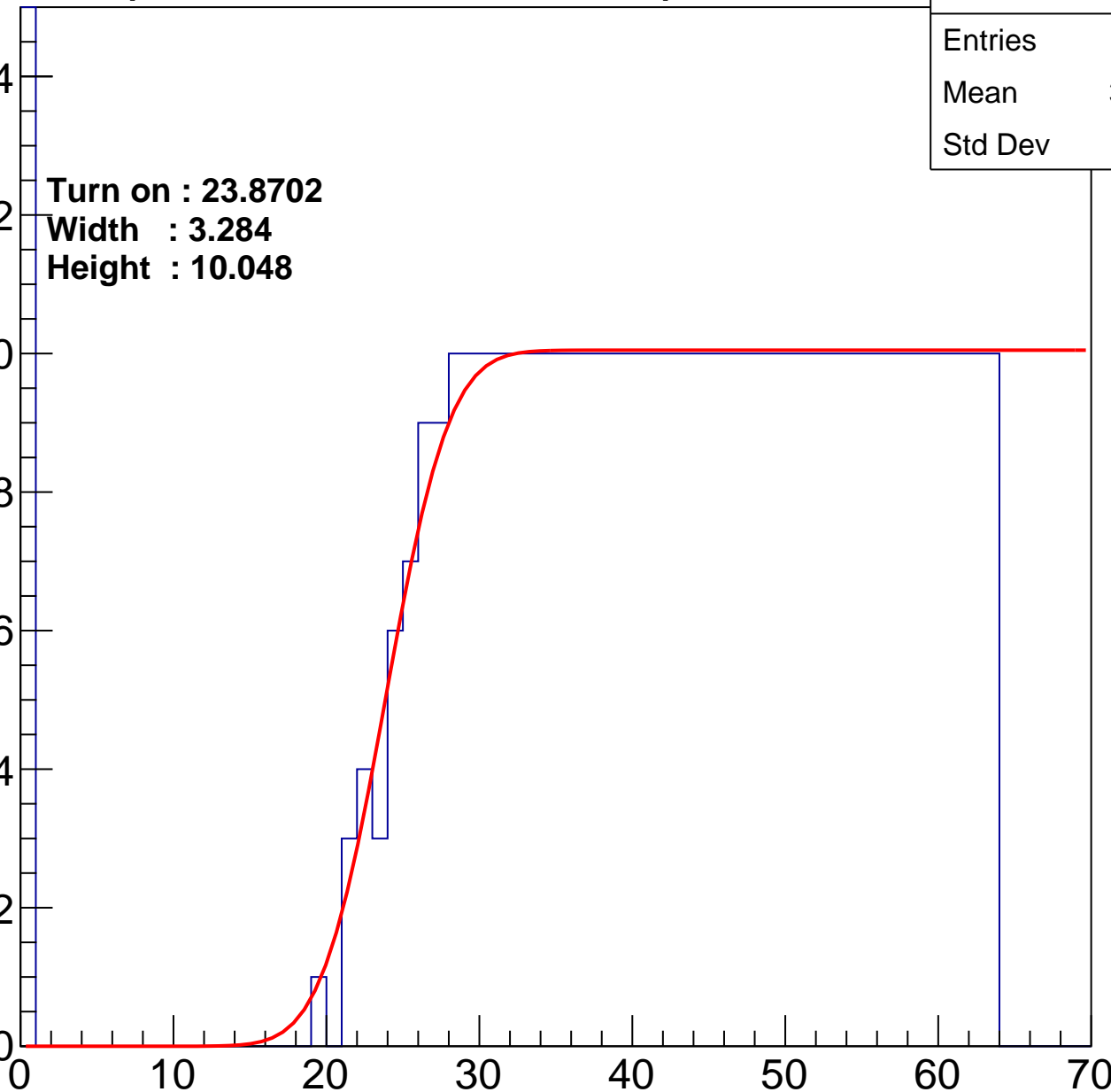
Width : 3.284

Height : 10.048

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch71

calib_packv5_041523_1651.root, FC#0, port C2

Entries	431
Mean	39.41
Std Dev	17.38

Turn on : 26.1237

Width : 1.468

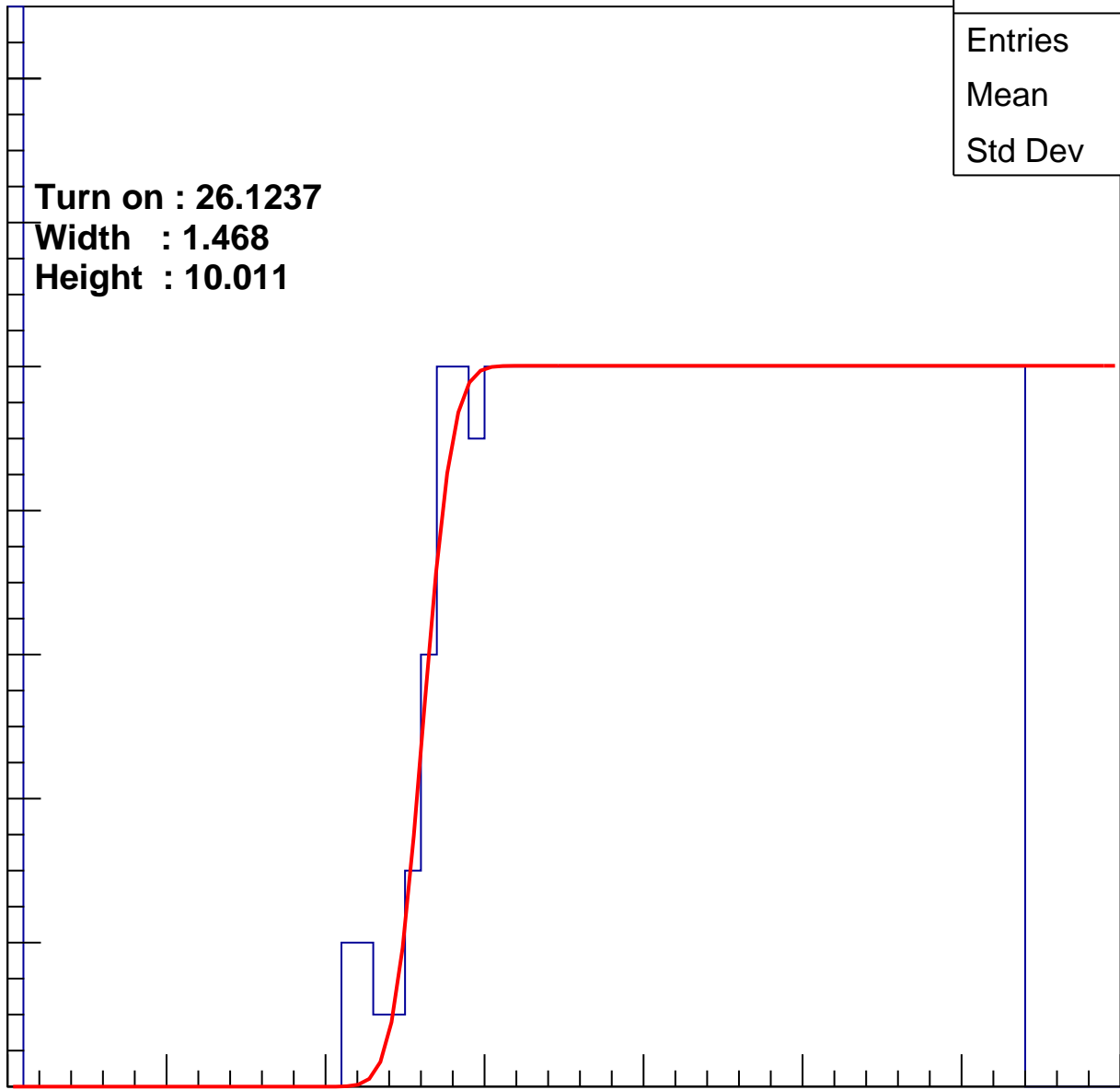
Height : 10.011

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L103S, U23-ch72

calib_packv5_041523_1651.root, FC#0, port C2

Entries	423
Mean	39.79
Std Dev	17.19

Turn on : 25.6331

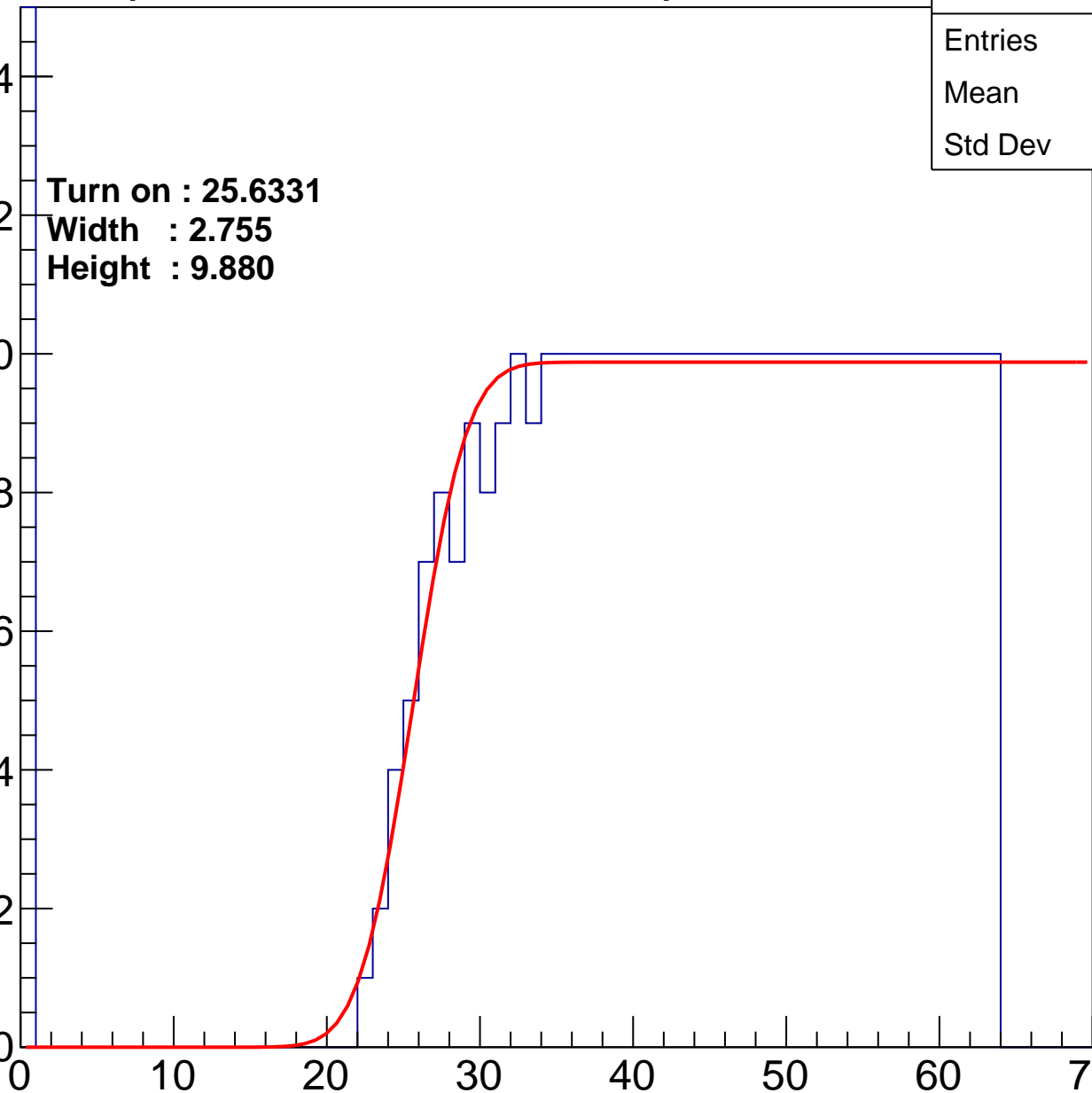
Width : 2.755

Height : 9.880

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch73

calib_packv5_041523_1651.root, FC#0, port C2

Entries	449
Mean	38.46
Std Dev	17.79

Turn on : 24.2162

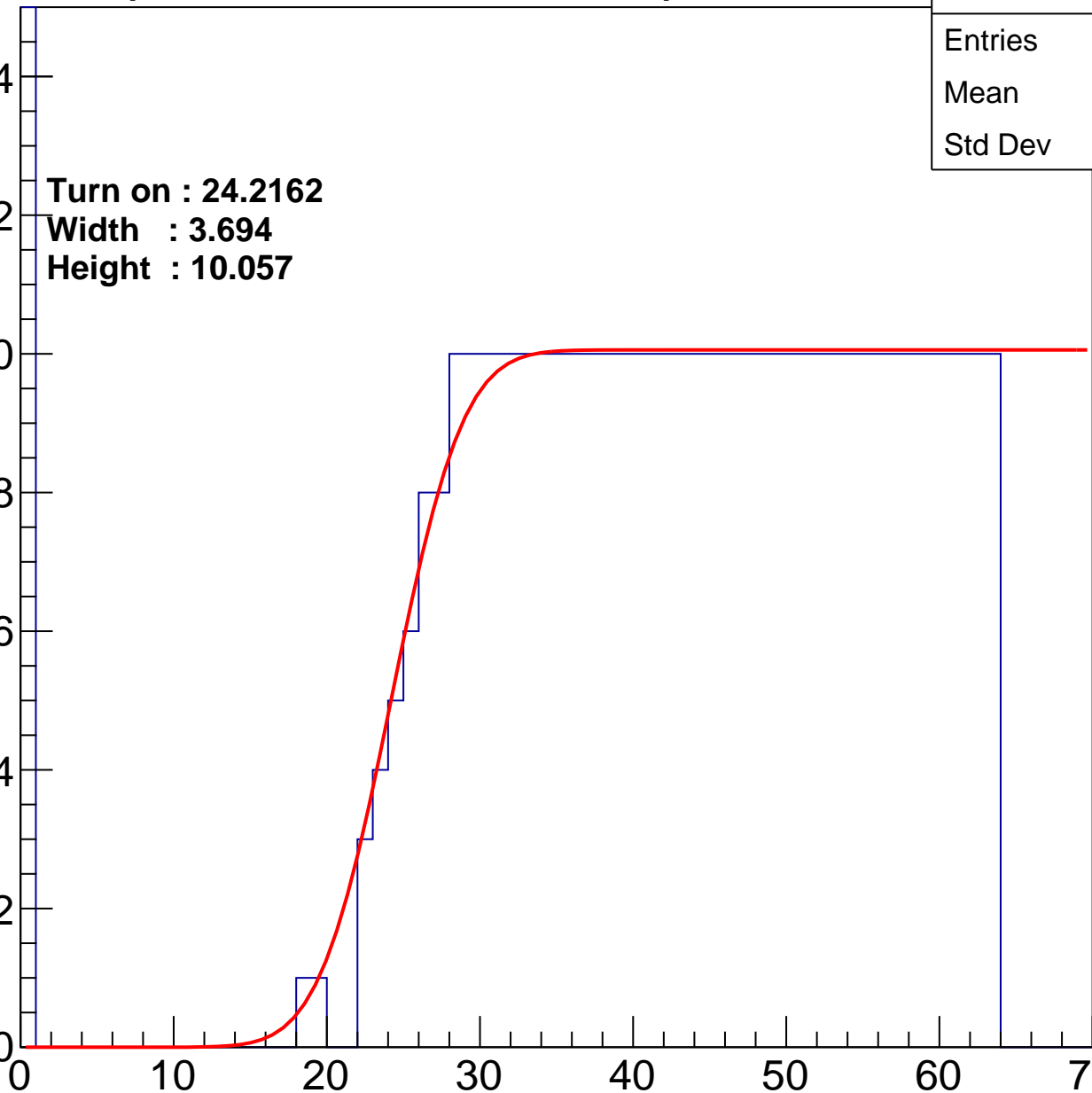
Width : 3.694

Height : 10.057

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch74

calib_packv5_041523_1651.root, FC#0, port C2

Entries	433
Mean	39.61
Std Dev	16.89

Turn on : 25.3430

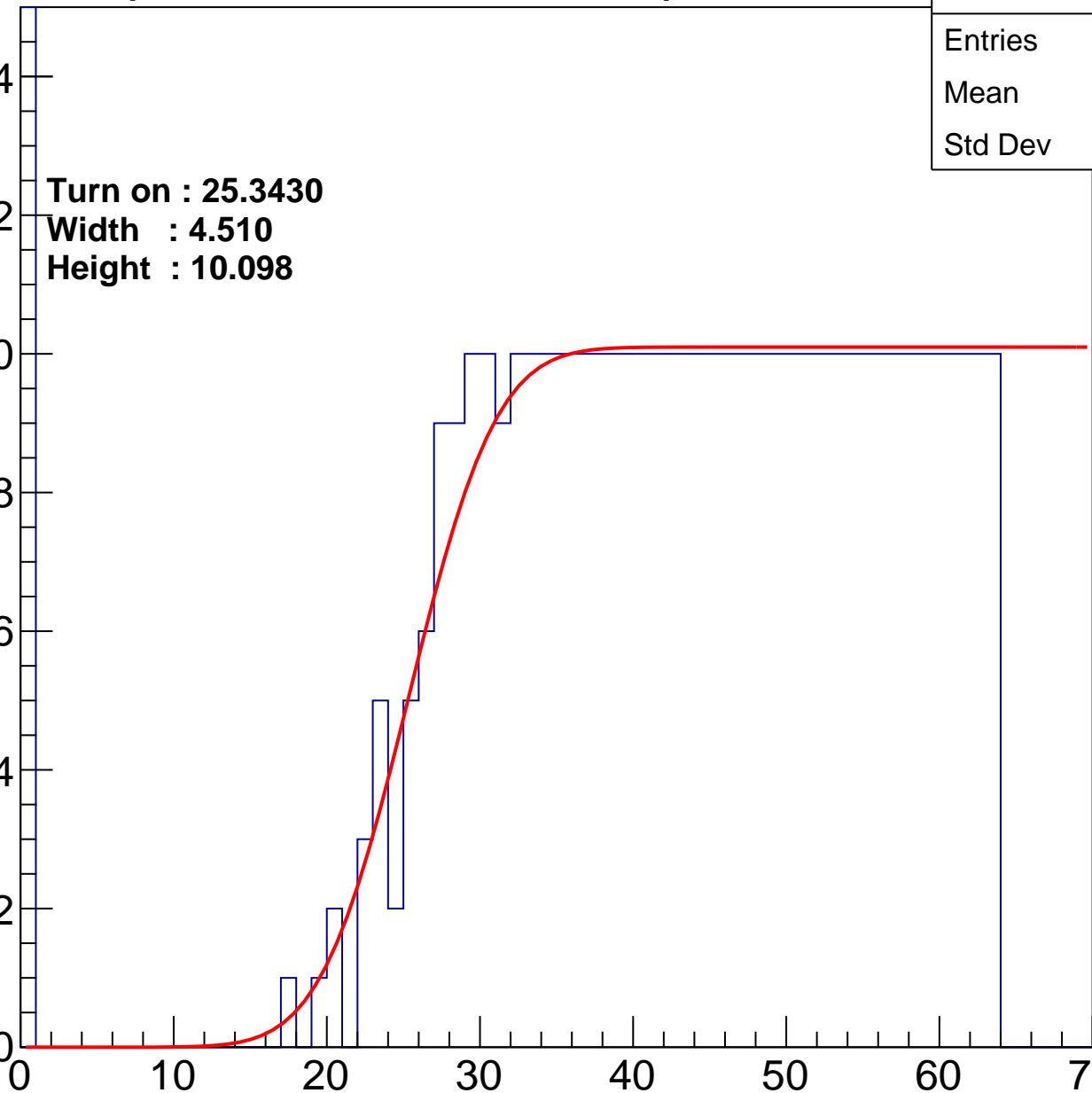
Width : 4.510

Height : 10.098

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch75

calib_packv5_041523_1651.root, FC#0, port C2

Entries	442
Mean	38.53
Std Dev	18.06

Turn on : 25.6265

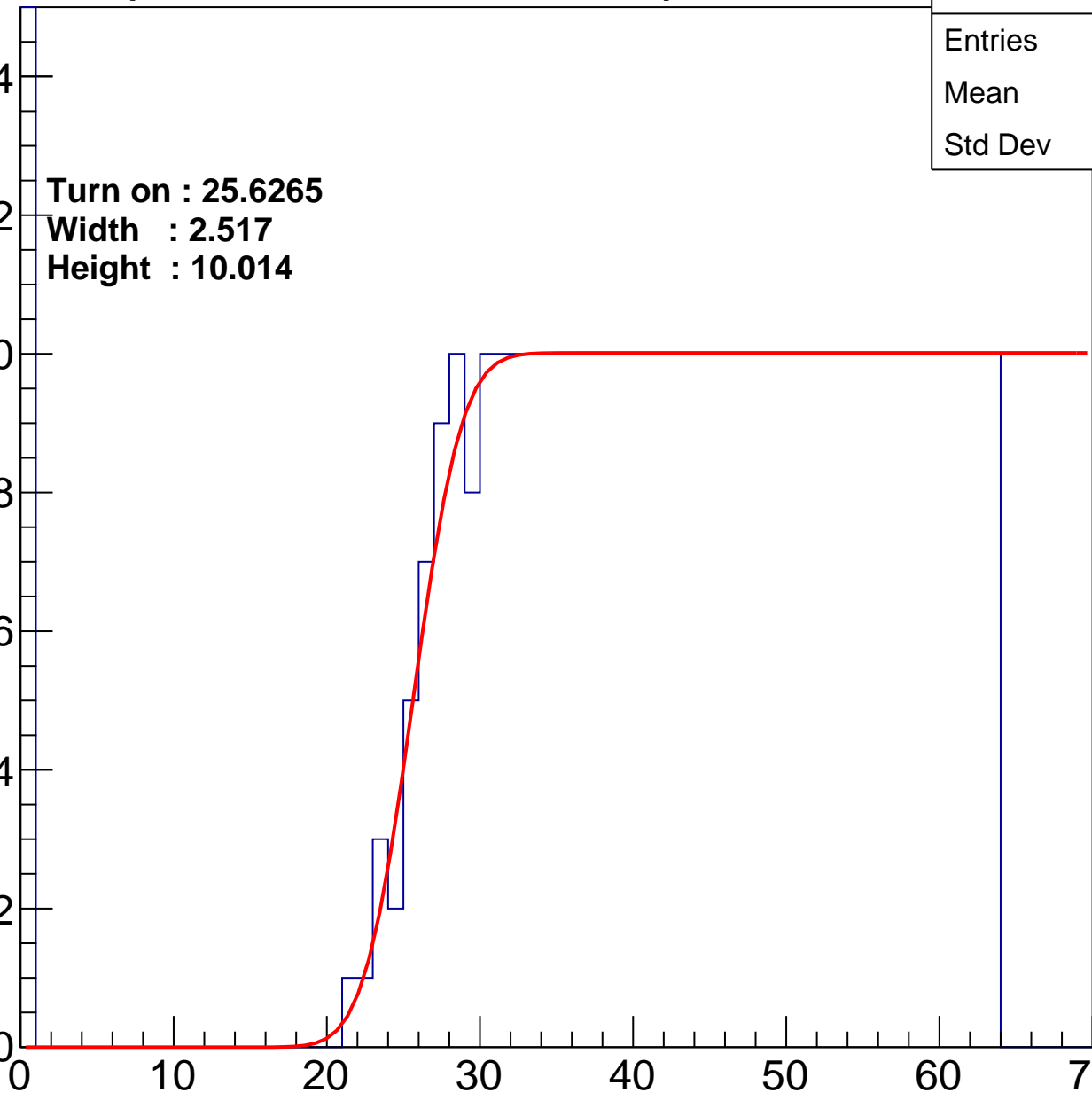
Width : 2.517

Height : 10.014

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch76

calib_packv5_041523_1651.root, FC#0, port C2

Entries	438
Mean	38.95
Std Dev	17.63

Turn on : 25.3575

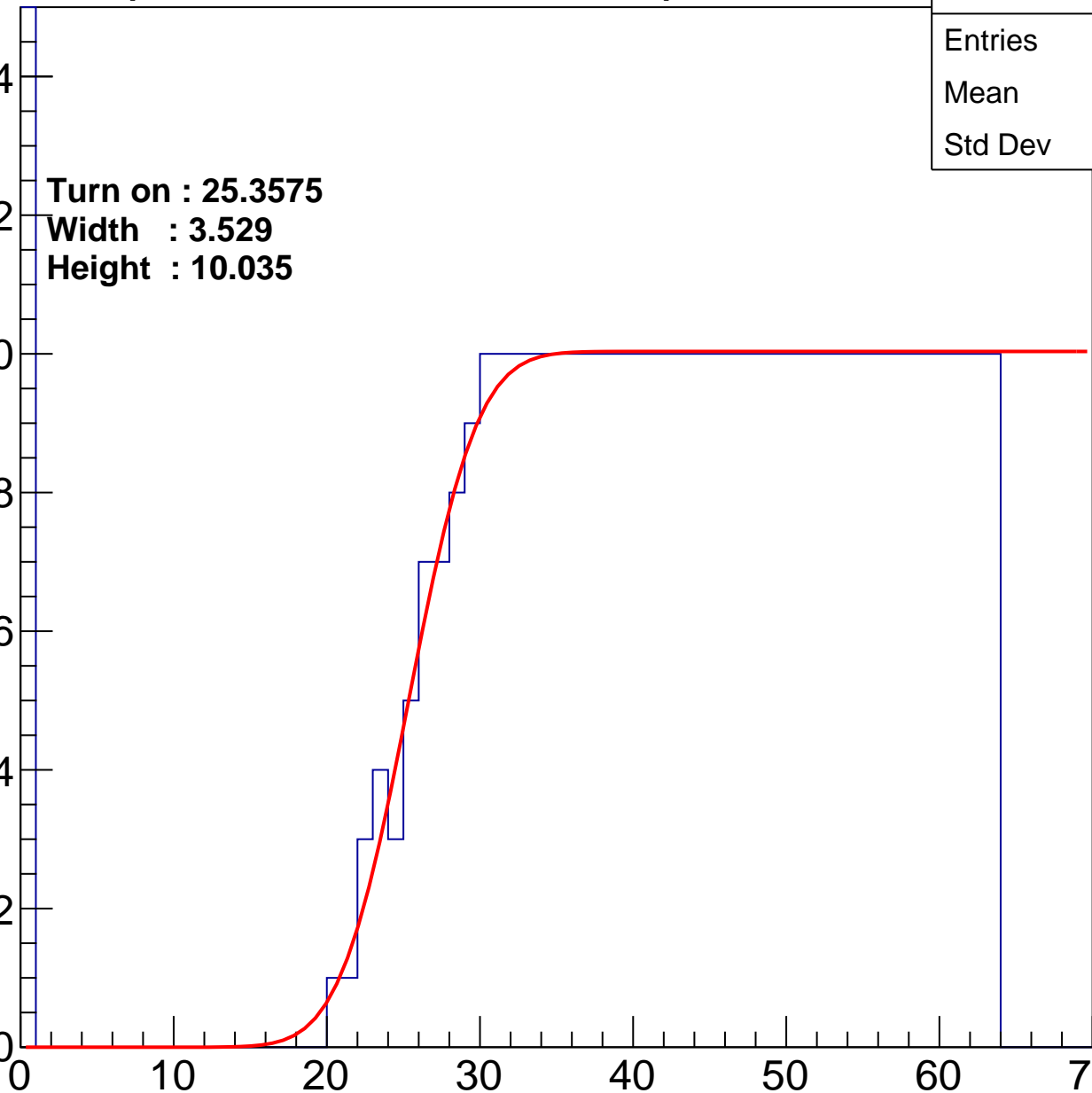
Width : 3.529

Height : 10.035

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch77

calib_packv5_041523_1651.root, FC#0, port C2

Entries	421
Mean	39.95
Std Dev	17.09

Turn on : 26.2703

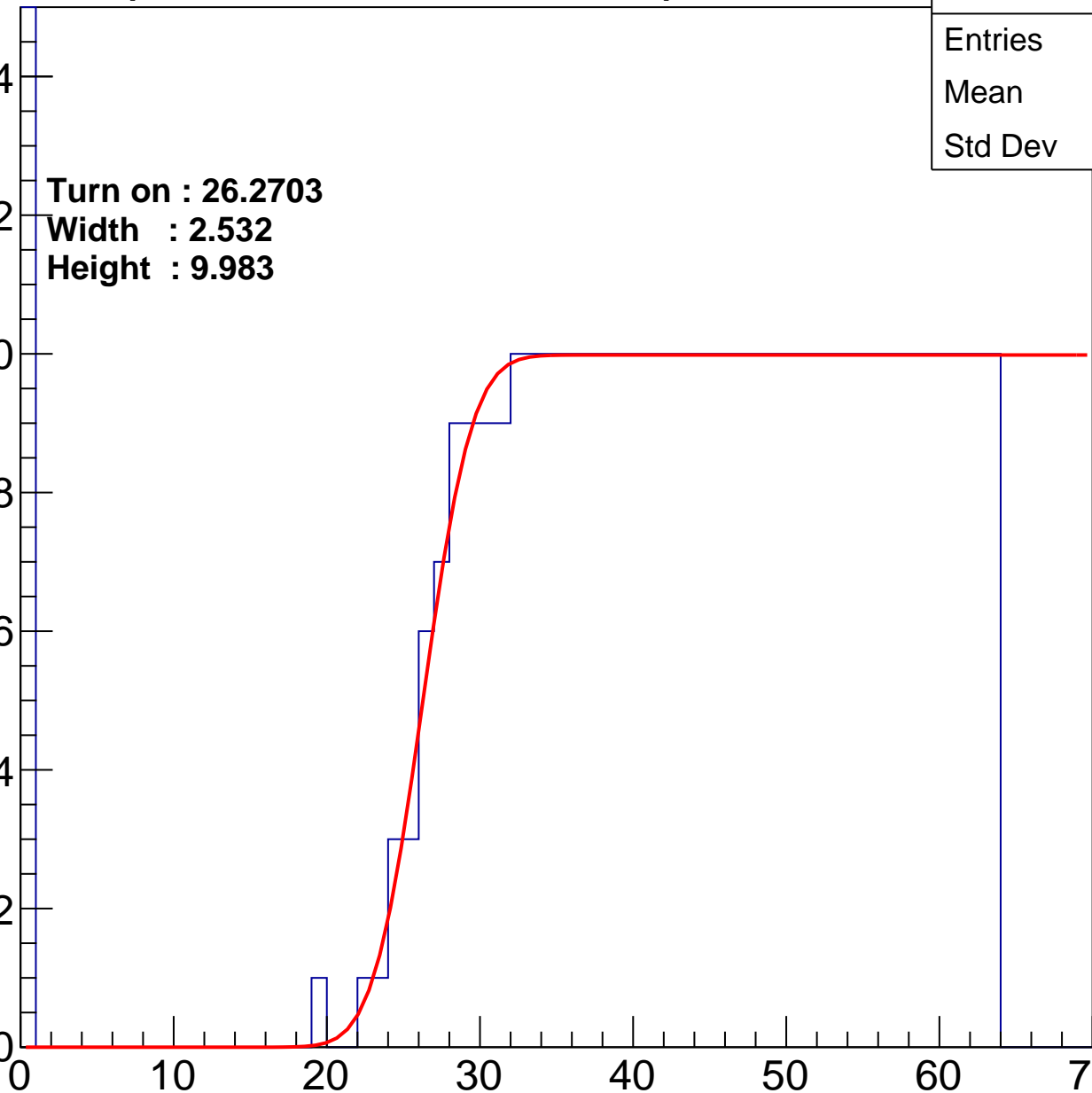
Width : 2.532

Height : 9.983

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch78

calib_packv5_041523_1651.root, FC#0, port C2

Entries	467
Mean	37.52
Std Dev	18.2

Turn on : 23.7644

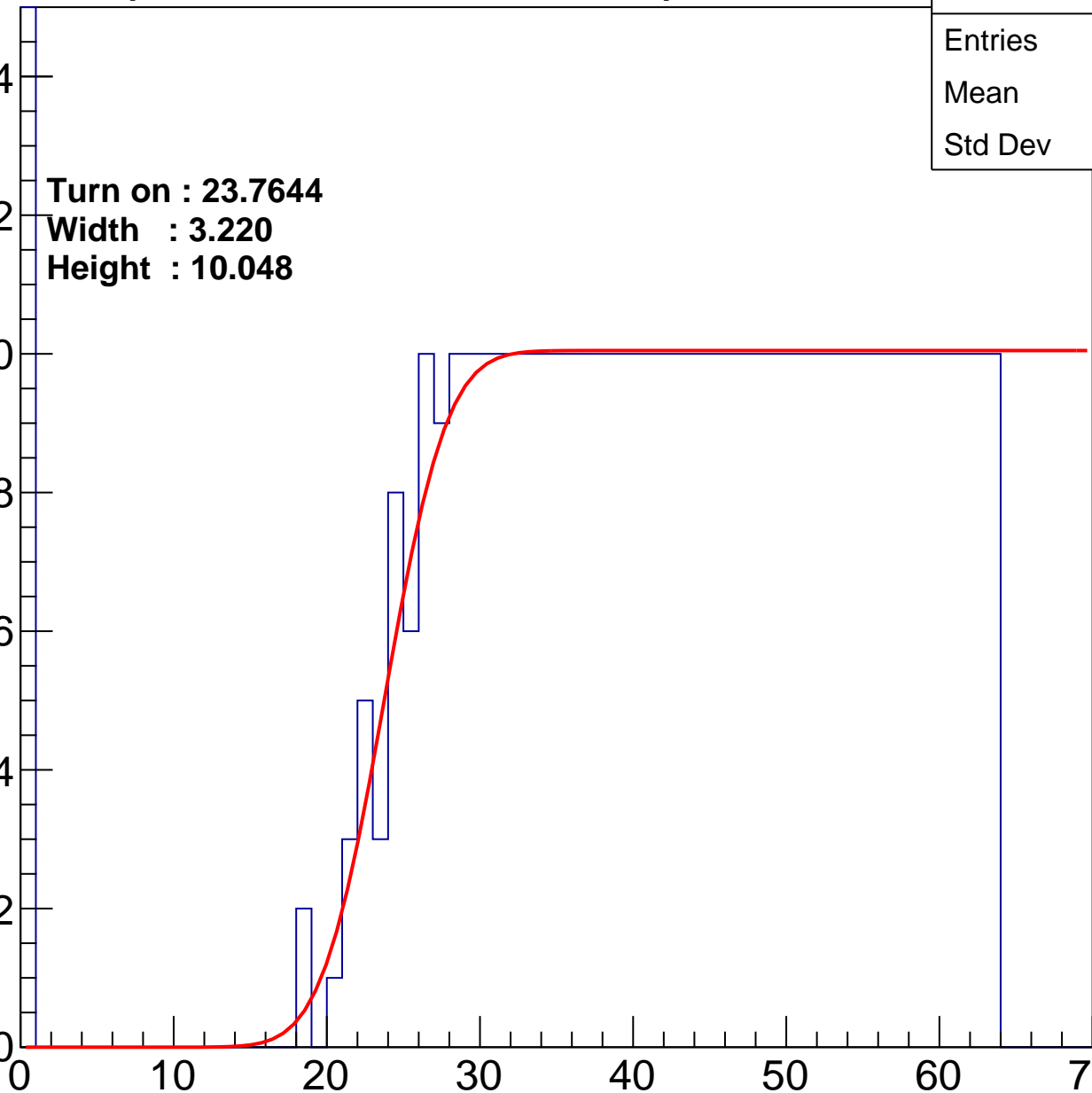
Width : 3.220

Height : 10.048

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch79

calib_packv5_041523_1651.root, FC#0, port C2

Entries	430
Mean	38.88
Std Dev	18.18

Turn on : 26.3161

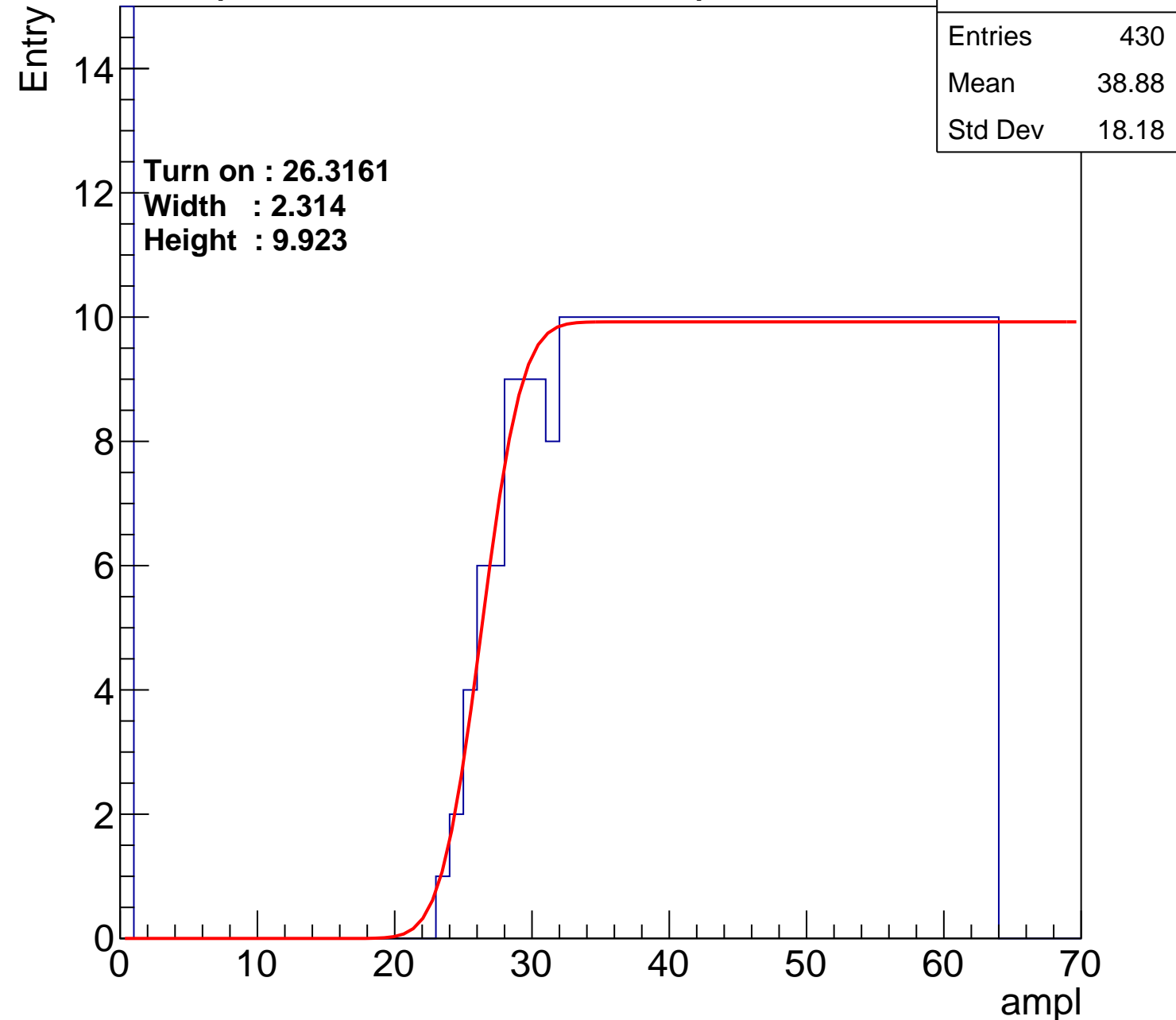
Width : 2.314

Height : 9.923

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch80

calib_packv5_041523_1651.root, FC#0, port C2

Entries	437
Mean	39.35
Std Dev	17.1

Turn on : 25.1431

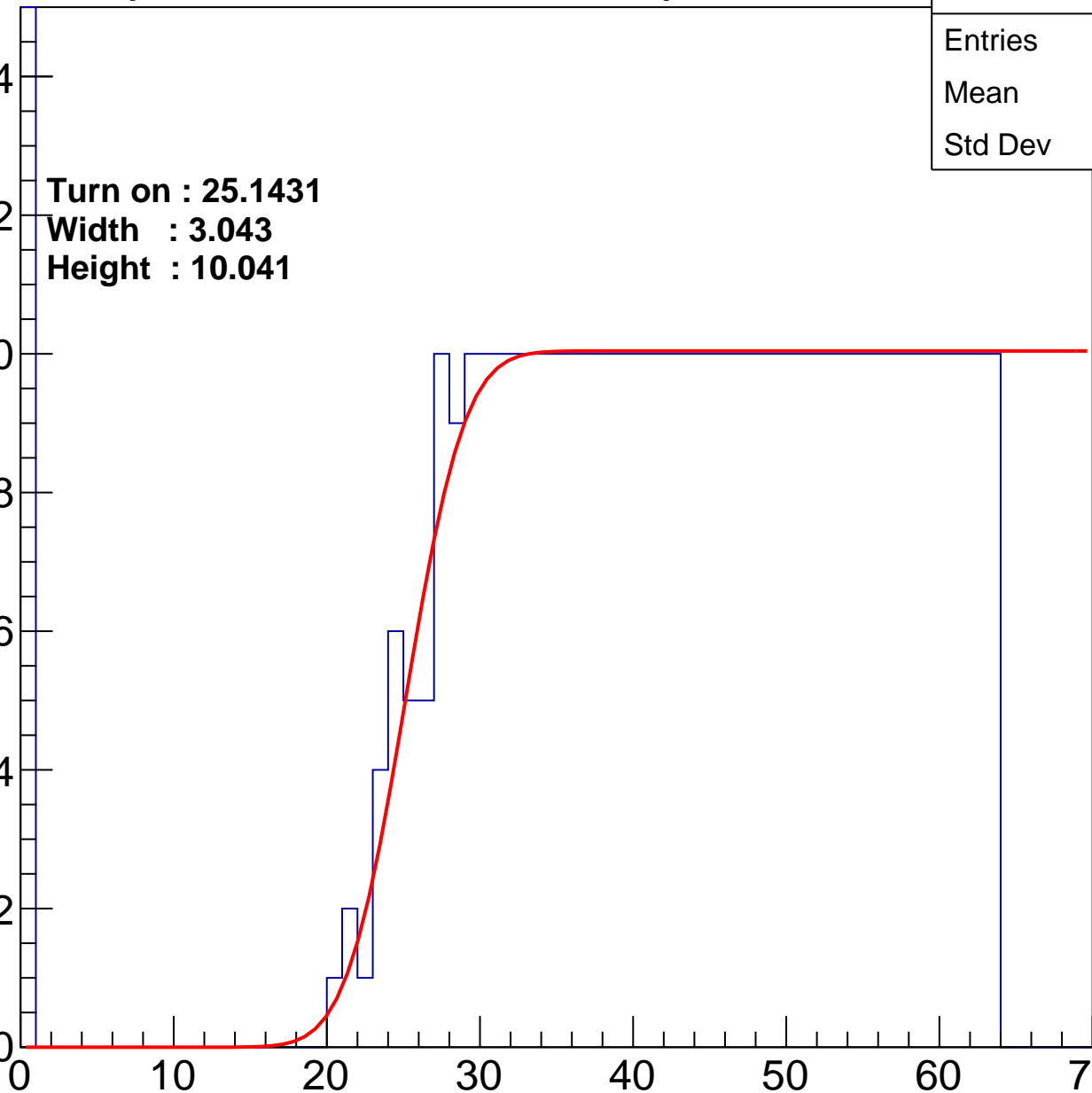
Width : 3.043

Height : 10.041

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch81

calib_packv5_041523_1651.root, FC#0, port C2

Entries	428
Mean	38.95
Std Dev	18.2

Turn on : 26.7568

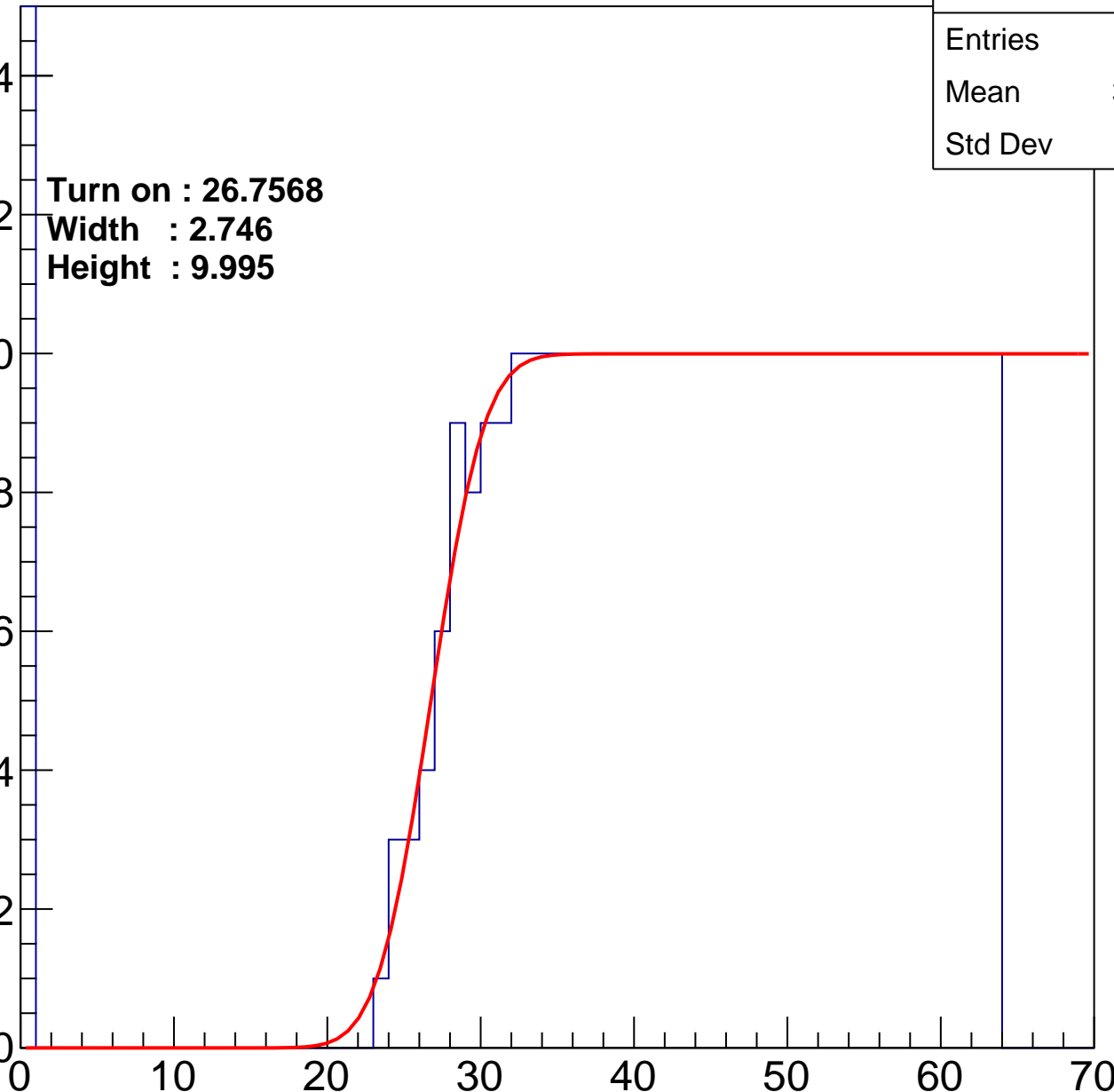
Width : 2.746

Height : 9.995

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch82

calib_packv5_041523_1651.root, FC#0, port C2

Entries	543
Mean	33.35
Std Dev	20.12

Turn on : 21.4562

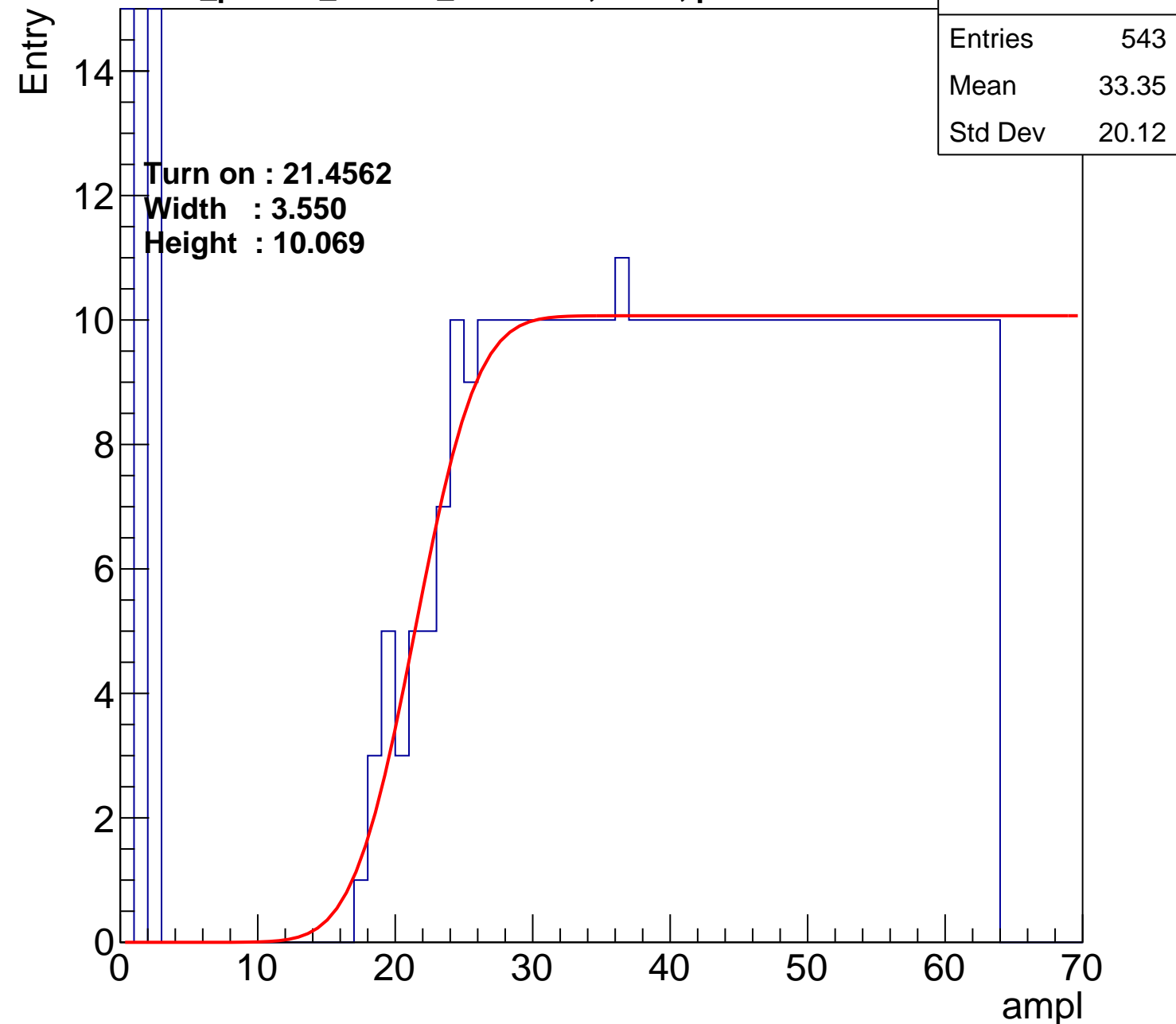
Width : 3.550

Height : 10.069

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch83

calib_packv5_041523_1651.root, FC#0, port C2

Entries	434
Mean	38.82
Std Dev	18.06

Turn on : 26.4109

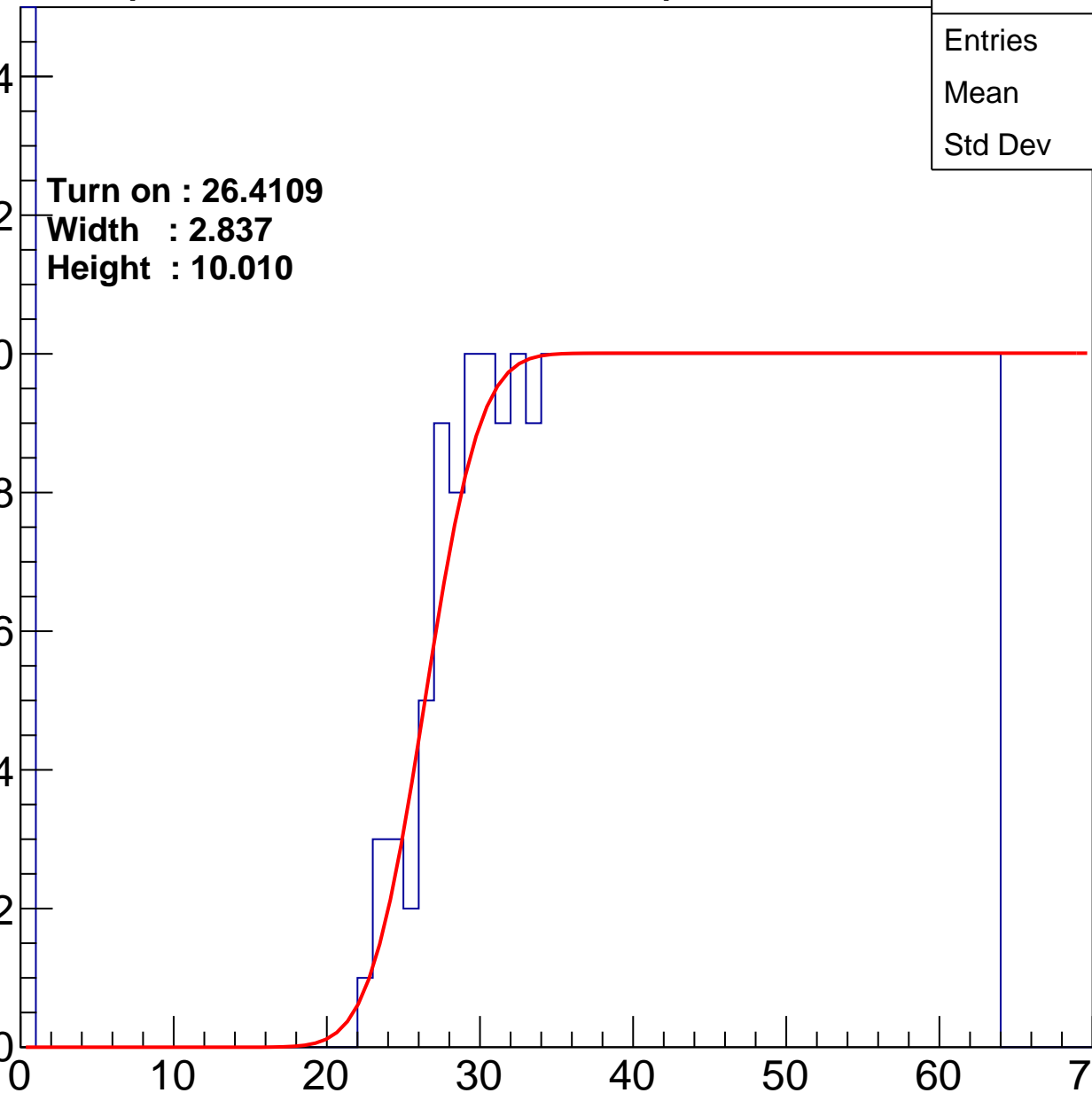
Width : 2.837

Height : 10.010

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch84

calib_packv5_041523_1651.root, FC#0, port C2

Entries	461
Mean	38.2
Std Dev	17.51

Turn on : 22.8055

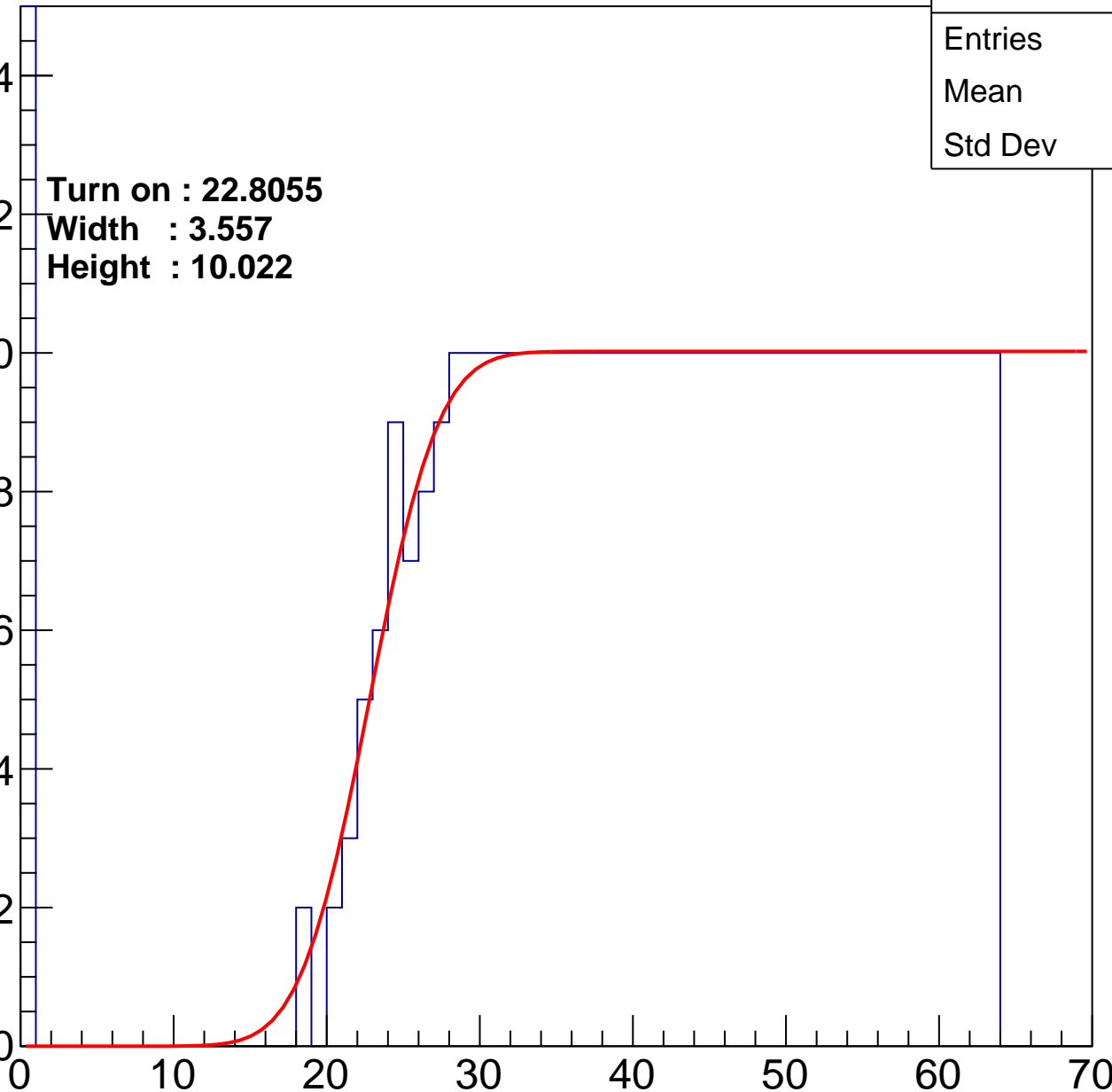
Width : 3.557

Height : 10.022

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch85

calib_packv5_041523_1651.root, FC#0, port C2

Entries	439
Mean	38.14
Std Dev	18.71

Turn on : 26.9037

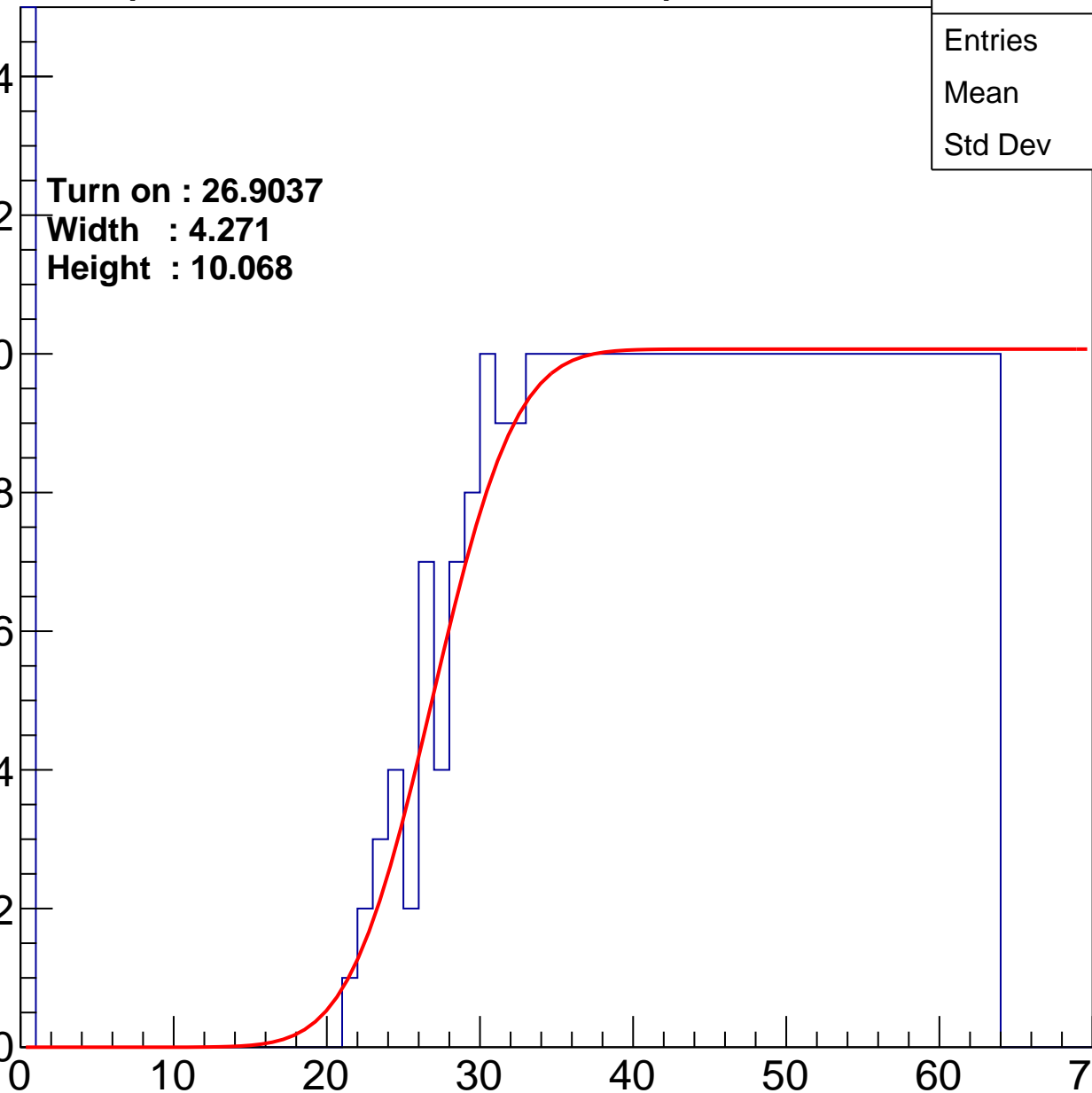
Width : 4.271

Height : 10.068

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch86

calib_packv5_041523_1651.root, FC#0, port C2

Entries	447
Mean	38.66
Std Dev	17.59

Turn on : 25.3239

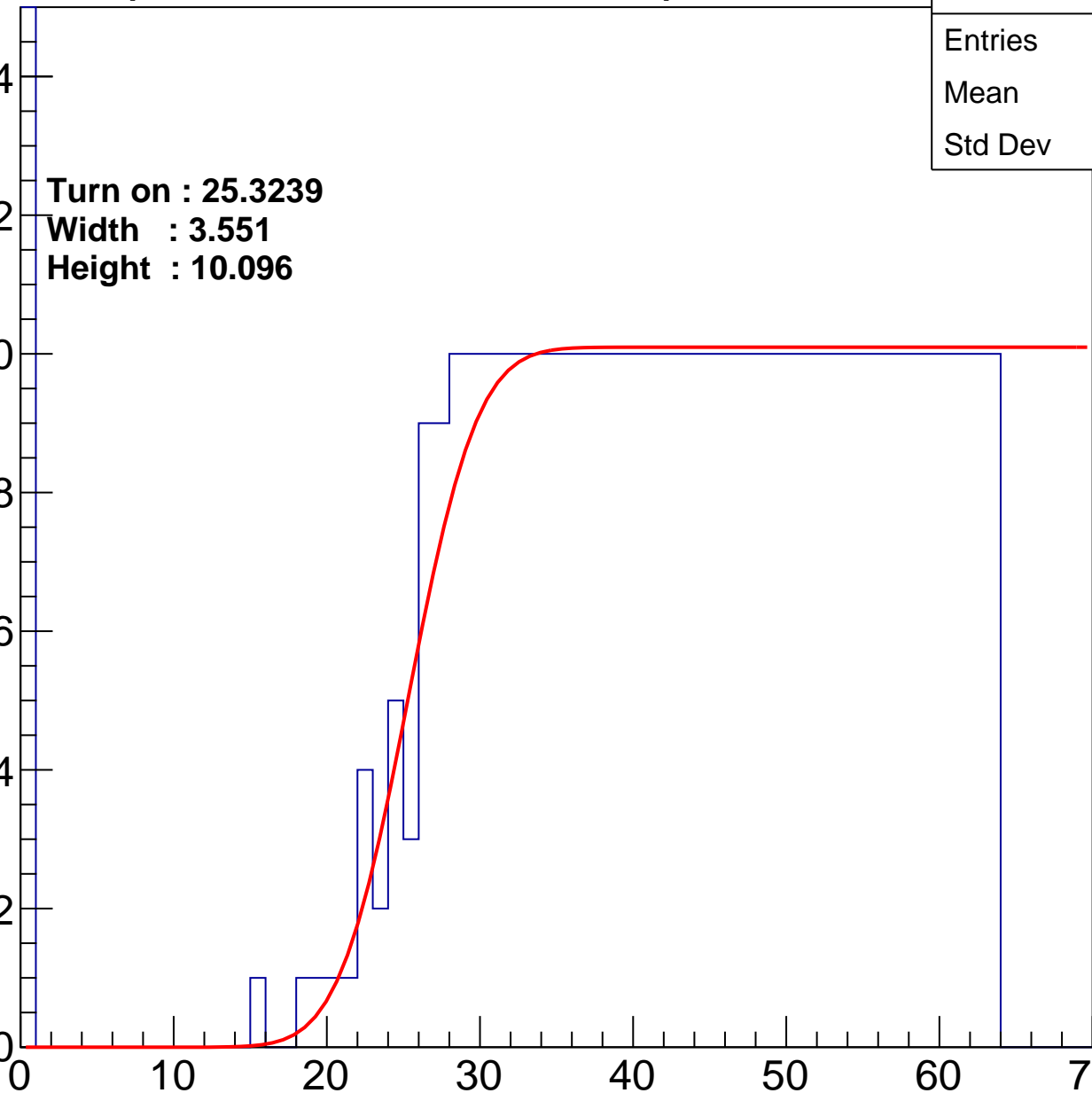
Width : 3.551

Height : 10.096

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch87

calib_packv5_041523_1651.root, FC#0, port C2

Entries	438
Mean	38.87
Std Dev	17.74

Turn on : 25.8419

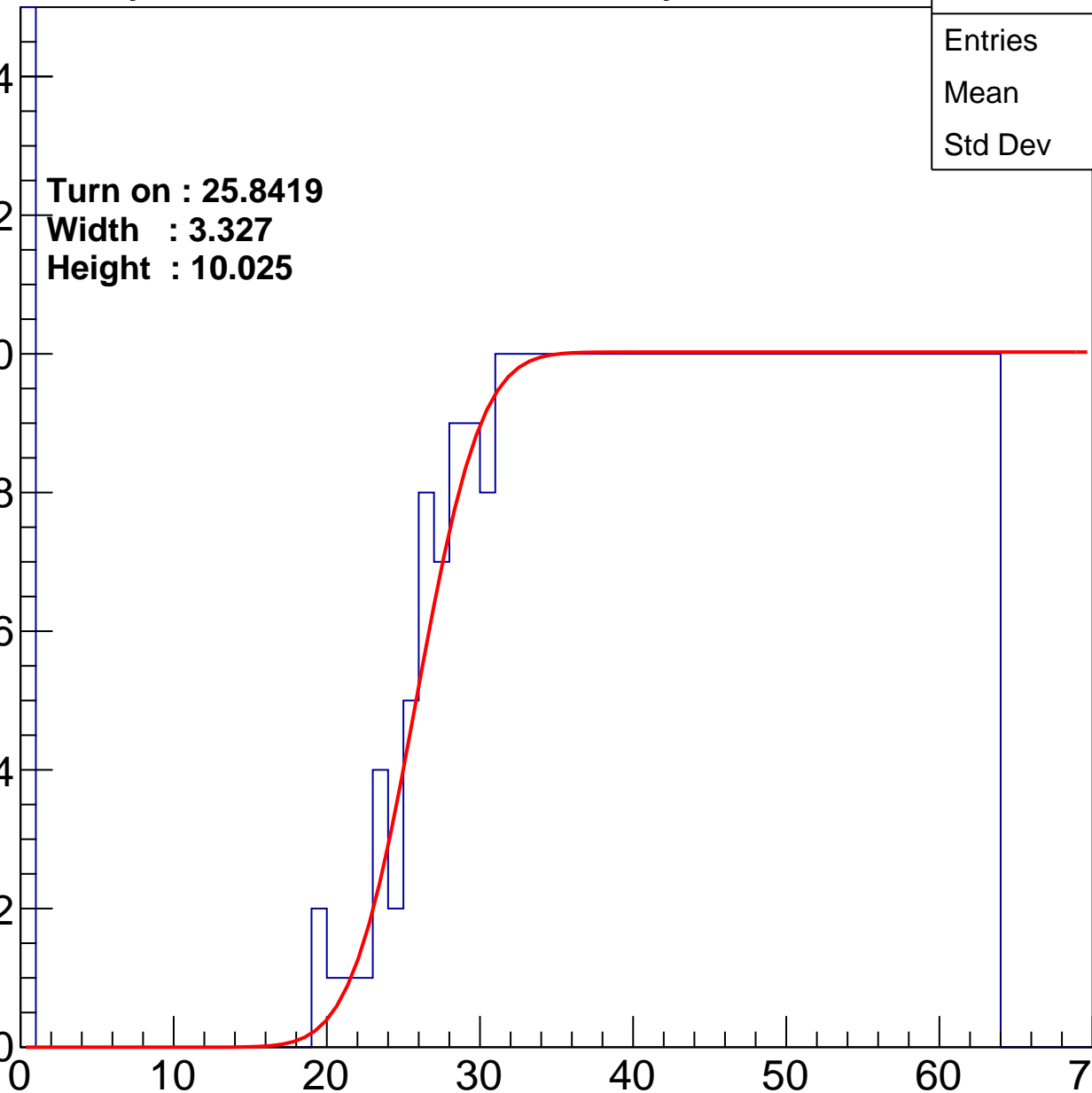
Width : 3.327

Height : 10.025

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch88

calib_packv5_041523_1651.root, FC#0, port C2

Entries	449
Mean	38.54
Std Dev	17.69

Turn on : 24.3612

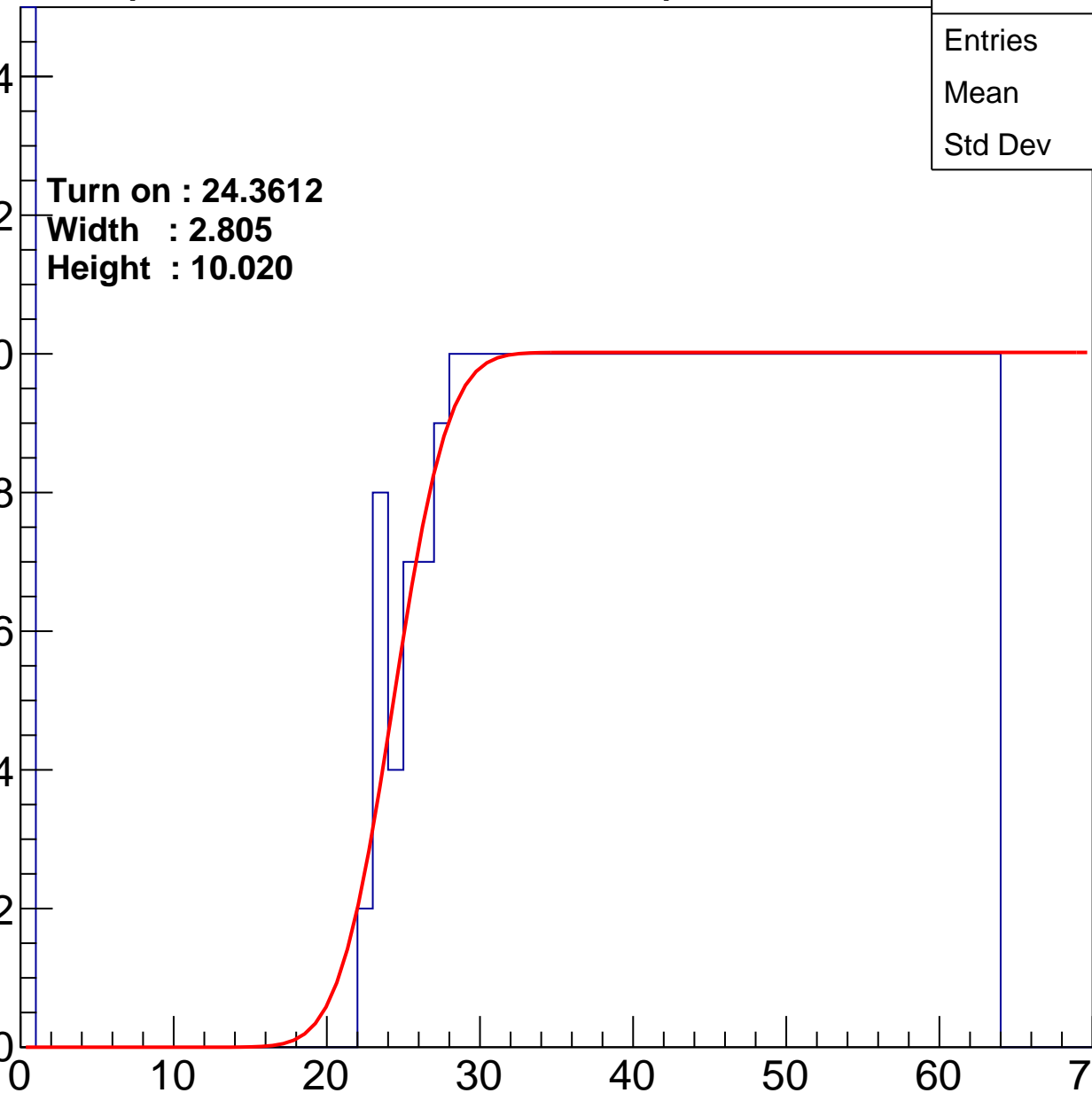
Width : 2.805

Height : 10.020

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch89

calib_packv5_041523_1651.root, FC#0, port C2

Entries	436
Mean	38.77
Std Dev	18.01

Turn on : 27.2099

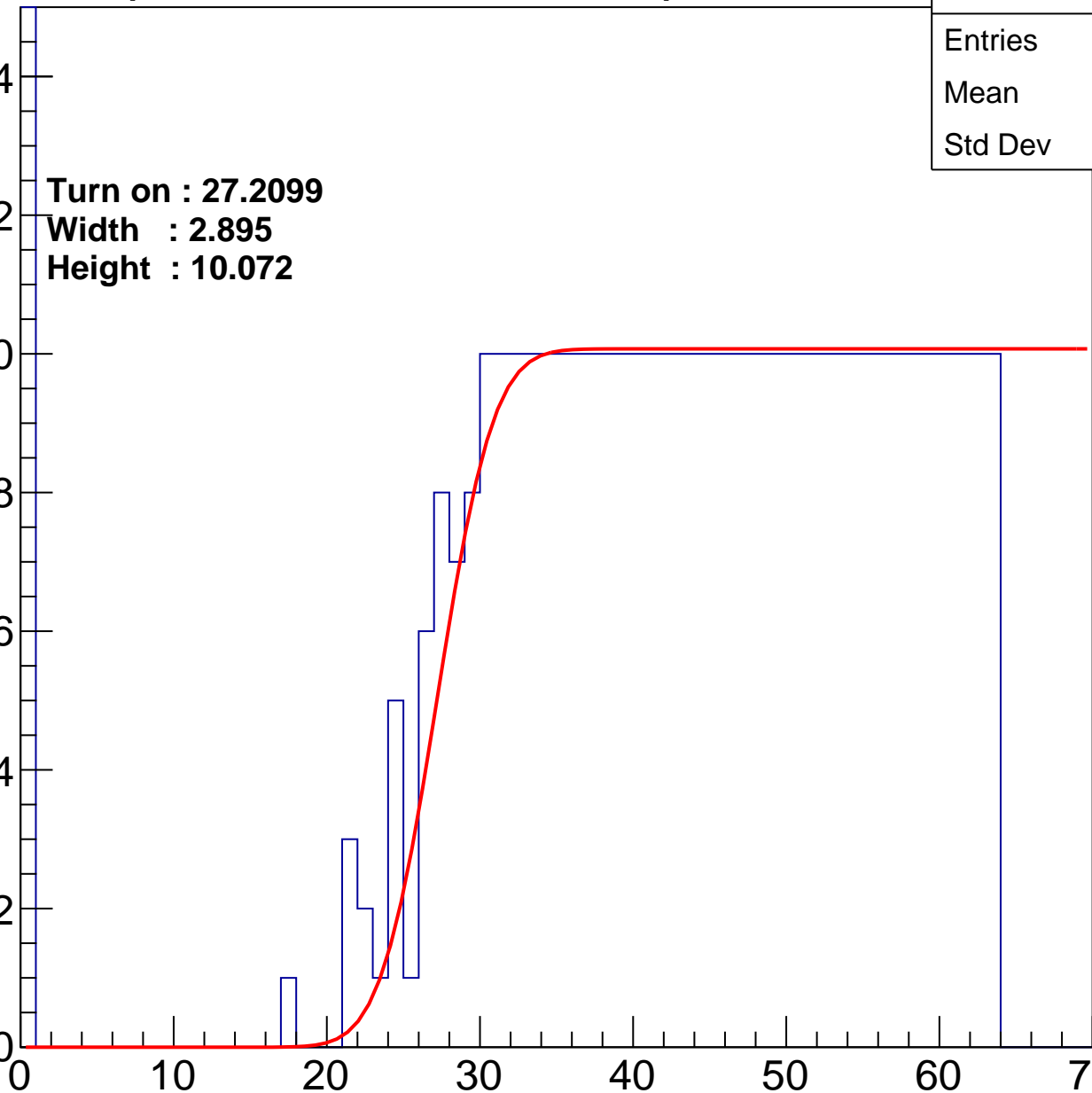
Width : 2.895

Height : 10.072

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch90

calib_packv5_041523_1651.root, FC#0, port C2

Entries	456
Mean	37.89
Std Dev	18.25

Turn on : 24.5903

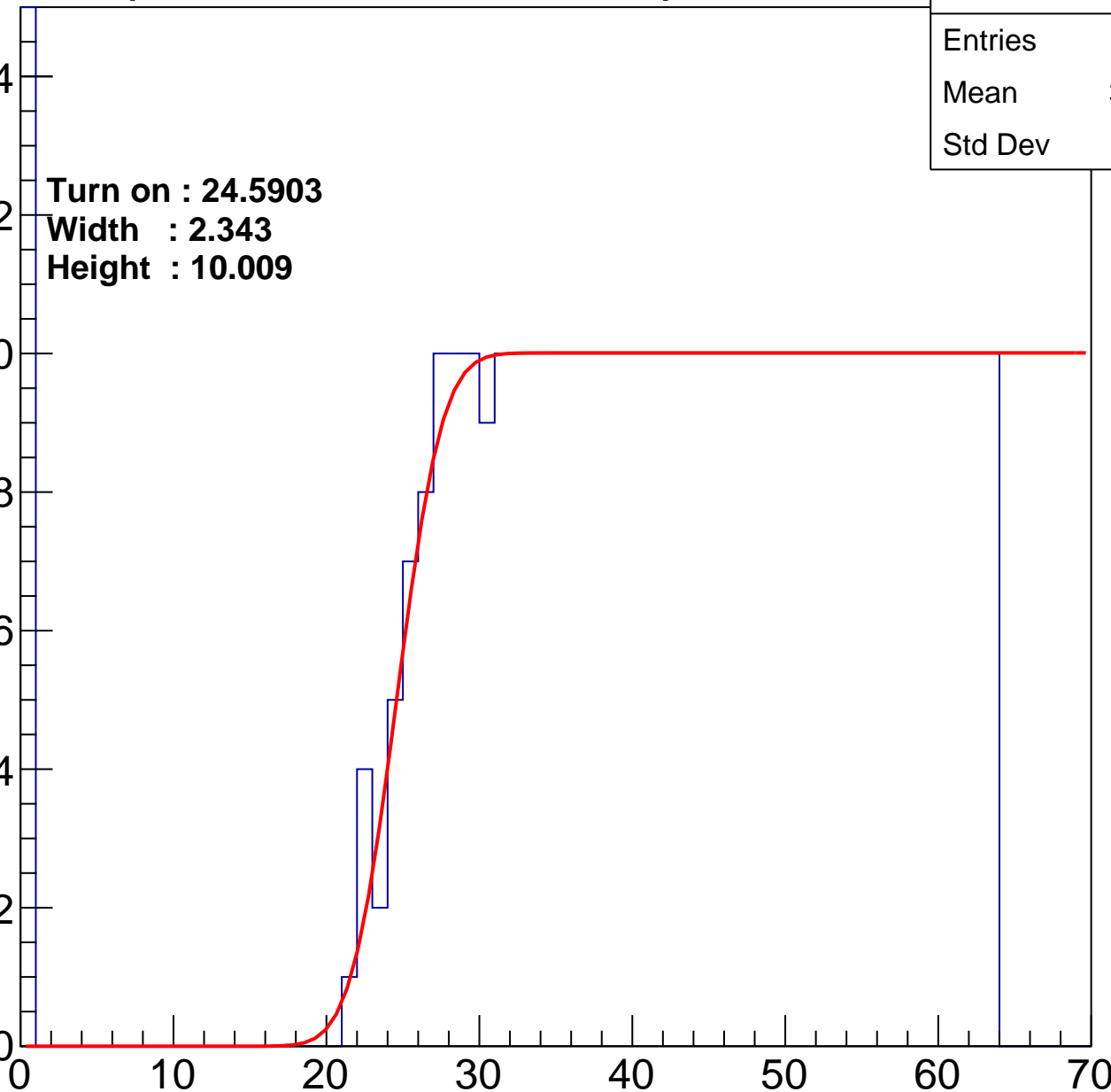
Width : 2.343

Height : 10.009

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch91

calib_packv5_041523_1651.root, FC#0, port C2

Entries	432
Mean	39.57
Std Dev	17.04

Turn on : 24.8826

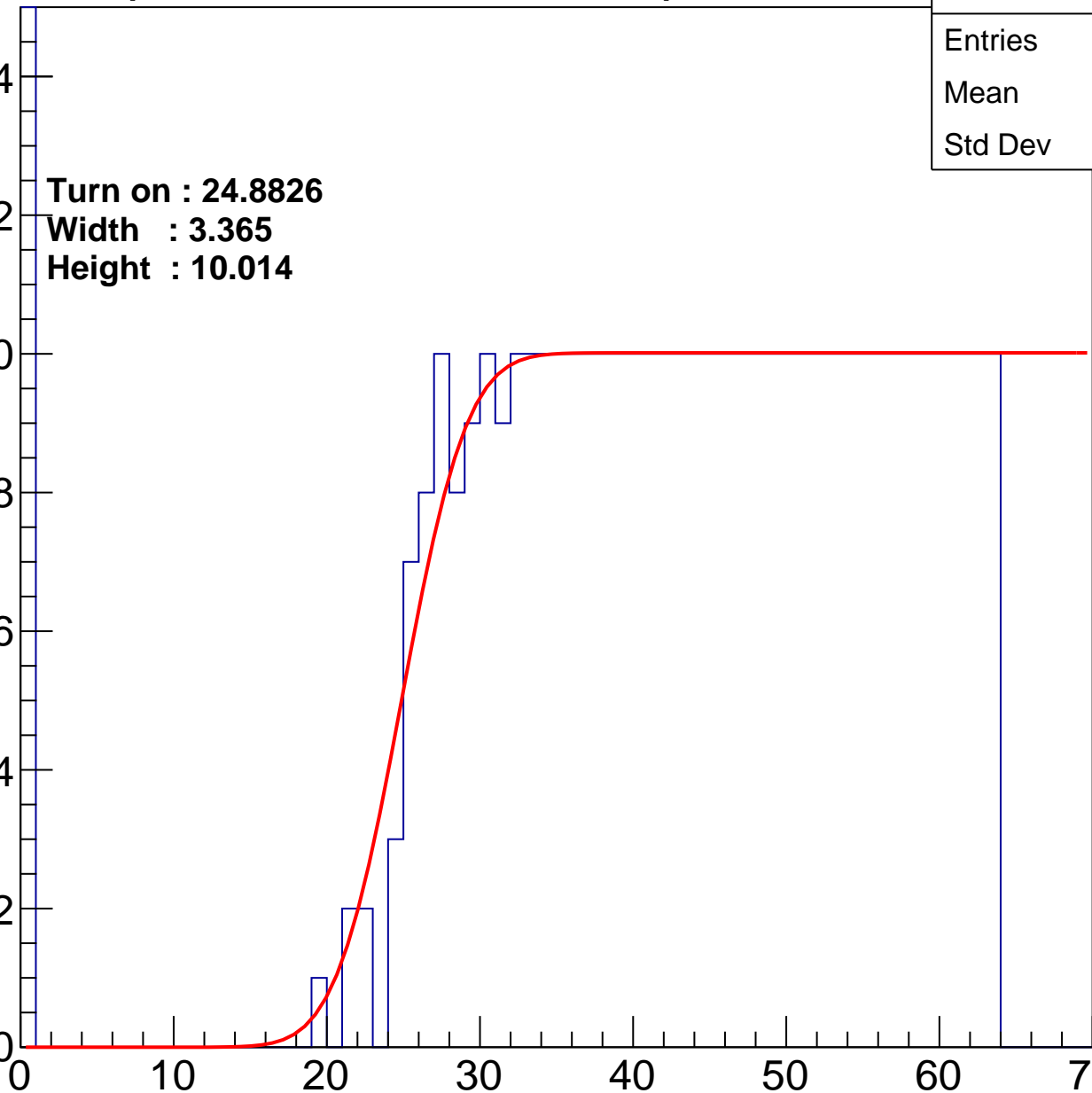
Width : 3.365

Height : 10.014

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch92

calib_packv5_041523_1651.root, FC#0, port C2

Entries	502
Mean	35.19
Std Dev	19.71

Turn on : 22.8459

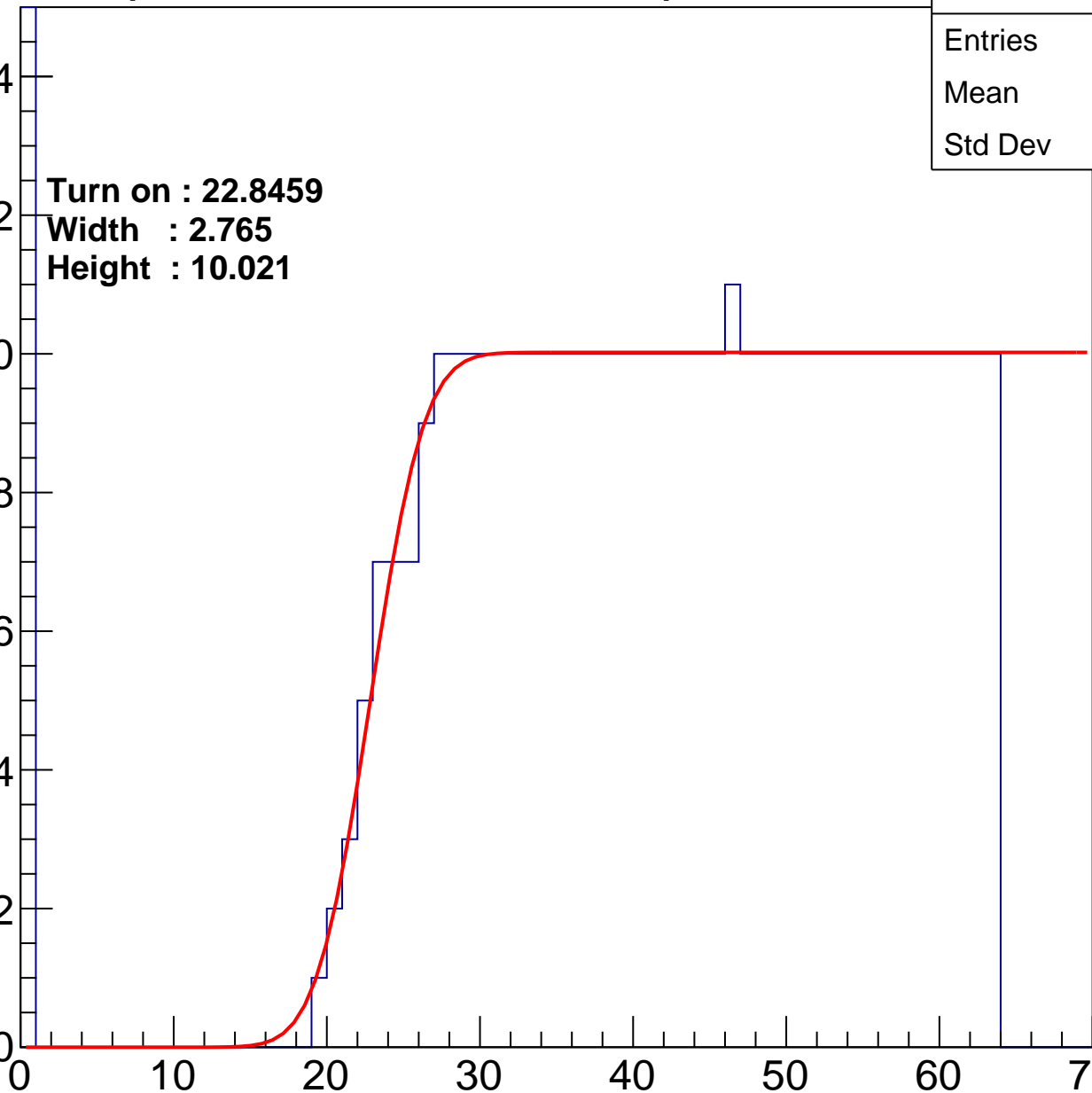
Width : 2.765

Height : 10.021

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch93

calib_packv5_041523_1651.root, FC#0, port C2

Entries	445
Mean	38.44
Std Dev	18

Turn on : 25.1613

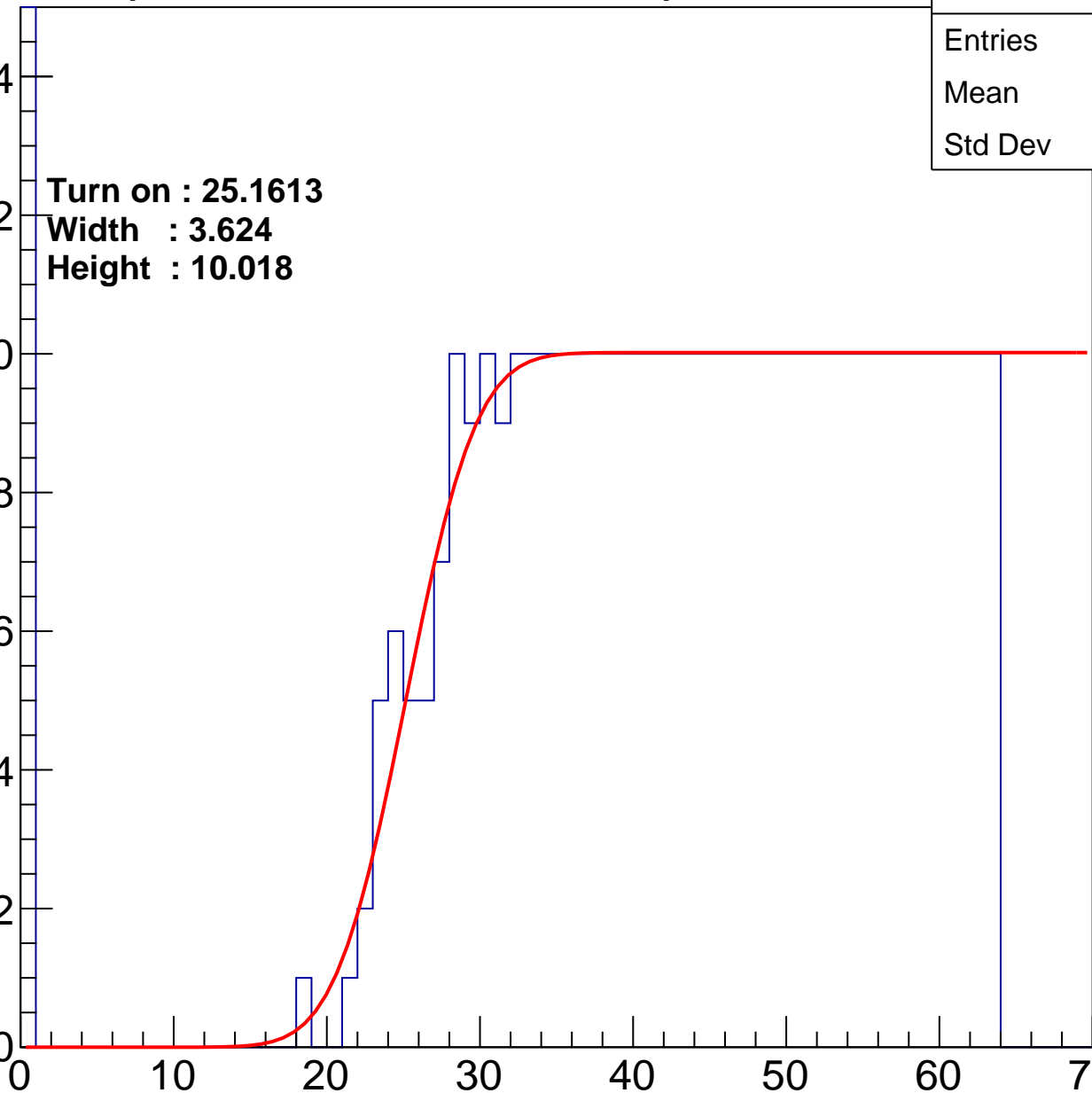
Width : 3.624

Height : 10.018

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch94

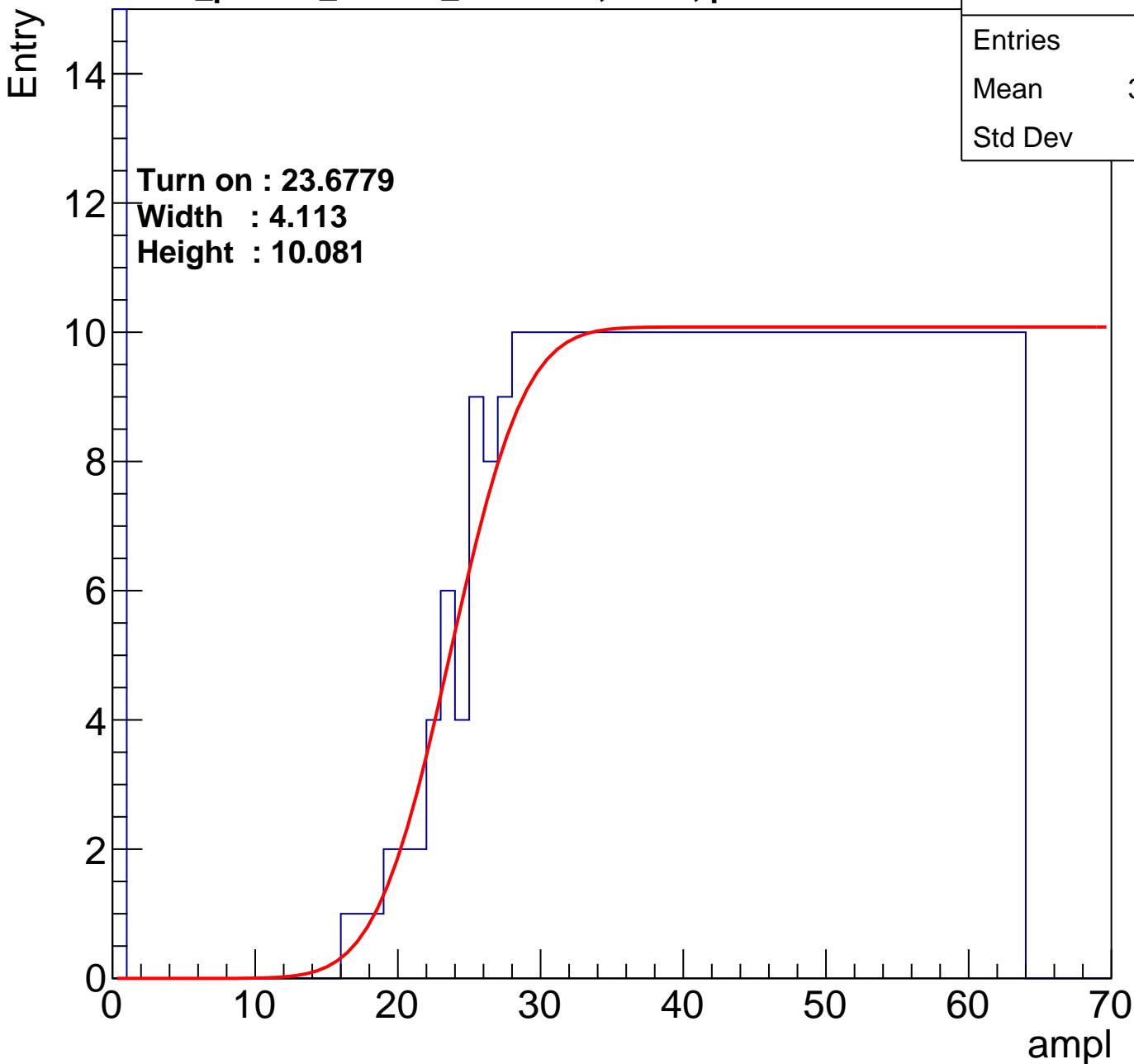
calib_packv5_041523_1651.root, FC#0, port C2

Entries	464
Mean	37.82
Std Dev	17.9

Turn on : 23.6779

Width : 4.113

Height : 10.081



B1L103S, U23-ch95

calib_packv5_041523_1651.root, FC#0, port C2

Entries	435
Mean	39.19
Std Dev	17.42

Turn on : 25.2249

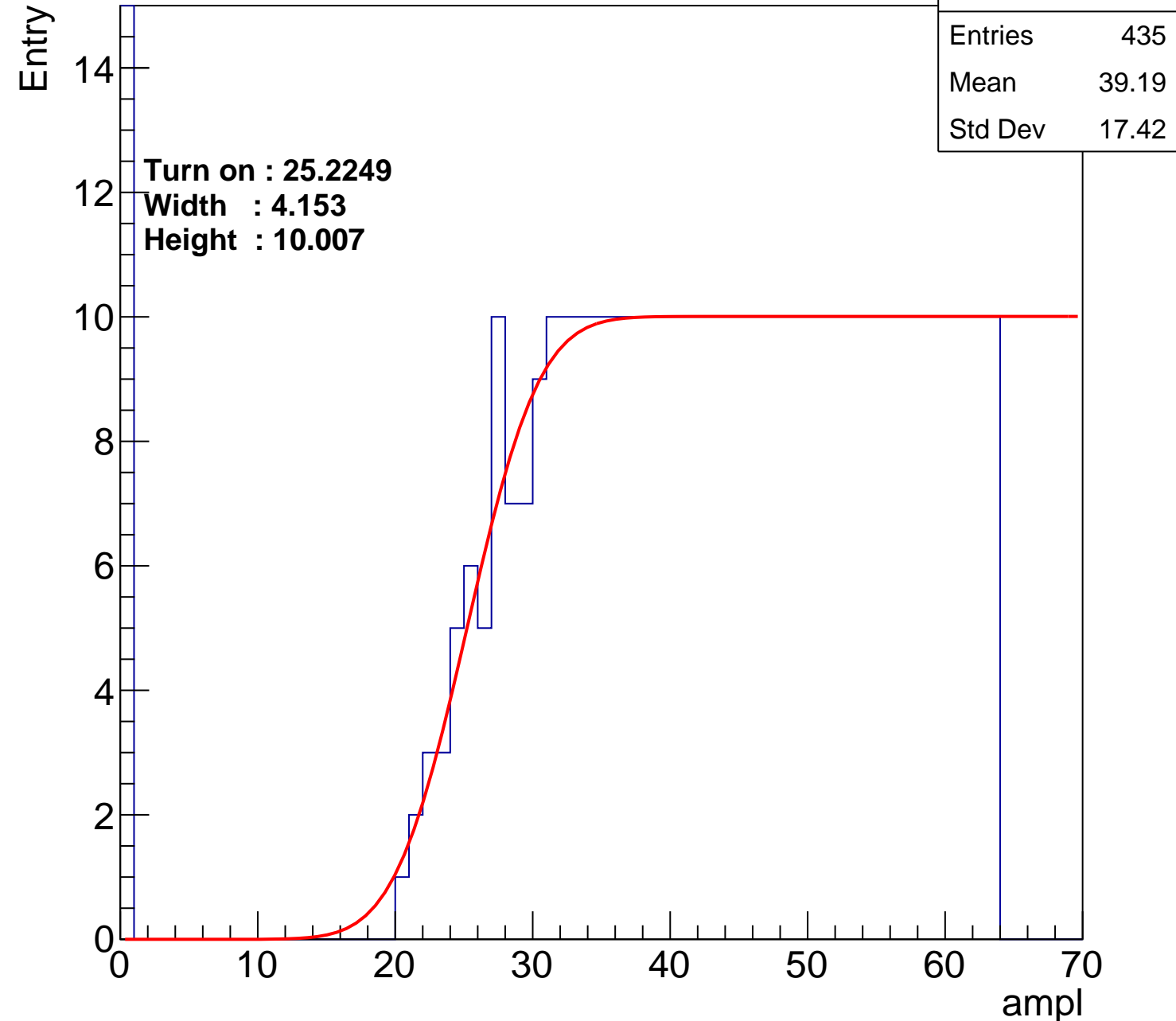
Width : 4.153

Height : 10.007

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch96

calib_packv5_041523_1651.root, FC#0, port C2

Entries	457
Mean	37.41
Std Dev	18.84

Turn on : 24.9563

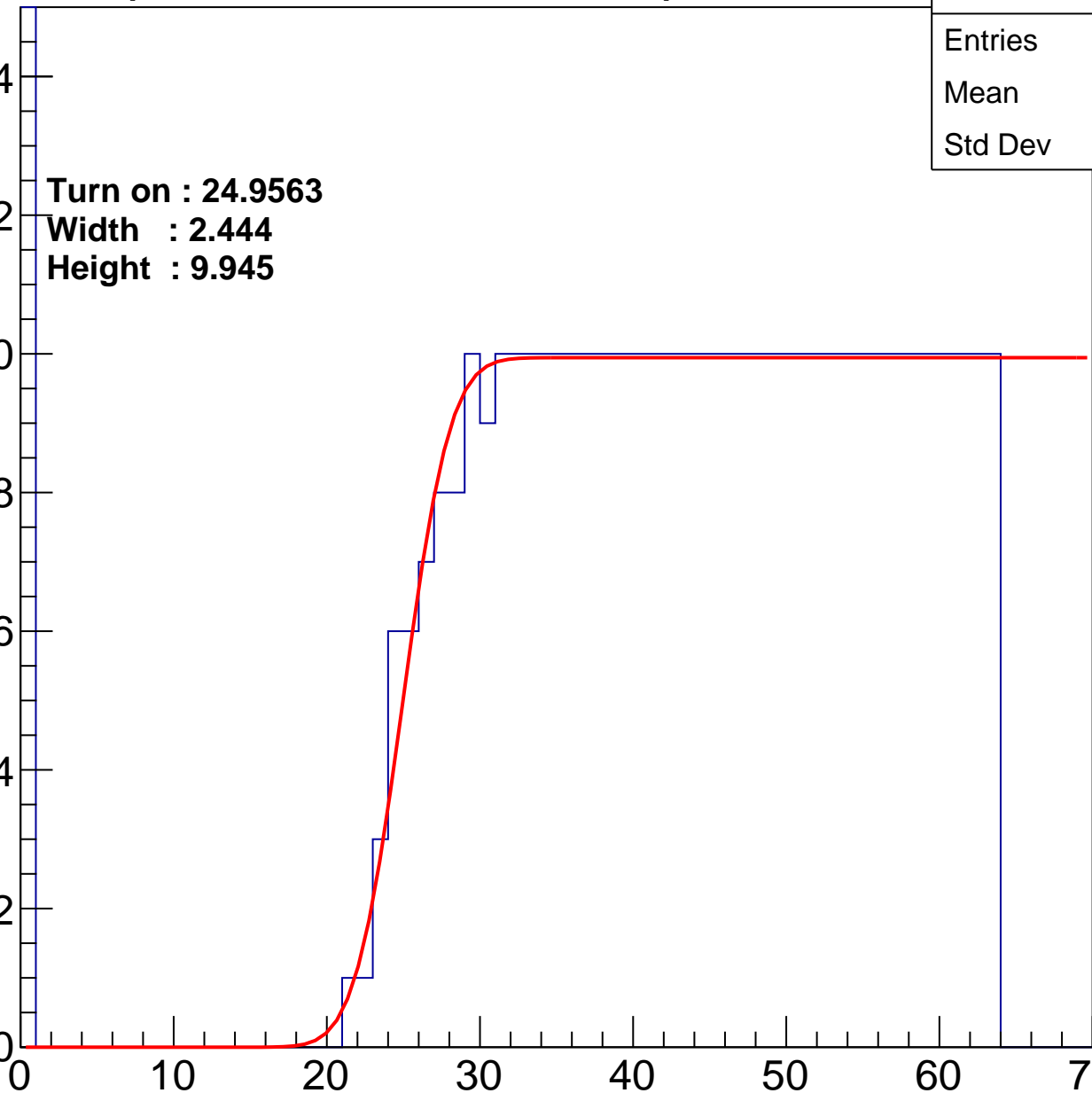
Width : 2.444

Height : 9.945

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch97

calib_packv5_041523_1651.root, FC#0, port C2

Entries	442
Mean	38.74
Std Dev	17.72

Turn on : 25.8237

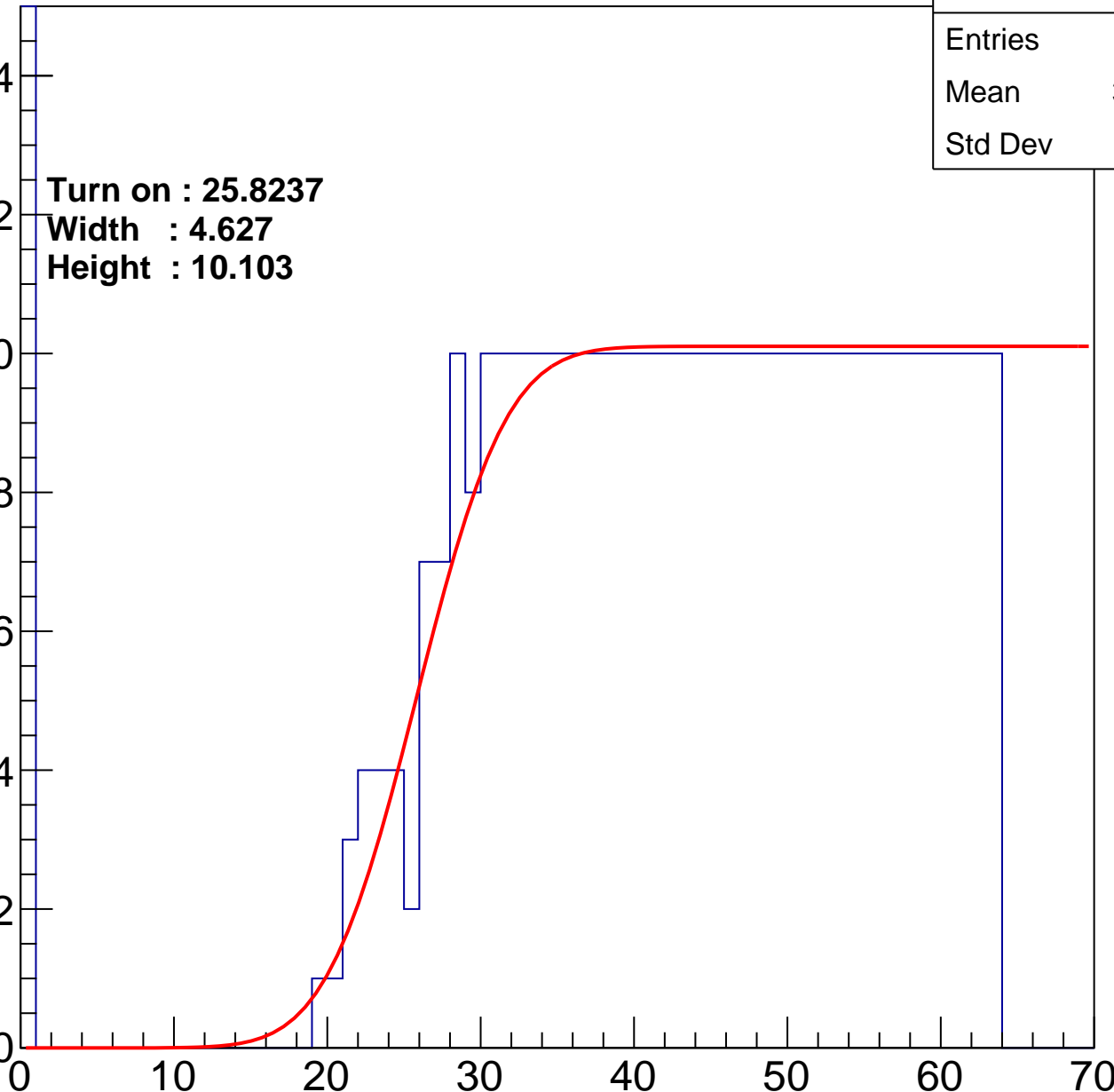
Width : 4.627

Height : 10.103

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch98

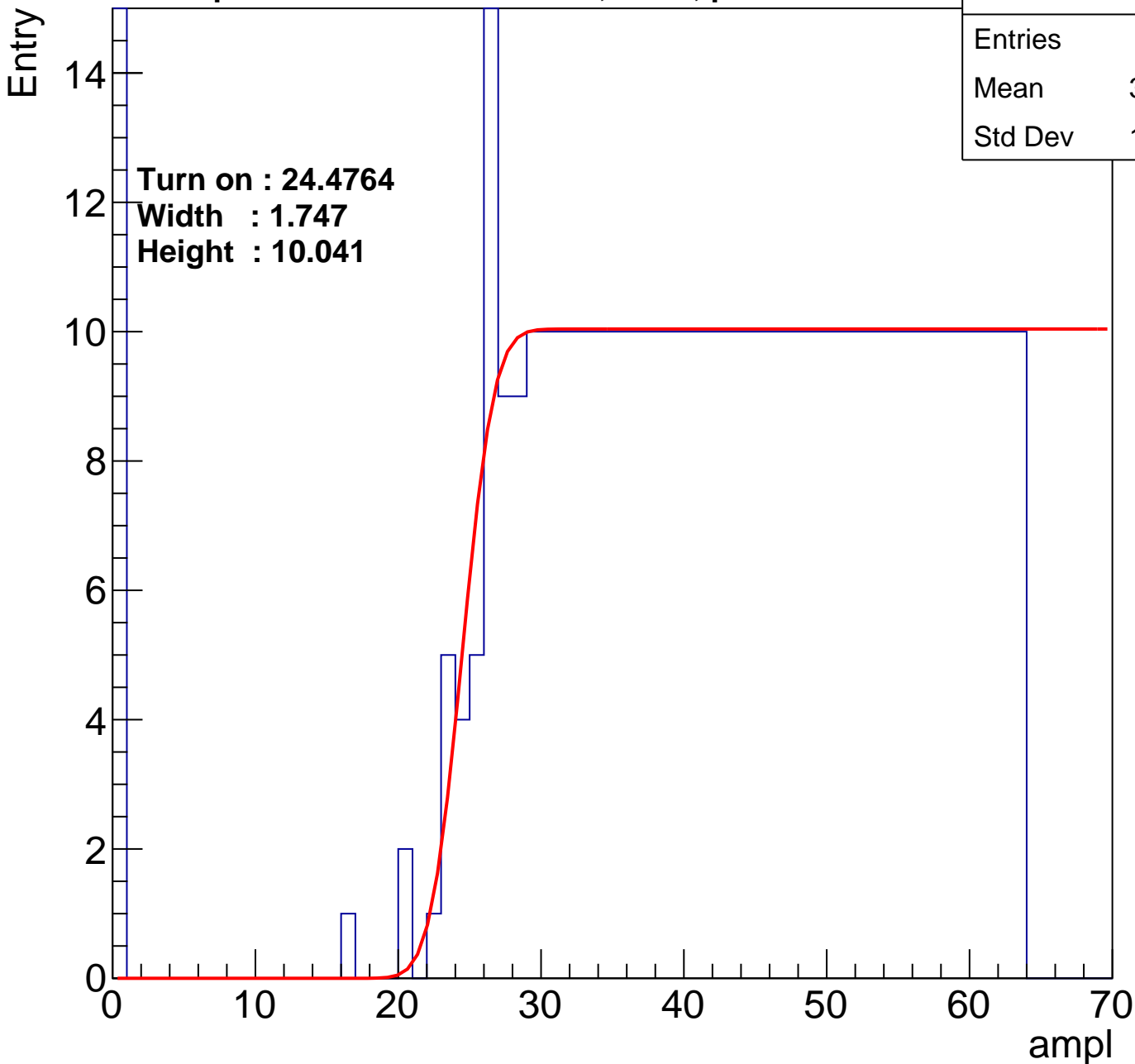
calib_packv5_041523_1651.root, FC#0, port C2

Entries	484
Mean	37.18
Std Dev	17.95

Turn on : 24.4764

Width : 1.747

Height : 10.041



B1L103S, U23-ch99

calib_packv5_041523_1651.root, FC#0, port C2

Entries	461
Mean	37.47
Std Dev	18.59

Turn on : 24.6275

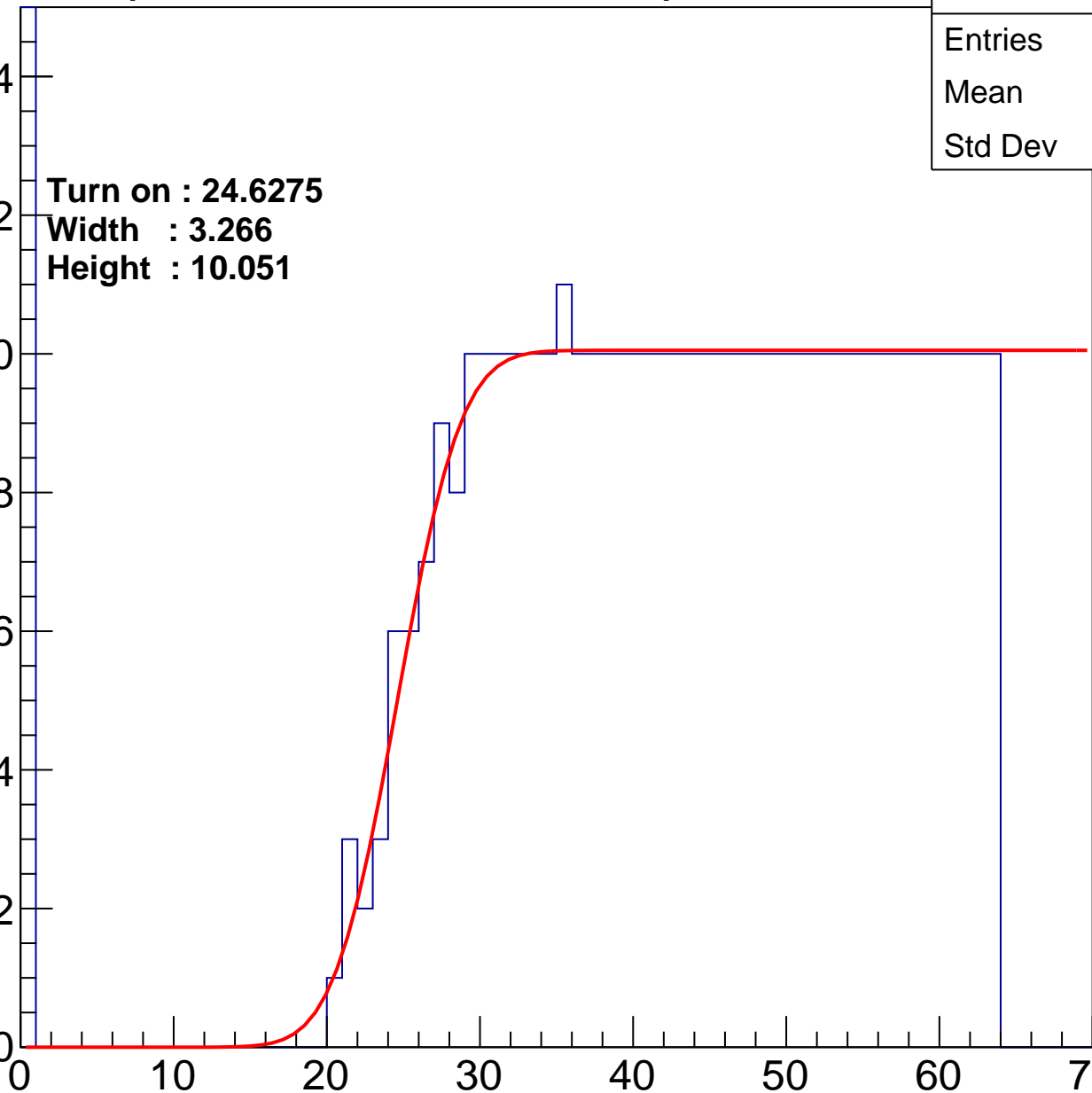
Width : 3.266

Height : 10.051

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch100

calib_packv5_041523_1651.root, FC#0, port C2

Entries	460
Mean	37.89
Std Dev	18

Turn on : 24.1648

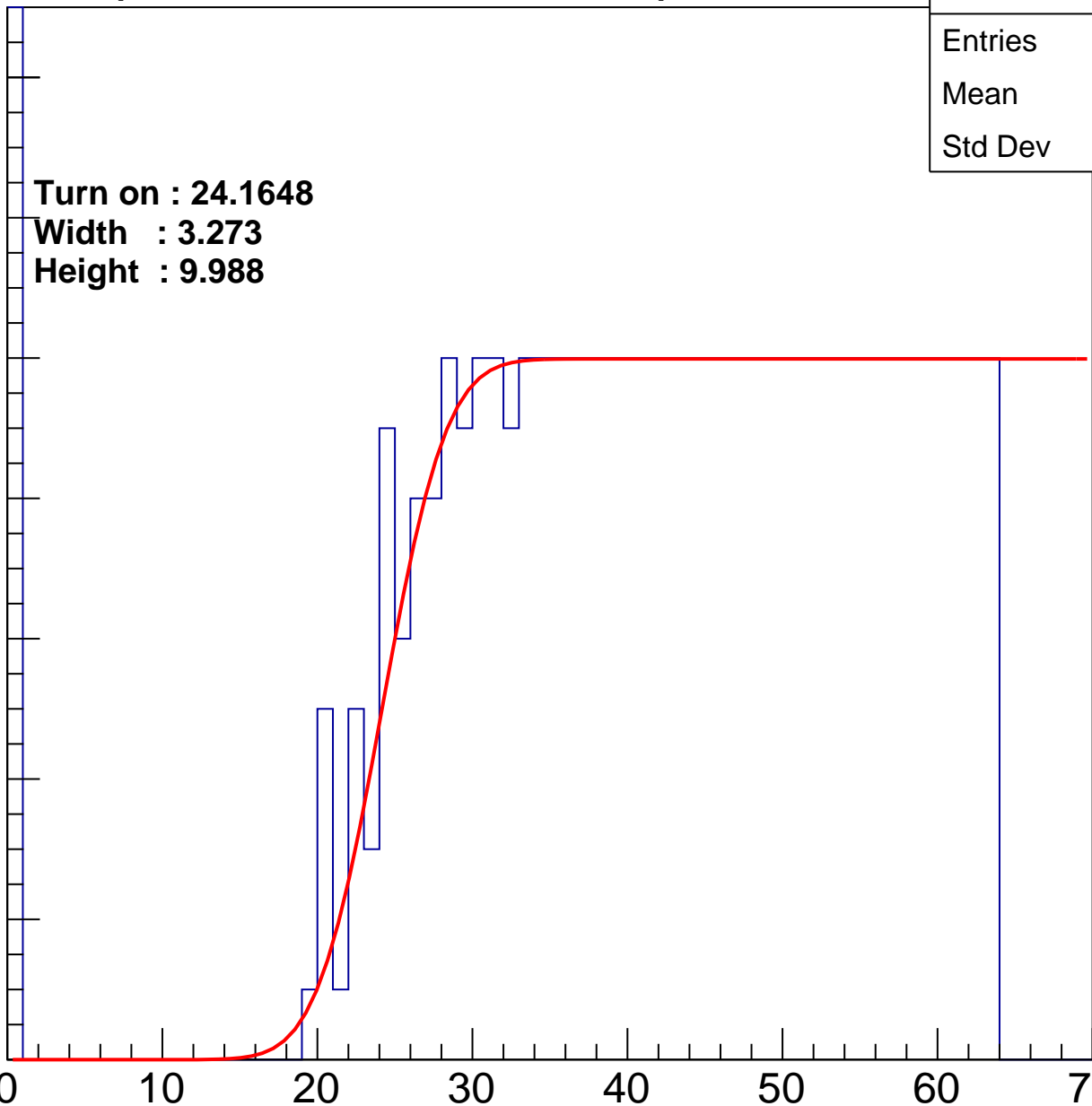
Width : 3.273

Height : 9.988

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch101

calib_packv5_041523_1651.root, FC#0, port C2

Entries	446
Mean	37.48
Std Dev	19.28

Turn on : 26.8704

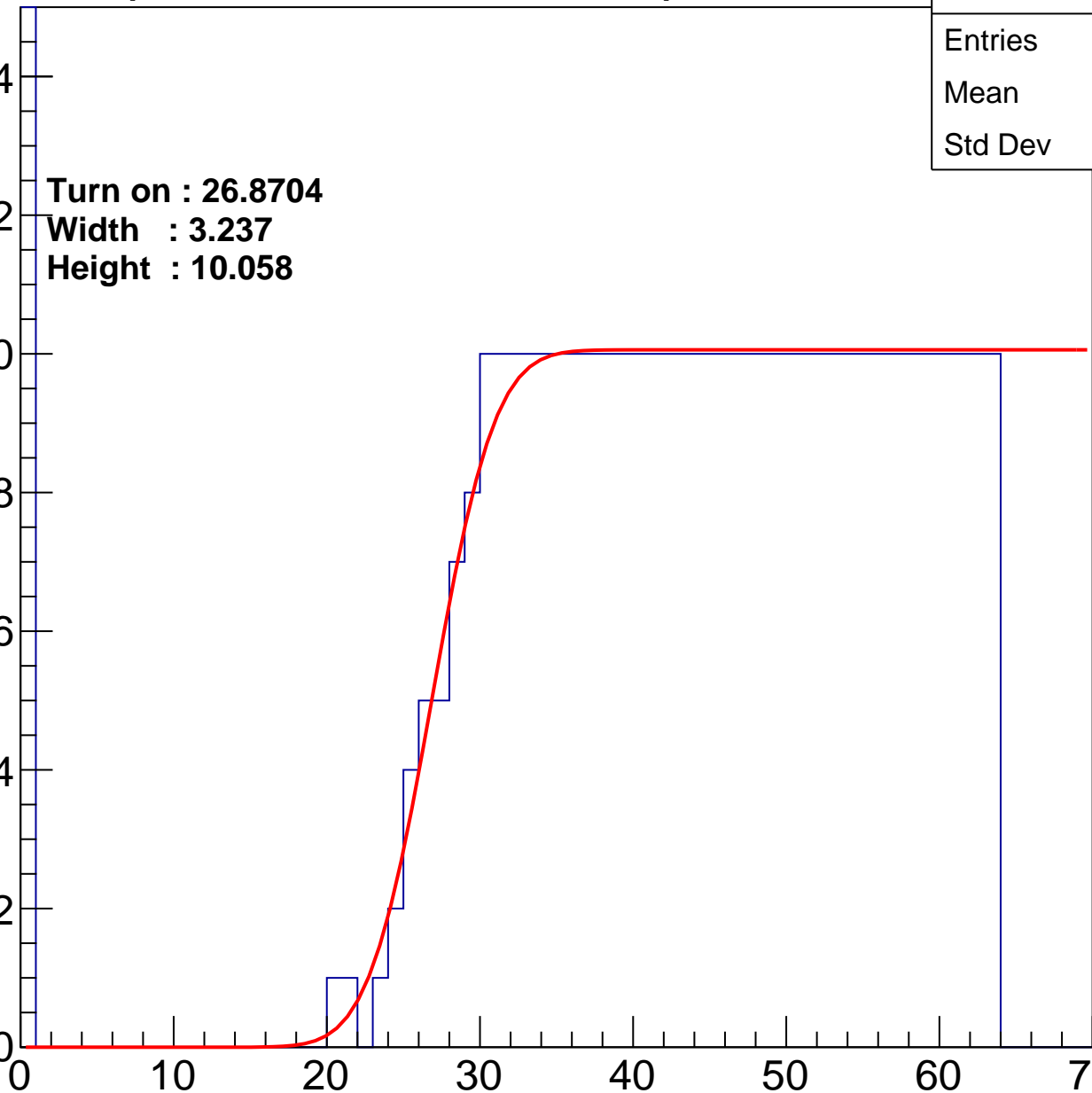
Width : 3.237

Height : 10.058

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch102

calib_packv5_041523_1651.root, FC#0, port C2

Entries	444
Mean	39.28
Std Dev	16.81

Turn on : 24.2511

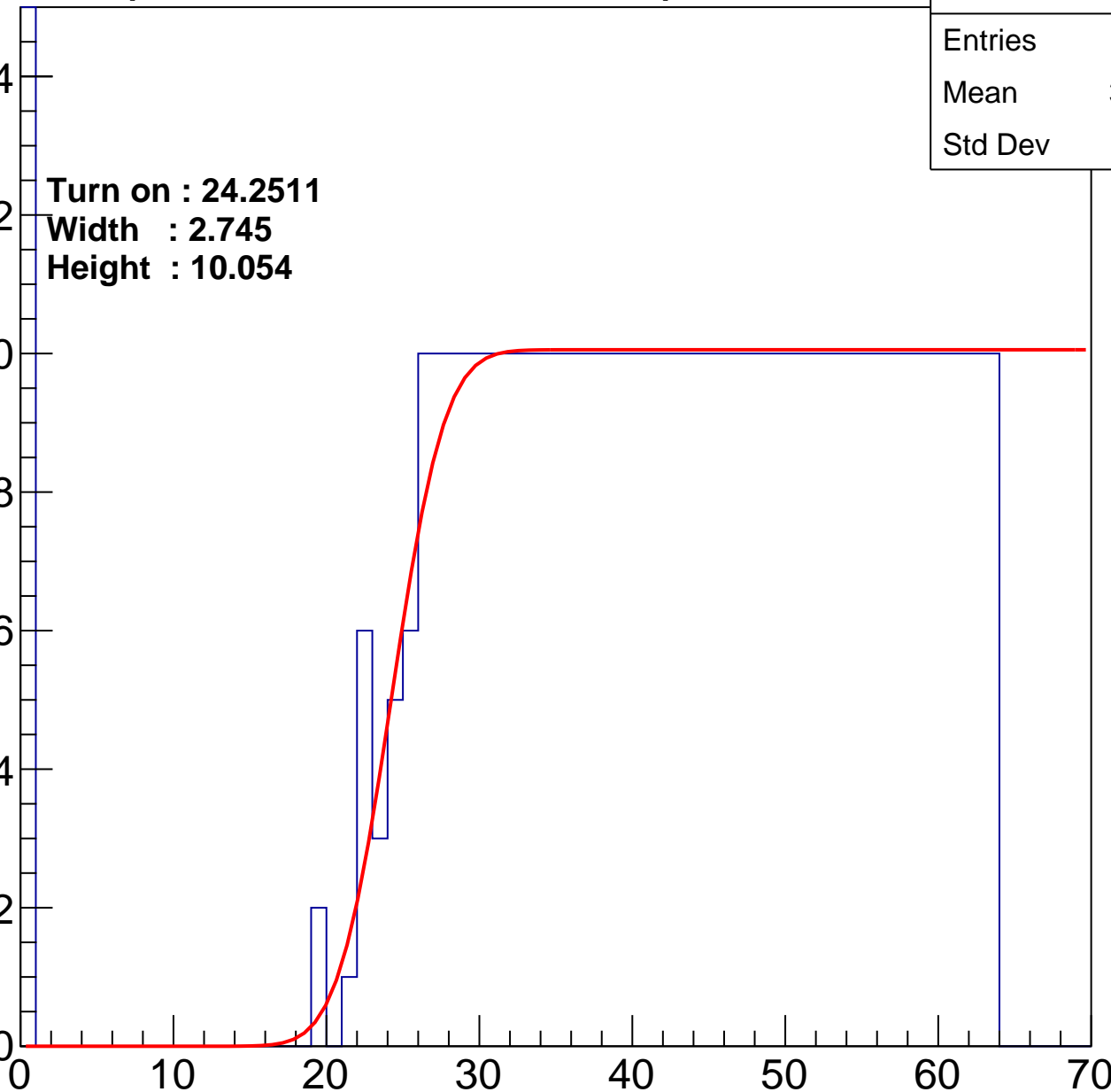
Width : 2.745

Height : 10.054

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch103

calib_packv5_041523_1651.root, FC#0, port C2

Entries	432
Mean	38.88
Std Dev	18.09

Turn on : 26.3283

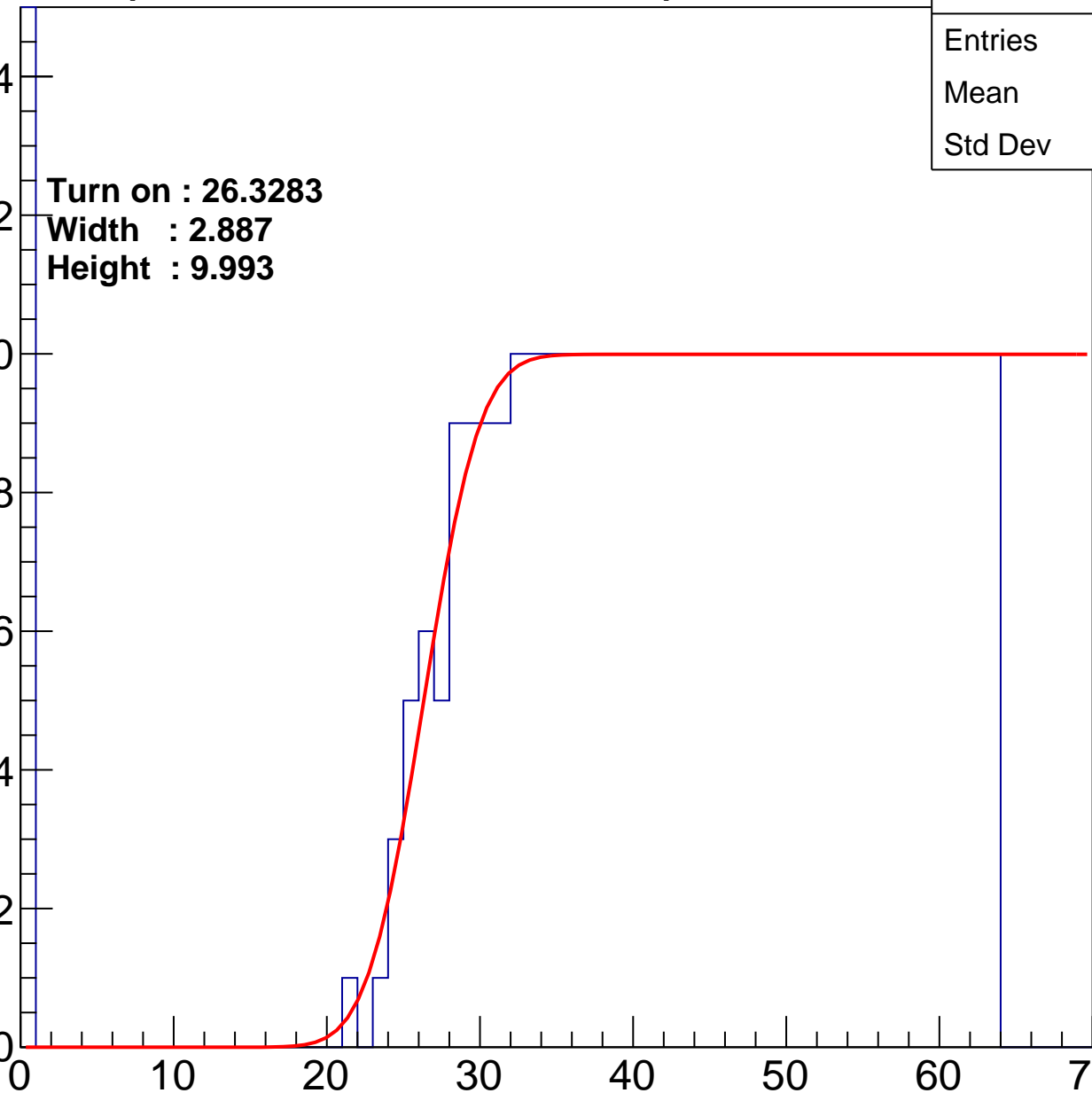
Width : 2.887

Height : 9.993

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch104

calib_packv5_041523_1651.root, FC#0, port C2

Entries	460
Mean	37.53
Std Dev	18.54

Turn on : 24.8282

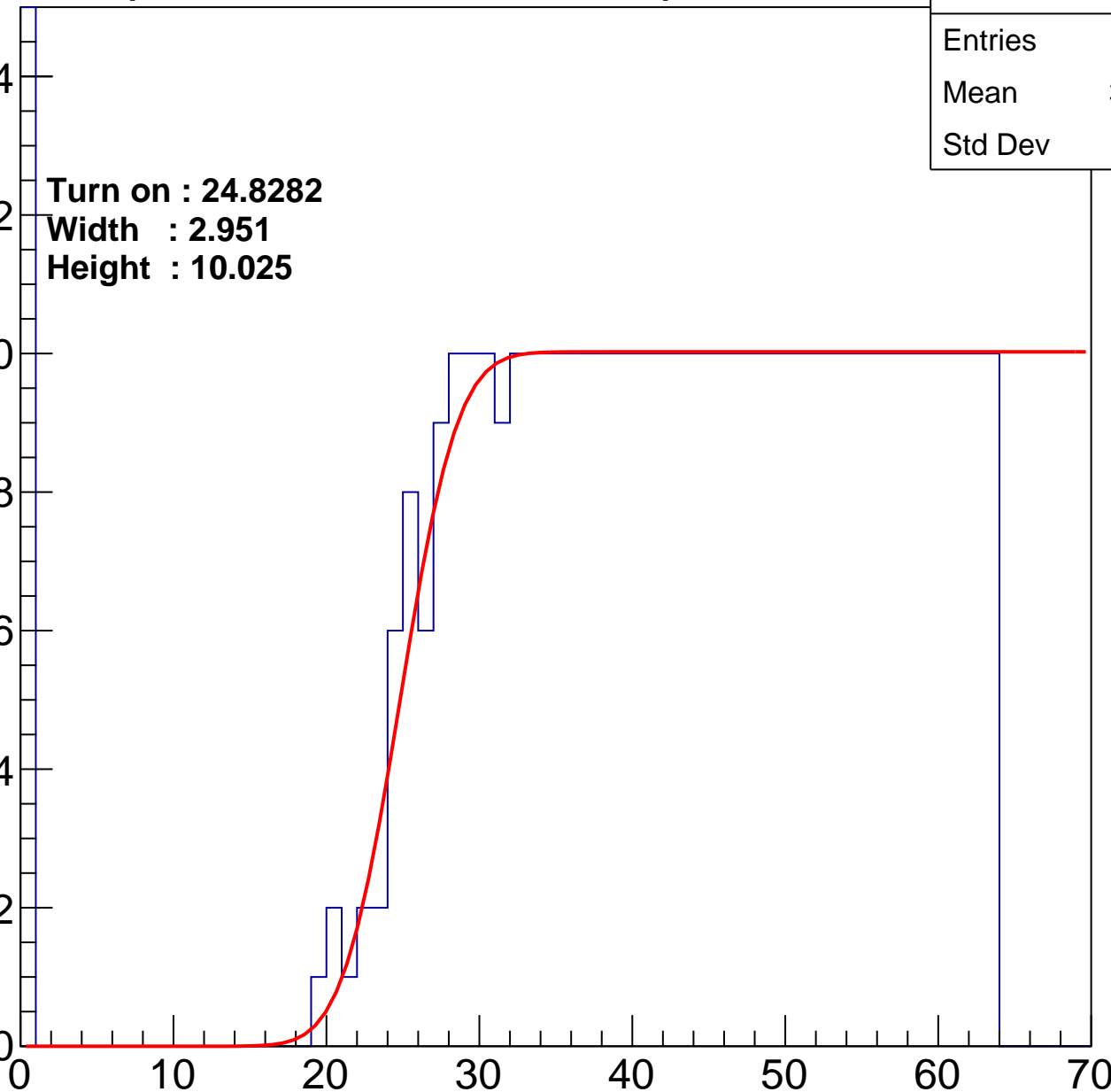
Width : 2.951

Height : 10.025

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch105

calib_packv5_041523_1651.root, FC#0, port C2

Entries	440
Mean	38.83
Std Dev	17.71

Turn on : 25.4191

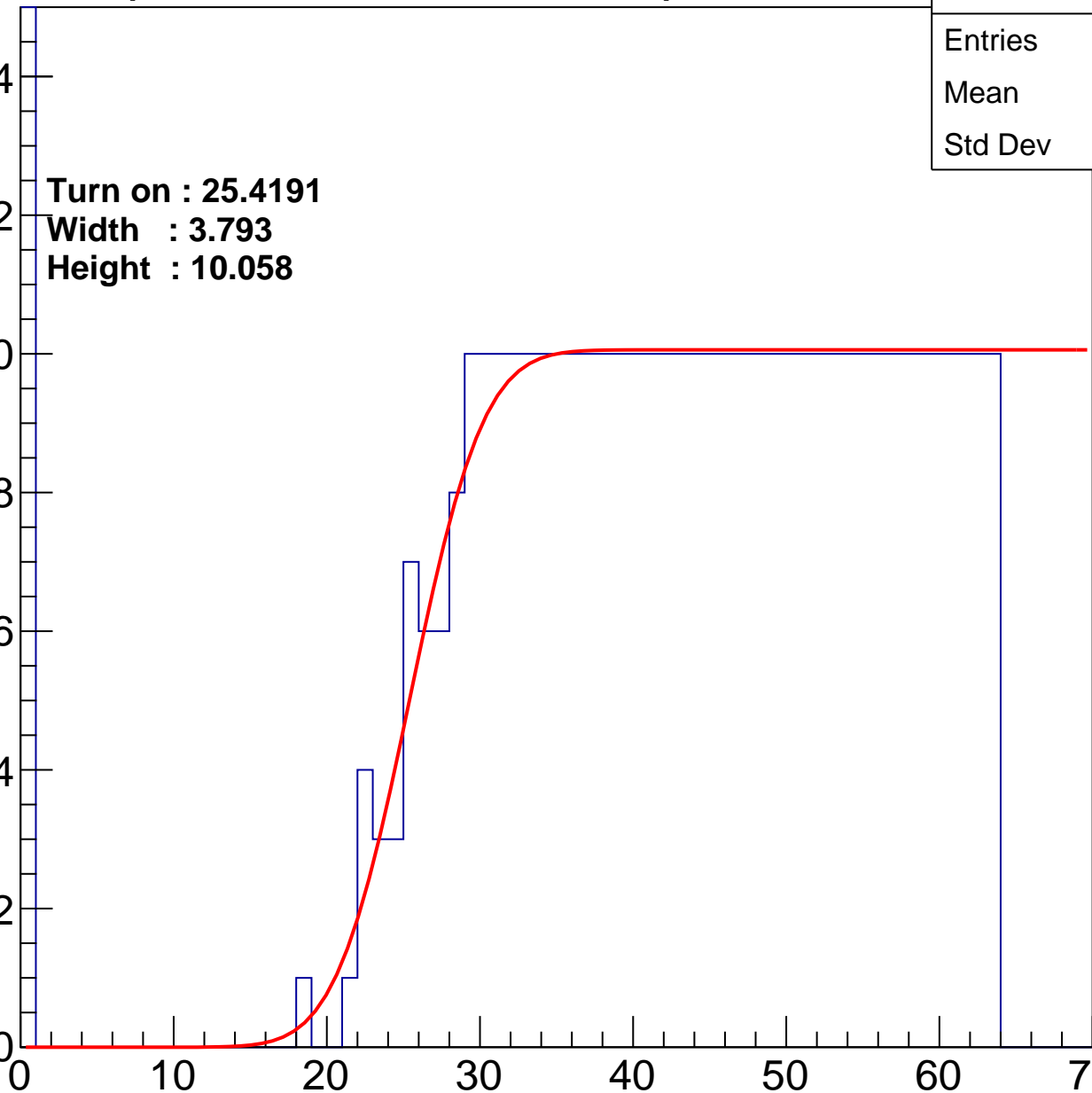
Width : 3.793

Height : 10.058

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch106

calib_packv5_041523_1651.root, FC#0, port C2

Entries	477
Mean	36.52
Std Dev	19.14

Turn on : 24.4102

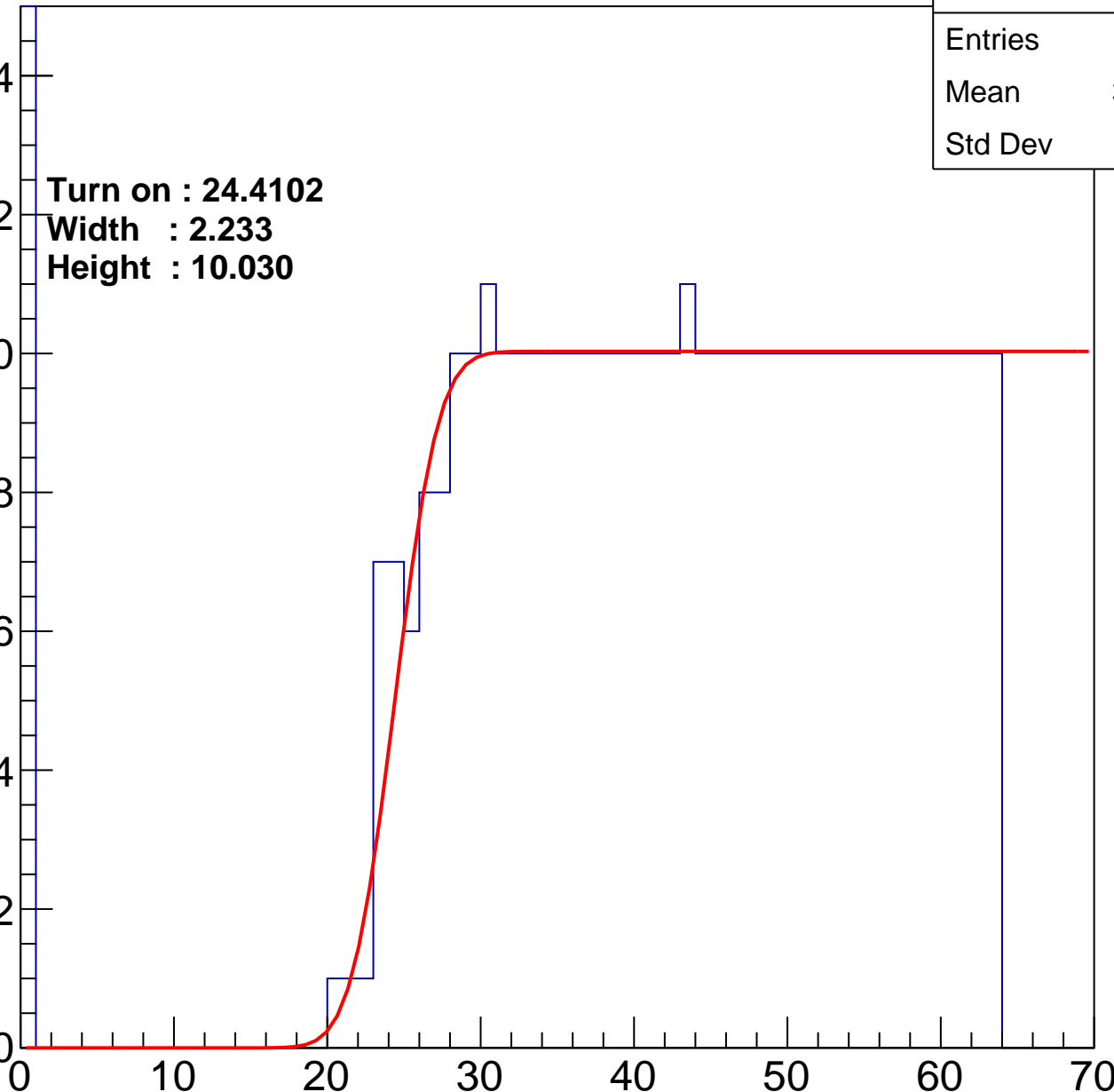
Width : 2.233

Height : 10.030

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch107

calib_packv5_041523_1651.root, FC#0, port C2

Entries	426
Mean	39.36
Std Dev	17.71

Turn on : 26.9643

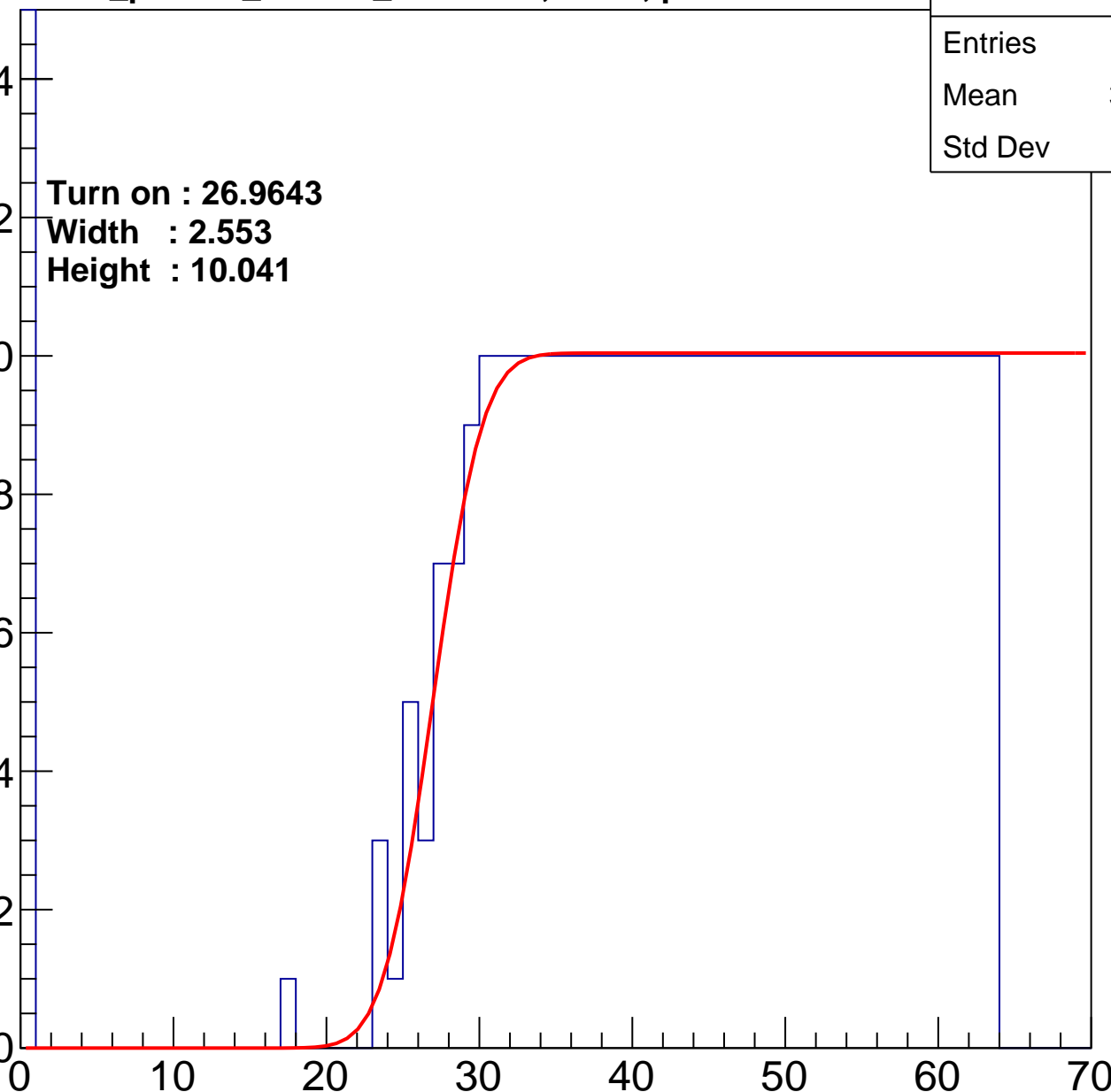
Width : 2.553

Height : 10.041

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch108

calib_packv5_041523_1651.root, FC#0, port C2

Entries	469
Mean	37.9
Std Dev	17.55

Turn on : 22.6597

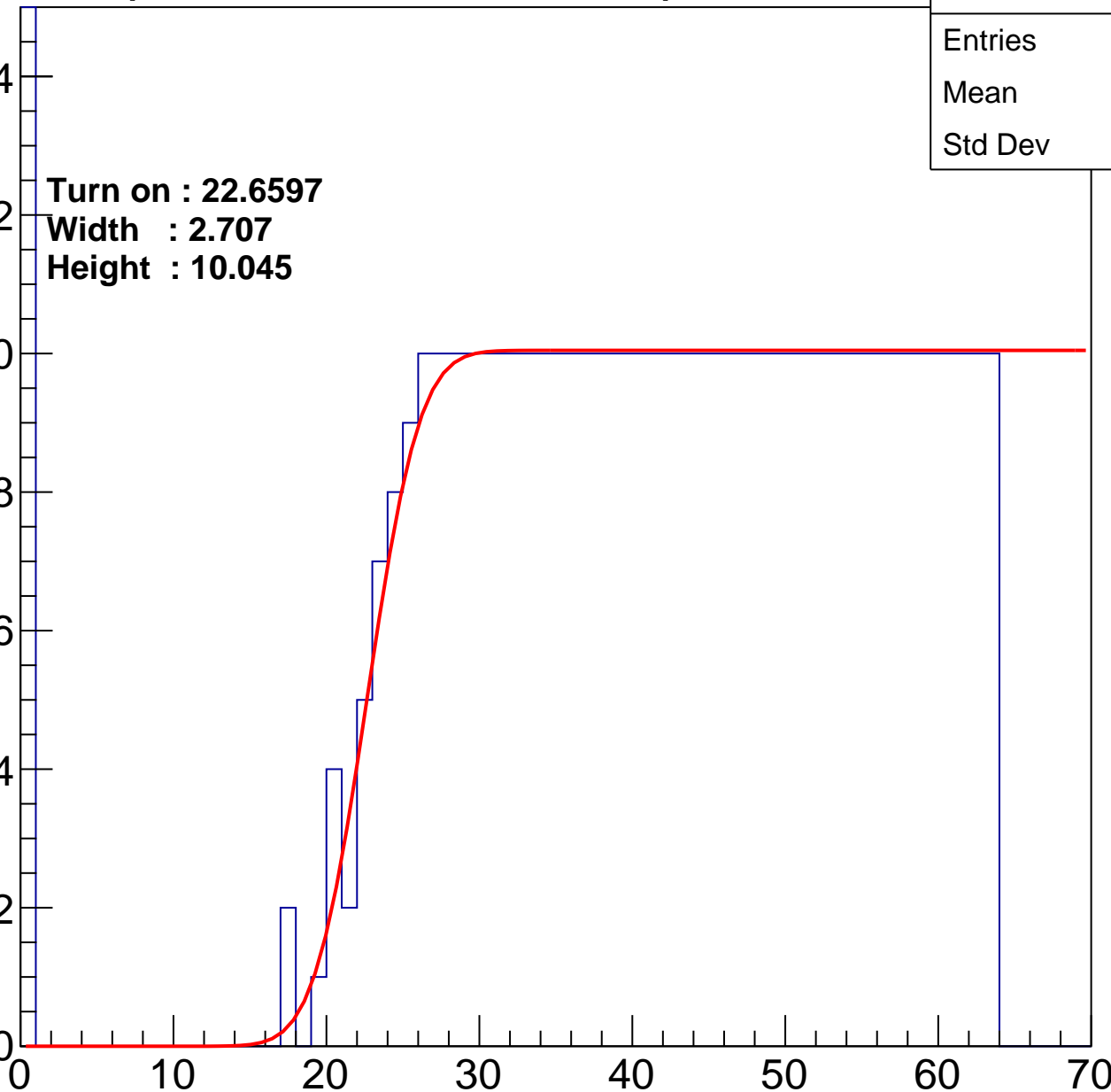
Width : 2.707

Height : 10.045

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch109

calib_packv5_041523_1651.root, FC#0, port C2

Entries	447
Mean	38.56
Std Dev	17.73

Turn on : 24.7822

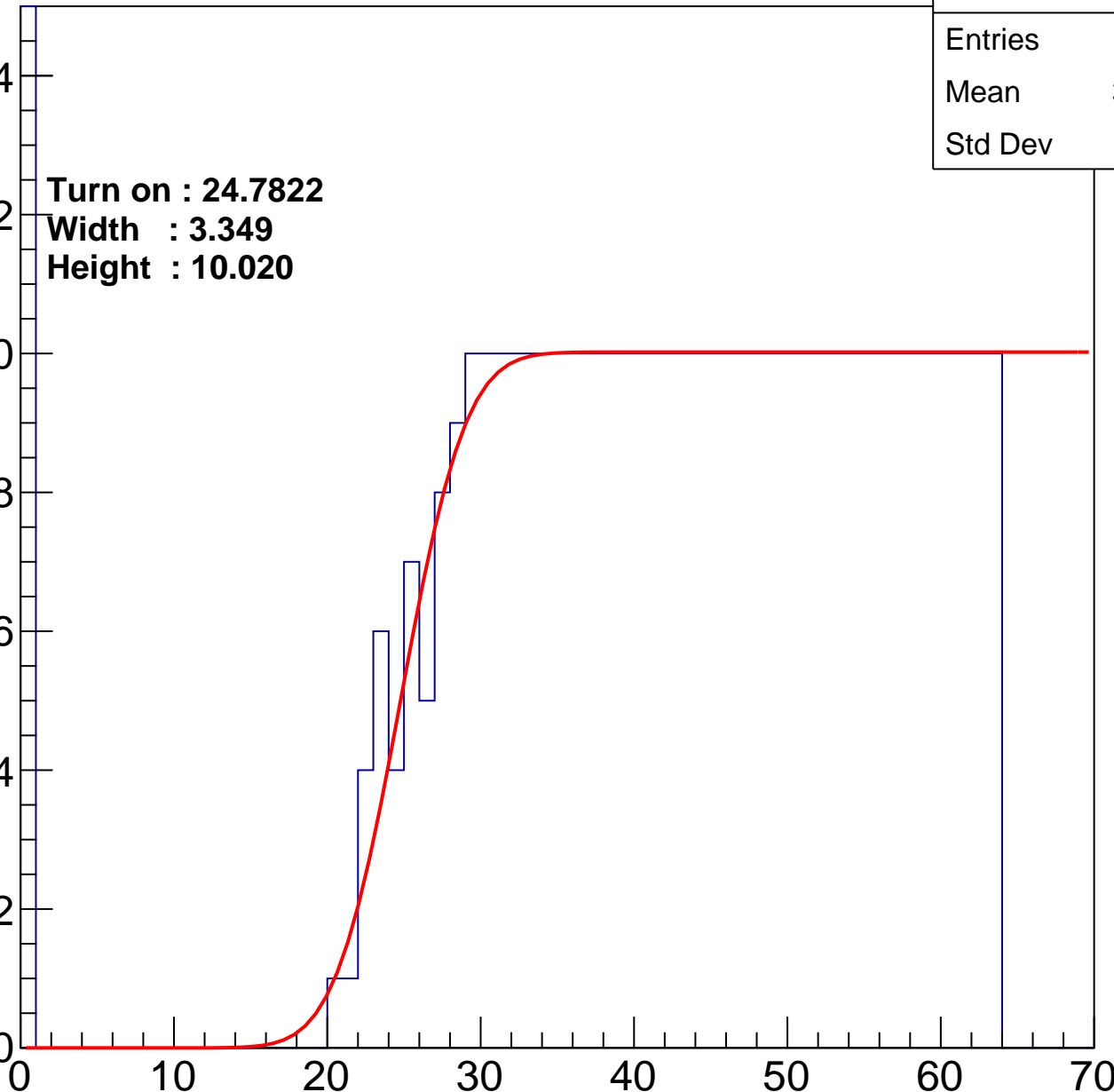
Width : 3.349

Height : 10.020

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch110

calib_packv5_041523_1651.root, FC#0, port C2

Entries	455
Mean	38.07
Std Dev	17.97

Turn on : 24.1004

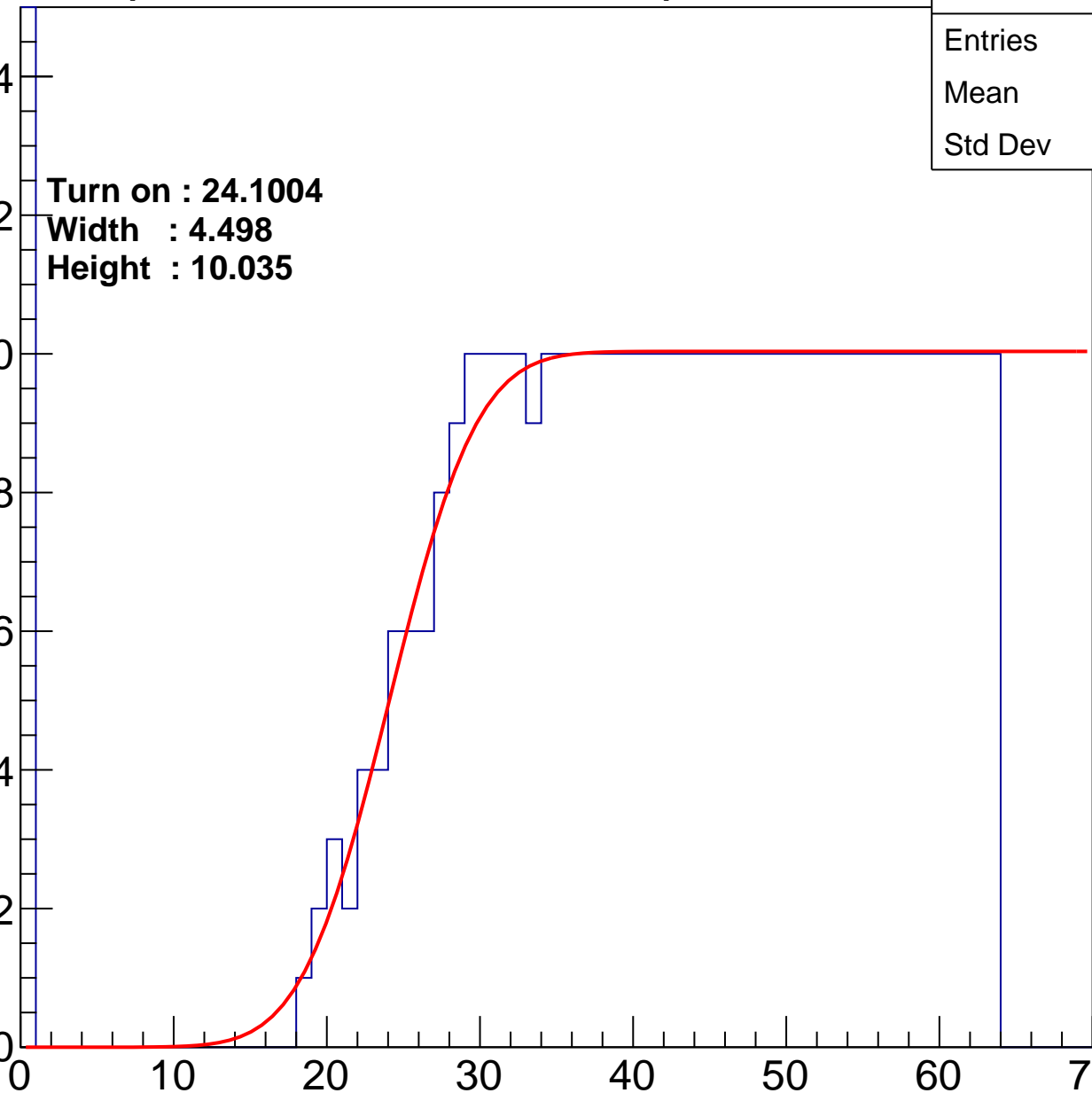
Width : 4.498

Height : 10.035

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch111

calib_packv5_041523_1651.root, FC#0, port C2

Entries	439
Mean	38.72
Std Dev	17.91

Turn on : 25.5282

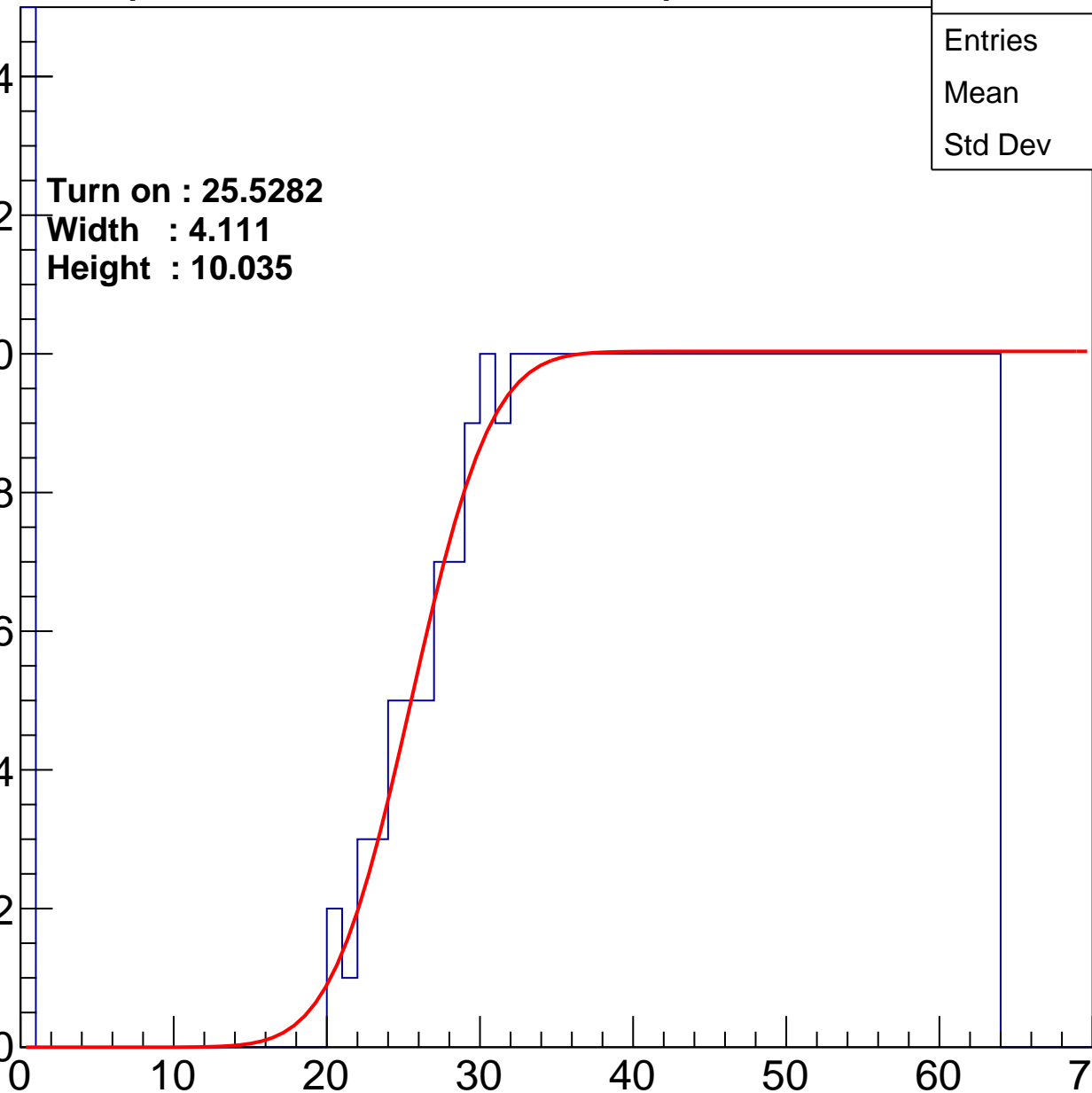
Width : 4.111

Height : 10.035

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch112

calib_packv5_041523_1651.root, FC#0, port C2

Entries	474
Mean	37.43
Std Dev	18.33

Turn on : 23.1881

Width : 2.753

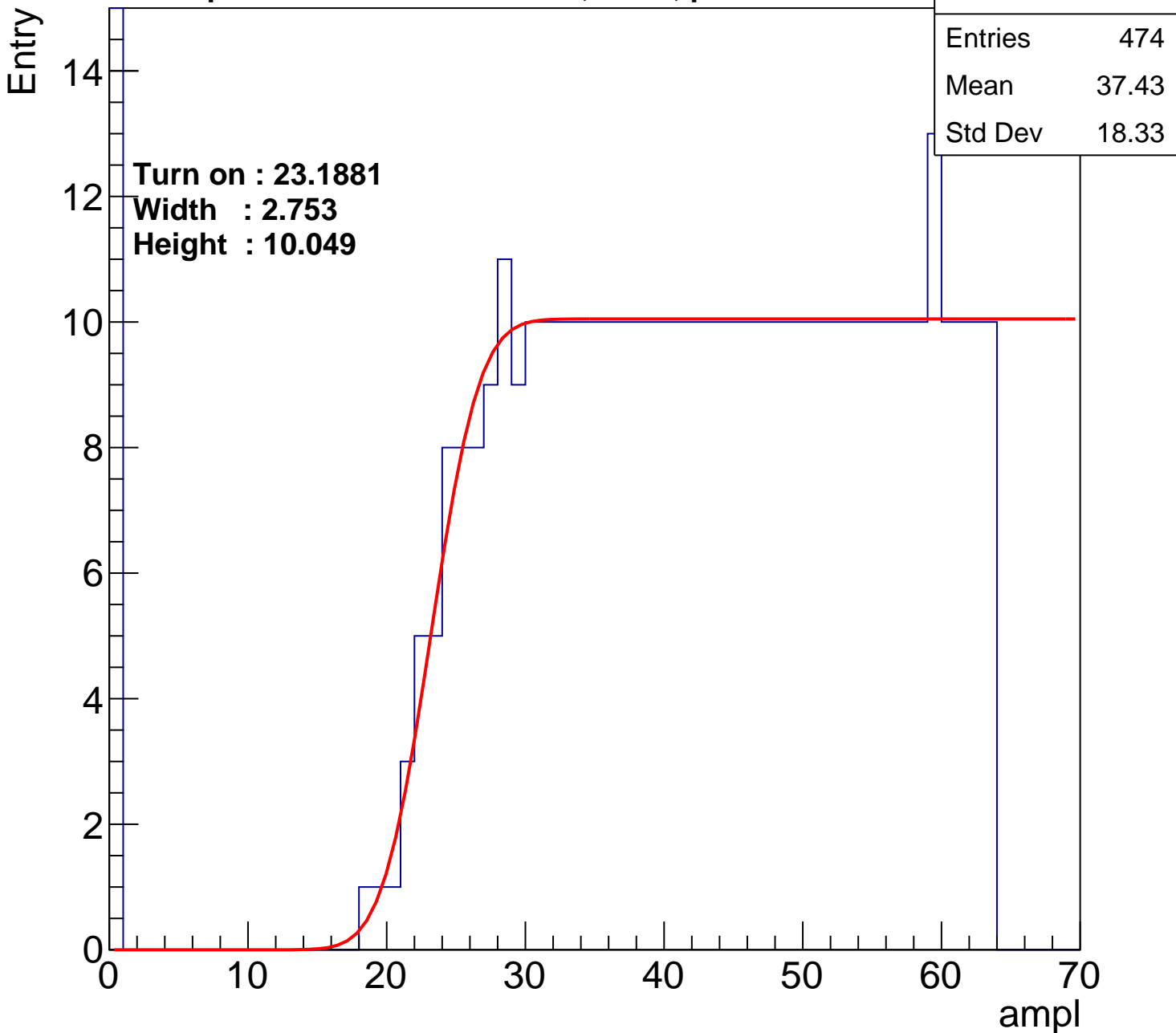
Height : 10.049

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L103S, U23-ch113

calib_packv5_041523_1651.root, FC#0, port C2

Entries	446
Mean	37.71
Std Dev	18.94

Turn on : 26.5708

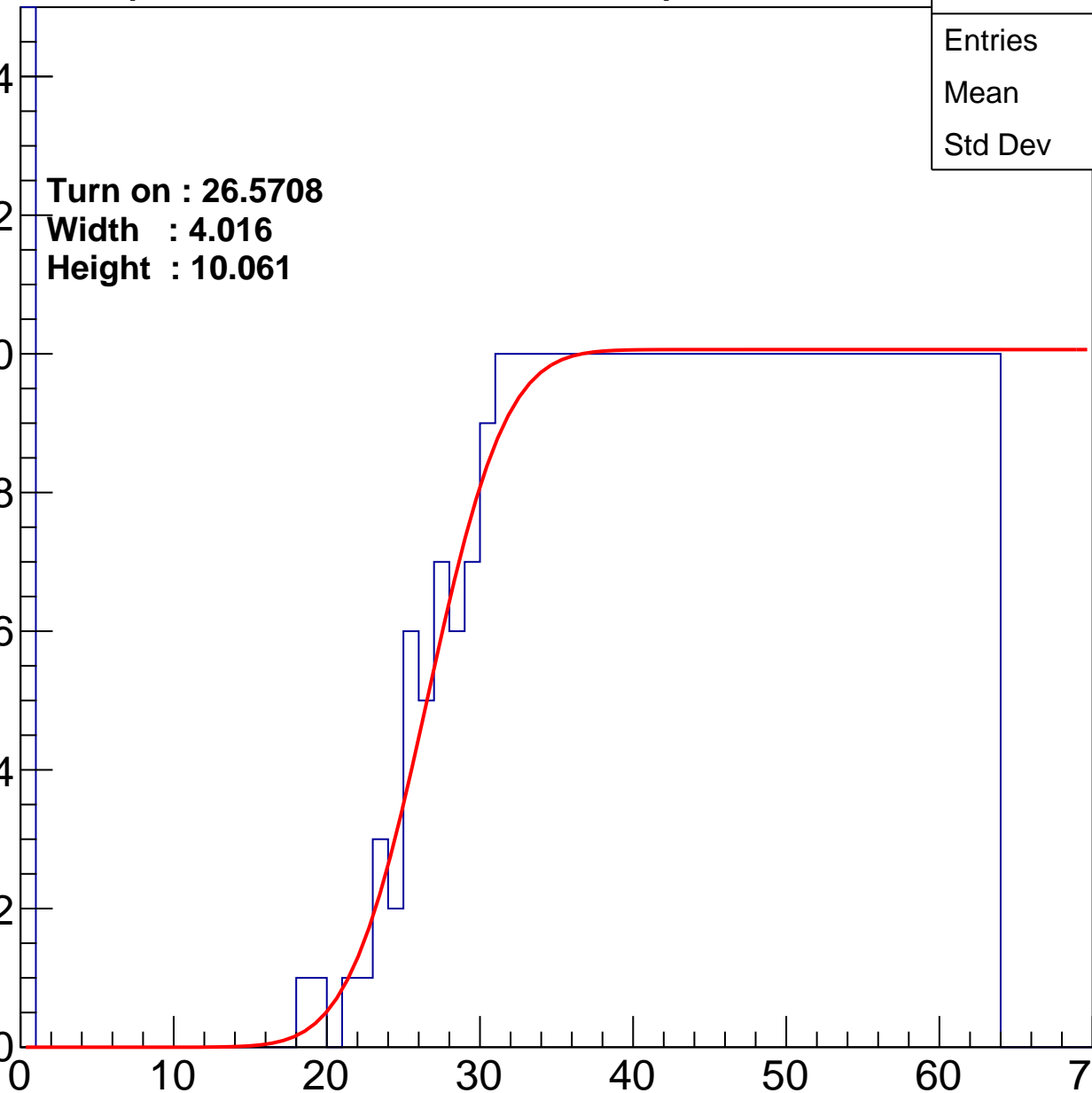
Width : 4.016

Height : 10.061

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch114

calib_packv5_041523_1651.root, FC#0, port C2

Entries	480
Mean	36.75
Std Dev	18.61

Turn on : 23.3854

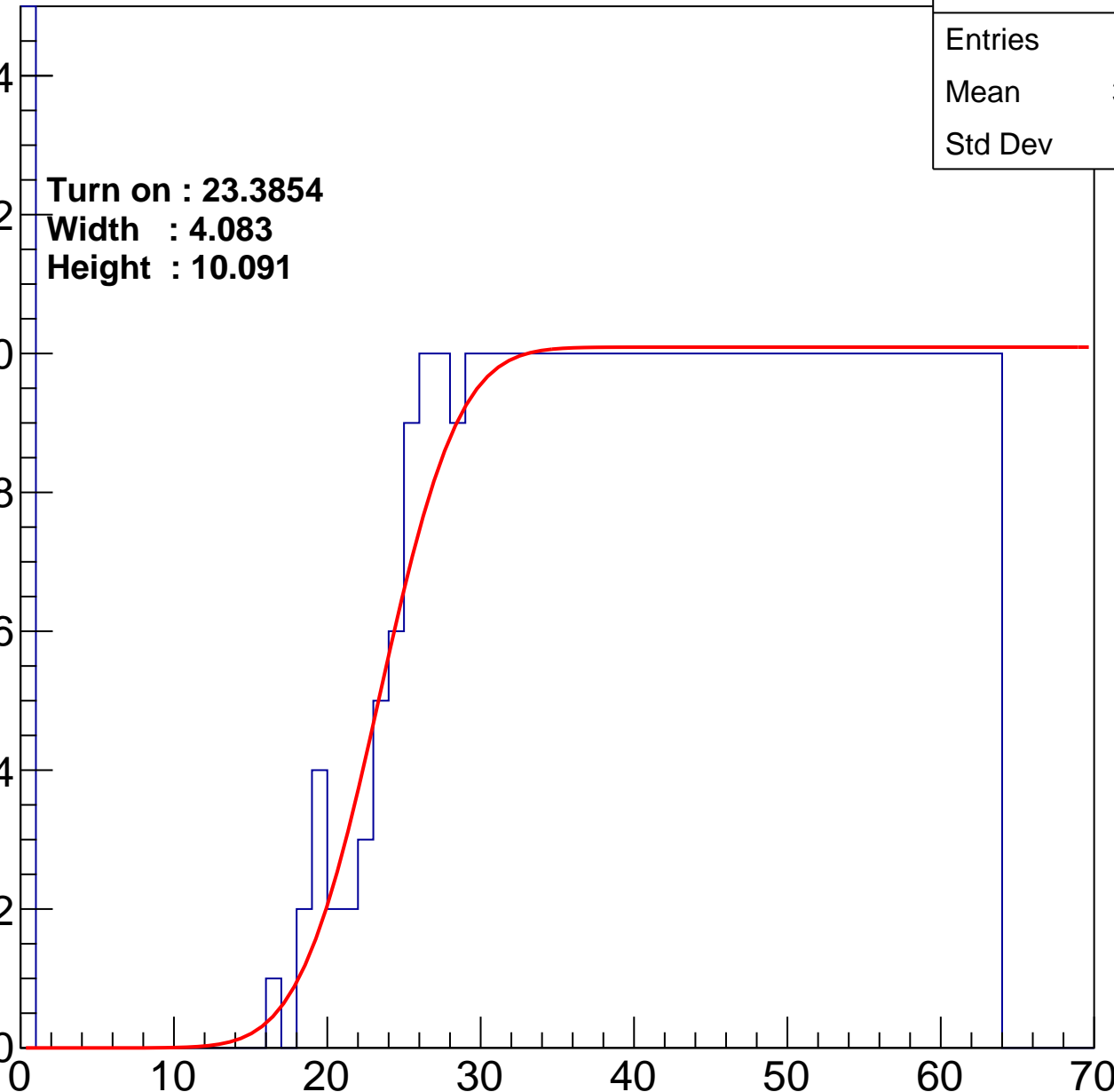
Width : 4.083

Height : 10.091

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch115

calib_packv5_041523_1651.root, FC#0, port C2

Entries	443
Mean	39.05
Std Dev	17.19

Turn on : 24.5215

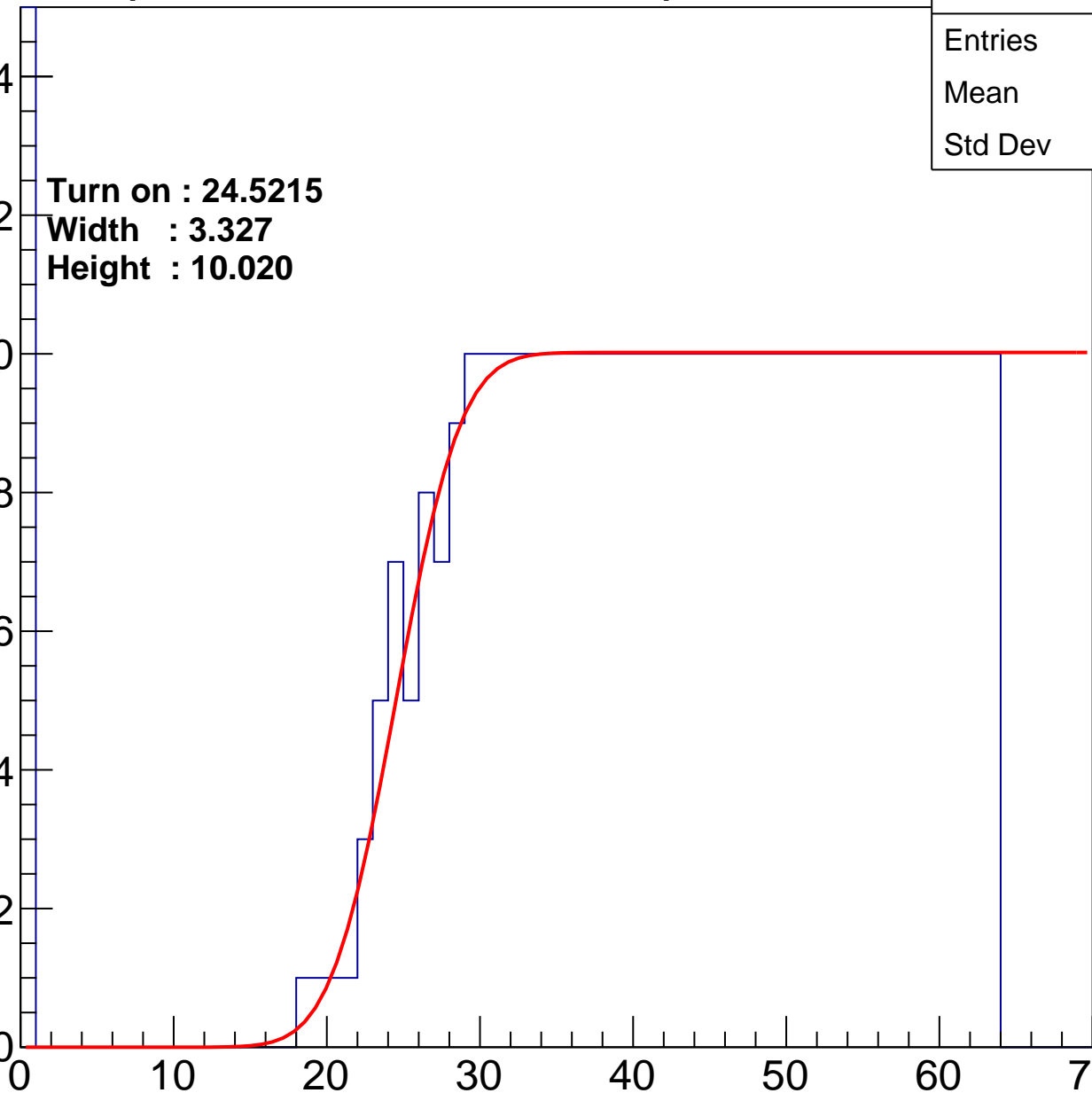
Width : 3.327

Height : 10.020

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch116

calib_packv5_041523_1651.root, FC#0, port C2

Entries	462
Mean	38.1
Std Dev	17.63

Turn on : 23.4325

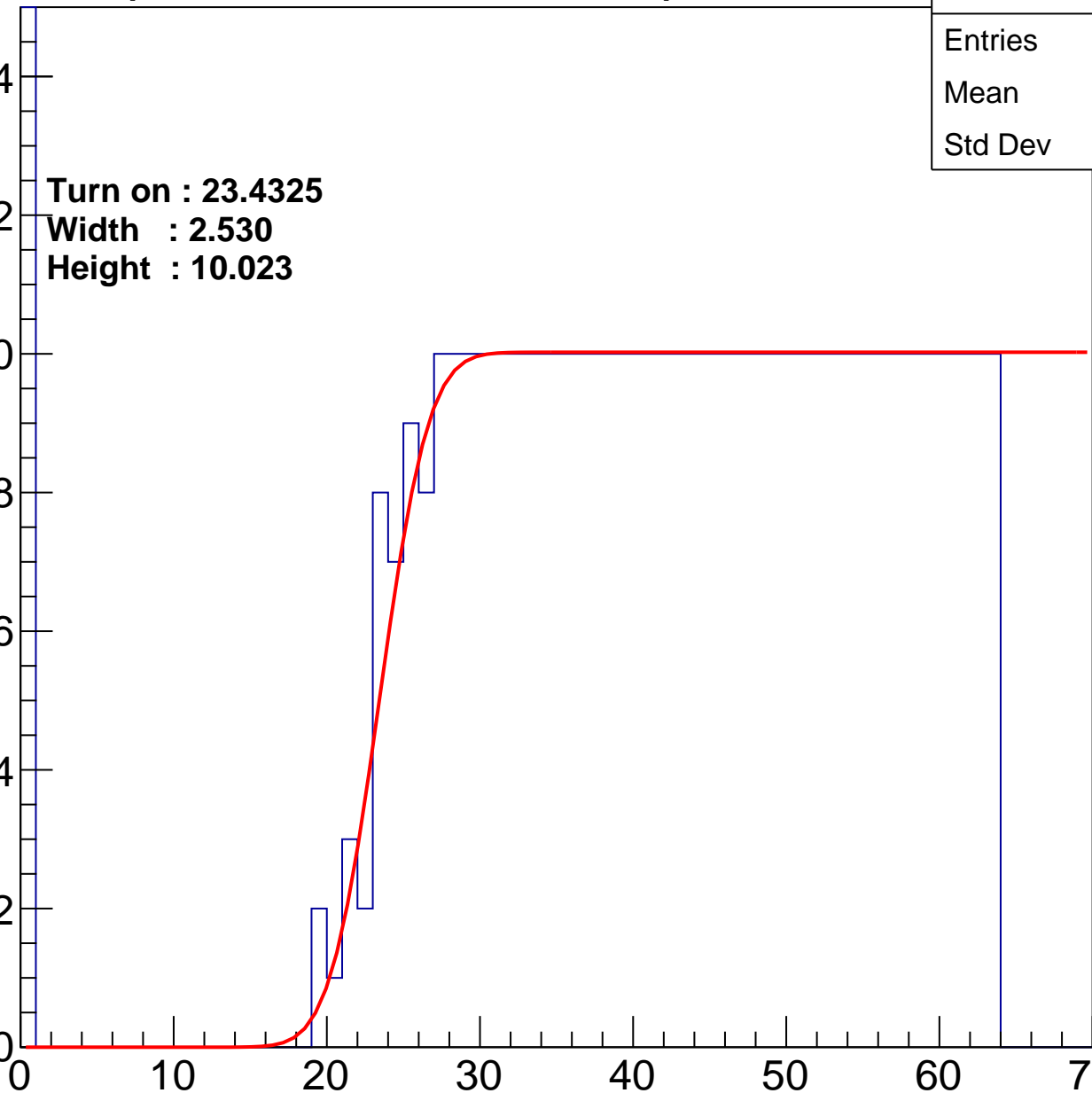
Width : 2.530

Height : 10.023

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch117

calib_packv5_041523_1651.root, FC#0, port C2

Entries	451
Mean	37.7
Std Dev	18.73

Turn on : 25.2146

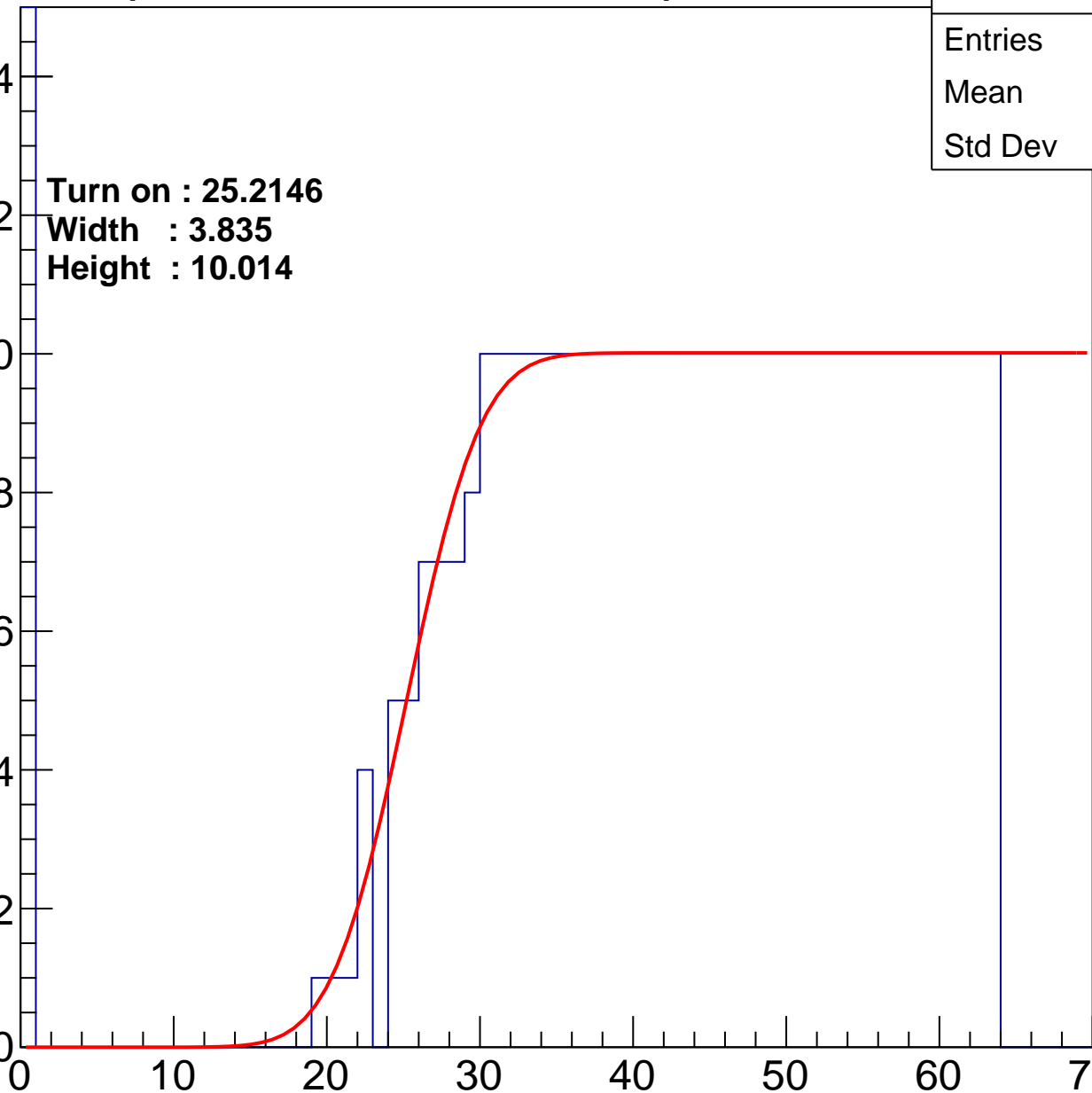
Width : 3.835

Height : 10.014

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch118

calib_packv5_041523_1651.root, FC#0, port C2

Entries	456
Mean	38.19
Std Dev	17.81

Turn on : 23.5004

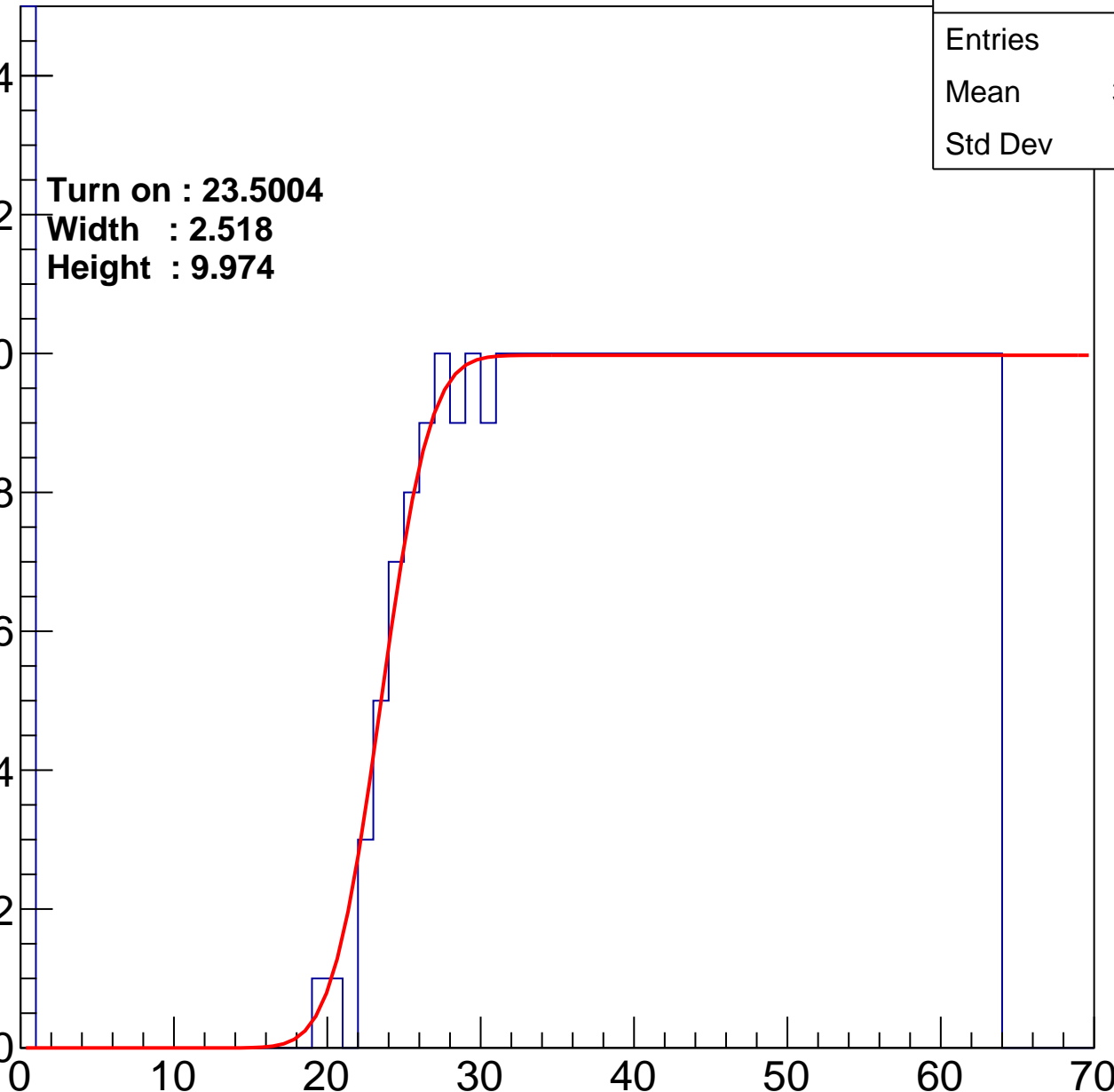
Width : 2.518

Height : 9.974

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch119

calib_packv5_041523_1651.root, FC#0, port C2

Entries	434
Mean	39.07
Std Dev	17.67

Turn on : 26.0702

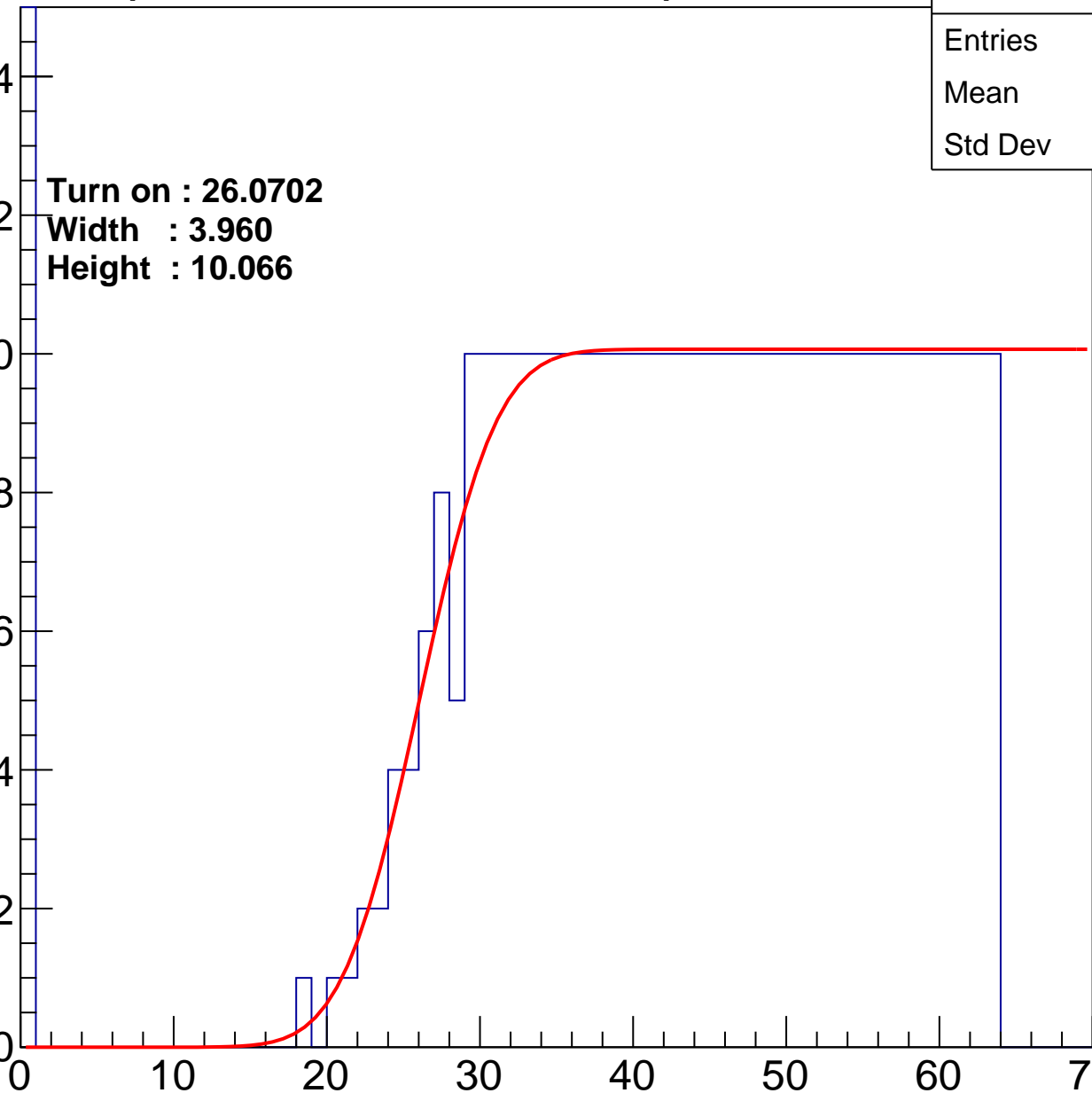
Width : 3.960

Height : 10.066

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch120

calib_packv5_041523_1651.root, FC#0, port C2

Entries	479
Mean	36.83
Std Dev	18.55

Turn on : 23.1371

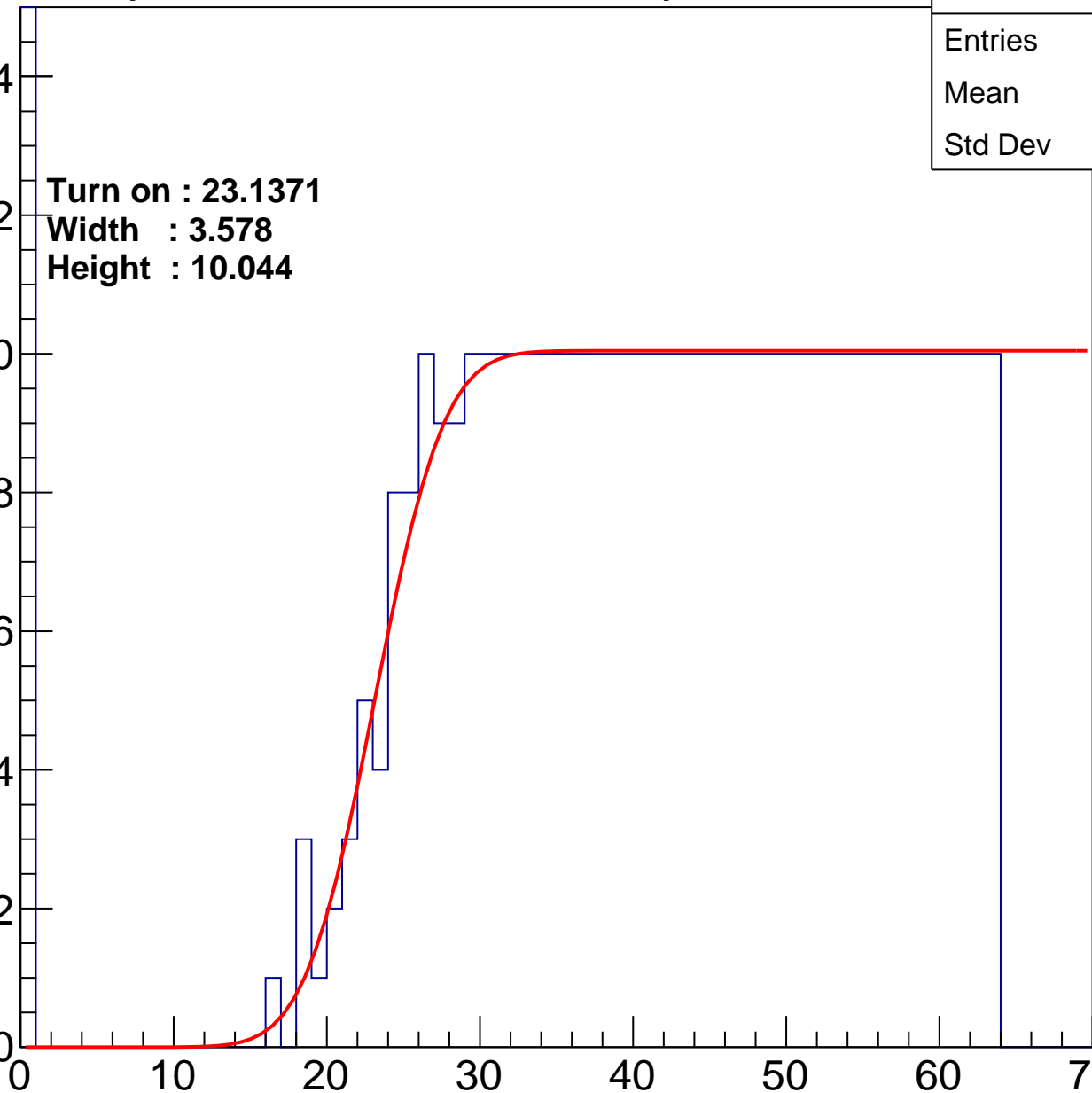
Width : 3.578

Height : 10.044

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch121

calib_packv5_041523_1651.root, FC#0, port C2

Entries	462
Mean	37.29
Std Dev	18.71

Turn on : 26.1833

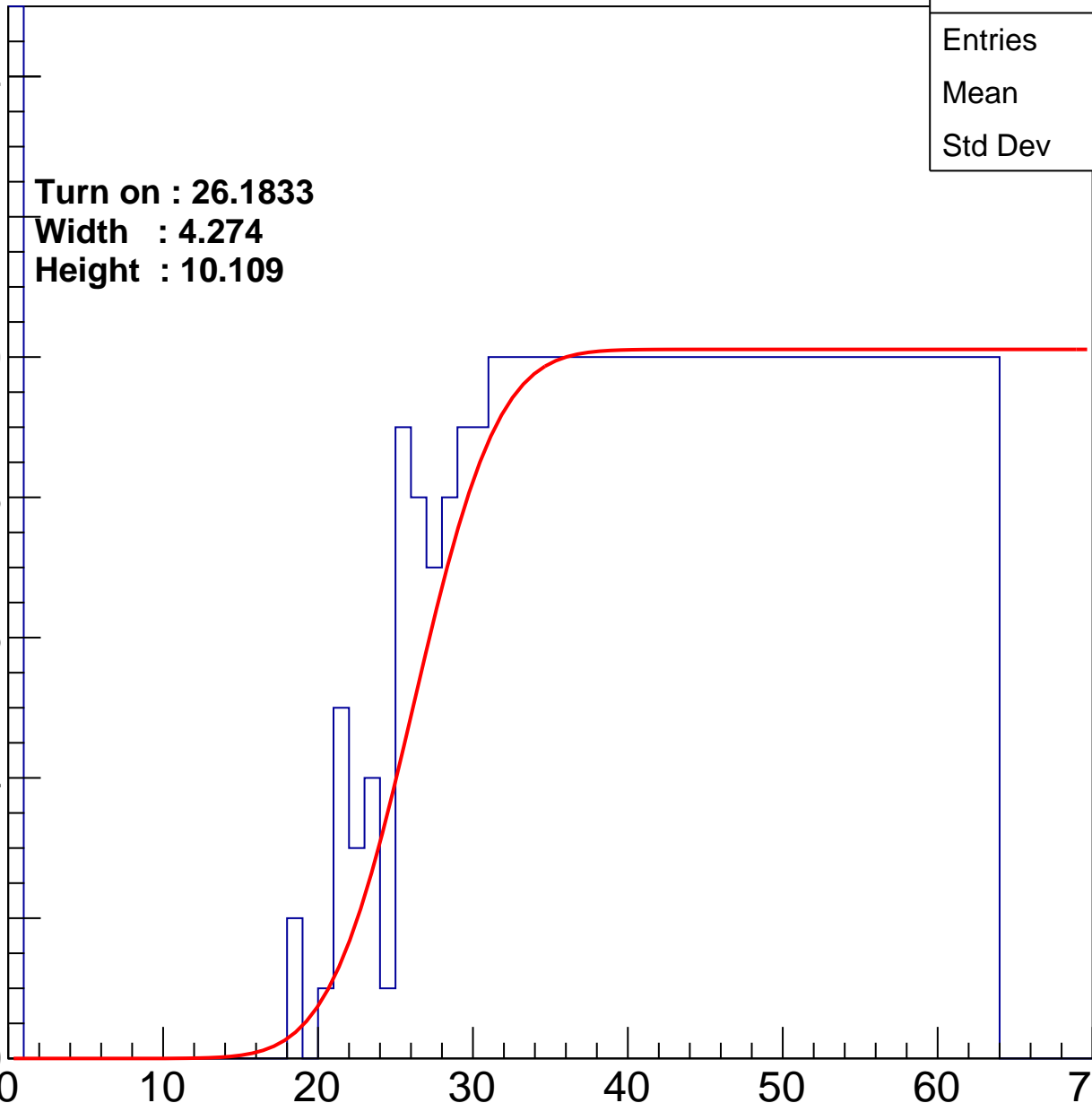
Width : 4.274

Height : 10.109

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch122

calib_packv5_041523_1651.root, FC#0, port C2

Entries	417
Mean	40.36
Std Dev	16.73

Turn on : 26.6732

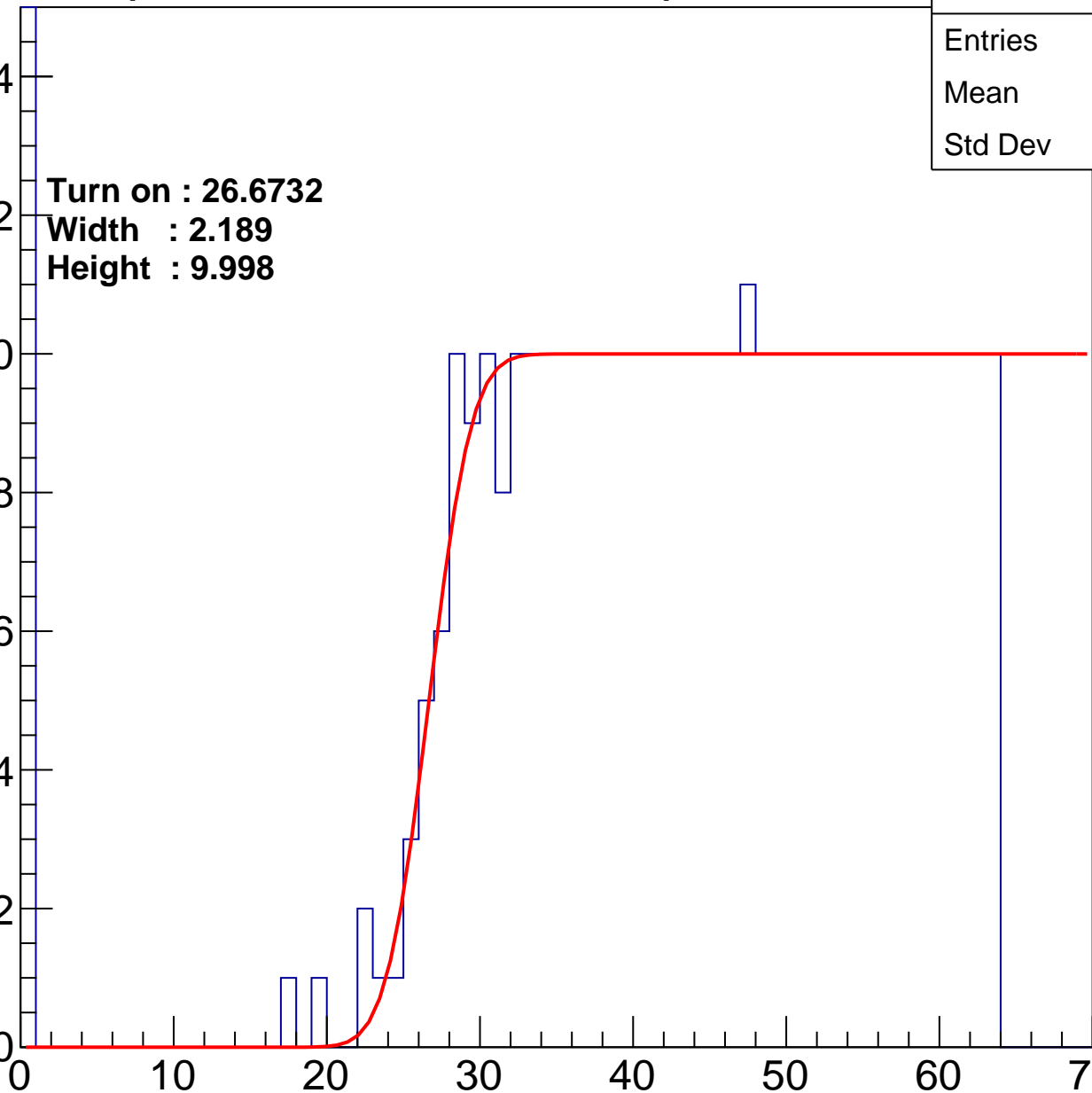
Width : 2.189

Height : 9.998

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch123

calib_packv5_041523_1651.root, FC#0, port C2

Entries	418
Mean	39.51
Std Dev	17.89

Turn on : 28.0291

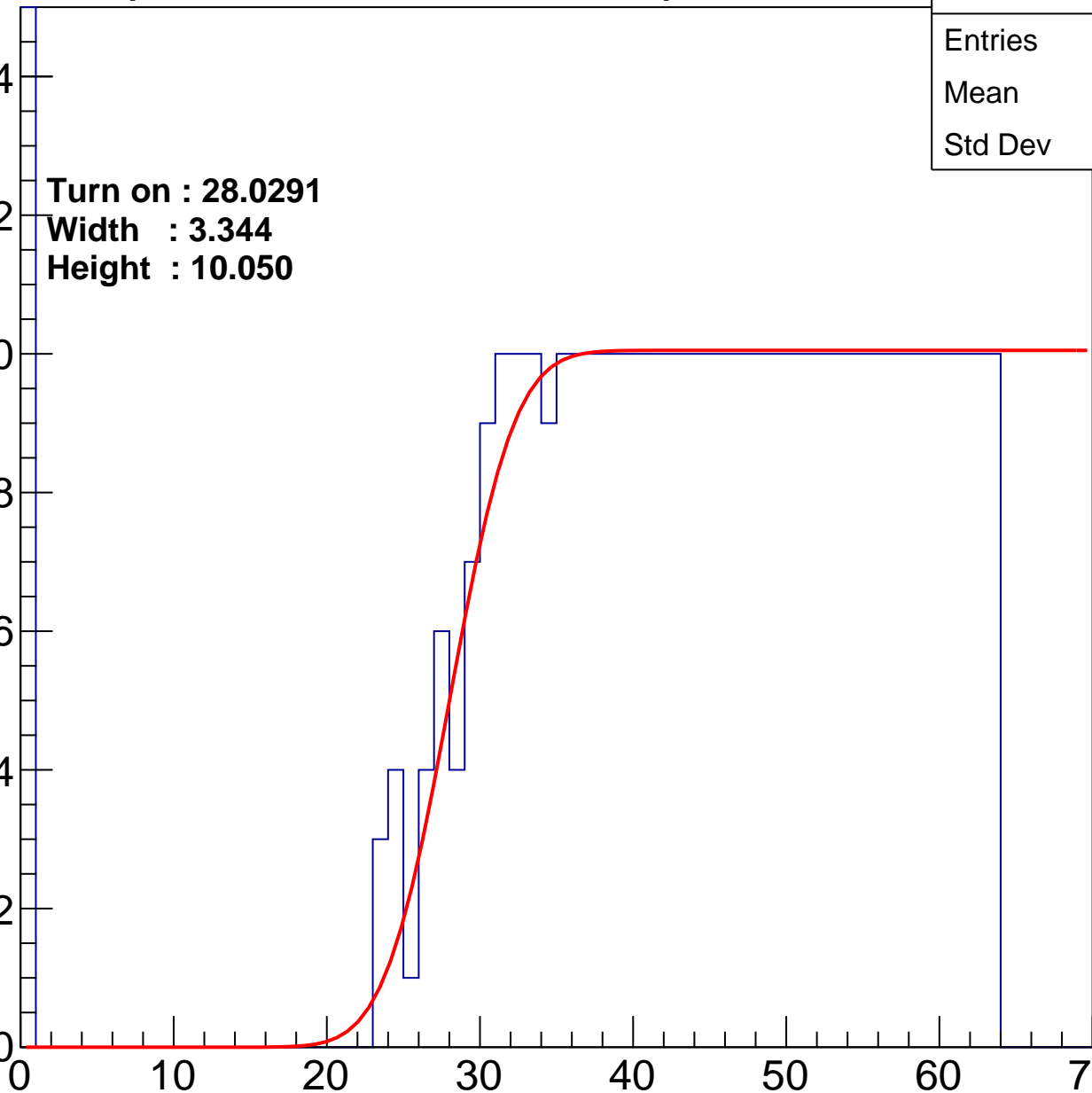
Width : 3.344

Height : 10.050

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch124

calib_packv5_041523_1651.root, FC#0, port C2

Entries	436
Mean	38.69
Std Dev	18.14

Turn on : 25.8991

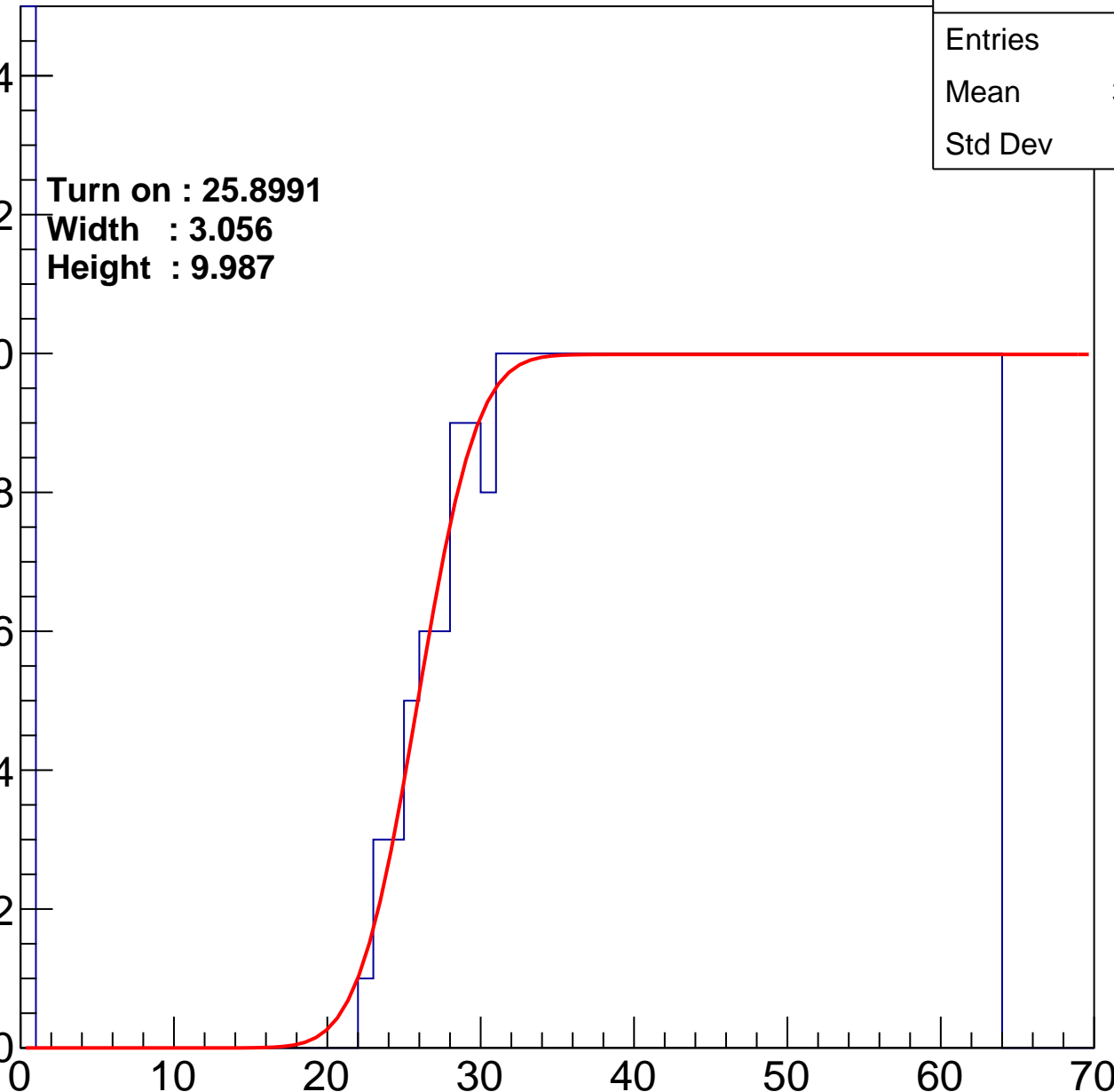
Width : 3.056

Height : 9.987

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch125

calib_packv5_041523_1651.root, FC#0, port C2

Entries	409
Mean	39.6
Std Dev	18.34

Turn on : 29.0293

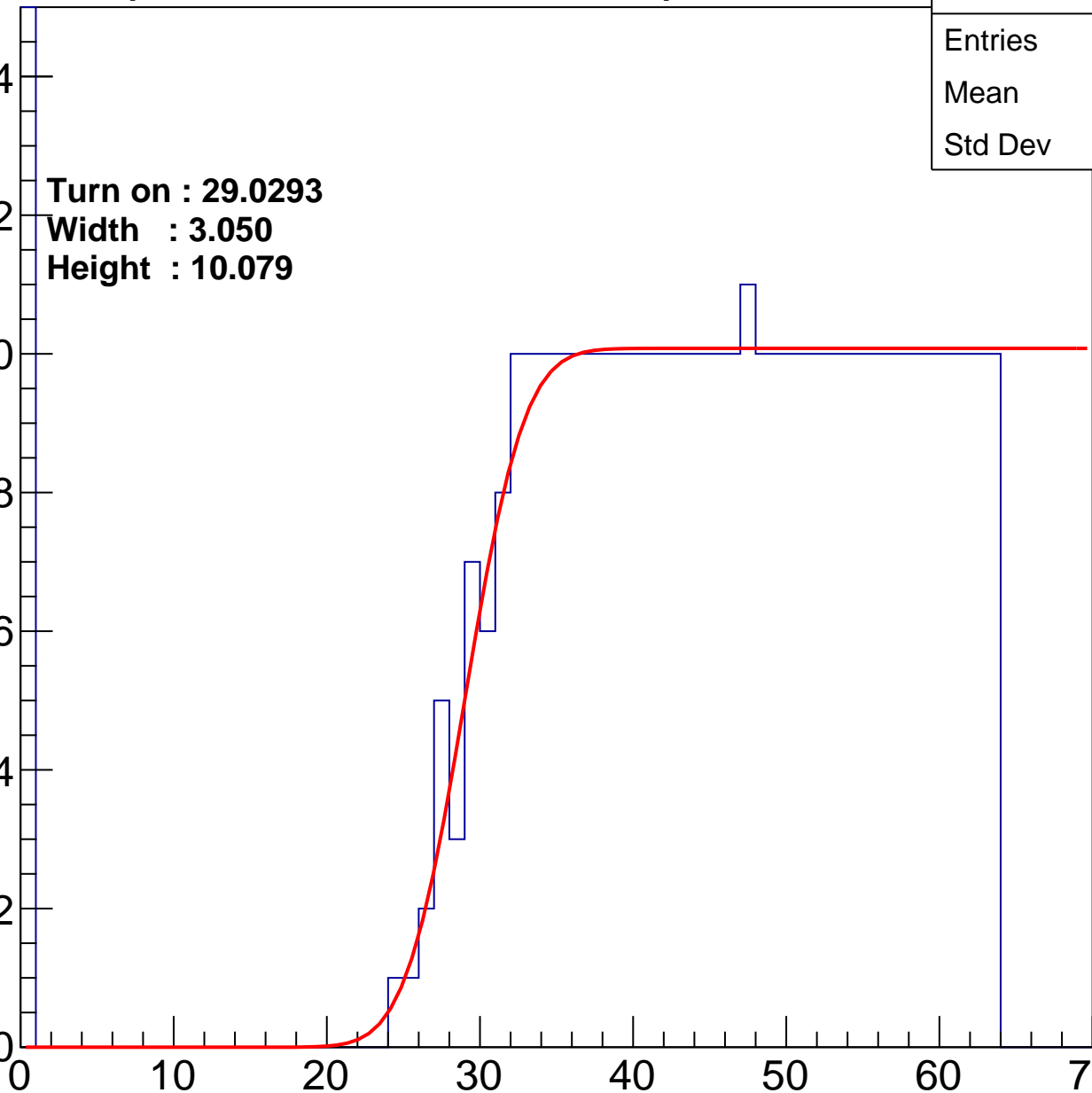
Width : 3.050

Height : 10.079

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch126

calib_packv5_041523_1651.root, FC#0, port C2

Entries	487
Mean	36.45
Std Dev	18.69

Turn on : 22.7745

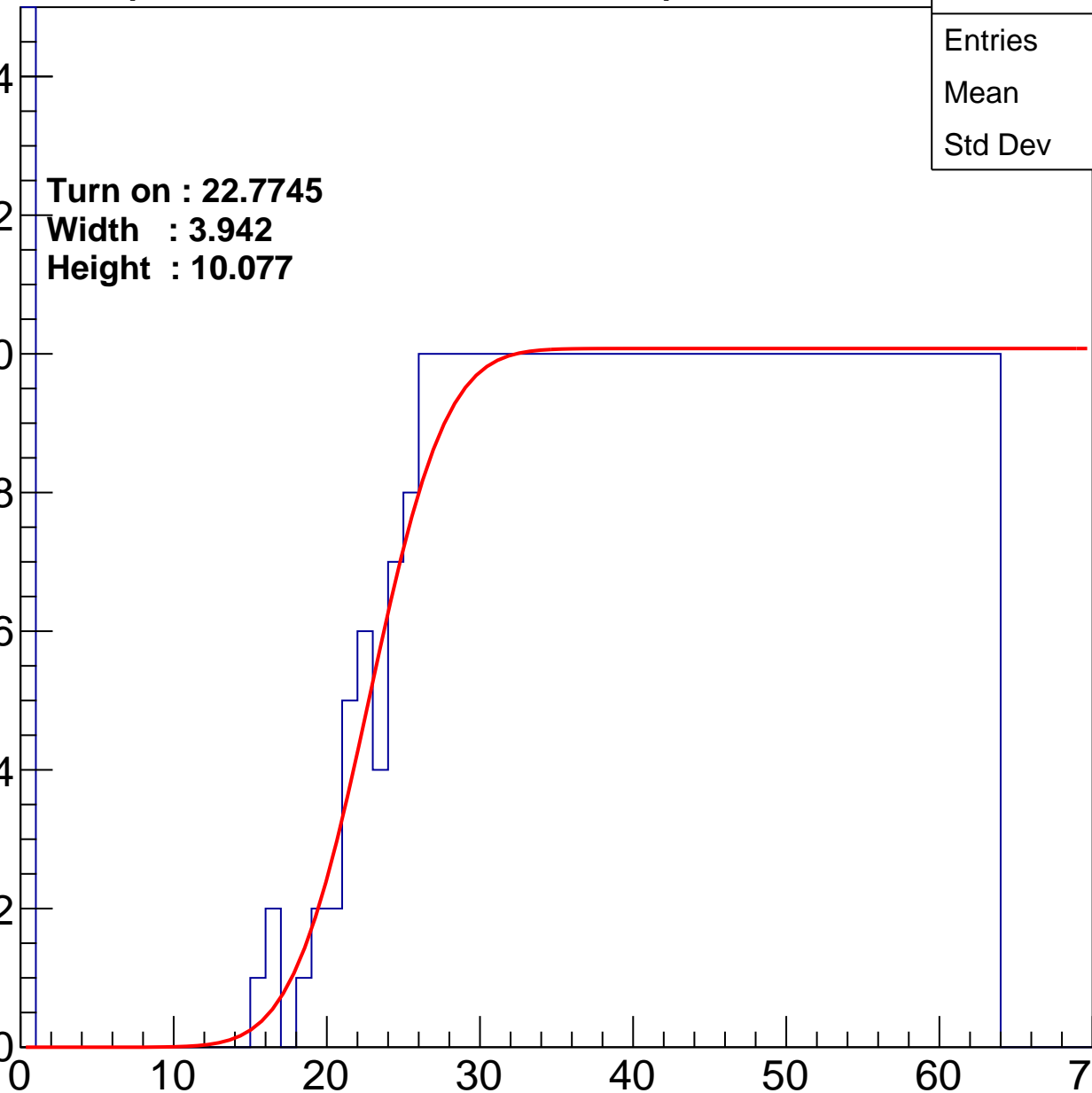
Width : 3.942

Height : 10.077

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch127

calib_packv5_041523_1651.root, FC#0, port C2

Entries	488
Mean	36.03
Std Dev	19.22

Turn on : 22.8531

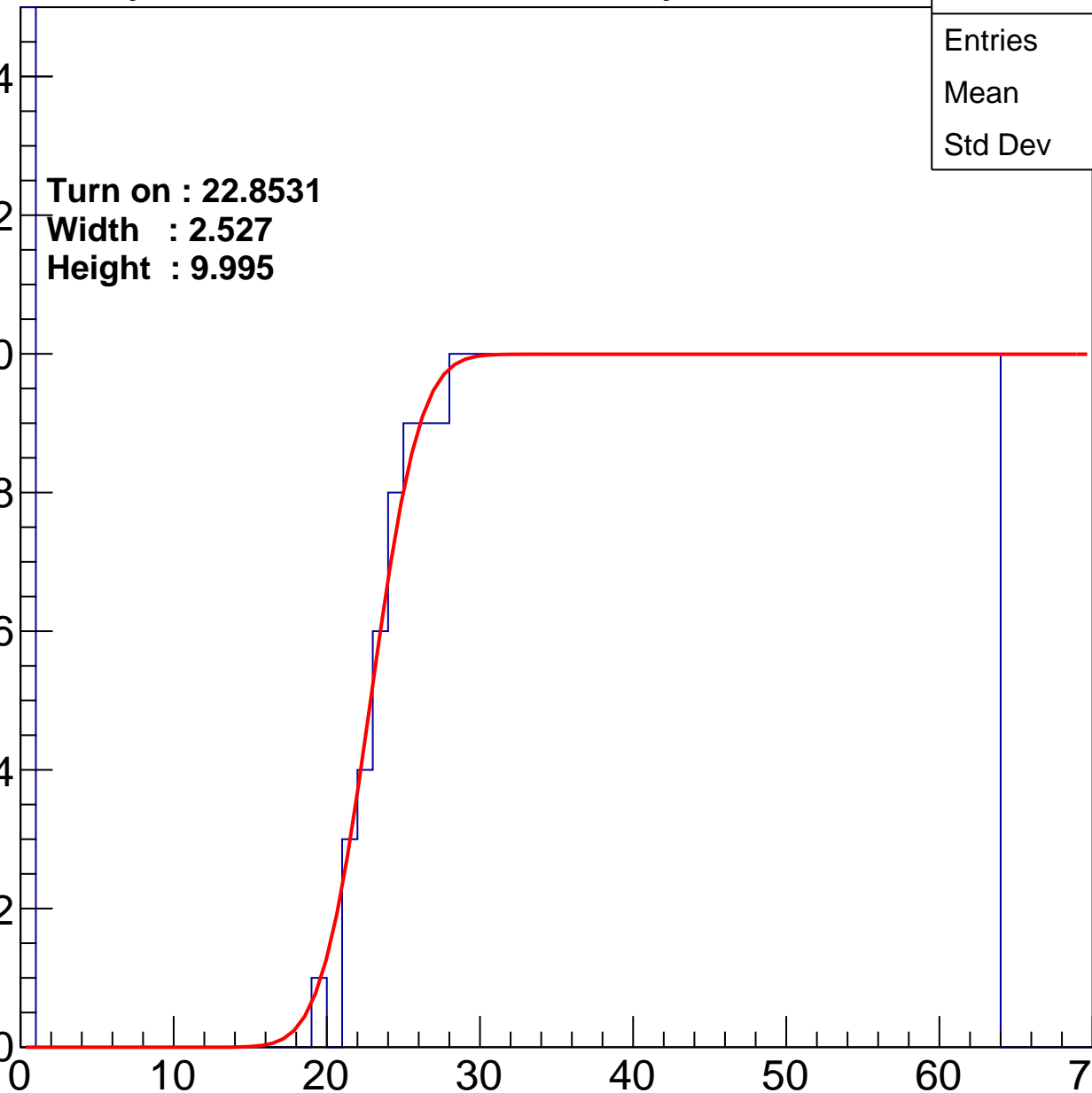
Width : 2.527

Height : 9.995

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch127

calib_packv5_041523_1651.root, FC#0, port C2

Entries	488
Mean	36.03
Std Dev	19.22

Turn on : 22.8531

Width : 2.527

Height : 9.995

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70

