

B1L103S, U1-ch0

calib_packv5_042523_0143.root, FC#7, port C2

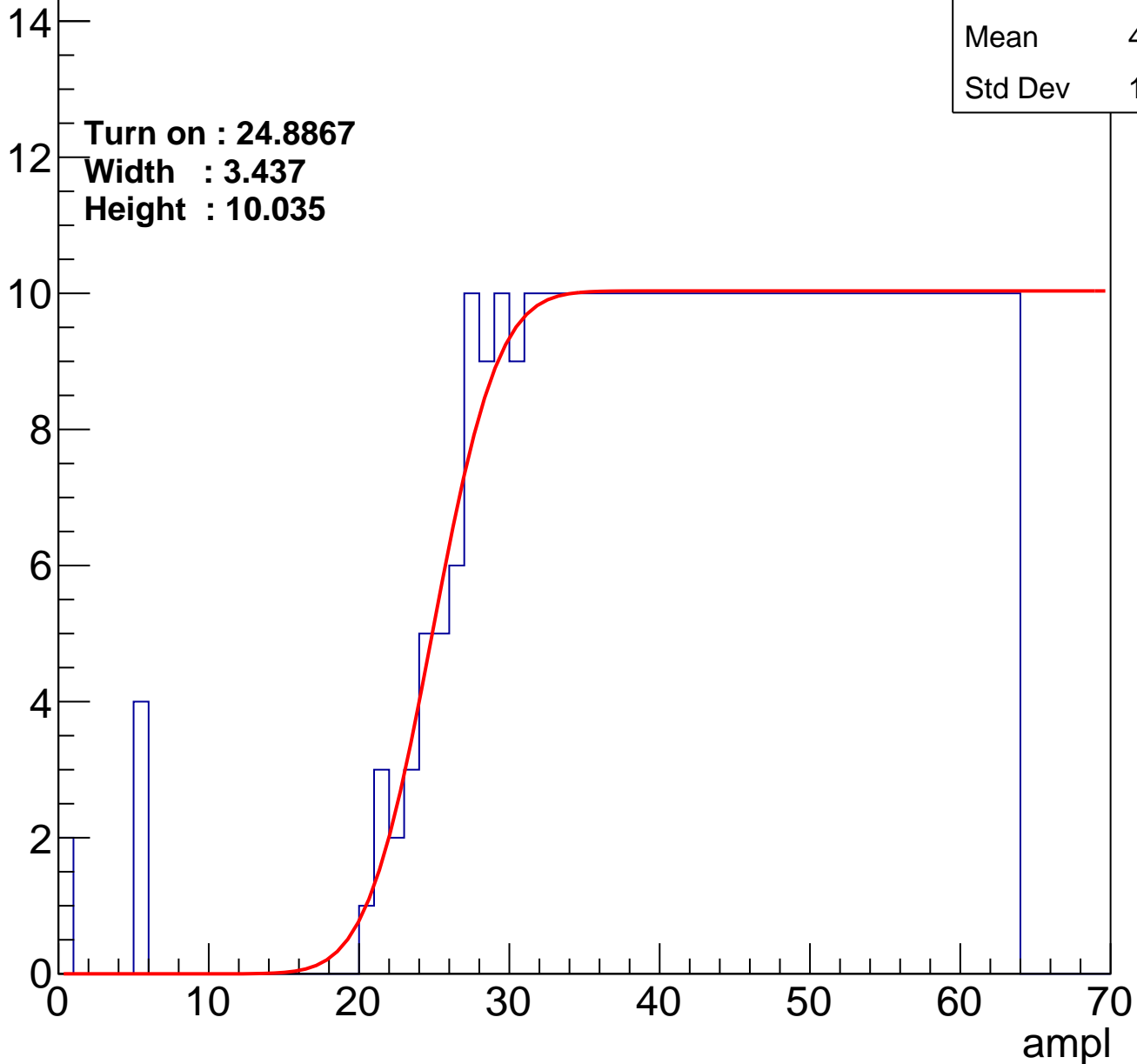
Entries	399
Mean	43.13
Std Dev	12.46

Turn on : 24.8867

Width : 3.437

Height : 10.035

Entry



B1L103S, U1-ch1

calib_packv5_042523_0143.root, FC#7, port C2

Entries	392
Mean	43.49
Std Dev	12.29

Turn on : 25.2303

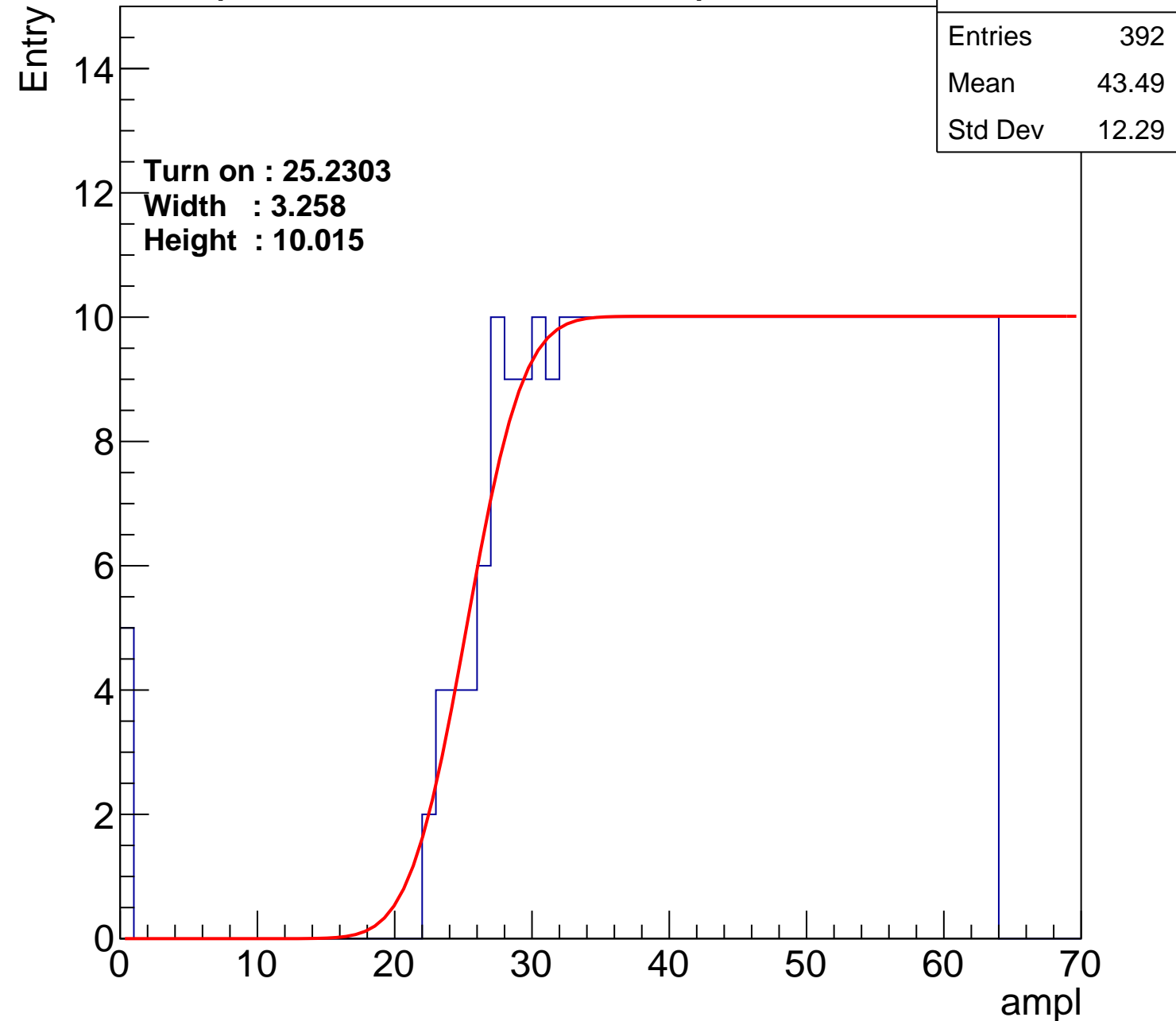
Width : 3.258

Height : 10.015

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch2

calib_packv5_042523_0143.root, FC#7, port C2

Entries	379
Mean	44.16
Std Dev	11.88

Turn on : 26.9797

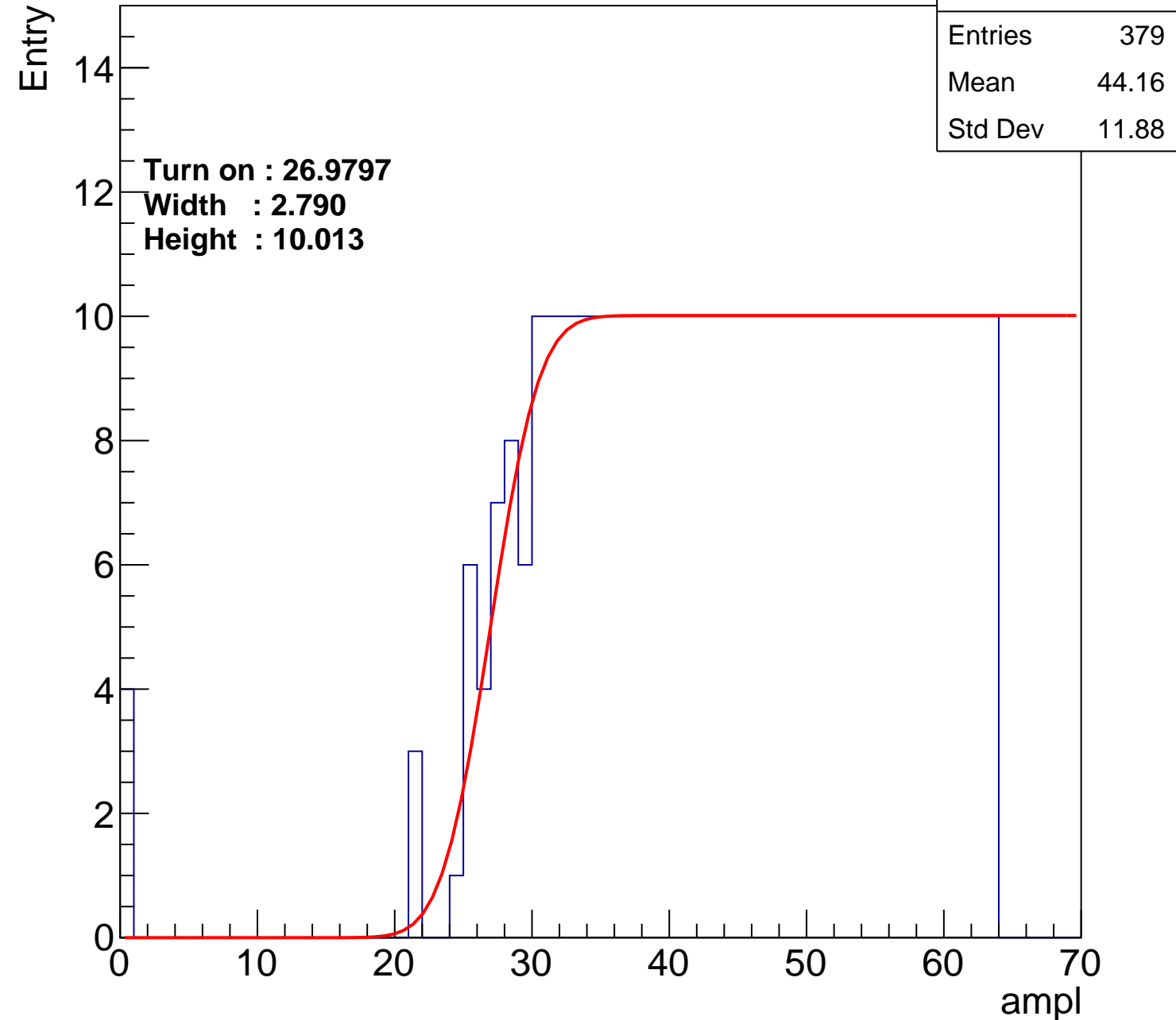
Width : 2.790

Height : 10.013

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch3

calib_packv5_042523_0143.root, FC#7, port C2

Entries	371
Mean	44.41
Std Dev	12.07

Turn on : 27.7734

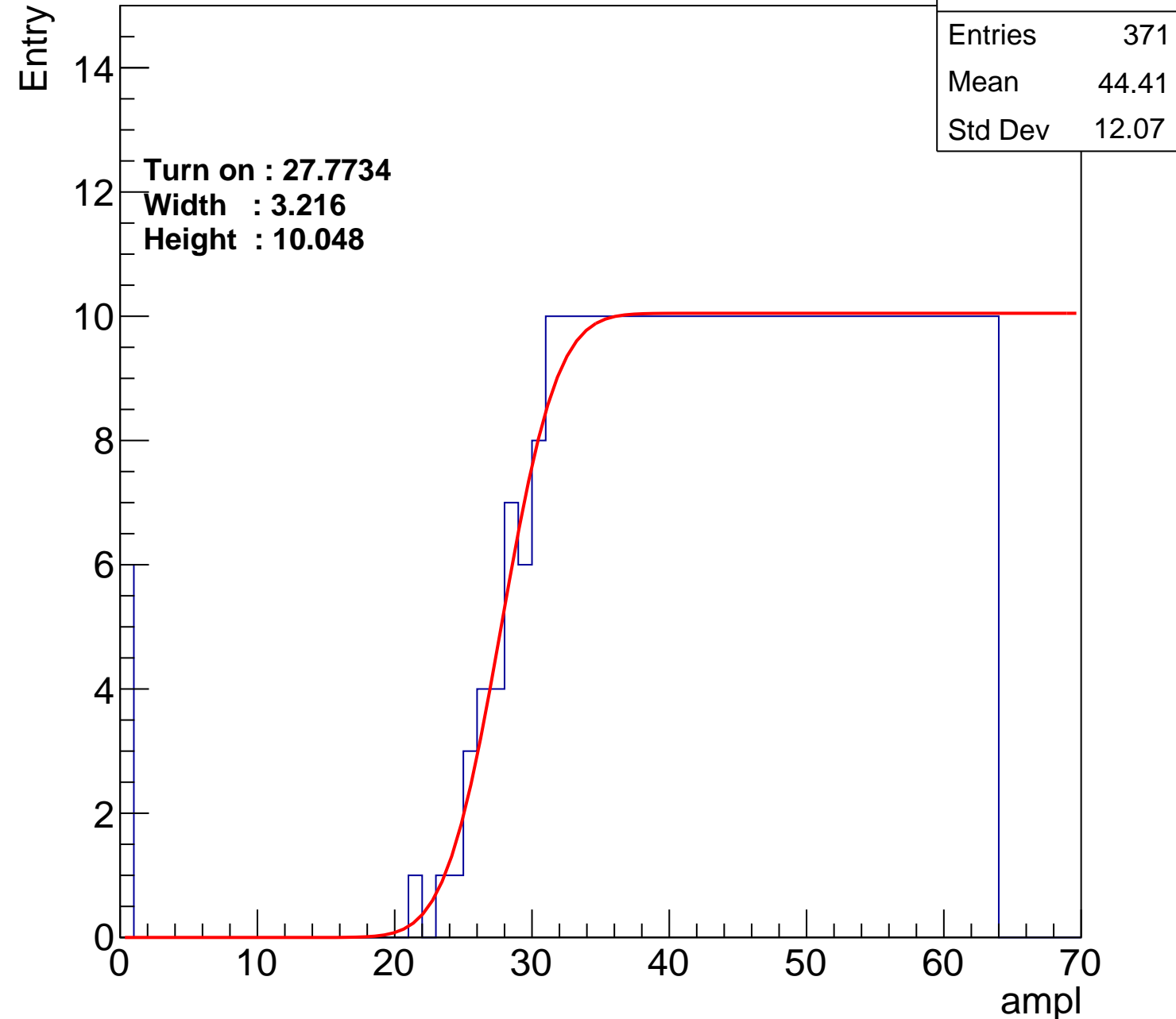
Width : 3.216

Height : 10.048

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch4

calib_packv5_042523_0143.root, FC#7, port C2

Entries	383
Mean	43.95
Std Dev	11.98

Turn on : 25.9696

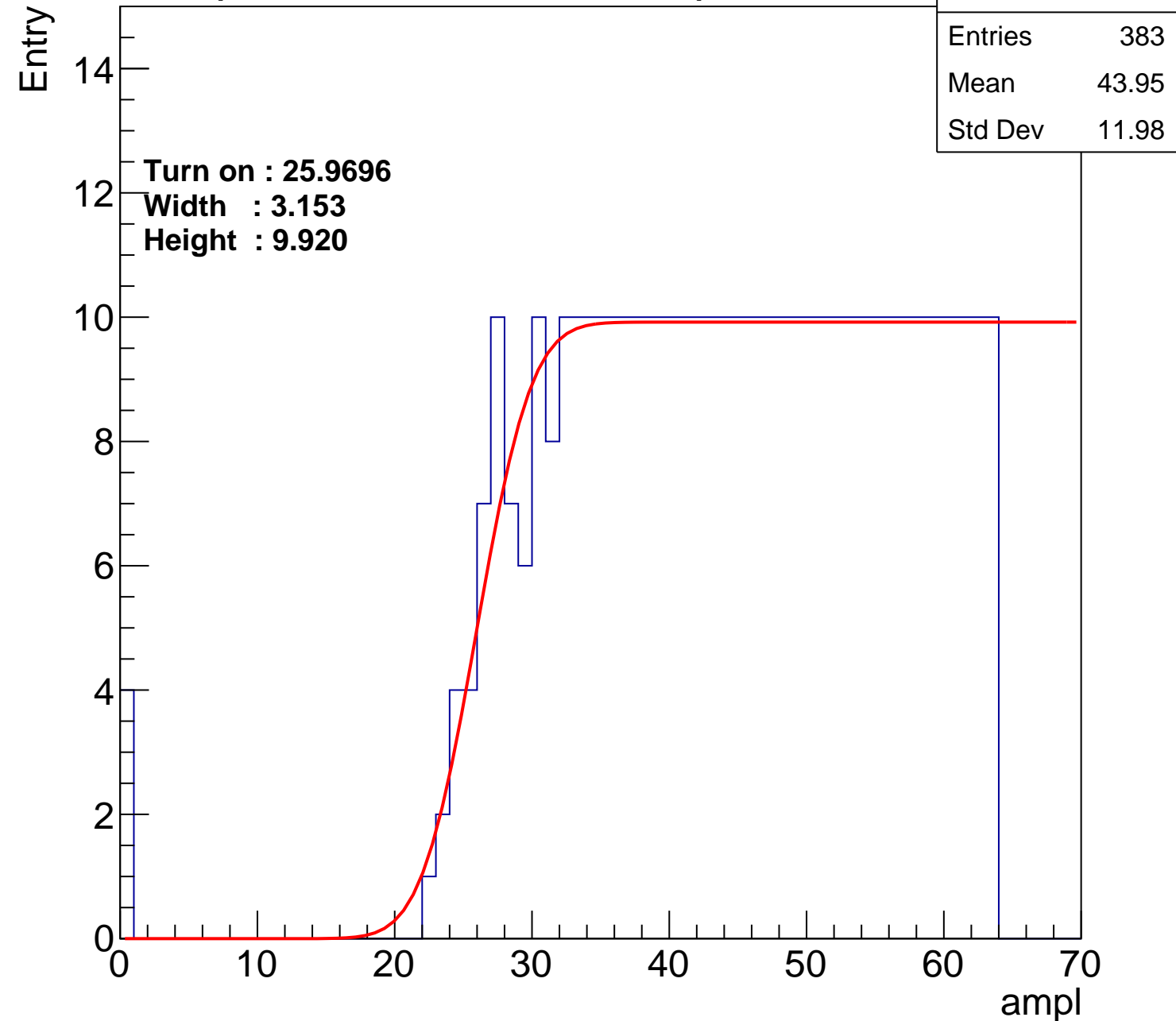
Width : 3.153

Height : 9.920

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch5

calib_packv5_042523_0143.root, FC#7, port C2

Entries	386
Mean	43.78
Std Dev	12.09

Turn on : 25.8927

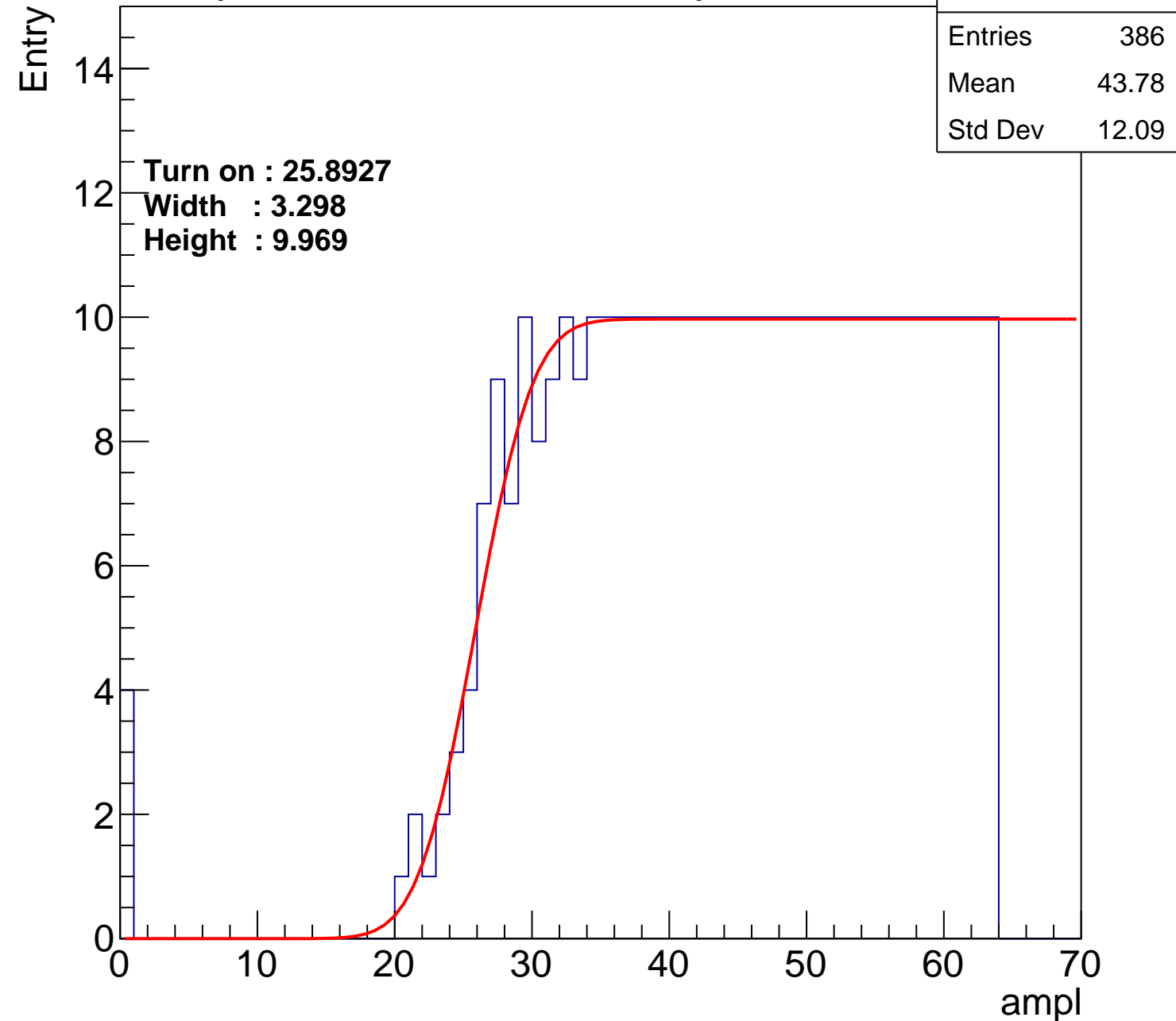
Width : 3.298

Height : 9.969

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch6

calib_packv5_042523_0143.root, FC#7, port C2

Entries	385
Mean	43.97
Std Dev	11.71

Turn on : 26.1104

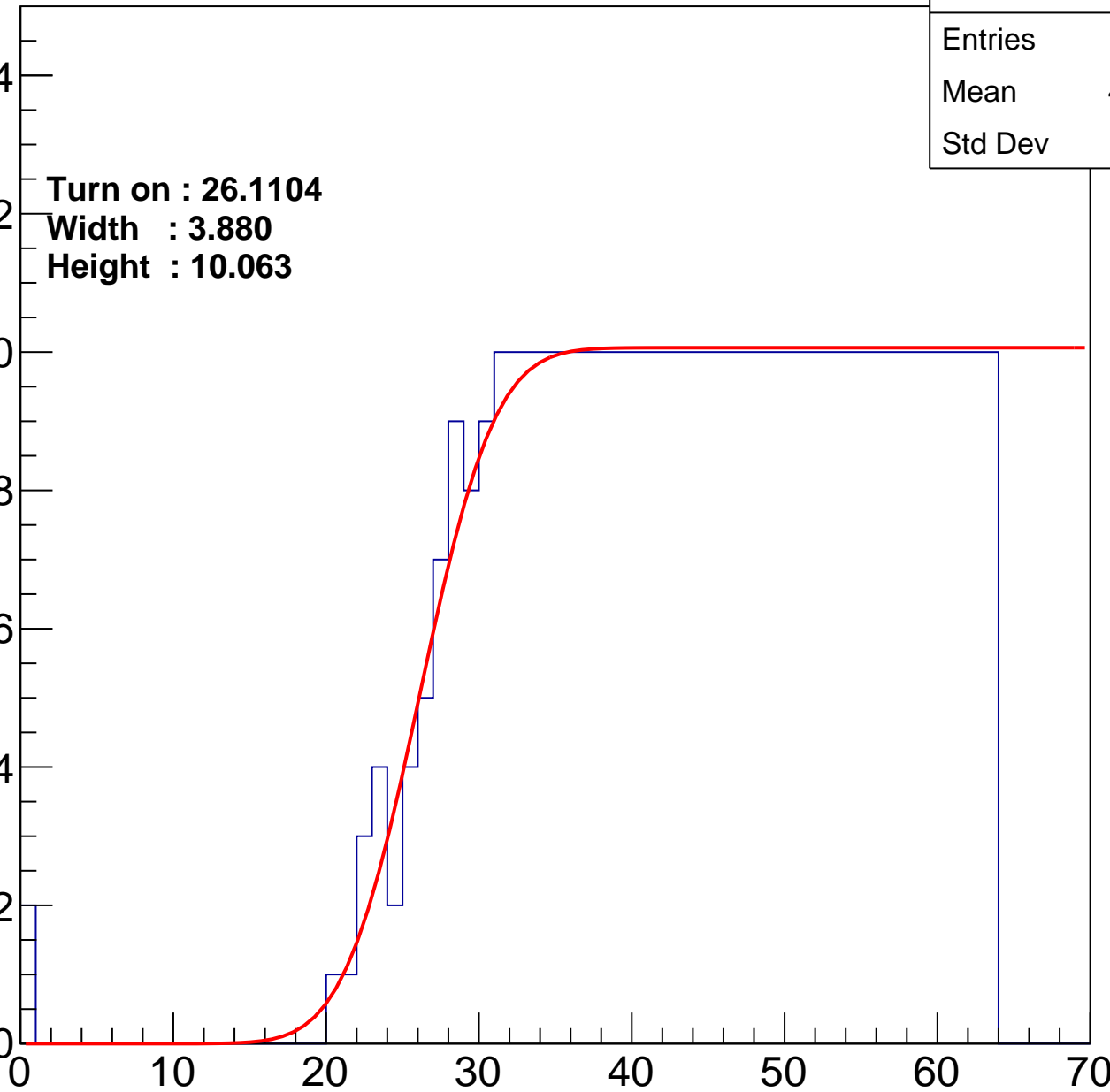
Width : 3.880

Height : 10.063

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch7

calib_packv5_042523_0143.root, FC#7, port C2

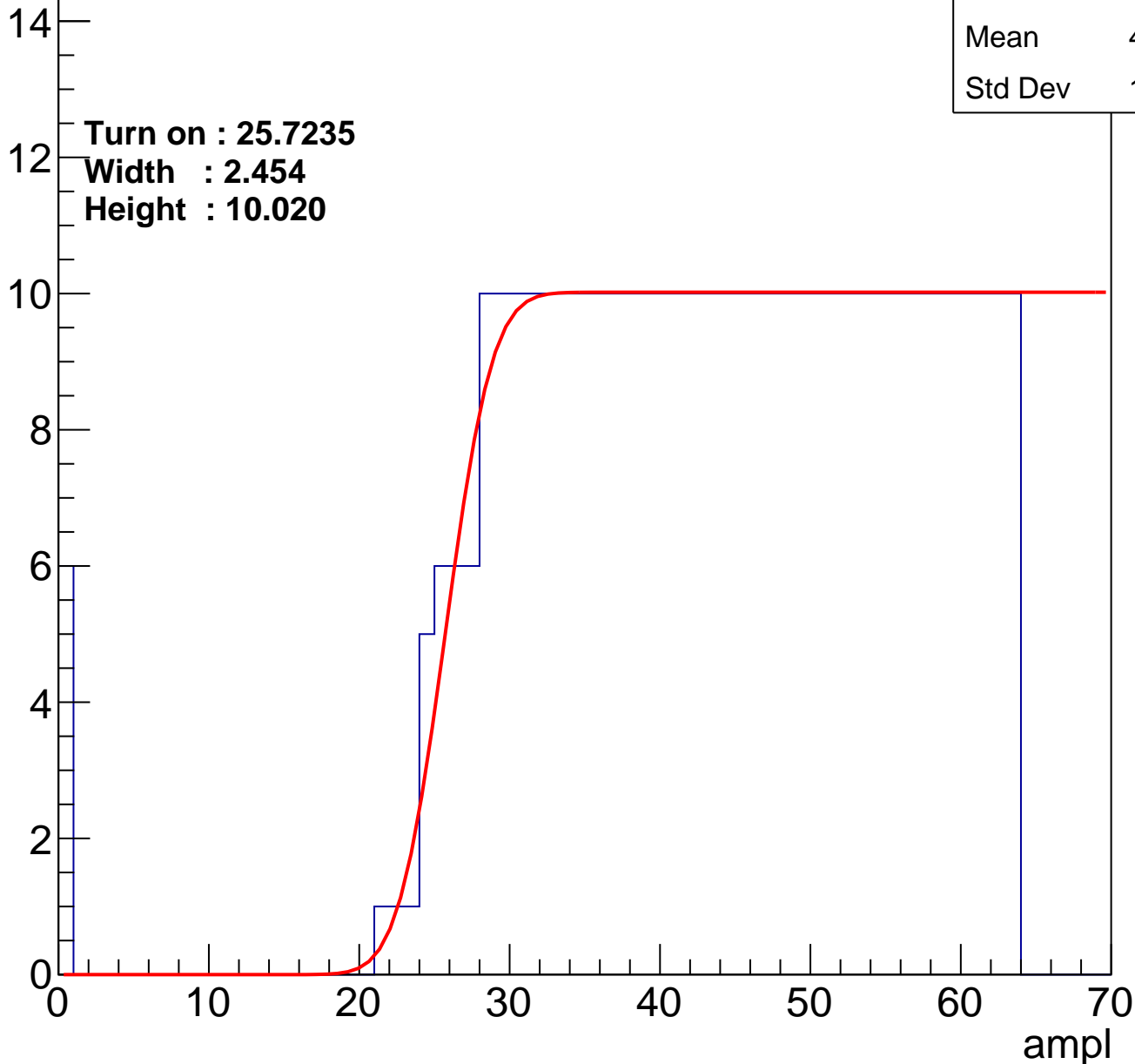
Entries	392
Mean	43.45
Std Dev	12.42

Turn on : 25.7235

Width : 2.454

Height : 10.020

Entry



B1L103S, U1-ch8

calib_packv5_042523_0143.root, FC#7, port C2

Entries	398
Mean	43.33
Std Dev	12.11

Turn on : 24.5836

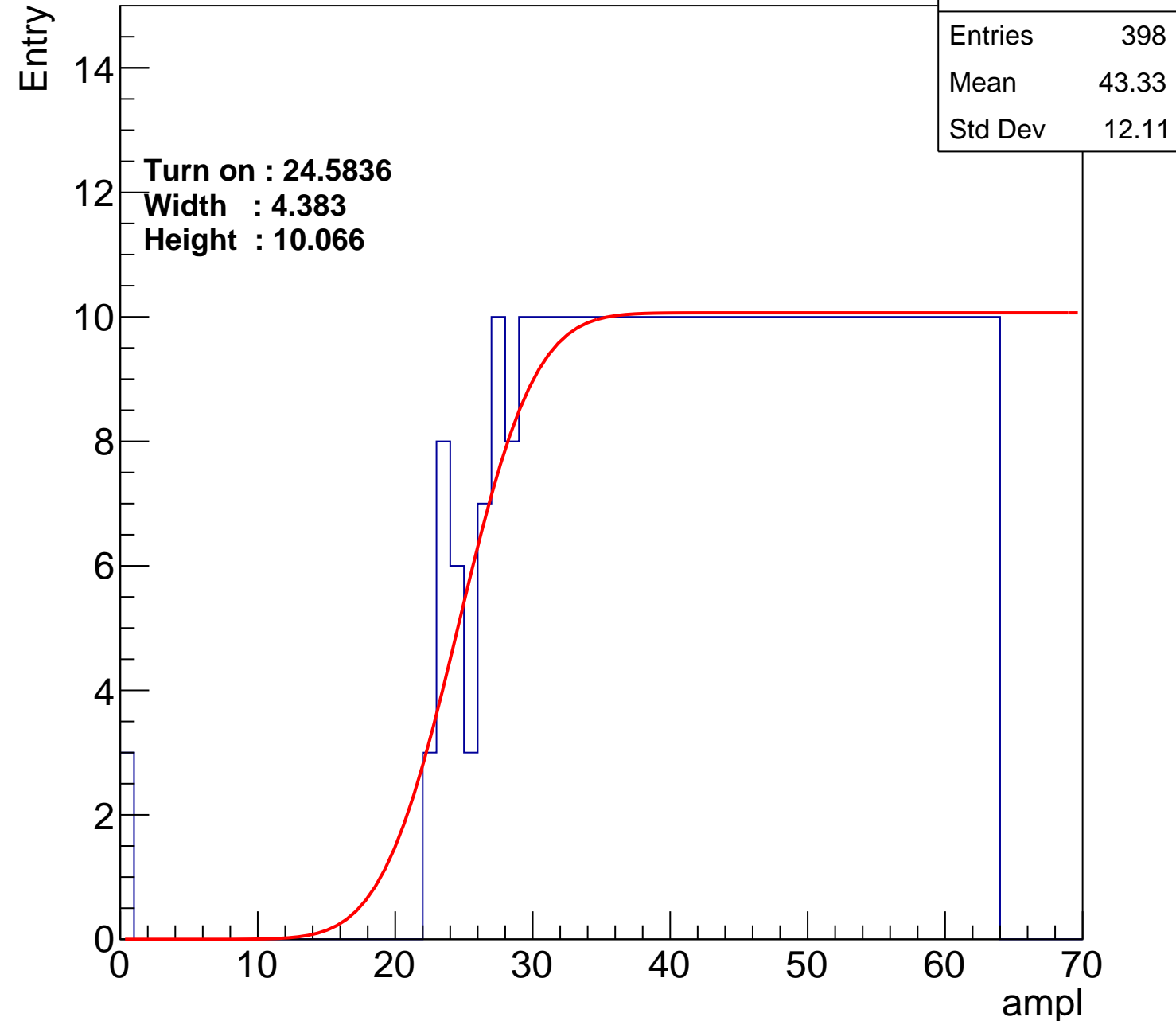
Width : 4.383

Height : 10.066

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch9

calib_packv5_042523_0143.root, FC#7, port C2

Entries	380
Mean	44.21
Std Dev	11.67

Turn on : 26.6777

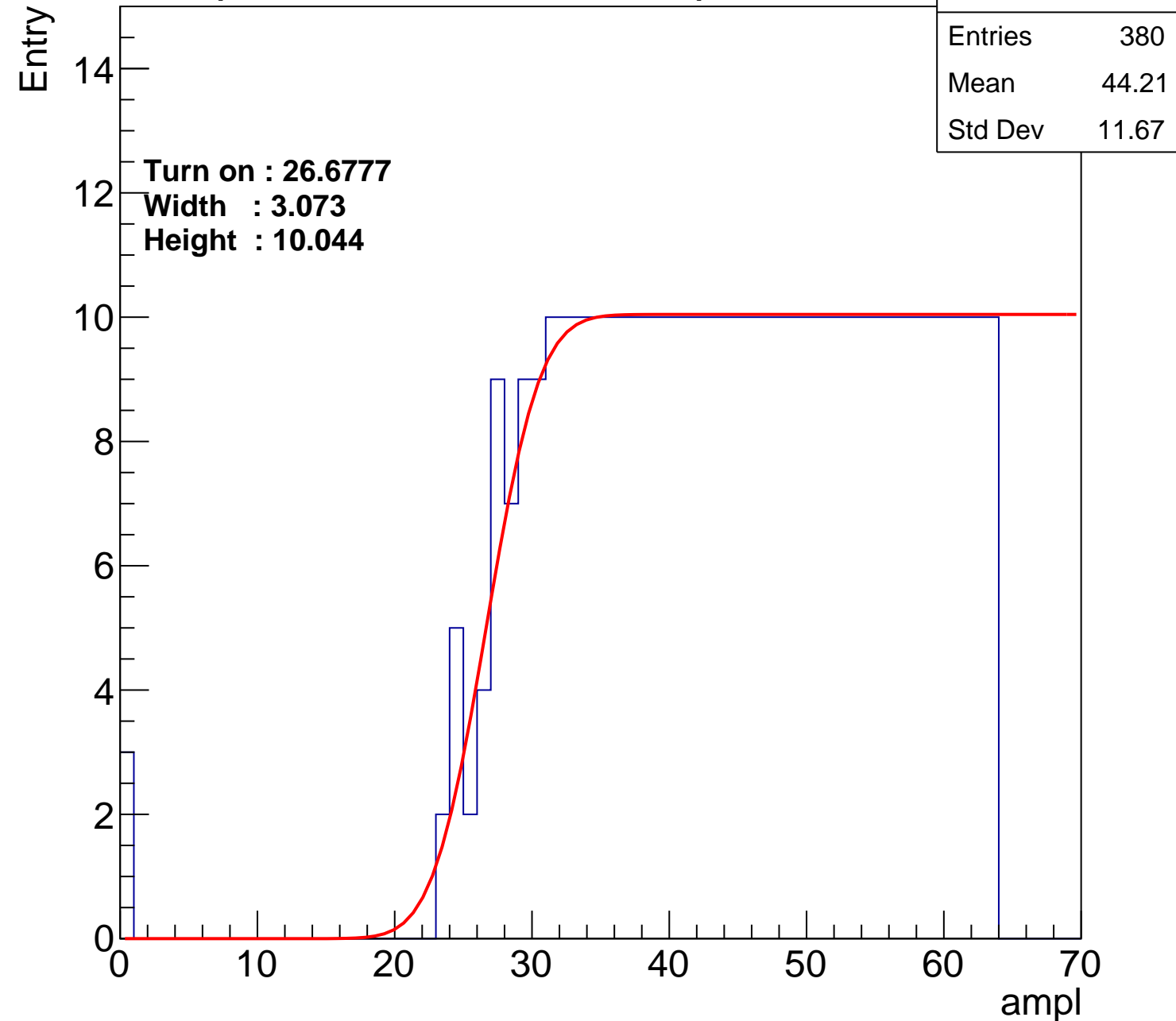
Width : 3.073

Height : 10.044

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch10

calib_packv5_042523_0143.root, FC#7, port C2

Entries	398
Mean	43.24
Std Dev	12.33

Turn on : 24.8965

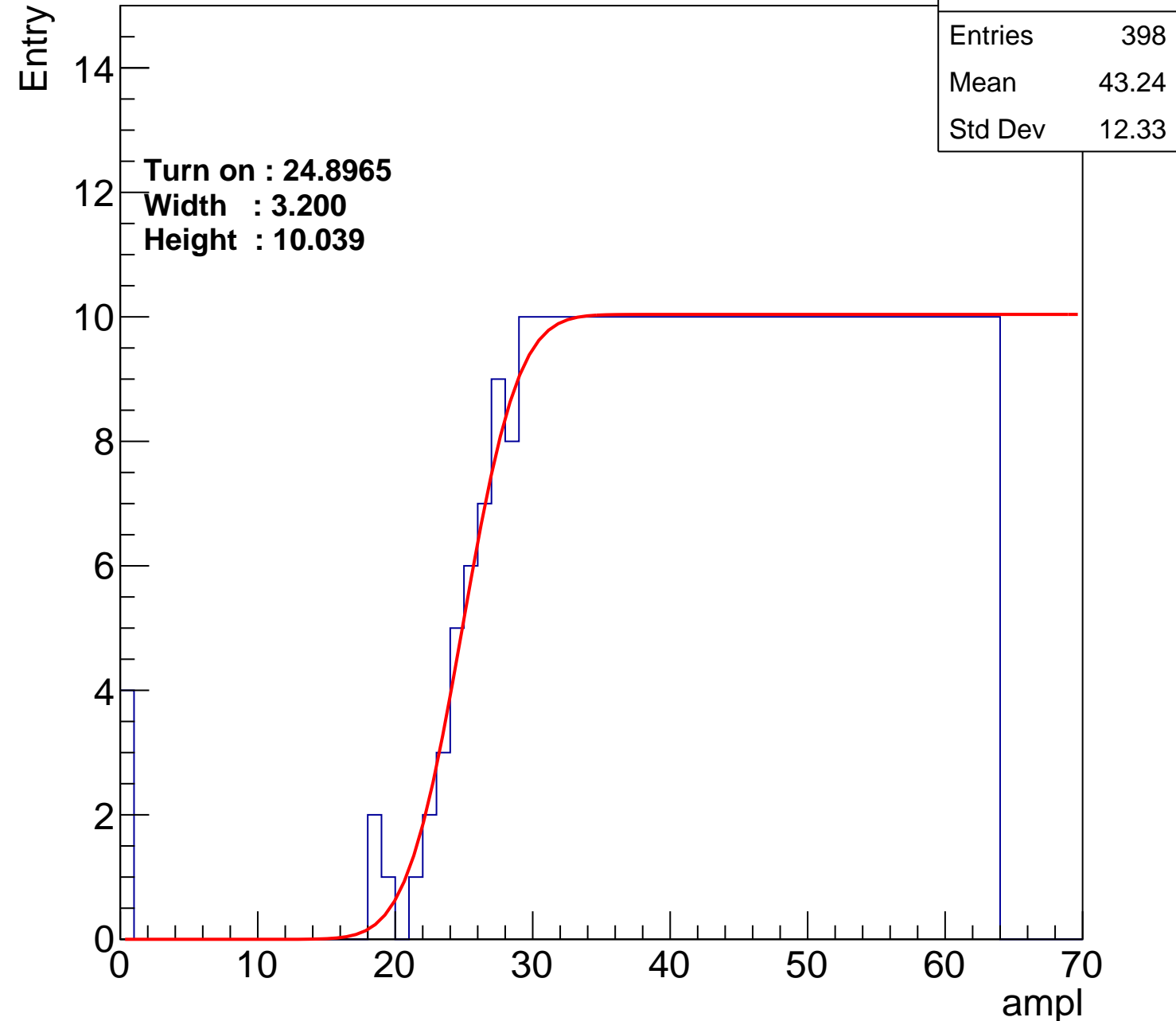
Width : 3.200

Height : 10.039

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch11

calib_packv5_042523_0143.root, FC#7, port C2

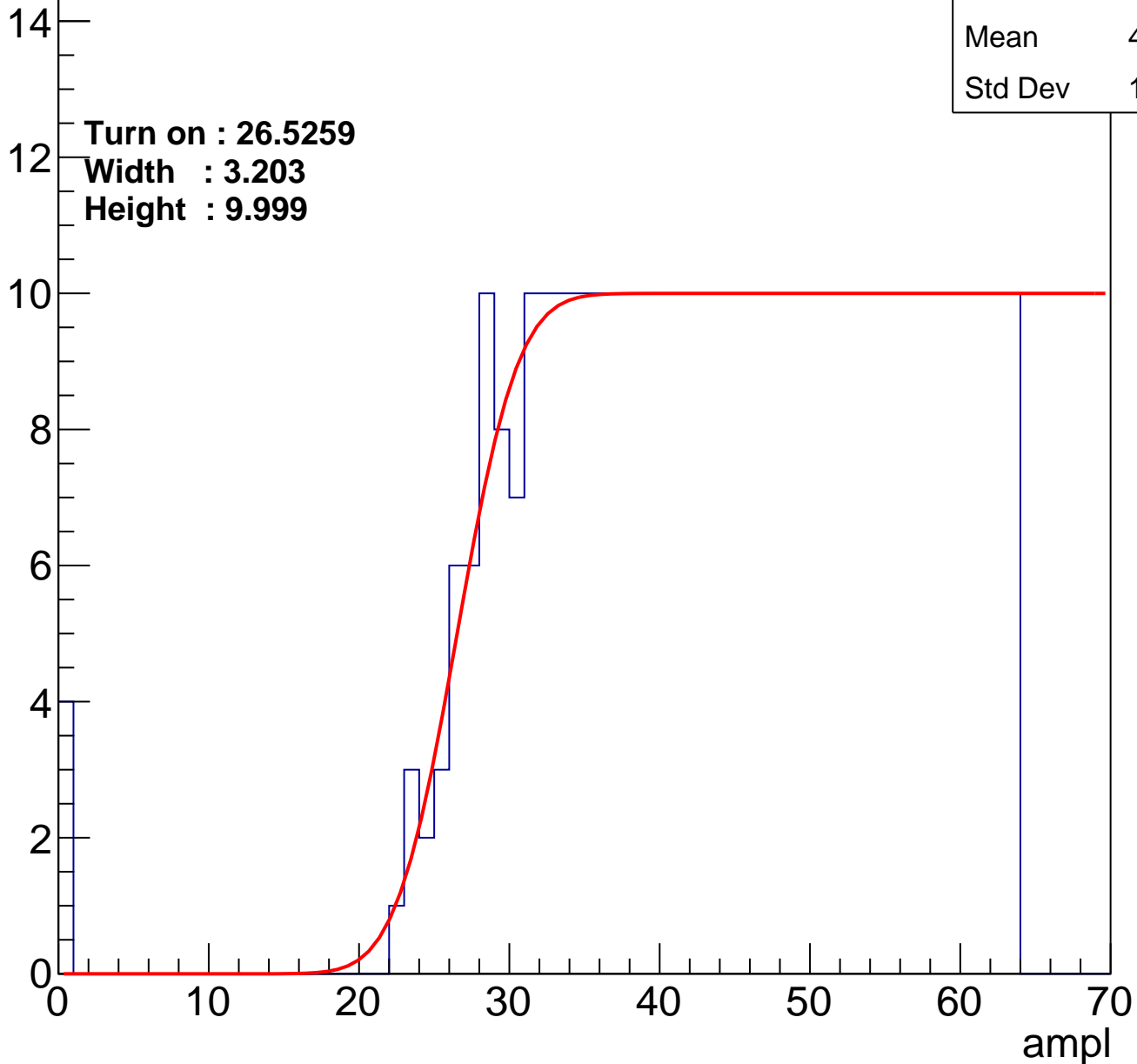
Entries	380
Mean	44.12
Std Dev	11.89

Turn on : 26.5259

Width : 3.203

Height : 9.999

Entry



B1L103S, U1-ch12

calib_packv5_042523_0143.root, FC#7, port C2

Entries	390
Mean	43.77
Std Dev	11.77

Turn on : 25.2589

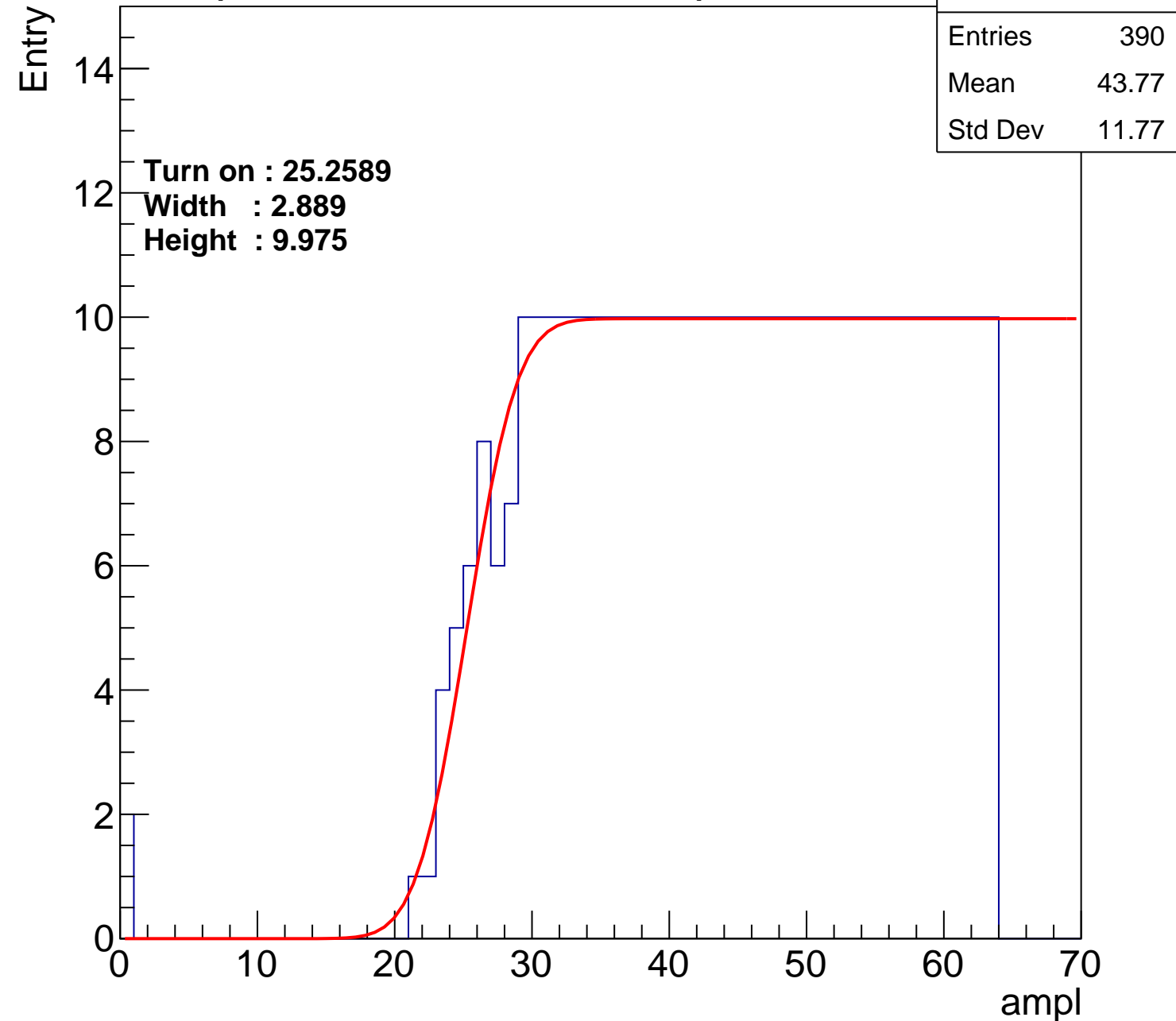
Width : 2.889

Height : 9.975

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch13

calib_packv5_042523_0143.root, FC#7, port C2

Entries	393
Mean	43.12
Std Dev	13.09

Turn on : 26.9747

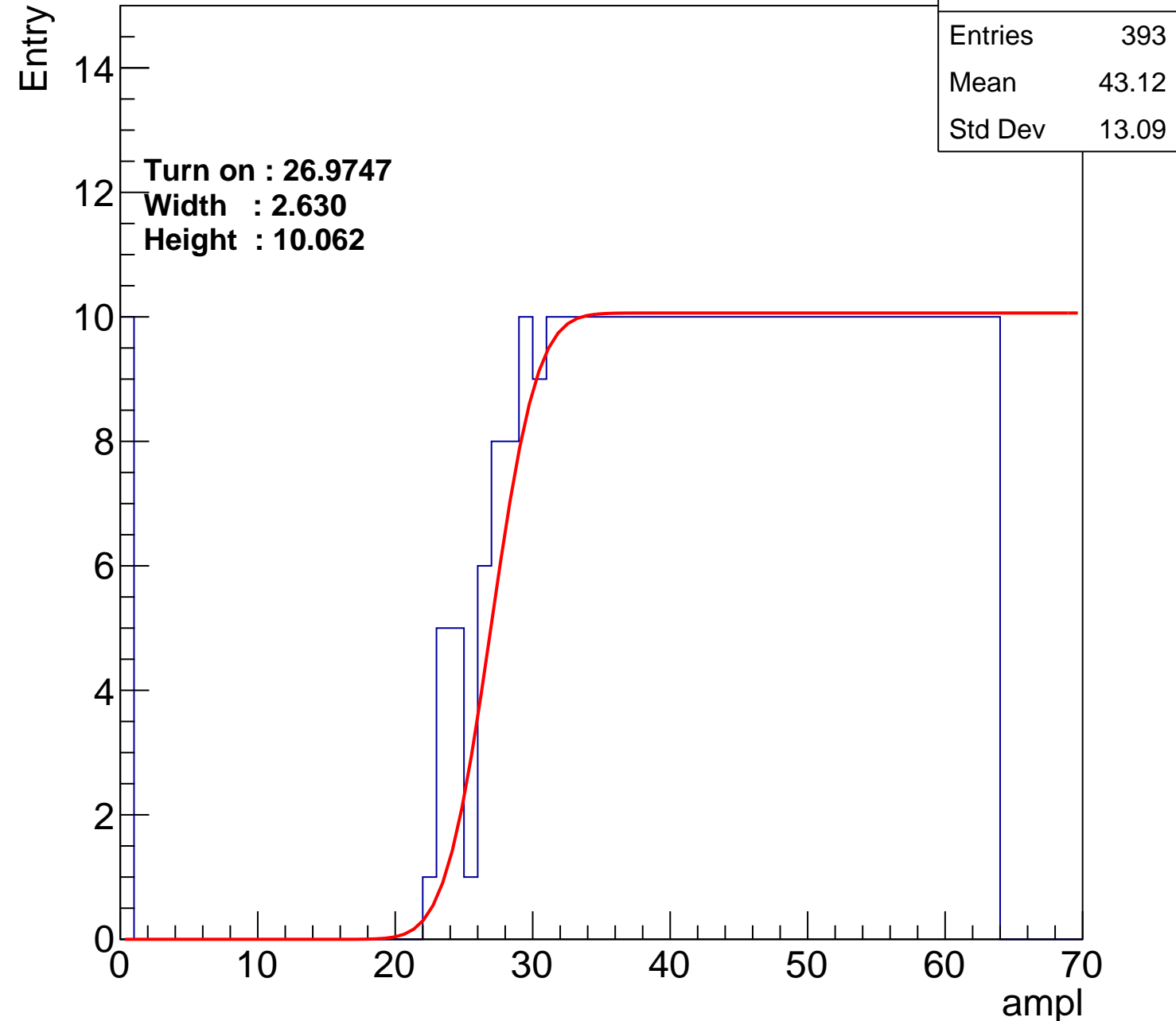
Width : 2.630

Height : 10.062

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch14

calib_packv5_042523_0143.root, FC#7, port C2

Entries	378
Mean	44.33
Std Dev	11.51

Turn on : 26.6076

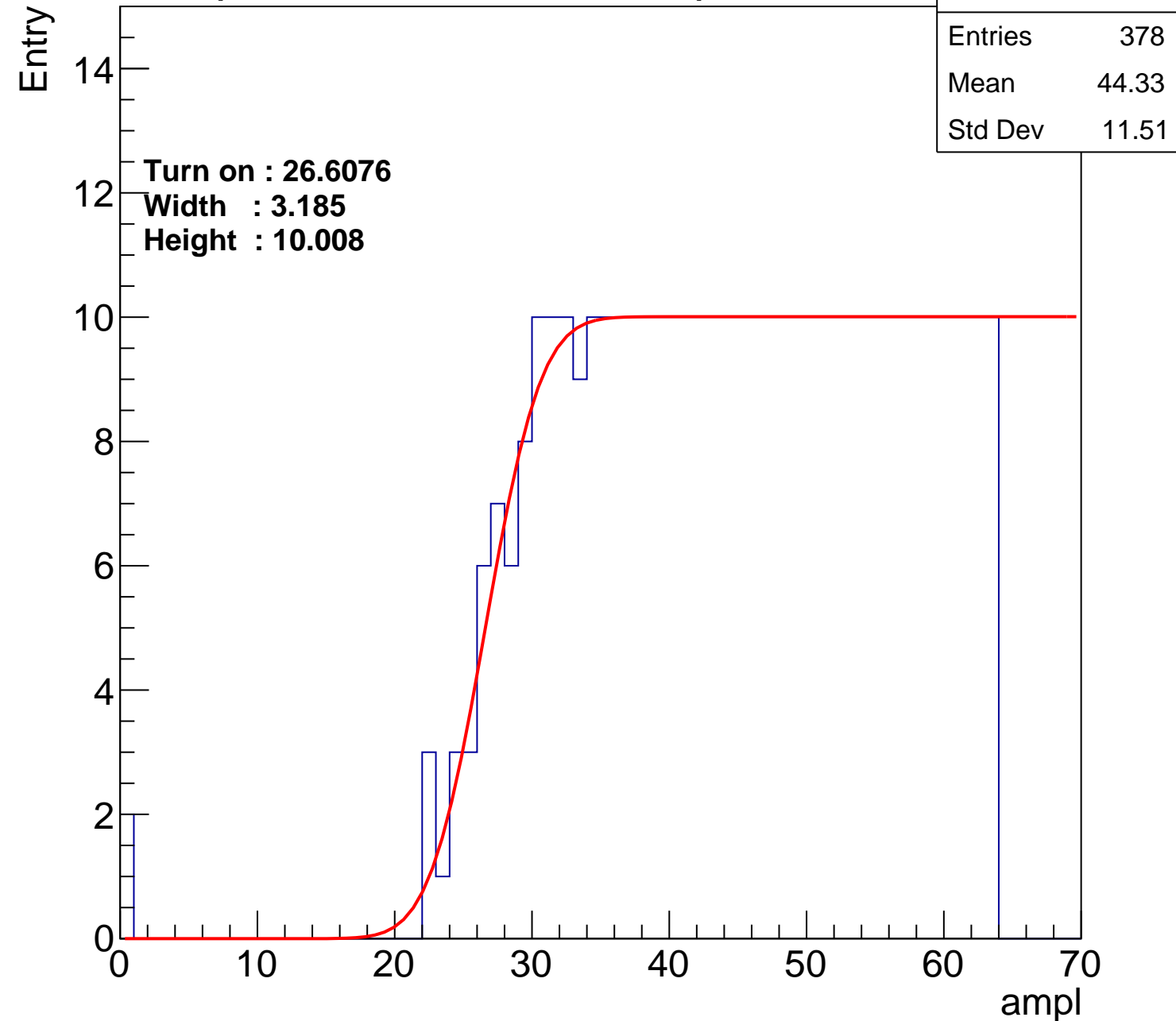
Width : 3.185

Height : 10.008

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch15

calib_packv5_042523_0143.root, FC#7, port C2

Entries	377
Mean	44.44
Std Dev	11.31

Turn on : 26.8286

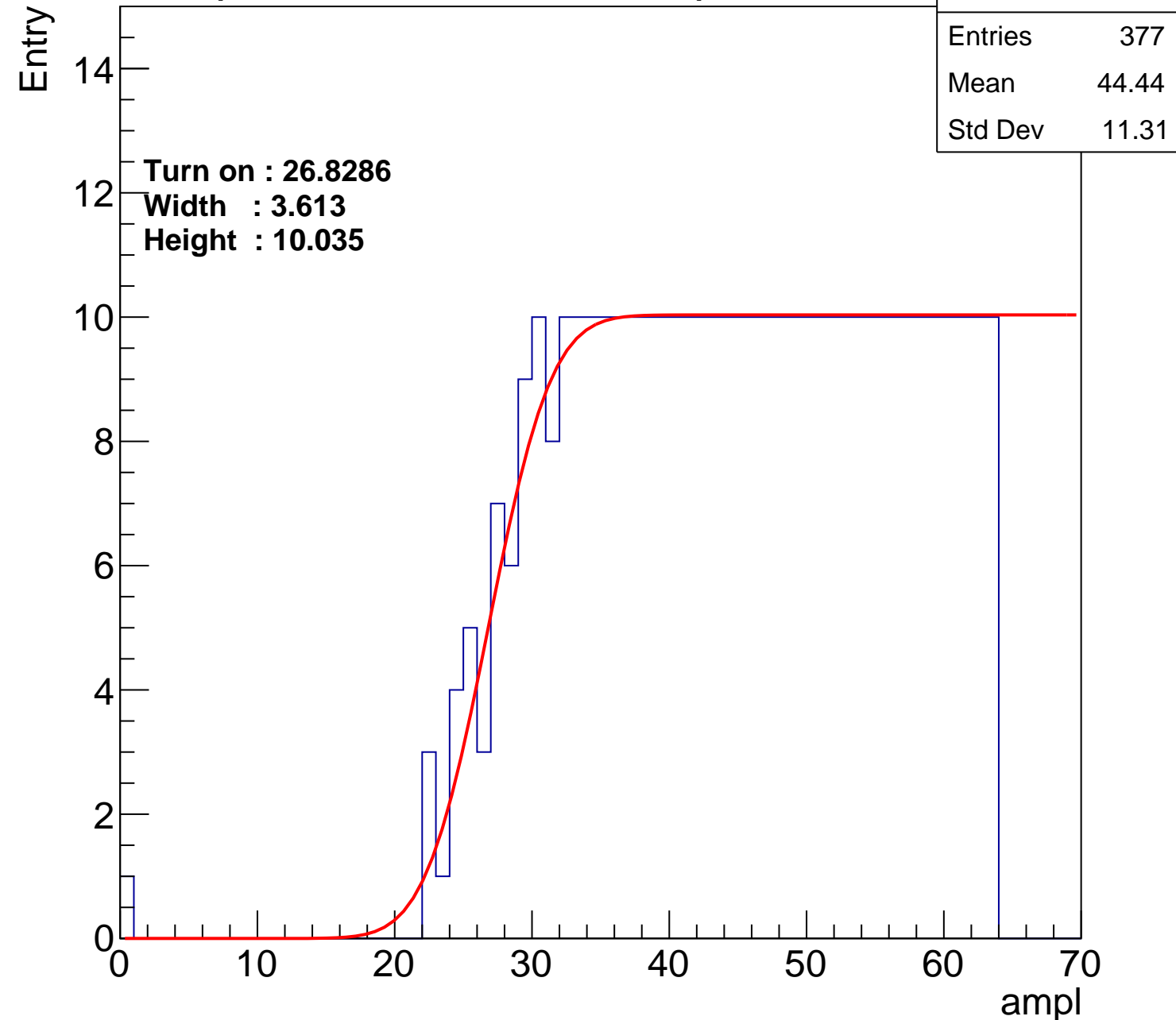
Width : 3.613

Height : 10.035

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch16

calib_packv5_042523_0143.root, FC#7, port C2

Entries	376
Mean	44.11
Std Dev	12.32

Turn on : 27.9208

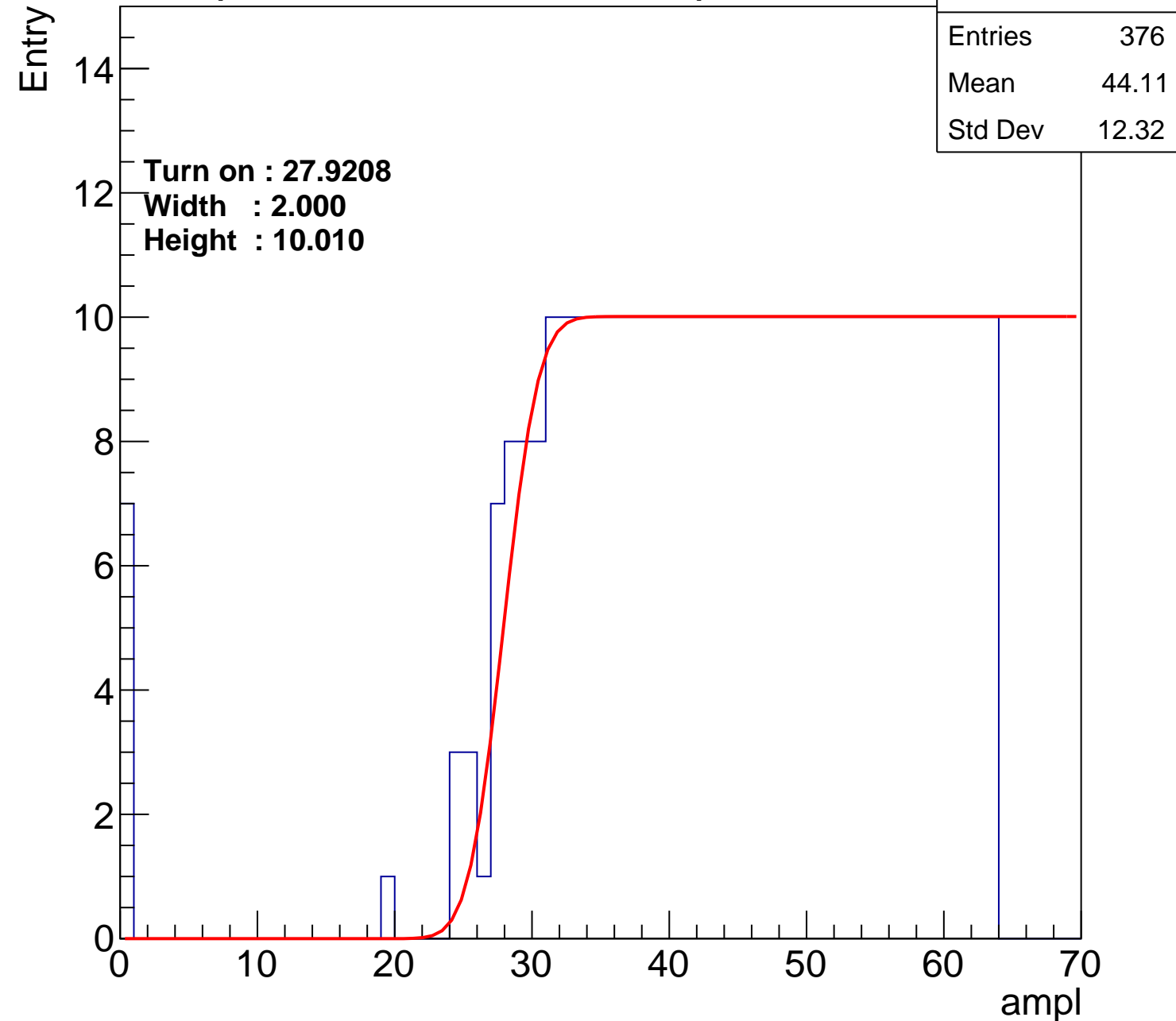
Width : 2.000

Height : 10.010

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch17

calib_packv5_042523_0143.root, FC#7, port C2

Entries	387
Mean	43.86
Std Dev	11.85

Turn on : 25.8896

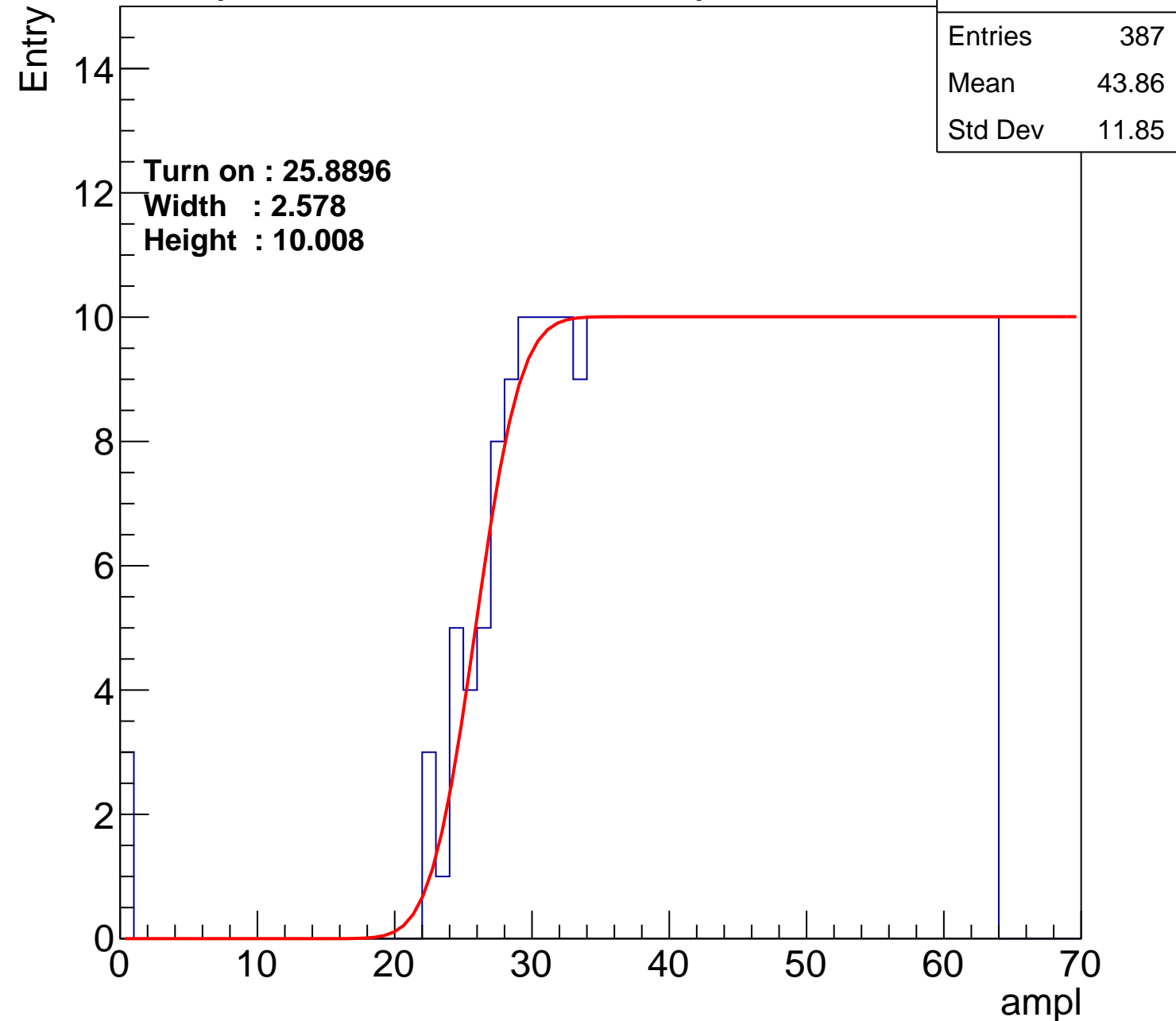
Width : 2.578

Height : 10.008

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch18

calib_packv5_042523_0143.root, FC#7, port C2

Entries	372
Mean	44.43
Std Dev	11.91

Turn on : 27.6390

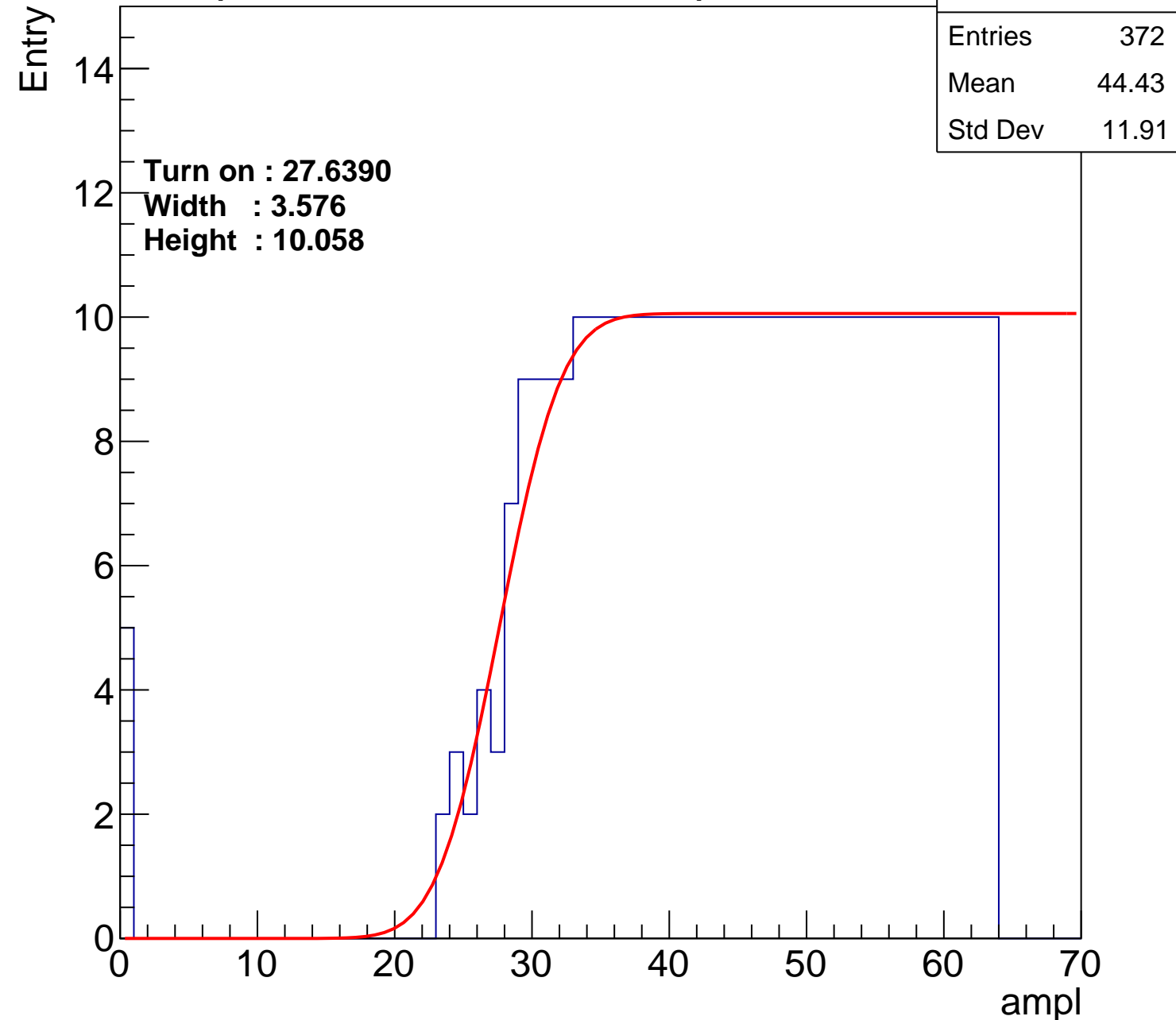
Width : 3.576

Height : 10.058

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch19

calib_packv5_042523_0143.root, FC#7, port C2

Entries	394
Mean	43.48
Std Dev	12.09

Turn on : 25.1804

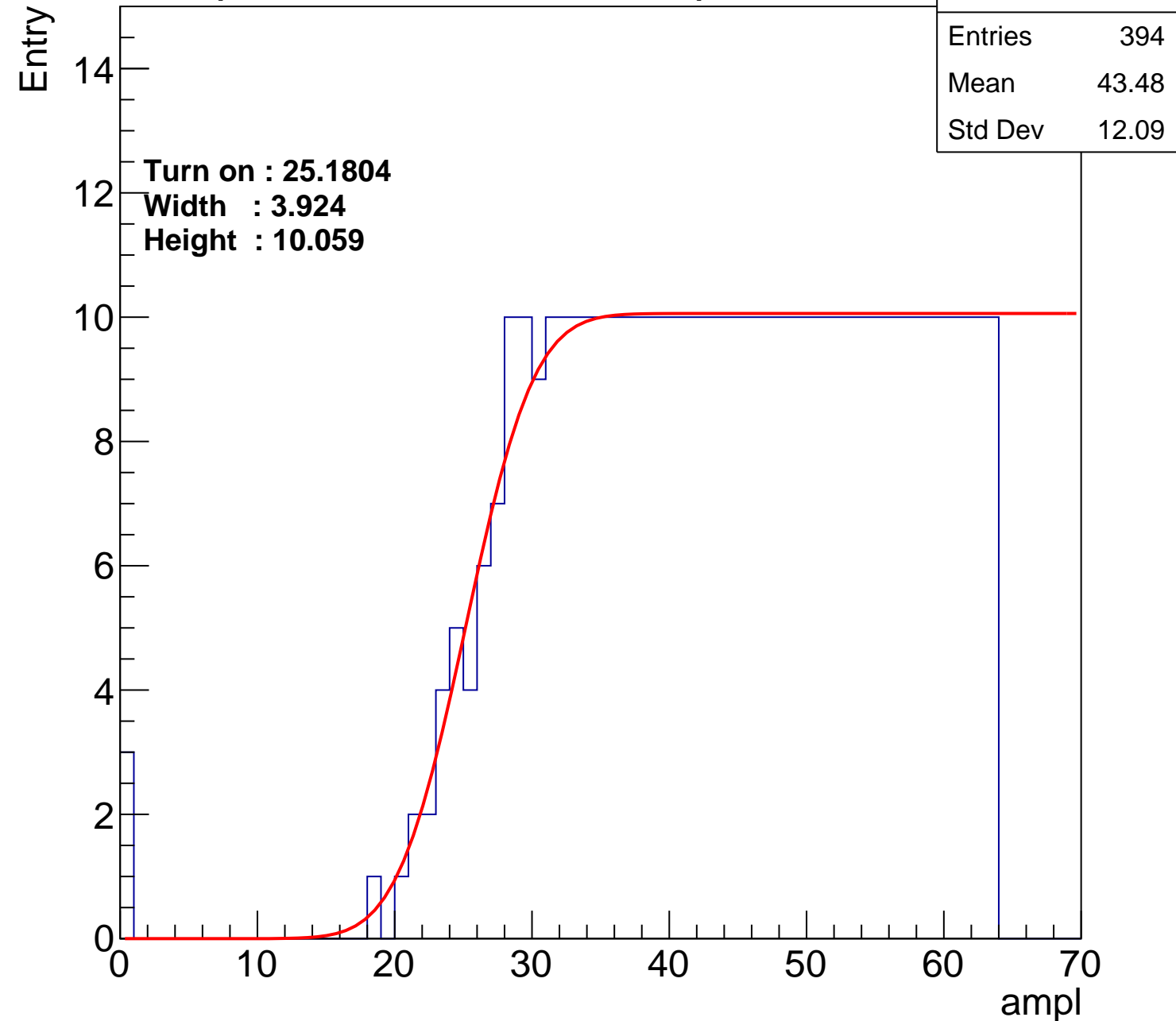
Width : 3.924

Height : 10.059

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch20

calib_packv5_042523_0143.root, FC#7, port C2

Entries	388
Mean	43.57
Std Dev	12.45

Turn on : 25.8381

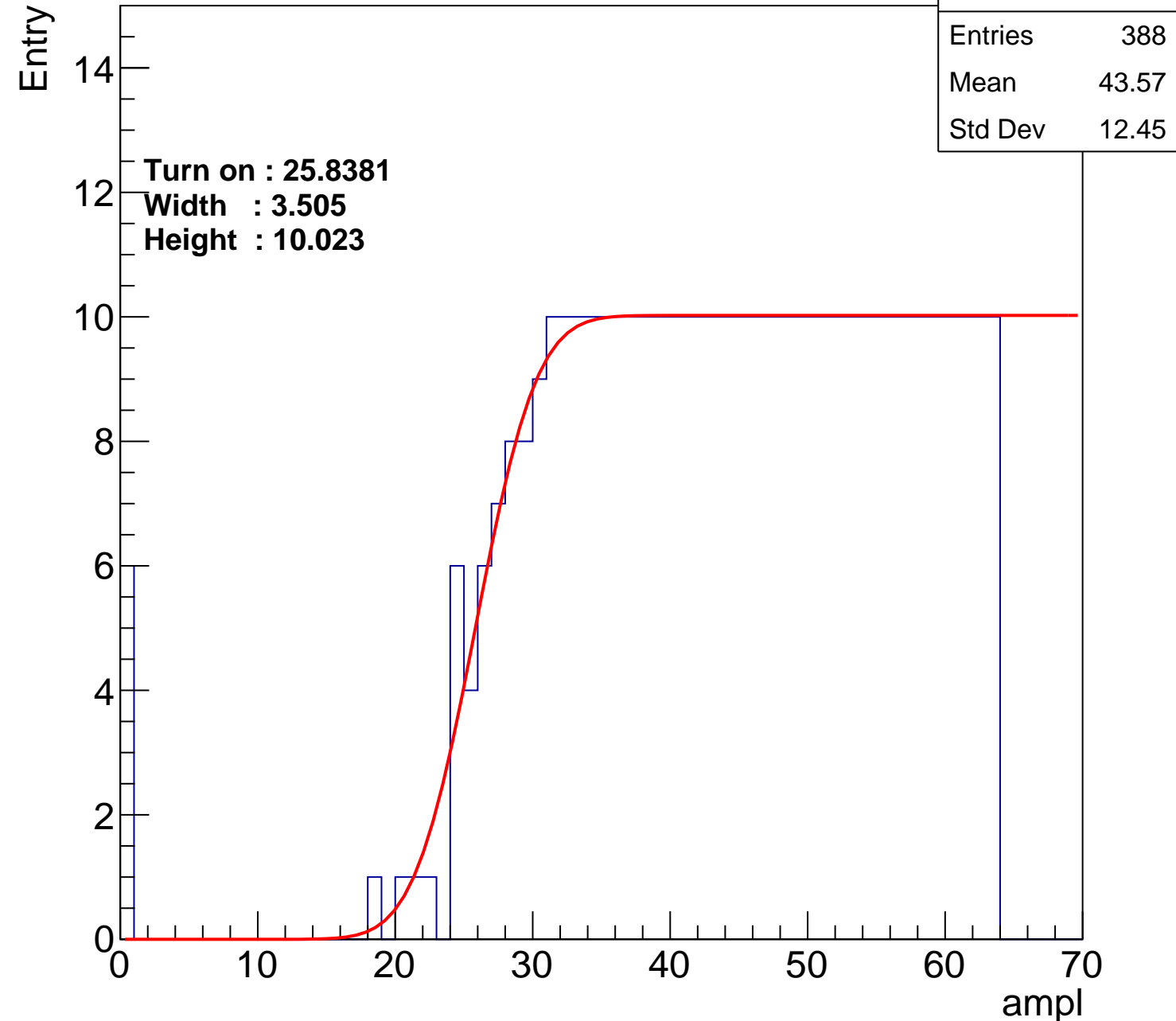
Width : 3.505

Height : 10.023

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch21

calib_packv5_042523_0143.root, FC#7, port C2

Entries	372
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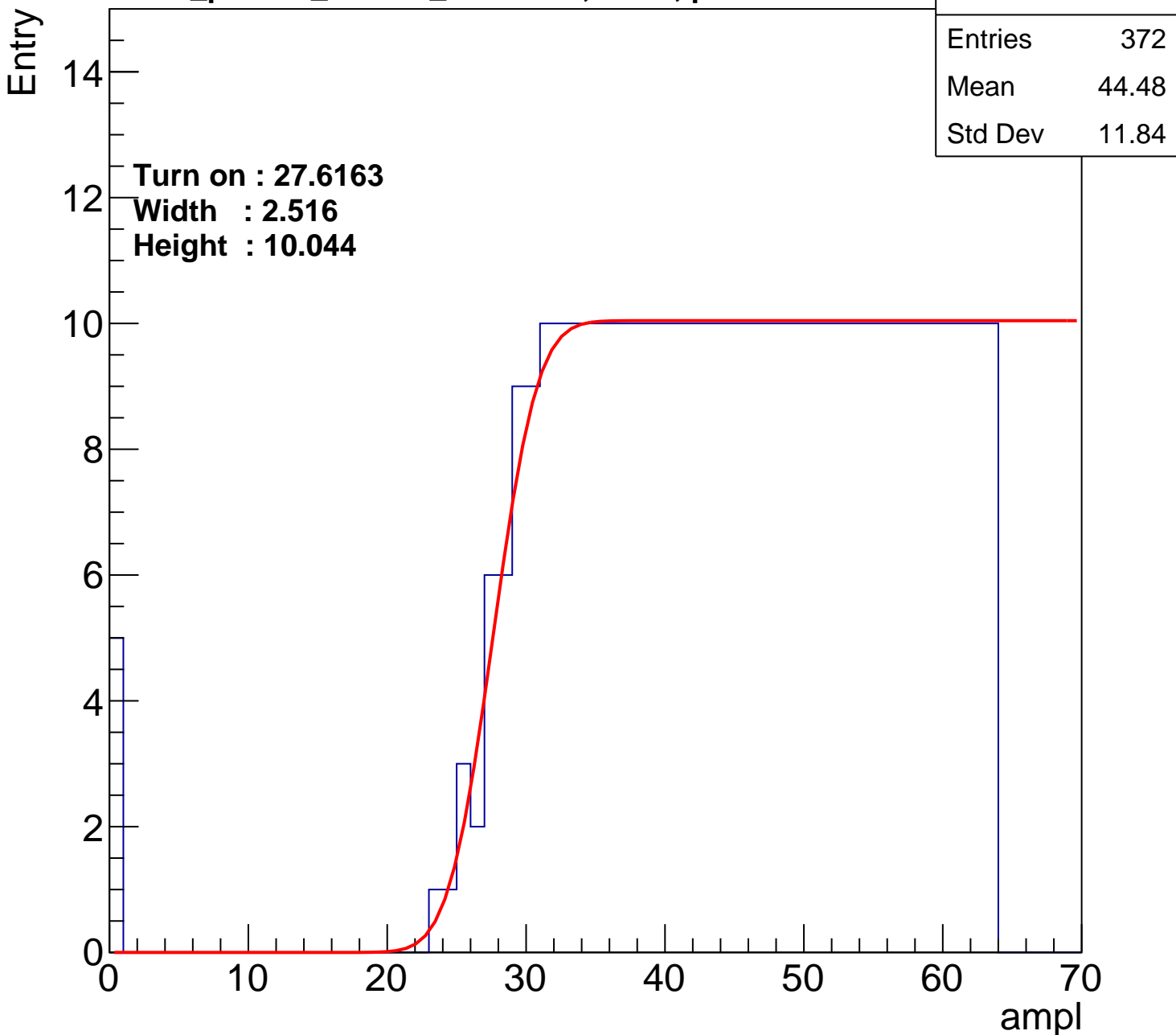
Mean	44.48
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Std Dev	11.84
---------	-------

Turn on : 27.6163

Width : 2.516

Height : 10.044



B1L103S, U1-ch22

calib_packv5_042523_0143.root, FC#7, port C2

Entries	385
Mean	43.89
Std Dev	11.99

Turn on : 26.1715

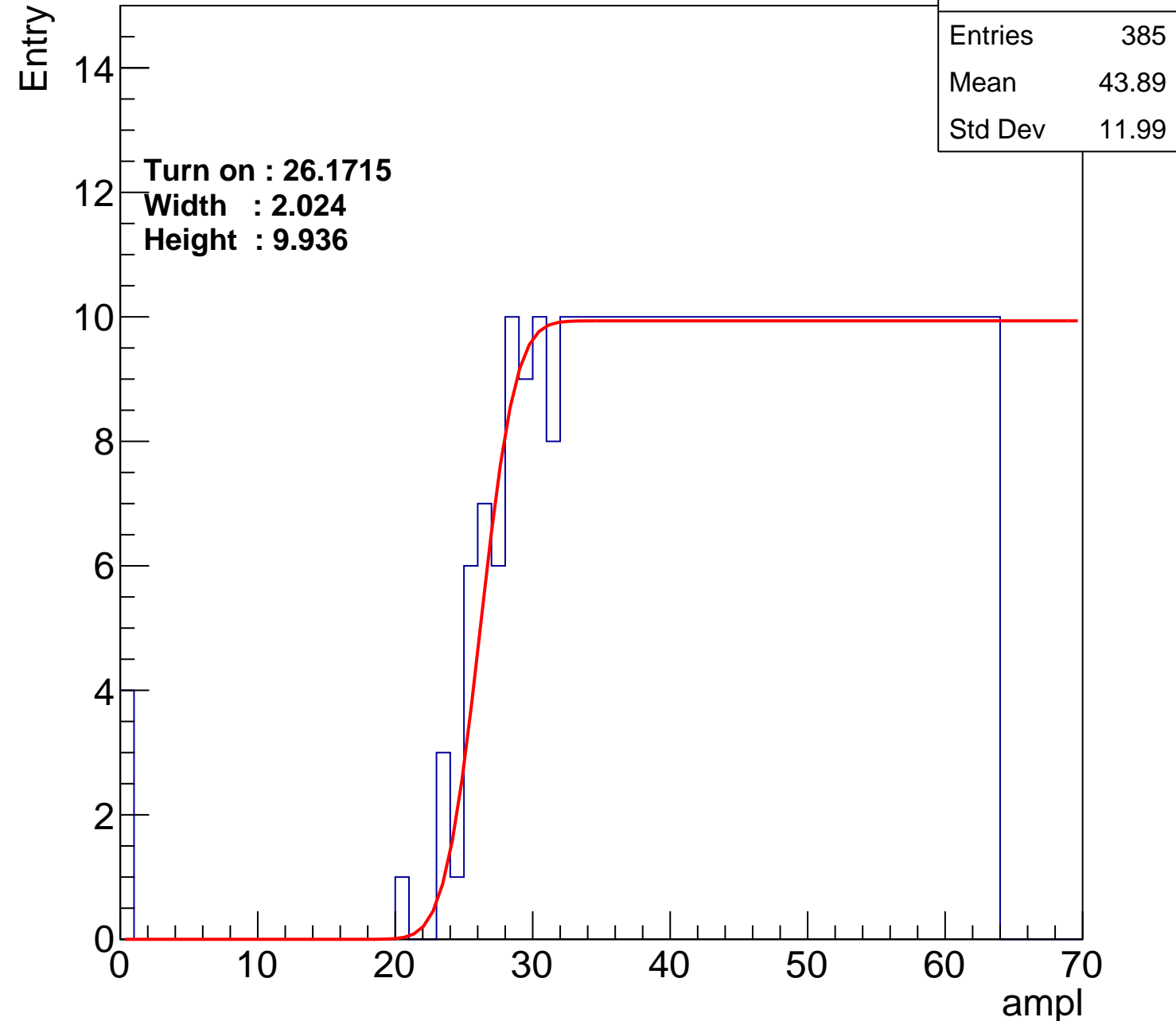
Width : 2.024

Height : 9.936

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch23

calib_packv5_042523_0143.root, FC#7, port C2

Entries	383
Mean	44.13
Std Dev	11.5

Turn on : 26.0116

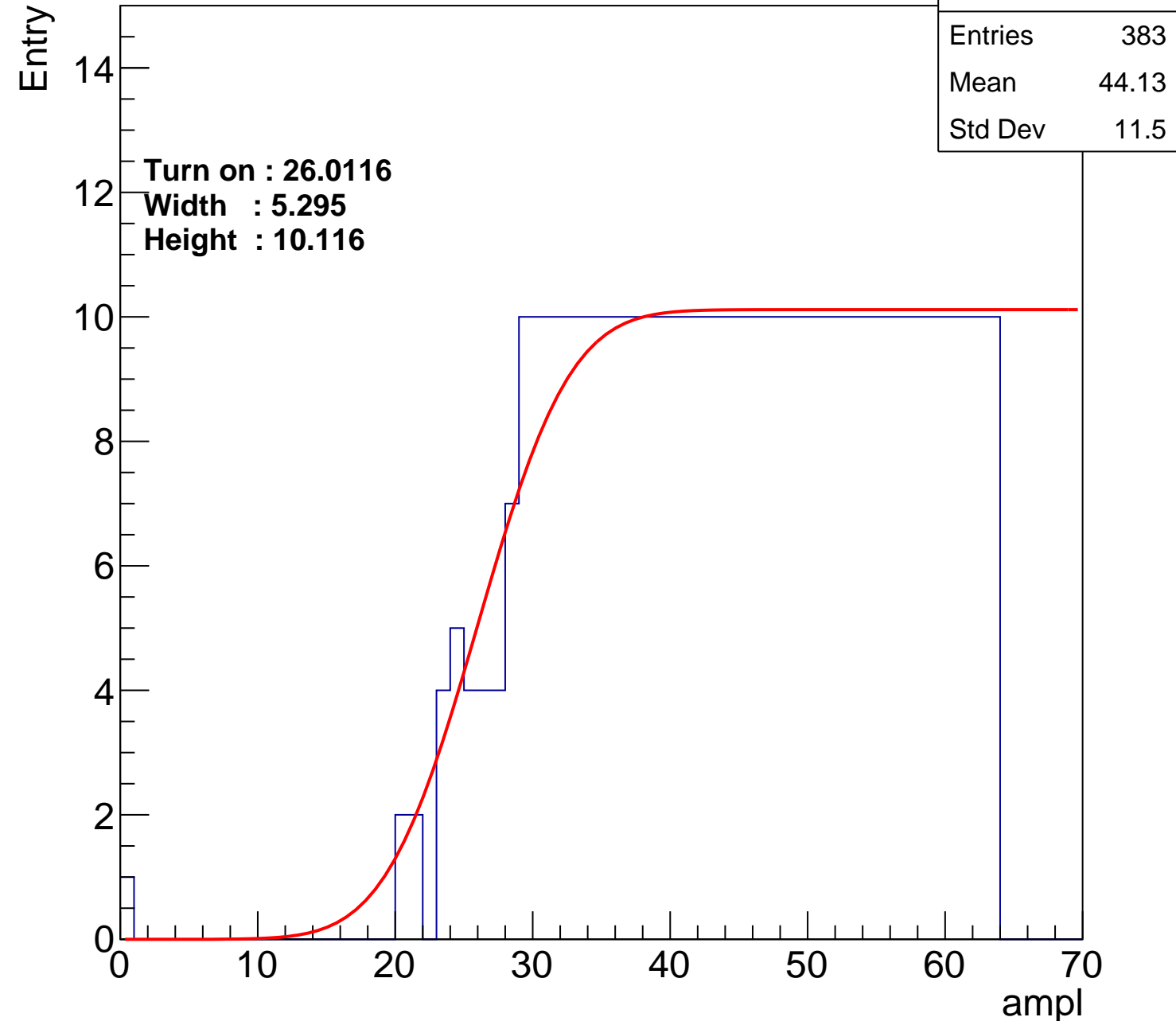
Width : 5.295

Height : 10.116

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch24

calib_packv5_042523_0143.root, FC#7, port C2

Entries	381
Mean	44.04
Std Dev	11.95

Turn on : 26.0039

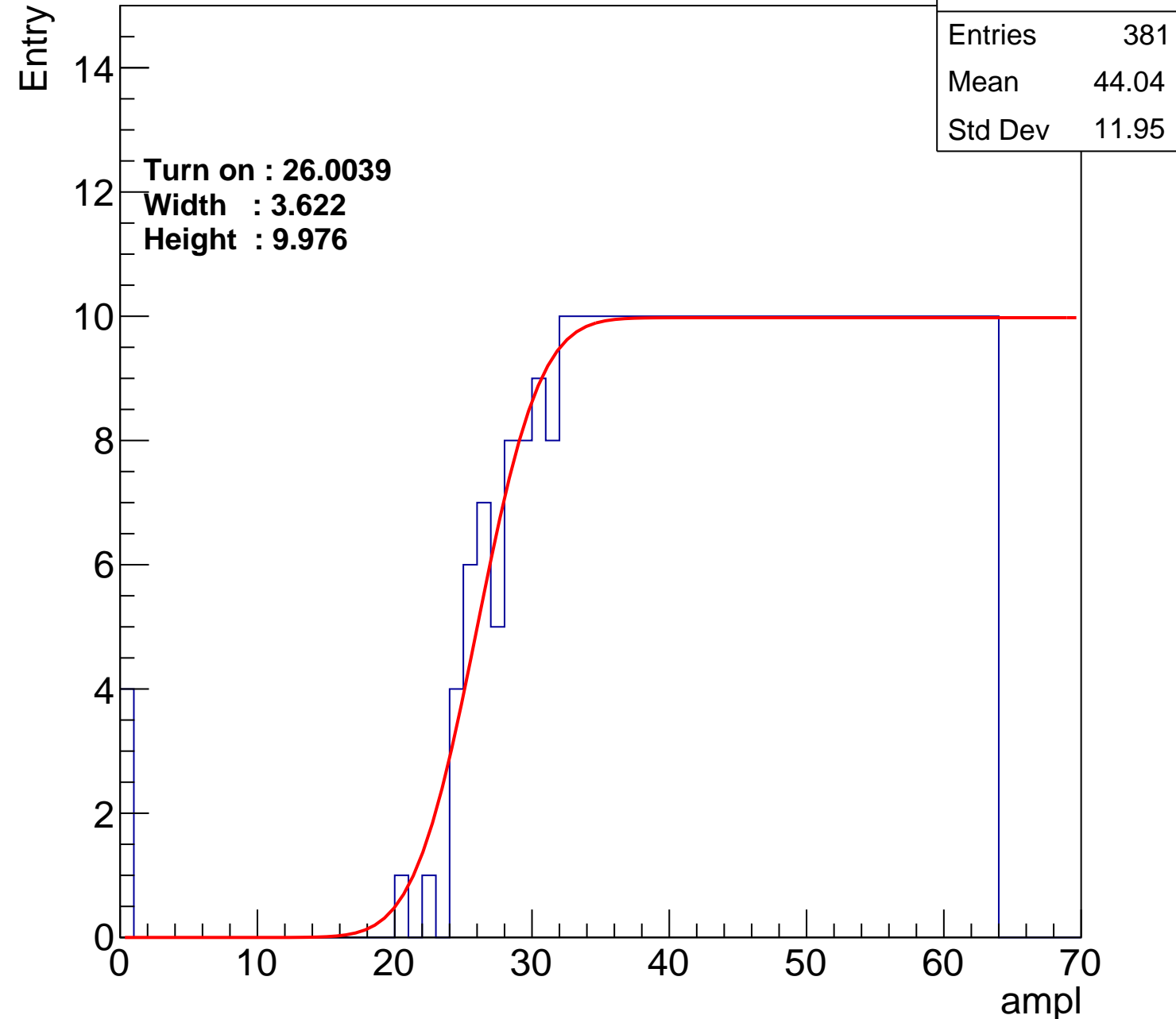
Width : 3.622

Height : 9.976

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch25

calib_packv5_042523_0143.root, FC#7, port C2

Entries	389
Mean	43.71
Std Dev	12.05

Turn on : 25.2484

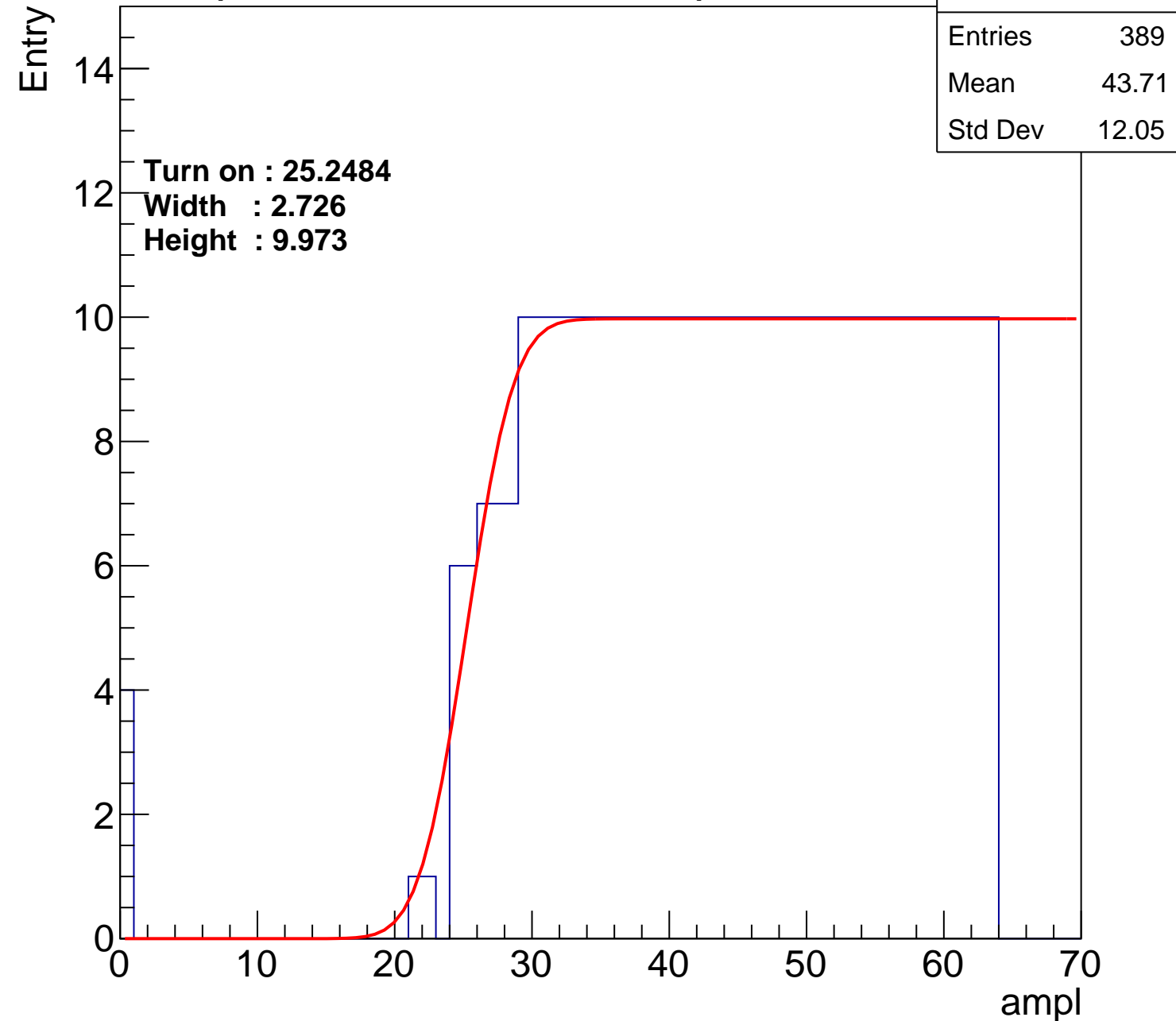
Width : 2.726

Height : 9.973

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch26

calib_packv5_042523_0143.root, FC#7, port C2

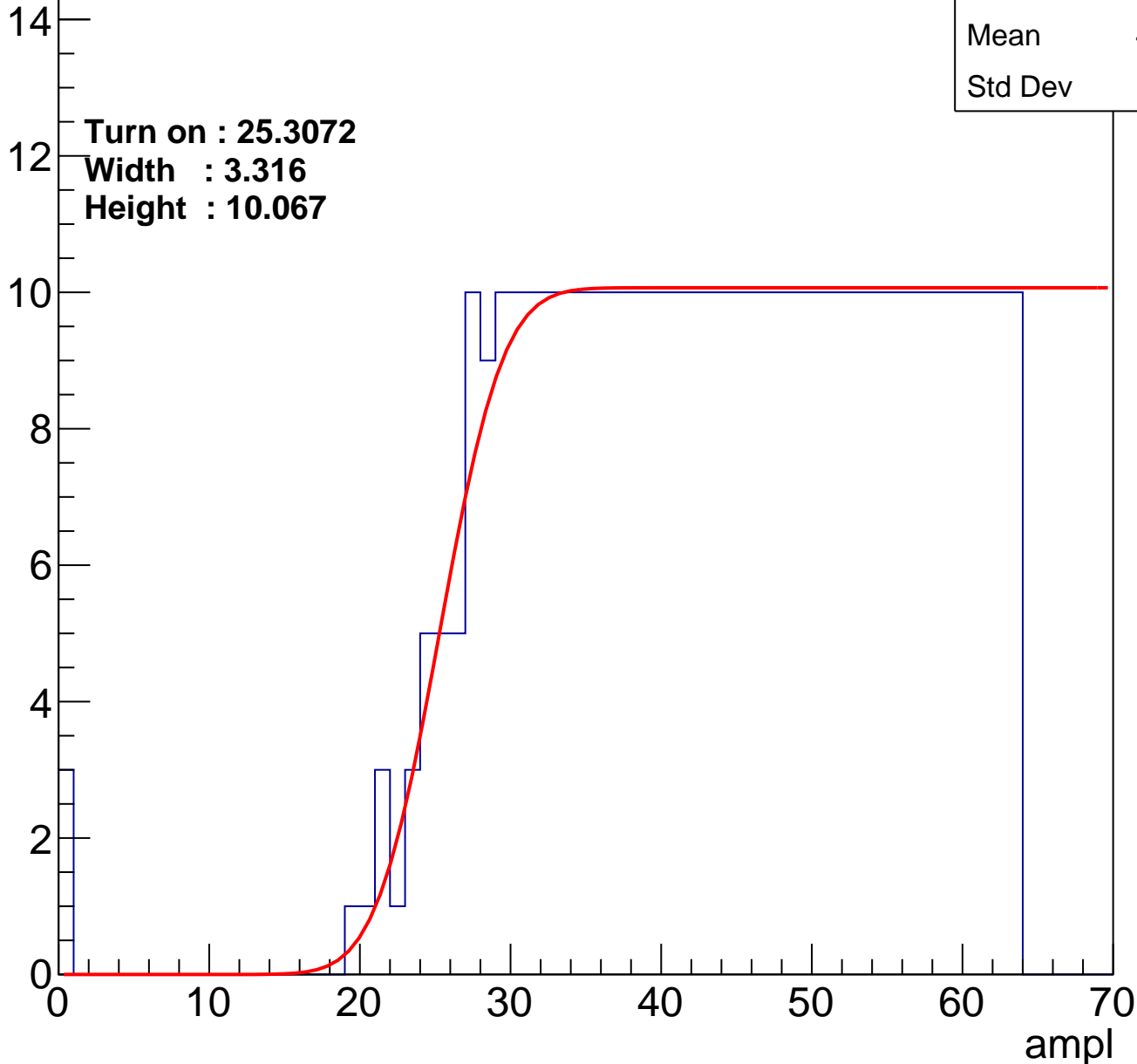
Entries	396
Mean	43.41
Std Dev	12.1

Turn on : 25.3072

Width : 3.316

Height : 10.067

Entry



B1L103S, U1-ch27

calib_packv5_042523_0143.root, FC#7, port C2

Entries	367
Mean	44.98
Std Dev	10.96

Turn on : 28.0703

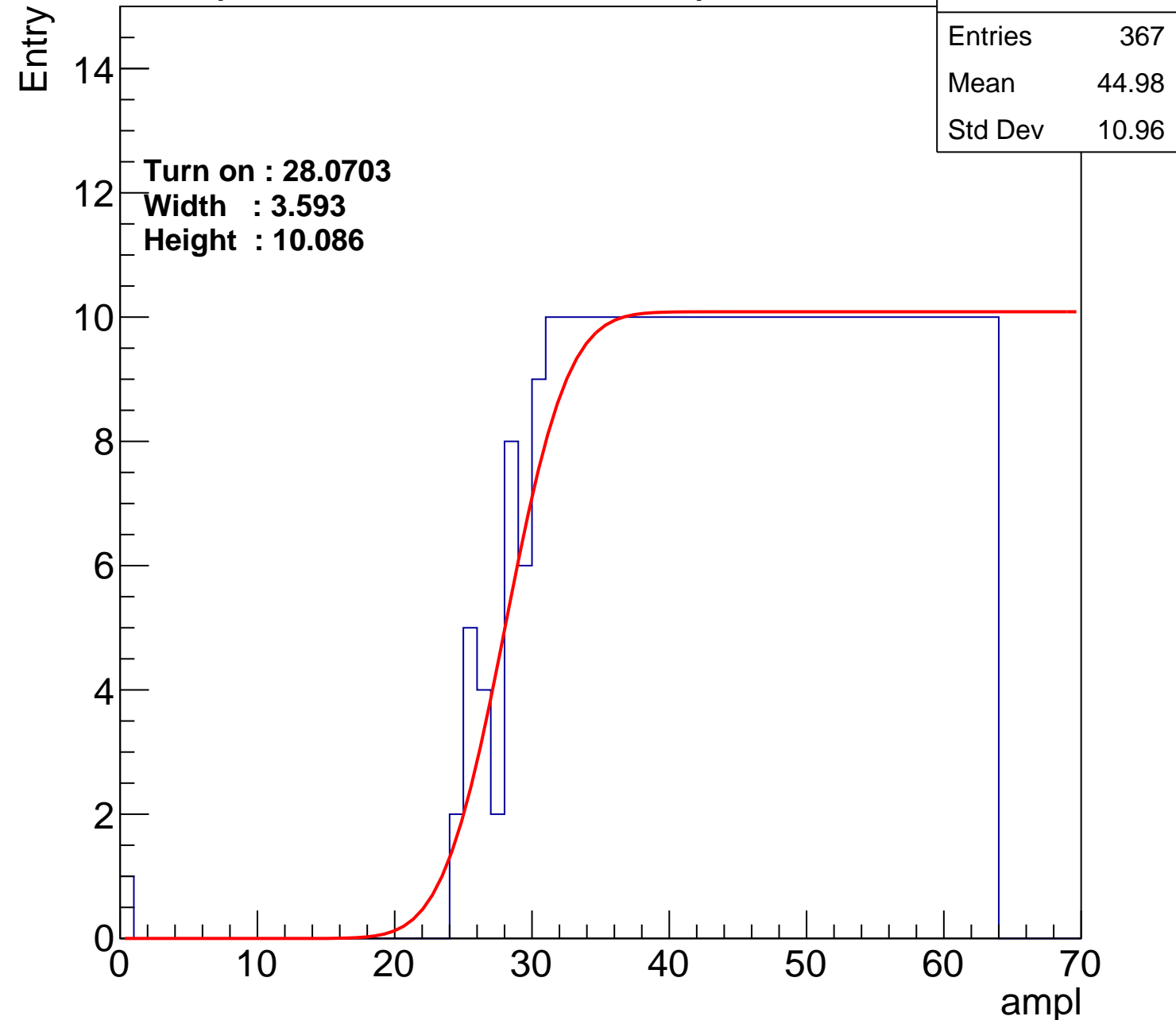
Width : 3.593

Height : 10.086

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch28

calib_packv5_042523_0143.root, FC#7, port C2

Entries	401
Mean	43.18
Std Dev	12.2

Turn on : 24.7371

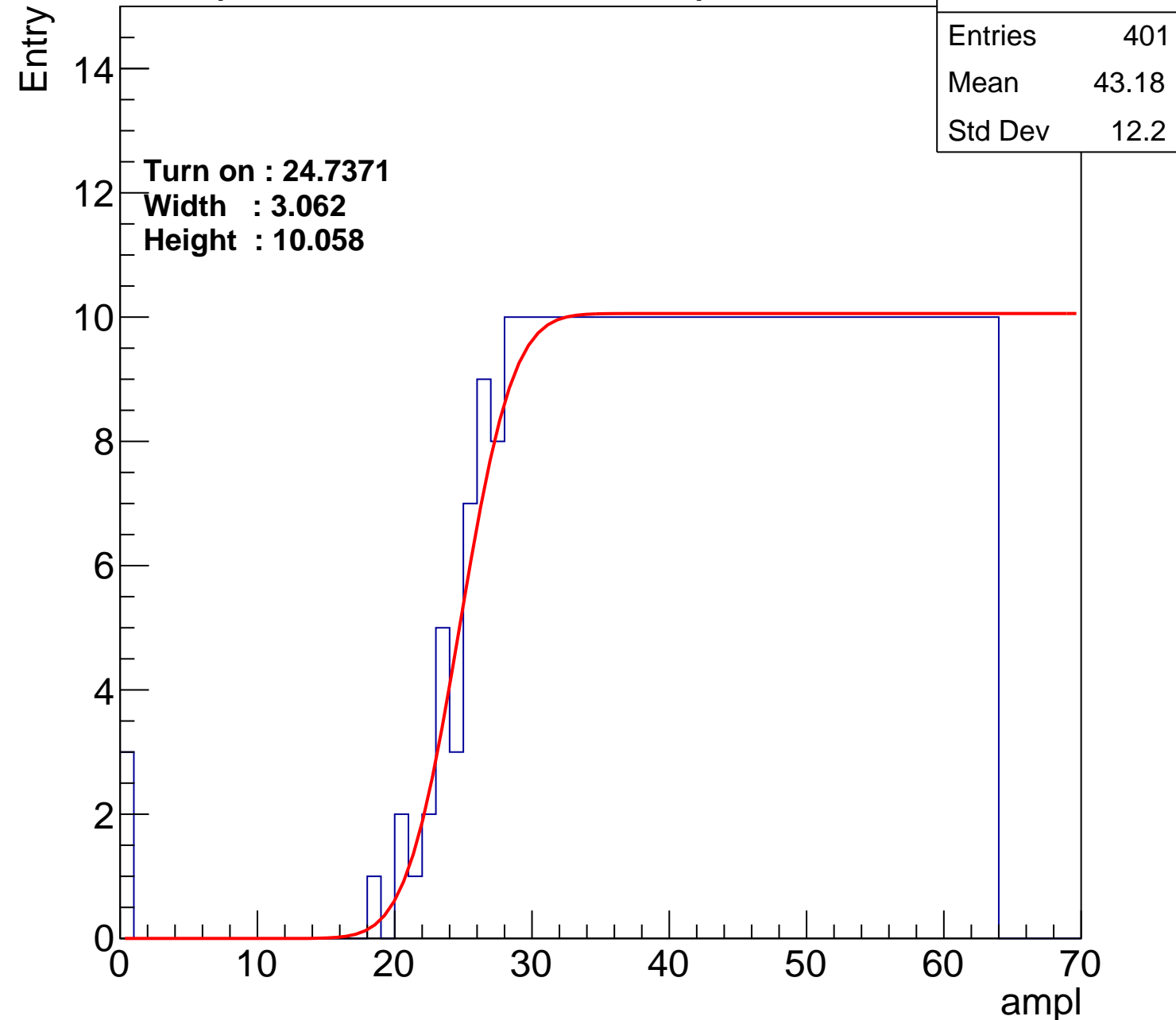
Width : 3.062

Height : 10.058

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch29

calib_packv5_042523_0143.root, FC#7, port C2

Entries	375
Mean	44.61
Std Dev	11.13

Turn on : 26.8158

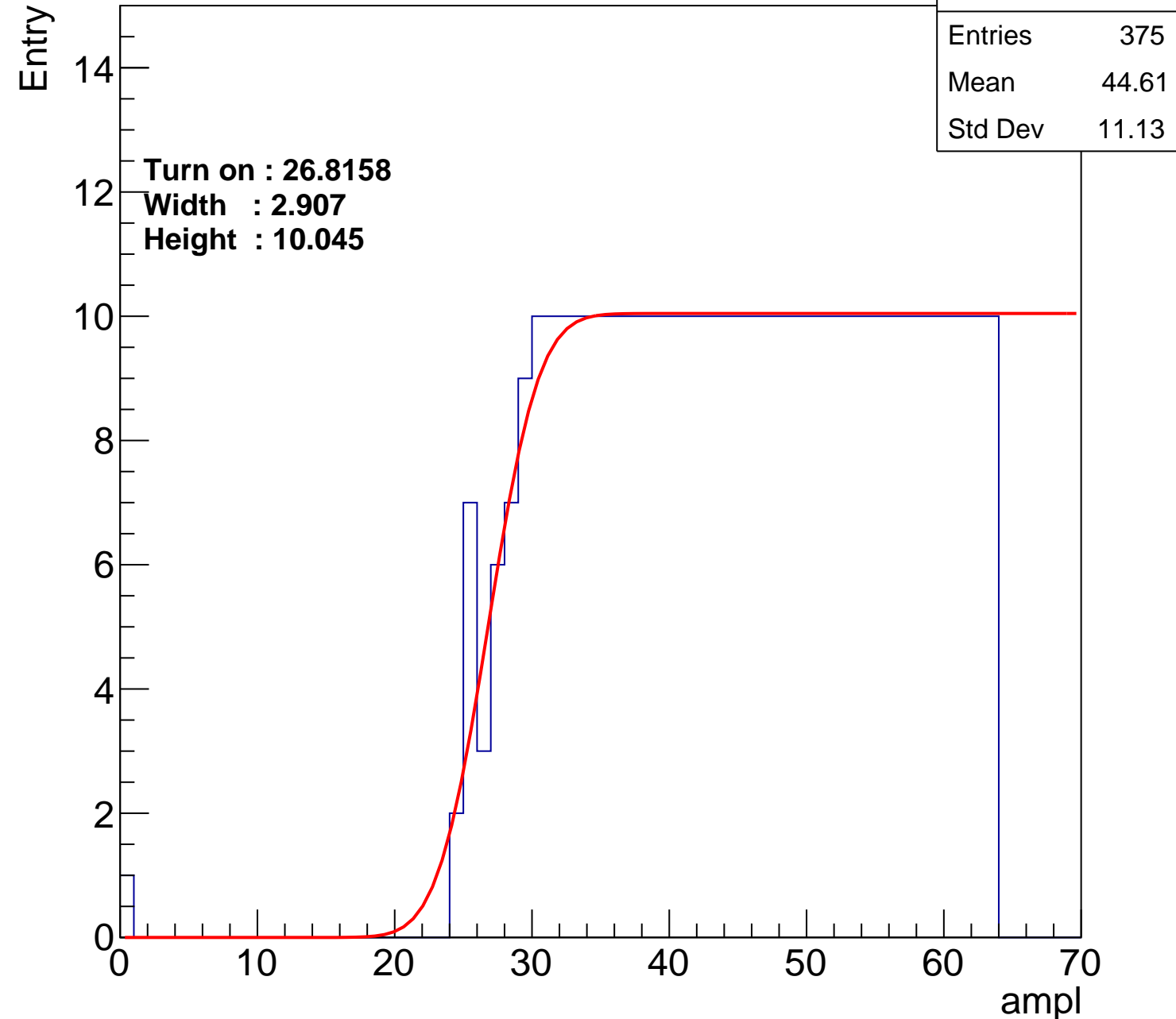
Width : 2.907

Height : 10.045

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch30

calib_packv5_042523_0143.root, FC#7, port C2

Entries	407
Mean	42.73
Std Dev	12.69

Turn on : 23.8799

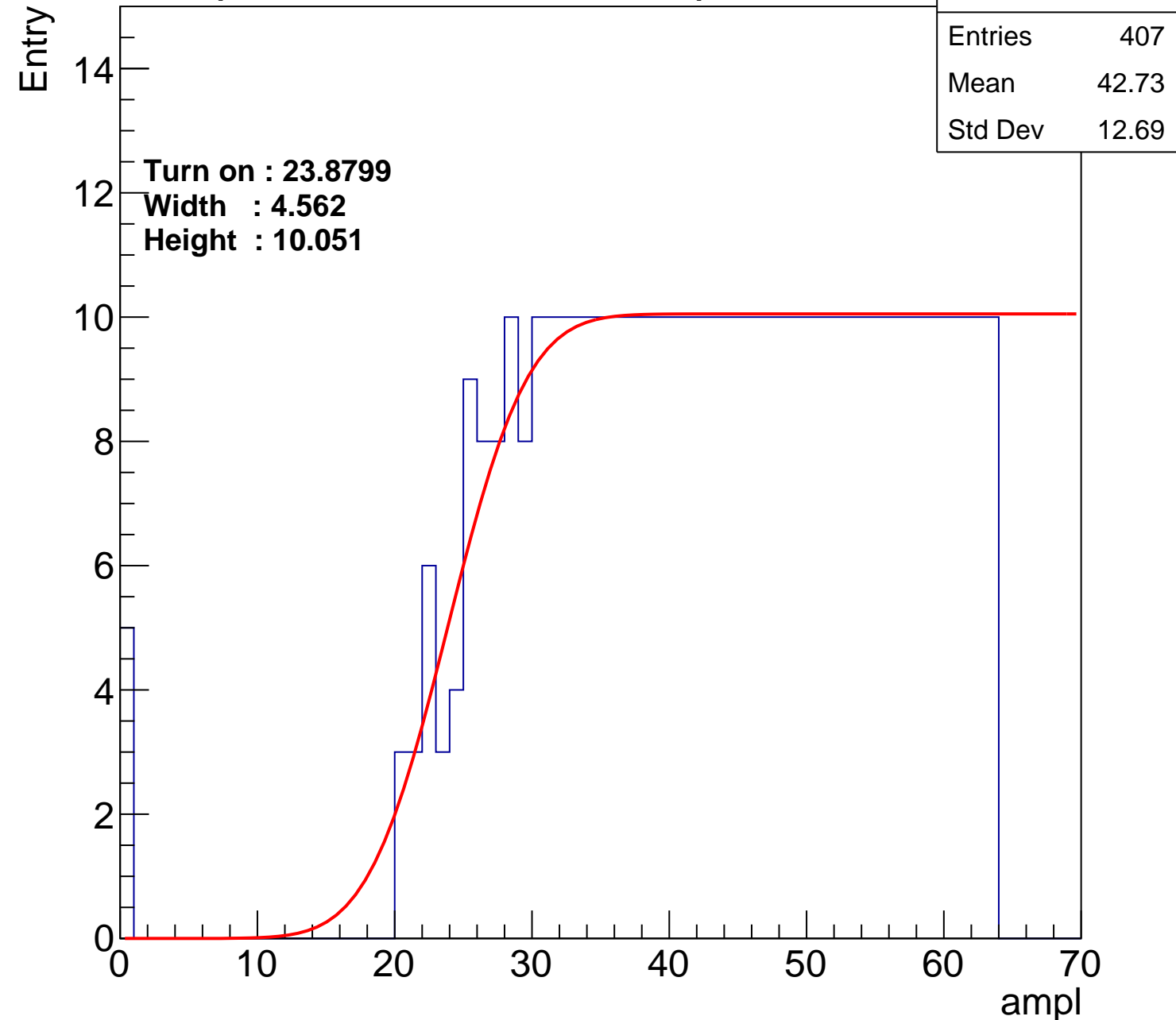
Width : 4.562

Height : 10.051

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch31

calib_packv5_042523_0143.root, FC#7, port C2

Entries	396
Mean	43.36
Std Dev	12.23

Turn on : 24.9820

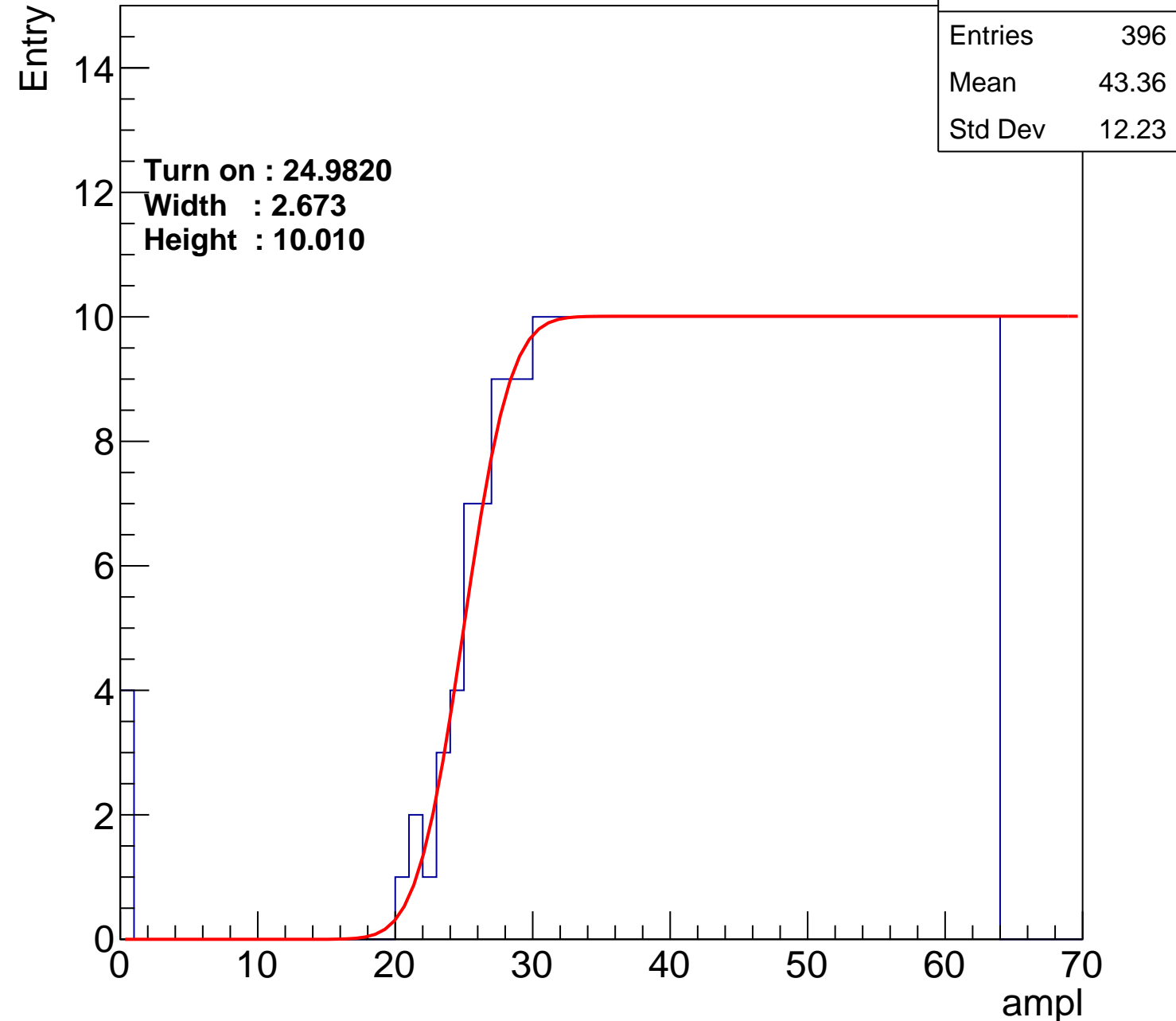
Width : 2.673

Height : 10.010

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch32

calib_packv5_042523_0143.root, FC#7, port C2

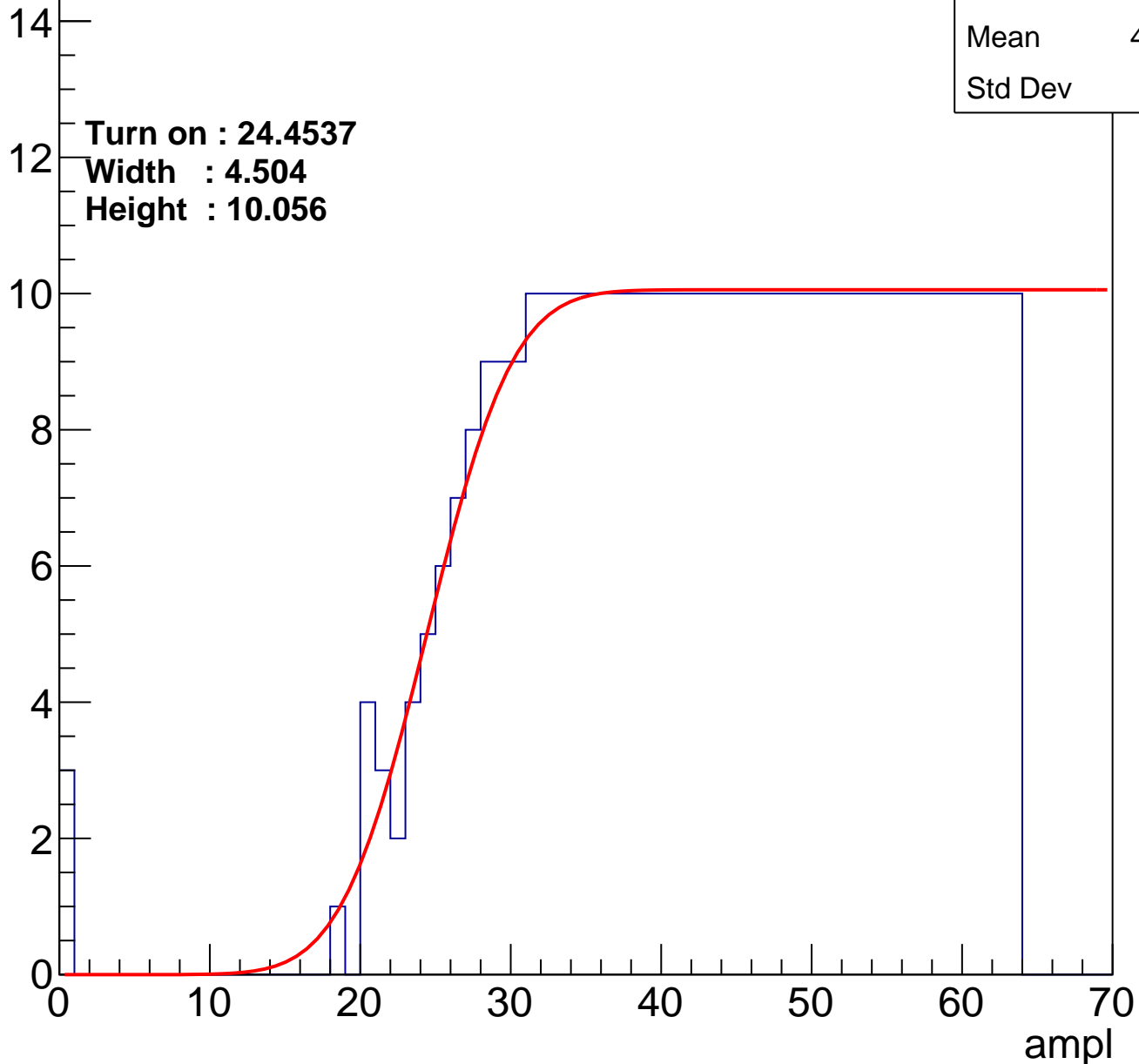
Entries	400
Mean	43.15
Std Dev	12.3

Turn on : 24.4537

Width : 4.504

Height : 10.056

Entry



B1L103S, U1-ch33

calib_packv5_042523_0143.root, FC#7, port C2

Entries	395
Mean	43.14
Std Dev	12.8

Turn on : 25.9627

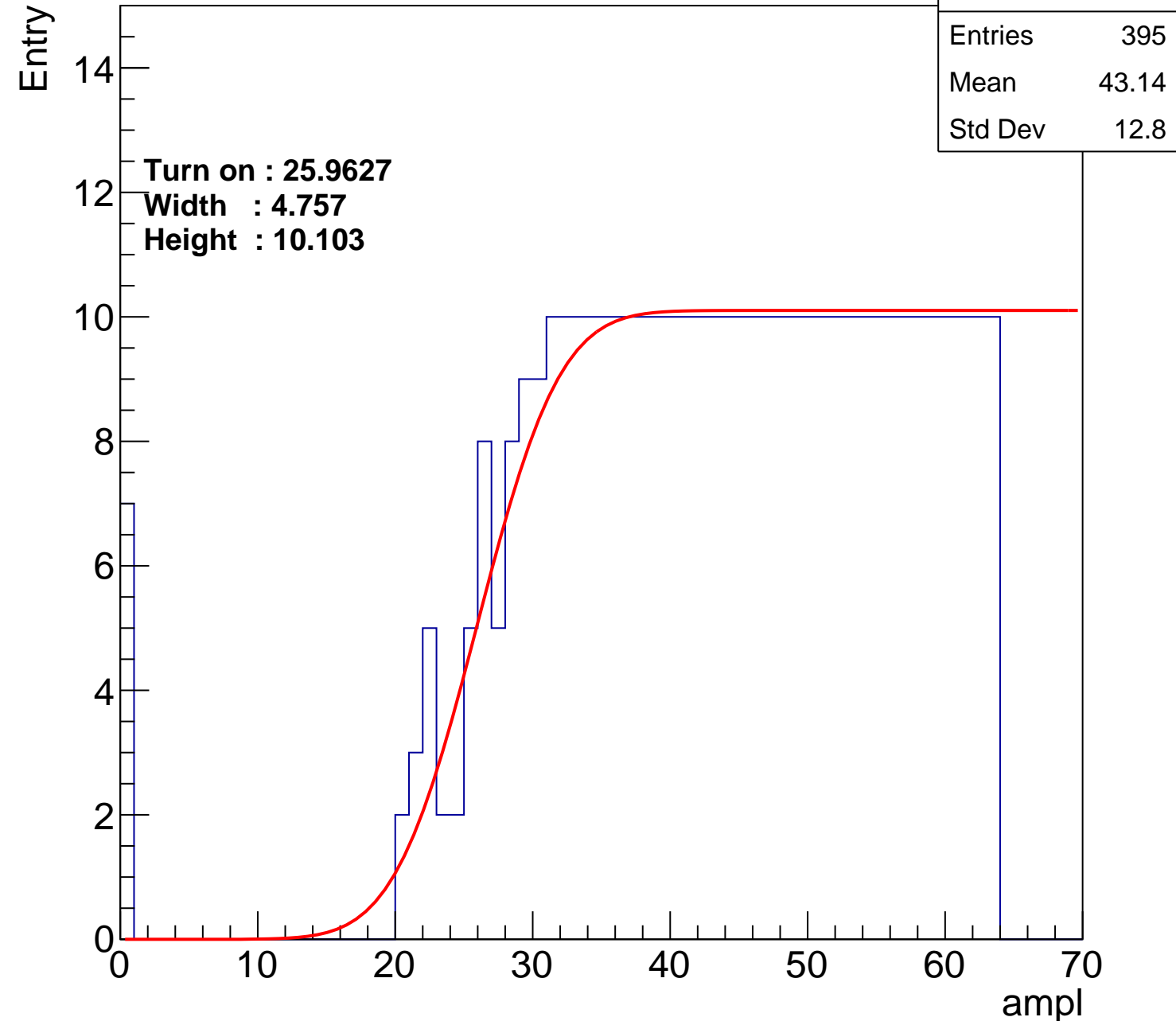
Width : 4.757

Height : 10.103

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch34

calib_packv5_042523_0143.root, FC#7, port C2

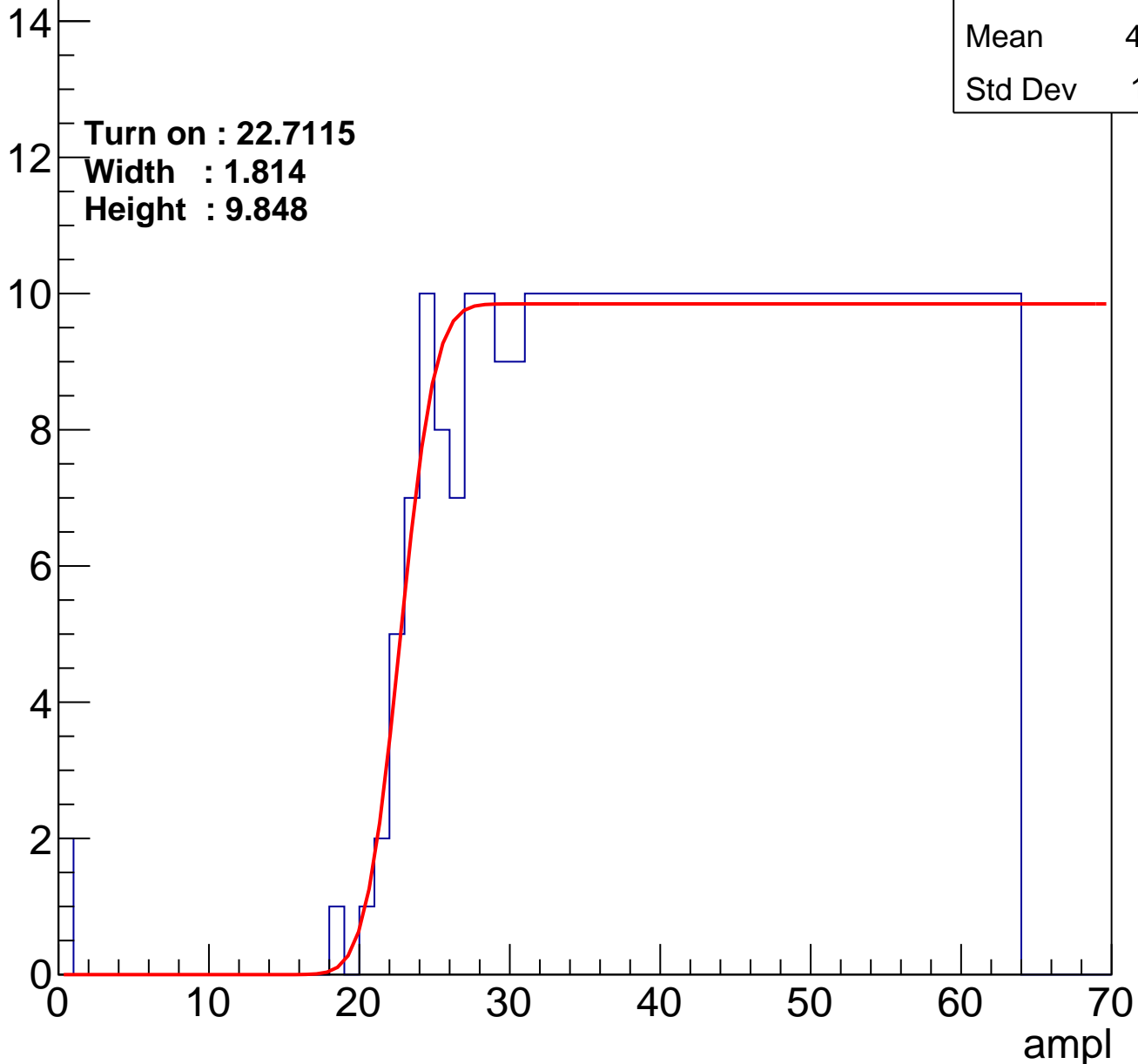
Entries	411
Mean	42.73
Std Dev	12.31

Turn on : 22.7115

Width : 1.814

Height : 9.848

Entry



B1L103S, U1-ch35

calib_packv5_042523_0143.root, FC#7, port C2

Entries	387
Mean	43.84
Std Dev	11.89

Turn on : 25.9444

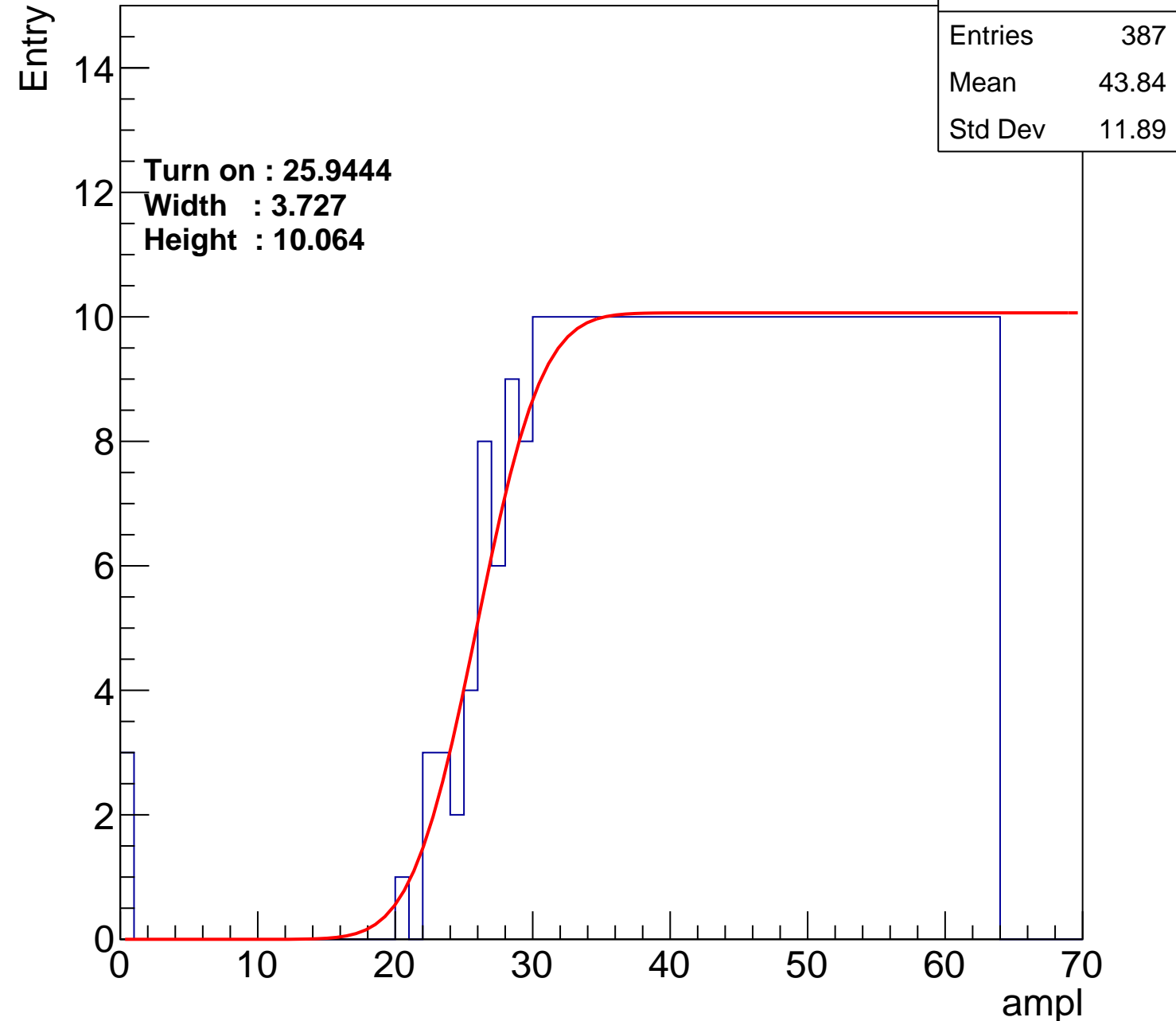
Width : 3.727

Height : 10.064

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch36

calib_packv5_042523_0143.root, FC#7, port C2

Entries	384
Mean	43.97
Std Dev	11.85

Turn on : 26.3492

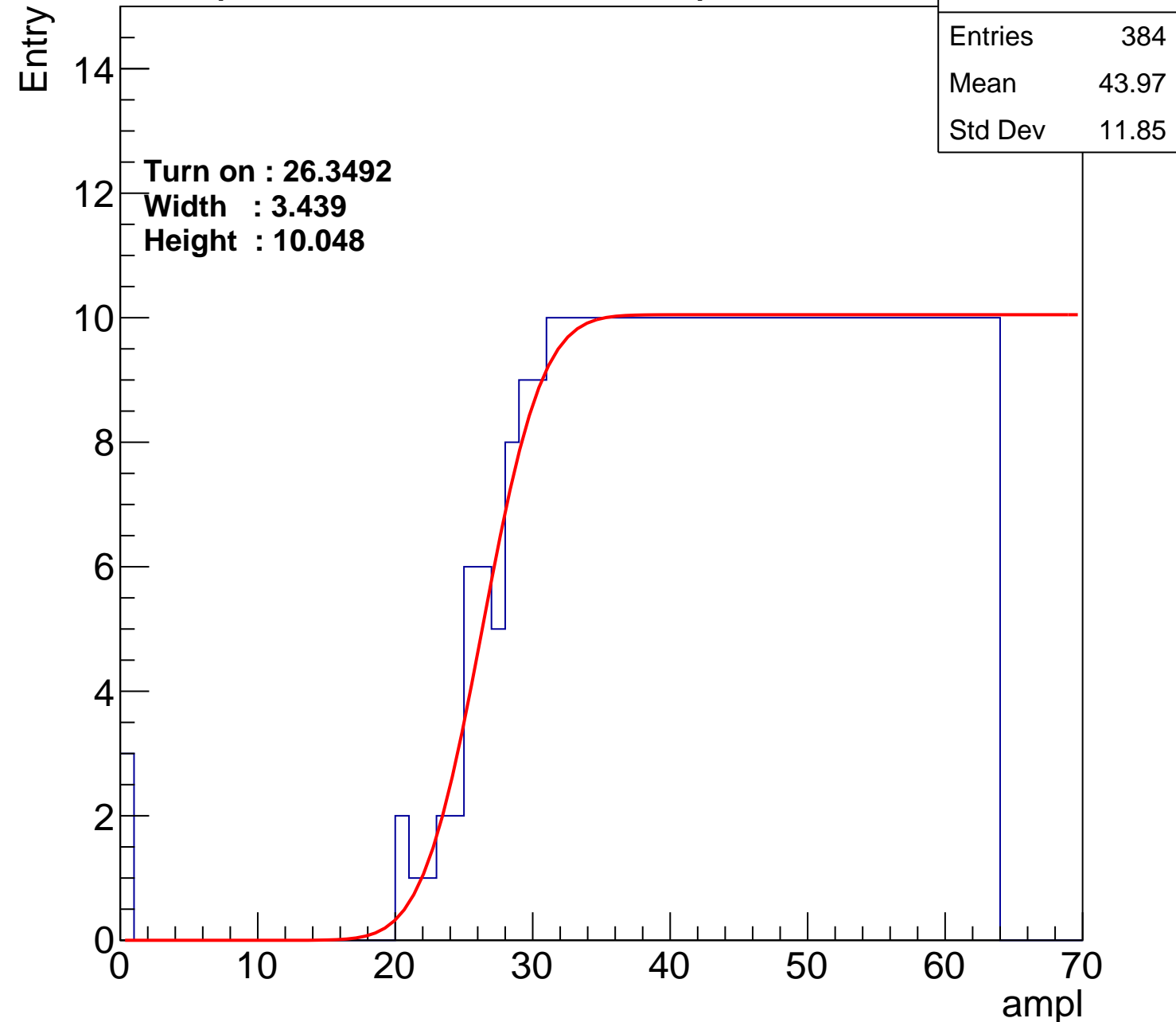
Width : 3.439

Height : 10.048

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch37

calib_packv5_042523_0143.root, FC#7, port C2

Entries	374
Mean	44.41
Std Dev	11.75

Turn on : 27.3459

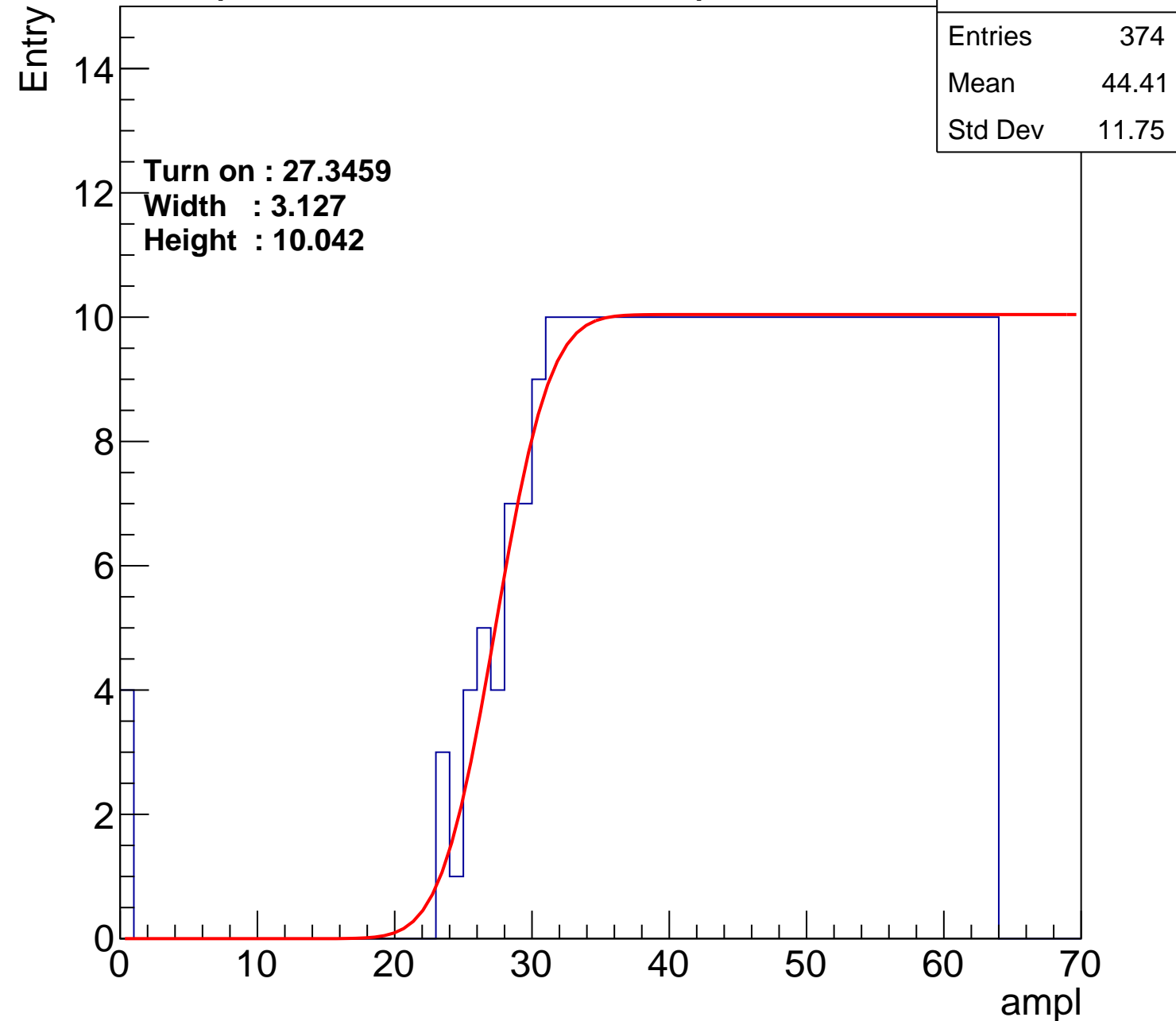
Width : 3.127

Height : 10.042

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch38

calib_packv5_042523_0143.root, FC#7, port C2

Entries	375
Mean	44.5
Std Dev	11.41

Turn on : 27.0235

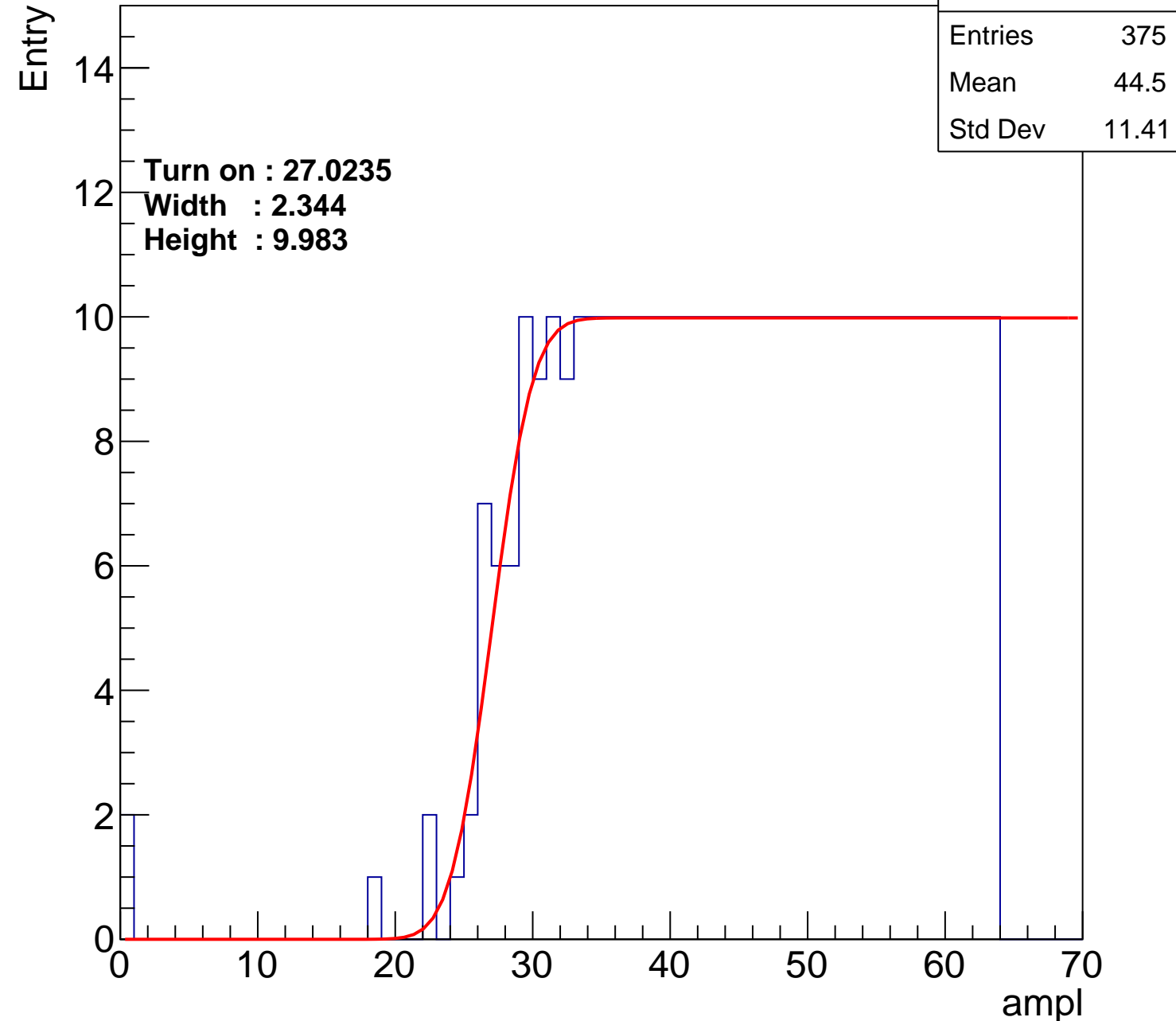
Width : 2.344

Height : 9.983

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch39

calib_packv5_042523_0143.root, FC#7, port C2

Entries	397
Mean	43.22
Std Dev	12.45

Turn on : 24.8498

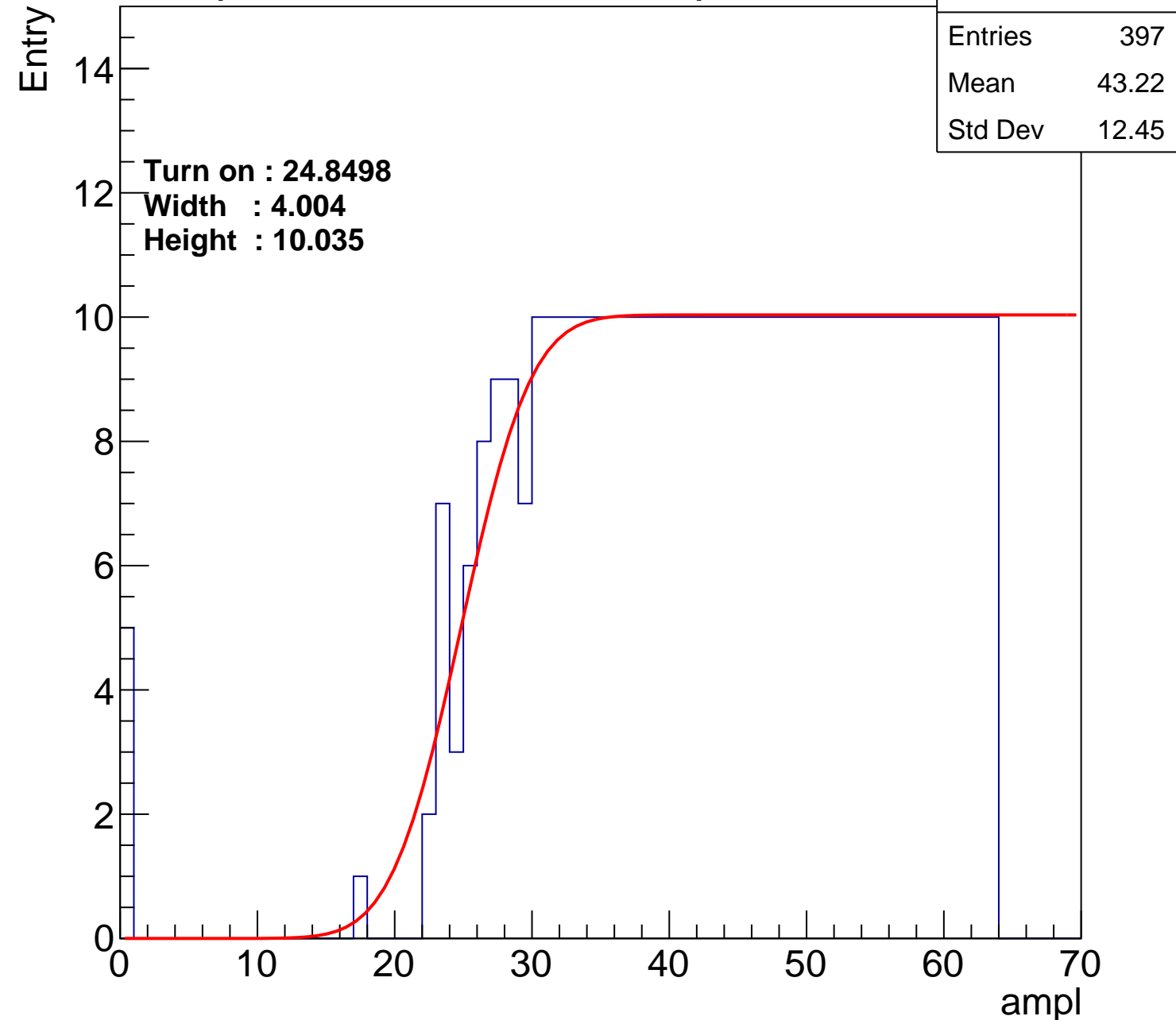
Width : 4.004

Height : 10.035

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch40

calib_packv5_042523_0143.root, FC#7, port C2

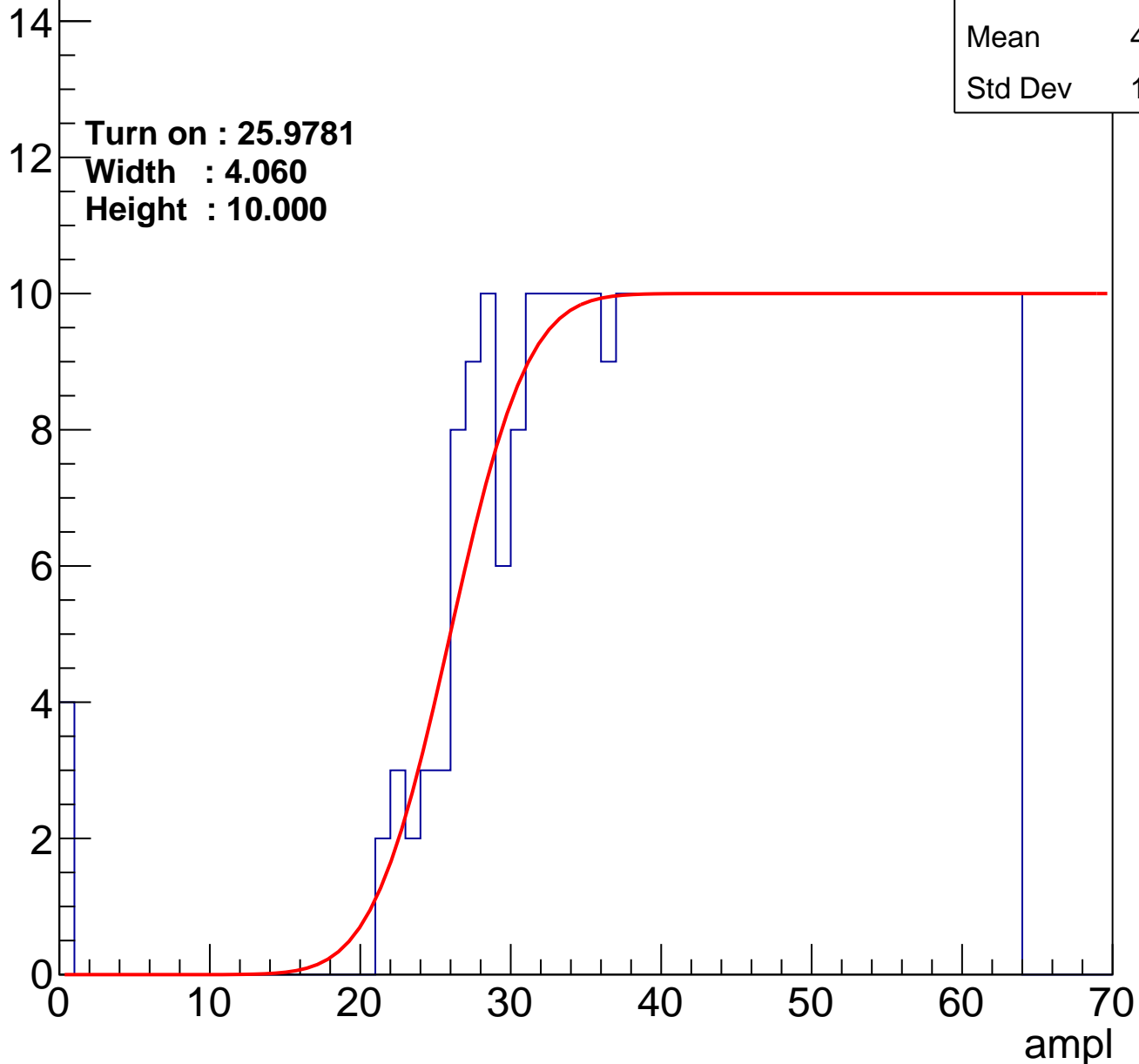
Entries	387
Mean	43.72
Std Dev	12.12

Turn on : 25.9781

Width : 4.060

Height : 10.000

Entry



B1L103S, U1-ch41

calib_packv5_042523_0143.root, FC#7, port C2

Entries	363
Mean	45.01
Std Dev	11.32

Turn on : 28.0943

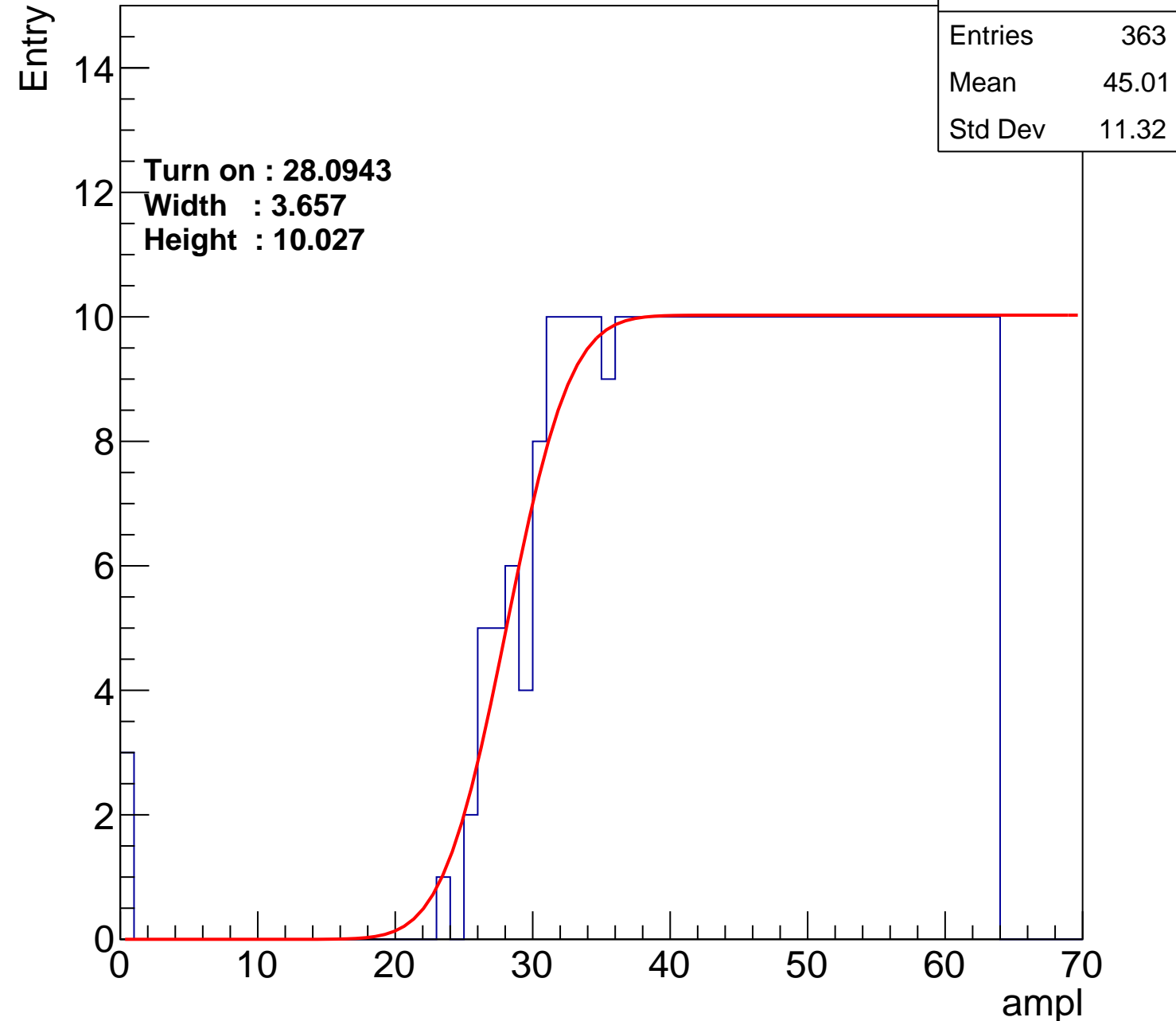
Width : 3.657

Height : 10.027

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch42

calib_packv5_042523_0143.root, FC#7, port C2

Entries	390
Mean	43.54
Std Dev	12.32

Turn on : 25.9350

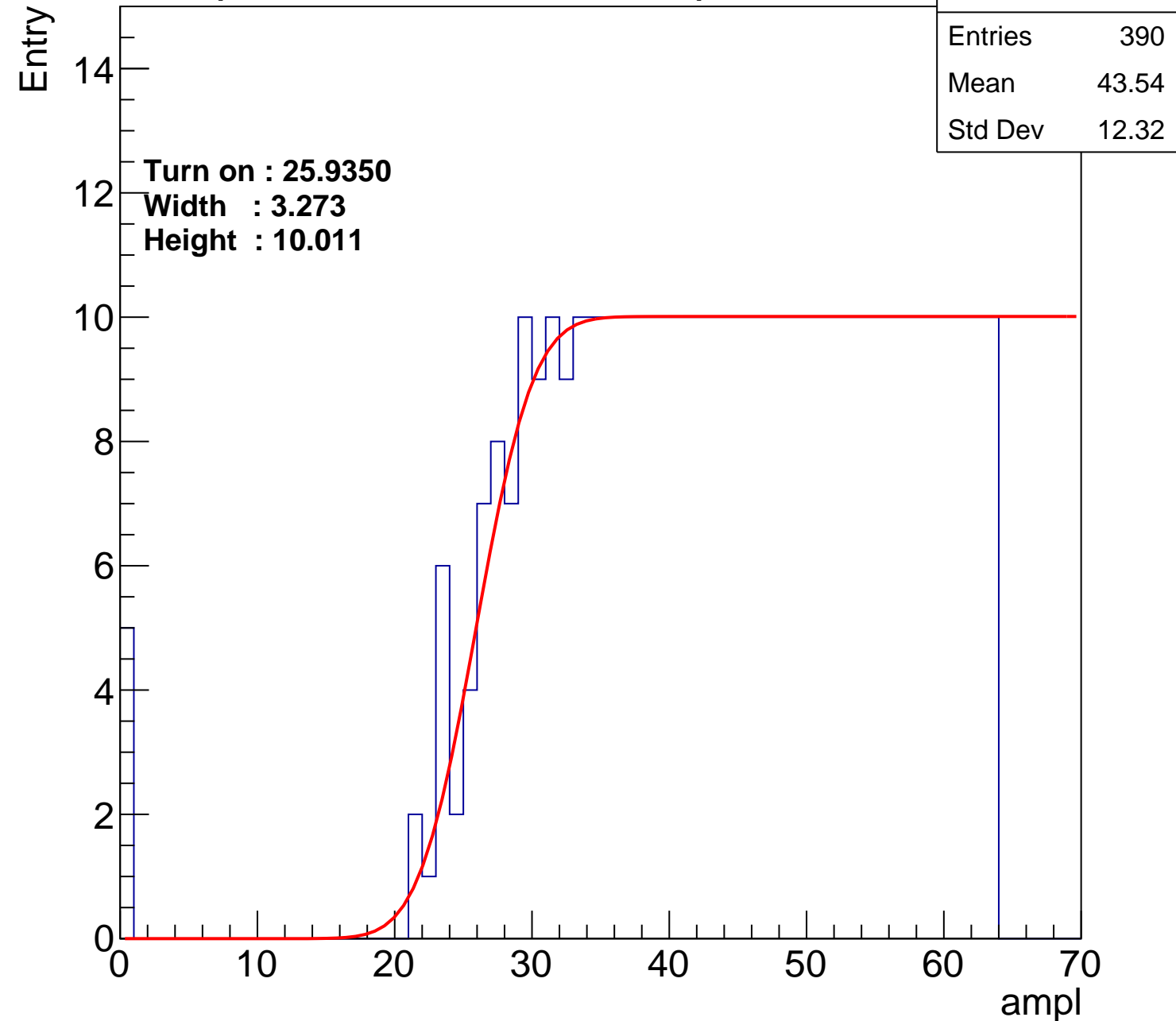
Width : 3.273

Height : 10.011

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch43

calib_packv5_042523_0143.root, FC#7, port C2

Entries	392
Mean	43.51
Std Dev	12.2

Turn on : 25.4780

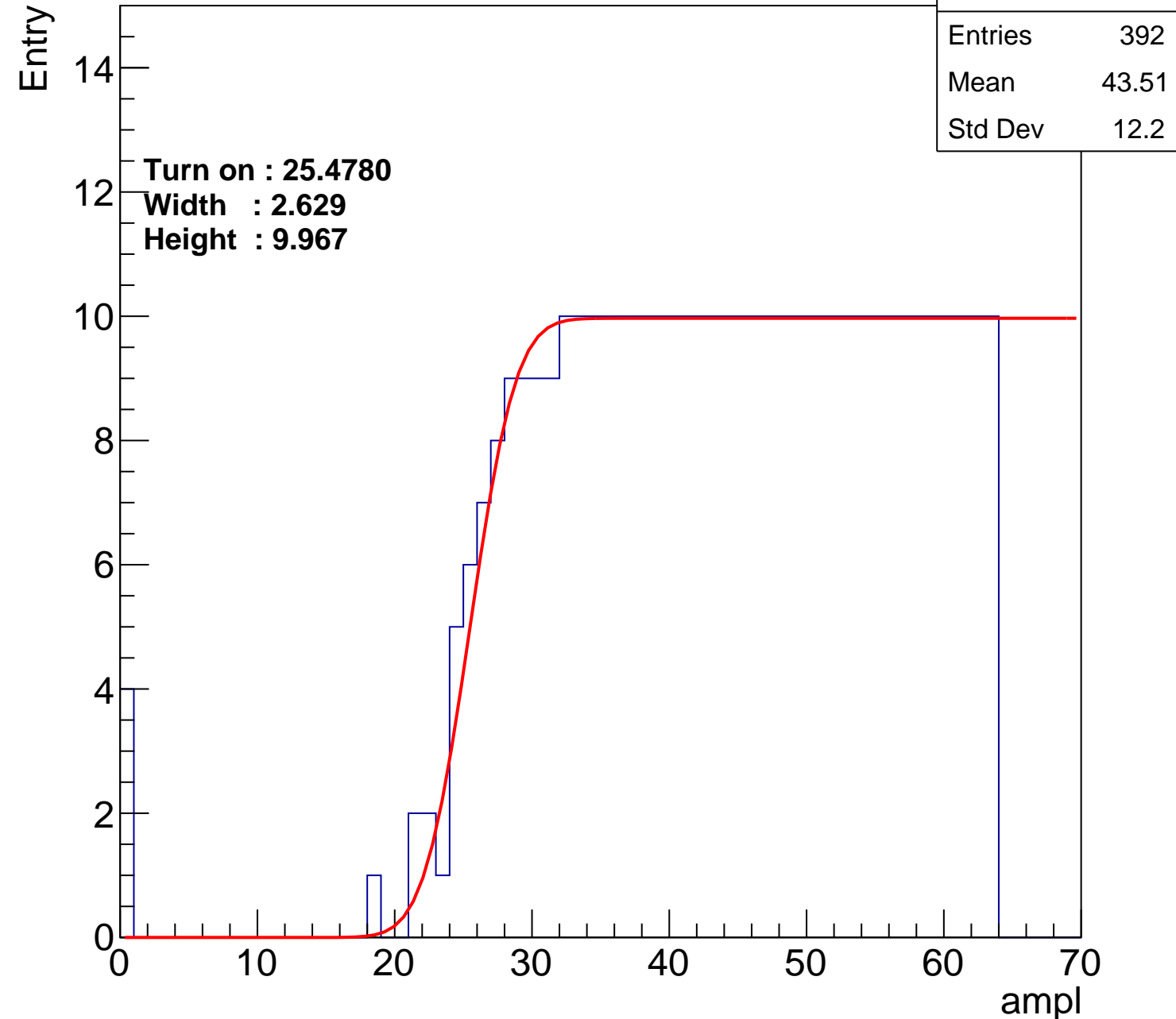
Width : 2.629

Height : 9.967

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch44

calib_packv5_042523_0143.root, FC#7, port C2

Entries	404
Mean	42.72
Std Dev	12.96

Turn on : 24.2239

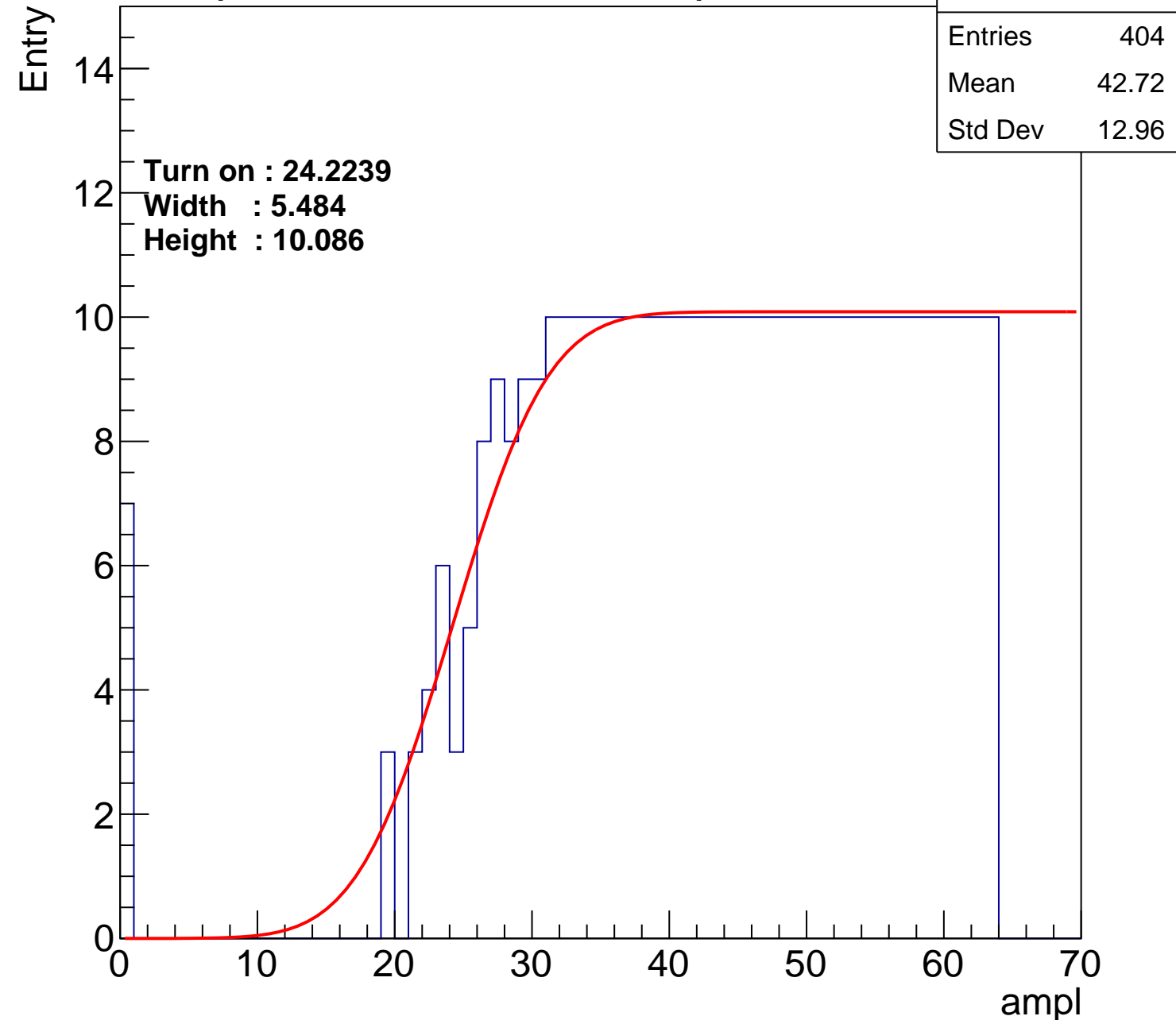
Width : 5.484

Height : 10.086

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch45

calib_packv5_042523_0143.root, FC#7, port C2

Entries	395
Mean	43.48
Std Dev	12.04

Turn on : 24.6988

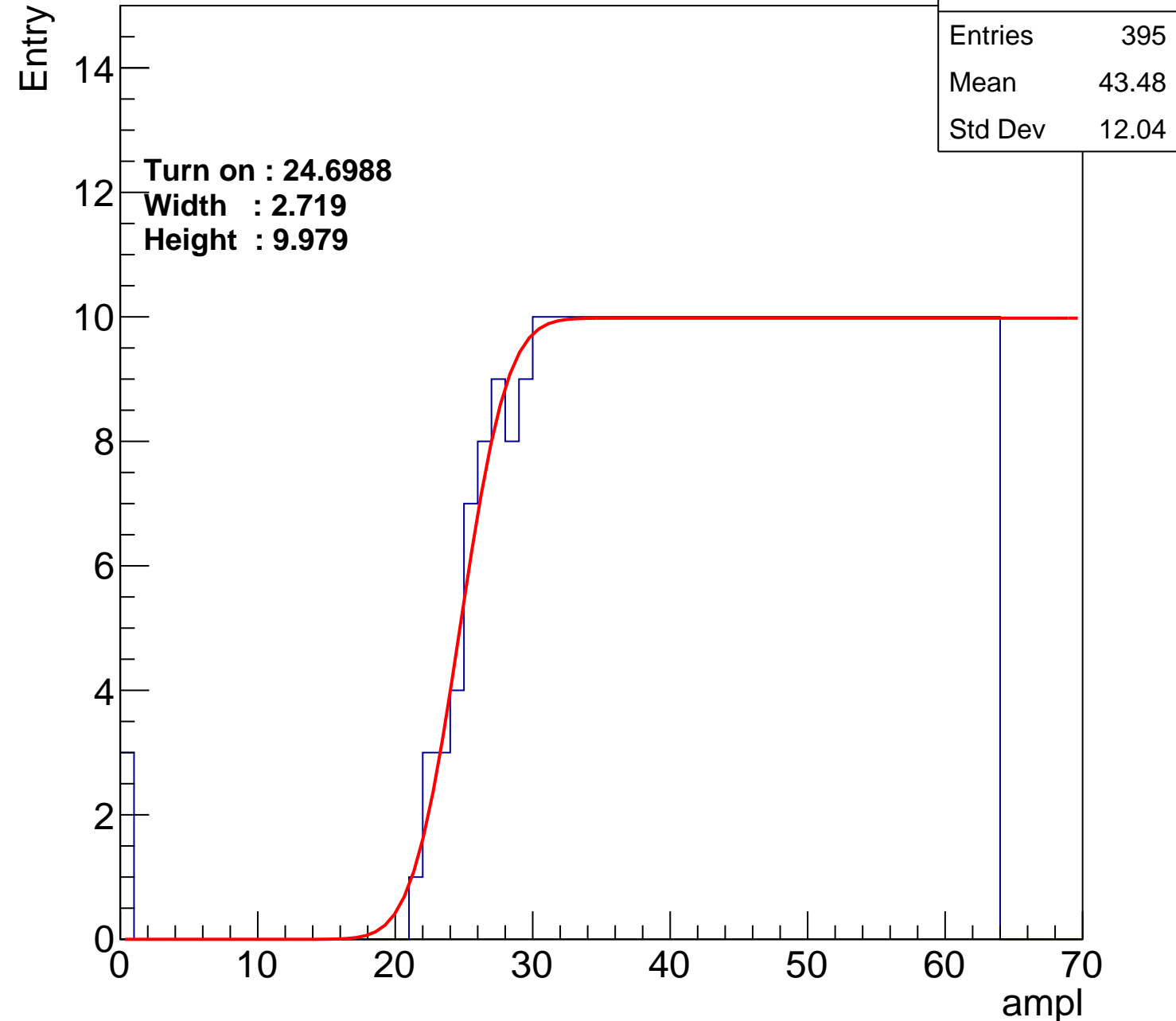
Width : 2.719

Height : 9.979

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch46

calib_packv5_042523_0143.root, FC#7, port C2

Entries	390
Mean	43.56
Std Dev	12.24

Turn on : 25.7300

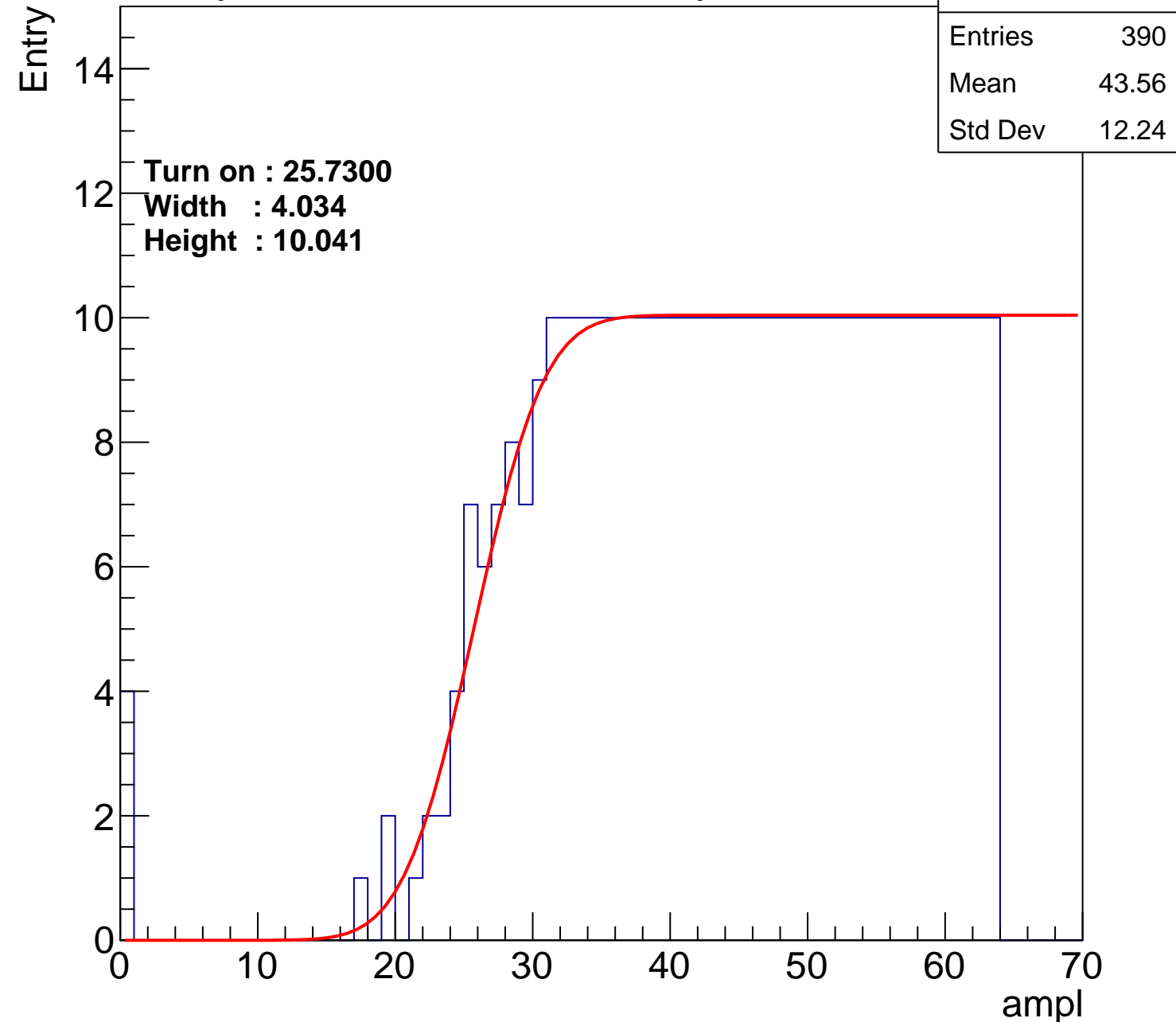
Width : 4.034

Height : 10.041

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch47

calib_packv5_042523_0143.root, FC#7, port C2

Entries	395
Mean	43.34
Std Dev	12.37

Turn on : 24.9328

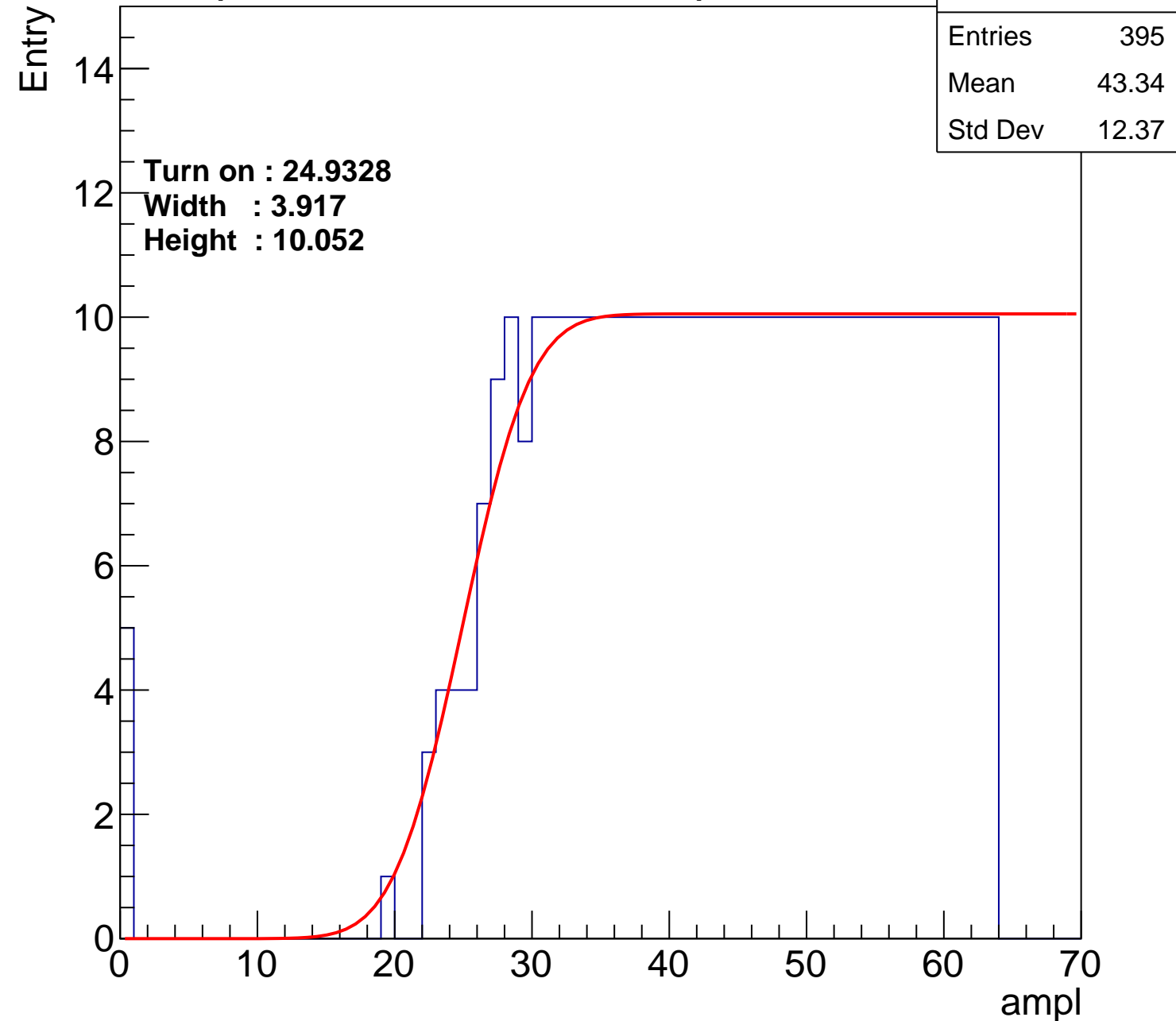
Width : 3.917

Height : 10.052

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch48

calib_packv5_042523_0143.root, FC#7, port C2

Entries	385
Mean	43.99
Std Dev	11.68

Turn on : 25.6014

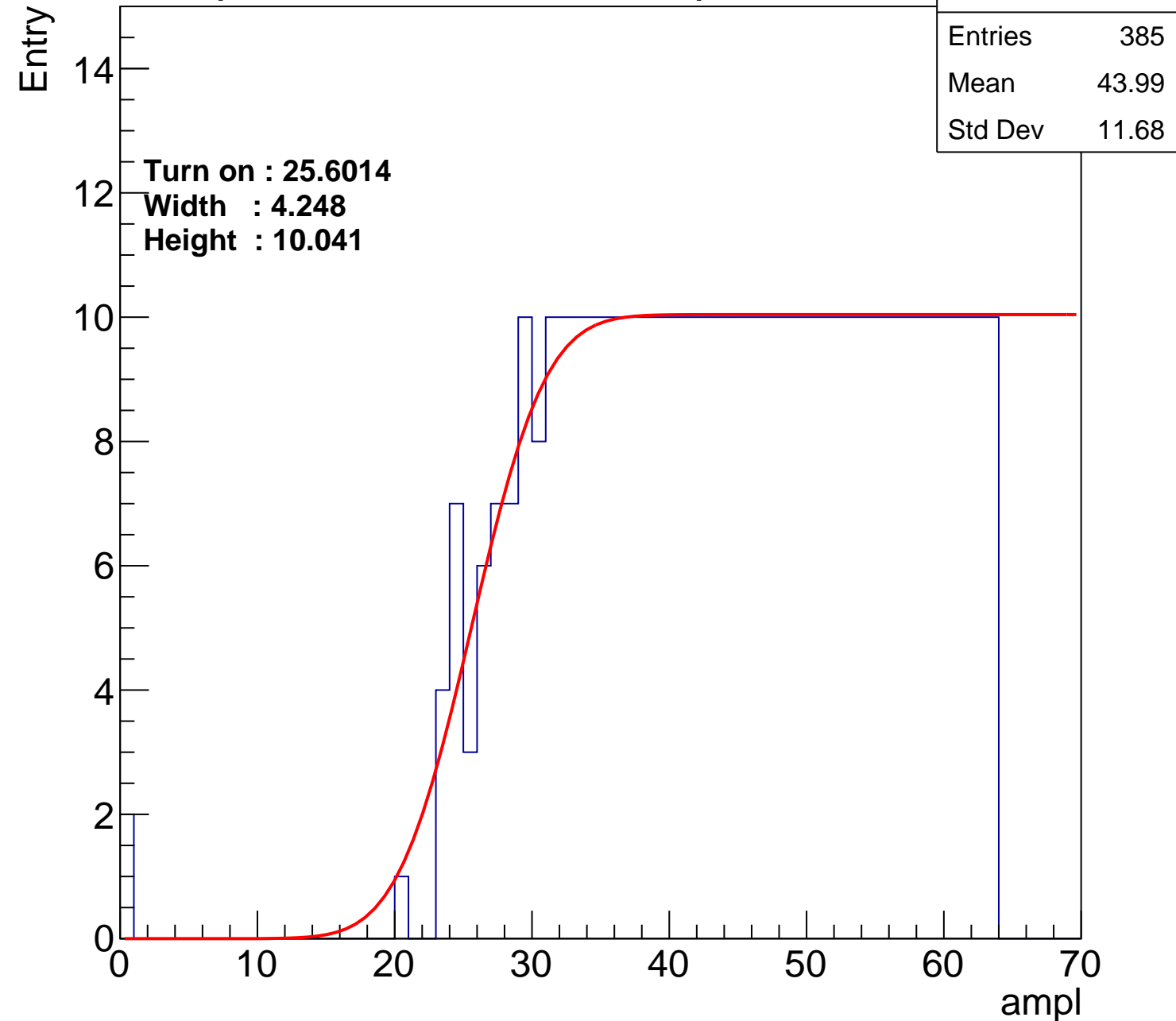
Width : 4.248

Height : 10.041

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch49

calib_packv5_042523_0143.root, FC#7, port C2

Entries	385
Mean	43.93
Std Dev	11.92

Turn on : 26.1903

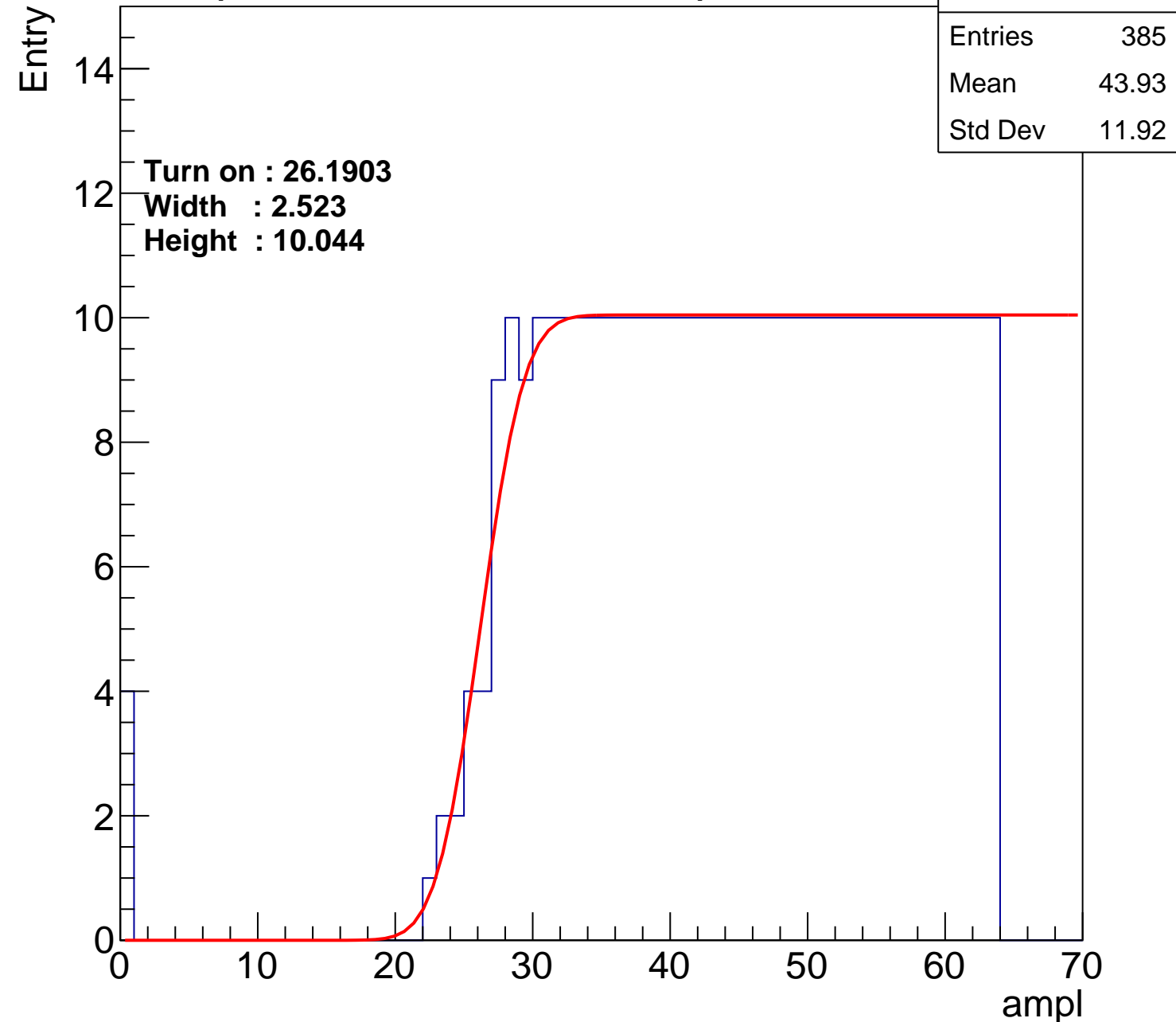
Width : 2.523

Height : 10.044

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch50

calib_packv5_042523_0143.root, FC#7, port C2

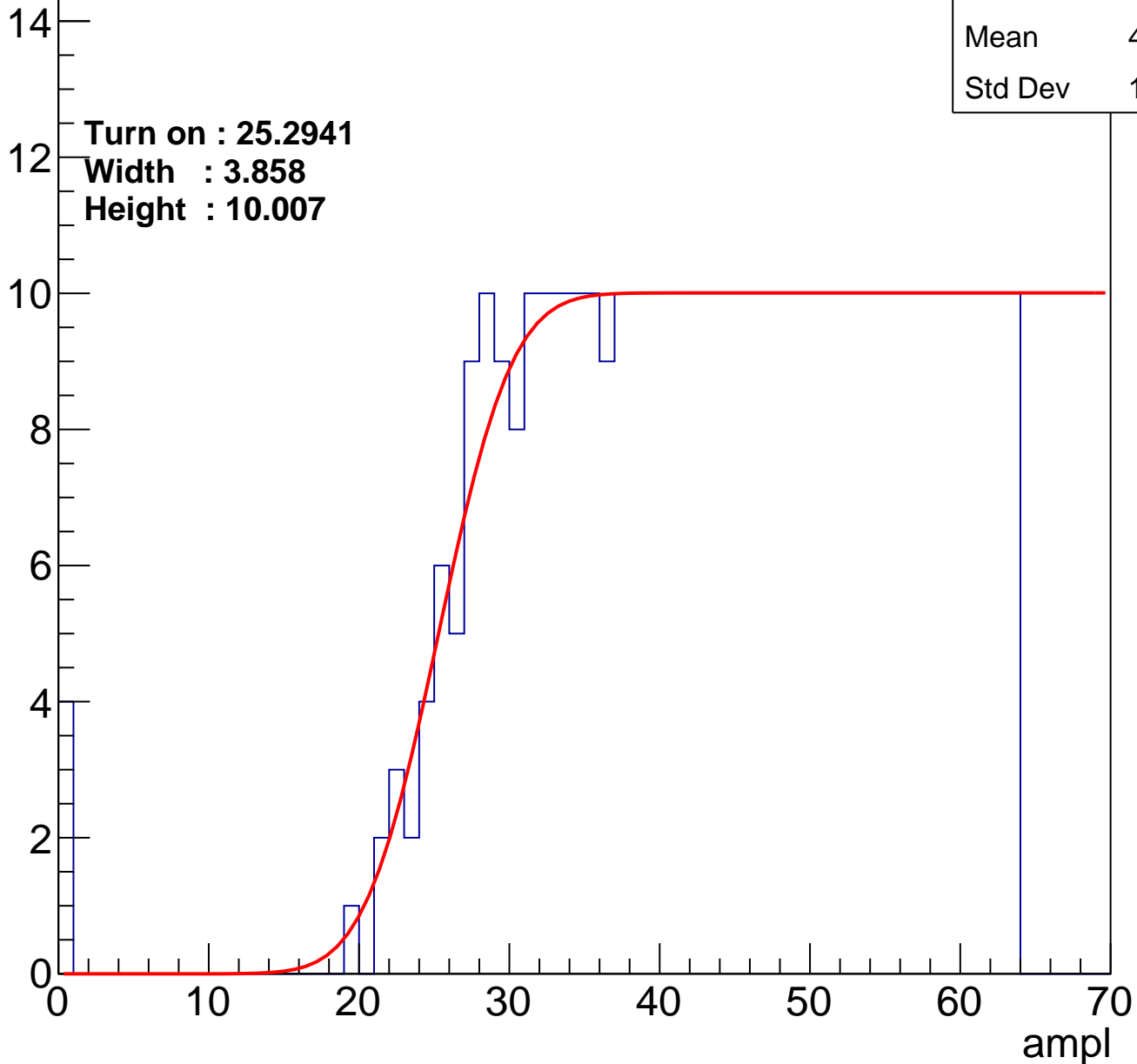
Entries	392
Mean	43.49
Std Dev	12.23

Turn on : 25.2941

Width : 3.858

Height : 10.007

Entry



B1L103S, U1-ch51

calib_packv5_042523_0143.root, FC#7, port C2

Entries	403
Mean	43.08
Std Dev	12.25

Turn on : 24.3693

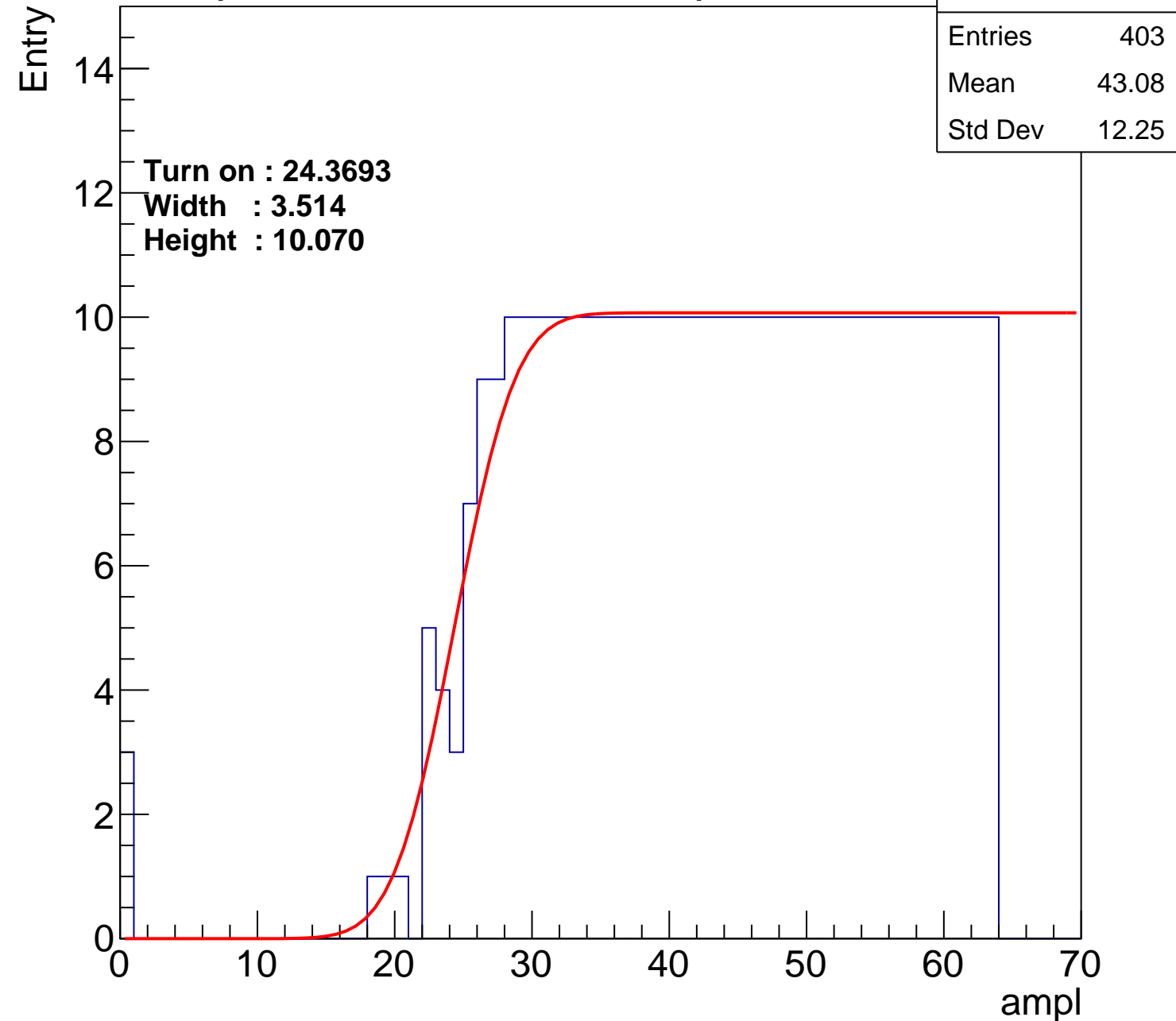
Width : 3.514

Height : 10.070

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch52

calib_packv5_042523_0143.root, FC#7, port C2

Entries	385
Mean	43.97
Std Dev	11.73

Turn on : 26.0370

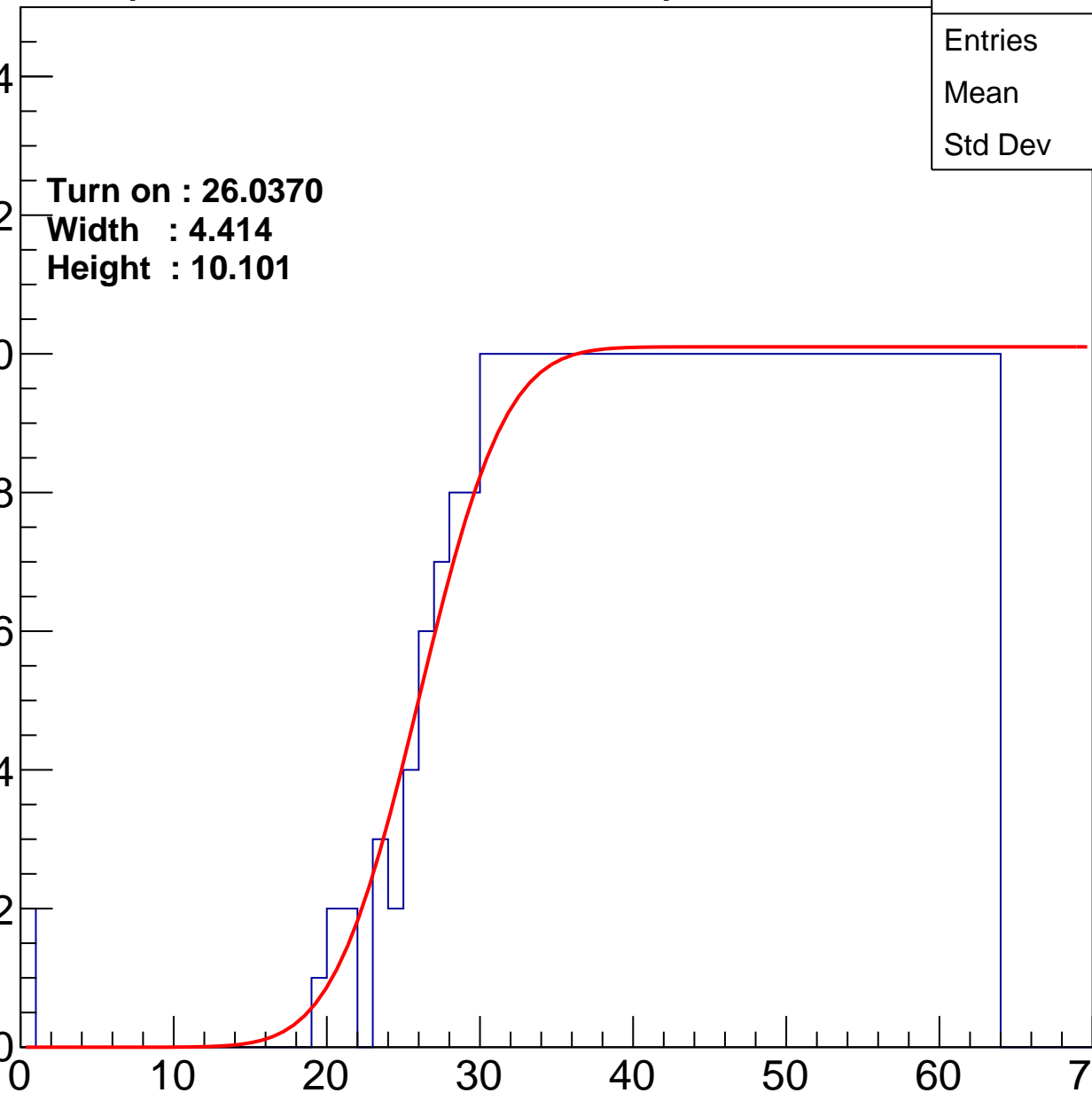
Width : 4.414

Height : 10.101

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch53

calib_packv5_042523_0143.root, FC#7, port C2

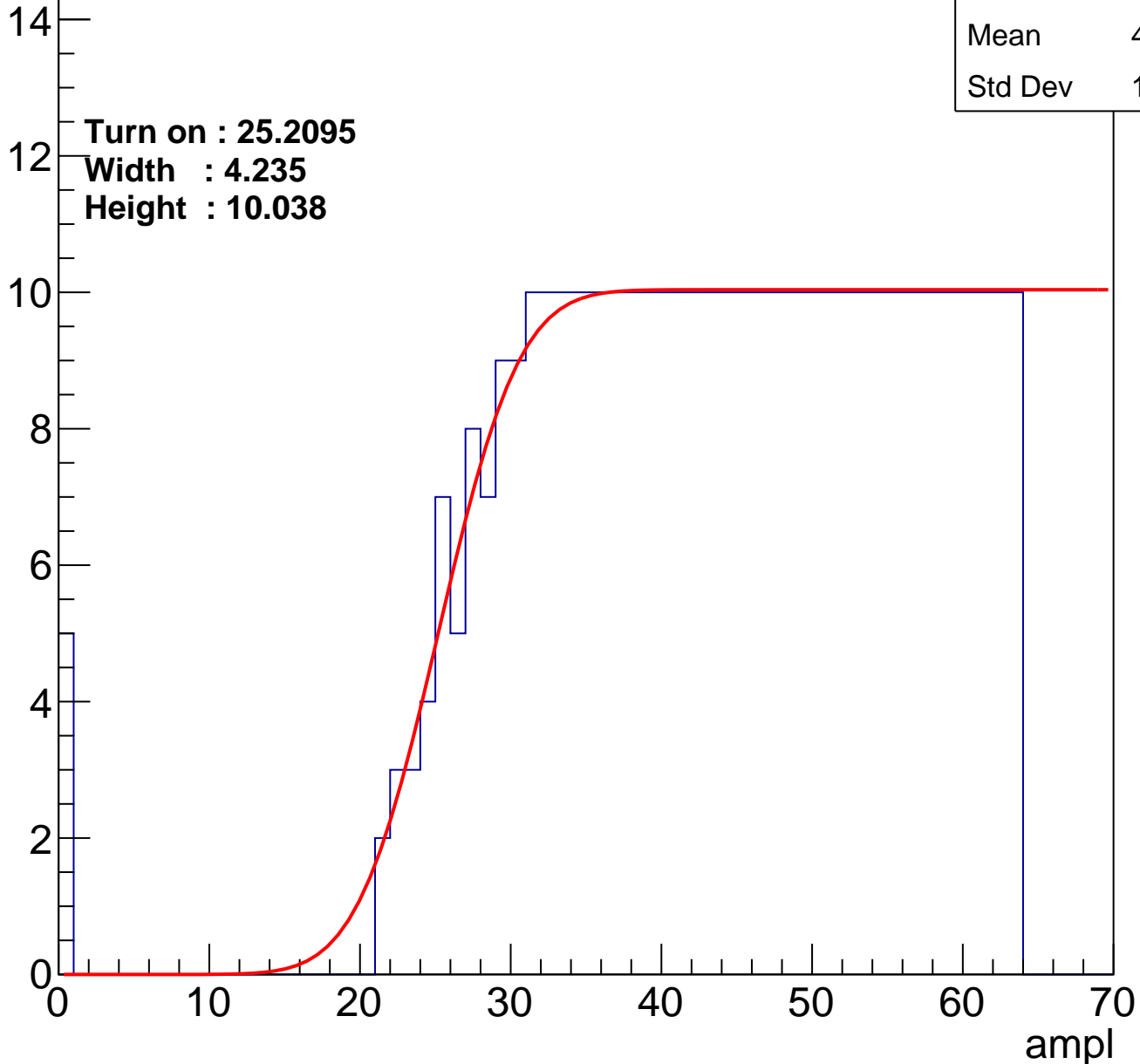
Entries	392
Mean	43.45
Std Dev	12.36

Turn on : 25.2095

Width : 4.235

Height : 10.038

Entry



B1L103S, U1-ch54

calib_packv5_042523_0143.root, FC#7, port C2

Entries	391
Mean	43.56
Std Dev	12.25

Turn on : 25.2306

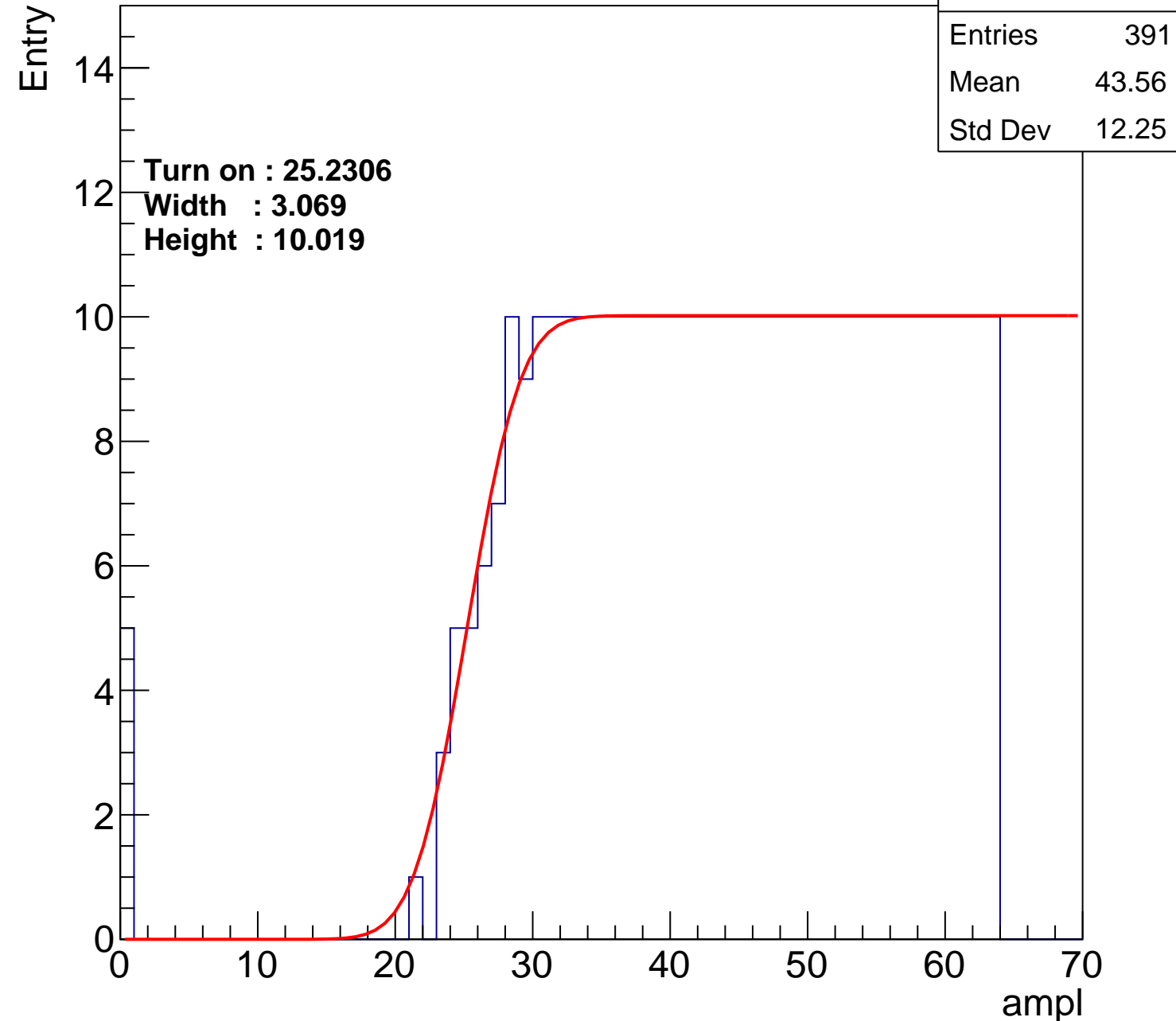
Width : 3.069

Height : 10.019

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch55

calib_packv5_042523_0143.root, FC#7, port C2

Entries	397
Mean	43.47
Std Dev	11.81

Turn on : 24.0528

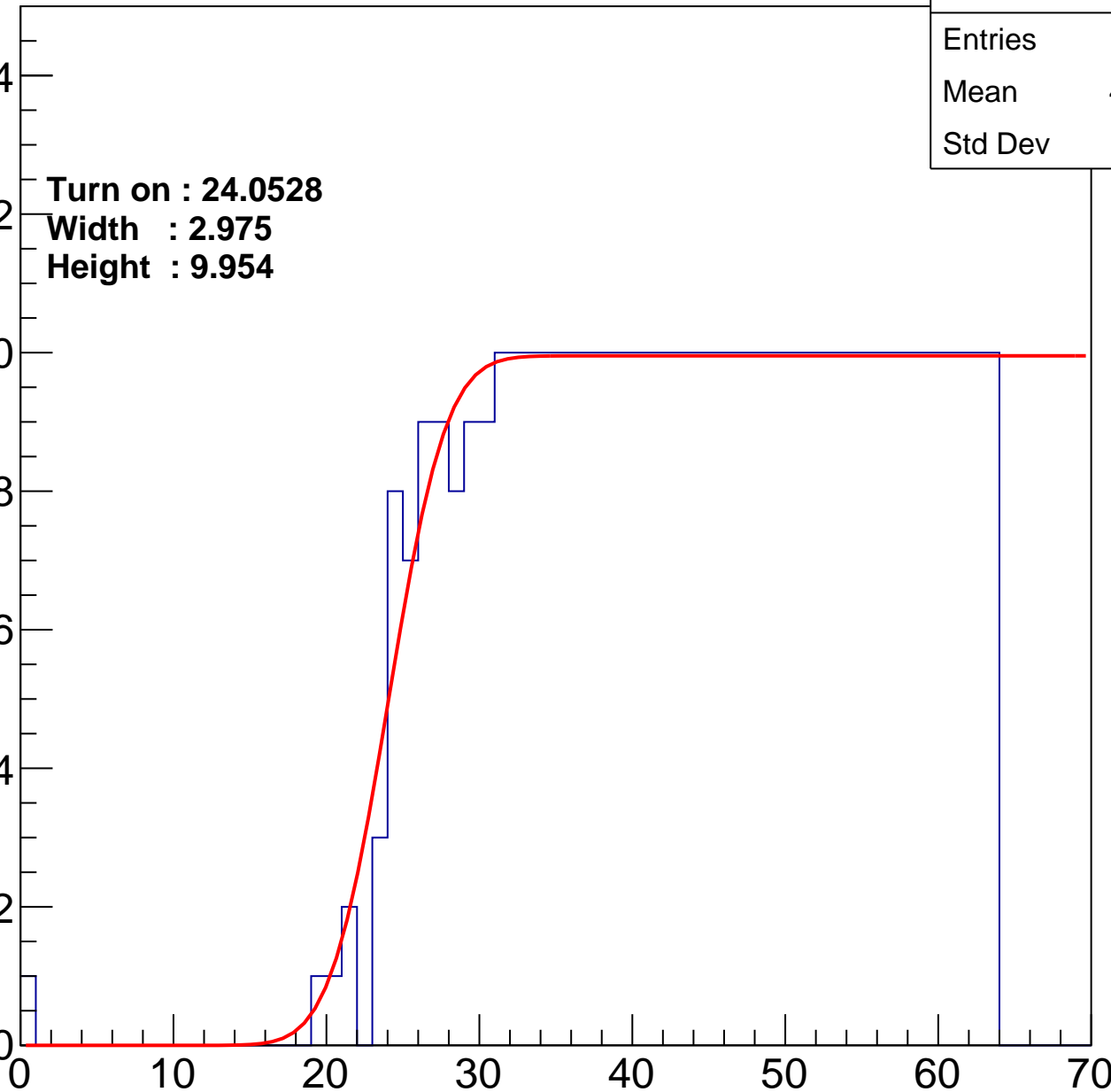
Width : 2.975

Height : 9.954

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch56

calib_packv5_042523_0143.root, FC#7, port C2

Entries	395
Mean	43.48
Std Dev	11.98

Turn on : 25.2309

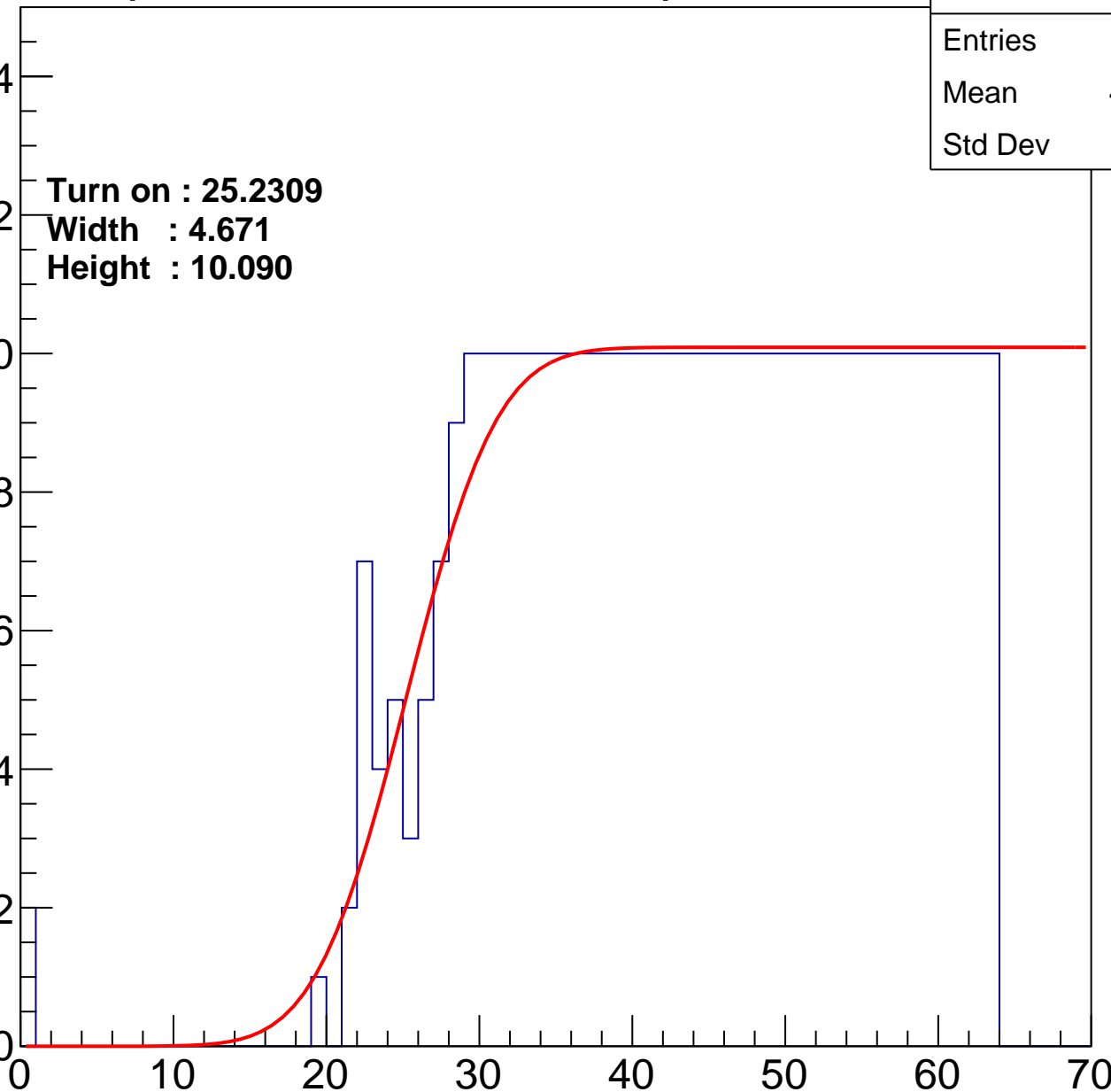
Width : 4.671

Height : 10.090

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch57

calib_packv5_042523_0143.root, FC#7, port C2

Entries	382
Mean	44.01
Std Dev	11.96

Turn on : 26.6851

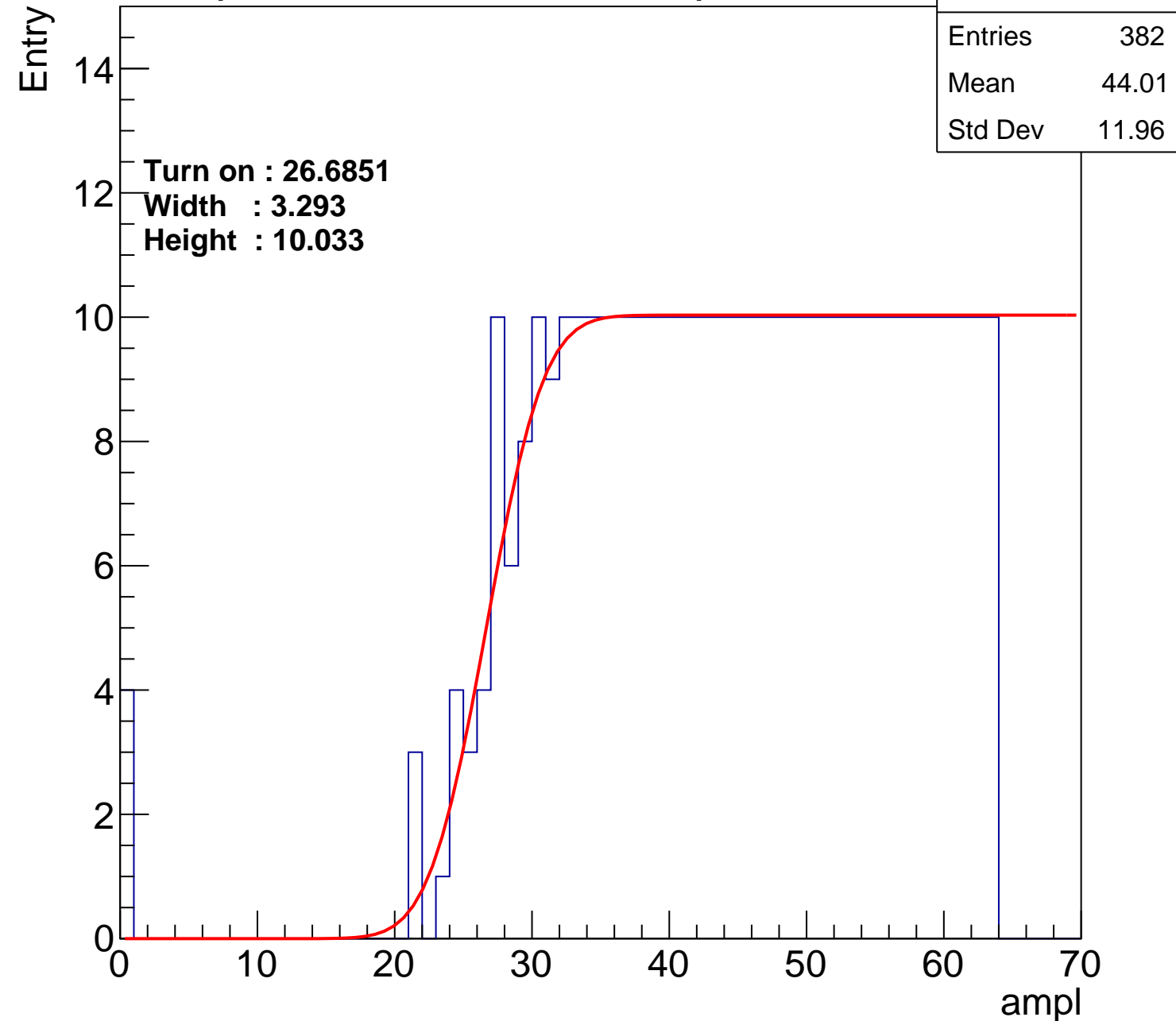
Width : 3.293

Height : 10.033

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch58

calib_packv5_042523_0143.root, FC#7, port C2

Entries	400
Mean	43.35
Std Dev	11.85

Turn on : 24.3385

Width : 3.085

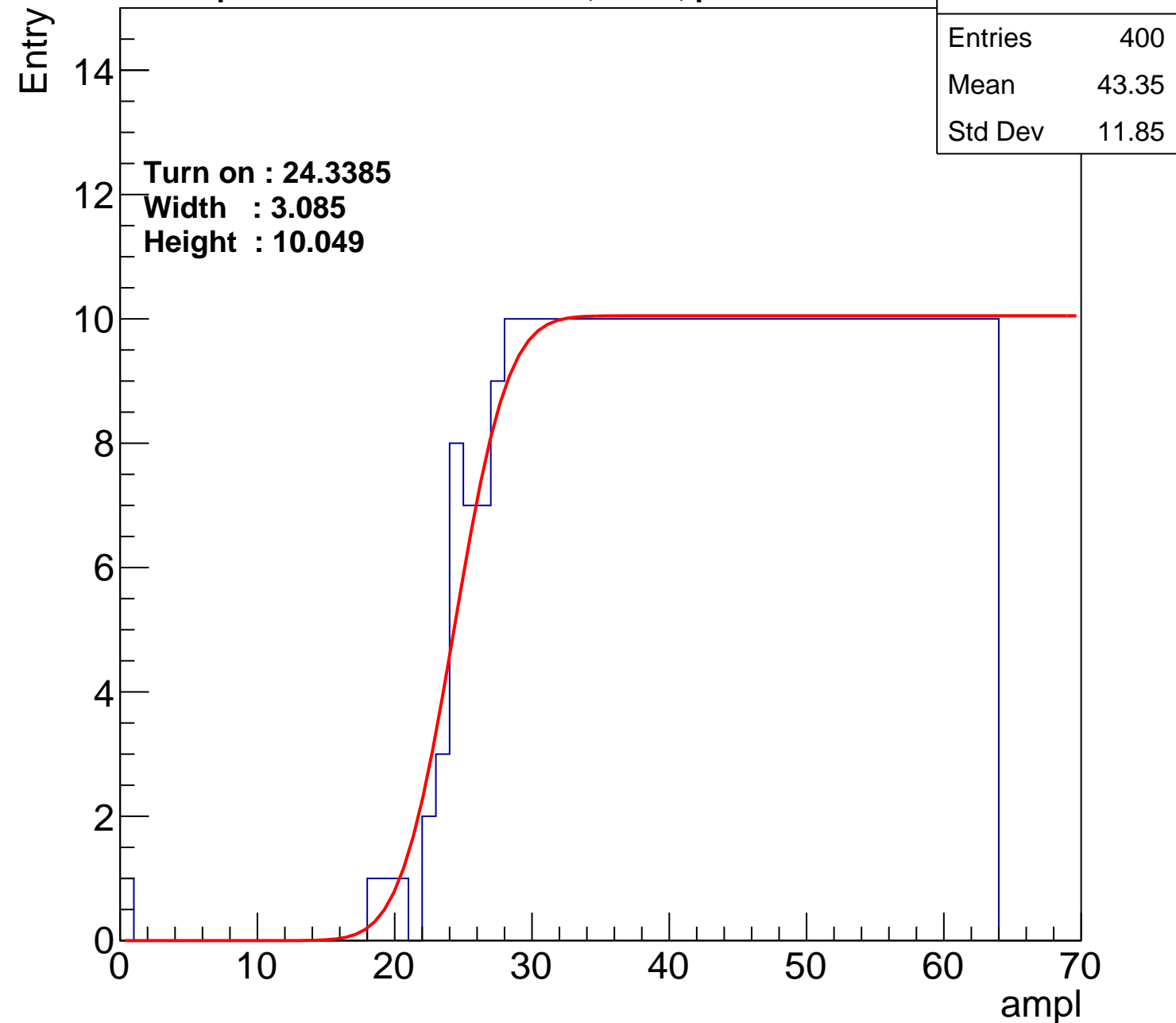
Height : 10.049

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L103S, U1-ch59

calib_packv5_042523_0143.root, FC#7, port C2

Entries	390
Mean	43.67
Std Dev	12

Turn on : 25.1156

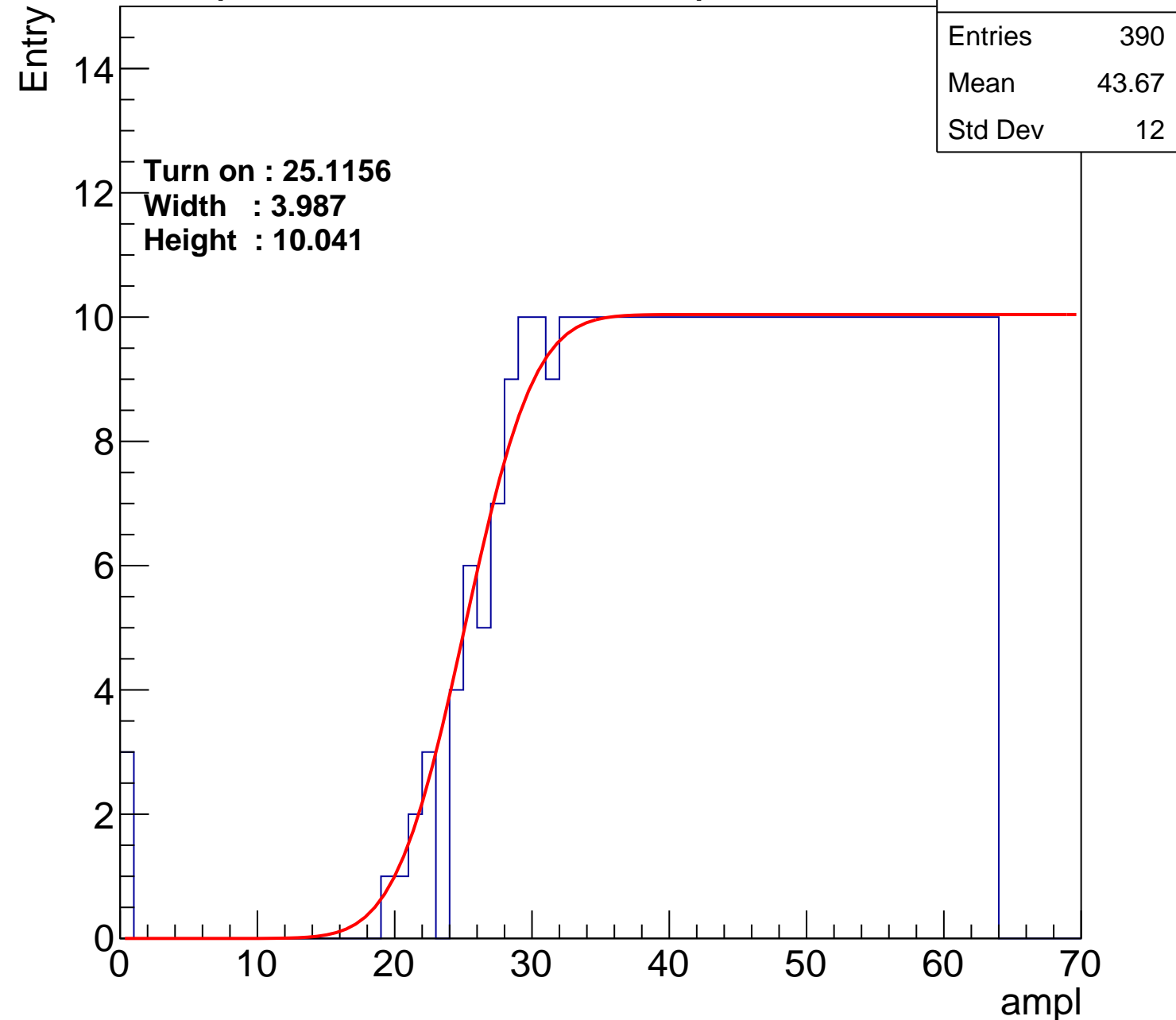
Width : 3.987

Height : 10.041

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch60

calib_packv5_042523_0143.root, FC#7, port C2

Entries	380
Mean	44.19
Std Dev	11.64

Turn on : 26.4396

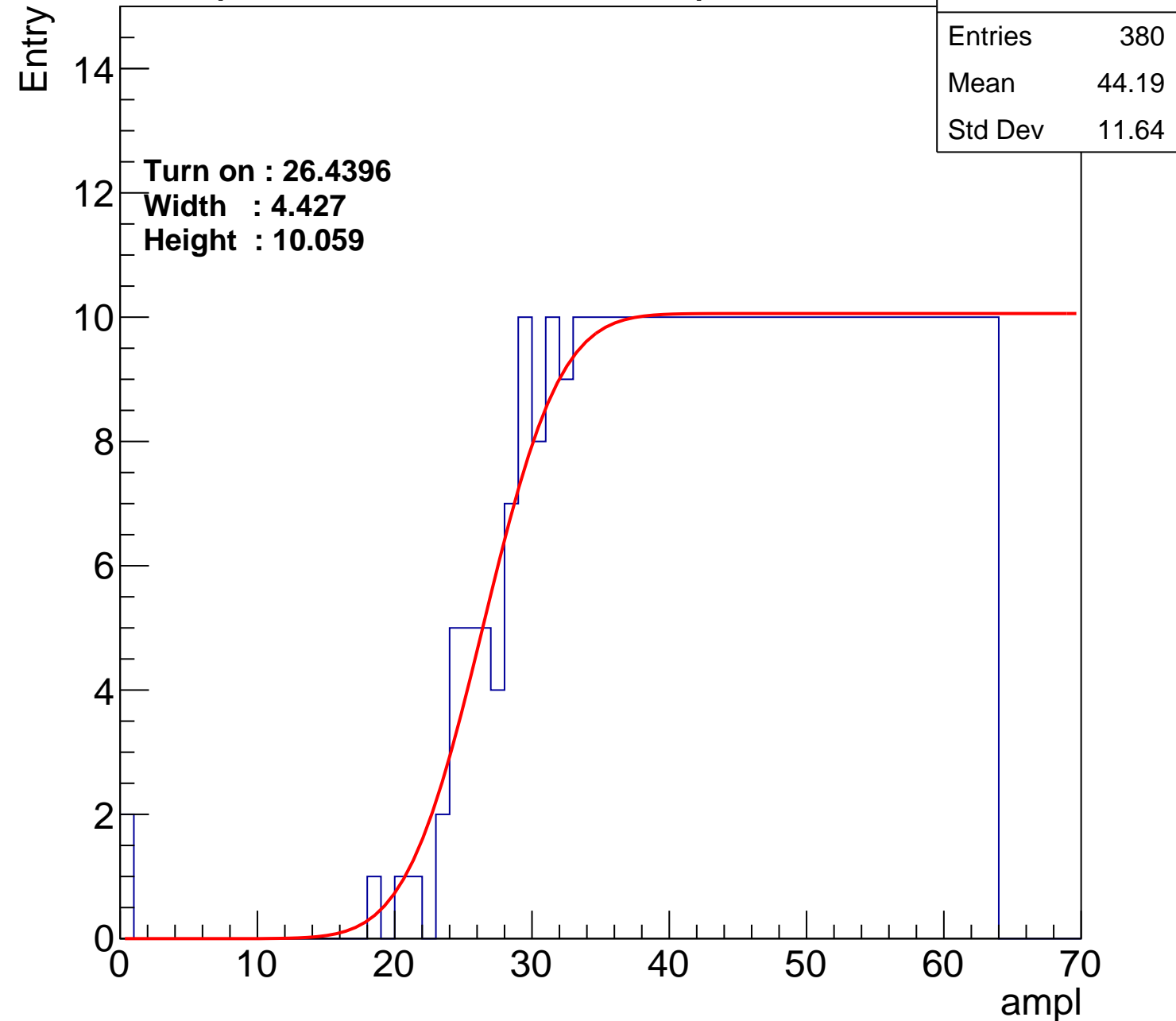
Width : 4.427

Height : 10.059

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch61

calib_packv5_042523_0143.root, FC#7, port C2

Entries	382
Mean	44.02
Std Dev	11.96

Turn on : 26.1696

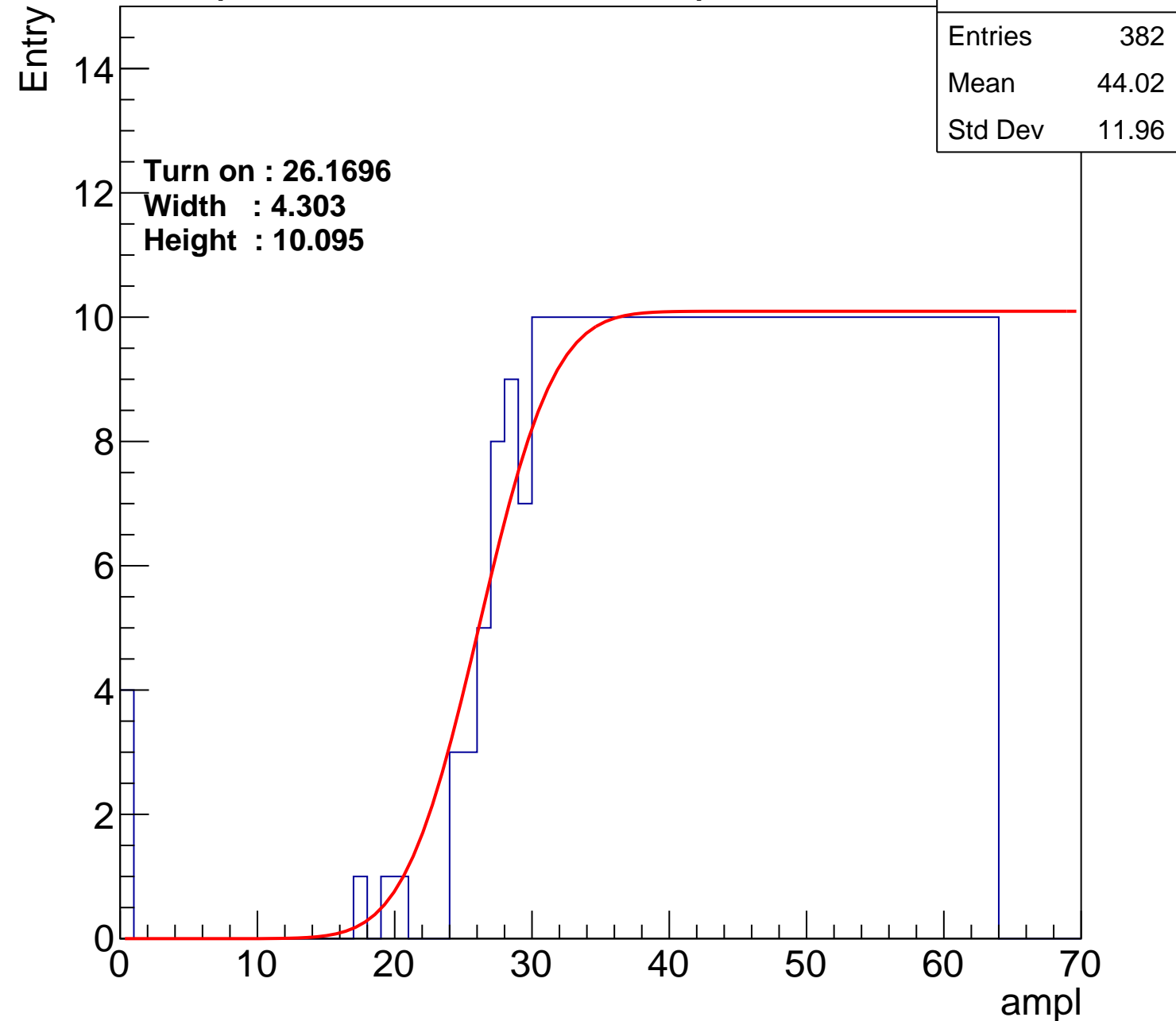
Width : 4.303

Height : 10.095

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch62

calib_packv5_042523_0143.root, FC#7, port C2

Entries	386
Mean	43.9
Std Dev	11.85

Turn on : 26.0977

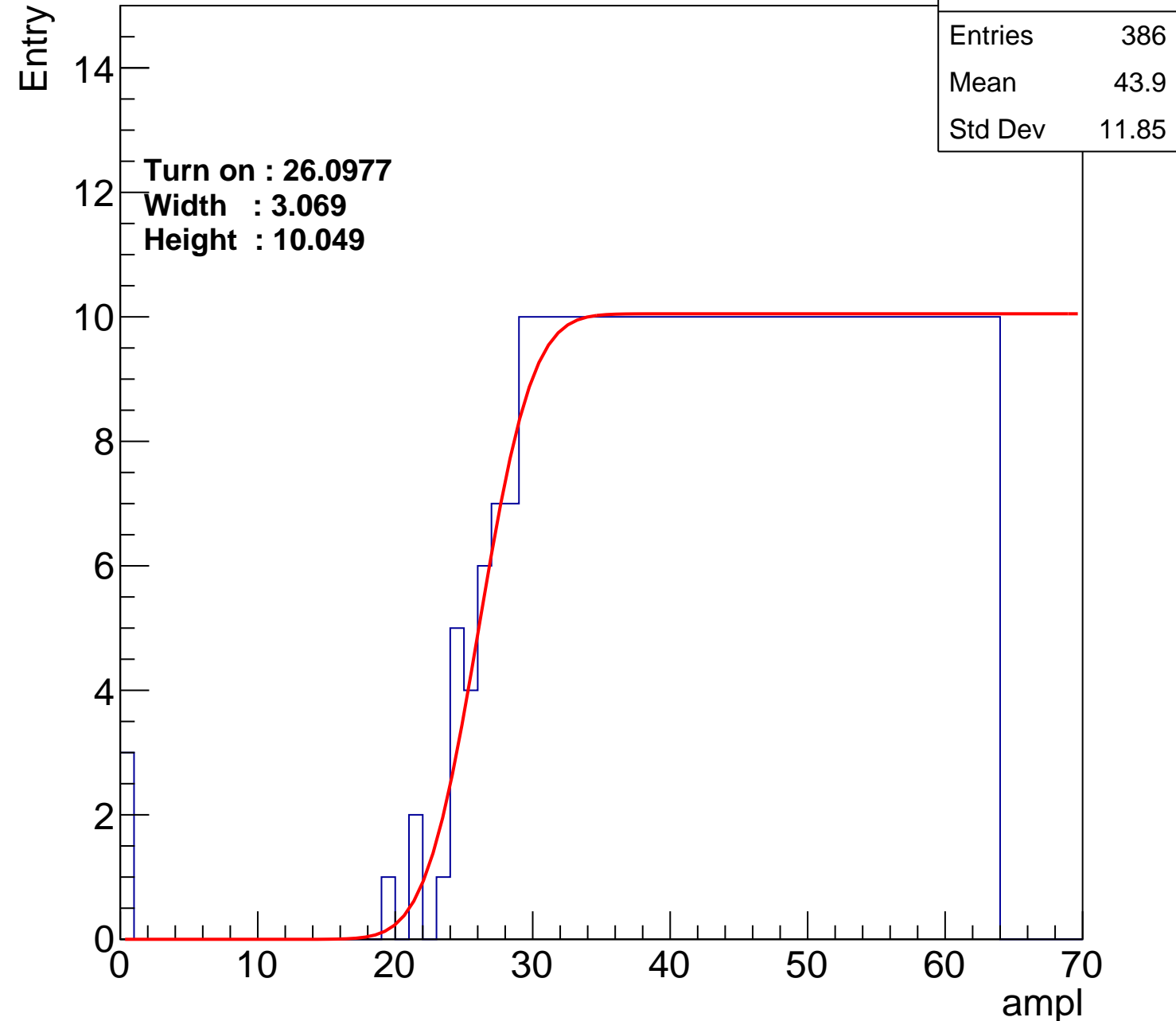
Width : 3.069

Height : 10.049

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch63

calib_packv5_042523_0143.root, FC#7, port C2

Entries	383
Mean	43.77
Std Dev	12.48

Turn on : 27.2300

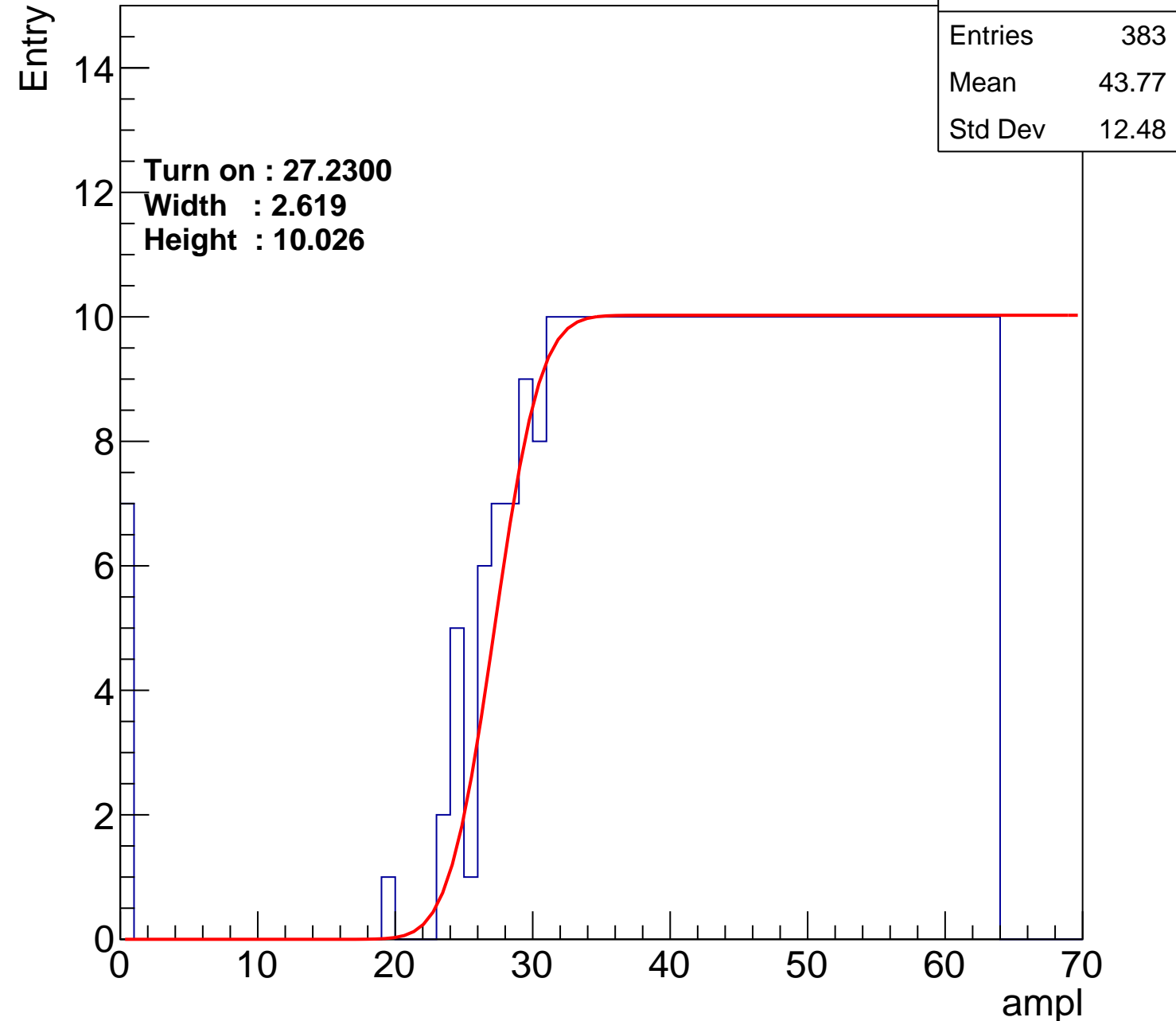
Width : 2.619

Height : 10.026

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch64

calib_packv5_042523_0143.root, FC#7, port C2

Entries	396
Mean	43.43
Std Dev	12.05

Turn on : 24.7698

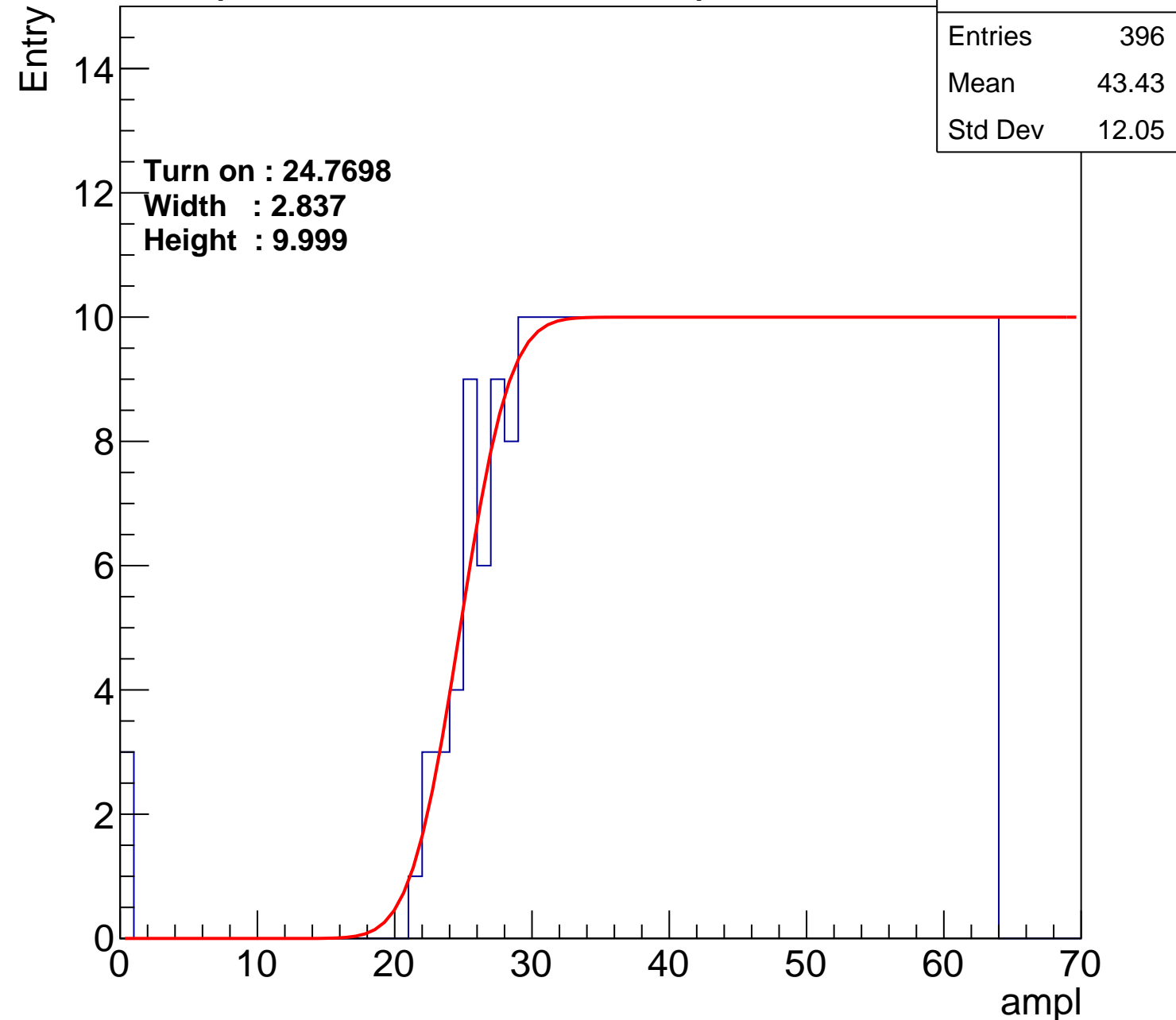
Width : 2.837

Height : 9.999

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch65

calib_packv5_042523_0143.root, FC#7, port C2

Entries	369
Mean	44.63
Std Dev	11.67

Turn on : 27.7012

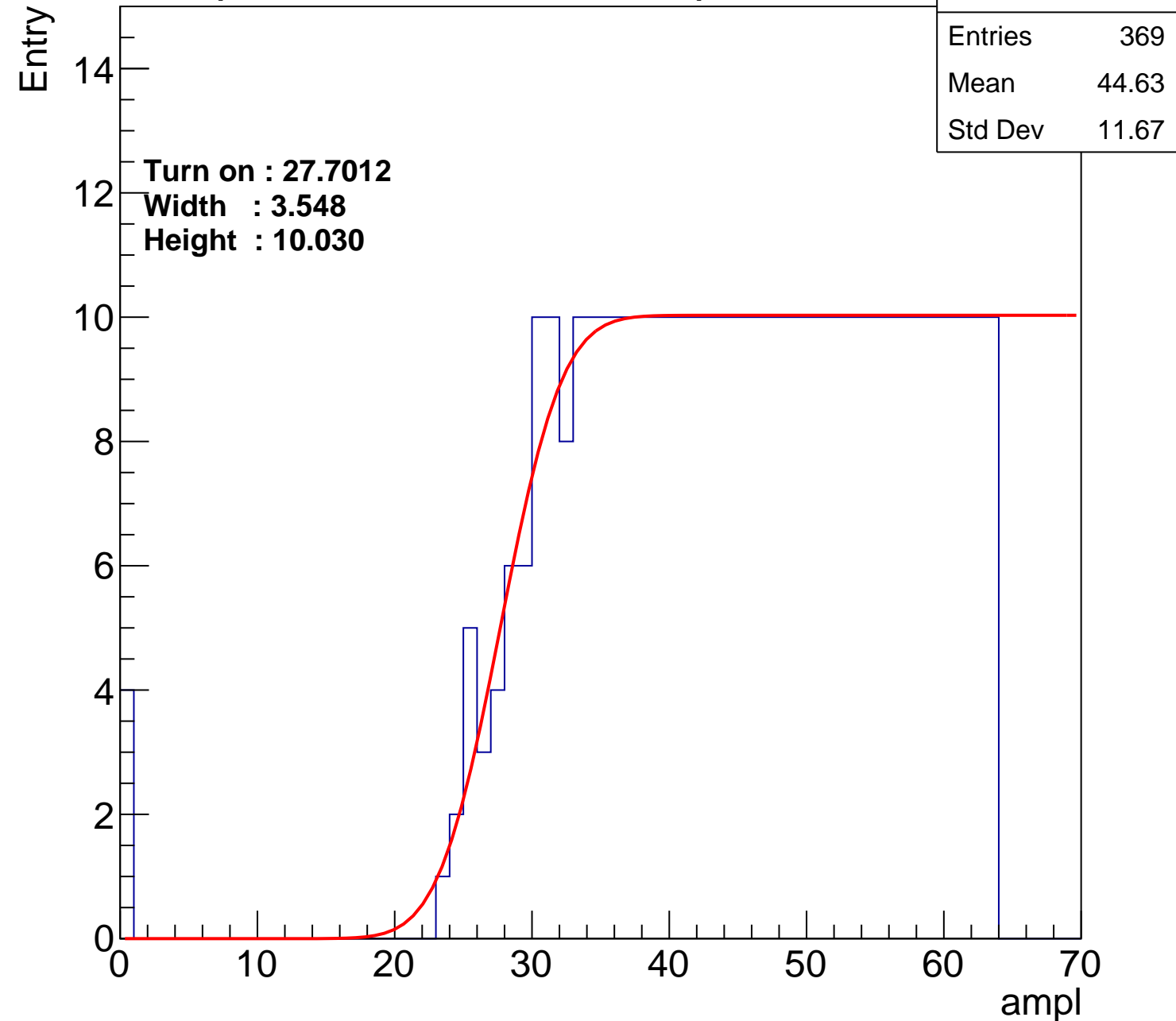
Width : 3.548

Height : 10.030

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch66

calib_packv5_042523_0143.root, FC#7, port C2

Entries	395
Mean	43.47
Std Dev	12.05

Turn on : 25.1924

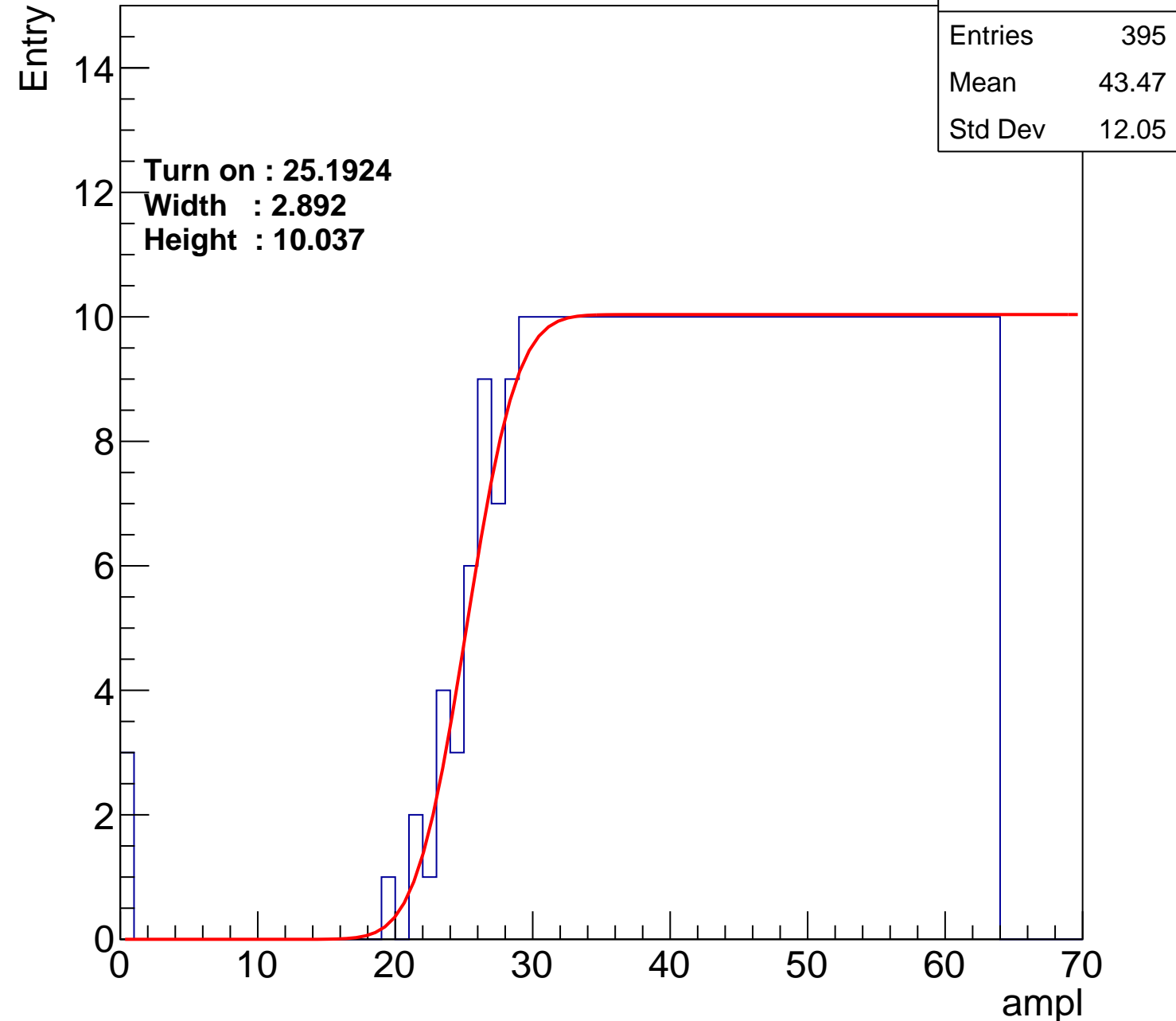
Width : 2.892

Height : 10.037

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch67

calib_packv5_042523_0143.root, FC#7, port C2

Entries	390
Mean	43.34
Std Dev	12.87

Turn on : 25.9762

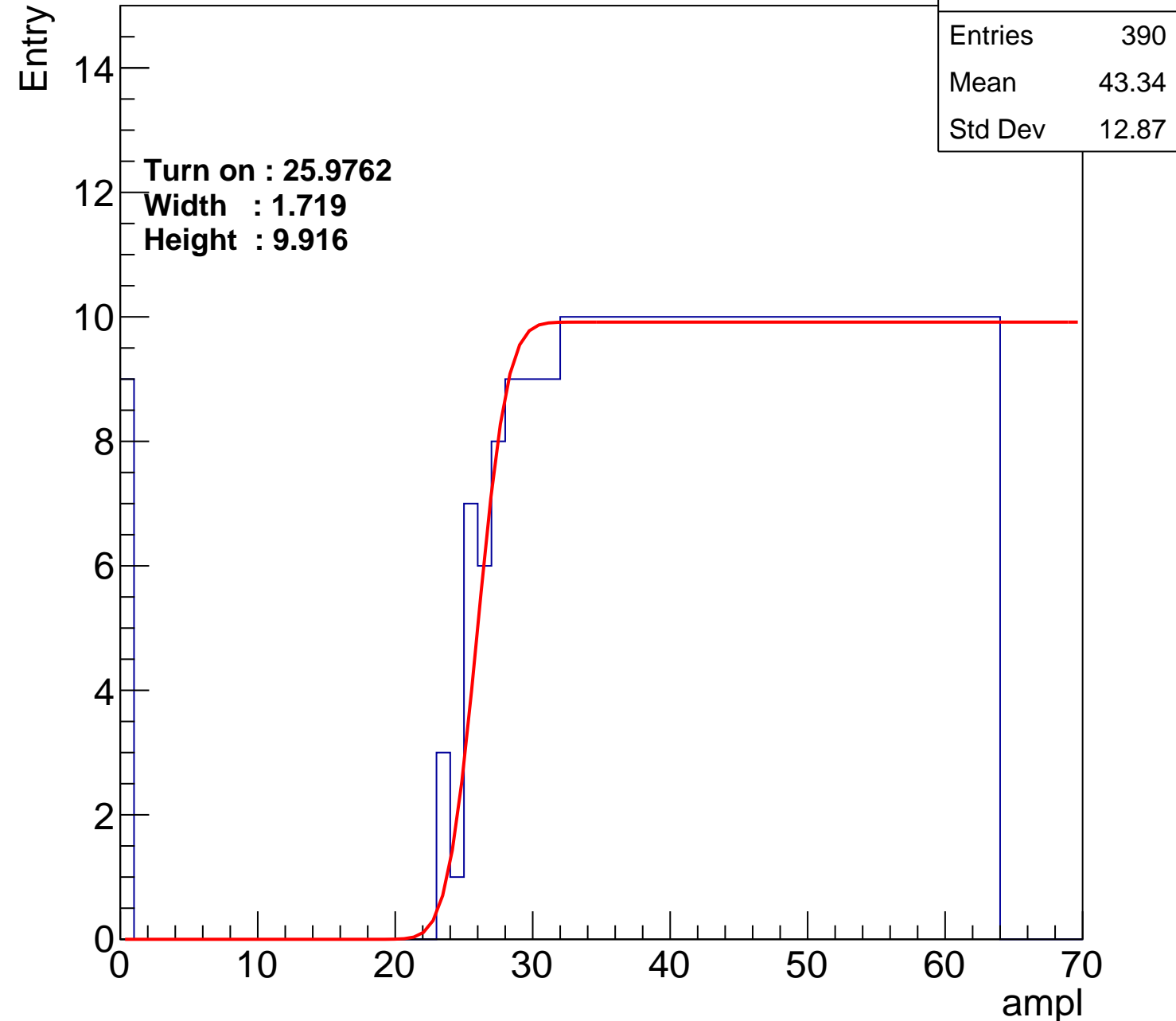
Width : 1.719

Height : 9.916

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch68

calib_packv5_042523_0143.root, FC#7, port C2

Entries	401
Mean	43.26
Std Dev	11.95

Turn on : 24.3016

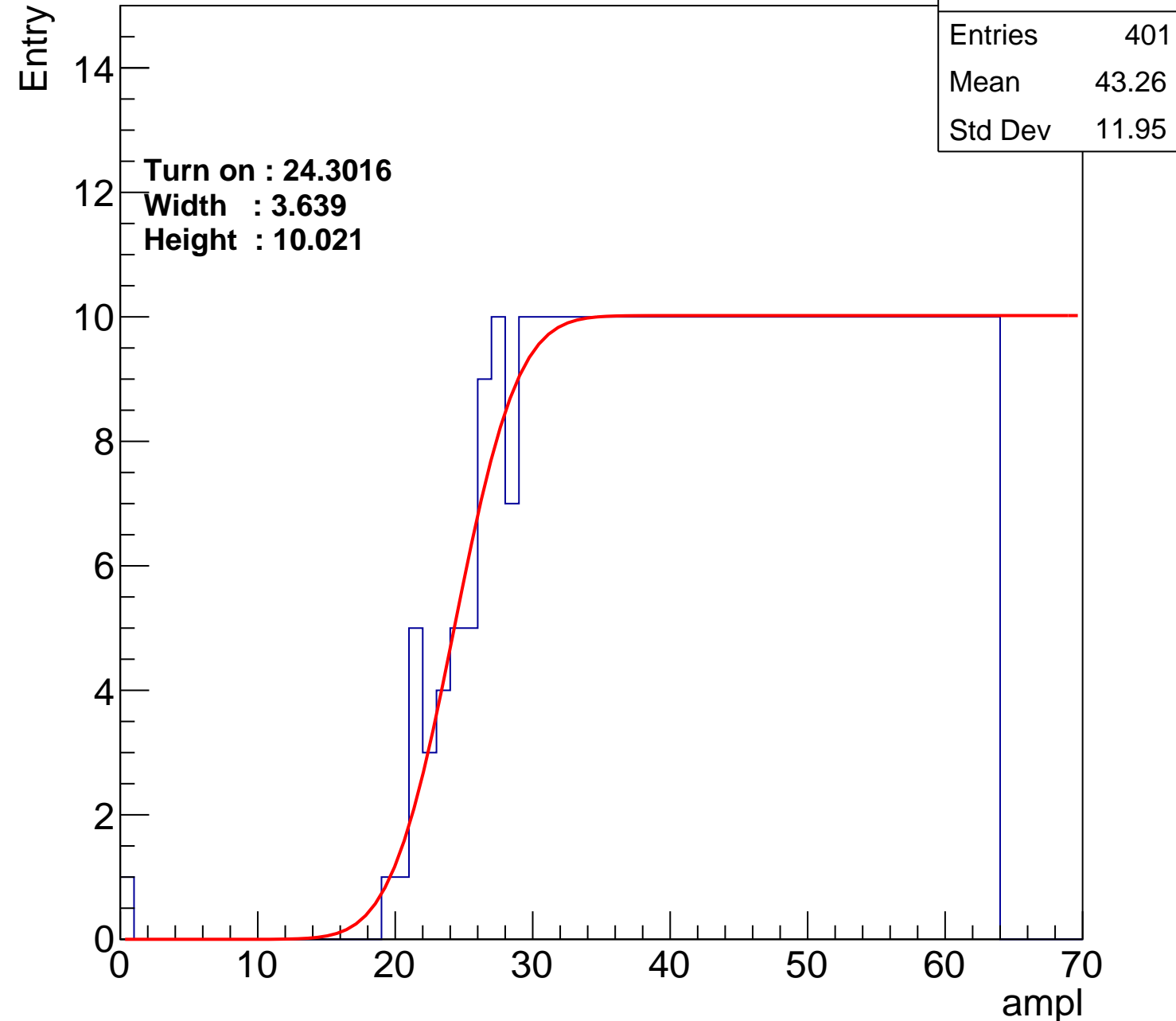
Width : 3.639

Height : 10.021

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch69

calib_packv5_042523_0143.root, FC#7, port C2

Entries	395
Mean	43.44
Std Dev	12.09

Turn on : 24.7027

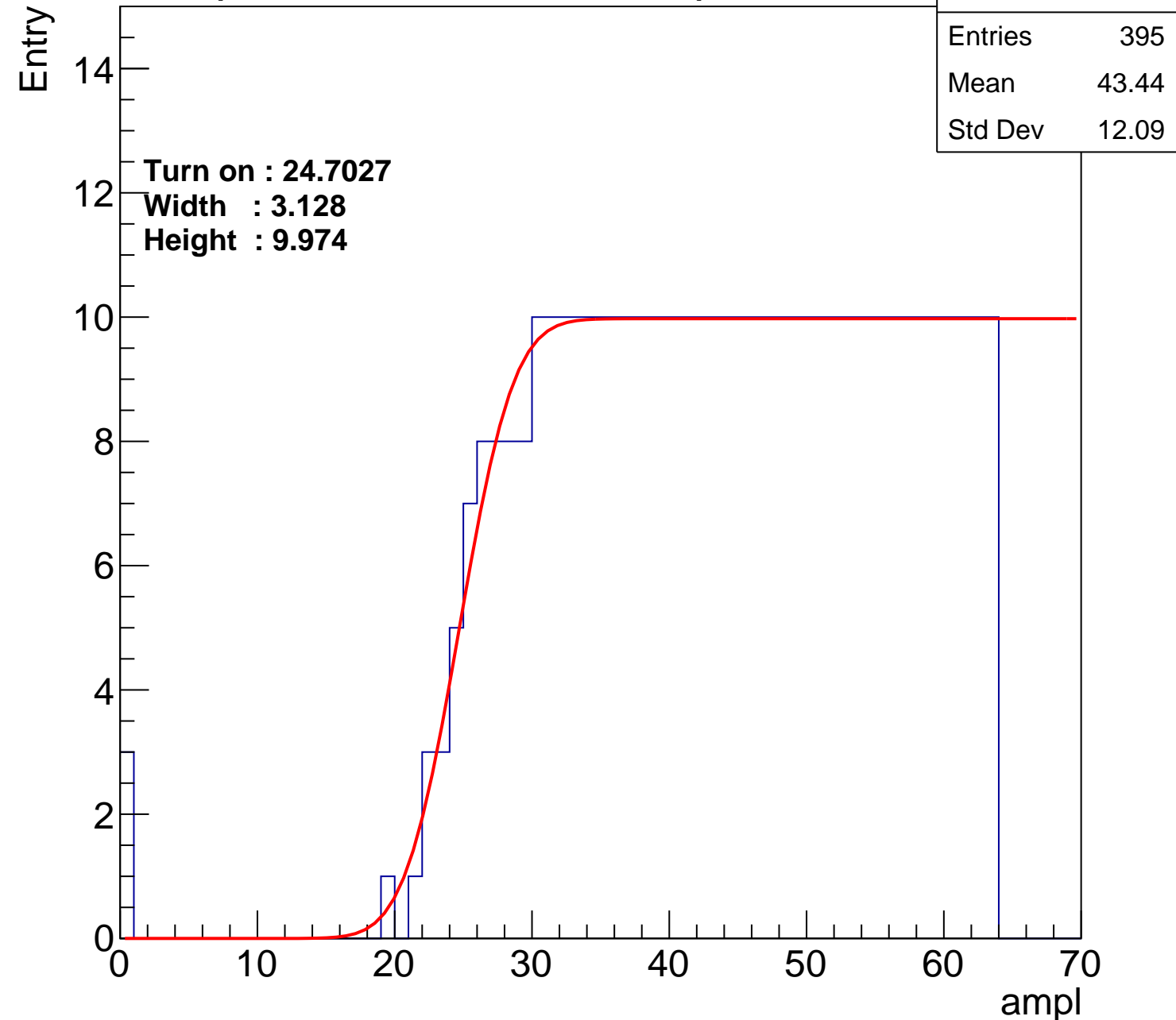
Width : 3.128

Height : 9.974

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch70

calib_packv5_042523_0143.root, FC#7, port C2

Entries	398
Mean	43.33
Std Dev	12.06

Turn on : 25.0269

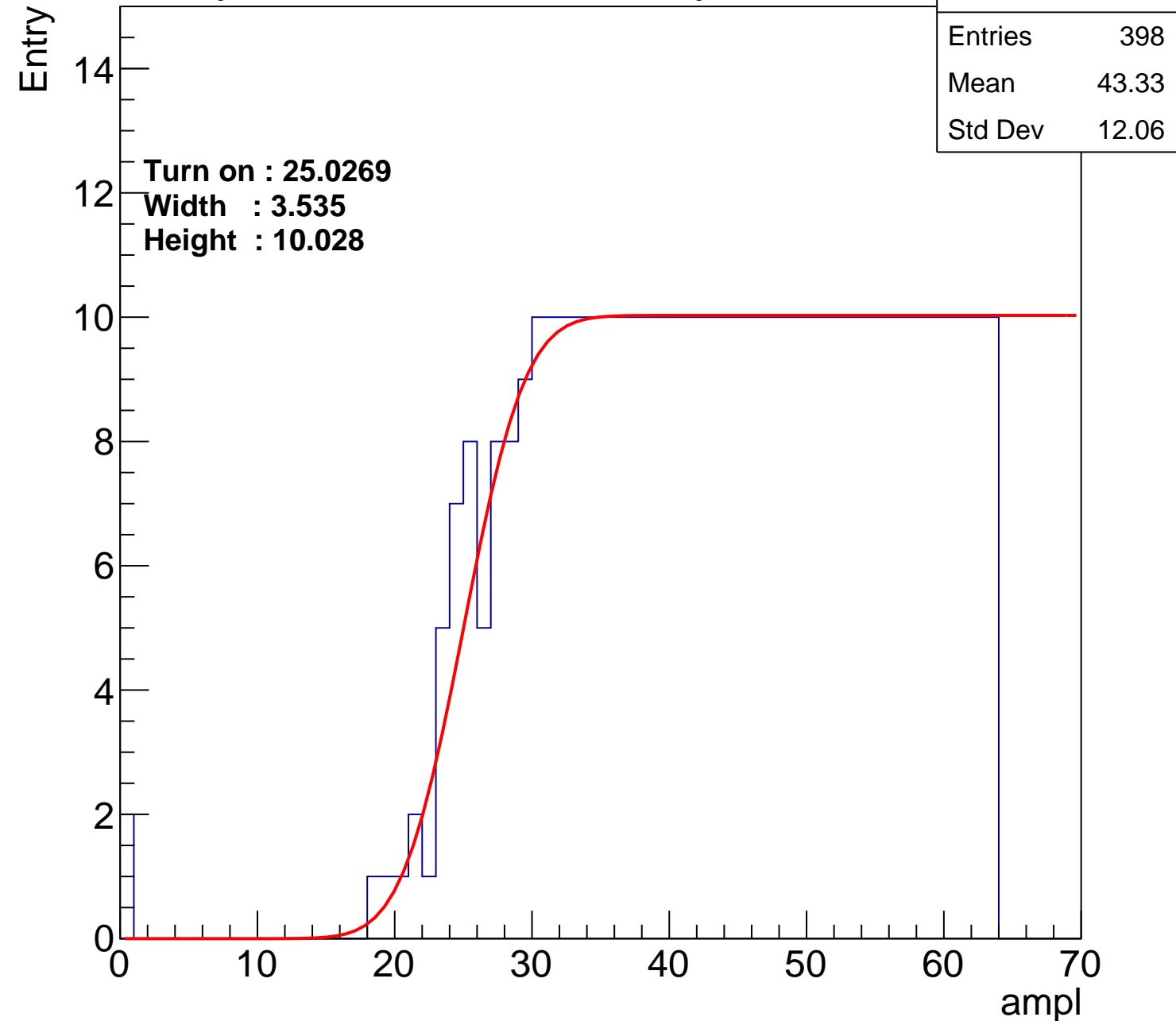
Width : 3.535

Height : 10.028

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch71

calib_packv5_042523_0143.root, FC#7, port C2

Entries	401
Mean	43.25
Std Dev	12.02

Turn on : 23.9347

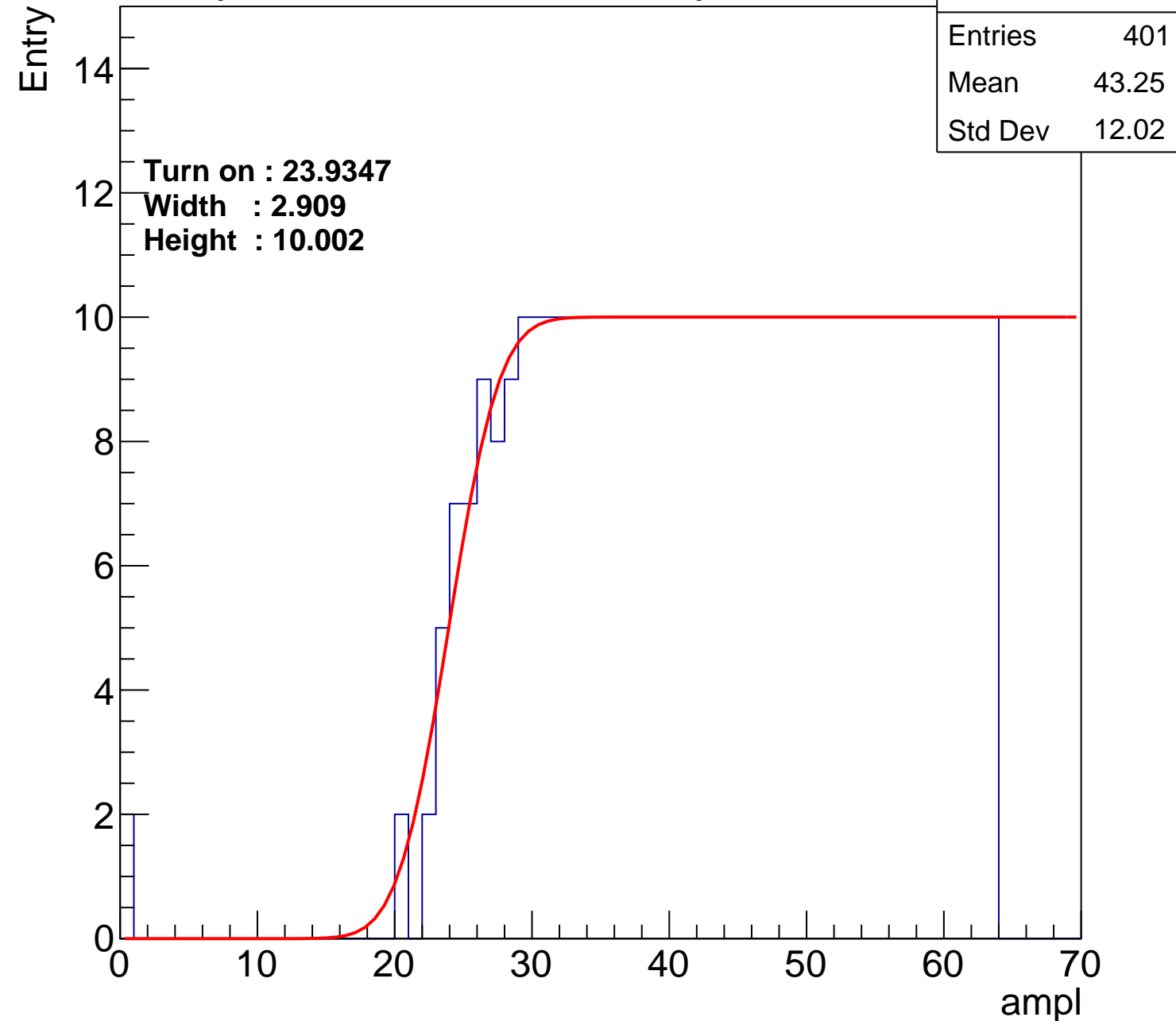
Width : 2.909

Height : 10.002

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch72

calib_packv5_042523_0143.root, FC#7, port C2

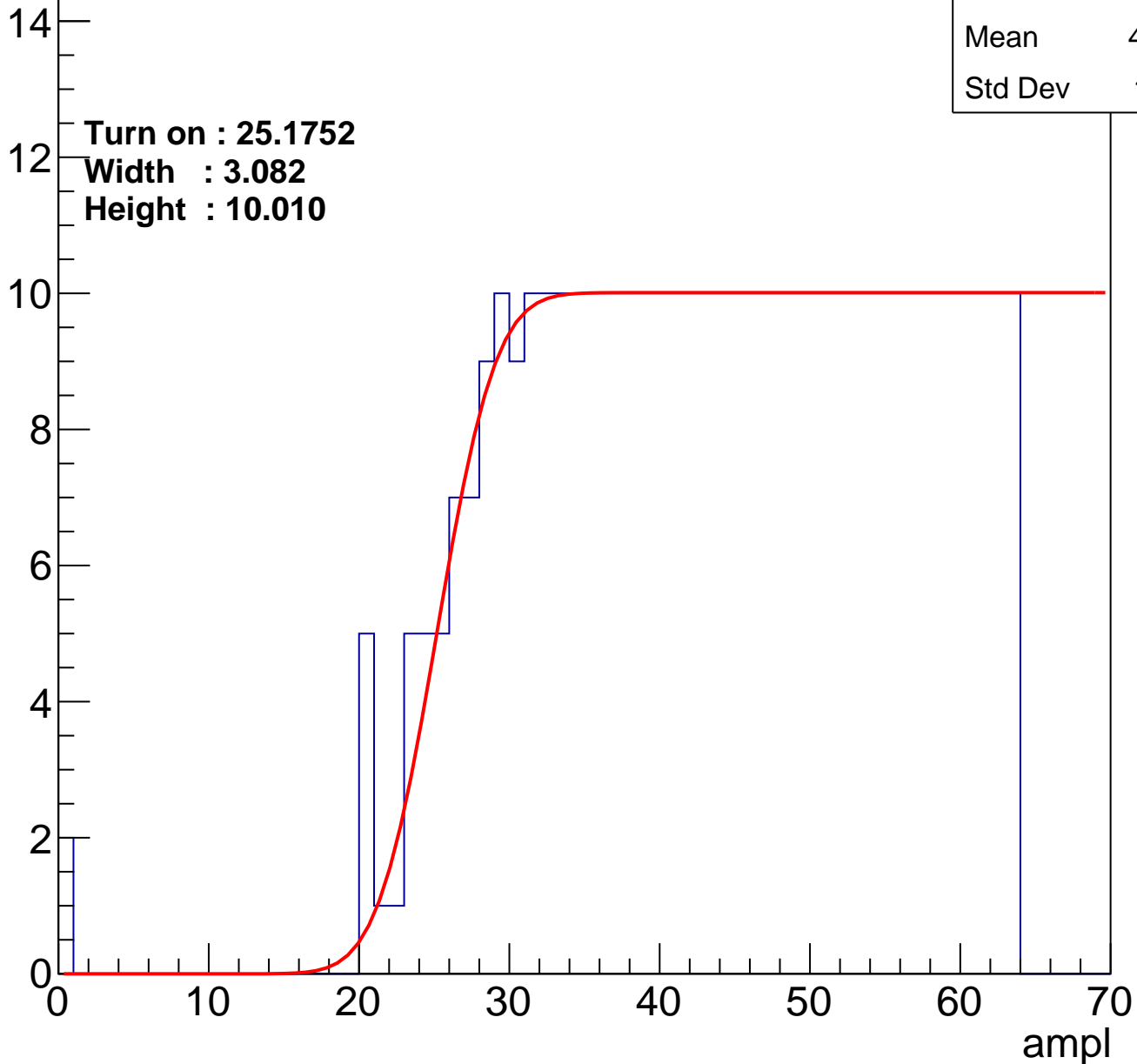
Entries	396
Mean	43.42
Std Dev	12.01

Turn on : 25.1752

Width : 3.082

Height : 10.010

Entry



B1L103S, U1-ch73

calib_packv5_042523_0143.root, FC#7, port C2

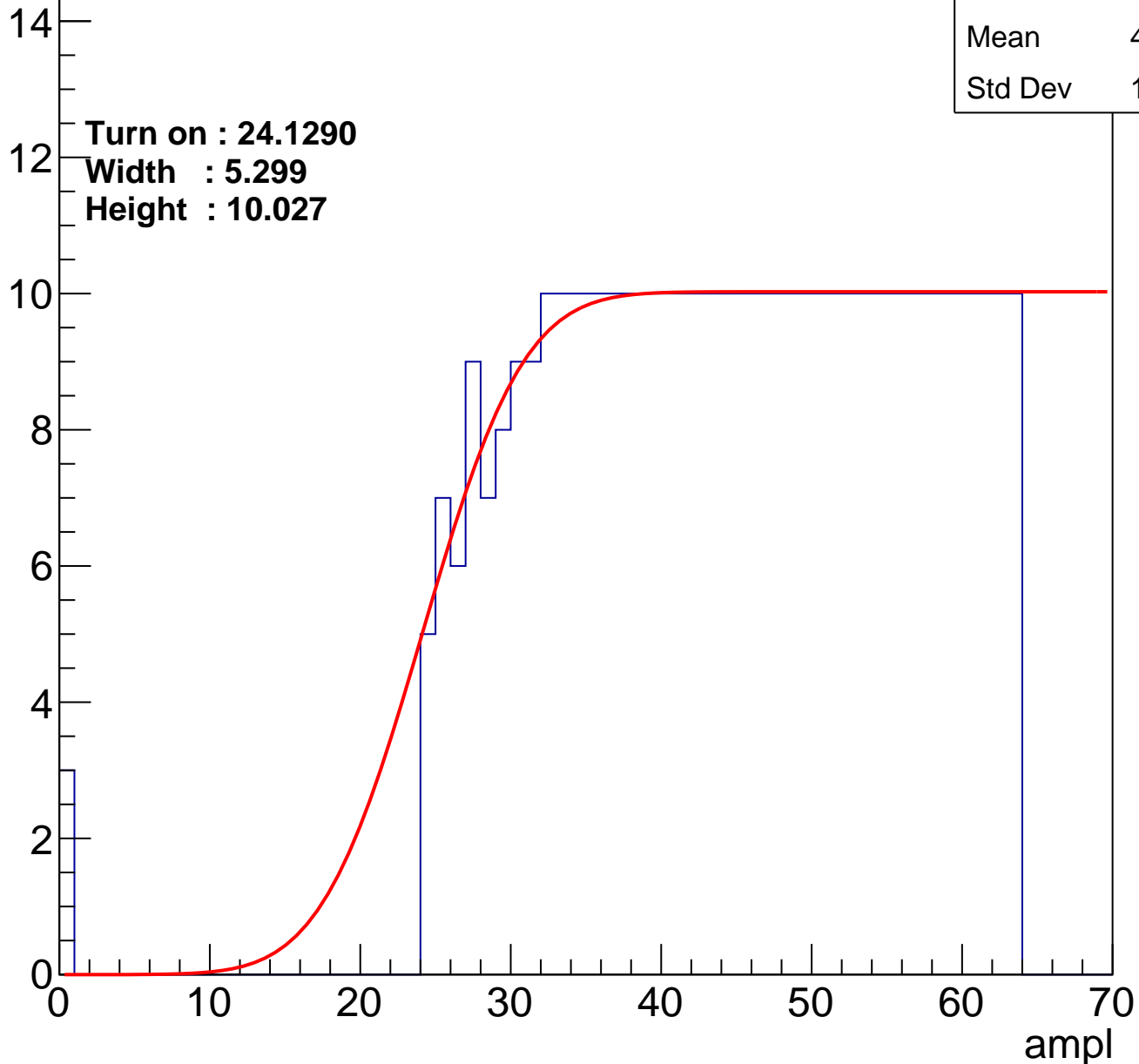
Entries	383
Mean	44.05
Std Dev	11.76

Turn on : 24.1290

Width : 5.299

Height : 10.027

Entry



B1L103S, U1-ch74

calib_packv5_042523_0143.root, FC#7, port C2

Entries	402
Mean	42.96
Std Dev	12.6

Turn on : 24.2419

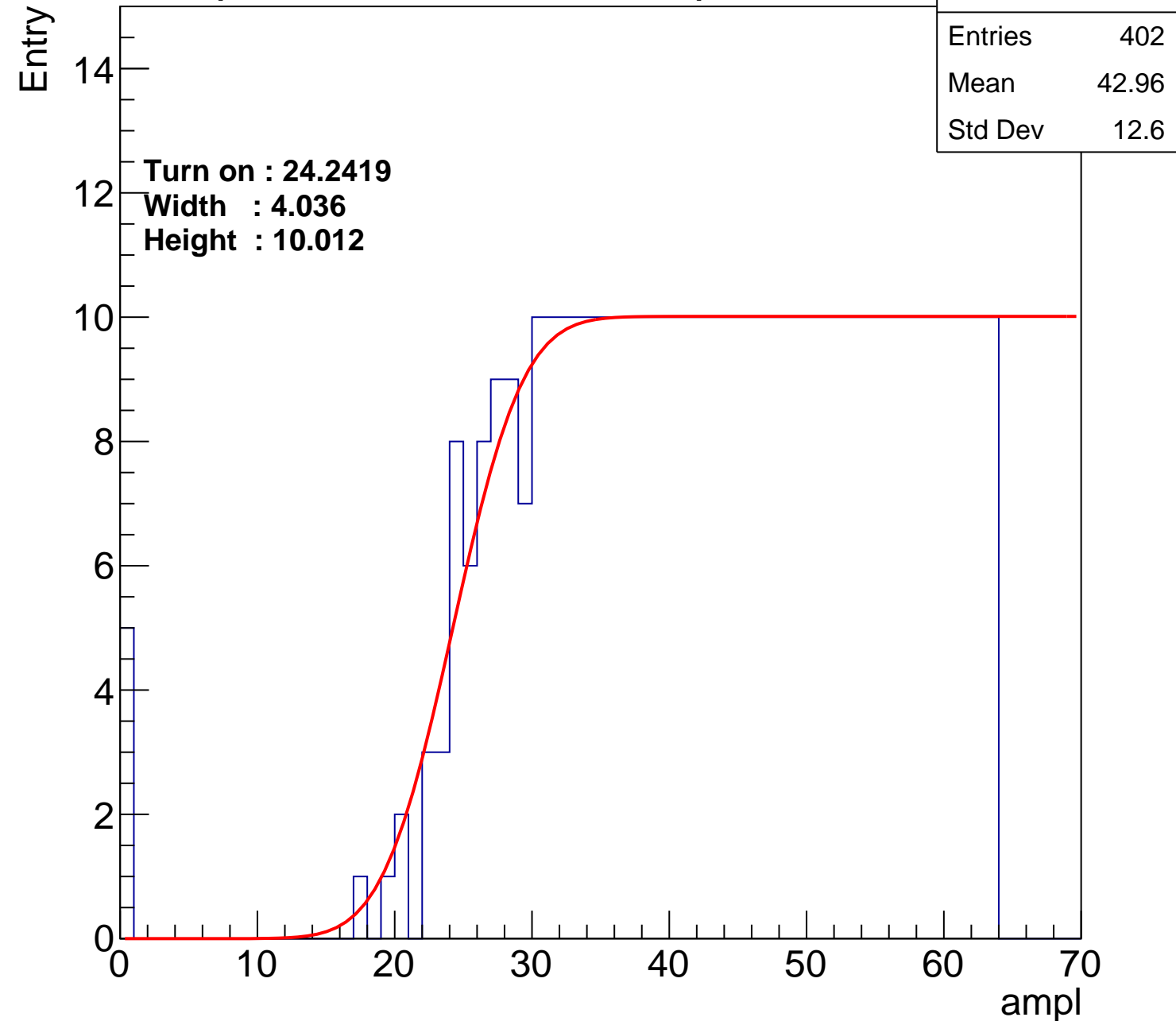
Width : 4.036

Height : 10.012

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch75

calib_packv5_042523_0143.root, FC#7, port C2

Entries	408
Mean	42.65
Std Dev	12.81

Turn on : 23.8245

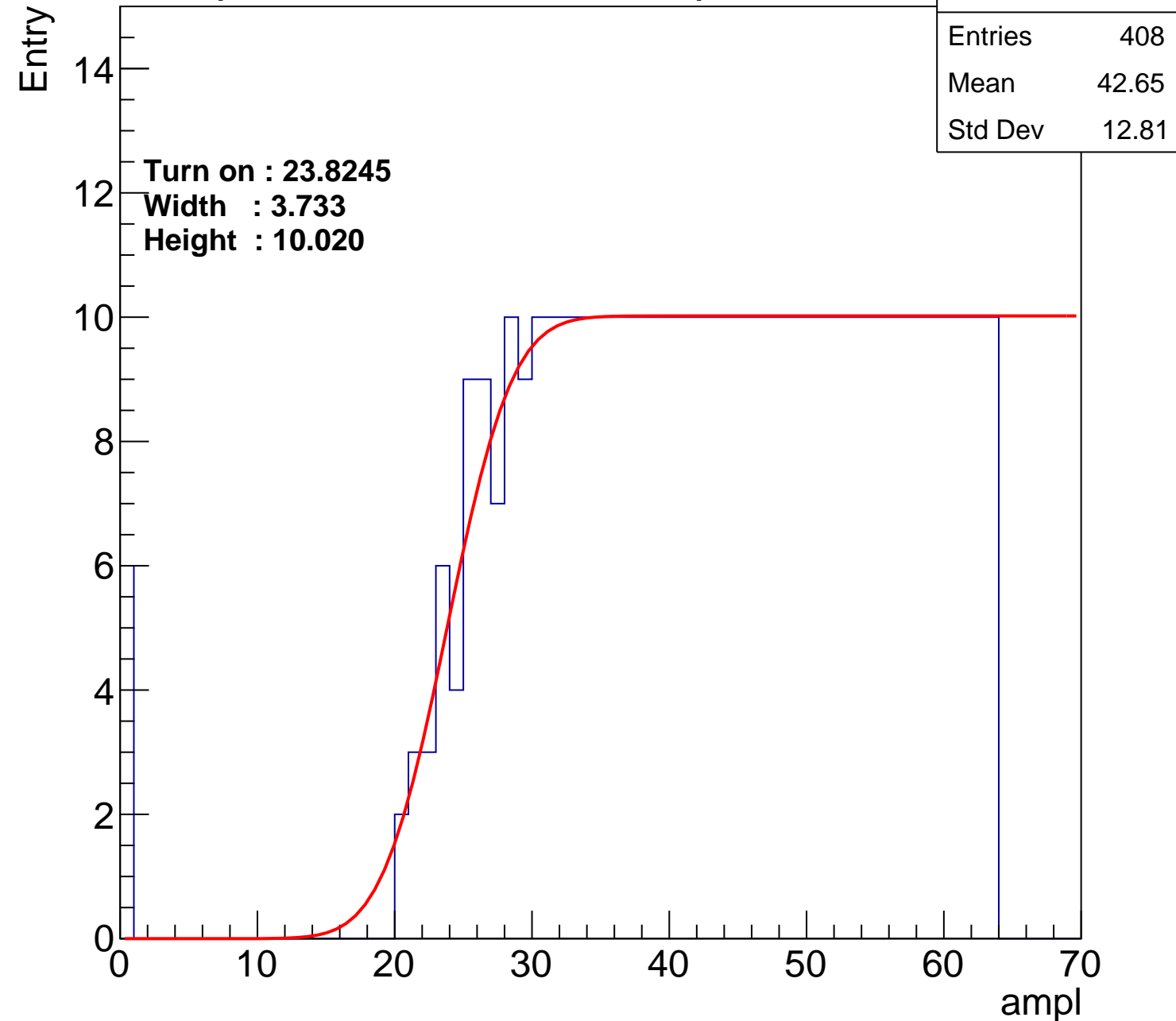
Width : 3.733

Height : 10.020

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch76

calib_packv5_042523_0143.root, FC#7, port C2

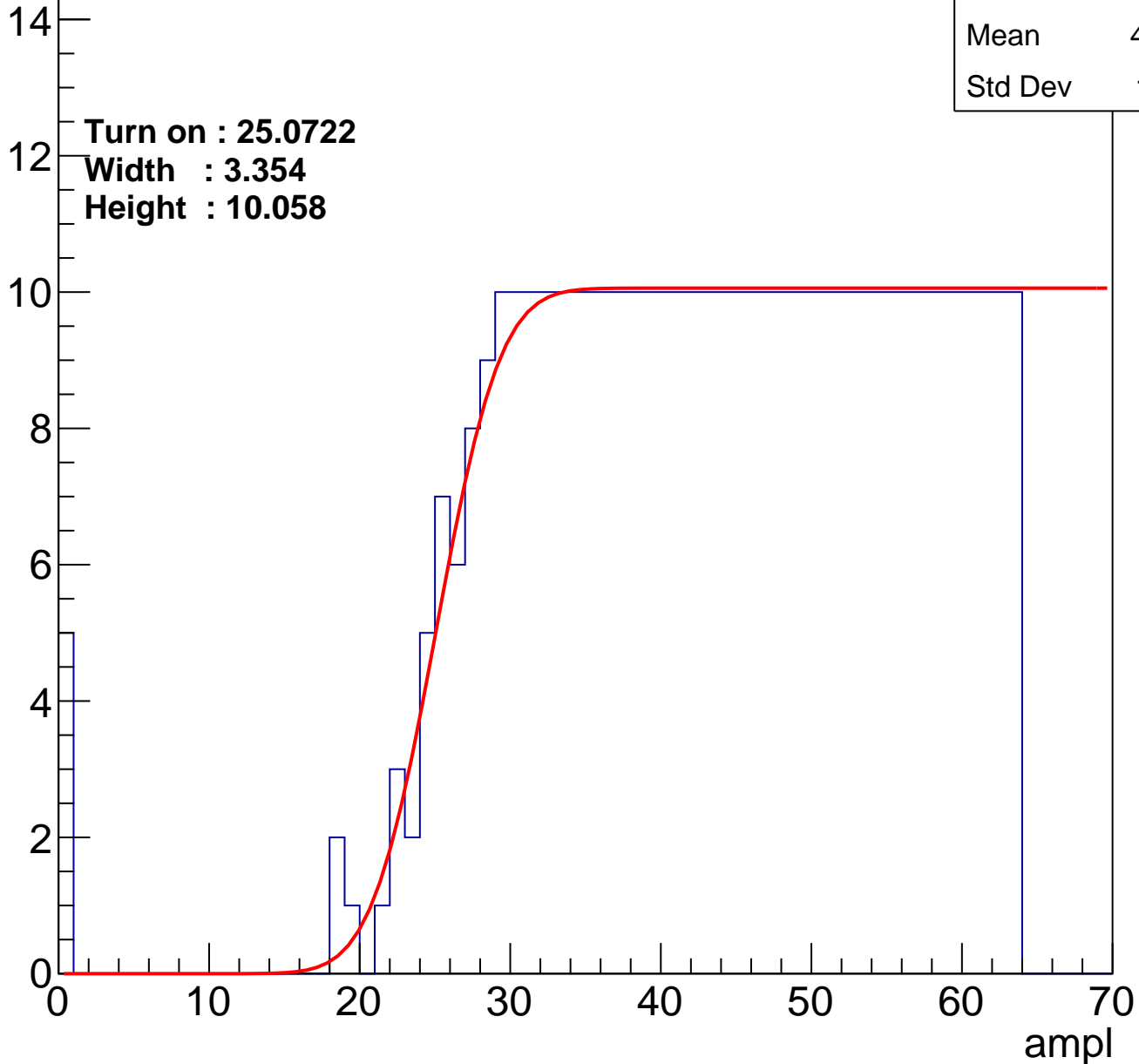
Entries	399
Mean	43.13
Std Dev	12.51

Turn on : 25.0722

Width : 3.354

Height : 10.058

Entry



B1L103S, U1-ch77

calib_packv5_042523_0143.root, FC#7, port C2

Entries	373
Mean	44.6
Std Dev	11.35

Turn on : 27.1471

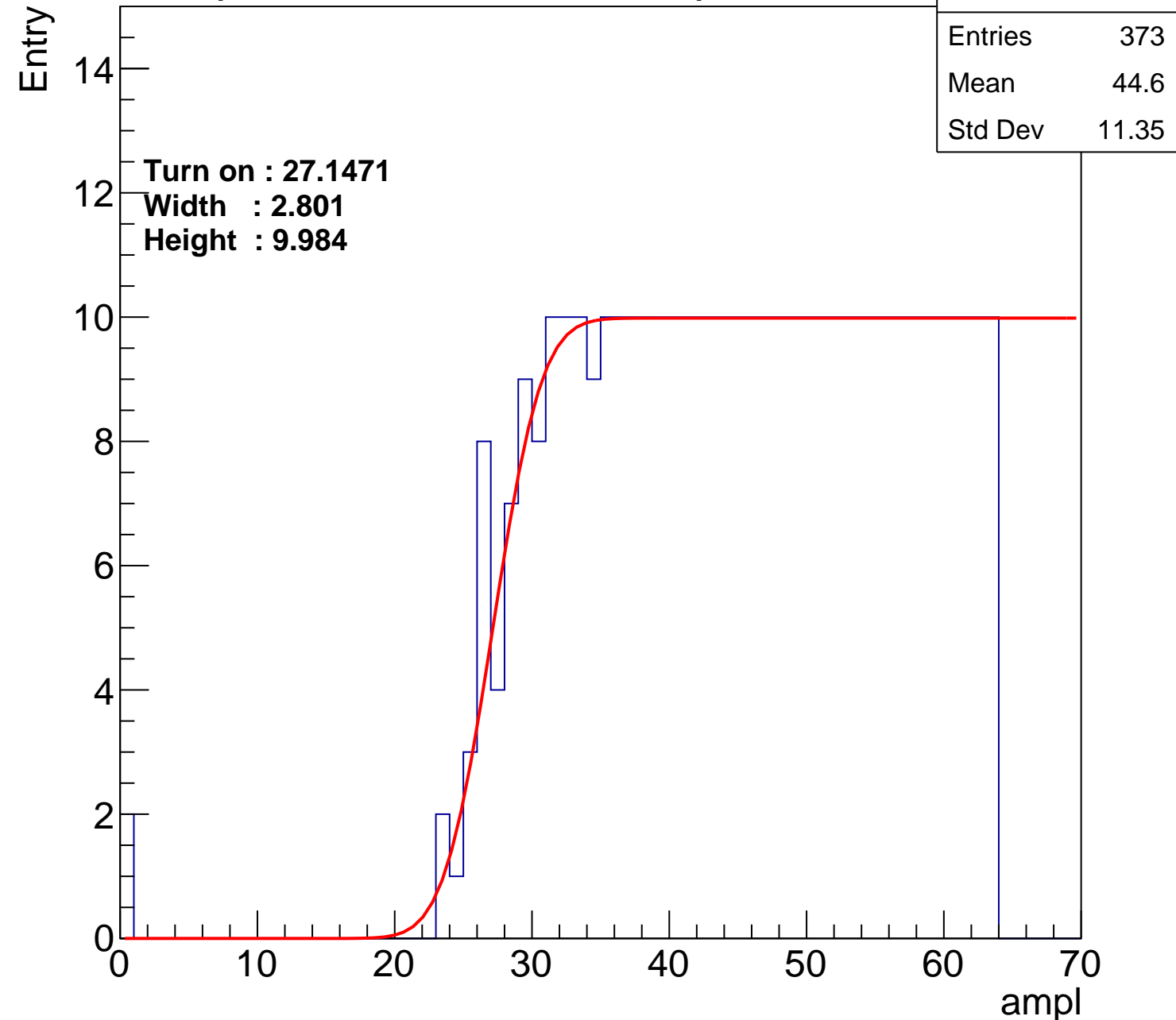
Width : 2.801

Height : 9.984

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch78

calib_packv5_042523_0143.root, FC#7, port C2

Entries	403
Mean	43.09
Std Dev	12.17

Turn on : 23.9505

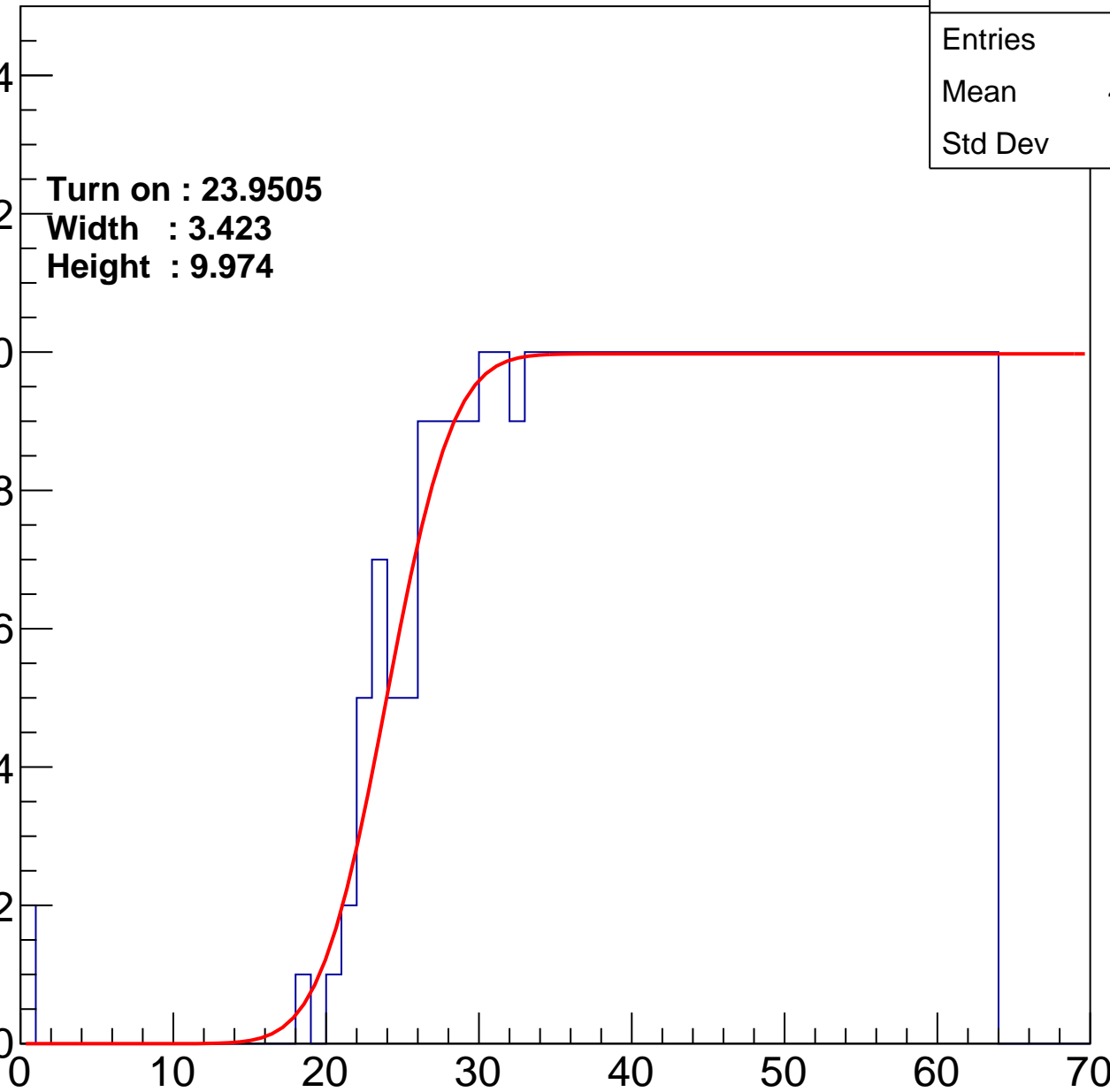
Width : 3.423

Height : 9.974

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch79

calib_packv5_042523_0143.root, FC#7, port C2

Entries	382
Mean	44.16
Std Dev	11.58

Turn on : 26.4372

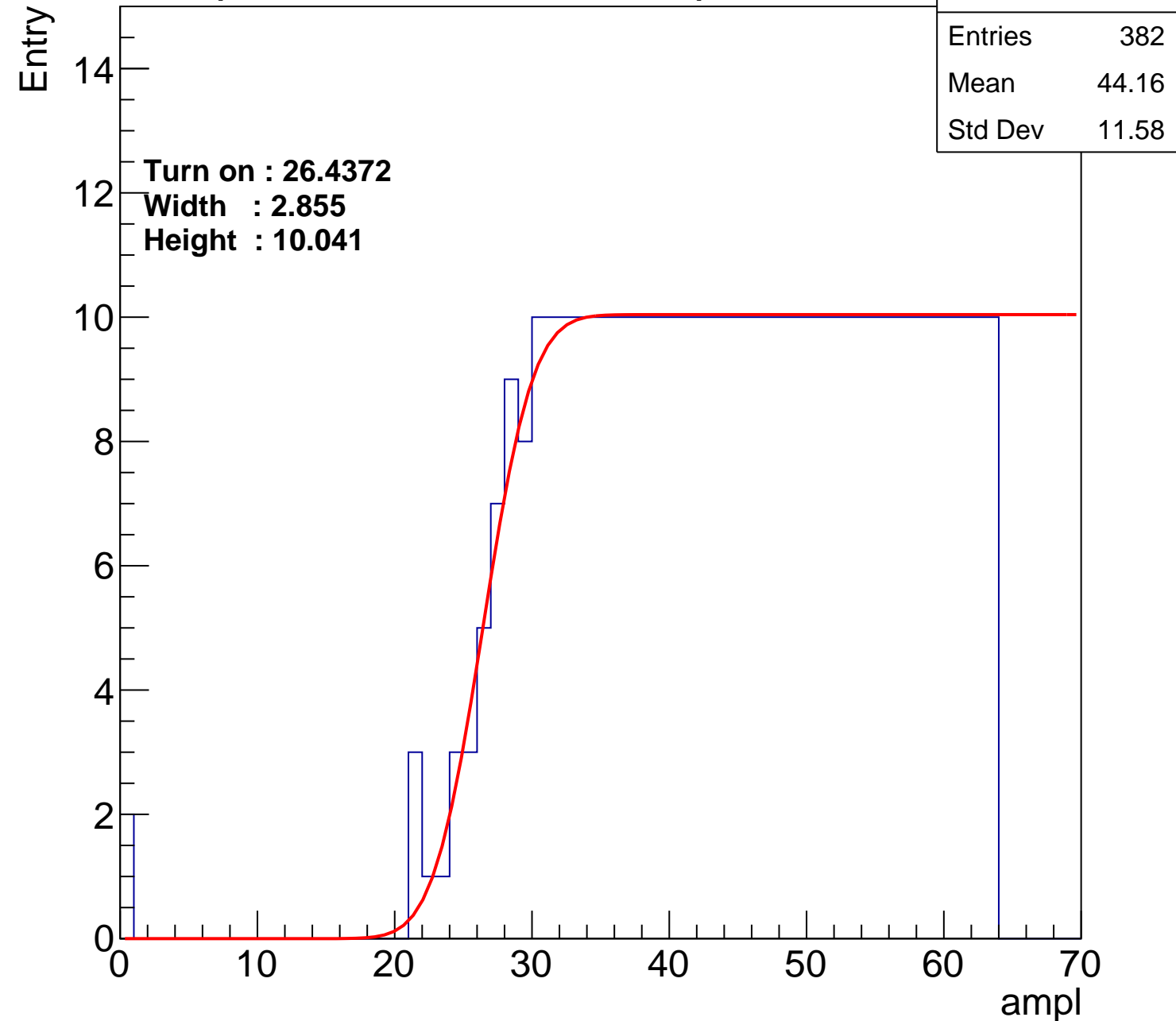
Width : 2.855

Height : 10.041

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch80

calib_packv5_042523_0143.root, FC#7, port C2

Entries	376
Mean	44.35
Std Dev	11.67

Turn on : 26.8897

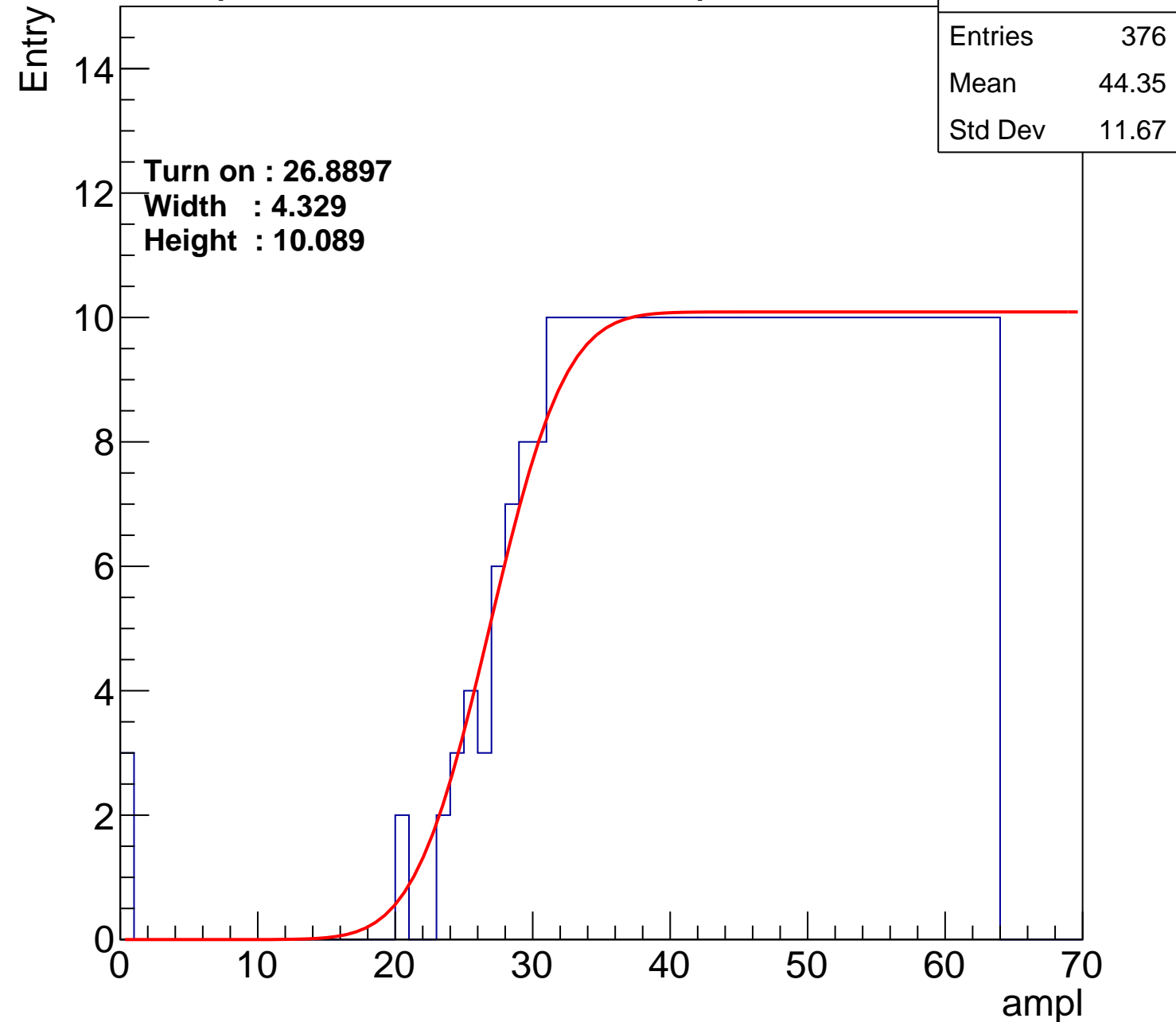
Width : 4.329

Height : 10.089

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch81

calib_packv5_042523_0143.root, FC#7, port C2

Entries	385
Mean	43.95
Std Dev	11.82

Turn on : 26.1047

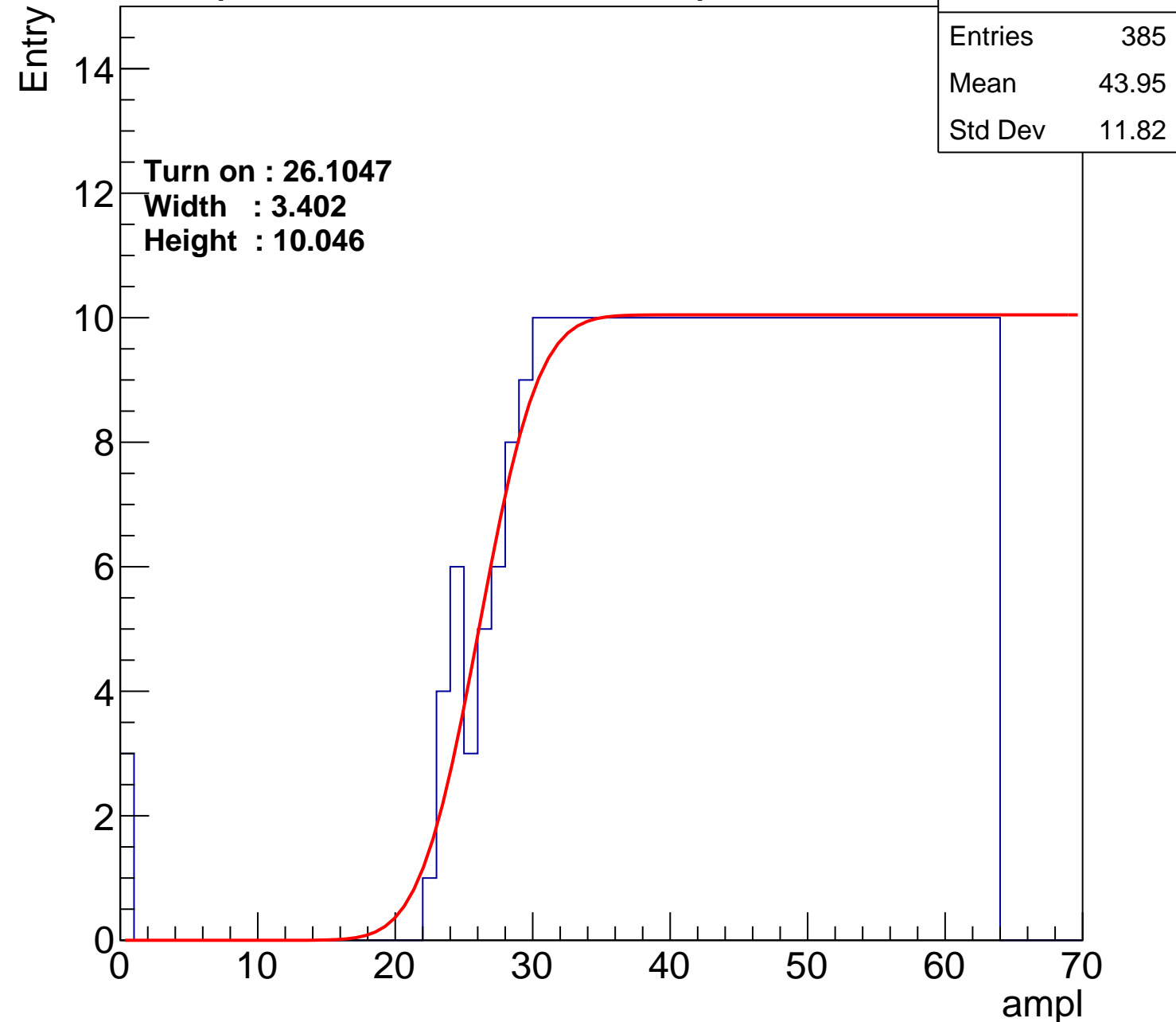
Width : 3.402

Height : 10.046

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch82

calib_packv5_042523_0143.root, FC#7, port C2

Entries	412
Mean	42.62
Std Dev	12.52

Turn on : 23.9408

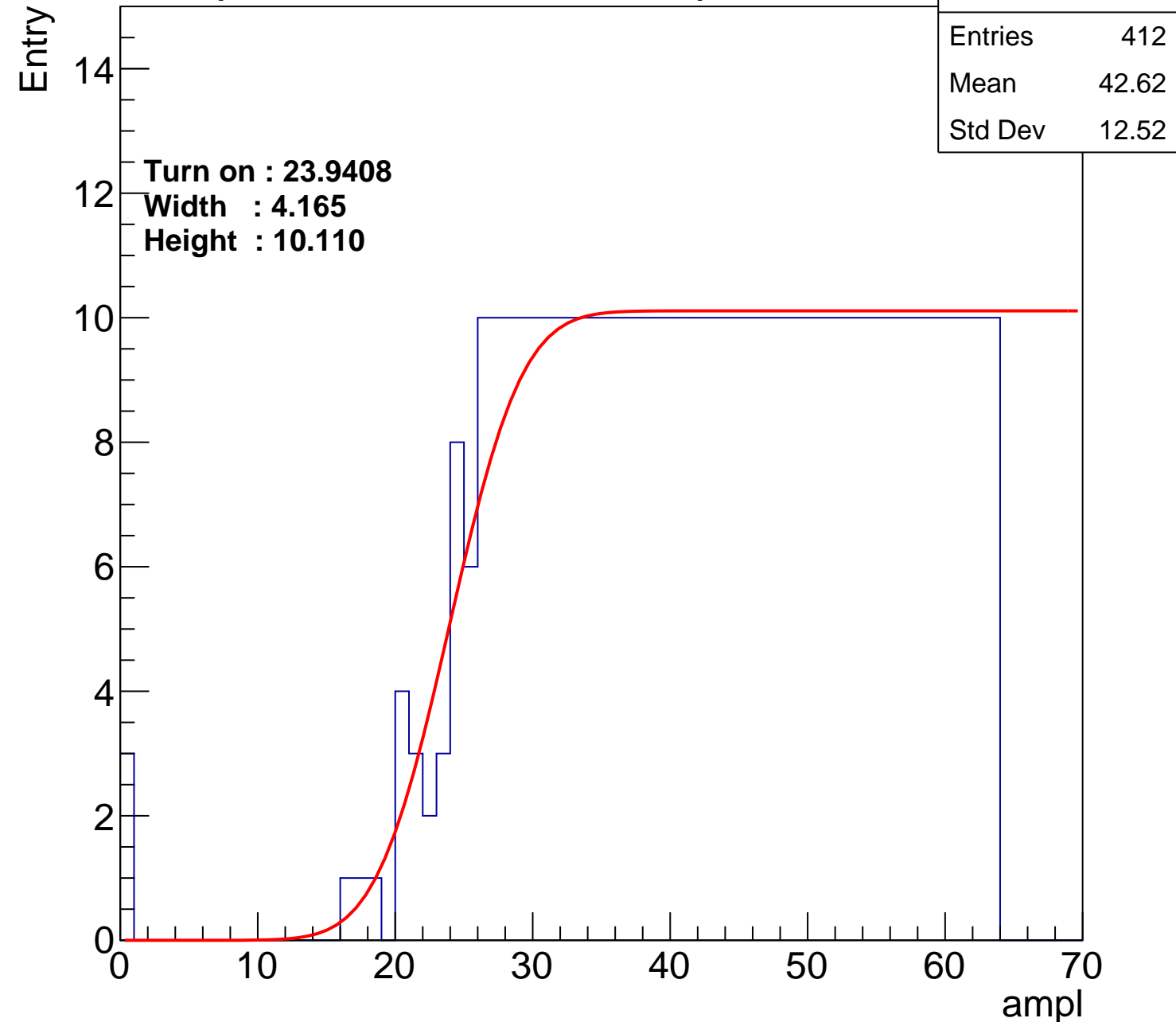
Width : 4.165

Height : 10.110

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch83

calib_packv5_042523_0143.root, FC#7, port C2

Entries	382
Mean	44.05
Std Dev	11.81

Turn on : 26.2623

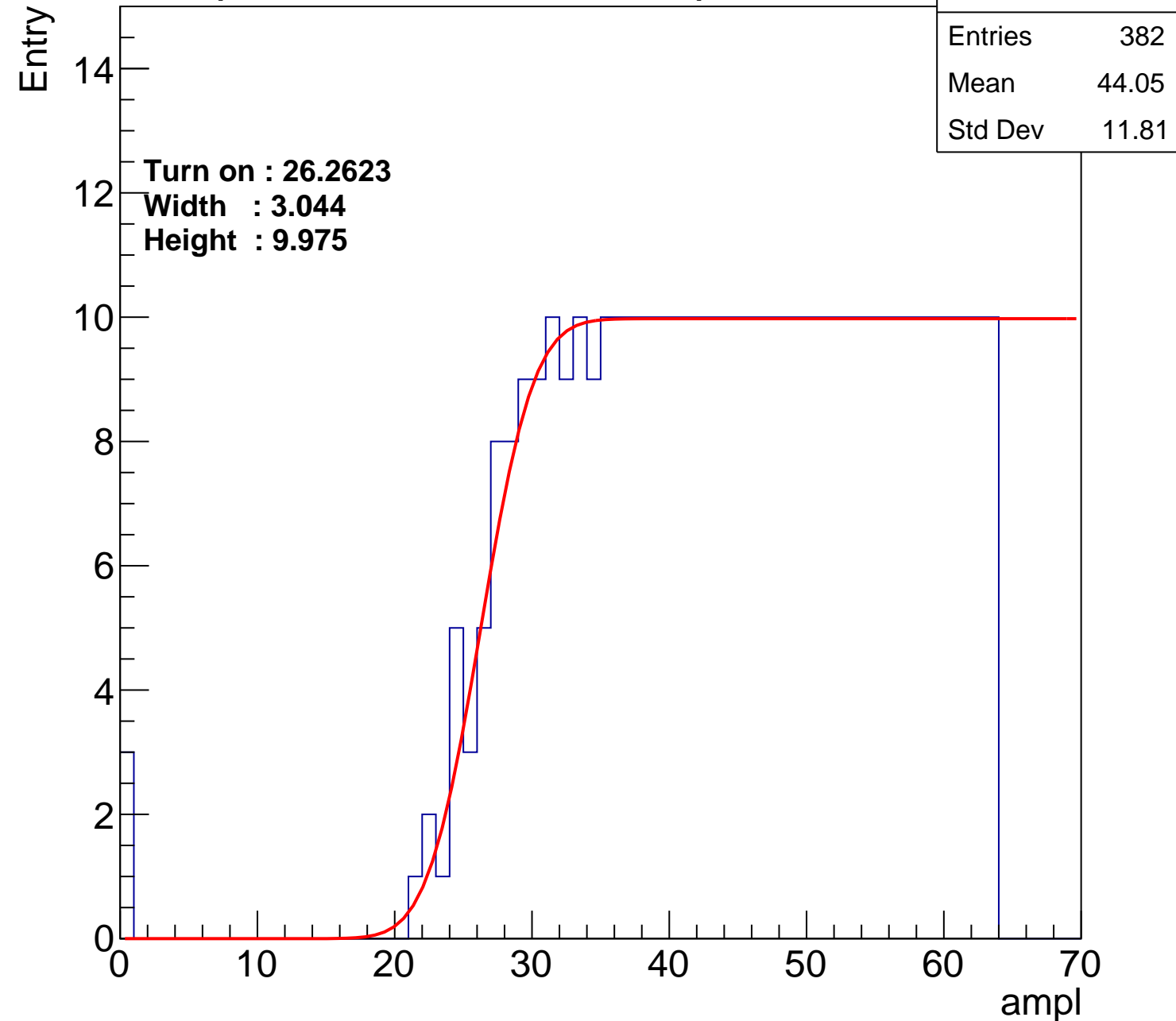
Width : 3.044

Height : 9.975

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch84

calib_packv5_042523_0143.root, FC#7, port C2

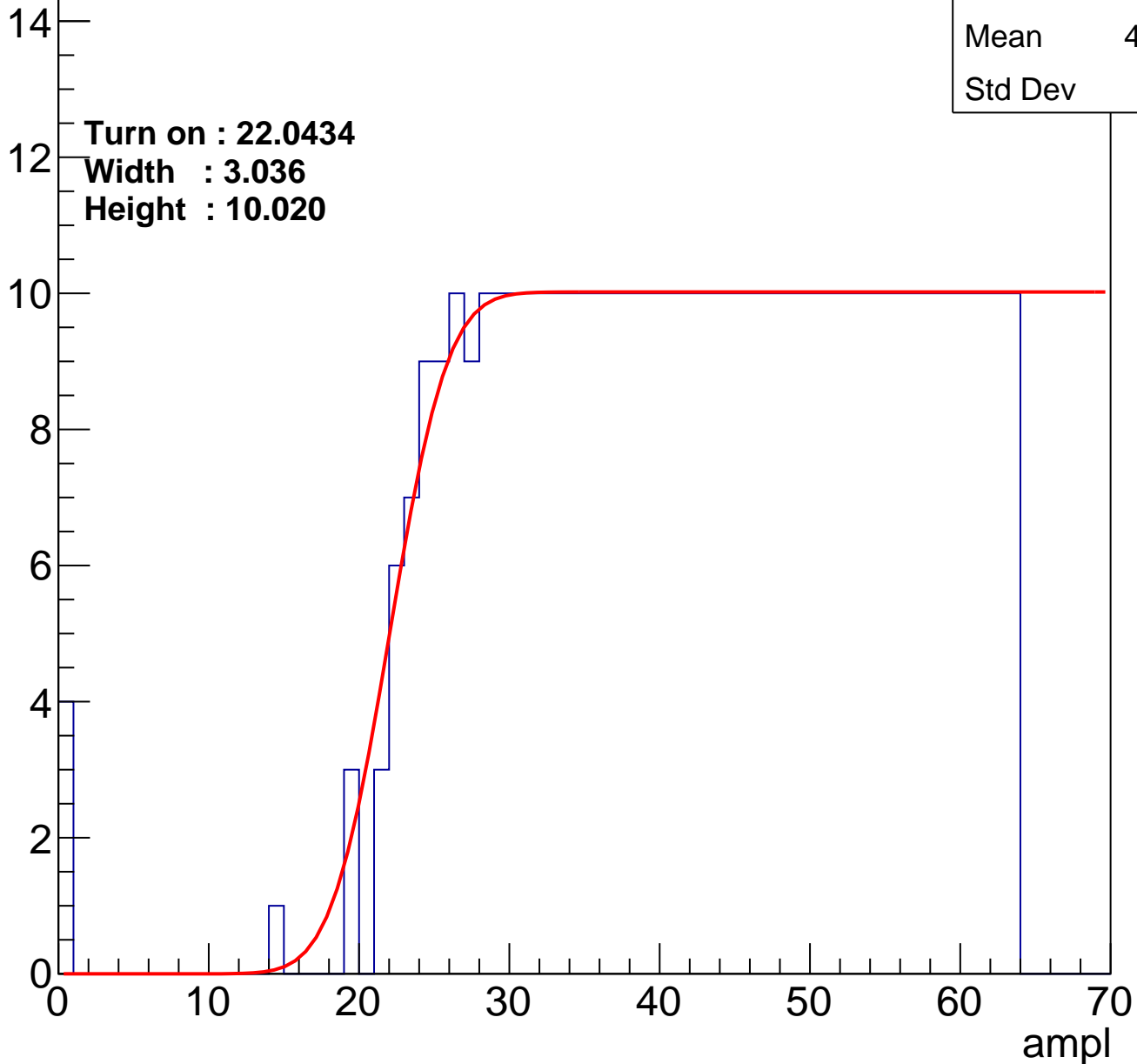
Entries	421
Mean	42.16
Std Dev	12.8

Turn on : 22.0434

Width : 3.036

Height : 10.020

Entry



B1L103S, U1-ch85

calib_packv5_042523_0143.root, FC#7, port C2

Entries	381
Mean	44.25
Std Dev	11.41

Turn on : 26.1965

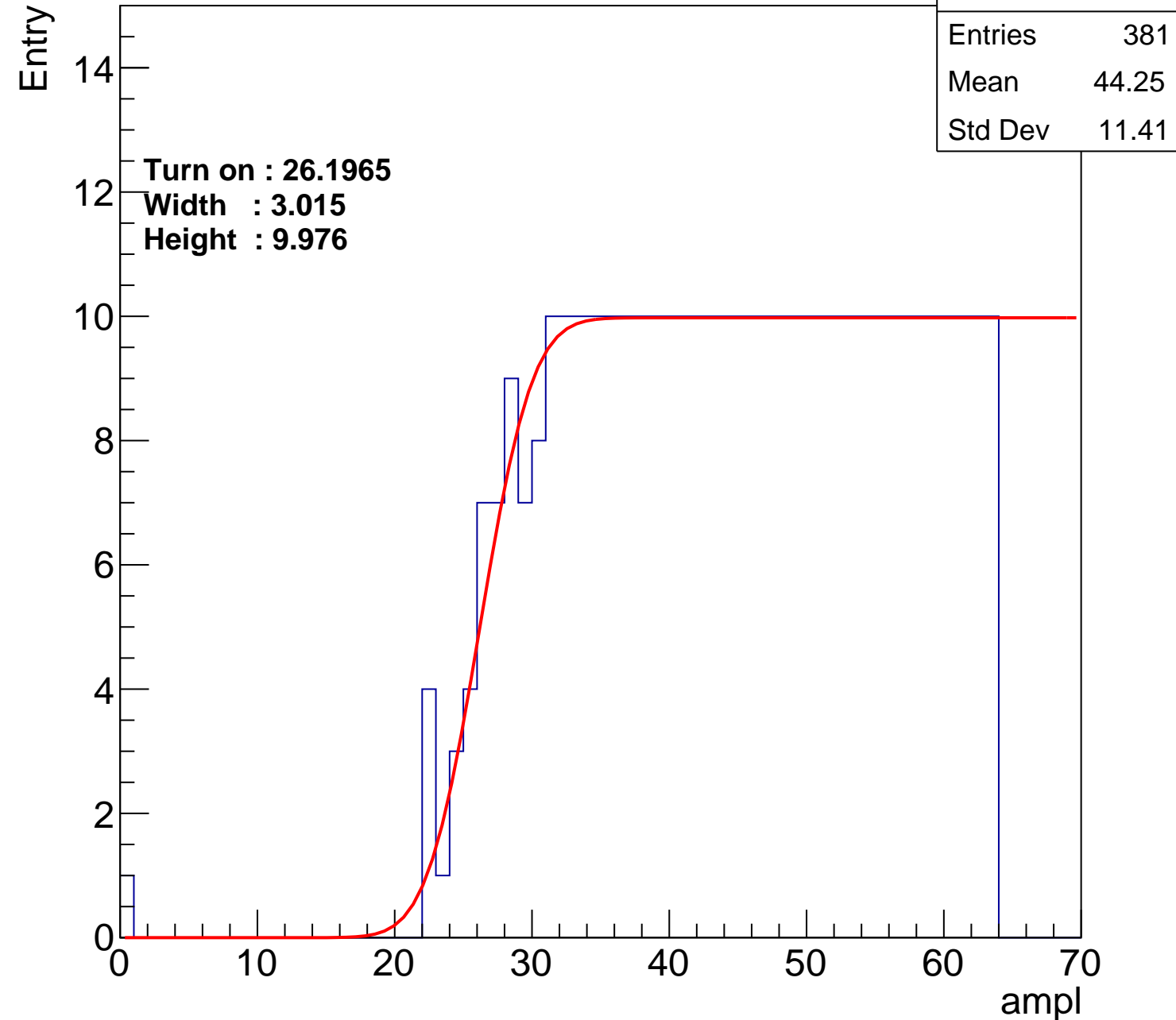
Width : 3.015

Height : 9.976

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch86

calib_packv5_042523_0143.root, FC#7, port C2

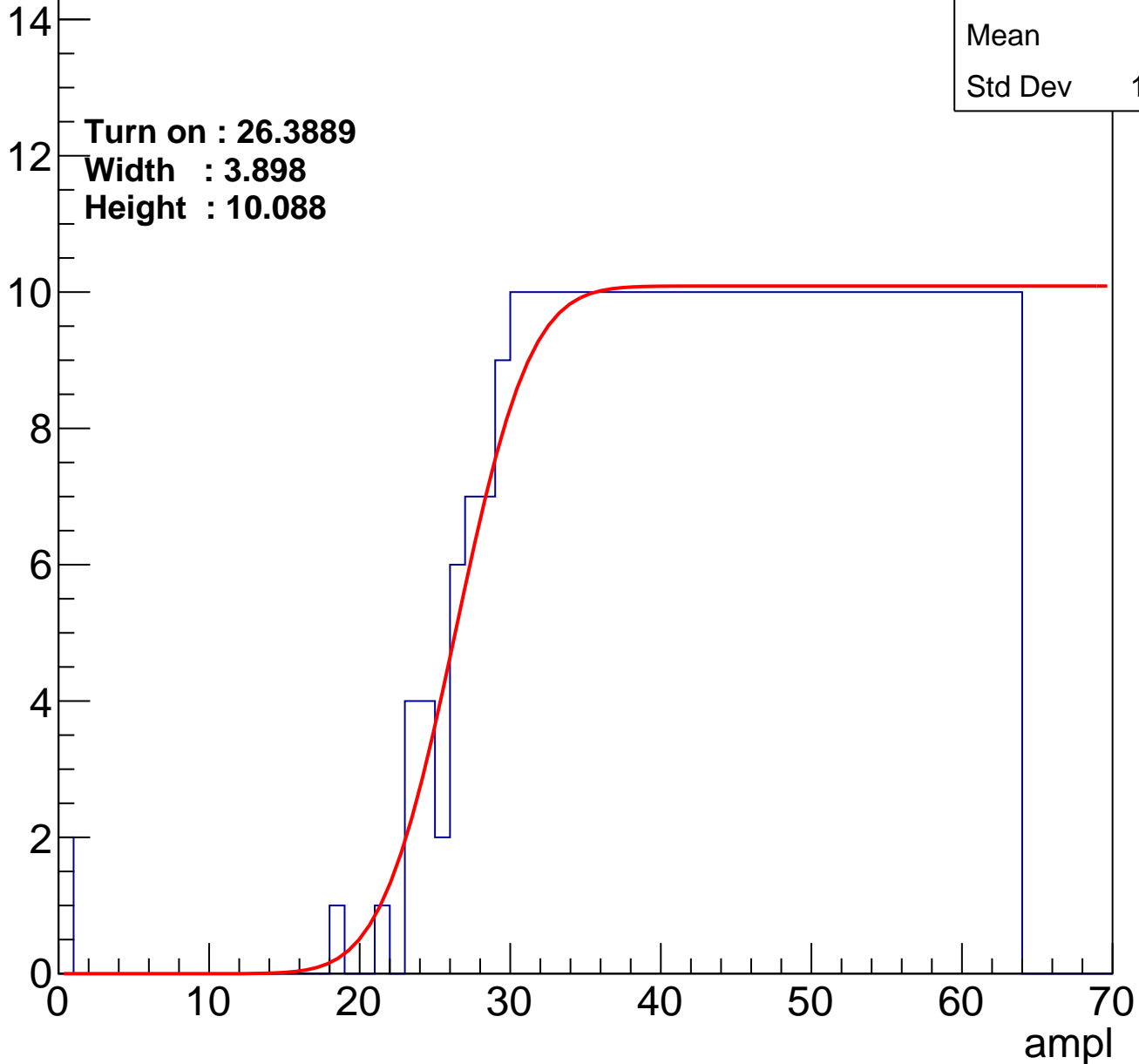
Entries	383
Mean	44.1
Std Dev	11.63

Turn on : 26.3889

Width : 3.898

Height : 10.088

Entry



B1L103S, U1-ch87

calib_packv5_042523_0143.root, FC#7, port C2

Entries	382
Mean	44.17
Std Dev	11.56

Turn on : 26.2122

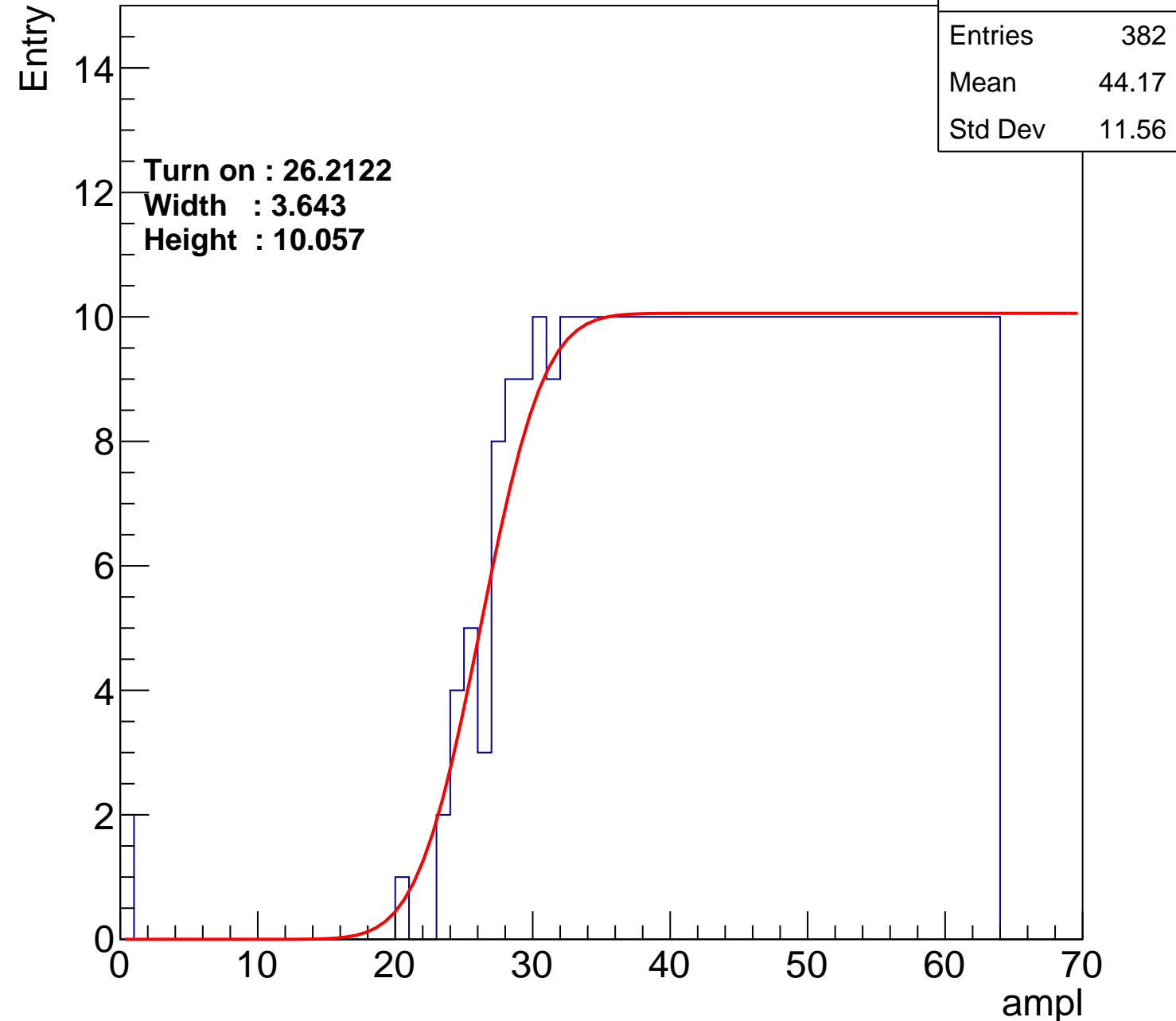
Width : 3.643

Height : 10.057

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch88

calib_packv5_042523_0143.root, FC#7, port C2

Entries	382
Mean	43.85
Std Dev	12.34

Turn on : 27.2511

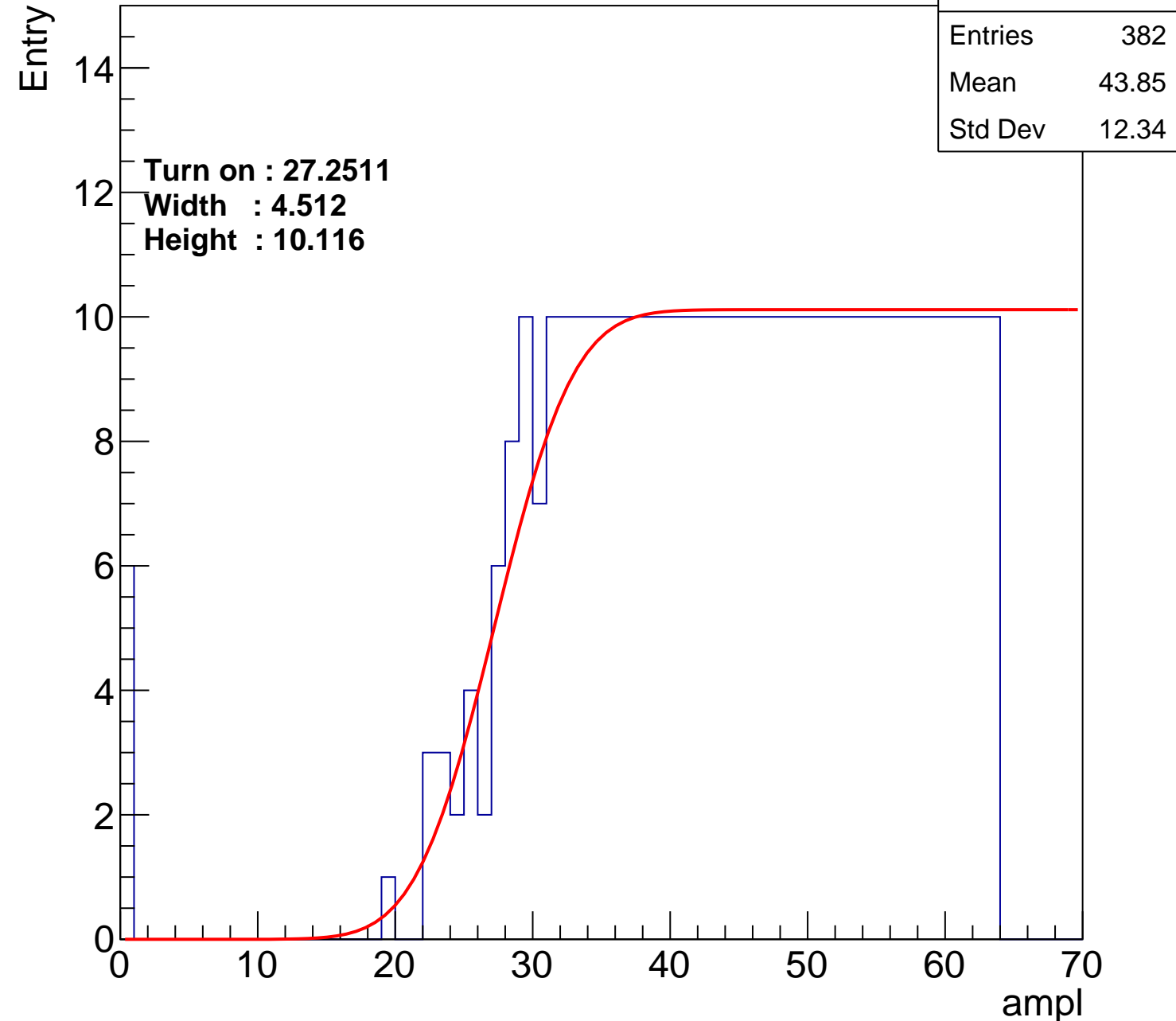
Width : 4.512

Height : 10.116

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch89

calib_packv5_042523_0143.root, FC#7, port C2

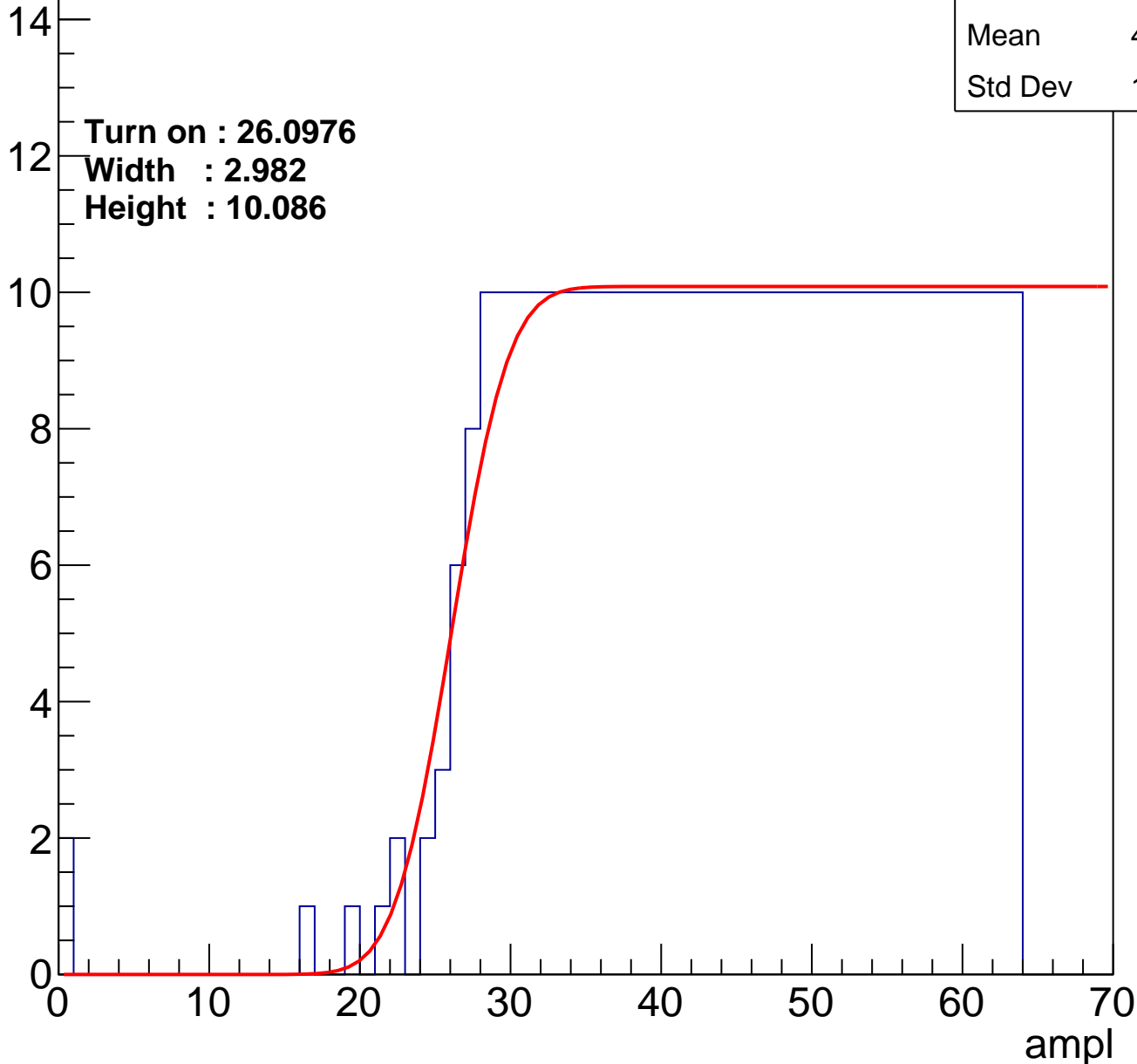
Entries	386
Mean	43.98
Std Dev	11.67

Turn on : 26.0976

Width : 2.982

Height : 10.086

Entry



B1L103S, U1-ch90

calib_packv5_042523_0143.root, FC#7, port C2

Entries	409
Mean	42.89
Std Dev	12.13

Turn on : 22.9657

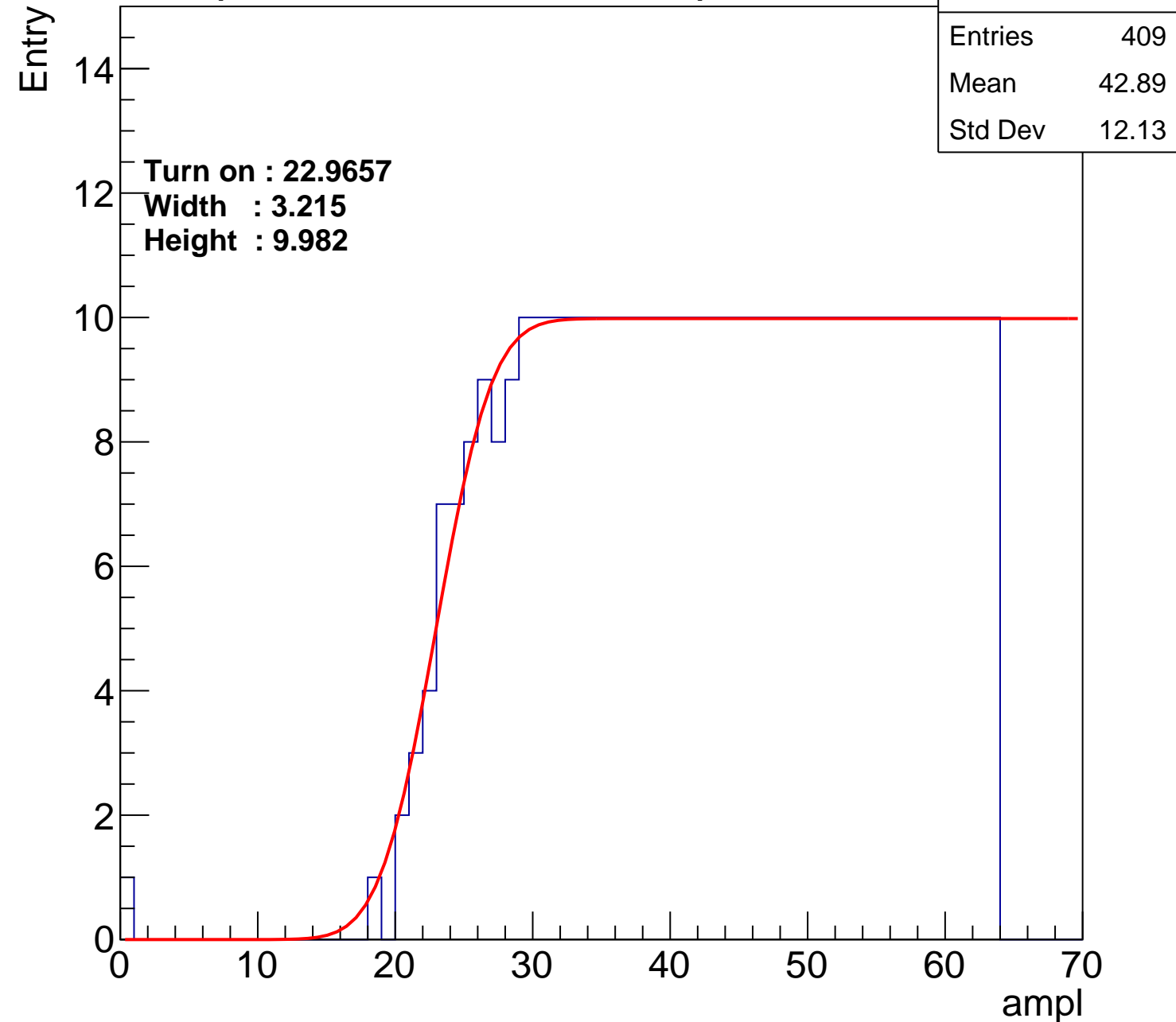
Width : 3.215

Height : 9.982

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch91

calib_packv5_042523_0143.root, FC#7, port C2

Entries	392
Mean	43.67
Std Dev	11.82

Turn on : 24.8263

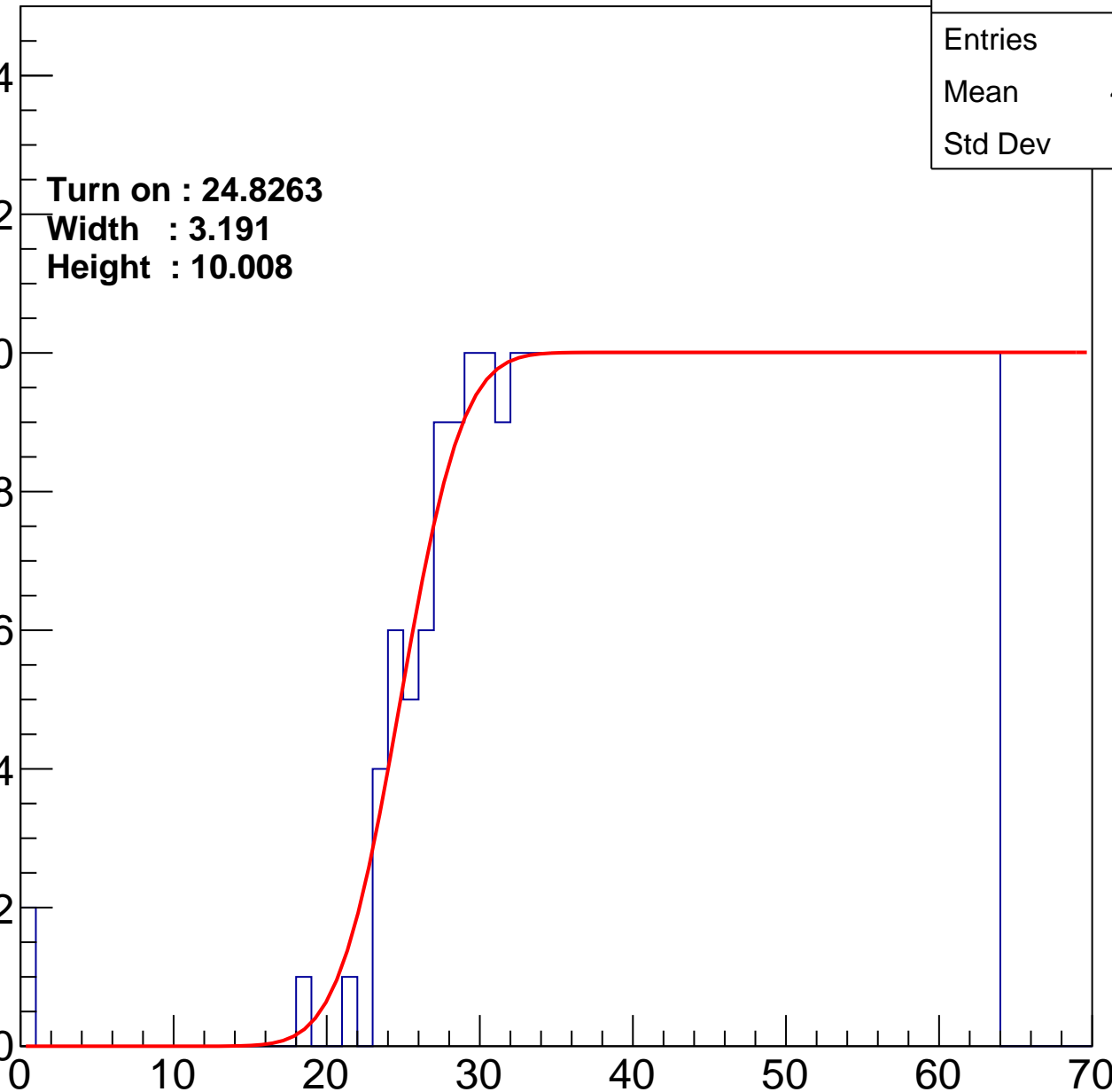
Width : 3.191

Height : 10.008

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch92

calib_packv5_042523_0143.root, FC#7, port C2

Entries	410
Mean	42.49
Std Dev	12.78

Turn on : 24.0522

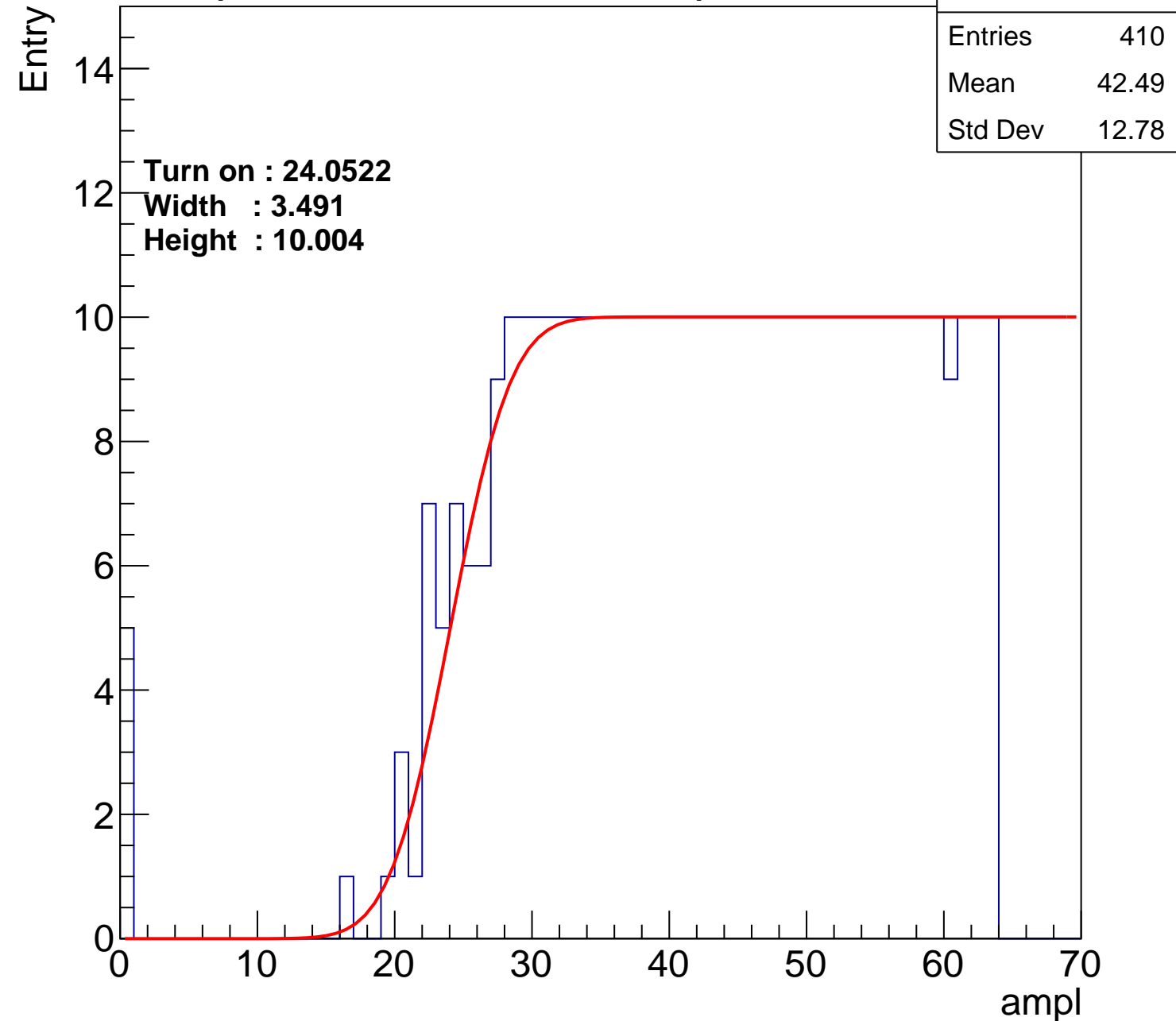
Width : 3.491

Height : 10.004

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch93

calib_packv5_042523_0143.root, FC#7, port C2

Entries	380
Mean	44.23
Std Dev	11.57

Turn on : 26.5482

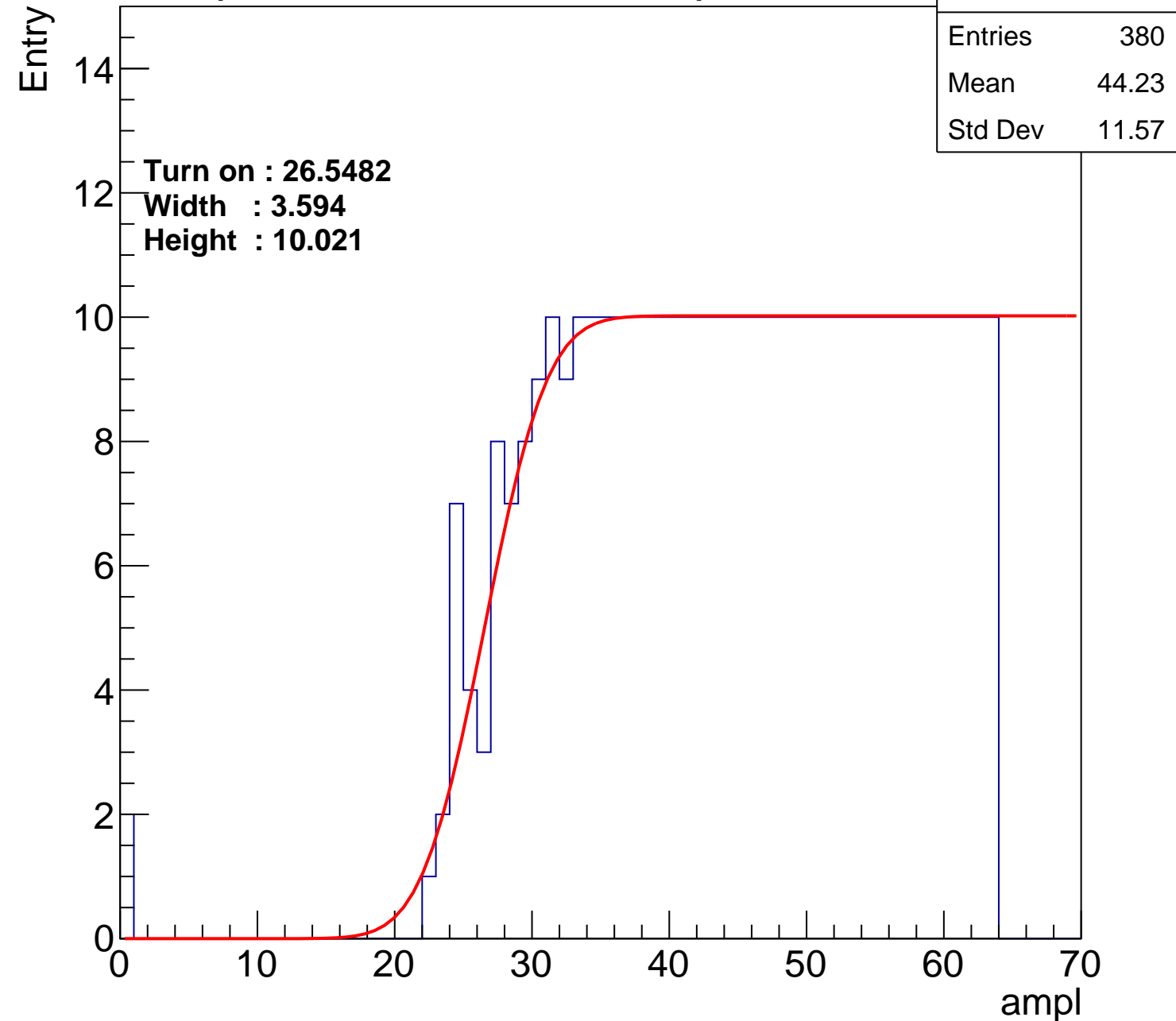
Width : 3.594

Height : 10.021

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch94

calib_packv5_042523_0143.root, FC#7, port C2

Entries	396
Mean	43.35
Std Dev	12.26

Turn on : 25.0821

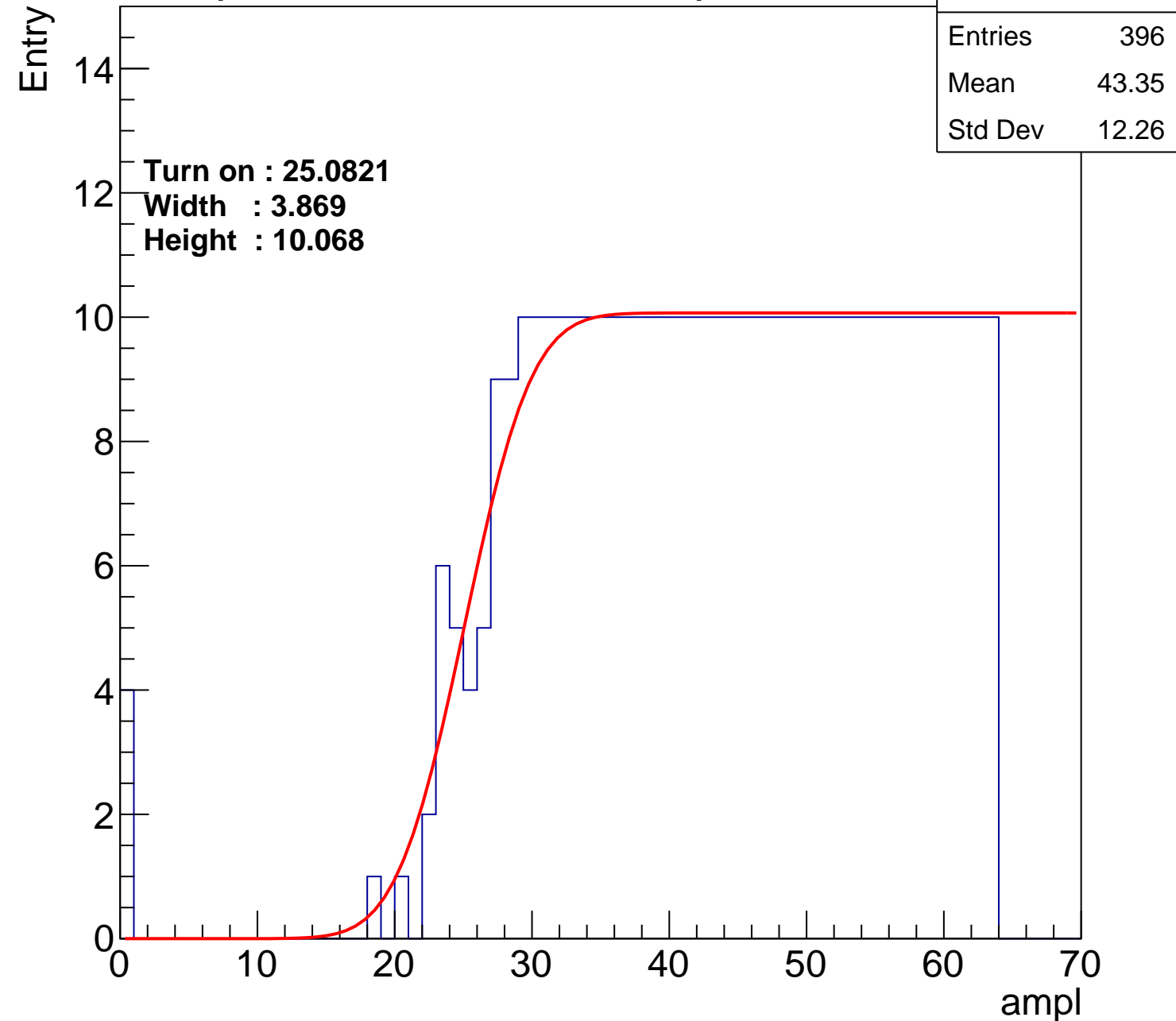
Width : 3.869

Height : 10.068

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch95

calib_packv5_042523_0143.root, FC#7, port C2

Entries	400
Mean	43.05
Std Dev	12.63

Turn on : 24.6780

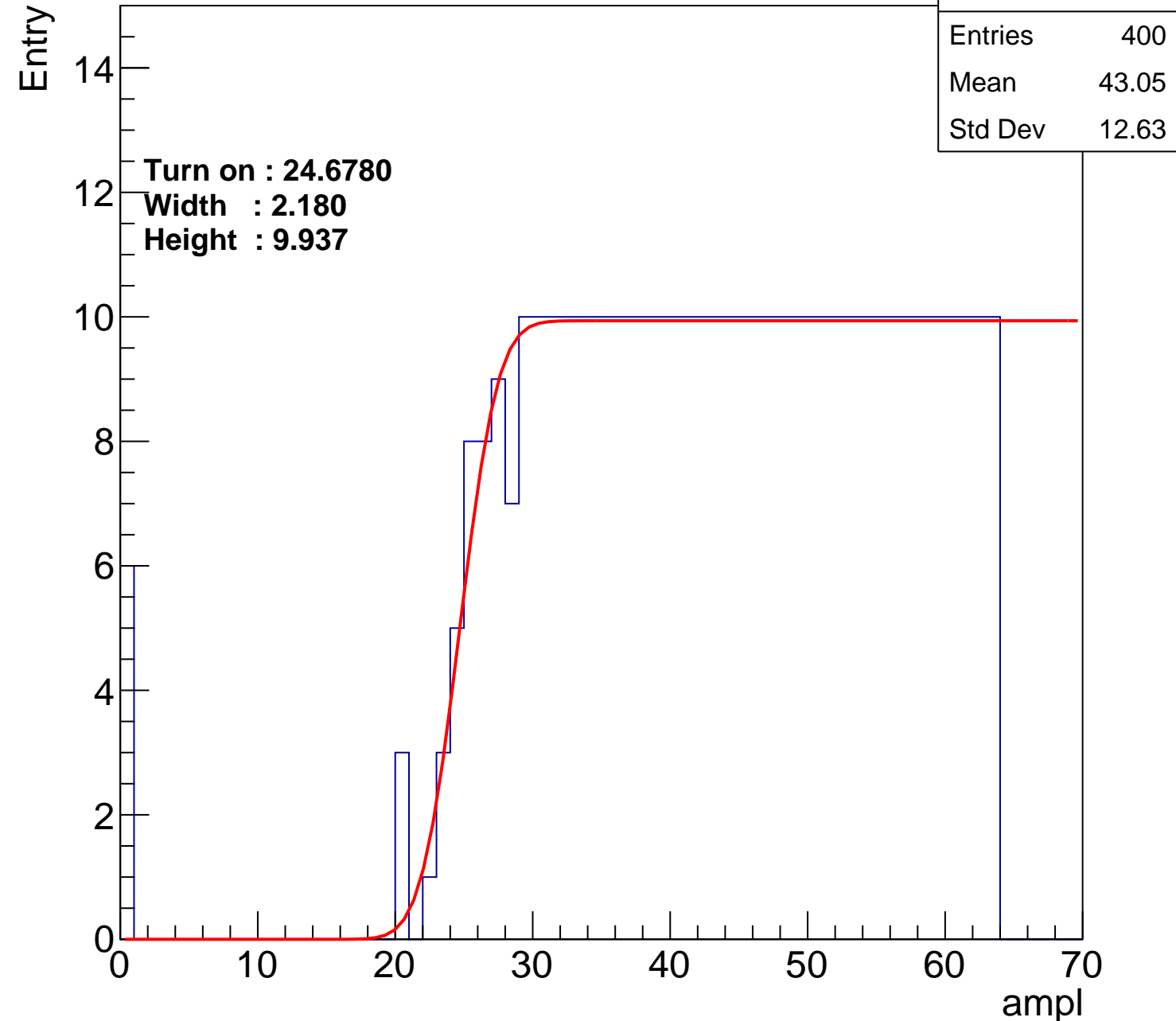
Width : 2.180

Height : 9.937

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch96

calib_packv5_042523_0143.root, FC#7, port C2

Entries	379
Mean	44.02
Std Dev	12.16

Turn on : 26.9176

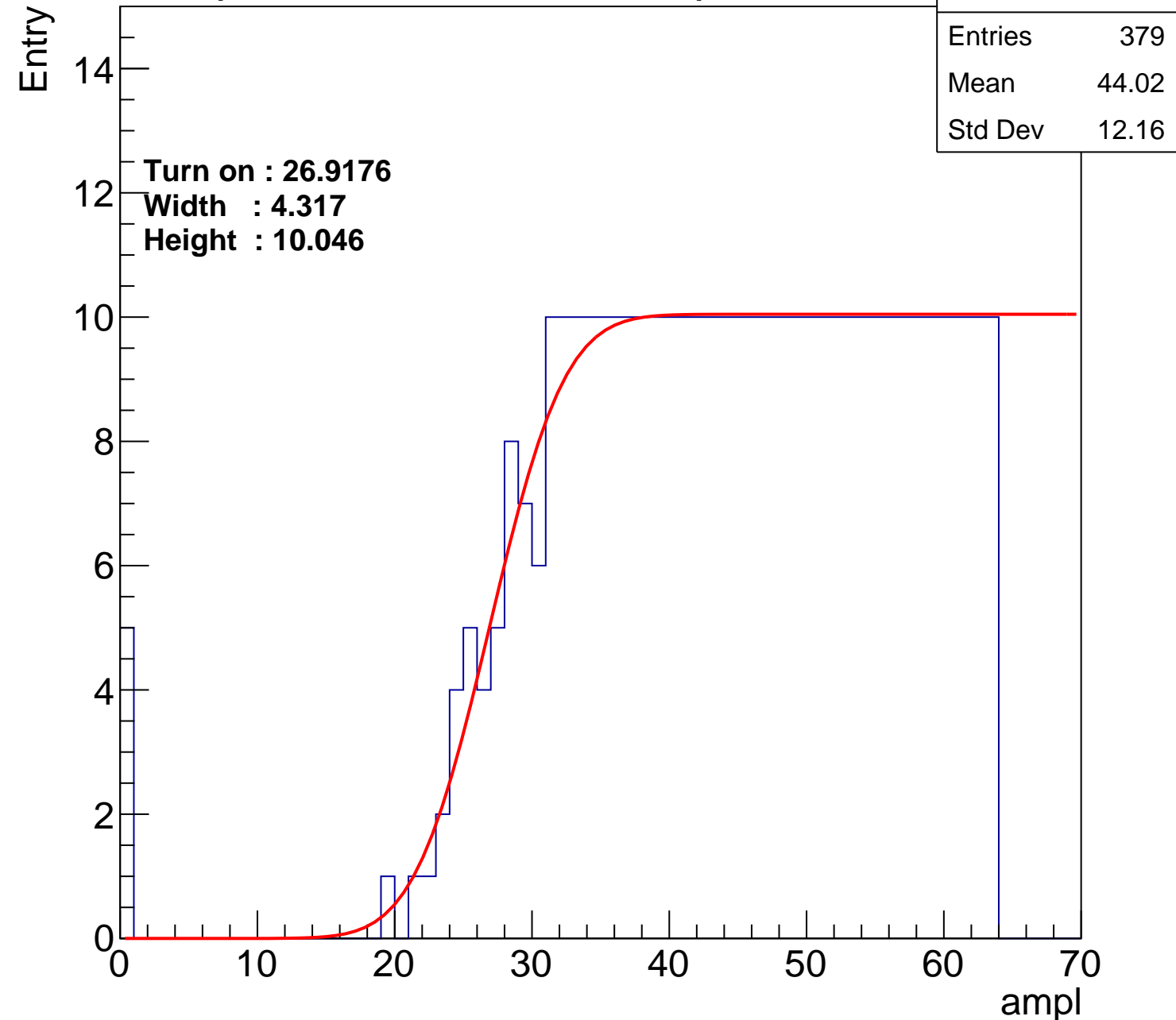
Width : 4.317

Height : 10.046

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch97

calib_packv5_042523_0143.root, FC#7, port C2

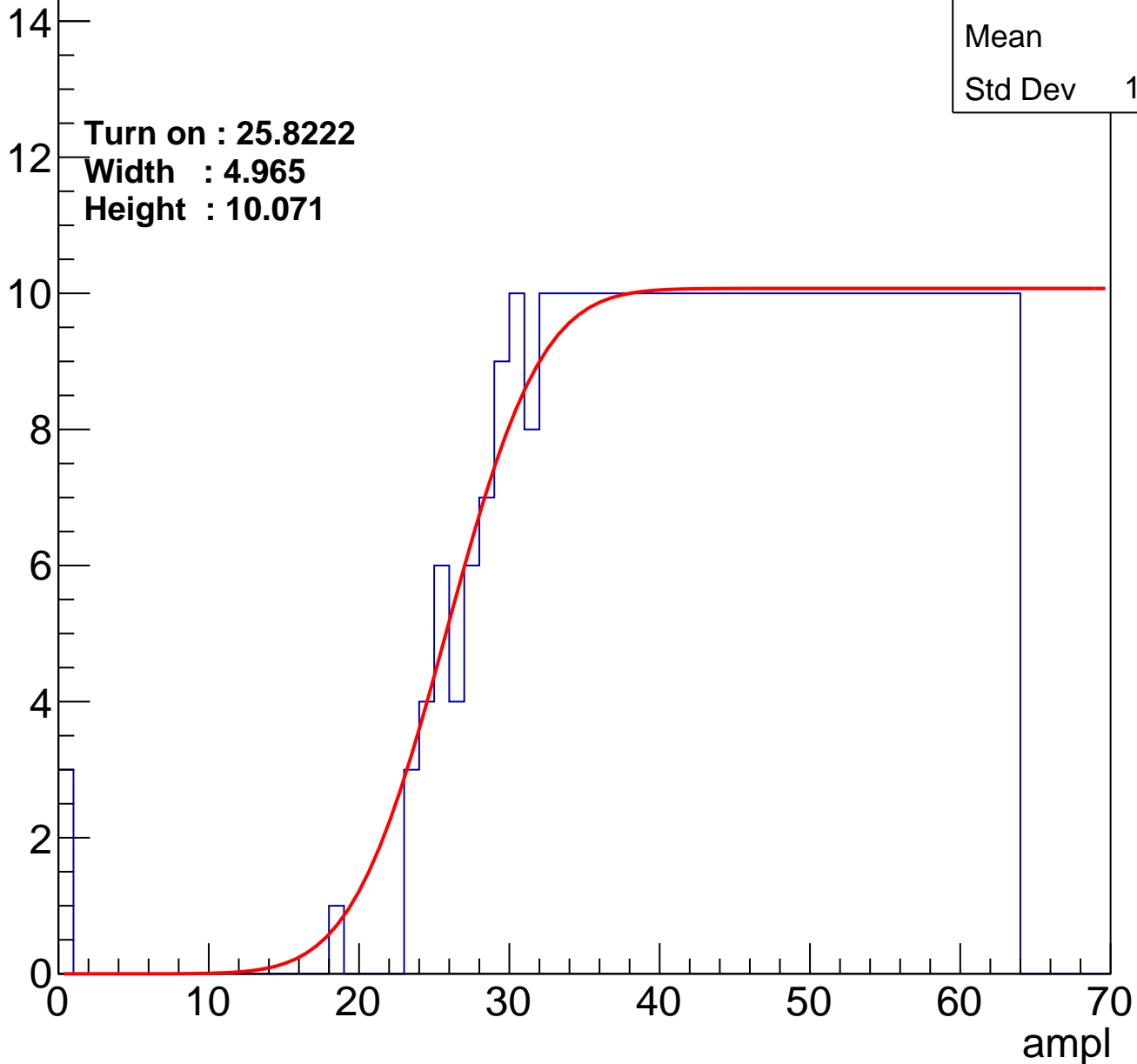
Entries	381
Mean	44.1
Std Dev	11.79

Turn on : 25.8222

Width : 4.965

Height : 10.071

Entry



B1L103S, U1-ch98

calib_packv5_042523_0143.root, FC#7, port C2

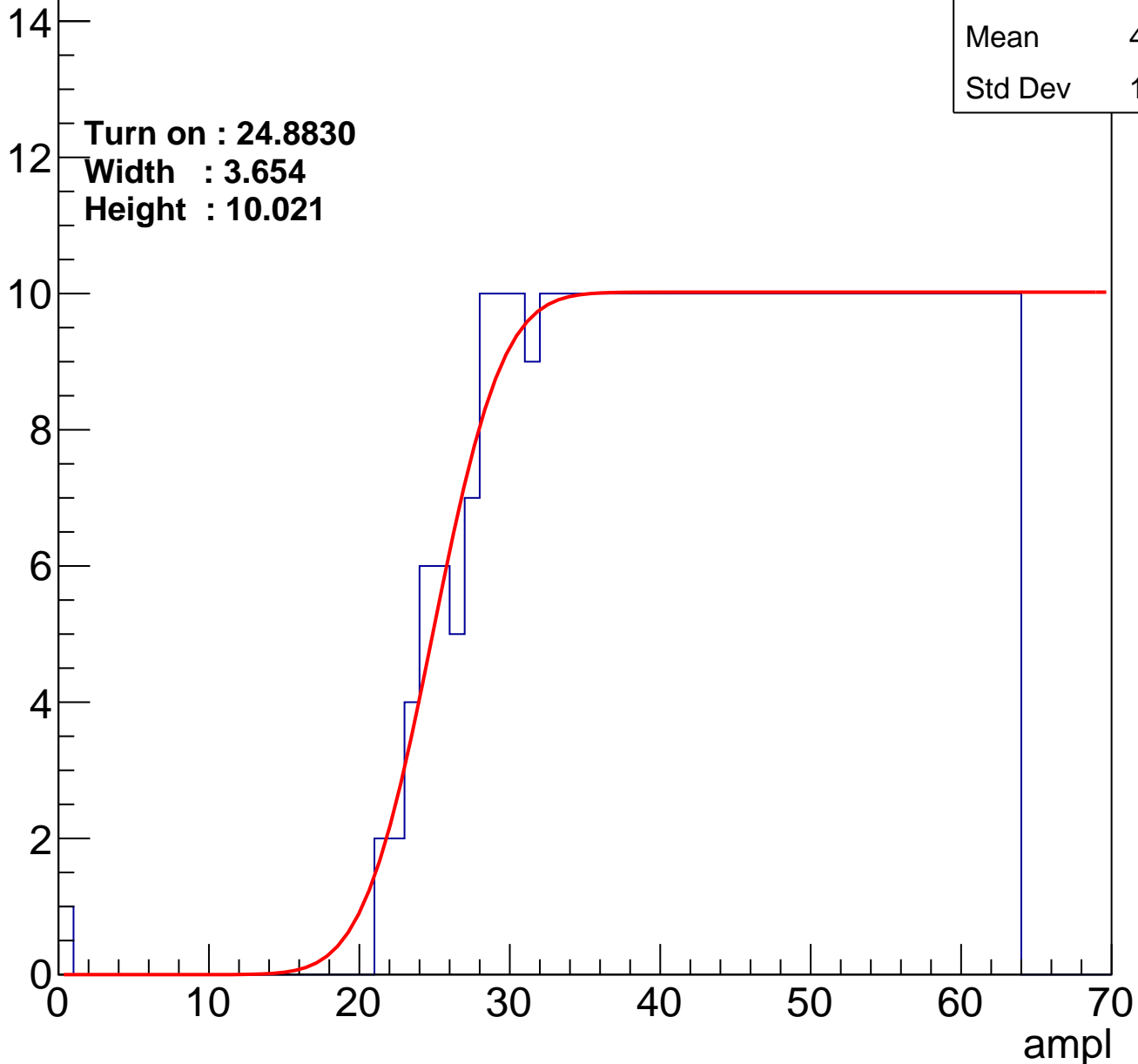
Entries	392
Mean	43.72
Std Dev	11.67

Turn on : 24.8830

Width : 3.654

Height : 10.021

Entry



B1L103S, U1-ch99

calib_packv5_042523_0143.root, FC#7, port C2

Entries	356
Mean	45.51
Std Dev	10.69

Turn on : 29.1463

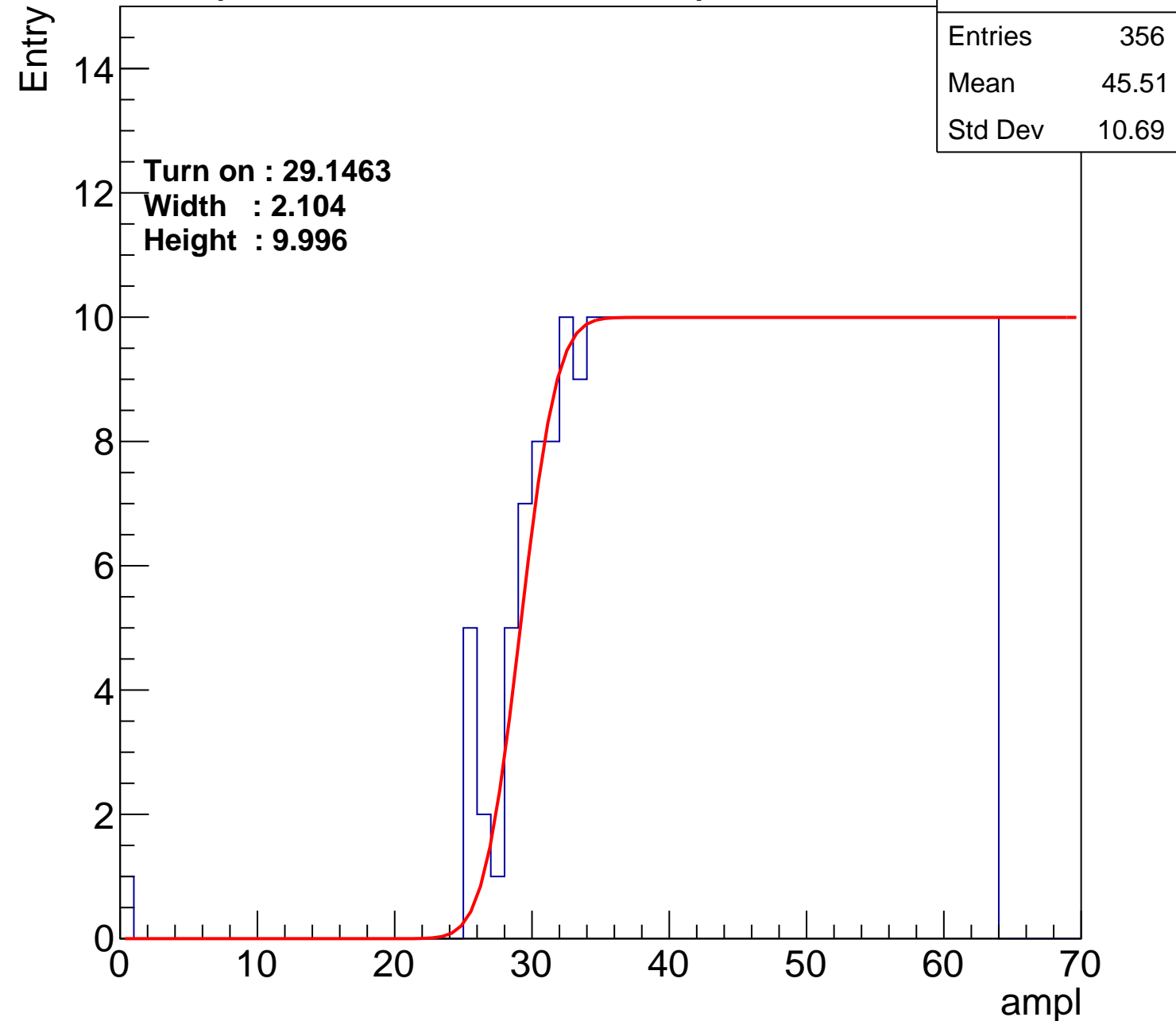
Width : 2.104

Height : 9.996

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch100

calib_packv5_042523_0143.root, FC#7, port C2

Entries	389
Mean	43.66
Std Dev	12.13

Turn on : 24.9525

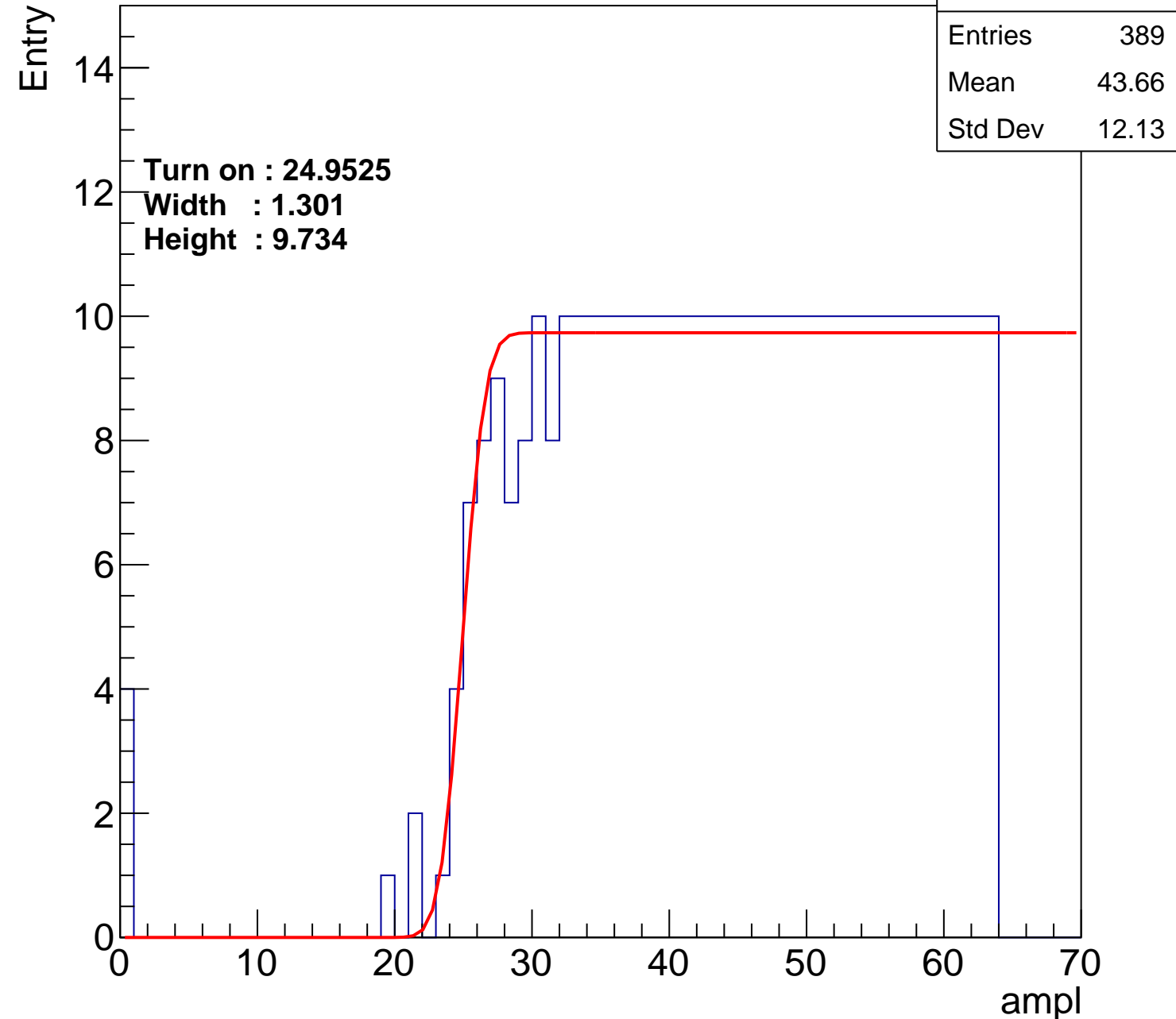
Width : 1.301

Height : 9.734

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch101

calib_packv5_042523_0143.root, FC#7, port C2

Entries	378
Mean	44.19
Std Dev	11.88

Turn on : 26.9092

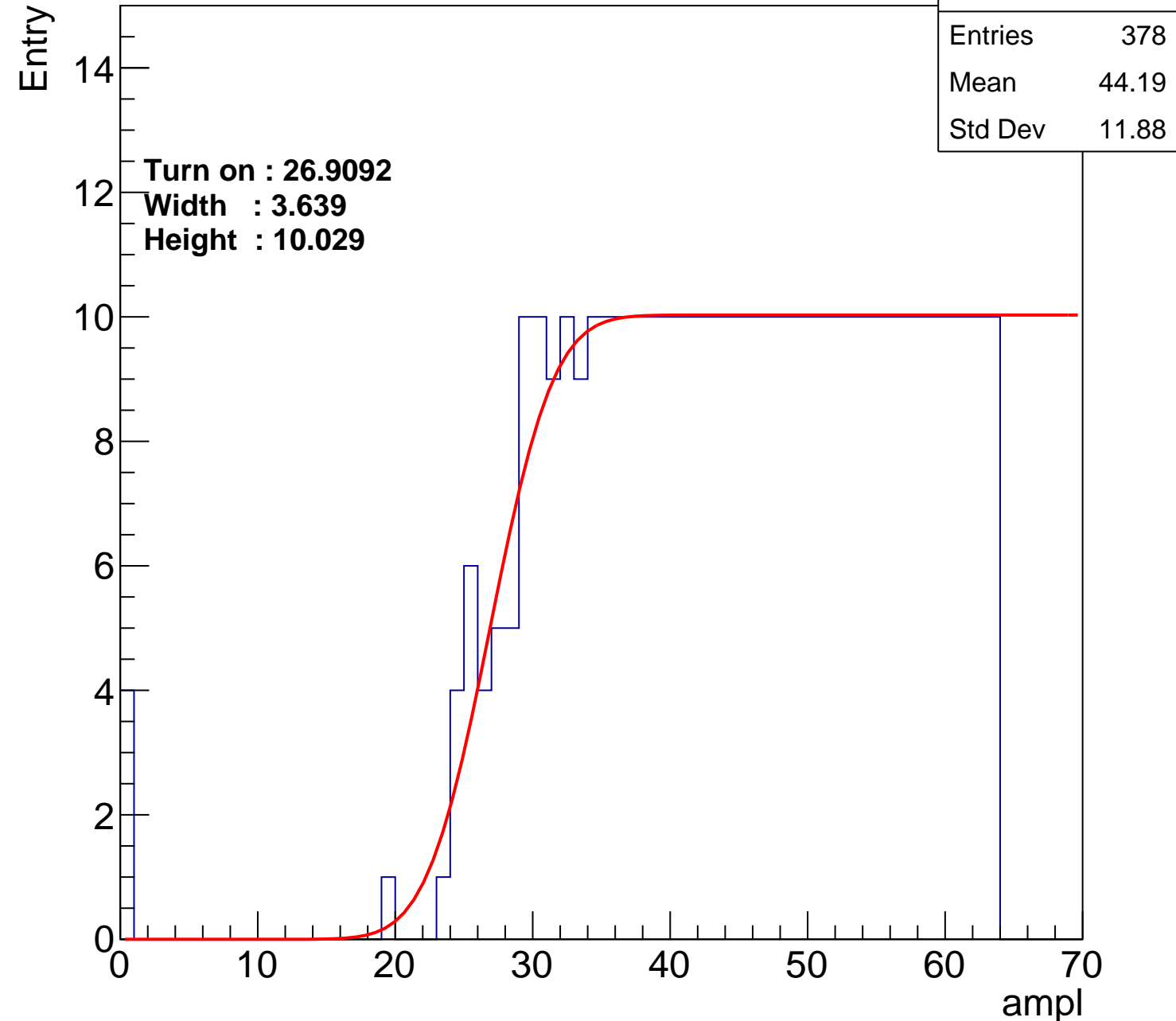
Width : 3.639

Height : 10.029

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch102

calib_packv5_042523_0143.root, FC#7, port C2

Entries	401
Mean	42.97
Std Dev	12.68

Turn on : 25.3346

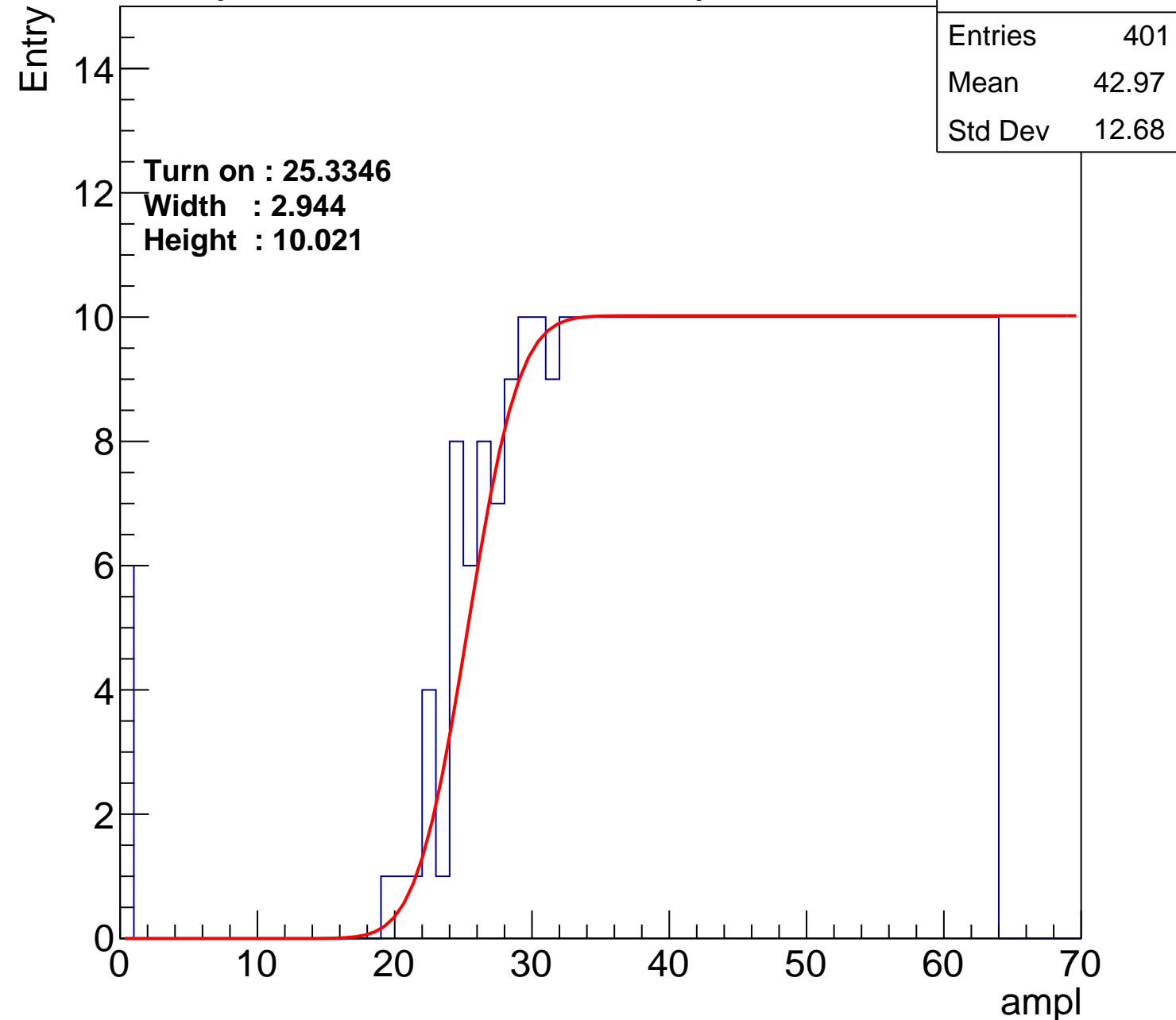
Width : 2.944

Height : 10.021

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch103

calib_packv5_042523_0143.root, FC#7, port C2

Entries	376
Mean	44.39
Std Dev	11.59

Turn on : 26.8425

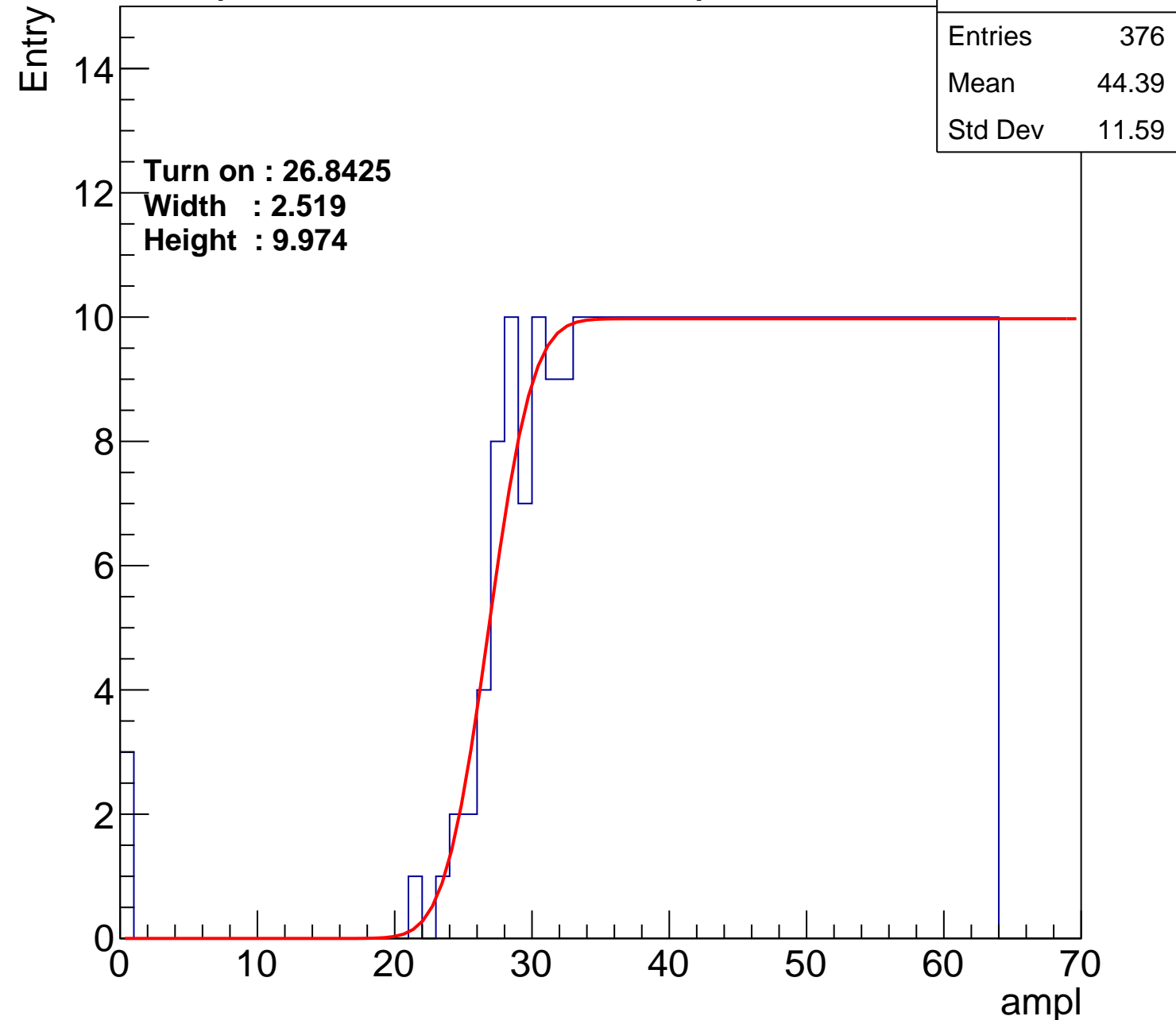
Width : 2.519

Height : 9.974

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch104

calib_packv5_042523_0143.root, FC#7, port C2

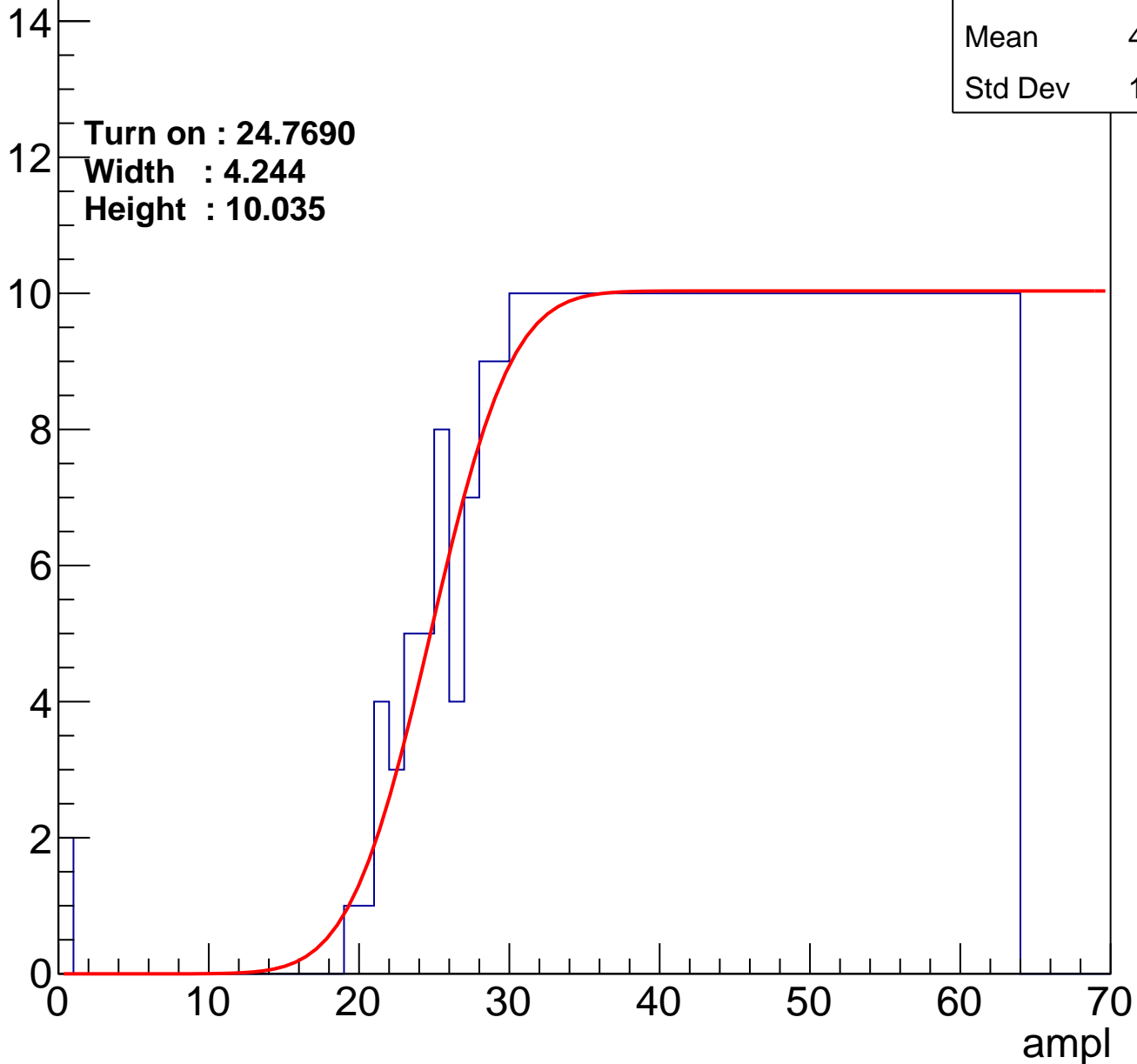
Entries	398
Mean	43.32
Std Dev	12.08

Turn on : 24.7690

Width : 4.244

Height : 10.035

Entry



B1L103S, U1-ch105

calib_packv5_042523_0143.root, FC#7, port C2

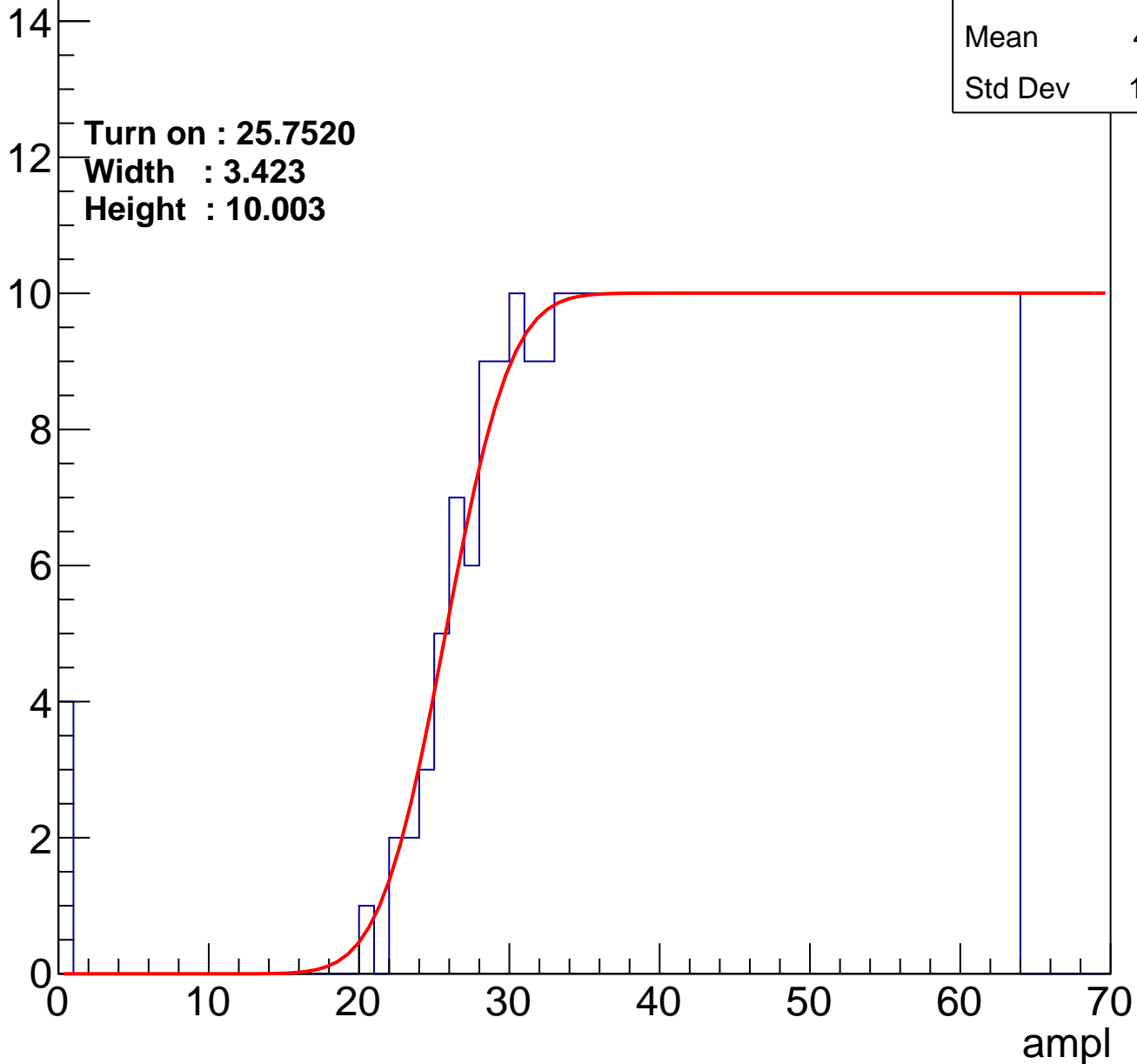
Entries	386
Mean	43.81
Std Dev	12.05

Turn on : 25.7520

Width : 3.423

Height : 10.003

Entry



B1L103S, U1-ch106

calib_packv5_042523_0143.root, FC#7, port C2

Entries	394
Mean	43.55
Std Dev	11.9

Turn on : 25.3438

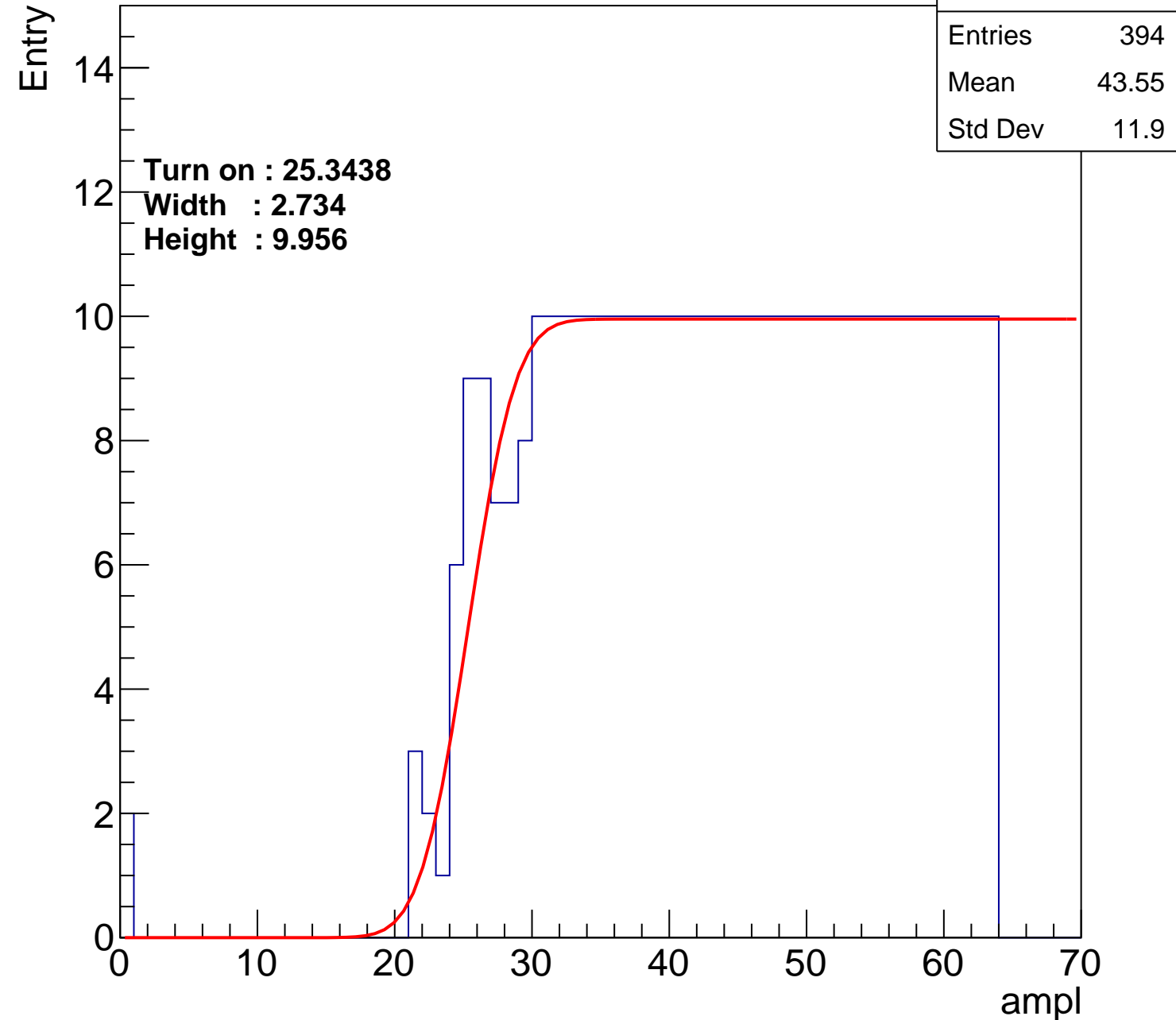
Width : 2.734

Height : 9.956

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch107

calib_packv5_042523_0143.root, FC#7, port C2

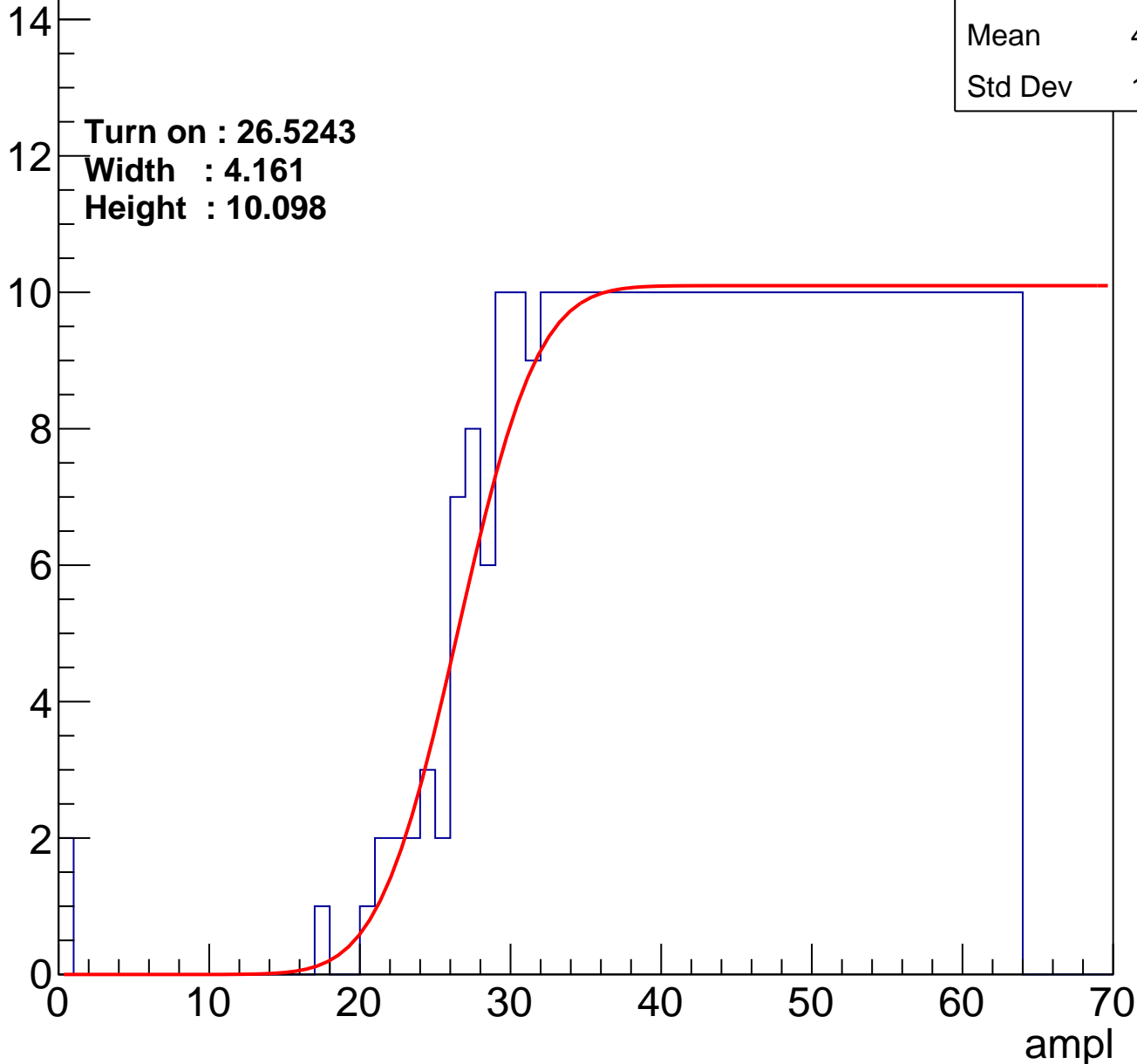
Entries	385
Mean	43.96
Std Dev	11.74

Turn on : 26.5243

Width : 4.161

Height : 10.098

Entry



B1L103S, U1-ch108

calib_packv5_042523_0143.root, FC#7, port C2

Entries	376
Mean	44.31
Std Dev	11.81

Turn on : 26.7218

Width : 3.147

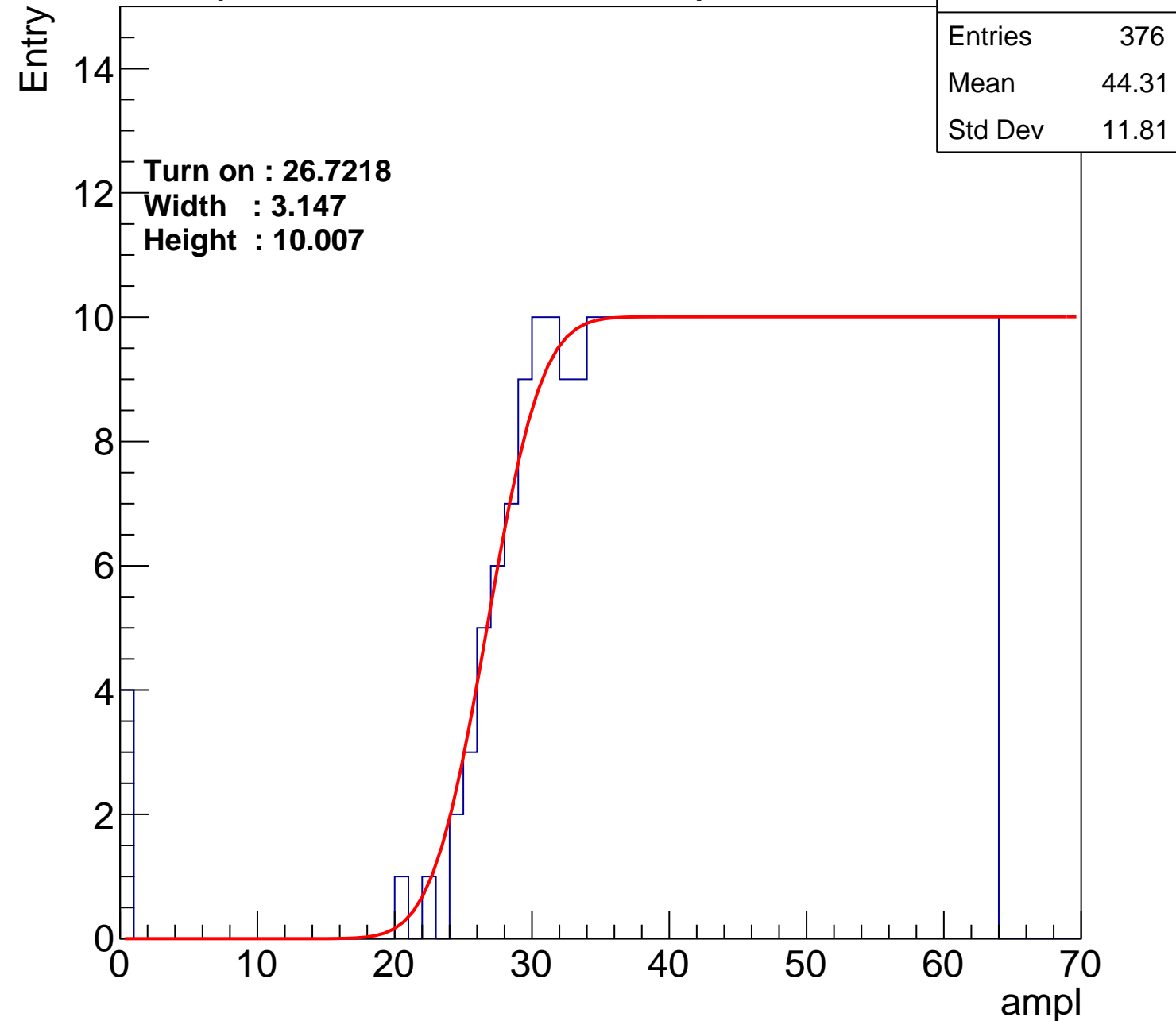
Height : 10.007

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L103S, U1-ch109

calib_packv5_042523_0143.root, FC#7, port C2

Entries	393
Mean	43.58
Std Dev	11.92

Turn on : 24.8819

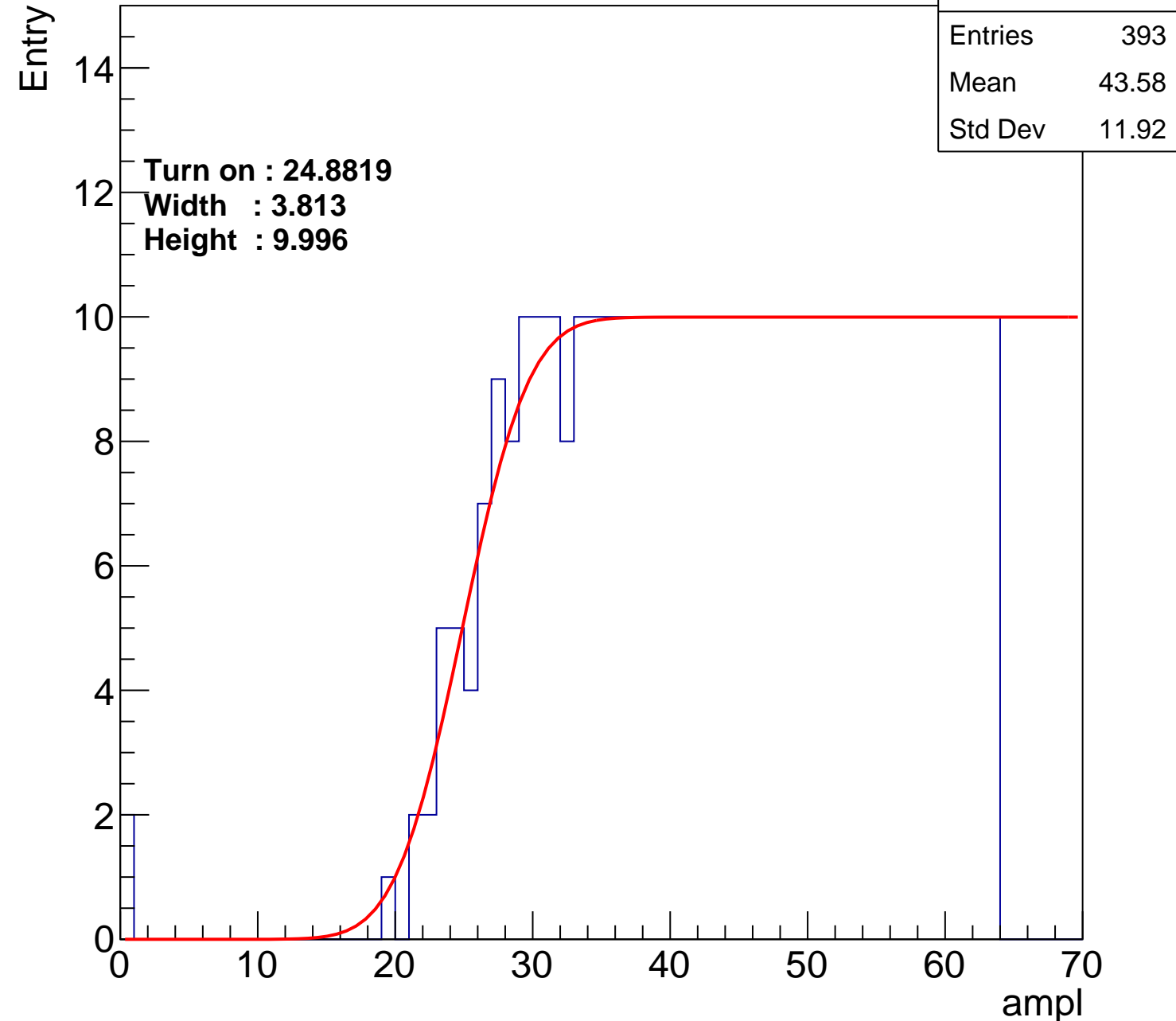
Width : 3.813

Height : 9.996

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch110

calib_packv5_042523_0143.root, FC#7, port C2

Entries	389
Mean	43.51
Std Dev	12.48

Turn on : 25.9484

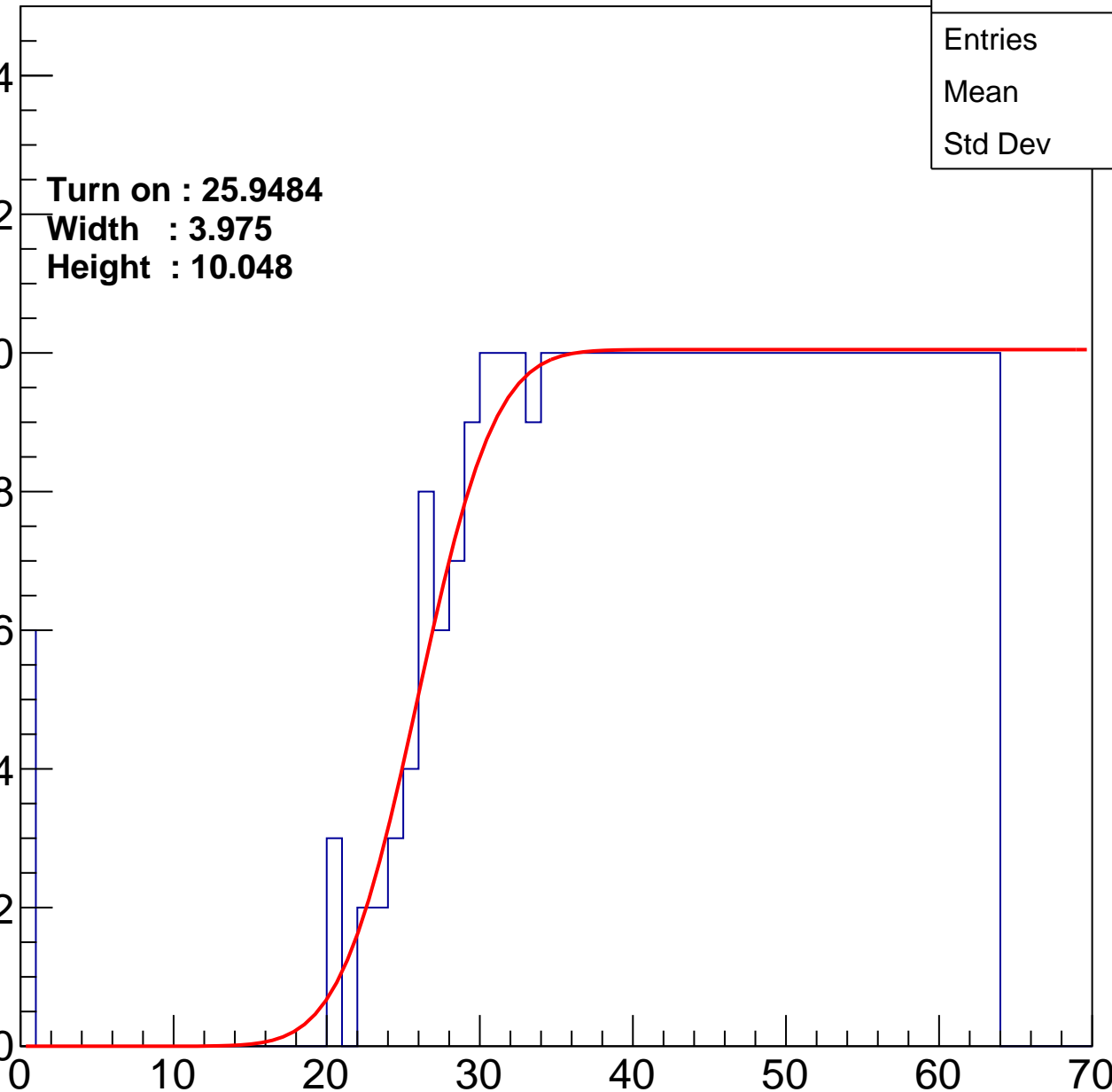
Width : 3.975

Height : 10.048

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch111

calib_packv5_042523_0143.root, FC#7, port C2

Entries	391
Mean	43.68
Std Dev	11.87

Turn on : 25.1574

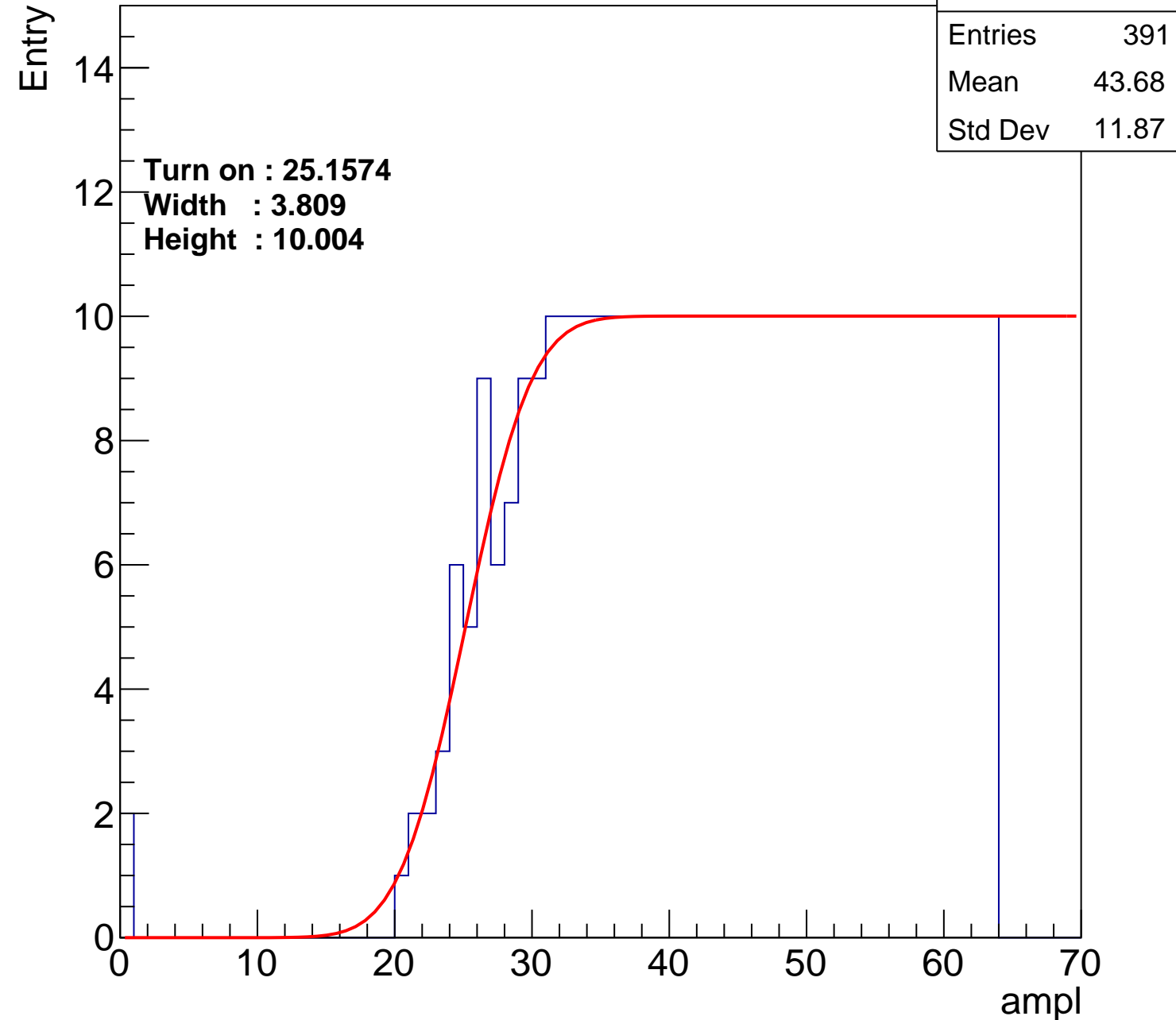
Width : 3.809

Height : 10.004

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch112

calib_packv5_042523_0143.root, FC#7, port C2

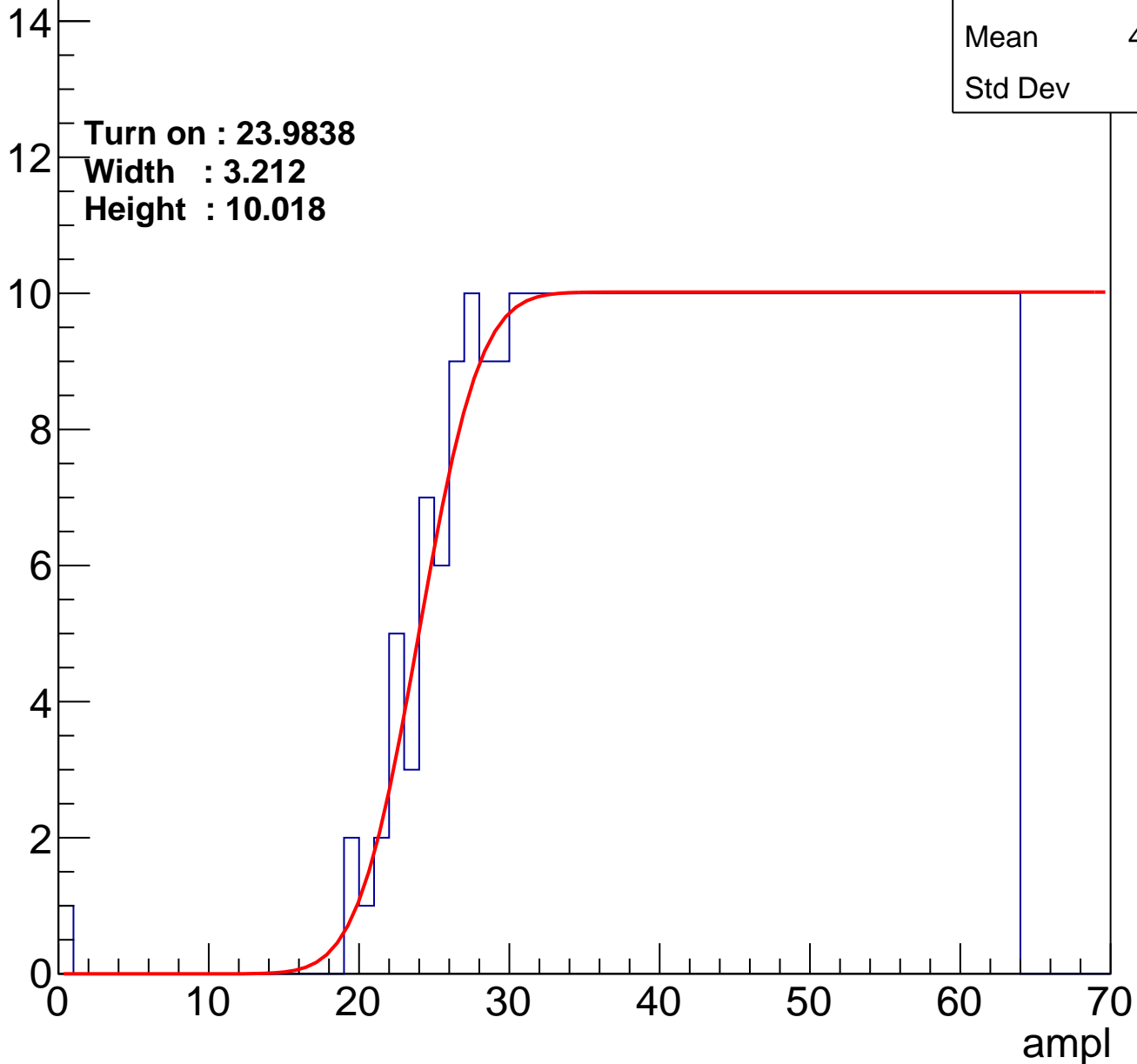
Entries	404
Mean	43.13
Std Dev	12

Turn on : 23.9838

Width : 3.212

Height : 10.018

Entry



B1L103S, U1-ch113

calib_packv5_042523_0143.root, FC#7, port C2

Entries	399
Mean	43.19
Std Dev	12.34

Turn on : 25.4286

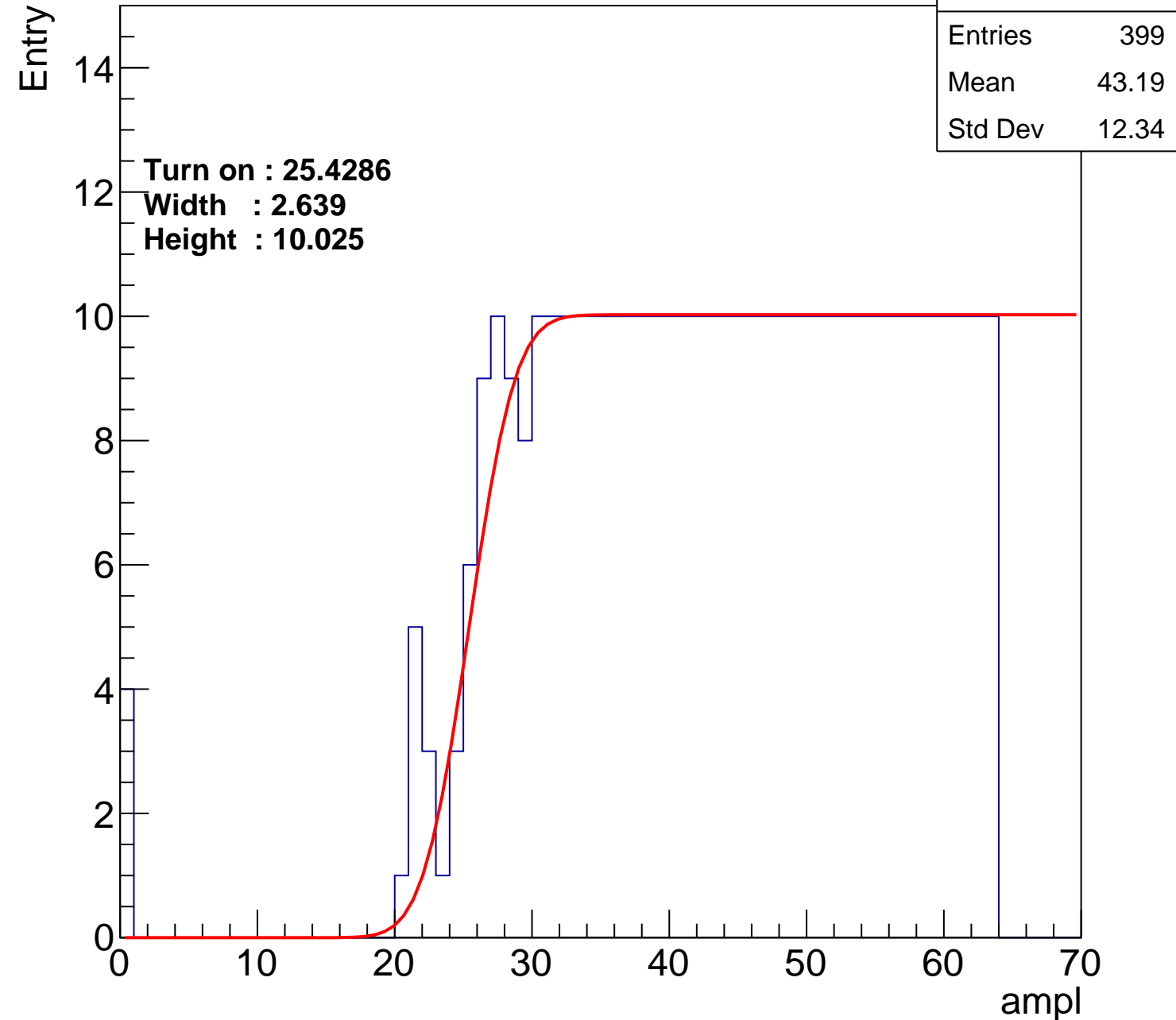
Width : 2.639

Height : 10.025

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch114

calib_packv5_042523_0143.root, FC#7, port C2

Entries	395
Mean	43.42
Std Dev	12.12

Turn on : 24.8666

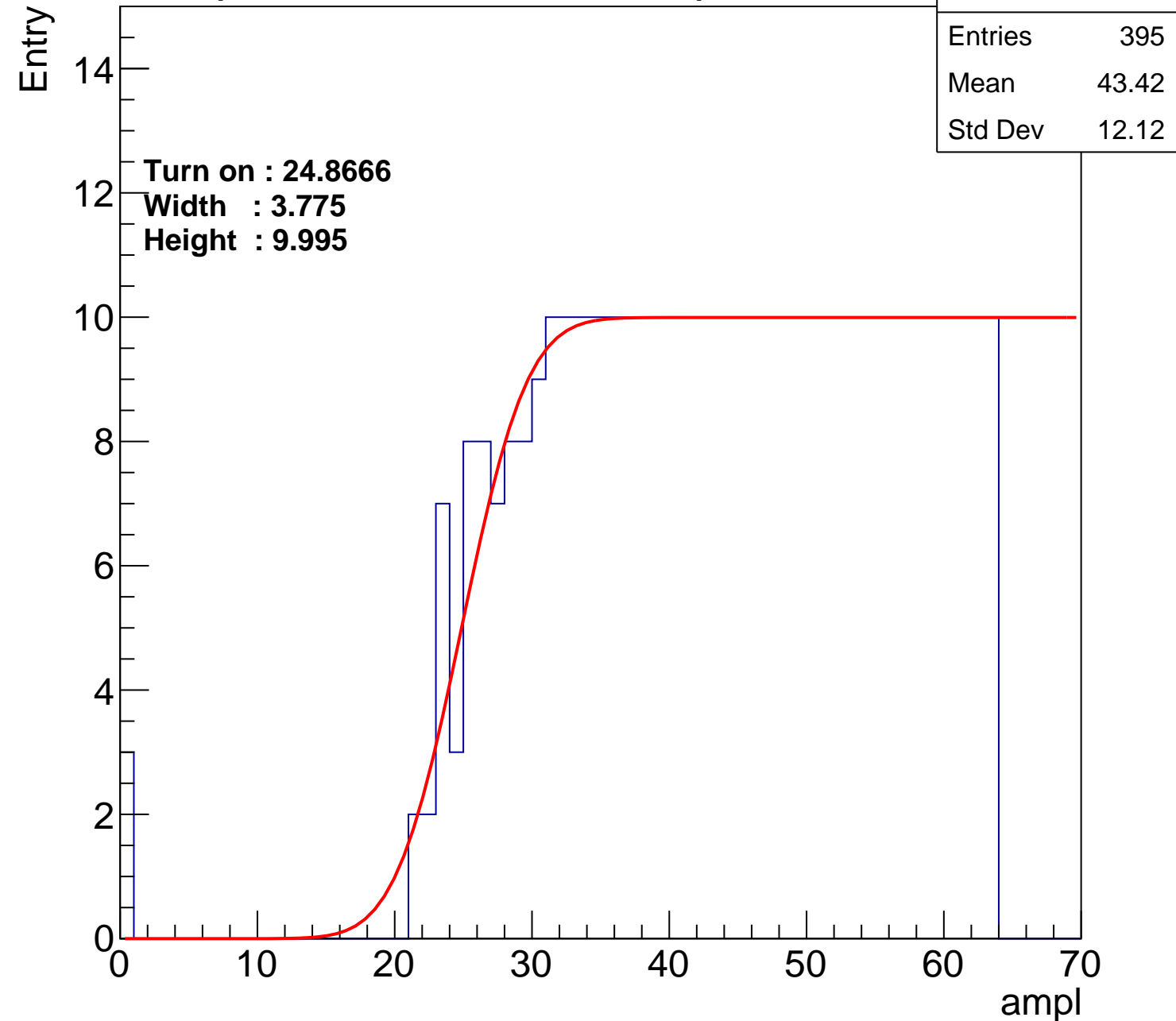
Width : 3.775

Height : 9.995

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch115

calib_packv5_042523_0143.root, FC#7, port C2

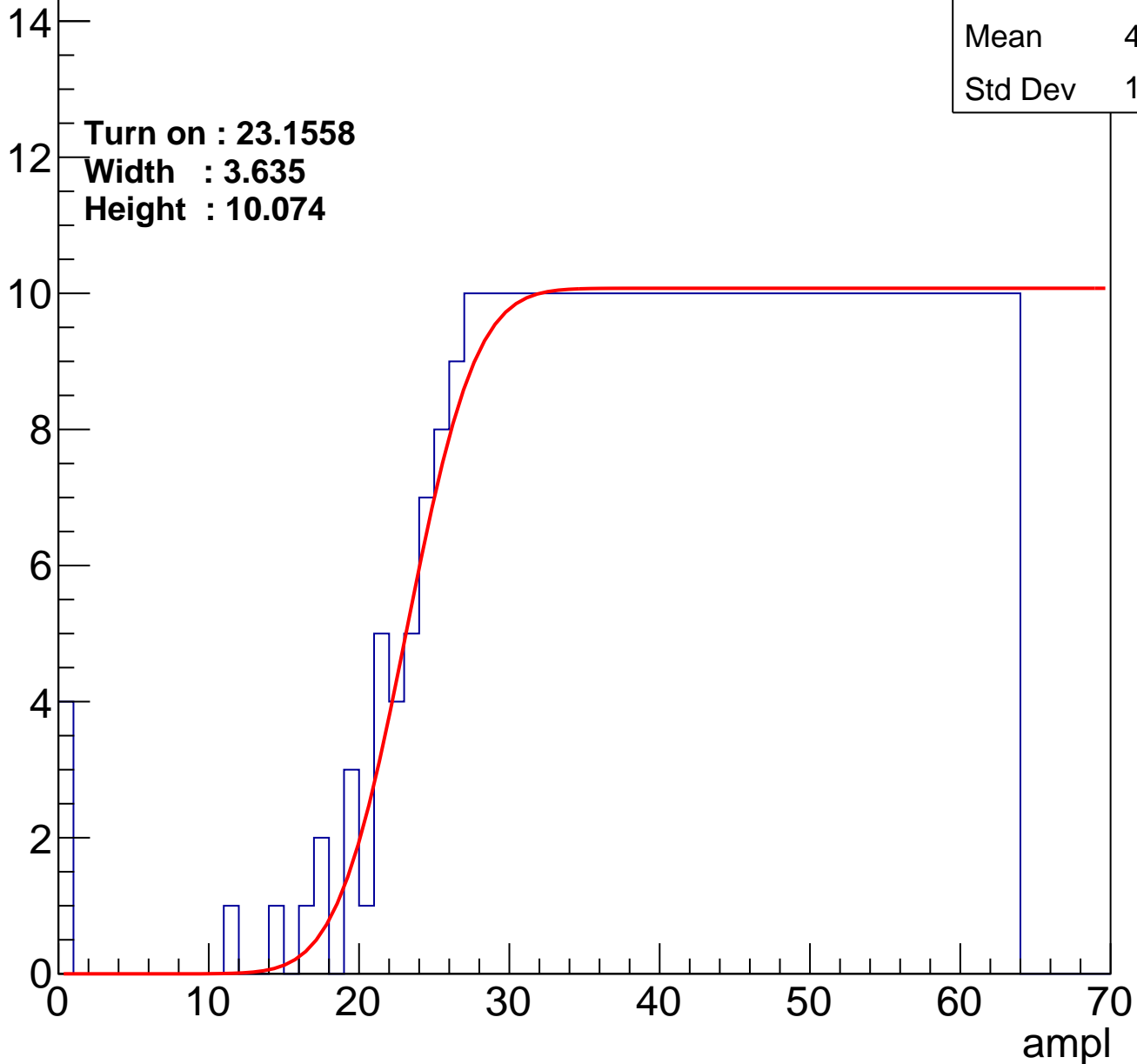
Entries	421
Mean	42.07
Std Dev	12.97

Turn on : 23.1558

Width : 3.635

Height : 10.074

Entry



B1L103S, U1-ch116

calib_packv5_042523_0143.root, FC#7, port C2

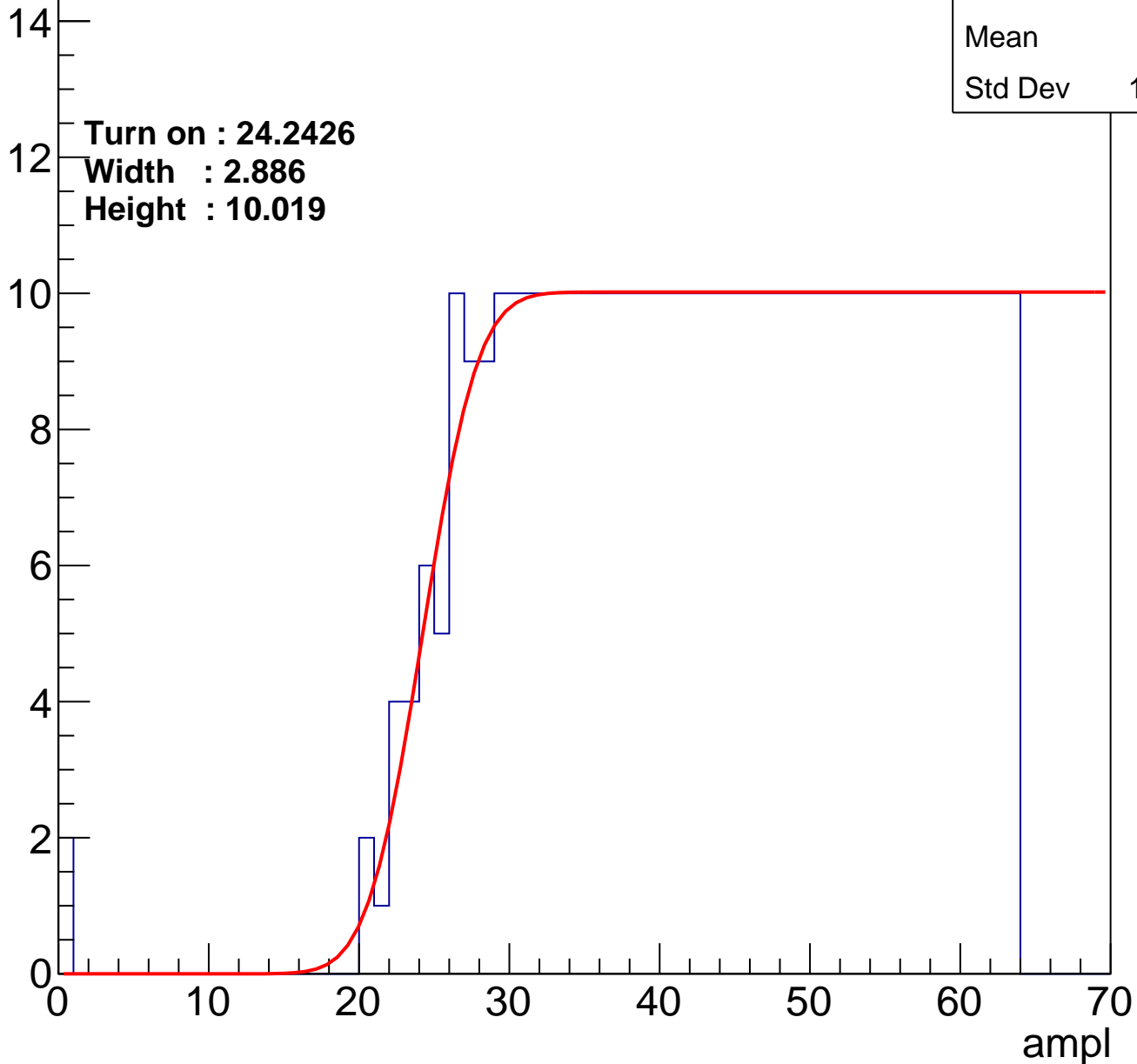
Entries	402
Mean	43.2
Std Dev	12.06

Turn on : 24.2426

Width : 2.886

Height : 10.019

Entry



B1L103S, U1-ch117

calib_packv5_042523_0143.root, FC#7, port C2

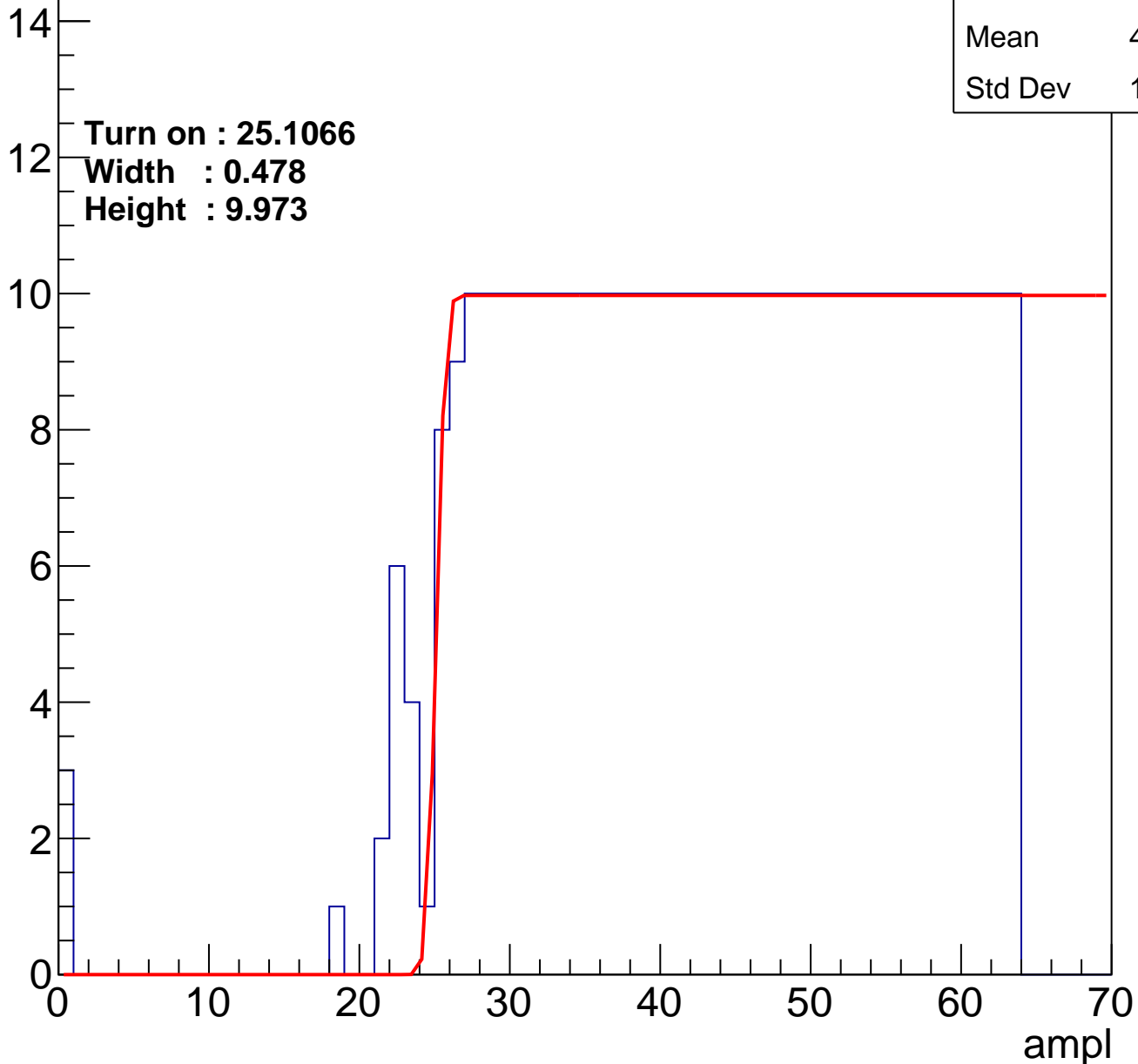
Entries	404
Mean	43.05
Std Dev	12.25

Turn on : 25.1066

Width : 0.478

Height : 9.973

Entry



B1L103S, U1-ch118

calib_packv5_042523_0143.root, FC#7, port C2

Entries	382
Mean	44.19
Std Dev	11.53

Turn on : 26.2178

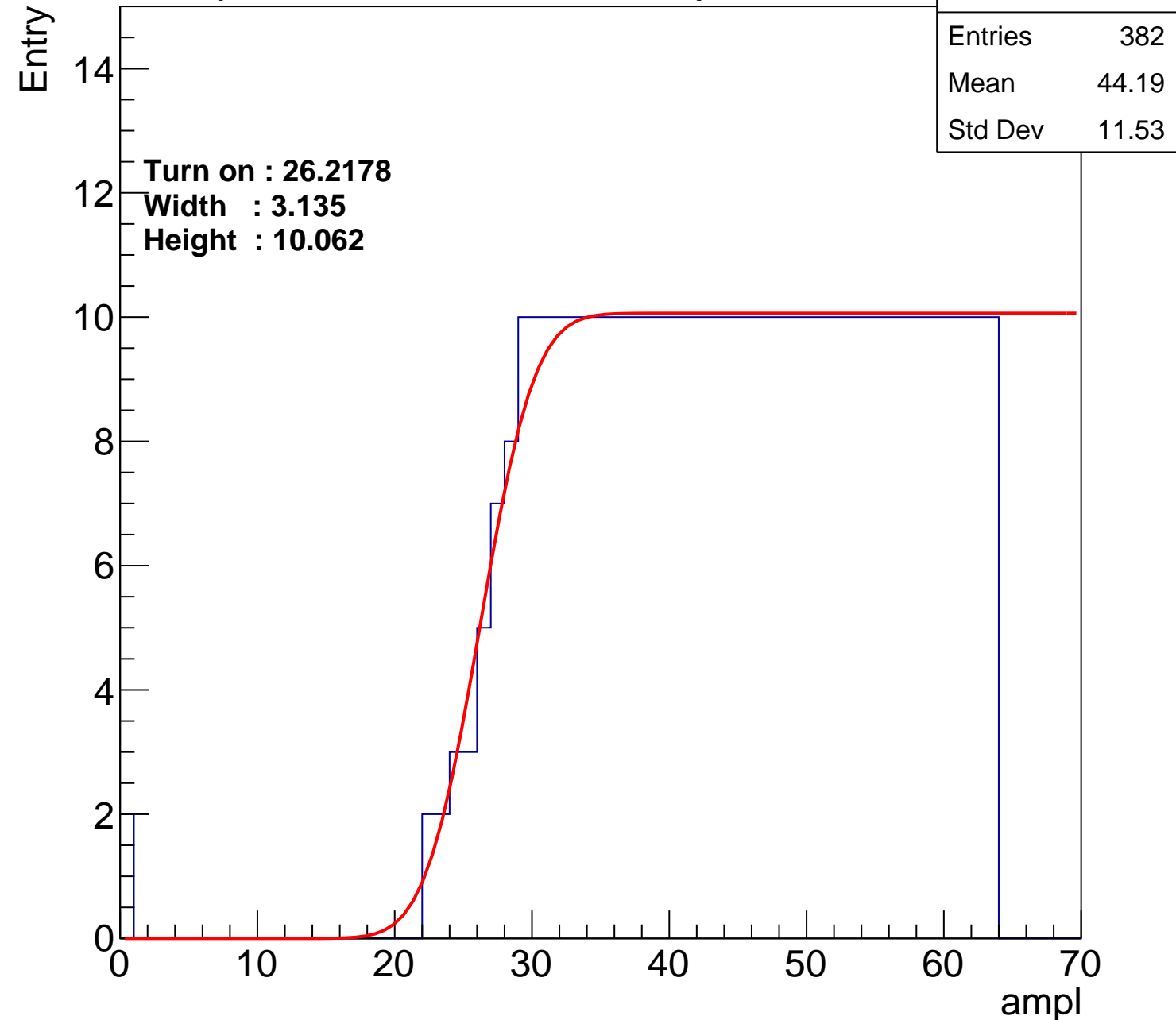
Width : 3.135

Height : 10.062

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch119

calib_packv5_042523_0143.root, FC#7, port C2

Entries	379
Mean	44.3
Std Dev	11.51

Turn on : 26.1213

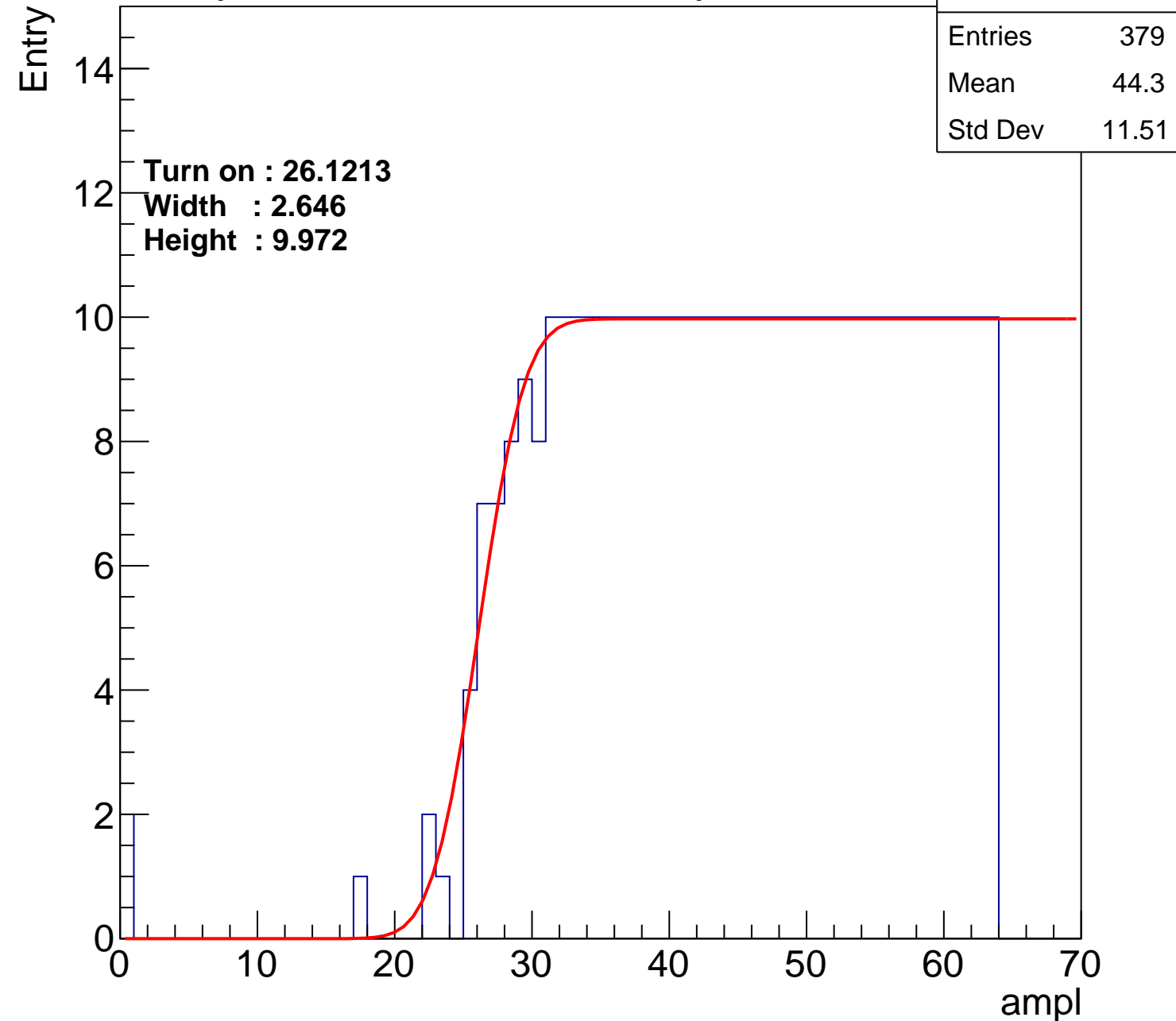
Width : 2.646

Height : 9.972

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch120

calib_packv5_042523_0143.root, FC#7, port C2

Entries	403
Mean	42.97
Std Dev	12.48

Turn on : 23.6681

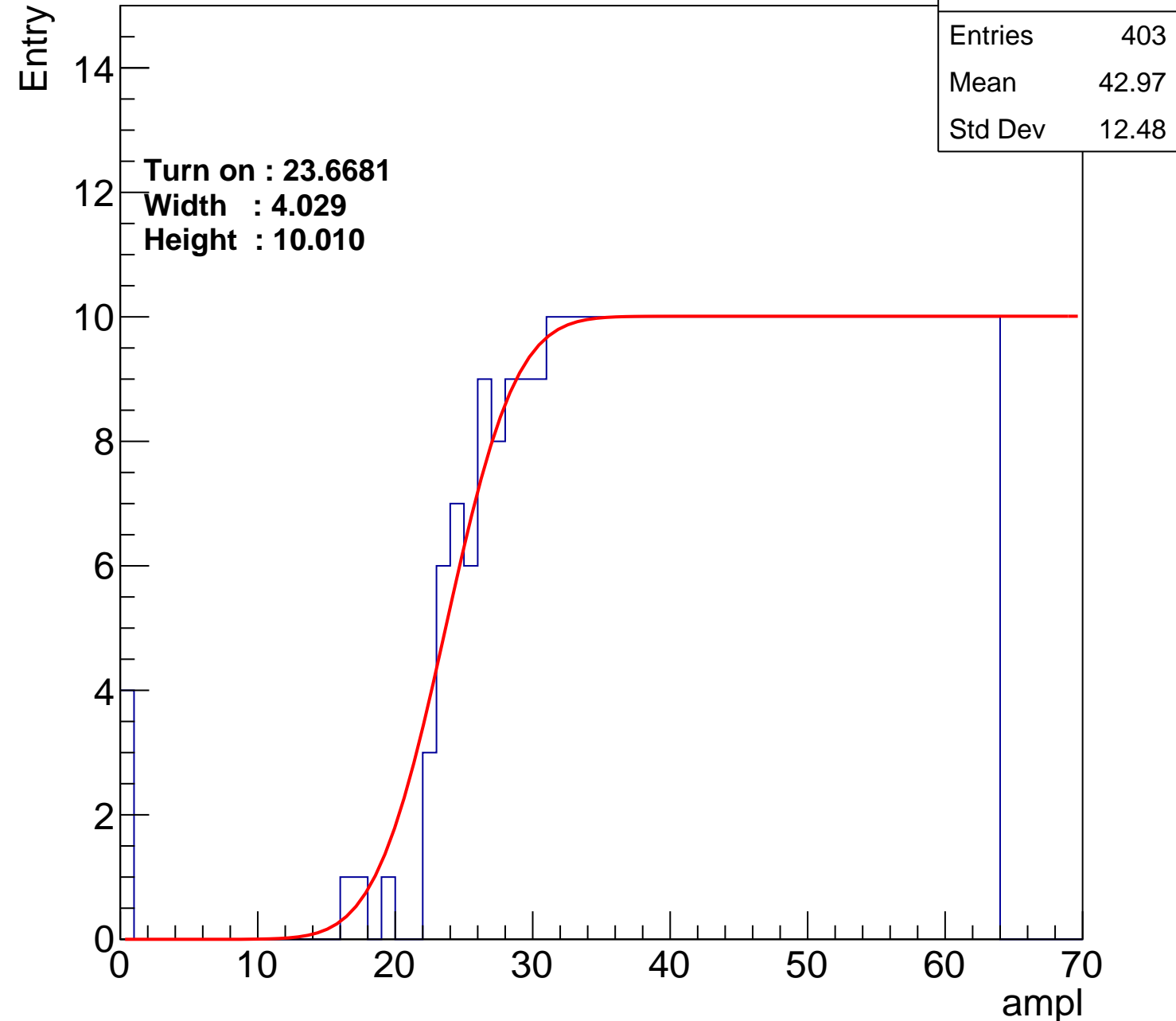
Width : 4.029

Height : 10.010

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch121

calib_packv5_042523_0143.root, FC#7, port C2

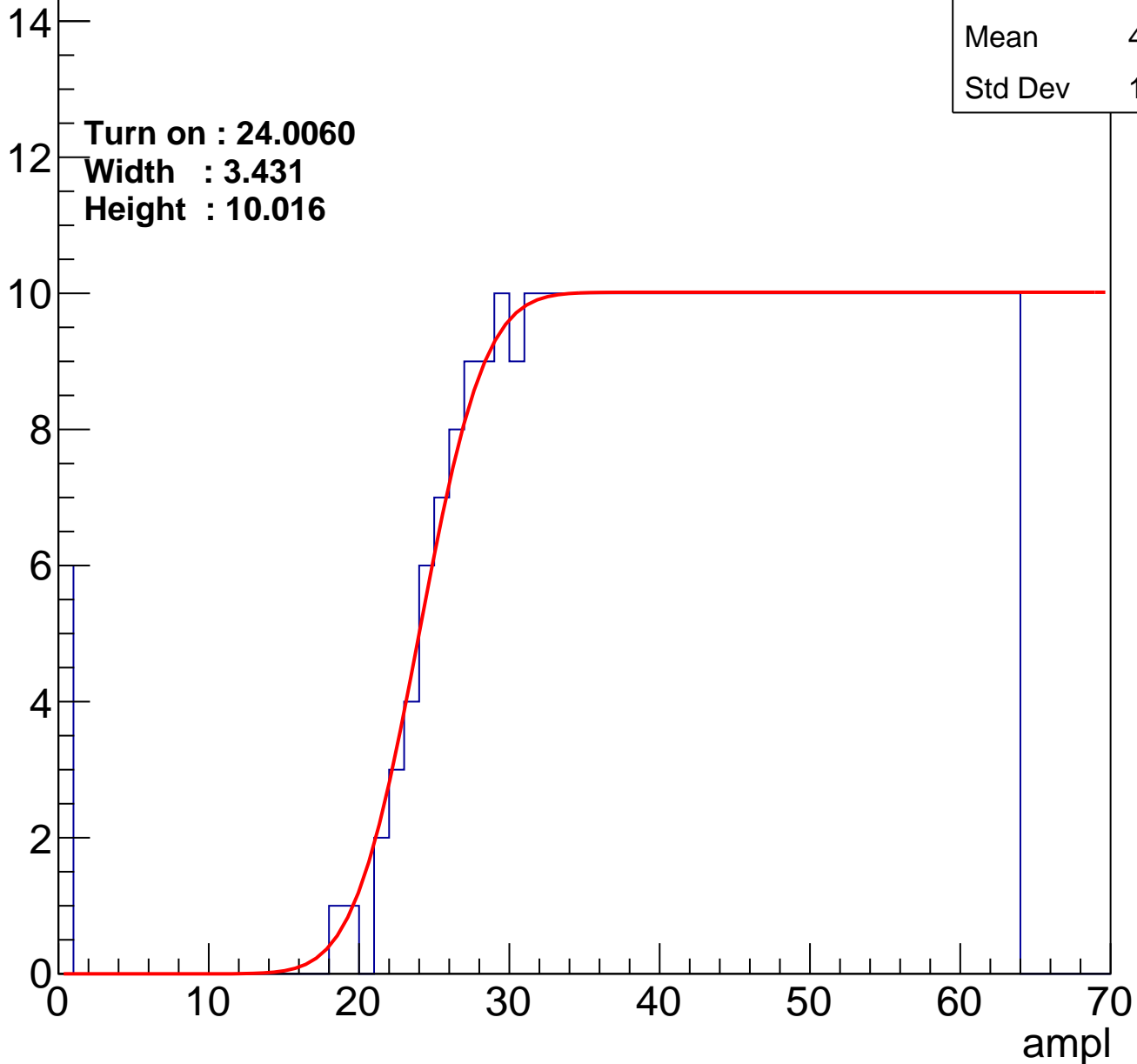
Entries	405
Mean	42.79
Std Dev	12.76

Turn on : 24.0060

Width : 3.431

Height : 10.016

Entry



B1L103S, U1-ch122

calib_packv5_042523_0143.root, FC#7, port C2

Entries	409
Mean	42.78
Std Dev	12.35

Turn on : 23.4670

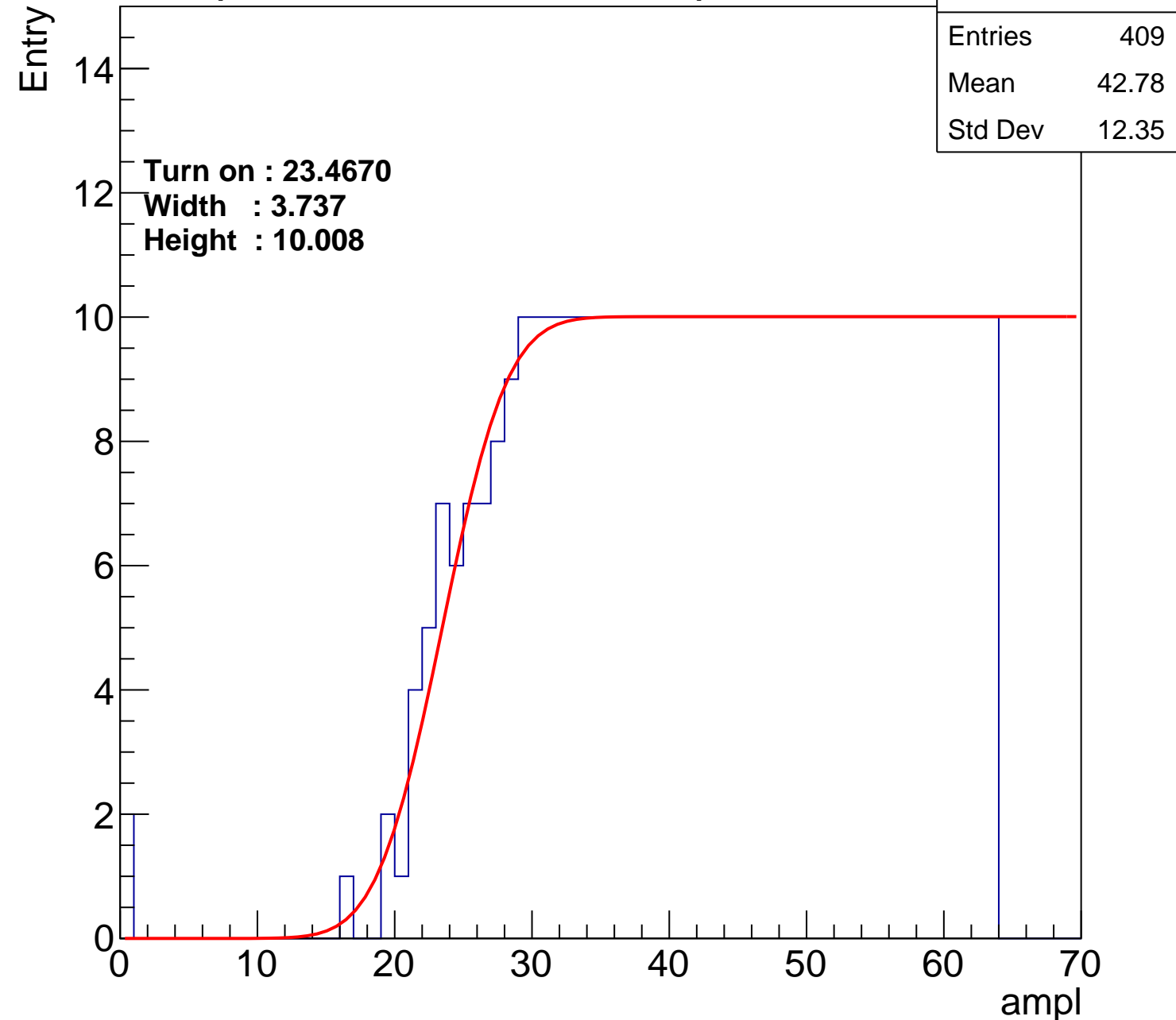
Width : 3.737

Height : 10.008

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch123

calib_packv5_042523_0143.root, FC#7, port C2

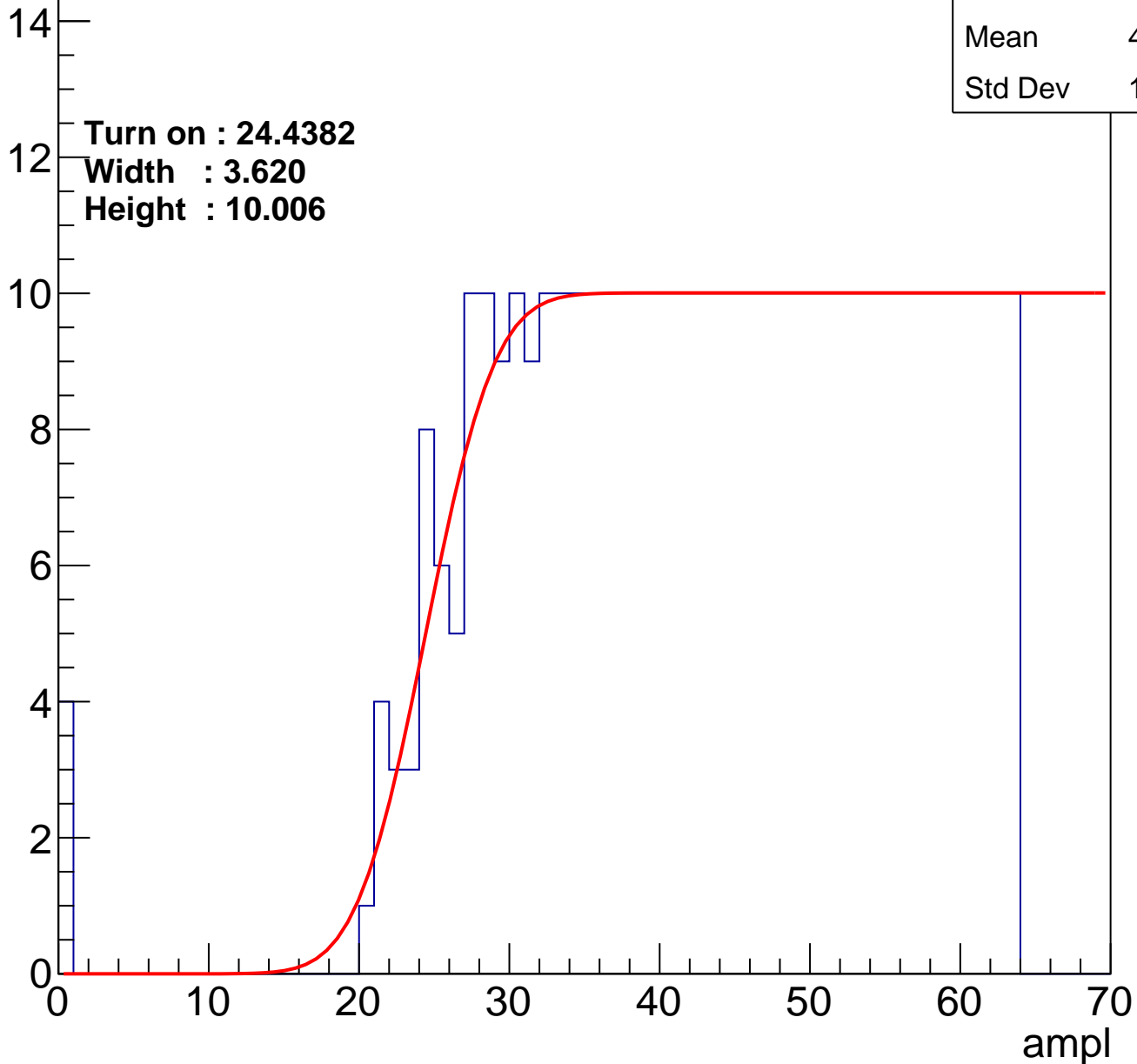
Entries	402
Mean	43.04
Std Dev	12.42

Turn on : 24.4382

Width : 3.620

Height : 10.006

Entry



B1L103S, U1-ch124

calib_packv5_042523_0143.root, FC#7, port C2

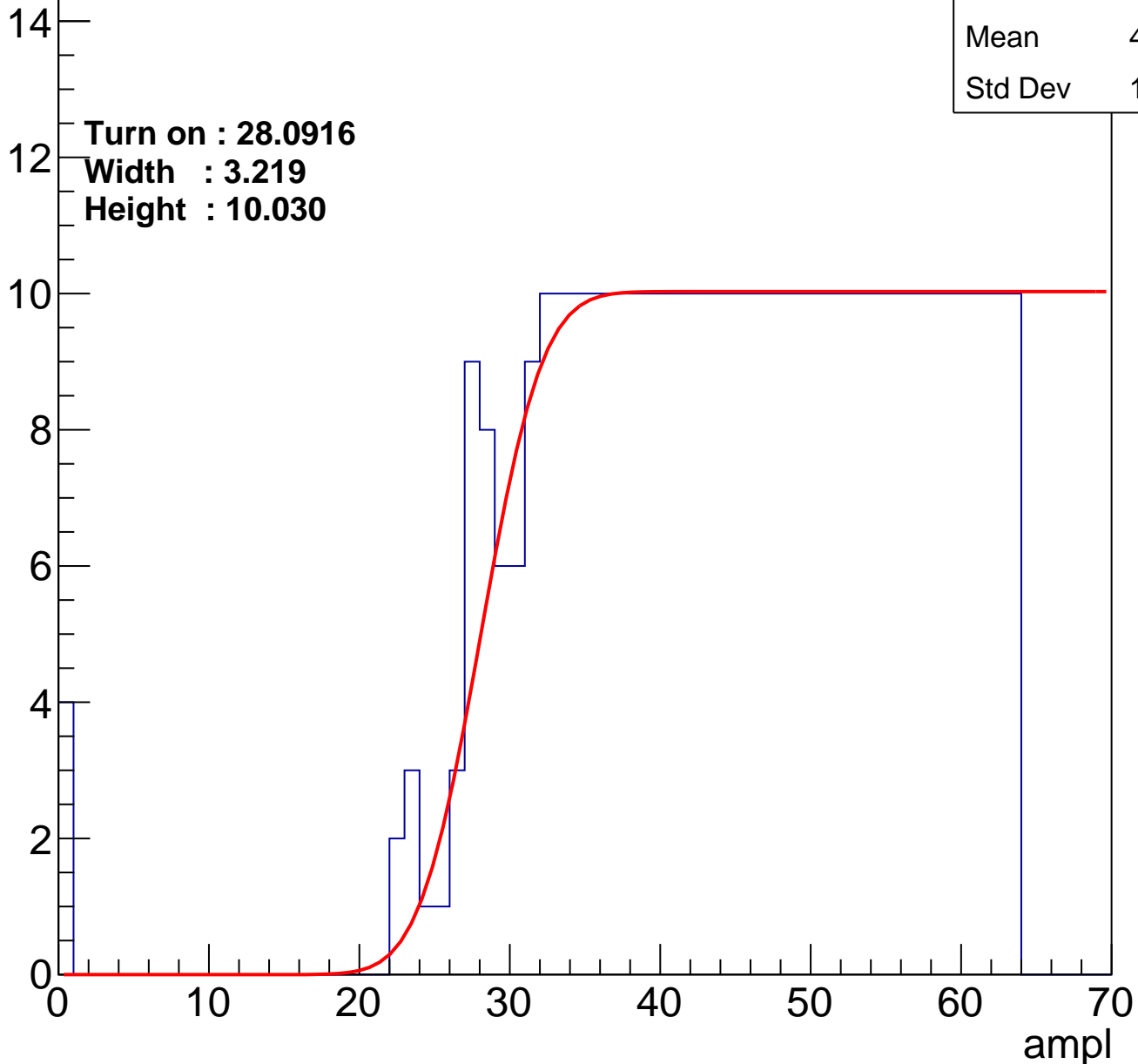
Entries	372
Mean	44.46
Std Dev	11.78

Turn on : 28.0916

Width : 3.219

Height : 10.030

Entry



B1L103S, U1-ch125

calib_packv5_042523_0143.root, FC#7, port C2

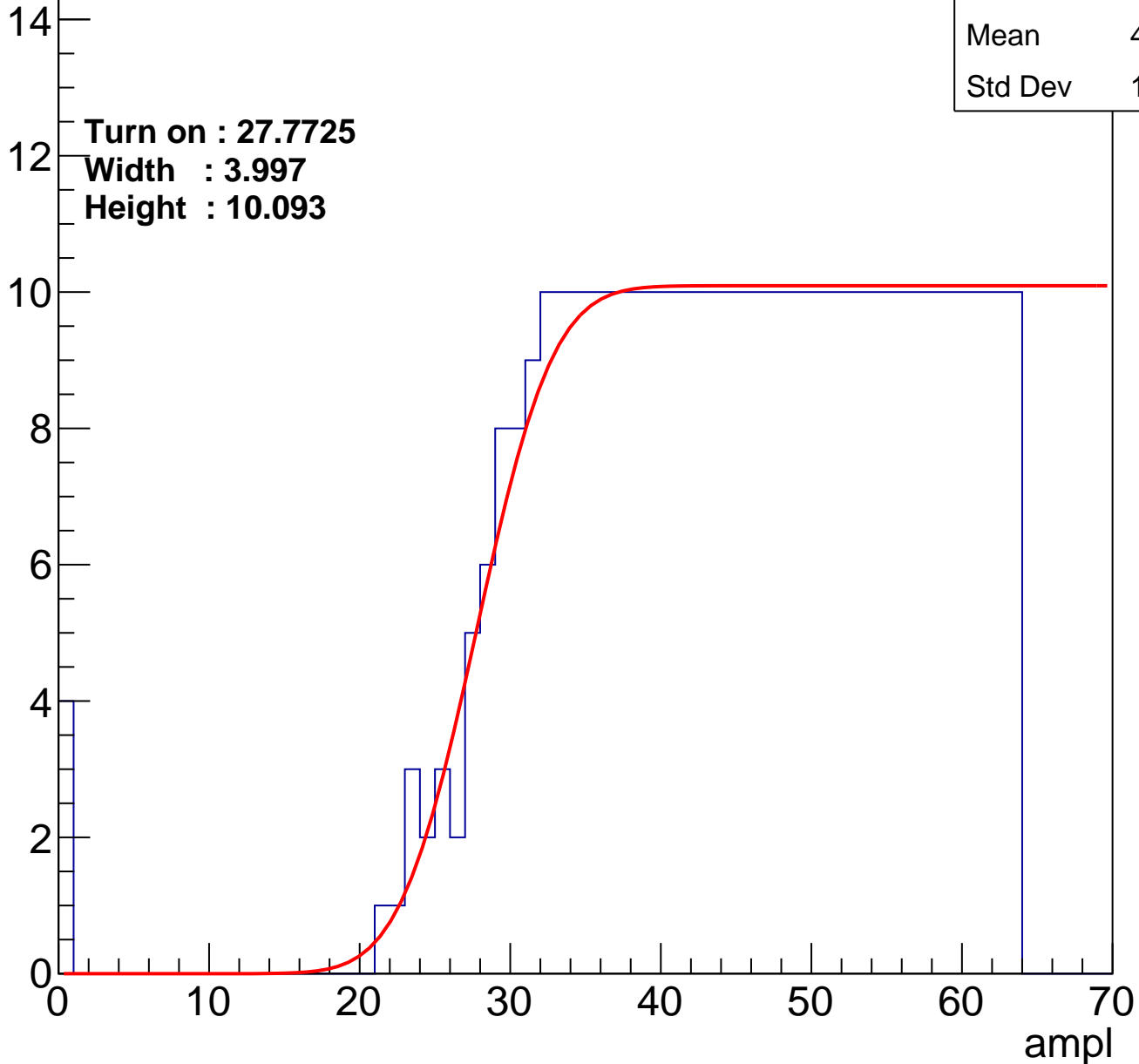
Entries	372
Mean	44.47
Std Dev	11.78

Turn on : 27.7725

Width : 3.997

Height : 10.093

Entry



B1L103S, U1-ch126

calib_packv5_042523_0143.root, FC#7, port C2

Entries	399
Mean	43.34
Std Dev	11.94

Turn on : 24.3484

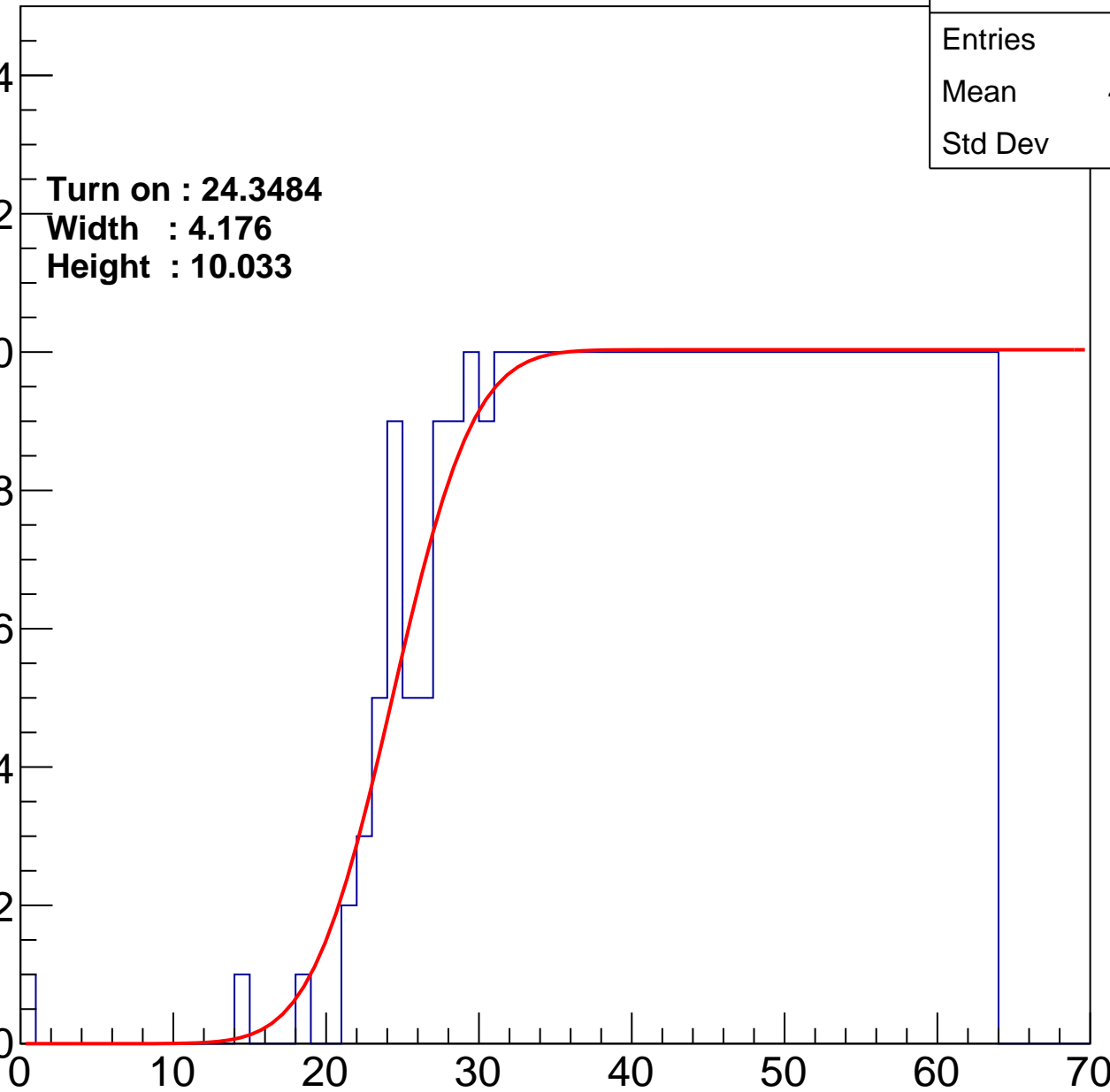
Width : 4.176

Height : 10.033

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch127

calib_packv5_042523_0143.root, FC#7, port C2

Entries	399
Mean	43.08
Std Dev	12.56

Turn on : 25.3553

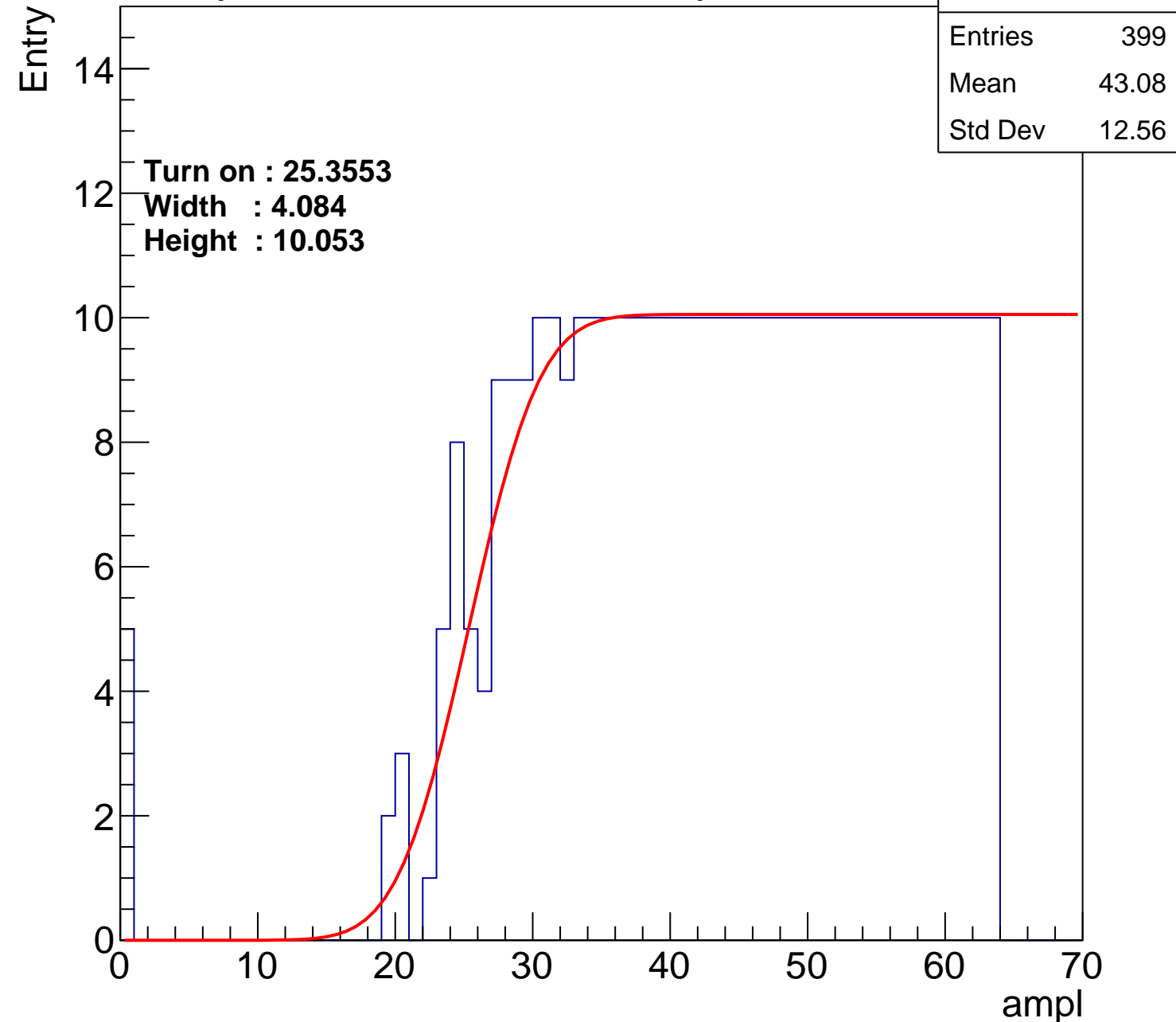
Width : 4.084

Height : 10.053

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U1-ch127

calib_packv5_042523_0143.root, FC#7, port C2

Entries	399
Mean	43.08
Std Dev	12.56

Turn on : 25.3553

Width : 4.084

Height : 10.053

Entry

14
12
10
8
6
4
2
0

ampl

