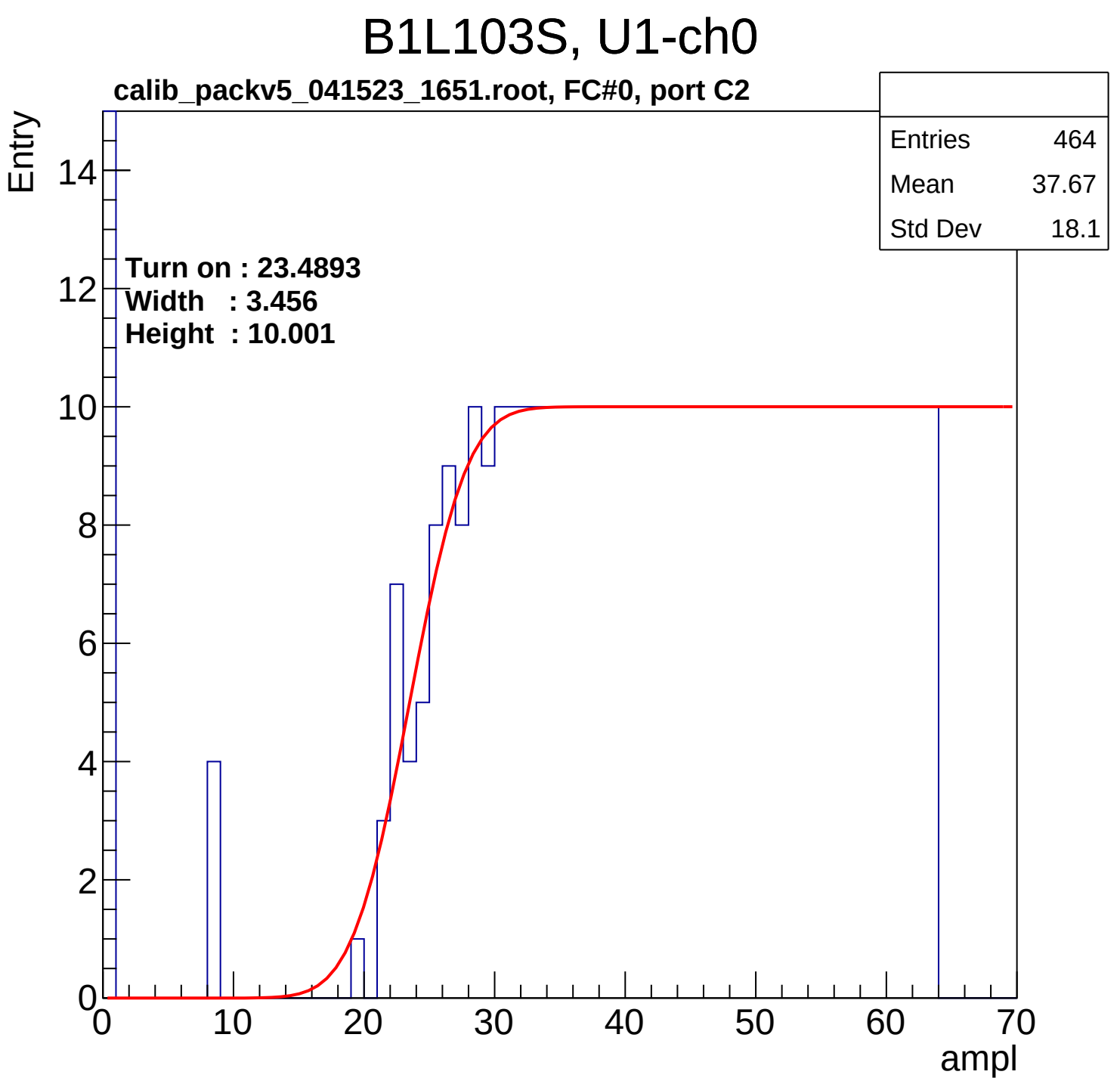
B1L103S, U1-ch0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 464
Mean 37.67
Std Dev 18.1
Turn on : 23.4893
Width : 3.456
Height : 10.001
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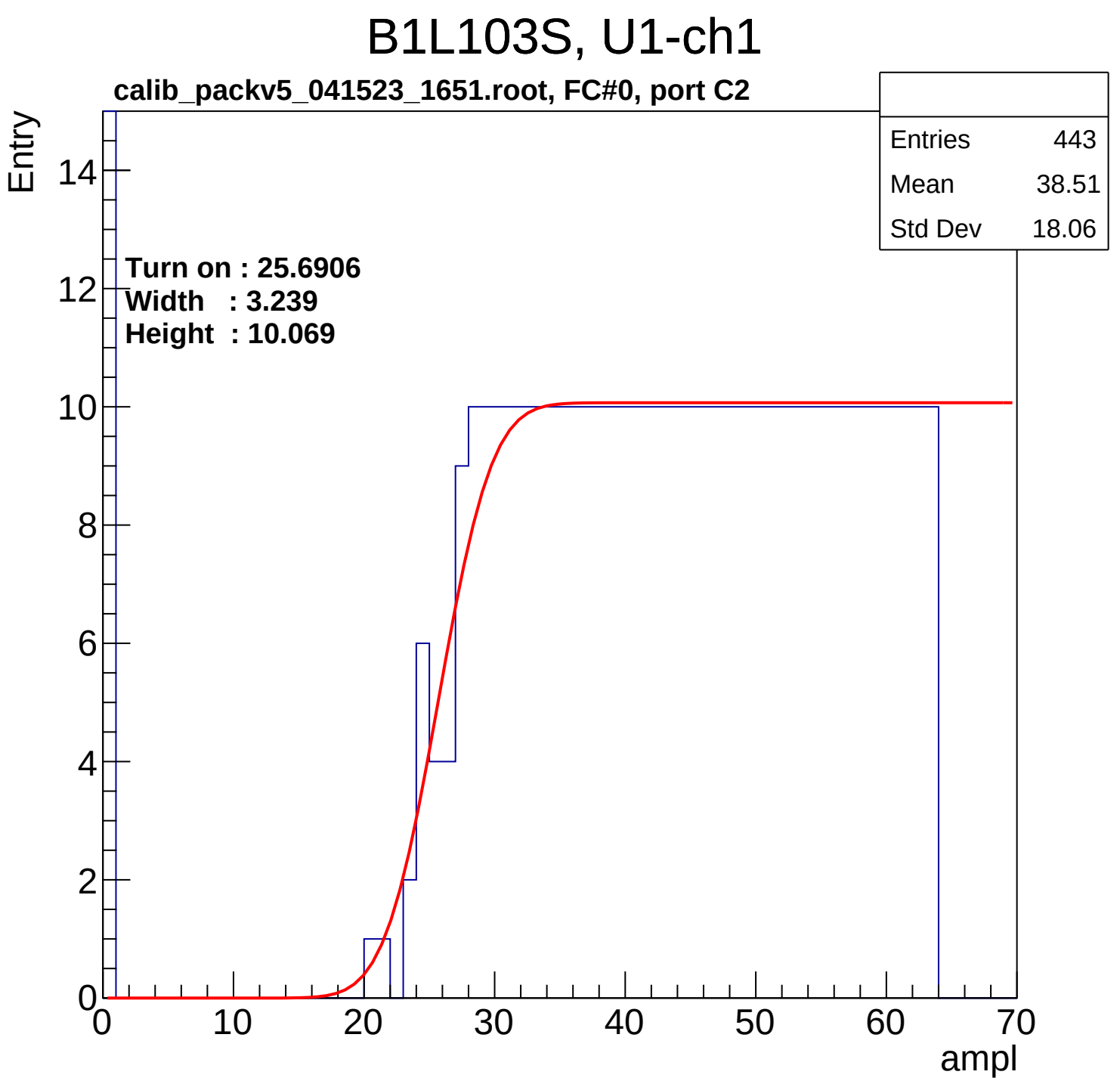
B1L103S, U1-ch1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 443
Mean 38.51
Std Dev 18.06
Turn on : 25.6906
Width : 3.239
Height : 10.069
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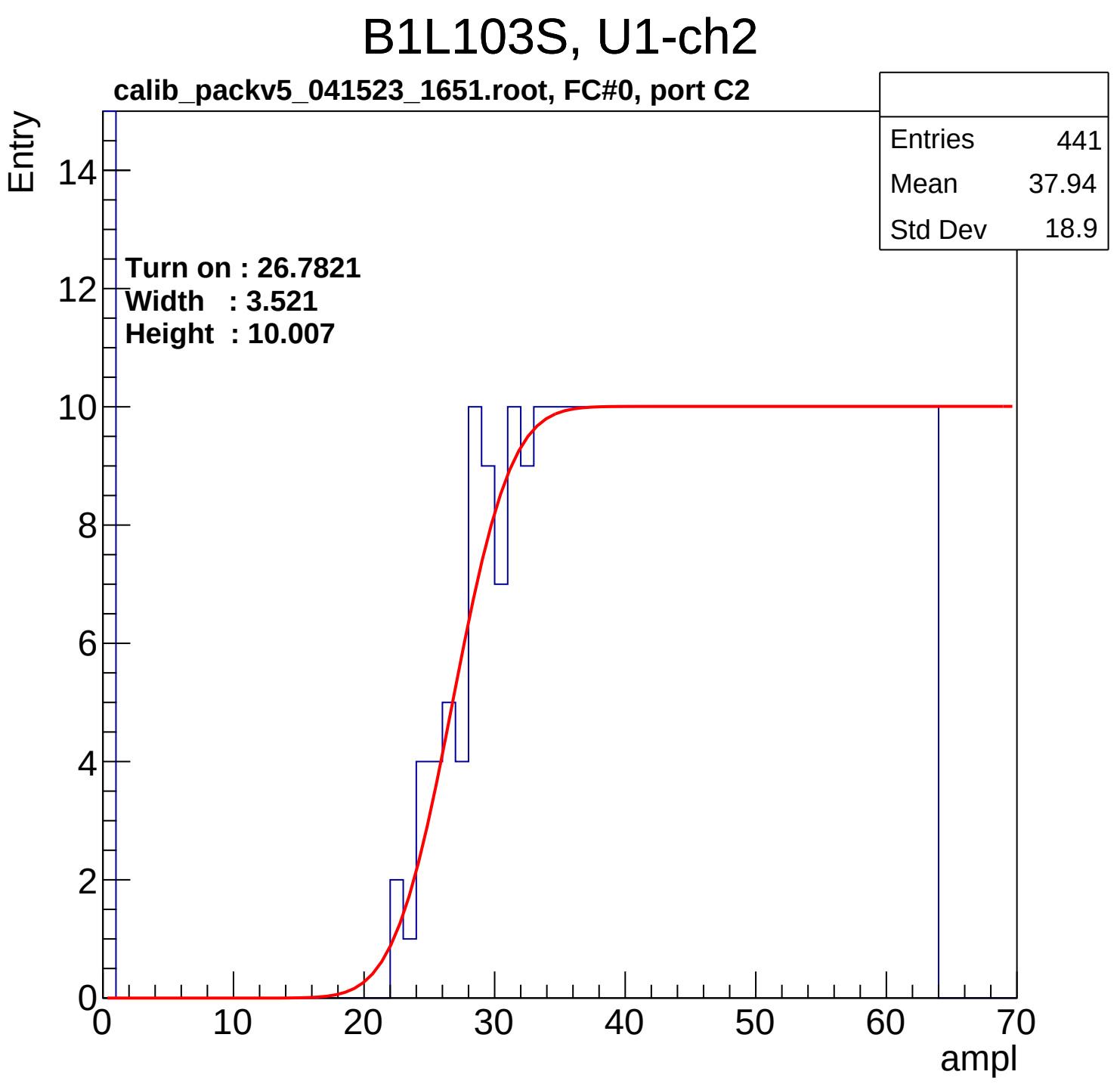
B1L103S, U1-ch2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 441
Mean 37.94
Std Dev 18.9
Turn on : 26.7821
Width : 3.521
Height : 10.007
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ampl
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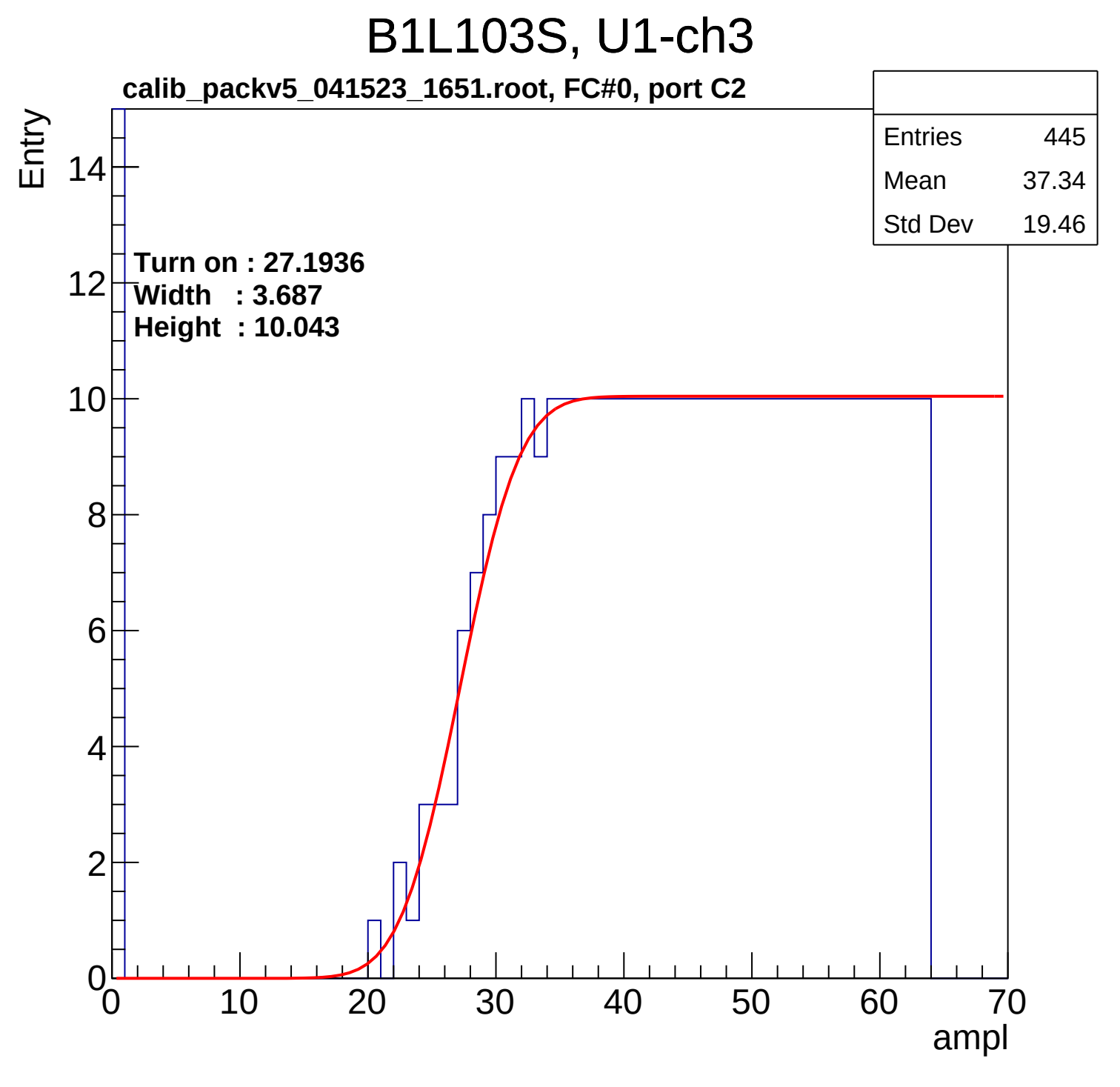
B1L103S, U1-ch3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 445
Mean 37.34
Std Dev 19.46
Turn on : 27.1936
Width : 3.687
Height : 10.043
Entry
ampl
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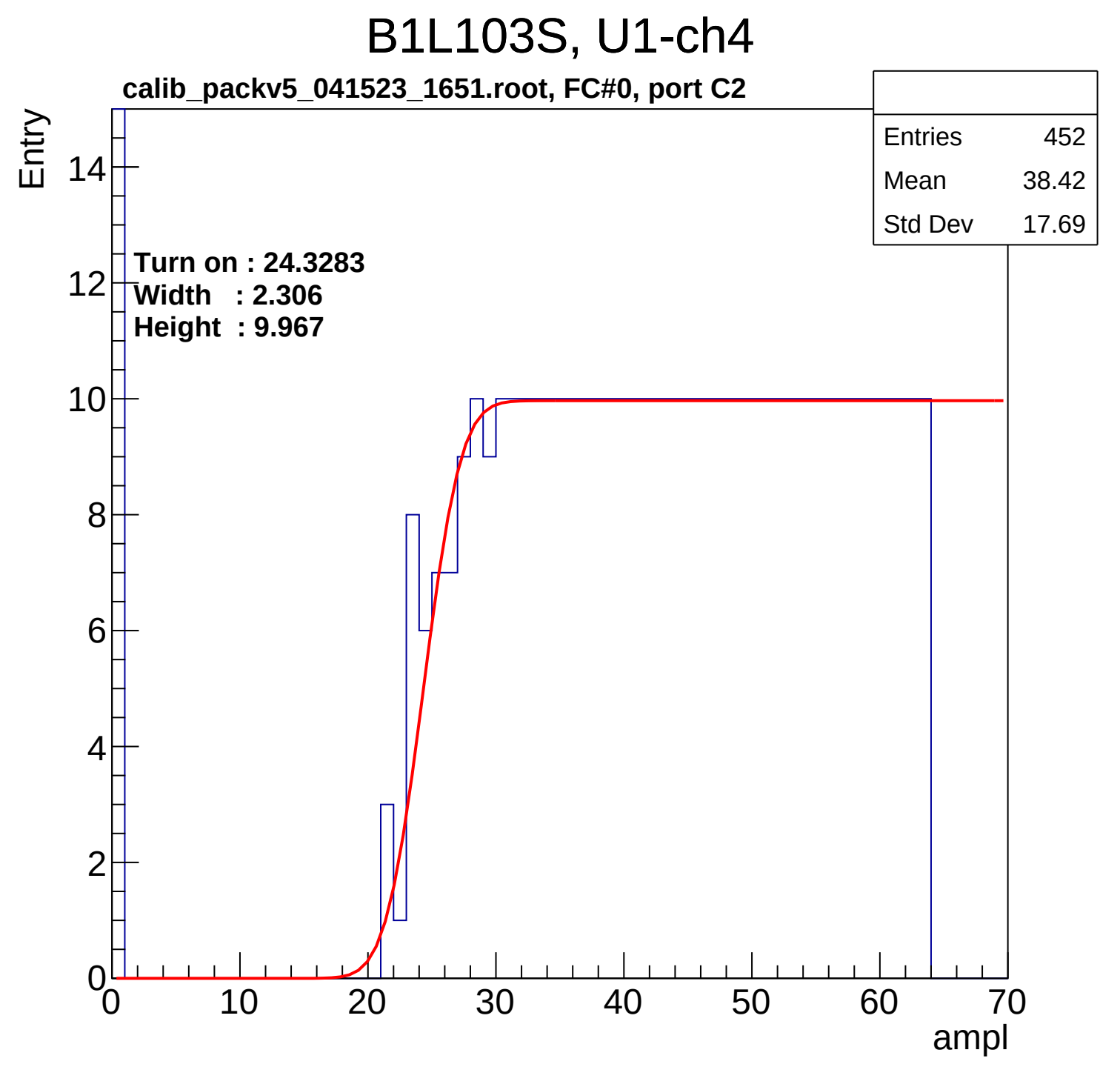
B1L103S, U1-ch4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 452
Mean 38.42
Std Dev 17.69
Turn on : 24.3283
Width : 2.306
Height : 9.967
Entry
ampl
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2
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6
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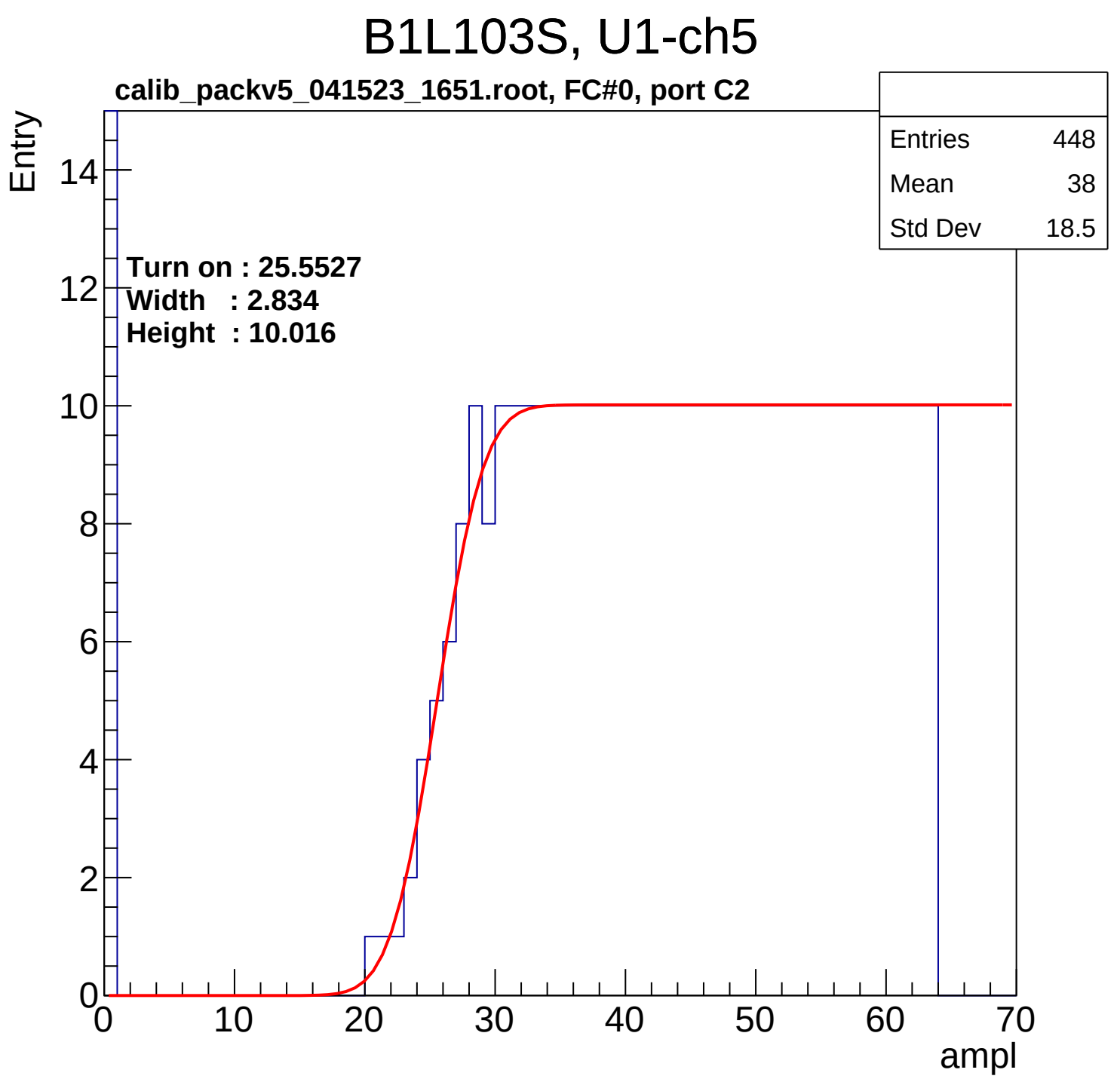
B1L103S, U1-ch5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 448
Mean 38
Std Dev 18.5
Turn on : 25.5527
Width : 2.834
Height : 10.016
Entry
ampl
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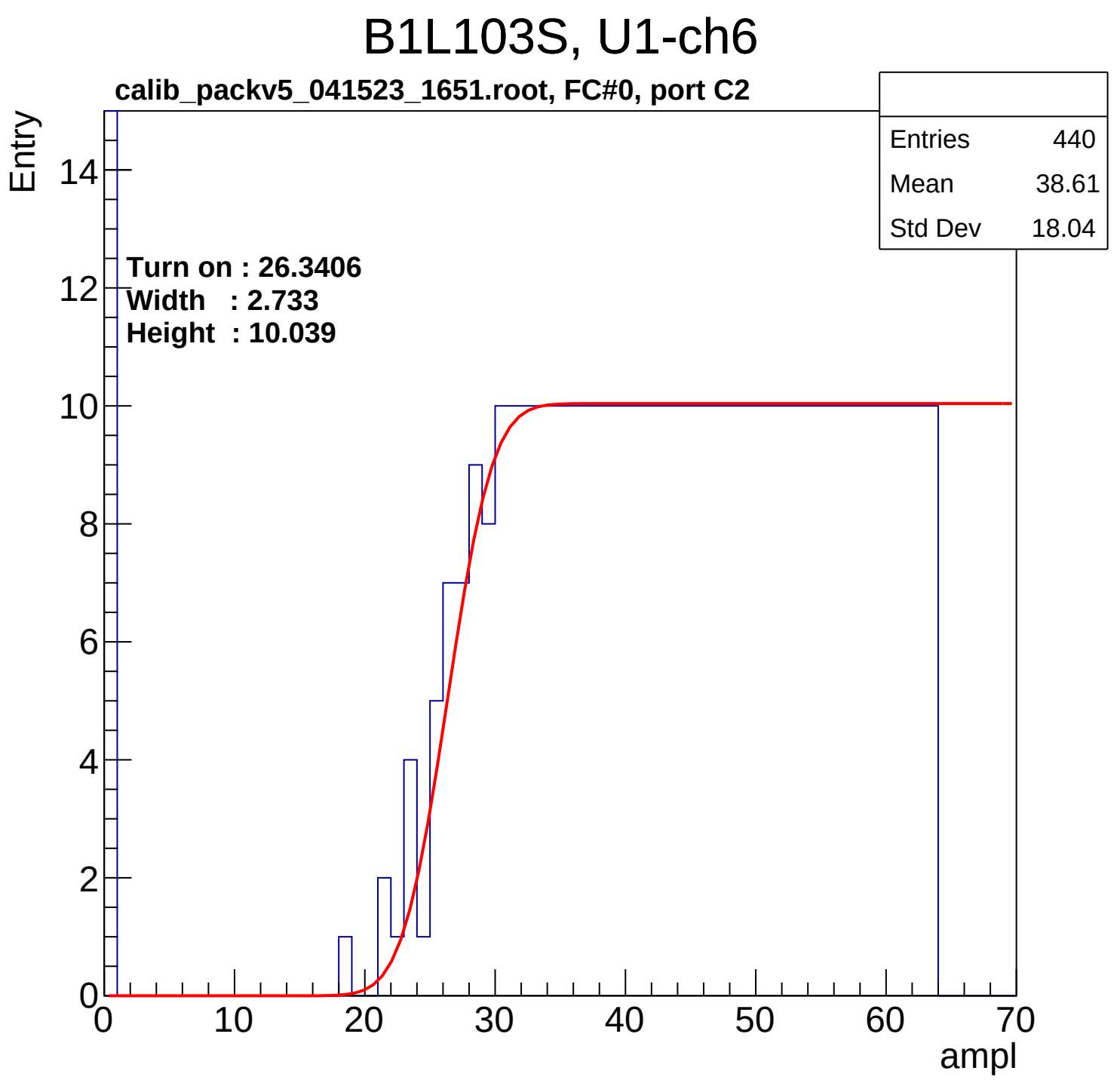
B1L103S, U1-ch6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 440
Mean 38.61
Std Dev 18.04
Turn on : 26.3406
Width : 2.733
Height : 10.039
Entry
ampl
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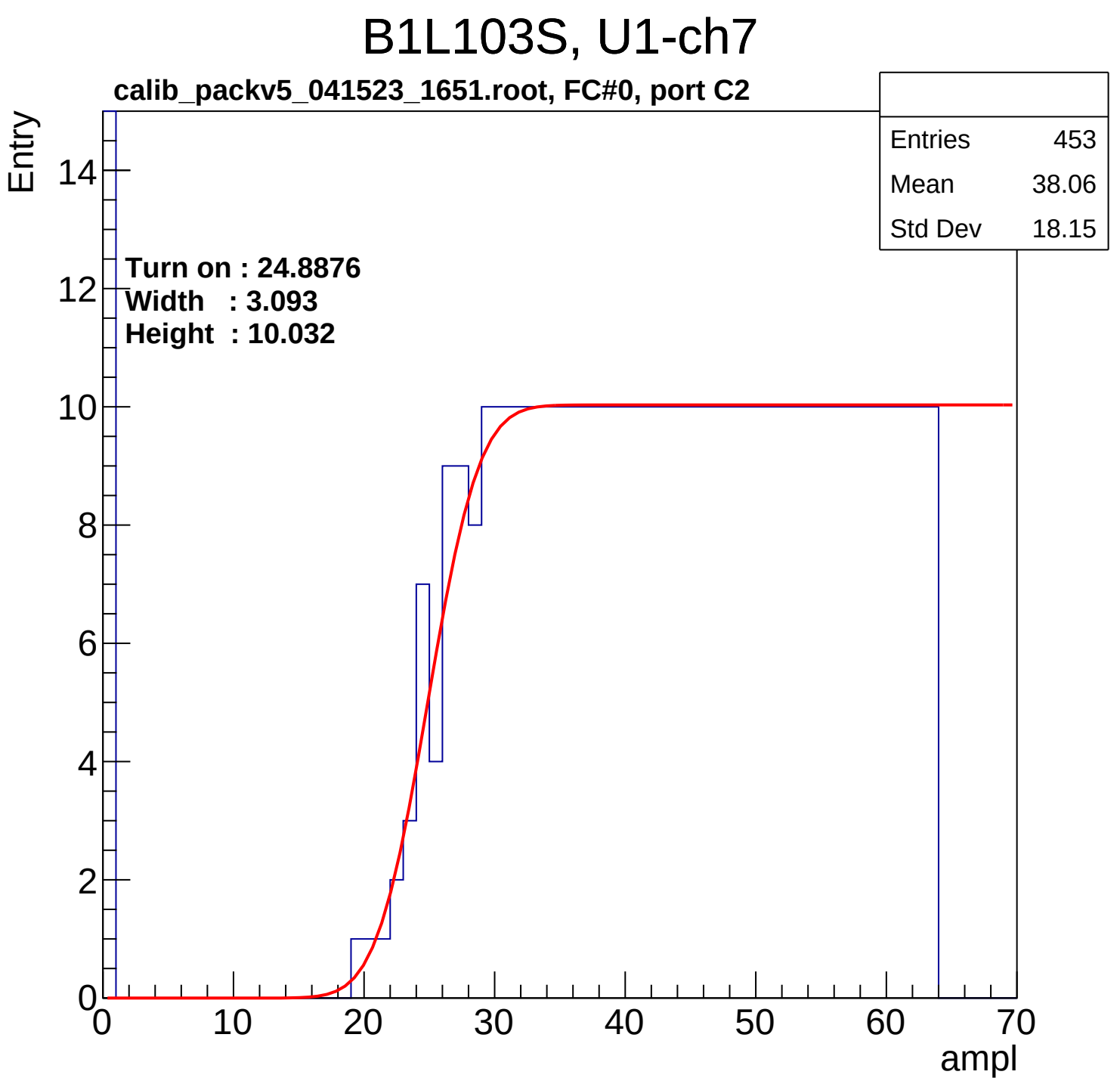
B1L103S, U1-ch7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 453
Mean 38.06
Std Dev 18.15
Turn on : 24.8876
Width : 3.093
Height : 10.032
Entry
ampl
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6
8
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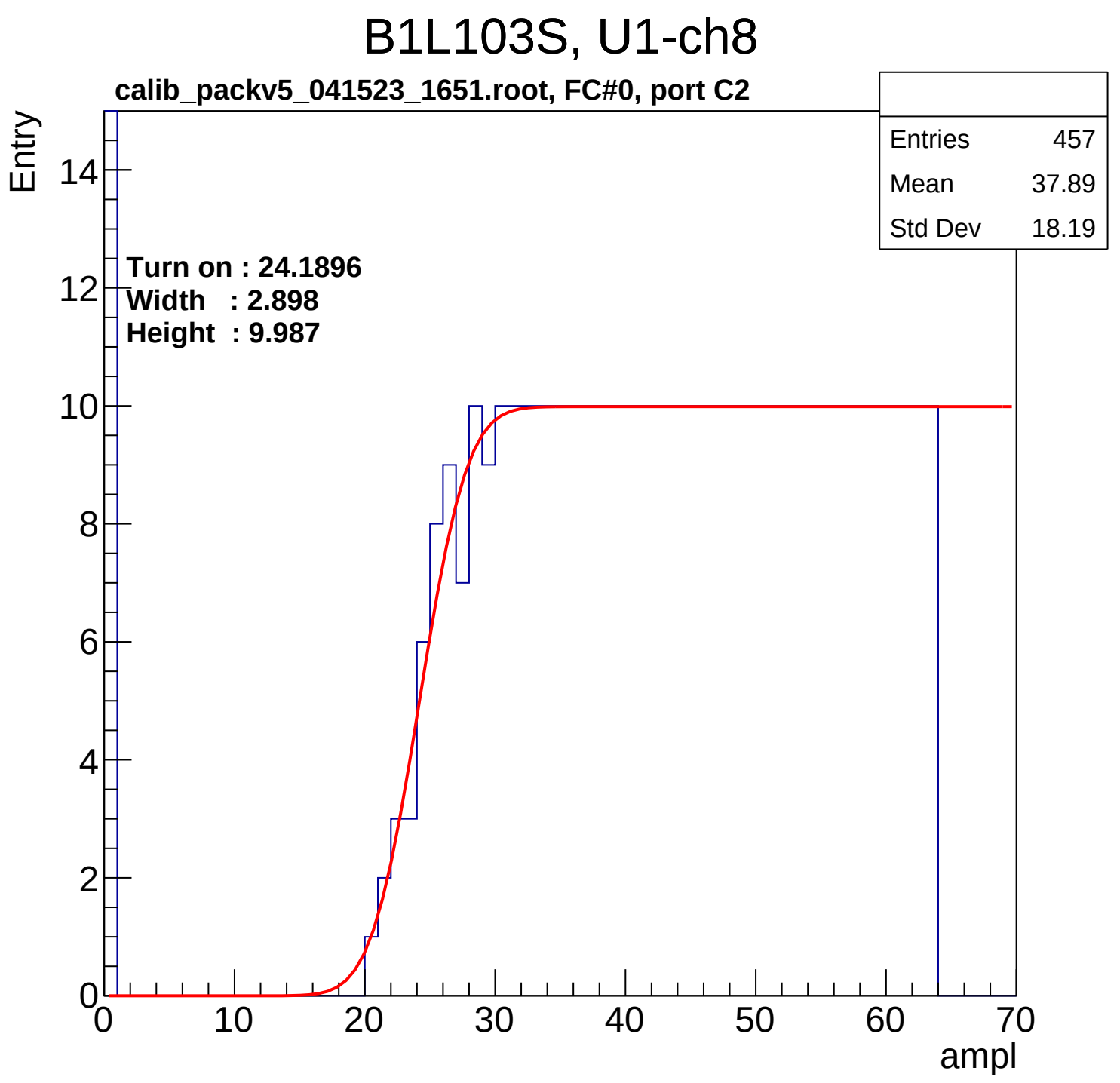
B1L103S, U1-ch8
calib_packv5_041523_1651.root, FC#0, port C2
Entries 457
Mean 37.89
Std Dev 18.19
Turn on : 24.1896
Width : 2.898
Height : 9.987
Entry
ampl
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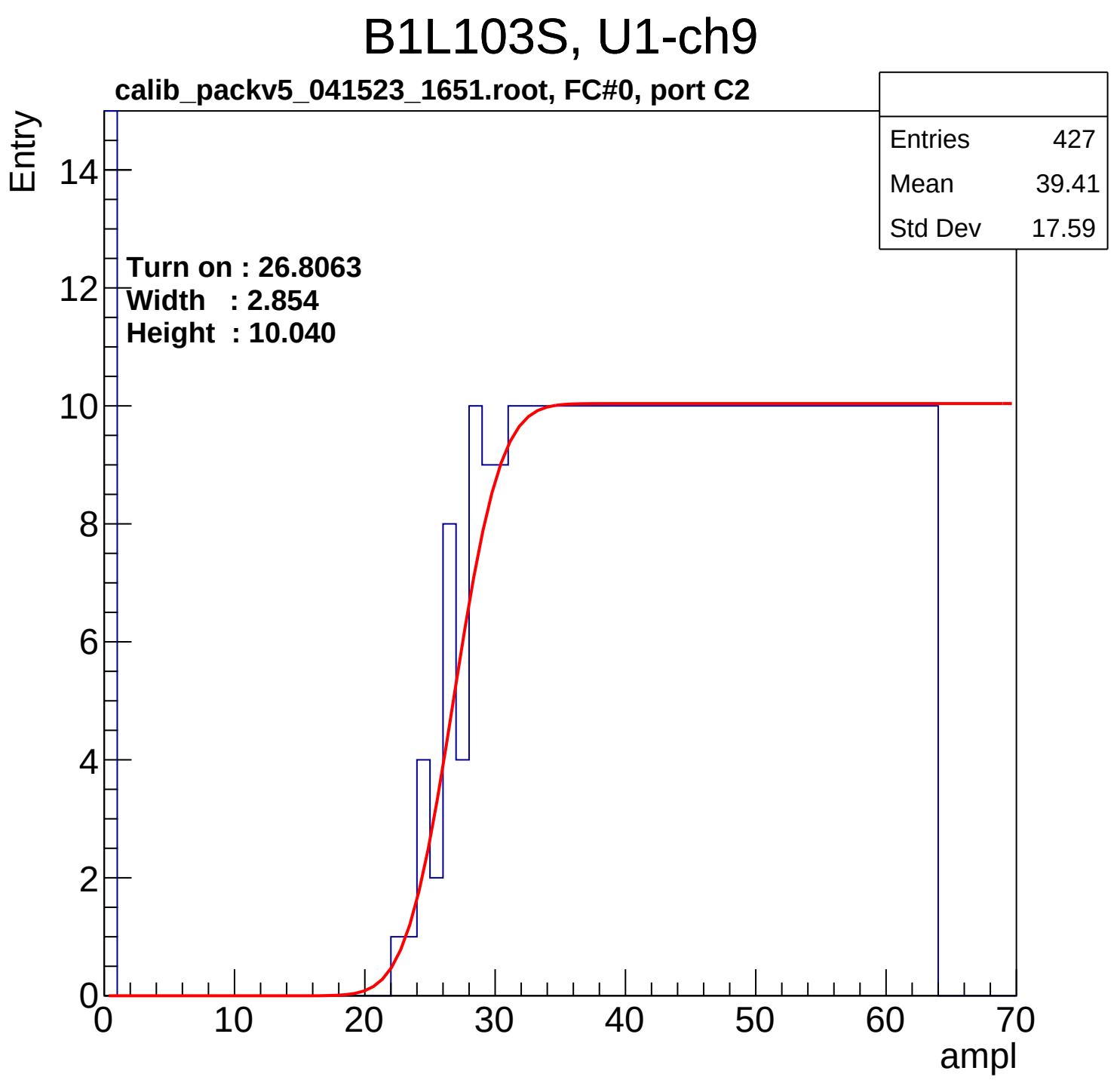
B1L103S, U1-ch9
calib_packv5_041523_1651.root, FC#0, port C2
Entries 427
Mean 39.41
Std Dev 17.59
Turn on : 26.8063
Width : 2.854
Height : 10.040
Entry
ampl
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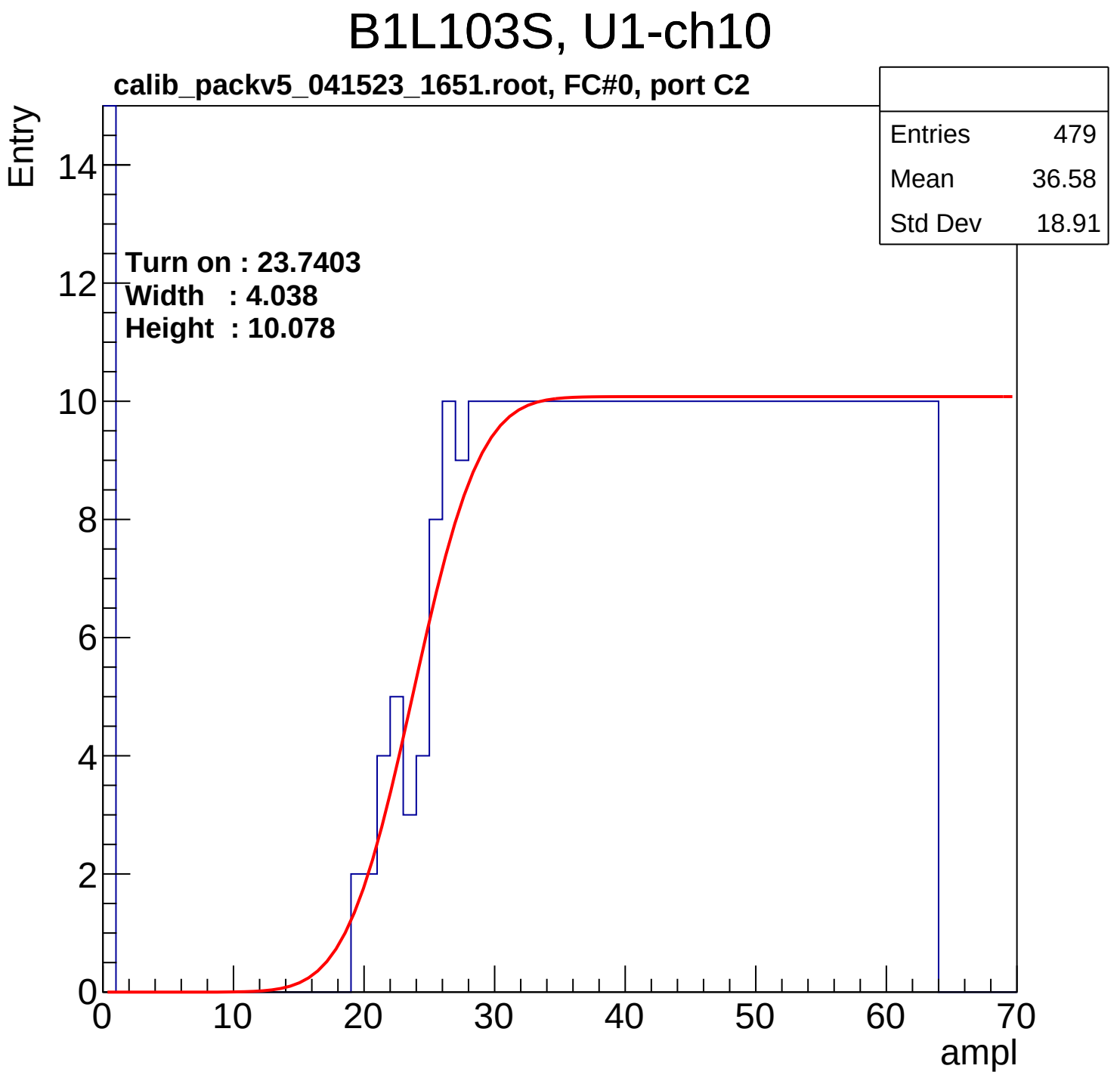
B1L103S, U1-ch10
calib_packv5_041523_1651.root, FC#0, port C2
Entries 479
Mean 36.58
Std Dev 18.91
Turn on : 23.7403
Width : 4.038
Height : 10.078
Entry
ampl
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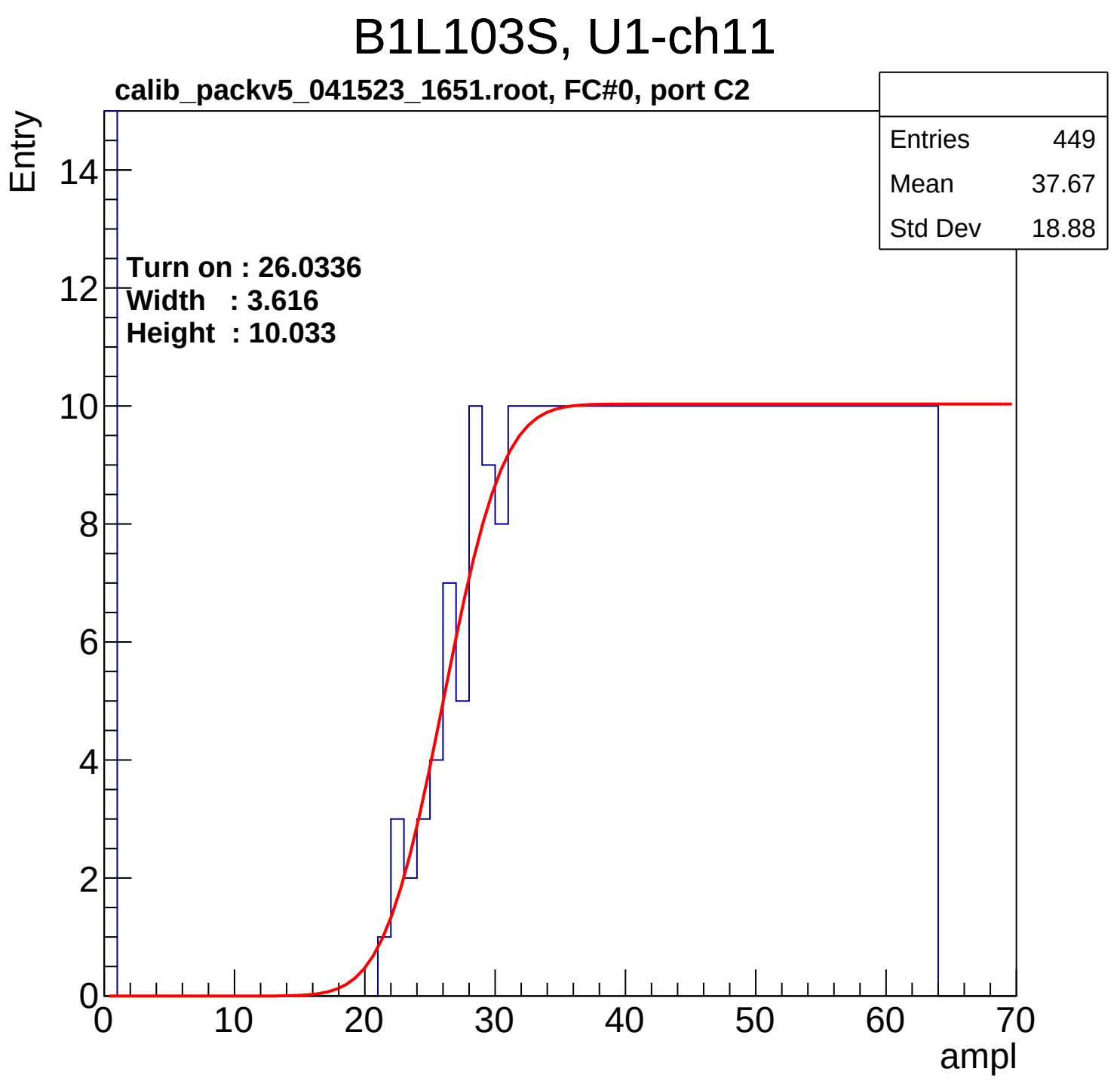
B1L103S, U1-ch11
calib_packv5_041523_1651.root, FC#0, port C2
Entries 449
Mean 37.67
Std Dev 18.88
Turn on : 26.0336
Width : 3.616
Height : 10.033
Entry
ampl
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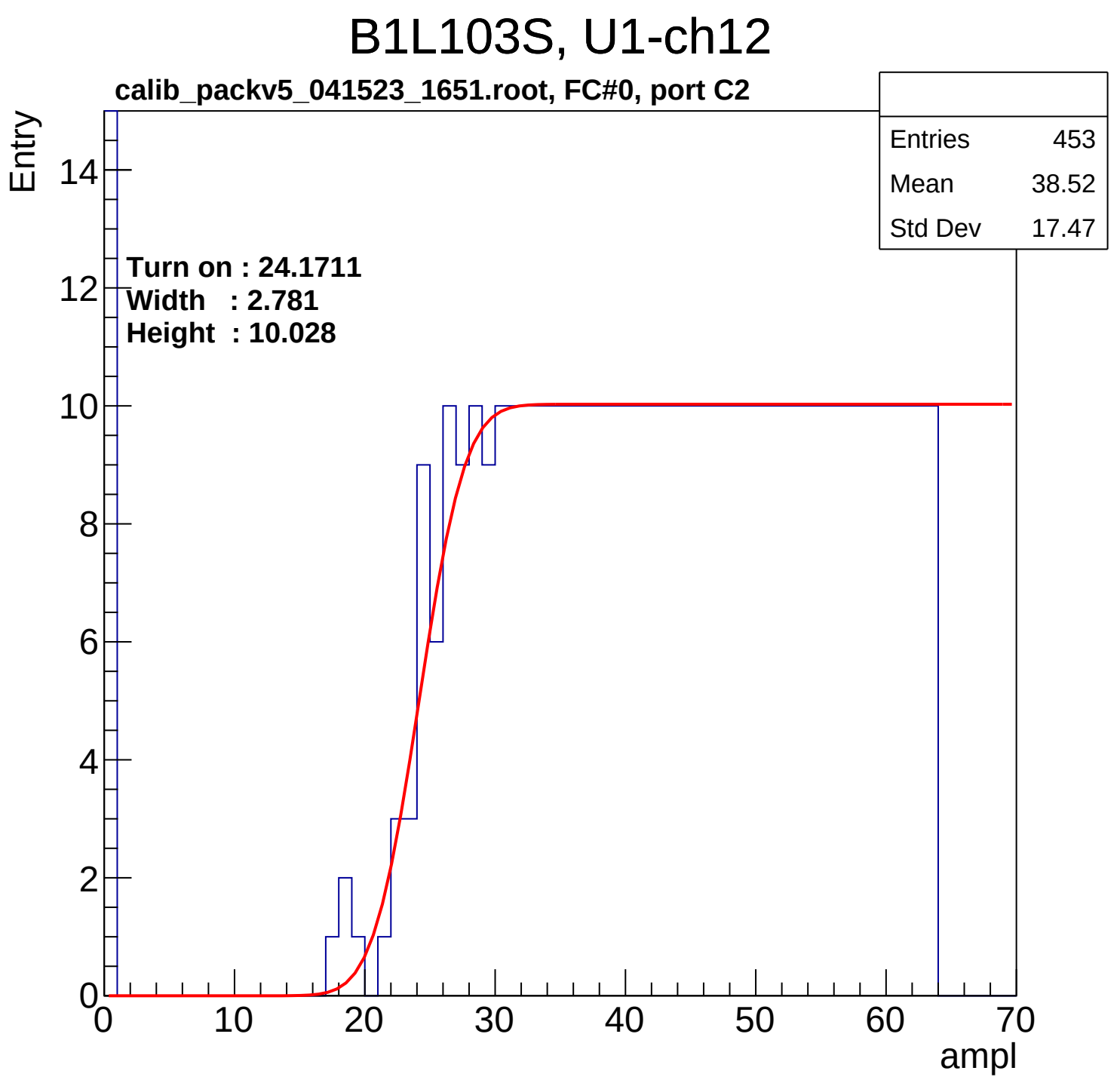
B1L103S, U1-ch12
calib_packv5_041523_1651.root, FC#0, port C2
Entries 453
Mean 38.52
Std Dev 17.47
Turn on : 24.1711
Width : 2.781
Height : 10.028
Entry
ampl
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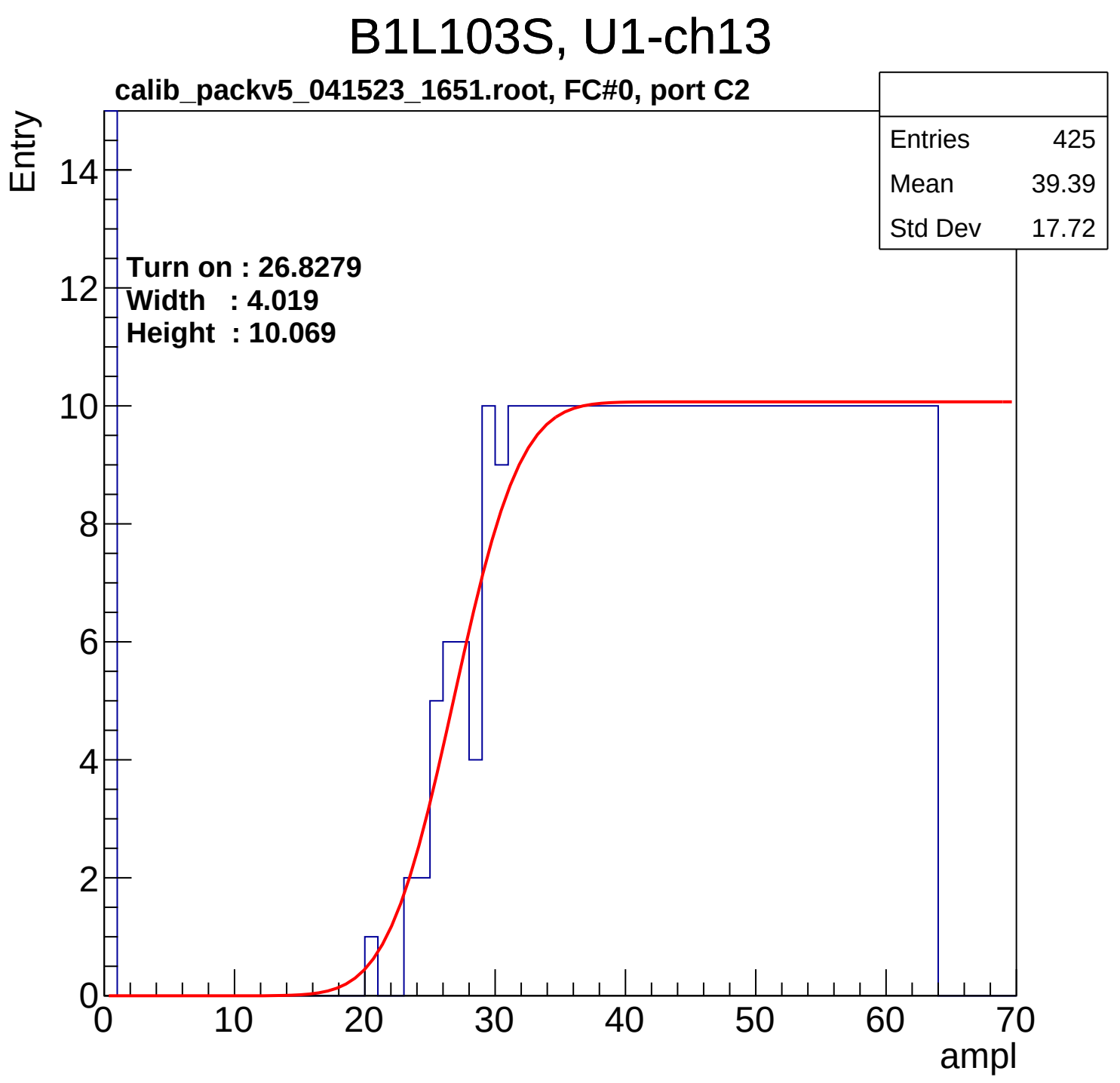
B1L103S, U1-ch13
calib_packv5_041523_1651.root, FC#0, port C2
Entries 425
Mean 39.39
Std Dev 17.72
Turn on : 26.8279
Width : 4.019
Height : 10.069
Entry
ampl
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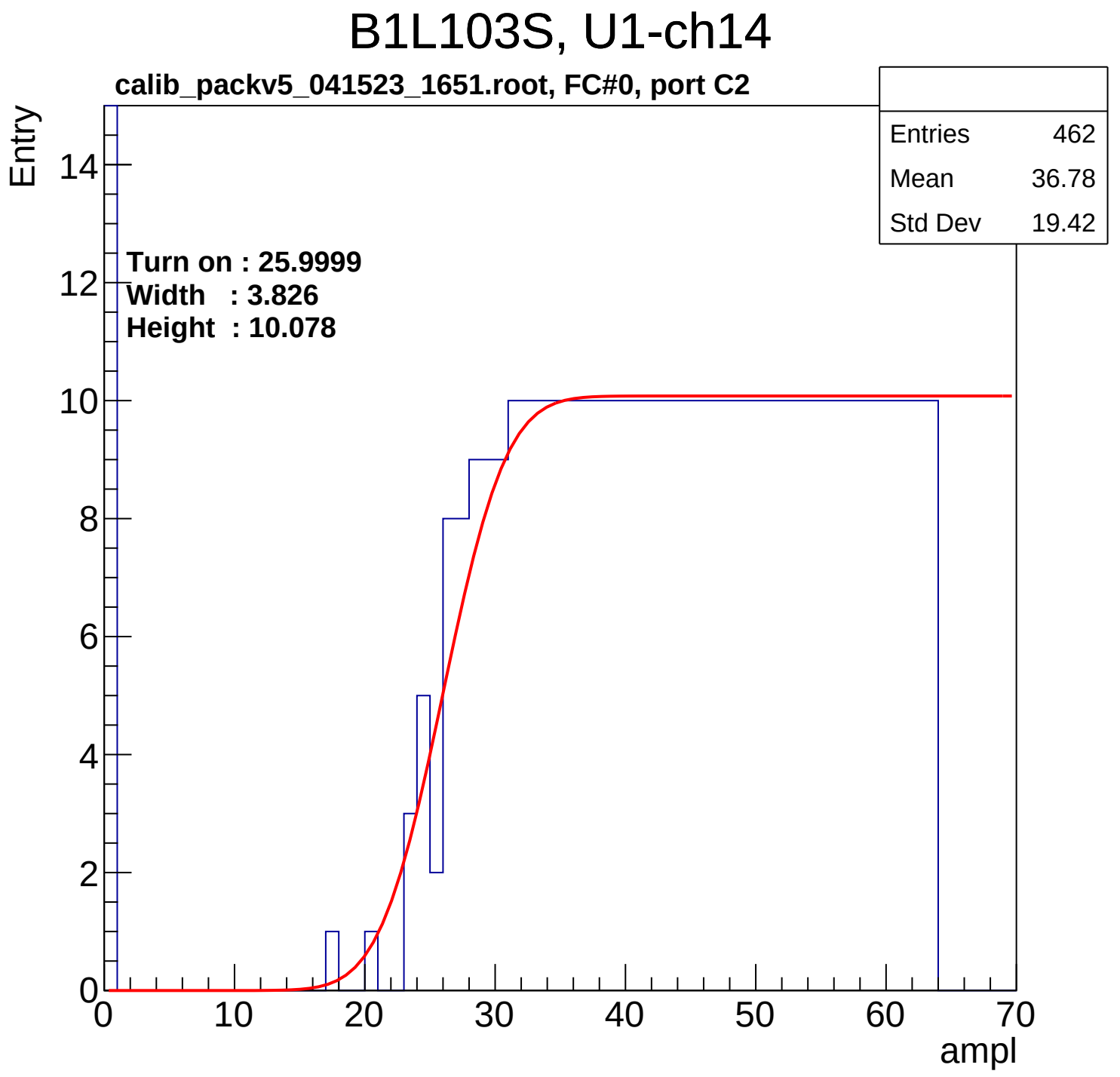
B1L103S, U1-ch14
calib_packv5_041523_1651.root, FC#0, port C2
Entries 462
Mean 36.78
Std Dev 19.42
Turn on : 25.9999
Width : 3.826
Height : 10.078
Entry
ampl
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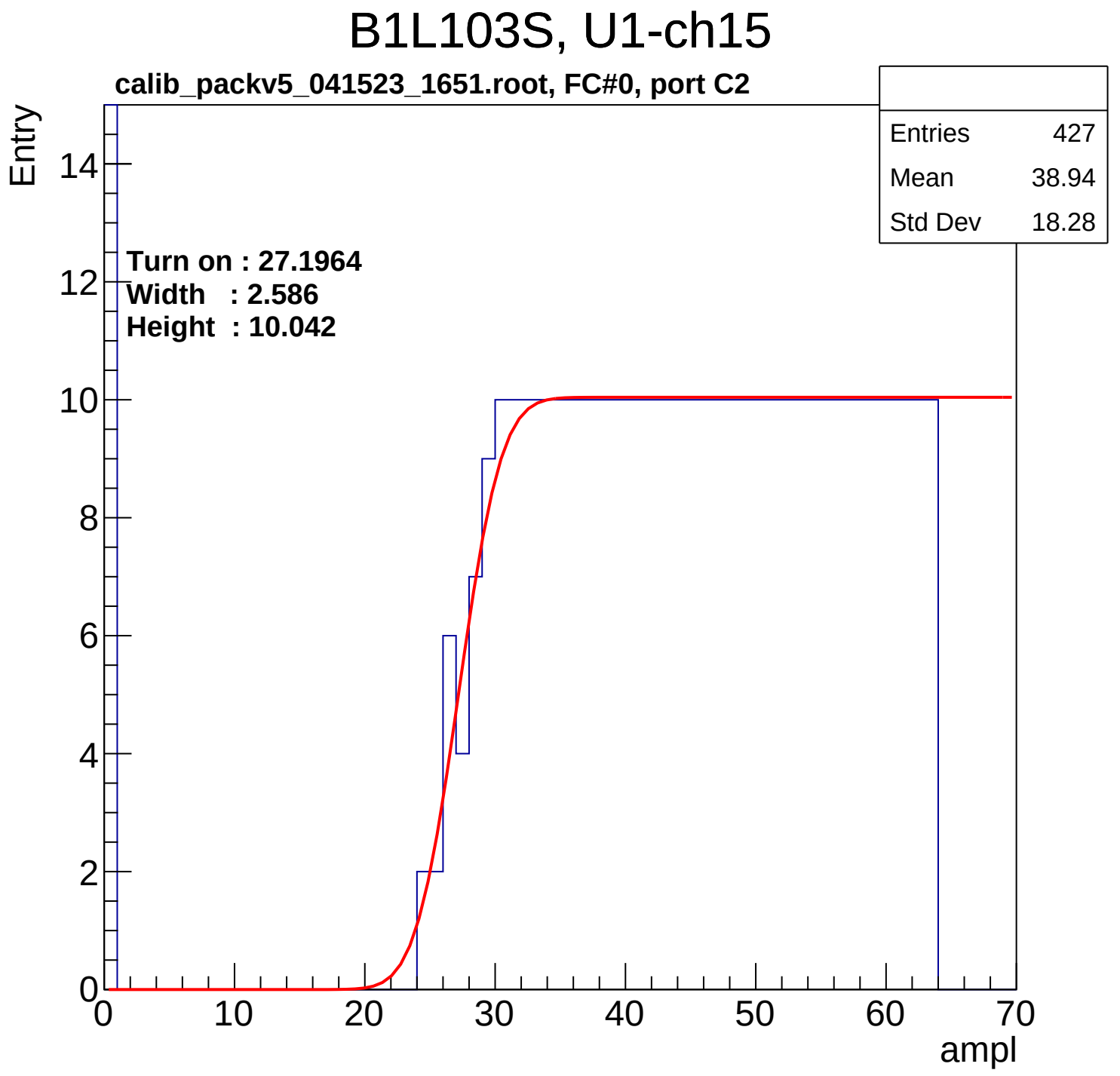
B1L103S, U1-ch15
calib_packv5_041523_1651.root, FC#0, port C2
Entries 427
Mean 38.94
Std Dev 18.28
Turn on : 27.1964
Width : 2.586
Height : 10.042
Entry
ampl
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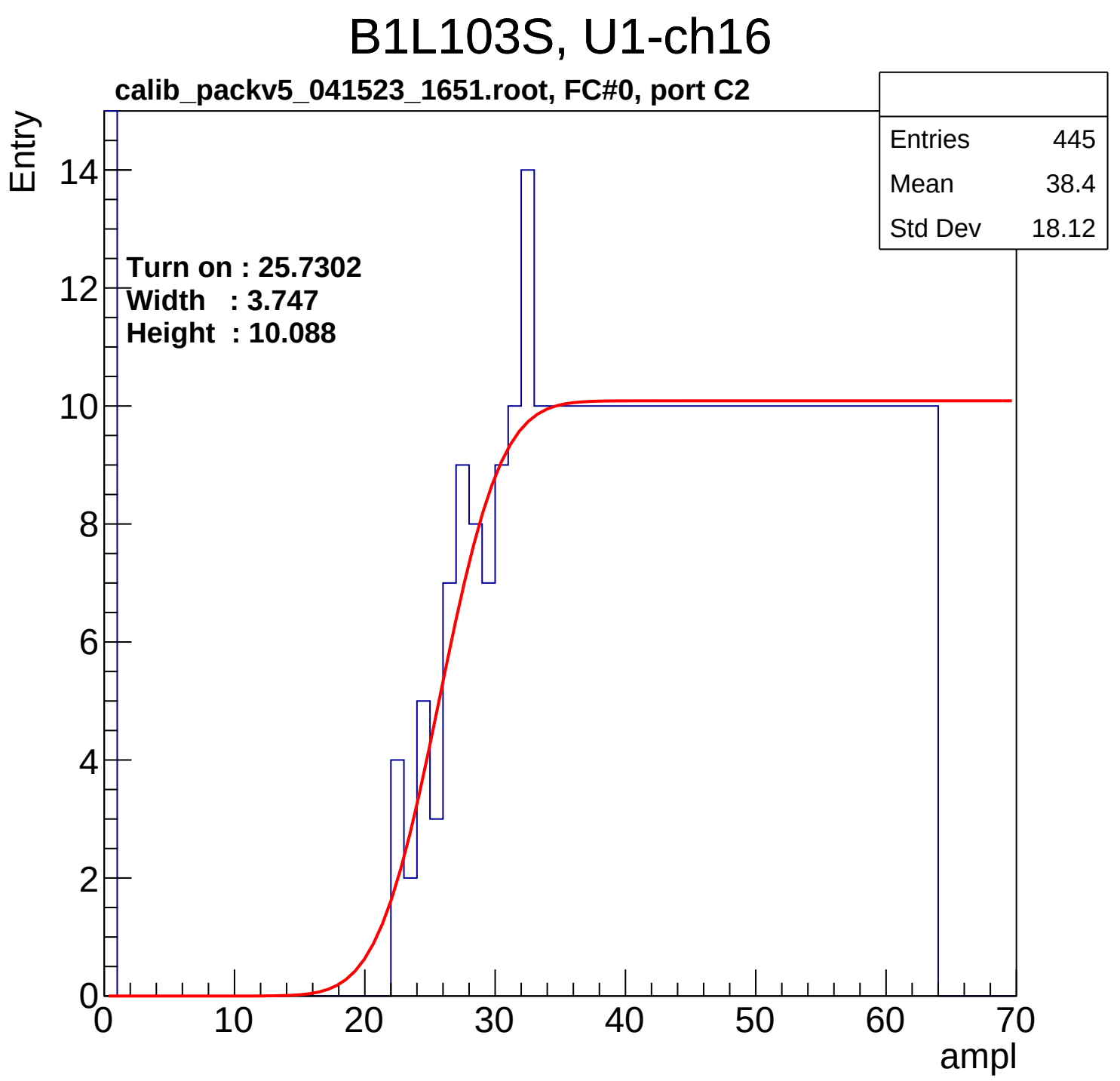
B1L103S, U1-ch16
calib_packv5_041523_1651.root, FC#0, port C2
Entries 445
Mean 38.4
Std Dev 18.12
Turn on : 25.7302
Width : 3.747
Height : 10.088
Entry
ampl
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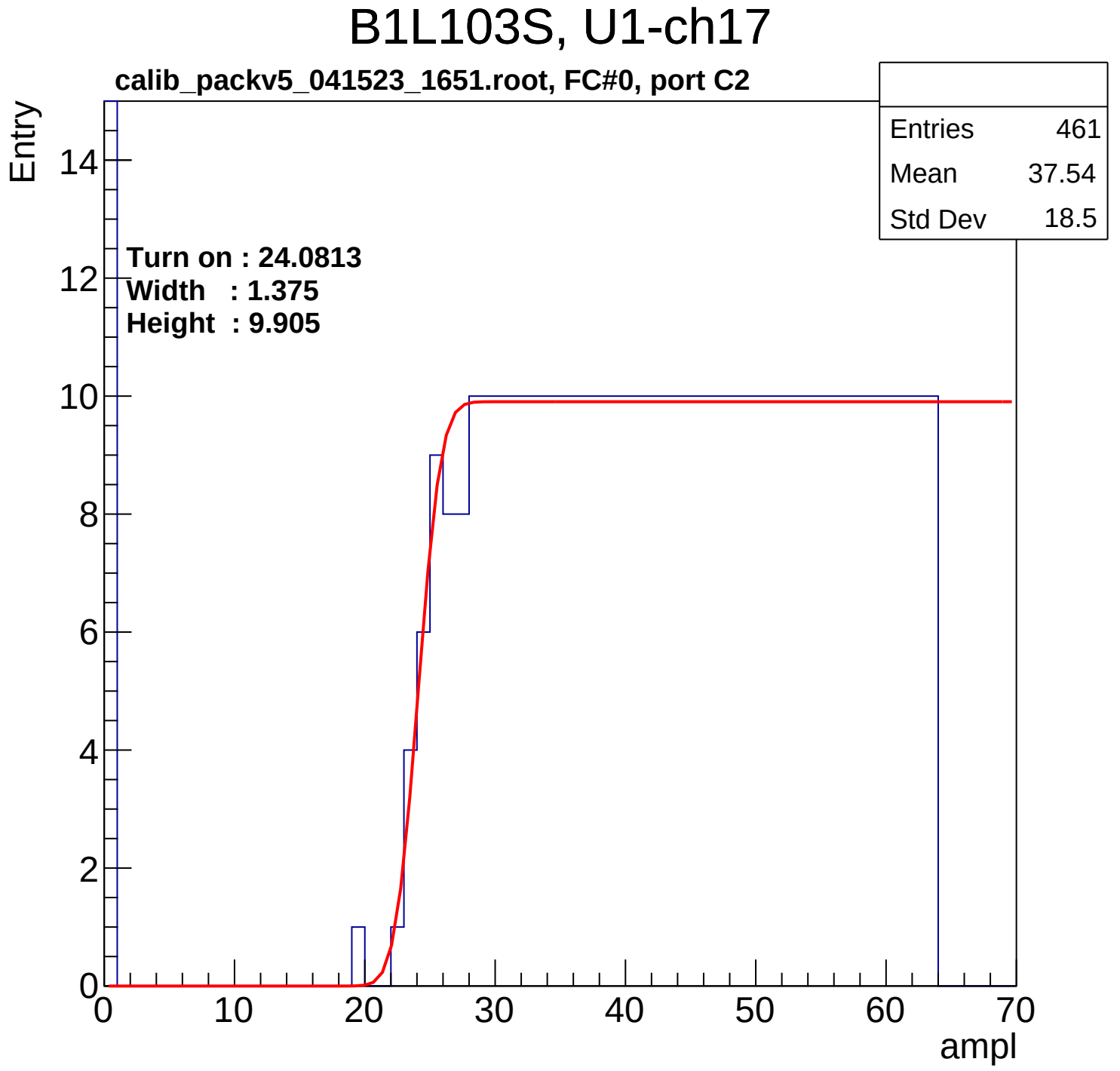
B1L103S, U1-ch17
calib_packv5_041523_1651.root, FC#0, port C2
Entries 461
Mean 37.54
Std Dev 18.5
Turn on : 24.0813
Width : 1.375
Height : 9.905
Entry
ampl
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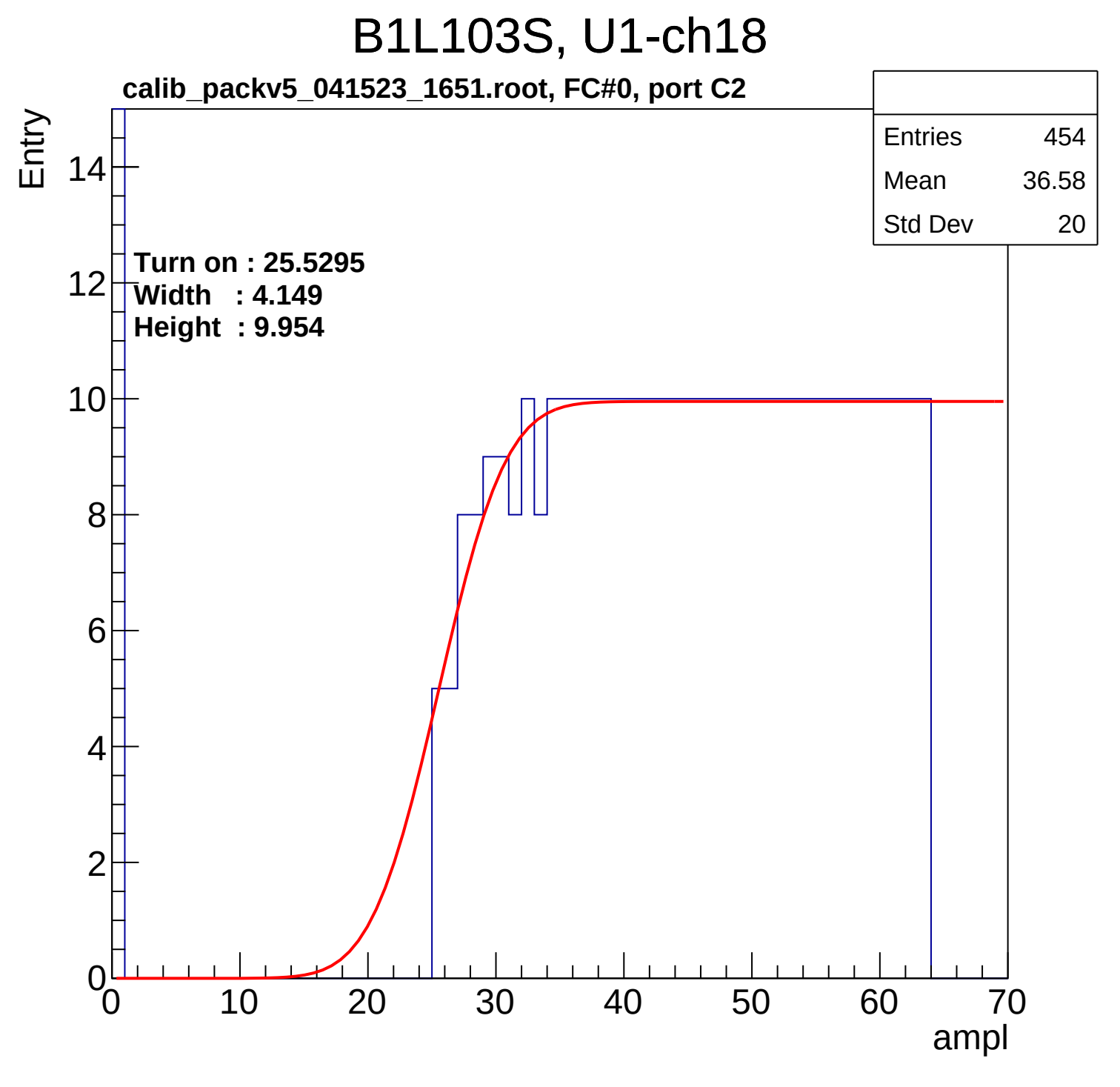
B1L103S, U1-ch18
calib_packv5_041523_1651.root, FC#0, port C2
Entries 454
Mean 36.58
Std Dev 20
Turn on : 25.5295
Width : 4.149
Height : 9.954
Entry
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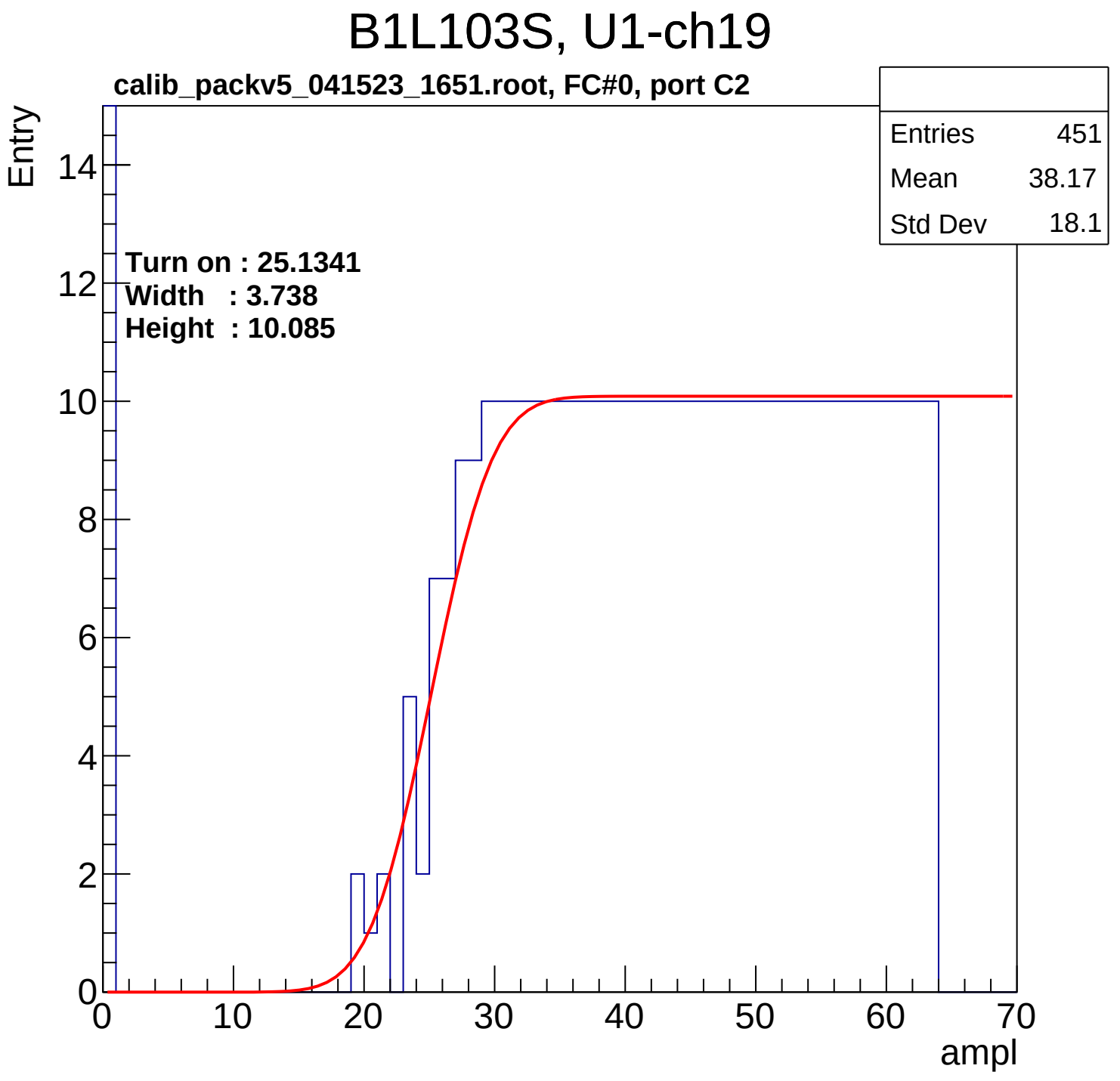
B1L103S, U1-ch19
calib_packv5_041523_1651.root, FC#0, port C2
Entries 451
Mean 38.17
Std Dev 18.1
Turn on : 25.1341
Width : 3.738
Height : 10.085
Entry
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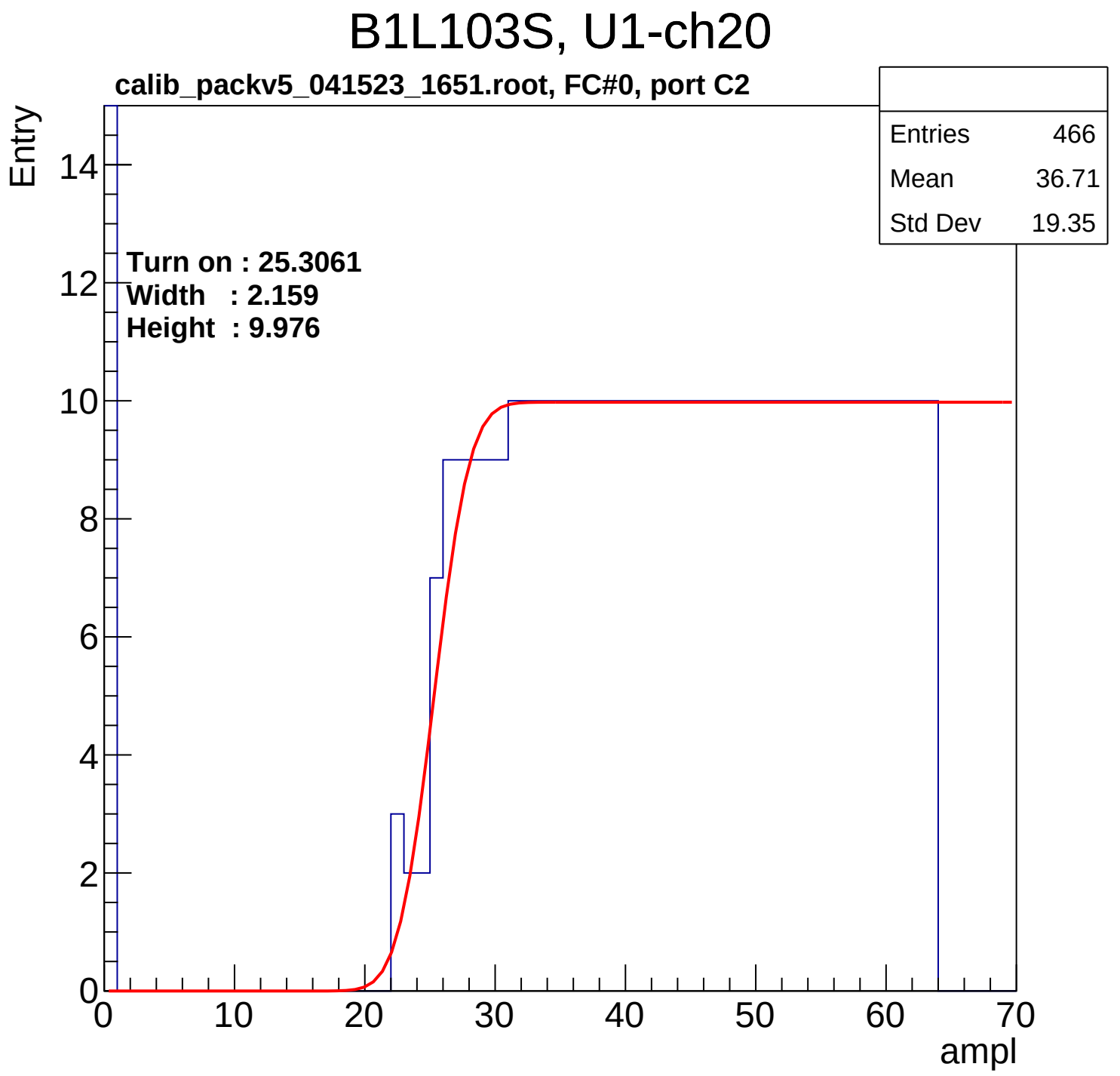
B1L103S, U1-ch20
calib_packv5_041523_1651.root, FC#0, port C2
Entries 466
Mean 36.71
Std Dev 19.35
Turn on : 25.3061
Width : 2.159
Height : 9.976
Entry
ampl
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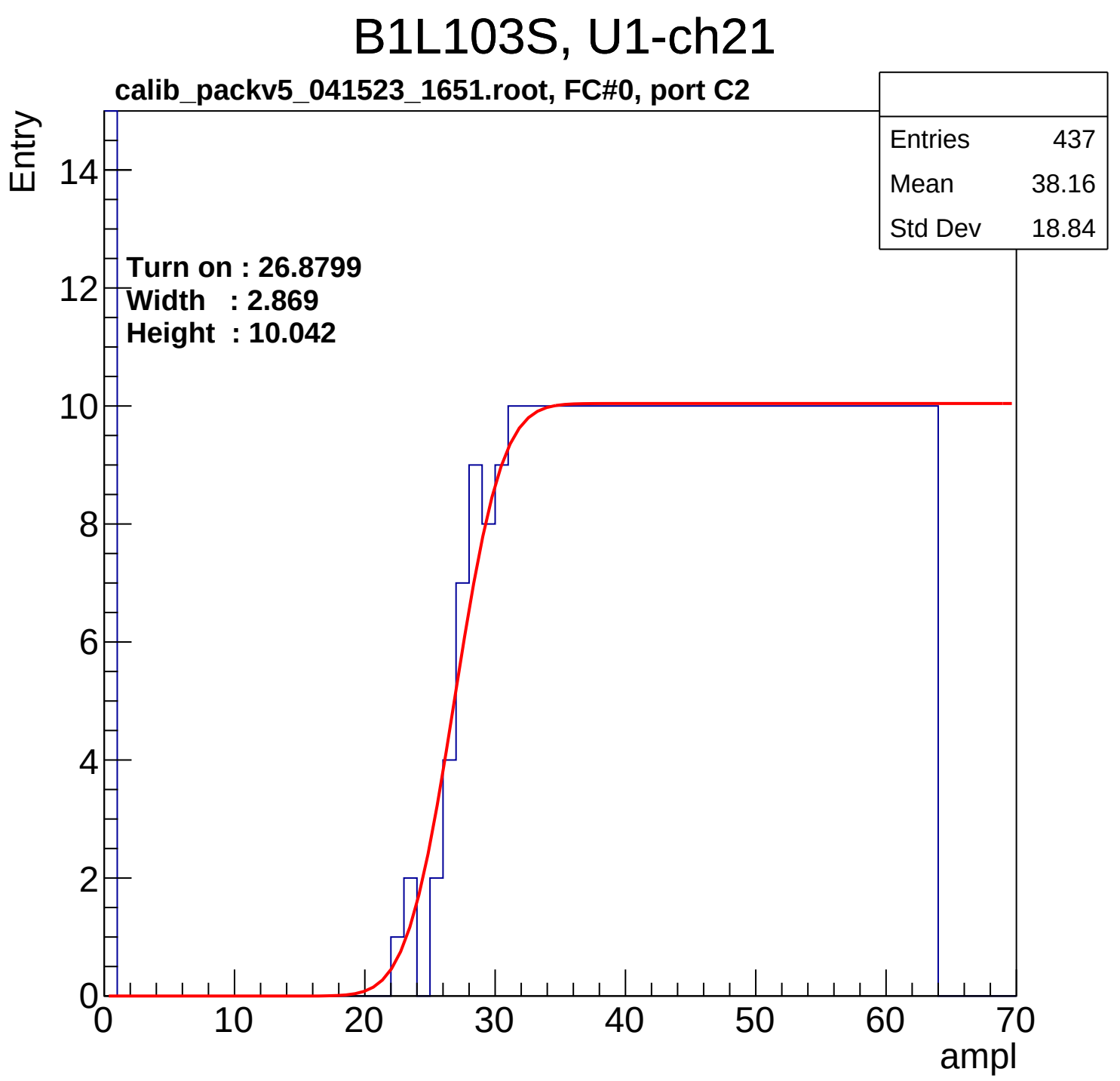
B1L103S, U1-ch21
calib_packv5_041523_1651.root, FC#0, port C2
Entries 437
Mean 38.16
Std Dev 18.84
Turn on : 26.8799
Width : 2.869
Height : 10.042
Entry
ampl
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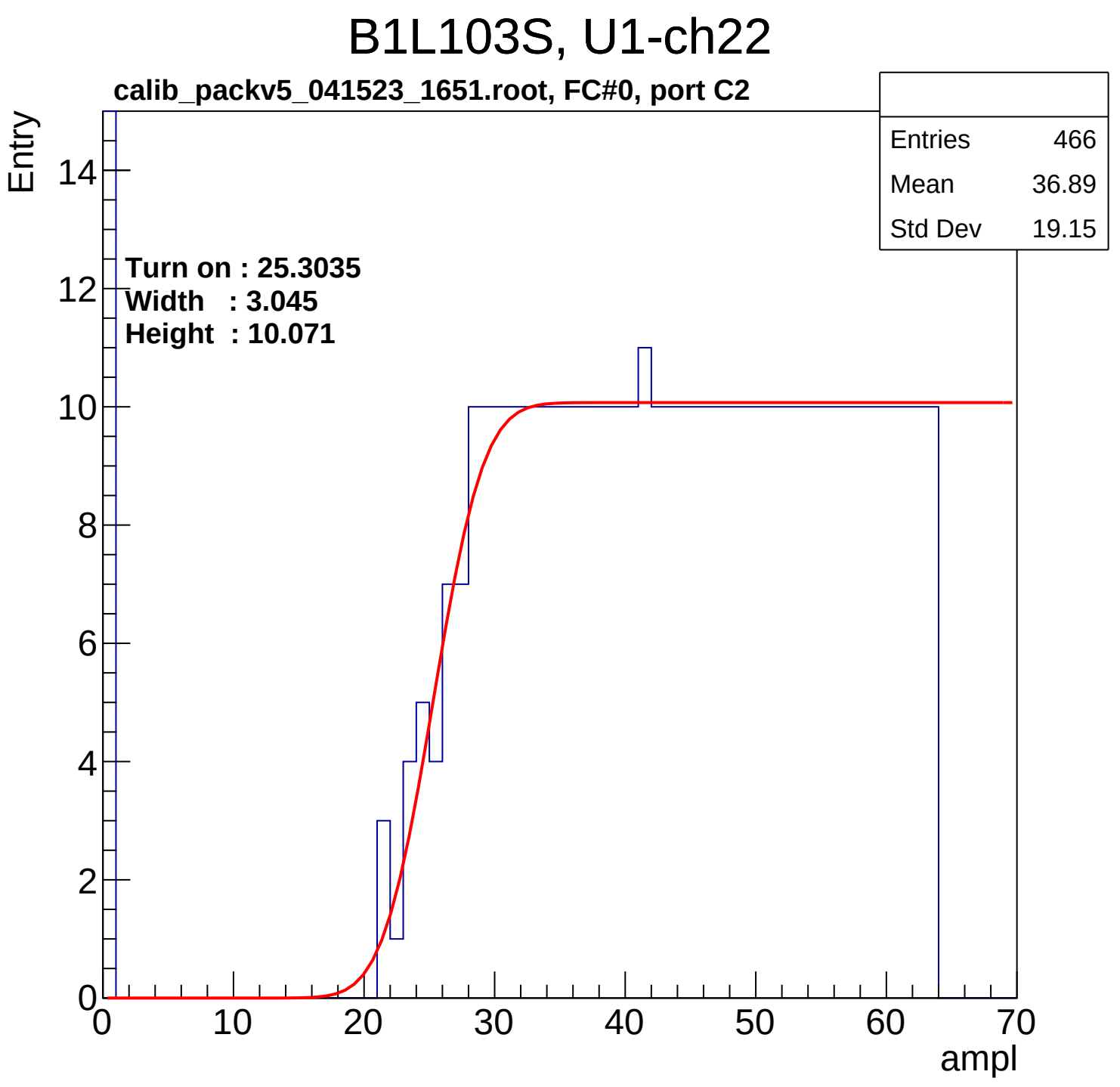
B1L103S, U1-ch22
calib_packv5_041523_1651.root, FC#0, port C2
Entries 466
Mean 36.89
Std Dev 19.15
Turn on : 25.3035
Width : 3.045
Height : 10.071
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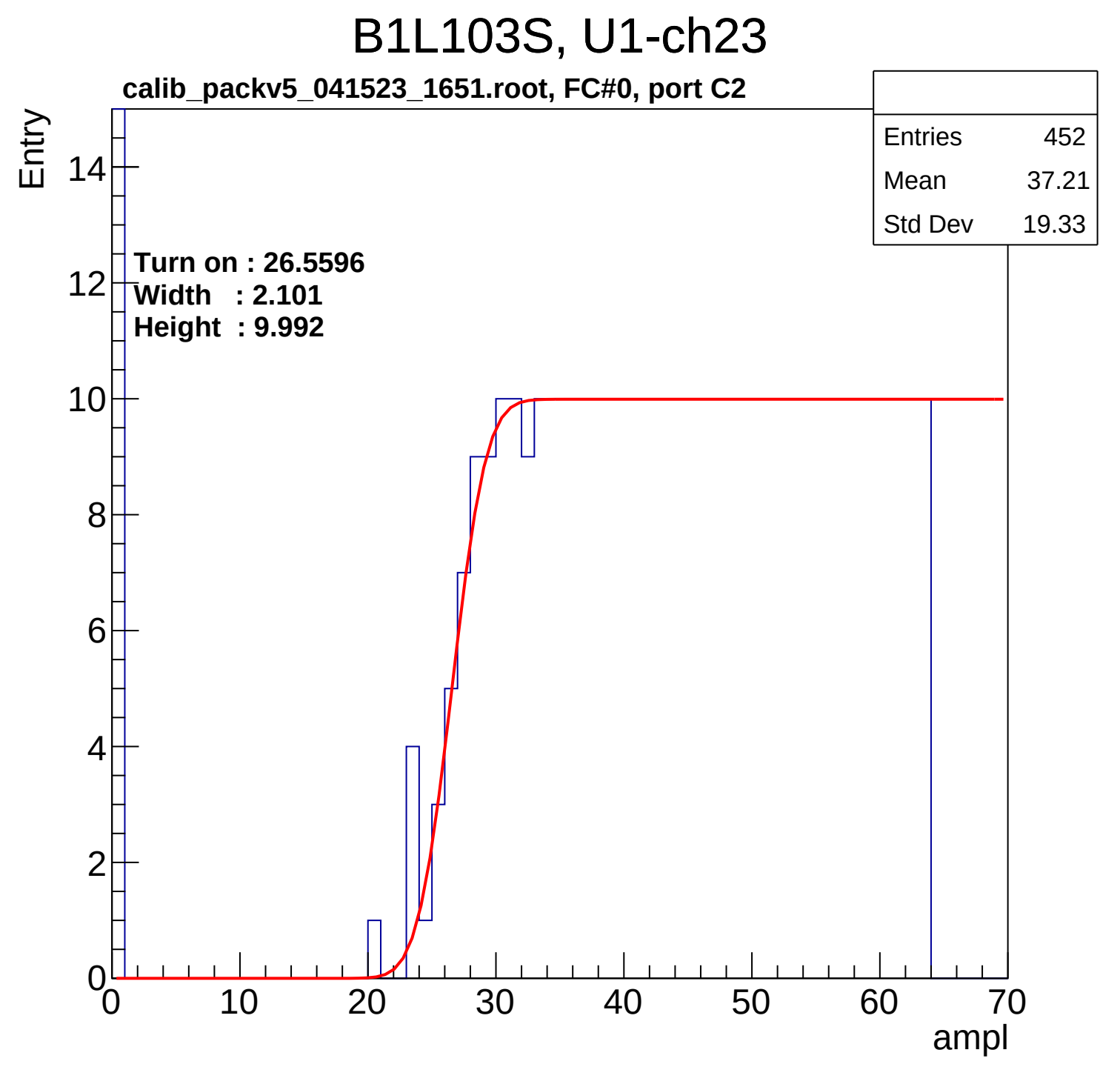
B1L103S, U1-ch23
calib_packv5_041523_1651.root, FC#0, port C2
Entries 452
Mean 37.21
Std Dev 19.33
Turn on : 26.5596
Width : 2.101
Height : 9.992
Entry
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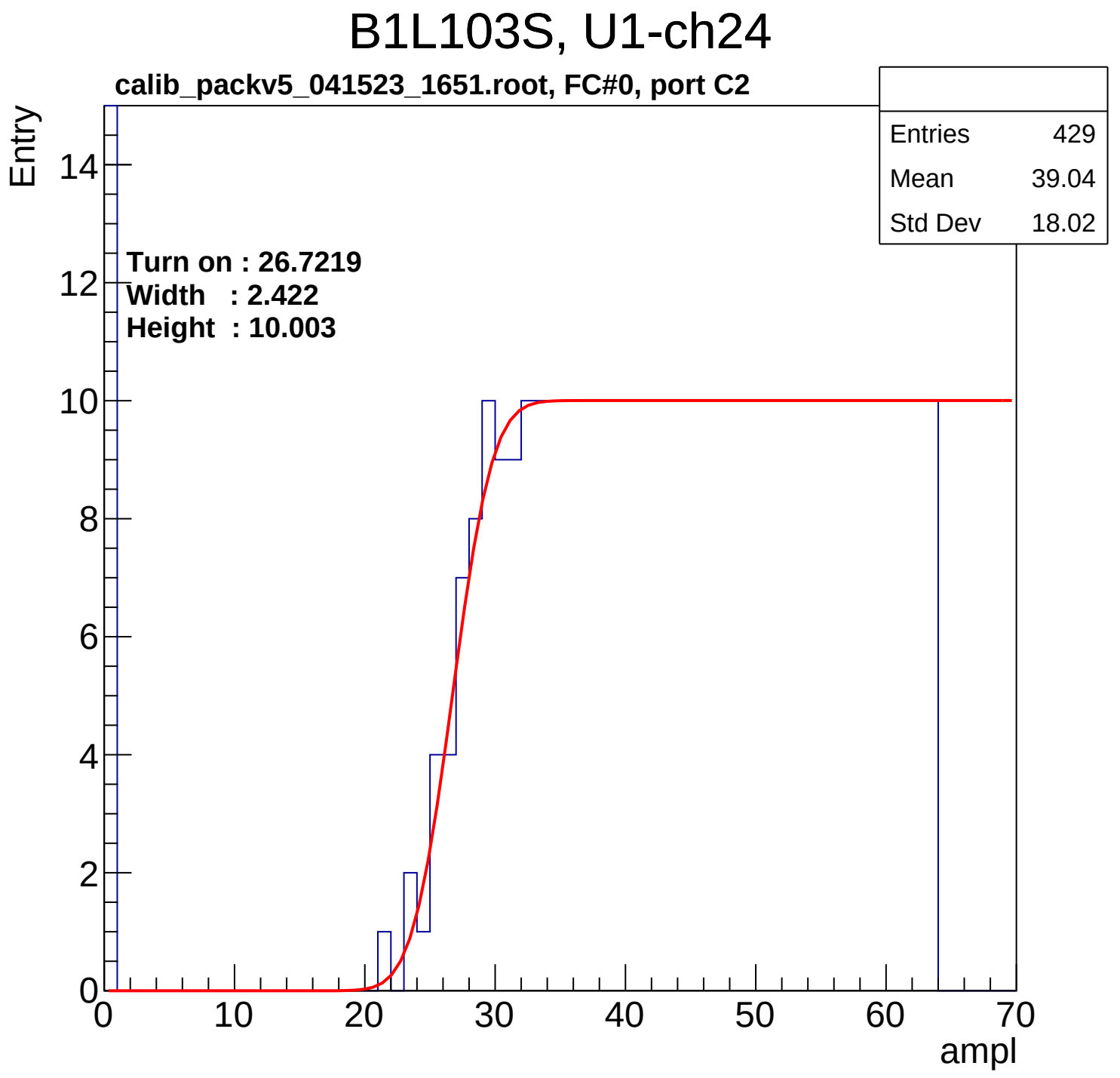
B1L103S, U1-ch24
calib_packv5_041523_1651.root, FC#0, port C2
Entries 429
Mean 39.04
Std Dev 18.02
Turn on : 26.7219
Width : 2.422
Height : 10.003
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ampl
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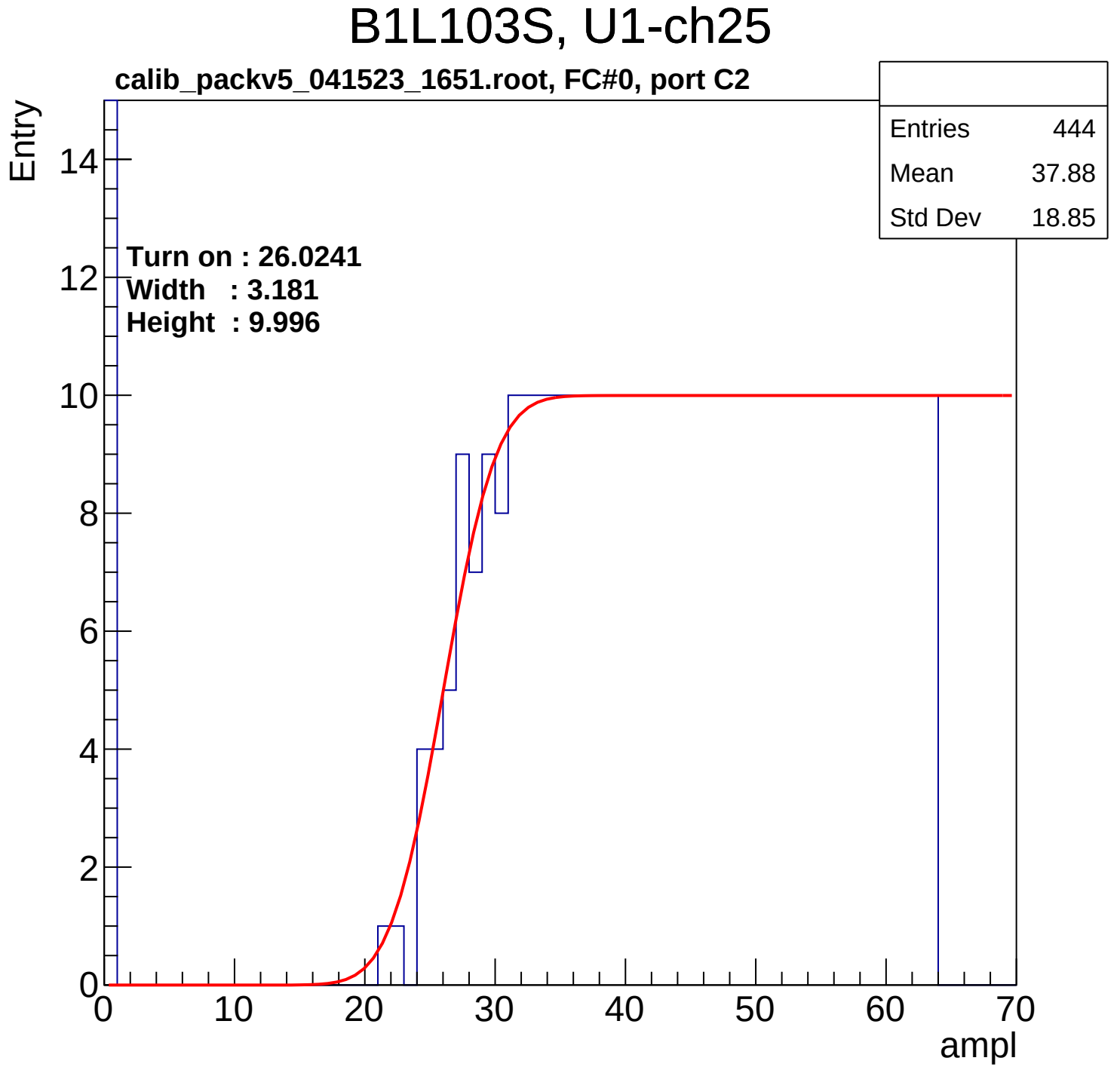
B1L103S, U1-ch25
calib_packv5_041523_1651.root, FC#0, port C2
Entries 444
Mean 37.88
Std Dev 18.85
Turn on : 26.0241
Width : 3.181
Height : 9.996
Entry
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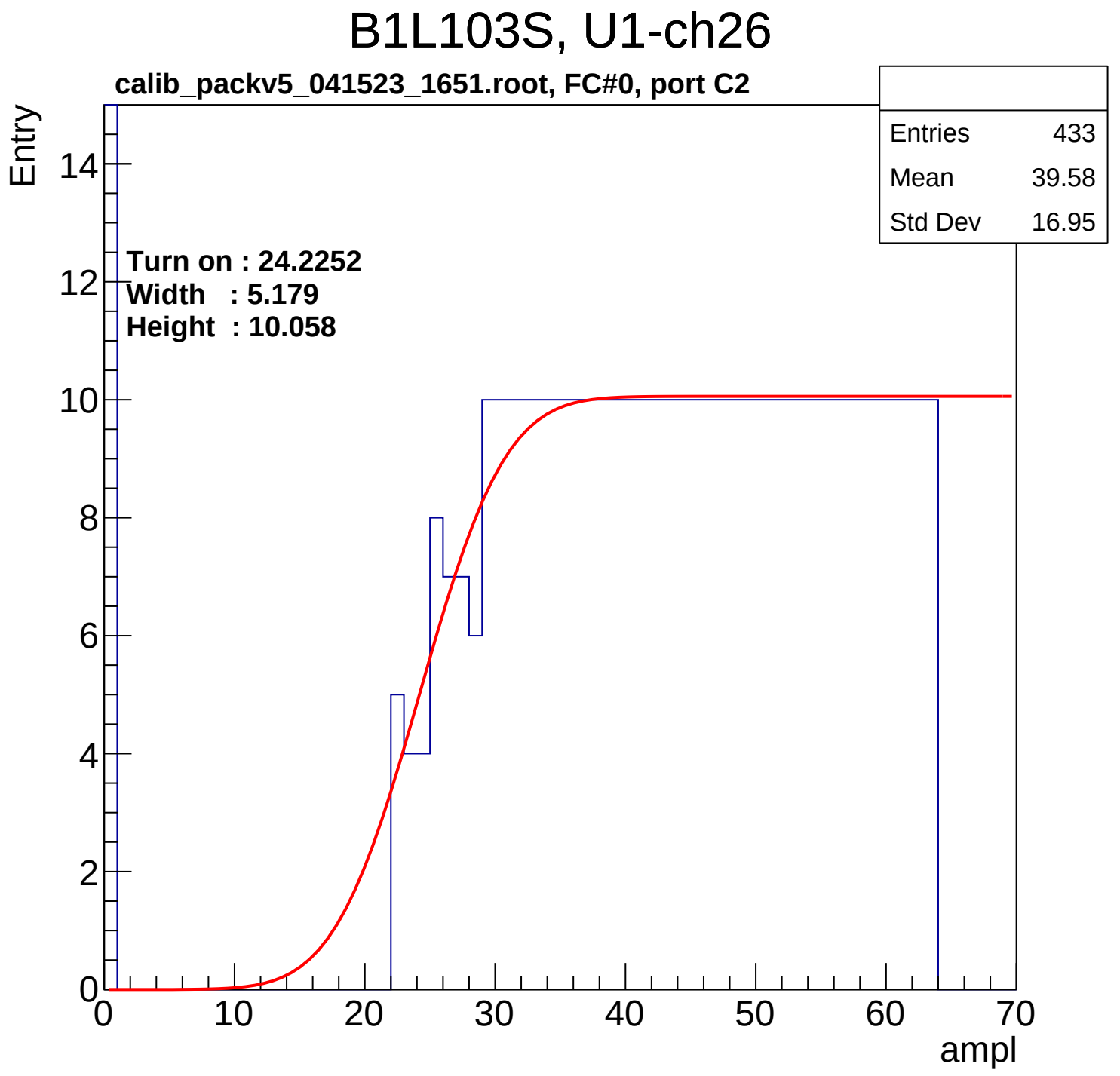
B1L103S, U1-ch26
calib_packv5_041523_1651.root, FC#0, port C2
Entries 433
Mean 39.58
Std Dev 16.95
Turn on : 24.2252
Width : 5.179
Height : 10.058
Entry
ampl
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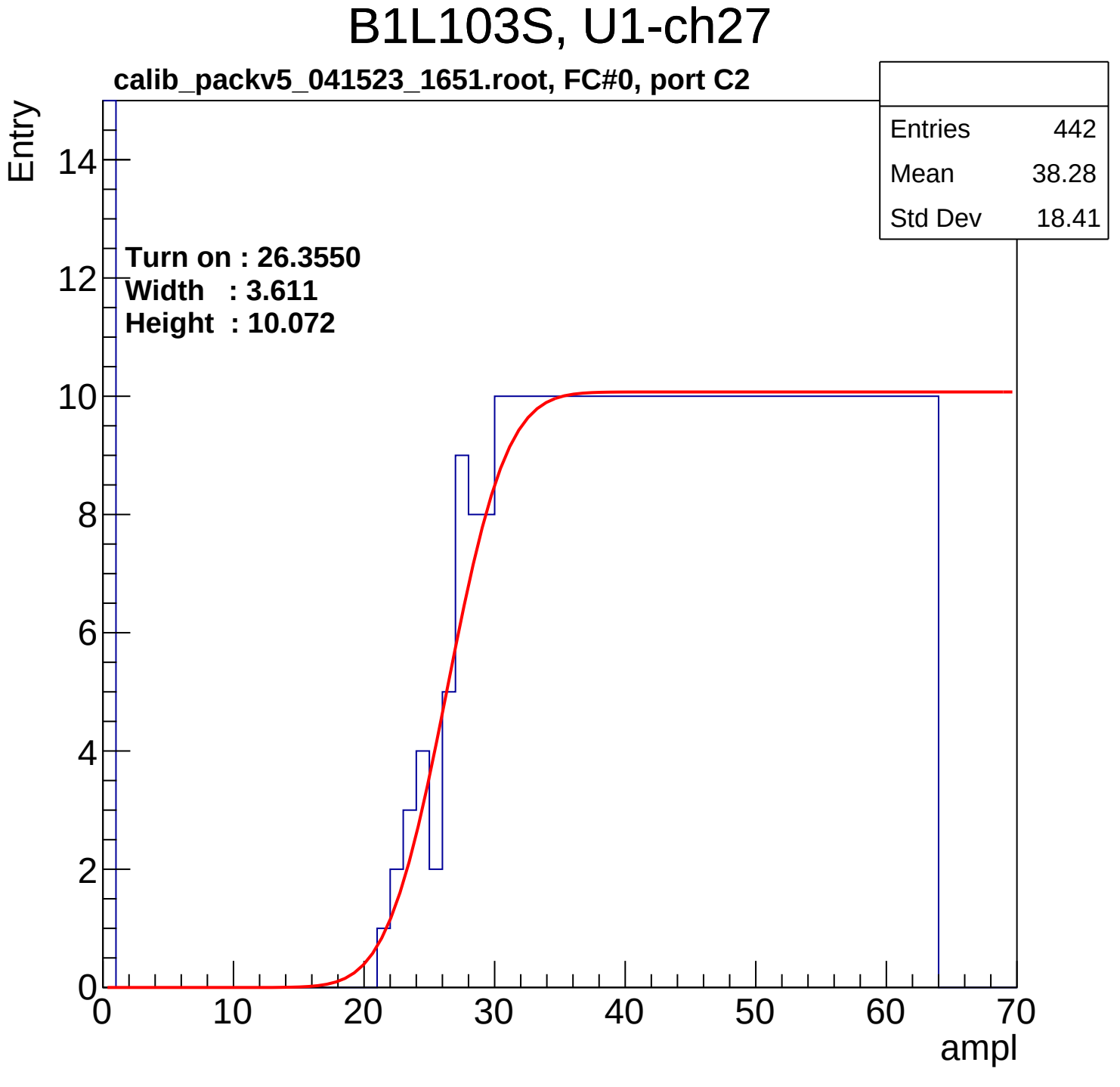
B1L103S, U1-ch27
calib_packv5_041523_1651.root, FC#0, port C2
Entries 442
Mean 38.28
Std Dev 18.41
Turn on : 26.3550
Width : 3.611
Height : 10.072
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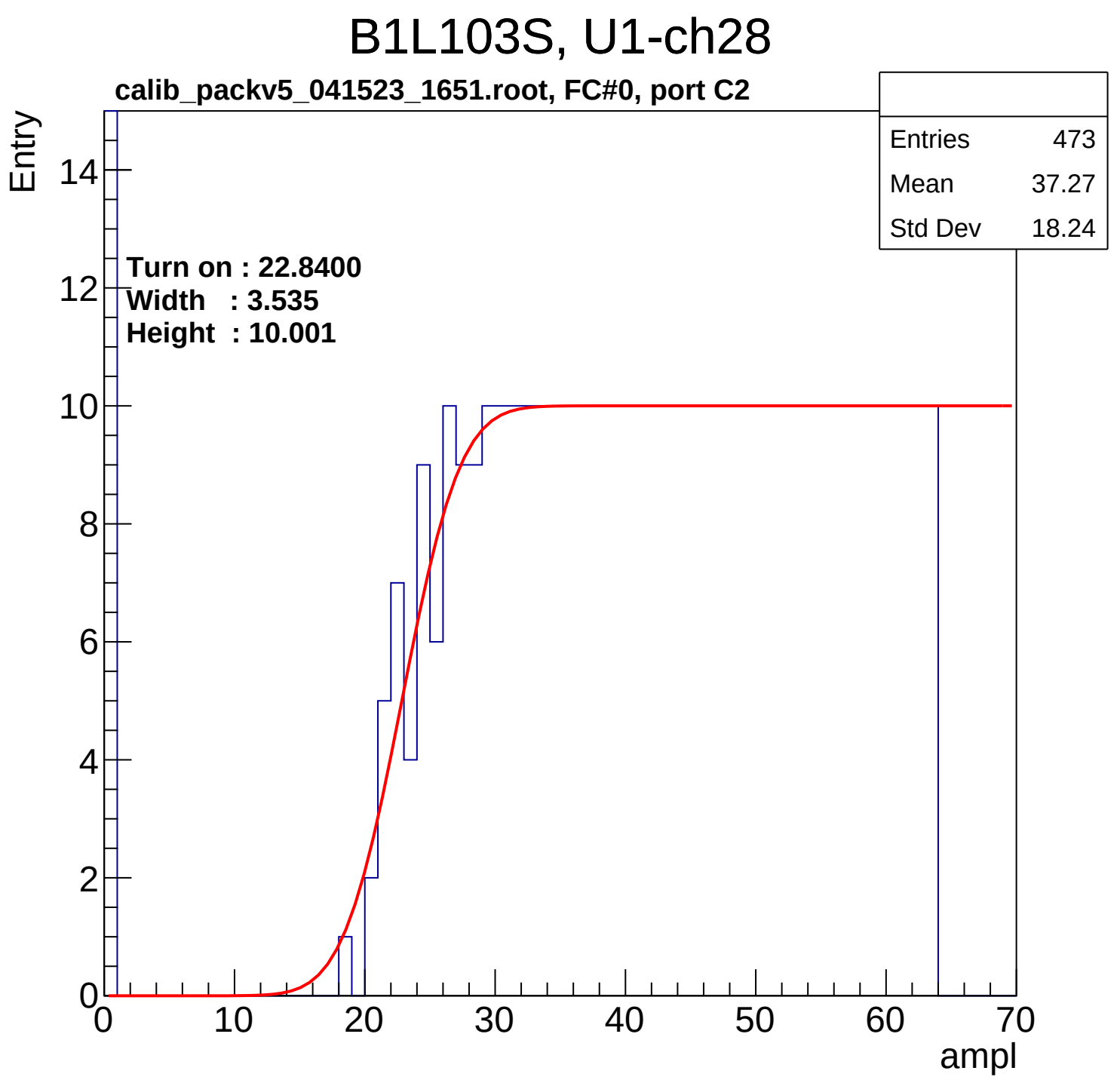
B1L103S, U1-ch28
calib_packv5_041523_1651.root, FC#0, port C2
Entries 473
Mean 37.27
Std Dev 18.24
Turn on : 22.8400
Width : 3.535
Height : 10.001
Entry
ampl
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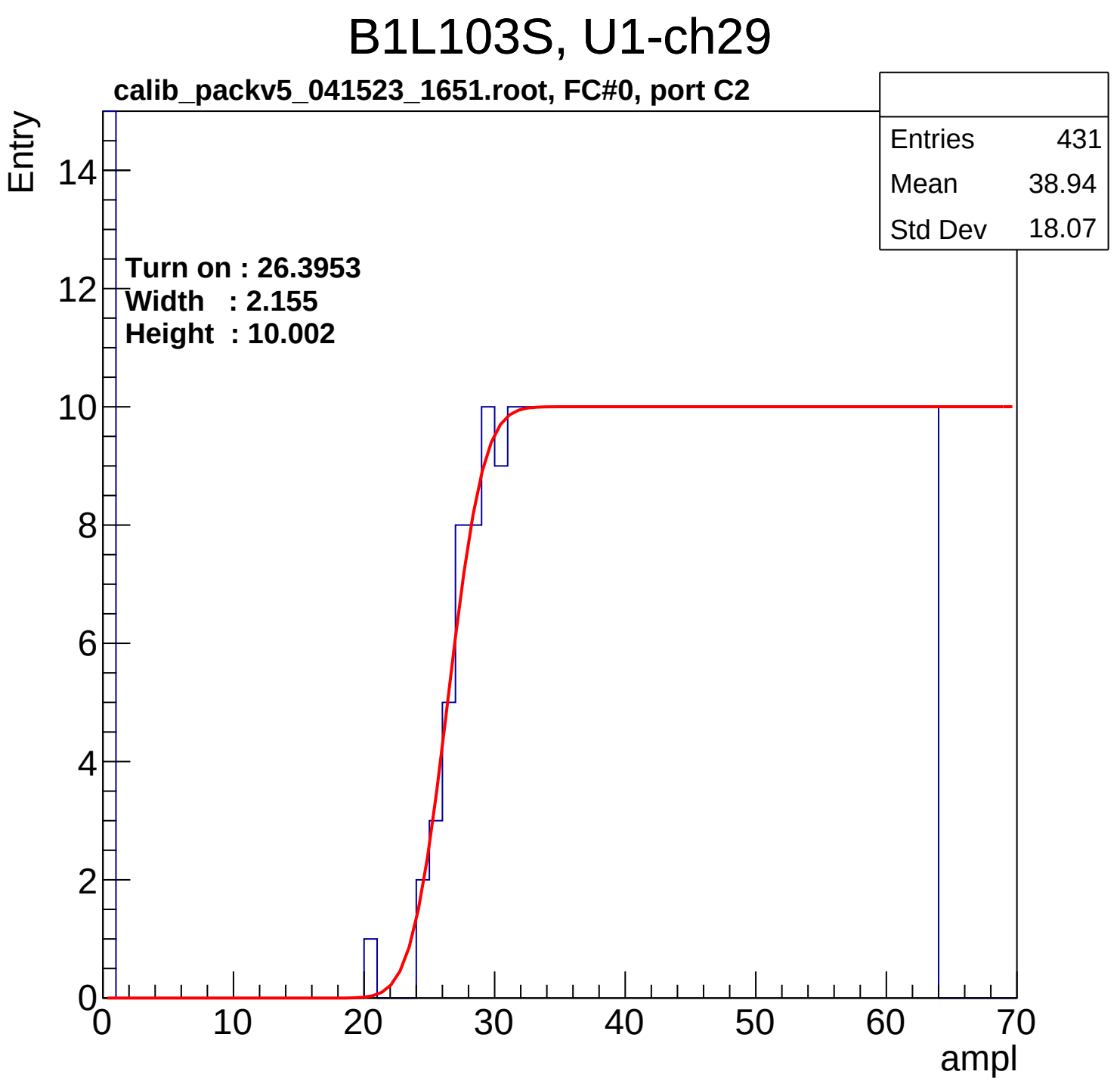
B1L103S, U1-ch29
calib_packv5_041523_1651.root, FC#0, port C2
Entries 431
Mean 38.94
Std Dev 18.07
Turn on : 26.3953
Width : 2.155
Height : 10.002
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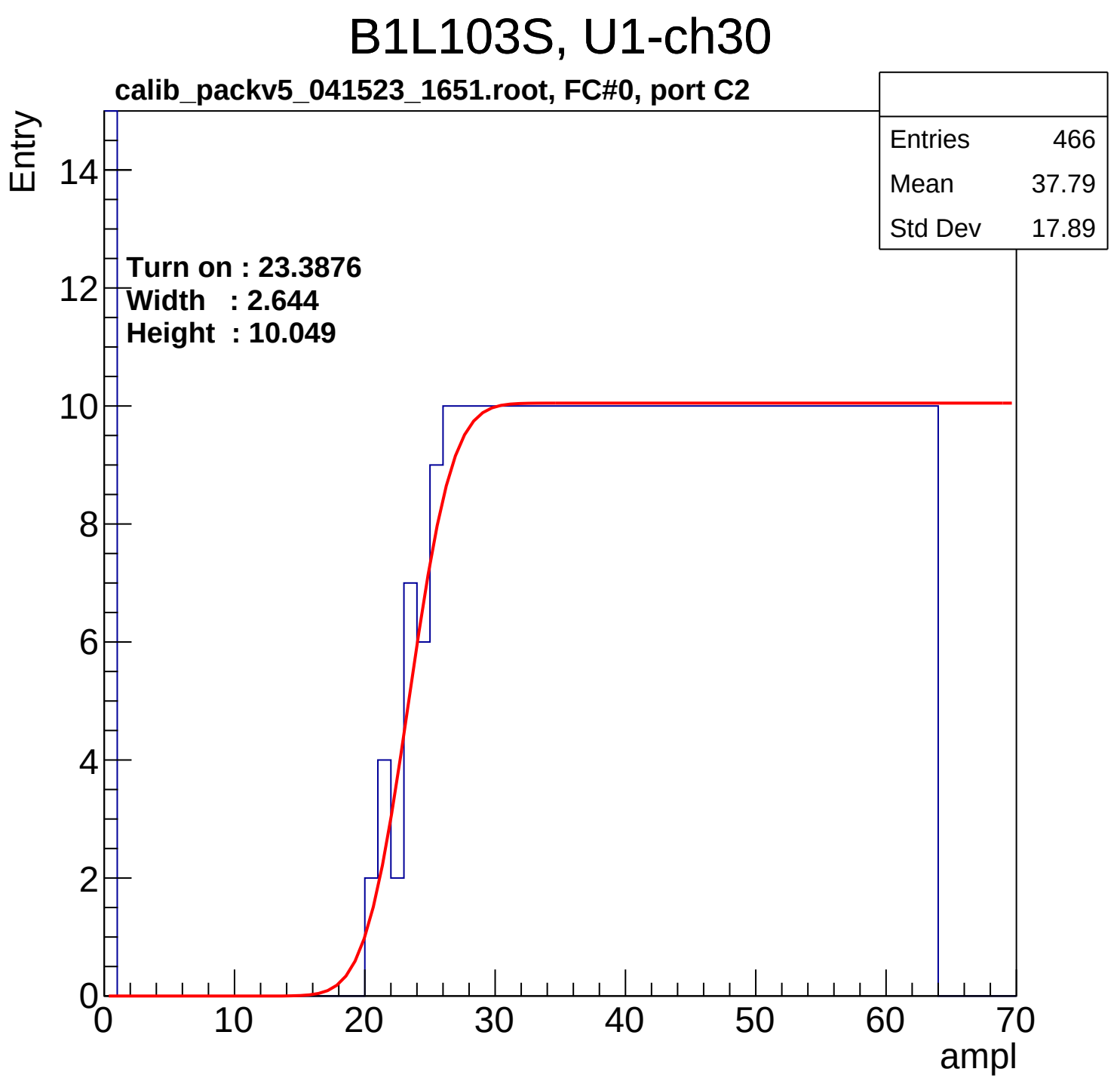
B1L103S, U1-ch30
calib_packv5_041523_1651.root, FC#0, port C2
Entries 466
Mean 37.79
Std Dev 17.89
Turn on : 23.3876
Width : 2.644
Height : 10.049
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ampl
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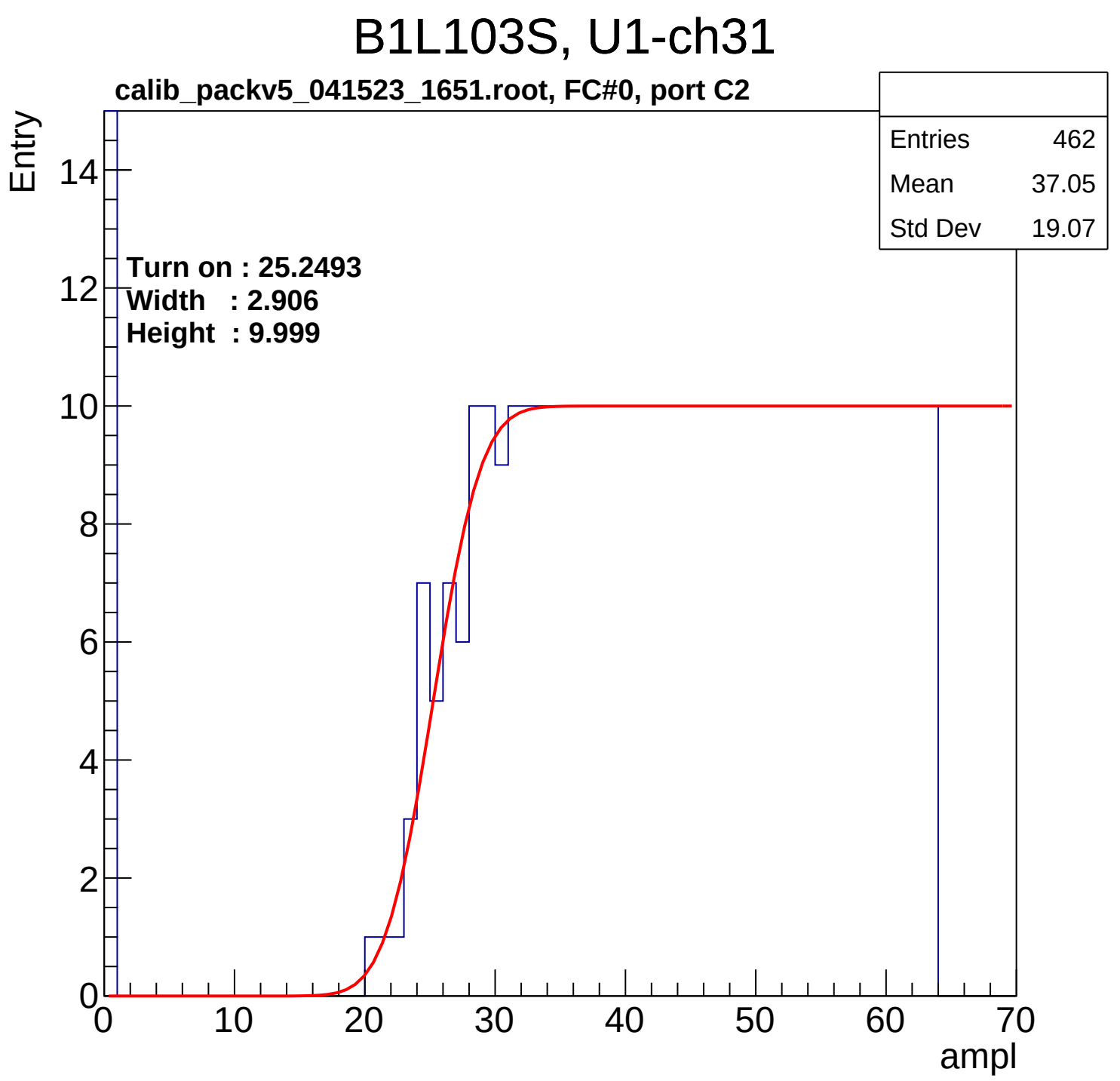
B1L103S, U1-ch31
calib_packv5_041523_1651.root, FC#0, port C2
Entries 462
Mean 37.05
Std Dev 19.07
Turn on : 25.2493
Width : 2.906
Height : 9.999
Entry
ampl
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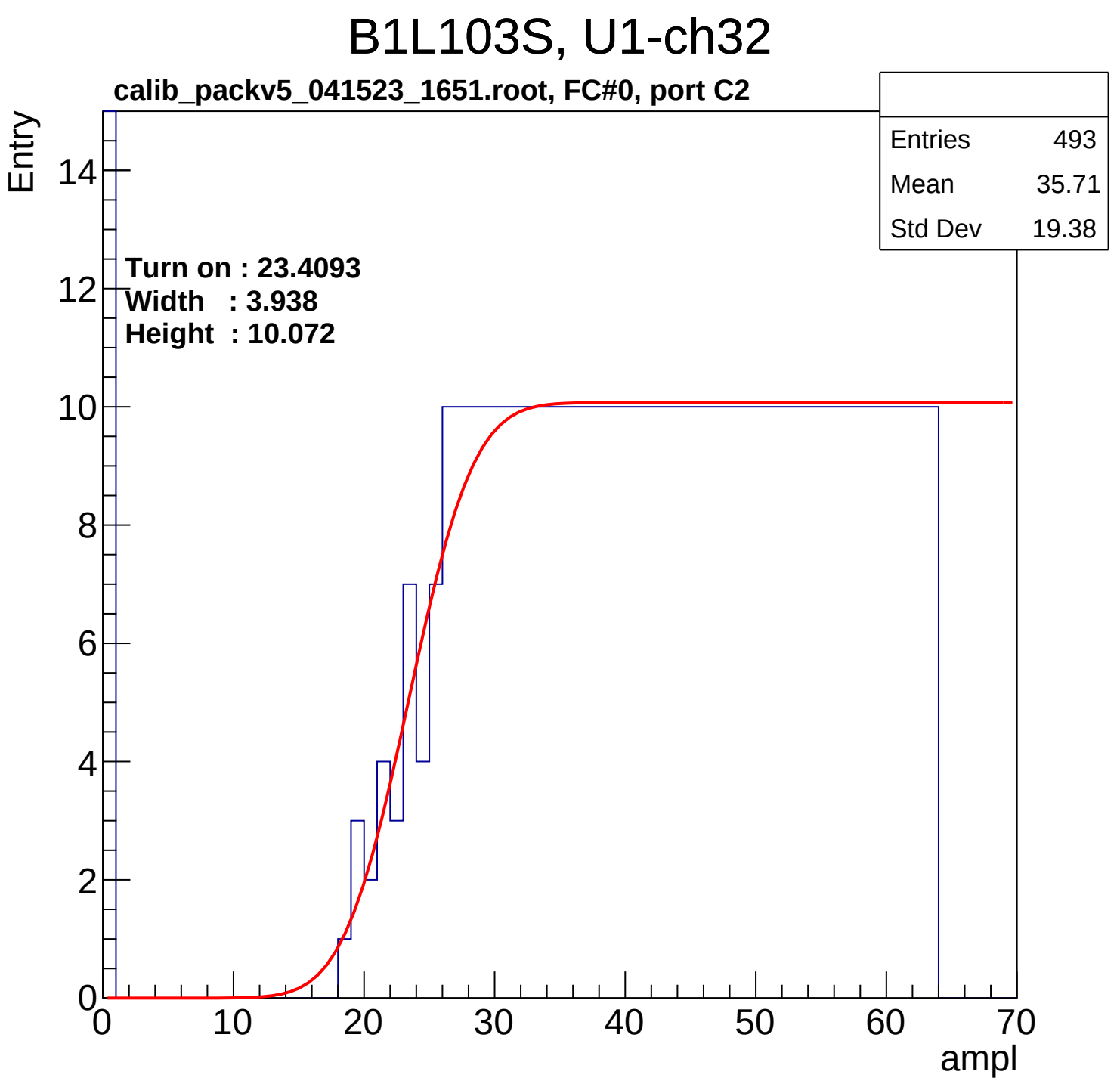
B1L103S, U1-ch32
calib_packv5_041523_1651.root, FC#0, port C2
Entries 493
Mean 35.71
Std Dev 19.38
Turn on : 23.4093
Width : 3.938
Height : 10.072
Entry
ampl
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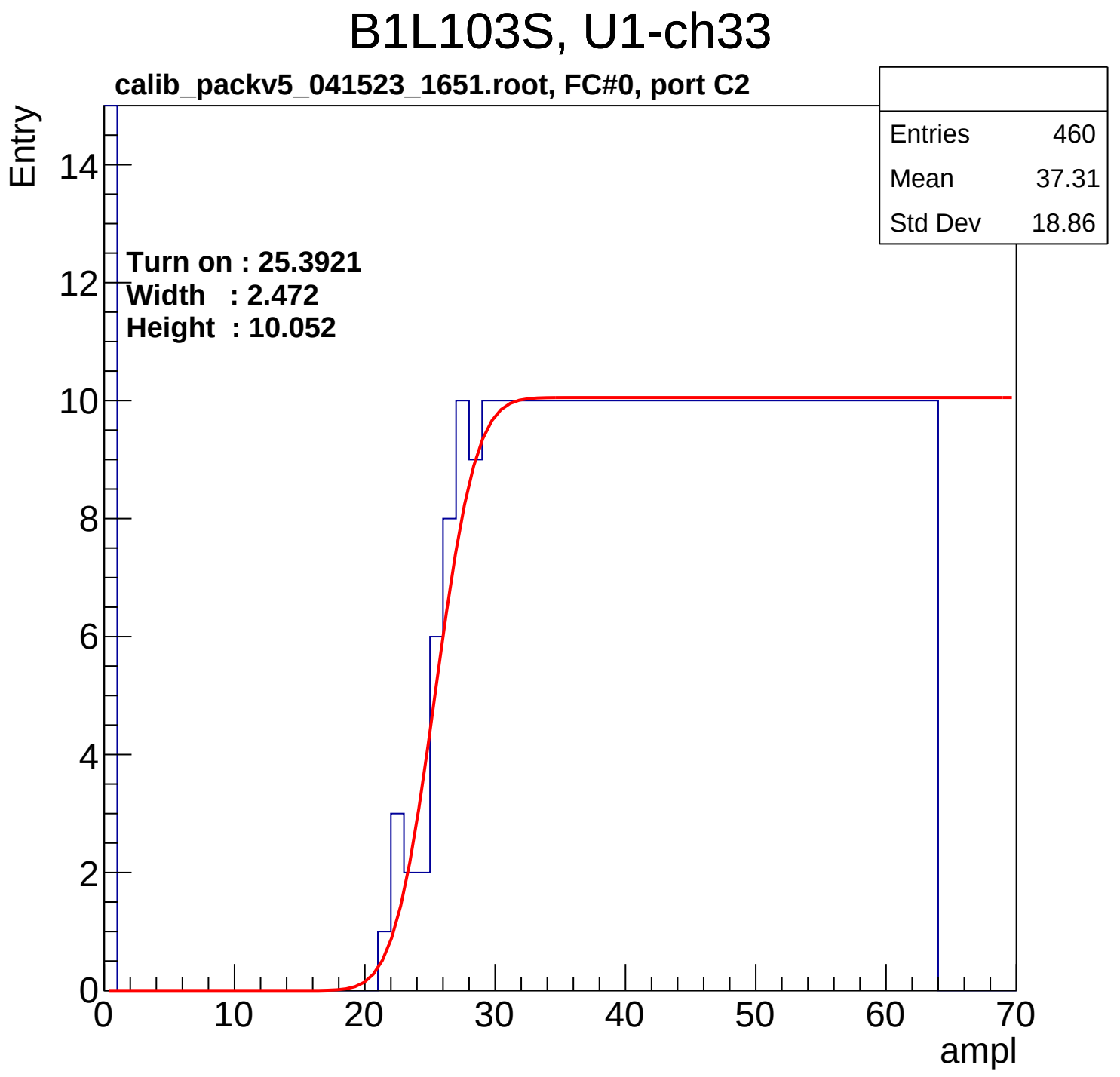
B1L103S, U1-ch33
calib_packv5_041523_1651.root, FC#0, port C2
Entries 460
Mean 37.31
Std Dev 18.86
Turn on : 25.3921
Width : 2.472
Height : 10.052
Entry
ampl
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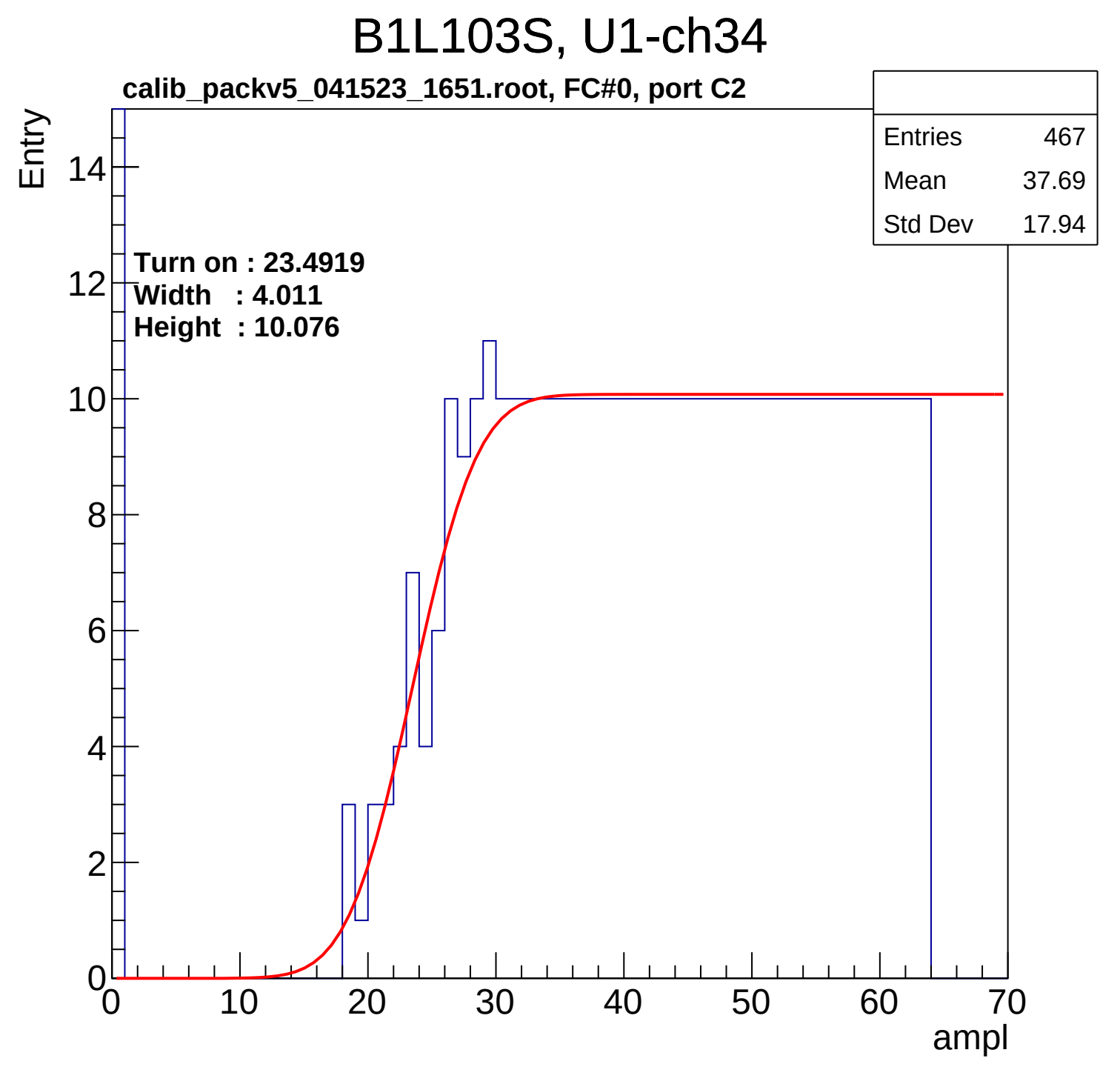
B1L103S, U1-ch34
calib_packv5_041523_1651.root, FC#0, port C2
Entries 467
Mean 37.69
Std Dev 17.94
Turn on : 23.4919
Width : 4.011
Height : 10.076
Entry
ampl
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2
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6
8
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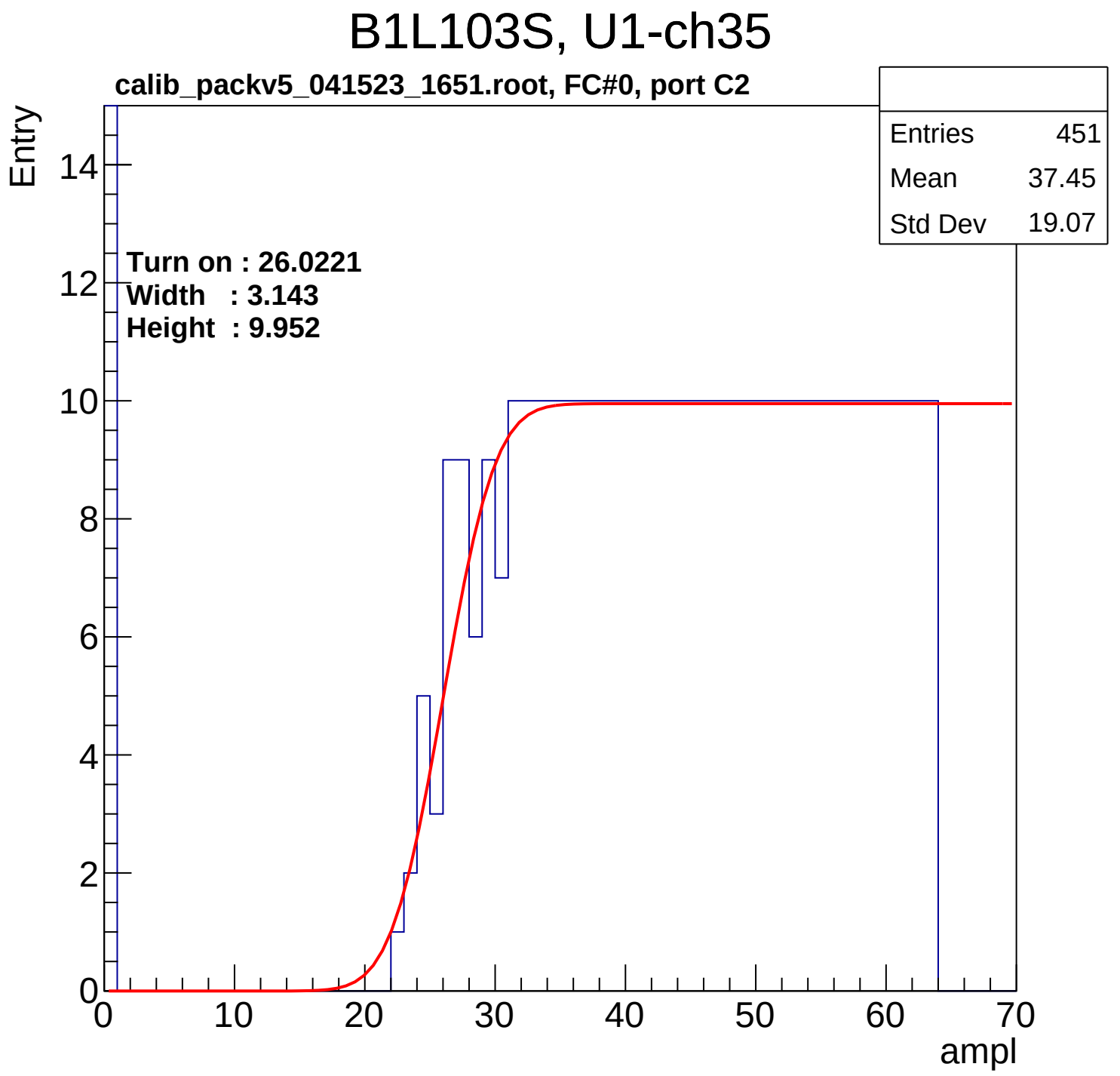
B1L103S, U1-ch35
calib_packv5_041523_1651.root, FC#0, port C2
Entries 451
Mean 37.45
Std Dev 19.07
Turn on : 26.0221
Width : 3.143
Height : 9.952
Entry
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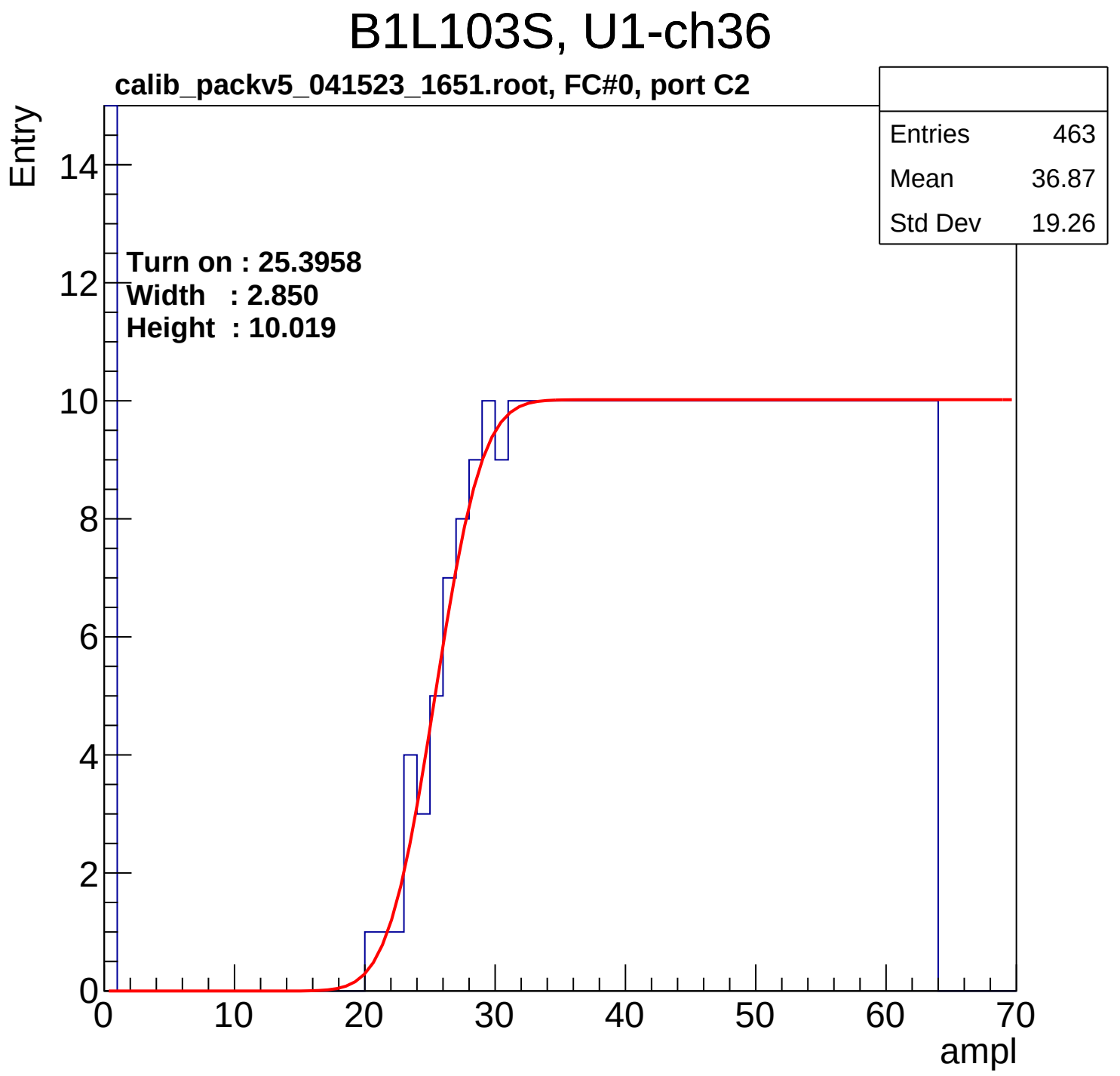
B1L103S, U1-ch36
calib_packv5_041523_1651.root, FC#0, port C2
Entries 463
Mean 36.87
Std Dev 19.26
Turn on : 25.3958
Width : 2.850
Height : 10.019
Entry
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6
8
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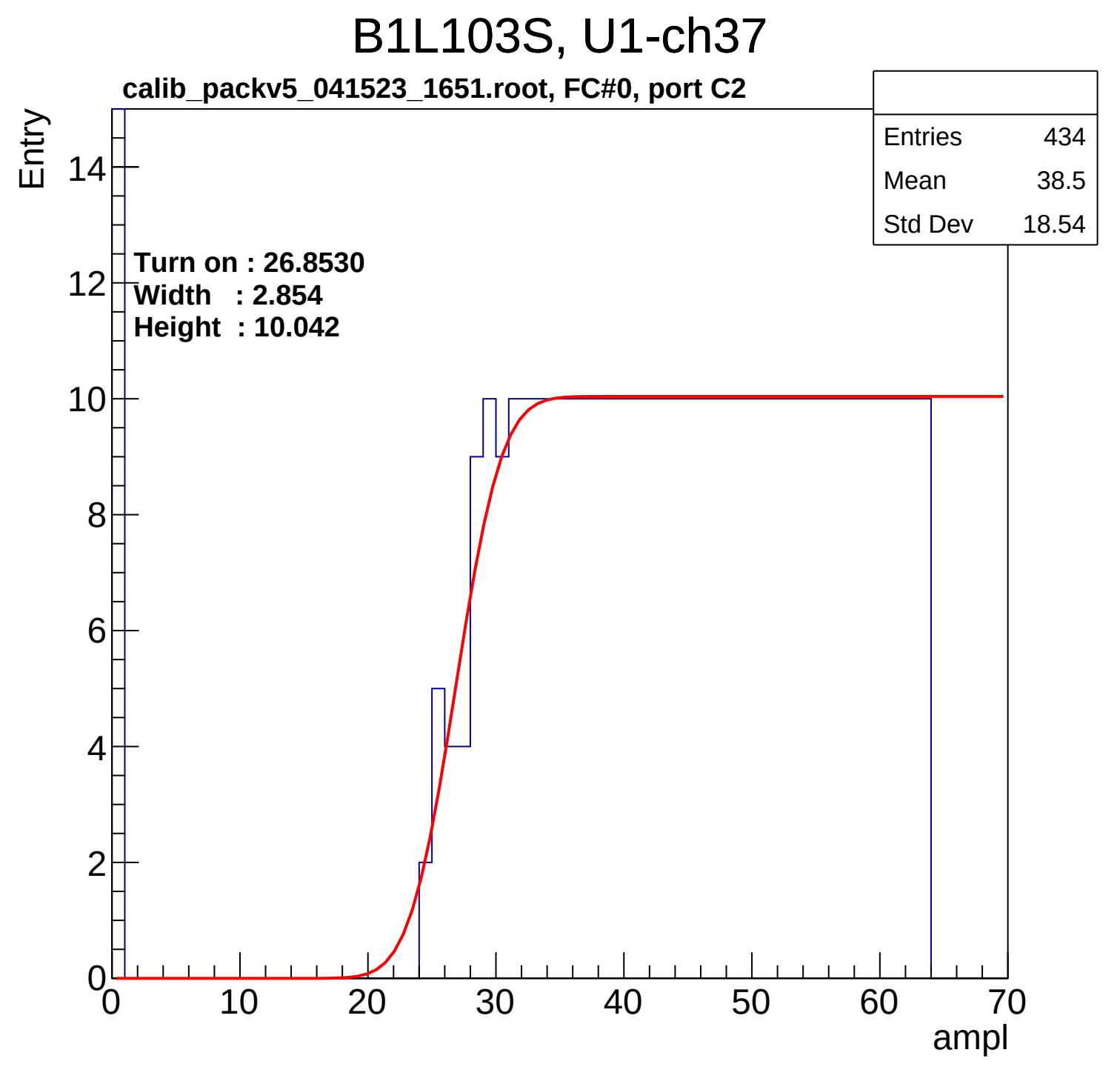
B1L103S, U1-ch37
calib_packv5_041523_1651.root, FC#0, port C2
Entries 434
Mean 38.5
Std Dev 18.54
Turn on : 26.8530
Width : 2.854
Height : 10.042
Entry
ampl
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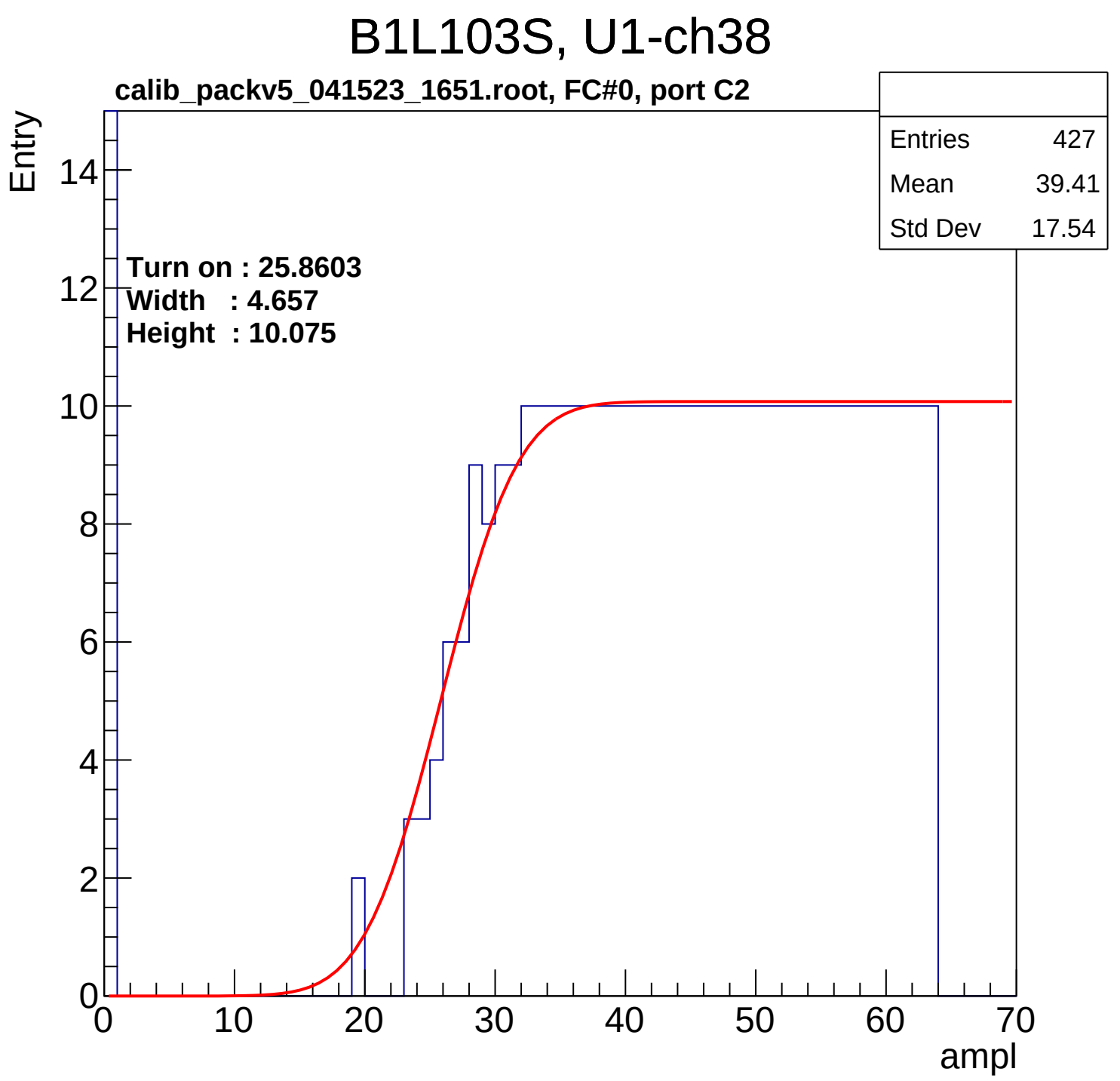
B1L103S, U1-ch38
calib_packv5_041523_1651.root, FC#0, port C2
Entries 427
Mean 39.41
Std Dev 17.54
Turn on : 25.8603
Width : 4.657
Height : 10.075
Entry
ampl
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6
8
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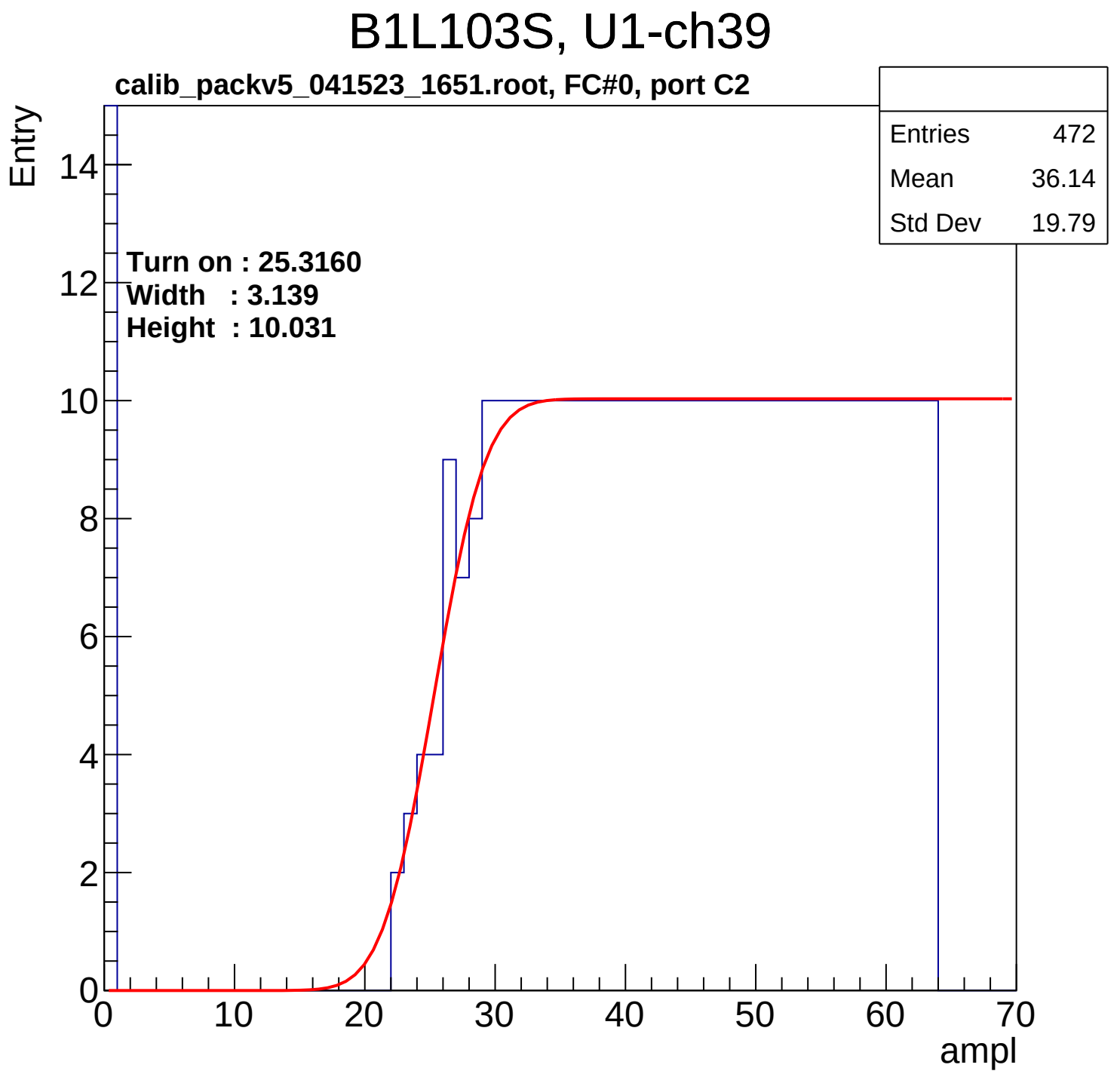
B1L103S, U1-ch39
calib_packv5_041523_1651.root, FC#0, port C2
Entries 472
Mean 36.14
Std Dev 19.79
Turn on : 25.3160
Width : 3.139
Height : 10.031
Entry
ampl
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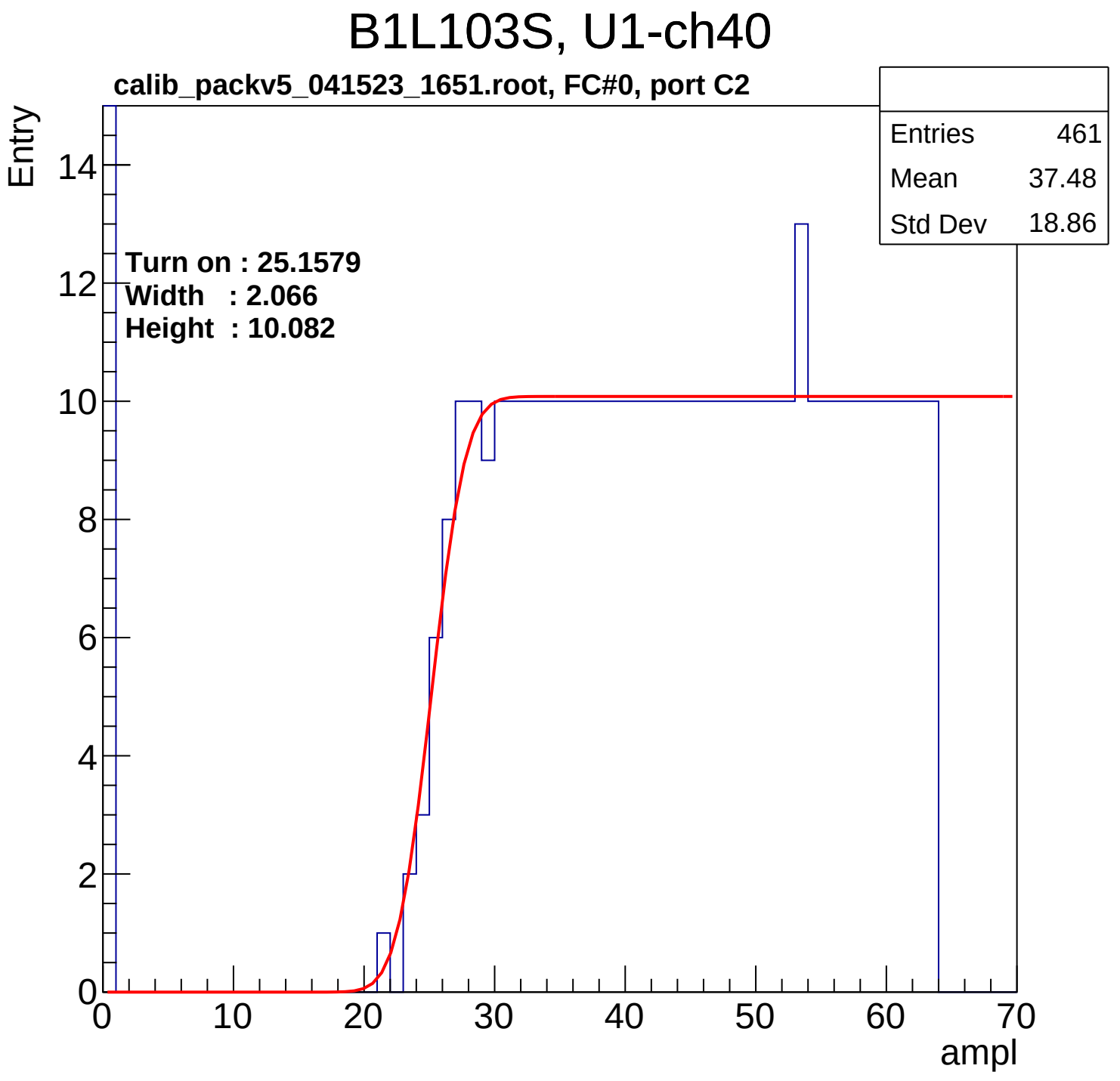
B1L103S, U1-ch40
calib_packv5_041523_1651.root, FC#0, port C2
Entries 461
Mean 37.48
Std Dev 18.86
Turn on : 25.1579
Width : 2.066
Height : 10.082
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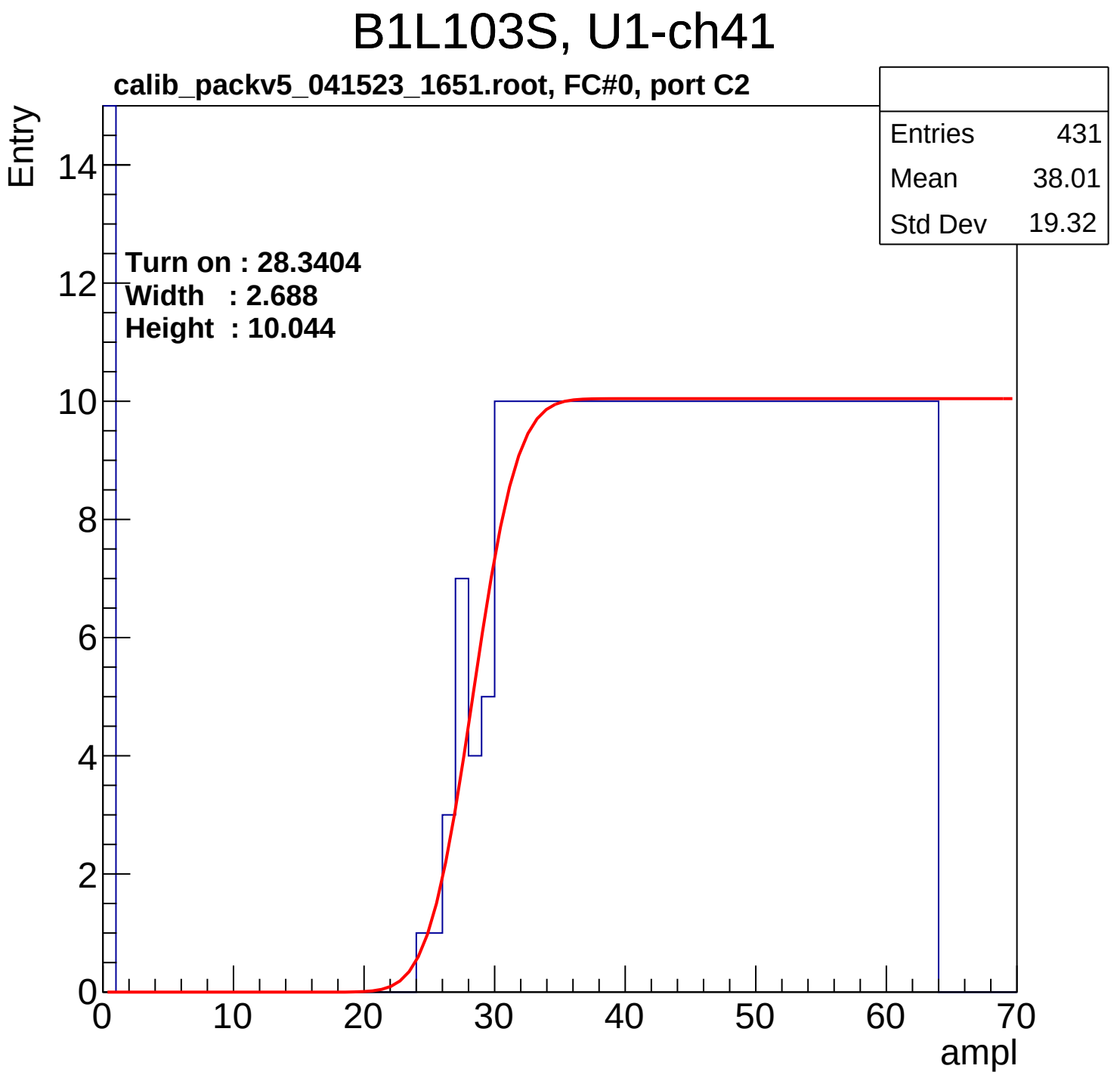
B1L103S, U1-ch41
calib_packv5_041523_1651.root, FC#0, port C2
Entries 431
Mean 38.01
Std Dev 19.32
Turn on : 28.3404
Width : 2.688
Height : 10.044
Entry
ampl
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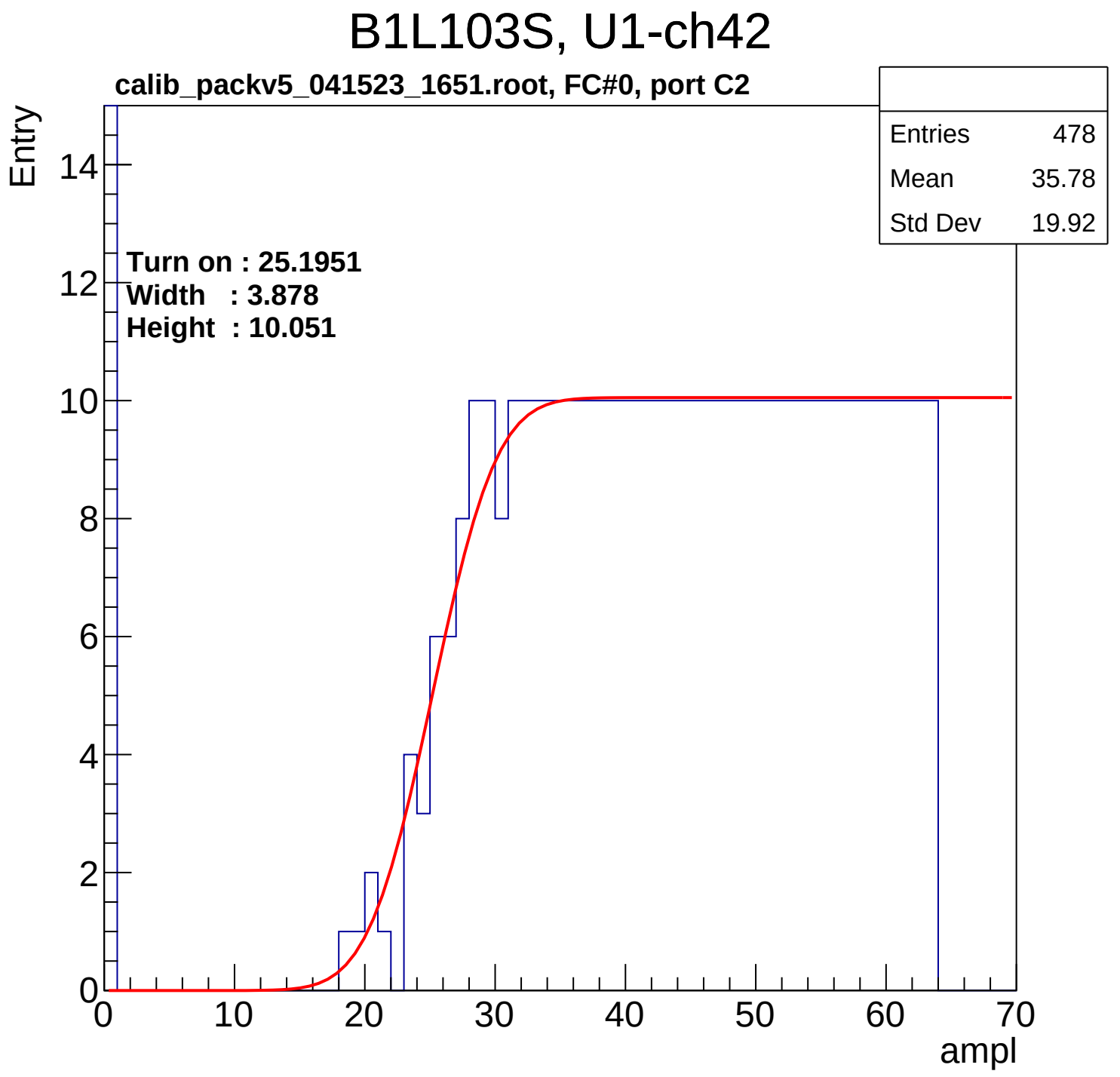
B1L103S, U1-ch42
calib_packv5_041523_1651.root, FC#0, port C2
Entries 478
Mean 35.78
Std Dev 19.92
Turn on : 25.1951
Width : 3.878
Height : 10.051
Entry
ampl
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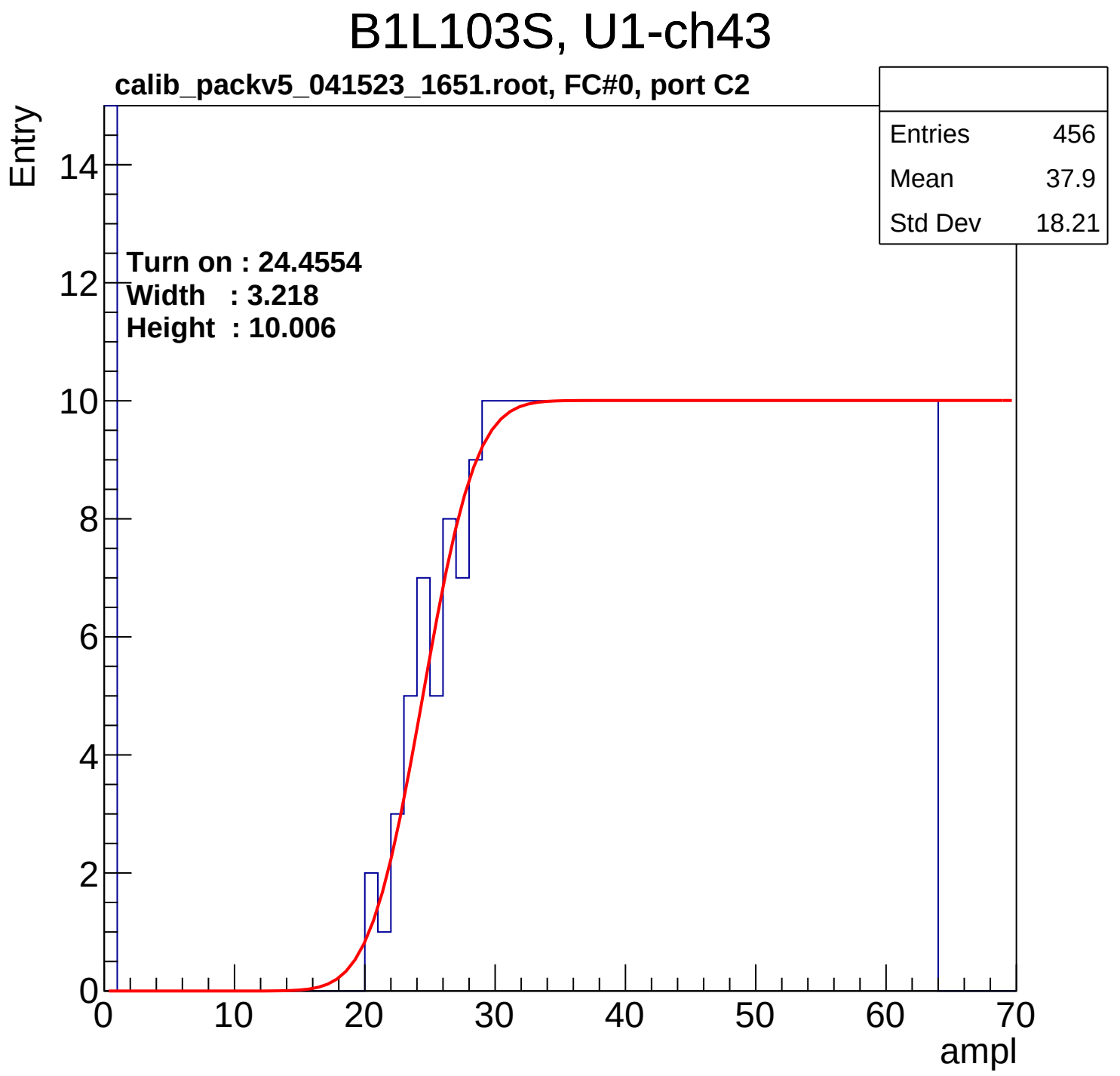
B1L103S, U1-ch43
calib_packv5_041523_1651.root, FC#0, port C2
Entries 456
Mean 37.9
Std Dev 18.21
Turn on : 24.4554
Width : 3.218
Height : 10.006
Entry
ampl
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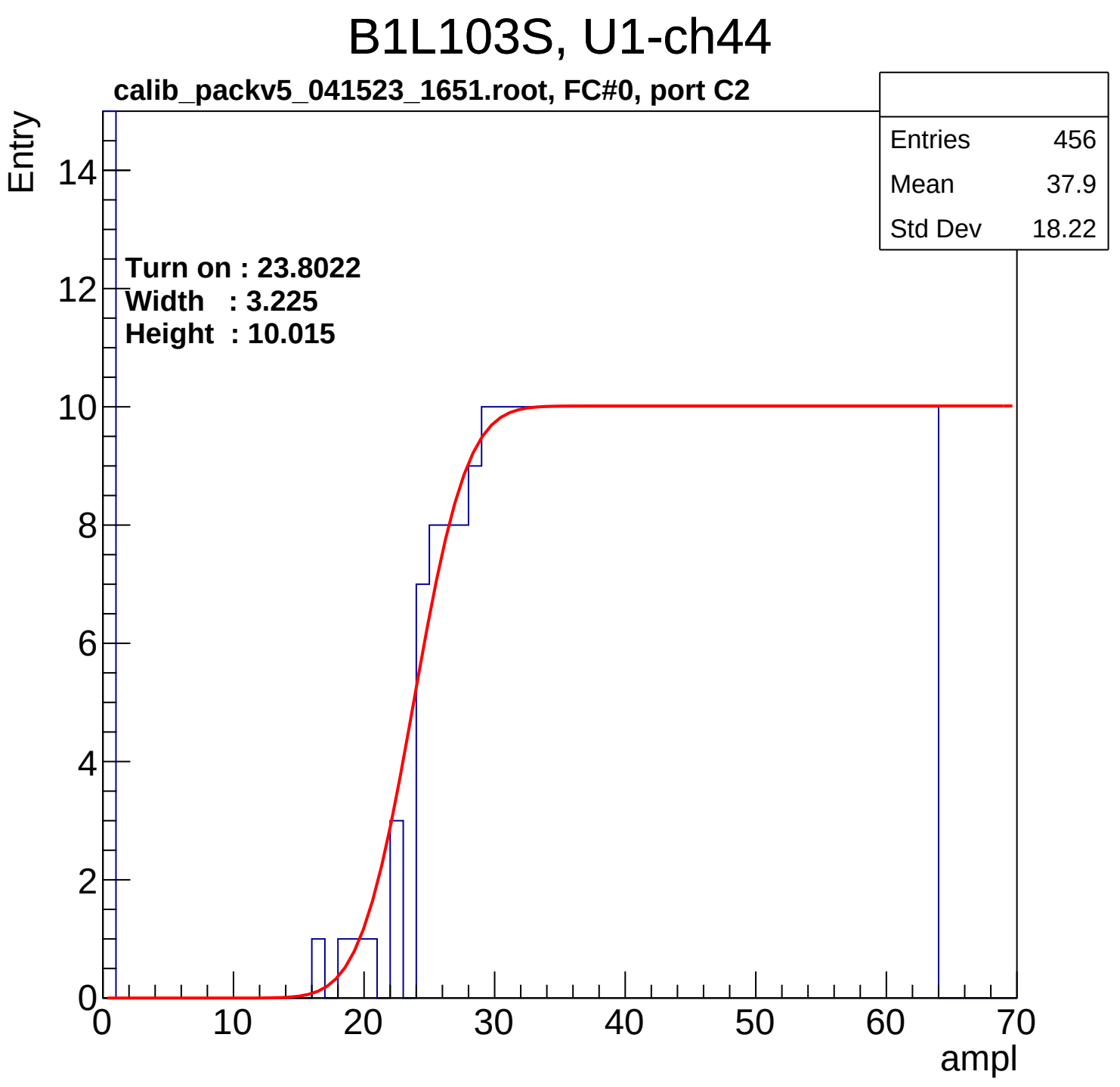
B1L103S, U1-ch44
calib_packv5_041523_1651.root, FC#0, port C2
Entries 456
Mean 37.9
Std Dev 18.22
Turn on : 23.8022
Width : 3.225
Height : 10.015
Entry
ampl
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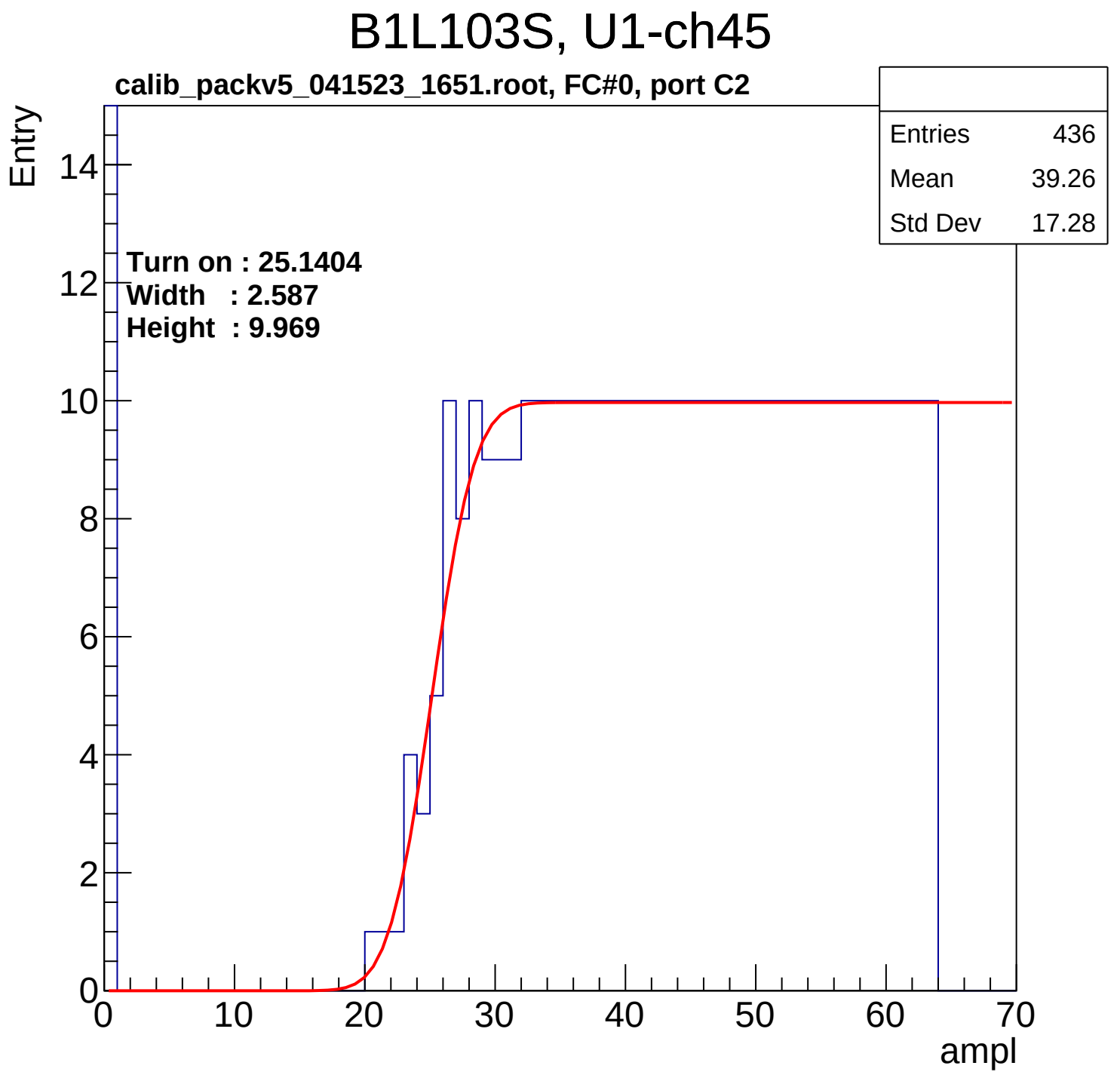
B1L103S, U1-ch45
calib_packv5_041523_1651.root, FC#0, port C2
Entries 436
Mean 39.26
Std Dev 17.28
Turn on : 25.1404
Width : 2.587
Height : 9.969
Entry
ampl
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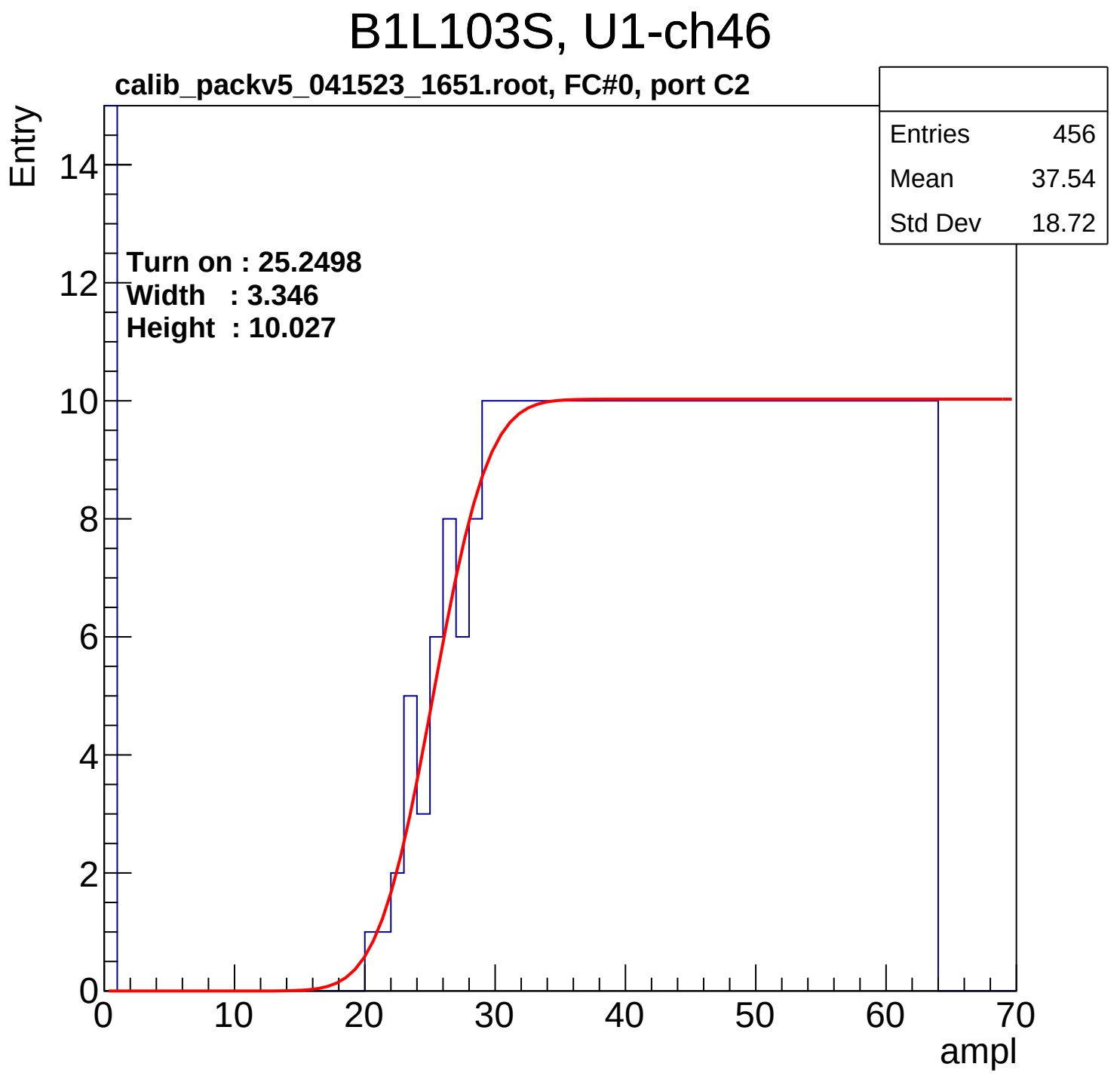
B1L103S, U1-ch46
calib_packv5_041523_1651.root, FC#0, port C2
Entries 456
Mean 37.54
Std Dev 18.72
Turn on : 25.2498
Width : 3.346
Height : 10.027
Entry
ampl
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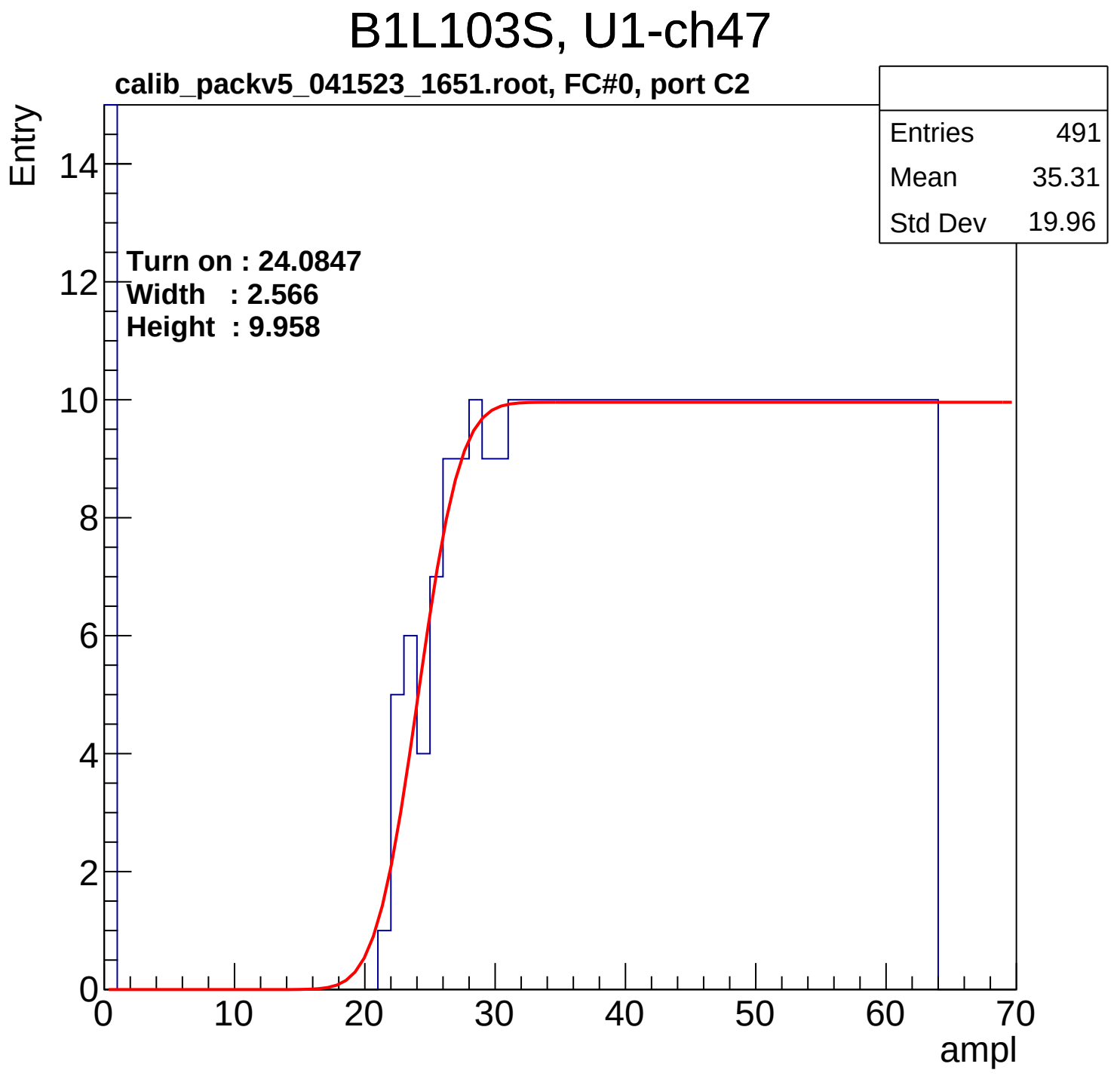
B1L103S, U1-ch47
calib_packv5_041523_1651.root, FC#0, port C2
Entries 491
Mean 35.31
Std Dev 19.96
Turn on : 24.0847
Width : 2.566
Height : 9.958
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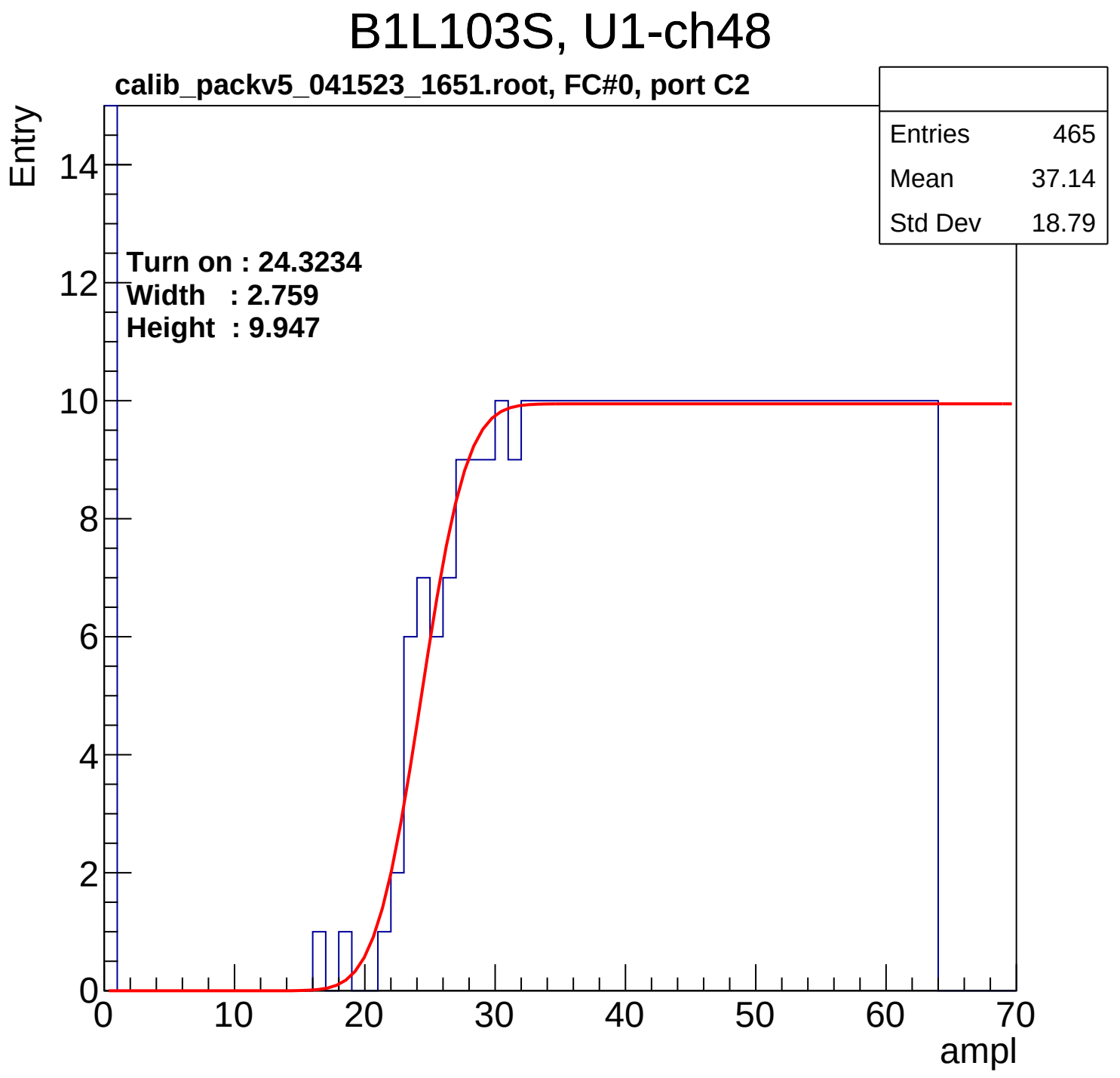
B1L103S, U1-ch48
calib_packv5_041523_1651.root, FC#0, port C2
Entries 465
Mean 37.14
Std Dev 18.79
Turn on : 24.3234
Width : 2.759
Height : 9.947
Entry
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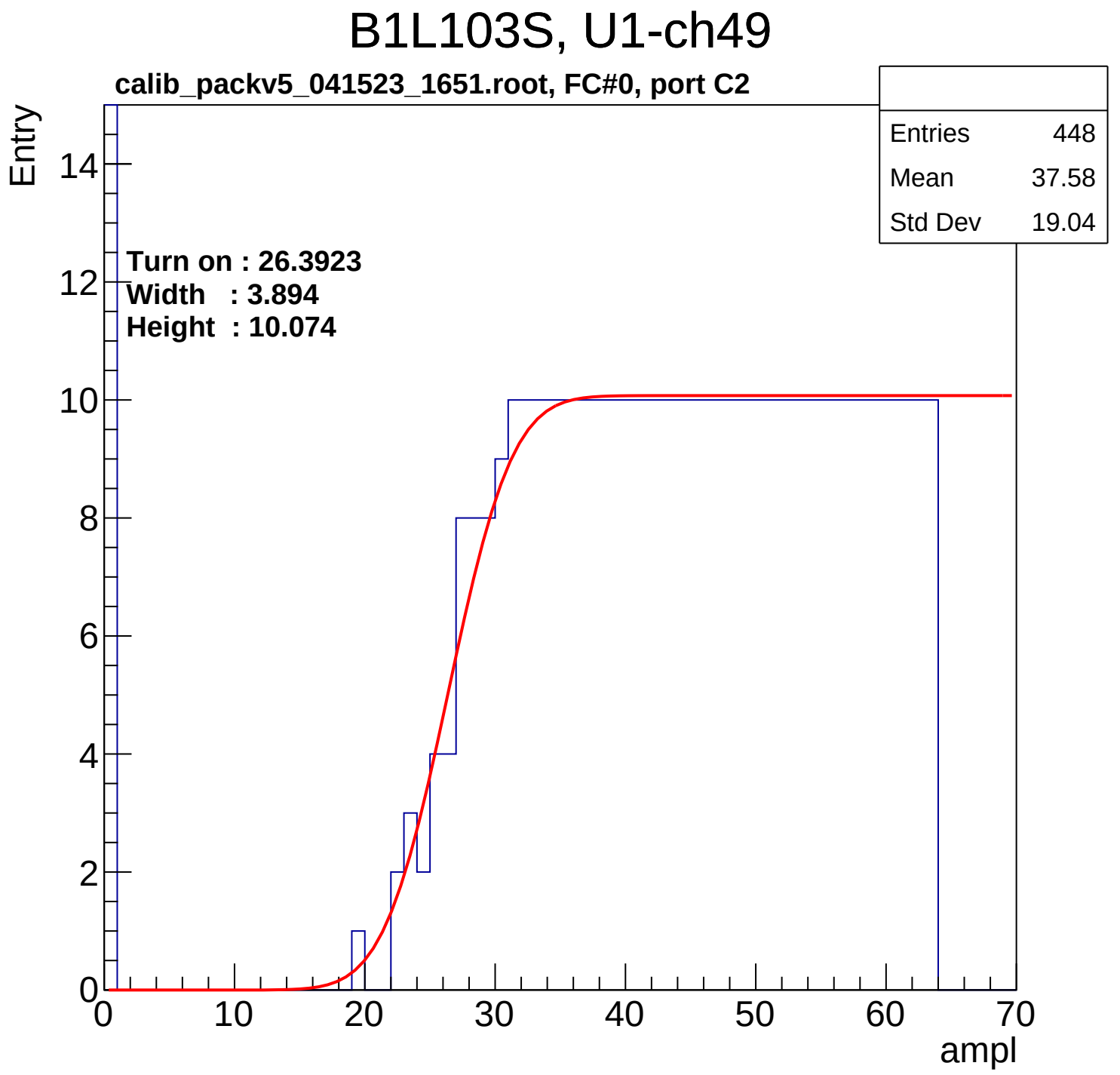
B1L103S, U1-ch49
calib_packv5_041523_1651.root, FC#0, port C2
Entries 448
Mean 37.58
Std Dev 19.04
Turn on : 26.3923
Width : 3.894
Height : 10.074
Entry
ampl
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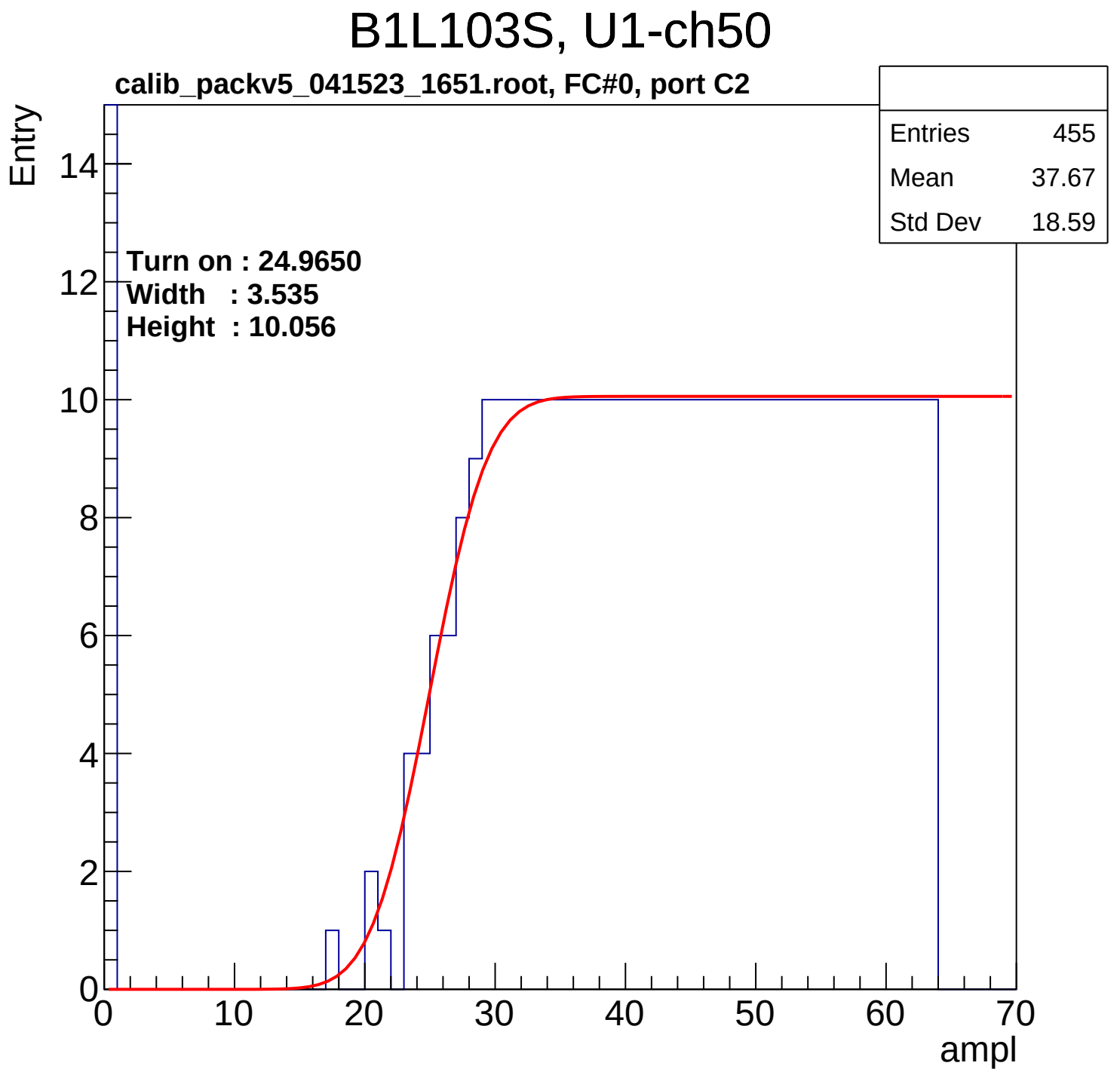
B1L103S, U1-ch50
calib_packv5_041523_1651.root, FC#0, port C2
Entries 455
Mean 37.67
Std Dev 18.59
Turn on : 24.9650
Width : 3.535
Height : 10.056
Entry
ampl
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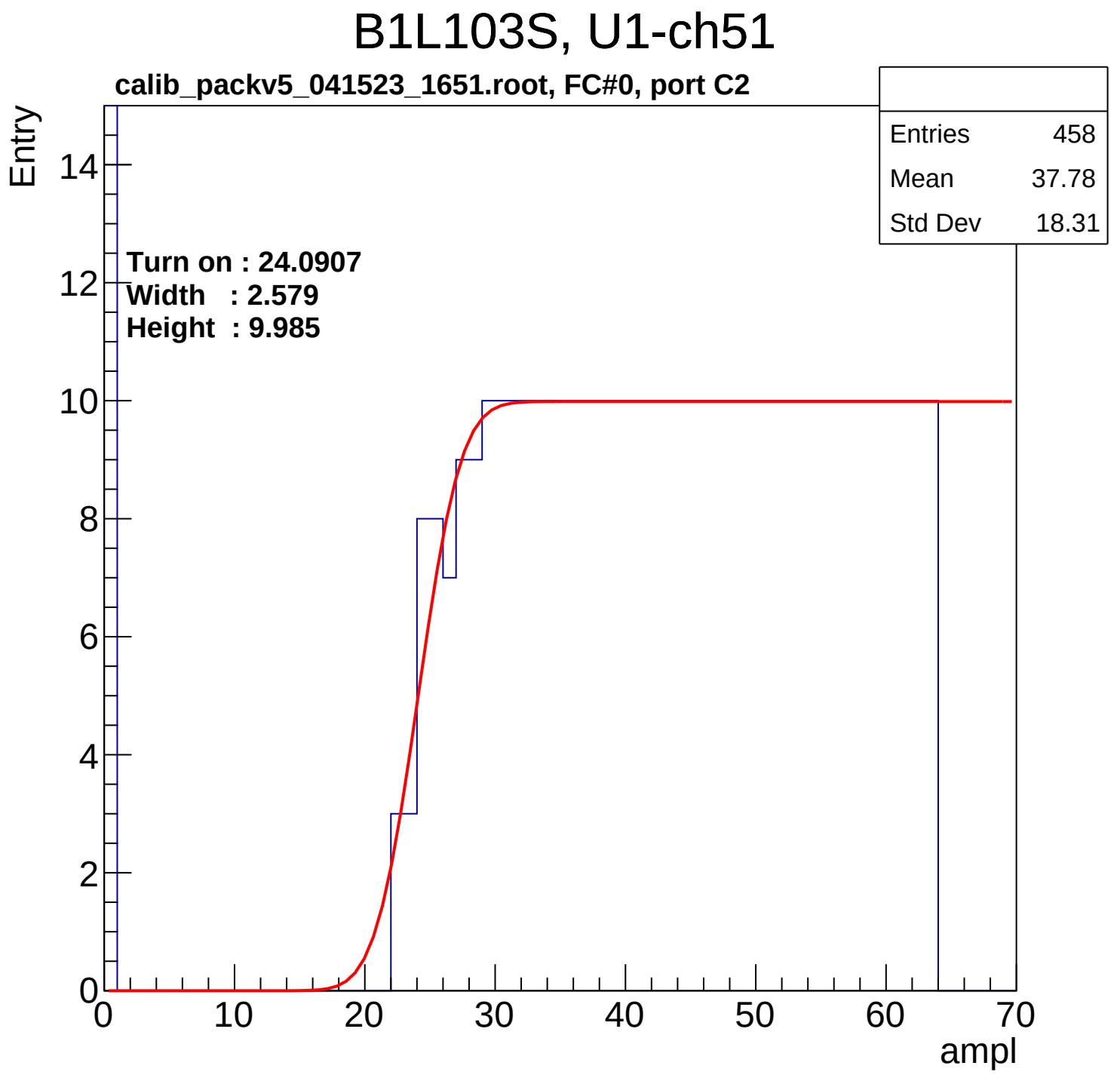
B1L103S, U1-ch51
calib_packv5_041523_1651.root, FC#0, port C2
Entries 458
Mean 37.78
Std Dev 18.31
Turn on : 24.0907
Width : 2.579
Height : 9.985
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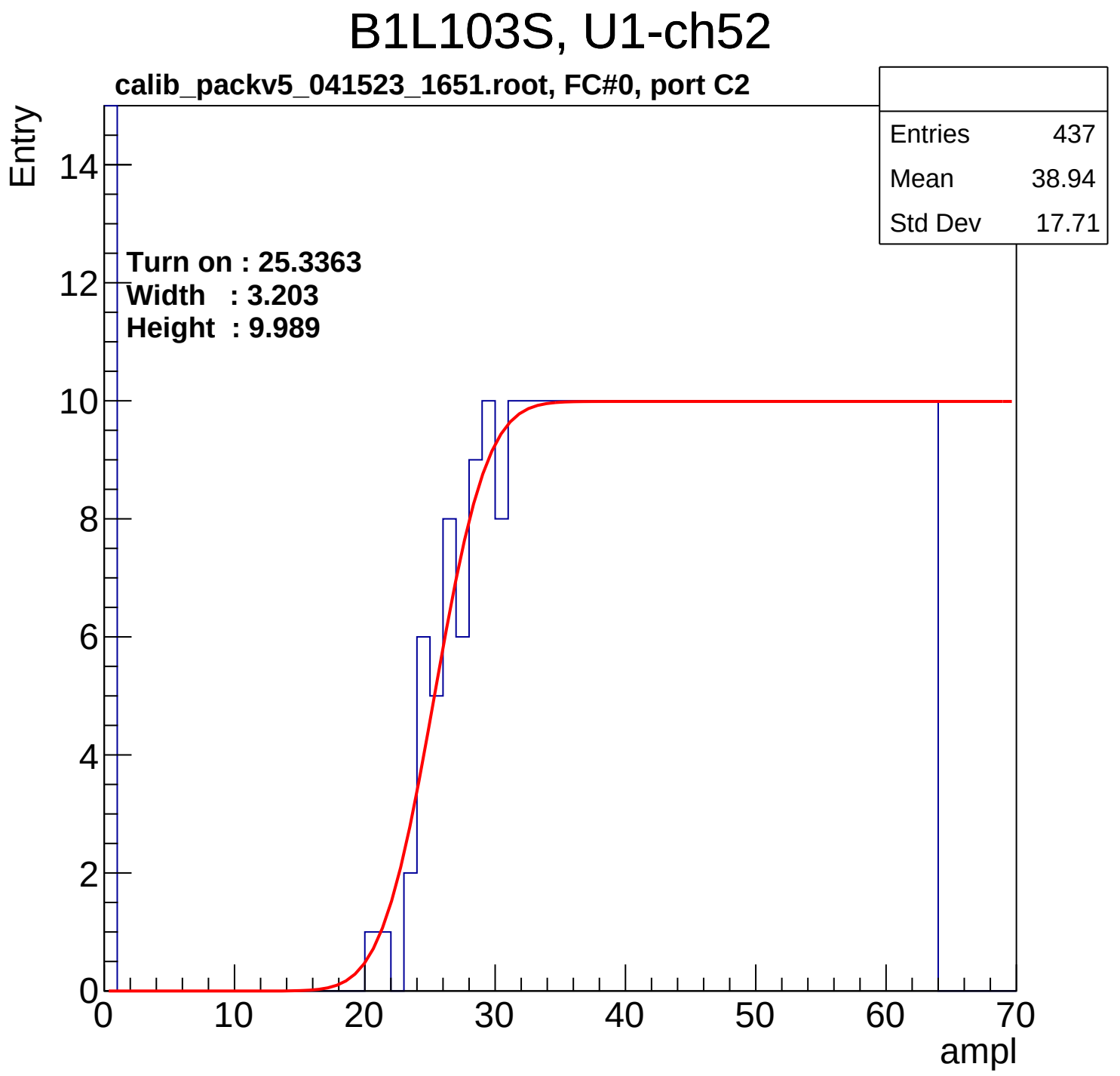
B1L103S, U1-ch52
calib_packv5_041523_1651.root, FC#0, port C2
Entries 437
Mean 38.94
Std Dev 17.71
Turn on : 25.3363
Width : 3.203
Height : 9.989
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ampl
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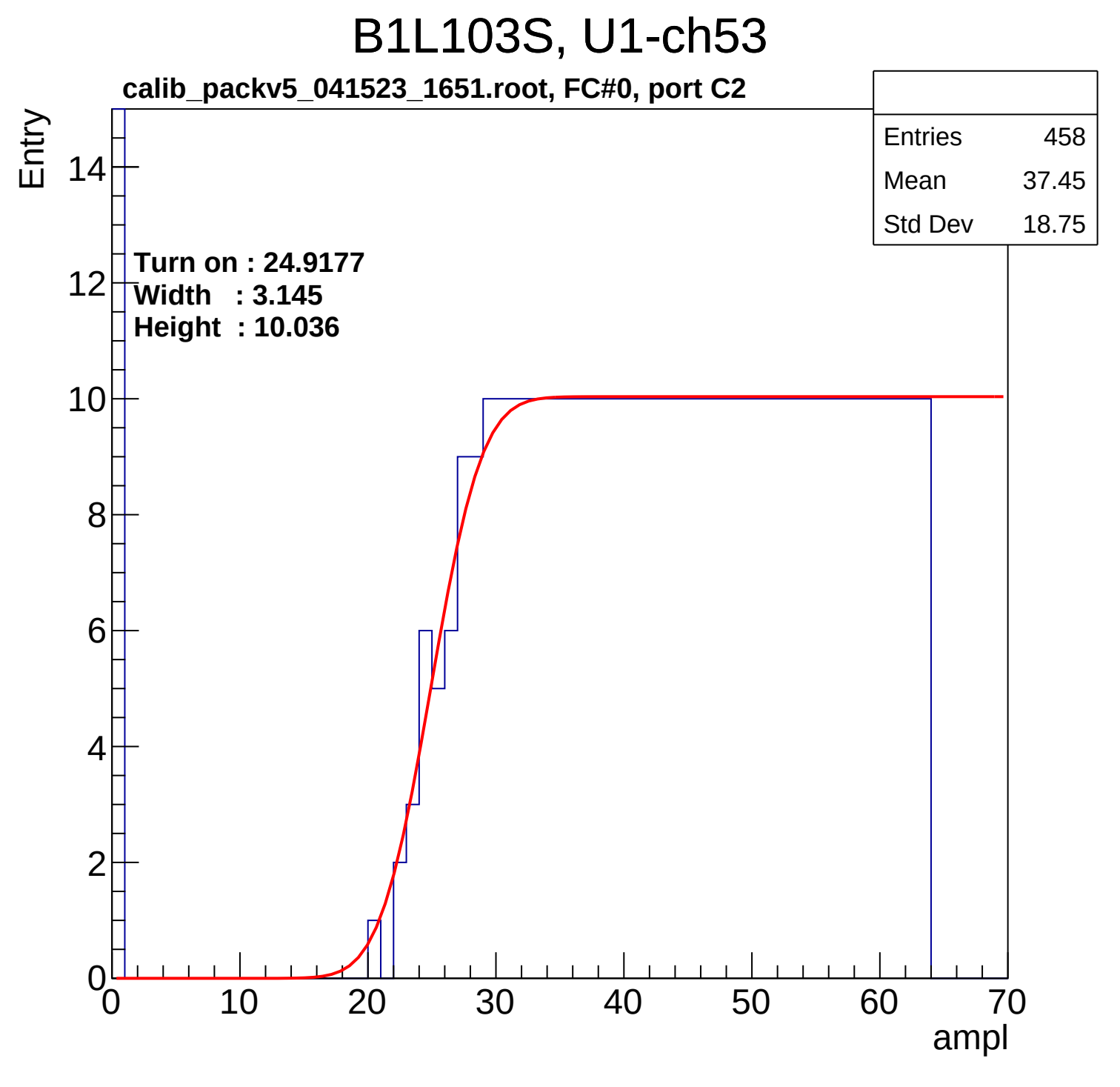
B1L103S, U1-ch53
calib_packv5_041523_1651.root, FC#0, port C2
Entries 458
Mean 37.45
Std Dev 18.75
Turn on : 24.9177
Width : 3.145
Height : 10.036
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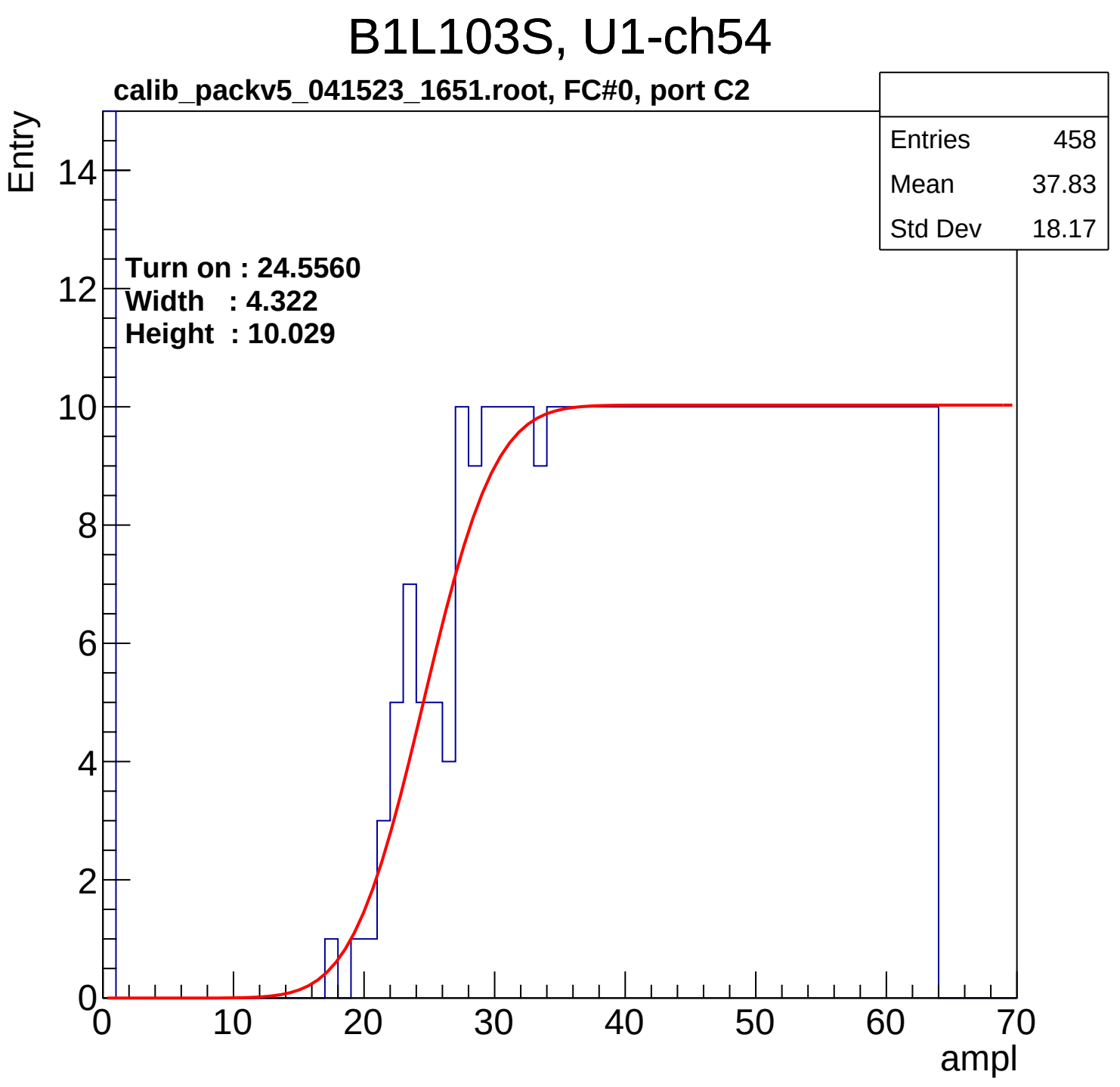
B1L103S, U1-ch54
calib_packv5_041523_1651.root, FC#0, port C2
Entries 458
Mean 37.83
Std Dev 18.17
Turn on : 24.5560
Width : 4.322
Height : 10.029
Entry
ampl
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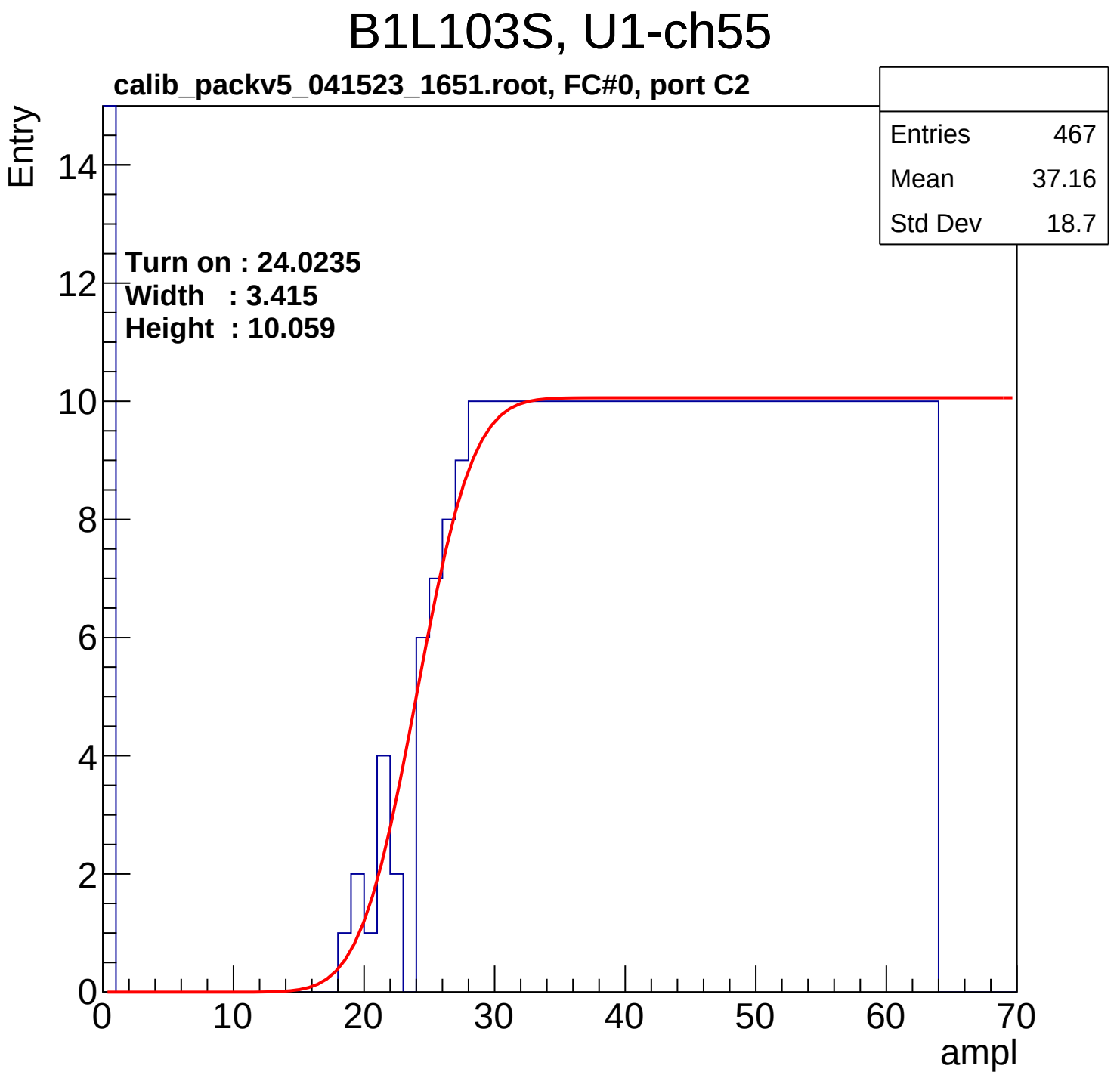
B1L103S, U1-ch55
calib_packv5_041523_1651.root, FC#0, port C2
Entries 467
Mean 37.16
Std Dev 18.7
Turn on : 24.0235
Width : 3.415
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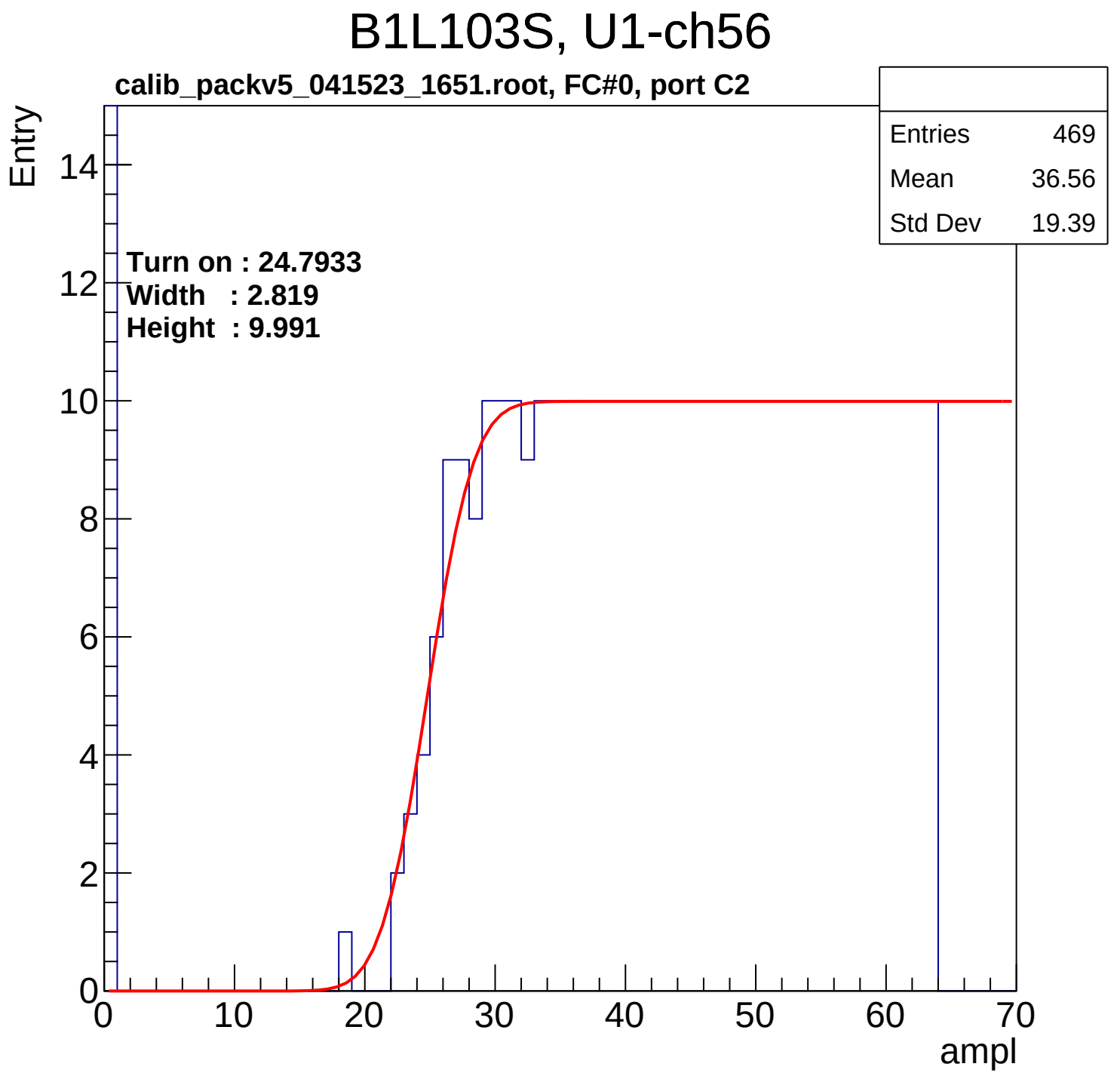
B1L103S, U1-ch56
calib_packv5_041523_1651.root, FC#0, port C2
Entries 469
Mean 36.56
Std Dev 19.39
Turn on : 24.7933
Width : 2.819
Height : 9.991
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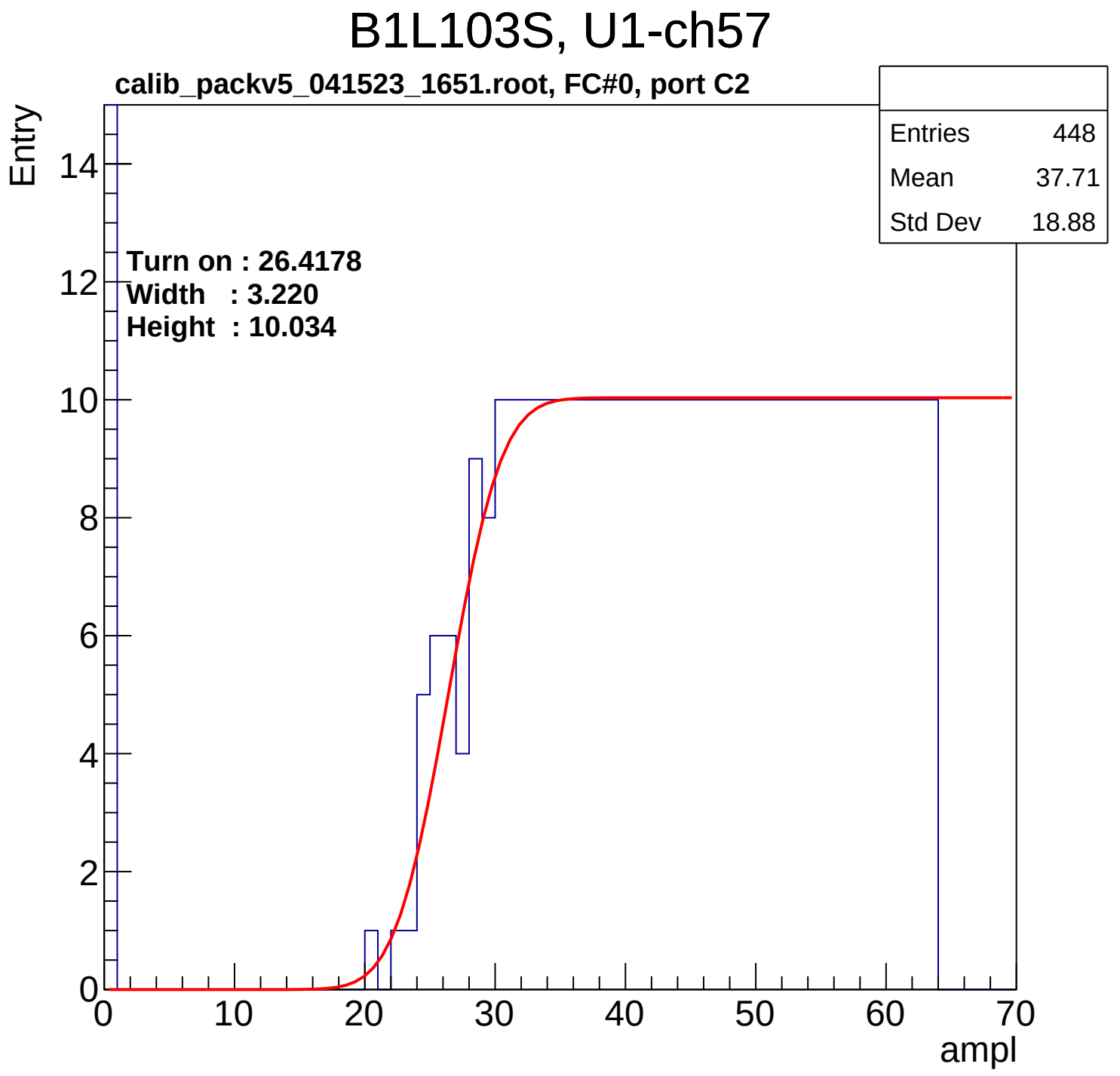
B1L103S, U1-ch57
calib_packv5_041523_1651.root, FC#0, port C2
Entries 448
Mean 37.71
Std Dev 18.88
Turn on : 26.4178
Width : 3.220
Height : 10.034
Entry
ampl
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6
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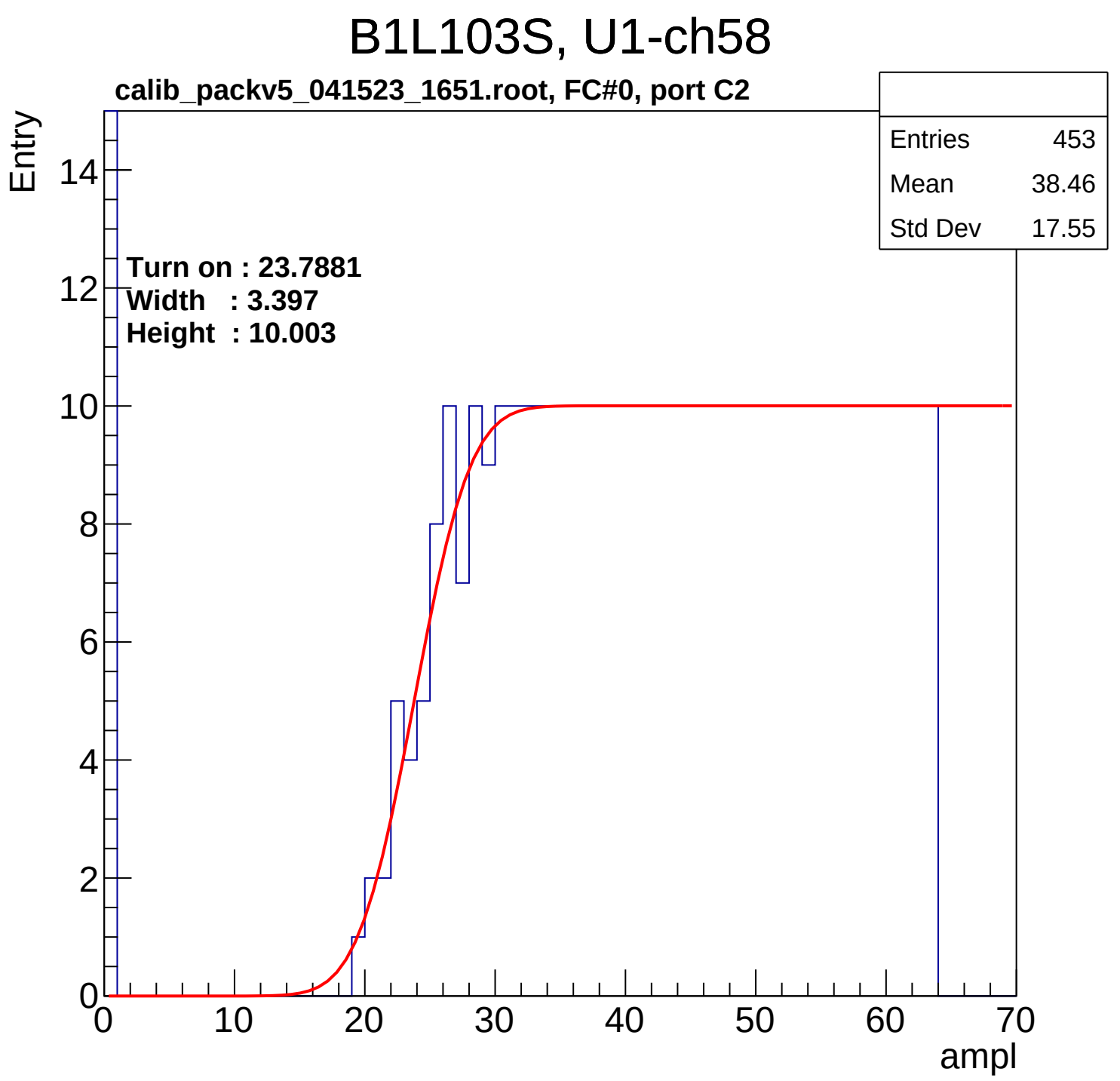
B1L103S, U1-ch58
calib_packv5_041523_1651.root, FC#0, port C2
Entries 453
Mean 38.46
Std Dev 17.55
Turn on : 23.7881
Width : 3.397
Height : 10.003
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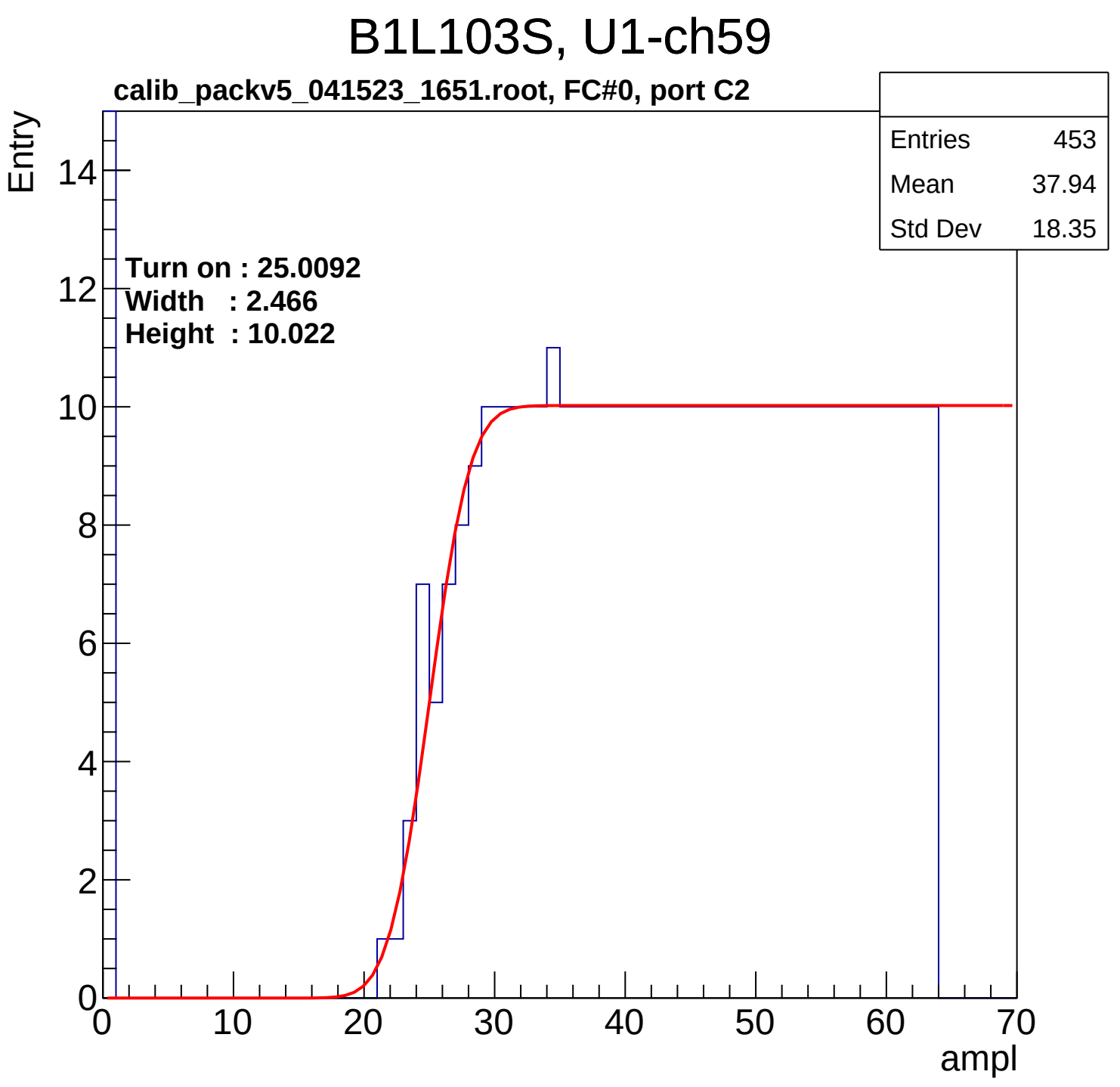
B1L103S, U1-ch59
calib_packv5_041523_1651.root, FC#0, port C2
Entries 453
Mean 37.94
Std Dev 18.35
Turn on : 25.0092
Width : 2.466
Height : 10.022
Entry
ampl
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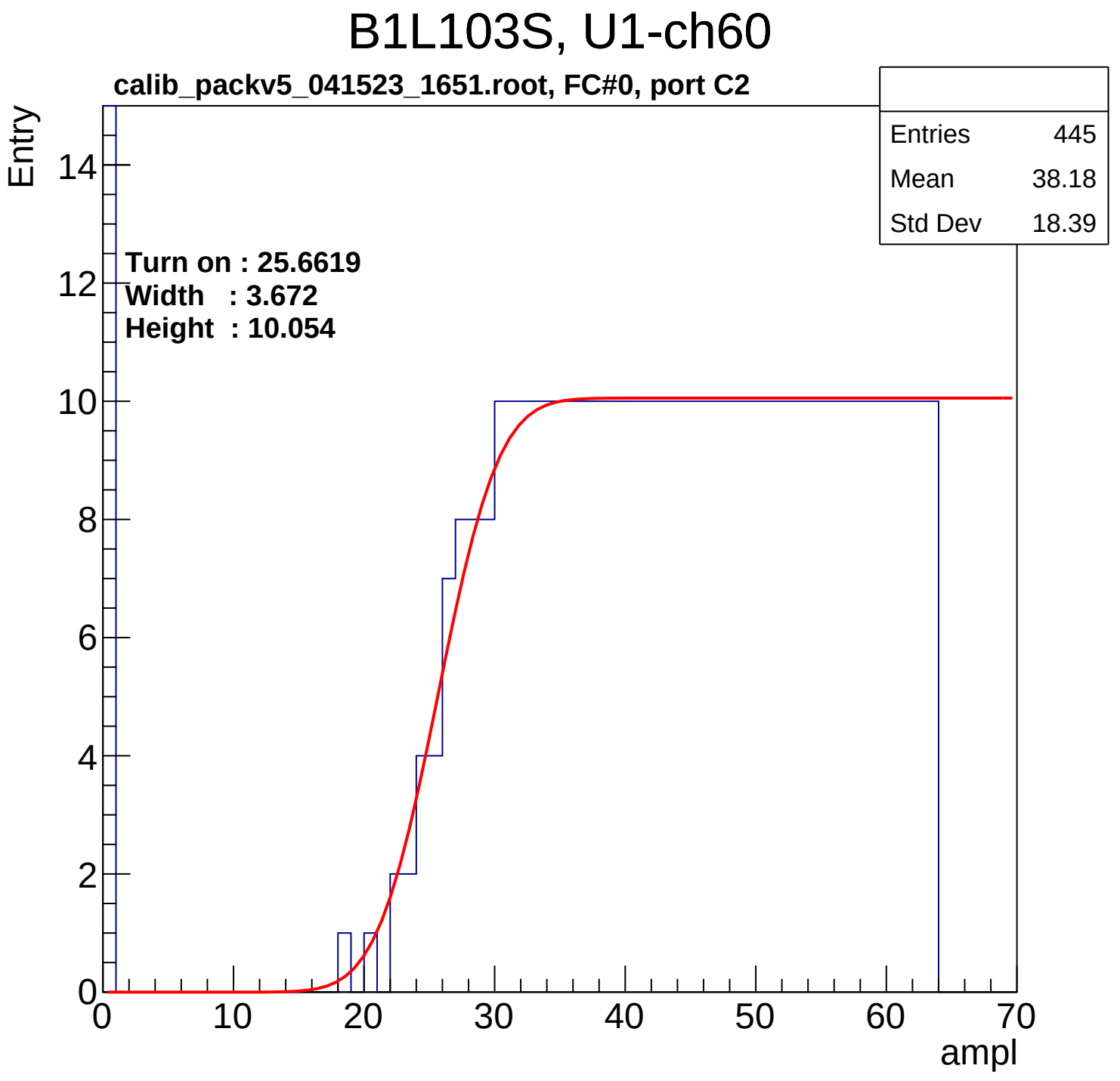
B1L103S, U1-ch60
calib_packv5_041523_1651.root, FC#0, port C2
Entries 445
Mean 38.18
Std Dev 18.39
Turn on : 25.6619
Width : 3.672
Height : 10.054
Entry
ampl
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2
4
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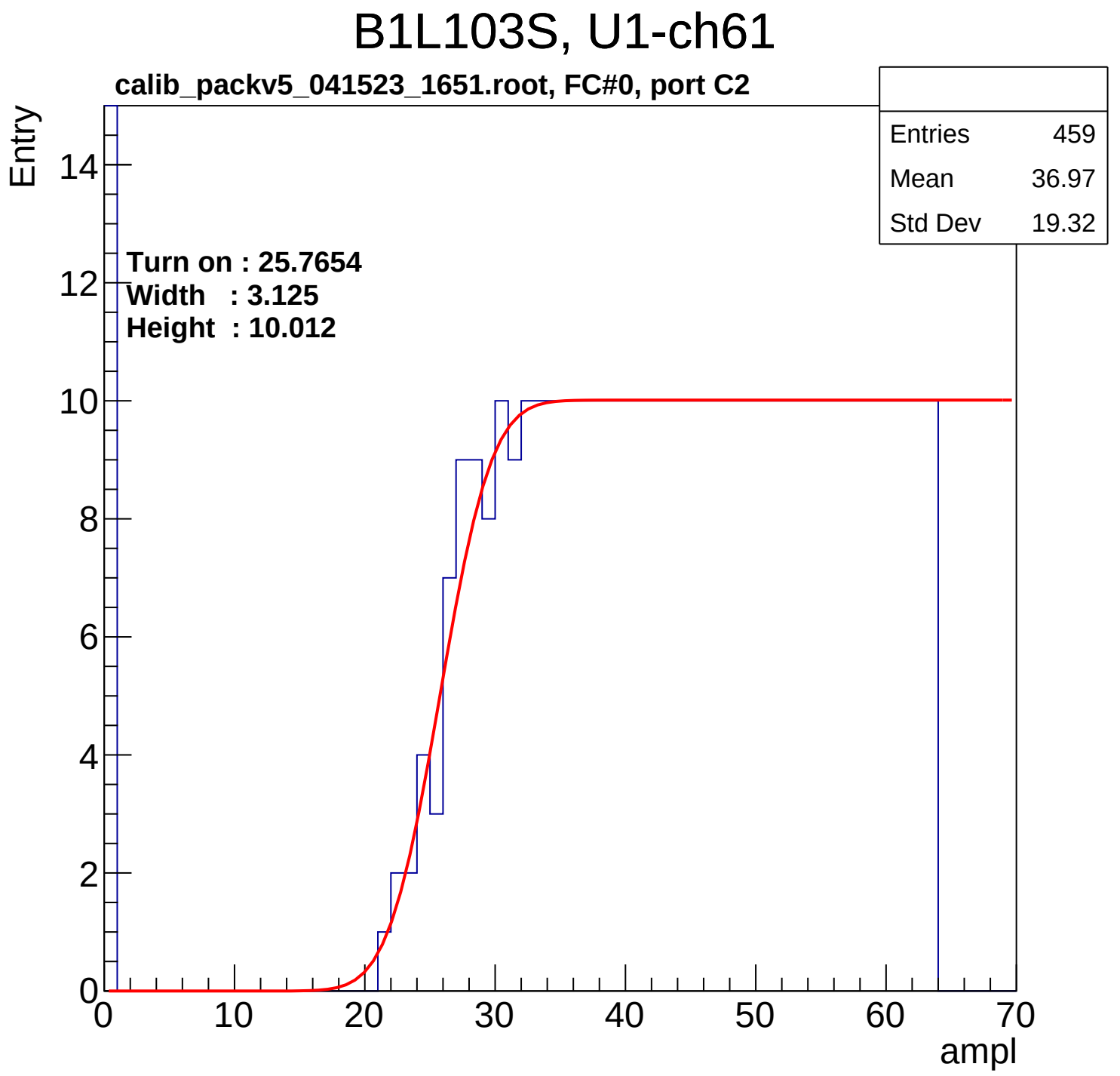
B1L103S, U1-ch61
calib_packv5_041523_1651.root, FC#0, port C2
Entries 459
Mean 36.97
Std Dev 19.32
Turn on : 25.7654
Width : 3.125
Height : 10.012
Entry
ampl
0
2
4
6
8
10
12
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0
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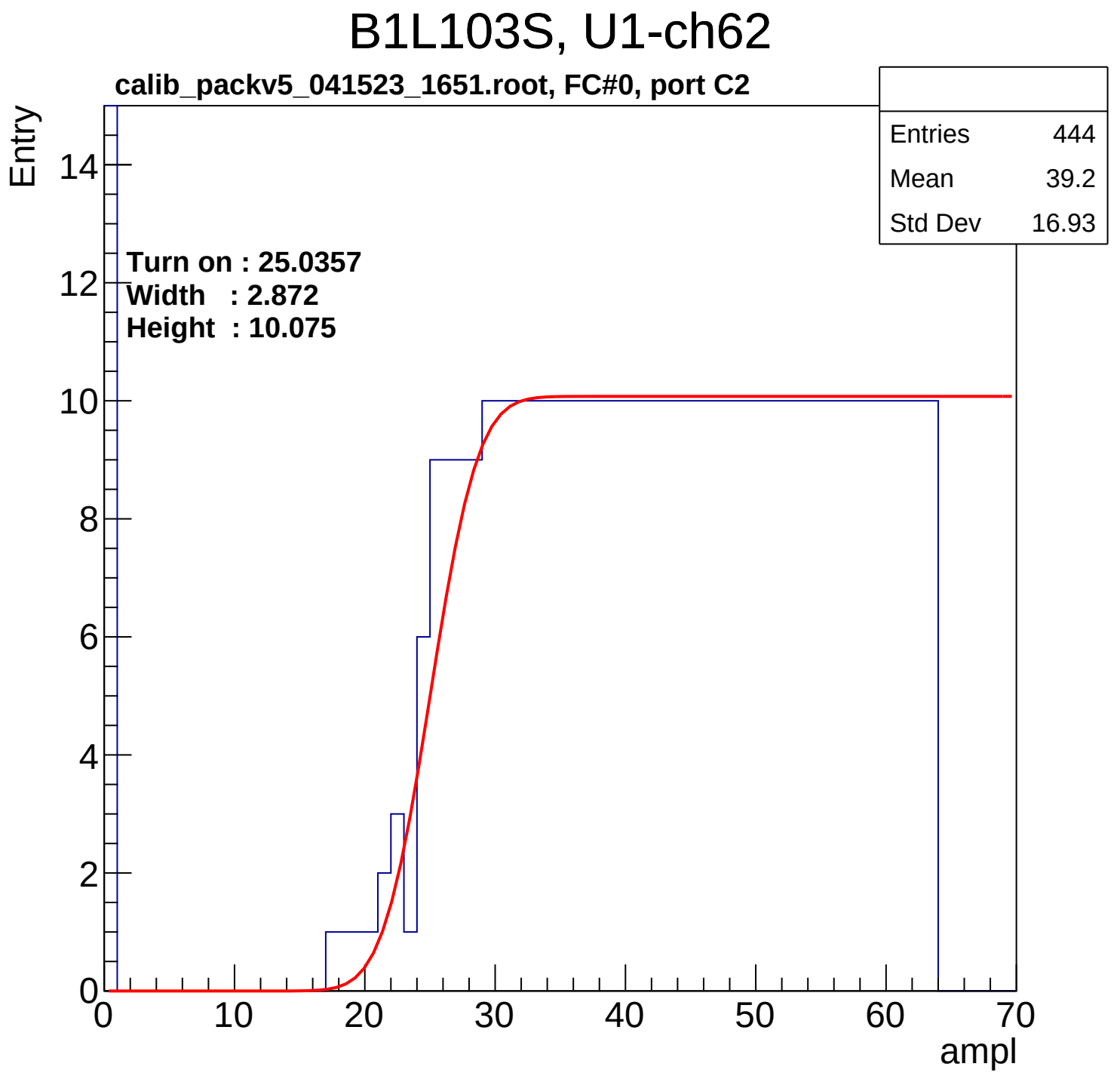
B1L103S, U1-ch62
calib_packv5_041523_1651.root, FC#0, port C2
Entries 444
Mean 39.2
Std Dev 16.93
Turn on : 25.0357
Width : 2.872
Height : 10.075
Entry
ampl
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2
4
6
8
10
12
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0
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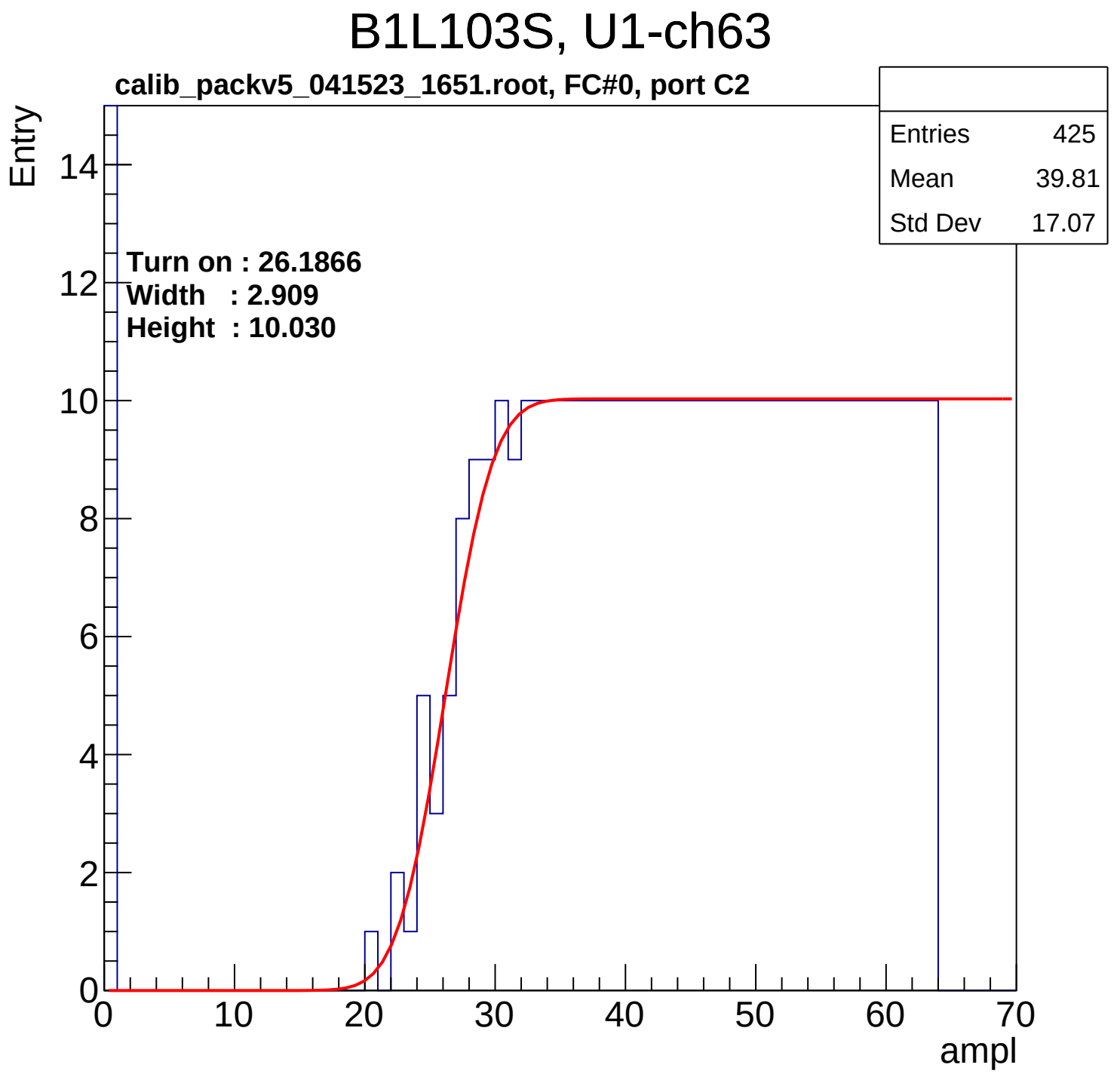
B1L103S, U1-ch63
calib_packv5_041523_1651.root, FC#0, port C2
Entries 425
Mean 39.81
Std Dev 17.07
Turn on : 26.1866
Width : 2.909
Height : 10.030
Entry
ampl
0
2
4
6
8
10
12
14
0
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60
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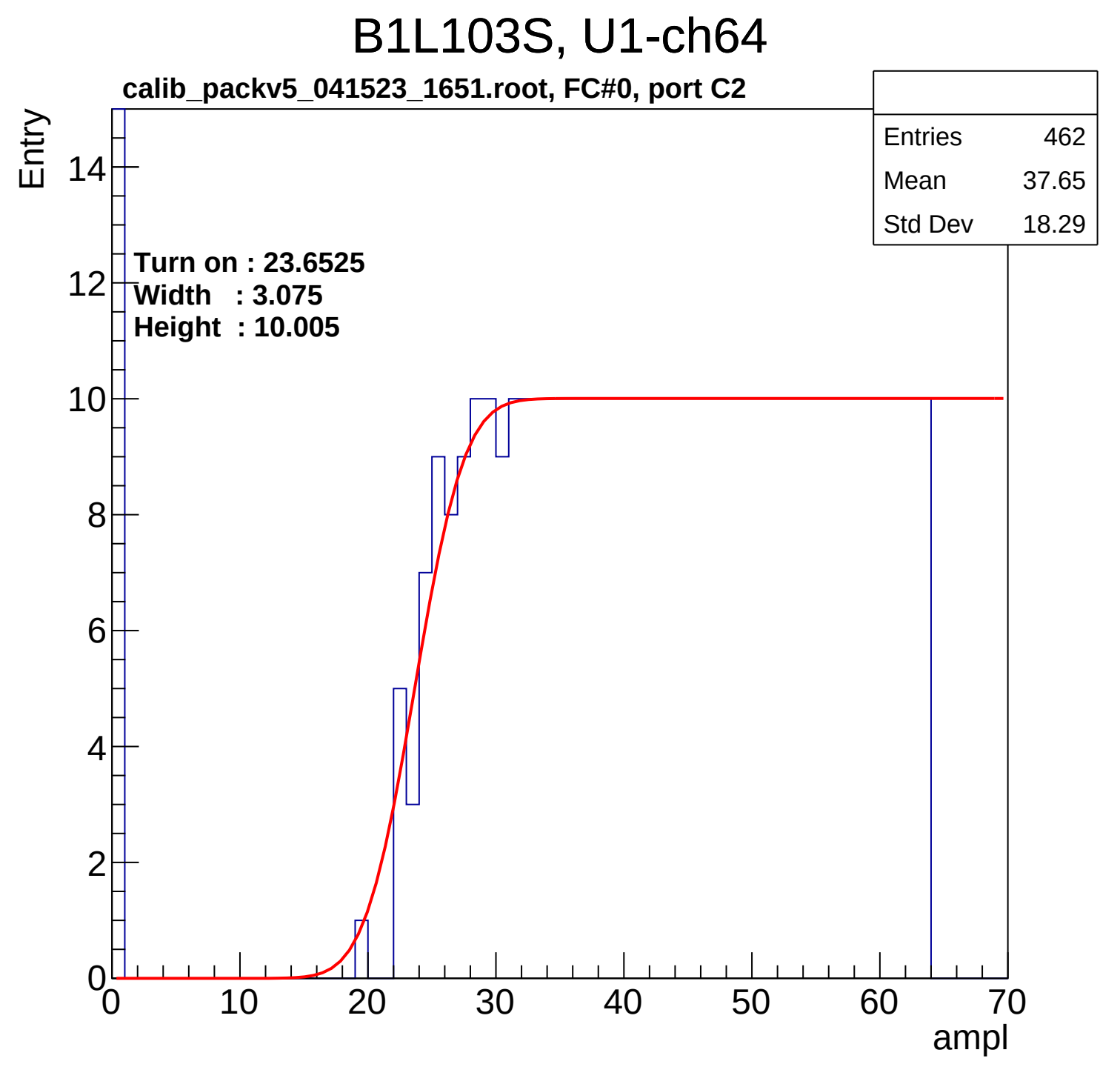
B1L103S, U1-ch64
calib_packv5_041523_1651.root, FC#0, port C2
Entries 462
Mean 37.65
Std Dev 18.29
Turn on : 23.6525
Width : 3.075
Height : 10.005
Entry
ampl
0
2
4
6
8
10
12
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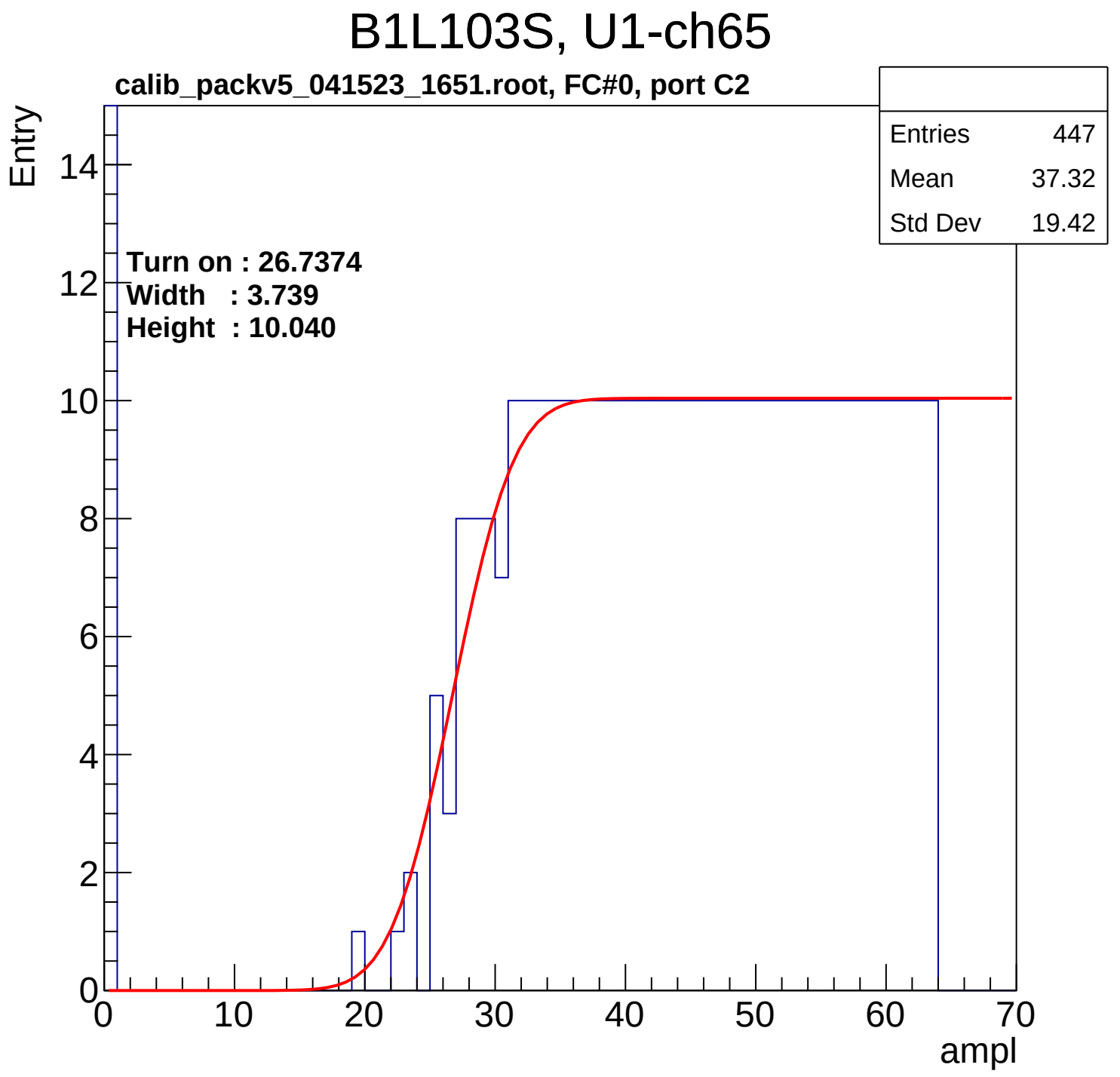
B1L103S, U1-ch65
calib_packv5_041523_1651.root, FC#0, port C2
Entries 447
Mean 37.32
Std Dev 19.42
Turn on : 26.7374
Width : 3.739
Height : 10.040
Entry
ampl
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2
4
6
8
10
12
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0
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60
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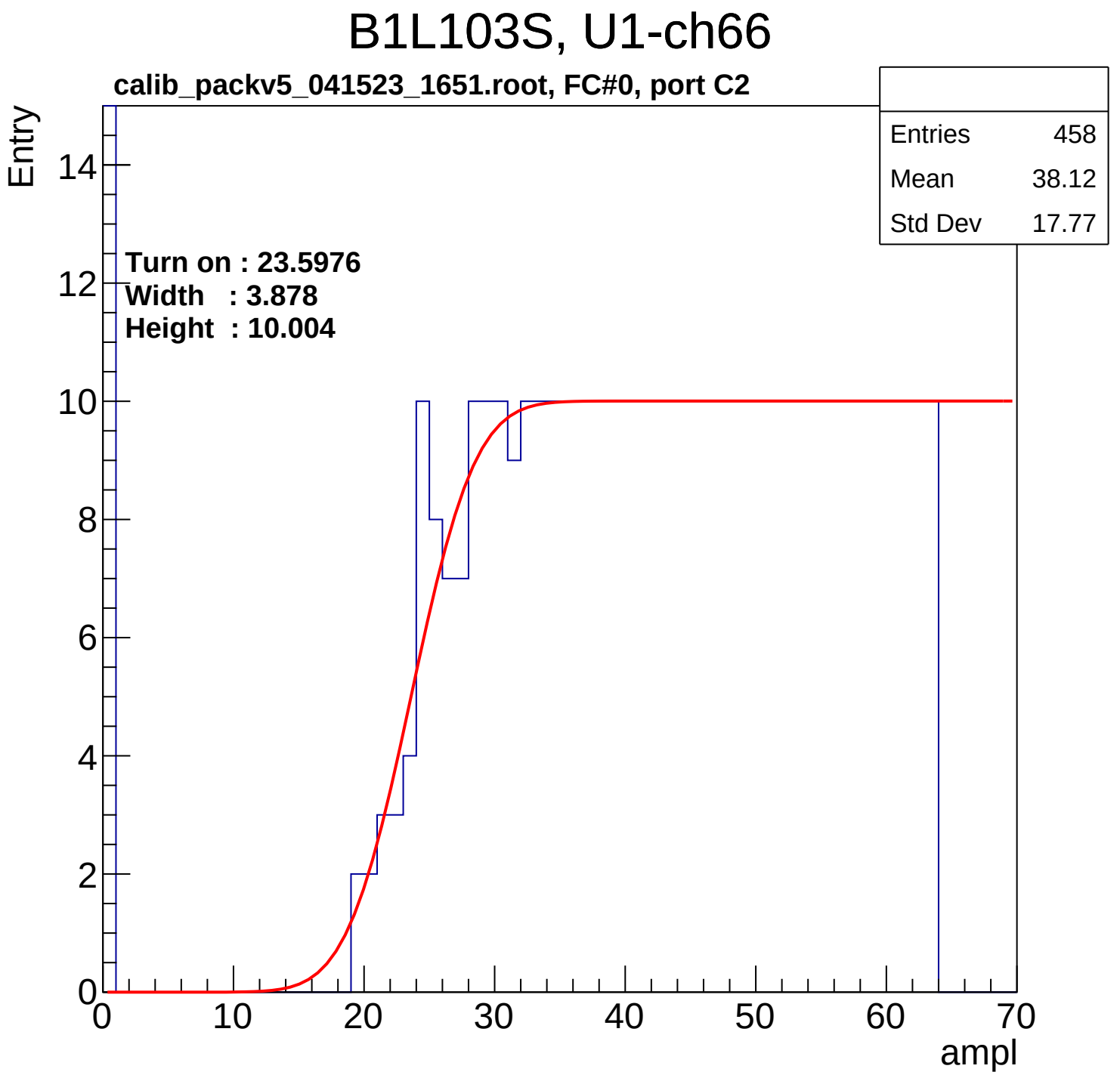
B1L103S, U1-ch66
calib_packv5_041523_1651.root, FC#0, port C2
Entries 458
Mean 38.12
Std Dev 17.77
Turn on : 23.5976
Width : 3.878
Height : 10.004
Entry
ampl
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8
10
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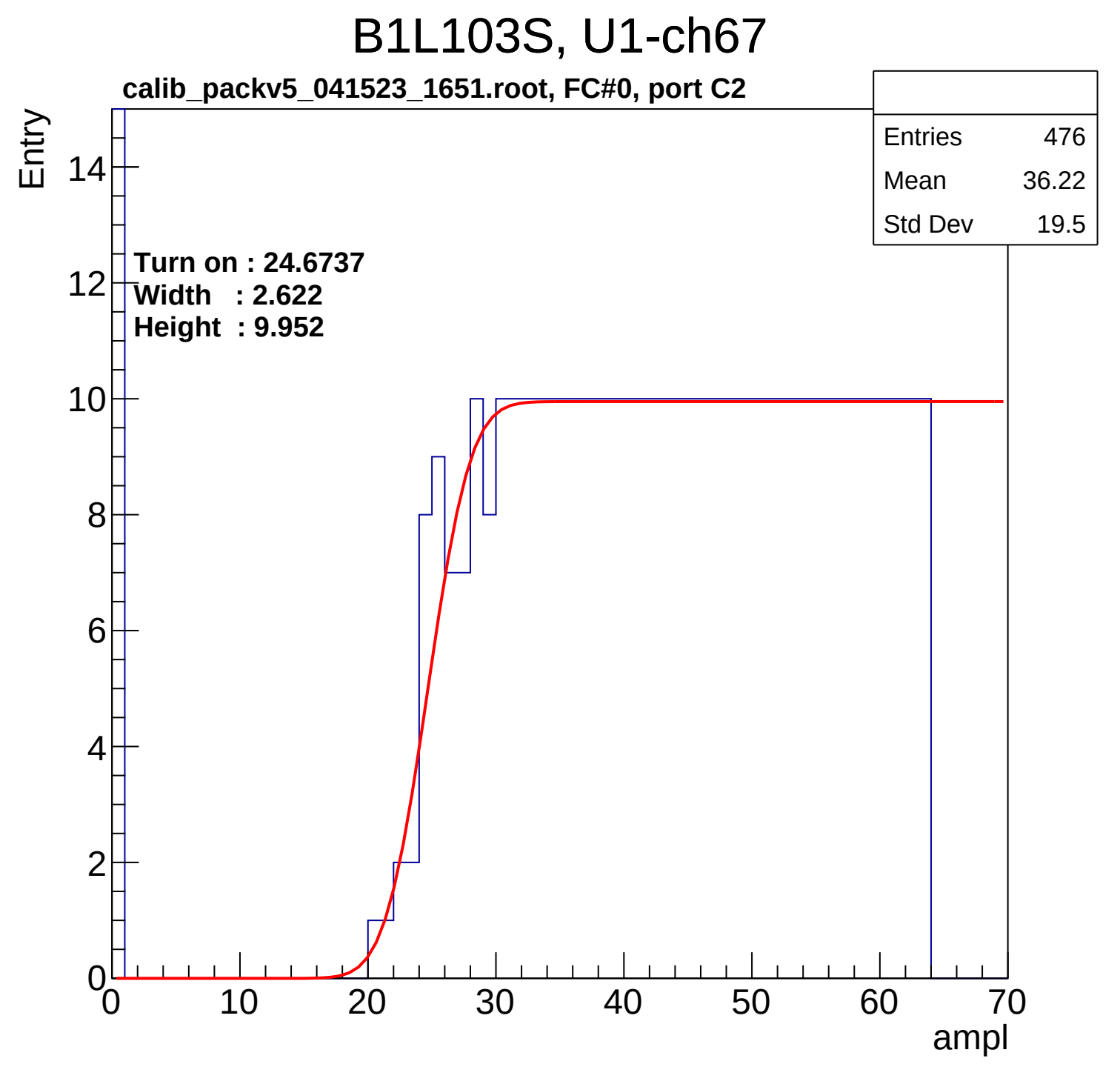
B1L103S, U1-ch67
calib_packv5_041523_1651.root, FC#0, port C2
Entries 476
Mean 36.22
Std Dev 19.5
Turn on : 24.6737
Width : 2.622
Height : 9.952
Entry
ampl
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6
8
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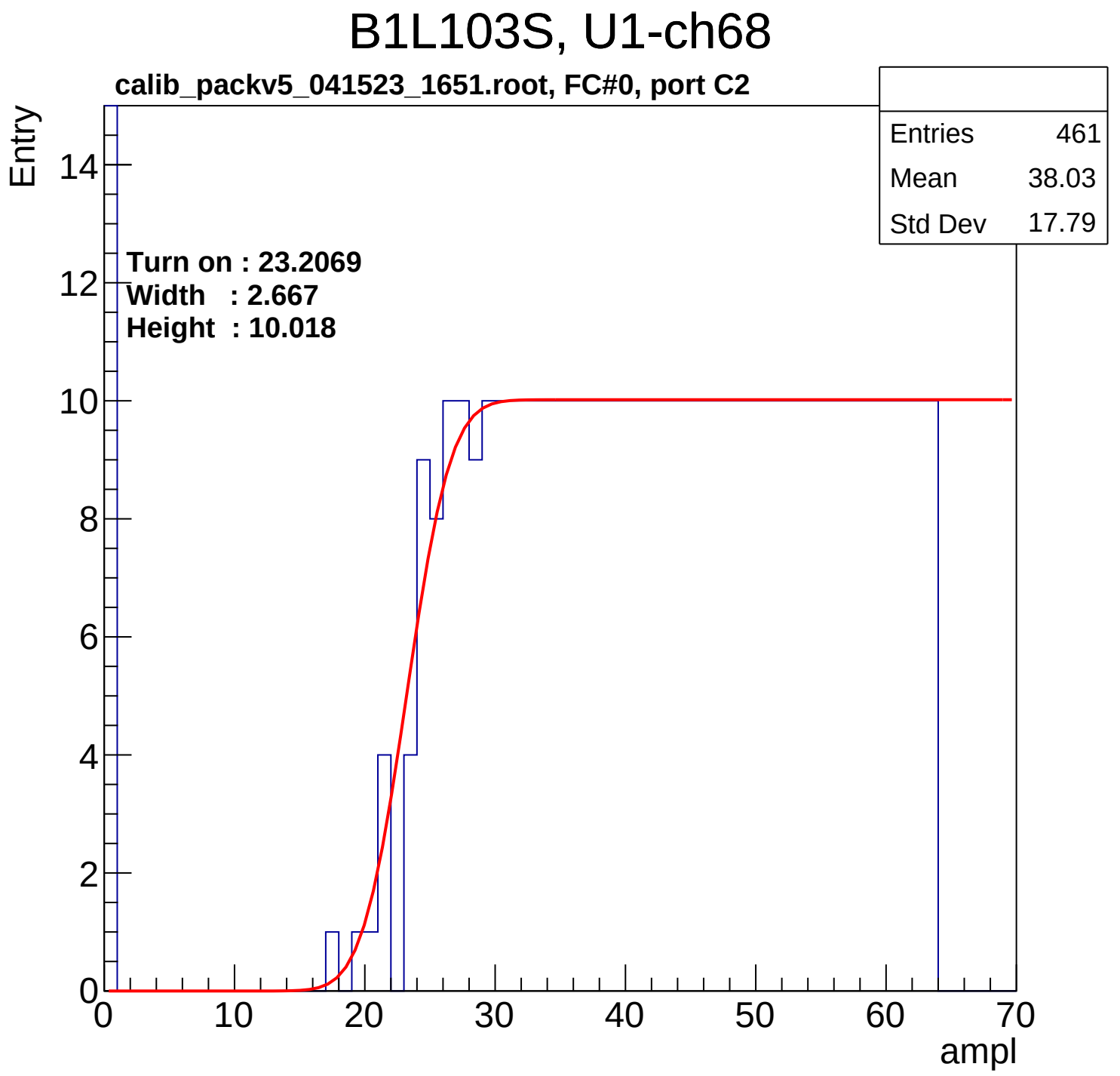
B1L103S, U1-ch68
calib_packv5_041523_1651.root, FC#0, port C2
Entries 461
Mean 38.03
Std Dev 17.79
Turn on : 23.2069
Width : 2.667
Height : 10.018
Entry
ampl
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10
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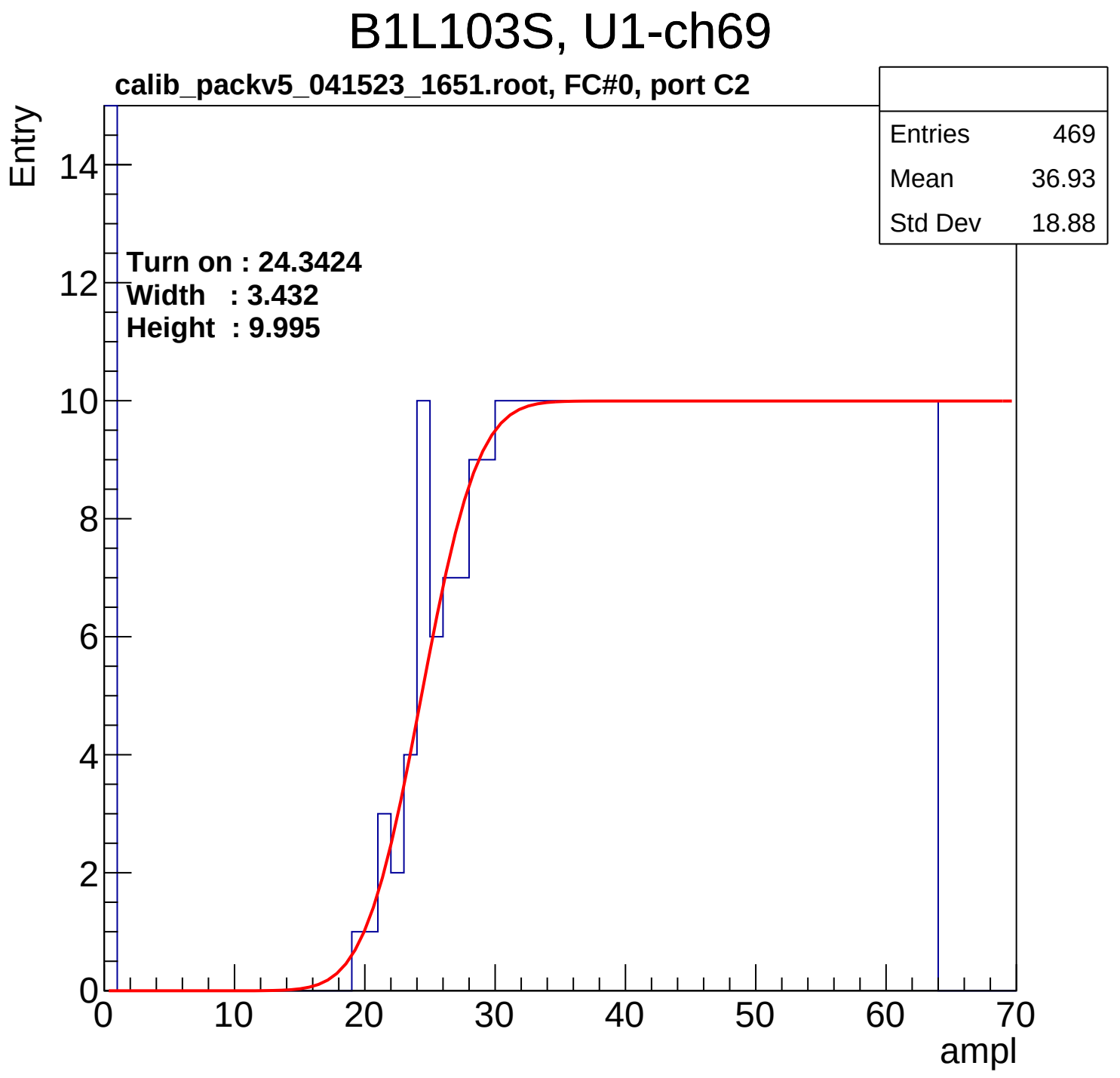
B1L103S, U1-ch69
calib_packv5_041523_1651.root, FC#0, port C2
Entries 469
Mean 36.93
Std Dev 18.88
Turn on : 24.3424
Width : 3.432
Height : 9.995
Entry
ampl
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6
8
10
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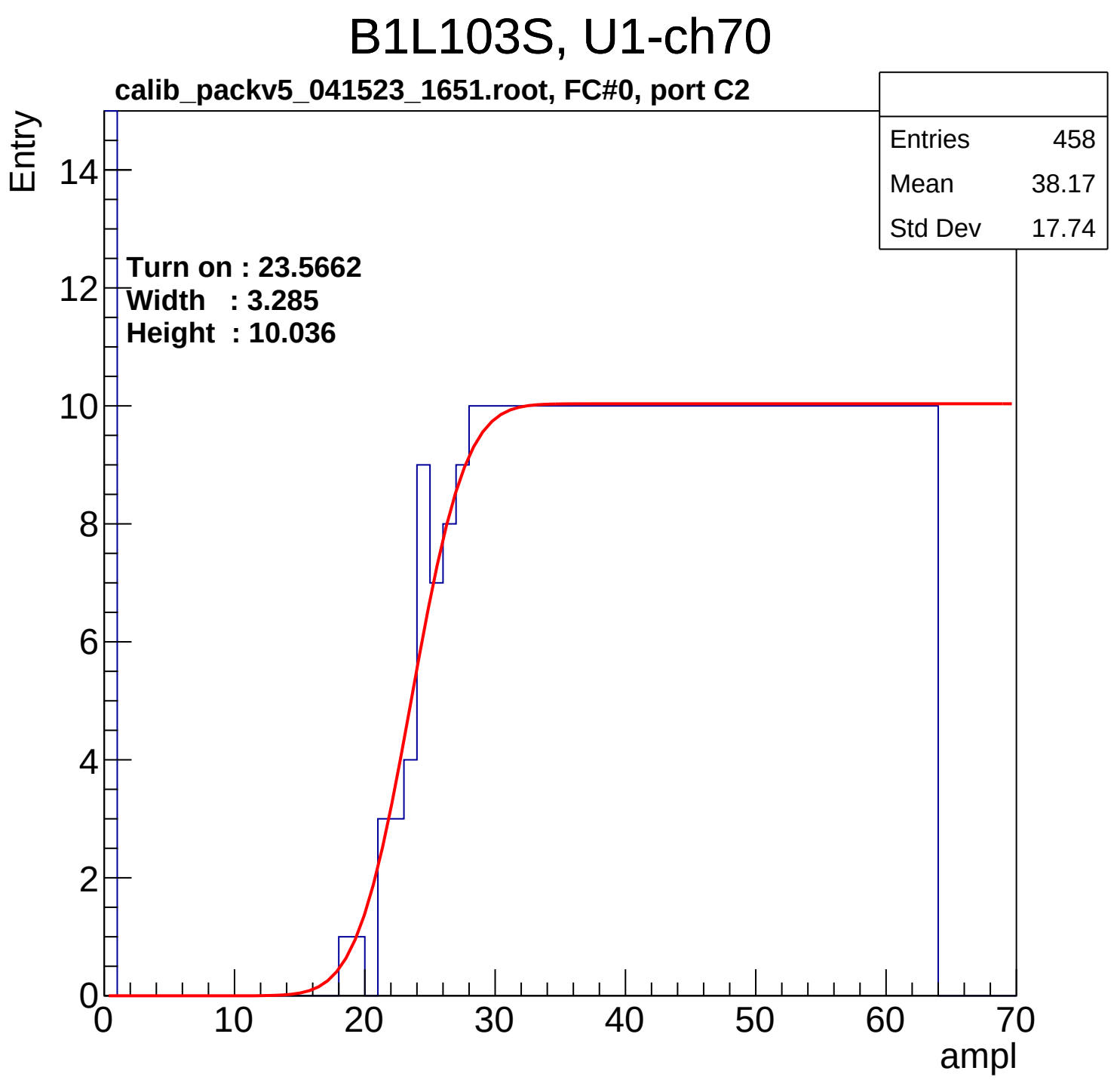
B1L103S, U1-ch70
calib_packv5_041523_1651.root, FC#0, port C2
Entries 458
Mean 38.17
Std Dev 17.74
Turn on : 23.5662
Width : 3.285
Height : 10.036
Entry
ampl
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6
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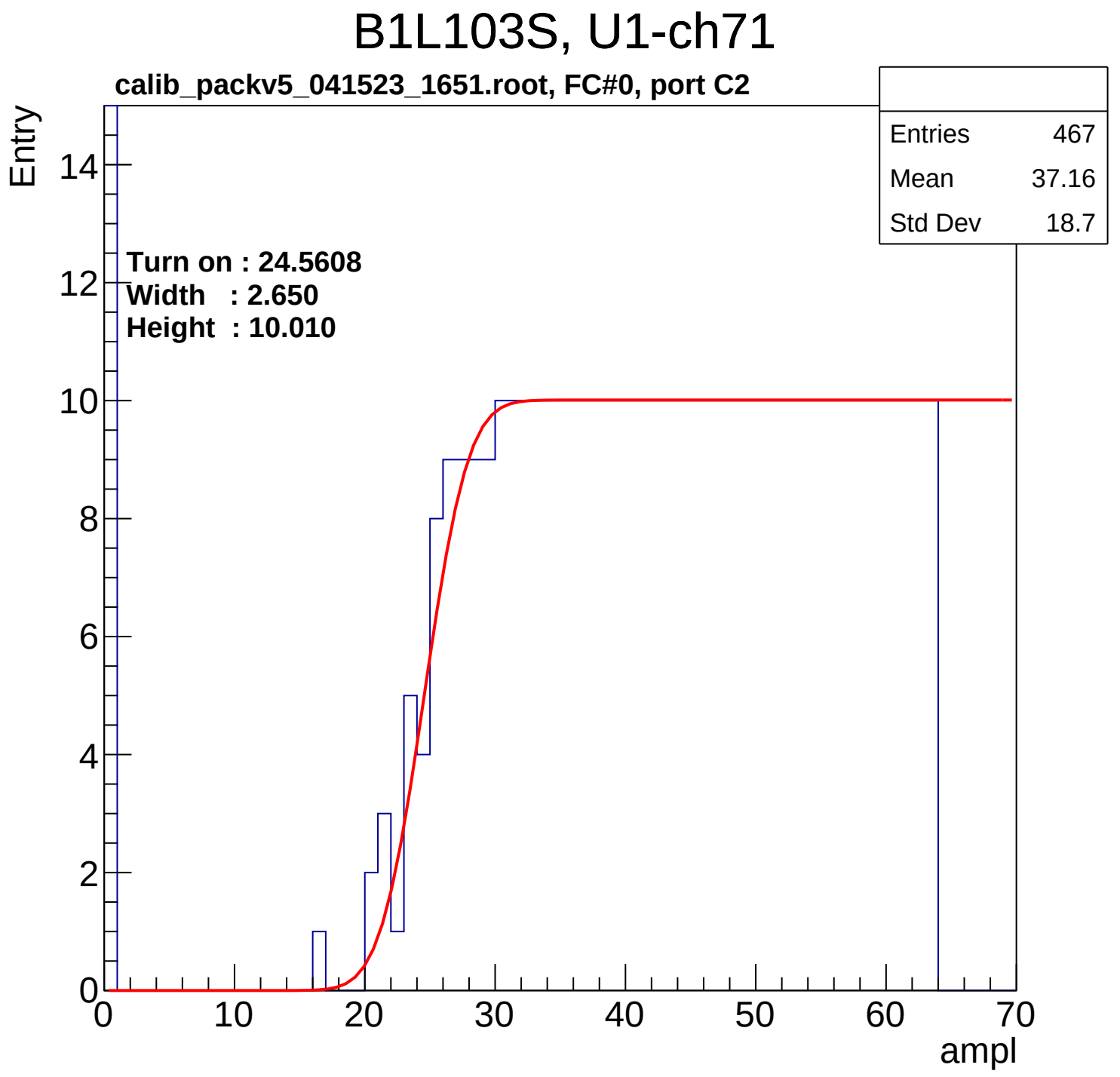
B1L103S, U1-ch71
calib_packv5_041523_1651.root, FC#0, port C2
Entries 467
Mean 37.16
Std Dev 18.7
Turn on : 24.5608
Width : 2.650
Height : 10.010
Entry
ampl
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2
4
6
8
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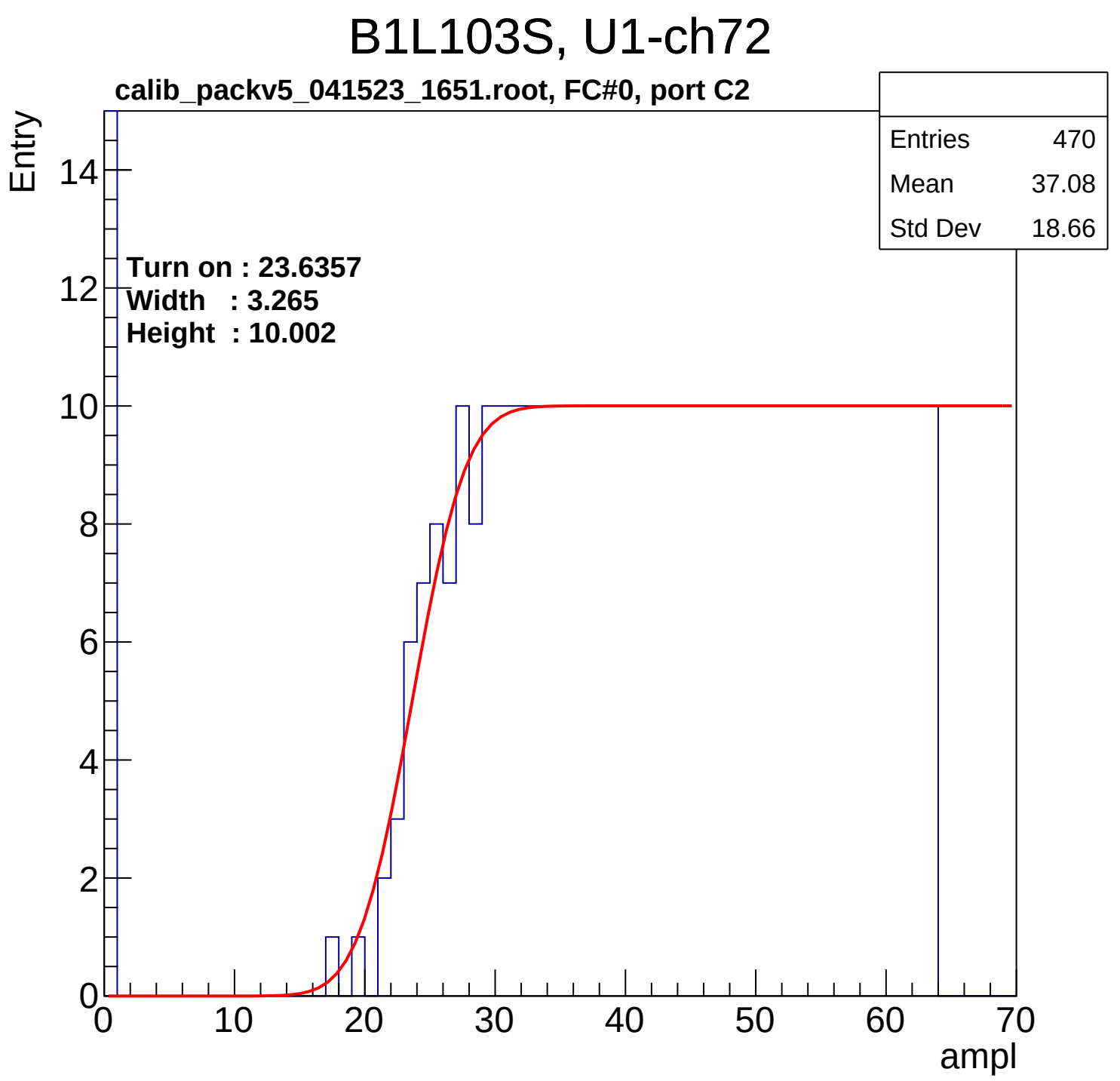
B1L103S, U1-ch72
calib_packv5_041523_1651.root, FC#0, port C2
Entries 470
Mean 37.08
Std Dev 18.66
Turn on : 23.6357
Width : 3.265
Height : 10.002
Entry
ampl
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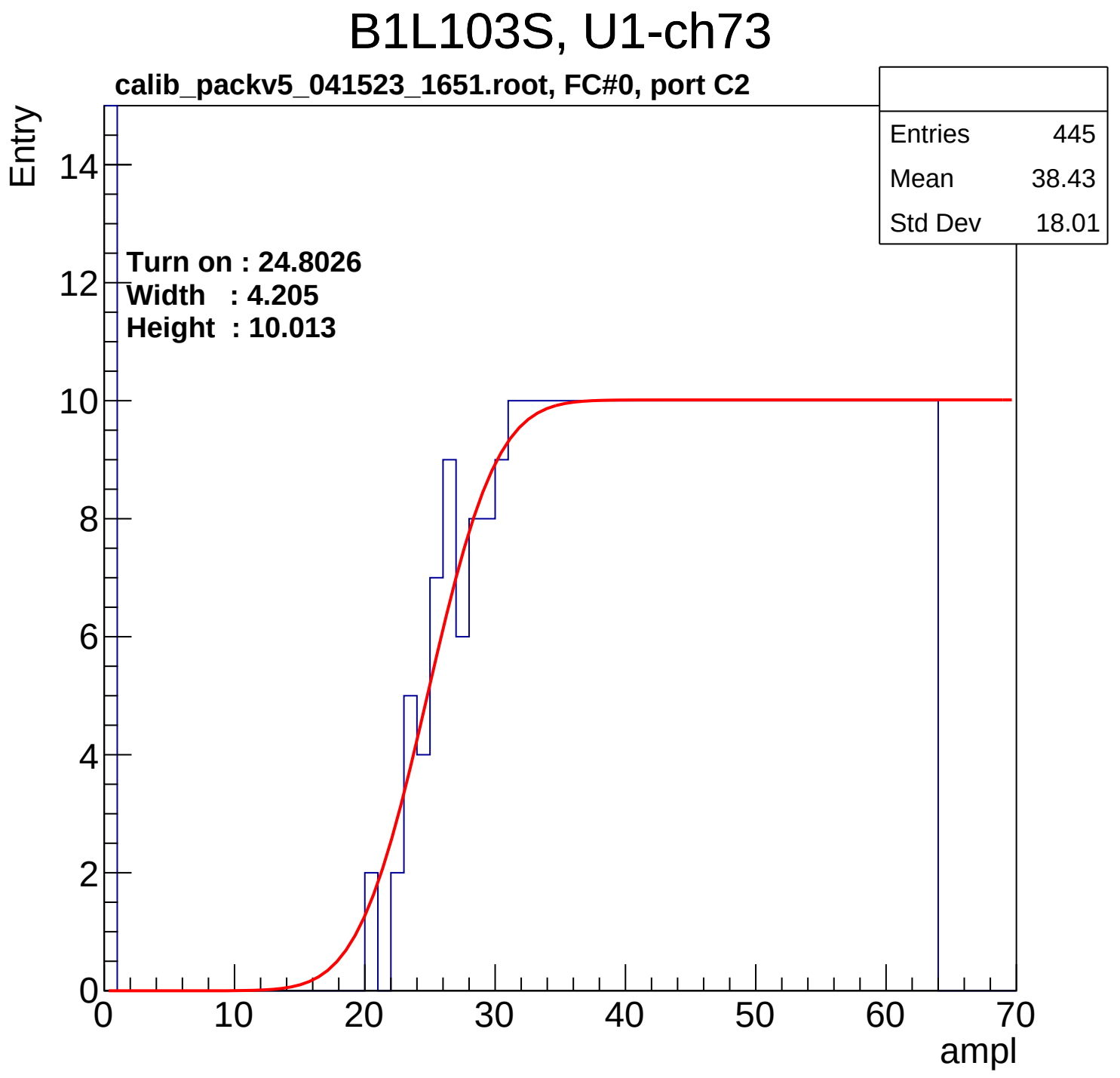
B1L103S, U1-ch73
calib_packv5_041523_1651.root, FC#0, port C2
Entries 445
Mean 38.43
Std Dev 18.01
Turn on : 24.8026
Width : 4.205
Height : 10.013
Entry
ampl
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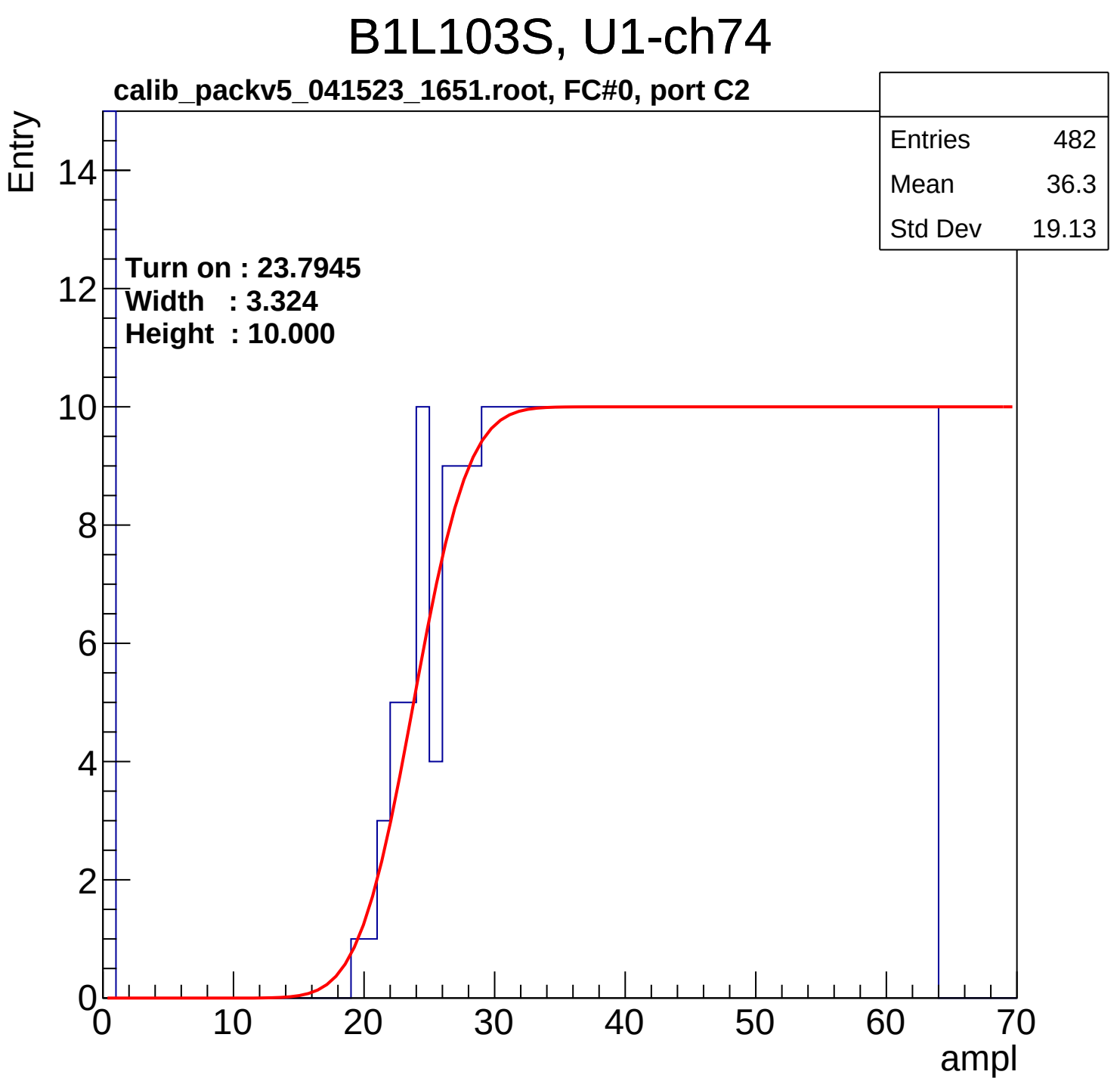
B1L103S, U1-ch74
calib_packv5_041523_1651.root, FC#0, port C2
Entries 482
Mean 36.3
Std Dev 19.13
Turn on : 23.7945
Width : 3.324
Height : 10.000
Entry
ampl
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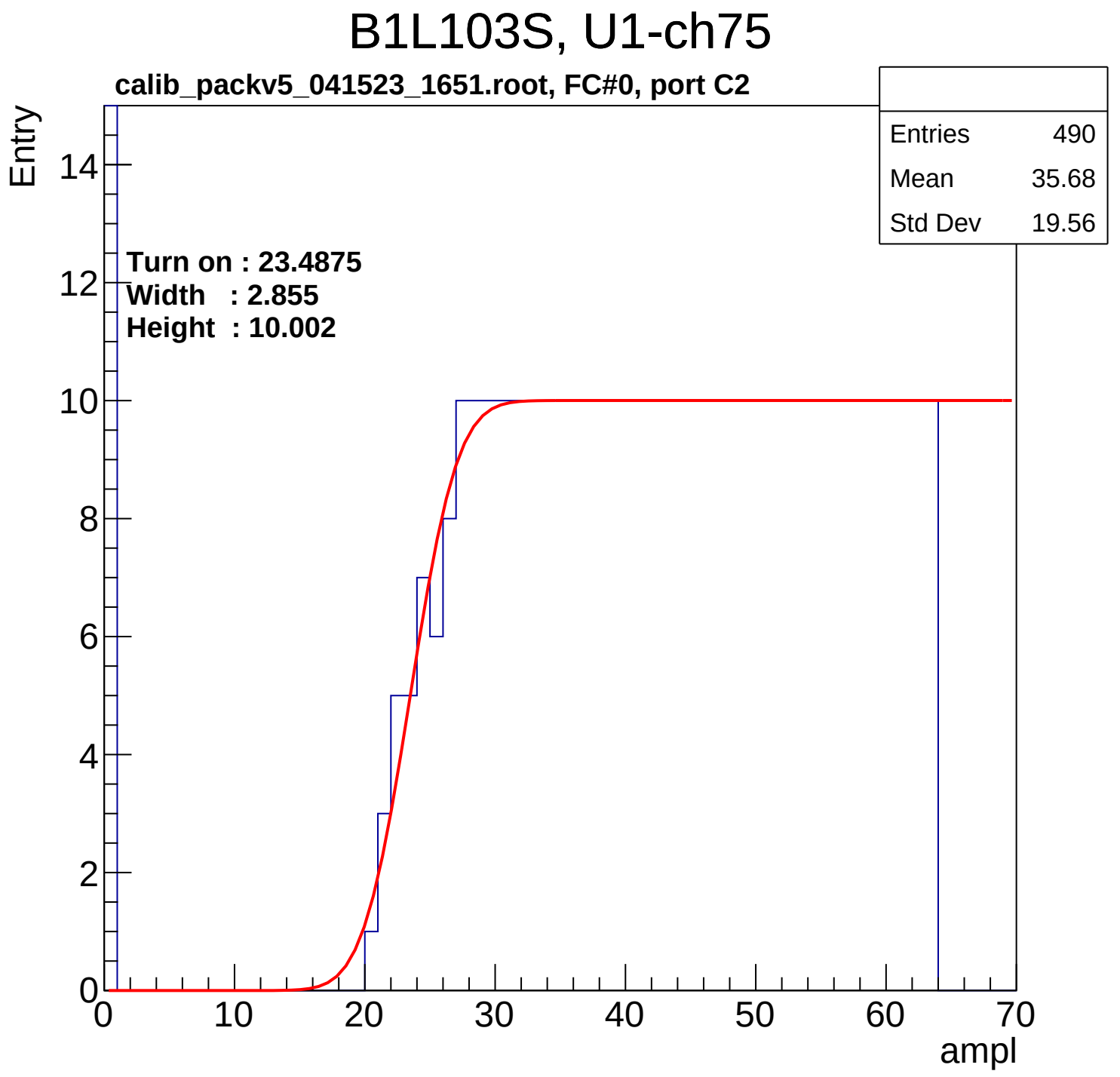
B1L103S, U1-ch75
calib_packv5_041523_1651.root, FC#0, port C2
Entries 490
Mean 35.68
Std Dev 19.56
Turn on : 23.4875
Width : 2.855
Height : 10.002
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ampl
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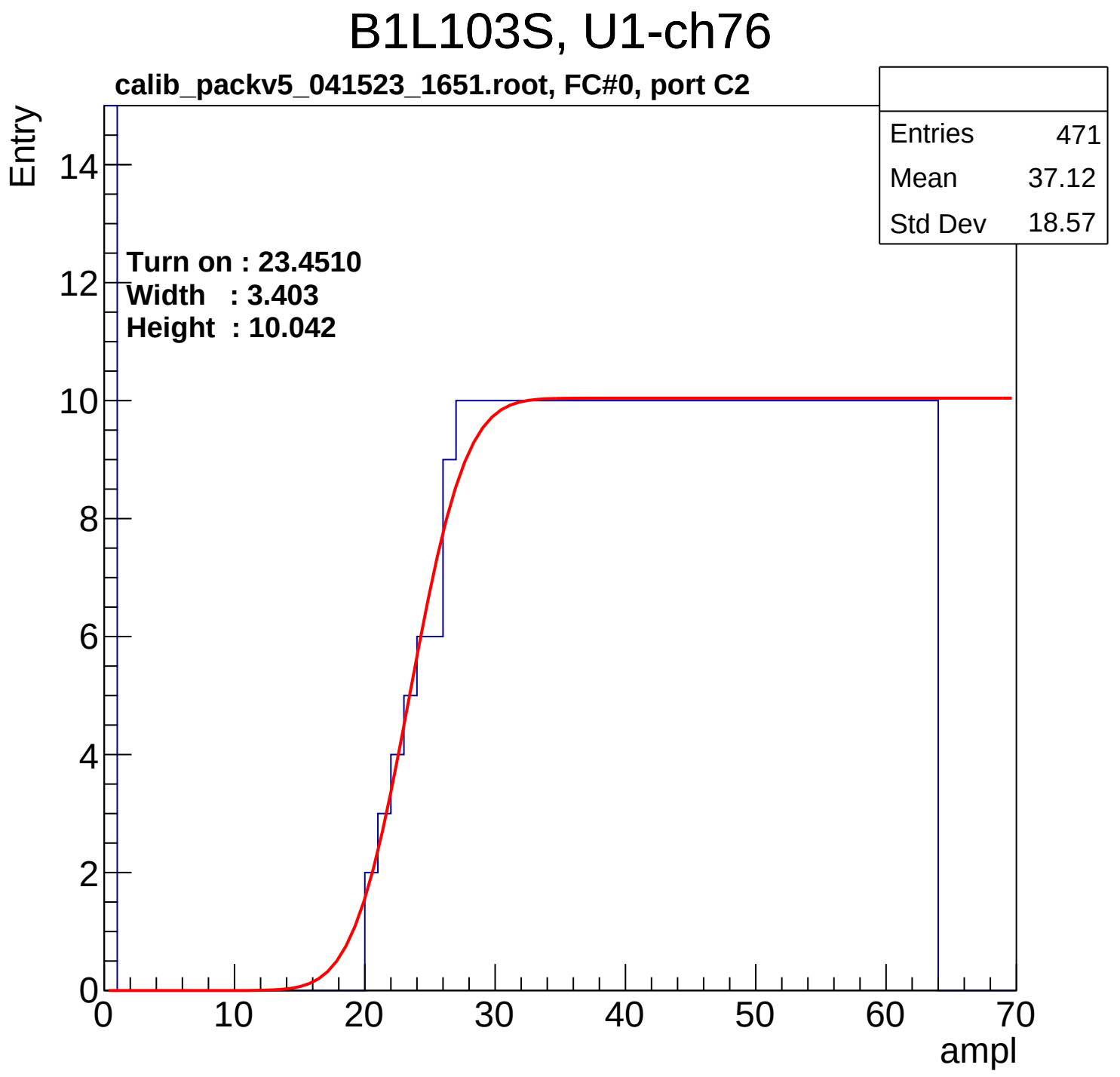
B1L103S, U1-ch76
calib_packv5_041523_1651.root, FC#0, port C2
Entries 471
Mean 37.12
Std Dev 18.57
Turn on : 23.4510
Width : 3.403
Height : 10.042
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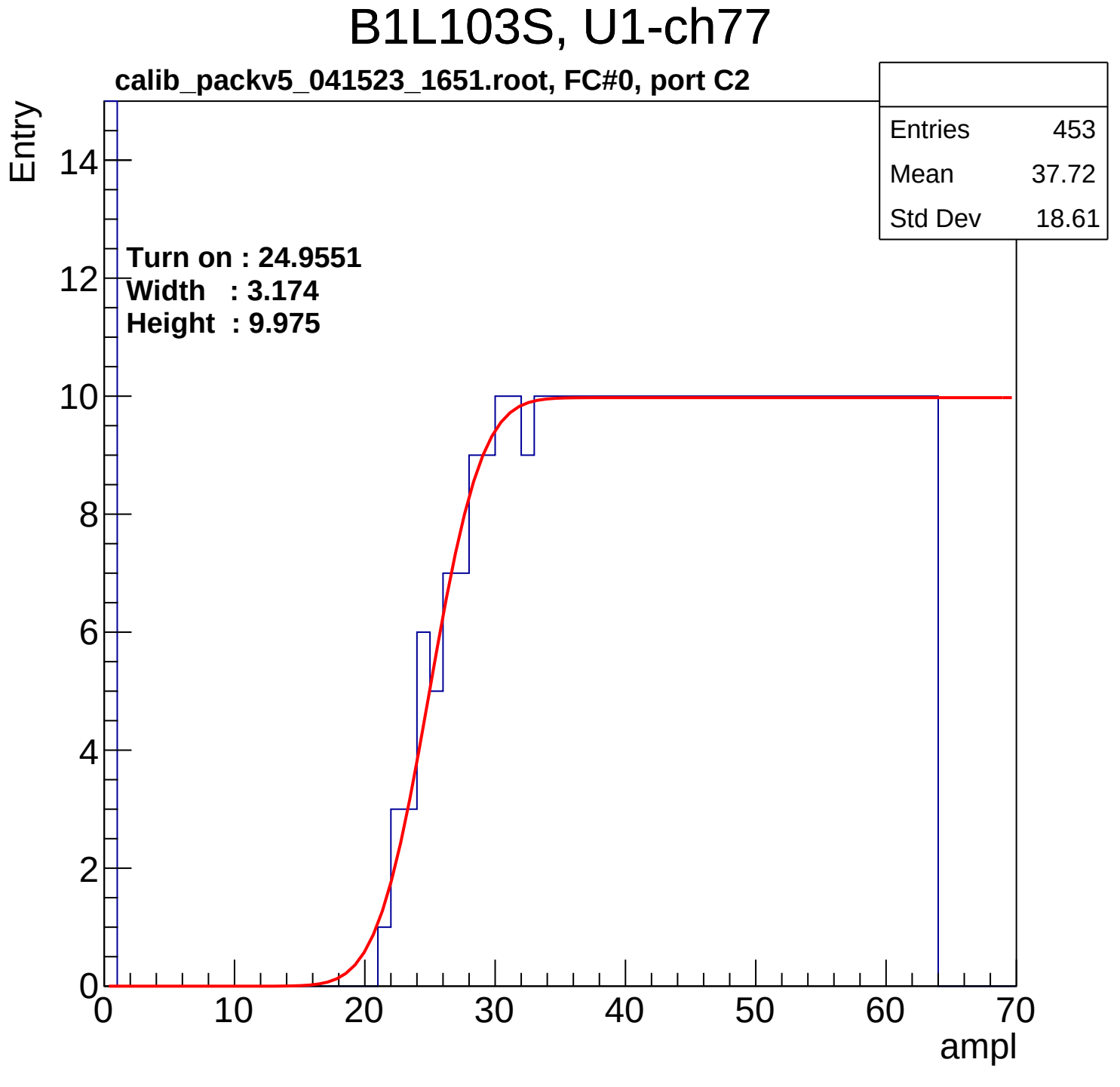
B1L103S, U1-ch77
calib_packv5_041523_1651.root, FC#0, port C2
Entries 453
Mean 37.72
Std Dev 18.61
Turn on : 24.9551
Width : 3.174
Height : 9.975
Entry
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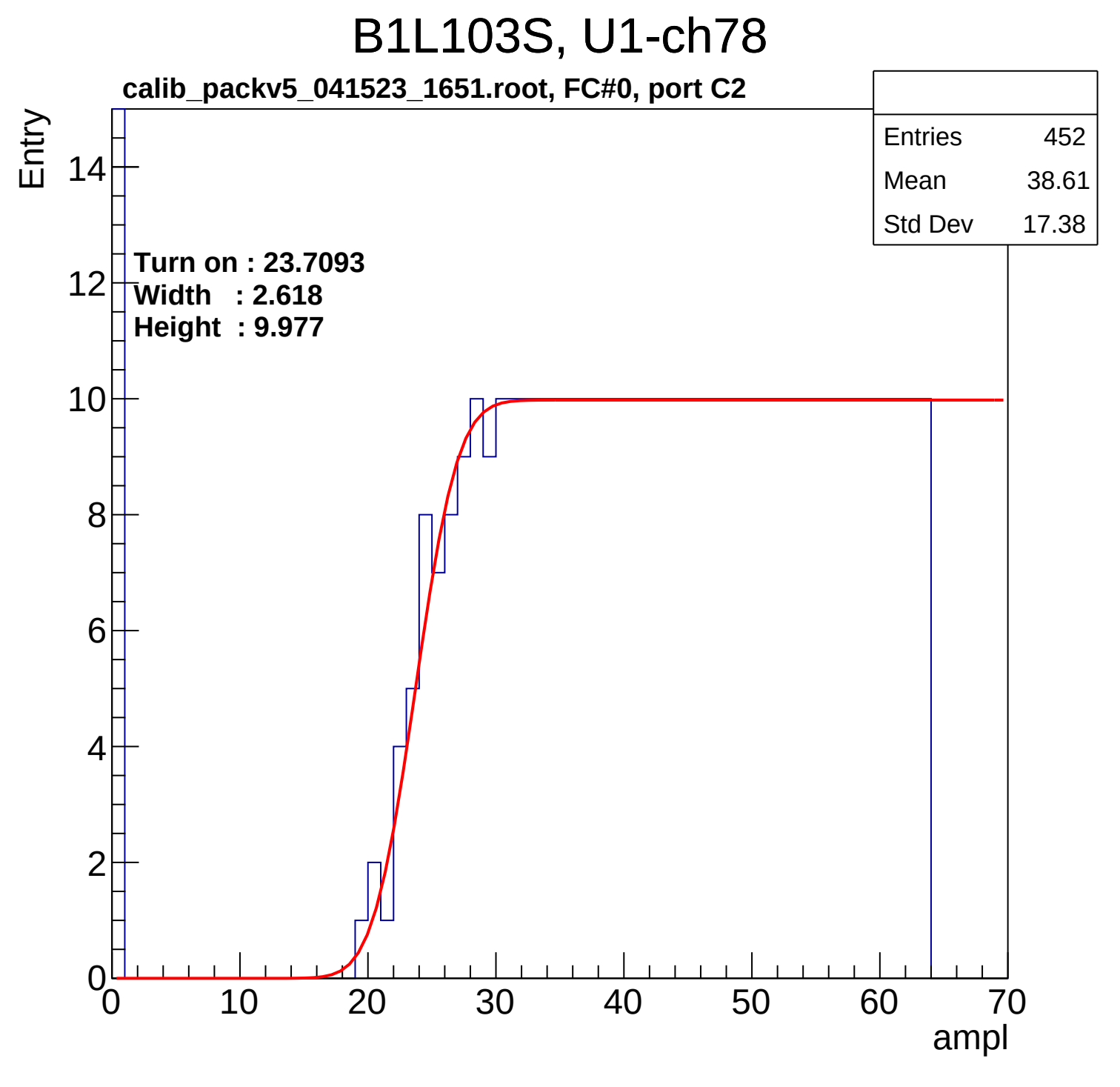
B1L103S, U1-ch78
calib_packv5_041523_1651.root, FC#0, port C2
Entries 452
Mean 38.61
Std Dev 17.38
Turn on : 23.7093
Width : 2.618
Height : 9.977
Entry
ampl
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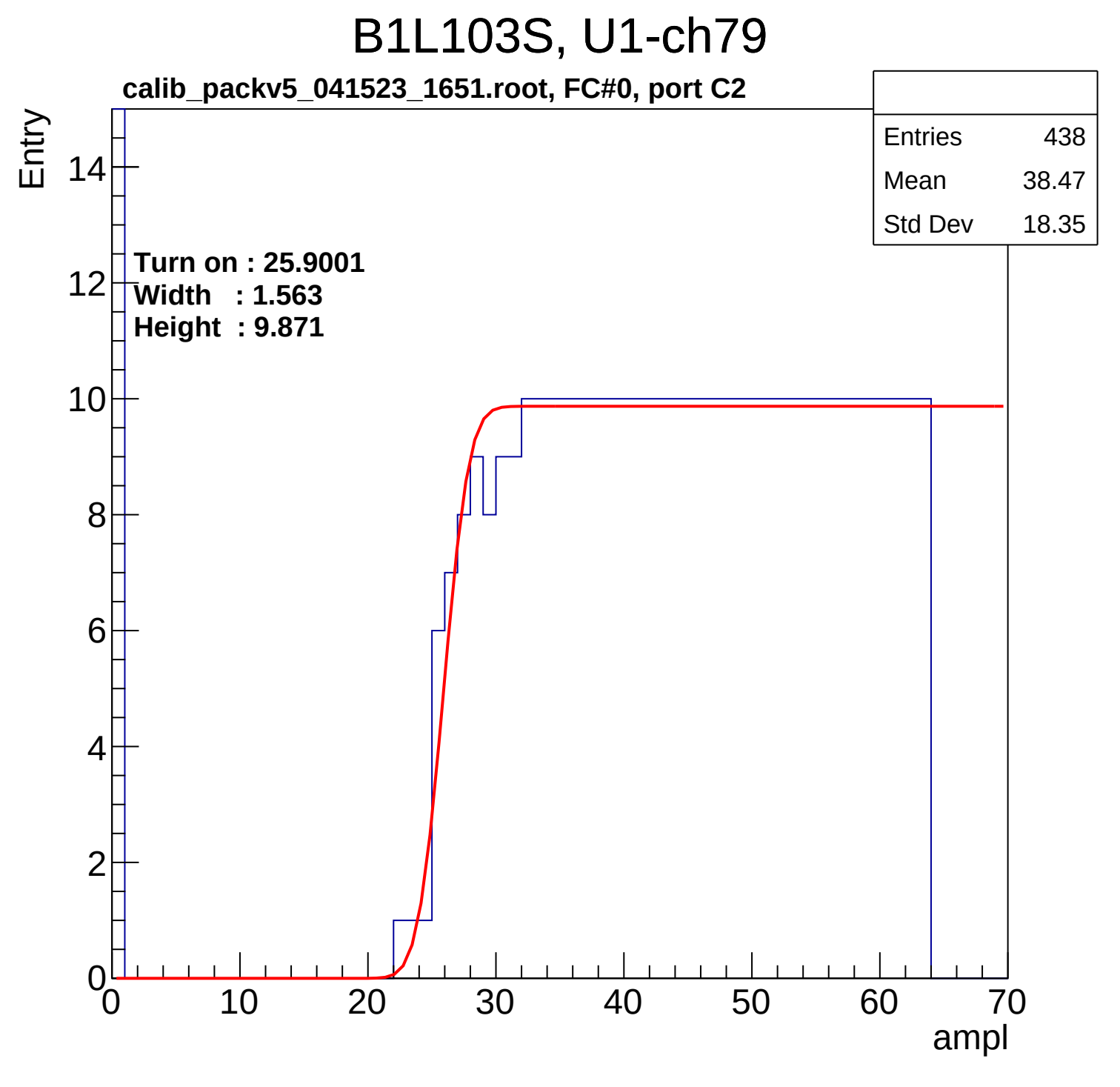
B1L103S, U1-ch79
calib_packv5_041523_1651.root, FC#0, port C2
Entries 438
Mean 38.47
Std Dev 18.35
Turn on : 25.9001
Width : 1.563
Height : 9.871
Entry
ampl
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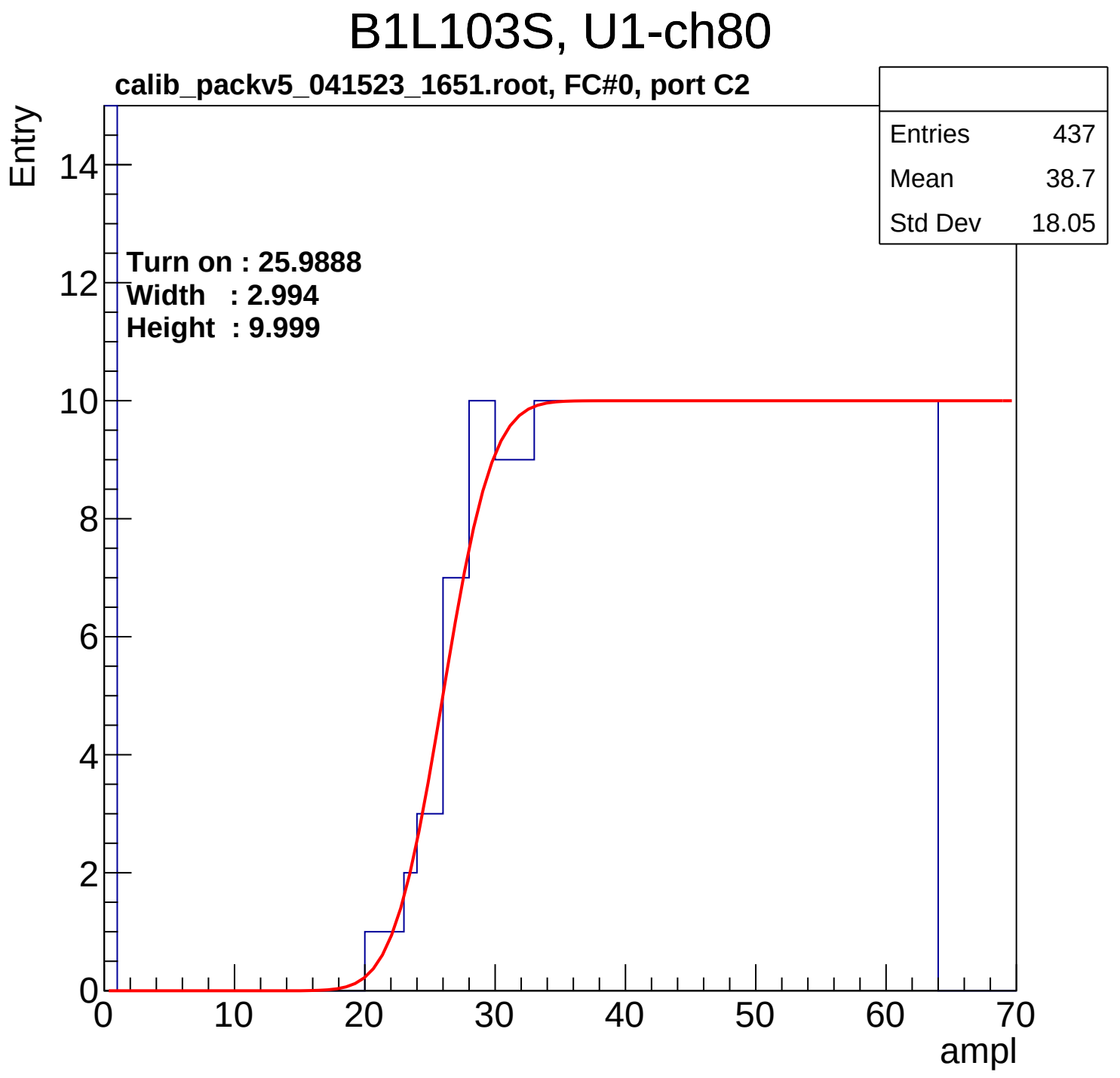
B1L103S, U1-ch80
calib_packv5_041523_1651.root, FC#0, port C2
Entries 437
Mean 38.7
Std Dev 18.05
Turn on : 25.9888
Width : 2.994
Height : 9.999
Entry
ampl
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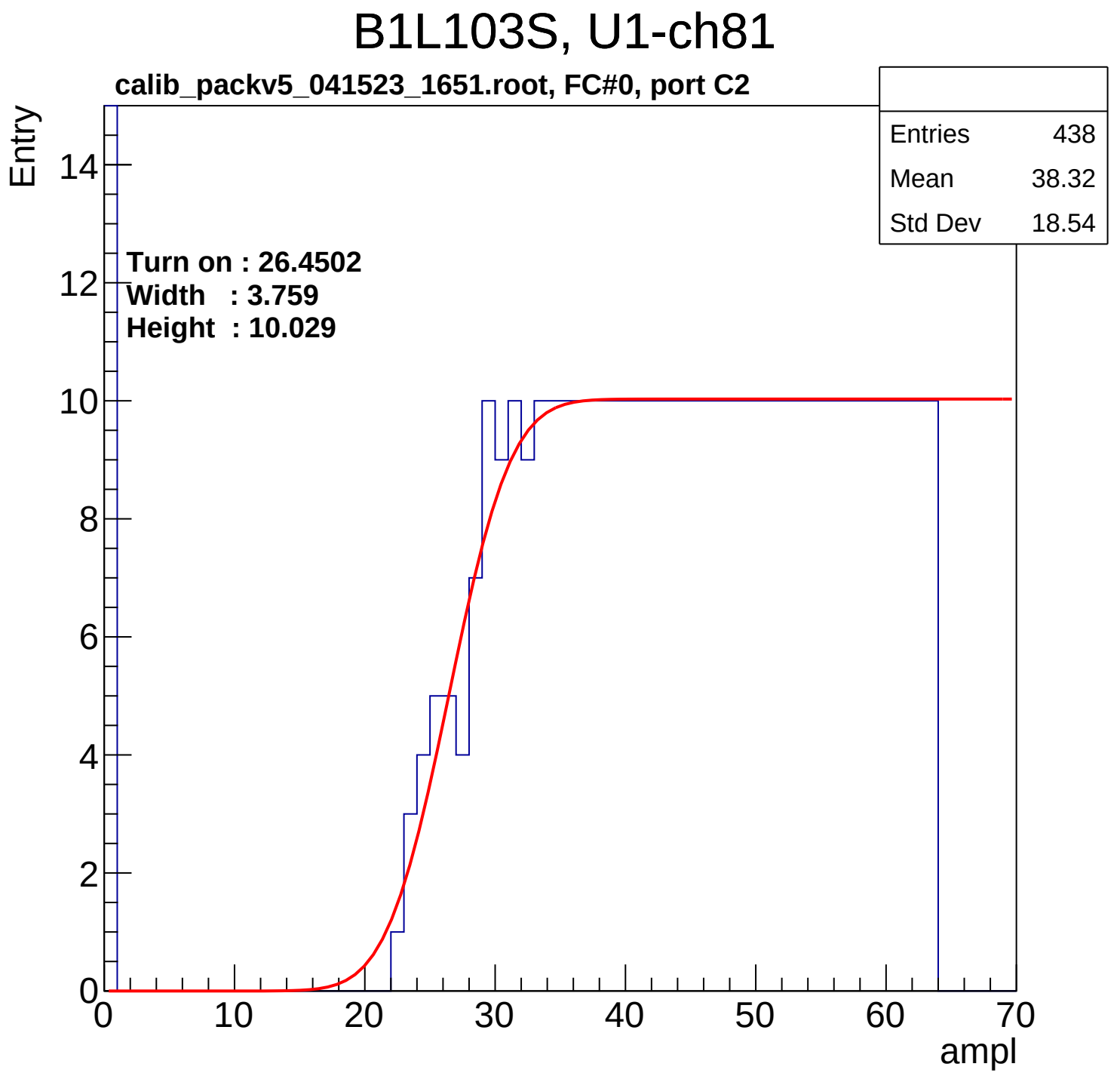
B1L103S, U1-ch81
calib_packv5_041523_1651.root, FC#0, port C2
Entries 438
Mean 38.32
Std Dev 18.54
Turn on : 26.4502
Width : 3.759
Height : 10.029
Entry
ampl
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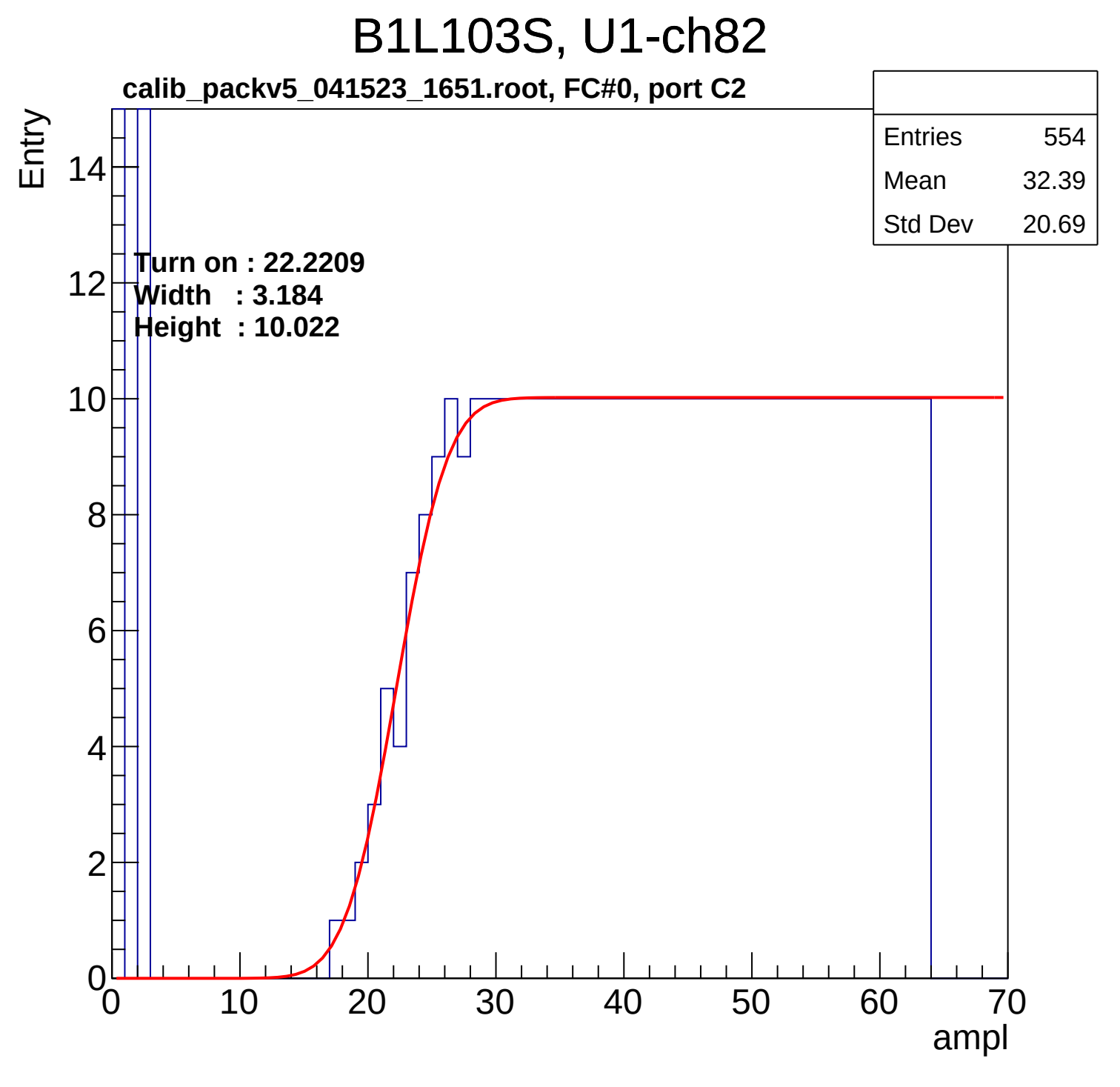
B1L103S, U1-ch82
calib_packv5_041523_1651.root, FC#0, port C2
Entries 554
Mean 32.39
Std Dev 20.69
Turn on : 22.2209
Width : 3.184
Height : 10.022
Entry
ampl
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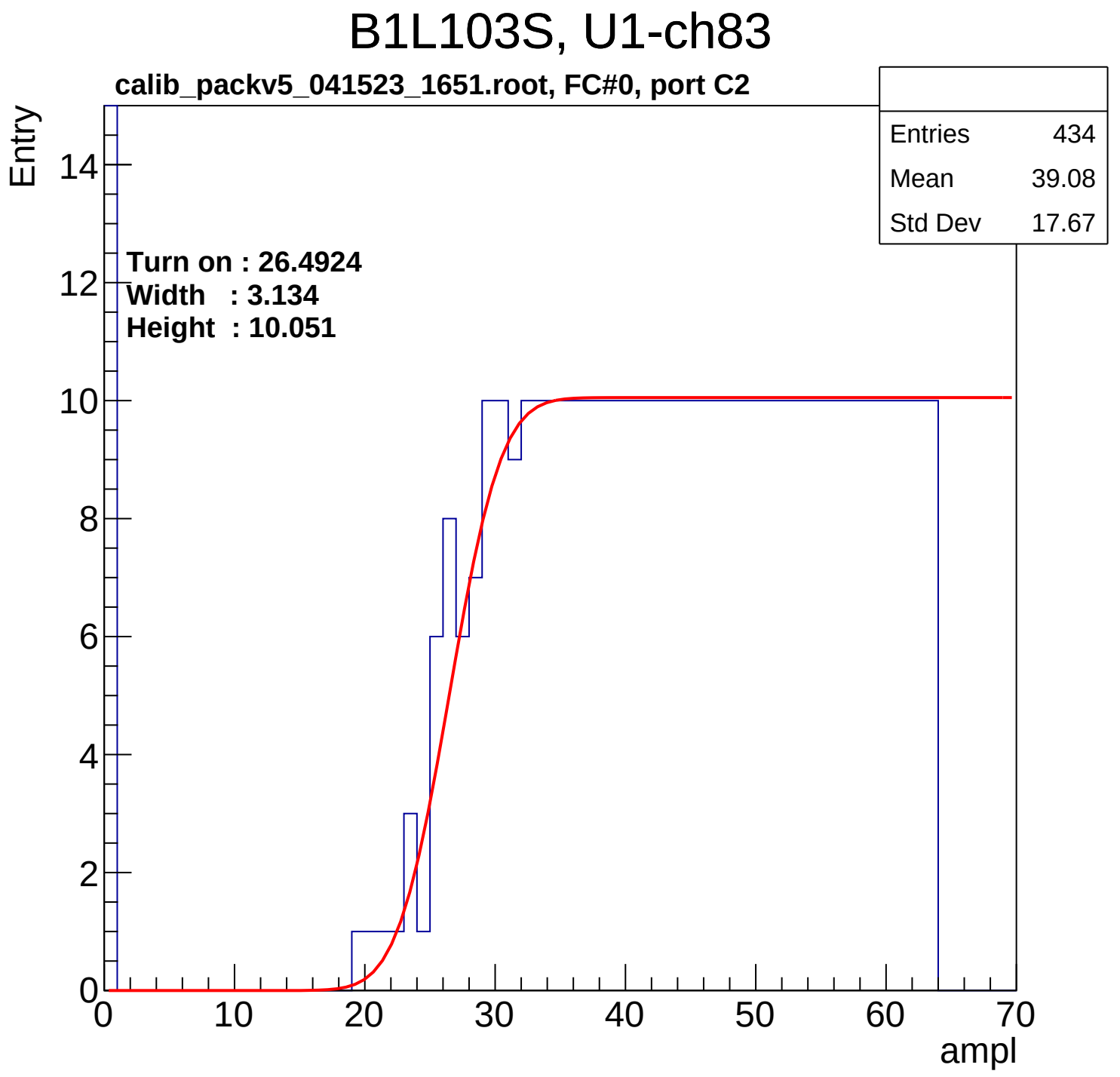
B1L103S, U1-ch83
calib_packv5_041523_1651.root, FC#0, port C2
Entries 434
Mean 39.08
Std Dev 17.67
Turn on : 26.4924
Width : 3.134
Height : 10.051
Entry
ampl
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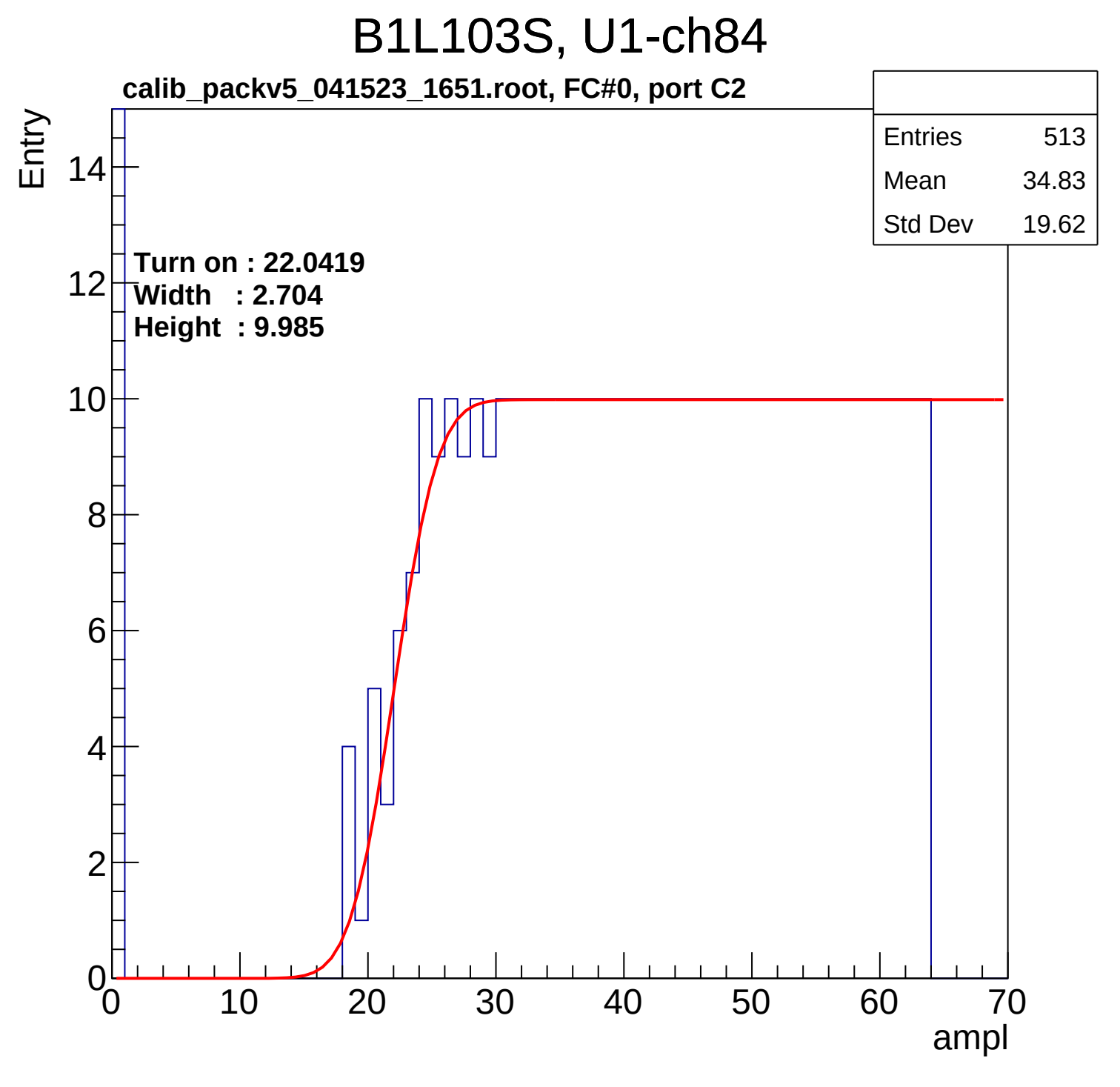
B1L103S, U1-ch84
calib_packv5_041523_1651.root, FC#0, port C2
Entries 513
Mean 34.83
Std Dev 19.62
Turn on : 22.0419
Width : 2.704
Height : 9.985
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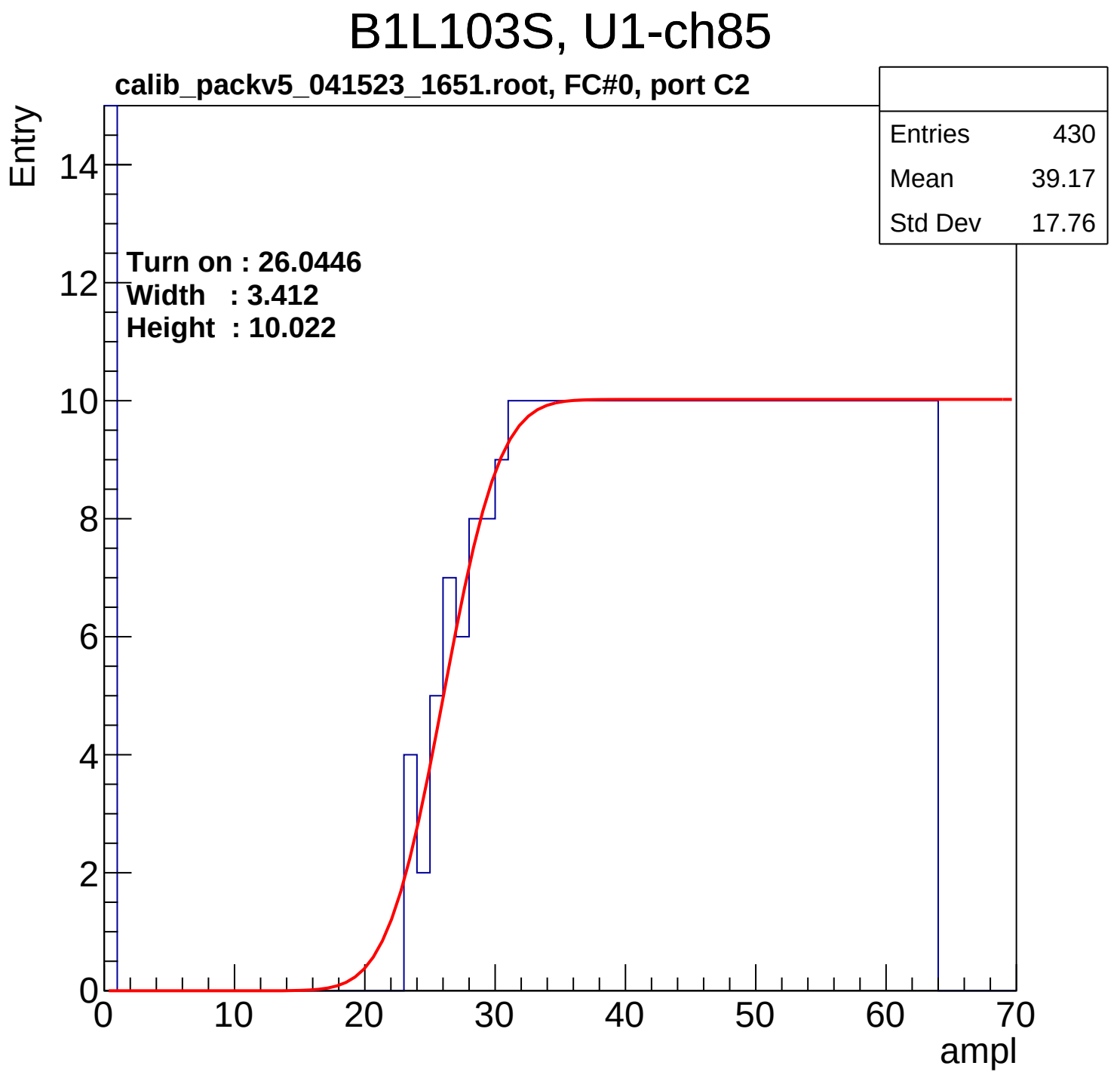
B1L103S, U1-ch85
calib_packv5_041523_1651.root, FC#0, port C2
Entries 430
Mean 39.17
Std Dev 17.76
Turn on : 26.0446
Width : 3.412
Height : 10.022
Entry
ampl
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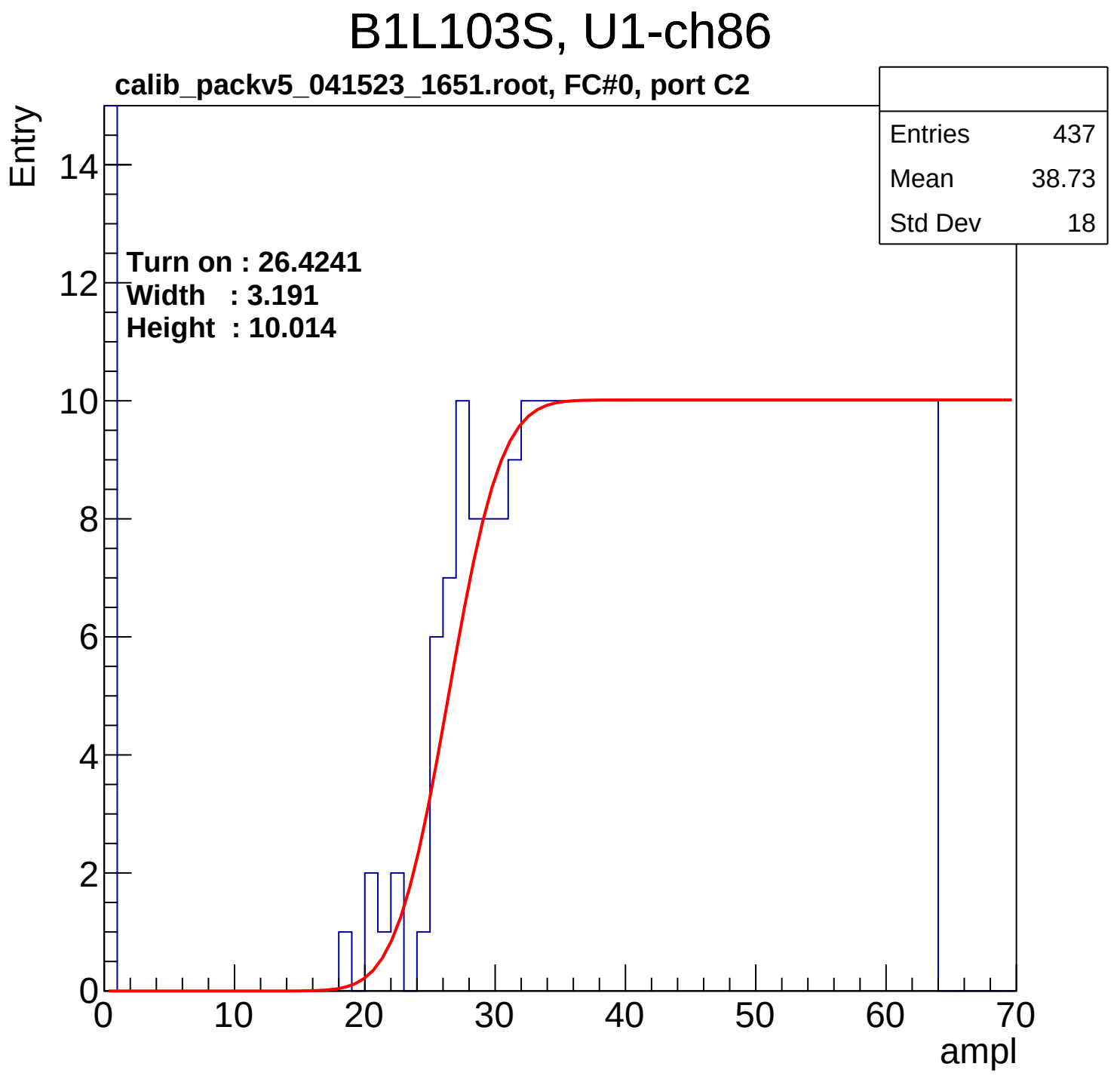
B1L103S, U1-ch86
calib_packv5_041523_1651.root, FC#0, port C2
Entries 437
Mean 38.73
Std Dev 18
Turn on : 26.4241
Width : 3.191
Height : 10.014
Entry
ampl
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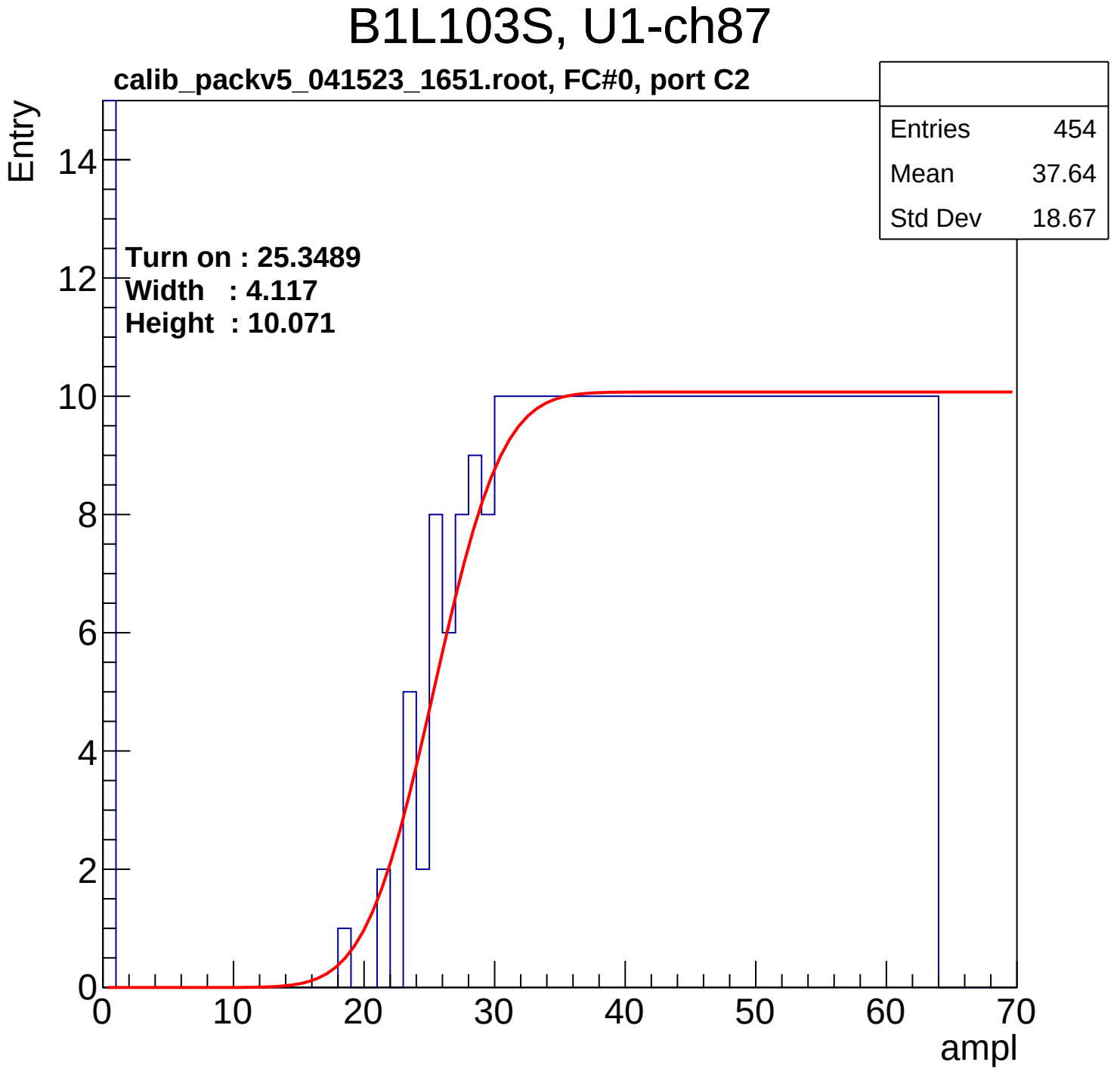
B1L103S, U1-ch87
calib_packv5_041523_1651.root, FC#0, port C2
Entries 454
Mean 37.64
Std Dev 18.67
Turn on : 25.3489
Width : 4.117
Height : 10.071
Entry
ampl
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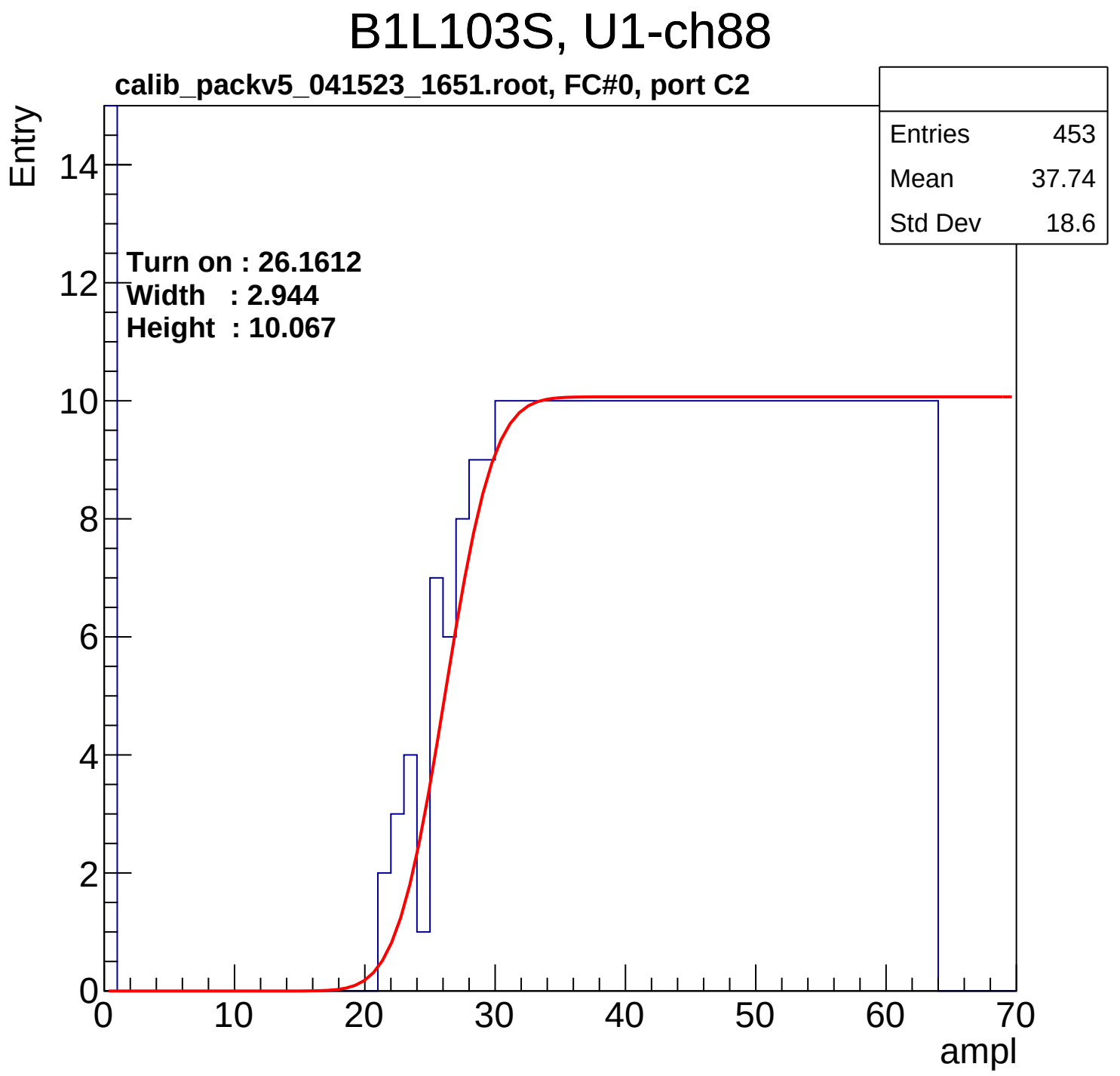
B1L103S, U1-ch88
calib_packv5_041523_1651.root, FC#0, port C2
Entries 453
Mean 37.74
Std Dev 18.6
Turn on : 26.1612
Width : 2.944
Height : 10.067
Entry
ampl
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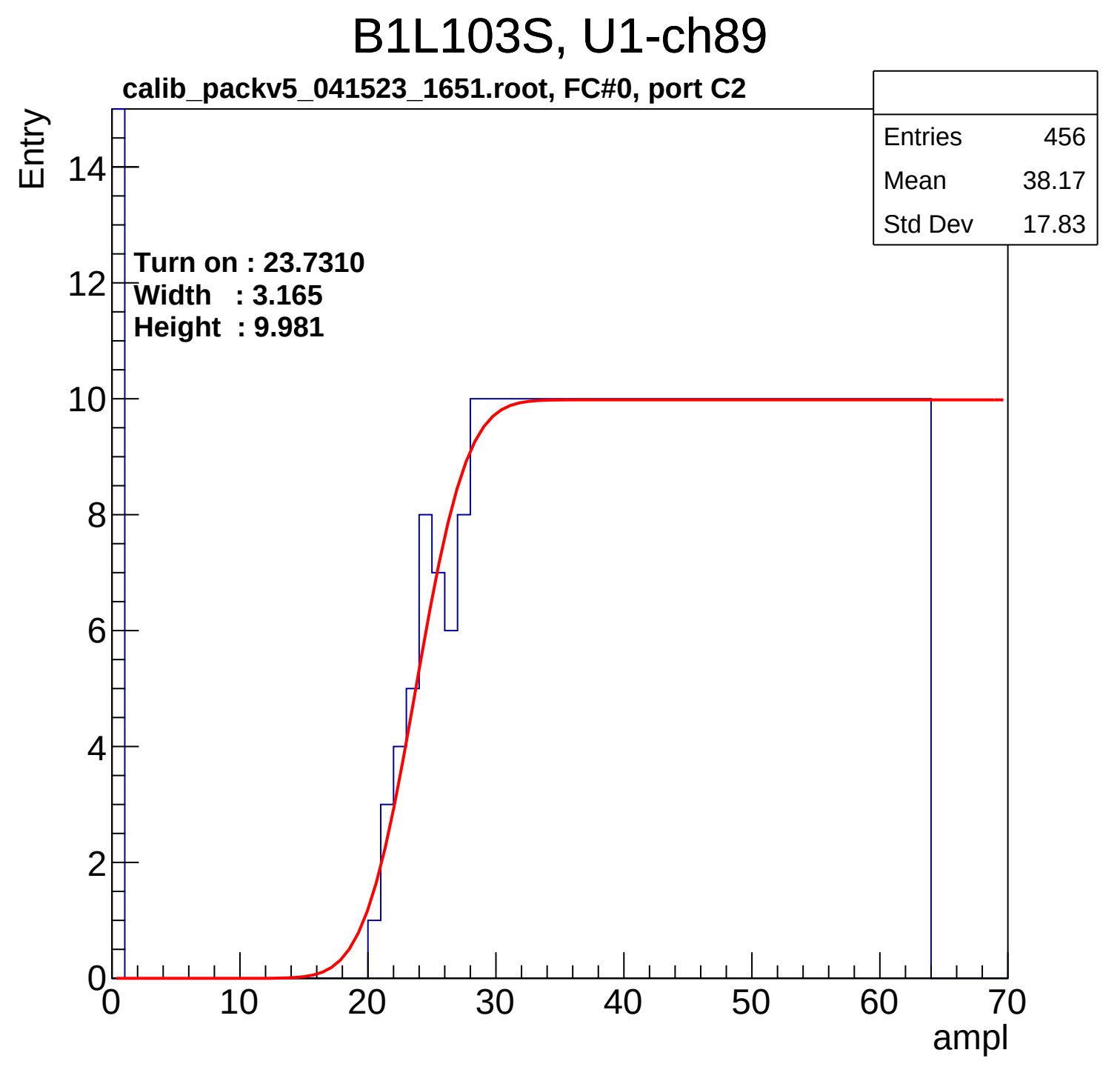
B1L103S, U1-ch89
calib_packv5_041523_1651.root, FC#0, port C2
Entries 456
Mean 38.17
Std Dev 17.83
Turn on : 23.7310
Width : 3.165
Height : 9.981
Entry
ampl
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2
4
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8
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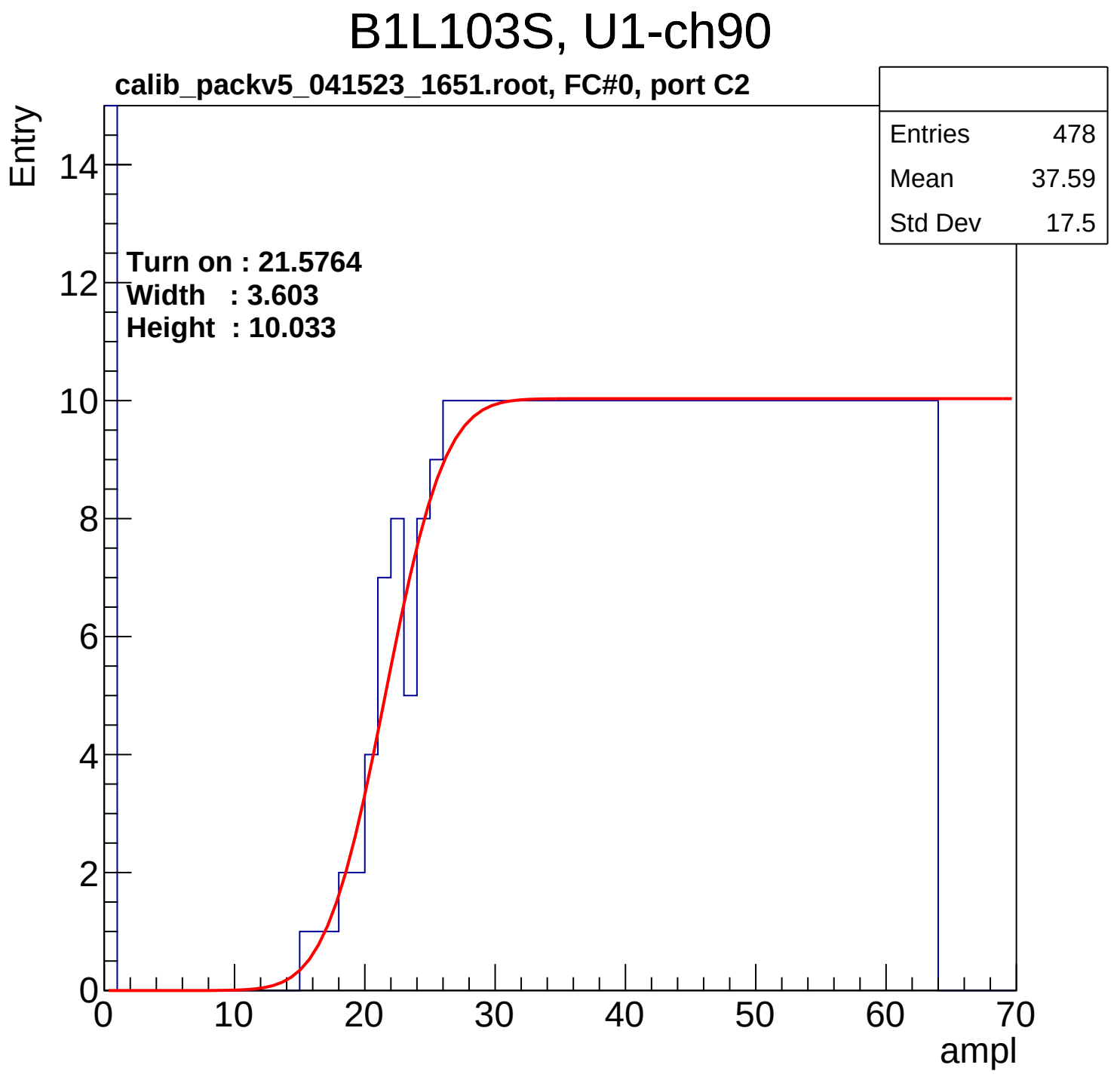
B1L103S, U1-ch90
calib_packv5_041523_1651.root, FC#0, port C2
Entries 478
Mean 37.59
Std Dev 17.5
Turn on : 21.5764
Width : 3.603
Height : 10.033
Entry
ampl
0
2
4
6
8
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12
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0
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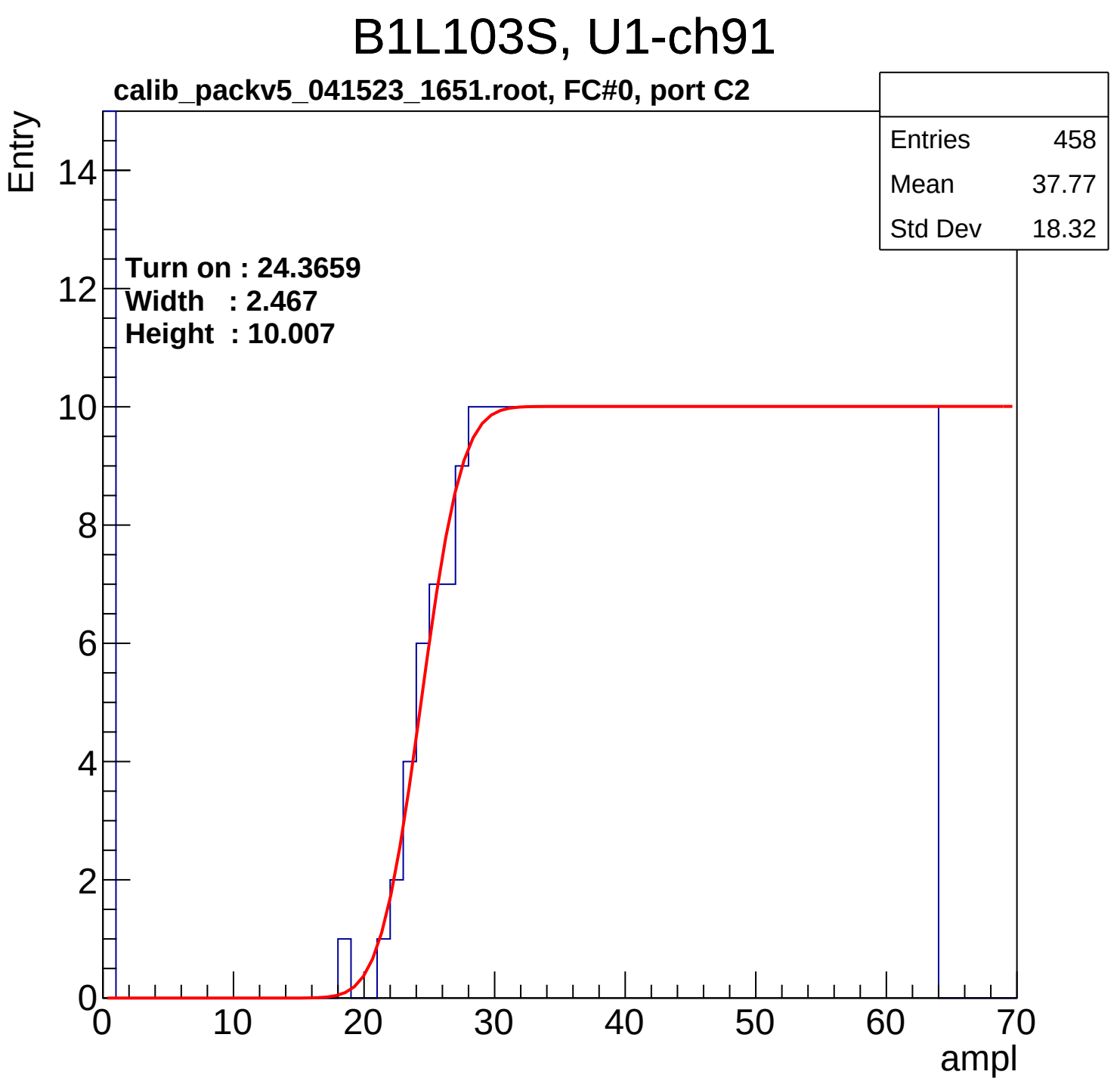
B1L103S, U1-ch91
calib_packv5_041523_1651.root, FC#0, port C2
Entries 458
Mean 37.77
Std Dev 18.32
Turn on : 24.3659
Width : 2.467
Height : 10.007
Entry
ampl
0
2
4
6
8
10
12
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0
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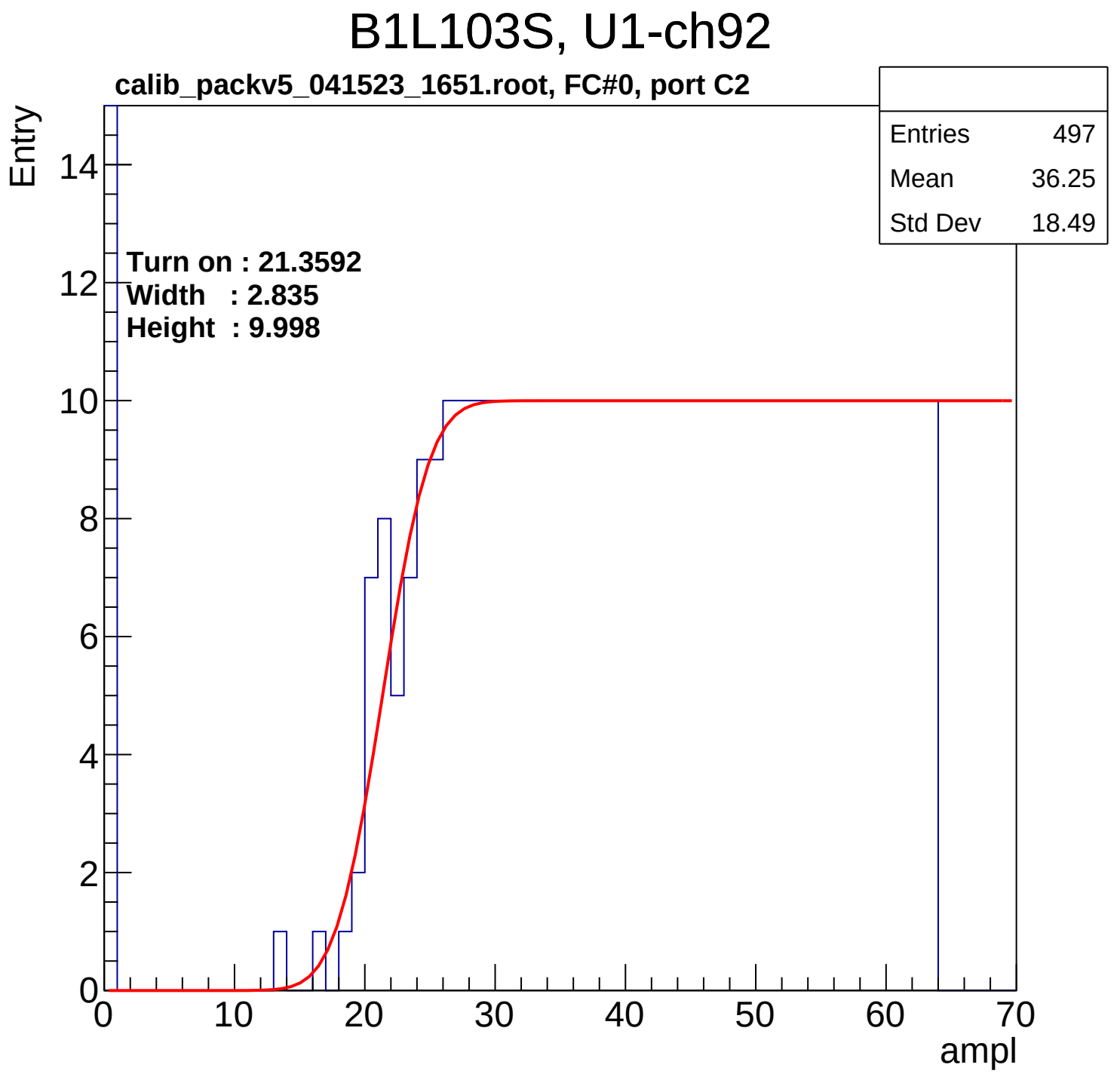
B1L103S, U1-ch92
calib_packv5_041523_1651.root, FC#0, port C2
Entries 497
Mean 36.25
Std Dev 18.49
Turn on : 21.3592
Width : 2.835
Height : 9.998
Entry
ampl
0
2
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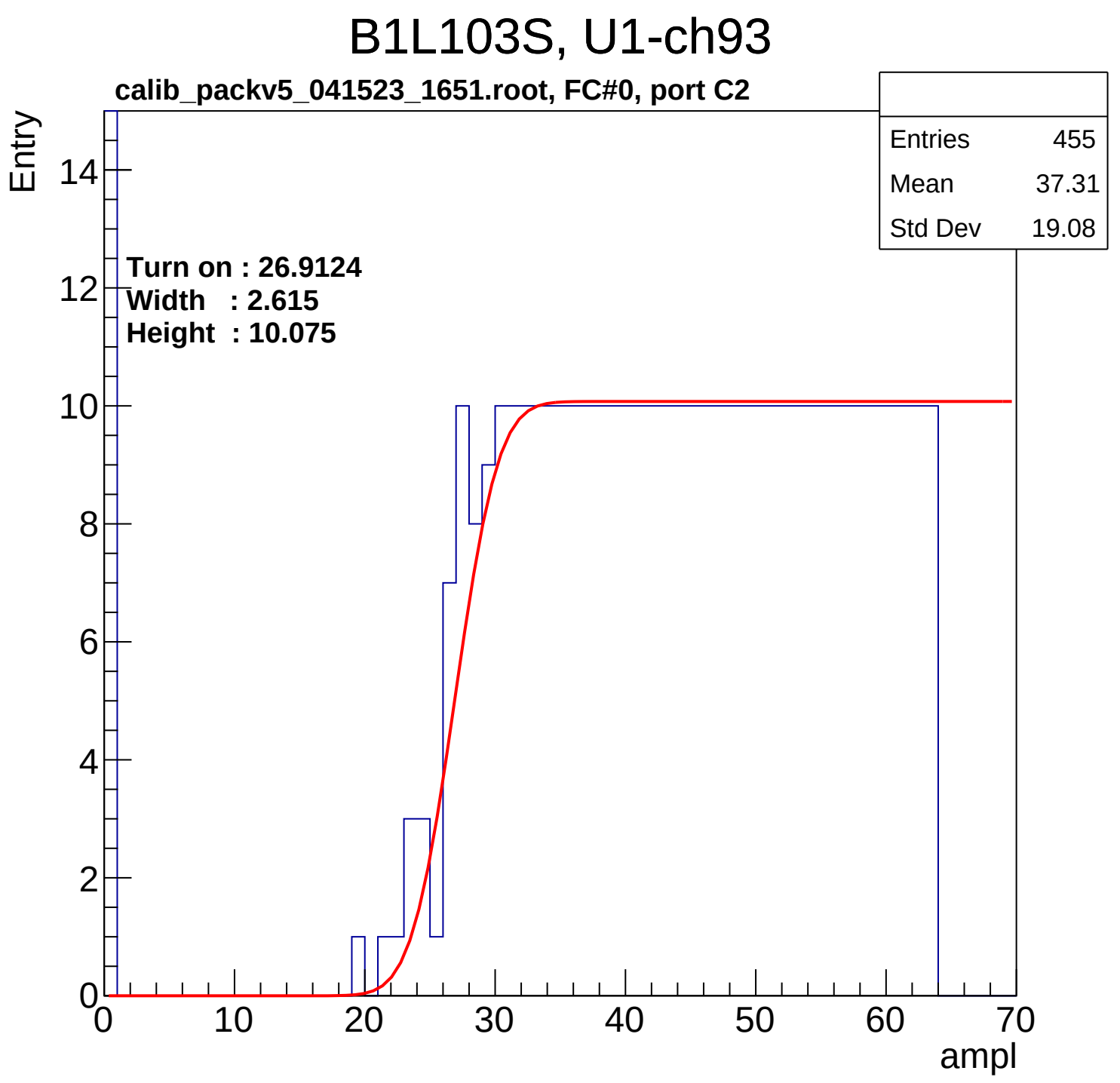
B1L103S, U1-ch93
calib_packv5_041523_1651.root, FC#0, port C2
Entries 455
Mean 37.31
Std Dev 19.08
Turn on : 26.9124
Width : 2.615
Height : 10.075
Entry
ampl
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4
6
8
10
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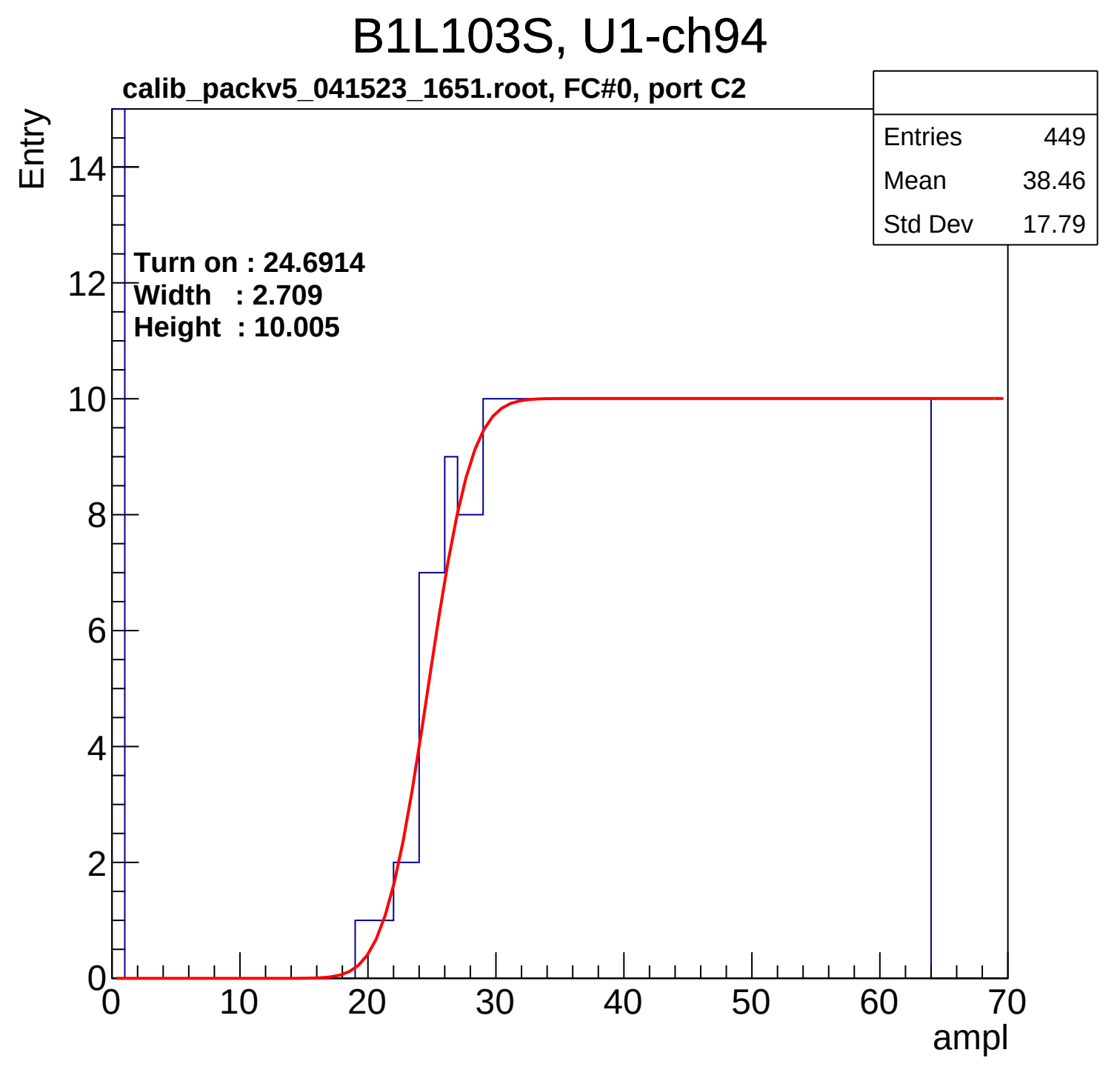
B1L103S, U1-ch94
calib_packv5_041523_1651.root, FC#0, port C2
Entries 449
Mean 38.46
Std Dev 17.79
Turn on : 24.6914
Width : 2.709
Height : 10.005
Entry
ampl
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6
8
10
12
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0
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60
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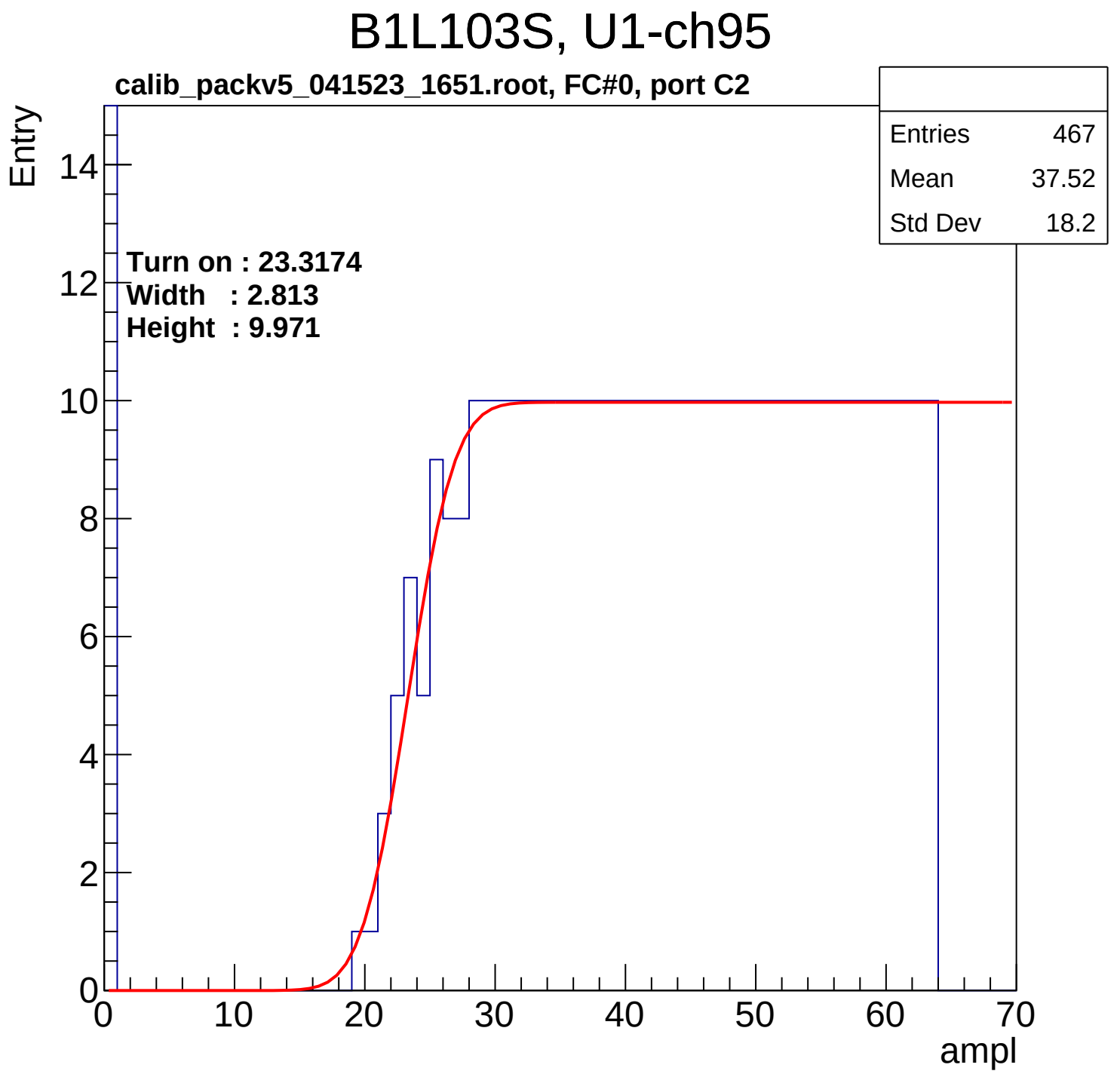
B1L103S, U1-ch95
calib_packv5_041523_1651.root, FC#0, port C2
Entries 467
Mean 37.52
Std Dev 18.2
Turn on : 23.3174
Width : 2.813
Height : 9.971
Entry
ampl
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2
4
6
8
10
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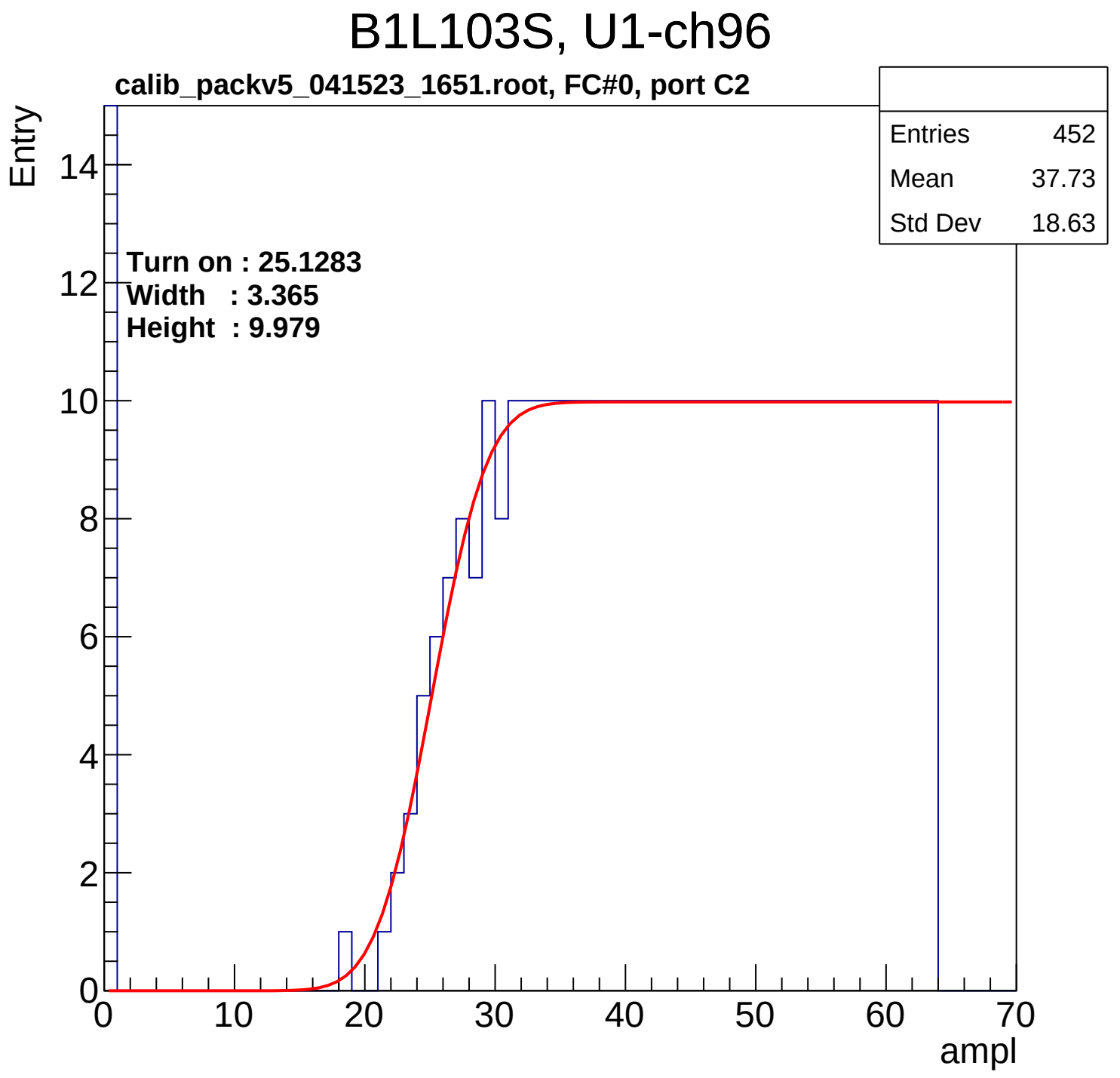
B1L103S, U1-ch96
calib_packv5_041523_1651.root, FC#0, port C2
Entries 452
Mean 37.73
Std Dev 18.63
Turn on : 25.1283
Width : 3.365
Height : 9.979
Entry
ampl
0
2
4
6
8
10
12
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20
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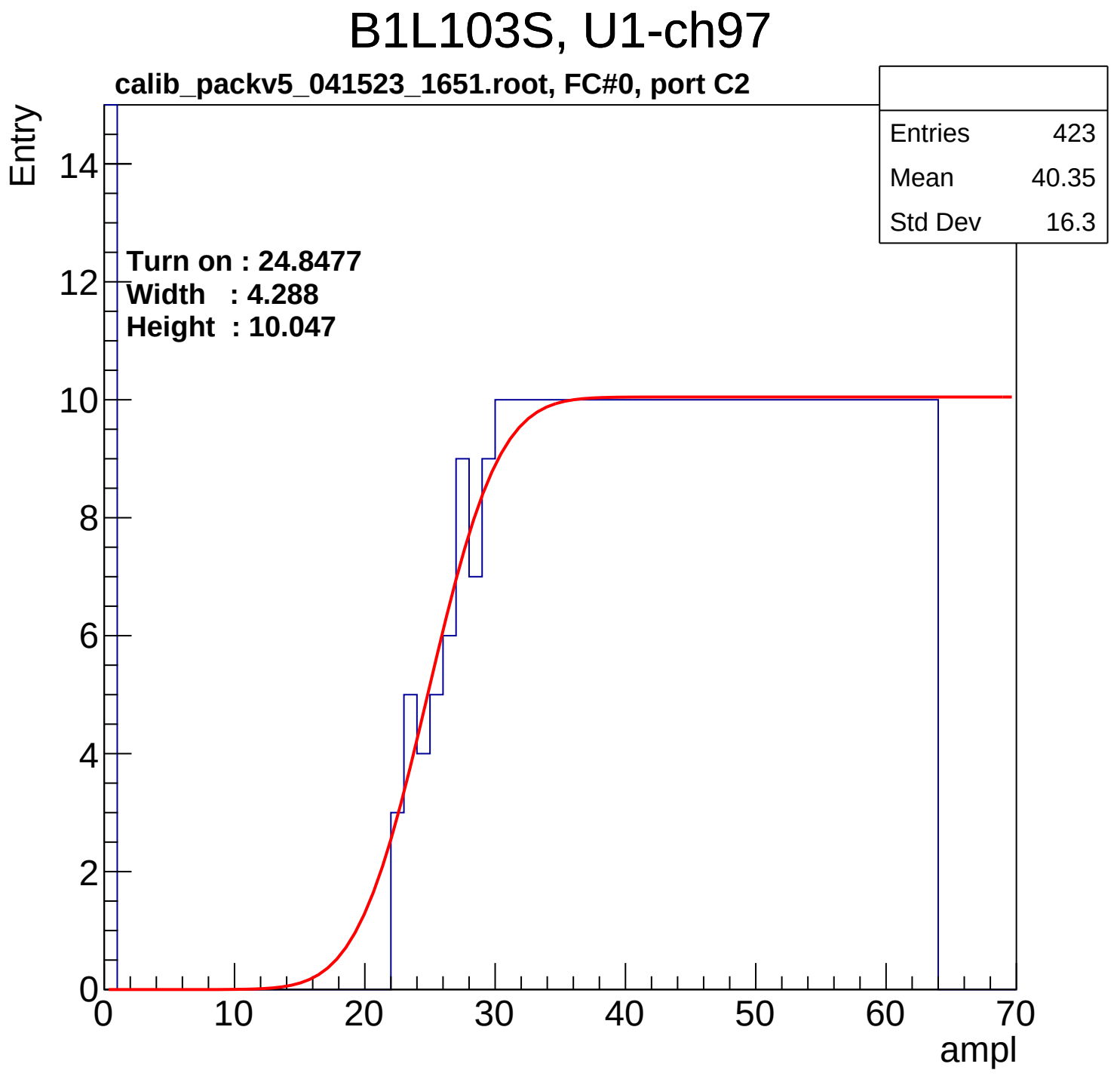
B1L103S, U1-ch97
calib_packv5_041523_1651.root, FC#0, port C2
Entries 423
Mean 40.35
Std Dev 16.3
Turn on : 24.8477
Width : 4.288
Height : 10.047
Entry
ampl
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4
6
8
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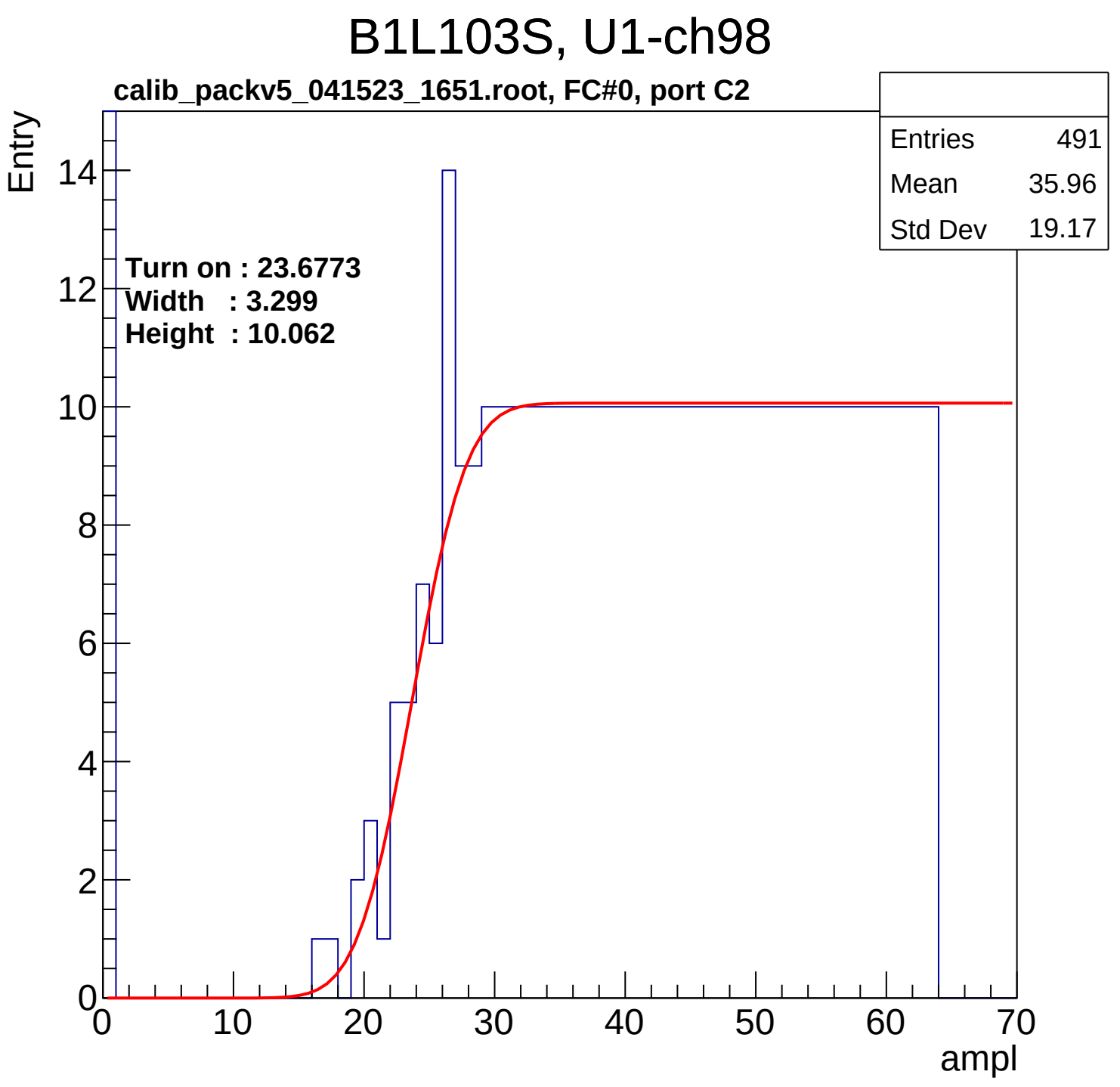
B1L103S, U1-ch98
calib_packv5_041523_1651.root, FC#0, port C2
Entries 491
Mean 35.96
Std Dev 19.17
Turn on : 23.6773
Width : 3.299
Height : 10.062
Entry
ampl
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6
8
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12
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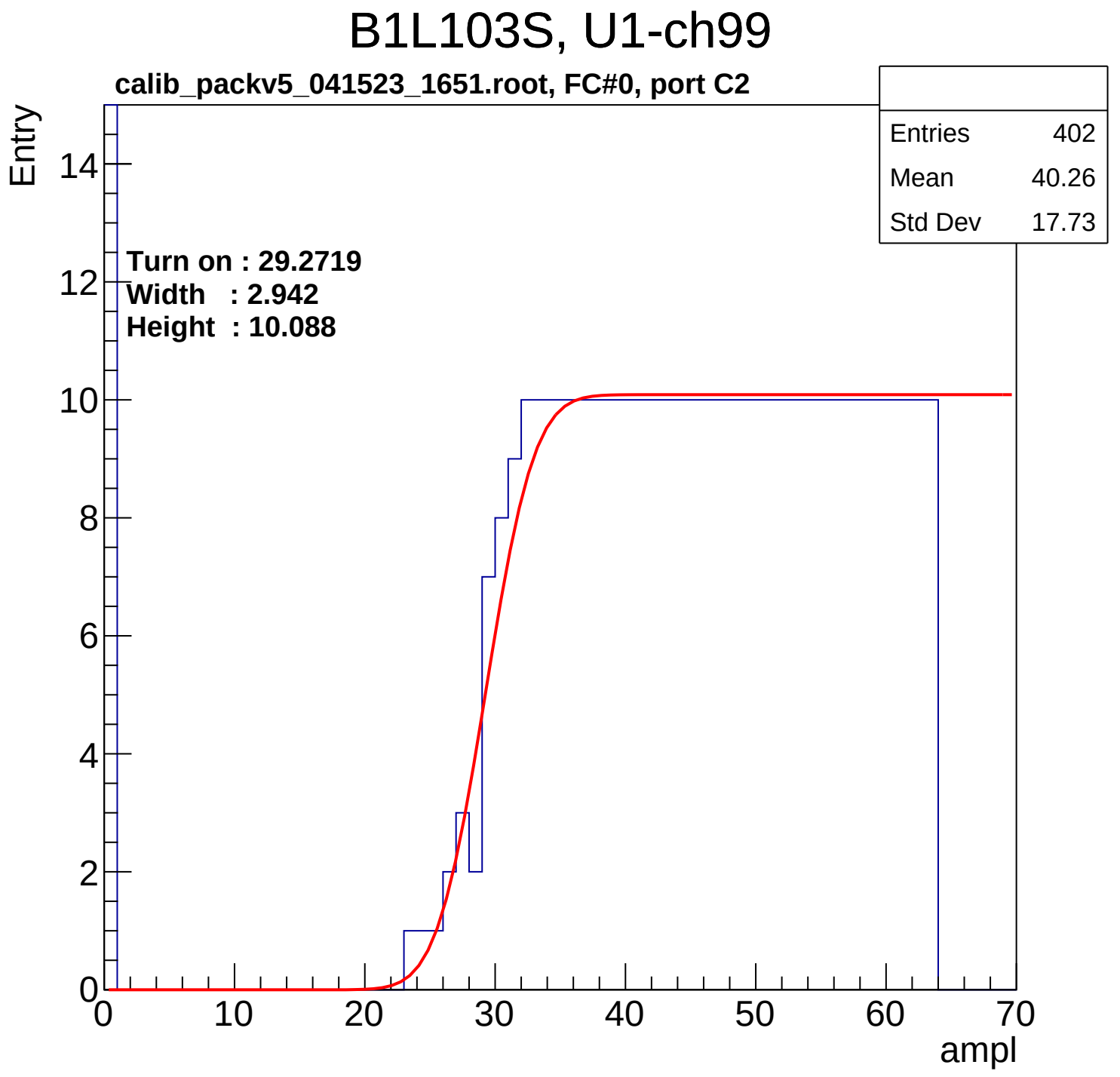
B1L103S, U1-ch99
calib_packv5_041523_1651.root, FC#0, port C2
Entries 402
Mean 40.26
Std Dev 17.73
Turn on : 29.2719
Width : 2.942
Height : 10.088
Entry
ampl
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2
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6
8
10
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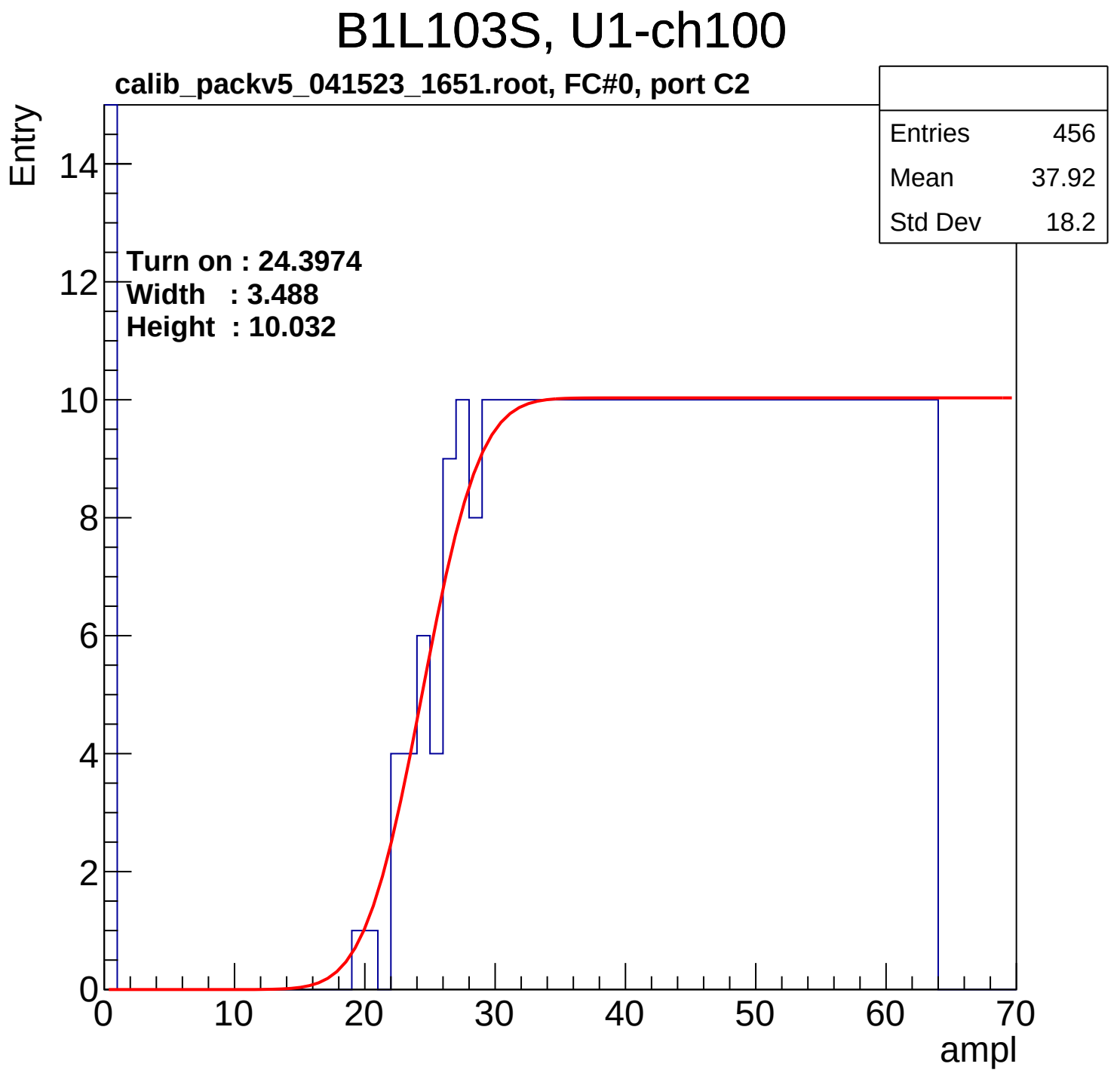
B1L103S, U1-ch100
calib_packv5_041523_1651.root, FC#0, port C2
Entries 456
Mean 37.92
Std Dev 18.2
Turn on : 24.3974
Width : 3.488
Height : 10.032
Entry
ampl
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6
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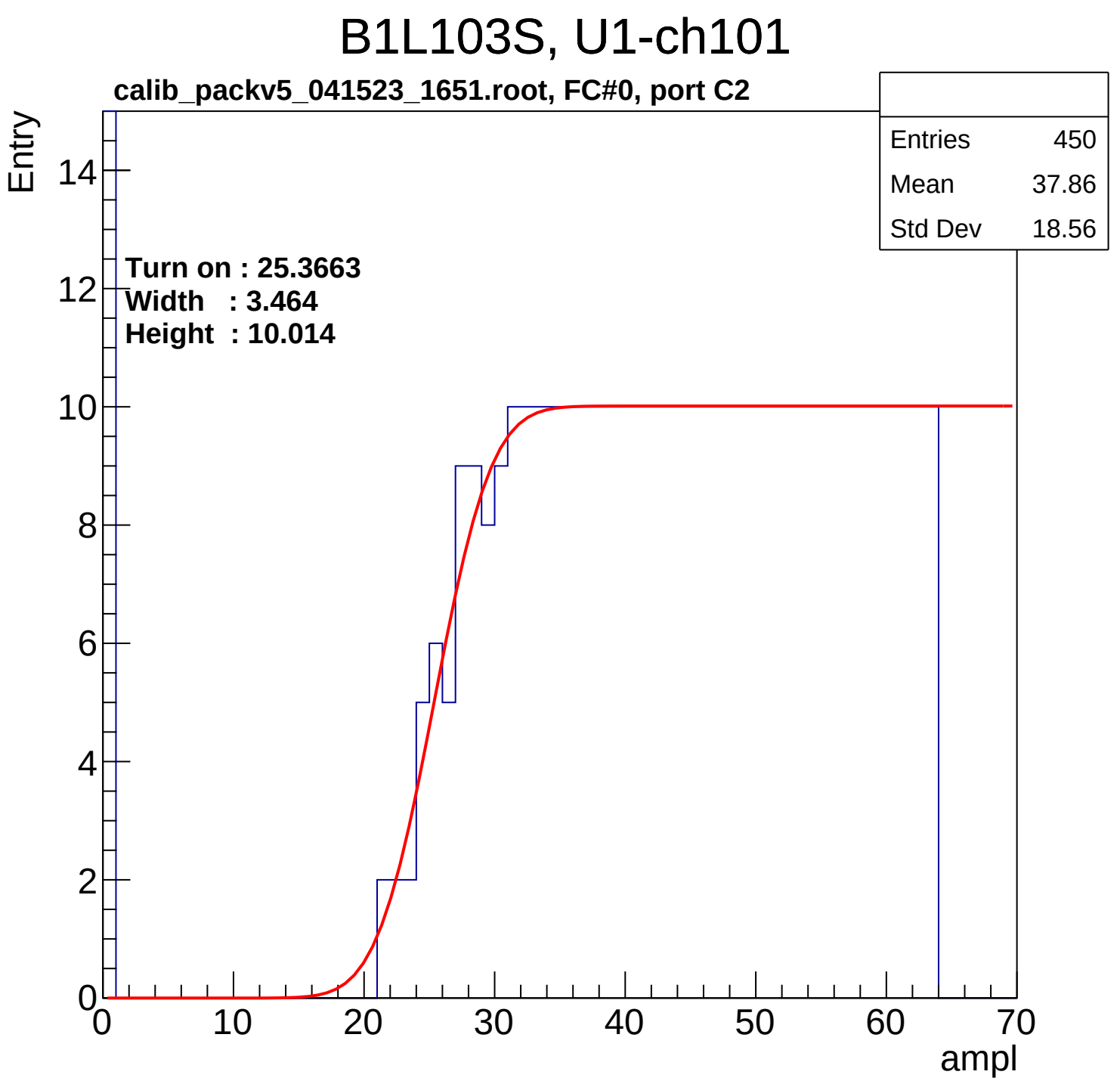
B1L103S, U1-ch101
calib_packv5_041523_1651.root, FC#0, port C2
Entries 450
Mean 37.86
Std Dev 18.56
Turn on : 25.3663
Width : 3.464
Height : 10.014
Entry
ampl
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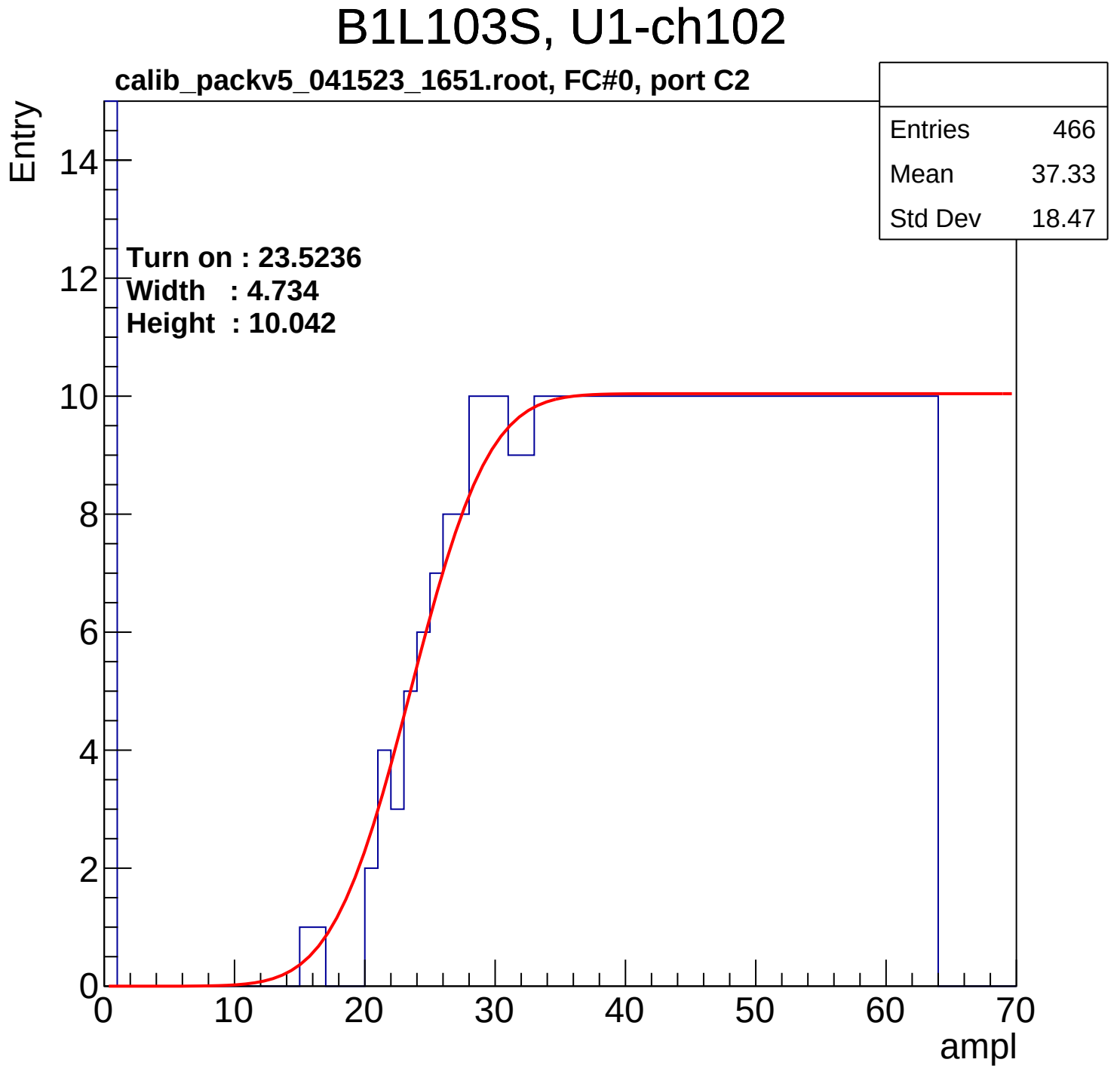
B1L103S, U1-ch102
calib_packv5_041523_1651.root, FC#0, port C2
Entries 466
Mean 37.33
Std Dev 18.47
Turn on : 23.5236
Width : 4.734
Height : 10.042
Entry
ampl
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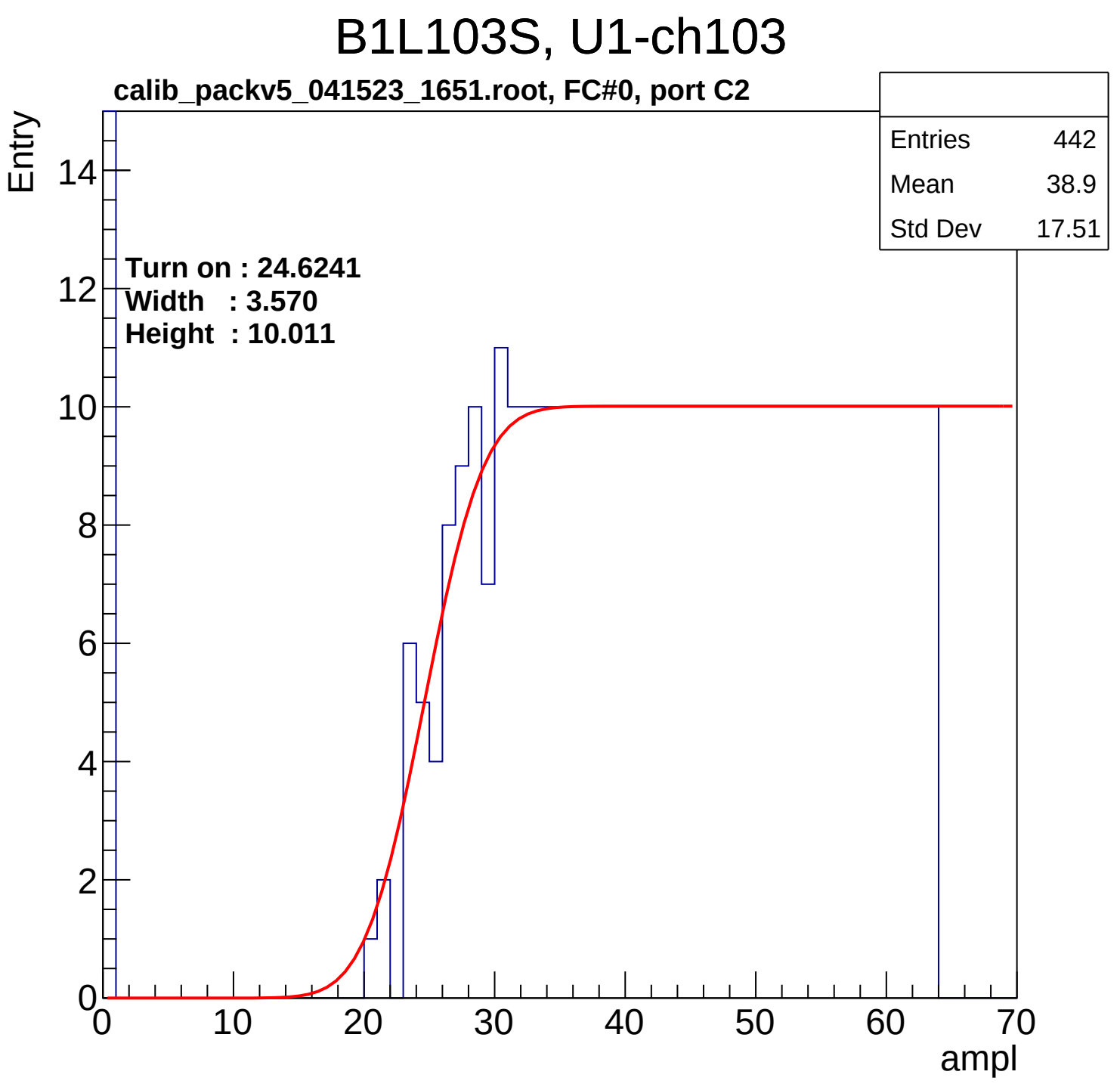
B1L103S, U1-ch103
calib_packv5_041523_1651.root, FC#0, port C2
Entries 442
Mean 38.9
Std Dev 17.51
Turn on : 24.6241
Width : 3.570
Height : 10.011
Entry
ampl
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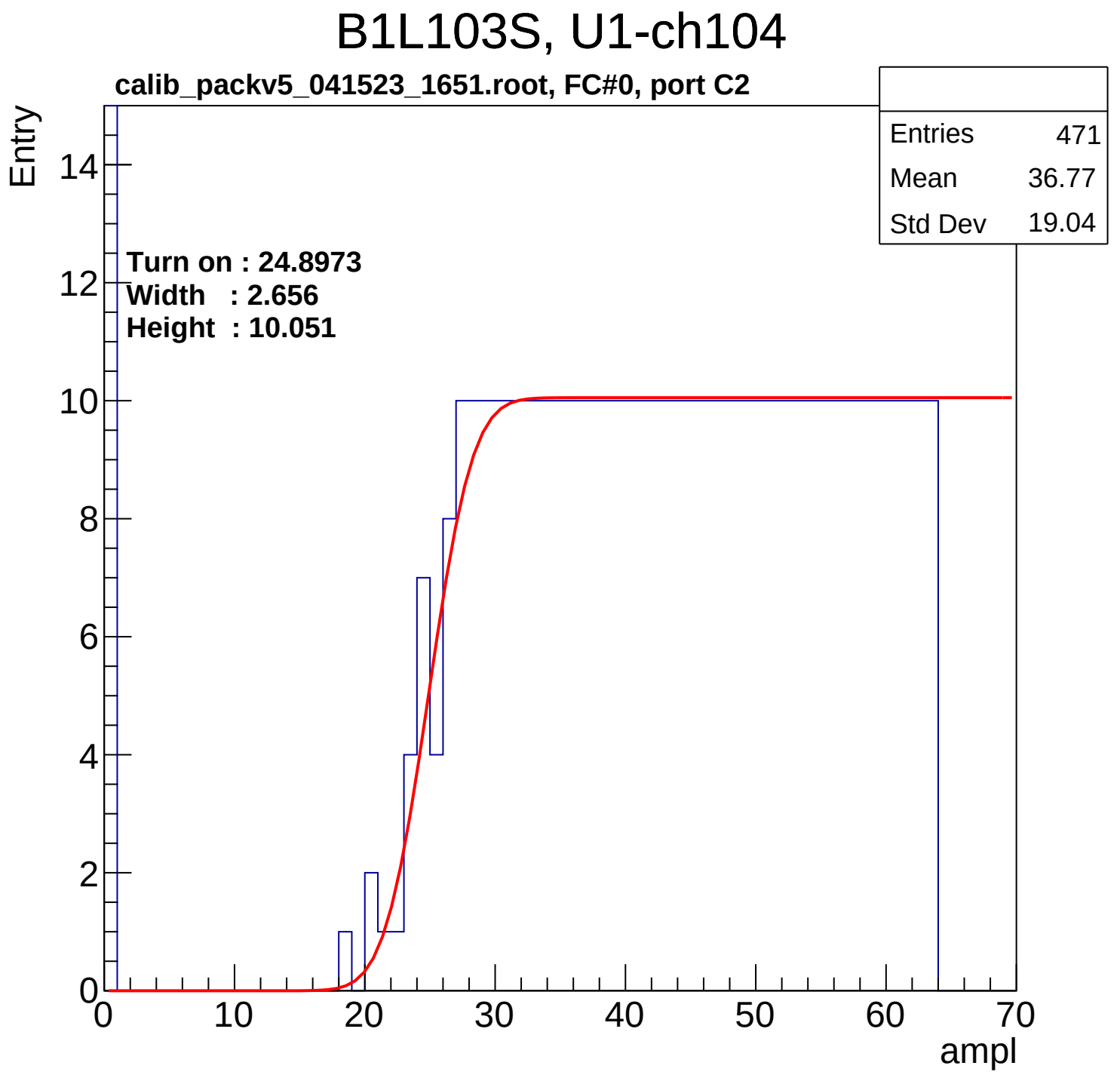
B1L103S, U1-ch104
calib_packv5_041523_1651.root, FC#0, port C2
Entries 471
Mean 36.77
Std Dev 19.04
Turn on : 24.8973
Width : 2.656
Height : 10.051
Entry
ampl
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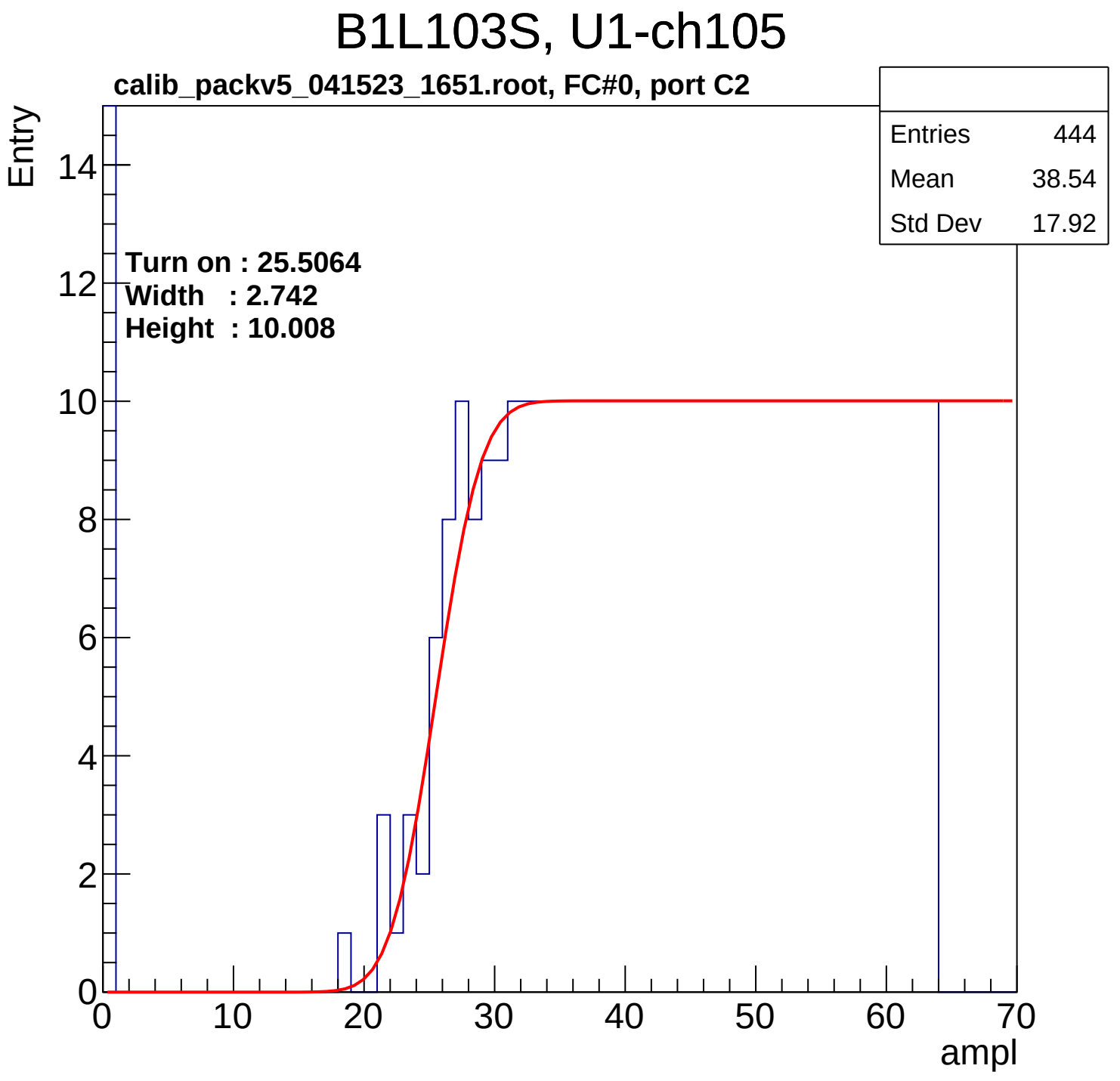
B1L103S, U1-ch105
calib_packv5_041523_1651.root, FC#0, port C2
Entries 444
Mean 38.54
Std Dev 17.92
Turn on : 25.5064
Width : 2.742
Height : 10.008
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ampl
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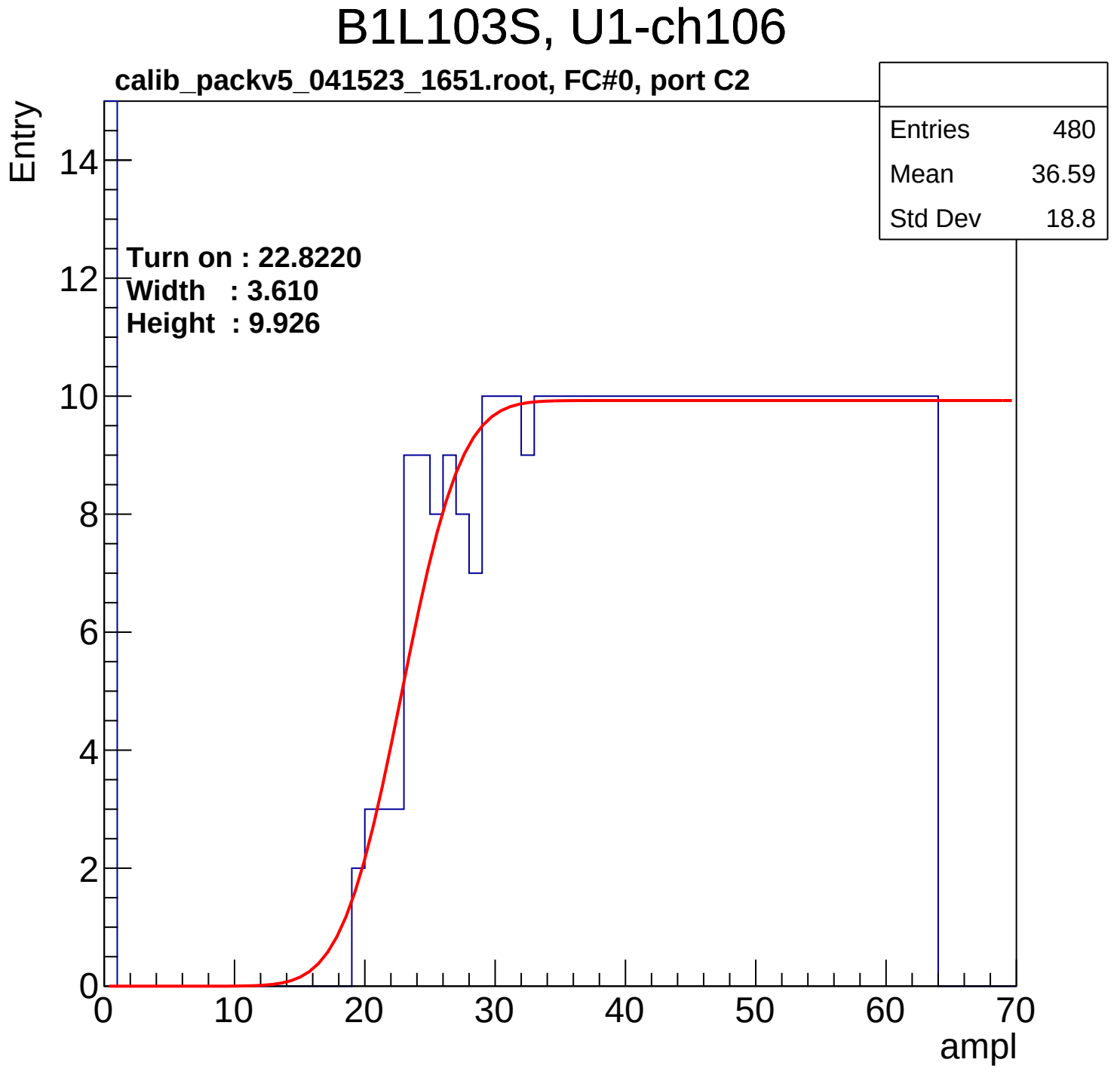
B1L103S, U1-ch106
calib_packv5_041523_1651.root, FC#0, port C2
Entries 480
Mean 36.59
Std Dev 18.8
Turn on : 22.8220
Width : 3.610
Height : 9.926
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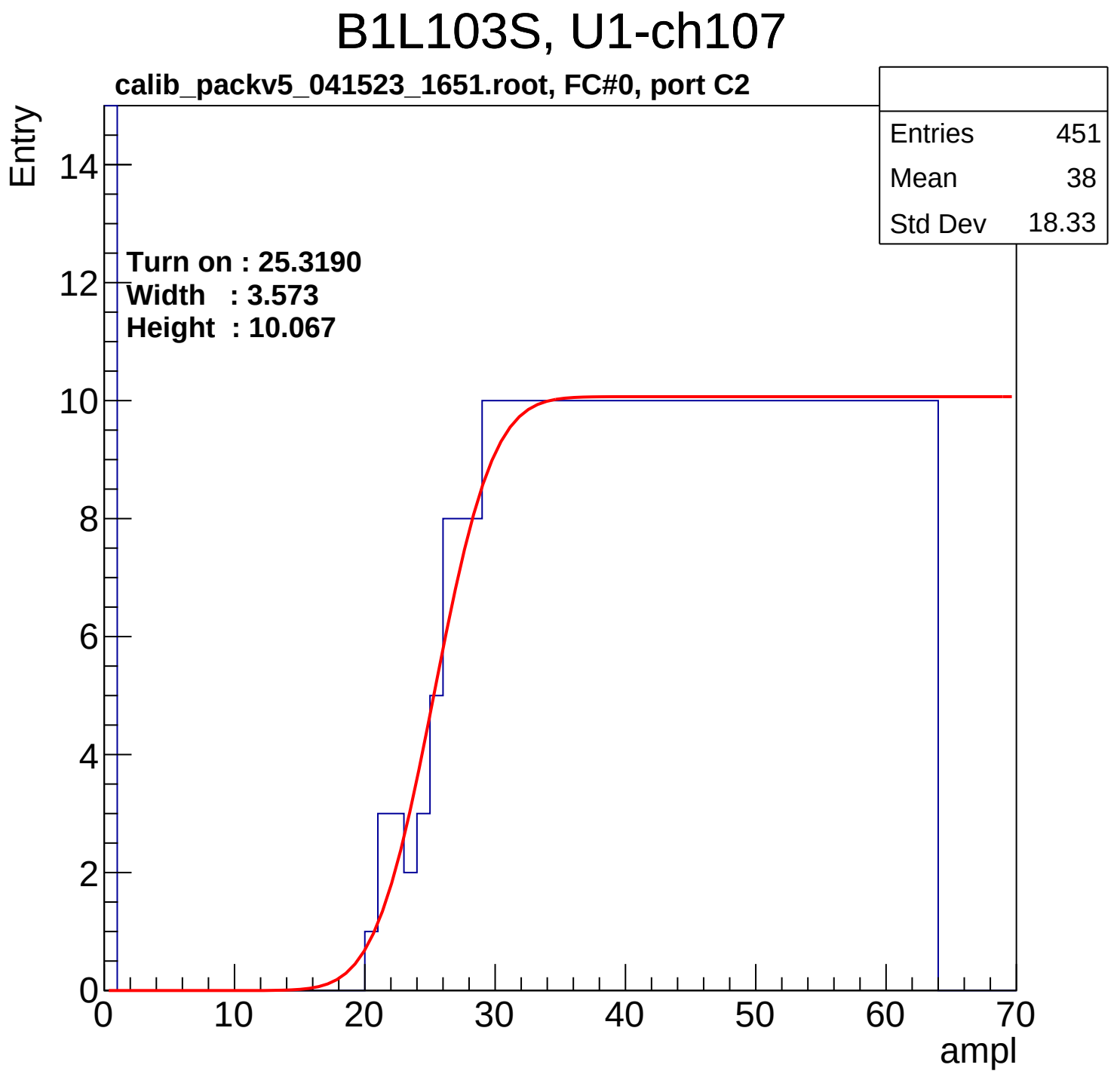
B1L103S, U1-ch107
calib_packv5_041523_1651.root, FC#0, port C2
Entries 451
Mean 38
Std Dev 18.33
Turn on : 25.3190
Width : 3.573
Height : 10.067
Entry
ampl
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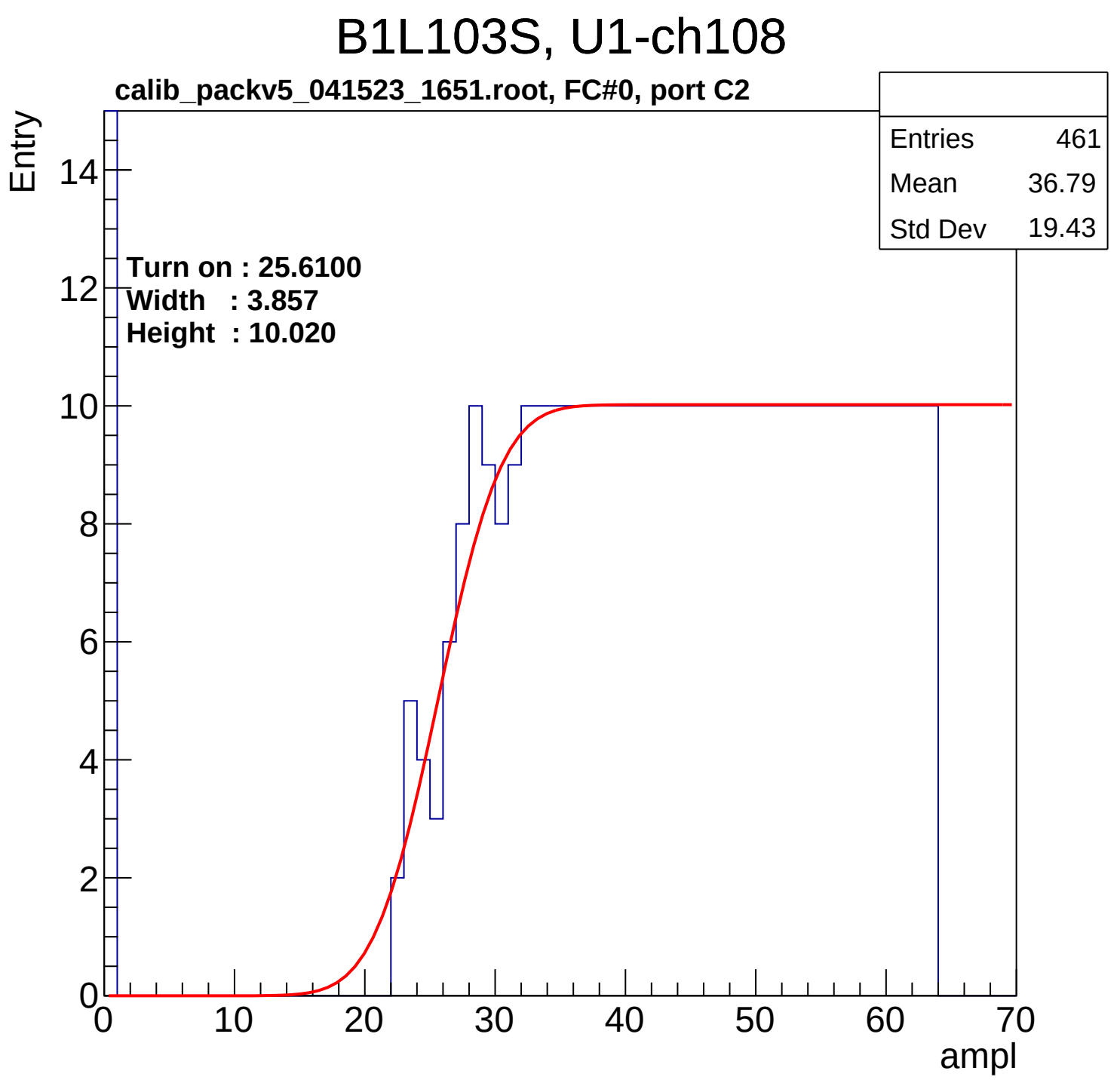
B1L103S, U1-ch108
calib_packv5_041523_1651.root, FC#0, port C2
Entries 461
Mean 36.79
Std Dev 19.43
Turn on : 25.6100
Width : 3.857
Height : 10.020
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ampl
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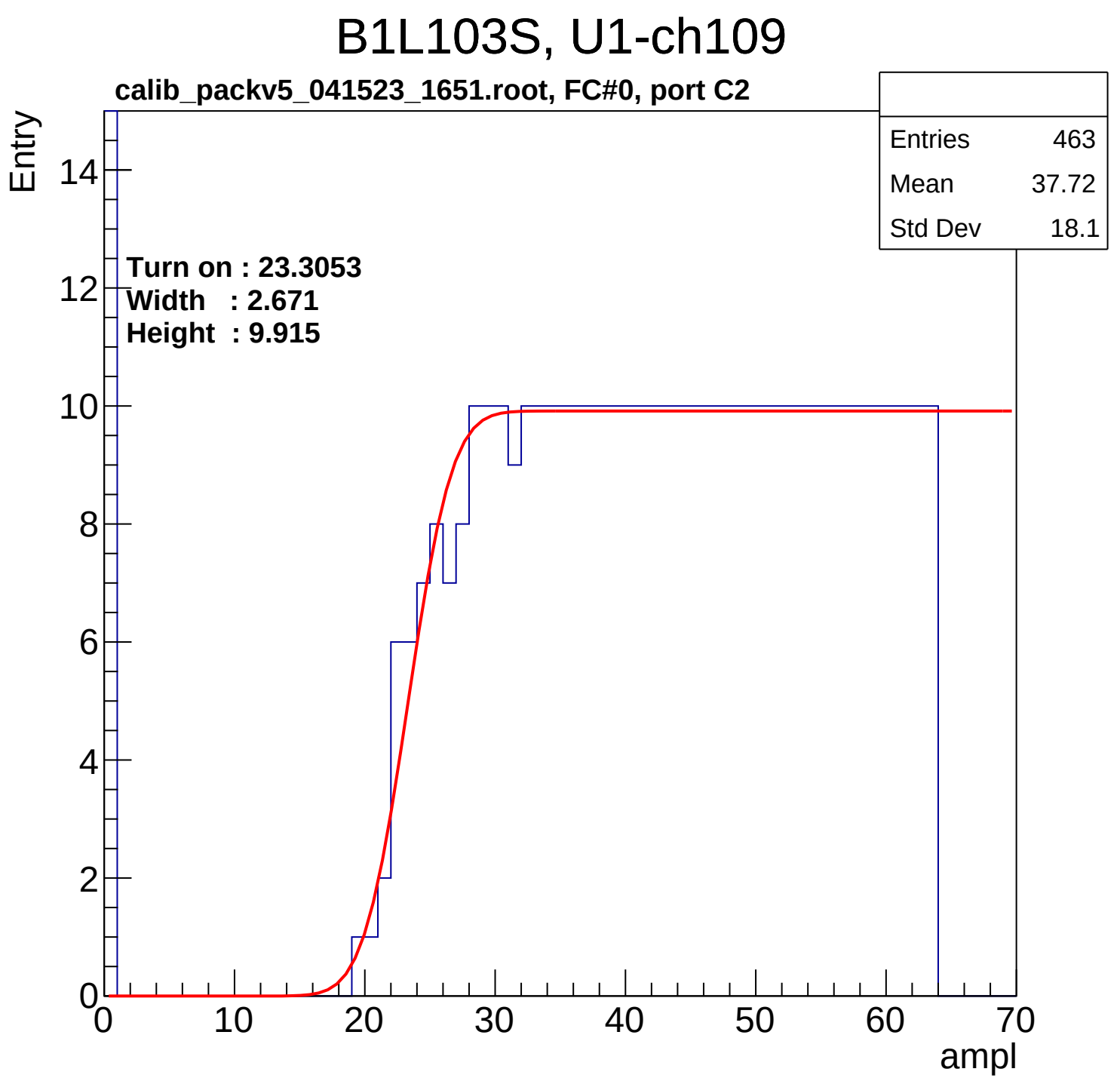
B1L103S, U1-ch109
calib_packv5_041523_1651.root, FC#0, port C2
Entries 463
Mean 37.72
Std Dev 18.1
Turn on : 23.3053
Width : 2.671
Height : 9.915
Entry
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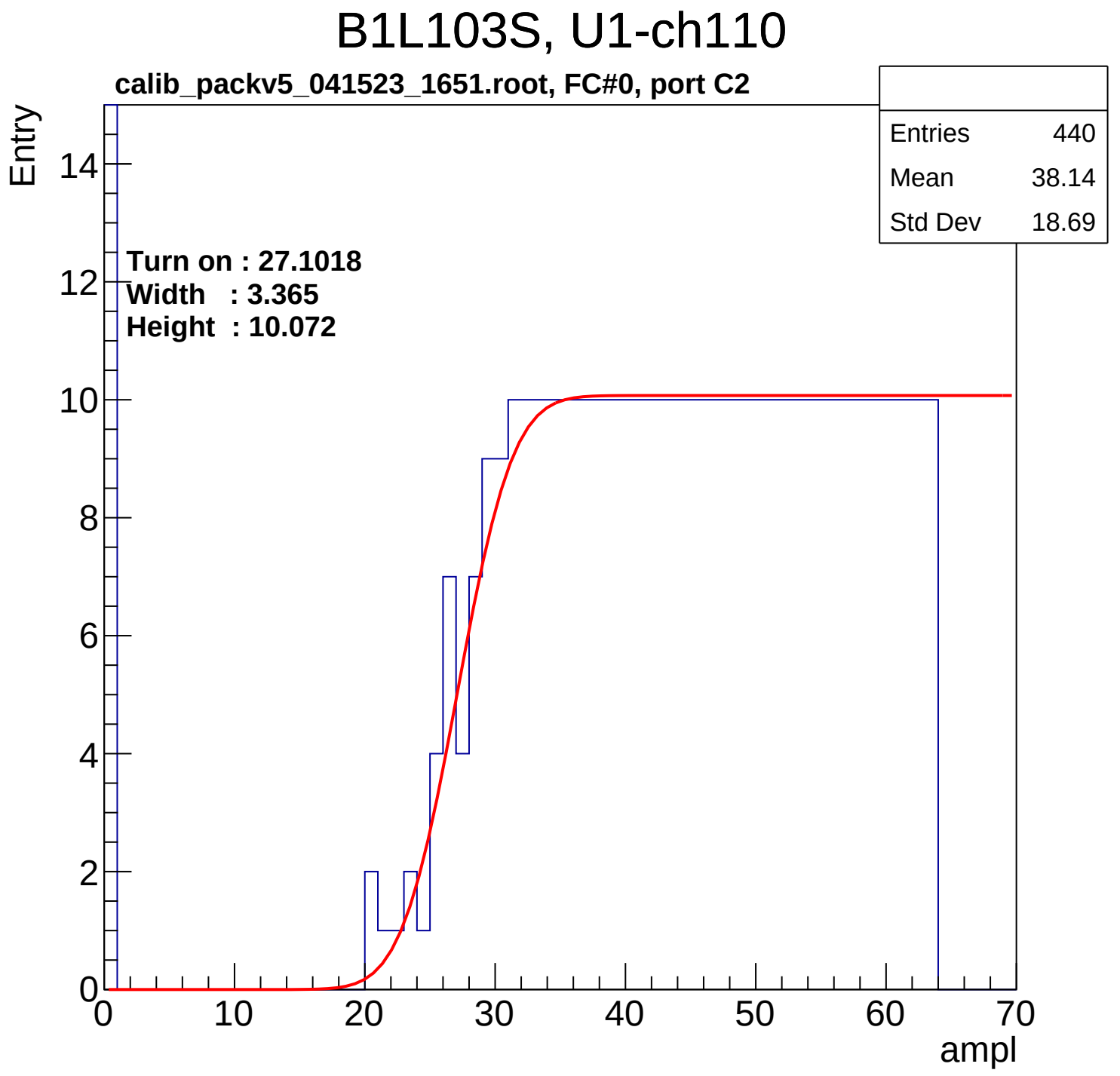
B1L103S, U1-ch110
calib_packv5_041523_1651.root, FC#0, port C2
Entries 440
Mean 38.14
Std Dev 18.69
Turn on : 27.1018
Width : 3.365
Height : 10.072
Entry
ampl
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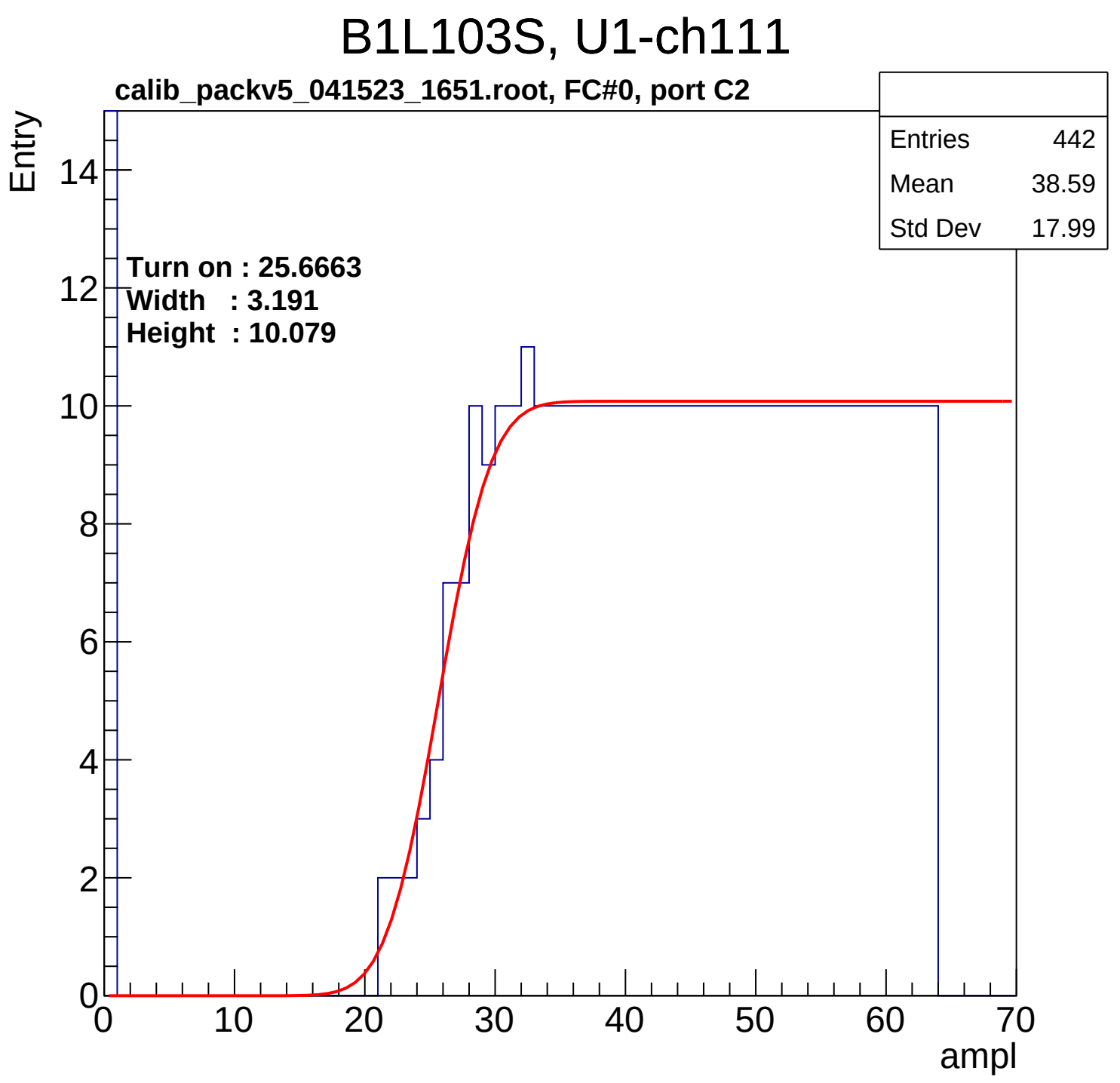
B1L103S, U1-ch111
calib_packv5_041523_1651.root, FC#0, port C2
Entries 442
Mean 38.59
Std Dev 17.99
Turn on : 25.6663
Width : 3.191
Height : 10.079
Entry
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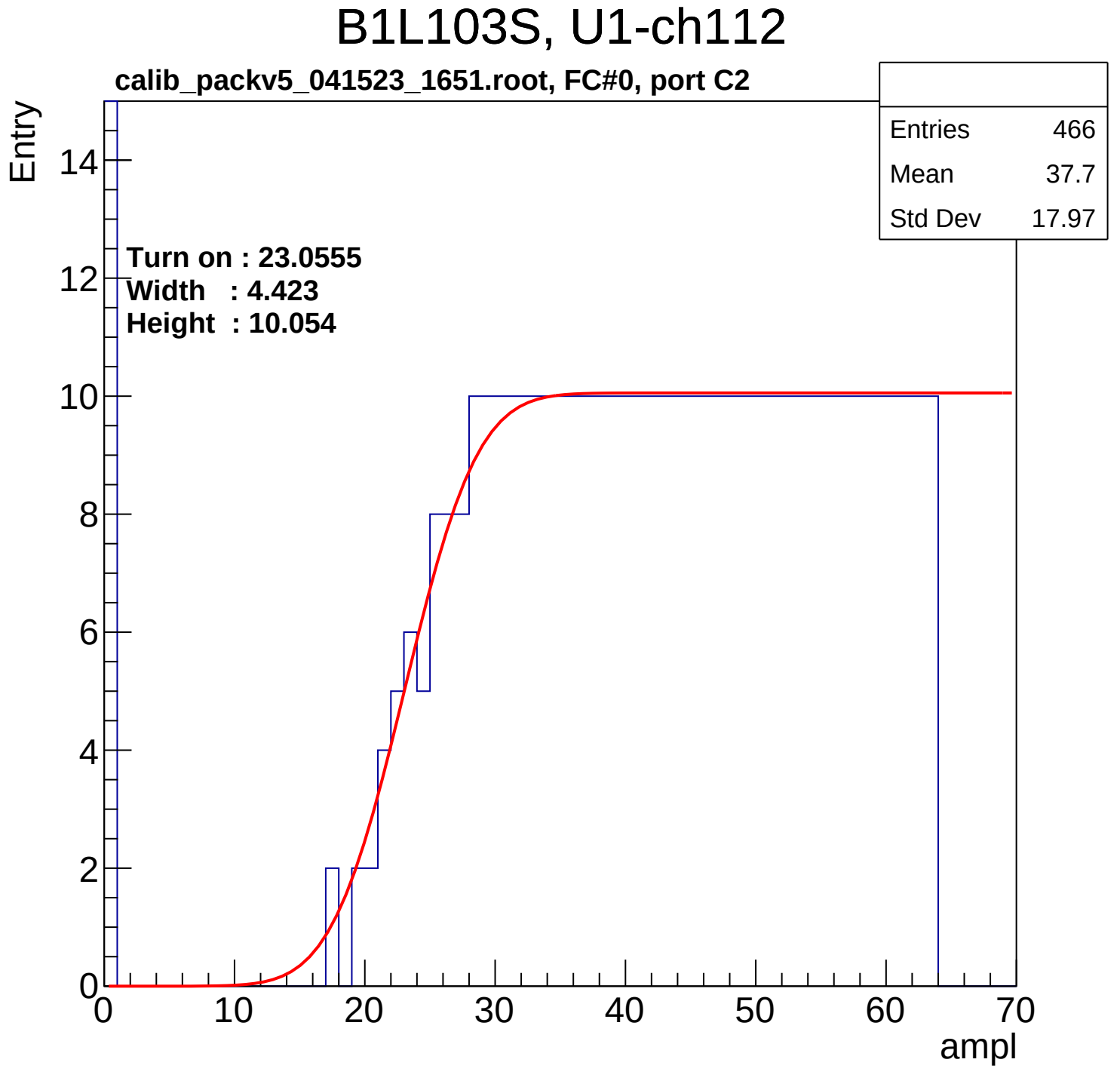
B1L103S, U1-ch112
calib_packv5_041523_1651.root, FC#0, port C2
Entries 466
Mean 37.7
Std Dev 17.97
Turn on : 23.0555
Width : 4.423
Height : 10.054
Entry
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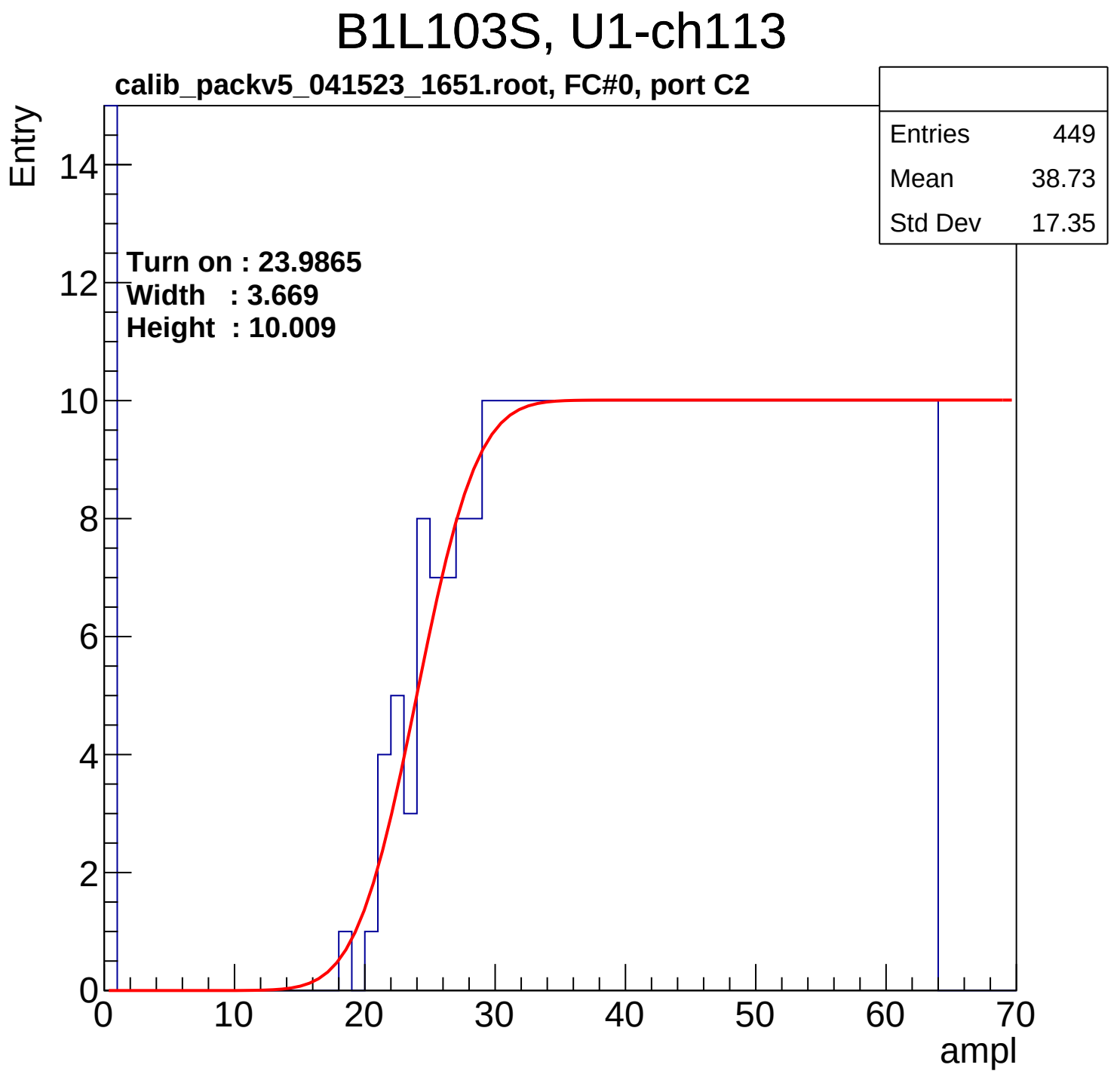
B1L103S, U1-ch113
calib_packv5_041523_1651.root, FC#0, port C2
Entries 449
Mean 38.73
Std Dev 17.35
Turn on : 23.9865
Width : 3.669
Height : 10.009
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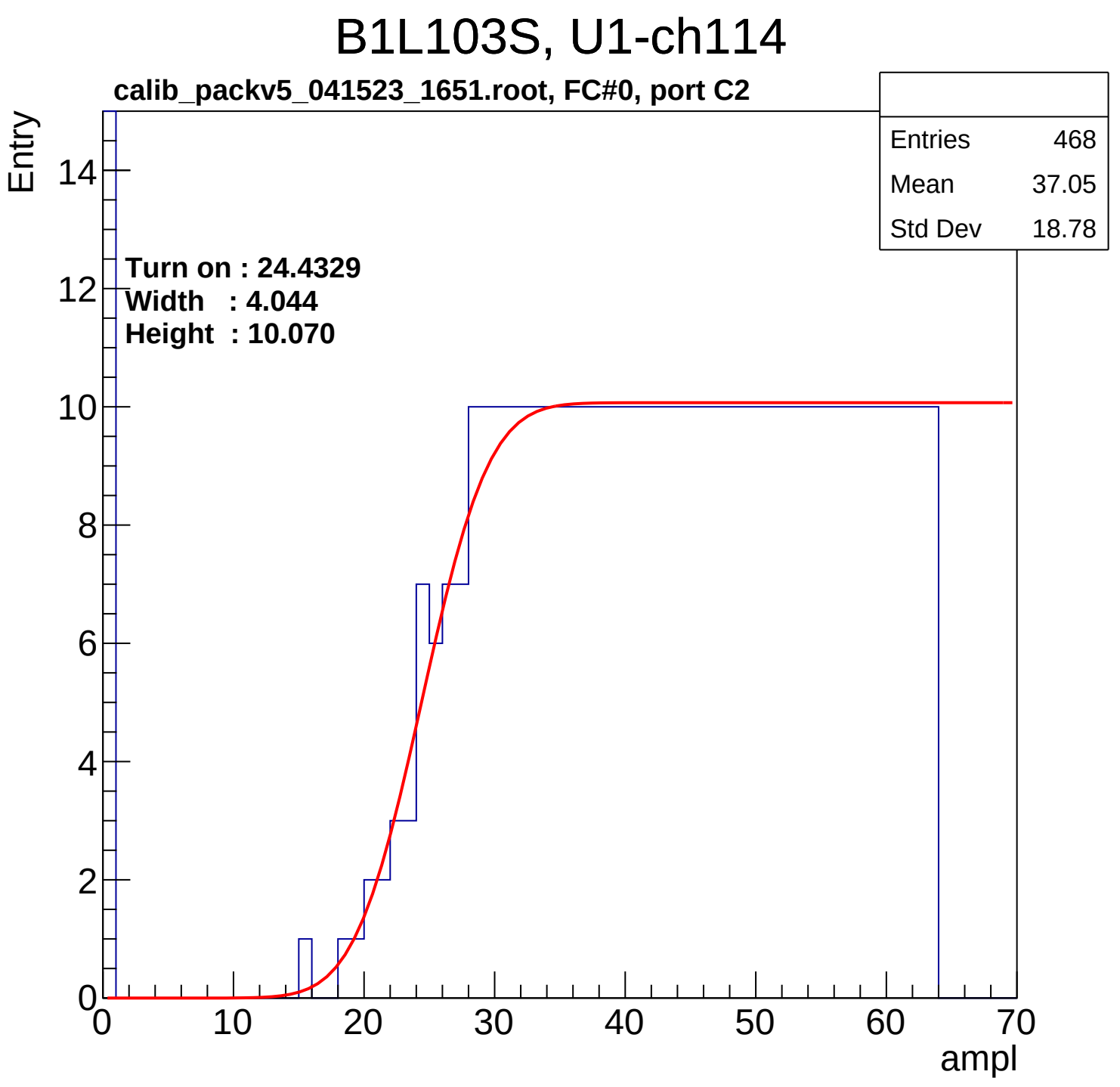
B1L103S, U1-ch114
calib_packv5_041523_1651.root, FC#0, port C2
Entries 468
Mean 37.05
Std Dev 18.78
Turn on : 24.4329
Width : 4.044
Height : 10.070
Entry
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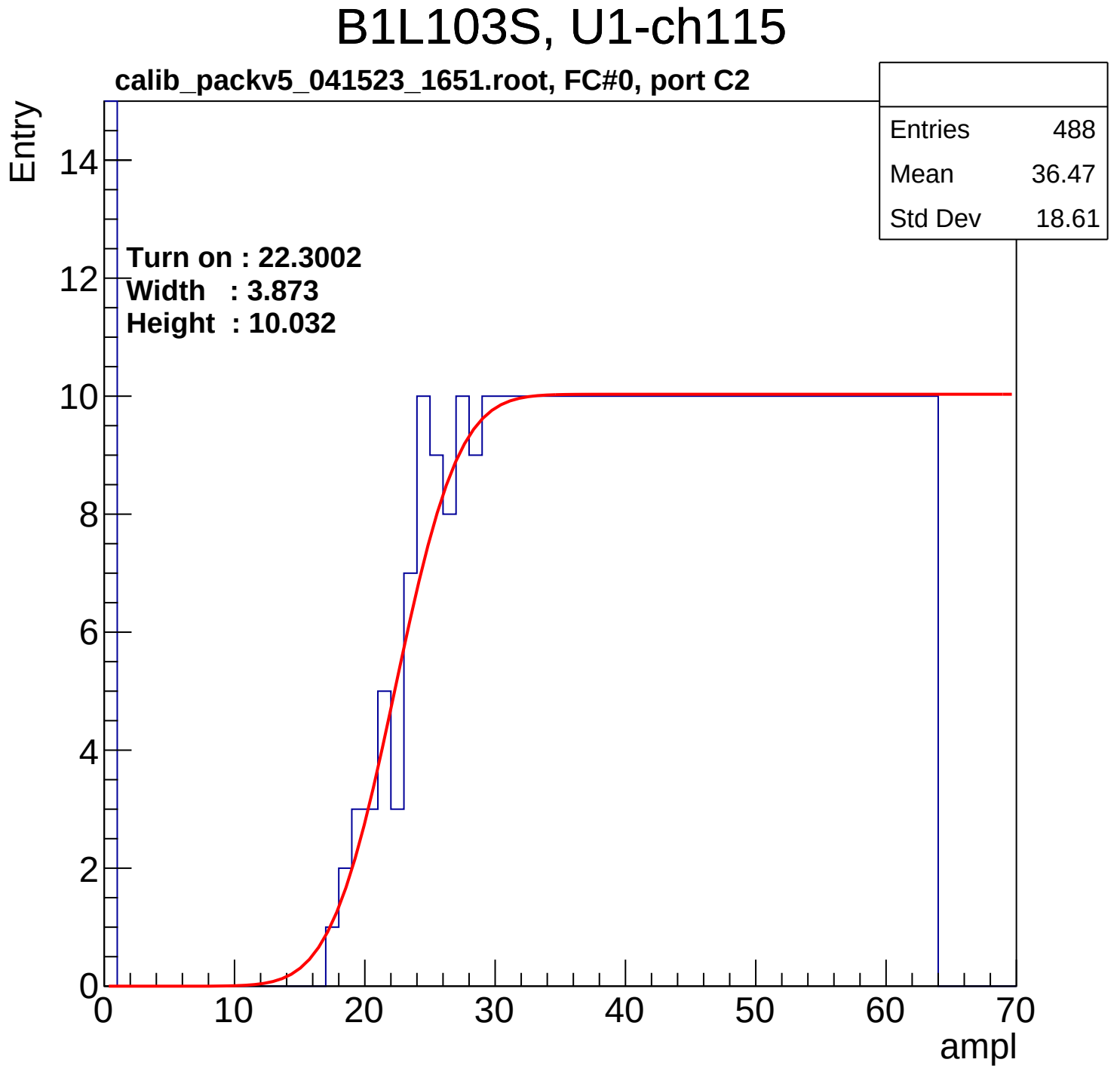
B1L103S, U1-ch115
calib_packv5_041523_1651.root, FC#0, port C2
Entries 488
Mean 36.47
Std Dev 18.61
Turn on : 22.3002
Width : 3.873
Height : 10.032
Entry
ampl
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4
6
8
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10
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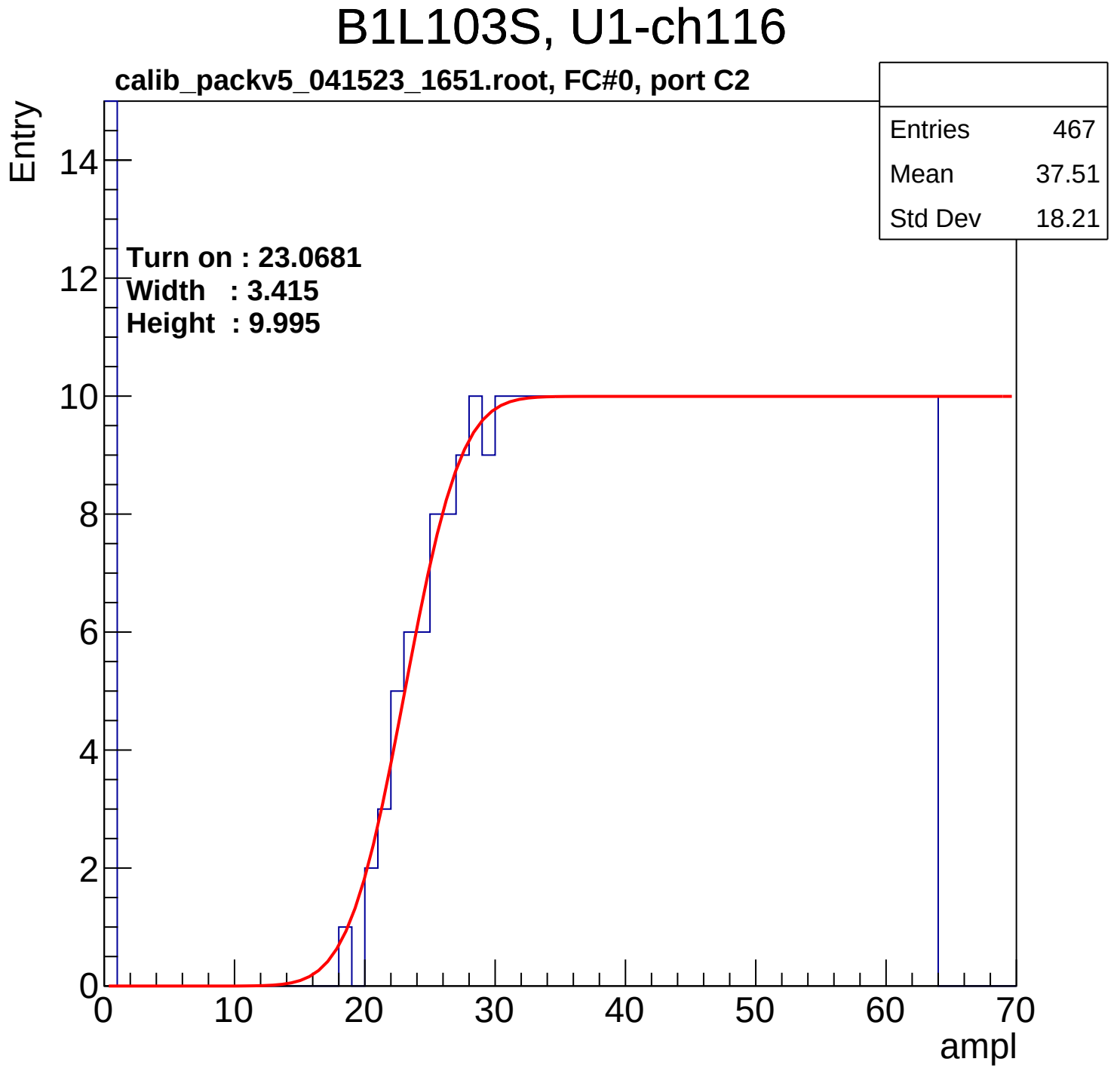
B1L103S, U1-ch116
calib_packv5_041523_1651.root, FC#0, port C2
Entries 467
Mean 37.51
Std Dev 18.21
Turn on : 23.0681
Width : 3.415
Height : 9.995
Entry
ampl
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4
6
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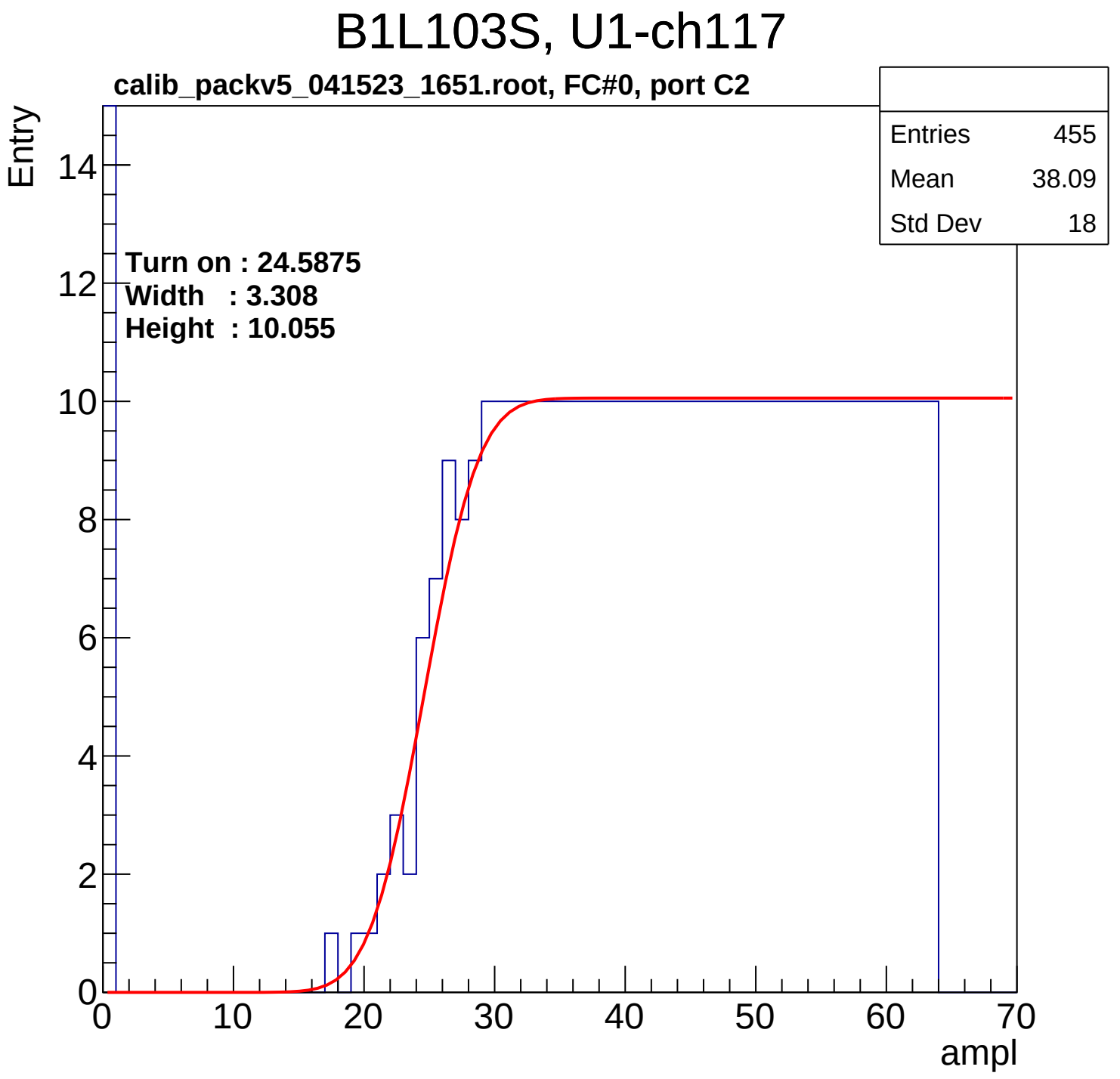
B1L103S, U1-ch117
calib_packv5_041523_1651.root, FC#0, port C2
Entries 455
Mean 38.09
Std Dev 18
Turn on : 24.5875
Width : 3.308
Height : 10.055
Entry
ampl
0
2
4
6
8
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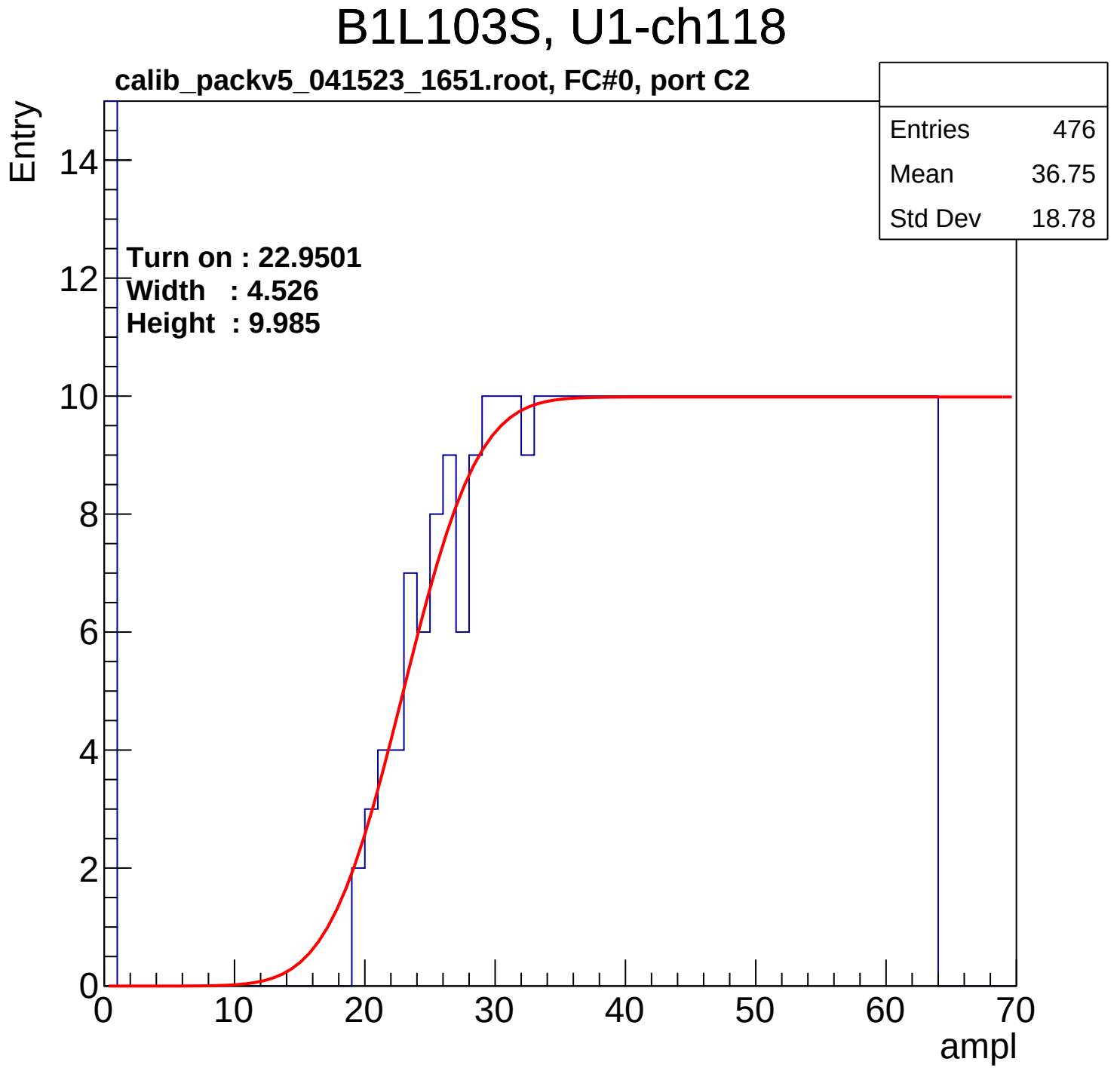
B1L103S, U1-ch118
calib_packv5_041523_1651.root, FC#0, port C2
Entries 476
Mean 36.75
Std Dev 18.78
Turn on : 22.9501
Width : 4.526
Height : 9.985
Entry
ampl
0
2
4
6
8
10
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0
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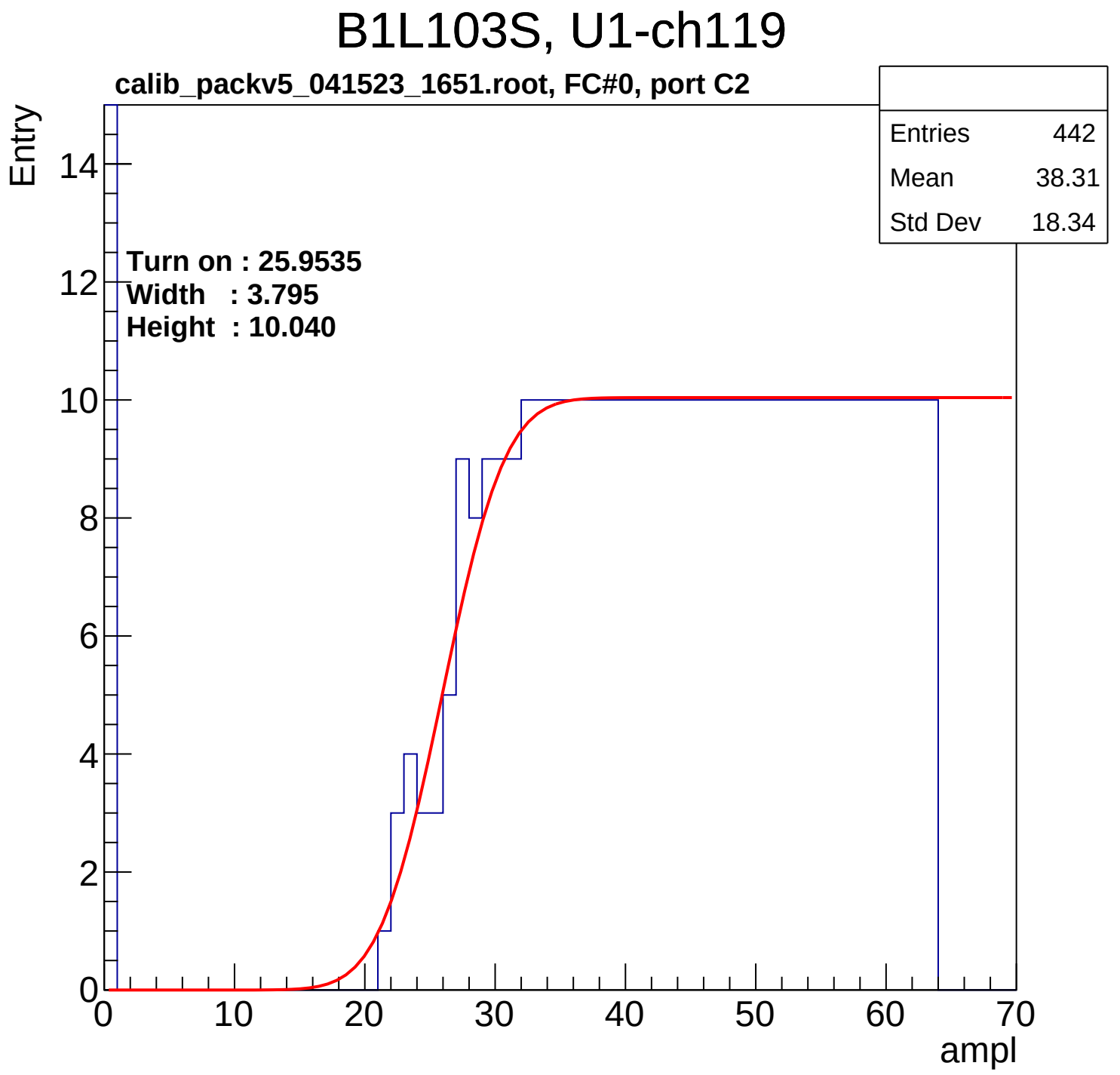
B1L103S, U1-ch119
calib_packv5_041523_1651.root, FC#0, port C2
Entries 442
Mean 38.31
Std Dev 18.34
Turn on : 25.9535
Width : 3.795
Height : 10.040
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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40
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60
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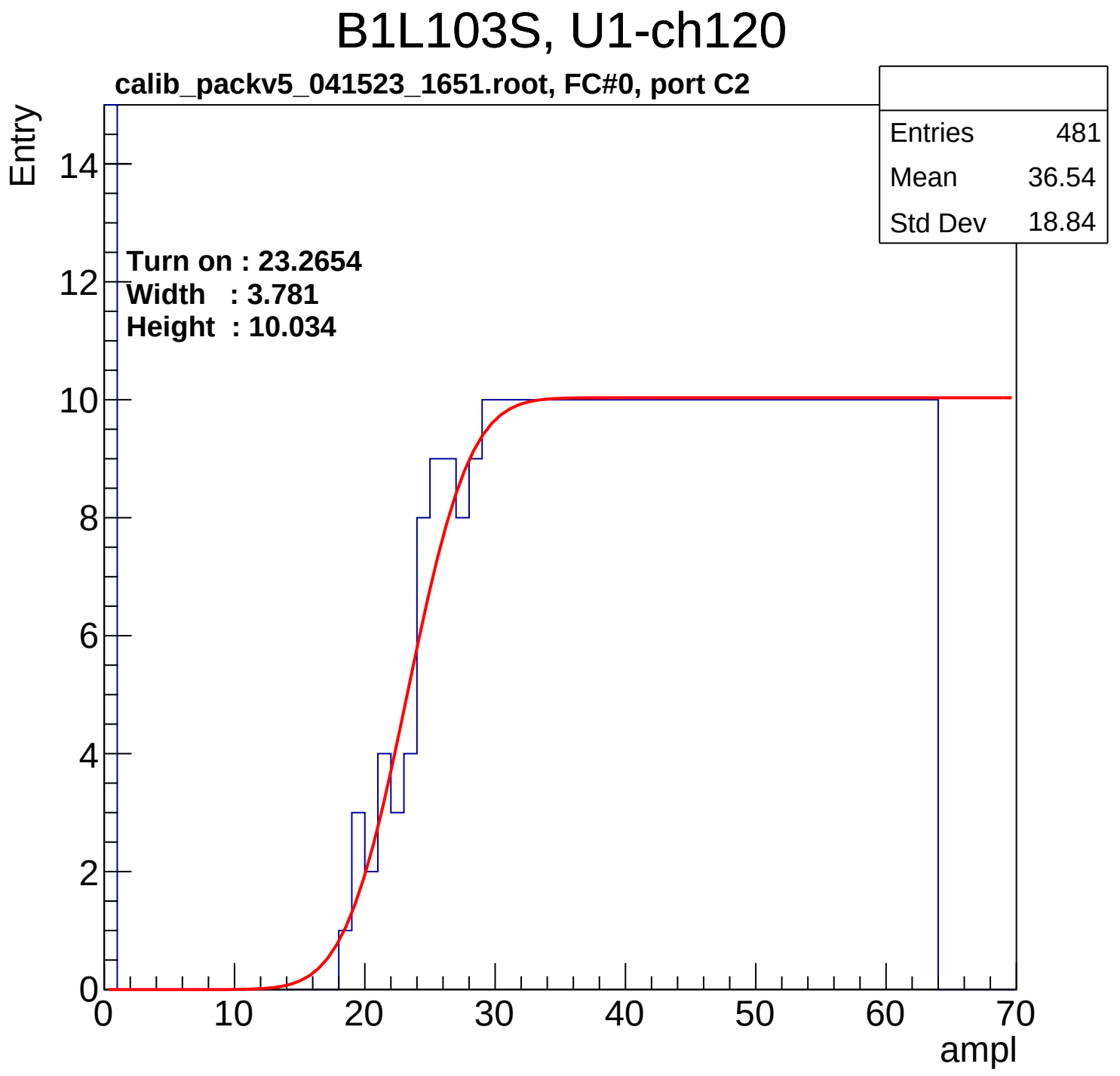
B1L103S, U1-ch120
calib_packv5_041523_1651.root, FC#0, port C2
Entries 481
Mean 36.54
Std Dev 18.84
Turn on : 23.2654
Width : 3.781
Height : 10.034
Entry
ampl
0
2
4
6
8
10
12
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0
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40
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60
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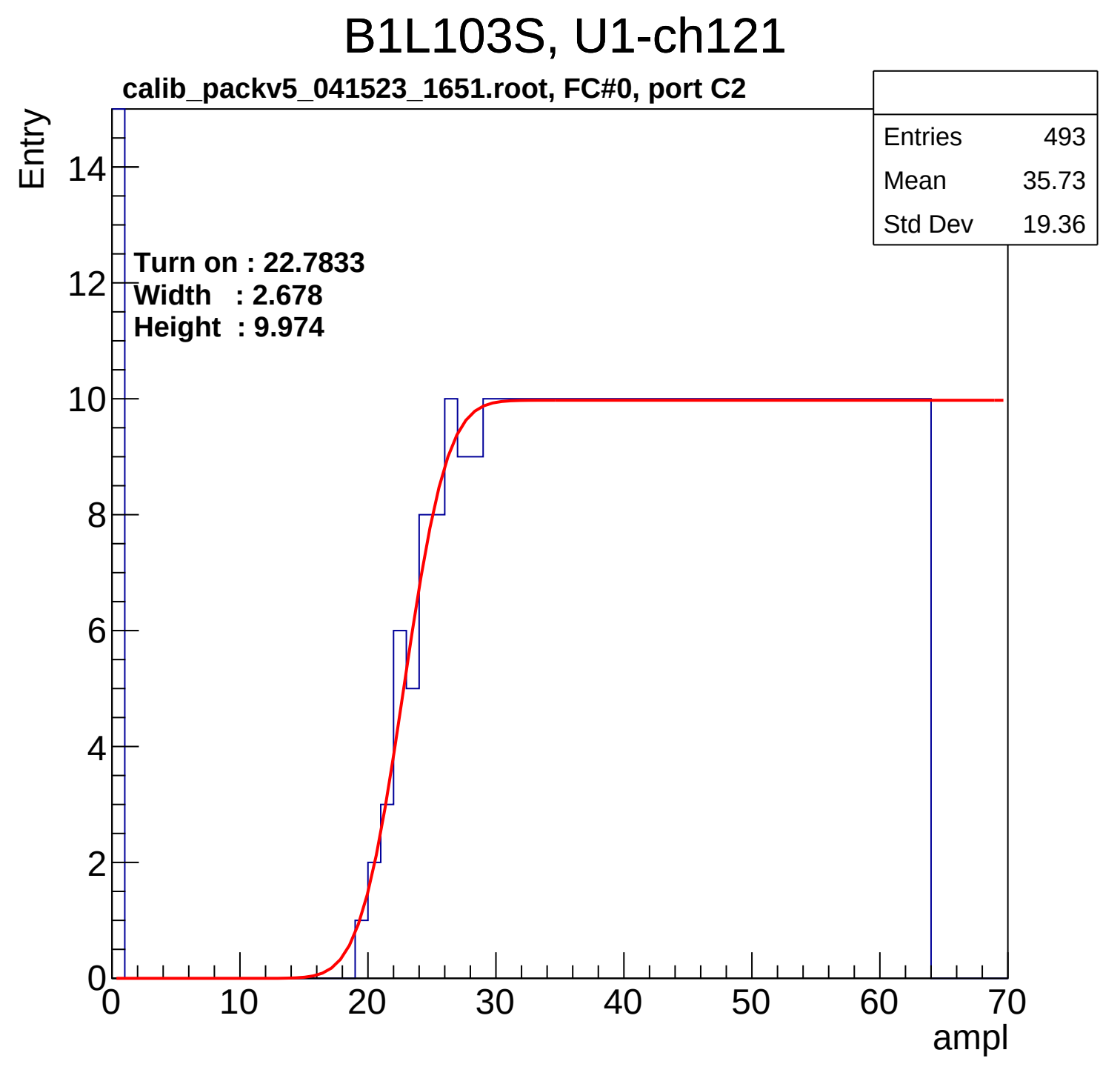
B1L103S, U1-ch121
calib_packv5_041523_1651.root, FC#0, port C2
Entries 493
Mean 35.73
Std Dev 19.36
Turn on : 22.7833
Width : 2.678
Height : 9.974
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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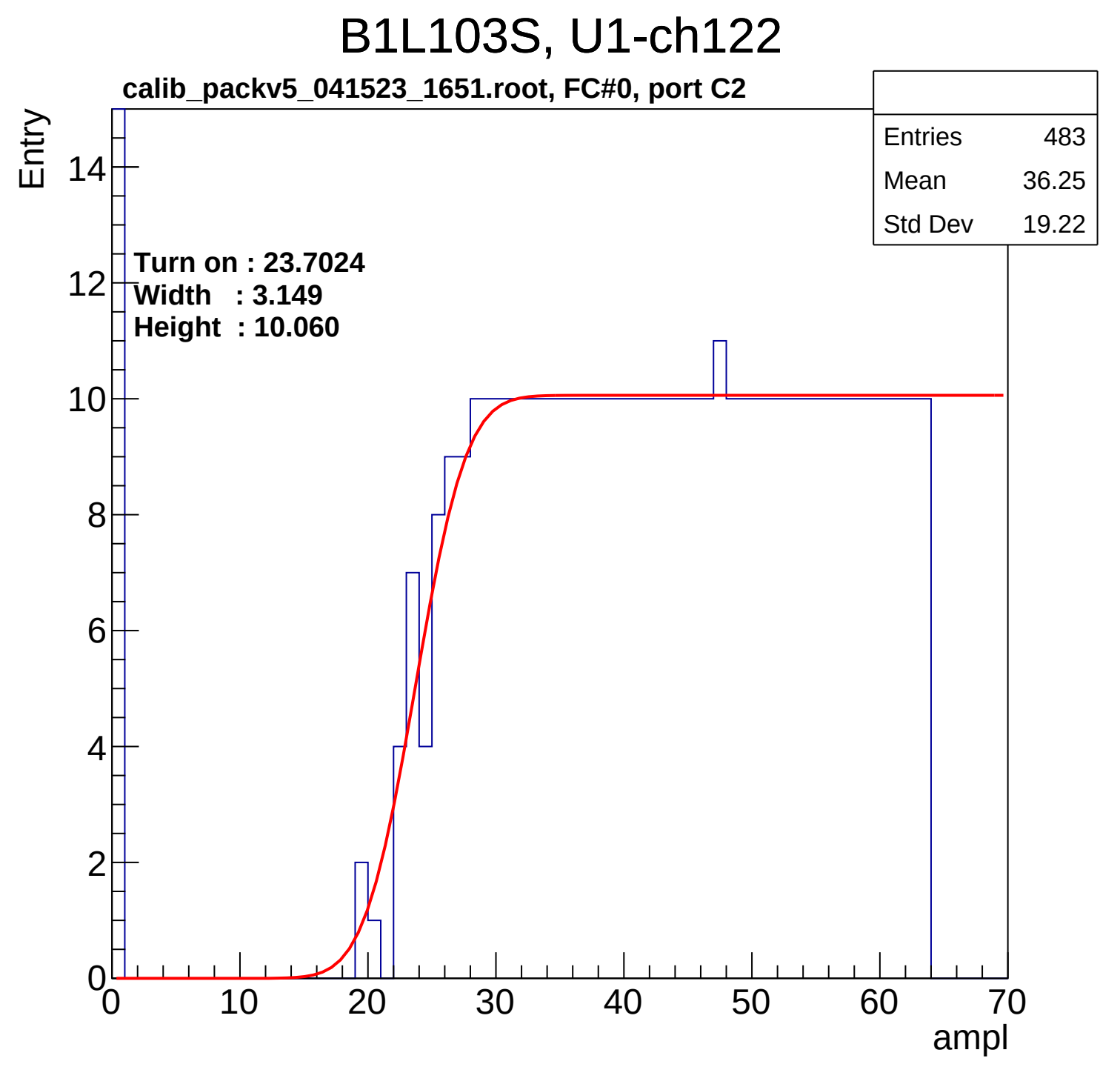
B1L103S, U1-ch122
calib_packv5_041523_1651.root, FC#0, port C2
Entries 483
Mean 36.25
Std Dev 19.22
Turn on : 23.7024
Width : 3.149
Height : 10.060
Entry
ampl
0
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4
6
8
10
12
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0
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20
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40
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60
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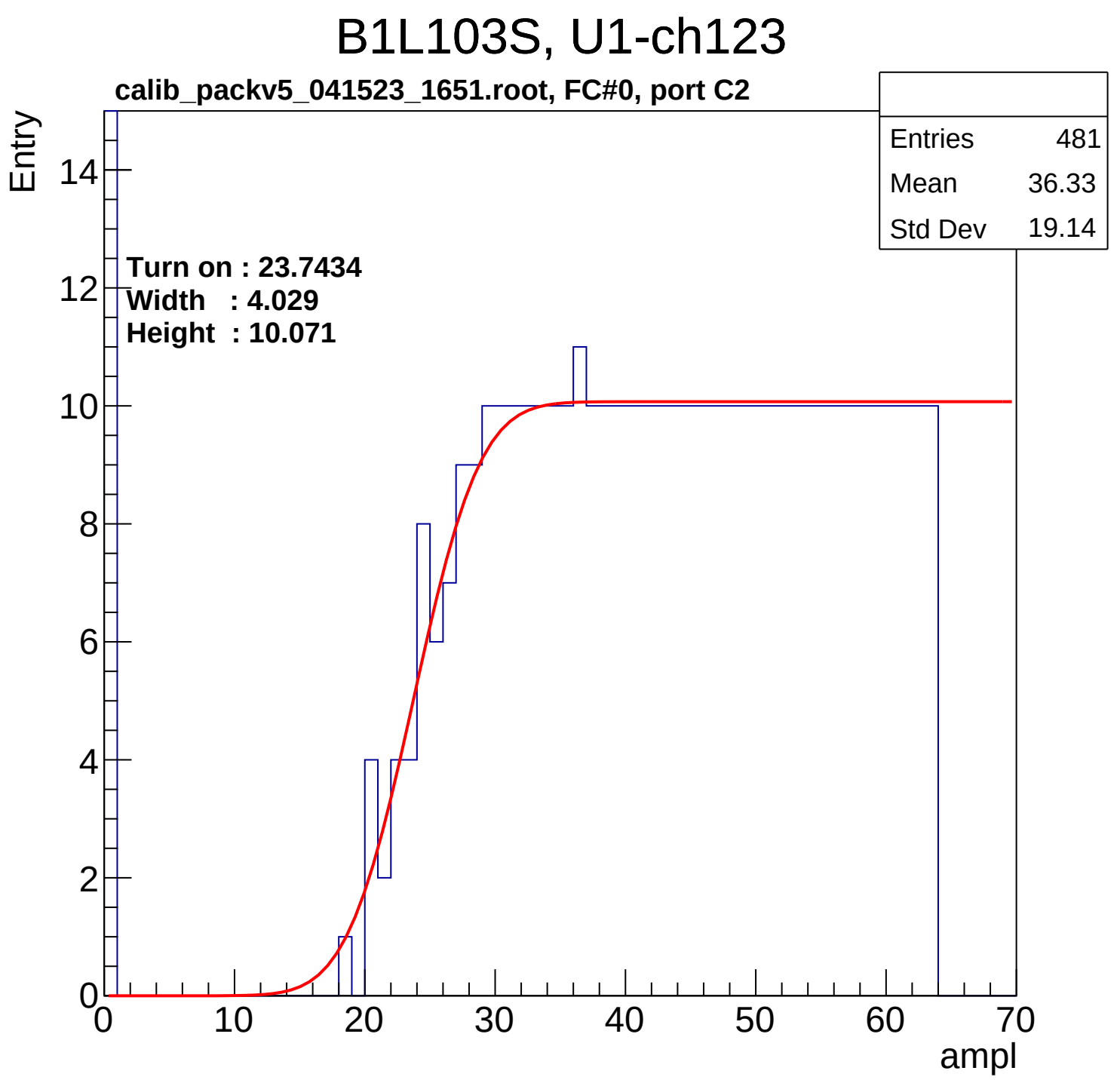
B1L103S, U1-ch123
calib_packv5_041523_1651.root, FC#0, port C2
Entries 481
Mean 36.33
Std Dev 19.14
Turn on : 23.7434
Width : 4.029
Height : 10.071
Entry
ampl
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2
4
6
8
10
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40
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60
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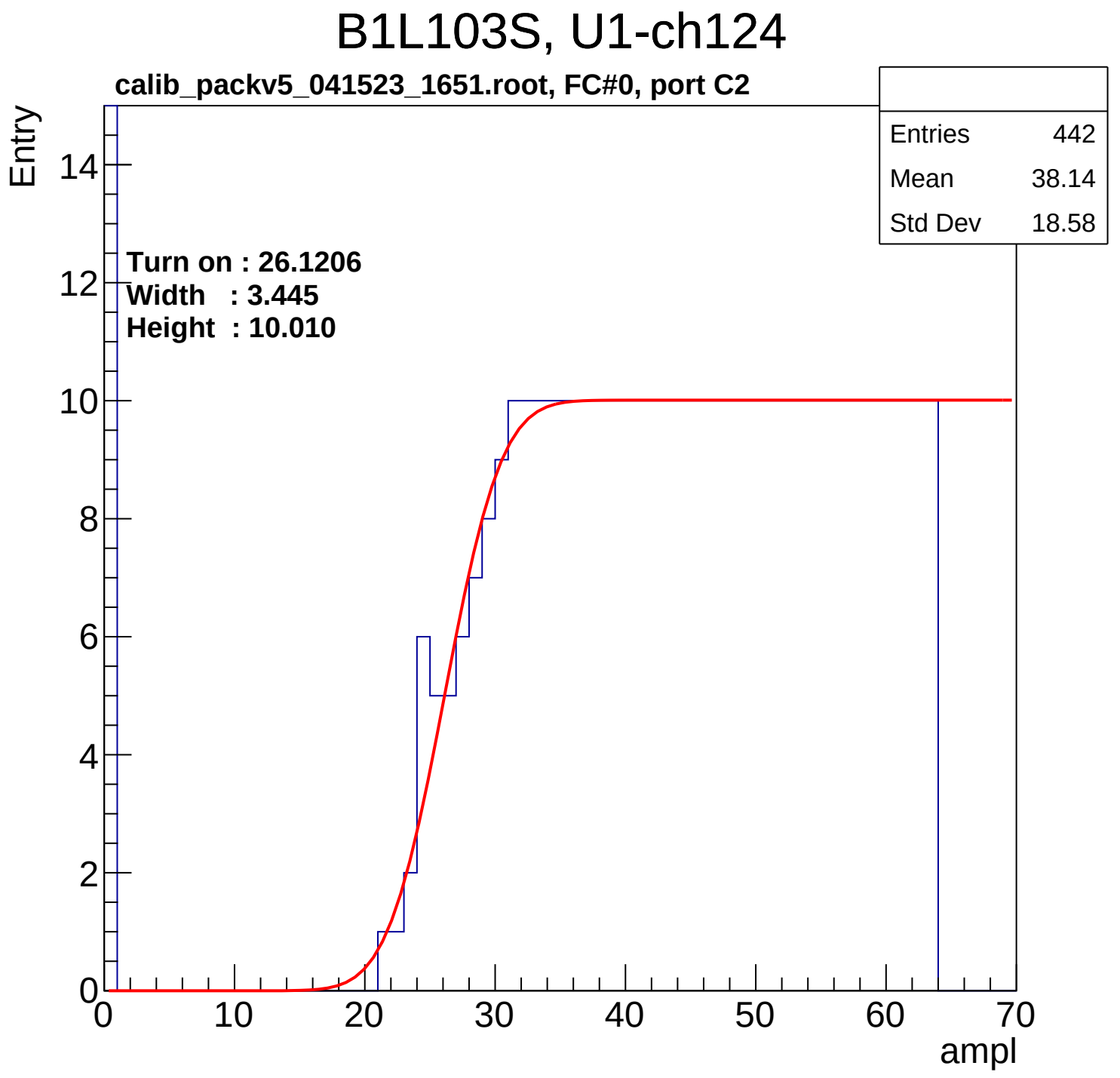
B1L103S, U1-ch124
calib_packv5_041523_1651.root, FC#0, port C2
Entries 442
Mean 38.14
Std Dev 18.58
Turn on : 26.1206
Width : 3.445
Height : 10.010
Entry
ampl
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4
6
8
10
12
14
0
10
20
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40
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60
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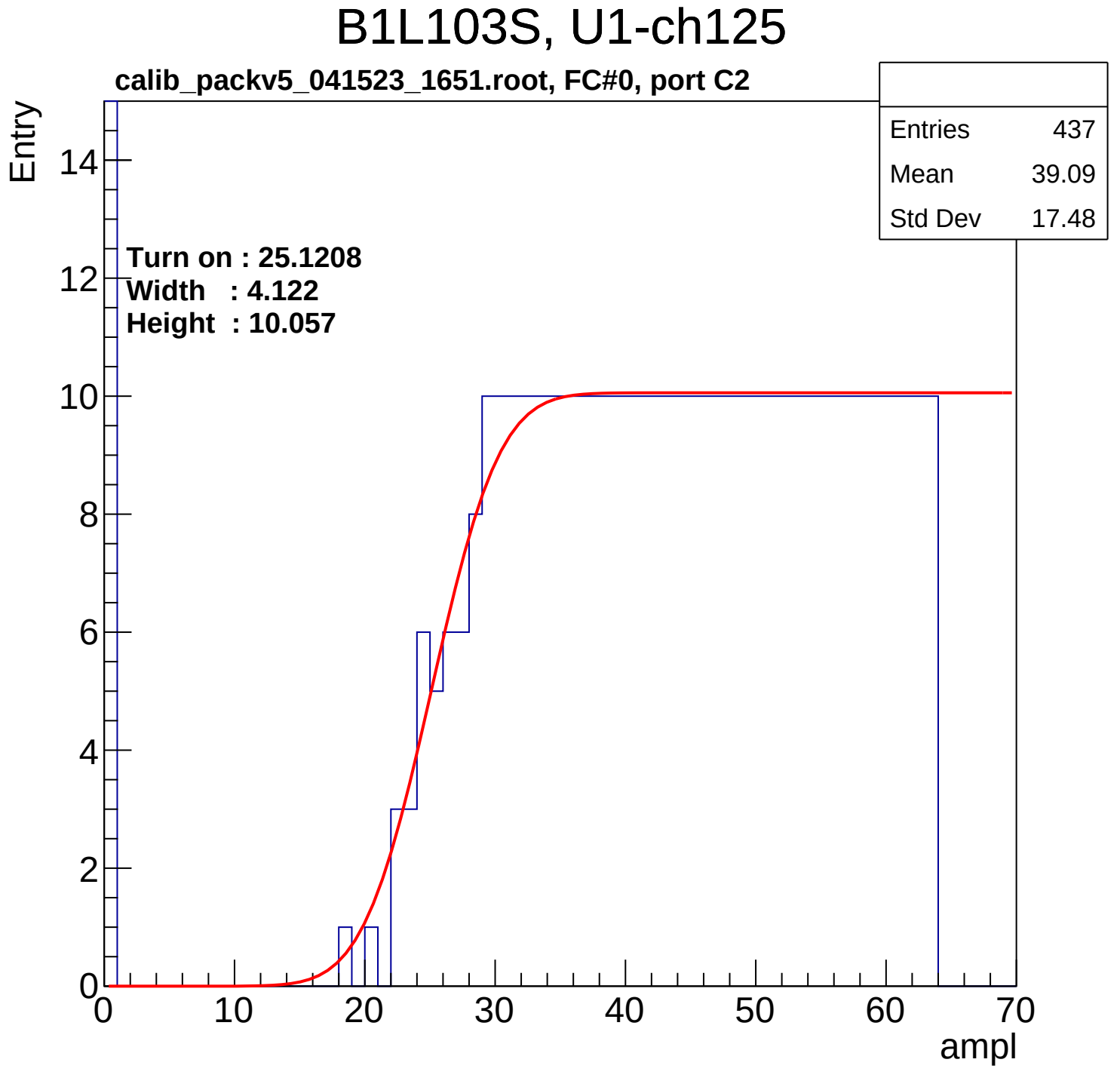
B1L103S, U1-ch125
calib_packv5_041523_1651.root, FC#0, port C2
Entries 437
Mean 39.09
Std Dev 17.48
Turn on : 25.1208
Width : 4.122
Height : 10.057
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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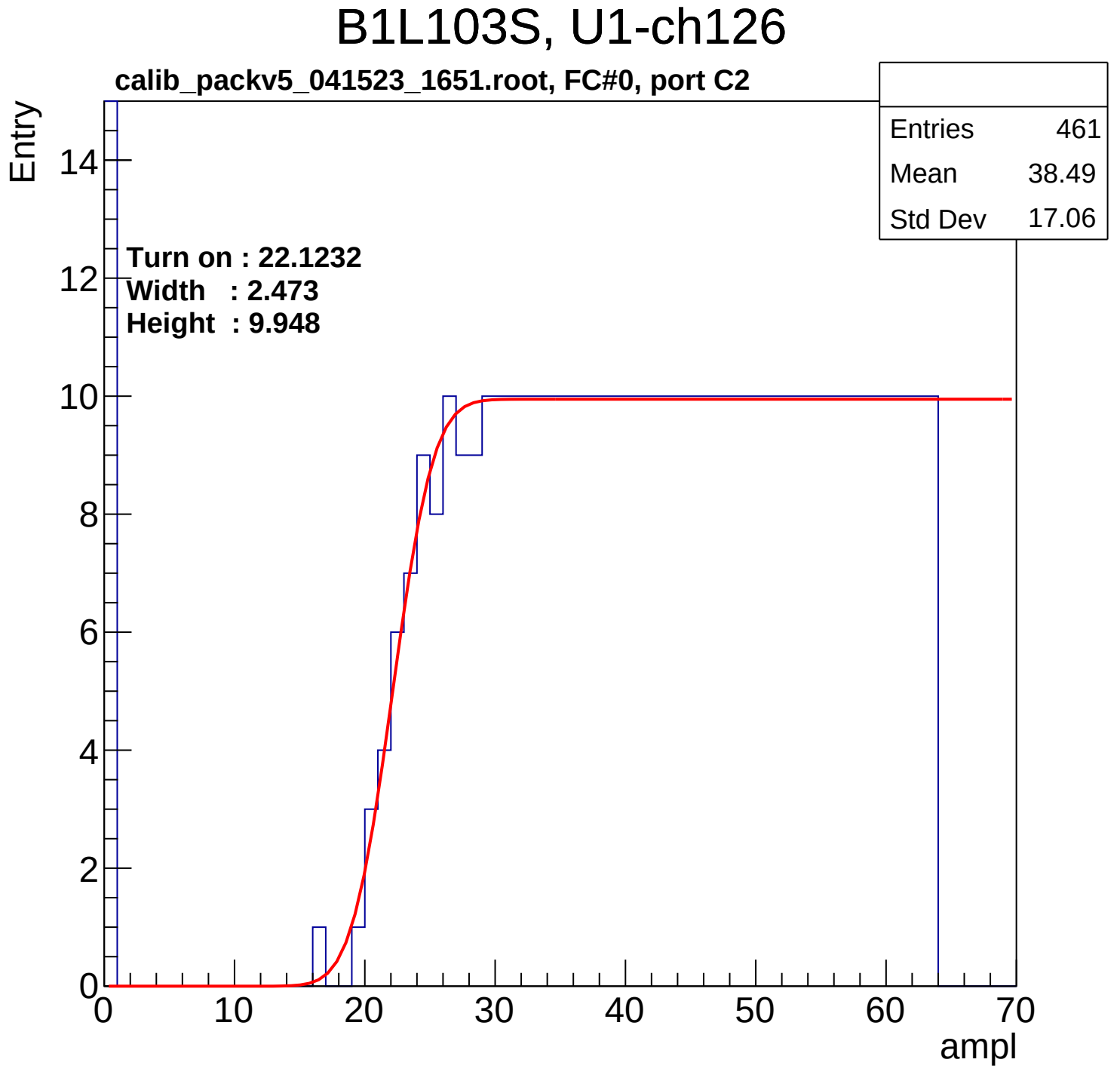
40
50
60
70


B1L103S, U1-ch126
calib_packv5_041523_1651.root, FC#0, port C2
Entries 461
Mean 38.49
Std Dev 17.06
Turn on : 22.1232
Width : 2.473
Height : 9.948
Entry
ampl
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6
8
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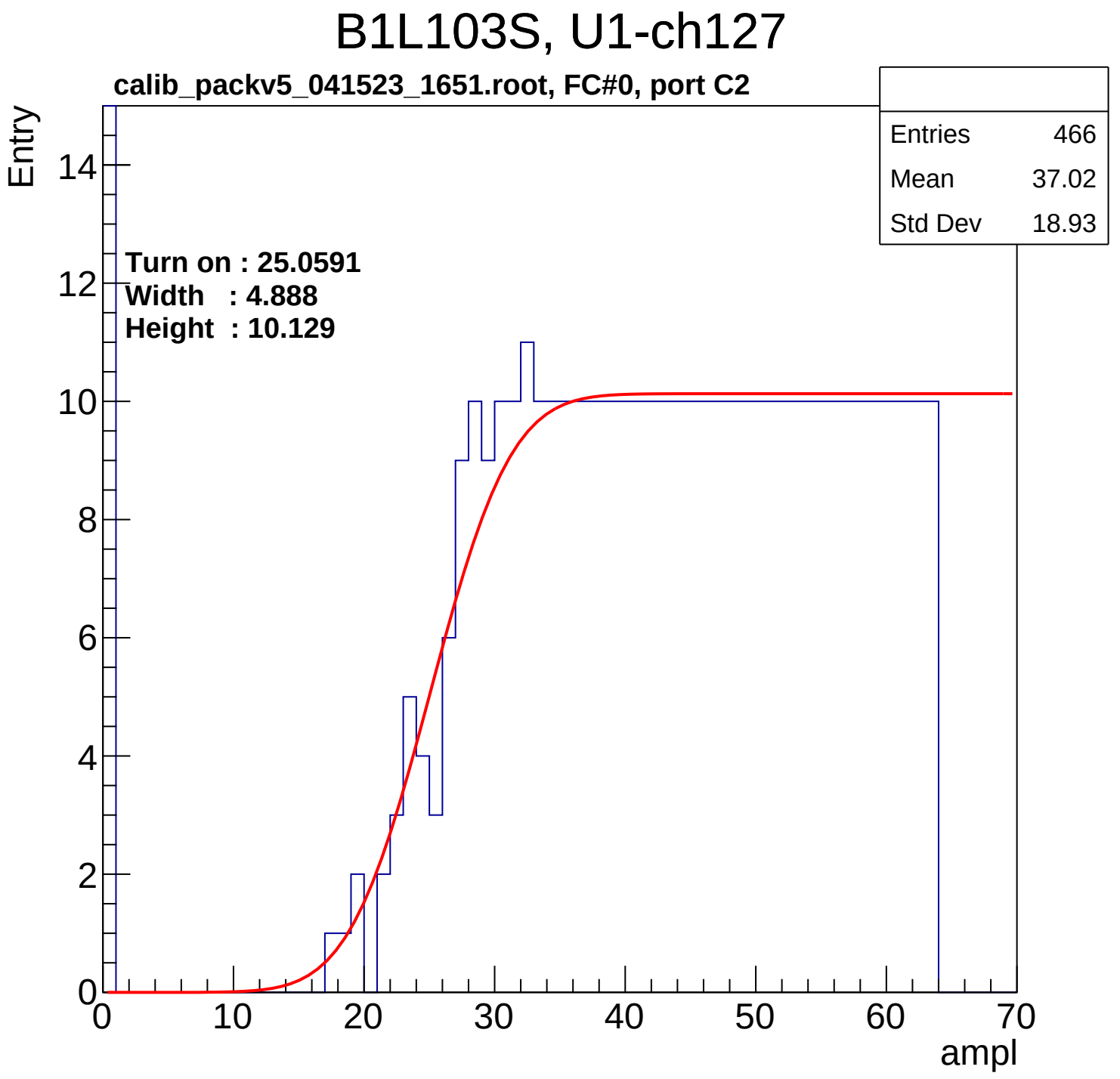
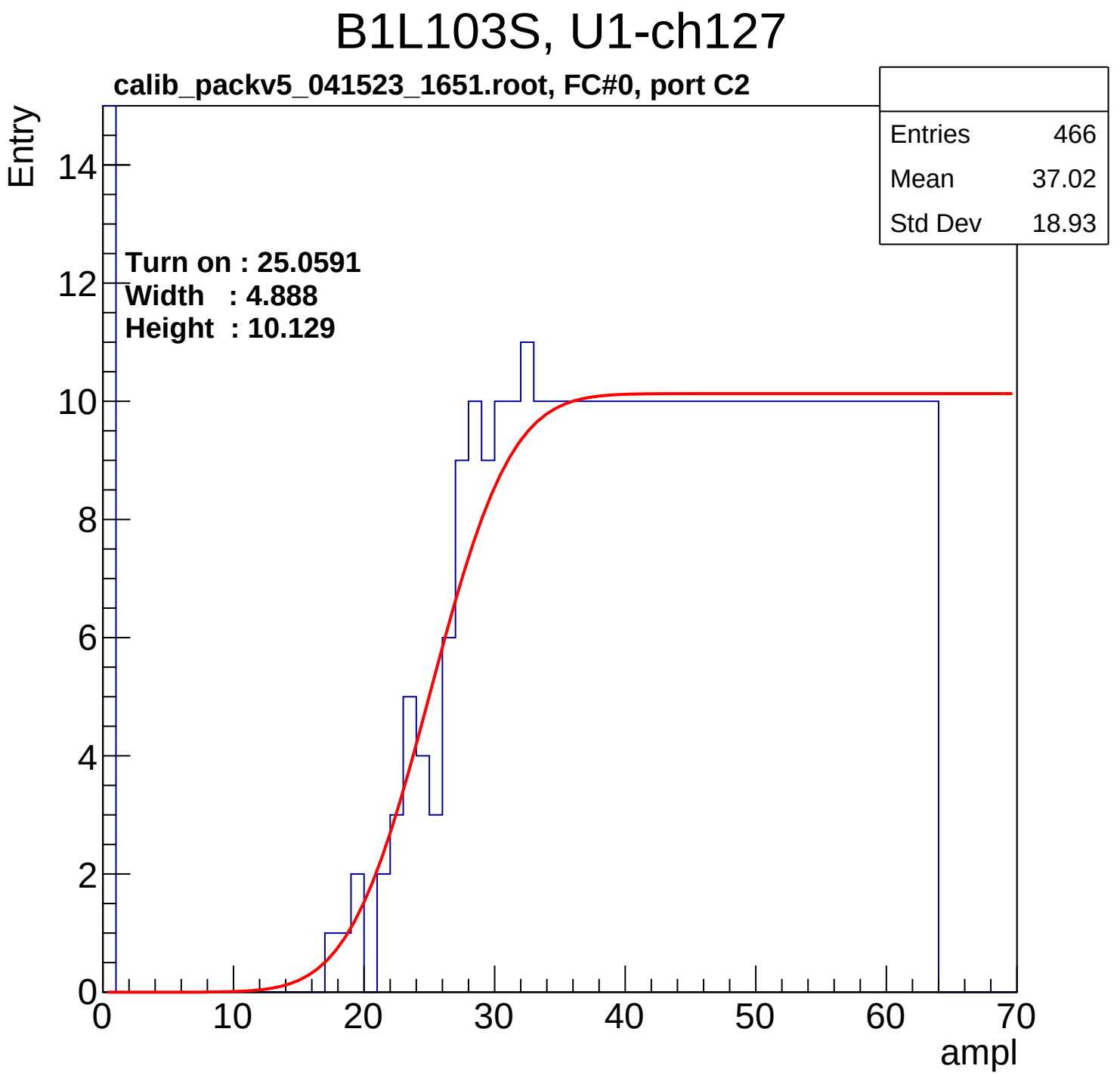

B1L103S, U1-ch127
calib_packv5_041523_1651.root, FC#0, port C2
Entries 466
Mean 37.02
Std Dev 18.93
Turn on : 25.0591
Width : 4.888
Height : 10.129
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U1-ch127
calib_packv5_041523_1651.root, FC#0, port C2
Entries 466
Mean 37.02
Std Dev 18.93
Turn on : 25.0591
Width : 4.888
Height : 10.129
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70