

B0L001S, U3-ch0

calib_packv5_042523_0143.root, FC#9, port A1

Entries	358
Mean	45.11
Std Dev	11.59

Turn on : 28.6271

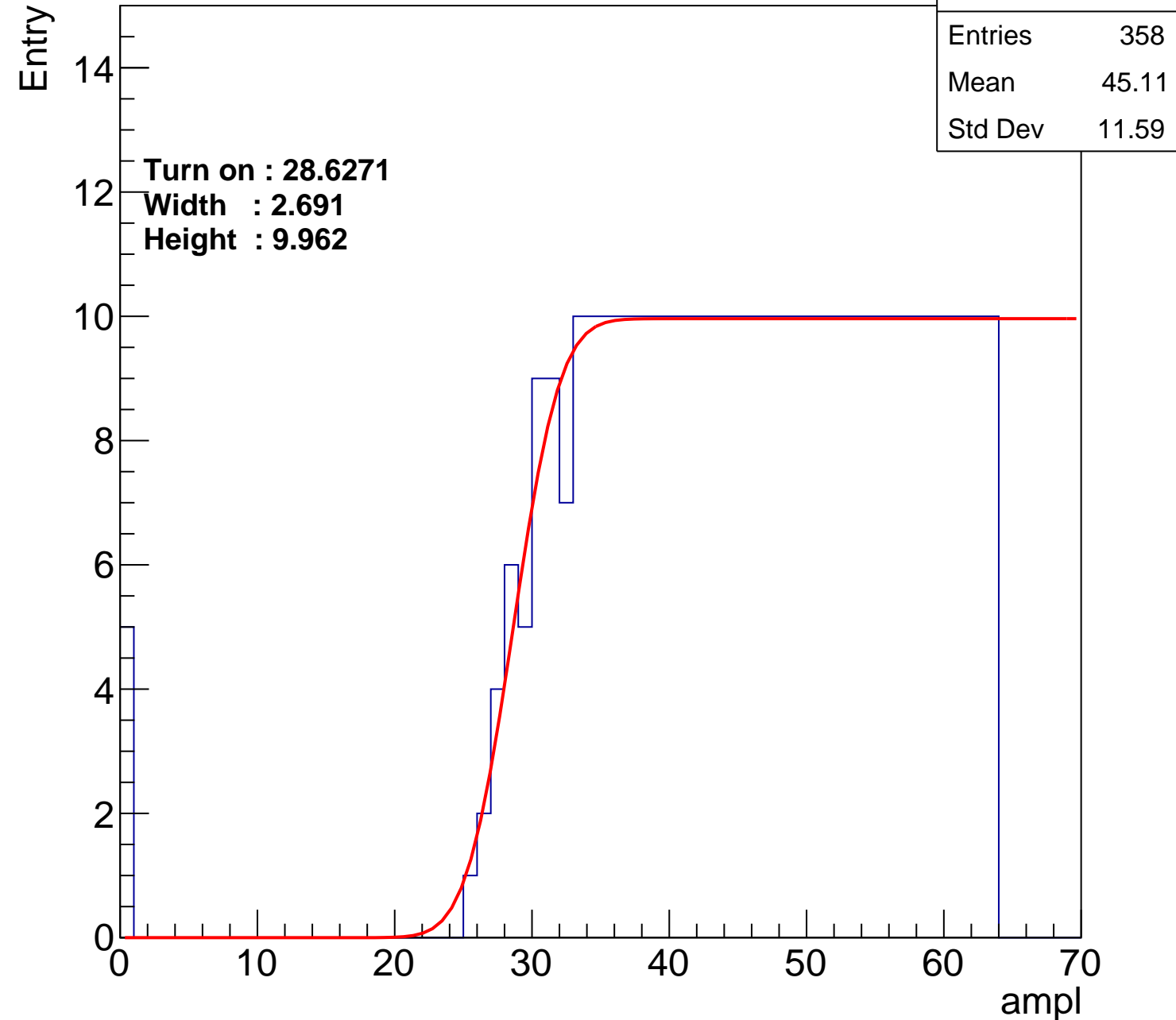
Width : 2.691

Height : 9.962

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch1

calib_packv5_042523_0143.root, FC#9, port A1

Entries	363
Mean	45.16
Std Dev	10.9

Turn on : 28.2131

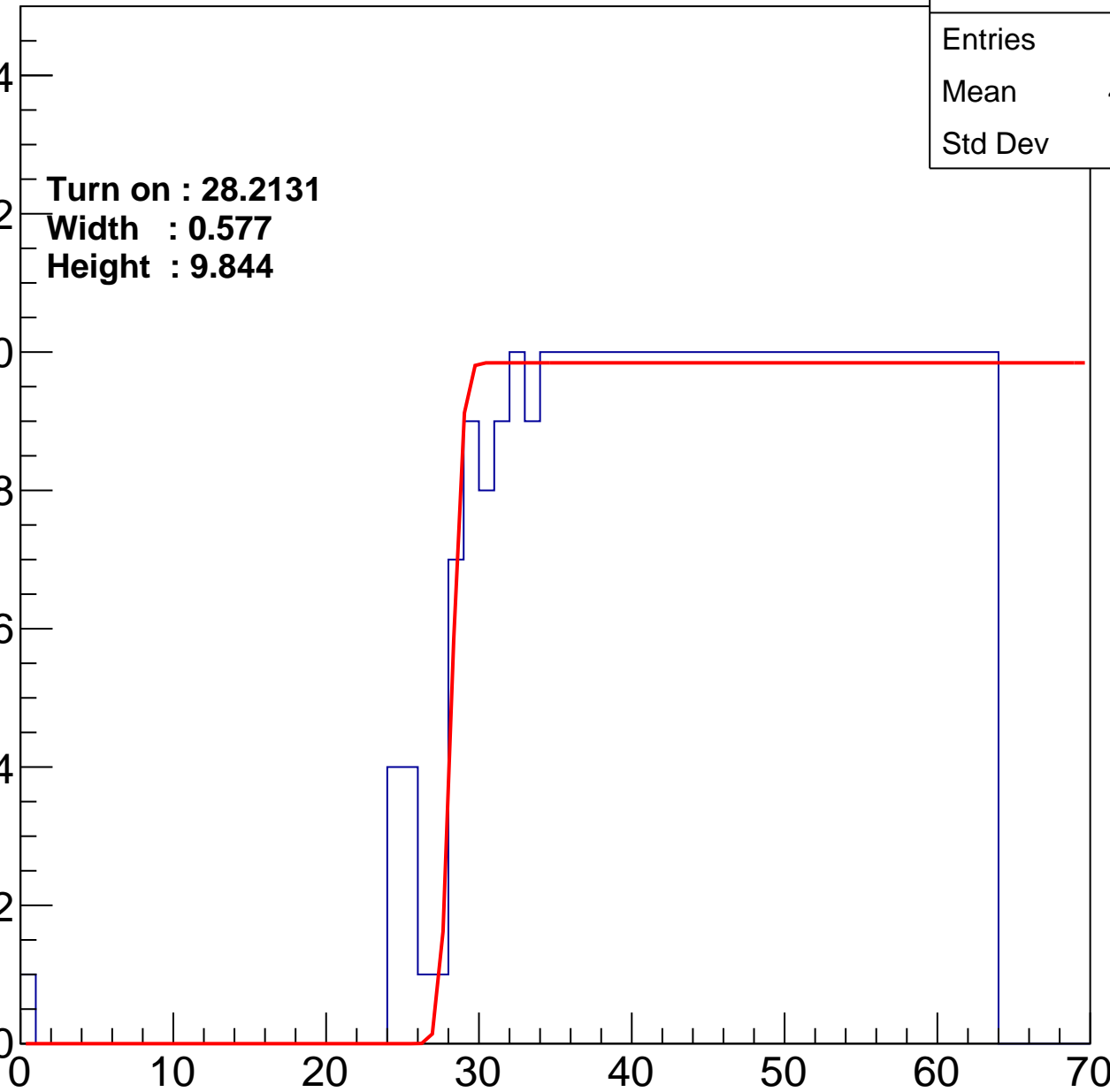
Width : 0.577

Height : 9.844

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch2

calib_packv5_042523_0143.root, FC#9, port A1

Entries	372
Mean	44.75
Std Dev	11.08

Turn on : 26.8683

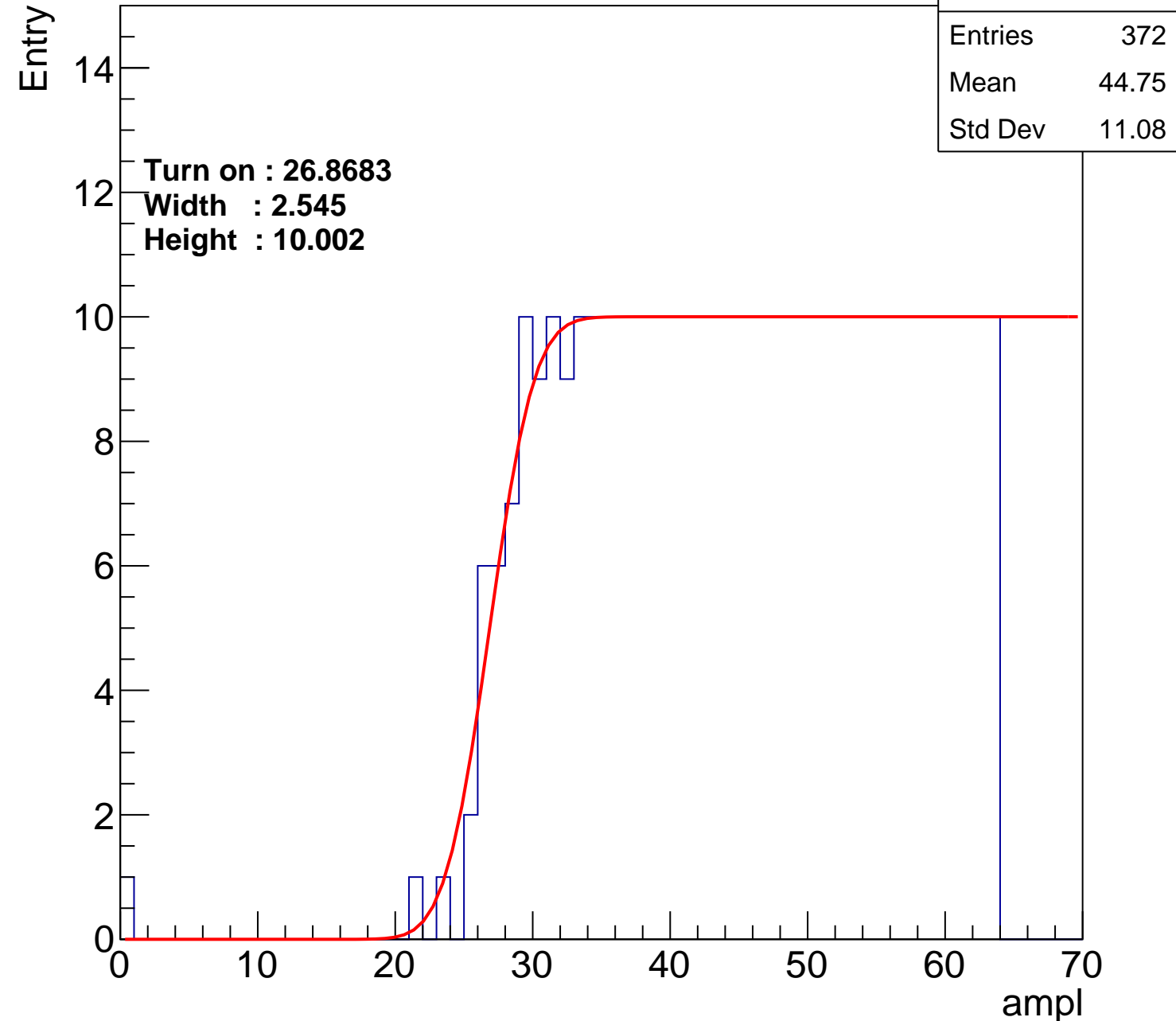
Width : 2.545

Height : 10.002

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch3

calib_packv5_042523_0143.root, FC#9, port A1

Entries	363
Mean	44.98
Std Dev	11.36

Turn on : 28.2501

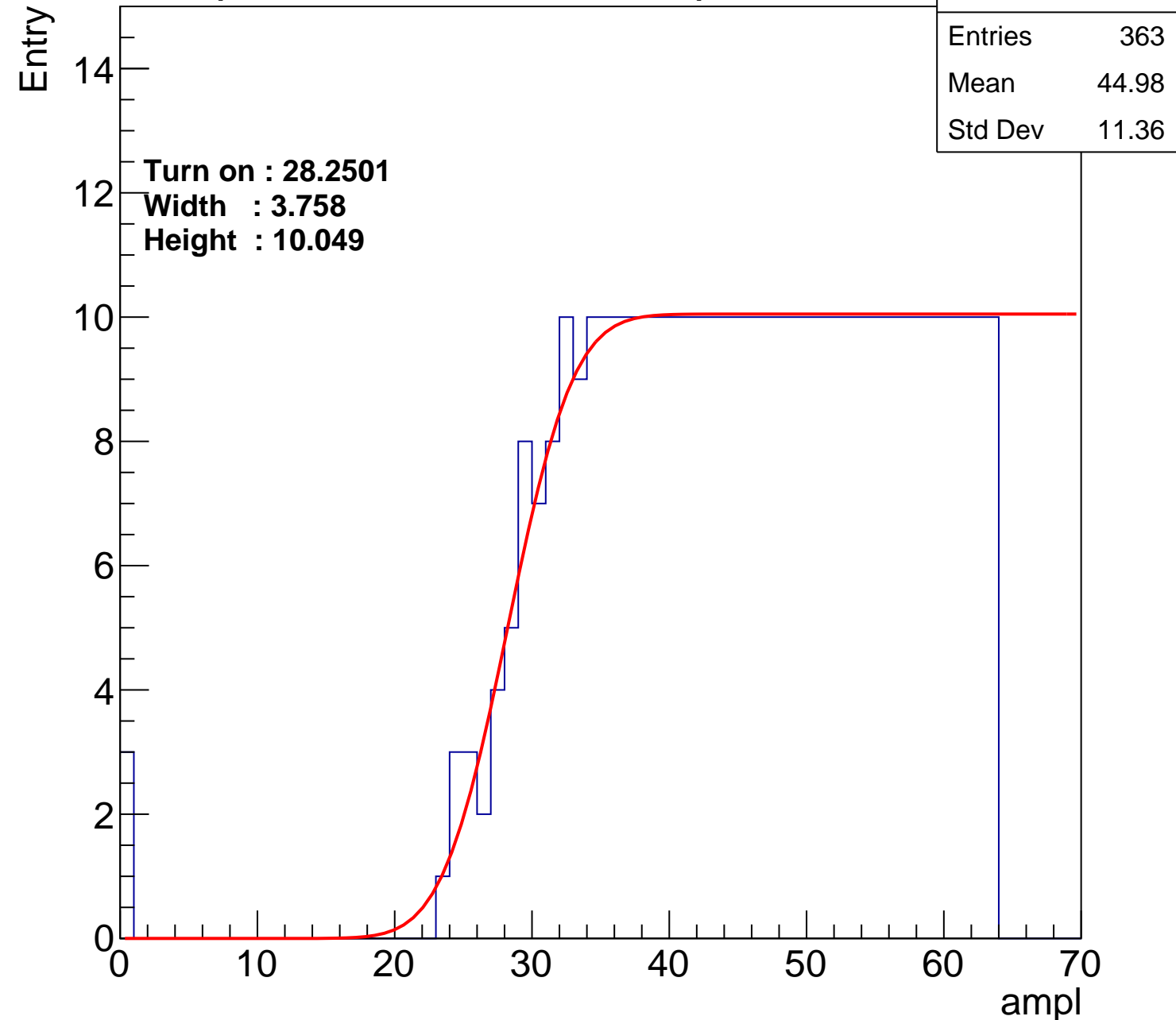
Width : 3.758

Height : 10.049

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch4

calib_packv5_042523_0143.root, FC#9, port A1

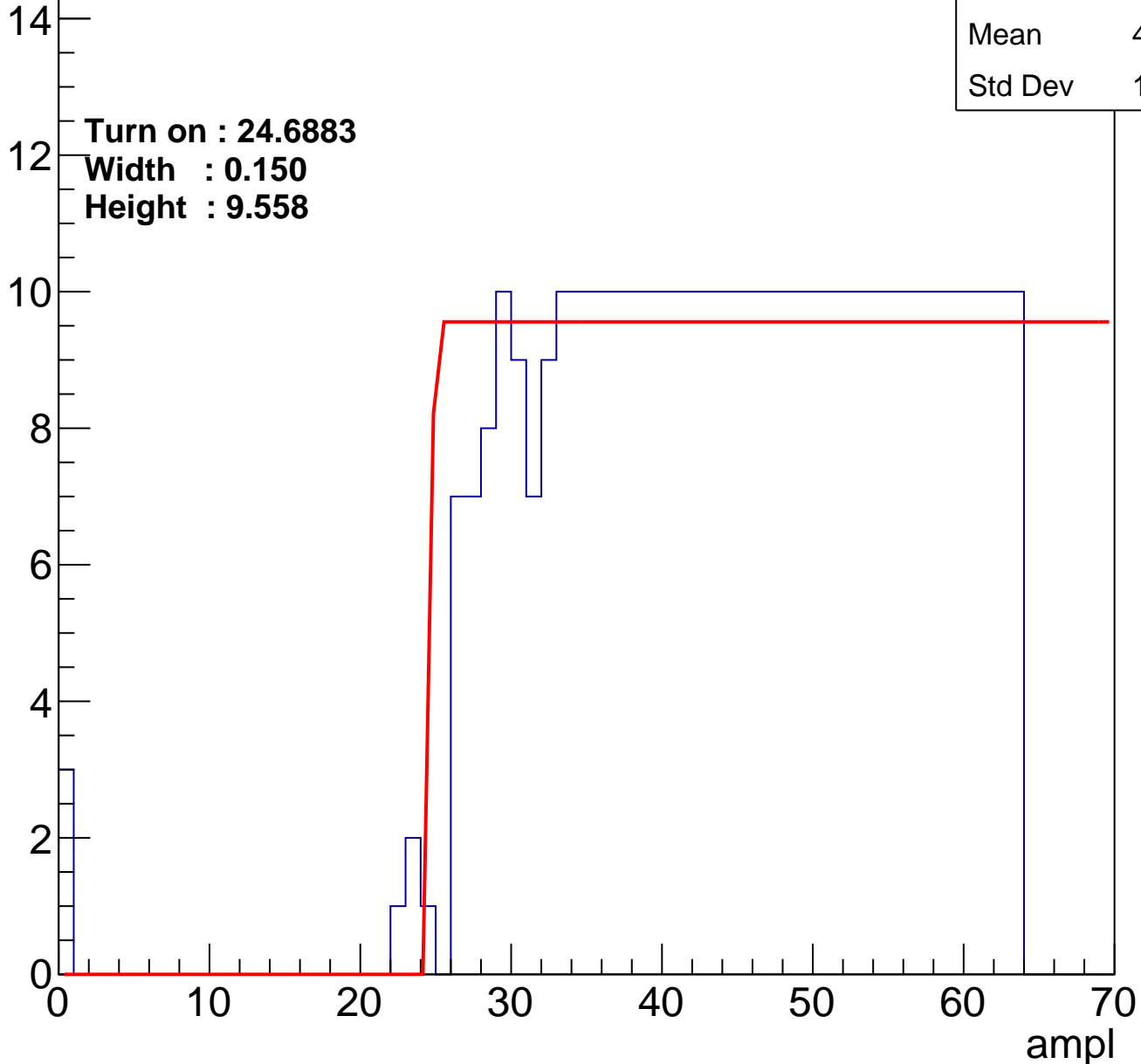
Entries	374
Mean	44.47
Std Dev	11.57

Turn on : 24.6883

Width : 0.150

Height : 9.558

Entry



B0L001S, U3-ch5

calib_packv5_042523_0143.root, FC#9, port A1

Entries	363
Mean	45.07
Std Dev	11.13

Turn on : 28.4112

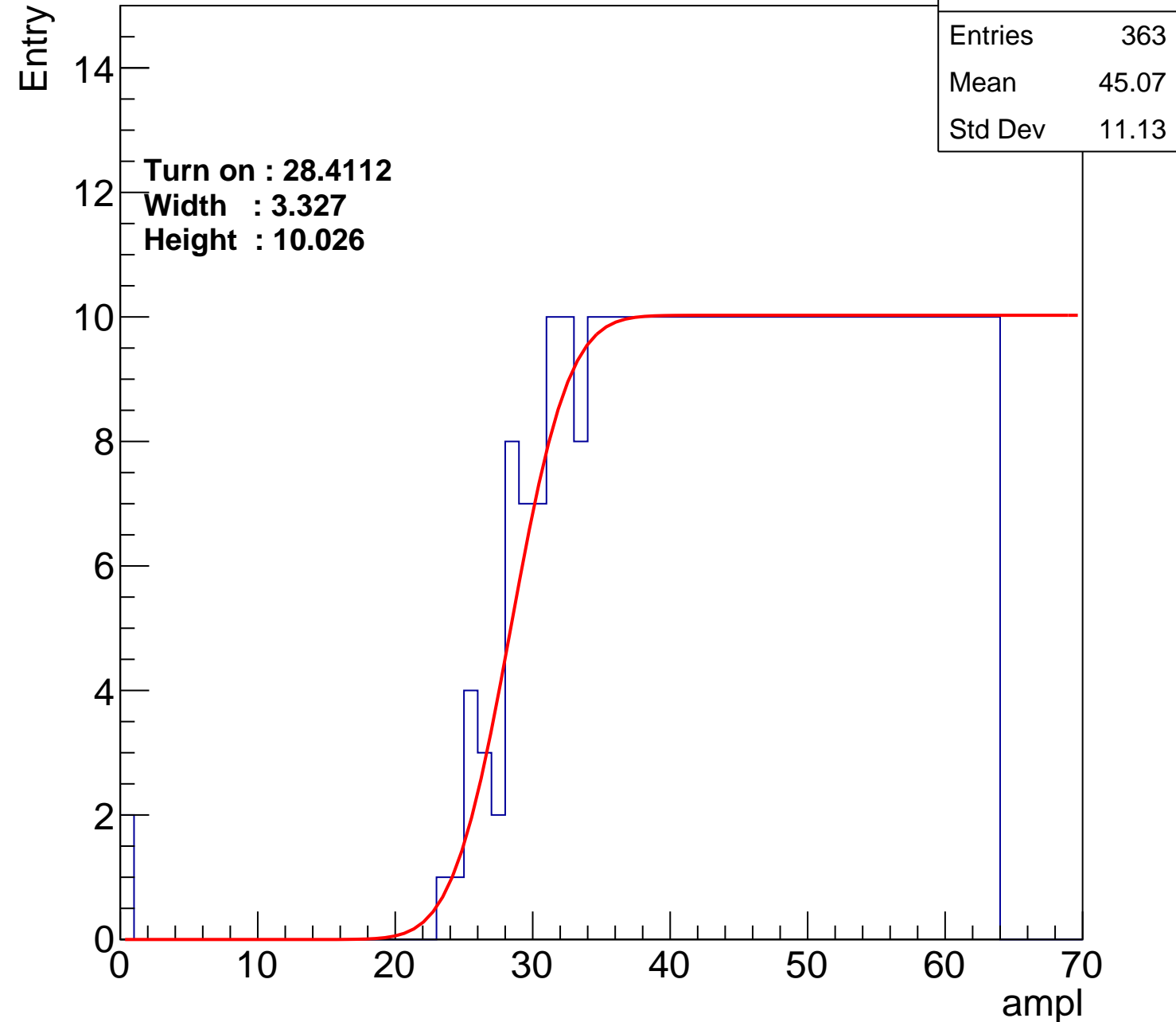
Width : 3.327

Height : 10.026

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch6

calib_packv5_042523_0143.root, FC#9, port A1

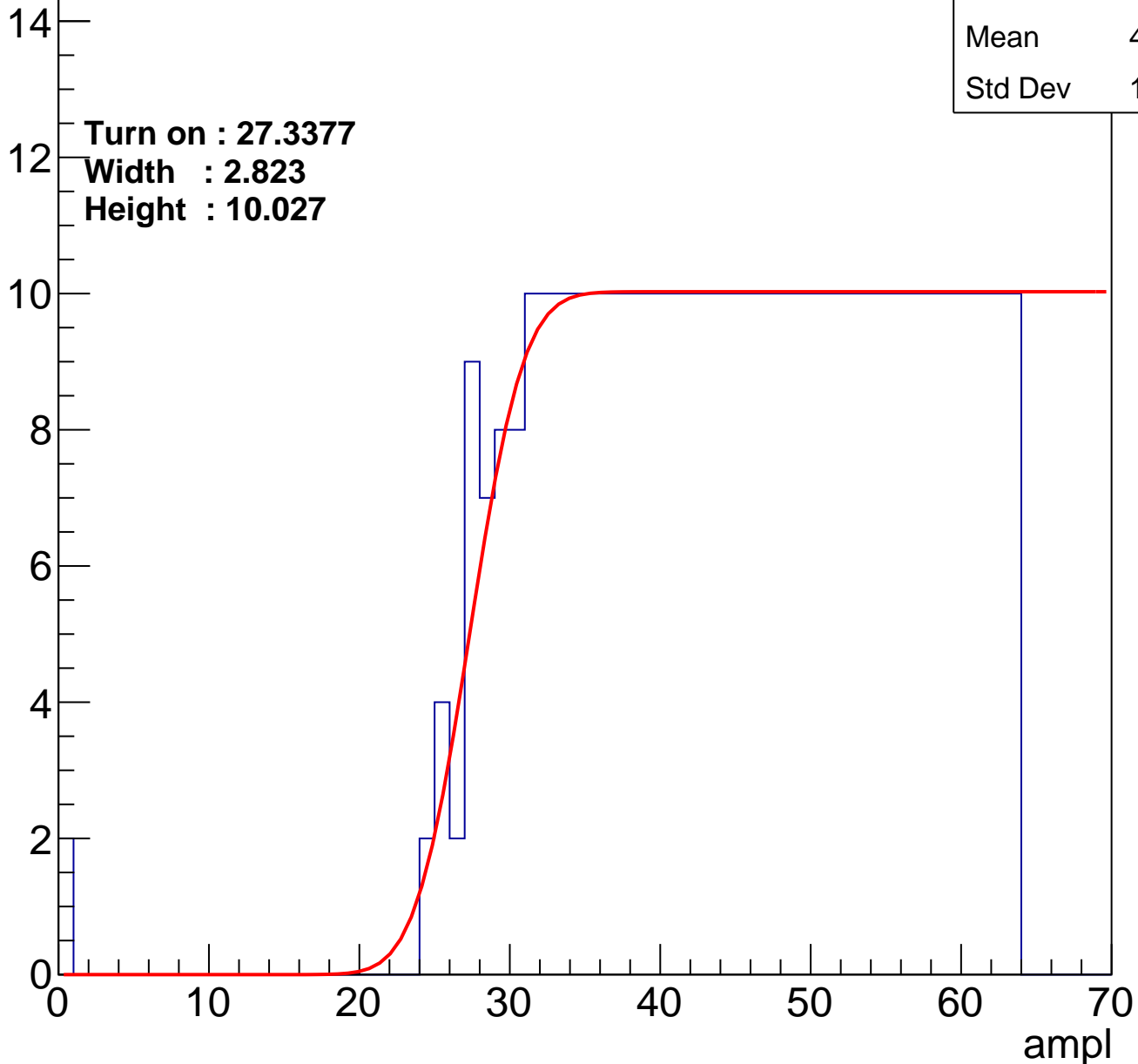
Entries	372
Mean	44.68
Std Dev	11.27

Turn on : 27.3377

Width : 2.823

Height : 10.027

Entry



B0L001S, U3-ch7

calib_packv5_042523_0143.root, FC#9, port A1

Entries	362
Mean	44.99
Std Dev	11.48

Turn on : 28.1861

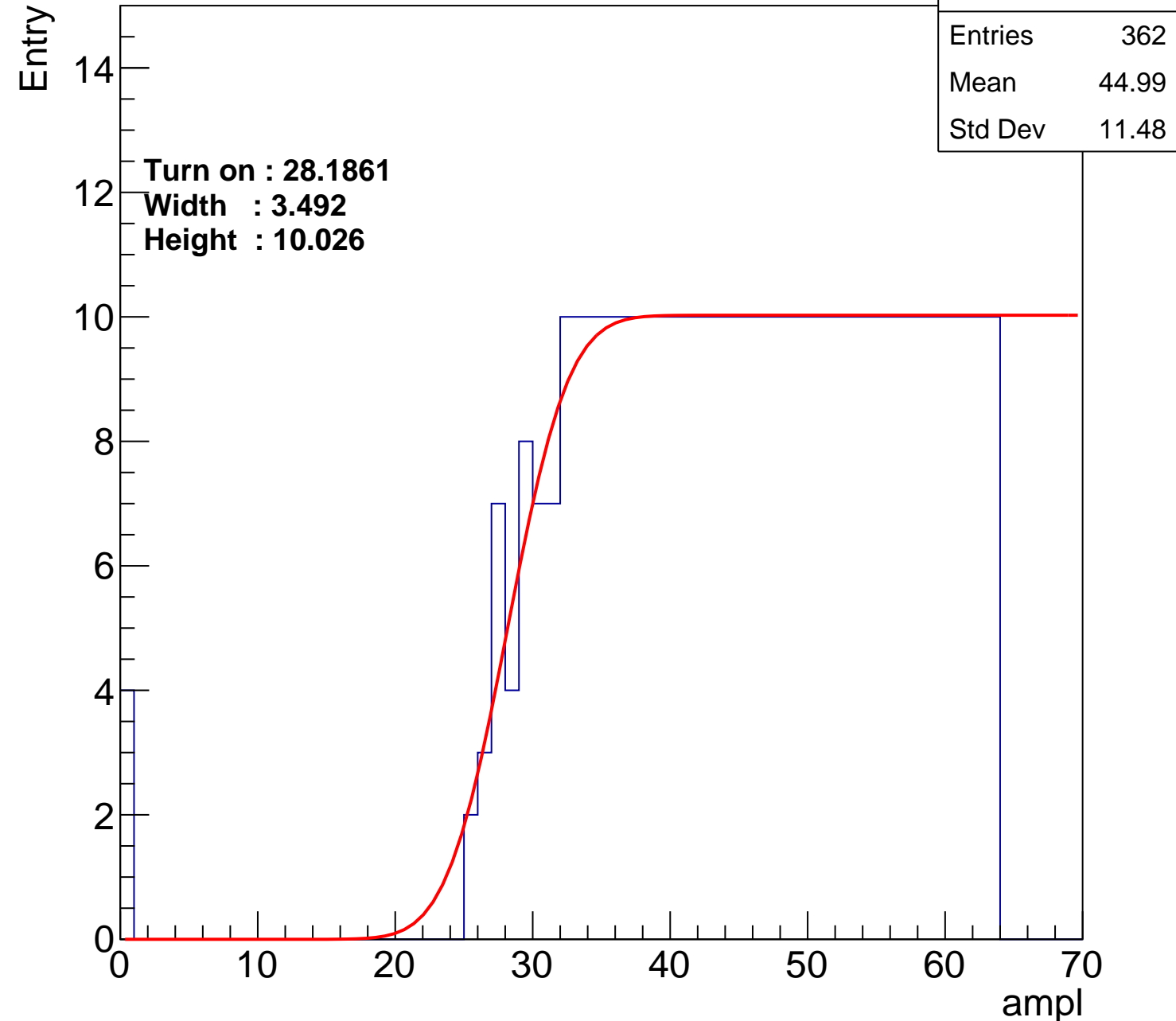
Width : 3.492

Height : 10.026

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch8

calib_packv5_042523_0143.root, FC#9, port A1

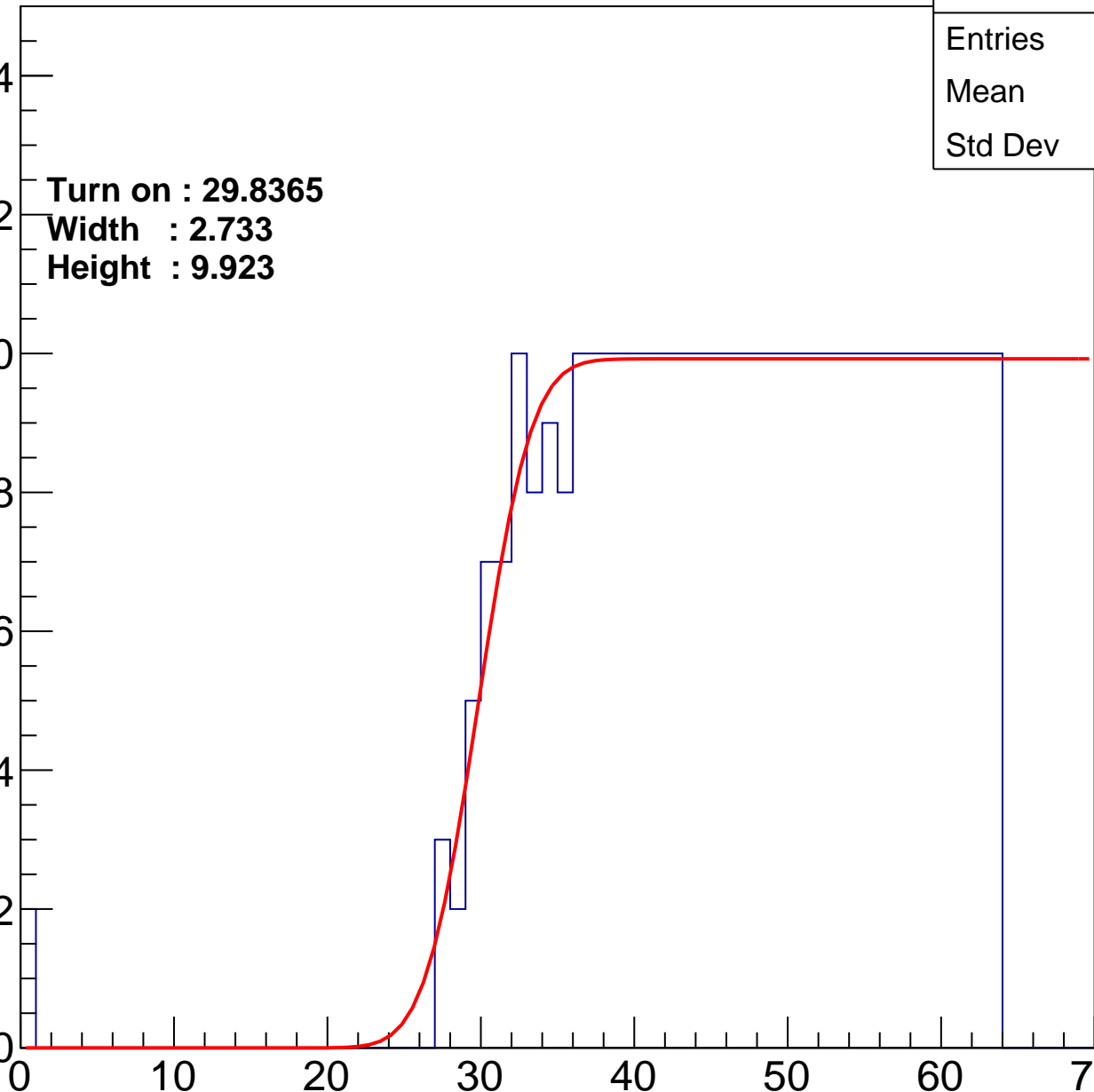
Entry

14
12
10
8
6
4
2
0

Turn on : 29.8365
Width : 2.733
Height : 9.923

Entries	341
Mean	46.16
Std Dev	10.56

ampl



B0L001S, U3-ch9

calib_packv5_042523_0143.root, FC#9, port A1

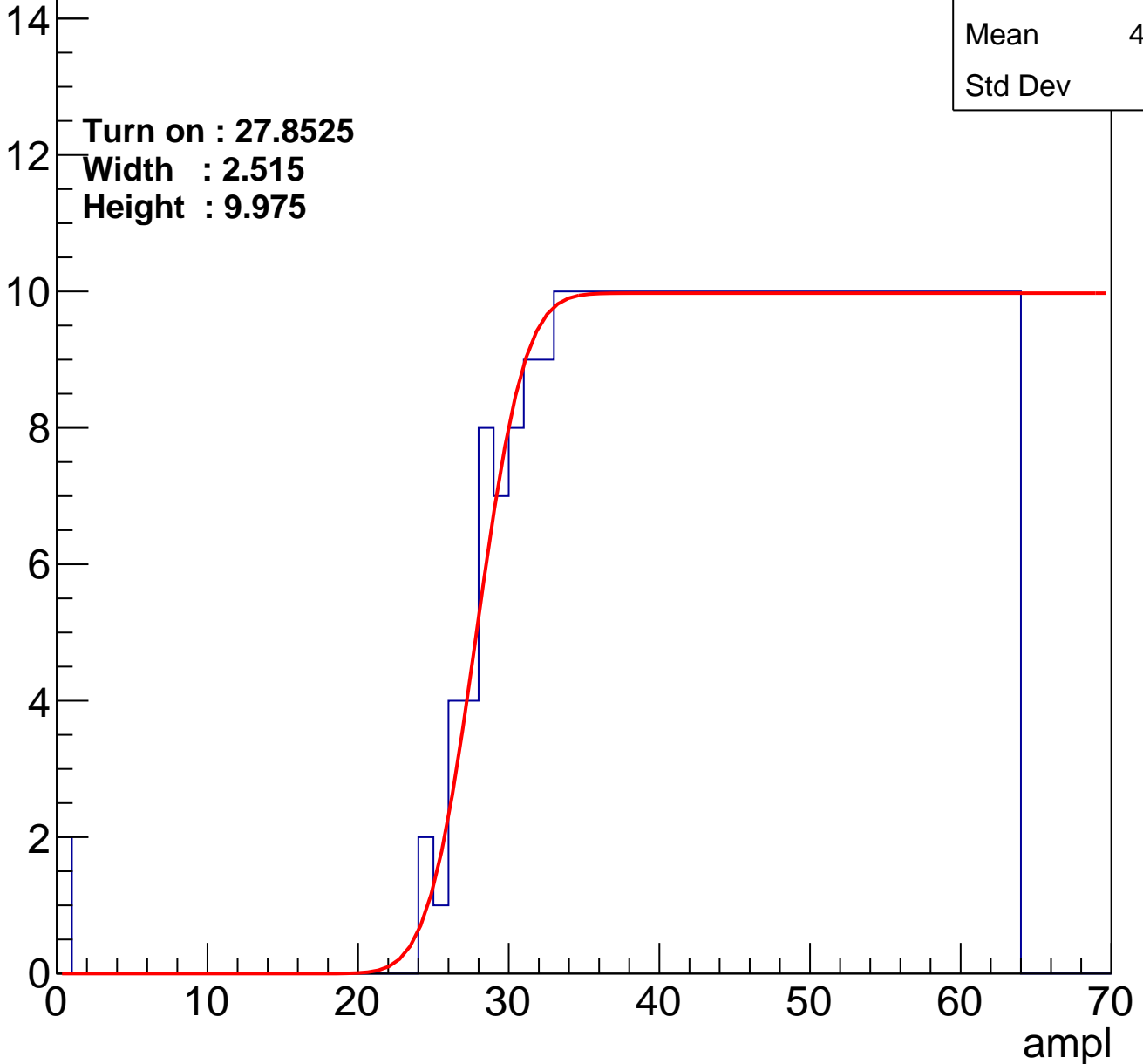
Entries	364
Mean	45.05
Std Dev	11.1

Turn on : 27.8525

Width : 2.515

Height : 9.975

Entry



B0L001S, U3-ch10

calib_packv5_042523_0143.root, FC#9, port A1

Entries	361
Mean	45.01
Std Dev	11.51

Turn on : 28.3726

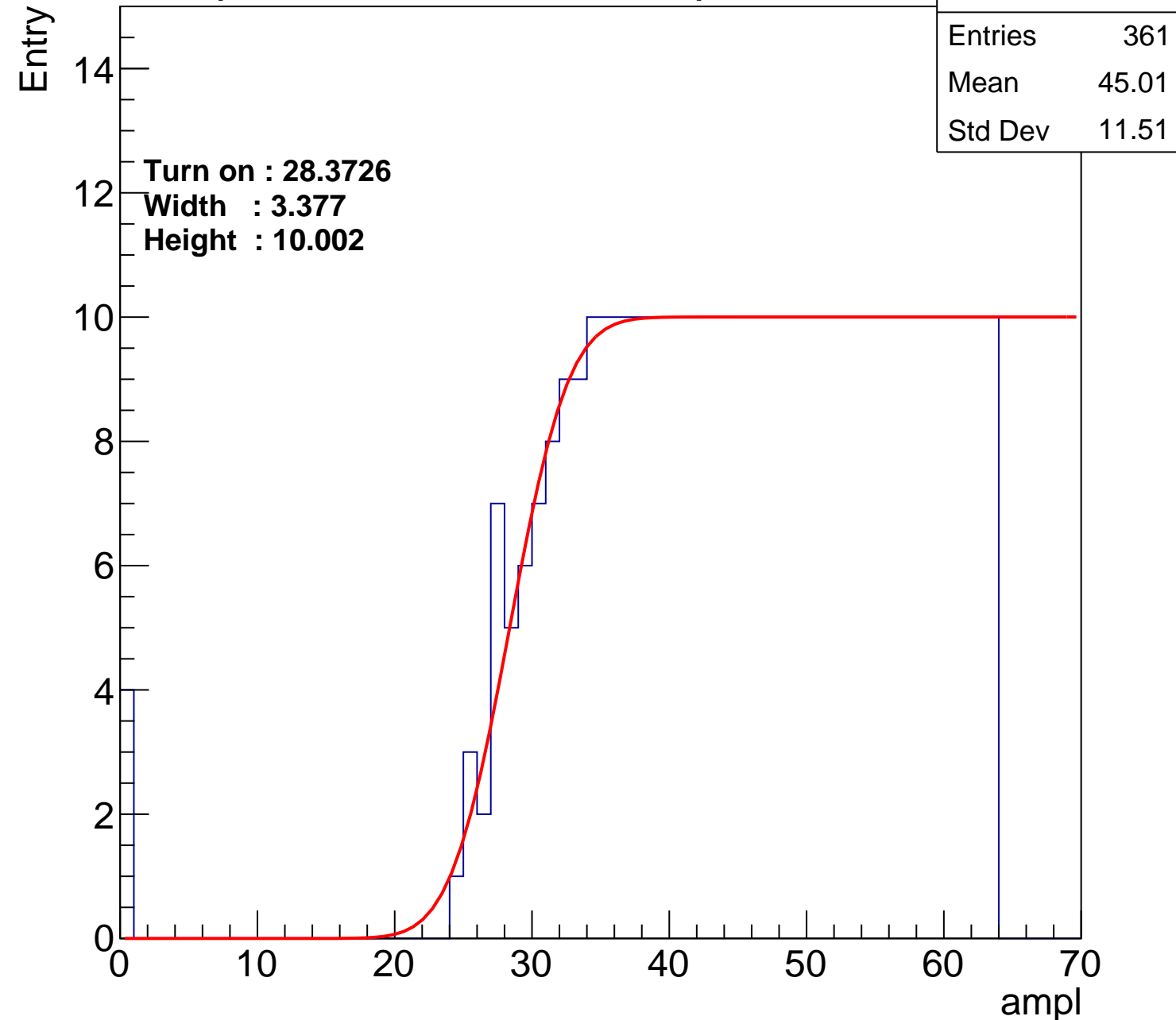
Width : 3.377

Height : 10.002

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch11

calib_packv5_042523_0143.root, FC#9, port A1

Entries	365
Mean	45.07
Std Dev	10.93

Turn on : 28.2268

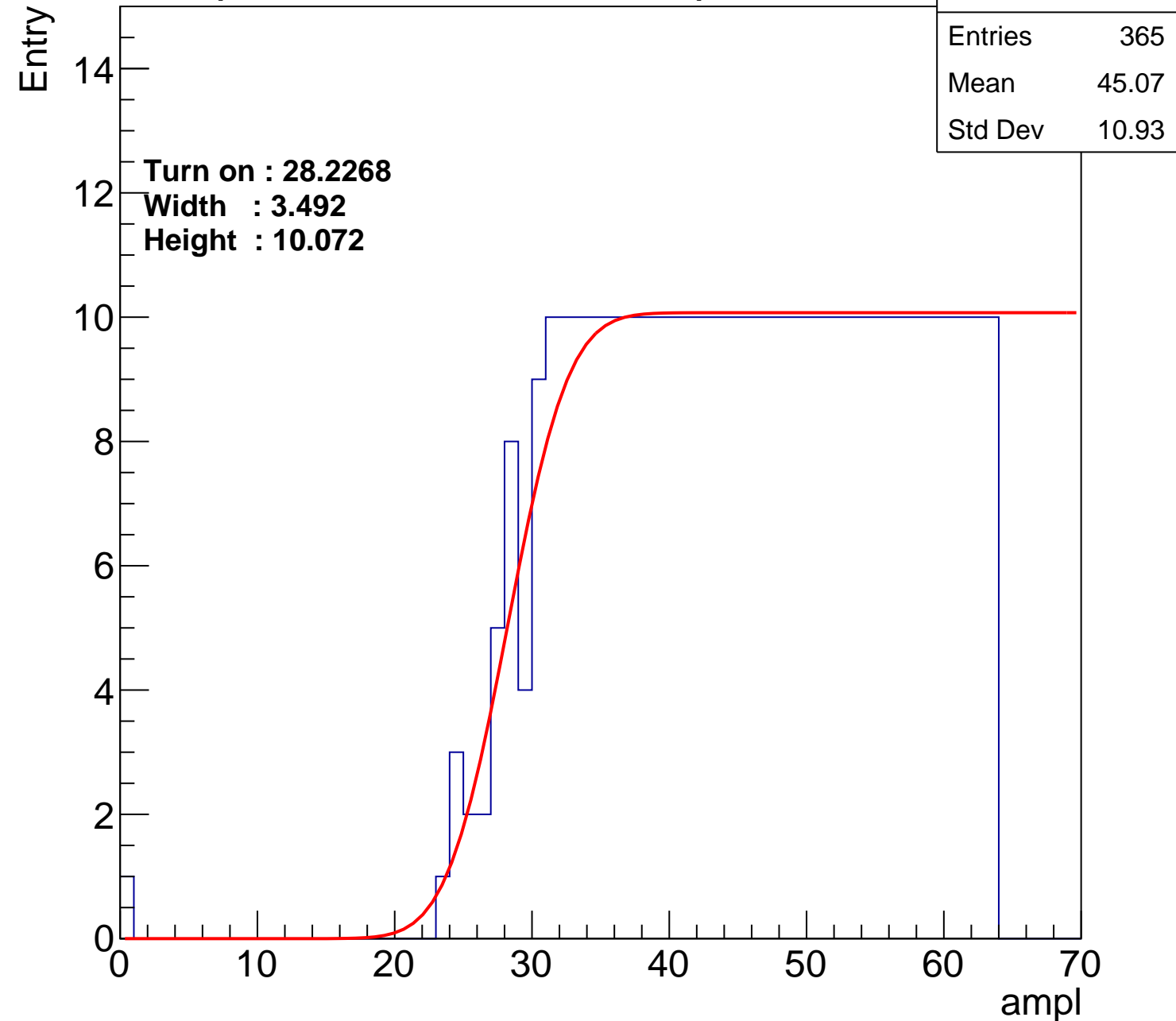
Width : 3.492

Height : 10.072

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch12

calib_packv5_042523_0143.root, FC#9, port A1

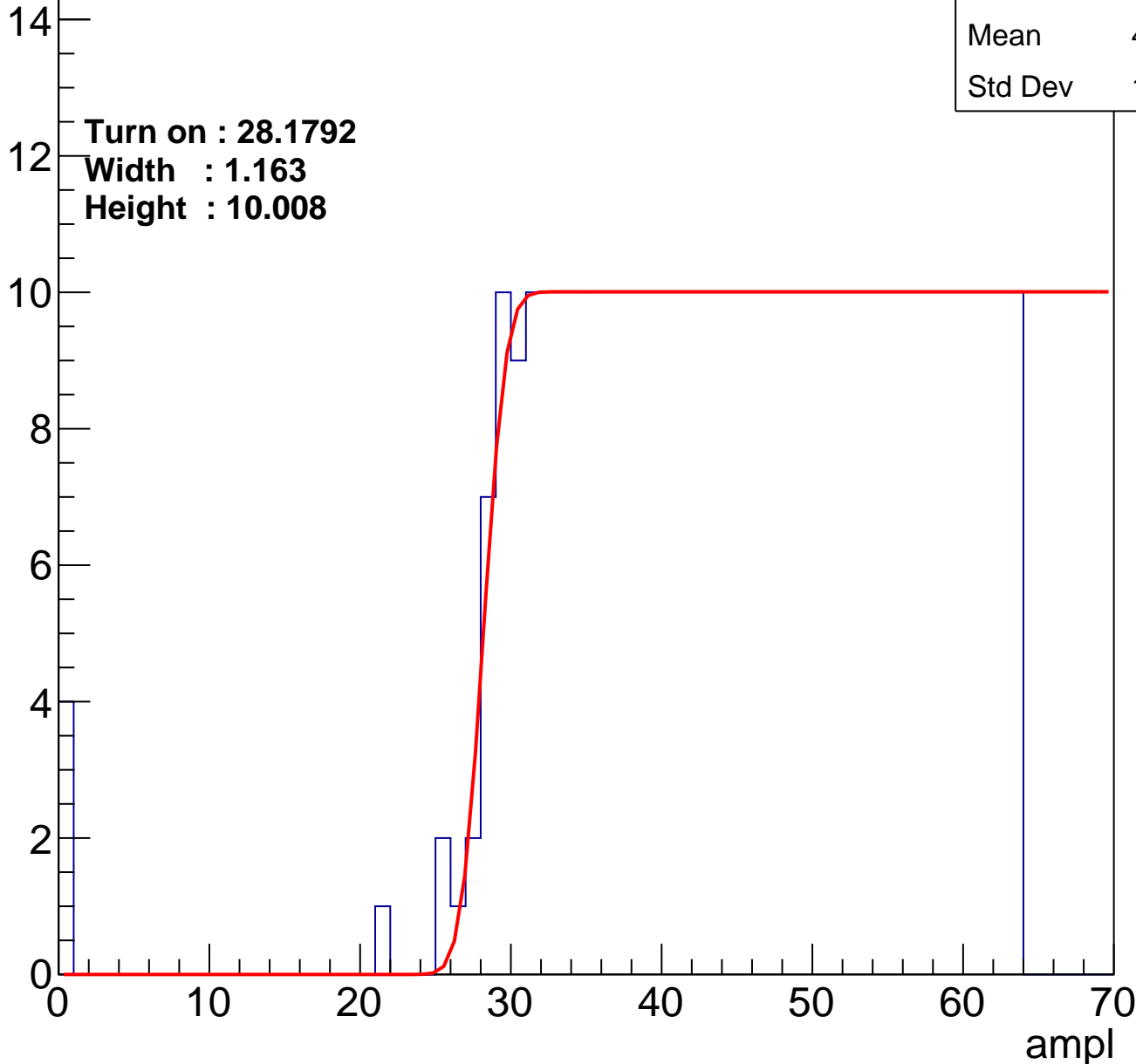
Entries	366
Mean	44.86
Std Dev	11.49

Turn on : 28.1792

Width : 1.163

Height : 10.008

Entry



B0L001S, U3-ch13

calib_packv5_042523_0143.root, FC#9, port A1

Entries	359
Mean	45.37
Std Dev	10.75

Turn on : 28.0302

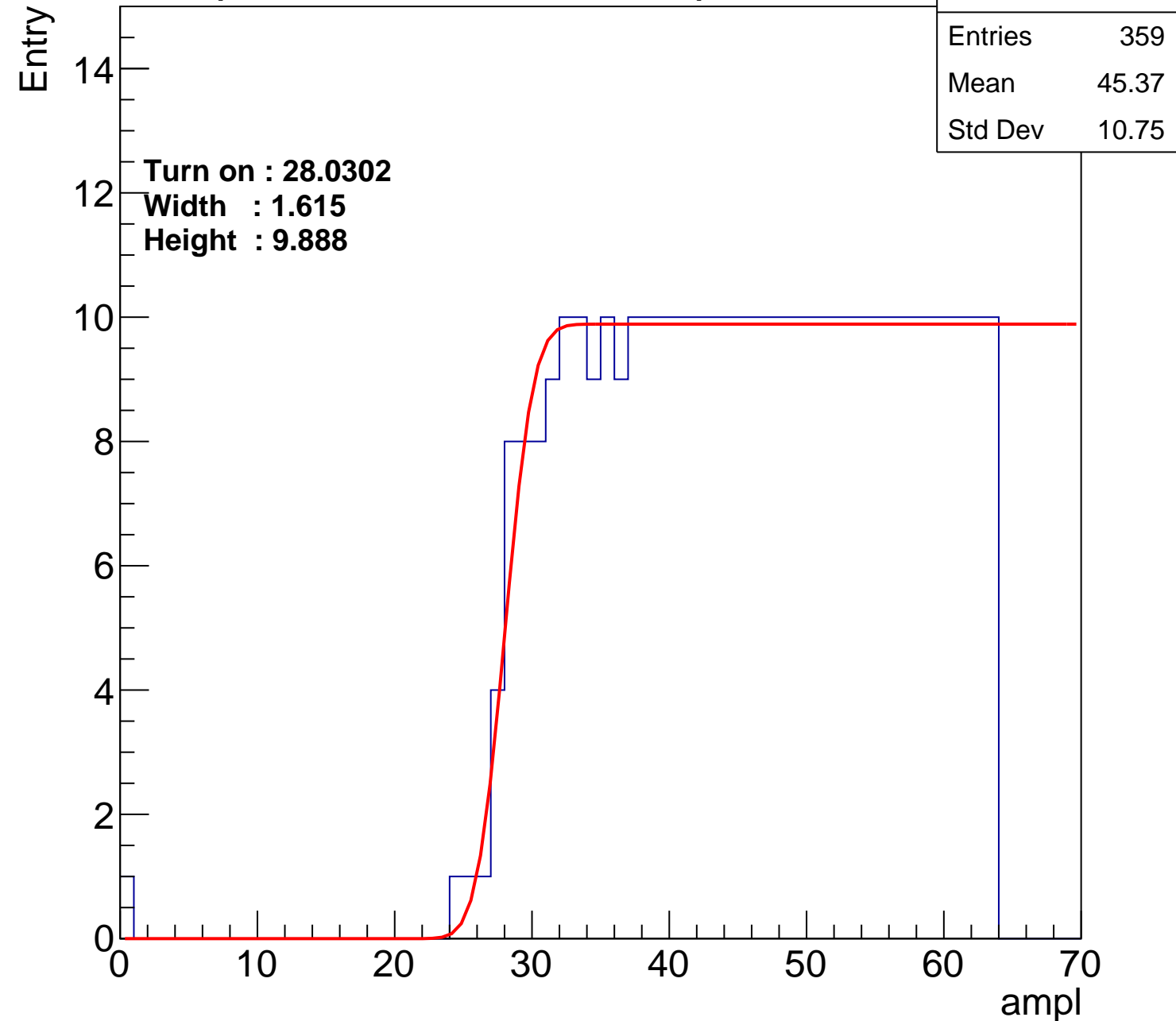
Width : 1.615

Height : 9.888

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch14

calib_packv5_042523_0143.root, FC#9, port A1

Entries	374
Mean	44.39
Std Dev	11.78

Turn on : 26.6584

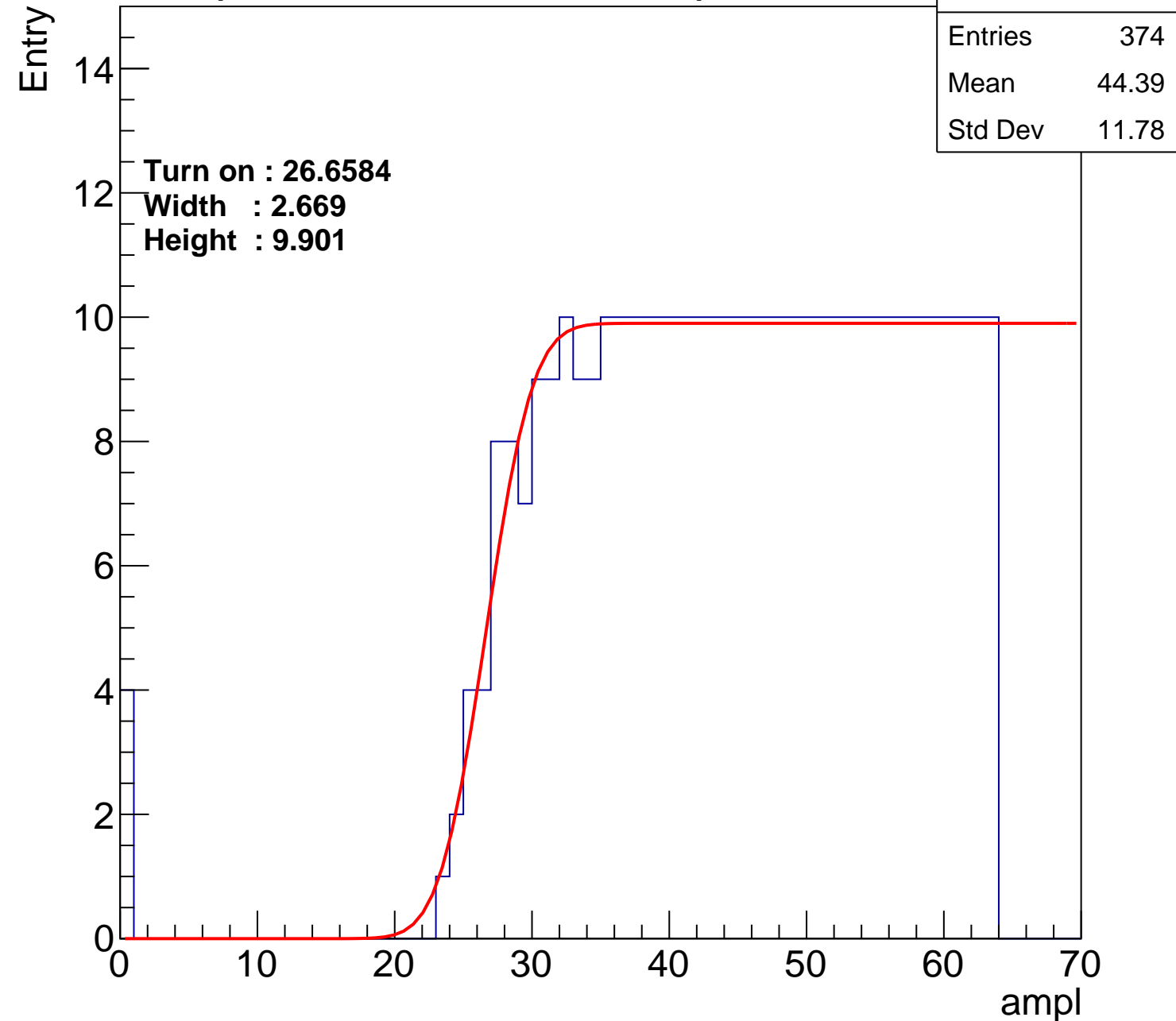
Width : 2.669

Height : 9.901

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch15

calib_packv5_042523_0143.root, FC#9, port A1

Entries	367
Mean	44.8
Std Dev	11.51

Turn on : 27.4288

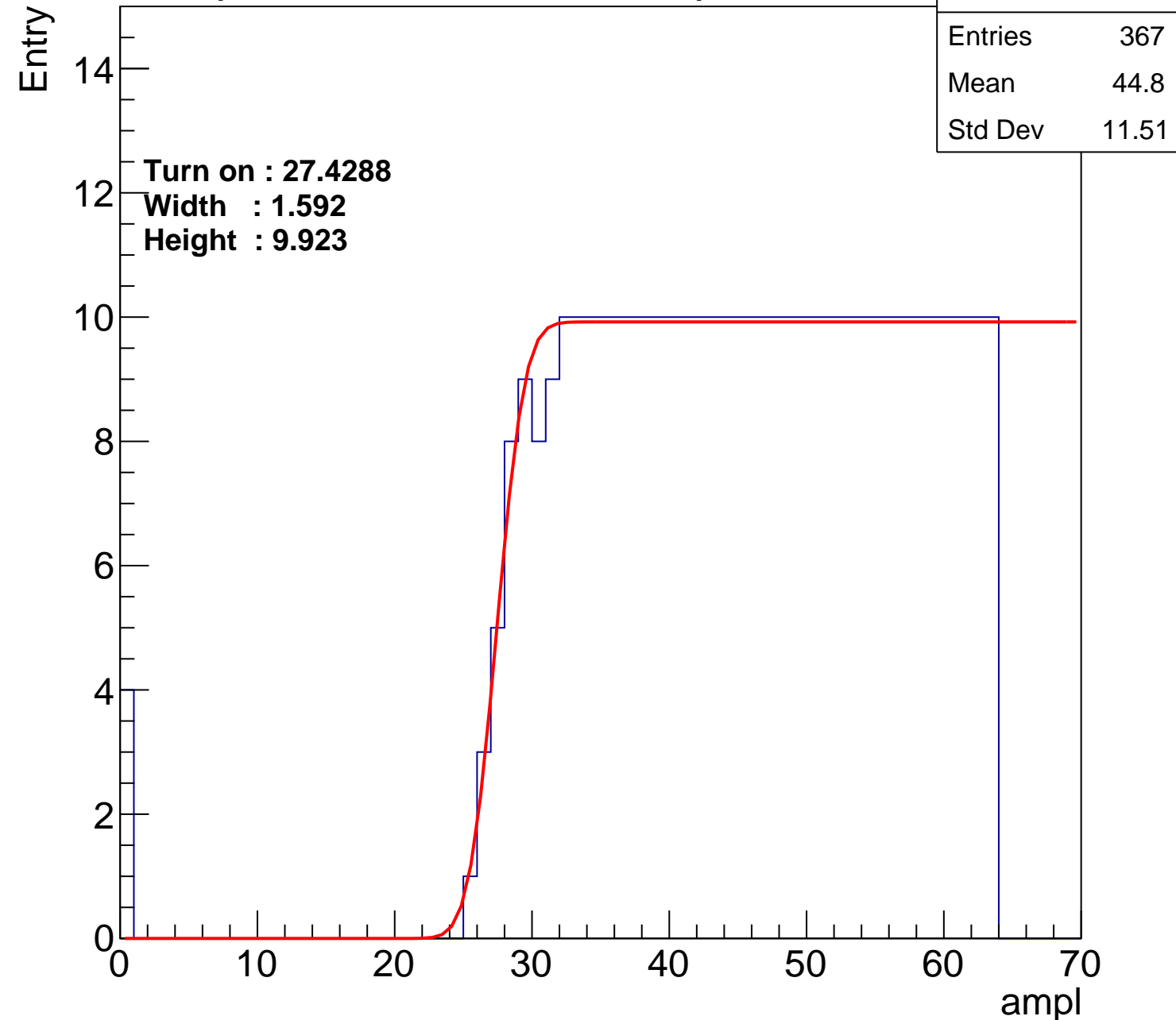
Width : 1.592

Height : 9.923

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch16

calib_packv5_042523_0143.root, FC#9, port A1

Entries	362
Mean	45.09
Std Dev	11.15

Turn on : 28.4137

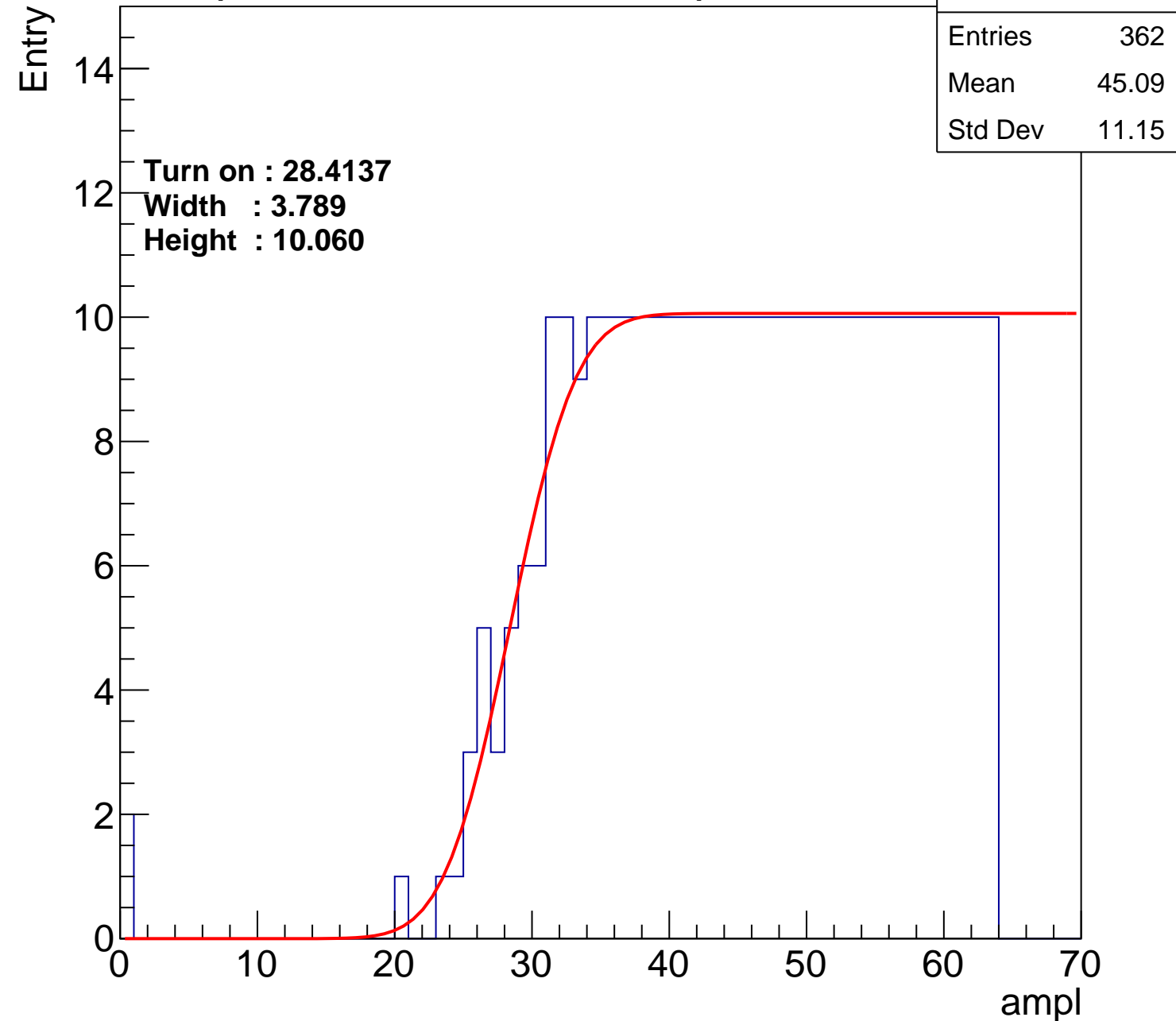
Width : 3.789

Height : 10.060

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch17

calib_packv5_042523_0143.root, FC#9, port A1

Entries	338
Mean	46.1
Std Dev	11.06

Turn on : 30.7837

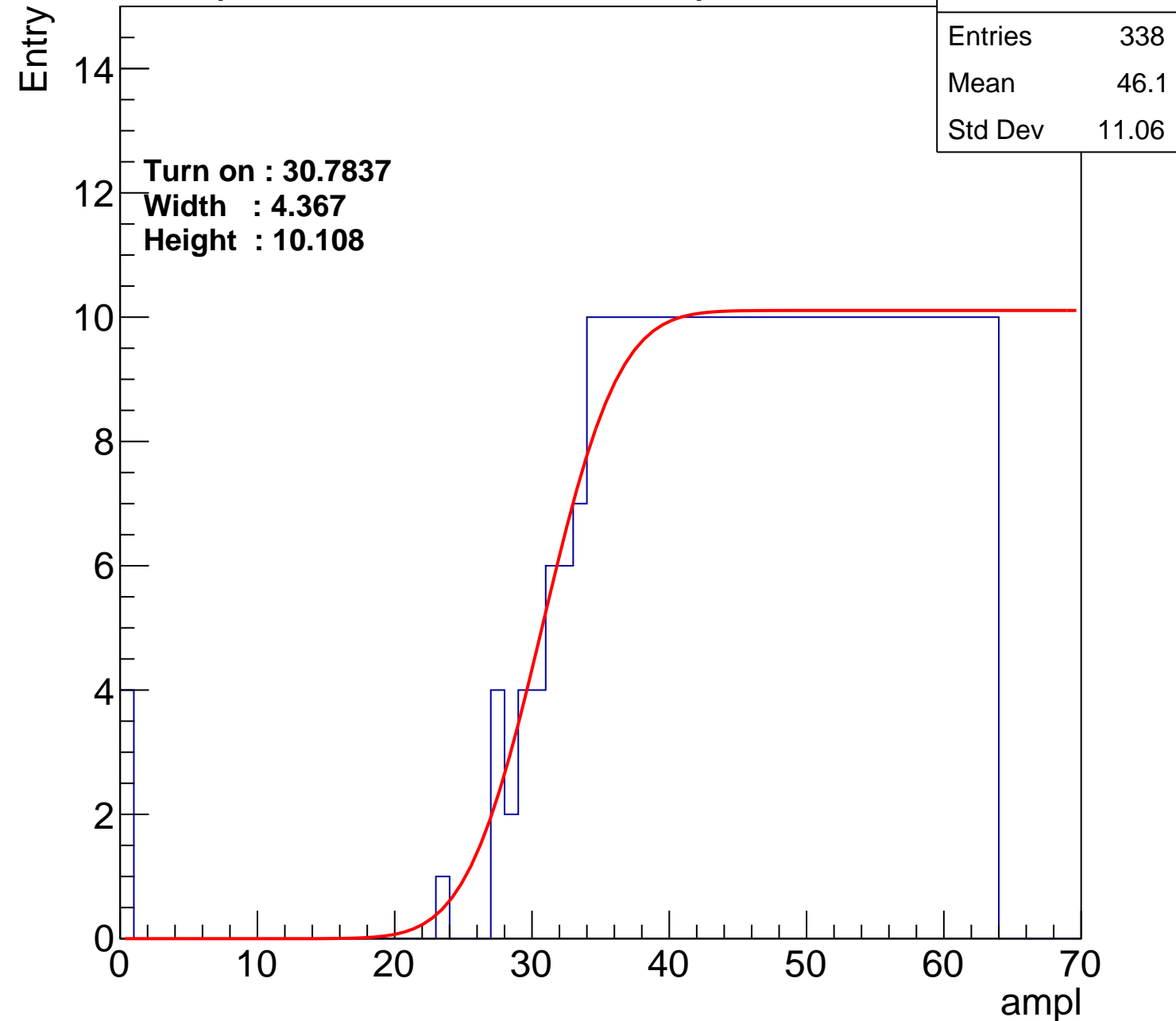
Width : 4.367

Height : 10.108

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch18

calib_packv5_042523_0143.root, FC#9, port A1

Entries	358
Mean	45.27
Std Dev	11.17

Turn on : 28.6987

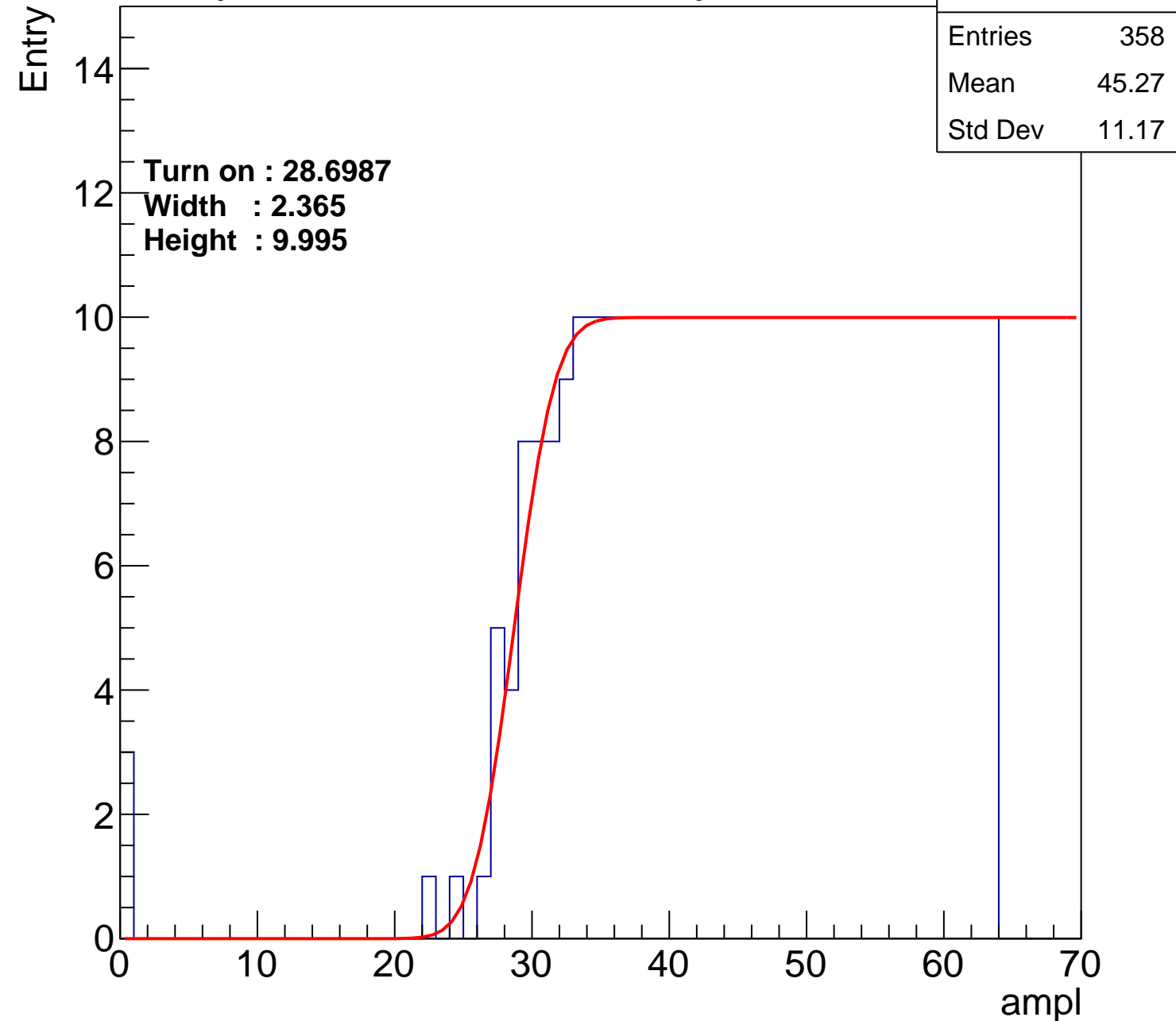
Width : 2.365

Height : 9.995

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch19

calib_packv5_042523_0143.root, FC#9, port A1

Entries	359
Mean	45.16
Std Dev	11.39

Turn on : 28.8316

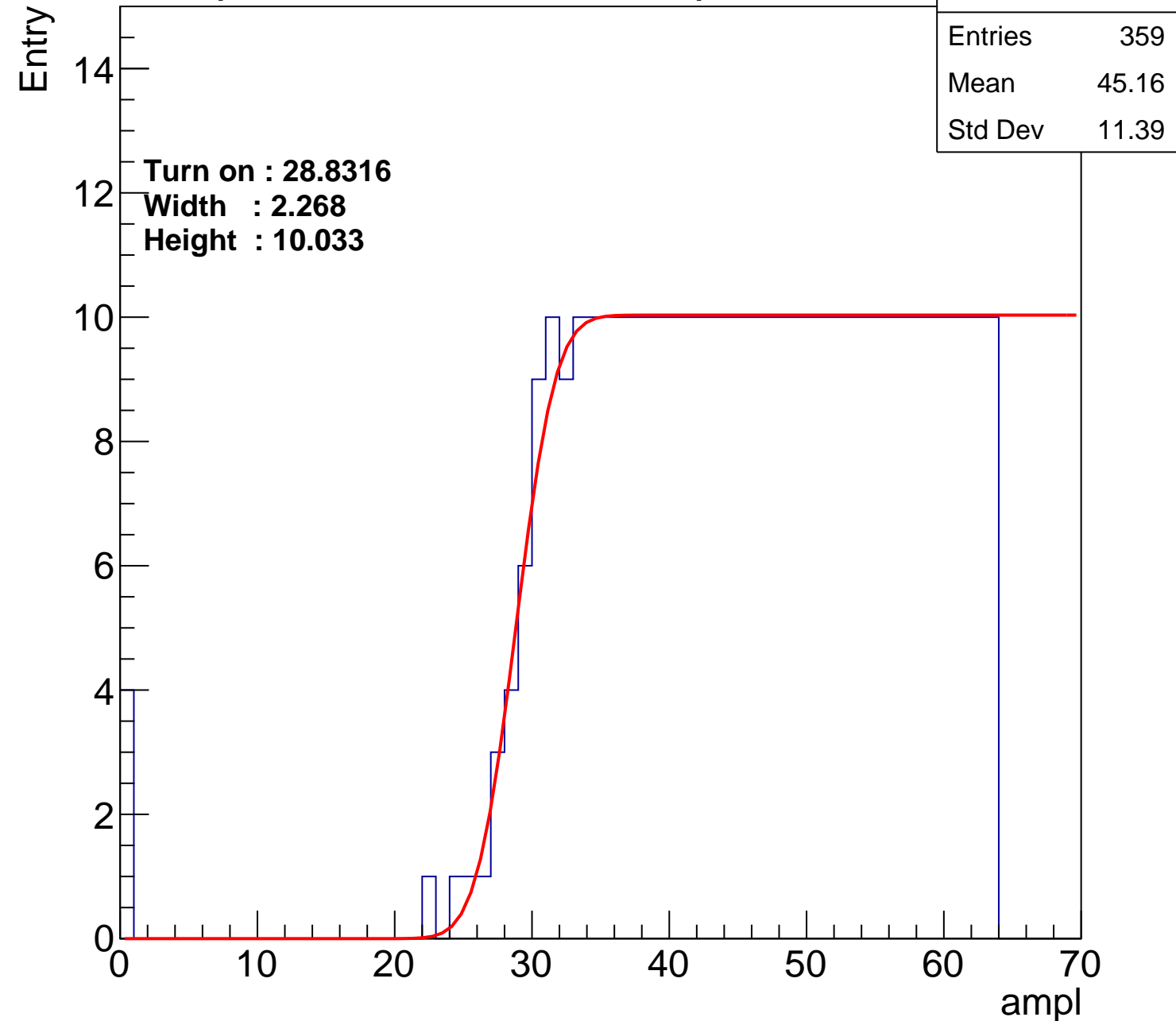
Width : 2.268

Height : 10.033

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch20

calib_packv5_042523_0143.root, FC#9, port A1

Entries	366
Mean	44.95
Std Dev	11.15

Turn on : 27.7522

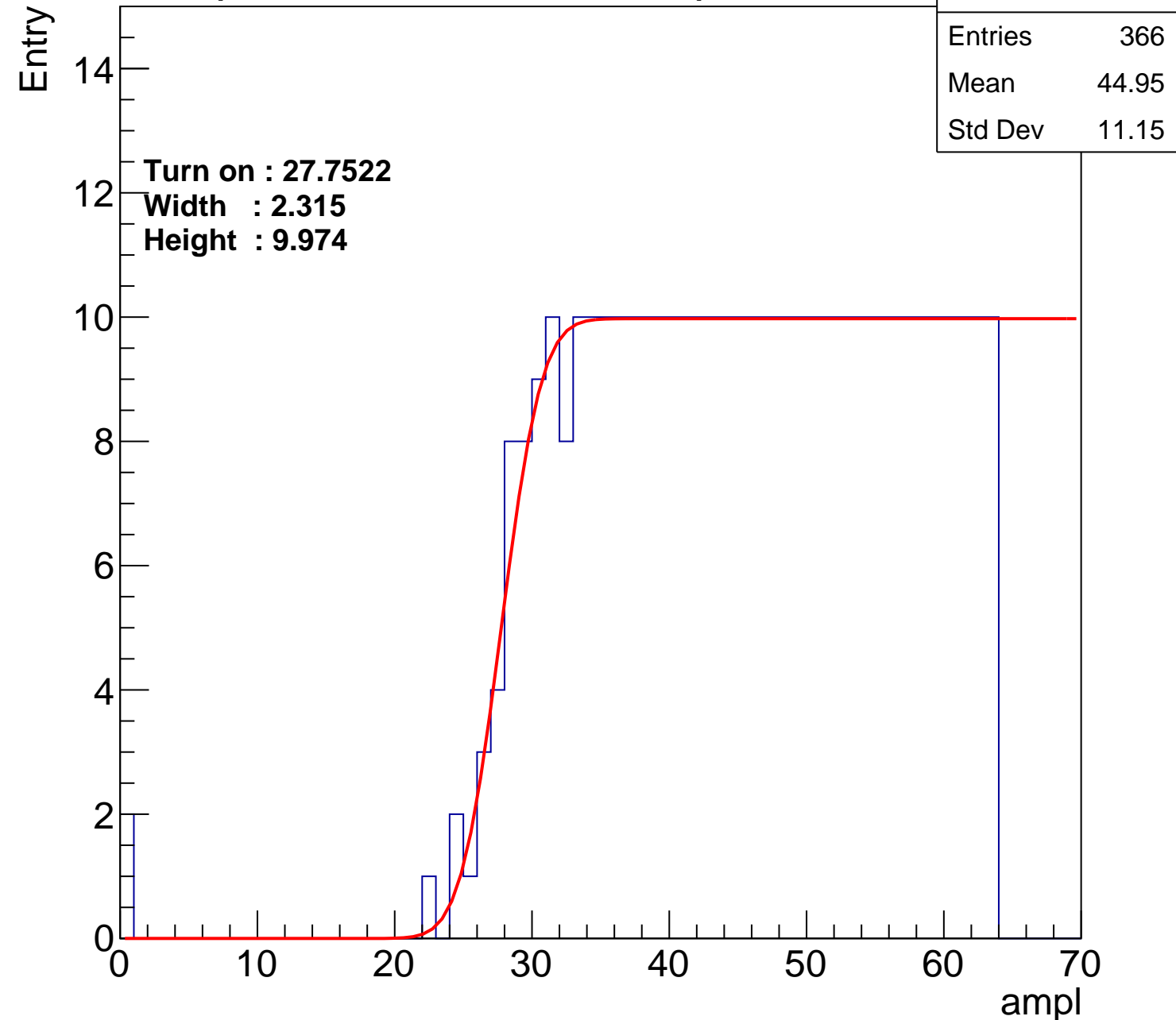
Width : 2.315

Height : 9.974

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch21

calib_packv5_042523_0143.root, FC#9, port A1

Entries	367
Mean	44.56
Std Dev	12.05

Turn on : 27.4552

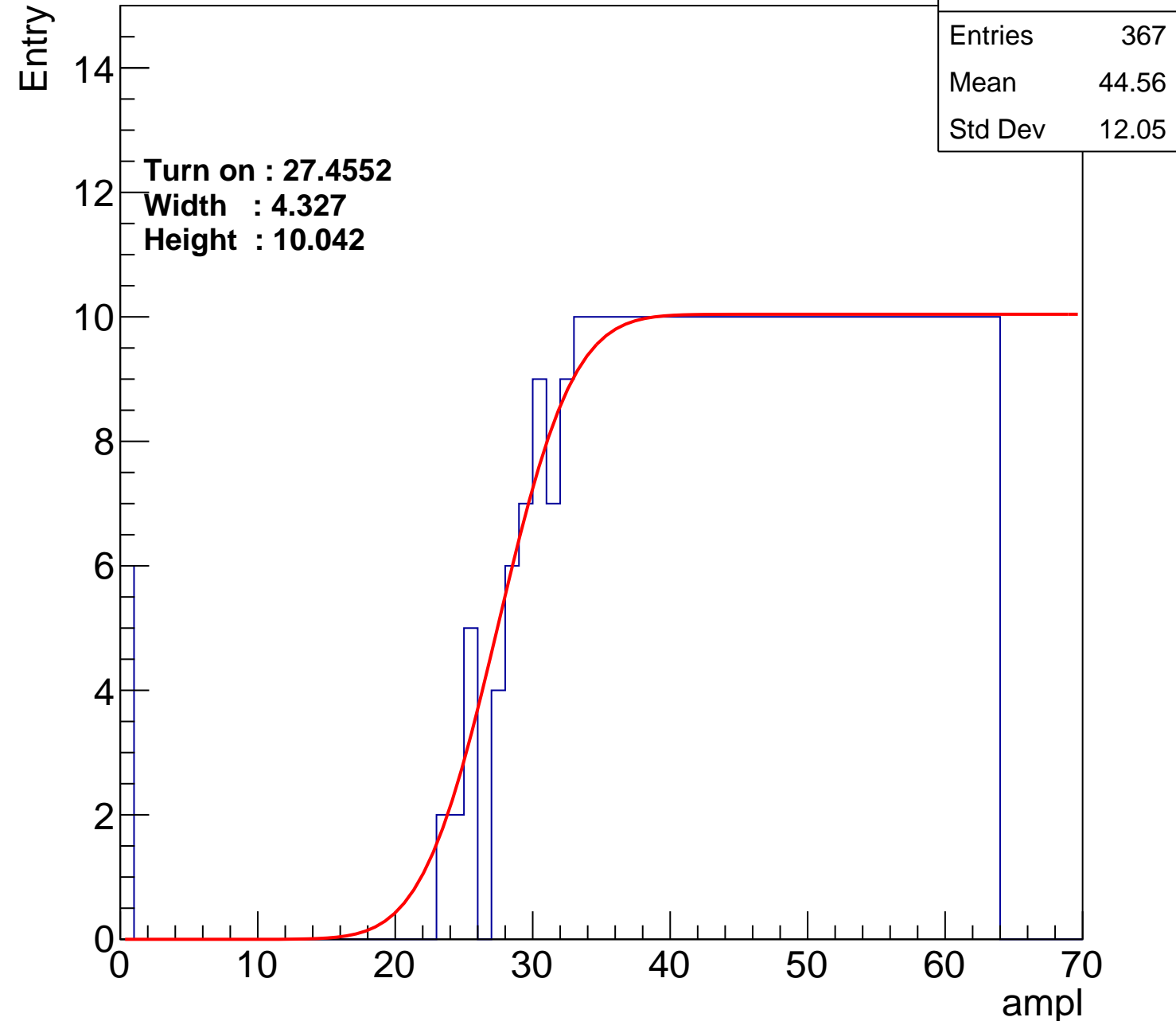
Width : 4.327

Height : 10.042

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch22

calib_packv5_042523_0143.root, FC#9, port A1

Entries	372
Mean	44.55
Std Dev	11.55

Turn on : 27.2221

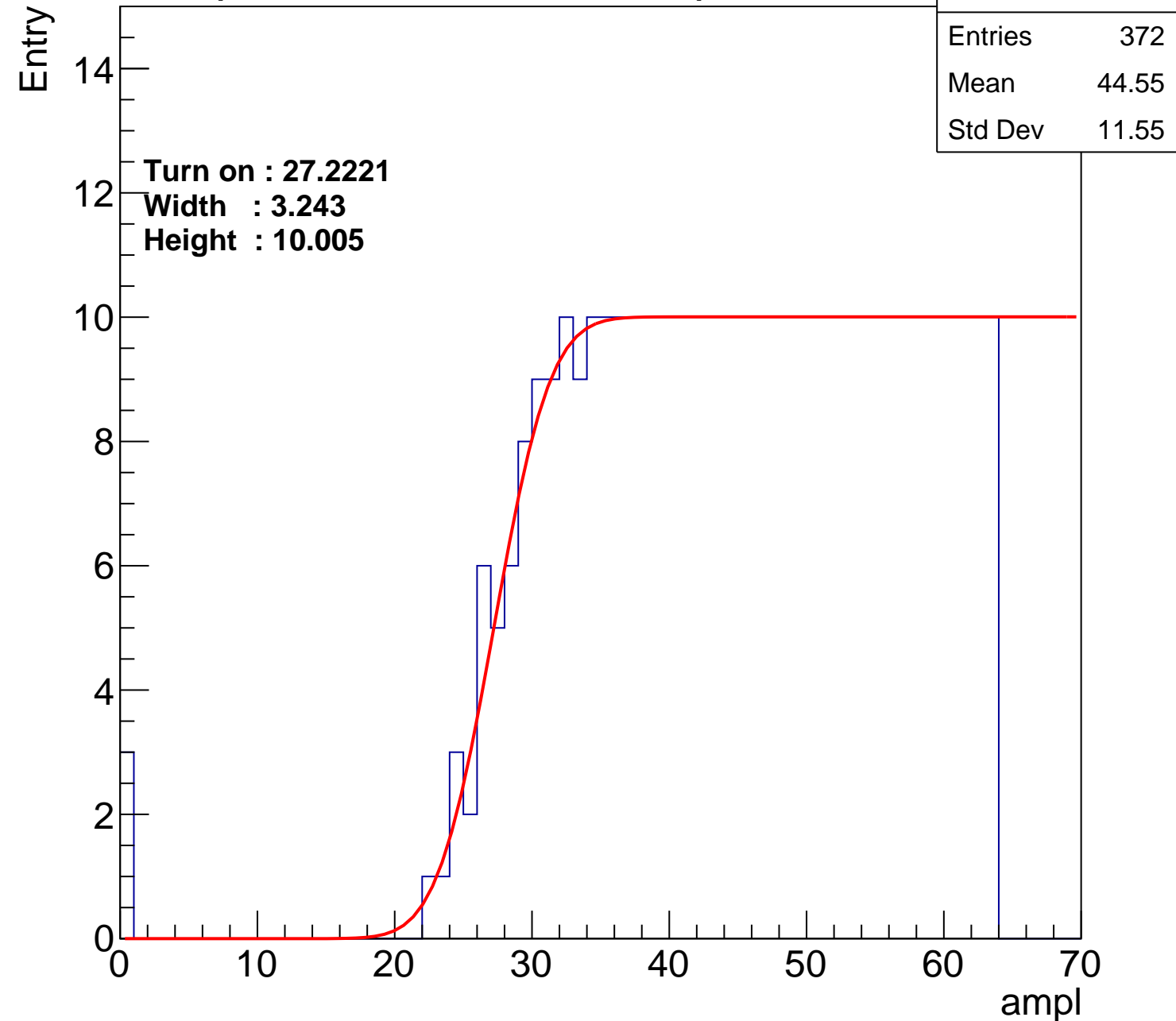
Width : 3.243

Height : 10.005

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch23

calib_packv5_042523_0143.root, FC#9, port A1

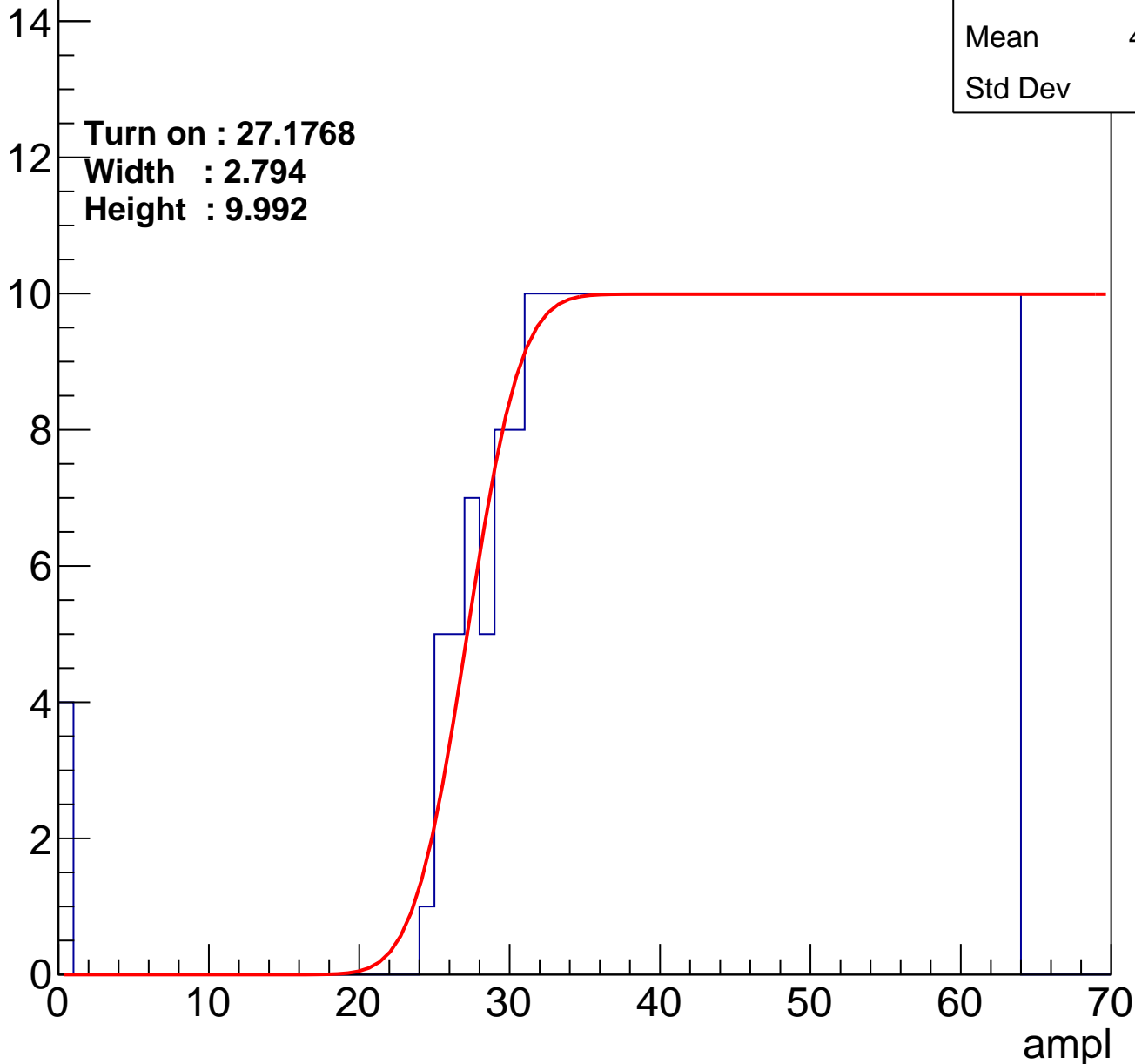
Entry

Entries	373
Mean	44.48
Std Dev	11.7

Turn on : 27.1768

Width : 2.794

Height : 9.992



B0L001S, U3-ch24

calib_packv5_042523_0143.root, FC#9, port A1

Entries	351
Mean	45.73
Std Dev	10.62

Turn on : 29.2130

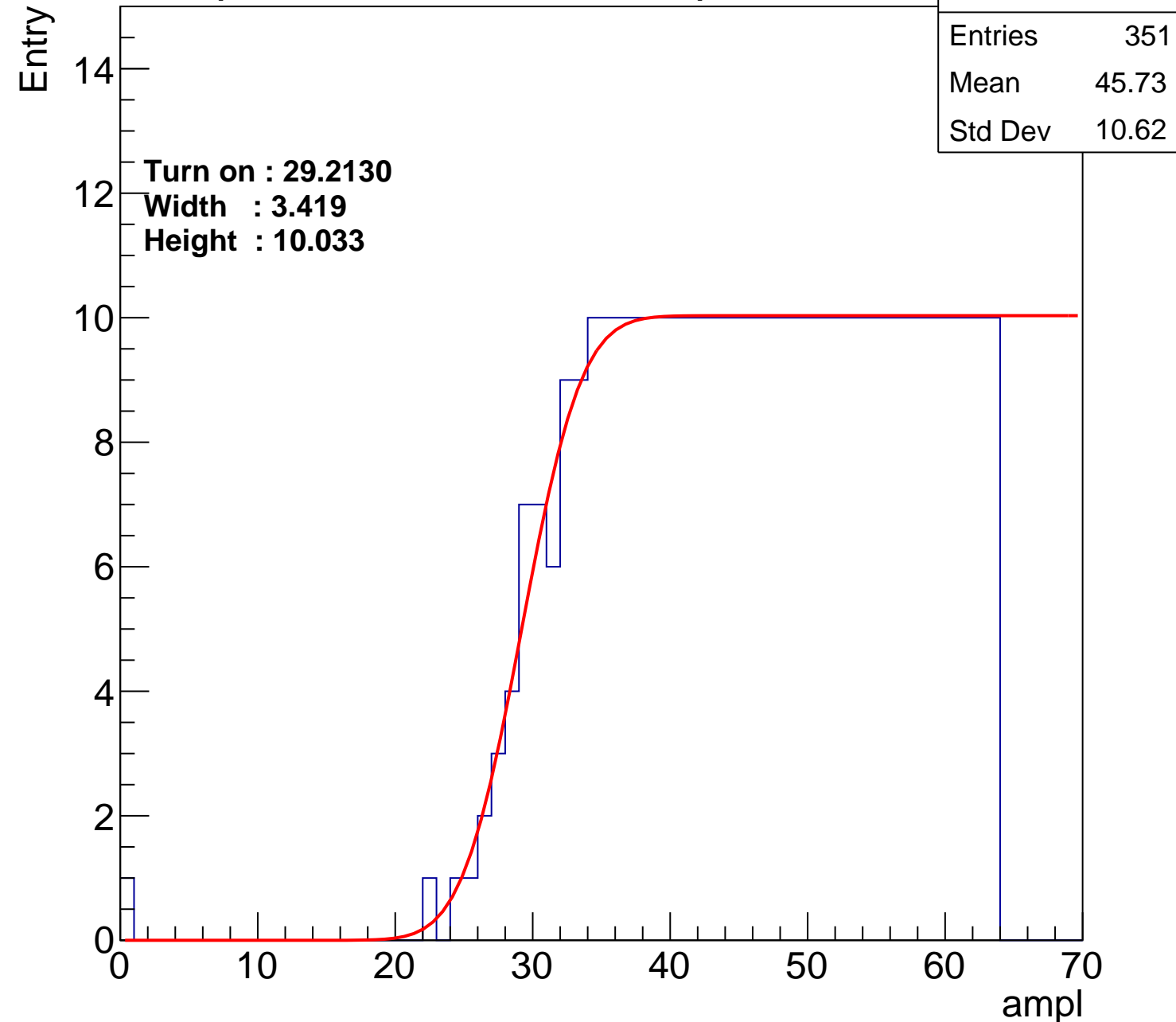
Width : 3.419

Height : 10.033

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch25

calib_packv5_042523_0143.root, FC#9, port A1

Entries	361
Mean	45.13
Std Dev	11.23

Turn on : 28.3958

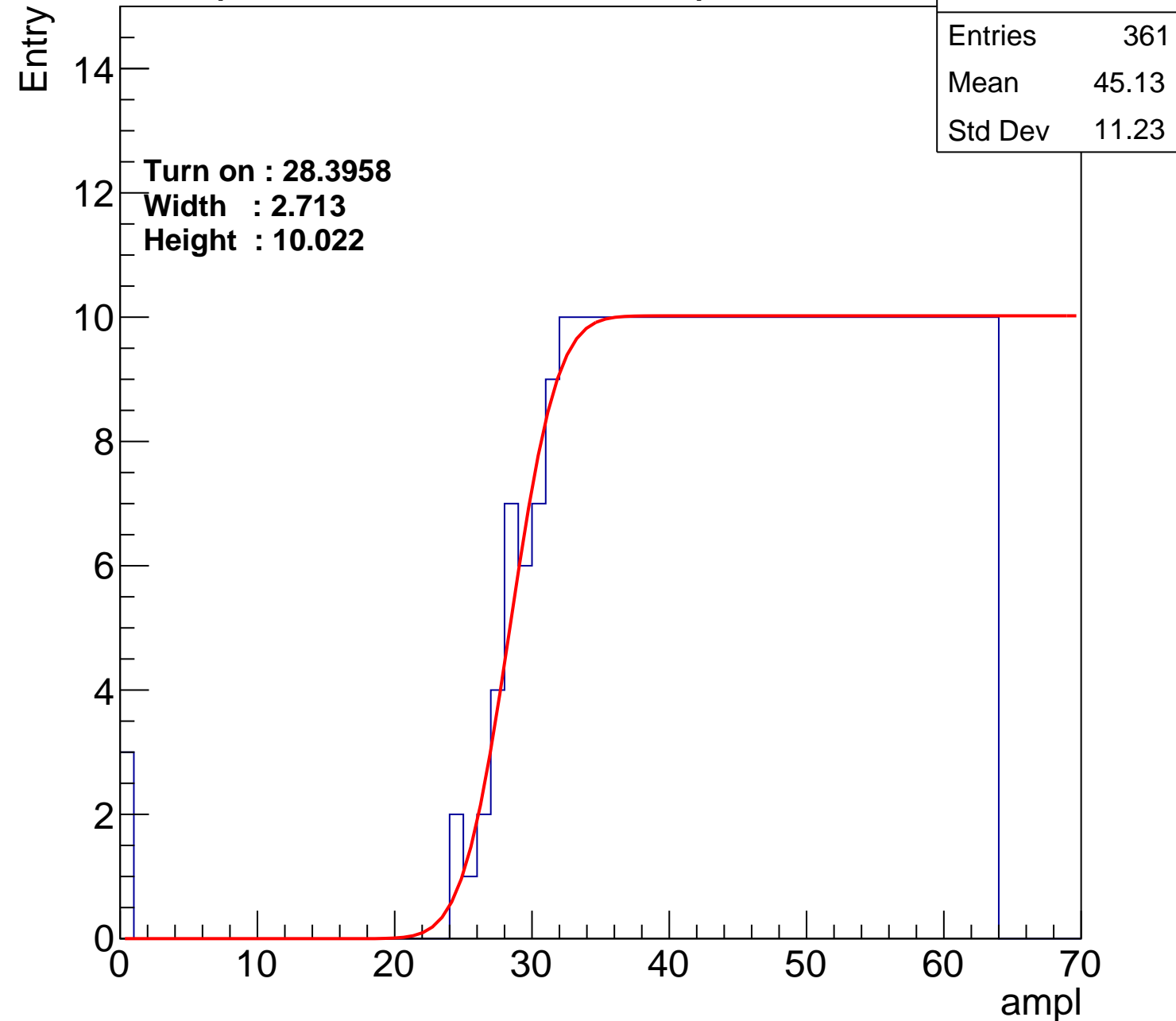
Width : 2.713

Height : 10.022

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch26

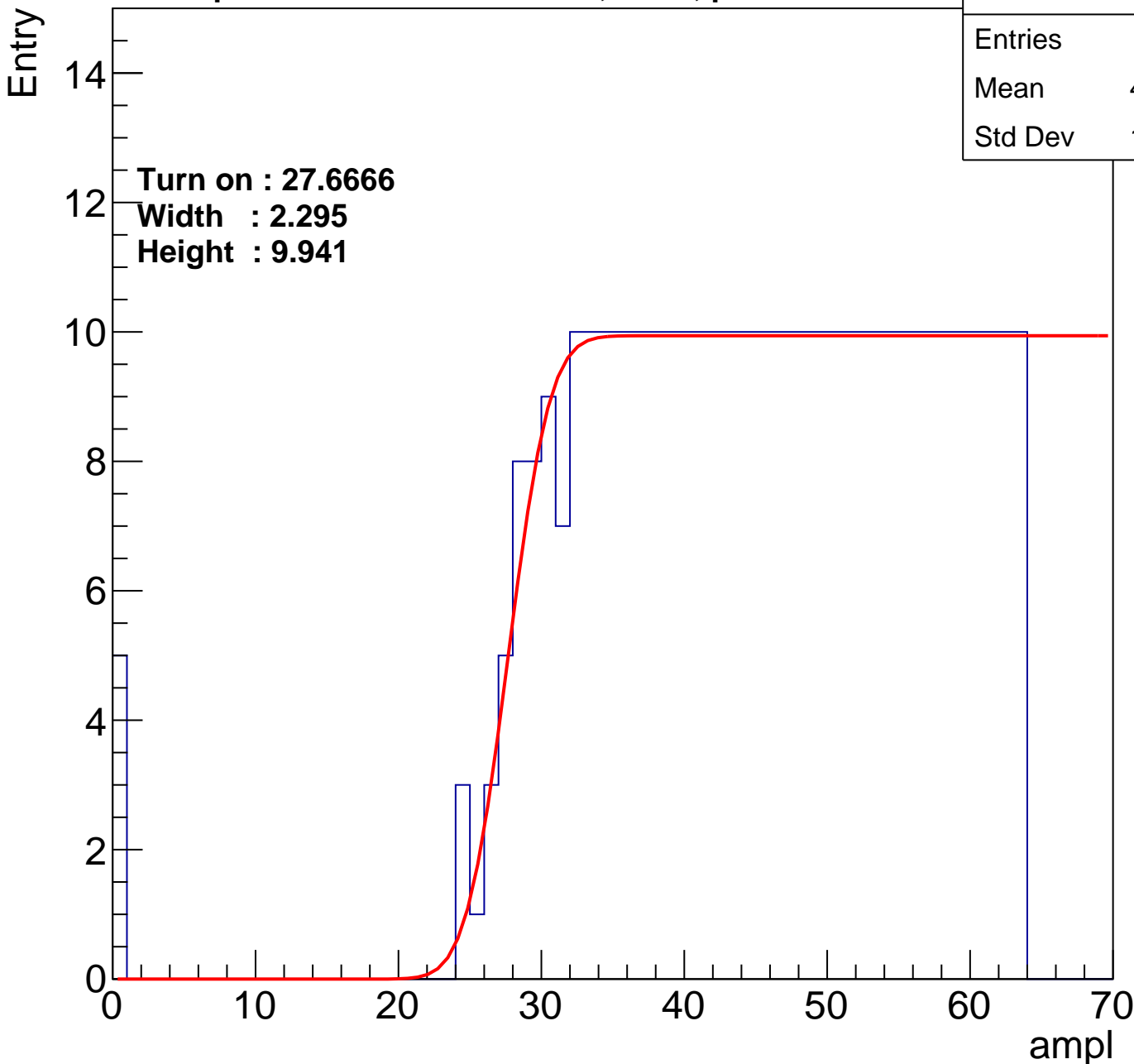
calib_packv5_042523_0143.root, FC#9, port A1

Entries	369
Mean	44.59
Std Dev	11.82

Turn on : 27.6666

Width : 2.295

Height : 9.941



B0L001S, U3-ch27

calib_packv5_042523_0143.root, FC#9, port A1

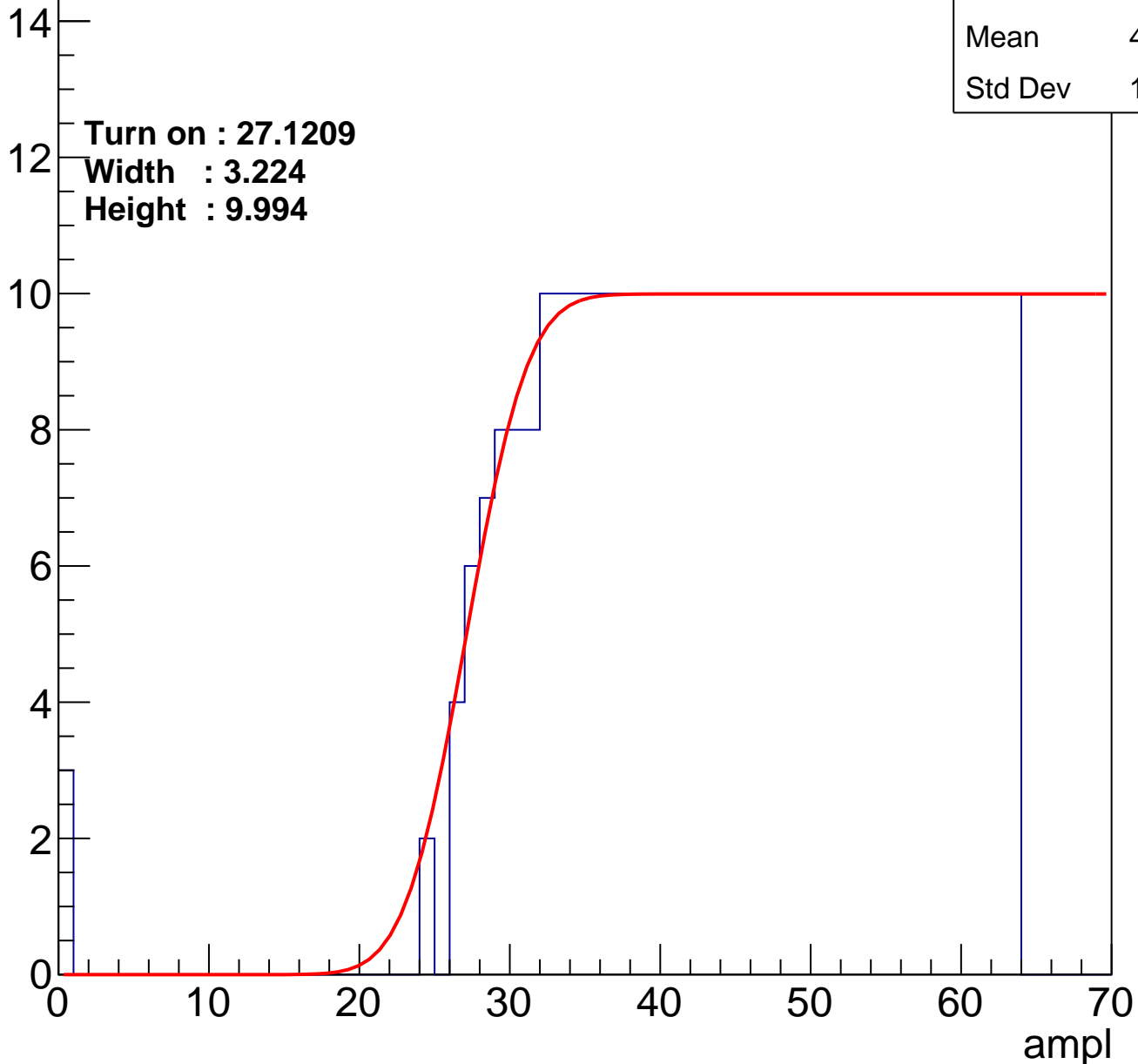
Entry

Entries	366
Mean	44.89
Std Dev	11.34

Turn on : 27.1209

Width : 3.224

Height : 9.994



B0L001S, U3-ch28

calib_packv5_042523_0143.root, FC#9, port A1

Entries	373
Mean	44.55
Std Dev	11.5

Turn on : 27.3754

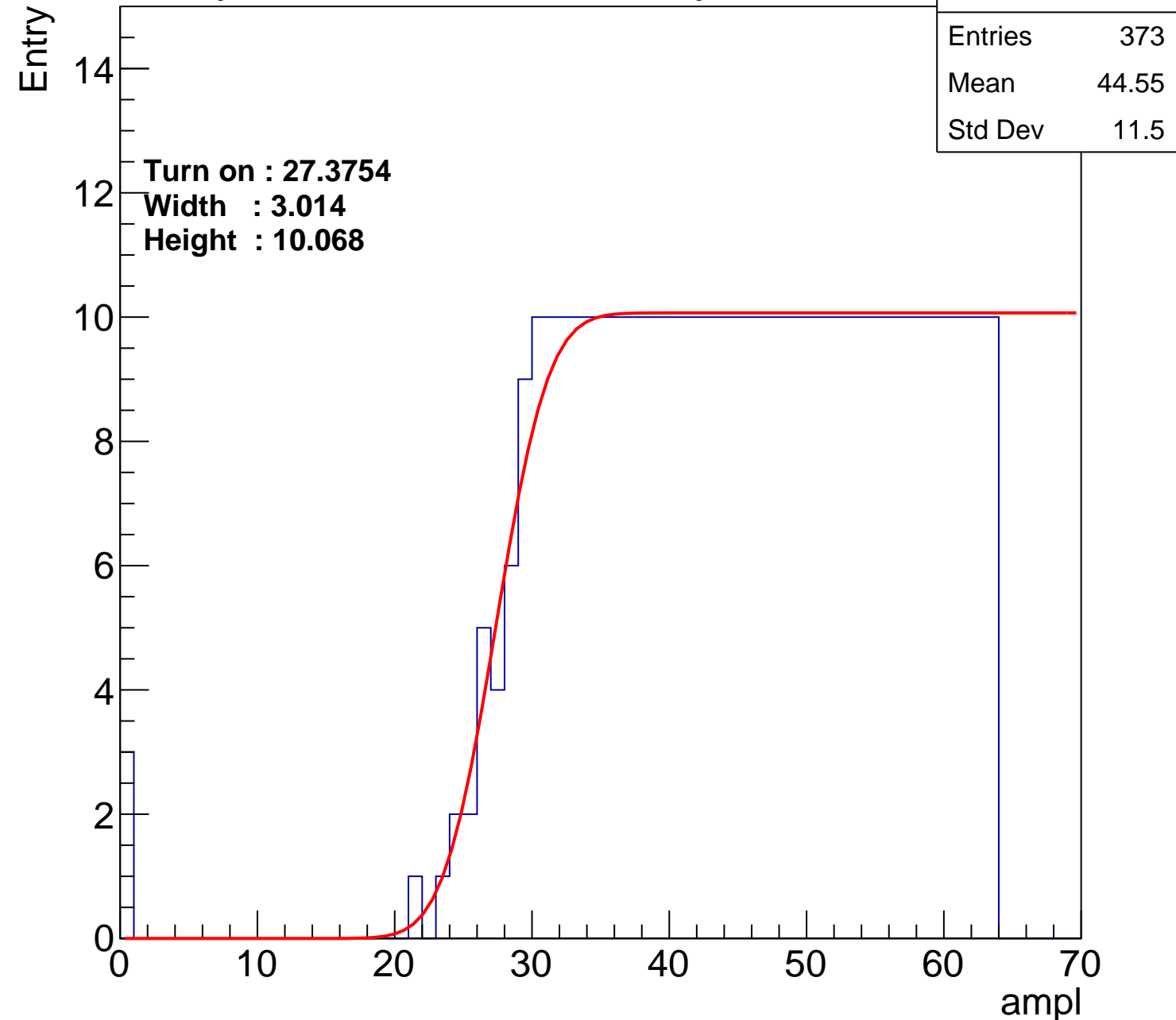
Width : 3.014

Height : 10.068

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch29

calib_packv5_042523_0143.root, FC#9, port A1

Entries	366
Mean	44.93
Std Dev	11.19

Turn on : 27.7847

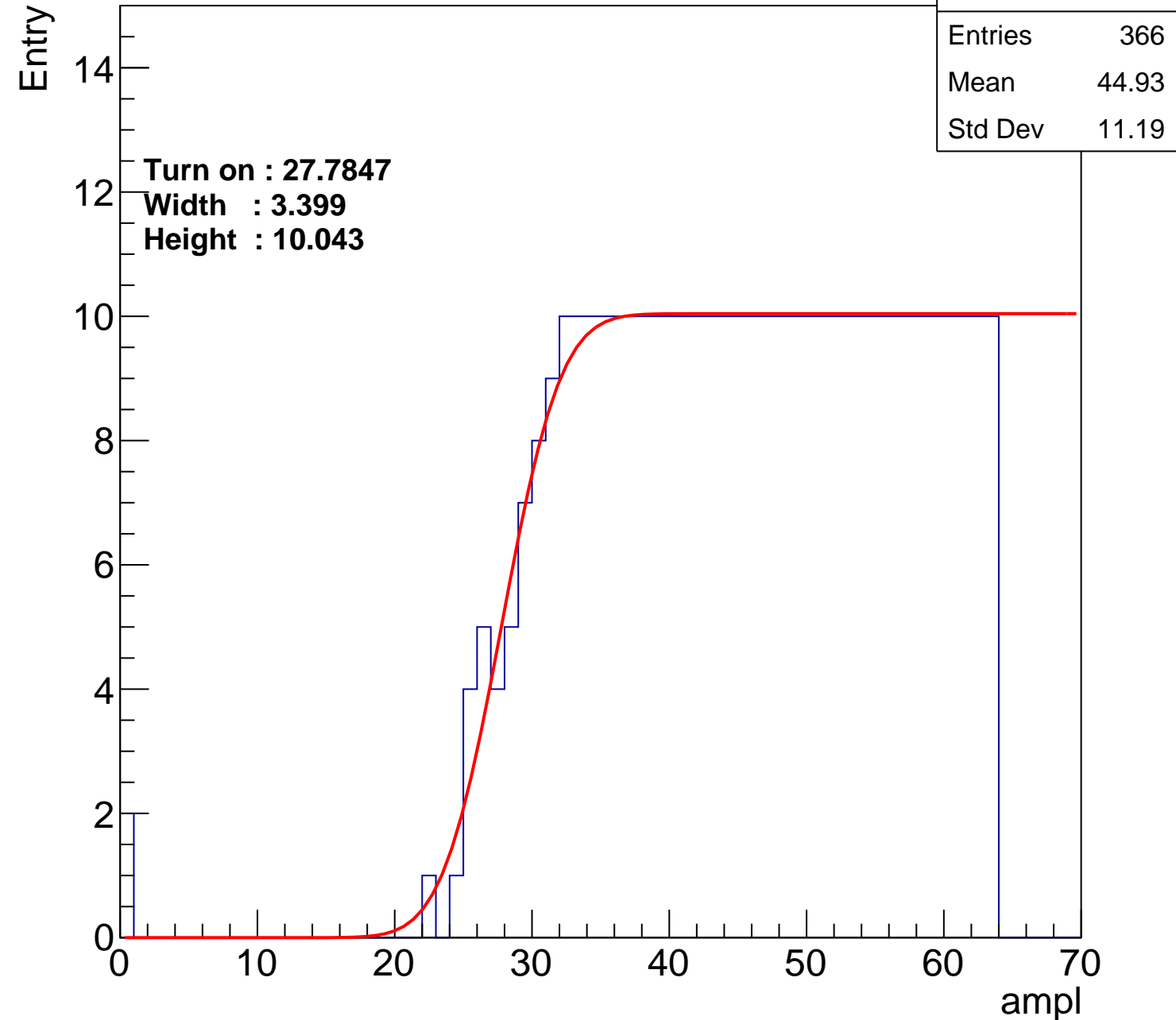
Width : 3.399

Height : 10.043

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch30

calib_packv5_042523_0143.root, FC#9, port A1

Entries	373
Mean	44.26
Std Dev	12.26

Turn on : 28.1826

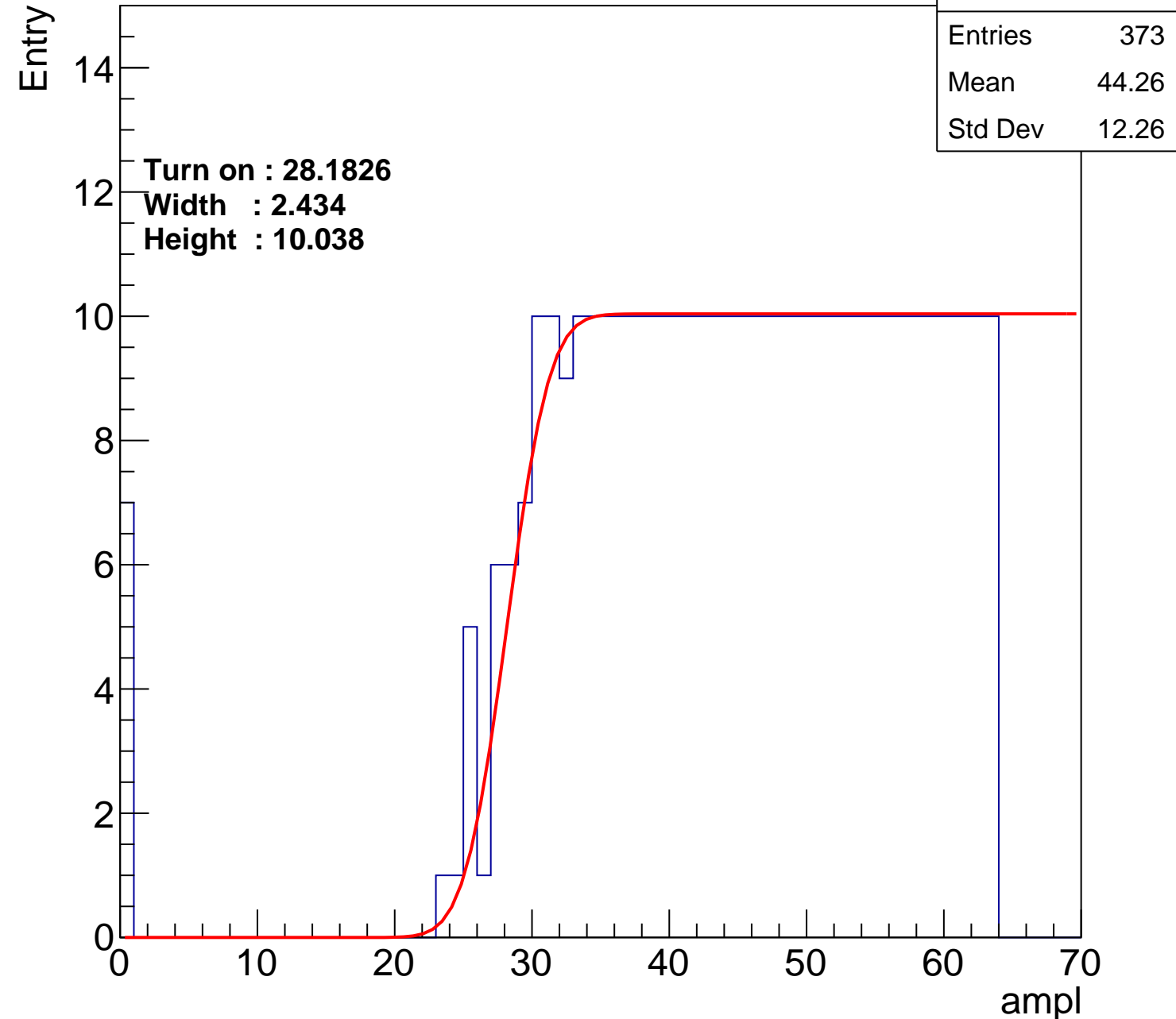
Width : 2.434

Height : 10.038

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch31

calib_packv5_042523_0143.root, FC#9, port A1

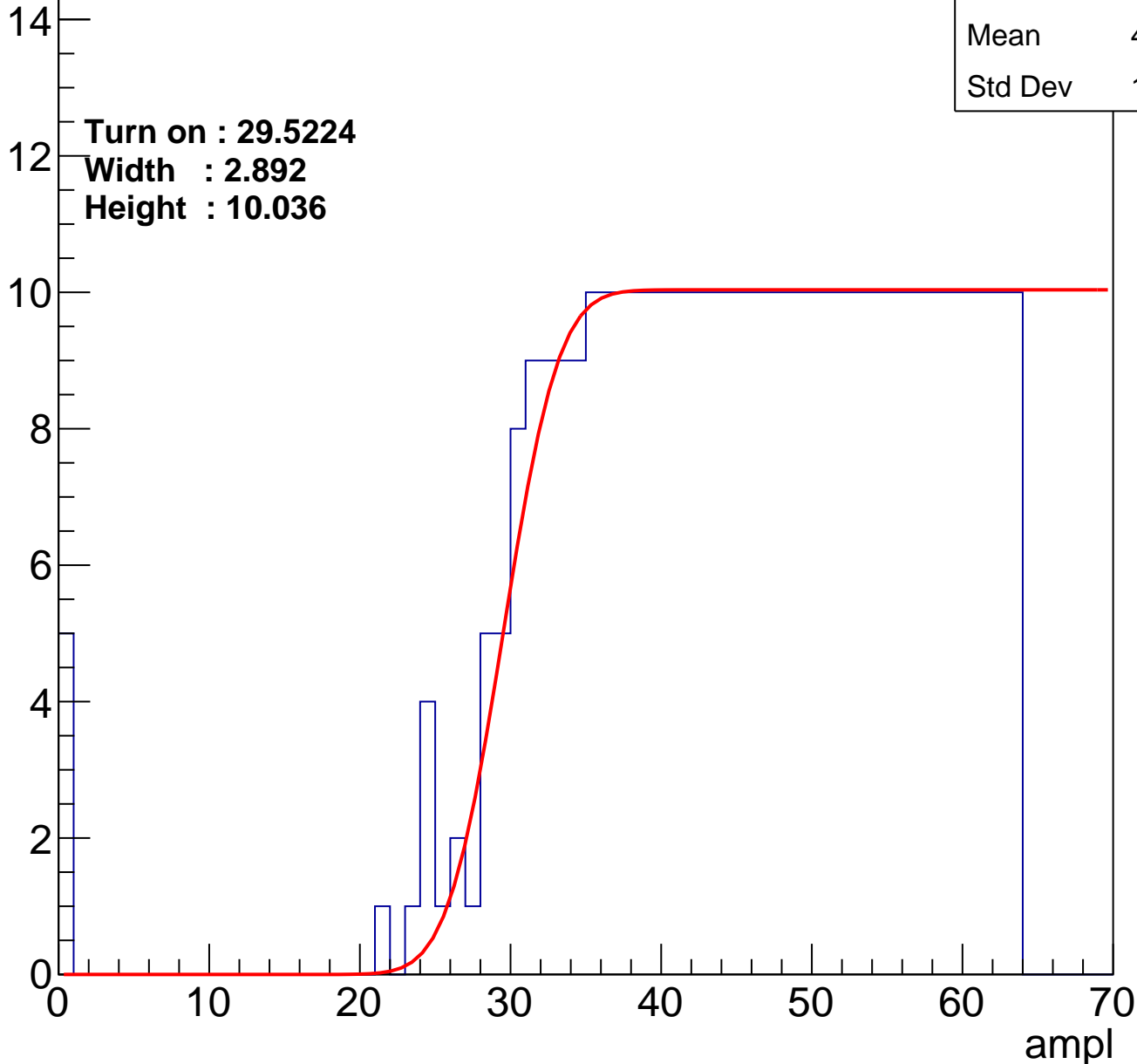
Entries	359
Mean	44.98
Std Dev	11.75

Turn on : 29.5224

Width : 2.892

Height : 10.036

Entry



B0L001S, U3-ch32

calib_packv5_042523_0143.root, FC#9, port A1

Entries	368
Mean	44.72
Std Dev	11.58

Turn on : 27.5490

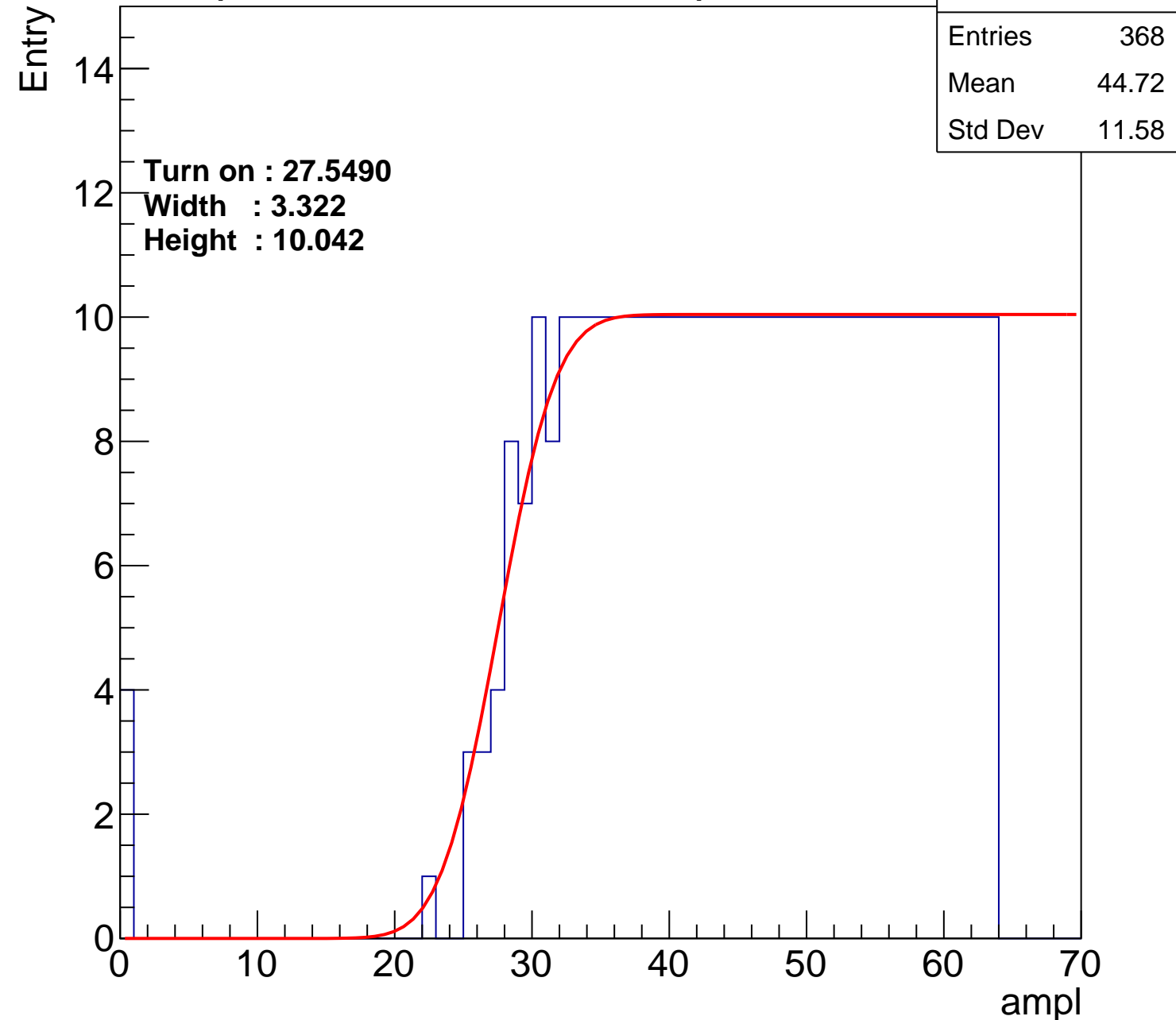
Width : 3.322

Height : 10.042

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch33

calib_packv5_042523_0143.root, FC#9, port A1

Entries	357
Mean	45.23
Std Dev	11.39

Turn on : 29.0418

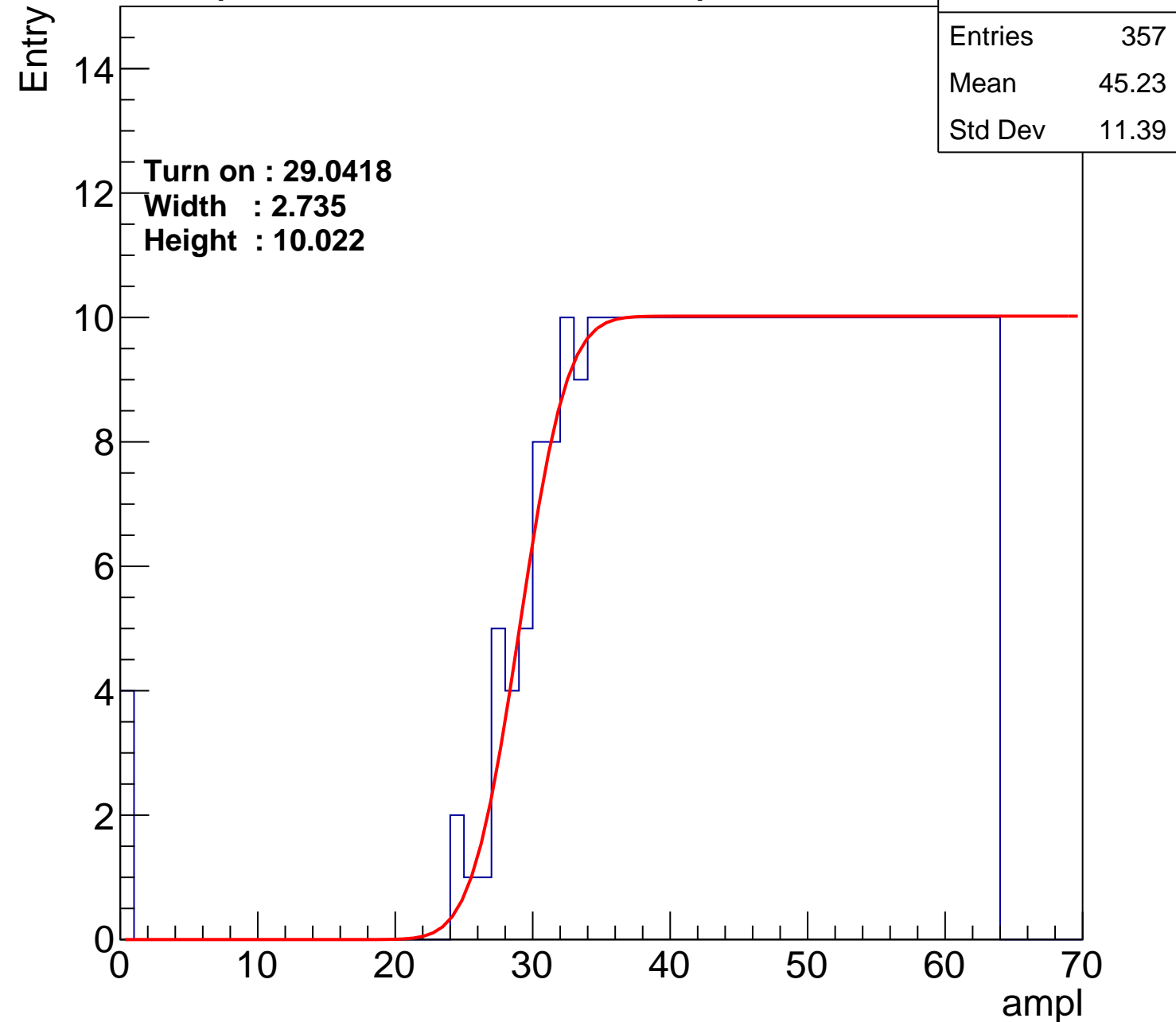
Width : 2.735

Height : 10.022

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch34

calib_packv5_042523_0143.root, FC#9, port A1

Entries	374
Mean	44.59
Std Dev	11.21

Turn on : 27.6490

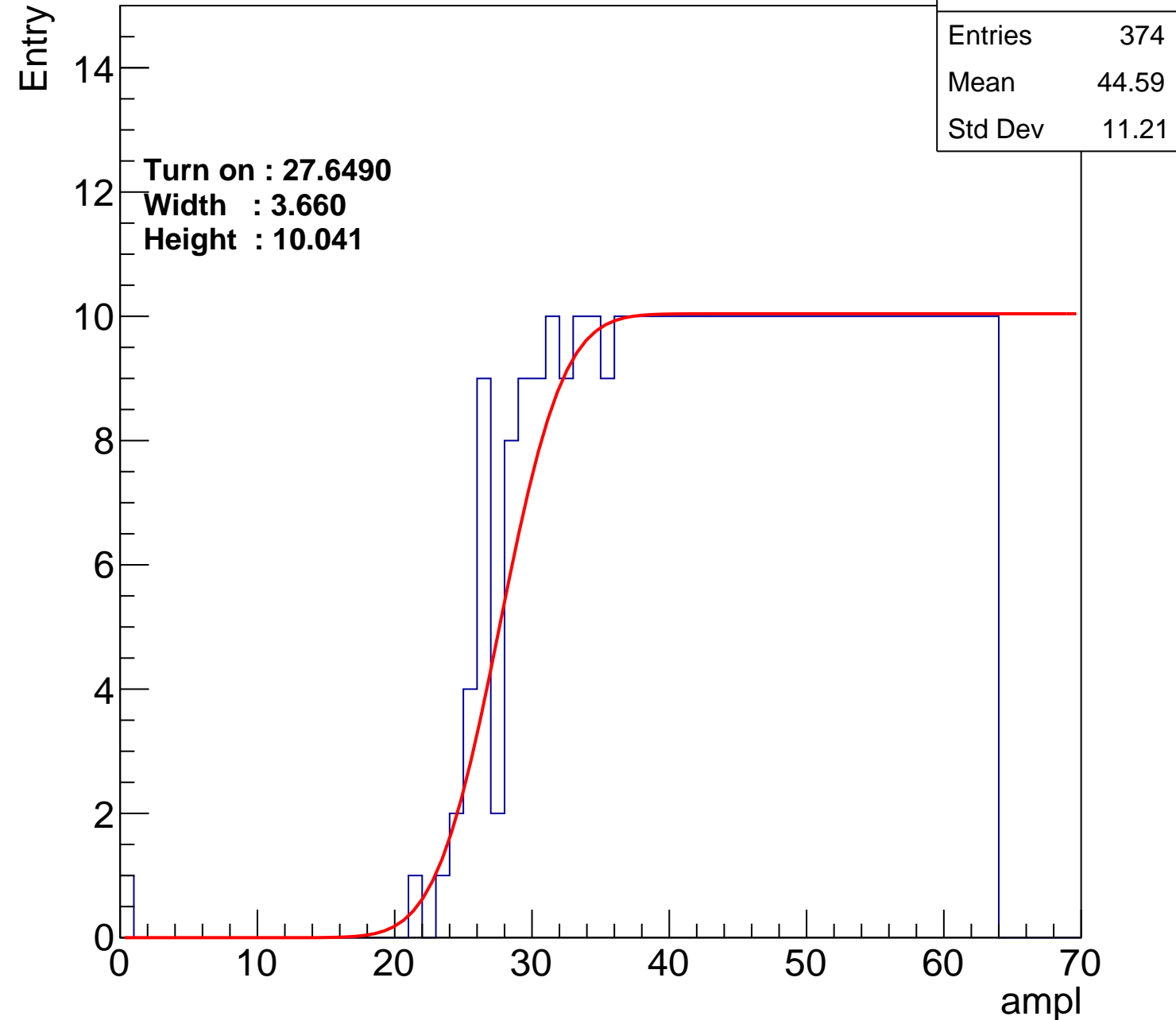
Width : 3.660

Height : 10.041

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch35

calib_packv5_042523_0143.root, FC#9, port A1

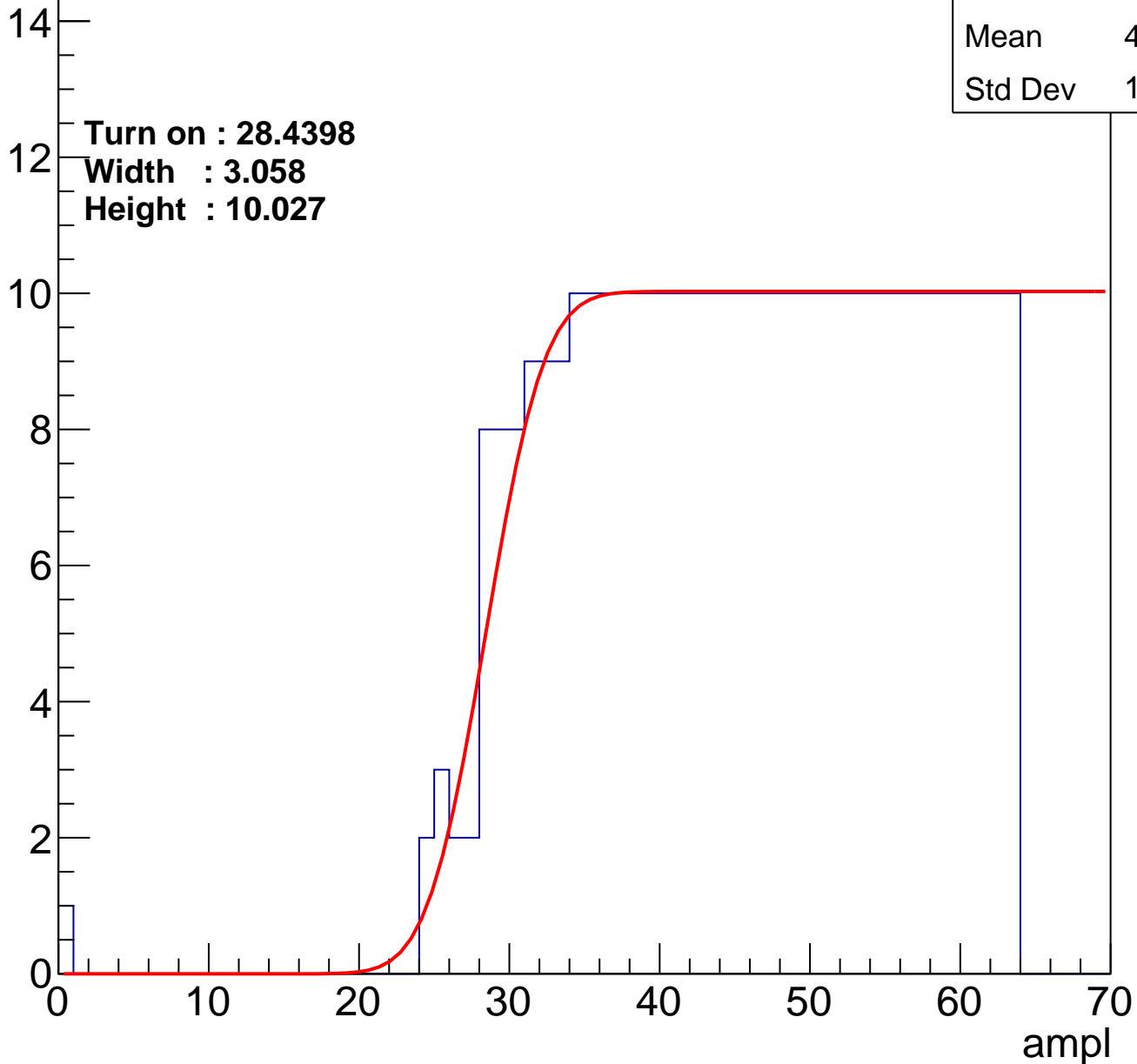
Entries	361
Mean	45.26
Std Dev	10.83

Turn on : 28.4398

Width : 3.058

Height : 10.027

Entry



B0L001S, U3-ch36

calib_packv5_042523_0143.root, FC#9, port A1

Entries	351
Mean	45.42
Std Dev	11.39

Turn on : 29.1309

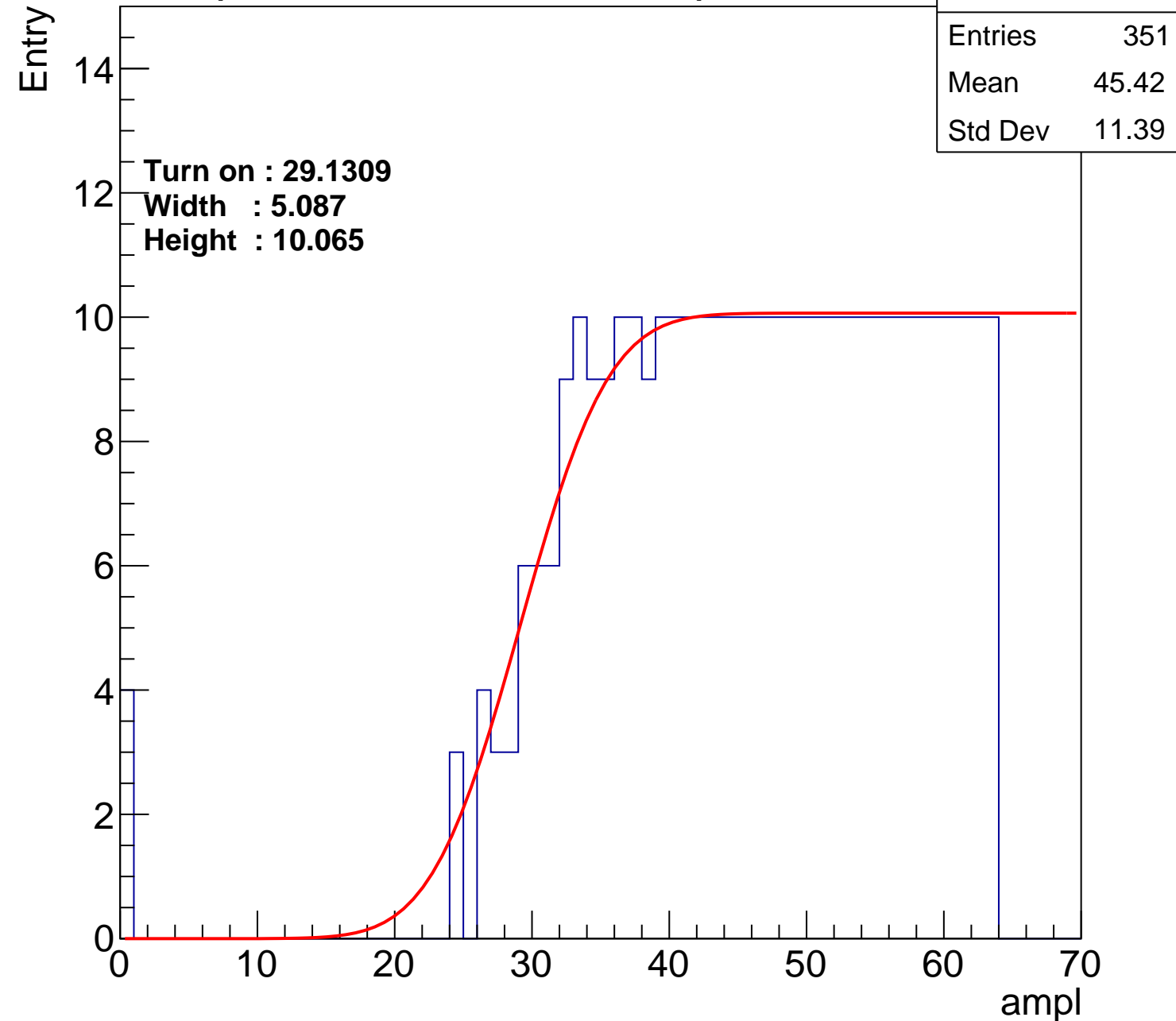
Width : 5.087

Height : 10.065

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch37

calib_packv5_042523_0143.root, FC#9, port A1

Entries	368
Mean	44.86
Std Dev	11.09

Turn on : 26.6902

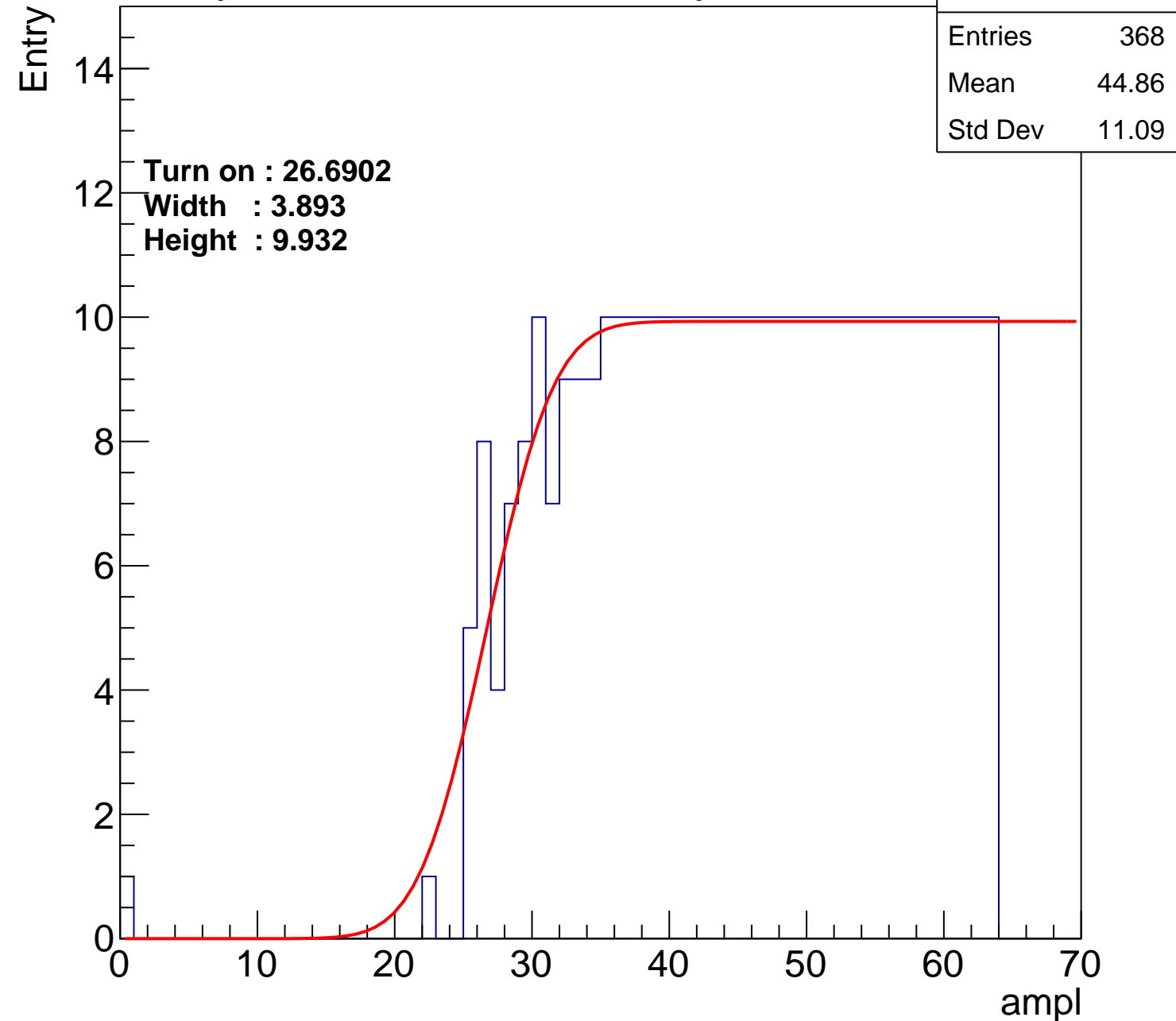
Width : 3.893

Height : 9.932

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch38

calib_packv5_042523_0143.root, FC#9, port A1

Entry

14

12

10

8

6

4

2

0

0

10

20

30

40

50

60

ampl

Turn on : 27.6276

Width : 2.235

Height : 9.937

Entries	369
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Mean	44.6
------	------

Std Dev	11.8
---------	------

B0L001S, U3-ch39

calib_packv5_042523_0143.root, FC#9, port A1

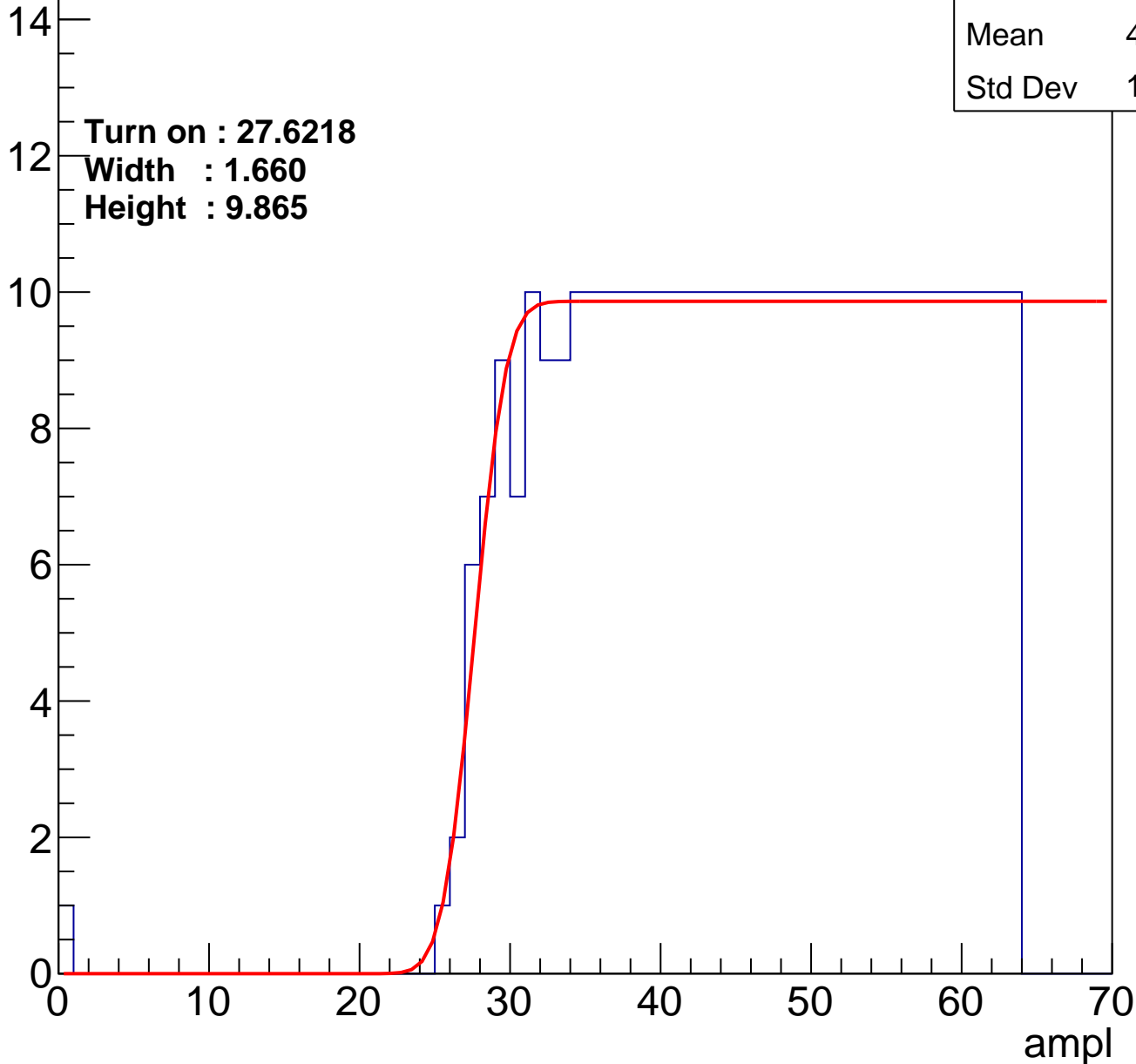
Entry

Entries	361
Mean	45.29
Std Dev	10.77

Turn on : 27.6218

Width : 1.660

Height : 9.865



B0L001S, U3-ch40

calib_packv5_042523_0143.root, FC#9, port A1

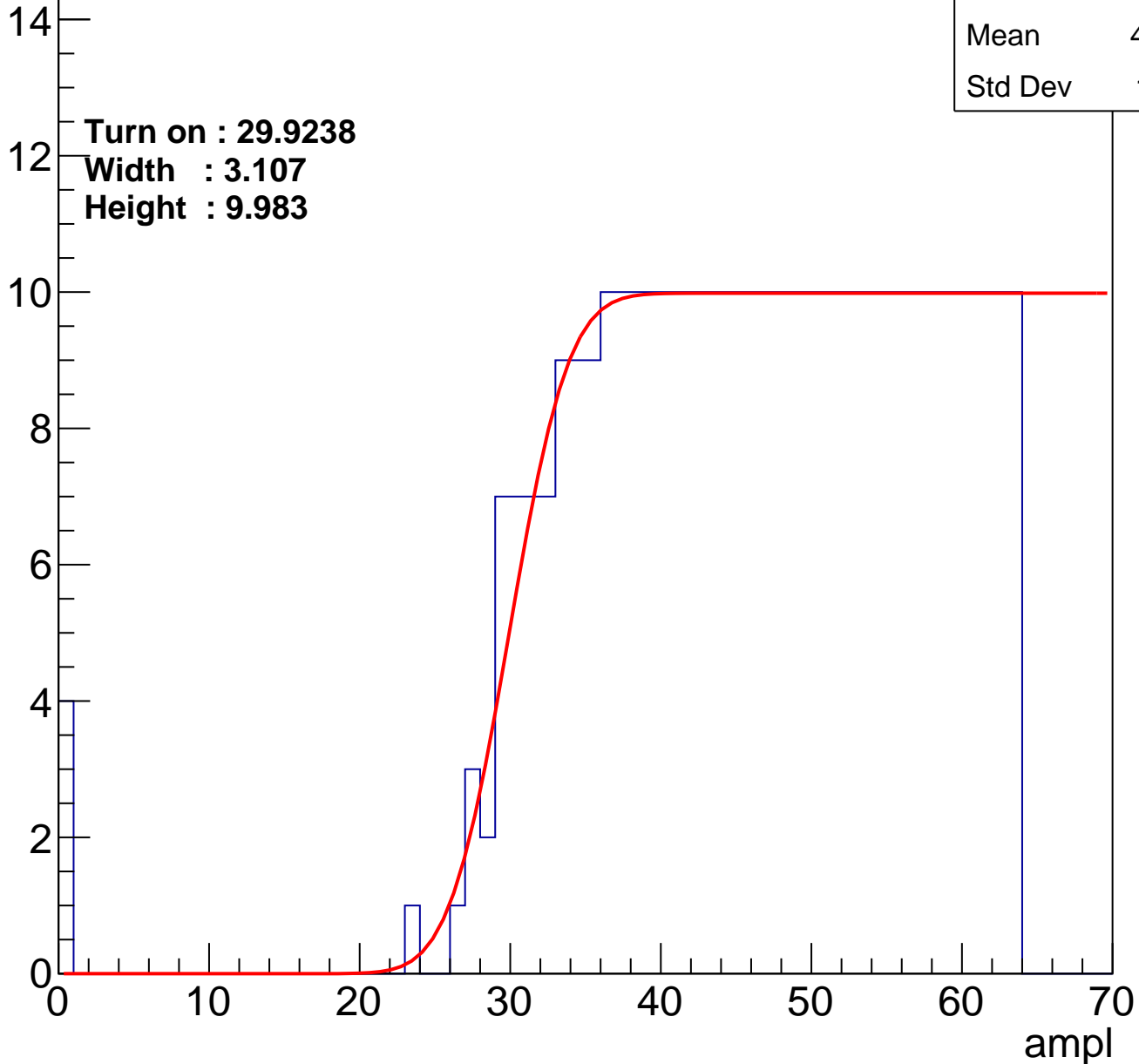
Entries	346
Mean	45.72
Std Dev	11.21

Turn on : 29.9238

Width : 3.107

Height : 9.983

Entry



B0L001S, U3-ch41

calib_packv5_042523_0143.root, FC#9, port A1

Entries	367
Mean	44.99
Std Dev	10.96

Turn on : 28.0224

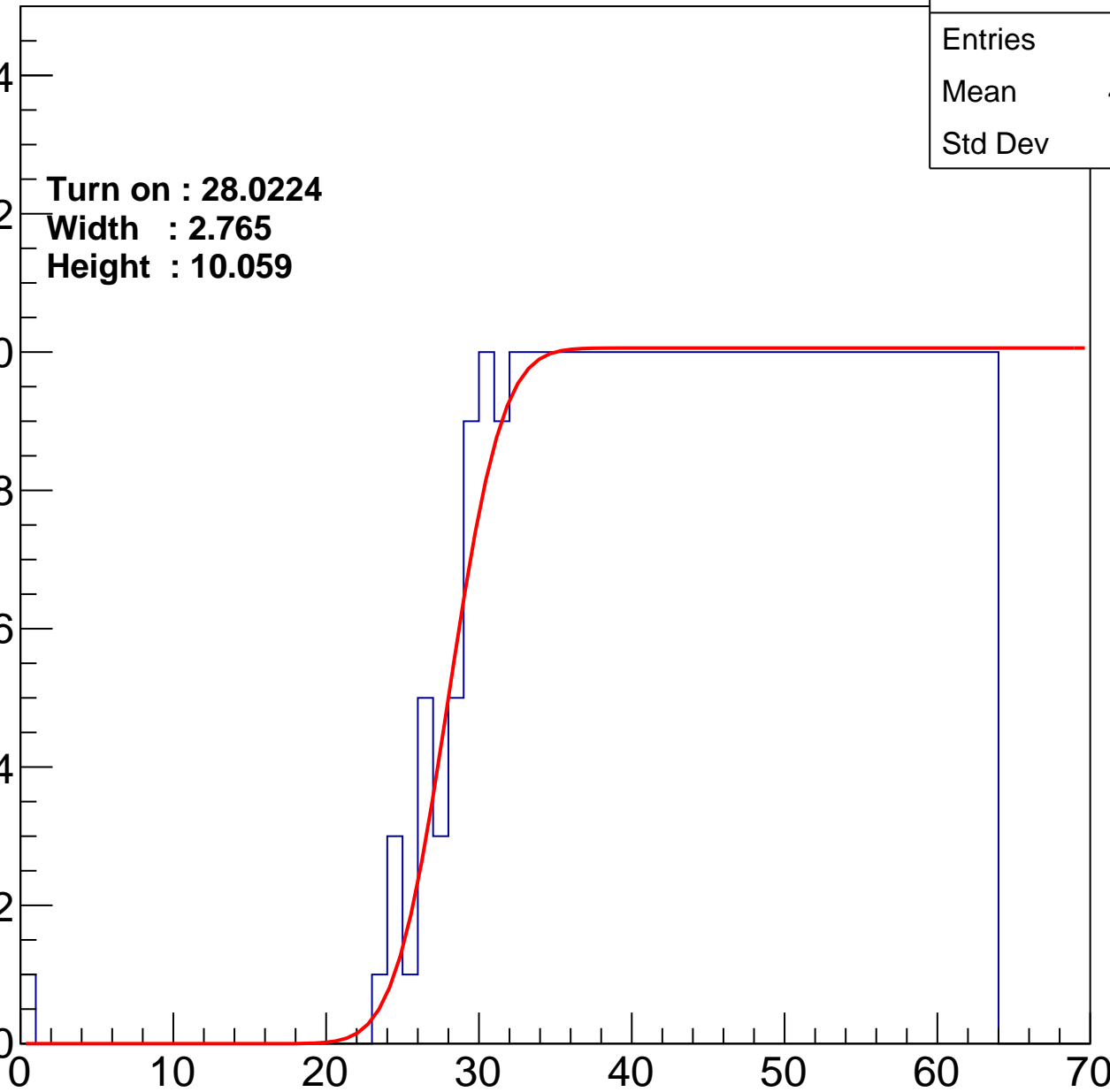
Width : 2.765

Height : 10.059

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch42

calib_packv5_042523_0143.root, FC#9, port A1

Entries	364
Mean	44.99
Std Dev	11.2

Turn on : 27.3571

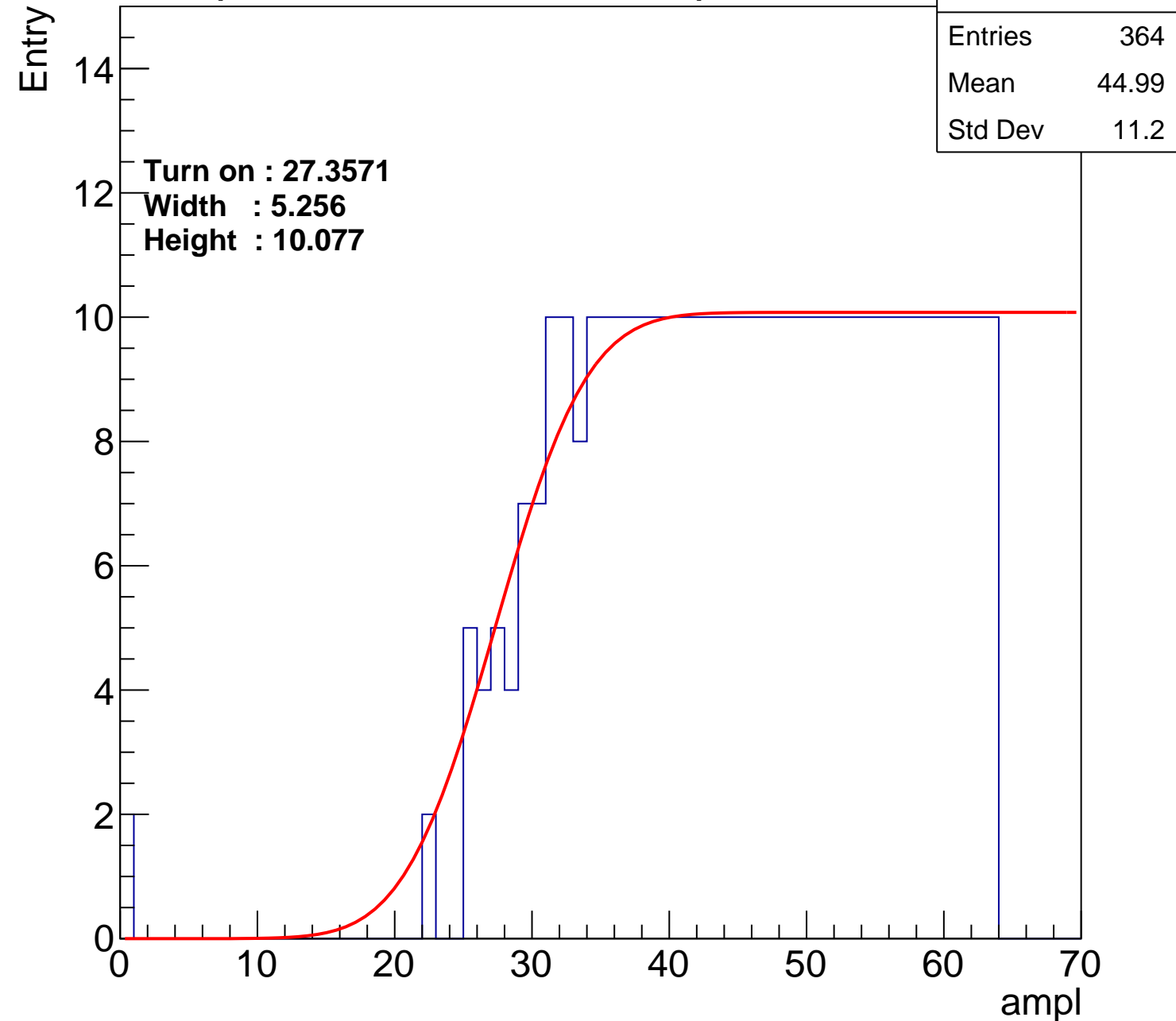
Width : 5.256

Height : 10.077

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch43

calib_packv5_042523_0143.root, FC#9, port A1

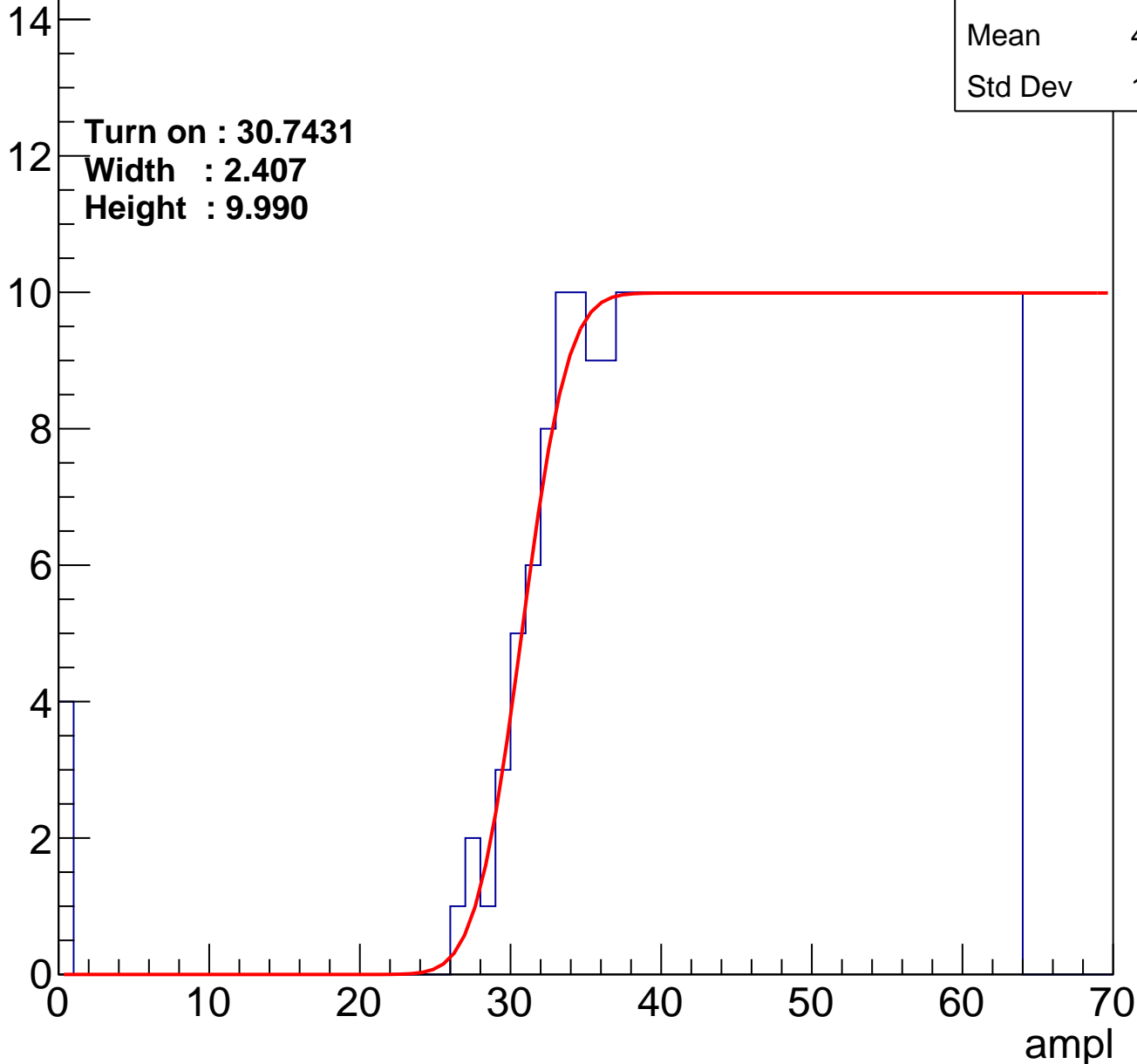
Entries	338
Mean	46.14
Std Dev	10.99

Turn on : 30.7431

Width : 2.407

Height : 9.990

Entry



B0L001S, U3-ch44

calib_packv5_042523_0143.root, FC#9, port A1

Entries	377
Mean	44.44
Std Dev	11.32

Turn on : 26.5934

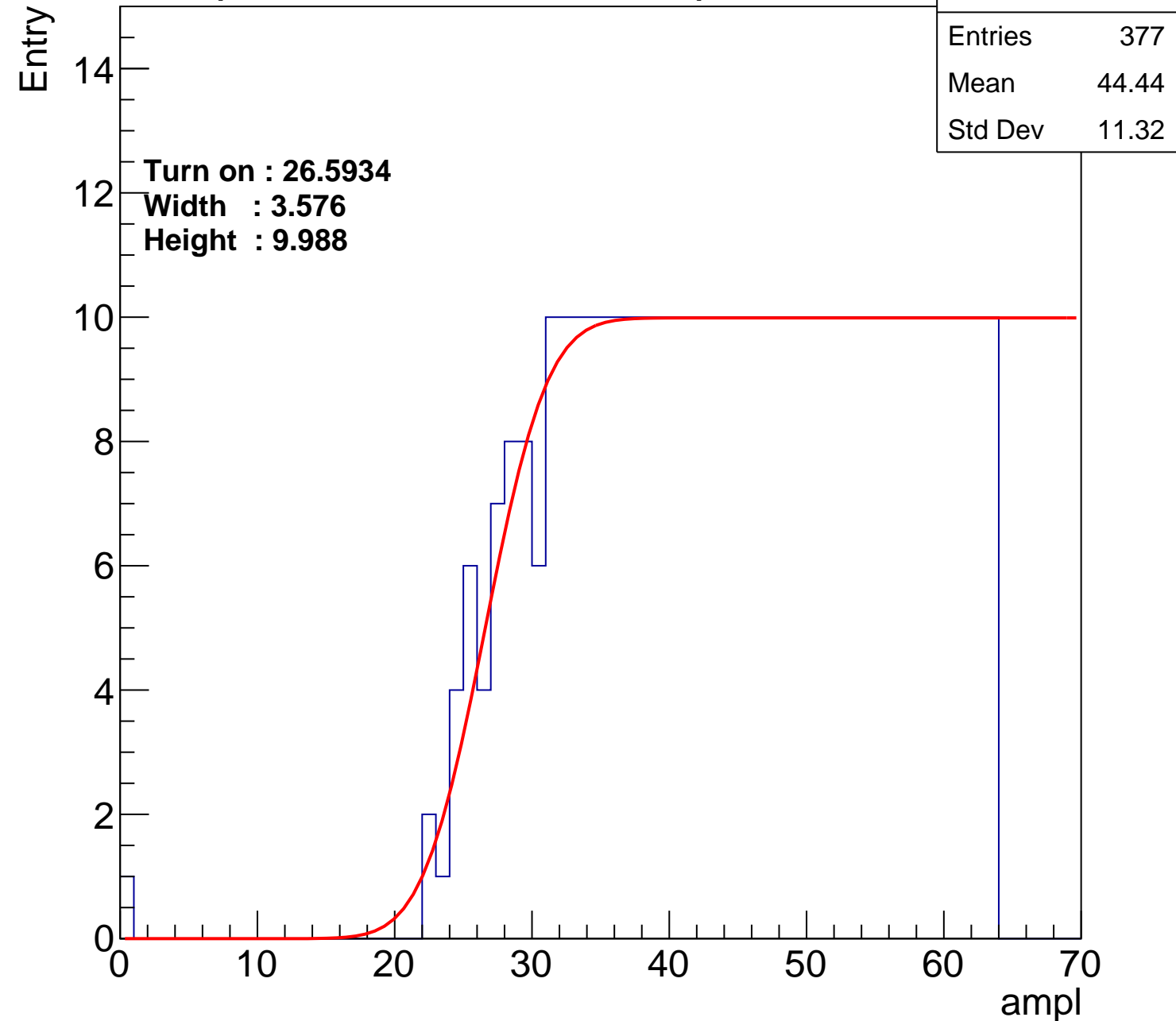
Width : 3.576

Height : 9.988

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch45

calib_packv5_042523_0143.root, FC#9, port A1

Entries	365
Mean	44.84
Std Dev	11.56

Turn on : 28.4317

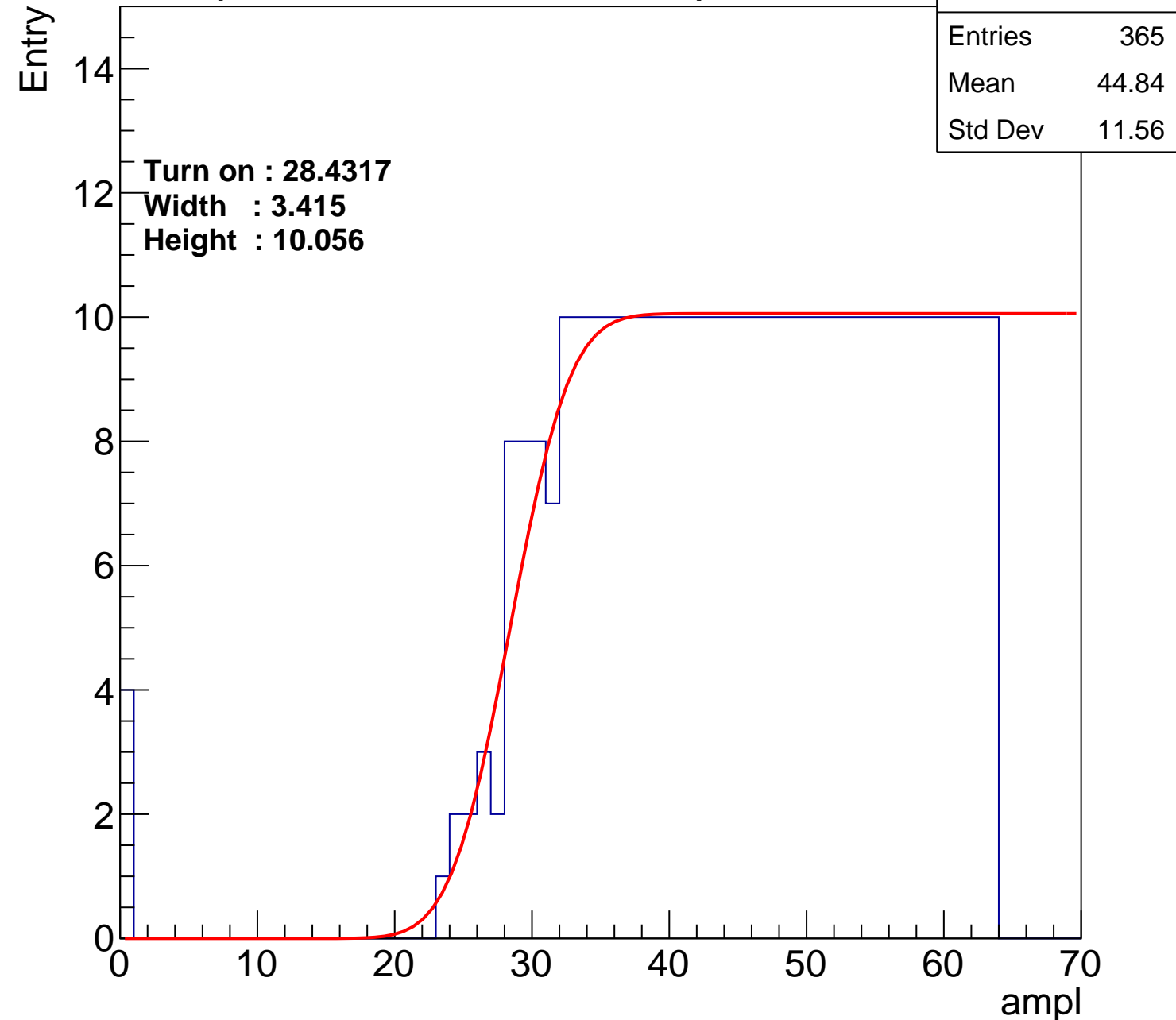
Width : 3.415

Height : 10.056

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch46

calib_packv5_042523_0143.root, FC#9, port A1

Entries	376
Mean	44.31
Std Dev	11.8

Turn on : 27.2835

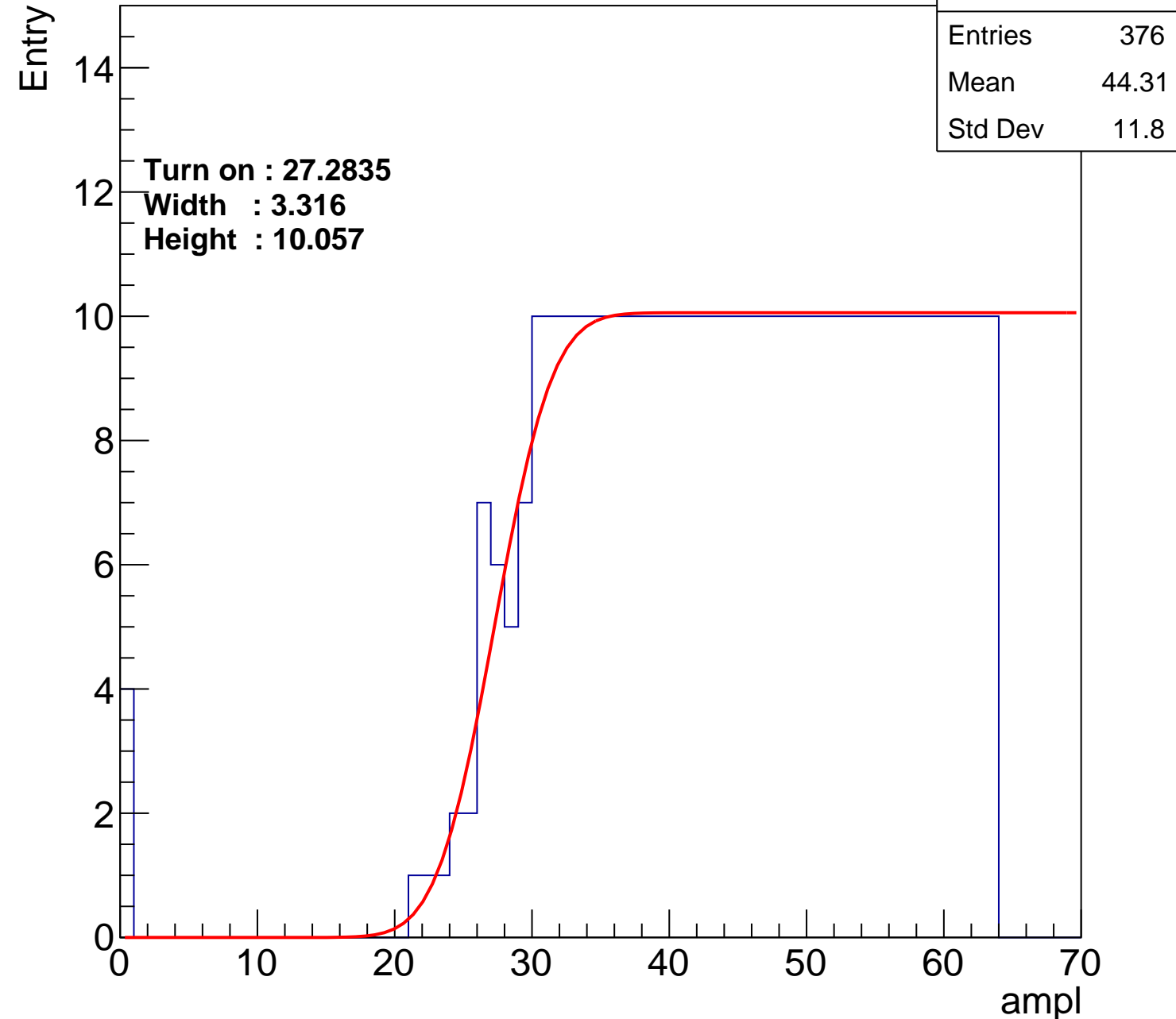
Width : 3.316

Height : 10.057

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch47

calib_packv5_042523_0143.root, FC#9, port A1

Entries	363
Mean	45.03
Std Dev	11.28

Turn on : 27.4973

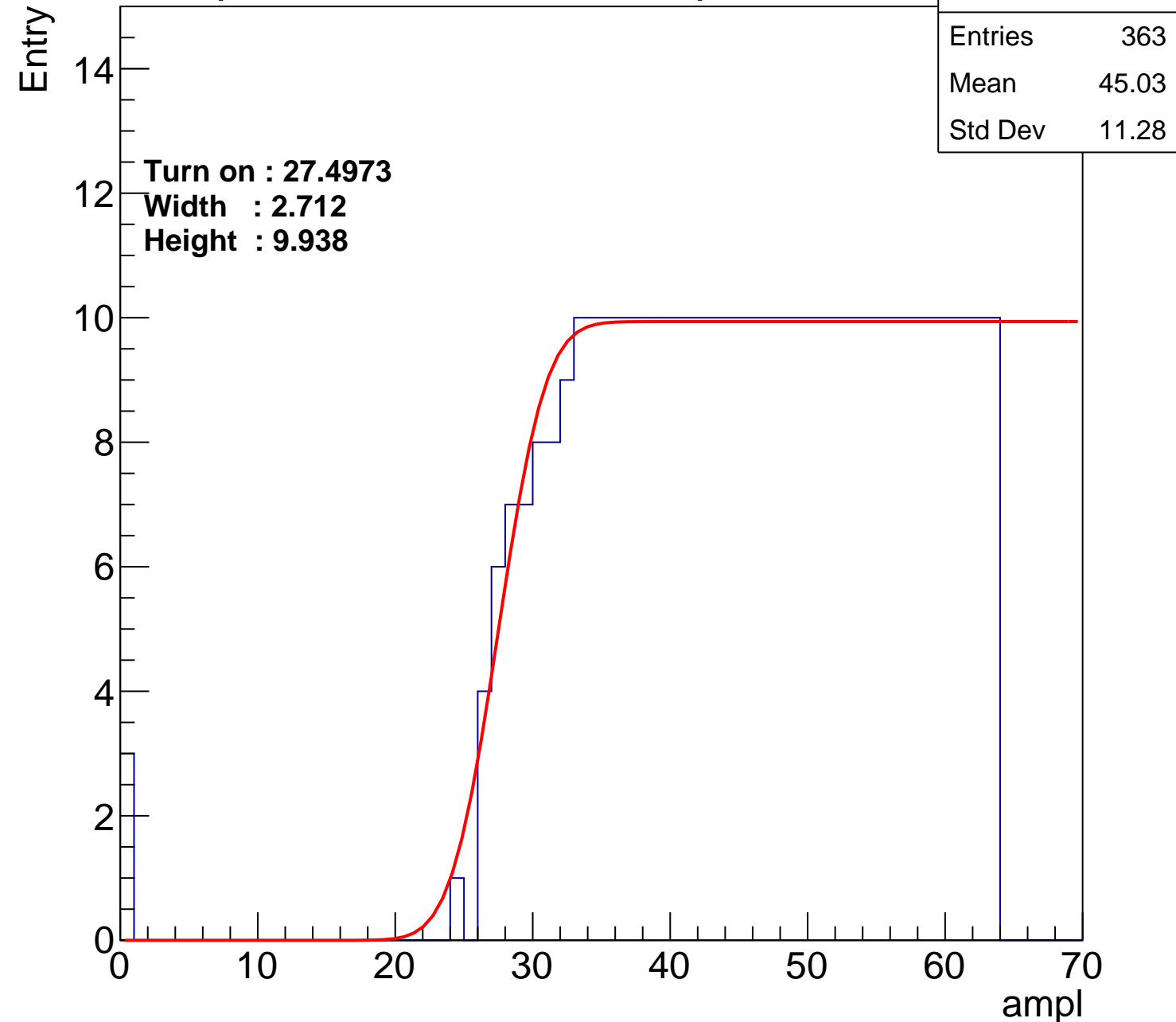
Width : 2.712

Height : 9.938

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch48

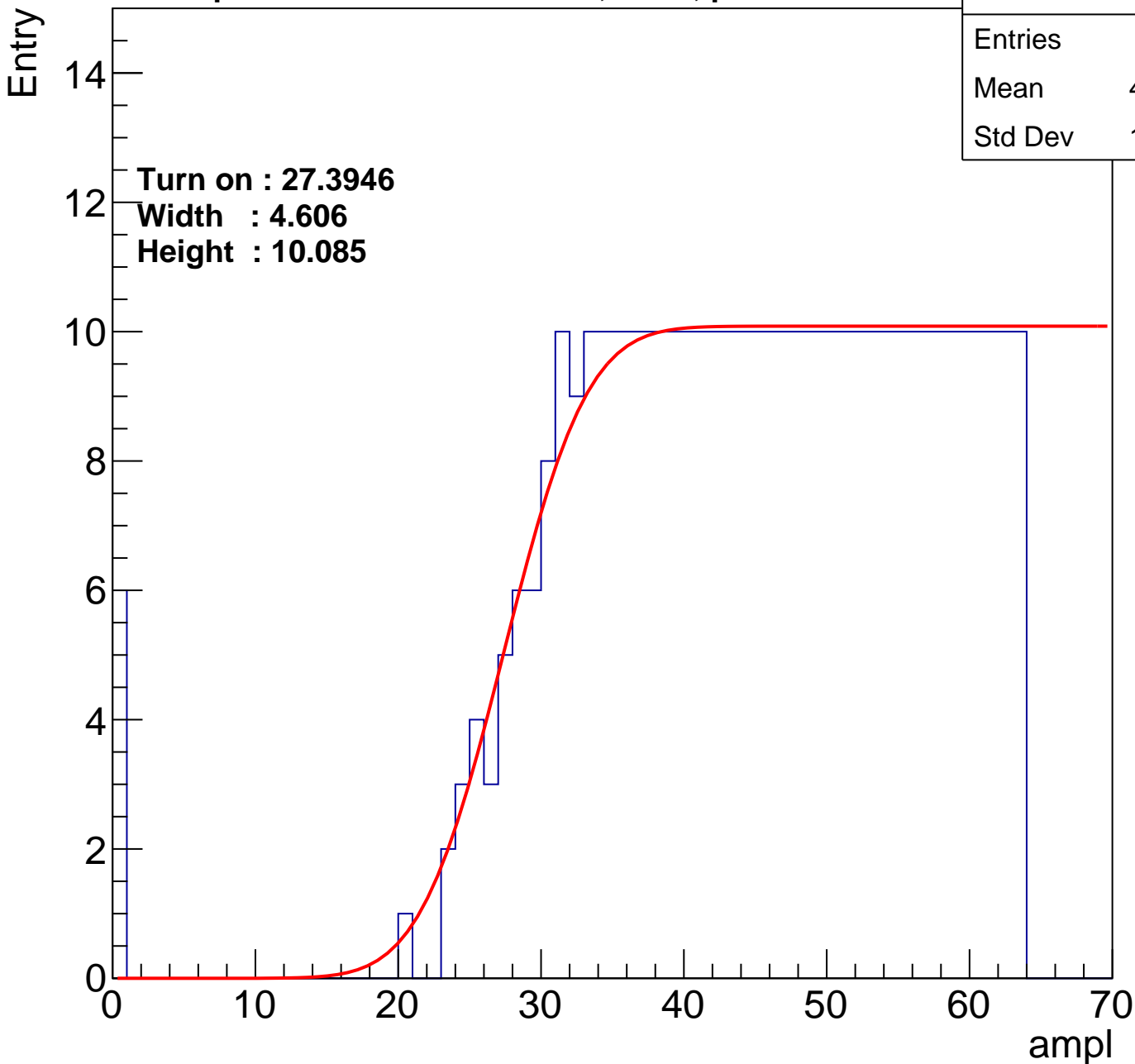
calib_packv5_042523_0143.root, FC#9, port A1

Entries	373
Mean	44.27
Std Dev	12.18

Turn on : 27.3946

Width : 4.606

Height : 10.085



B0L001S, U3-ch49

calib_packv5_042523_0143.root, FC#9, port A1

Entries	369
Mean	44.6
Std Dev	11.72

Turn on : 27.6987

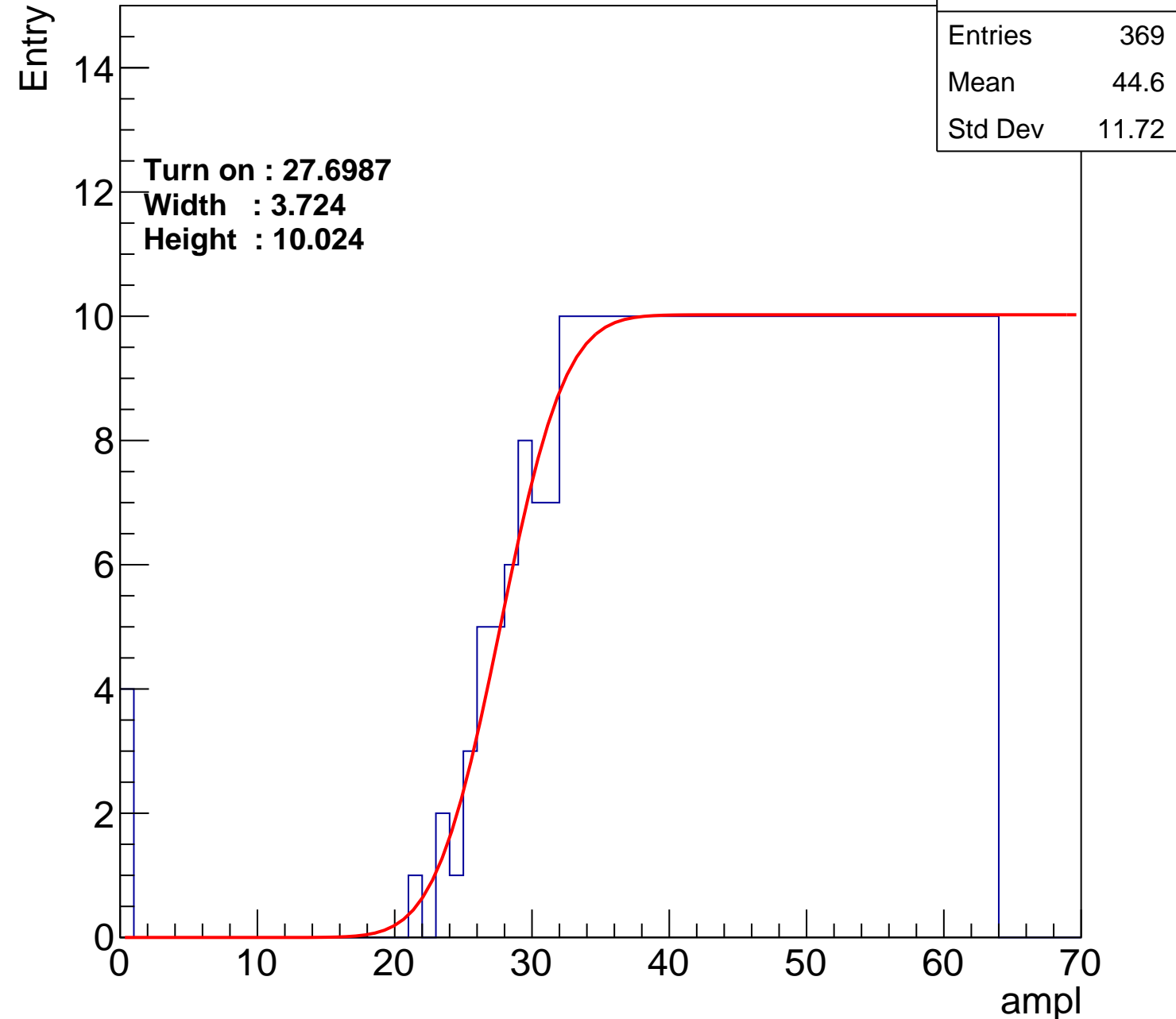
Width : 3.724

Height : 10.024

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch50

calib_packv5_042523_0143.root, FC#9, port A1

Entries	356
Mean	45.09
Std Dev	11.74

Turn on : 28.9810

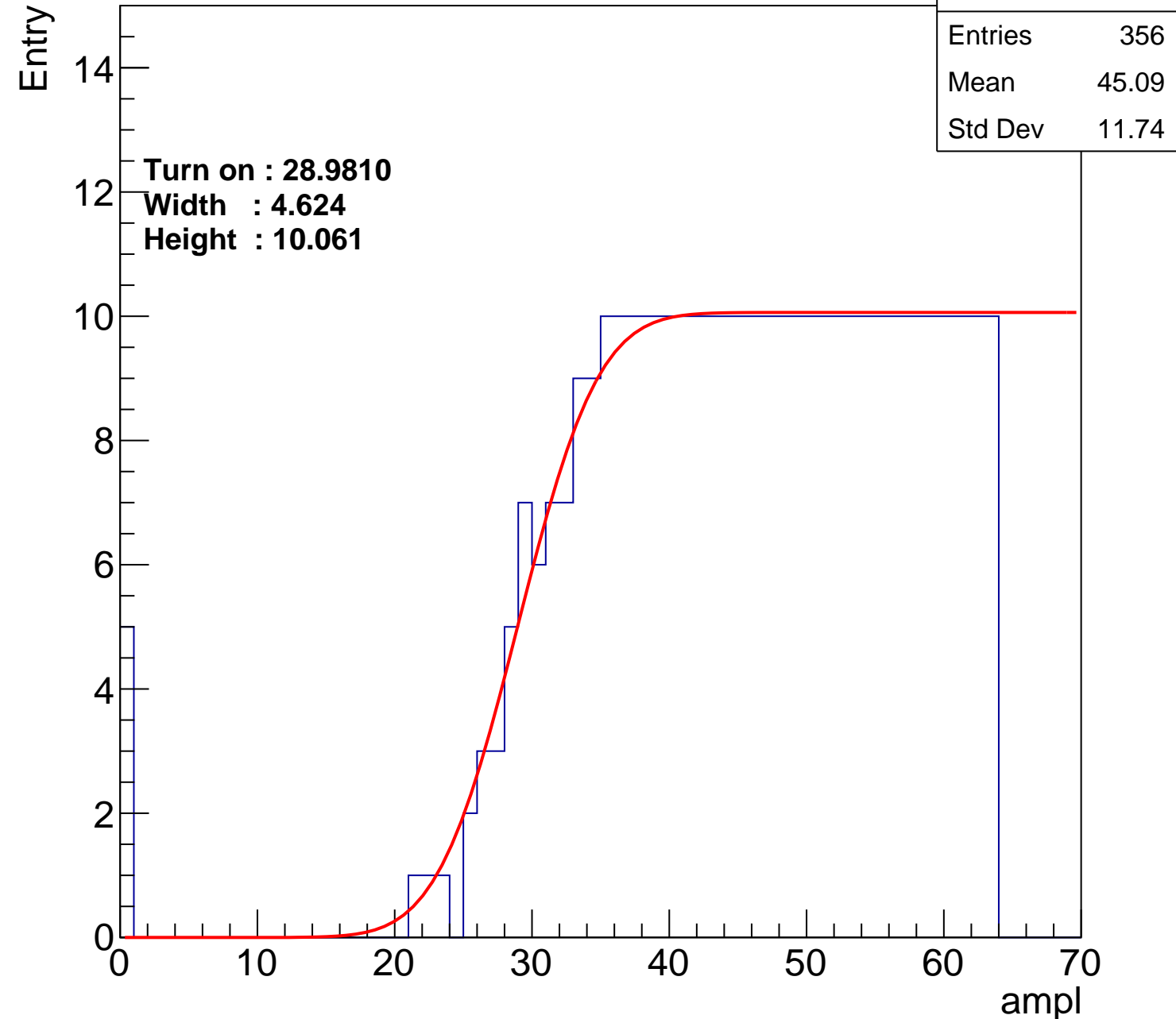
Width : 4.624

Height : 10.061

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch51

calib_packv5_042523_0143.root, FC#9, port A1

Entries	354
Mean	45.47
Std Dev	11.08

Turn on : 29.0474

Width : 2.531

Height : 10.006

Entry

14

12

10

8

6

4

2

0

0

10

20

30

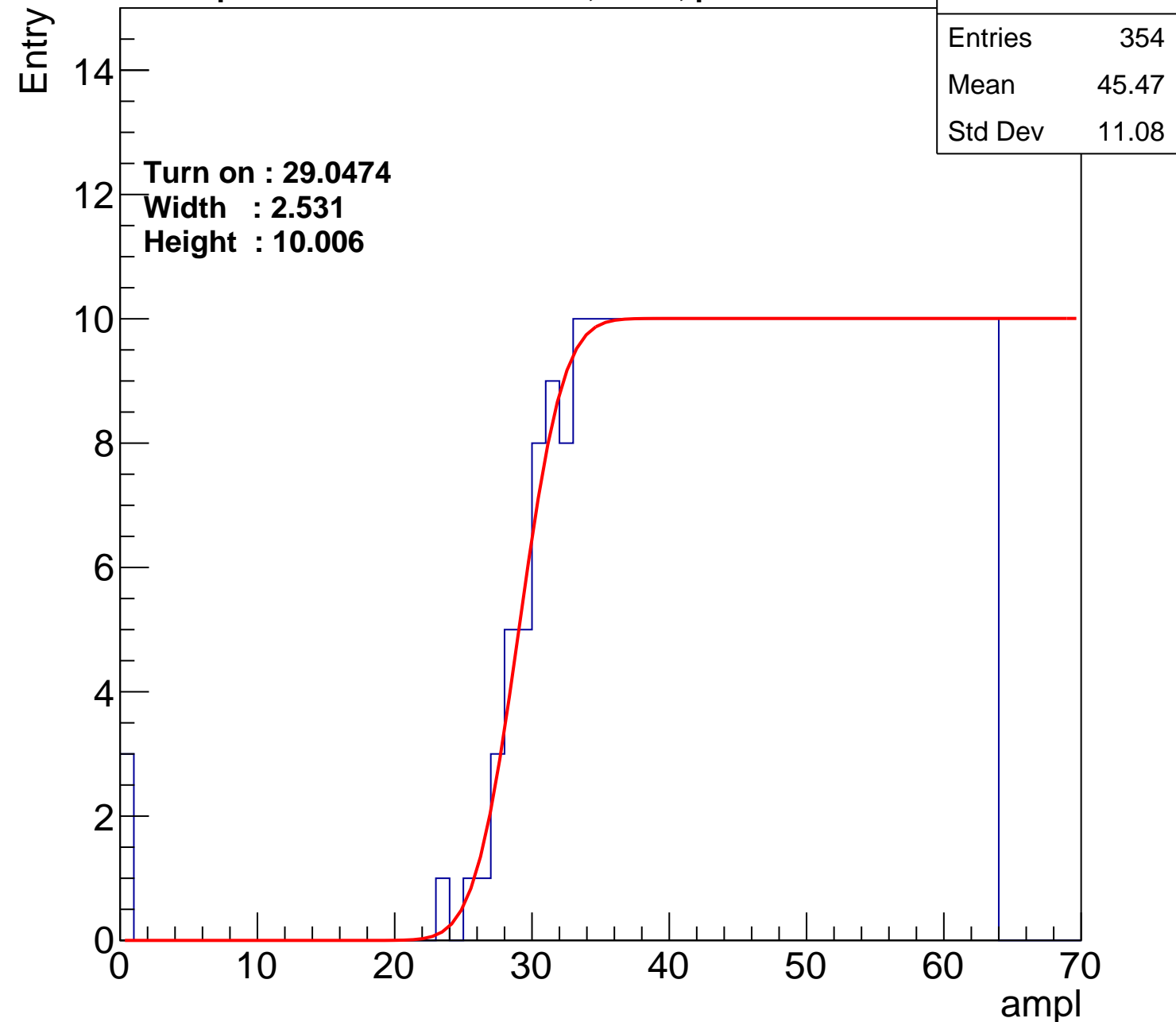
40

50

60

70

ampl



B0L001S, U3-ch52

calib_packv5_042523_0143.root, FC#9, port A1

Entries	355
Mean	45.48
Std Dev	10.91

Turn on : 29.3920

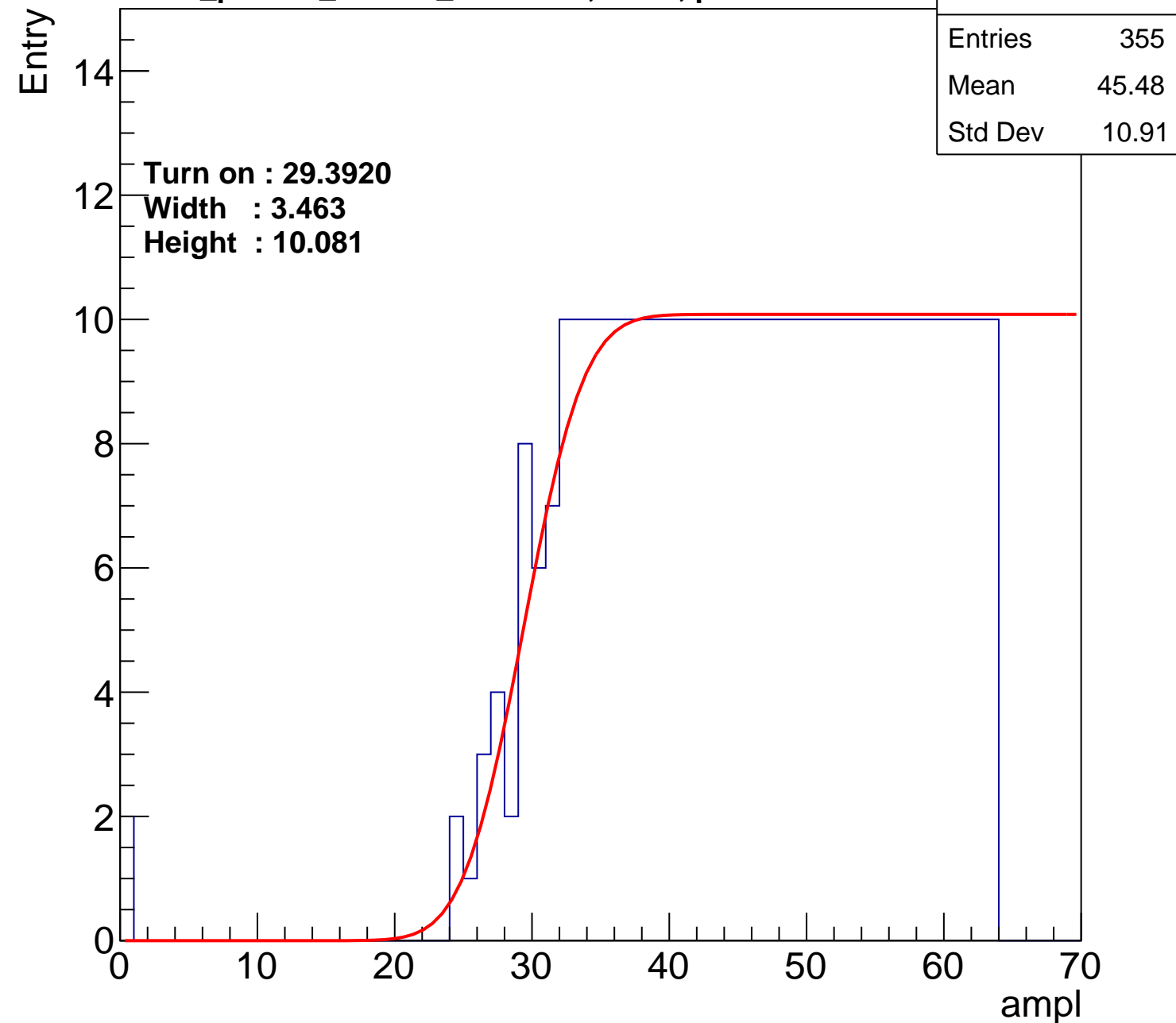
Width : 3.463

Height : 10.081

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch53

calib_packv5_042523_0143.root, FC#9, port A1

Entries	370
Mean	44.52
Std Dev	11.79

Turn on : 27.4373

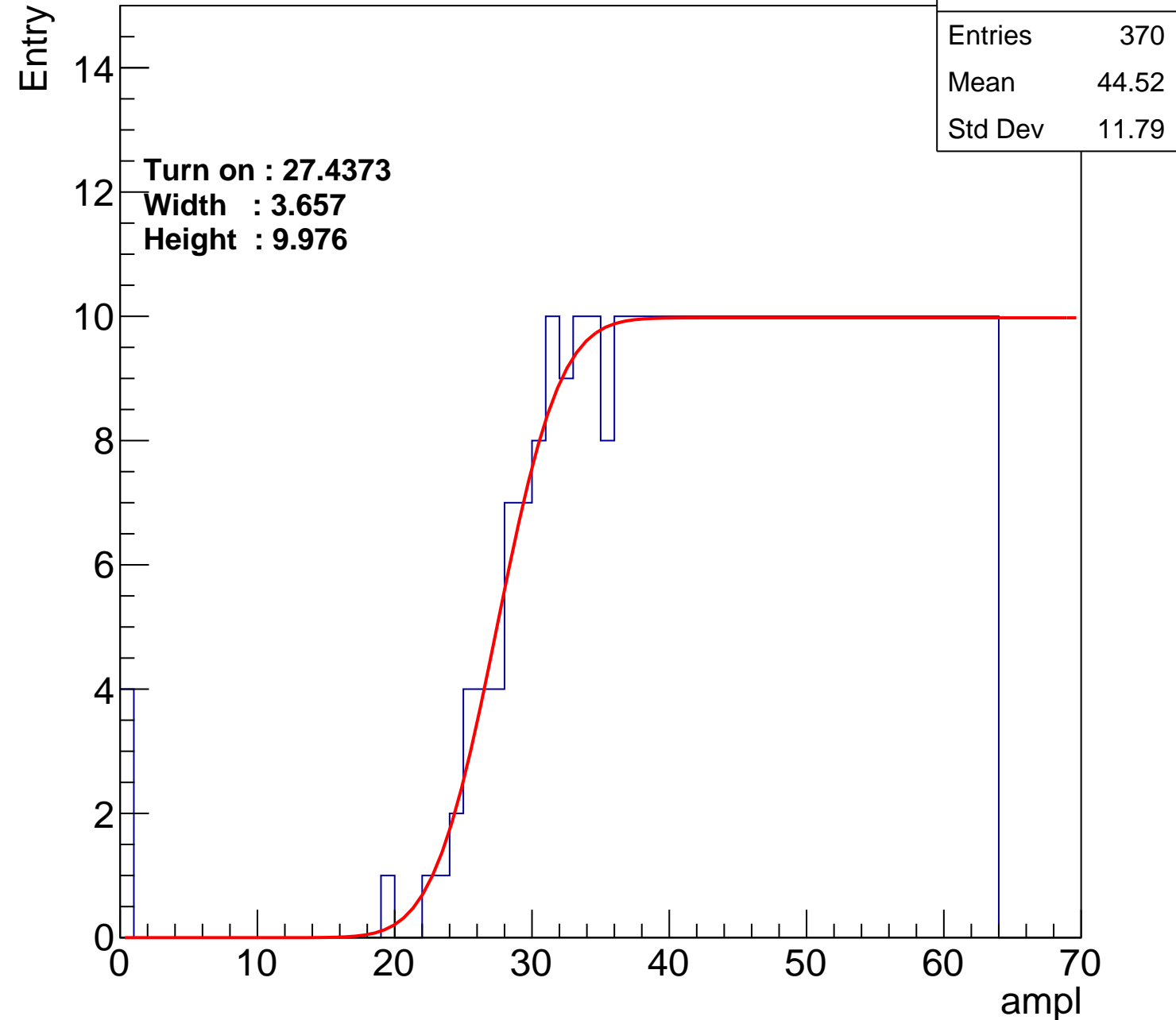
Width : 3.657

Height : 9.976

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch54

calib_packv5_042523_0143.root, FC#9, port A1

Entries	355
Mean	45.15
Std Dev	11.78

Turn on : 28.9254

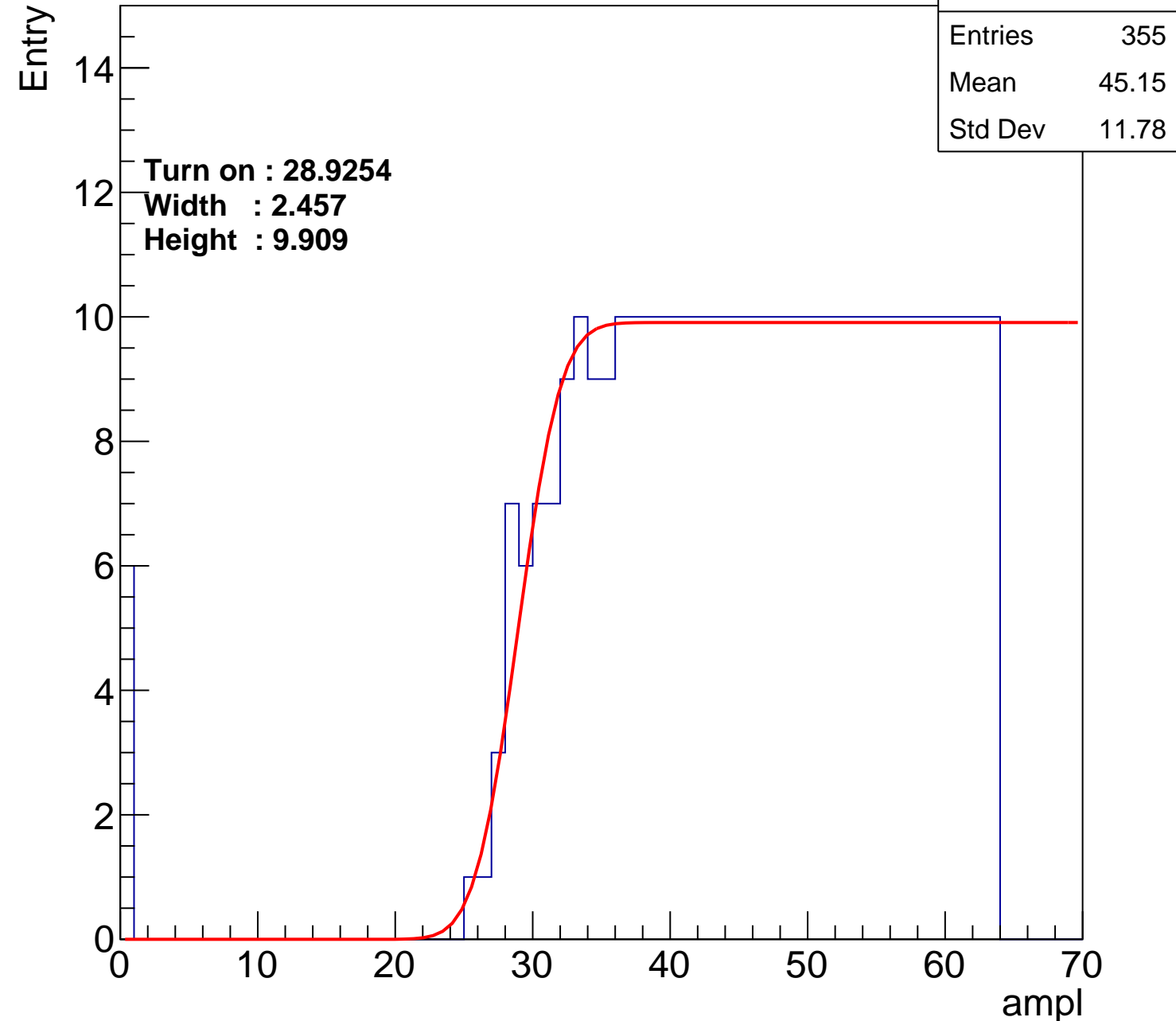
Width : 2.457

Height : 9.909

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch55

calib_packv5_042523_0143.root, FC#9, port A1

Entries	355
Mean	45.25
Std Dev	11.45

Turn on : 28.9889

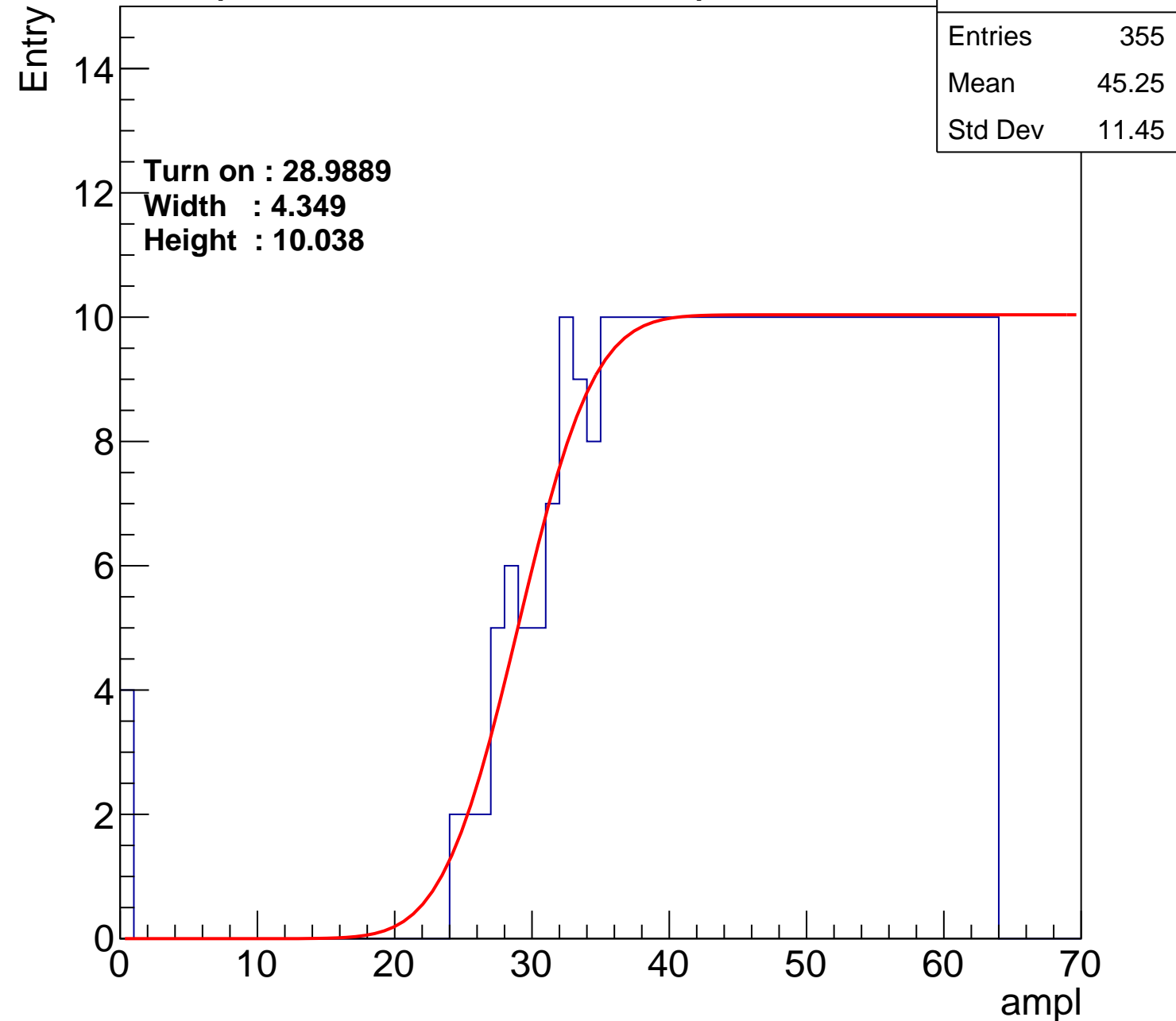
Width : 4.349

Height : 10.038

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch56

calib_packv5_042523_0143.root, FC#9, port A1

Entries	364
Mean	44.92
Std Dev	11.41

Turn on : 28.3948

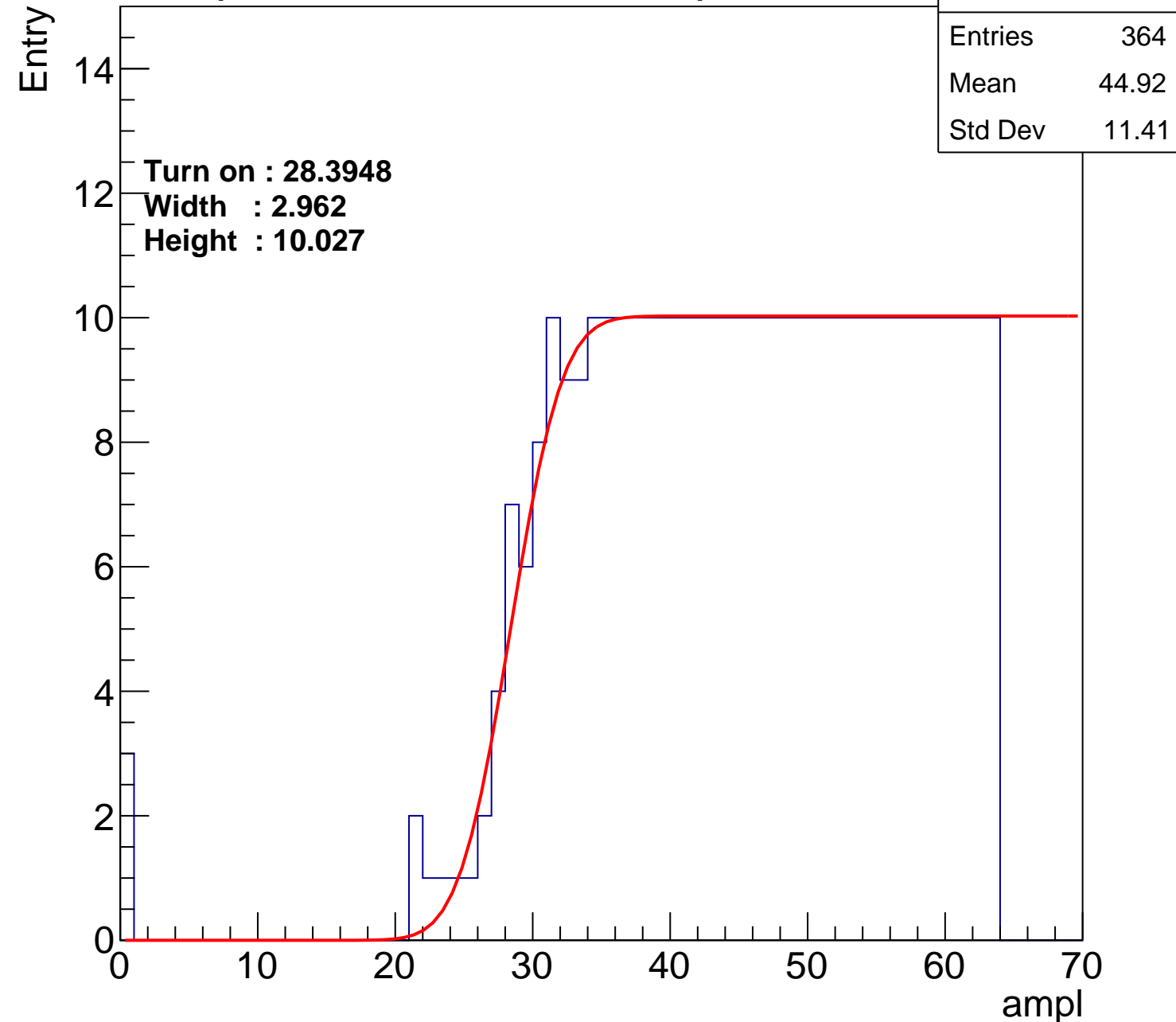
Width : 2.962

Height : 10.027

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch57

calib_packv5_042523_0143.root, FC#9, port A1

Entries	381
Mean	44.13
Std Dev	11.74

Turn on : 26.5153

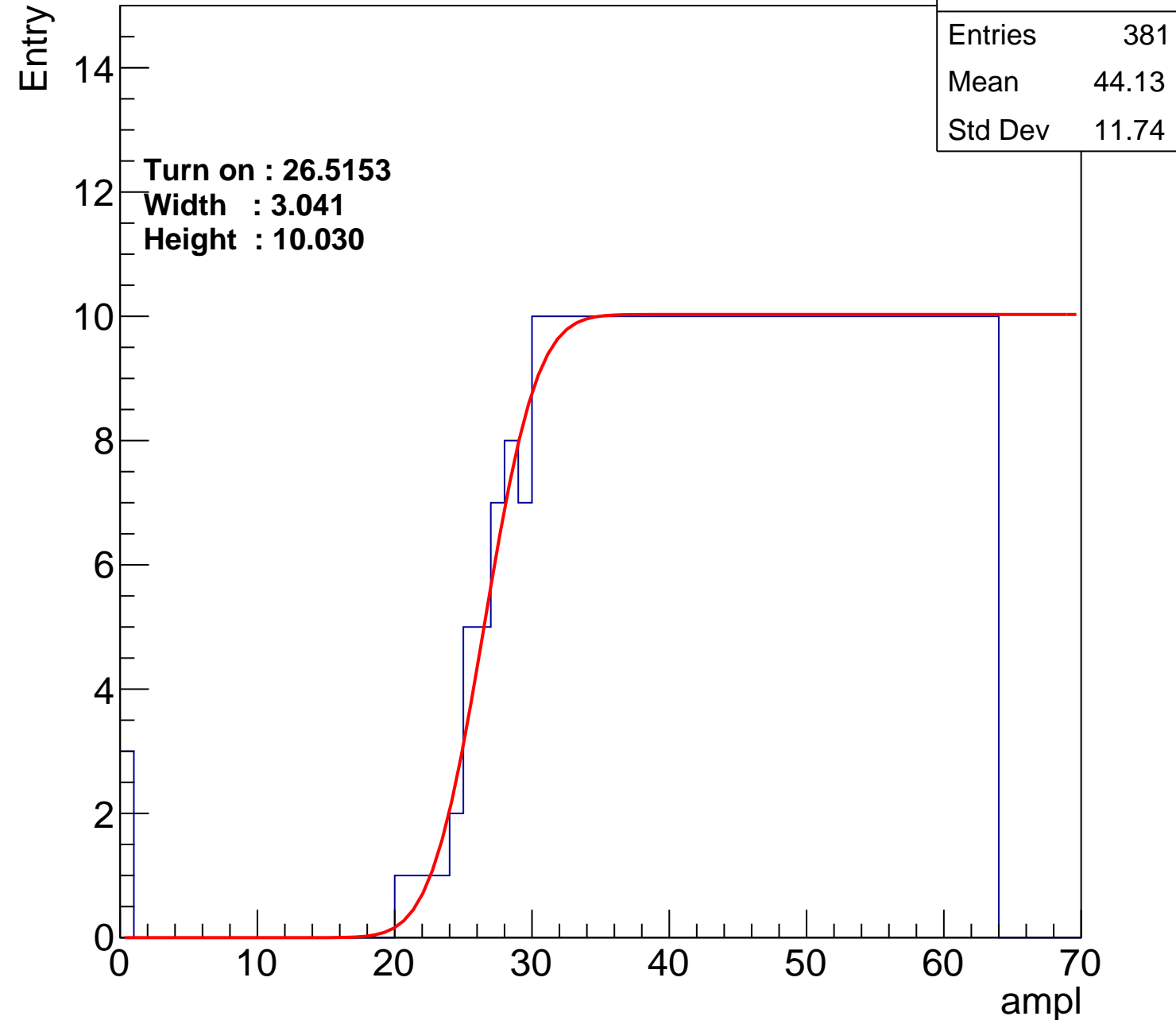
Width : 3.041

Height : 10.030

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch58

calib_packv5_042523_0143.root, FC#9, port A1

Entries	381
Mean	44.2
Std Dev	11.64

Turn on : 26.1424

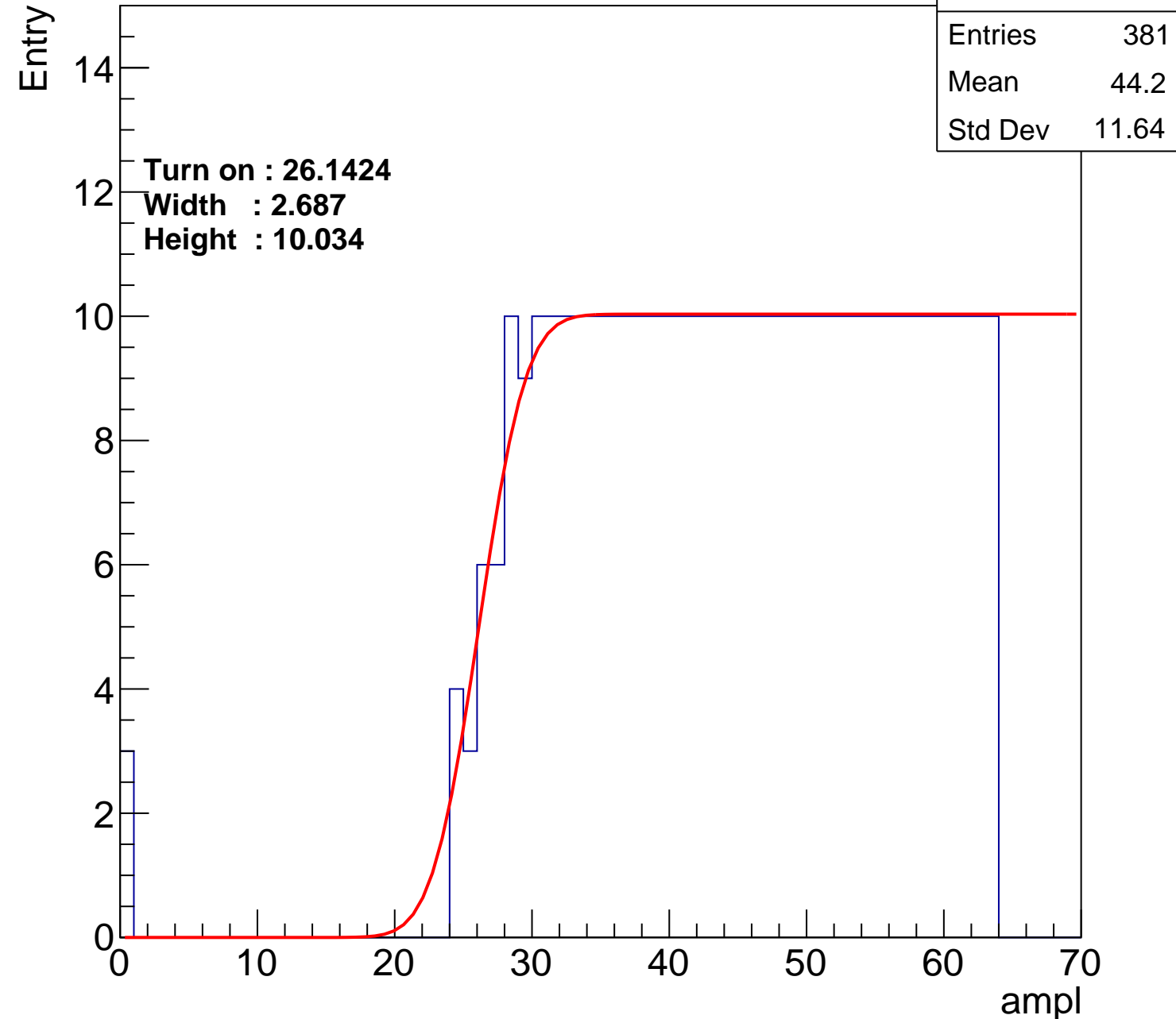
Width : 2.687

Height : 10.034

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch59

calib_packv5_042523_0143.root, FC#9, port A1

Entries	361
Mean	45.07
Std Dev	11.33

Turn on : 28.5154

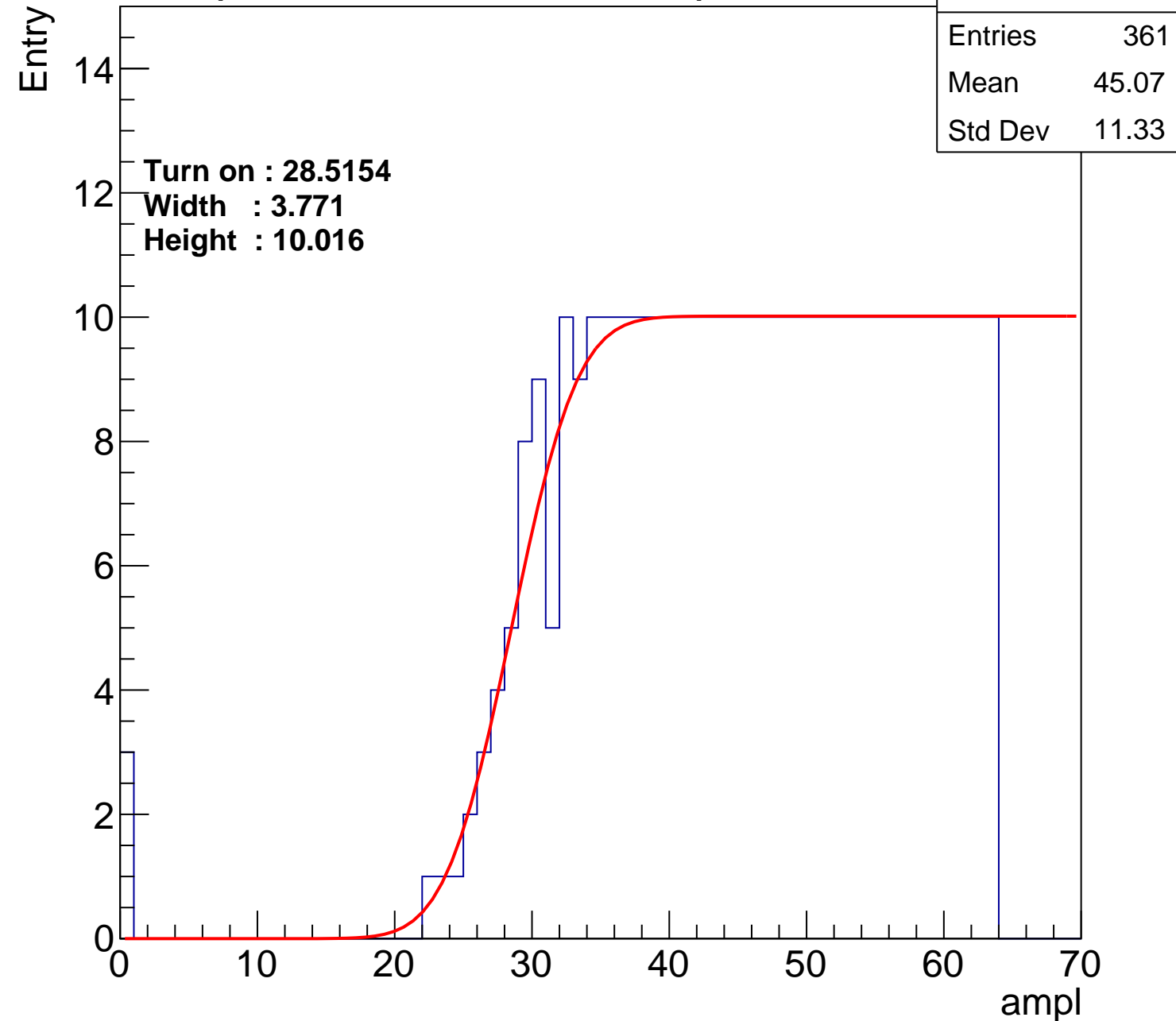
Width : 3.771

Height : 10.016

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch60

calib_packv5_042523_0143.root, FC#9, port A1

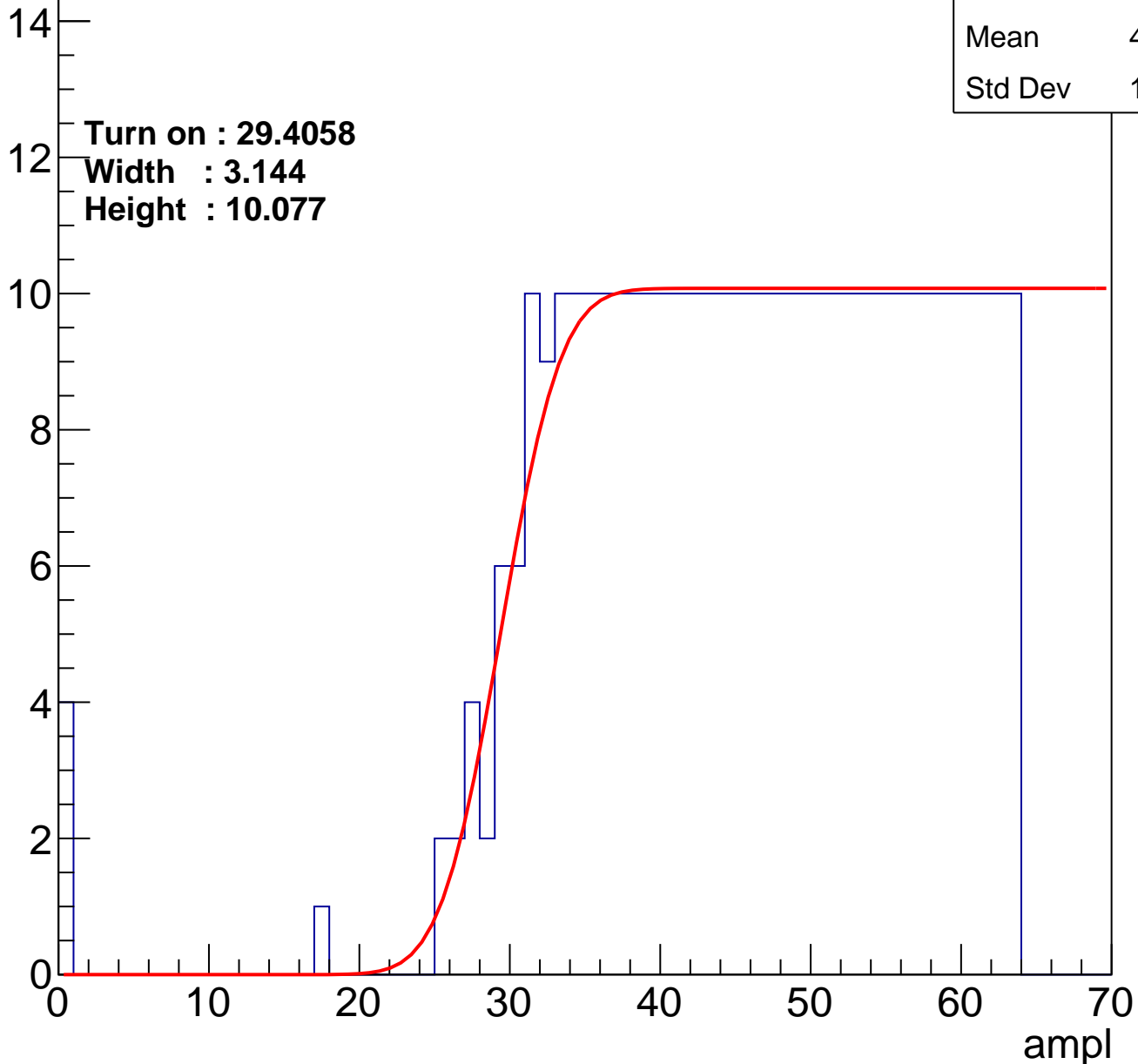
Entries	356
Mean	45.27
Std Dev	11.39

Turn on : 29.4058

Width : 3.144

Height : 10.077

Entry



B0L001S, U3-ch61

calib_packv5_042523_0143.root, FC#9, port A1

Entries	361
Mean	44.96
Std Dev	11.67

Turn on : 27.9448

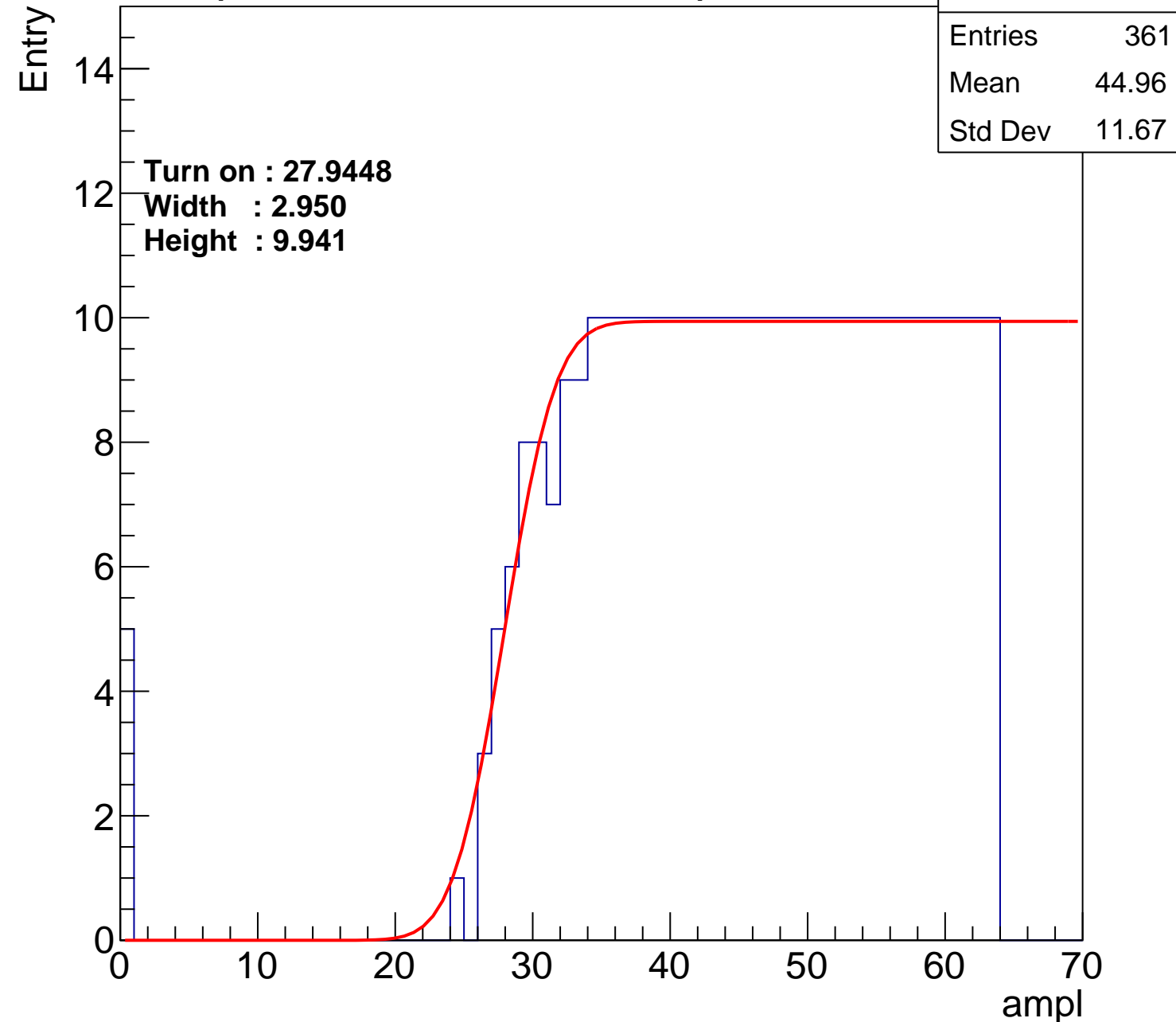
Width : 2.950

Height : 9.941

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch62

calib_packv5_042523_0143.root, FC#9, port A1

Entries	369
Mean	44.73
Std Dev	11.44

Turn on : 27.6941

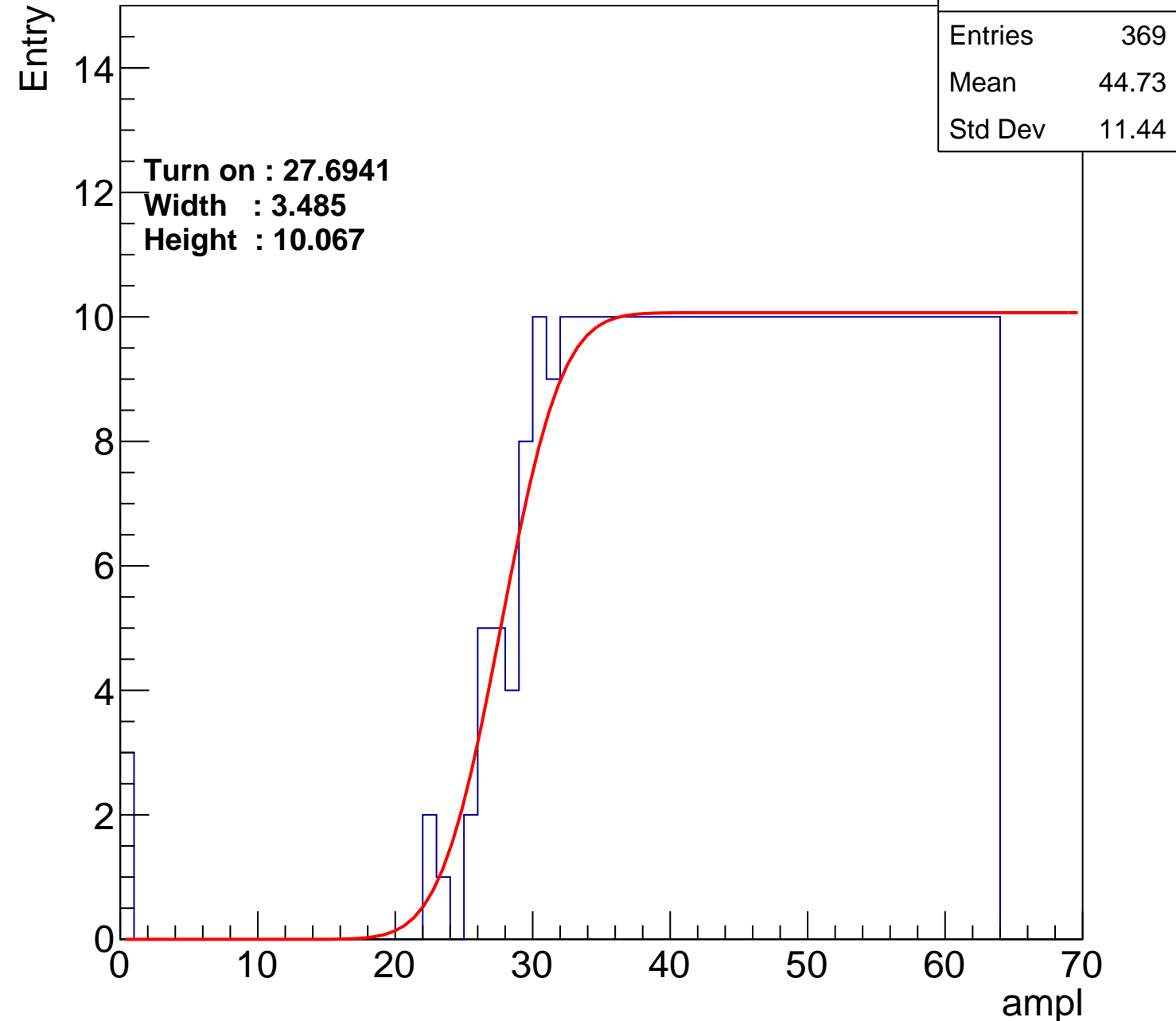
Width : 3.485

Height : 10.067

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch63

calib_packv5_042523_0143.root, FC#9, port A1

Entries	359
Mean	45.27
Std Dev	11.03

Turn on : 28.6667

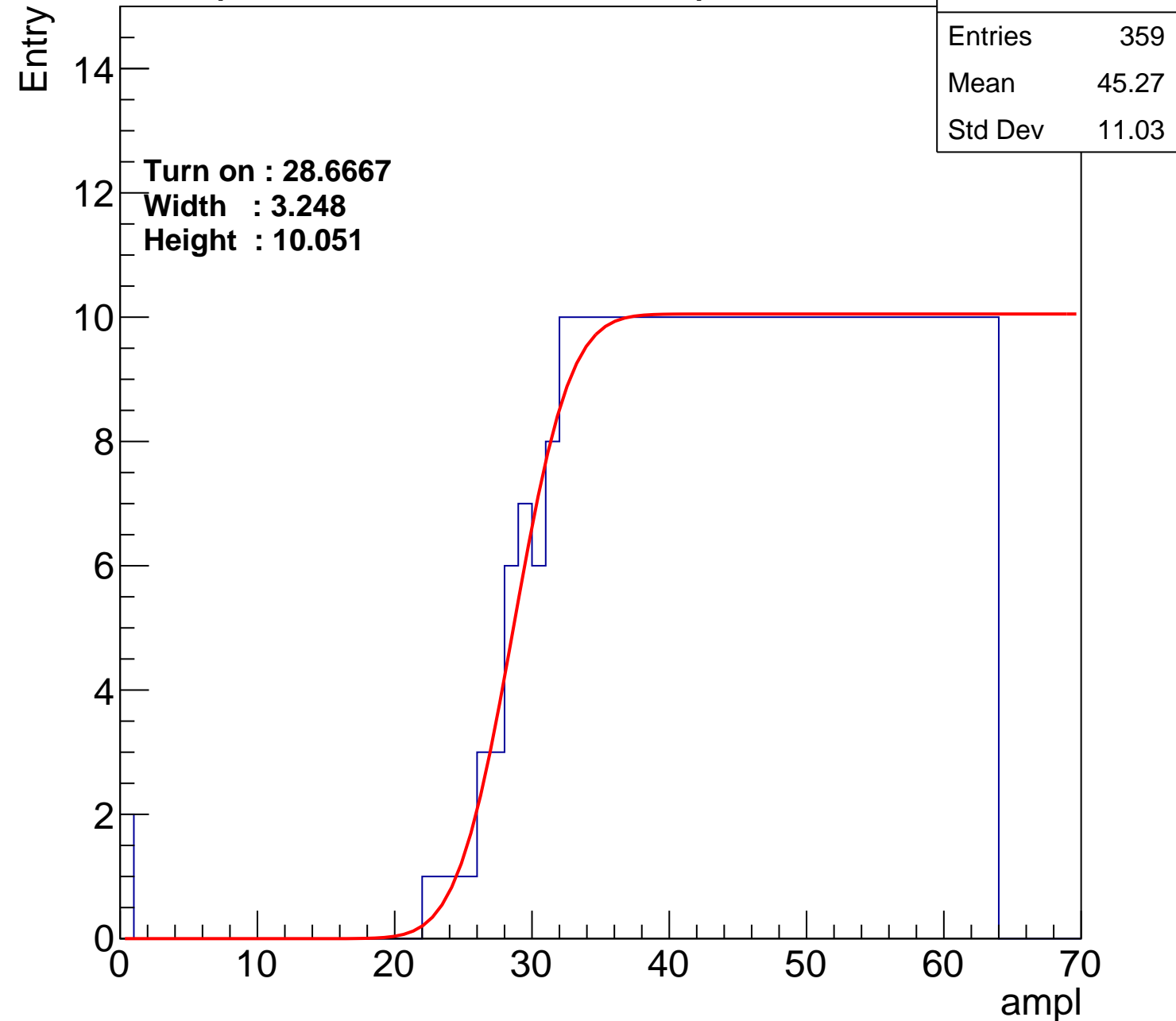
Width : 3.248

Height : 10.051

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch64

calib_packv5_042523_0143.root, FC#9, port A1

Entries	363
Mean	44.94
Std Dev	11.51

Turn on : 28.4172

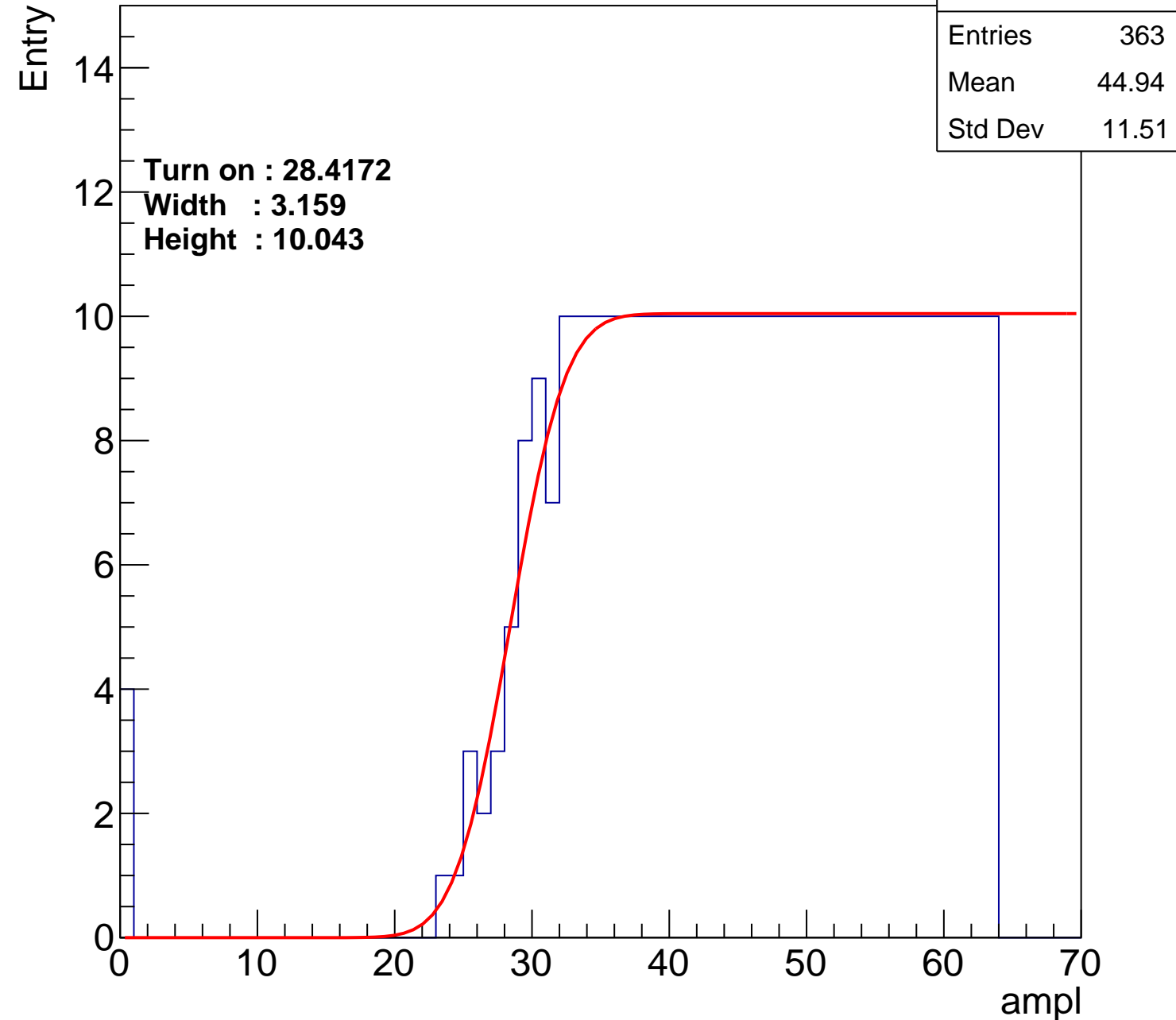
Width : 3.159

Height : 10.043

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch65

calib_packv5_042523_0143.root, FC#9, port A1

Entries	362
Mean	44.99
Std Dev	11.49

Turn on : 28.0880

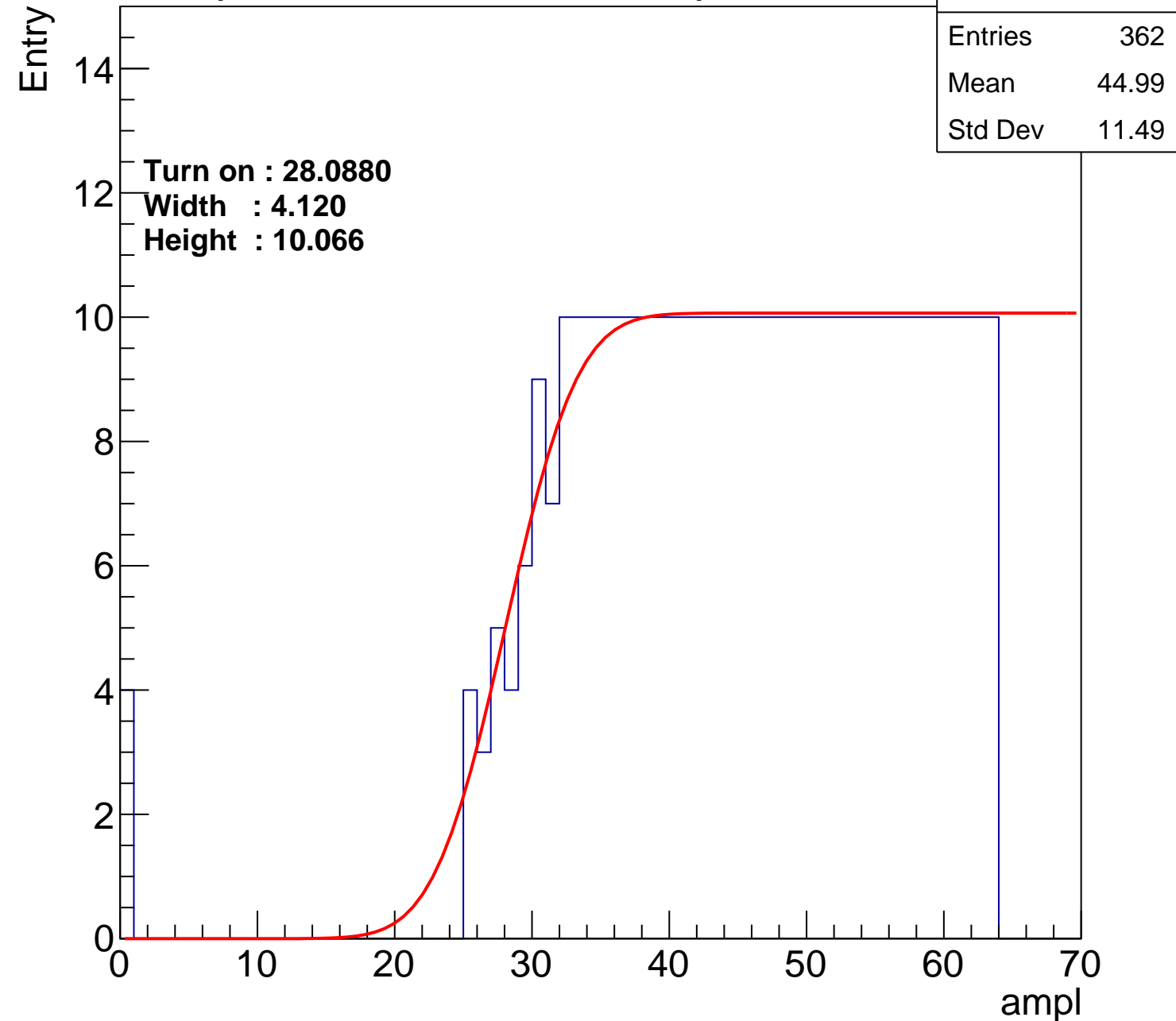
Width : 4.120

Height : 10.066

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch66

calib_packv5_042523_0143.root, FC#9, port A1

Entries	373
Mean	44.35
Std Dev	11.96

Turn on : 27.4112

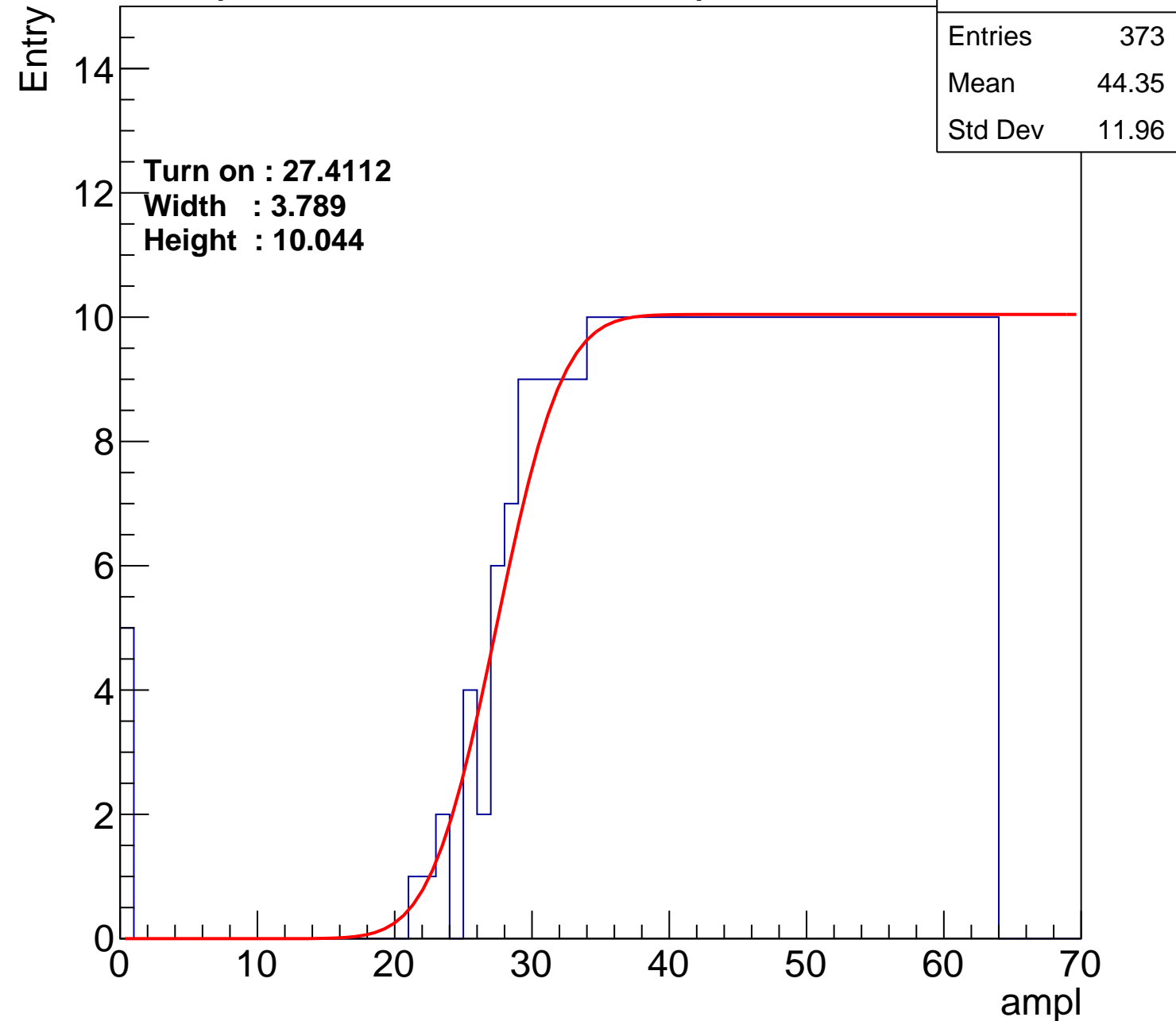
Width : 3.789

Height : 10.044

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch67

calib_packv5_042523_0143.root, FC#9, port A1

Entries	382
Mean	44.25
Std Dev	11.35

Turn on : 26.2278

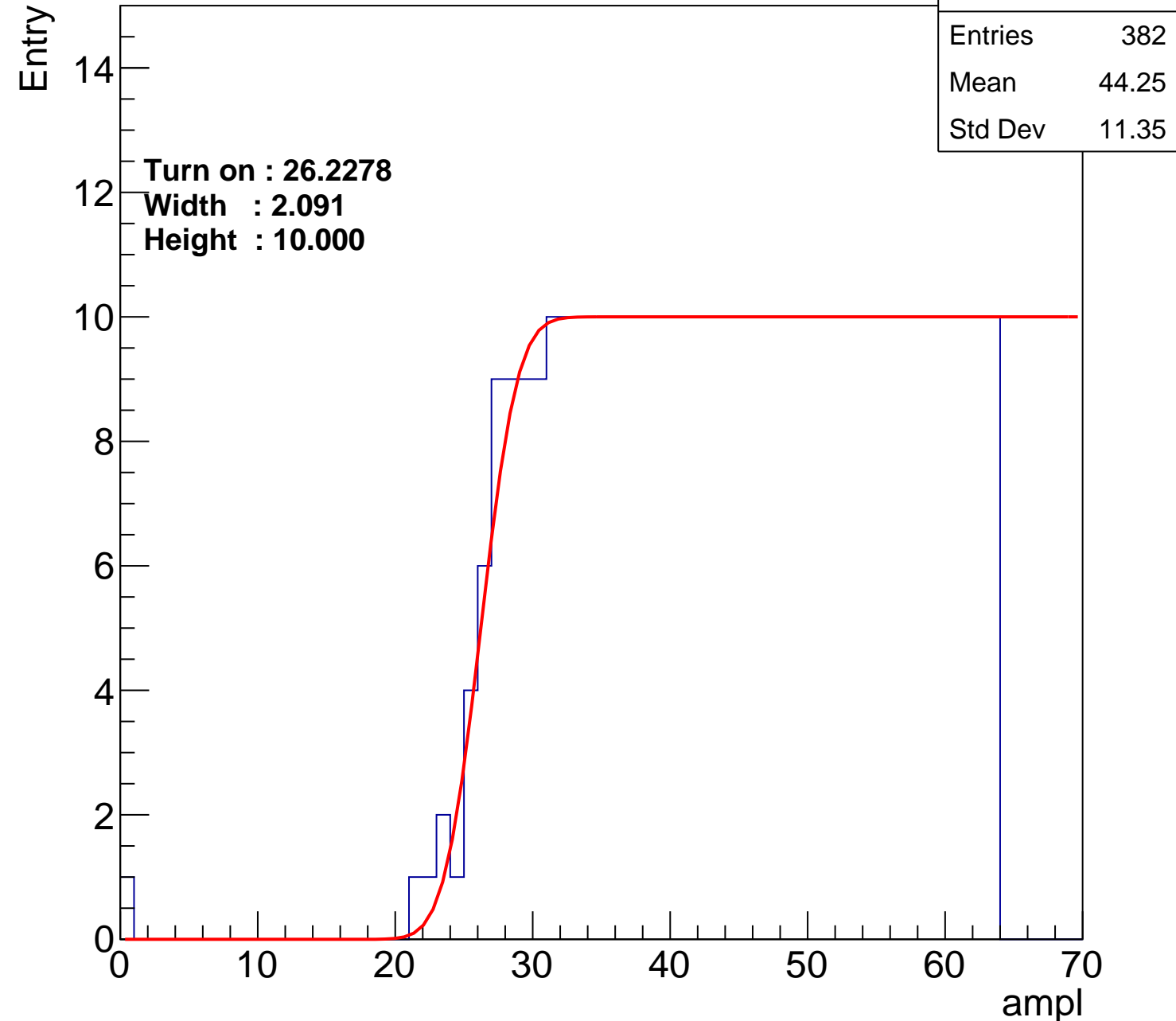
Width : 2.091

Height : 10.000

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch68

calib_packv5_042523_0143.root, FC#9, port A1

Entries	358
Mean	45.29
Std Dev	11.13

Turn on : 28.4505

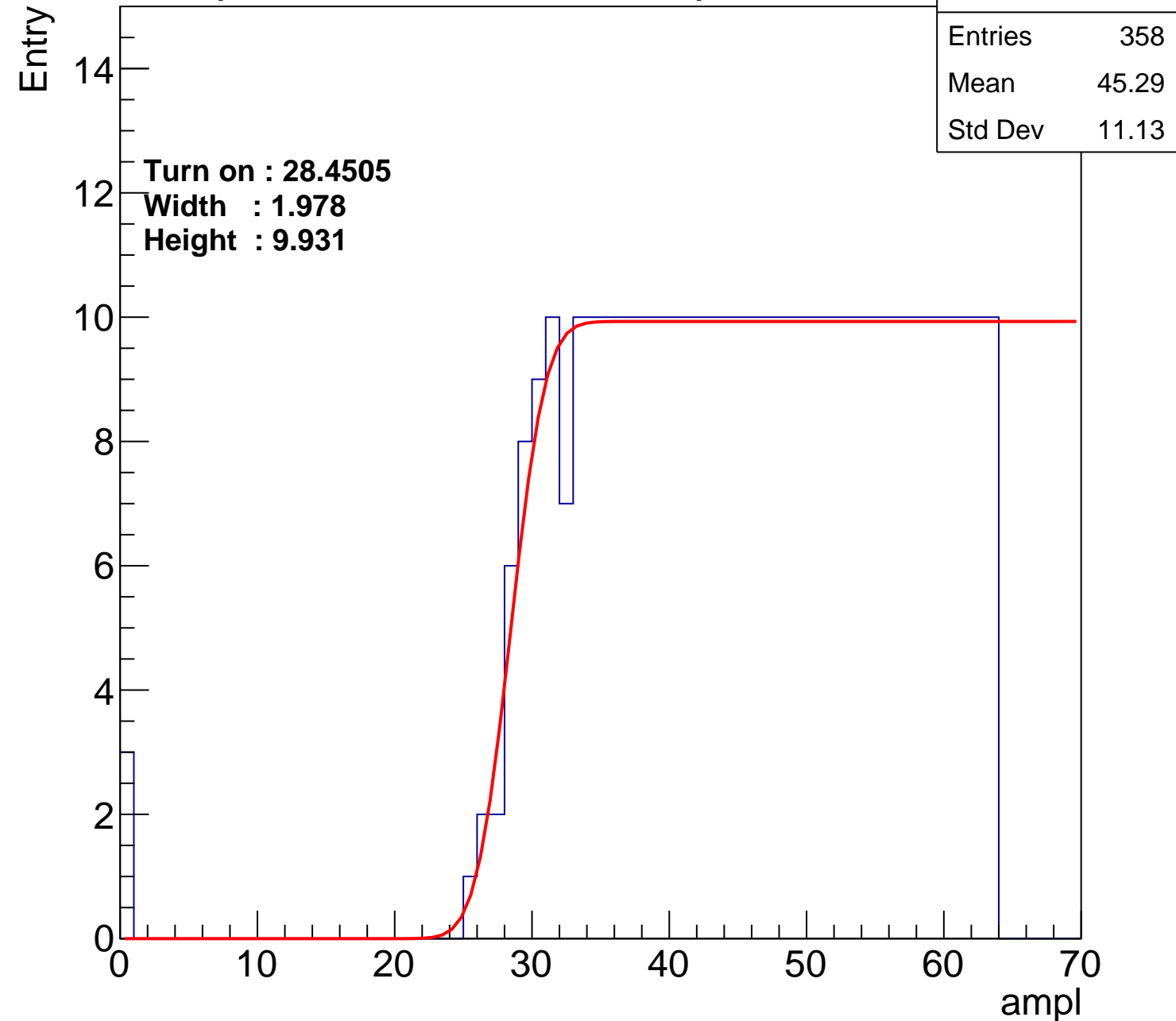
Width : 1.978

Height : 9.931

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch69

calib_packv5_042523_0143.root, FC#9, port A1

Entries	363
Mean	44.9
Std Dev	11.58

Turn on : 28.6195

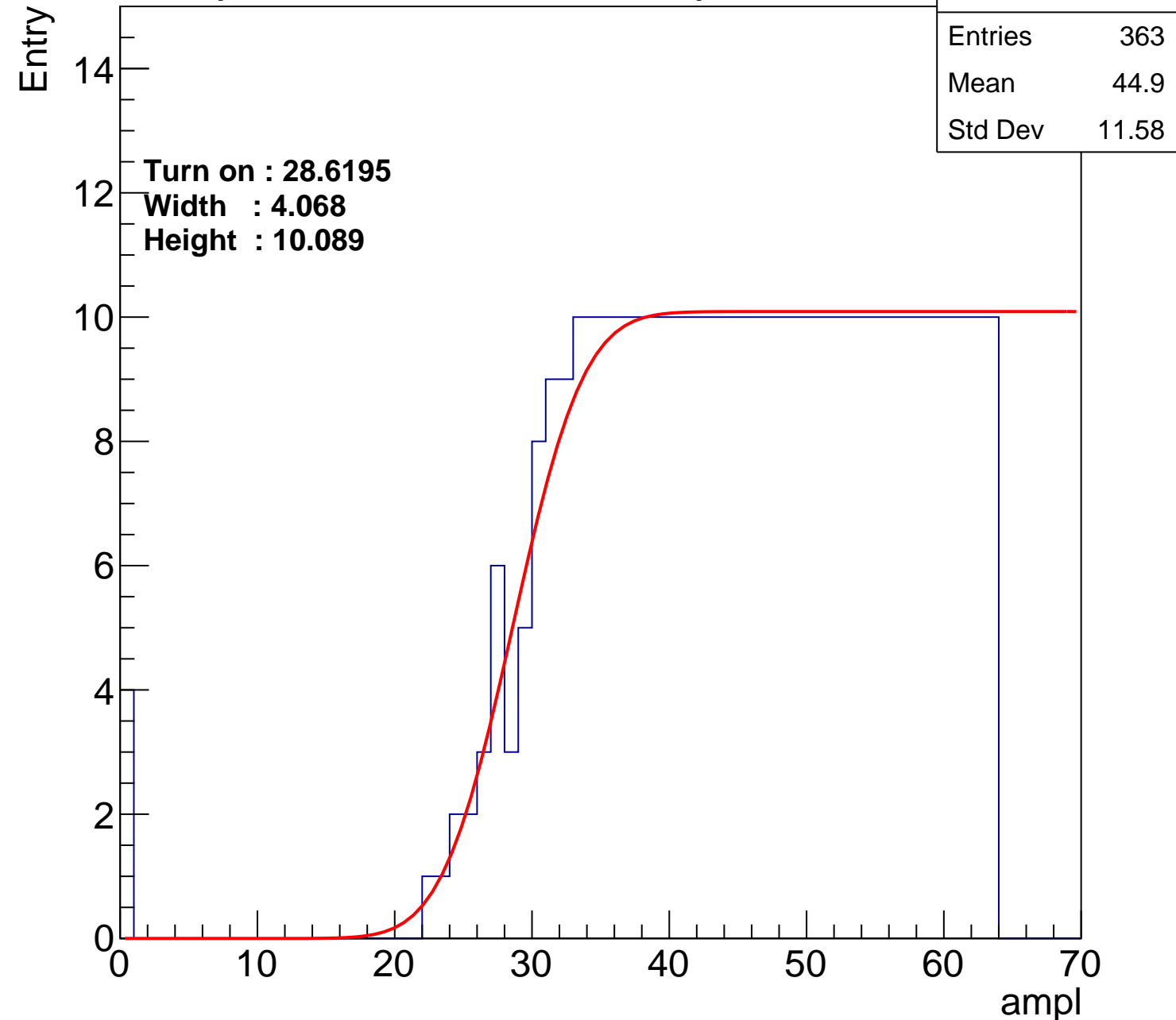
Width : 4.068

Height : 10.089

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch70

calib_packv5_042523_0143.root, FC#9, port A1

Entries	366
Mean	44.96
Std Dev	11.15

Turn on : 27.7987

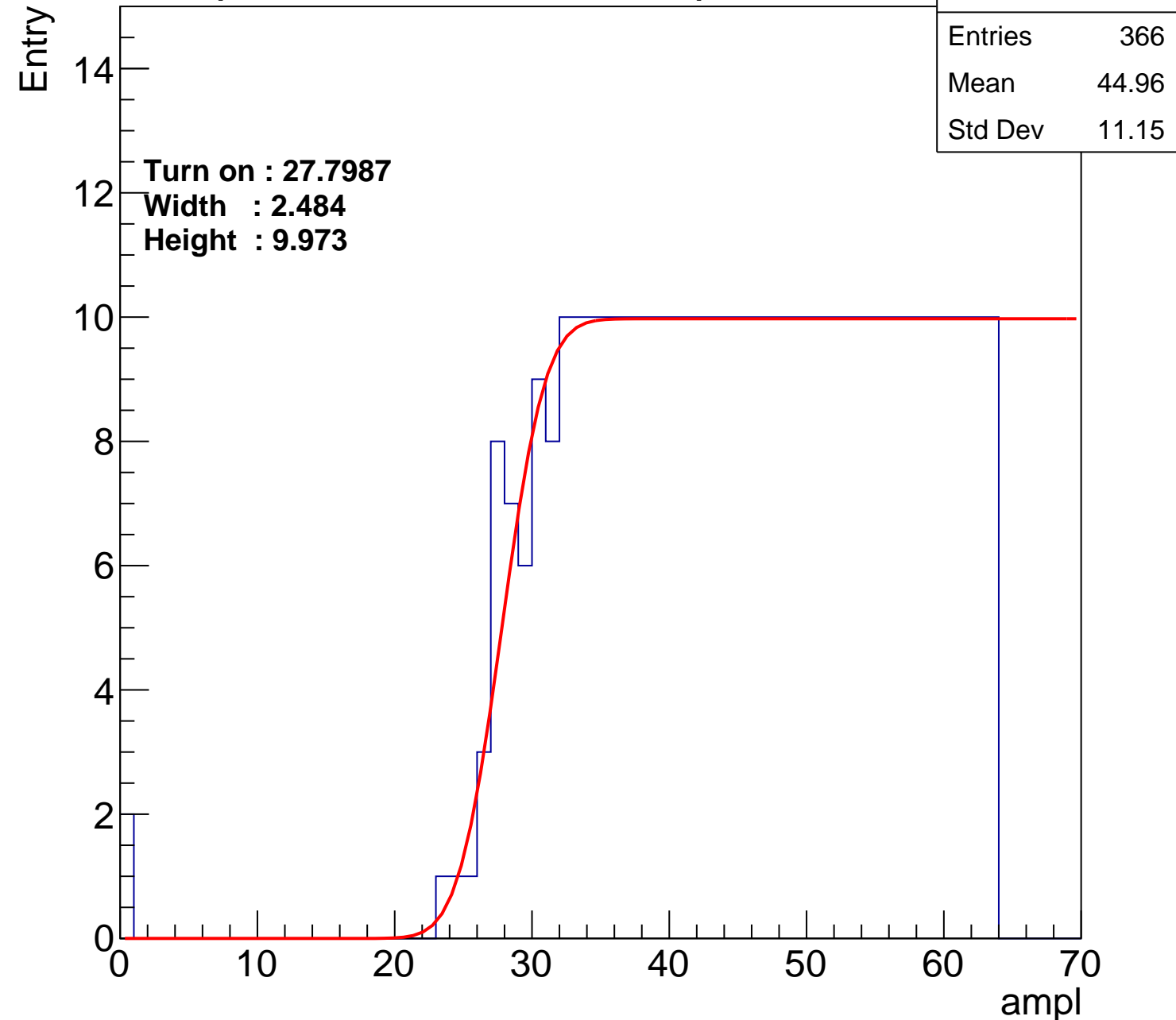
Width : 2.484

Height : 9.973

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch71

calib_packv5_042523_0143.root, FC#9, port A1

Entries	374
Mean	44.26
Std Dev	12.14

Turn on : 27.8179

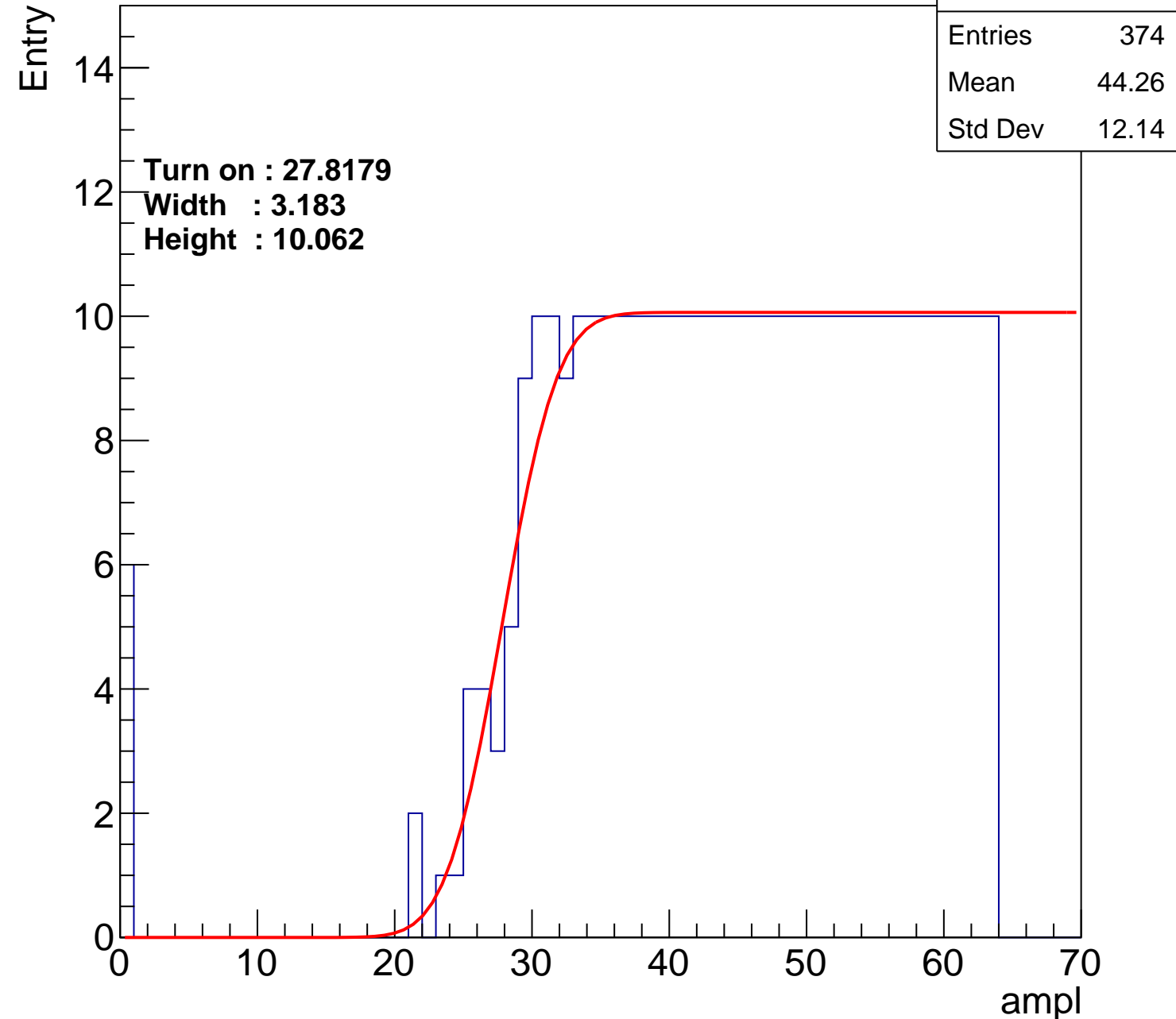
Width : 3.183

Height : 10.062

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch72

calib_packv5_042523_0143.root, FC#9, port A1

Entries	363
Mean	45.01
Std Dev	11.31

Turn on : 28.0202

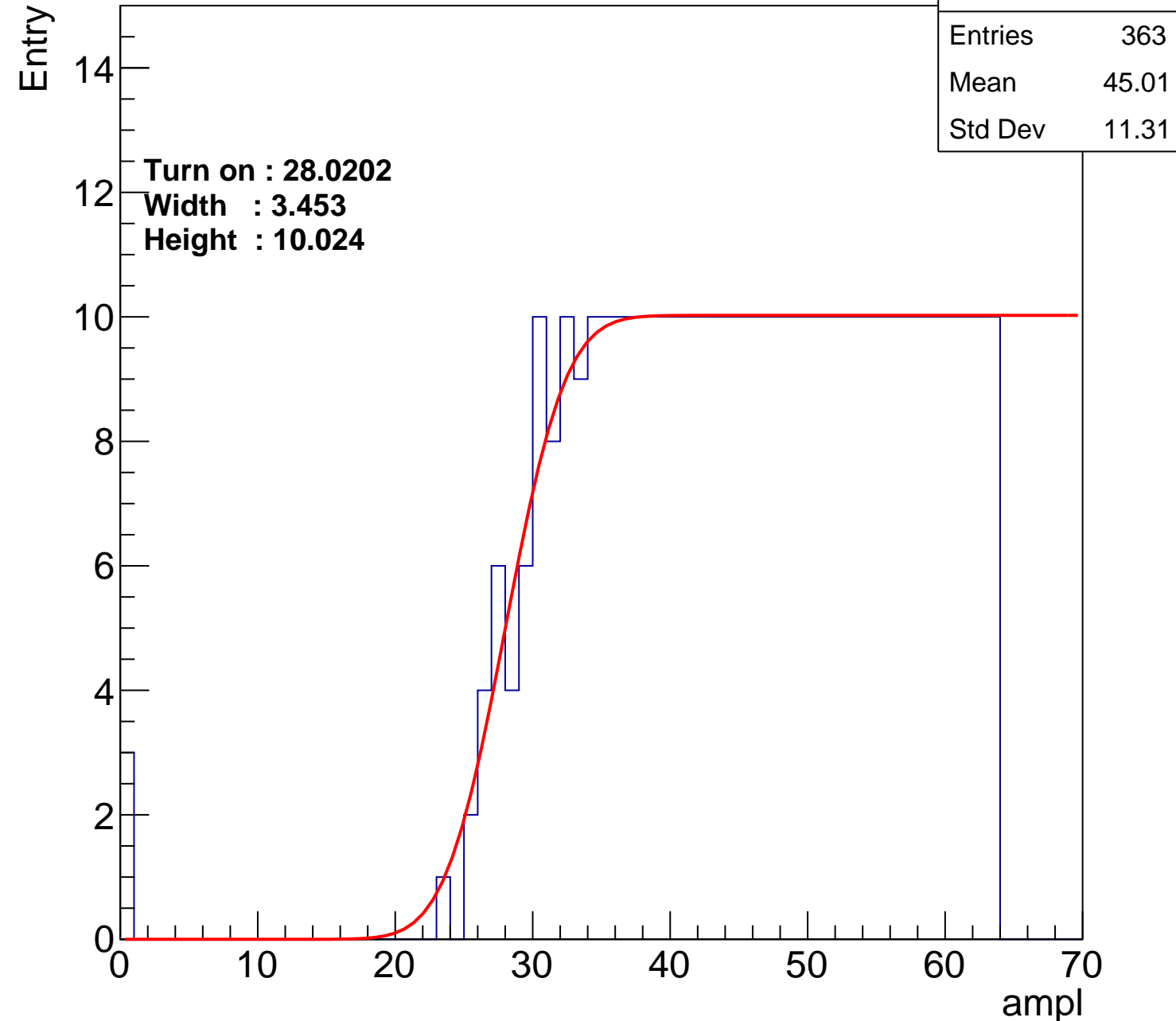
Width : 3.453

Height : 10.024

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch73

calib_packv5_042523_0143.root, FC#9, port A1

Entries	358
Mean	45.36
Std Dev	10.94

Turn on : 28.4835

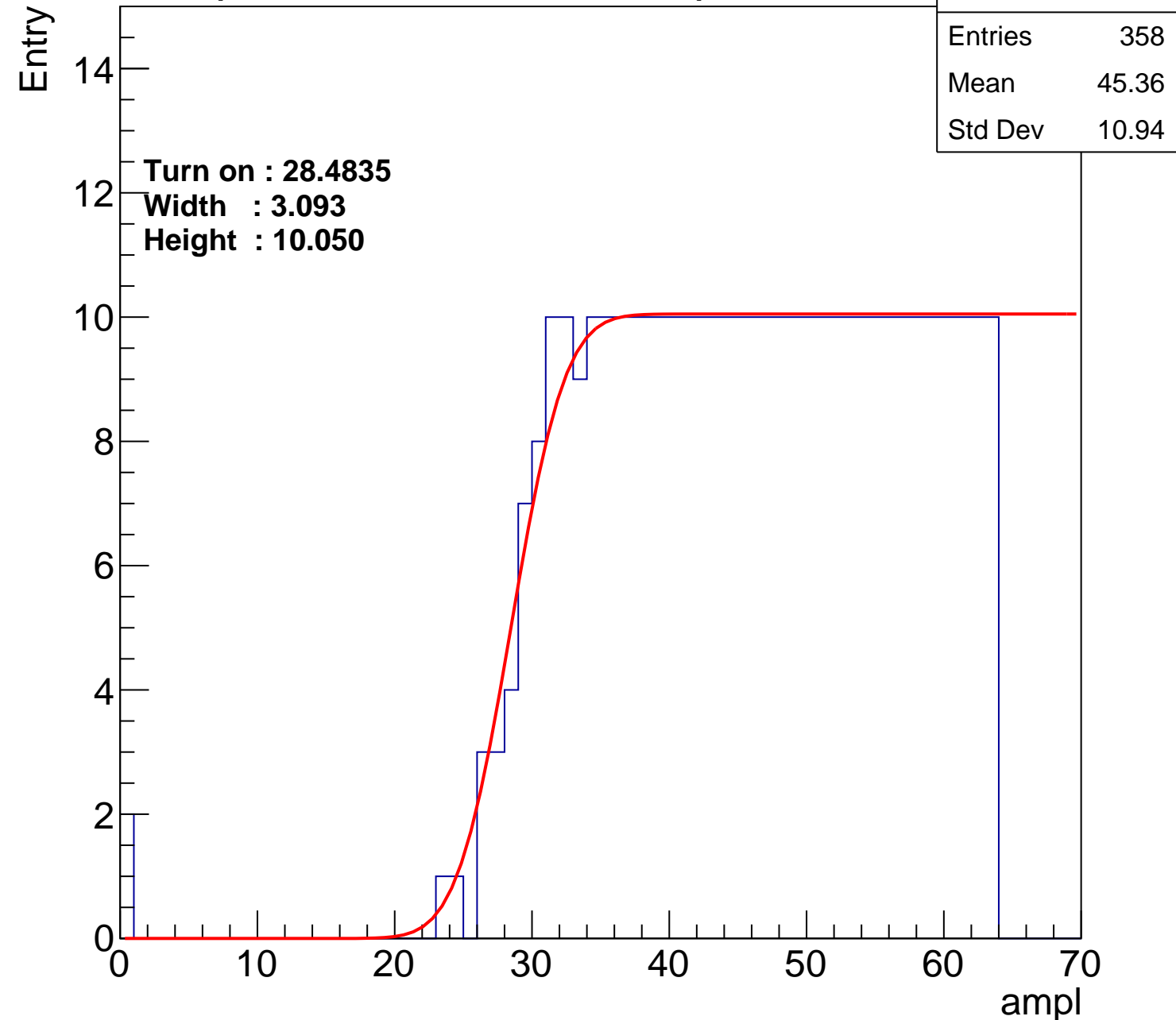
Width : 3.093

Height : 10.050

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch74

calib_packv5_042523_0143.root, FC#9, port A1

Entries	348
Mean	45.78
Std Dev	10.8

Turn on : 29.5152

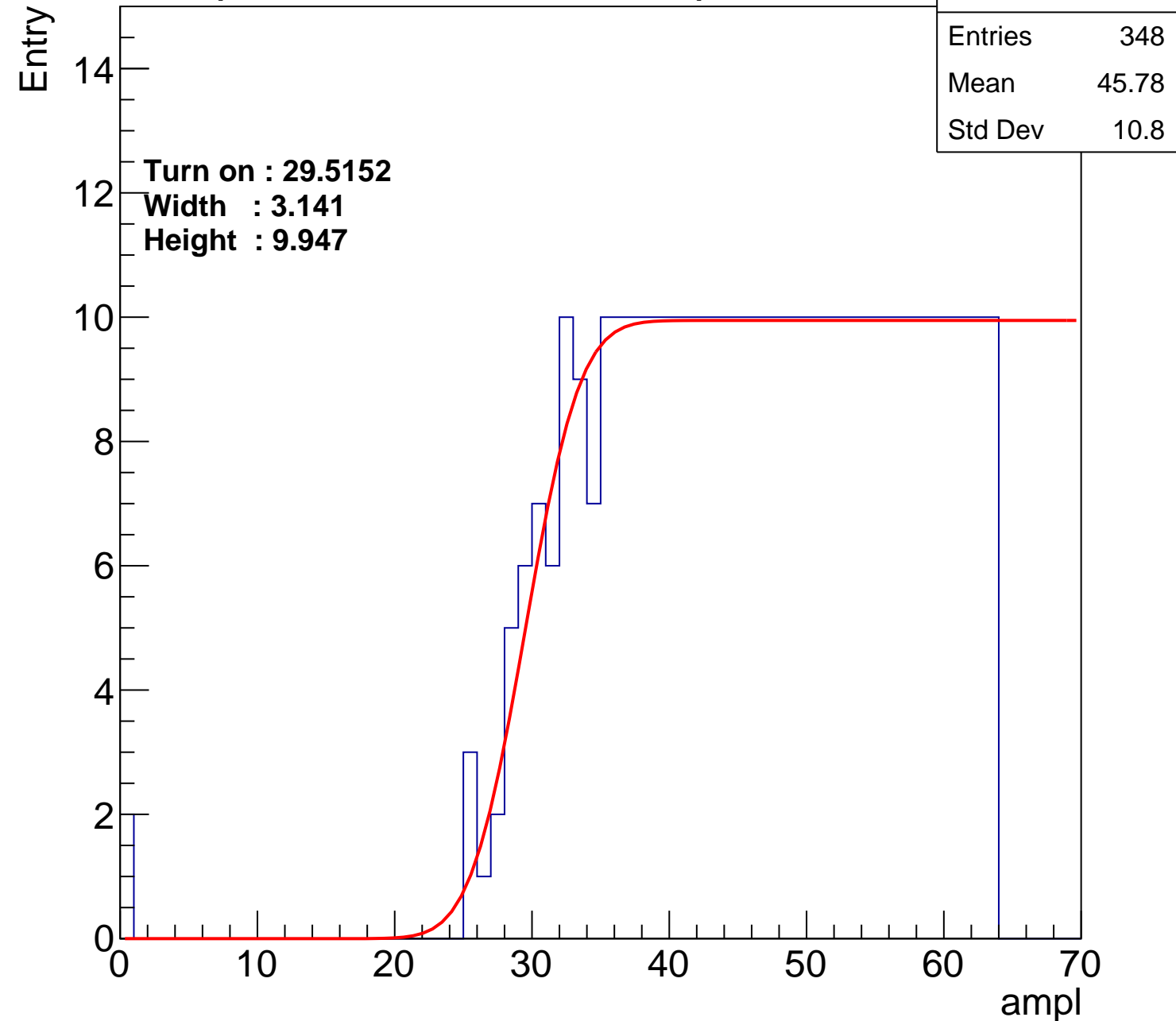
Width : 3.141

Height : 9.947

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch75

calib_packv5_042523_0143.root, FC#9, port A1

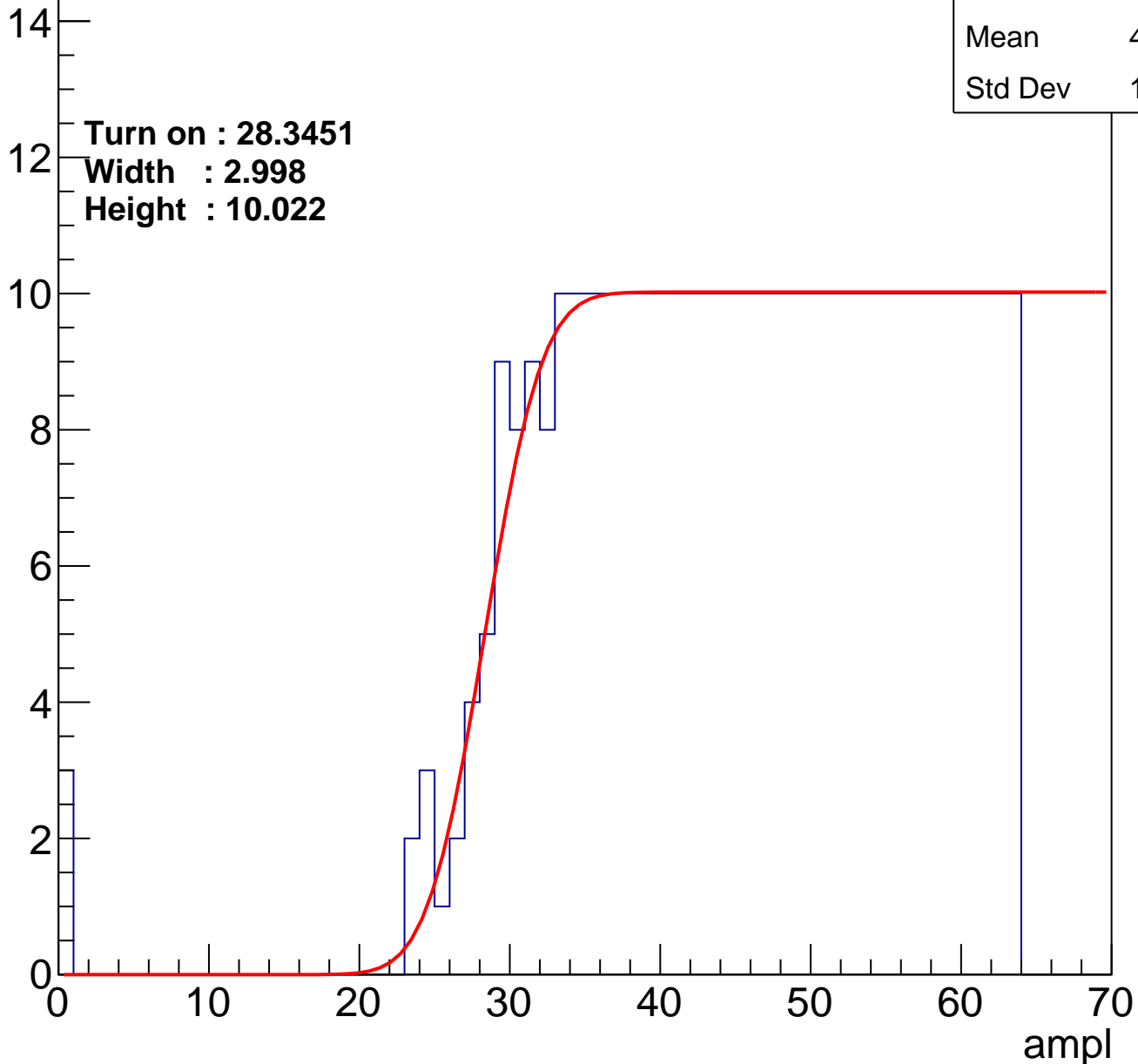
Entries	364
Mean	44.94
Std Dev	11.37

Turn on : 28.3451

Width : 2.998

Height : 10.022

Entry



B0L001S, U3-ch76

calib_packv5_042523_0143.root, FC#9, port A1

Entries	371
Mean	44.8
Std Dev	11.04

Turn on : 27.1522

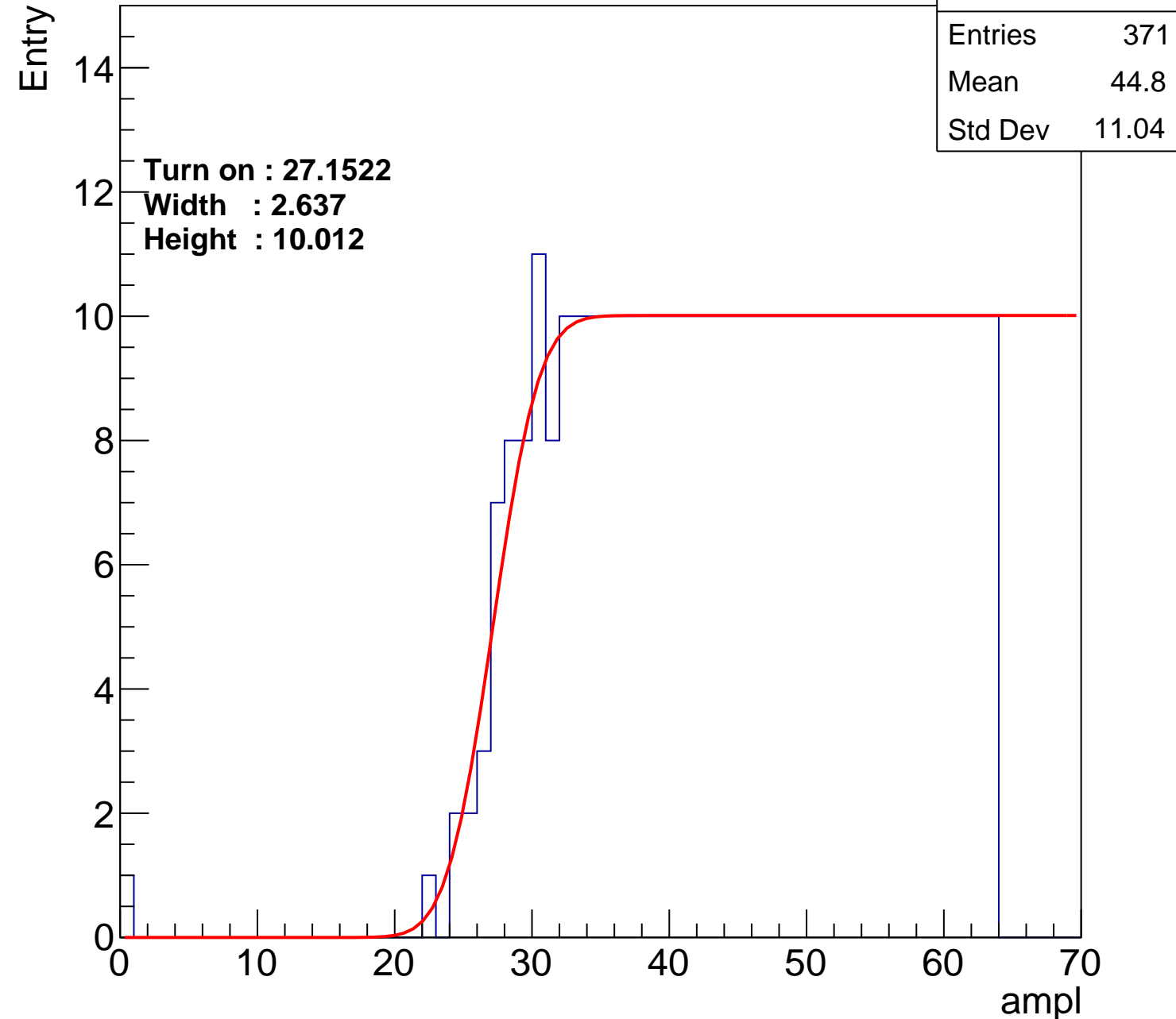
Width : 2.637

Height : 10.012

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch77

calib_packv5_042523_0143.root, FC#9, port A1

Entries	364
Mean	44.96
Std Dev	11.33

Turn on : 27.4658

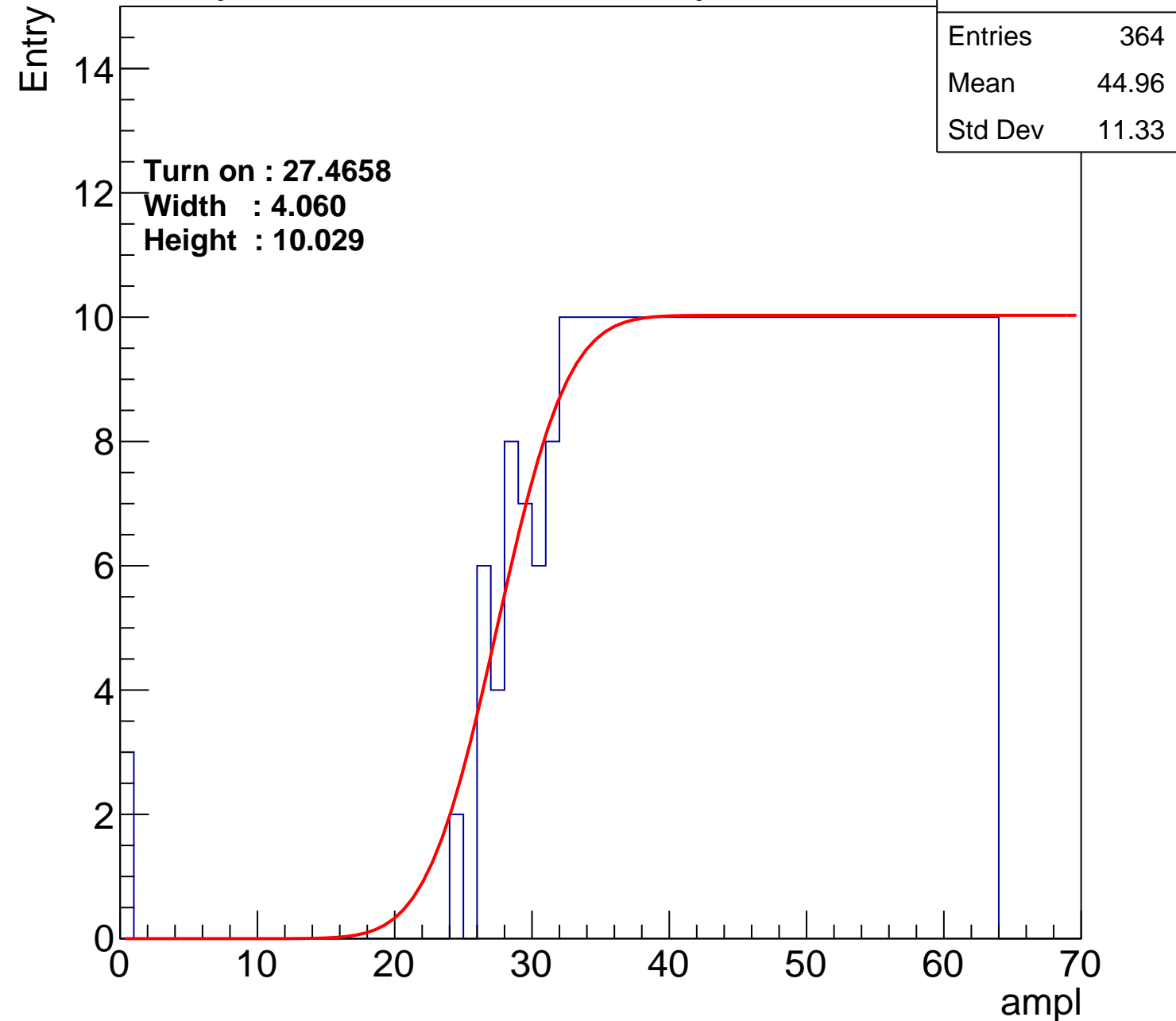
Width : 4.060

Height : 10.029

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch78

calib_packv5_042523_0143.root, FC#9, port A1

Entries	363
Mean	44.91
Std Dev	11.57

Turn on : 28.8458

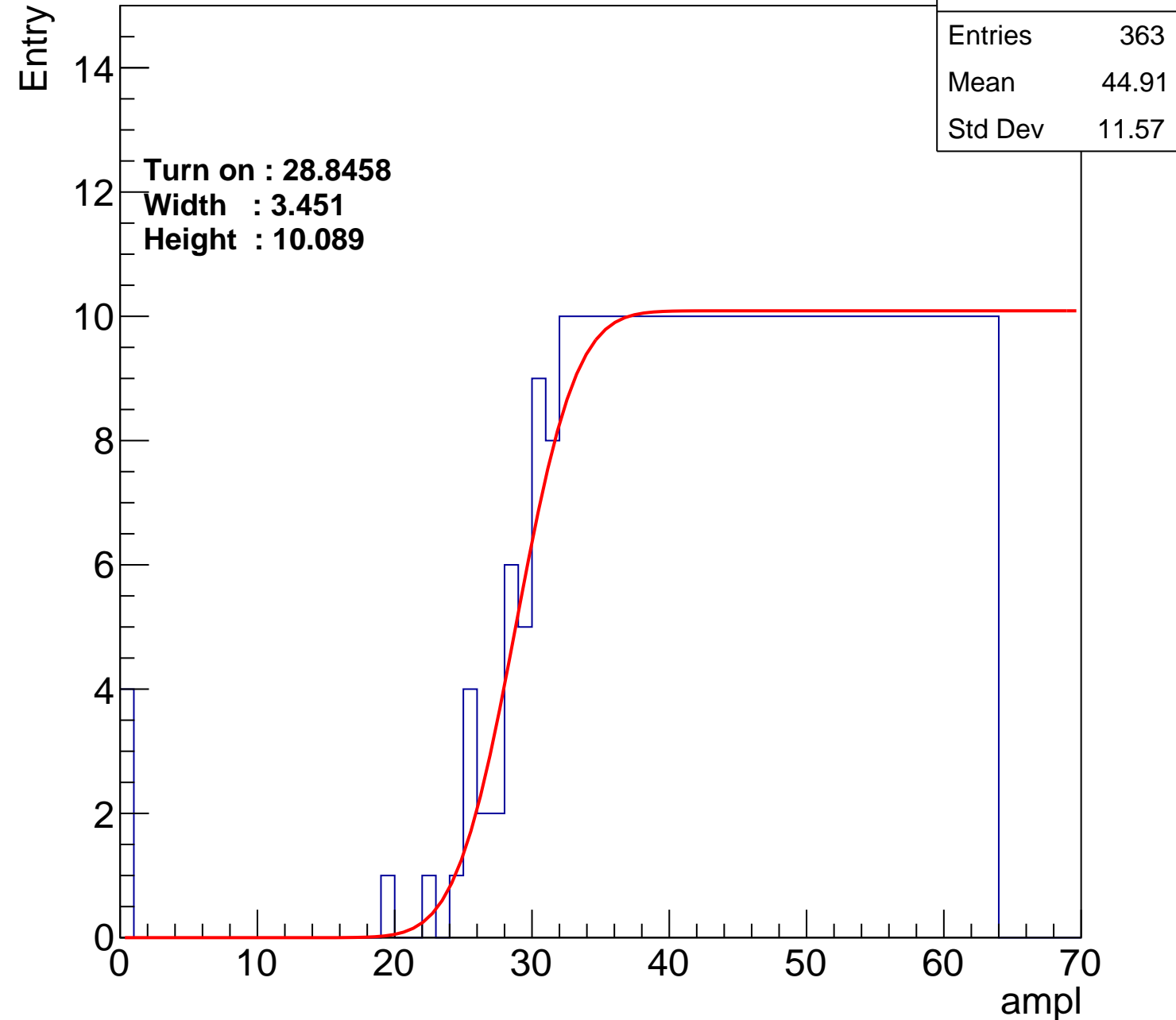
Width : 3.451

Height : 10.089

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch79

calib_packv5_042523_0143.root, FC#9, port A1

Entries	349
Mean	45.81
Std Dev	10.69

Turn on : 28.9602

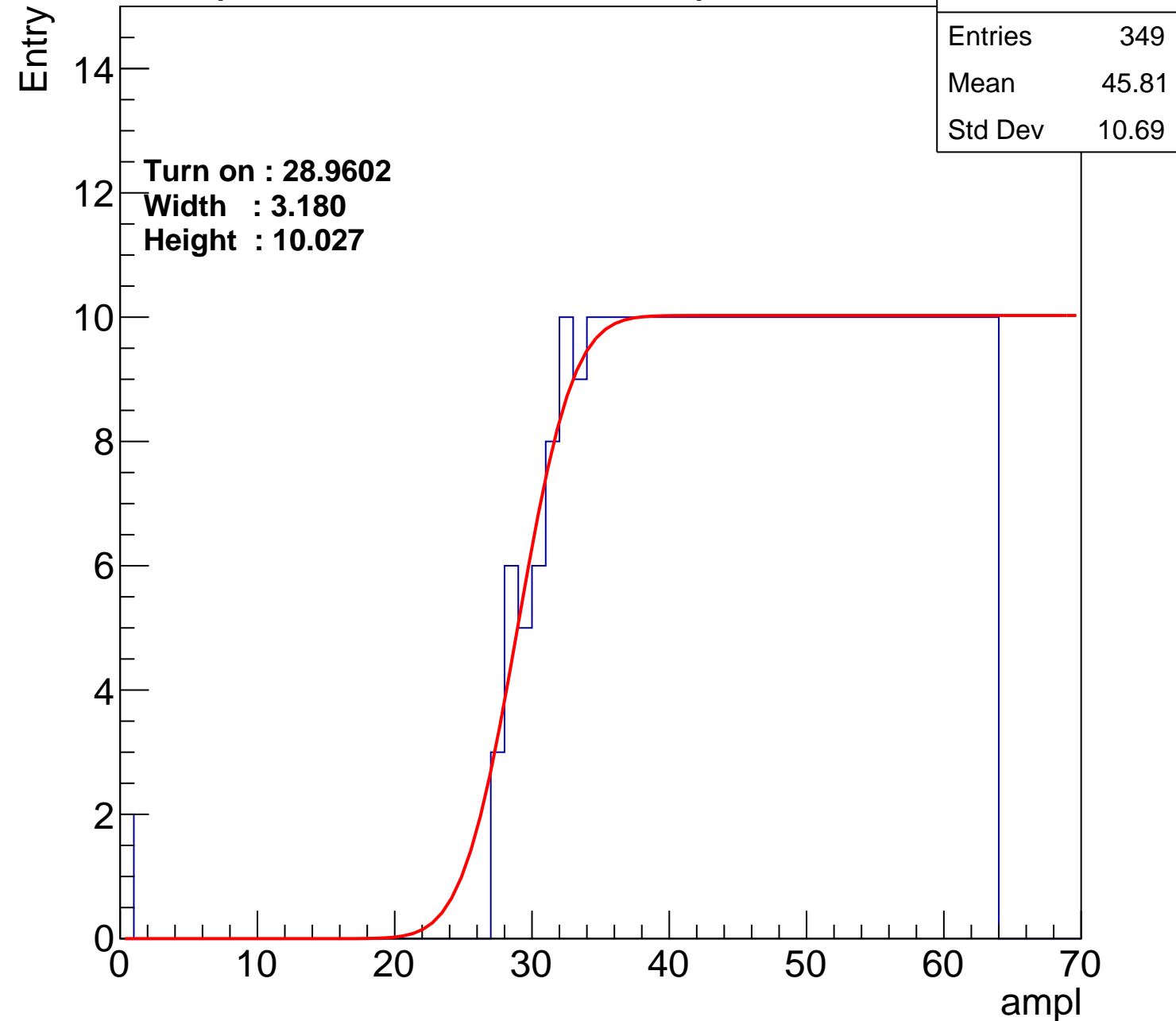
Width : 3.180

Height : 10.027

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch80

calib_packv5_042523_0143.root, FC#9, port A1

Entries	391
Mean	43.66
Std Dev	11.96

Turn on : 25.0840

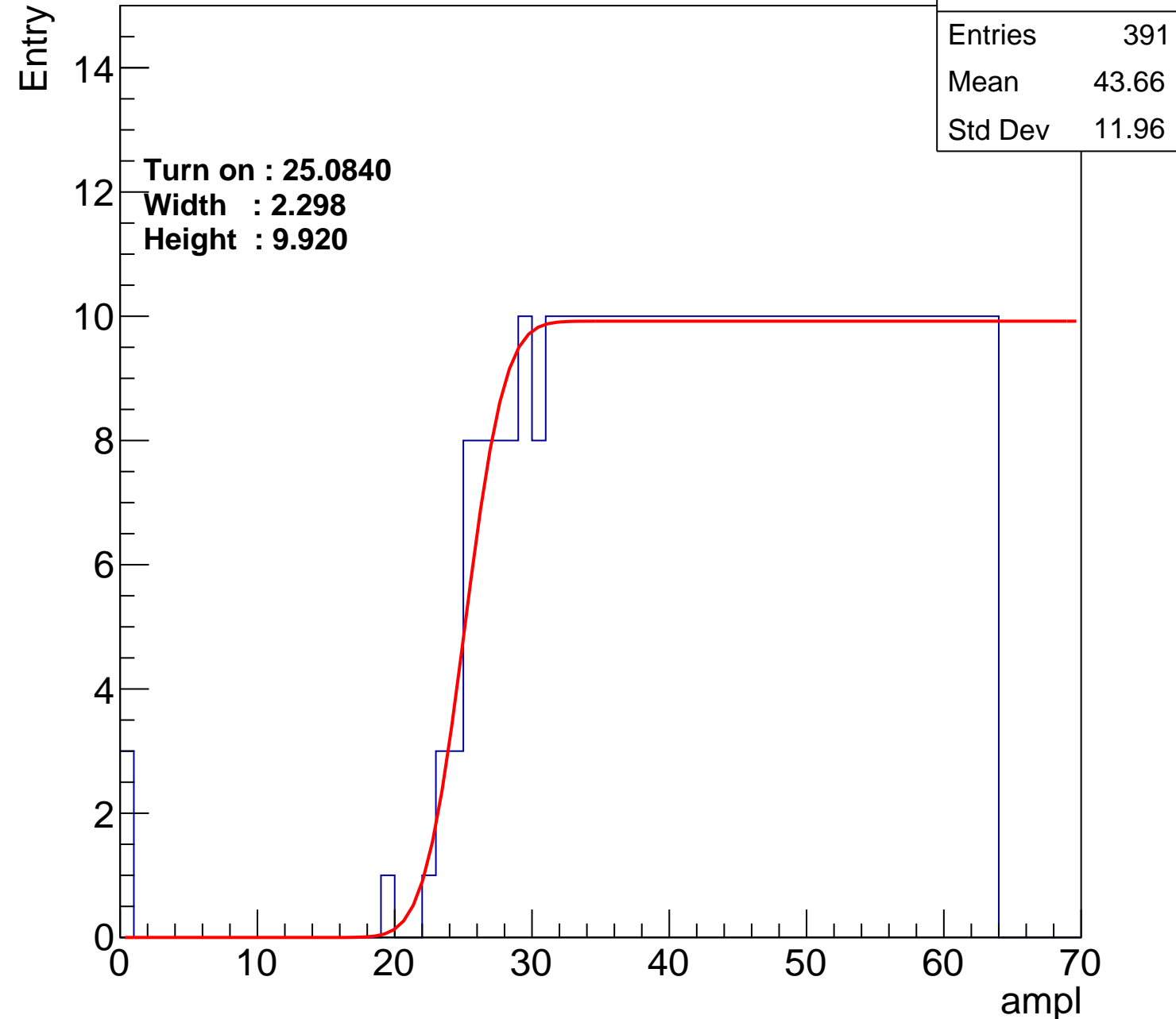
Width : 2.298

Height : 9.920

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch81

calib_packv5_042523_0143.root, FC#9, port A1

Entries	358
Mean	45.32
Std Dev	10.98

Turn on : 28.2348

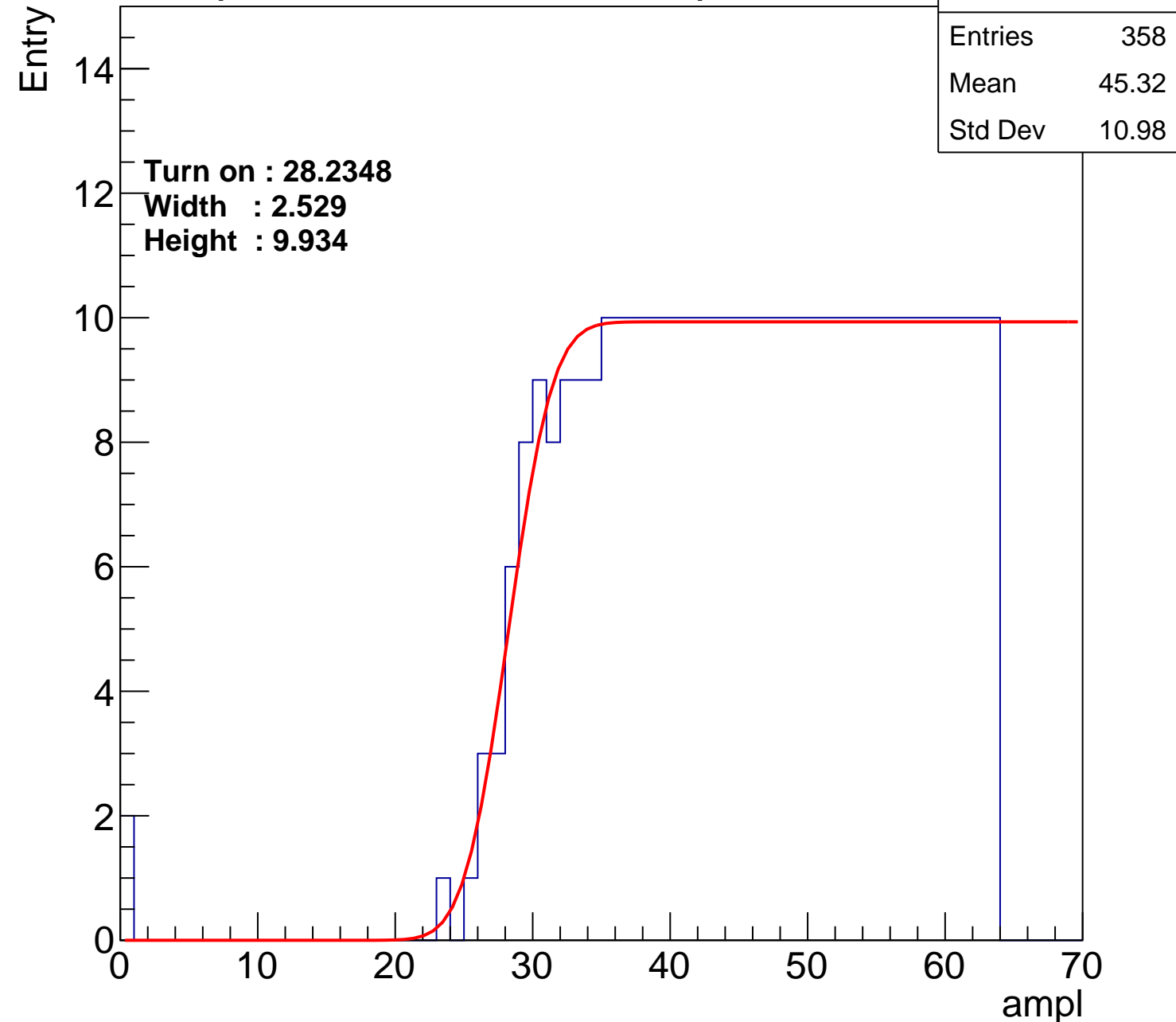
Width : 2.529

Height : 9.934

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch82

calib_packv5_042523_0143.root, FC#9, port A1

Entries	390
Mean	43.42
Std Dev	12.62

Turn on : 25.9136

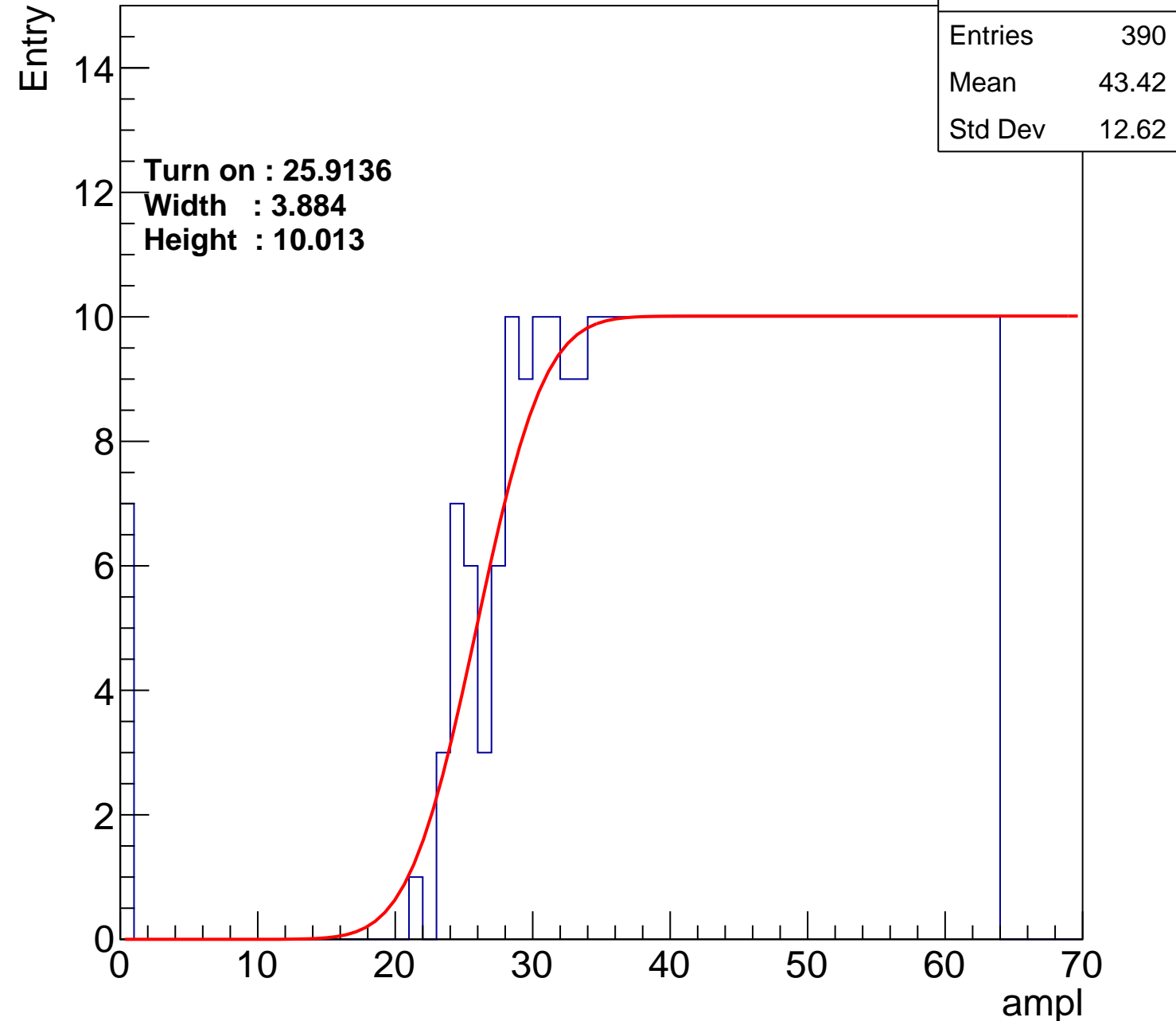
Width : 3.884

Height : 10.013

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch83

calib_packv5_042523_0143.root, FC#9, port A1

Entries	348
Mean	45.45
Std Dev	11.6

Turn on : 30.3112

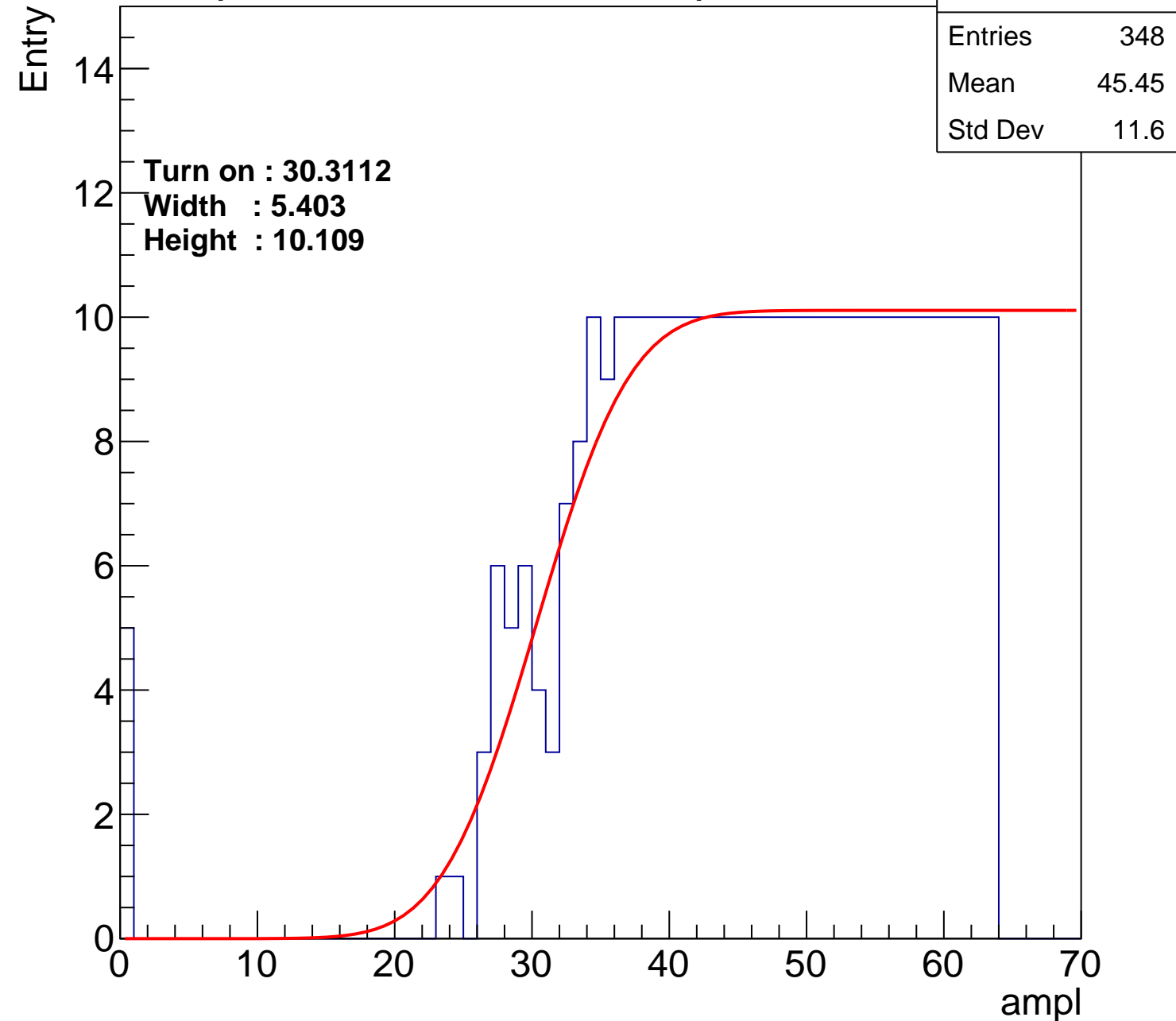
Width : 5.403

Height : 10.109

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch84

calib_packv5_042523_0143.root, FC#9, port A1

Entries	375
Mean	44.29
Std Dev	11.89

Turn on : 27.2999

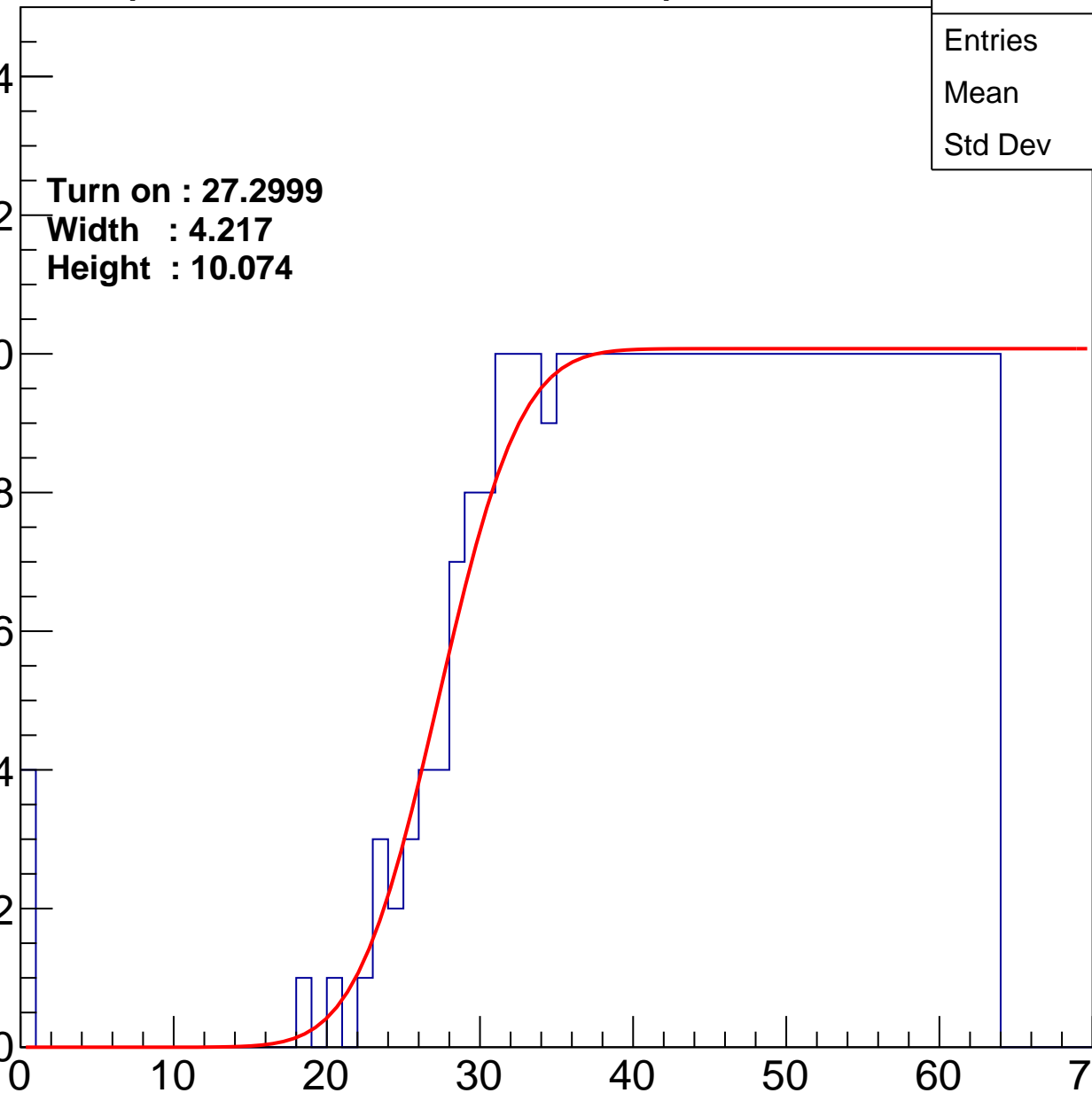
Width : 4.217

Height : 10.074

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch85

calib_packv5_042523_0143.root, FC#9, port A1

Entries	371
Mean	44.5
Std Dev	11.85

Turn on : 28.0155

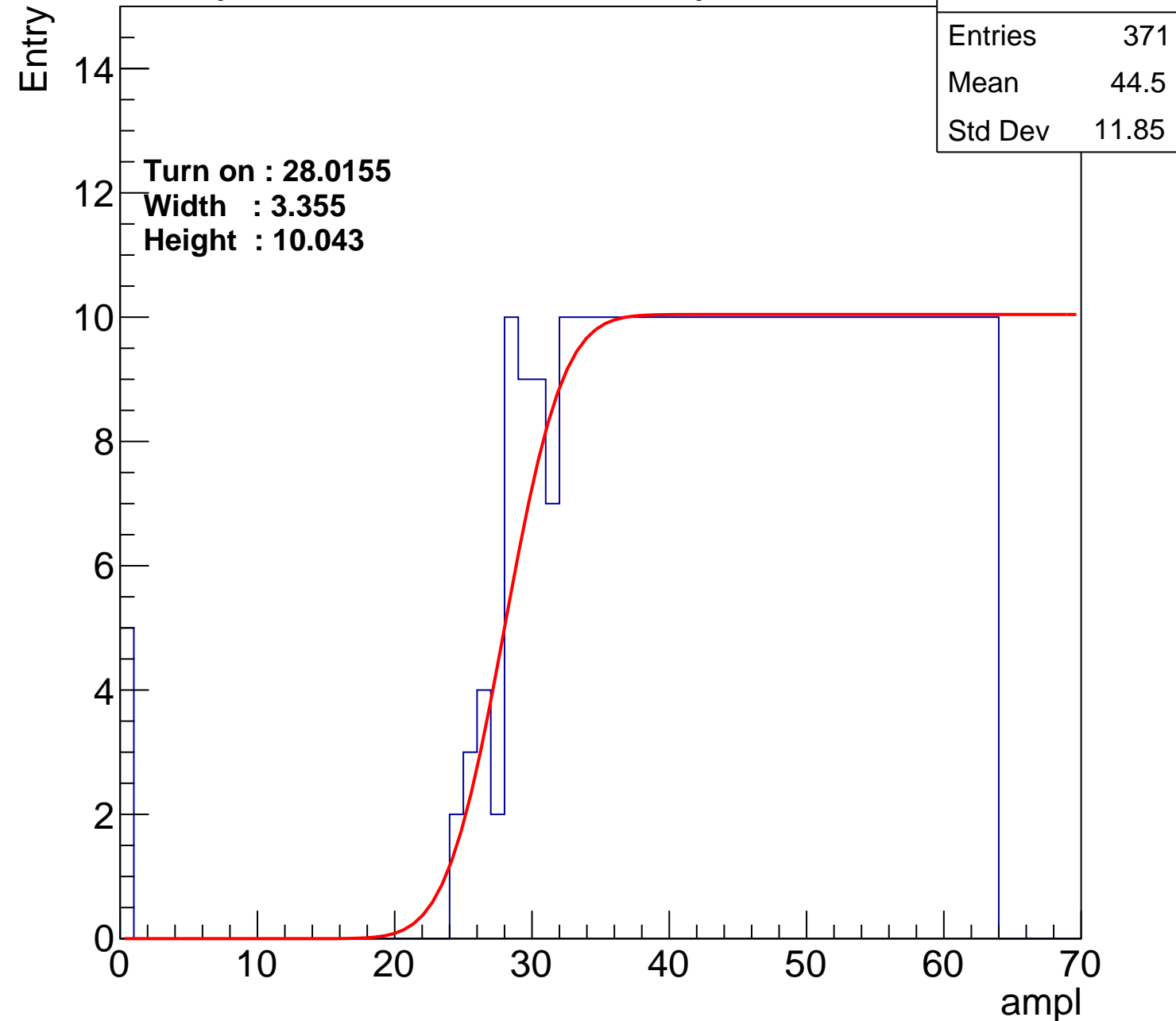
Width : 3.355

Height : 10.043

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch86

calib_packv5_042523_0143.root, FC#9, port A1

Entries	383
Mean	43.93
Std Dev	12.03

Turn on : 26.6640

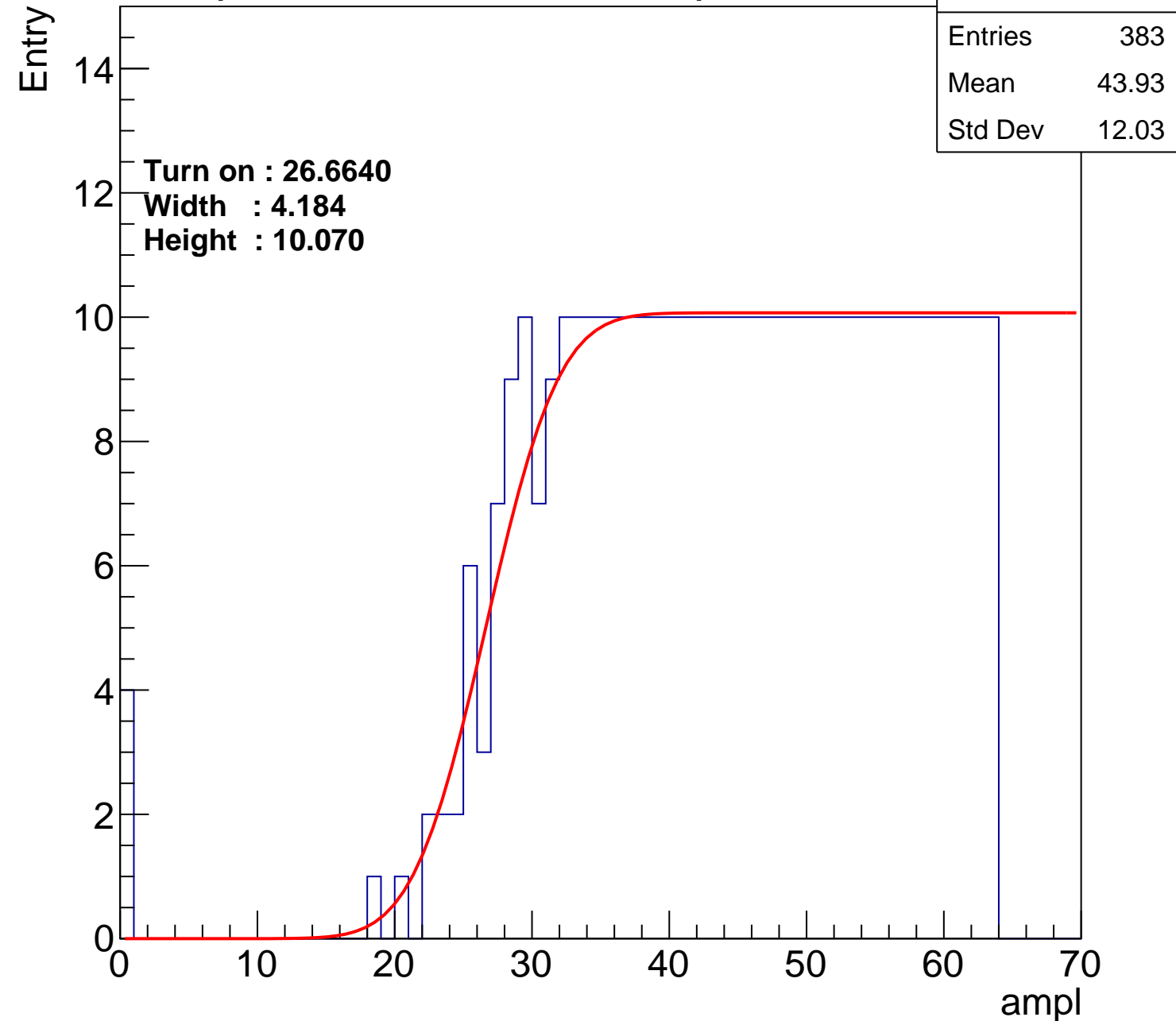
Width : 4.184

Height : 10.070

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch87

calib_packv5_042523_0143.root, FC#9, port A1

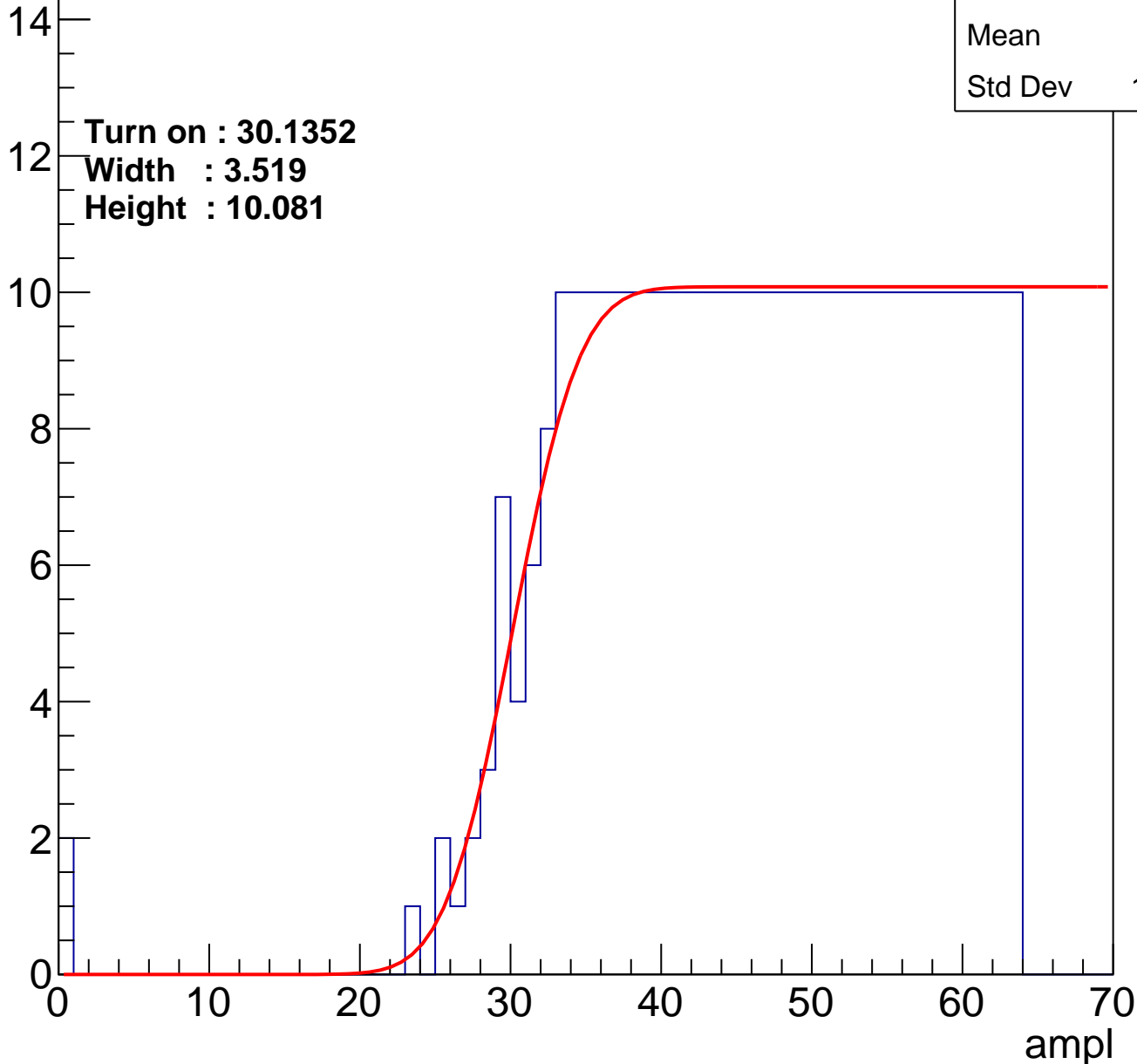
Entries	346
Mean	45.9
Std Dev	10.72

Turn on : 30.1352

Width : 3.519

Height : 10.081

Entry



B0L001S, U3-ch88

calib_packv5_042523_0143.root, FC#9, port A1

Entries	357
Mean	45.22
Std Dev	11.3

Turn on : 28.6399

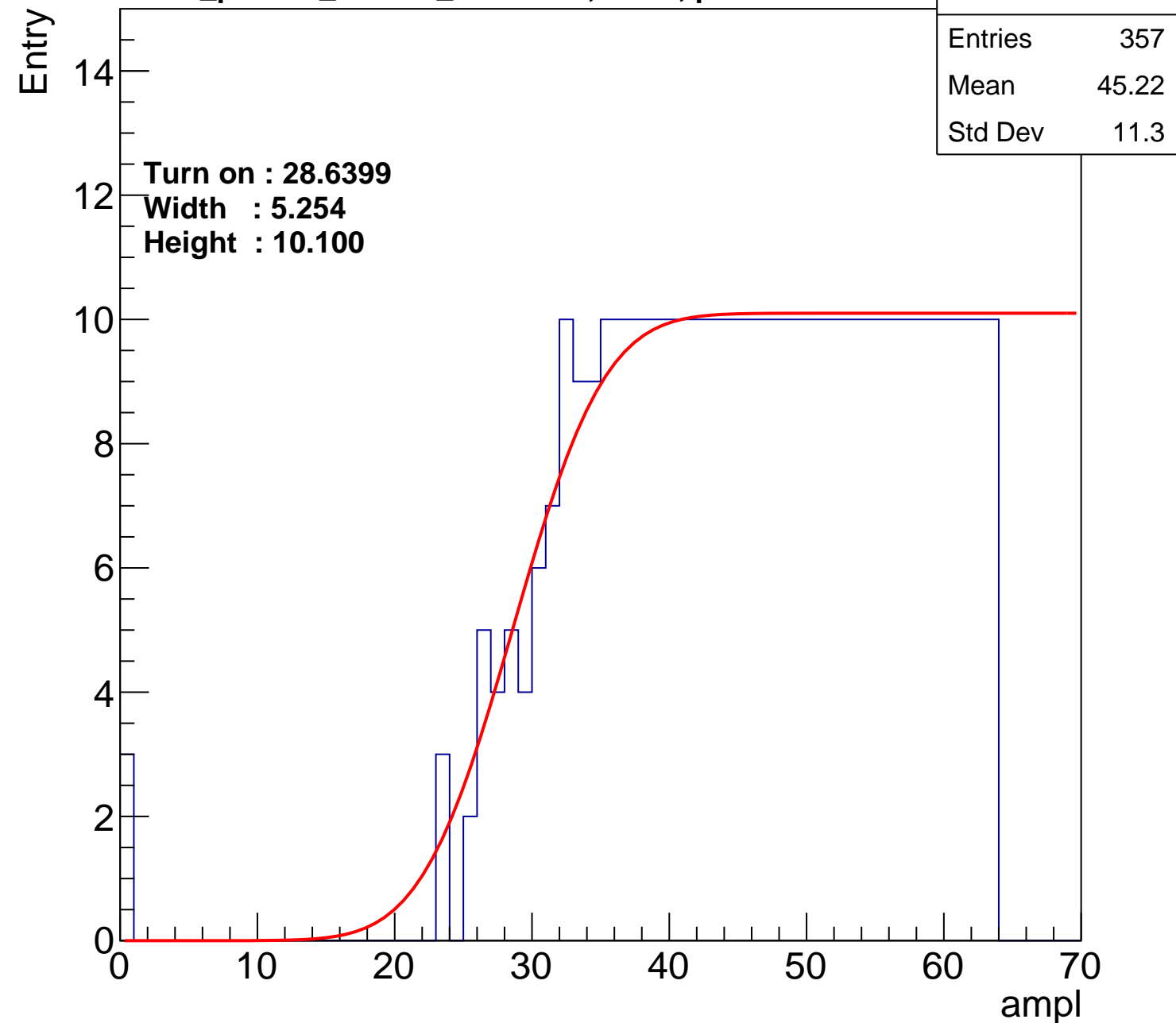
Width : 5.254

Height : 10.100

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch89

calib_packv5_042523_0143.root, FC#9, port A1

Entries	353
Mean	45.63
Std Dev	10.67

Turn on : 29.6433

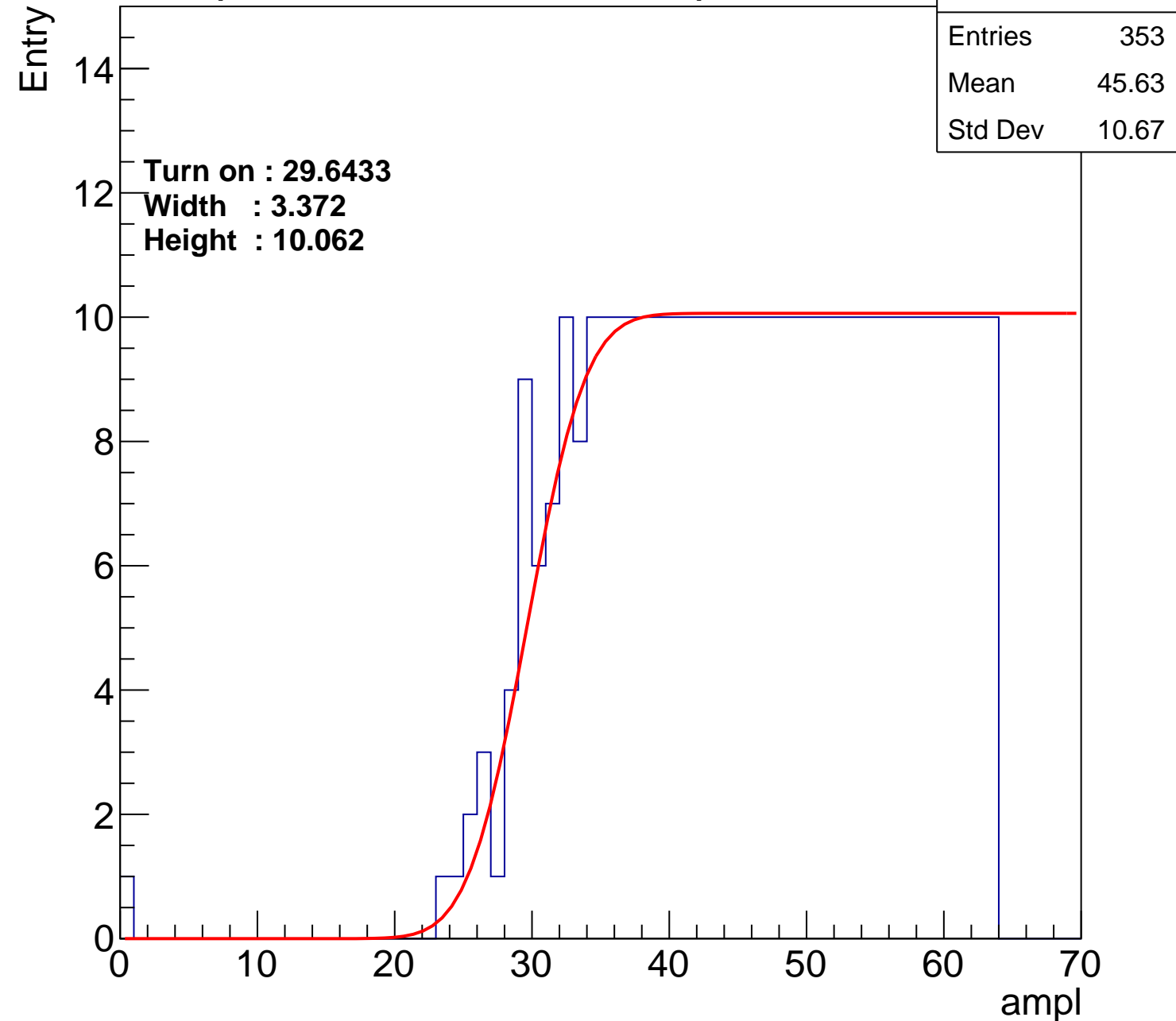
Width : 3.372

Height : 10.062

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch90

calib_packv5_042523_0143.root, FC#9, port A1

Entries	367
Mean	44.6
Std Dev	11.98

Turn on : 27.8186

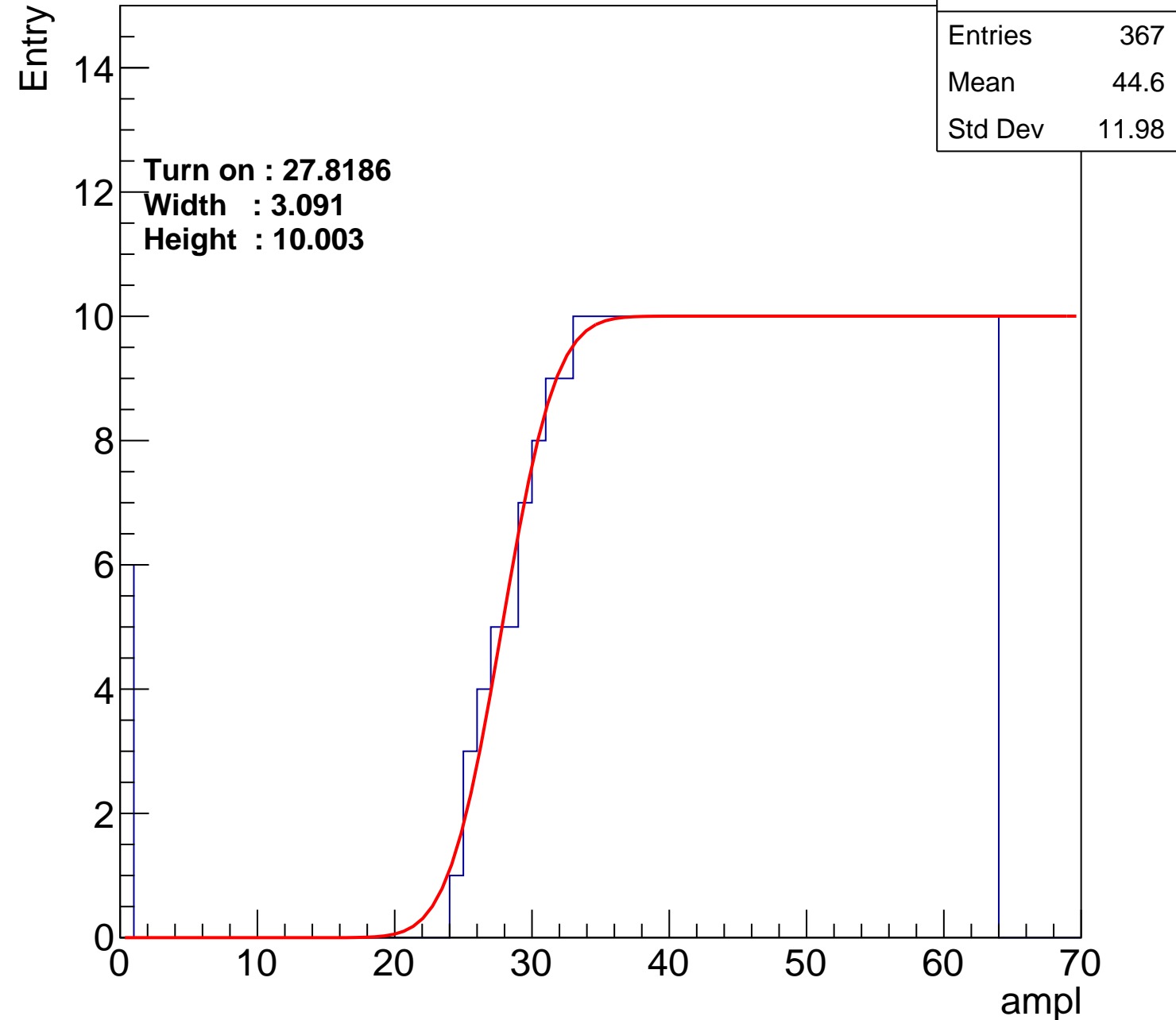
Width : 3.091

Height : 10.003

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch91

calib_packv5_042523_0143.root, FC#9, port A1

Entries	363
Mean	44.91
Std Dev	11.55

Turn on : 28.4852

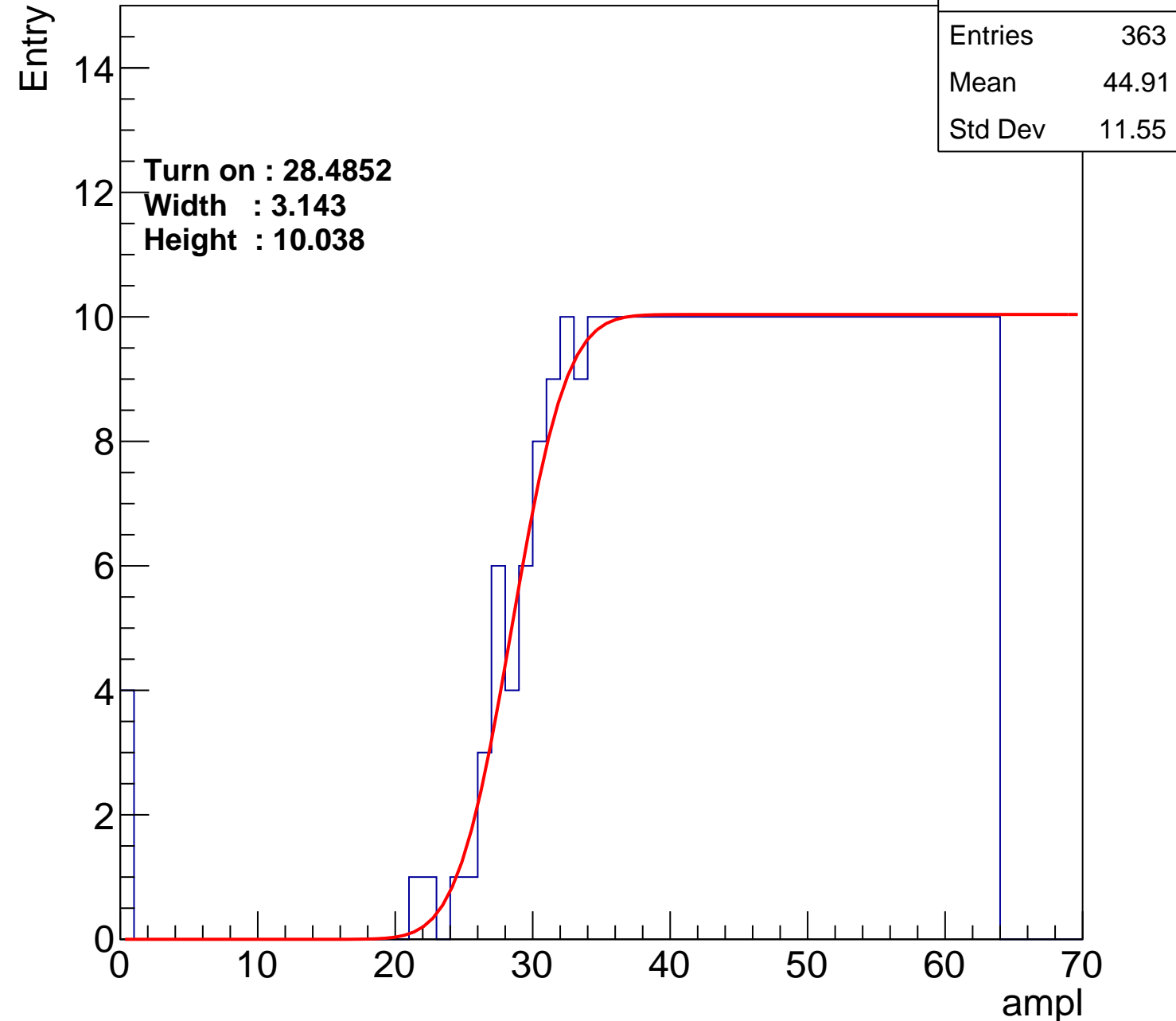
Width : 3.143

Height : 10.038

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch92

calib_packv5_042523_0143.root, FC#9, port A1

Entries	372
Mean	44.57
Std Dev	11.52

Turn on : 26.9760

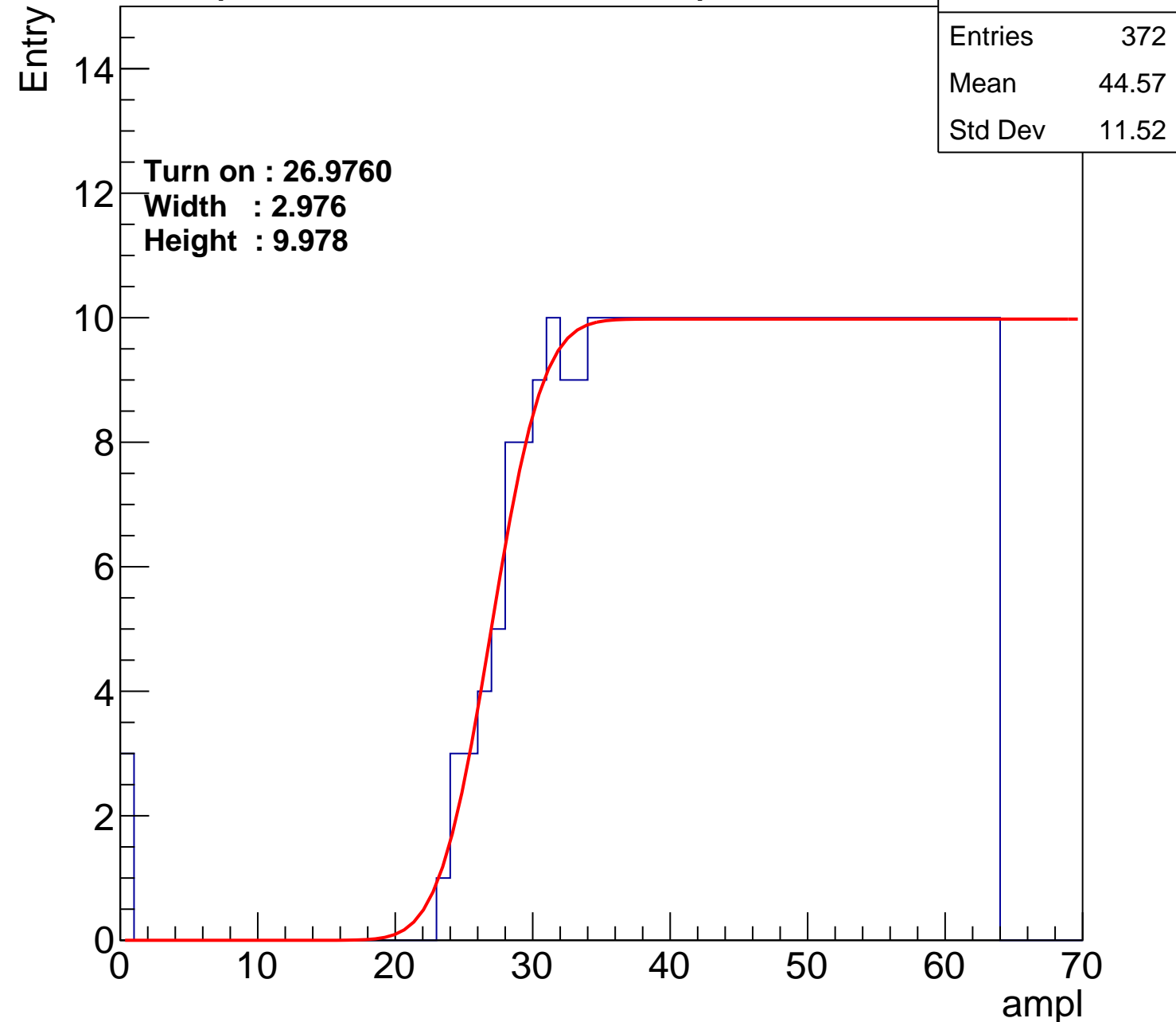
Width : 2.976

Height : 9.978

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch93

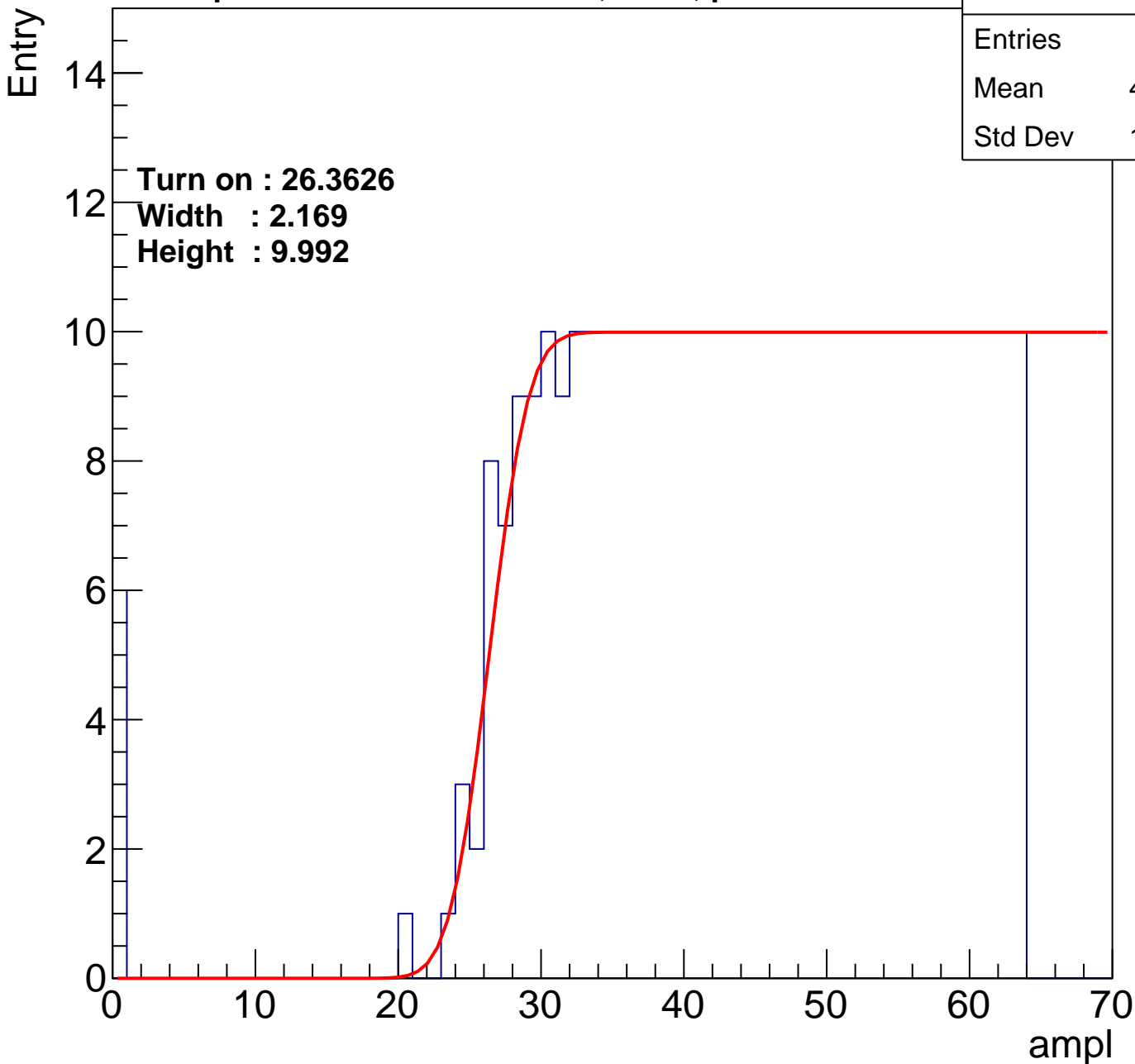
calib_packv5_042523_0143.root, FC#9, port A1

Entries	385
Mean	43.78
Std Dev	12.29

Turn on : 26.3626

Width : 2.169

Height : 9.992



B0L001S, U3-ch94

calib_packv5_042523_0143.root, FC#9, port A1

Entries	373
Mean	44.3
Std Dev	12.12

Turn on : 27.4329

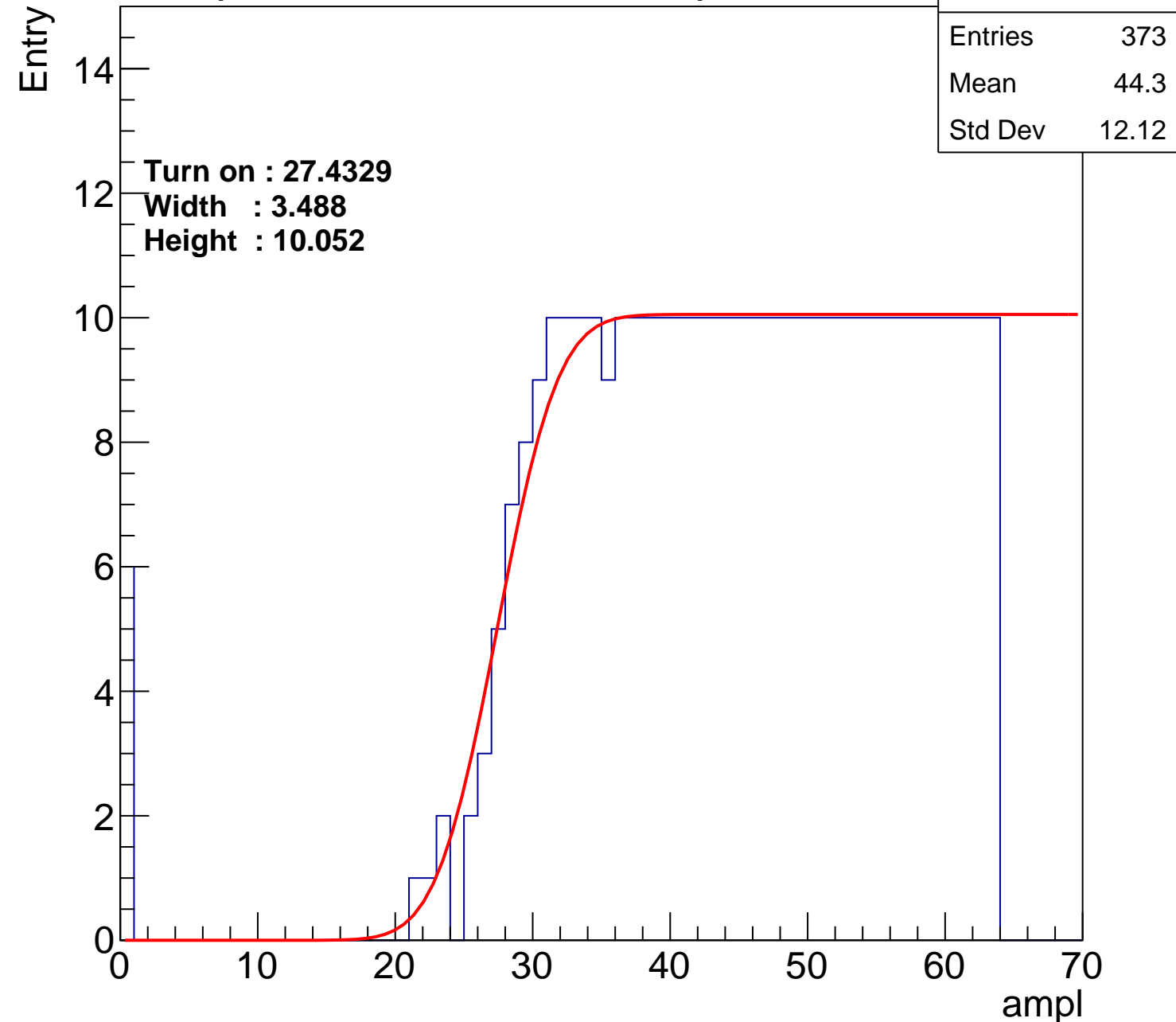
Width : 3.488

Height : 10.052

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch95

calib_packv5_042523_0143.root, FC#9, port A1

Entries	377
Mean	44.38
Std Dev	11.57

Turn on : 26.7626

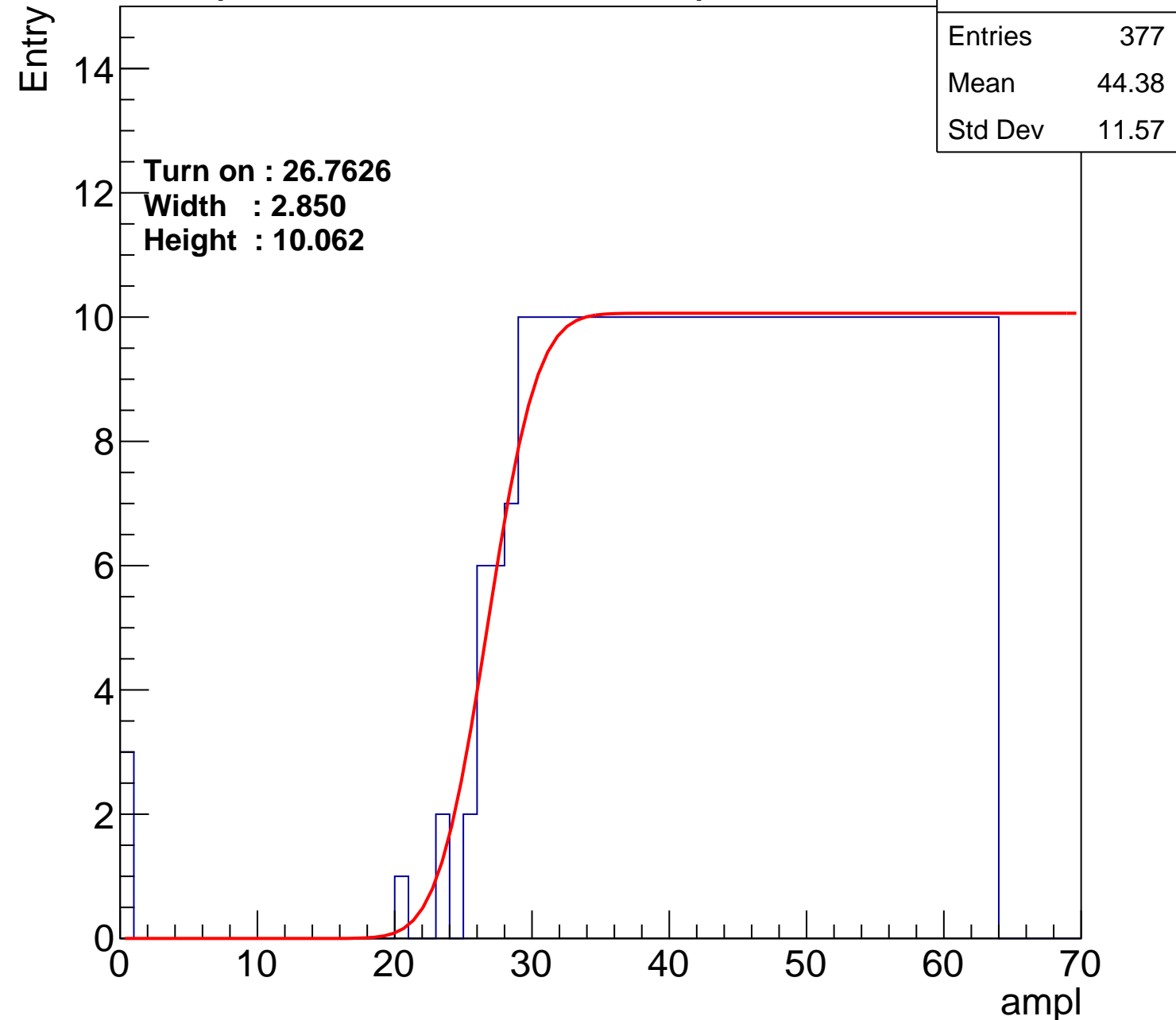
Width : 2.850

Height : 10.062

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch96

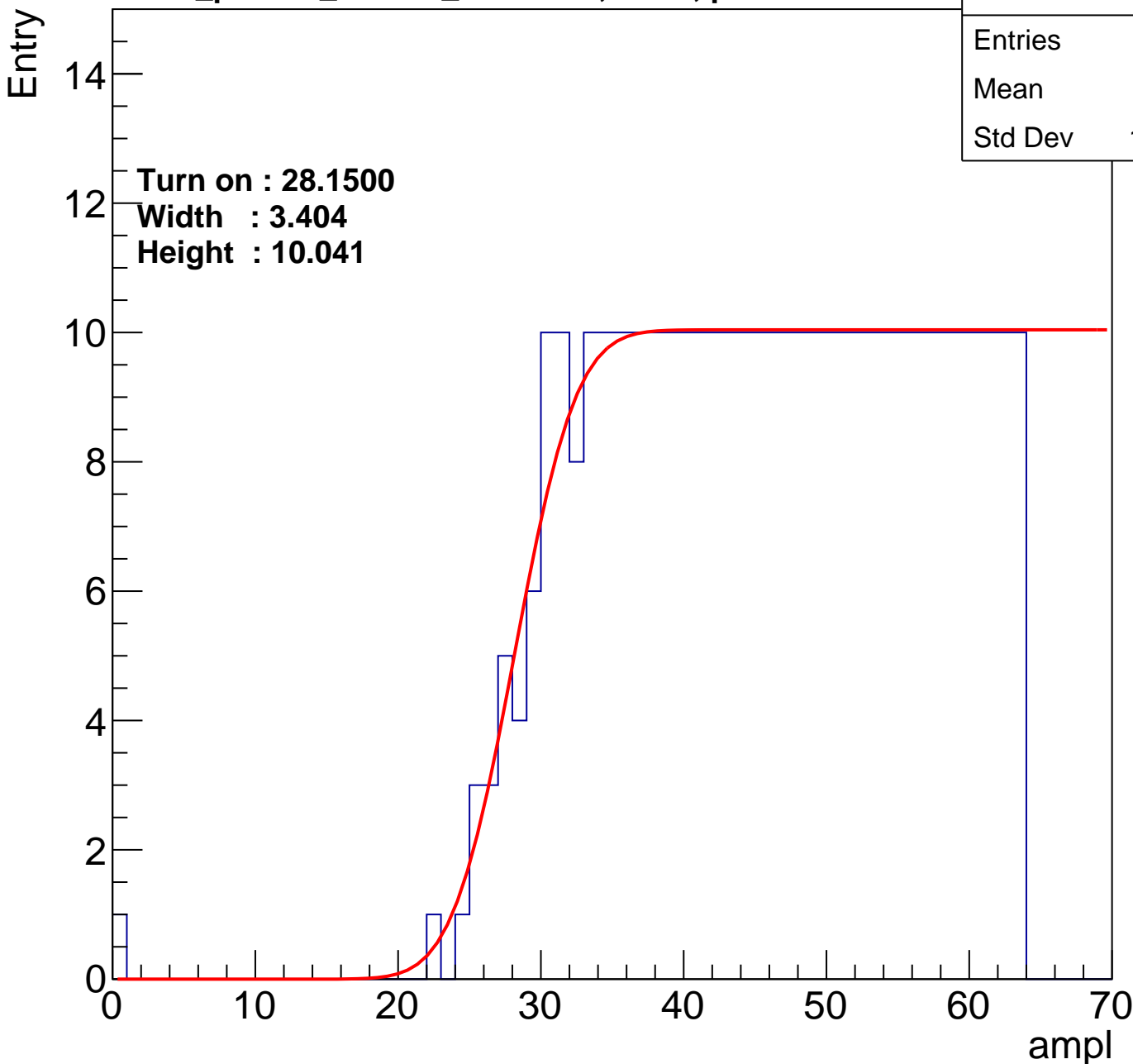
calib_packv5_042523_0143.root, FC#9, port A1

Entries	362
Mean	45.21
Std Dev	10.86

Turn on : 28.1500

Width : 3.404

Height : 10.041



B0L001S, U3-ch97

calib_packv5_042523_0143.root, FC#9, port A1

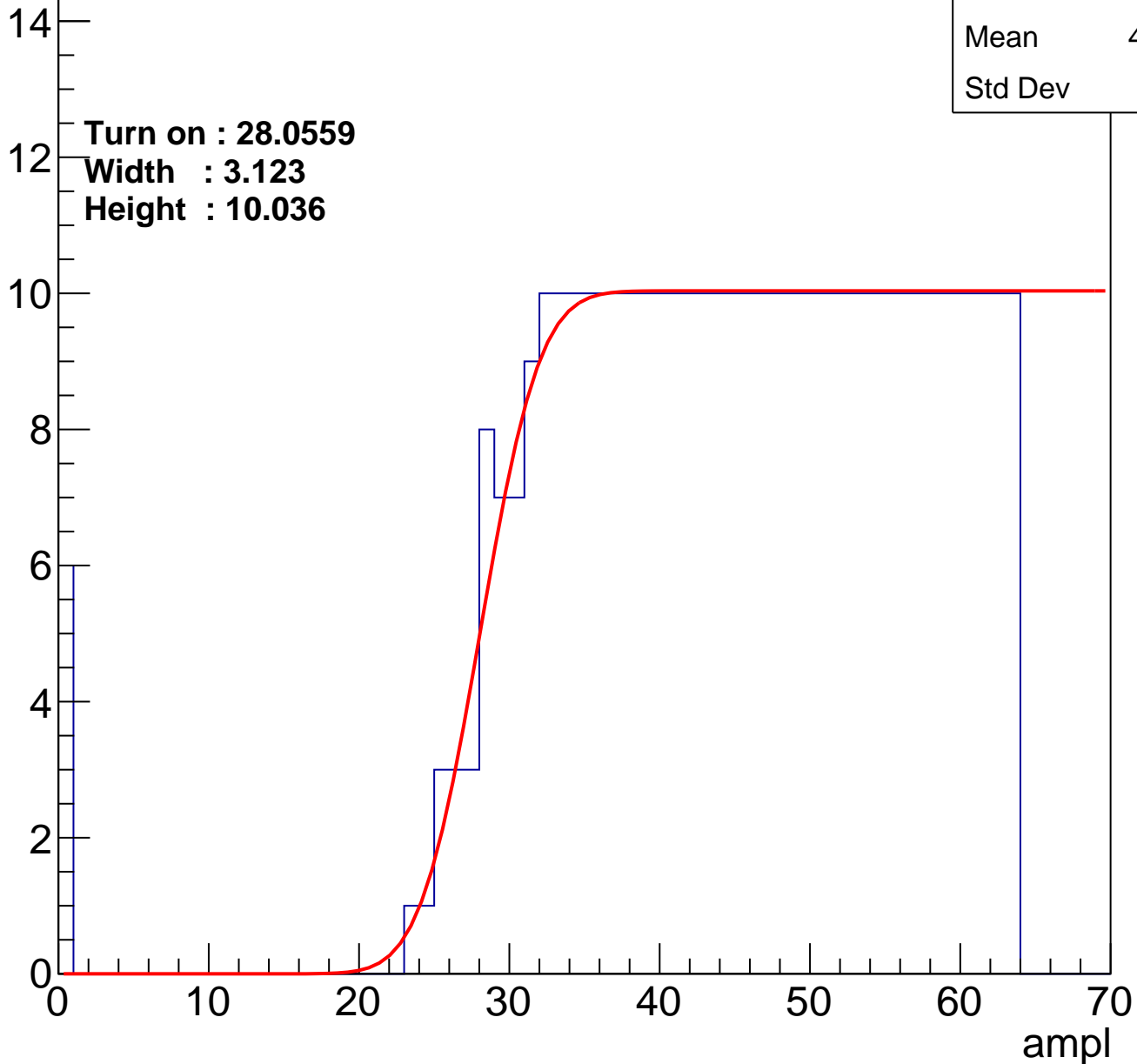
Entries	368
Mean	44.56
Std Dev	12

Turn on : 28.0559

Width : 3.123

Height : 10.036

Entry



B0L001S, U3-ch98

calib_packv5_042523_0143.root, FC#9, port A1

Entries	372
Mean	44.42
Std Dev	11.84

Turn on : 27.4457

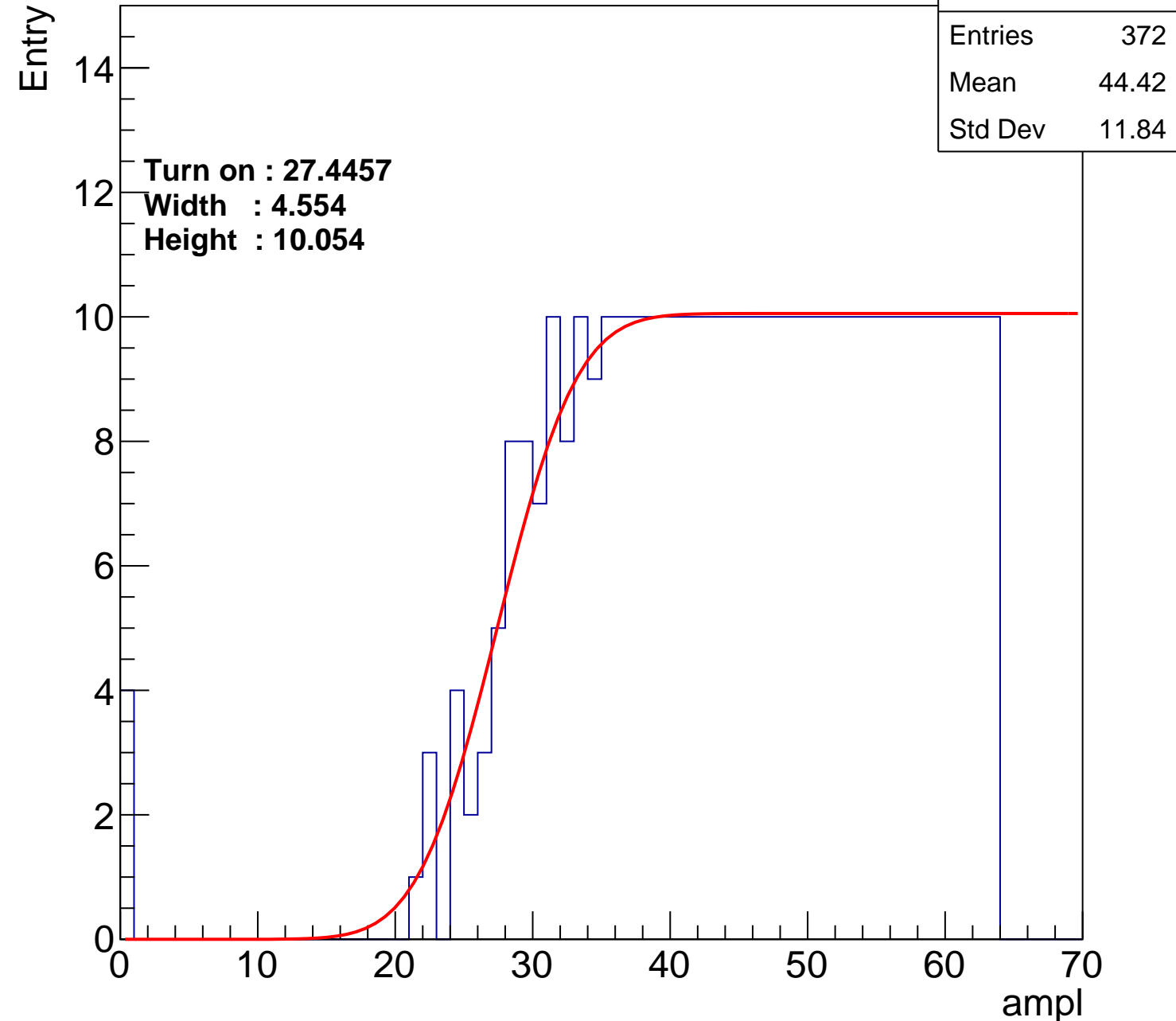
Width : 4.554

Height : 10.054

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch99

calib_packv5_042523_0143.root, FC#9, port A1

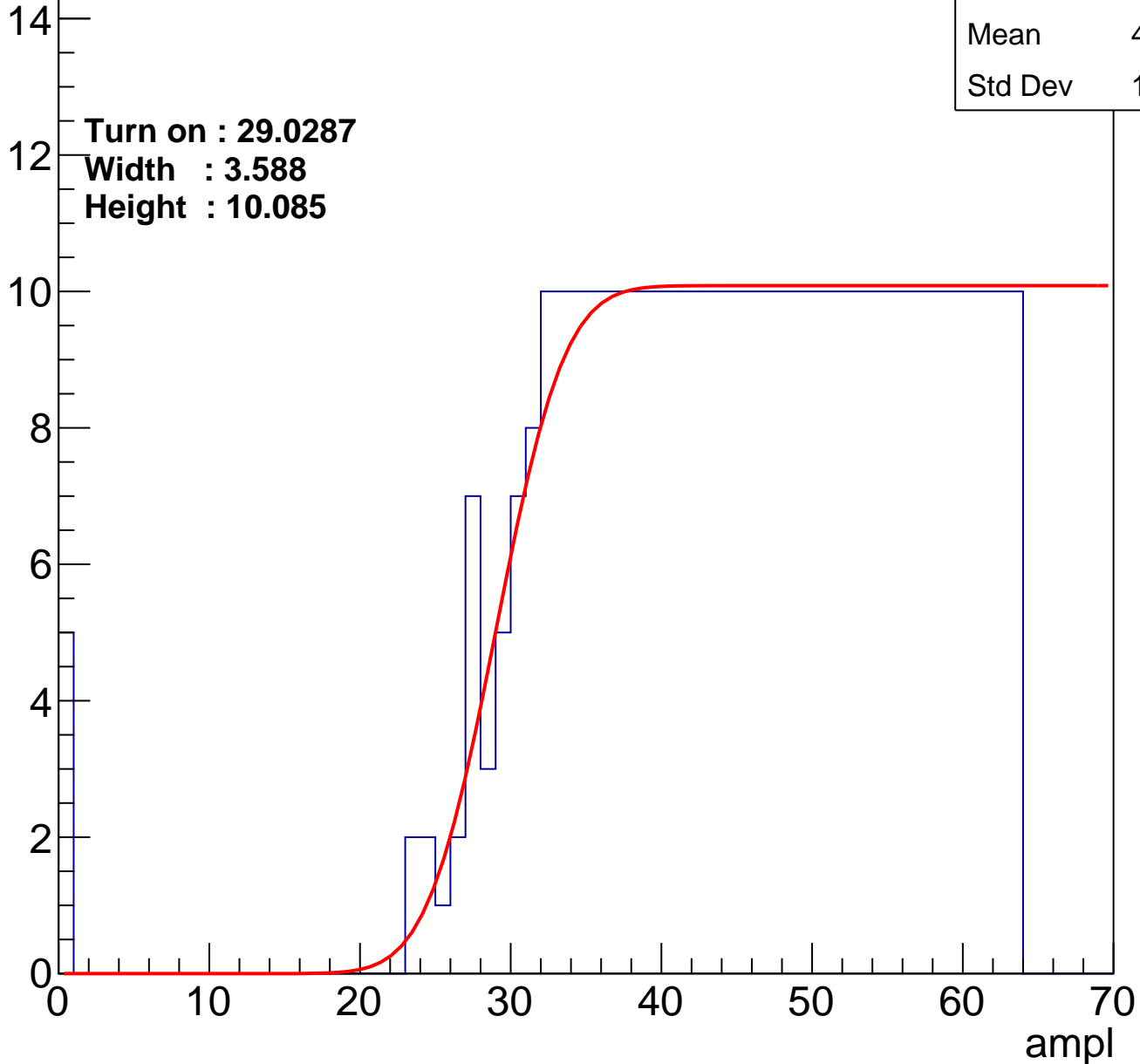
Entry

Entries	362
Mean	44.88
Std Dev	11.74

Turn on : 29.0287

Width : 3.588

Height : 10.085



B0L001S, U3-ch100

calib_packv5_042523_0143.root, FC#9, port A1

Entries	367
Mean	44.88
Std Dev	11.21

Turn on : 27.4498

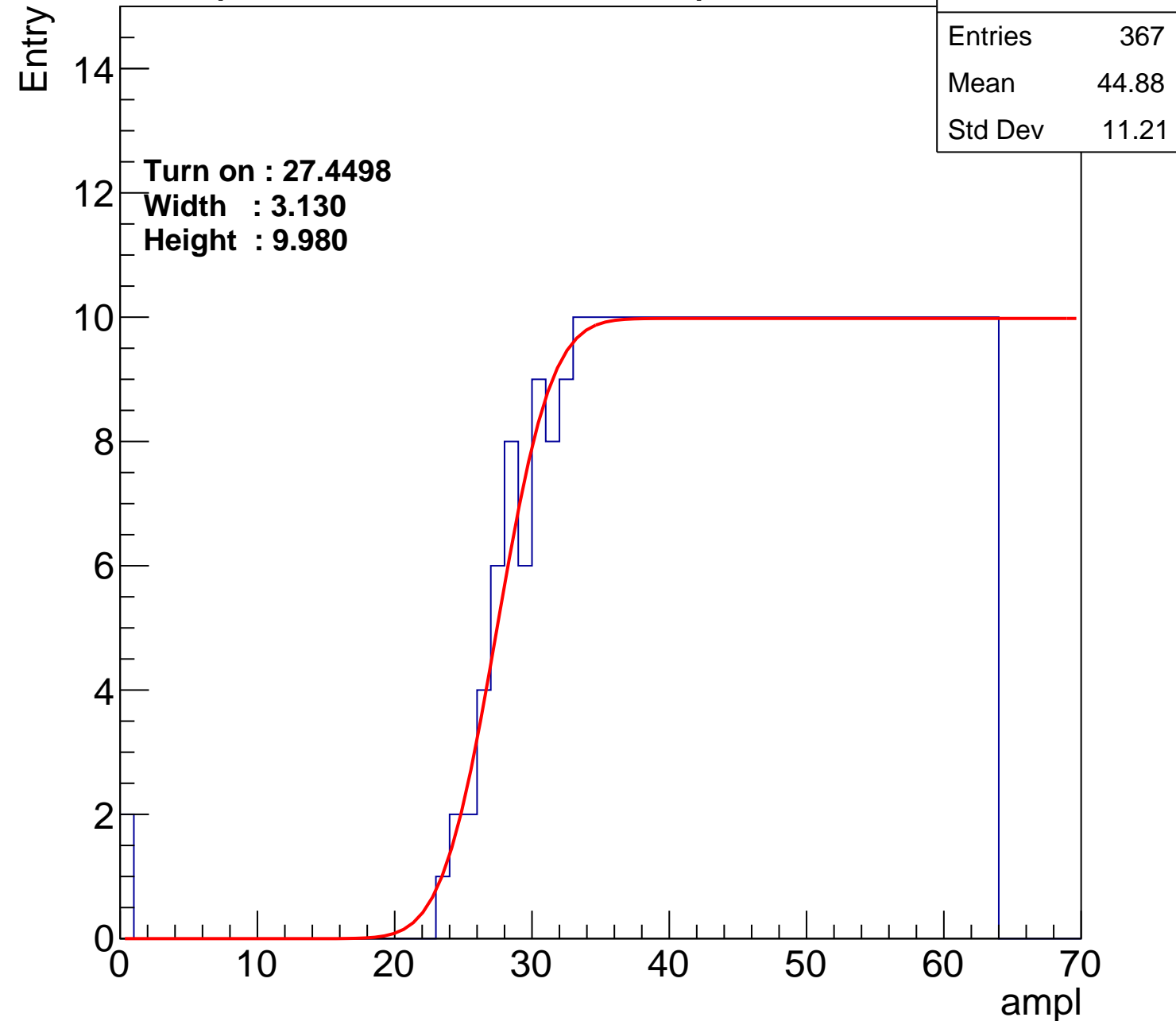
Width : 3.130

Height : 9.980

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch101

calib_packv5_042523_0143.root, FC#9, port A1

Entries	365
Mean	44.69
Std Dev	11.96

Turn on : 28.6419

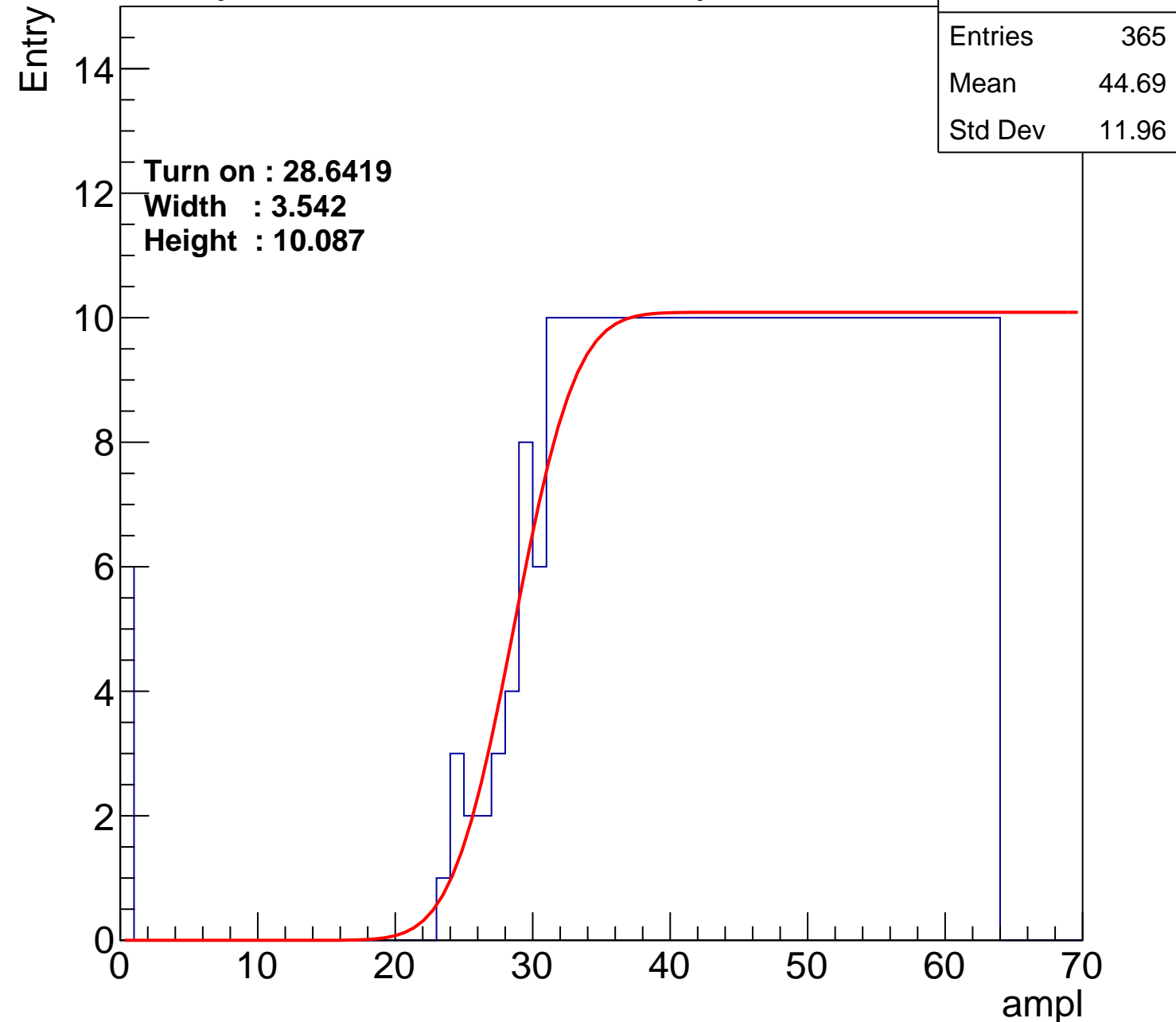
Width : 3.542

Height : 10.087

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch102

calib_packv5_042523_0143.root, FC#9, port A1

Entries	362
Mean	45.21
Std Dev	10.87

Turn on : 28.2074

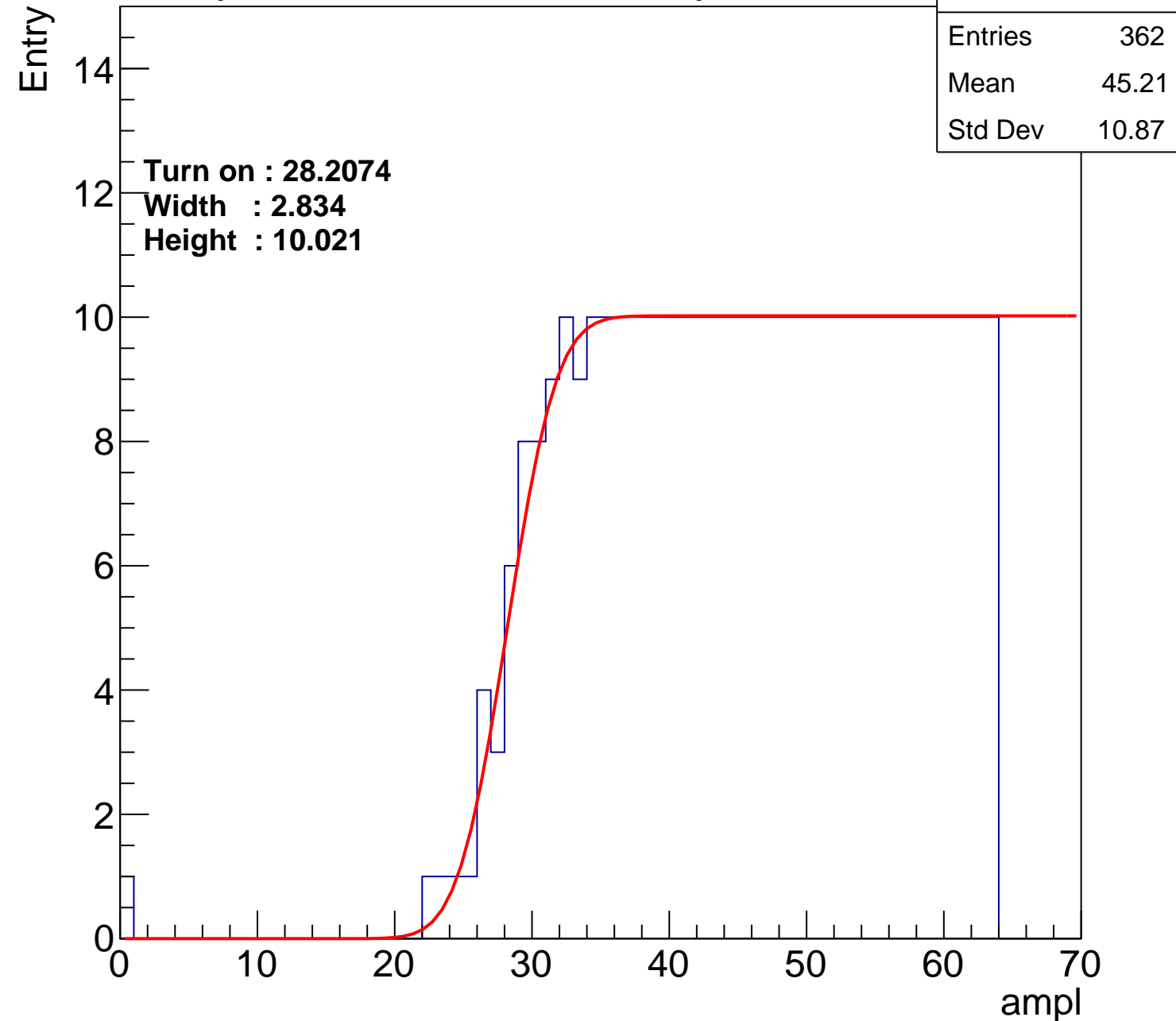
Width : 2.834

Height : 10.021

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch103

calib_packv5_042523_0143.root, FC#9, port A1

Entries	380
Mean	44.08
Std Dev	11.95

Turn on : 26.9506

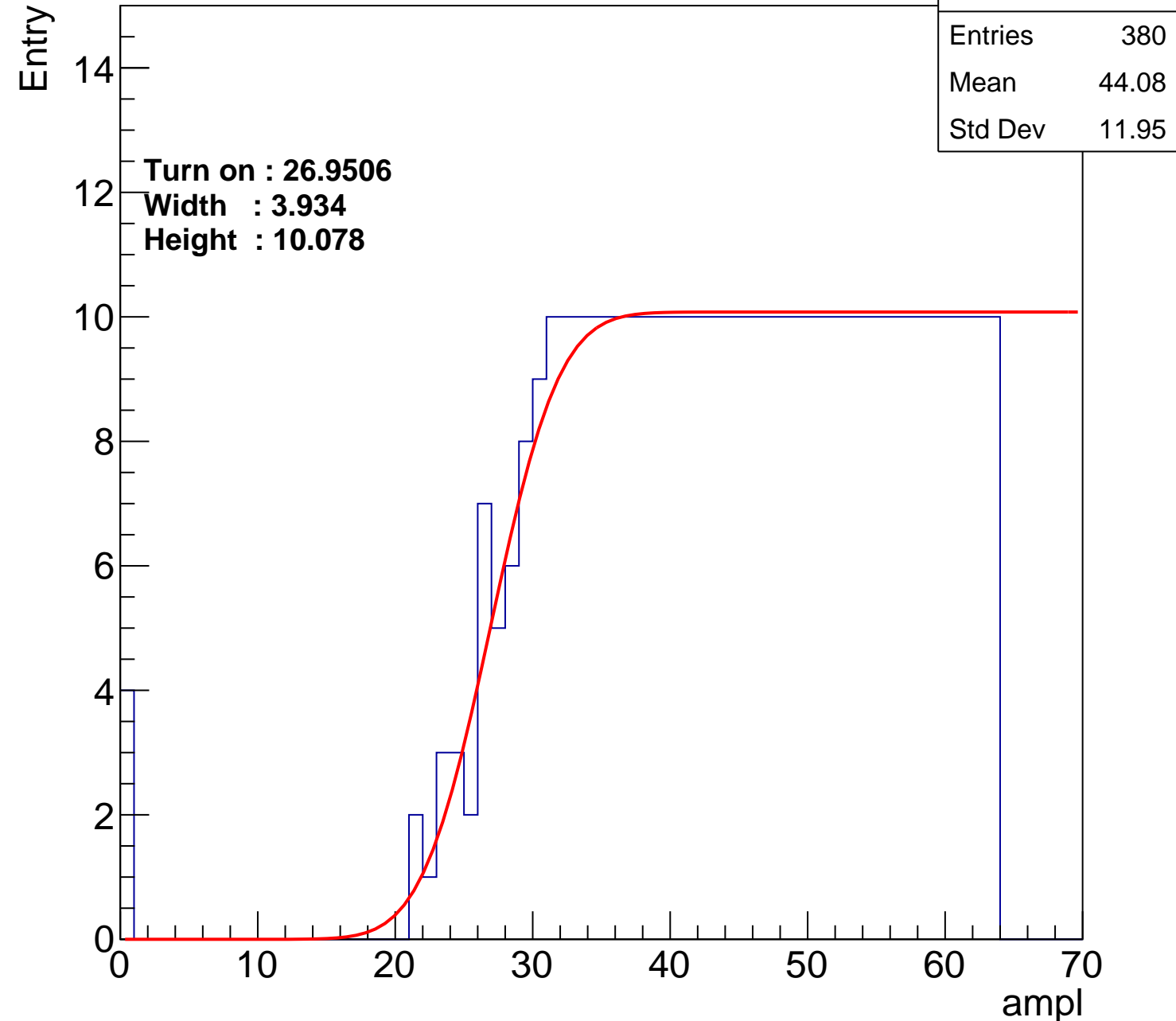
Width : 3.934

Height : 10.078

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch104

calib_packv5_042523_0143.root, FC#9, port A1

Entries	351
Mean	45.44
Std Dev	11.38

Turn on : 29.8369

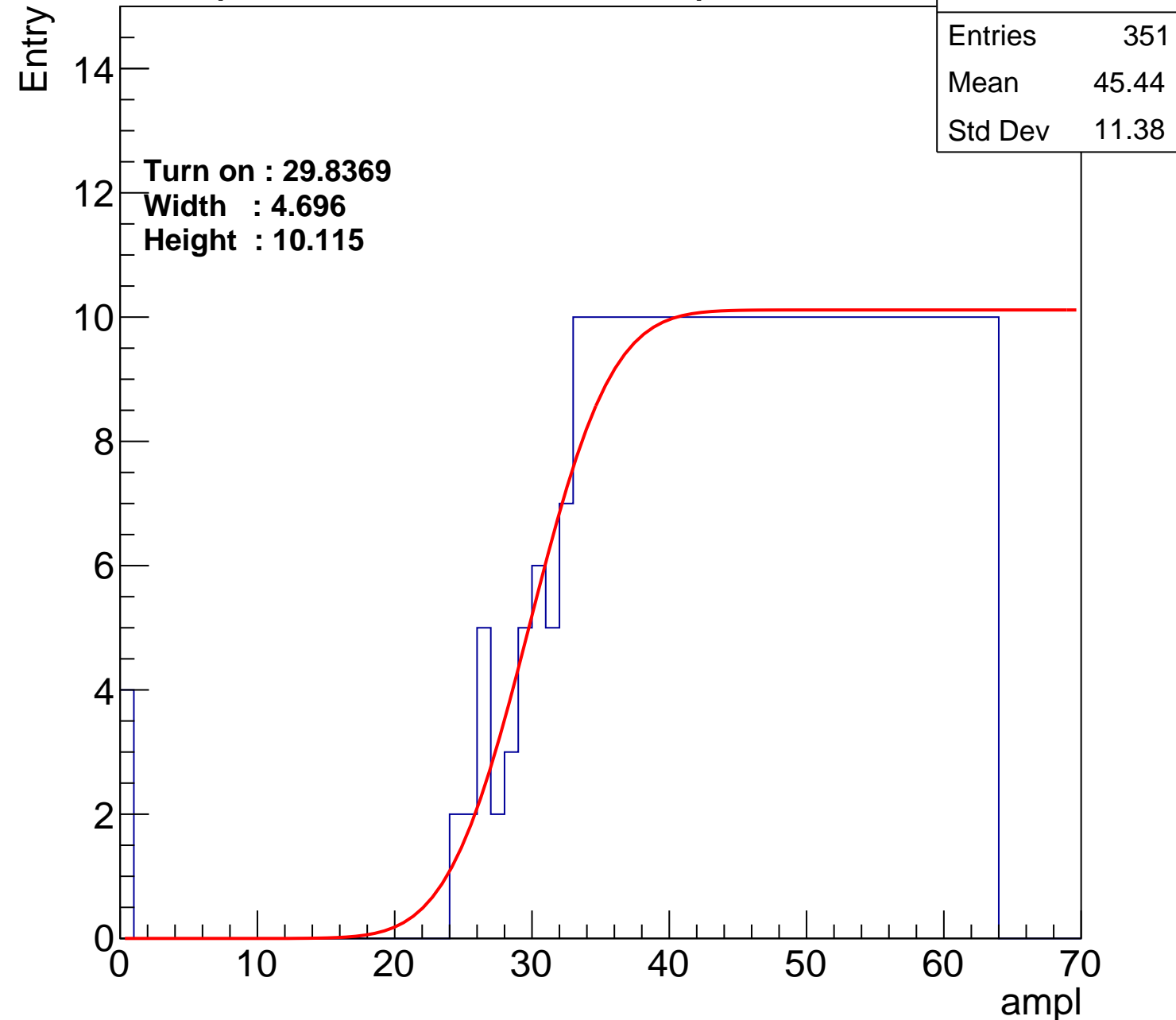
Width : 4.696

Height : 10.115

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch105

calib_packv5_042523_0143.root, FC#9, port A1

Entries	340
Mean	45.87
Std Dev	11.4

Turn on : 30.9784

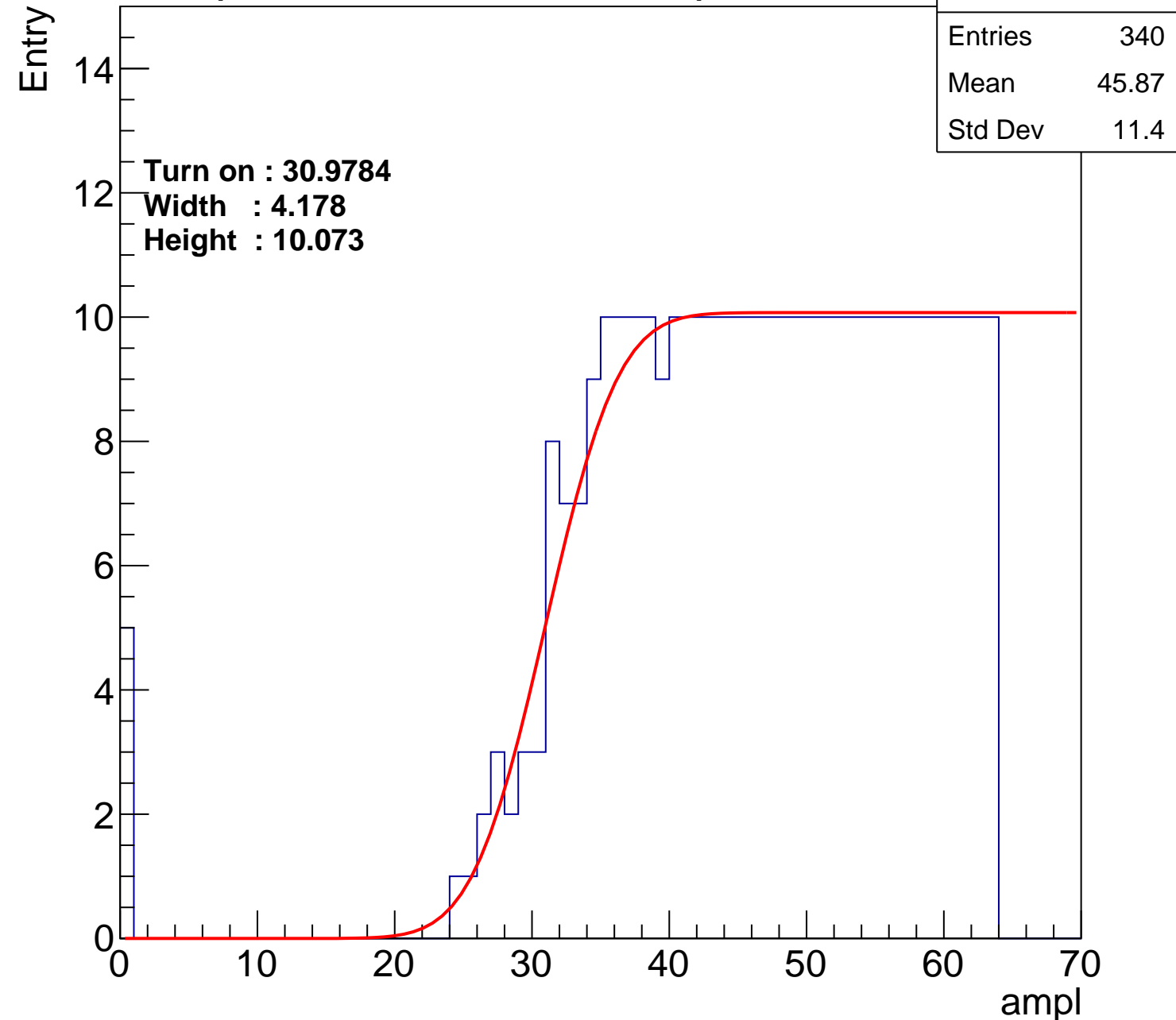
Width : 4.178

Height : 10.073

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch106

calib_packv5_042523_0143.root, FC#9, port A1

Entries	363
Mean	45.03
Std Dev	11.18

Turn on : 27.9162

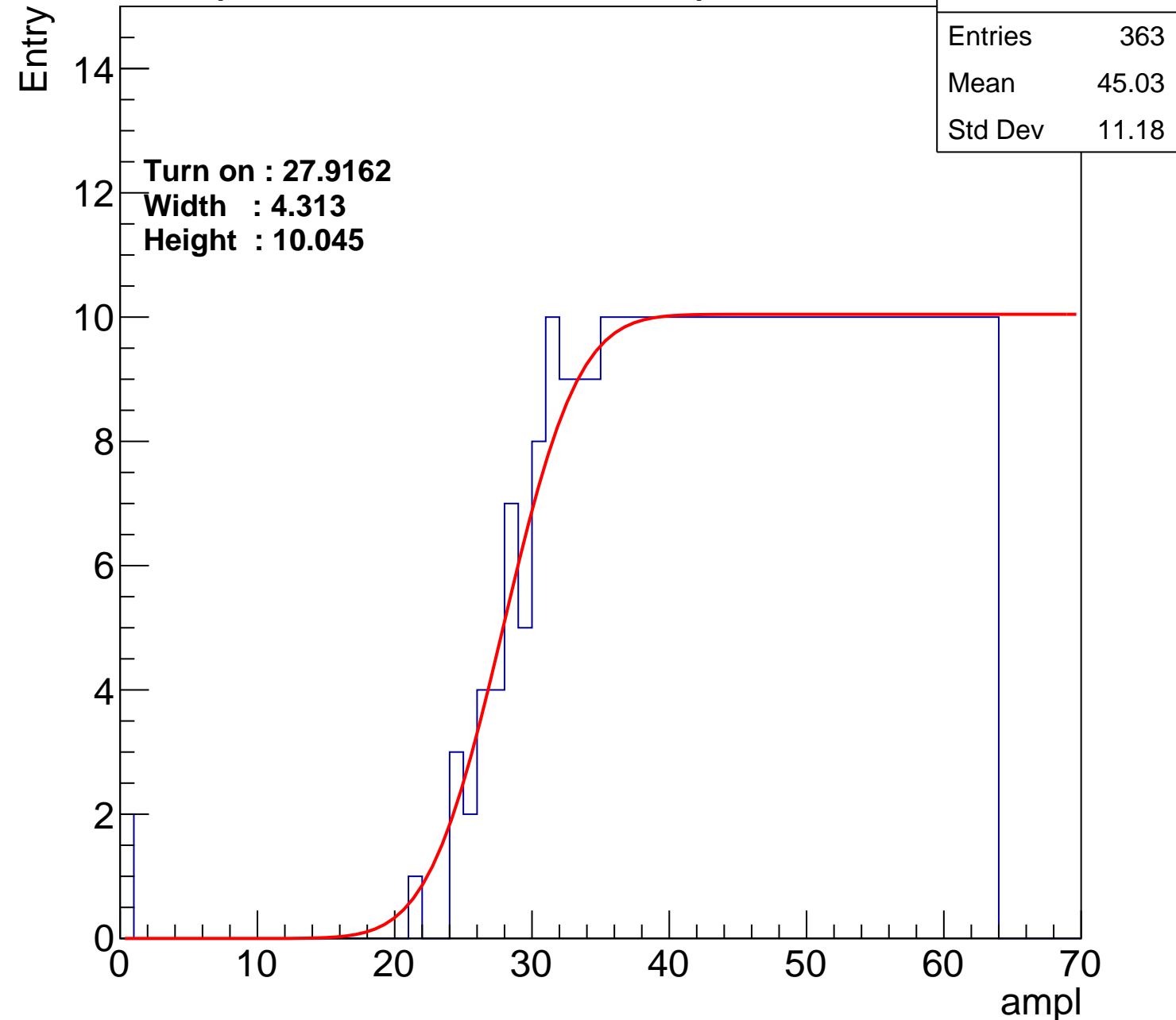
Width : 4.313

Height : 10.045

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch107

calib_packv5_042523_0143.root, FC#9, port A1

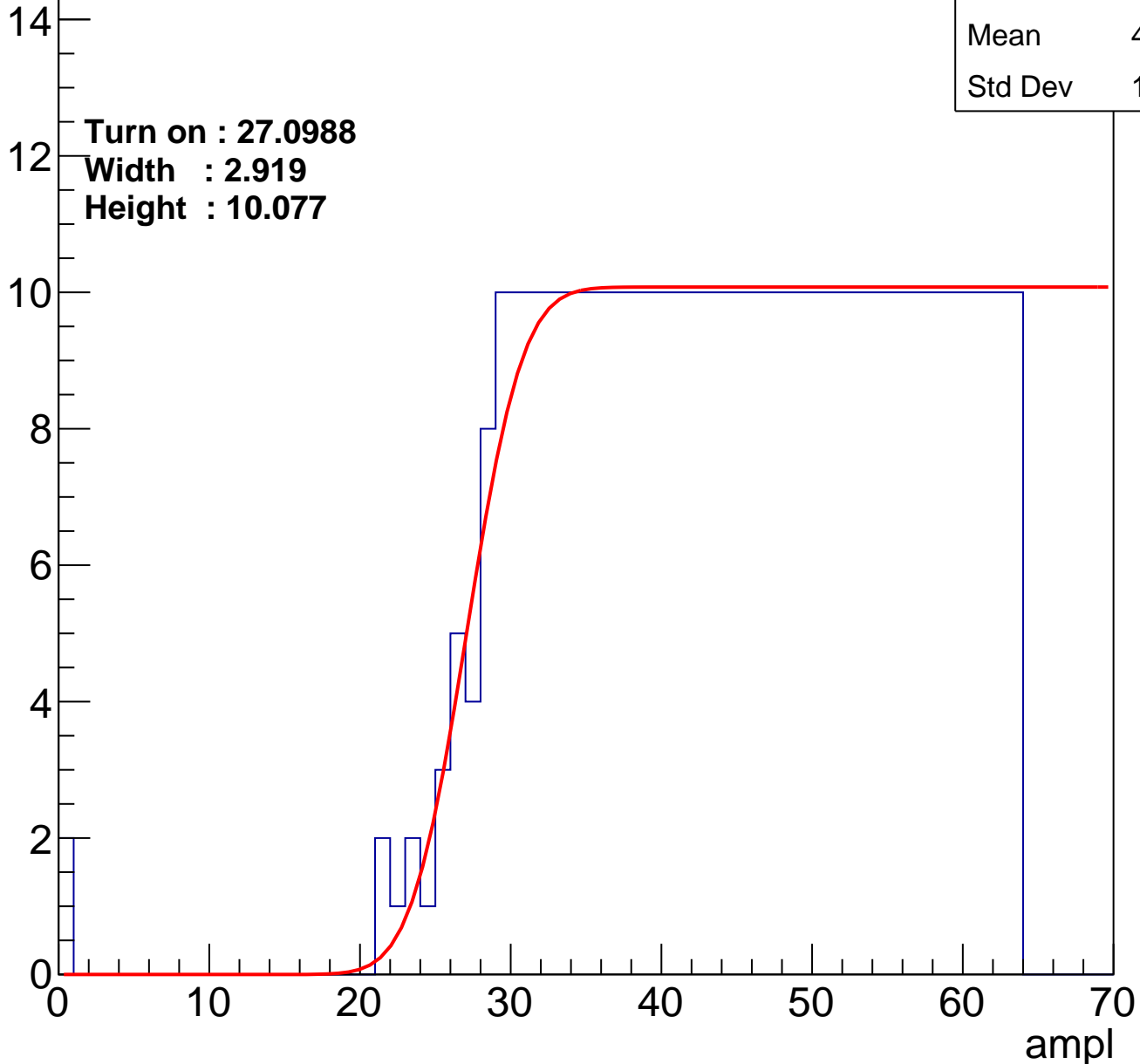
Entries	378
Mean	44.37
Std Dev	11.46

Turn on : 27.0988

Width : 2.919

Height : 10.077

Entry



B0L001S, U3-ch108

calib_packv5_042523_0143.root, FC#9, port A1

Entries	376
Mean	44.31
Std Dev	11.81

Turn on : 27.5246

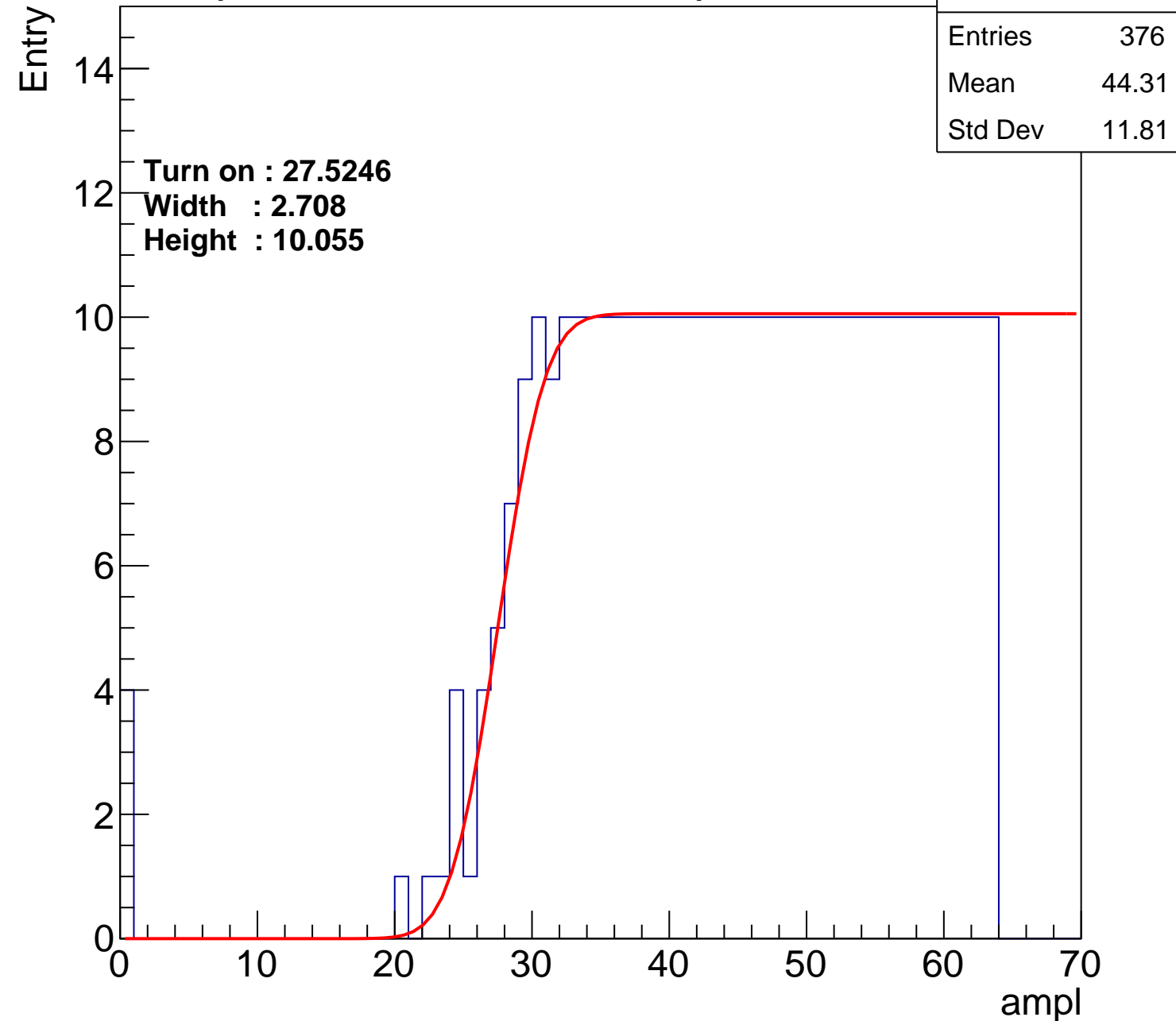
Width : 2.708

Height : 10.055

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch109

calib_packv5_042523_0143.root, FC#9, port A1

Entries	334
Mean	46.37
Std Dev	10.74

Turn on : 31.4632

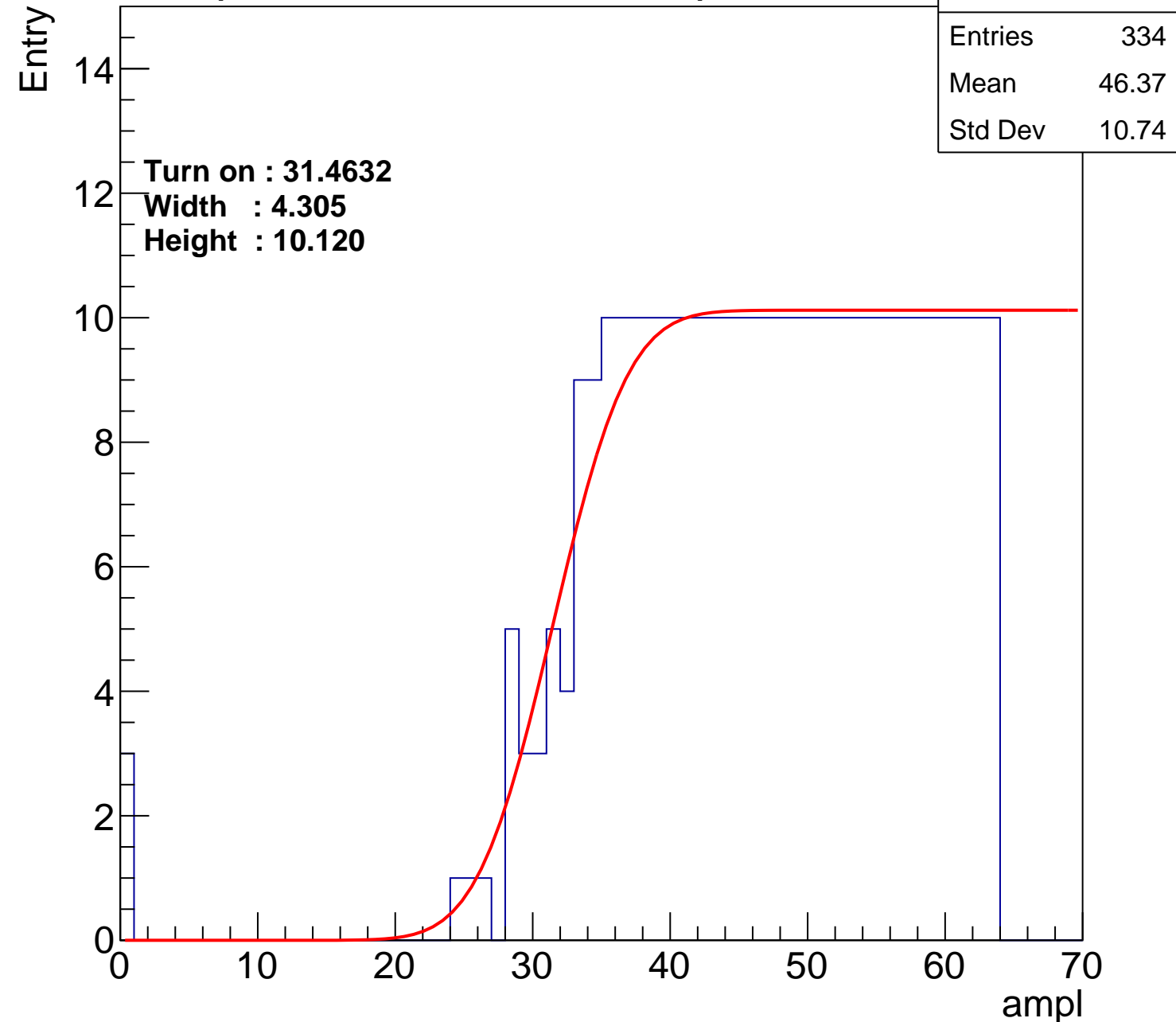
Width : 4.305

Height : 10.120

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch110

calib_packv5_042523_0143.root, FC#9, port A1

Entries	373
Mean	44.27
Std Dev	12.25

Turn on : 28.4338

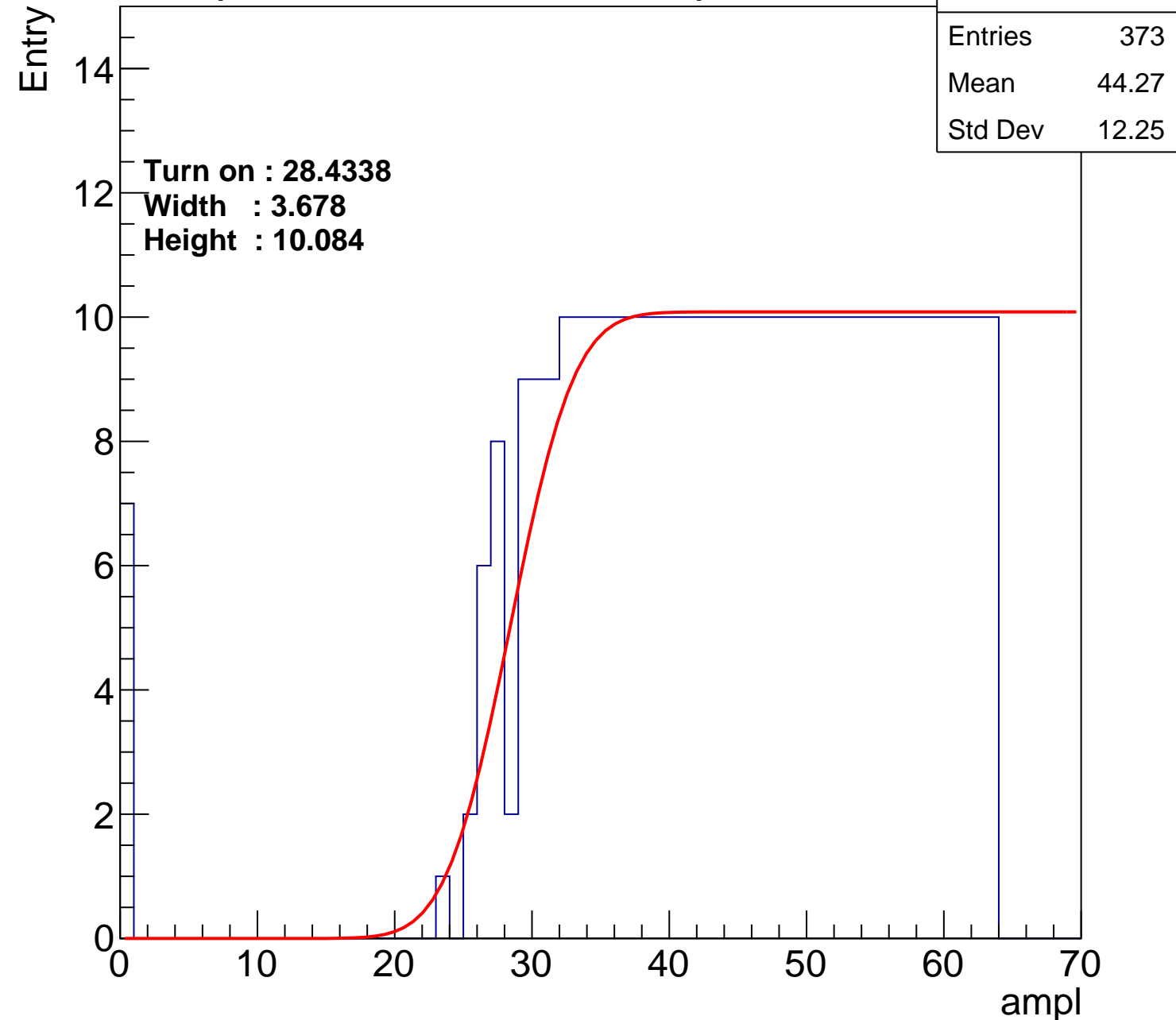
Width : 3.678

Height : 10.084

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch111

calib_packv5_042523_0143.root, FC#9, port A1

Entries	377
Mean	44.32
Std Dev	11.65

Turn on : 26.7100

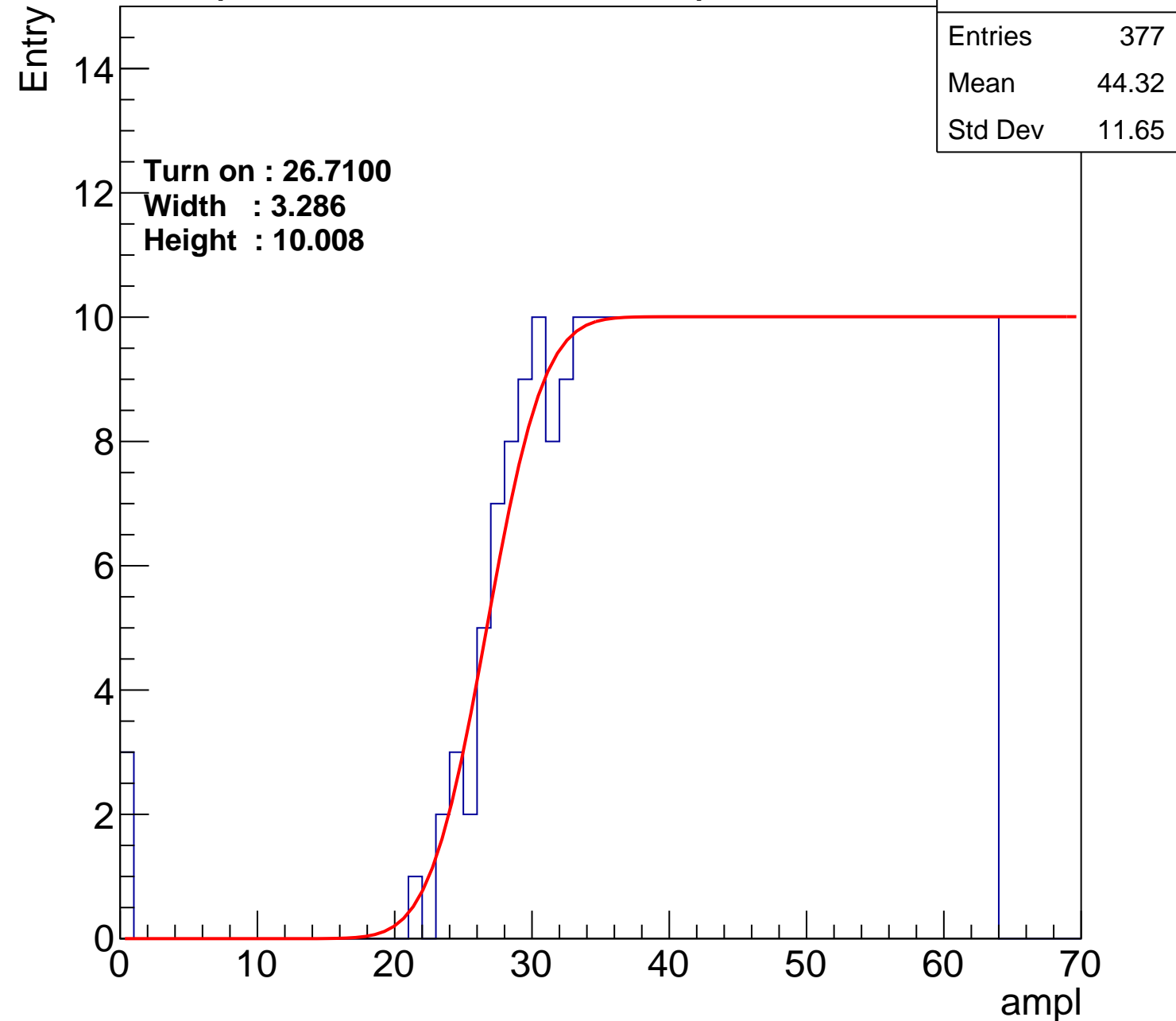
Width : 3.286

Height : 10.008

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch112

calib_packv5_042523_0143.root, FC#9, port A1

Entries	356
Mean	45.29
Std Dev	11.22

Turn on : 28.5616

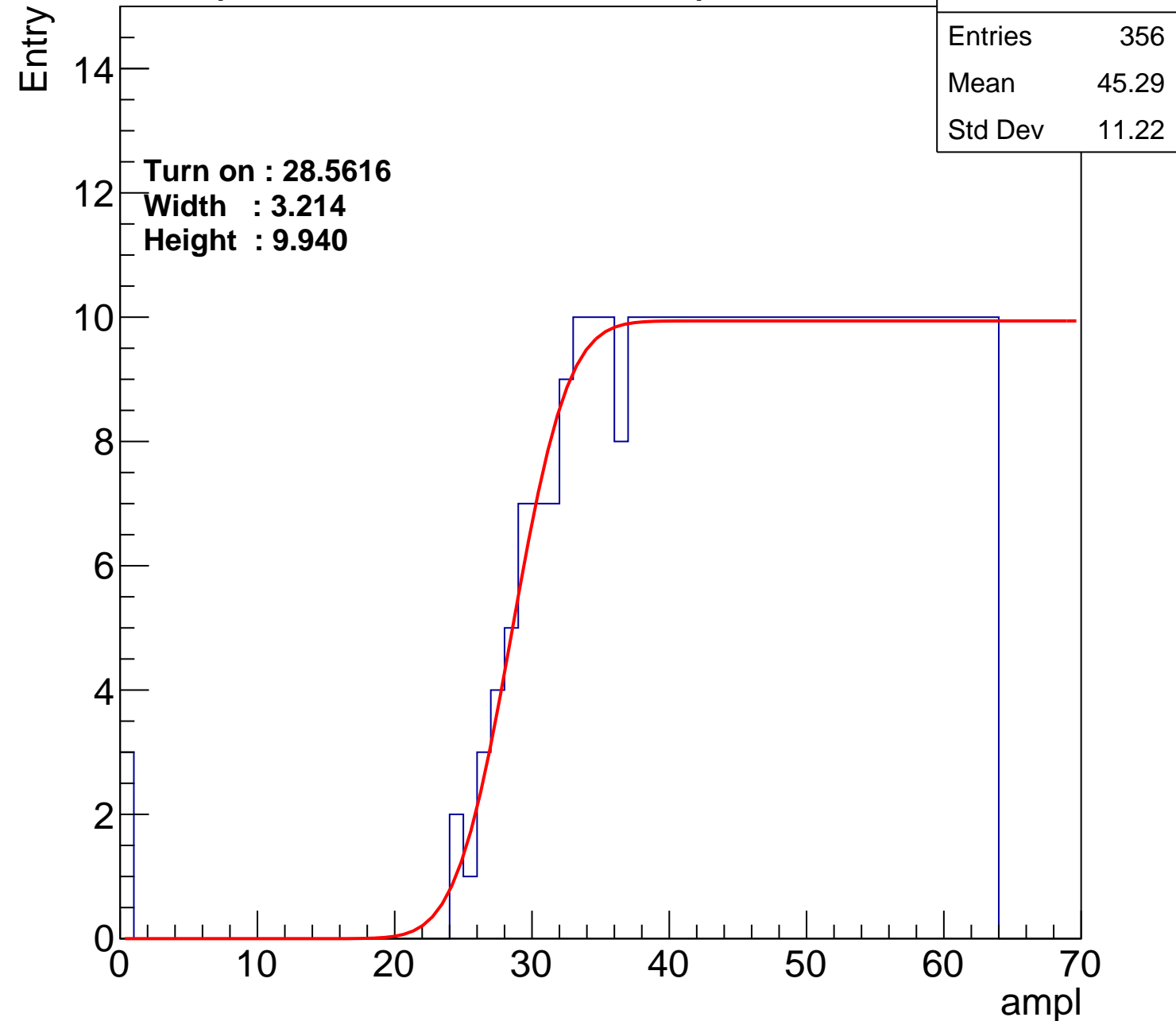
Width : 3.214

Height : 9.940

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch113

calib_packv5_042523_0143.root, FC#9, port A1

Entries	368
Mean	44.52
Std Dev	12.05

Turn on : 27.9156

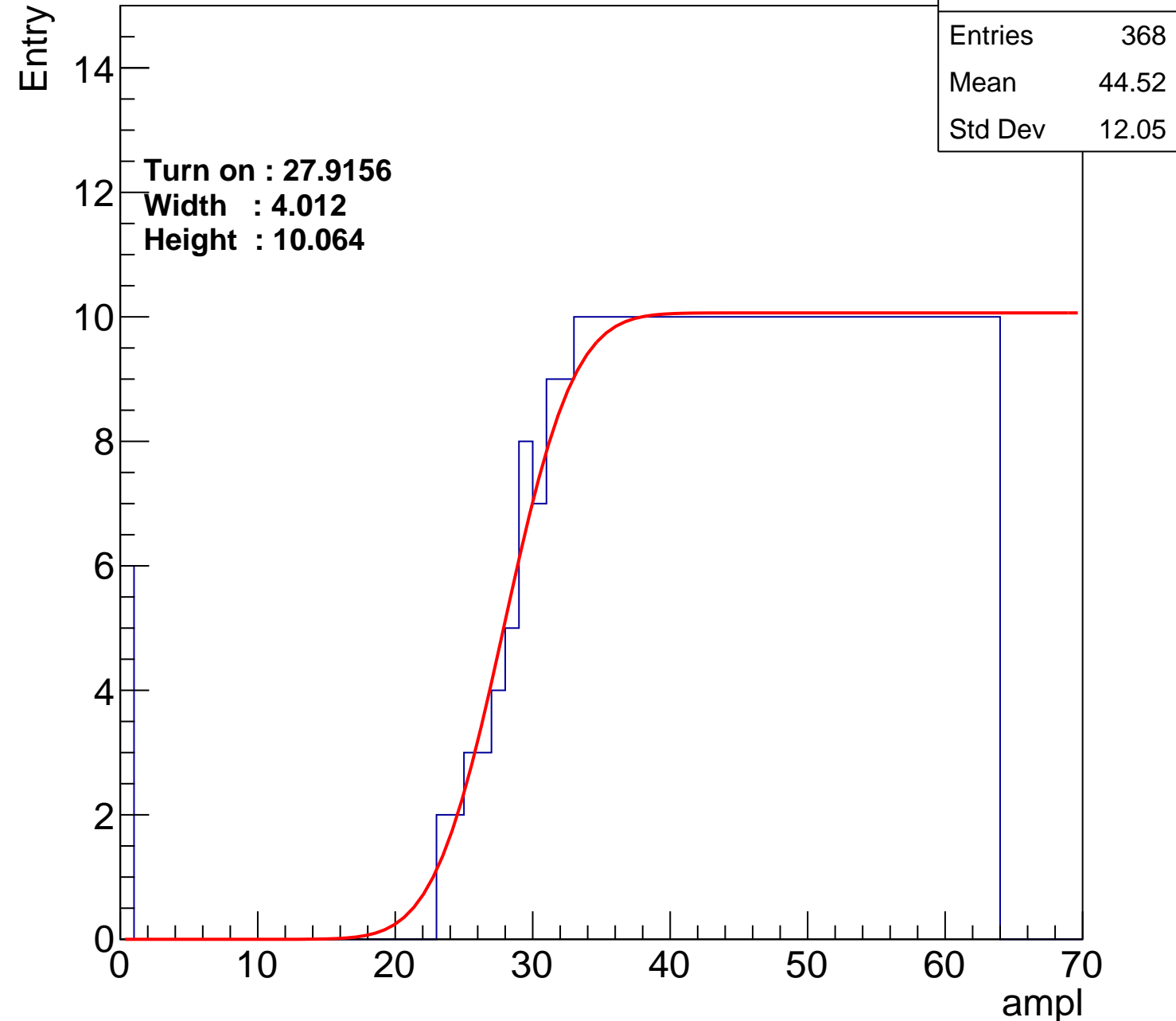
Width : 4.012

Height : 10.064

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch114

calib_packv5_042523_0143.root, FC#9, port A1

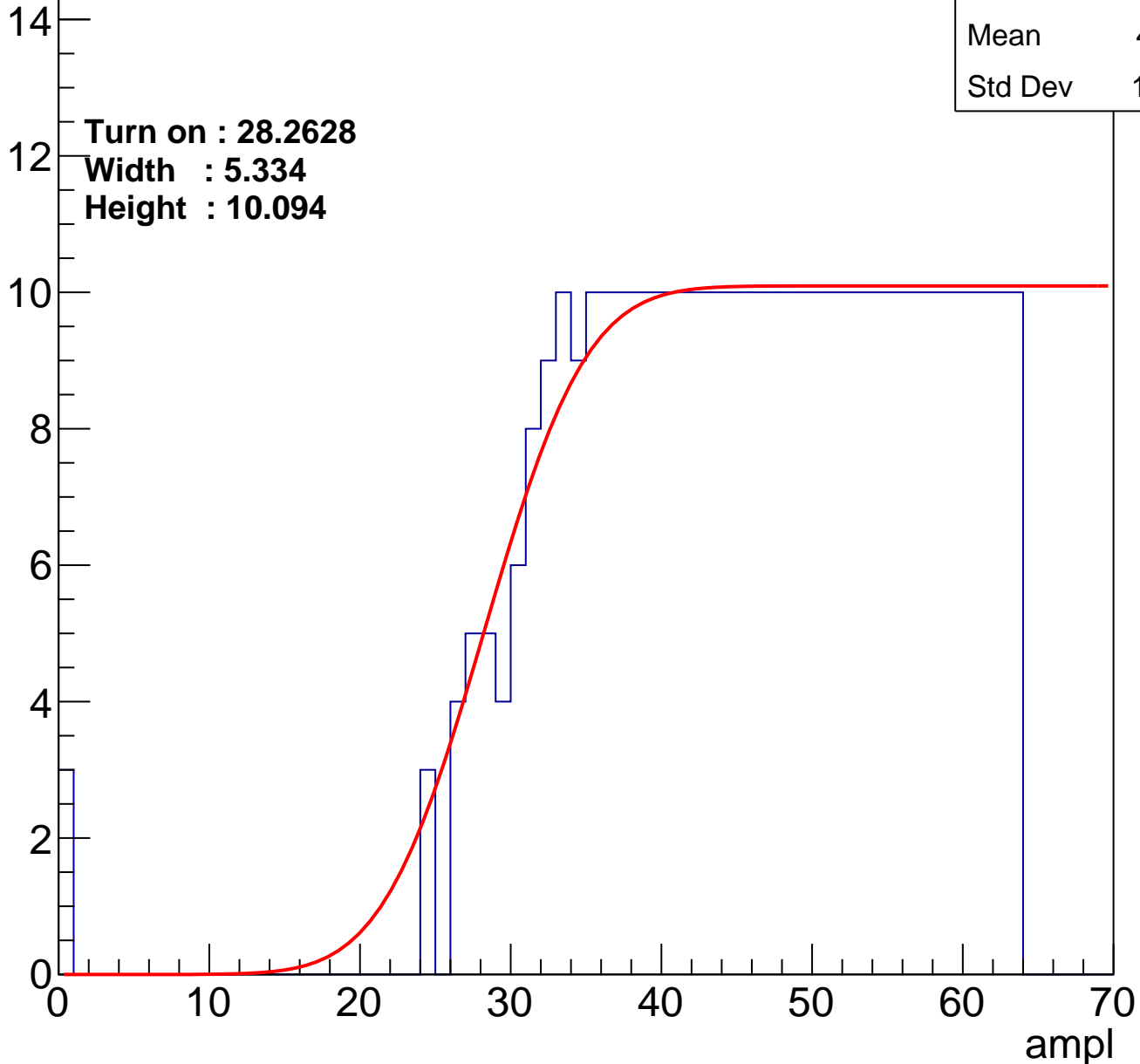
Entries	356
Mean	45.31
Std Dev	11.22

Turn on : 28.2628

Width : 5.334

Height : 10.094

Entry



B0L001S, U3-ch115

calib_packv5_042523_0143.root, FC#9, port A1

Entries	386
Mean	43.75
Std Dev	12.21

Turn on : 25.9326

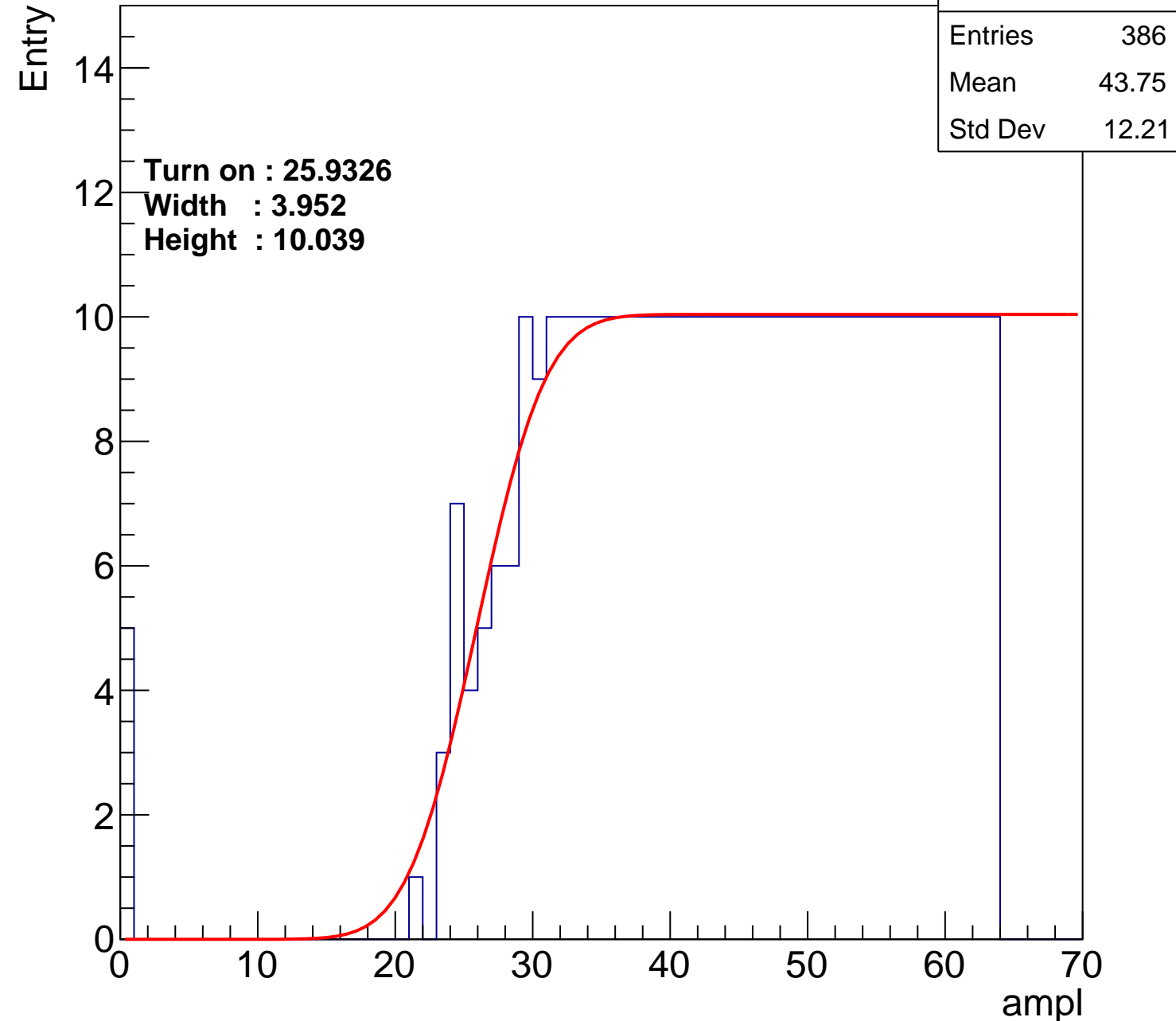
Width : 3.952

Height : 10.039

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch116

calib_packv5_042523_0143.root, FC#9, port A1

Entries	364
Mean	45.04
Std Dev	11.13

Turn on : 27.8990

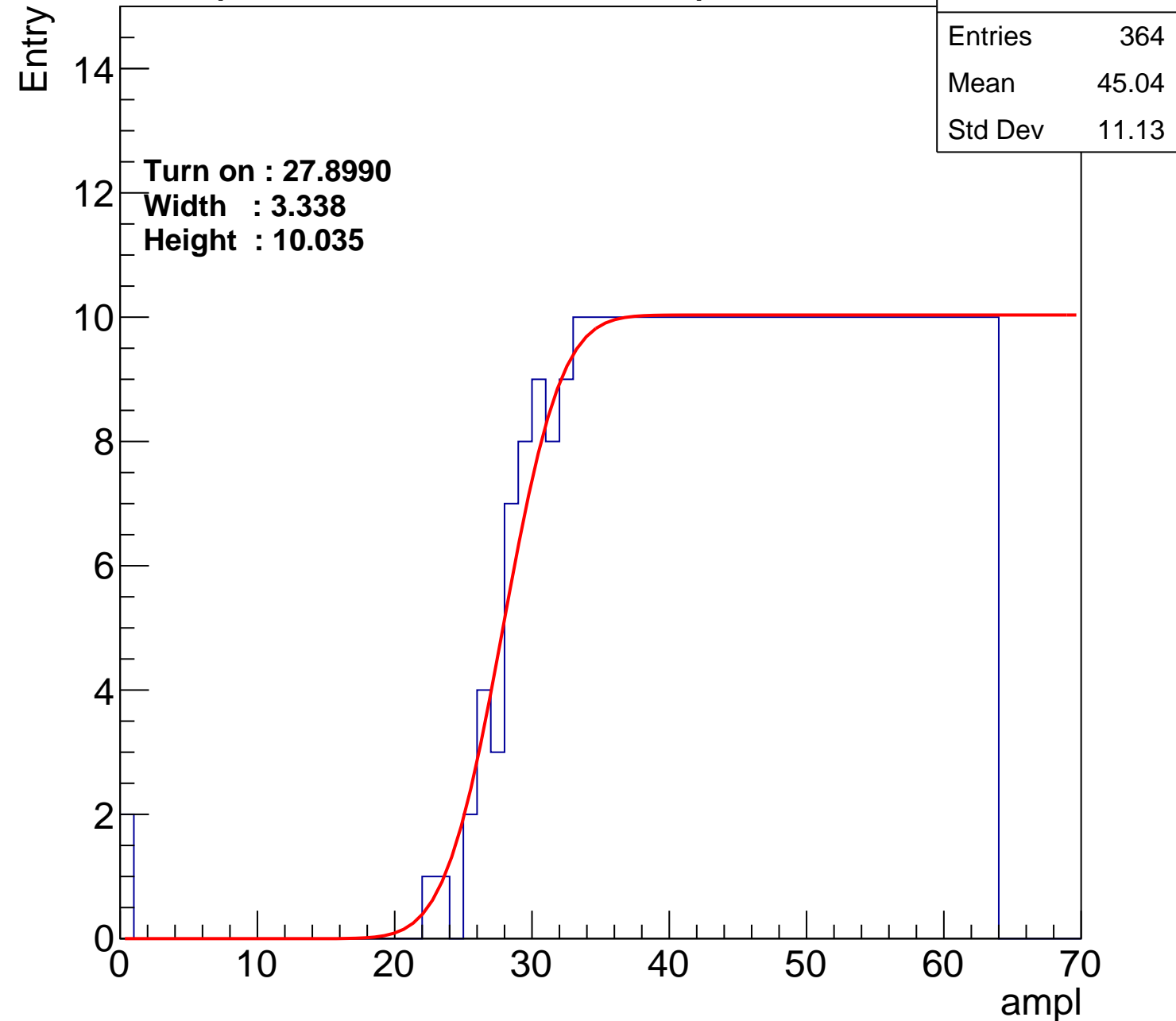
Width : 3.338

Height : 10.035

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch117

calib_packv5_042523_0143.root, FC#9, port A1

Entries	366
Mean	44.95
Std Dev	11.08

Turn on : 28.4934

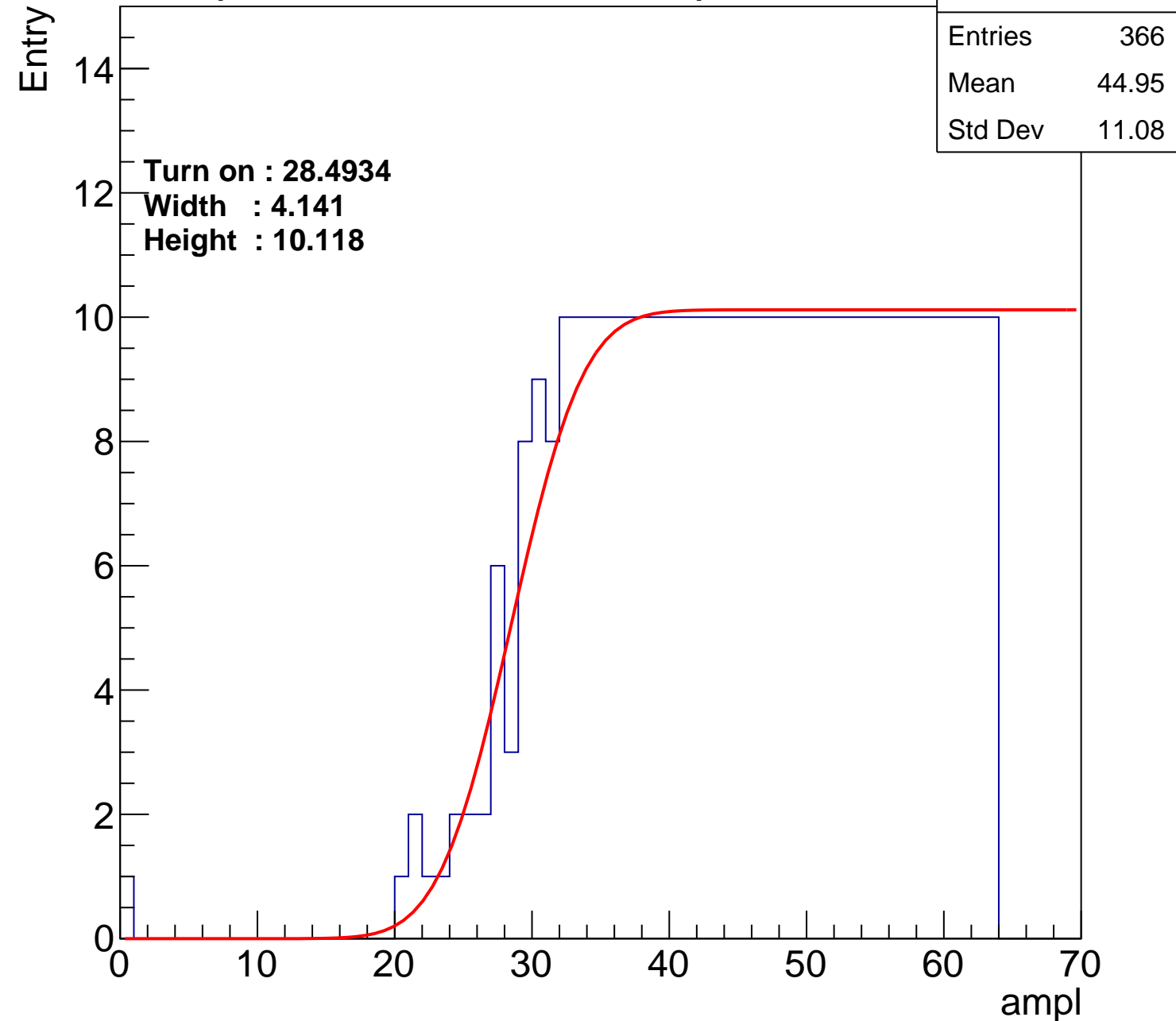
Width : 4.141

Height : 10.118

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch118

calib_packv5_042523_0143.root, FC#9, port A1

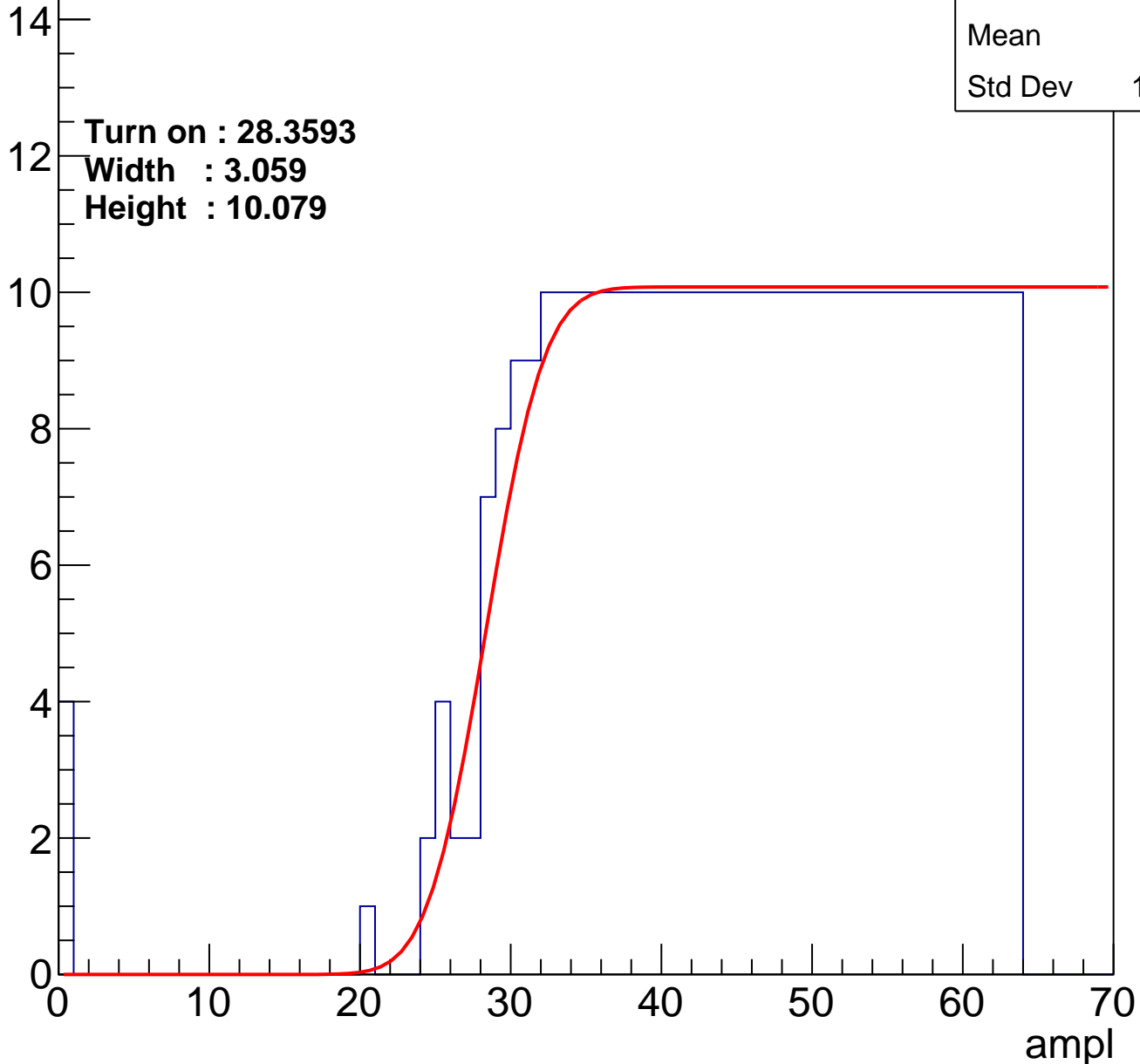
Entries	368
Mean	44.7
Std Dev	11.62

Turn on : 28.3593

Width : 3.059

Height : 10.079

Entry



B0L001S, U3-ch119

calib_packv5_042523_0143.root, FC#9, port A1

Entries	367
Mean	44.88
Std Dev	11.22

Turn on : 27.5120

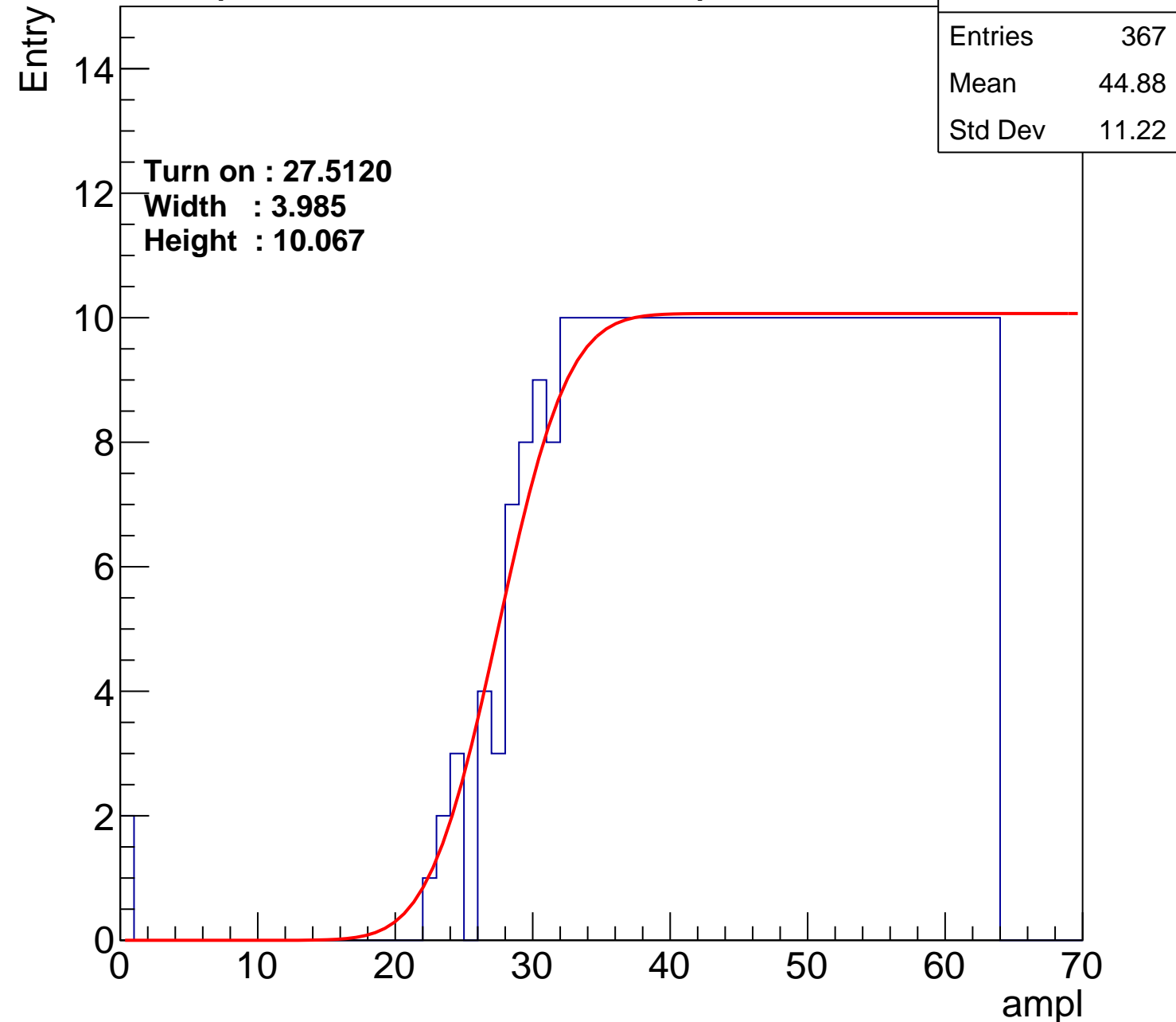
Width : 3.985

Height : 10.067

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch120

calib_packv5_042523_0143.root, FC#9, port A1

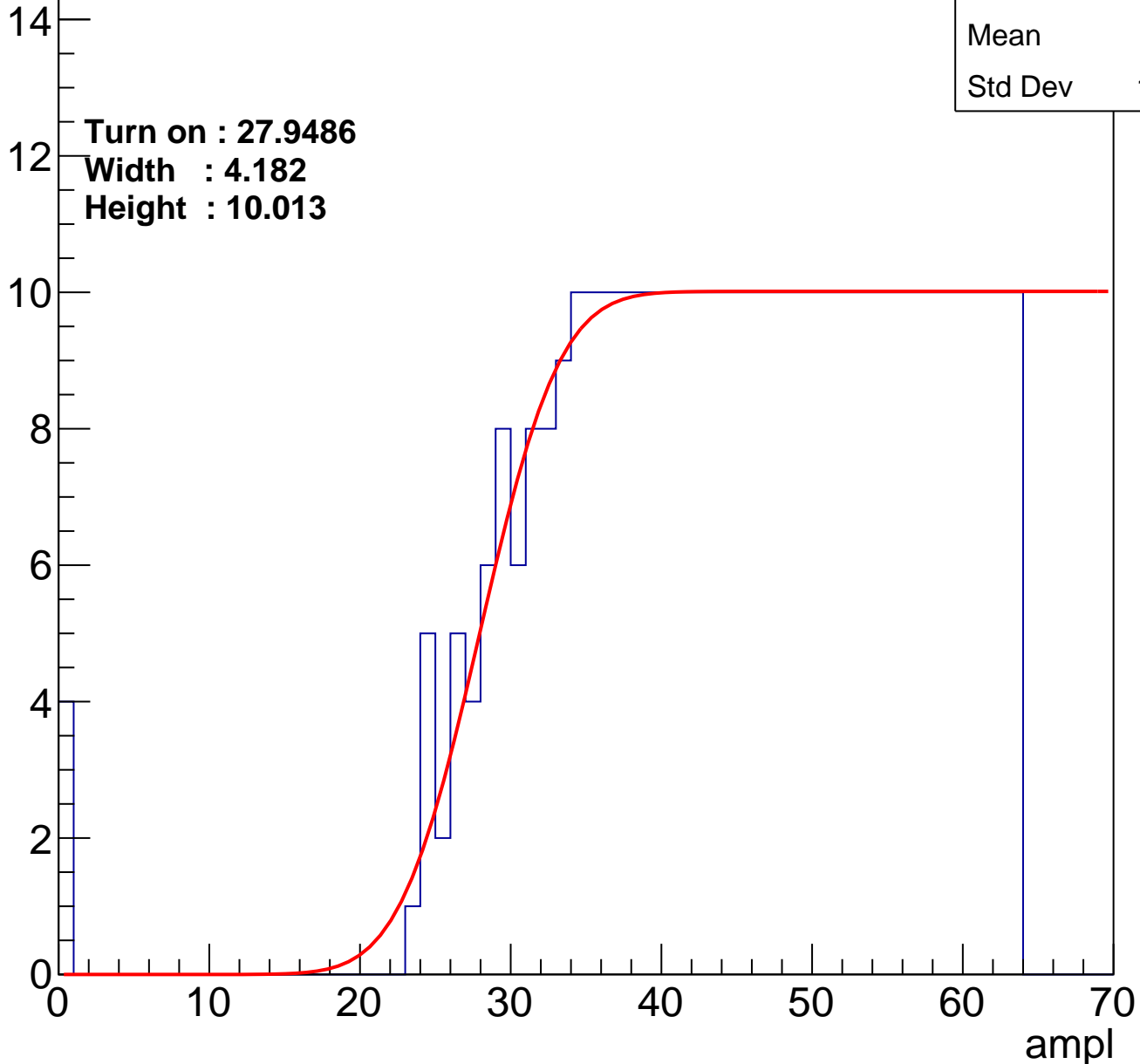
Entries	366
Mean	44.7
Std Dev	11.71

Turn on : 27.9486

Width : 4.182

Height : 10.013

Entry



B0L001S, U3-ch121

calib_packv5_042523_0143.root, FC#9, port A1

Entries	358
Mean	44.96
Std Dev	11.9

Turn on : 28.3090

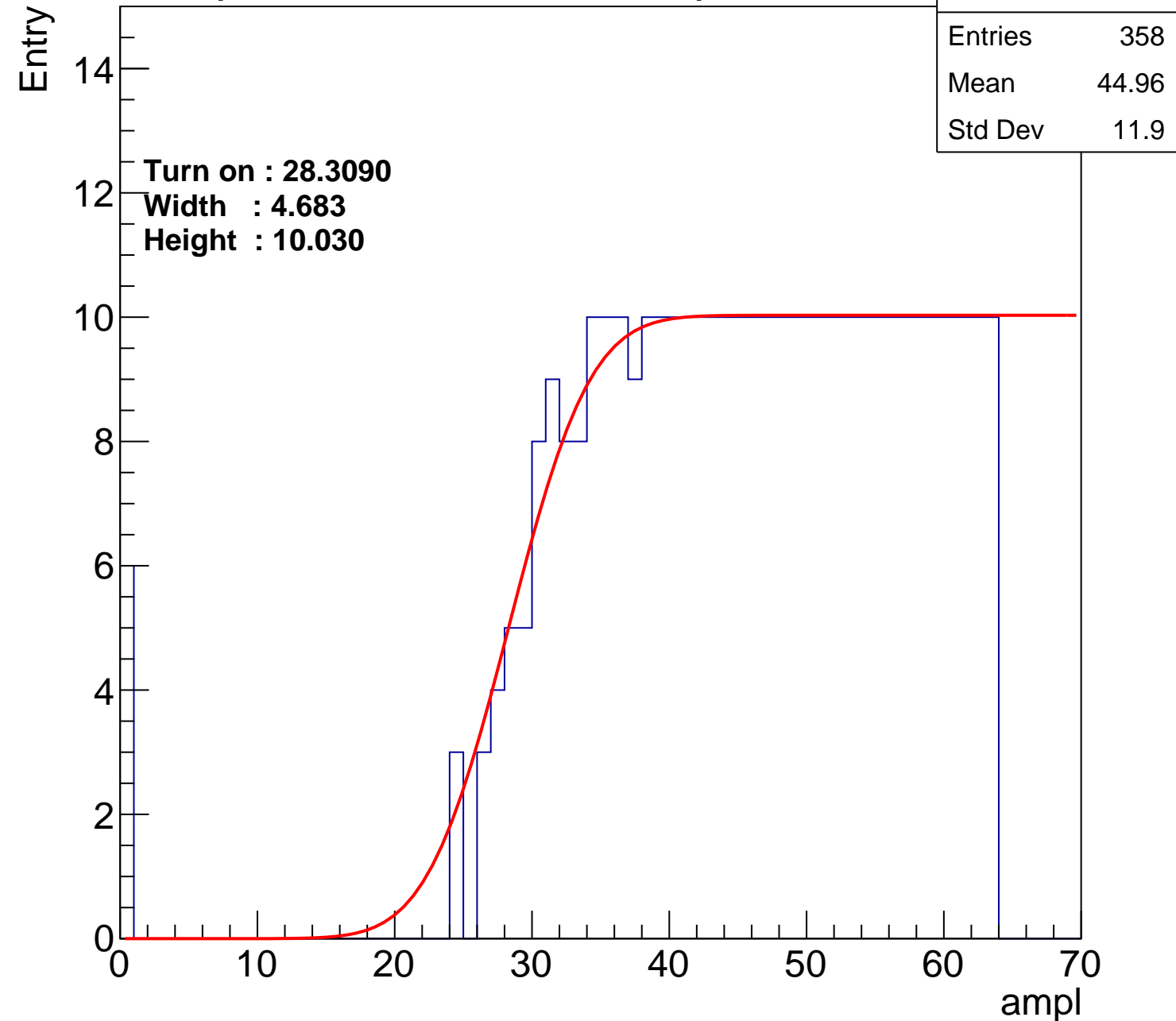
Width : 4.683

Height : 10.030

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch122

calib_packv5_042523_0143.root, FC#9, port A1

Entries	368
Mean	44.54
Std Dev	12.03

Turn on : 28.2533

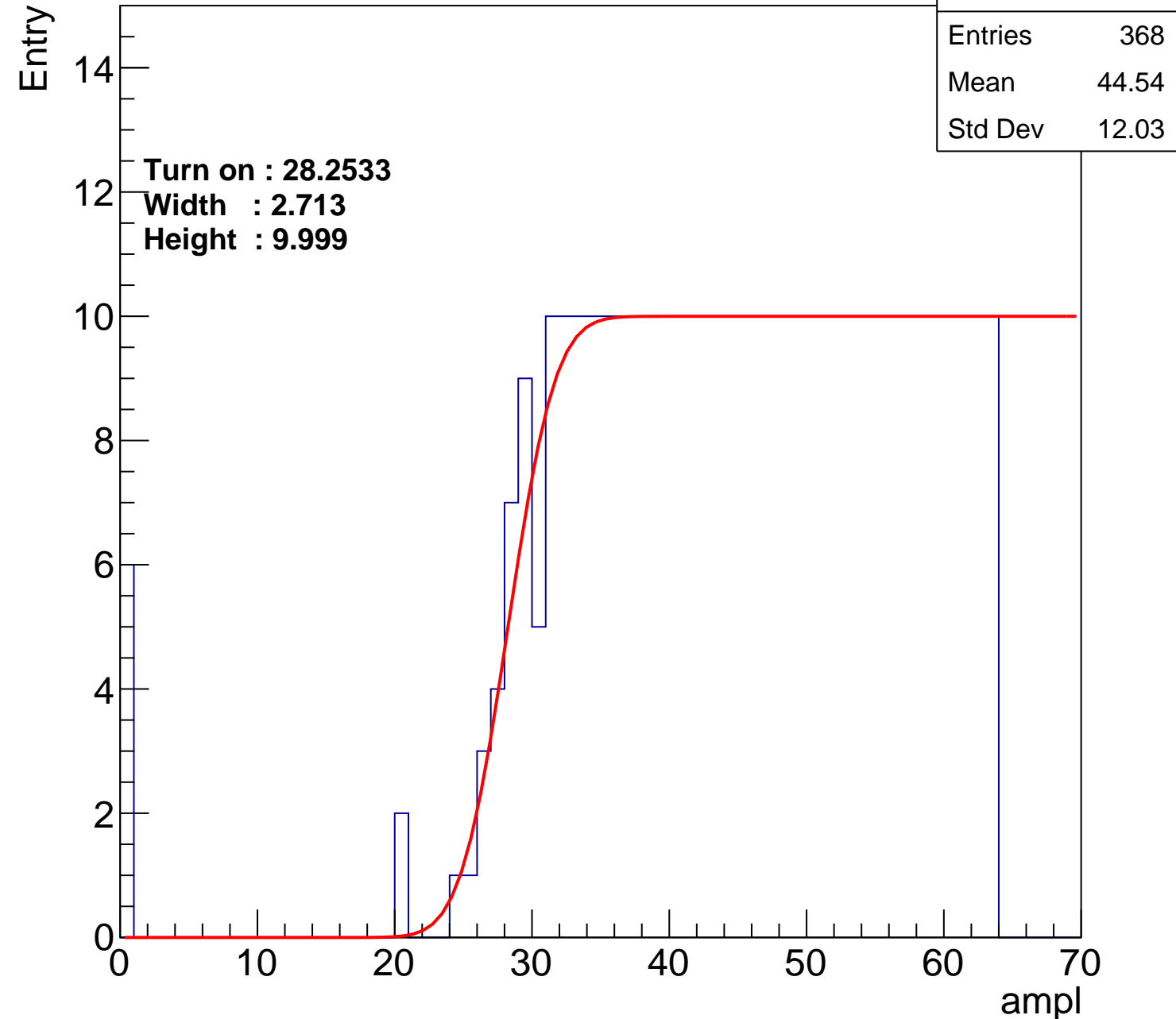
Width : 2.713

Height : 9.999

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch123

calib_packv5_042523_0143.root, FC#9, port A1

Entries	367
Mean	44.65
Std Dev	11.83

Turn on : 28.0647

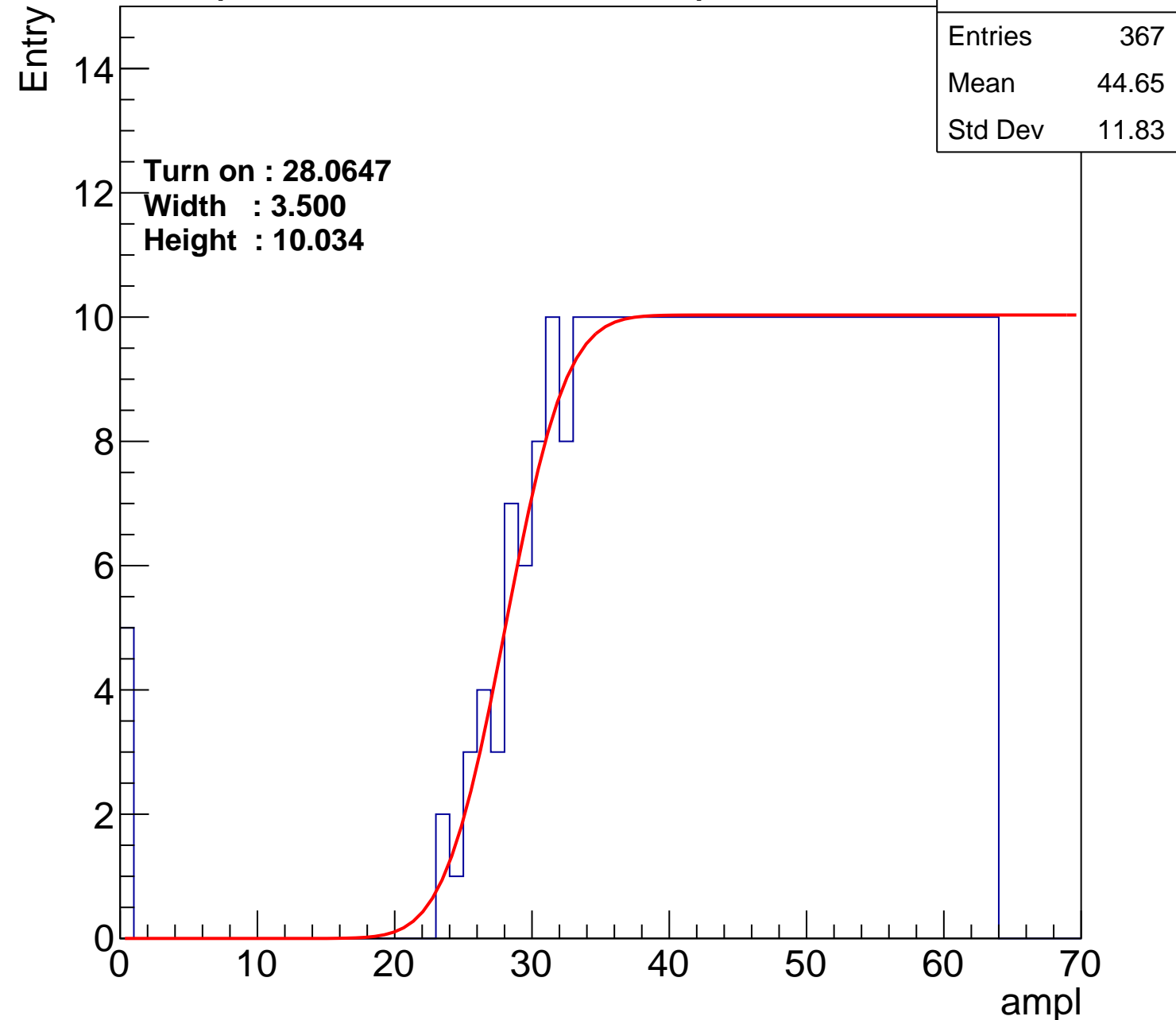
Width : 3.500

Height : 10.034

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch124

calib_packv5_042523_0143.root, FC#9, port A1

Entries	352
Mean	45.62
Std Dev	10.84

Turn on : 29.4002

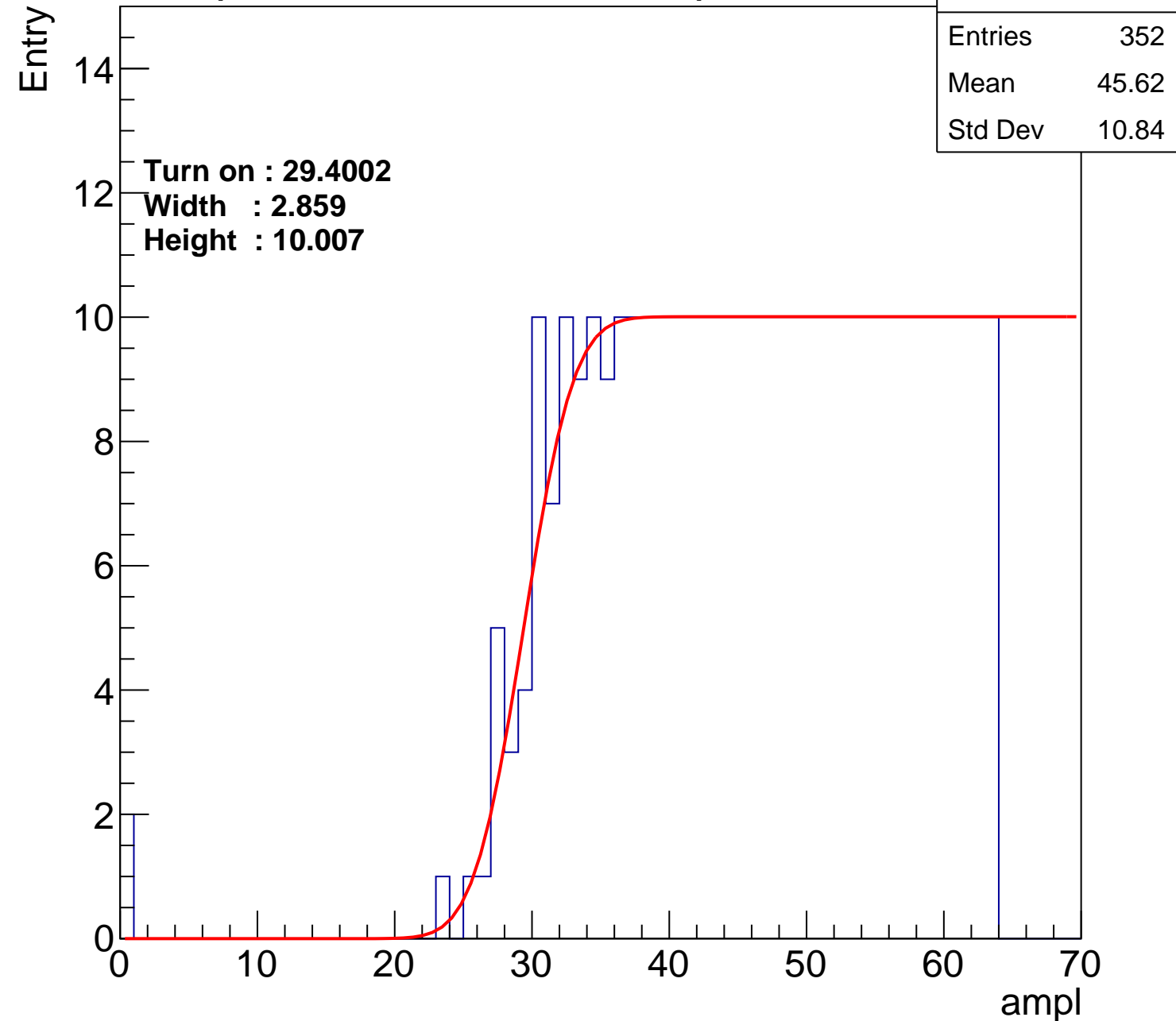
Width : 2.859

Height : 10.007

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch125

calib_packv5_042523_0143.root, FC#9, port A1

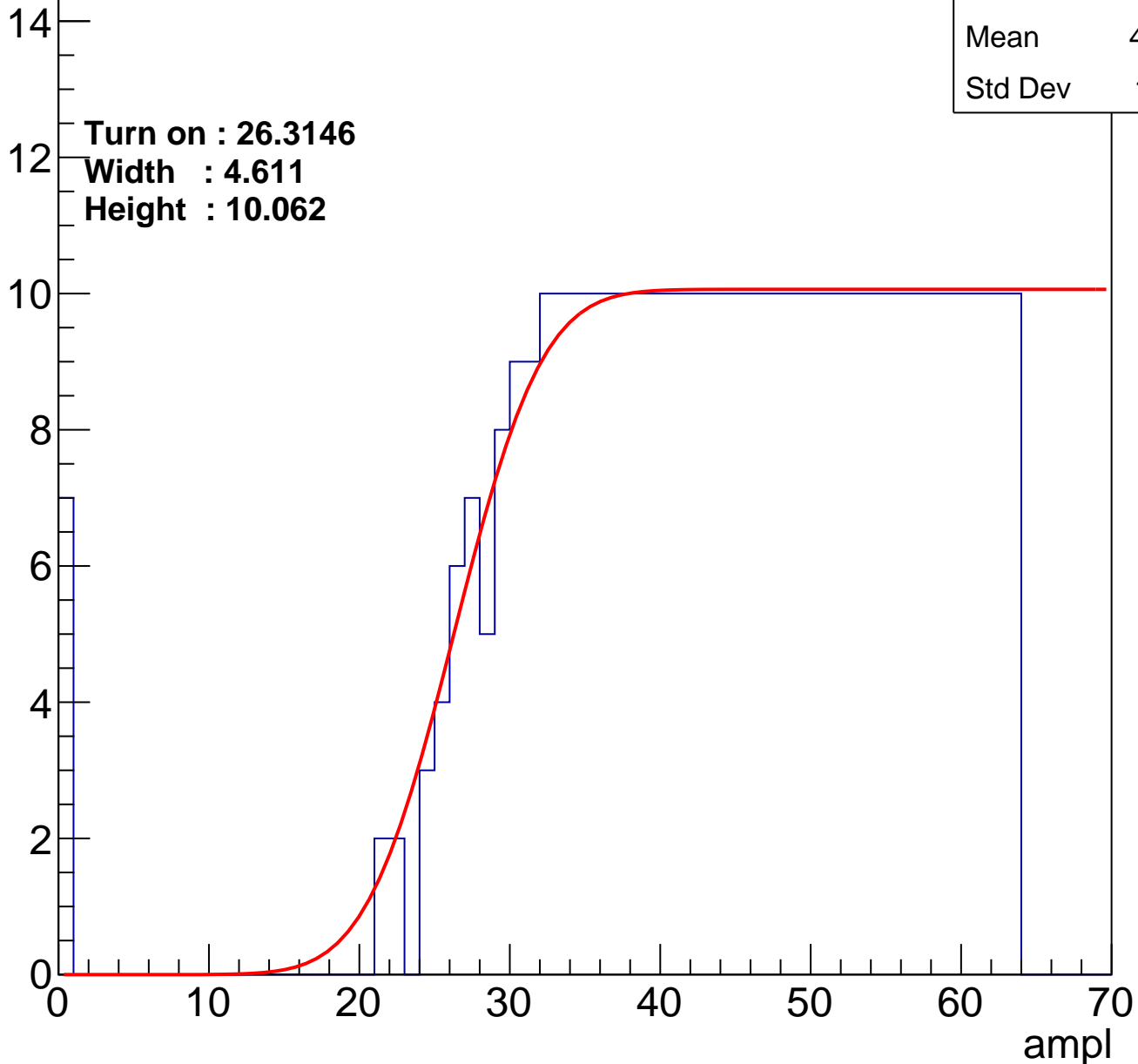
Entries	382
Mean	43.78
Std Dev	12.51

Turn on : 26.3146

Width : 4.611

Height : 10.062

Entry



B0L001S, U3-ch126

calib_packv5_042523_0143.root, FC#9, port A1

Entries	365
Mean	44.87
Std Dev	11.42

Turn on : 27.7408

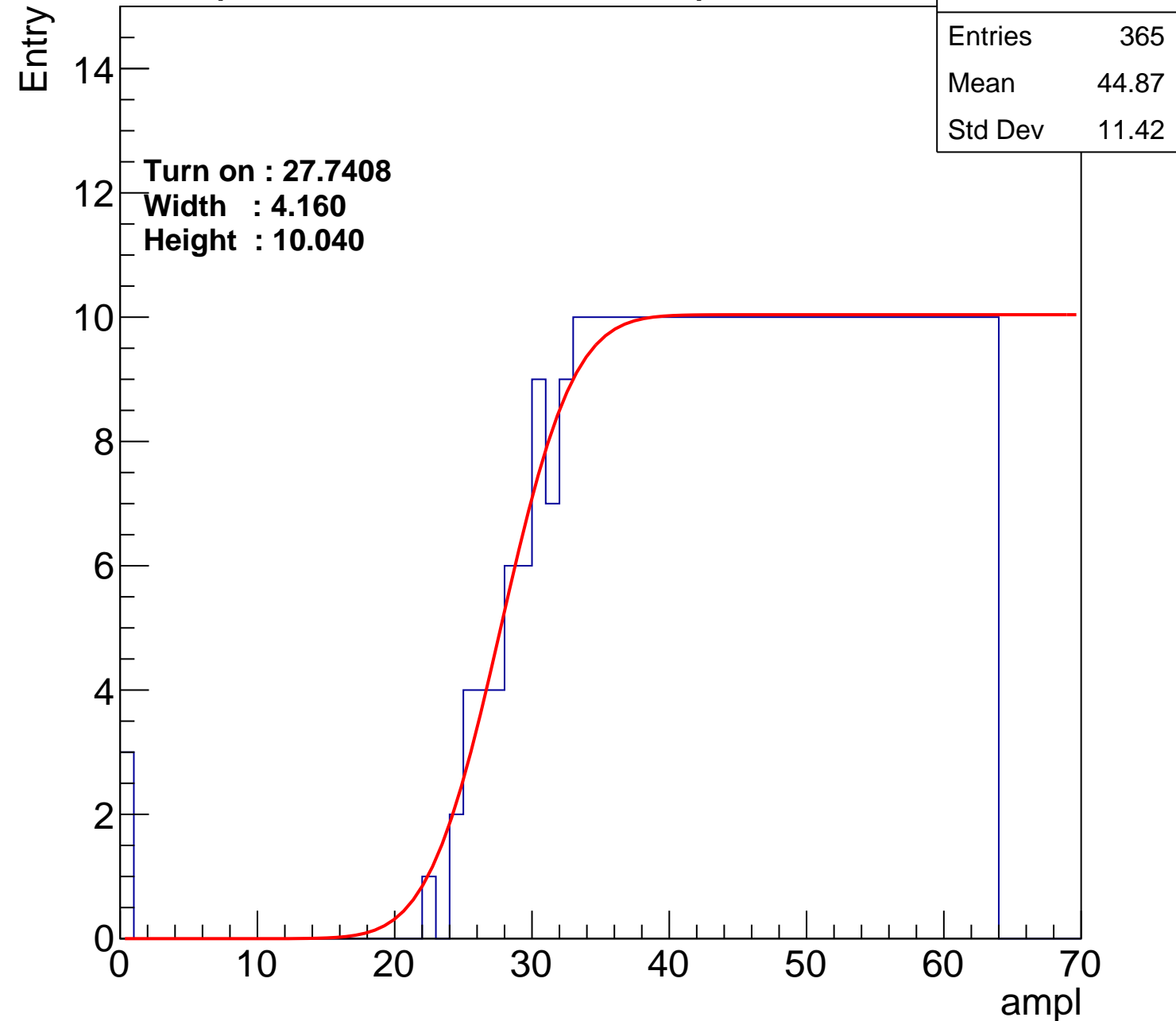
Width : 4.160

Height : 10.040

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch127

calib_packv5_042523_0143.root, FC#9, port A1

Entries	360
Mean	45.14
Std Dev	11.27

Turn on : 28.4474

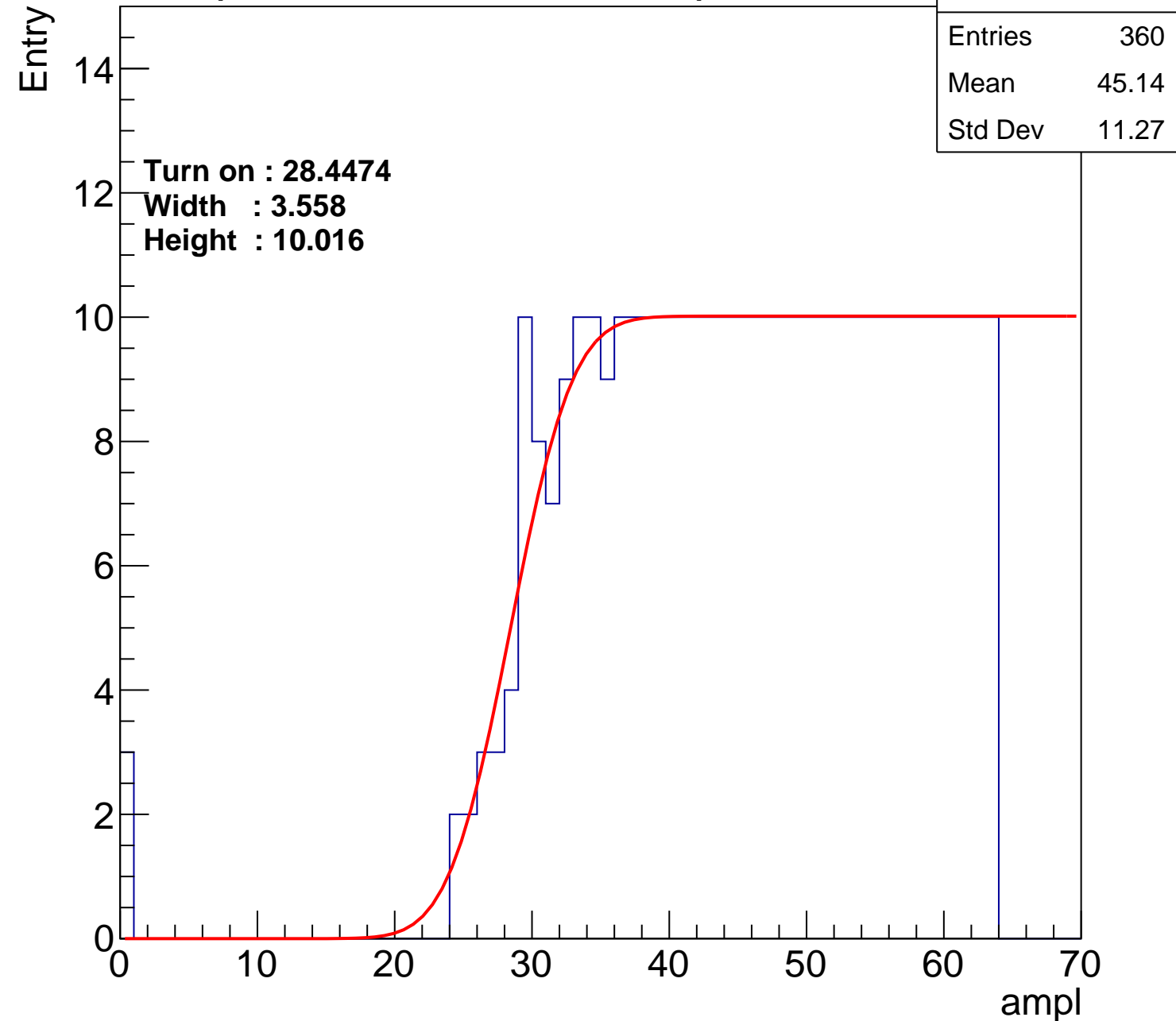
Width : 3.558

Height : 10.016

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U3-ch127

calib_packv5_042523_0143.root, FC#9, port A1

Entries	360
Mean	45.14
Std Dev	11.27

Turn on : 28.4474

Width : 3.558

Height : 10.016

Entry

14
12
10
8
6
4
2
0

ampl

