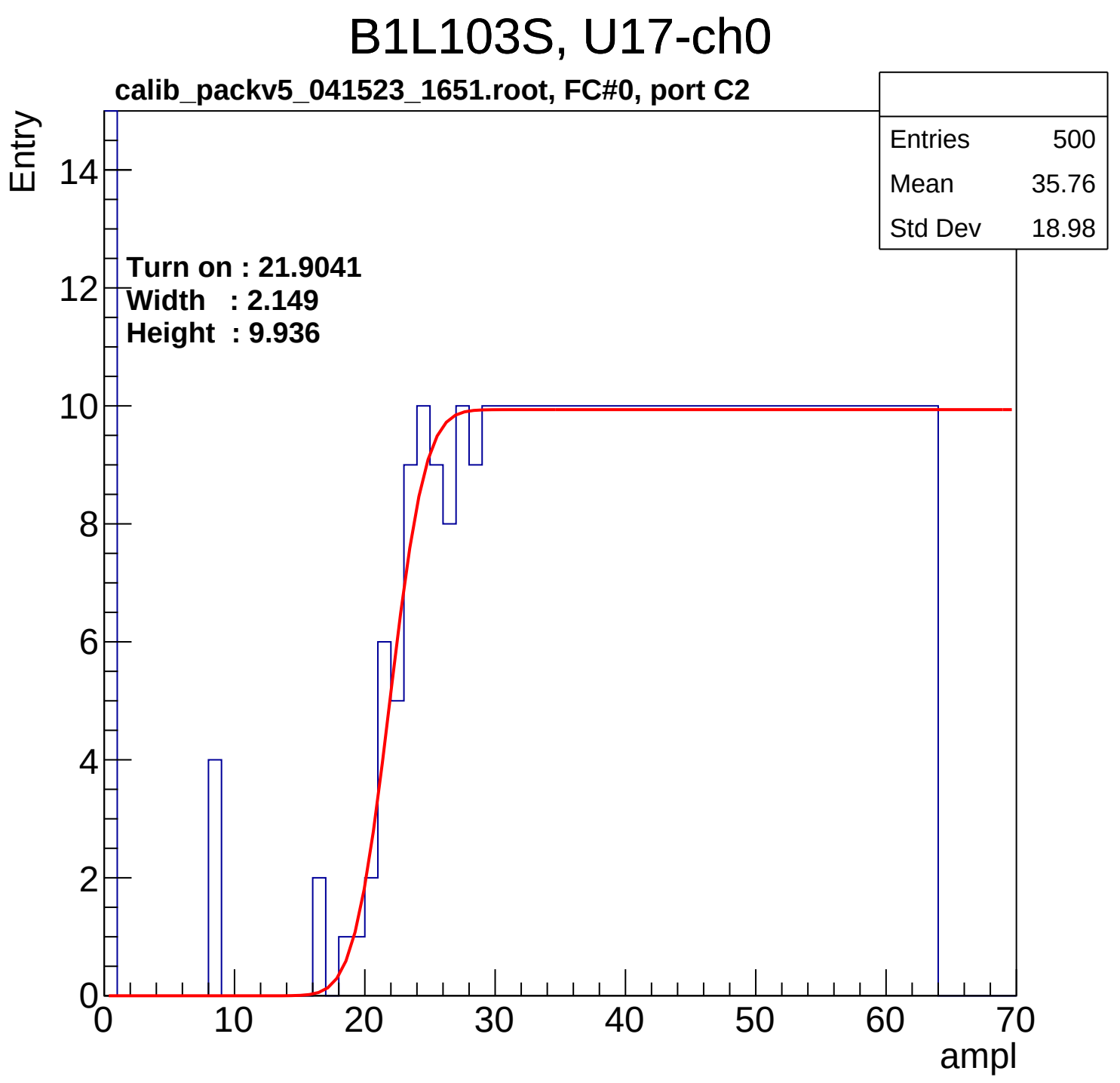
B1L103S, U17-ch0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 500
Mean 35.76
Std Dev 18.98
Turn on : 21.9041
Width : 2.149
Height : 9.936
Entry
ampl
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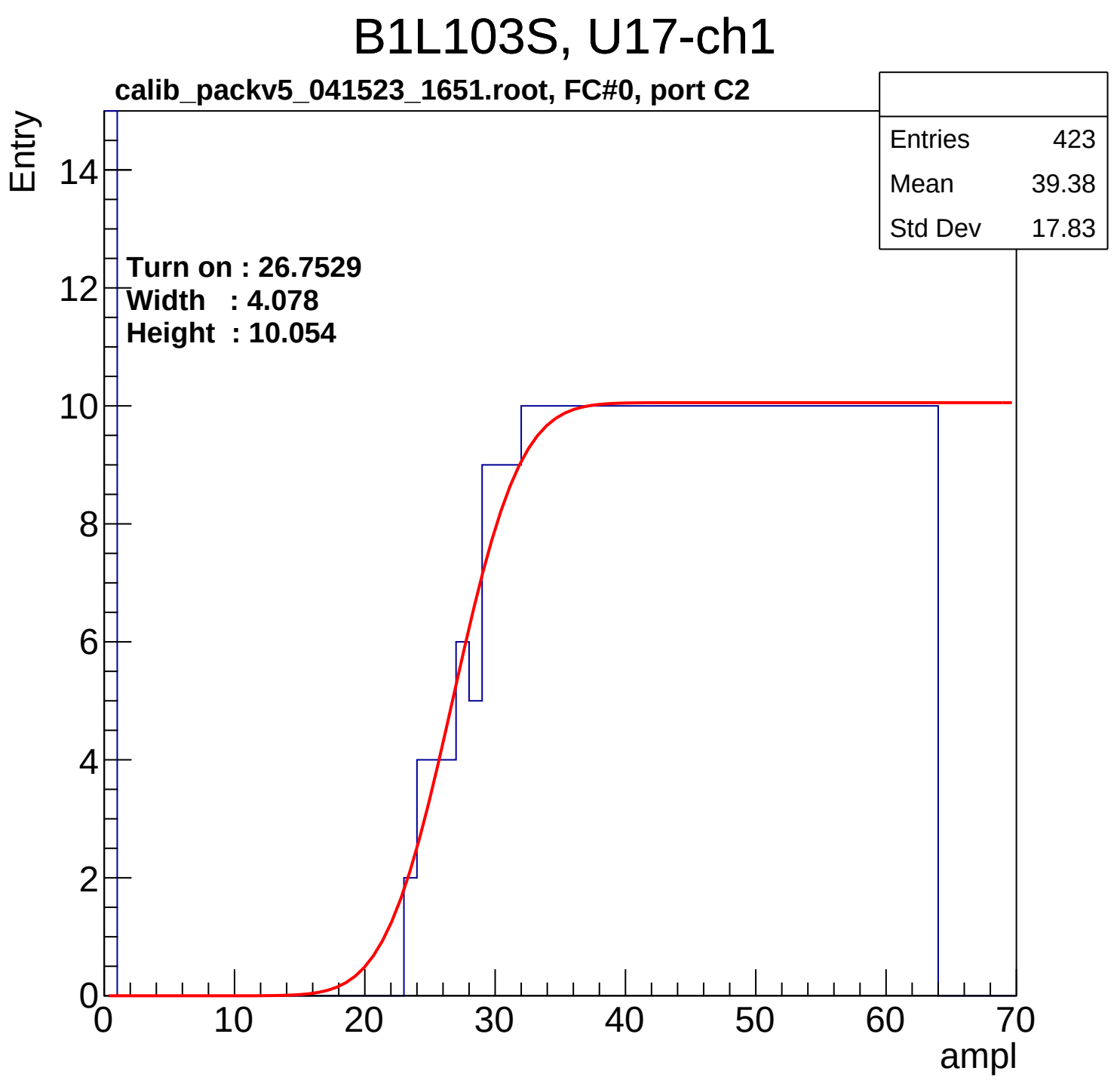
B1L103S, U17-ch1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 423
Mean 39.38
Std Dev 17.83
Turn on : 26.7529
Width : 4.078
Height : 10.054
Entry
ampl
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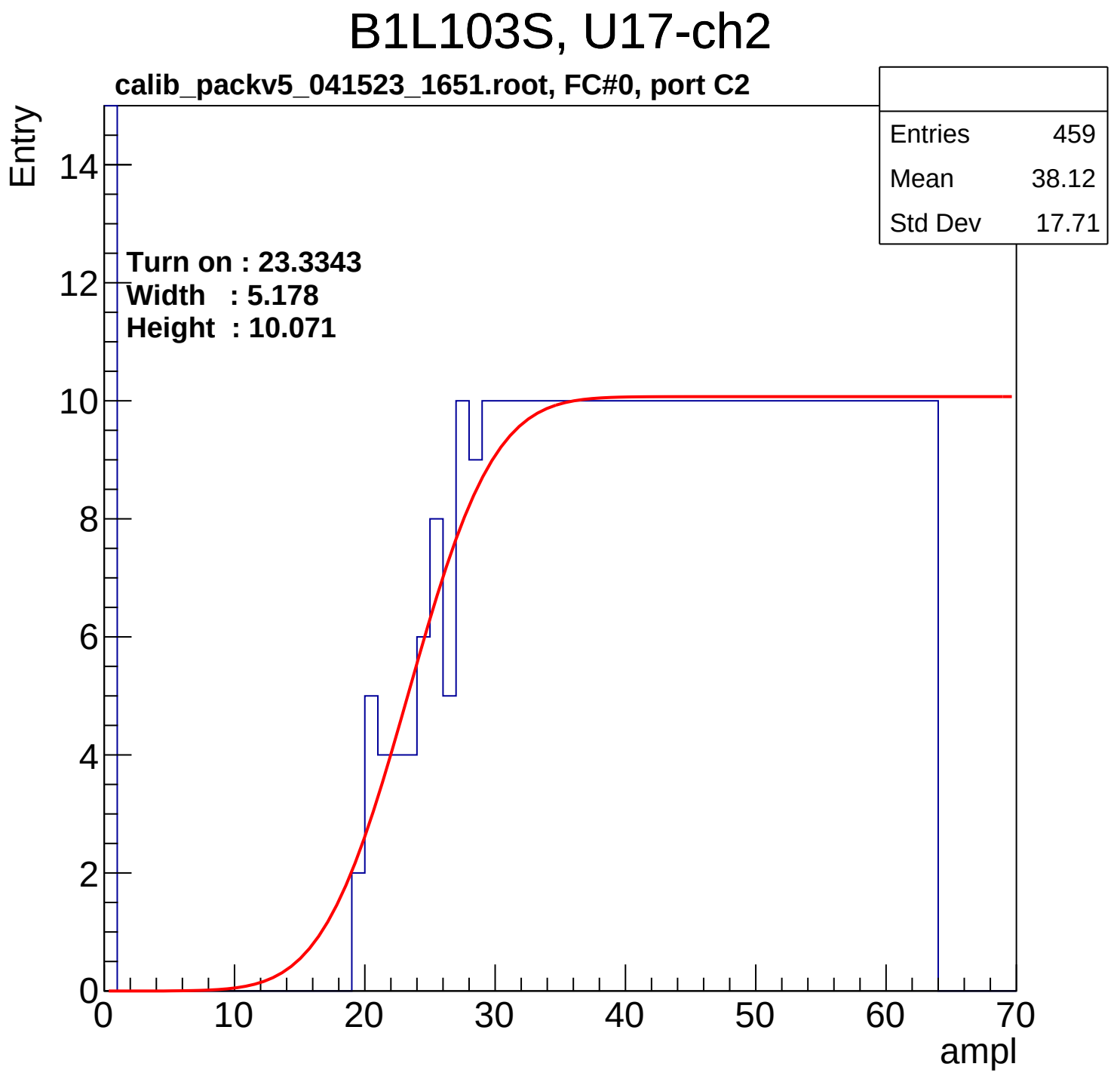
B1L103S, U17-ch2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 459
Mean 38.12
Std Dev 17.71
Turn on : 23.3343
Width : 5.178
Height : 10.071
Entry
ampl
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2
4
6
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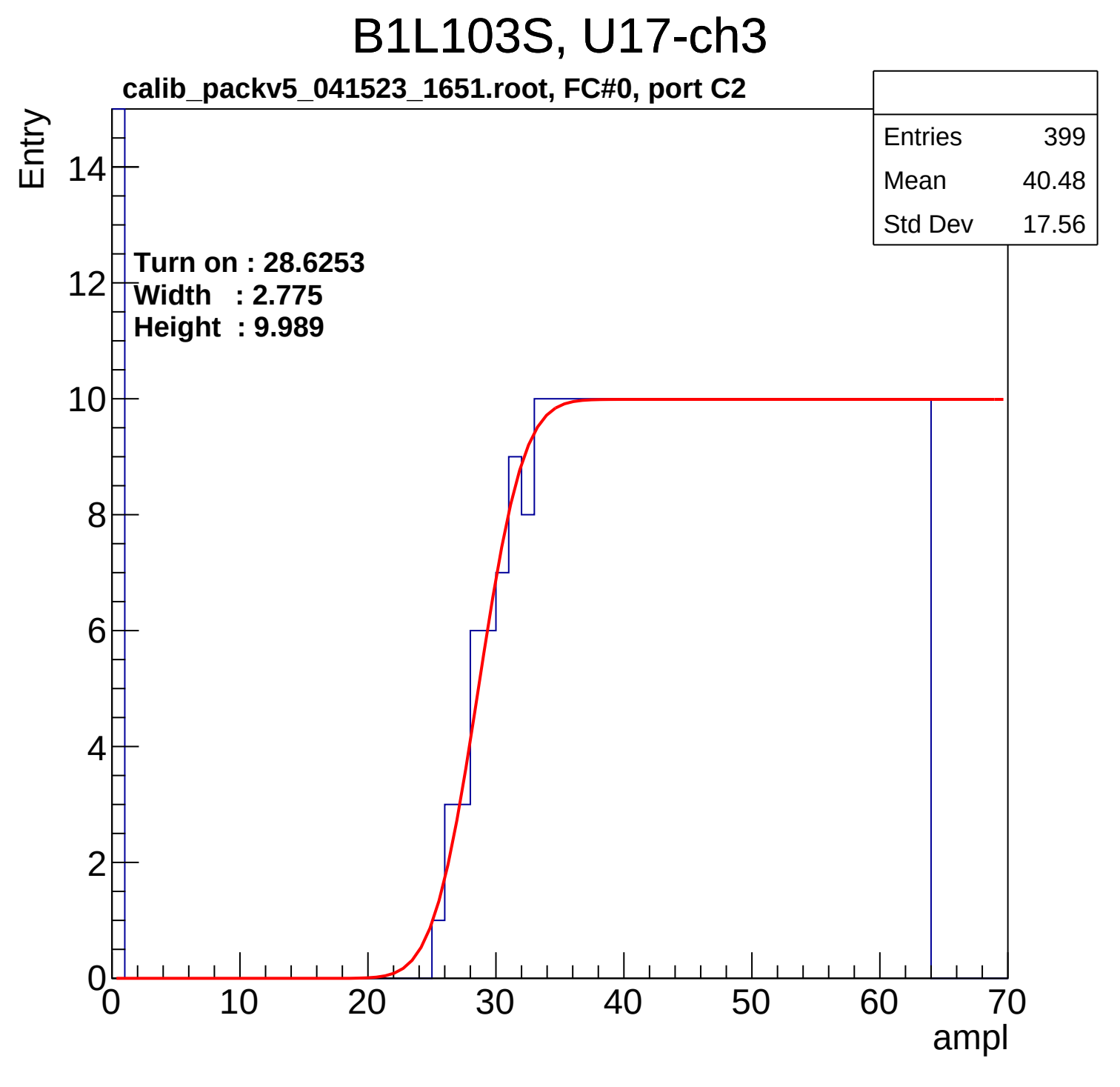
B1L103S, U17-ch3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 399
Mean 40.48
Std Dev 17.56
Turn on : 28.6253
Width : 2.775
Height : 9.989
Entry
ampl
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4
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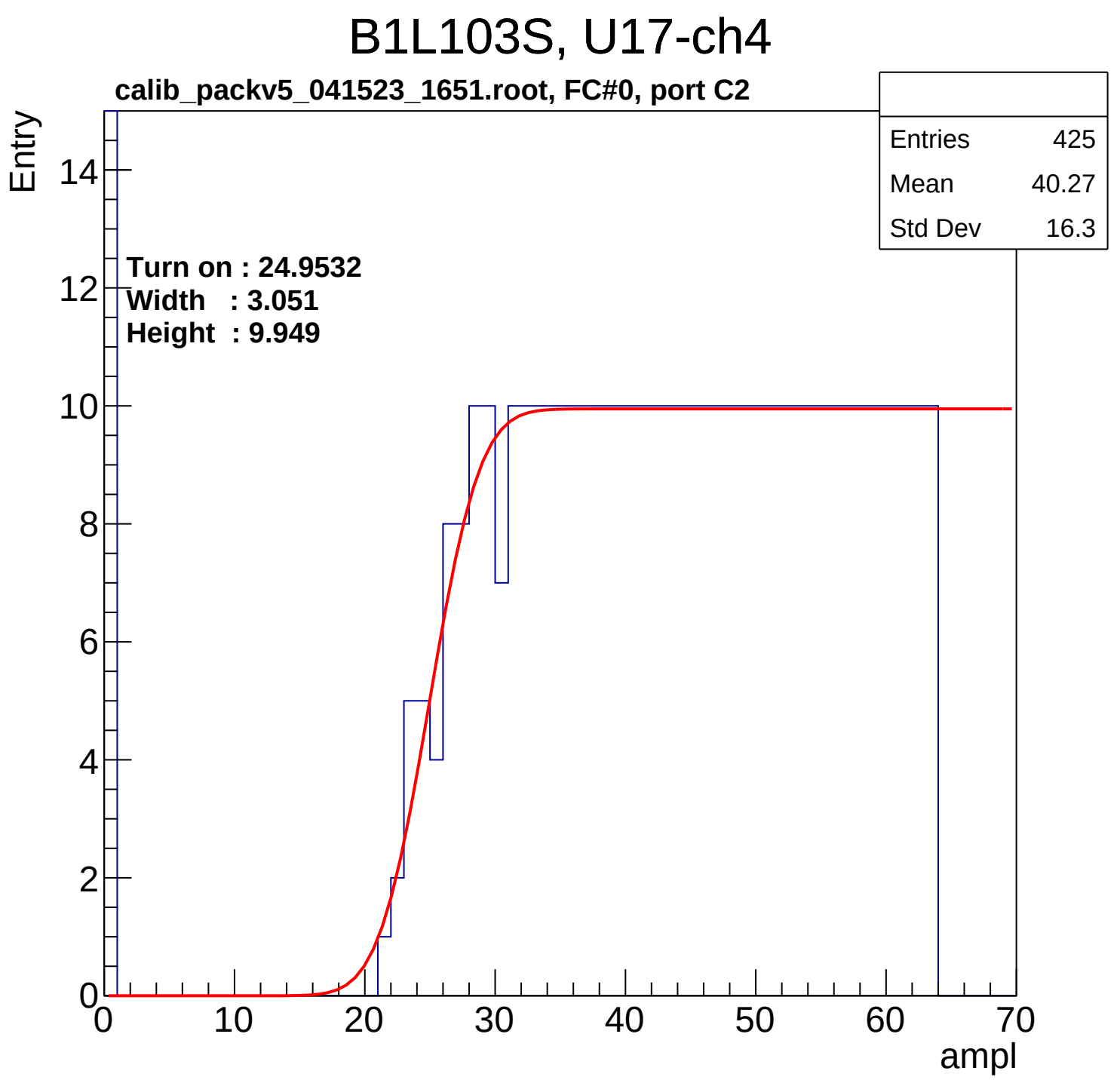
B1L103S, U17-ch4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 425
Mean 40.27
Std Dev 16.3
Turn on : 24.9532
Width : 3.051
Height : 9.949
Entry
ampl
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6
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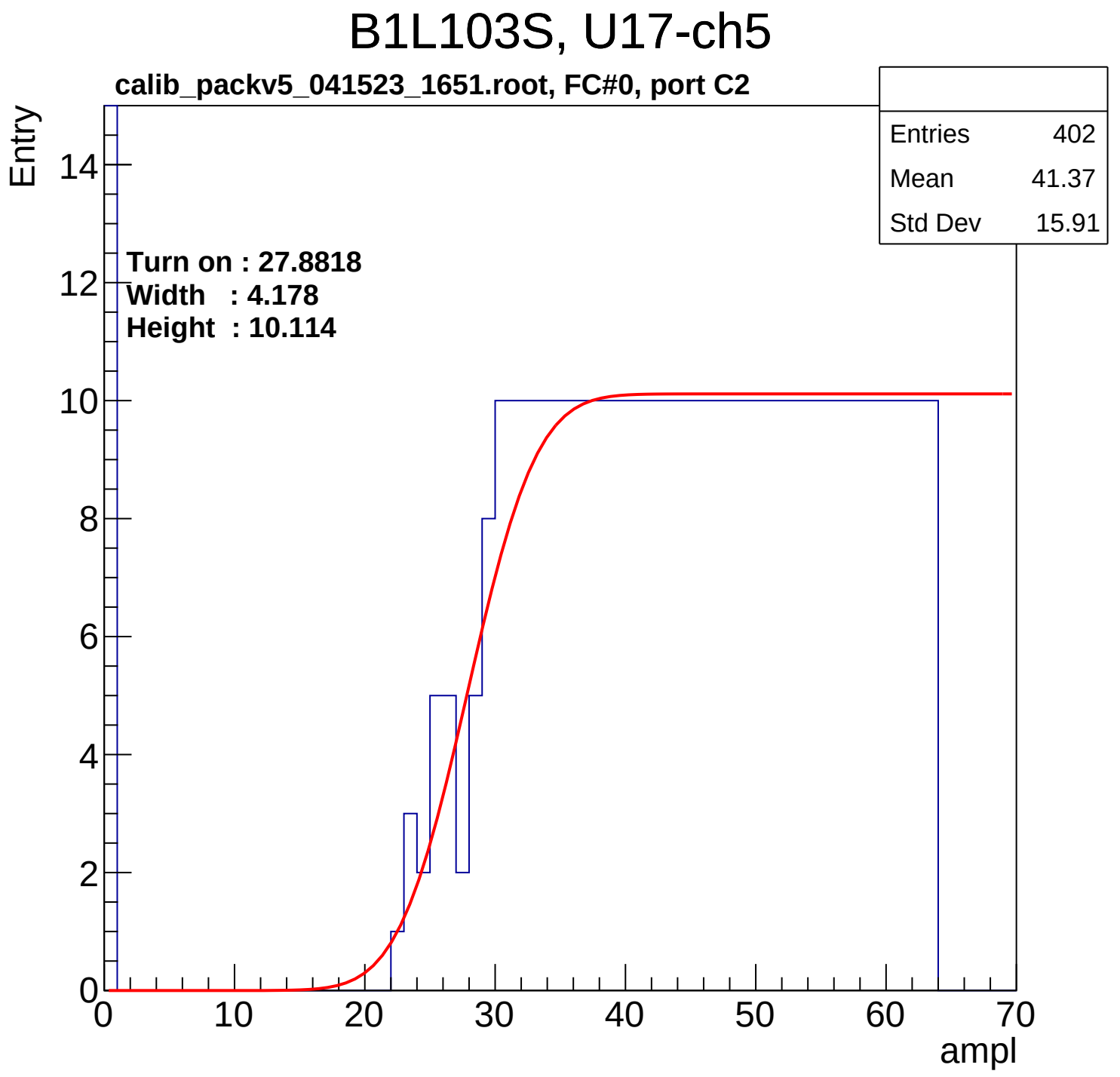
B1L103S, U17-ch5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 402
Mean 41.37
Std Dev 15.91
Turn on : 27.8818
Width : 4.178
Height : 10.114
Entry
ampl
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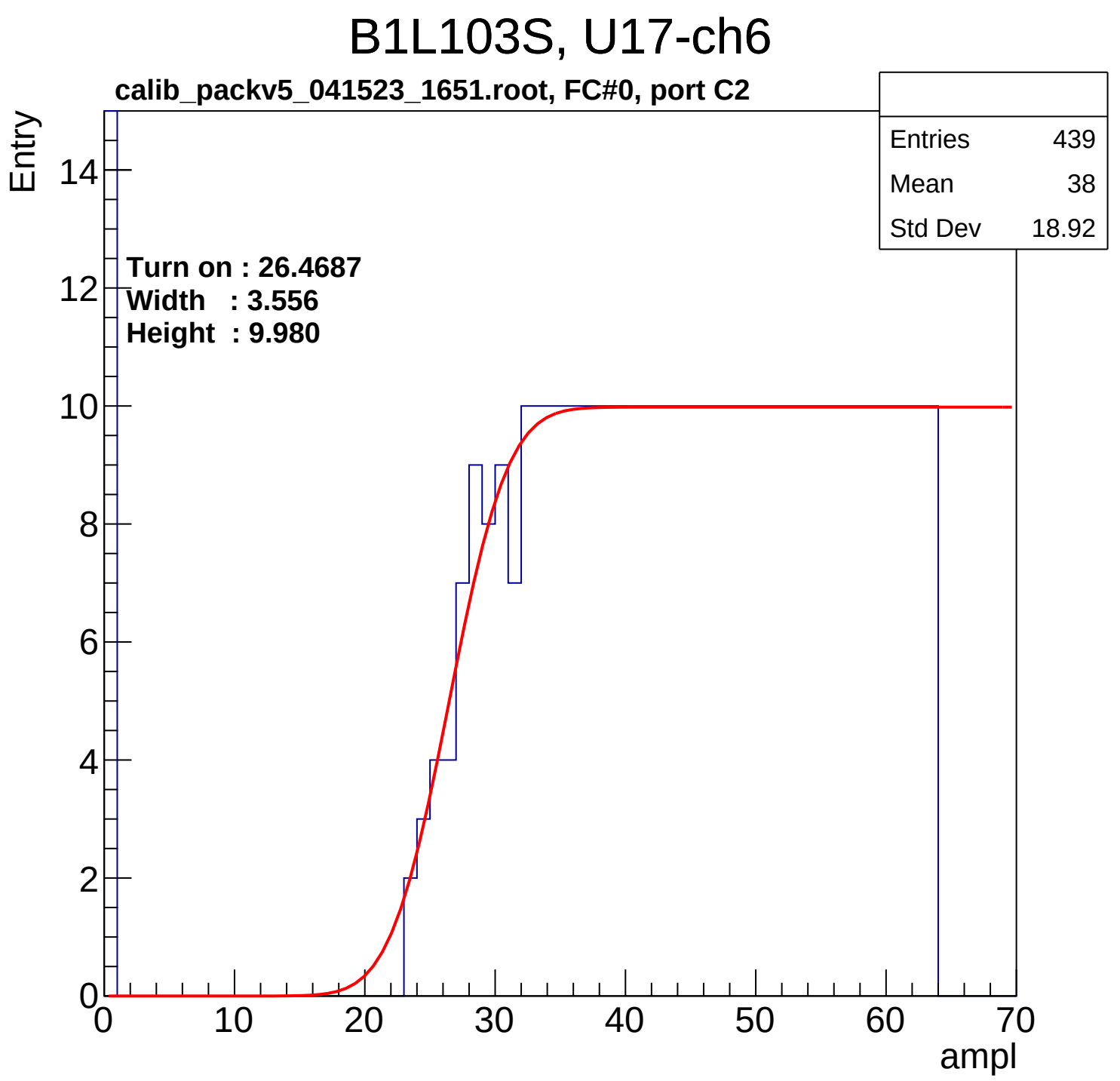
B1L103S, U17-ch6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 439
Mean 38
Std Dev 18.92
Turn on : 26.4687
Width : 3.556
Height : 9.980
Entry
ampl
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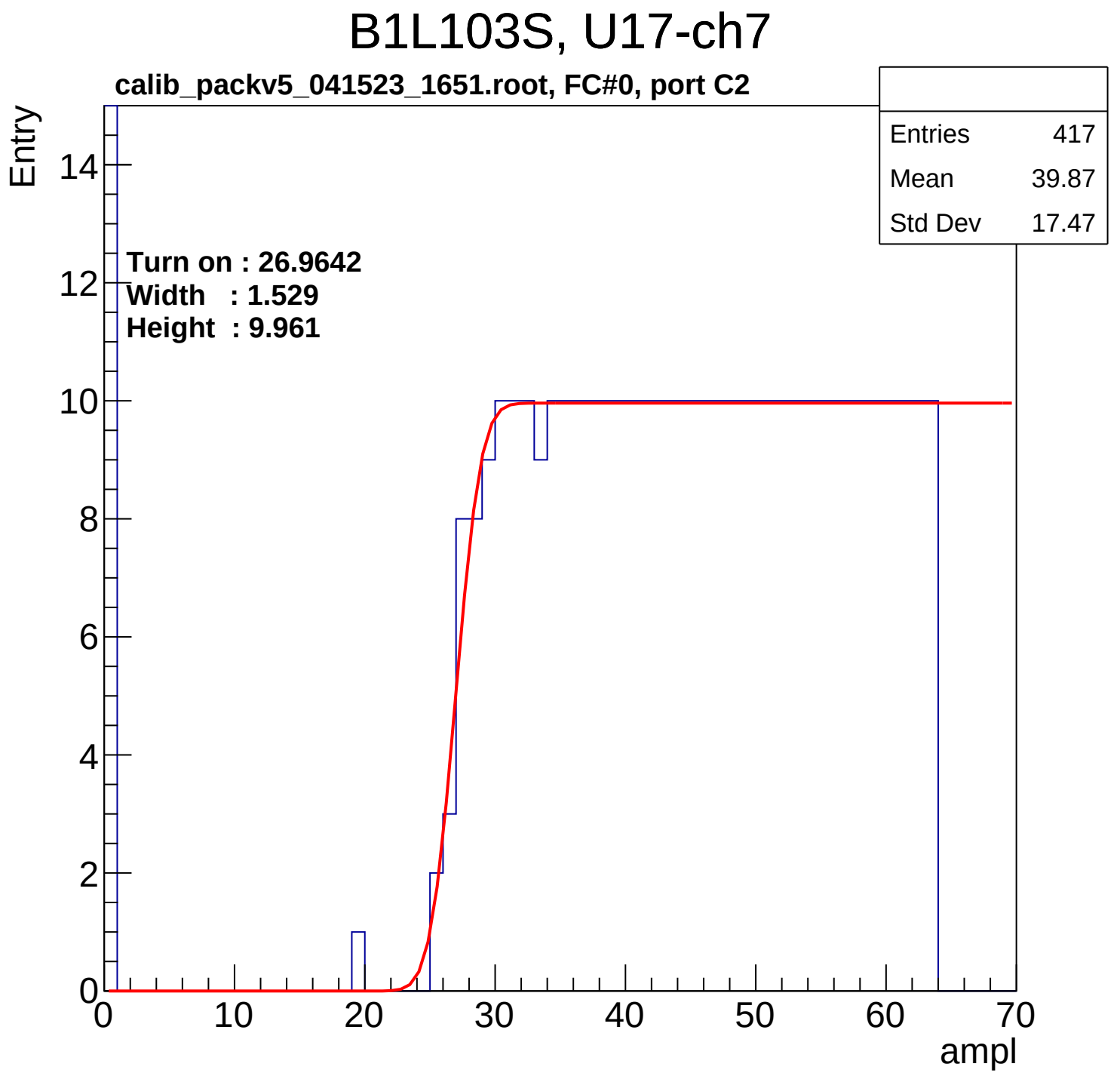
B1L103S, U17-ch7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 417
Mean 39.87
Std Dev 17.47
Turn on : 26.9642
Width : 1.529
Height : 9.961
Entry
ampl
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6
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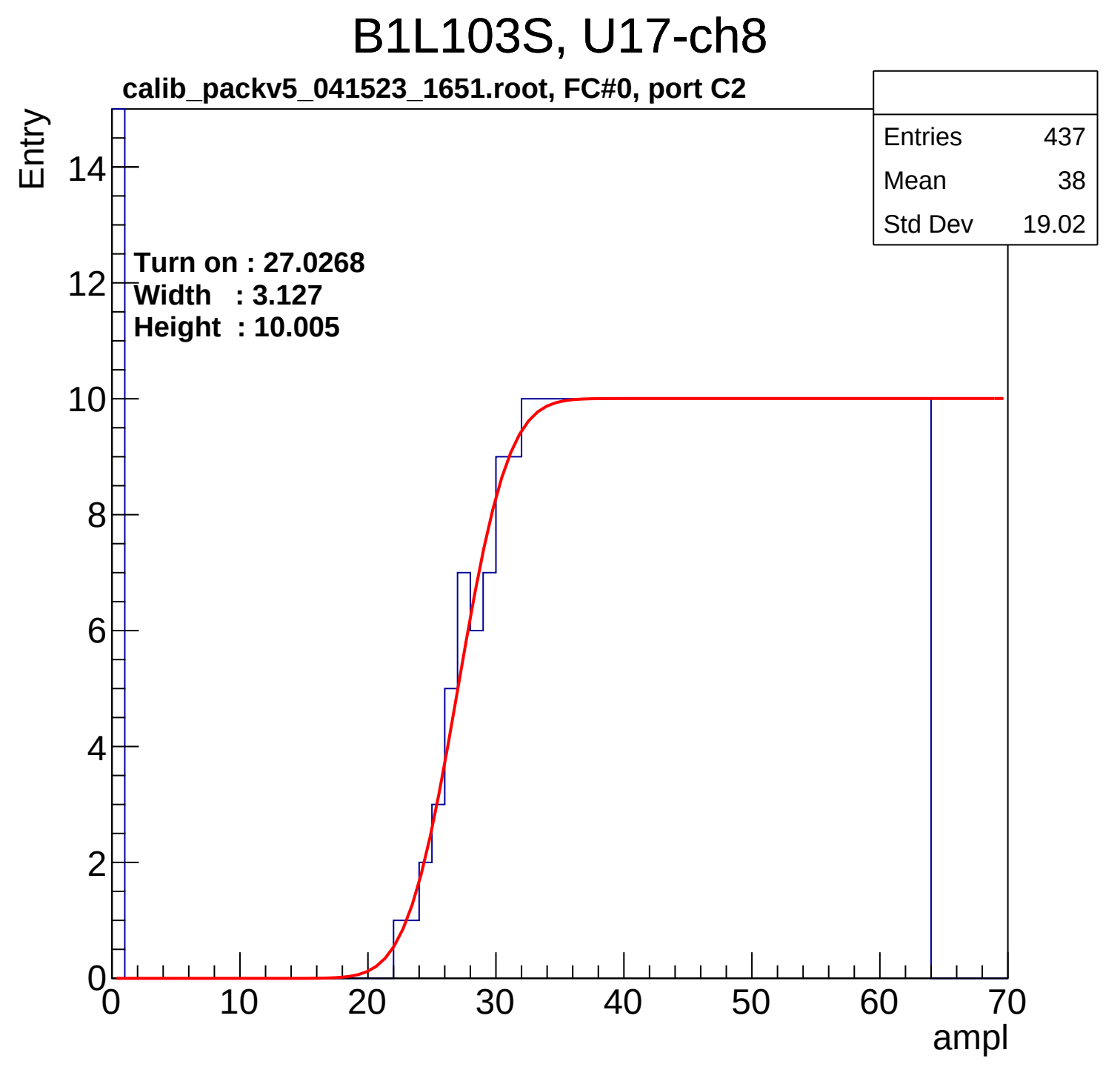
B1L103S, U17-ch8
calib_packv5_041523_1651.root, FC#0, port C2
Entries 437
Mean 38
Std Dev 19.02
Turn on : 27.0268
Width : 3.127
Height : 10.005
Entry
ampl
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6
8
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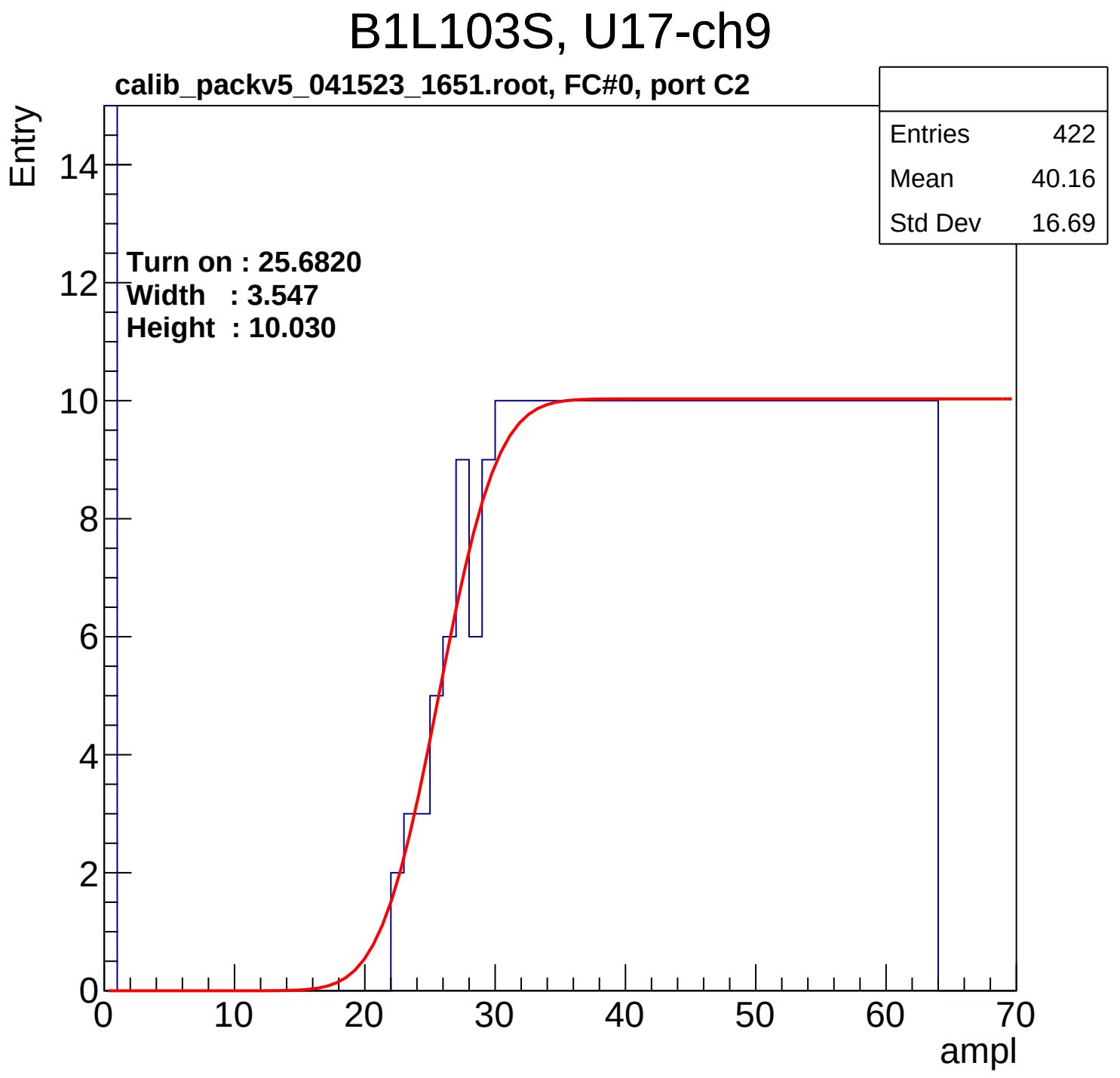
B1L103S, U17-ch9
calib_packv5_041523_1651.root, FC#0, port C2
Entries 422
Mean 40.16
Std Dev 16.69
Turn on : 25.6820
Width : 3.547
Height : 10.030
Entry
ampl
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6
8
10
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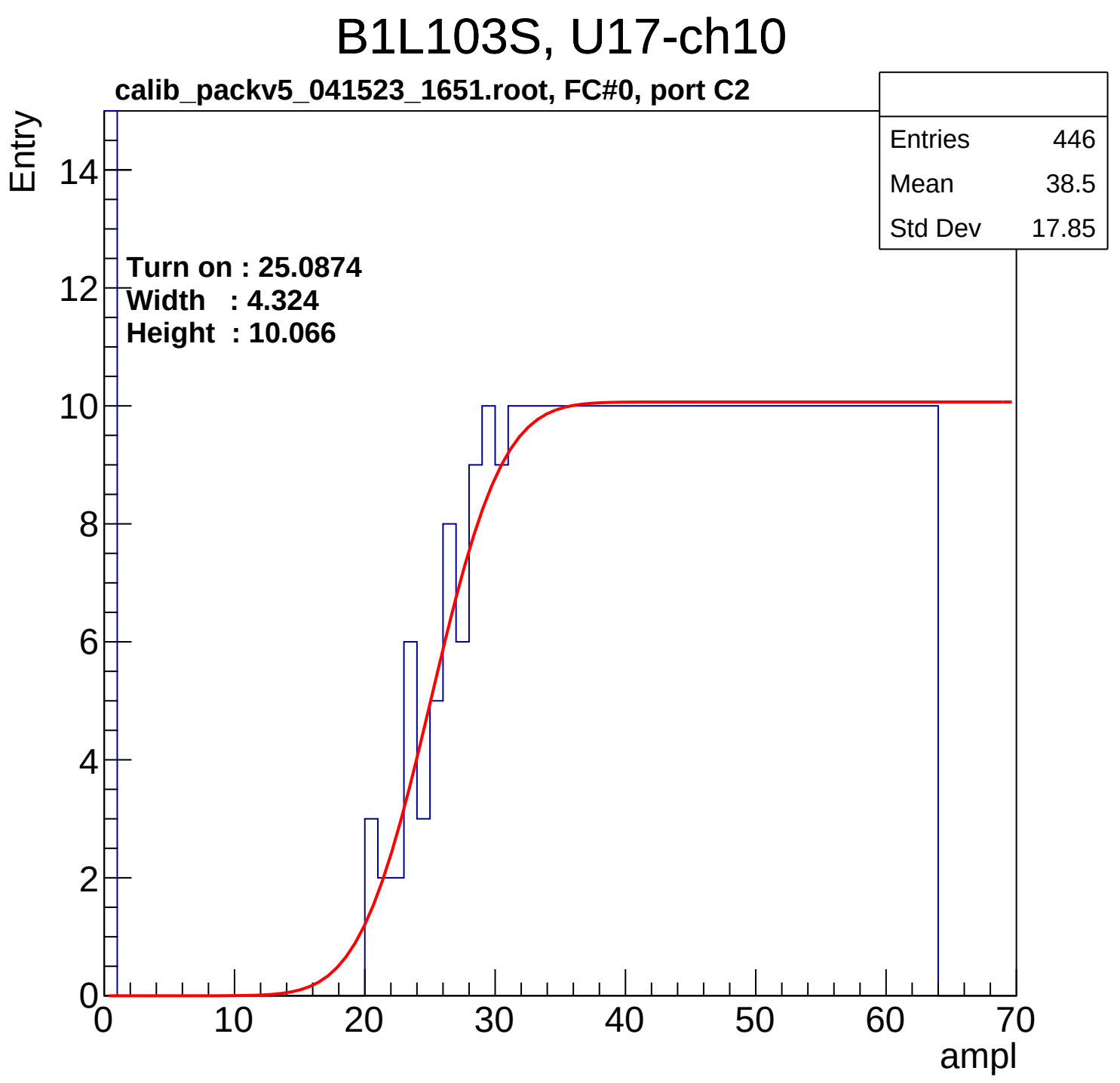
B1L103S, U17-ch10
calib_packv5_041523_1651.root, FC#0, port C2
Entries 446
Mean 38.5
Std Dev 17.85
Turn on : 25.0874
Width : 4.324
Height : 10.066
Entry
ampl
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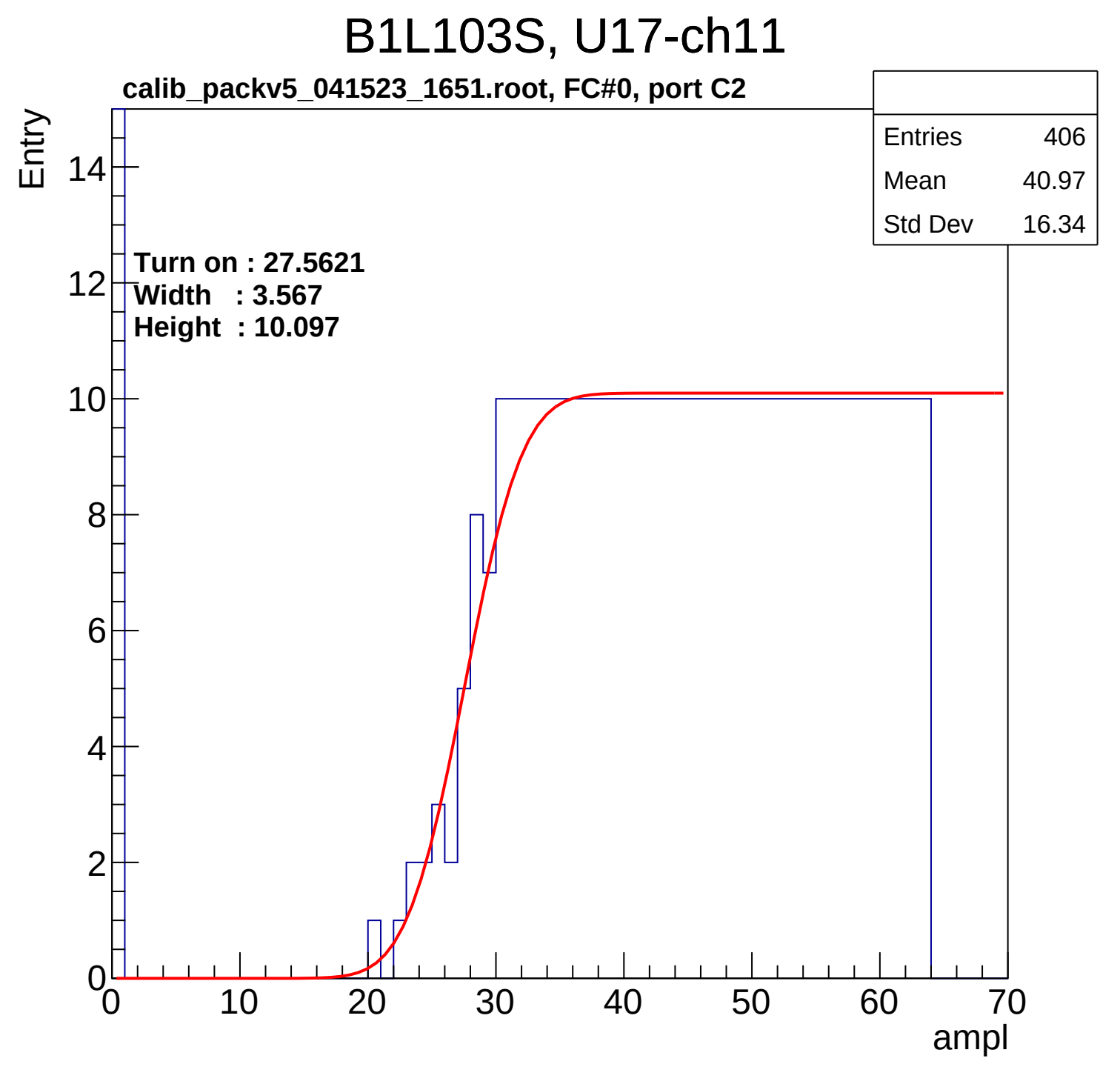
B1L103S, U17-ch11
calib_packv5_041523_1651.root, FC#0, port C2
Entries 406
Mean 40.97
Std Dev 16.34
Turn on : 27.5621
Width : 3.567
Height : 10.097
Entry
ampl
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8
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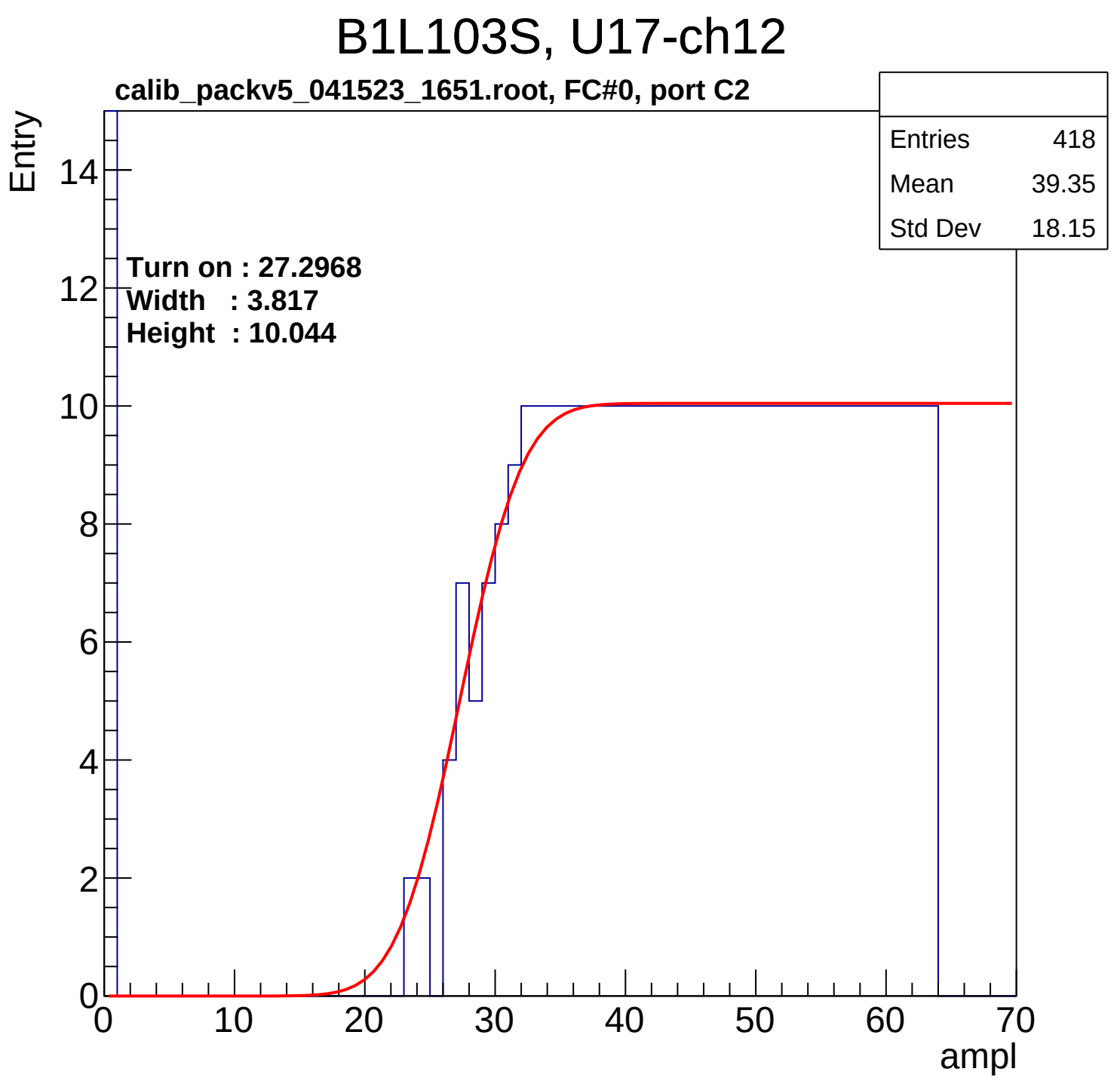
B1L103S, U17-ch12
calib_packv5_041523_1651.root, FC#0, port C2
Entries 418
Mean 39.35
Std Dev 18.15
Turn on : 27.2968
Width : 3.817
Height : 10.044
Entry
ampl
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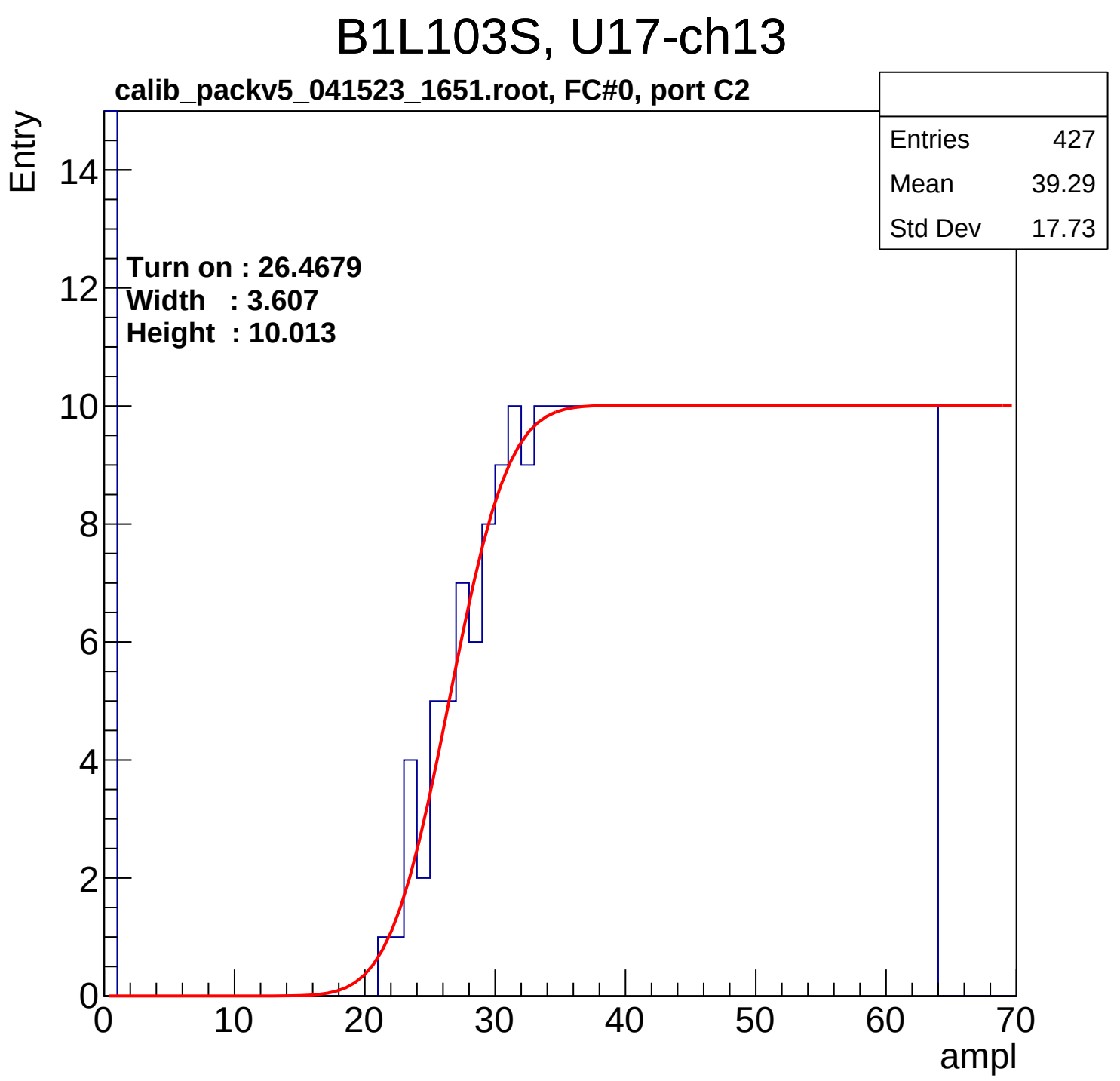
B1L103S, U17-ch13
calib_packv5_041523_1651.root, FC#0, port C2
Entries 427
Mean 39.29
Std Dev 17.73
Turn on : 26.4679
Width : 3.607
Height : 10.013
Entry
ampl
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6
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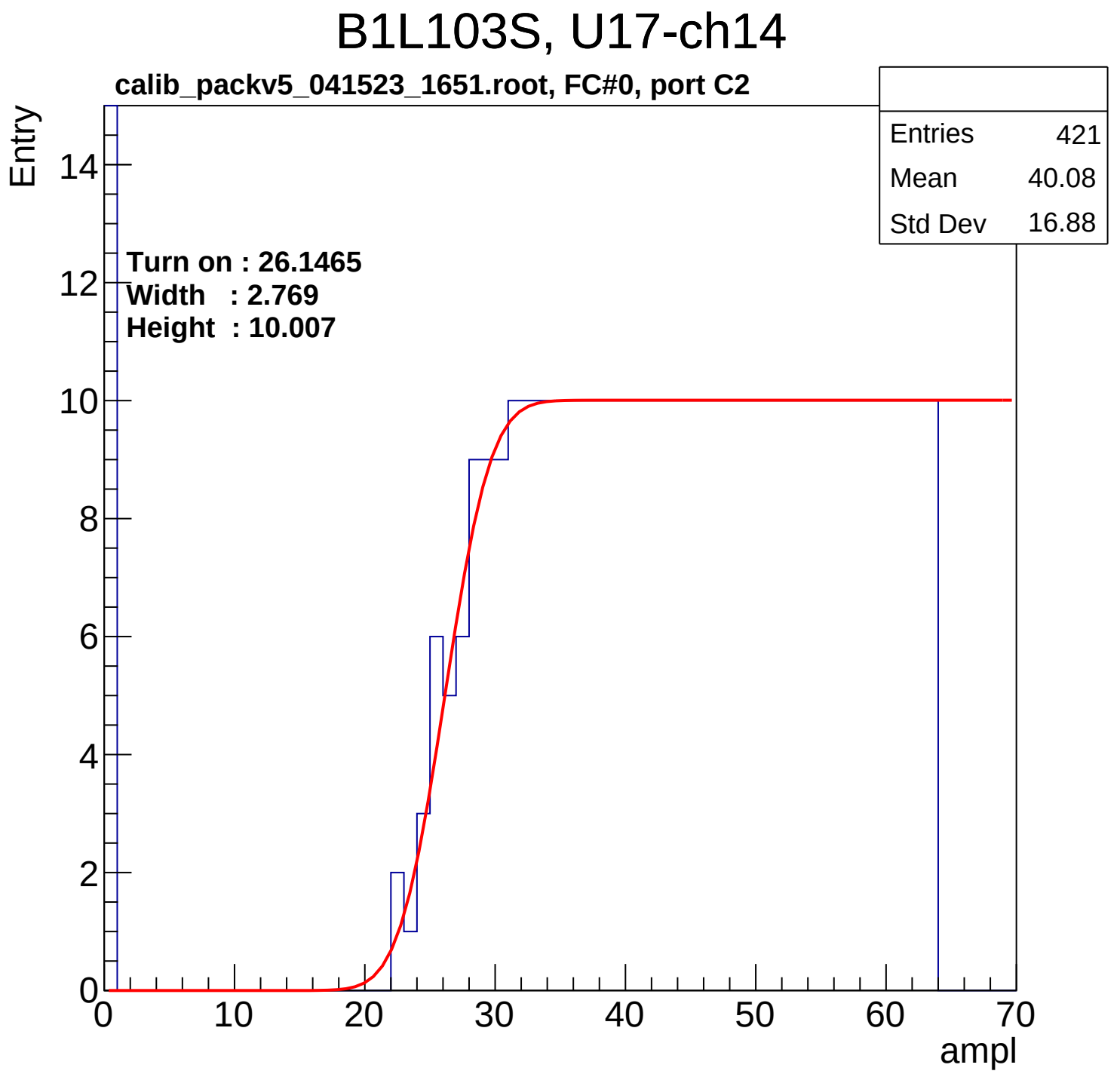
B1L103S, U17-ch14
calib_packv5_041523_1651.root, FC#0, port C2
Entries 421
Mean 40.08
Std Dev 16.88
Turn on : 26.1465
Width : 2.769
Height : 10.007
Entry
ampl
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6
8
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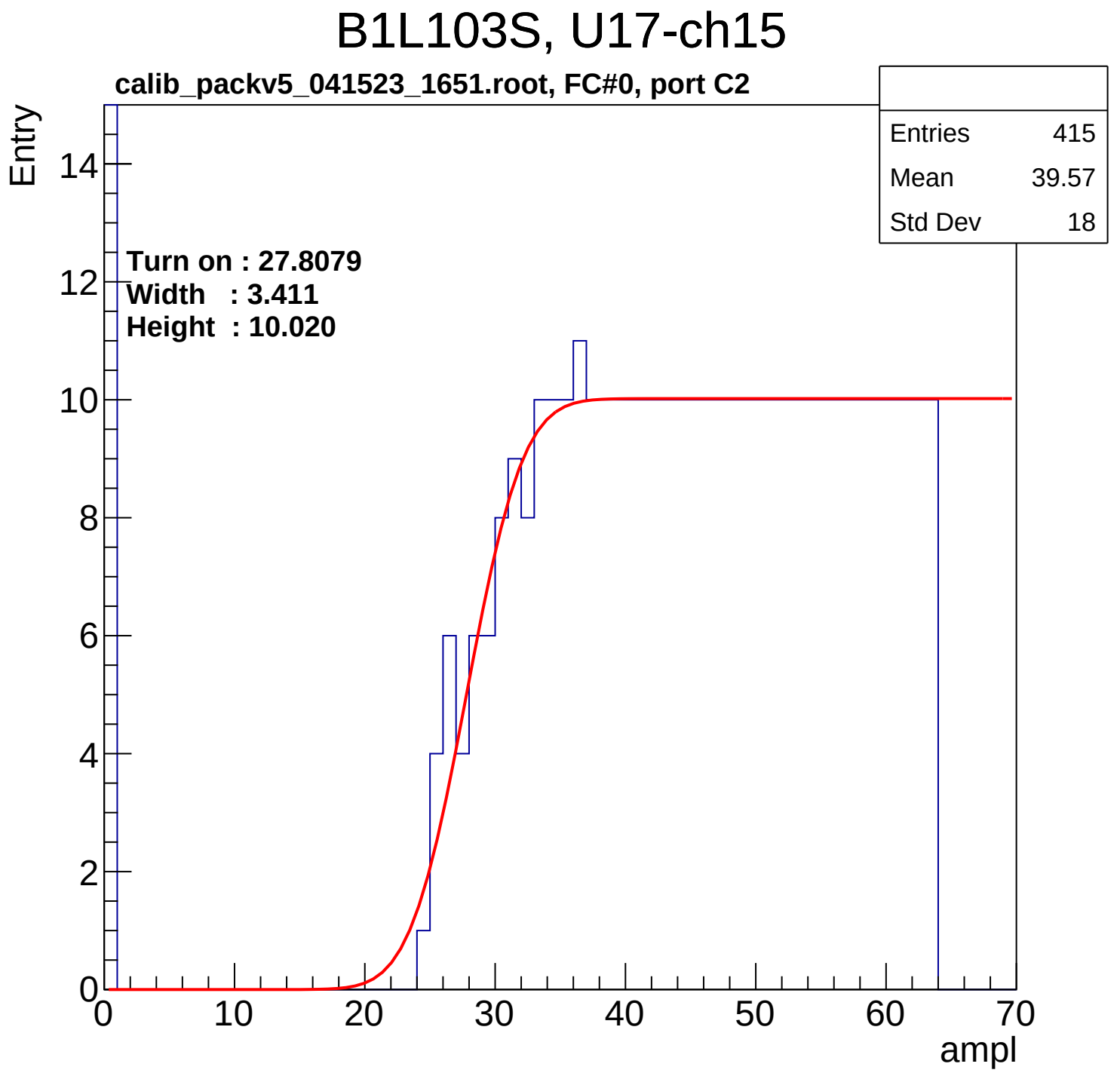
B1L103S, U17-ch15
calib_packv5_041523_1651.root, FC#0, port C2
Entries 415
Mean 39.57
Std Dev 18
Turn on : 27.8079
Width : 3.411
Height : 10.020
Entry
ampl
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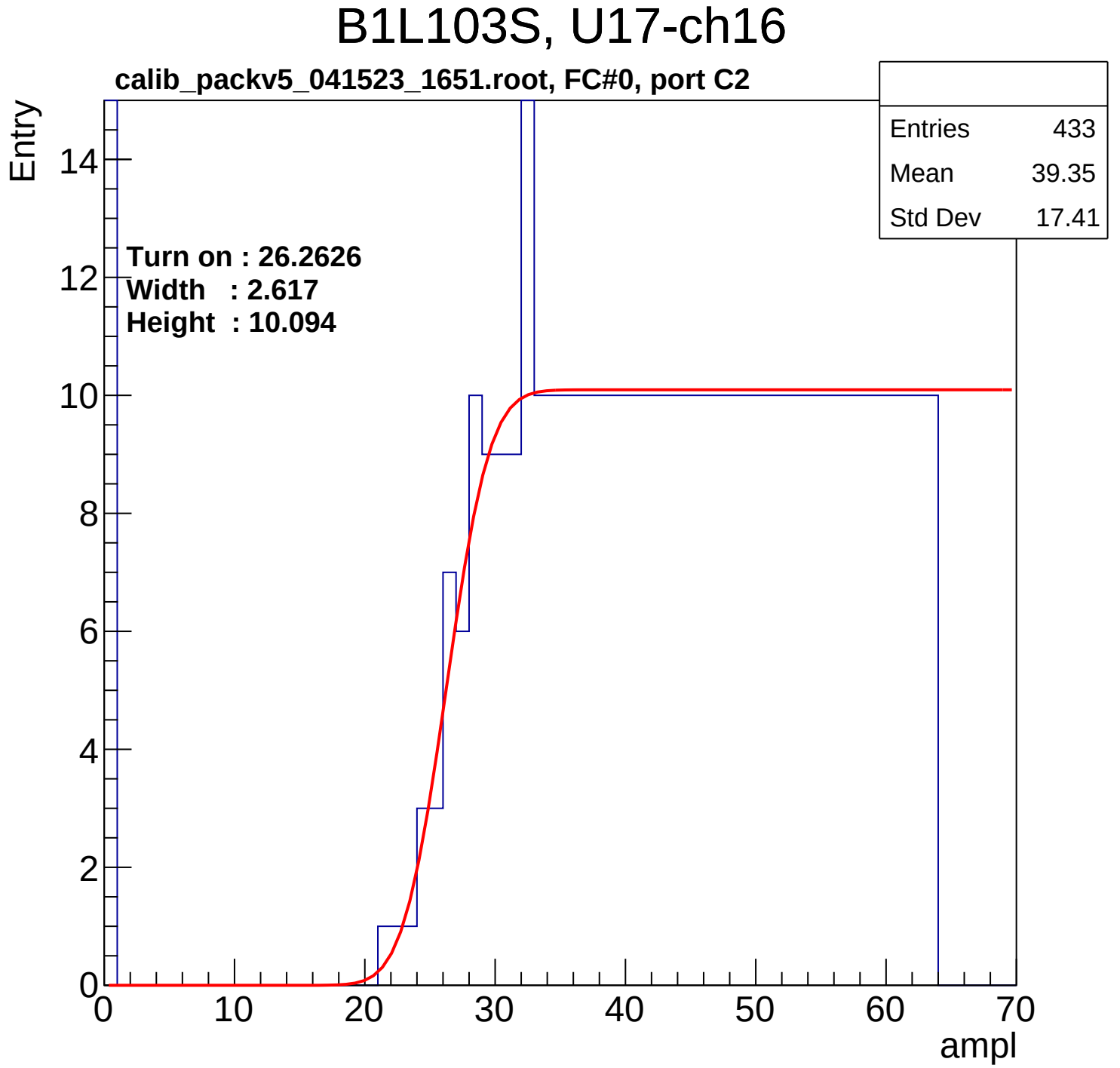
B1L103S, U17-ch16
calib_packv5_041523_1651.root, FC#0, port C2
Entries 433
Mean 39.35
Std Dev 17.41
Turn on : 26.2626
Width : 2.617
Height : 10.094
Entry
ampl
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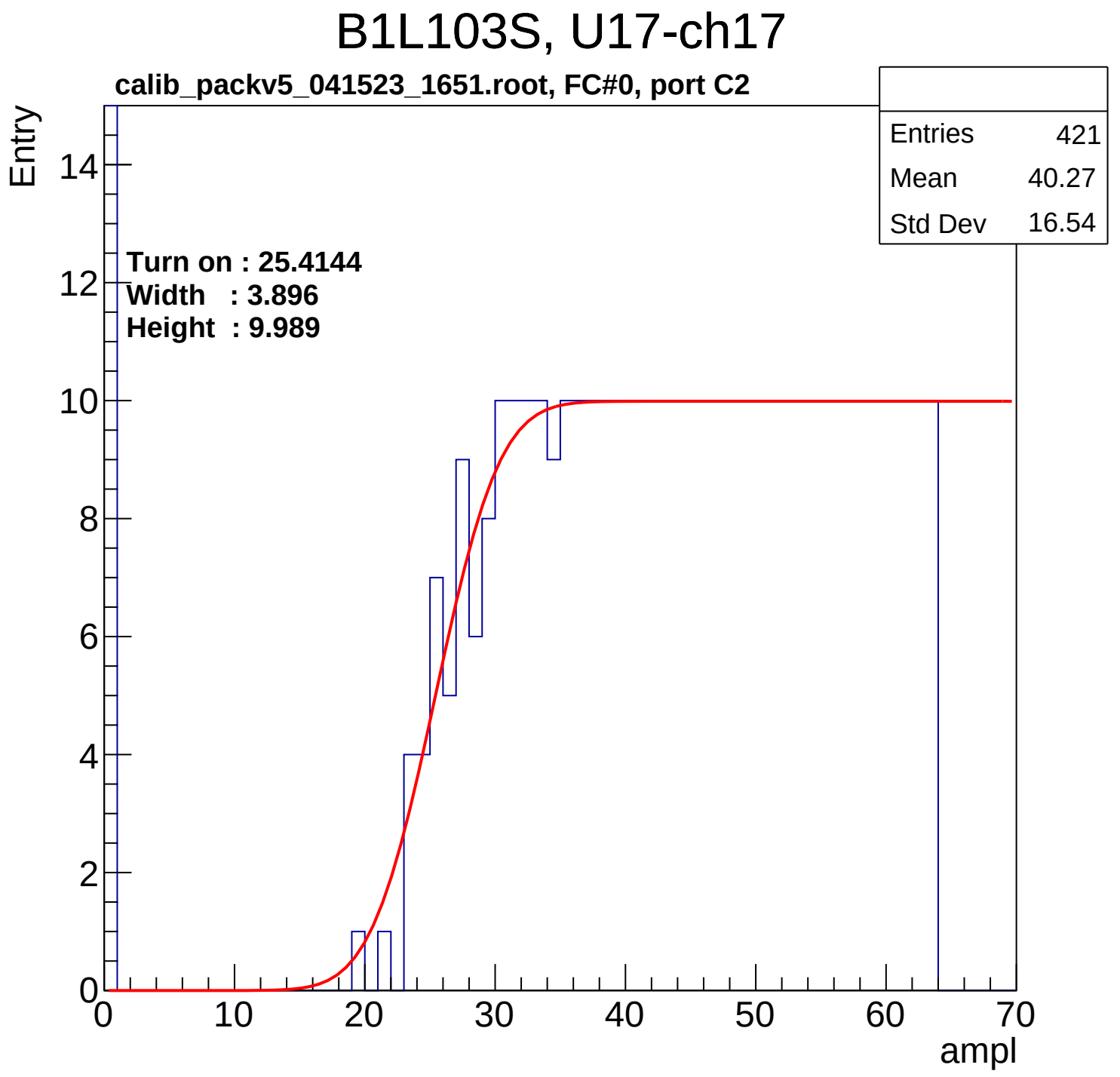
B1L103S, U17-ch17
calib_packv5_041523_1651.root, FC#0, port C2
Entries 421
Mean 40.27
Std Dev 16.54
Turn on : 25.4144
Width : 3.896
Height : 9.989
Entry
ampl
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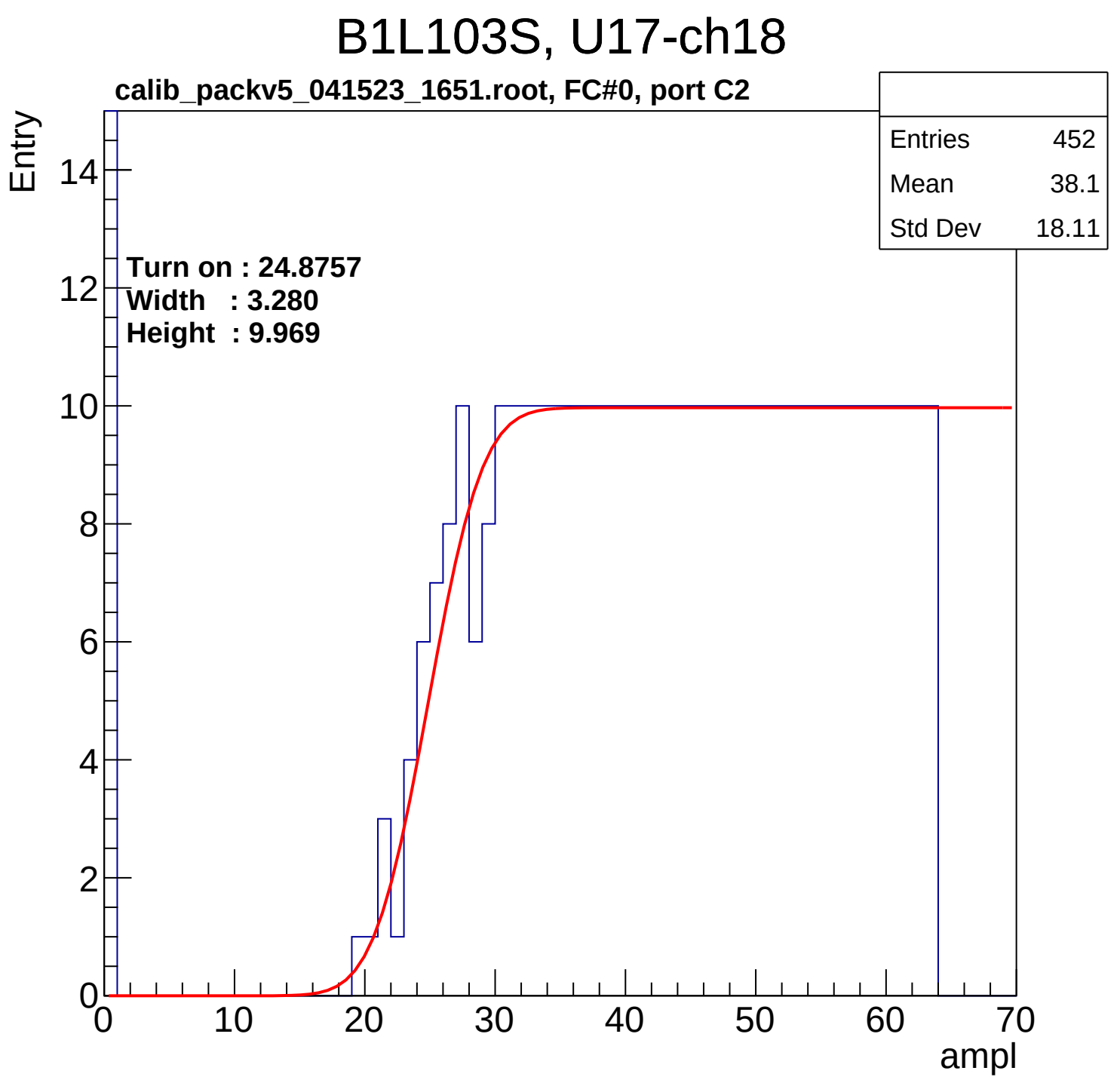
B1L103S, U17-ch18
calib_packv5_041523_1651.root, FC#0, port C2
Entries 452
Mean 38.1
Std Dev 18.11
Turn on : 24.8757
Width : 3.280
Height : 9.969
Entry
ampl
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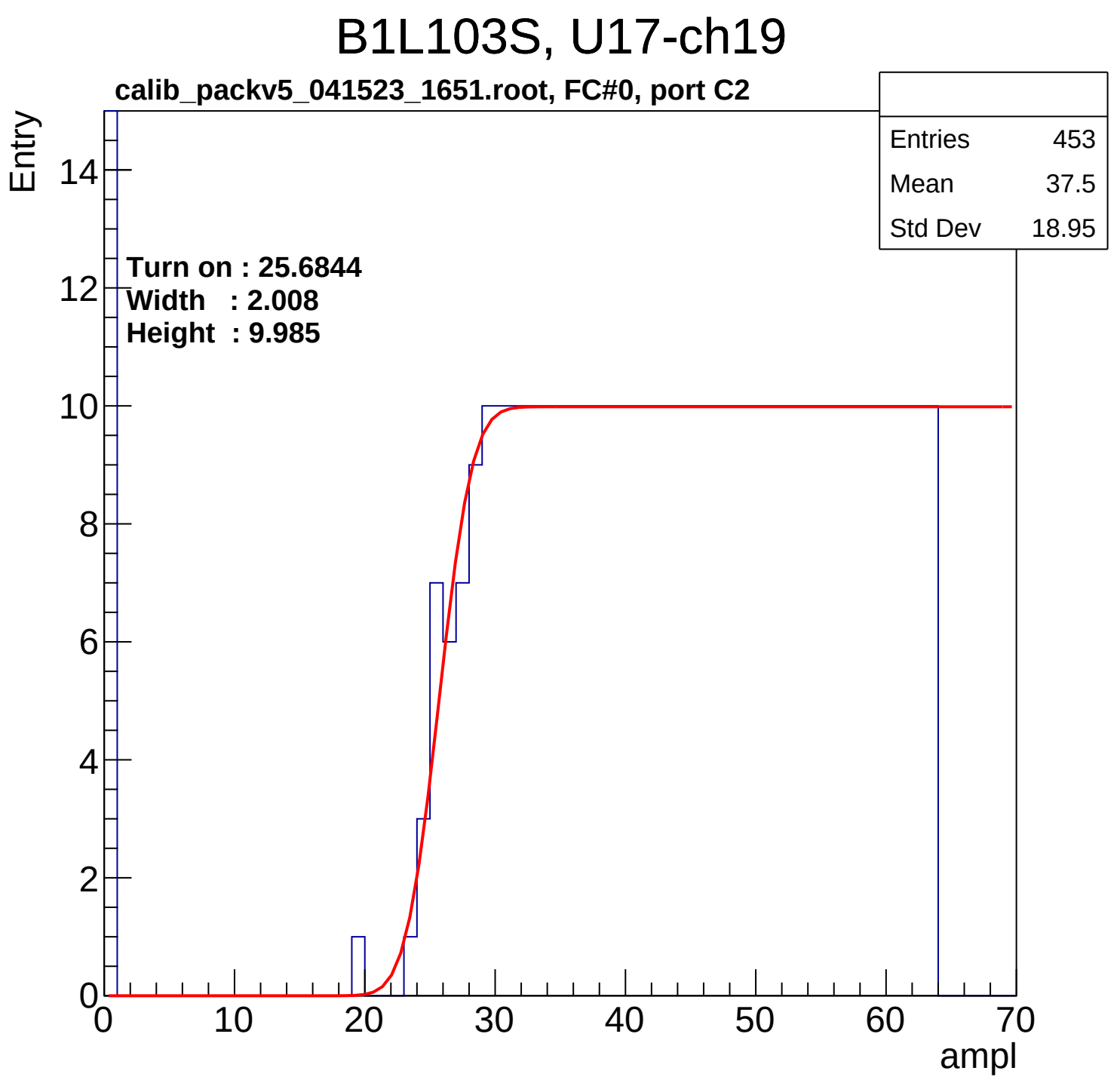
B1L103S, U17-ch19
calib_packv5_041523_1651.root, FC#0, port C2
Entries 453
Mean 37.5
Std Dev 18.95
Turn on : 25.6844
Width : 2.008
Height : 9.985
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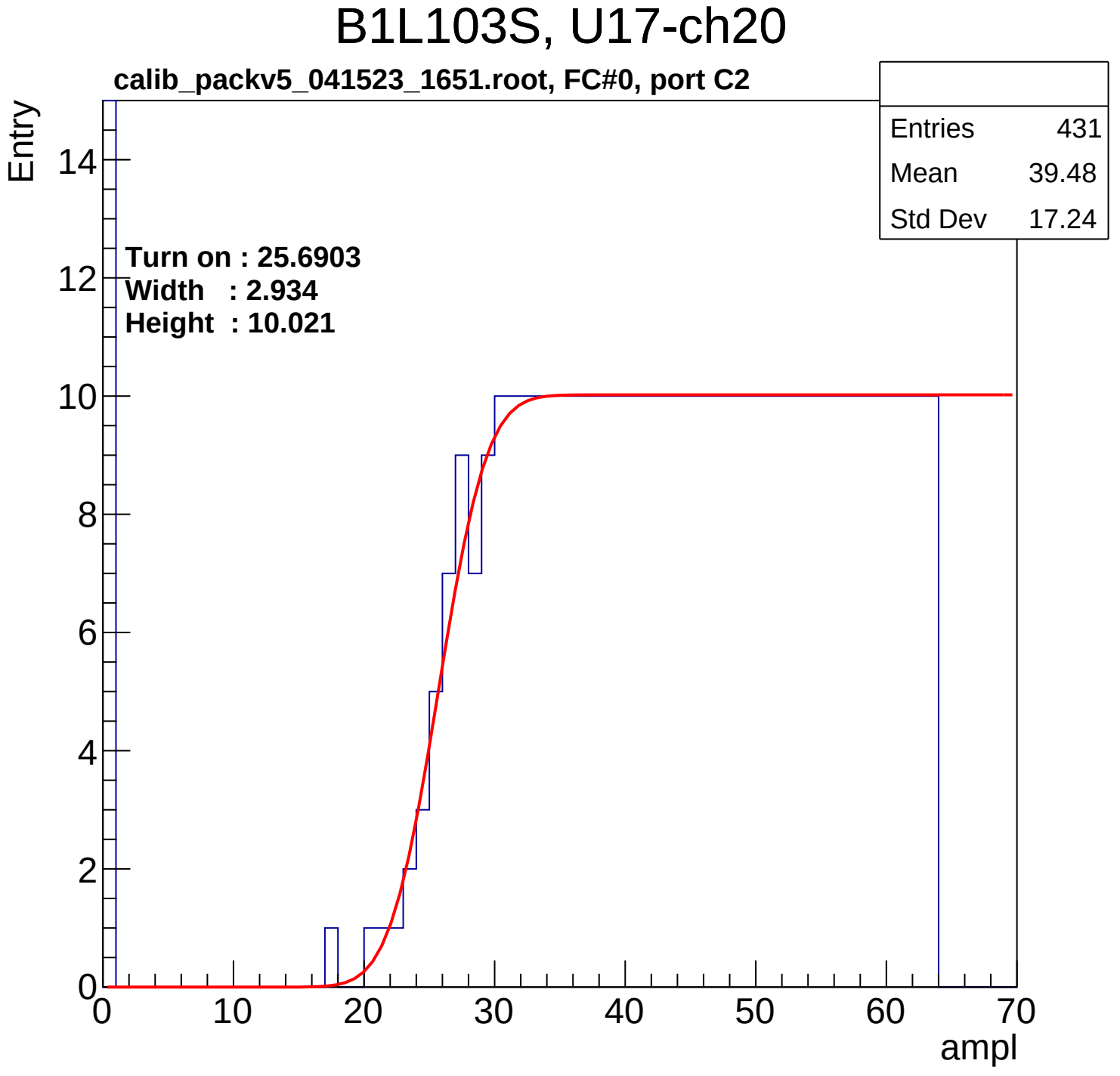
B1L103S, U17-ch20
calib_packv5_041523_1651.root, FC#0, port C2
Entries 431
Mean 39.48
Std Dev 17.24
Turn on : 25.6903
Width : 2.934
Height : 10.021
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ampl
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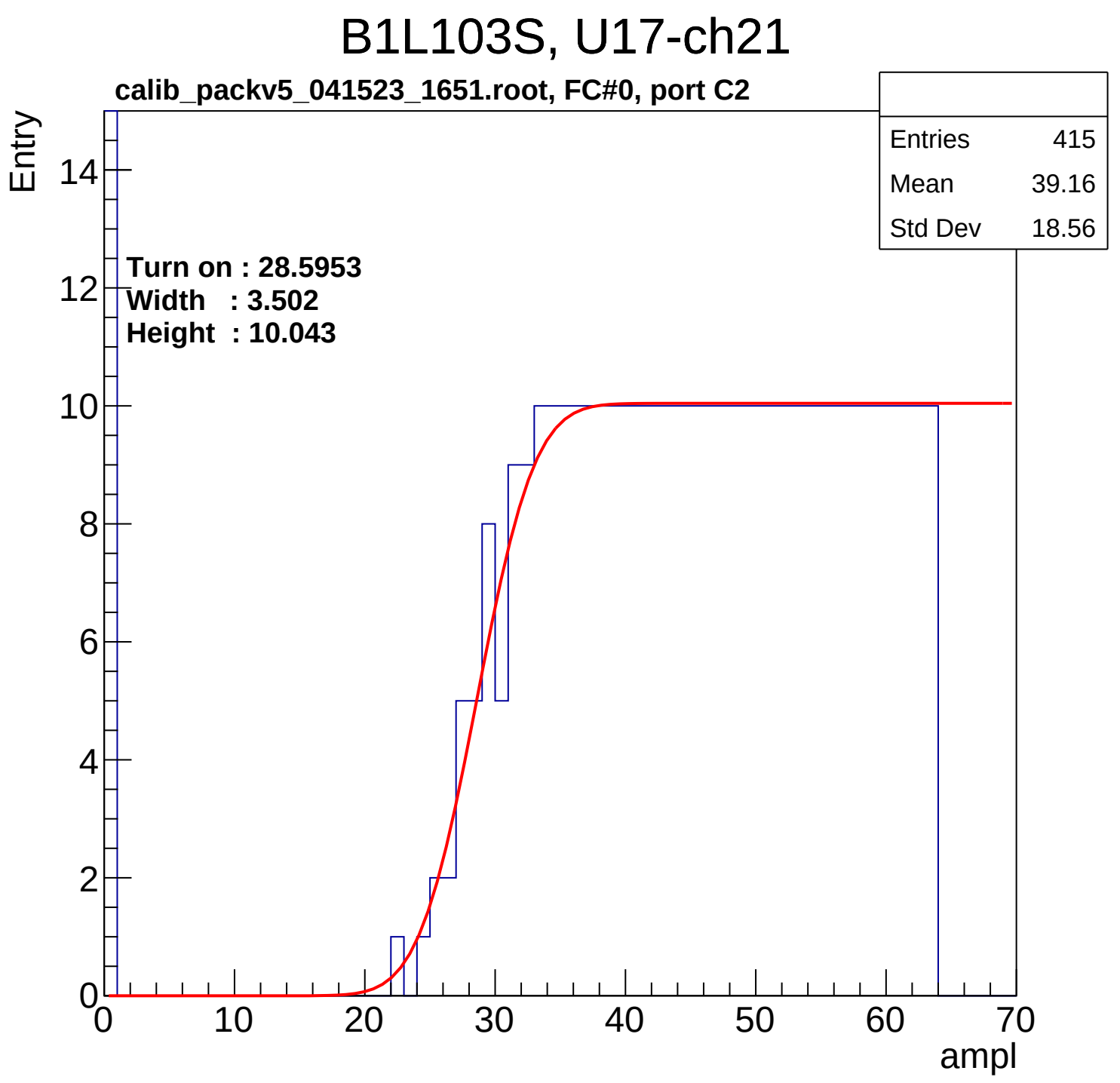
B1L103S, U17-ch21
calib_packv5_041523_1651.root, FC#0, port C2
Entries 415
Mean 39.16
Std Dev 18.56
Turn on : 28.5953
Width : 3.502
Height : 10.043
Entry
ampl
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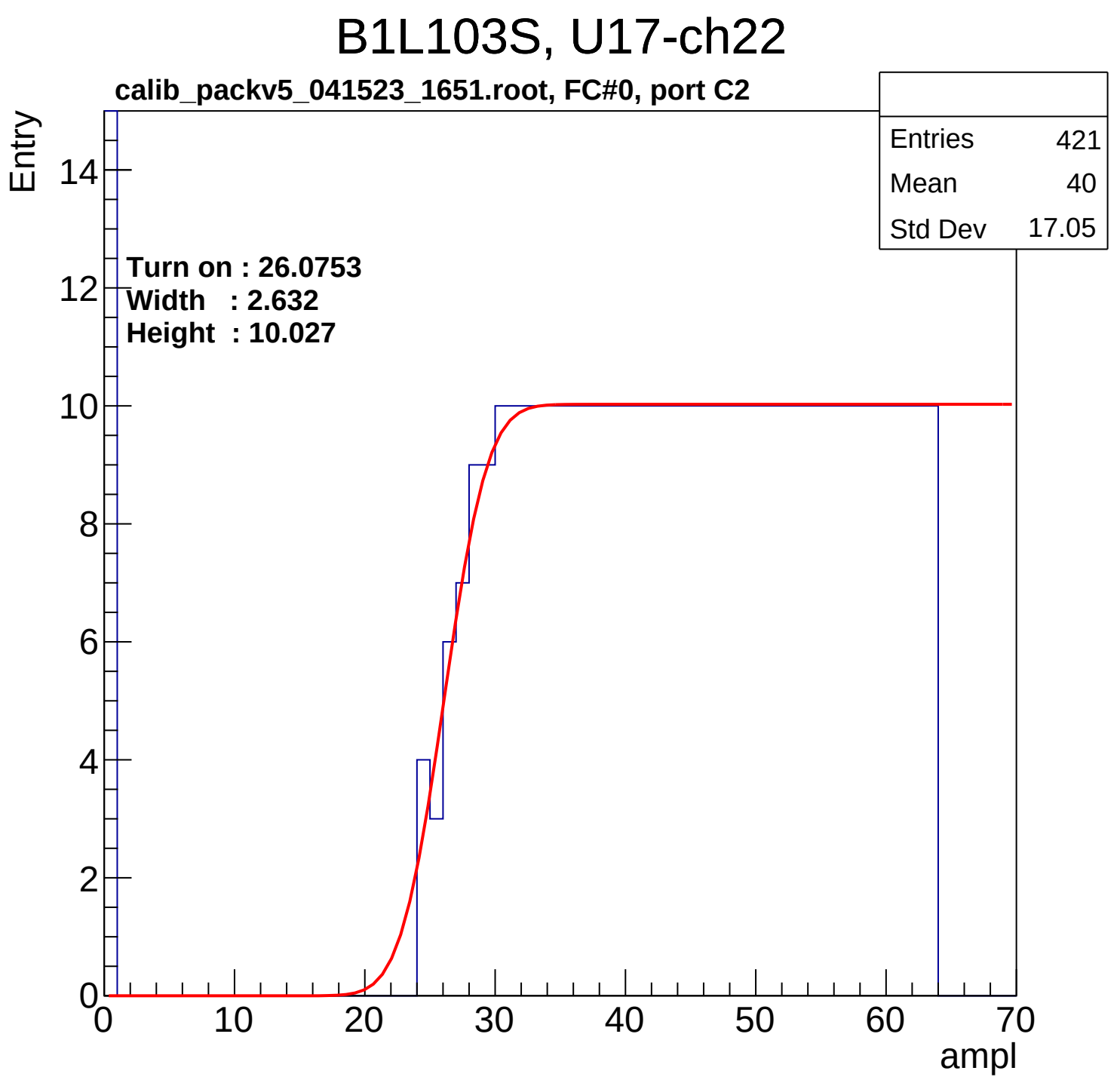
B1L103S, U17-ch22
calib_packv5_041523_1651.root, FC#0, port C2
Entries 421
Mean 40
Std Dev 17.05
Turn on : 26.0753
Width : 2.632
Height : 10.027
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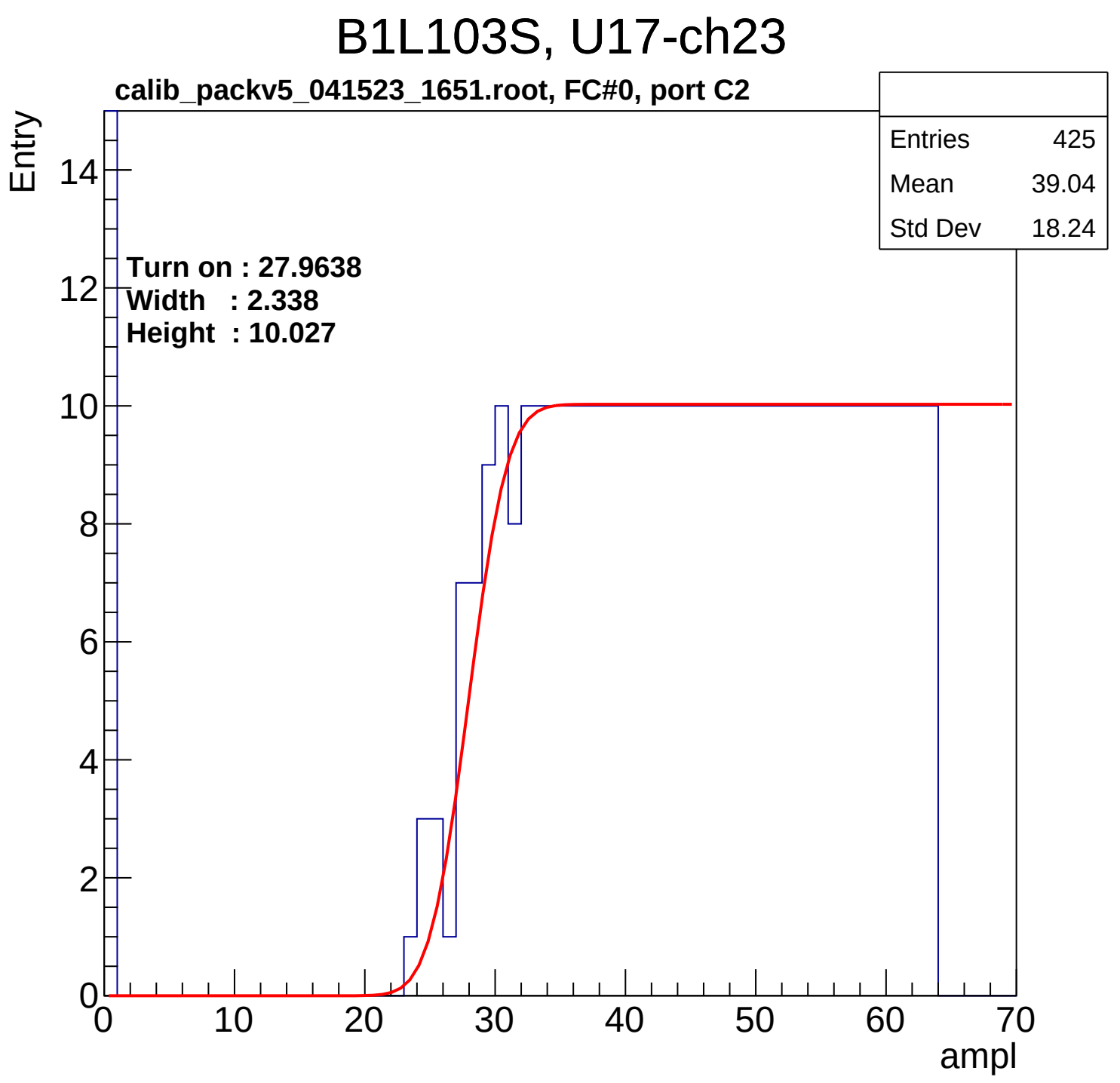
B1L103S, U17-ch23
calib_packv5_041523_1651.root, FC#0, port C2
Entries 425
Mean 39.04
Std Dev 18.24
Turn on : 27.9638
Width : 2.338
Height : 10.027
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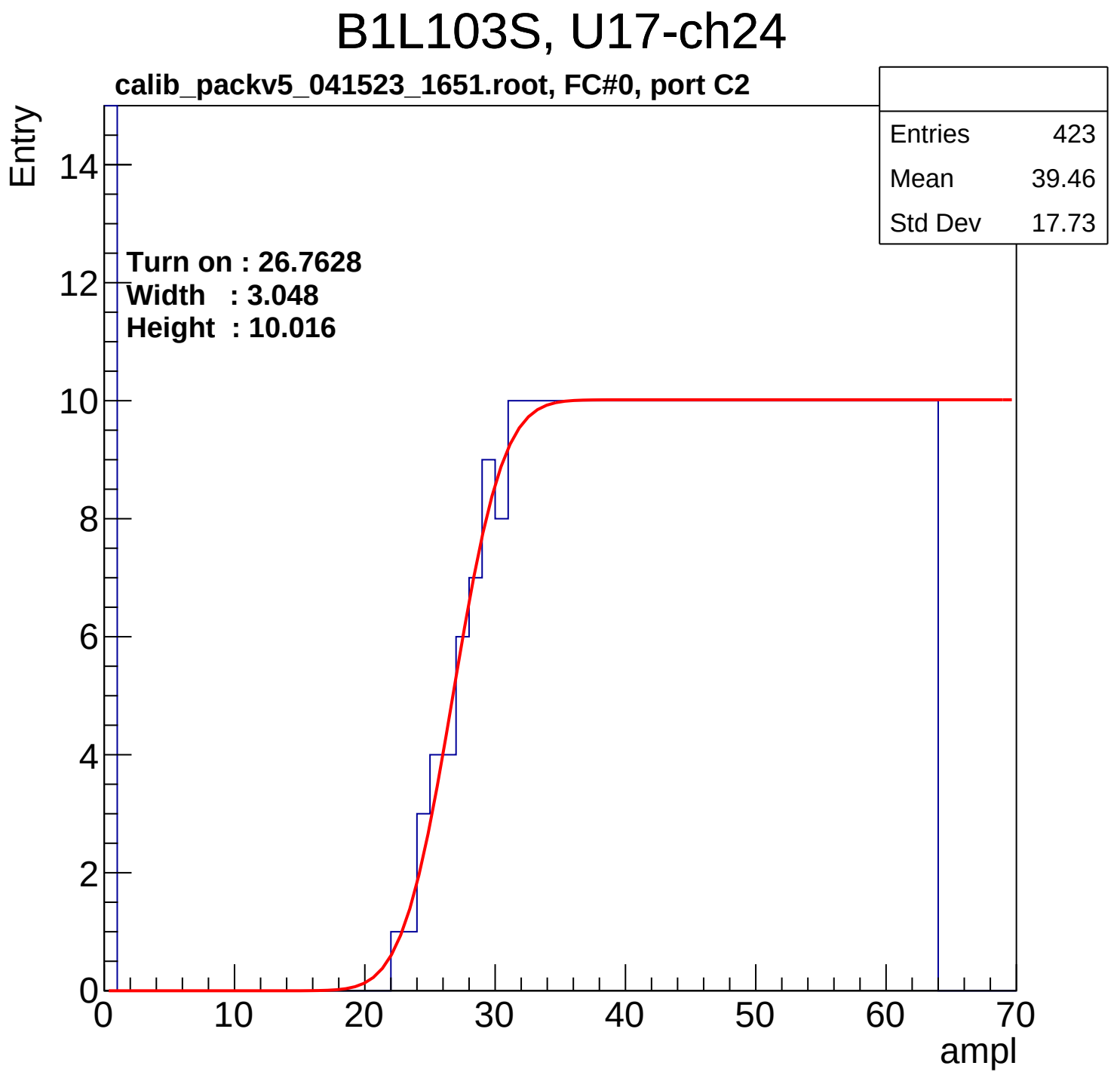
B1L103S, U17-ch24
calib_packv5_041523_1651.root, FC#0, port C2
Entries 423
Mean 39.46
Std Dev 17.73
Turn on : 26.7628
Width : 3.048
Height : 10.016
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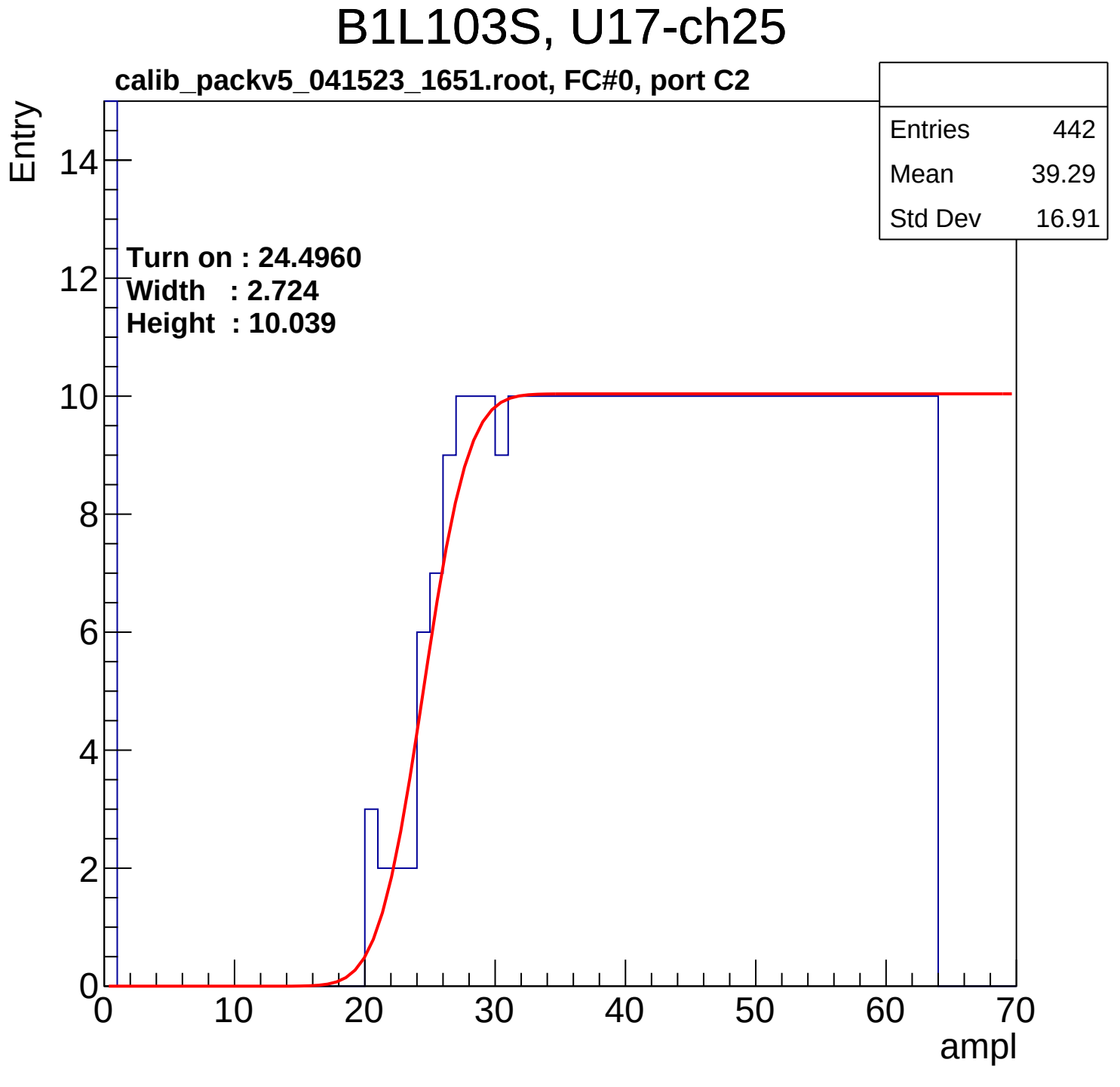
B1L103S, U17-ch25
calib_packv5_041523_1651.root, FC#0, port C2
Entries 442
Mean 39.29
Std Dev 16.91
Turn on : 24.4960
Width : 2.724
Height : 10.039
Entry
ampl
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6
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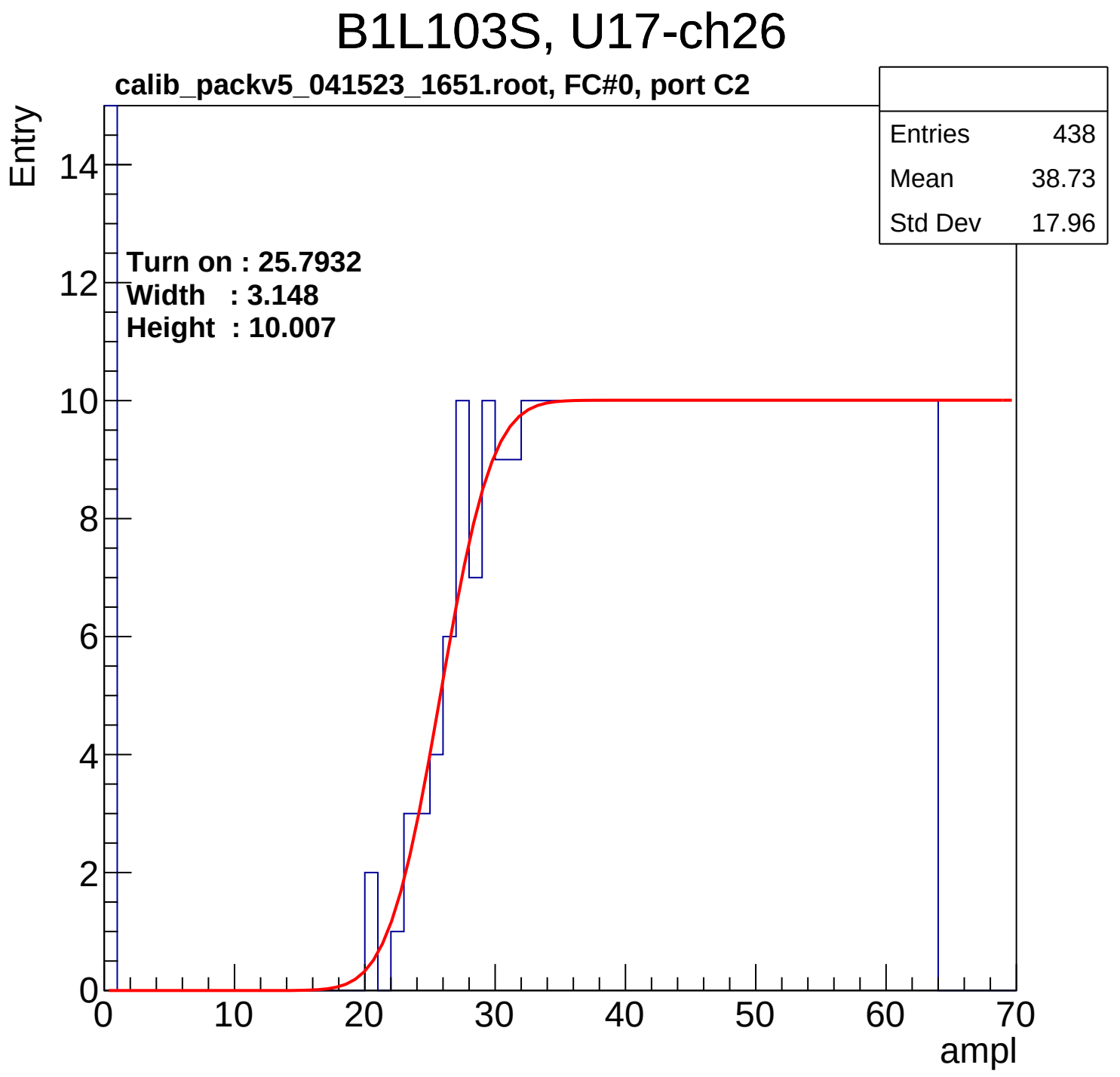
B1L103S, U17-ch26
calib_packv5_041523_1651.root, FC#0, port C2
Entries 438
Mean 38.73
Std Dev 17.96
Turn on : 25.7932
Width : 3.148
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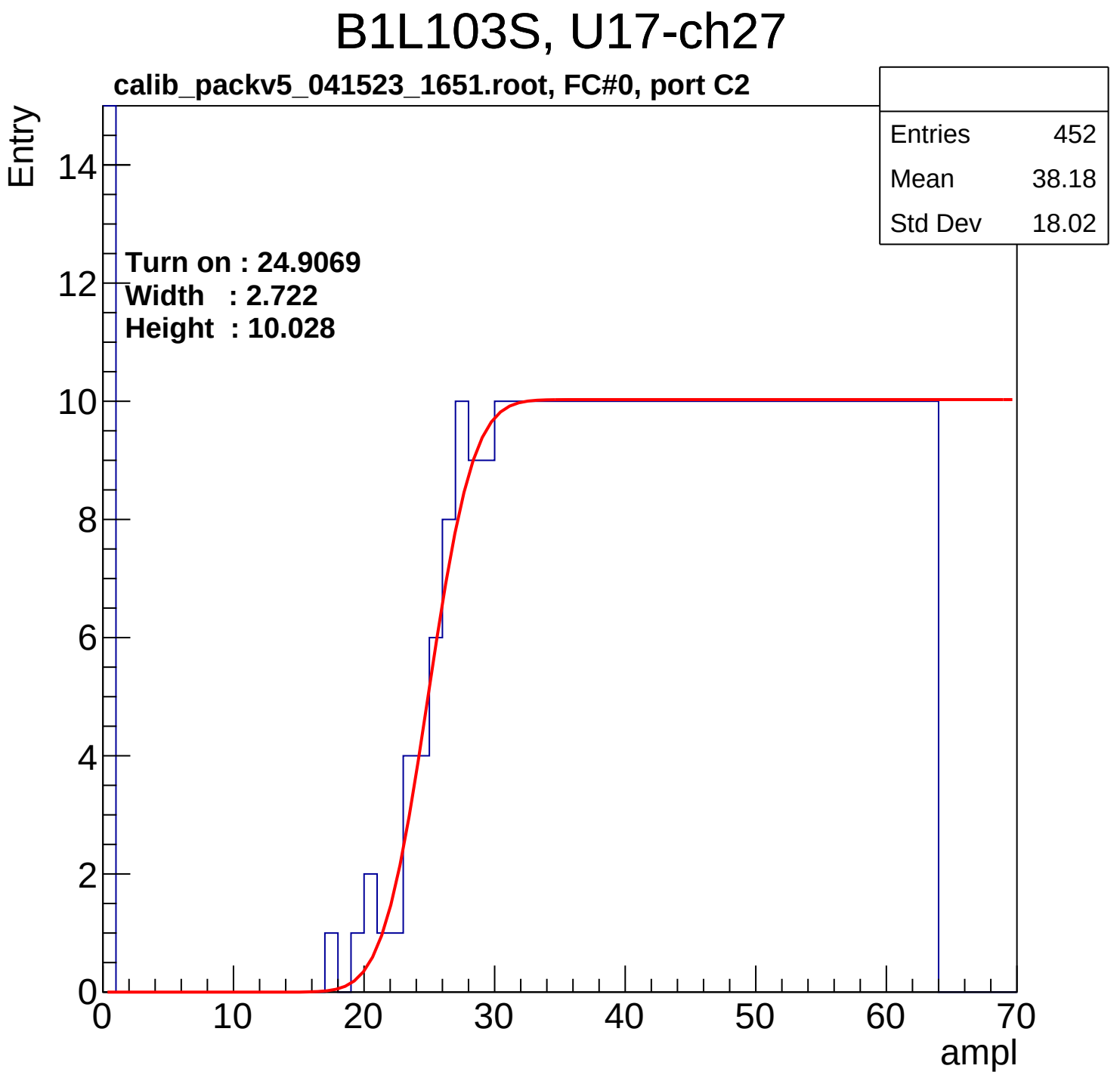
B1L103S, U17-ch27
calib_packv5_041523_1651.root, FC#0, port C2
Entries 452
Mean 38.18
Std Dev 18.02
Turn on : 24.9069
Width : 2.722
Height : 10.028
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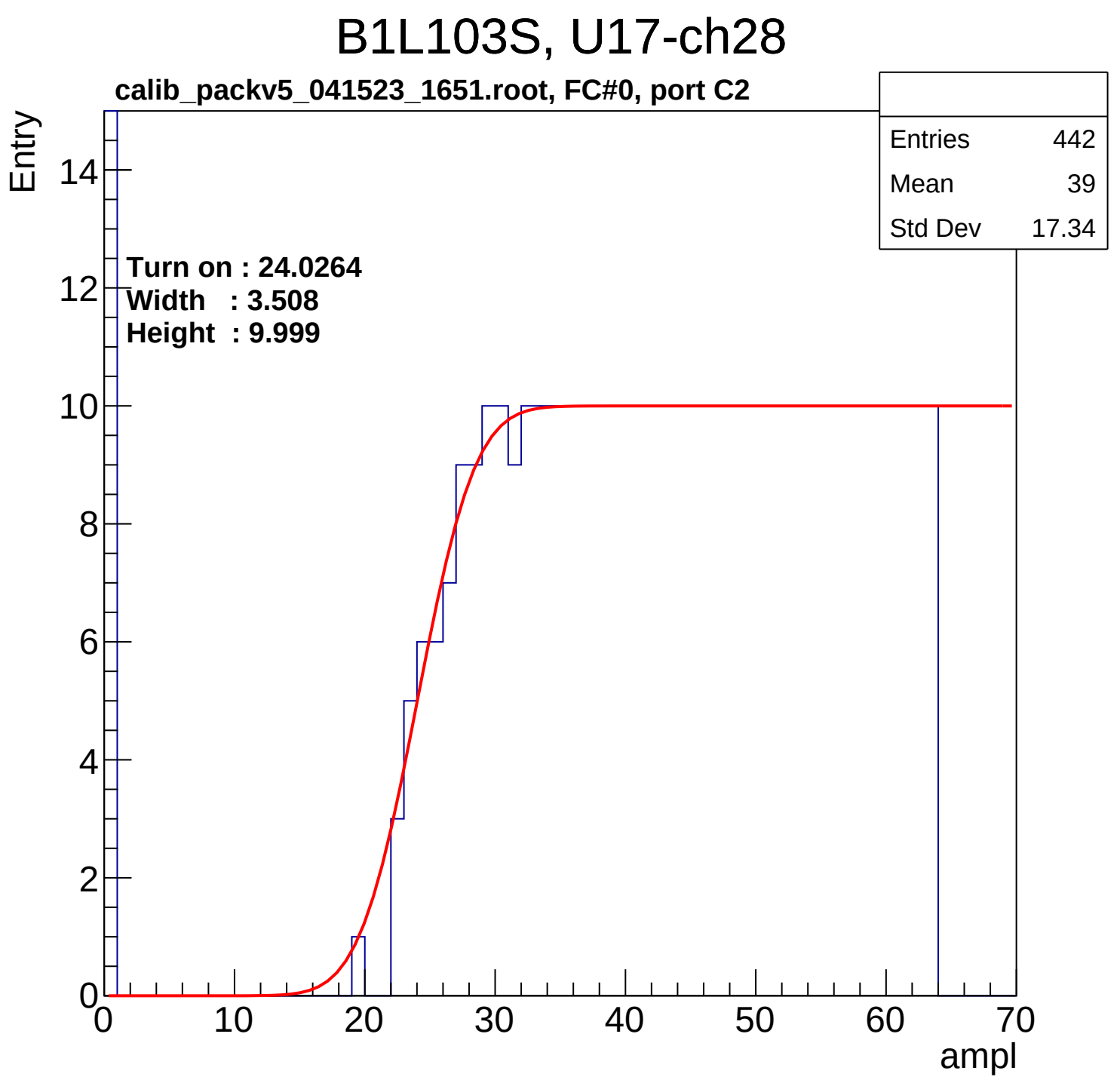
B1L103S, U17-ch28
calib_packv5_041523_1651.root, FC#0, port C2
Entries 442
Mean 39
Std Dev 17.34
Turn on : 24.0264
Width : 3.508
Height : 9.999
Entry
ampl
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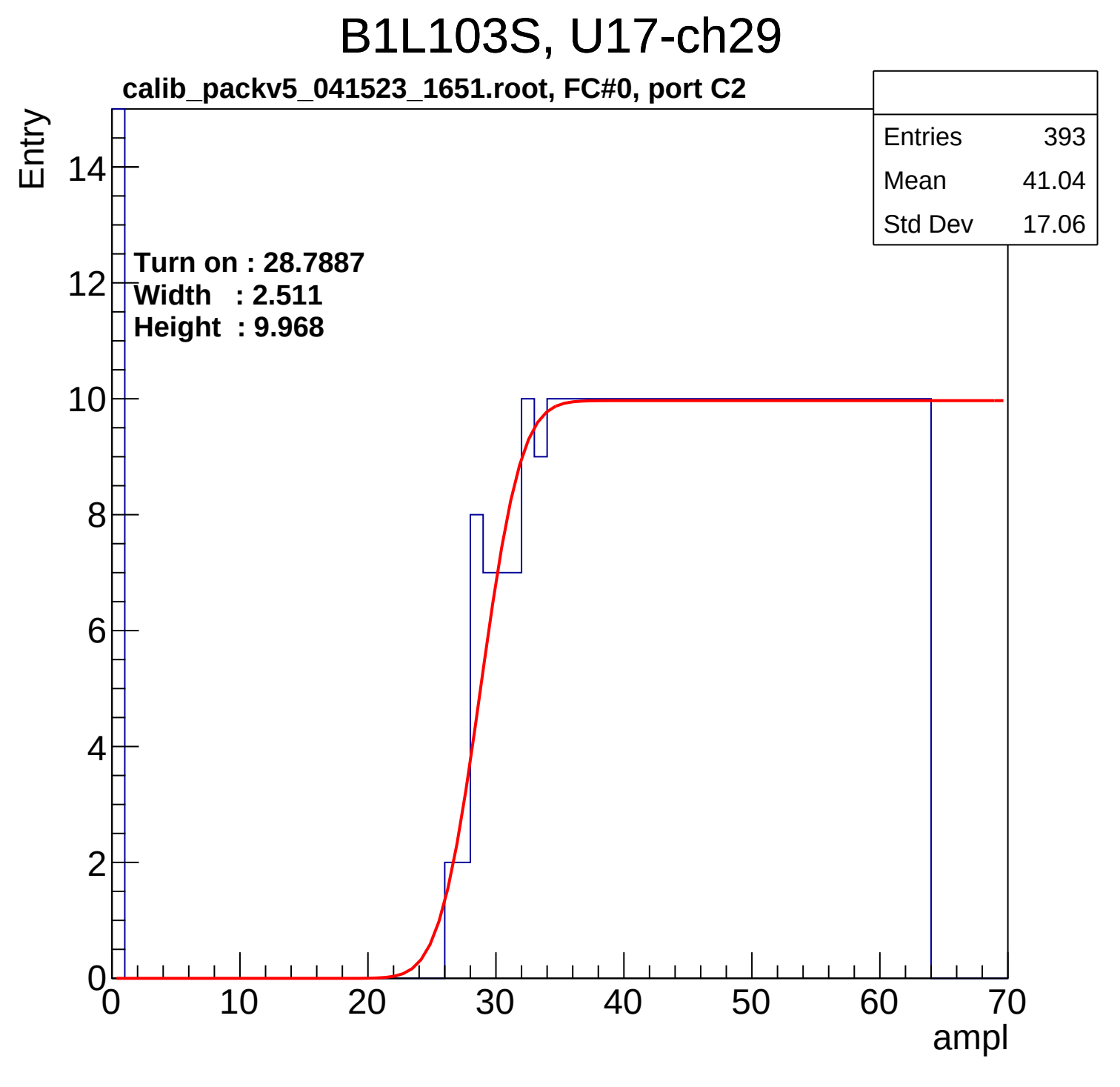
B1L103S, U17-ch29
calib_packv5_041523_1651.root, FC#0, port C2
Entries 393
Mean 41.04
Std Dev 17.06
Turn on : 28.7887
Width : 2.511
Height : 9.968
Entry
ampl
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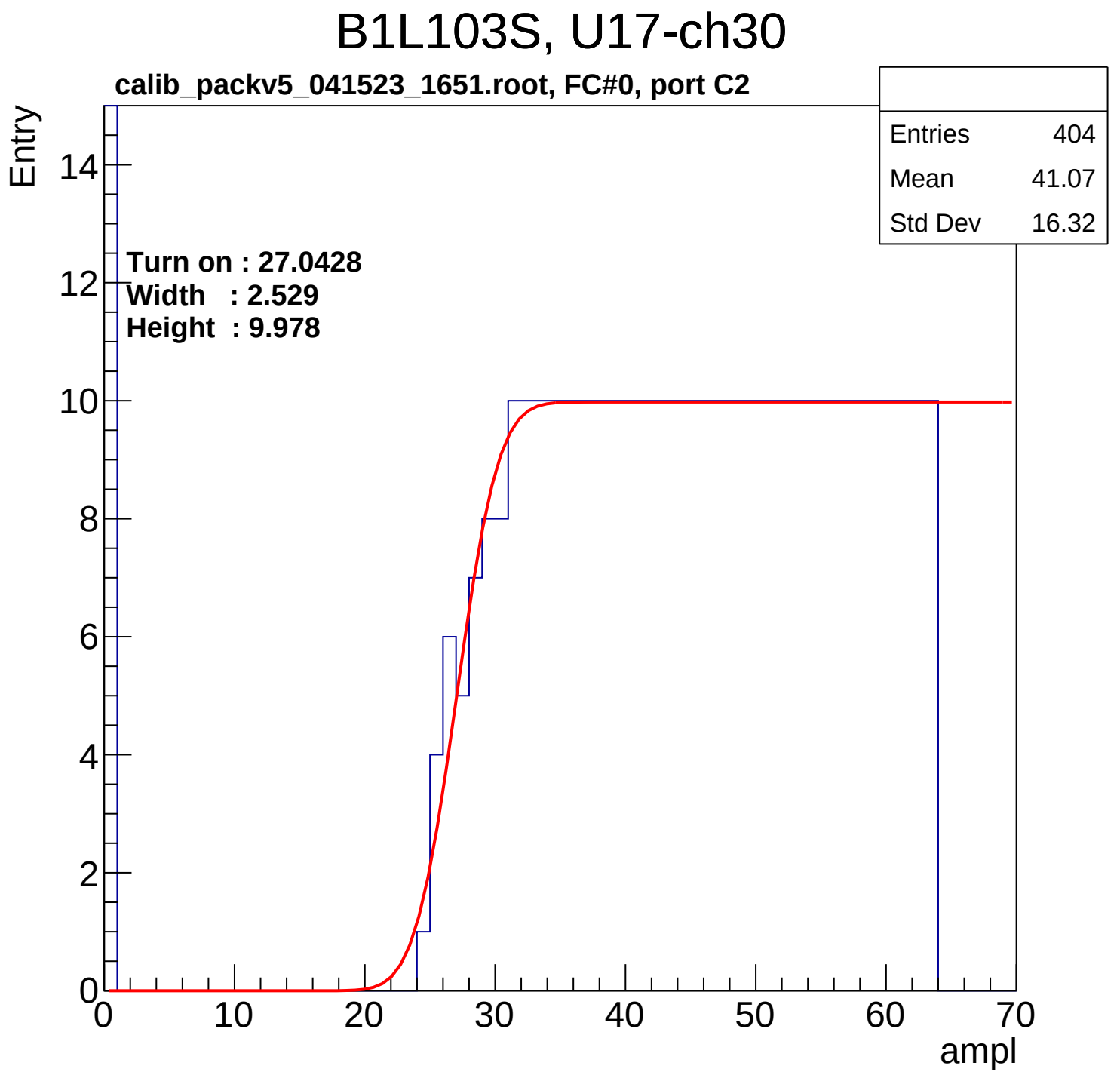
B1L103S, U17-ch30
calib_packv5_041523_1651.root, FC#0, port C2
Entries 404
Mean 41.07
Std Dev 16.32
Turn on : 27.0428
Width : 2.529
Height : 9.978
Entry
ampl
0
2
4
6
8
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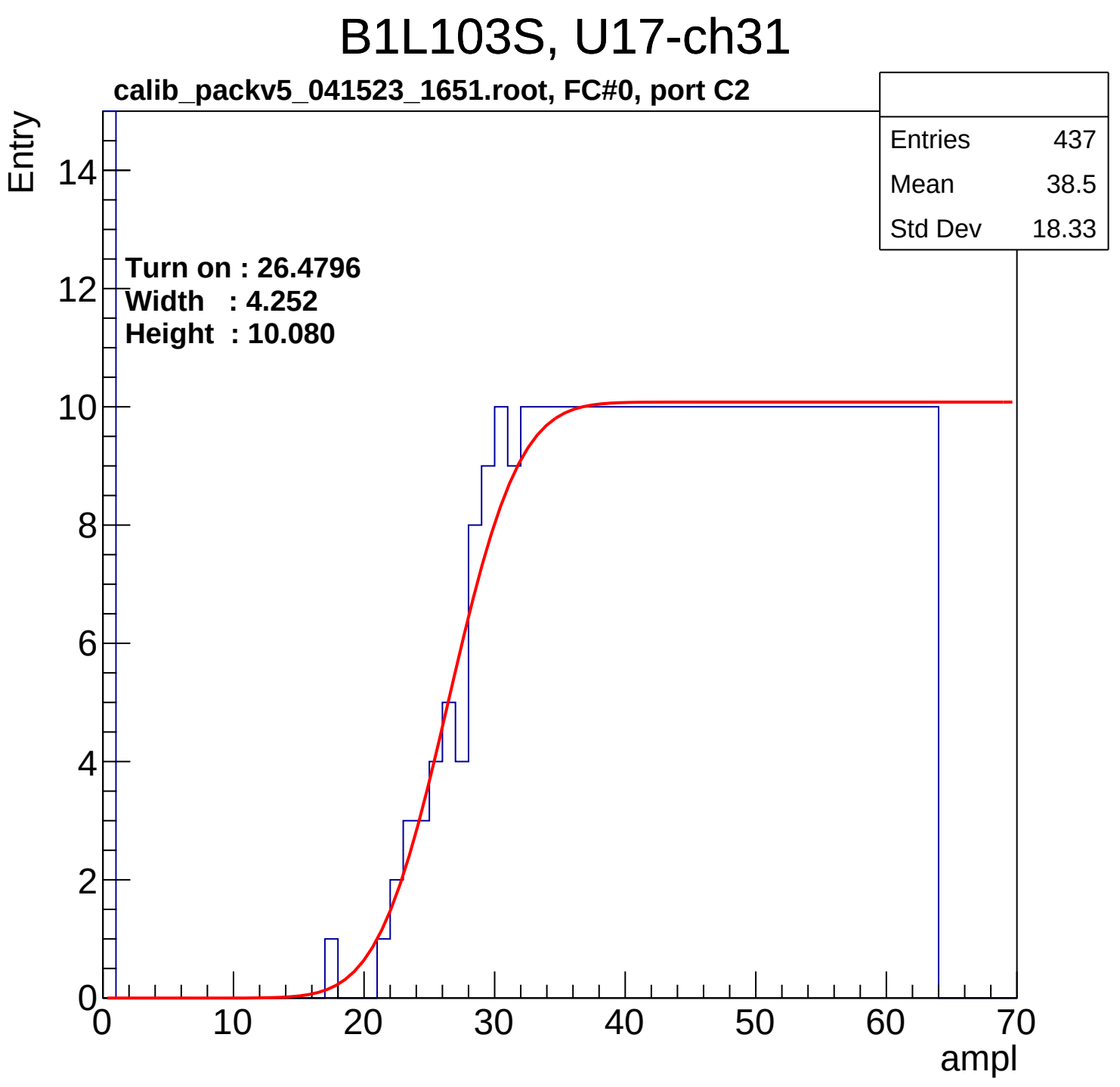
B1L103S, U17-ch31
calib_packv5_041523_1651.root, FC#0, port C2
Entries 437
Mean 38.5
Std Dev 18.33
Turn on : 26.4796
Width : 4.252
Height : 10.080
Entry
ampl
0
2
4
6
8
10
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0
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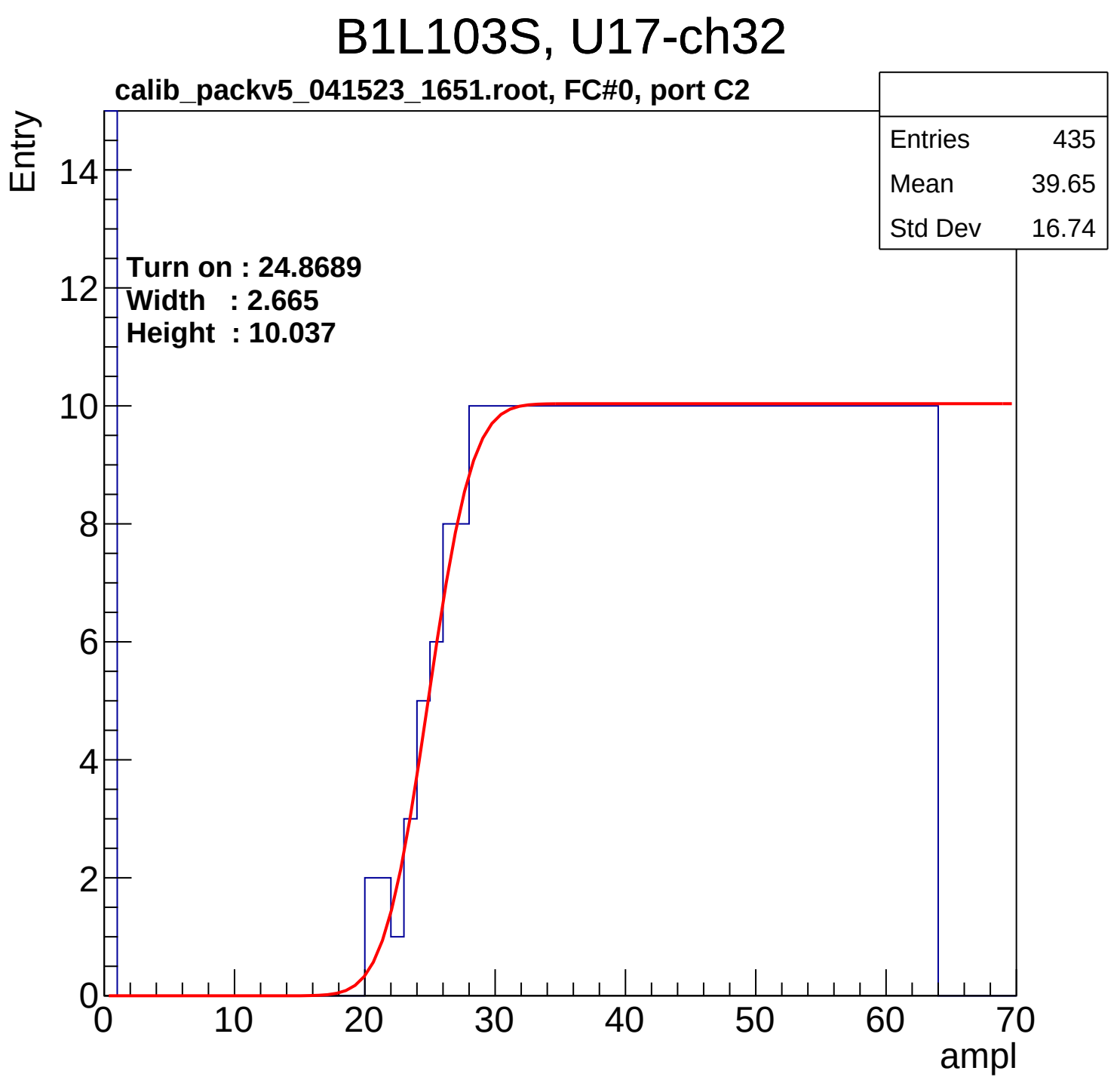
B1L103S, U17-ch32
calib_packv5_041523_1651.root, FC#0, port C2
Entries 435
Mean 39.65
Std Dev 16.74
Turn on : 24.8689
Width : 2.665
Height : 10.037
Entry
ampl
0
2
4
6
8
10
12
14
0
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60
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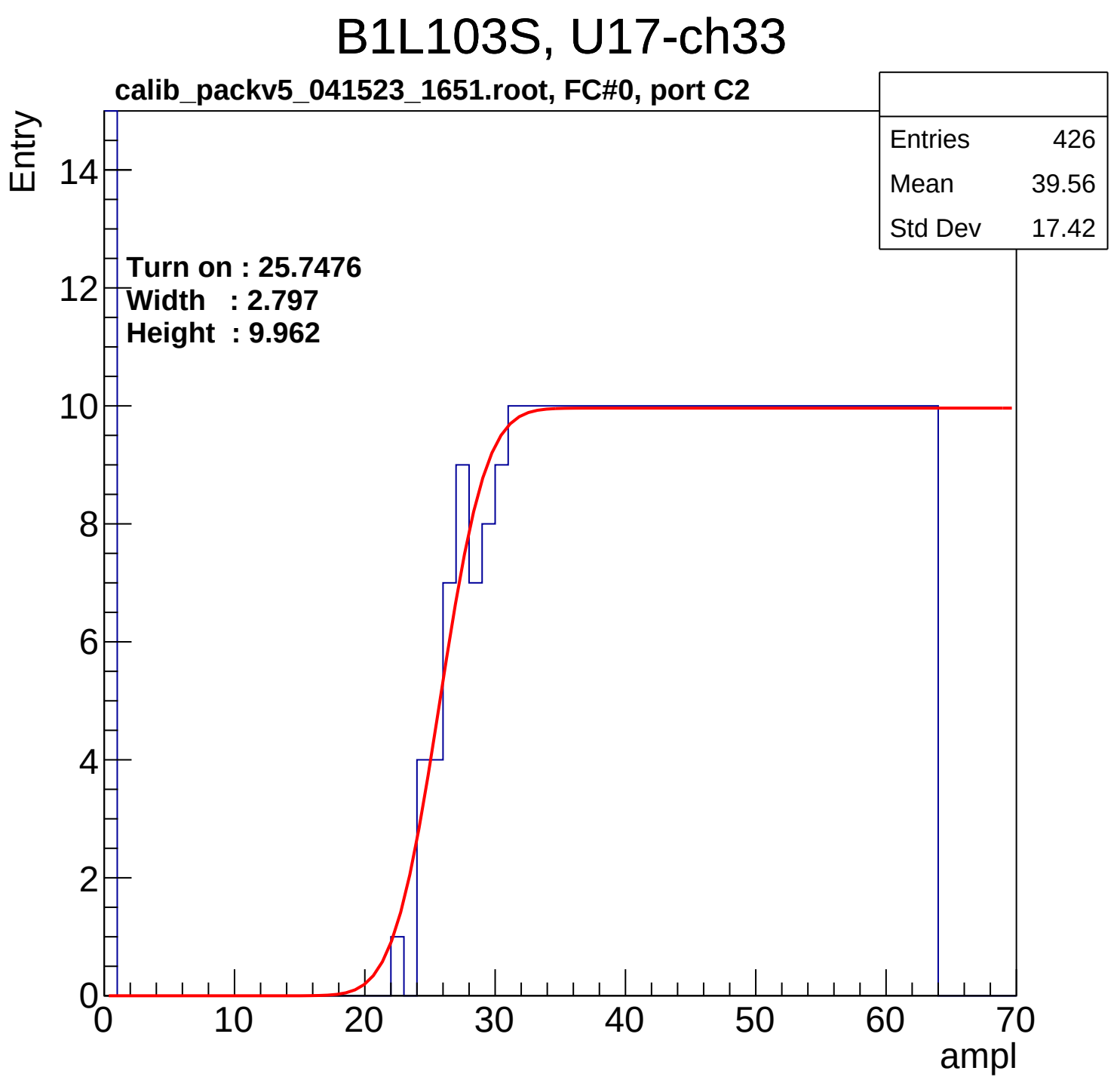
B1L103S, U17-ch33
calib_packv5_041523_1651.root, FC#0, port C2
Entries 426
Mean 39.56
Std Dev 17.42
Turn on : 25.7476
Width : 2.797
Height : 9.962
Entry
ampl
0
2
4
6
8
10
12
14
0
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60
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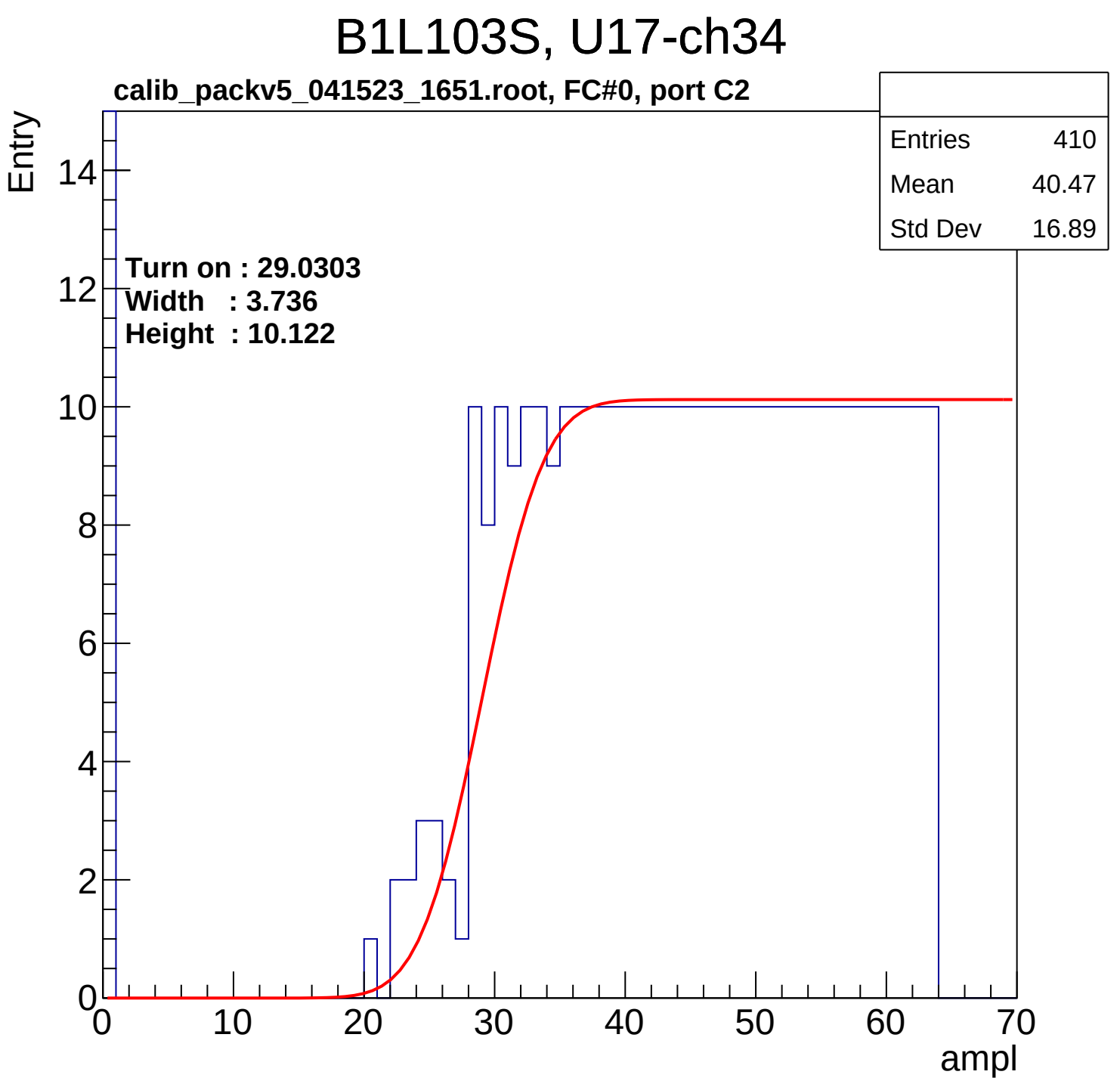
B1L103S, U17-ch34
calib_packv5_041523_1651.root, FC#0, port C2
Entries 410
Mean 40.47
Std Dev 16.89
Turn on : 29.0303
Width : 3.736
Height : 10.122
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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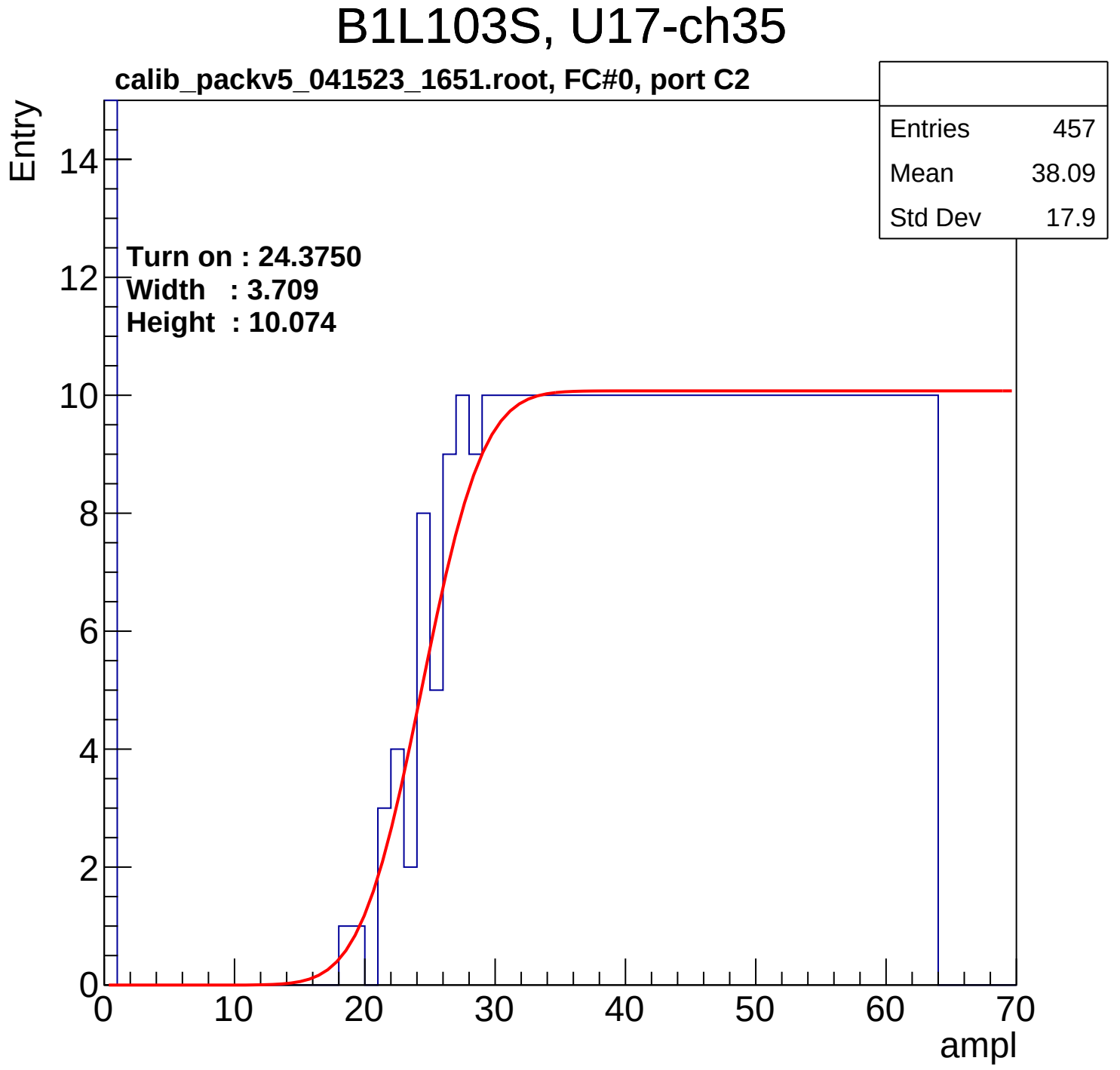
B1L103S, U17-ch35
calib_packv5_041523_1651.root, FC#0, port C2
Entries 457
Mean 38.09
Std Dev 17.9
Turn on : 24.3750
Width : 3.709
Height : 10.074
Entry
ampl
0
2
4
6
8
10
12
14
0
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60
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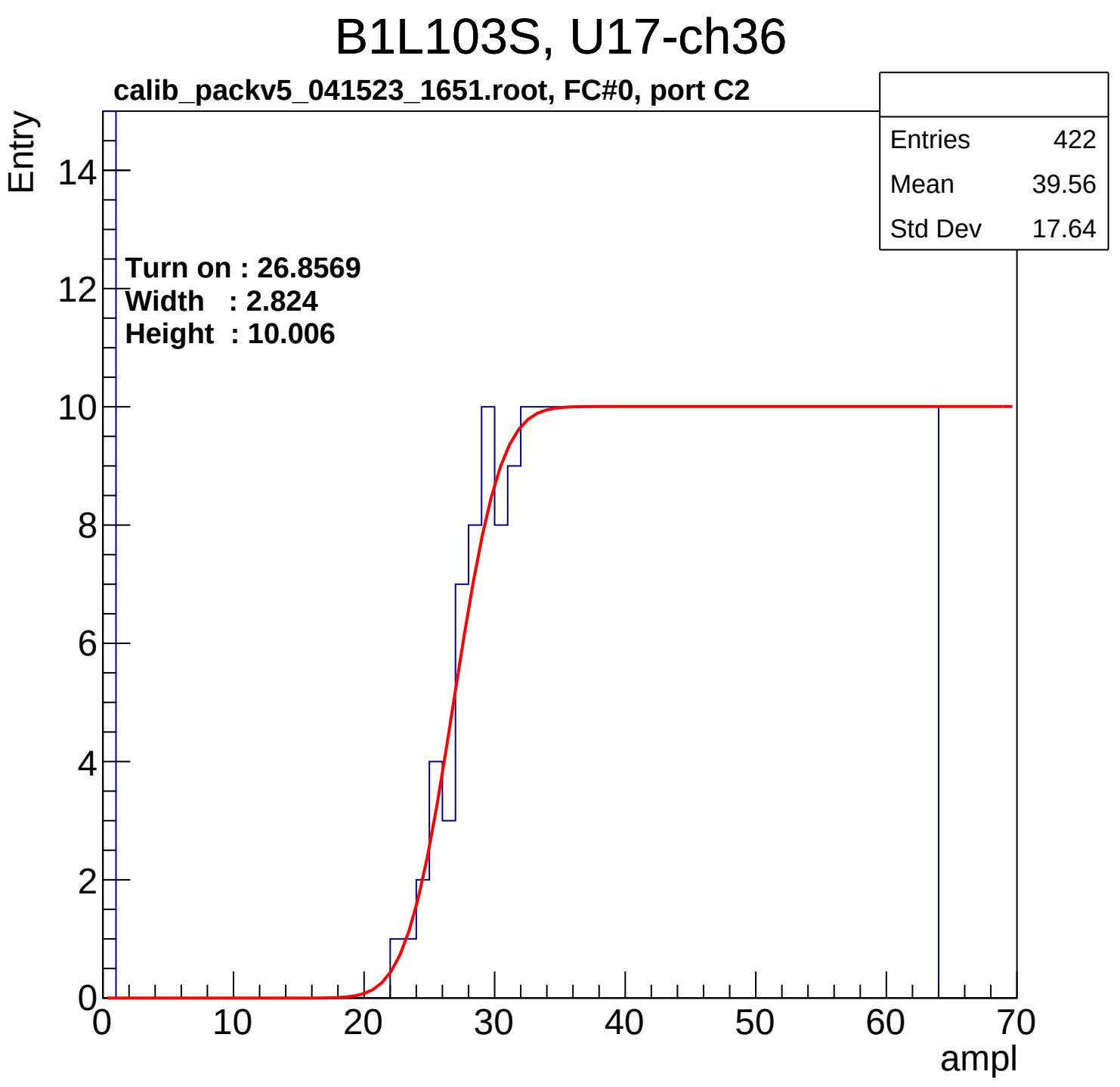
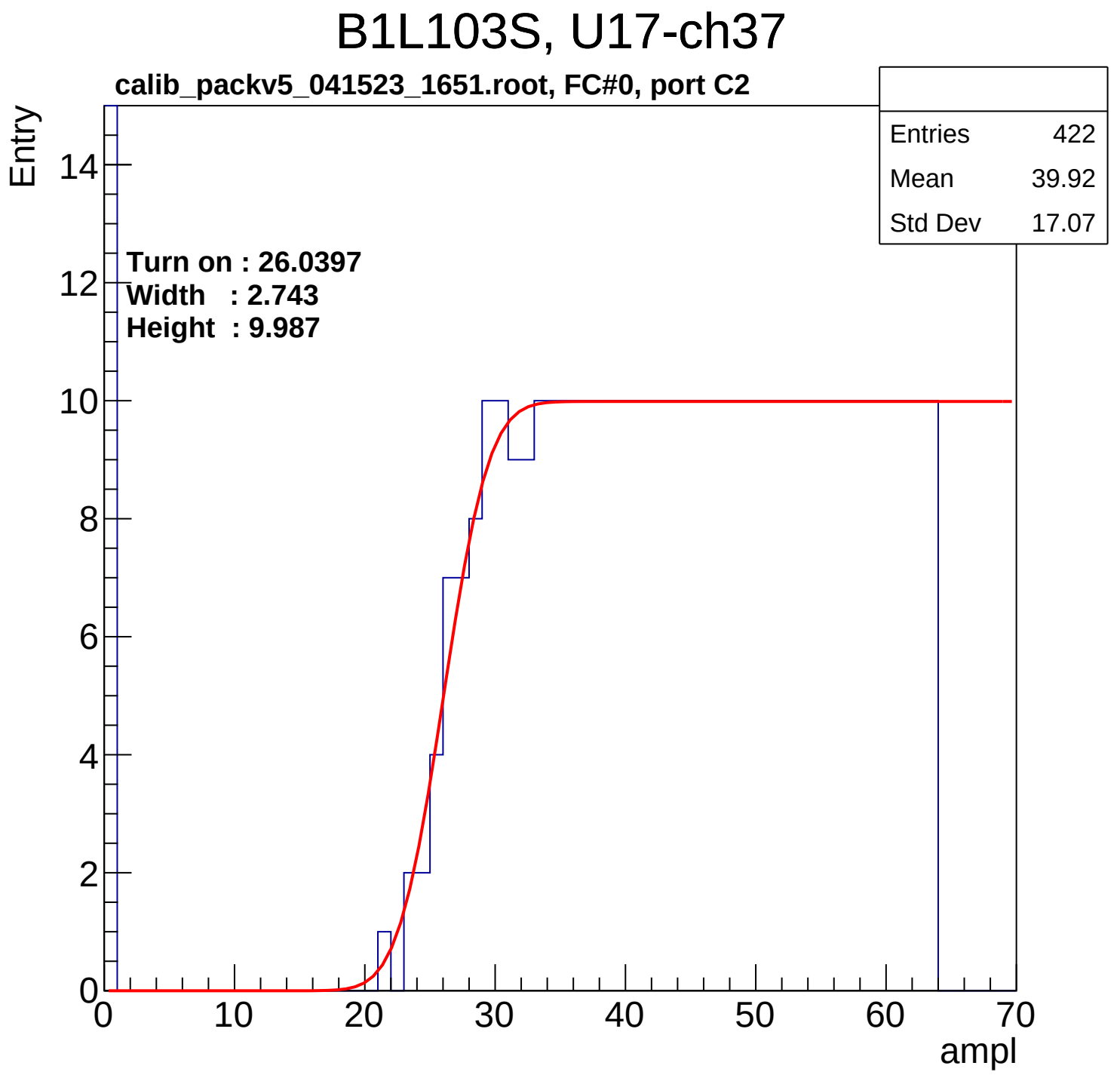

B1L103S, U17-ch36
calib_packv5_041523_1651.root, FC#0, port C2
Entries 422
Mean 39.56
Std Dev 17.64
Turn on : 26.8569
Width : 2.824
Height : 10.006
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U17-ch37
calib_packv5_041523_1651.root, FC#0, port C2
Entries 422
Mean 39.92
Std Dev 17.07
Turn on : 26.0397
Width : 2.743
Height : 9.987
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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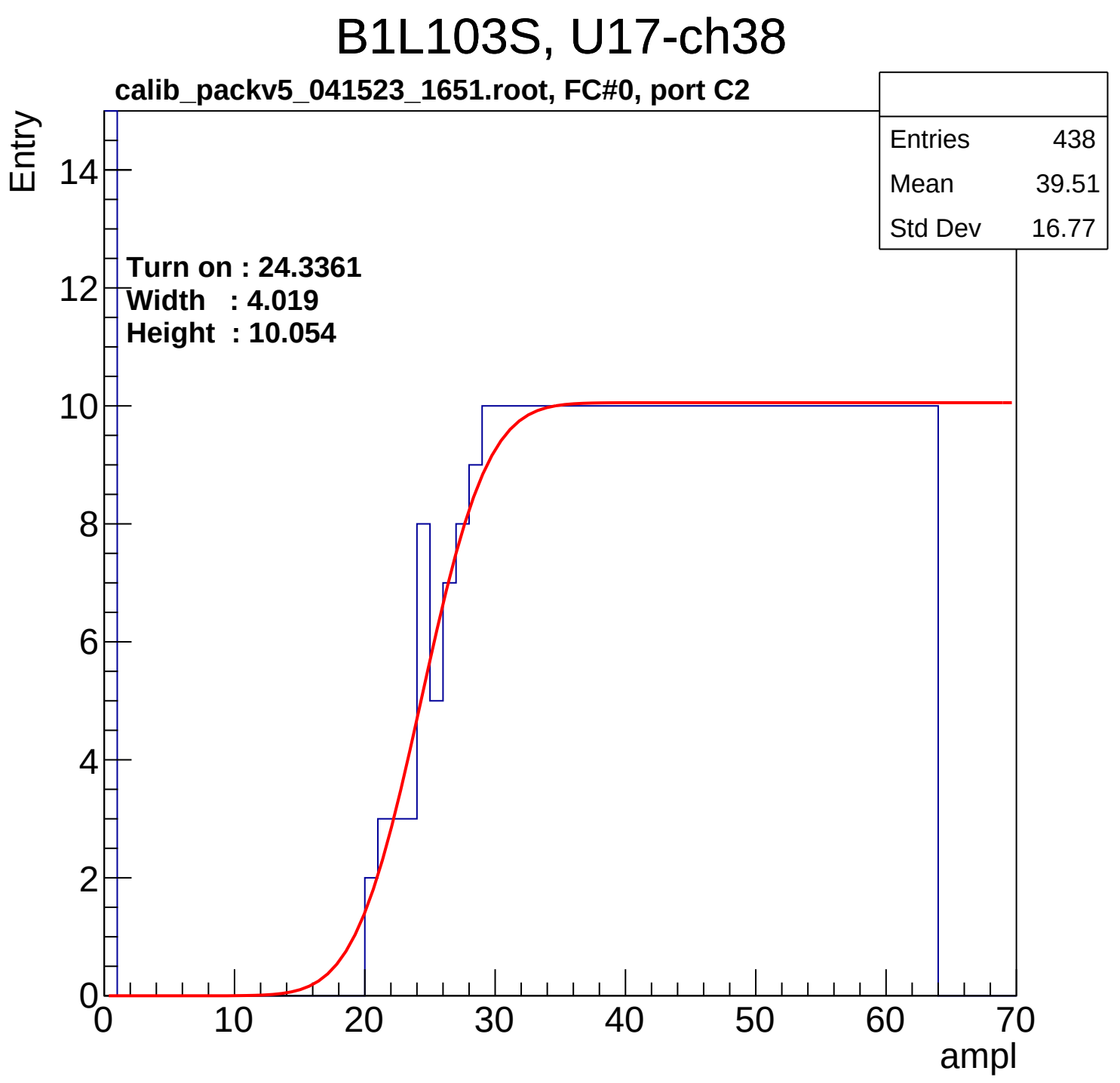
B1L103S, U17-ch38
calib_packv5_041523_1651.root, FC#0, port C2
Entries 438
Mean 39.51
Std Dev 16.77
Turn on : 24.3361
Width : 4.019
Height : 10.054
Entry
ampl
0
2
4
6
8
10
12
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0
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20
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60
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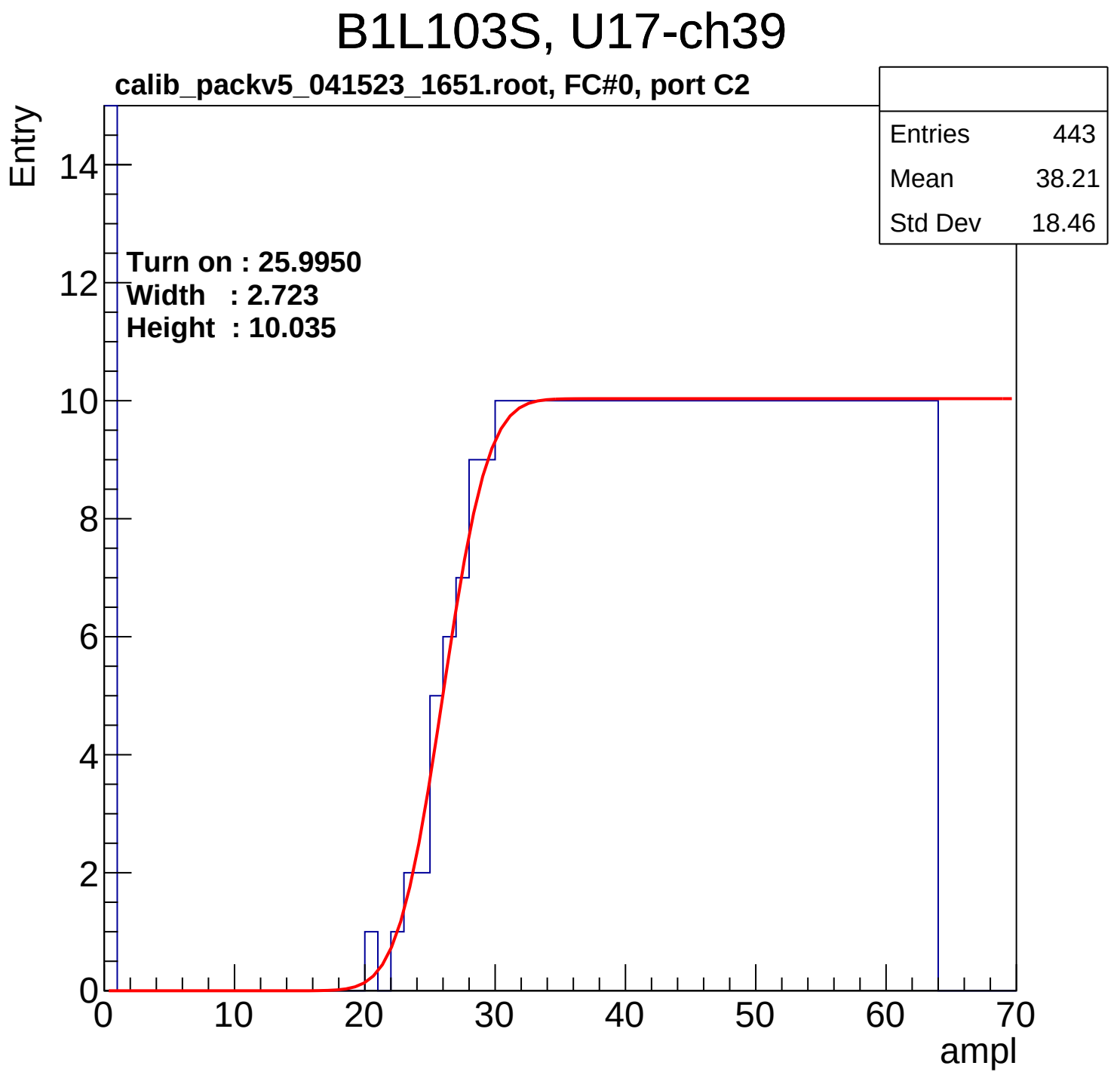
B1L103S, U17-ch39
calib_packv5_041523_1651.root, FC#0, port C2
Entries 443
Mean 38.21
Std Dev 18.46
Turn on : 25.9950
Width : 2.723
Height : 10.035
Entry
ampl
0
2
4
6
8
10
12
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0
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20
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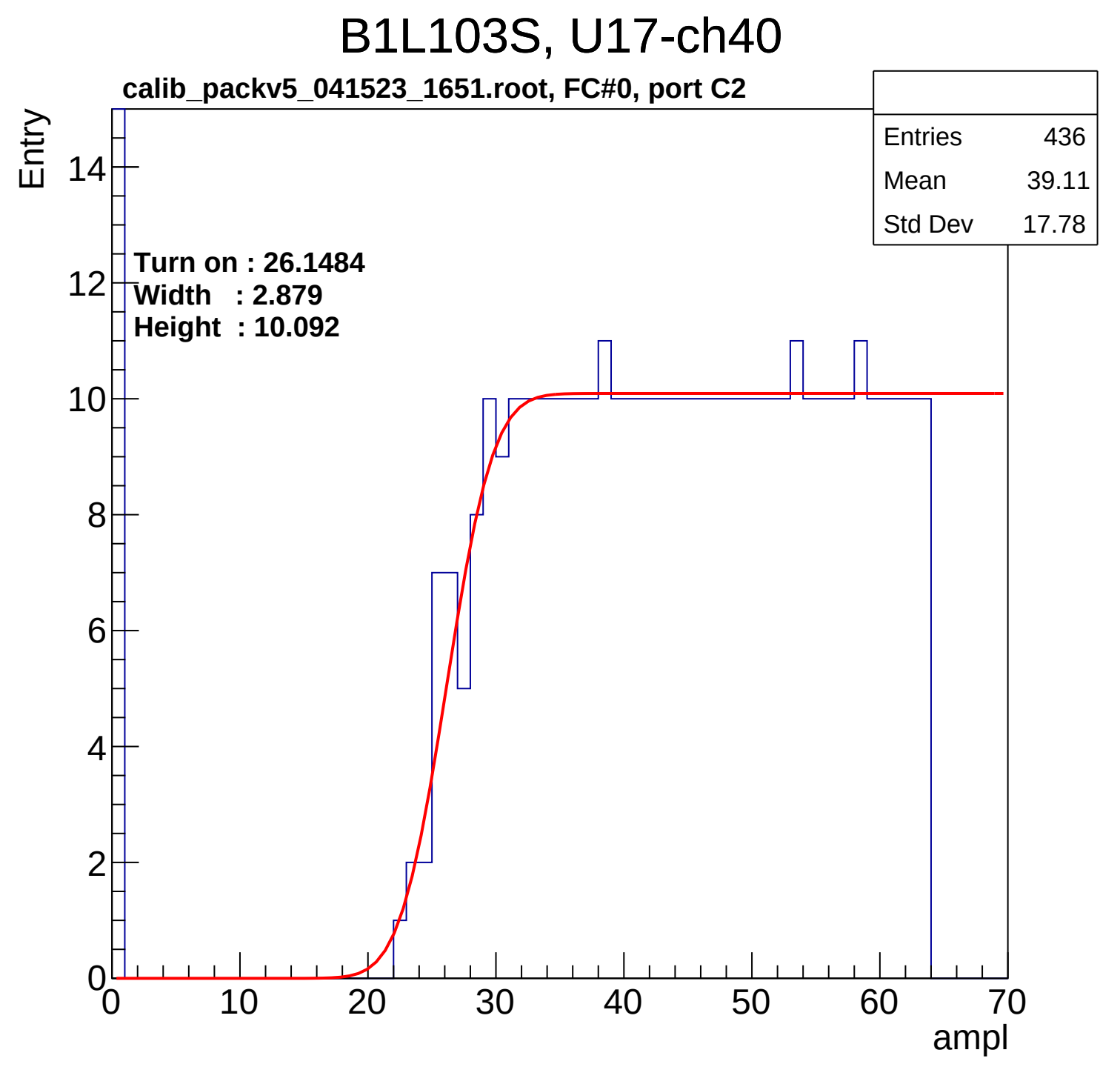
B1L103S, U17-ch40
calib_packv5_041523_1651.root, FC#0, port C2
Entries 436
Mean 39.11
Std Dev 17.78
Turn on : 26.1484
Width : 2.879
Height : 10.092
Entry
ampl
0
2
4
6
8
10
12
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0
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20
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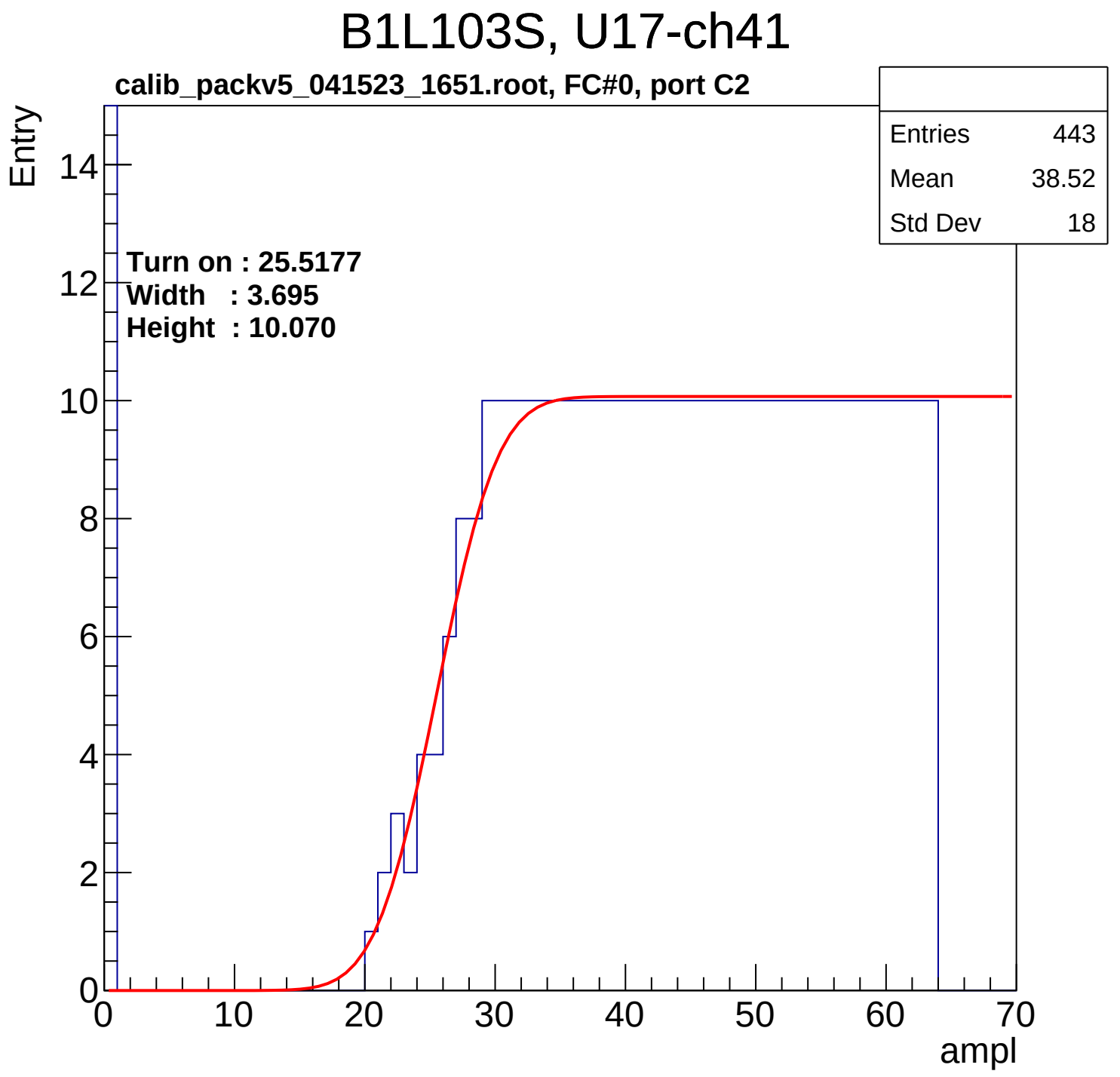
B1L103S, U17-ch41
calib_packv5_041523_1651.root, FC#0, port C2
Entries 443
Mean 38.52
Std Dev 18
Turn on : 25.5177
Width : 3.695
Height : 10.070
Entry
ampl
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2
4
6
8
10
12
14
0
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20
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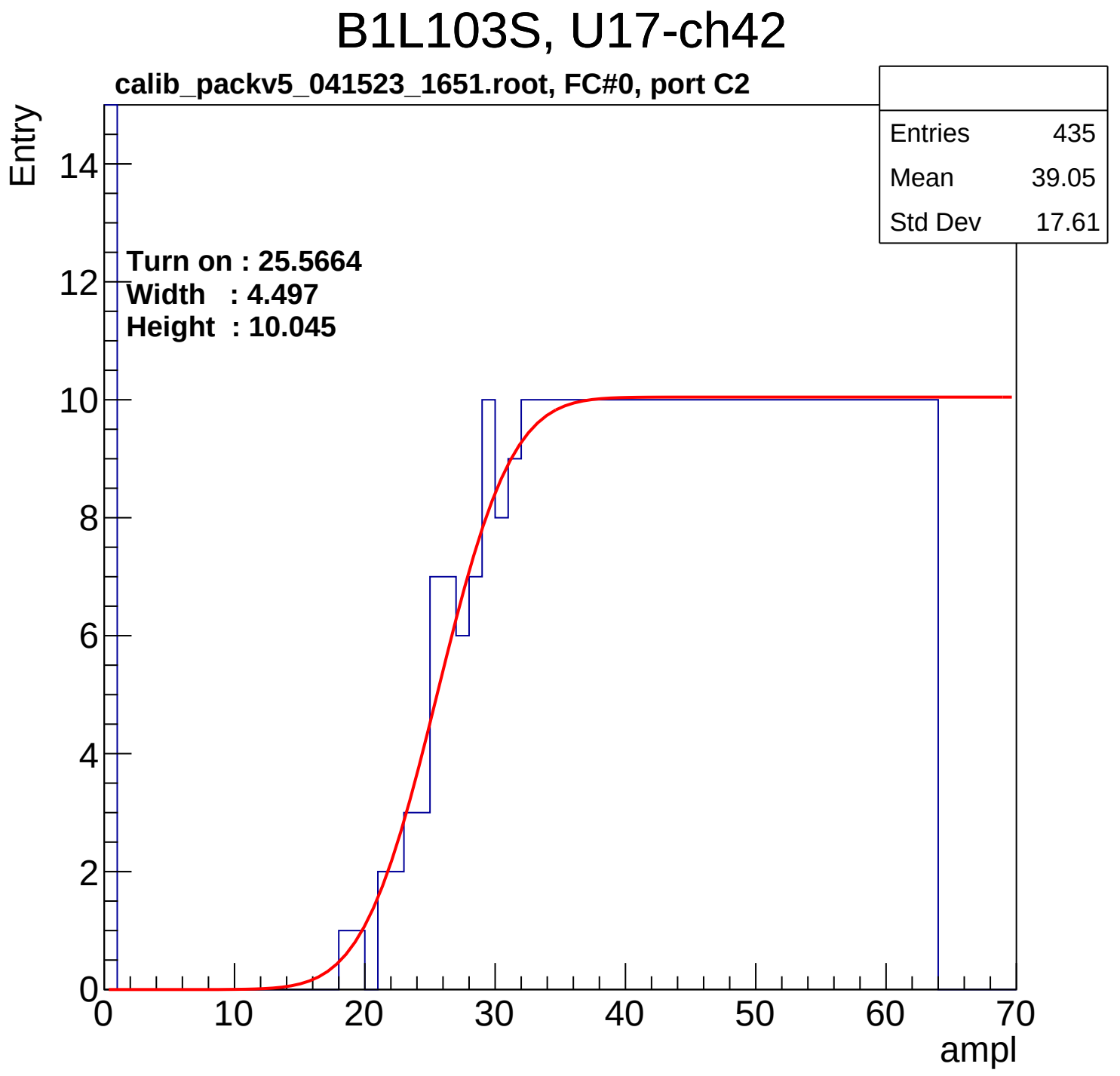
B1L103S, U17-ch42
calib_packv5_041523_1651.root, FC#0, port C2
Entries 435
Mean 39.05
Std Dev 17.61
Turn on : 25.5664
Width : 4.497
Height : 10.045
Entry
ampl
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2
4
6
8
10
12
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0
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20
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60
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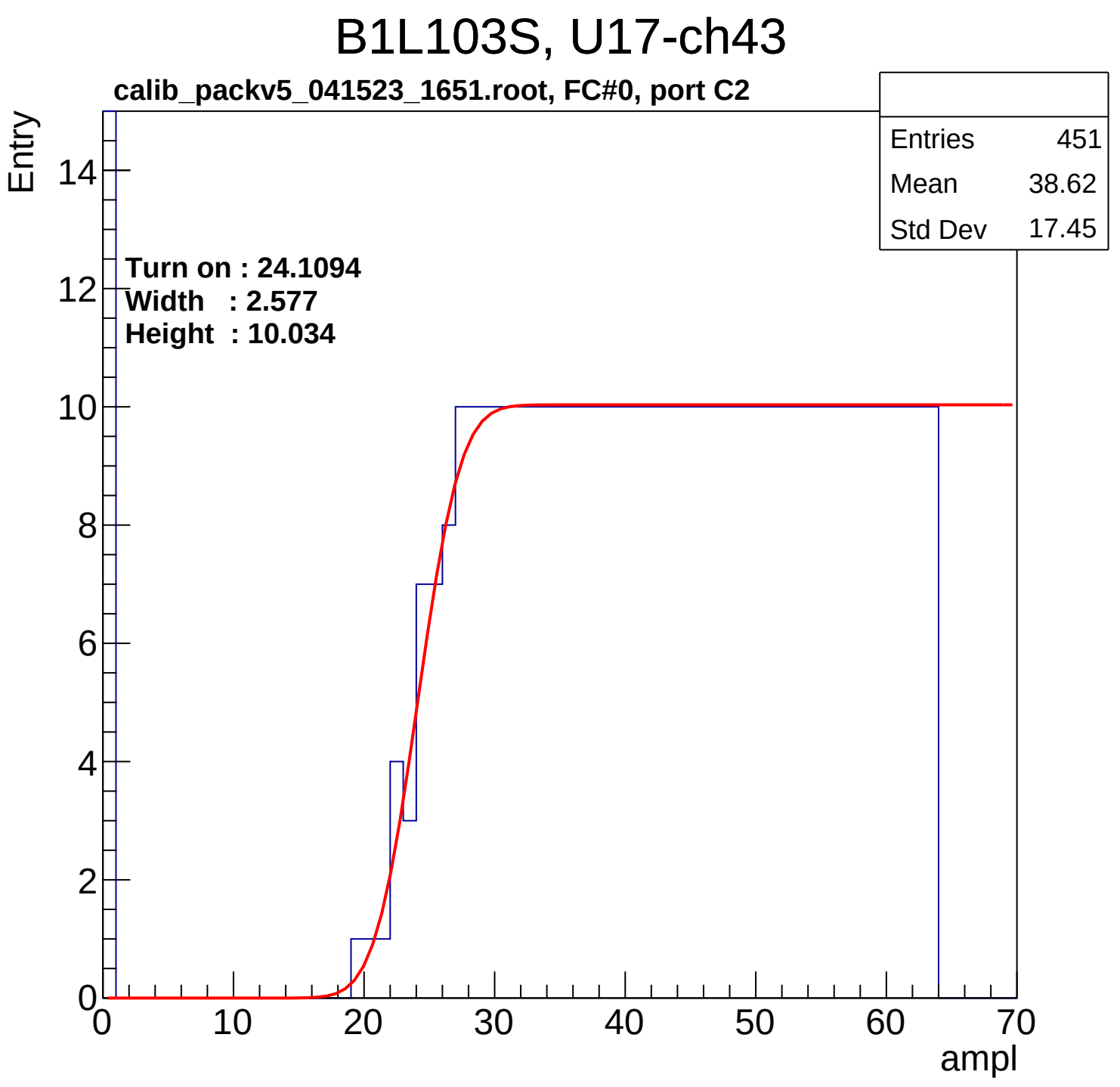
B1L103S, U17-ch43
calib_packv5_041523_1651.root, FC#0, port C2
Entries 451
Mean 38.62
Std Dev 17.45
Turn on : 24.1094
Width : 2.577
Height : 10.034
Entry
ampl
0
2
4
6
8
10
12
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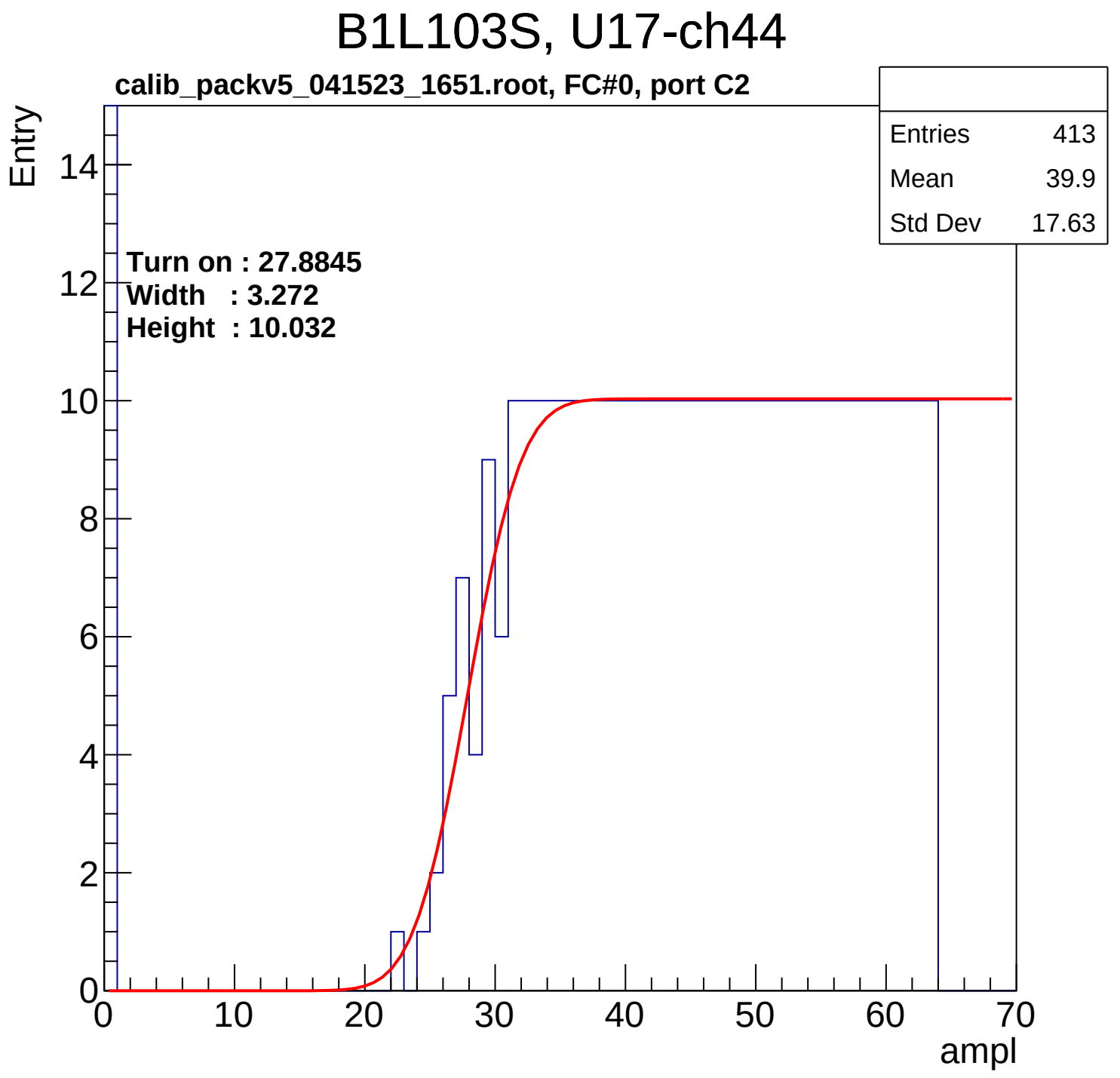
B1L103S, U17-ch44
calib_packv5_041523_1651.root, FC#0, port C2
Entries 413
Mean 39.9
Std Dev 17.63
Turn on : 27.8845
Width : 3.272
Height : 10.032
Entry
ampl
0
2
4
6
8
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12
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20
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60
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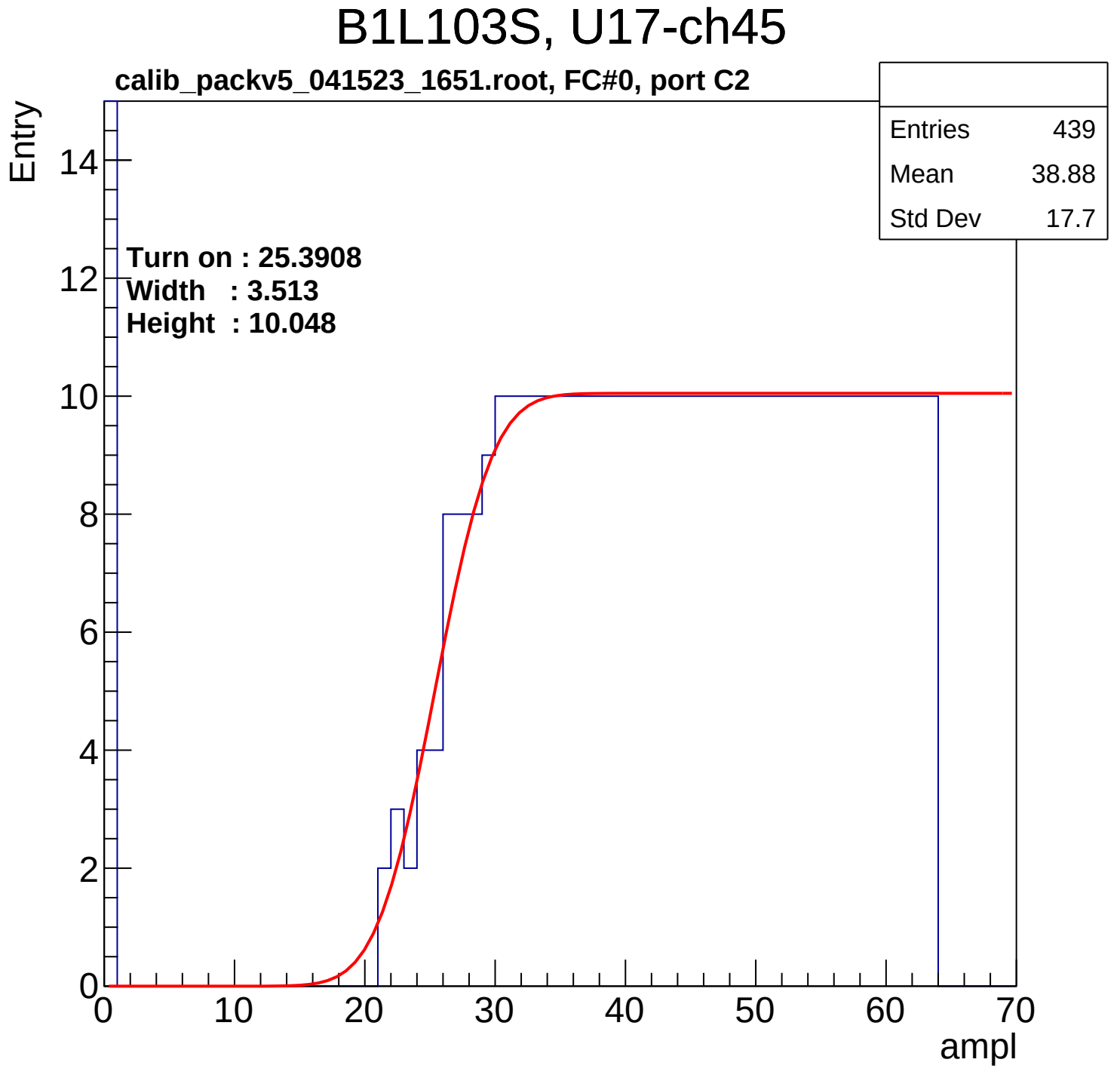
B1L103S, U17-ch45
calib_packv5_041523_1651.root, FC#0, port C2
Entries 439
Mean 38.88
Std Dev 17.7
Turn on : 25.3908
Width : 3.513
Height : 10.048
Entry
ampl
0
2
4
6
8
10
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60
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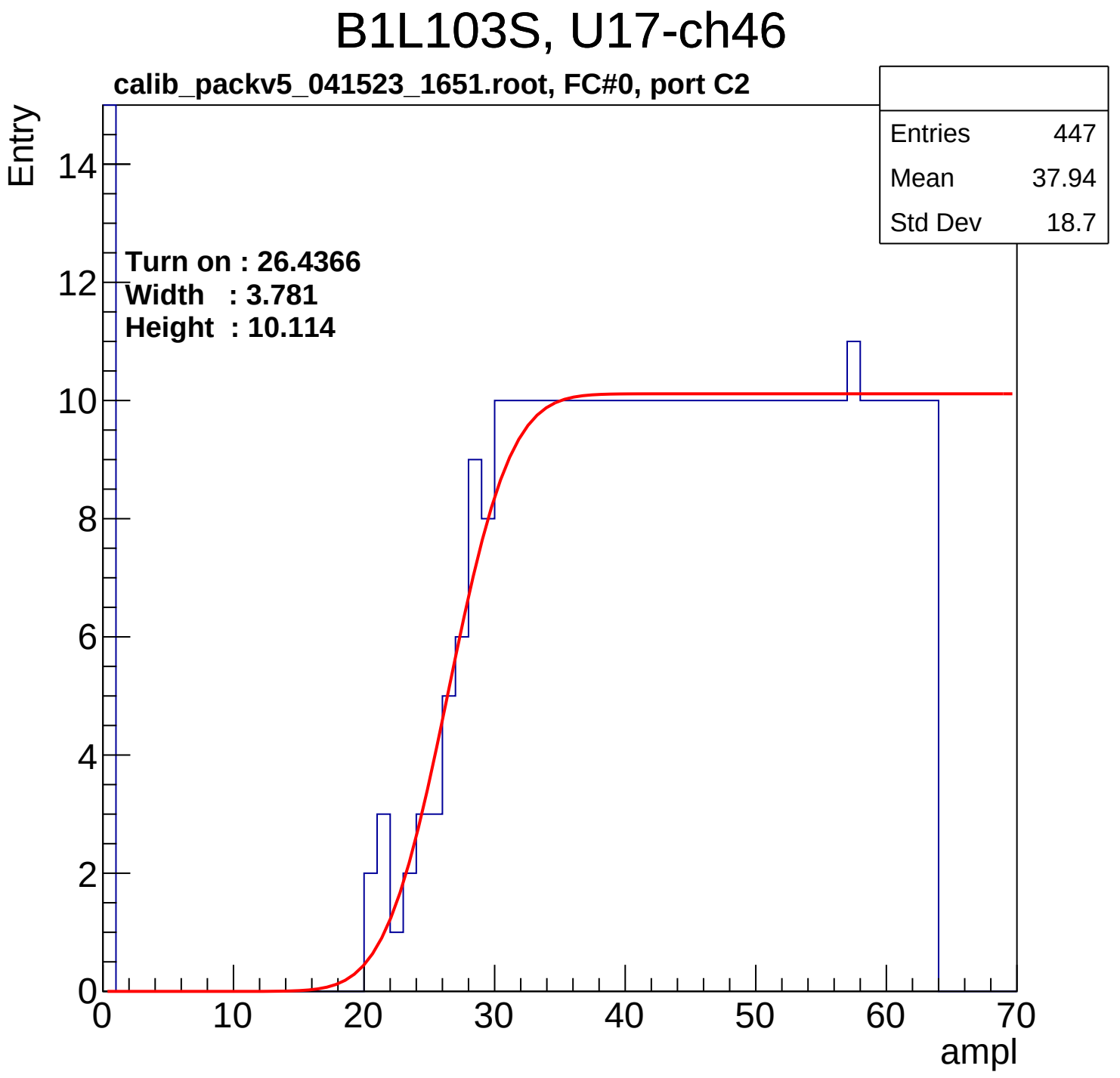
B1L103S, U17-ch46
calib_packv5_041523_1651.root, FC#0, port C2
Entries 447
Mean 37.94
Std Dev 18.7
Turn on : 26.4366
Width : 3.781
Height : 10.114
Entry
ampl
0
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8
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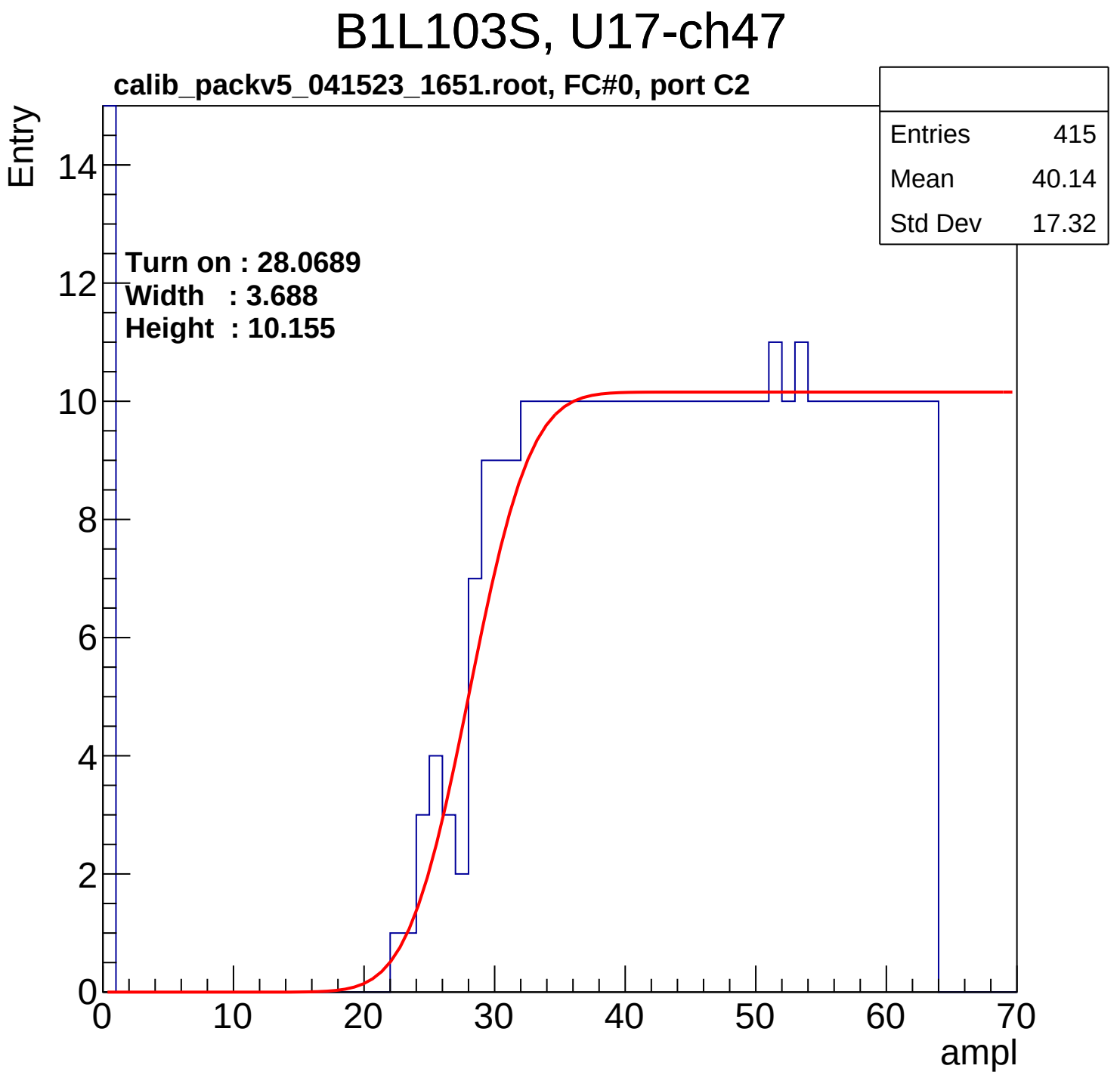
B1L103S, U17-ch47
calib_packv5_041523_1651.root, FC#0, port C2
Entries 415
Mean 40.14
Std Dev 17.32
Turn on : 28.0689
Width : 3.688
Height : 10.155
Entry
ampl
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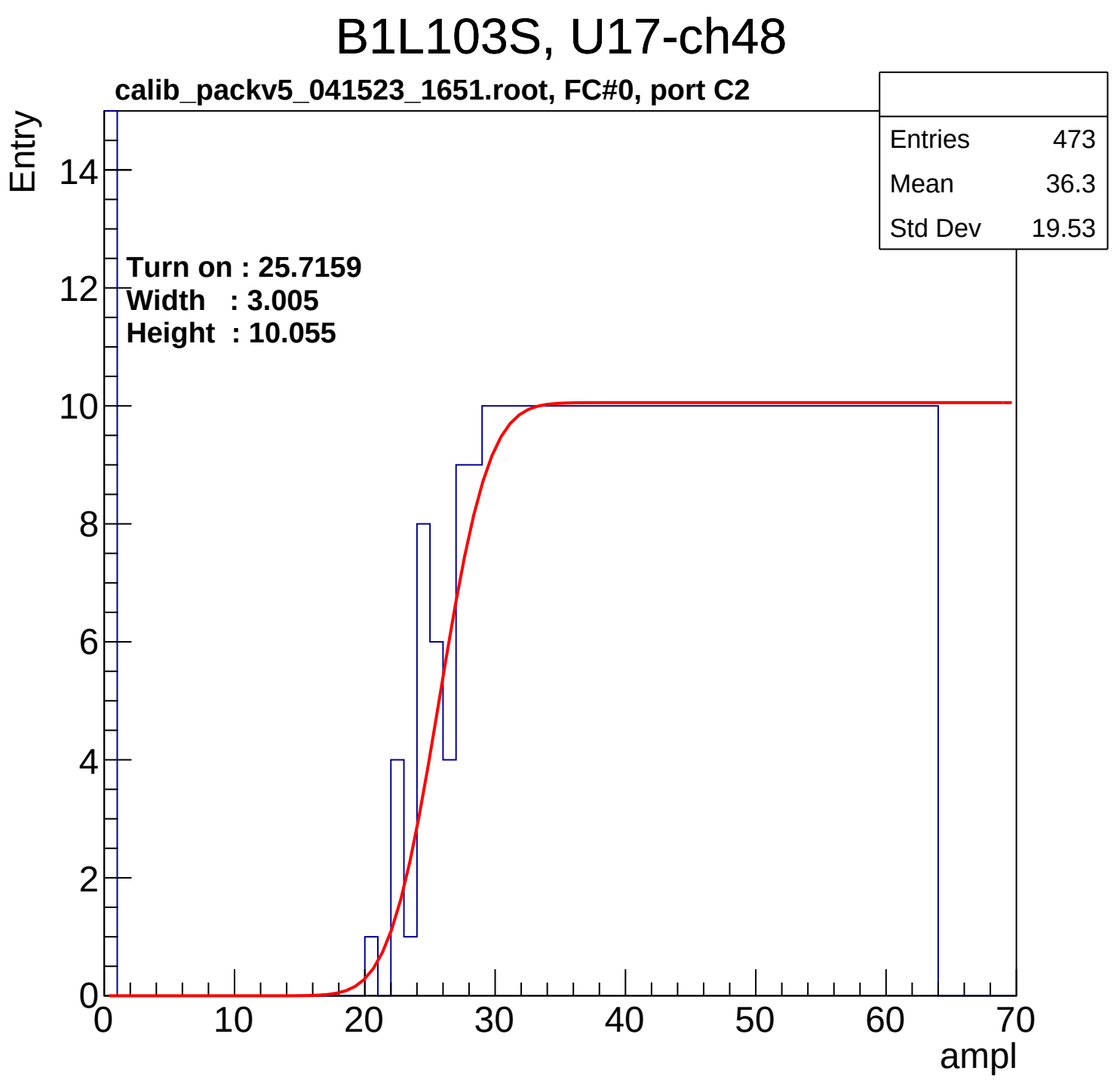
B1L103S, U17-ch48
calib_packv5_041523_1651.root, FC#0, port C2
Entries 473
Mean 36.3
Std Dev 19.53
Turn on : 25.7159
Width : 3.005
Height : 10.055
Entry
ampl
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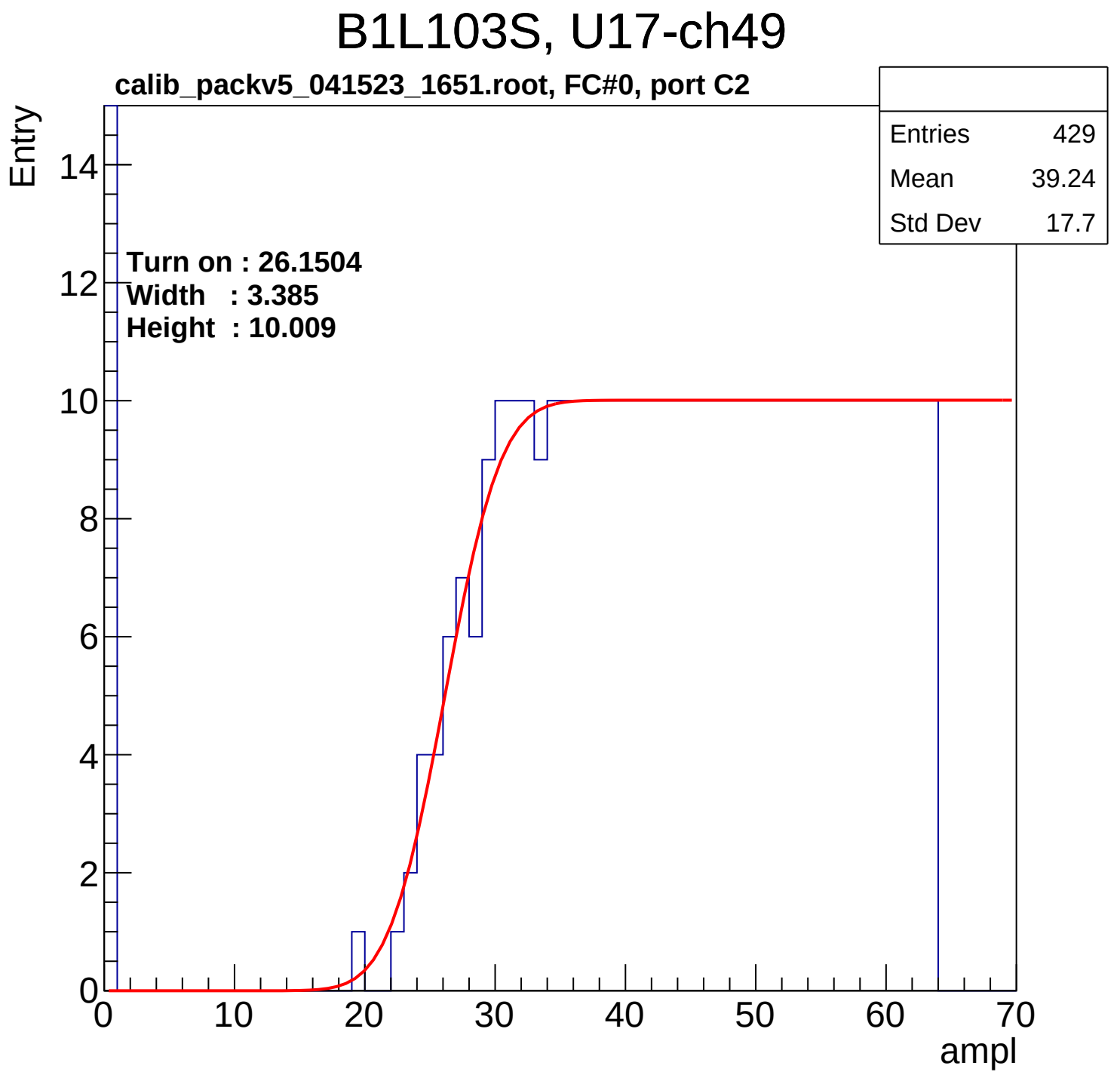
B1L103S, U17-ch49
calib_packv5_041523_1651.root, FC#0, port C2
Entries 429
Mean 39.24
Std Dev 17.7
Turn on : 26.1504
Width : 3.385
Height : 10.009
Entry
ampl
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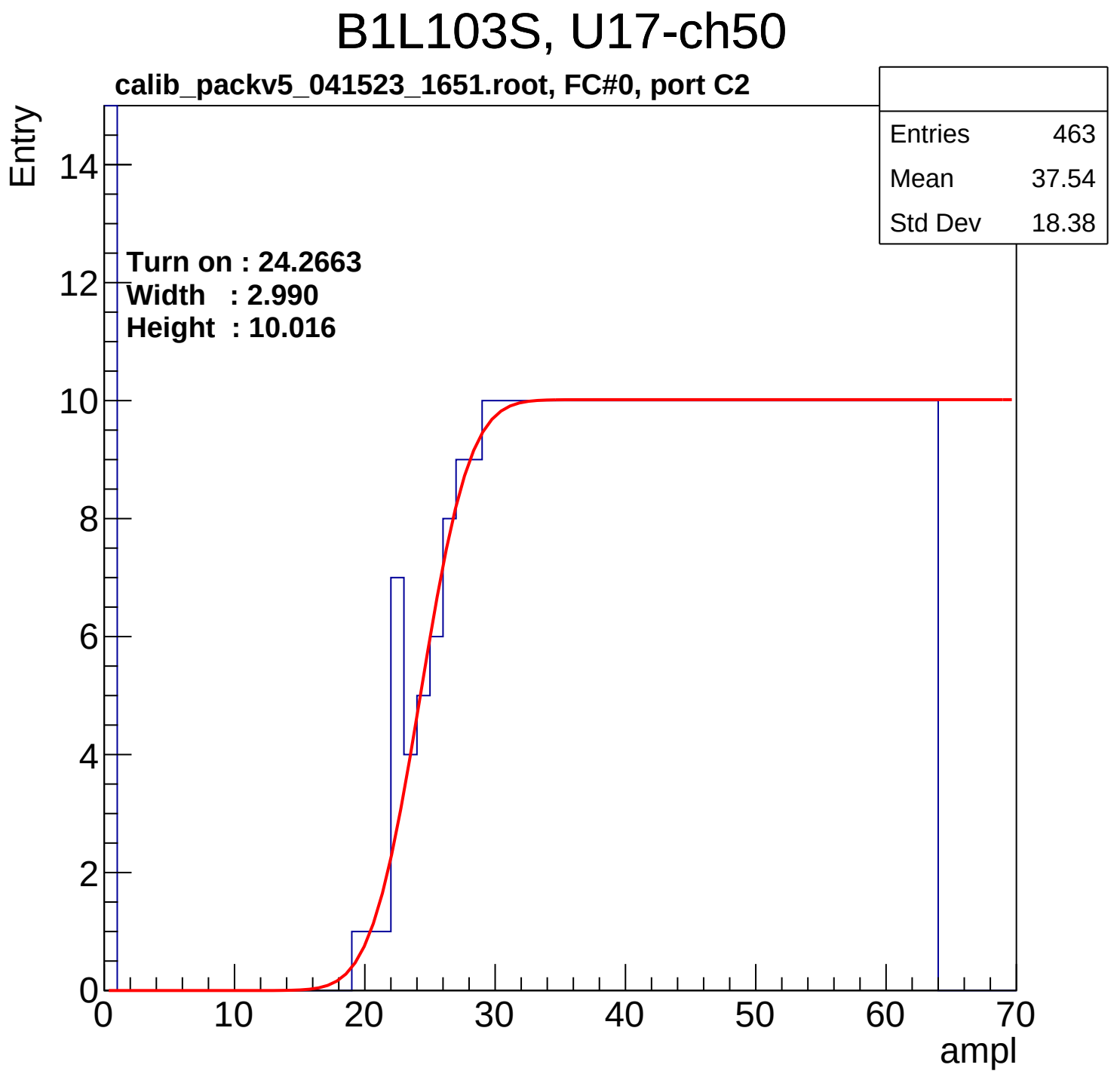
B1L103S, U17-ch50
calib_packv5_041523_1651.root, FC#0, port C2
Entries 463
Mean 37.54
Std Dev 18.38
Turn on : 24.2663
Width : 2.990
Height : 10.016
Entry
ampl
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2
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8
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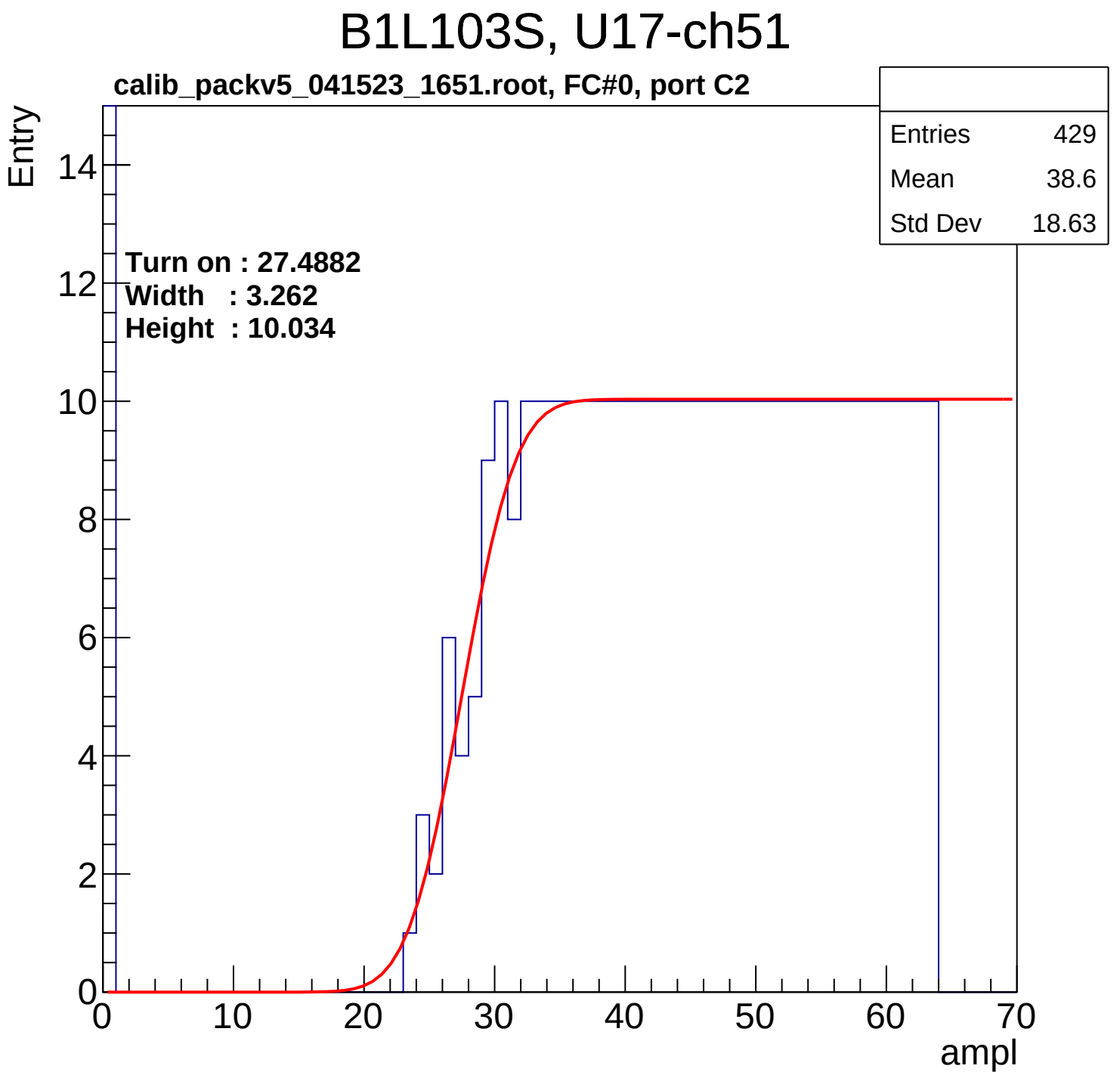
B1L103S, U17-ch51
calib_packv5_041523_1651.root, FC#0, port C2
Entries 429
Mean 38.6
Std Dev 18.63
Turn on : 27.4882
Width : 3.262
Height : 10.034
Entry
ampl
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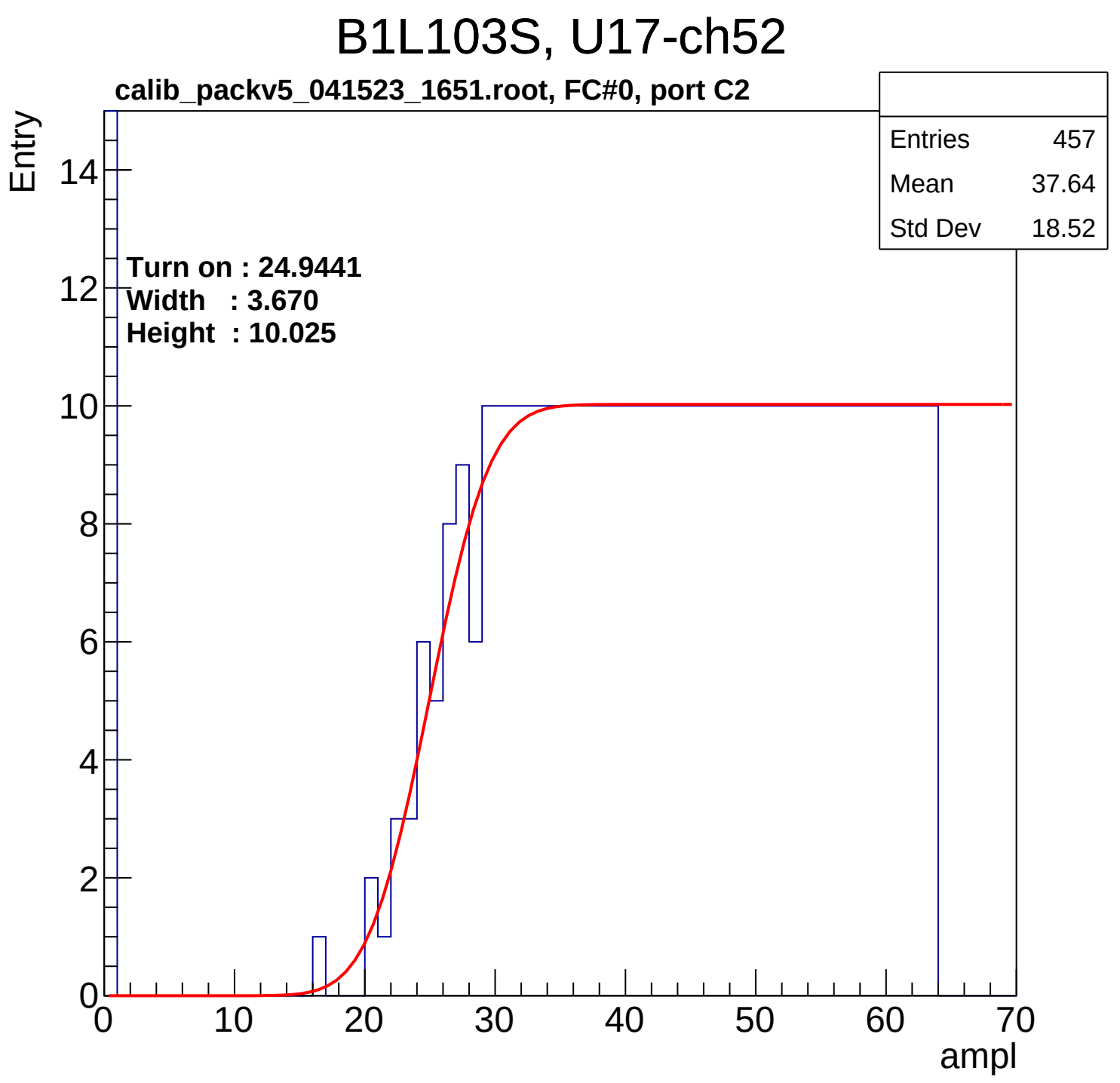
B1L103S, U17-ch52
calib_packv5_041523_1651.root, FC#0, port C2
Entries 457
Mean 37.64
Std Dev 18.52
Turn on : 24.9441
Width : 3.670
Height : 10.025
Entry
ampl
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4
6
8
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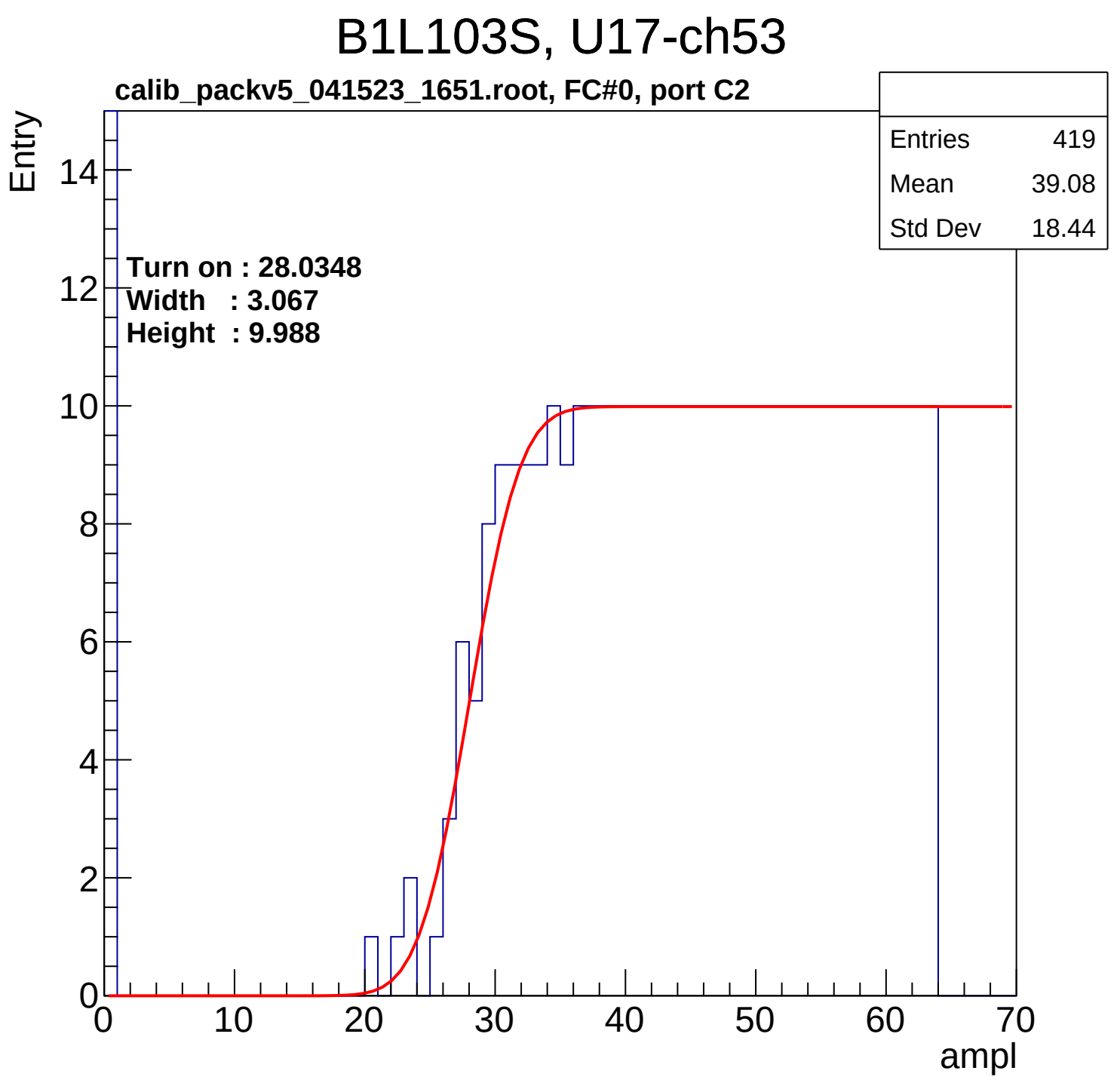
B1L103S, U17-ch53
calib_packv5_041523_1651.root, FC#0, port C2
Entries 419
Mean 39.08
Std Dev 18.44
Turn on : 28.0348
Width : 3.067
Height : 9.988
Entry
ampl
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8
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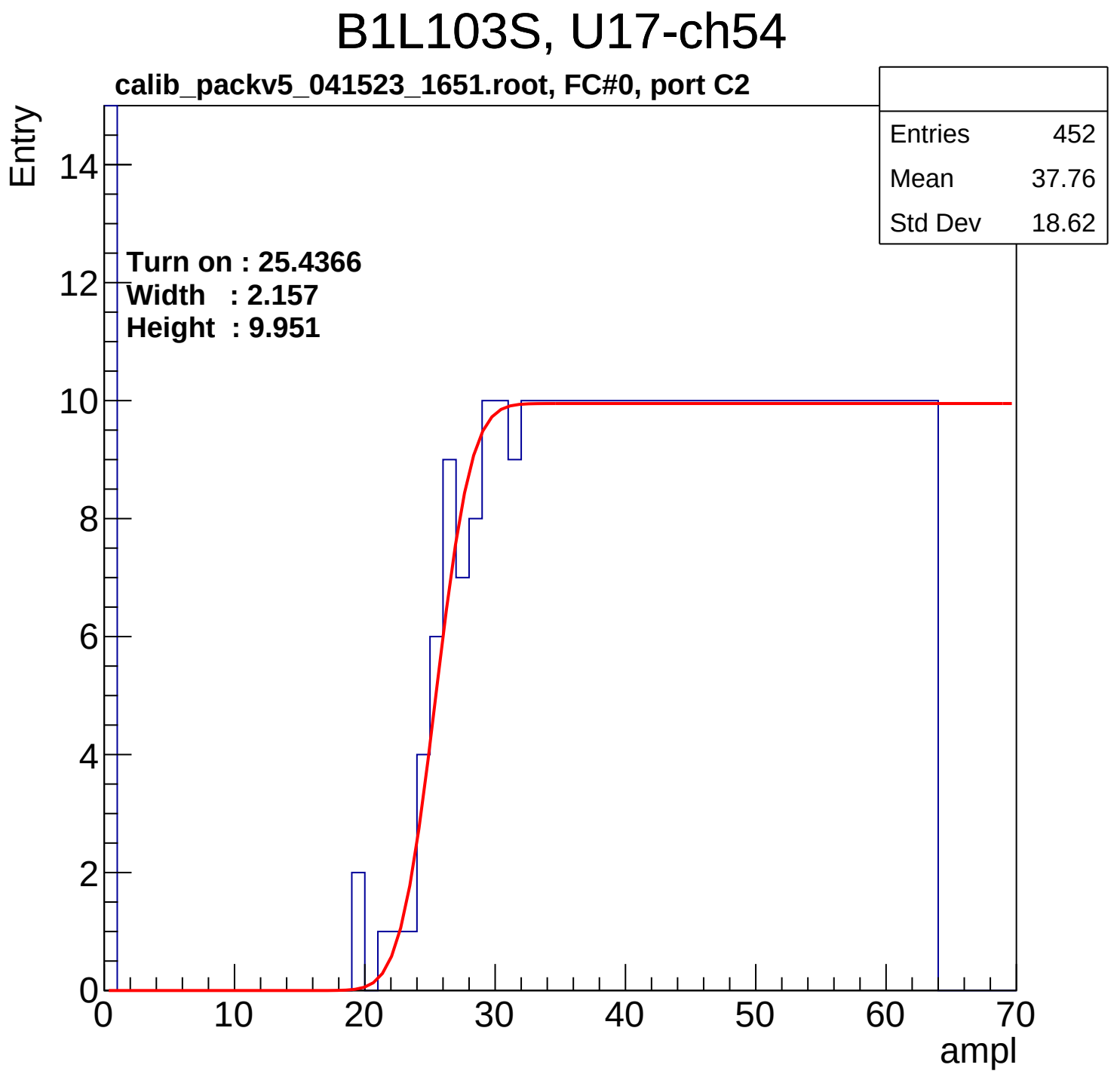
B1L103S, U17-ch54
calib_packv5_041523_1651.root, FC#0, port C2
Entries 452
Mean 37.76
Std Dev 18.62
Turn on : 25.4366
Width : 2.157
Height : 9.951
Entry
ampl
0
2
4
6
8
10
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60
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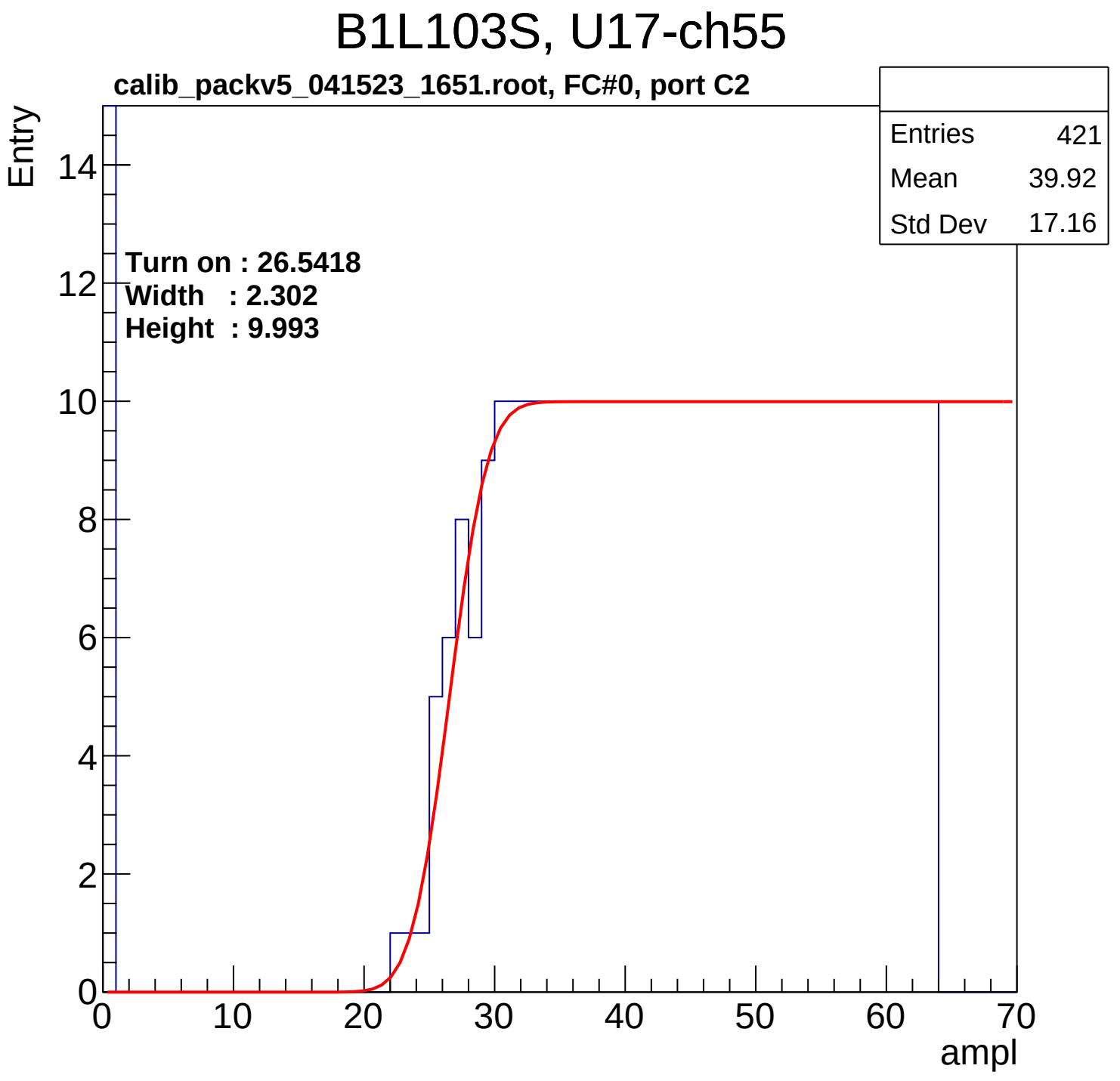
B1L103S, U17-ch55
calib_packv5_041523_1651.root, FC#0, port C2
Entries 421
Mean 39.92
Std Dev 17.16
Turn on : 26.5418
Width : 2.302
Height : 9.993
Entry
ampl
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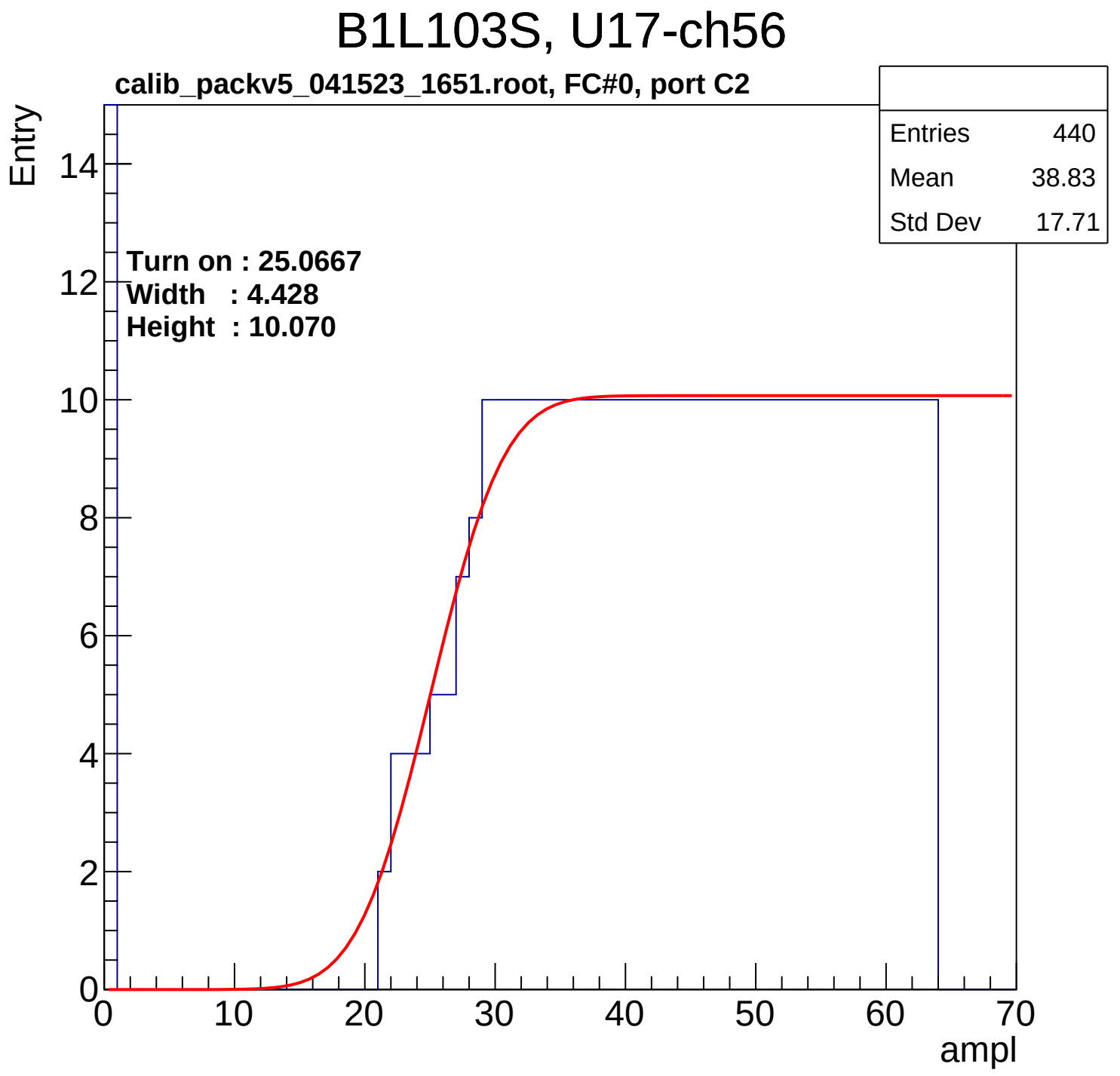
B1L103S, U17-ch56
calib_packv5_041523_1651.root, FC#0, port C2
Entries 440
Mean 38.83
Std Dev 17.71
Turn on : 25.0667
Width : 4.428
Height : 10.070
Entry
ampl
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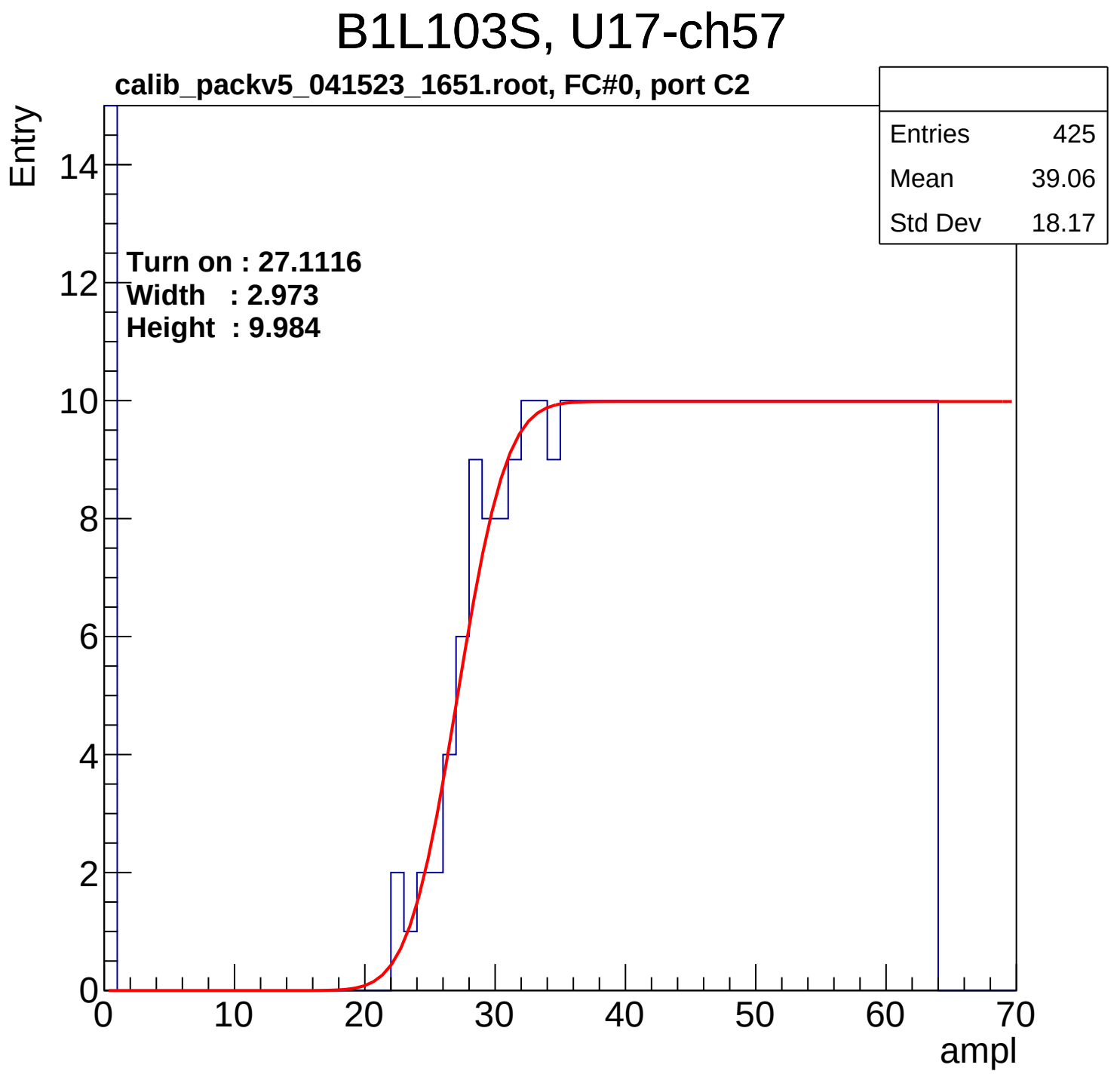
B1L103S, U17-ch57
calib_packv5_041523_1651.root, FC#0, port C2
Entries 425
Mean 39.06
Std Dev 18.17
Turn on : 27.1116
Width : 2.973
Height : 9.984
Entry
ampl
0
2
4
6
8
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12
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10
20
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40
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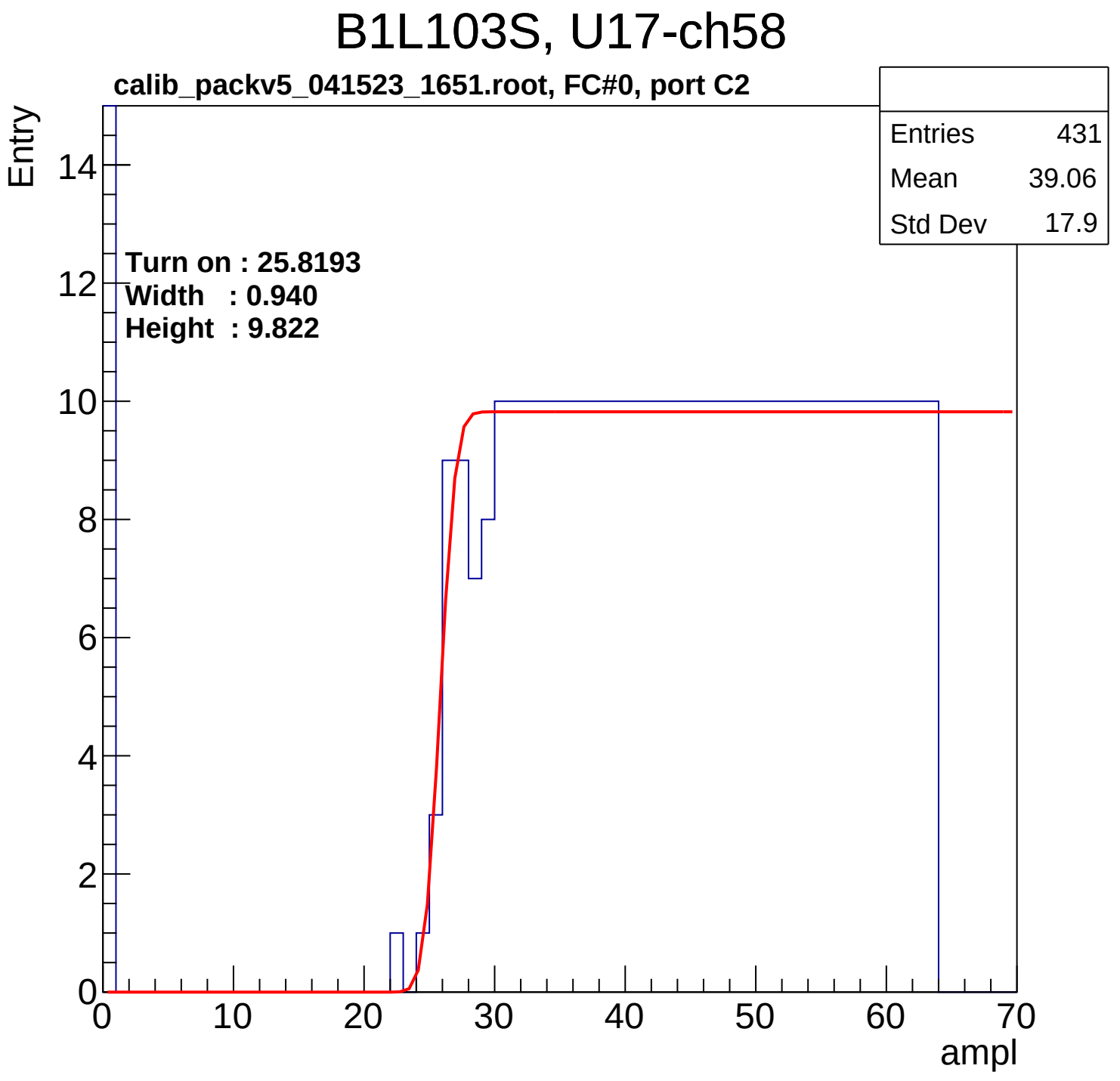
B1L103S, U17-ch58
calib_packv5_041523_1651.root, FC#0, port C2
Entries 431
Mean 39.06
Std Dev 17.9
Turn on : 25.8193
Width : 0.940
Height : 9.822
Entry
ampl
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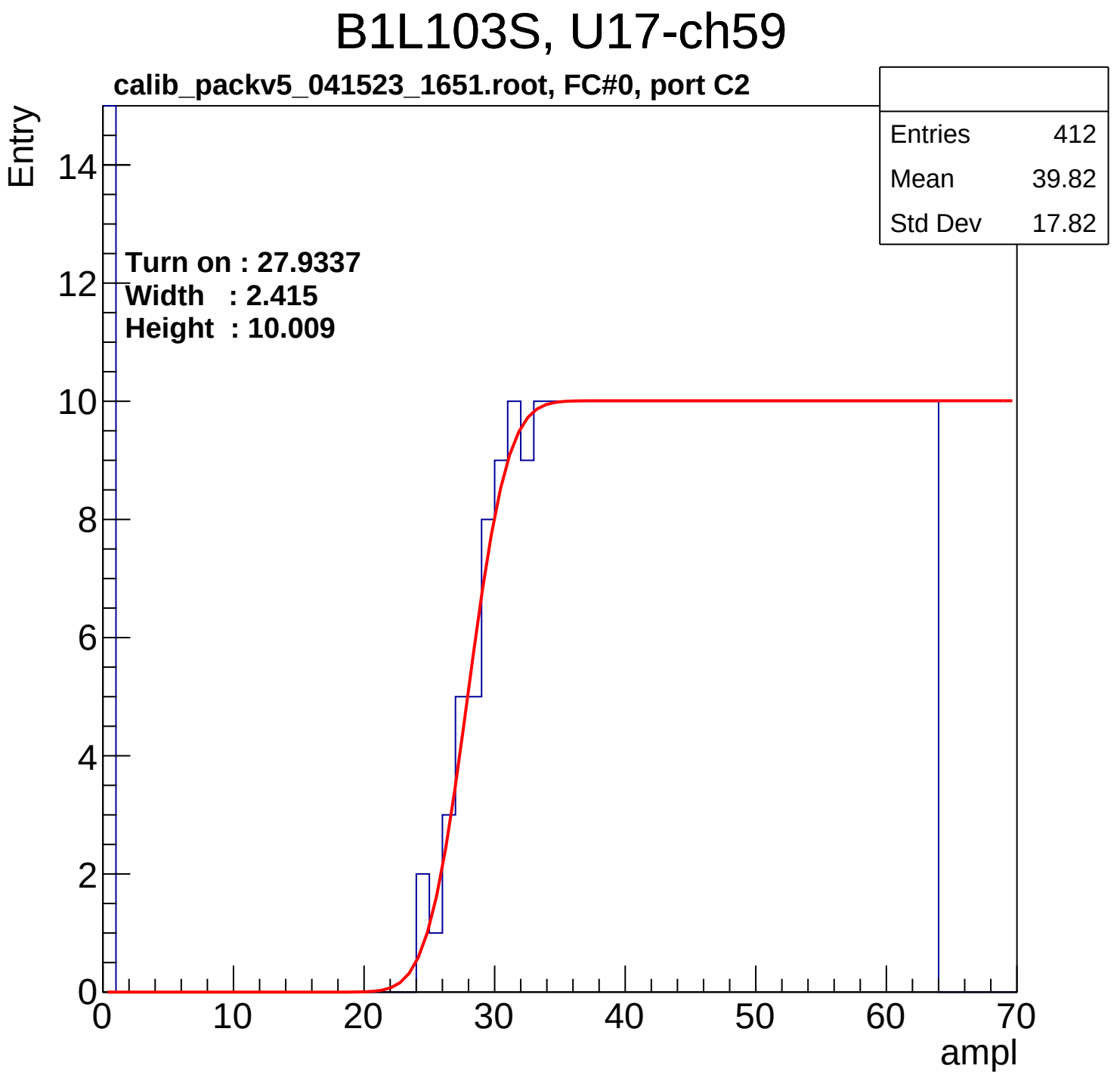
B1L103S, U17-ch59
calib_packv5_041523_1651.root, FC#0, port C2
Entries 412
Mean 39.82
Std Dev 17.82
Turn on : 27.9337
Width : 2.415
Height : 10.009
Entry
ampl
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2
4
6
8
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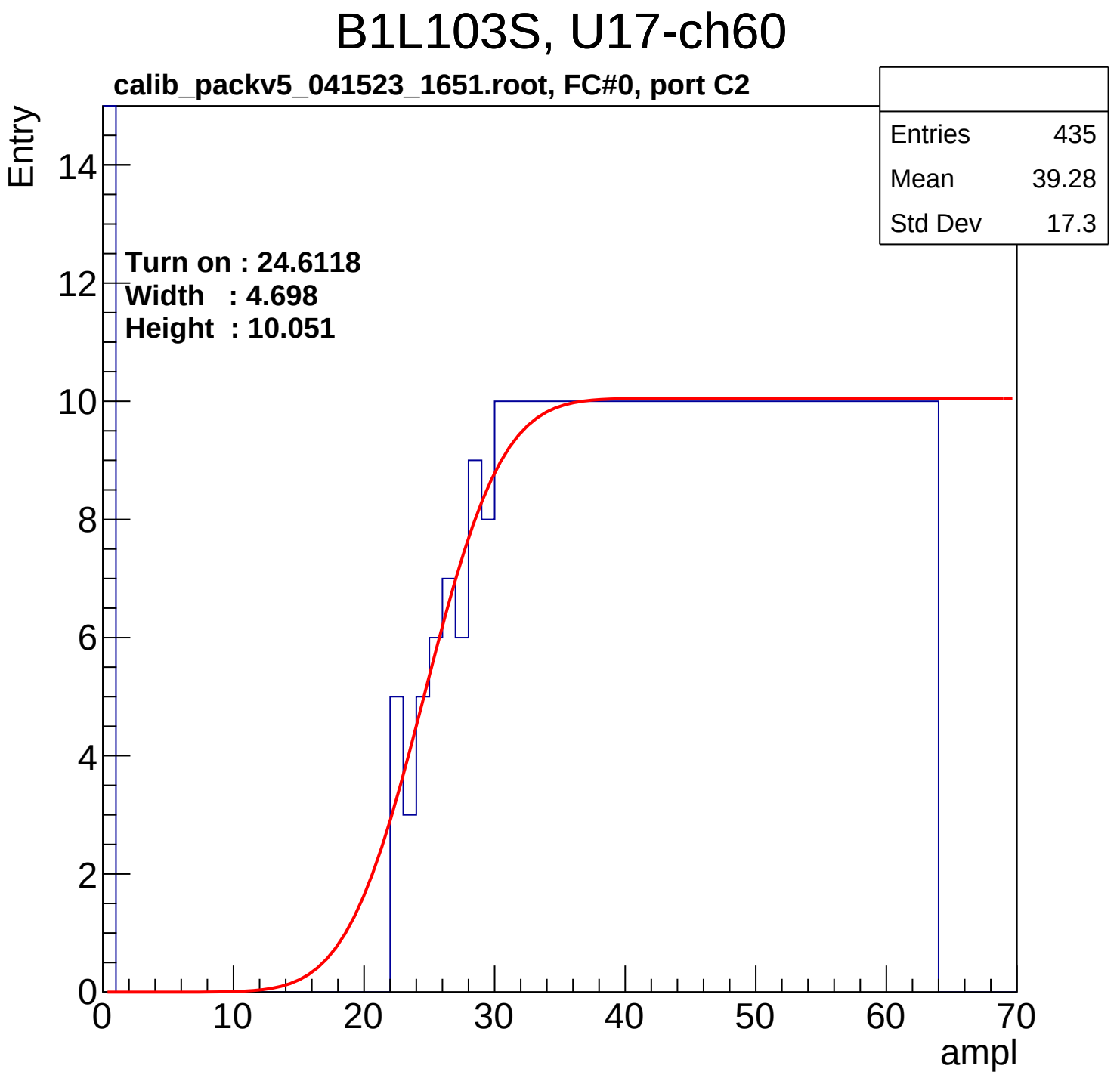
B1L103S, U17-ch60
calib_packv5_041523_1651.root, FC#0, port C2
Entries 435
Mean 39.28
Std Dev 17.3
Turn on : 24.6118
Width : 4.698
Height : 10.051
Entry
ampl
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2
4
6
8
10
12
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0
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60
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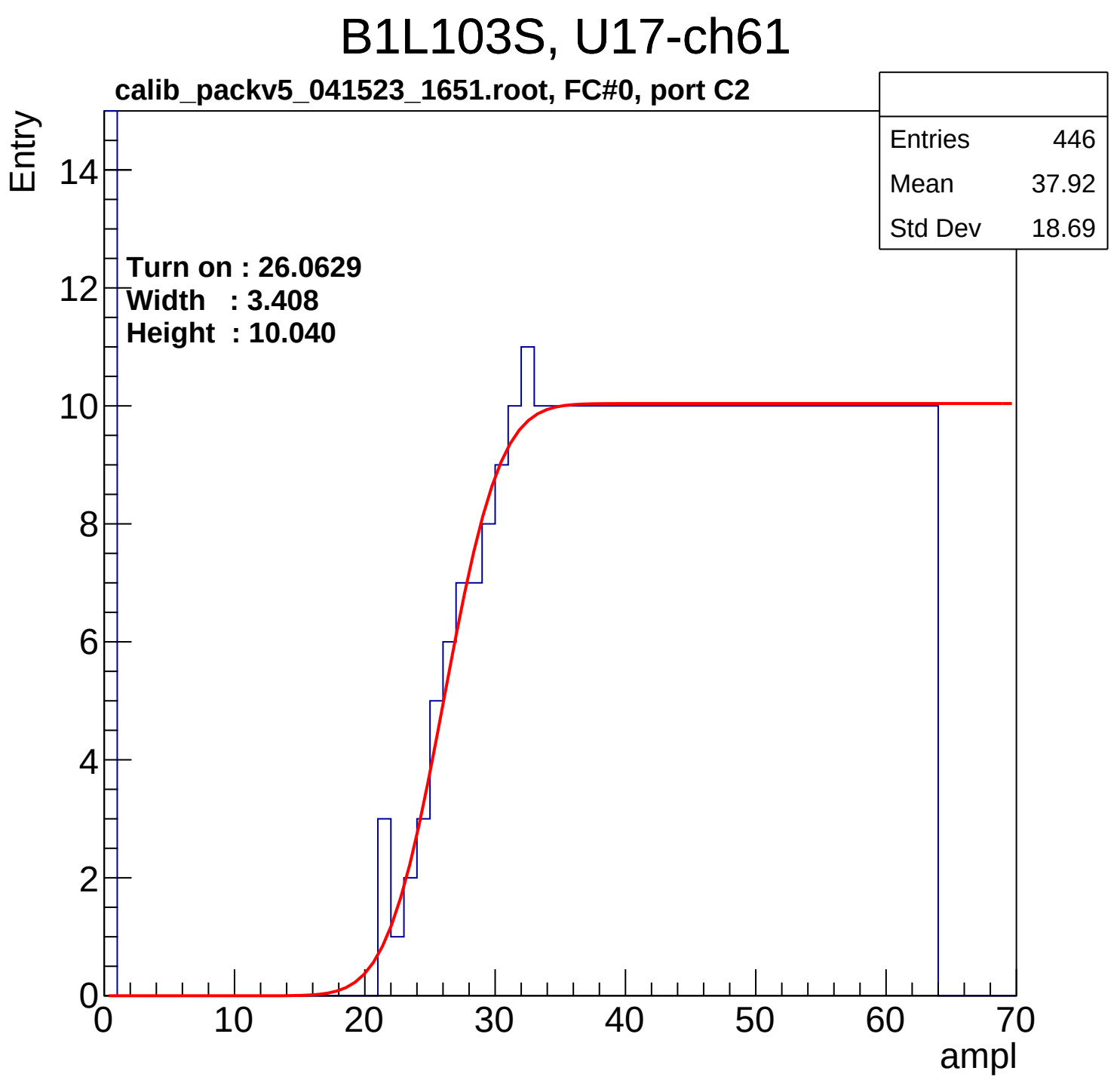
B1L103S, U17-ch61
calib_packv5_041523_1651.root, FC#0, port C2
Entries 446
Mean 37.92
Std Dev 18.69
Turn on : 26.0629
Width : 3.408
Height : 10.040
Entry
ampl
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2
4
6
8
10
12
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0
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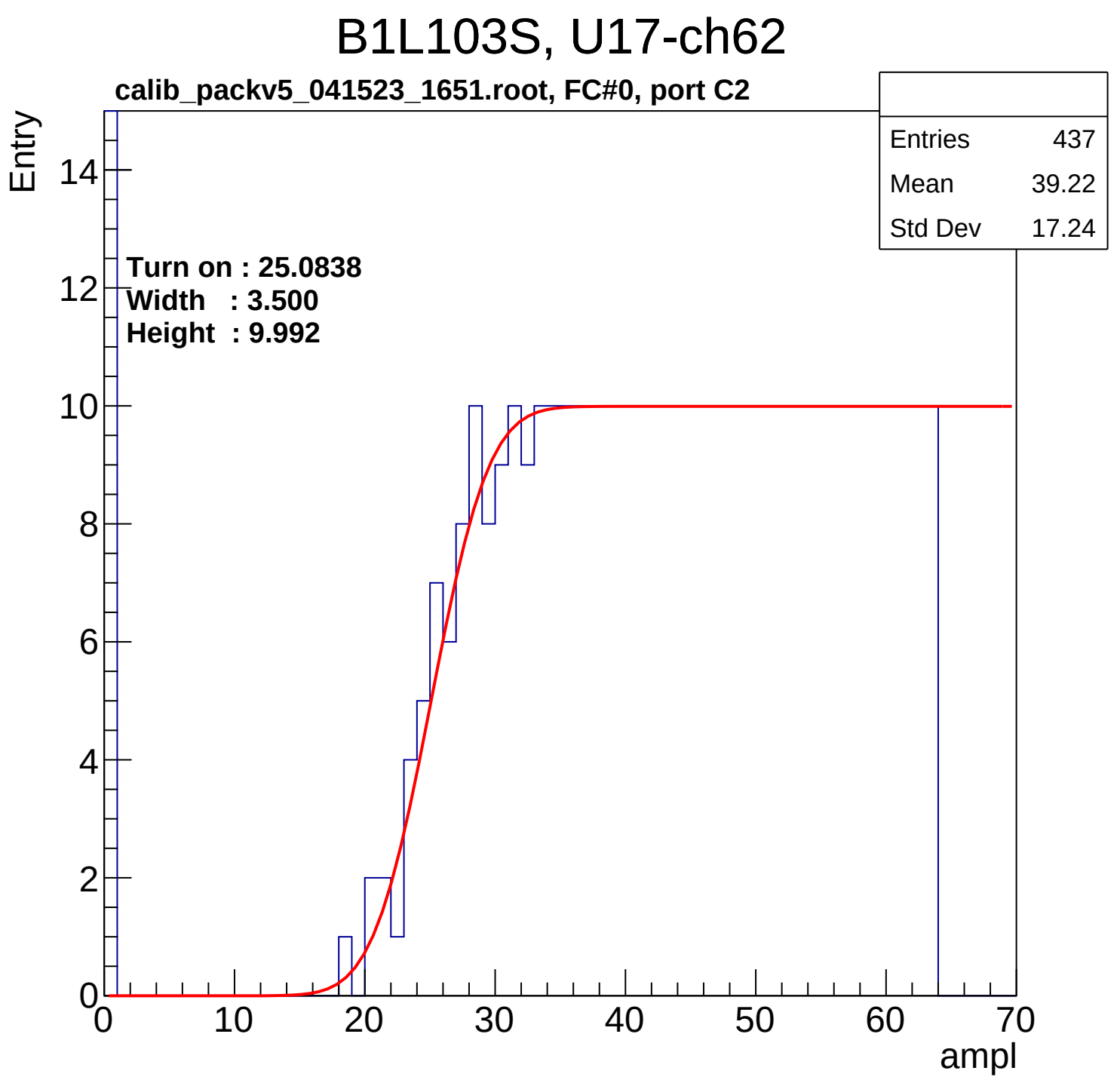
B1L103S, U17-ch62
calib_packv5_041523_1651.root, FC#0, port C2
Entries 437
Mean 39.22
Std Dev 17.24
Turn on : 25.0838
Width : 3.500
Height : 9.992
Entry
ampl
0
2
4
6
8
10
12
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0
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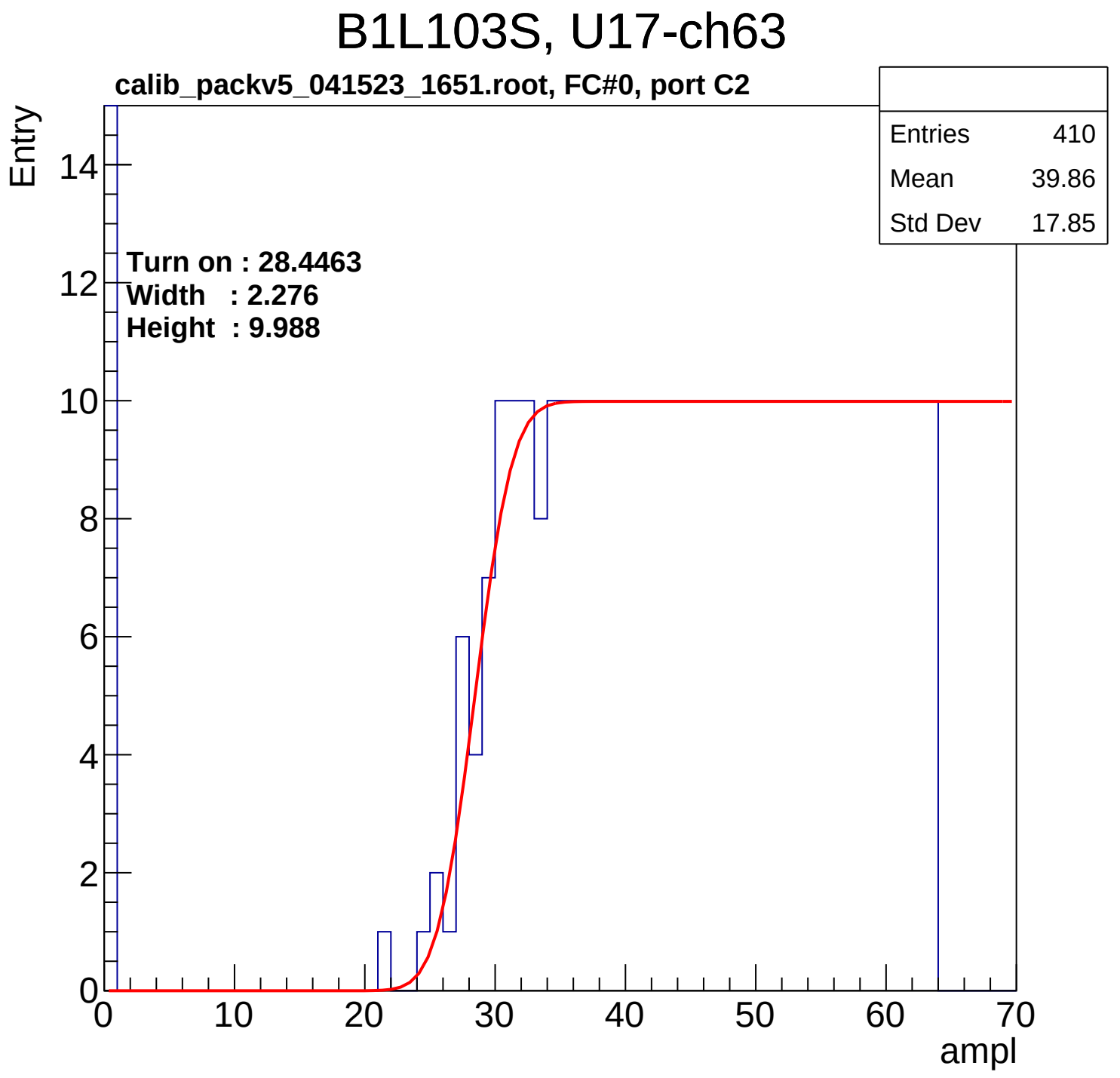
B1L103S, U17-ch63
calib_packv5_041523_1651.root, FC#0, port C2
Entries 410
Mean 39.86
Std Dev 17.85
Turn on : 28.4463
Width : 2.276
Height : 9.988
Entry
ampl
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2
4
6
8
10
12
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0
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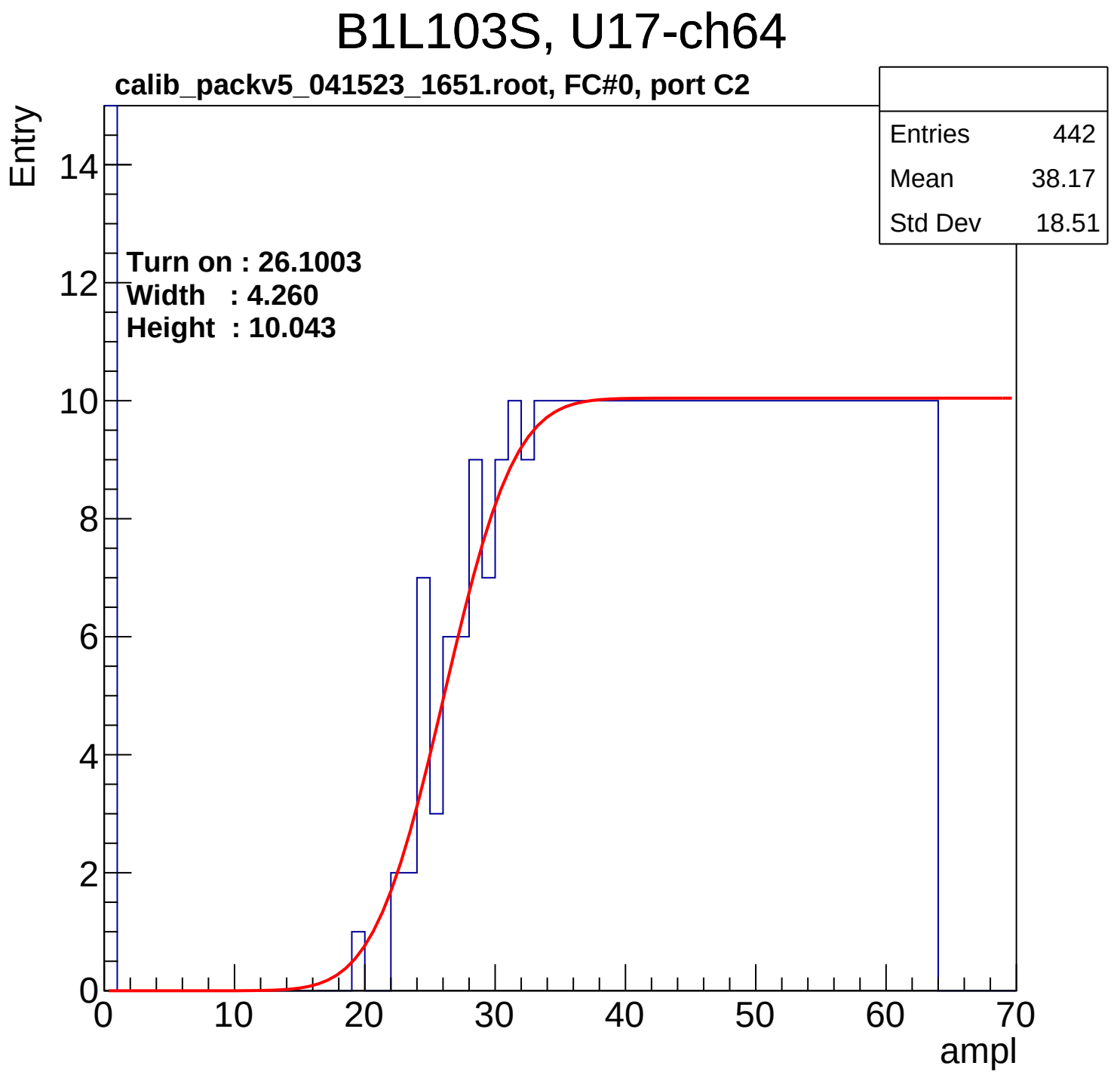
B1L103S, U17-ch64
calib_packv5_041523_1651.root, FC#0, port C2
Entries 442
Mean 38.17
Std Dev 18.51
Turn on : 26.1003
Width : 4.260
Height : 10.043
Entry
ampl
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6
8
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12
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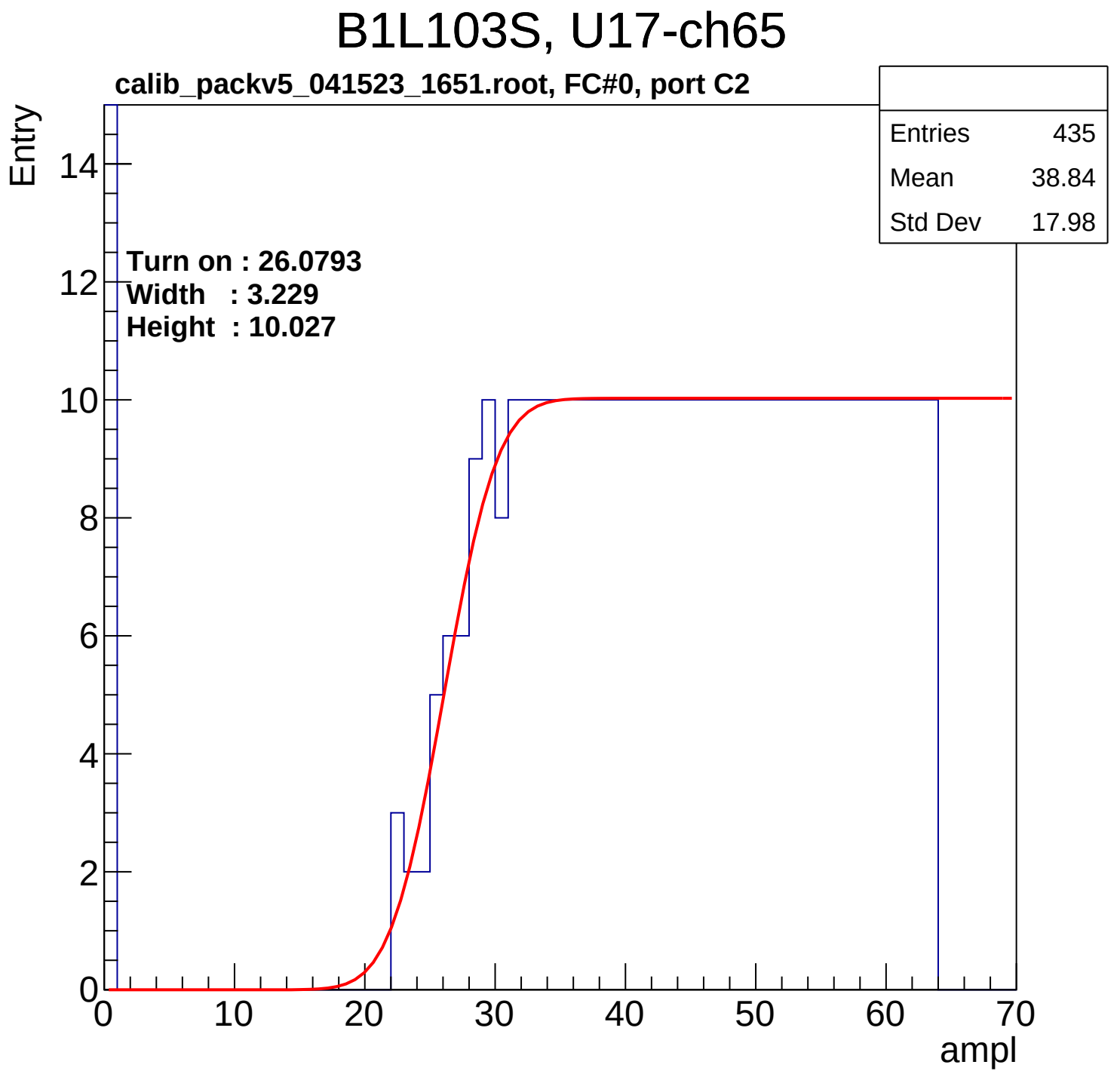
B1L103S, U17-ch65
calib_packv5_041523_1651.root, FC#0, port C2
Entries 435
Mean 38.84
Std Dev 17.98
Turn on : 26.0793
Width : 3.229
Height : 10.027
Entry
ampl
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6
8
10
12
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0
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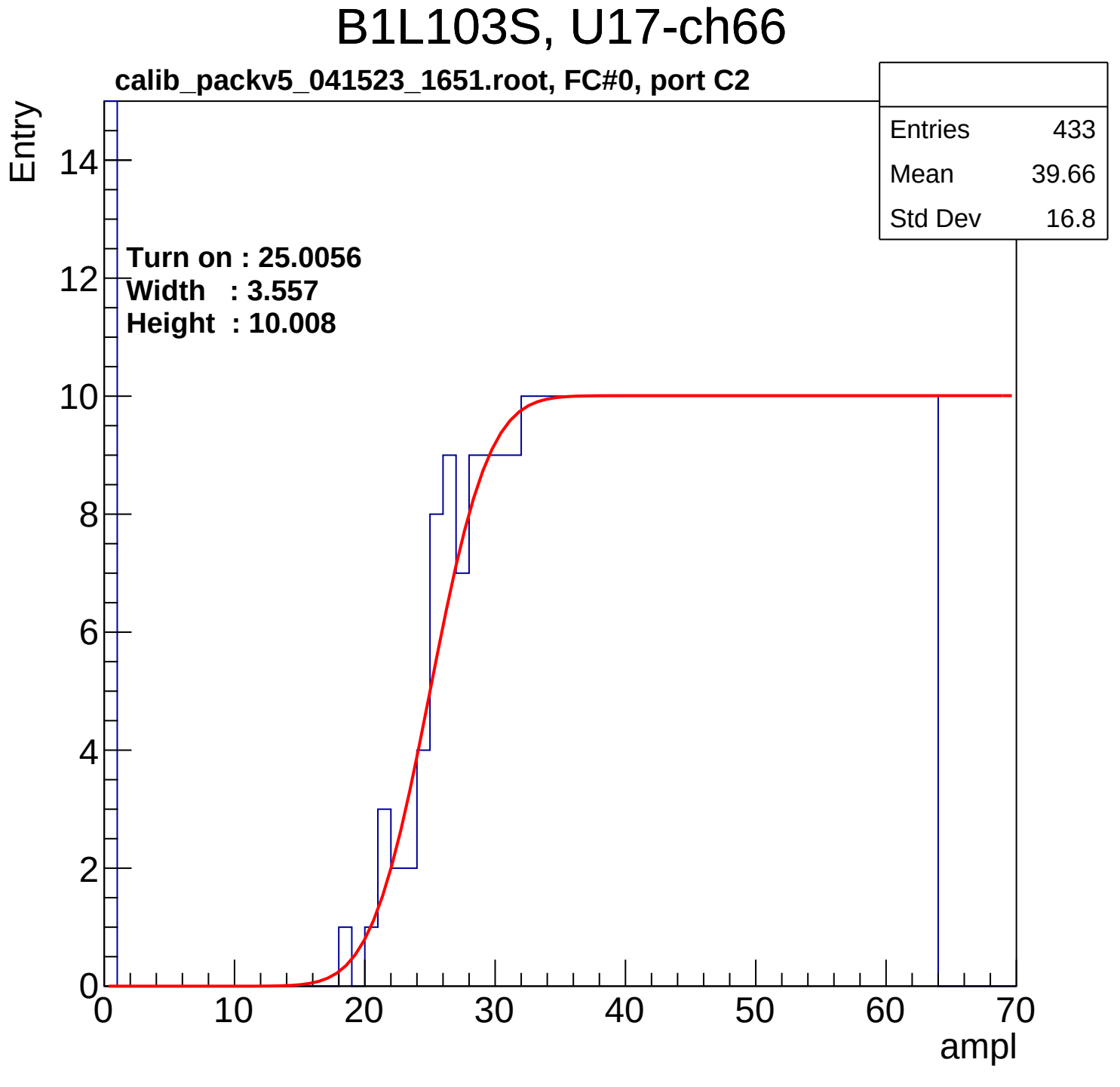
B1L103S, U17-ch66
calib_packv5_041523_1651.root, FC#0, port C2
Entries 433
Mean 39.66
Std Dev 16.8
Turn on : 25.0056
Width : 3.557
Height : 10.008
Entry
ampl
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6
8
10
12
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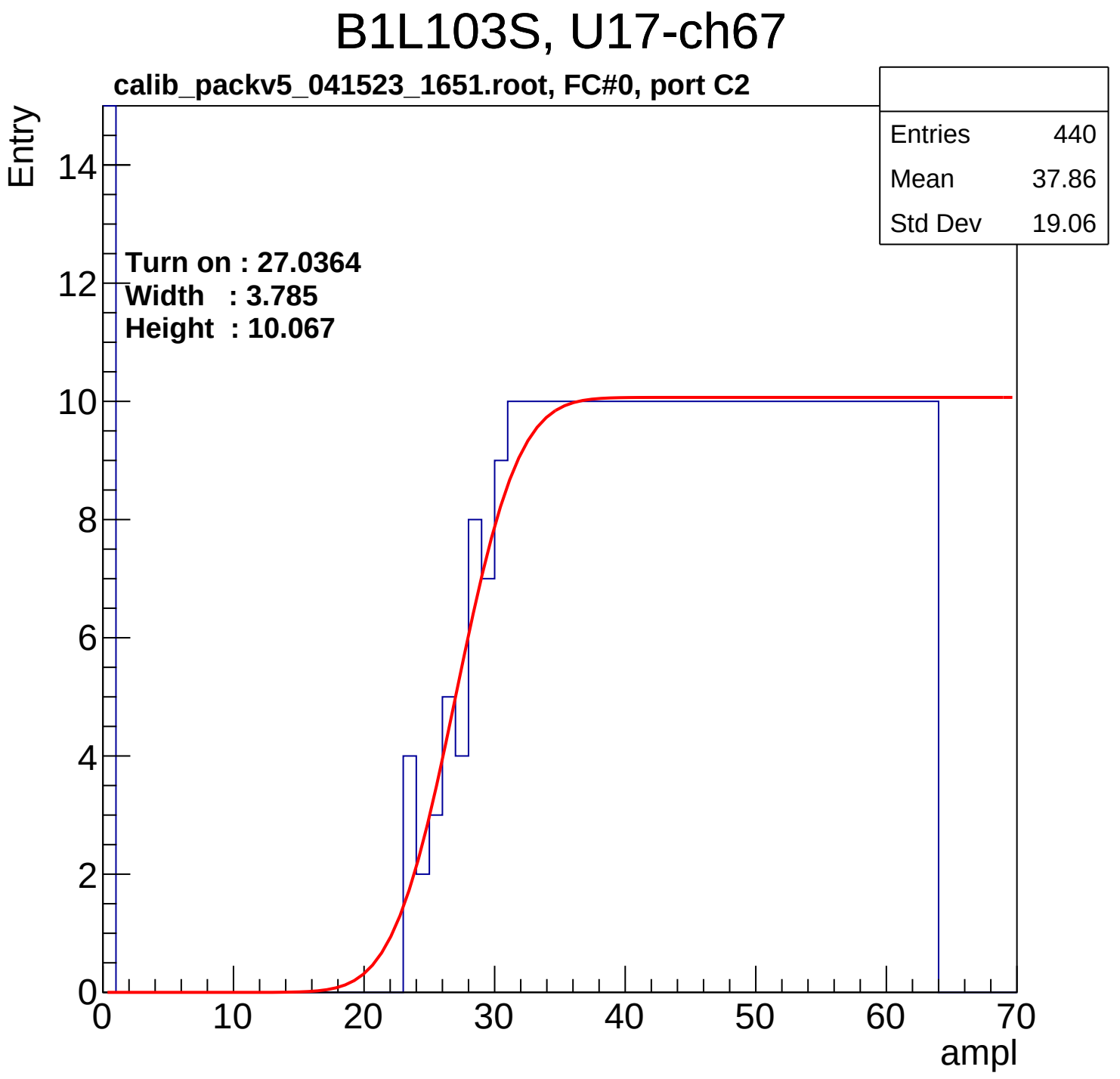
B1L103S, U17-ch67
calib_packv5_041523_1651.root, FC#0, port C2
Entries 440
Mean 37.86
Std Dev 19.06
Turn on : 27.0364
Width : 3.785
Height : 10.067
Entry
ampl
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4
6
8
10
12
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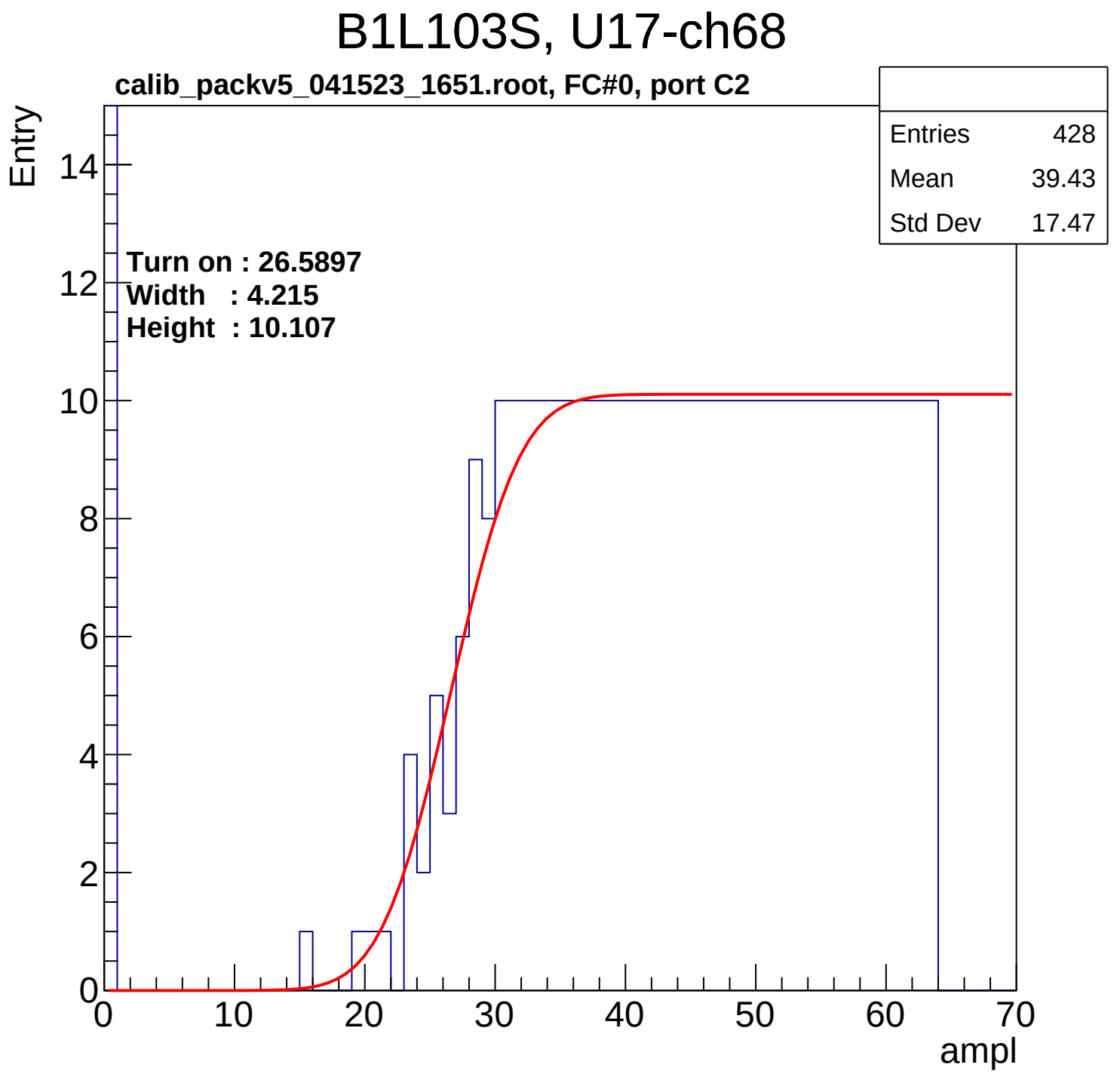
B1L103S, U17-ch68
calib_packv5_041523_1651.root, FC#0, port C2
Entries 428
Mean 39.43
Std Dev 17.47
Turn on : 26.5897
Width : 4.215
Height : 10.107
Entry
ampl
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4
6
8
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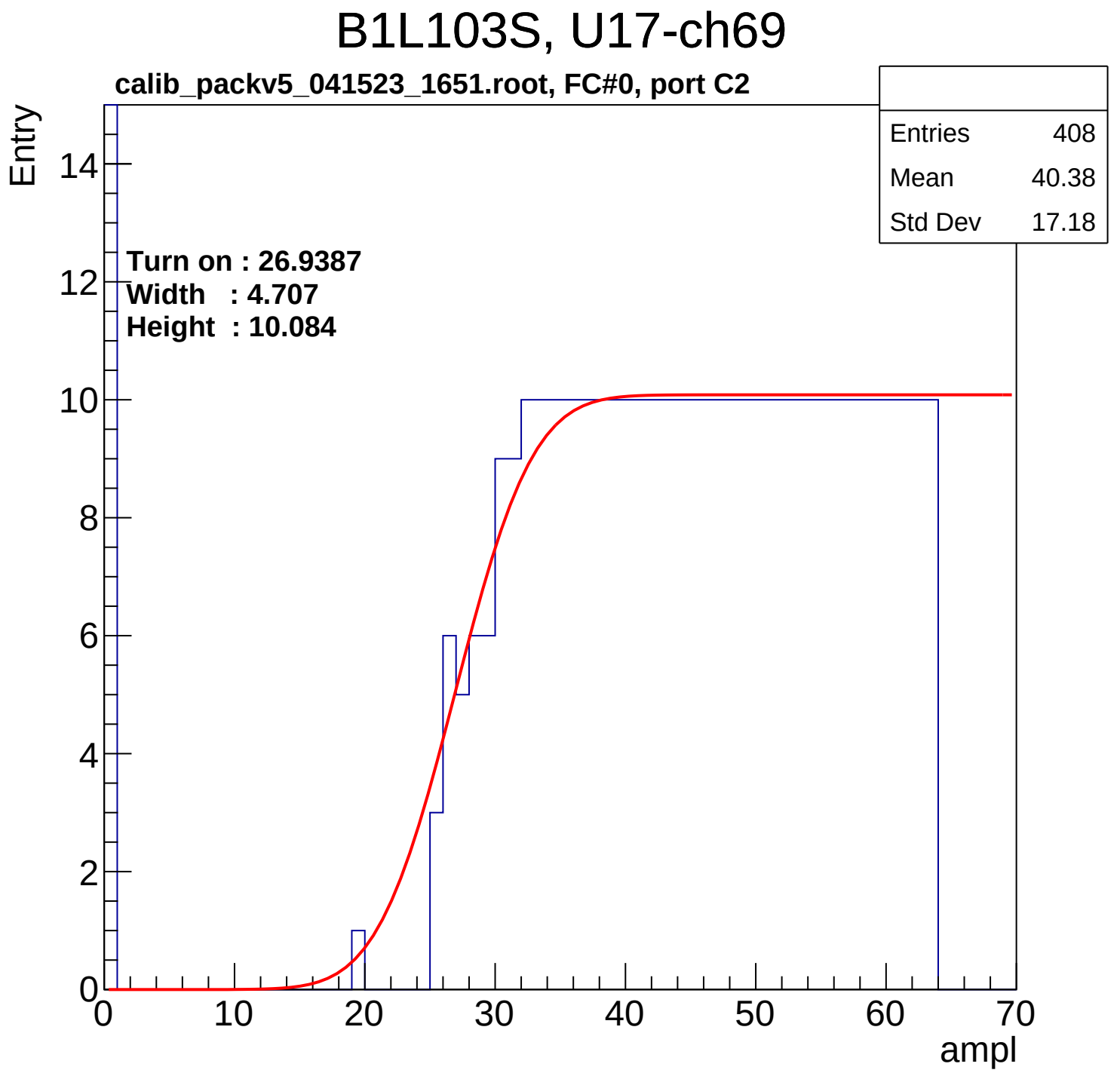
B1L103S, U17-ch69
calib_packv5_041523_1651.root, FC#0, port C2
Entries 408
Mean 40.38
Std Dev 17.18
Turn on : 26.9387
Width : 4.707
Height : 10.084
Entry
ampl
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6
8
10
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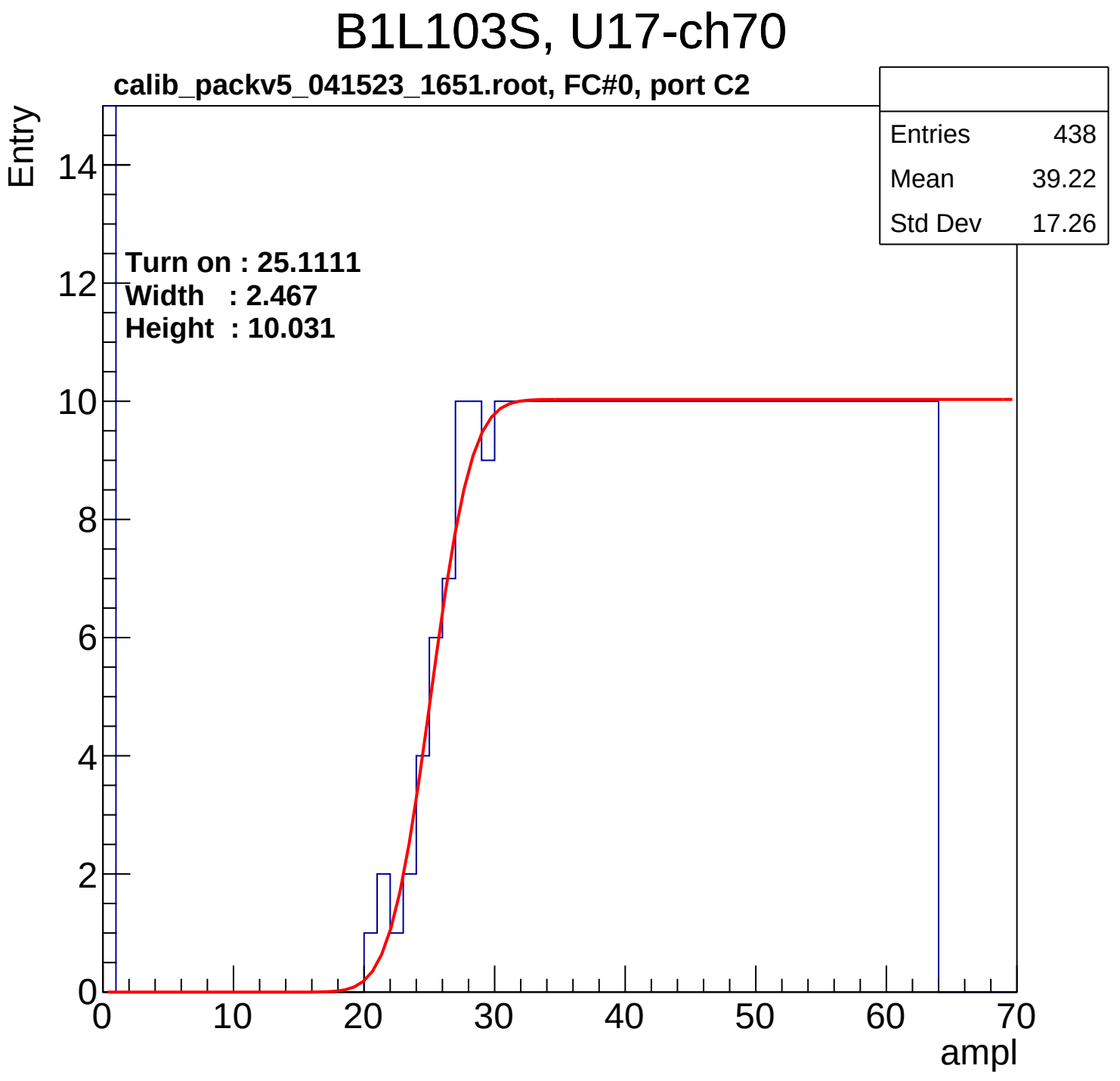
B1L103S, U17-ch70
calib_packv5_041523_1651.root, FC#0, port C2
Entries 438
Mean 39.22
Std Dev 17.26
Turn on : 25.1111
Width : 2.467
Height : 10.031
Entry
ampl
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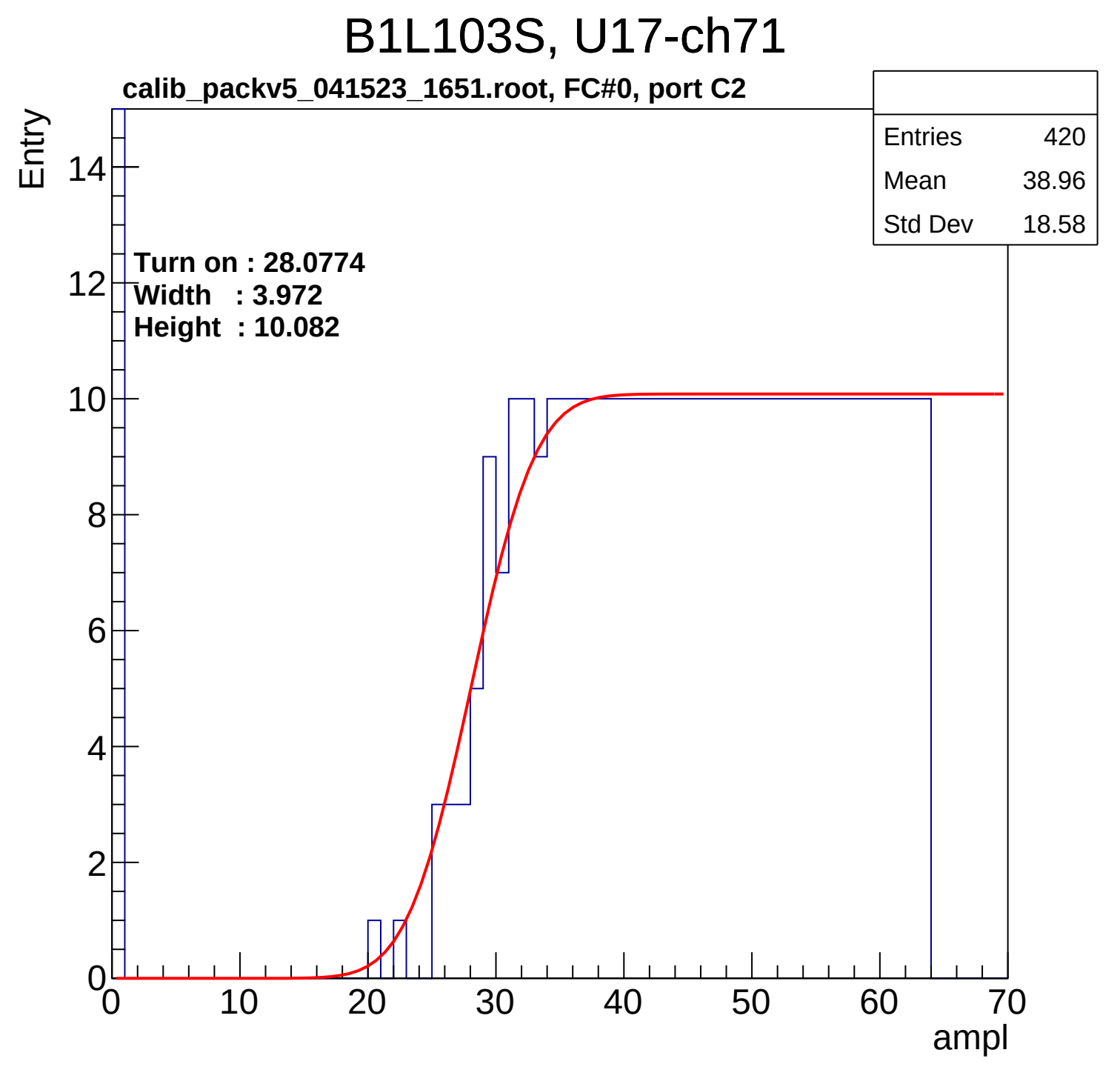
B1L103S, U17-ch71
calib_packv5_041523_1651.root, FC#0, port C2
Entries 420
Mean 38.96
Std Dev 18.58
Turn on : 28.0774
Width : 3.972
Height : 10.082
Entry
ampl
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6
8
10
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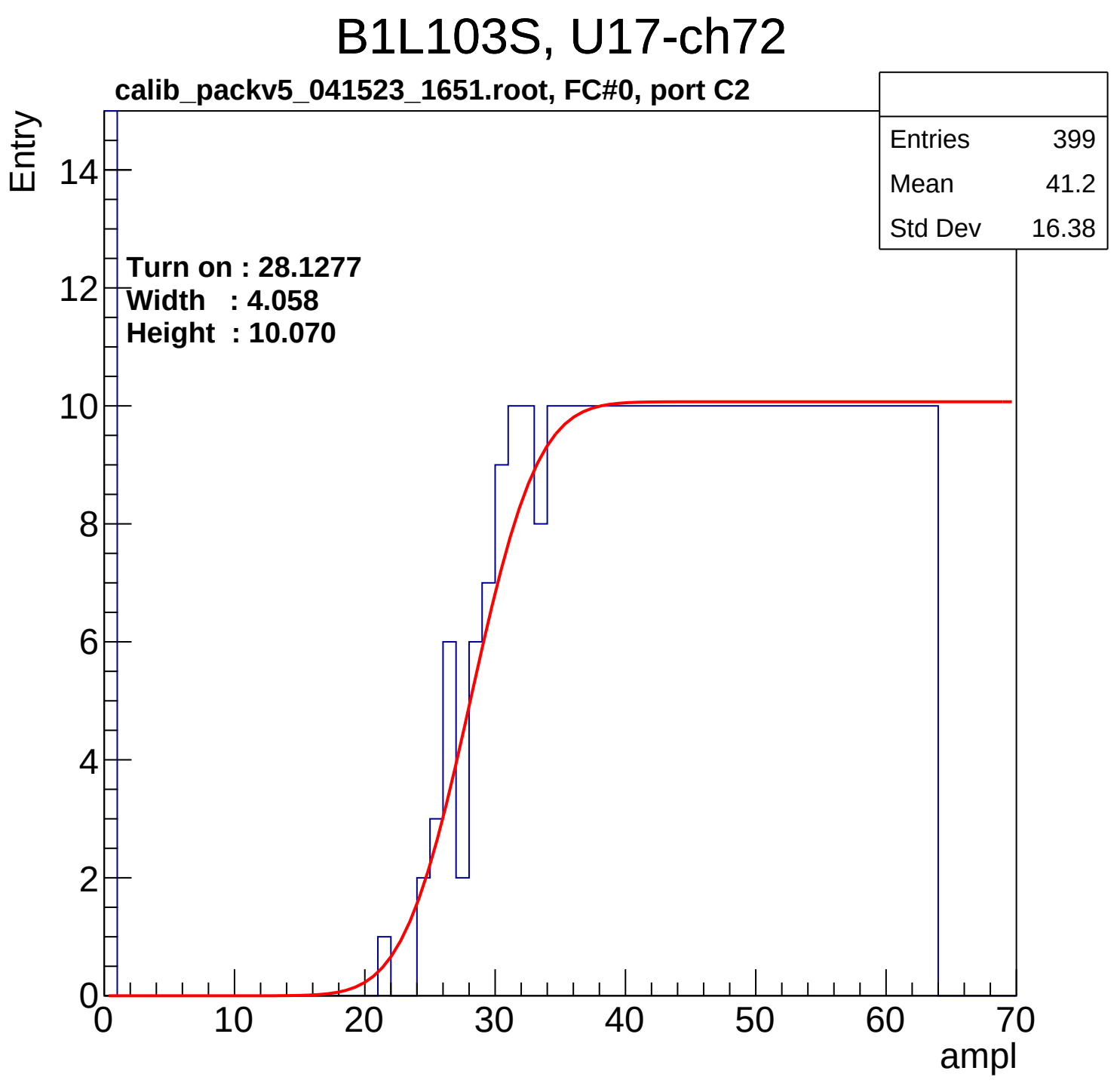
B1L103S, U17-ch72
calib_packv5_041523_1651.root, FC#0, port C2
Entries 399
Mean 41.2
Std Dev 16.38
Turn on : 28.1277
Width : 4.058
Height : 10.070
Entry
ampl
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2
4
6
8
10
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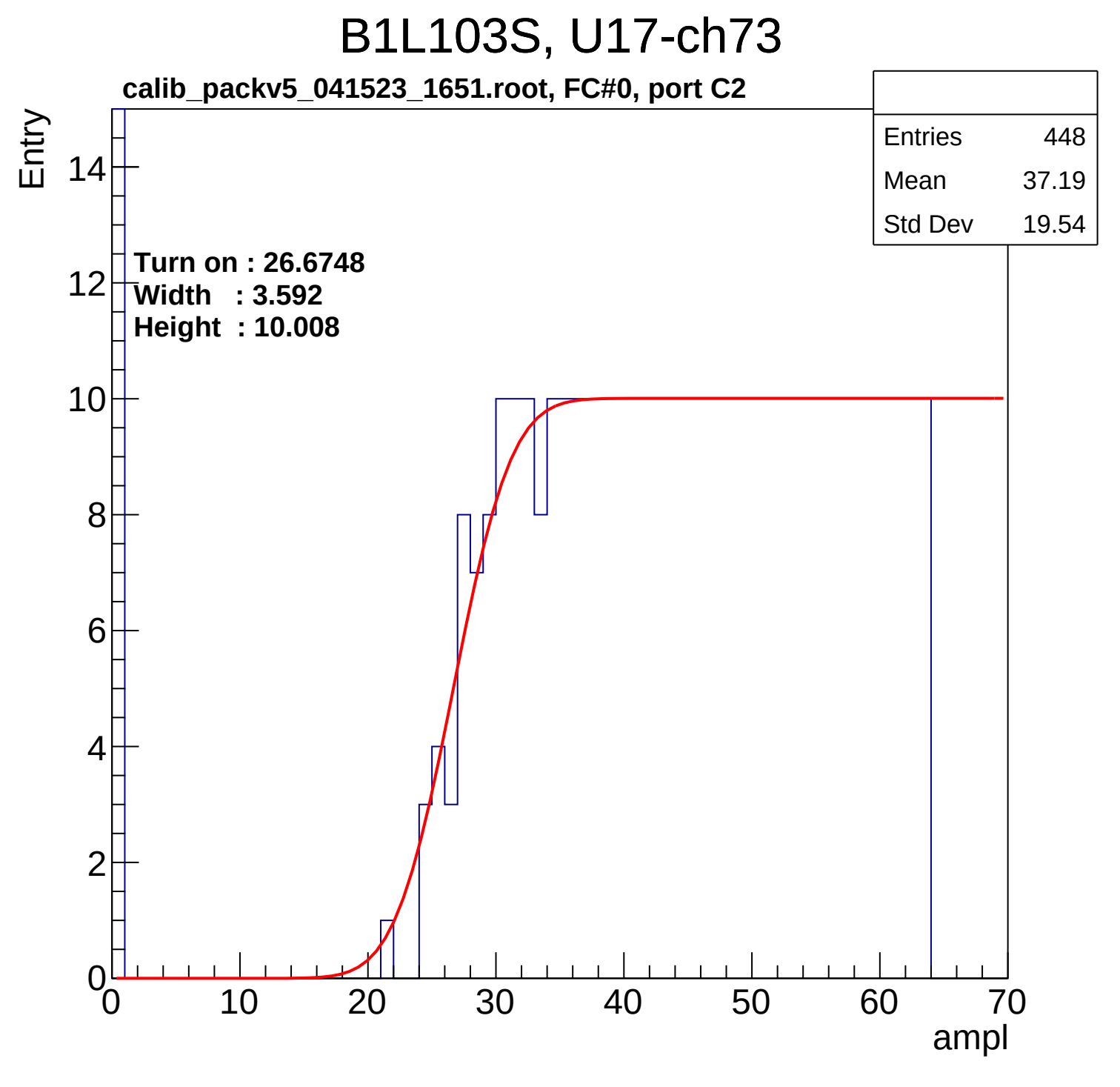
B1L103S, U17-ch73
calib_packv5_041523_1651.root, FC#0, port C2
Entries 448
Mean 37.19
Std Dev 19.54
Turn on : 26.6748
Width : 3.592
Height : 10.008
Entry
ampl
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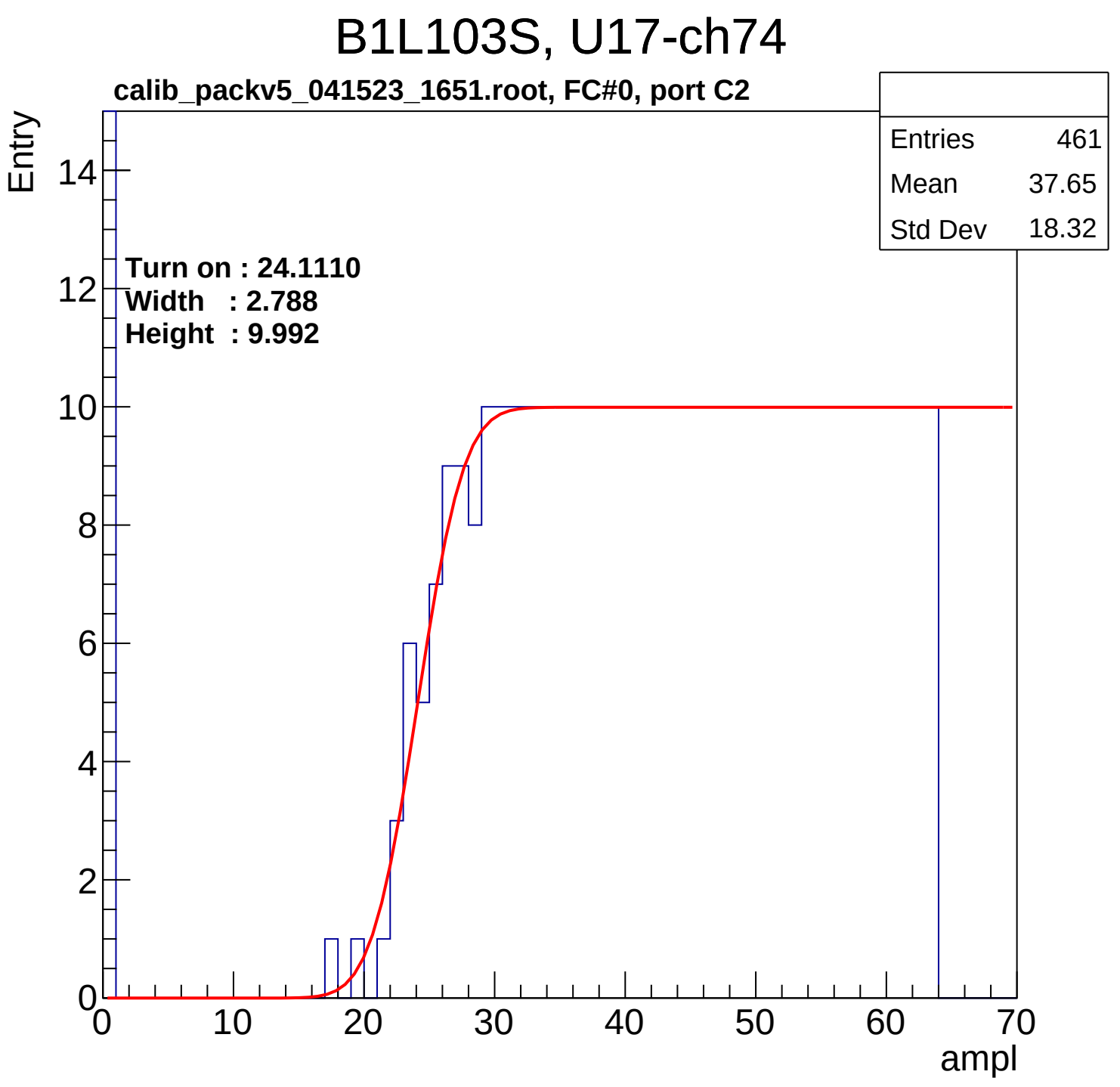
B1L103S, U17-ch74
calib_packv5_041523_1651.root, FC#0, port C2
Entries 461
Mean 37.65
Std Dev 18.32
Turn on : 24.1110
Width : 2.788
Height : 9.992
Entry
ampl
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6
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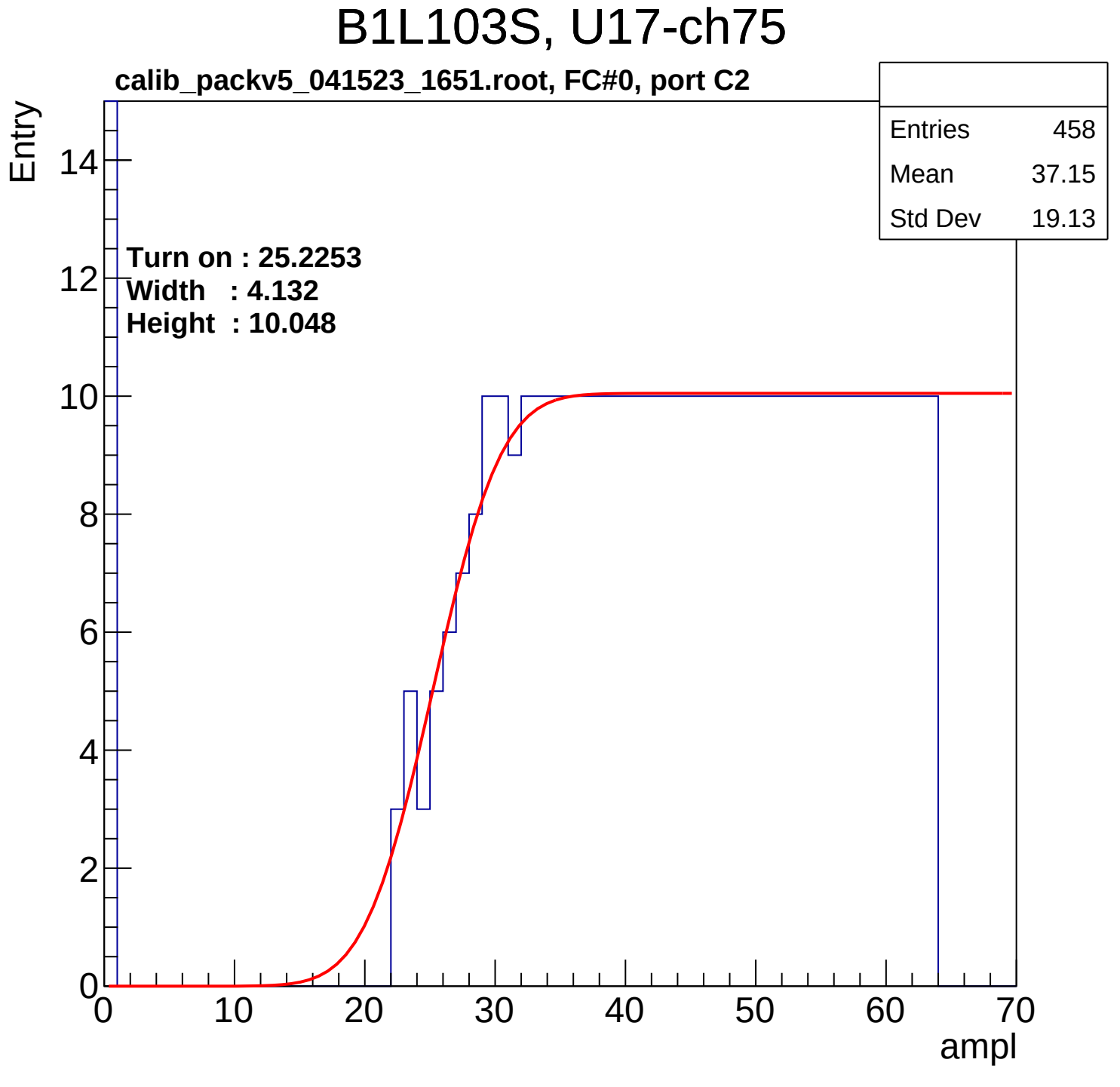
B1L103S, U17-ch75
calib_packv5_041523_1651.root, FC#0, port C2
Entries 458
Mean 37.15
Std Dev 19.13
Turn on : 25.2253
Width : 4.132
Height : 10.048
Entry
ampl
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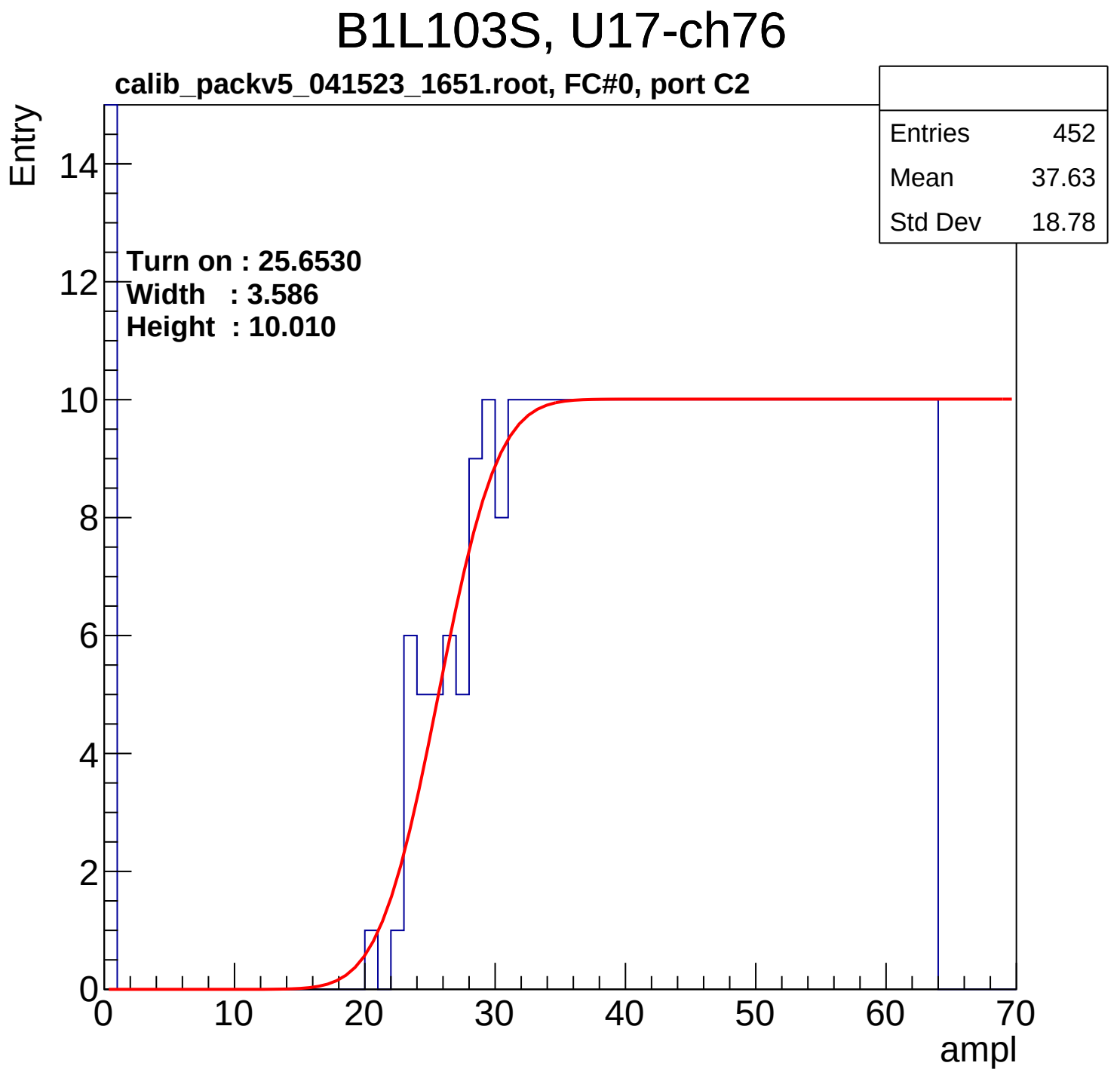
B1L103S, U17-ch76
calib_packv5_041523_1651.root, FC#0, port C2
Entries 452
Mean 37.63
Std Dev 18.78
Turn on : 25.6530
Width : 3.586
Height : 10.010
Entry
ampl
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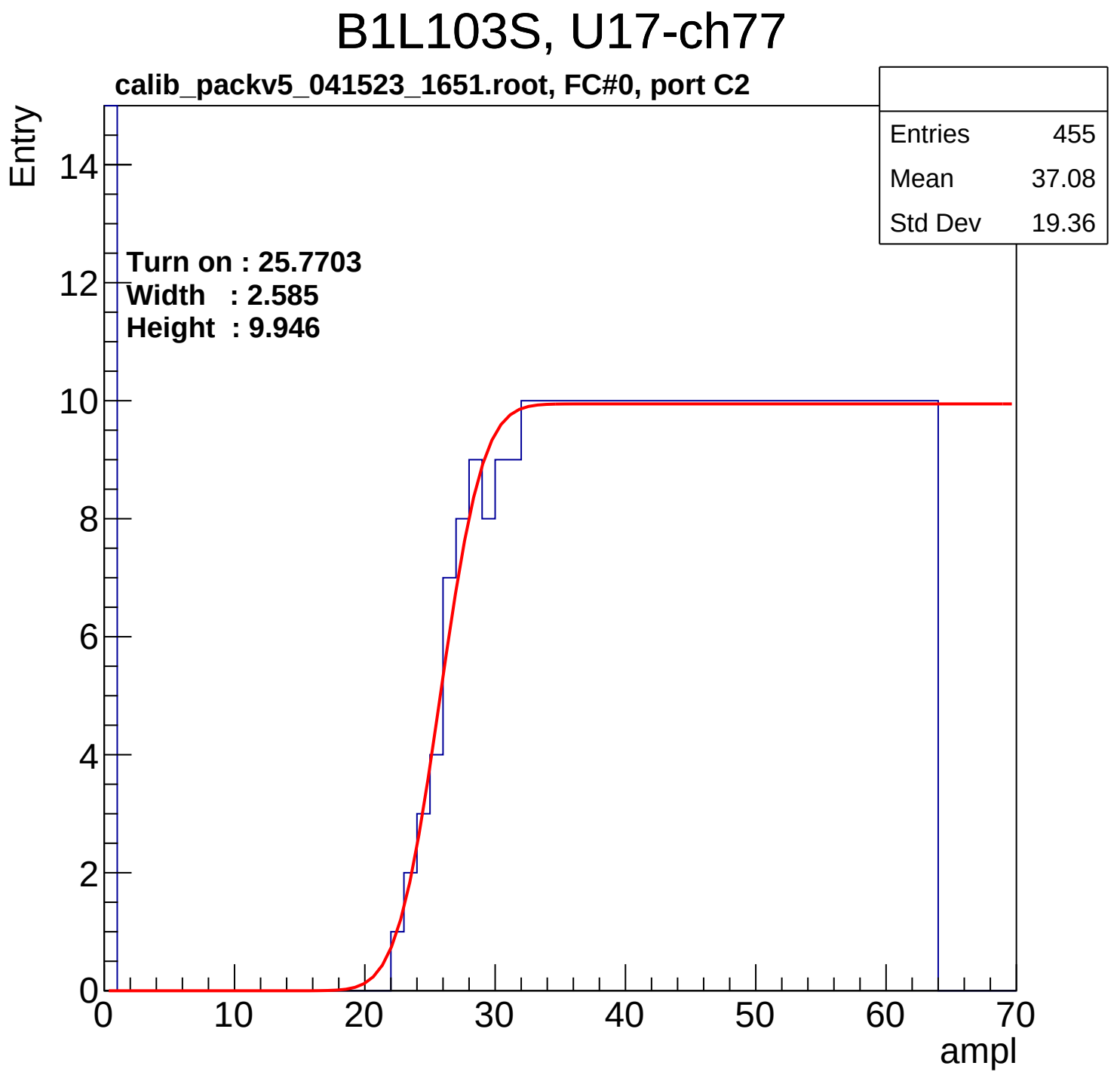
B1L103S, U17-ch77
calib_packv5_041523_1651.root, FC#0, port C2
Entries 455
Mean 37.08
Std Dev 19.36
Turn on : 25.7703
Width : 2.585
Height : 9.946
Entry
ampl
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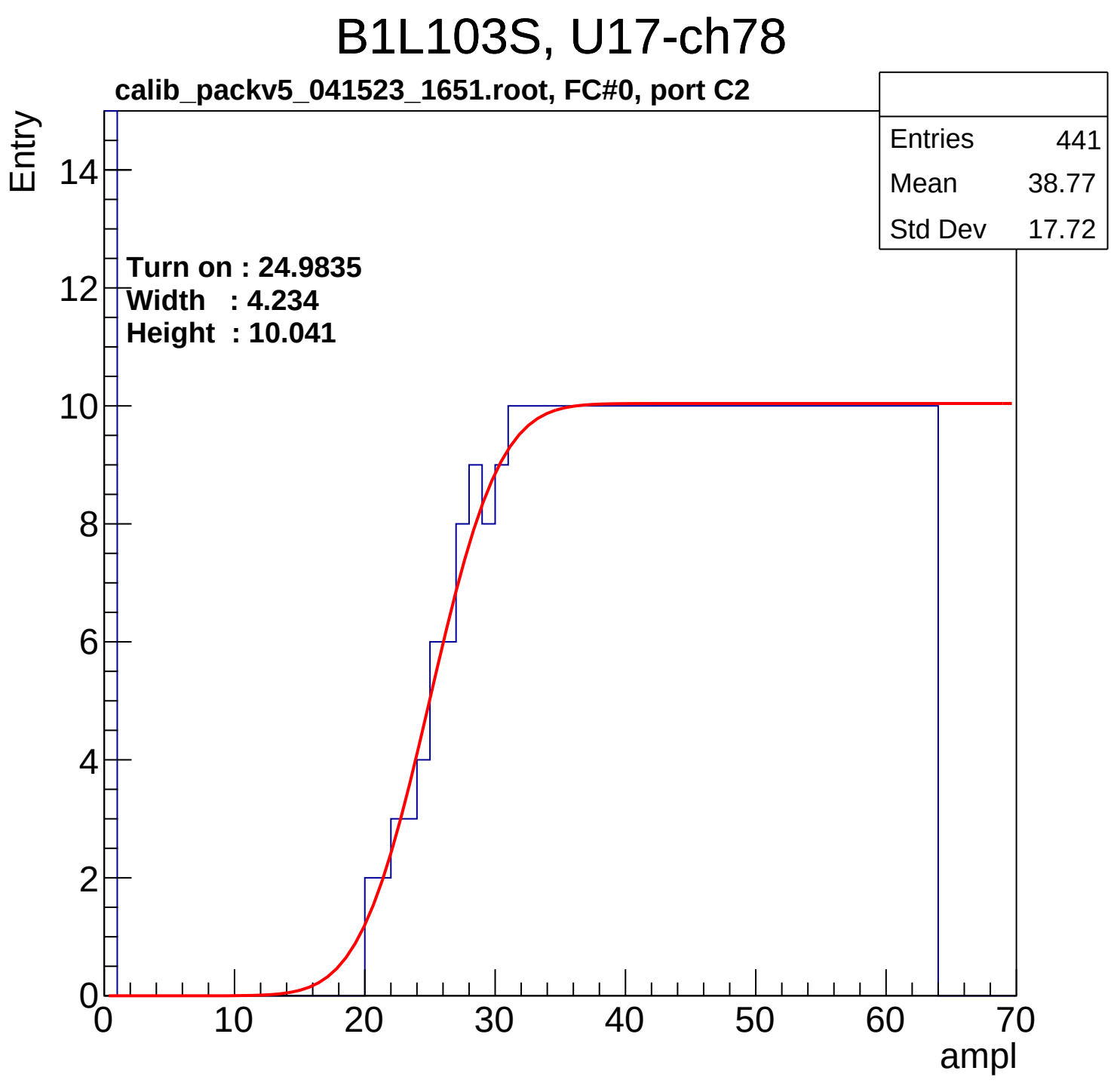
B1L103S, U17-ch78
calib_packv5_041523_1651.root, FC#0, port C2
Entries 441
Mean 38.77
Std Dev 17.72
Turn on : 24.9835
Width : 4.234
Height : 10.041
Entry
ampl
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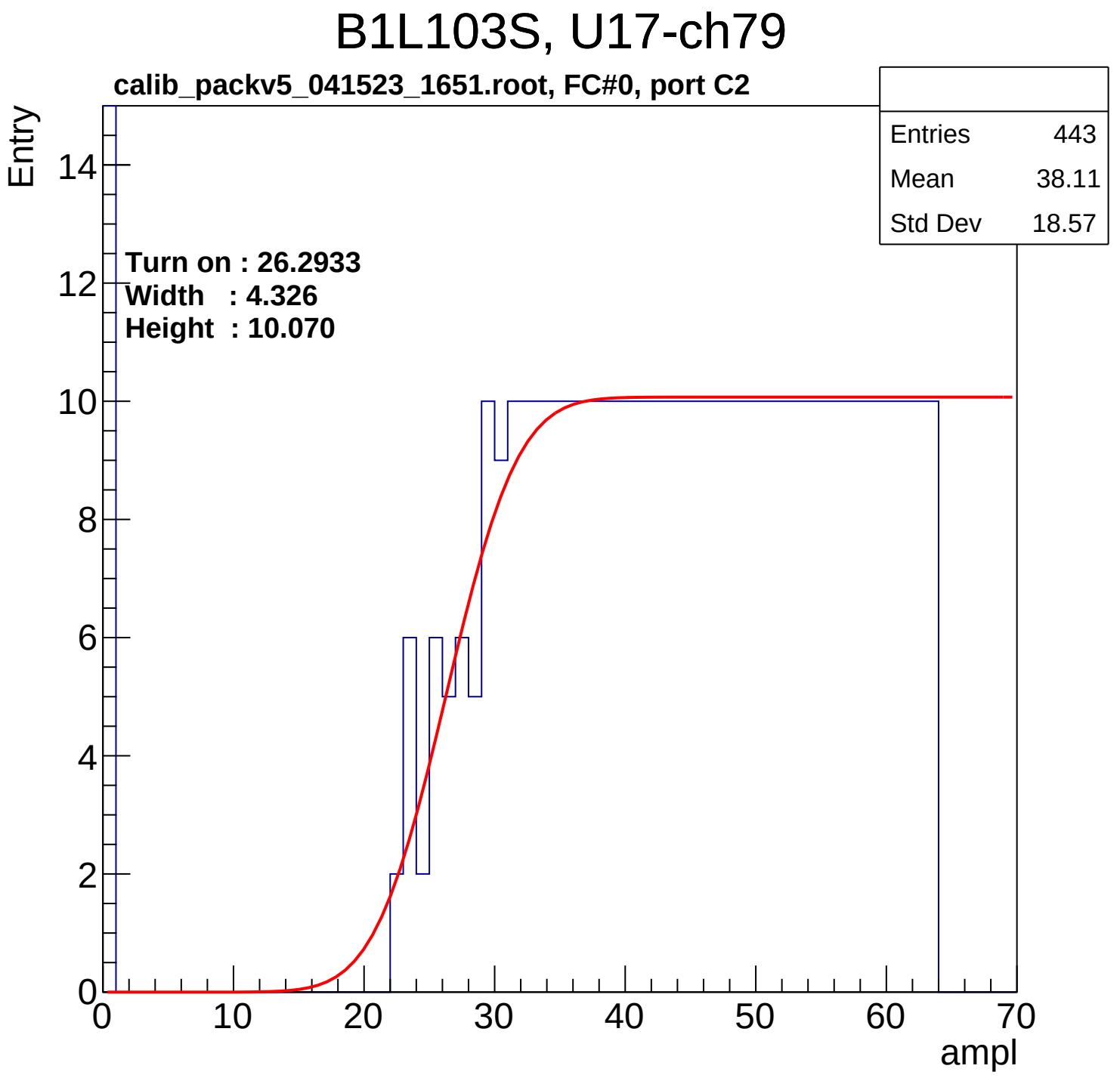
B1L103S, U17-ch79
calib_packv5_041523_1651.root, FC#0, port C2
Entries 443
Mean 38.11
Std Dev 18.57
Turn on : 26.2933
Width : 4.326
Height : 10.070
Entry
ampl
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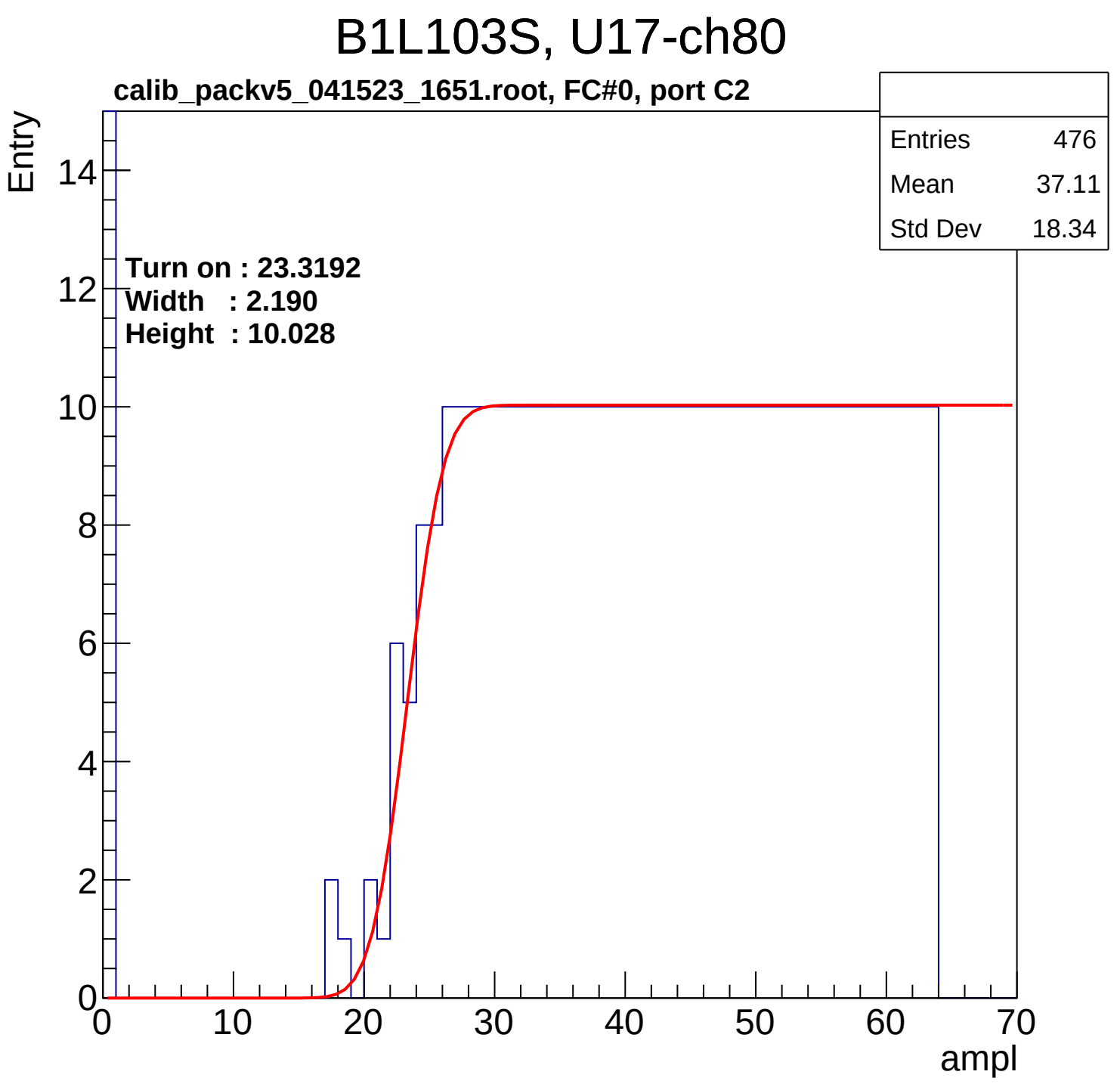
B1L103S, U17-ch80
calib_packv5_041523_1651.root, FC#0, port C2
Entries 476
Mean 37.11
Std Dev 18.34
Turn on : 23.3192
Width : 2.190
Height : 10.028
Entry
ampl
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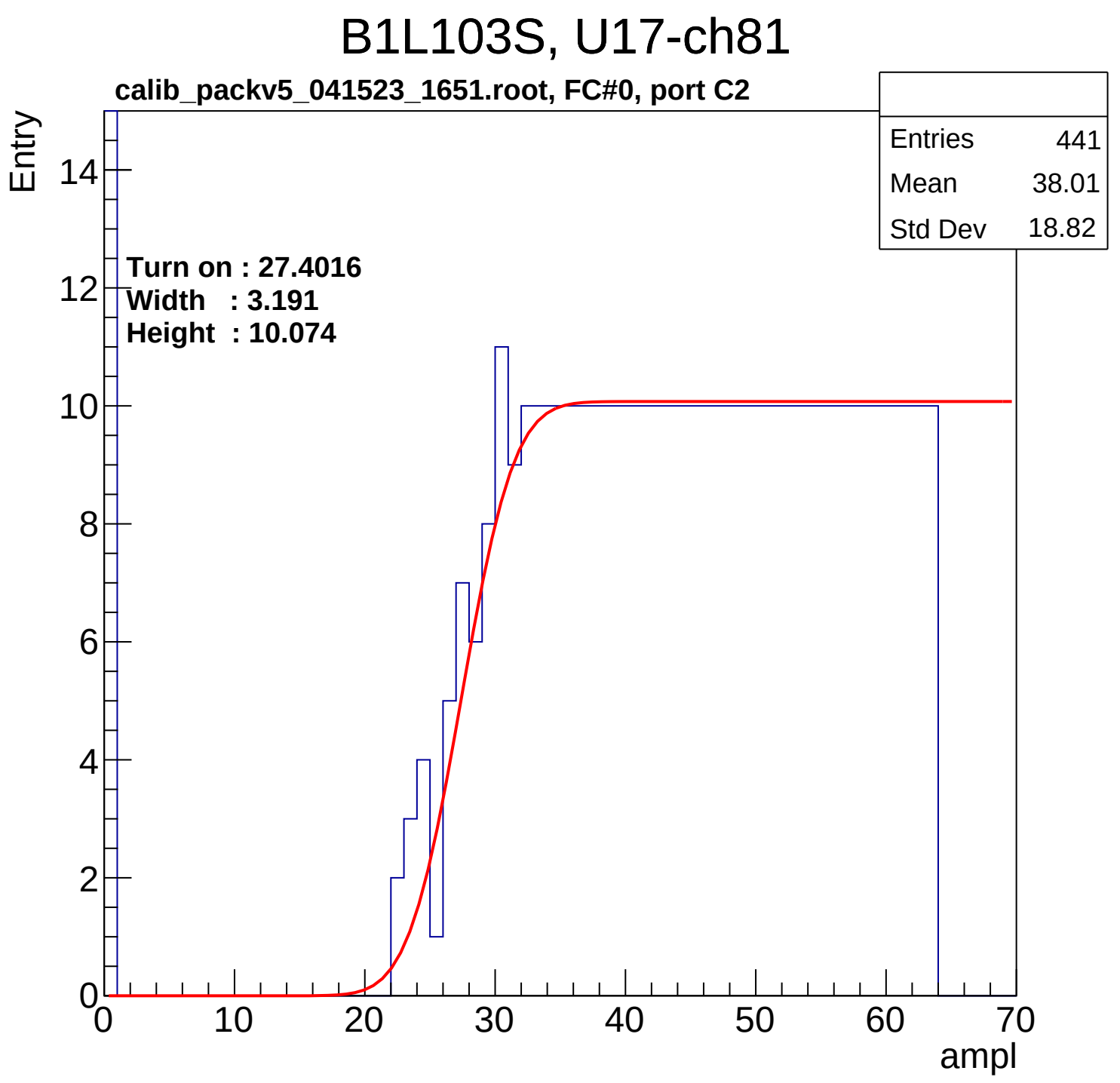
B1L103S, U17-ch81
calib_packv5_041523_1651.root, FC#0, port C2
Entries 441
Mean 38.01
Std Dev 18.82
Turn on : 27.4016
Width : 3.191
Height : 10.074
Entry
ampl
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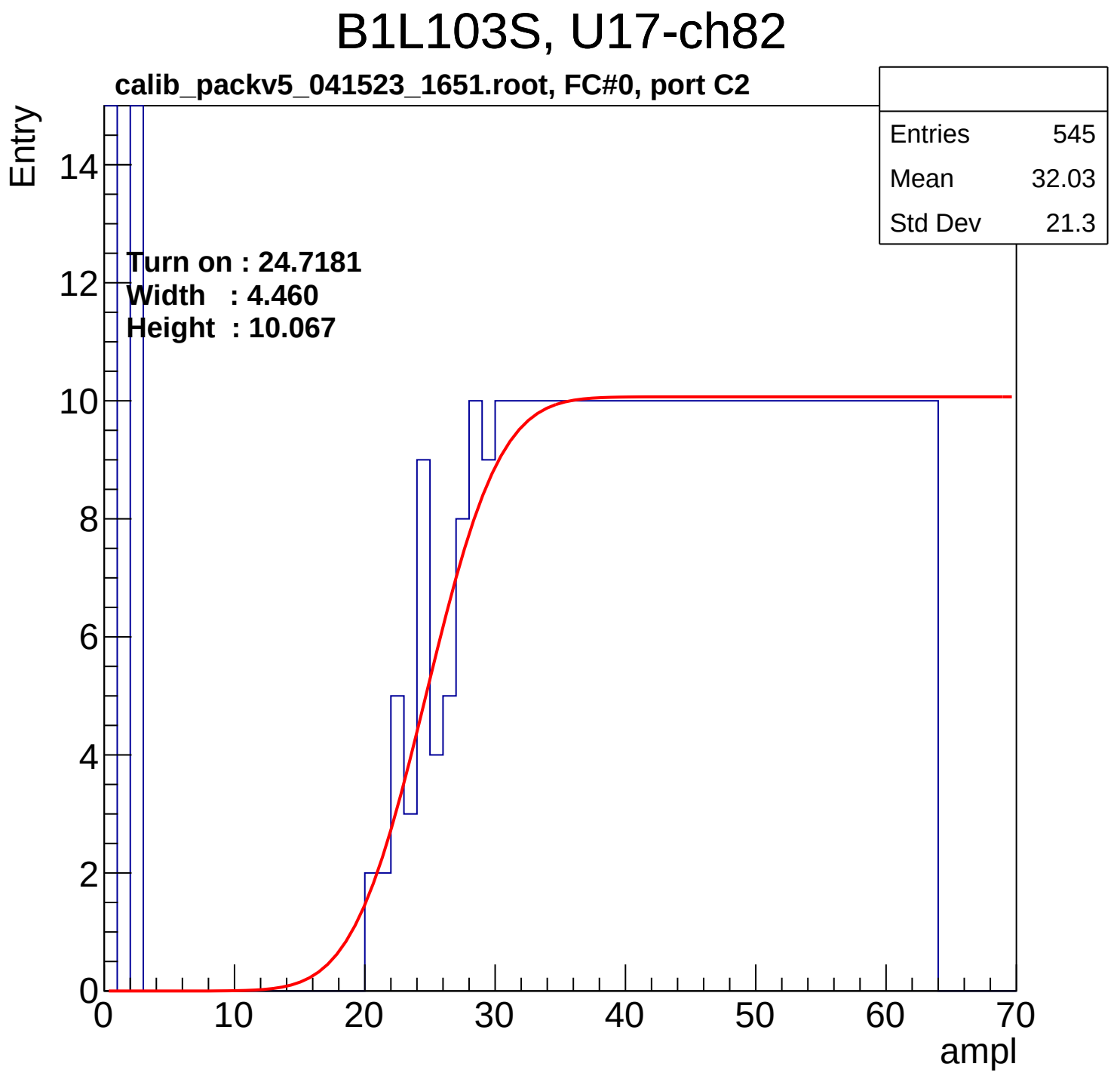
B1L103S, U17-ch82
calib_packv5_041523_1651.root, FC#0, port C2
Entries 545
Mean 32.03
Std Dev 21.3
Turn on : 24.7181
Width : 4.460
Height : 10.067
Entry
ampl
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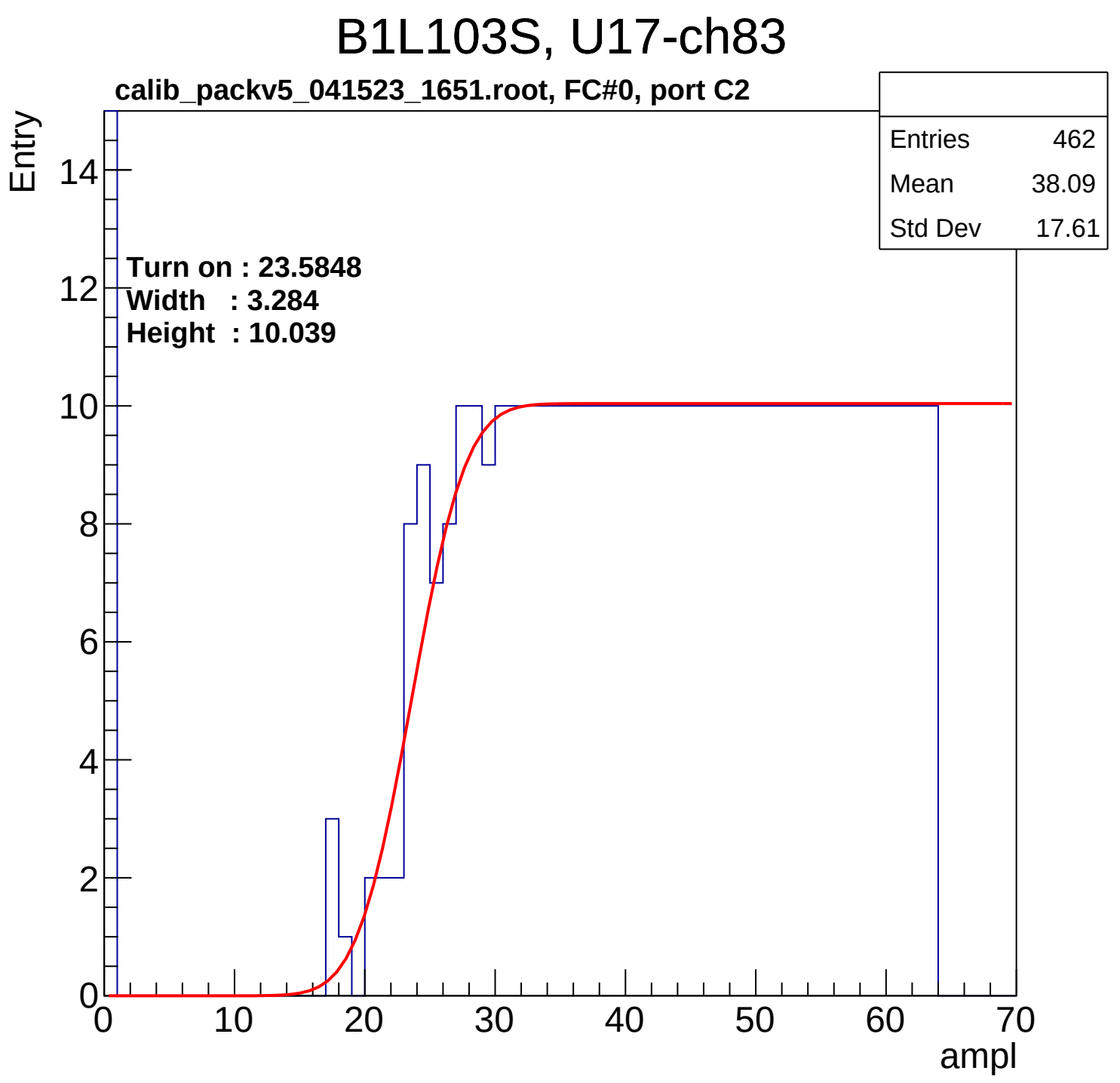
B1L103S, U17-ch83
calib_packv5_041523_1651.root, FC#0, port C2
Entries 462
Mean 38.09
Std Dev 17.61
Turn on : 23.5848
Width : 3.284
Height : 10.039
Entry
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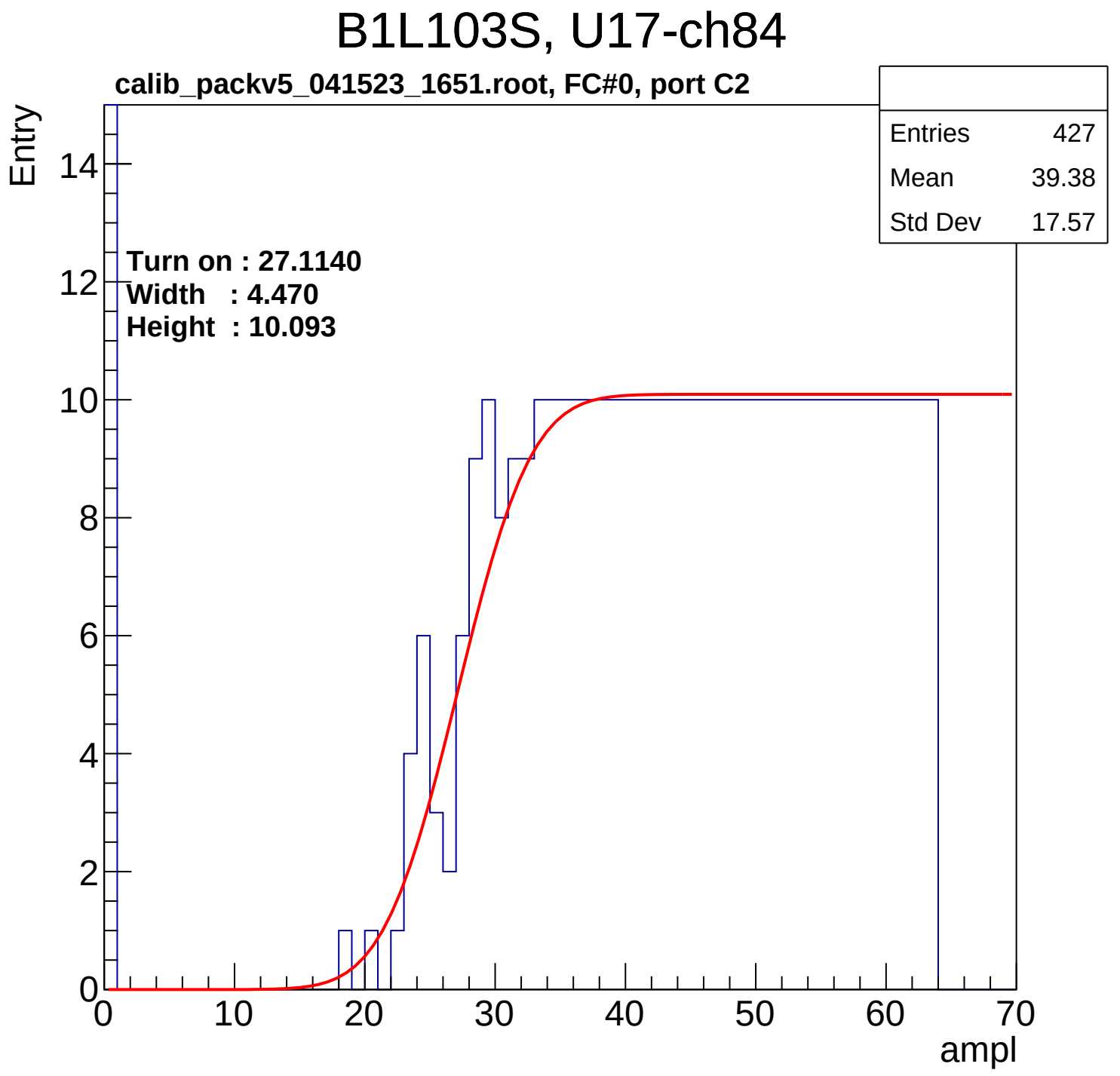
B1L103S, U17-ch84
calib_packv5_041523_1651.root, FC#0, port C2
Entries 427
Mean 39.38
Std Dev 17.57
Turn on : 27.1140
Width : 4.470
Height : 10.093
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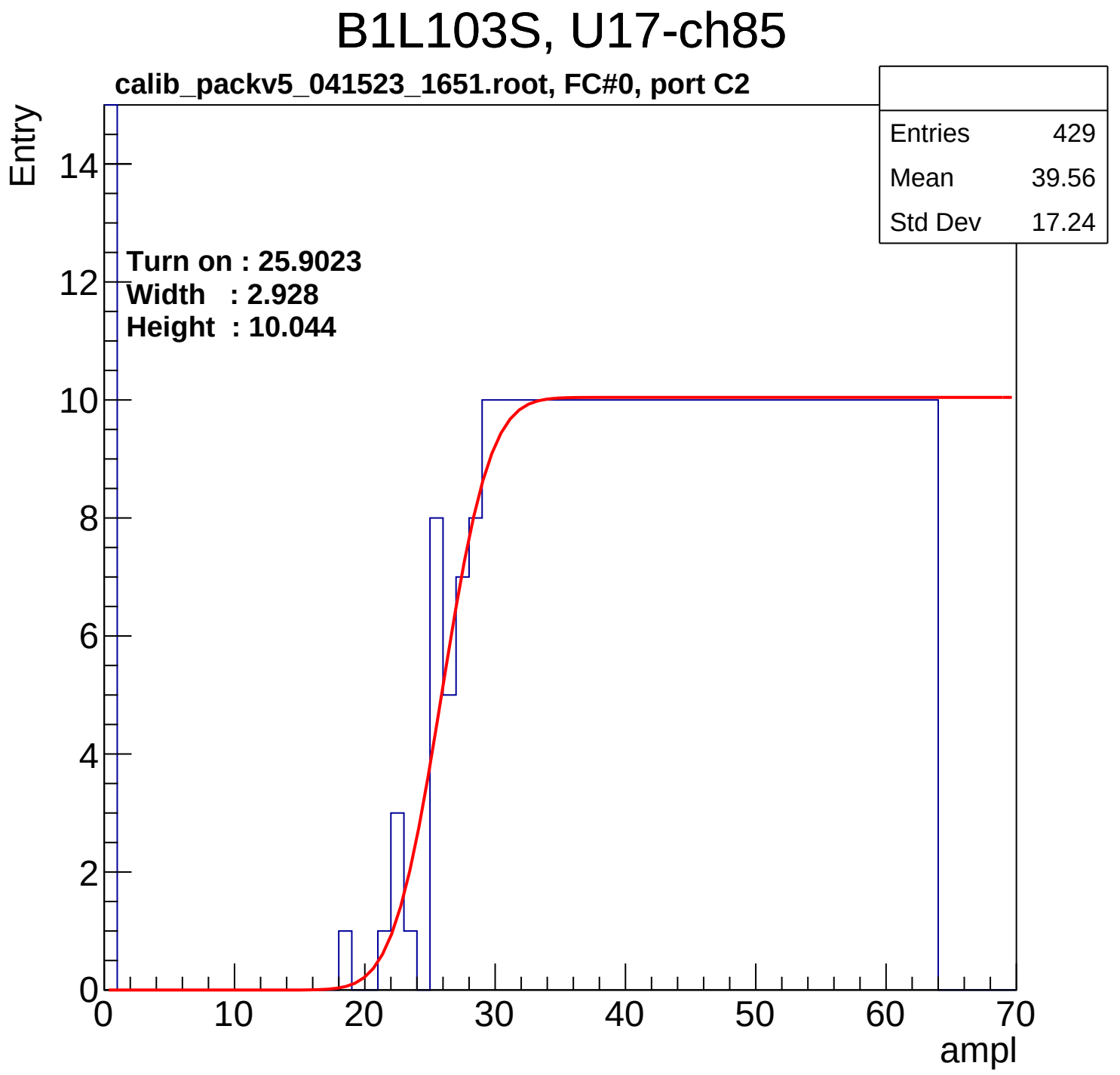
B1L103S, U17-ch85
calib_packv5_041523_1651.root, FC#0, port C2
Entries 429
Mean 39.56
Std Dev 17.24
Turn on : 25.9023
Width : 2.928
Height : 10.044
Entry
ampl
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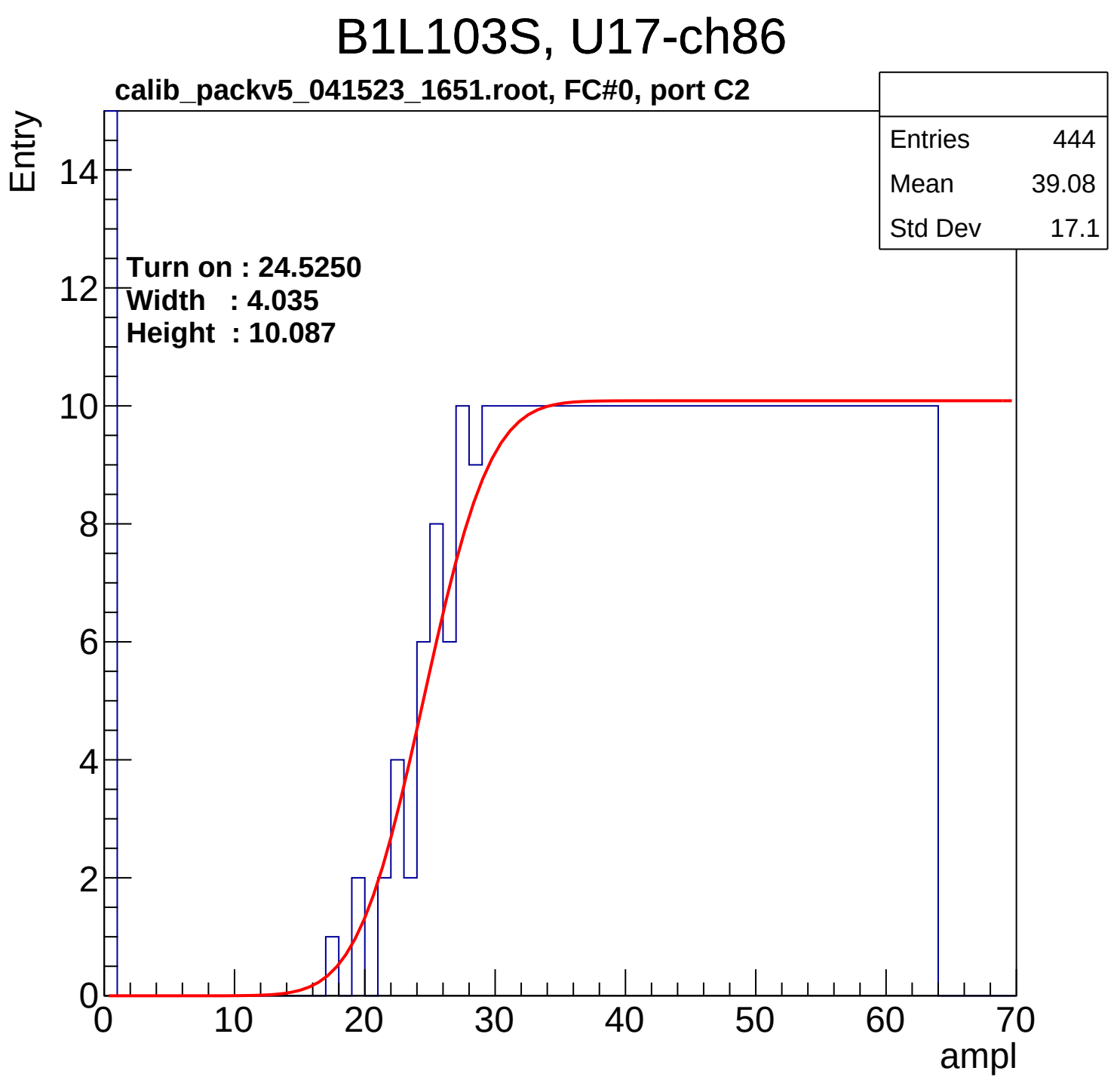
B1L103S, U17-ch86
calib_packv5_041523_1651.root, FC#0, port C2
Entries 444
Mean 39.08
Std Dev 17.1
Turn on : 24.5250
Width : 4.035
Height : 10.087
Entry
ampl
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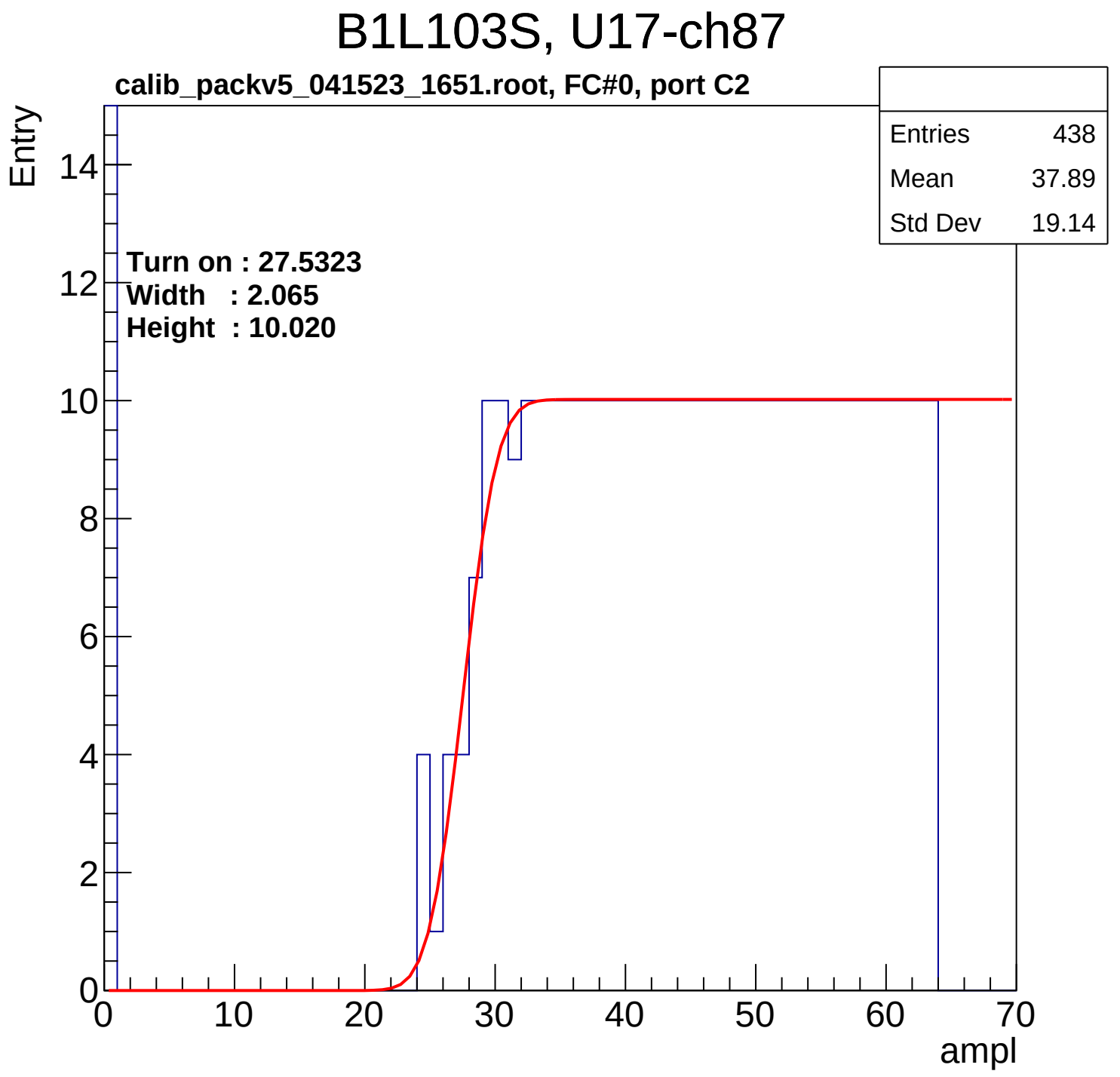
B1L103S, U17-ch87
calib_packv5_041523_1651.root, FC#0, port C2
Entries 438
Mean 37.89
Std Dev 19.14
Turn on : 27.5323
Width : 2.065
Height : 10.020
Entry
ampl
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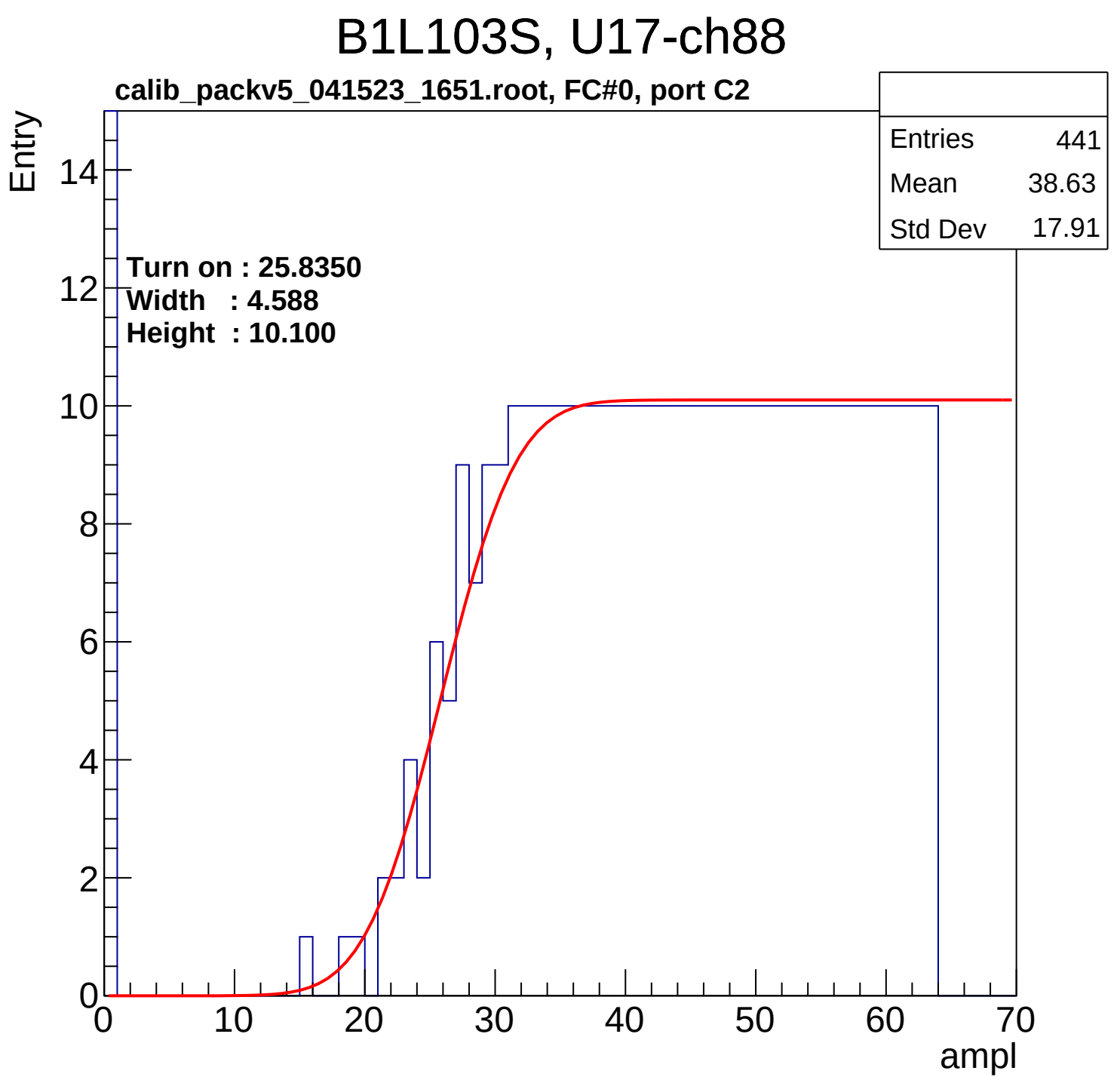
B1L103S, U17-ch88
calib_packv5_041523_1651.root, FC#0, port C2
Entries 441
Mean 38.63
Std Dev 17.91
Turn on : 25.8350
Width : 4.588
Height : 10.100
Entry
ampl
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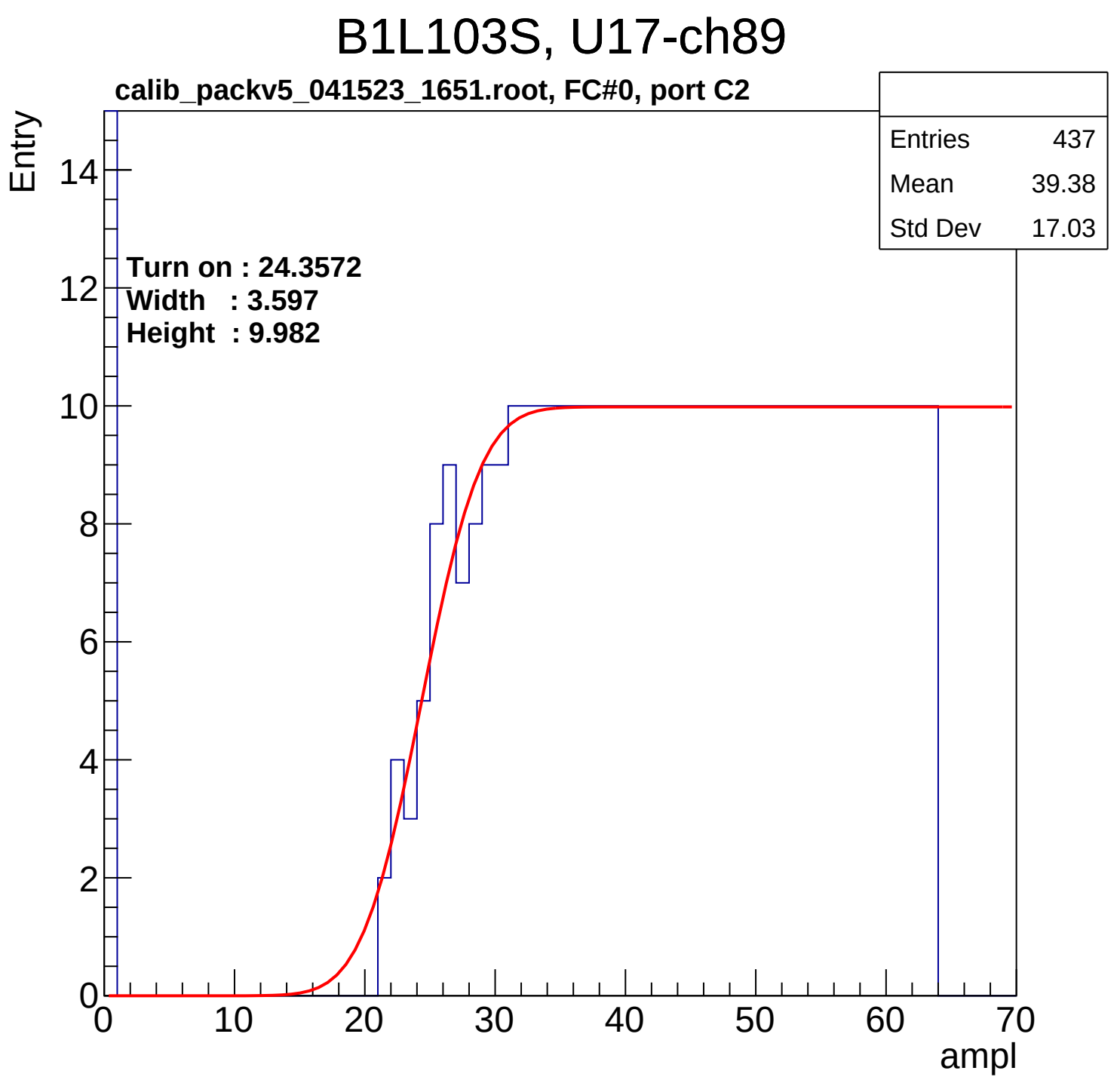
B1L103S, U17-ch89
calib_packv5_041523_1651.root, FC#0, port C2
Entries 437
Mean 39.38
Std Dev 17.03
Turn on : 24.3572
Width : 3.597
Height : 9.982
Entry
ampl
0
2
4
6
8
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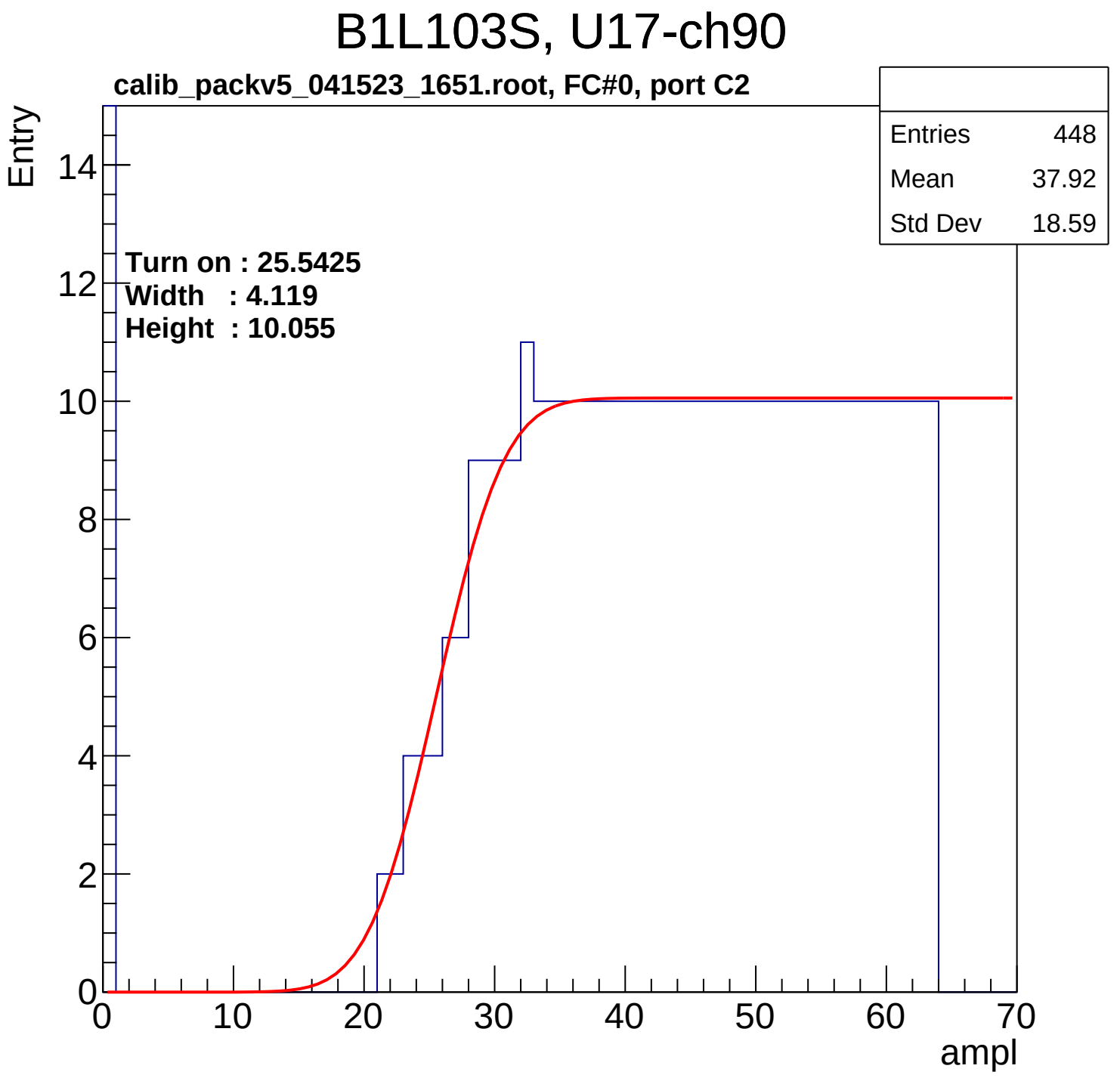
B1L103S, U17-ch90
calib_packv5_041523_1651.root, FC#0, port C2
Entries 448
Mean 37.92
Std Dev 18.59
Turn on : 25.5425
Width : 4.119
Height : 10.055
Entry
ampl
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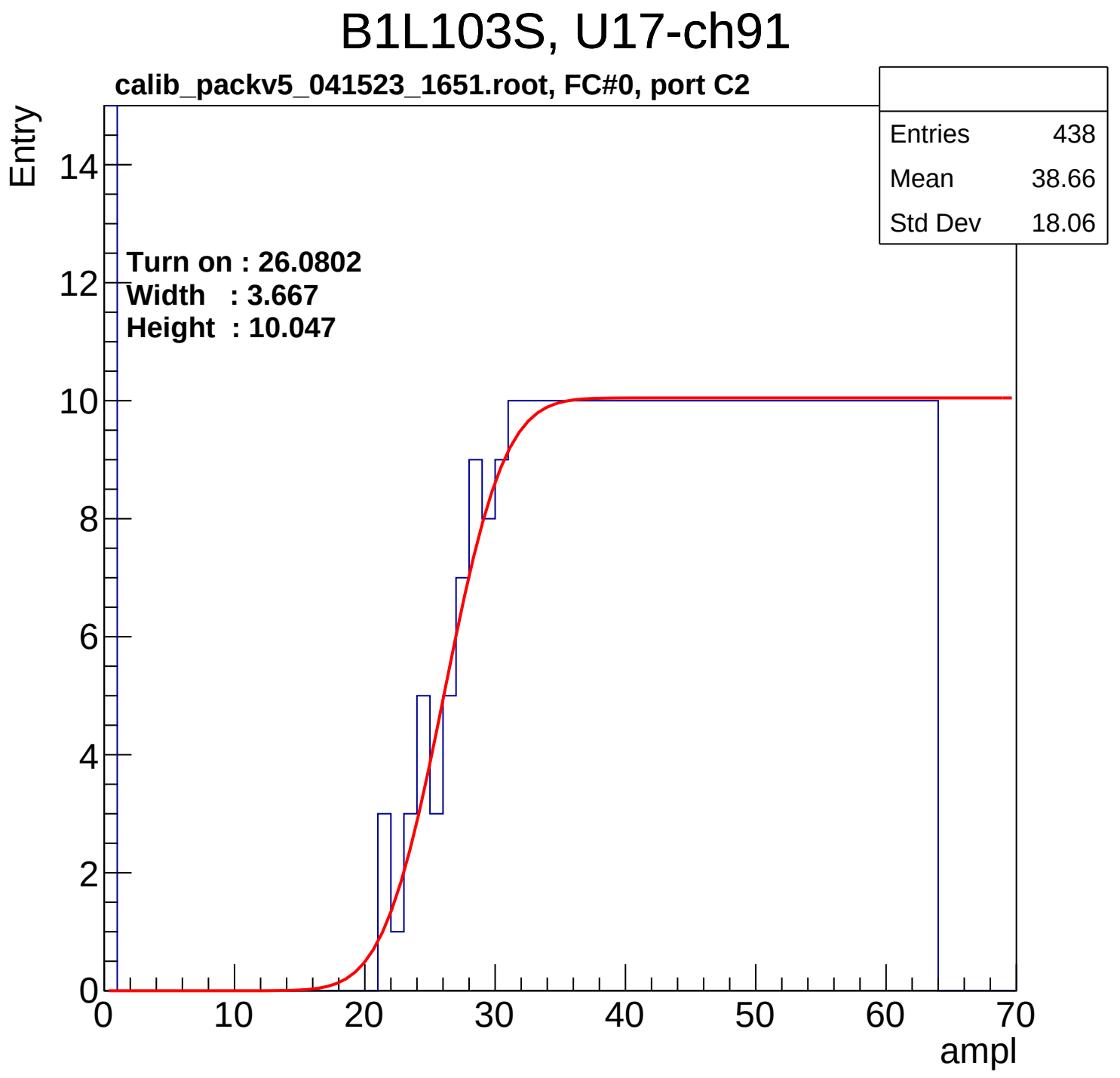
B1L103S, U17-ch91
calib_packv5_041523_1651.root, FC#0, port C2
Entries 438
Mean 38.66
Std Dev 18.06
Turn on : 26.0802
Width : 3.667
Height : 10.047
Entry
ampl
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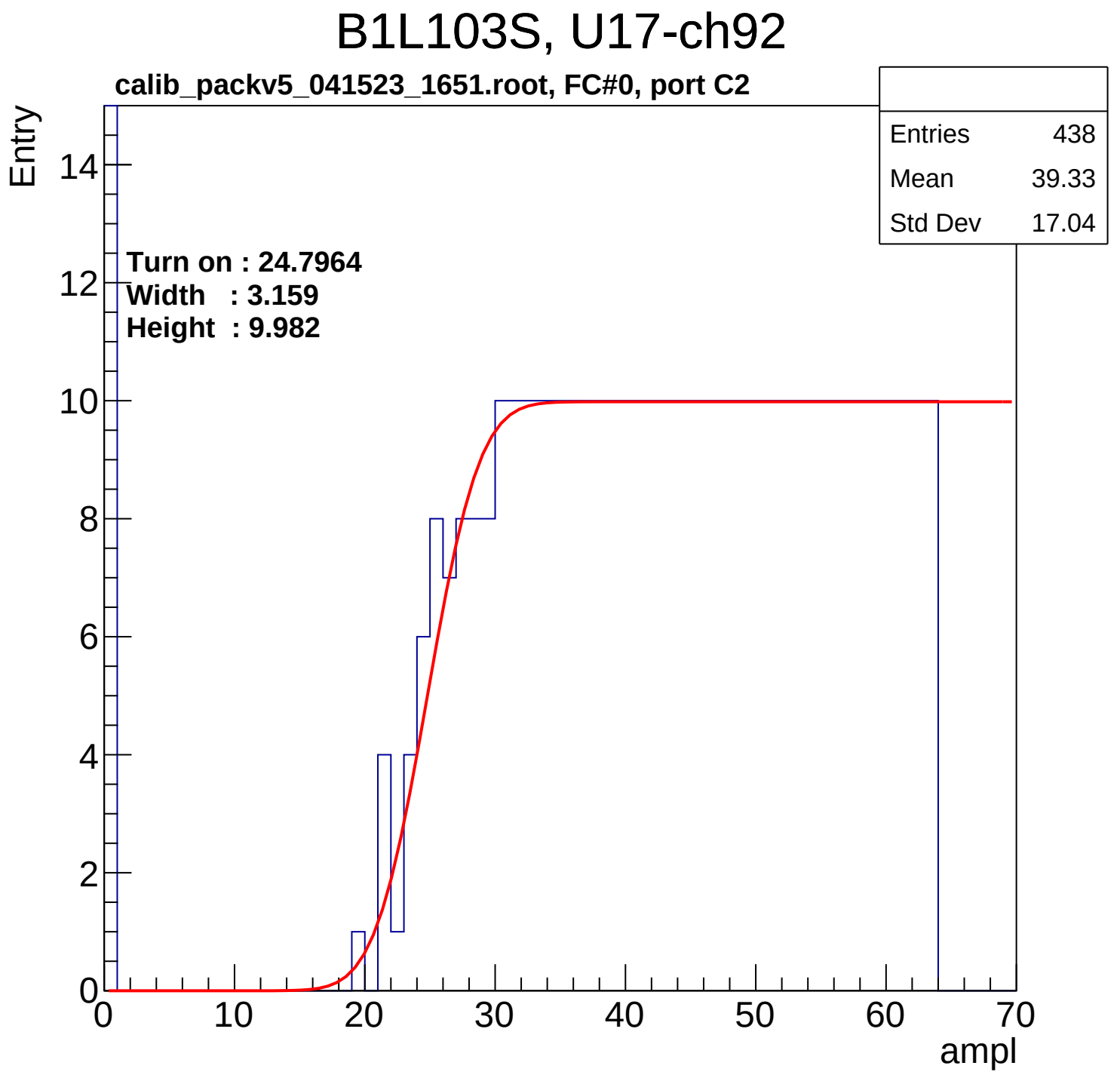
B1L103S, U17-ch92
calib_packv5_041523_1651.root, FC#0, port C2
Entries 438
Mean 39.33
Std Dev 17.04
Turn on : 24.7964
Width : 3.159
Height : 9.982
Entry
ampl
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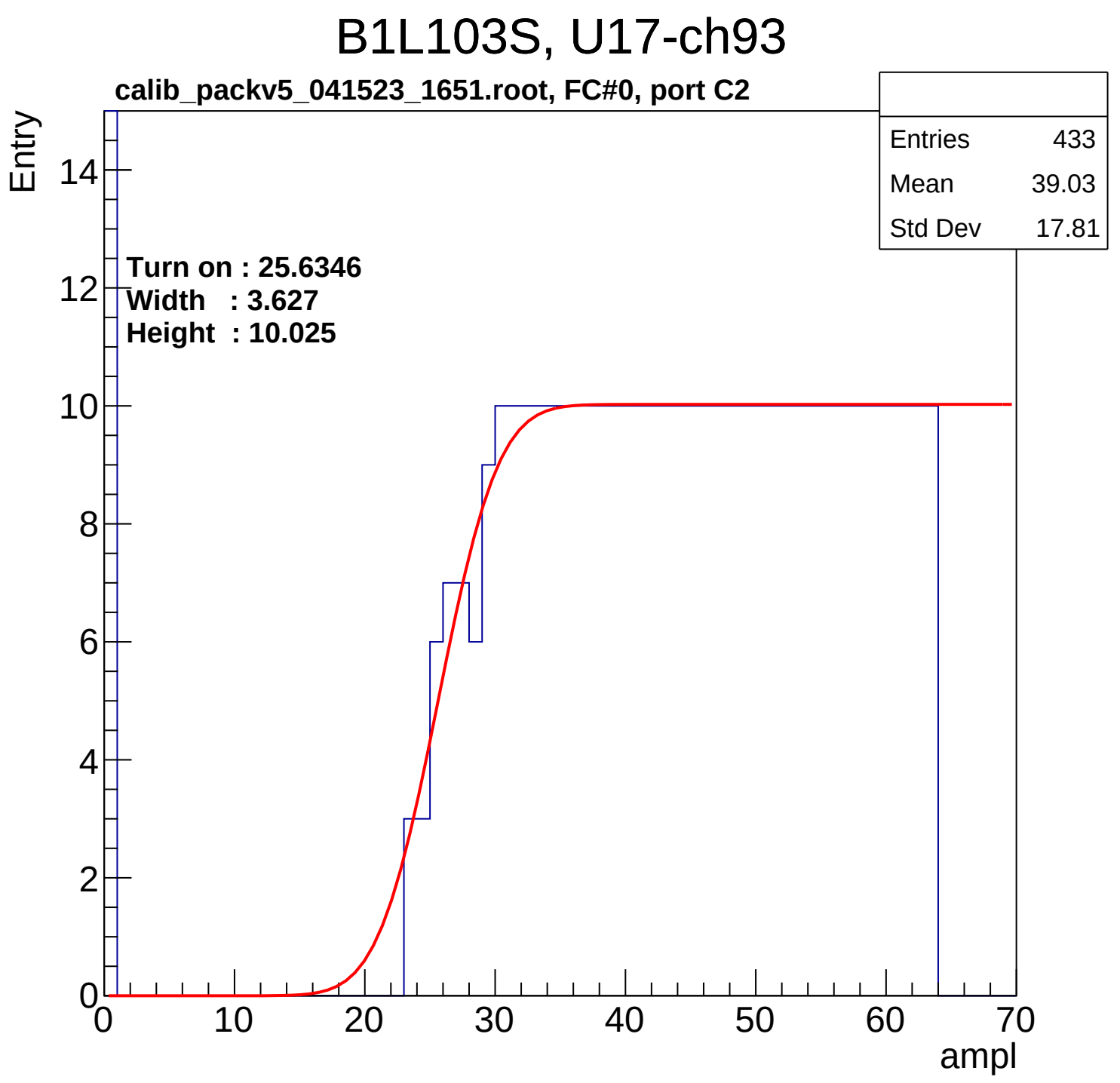
B1L103S, U17-ch93
calib_packv5_041523_1651.root, FC#0, port C2
Entries 433
Mean 39.03
Std Dev 17.81
Turn on : 25.6346
Width : 3.627
Height : 10.025
Entry
ampl
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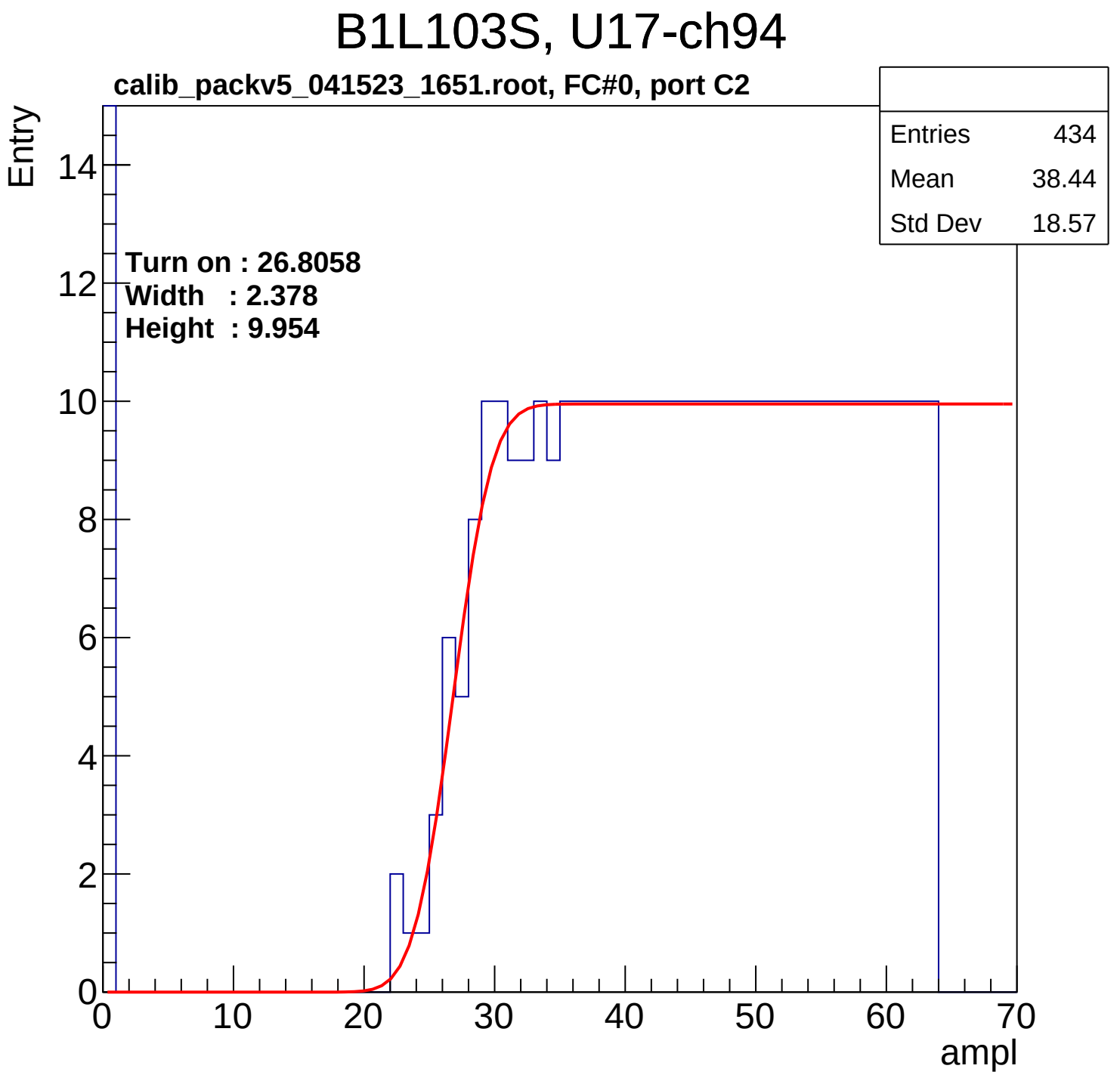
B1L103S, U17-ch94
calib_packv5_041523_1651.root, FC#0, port C2
Entries 434
Mean 38.44
Std Dev 18.57
Turn on : 26.8058
Width : 2.378
Height : 9.954
Entry
ampl
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2
4
6
8
10
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0
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60
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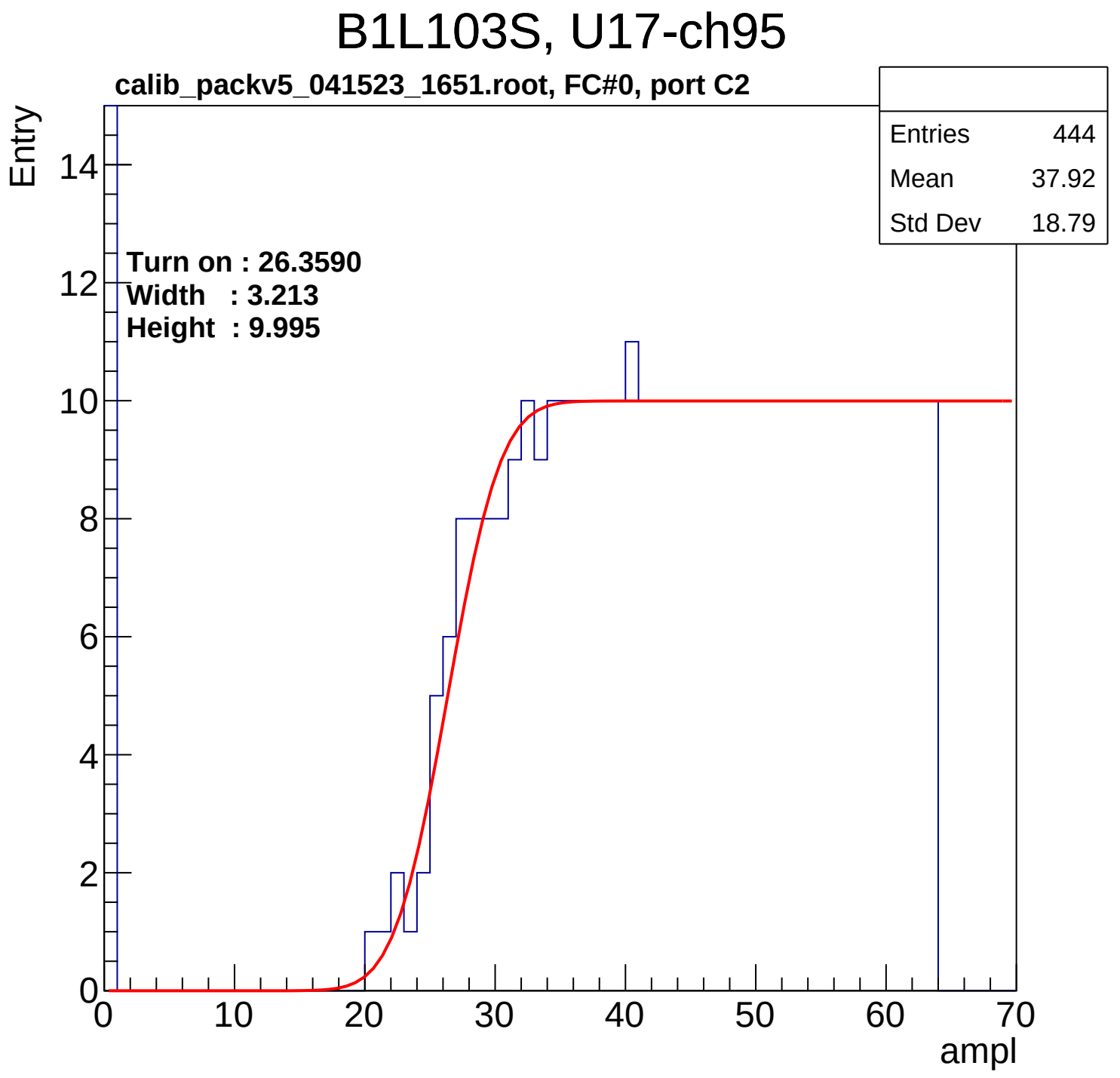
B1L103S, U17-ch95
calib_packv5_041523_1651.root, FC#0, port C2
Entries 444
Mean 37.92
Std Dev 18.79
Turn on : 26.3590
Width : 3.213
Height : 9.995
Entry
ampl
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6
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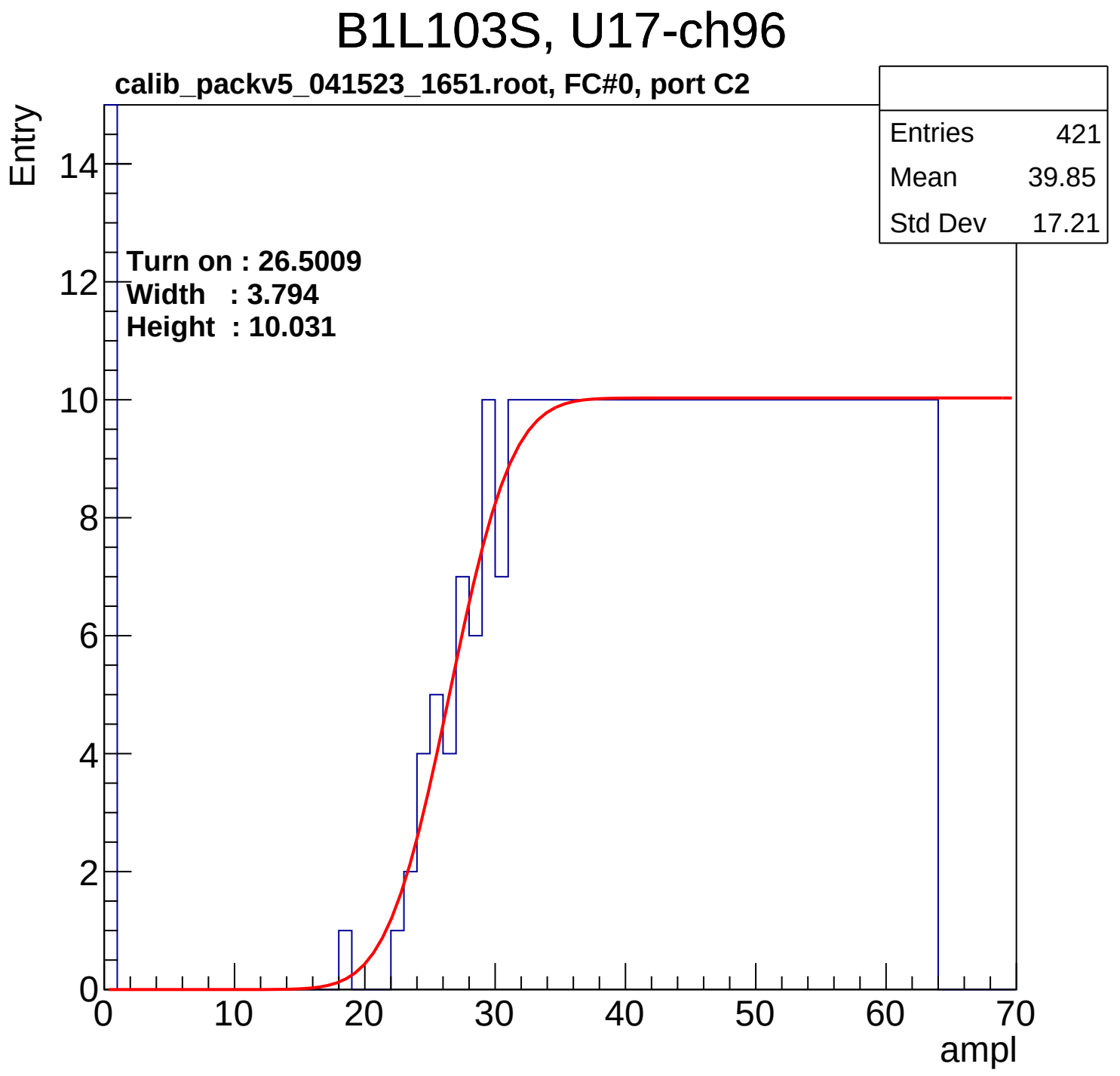
B1L103S, U17-ch96
calib_packv5_041523_1651.root, FC#0, port C2
Entries 421
Mean 39.85
Std Dev 17.21
Turn on : 26.5009
Width : 3.794
Height : 10.031
Entry
ampl
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2
4
6
8
10
12
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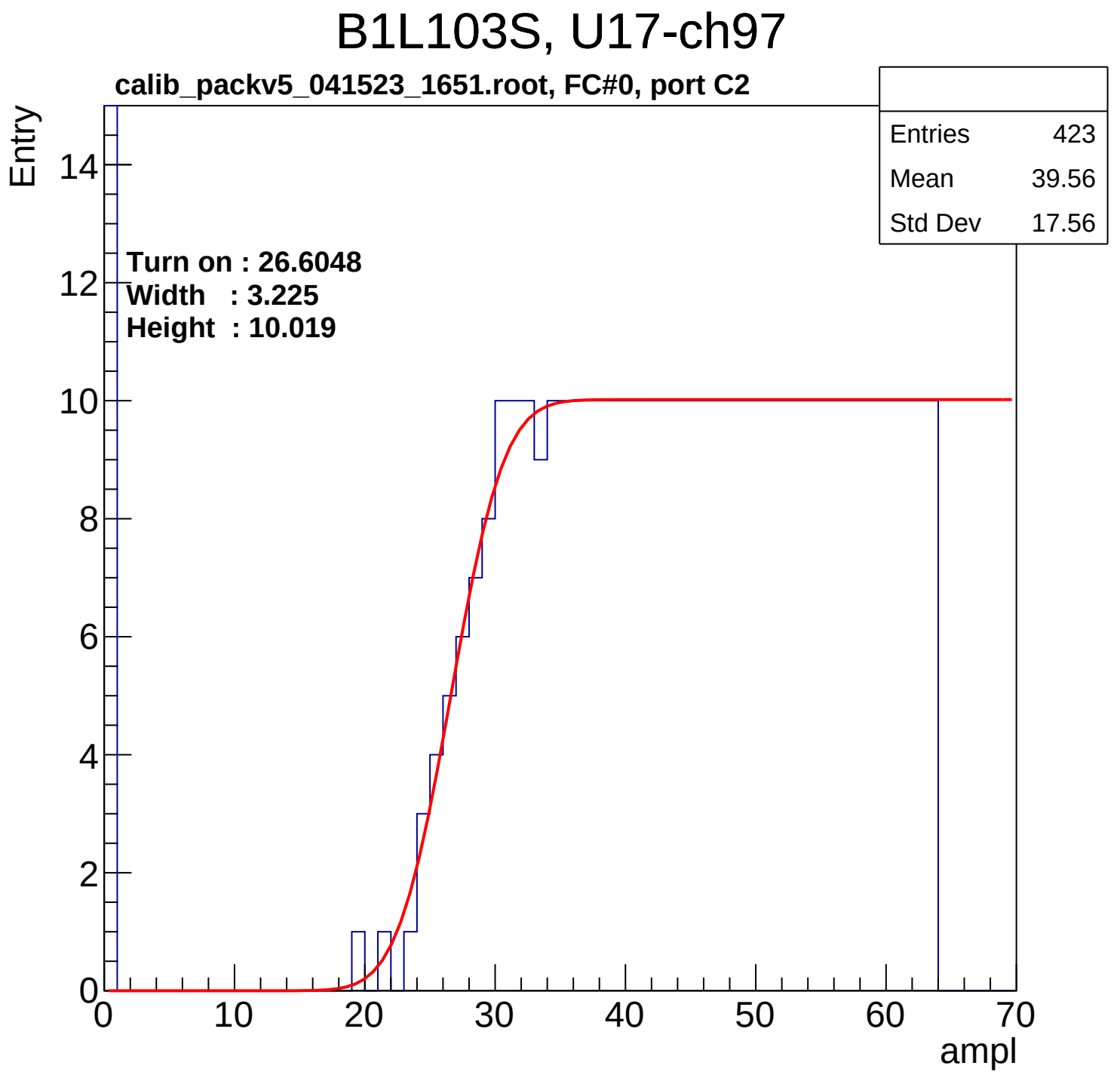
B1L103S, U17-ch97
calib_packv5_041523_1651.root, FC#0, port C2
Entries 423
Mean 39.56
Std Dev 17.56
Turn on : 26.6048
Width : 3.225
Height : 10.019
Entry
ampl
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6
8
10
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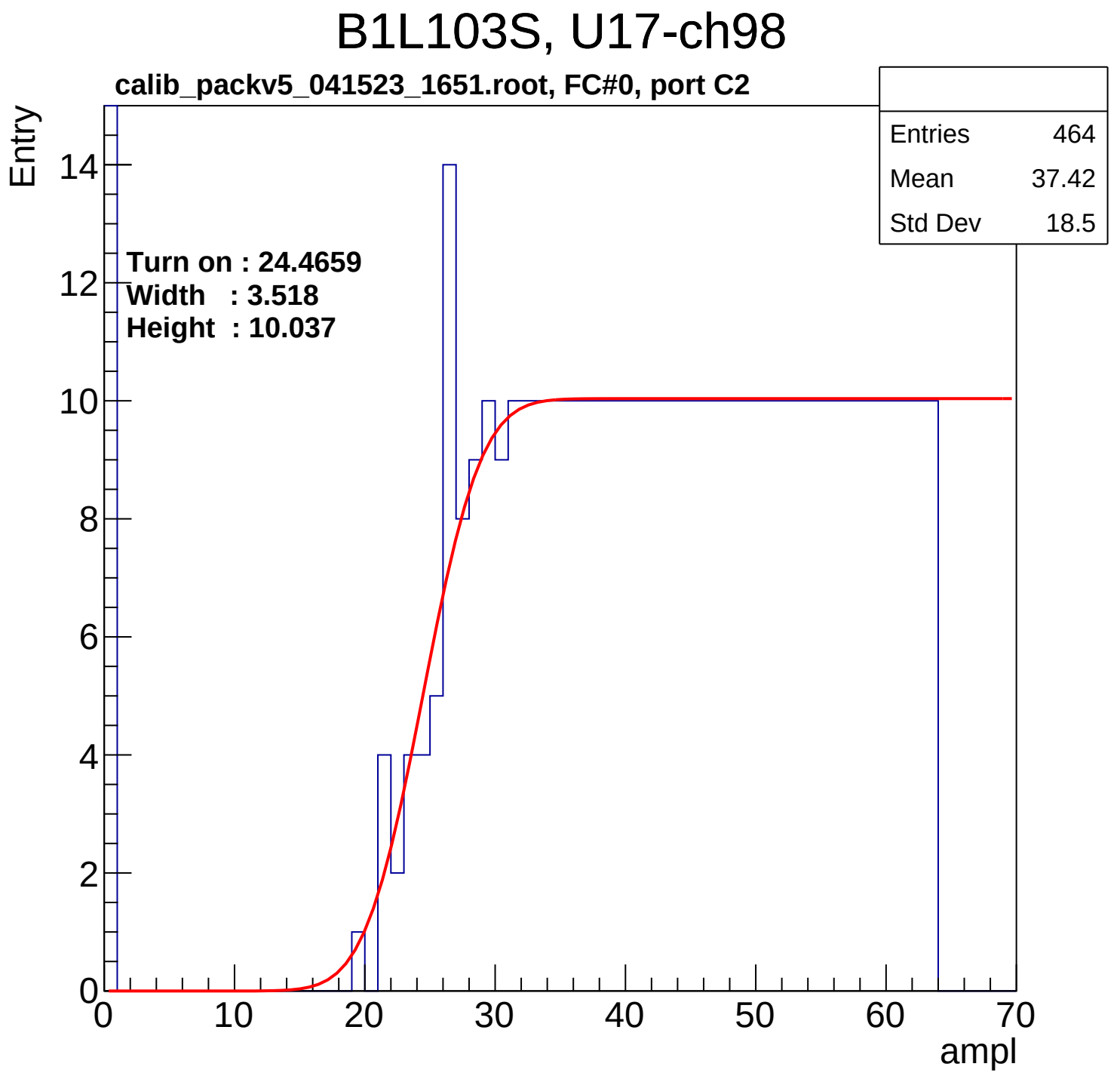
B1L103S, U17-ch98
calib_packv5_041523_1651.root, FC#0, port C2
Entries 464
Mean 37.42
Std Dev 18.5
Turn on : 24.4659
Width : 3.518
Height : 10.037
Entry
ampl
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8
10
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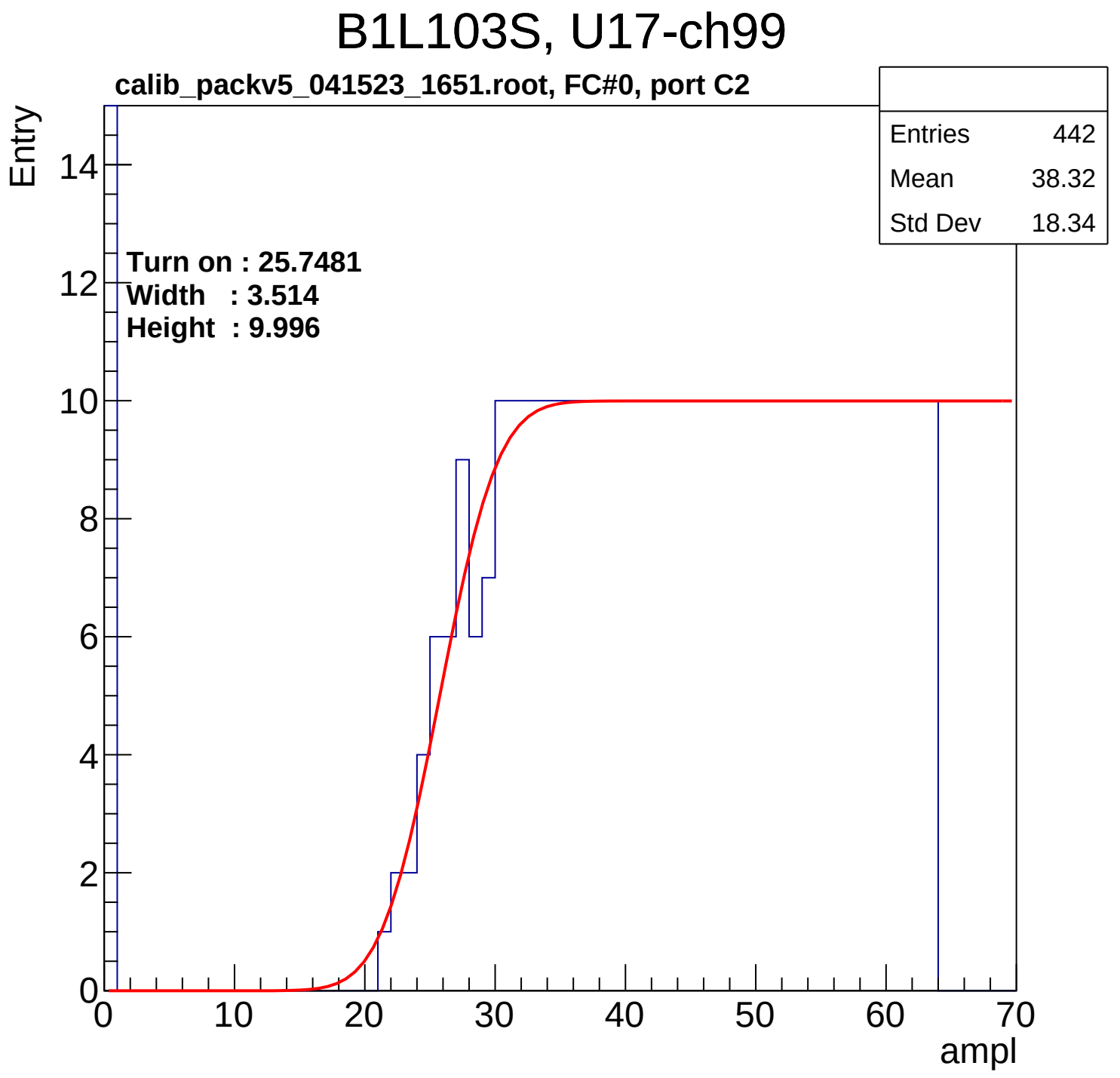
B1L103S, U17-ch99
calib_packv5_041523_1651.root, FC#0, port C2
Entries 442
Mean 38.32
Std Dev 18.34
Turn on : 25.7481
Width : 3.514
Height : 9.996
Entry
ampl
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6
8
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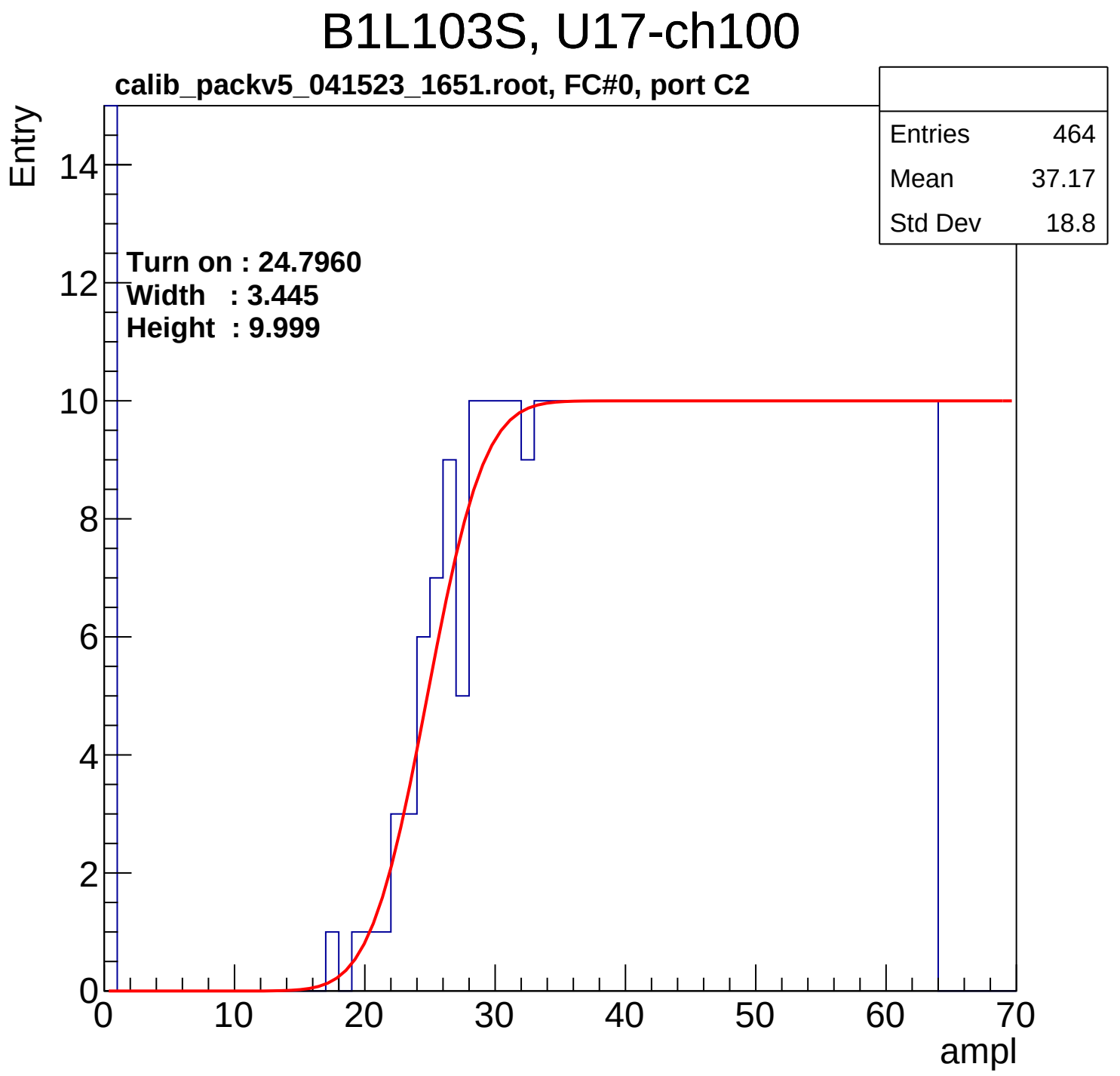
B1L103S, U17-ch100
calib_packv5_041523_1651.root, FC#0, port C2
Entries 464
Mean 37.17
Std Dev 18.8
Turn on : 24.7960
Width : 3.445
Height : 9.999
Entry
ampl
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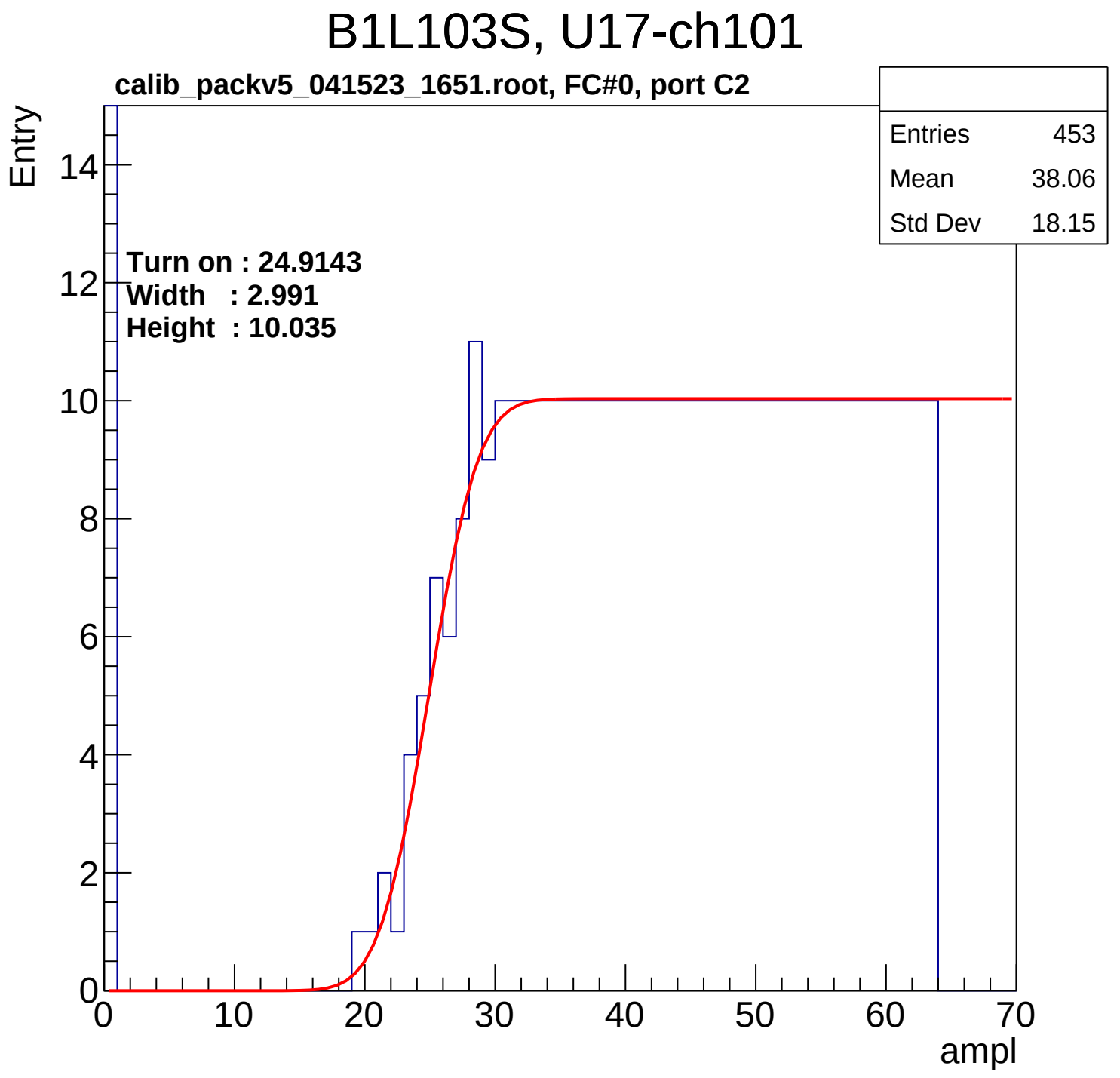
B1L103S, U17-ch101
calib_packv5_041523_1651.root, FC#0, port C2
Entries 453
Mean 38.06
Std Dev 18.15
Turn on : 24.9143
Width : 2.991
Height : 10.035
Entry
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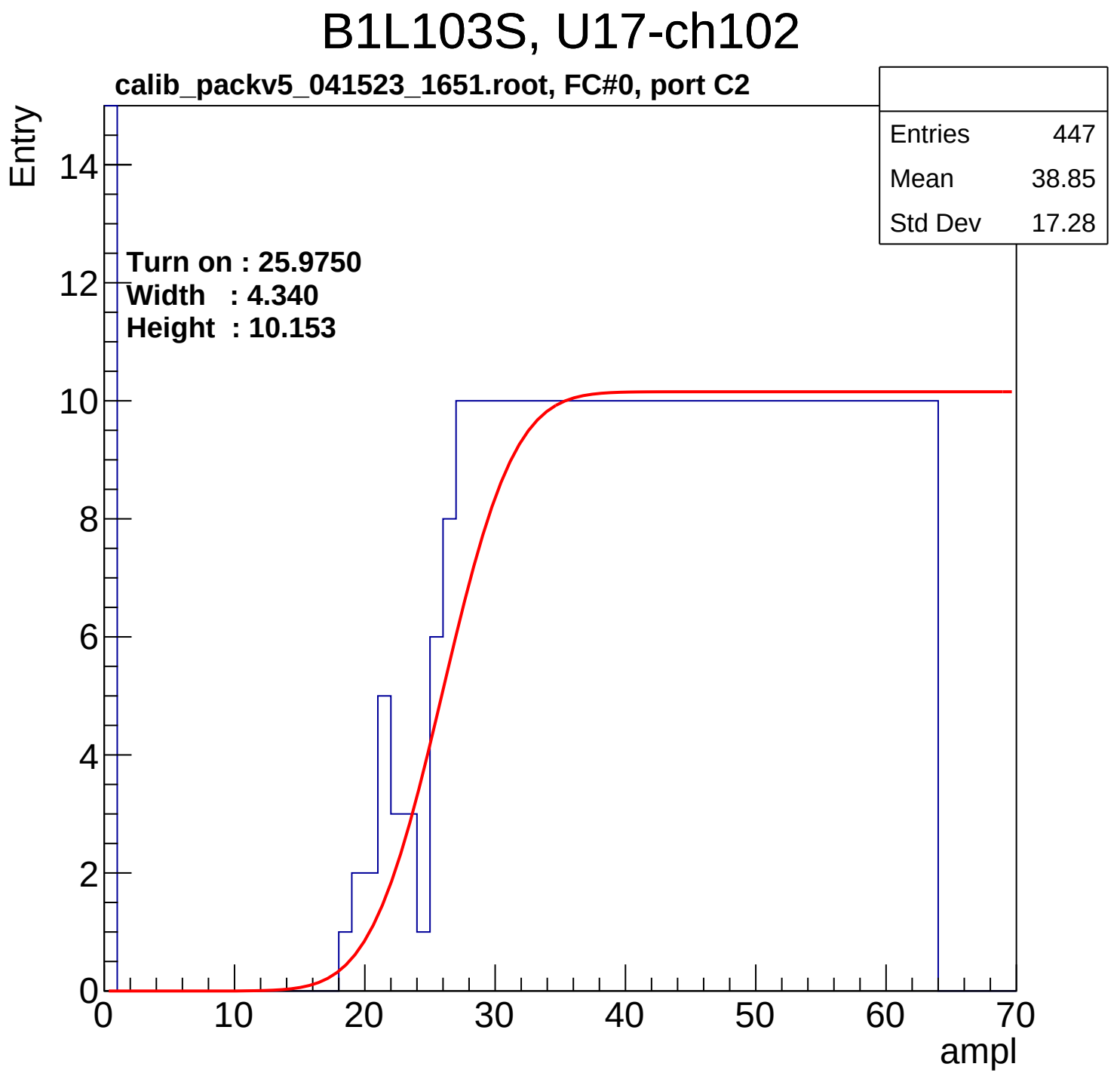
B1L103S, U17-ch102
calib_packv5_041523_1651.root, FC#0, port C2
Entries 447
Mean 38.85
Std Dev 17.28
Turn on : 25.9750
Width : 4.340
Height : 10.153
Entry
ampl
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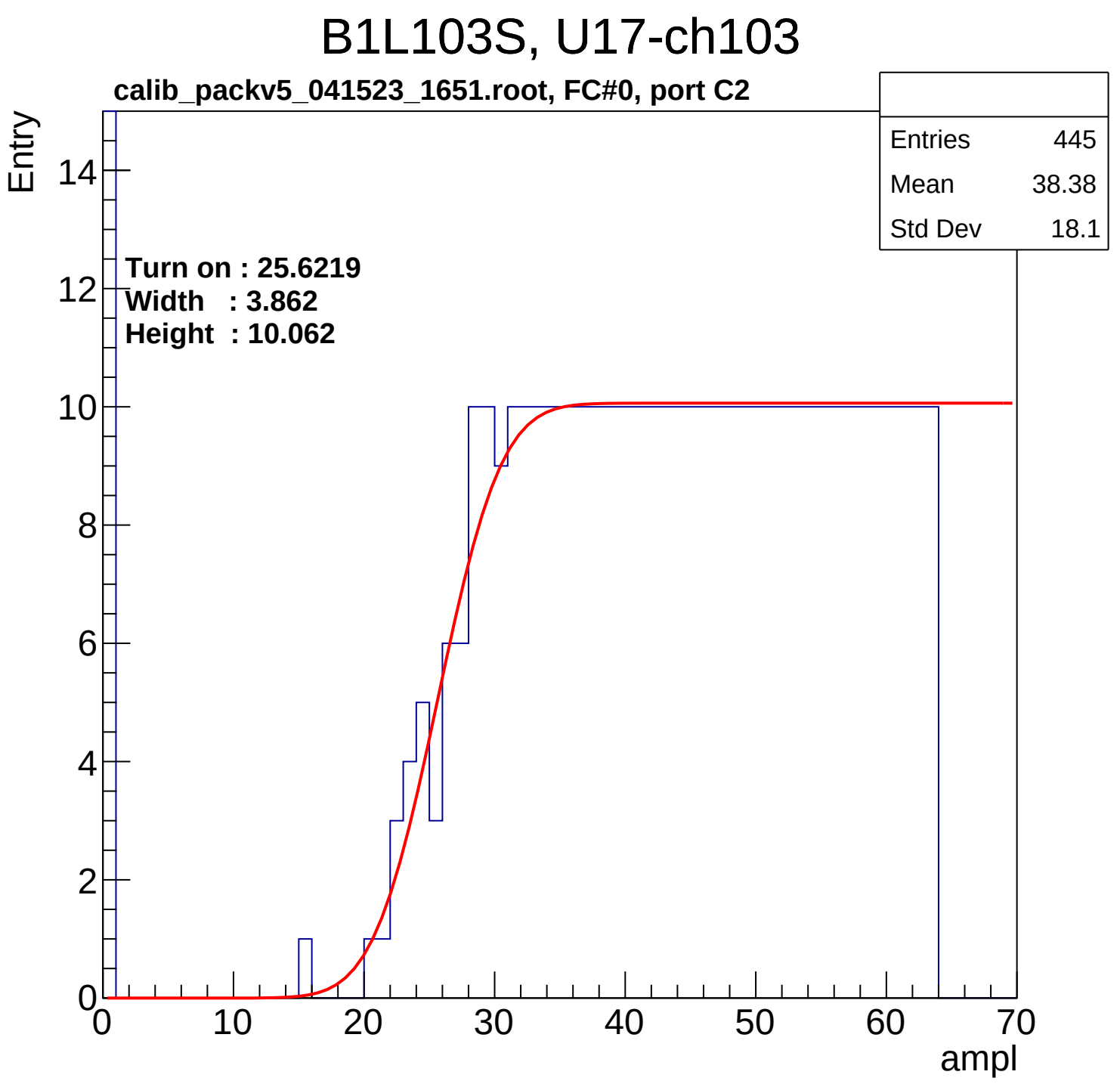
B1L103S, U17-ch103
calib_packv5_041523_1651.root, FC#0, port C2
Entries 445
Mean 38.38
Std Dev 18.1
Turn on : 25.6219
Width : 3.862
Height : 10.062
Entry
ampl
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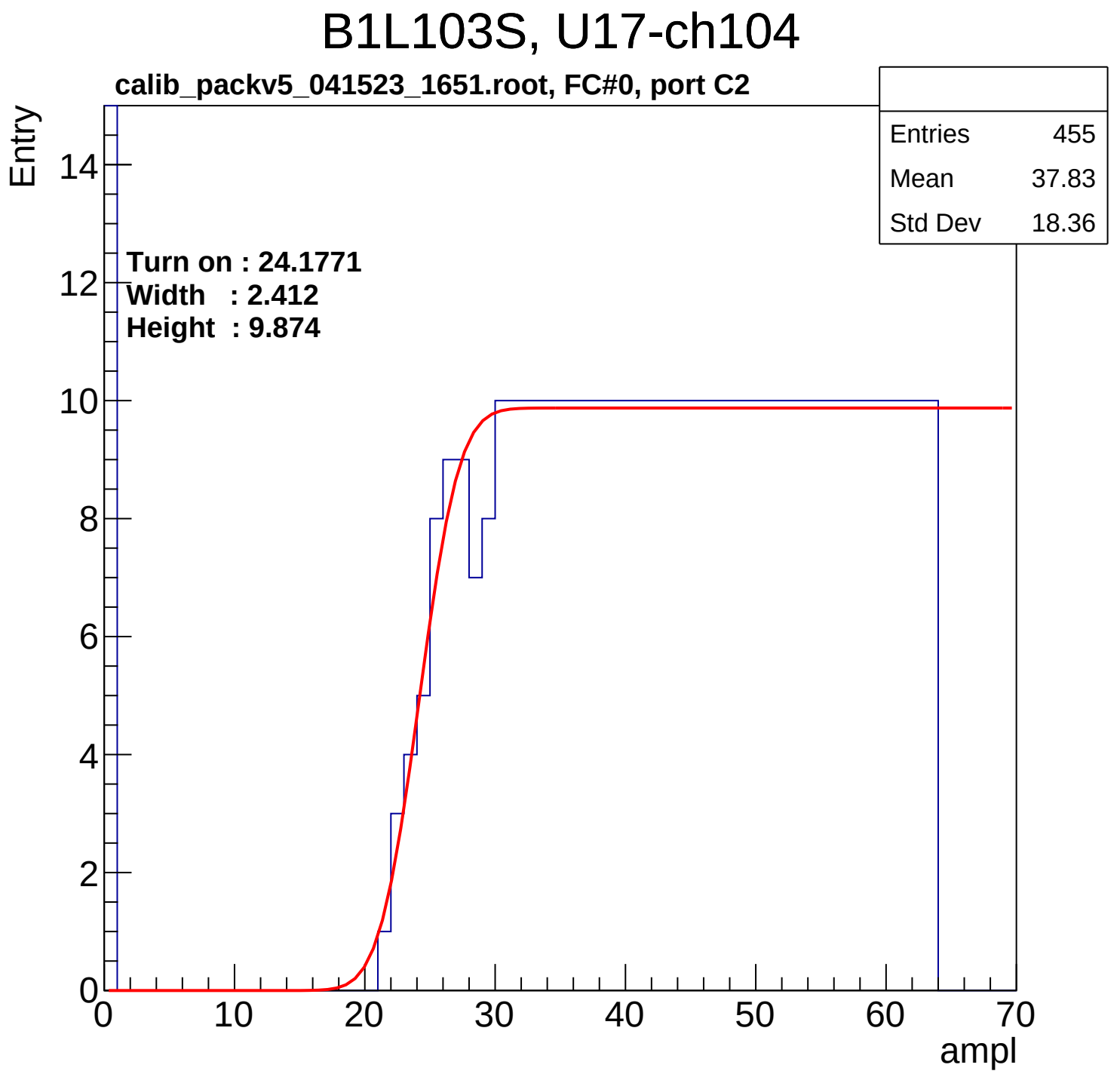
B1L103S, U17-ch104
calib_packv5_041523_1651.root, FC#0, port C2
Entries 455
Mean 37.83
Std Dev 18.36
Turn on : 24.1771
Width : 2.412
Height : 9.874
Entry
ampl
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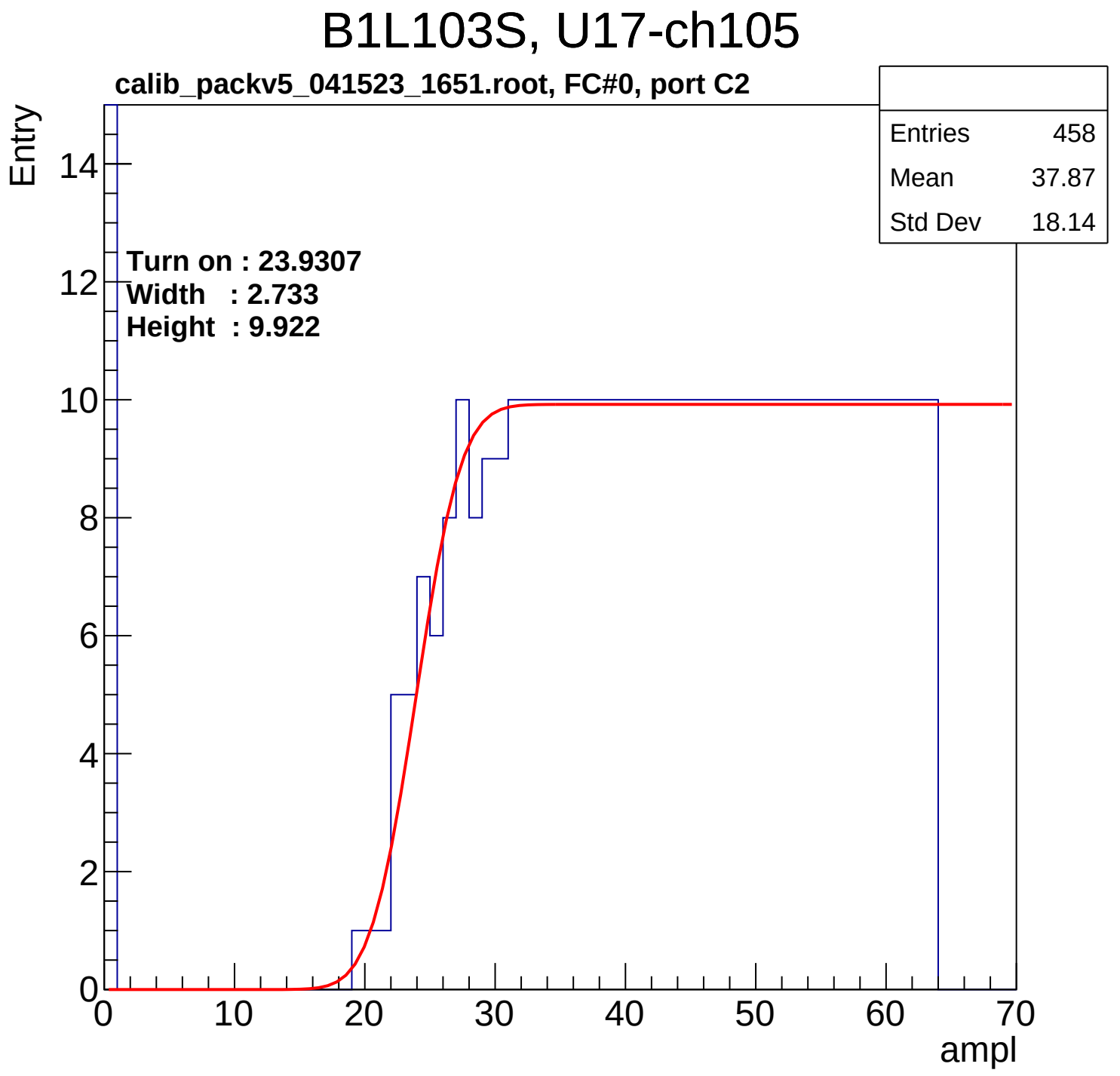
B1L103S, U17-ch105
calib_packv5_041523_1651.root, FC#0, port C2
Entries 458
Mean 37.87
Std Dev 18.14
Turn on : 23.9307
Width : 2.733
Height : 9.922
Entry
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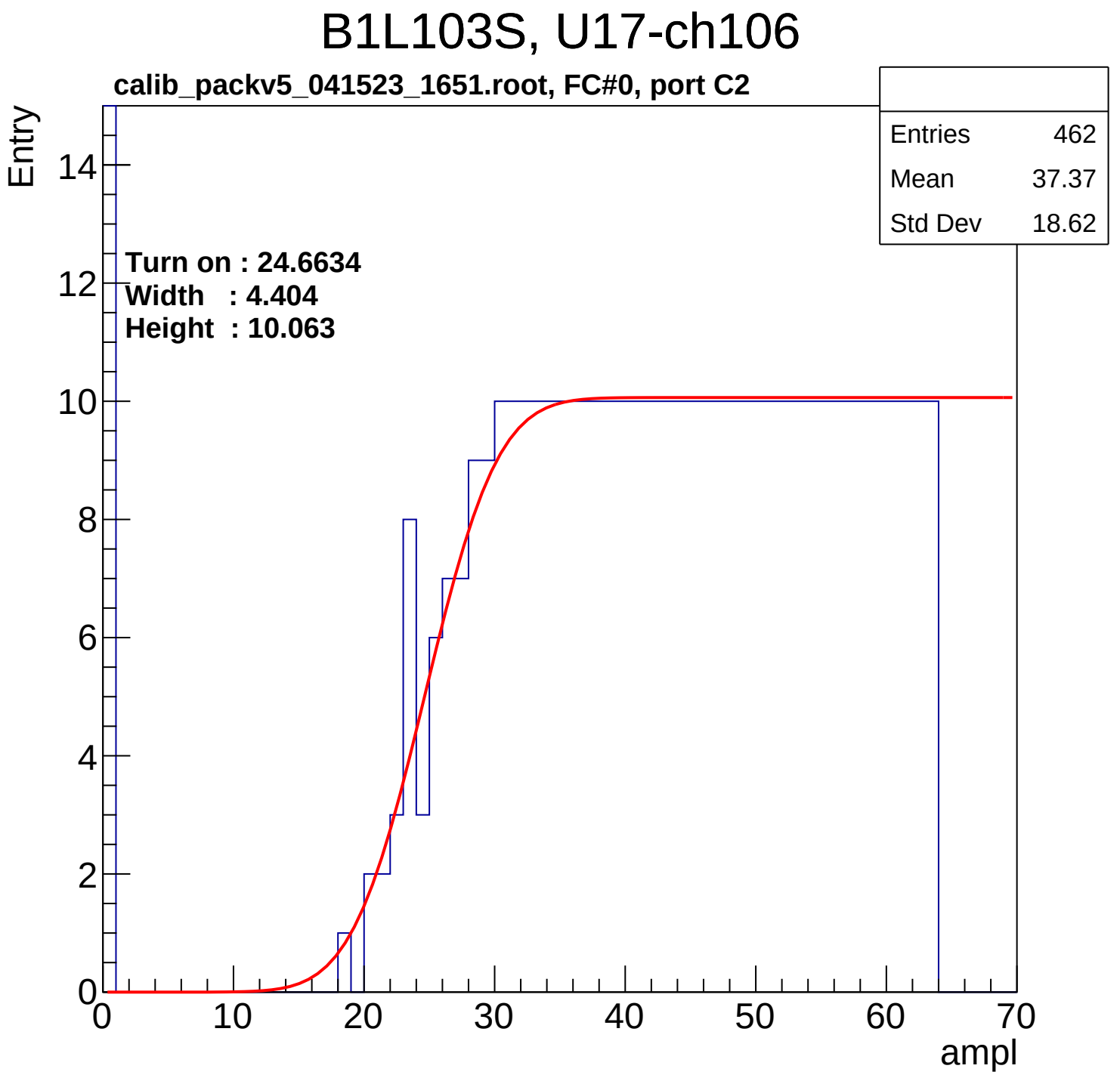
B1L103S, U17-ch106
calib_packv5_041523_1651.root, FC#0, port C2
Entries 462
Mean 37.37
Std Dev 18.62
Turn on : 24.6634
Width : 4.404
Height : 10.063
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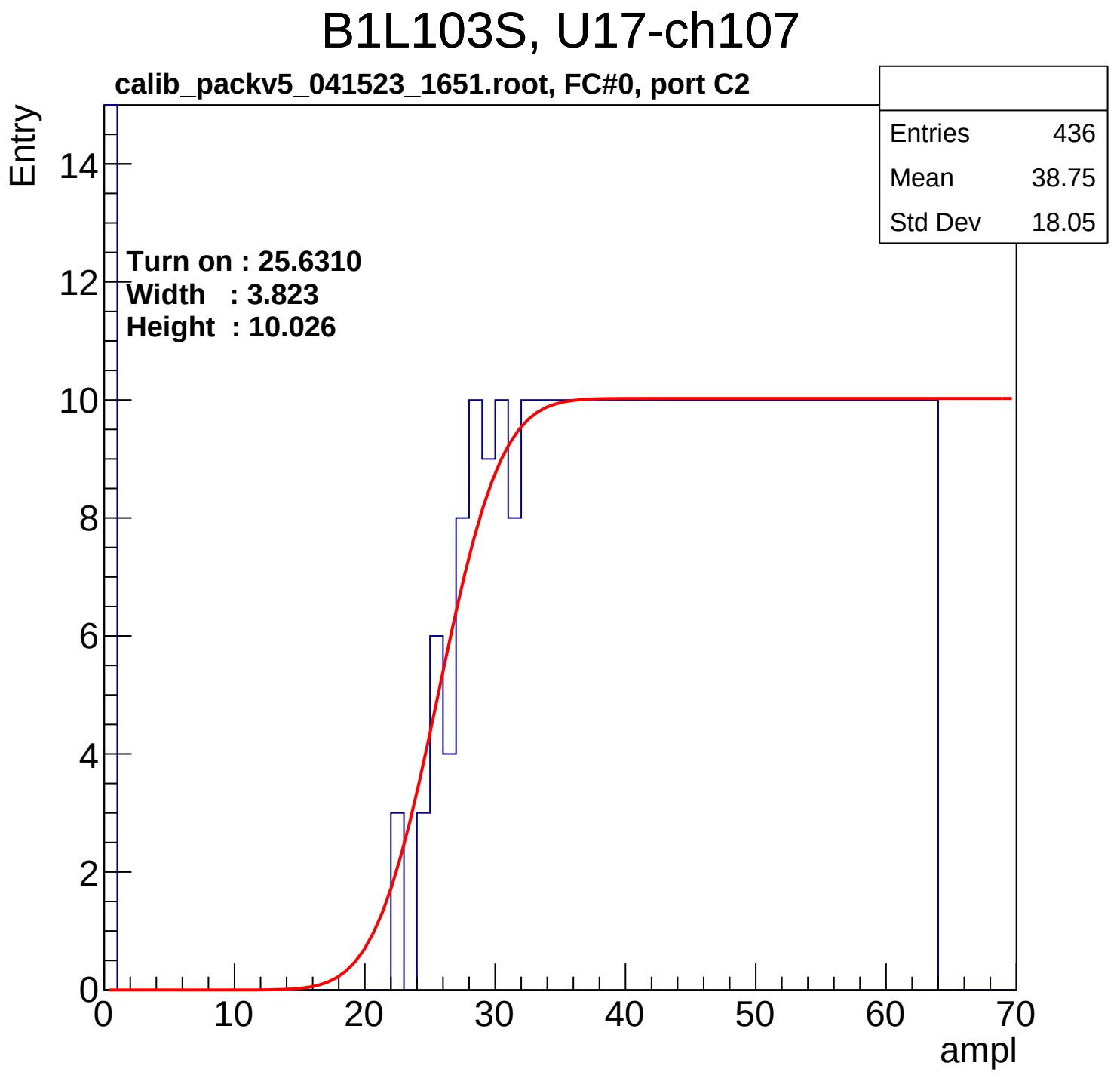
B1L103S, U17-ch107
calib_packv5_041523_1651.root, FC#0, port C2
Entries 436
Mean 38.75
Std Dev 18.05
Turn on : 25.6310
Width : 3.823
Height : 10.026
Entry
ampl
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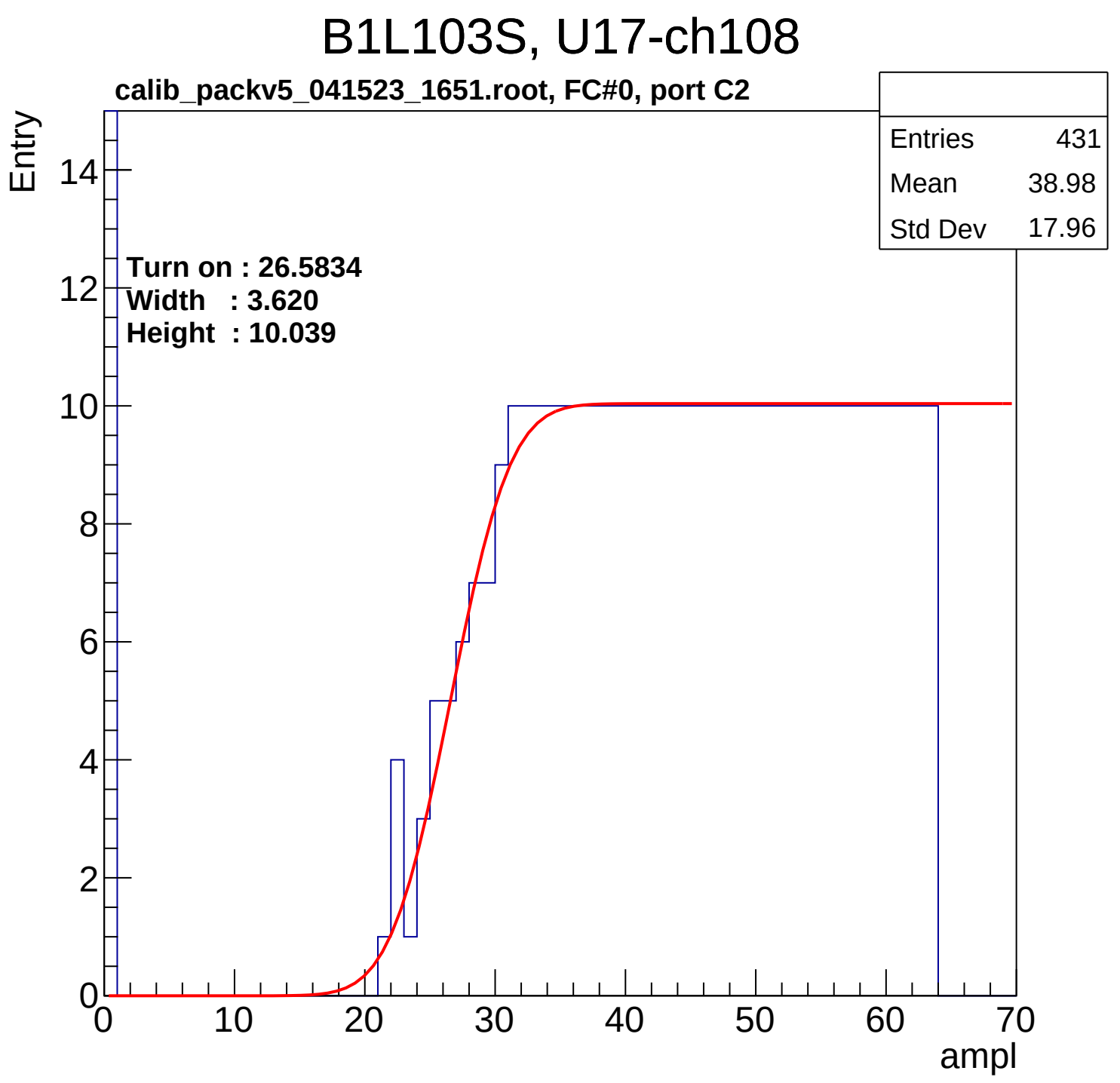
B1L103S, U17-ch108
calib_packv5_041523_1651.root, FC#0, port C2
Entries 431
Mean 38.98
Std Dev 17.96
Turn on : 26.5834
Width : 3.620
Height : 10.039
Entry
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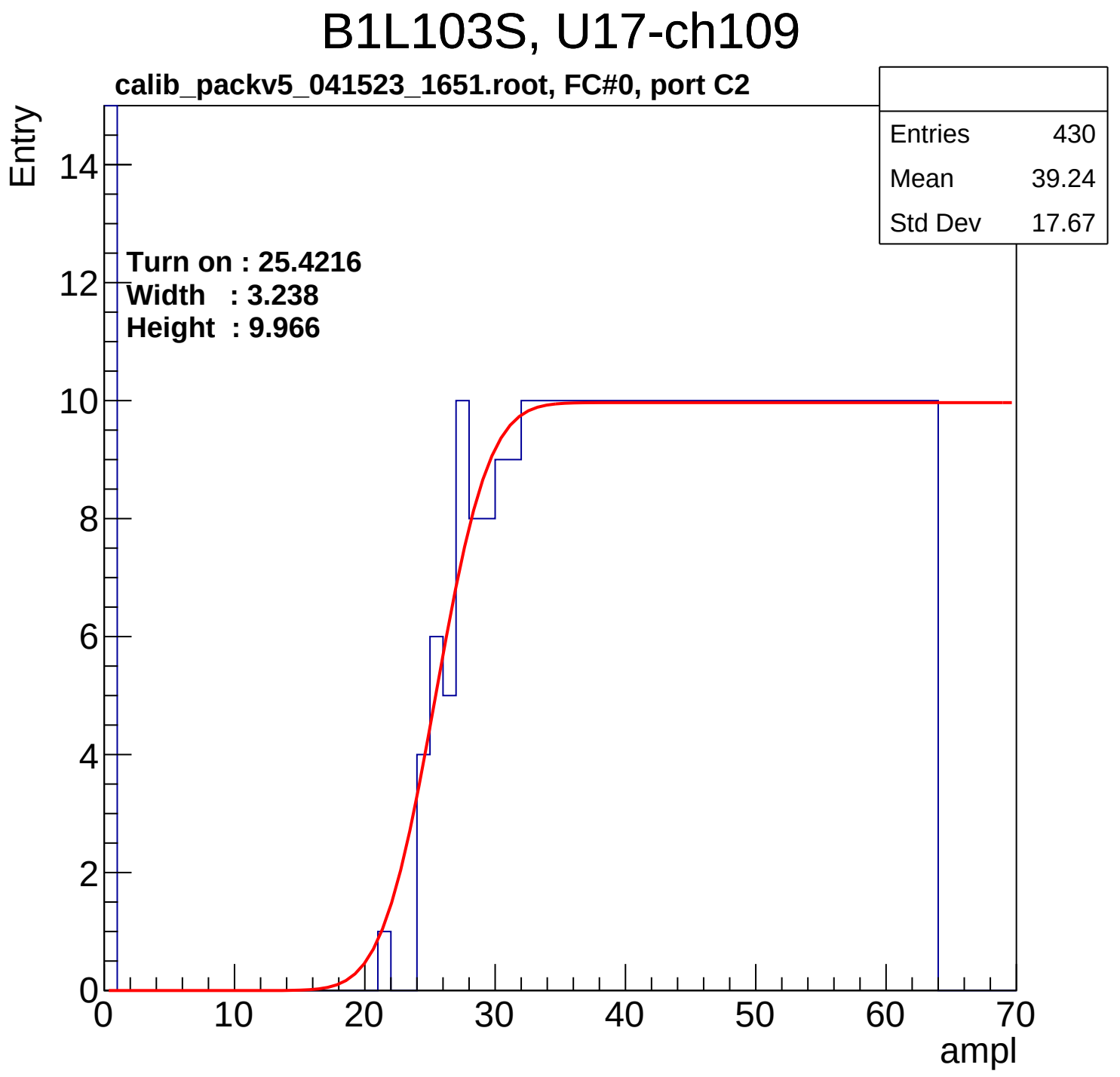
B1L103S, U17-ch109
calib_packv5_041523_1651.root, FC#0, port C2
Entries 430
Mean 39.24
Std Dev 17.67
Turn on : 25.4216
Width : 3.238
Height : 9.966
Entry
ampl
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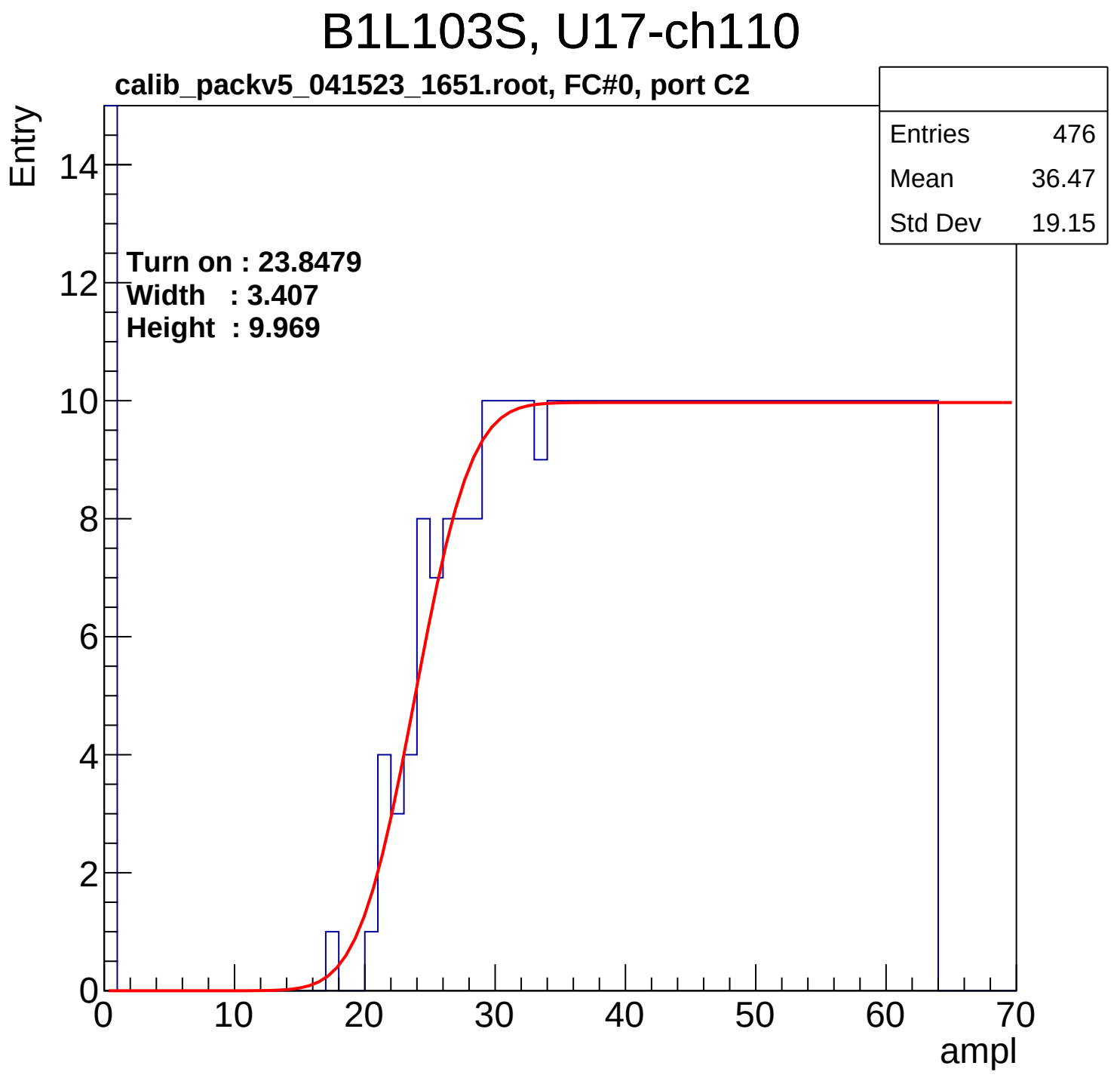
B1L103S, U17-ch110
calib_packv5_041523_1651.root, FC#0, port C2
Entries 476
Mean 36.47
Std Dev 19.15
Turn on : 23.8479
Width : 3.407
Height : 9.969
Entry
ampl
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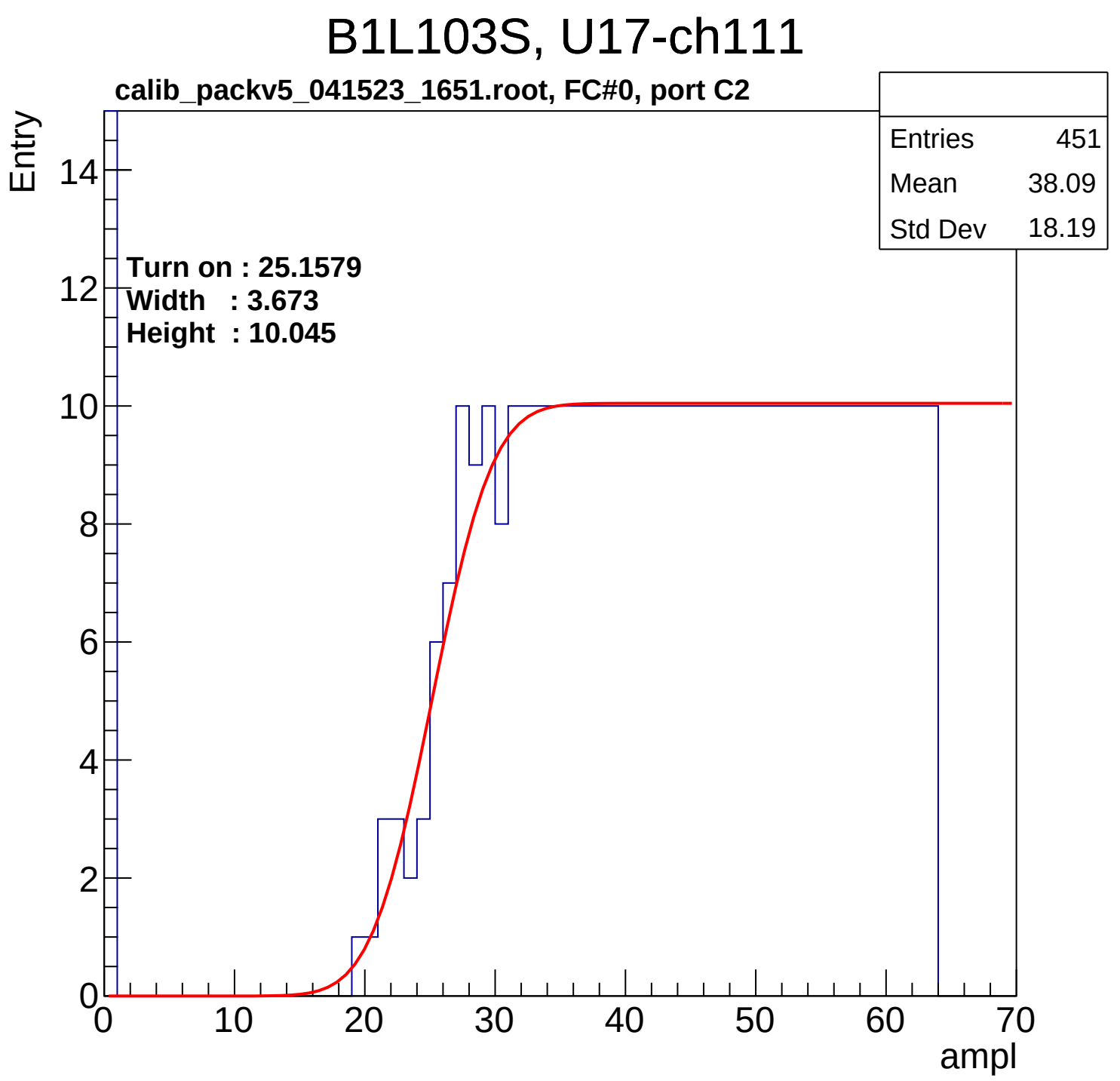
B1L103S, U17-ch111
calib_packv5_041523_1651.root, FC#0, port C2
Entries 451
Mean 38.09
Std Dev 18.19
Turn on : 25.1579
Width : 3.673
Height : 10.045
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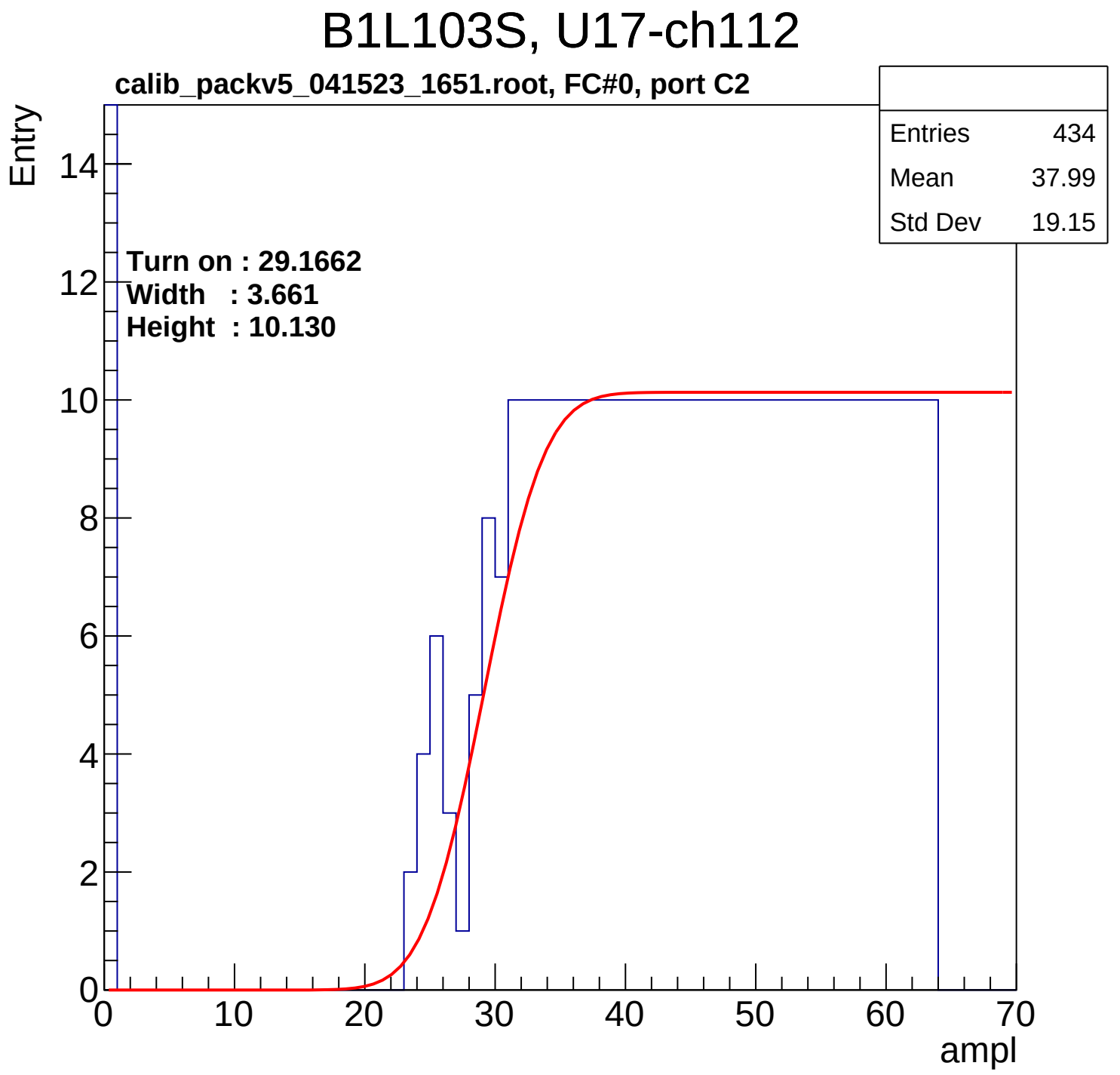
B1L103S, U17-ch112
calib_packv5_041523_1651.root, FC#0, port C2
Entries 434
Mean 37.99
Std Dev 19.15
Turn on : 29.1662
Width : 3.661
Height : 10.130
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ampl
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6
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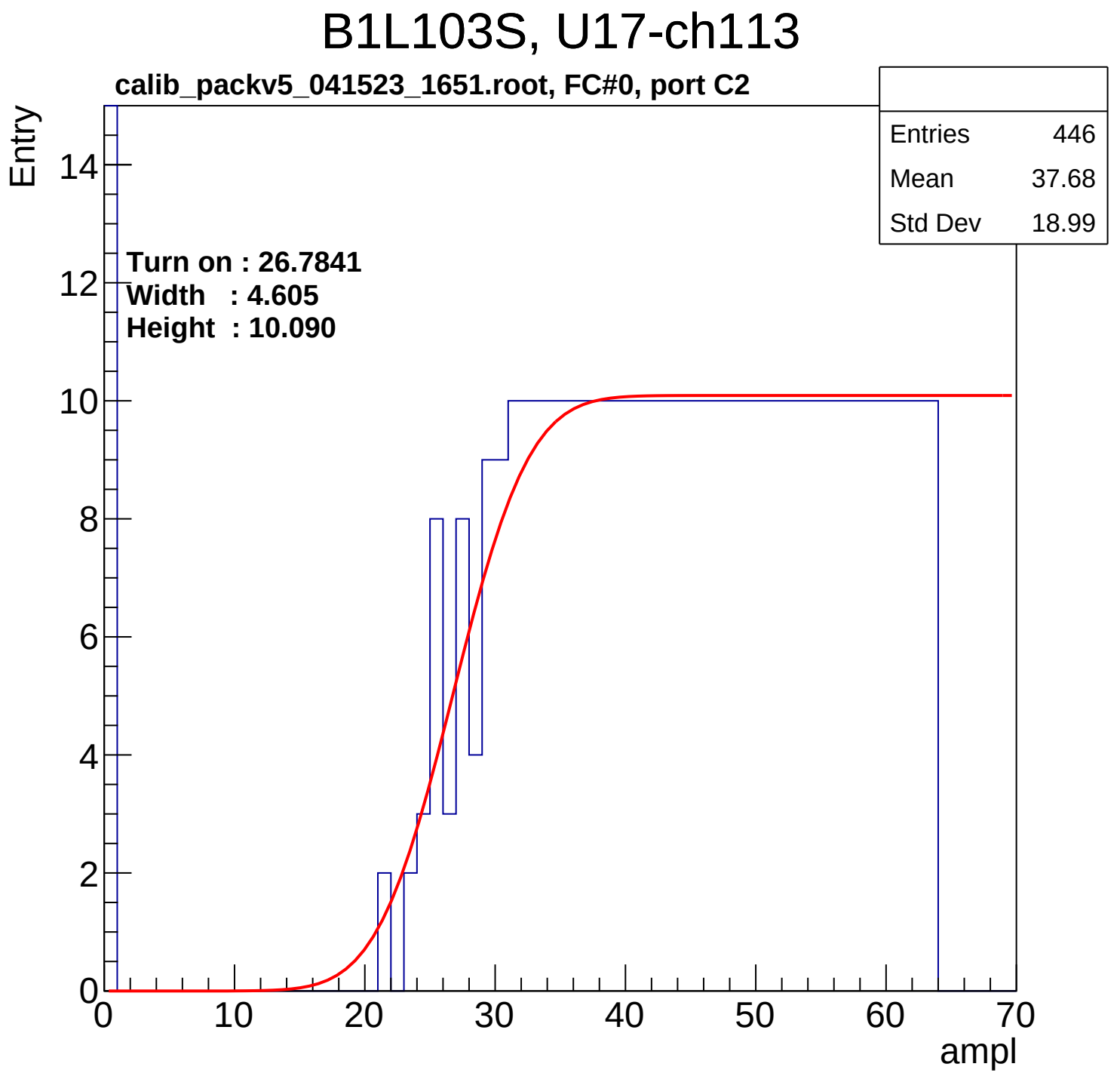
B1L103S, U17-ch113
calib_packv5_041523_1651.root, FC#0, port C2
Entries 446
Mean 37.68
Std Dev 18.99
Turn on : 26.7841
Width : 4.605
Height : 10.090
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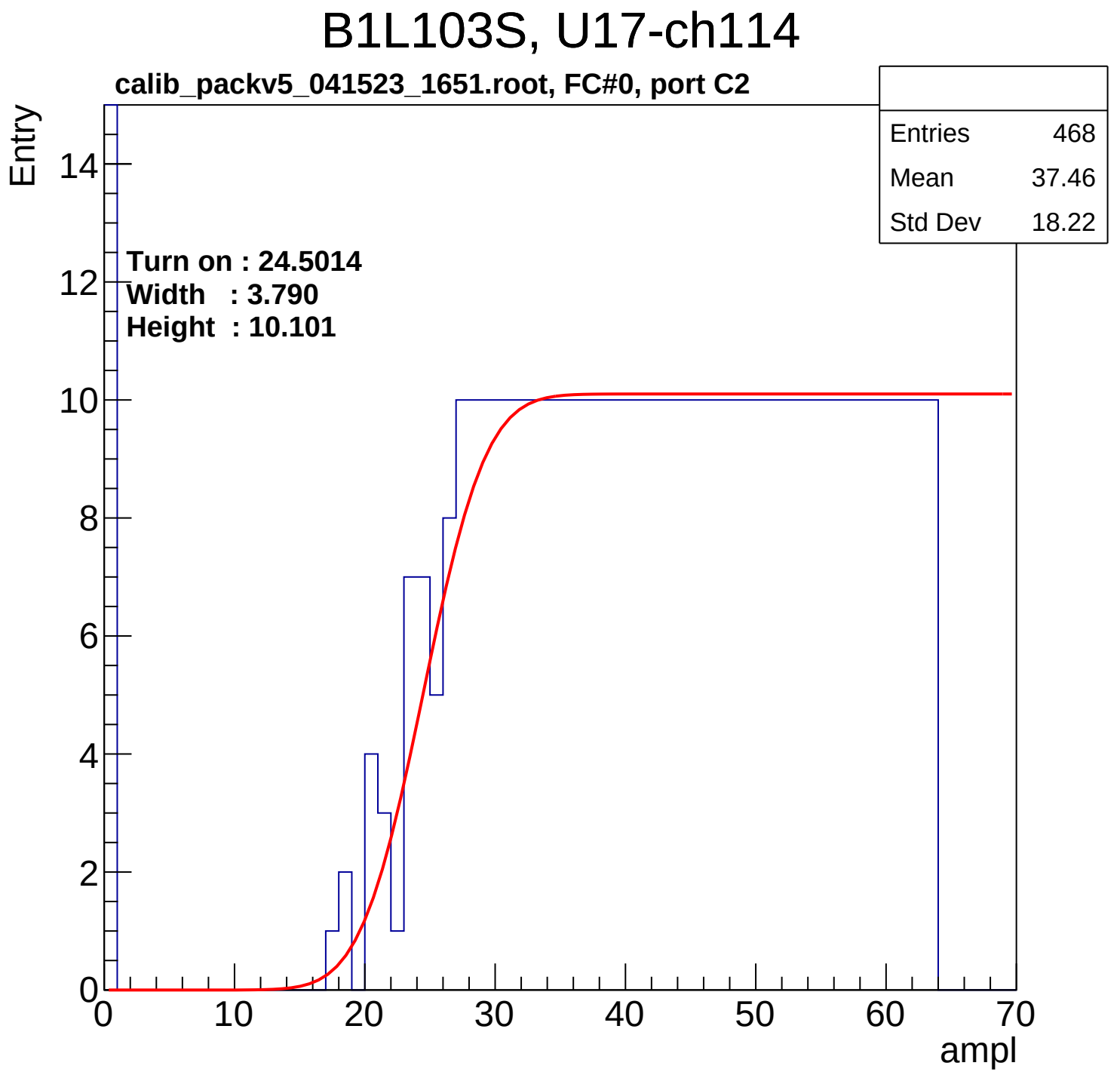
B1L103S, U17-ch114
calib_packv5_041523_1651.root, FC#0, port C2
Entries 468
Mean 37.46
Std Dev 18.22
Turn on : 24.5014
Width : 3.790
Height : 10.101
Entry
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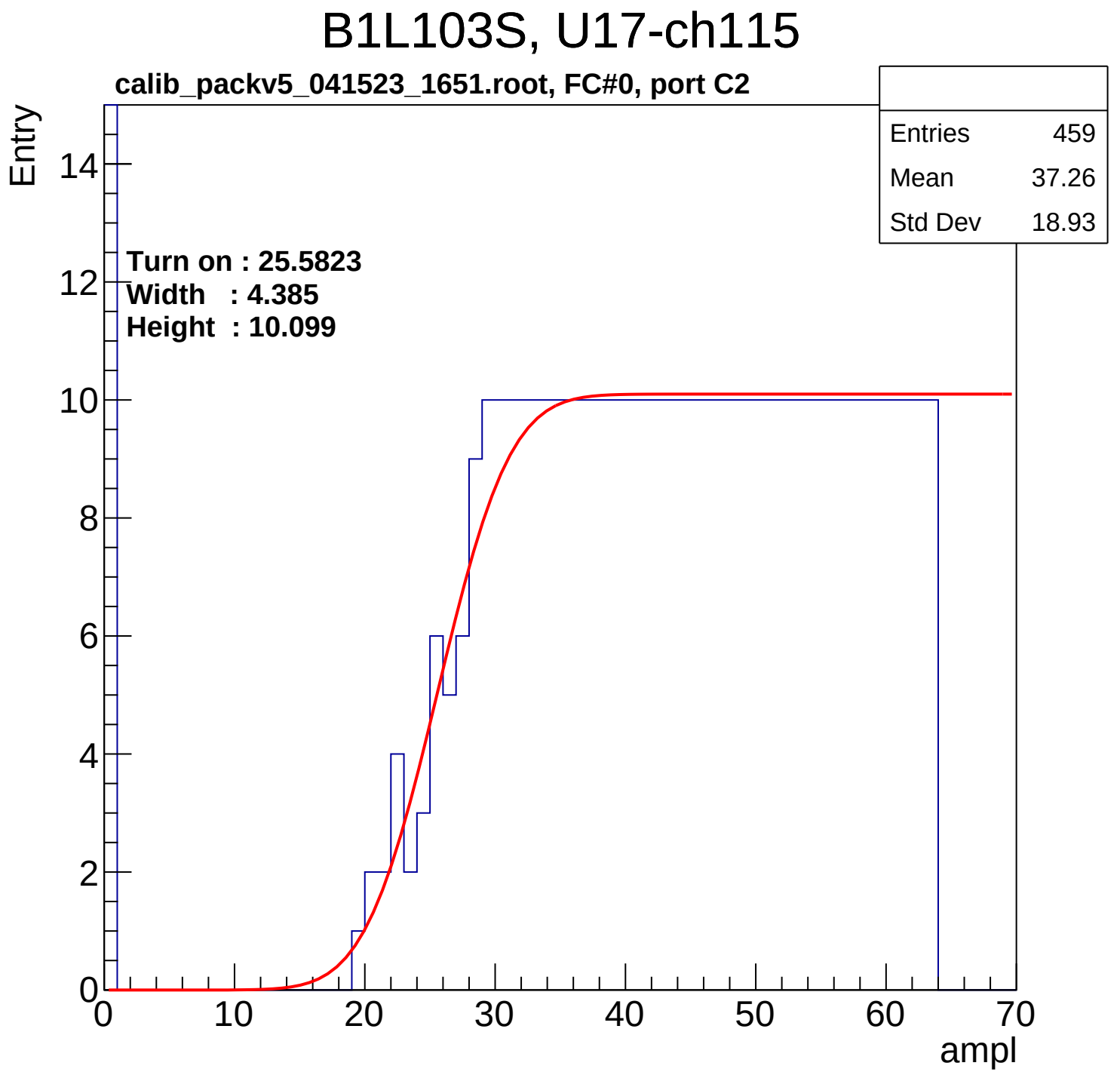
B1L103S, U17-ch115
calib_packv5_041523_1651.root, FC#0, port C2
Entries 459
Mean 37.26
Std Dev 18.93
Turn on : 25.5823
Width : 4.385
Height : 10.099
Entry
ampl
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6
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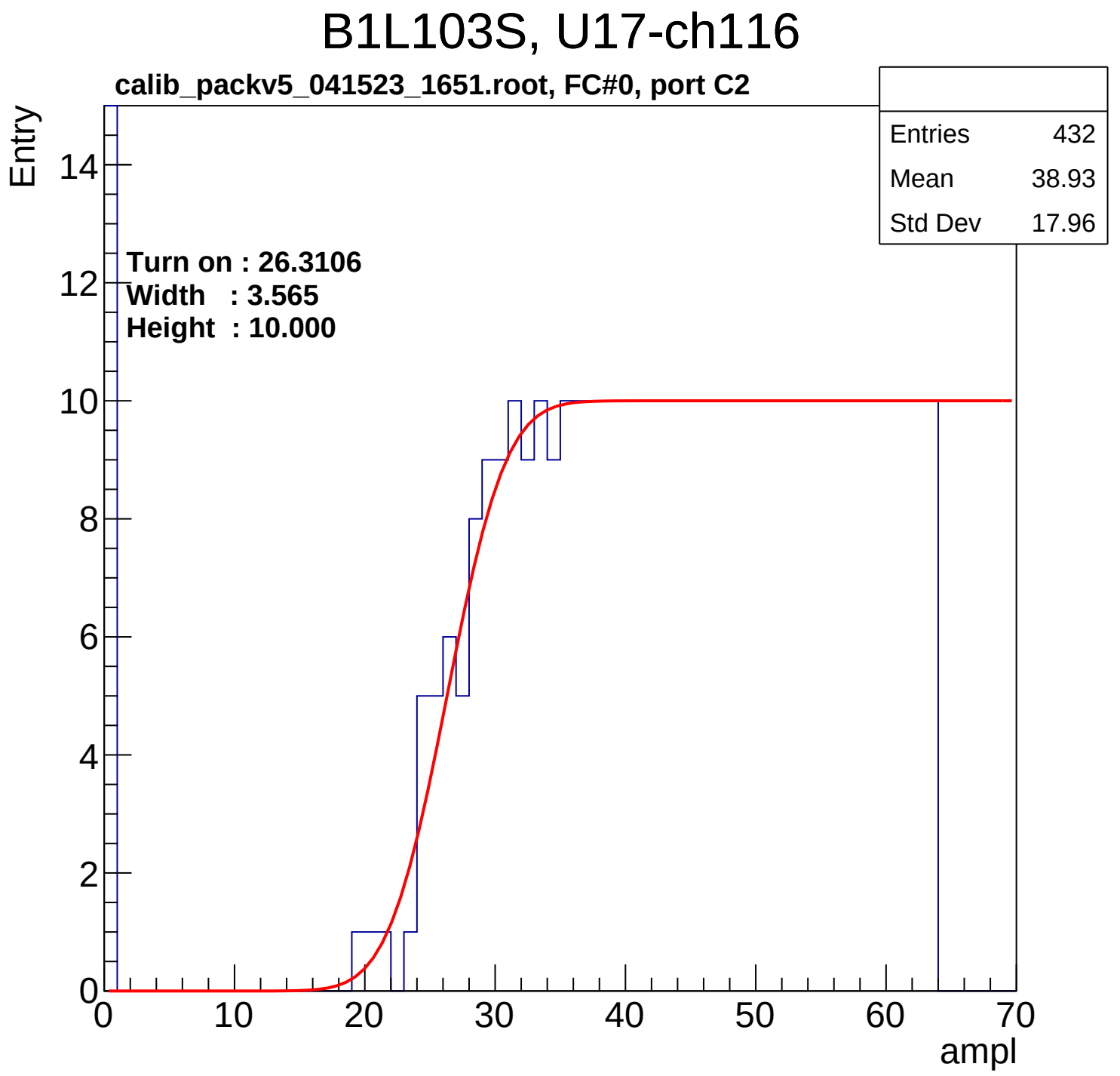
B1L103S, U17-ch116
calib_packv5_041523_1651.root, FC#0, port C2
Entries 432
Mean 38.93
Std Dev 17.96
Turn on : 26.3106
Width : 3.565
Height : 10.000
Entry
ampl
0
2
4
6
8
10
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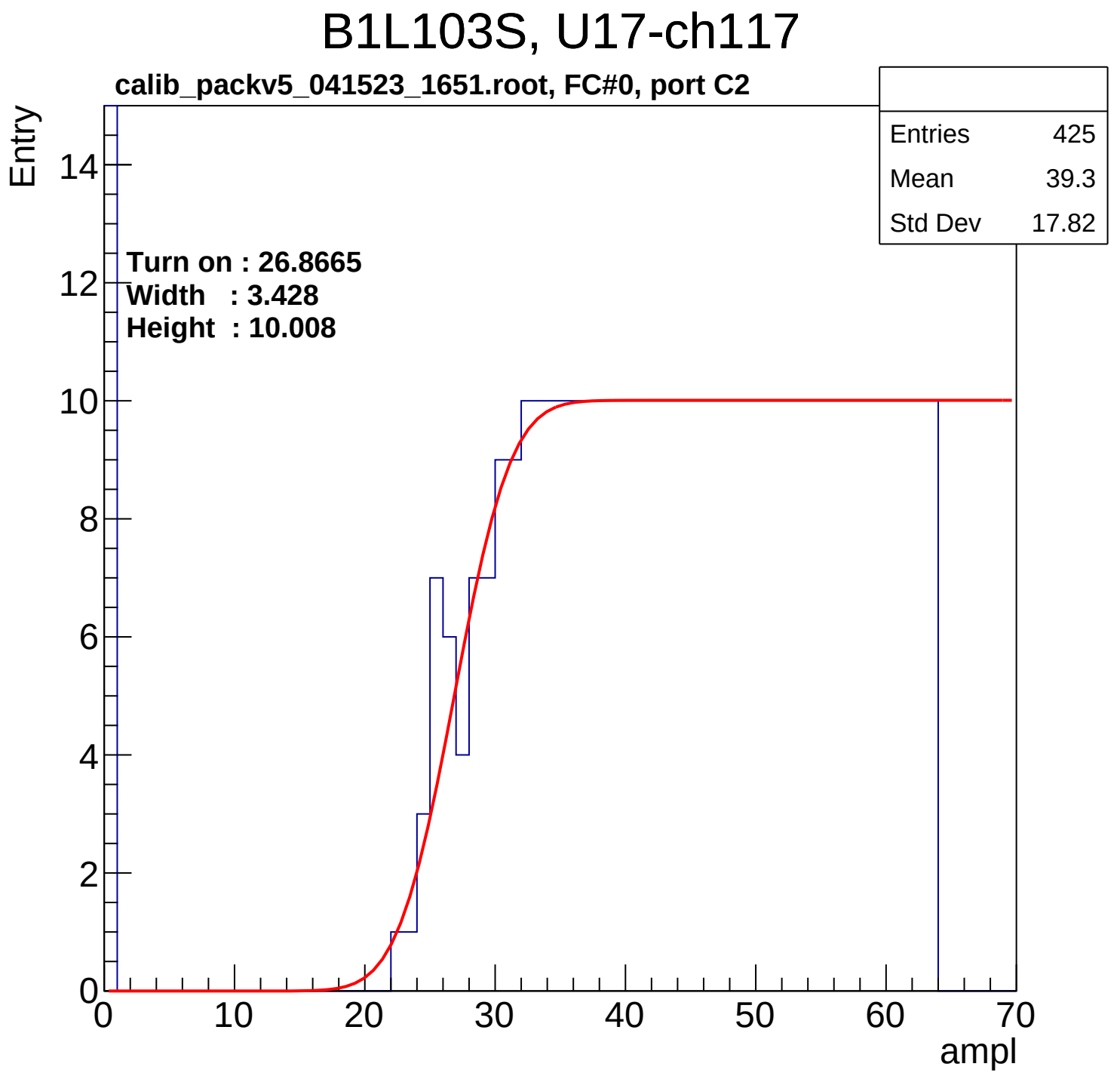
B1L103S, U17-ch117
calib_packv5_041523_1651.root, FC#0, port C2
Entries 425
Mean 39.3
Std Dev 17.82
Turn on : 26.8665
Width : 3.428
Height : 10.008
Entry
ampl
0
2
4
6
8
10
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0
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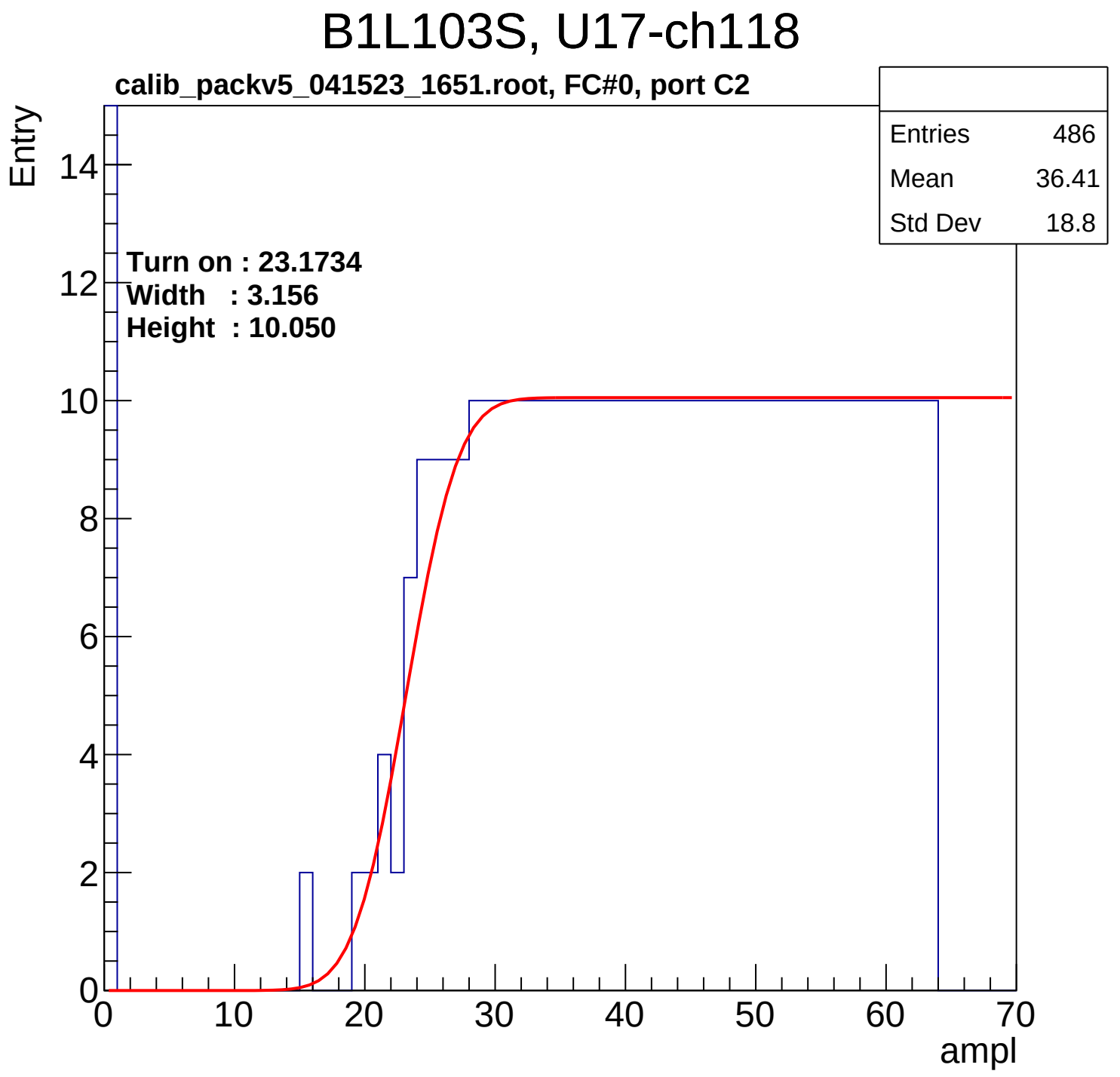
B1L103S, U17-ch118
calib_packv5_041523_1651.root, FC#0, port C2
Entries 486
Mean 36.41
Std Dev 18.8
Turn on : 23.1734
Width : 3.156
Height : 10.050
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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60
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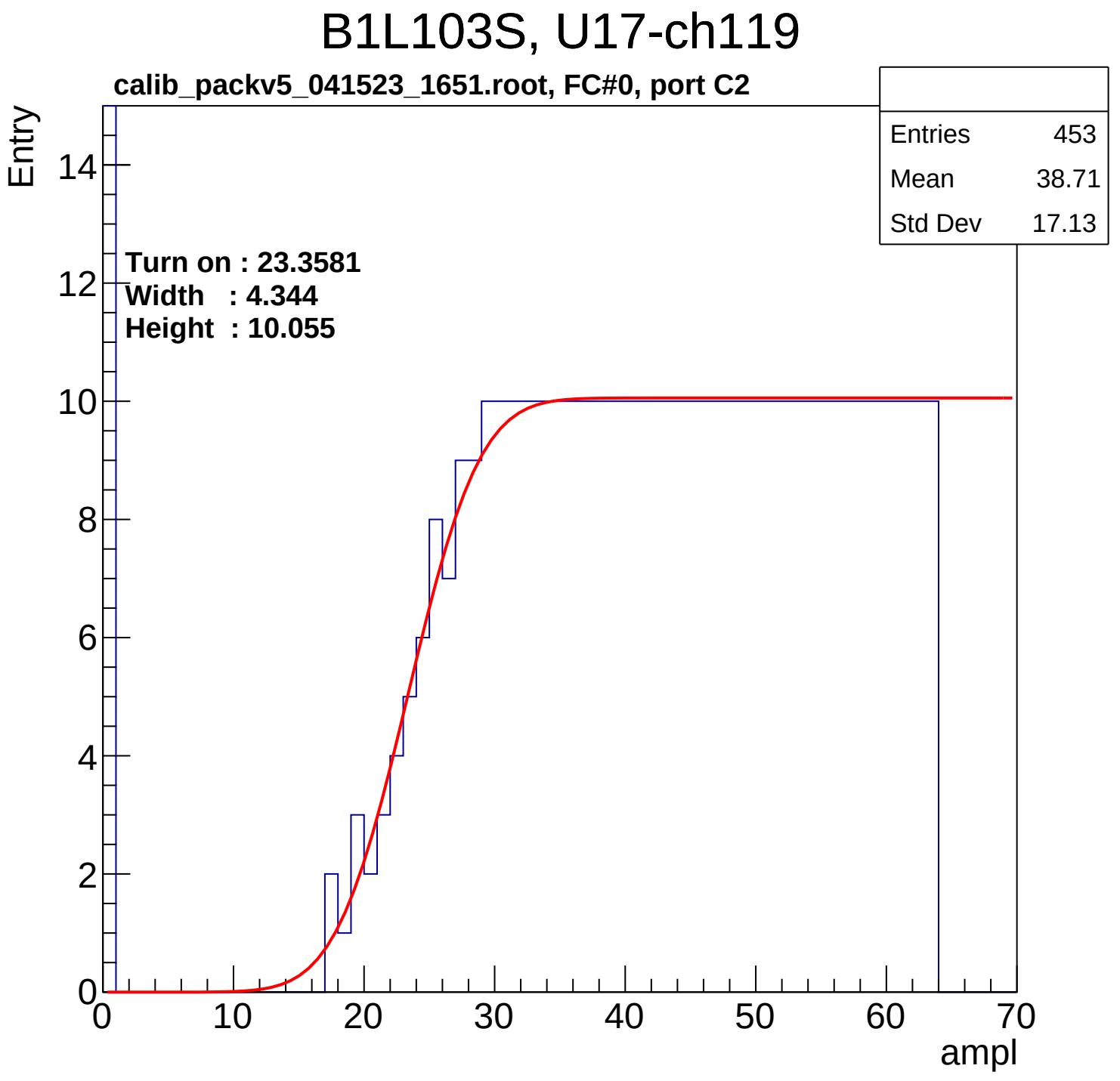
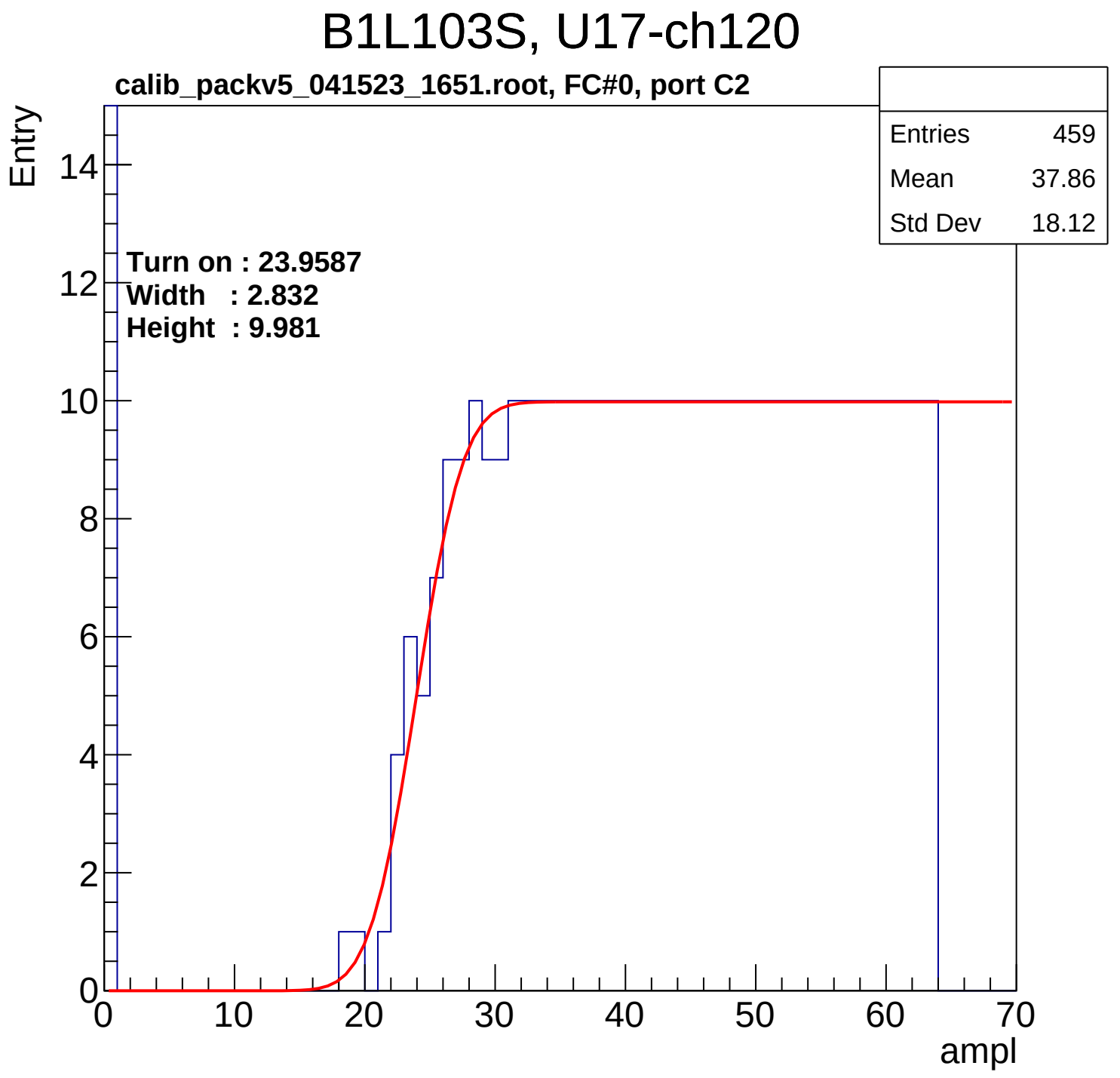

B1L103S, U17-ch119
calib_packv5_041523_1651.root, FC#0, port C2
Entries 453
Mean 38.71
Std Dev 17.13
Turn on : 23.3581
Width : 4.344
Height : 10.055
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U17-ch120
calib_packv5_041523_1651.root, FC#0, port C2
Entries 459
Mean 37.86
Std Dev 18.12
Turn on : 23.9587
Width : 2.832
Height : 9.981
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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60
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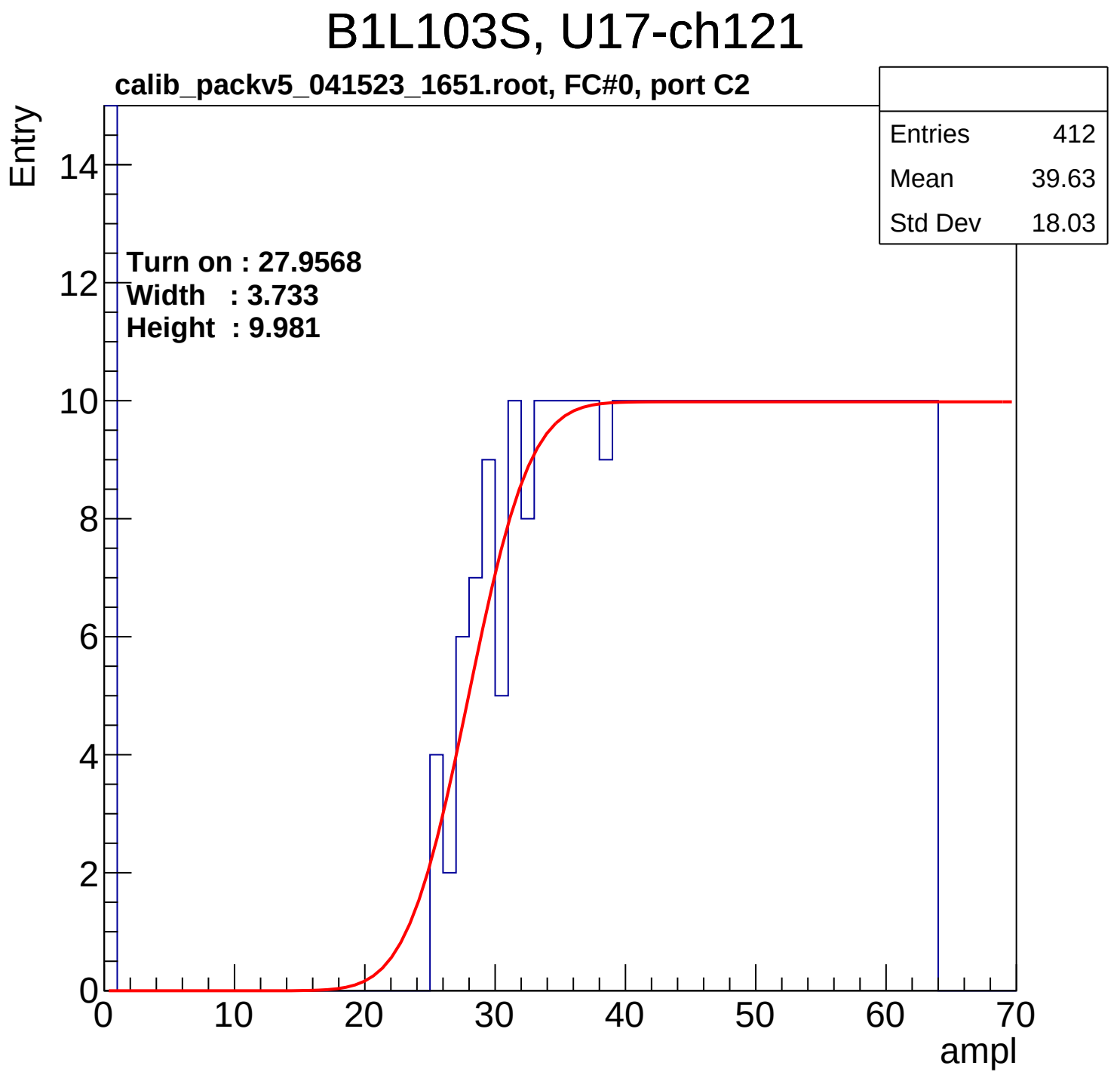
B1L103S, U17-ch121
calib_packv5_041523_1651.root, FC#0, port C2
Entries 412
Mean 39.63
Std Dev 18.03
Turn on : 27.9568
Width : 3.733
Height : 9.981
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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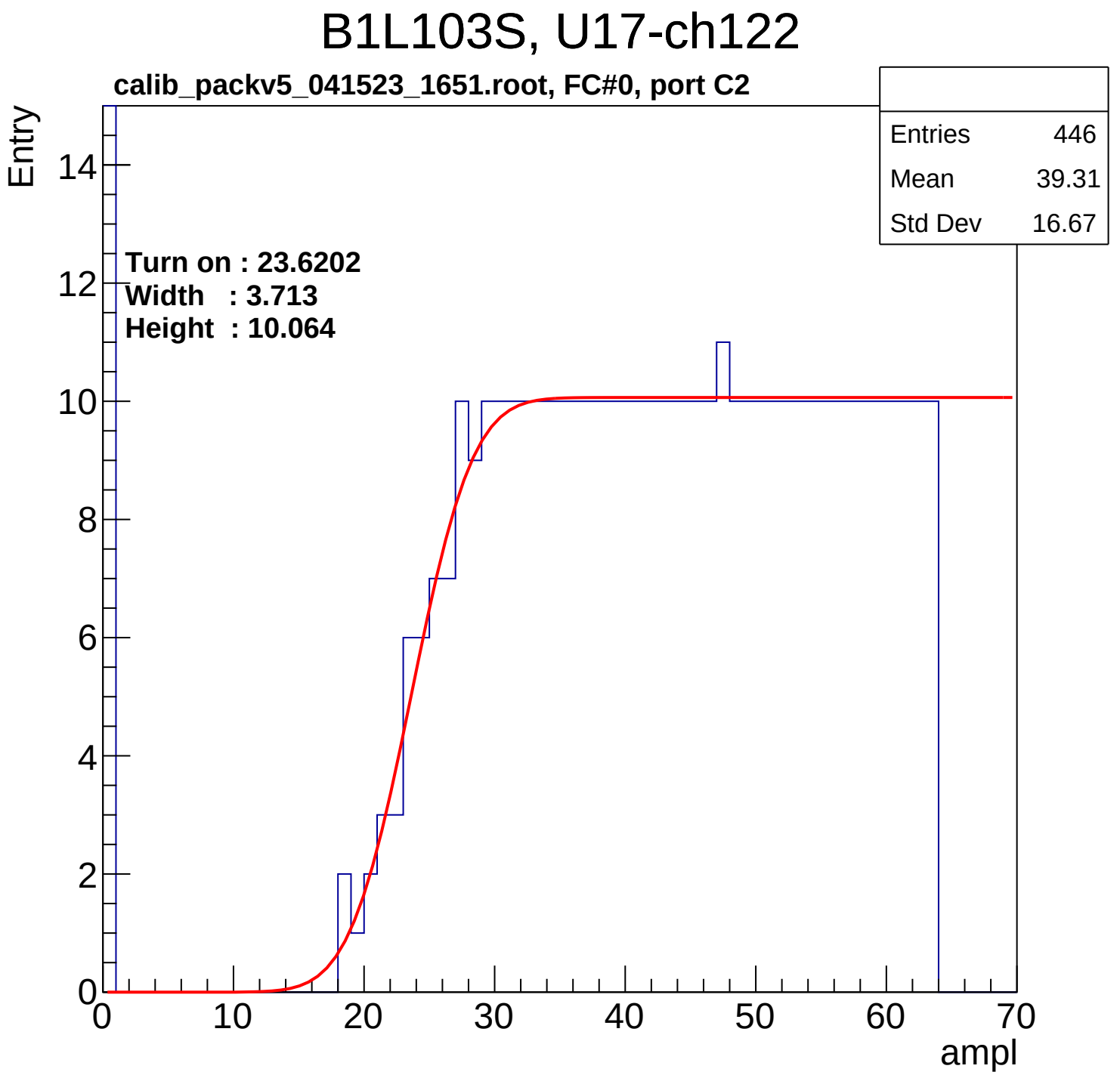
B1L103S, U17-ch122
calib_packv5_041523_1651.root, FC#0, port C2
Entries 446
Mean 39.31
Std Dev 16.67
Turn on : 23.6202
Width : 3.713
Height : 10.064
Entry
ampl
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2
4
6
8
10
12
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0
10
20
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40
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60
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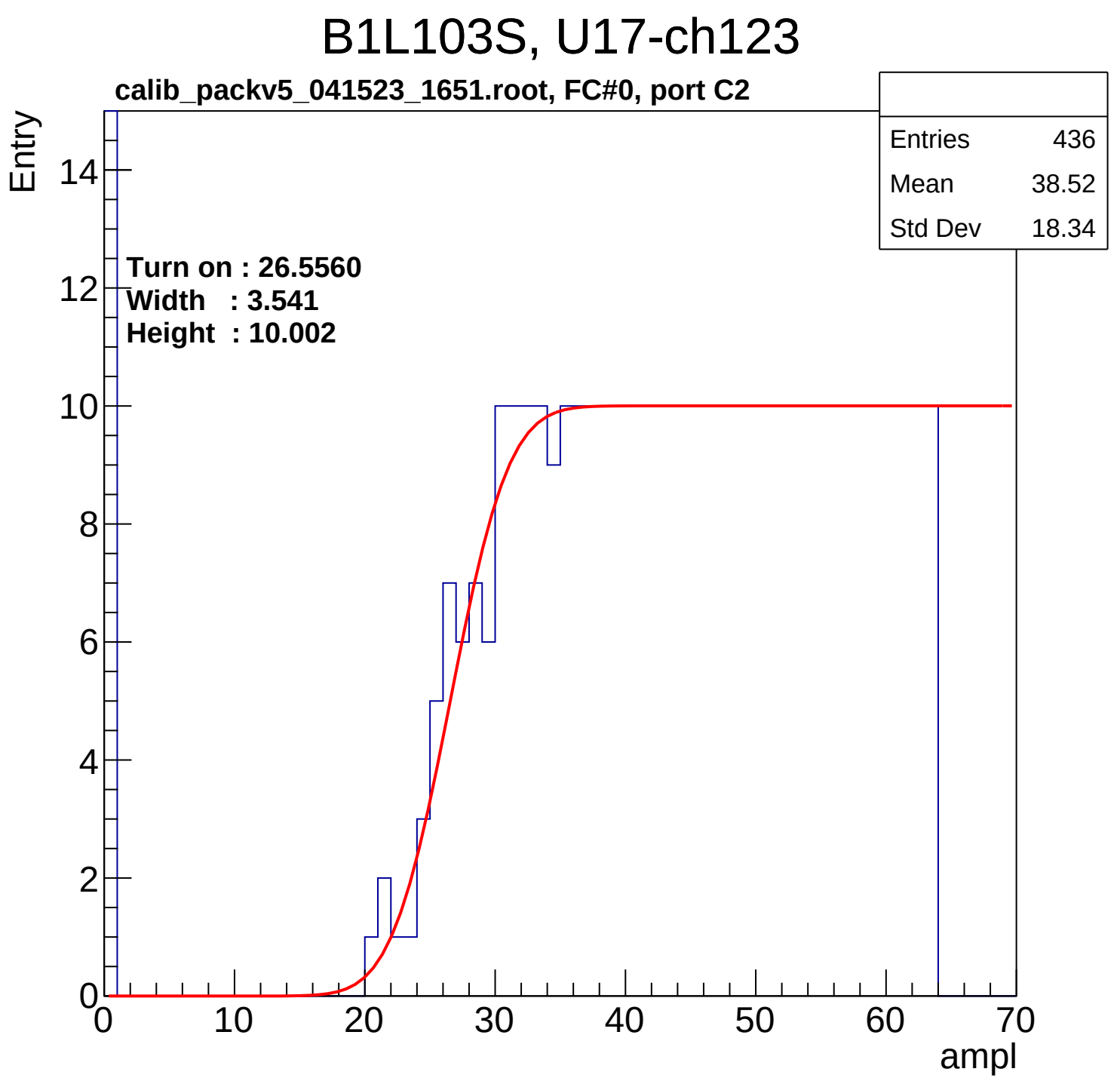
B1L103S, U17-ch123
calib_packv5_041523_1651.root, FC#0, port C2
Entries 436
Mean 38.52
Std Dev 18.34
Turn on : 26.5560
Width : 3.541
Height : 10.002
Entry
ampl
0
2
4
6
8
10
12
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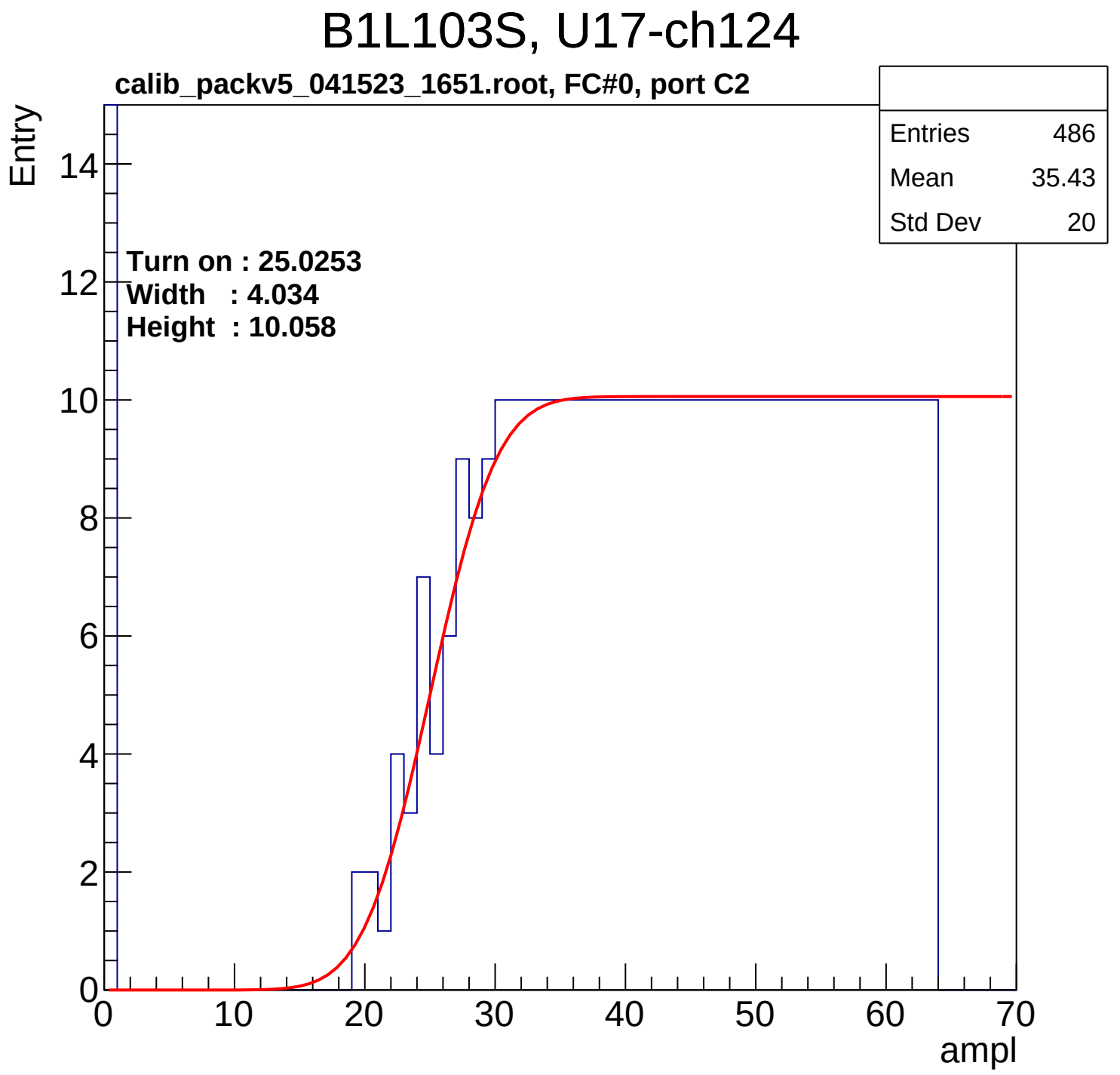
0
10
20
30
40
50
60
70


B1L103S, U17-ch124
calib_packv5_041523_1651.root, FC#0, port C2
Entries 486
Mean 35.43
Std Dev 20
Turn on : 25.0253
Width : 4.034
Height : 10.058
Entry
ampl
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2
4
6
8
10
12
14
0
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20
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40
50
60
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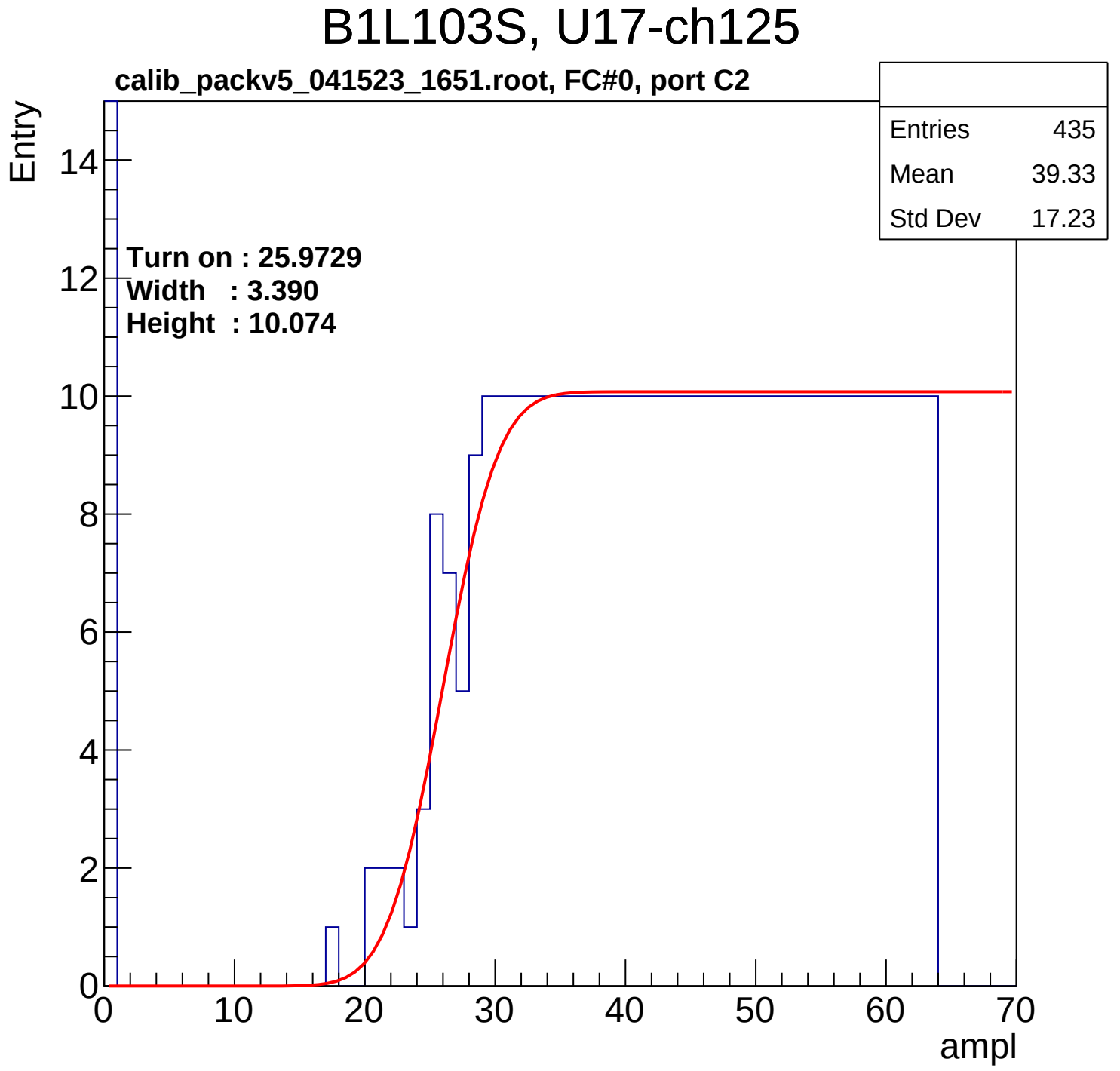
B1L103S, U17-ch125
calib_packv5_041523_1651.root, FC#0, port C2
Entries 435
Mean 39.33
Std Dev 17.23
Turn on : 25.9729
Width : 3.390
Height : 10.074
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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40
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60
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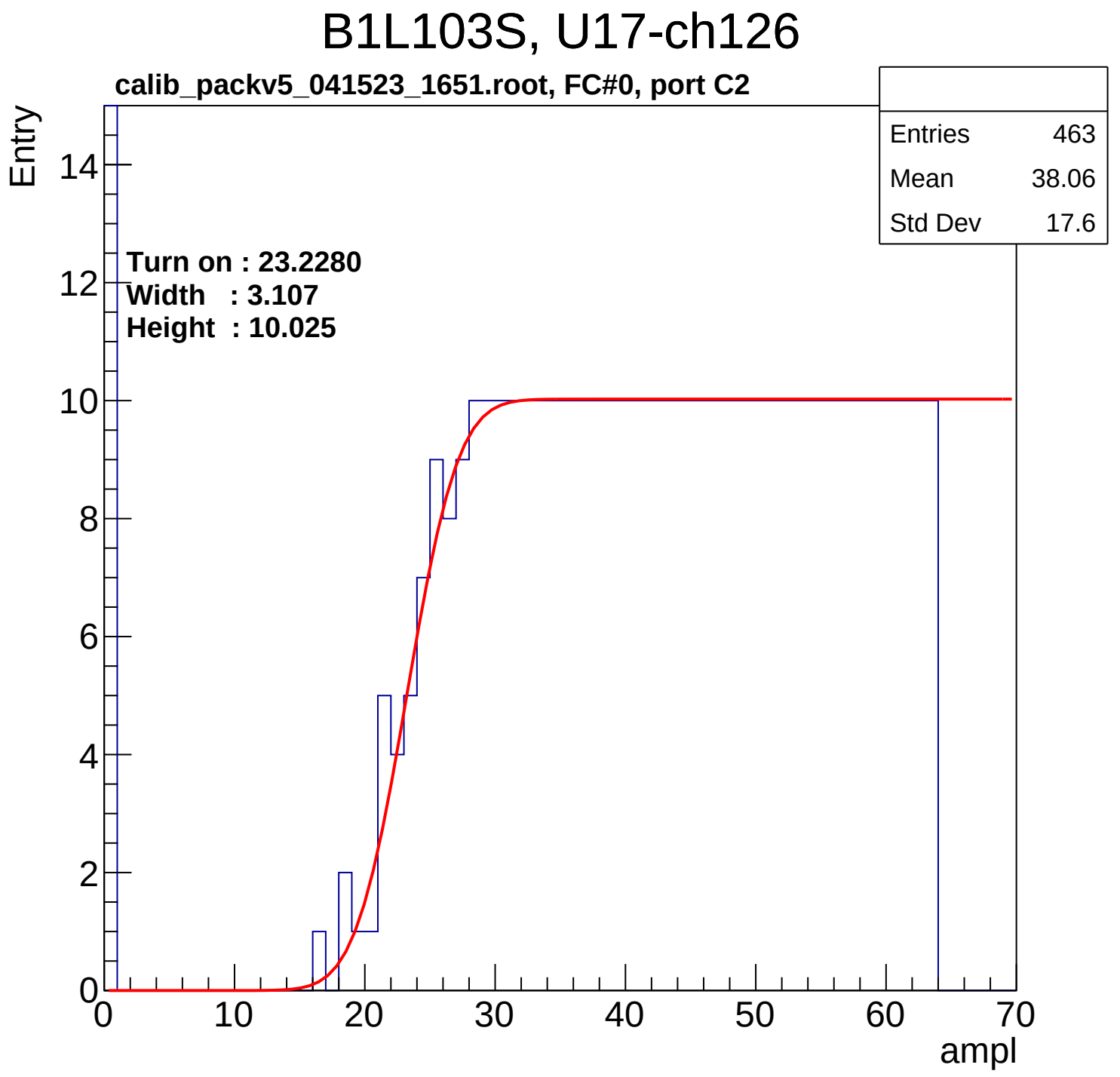
B1L103S, U17-ch126
calib_packv5_041523_1651.root, FC#0, port C2
Entries 463
Mean 38.06
Std Dev 17.6
Turn on : 23.2280
Width : 3.107
Height : 10.025
Entry
ampl
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4
6
8
10
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0
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20
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60
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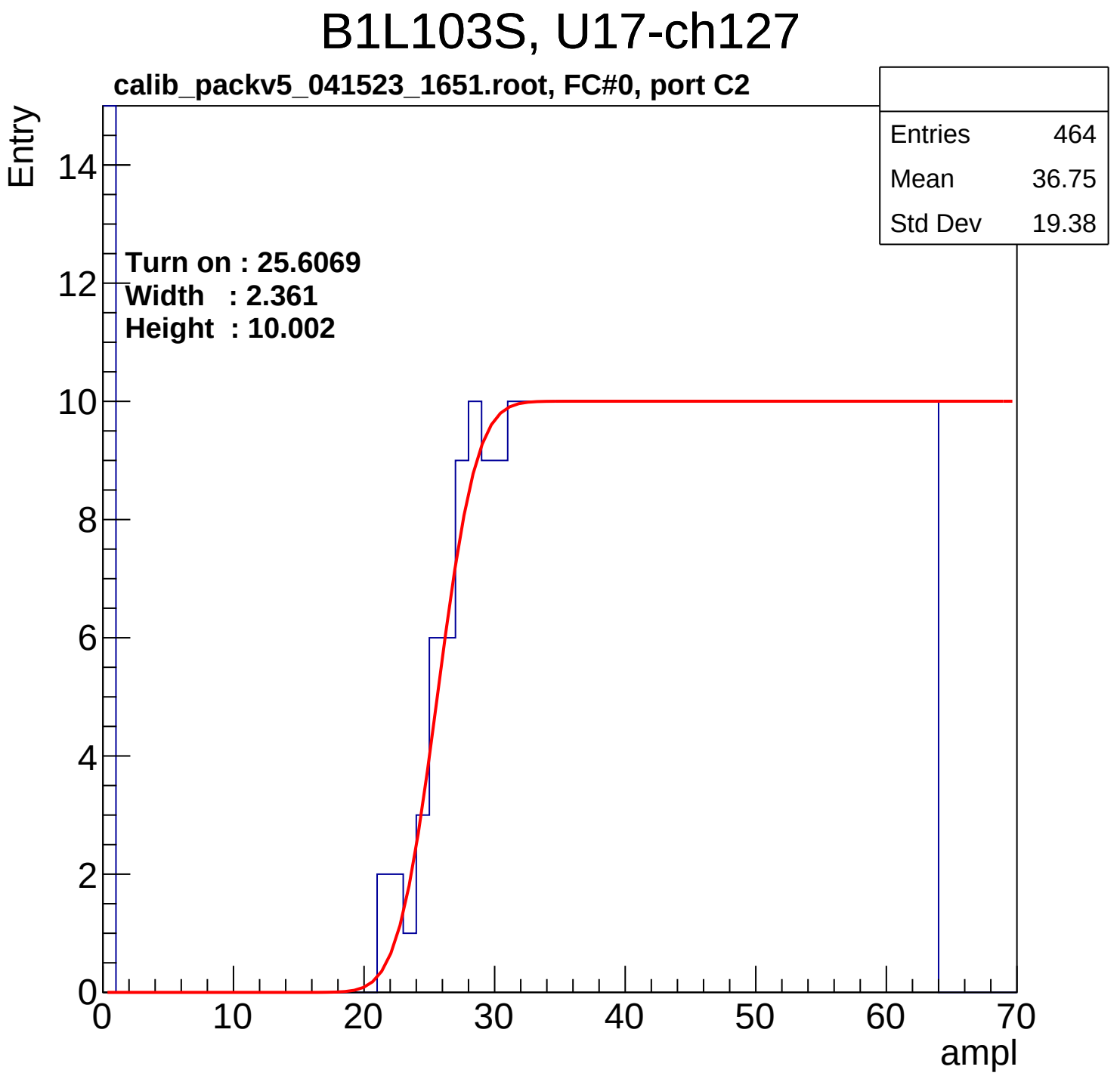
B1L103S, U17-ch127
calib_packv5_041523_1651.root, FC#0, port C2
Entries 464
Mean 36.75
Std Dev 19.38
Turn on : 25.6069
Width : 2.361
Height : 10.002
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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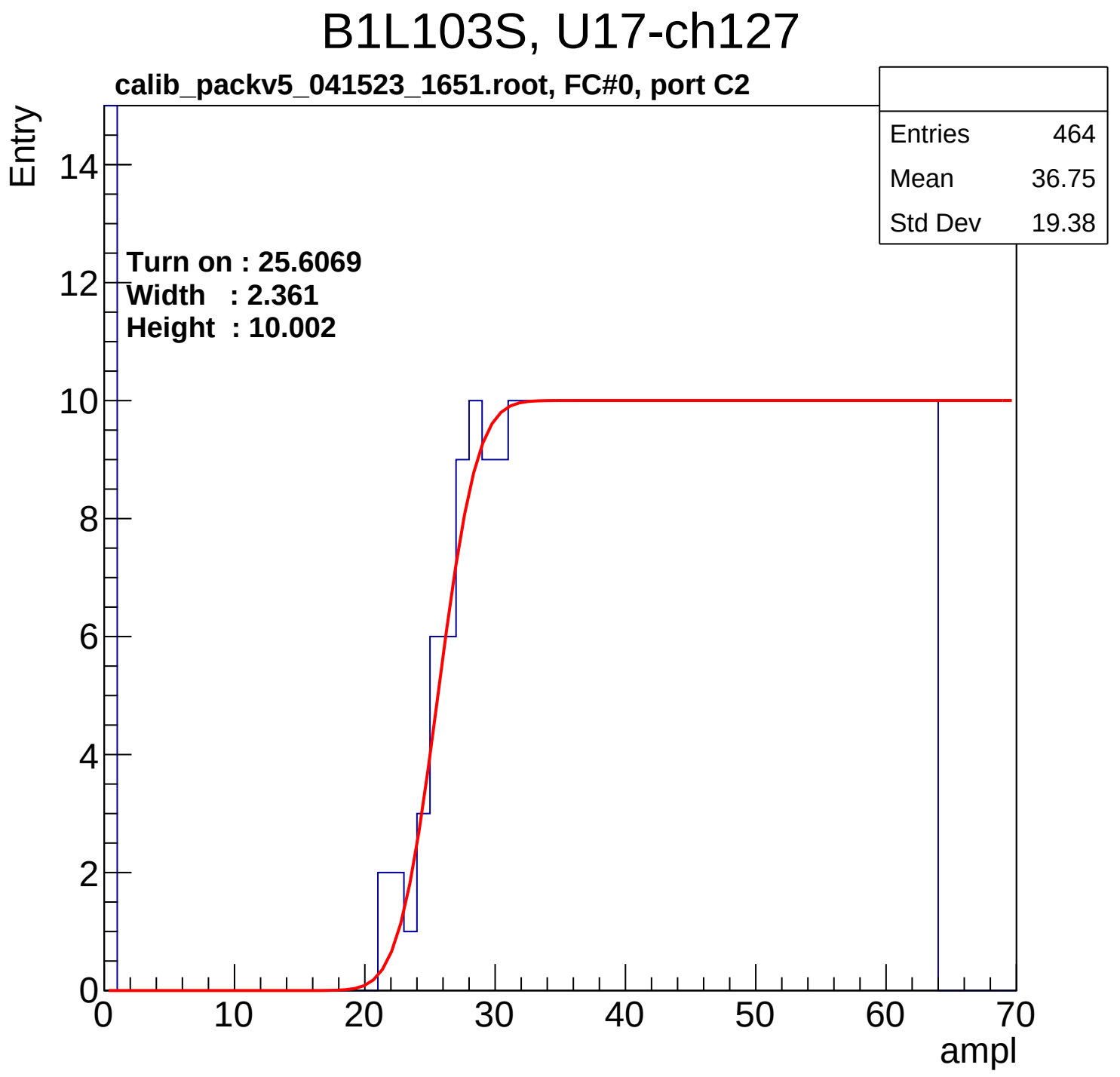
60
70


B1L103S, U17-ch127
calib_packv5_041523_1651.root, FC#0, port C2
Entries 464
Mean 36.75
Std Dev 19.38
Turn on : 25.6069
Width : 2.361
Height : 10.002
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70