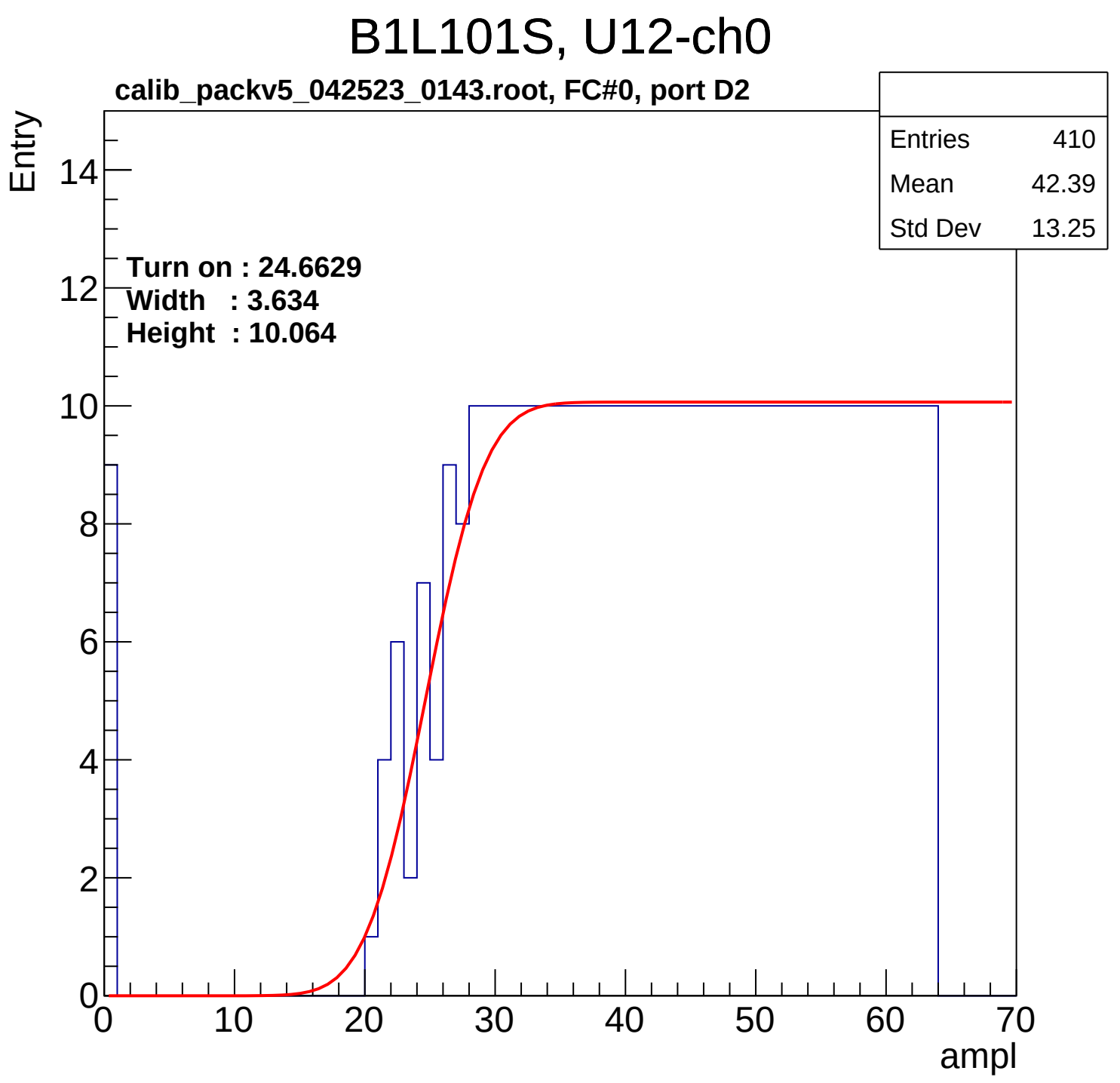
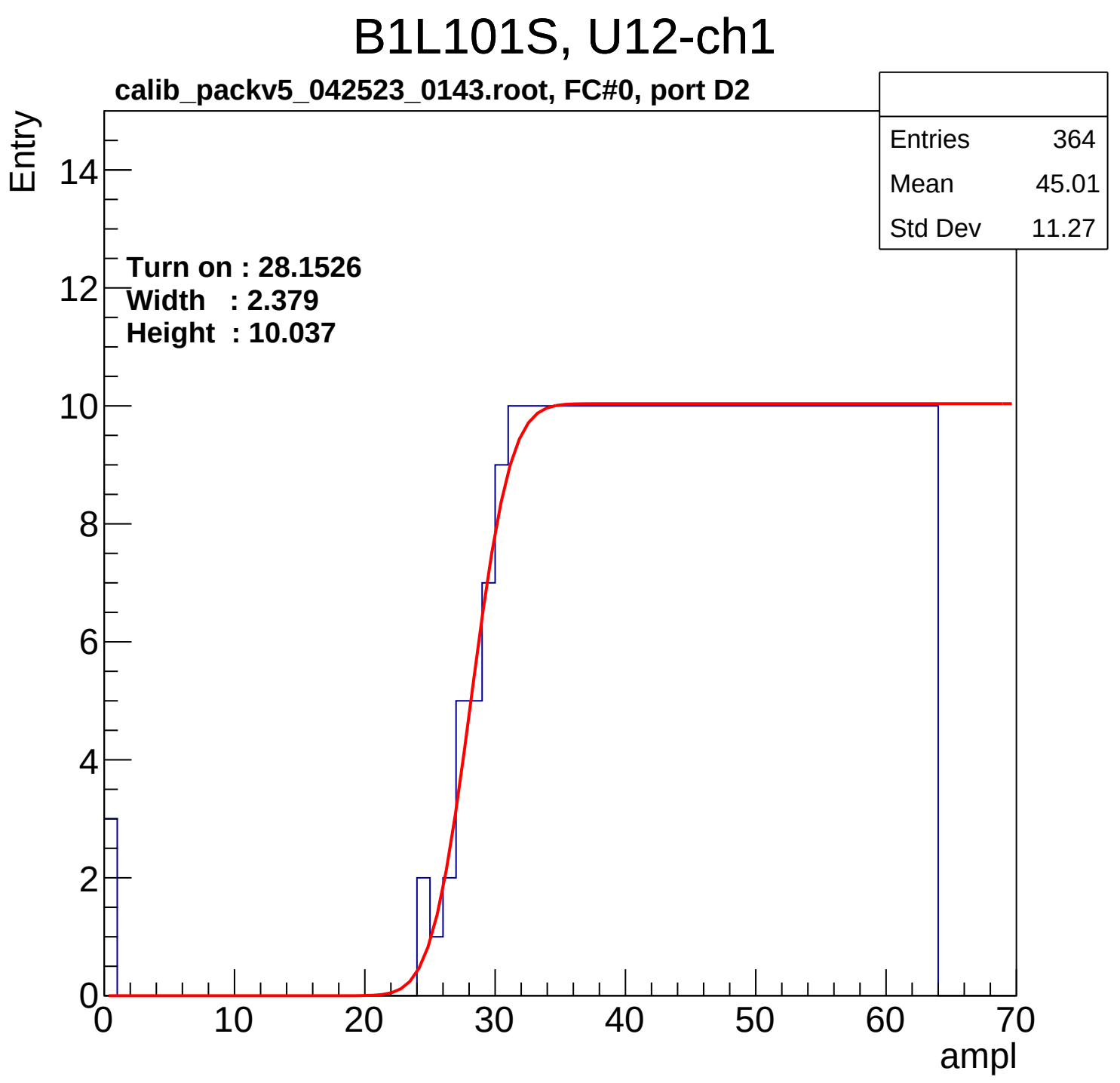
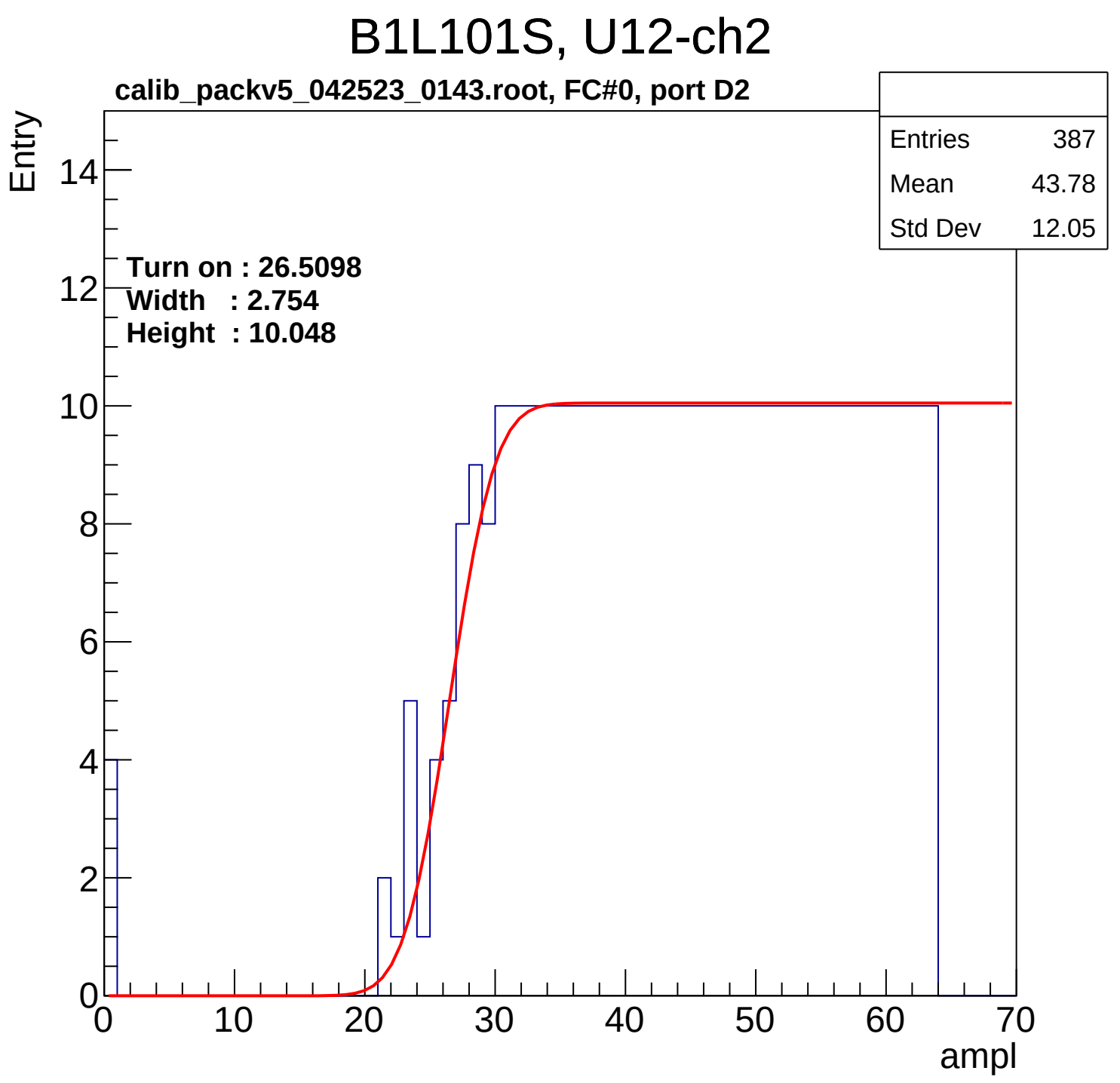
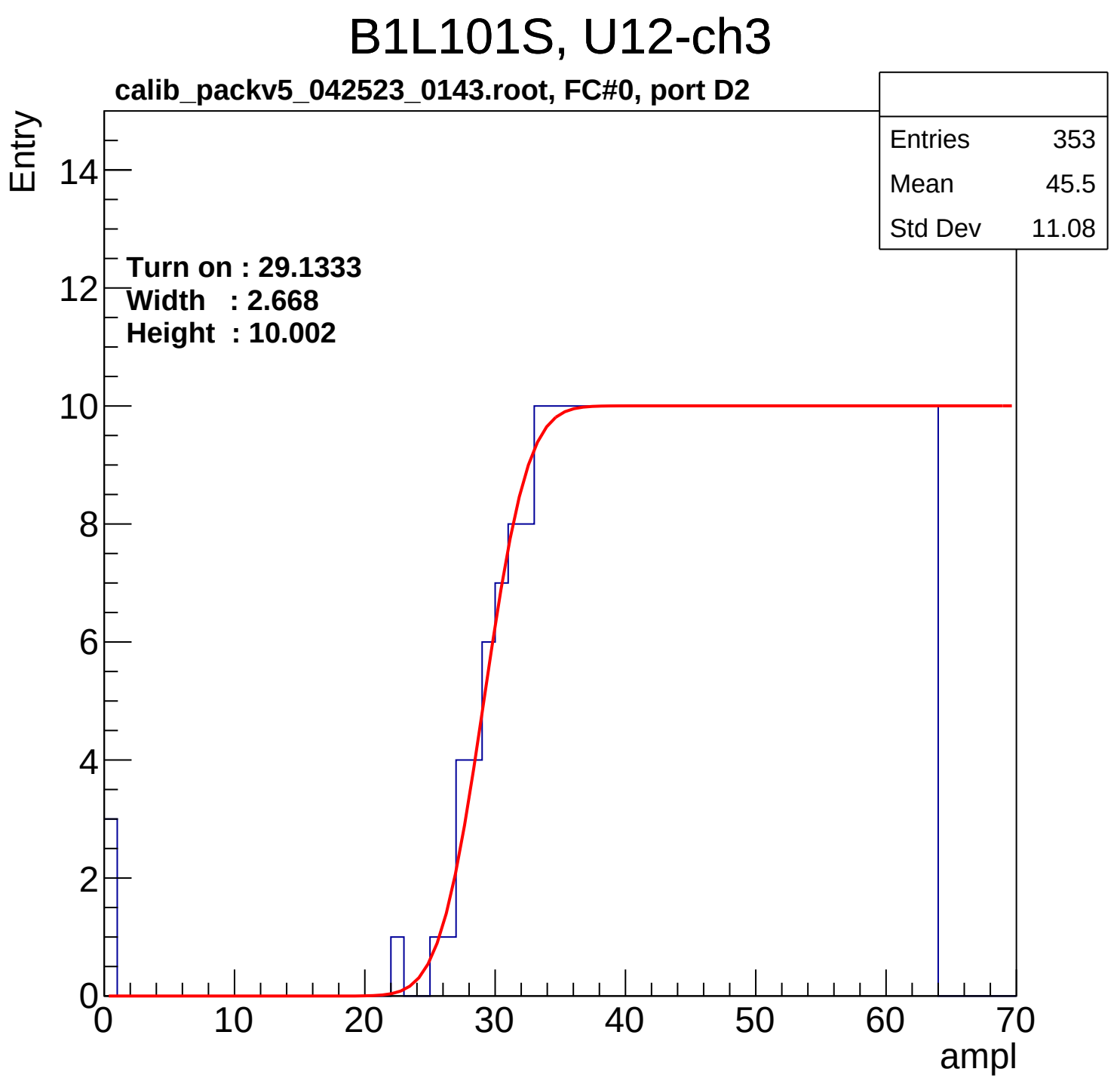
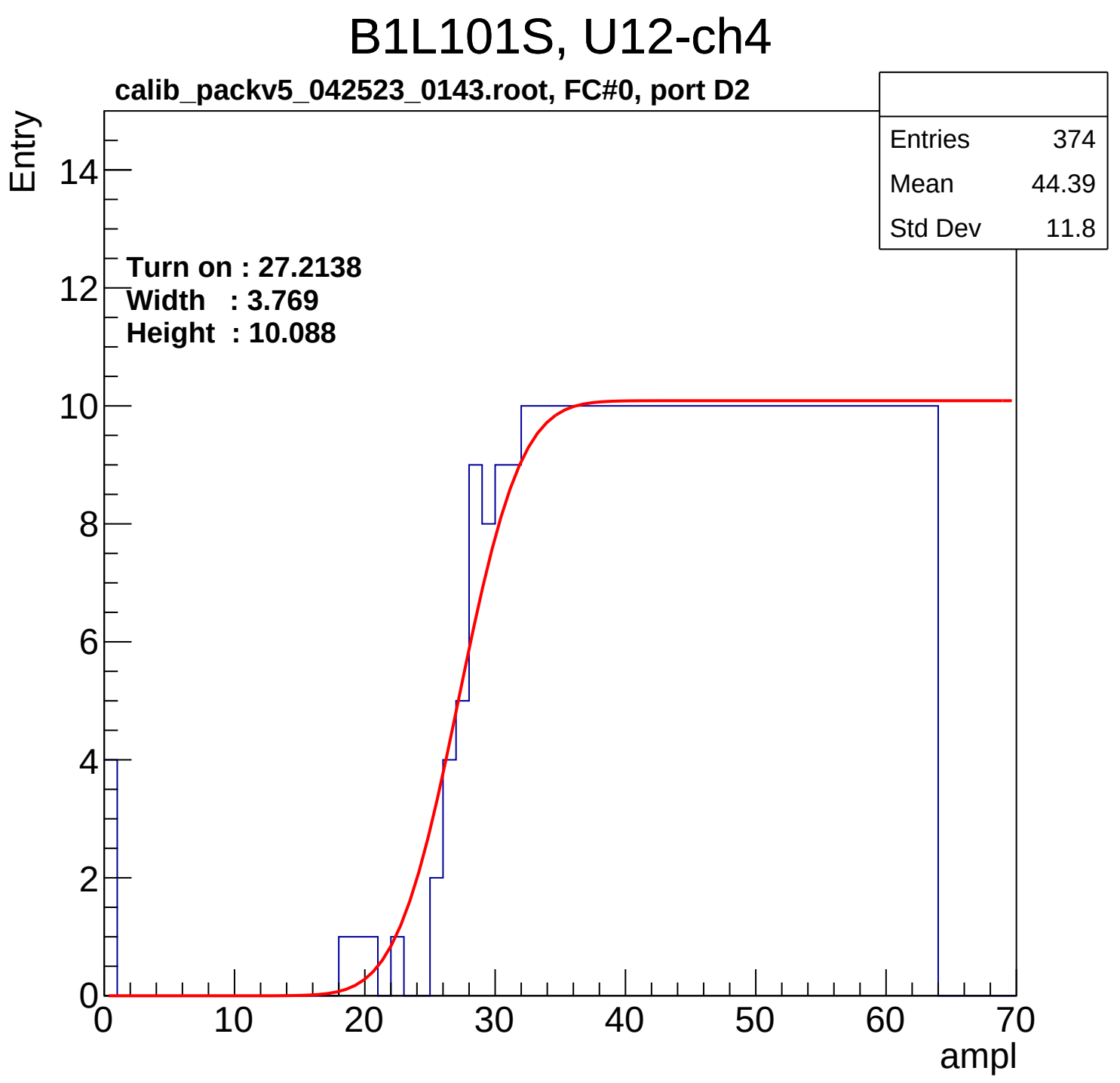
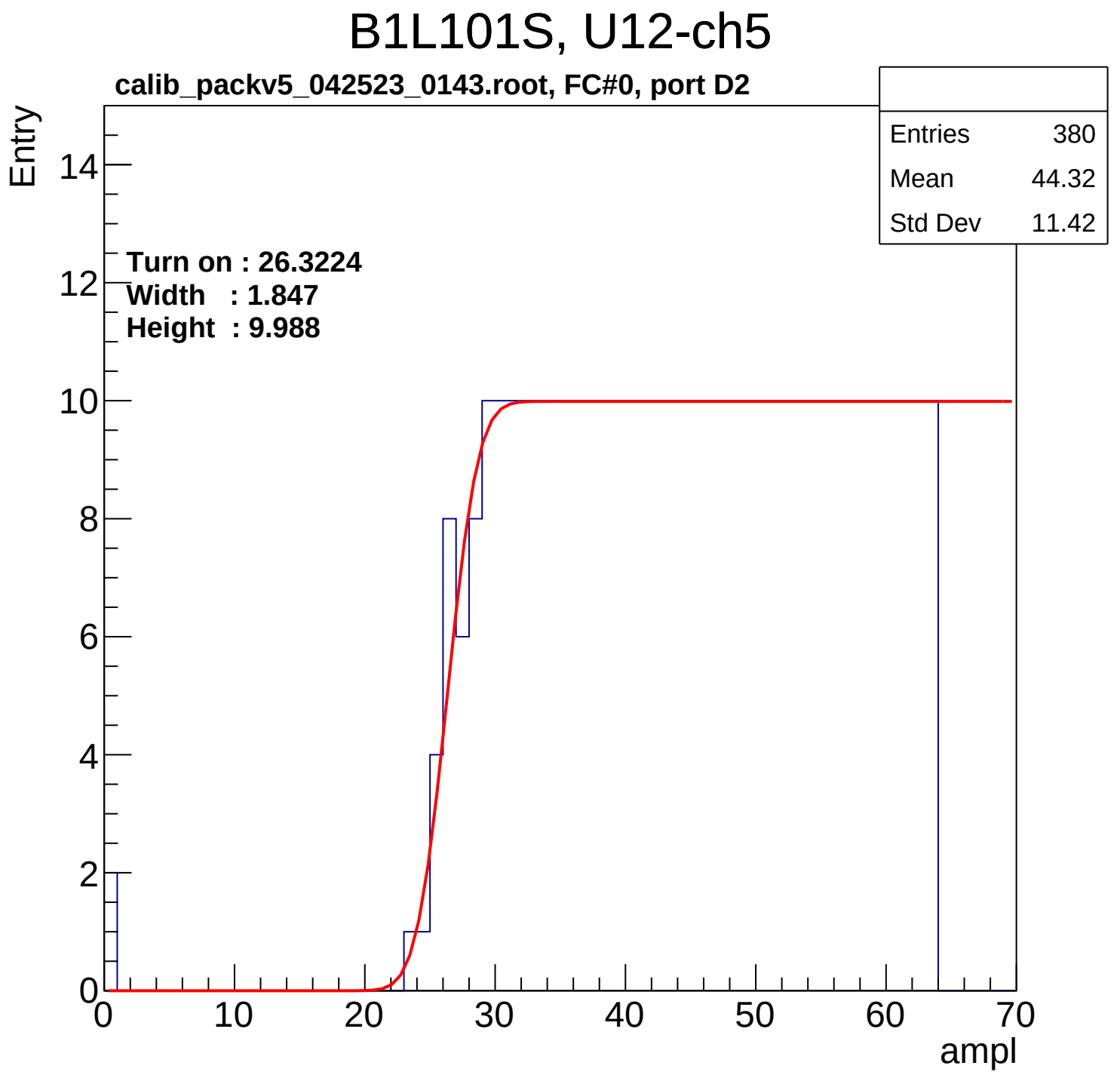

B1L101S, U12-ch0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 410
Mean 42.39
Std Dev 13.25
Turn on : 24.6629
Width : 3.634
Height : 10.064
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

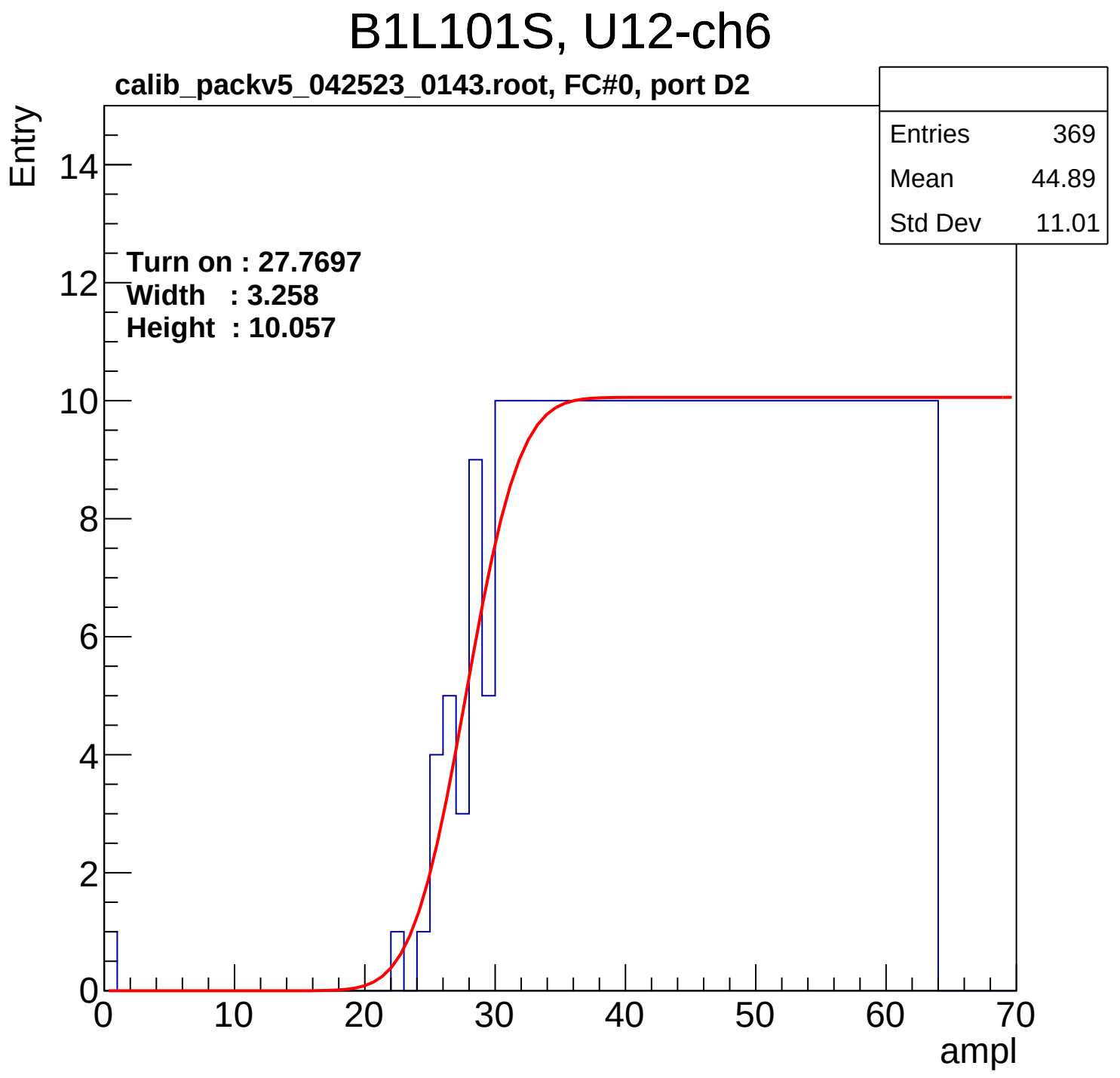

B1L101S, U12-ch1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 364
Mean 45.01
Std Dev 11.27
Turn on : 28.1526
Width : 2.379
Height : 10.037
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

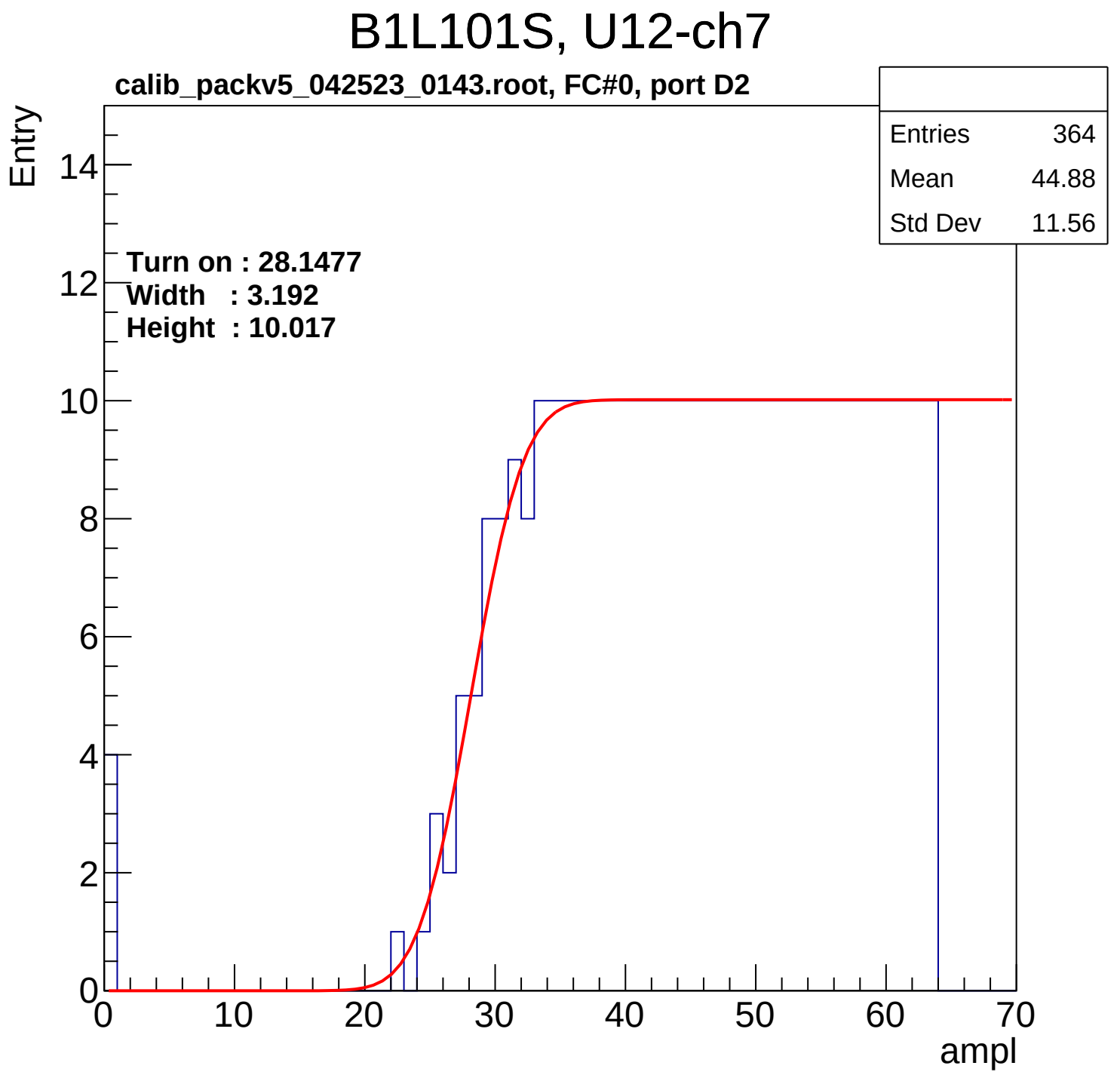

B1L101S, U12-ch2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 387
Mean 43.78
Std Dev 12.05
Turn on : 26.5098
Width : 2.754
Height : 10.048
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

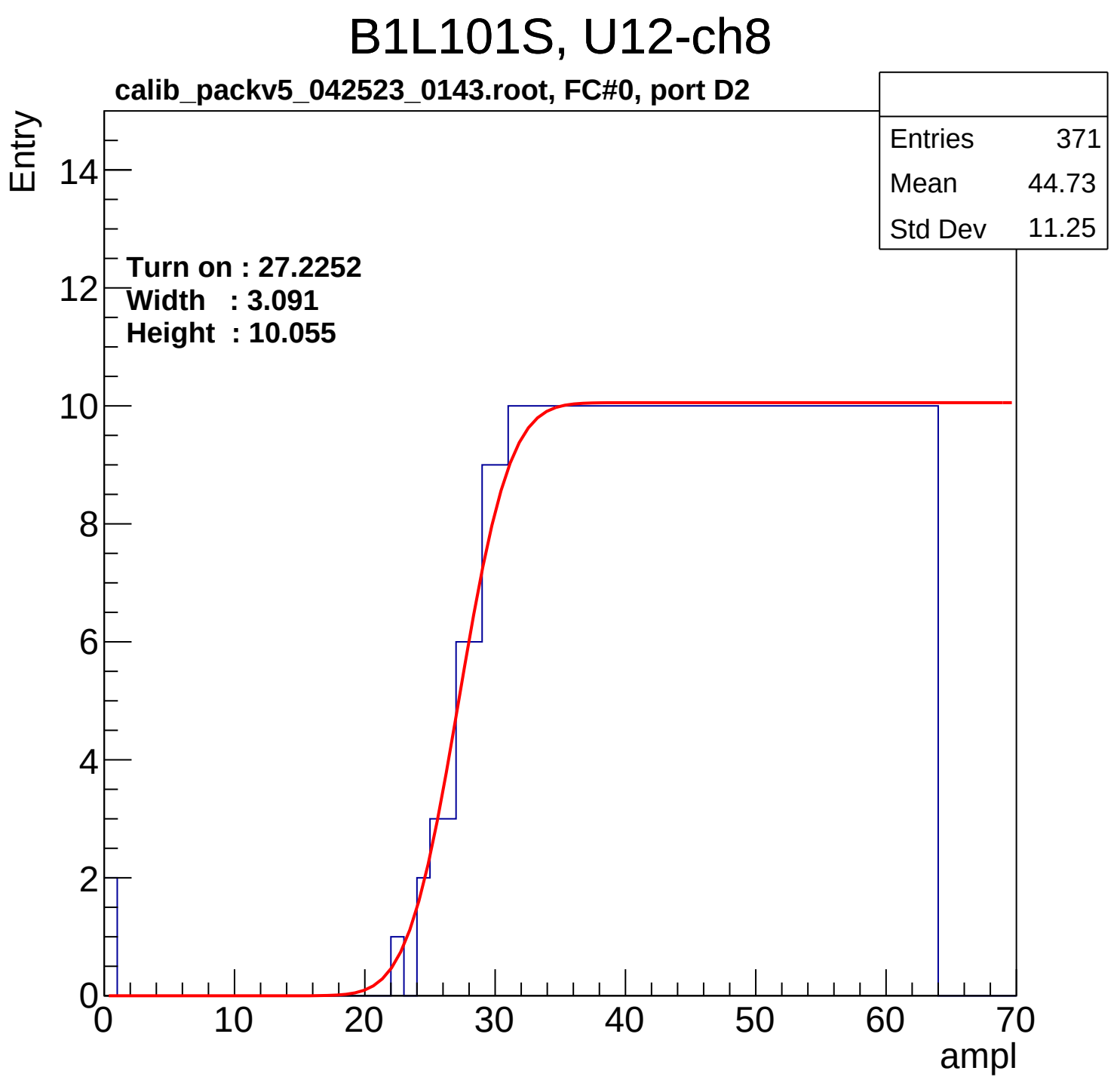

B1L101S, U12-ch3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 353
Mean 45.5
Std Dev 11.08
Turn on : 29.1333
Width : 2.668
Height : 10.002
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

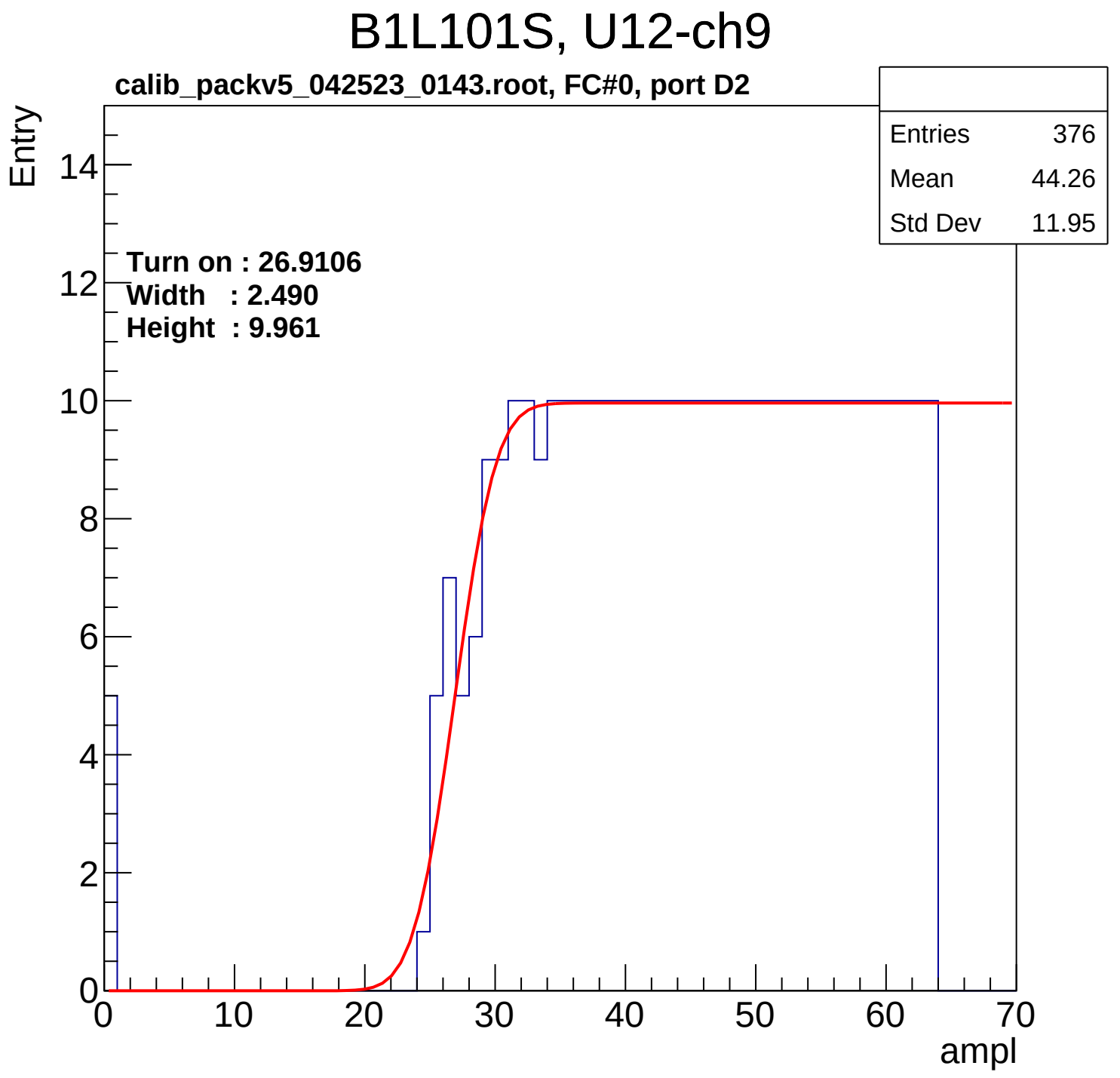

B1L101S, U12-ch4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 374
Mean 44.39
Std Dev 11.8
Turn on : 27.2138
Width : 3.769
Height : 10.088
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

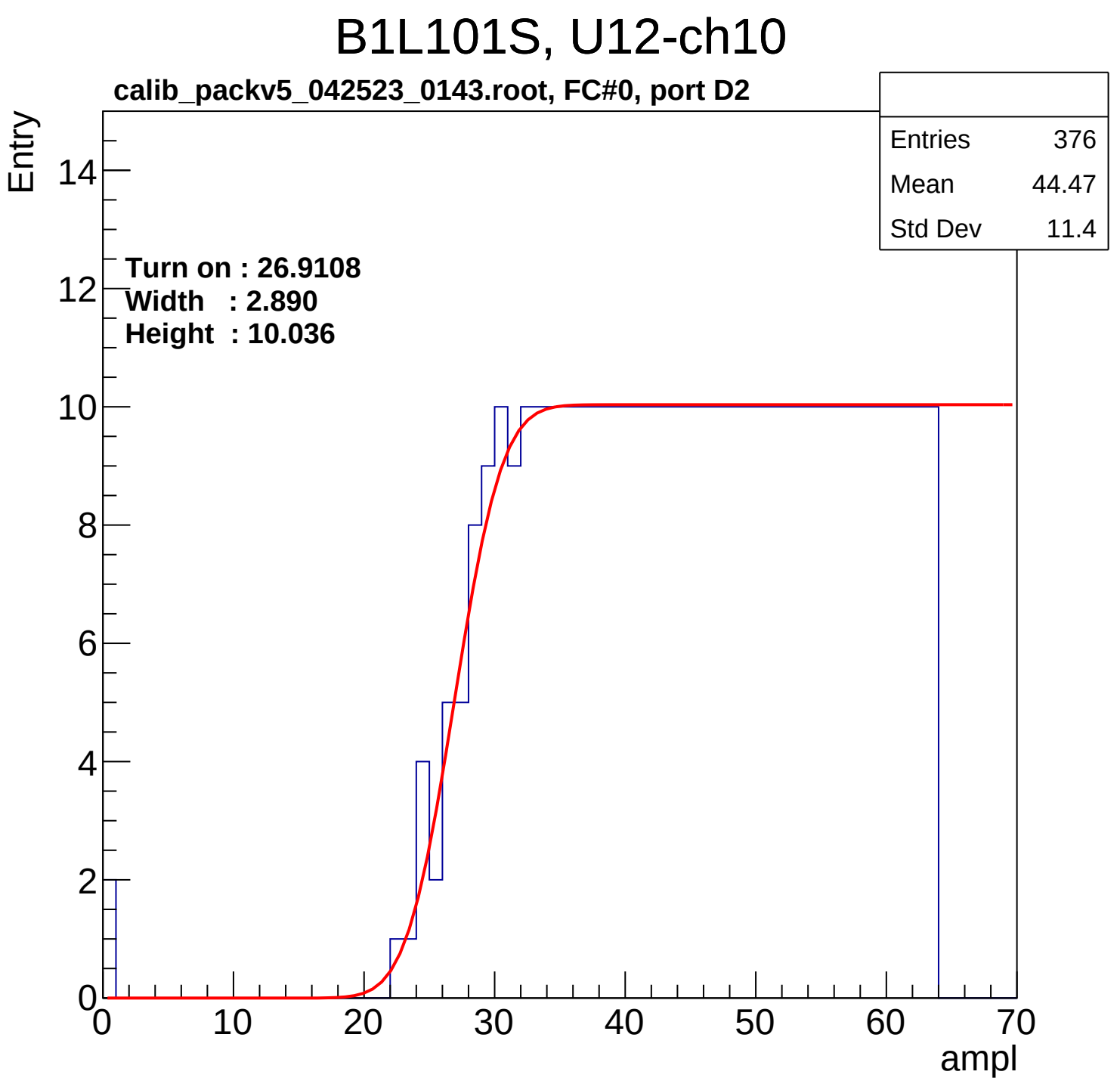

B1L101S, U12-ch5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 380
Mean 44.32
Std Dev 11.42
Turn on : 26.3224
Width : 1.847
Height : 9.988
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

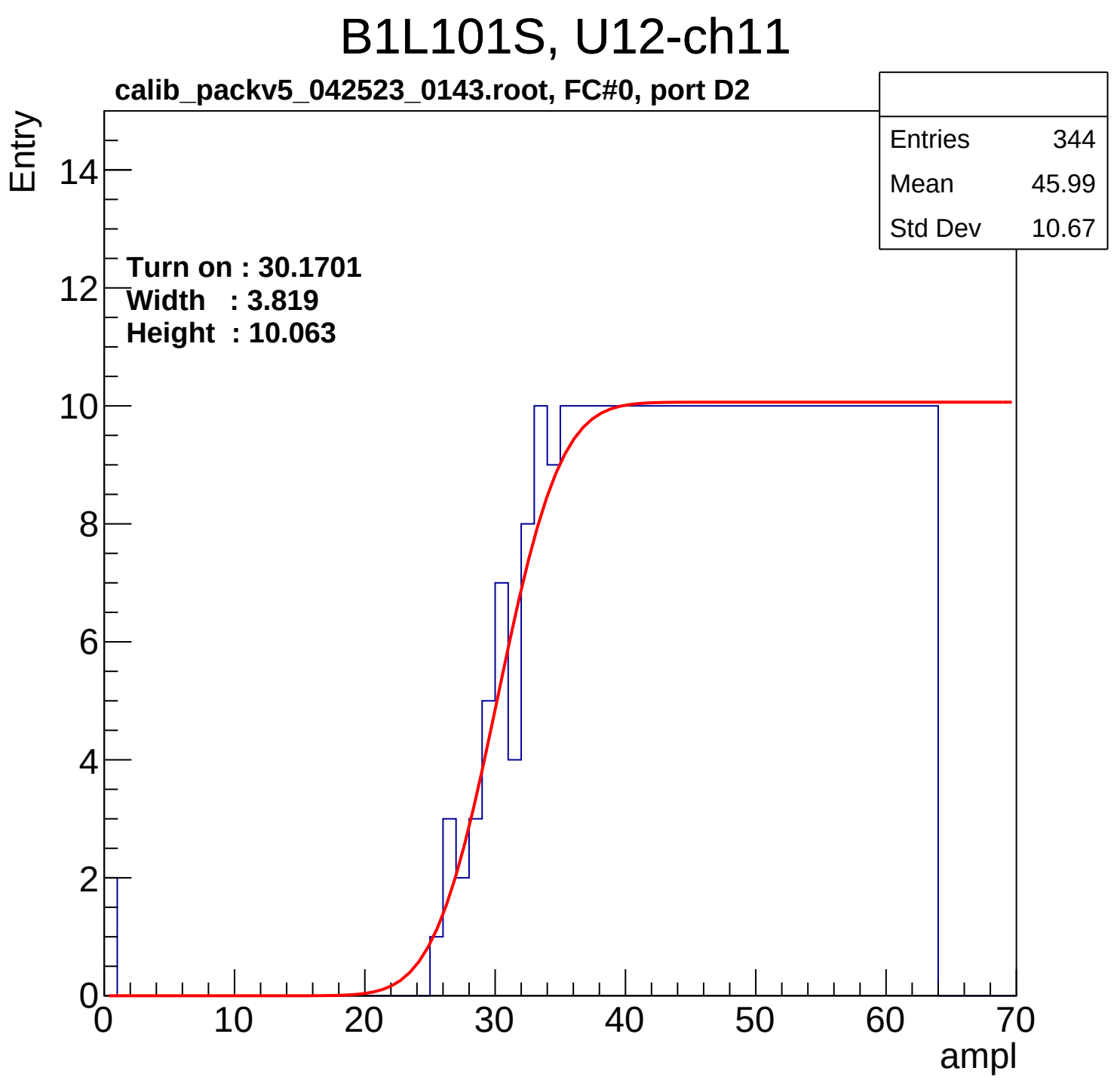

B1L101S, U12-ch6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 369
Mean 44.89
Std Dev 11.01
Turn on : 27.7697
Width : 3.258
Height : 10.057
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

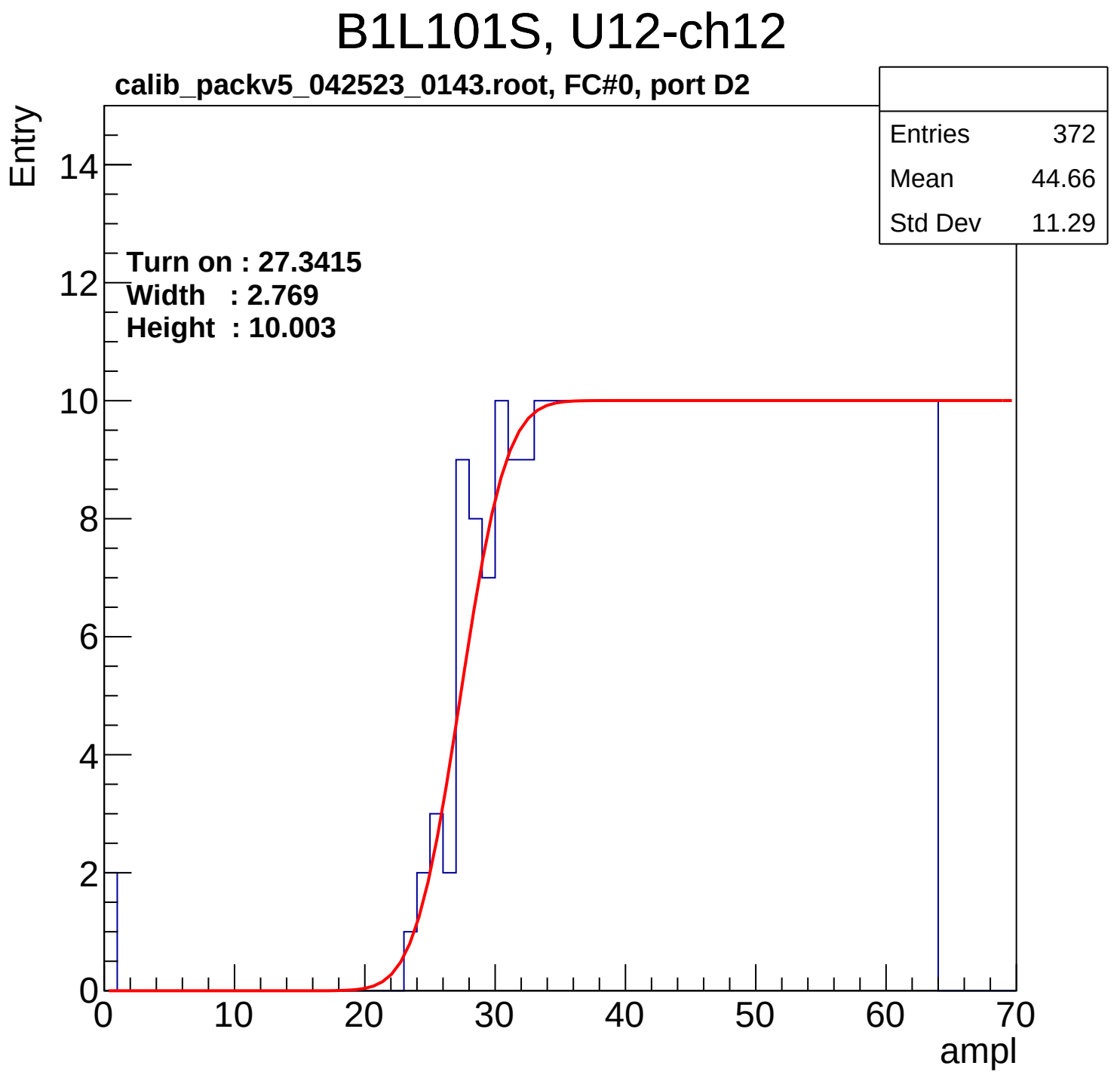

B1L101S, U12-ch7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 364
Mean 44.88
Std Dev 11.56
Turn on : 28.1477
Width : 3.192
Height : 10.017
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

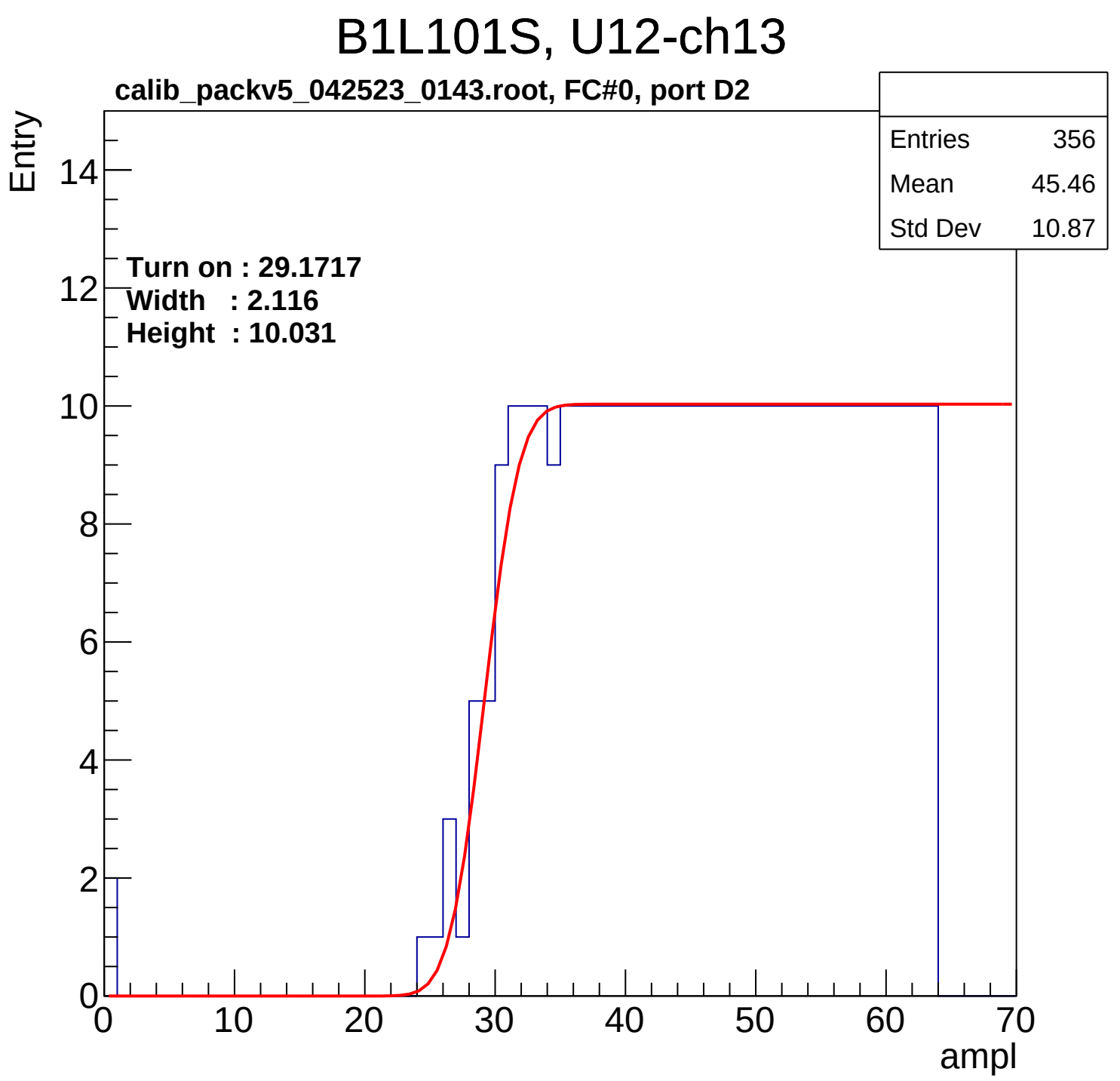

B1L101S, U12-ch8
calib_packv5_042523_0143.root, FC#0, port D2
Entries 371
Mean 44.73
Std Dev 11.25
Turn on : 27.2252
Width : 3.091
Height : 10.055
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

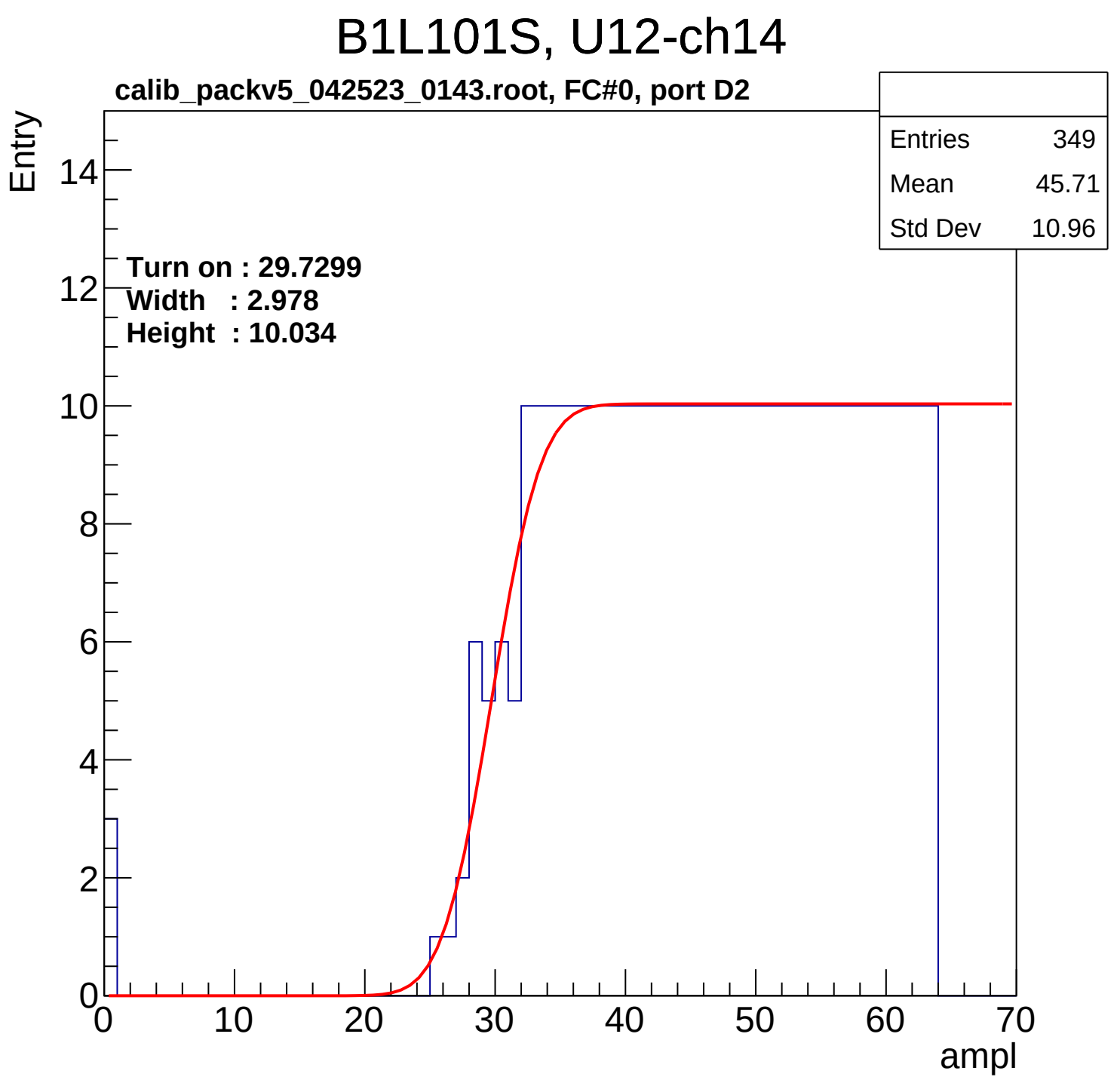

B1L101S, U12-ch9
calib_packv5_042523_0143.root, FC#0, port D2
Entries 376
Mean 44.26
Std Dev 11.95
Turn on : 26.9106
Width : 2.490
Height : 9.961
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

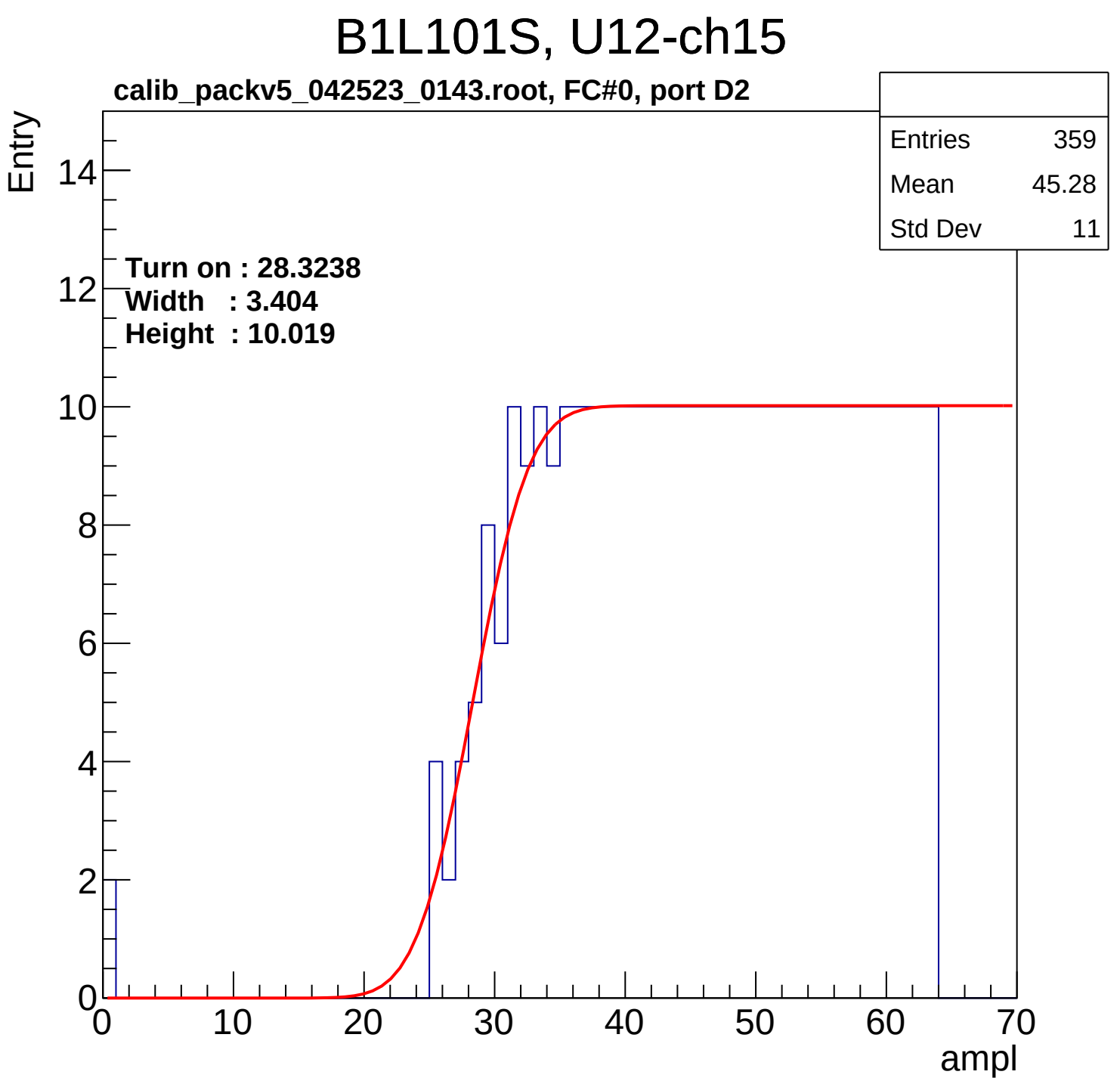

B1L101S, U12-ch10
calib_packv5_042523_0143.root, FC#0, port D2
Entries 376
Mean 44.47
Std Dev 11.4
Turn on : 26.9108
Width : 2.890
Height : 10.036
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

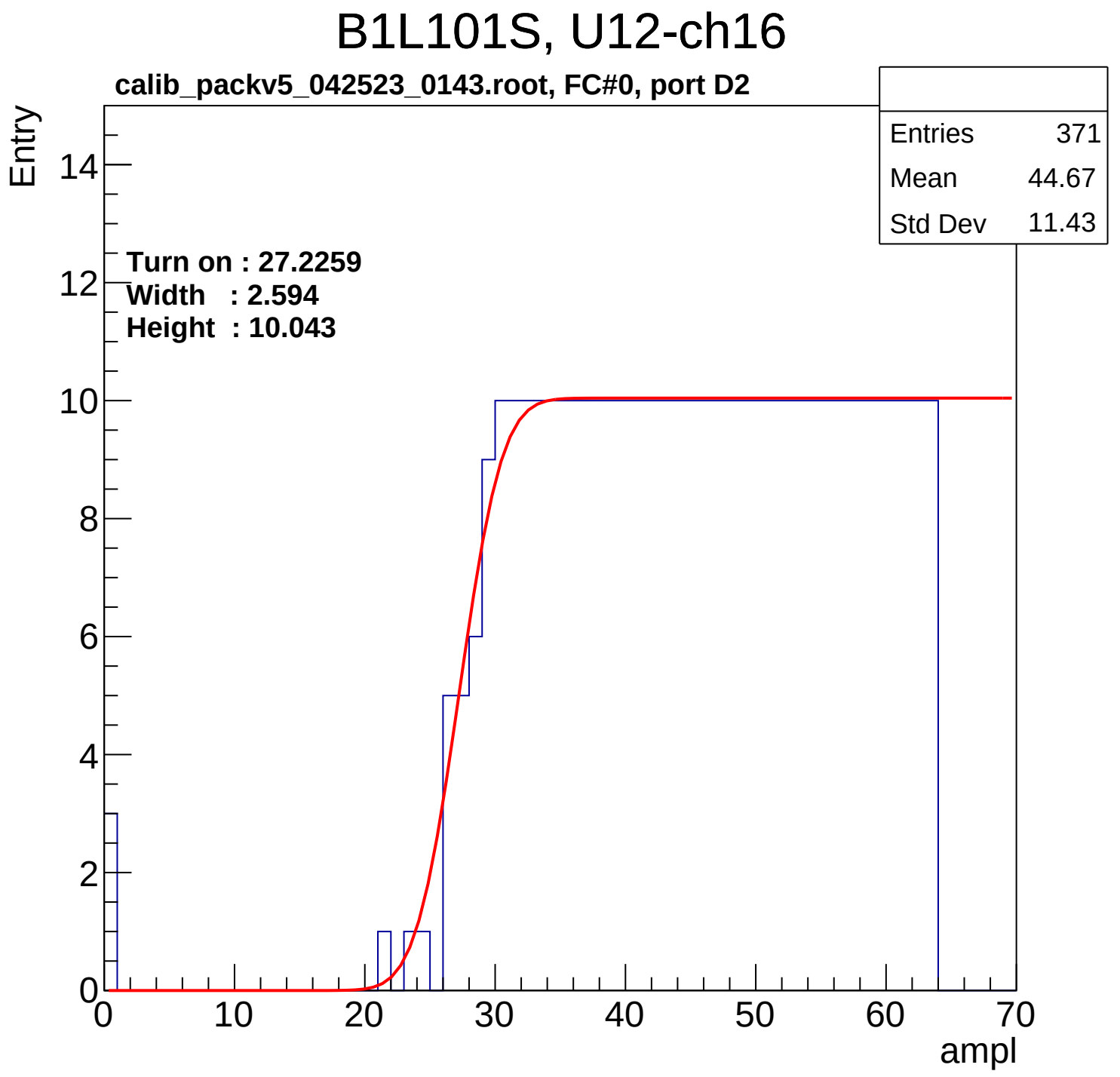

B1L101S, U12-ch11
calib_packv5_042523_0143.root, FC#0, port D2
Entries 344
Mean 45.99
Std Dev 10.67
Turn on : 30.1701
Width : 3.819
Height : 10.063
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

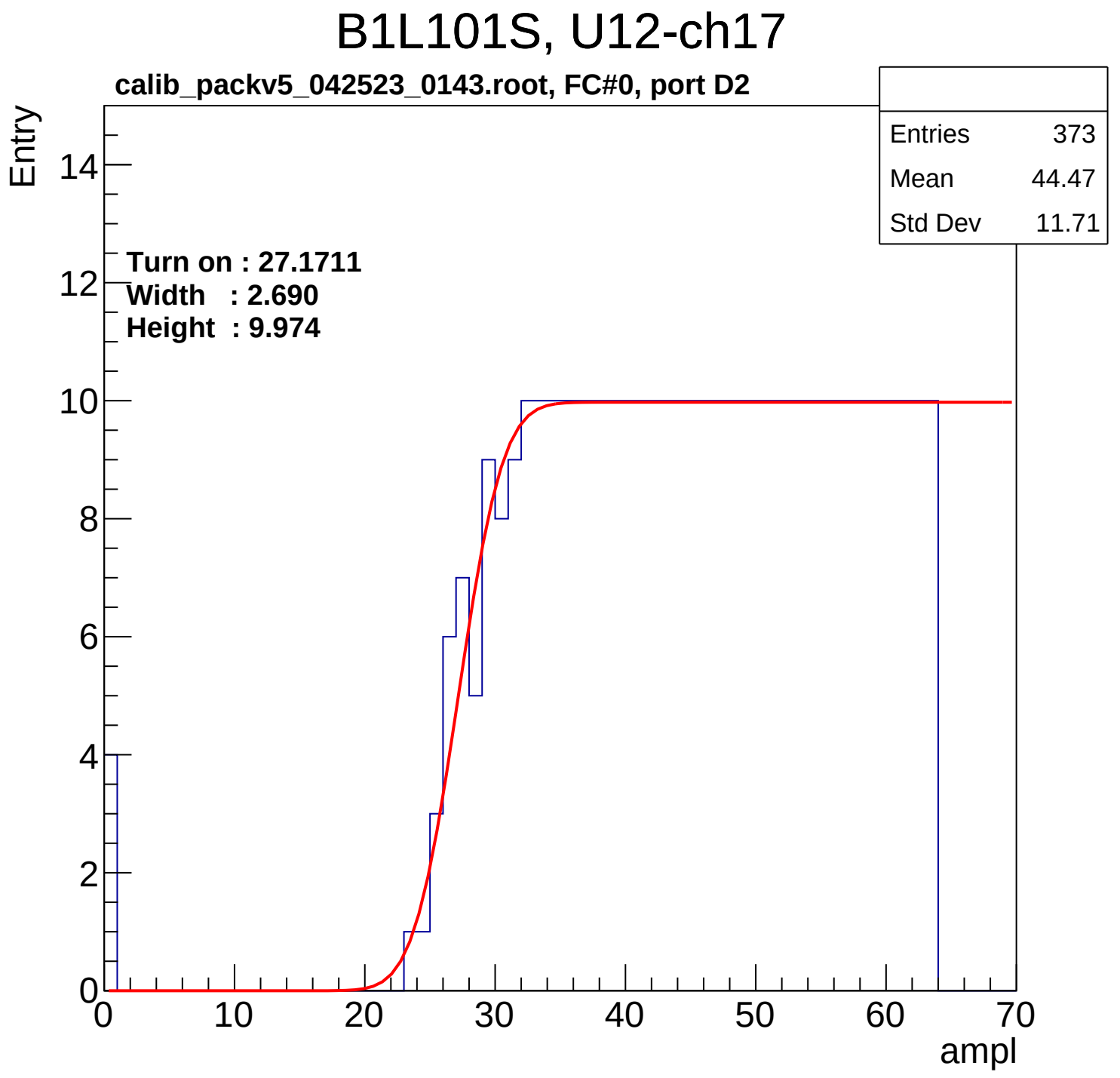

B1L101S, U12-ch12
calib_packv5_042523_0143.root, FC#0, port D2
Entries 372
Mean 44.66
Std Dev 11.29
Turn on : 27.3415
Width : 2.769
Height : 10.003
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

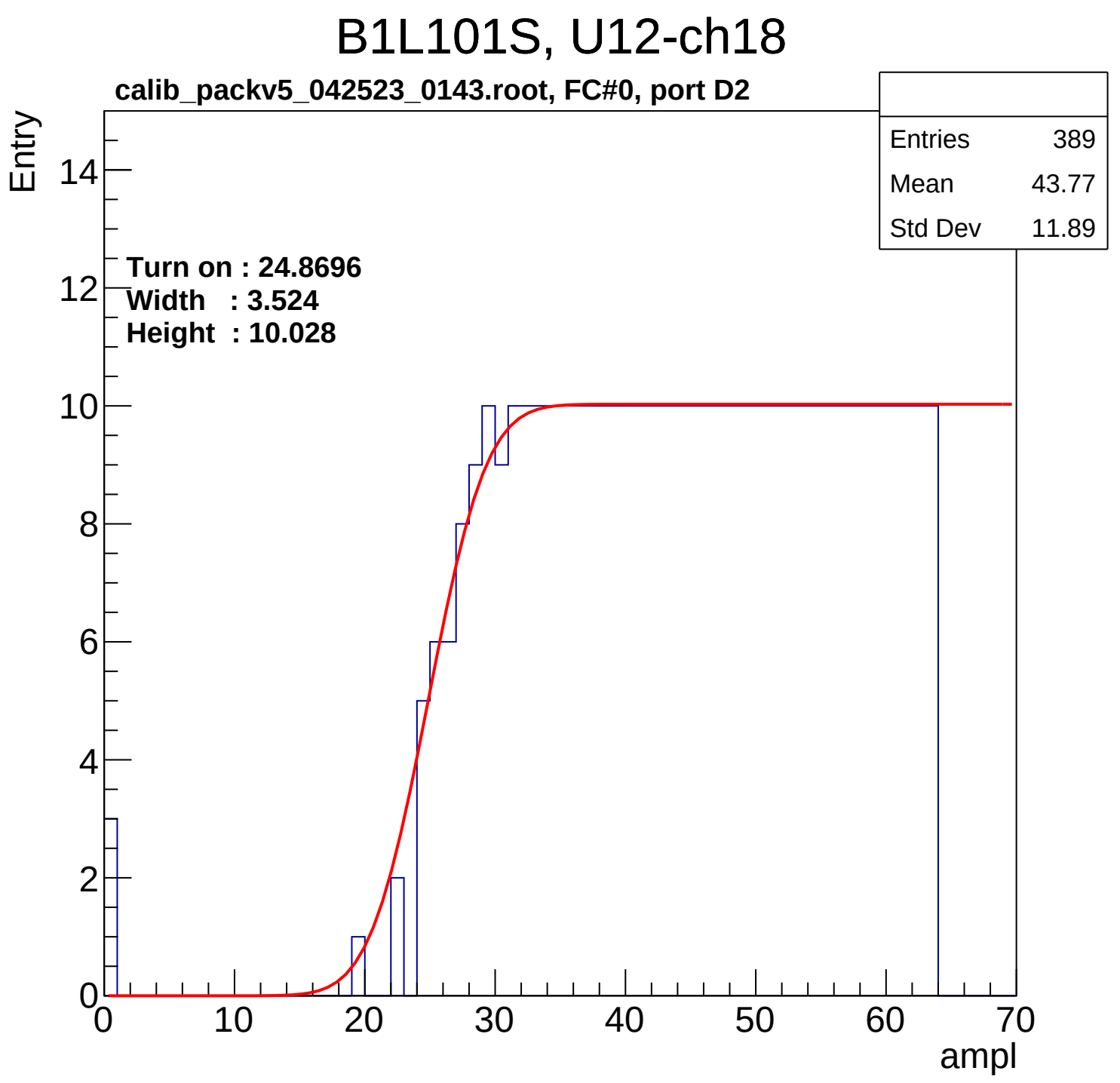

B1L101S, U12-ch13
calib_packv5_042523_0143.root, FC#0, port D2
Entries 356
Mean 45.46
Std Dev 10.87
Turn on : 29.1717
Width : 2.116
Height : 10.031
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

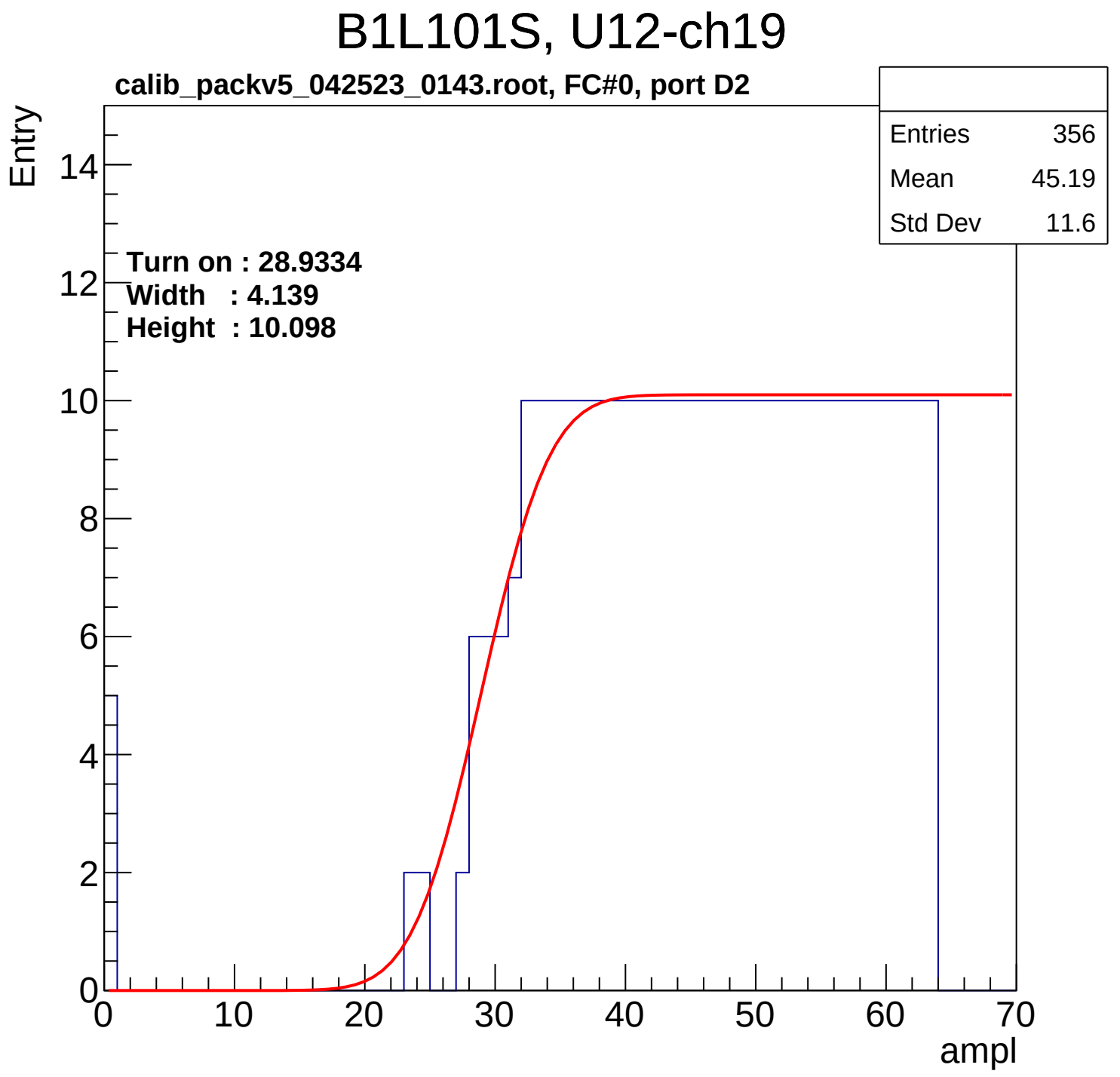

B1L101S, U12-ch14
calib_packv5_042523_0143.root, FC#0, port D2
Entries 349
Mean 45.71
Std Dev 10.96
Turn on : 29.7299
Width : 2.978
Height : 10.034
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

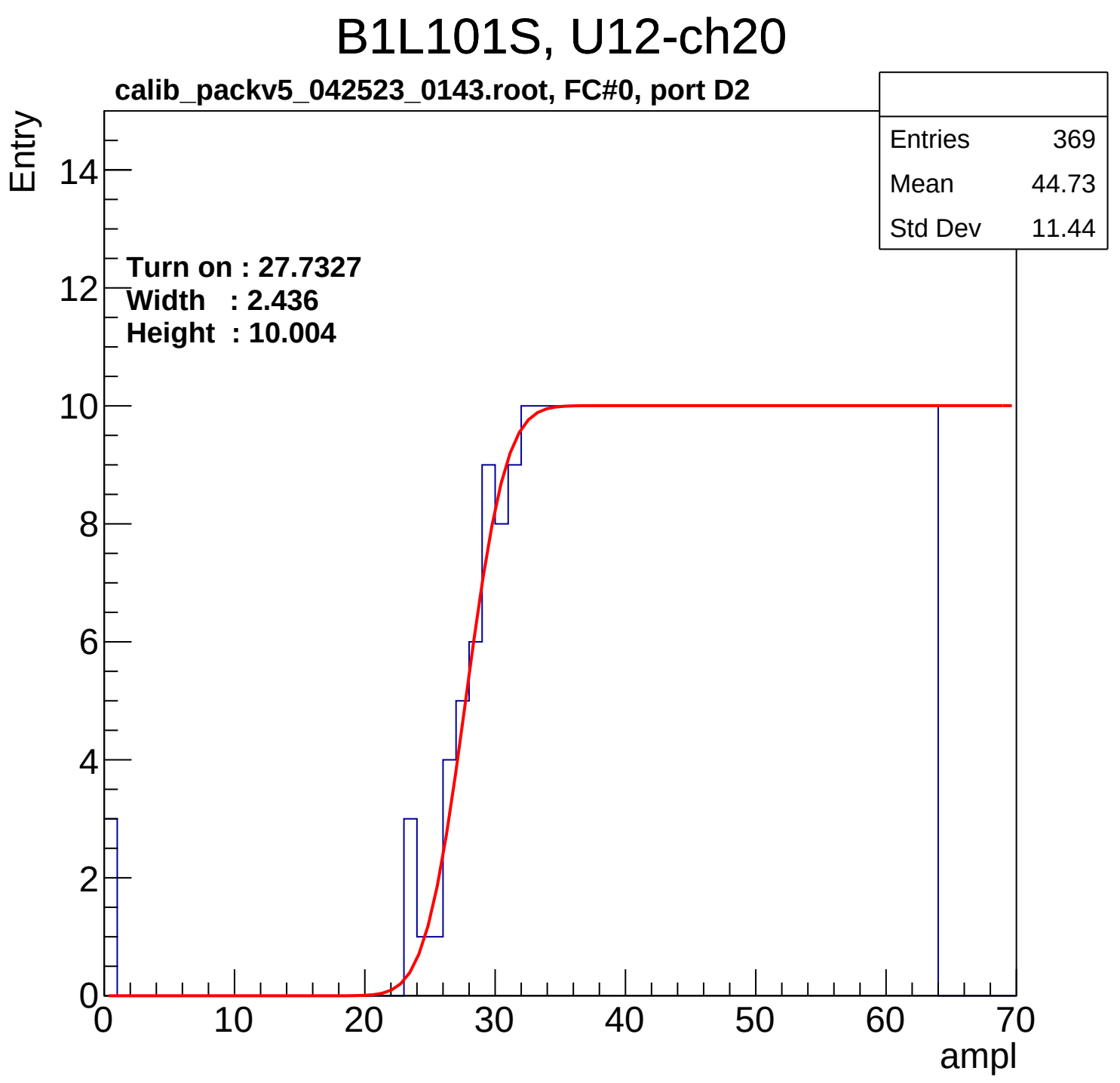

B1L101S, U12-ch15
calib_packv5_042523_0143.root, FC#0, port D2
Entries 359
Mean 45.28
Std Dev 11
Turn on : 28.3238
Width : 3.404
Height : 10.019
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

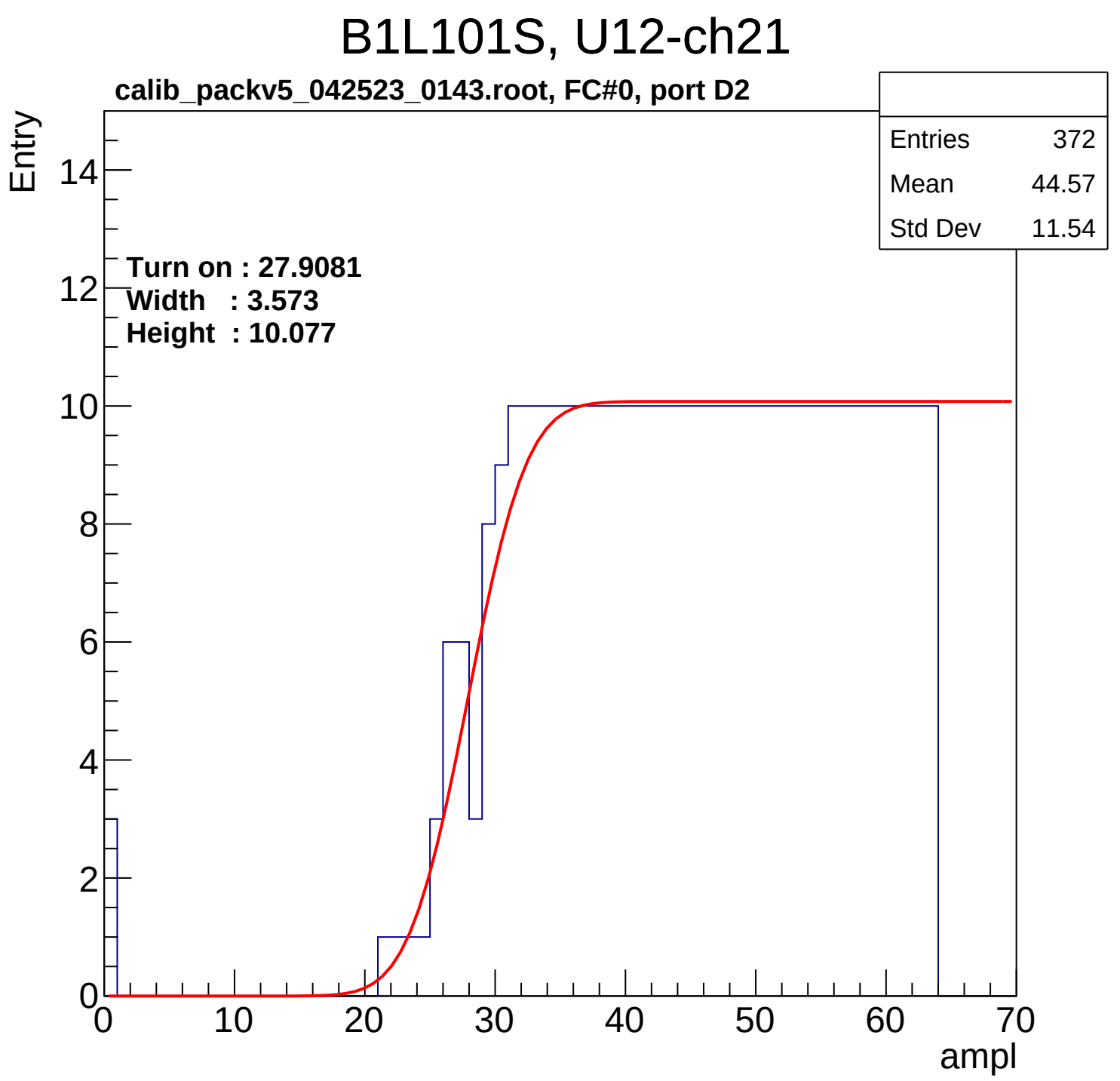

B1L101S, U12-ch16
calib_packv5_042523_0143.root, FC#0, port D2
Entries 371
Mean 44.67
Std Dev 11.43
Turn on : 27.2259
Width : 2.594
Height : 10.043
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

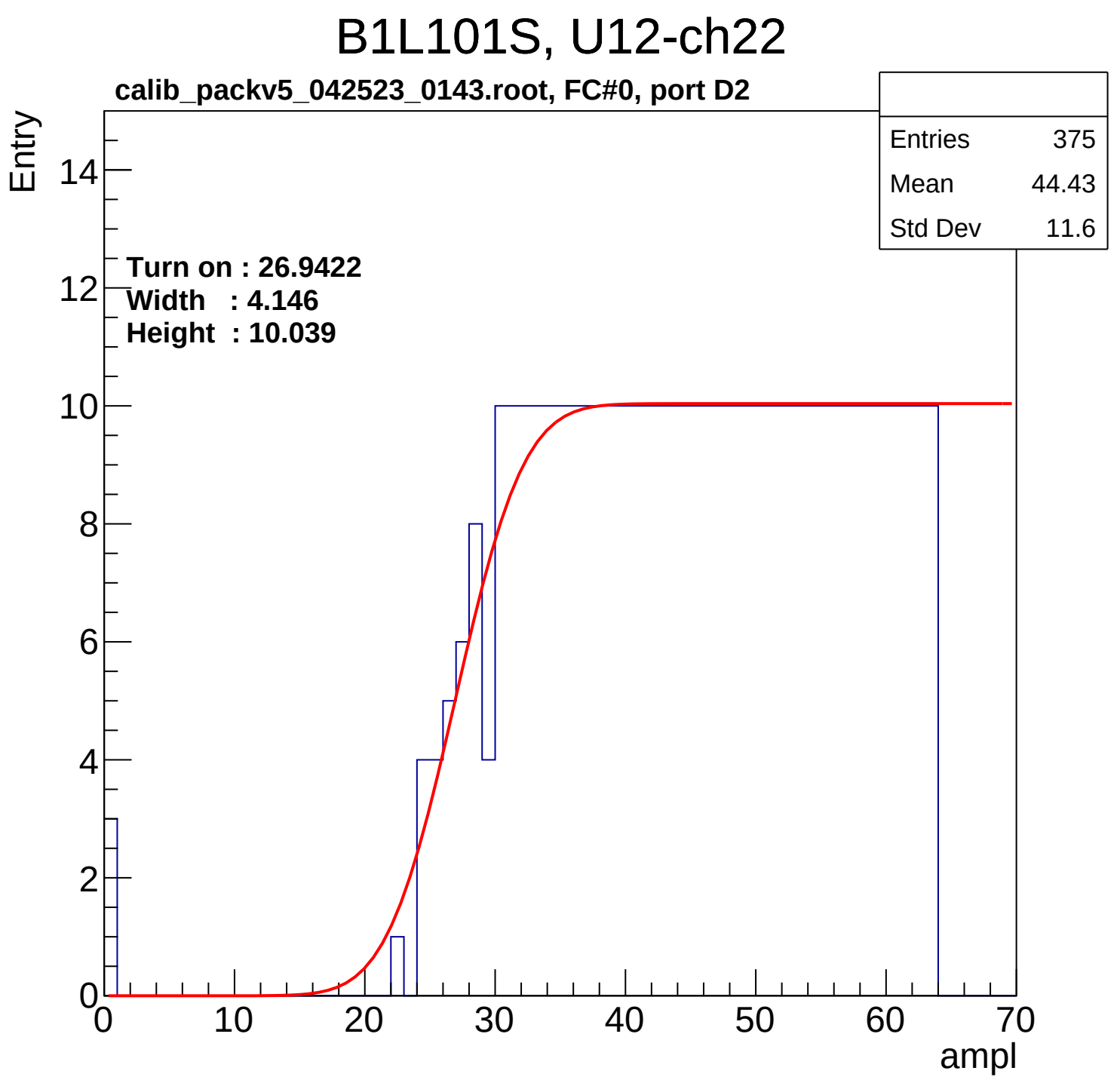

B1L101S, U12-ch17
calib_packv5_042523_0143.root, FC#0, port D2
Entries 373
Mean 44.47
Std Dev 11.71
Turn on : 27.1711
Width : 2.690
Height : 9.974
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

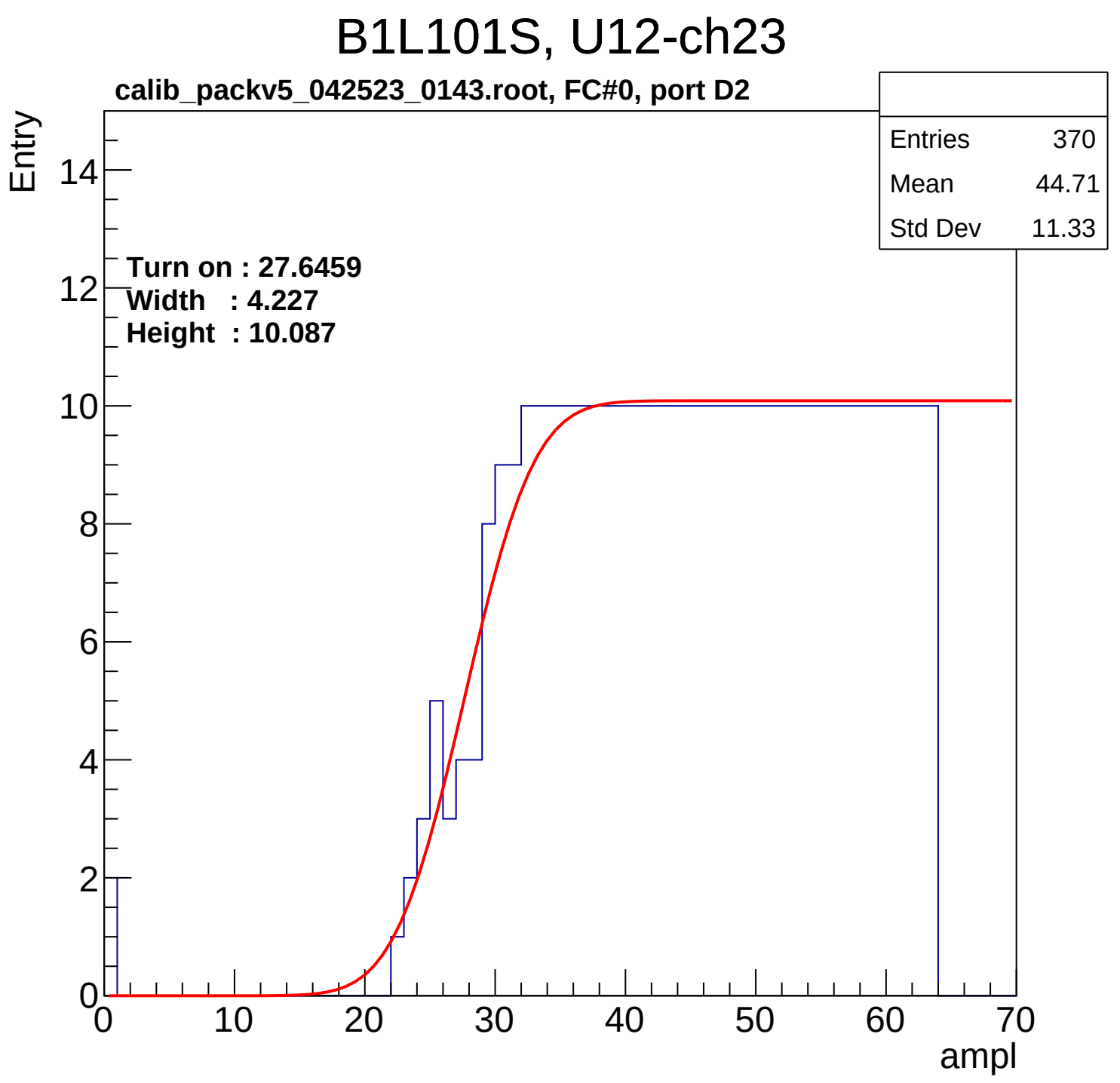

B1L101S, U12-ch18
calib_packv5_042523_0143.root, FC#0, port D2
Entries 389
Mean 43.77
Std Dev 11.89
Turn on : 24.8696
Width : 3.524
Height : 10.028
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

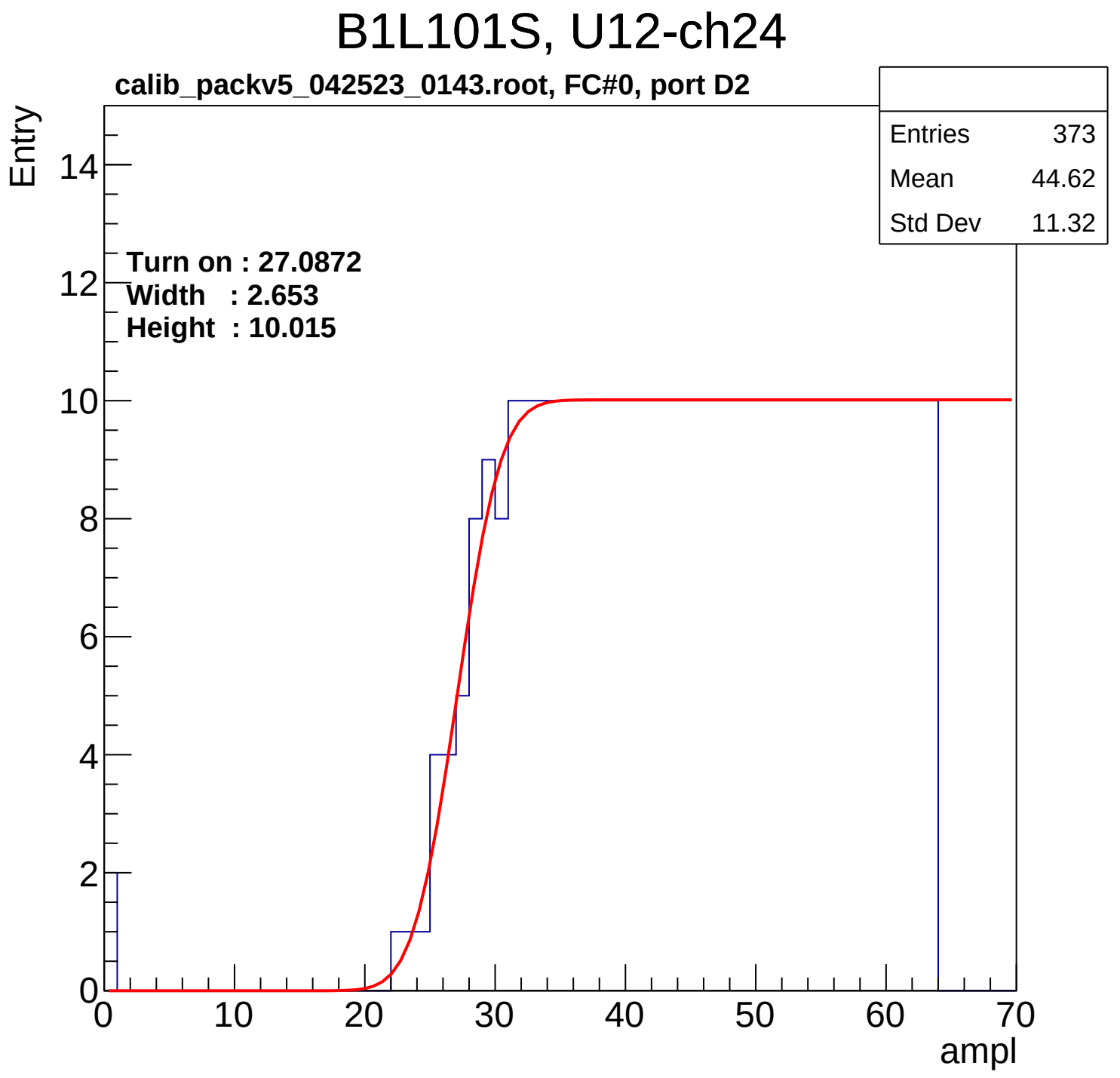

B1L101S, U12-ch19
calib_packv5_042523_0143.root, FC#0, port D2
Entries 356
Mean 45.19
Std Dev 11.6
Turn on : 28.9334
Width : 4.139
Height : 10.098
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

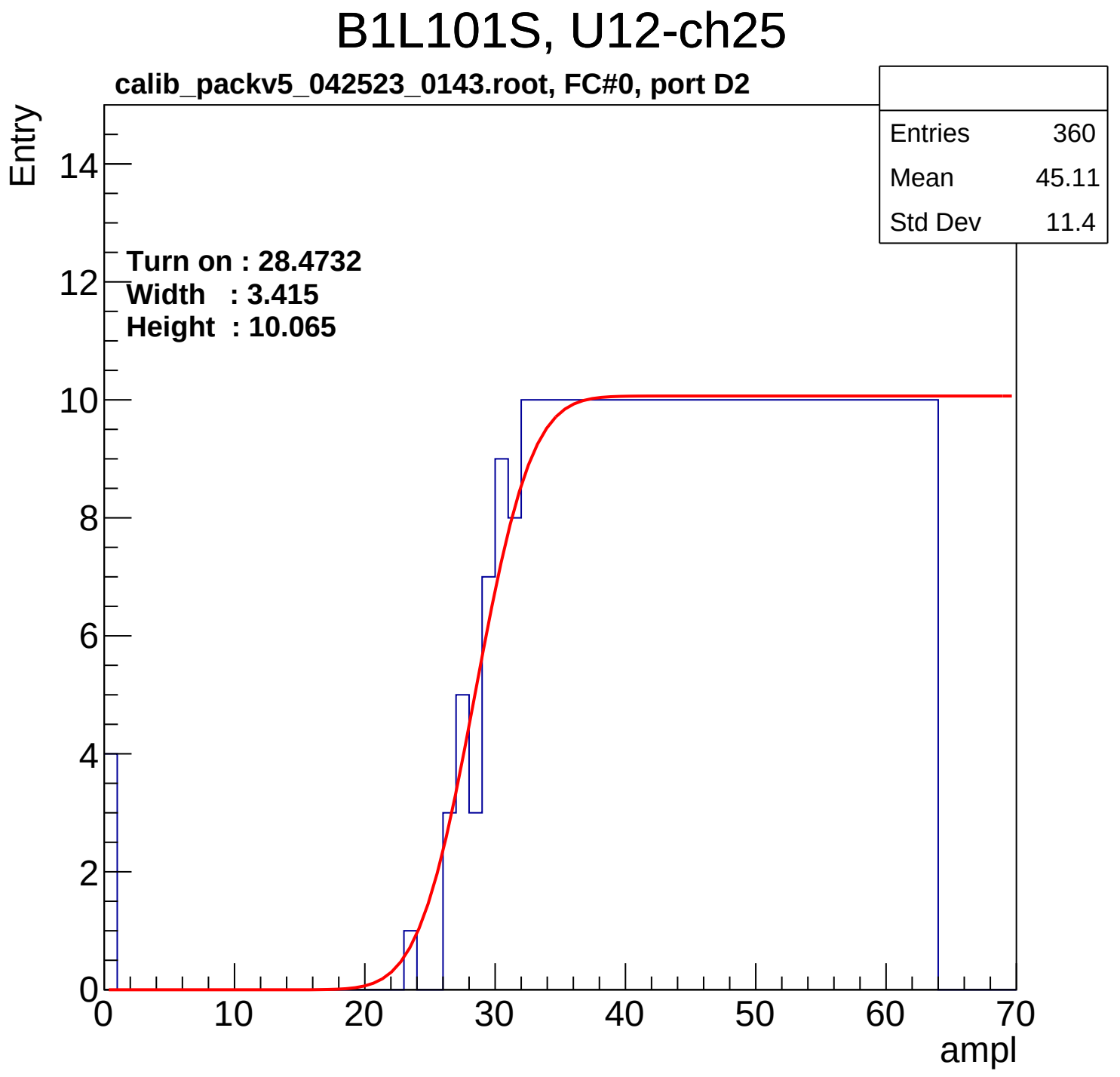

B1L101S, U12-ch20
calib_packv5_042523_0143.root, FC#0, port D2
Entries 369
Mean 44.73
Std Dev 11.44
Turn on : 27.7327
Width : 2.436
Height : 10.004
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

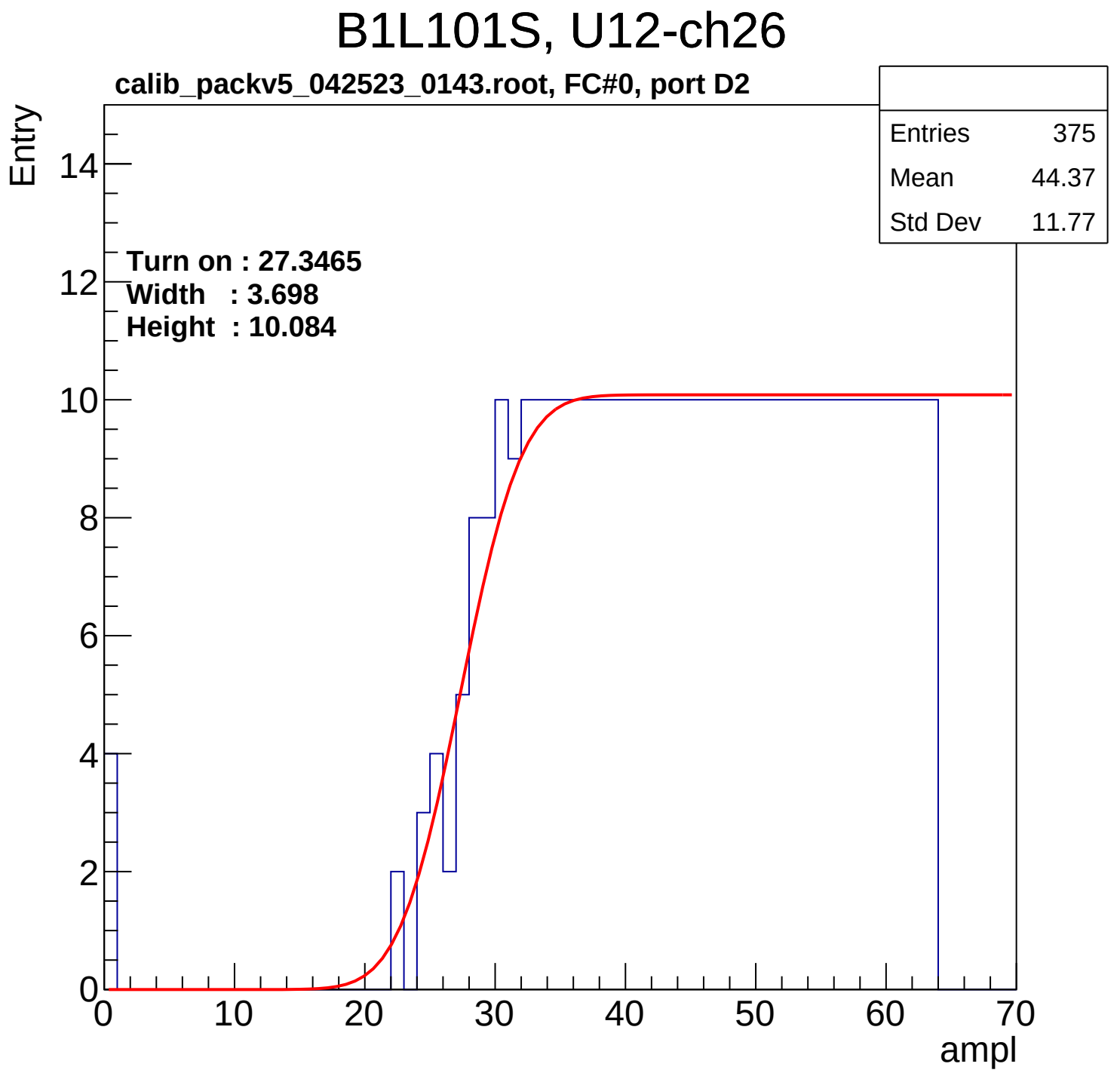

B1L101S, U12-ch21
calib_packv5_042523_0143.root, FC#0, port D2
Entries 372
Mean 44.57
Std Dev 11.54
Turn on : 27.9081
Width : 3.573
Height : 10.077
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

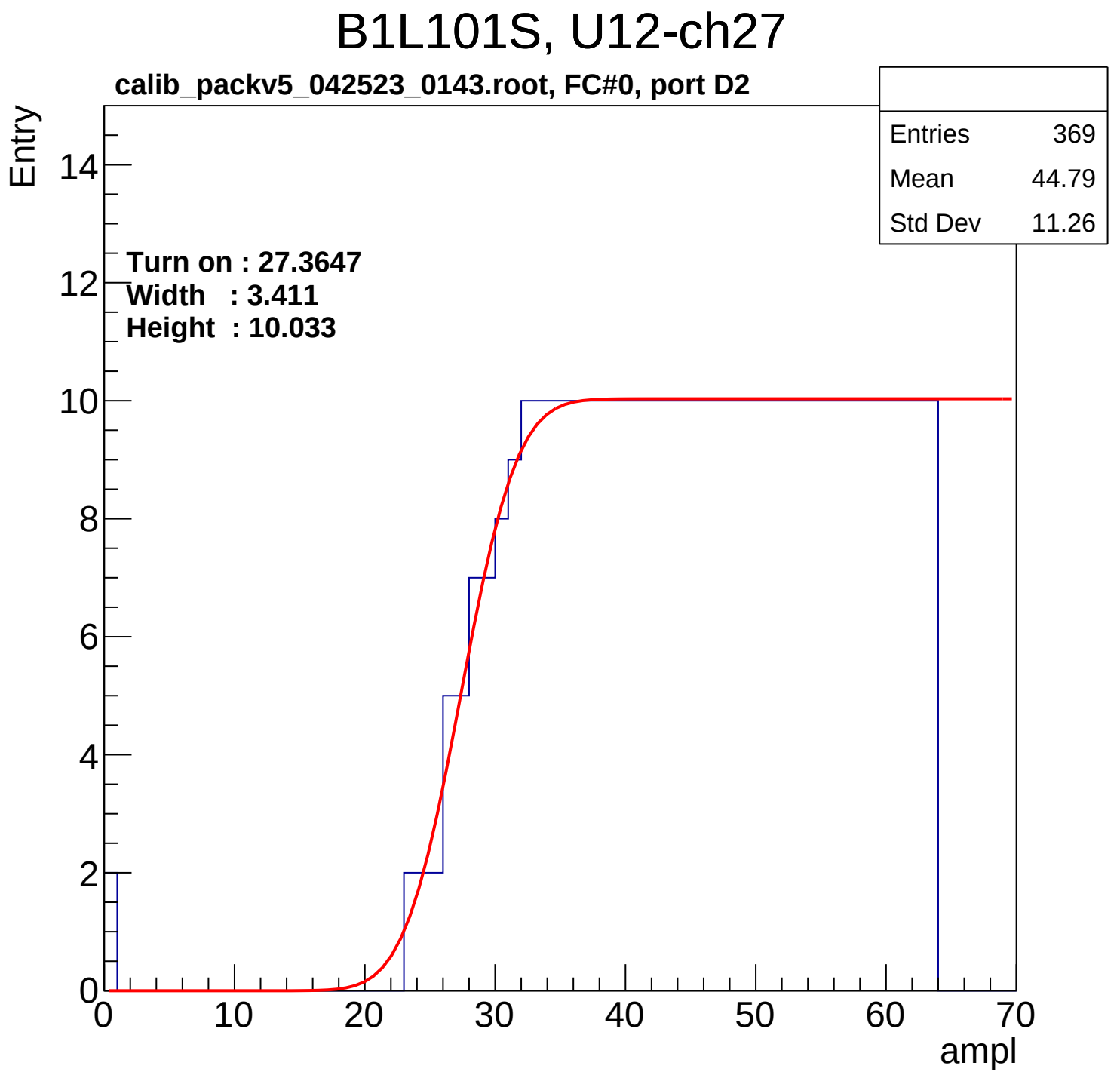

B1L101S, U12-ch22
calib_packv5_042523_0143.root, FC#0, port D2
Entries 375
Mean 44.43
Std Dev 11.6
Turn on : 26.9422
Width : 4.146
Height : 10.039
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

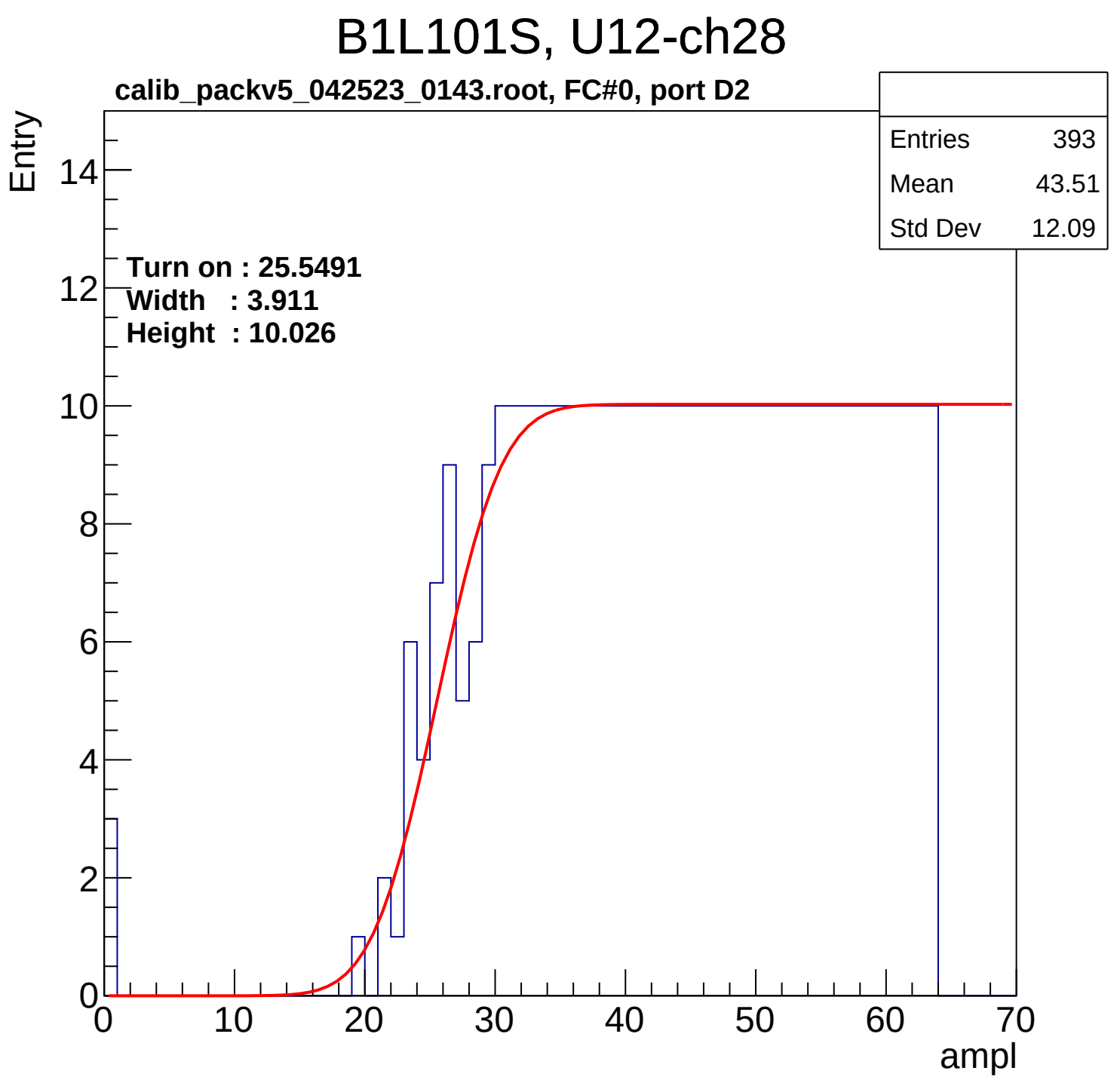

B1L101S, U12-ch23
calib_packv5_042523_0143.root, FC#0, port D2
Entries 370
Mean 44.71
Std Dev 11.33
Turn on : 27.6459
Width : 4.227
Height : 10.087
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

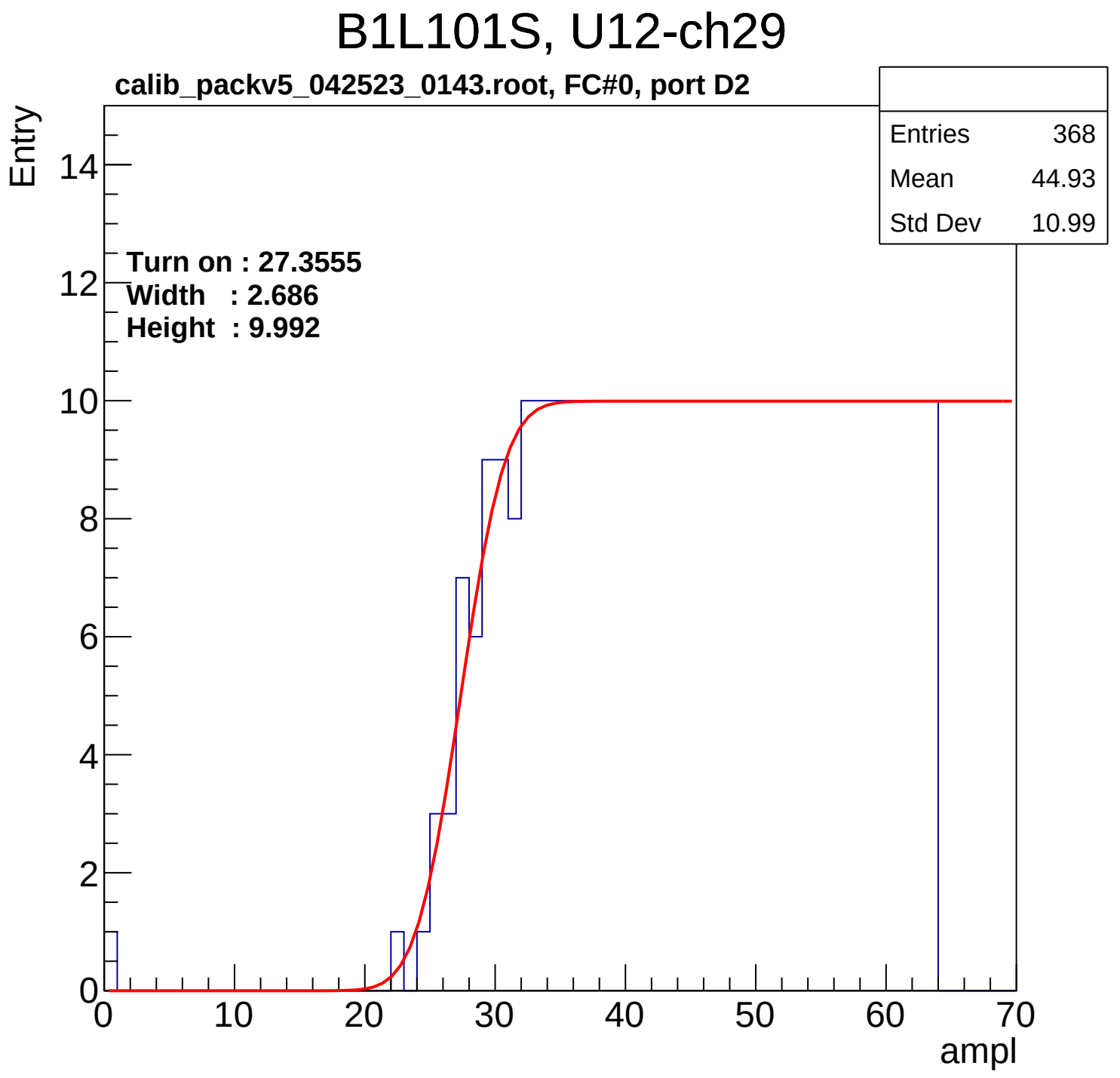

B1L101S, U12-ch24
calib_packv5_042523_0143.root, FC#0, port D2
Entries 373
Mean 44.62
Std Dev 11.32
Turn on : 27.0872
Width : 2.653
Height : 10.015
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

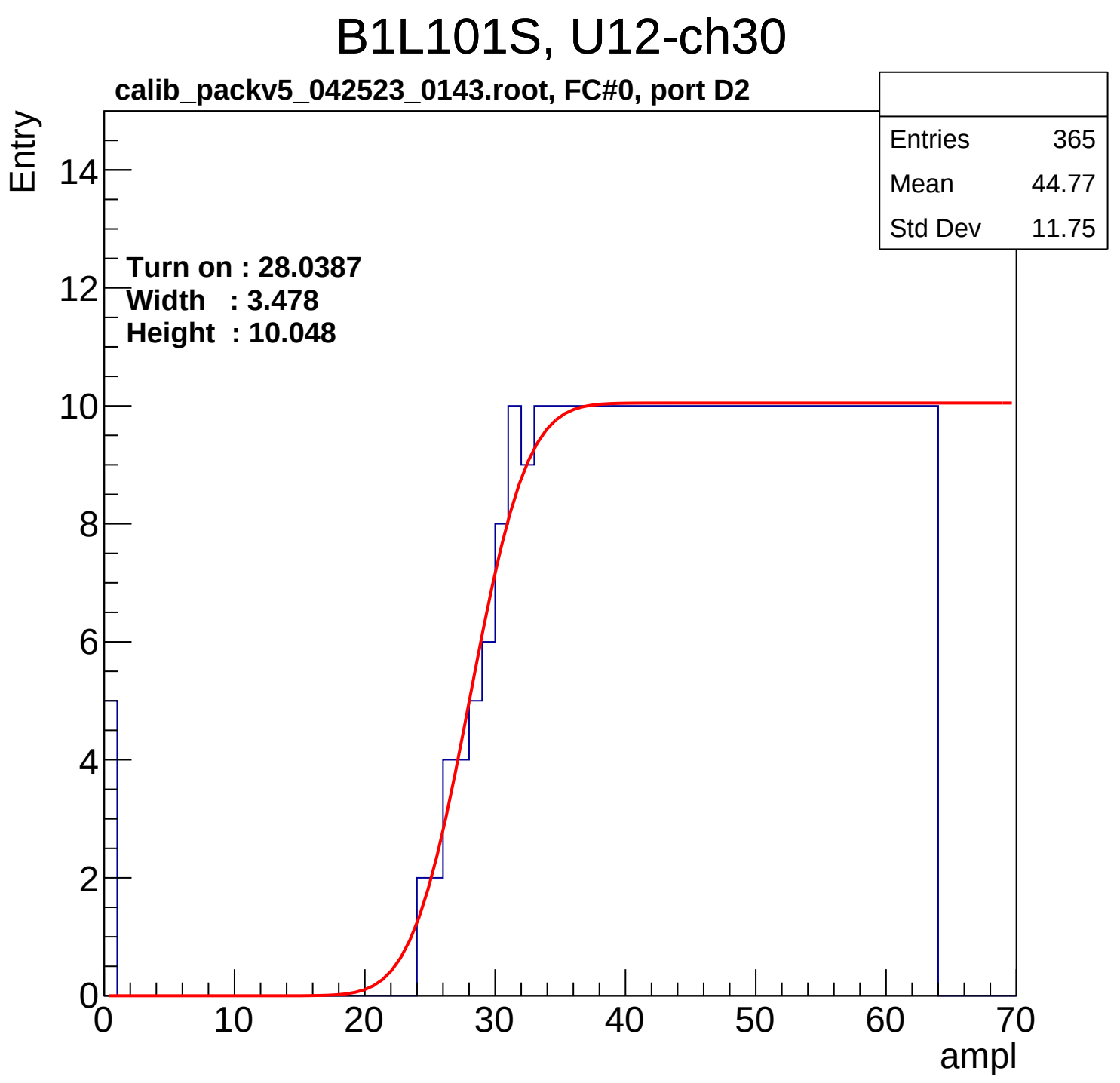

B1L101S, U12-ch25
calib_packv5_042523_0143.root, FC#0, port D2
Entries 360
Mean 45.11
Std Dev 11.4
Turn on : 28.4732
Width : 3.415
Height : 10.065
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

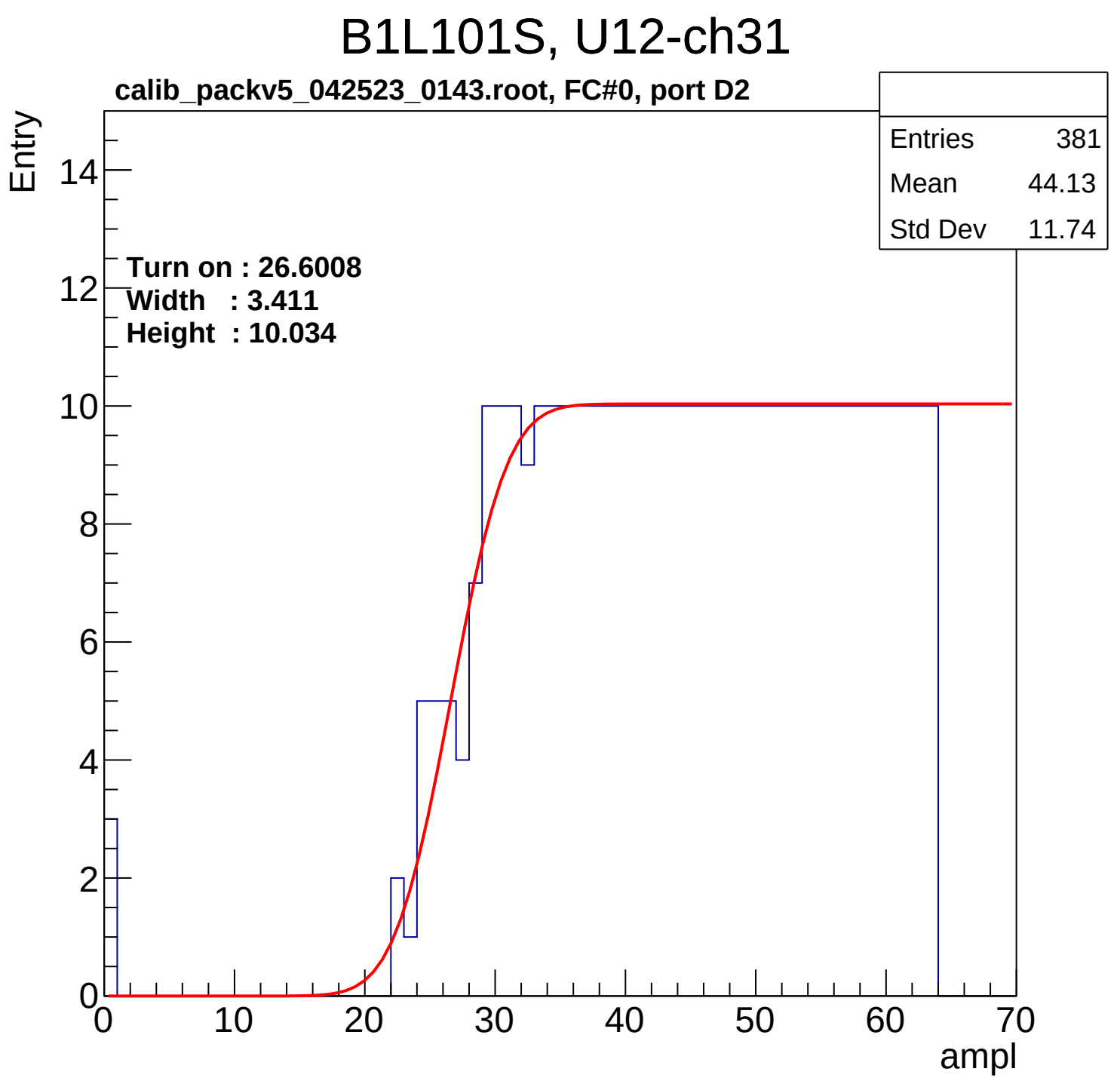

B1L101S, U12-ch26
calib_packv5_042523_0143.root, FC#0, port D2
Entries 375
Mean 44.37
Std Dev 11.77
Turn on : 27.3465
Width : 3.698
Height : 10.084
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

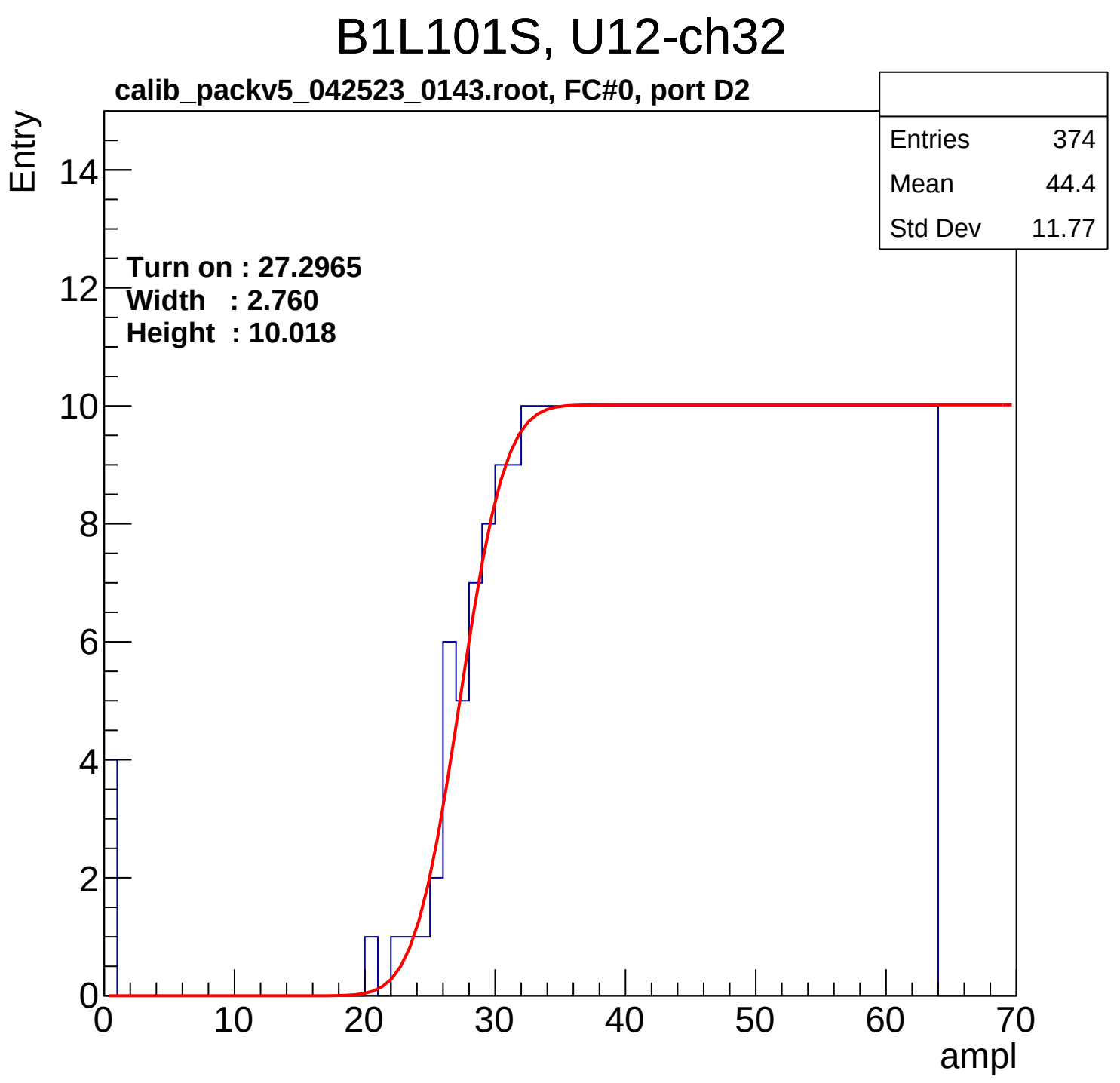

B1L101S, U12-ch27
calib_packv5_042523_0143.root, FC#0, port D2
Entries 369
Mean 44.79
Std Dev 11.26
Turn on : 27.3647
Width : 3.411
Height : 10.033
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

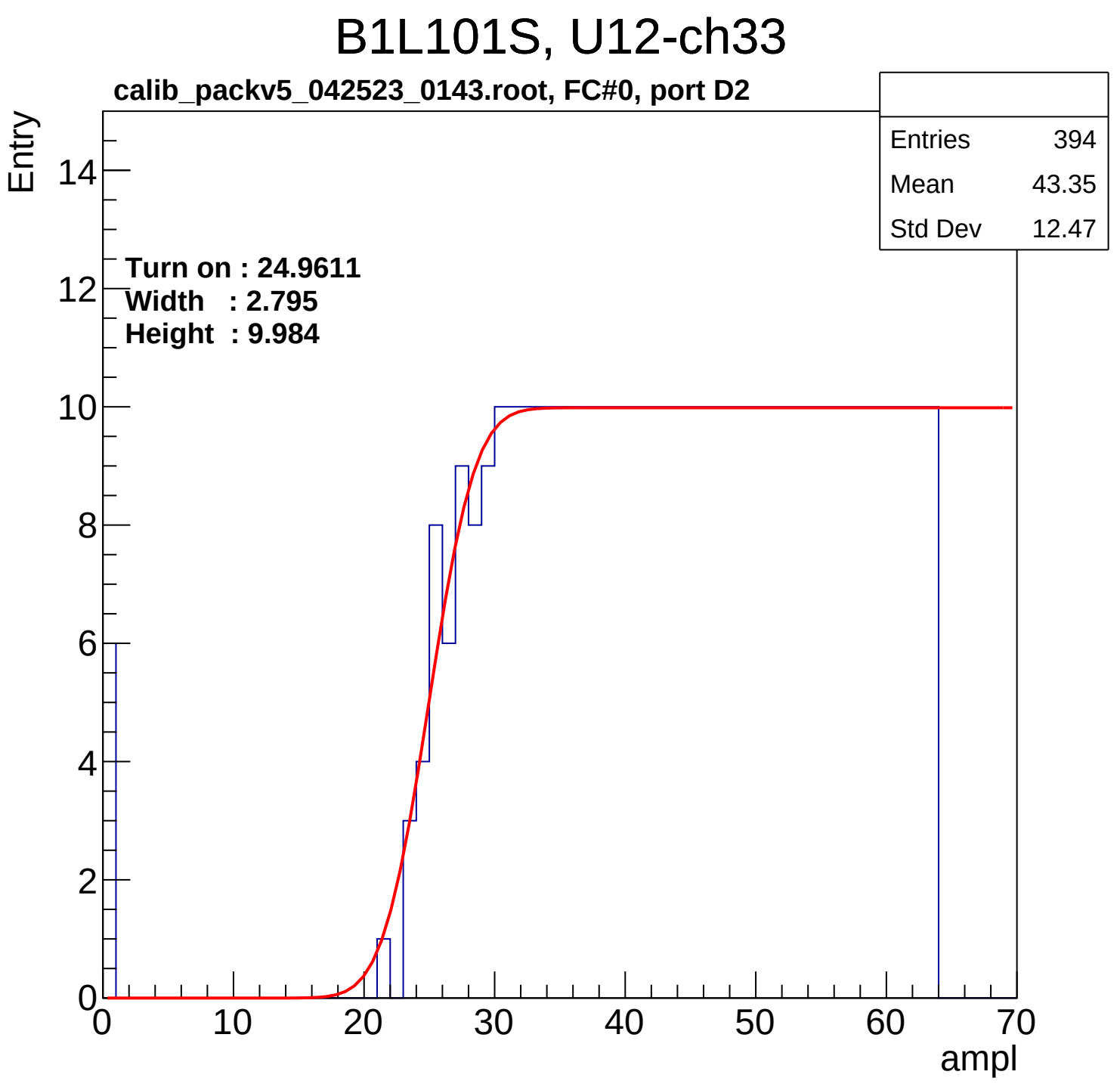

B1L101S, U12-ch28
calib_packv5_042523_0143.root, FC#0, port D2
Entries 393
Mean 43.51
Std Dev 12.09
Turn on : 25.5491
Width : 3.911
Height : 10.026
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

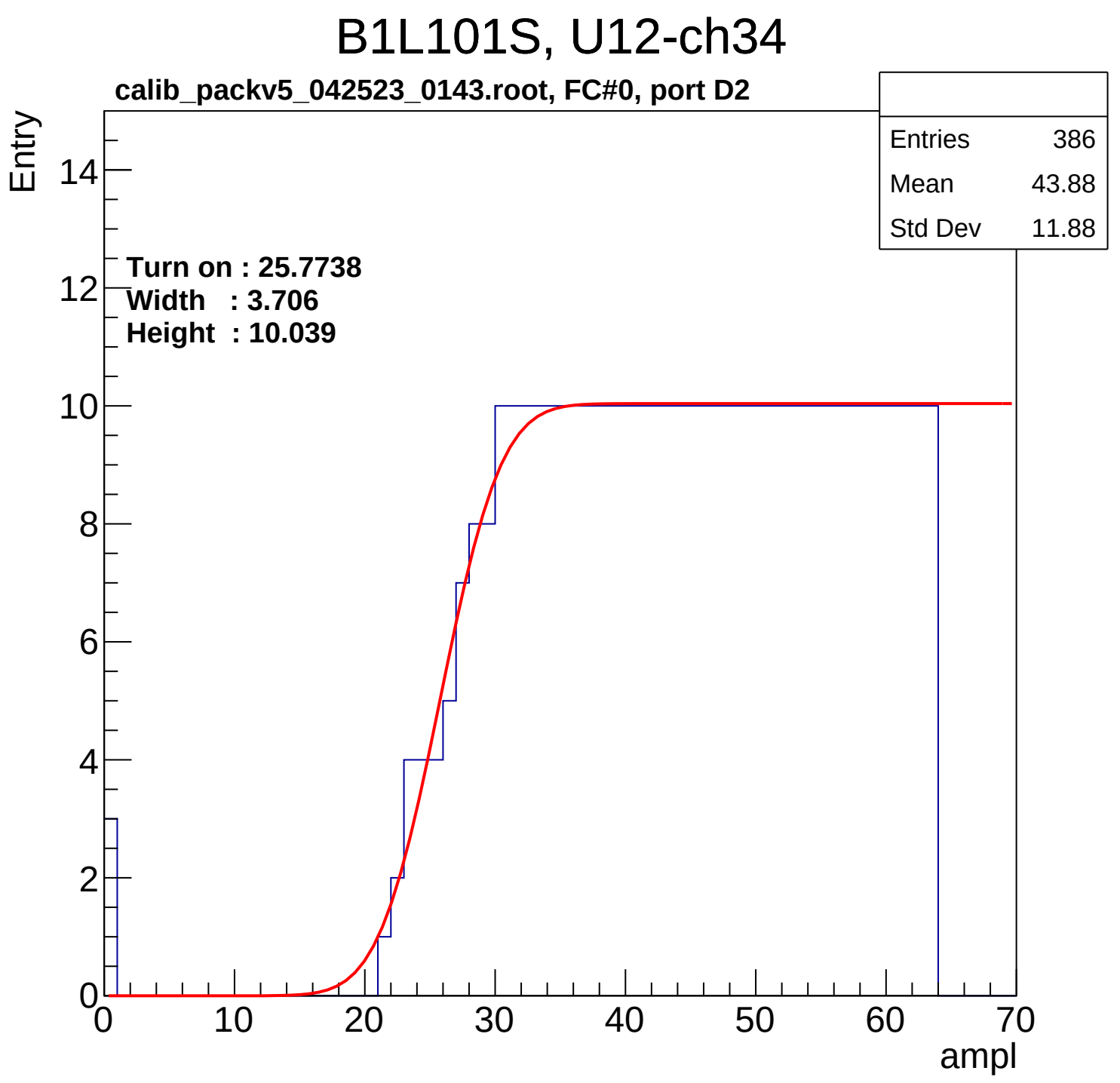

B1L101S, U12-ch29
calib_packv5_042523_0143.root, FC#0, port D2
Entries 368
Mean 44.93
Std Dev 10.99
Turn on : 27.3555
Width : 2.686
Height : 9.992
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

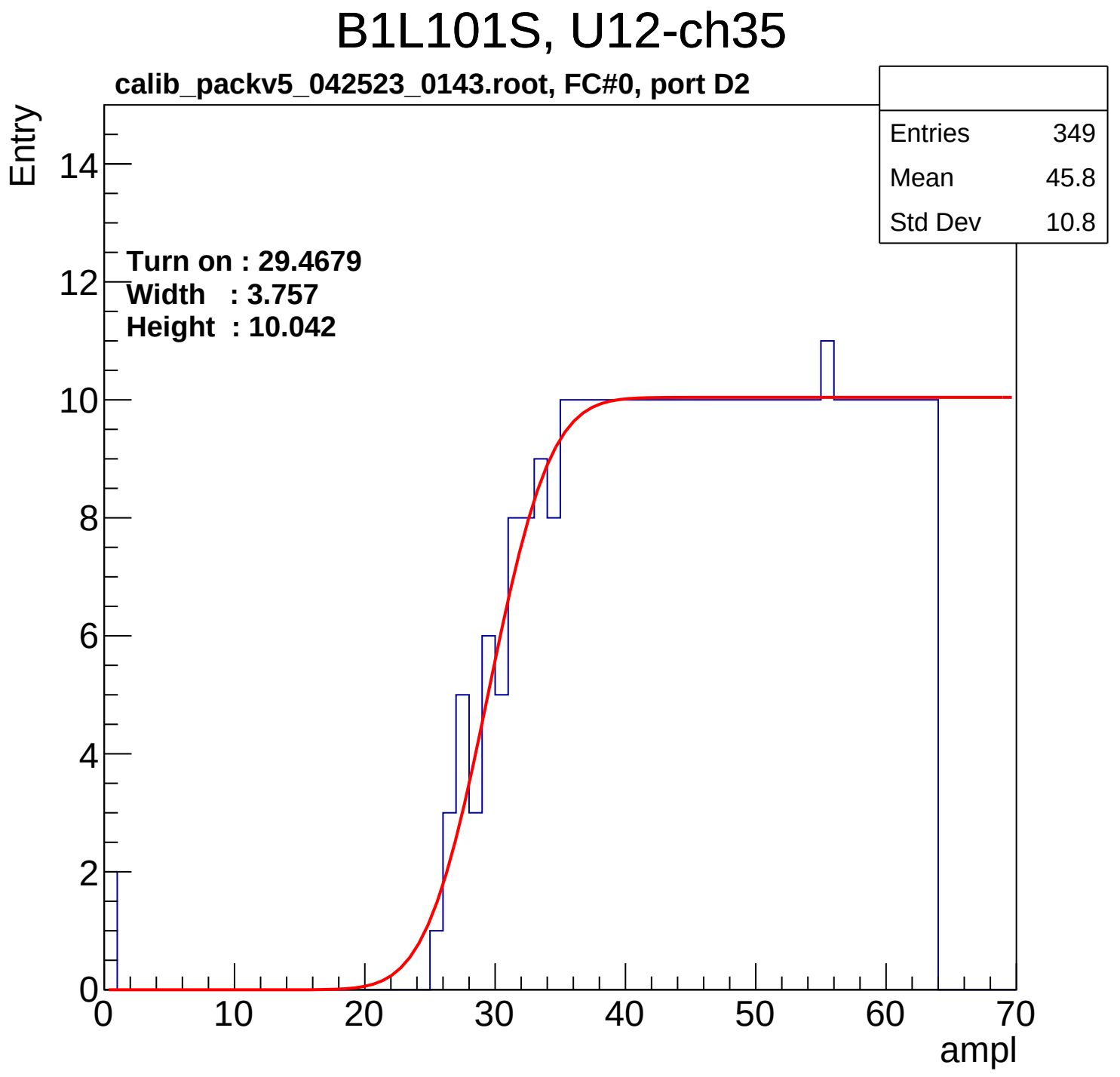

B1L101S, U12-ch30
calib_packv5_042523_0143.root, FC#0, port D2
Entries 365
Mean 44.77
Std Dev 11.75
Turn on : 28.0387
Width : 3.478
Height : 10.048
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

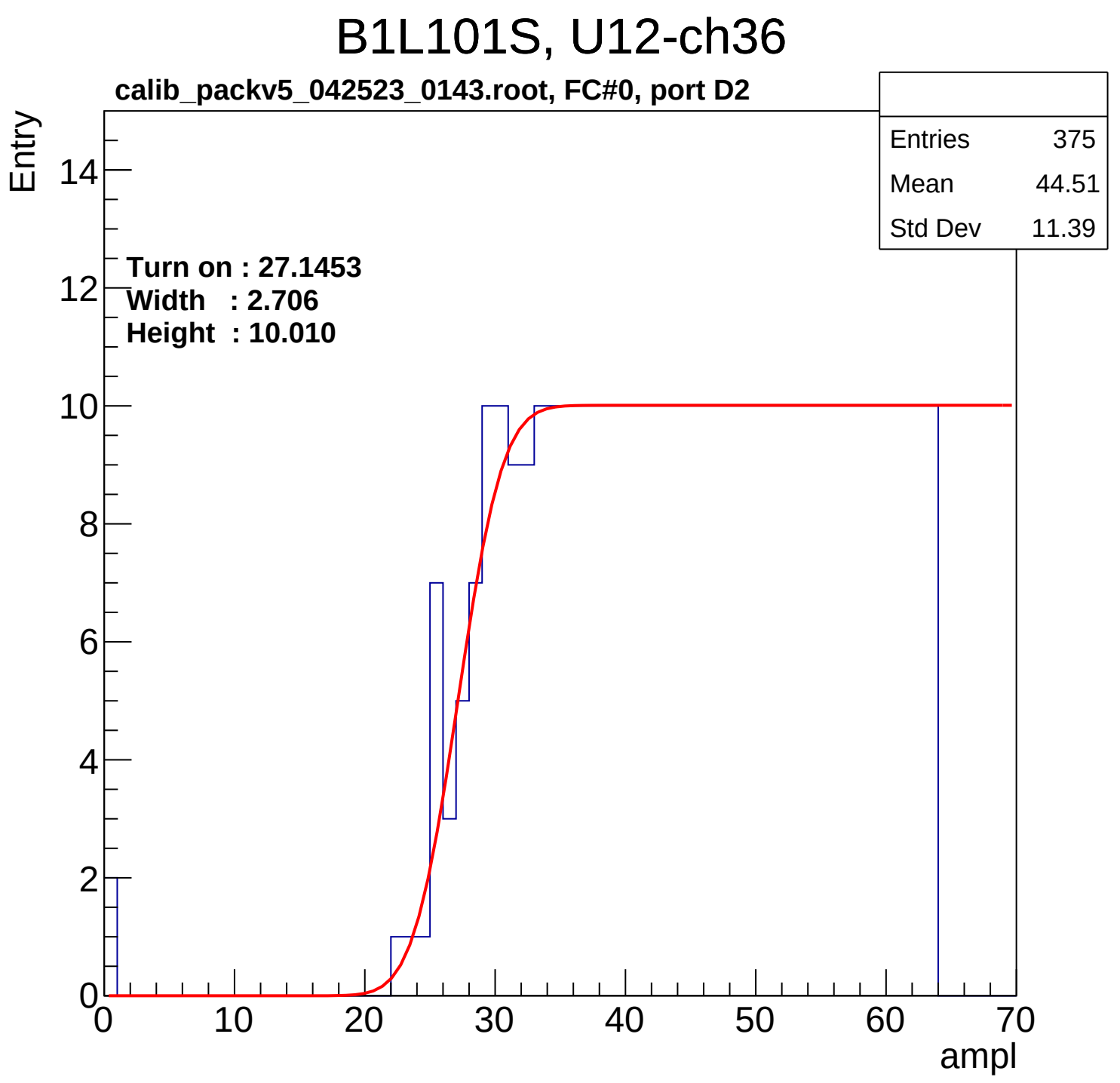

B1L101S, U12-ch31
calib_packv5_042523_0143.root, FC#0, port D2
Entries 381
Mean 44.13
Std Dev 11.74
Turn on : 26.6008
Width : 3.411
Height : 10.034
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

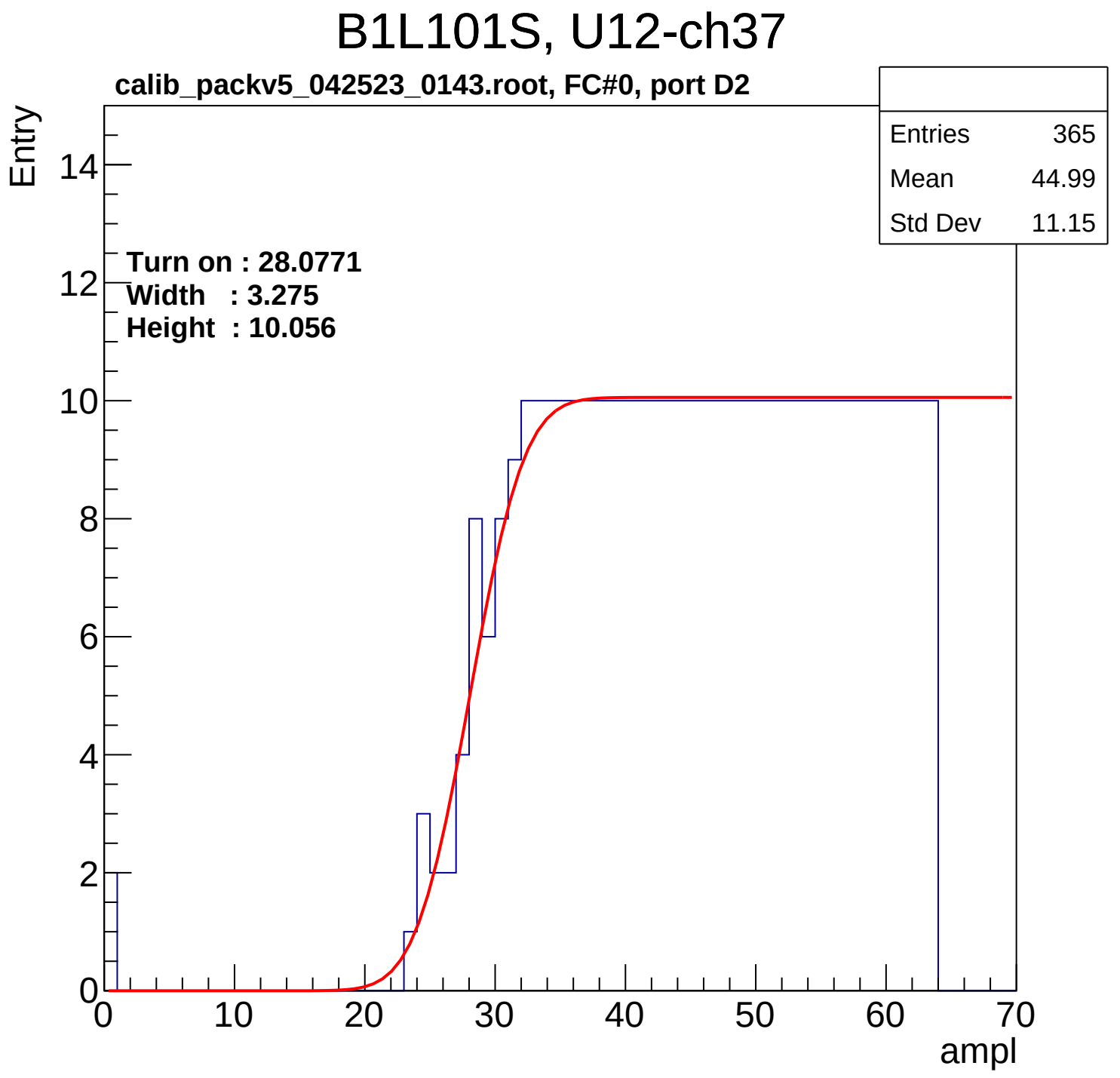

B1L101S, U12-ch32
calib_packv5_042523_0143.root, FC#0, port D2
Entries 374
Mean 44.4
Std Dev 11.77
Turn on : 27.2965
Width : 2.760
Height : 10.018
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

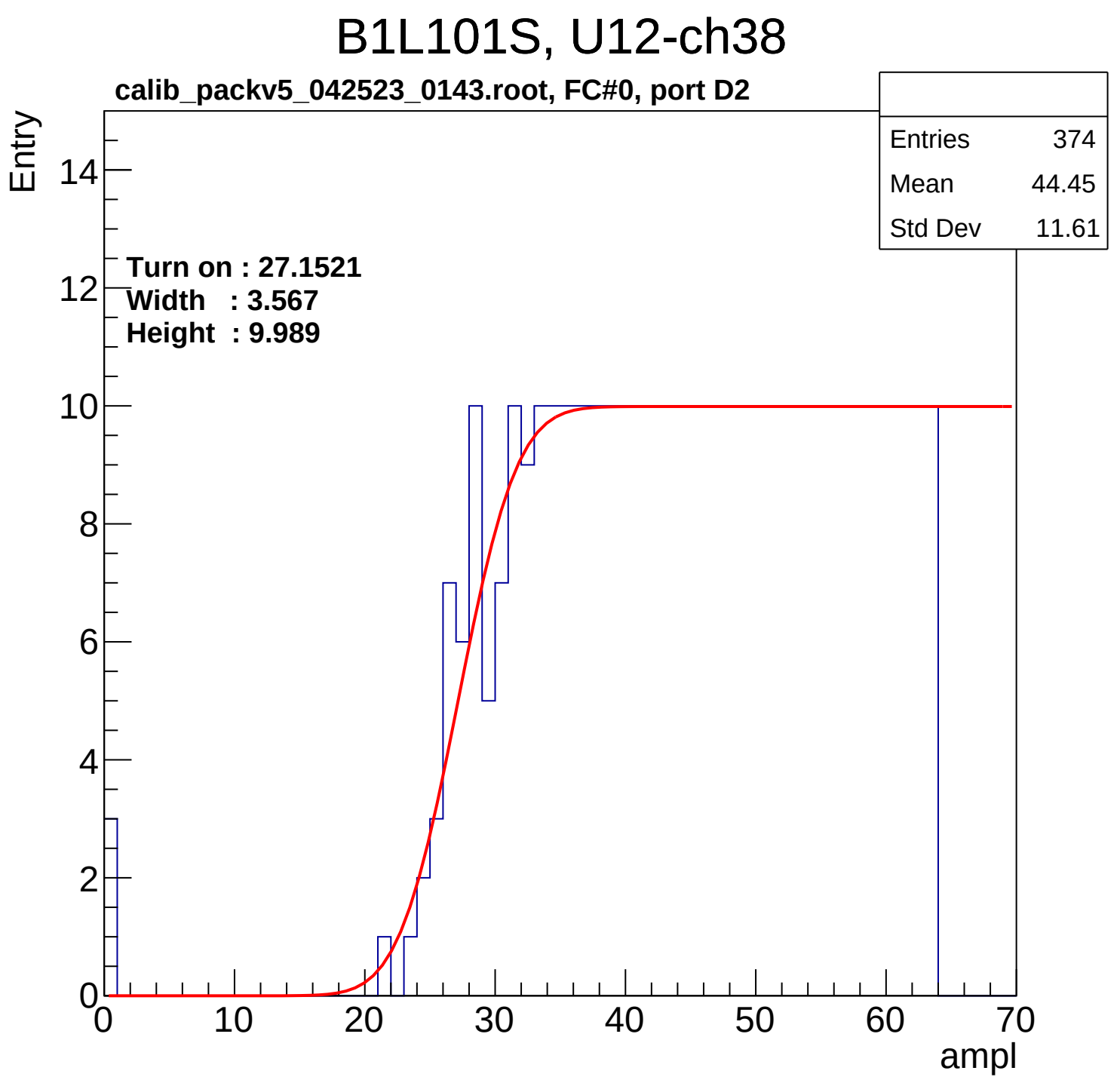

B1L101S, U12-ch33
calib_packv5_042523_0143.root, FC#0, port D2
Entries 394
Mean 43.35
Std Dev 12.47
Turn on : 24.9611
Width : 2.795
Height : 9.984
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

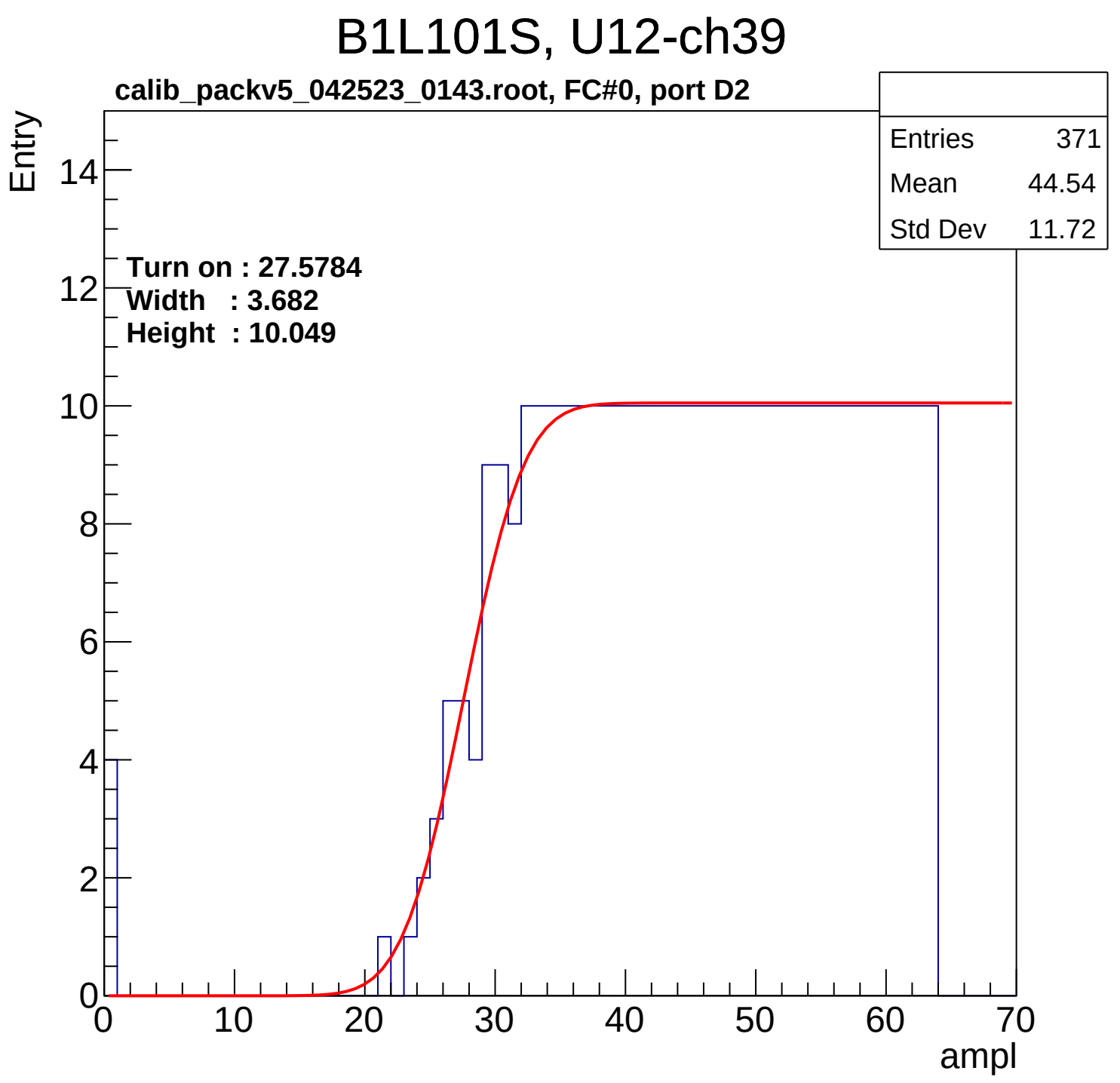

B1L101S, U12-ch34
calib_packv5_042523_0143.root, FC#0, port D2
Entries 386
Mean 43.88
Std Dev 11.88
Turn on : 25.7738
Width : 3.706
Height : 10.039
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

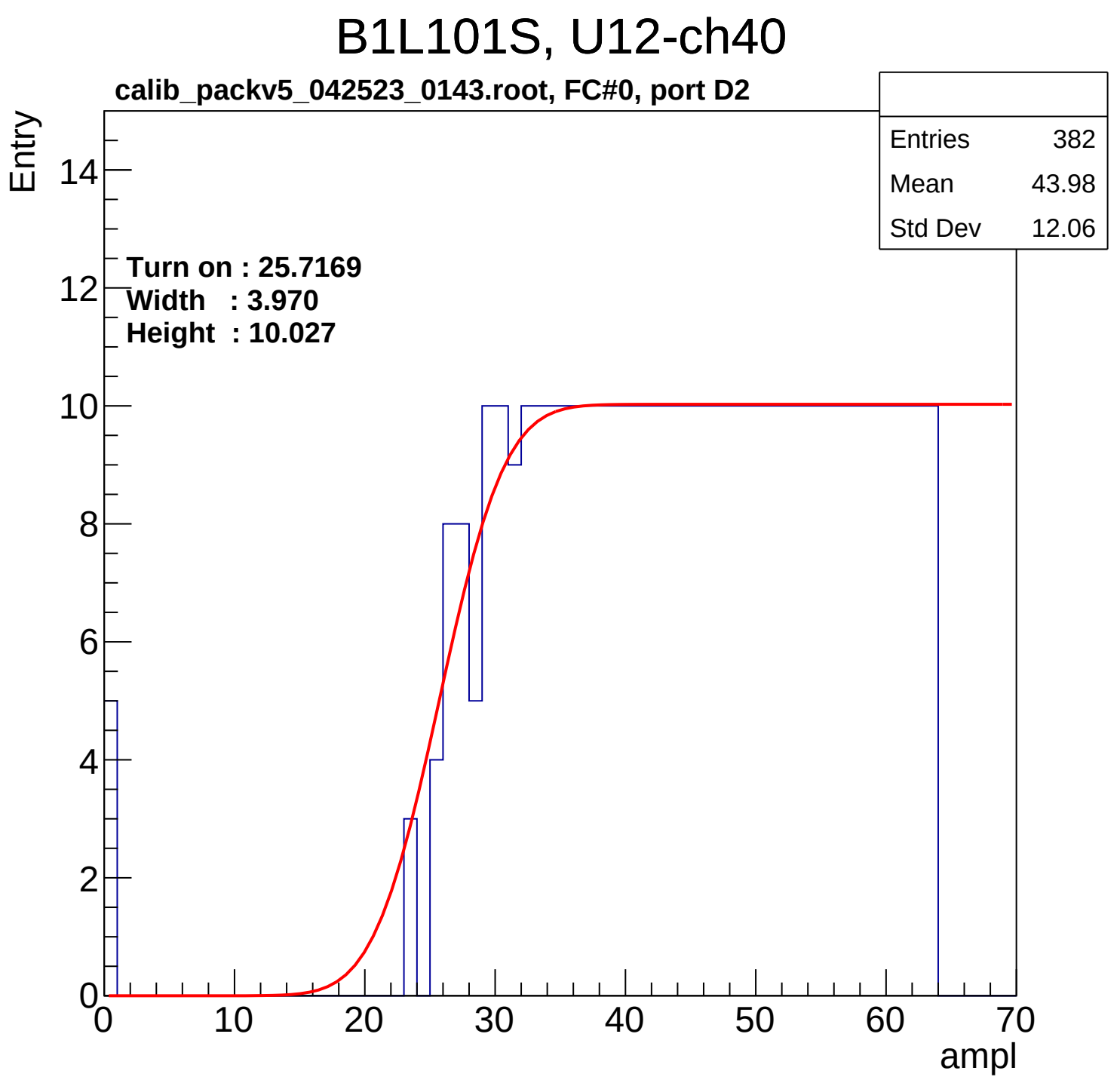

B1L101S, U12-ch35
calib_packv5_042523_0143.root, FC#0, port D2
Entries 349
Mean 45.8
Std Dev 10.8
Turn on : 29.4679
Width : 3.757
Height : 10.042
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

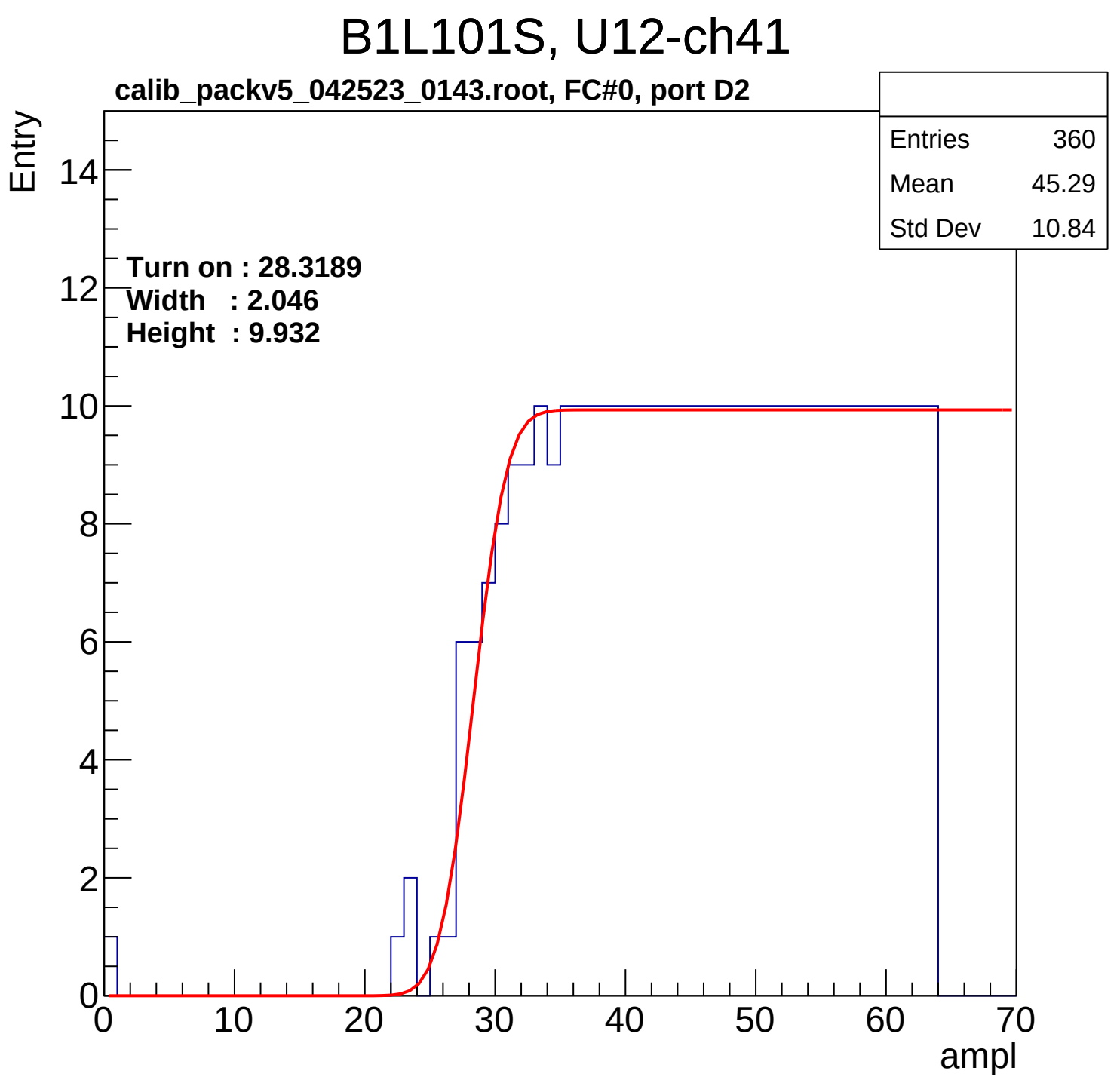

B1L101S, U12-ch36
calib_packv5_042523_0143.root, FC#0, port D2
Entries 375
Mean 44.51
Std Dev 11.39
Turn on : 27.1453
Width : 2.706
Height : 10.010
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

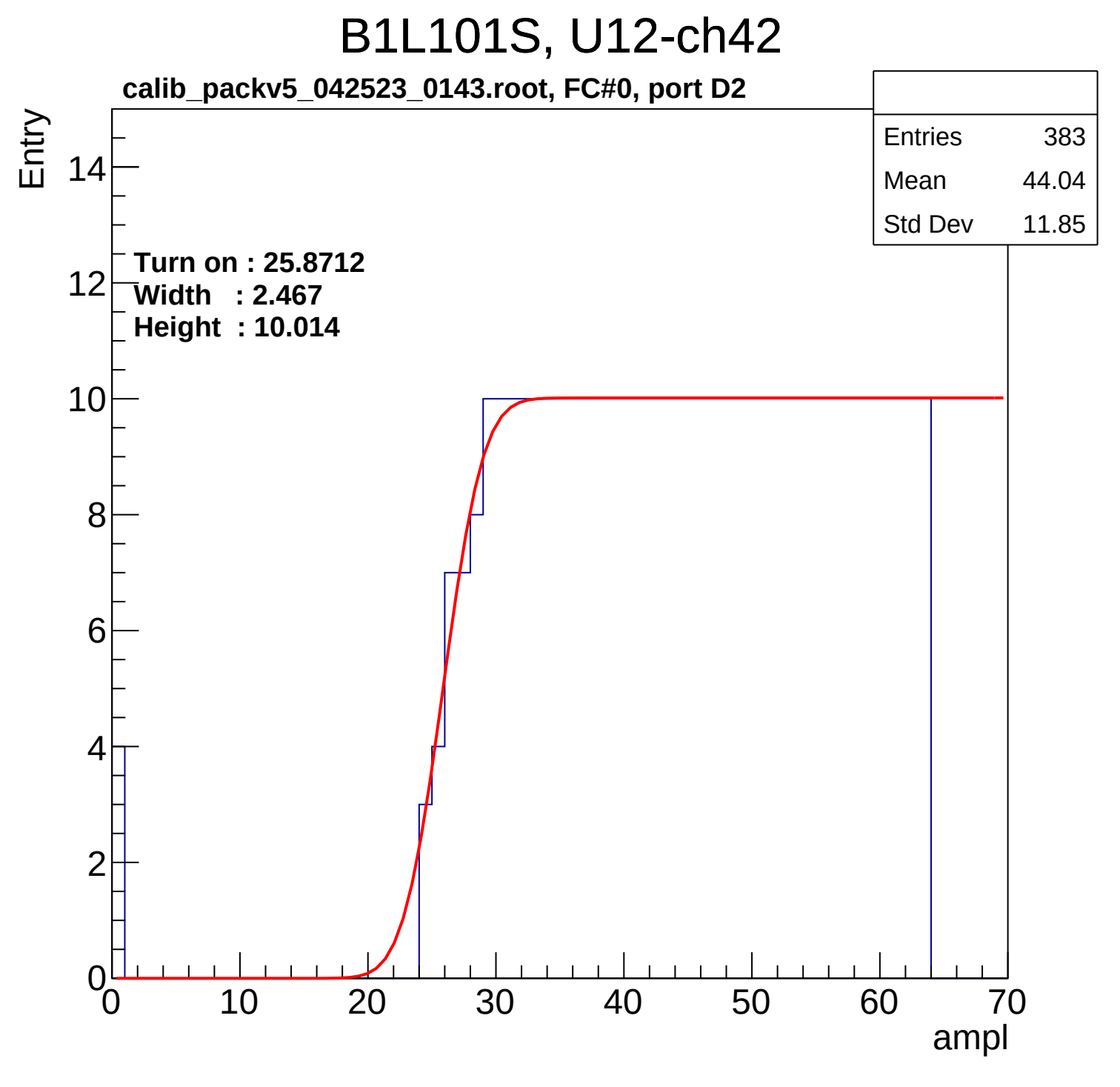

B1L101S, U12-ch37
calib_packv5_042523_0143.root, FC#0, port D2
Entries 365
Mean 44.99
Std Dev 11.15
Turn on : 28.0771
Width : 3.275
Height : 10.056
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

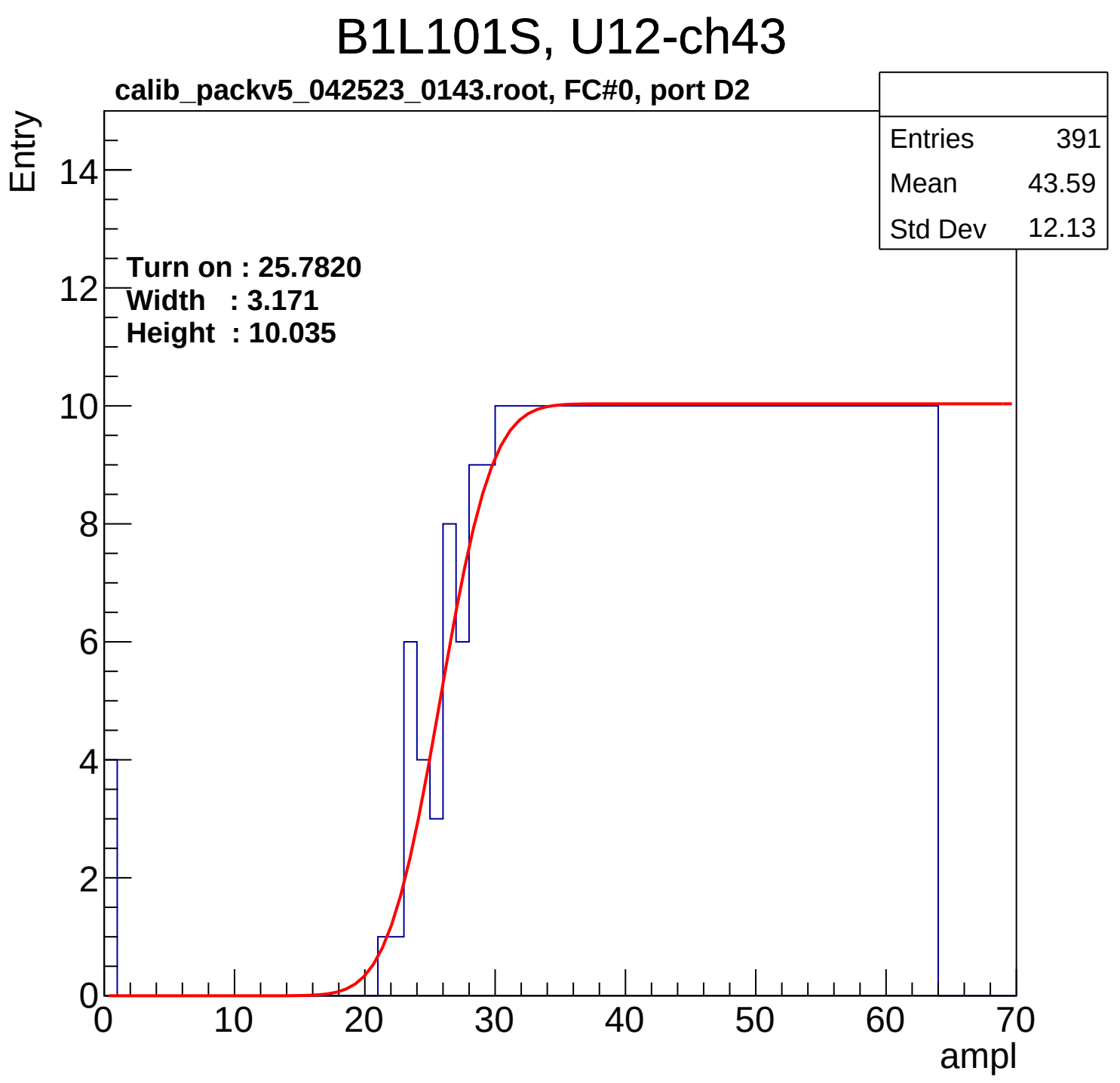

B1L101S, U12-ch38
calib_packv5_042523_0143.root, FC#0, port D2
Entries 374
Mean 44.45
Std Dev 11.61
Turn on : 27.1521
Width : 3.567
Height : 9.989
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

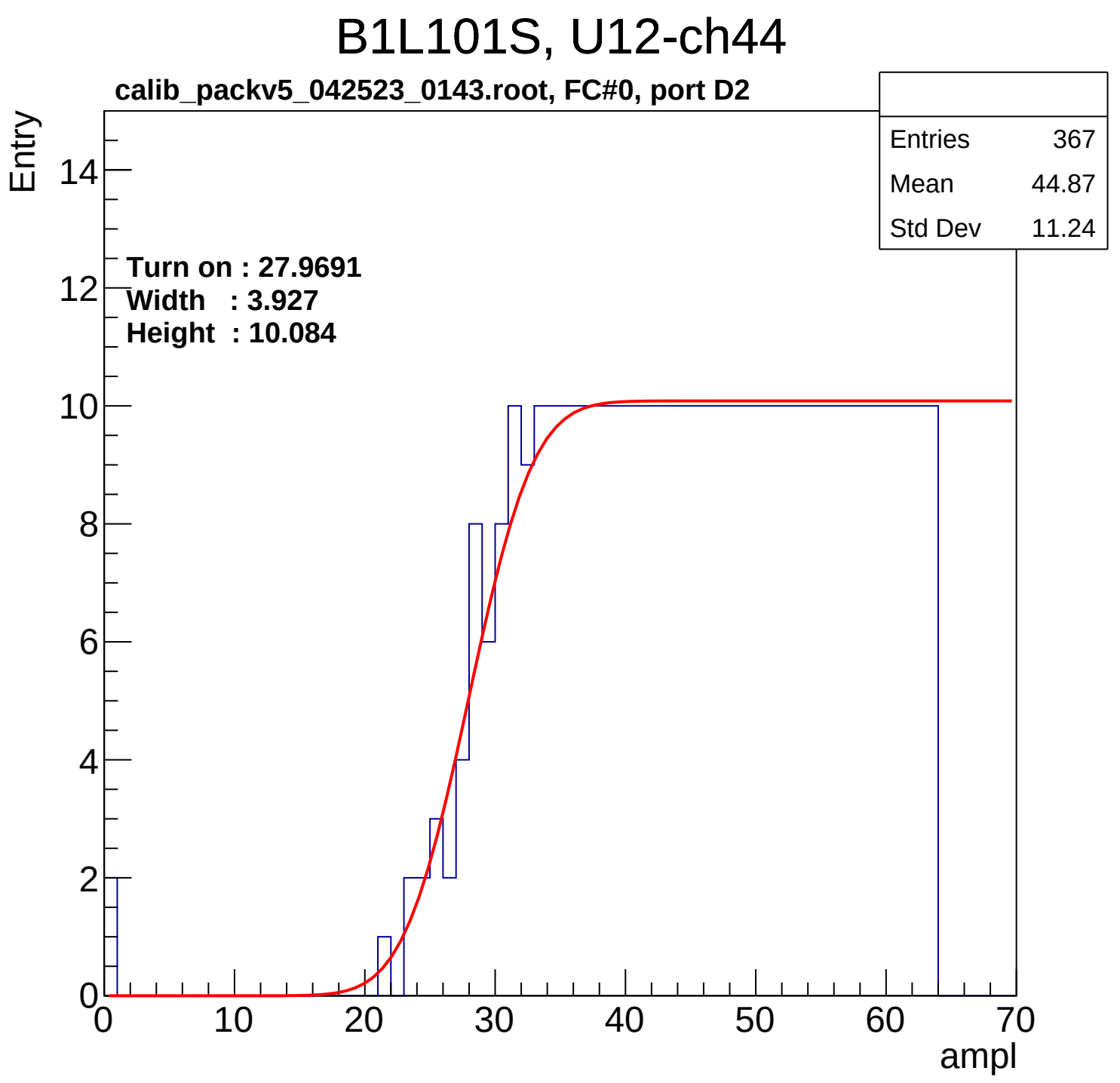

B1L101S, U12-ch39
calib_packv5_042523_0143.root, FC#0, port D2
Entries 371
Mean 44.54
Std Dev 11.72
Turn on : 27.5784
Width : 3.682
Height : 10.049
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

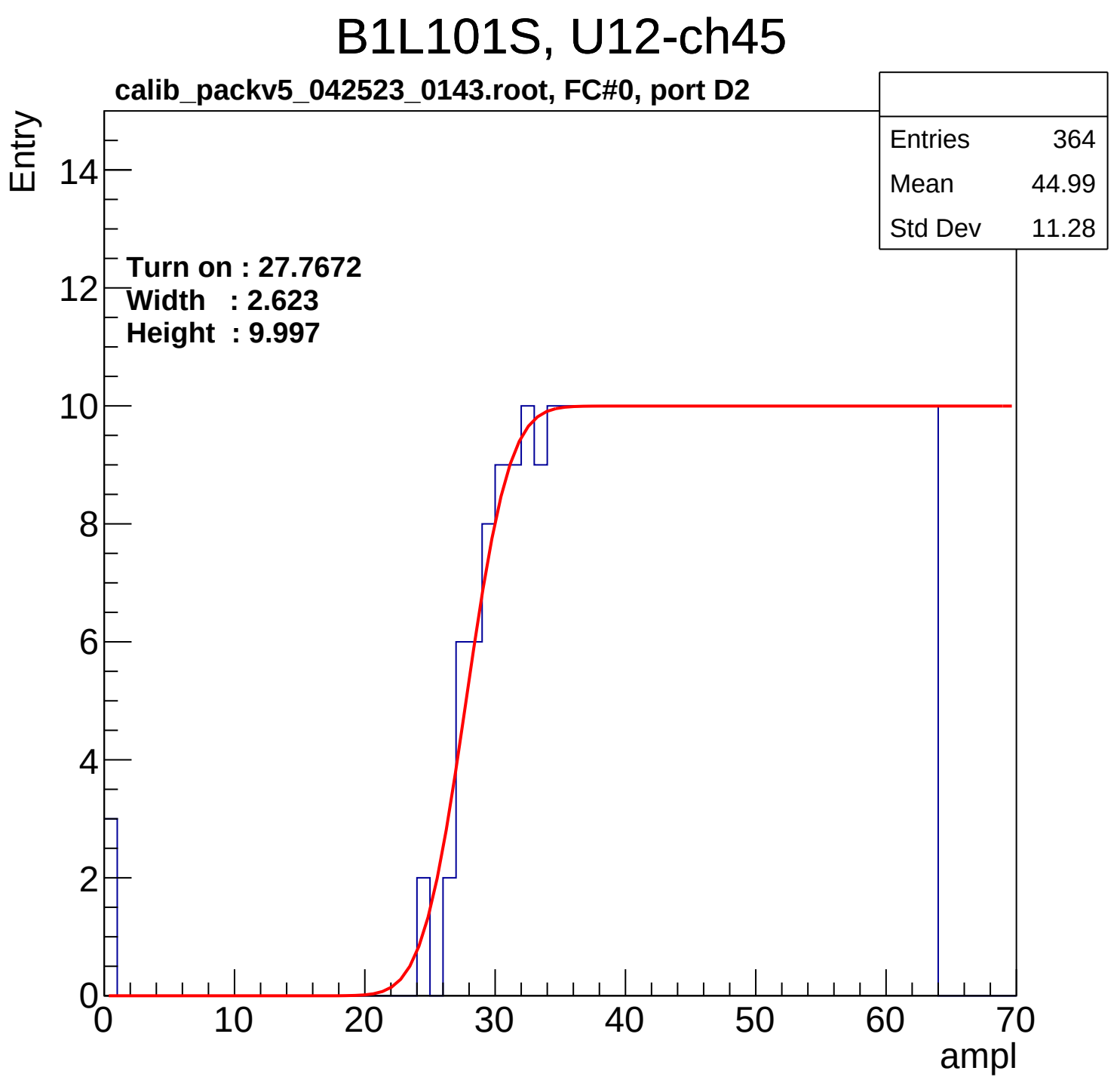

B1L101S, U12-ch40
calib_packv5_042523_0143.root, FC#0, port D2
Entries 382
Mean 43.98
Std Dev 12.06
Turn on : 25.7169
Width : 3.970
Height : 10.027
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

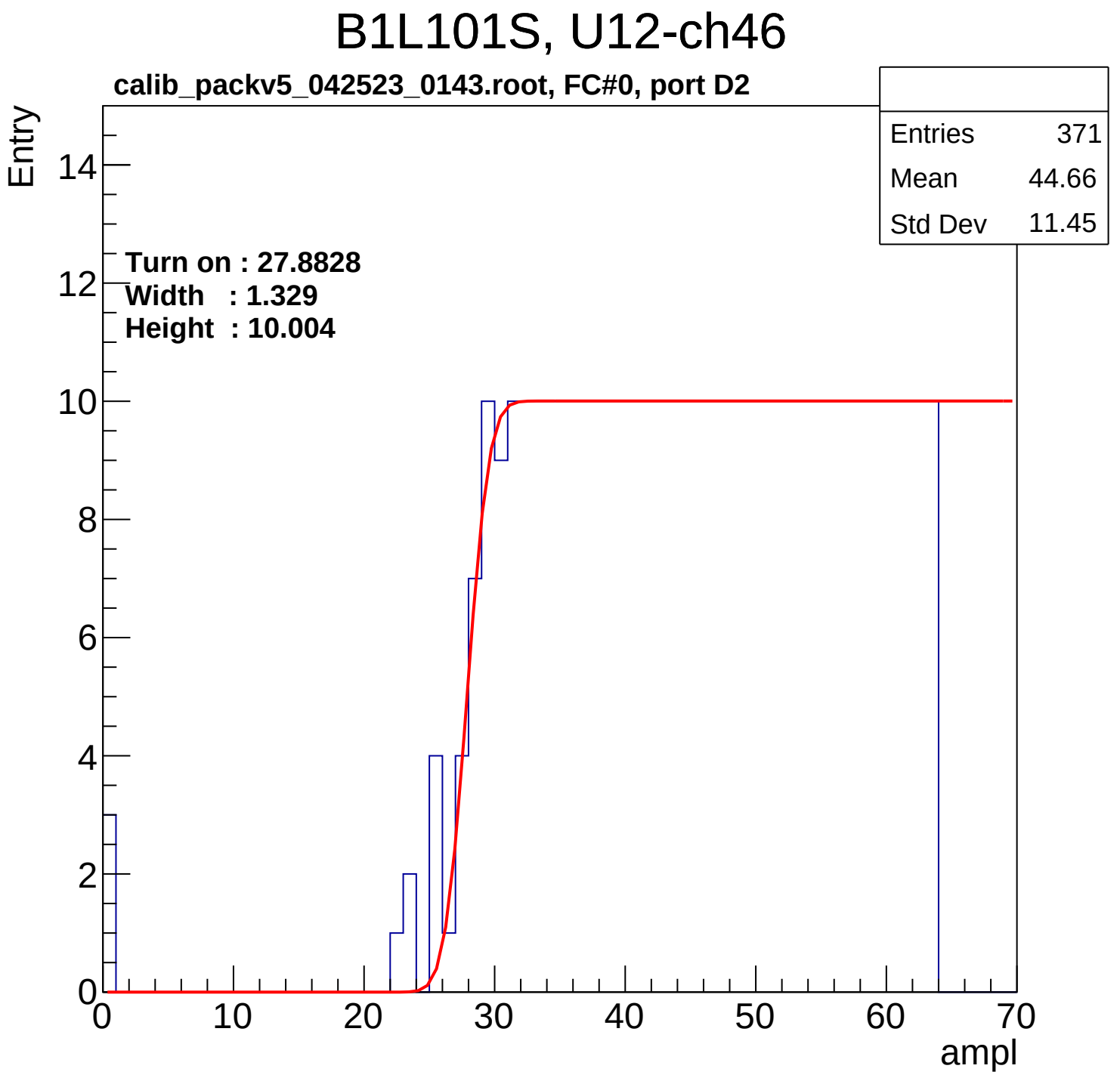

B1L101S, U12-ch41
calib_packv5_042523_0143.root, FC#0, port D2
Entries 360
Mean 45.29
Std Dev 10.84
Turn on : 28.3189
Width : 2.046
Height : 9.932
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

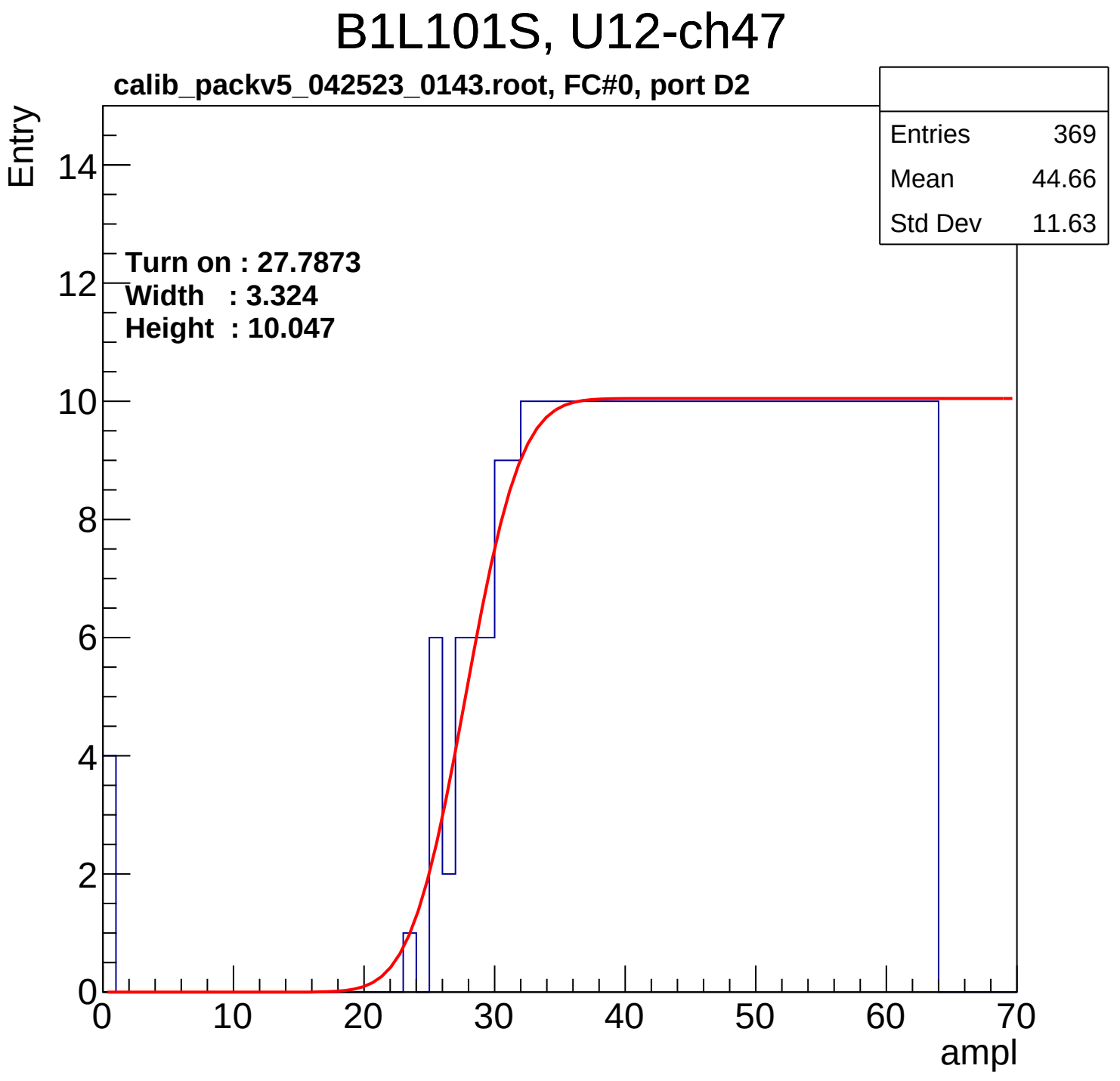

B1L101S, U12-ch42
calib_packv5_042523_0143.root, FC#0, port D2
Entries 383
Mean 44.04
Std Dev 11.85
Turn on : 25.8712
Width : 2.467
Height : 10.014
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

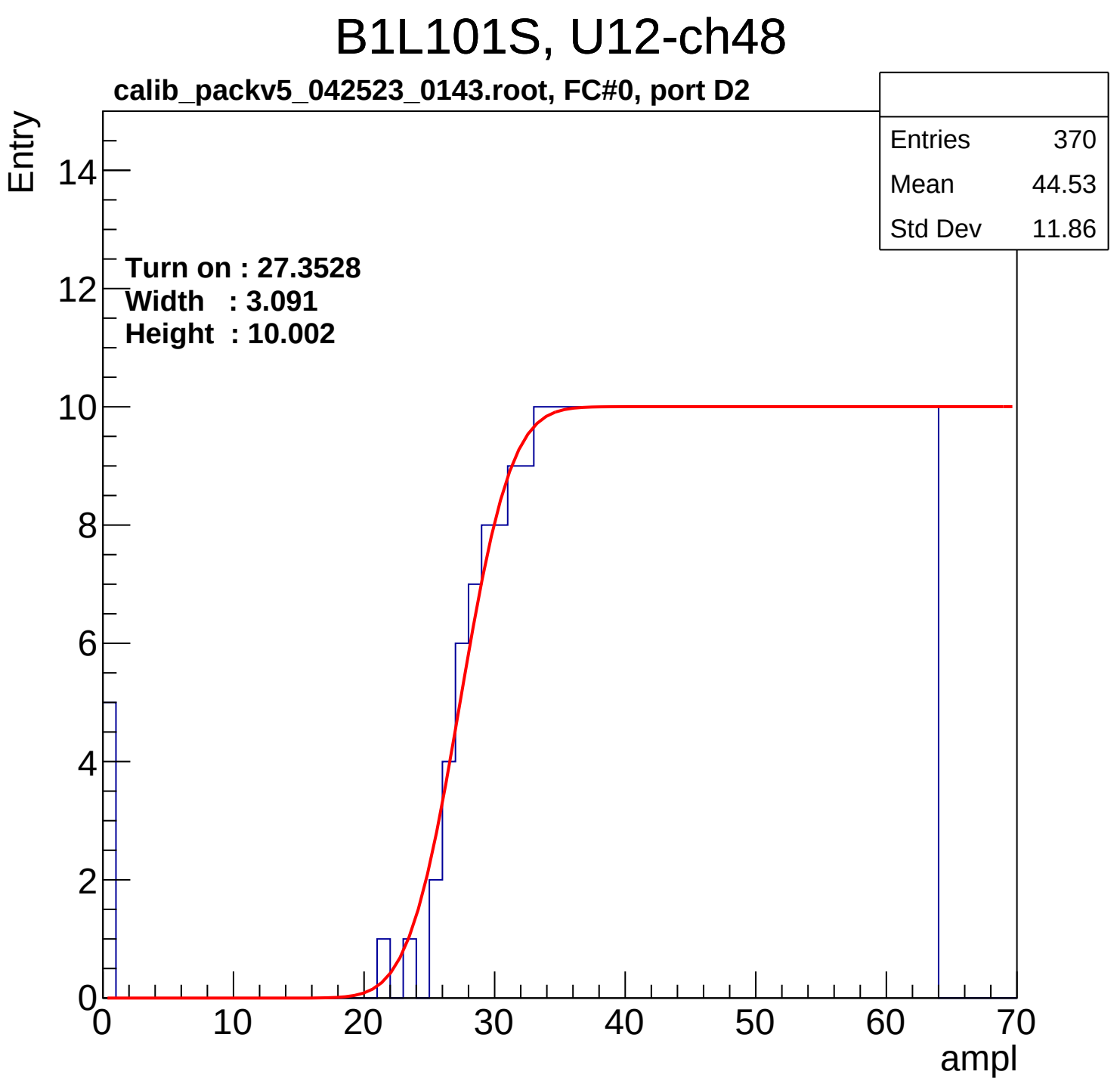

B1L101S, U12-ch43
calib_packv5_042523_0143.root, FC#0, port D2
Entries 391
Mean 43.59
Std Dev 12.13
Turn on : 25.7820
Width : 3.171
Height : 10.035
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

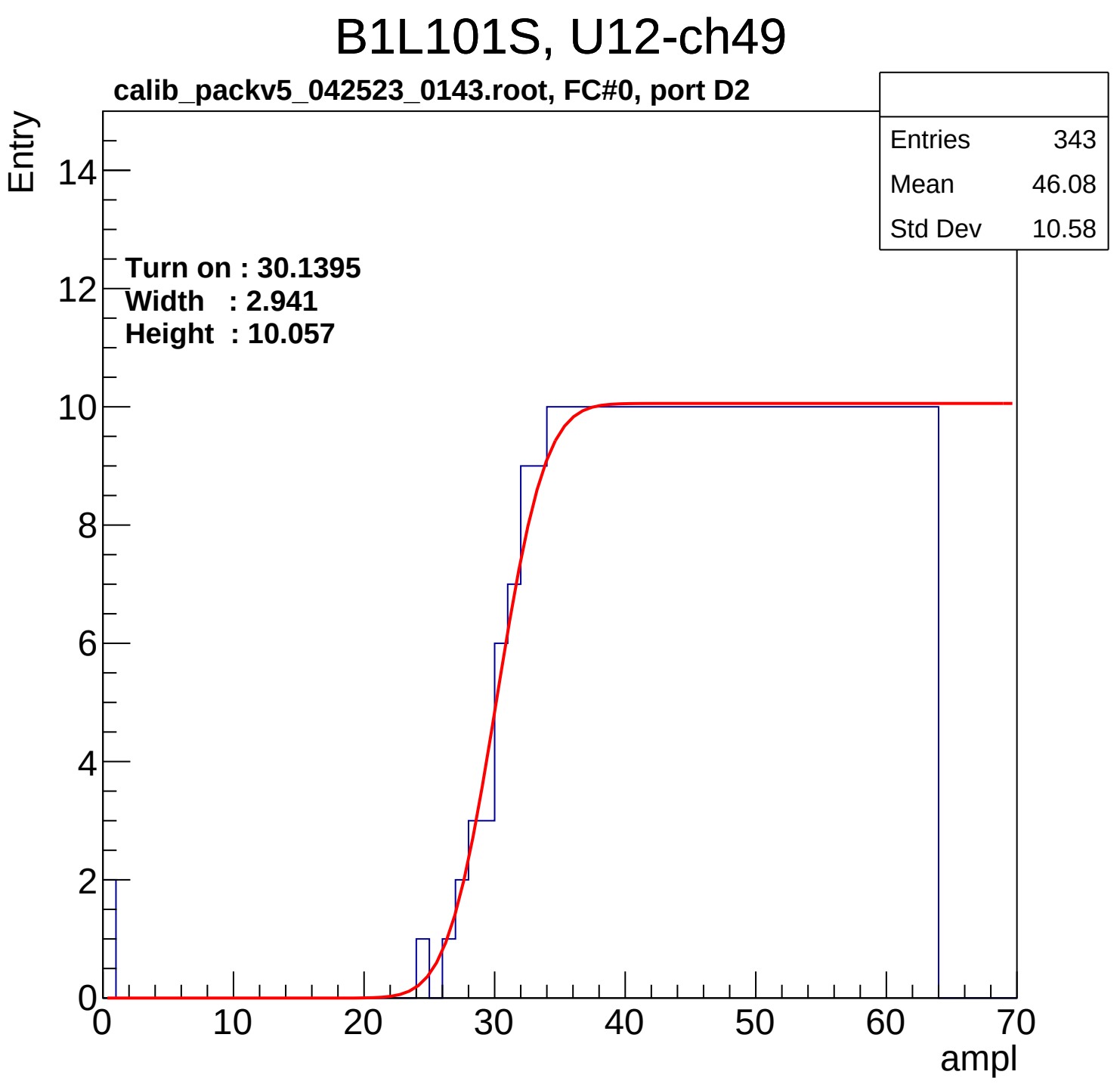

B1L101S, U12-ch44
calib_packv5_042523_0143.root, FC#0, port D2
Entries 367
Mean 44.87
Std Dev 11.24
Turn on : 27.9691
Width : 3.927
Height : 10.084
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

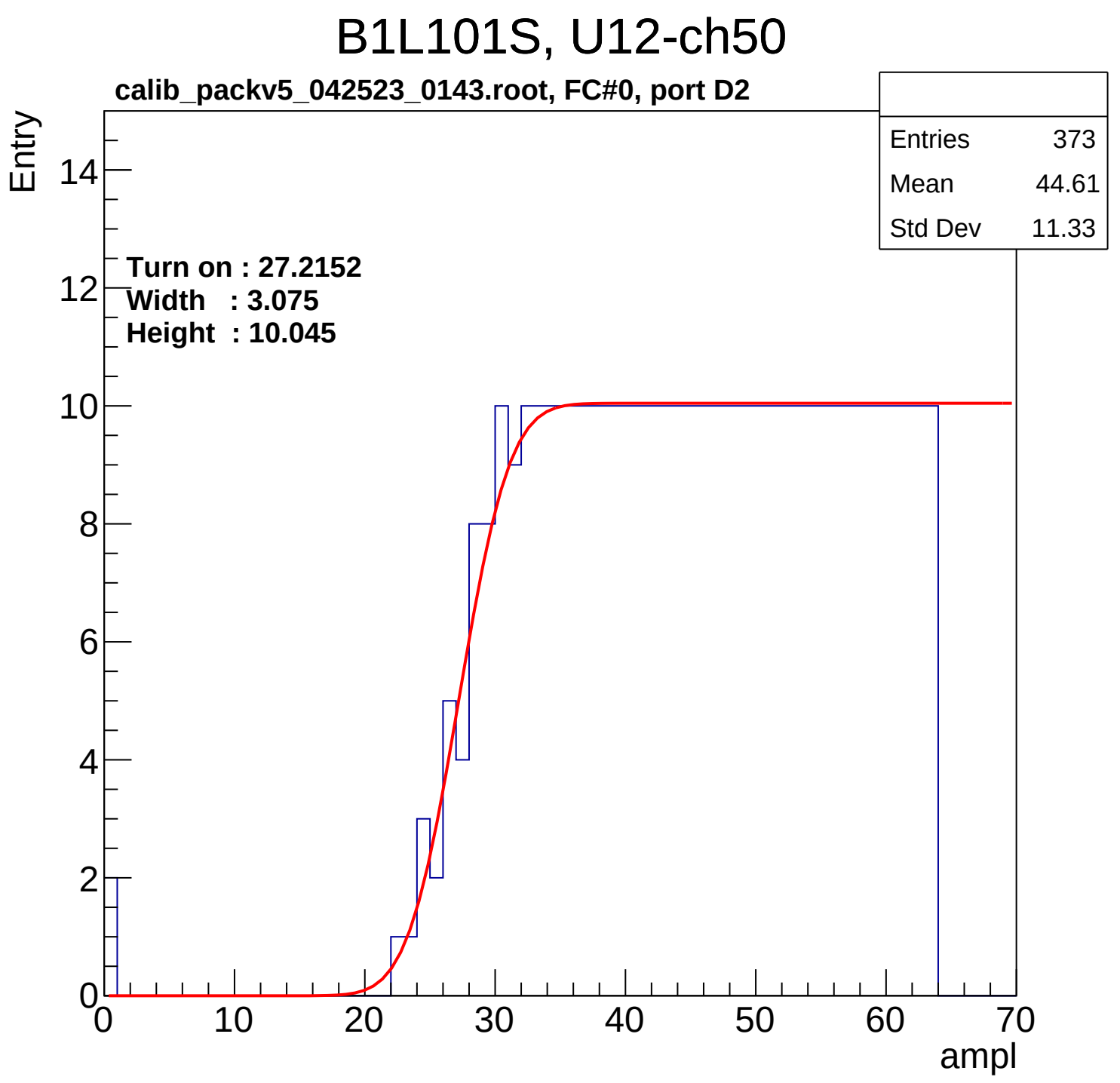

B1L101S, U12-ch45
calib_packv5_042523_0143.root, FC#0, port D2
Entries 364
Mean 44.99
Std Dev 11.28
Turn on : 27.7672
Width : 2.623
Height : 9.997
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

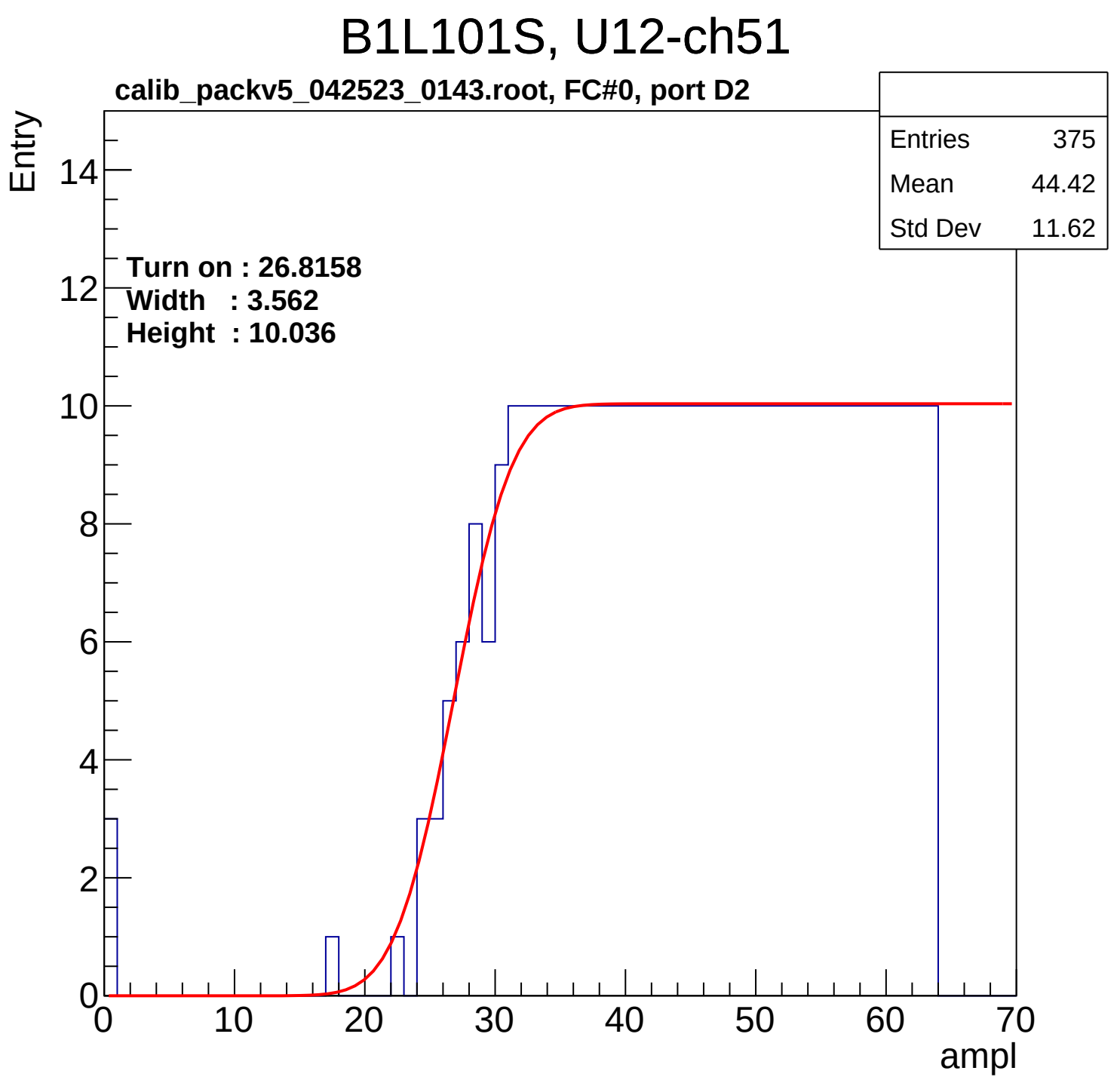

B1L101S, U12-ch46
calib_packv5_042523_0143.root, FC#0, port D2
Entries 371
Mean 44.66
Std Dev 11.45
Turn on : 27.8828
Width : 1.329
Height : 10.004
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

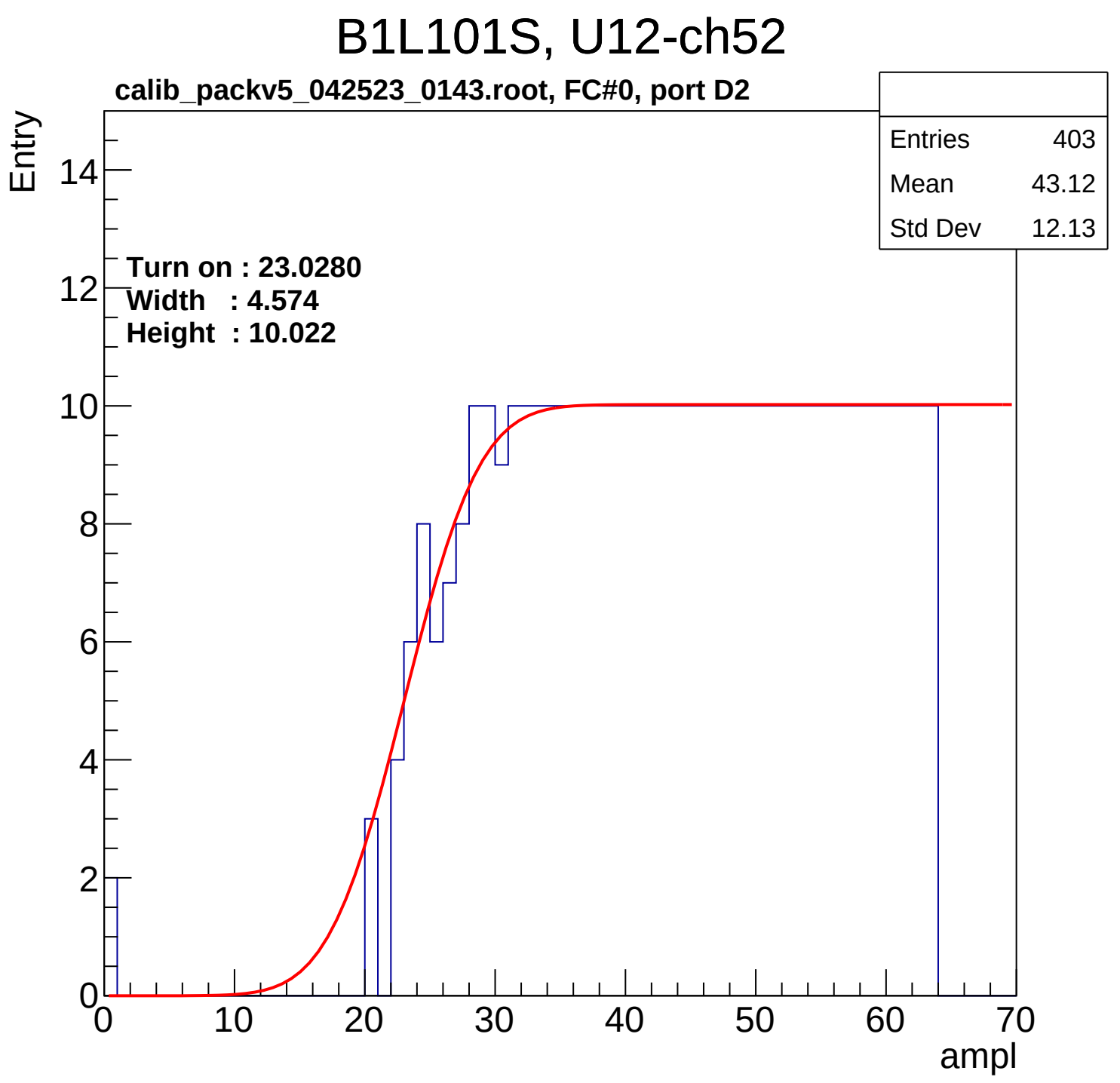

B1L101S, U12-ch47
calib_packv5_042523_0143.root, FC#0, port D2
Entries 369
Mean 44.66
Std Dev 11.63
Turn on : 27.7873
Width : 3.324
Height : 10.047
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

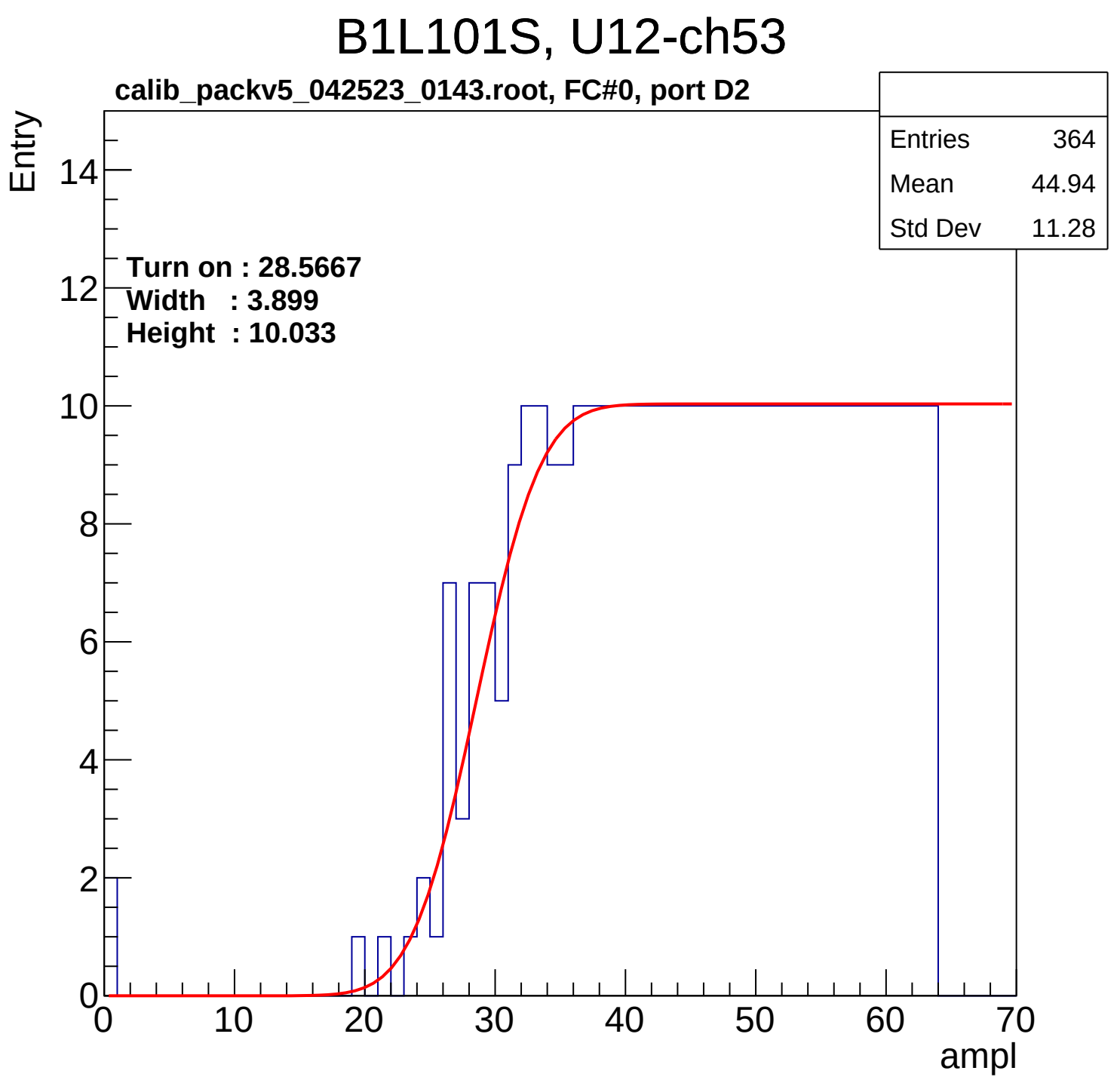

B1L101S, U12-ch48
calib_packv5_042523_0143.root, FC#0, port D2
Entries 370
Mean 44.53
Std Dev 11.86
Turn on : 27.3528
Width : 3.091
Height : 10.002
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

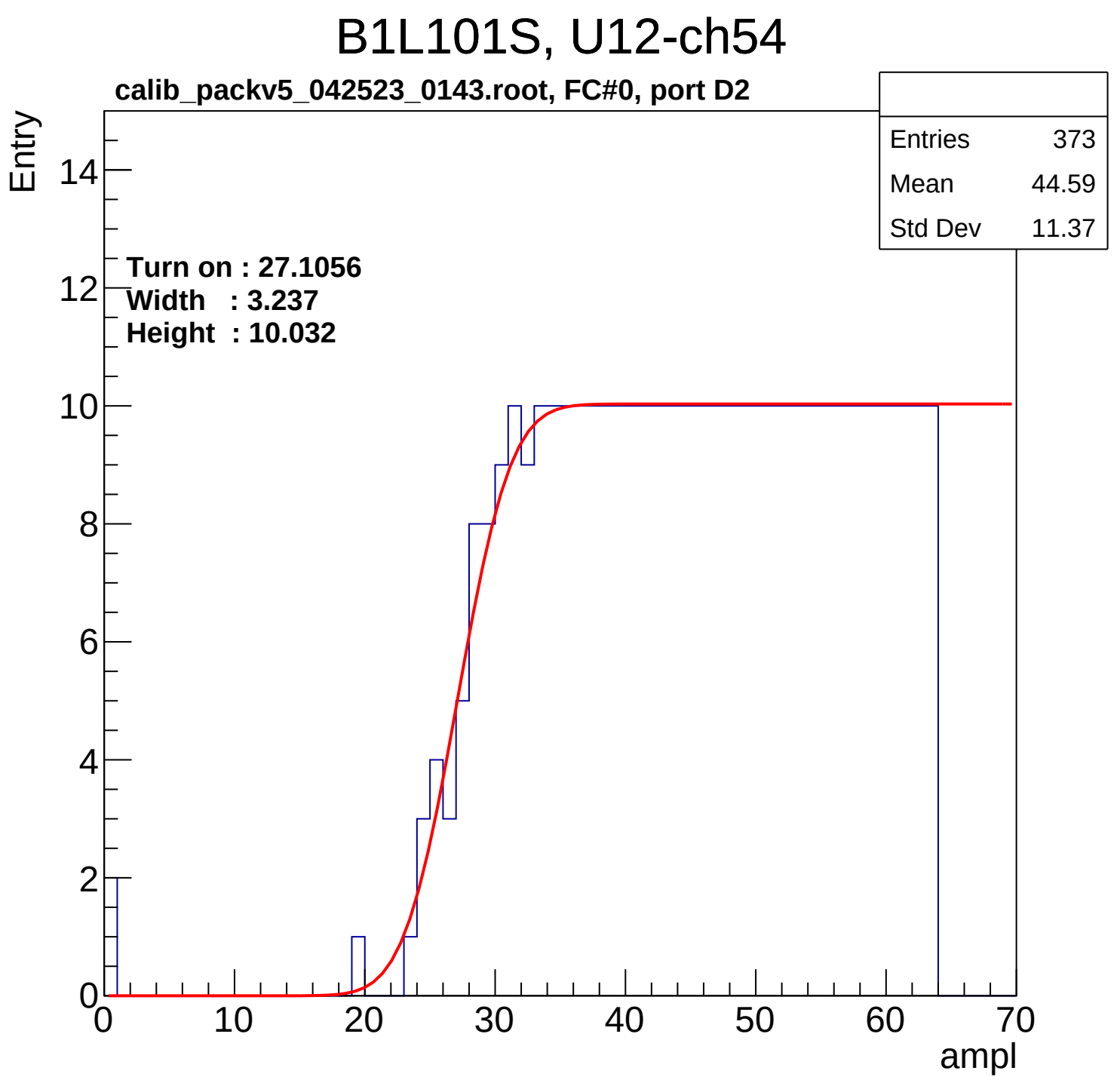

B1L101S, U12-ch49
calib_packv5_042523_0143.root, FC#0, port D2
Entries 343
Mean 46.08
Std Dev 10.58
Turn on : 30.1395
Width : 2.941
Height : 10.057
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

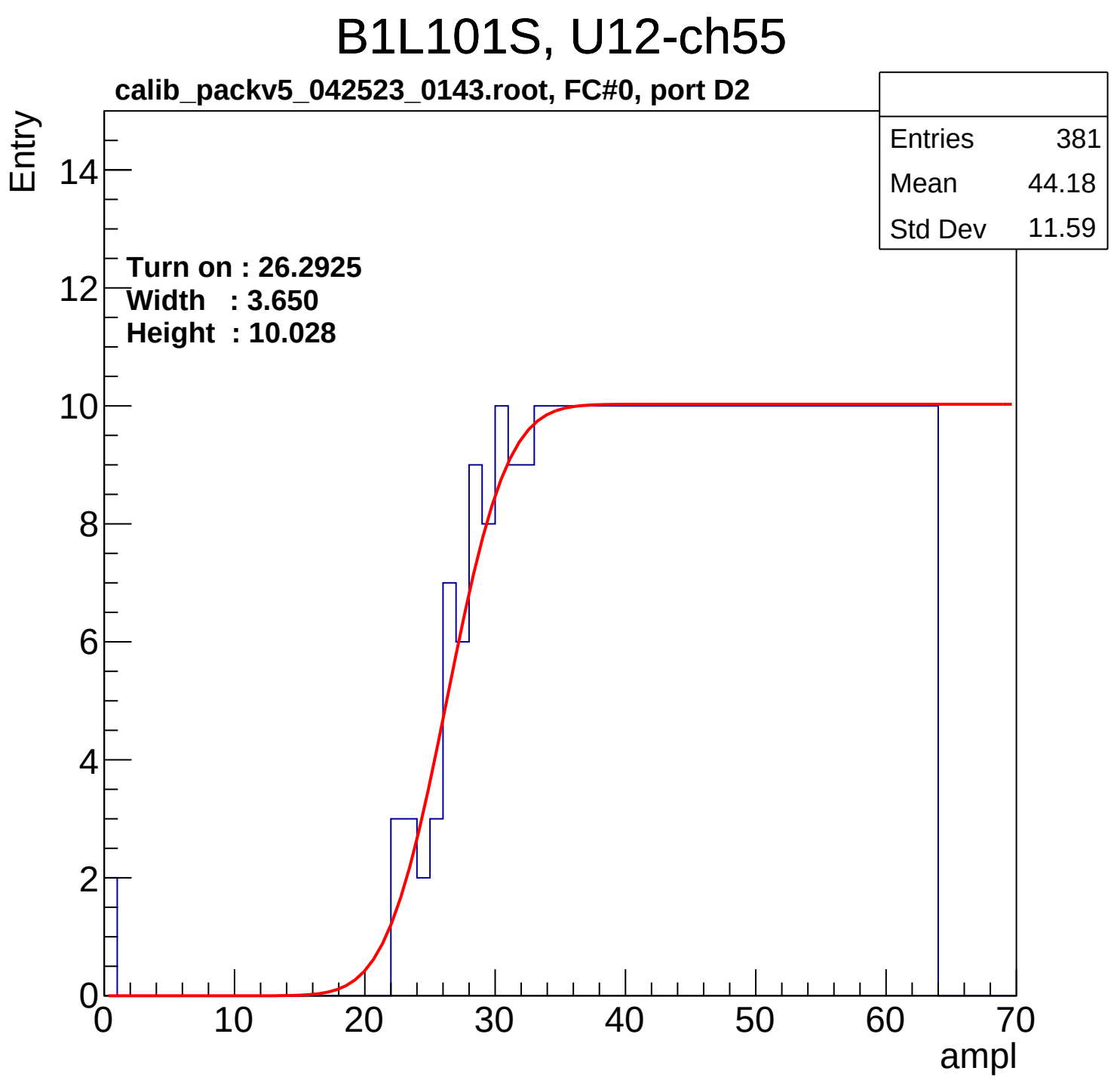

B1L101S, U12-ch50
calib_packv5_042523_0143.root, FC#0, port D2
Entries 373
Mean 44.61
Std Dev 11.33
Turn on : 27.2152
Width : 3.075
Height : 10.045
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

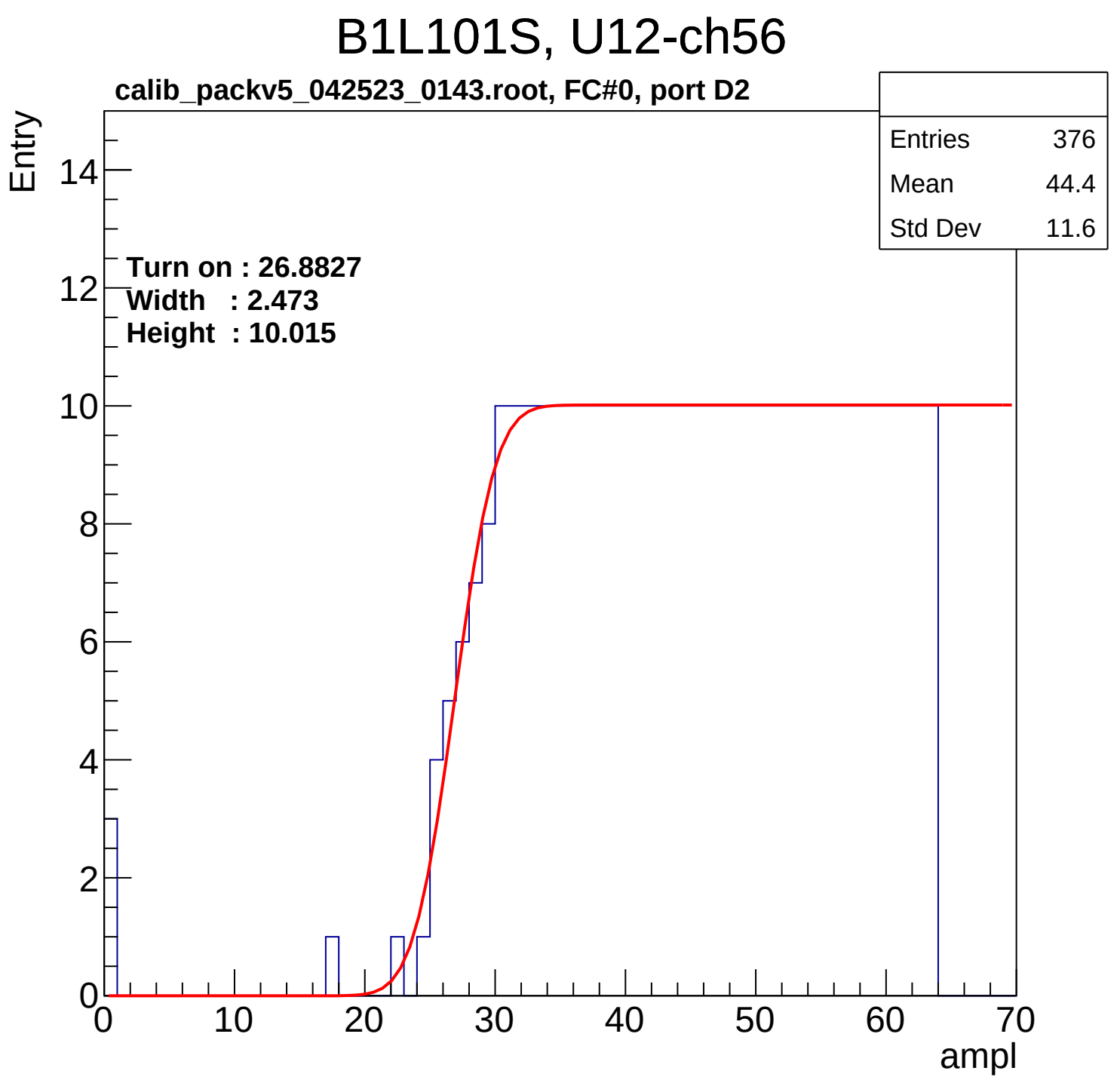

B1L101S, U12-ch51
calib_packv5_042523_0143.root, FC#0, port D2
Entries 375
Mean 44.42
Std Dev 11.62
Turn on : 26.8158
Width : 3.562
Height : 10.036
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

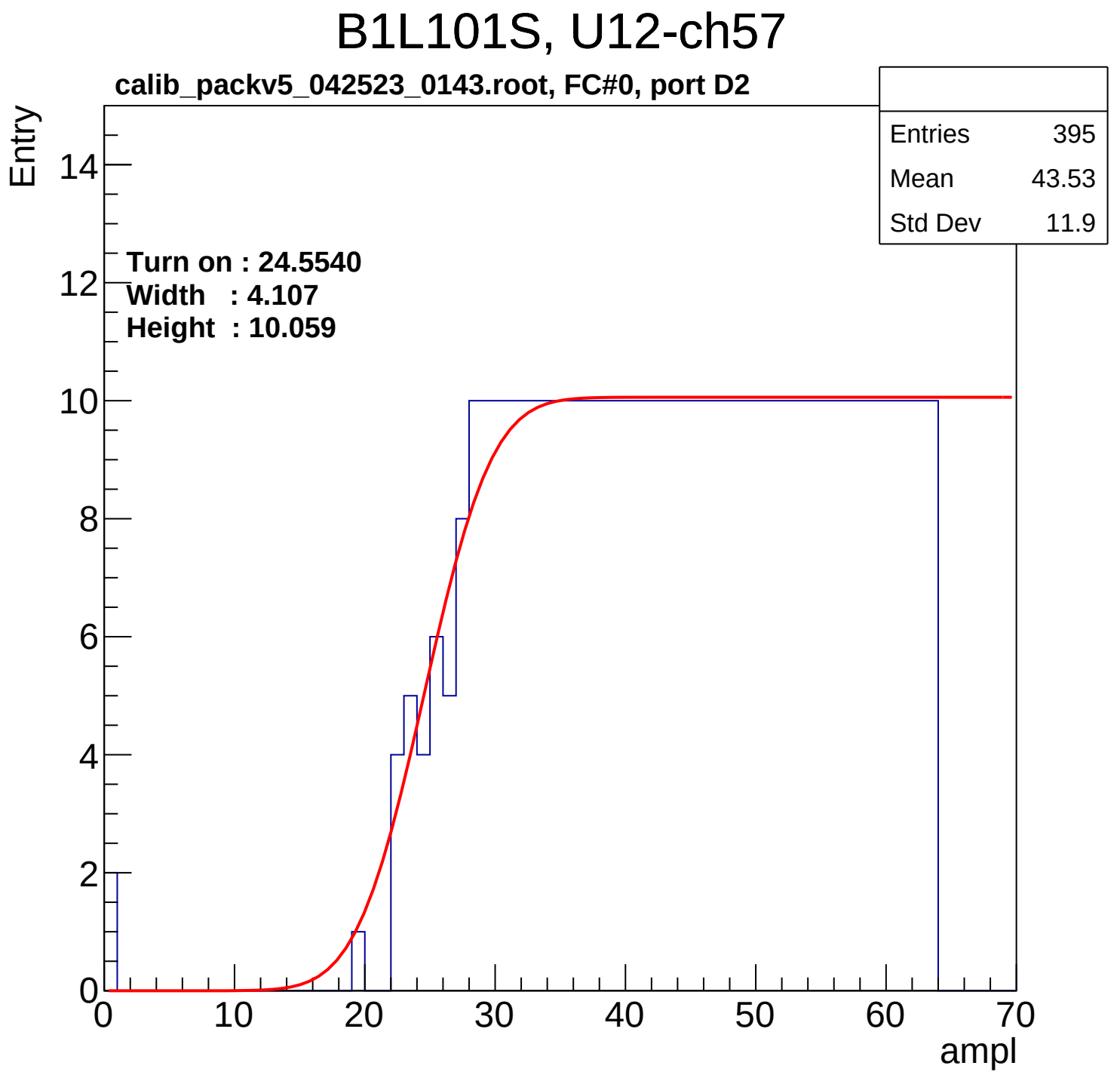

B1L101S, U12-ch52
calib_packv5_042523_0143.root, FC#0, port D2
Entries 403
Mean 43.12
Std Dev 12.13
Turn on : 23.0280
Width : 4.574
Height : 10.022
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

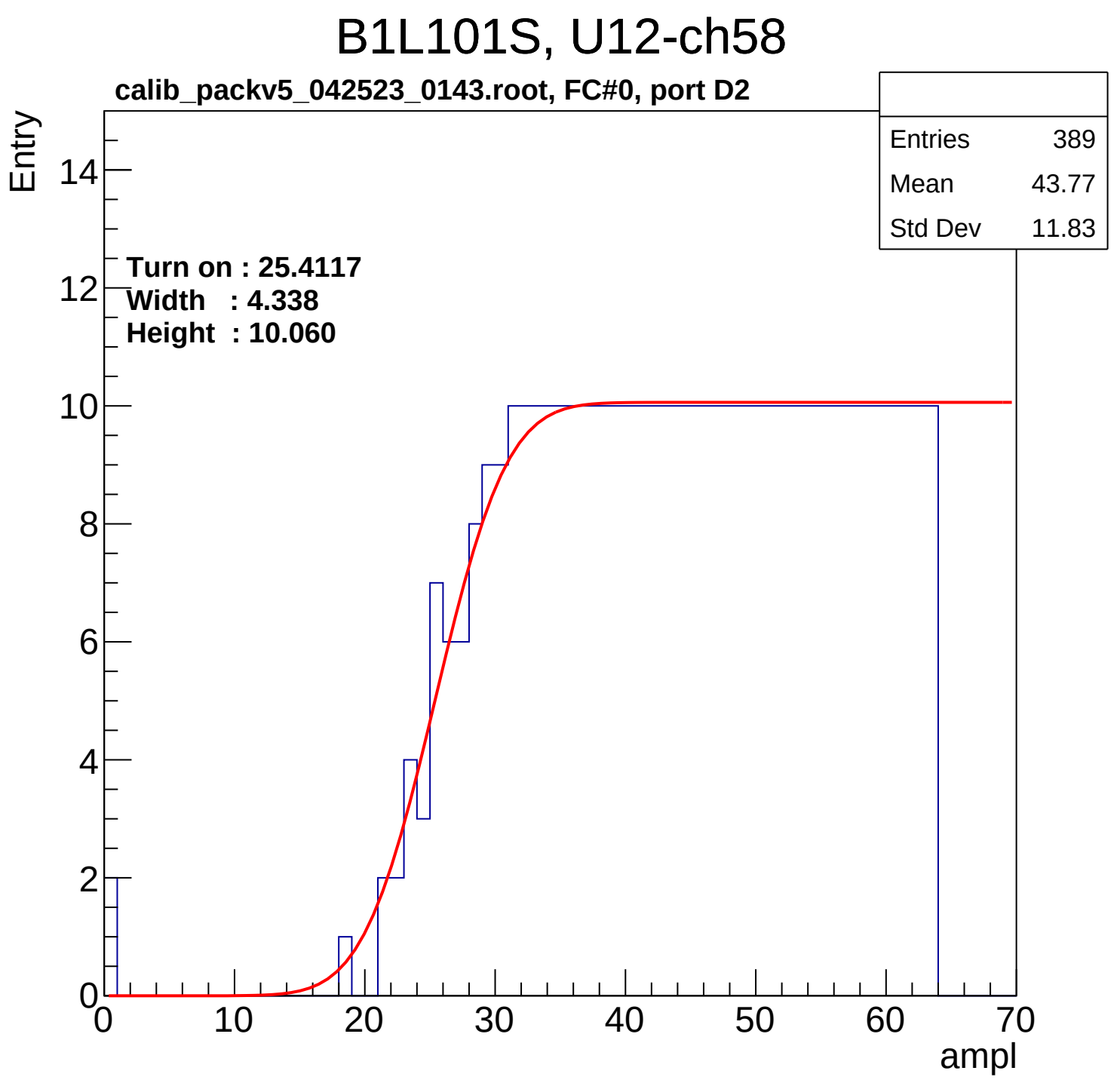

B1L101S, U12-ch53
calib_packv5_042523_0143.root, FC#0, port D2
Entries 364
Mean 44.94
Std Dev 11.28
Turn on : 28.5667
Width : 3.899
Height : 10.033
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

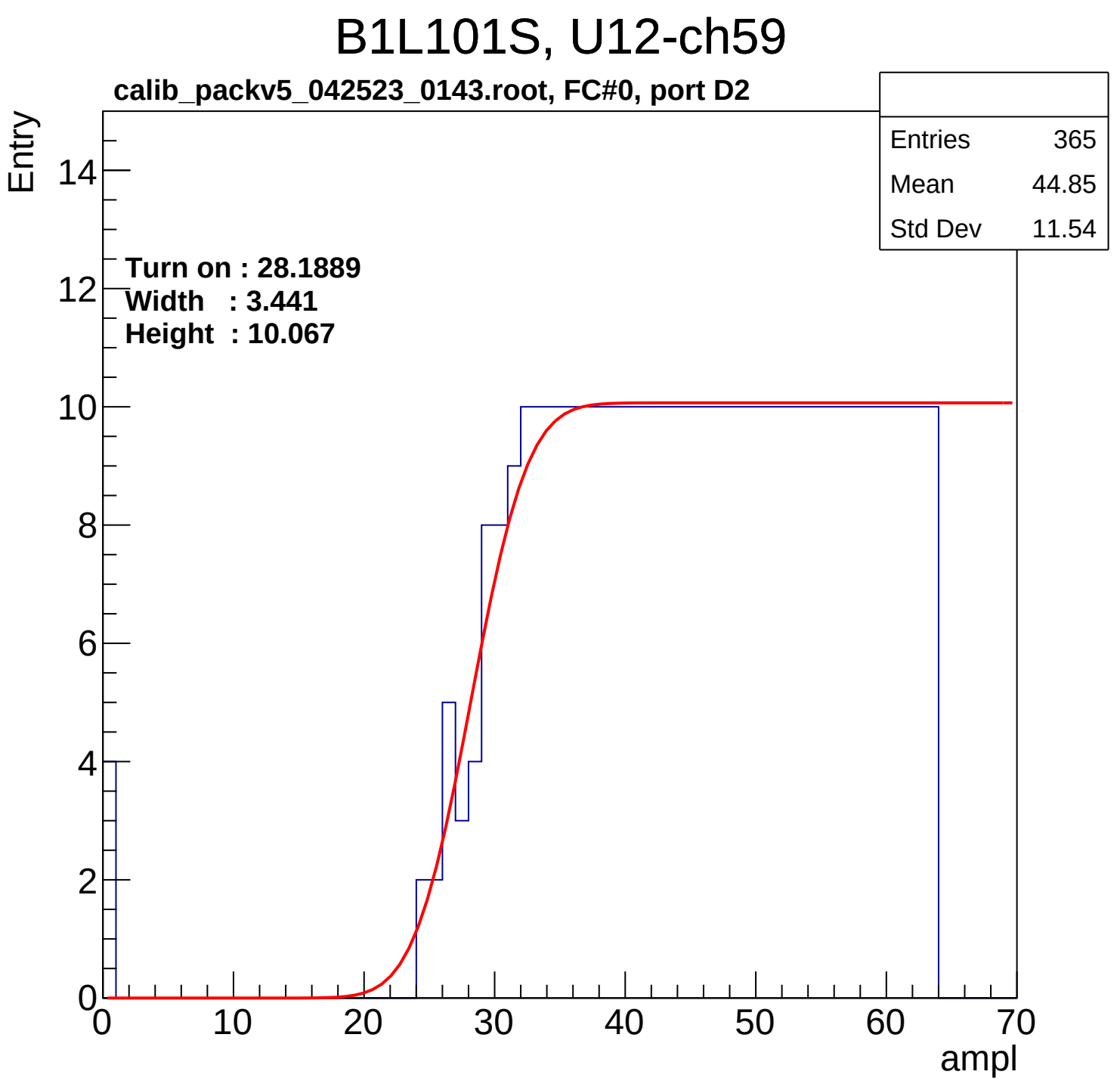

B1L101S, U12-ch54
calib_packv5_042523_0143.root, FC#0, port D2
Entries 373
Mean 44.59
Std Dev 11.37
Turn on : 27.1056
Width : 3.237
Height : 10.032
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

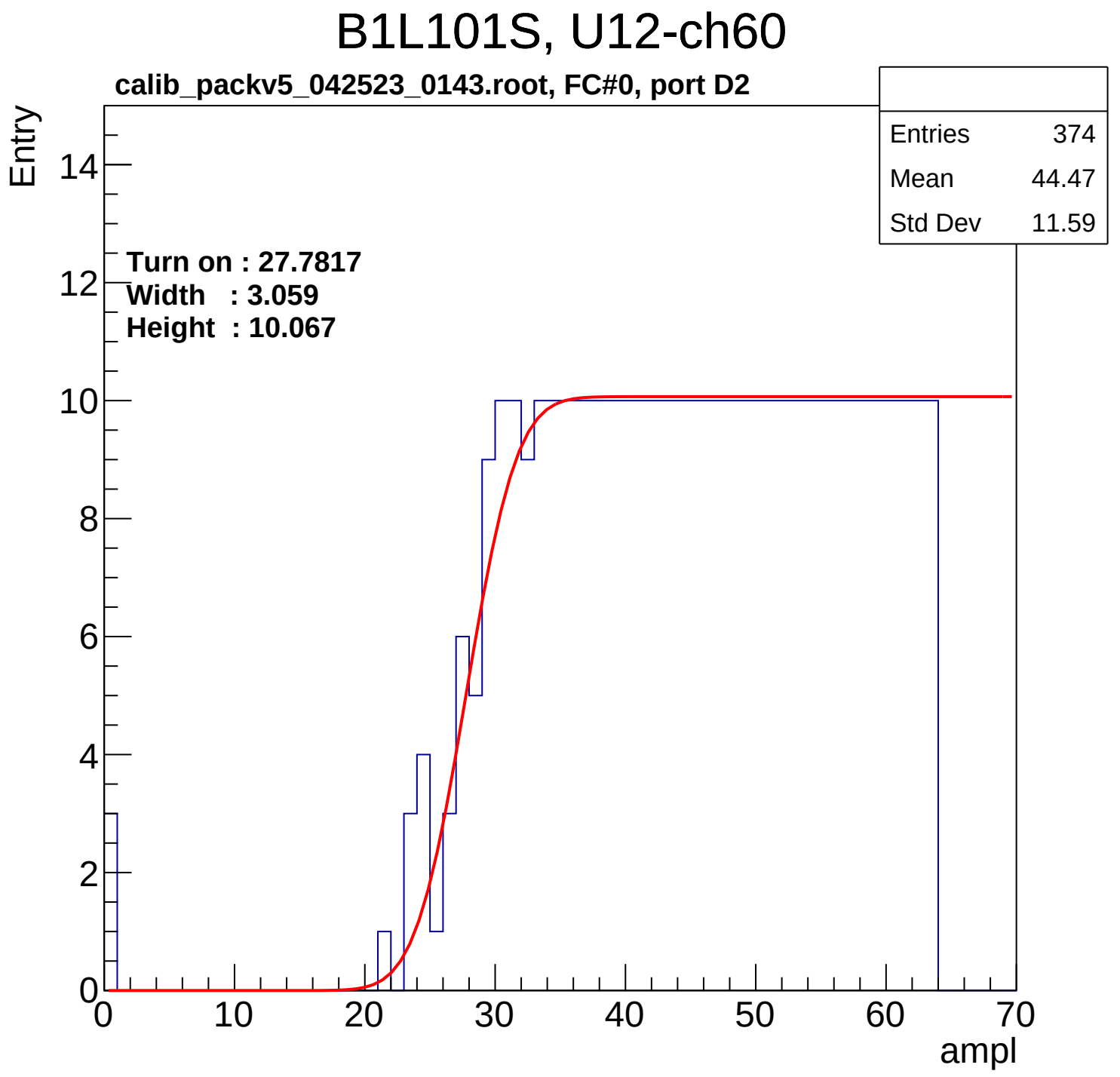

B1L101S, U12-ch55
calib_packv5_042523_0143.root, FC#0, port D2
Entries 381
Mean 44.18
Std Dev 11.59
Turn on : 26.2925
Width : 3.650
Height : 10.028
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

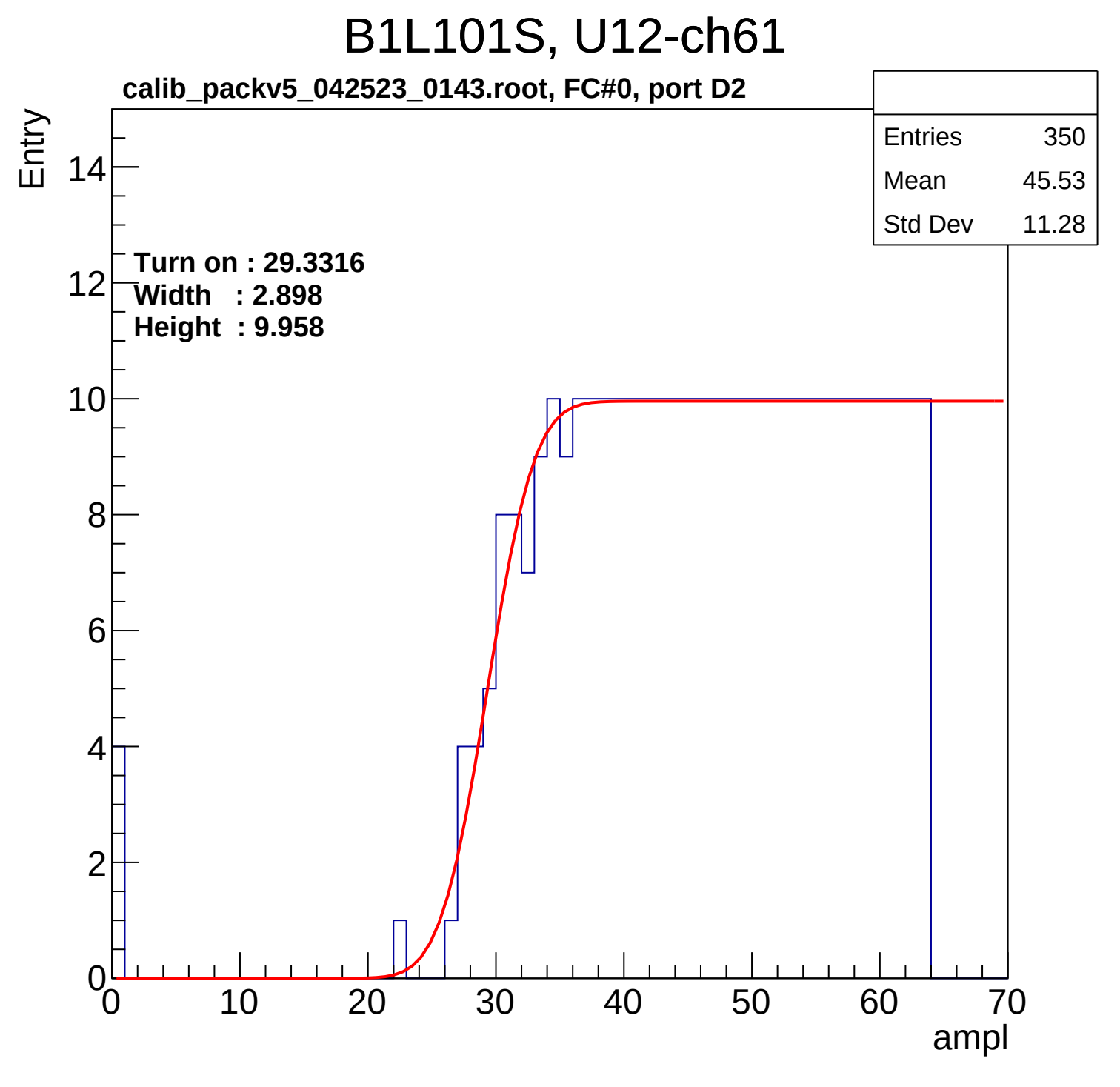

B1L101S, U12-ch56
calib_packv5_042523_0143.root, FC#0, port D2
Entries 376
Mean 44.4
Std Dev 11.6
Turn on : 26.8827
Width : 2.473
Height : 10.015
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

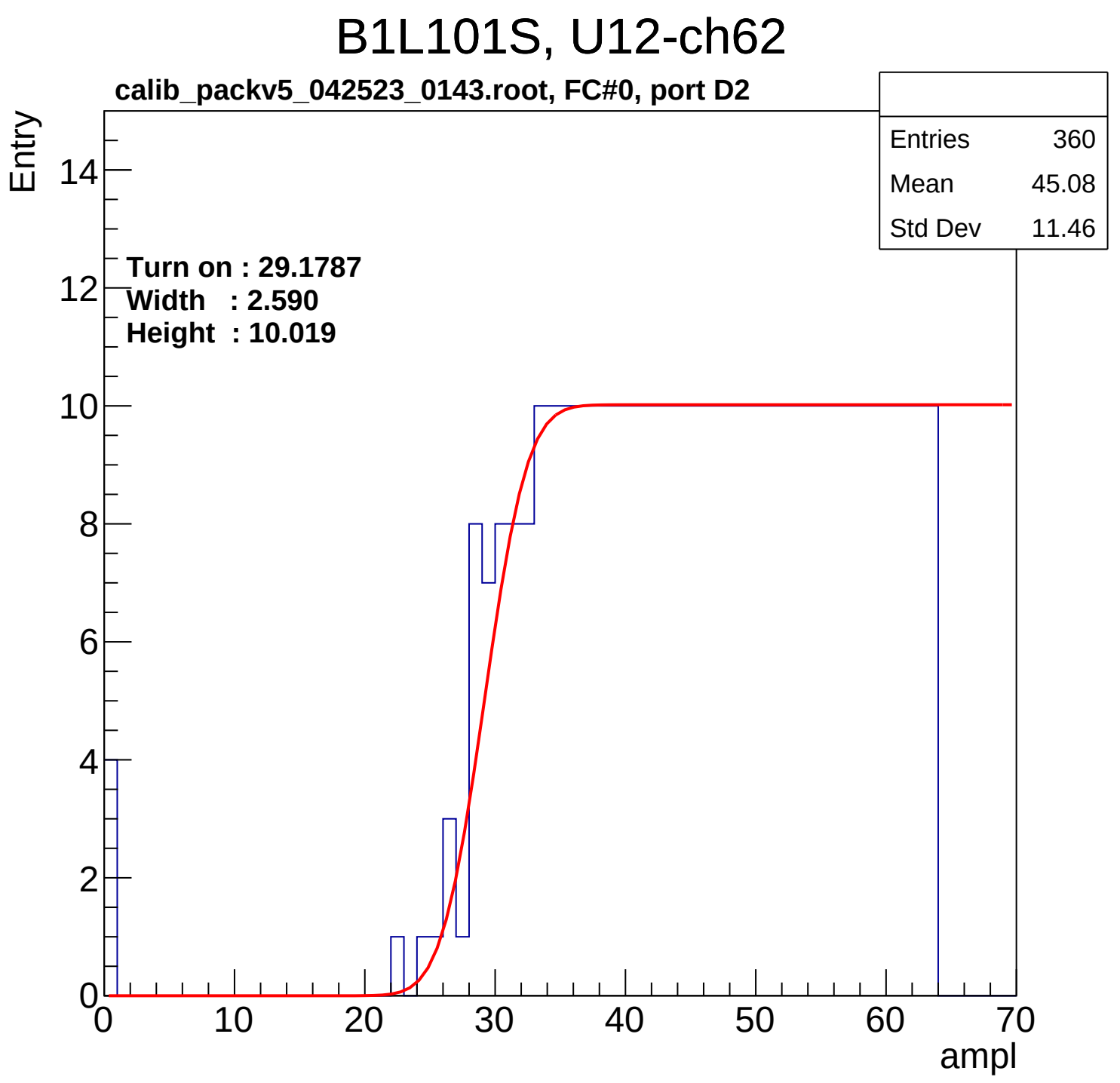

B1L101S, U12-ch57
calib_packv5_042523_0143.root, FC#0, port D2
Entries 395
Mean 43.53
Std Dev 11.9
Turn on : 24.5540
Width : 4.107
Height : 10.059
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

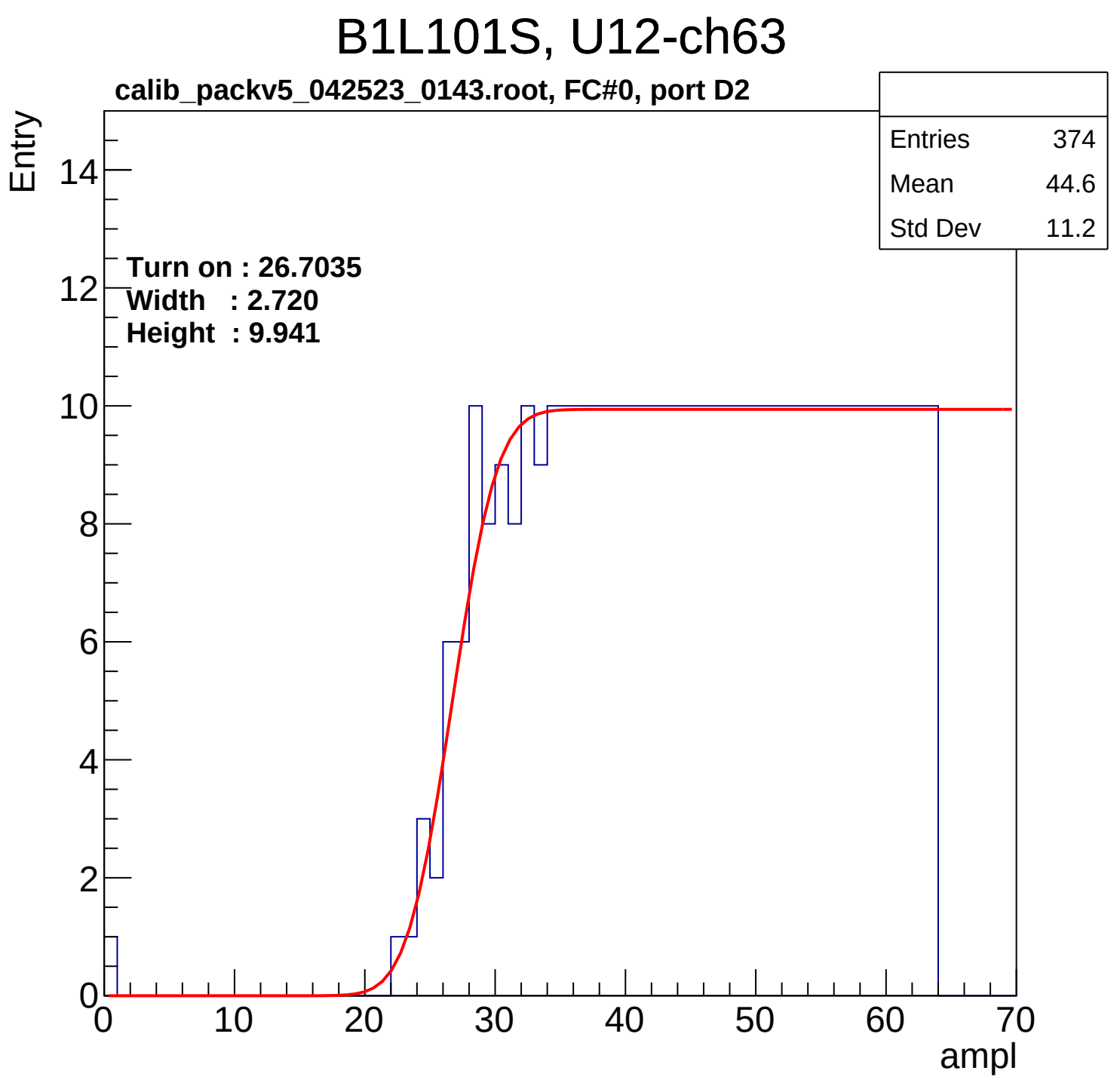

B1L101S, U12-ch58
calib_packv5_042523_0143.root, FC#0, port D2
Entries 389
Mean 43.77
Std Dev 11.83
Turn on : 25.4117
Width : 4.338
Height : 10.060
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

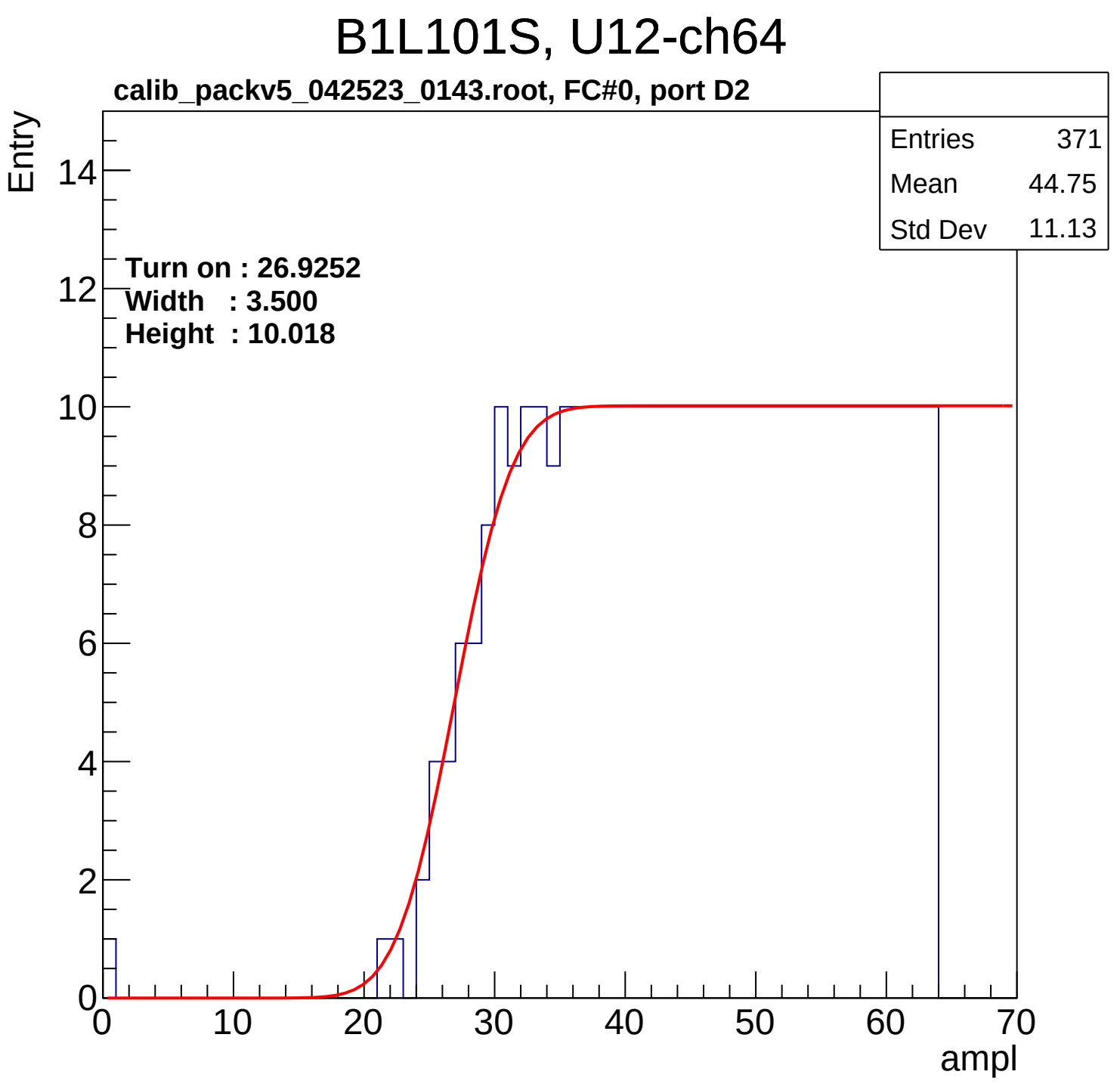

B1L101S, U12-ch59
calib_packv5_042523_0143.root, FC#0, port D2
Entries 365
Mean 44.85
Std Dev 11.54
Turn on : 28.1889
Width : 3.441
Height : 10.067
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

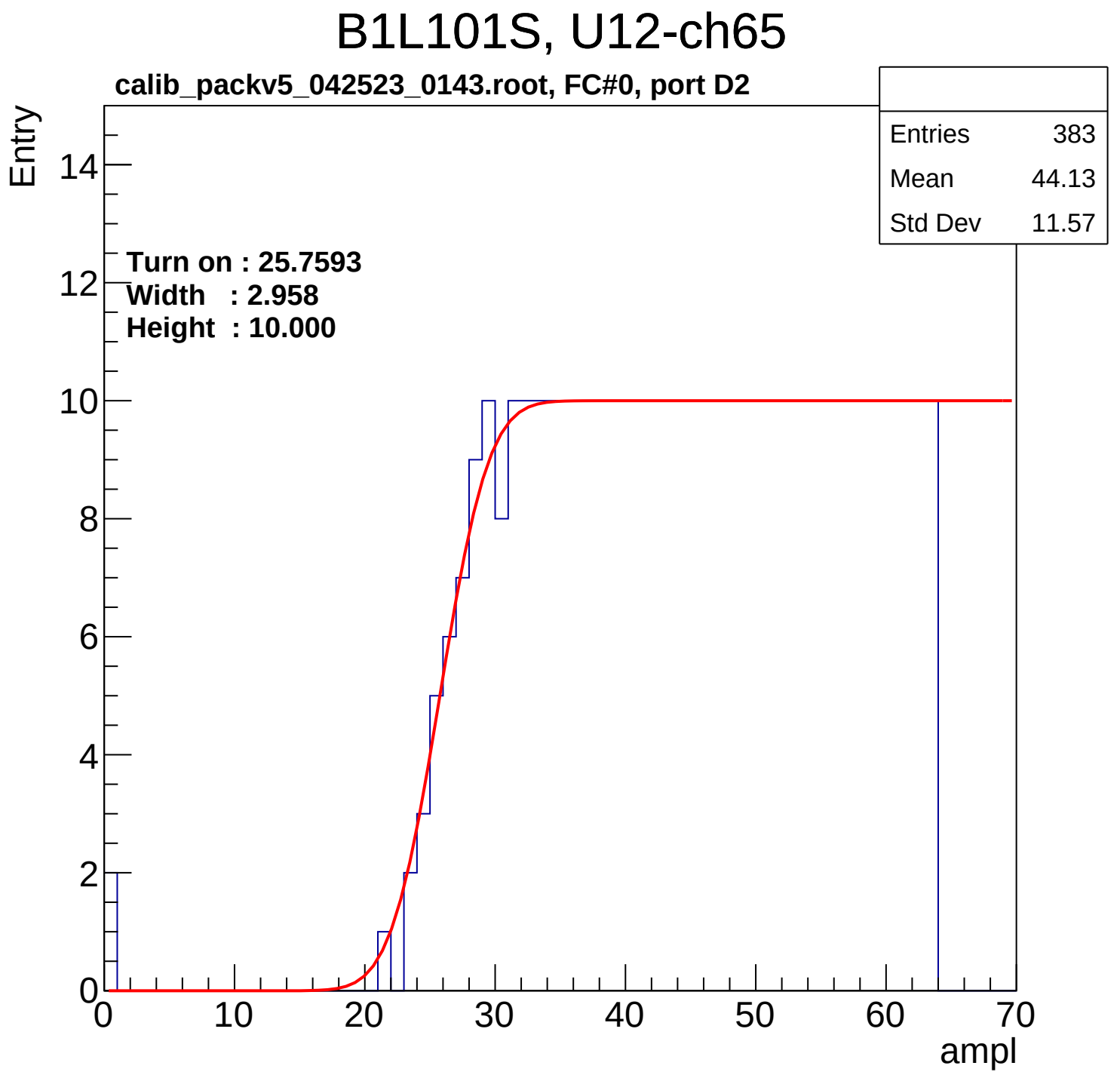

B1L101S, U12-ch60
calib_packv5_042523_0143.root, FC#0, port D2
Entries 374
Mean 44.47
Std Dev 11.59
Turn on : 27.7817
Width : 3.059
Height : 10.067
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

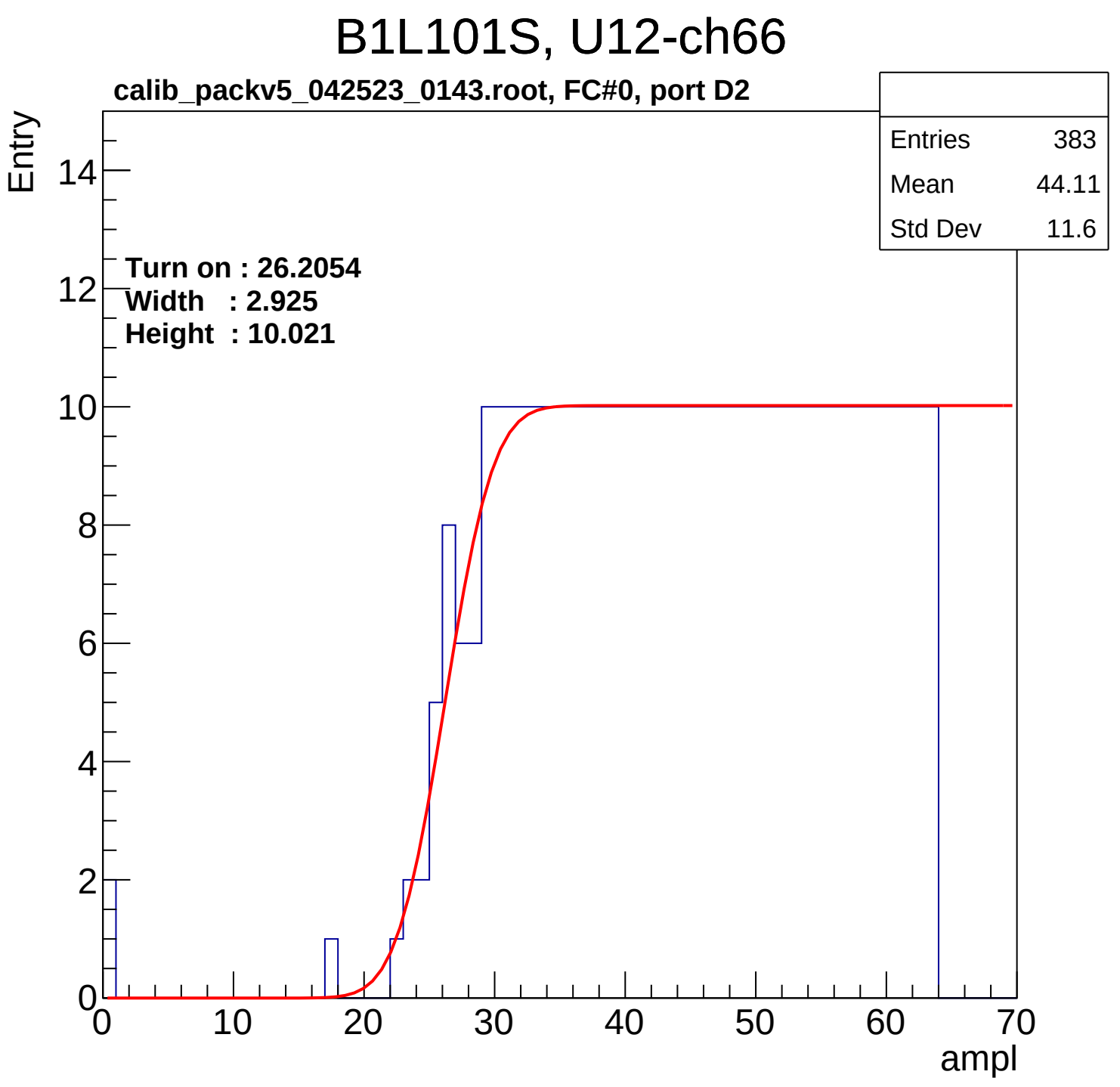

B1L101S, U12-ch61
calib_packv5_042523_0143.root, FC#0, port D2
Entries 350
Mean 45.53
Std Dev 11.28
Turn on : 29.3316
Width : 2.898
Height : 9.958
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

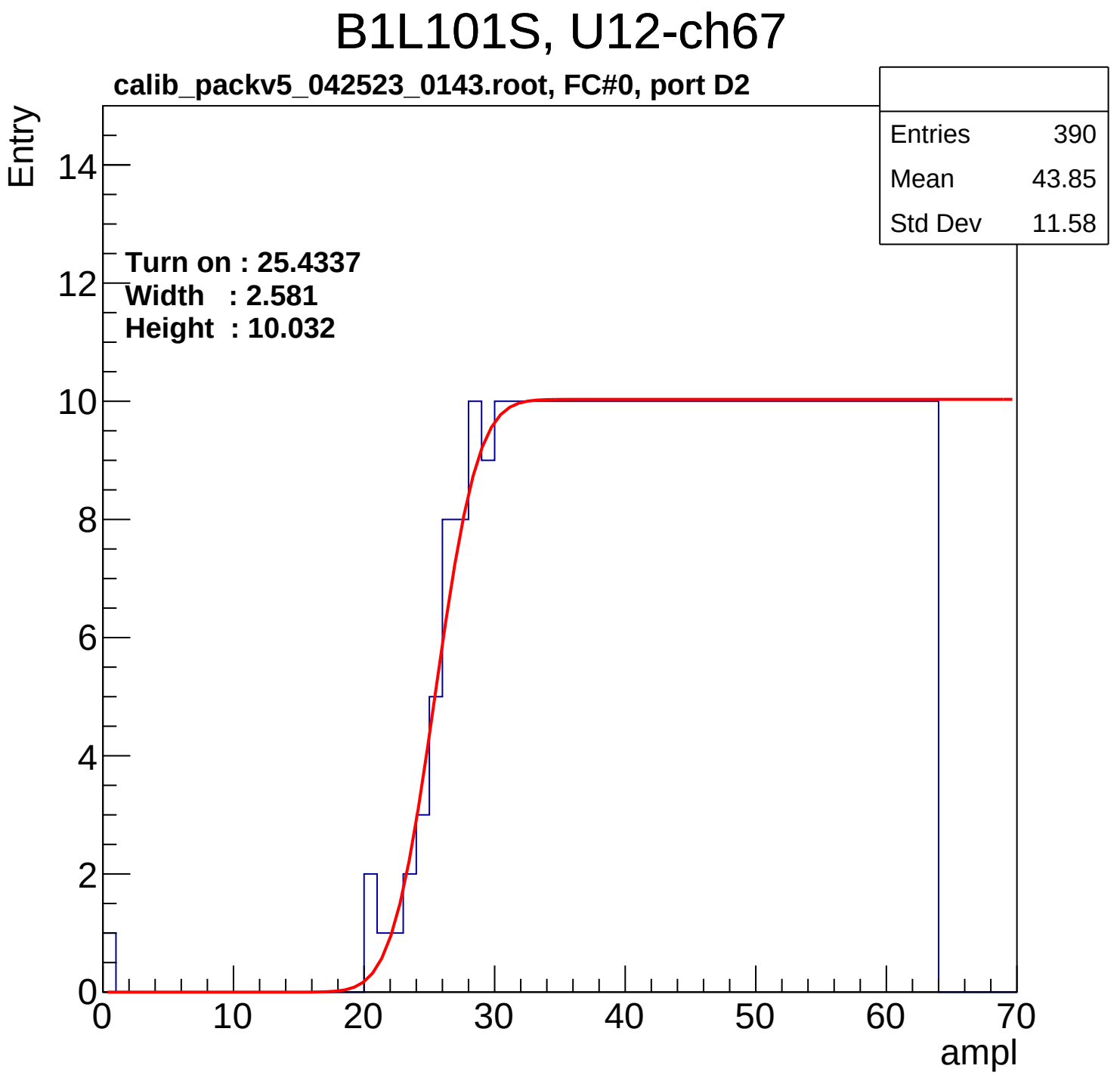

B1L101S, U12-ch62
calib_packv5_042523_0143.root, FC#0, port D2
Entries 360
Mean 45.08
Std Dev 11.46
Turn on : 29.1787
Width : 2.590
Height : 10.019
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

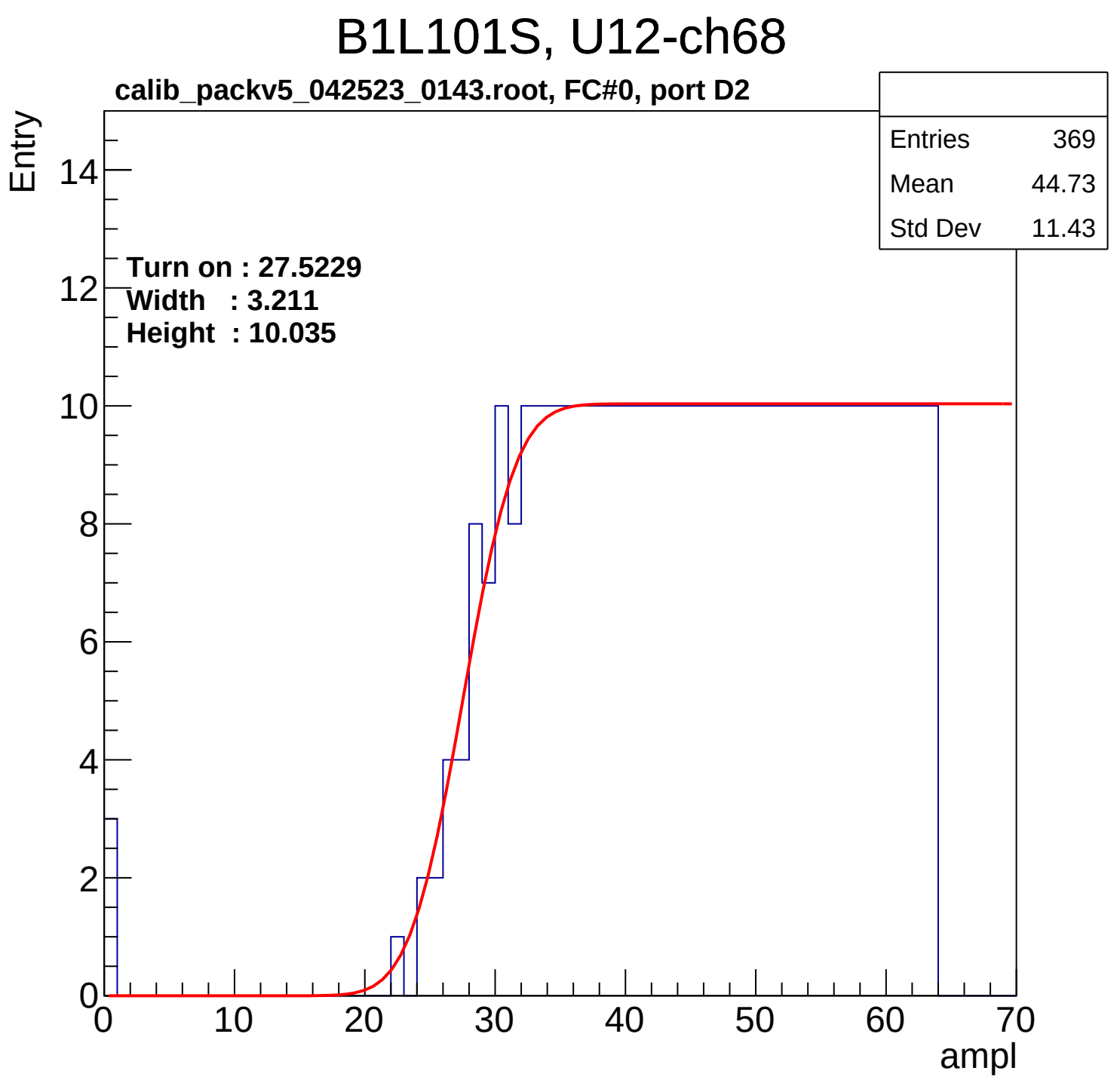

B1L101S, U12-ch63
calib_packv5_042523_0143.root, FC#0, port D2
Entries 374
Mean 44.6
Std Dev 11.2
Turn on : 26.7035
Width : 2.720
Height : 9.941
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

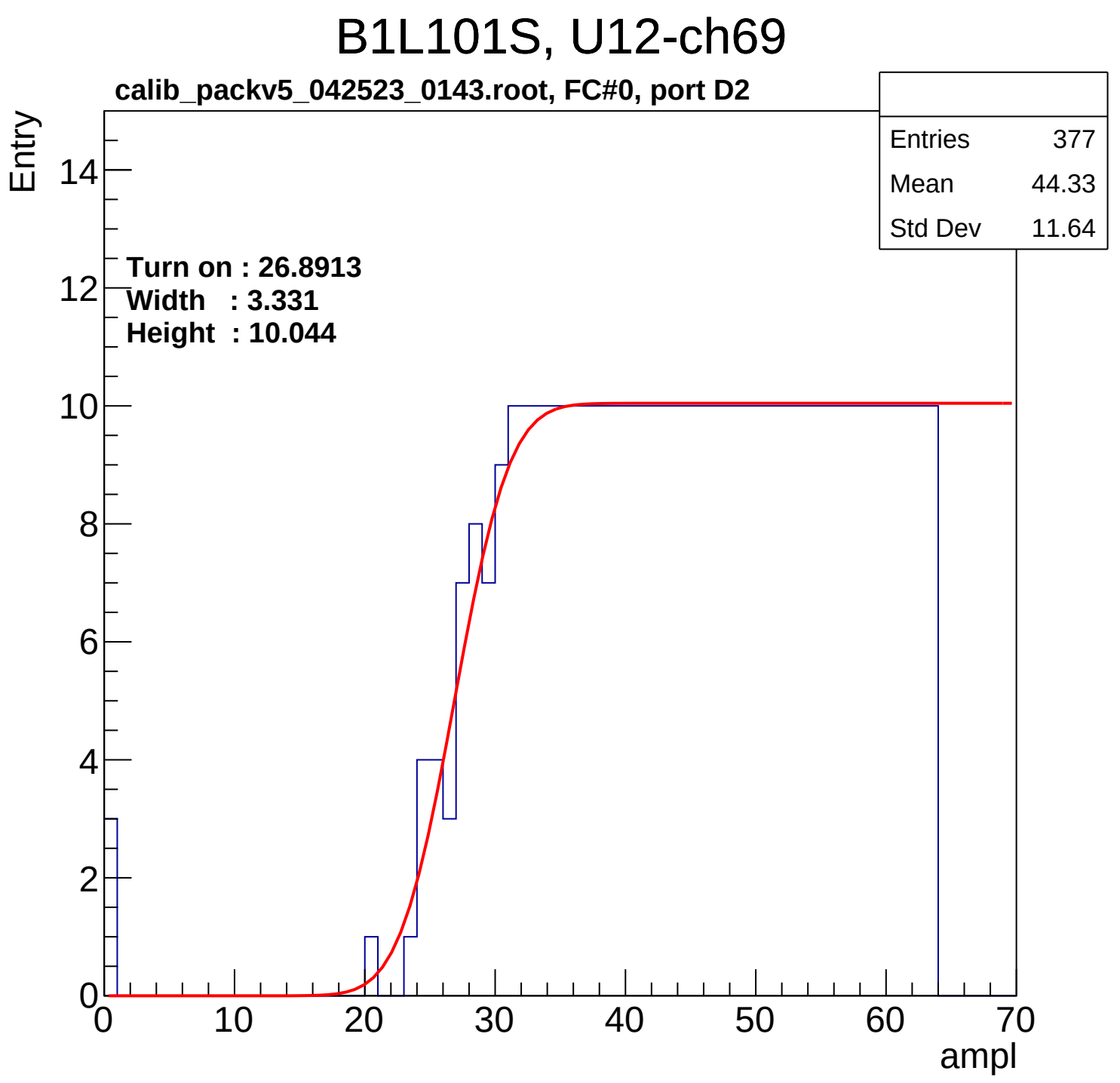

B1L101S, U12-ch64
calib_packv5_042523_0143.root, FC#0, port D2
Entries 371
Mean 44.75
Std Dev 11.13
Turn on : 26.9252
Width : 3.500
Height : 10.018
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

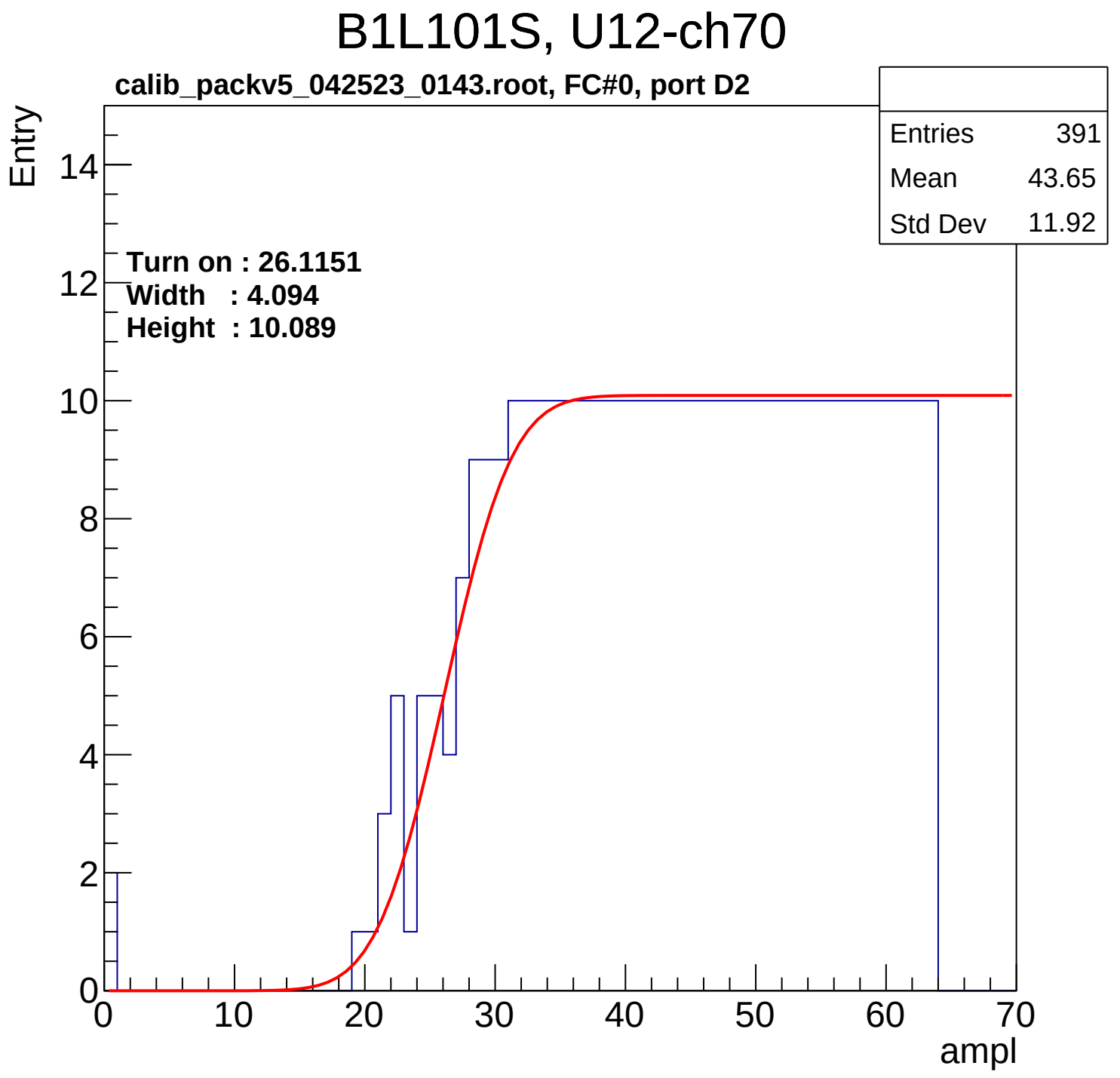

B1L101S, U12-ch65
calib_packv5_042523_0143.root, FC#0, port D2
Entries 383
Mean 44.13
Std Dev 11.57
Turn on : 25.7593
Width : 2.958
Height : 10.000
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

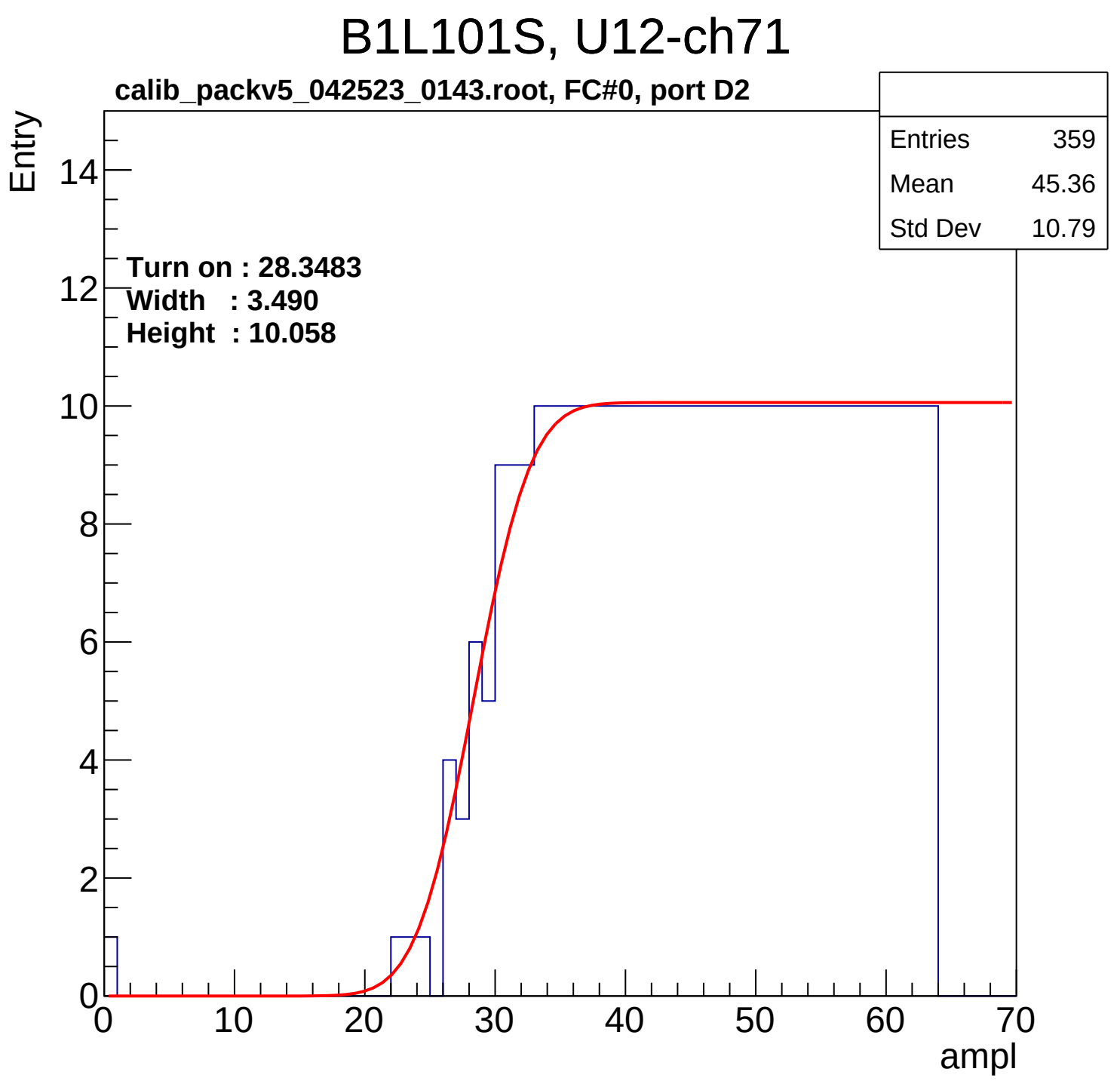

B1L101S, U12-ch66
calib_packv5_042523_0143.root, FC#0, port D2
Entries 383
Mean 44.11
Std Dev 11.6
Turn on : 26.2054
Width : 2.925
Height : 10.021
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

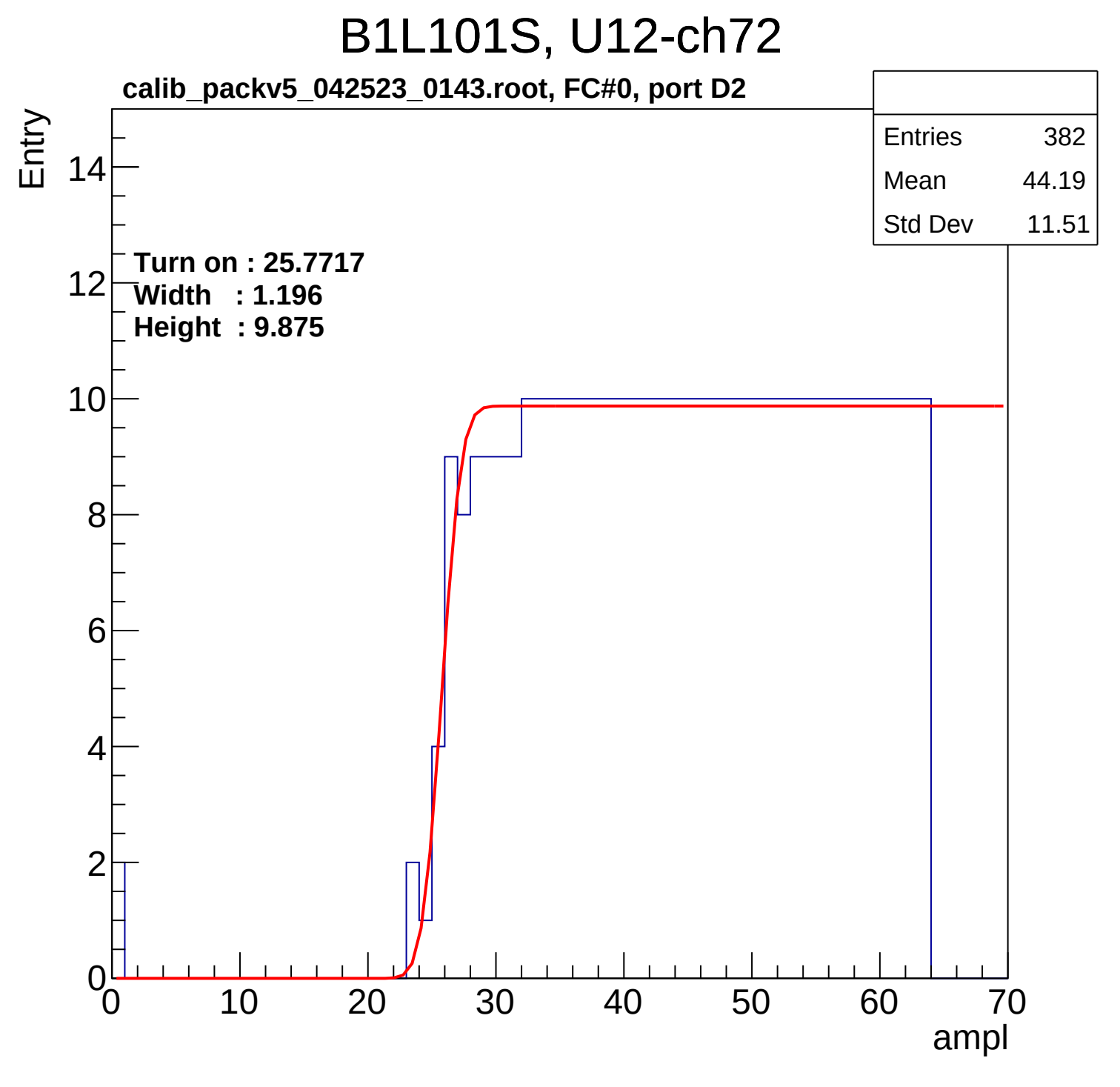

B1L101S, U12-ch67
calib_packv5_042523_0143.root, FC#0, port D2
Entries 390
Mean 43.85
Std Dev 11.58
Turn on : 25.4337
Width : 2.581
Height : 10.032
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

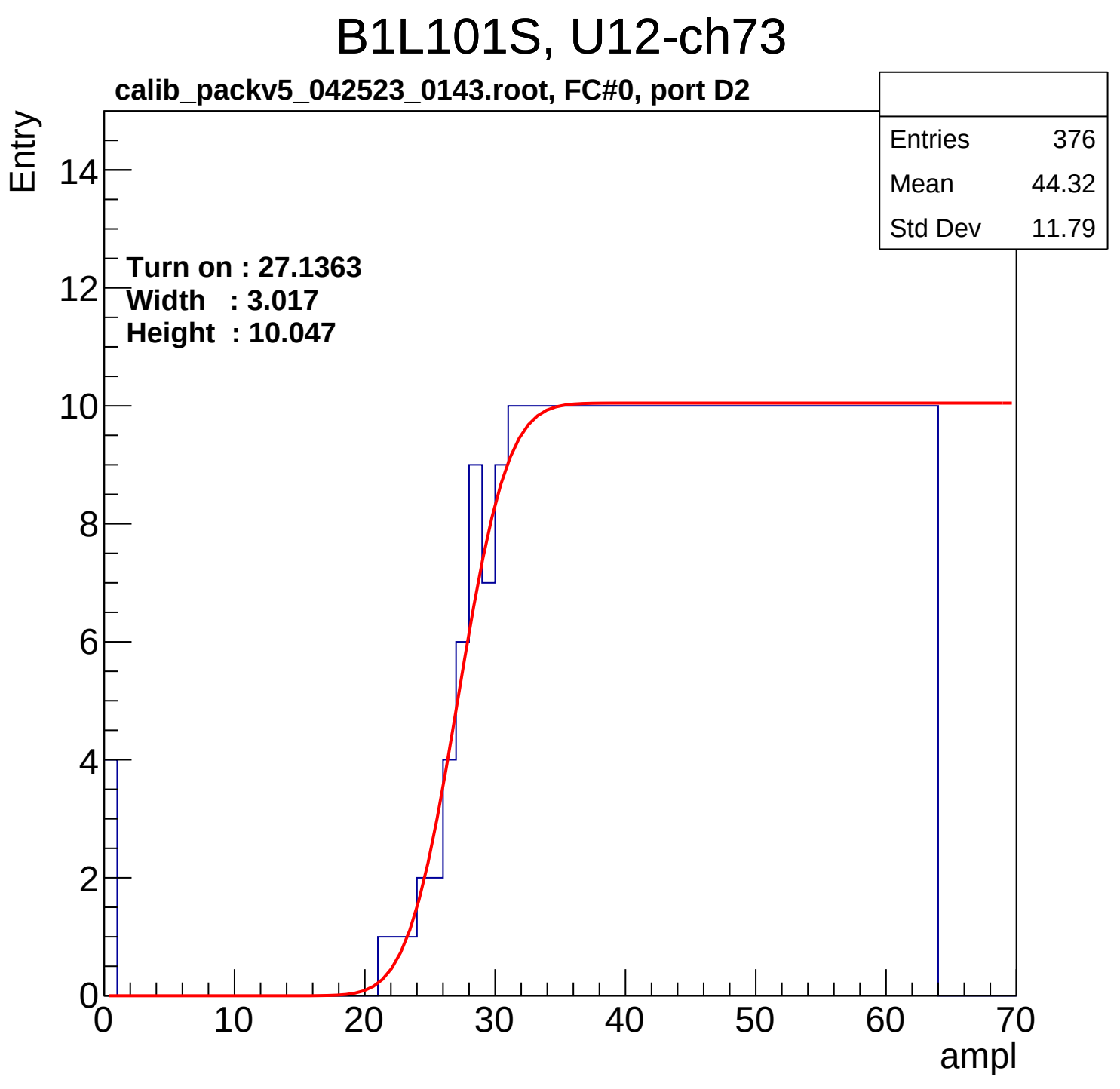

B1L101S, U12-ch68
calib_packv5_042523_0143.root, FC#0, port D2
Entries 369
Mean 44.73
Std Dev 11.43
Turn on : 27.5229
Width : 3.211
Height : 10.035
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

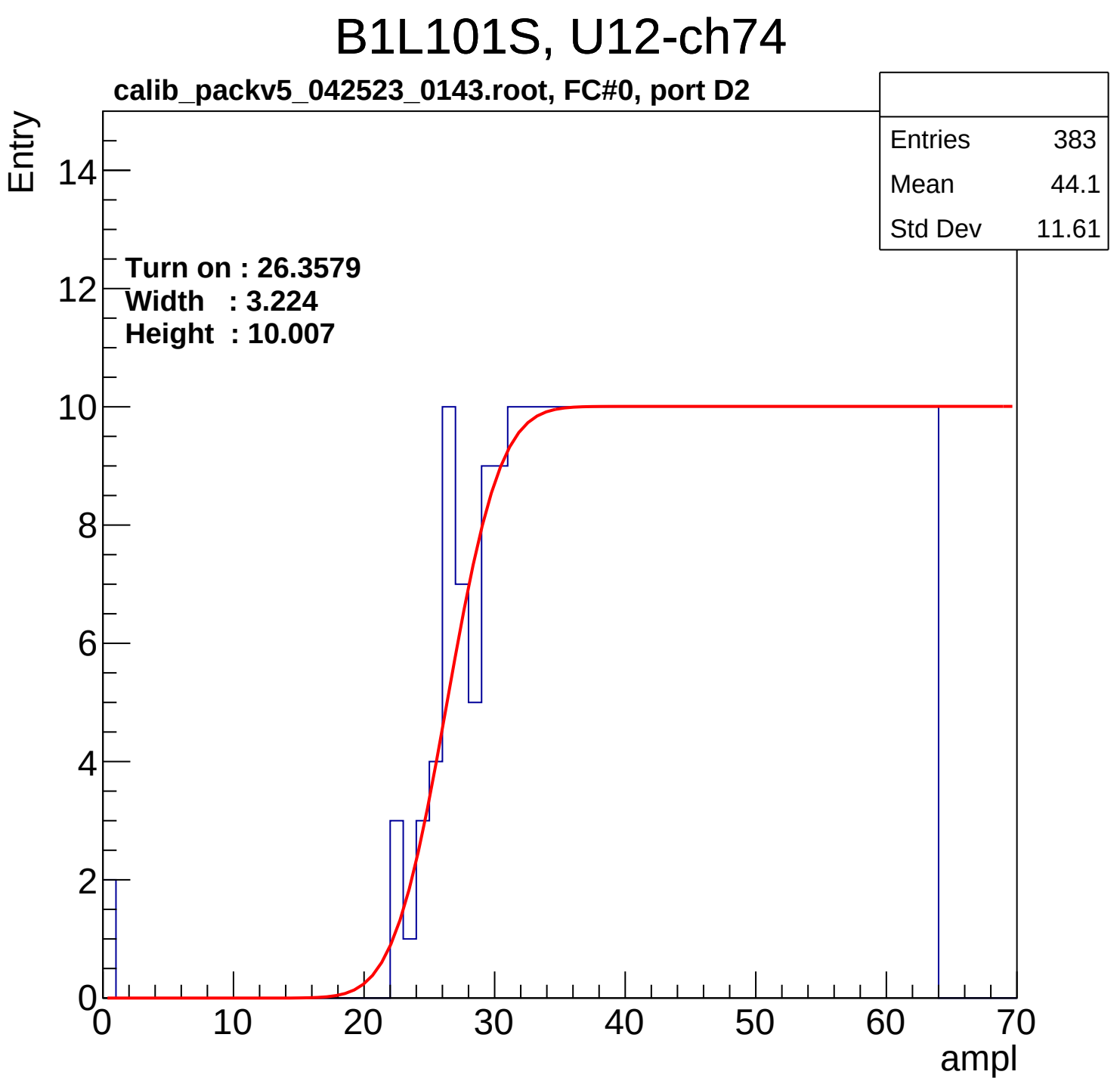

B1L101S, U12-ch69
calib_packv5_042523_0143.root, FC#0, port D2
Entries 377
Mean 44.33
Std Dev 11.64
Turn on : 26.8913
Width : 3.331
Height : 10.044
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

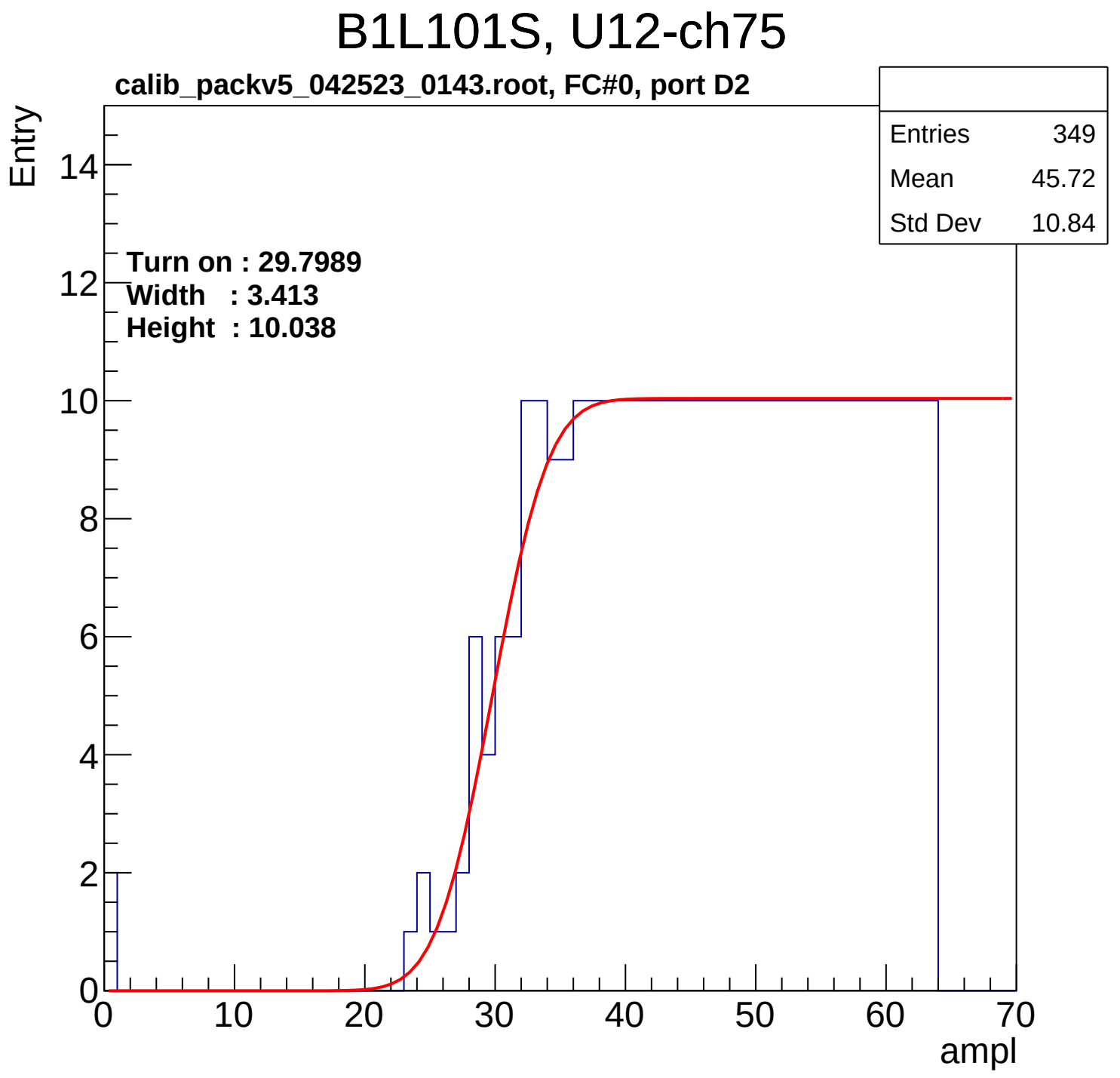

B1L101S, U12-ch70
calib_packv5_042523_0143.root, FC#0, port D2
Entries 391
Mean 43.65
Std Dev 11.92
Turn on : 26.1151
Width : 4.094
Height : 10.089
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

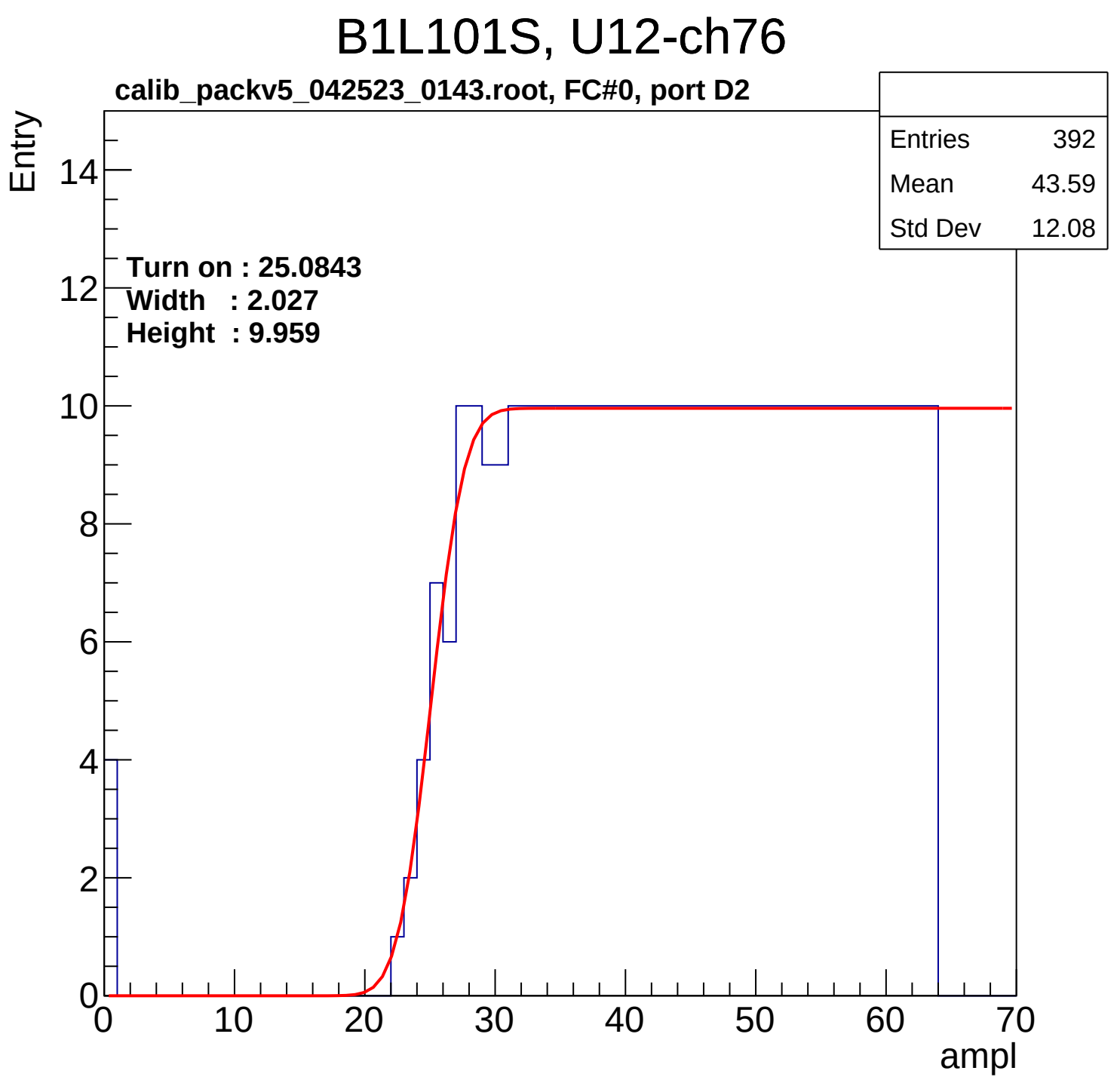

B1L101S, U12-ch71
calib_packv5_042523_0143.root, FC#0, port D2
Entries 359
Mean 45.36
Std Dev 10.79
Turn on : 28.3483
Width : 3.490
Height : 10.058
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

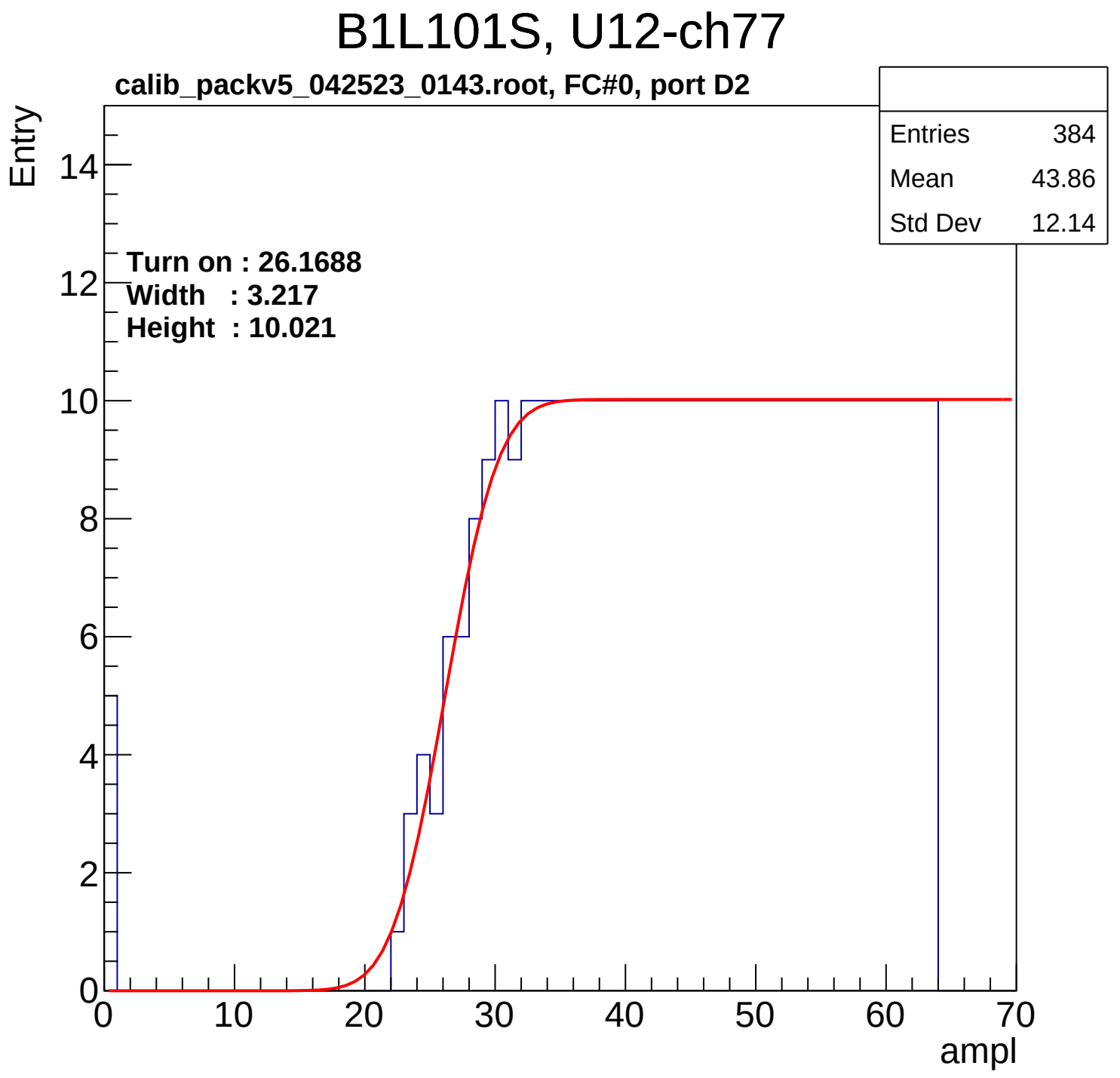

B1L101S, U12-ch72
calib_packv5_042523_0143.root, FC#0, port D2
Entries 382
Mean 44.19
Std Dev 11.51
Turn on : 25.7717
Width : 1.196
Height : 9.875
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

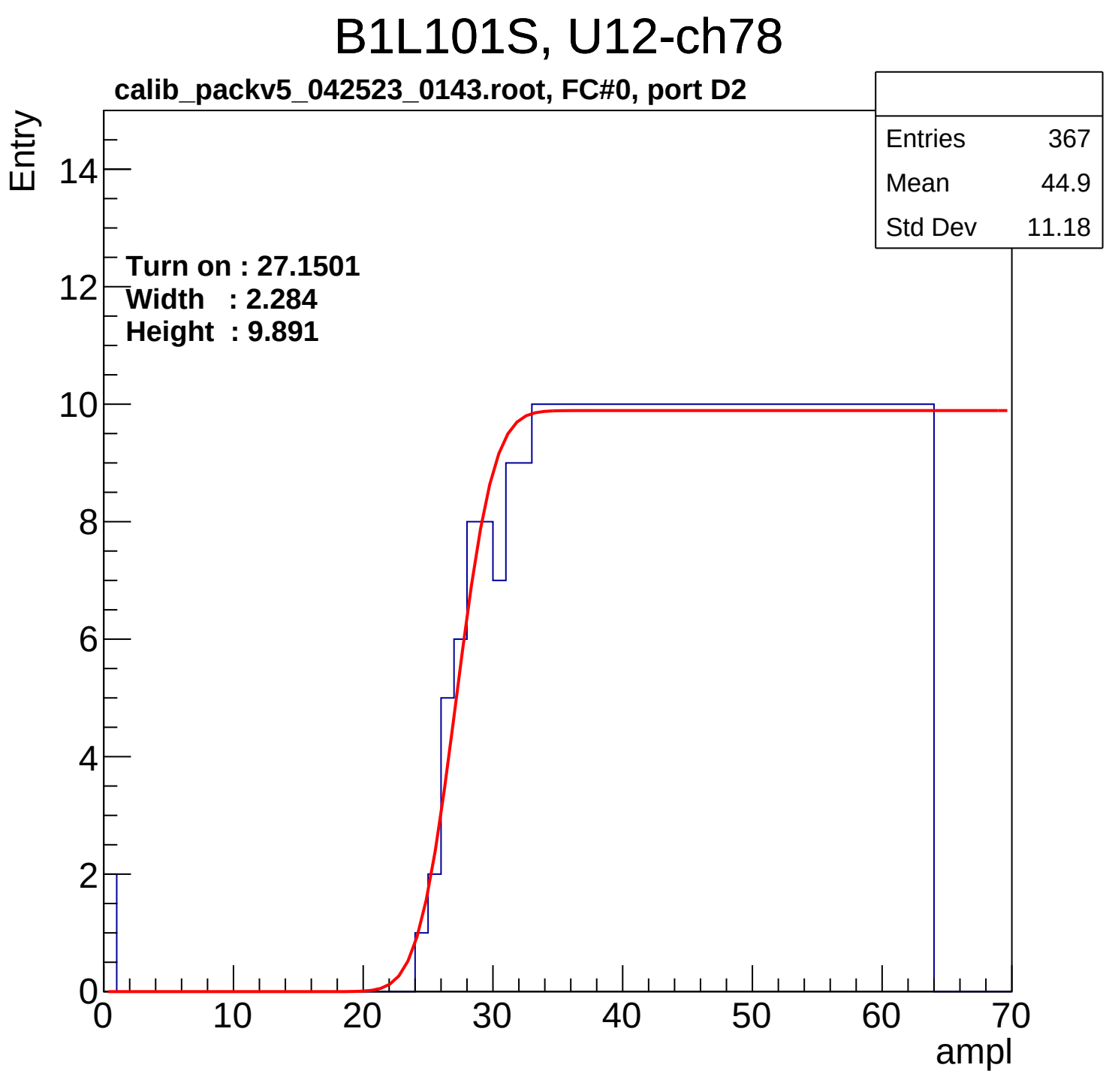

B1L101S, U12-ch73
calib_packv5_042523_0143.root, FC#0, port D2
Entries 376
Mean 44.32
Std Dev 11.79
Turn on : 27.1363
Width : 3.017
Height : 10.047
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

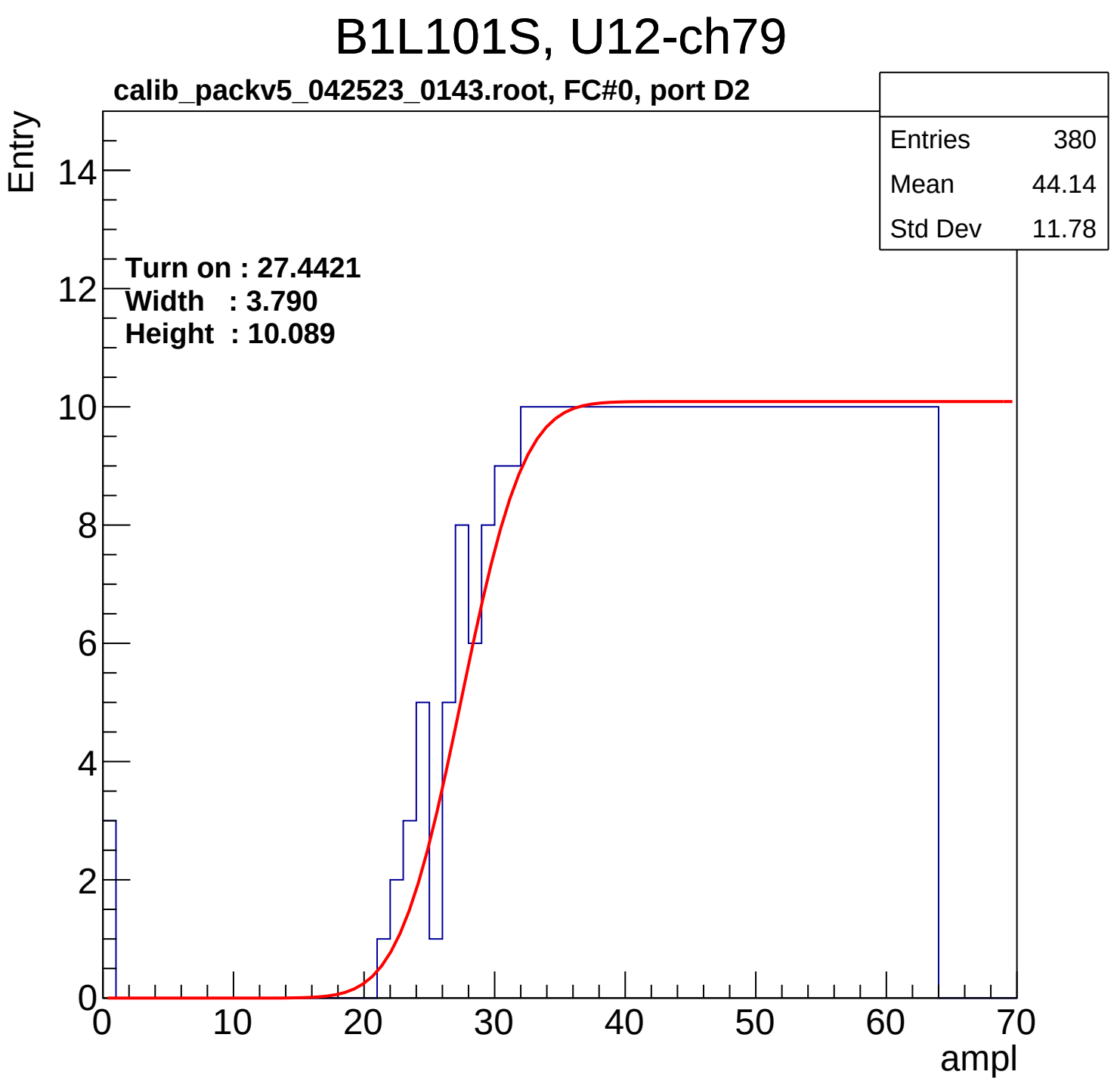

B1L101S, U12-ch74
calib_packv5_042523_0143.root, FC#0, port D2
Entries 383
Mean 44.1
Std Dev 11.61
Turn on : 26.3579
Width : 3.224
Height : 10.007
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

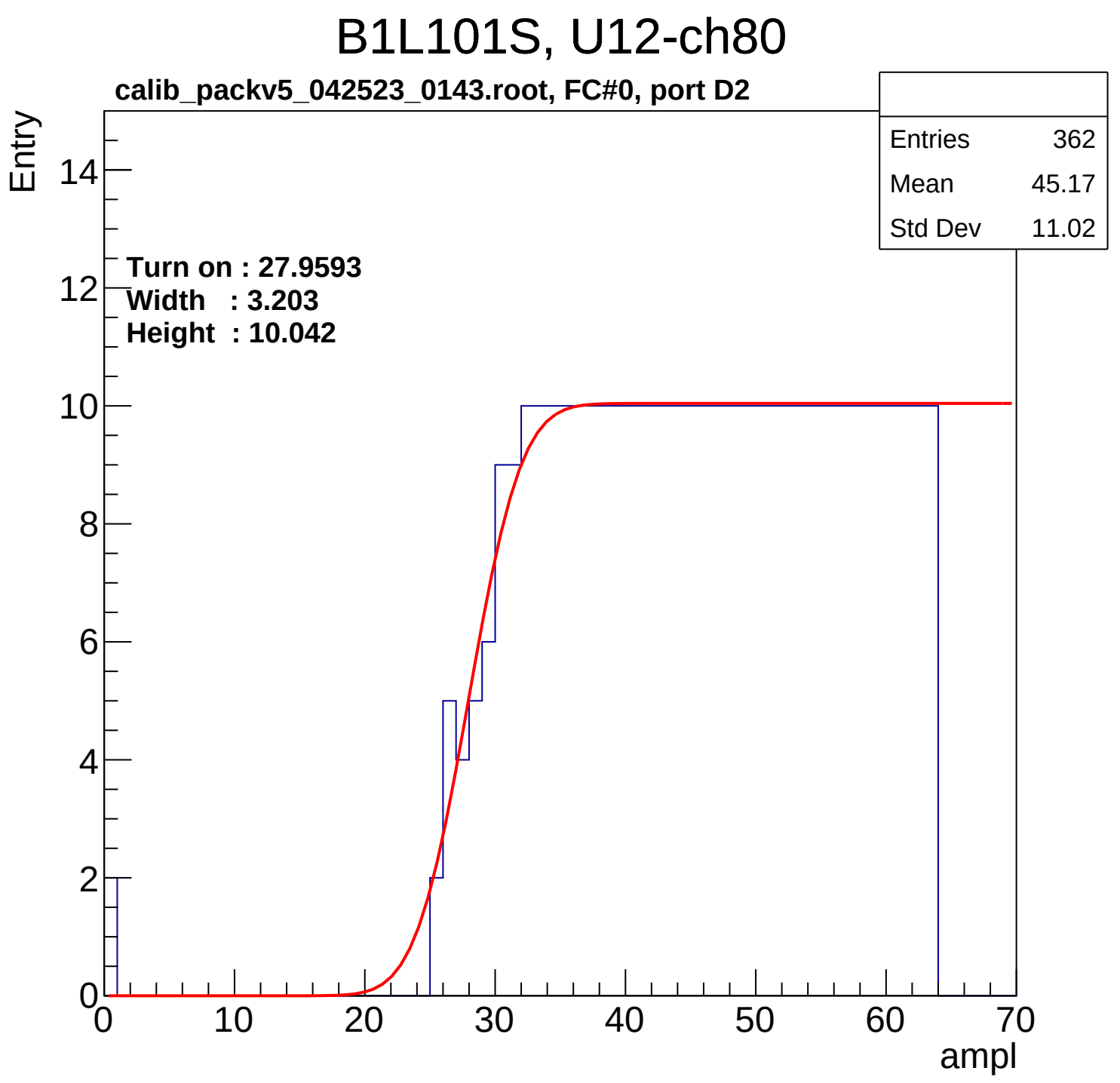

B1L101S, U12-ch75
calib_packv5_042523_0143.root, FC#0, port D2
Entries 349
Mean 45.72
Std Dev 10.84
Turn on : 29.7989
Width : 3.413
Height : 10.038
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

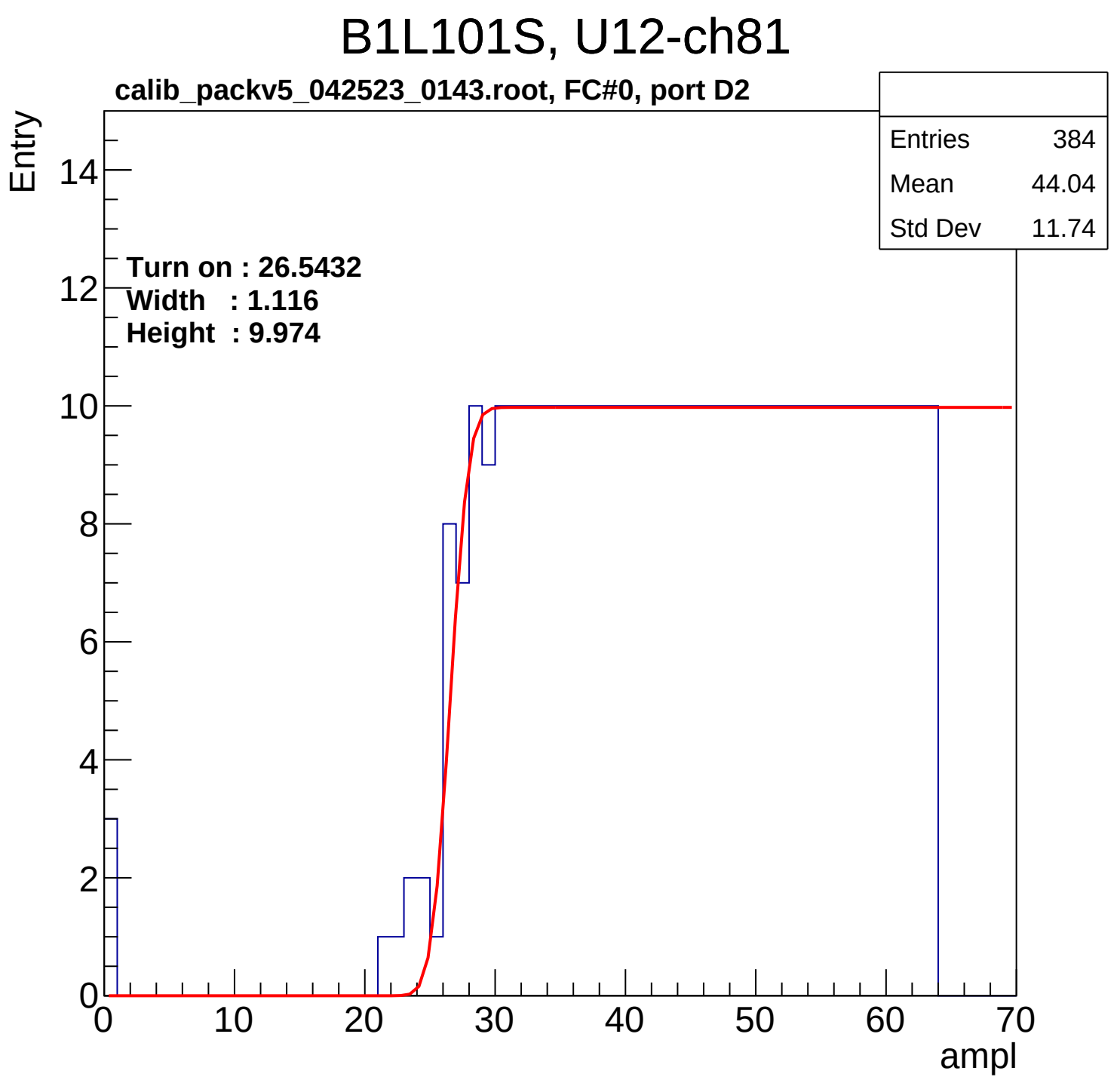

B1L101S, U12-ch76
calib_packv5_042523_0143.root, FC#0, port D2
Entries 392
Mean 43.59
Std Dev 12.08
Turn on : 25.0843
Width : 2.027
Height : 9.959
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

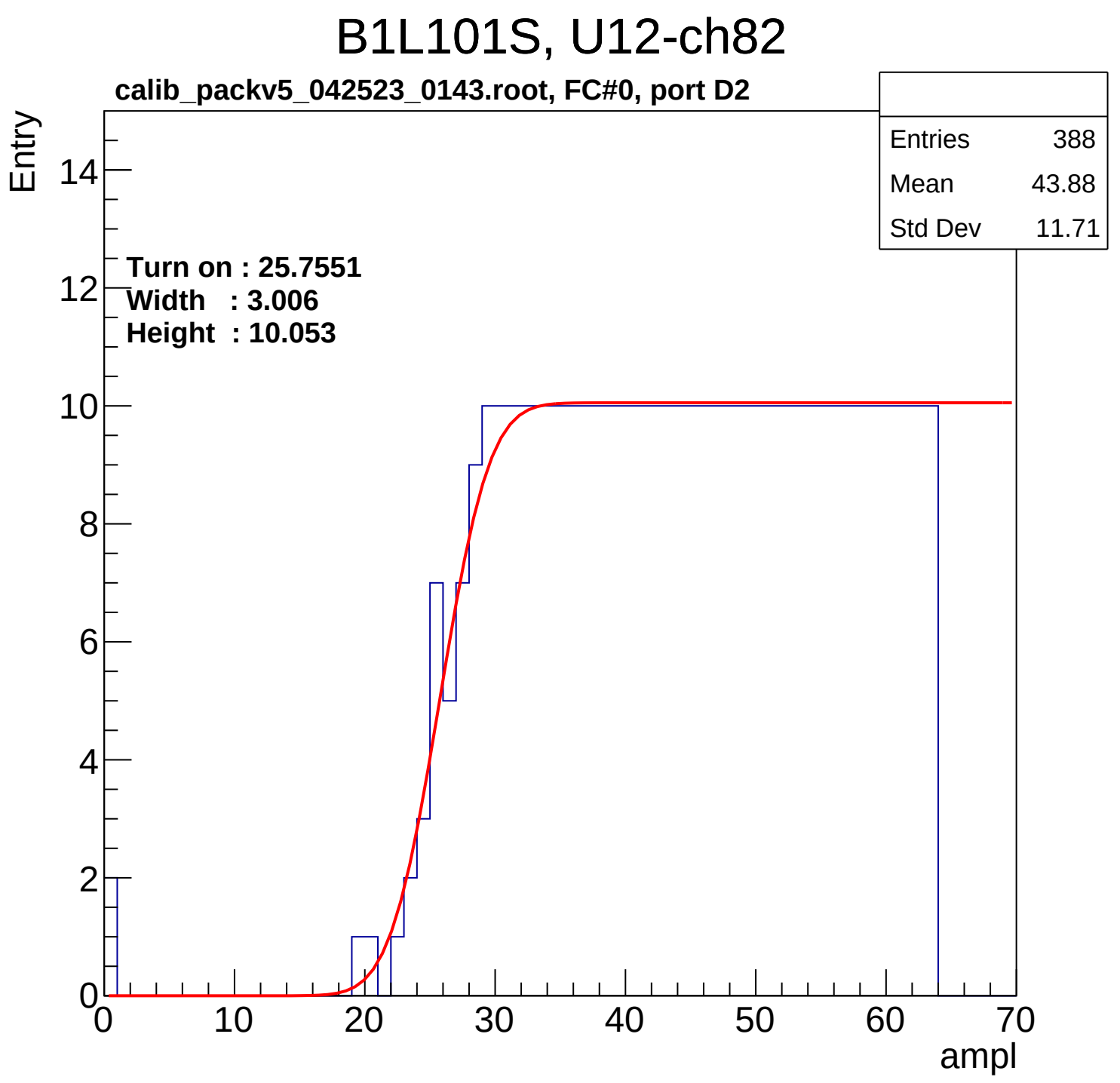

B1L101S, U12-ch77
calib_packv5_042523_0143.root, FC#0, port D2
Entries 384
Mean 43.86
Std Dev 12.14
Turn on : 26.1688
Width : 3.217
Height : 10.021
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

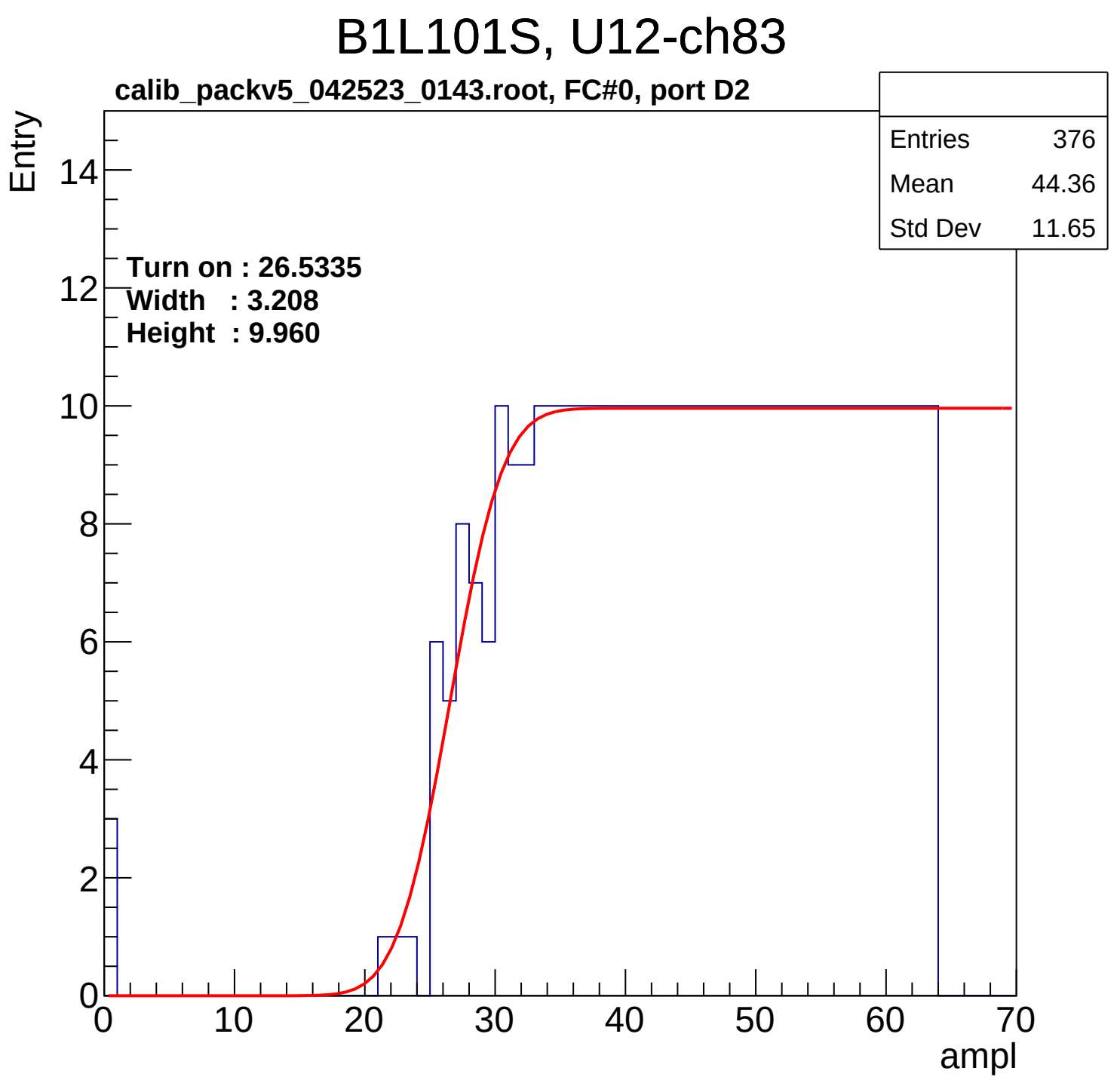

B1L101S, U12-ch78
calib_packv5_042523_0143.root, FC#0, port D2
Entries 367
Mean 44.9
Std Dev 11.18
Turn on : 27.1501
Width : 2.284
Height : 9.891
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

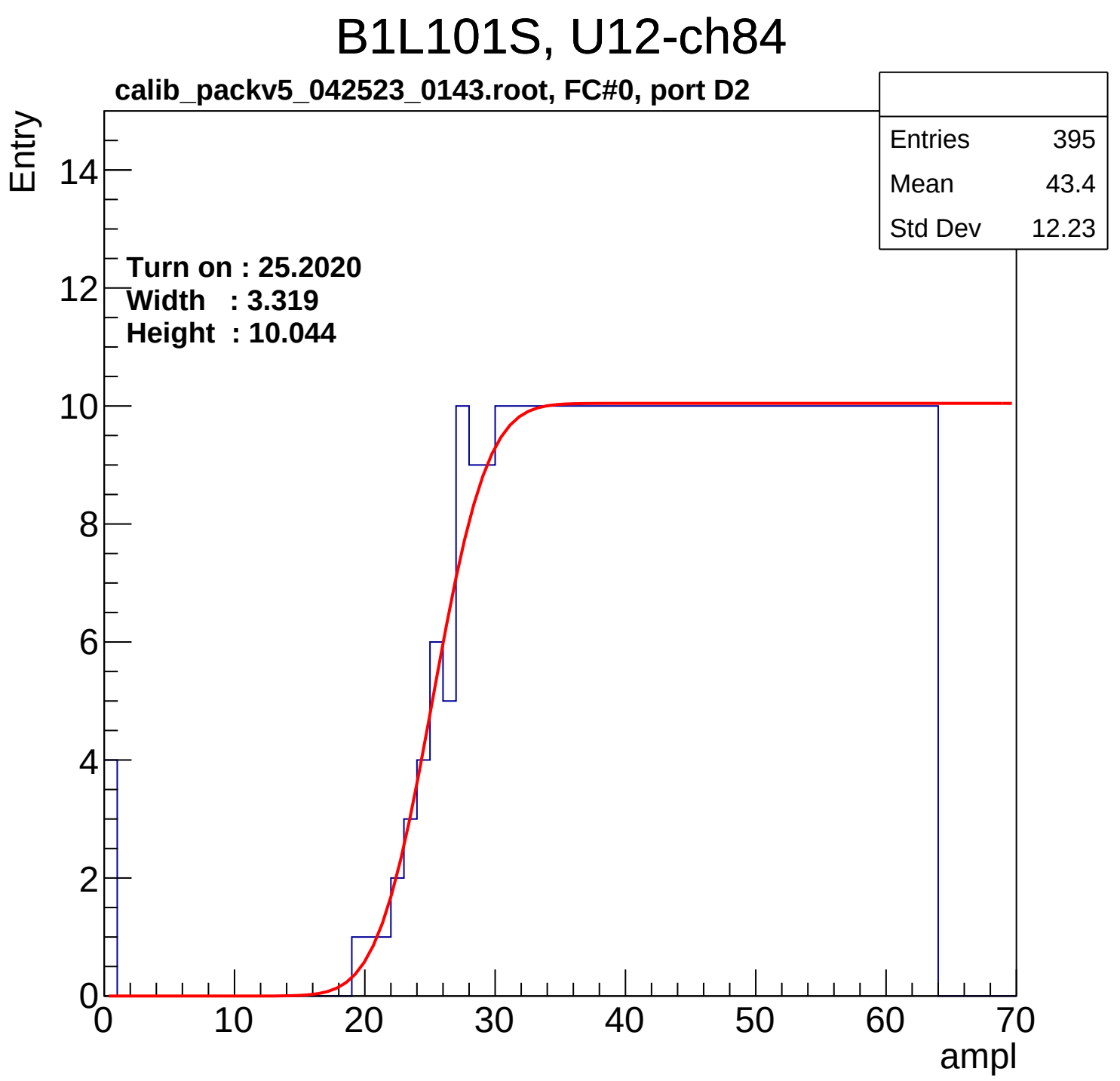

B1L101S, U12-ch79
calib_packv5_042523_0143.root, FC#0, port D2
Entries 380
Mean 44.14
Std Dev 11.78
Turn on : 27.4421
Width : 3.790
Height : 10.089
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

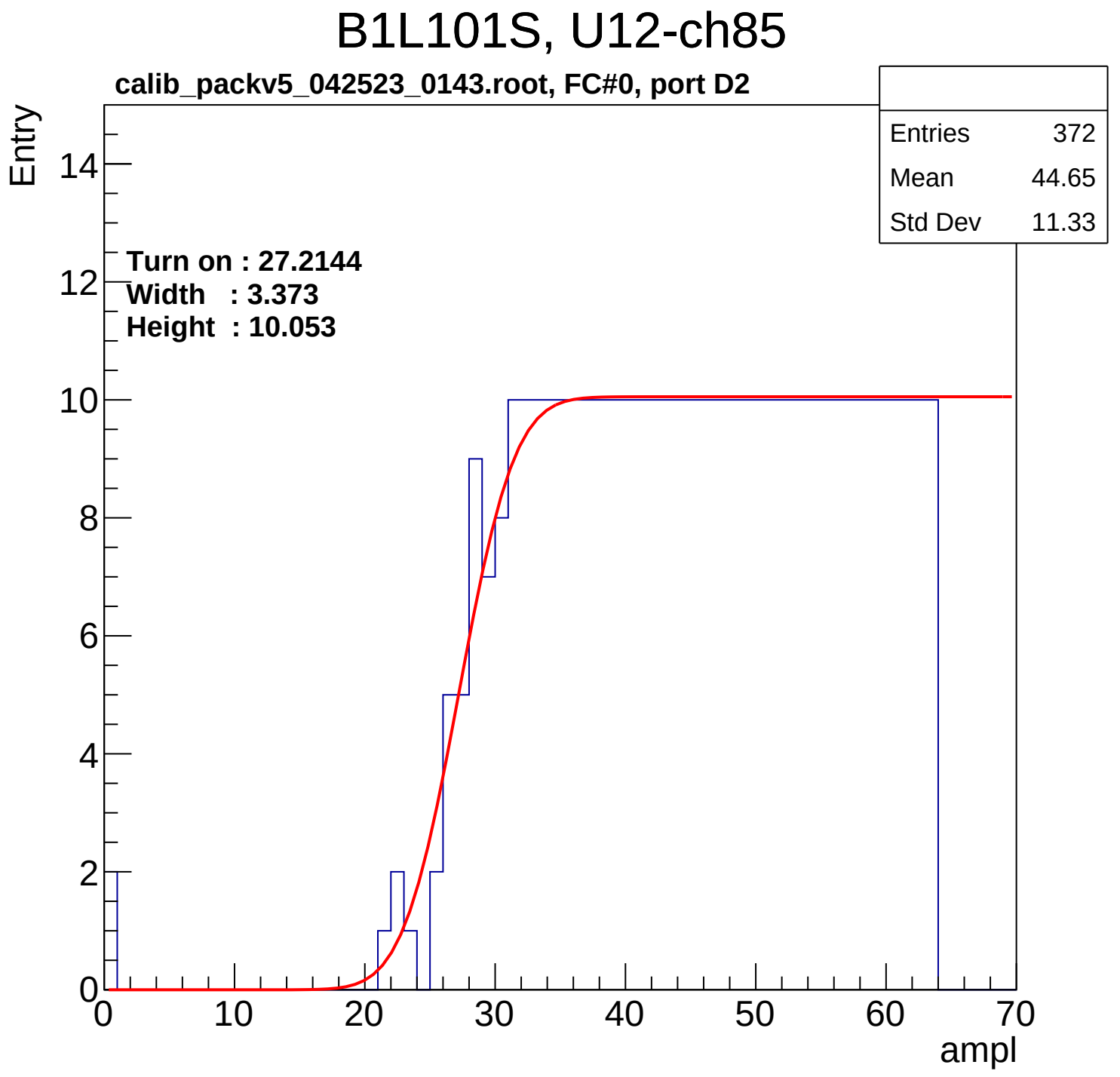

B1L101S, U12-ch80
calib_packv5_042523_0143.root, FC#0, port D2
Entries 362
Mean 45.17
Std Dev 11.02
Turn on : 27.9593
Width : 3.203
Height : 10.042
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

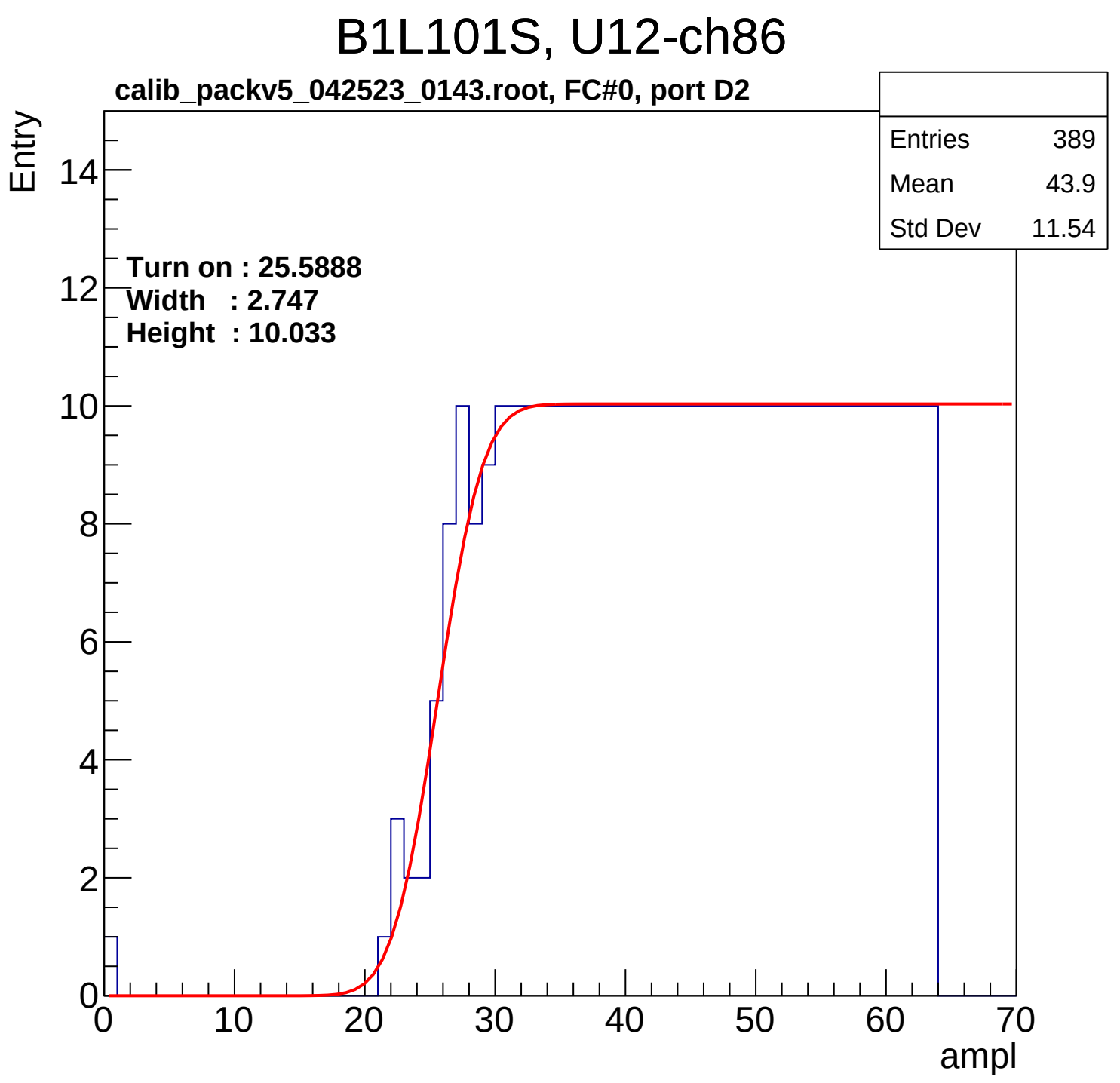

B1L101S, U12-ch81
calib_packv5_042523_0143.root, FC#0, port D2
Entries 384
Mean 44.04
Std Dev 11.74
Turn on : 26.5432
Width : 1.116
Height : 9.974
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

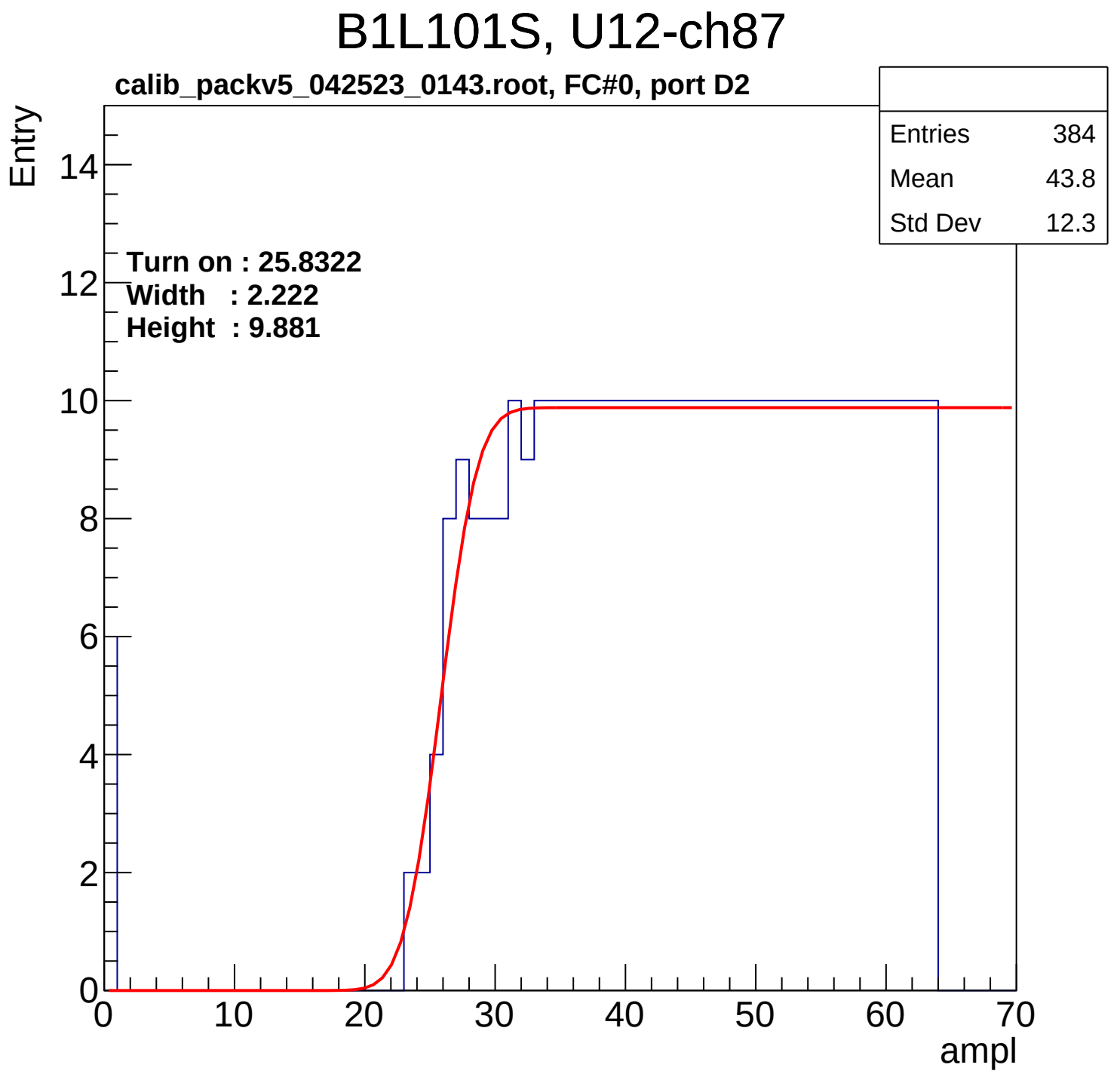

B1L101S, U12-ch82
calib_packv5_042523_0143.root, FC#0, port D2
Entries 388
Mean 43.88
Std Dev 11.71
Turn on : 25.7551
Width : 3.006
Height : 10.053
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

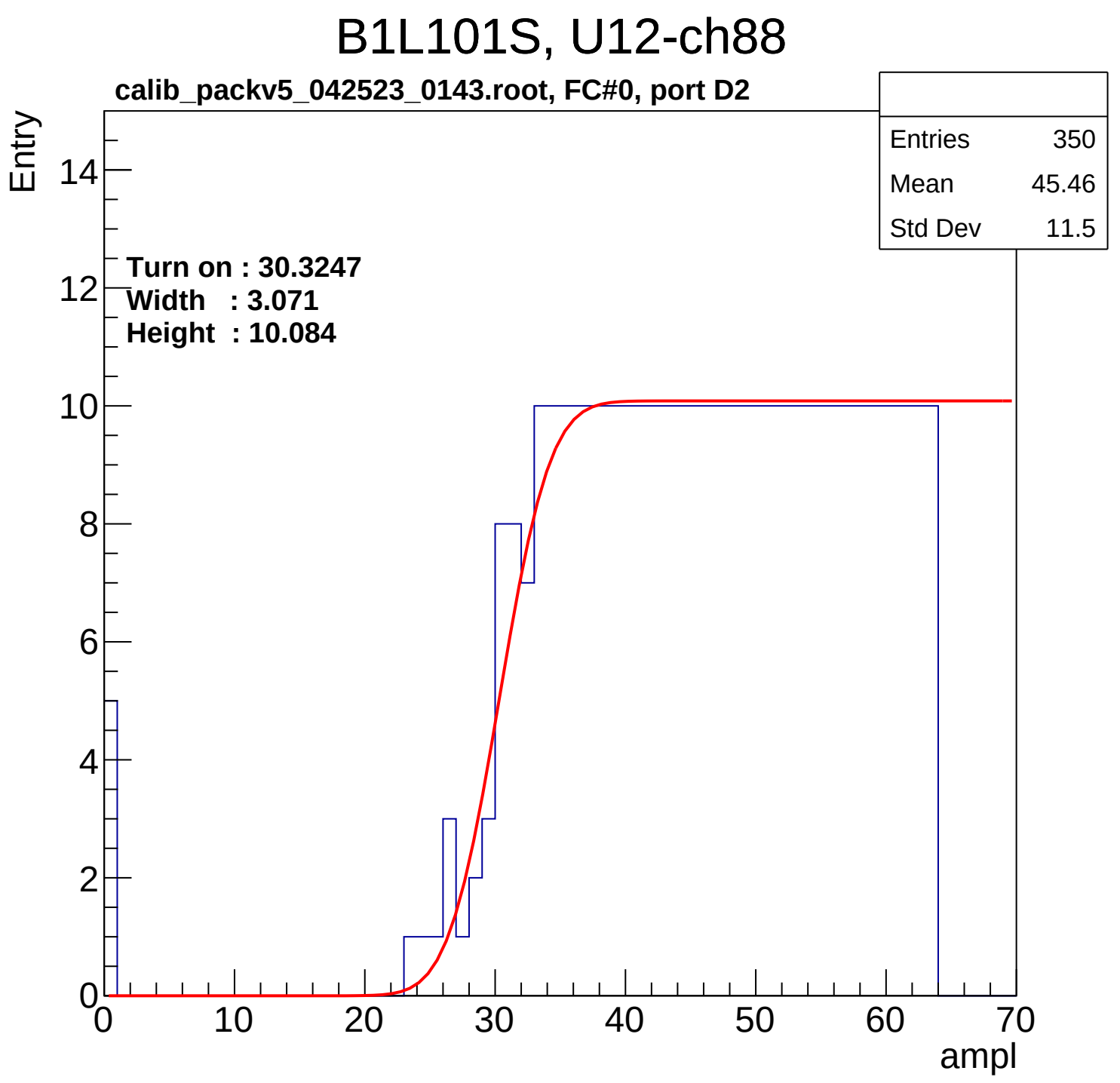

B1L101S, U12-ch83
calib_packv5_042523_0143.root, FC#0, port D2
Entries 376
Mean 44.36
Std Dev 11.65
Turn on : 26.5335
Width : 3.208
Height : 9.960
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

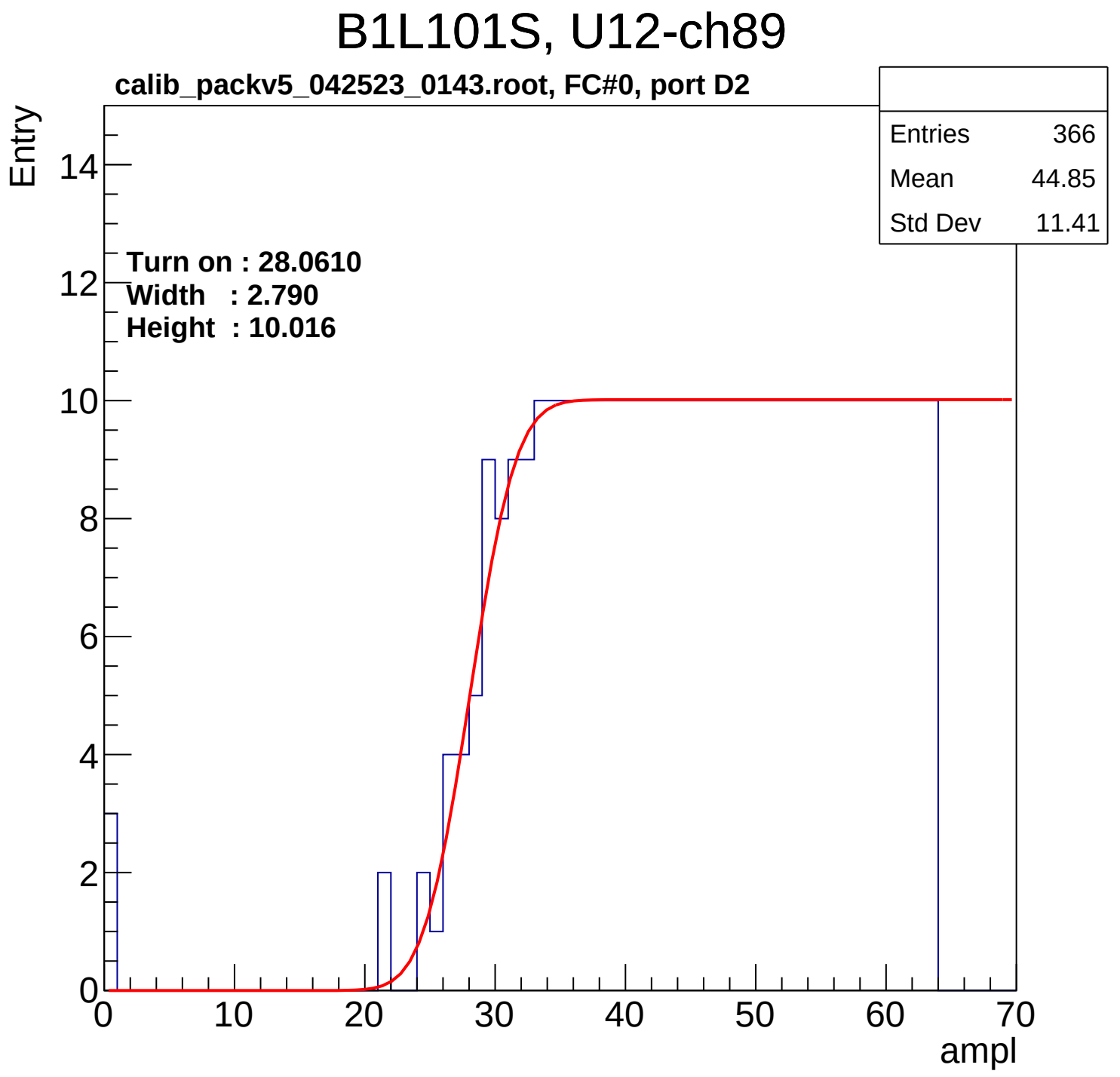

B1L101S, U12-ch84
calib_packv5_042523_0143.root, FC#0, port D2
Entries 395
Mean 43.4
Std Dev 12.23
Turn on : 25.2020
Width : 3.319
Height : 10.044
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

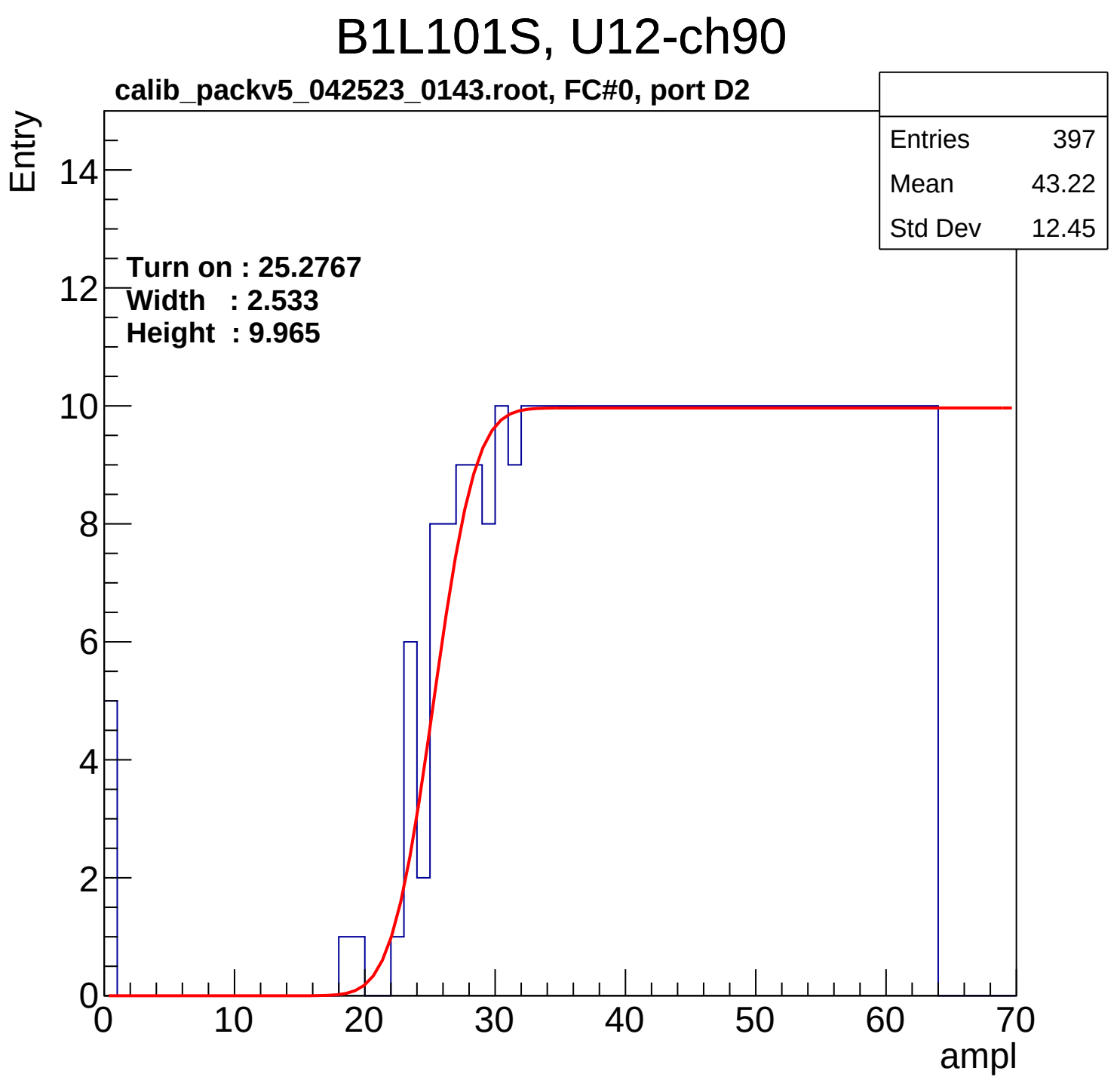

B1L101S, U12-ch85
calib_packv5_042523_0143.root, FC#0, port D2
Entries 372
Mean 44.65
Std Dev 11.33
Turn on : 27.2144
Width : 3.373
Height : 10.053
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

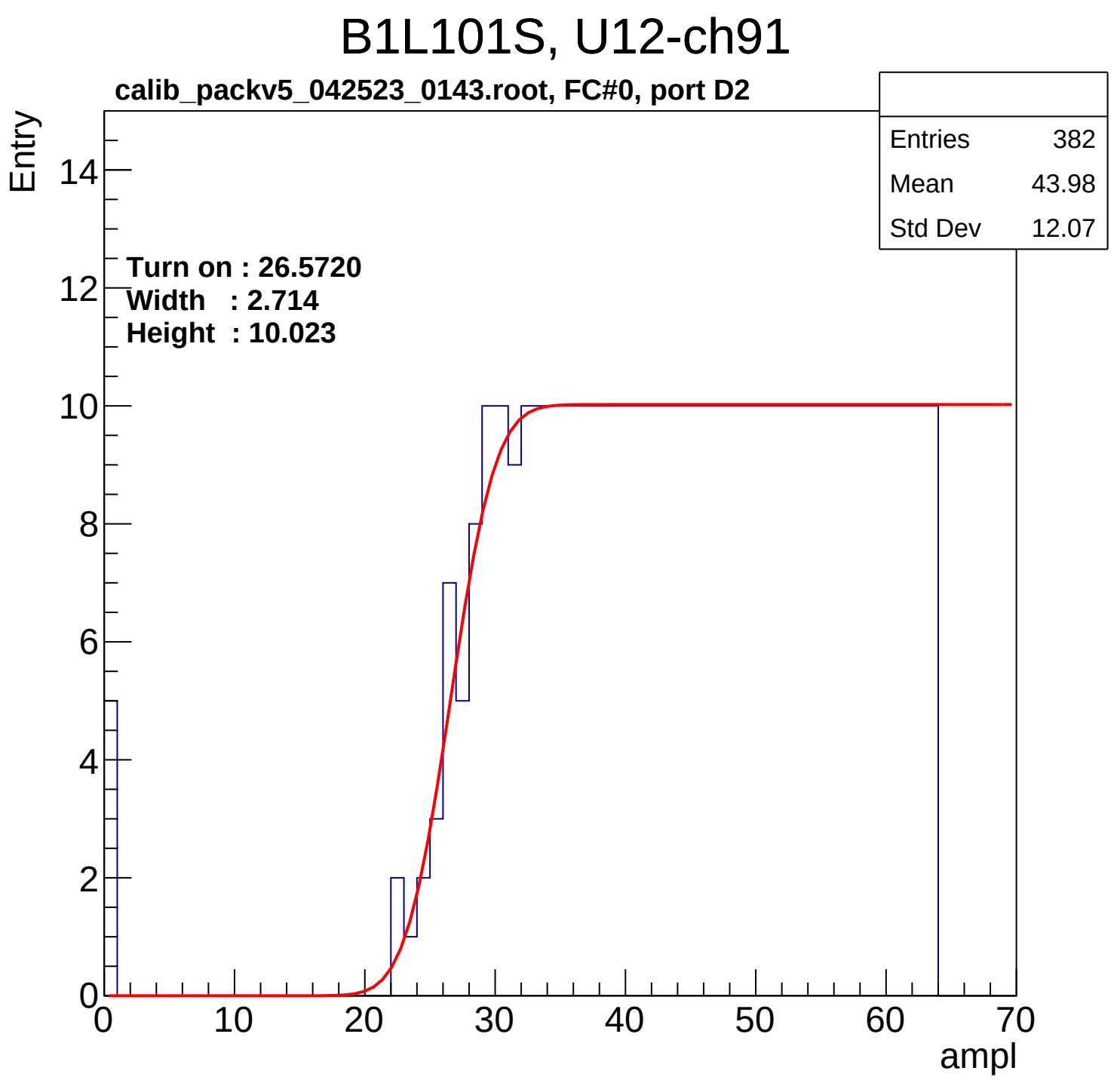

B1L101S, U12-ch86
calib_packv5_042523_0143.root, FC#0, port D2
Entries 389
Mean 43.9
Std Dev 11.54
Turn on : 25.5888
Width : 2.747
Height : 10.033
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

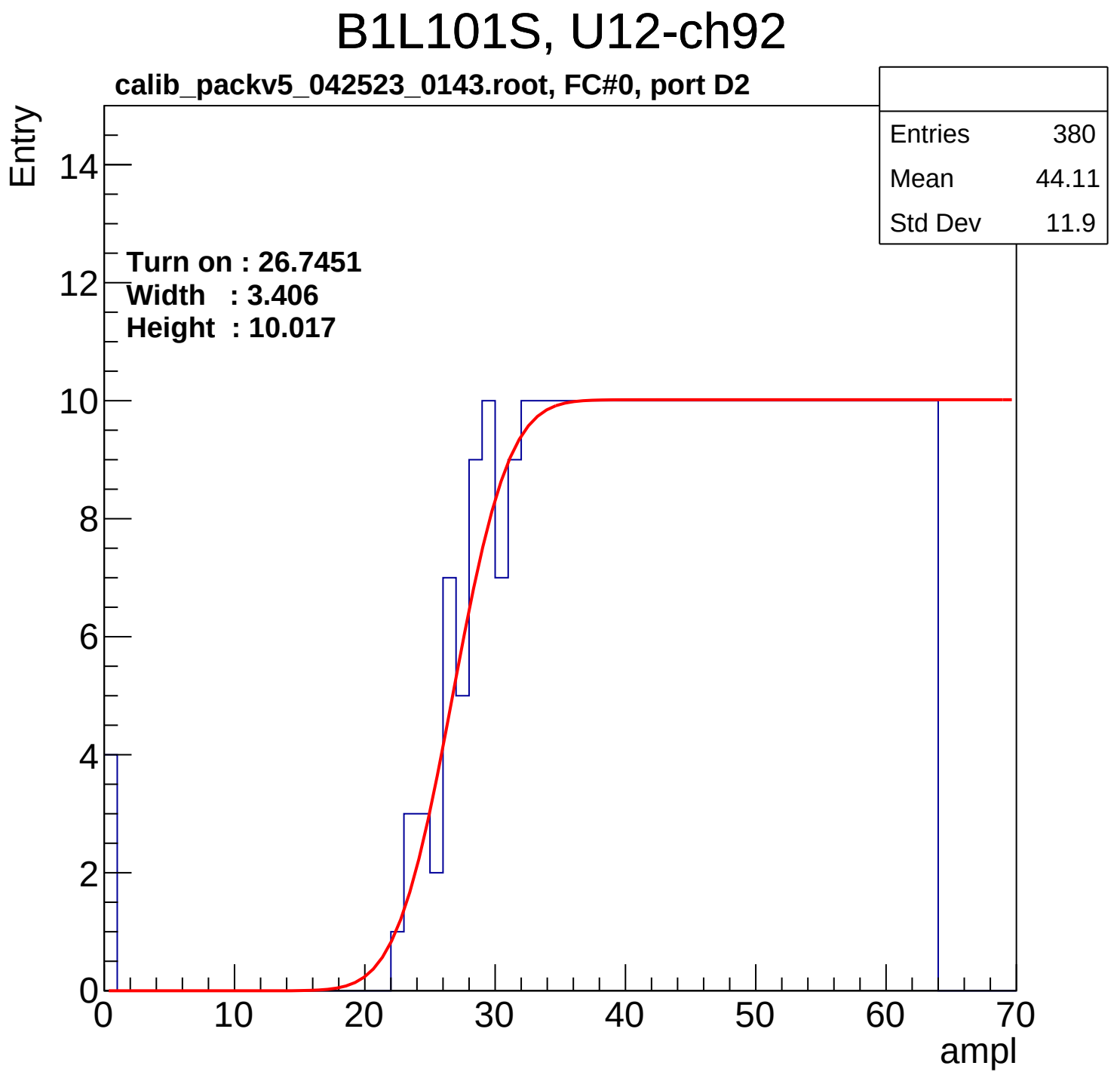

B1L101S, U12-ch87
calib_packv5_042523_0143.root, FC#0, port D2
Entries 384
Mean 43.8
Std Dev 12.3
Turn on : 25.8322
Width : 2.222
Height : 9.881
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

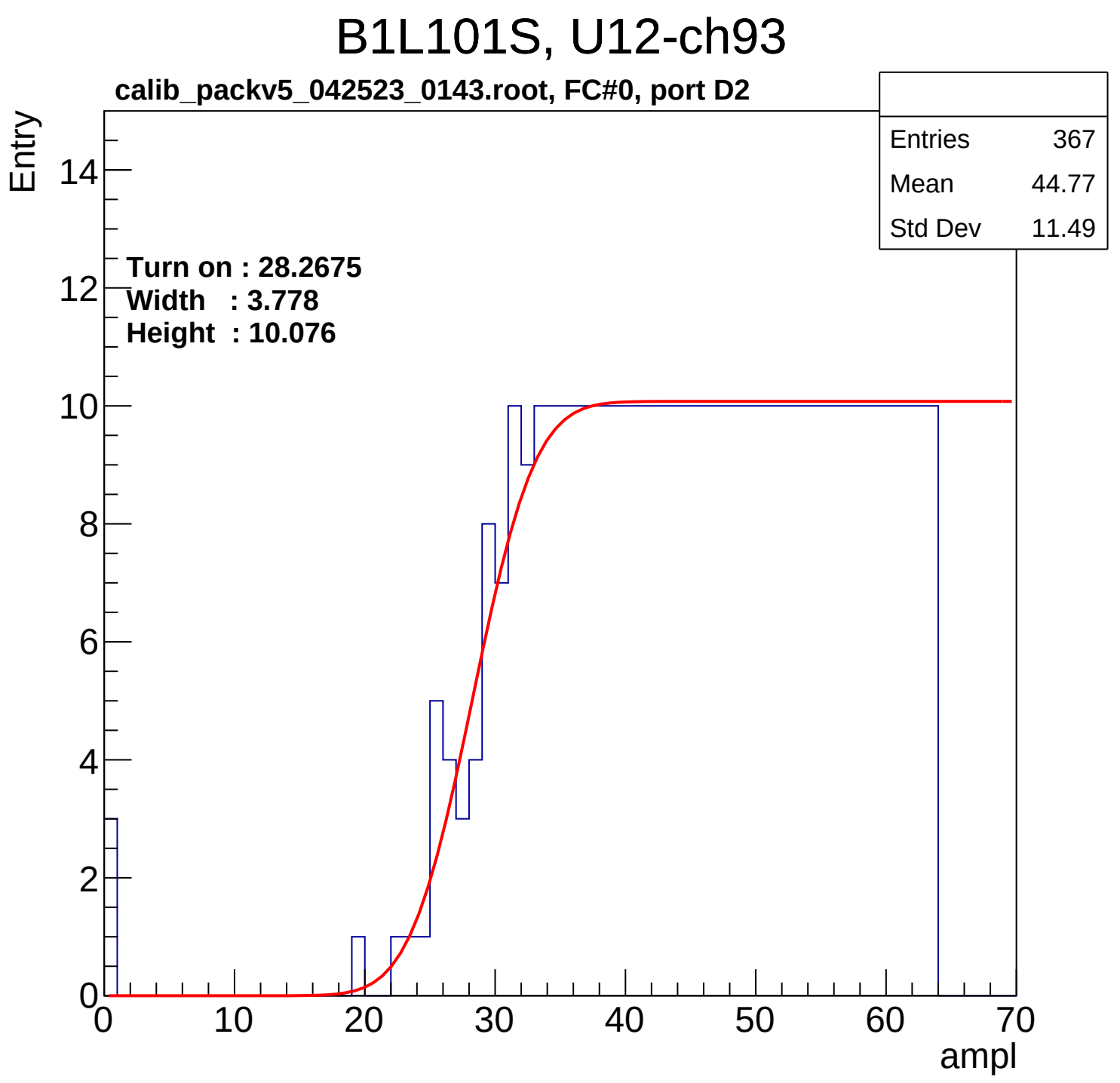

B1L101S, U12-ch88
calib_packv5_042523_0143.root, FC#0, port D2
Entries 350
Mean 45.46
Std Dev 11.5
Turn on : 30.3247
Width : 3.071
Height : 10.084
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

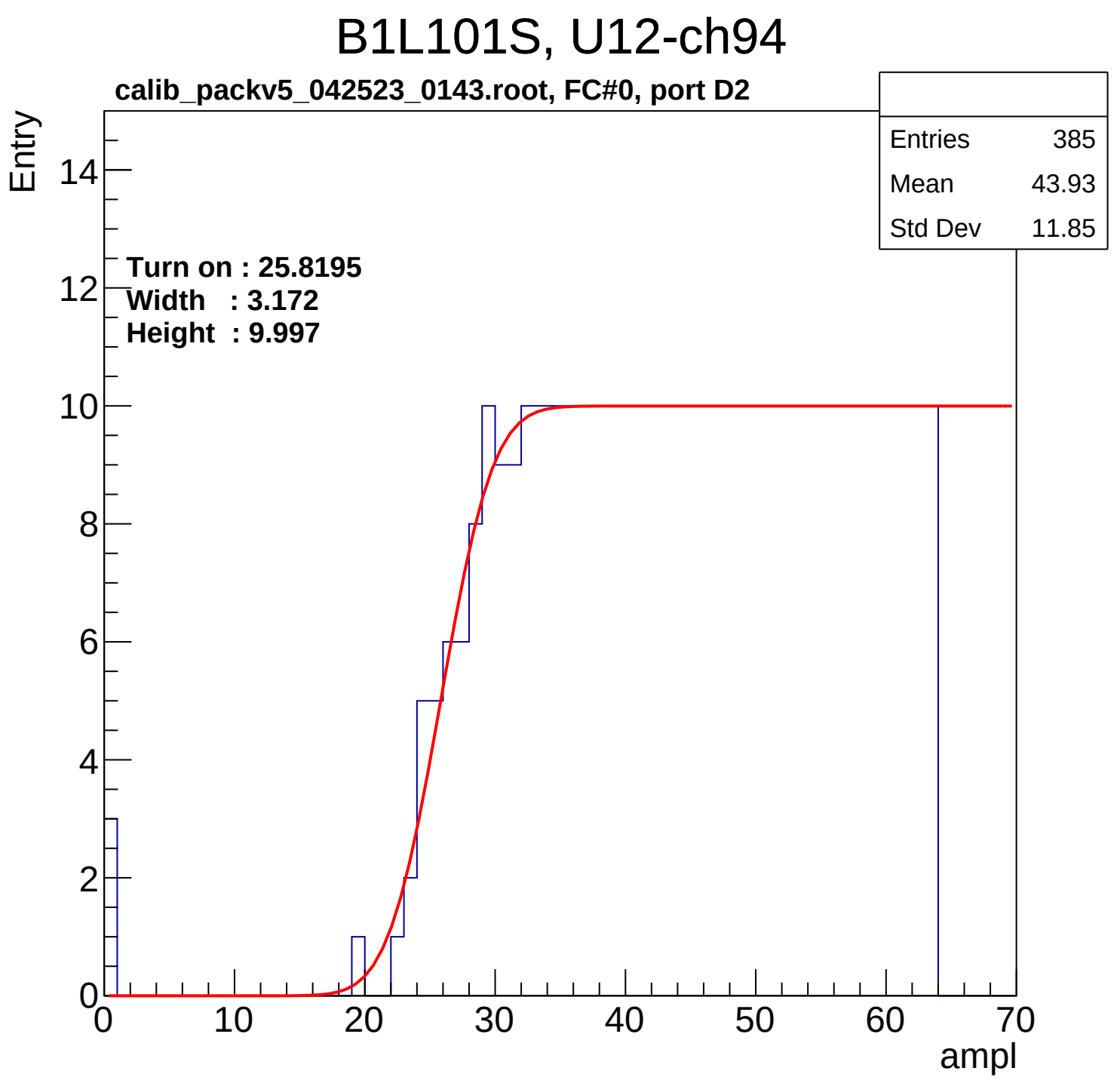

B1L101S, U12-ch89
calib_packv5_042523_0143.root, FC#0, port D2
Entries 366
Mean 44.85
Std Dev 11.41
Turn on : 28.0610
Width : 2.790
Height : 10.016
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

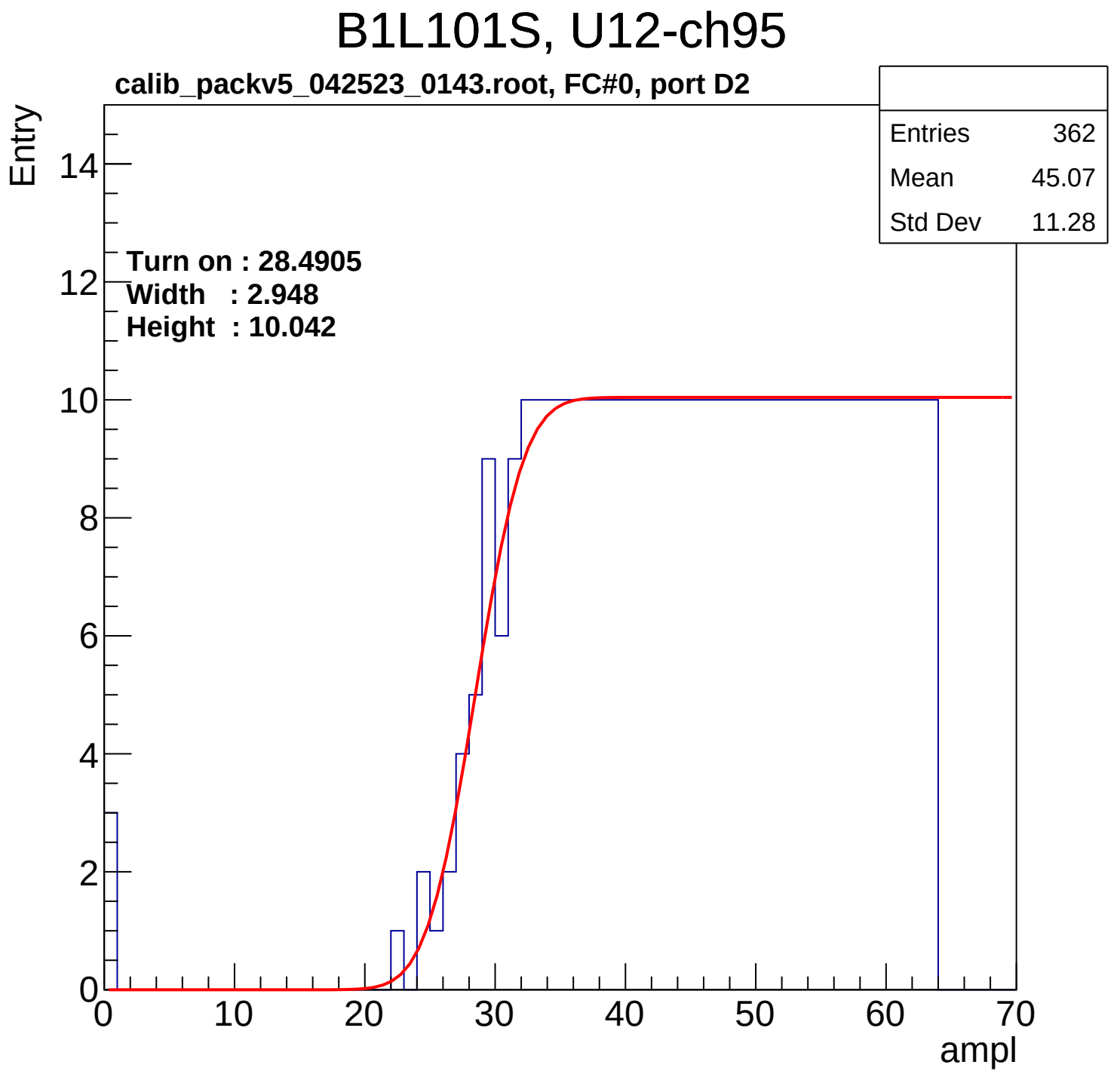

B1L101S, U12-ch90
calib_packv5_042523_0143.root, FC#0, port D2
Entries 397
Mean 43.22
Std Dev 12.45
Turn on : 25.2767
Width : 2.533
Height : 9.965
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

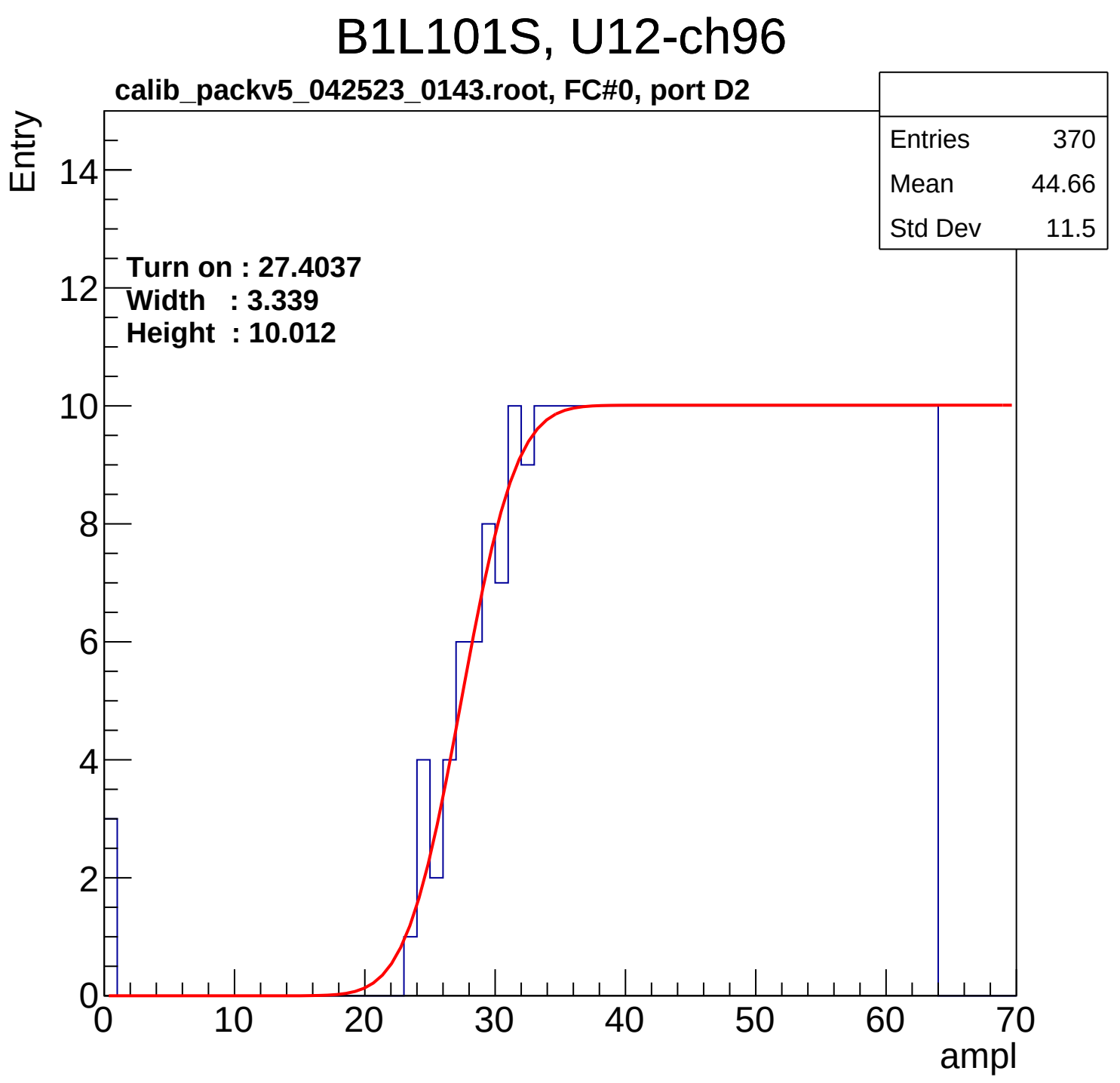

B1L101S, U12-ch91
calib_packv5_042523_0143.root, FC#0, port D2
Entries 382
Mean 43.98
Std Dev 12.07
Turn on : 26.5720
Width : 2.714
Height : 10.023
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

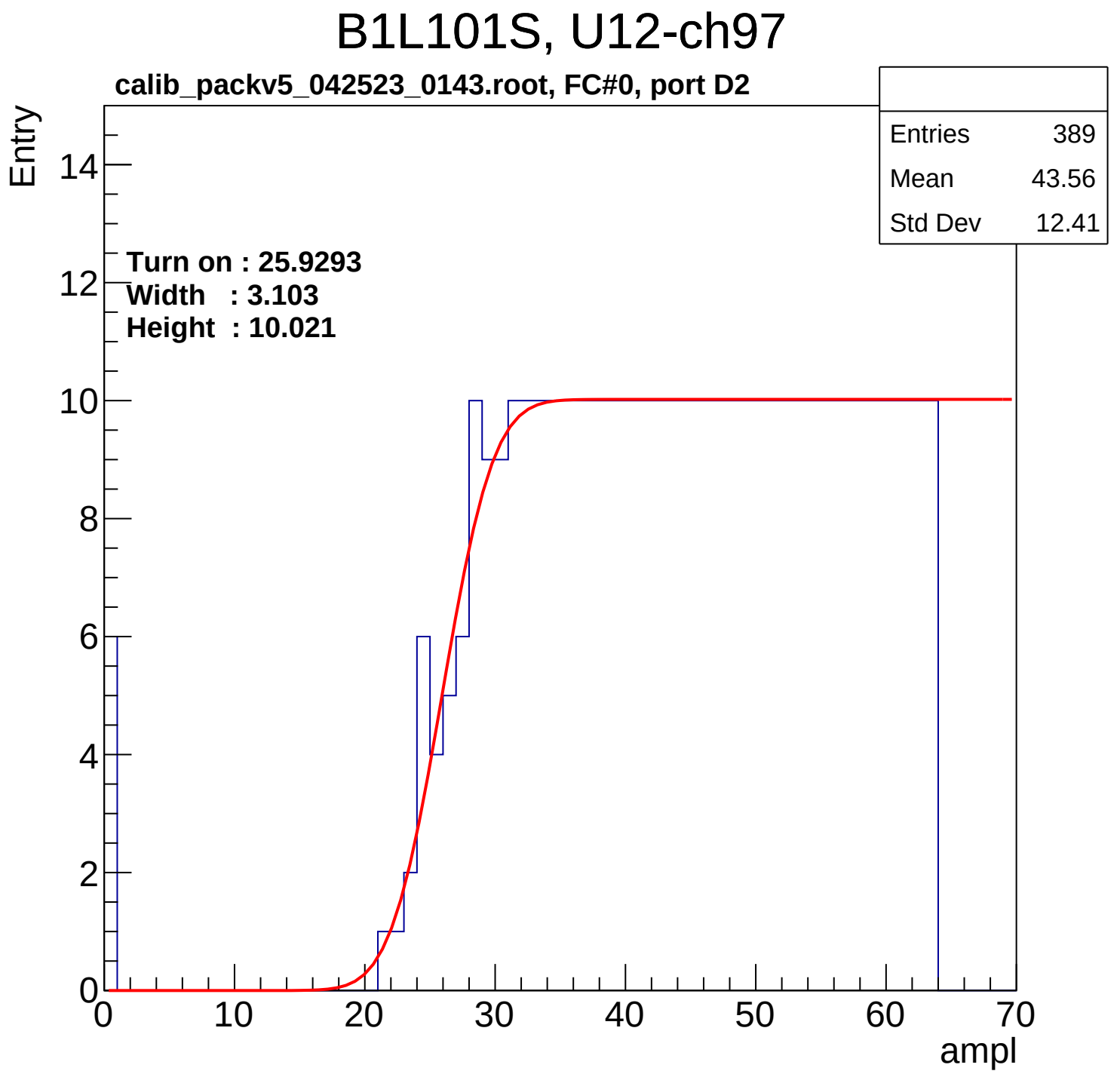

B1L101S, U12-ch92
calib_packv5_042523_0143.root, FC#0, port D2
Entries 380
Mean 44.11
Std Dev 11.9
Turn on : 26.7451
Width : 3.406
Height : 10.017
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

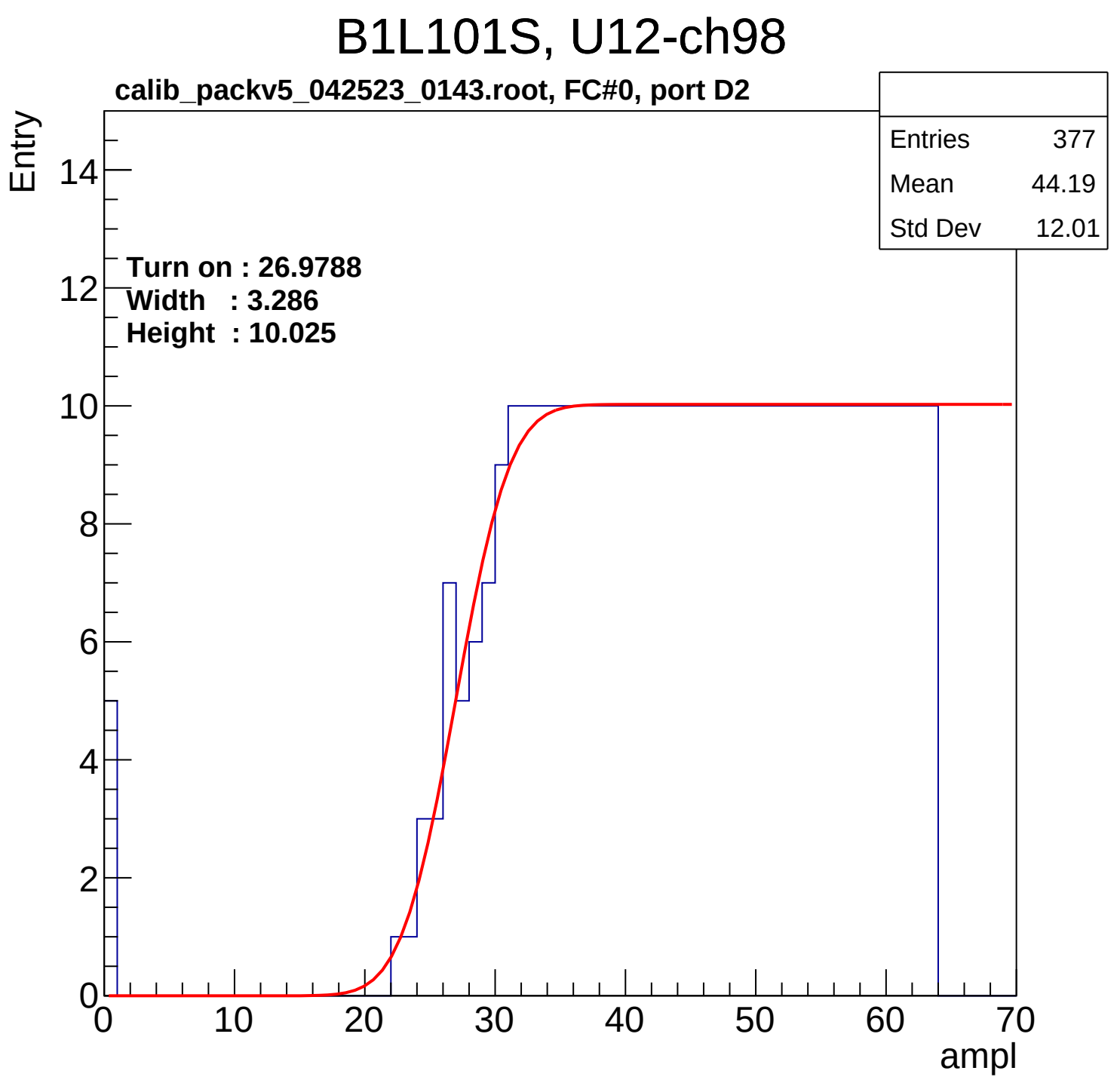

B1L101S, U12-ch93
calib_packv5_042523_0143.root, FC#0, port D2
Entries 367
Mean 44.77
Std Dev 11.49
Turn on : 28.2675
Width : 3.778
Height : 10.076
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

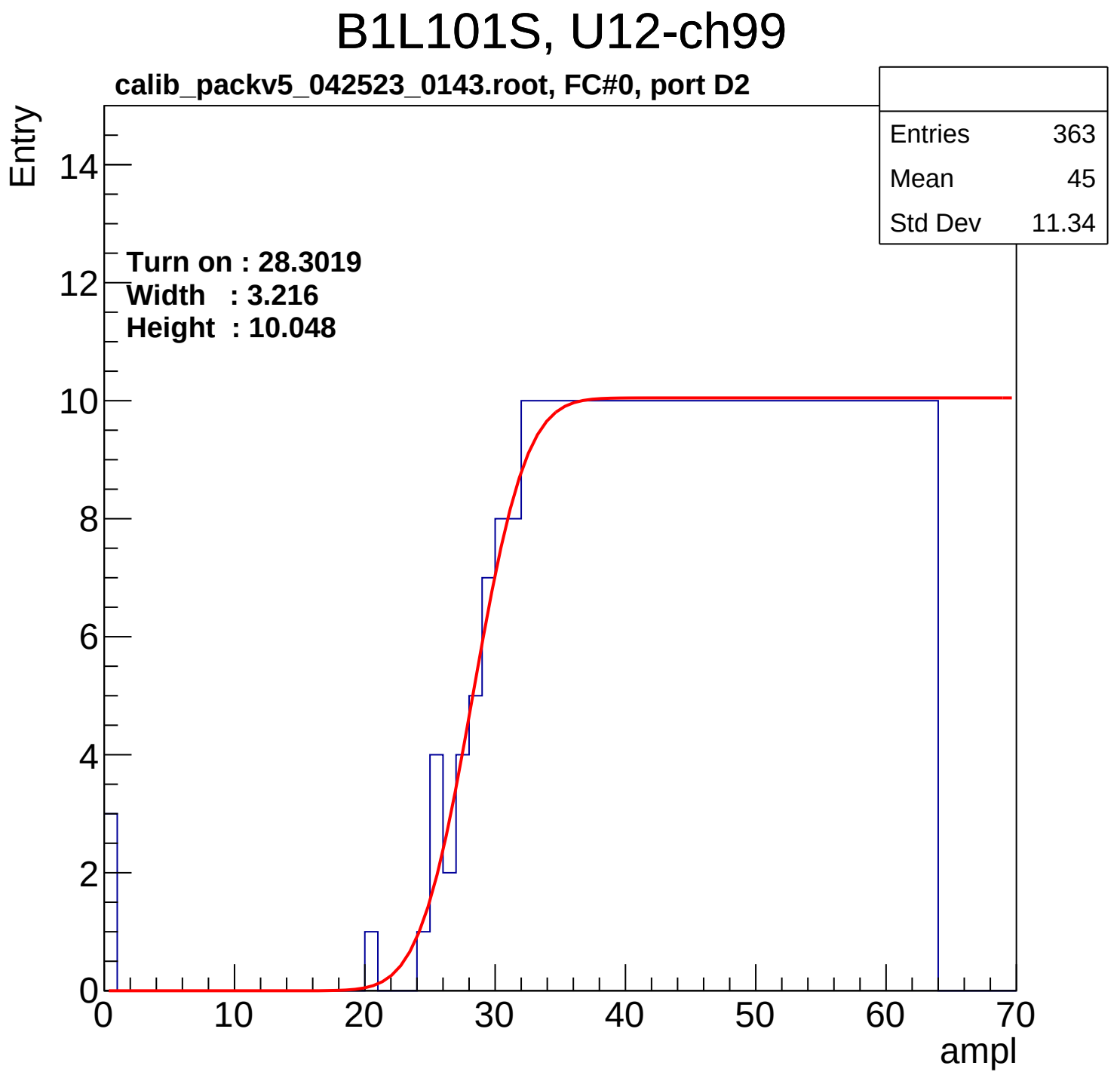

B1L101S, U12-ch94
calib_packv5_042523_0143.root, FC#0, port D2
Entries 385
Mean 43.93
Std Dev 11.85
Turn on : 25.8195
Width : 3.172
Height : 9.997
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

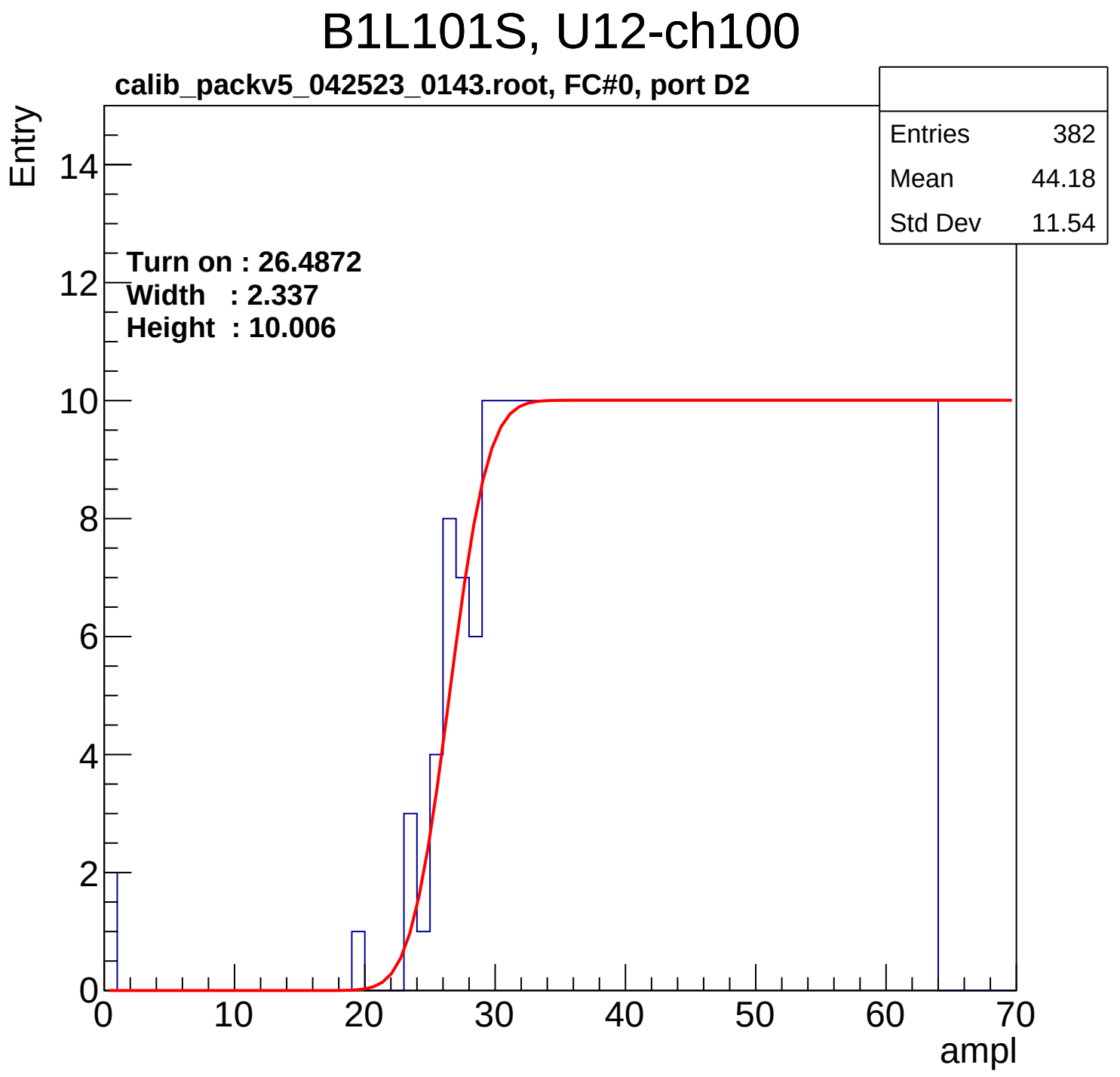

B1L101S, U12-ch95
calib_packv5_042523_0143.root, FC#0, port D2
Entries 362
Mean 45.07
Std Dev 11.28
Turn on : 28.4905
Width : 2.948
Height : 10.042
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

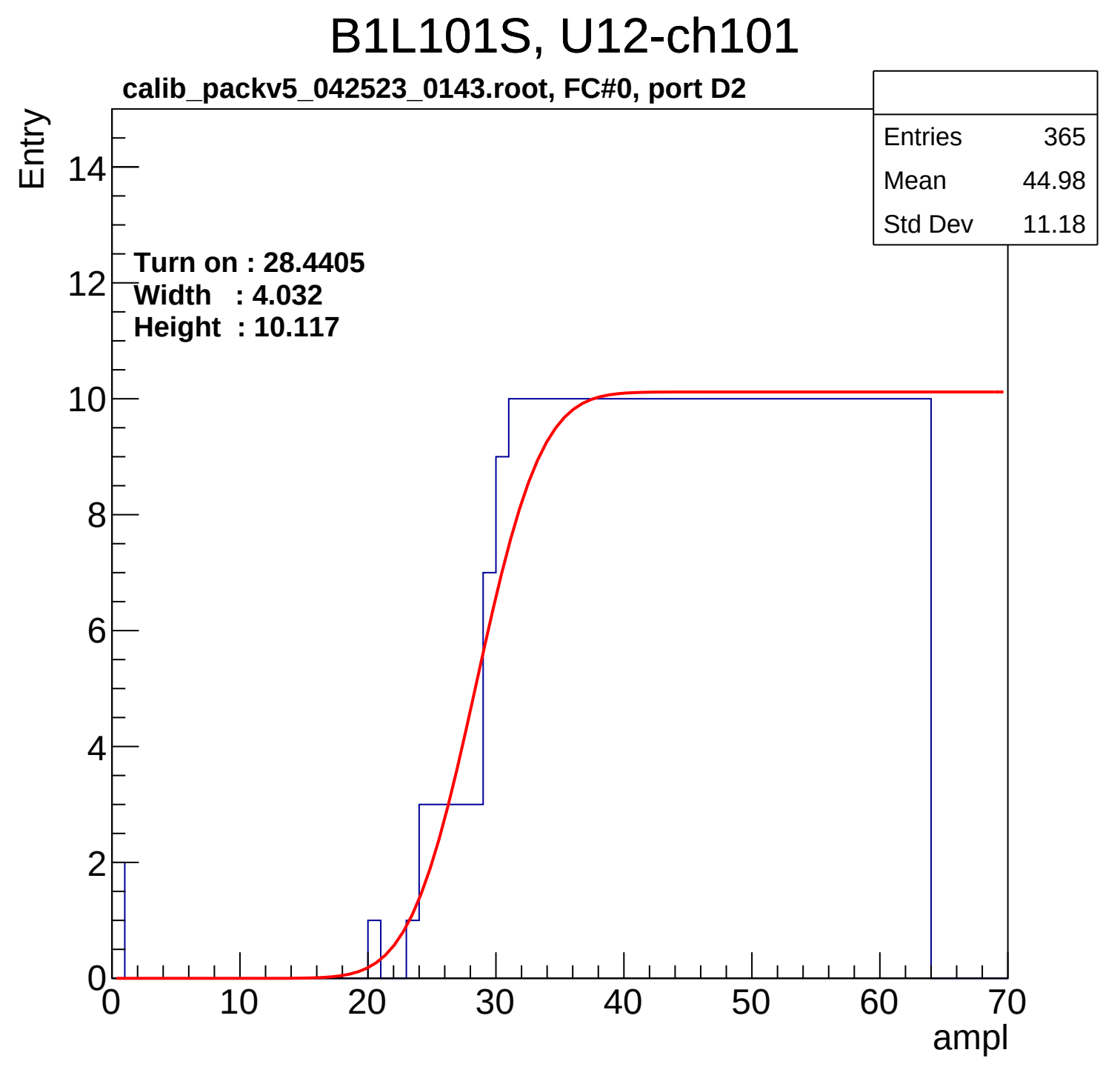

B1L101S, U12-ch96
calib_packv5_042523_0143.root, FC#0, port D2
Entries 370
Mean 44.66
Std Dev 11.5
Turn on : 27.4037
Width : 3.339
Height : 10.012
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

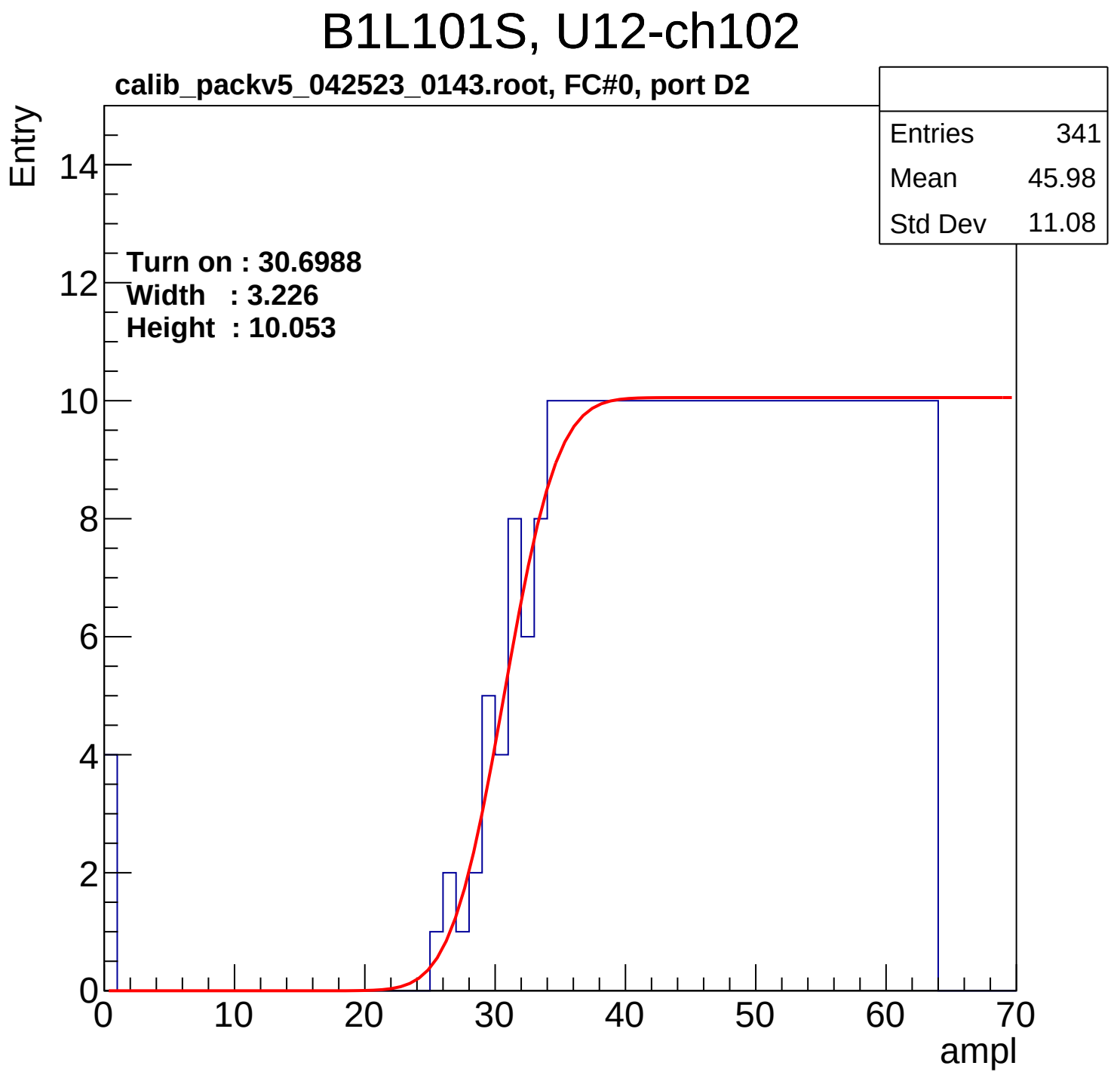

B1L101S, U12-ch97
calib_packv5_042523_0143.root, FC#0, port D2
Entries 389
Mean 43.56
Std Dev 12.41
Turn on : 25.9293
Width : 3.103
Height : 10.021
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

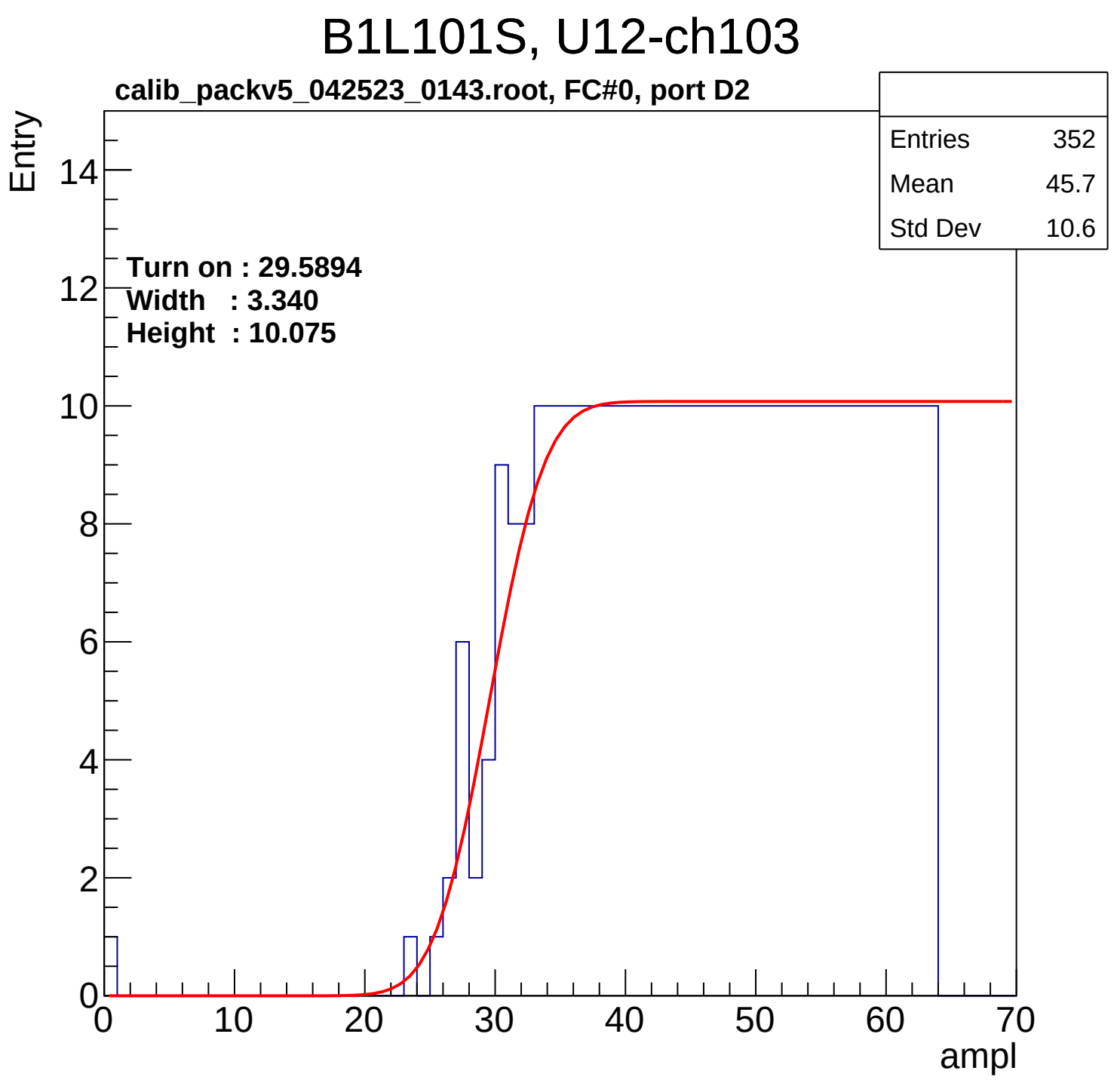

B1L101S, U12-ch98
calib_packv5_042523_0143.root, FC#0, port D2
Entries 377
Mean 44.19
Std Dev 12.01
Turn on : 26.9788
Width : 3.286
Height : 10.025
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

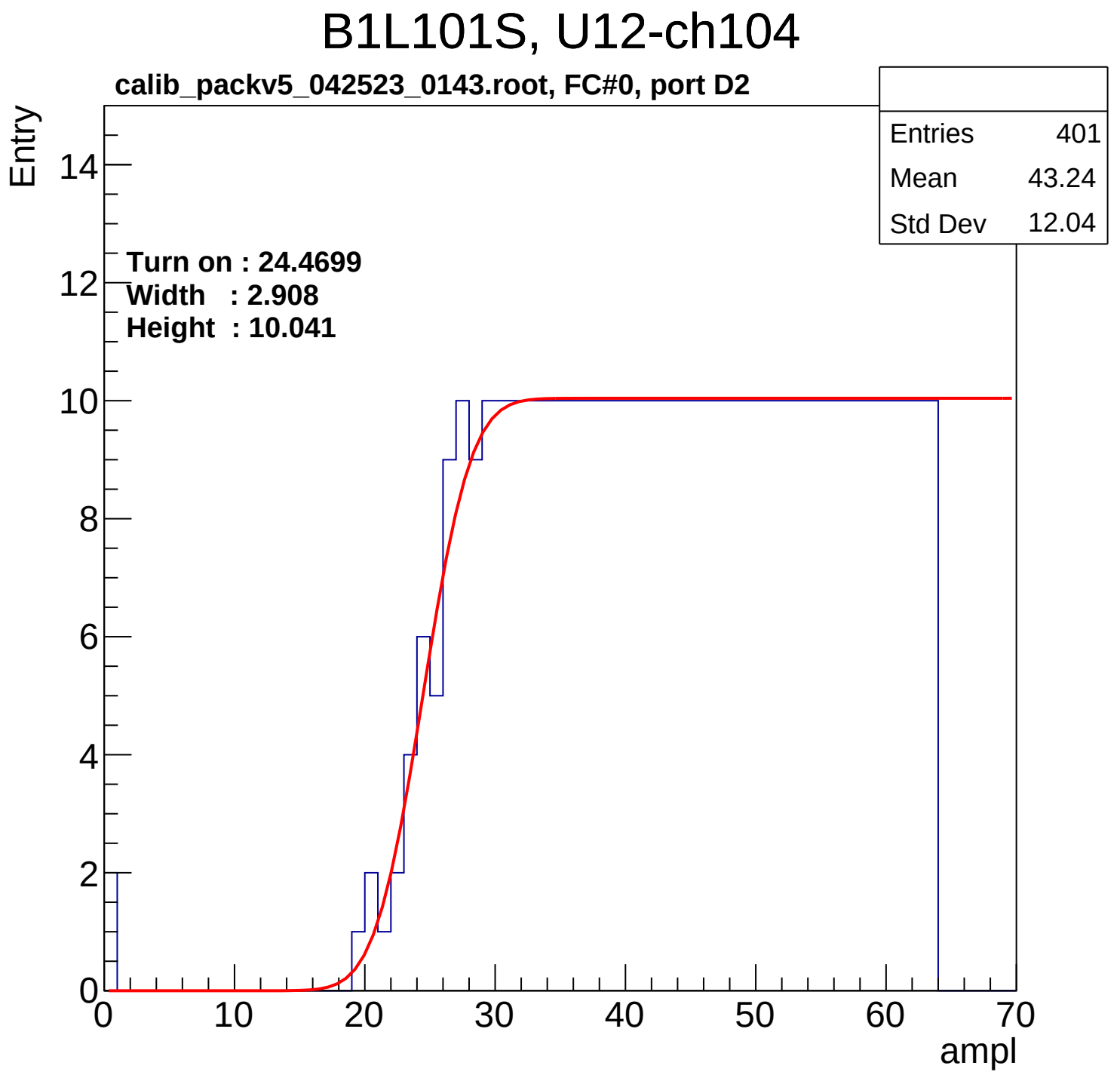

B1L101S, U12-ch99
calib_packv5_042523_0143.root, FC#0, port D2
Entries 363
Mean 45
Std Dev 11.34
Turn on : 28.3019
Width : 3.216
Height : 10.048
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

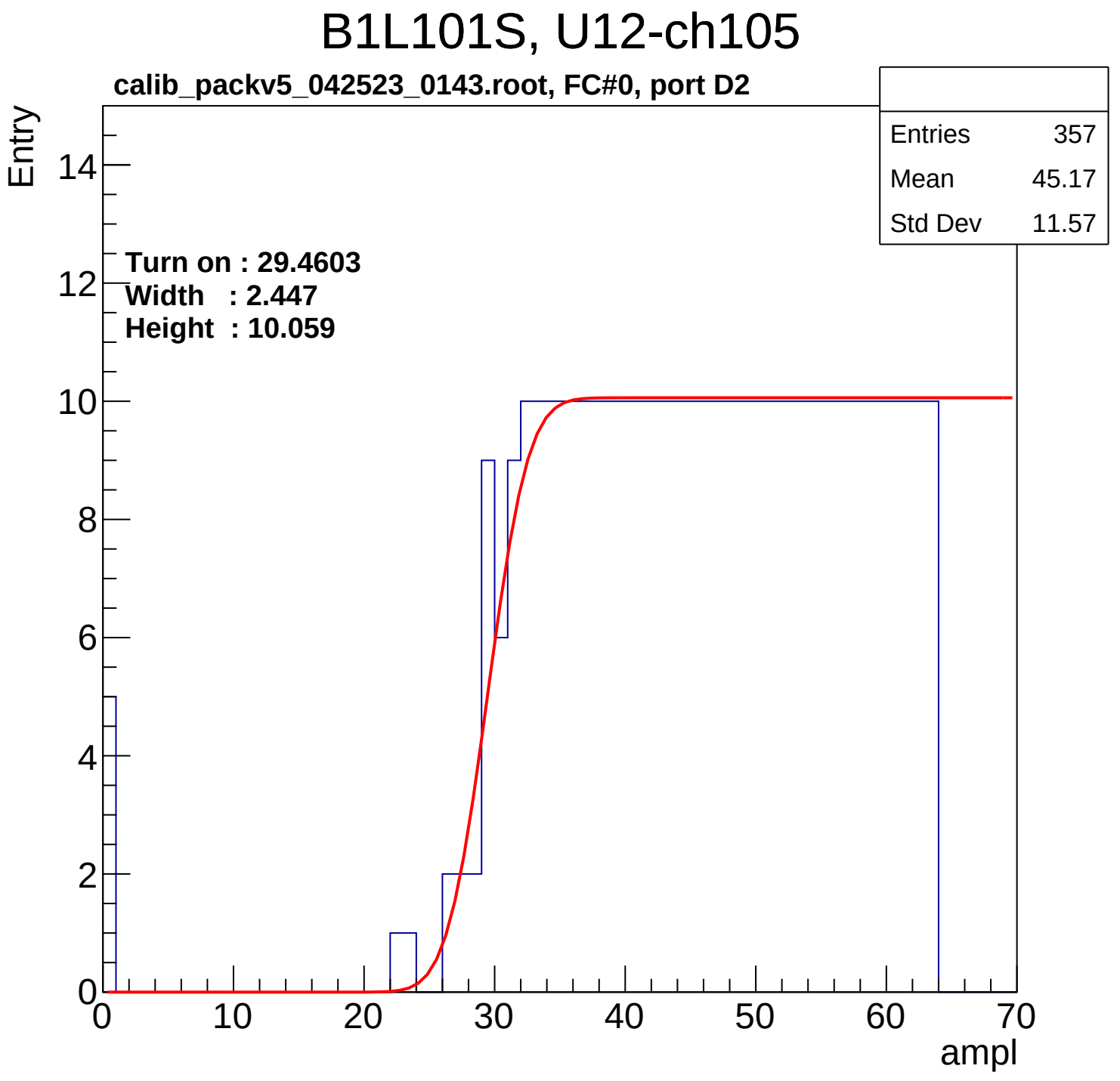

B1L101S, U12-ch100
calib_packv5_042523_0143.root, FC#0, port D2
Entries 382
Mean 44.18
Std Dev 11.54
Turn on : 26.4872
Width : 2.337
Height : 10.006
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

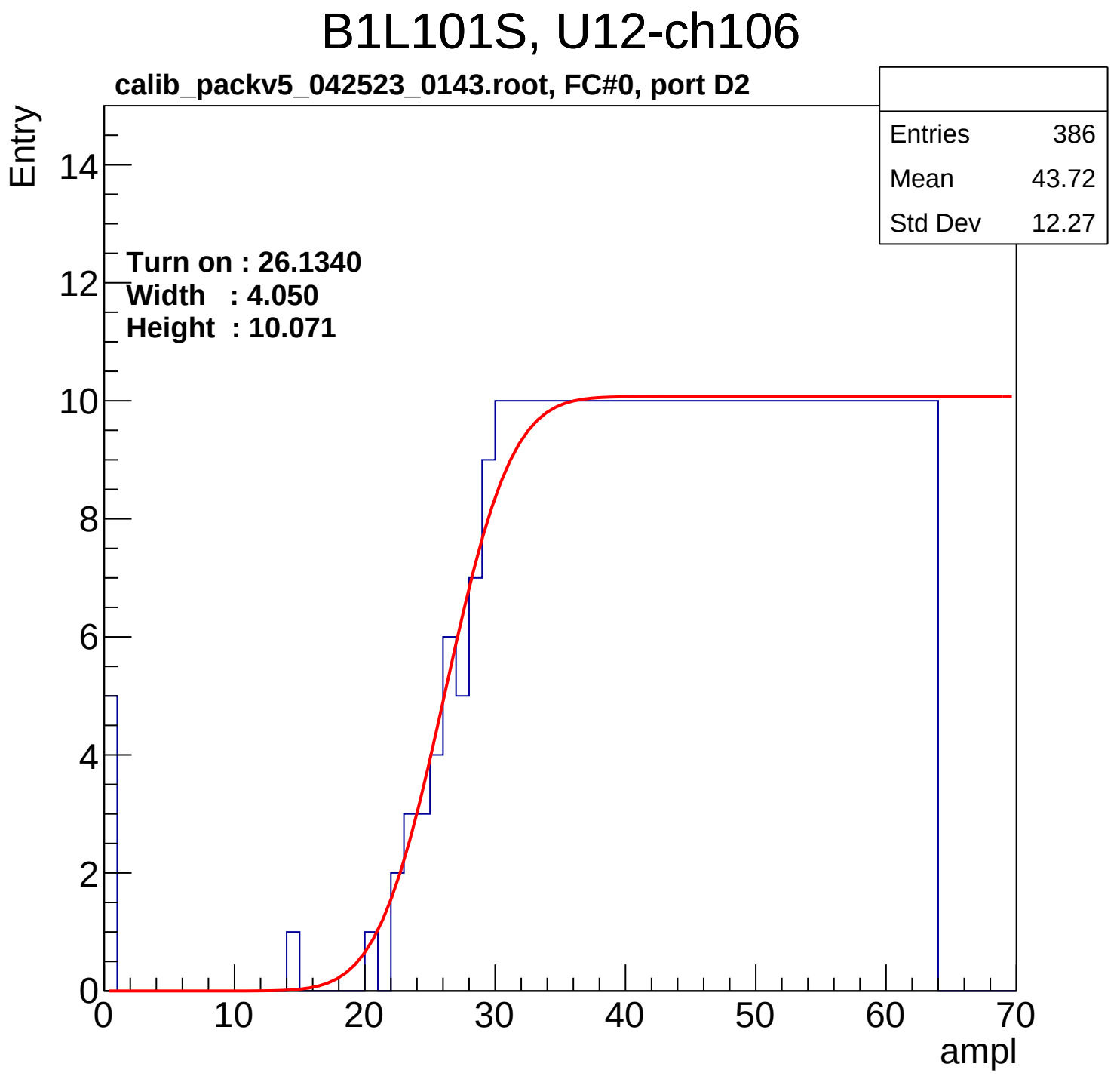

B1L101S, U12-ch101
calib_packv5_042523_0143.root, FC#0, port D2
Entries 365
Mean 44.98
Std Dev 11.18
Turn on : 28.4405
Width : 4.032
Height : 10.117
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

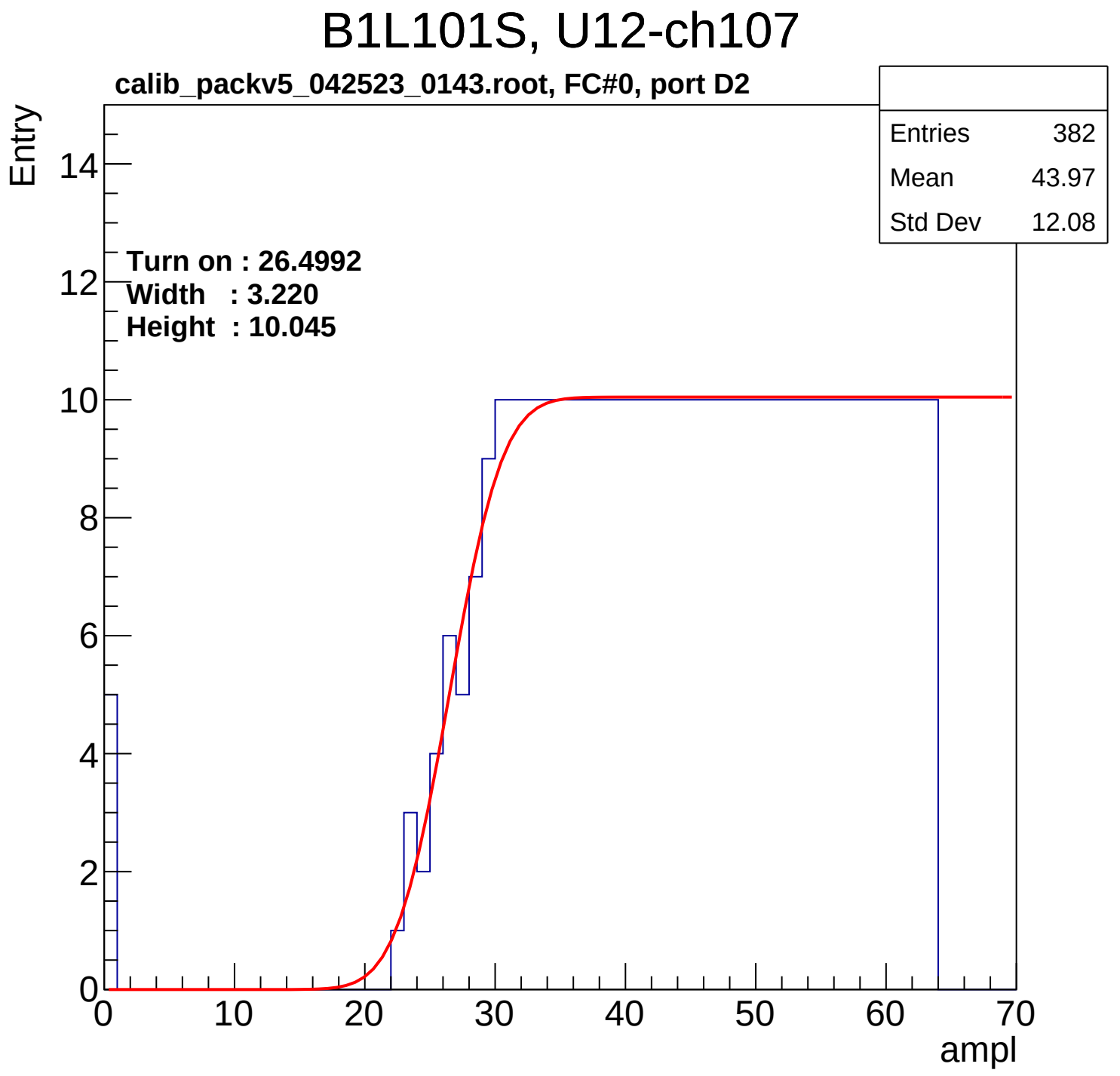

B1L101S, U12-ch102
calib_packv5_042523_0143.root, FC#0, port D2
Entries 341
Mean 45.98
Std Dev 11.08
Turn on : 30.6988
Width : 3.226
Height : 10.053
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

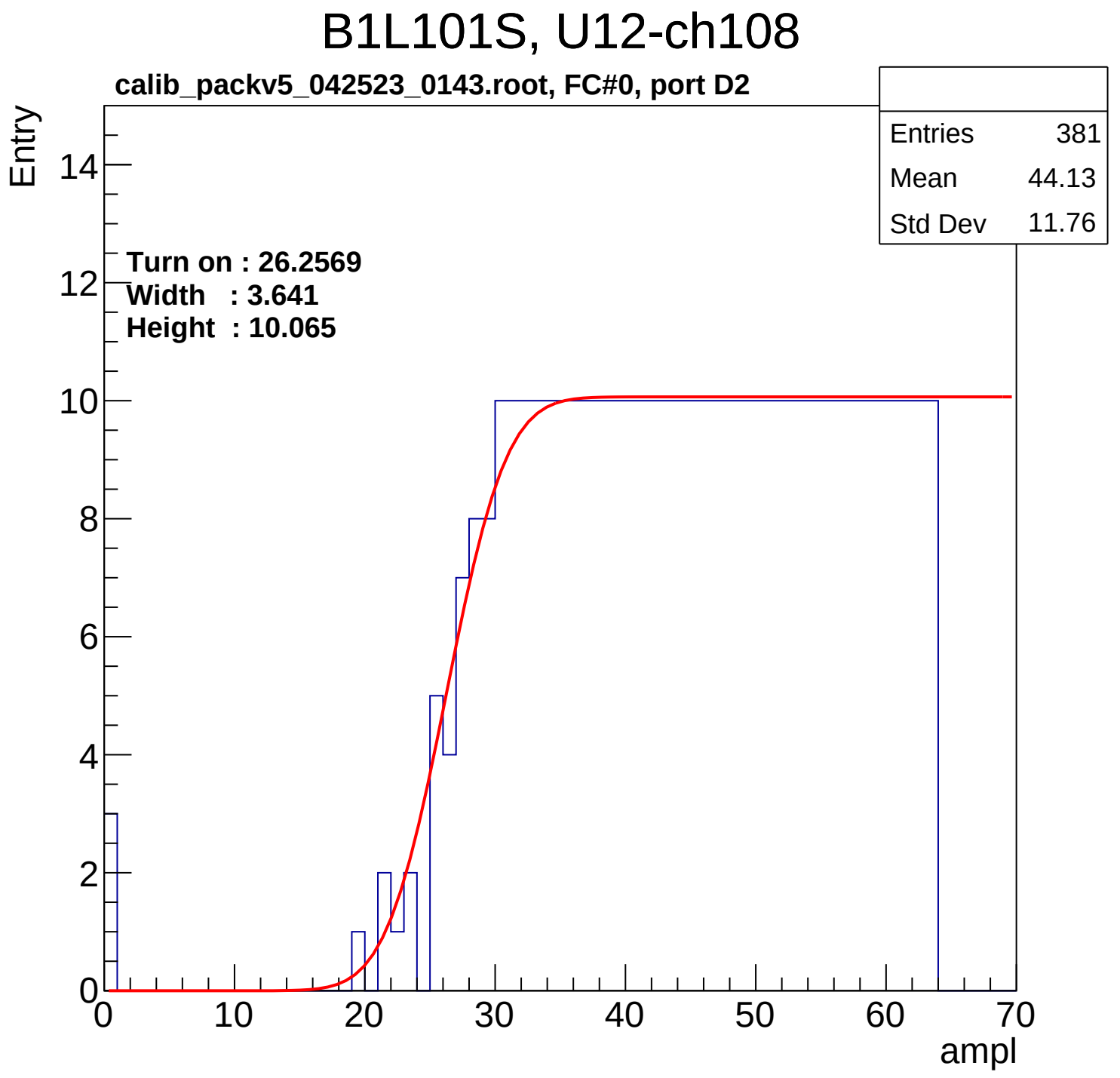

B1L101S, U12-ch103
calib_packv5_042523_0143.root, FC#0, port D2
Entries 352
Mean 45.7
Std Dev 10.6
Turn on : 29.5894
Width : 3.340
Height : 10.075
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

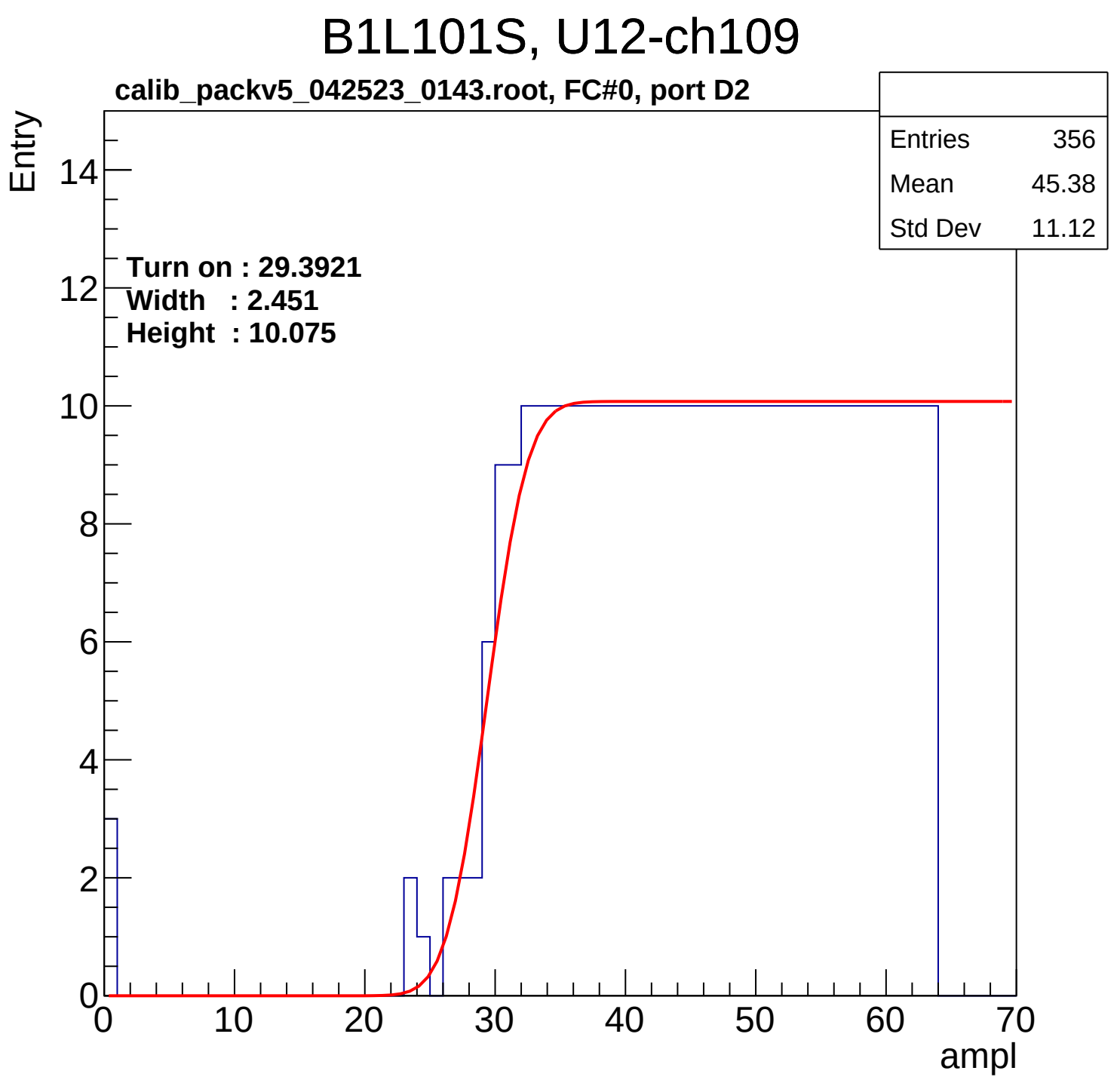

B1L101S, U12-ch104
calib_packv5_042523_0143.root, FC#0, port D2
Entries 401
Mean 43.24
Std Dev 12.04
Turn on : 24.4699
Width : 2.908
Height : 10.041
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

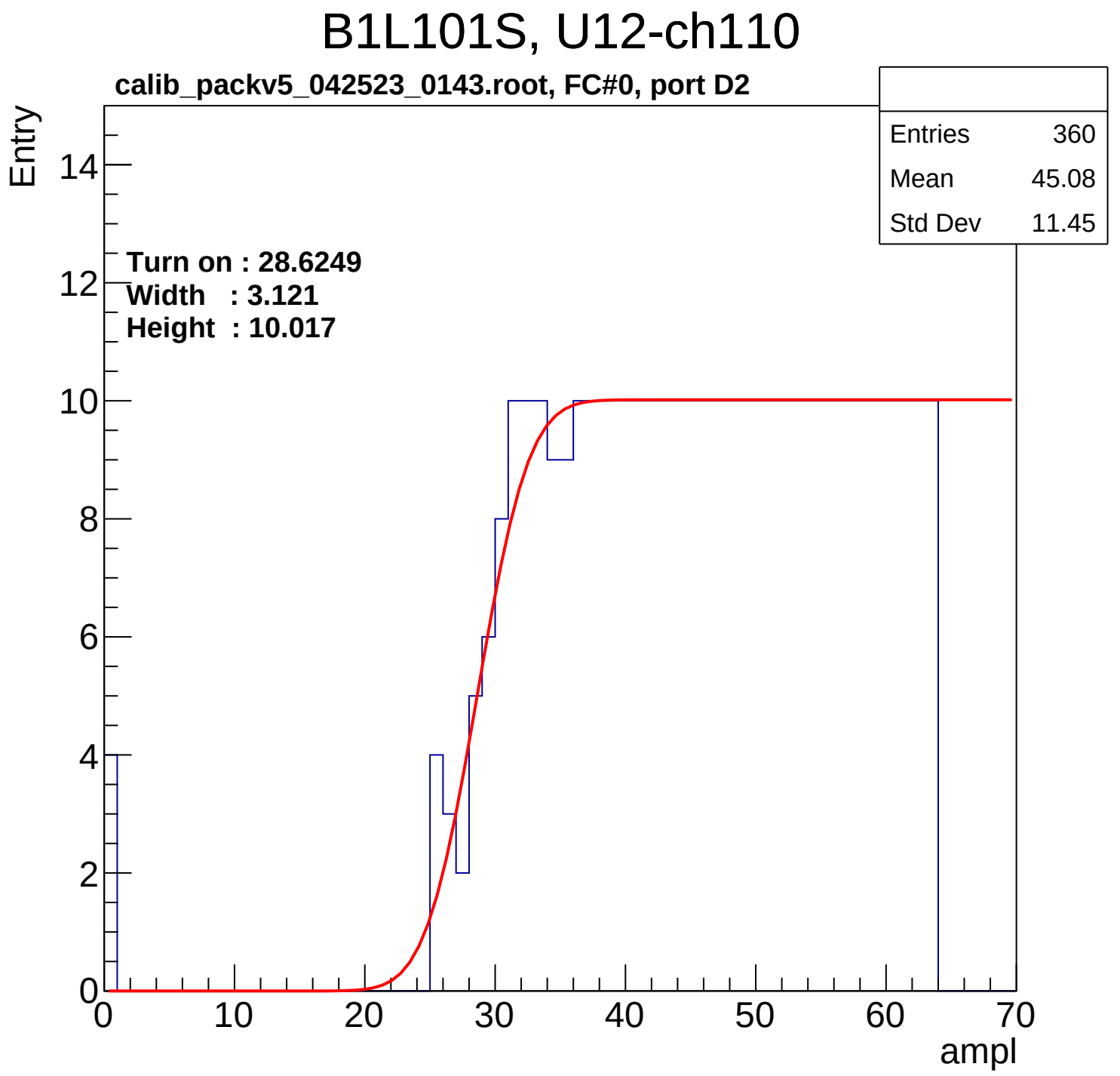

B1L101S, U12-ch105
calib_packv5_042523_0143.root, FC#0, port D2
Entries 357
Mean 45.17
Std Dev 11.57
Turn on : 29.4603
Width : 2.447
Height : 10.059
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

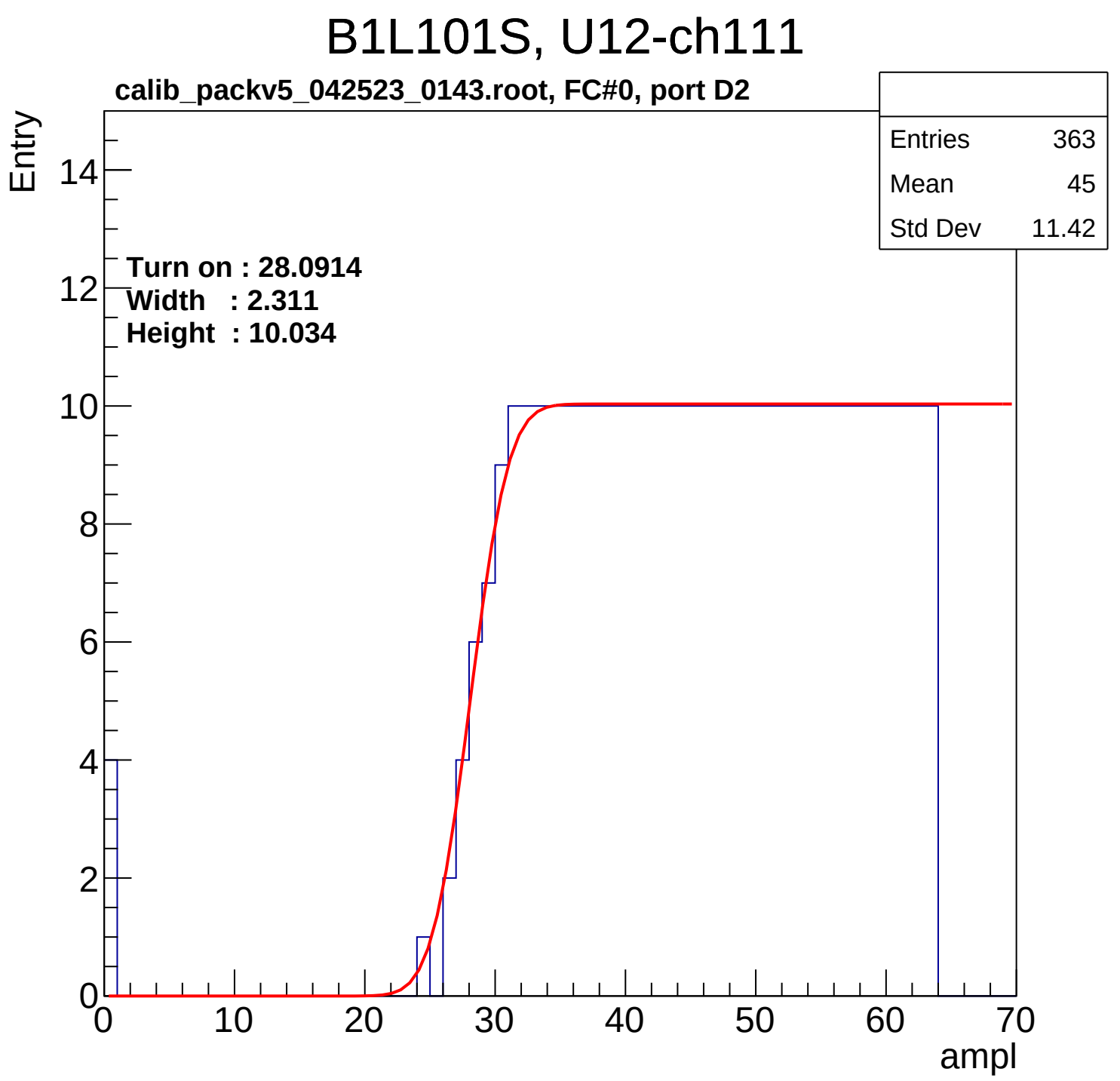

B1L101S, U12-ch106
calib_packv5_042523_0143.root, FC#0, port D2
Entries 386
Mean 43.72
Std Dev 12.27
Turn on : 26.1340
Width : 4.050
Height : 10.071
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

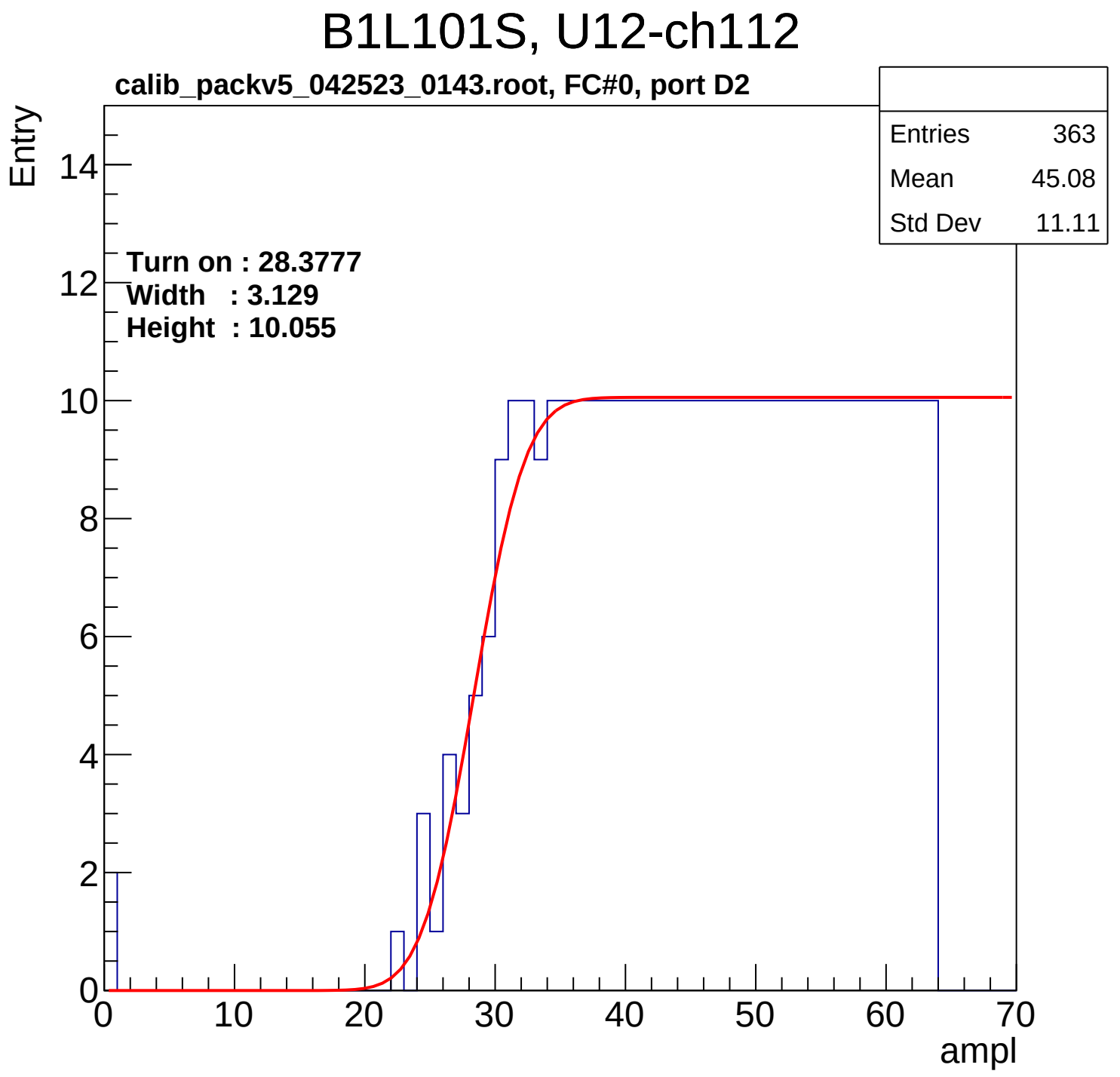

B1L101S, U12-ch107
calib_packv5_042523_0143.root, FC#0, port D2
Entries 382
Mean 43.97
Std Dev 12.08
Turn on : 26.4992
Width : 3.220
Height : 10.045
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

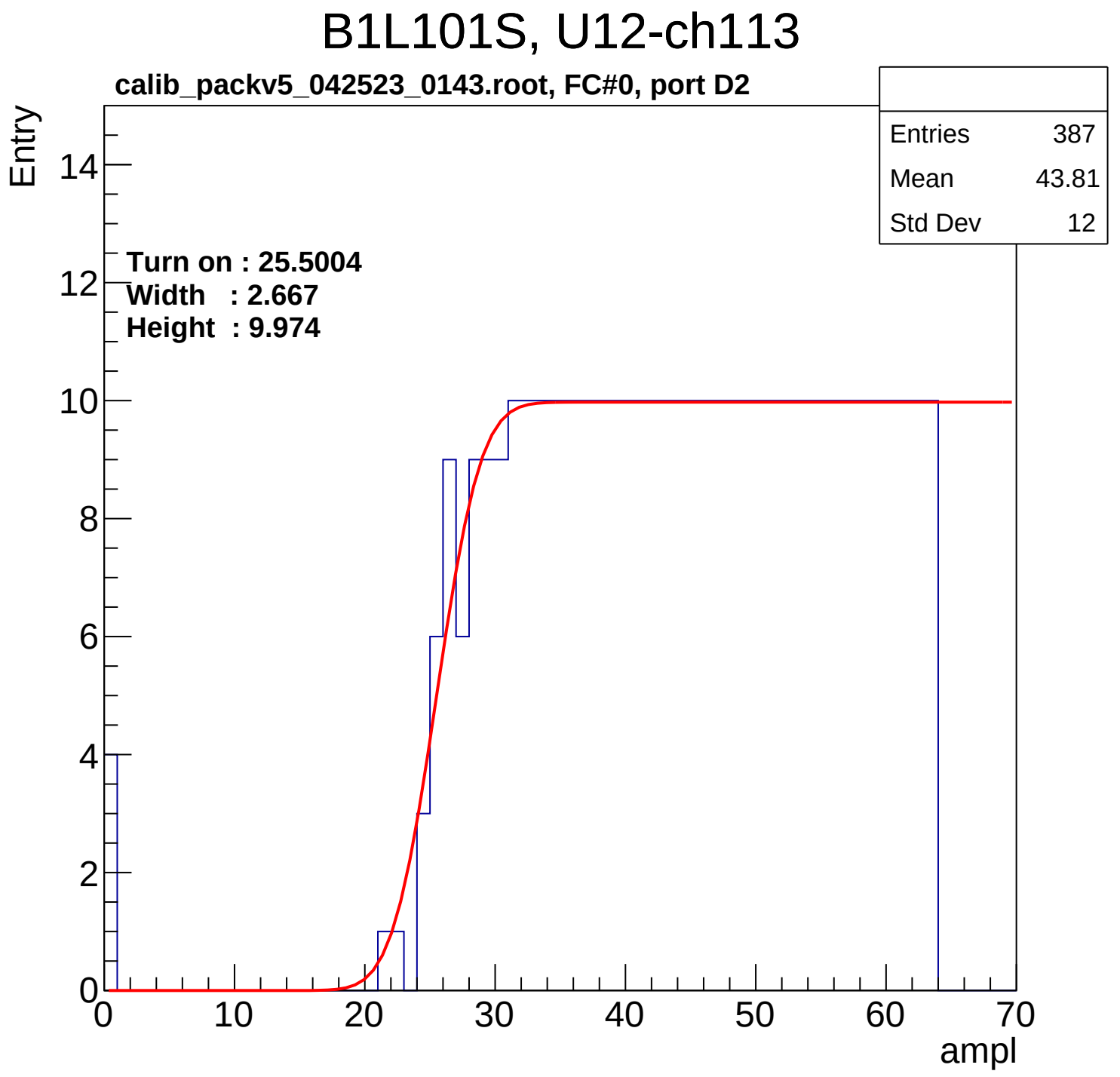

B1L101S, U12-ch108
calib_packv5_042523_0143.root, FC#0, port D2
Entries 381
Mean 44.13
Std Dev 11.76
Turn on : 26.2569
Width : 3.641
Height : 10.065
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

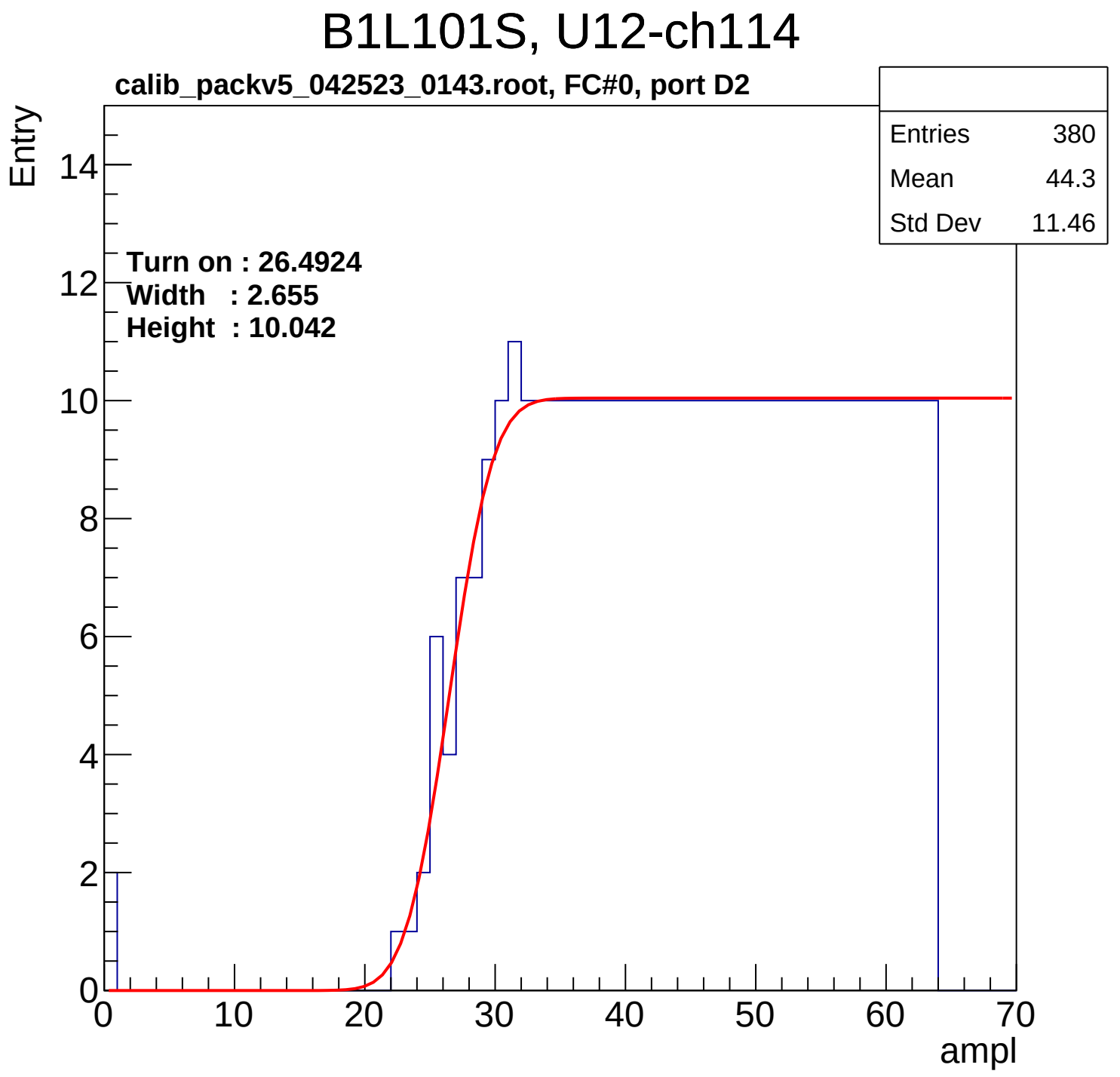

B1L101S, U12-ch109
calib_packv5_042523_0143.root, FC#0, port D2
Entries 356
Mean 45.38
Std Dev 11.12
Turn on : 29.3921
Width : 2.451
Height : 10.075
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

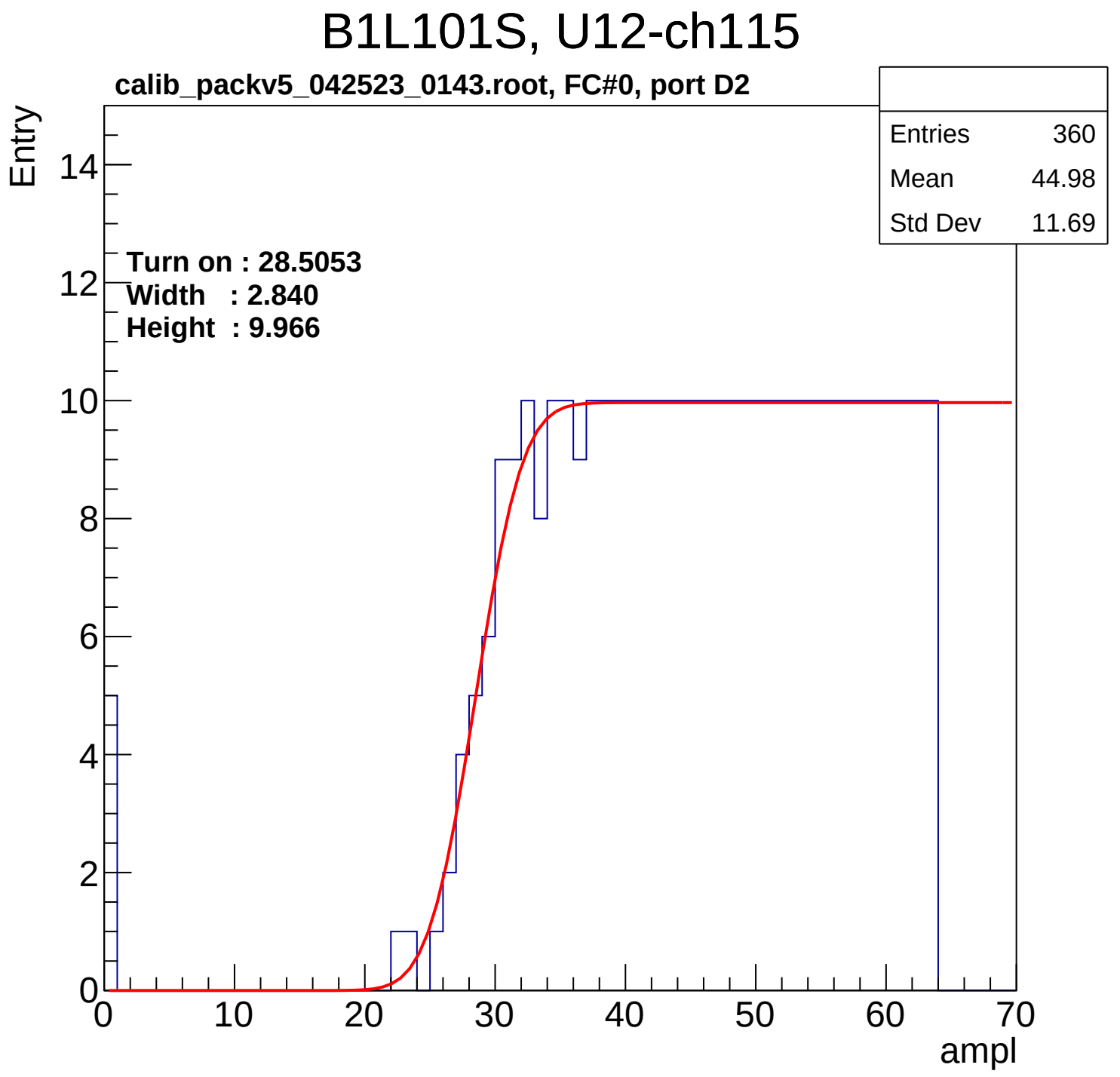

B1L101S, U12-ch110
calib_packv5_042523_0143.root, FC#0, port D2
Entries 360
Mean 45.08
Std Dev 11.45
Turn on : 28.6249
Width : 3.121
Height : 10.017
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

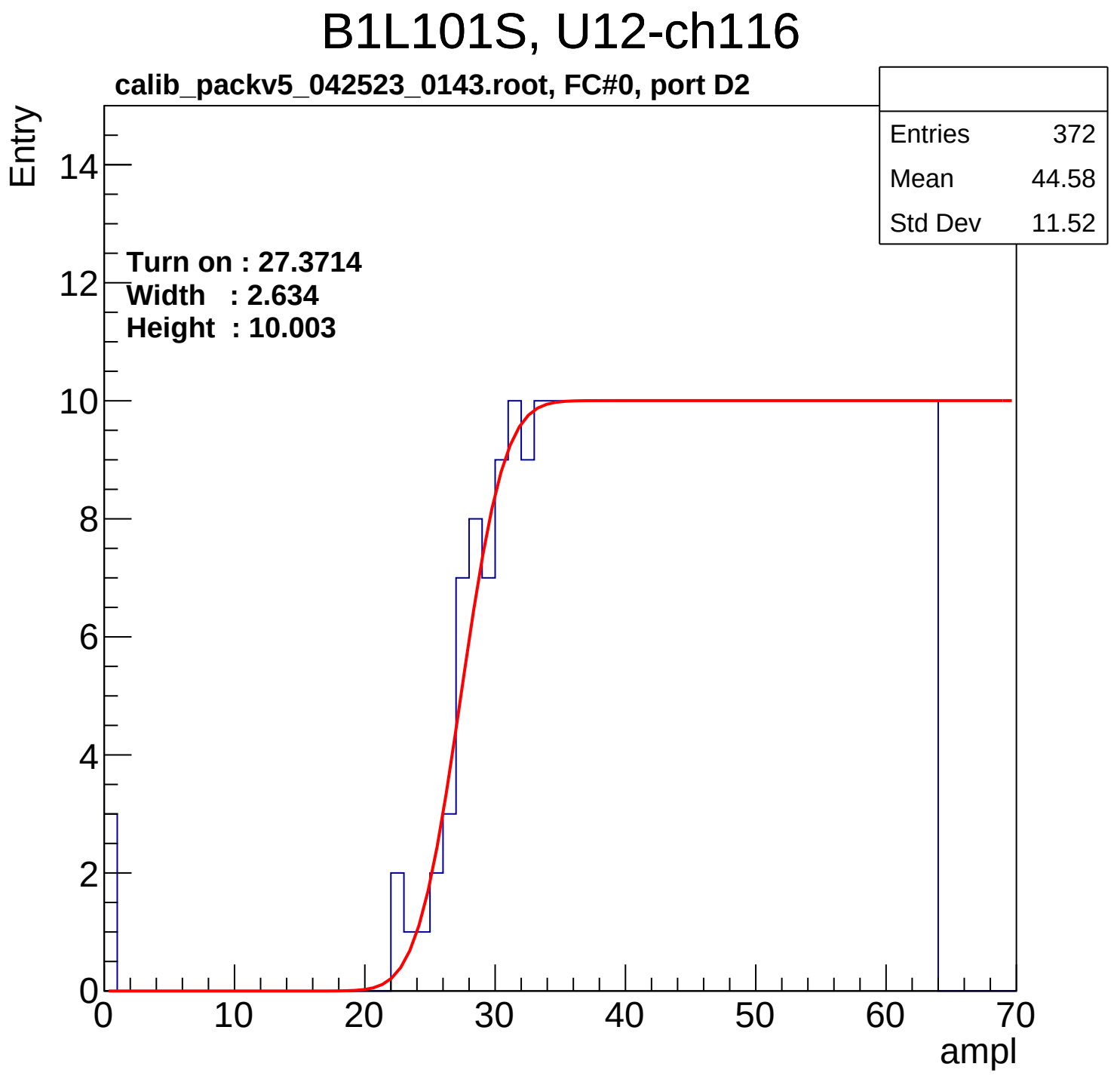

B1L101S, U12-ch111
calib_packv5_042523_0143.root, FC#0, port D2
Entries 363
Mean 45
Std Dev 11.42
Turn on : 28.0914
Width : 2.311
Height : 10.034
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

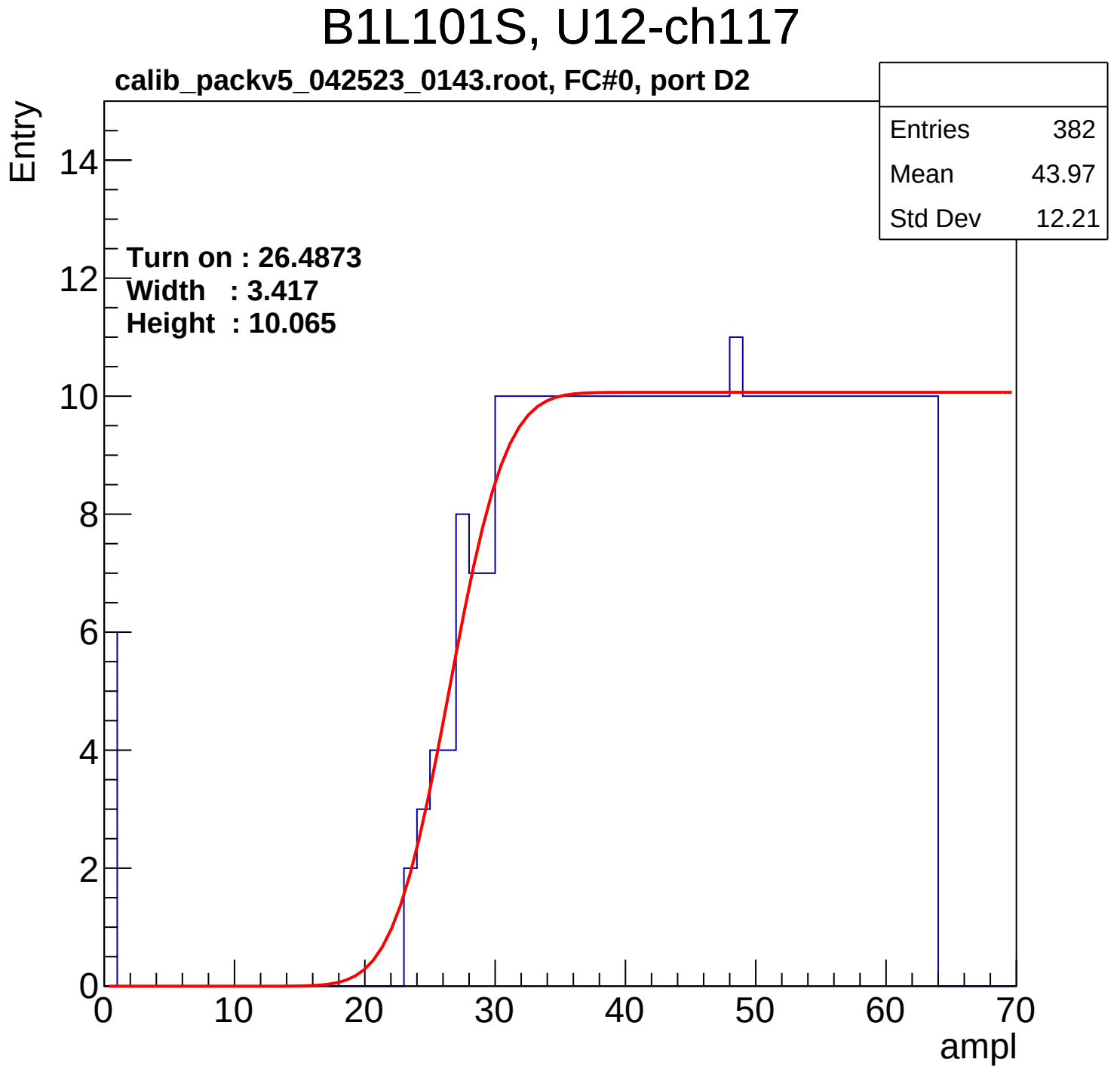

B1L101S, U12-ch112
calib_packv5_042523_0143.root, FC#0, port D2
Entries 363
Mean 45.08
Std Dev 11.11
Turn on : 28.3777
Width : 3.129
Height : 10.055
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

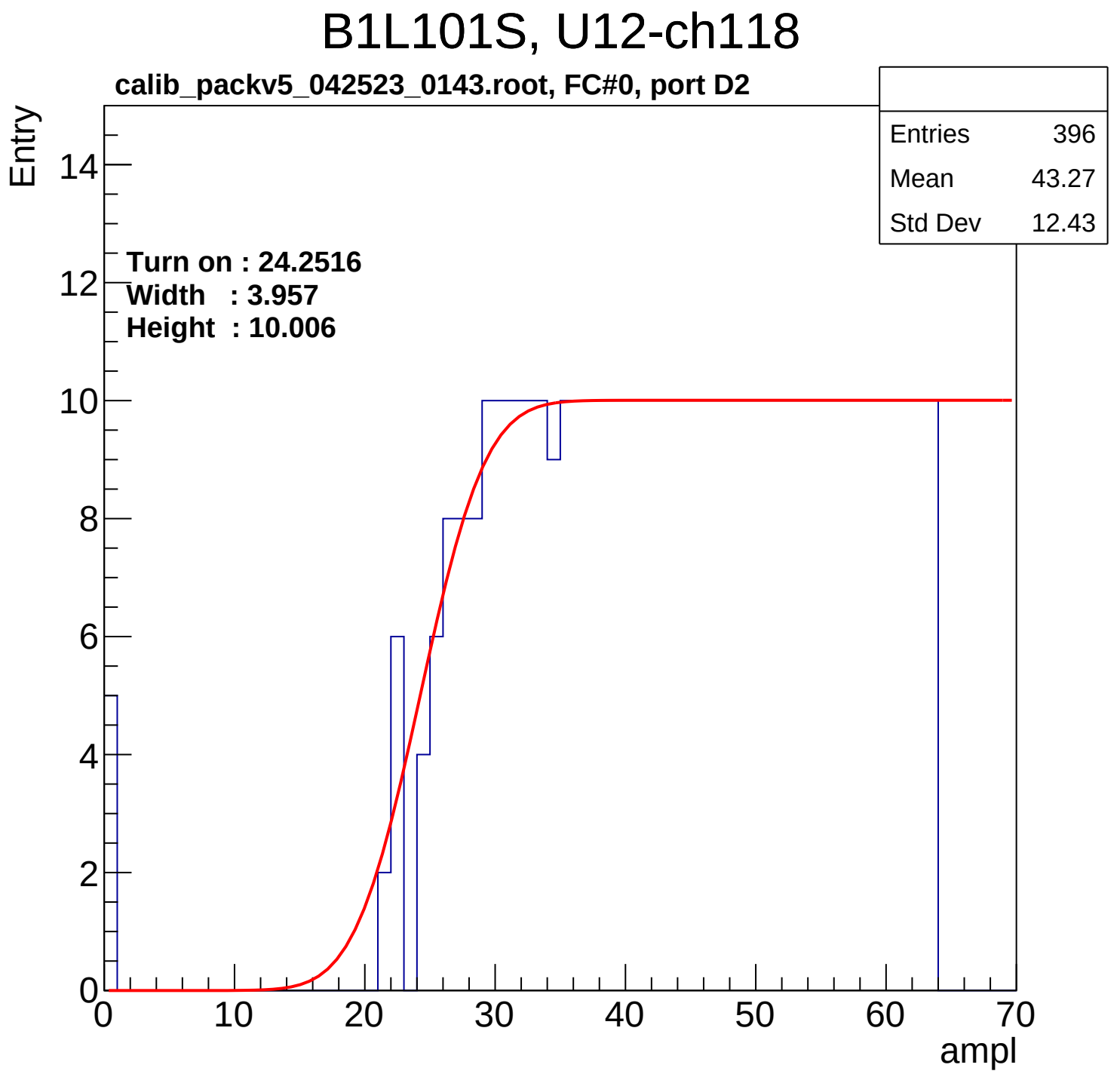

B1L101S, U12-ch113
calib_packv5_042523_0143.root, FC#0, port D2
Entries 387
Mean 43.81
Std Dev 12
Turn on : 25.5004
Width : 2.667
Height : 9.974
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

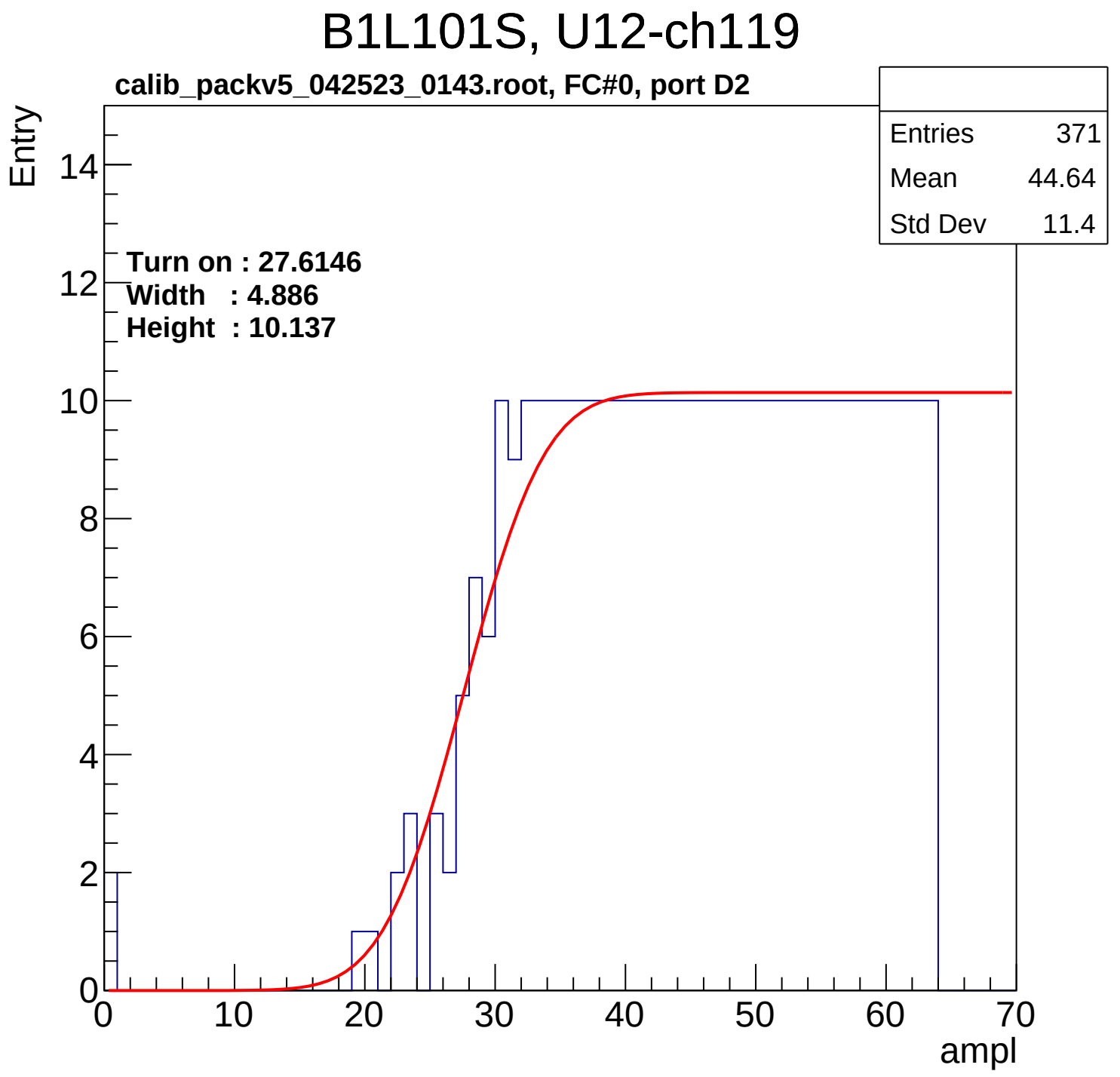

B1L101S, U12-ch114
calib_packv5_042523_0143.root, FC#0, port D2
Entries 380
Mean 44.3
Std Dev 11.46
Turn on : 26.4924
Width : 2.655
Height : 10.042
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

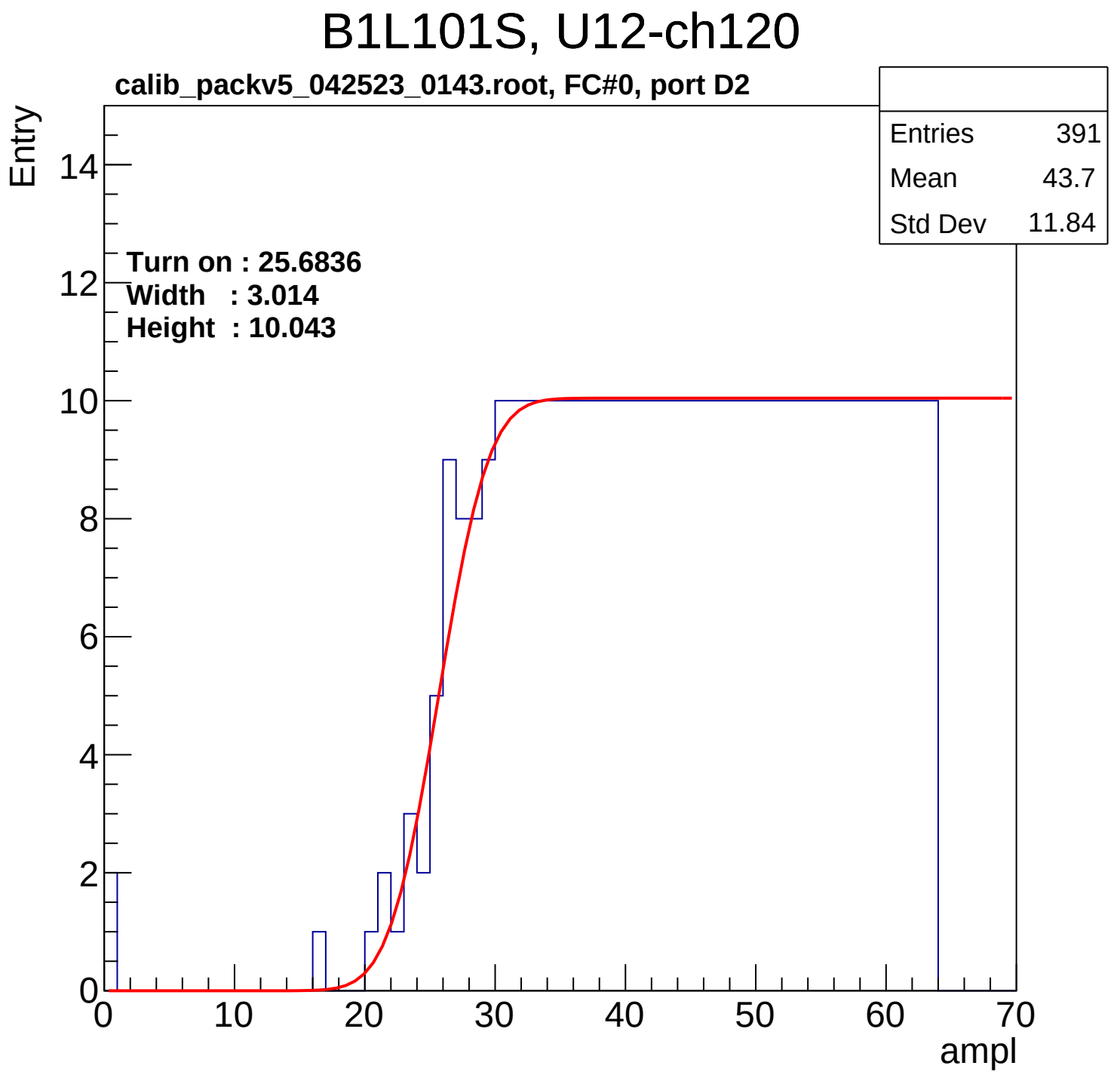

B1L101S, U12-ch115
calib_packv5_042523_0143.root, FC#0, port D2
Entries 360
Mean 44.98
Std Dev 11.69
Turn on : 28.5053
Width : 2.840
Height : 9.966
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

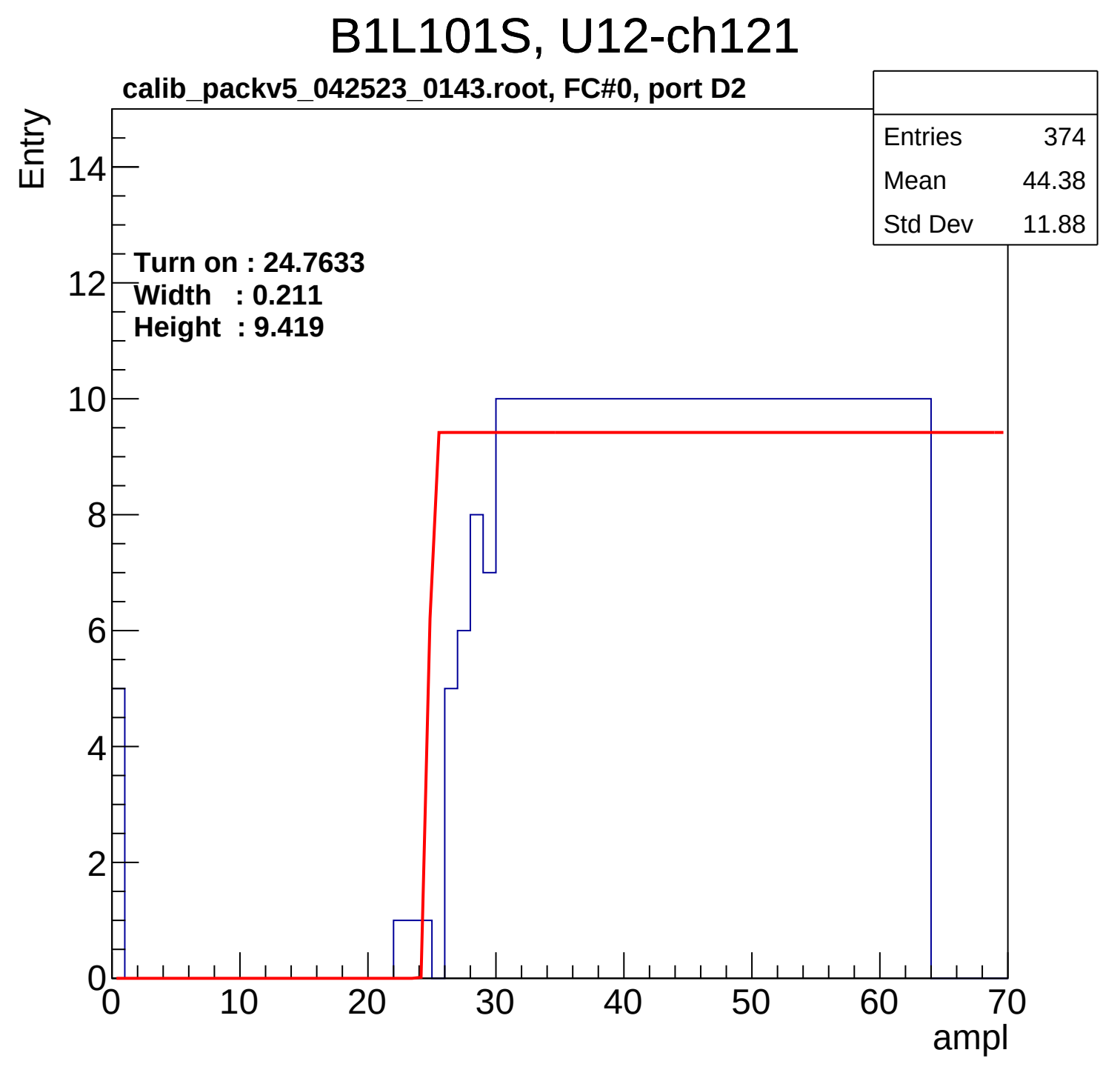

B1L101S, U12-ch116
calib_packv5_042523_0143.root, FC#0, port D2
Entries 372
Mean 44.58
Std Dev 11.52
Turn on : 27.3714
Width : 2.634
Height : 10.003
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

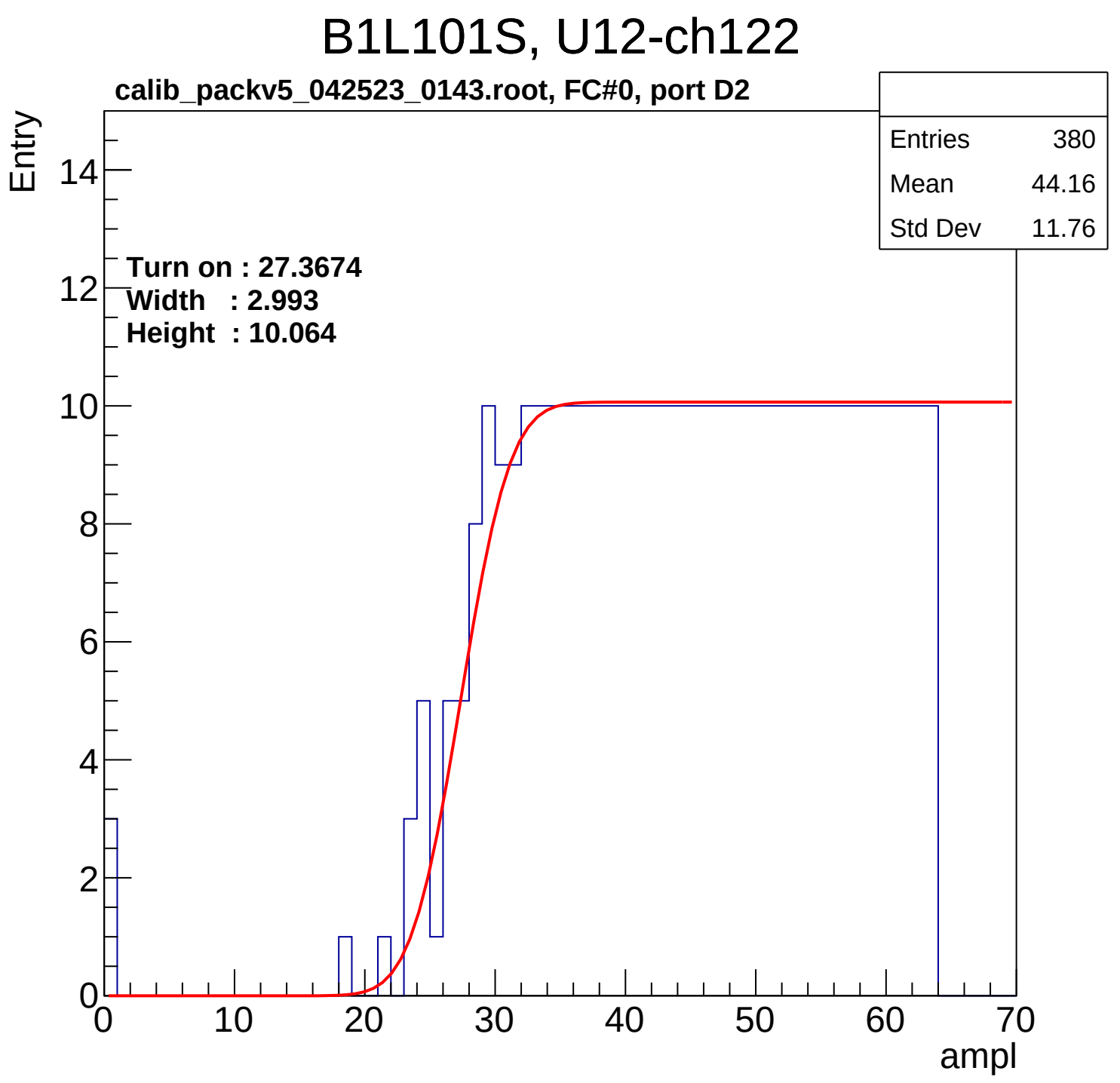

B1L101S, U12-ch117
calib_packv5_042523_0143.root, FC#0, port D2
Entries 382
Mean 43.97
Std Dev 12.21
Turn on : 26.4873
Width : 3.417
Height : 10.065
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

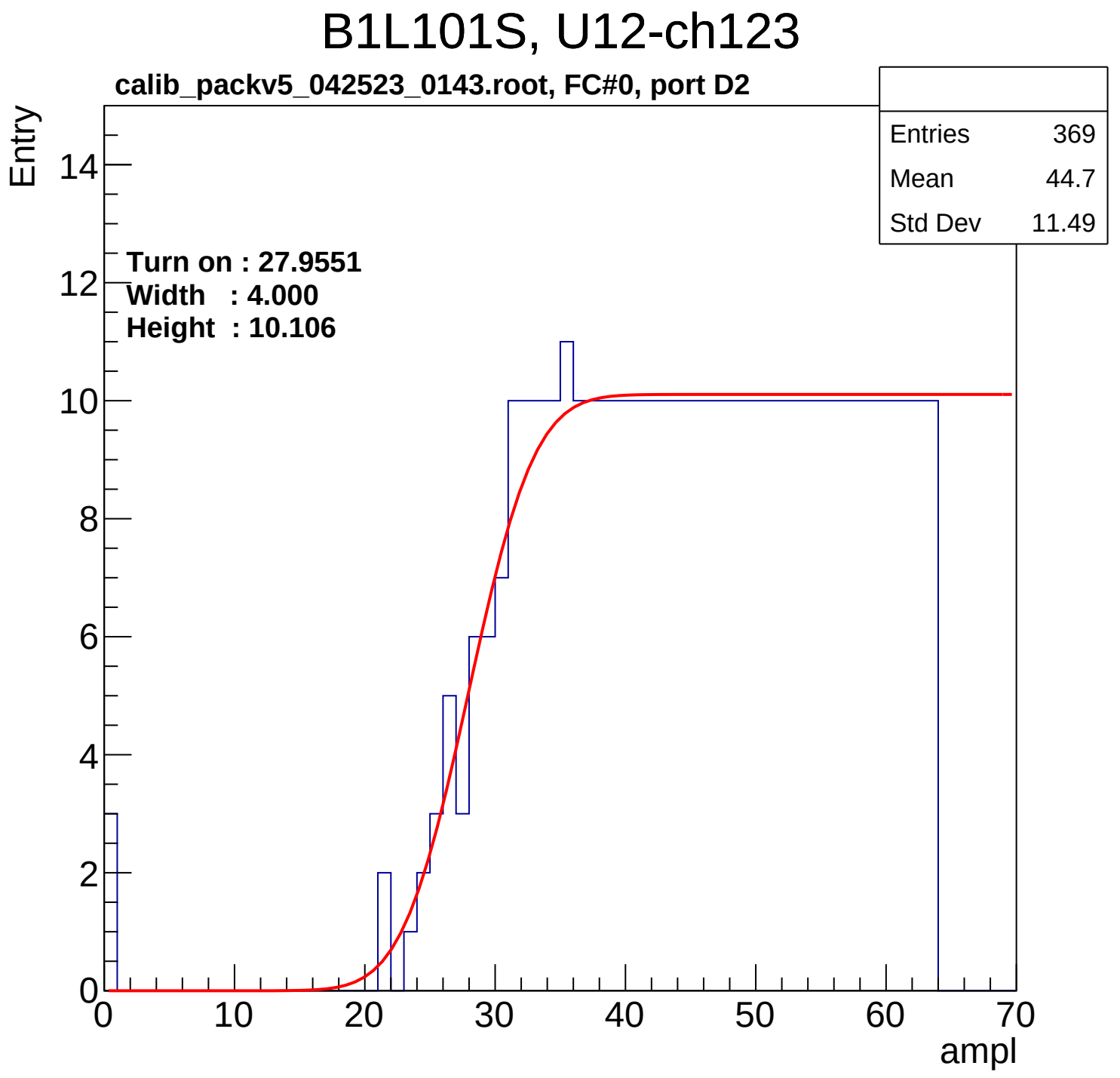

B1L101S, U12-ch118
calib_packv5_042523_0143.root, FC#0, port D2
Entries 396
Mean 43.27
Std Dev 12.43
Turn on : 24.2516
Width : 3.957
Height : 10.006
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

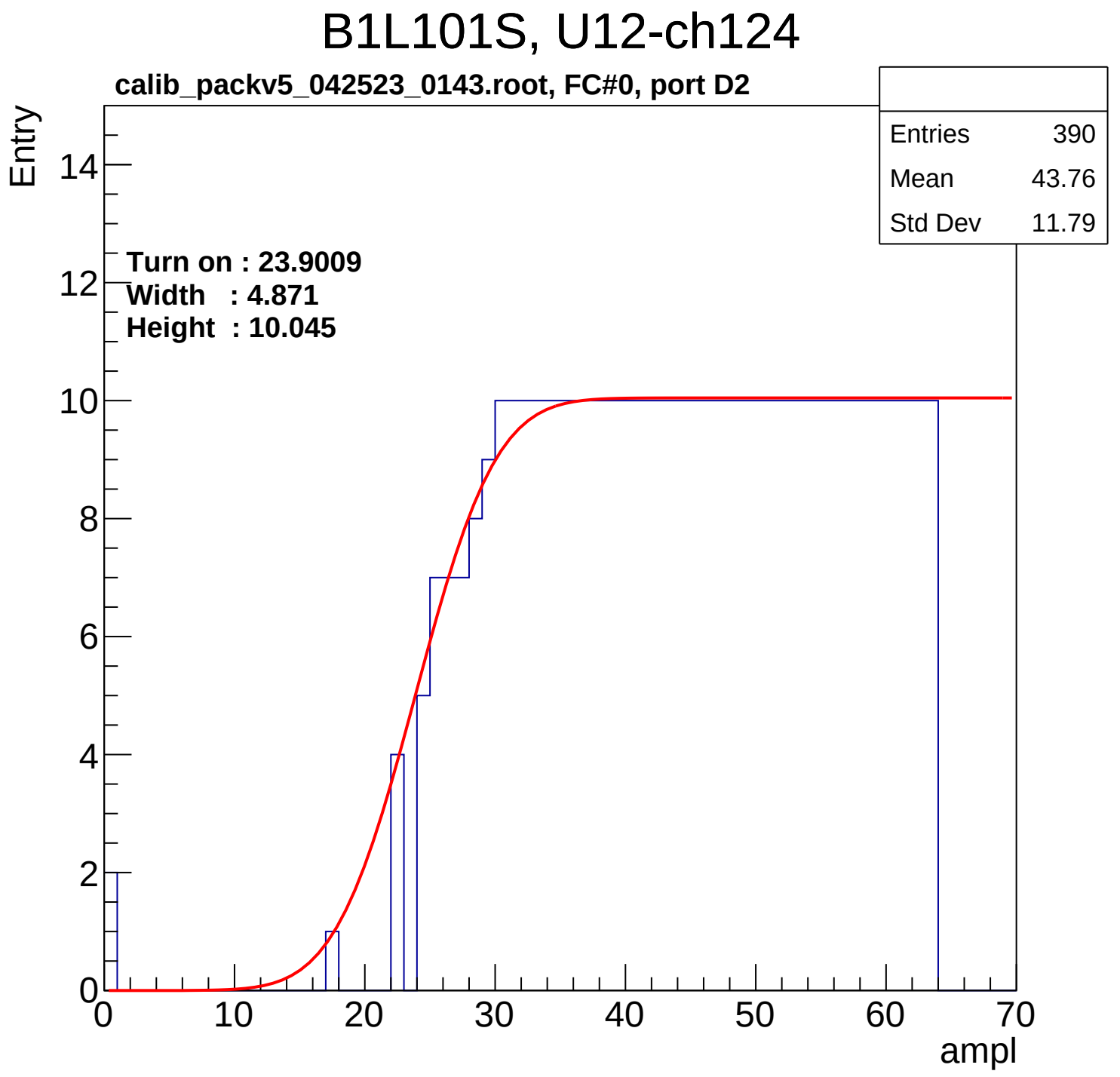

B1L101S, U12-ch119
calib_packv5_042523_0143.root, FC#0, port D2
Entries 371
Mean 44.64
Std Dev 11.4
Turn on : 27.6146
Width : 4.886
Height : 10.137
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

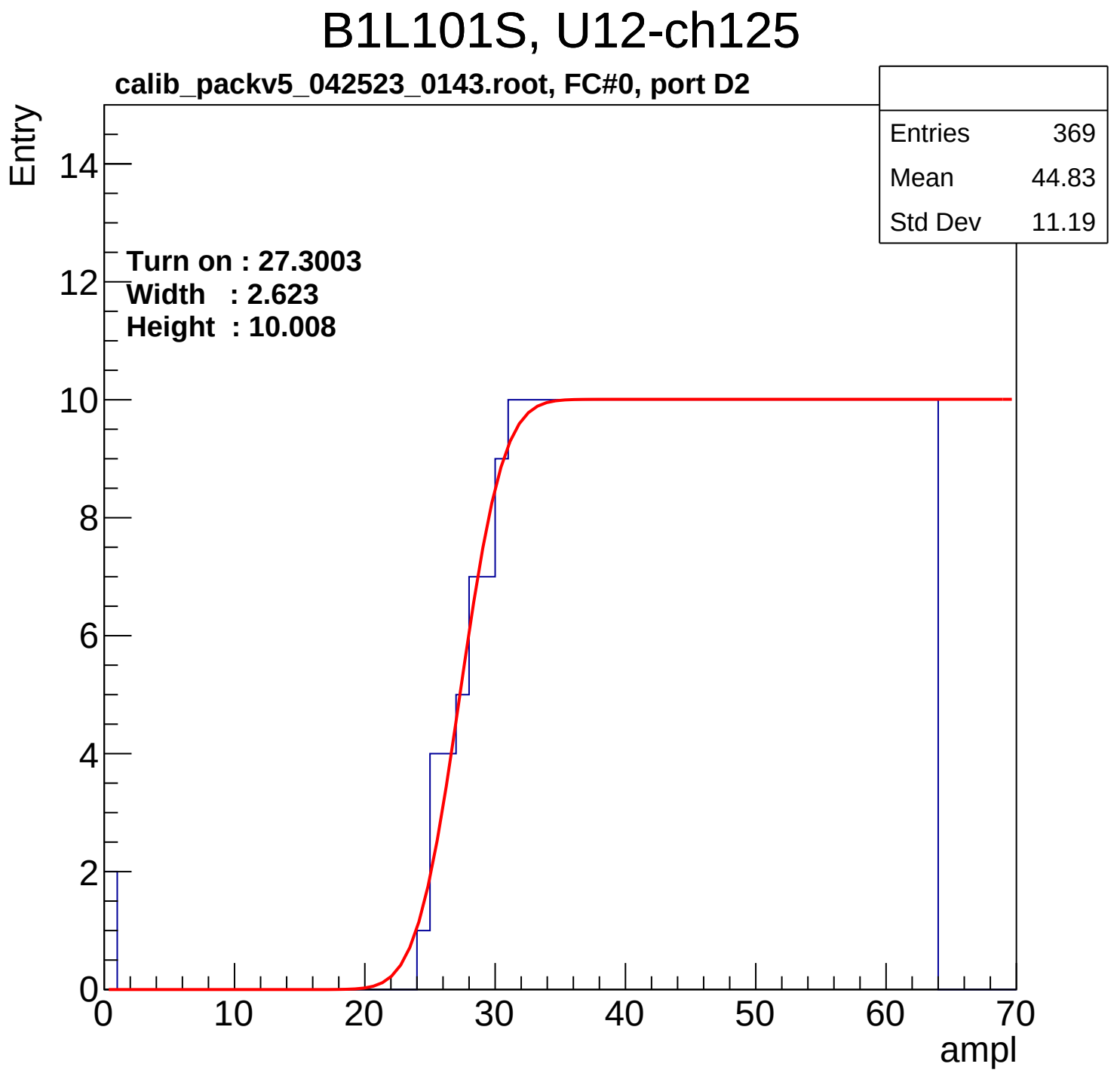

B1L101S, U12-ch120
calib_packv5_042523_0143.root, FC#0, port D2
Entries 391
Mean 43.7
Std Dev 11.84
Turn on : 25.6836
Width : 3.014
Height : 10.043
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

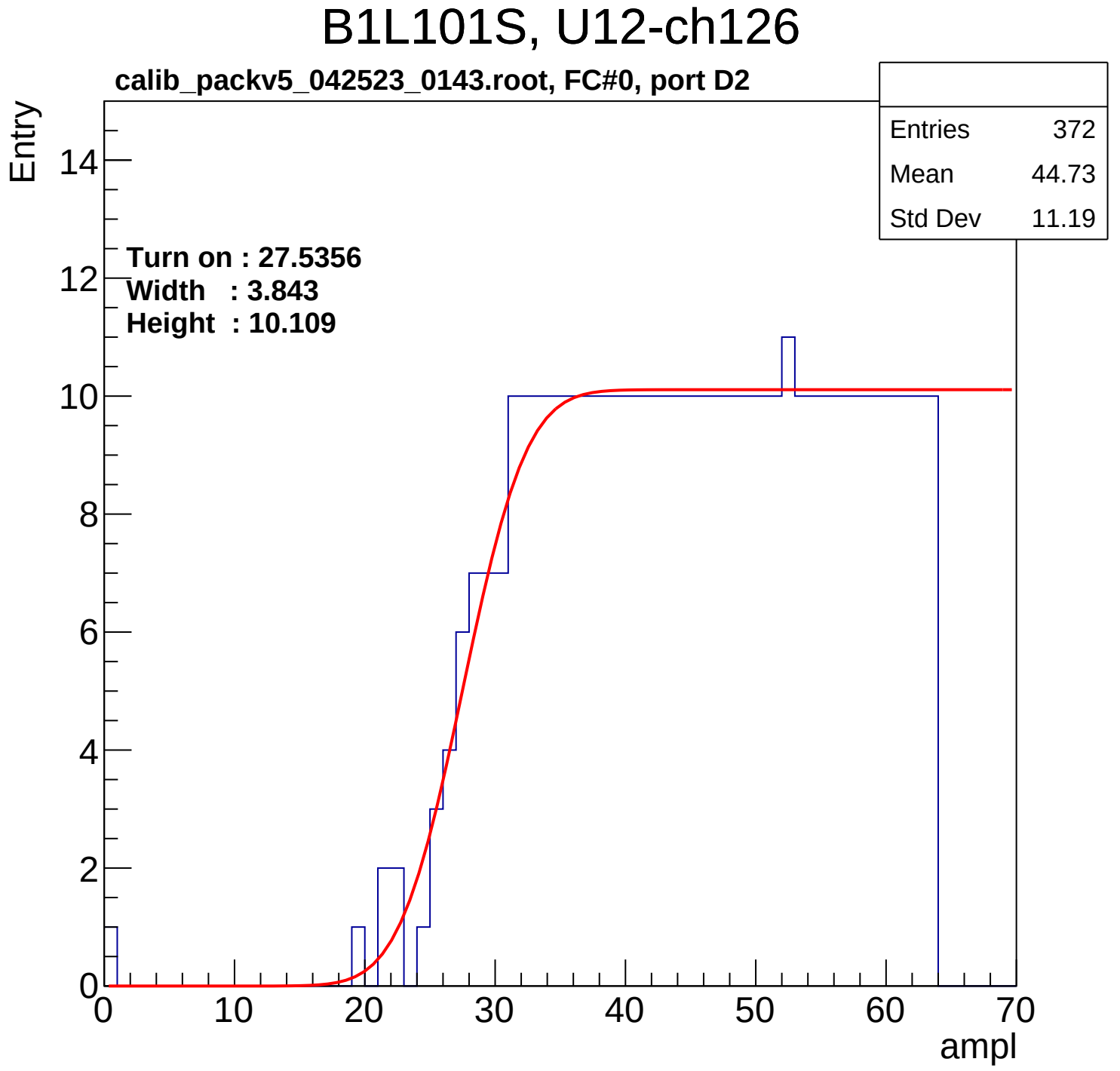

B1L101S, U12-ch121
calib_packv5_042523_0143.root, FC#0, port D2
Entries 374
Mean 44.38
Std Dev 11.88
Turn on : 24.7633
Width : 0.211
Height : 9.419
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

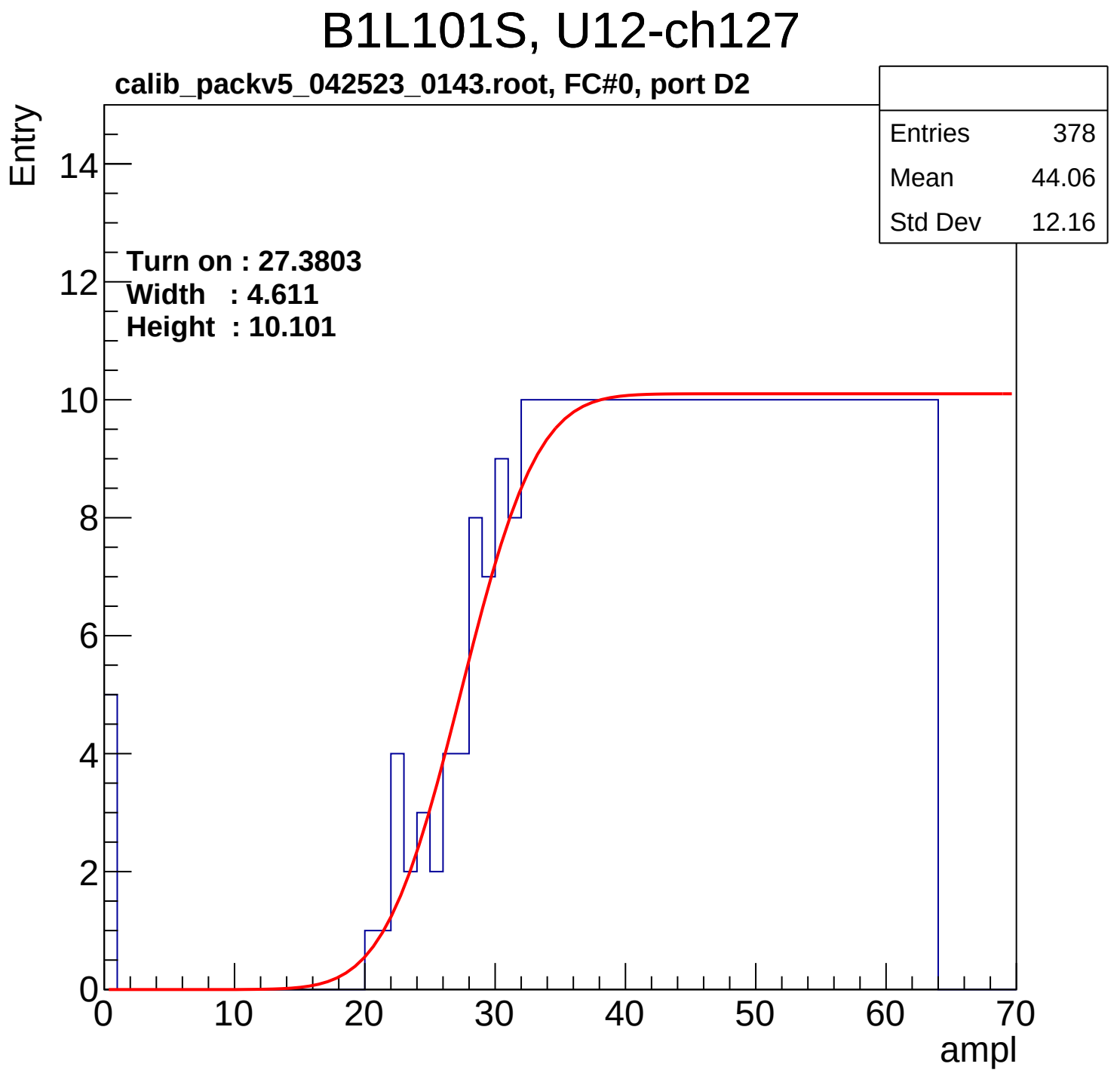

B1L101S, U12-ch122
calib_packv5_042523_0143.root, FC#0, port D2
Entries 380
Mean 44.16
Std Dev 11.76
Turn on : 27.3674
Width : 2.993
Height : 10.064
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

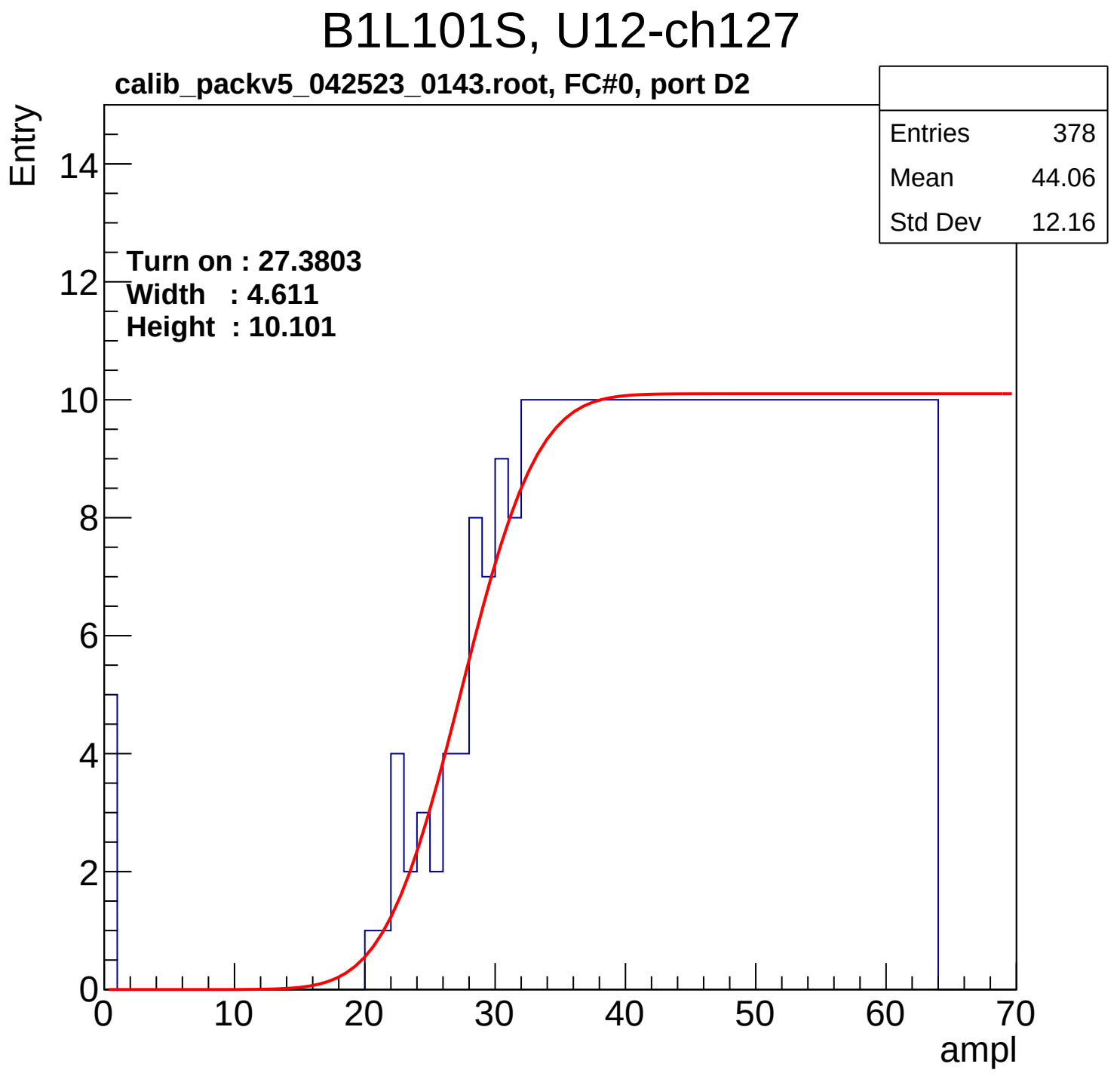

B1L101S, U12-ch123
calib_packv5_042523_0143.root, FC#0, port D2
Entries 369
Mean 44.7
Std Dev 11.49
Turn on : 27.9551
Width : 4.000
Height : 10.106
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L101S, U12-ch124
calib_packv5_042523_0143.root, FC#0, port D2
Entries 390
Mean 43.76
Std Dev 11.79
Turn on : 23.9009
Width : 4.871
Height : 10.045
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L101S, U12-ch125
calib_packv5_042523_0143.root, FC#0, port D2
Entries 369
Mean 44.83
Std Dev 11.19
Turn on : 27.3003
Width : 2.623
Height : 10.008
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L101S, U12-ch126
calib_packv5_042523_0143.root, FC#0, port D2
Entries 372
Mean 44.73
Std Dev 11.19
Turn on : 27.5356
Width : 3.843
Height : 10.109
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L101S, U12-ch127
calib_packv5_042523_0143.root, FC#0, port D2
Entries 378
Mean 44.06
Std Dev 12.16
Turn on : 27.3803
Width : 4.611
Height : 10.101
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L101S, U12-ch127
calib_packv5_042523_0143.root, FC#0, port D2
Entries 378
Mean 44.06
Std Dev 12.16
Turn on : 27.3803
Width : 4.611
Height : 10.101
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70