

B1L101S, U19-ch0

calib_packv5_042523_0143.root, FC#0, port D2

Entries	385
Mean	44.05
Std Dev	11.52

Turn on : 26.4208

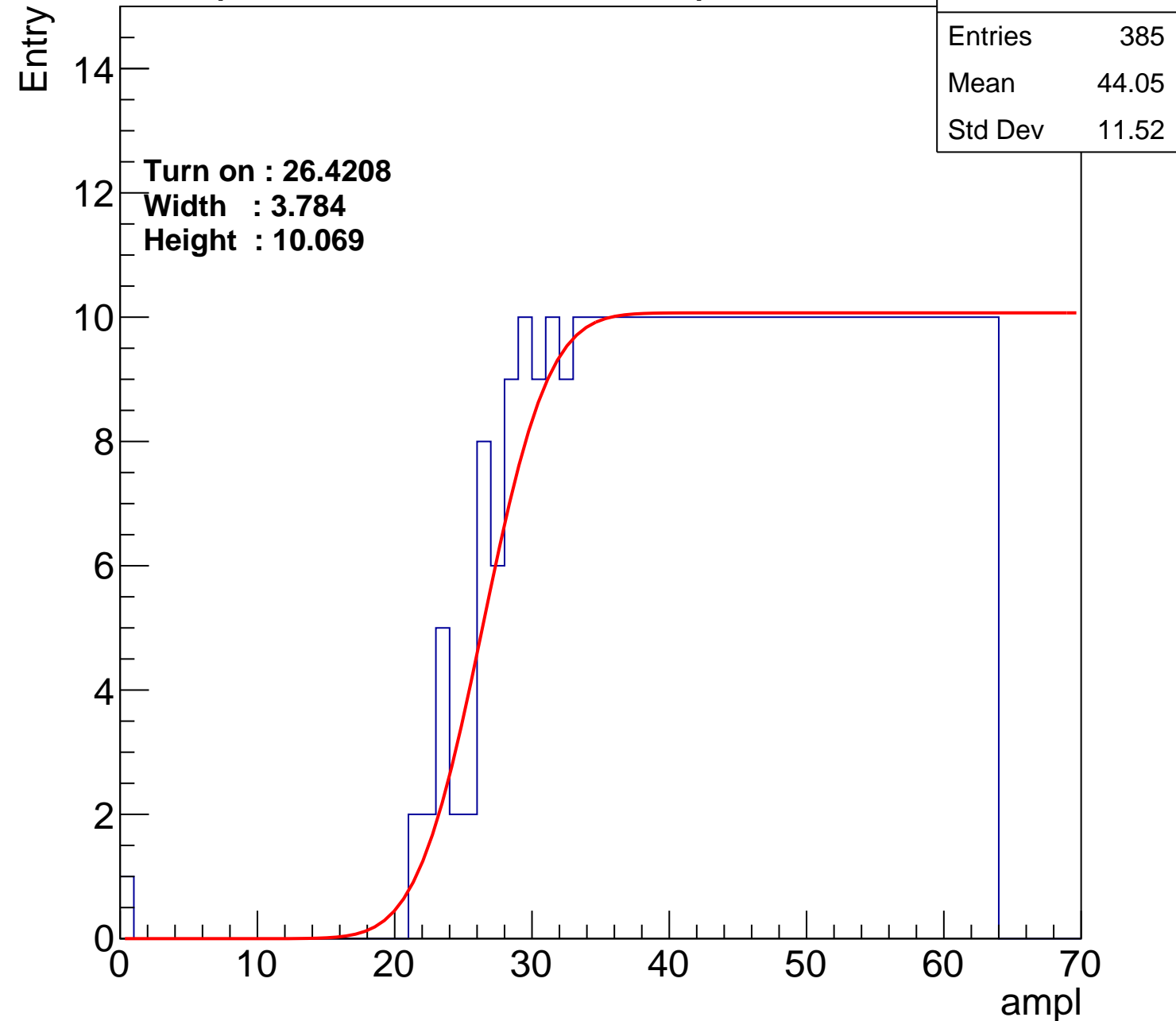
Width : 3.784

Height : 10.069

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch1

calib_packv5_042523_0143.root, FC#0, port D2

Entries	363
Mean	45.2
Std Dev	10.82

Turn on : 27.8847

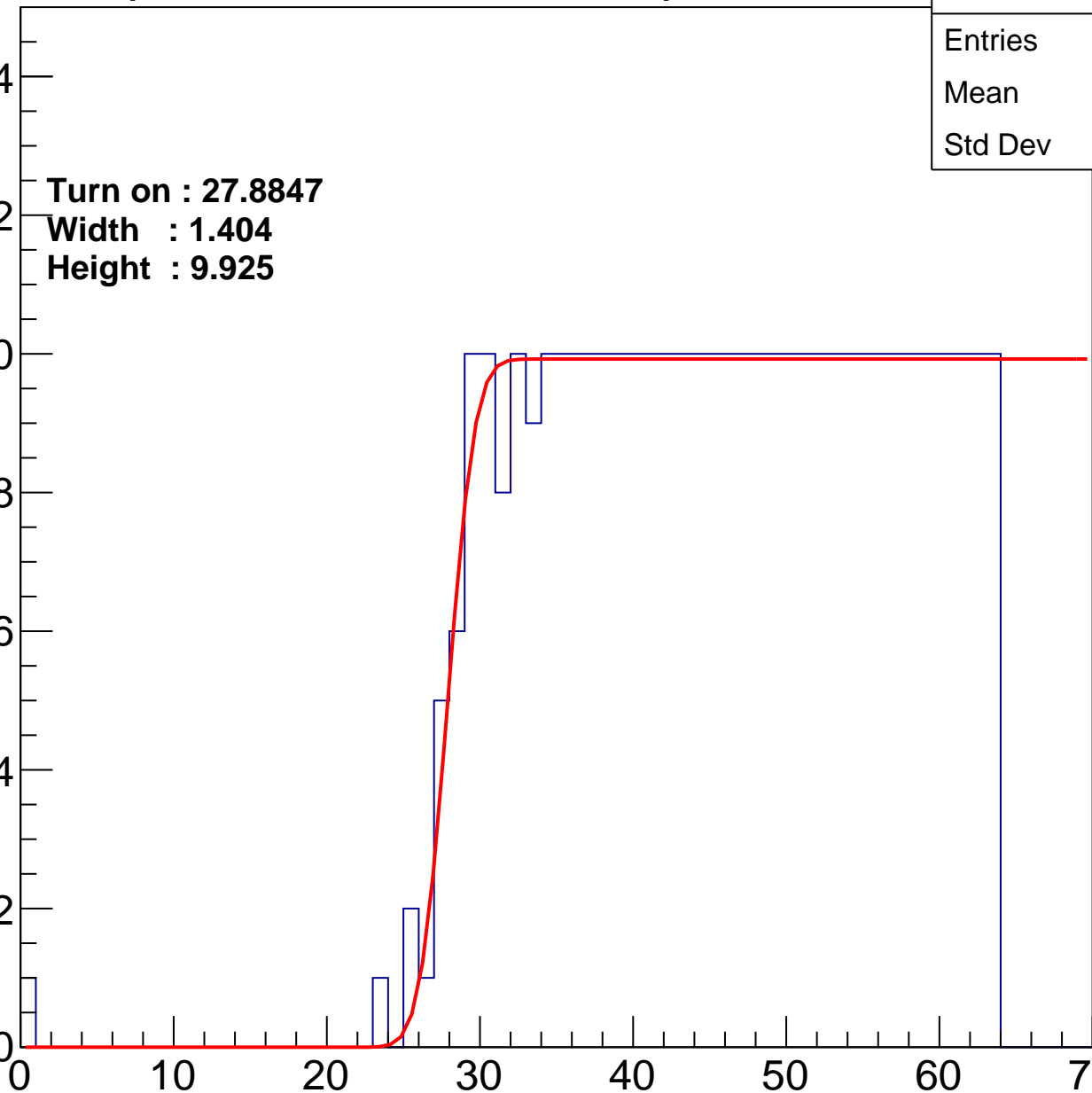
Width : 1.404

Height : 9.925

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch2

calib_packv5_042523_0143.root, FC#0, port D2

Entries	363
Mean	45
Std Dev	11.33

Turn on : 28.3593

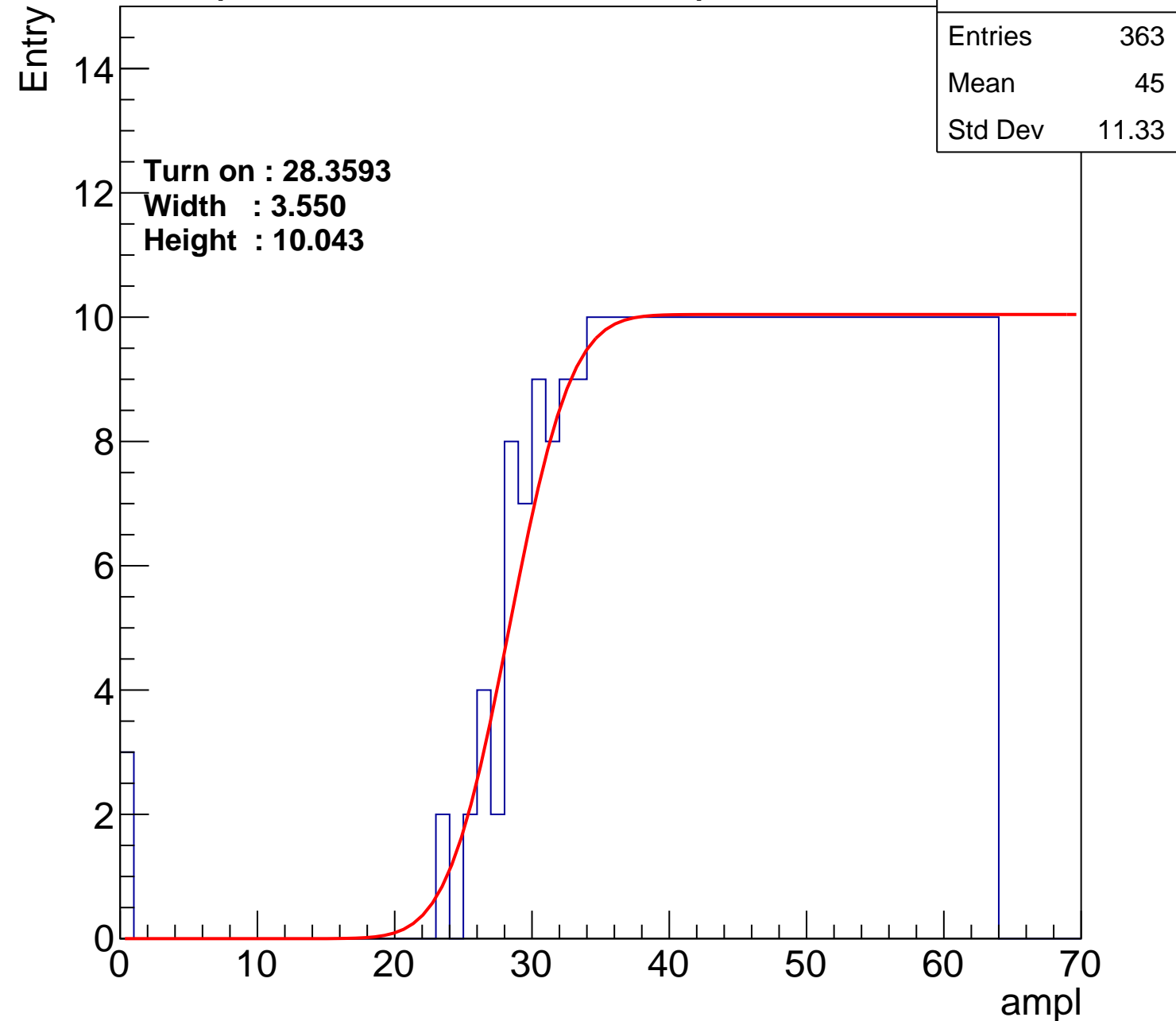
Width : 3.550

Height : 10.043

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch3

calib_packv5_042523_0143.root, FC#0, port D2

Entries	367
Mean	44.82
Std Dev	11.4

Turn on : 28.2052

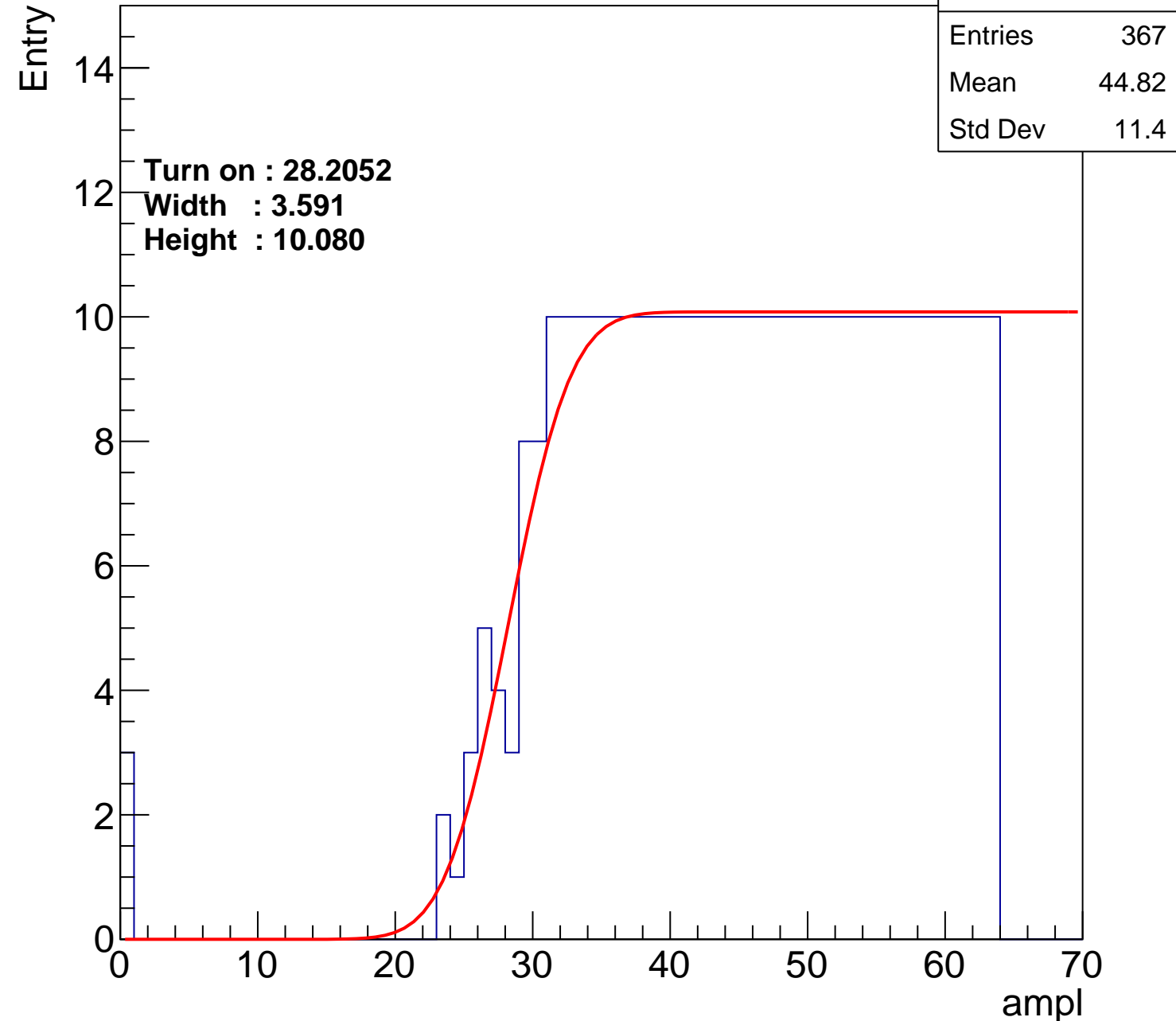
Width : 3.591

Height : 10.080

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch4

calib_packv5_042523_0143.root, FC#0, port D2

Entries	366
Mean	44.99
Std Dev	11.1

Turn on : 27.6574

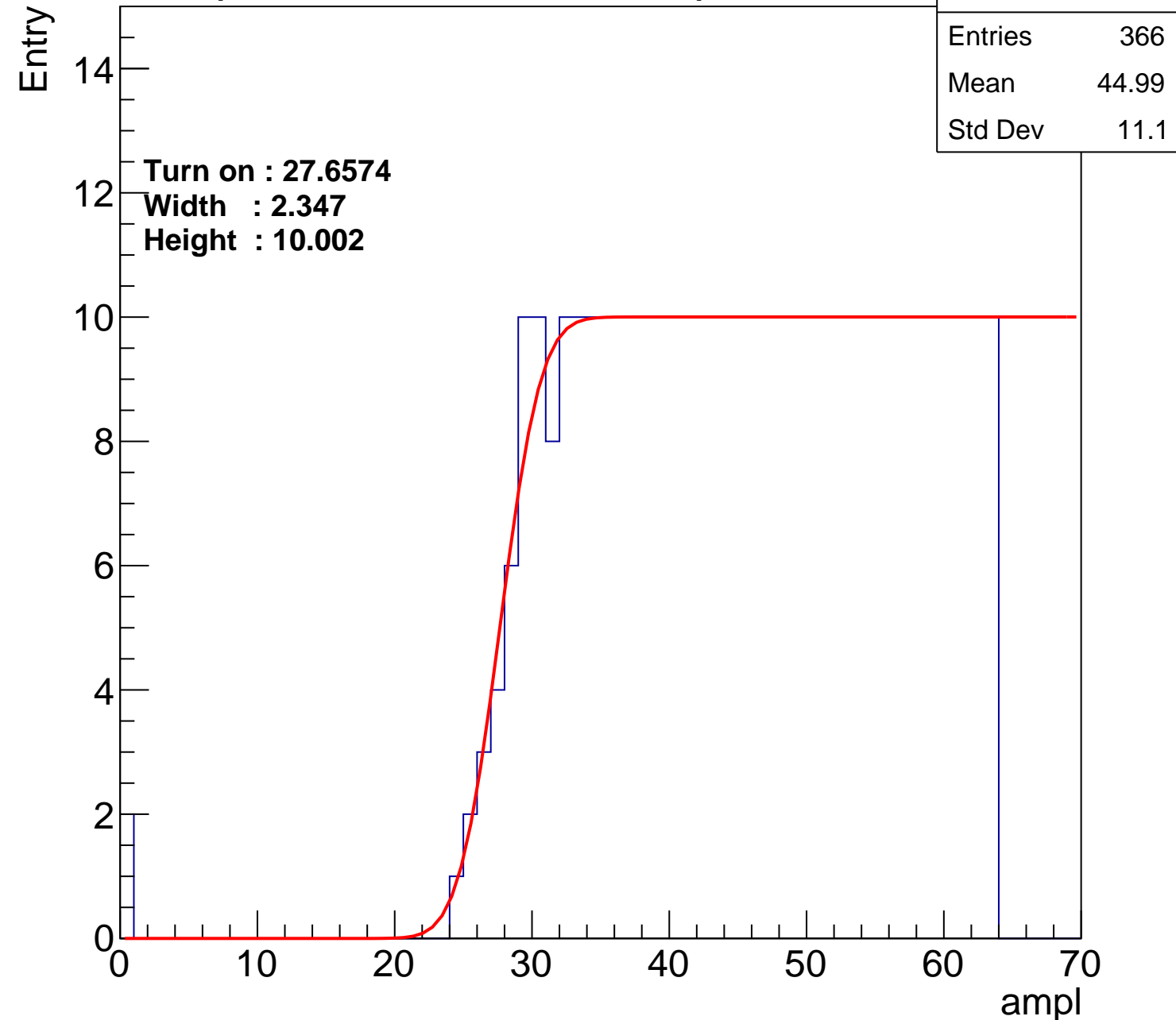
Width : 2.347

Height : 10.002

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch5

calib_packv5_042523_0143.root, FC#0, port D2

Entries	390
Mean	43.52
Std Dev	12.42

Turn on : 25.8177

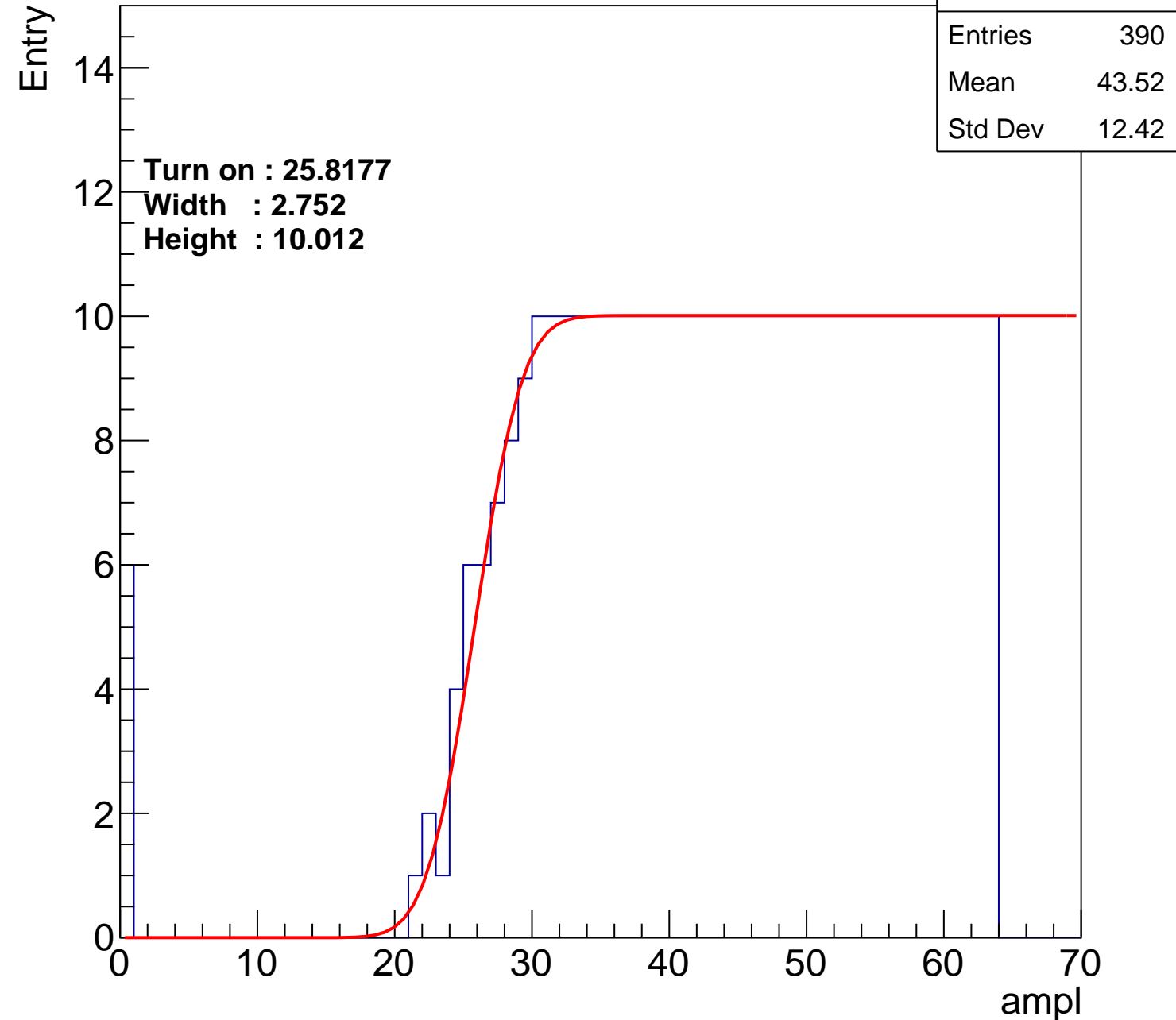
Width : 2.752

Height : 10.012

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch6

calib_packv5_042523_0143.root, FC#0, port D2

Entries	391
Mean	43.71
Std Dev	11.82

Turn on : 25.2244

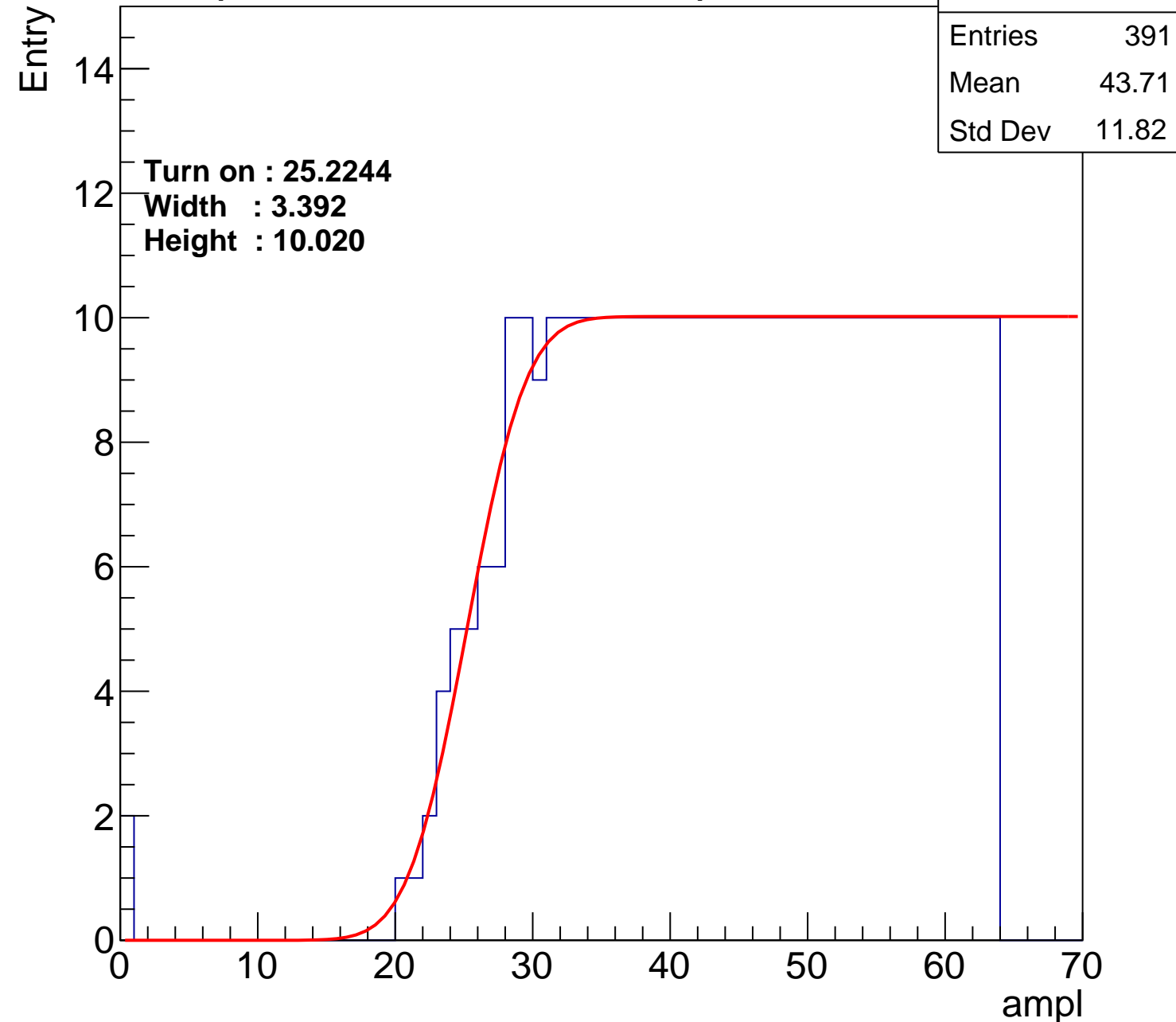
Width : 3.392

Height : 10.020

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch7

calib_packv5_042523_0143.root, FC#0, port D2

Entries	370
Mean	44.85
Std Dev	11.03

Turn on : 27.3759

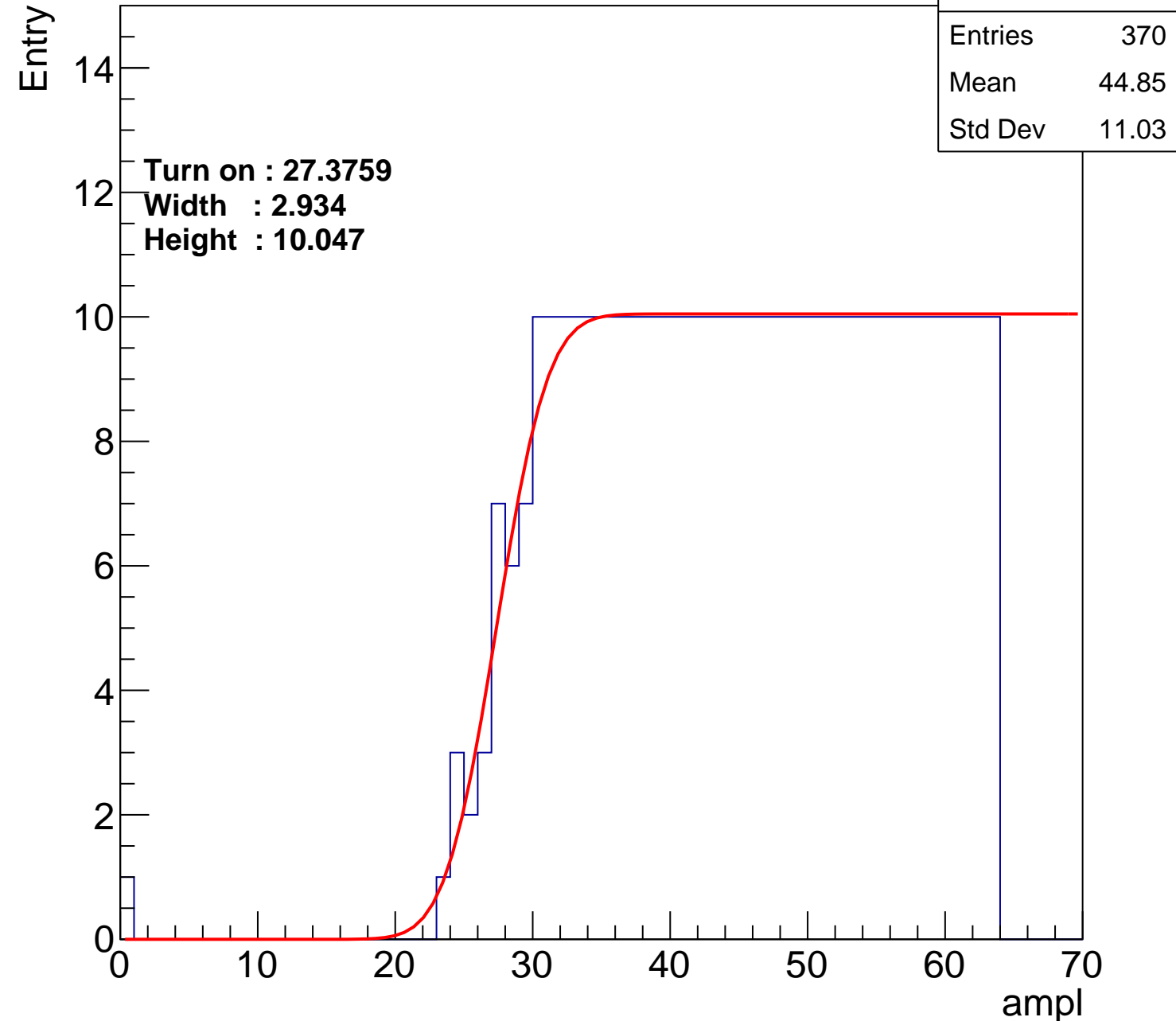
Width : 2.934

Height : 10.047

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch8

calib_packv5_042523_0143.root, FC#0, port D2

Entries	371
Mean	44.81
Std Dev	11.03

Turn on : 27.2841

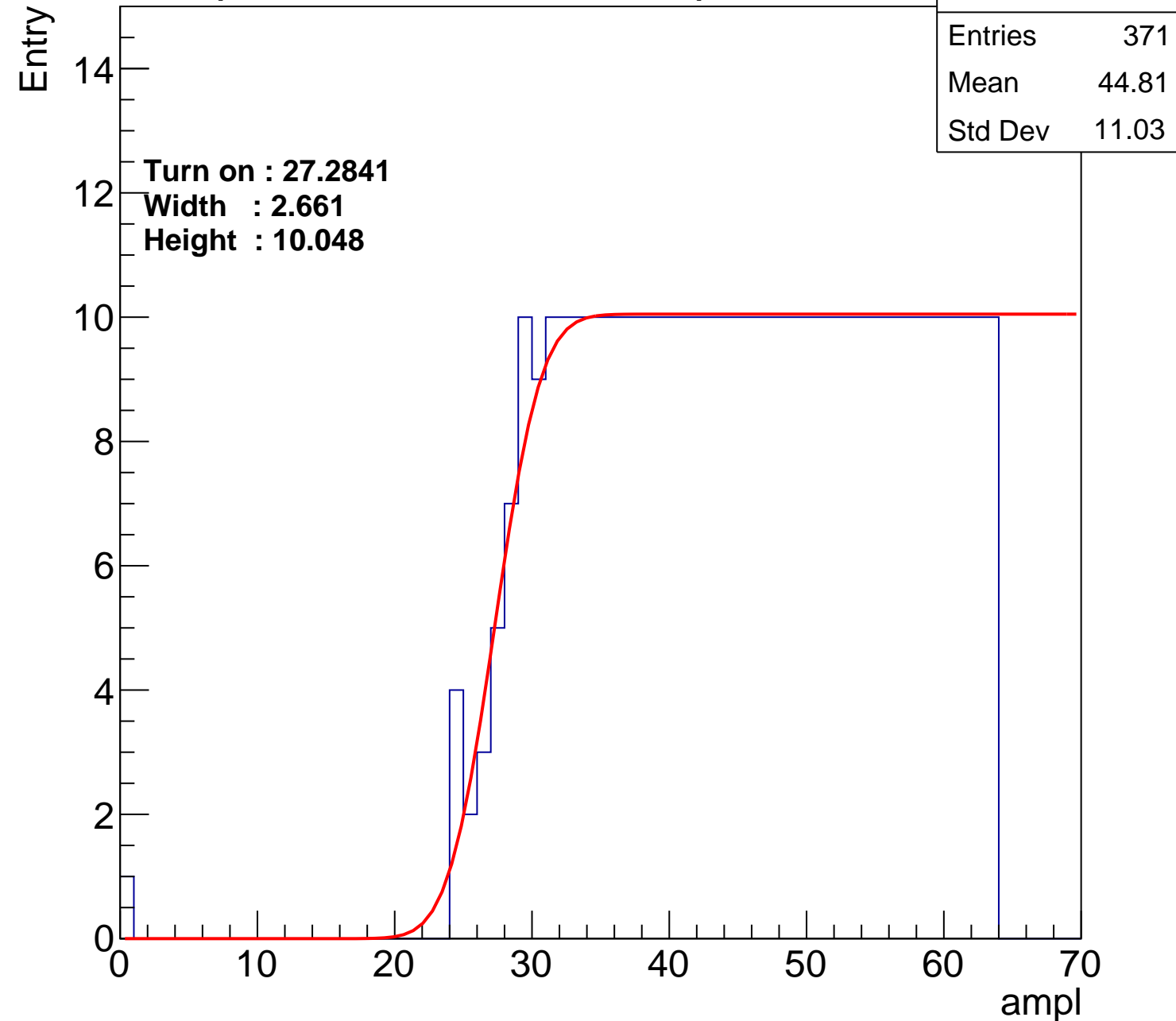
Width : 2.661

Height : 10.048

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch9

calib_packv5_042523_0143.root, FC#0, port D2

Entries	374
Mean	44.5
Std Dev	11.53

Turn on : 27.0691

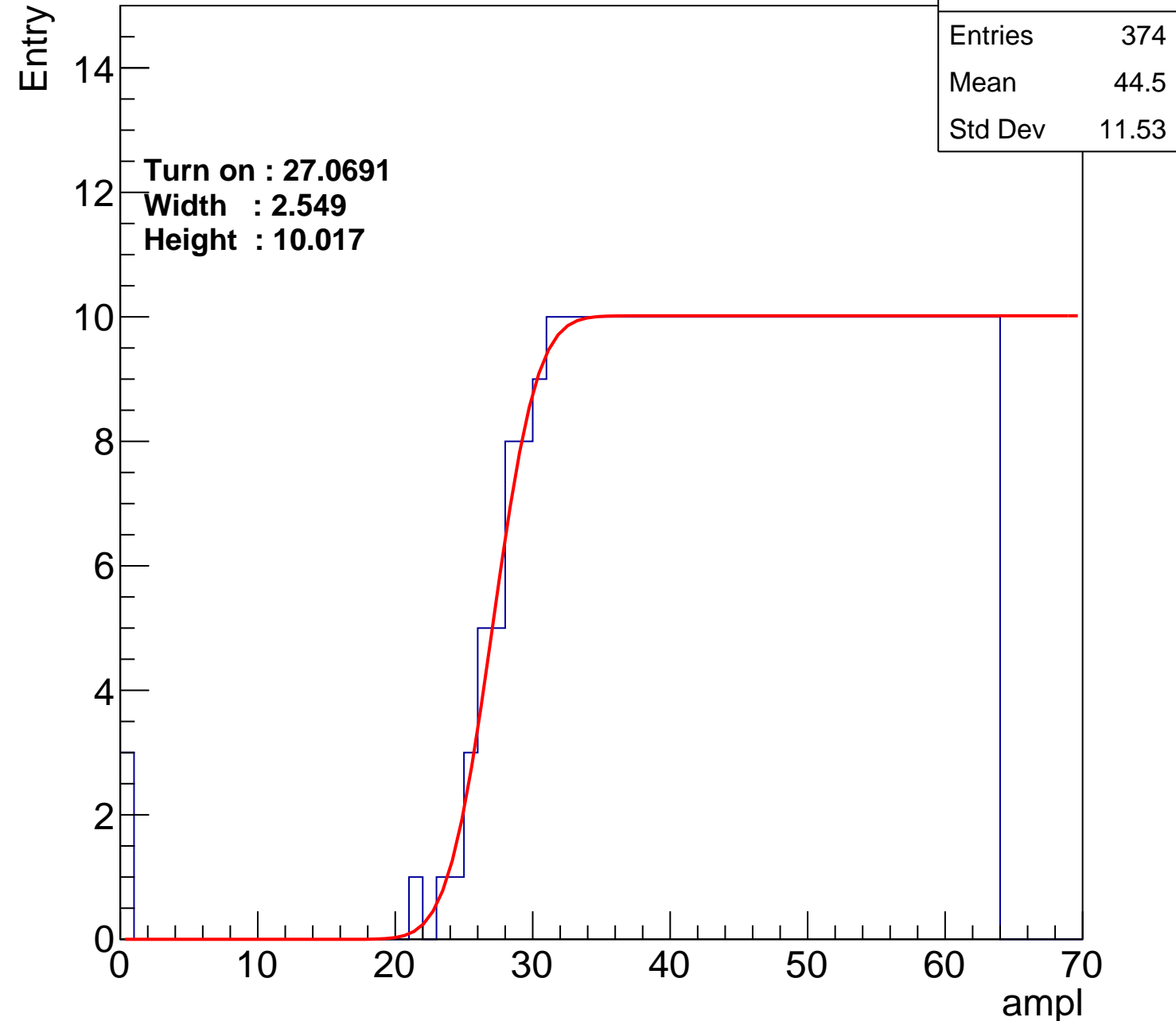
Width : 2.549

Height : 10.017

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch10

calib_packv5_042523_0143.root, FC#0, port D2

Entries	350
Mean	45.74
Std Dev	10.65

Turn on : 29.5622

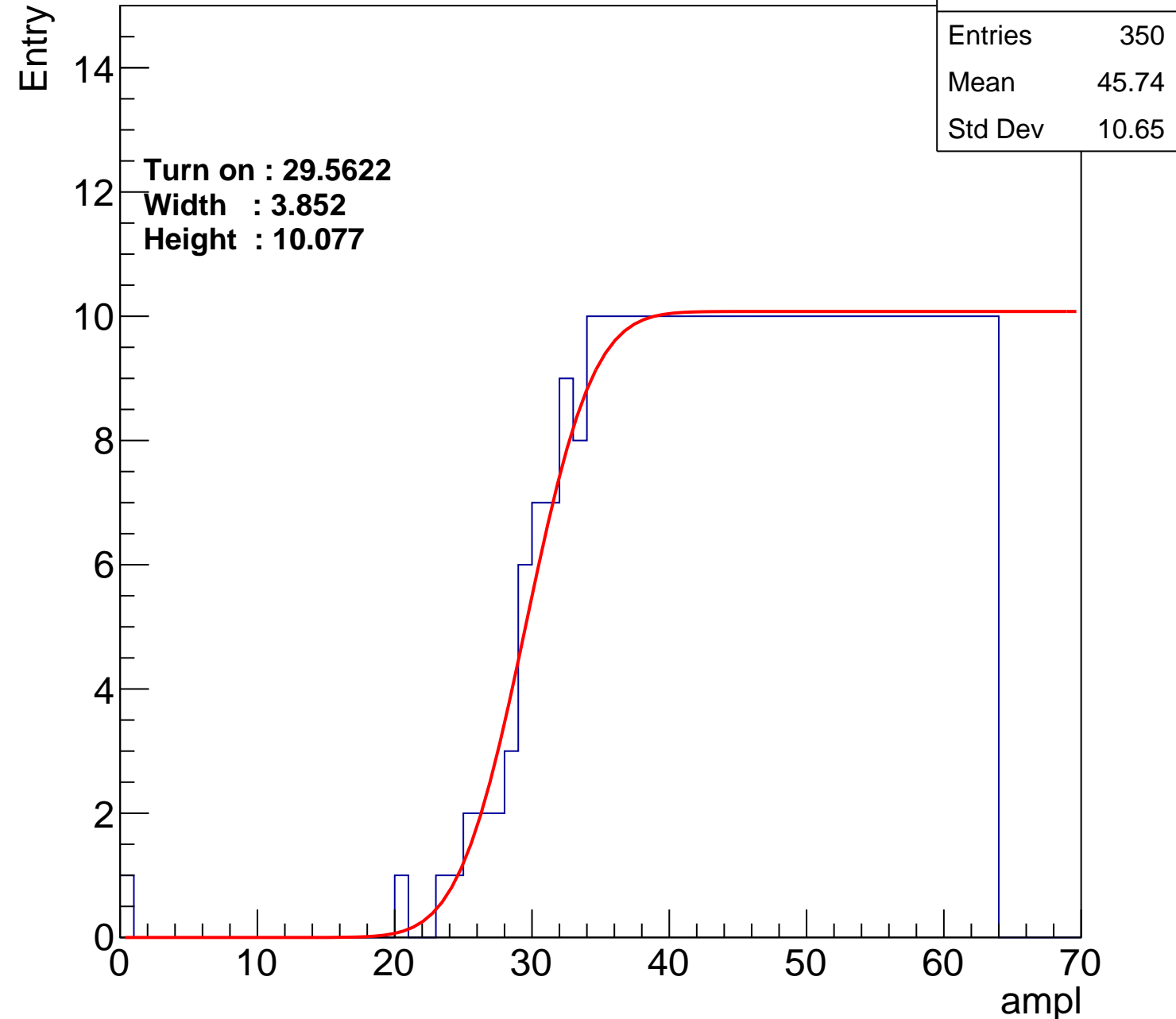
Width : 3.852

Height : 10.077

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch11

calib_packv5_042523_0143.root, FC#0, port D2

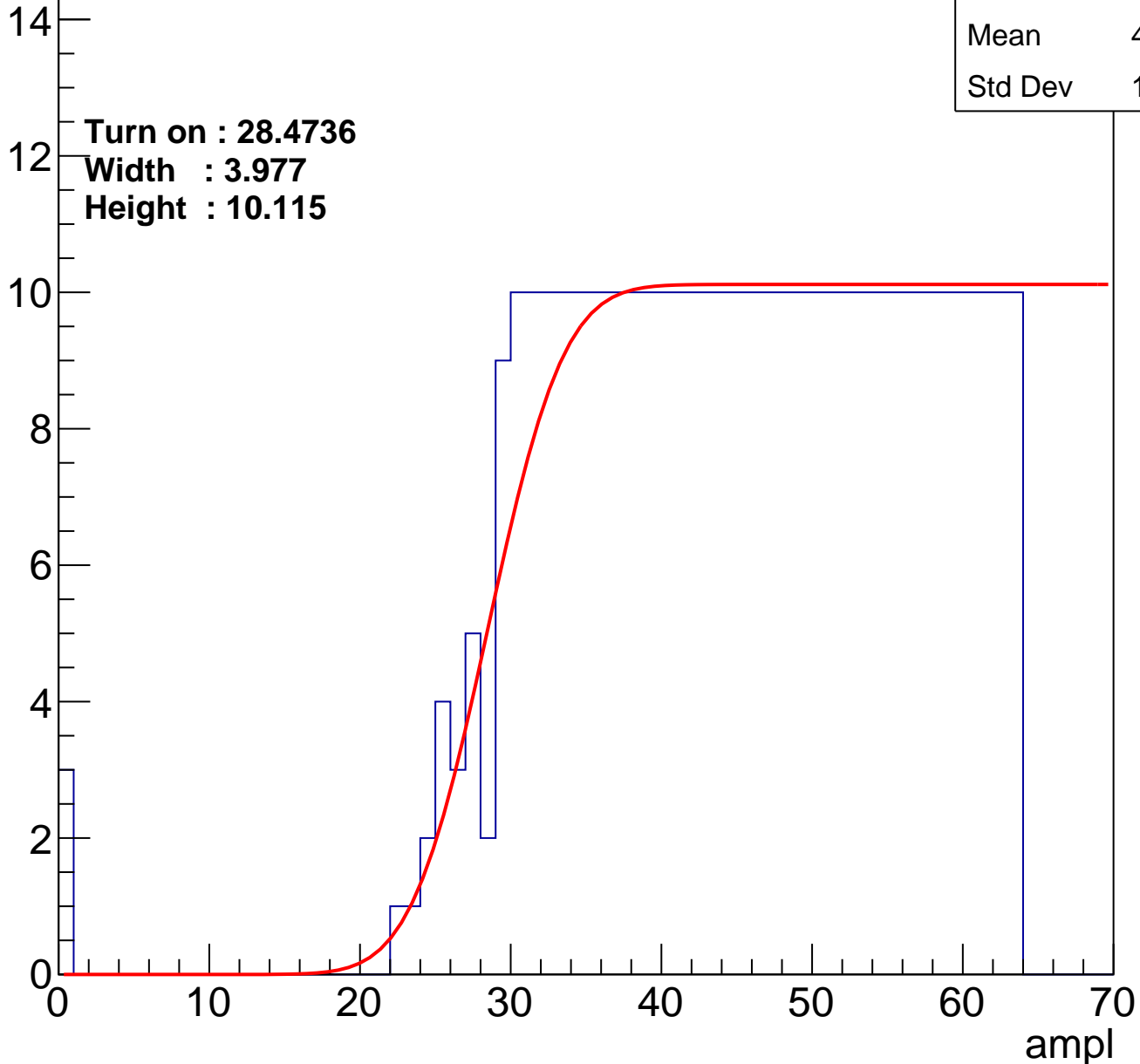
Entries	370
Mean	44.68
Std Dev	11.46

Turn on : 28.4736

Width : 3.977

Height : 10.115

Entry



B1L101S, U19-ch12

calib_packv5_042523_0143.root, FC#0, port D2

Entries	372
Mean	44.68
Std Dev	11.28

Turn on : 27.5585

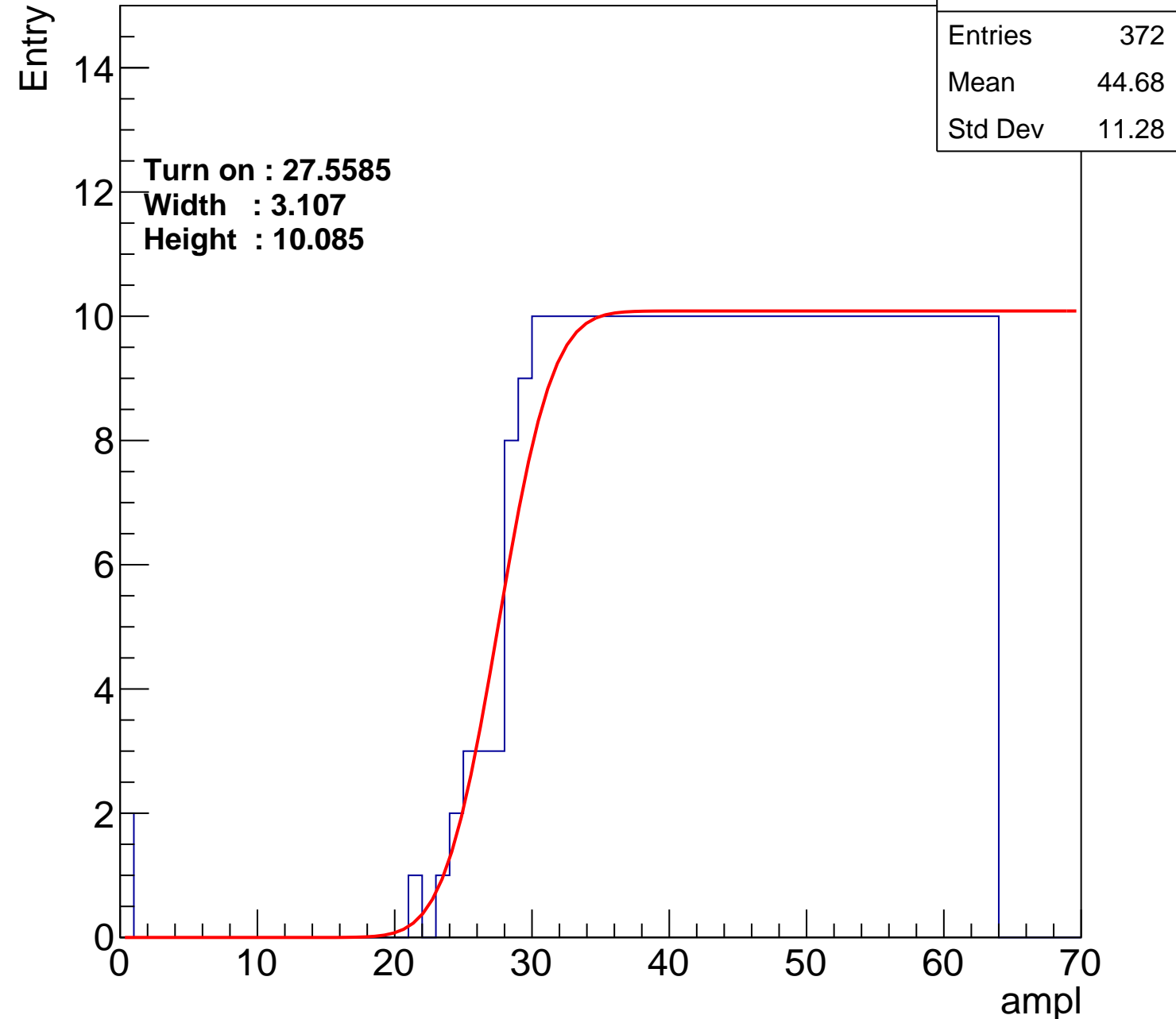
Width : 3.107

Height : 10.085

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch13

calib_packv5_042523_0143.root, FC#0, port D2

Entries	362
Mean	45.07
Std Dev	11.26

Turn on : 28.1335

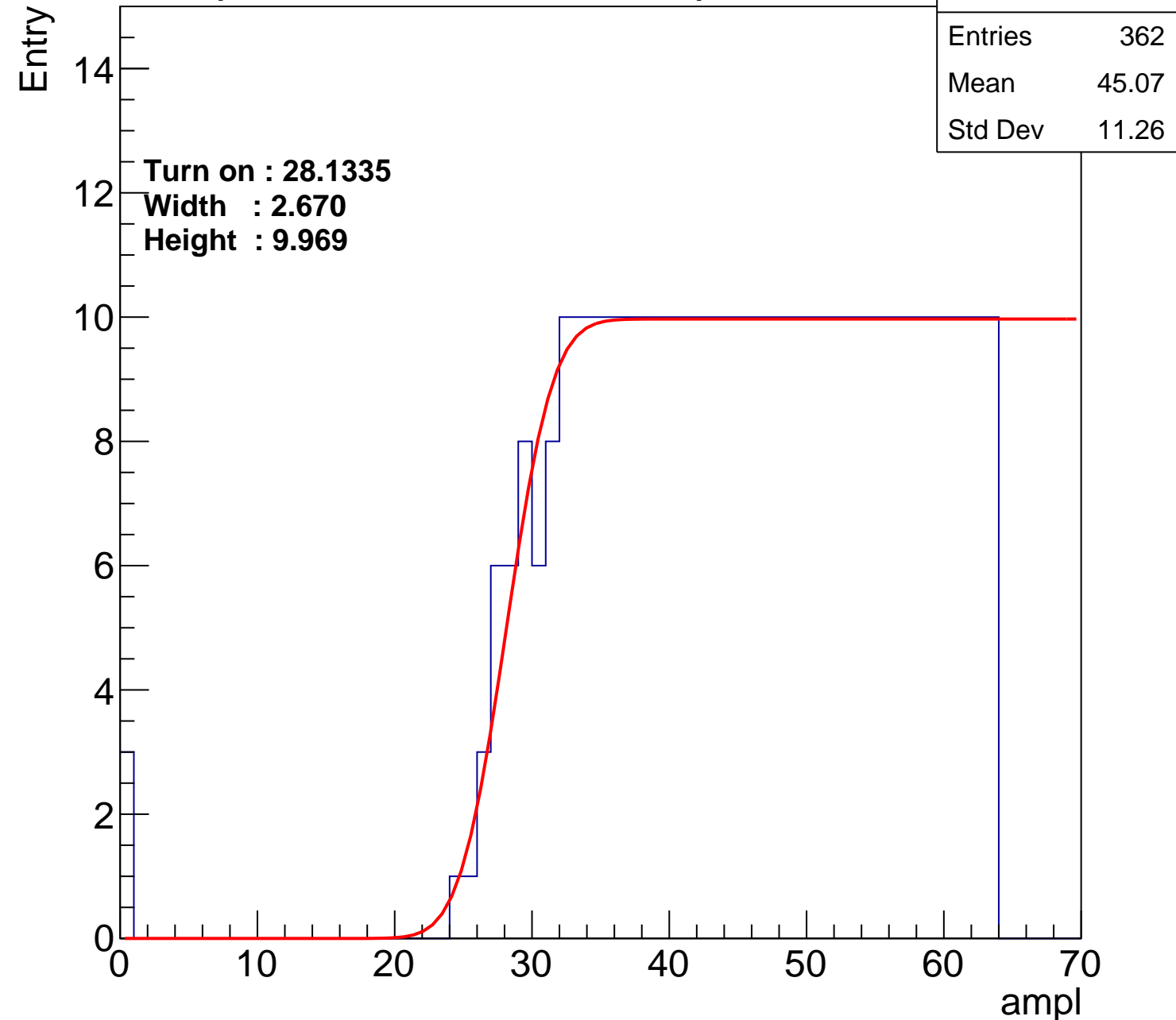
Width : 2.670

Height : 9.969

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch14

calib_packv5_042523_0143.root, FC#0, port D2

Entries	378
Mean	44.39
Std Dev	11.42

Turn on : 26.6380

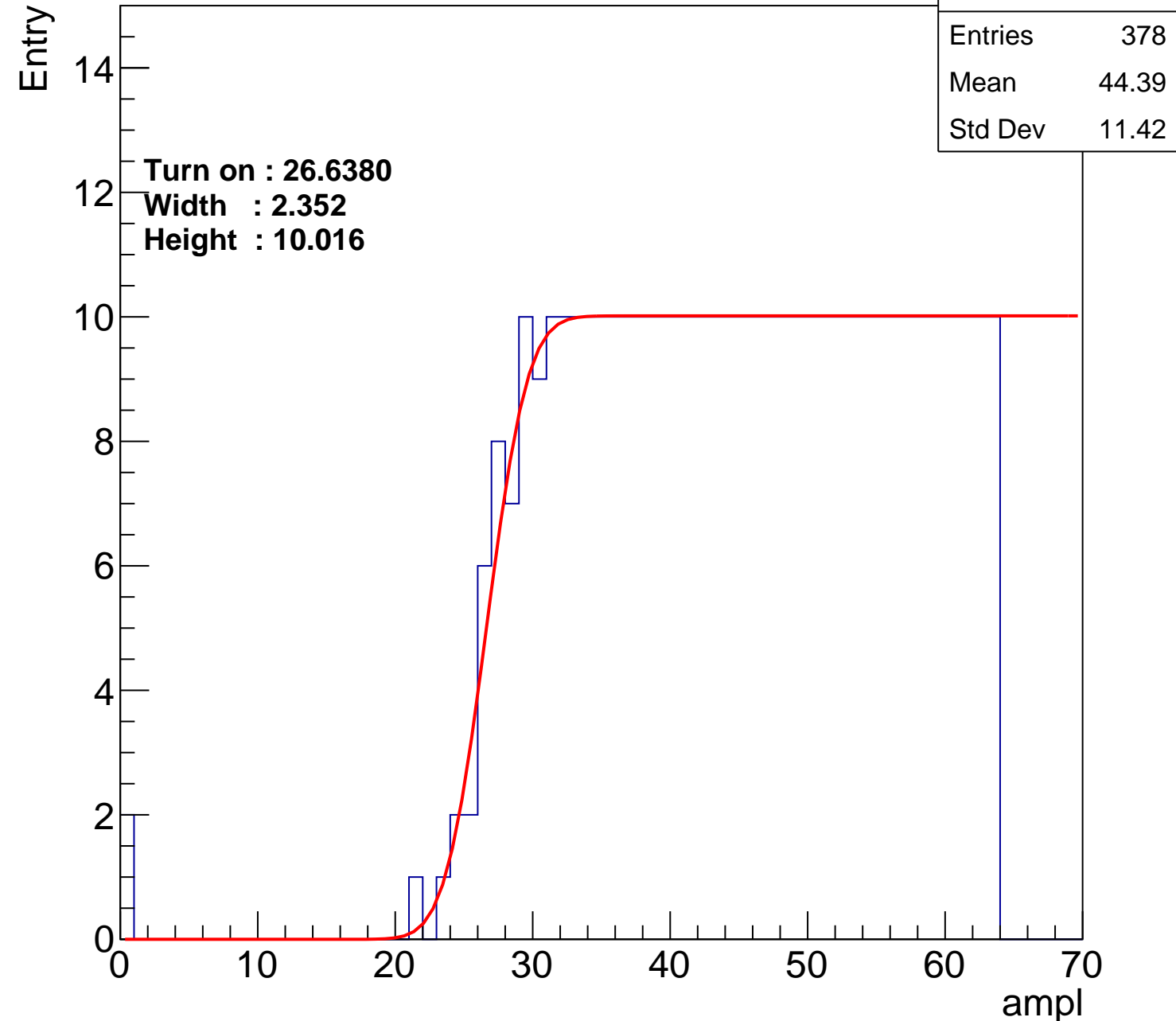
Width : 2.352

Height : 10.016

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch15

calib_packv5_042523_0143.root, FC#0, port D2

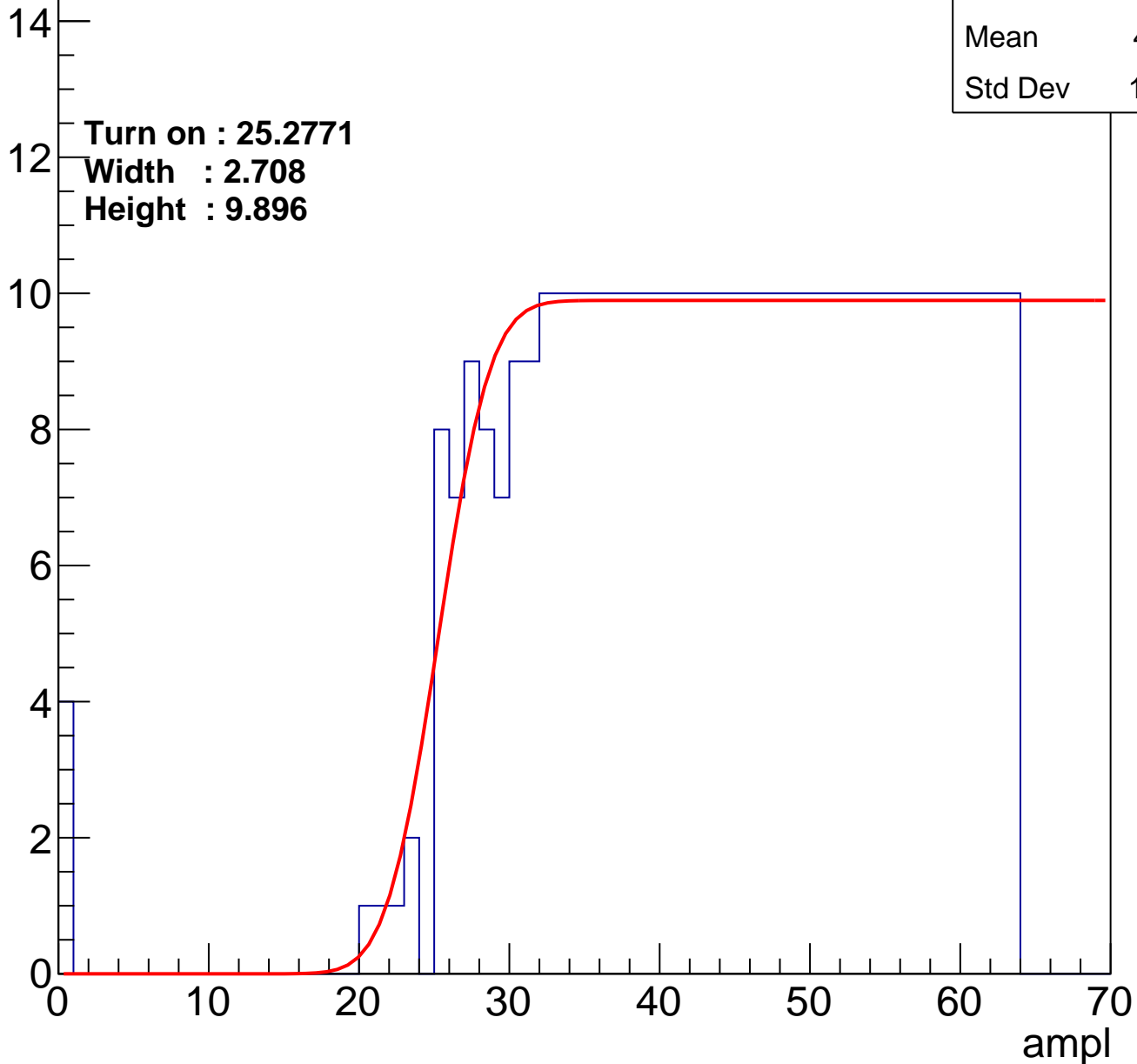
Entries	386
Mean	43.81
Std Dev	12.05

Turn on : 25.2771

Width : 2.708

Height : 9.896

Entry



B1L101S, U19-ch16

calib_packv5_042523_0143.root, FC#0, port D2

Entries	384
Mean	44.01
Std Dev	11.71

Turn on : 26.6797

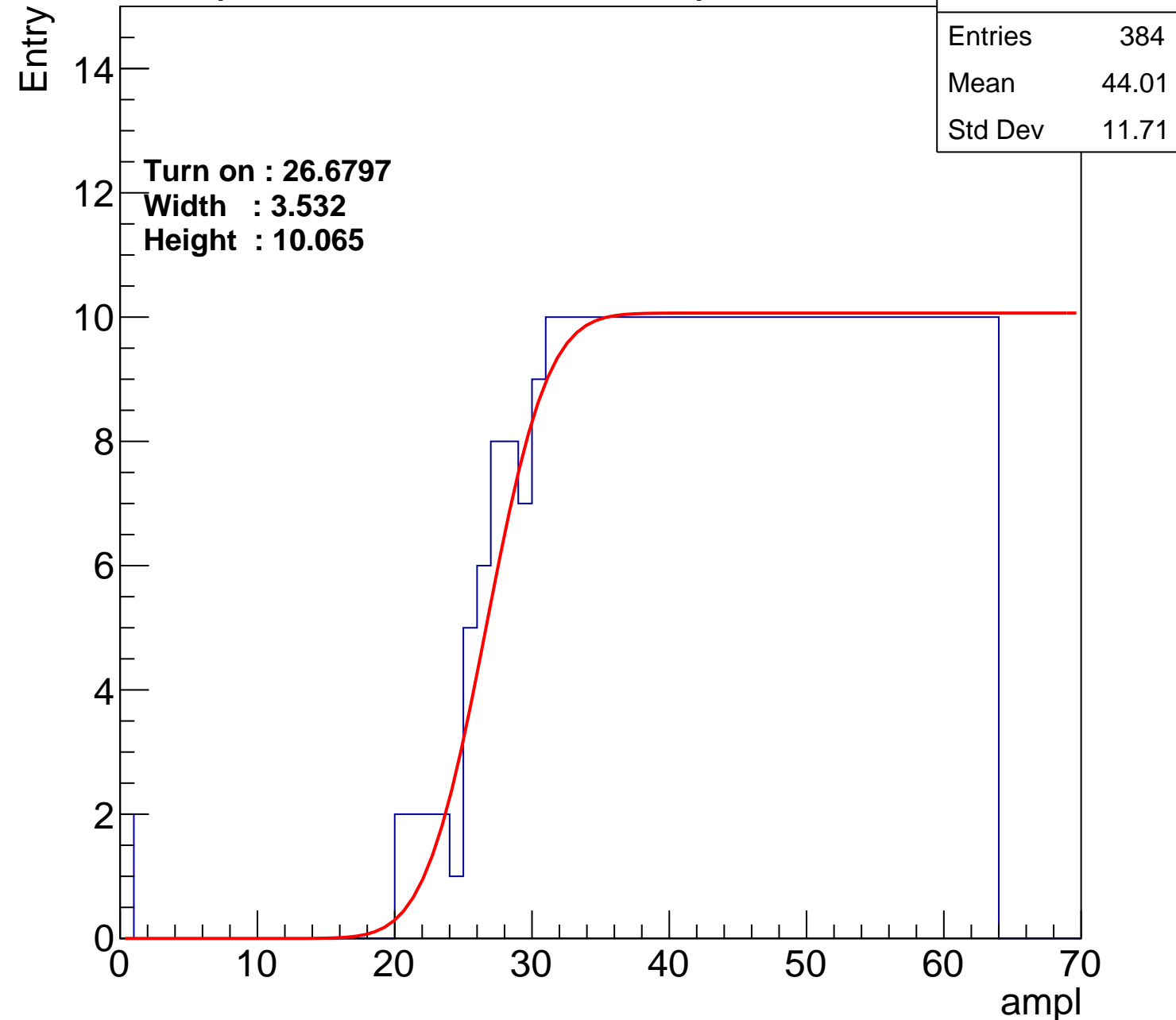
Width : 3.532

Height : 10.065

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch17

calib_packv5_042523_0143.root, FC#0, port D2

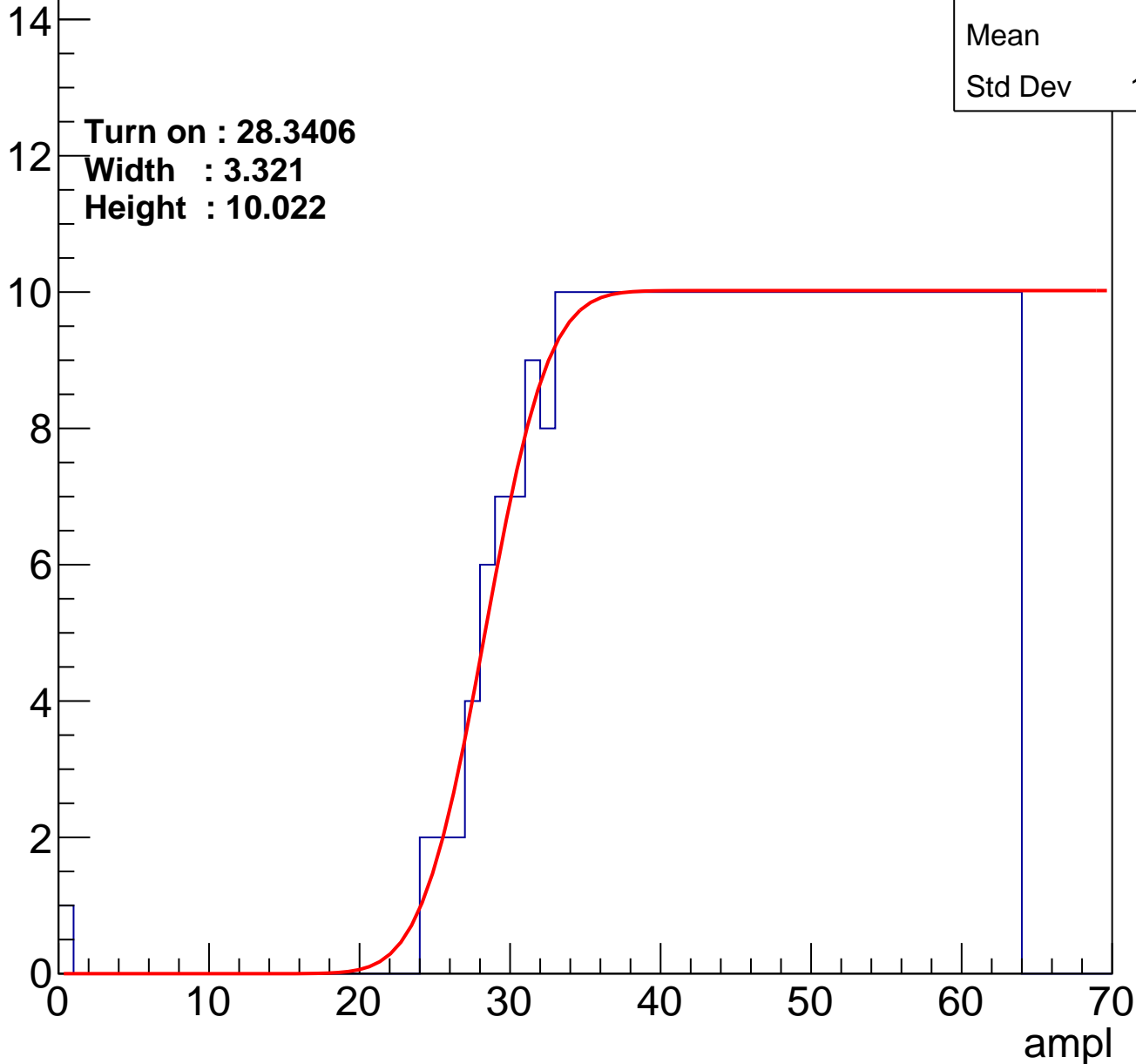
Entries	358
Mean	45.4
Std Dev	10.76

Turn on : 28.3406

Width : 3.321

Height : 10.022

Entry



B1L101S, U19-ch18

calib_packv5_042523_0143.root, FC#0, port D2

Entries	392
Mean	43.62
Std Dev	11.97

Turn on : 25.2982

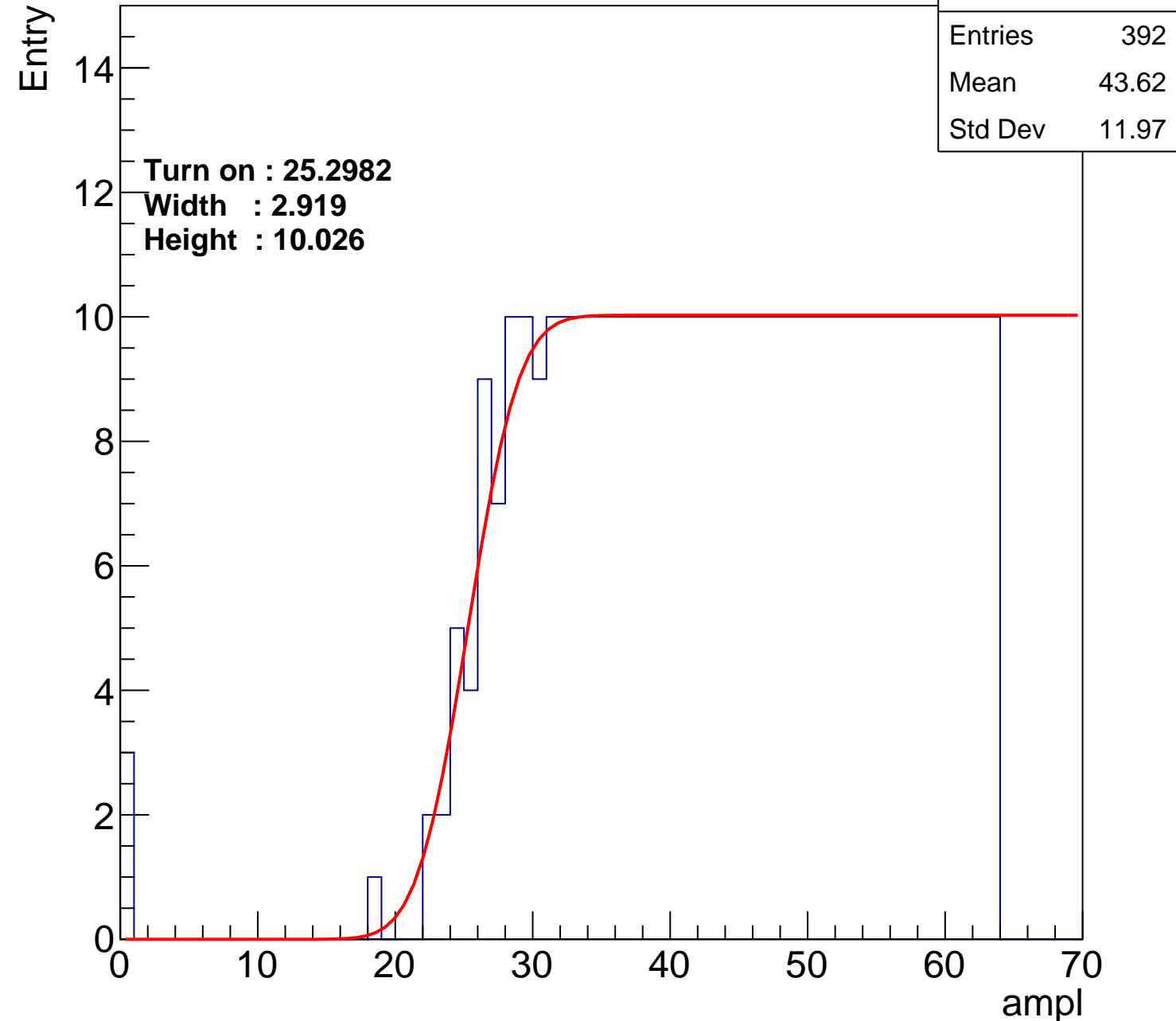
Width : 2.919

Height : 10.026

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch19

calib_packv5_042523_0143.root, FC#0, port D2

Entries	361
Mean	45.19
Std Dev	11.04

Turn on : 28.4208

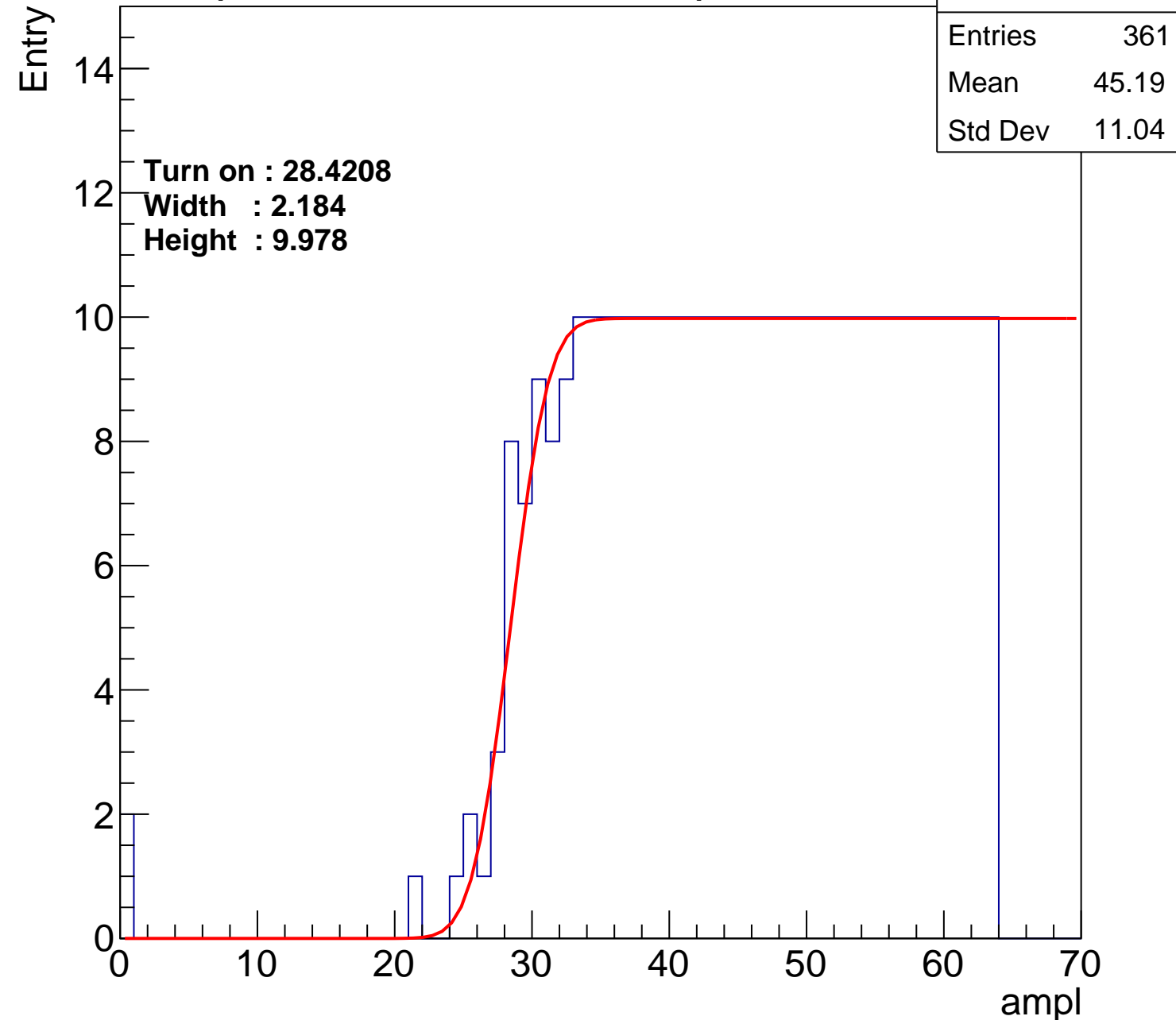
Width : 2.184

Height : 9.978

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch20

calib_packv5_042523_0143.root, FC#0, port D2

Entries	390
Mean	43.71
Std Dev	11.94

Turn on : 25.4930

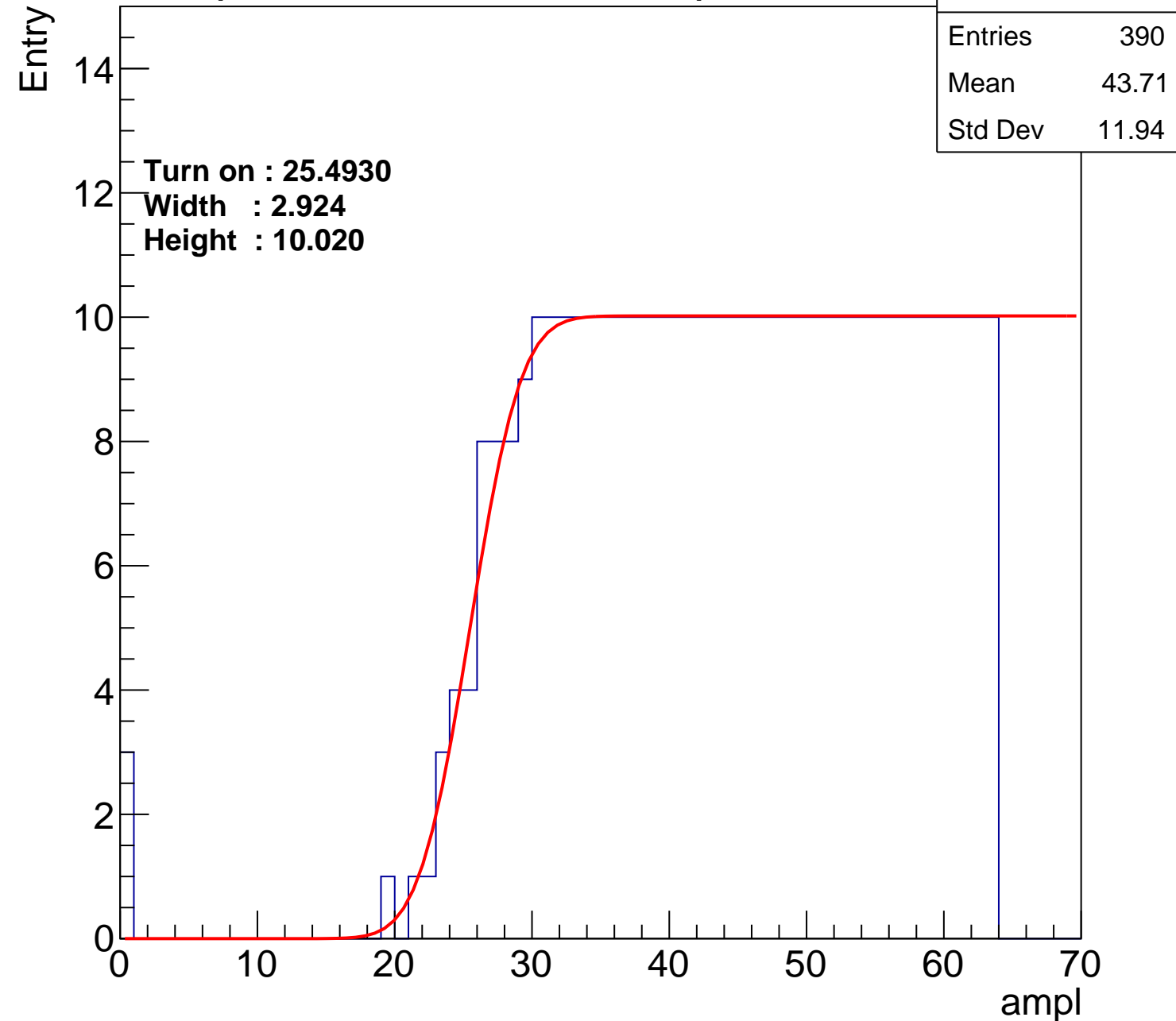
Width : 2.924

Height : 10.020

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch21

calib_packv5_042523_0143.root, FC#0, port D2

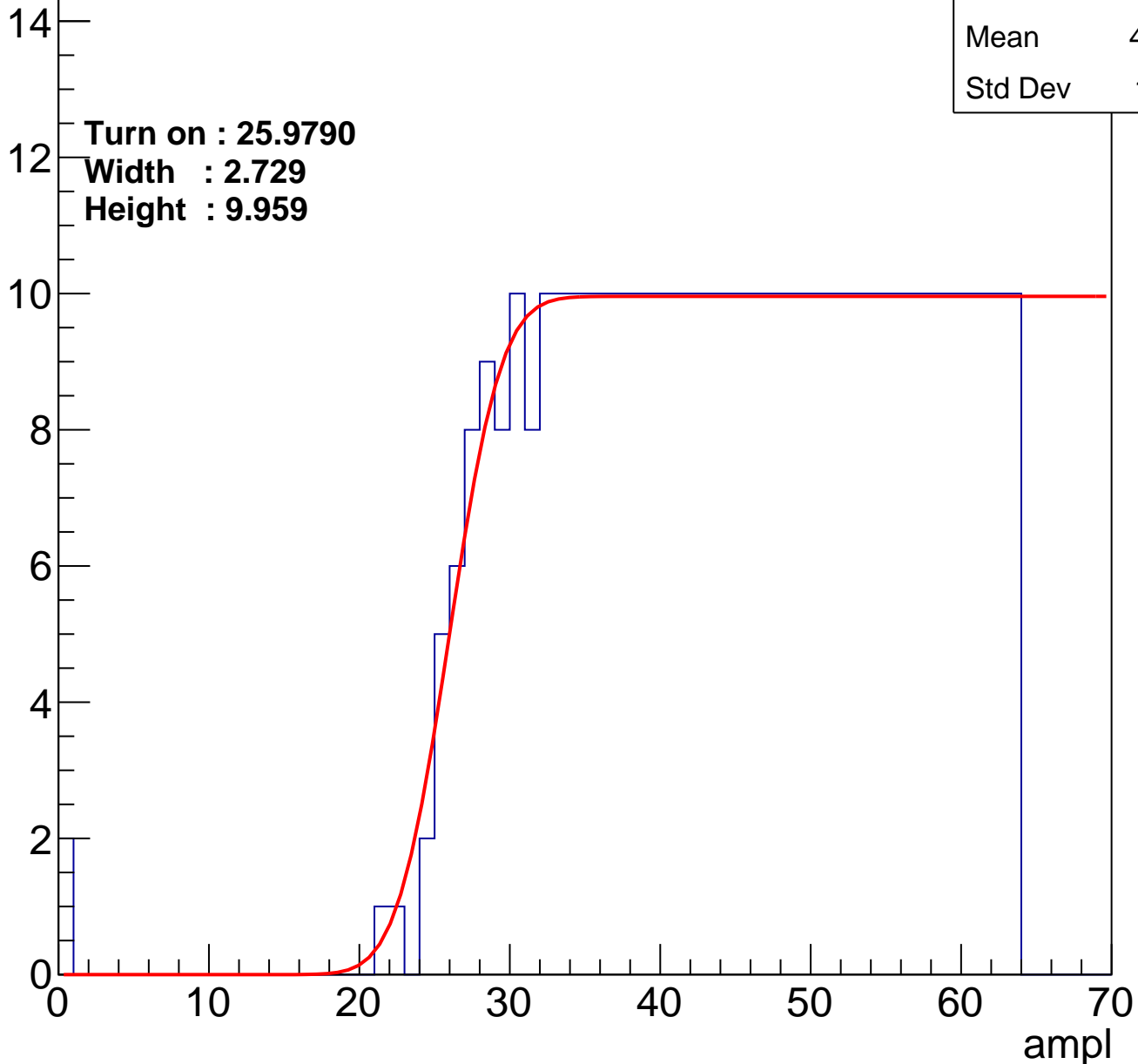
Entries	380
Mean	44.26
Std Dev	11.51

Turn on : 25.9790

Width : 2.729

Height : 9.959

Entry



B1L101S, U19-ch22

calib_packv5_042523_0143.root, FC#0, port D2

Entries	376
Mean	44.45
Std Dev	11.42

Turn on : 26.7738

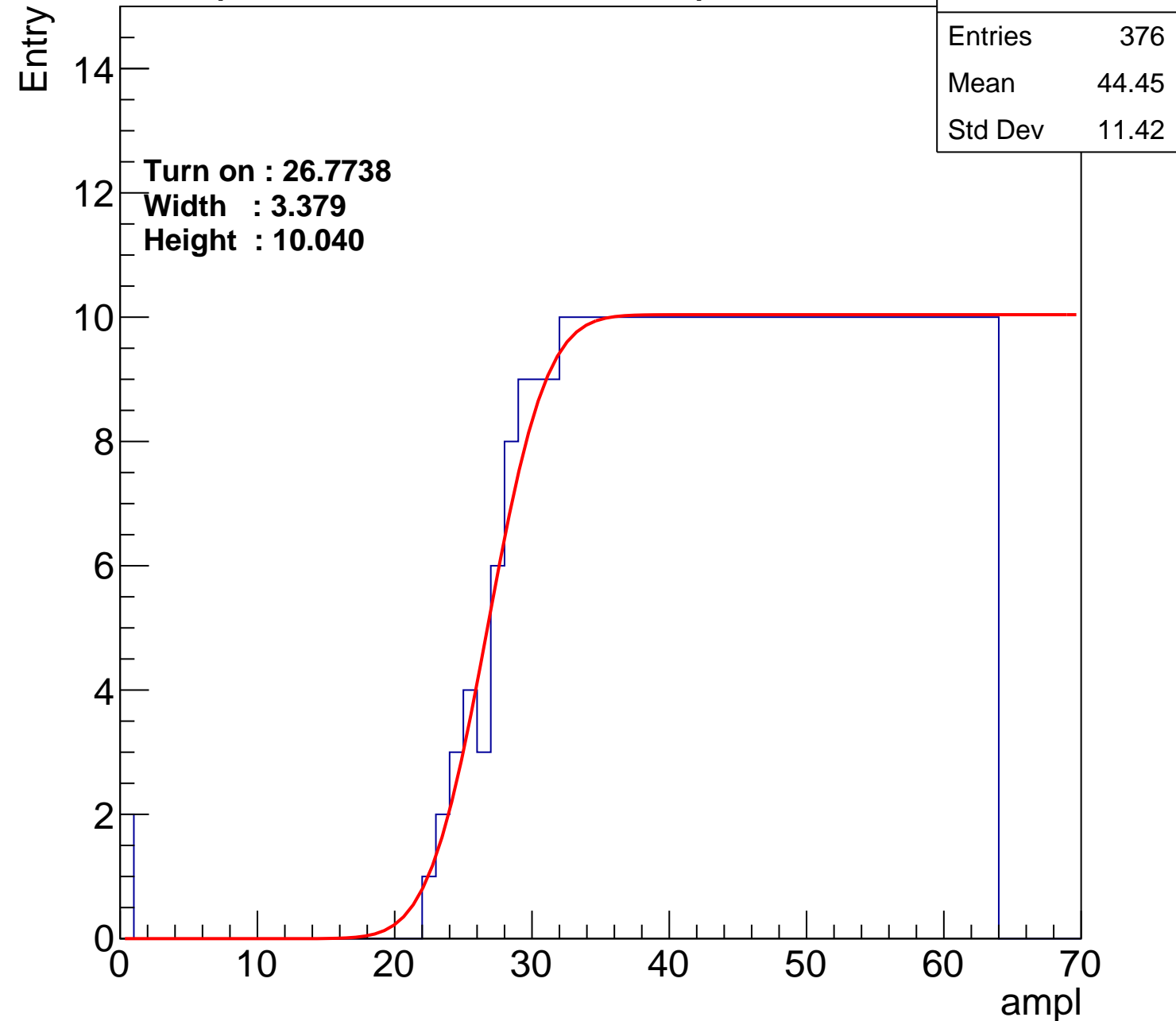
Width : 3.379

Height : 10.040

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch23

calib_packv5_042523_0143.root, FC#0, port D2

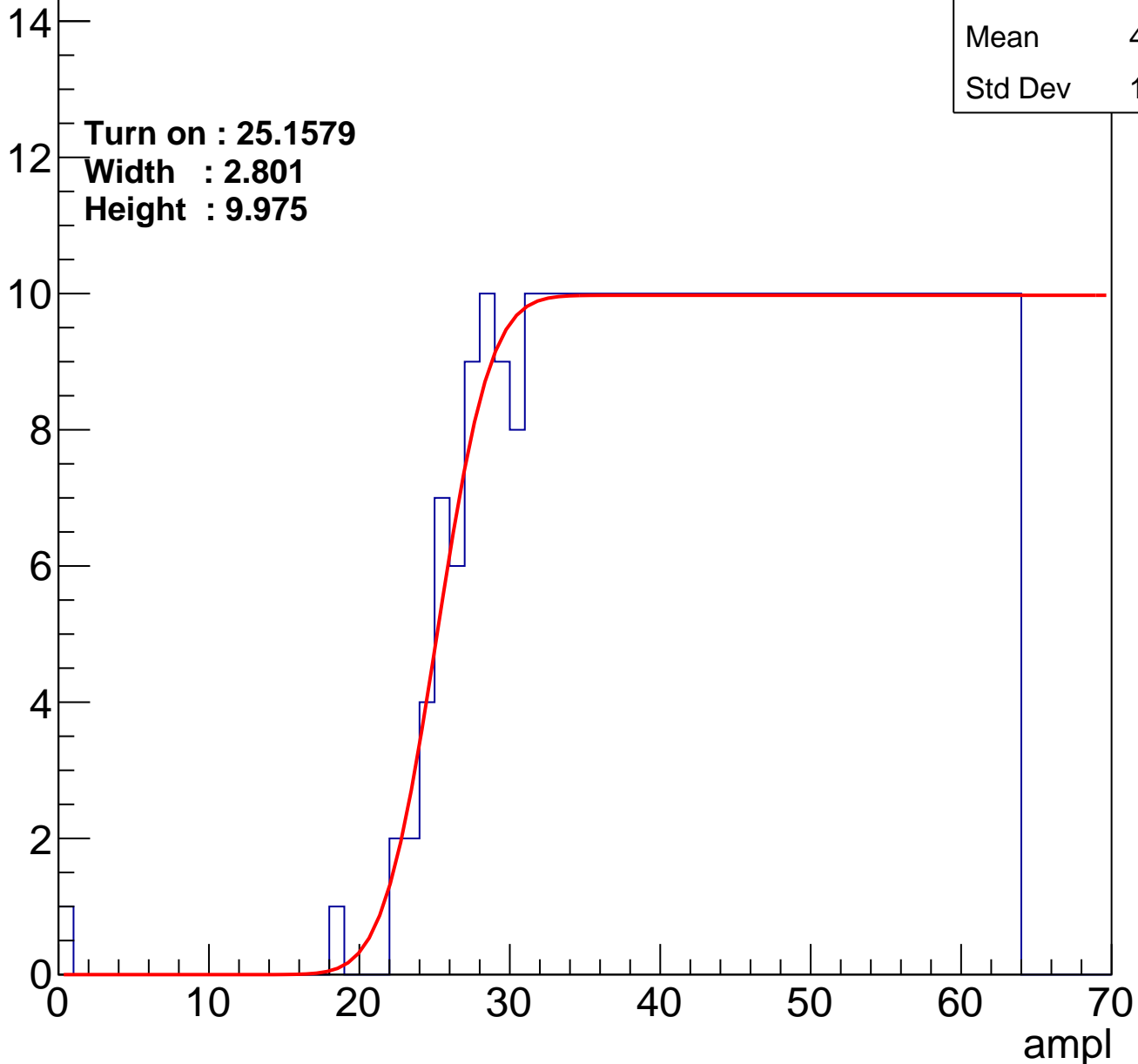
Entries	389
Mean	43.88
Std Dev	11.58

Turn on : 25.1579

Width : 2.801

Height : 9.975

Entry



B1L101S, U19-ch24

calib_packv5_042523_0143.root, FC#0, port D2

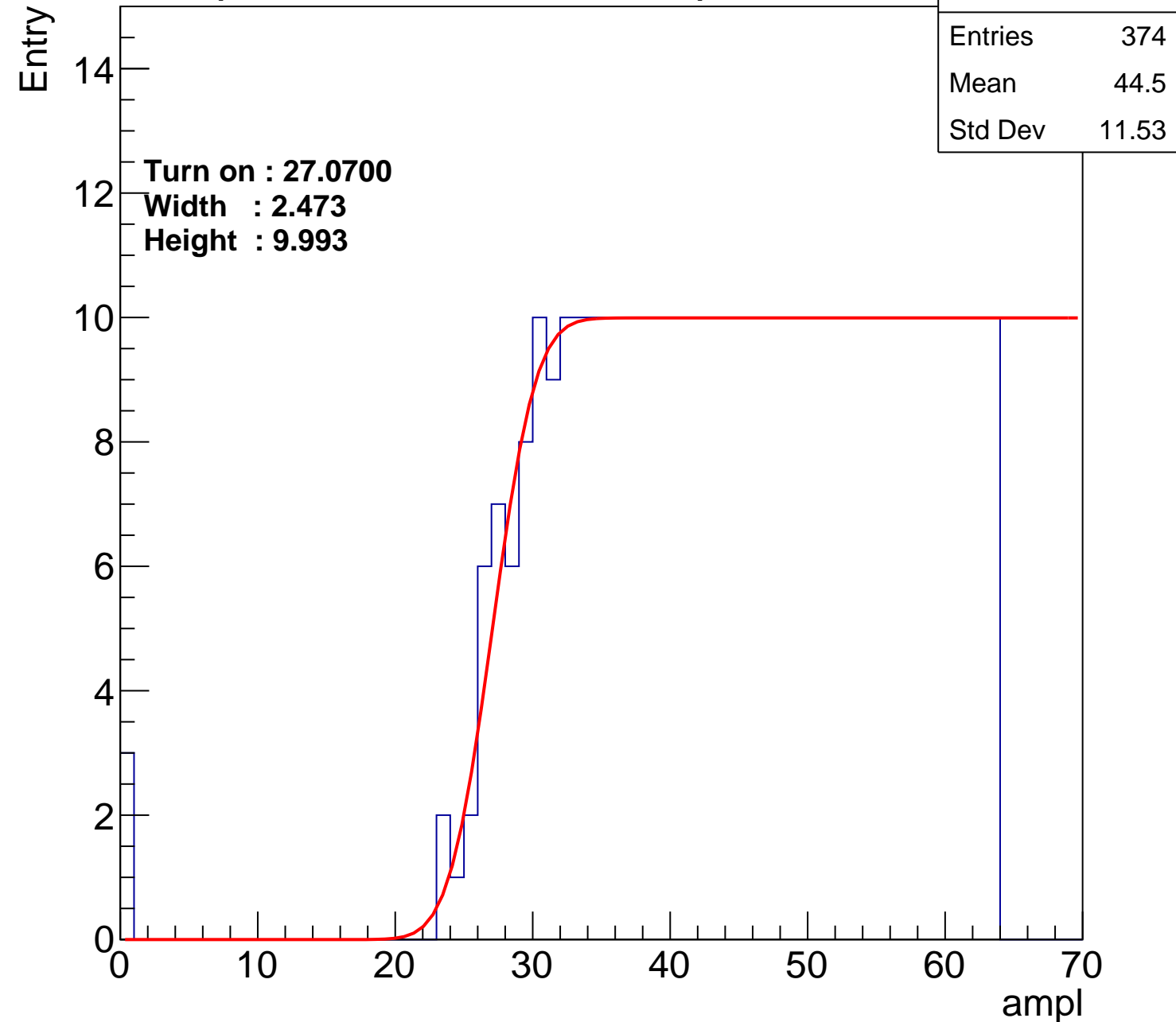
Entry

14
12
10
8
6
4
2
0

Turn on : 27.0700
Width : 2.473
Height : 9.993

Entries	374
Mean	44.5
Std Dev	11.53

ampl



B1L101S, U19-ch25

calib_packv5_042523_0143.root, FC#0, port D2

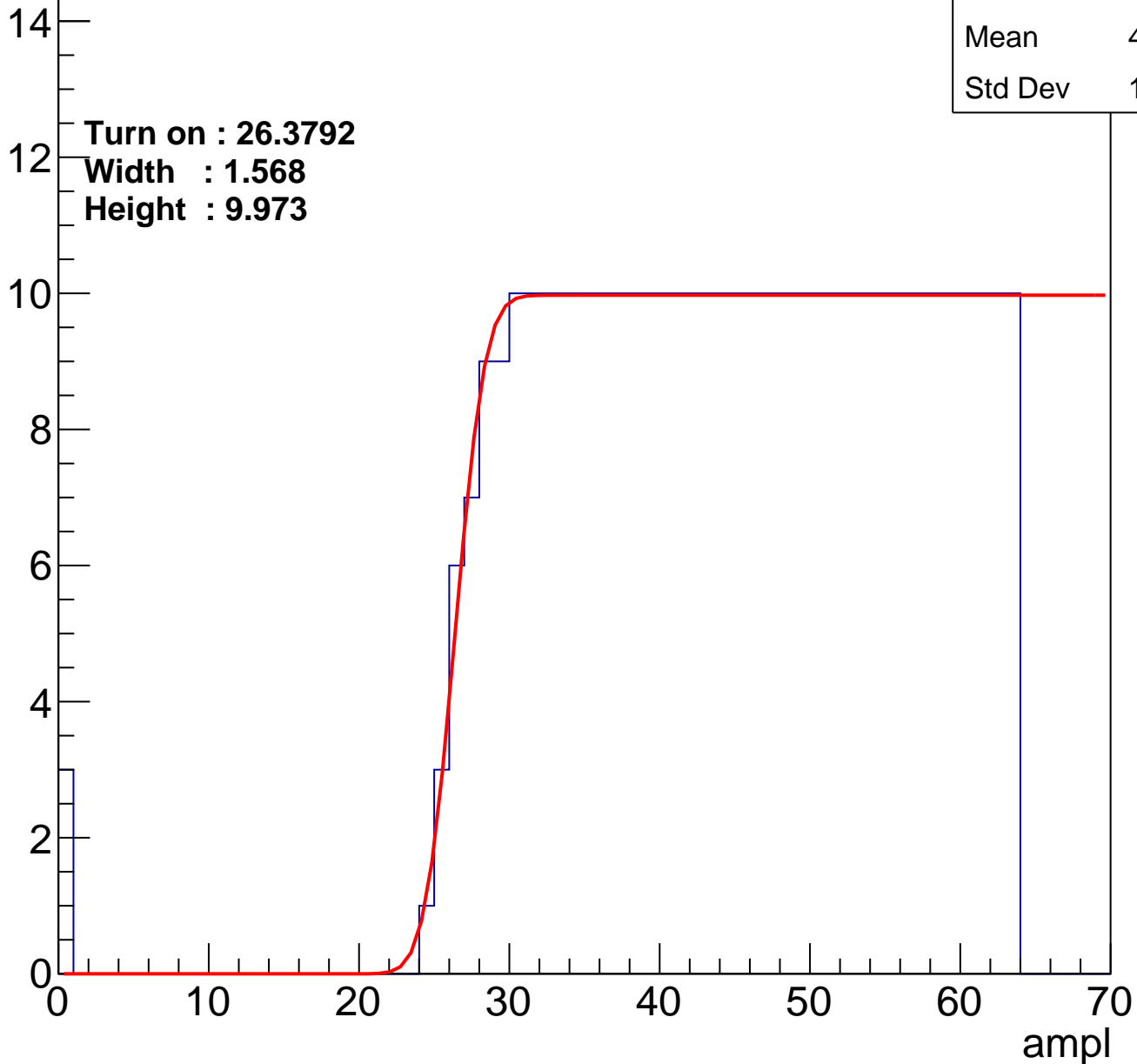
Entries	378
Mean	44.36
Std Dev	11.55

Turn on : 26.3792

Width : 1.568

Height : 9.973

Entry



B1L101S, U19-ch26

calib_packv5_042523_0143.root, FC#0, port D2

Entries	380
Mean	44.26
Std Dev	11.59

Turn on : 26.3723

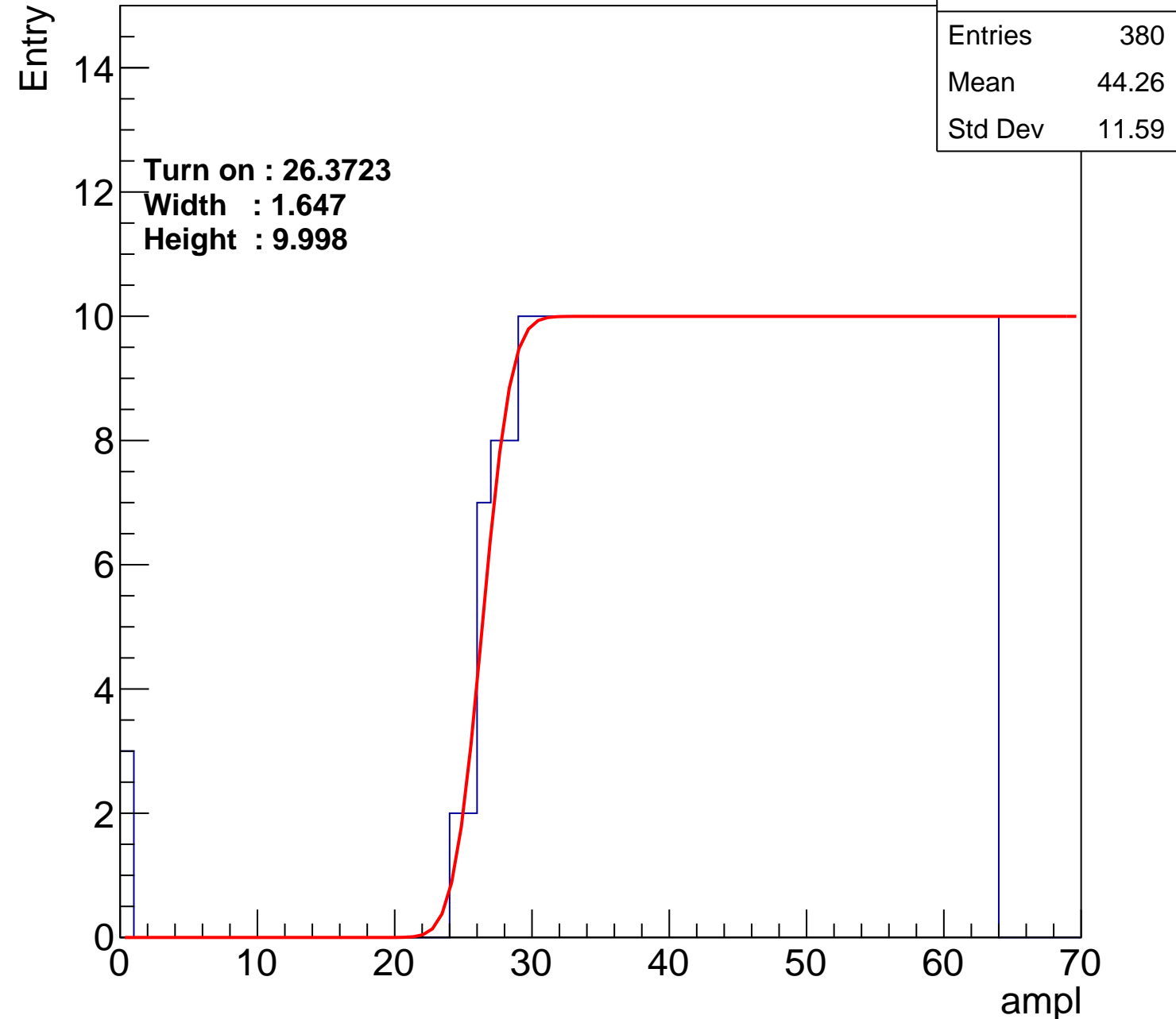
Width : 1.647

Height : 9.998

Entry

14
12
10
8
6
4
2
0

ampl



calib_packv5_042523_0143.root, FC#0, port D2

Entries	367
Mean	44.84
Std Dev	11.37

Mean	44.84
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Std Dev	11.37
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Width : 1.911

Height : 9.915



14

12

100

10

10

8

•

6

9

4

1

2

2

0

0

10

20

30

40

50

60

ampl

B1L101S, U19-ch28

calib_packv5_042523_0143.root, FC#0, port D2

Entries	361
Mean	45.15
Std Dev	11.2

Turn on : 28.1848

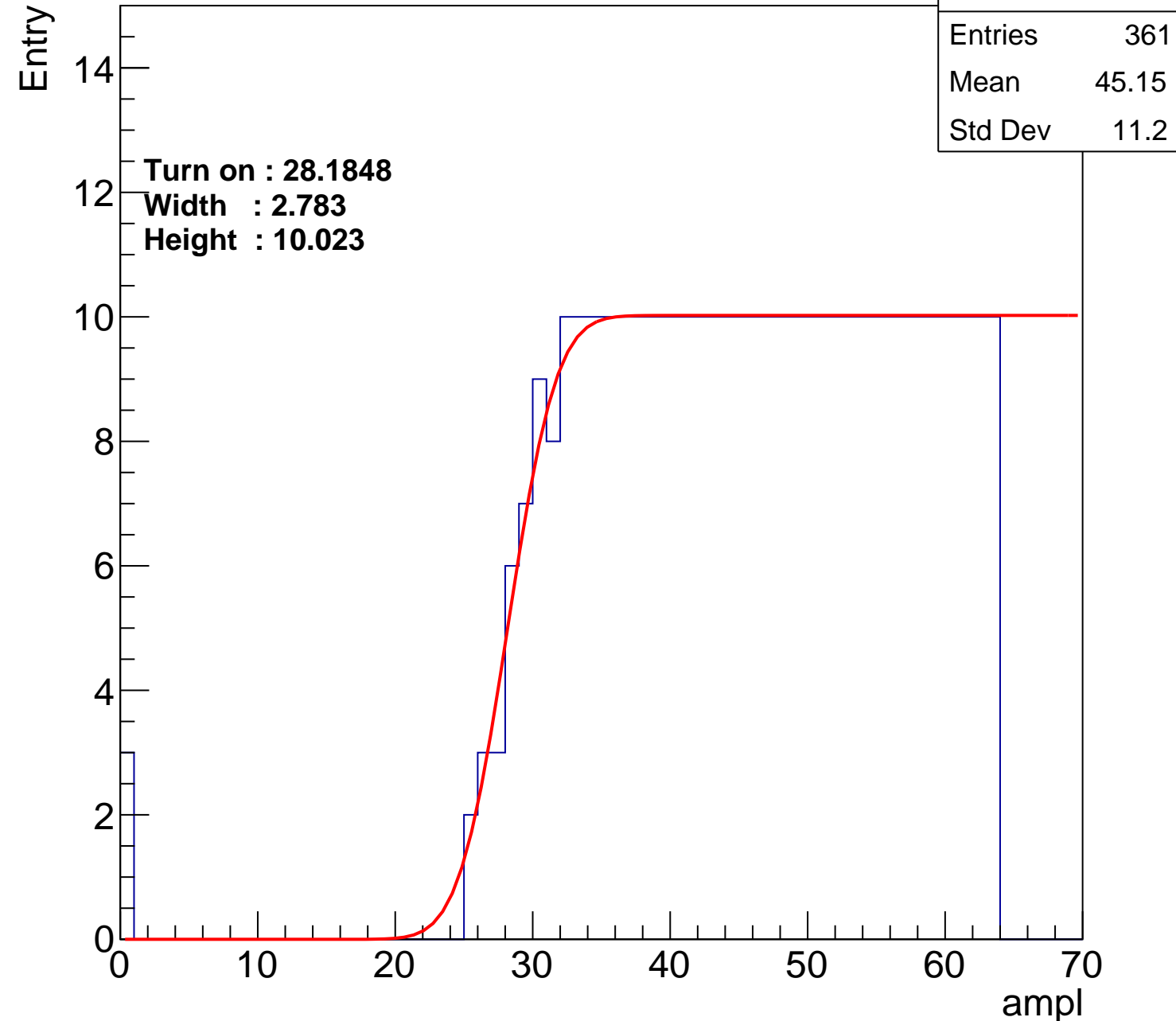
Width : 2.783

Height : 10.023

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch29

calib_packv5_042523_0143.root, FC#0, port D2

Entries	354
Mean	45.55
Std Dev	10.84

Turn on : 28.5654

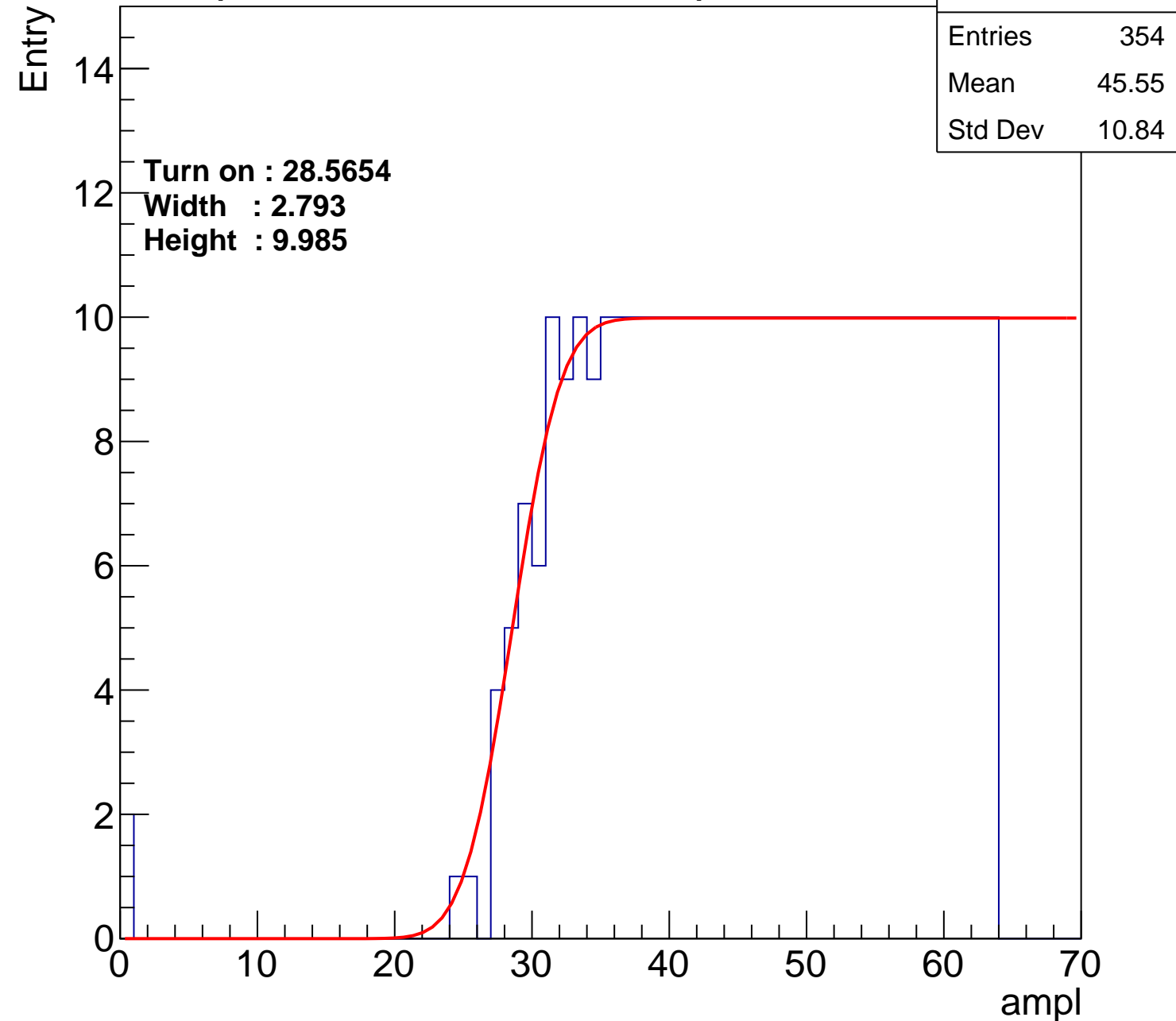
Width : 2.793

Height : 9.985

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch30

calib_packv5_042523_0143.root, FC#0, port D2

Entries	376
Mean	44.52
Std Dev	11.25

Turn on : 27.3363

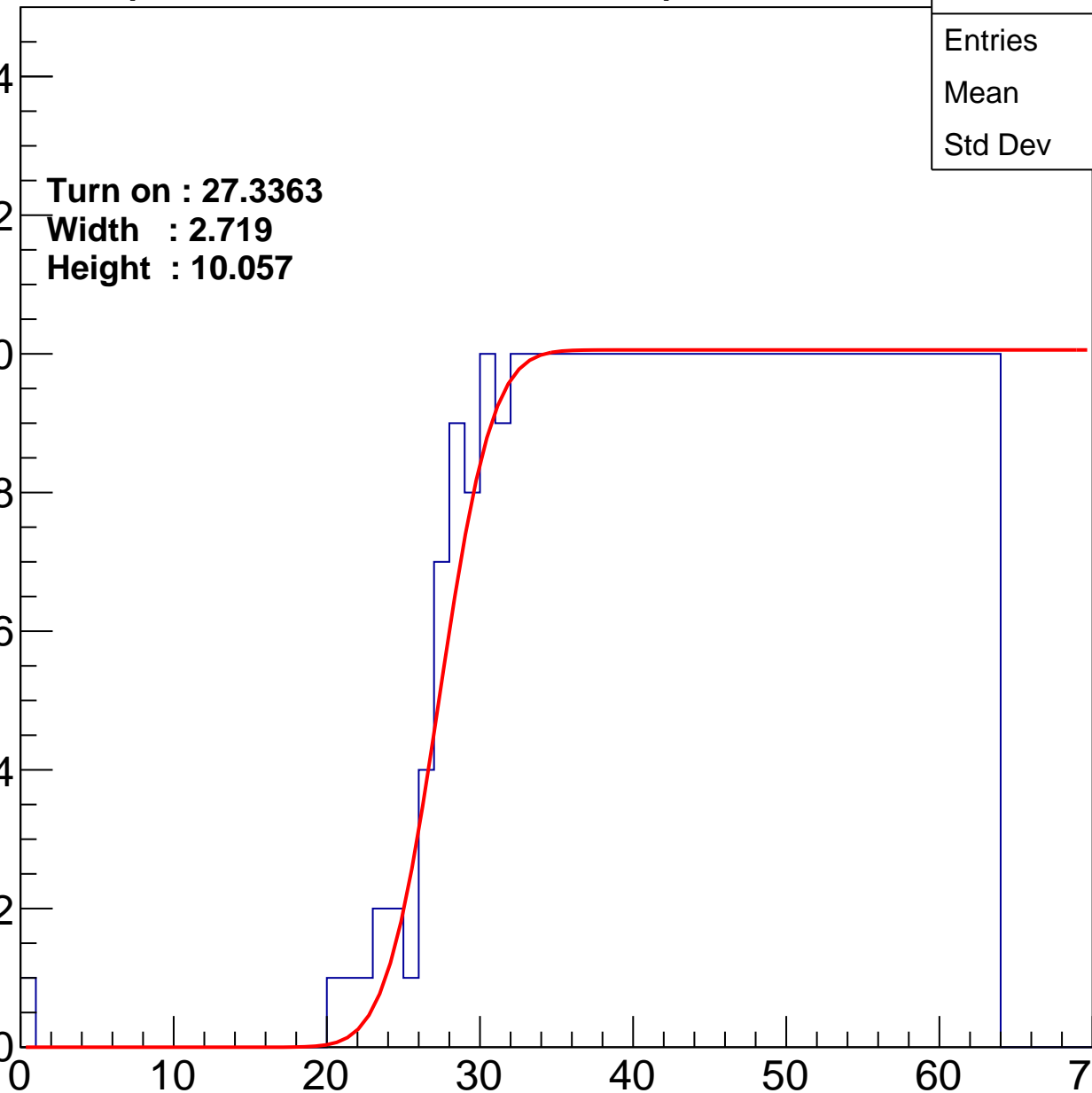
Width : 2.719

Height : 10.057

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch31

calib_packv5_042523_0143.root, FC#0, port D2

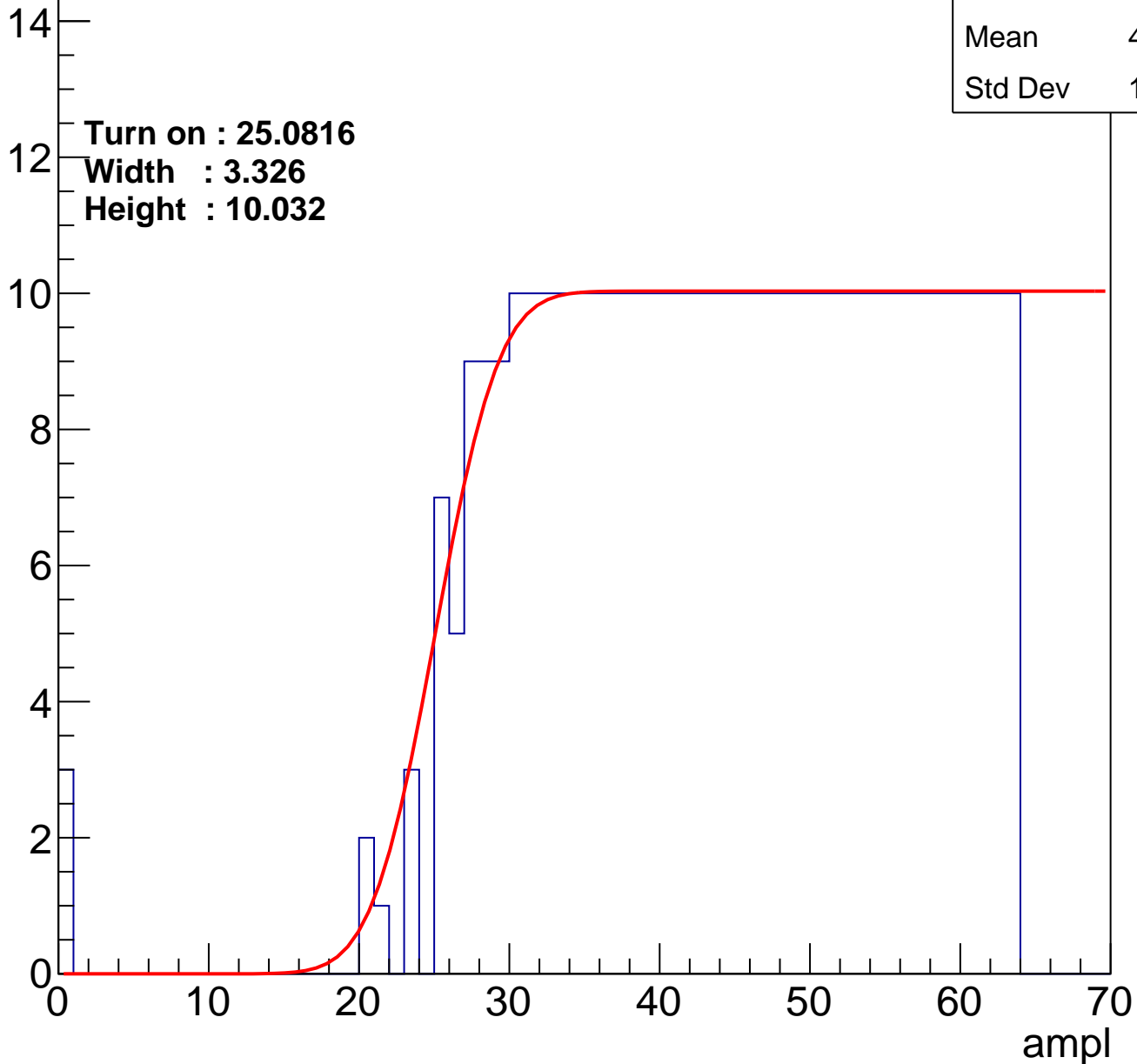
Entries	388
Mean	43.82
Std Dev	11.88

Turn on : 25.0816

Width : 3.326

Height : 10.032

Entry



B1L101S, U19-ch32

calib_packv5_042523_0143.root, FC#0, port D2

Entries	373
Mean	44.55
Std Dev	11.51

Turn on : 26.6895

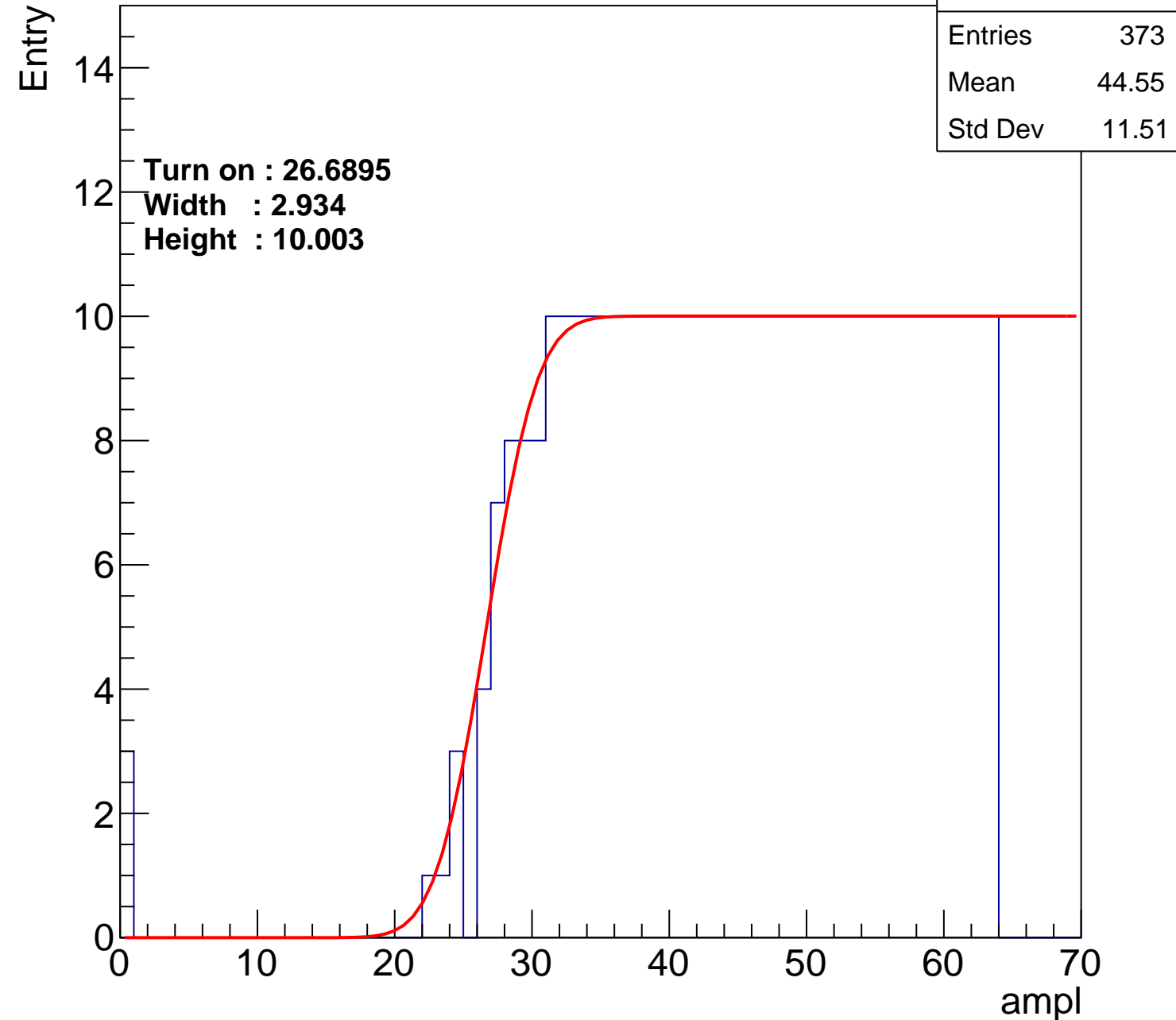
Width : 2.934

Height : 10.003

Entry

14
12
10
8
6
4
2
0

ampl



calib_packv5_042523_0143.root, FC#0, port D2

calib_packv5_042523_0143.root, FC#0, port D2

Turn on : 25.7320
Width : 2.994
Height : 10.041



B1L101S, U19-ch34

calib_packv5_042523_0143.root, FC#0, port D2

Entries	377
Mean	44.44
Std Dev	11.32

Turn on : 27.0304

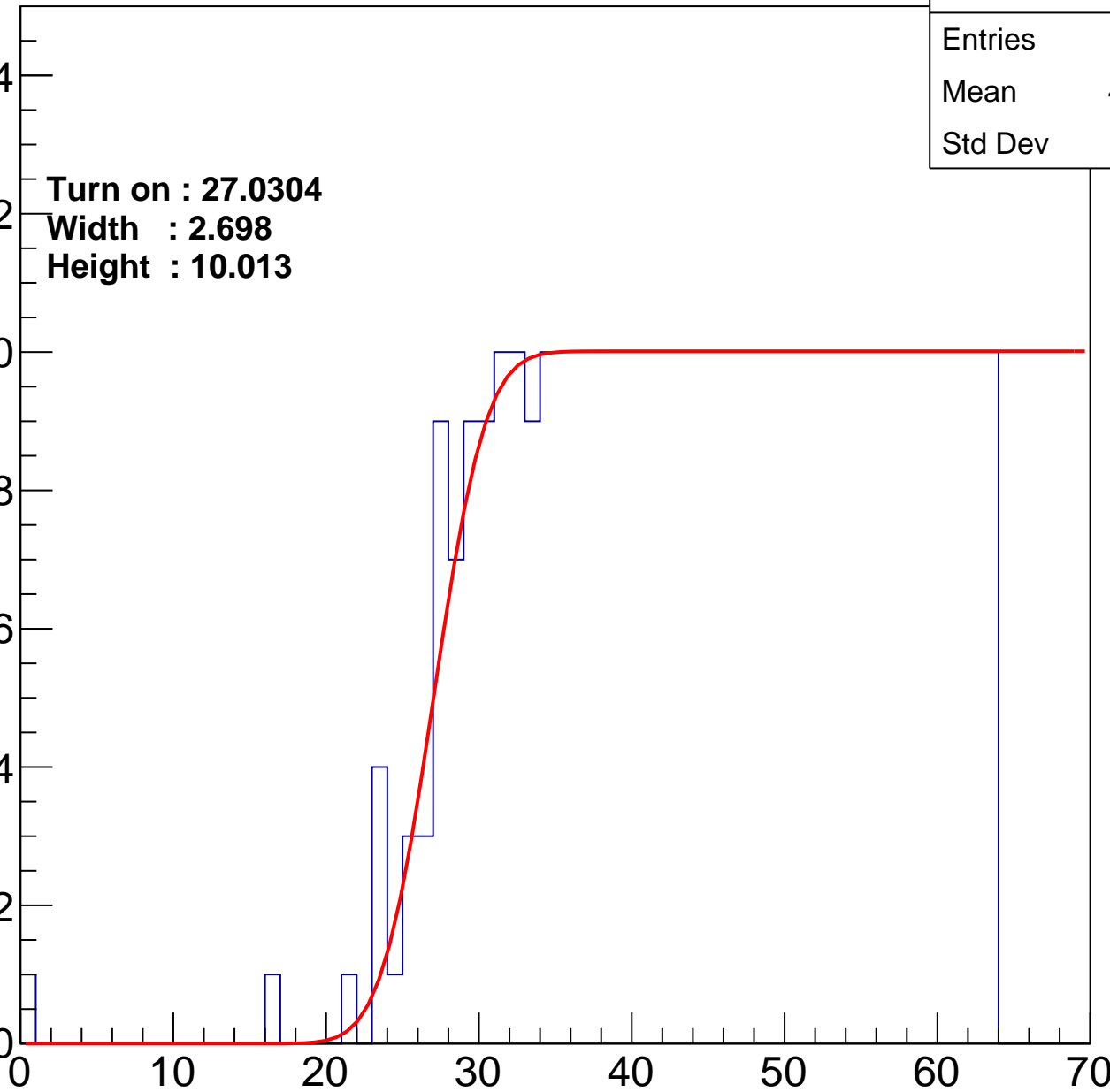
Width : 2.698

Height : 10.013

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch35

calib_packv5_042523_0143.root, FC#0, port D2

Entries	382
Mean	44.22
Std Dev	11.65

Turn on : 26.4546

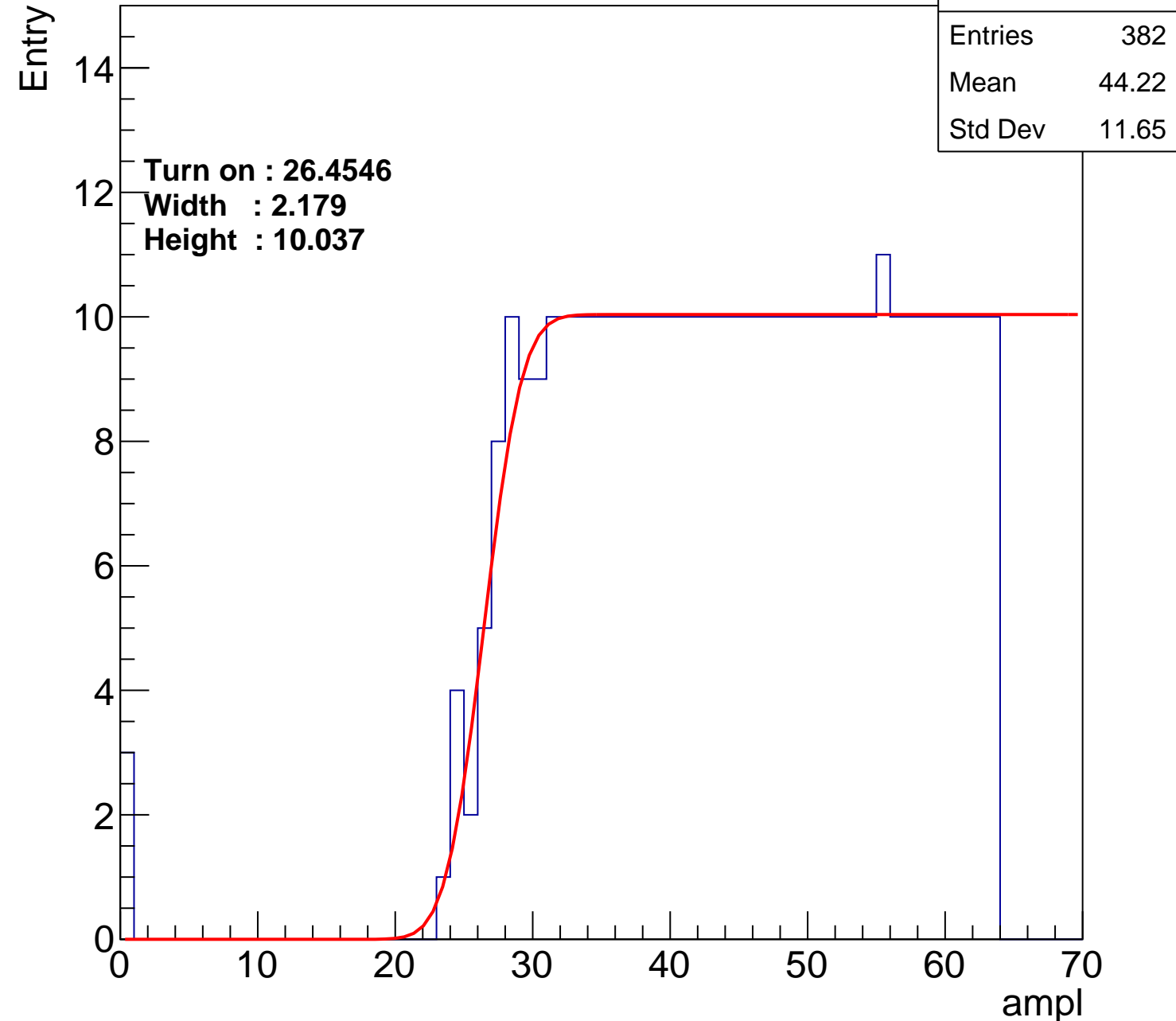
Width : 2.179

Height : 10.037

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch36

calib_packv5_042523_0143.root, FC#0, port D2

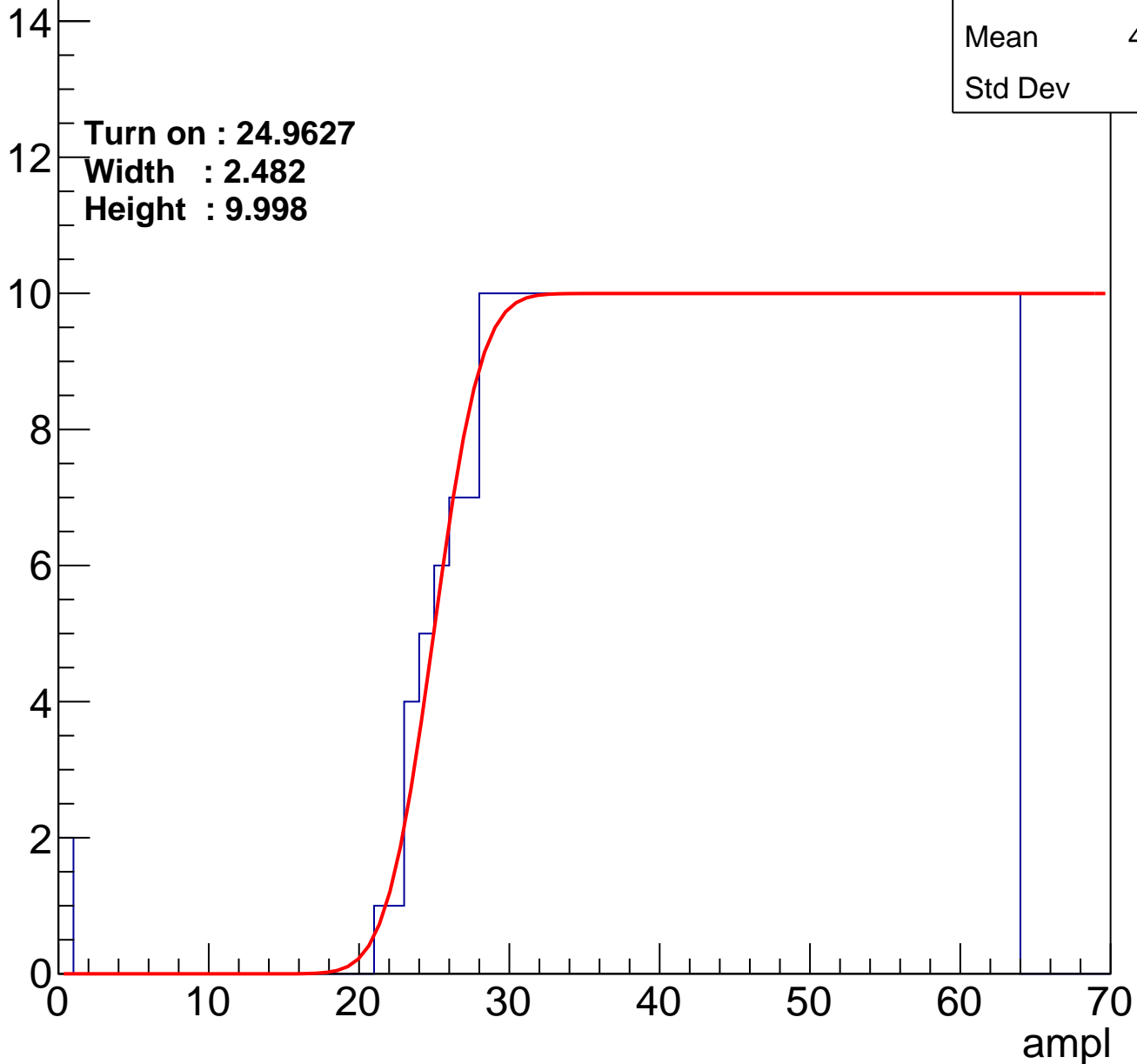
Entries	393
Mean	43.65
Std Dev	11.8

Turn on : 24.9627

Width : 2.482

Height : 9.998

Entry



B1L101S, U19-ch37

calib_packv5_042523_0143.root, FC#0, port D2

Entries	370
Mean	44.72
Std Dev	11.32

Turn on : 27.3156

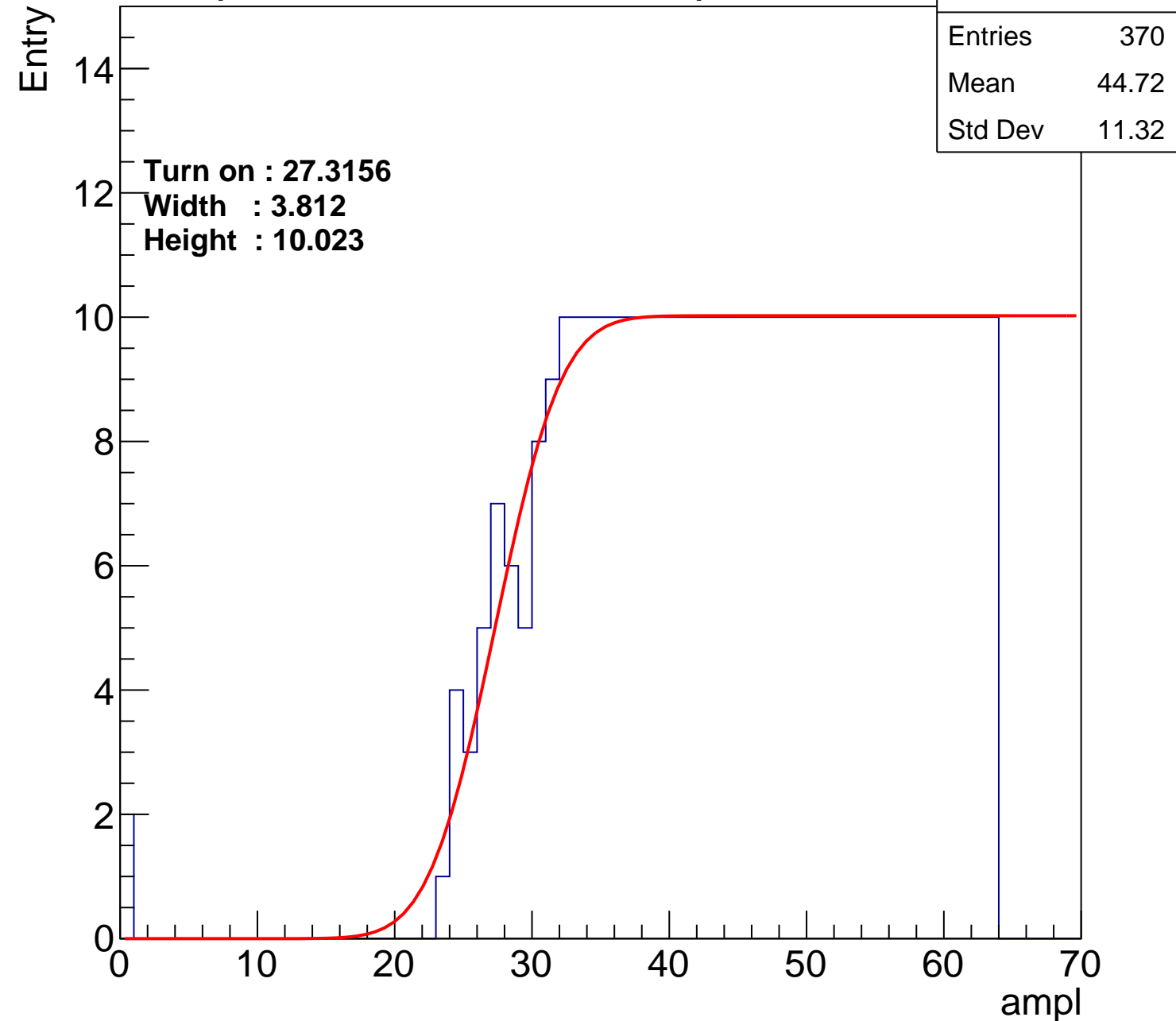
Width : 3.812

Height : 10.023

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch38

calib_packv5_042523_0143.root, FC#0, port D2

Entries	369
Mean	44.7
Std Dev	11.49

Turn on : 28.1144

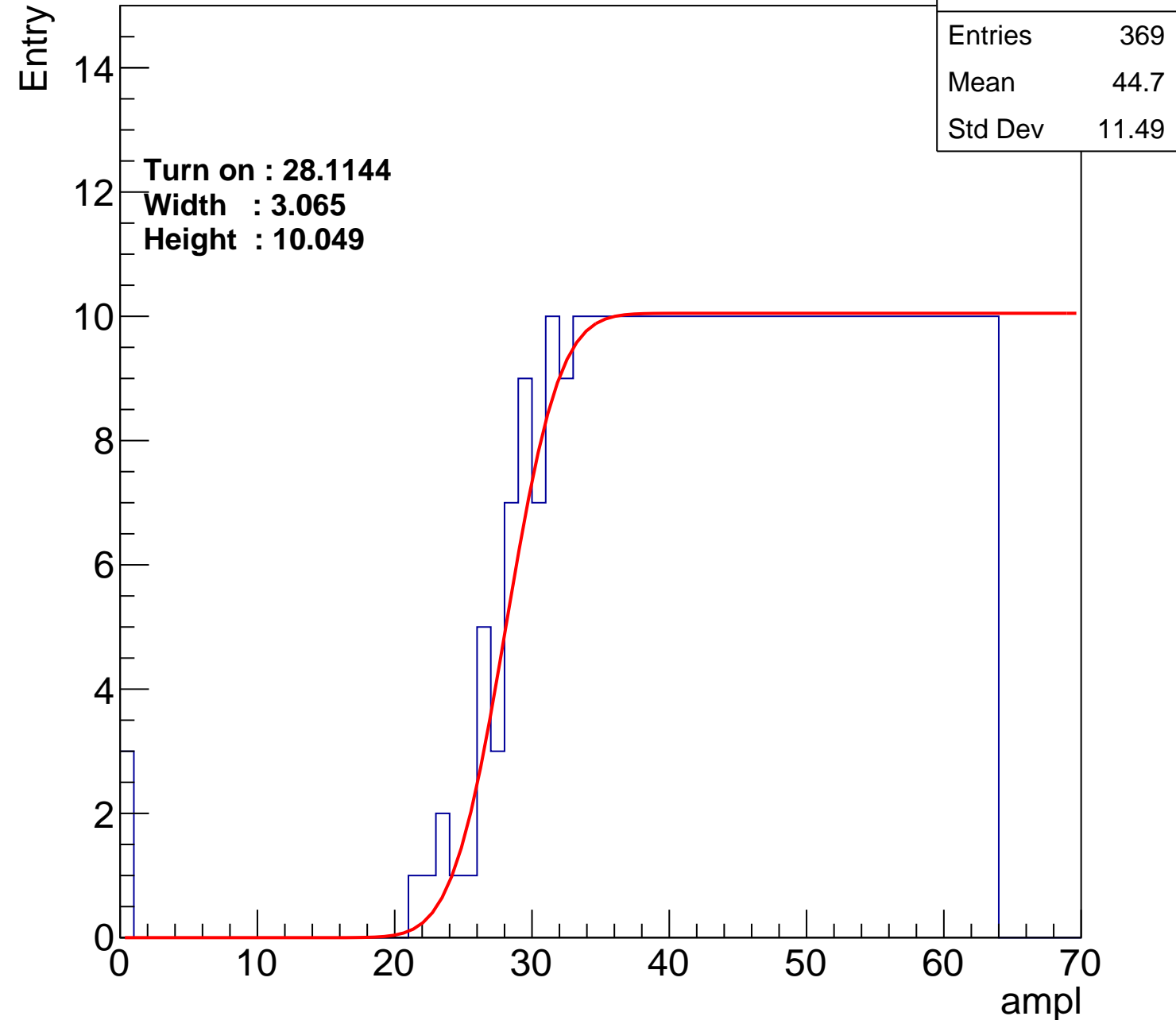
Width : 3.065

Height : 10.049

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch39

calib_packv5_042523_0143.root, FC#0, port D2

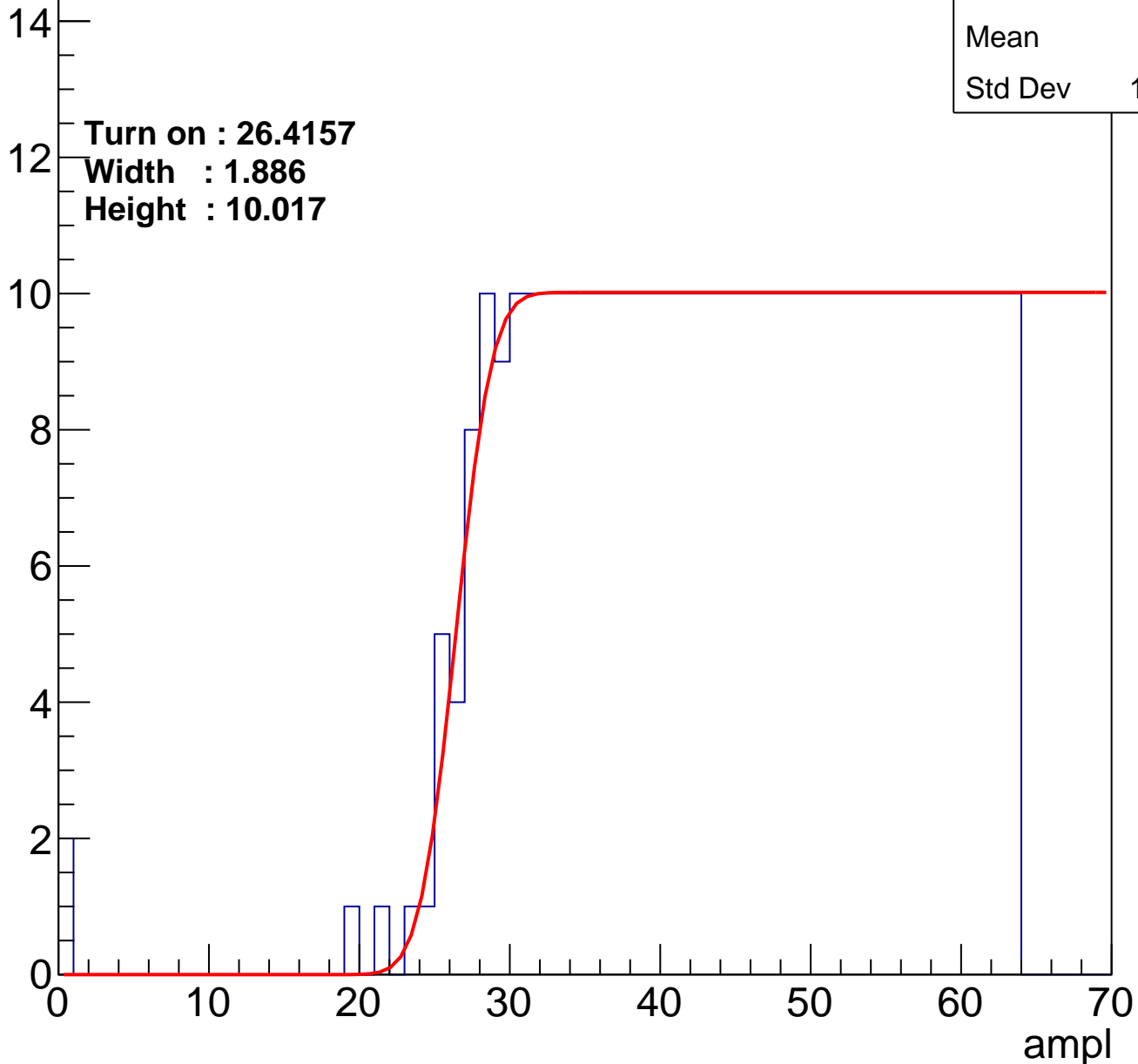
Entries	382
Mean	44.2
Std Dev	11.52

Turn on : 26.4157

Width : 1.886

Height : 10.017

Entry



B1L101S, U19-ch40

calib_packv5_042523_0143.root, FC#0, port D2

Entries	389
Mean	43.7
Std Dev	12.07

Turn on : 25.6204

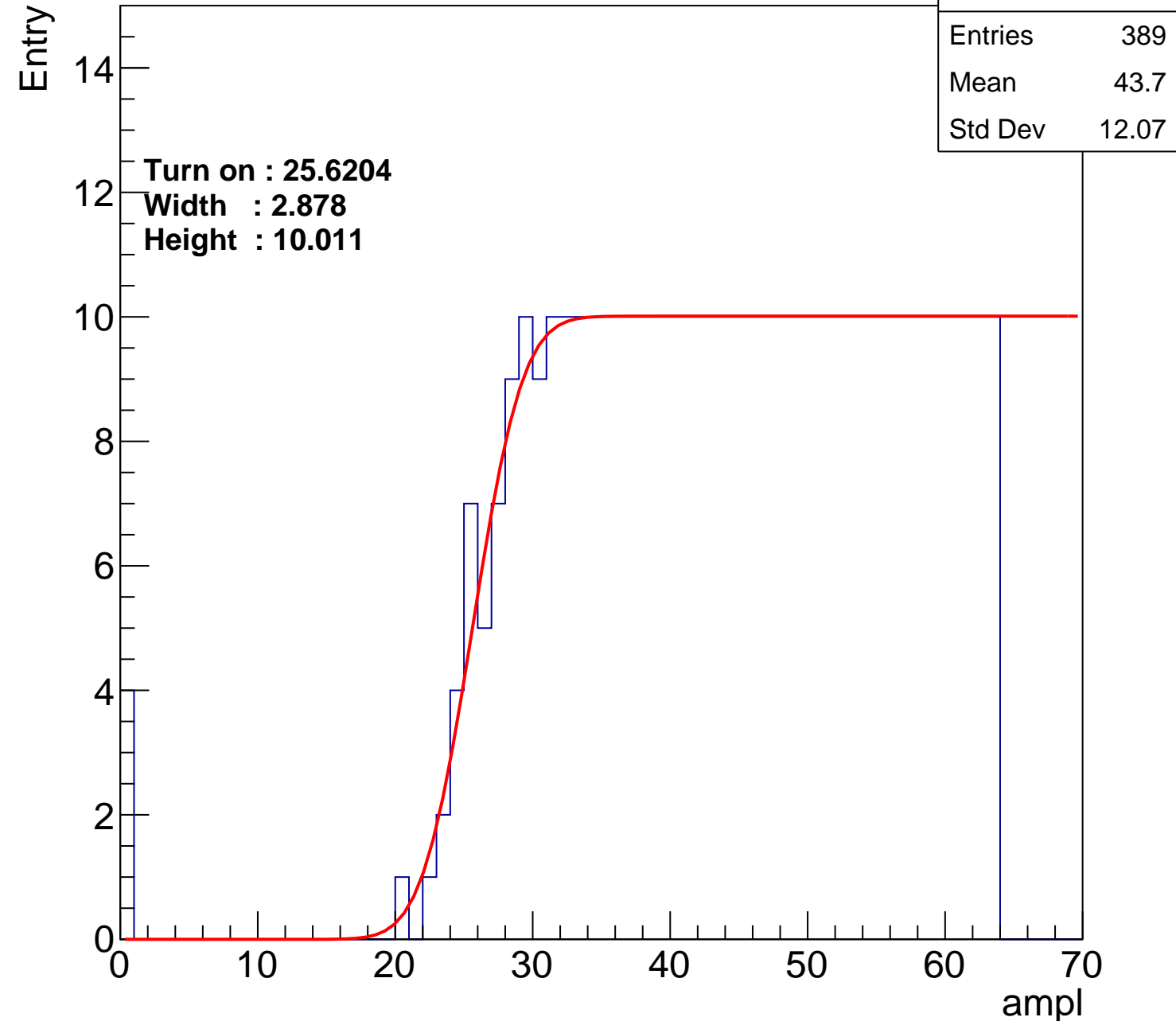
Width : 2.878

Height : 10.011

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch41

calib_packv5_042523_0143.root, FC#0, port D2

Entries	353
Mean	45.62
Std Dev	10.79

Turn on : 28.8383

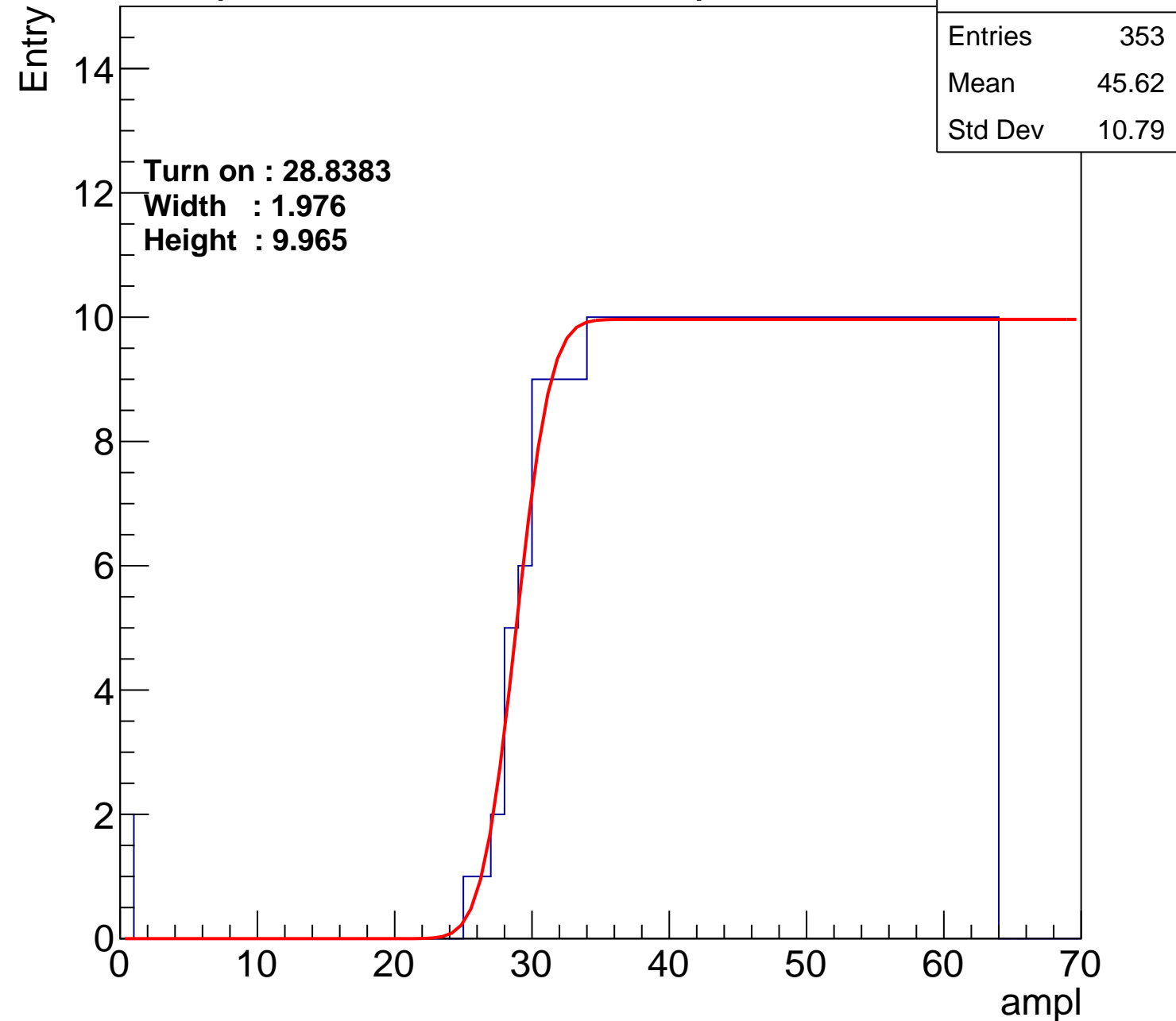
Width : 1.976

Height : 9.965

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch42

calib_packv5_042523_0143.root, FC#0, port D2

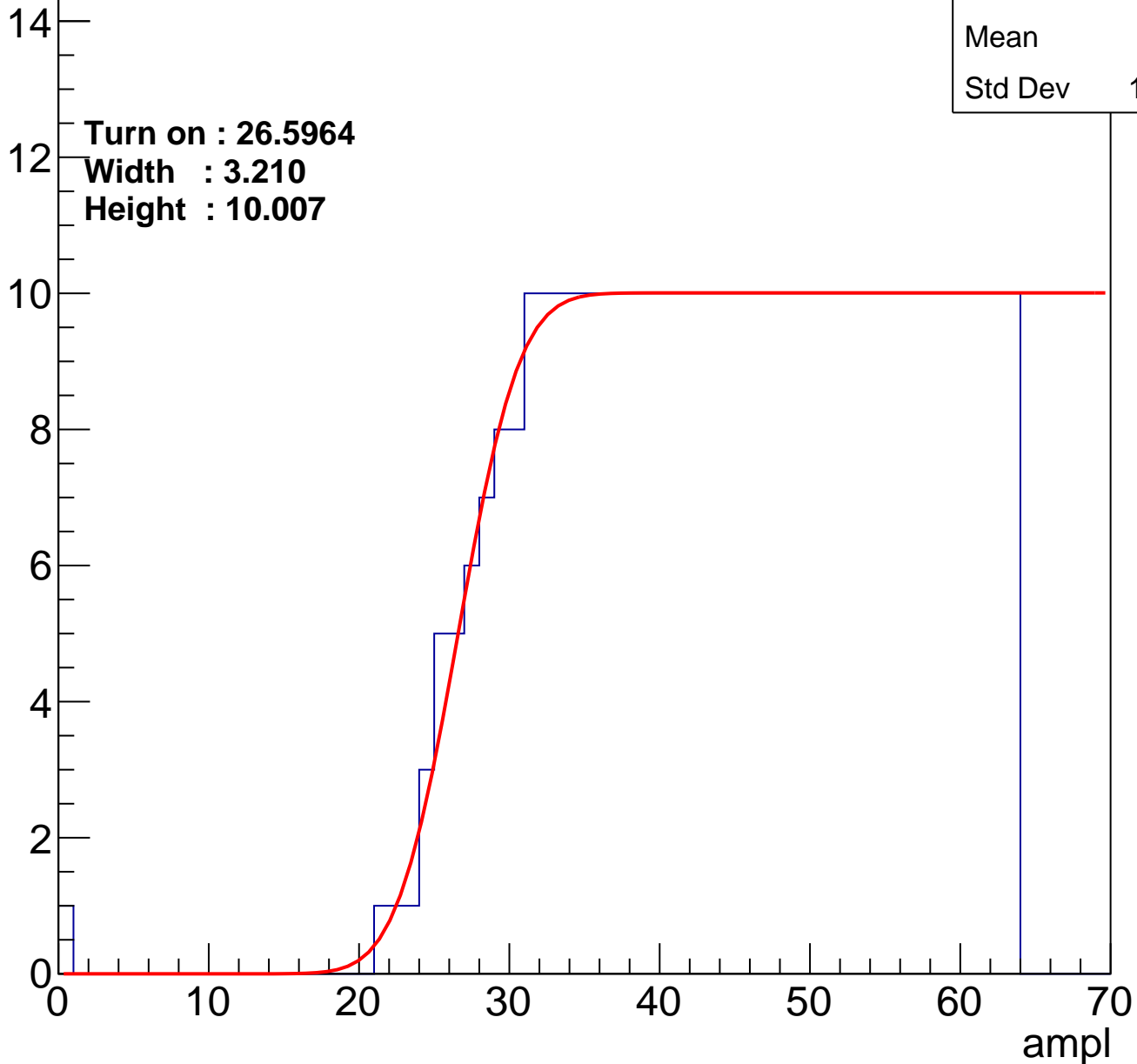
Entries	376
Mean	44.5
Std Dev	11.26

Turn on : 26.5964

Width : 3.210

Height : 10.007

Entry



B1L101S, U19-ch43

calib_packv5_042523_0143.root, FC#0, port D2

Entries	364
Mean	44.82
Std Dev	11.73

Turn on : 27.8955

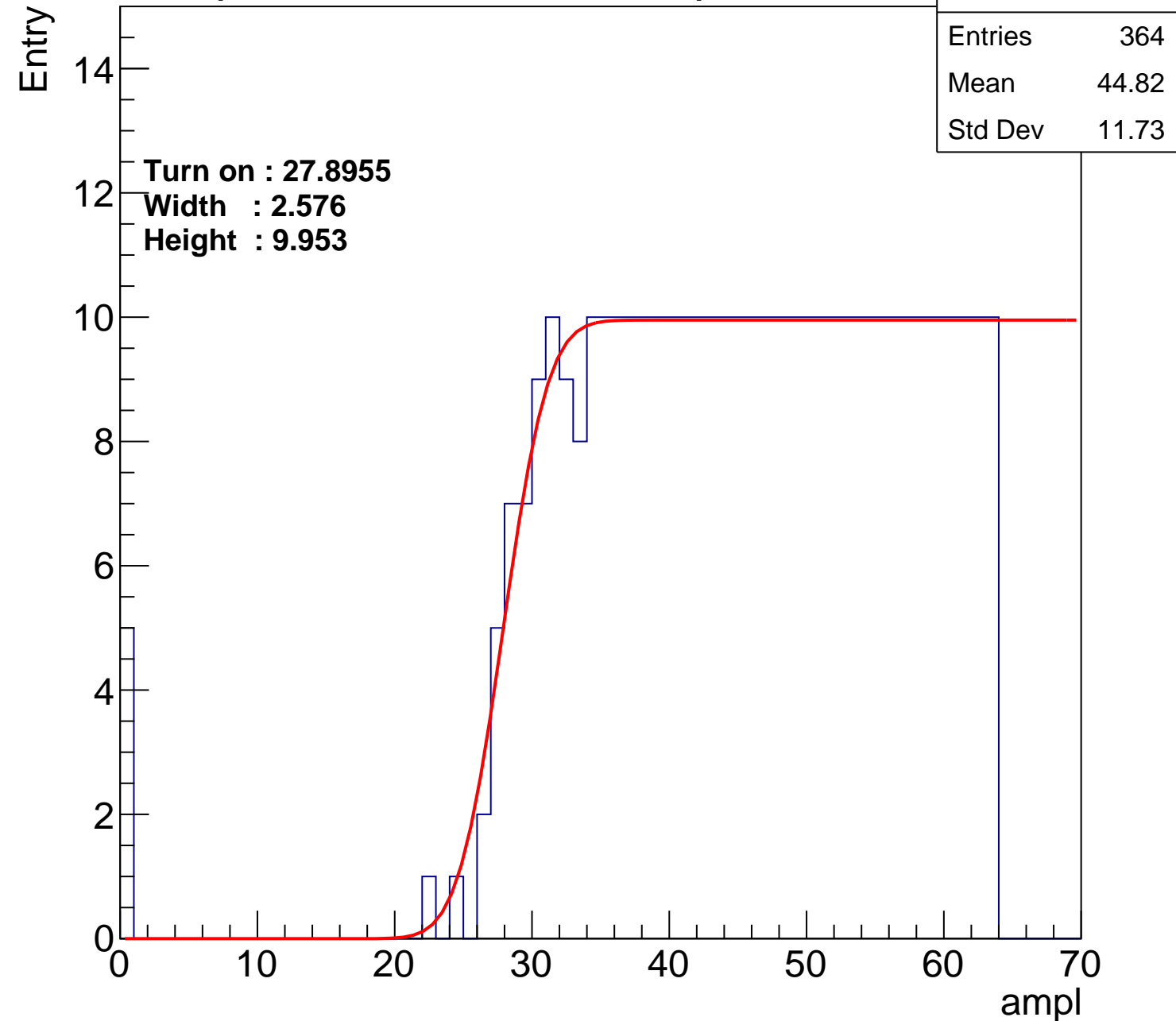
Width : 2.576

Height : 9.953

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch44

calib_packv5_042523_0143.root, FC#0, port D2

Entries	390
Mean	43.83
Std Dev	11.62

Turn on : 25.2827

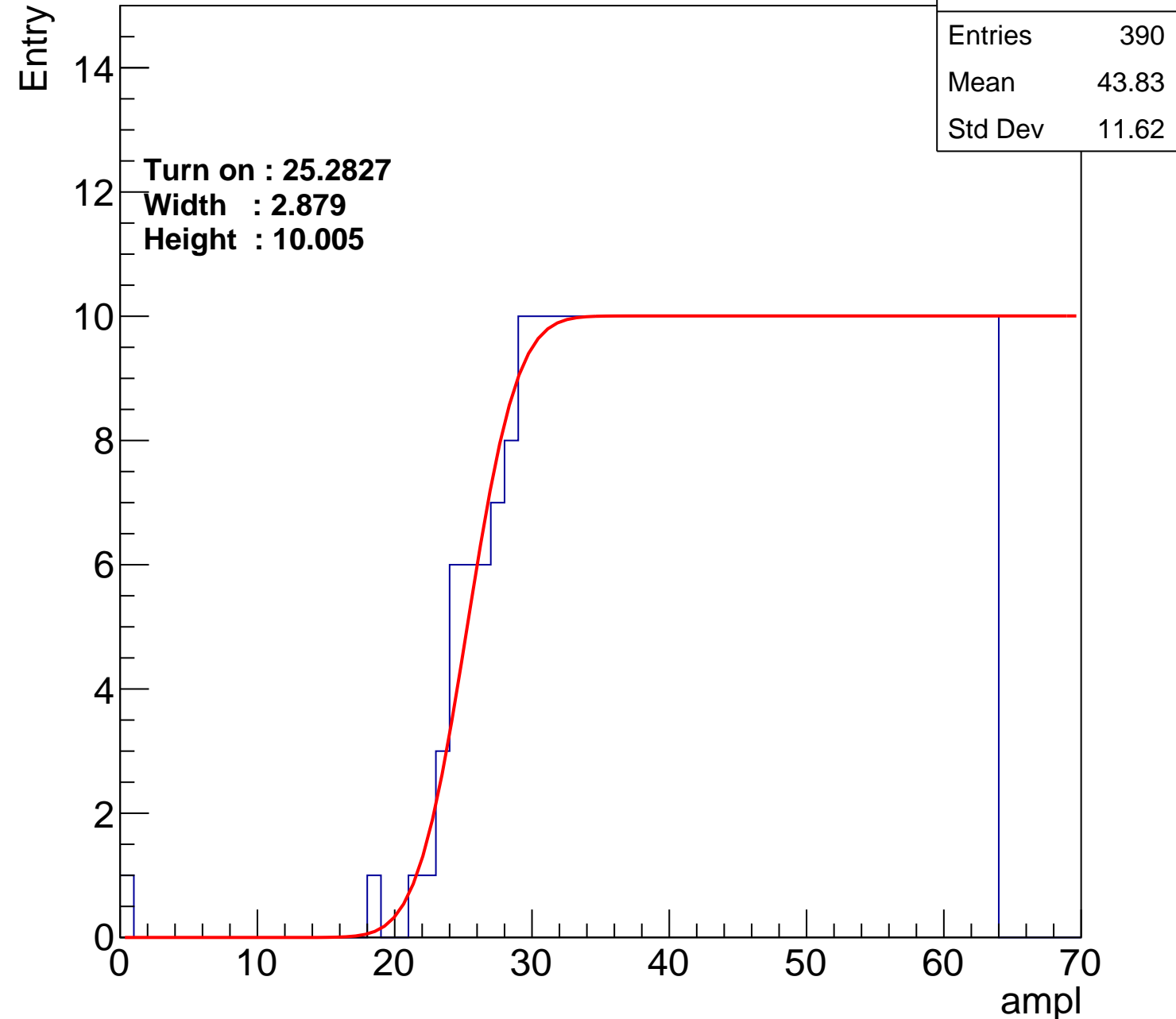
Width : 2.879

Height : 10.005

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch45

calib_packv5_042523_0143.root, FC#0, port D2

Entries	365
Mean	45.06
Std Dev	10.94

Turn on : 27.8010

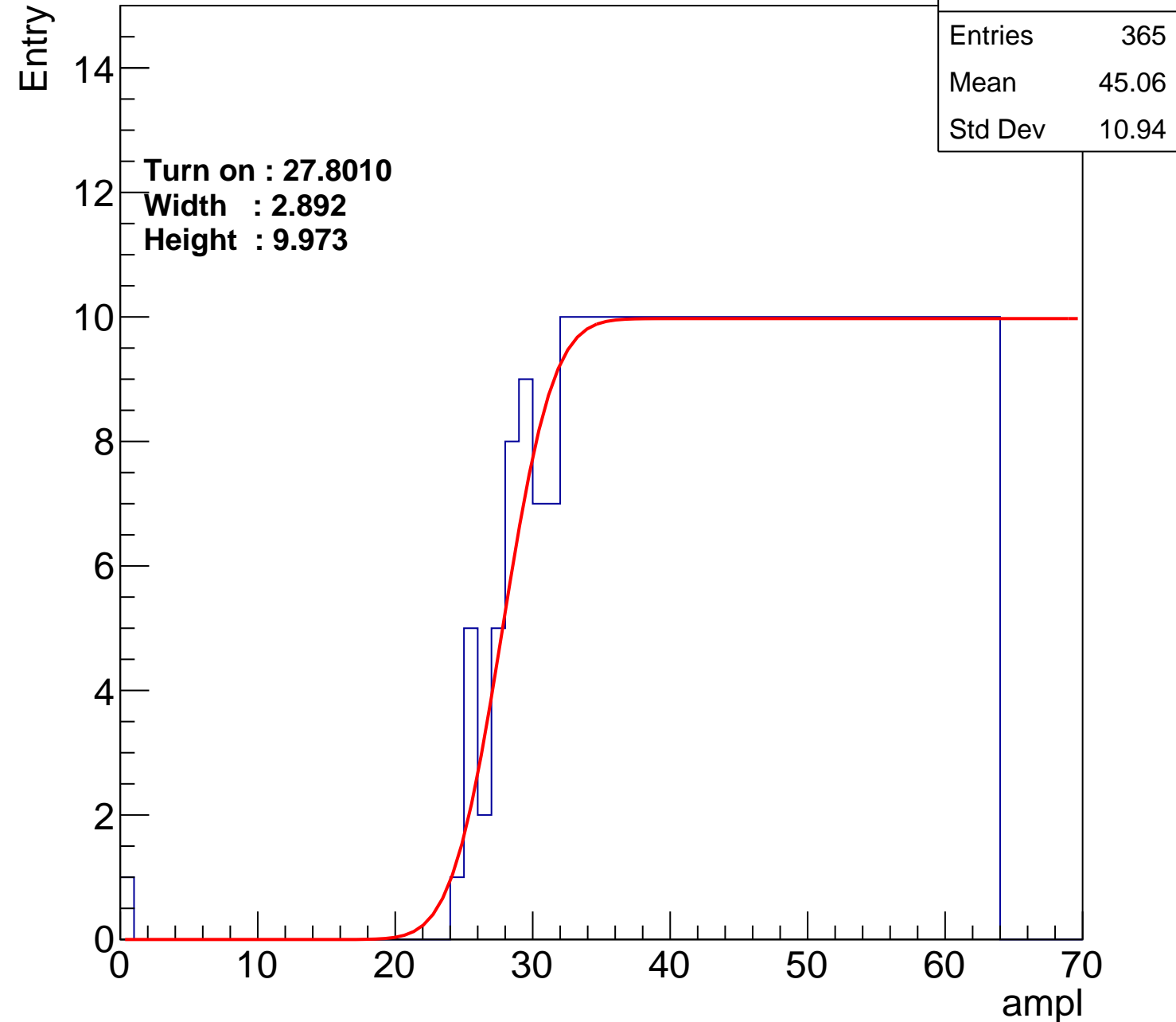
Width : 2.892

Height : 9.973

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch46

calib_packv5_042523_0143.root, FC#0, port D2

Entries	374
Mean	44.59
Std Dev	11.31

Turn on : 27.3501

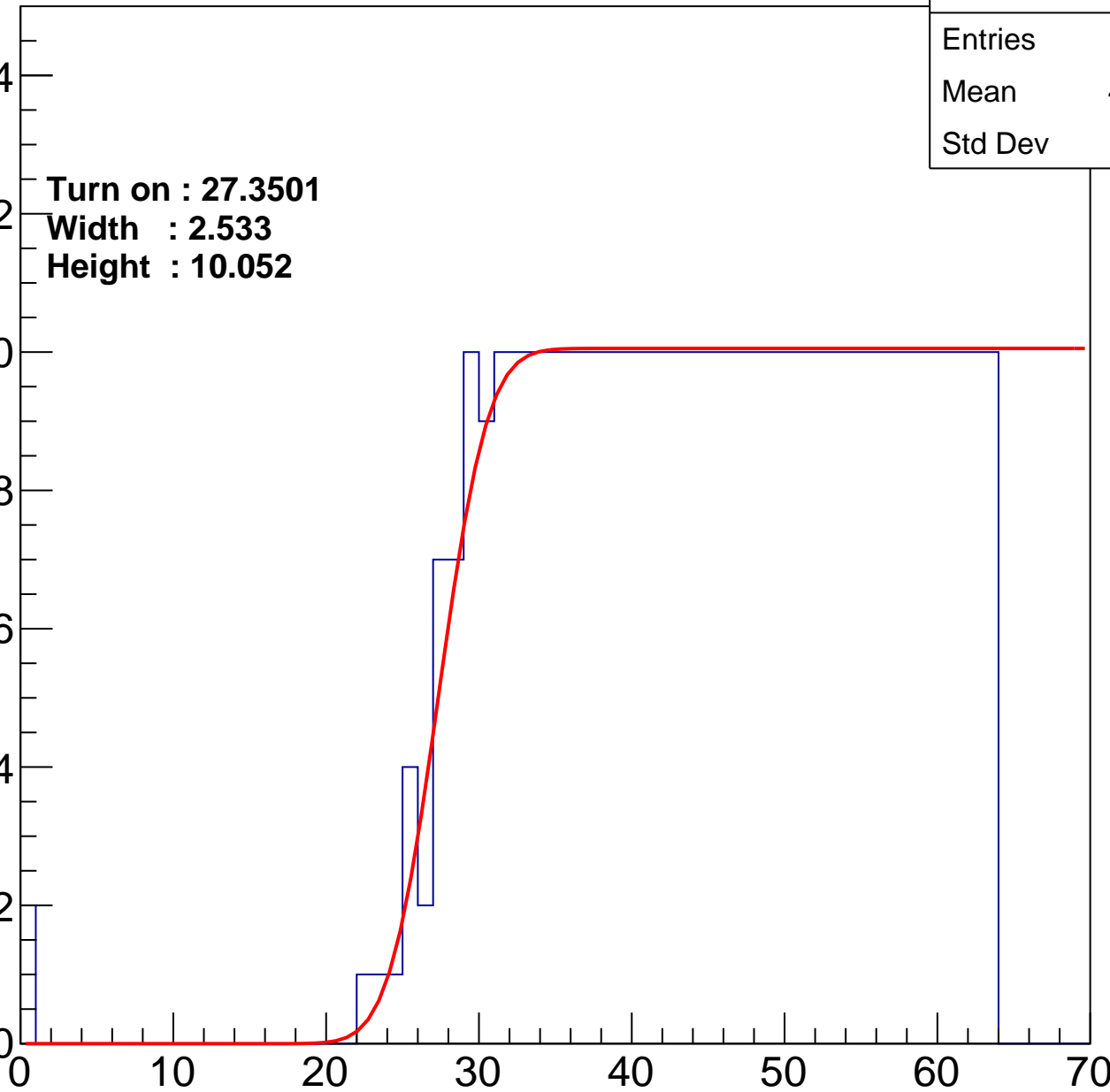
Width : 2.533

Height : 10.052

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch47

calib_packv5_042523_0143.root, FC#0, port D2

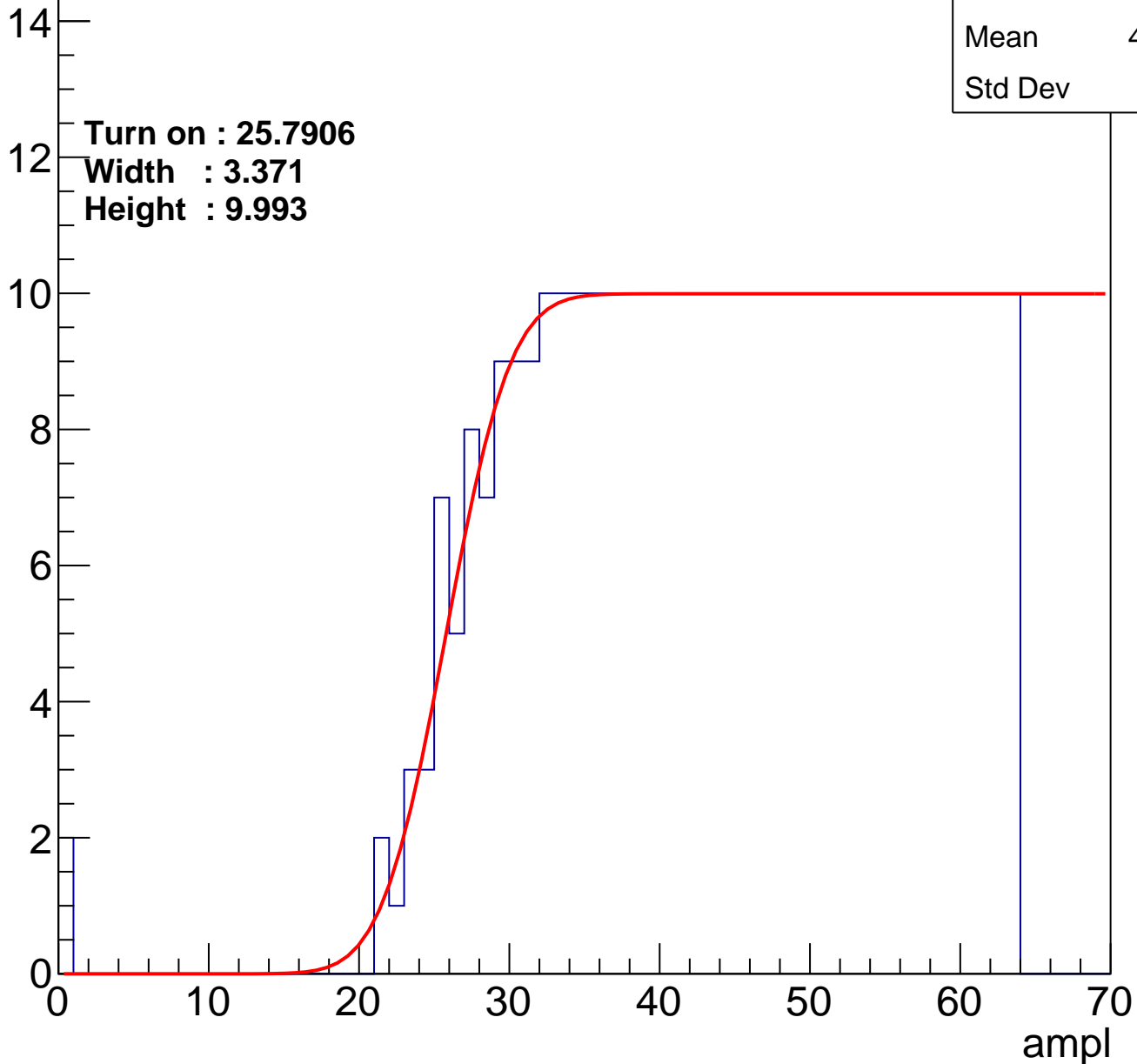
Entries	385
Mean	43.98
Std Dev	11.7

Turn on : 25.7906

Width : 3.371

Height : 9.993

Entry



B1L101S, U19-ch48

calib_packv5_042523_0143.root, FC#0, port D2

Entries	393
Mean	43.6
Std Dev	11.96

Turn on : 24.9824

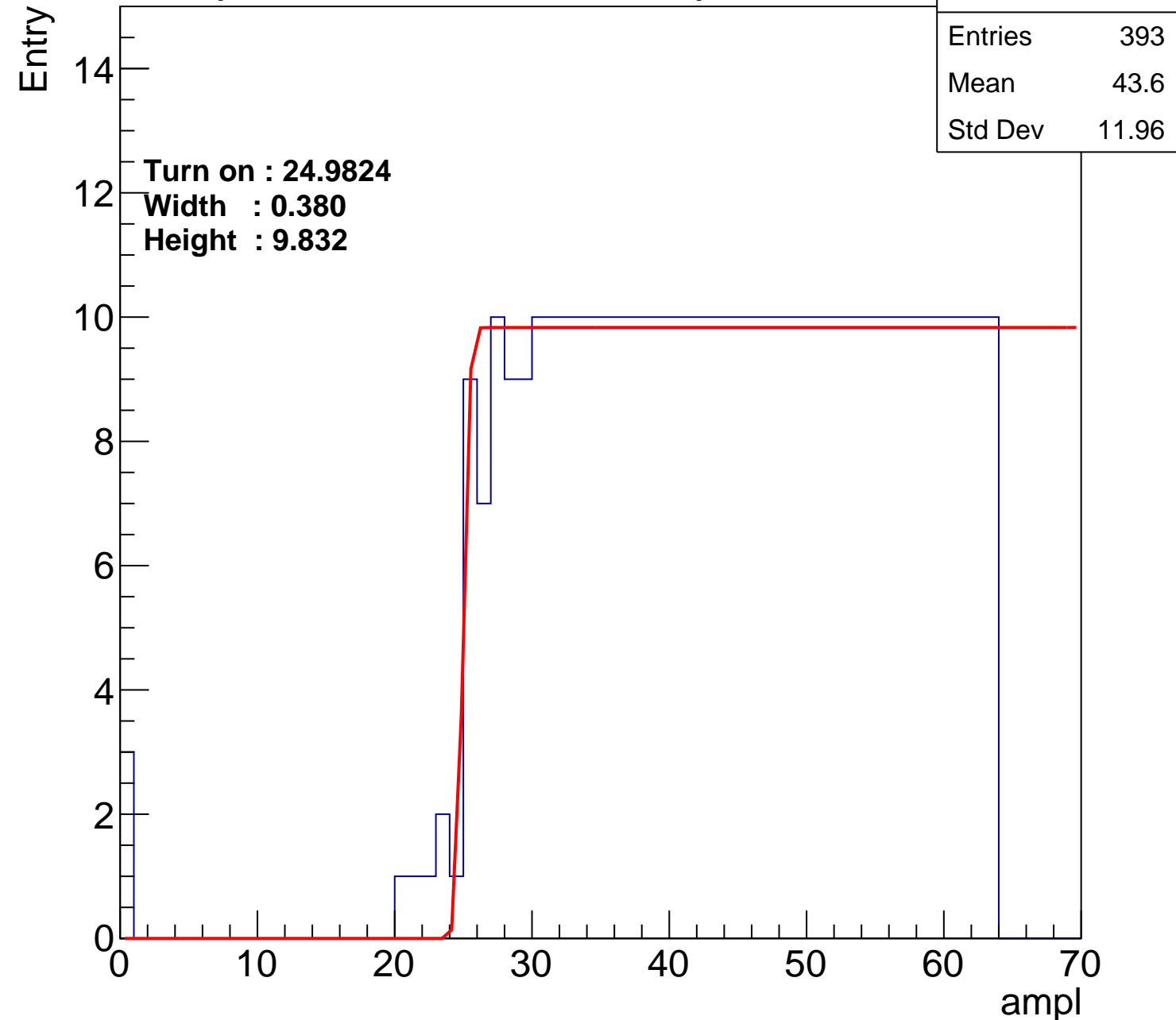
Width : 0.380

Height : 9.832

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch49

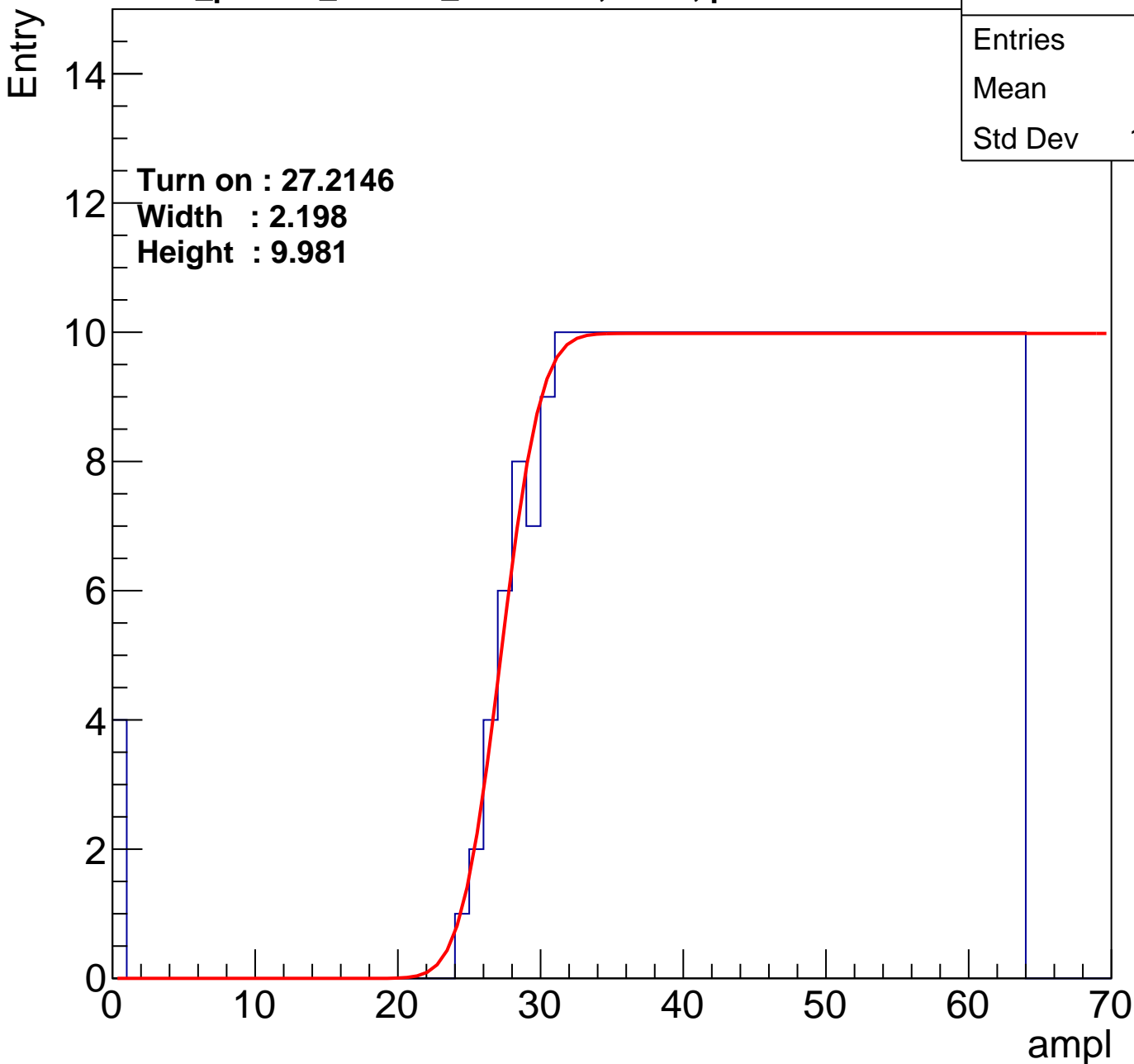
calib_packv5_042523_0143.root, FC#0, port D2

Entries	371
Mean	44.6
Std Dev	11.61

Turn on : 27.2146

Width : 2.198

Height : 9.981



B1L101S, U19-ch50

calib_packv5_042523_0143.root, FC#0, port D2

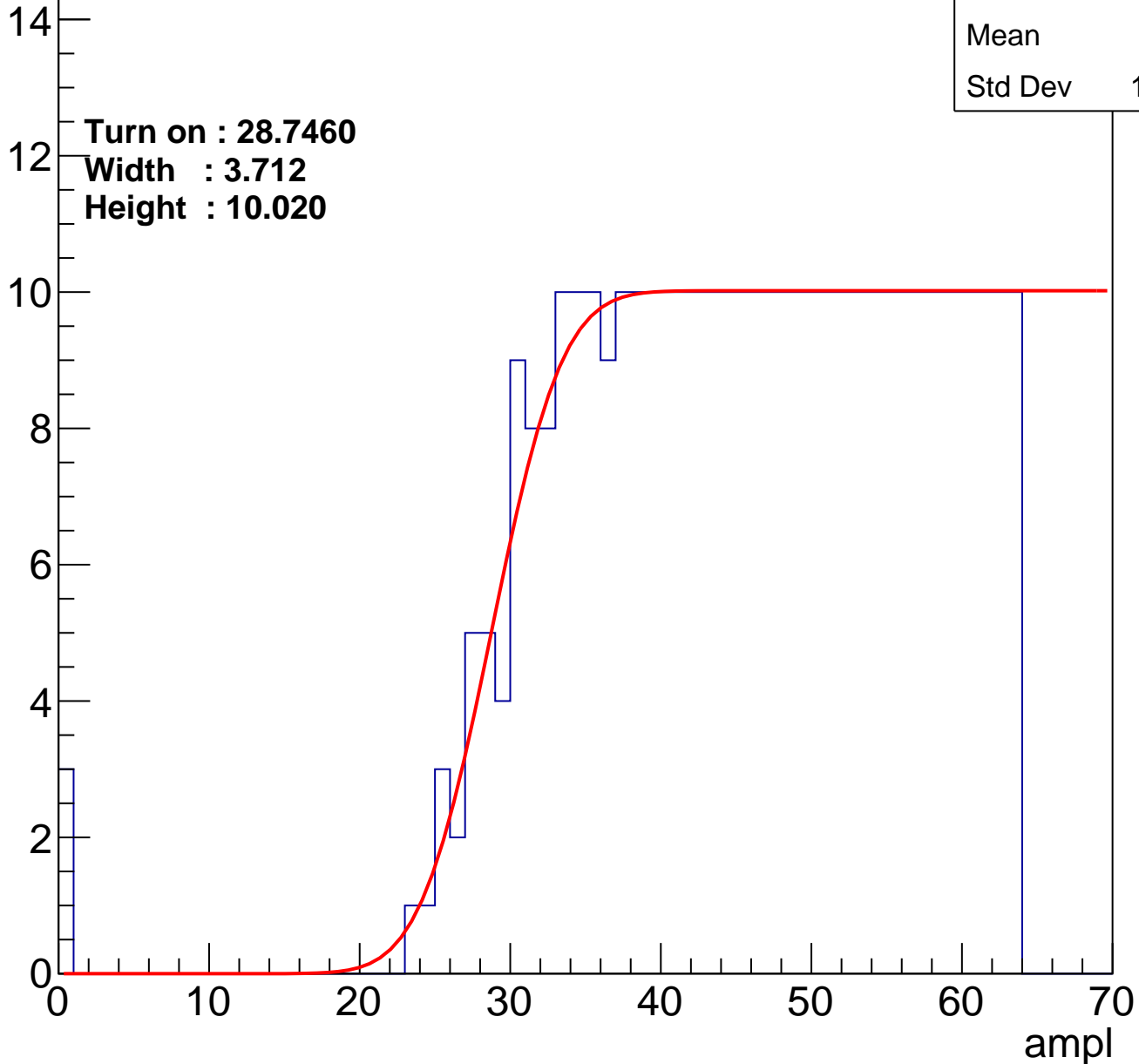
Entries	358
Mean	45.2
Std Dev	11.27

Turn on : 28.7460

Width : 3.712

Height : 10.020

Entry



B1L101S, U19-ch51

calib_packv5_042523_0143.root, FC#0, port D2

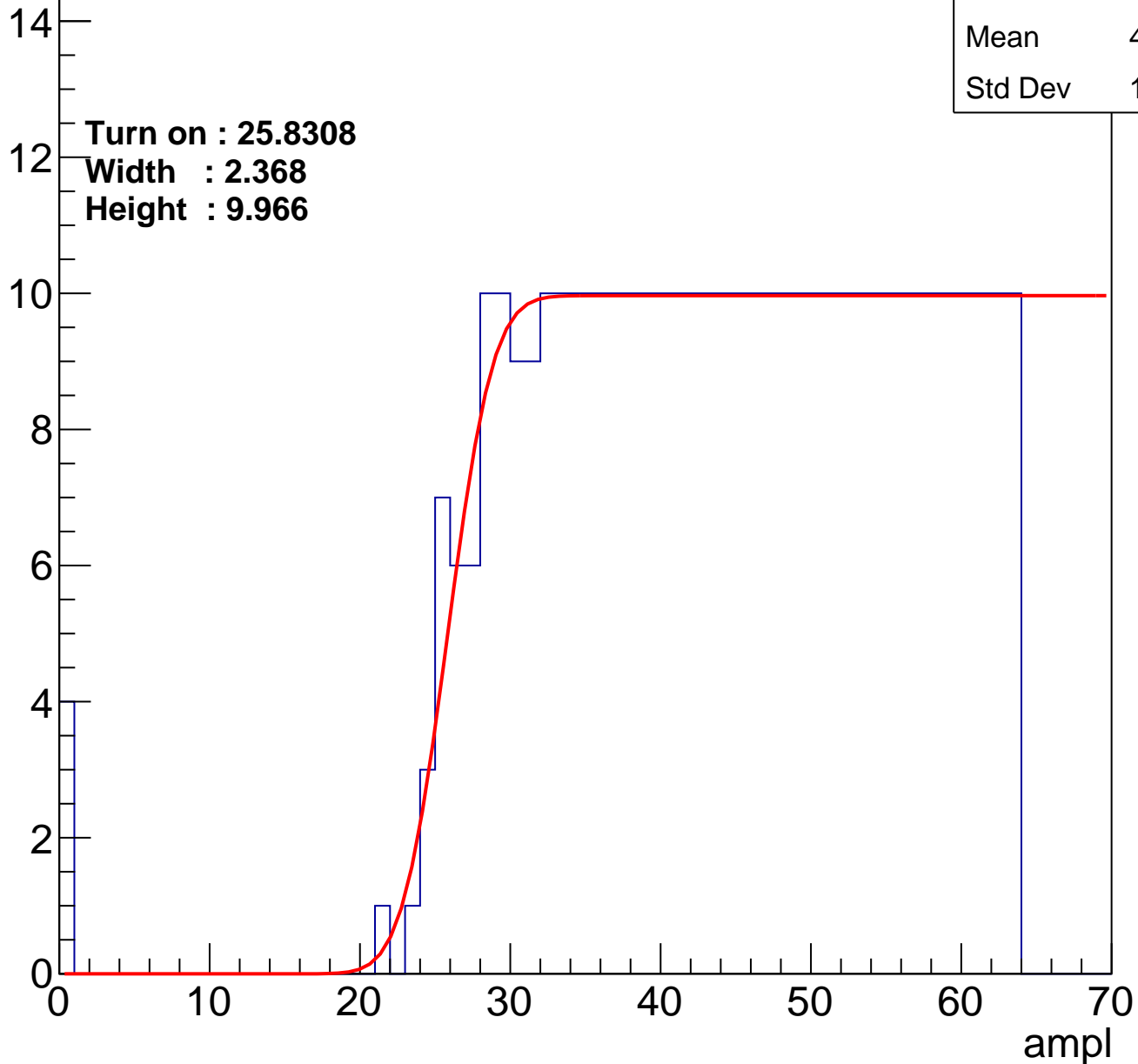
Entries	386
Mean	43.85
Std Dev	11.98

Turn on : 25.8308

Width : 2.368

Height : 9.966

Entry



B1L101S, U19-ch52

calib_packv5_042523_0143.root, FC#0, port D2

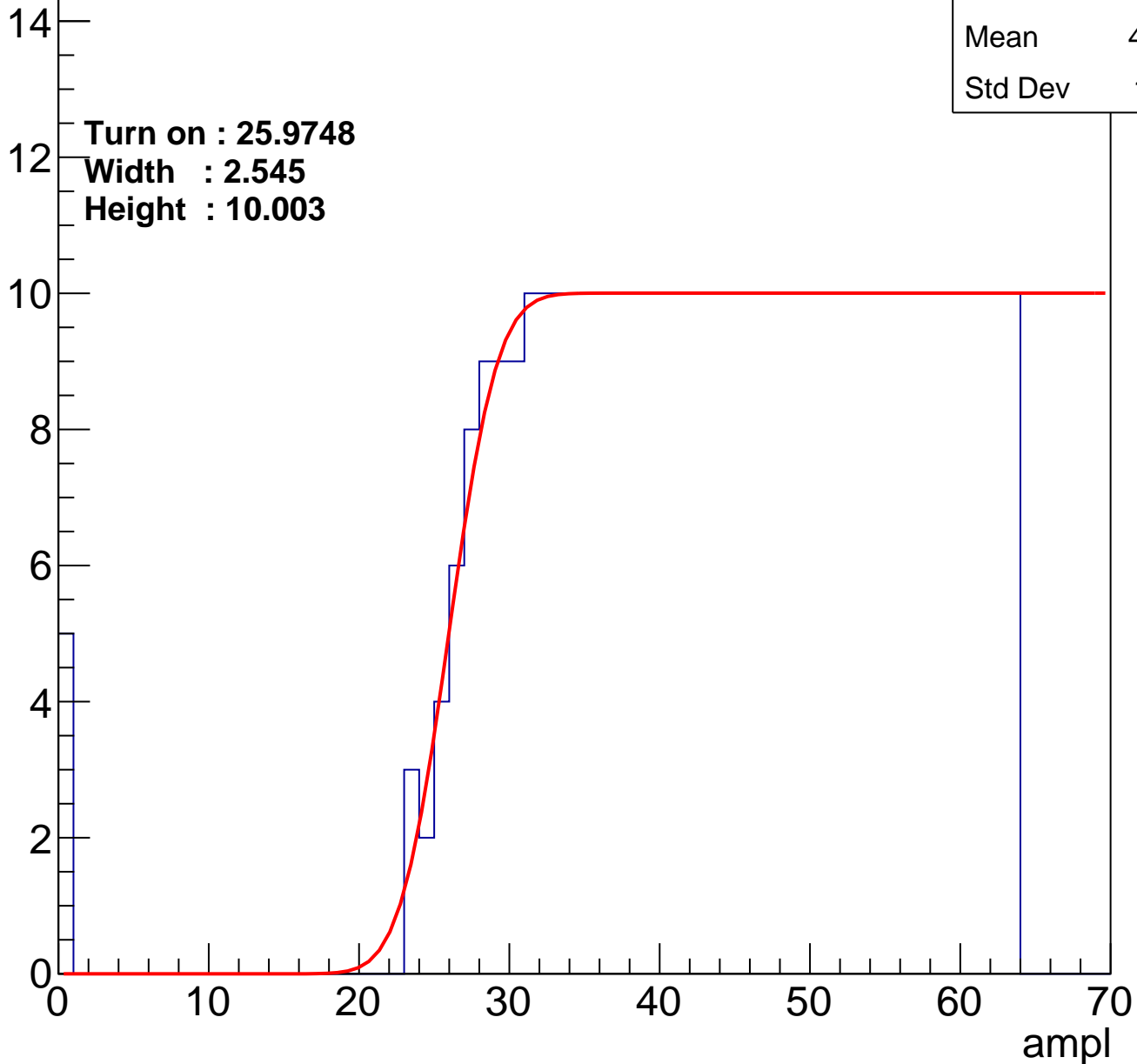
Entries	385
Mean	43.85
Std Dev	12.11

Turn on : 25.9748

Width : 2.545

Height : 10.003

Entry



B1L101S, U19-ch53

calib_packv5_042523_0143.root, FC#0, port D2

Entries	369
Mean	44.82
Std Dev	11.2

Turn on : 27.5955

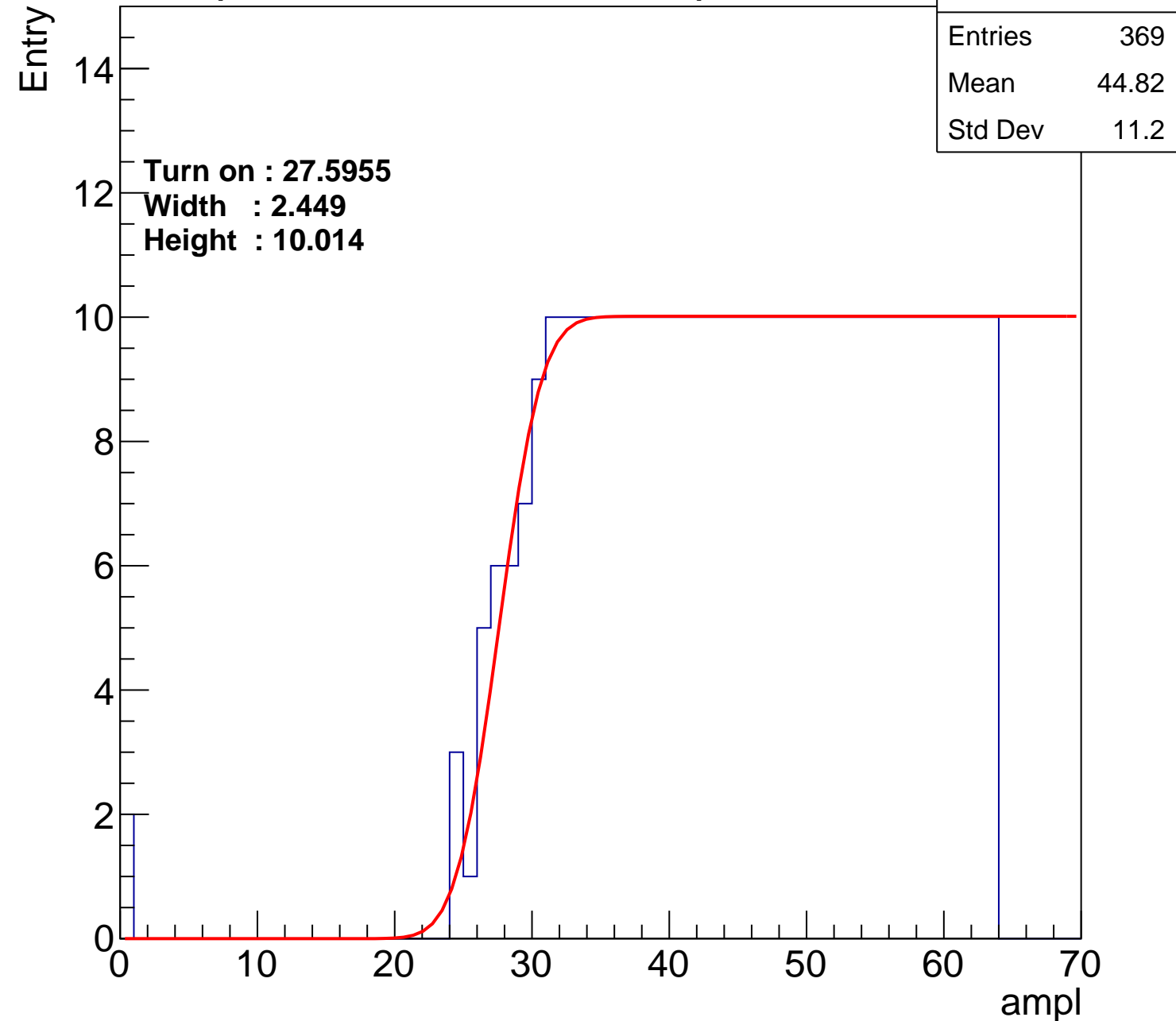
Width : 2.449

Height : 10.014

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch54

calib_packv5_042523_0143.root, FC#0, port D2

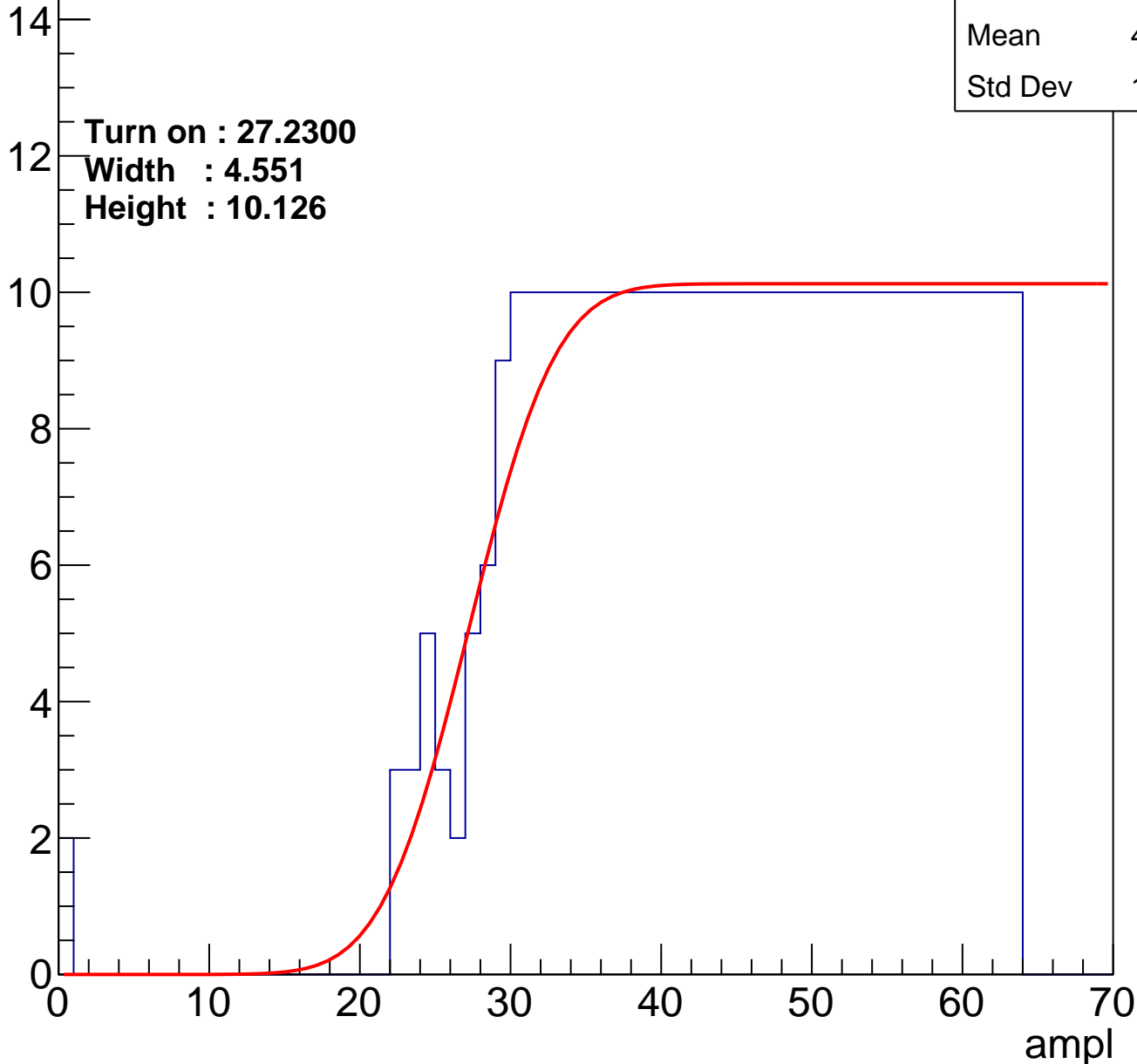
Entries	378
Mean	44.33
Std Dev	11.52

Turn on : 27.2300

Width : 4.551

Height : 10.126

Entry



B1L101S, U19-ch55

calib_packv5_042523_0143.root, FC#0, port D2

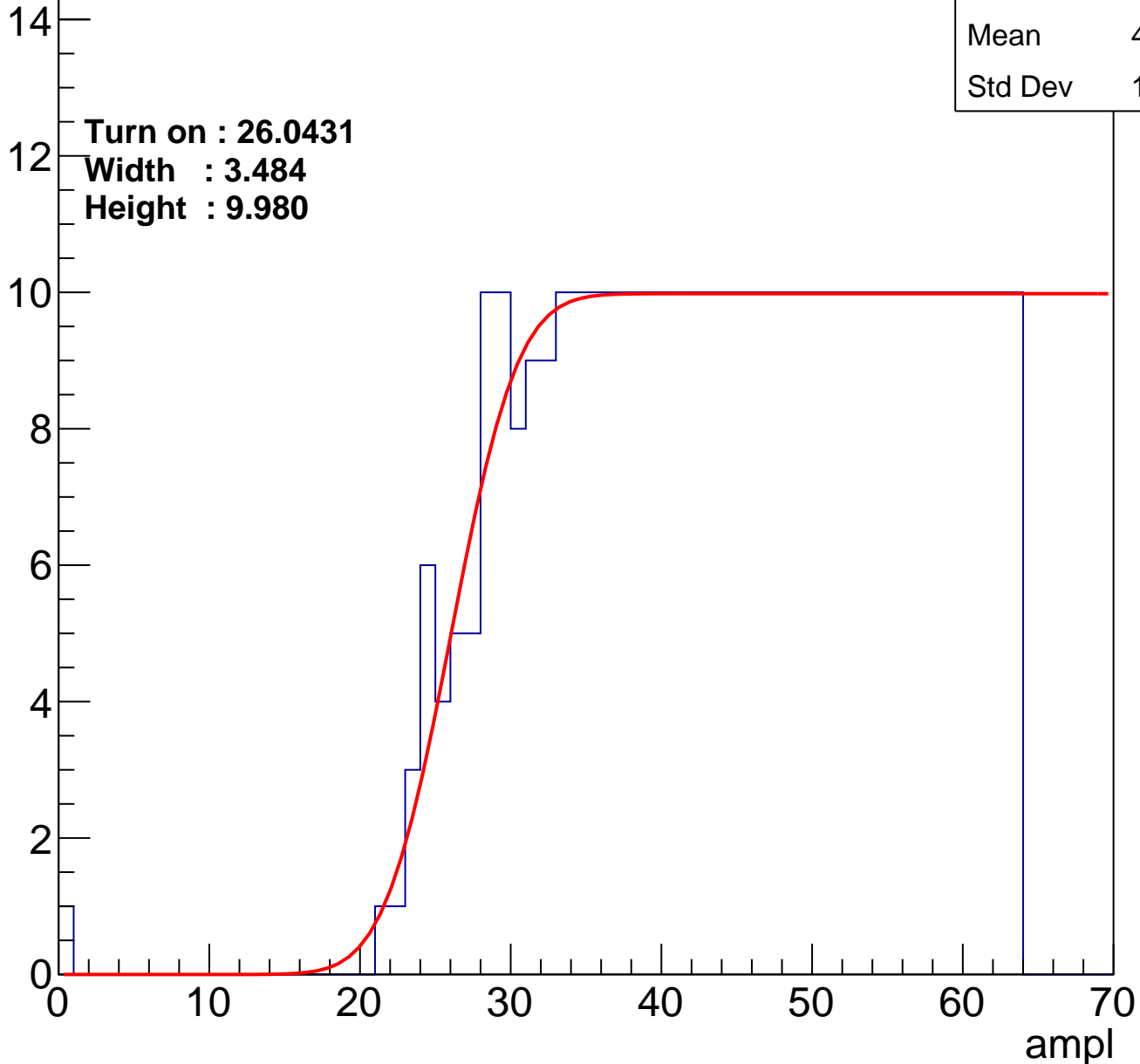
Entries	382
Mean	44.18
Std Dev	11.45

Turn on : 26.0431

Width : 3.484

Height : 9.980

Entry



B1L101S, U19-ch56

calib_packv5_042523_0143.root, FC#0, port D2

Entries	401
Mean	43.21
Std Dev	12.1

Turn on : 24.9298

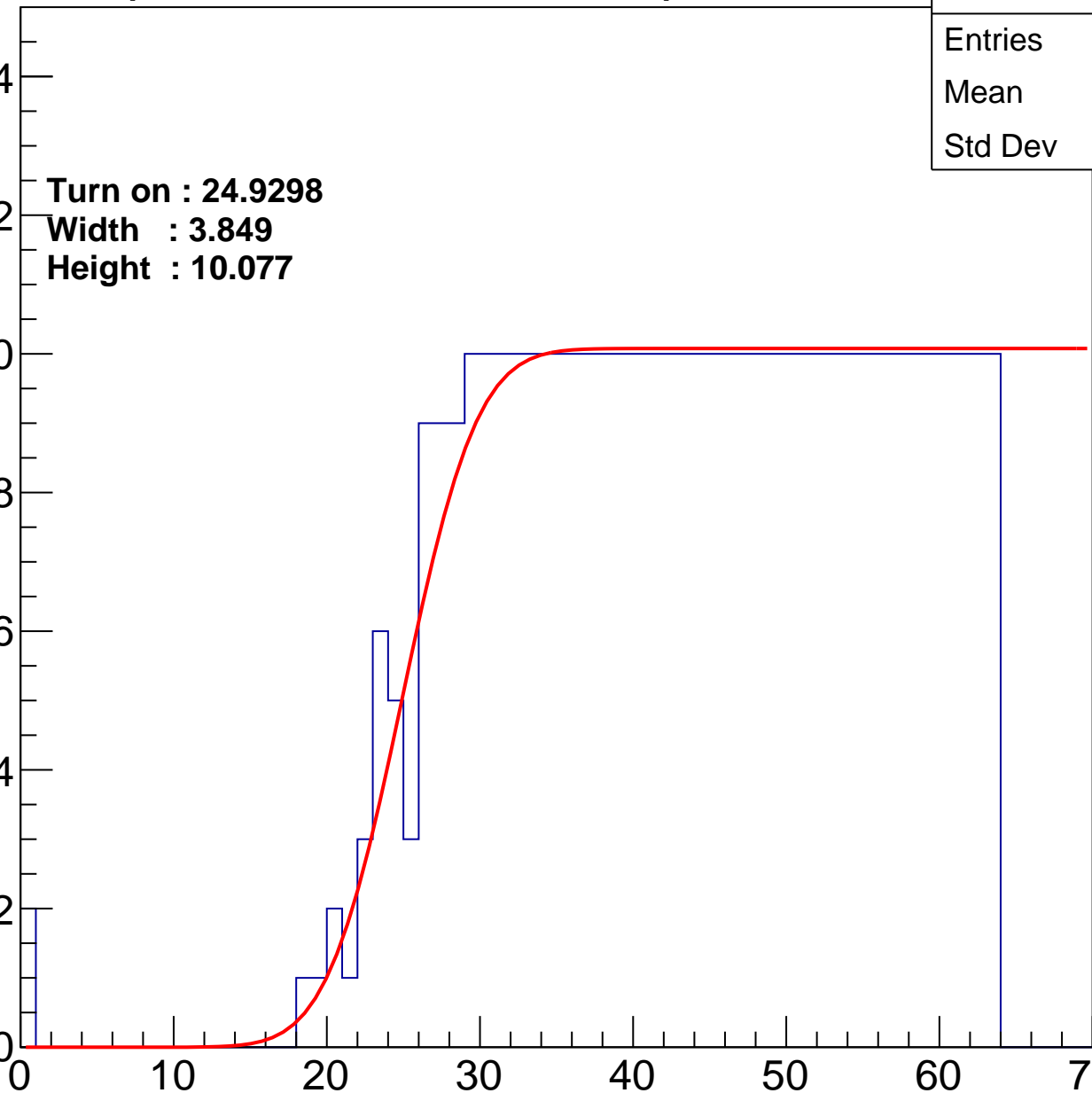
Width : 3.849

Height : 10.077

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch57

calib_packv5_042523_0143.root, FC#0, port D2

Entries	353
Mean	45.66
Std Dev	10.61

Turn on : 28.8708

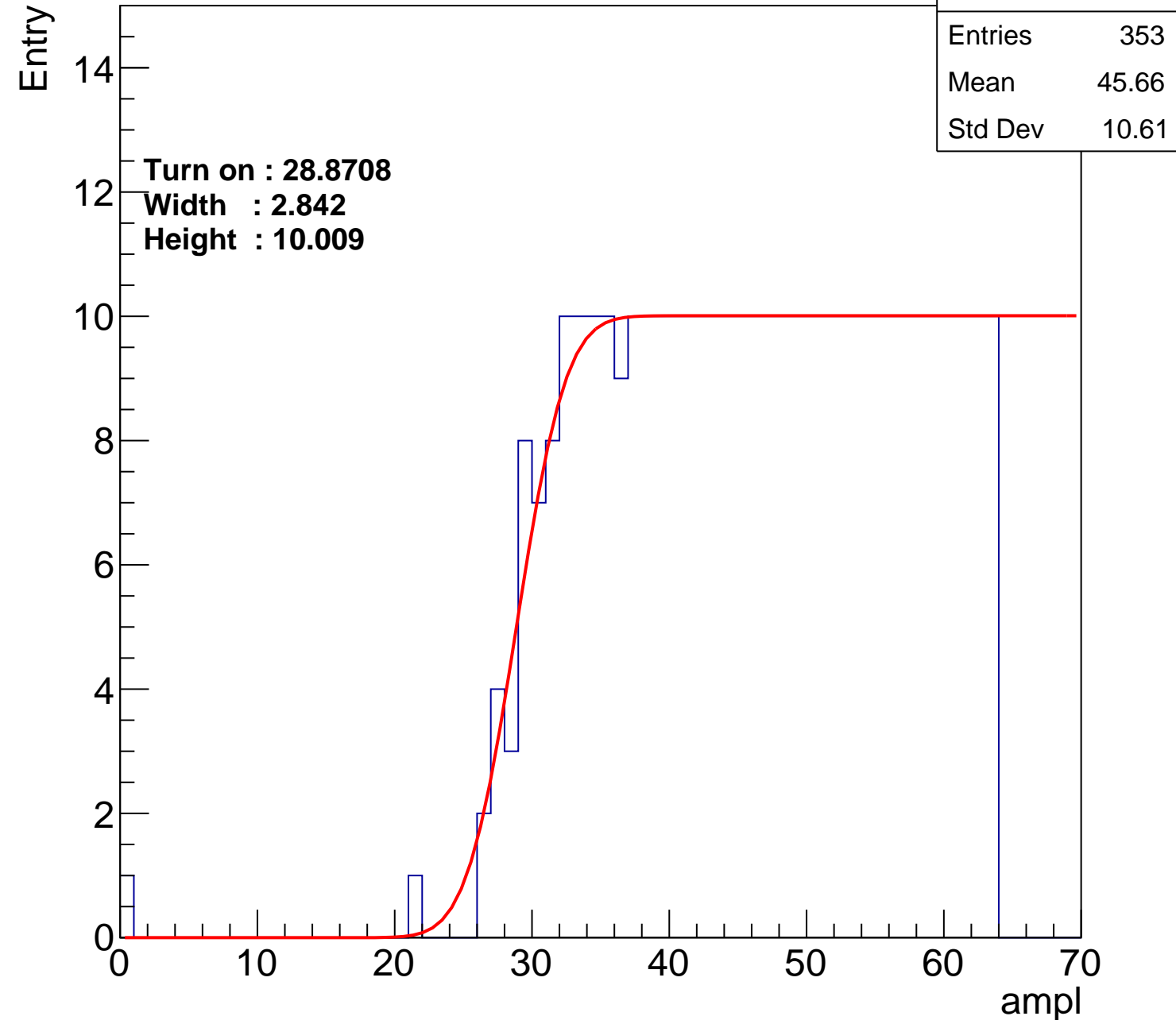
Width : 2.842

Height : 10.009

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch58

calib_packv5_042523_0143.root, FC#0, port D2

Entries	391
Mean	43.64
Std Dev	11.99

Turn on : 25.6854

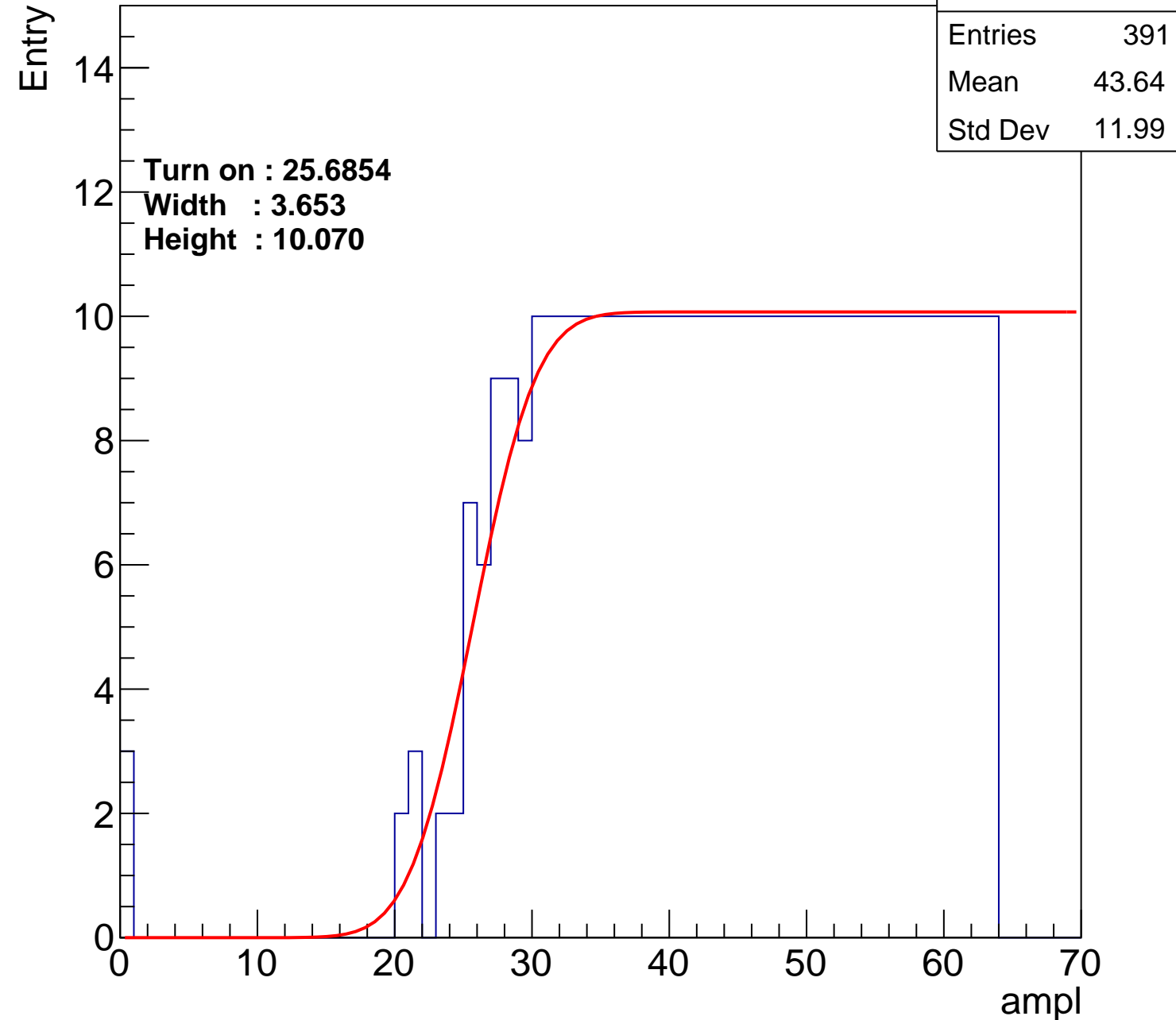
Width : 3.653

Height : 10.070

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch59

calib_packv5_042523_0143.root, FC#0, port D2

Entries	377
Mean	44.36
Std Dev	11.61

Turn on : 27.7389

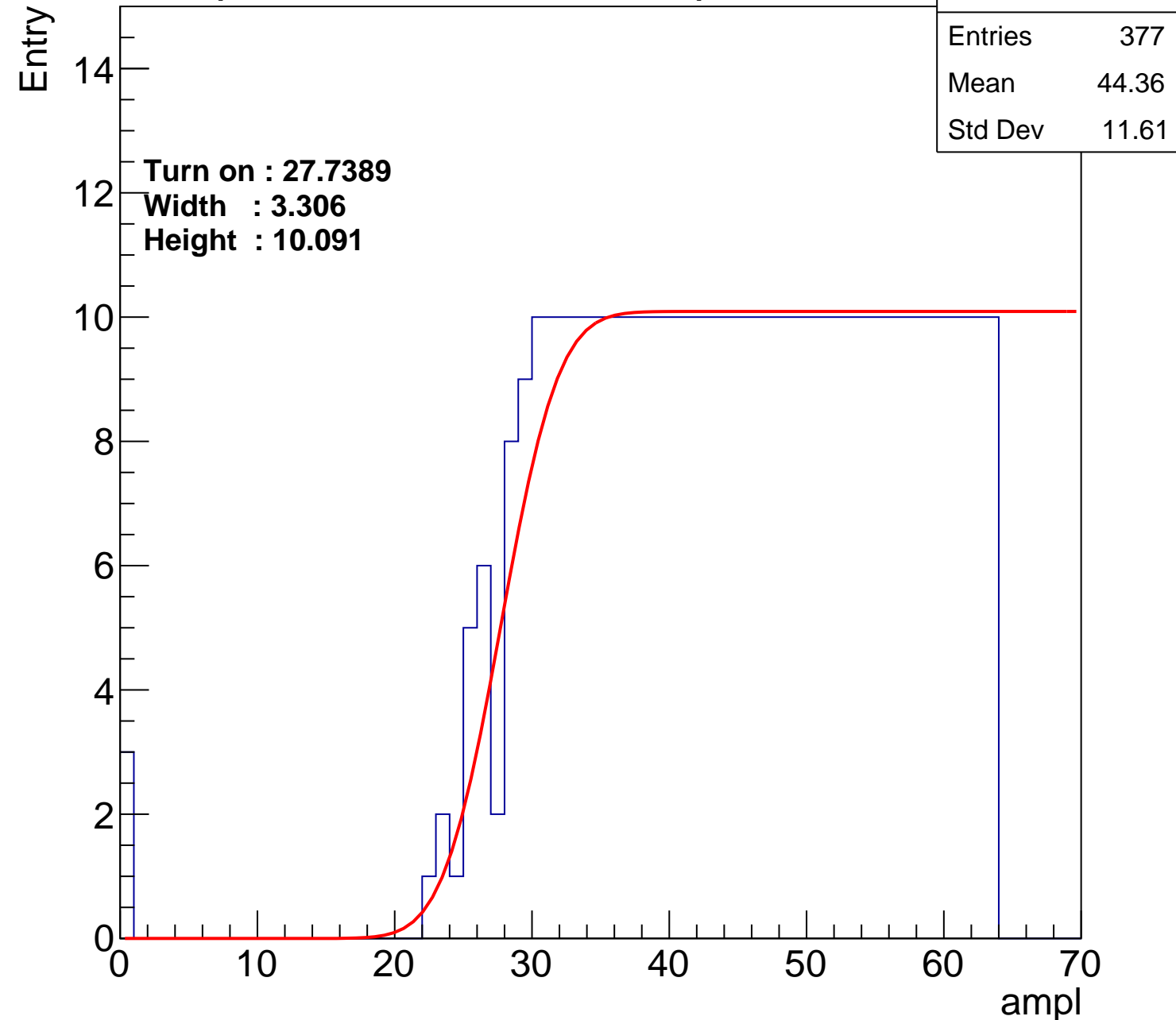
Width : 3.306

Height : 10.091

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch60

calib_packv5_042523_0143.root, FC#0, port D2

Entries	376
Mean	44.51
Std Dev	11.33

Turn on : 25.6977

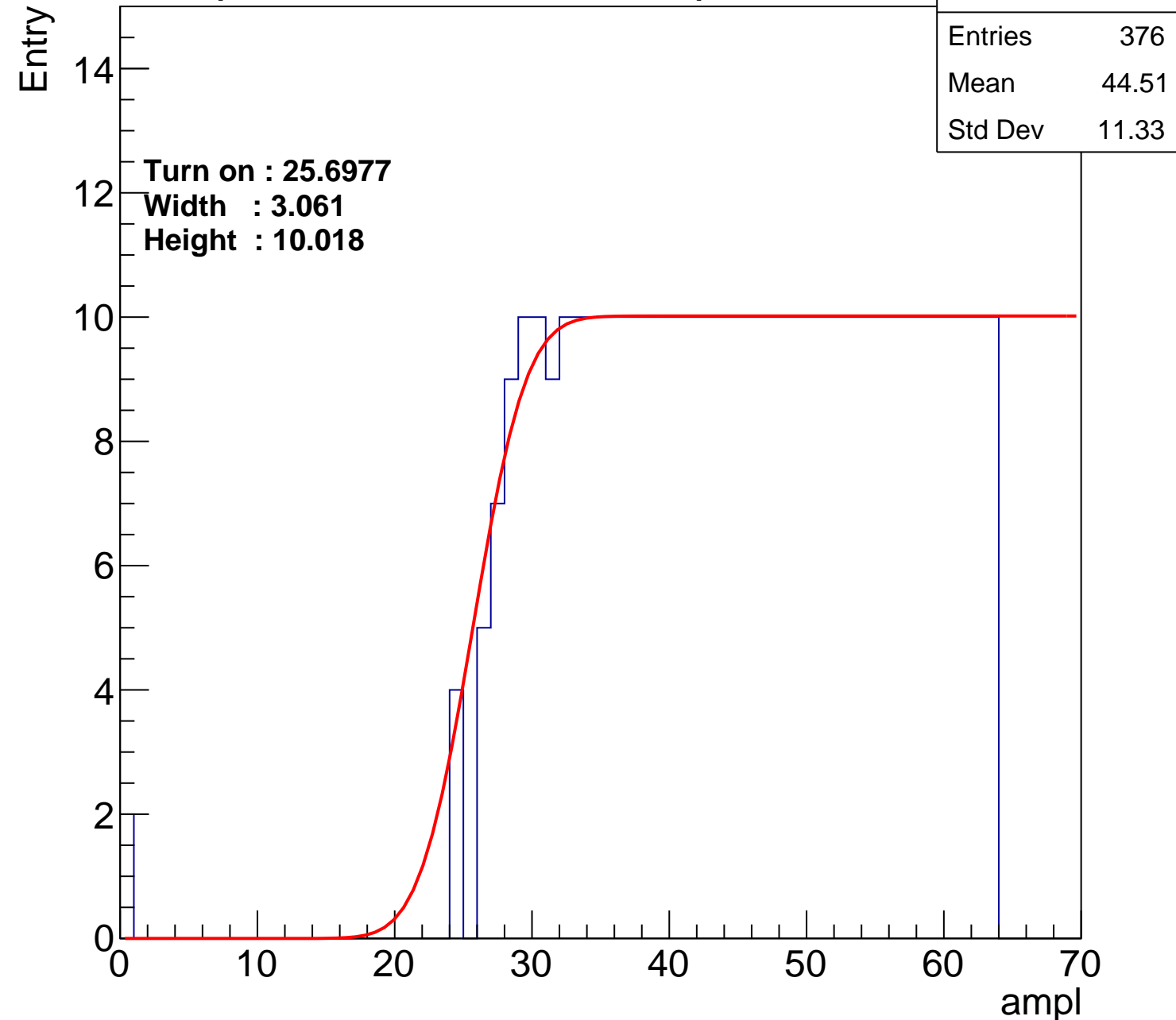
Width : 3.061

Height : 10.018

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch61

calib_packv5_042523_0143.root, FC#0, port D2

Entries	372
Mean	44.77
Std Dev	11.05

Turn on : 26.6597

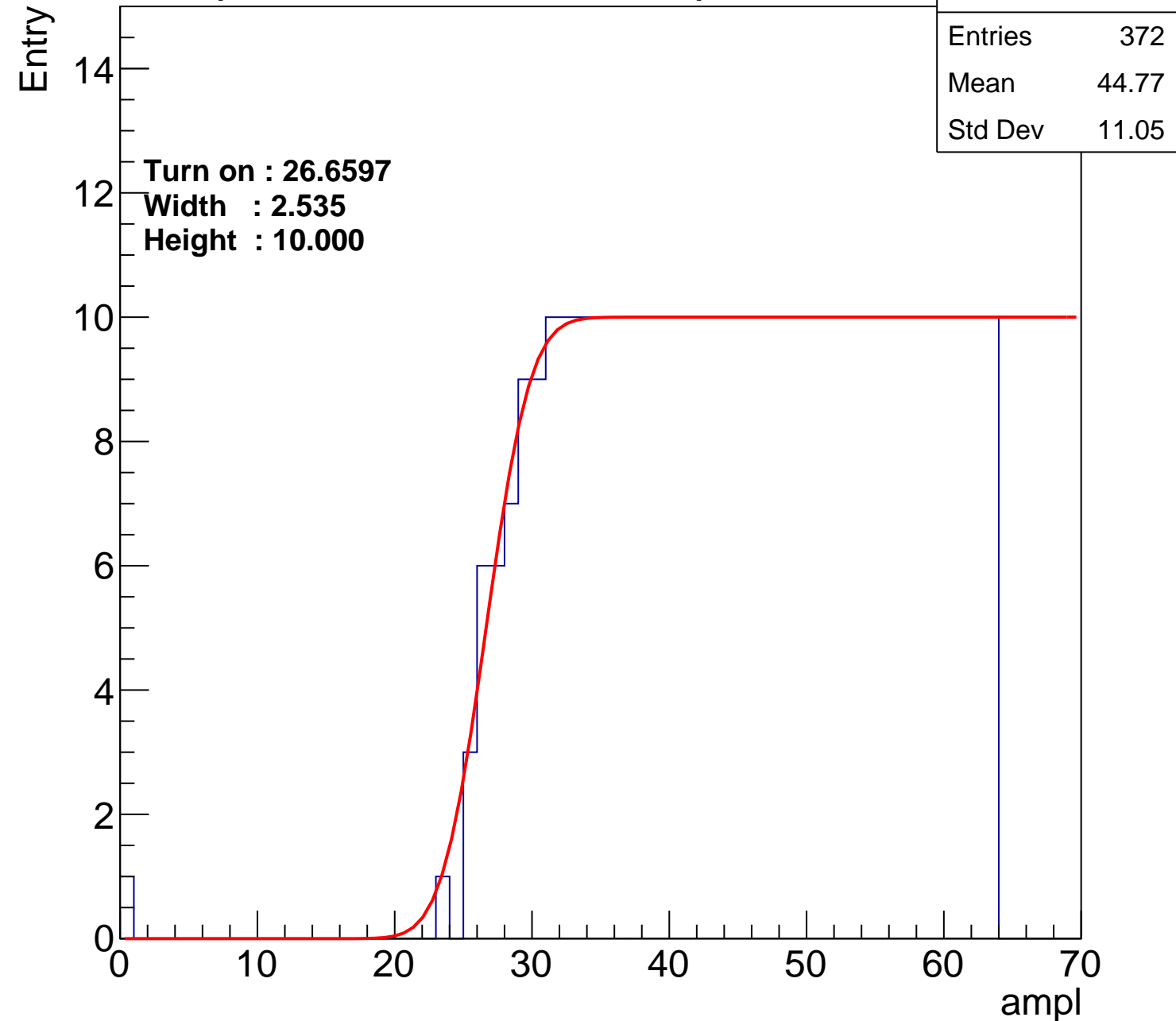
Width : 2.535

Height : 10.000

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch62

calib_packv5_042523_0143.root, FC#0, port D2

Entries	374
Mean	44.41
Std Dev	11.75

Turn on : 26.8429

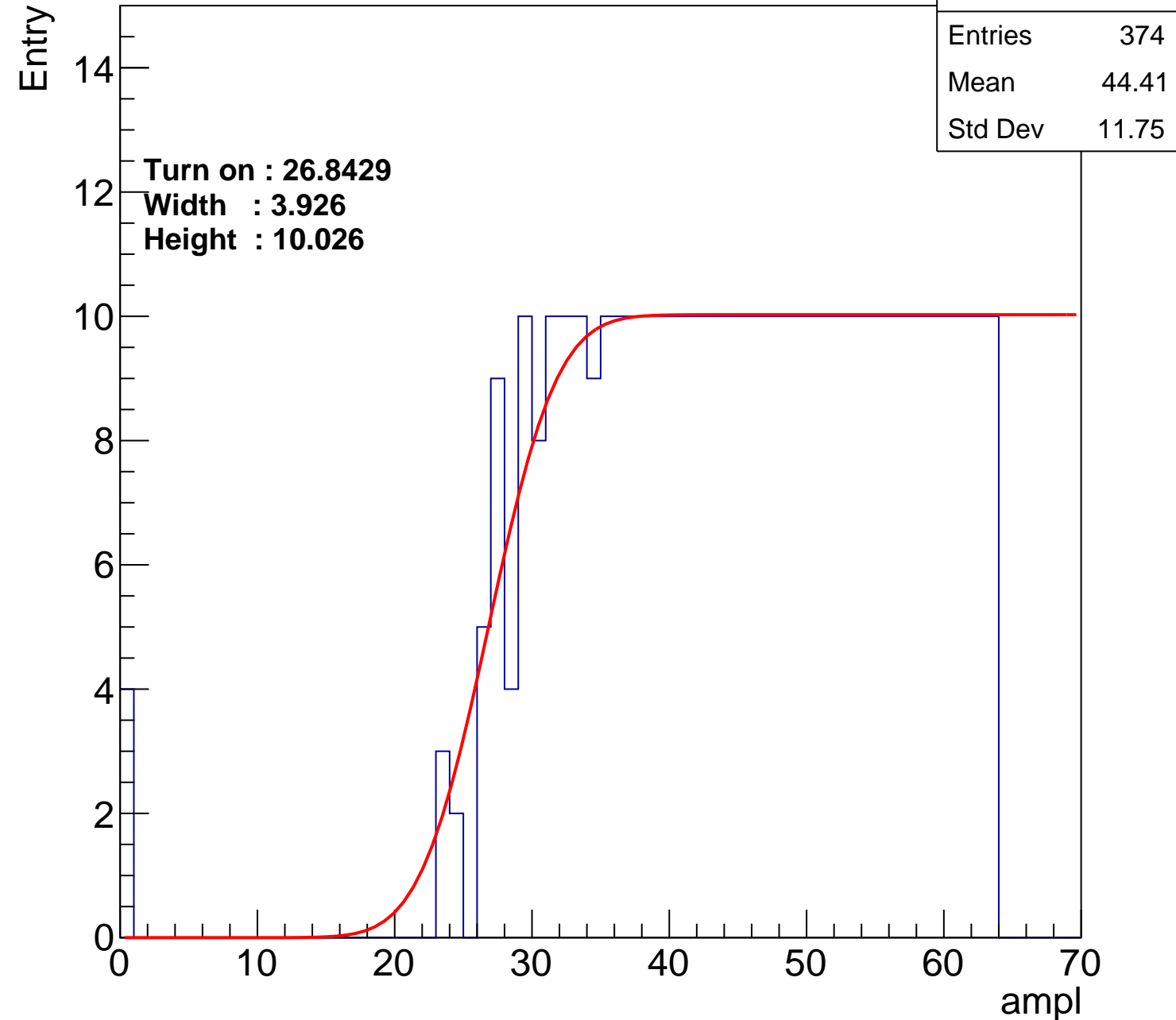
Width : 3.926

Height : 10.026

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch63

calib_packv5_042523_0143.root, FC#0, port D2

Entries	367
Mean	44.75
Std Dev	11.59

Turn on : 27.4912

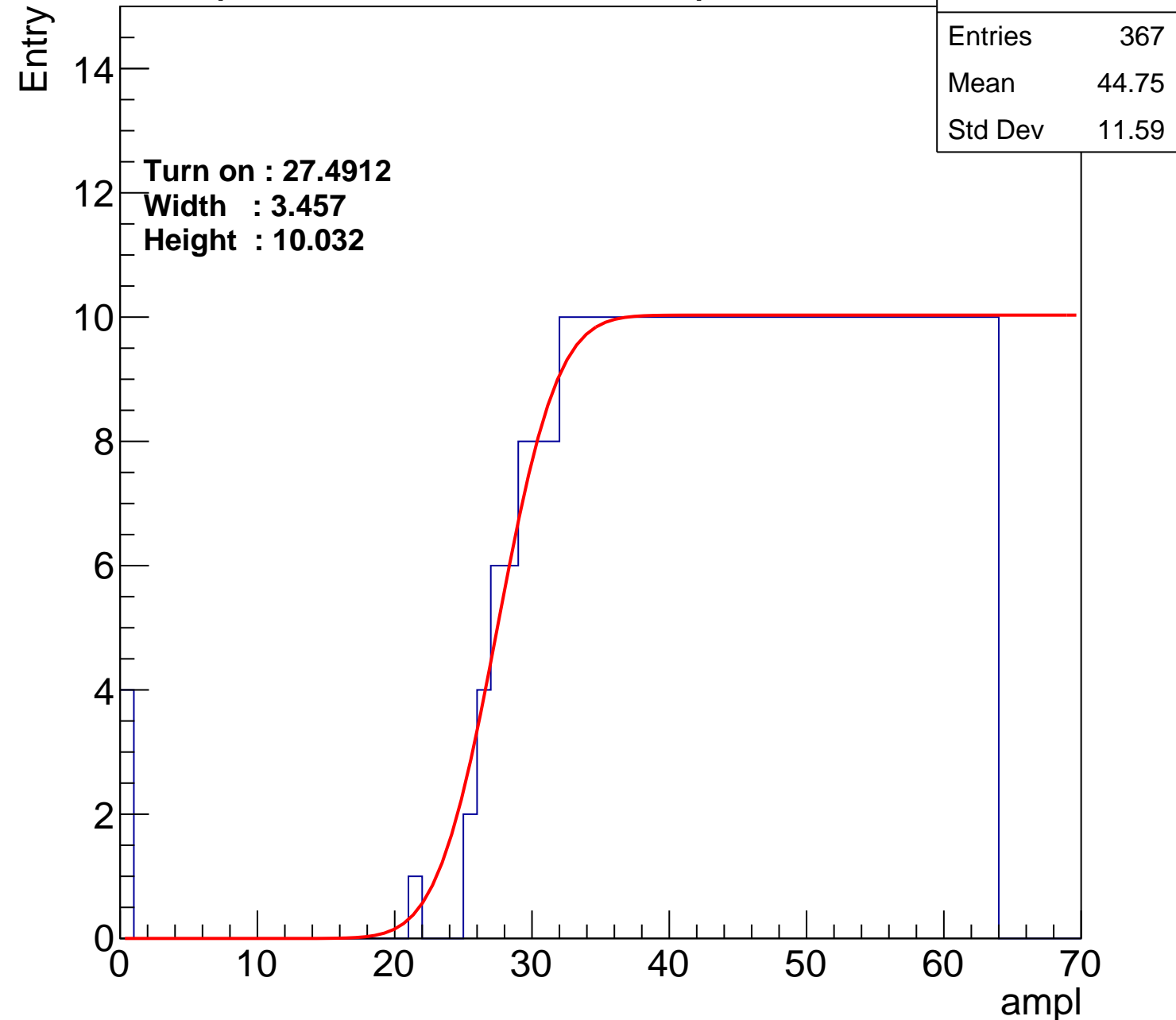
Width : 3.457

Height : 10.032

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch64

calib_packv5_042523_0143.root, FC#0, port D2

Entries	354
Mean	45.49
Std Dev	10.93

Turn on : 28.7122

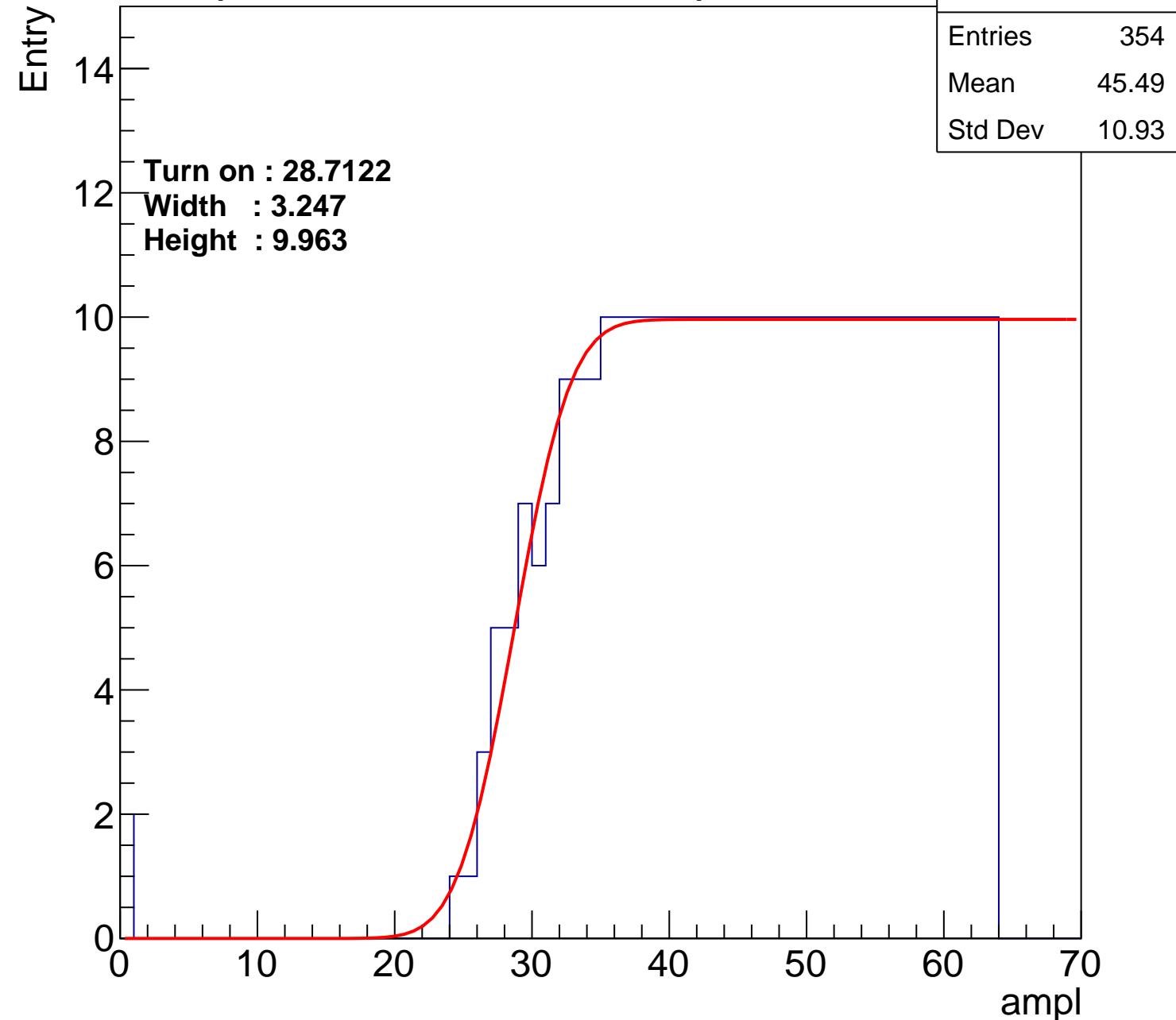
Width : 3.247

Height : 9.963

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch65

calib_packv5_042523_0143.root, FC#0, port D2

Entries	354
Mean	45.49
Std Dev	10.94

Turn on : 29.2208

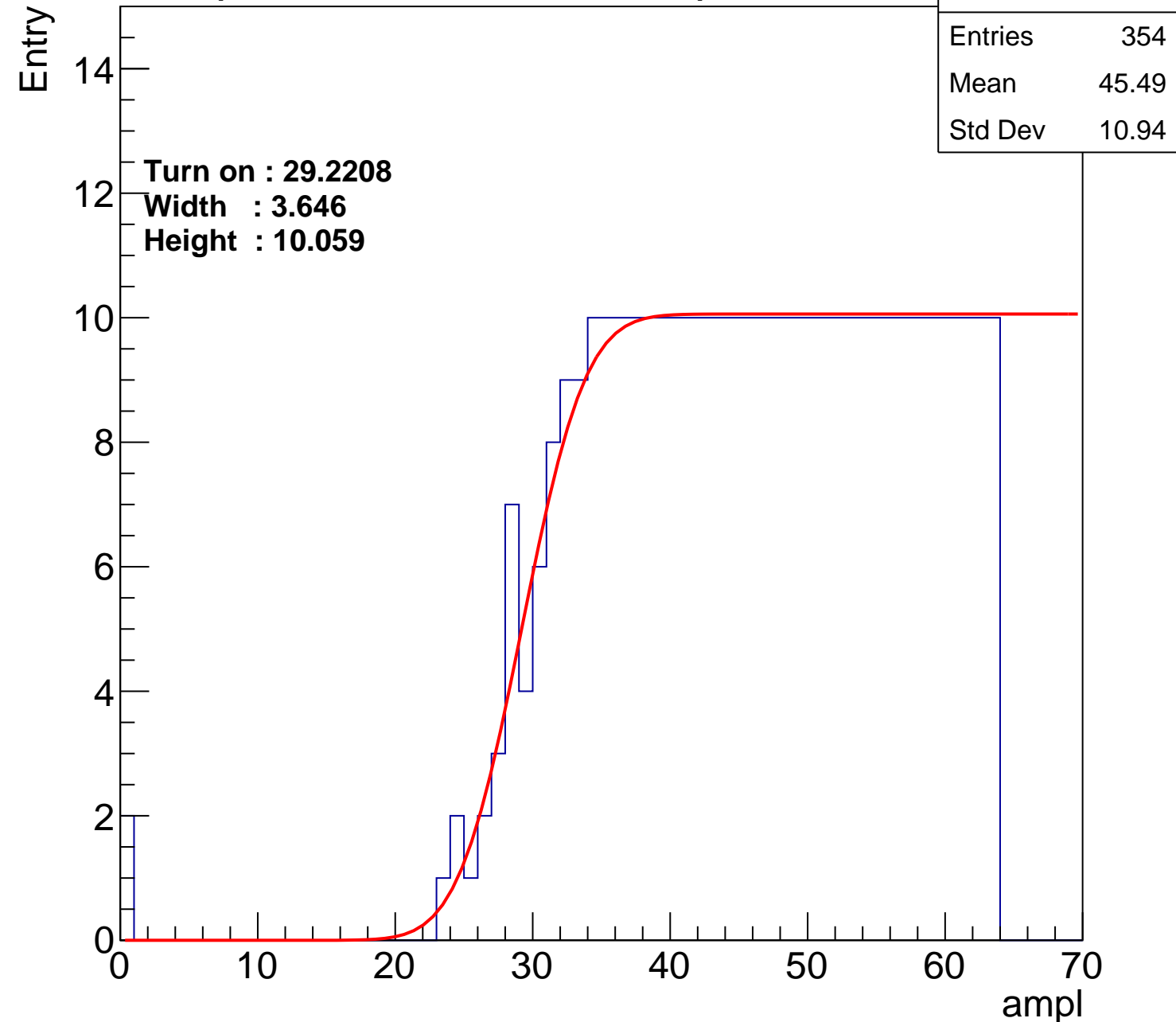
Width : 3.646

Height : 10.059

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch66

calib_packv5_042523_0143.root, FC#0, port D2

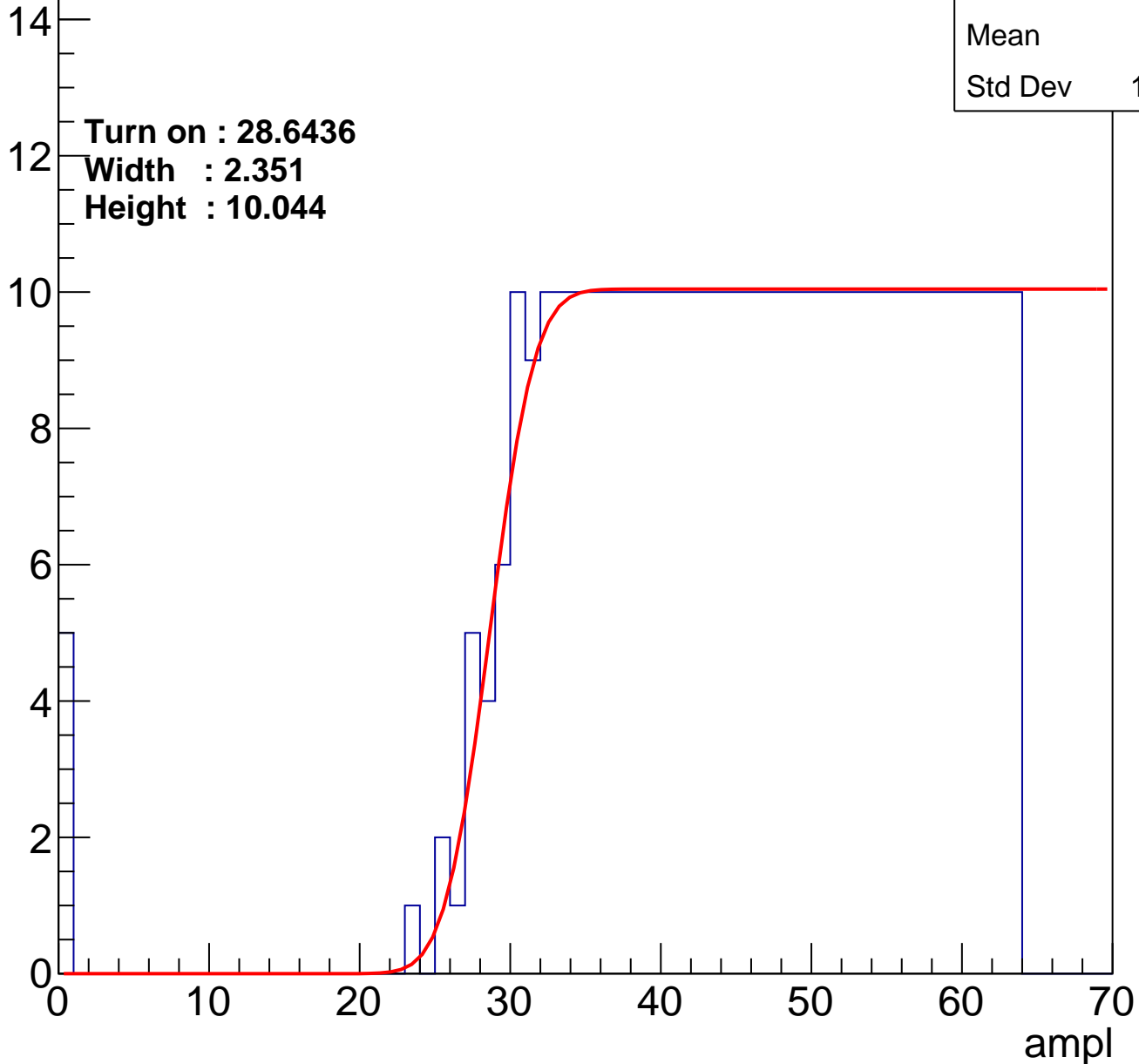
Entries	363
Mean	44.9
Std Dev	11.66

Turn on : 28.6436

Width : 2.351

Height : 10.044

Entry



B1L101S, U19-ch67

calib_packv5_042523_0143.root, FC#0, port D2

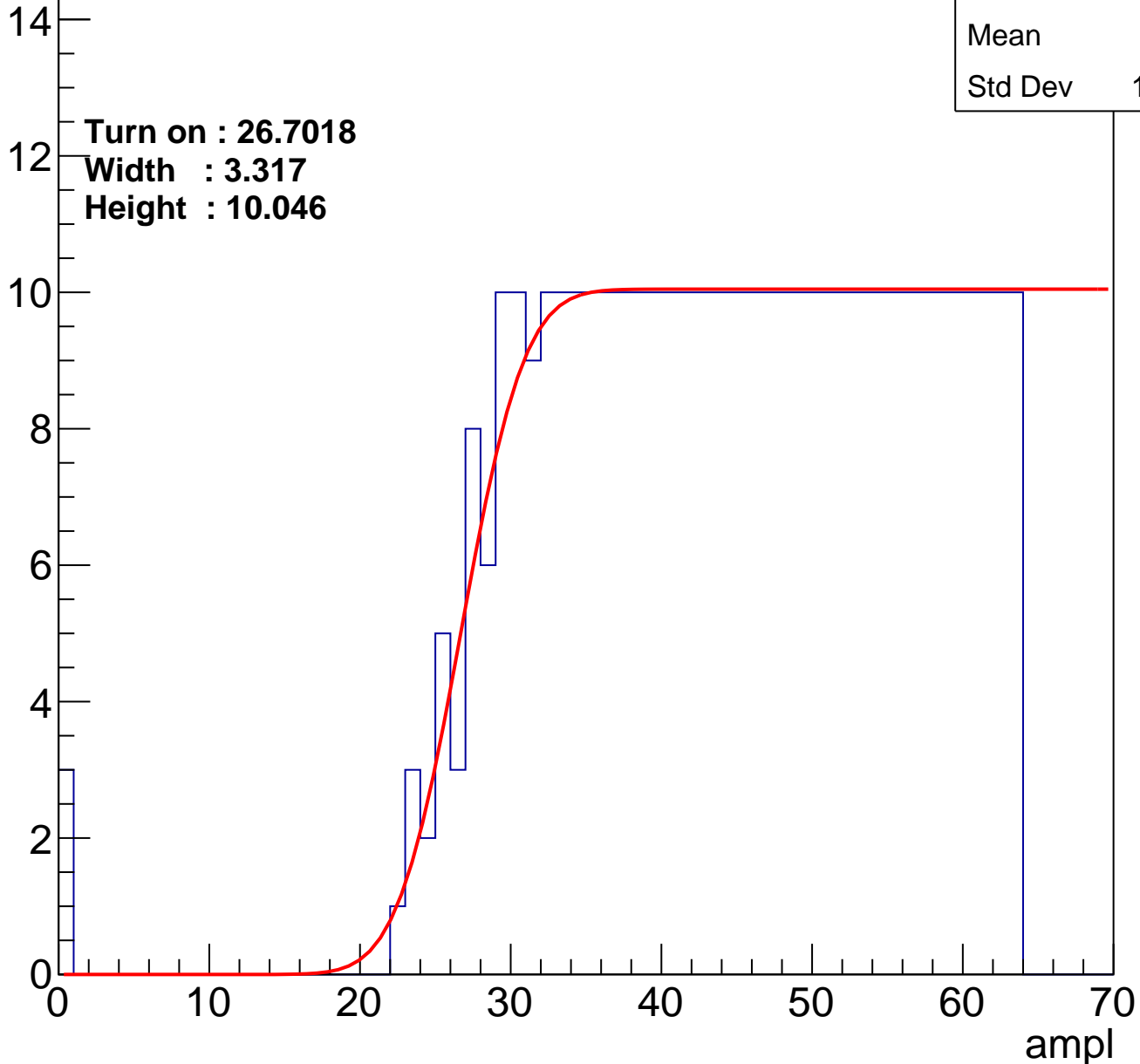
Entries	380
Mean	44.2
Std Dev	11.69

Turn on : 26.7018

Width : 3.317

Height : 10.046

Entry



B1L101S, U19-ch68

calib_packv5_042523_0143.root, FC#0, port D2

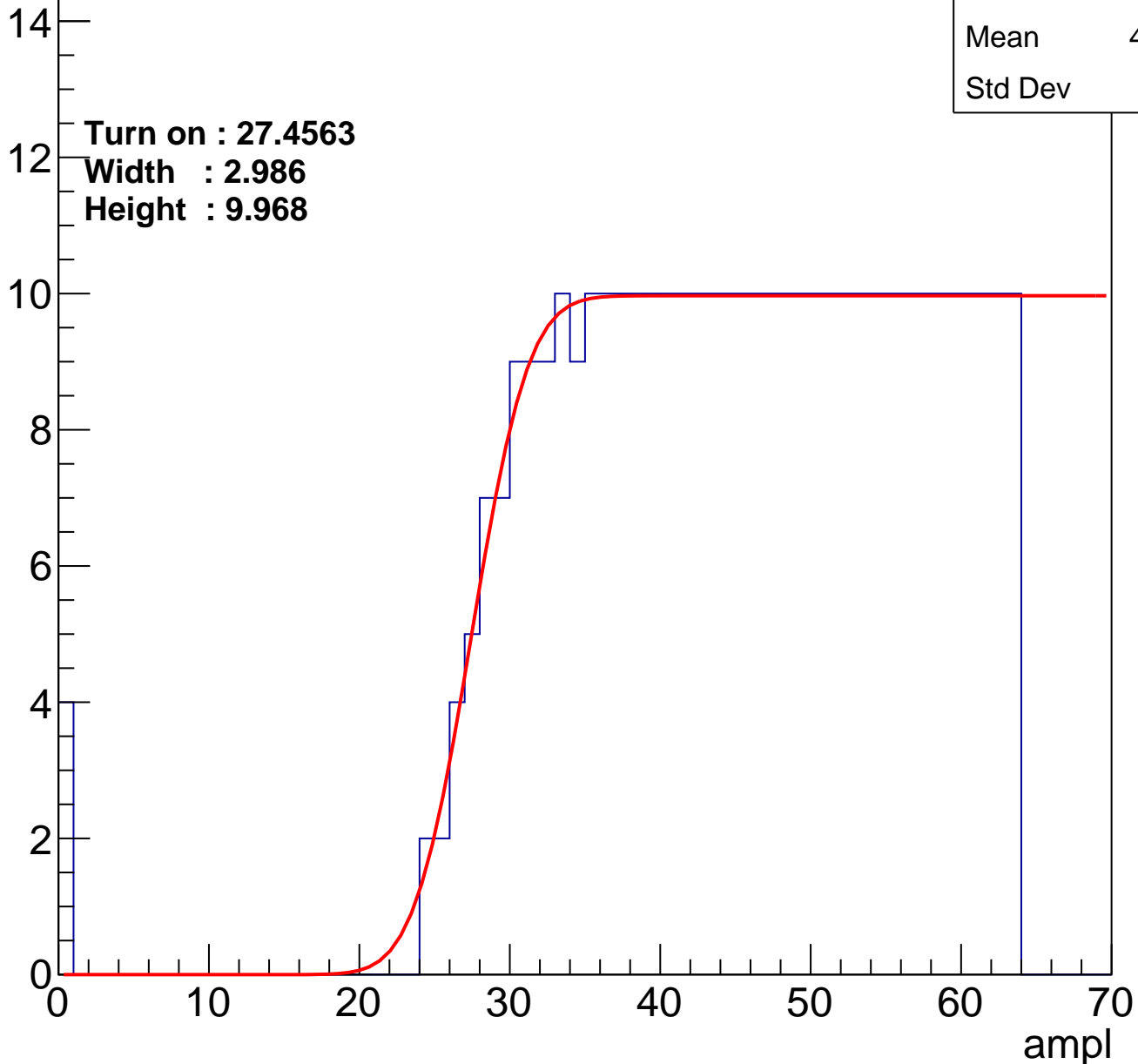
Entries	367
Mean	44.74
Std Dev	11.6

Turn on : 27.4563

Width : 2.986

Height : 9.968

Entry



B1L101S, U19-ch69

calib_packv5_042523_0143.root, FC#0, port D2

Entries	332
Mean	46.76
Std Dev	9.959

Turn on : 30.8908

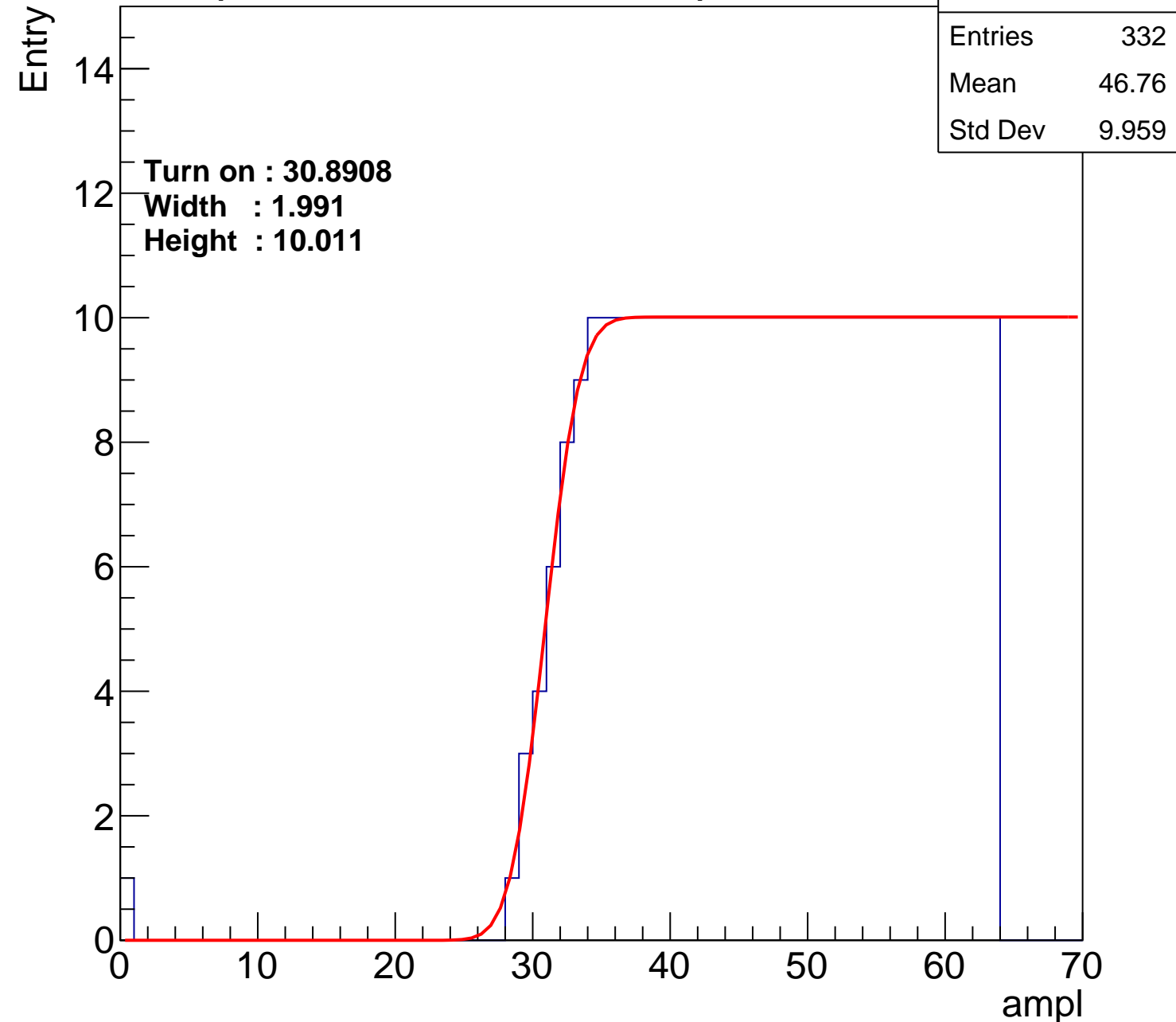
Width : 1.991

Height : 10.011

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch70

calib_packv5_042523_0143.root, FC#0, port D2

Entries	376
Mean	44.39
Std Dev	11.61

Turn on : 27.0064

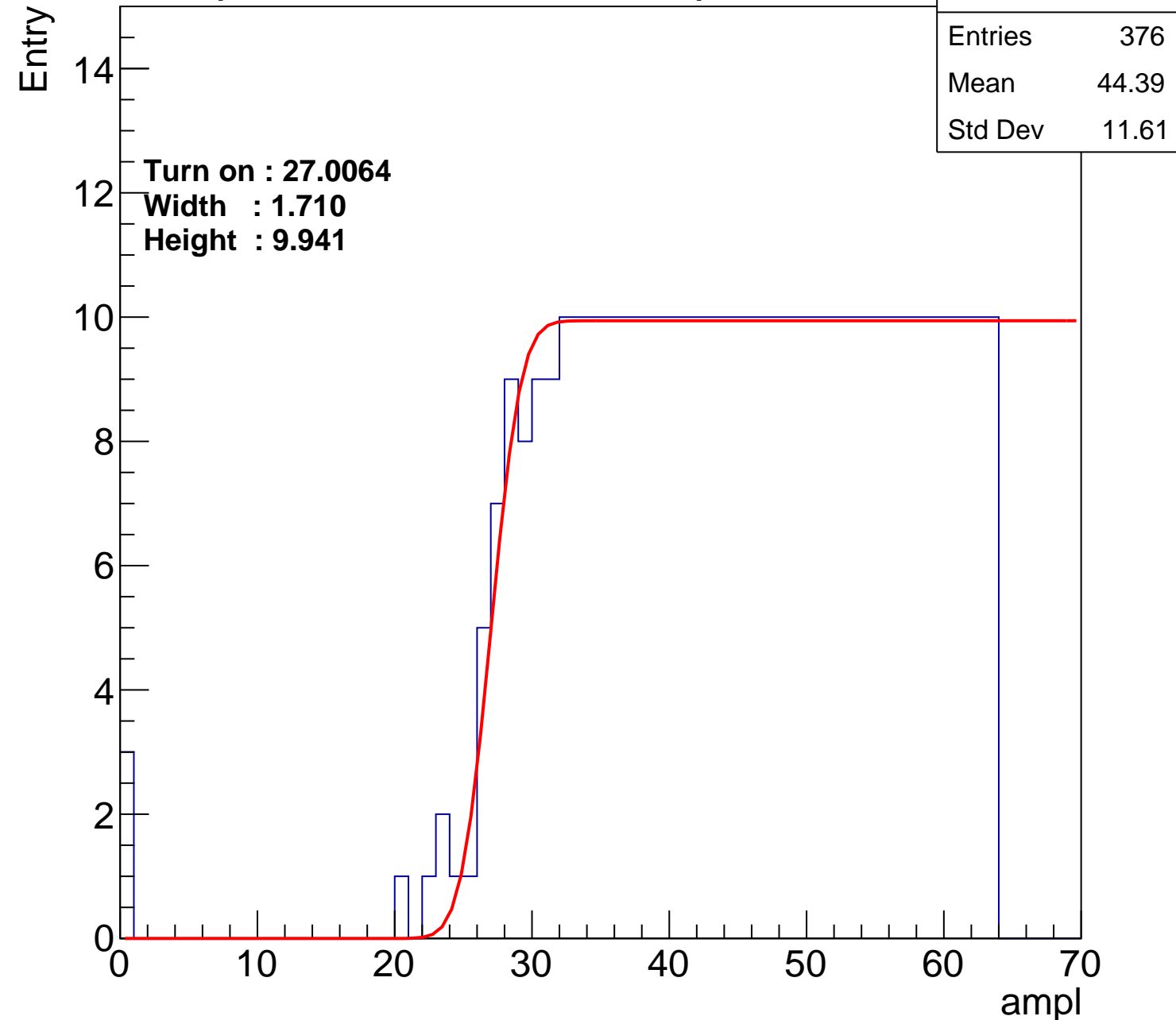
Width : 1.710

Height : 9.941

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch71

calib_packv5_042523_0143.root, FC#0, port D2

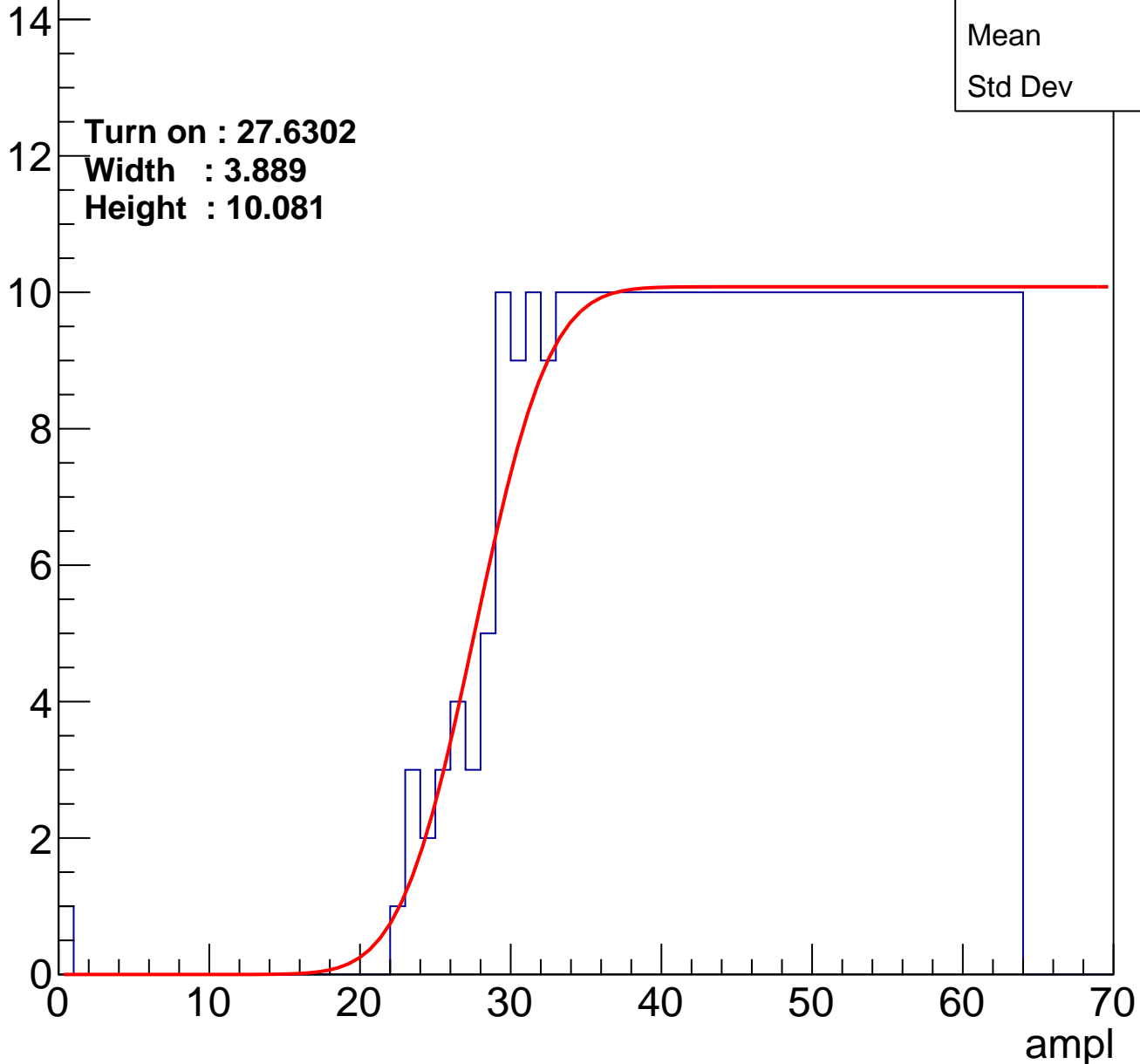
Entries	370
Mean	44.8
Std Dev	11.1

Turn on : 27.6302

Width : 3.889

Height : 10.081

Entry



B1L101S, U19-ch72

calib_packv5_042523_0143.root, FC#0, port D2

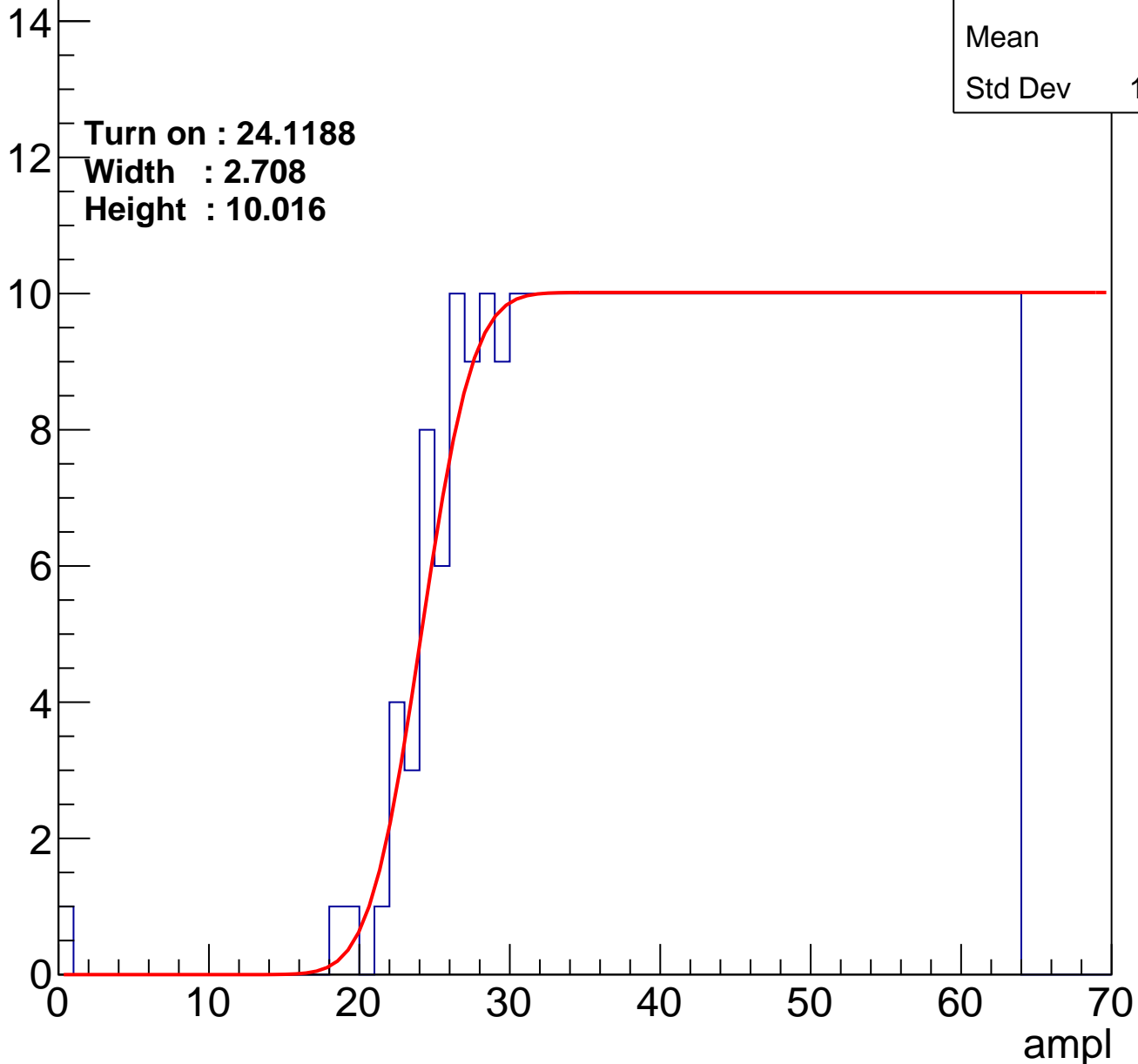
Entries	403
Mean	43.2
Std Dev	11.94

Turn on : 24.1188

Width : 2.708

Height : 10.016

Entry



B1L101S, U19-ch73

calib_packv5_042523_0143.root, FC#0, port D2

Entries	367
Mean	44.98
Std Dev	10.96

Turn on : 27.1407

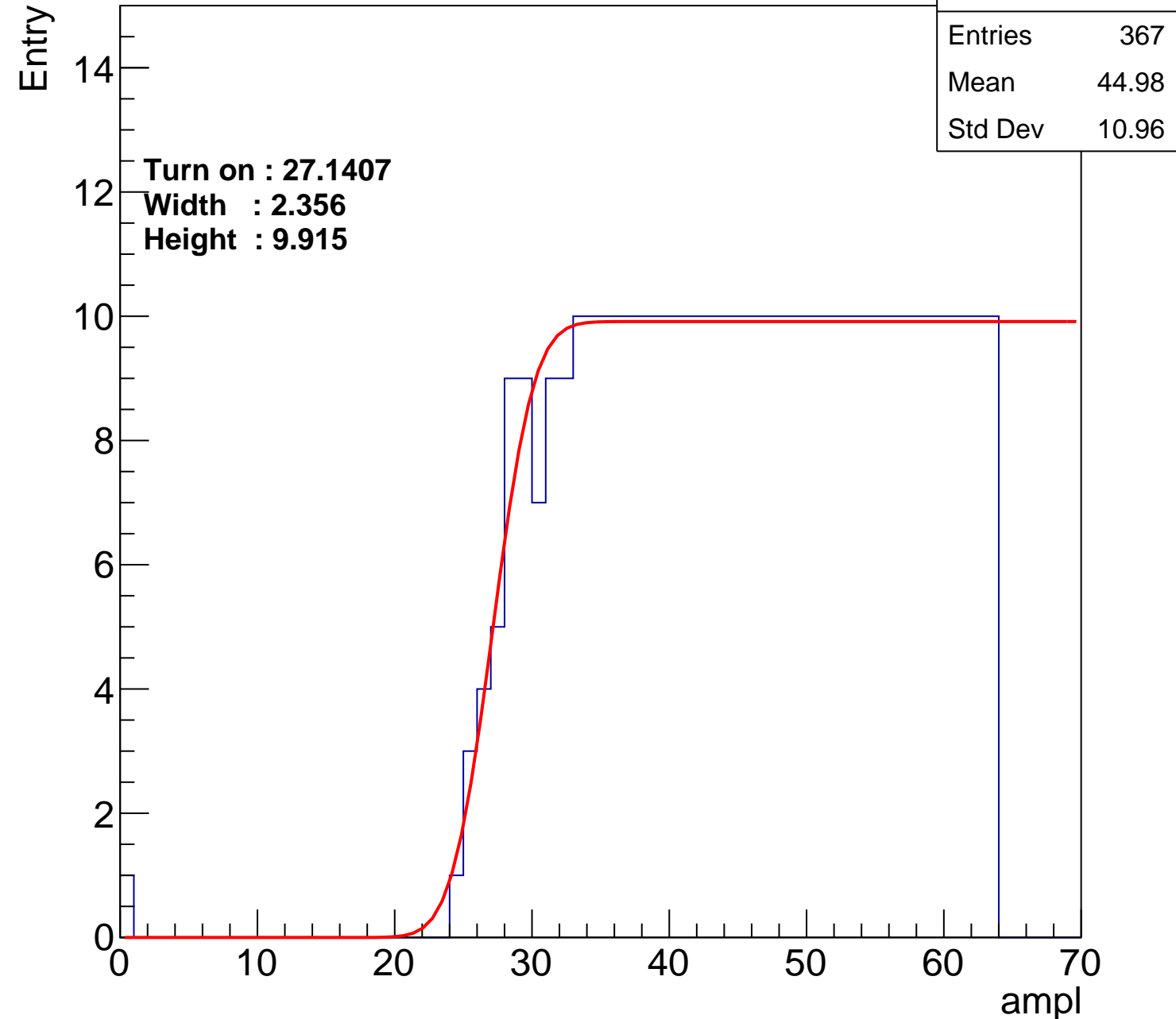
Width : 2.356

Height : 9.915

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch74

calib_packv5_042523_0143.root, FC#0, port D2

Entries	392
Mean	43.67
Std Dev	11.83

Turn on : 25.2408

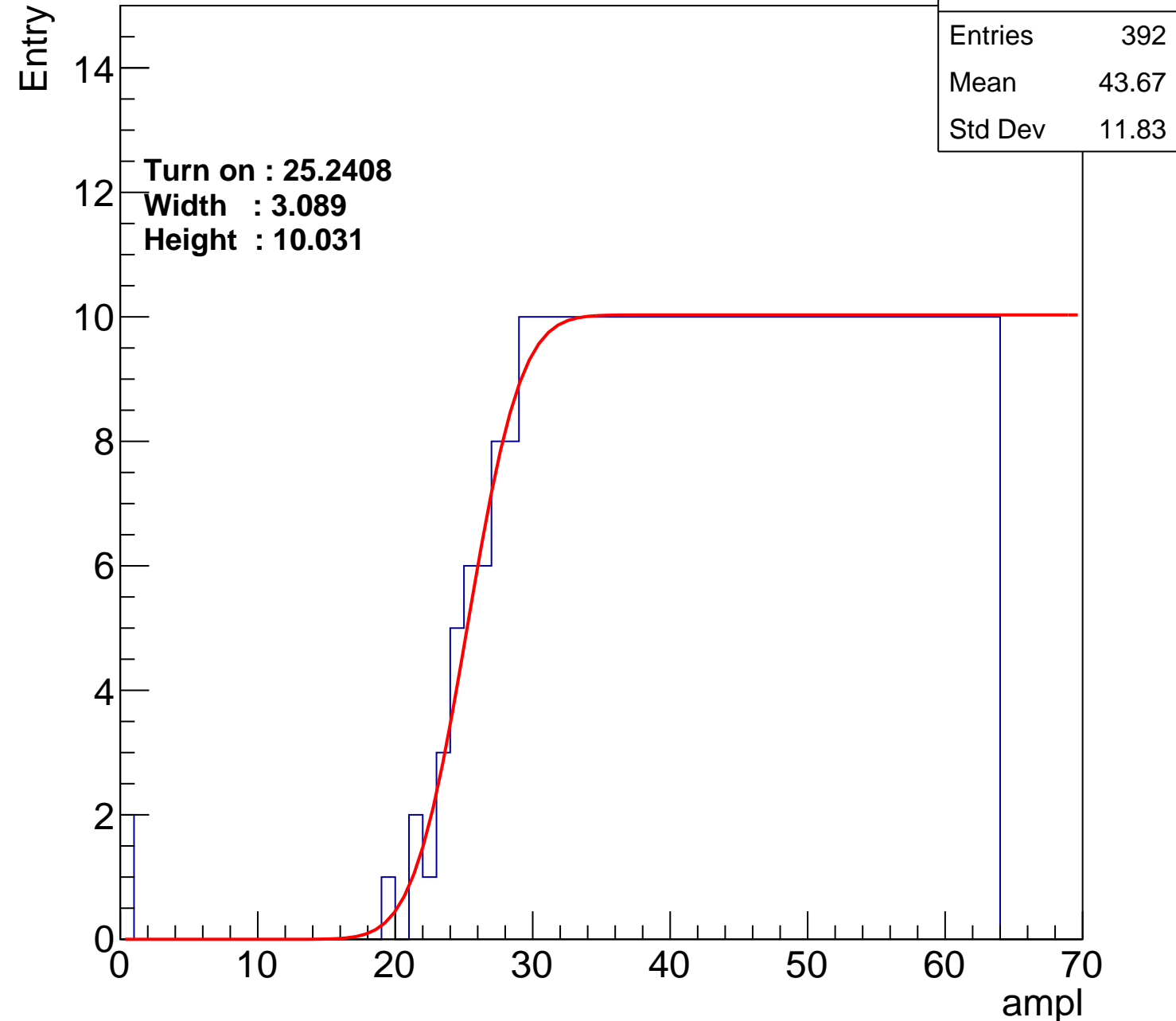
Width : 3.089

Height : 10.031

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch75

calib_packv5_042523_0143.root, FC#0, port D2

Entries	372
Mean	44.46
Std Dev	11.86

Turn on : 27.1492

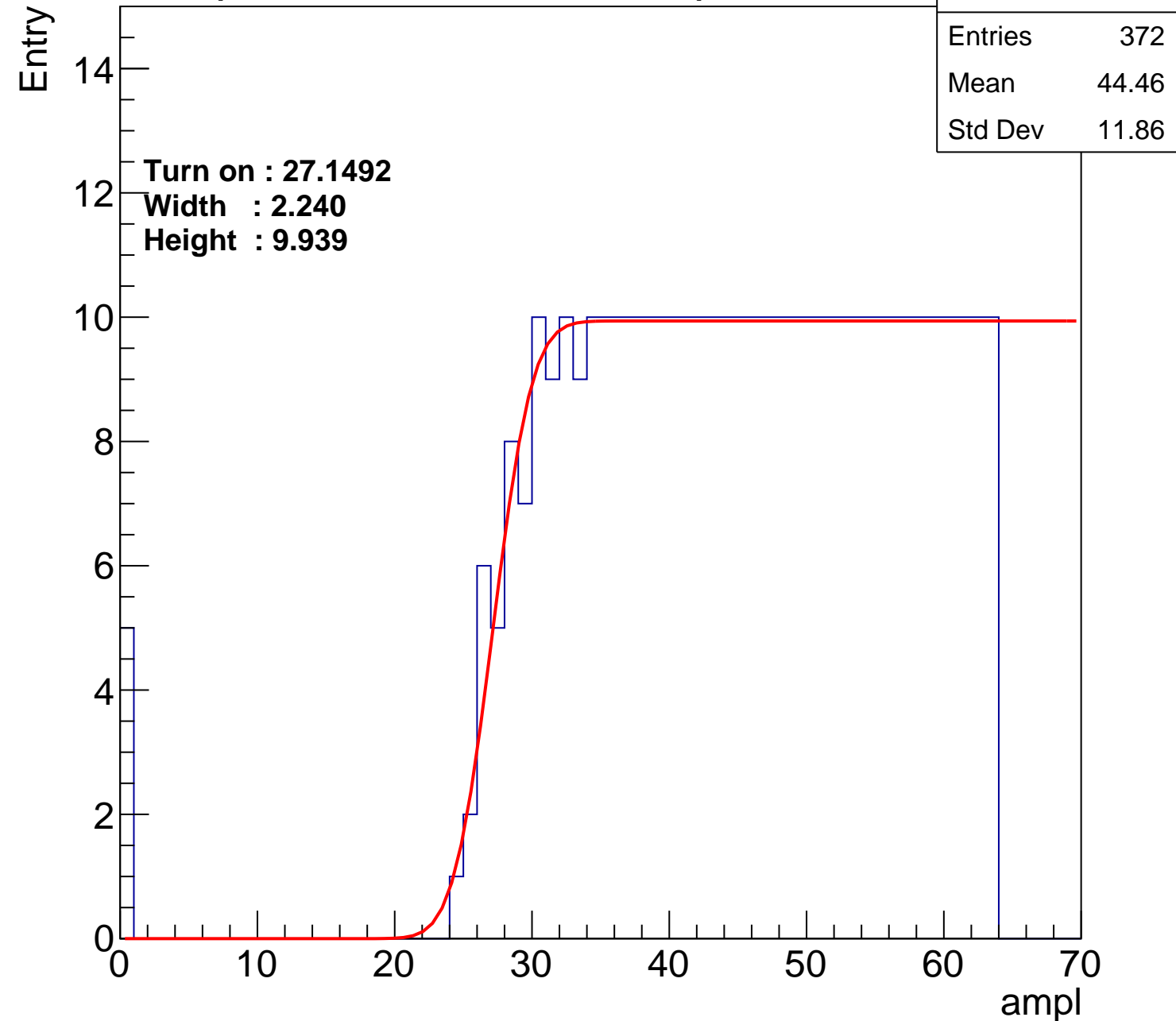
Width : 2.240

Height : 9.939

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch76

calib_packv5_042523_0143.root, FC#0, port D2

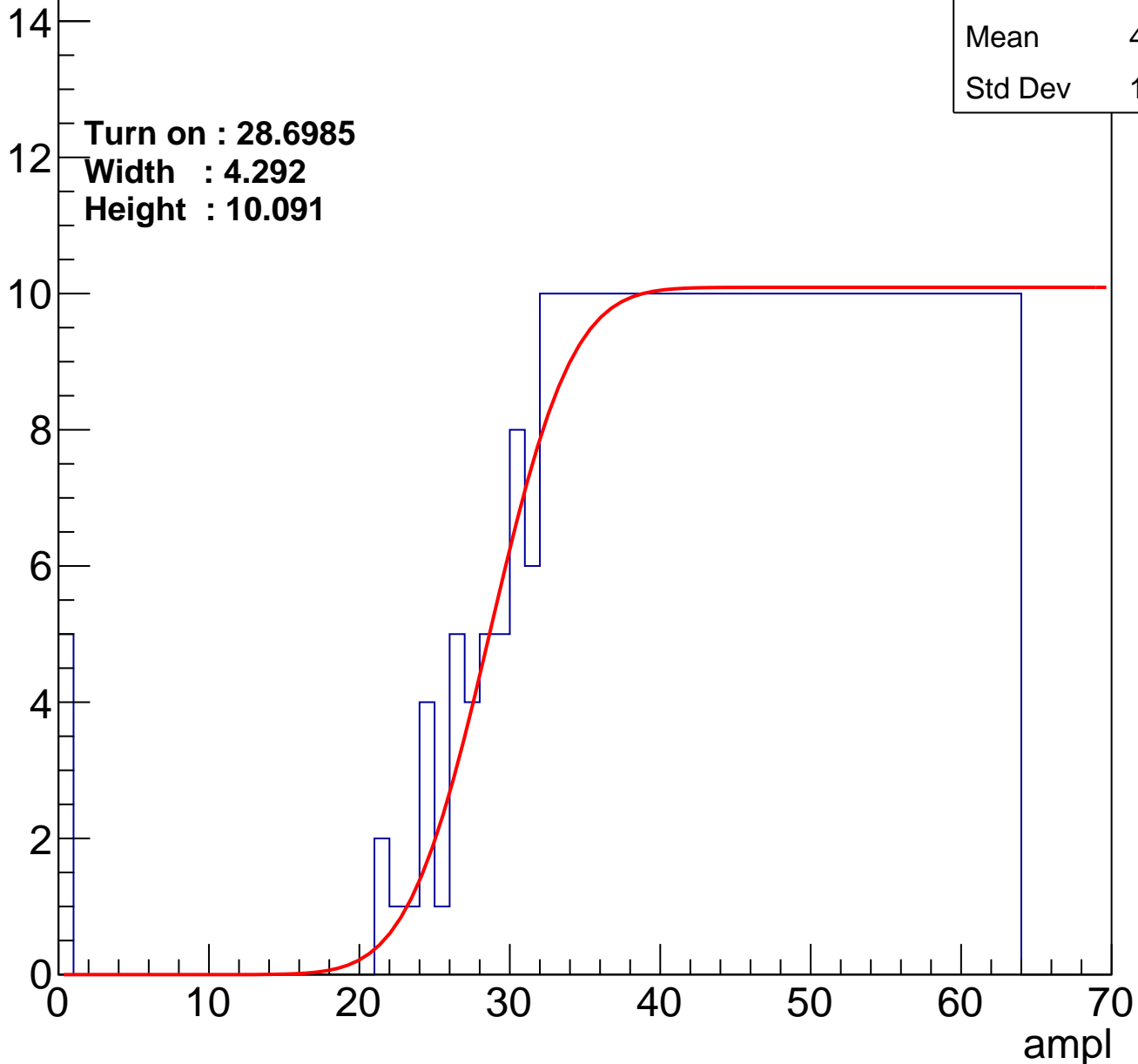
Entries	367
Mean	44.57
Std Dev	11.96

Turn on : 28.6985

Width : 4.292

Height : 10.091

Entry



B1L101S, U19-ch77

calib_packv5_042523_0143.root, FC#0, port D2

Entries	376
Mean	44.23
Std Dev	12

Turn on : 27.2766

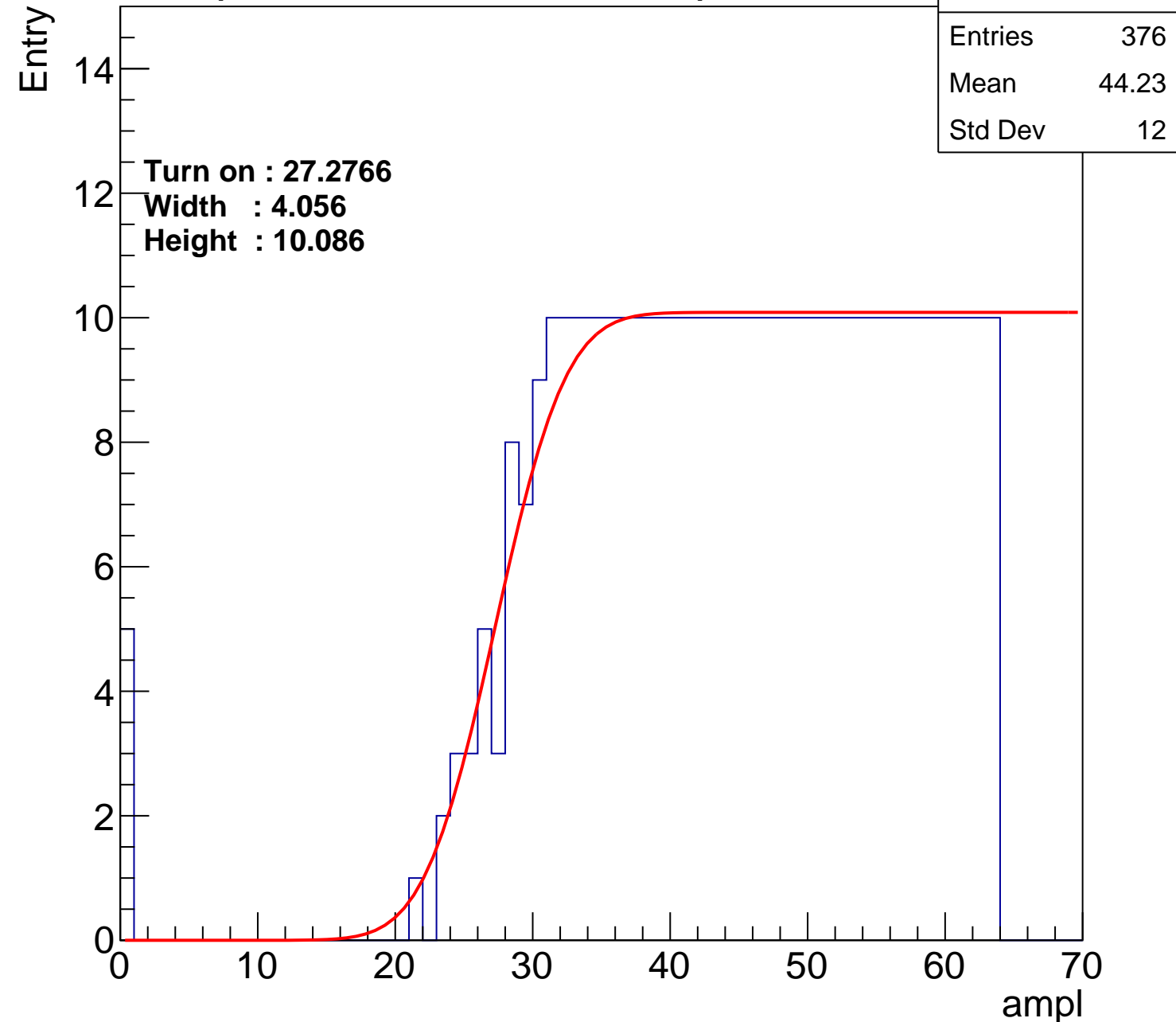
Width : 4.056

Height : 10.086

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch78

calib_packv5_042523_0143.root, FC#0, port D2

Entries	365
Mean	44.84
Std Dev	11.56

Turn on : 26.9756

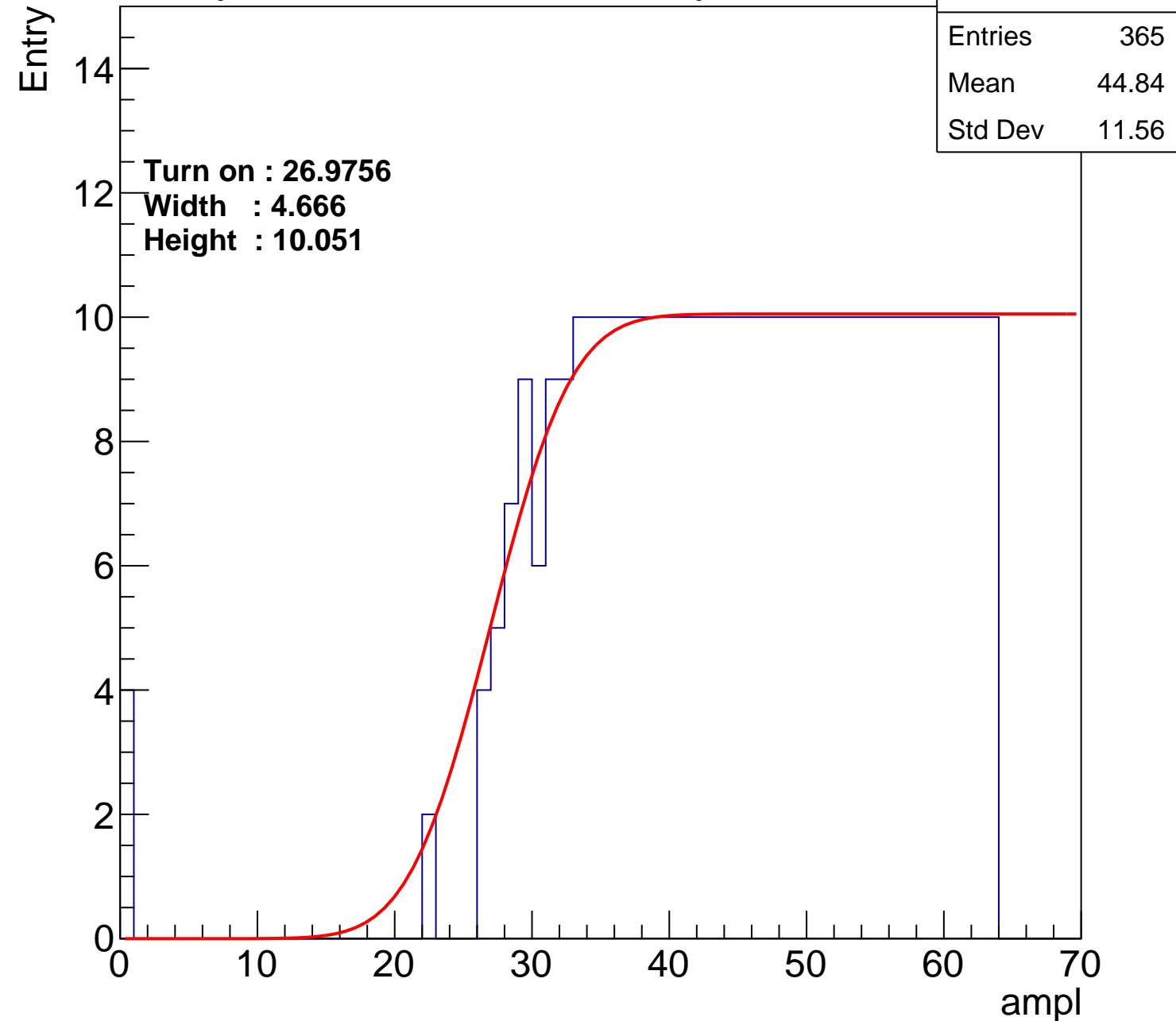
Width : 4.666

Height : 10.051

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch79

calib_packv5_042523_0143.root, FC#0, port D2

Entries	363
Mean	45.05
Std Dev	11.16

Turn on : 28.1901

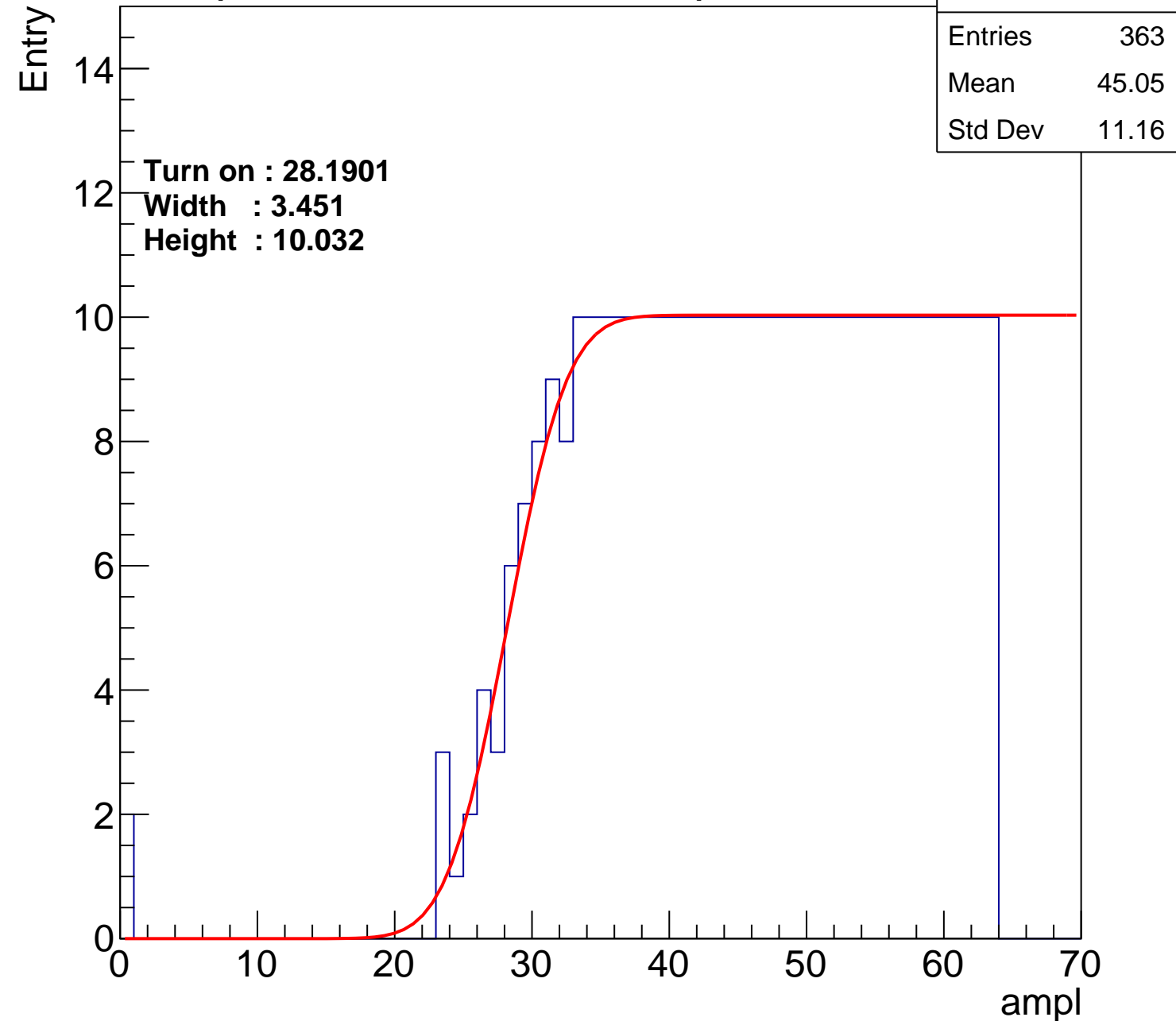
Width : 3.451

Height : 10.032

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch80

calib_packv5_042523_0143.root, FC#0, port D2

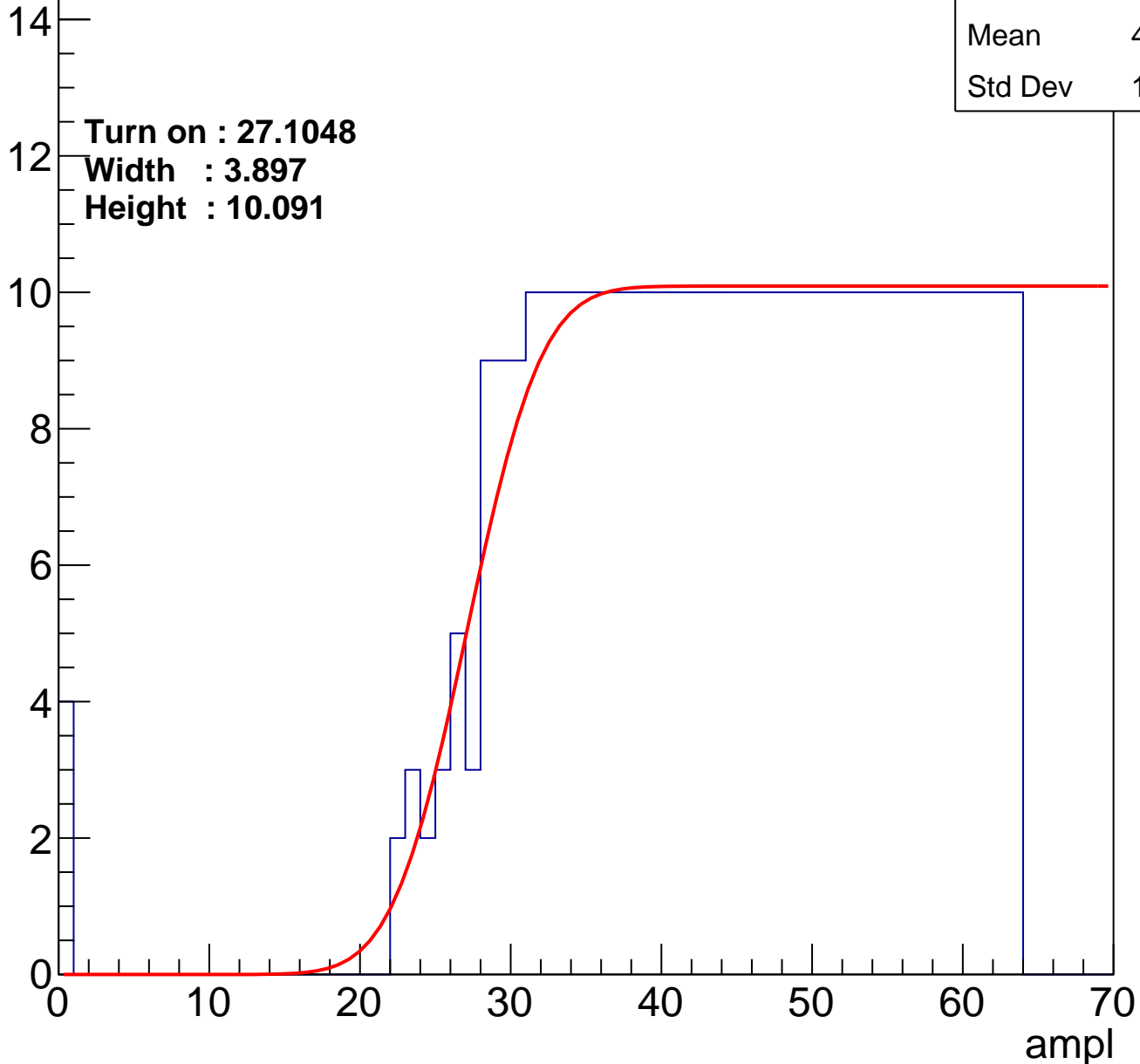
Entries	379
Mean	44.17
Std Dev	11.87

Turn on : 27.1048

Width : 3.897

Height : 10.091

Entry



B1L101S, U19-ch81

calib_packv5_042523_0143.root, FC#0, port D2

Entries	387
Mean	43.76
Std Dev	12.07

Turn on : 25.8864

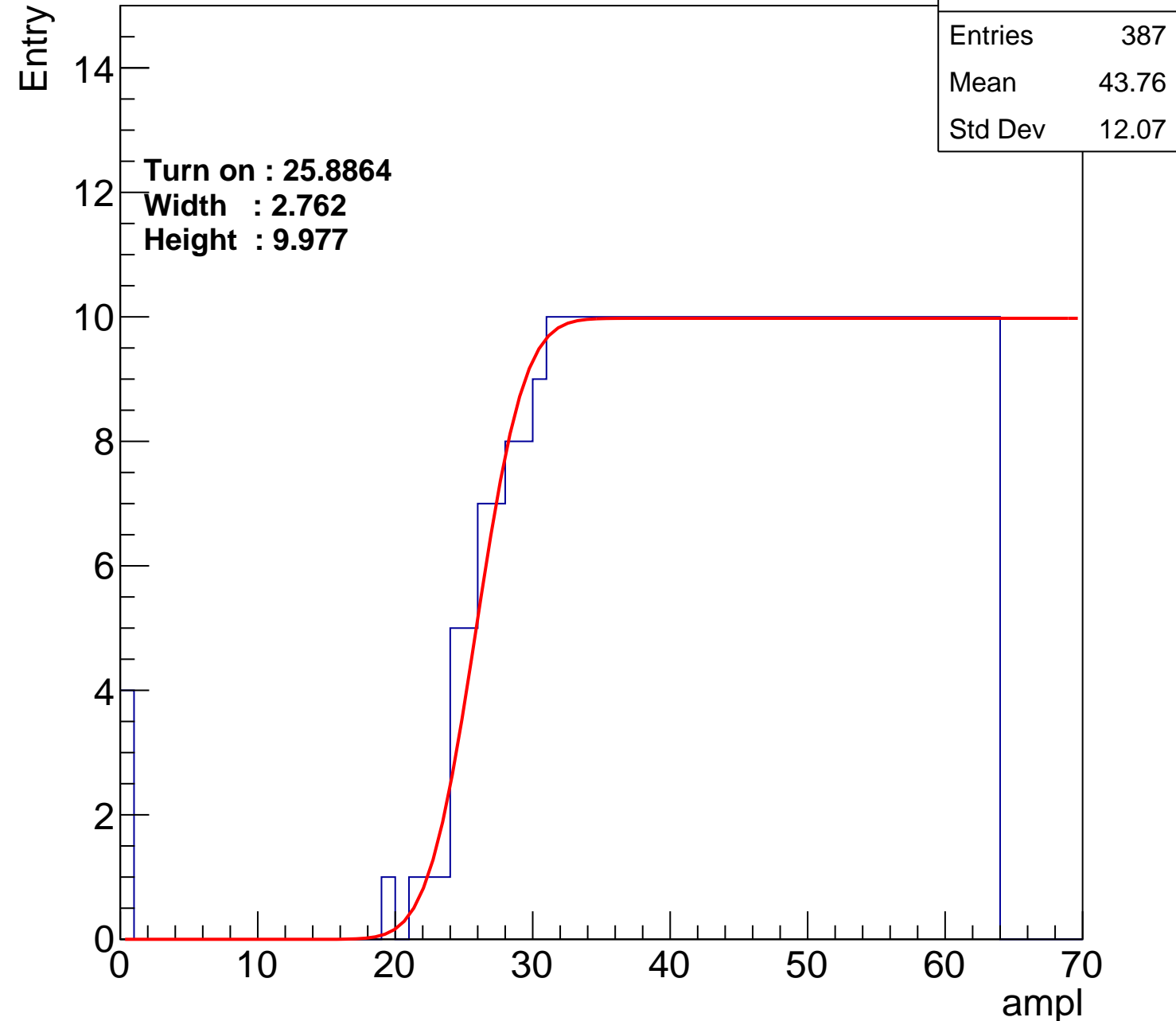
Width : 2.762

Height : 9.977

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch82

calib_packv5_042523_0143.root, FC#0, port D2

Entries	390
Mean	43.64
Std Dev	12.11

Turn on : 25.5263

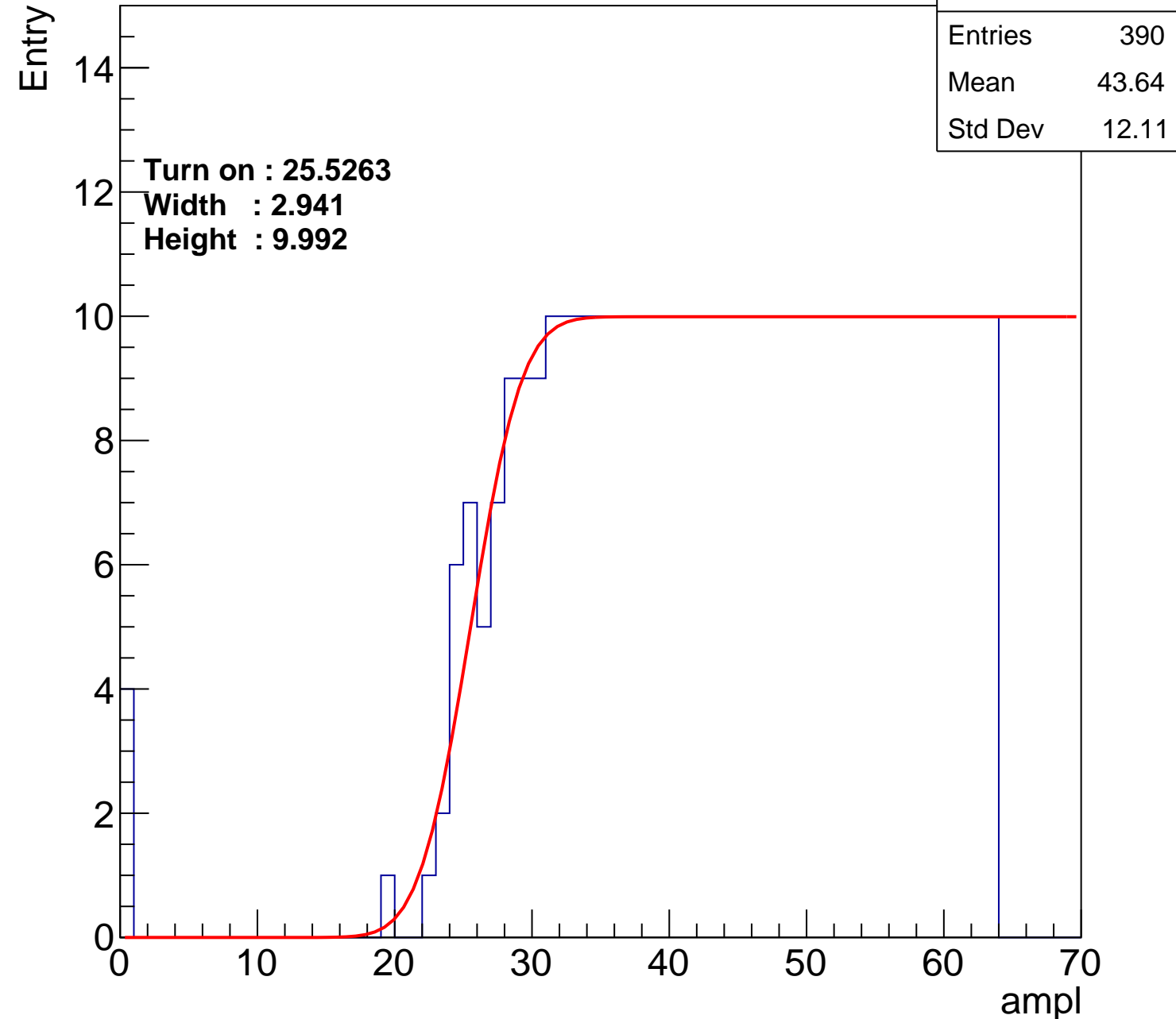
Width : 2.941

Height : 9.992

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch83

calib_packv5_042523_0143.root, FC#0, port D2

Entries	369
Mean	44.74
Std Dev	11.42

Turn on : 27.4363

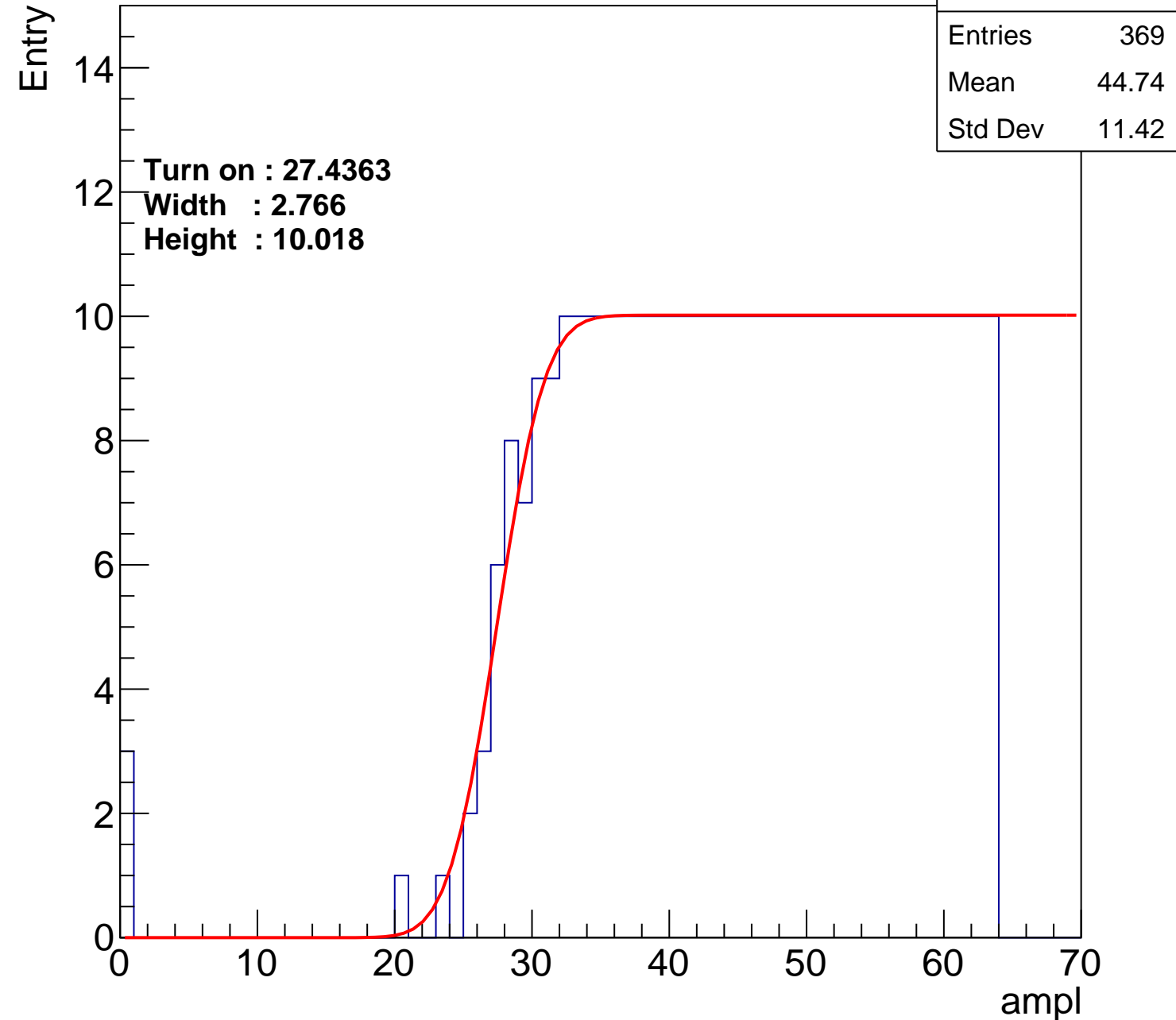
Width : 2.766

Height : 10.018

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch84

calib_packv5_042523_0143.root, FC#0, port D2

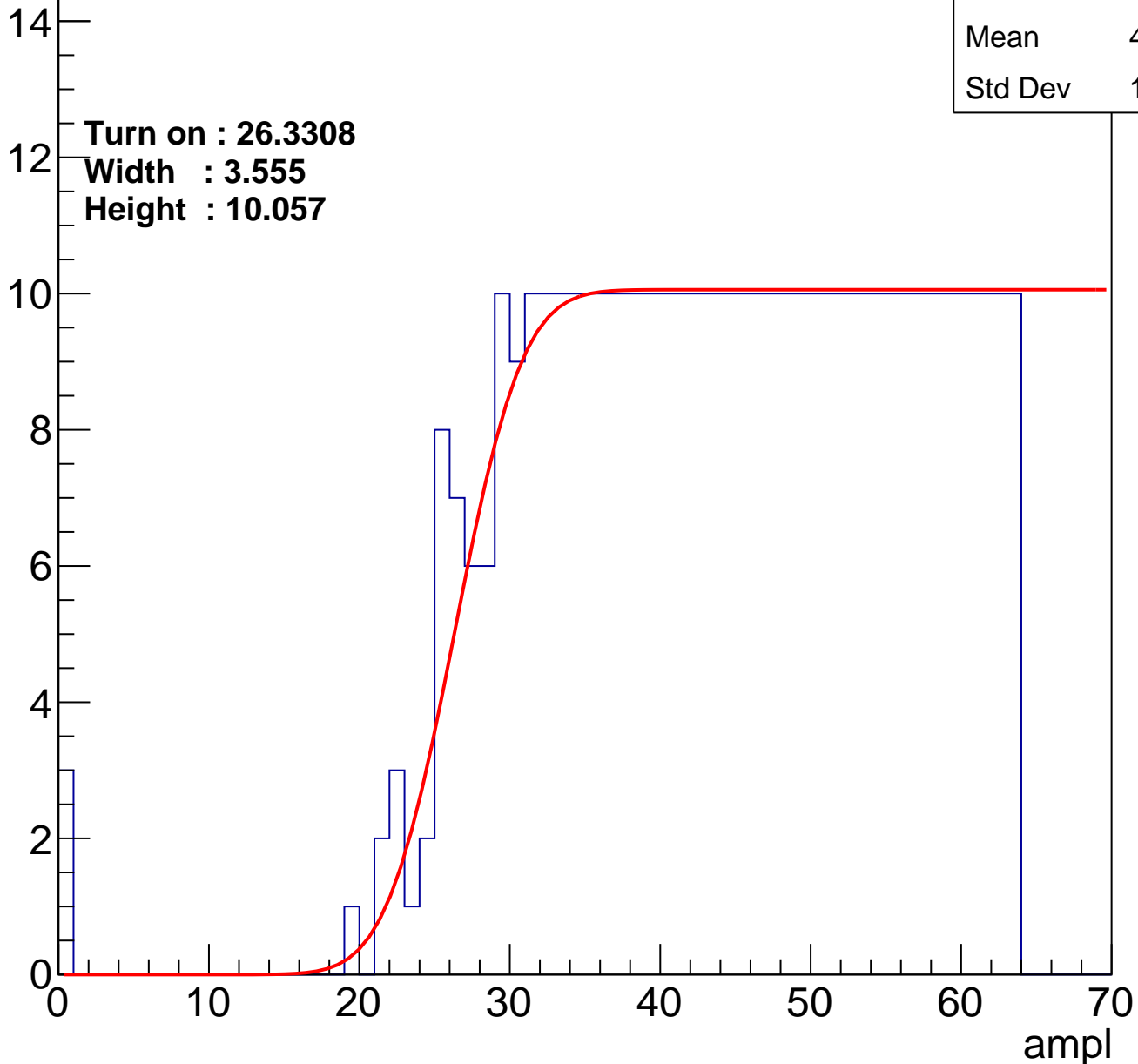
Entries	388
Mean	43.76
Std Dev	11.96

Turn on : 26.3308

Width : 3.555

Height : 10.057

Entry



B1L101S, U19-ch85

calib_packv5_042523_0143.root, FC#0, port D2

Entries	364
Mean	44.92
Std Dev	11.49

Turn on : 28.2016

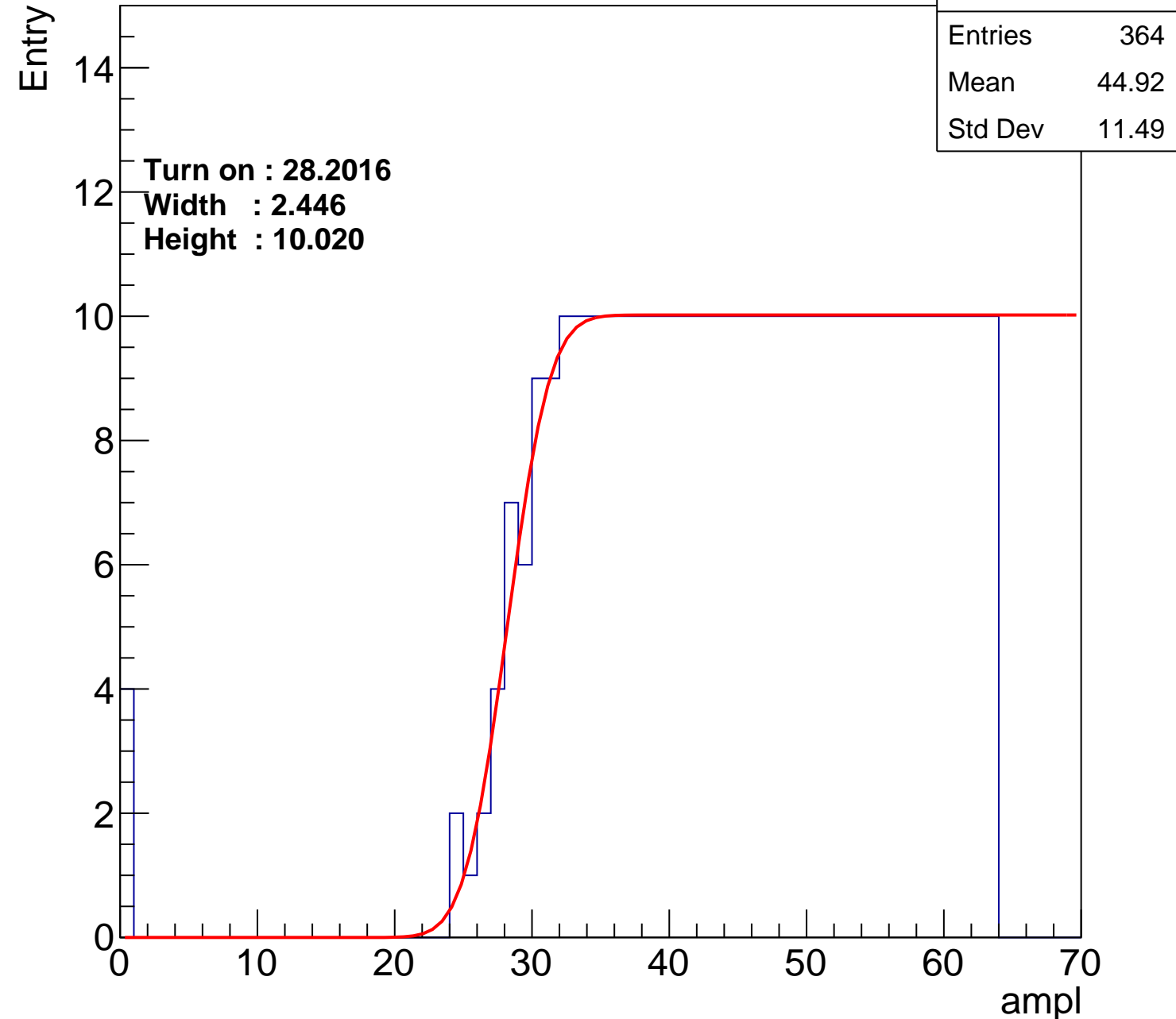
Width : 2.446

Height : 10.020

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch86

calib_packv5_042523_0143.root, FC#0, port D2

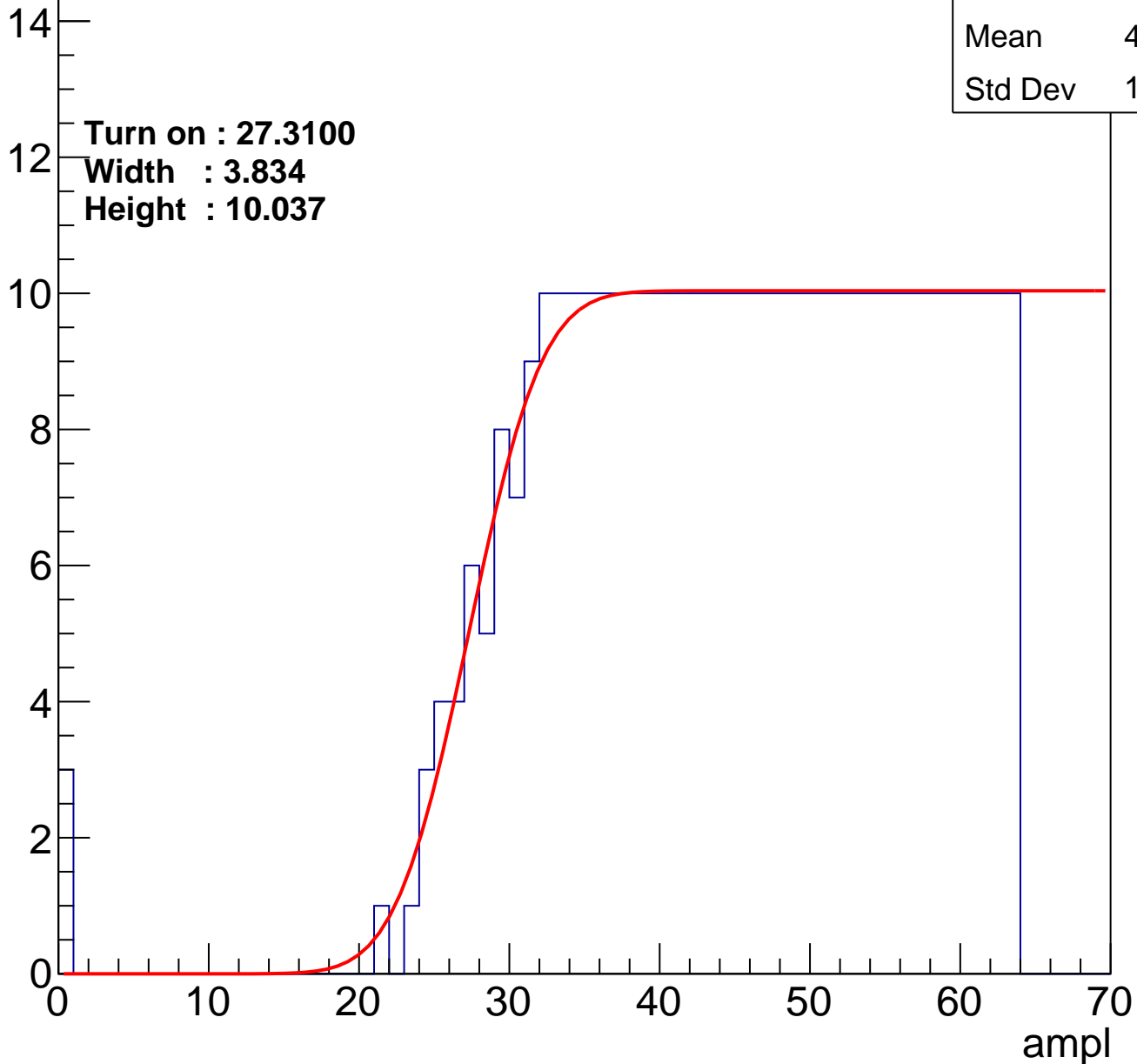
Entries	371
Mean	44.59
Std Dev	11.55

Turn on : 27.3100

Width : 3.834

Height : 10.037

Entry



B1L101S, U19-ch87

calib_packv5_042523_0143.root, FC#0, port D2

Entries	373
Mean	44.43
Std Dev	11.78

Turn on : 27.3069

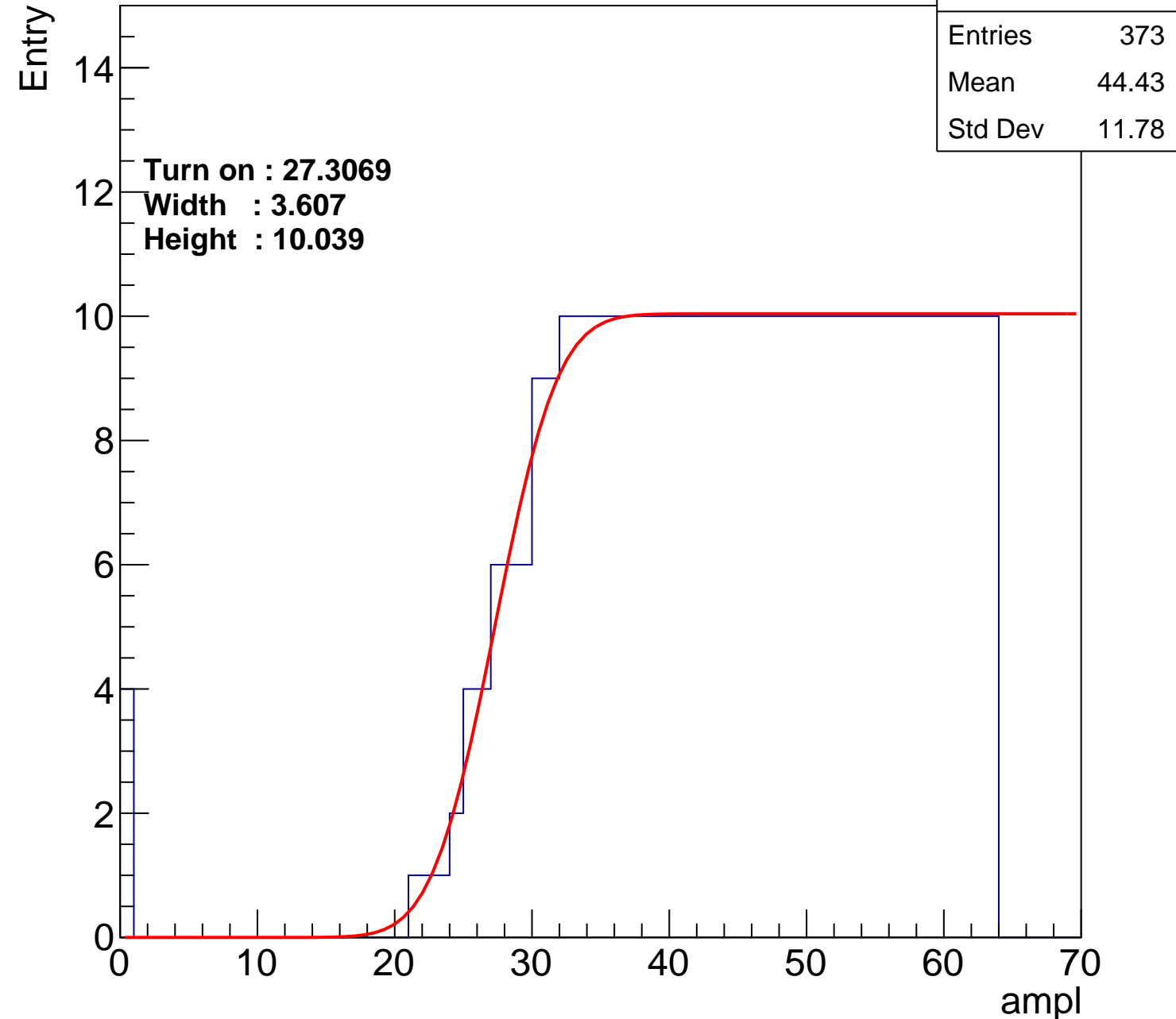
Width : 3.607

Height : 10.039

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch88

calib_packv5_042523_0143.root, FC#0, port D2

Entries	379
Mean	44.22
Std Dev	11.71

Turn on : 26.4266

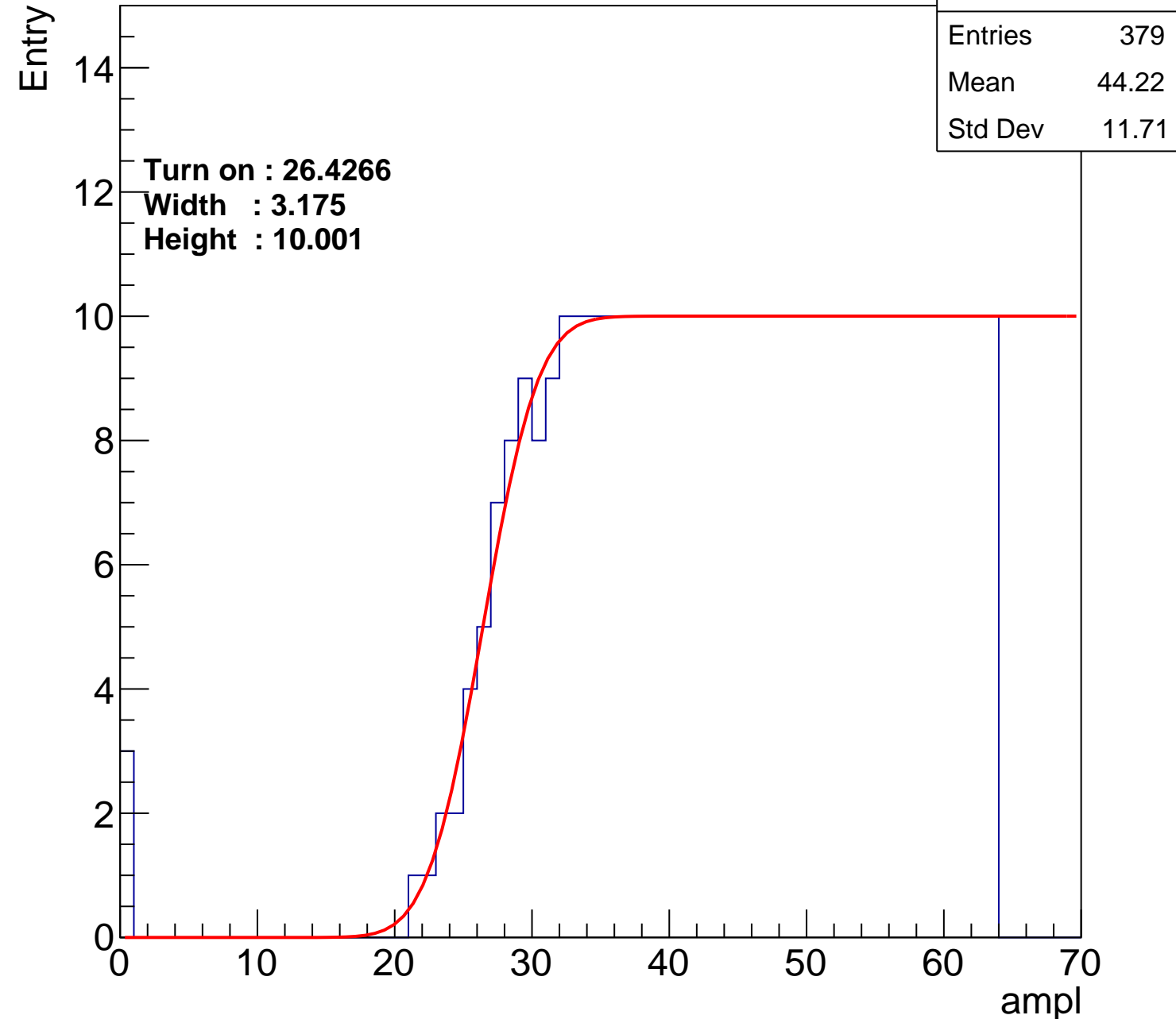
Width : 3.175

Height : 10.001

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch89

calib_packv5_042523_0143.root, FC#0, port D2

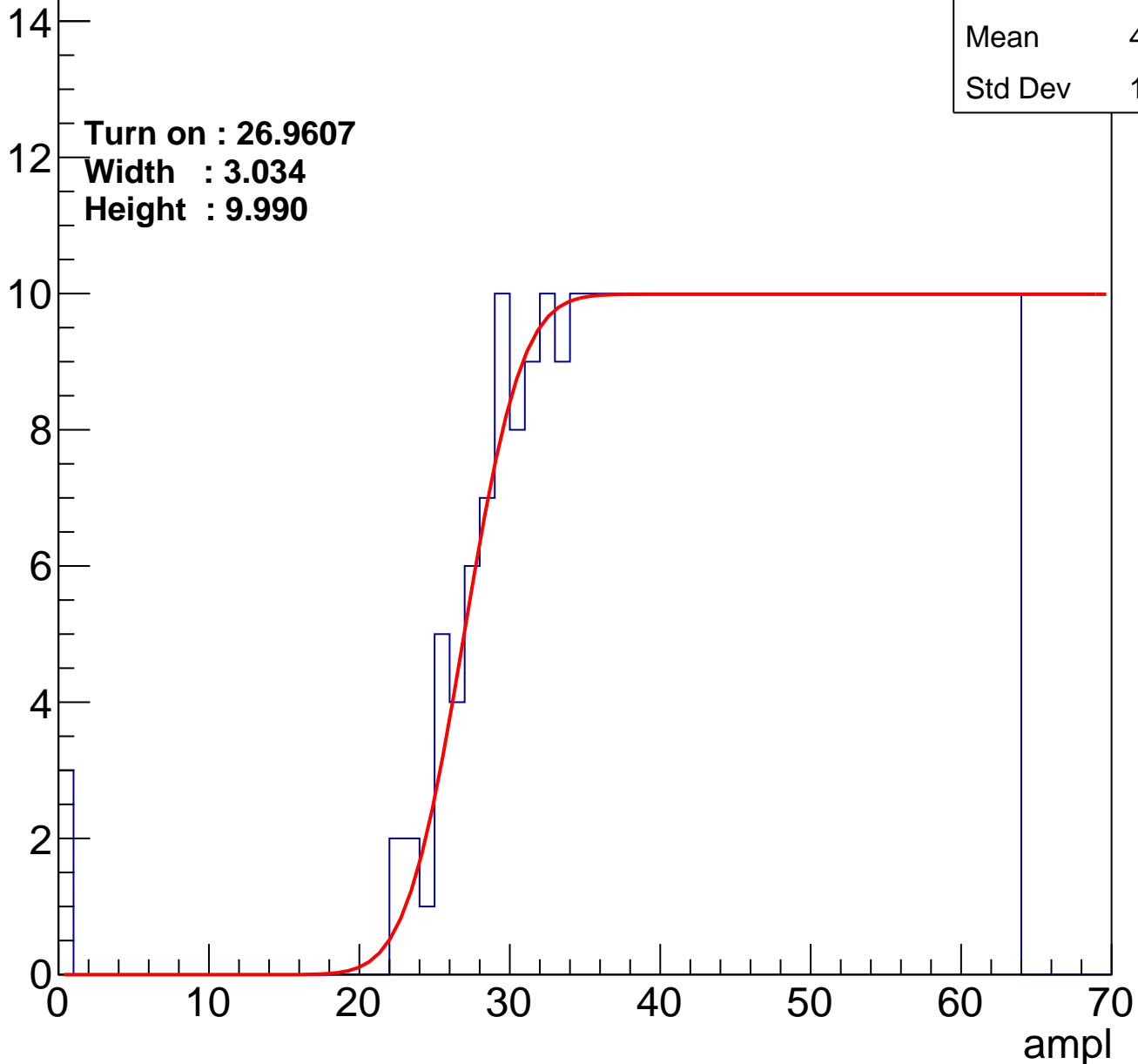
Entries	376
Mean	44.35
Std Dev	11.65

Turn on : 26.9607

Width : 3.034

Height : 9.990

Entry



B1L101S, U19-ch90

calib_packv5_042523_0143.root, FC#0, port D2

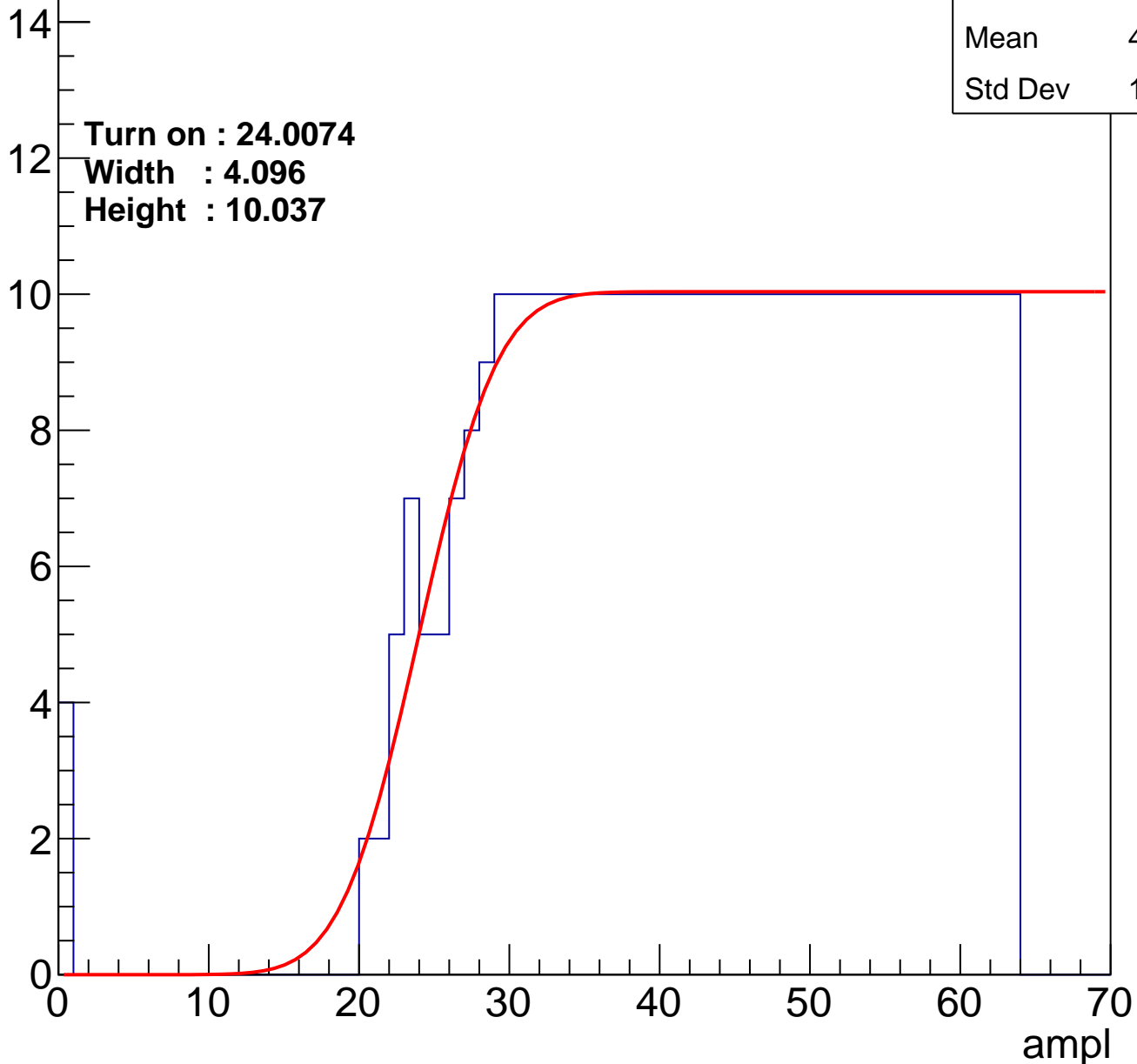
Entries	404
Mean	42.94
Std Dev	12.47

Turn on : 24.0074

Width : 4.096

Height : 10.037

Entry



B1L101S, U19-ch91

calib_packv5_042523_0143.root, FC#0, port D2

Entries	386
Mean	43.97
Std Dev	11.66

Turn on : 25.7167

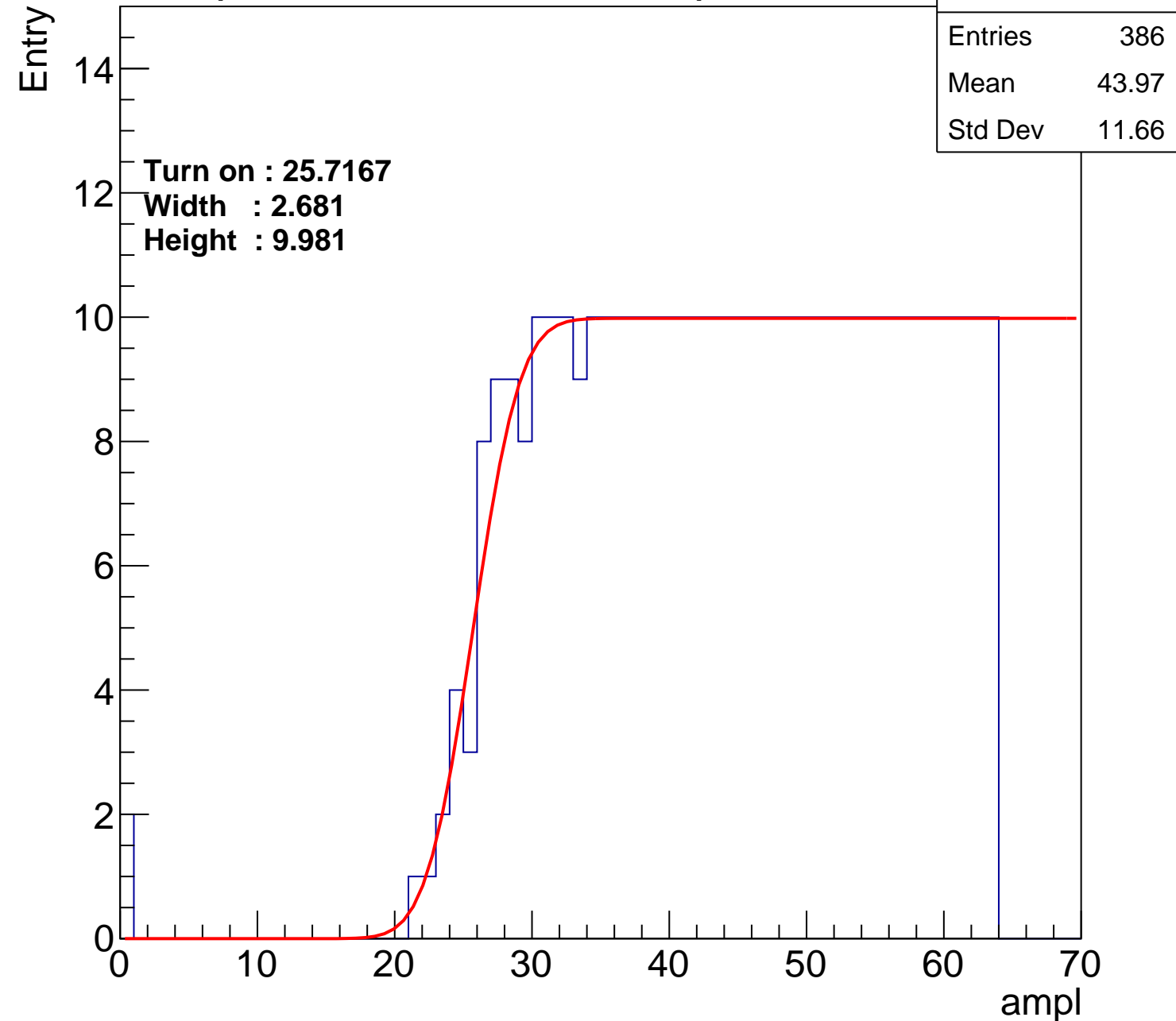
Width : 2.681

Height : 9.981

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch92

calib_packv5_042523_0143.root, FC#0, port D2

Entries	379
Mean	44.27
Std Dev	11.63

Turn on : 26.3380

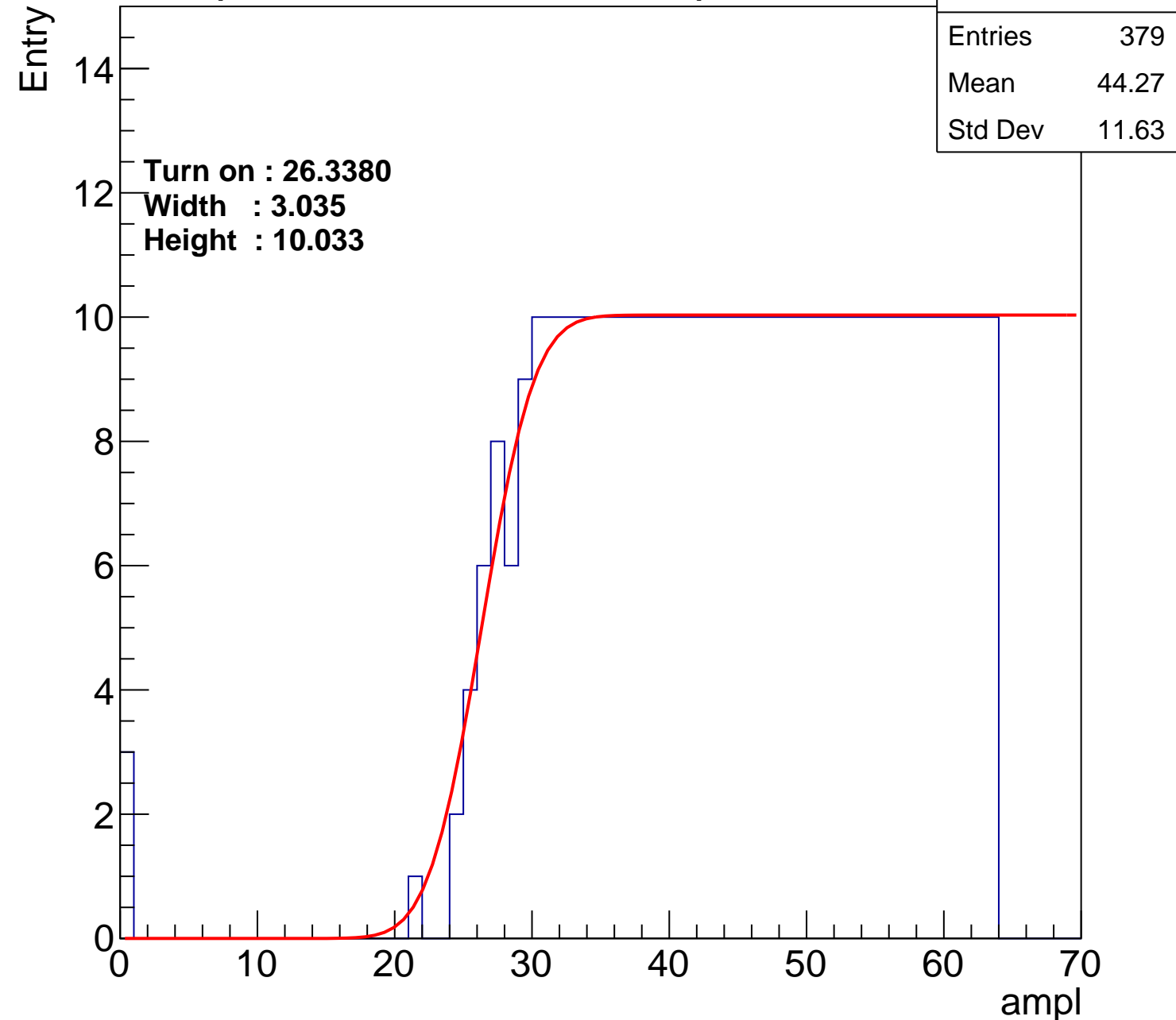
Width : 3.035

Height : 10.033

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch93

calib_packv5_042523_0143.root, FC#0, port D2

Entries	387
Mean	43.79
Std Dev	12.05

Turn on : 25.9889

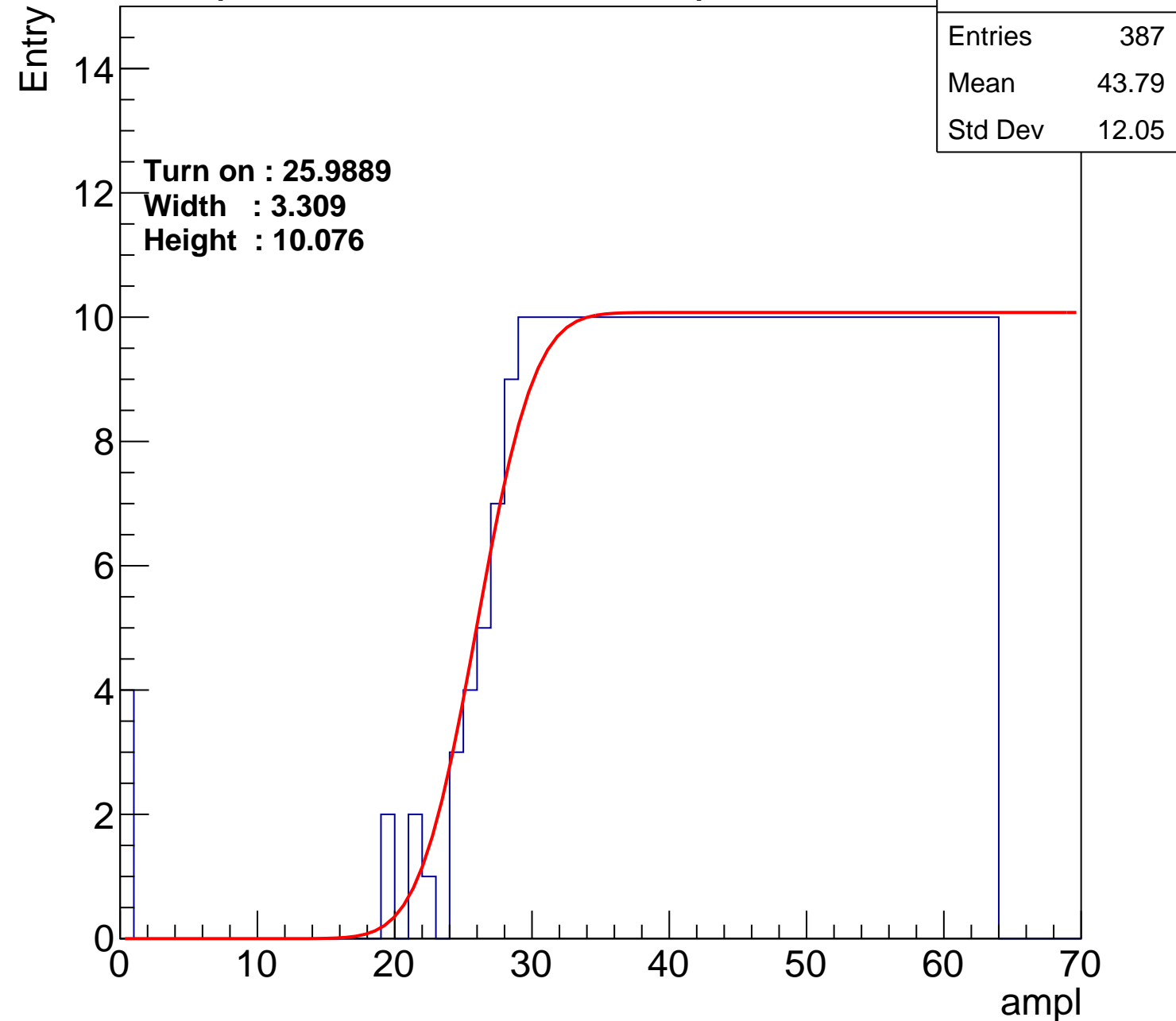
Width : 3.309

Height : 10.076

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch94

calib_packv5_042523_0143.root, FC#0, port D2

Entries	391
Mean	43.7
Std Dev	11.83

Turn on : 25.0570

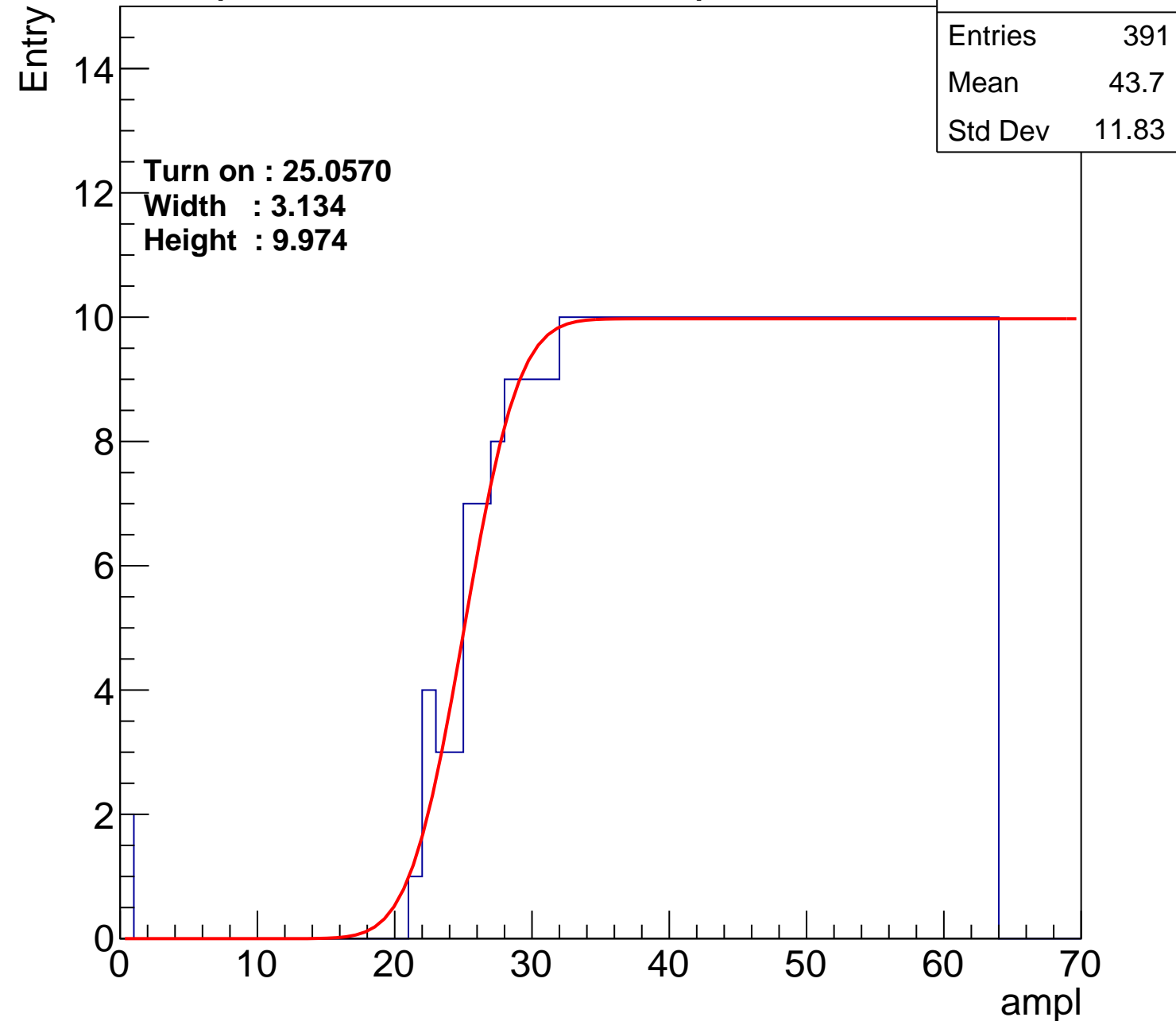
Width : 3.134

Height : 9.974

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch95

calib_packv5_042523_0143.root, FC#0, port D2

Entries	372
Mean	44.59
Std Dev	11.5

Turn on : 27.5159

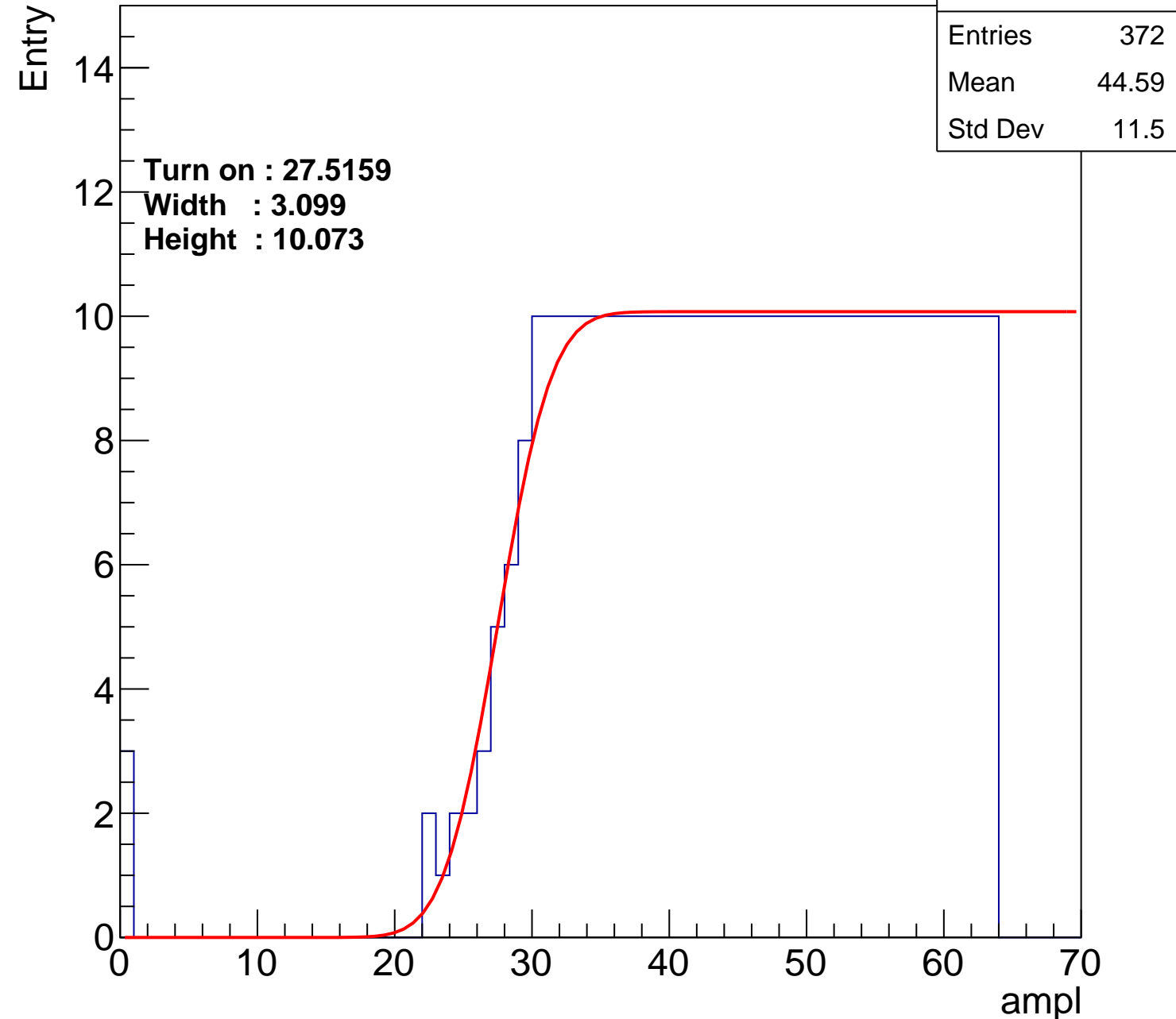
Width : 3.099

Height : 10.073

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch96

calib_packv5_042523_0143.root, FC#0, port D2

Entries	392
Mean	43.69
Std Dev	11.73

Turn on : 25.5904

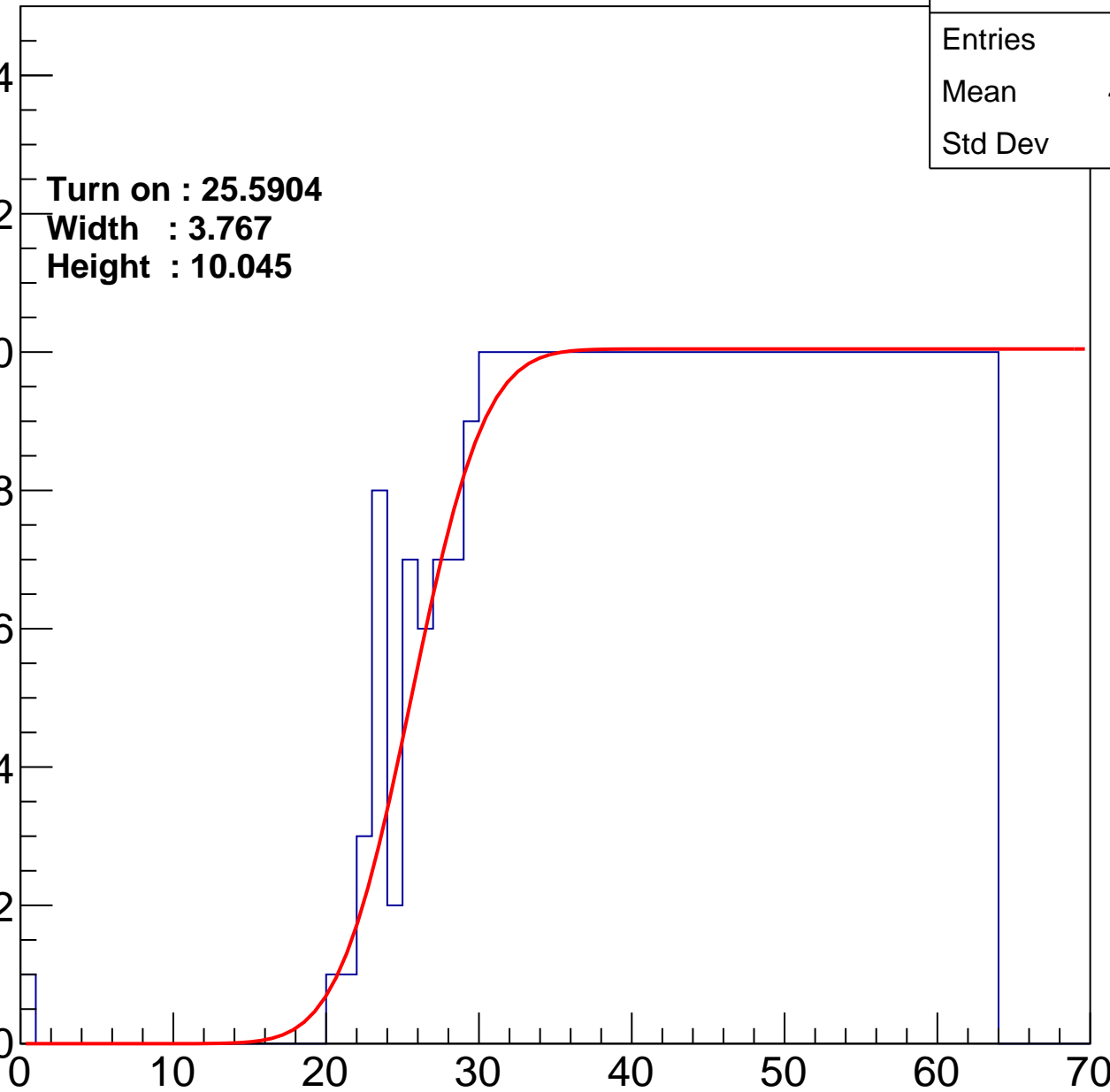
Width : 3.767

Height : 10.045

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch97

calib_packv5_042523_0143.root, FC#0, port D2

Entries	376
Mean	44.33
Std Dev	11.77

Turn on : 26.8331

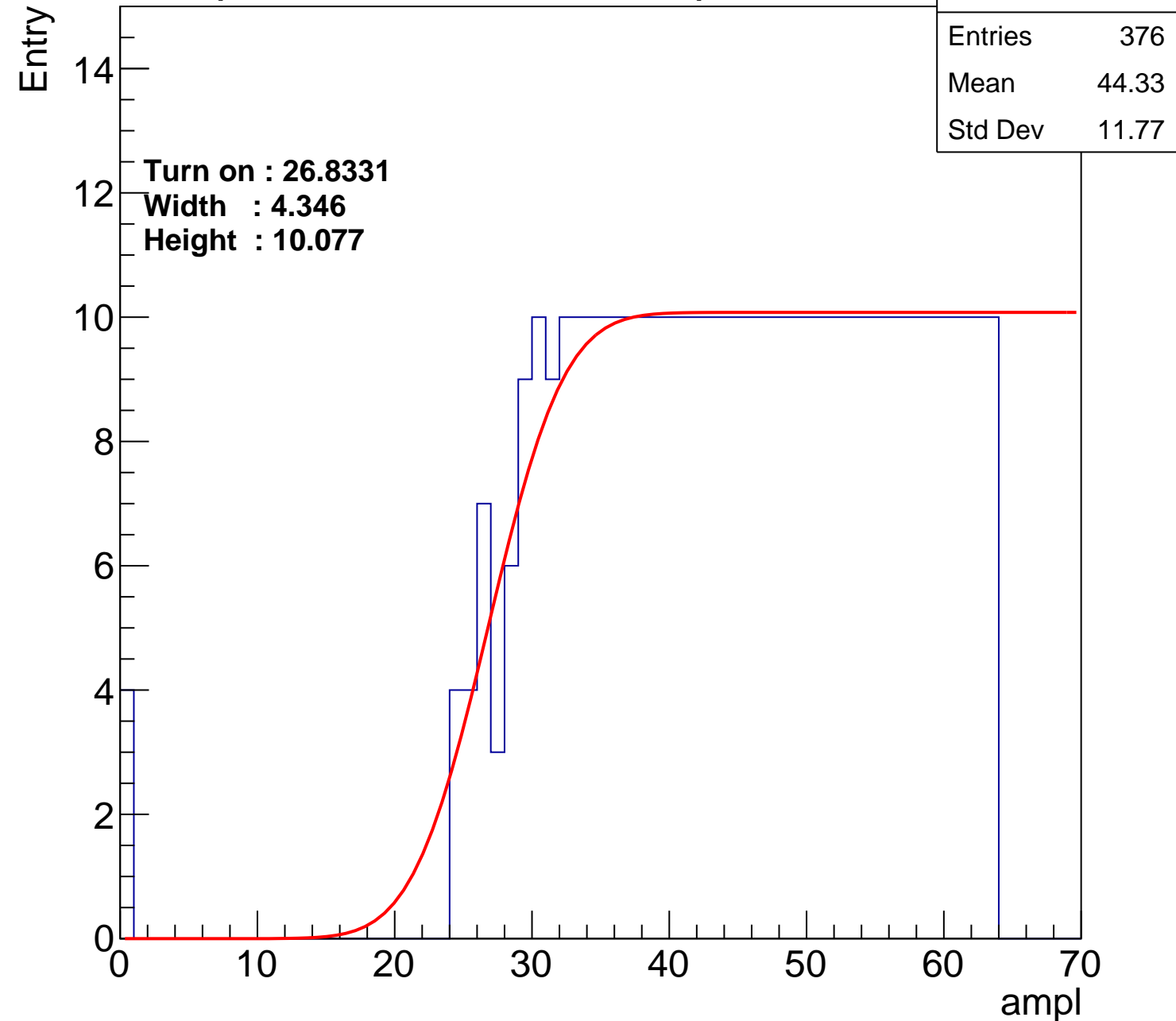
Width : 4.346

Height : 10.077

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch98

calib_packv5_042523_0143.root, FC#0, port D2

Entries	381
Mean	44.1
Std Dev	11.87

Turn on : 26.8044

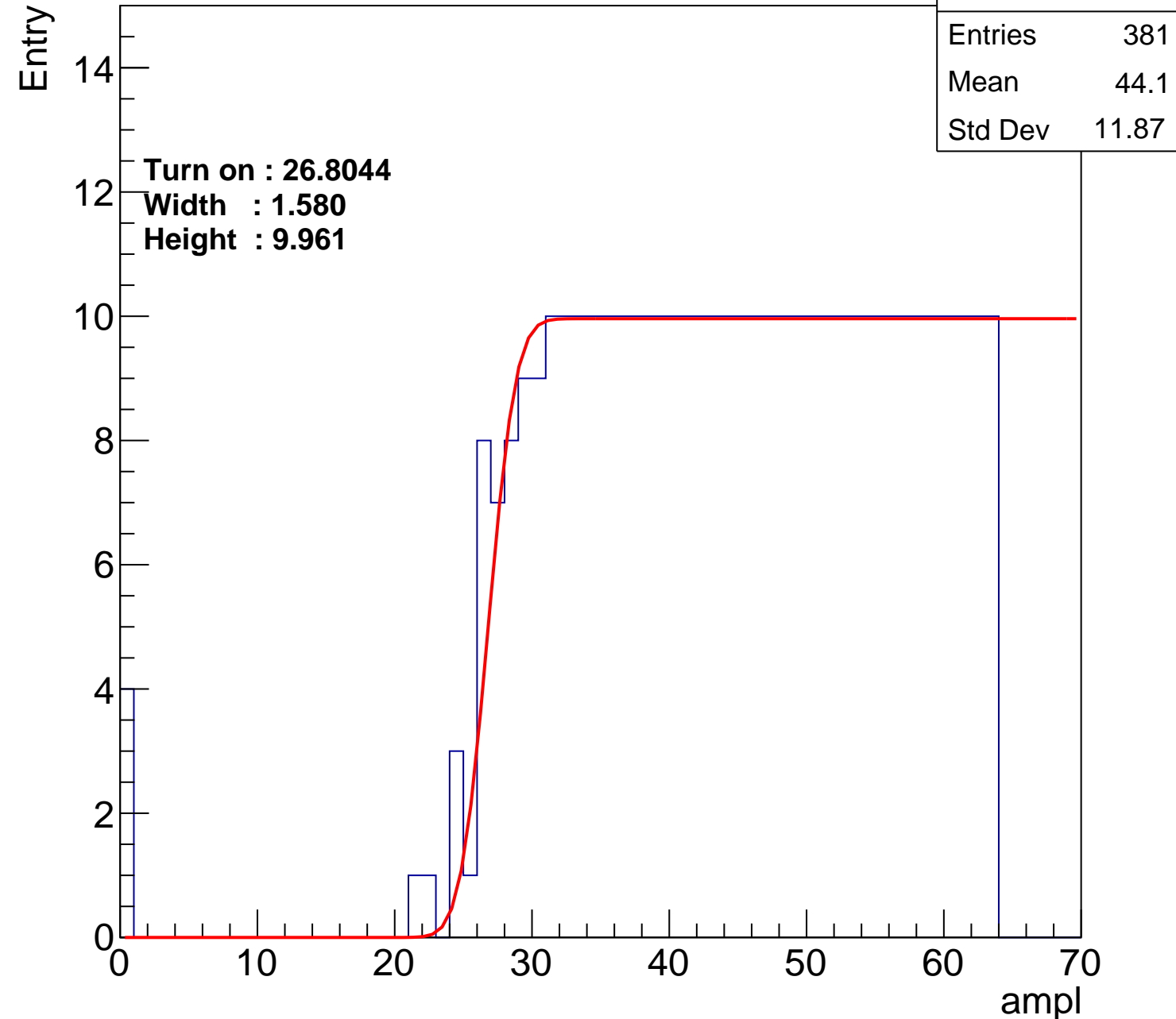
Width : 1.580

Height : 9.961

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch99

calib_packv5_042523_0143.root, FC#0, port D2

Entries	361
Mean	45.08
Std Dev	11.31

Turn on : 28.7771

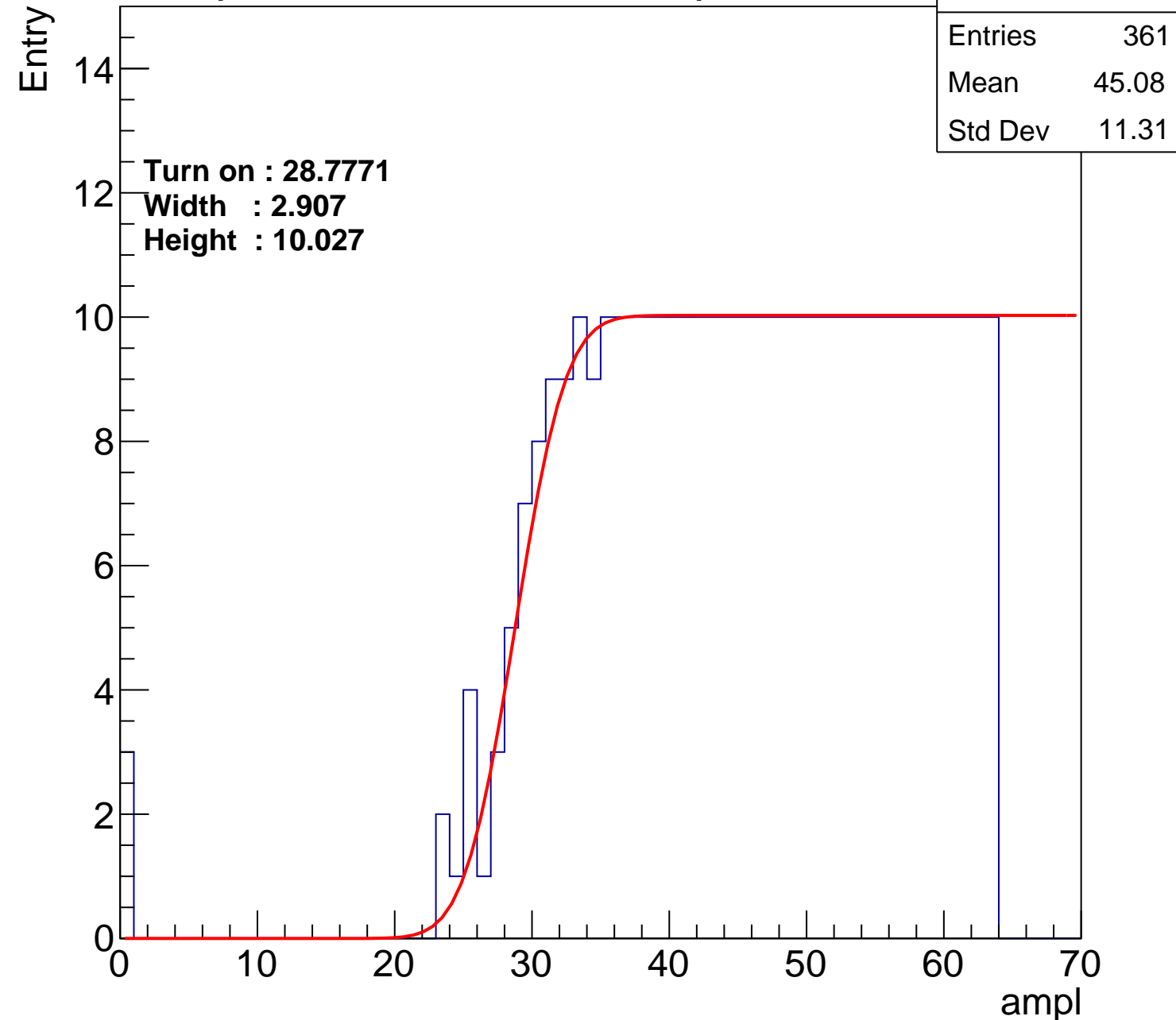
Width : 2.907

Height : 10.027

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch100

calib_packv5_042523_0143.root, FC#0, port D2

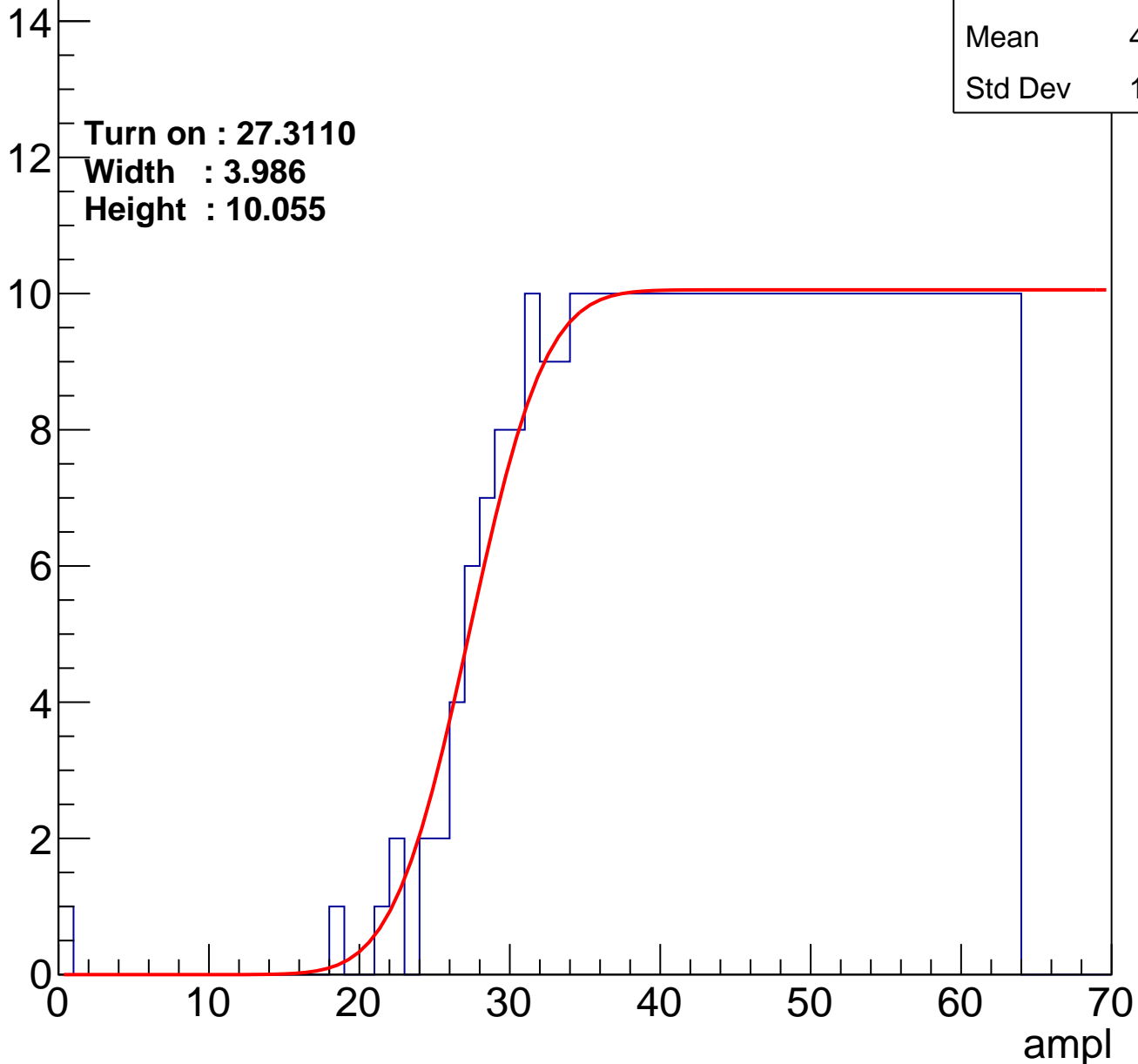
Entries	370
Mean	44.76
Std Dev	11.18

Turn on : 27.3110

Width : 3.986

Height : 10.055

Entry



B1L101S, U19-ch101

calib_packv5_042523_0143.root, FC#0, port D2

Entries	361
Mean	45.11
Std Dev	11.26

Turn on : 28.7327

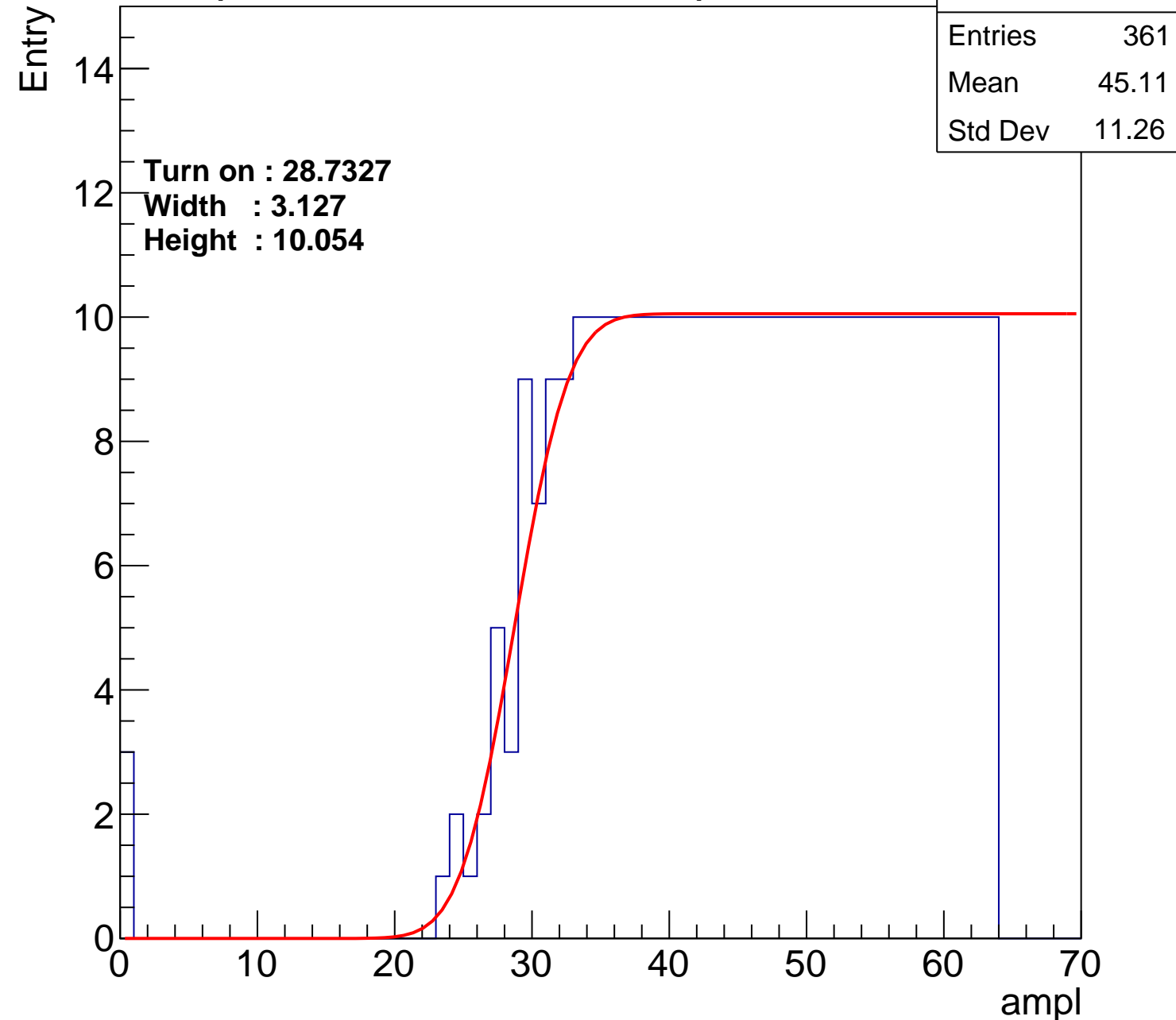
Width : 3.127

Height : 10.054

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch102

calib_packv5_042523_0143.root, FC#0, port D2

Entries	394
Mean	43.38
Std Dev	12.31

Turn on : 25.7782

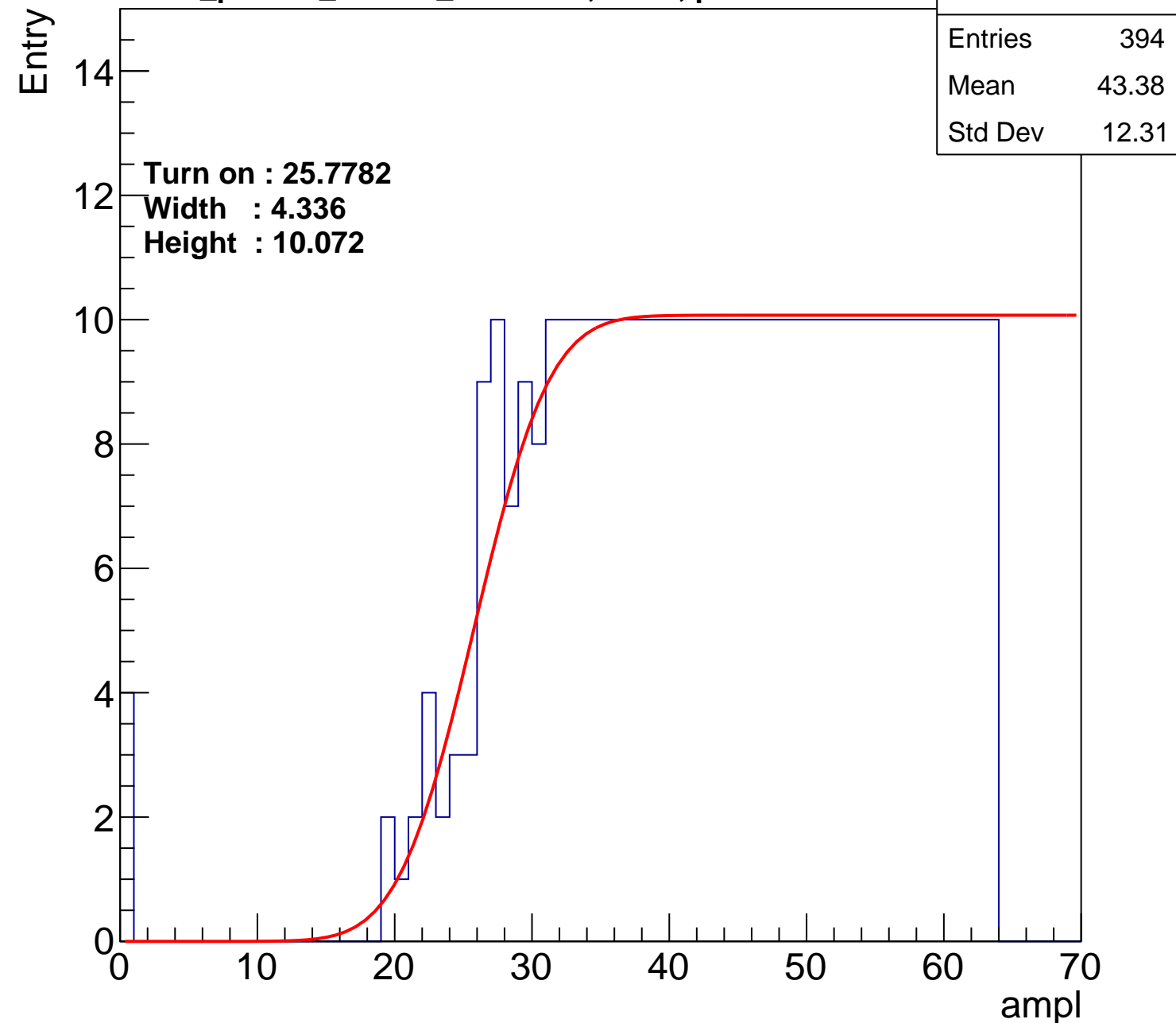
Width : 4.336

Height : 10.072

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch103

calib_packv5_042523_0143.root, FC#0, port D2

Entries	384
Mean	44.05
Std Dev	11.64

Turn on : 26.3125

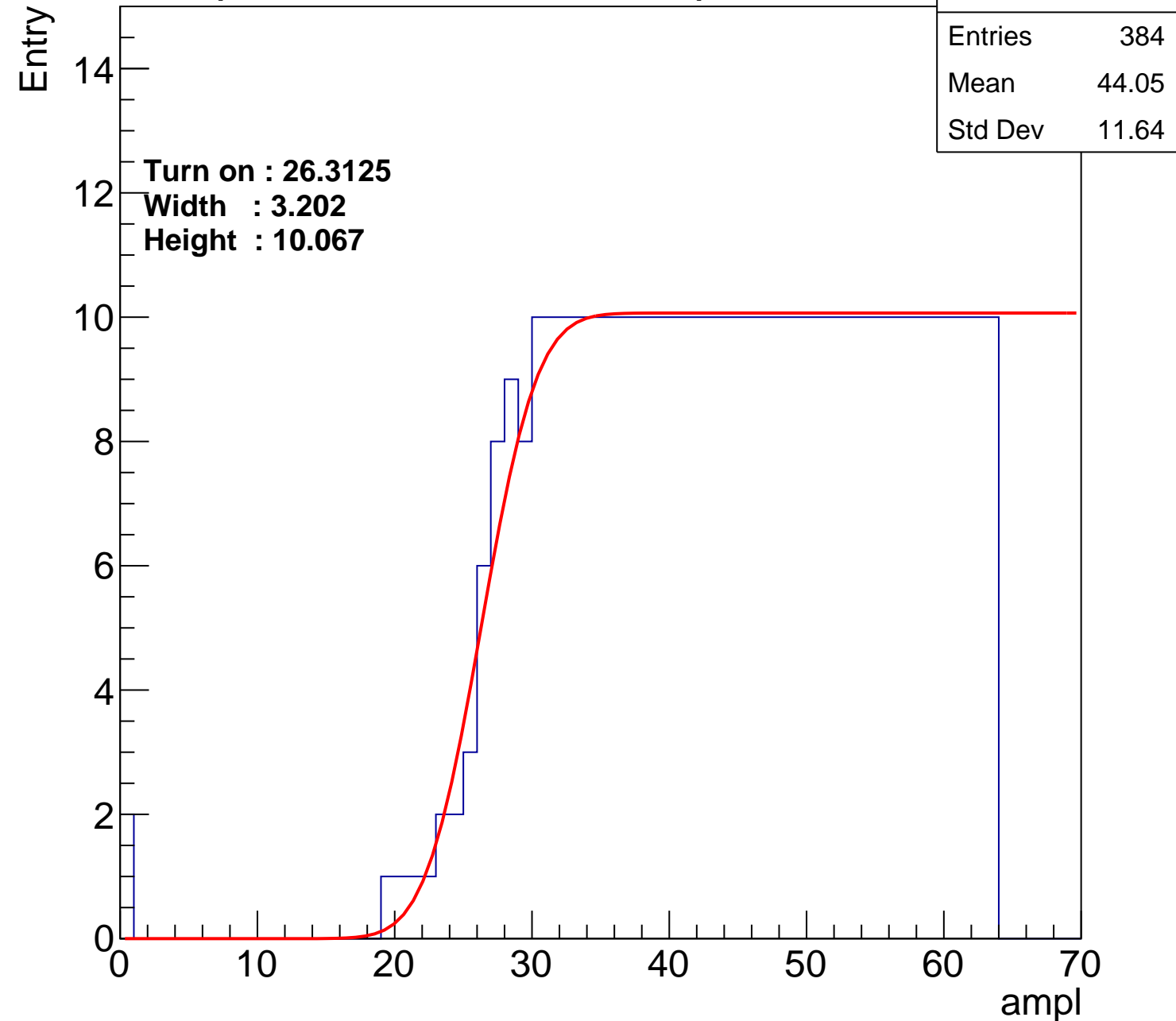
Width : 3.202

Height : 10.067

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch104

calib_packv5_042523_0143.root, FC#0, port D2

Entries	372
Mean	44.54
Std Dev	11.58

Turn on : 27.5427

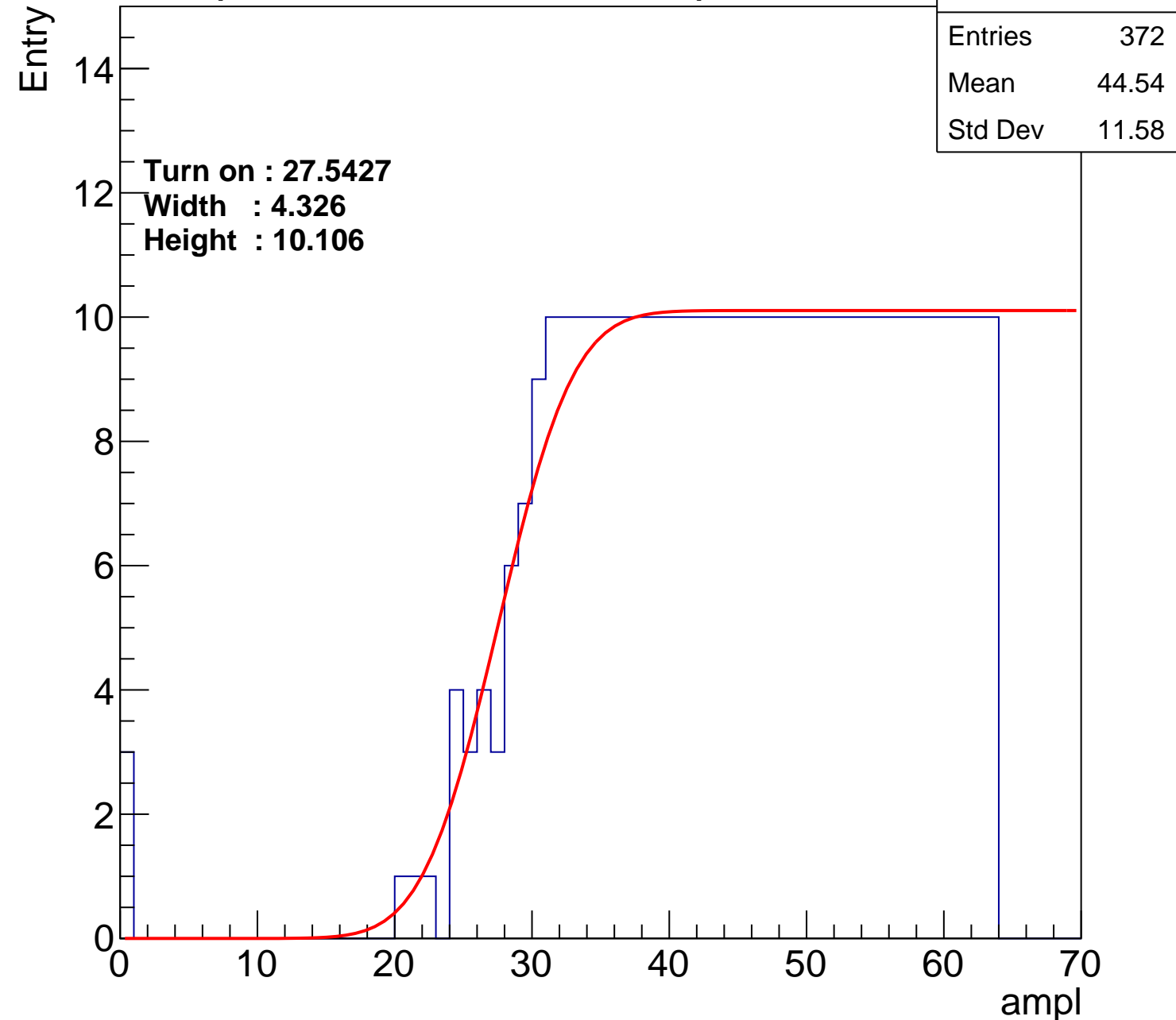
Width : 4.326

Height : 10.106

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch105

calib_packv5_042523_0143.root, FC#0, port D2

Entries	375
Mean	44.43
Std Dev	11.59

Turn on : 26.6657

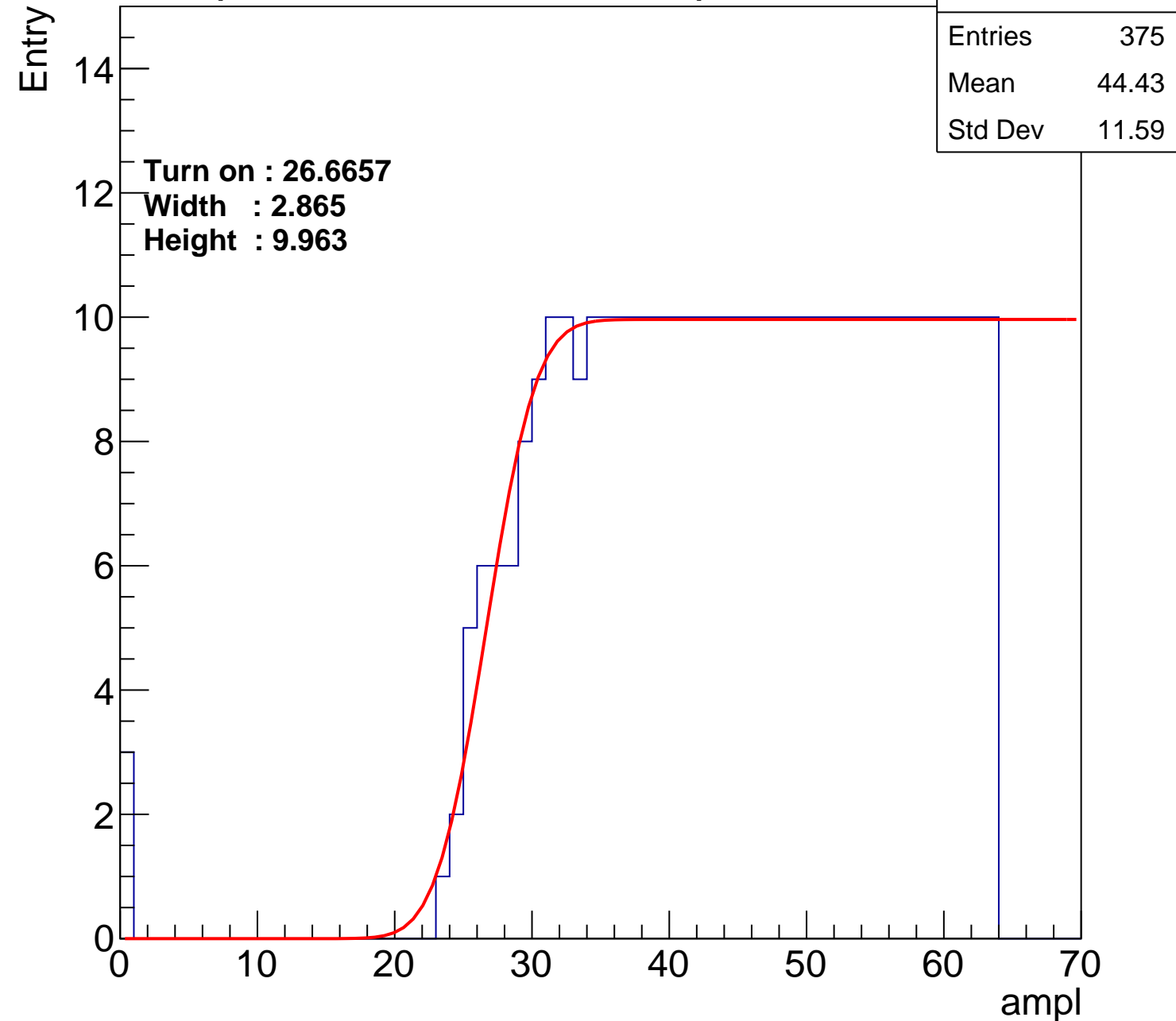
Width : 2.865

Height : 9.963

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch106

calib_packv5_042523_0143.root, FC#0, port D2

Entries	375
Mean	44.58
Std Dev	11.19

Turn on : 26.8289

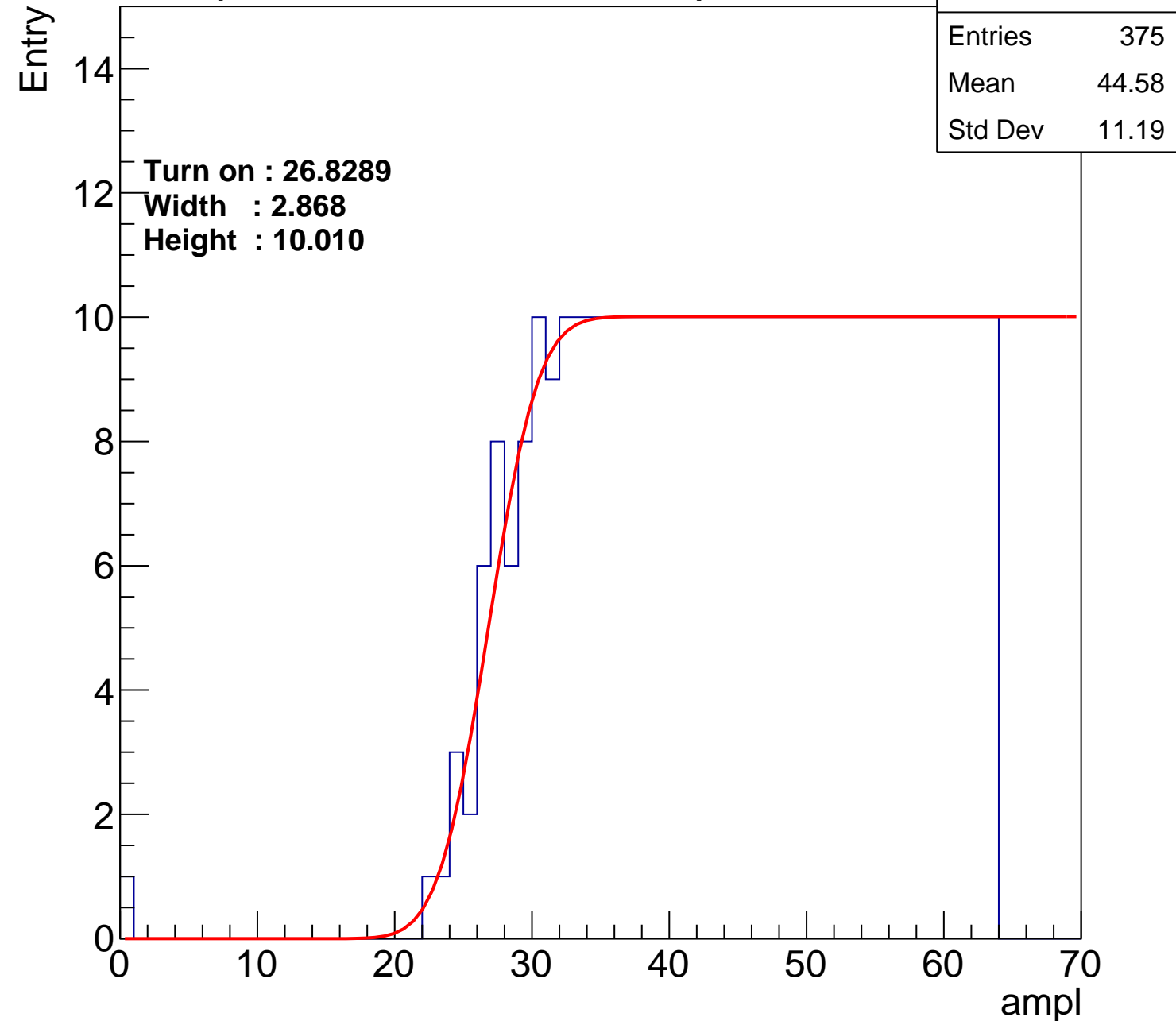
Width : 2.868

Height : 10.010

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch107

calib_packv5_042523_0143.root, FC#0, port D2

Entries	363
Mean	45.08
Std Dev	11.11

Turn on : 28.1943

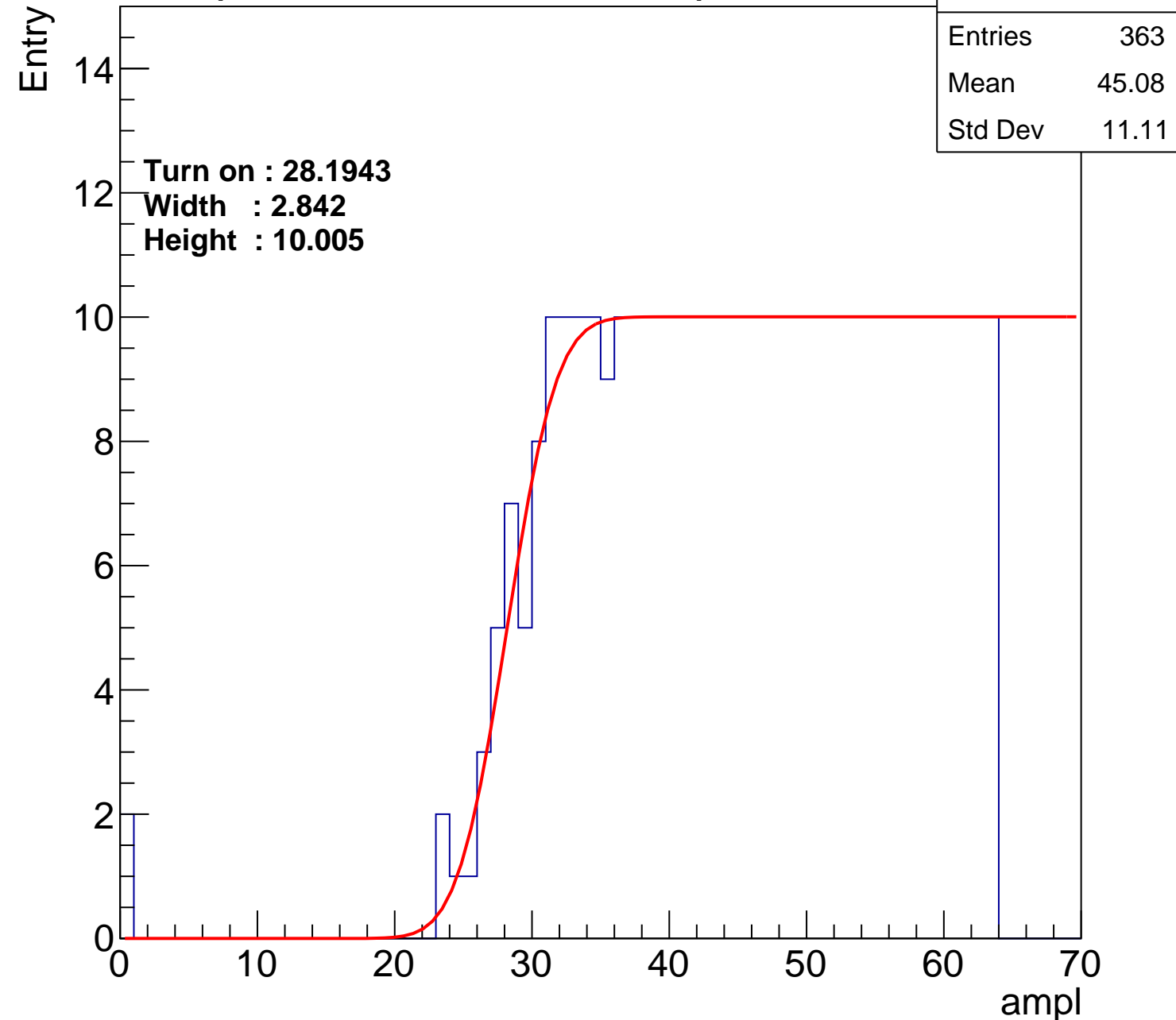
Width : 2.842

Height : 10.005

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch108

calib_packv5_042523_0143.root, FC#0, port D2

Entries	369
Mean	44.72
Std Dev	11.37

Turn on : 28.5477

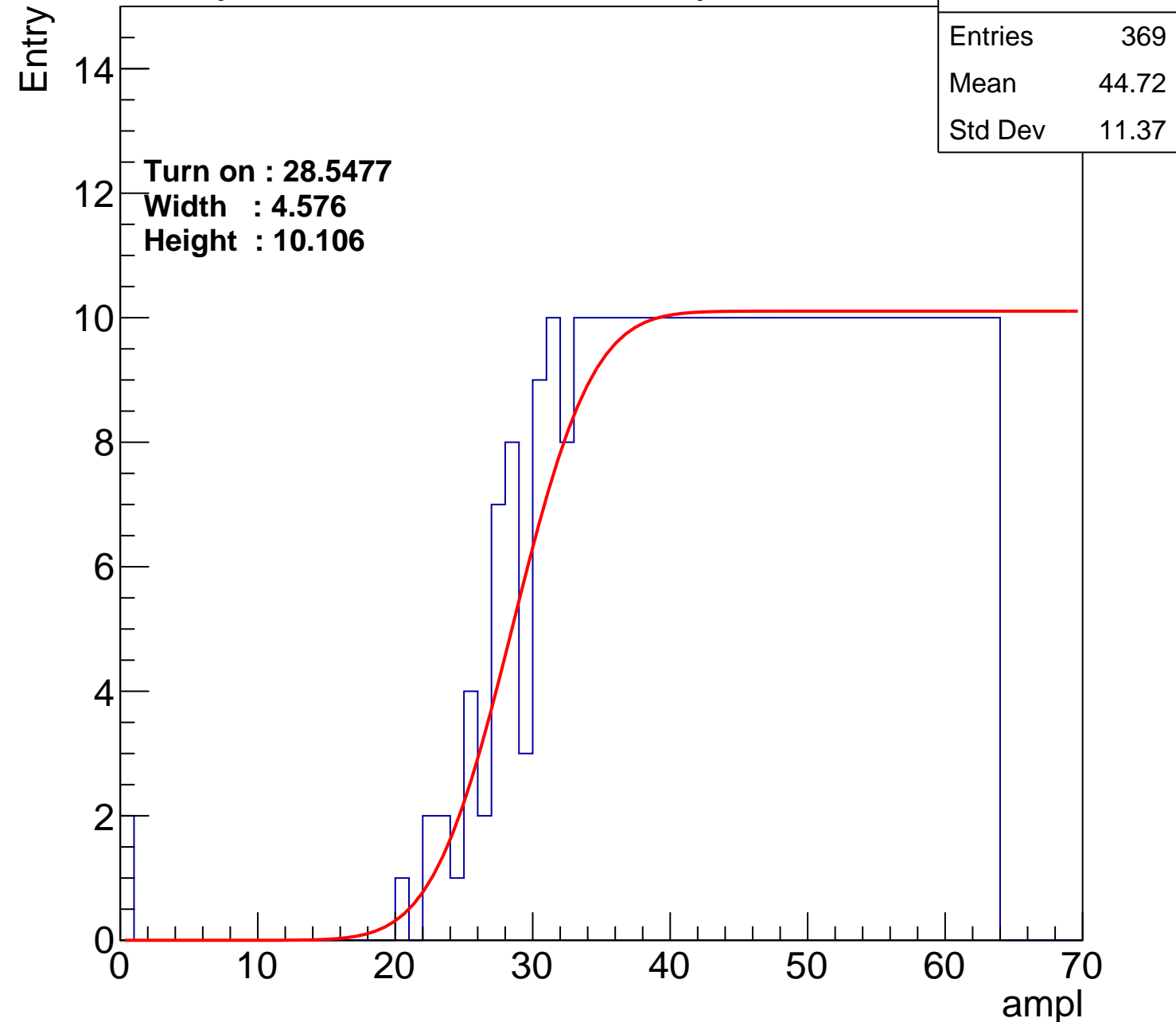
Width : 4.576

Height : 10.106

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch109

calib_packv5_042523_0143.root, FC#0, port D2

Entries	368
Mean	44.8
Std Dev	11.37

Turn on : 27.5209

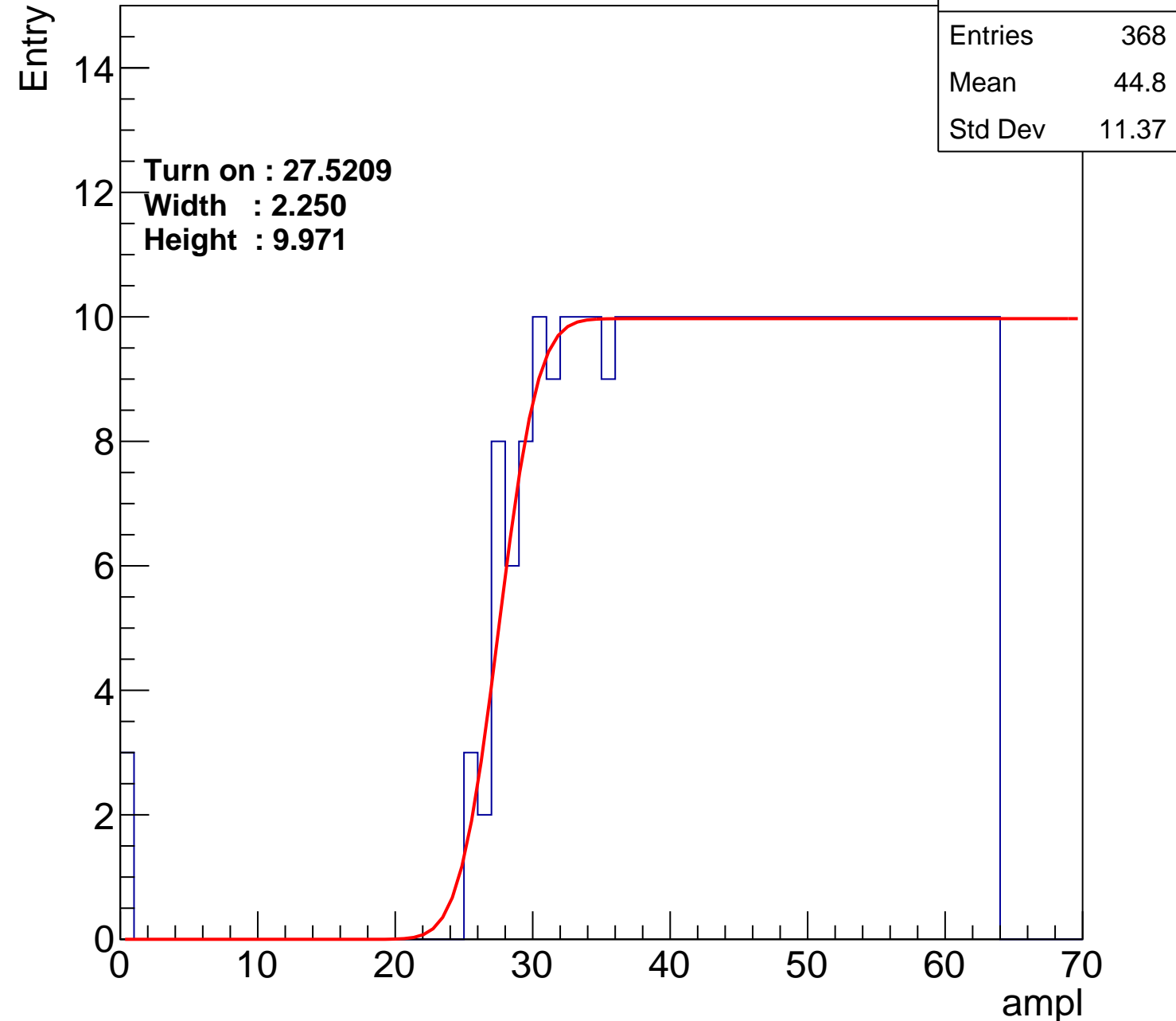
Width : 2.250

Height : 9.971

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch110

calib_packv5_042523_0143.root, FC#0, port D2

Entries	375
Mean	44.48
Std Dev	11.44

Turn on : 26.7787

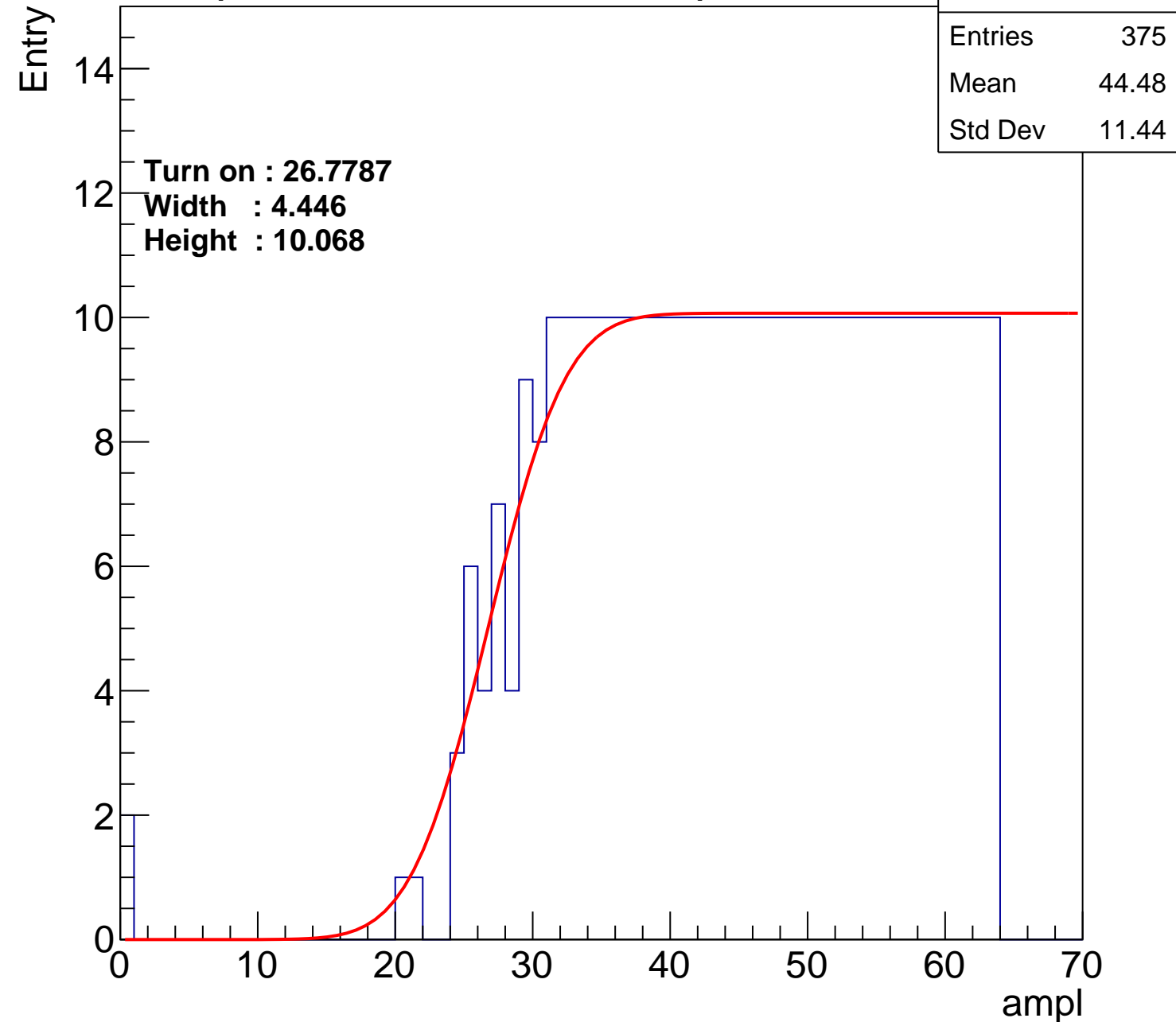
Width : 4.446

Height : 10.068

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch111

calib_packv5_042523_0143.root, FC#0, port D2

Entries	369
Mean	44.78
Std Dev	11.37

Turn on : 28.1752

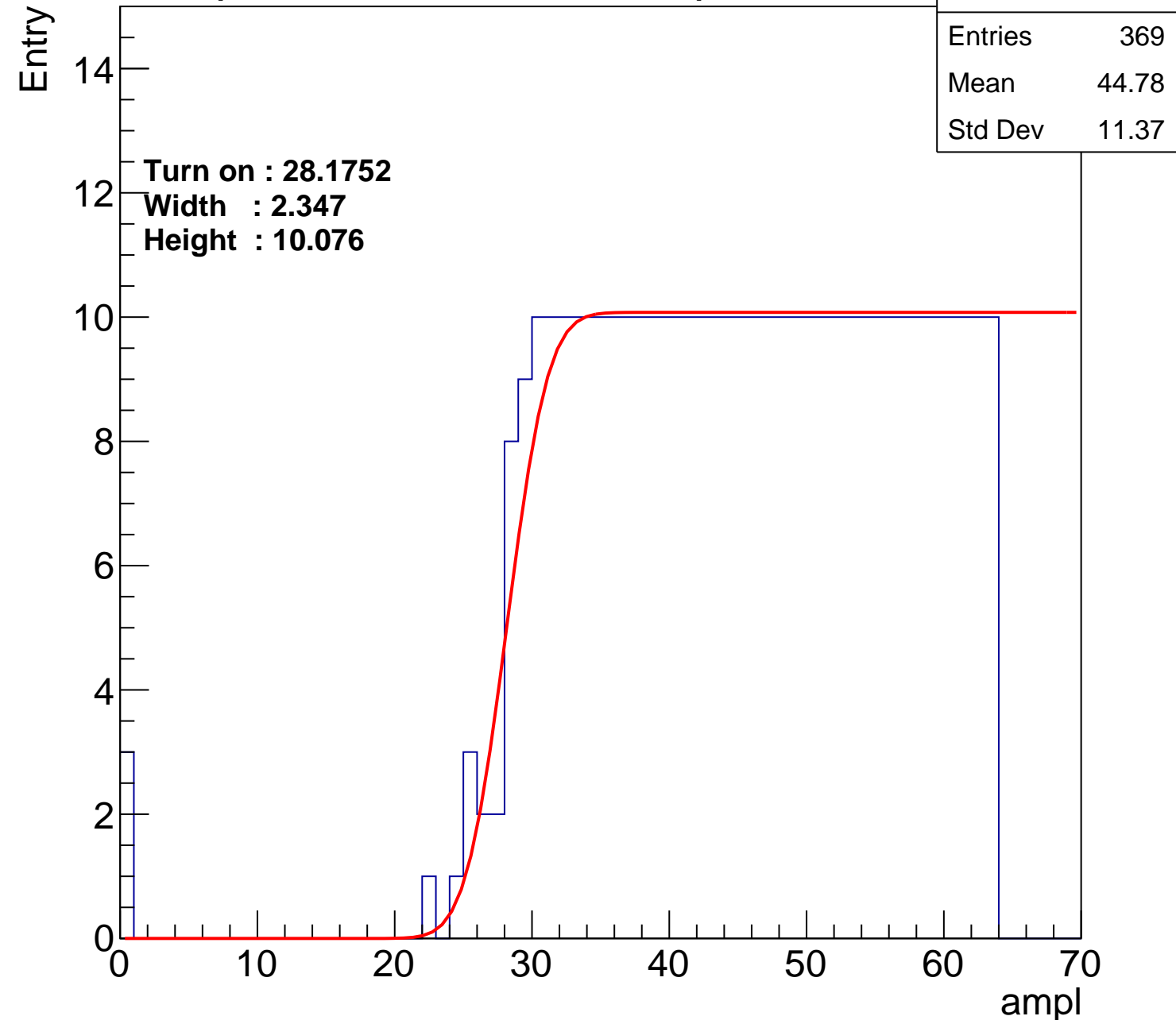
Width : 2.347

Height : 10.076

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch112

calib_packv5_042523_0143.root, FC#0, port D2

Entries	362
Mean	45.03
Std Dev	11.34

Turn on : 28.2480

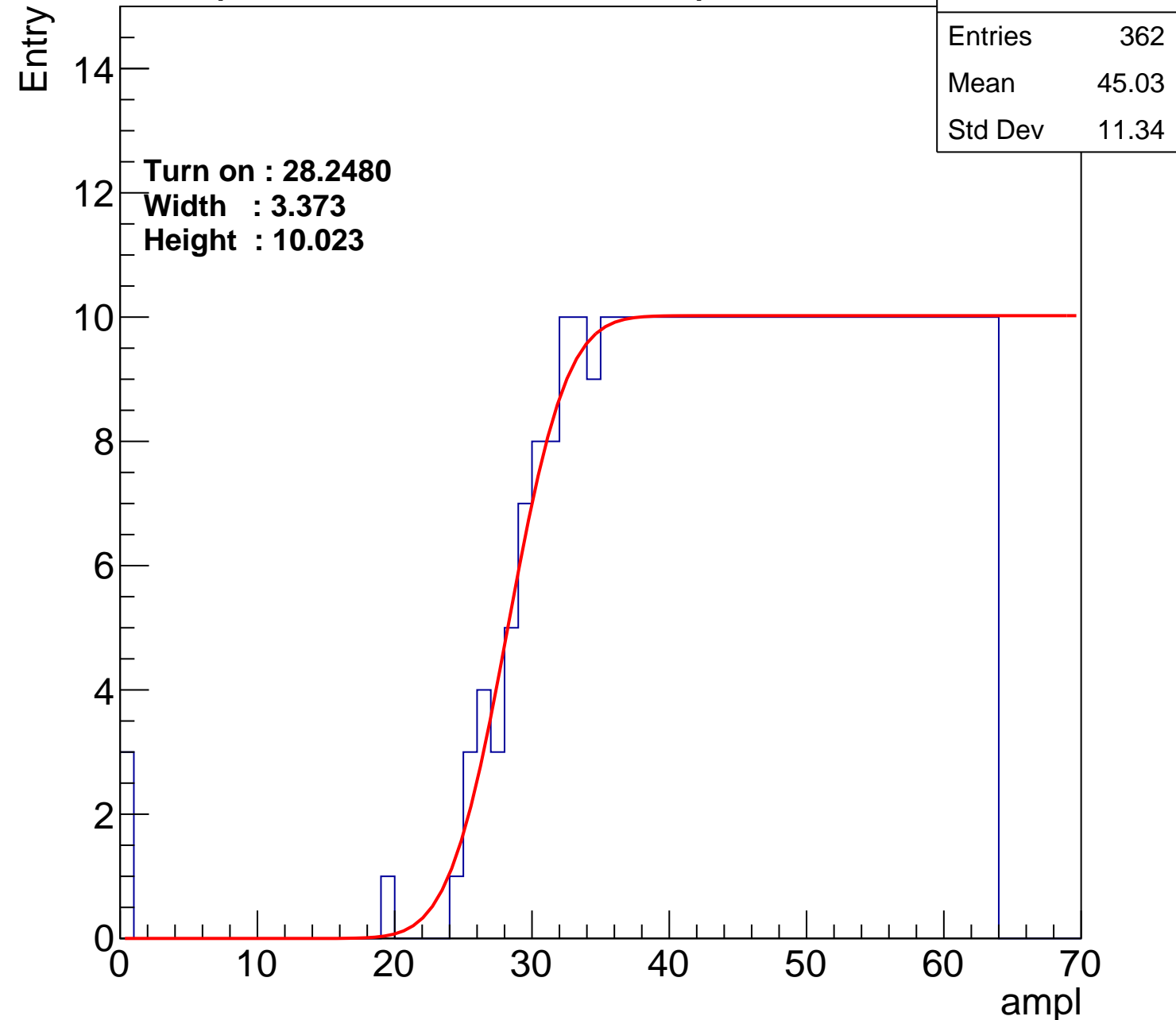
Width : 3.373

Height : 10.023

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch113

calib_packv5_042523_0143.root, FC#0, port D2

Entries	350
Mean	45.59
Std Dev	11.11

Turn on : 30.1911

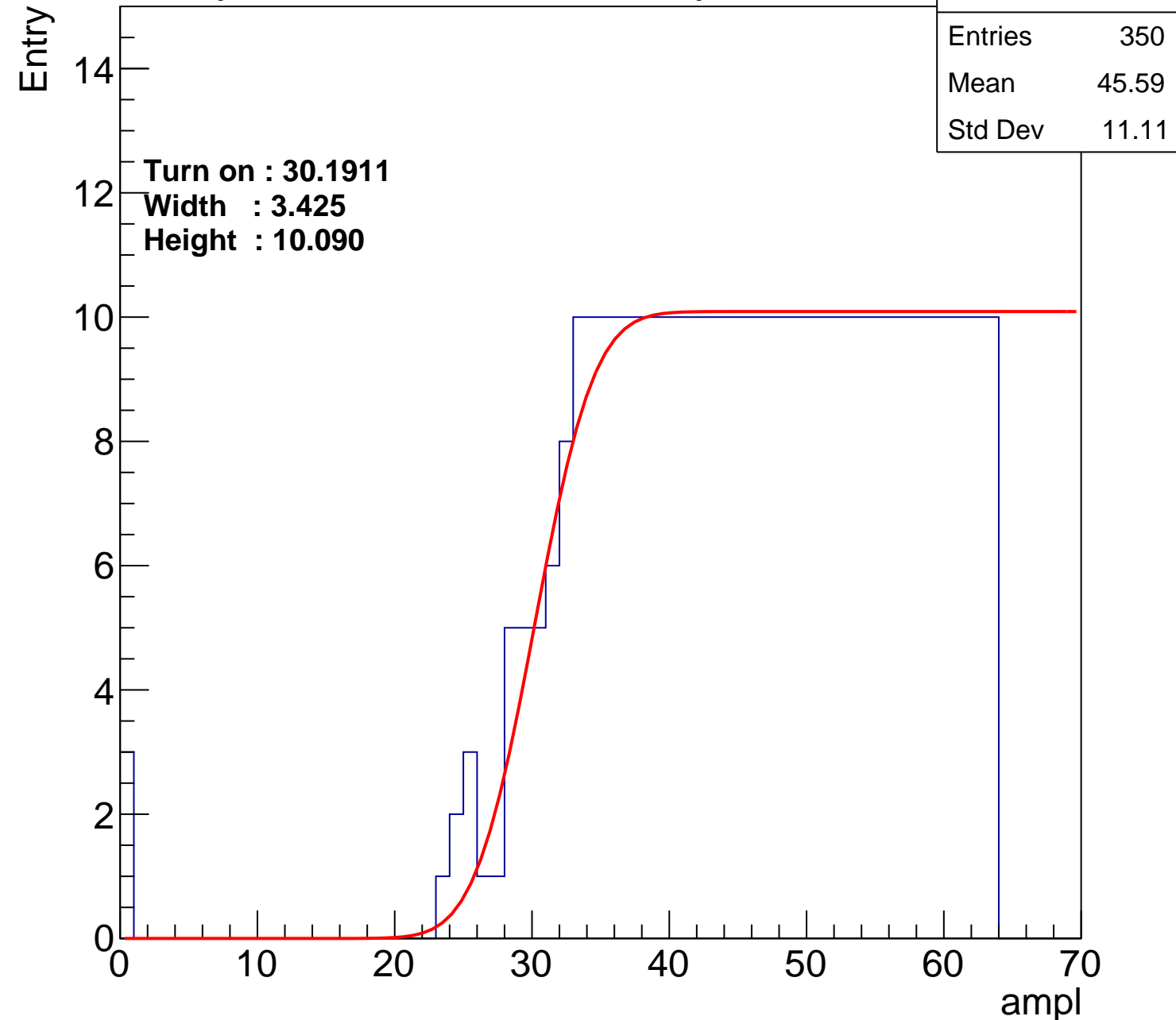
Width : 3.425

Height : 10.090

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch114

calib_packv5_042523_0143.root, FC#0, port D2

Entries	375
Mean	44.42
Std Dev	11.61

Turn on : 27.0285

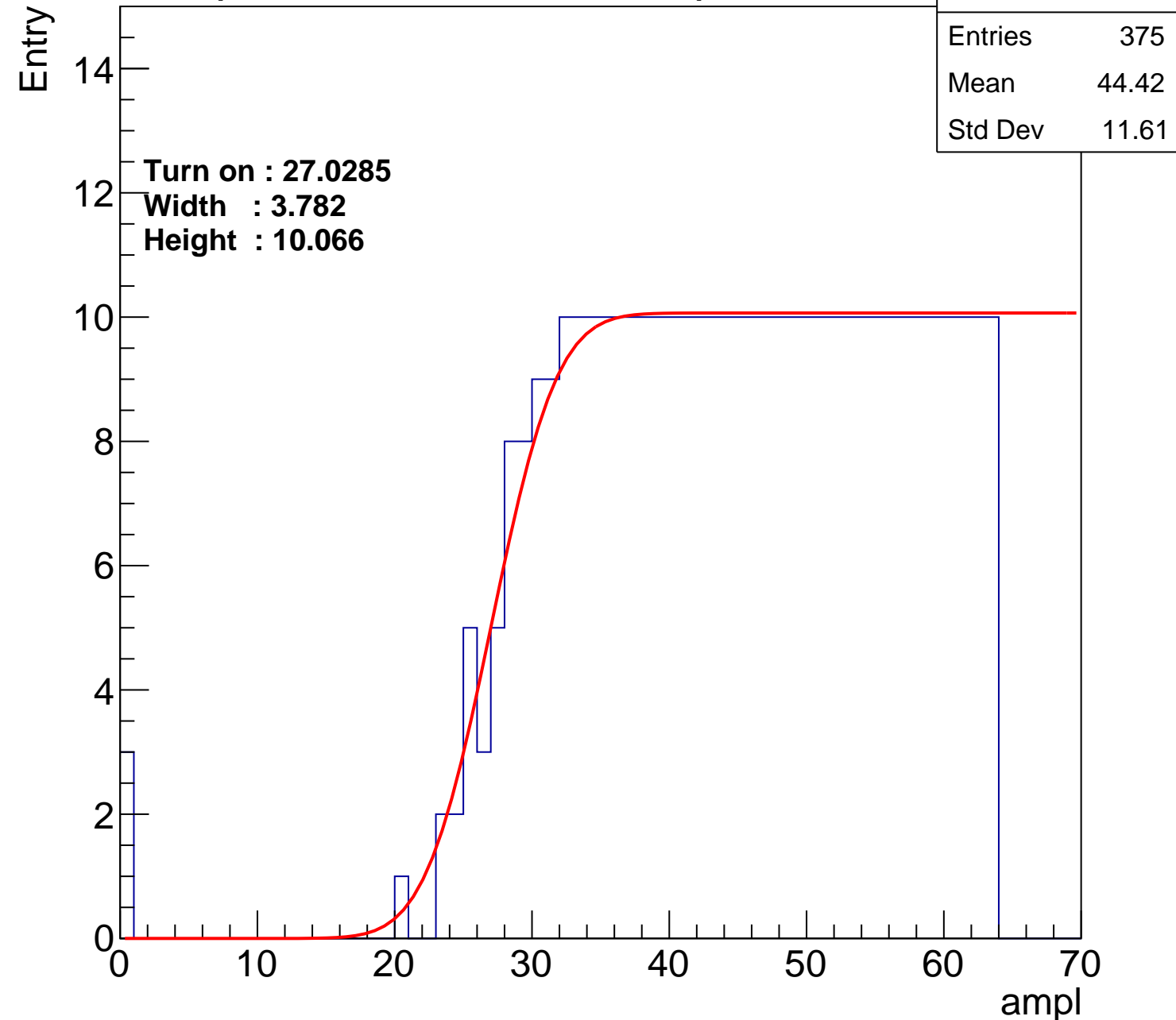
Width : 3.782

Height : 10.066

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch115

calib_packv5_042523_0143.root, FC#0, port D2

Entries	376
Mean	44.4
Std Dev	11.59

Turn on : 26.9992

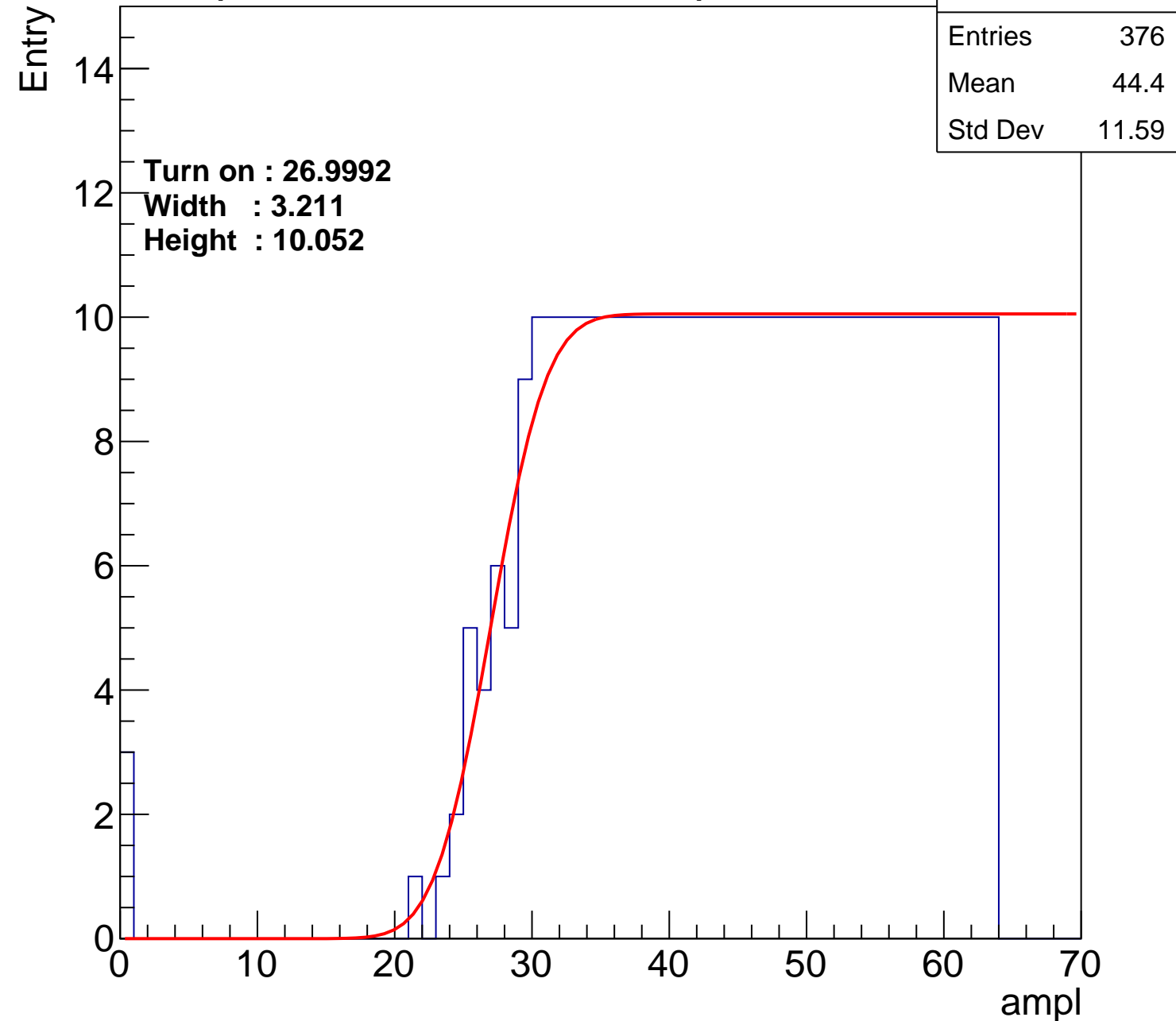
Width : 3.211

Height : 10.052

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch116

calib_packv5_042523_0143.root, FC#0, port D2

Entries	351
Mean	45.56
Std Dev	11.09

Turn on : 29.3433

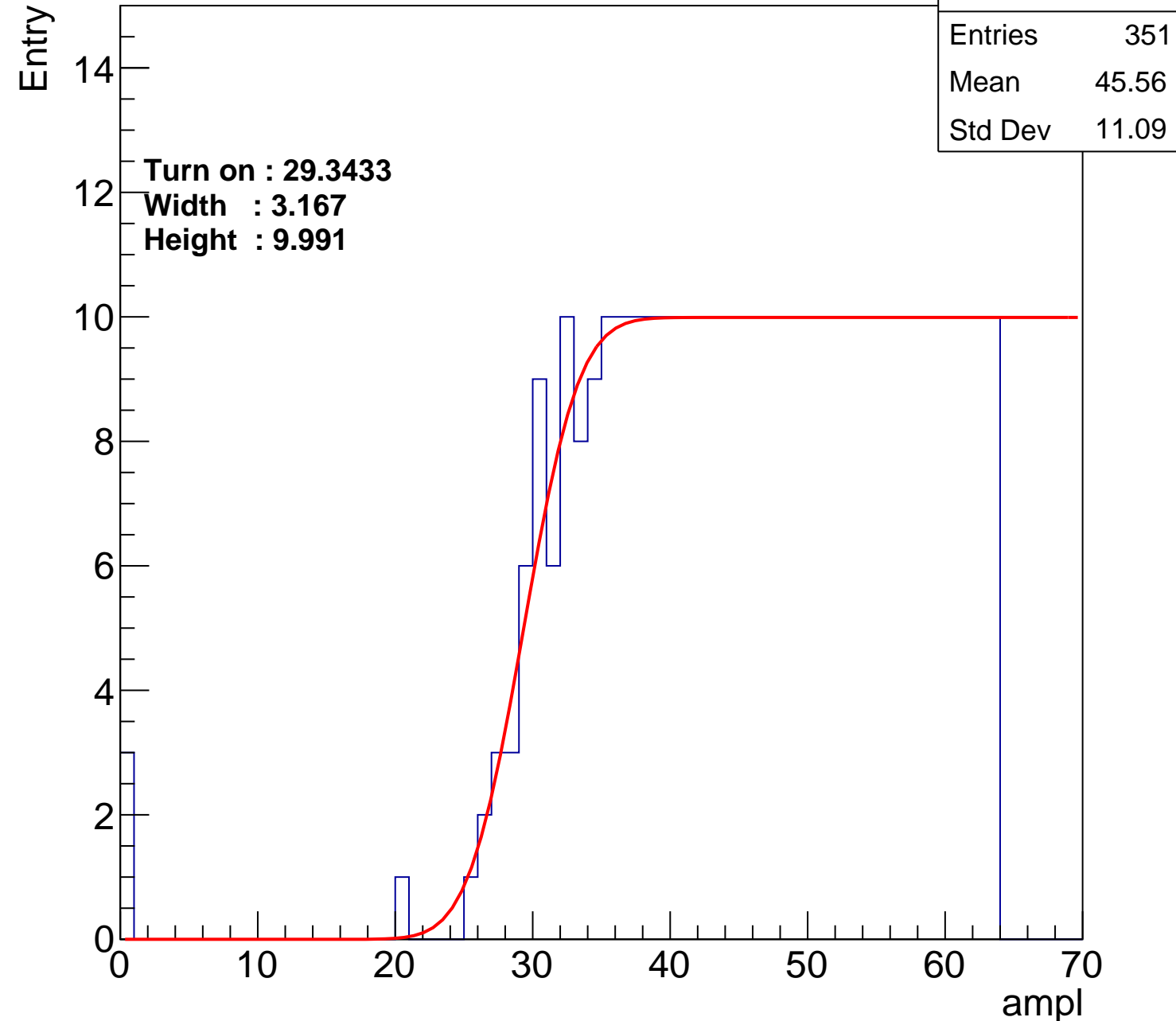
Width : 3.167

Height : 9.991

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch117

calib_packv5_042523_0143.root, FC#0, port D2

Entries	374
Mean	44.6
Std Dev	11.3

Turn on : 27.3811

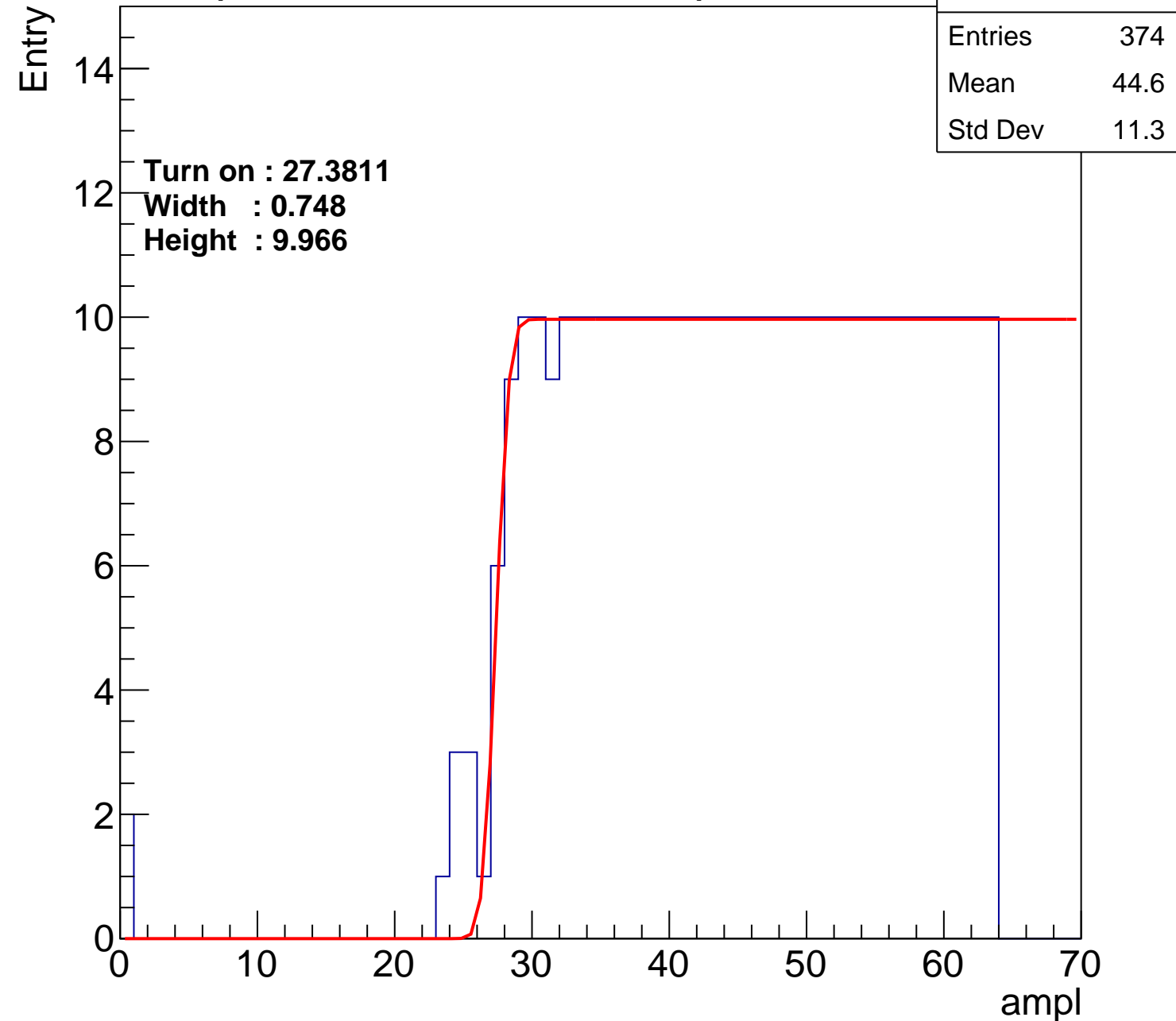
Width : 0.748

Height : 9.966

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch118

calib_packv5_042523_0143.root, FC#0, port D2

Entries	403
Mean	43.05
Std Dev	12.3

Turn on : 24.4375

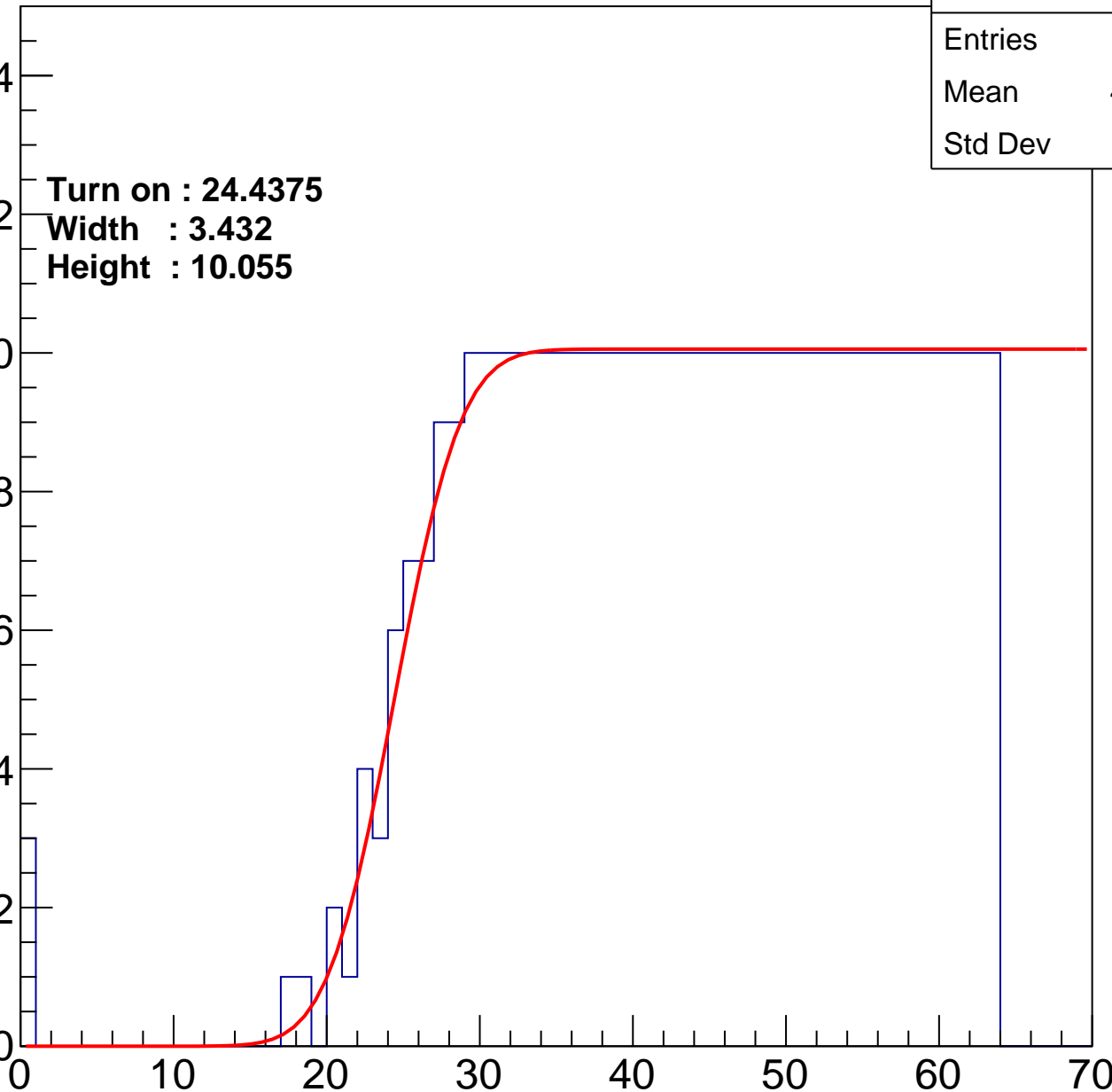
Width : 3.432

Height : 10.055

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch119

calib_packv5_042523_0143.root, FC#0, port D2

Entries	375
Mean	44.4
Std Dev	11.64

Turn on : 26.7654

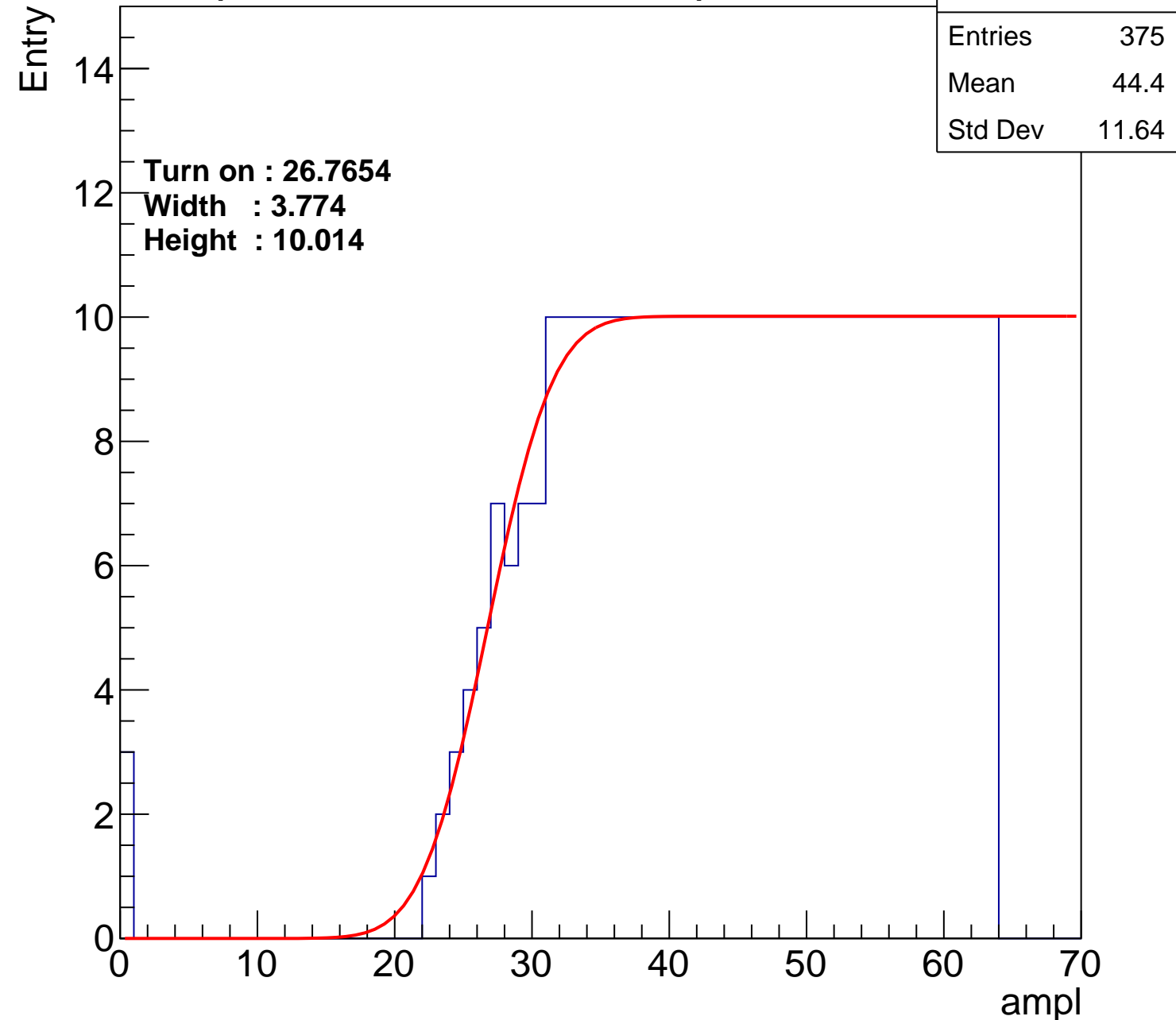
Width : 3.774

Height : 10.014

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch120

calib_packv5_042523_0143.root, FC#0, port D2

Entries	378
Mean	44.17
Std Dev	11.89

Turn on : 26.2388

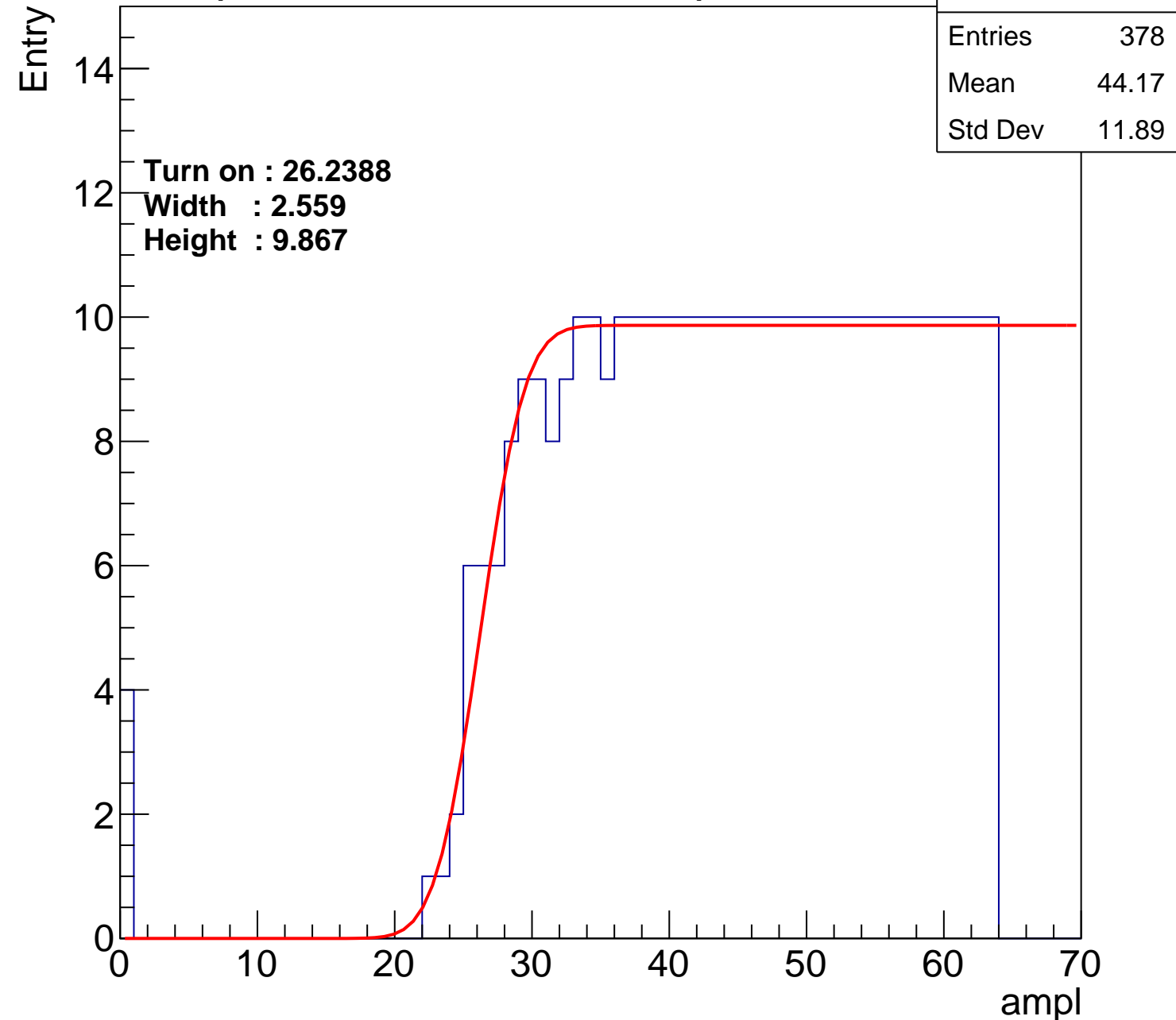
Width : 2.559

Height : 9.867

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch121

calib_packv5_042523_0143.root, FC#0, port D2

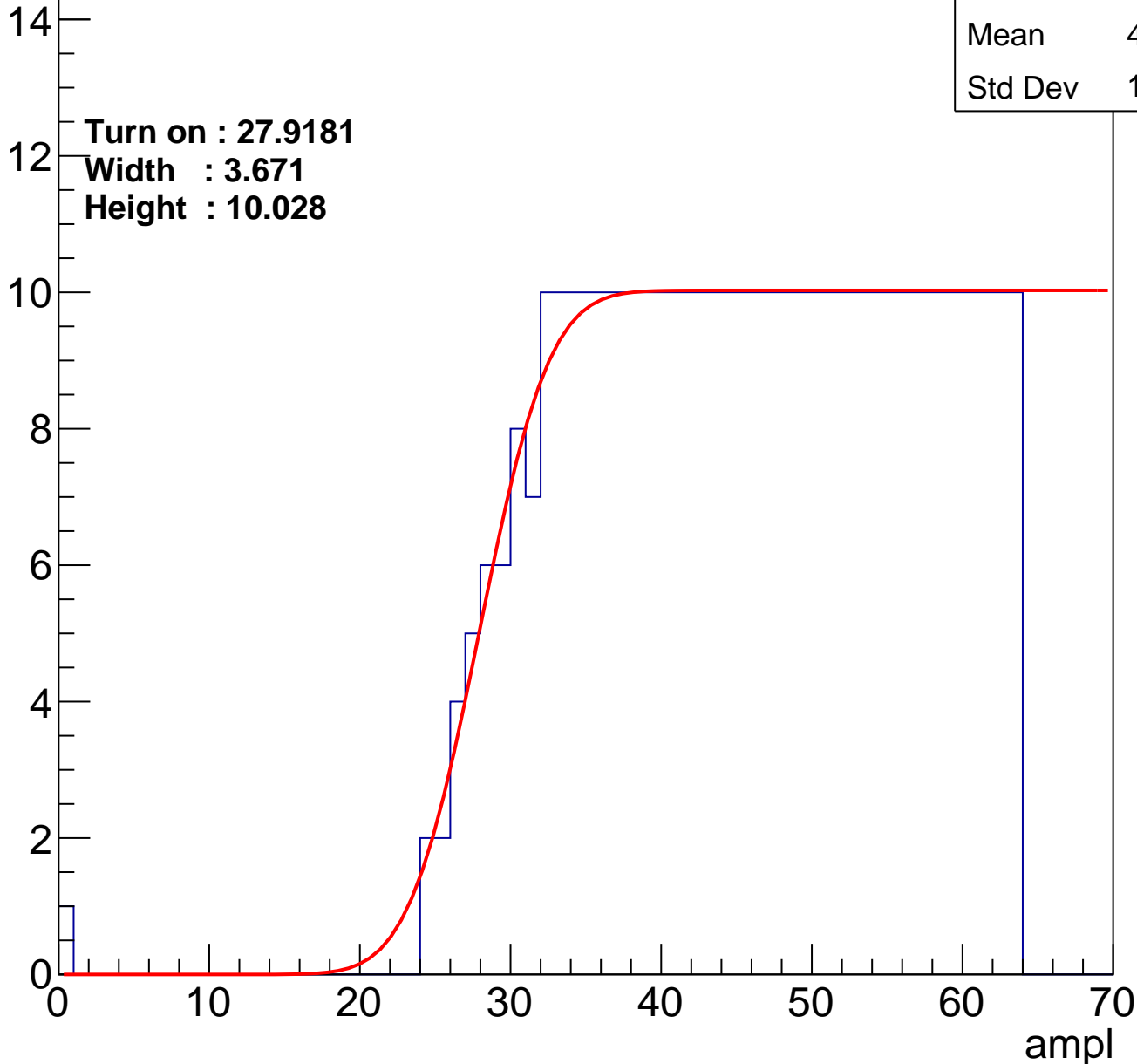
Entries	361
Mean	45.25
Std Dev	10.85

Turn on : 27.9181

Width : 3.671

Height : 10.028

Entry



B1L101S, U19-ch122

calib_packv5_042523_0143.root, FC#0, port D2

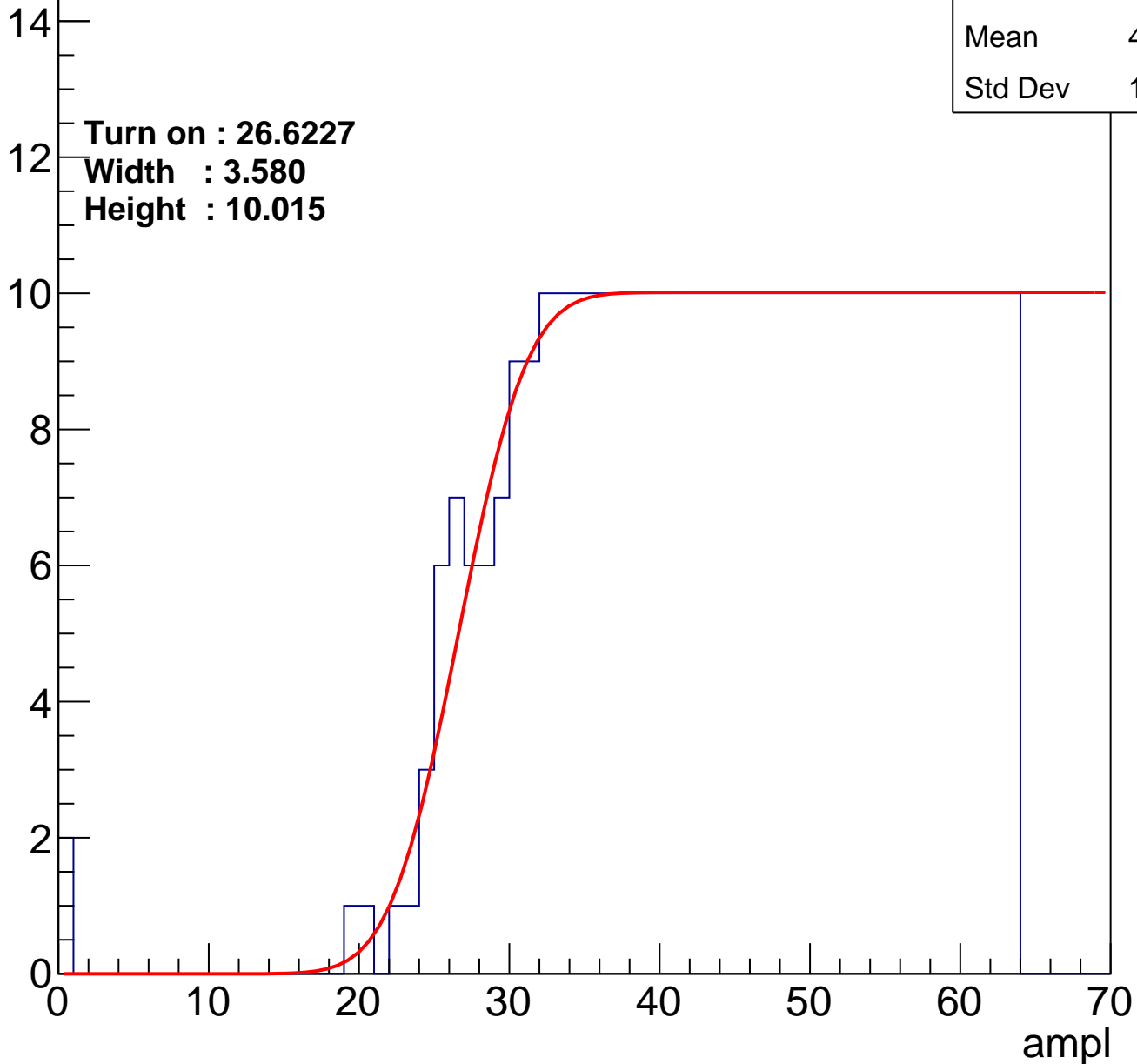
Entries	379
Mean	44.25
Std Dev	11.59

Turn on : 26.6227

Width : 3.580

Height : 10.015

Entry



B1L101S, U19-ch123

calib_packv5_042523_0143.root, FC#0, port D2

Entries	369
Mean	44.86
Std Dev	11.16

Turn on : 28.2432

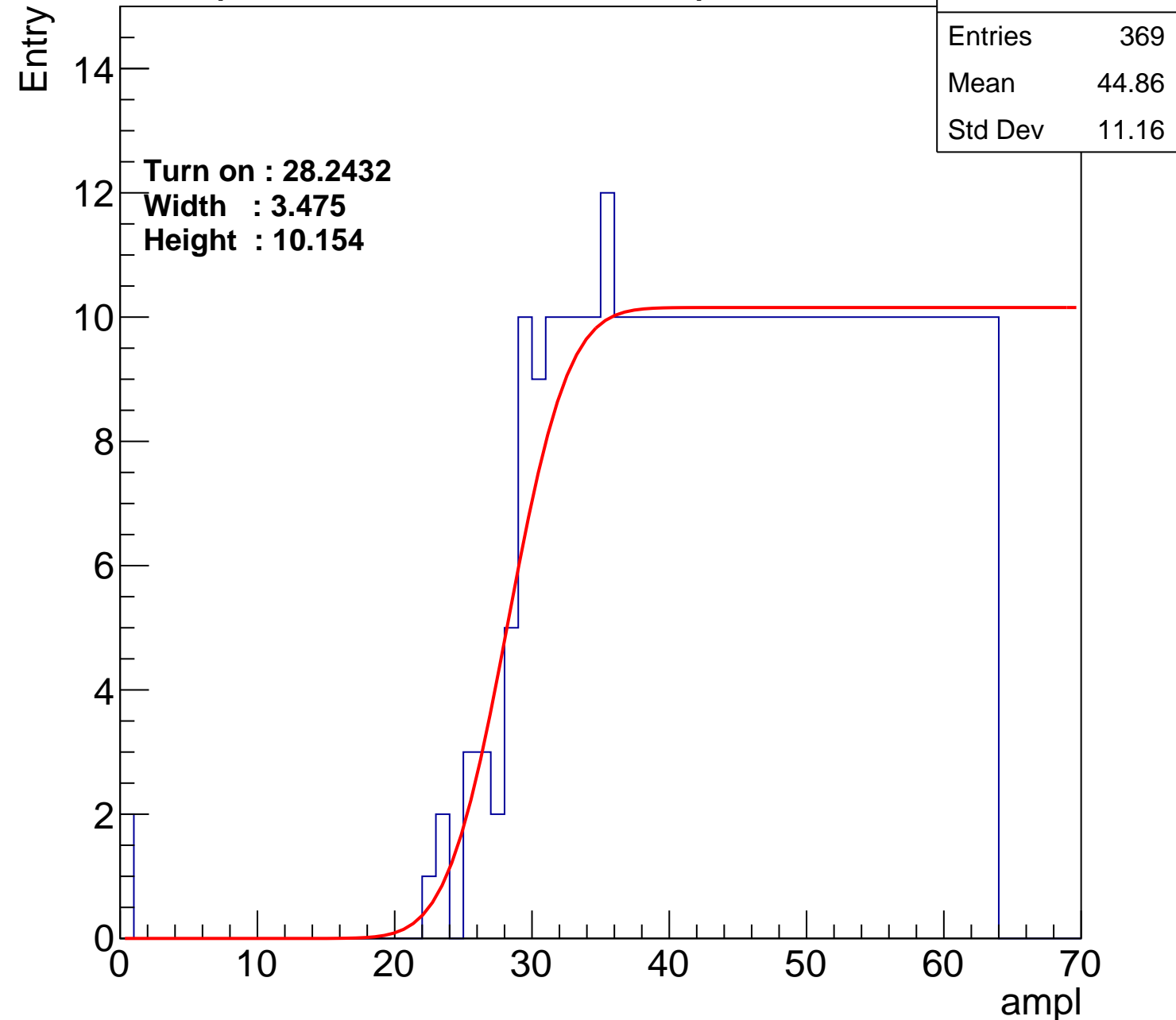
Width : 3.475

Height : 10.154

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch124

calib_packv5_042523_0143.root, FC#0, port D2

Entries	379
Mean	44.16
Std Dev	11.89

Turn on : 26.9147

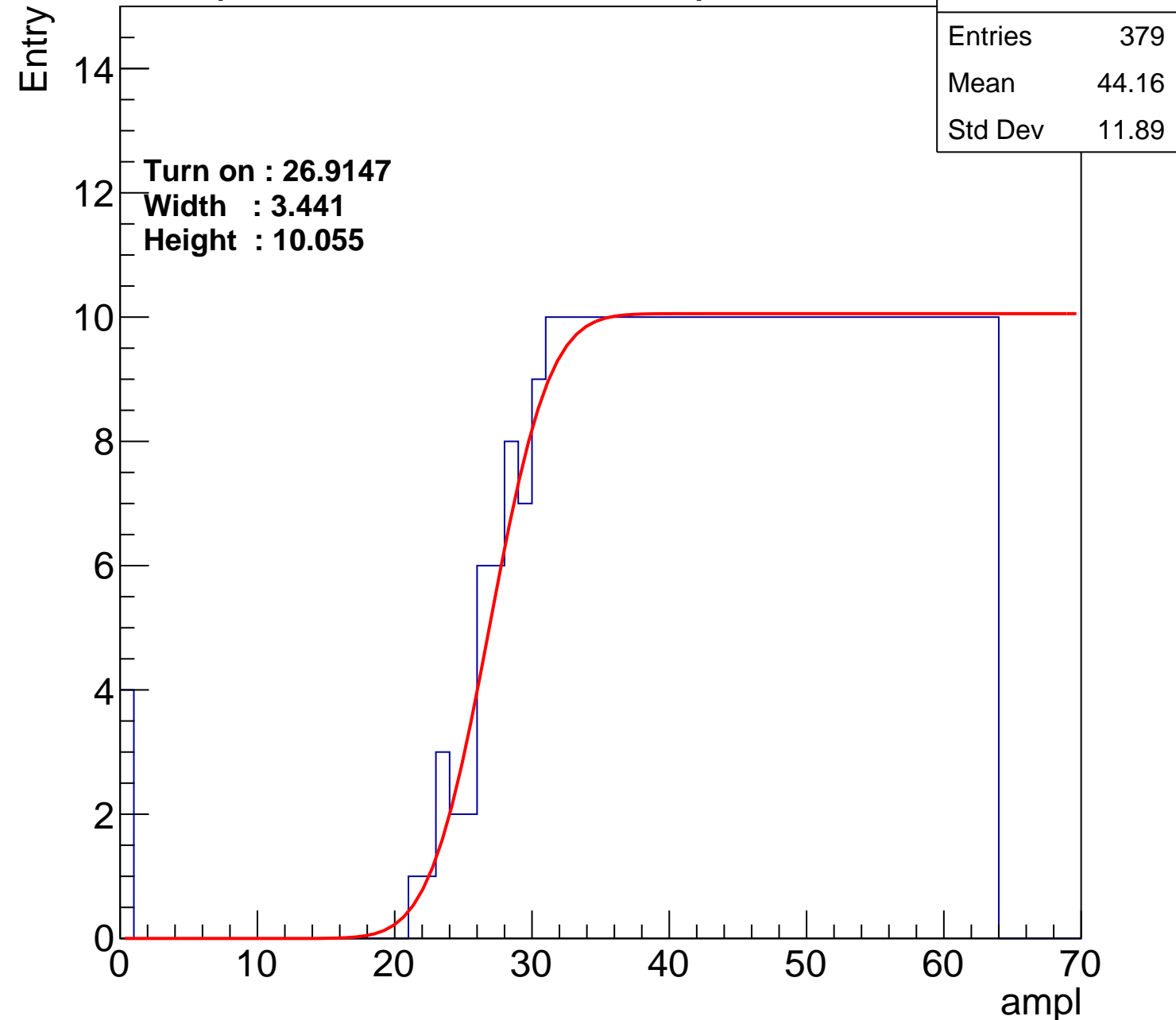
Width : 3.441

Height : 10.055

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch125

calib_packv5_042523_0143.root, FC#0, port D2

Entries	371
Mean	44.72
Std Dev	11.26

Turn on : 27.4067

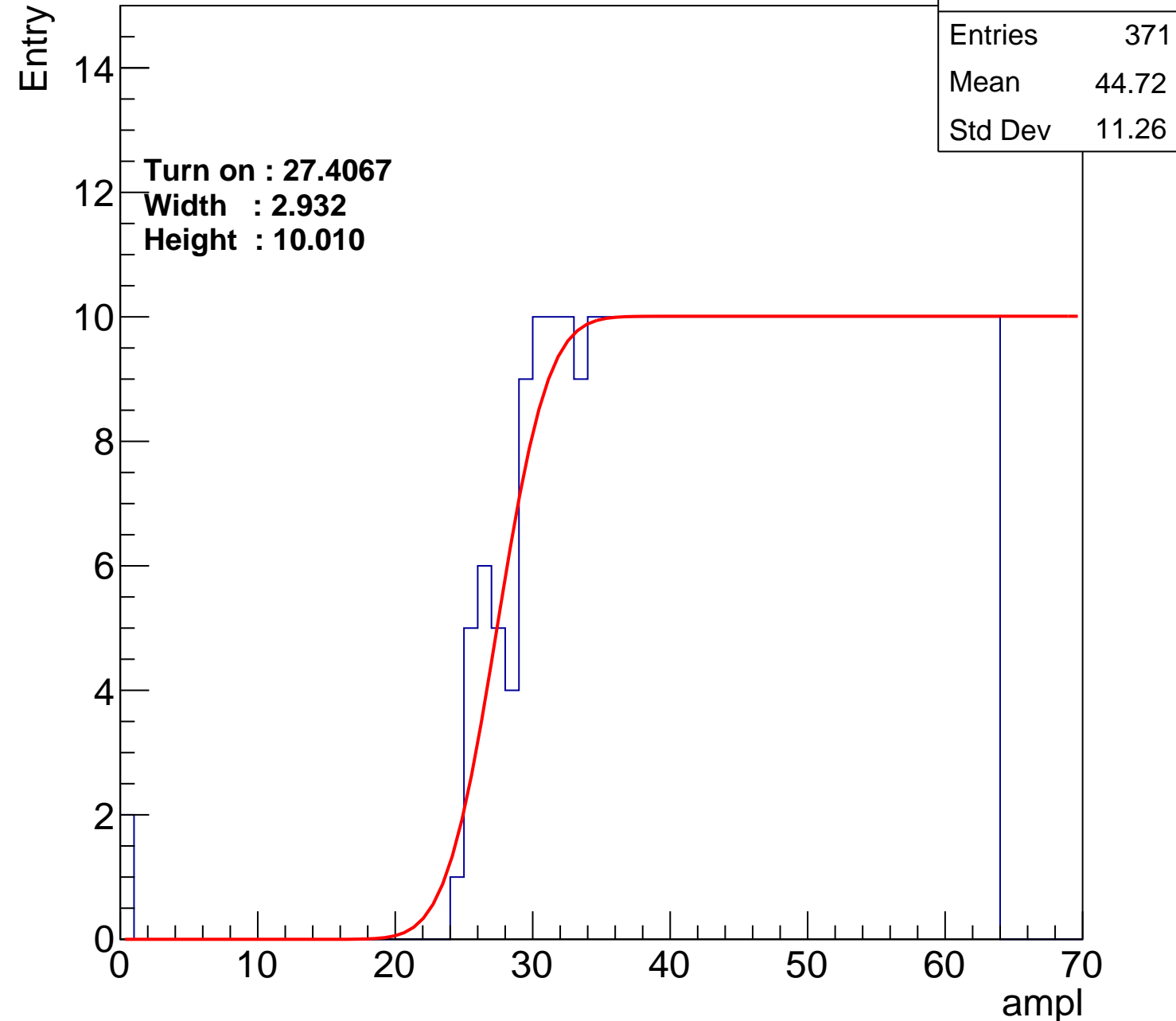
Width : 2.932

Height : 10.010

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch126

calib_packv5_042523_0143.root, FC#0, port D2

Entries	396
Mean	43.33
Std Dev	12.41

Turn on : 25.1325

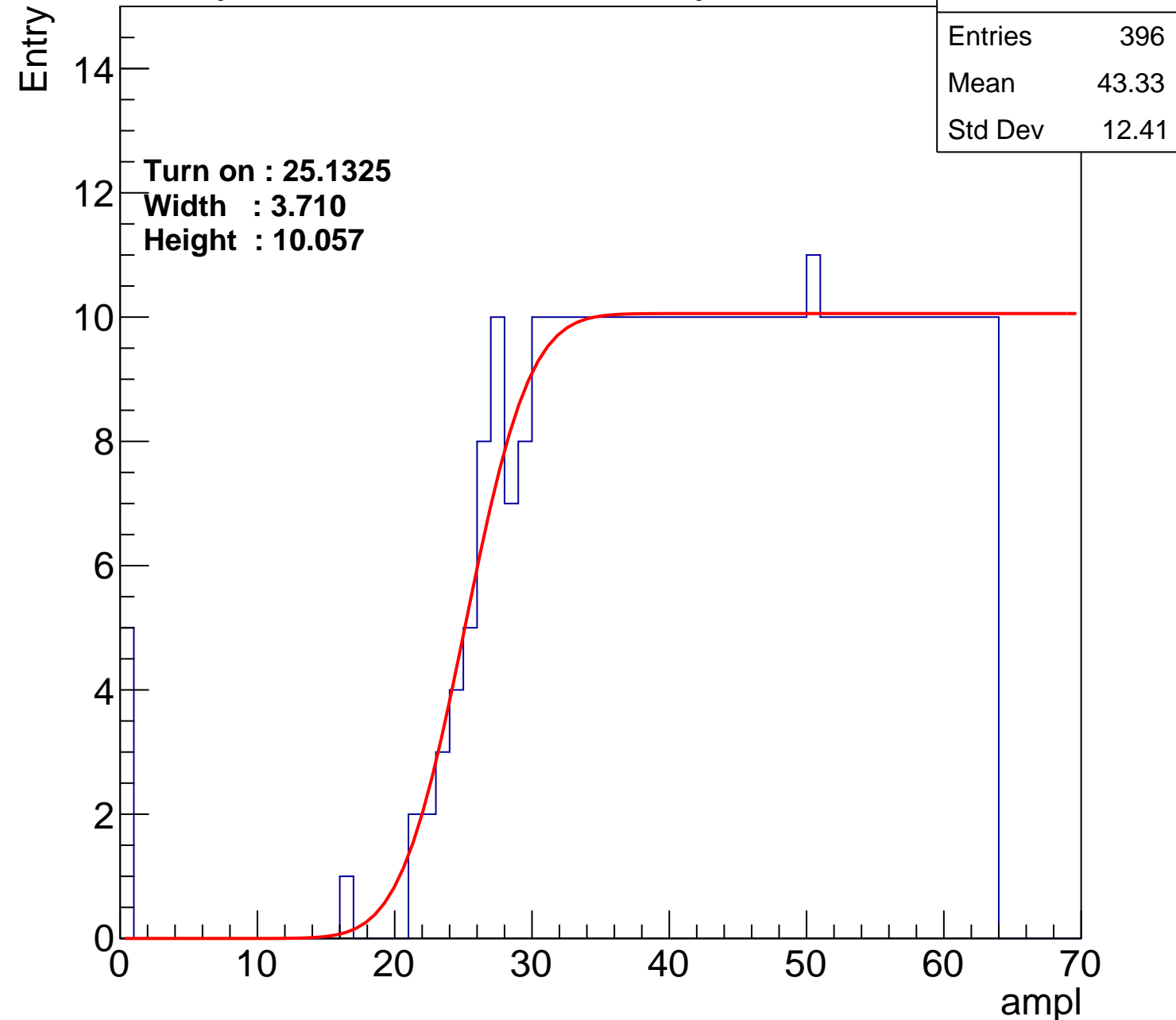
Width : 3.710

Height : 10.057

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U19-ch127

calib_packv5_042523_0143.root, FC#0, port D2

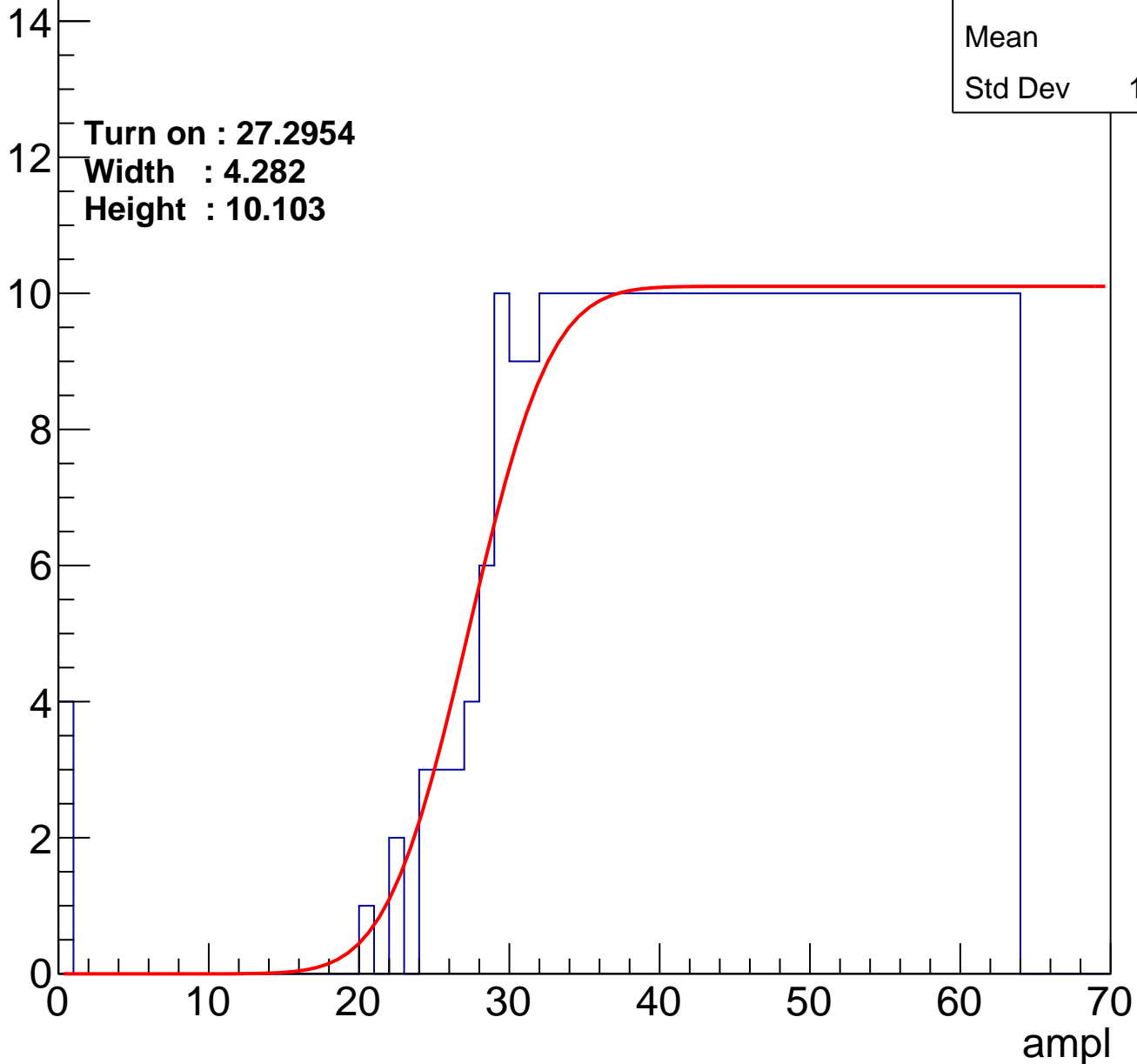
Entries	374
Mean	44.4
Std Dev	11.78

Turn on : 27.2954

Width : 4.282

Height : 10.103

Entry



B1L101S, U19-ch127

calib_packv5_042523_0143.root, FC#0, port D2

Entries	374
Mean	44.4
Std Dev	11.78

Turn on : 27.2954

Width : 4.282

Height : 10.103

Entry

