



# B1L103S, U4-ch0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	451
Mean	37.55
Std Dev	18.93

**Turn on : 26.5006**

**Width : 2.995**

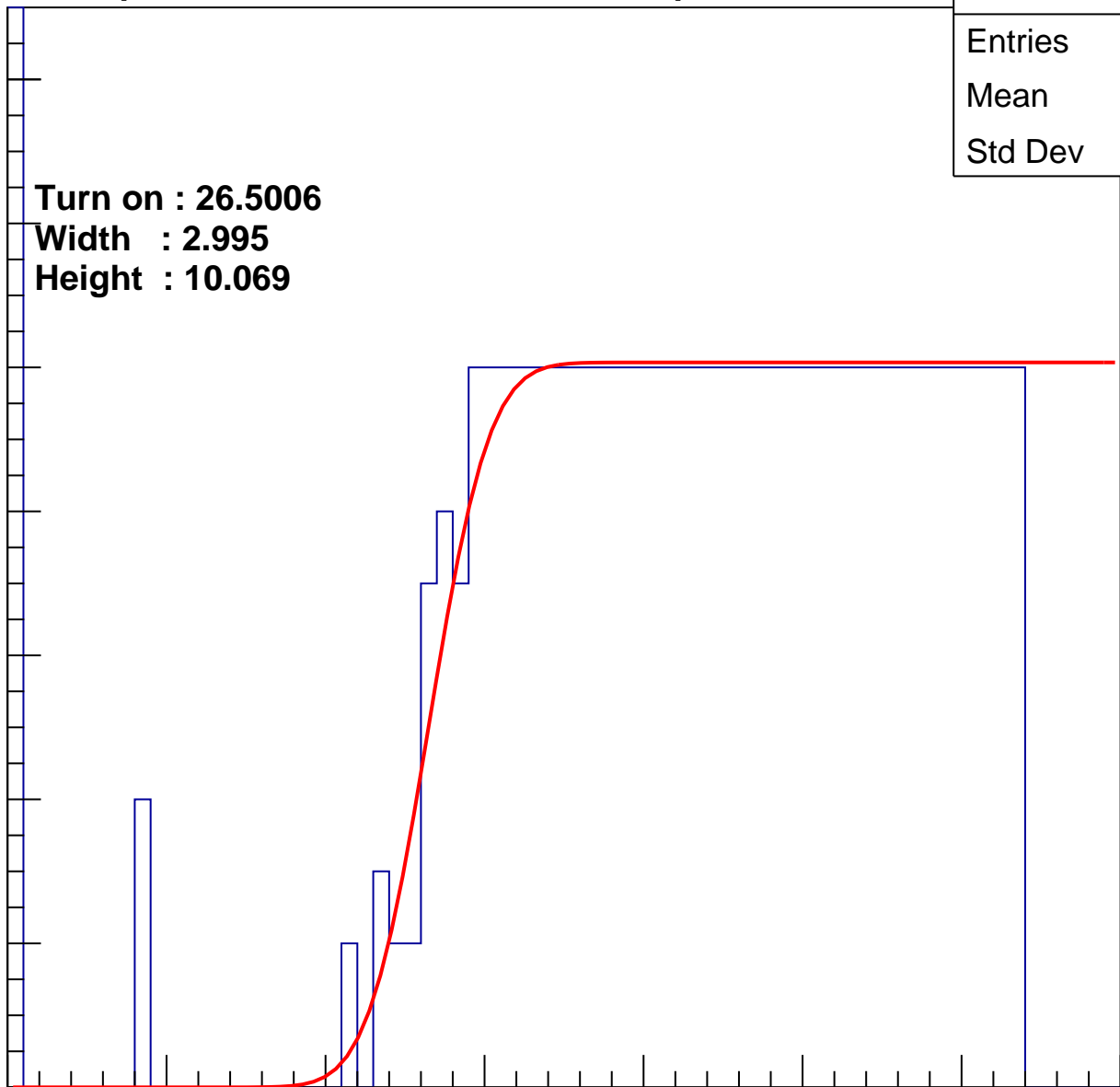
**Height : 10.069**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U4-ch1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	425
Mean	38.82
Std Dev	18.48

Turn on : 28.5123

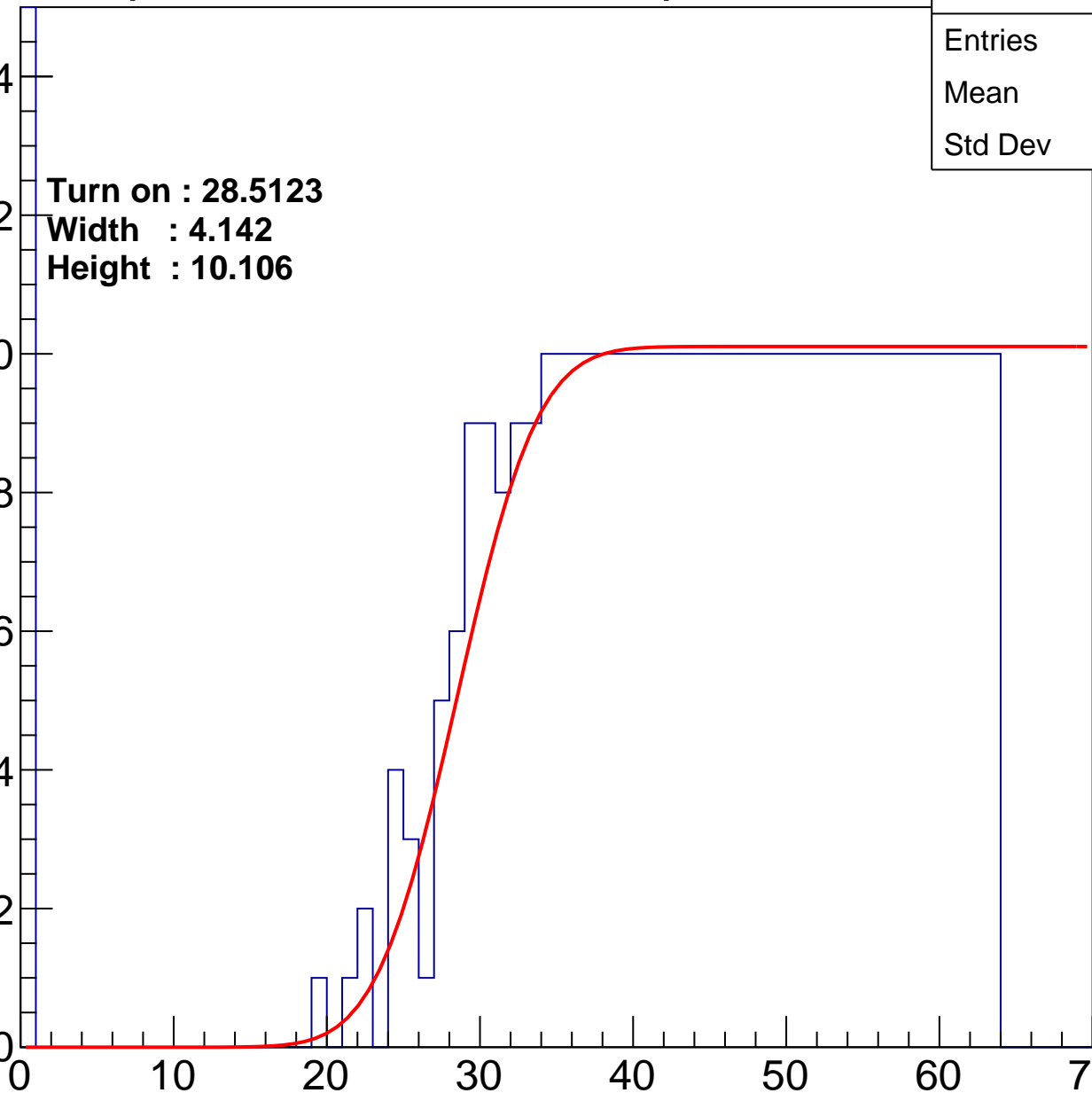
Width : 4.142

Height : 10.106

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	442
Mean	38.58
Std Dev	17.99

Turn on : 25.7896

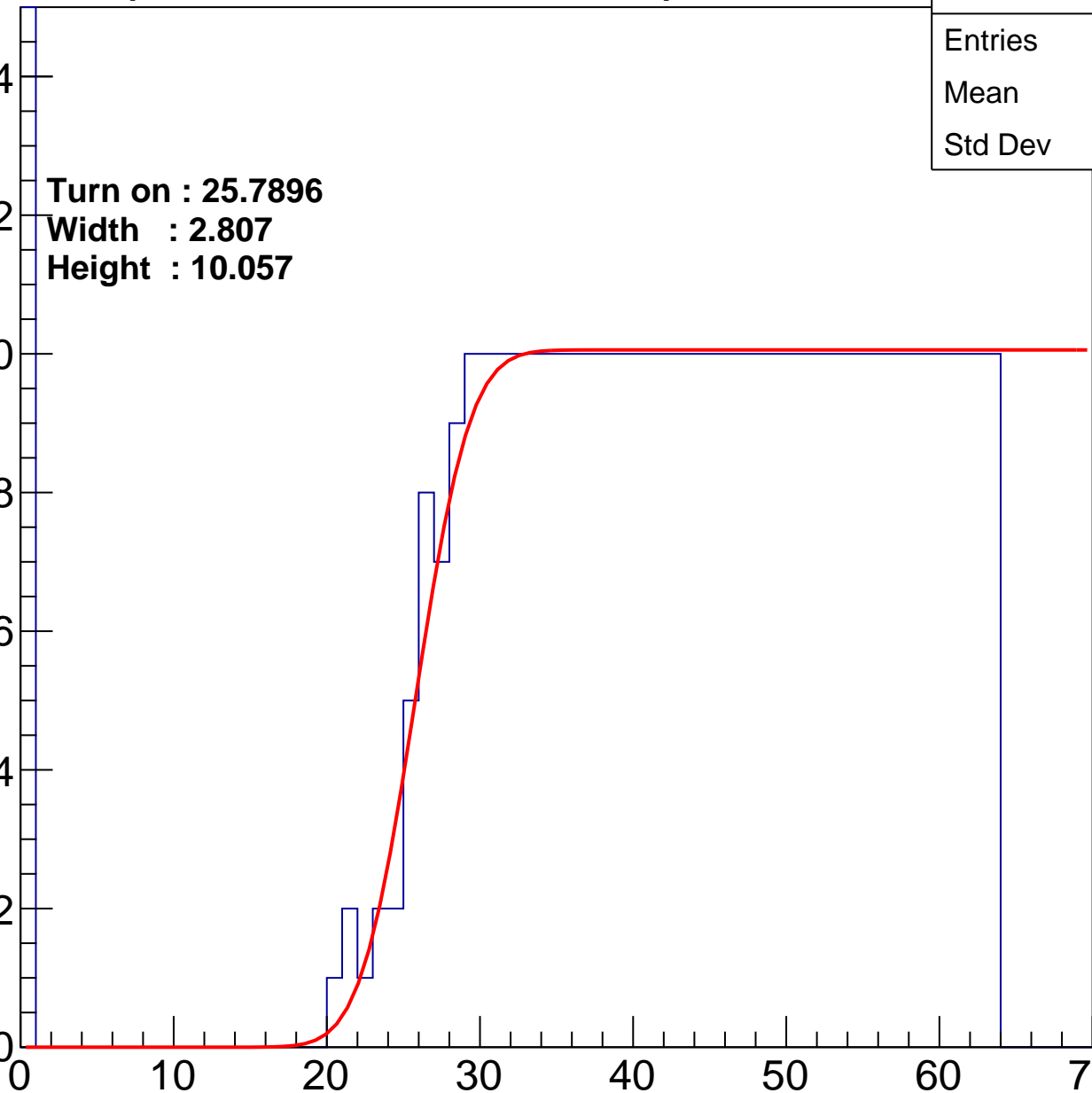
Width : 2.807

Height : 10.057

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch3

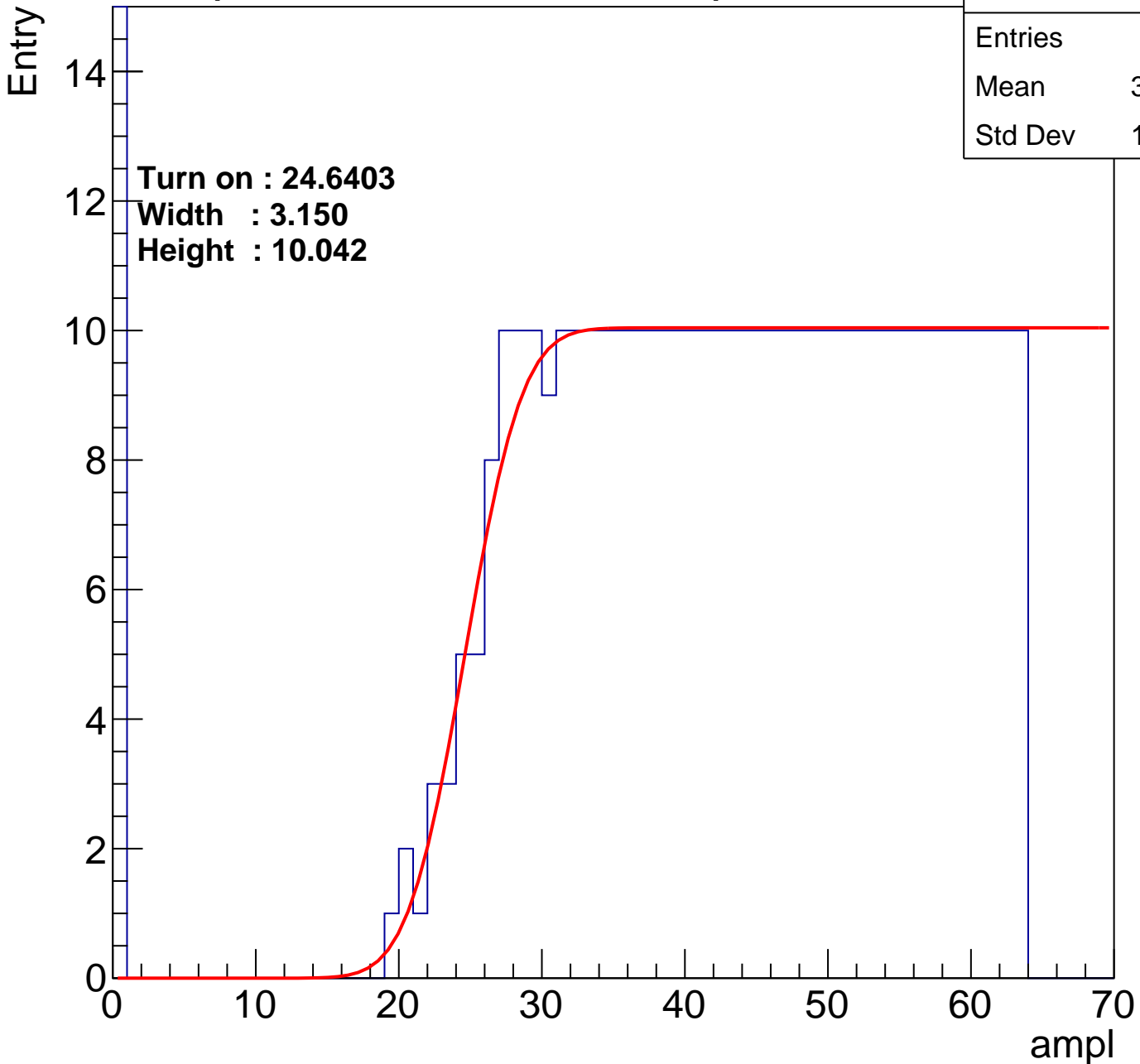
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	439
Mean	39.38
Std Dev	16.93

Turn on : 24.6403

Width : 3.150

Height : 10.042



# B1L103S, U4-ch4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	441
Mean	38.88
Std Dev	17.6

Turn on : 25.0810

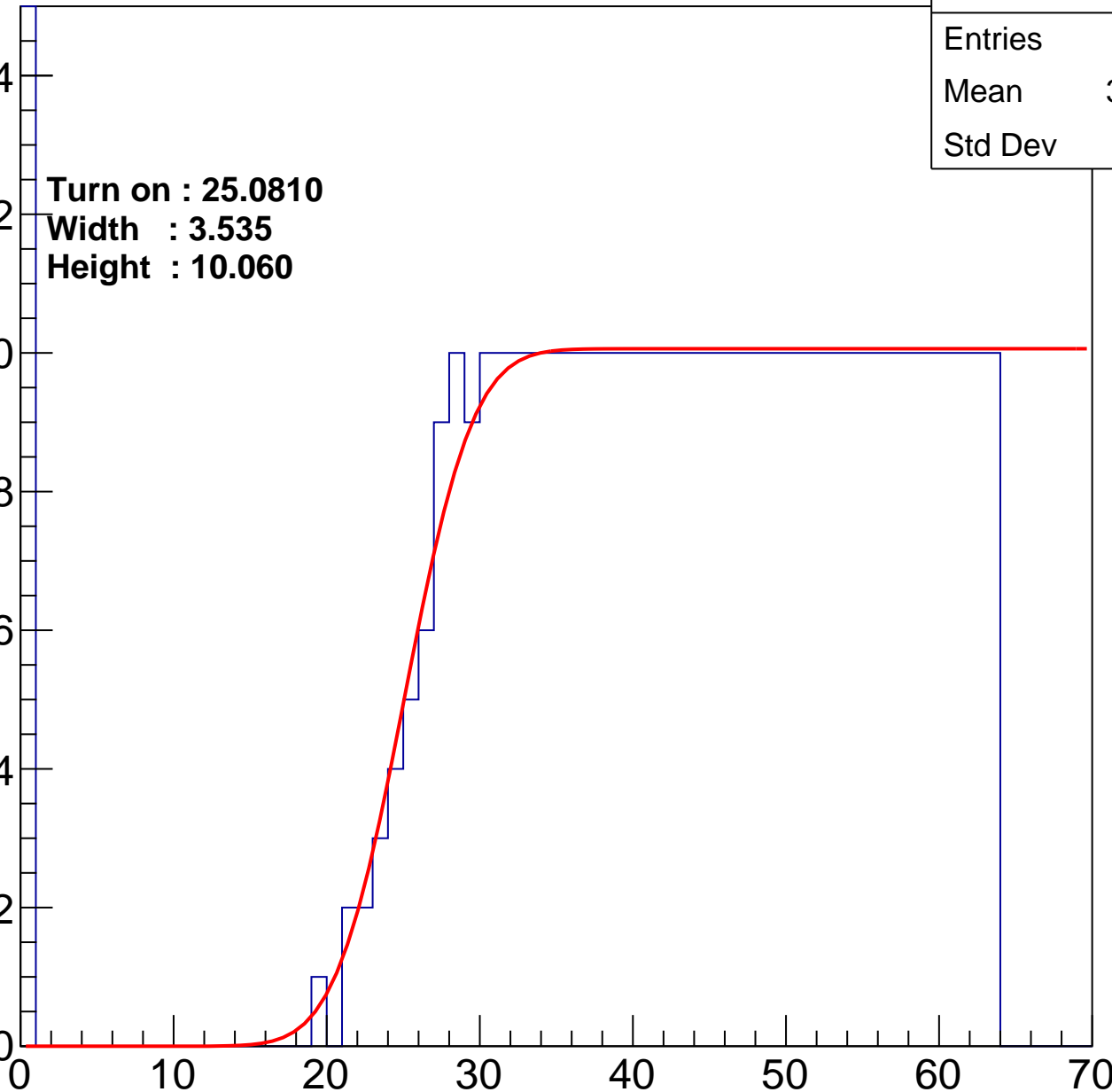
Width : 3.535

Height : 10.060

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	435
Mean	38.94
Std Dev	17.86

Turn on : 25.8713

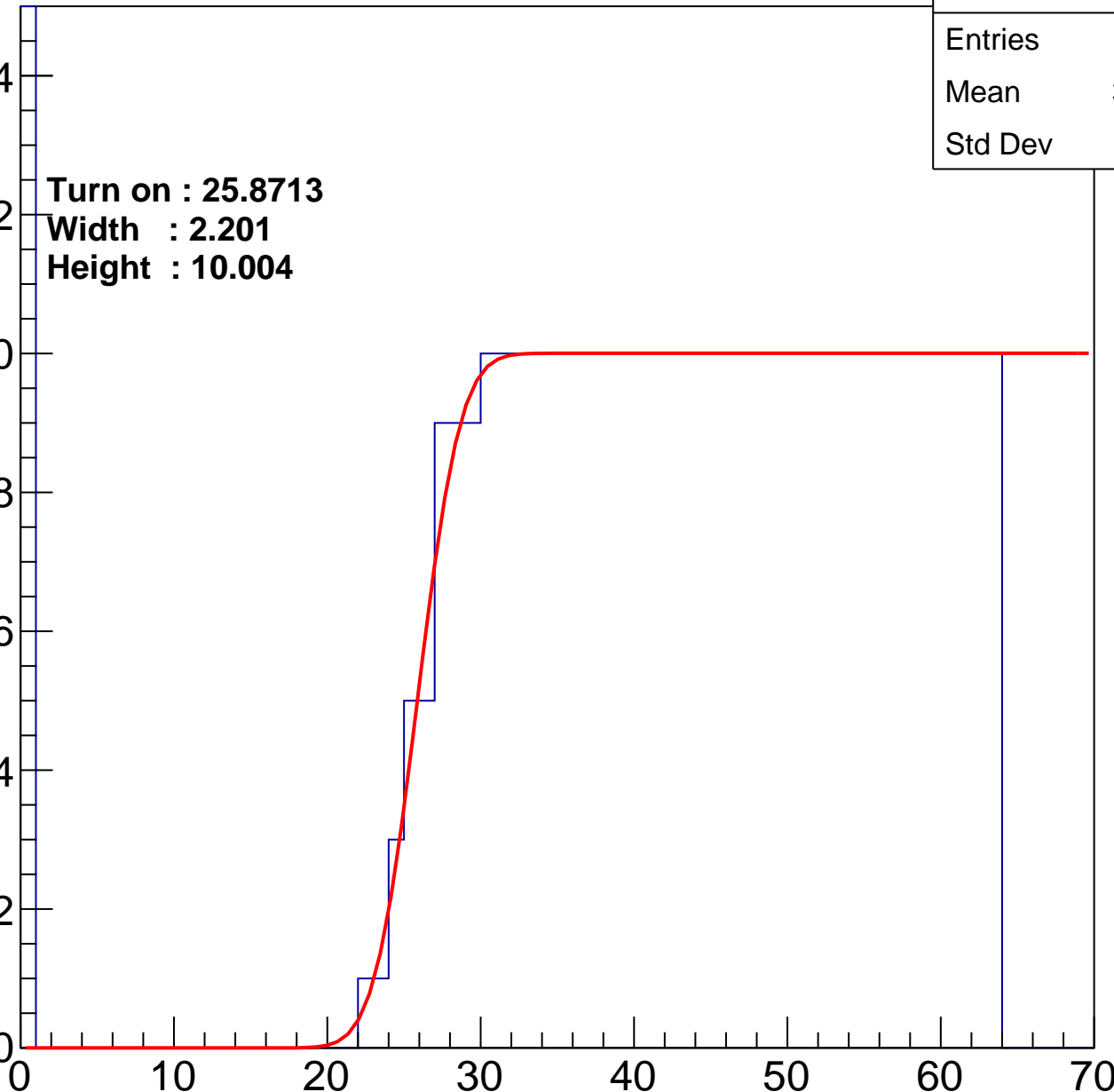
Width : 2.201

Height : 10.004

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	440
Mean	38.78
Std Dev	17.78

Turn on : 24.7500

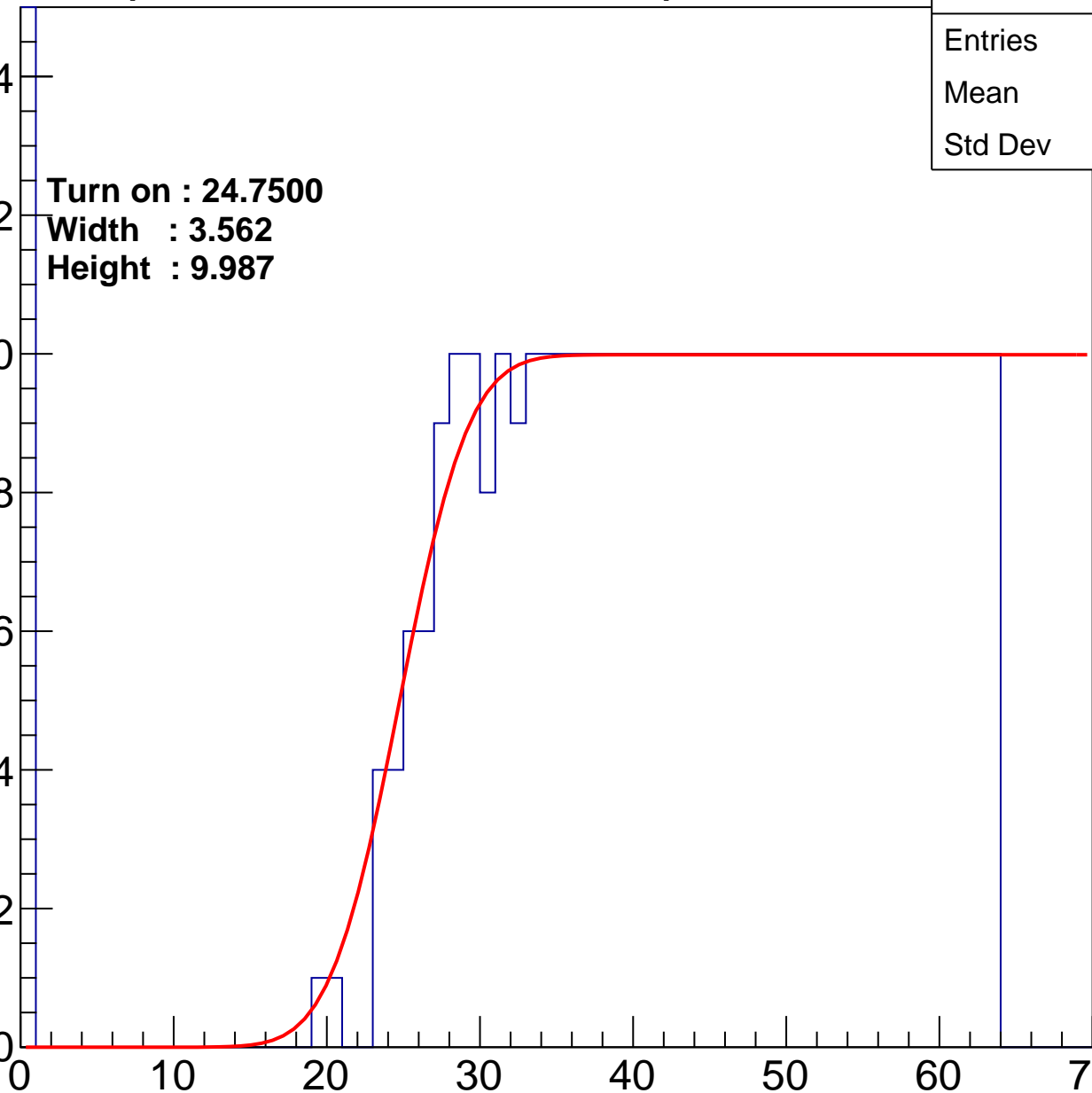
Width : 3.562

Height : 9.987

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L103S, U4-ch7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	429
Mean	39.08
Std Dev	17.91

**Turn on : 26.7353**

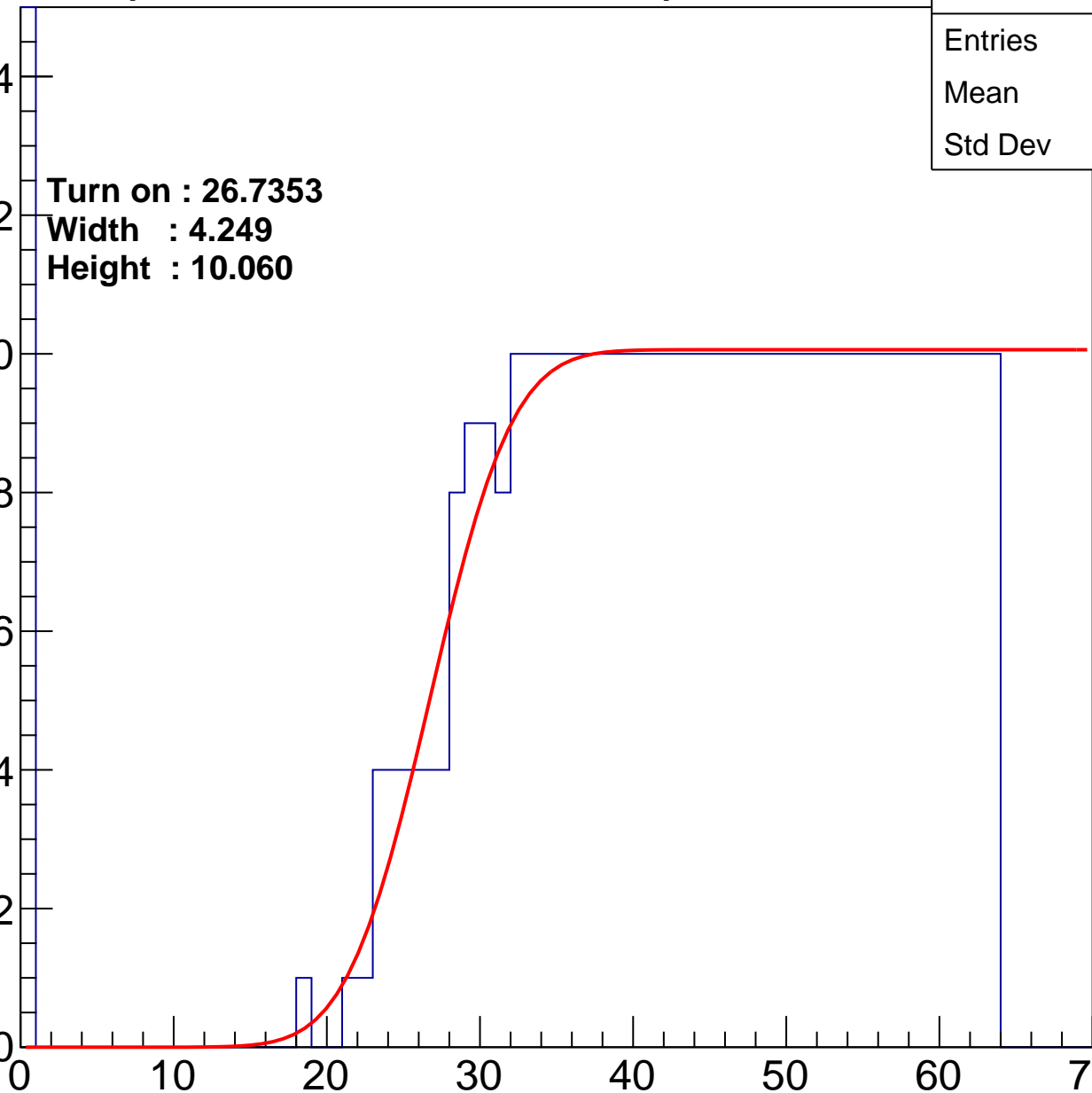
**Width : 4.249**

**Height : 10.060**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch8

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	432
Mean	38.97
Std Dev	17.93

**Turn on : 25.9257**

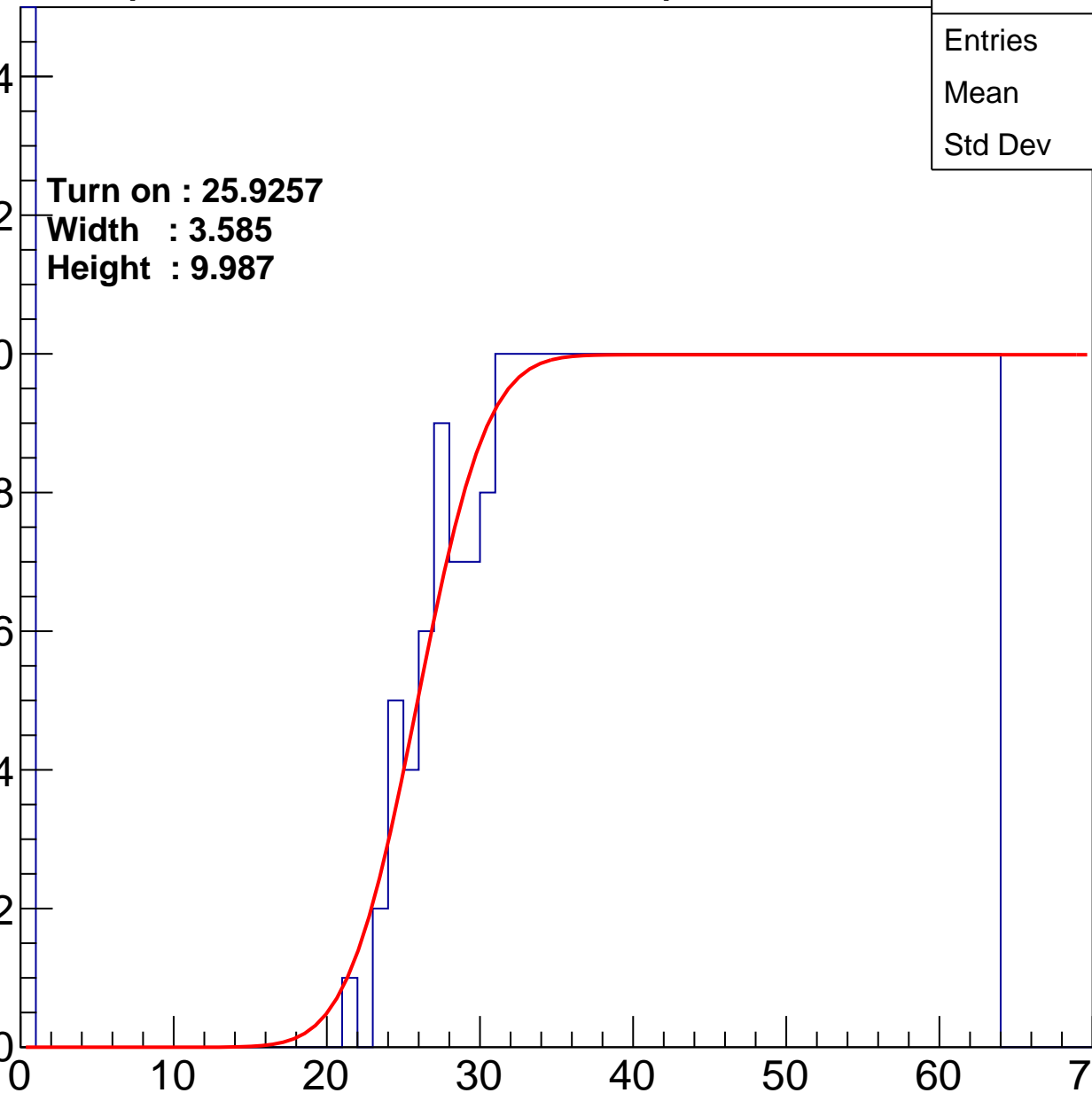
**Width : 3.585**

**Height : 9.987**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch9

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	423
Mean	39.77
Std Dev	17.21

Turn on : 26.1373

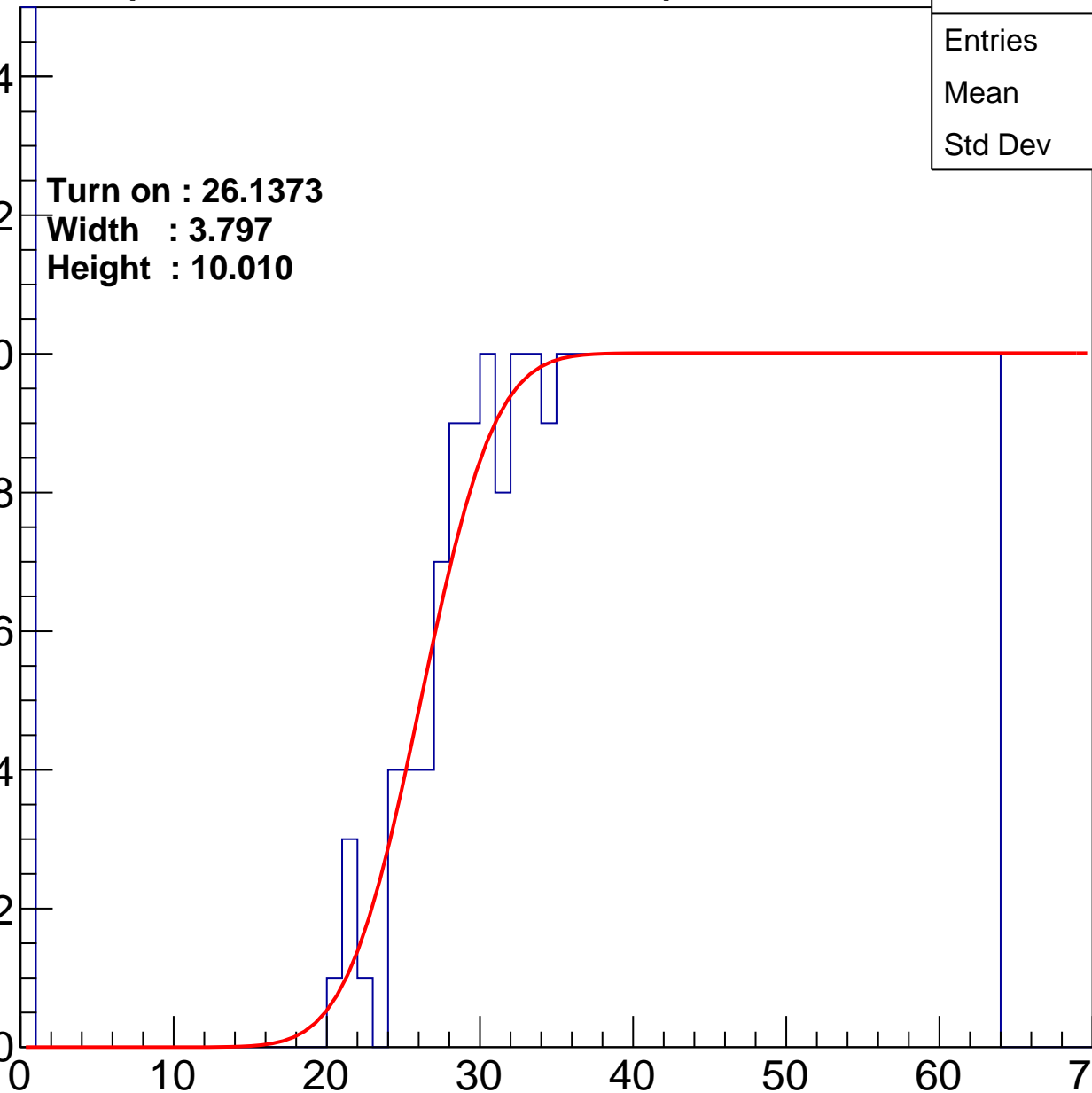
Width : 3.797

Height : 10.010

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch10

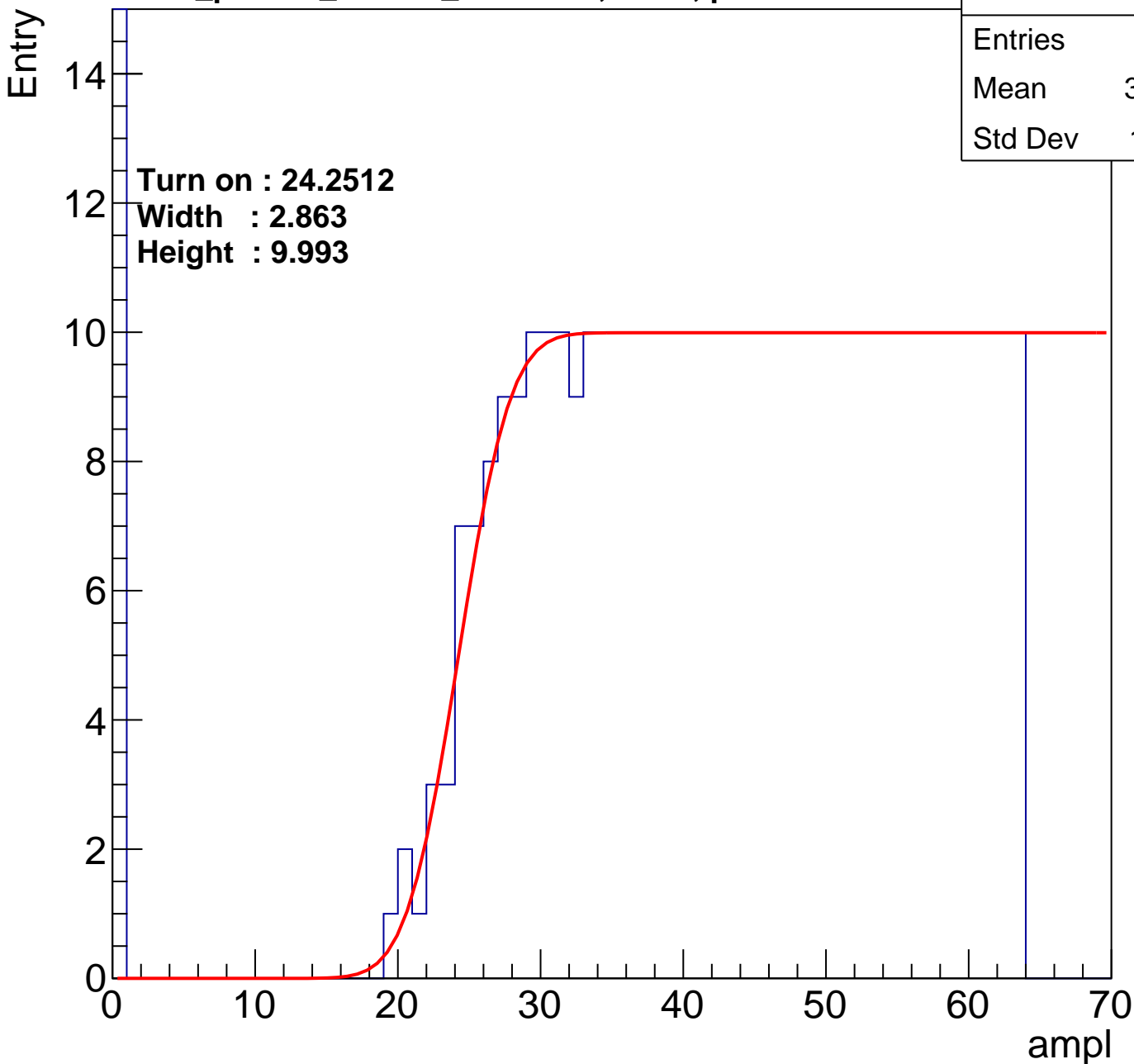
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	451
Mean	38.42
Std Dev	17.71

Turn on : 24.2512

Width : 2.863

Height : 9.993



# B1L103S, U4-ch11

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	405
Mean	40.55
Std Dev	17.09

**Turn on : 27.8582**

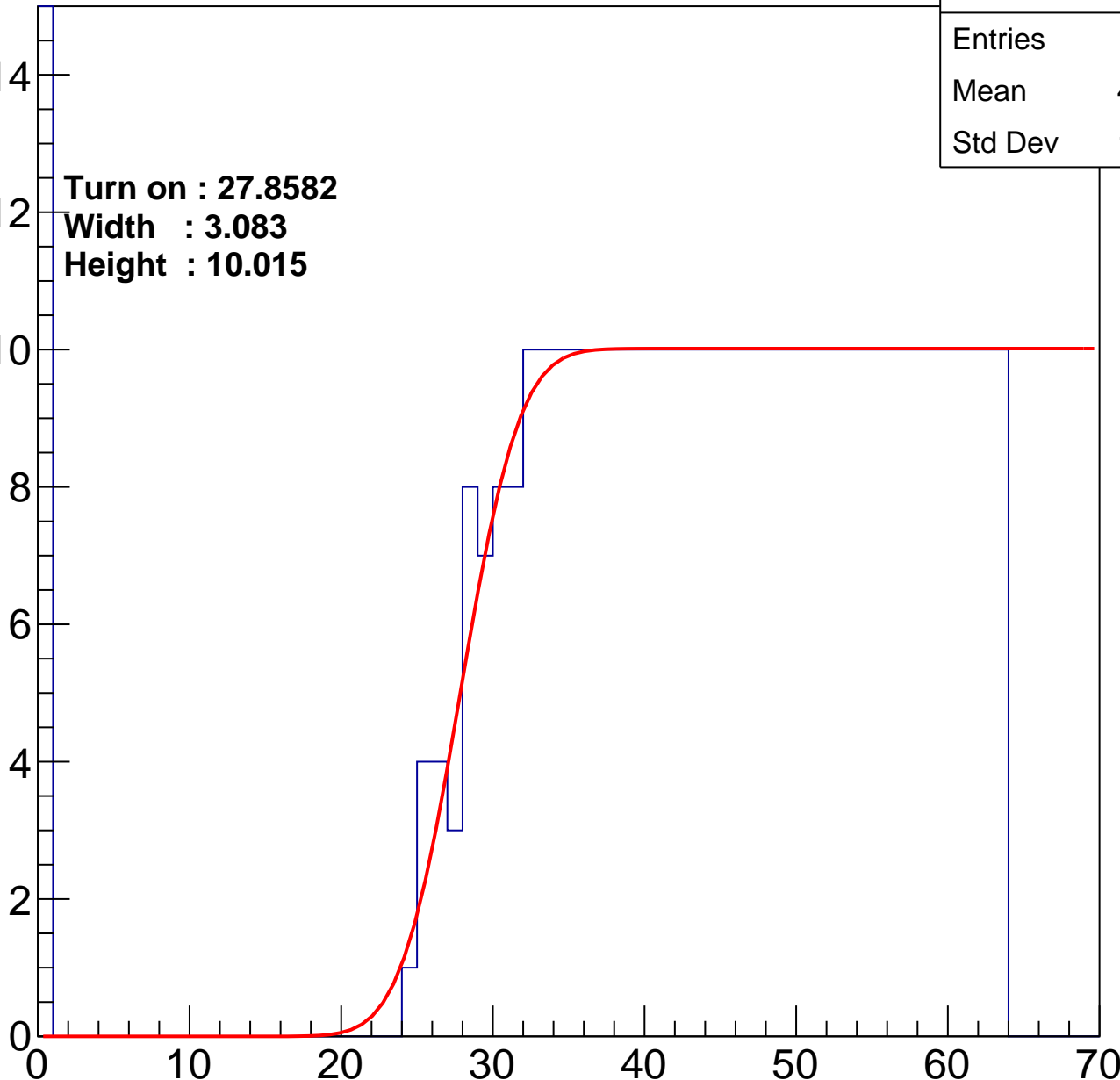
**Width : 3.083**

**Height : 10.015**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch12

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	443
Mean	38.87
Std Dev	17.5

**Turn on : 24.8400**

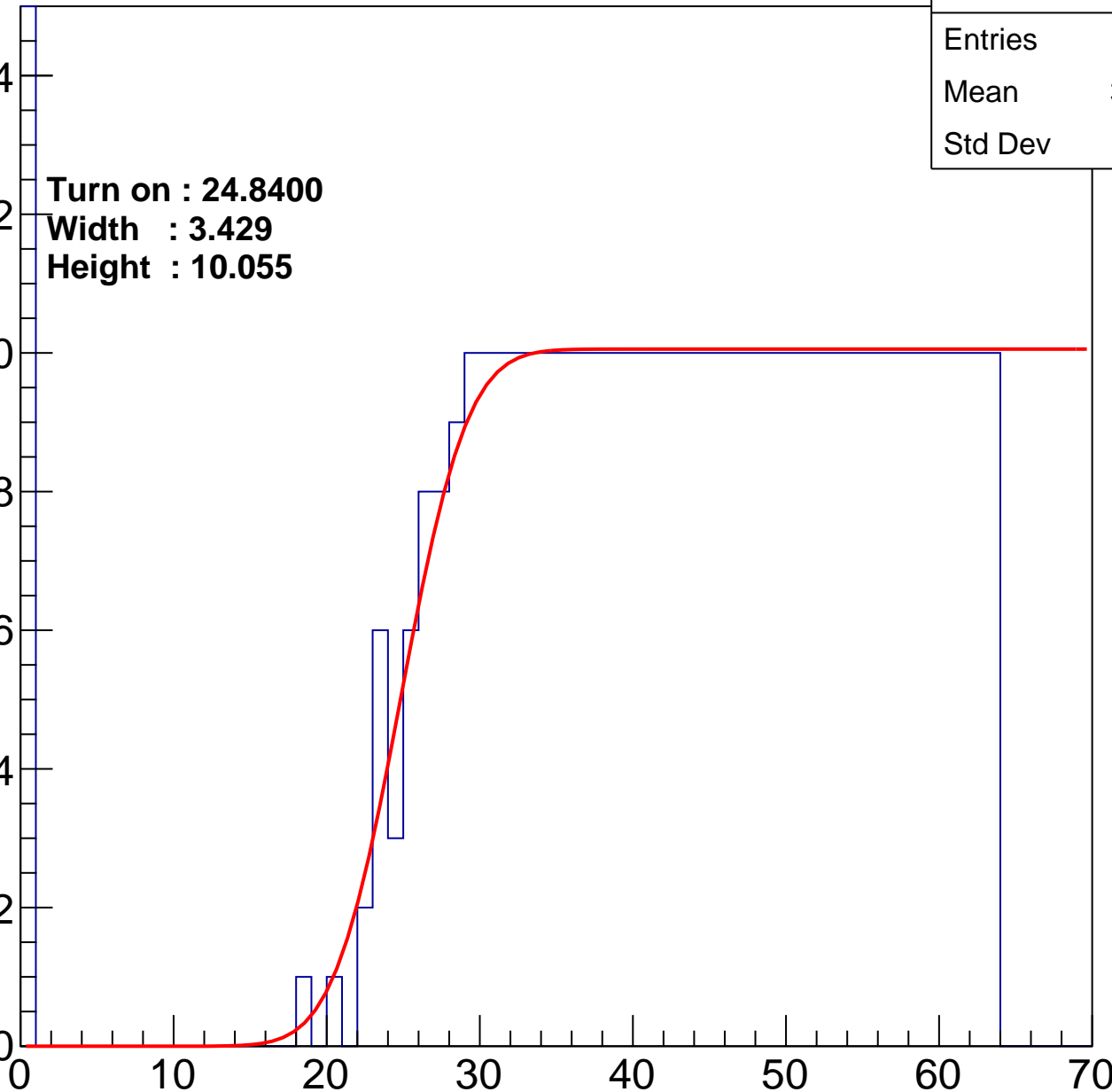
**Width : 3.429**

**Height : 10.055**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch13

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	406
Mean	39.94
Std Dev	17.93

**Turn on : 28.7658**

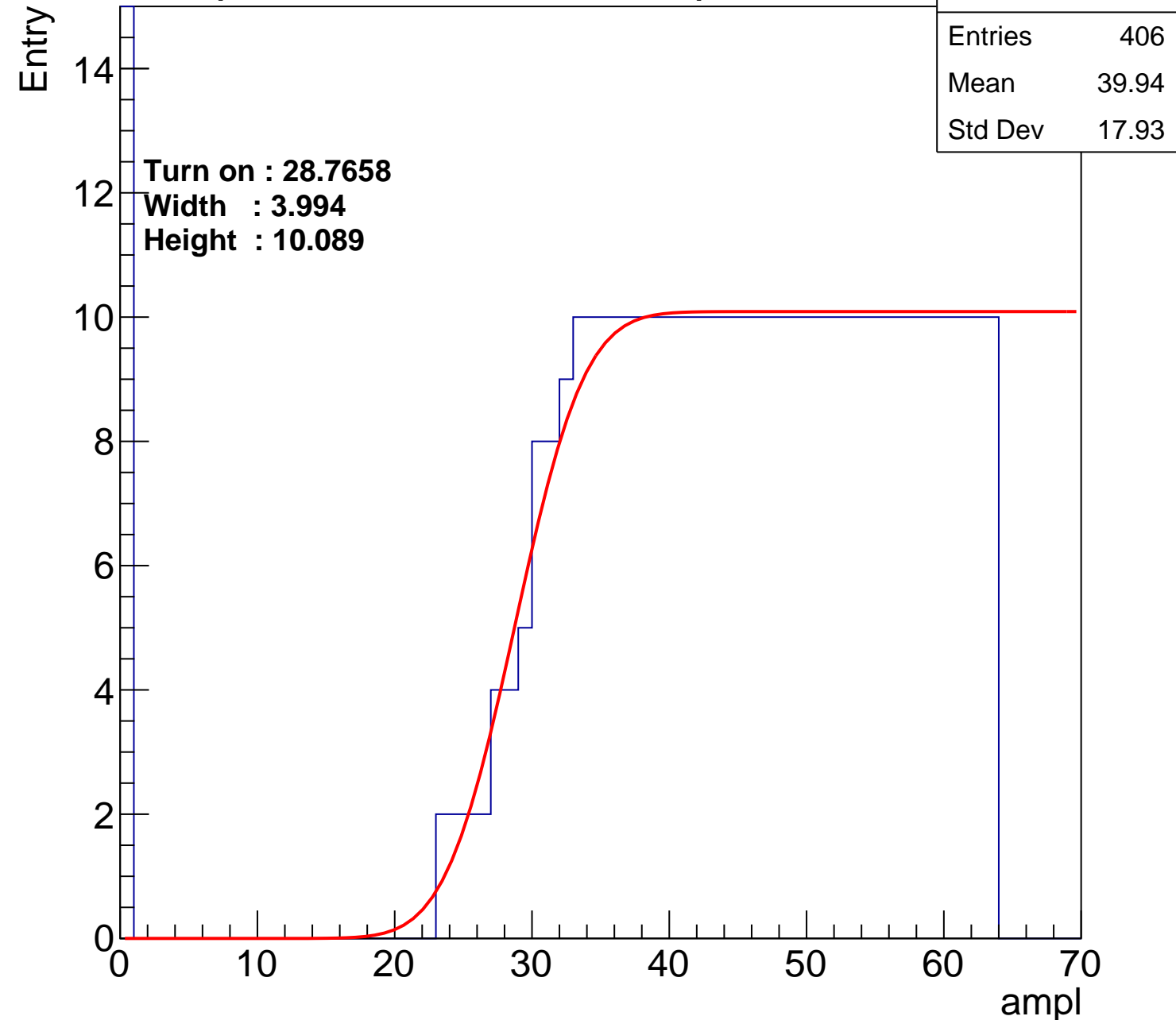
**Width : 3.994**

**Height : 10.089**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch14

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	451
Mean	37.81
Std Dev	18.61

Turn on : 24.4015

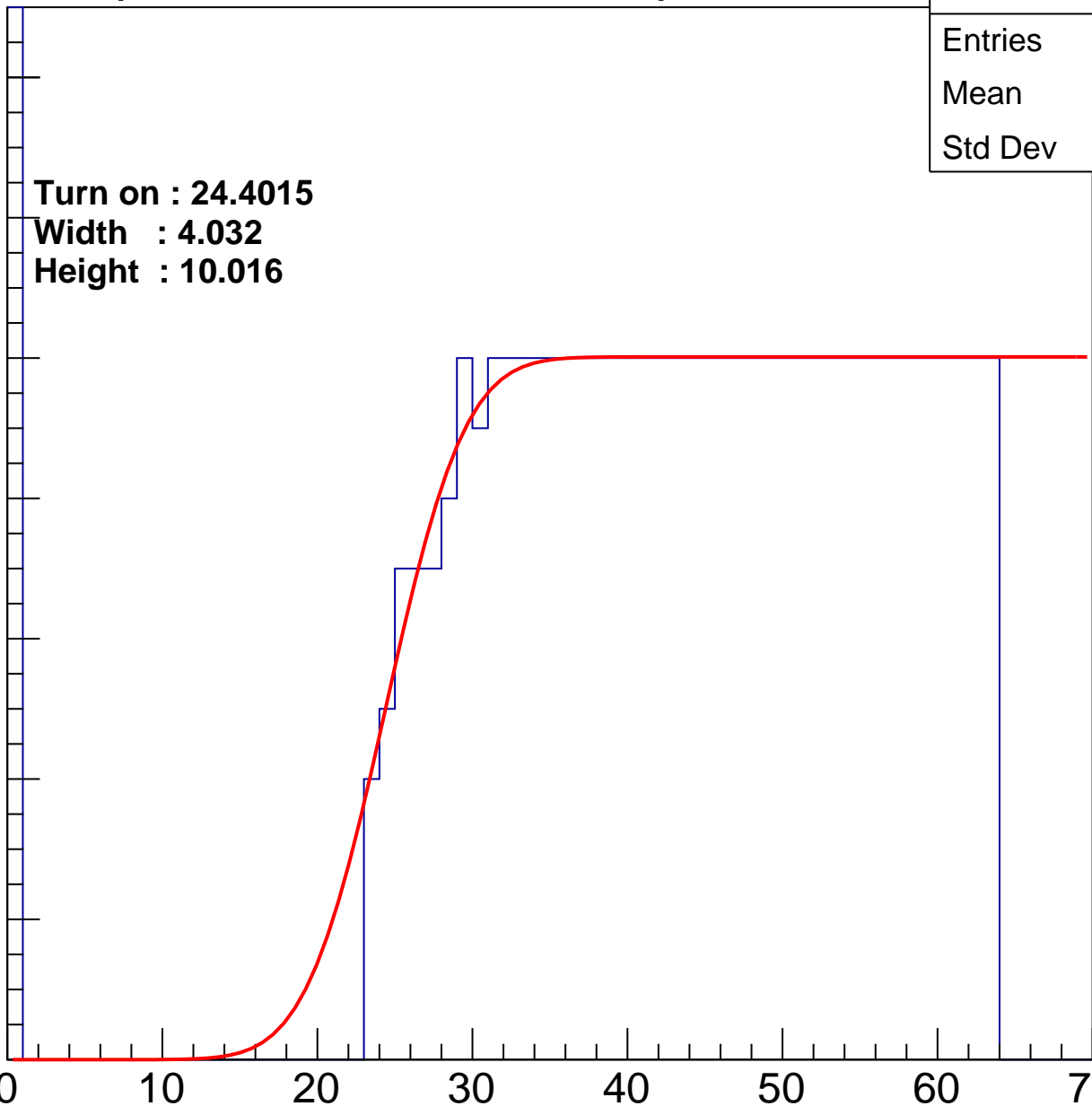
Width : 4.032

Height : 10.016

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L103S, U4-ch15

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	395
Mean	41.43
Std Dev	16.28

**Turn on : 28.8553**

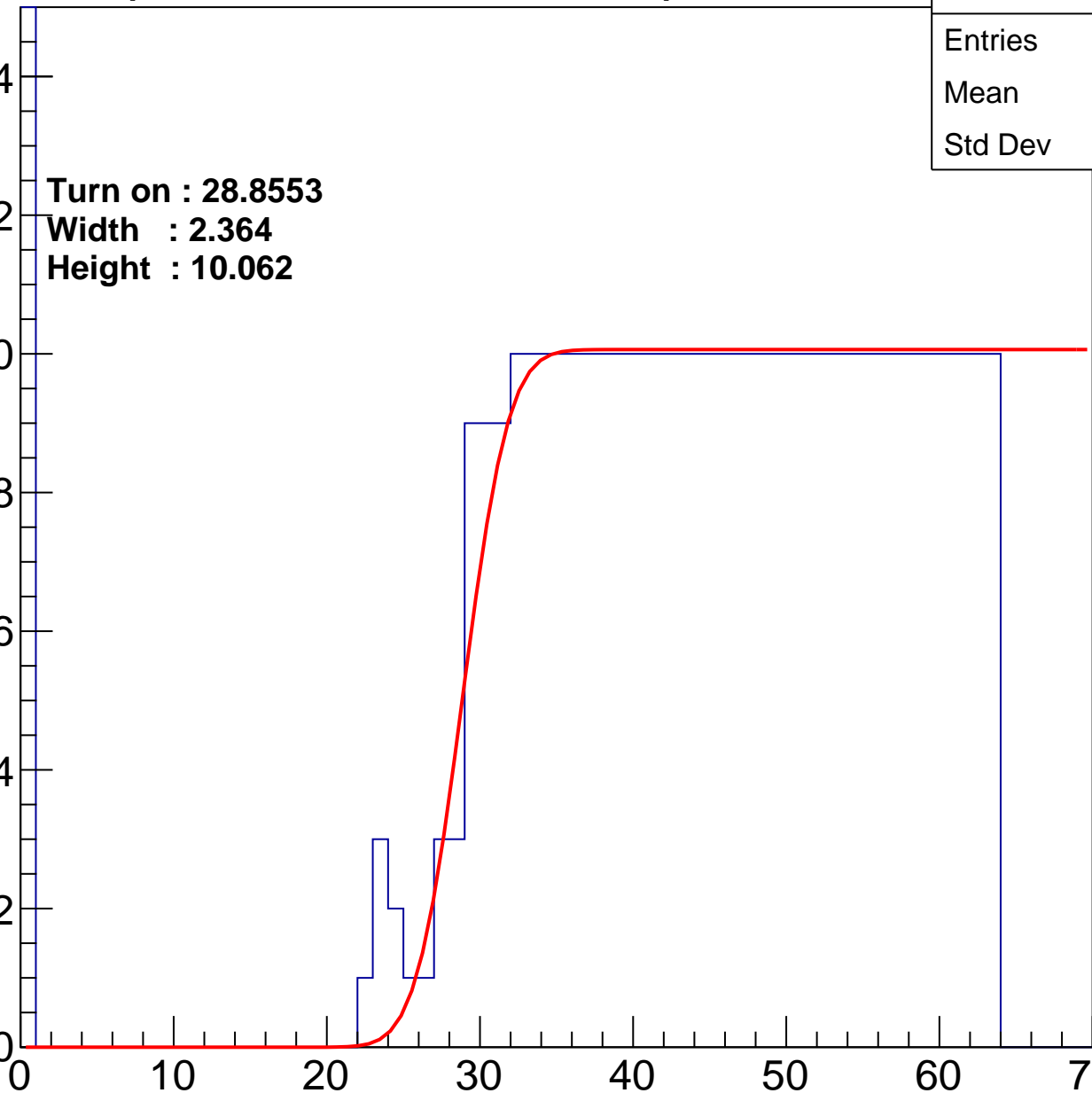
**Width : 2.364**

**Height : 10.062**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch16

calib\_packv5\_041523\_1651.root, FC#0, port C2

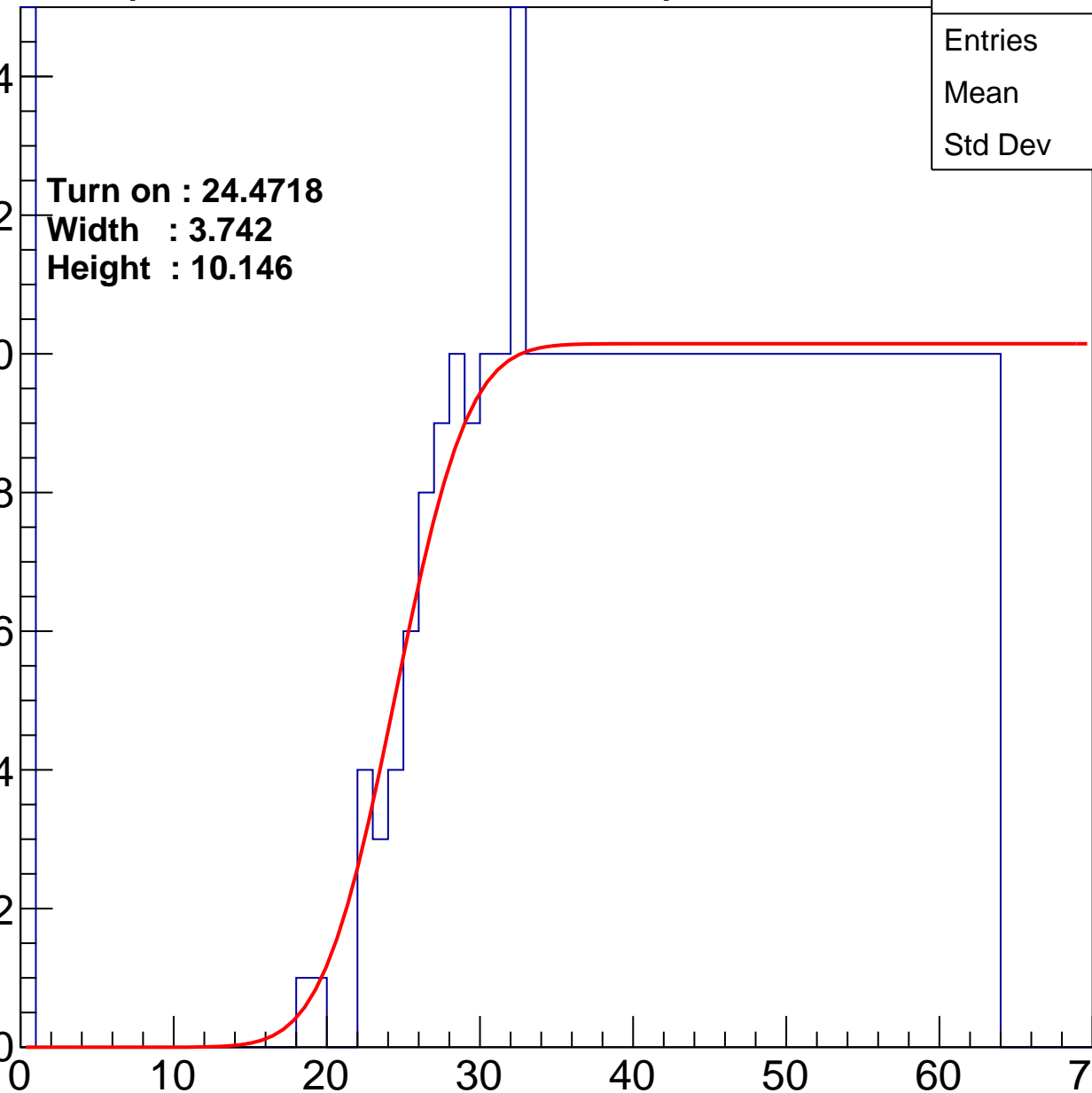
Entries	434
Mean	40.1
Std Dev	16.13

Turn on : 24.4718  
Width : 3.742  
Height : 10.146

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch17

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	409
Mean	40.09
Std Dev	17.57

Turn on : 27.3996

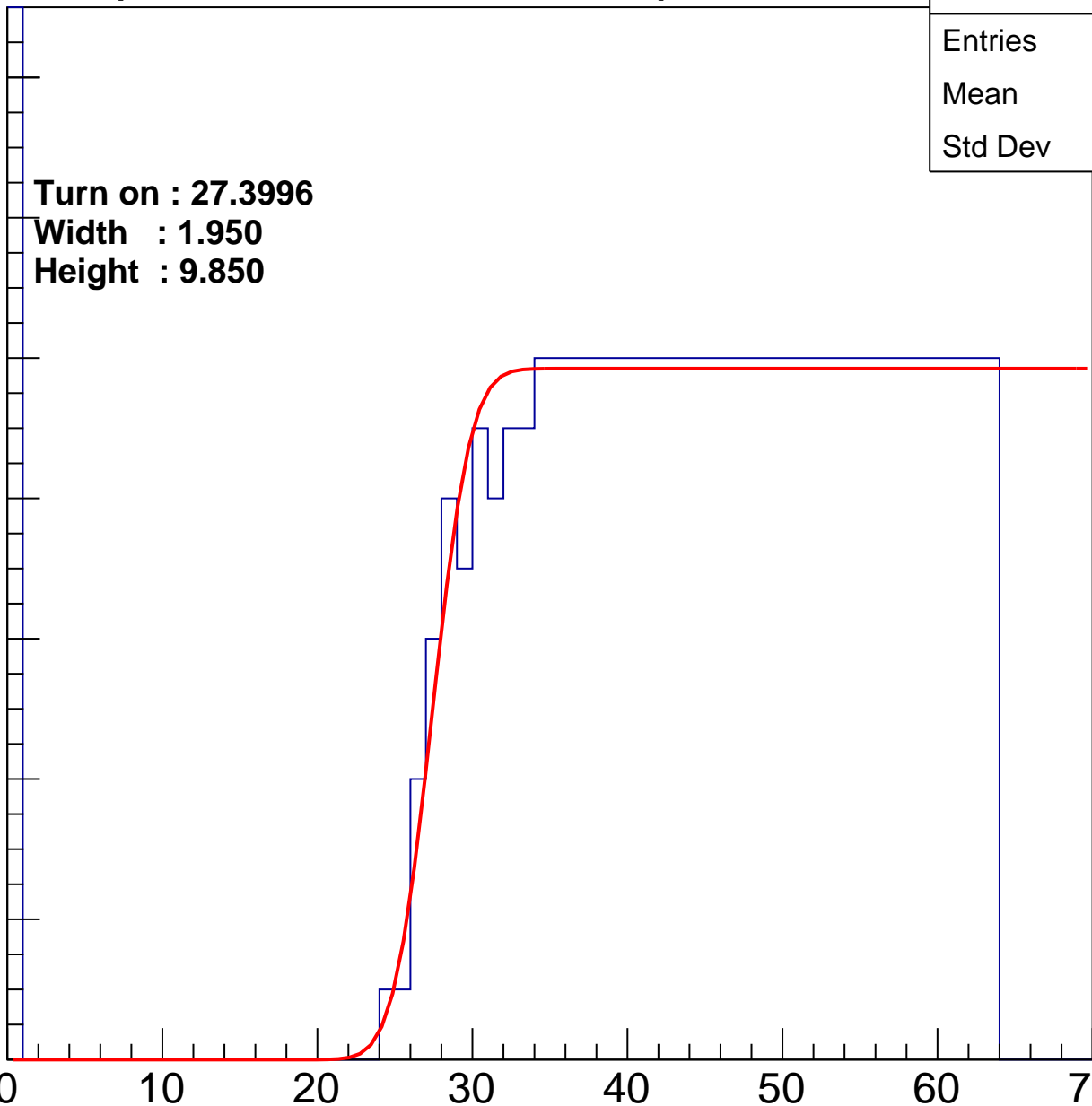
Width : 1.950

Height : 9.850

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch18

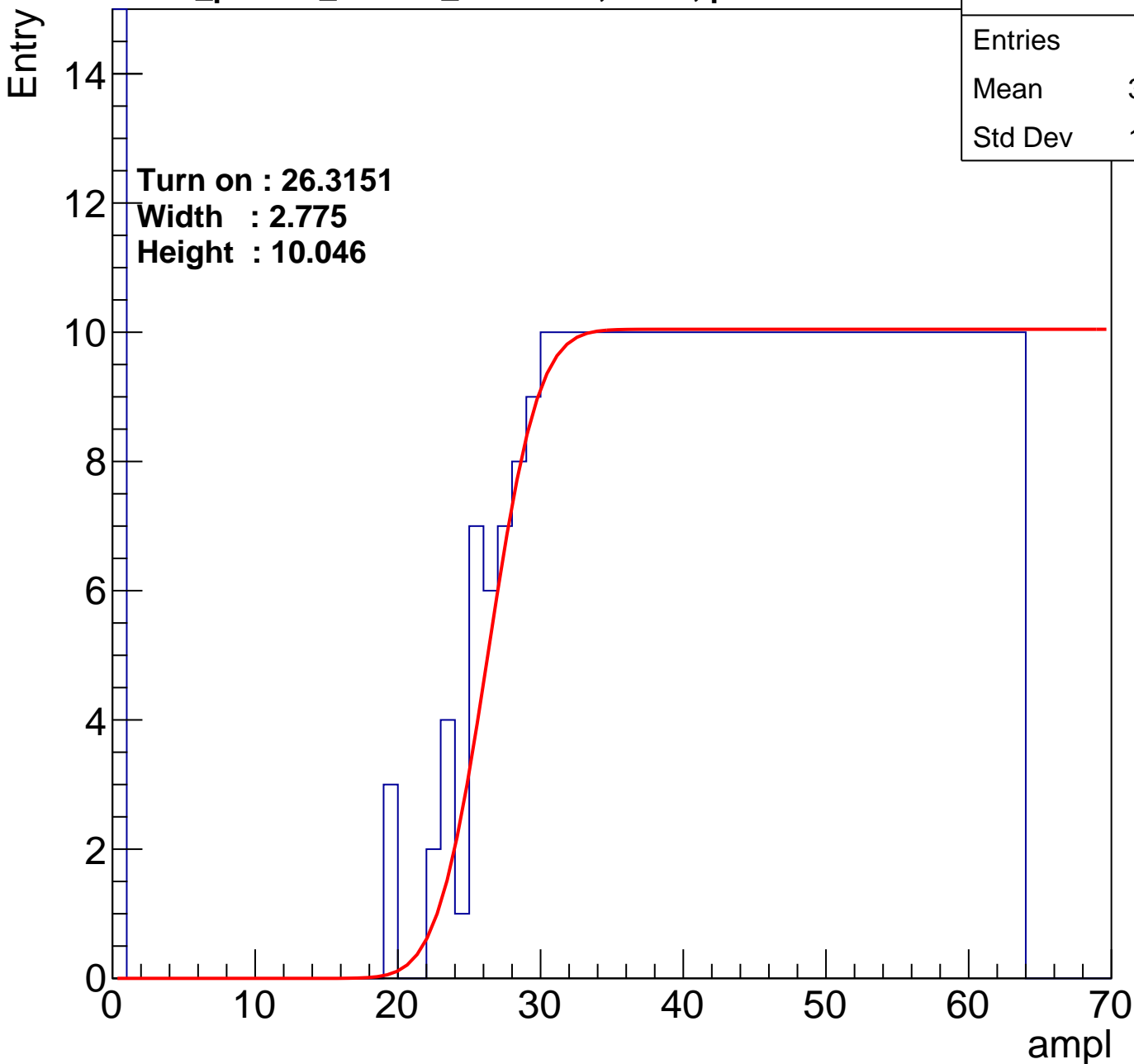
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	433
Mean	39.33
Std Dev	17.33

Turn on : 26.3151

Width : 2.775

Height : 10.046



# B1L103S, U4-ch19

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	405
Mean	40.44
Std Dev	17.28

Turn on : 28.2213

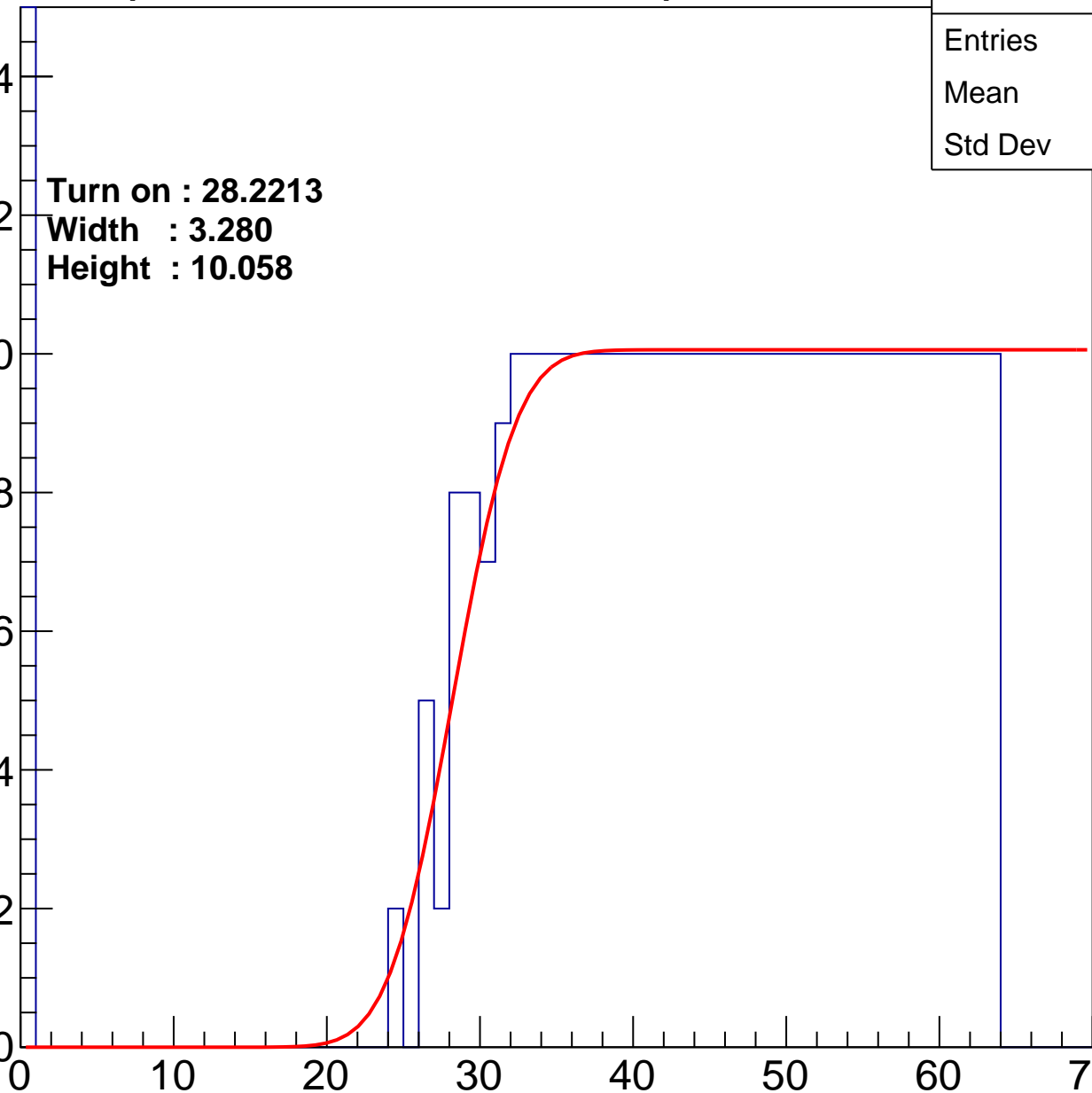
Width : 3.280

Height : 10.058

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch20

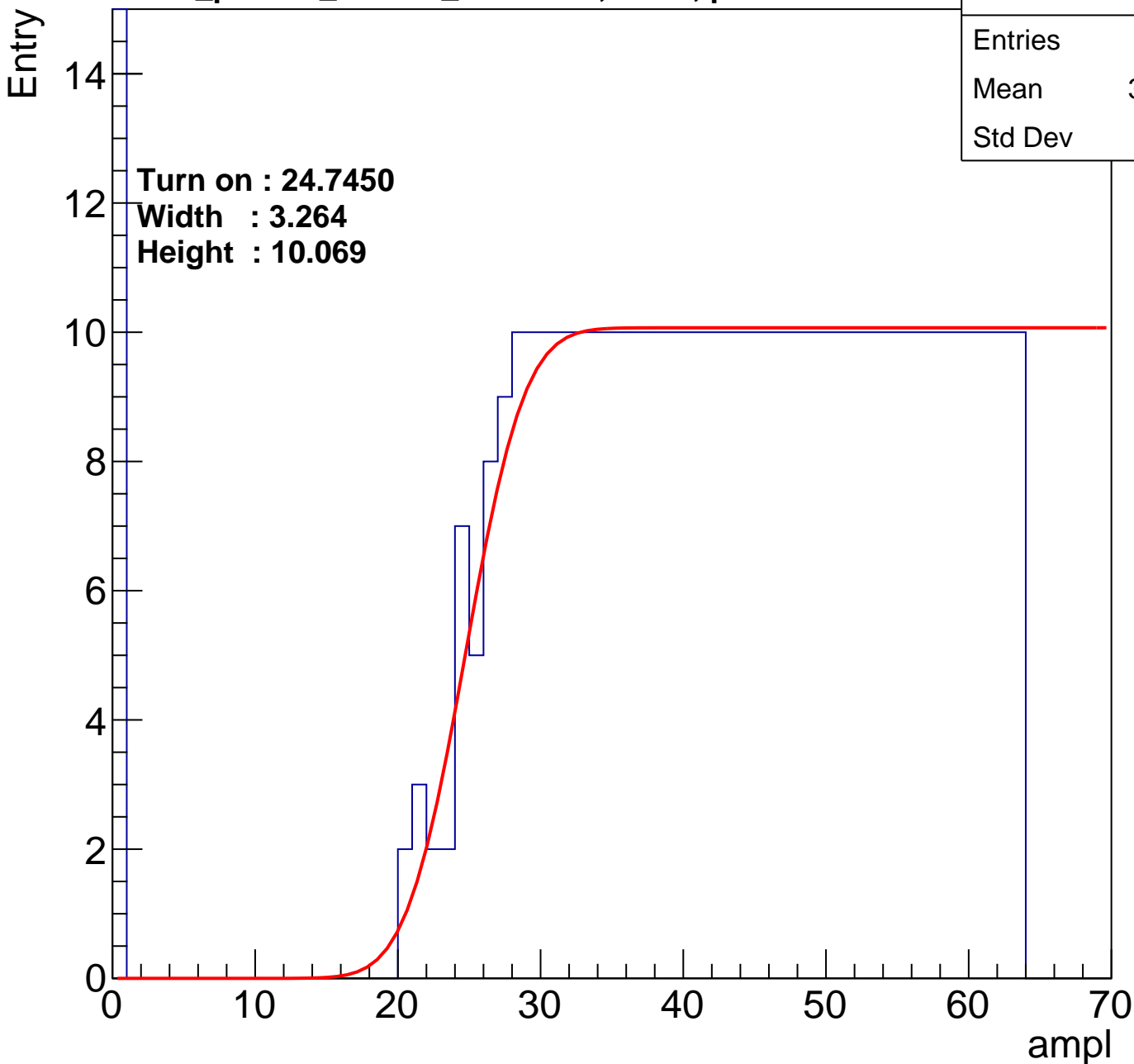
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	446
Mean	38.83
Std Dev	17.4

Turn on : 24.7450

Width : 3.264

Height : 10.069



# B1L103S, U4-ch21

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	439
Mean	38.74
Std Dev	17.93

Turn on : 25.6977

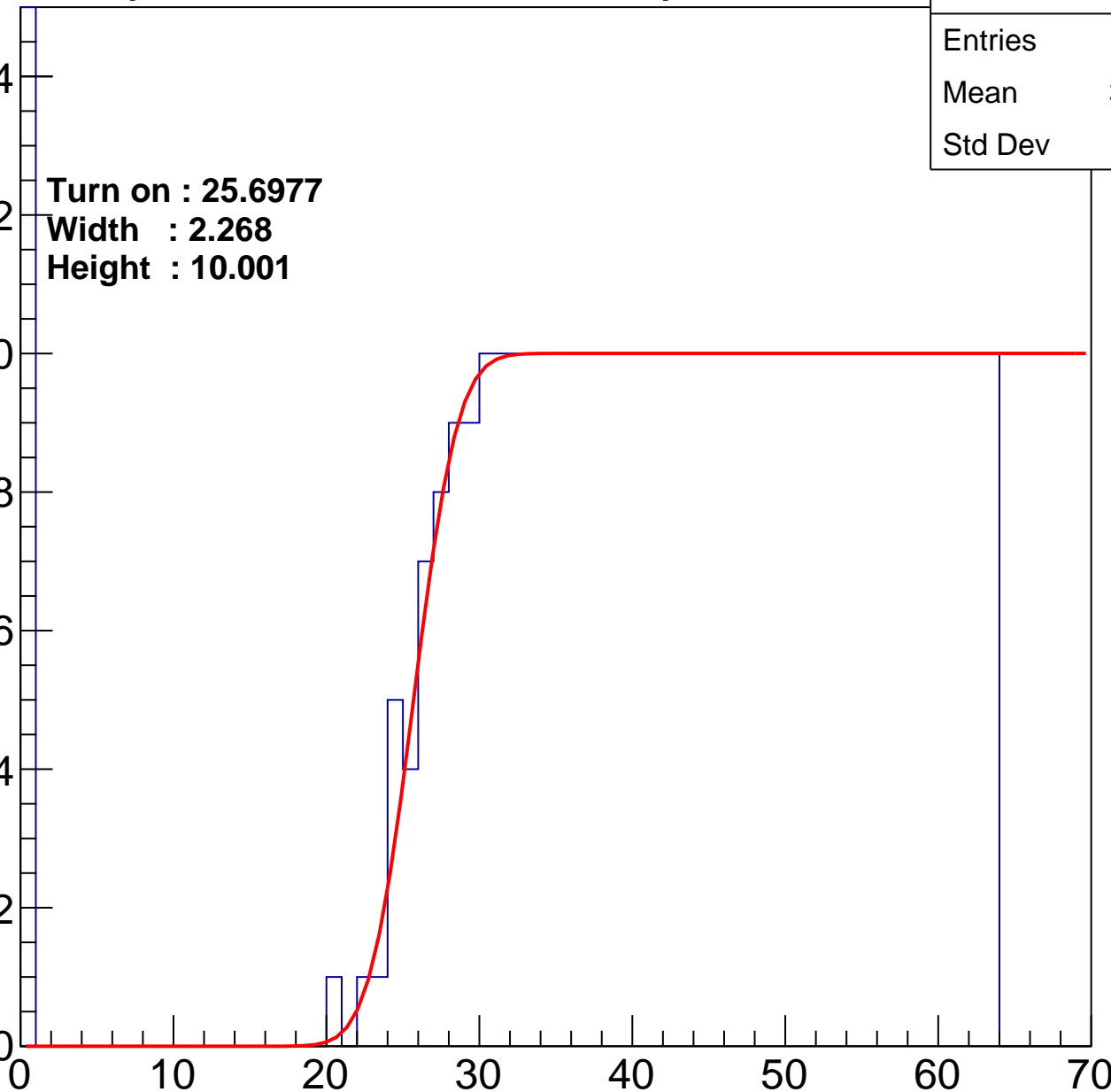
Width : 2.268

Height : 10.001

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch22

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	429
Mean	39.52
Std Dev	17.3

Turn on : 25.4492

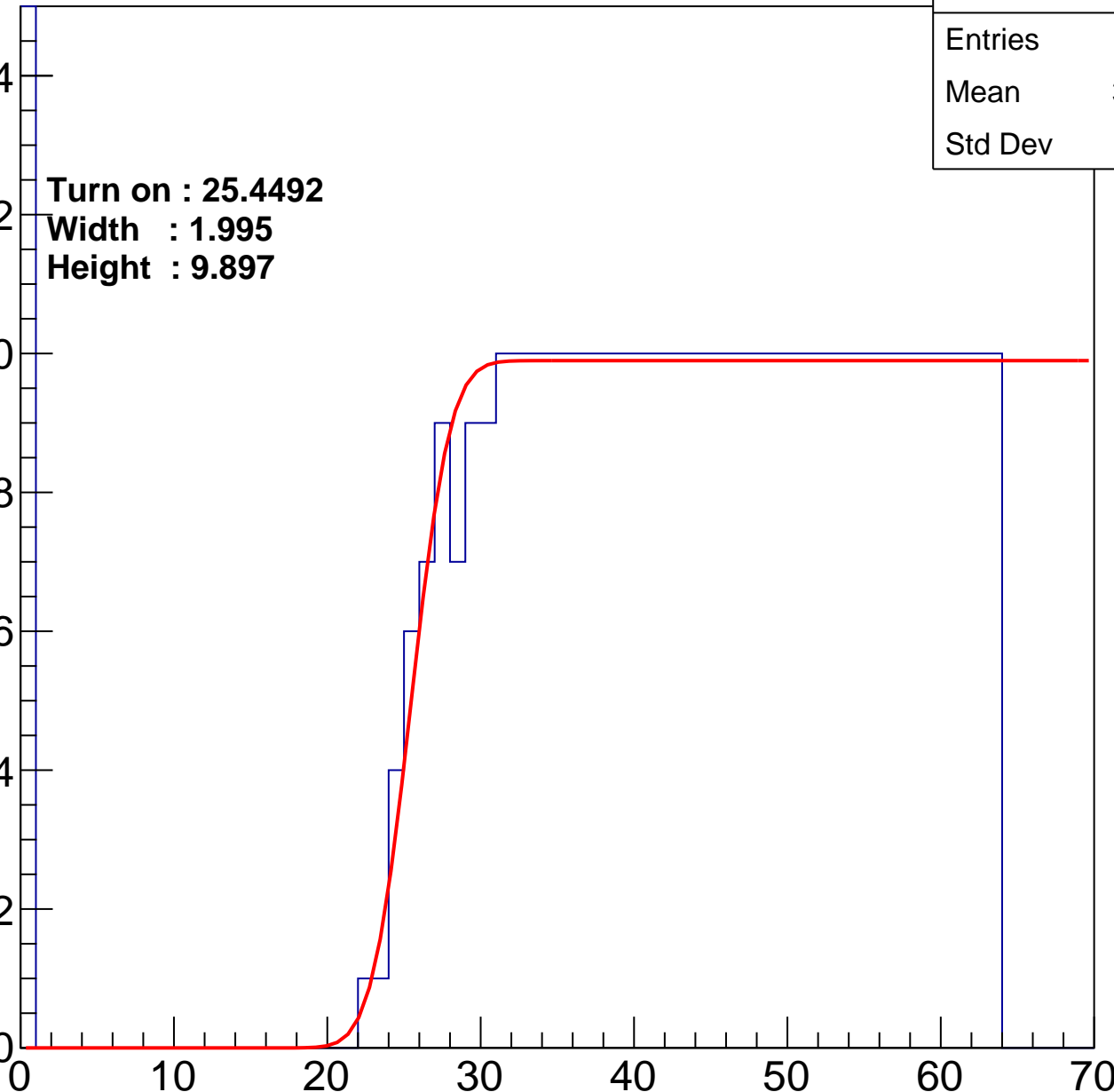
Width : 1.995

Height : 9.897

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L103S, U4-ch23

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	413
Mean	39.89
Std Dev	17.63

Turn on : 27.6720

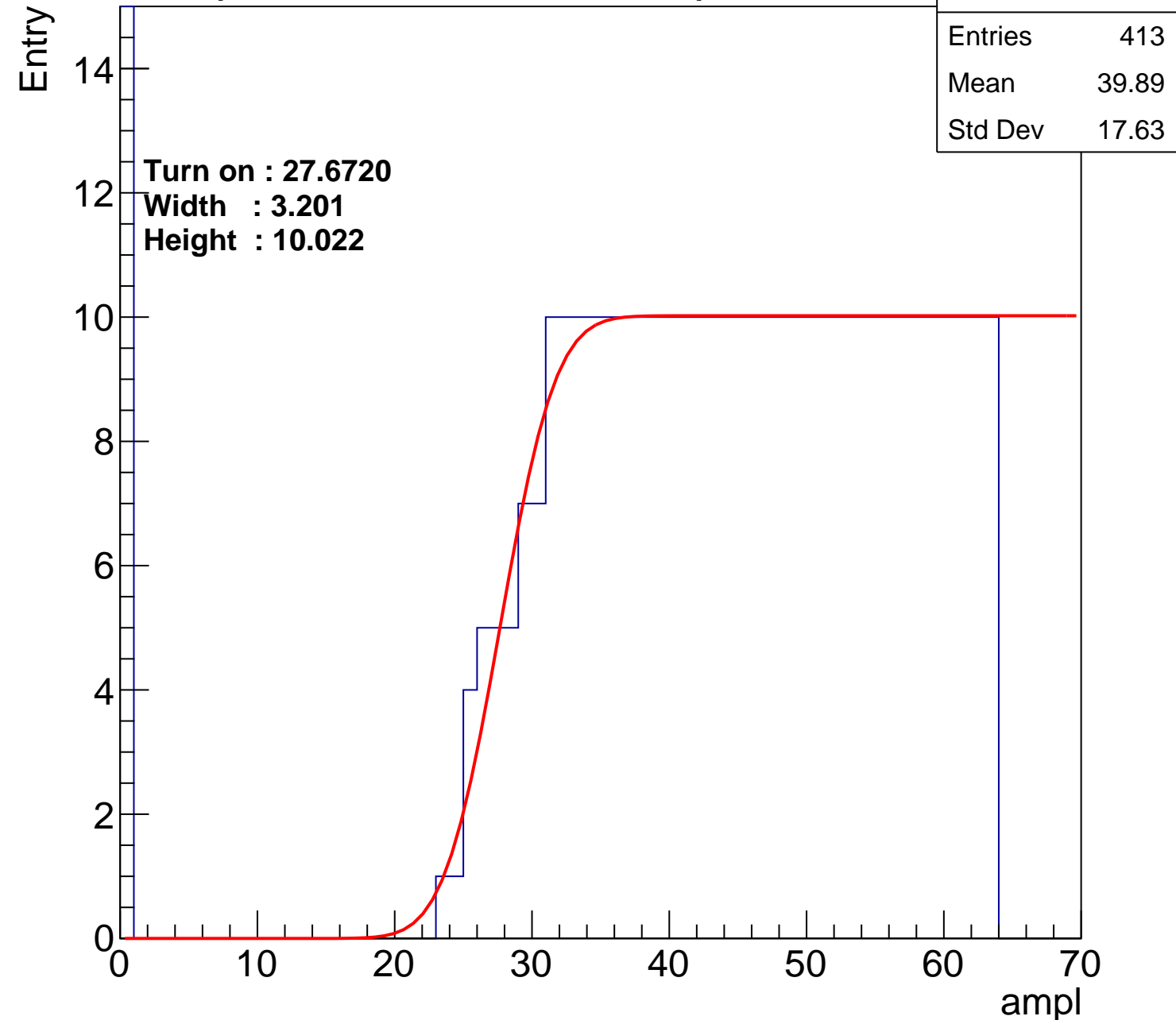
Width : 3.201

Height : 10.022

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch24

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	445
Mean	38.92
Std Dev	17.32

Turn on : 24.5986

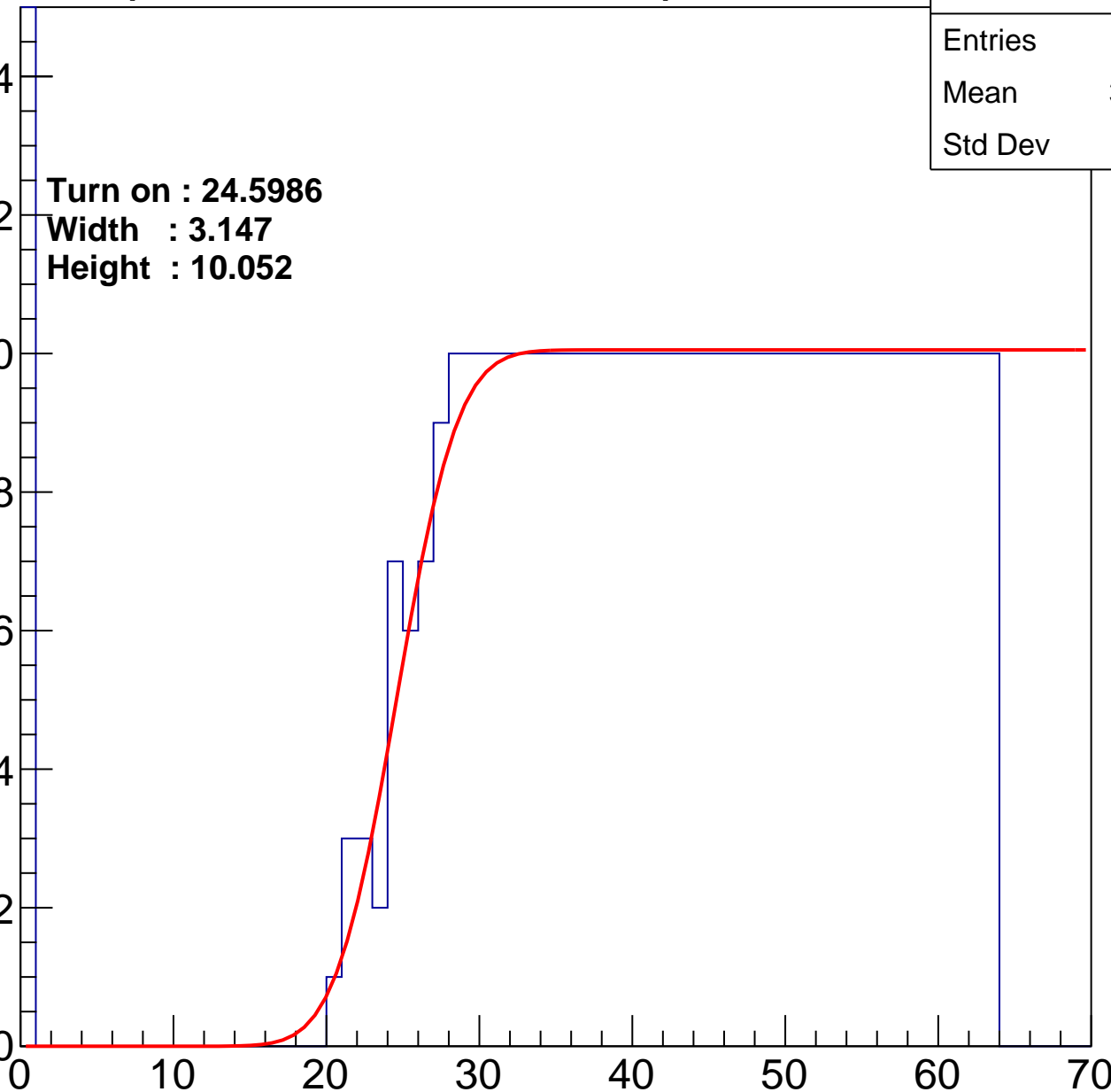
Width : 3.147

Height : 10.052

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch25

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	412
Mean	40.69
Std Dev	16.43

Turn on : 27.0932

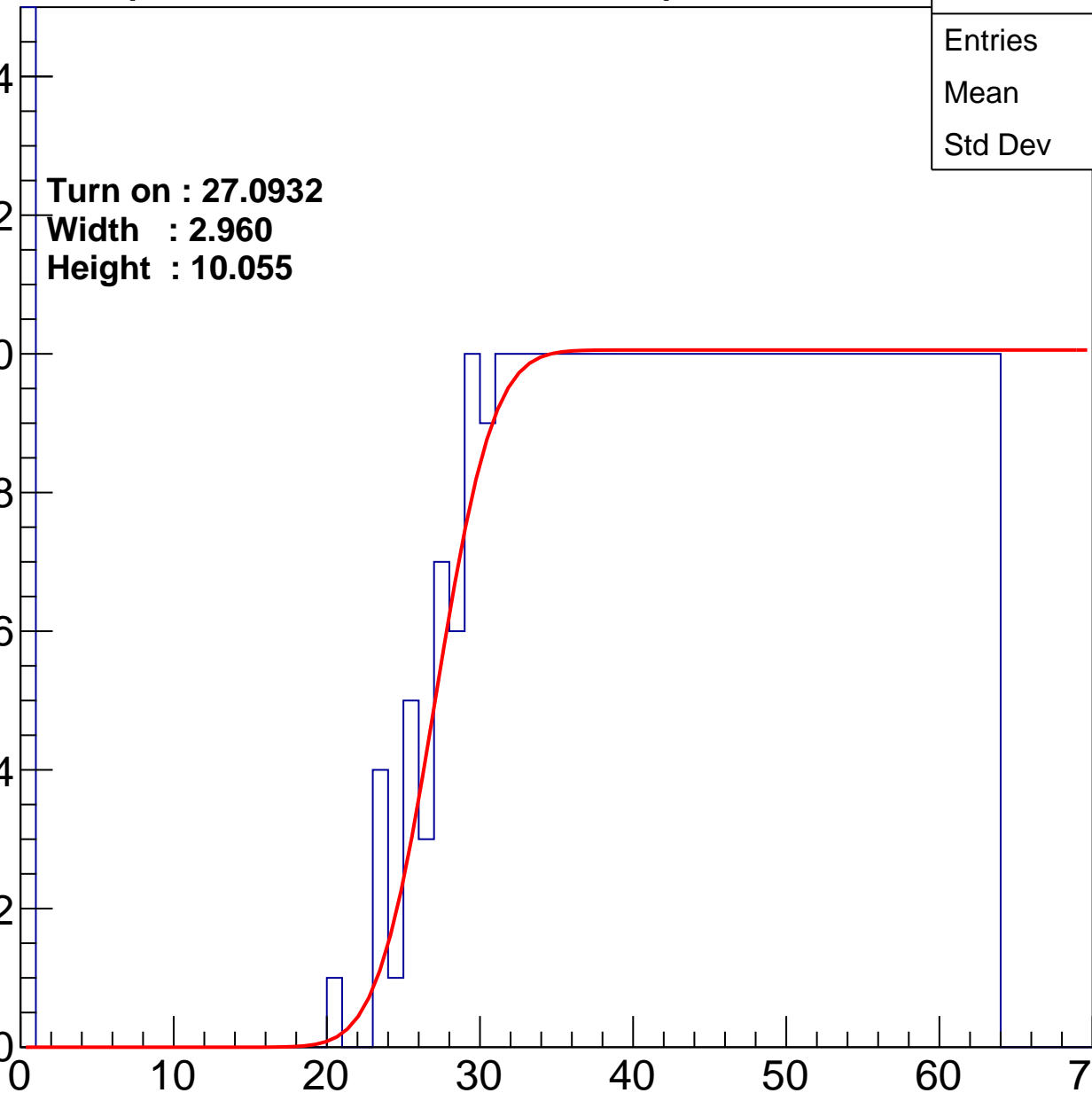
Width : 2.960

Height : 10.055

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch26

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	425
Mean	39.86
Std Dev	16.99

Turn on : 25.8446

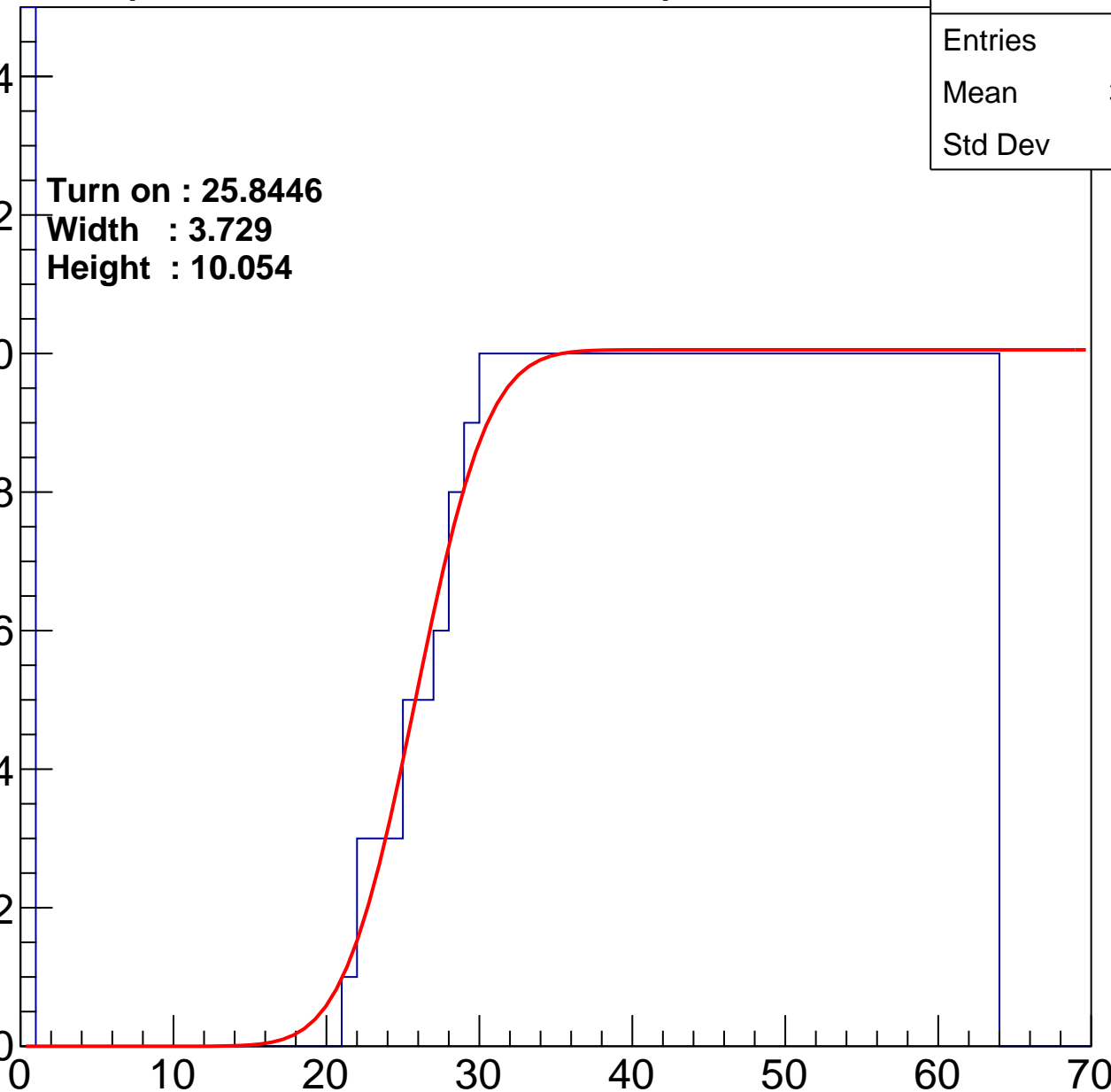
Width : 3.729

Height : 10.054

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch27

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	417
Mean	39.58
Std Dev	17.88

Turn on : 27.7462

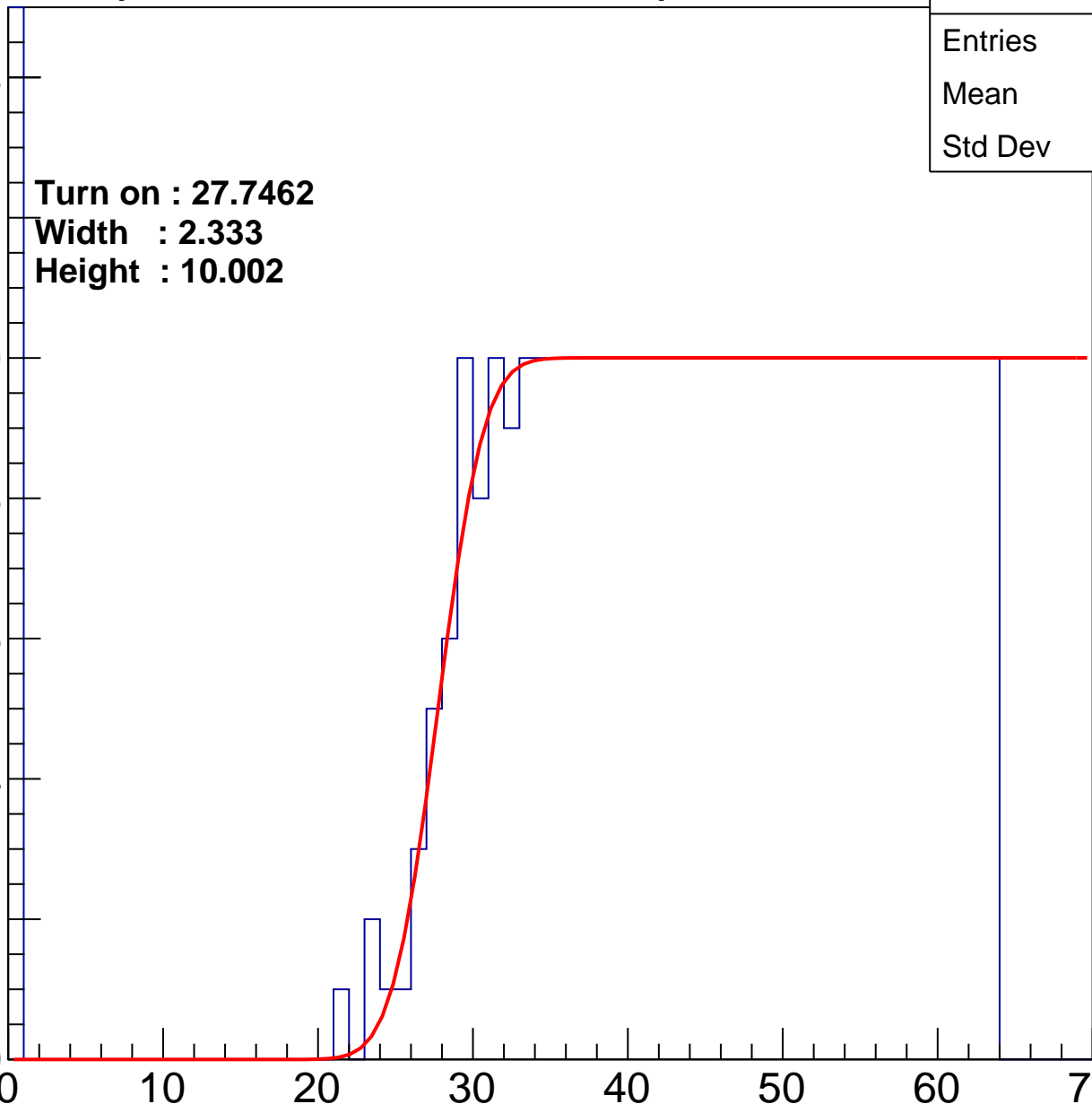
Width : 2.333

Height : 10.002

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch28

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	436
Mean	39.17
Std Dev	17.4

Turn on : 25.2425

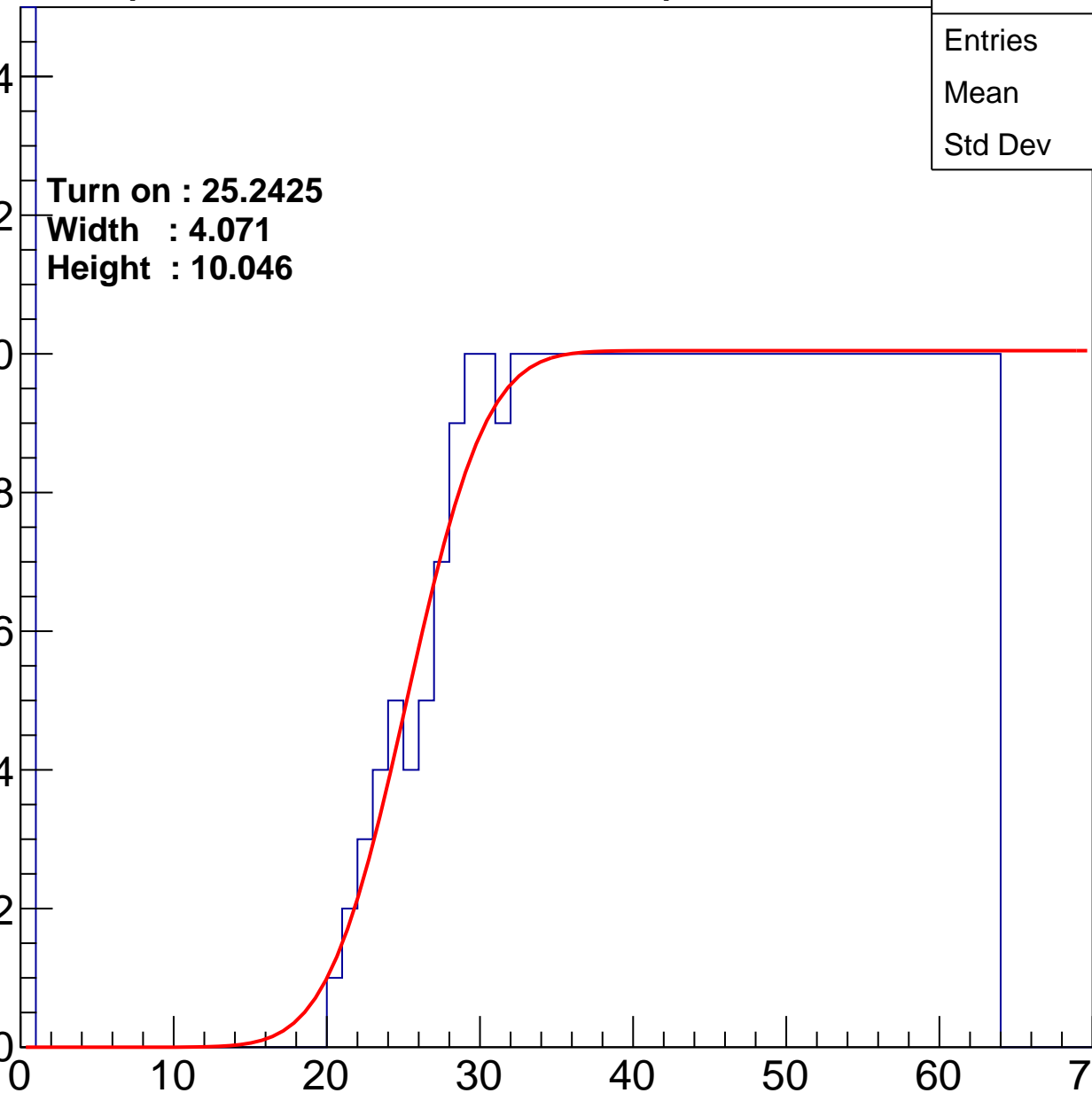
Width : 4.071

Height : 10.046

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch29

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	417
Mean	39.87
Std Dev	17.47

Turn on : 27.5450

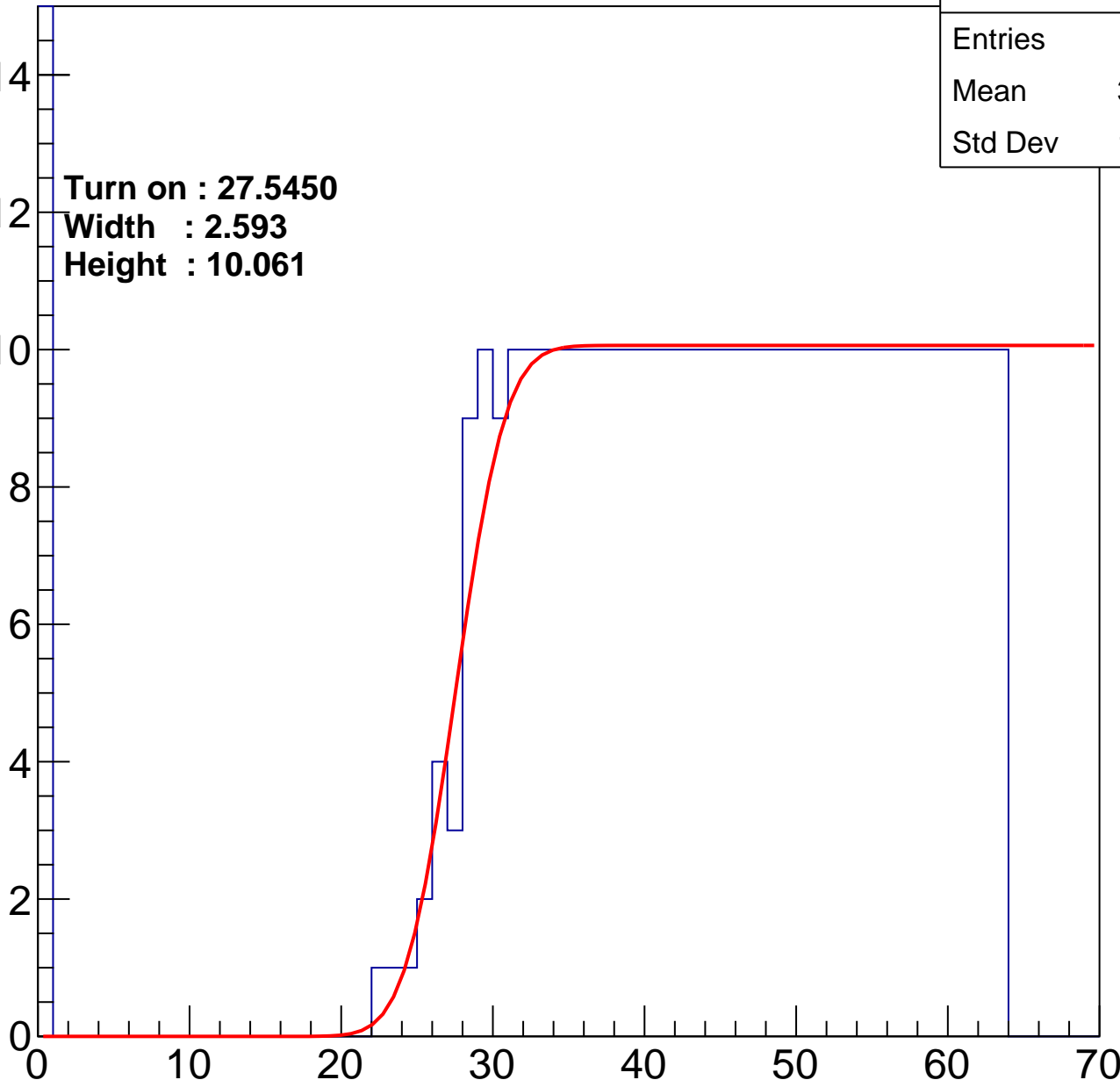
Width : 2.593

Height : 10.061

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch30

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	447
Mean	38.85
Std Dev	17.27

Turn on : 24.2227

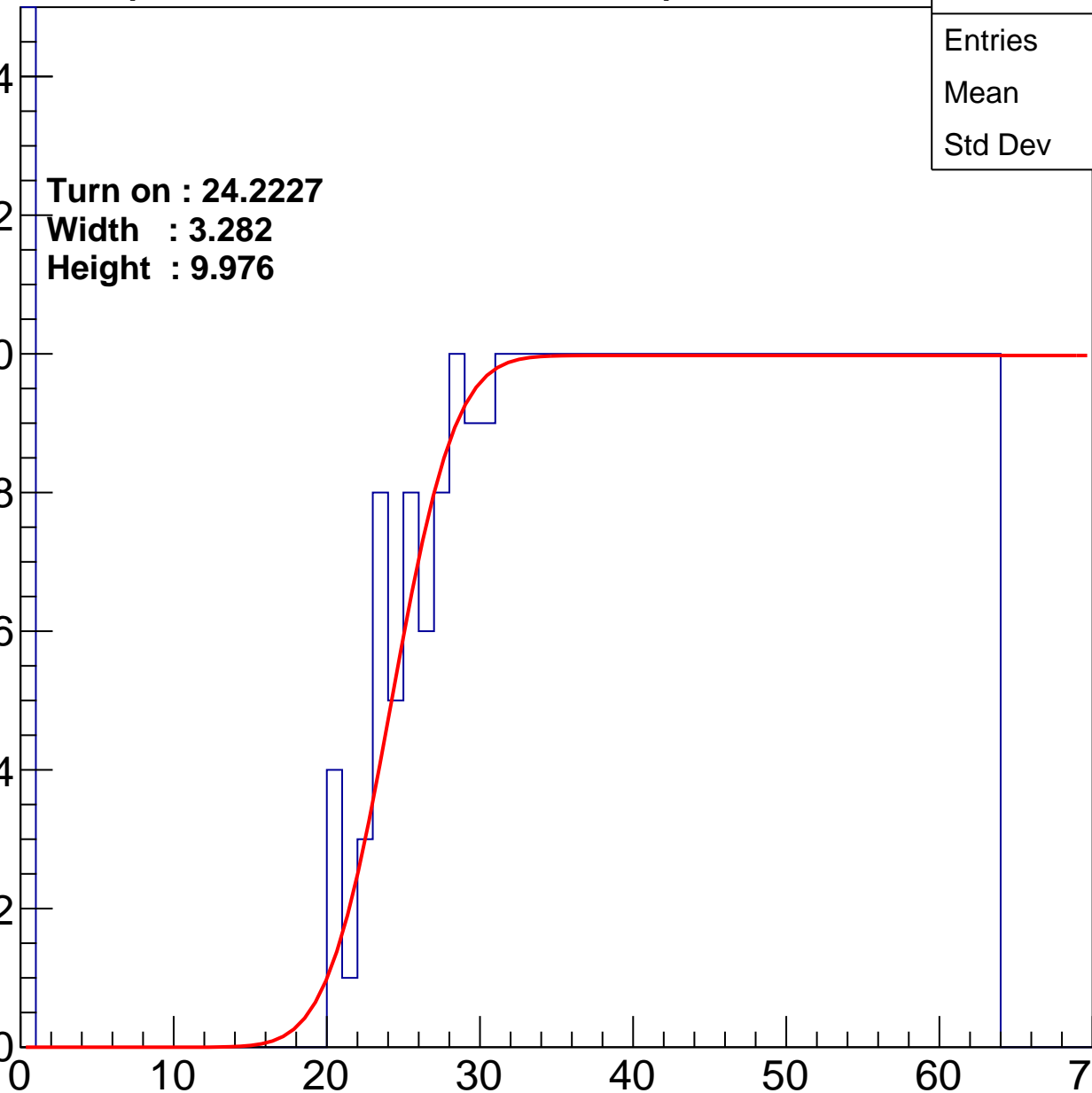
Width : 3.282

Height : 9.976

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L103S, U4-ch31

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	415
Mean	40.38
Std Dev	16.74

Turn on : 27.2554

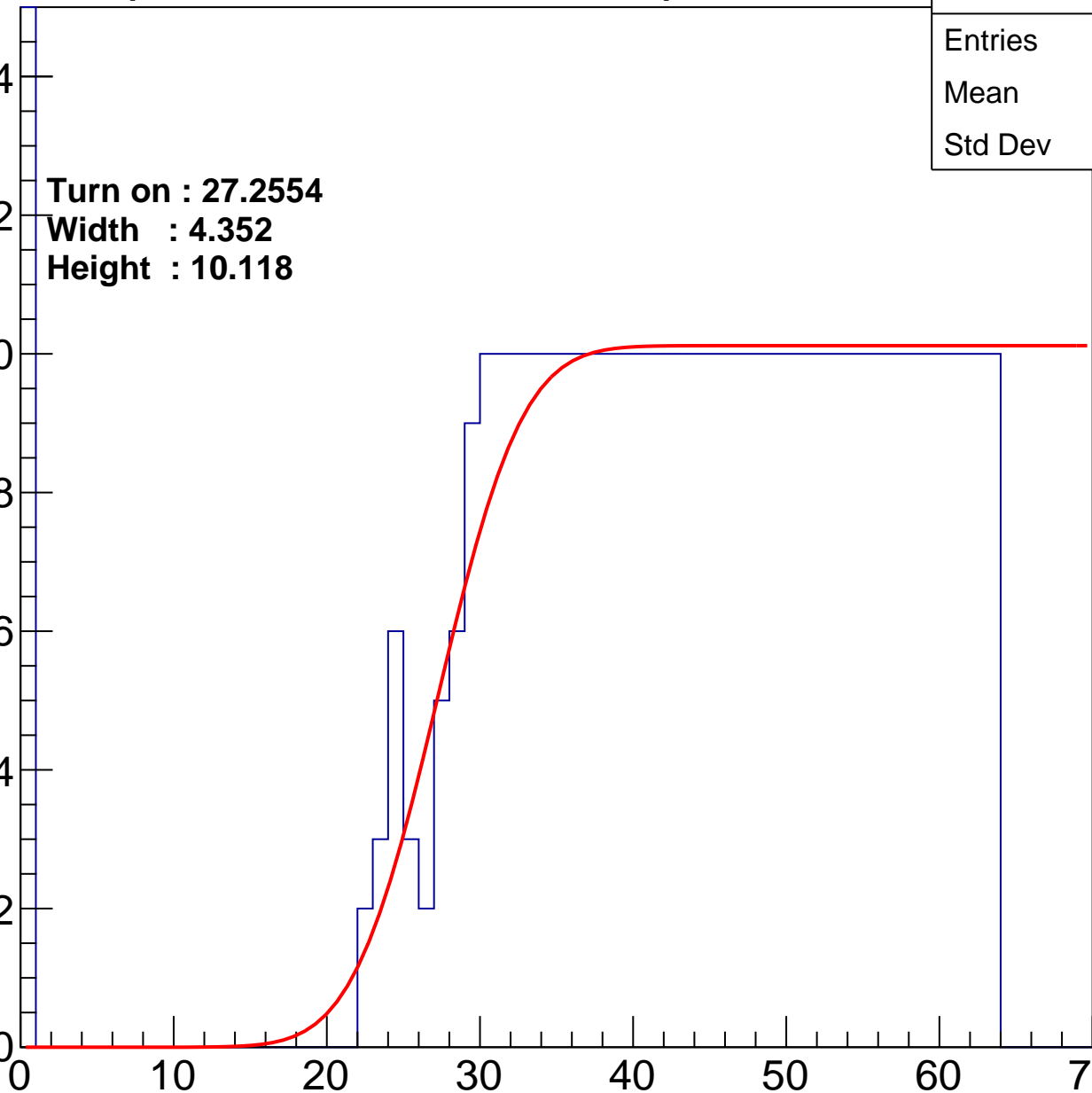
Width : 4.352

Height : 10.118

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch32

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	451
Mean	38.98
Std Dev	16.88

Turn on : 23.1595

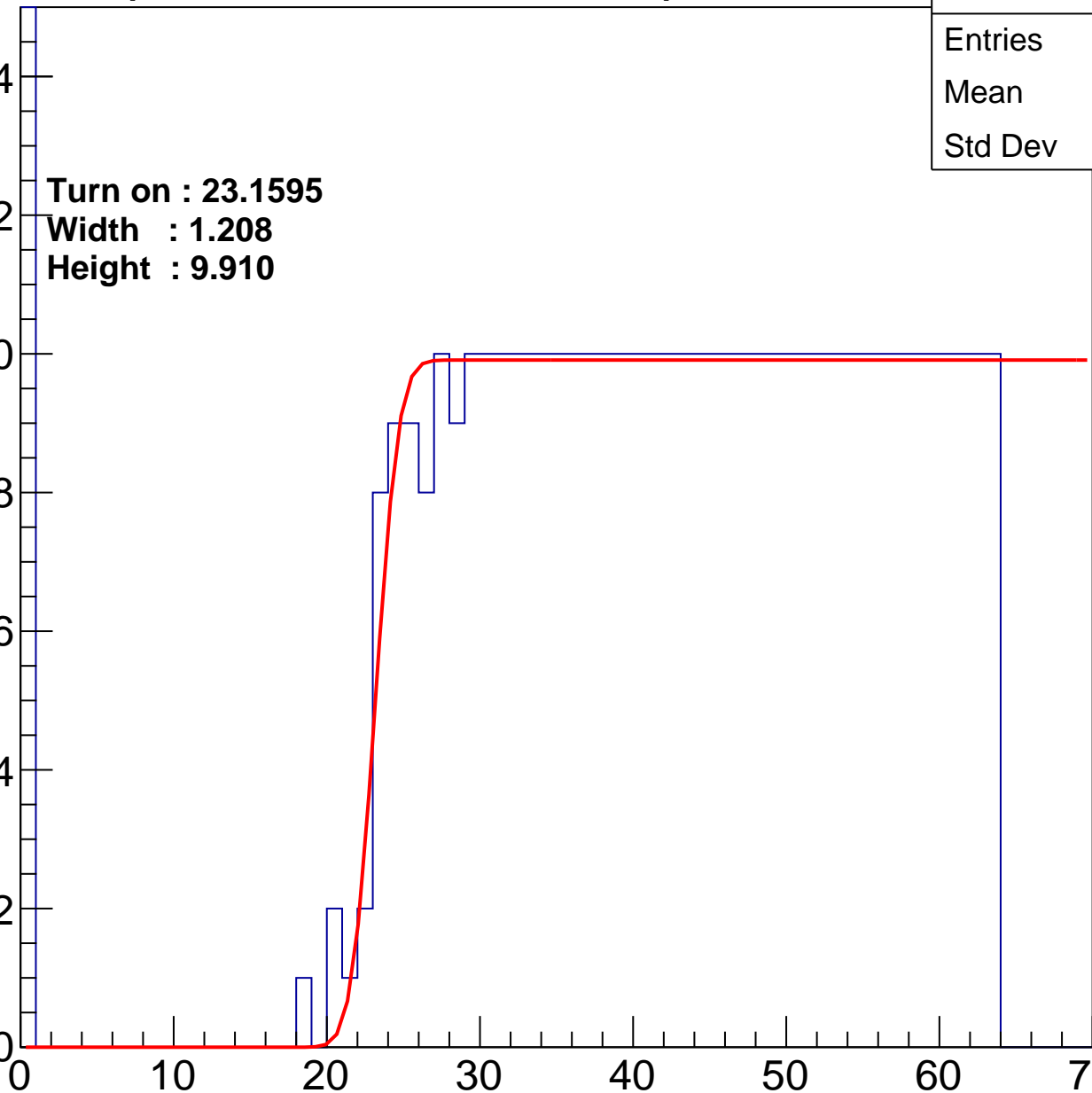
Width : 1.208

Height : 9.910

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch33

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	427
Mean	39.2
Std Dev	17.84

Turn on : 26.4105

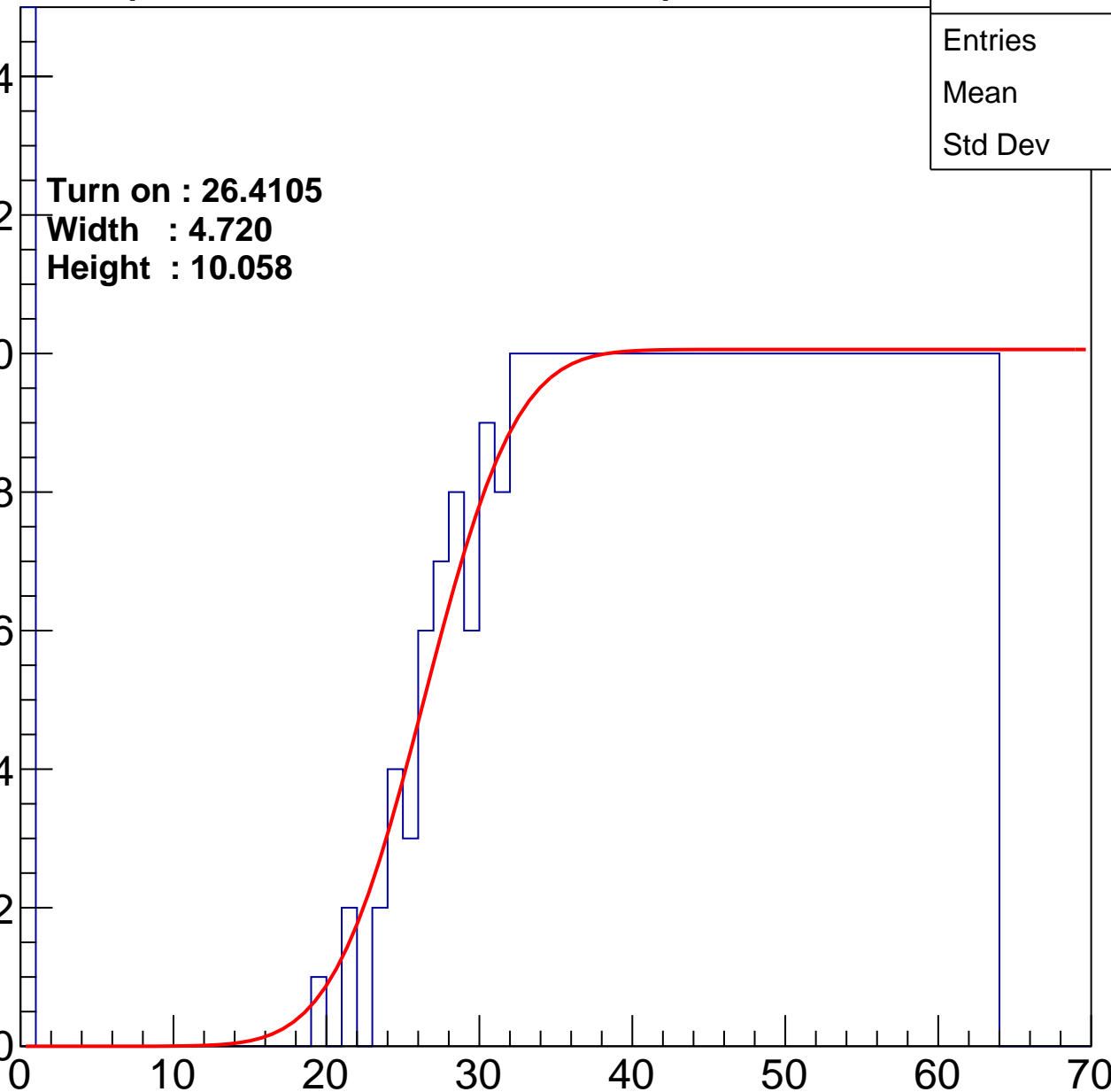
Width : 4.720

Height : 10.058

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch34

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	429
Mean	39.86
Std Dev	16.76

**Turn on : 24.8556**

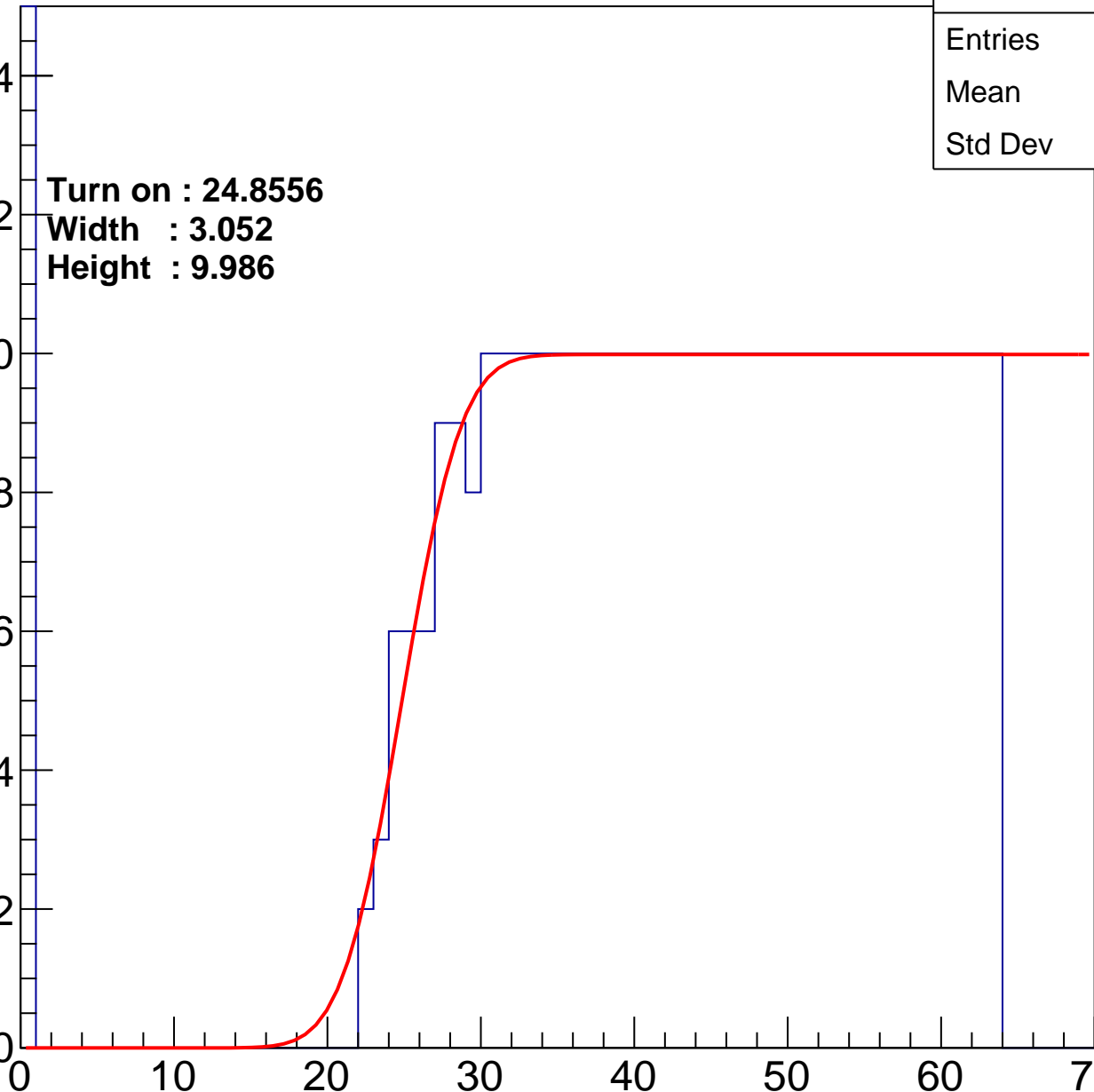
**Width : 3.052**

**Height : 9.986**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch35

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	404
Mean	40.8
Std Dev	16.77

Turn on : 27.6536

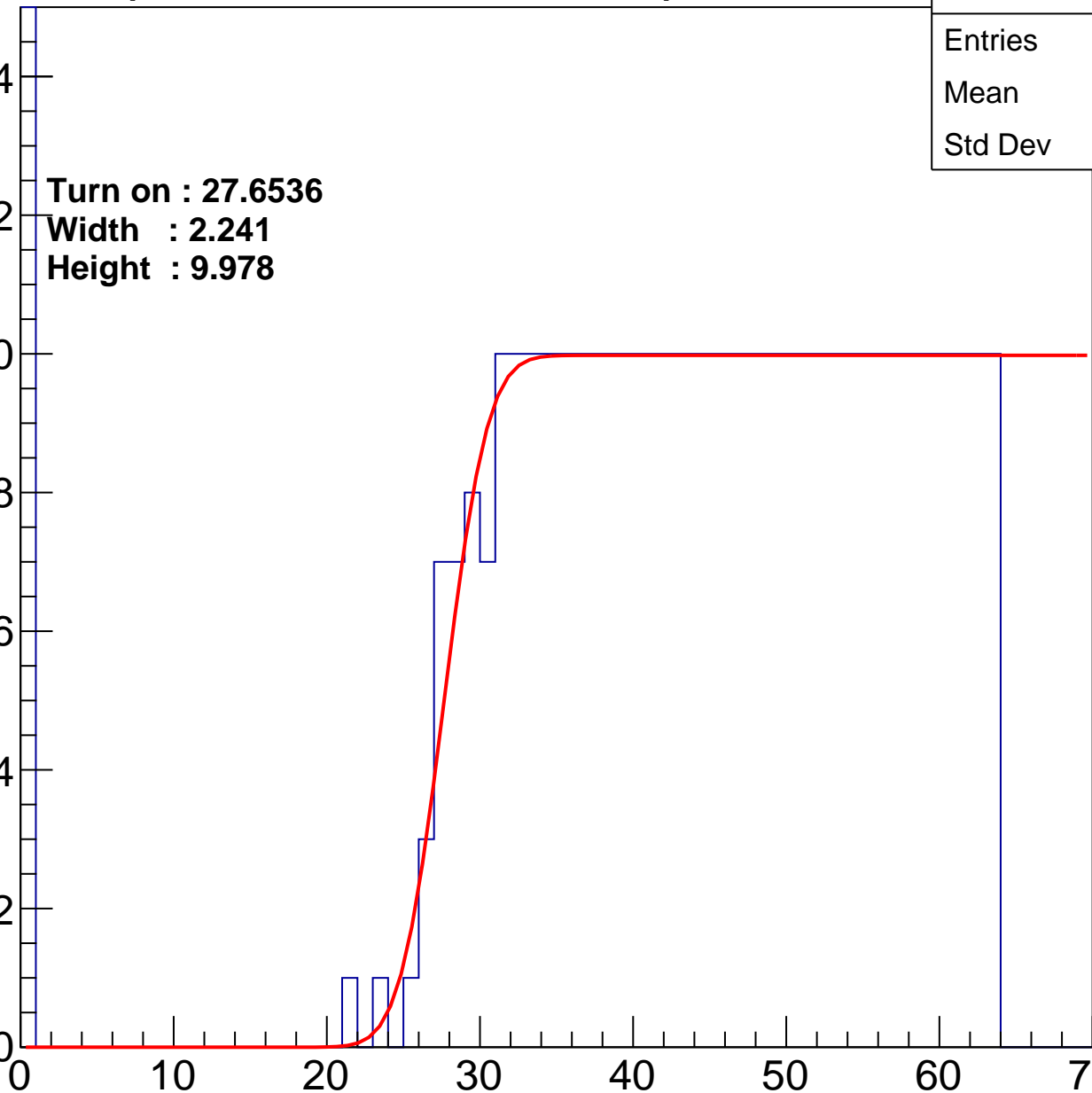
Width : 2.241

Height : 9.978

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch36

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	420
Mean	39.85
Std Dev	17.29

**Turn on : 26.8157**

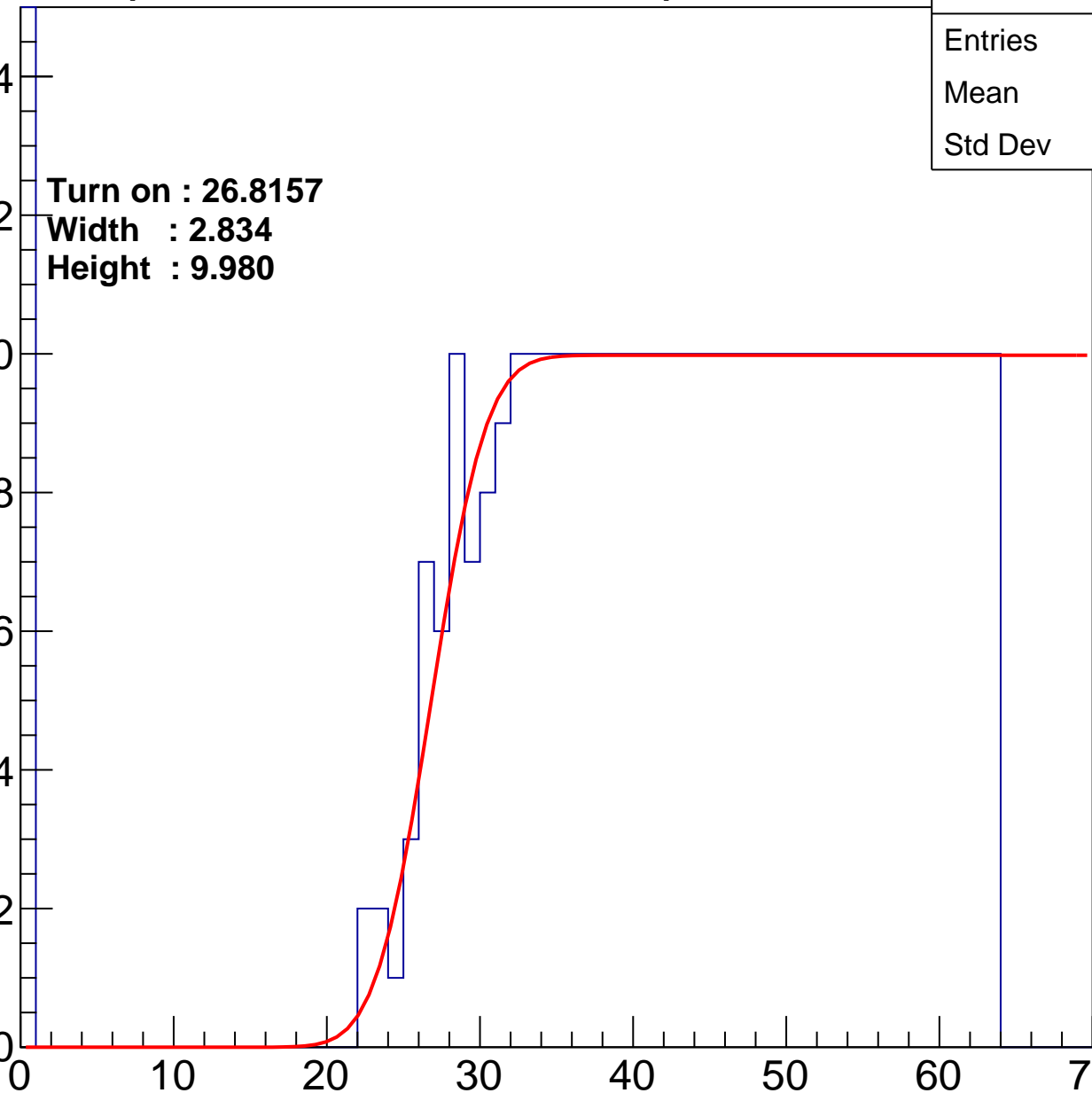
**Width : 2.834**

**Height : 9.980**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch37

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	413
Mean	40.39
Std Dev	16.84

Turn on : 26.4865

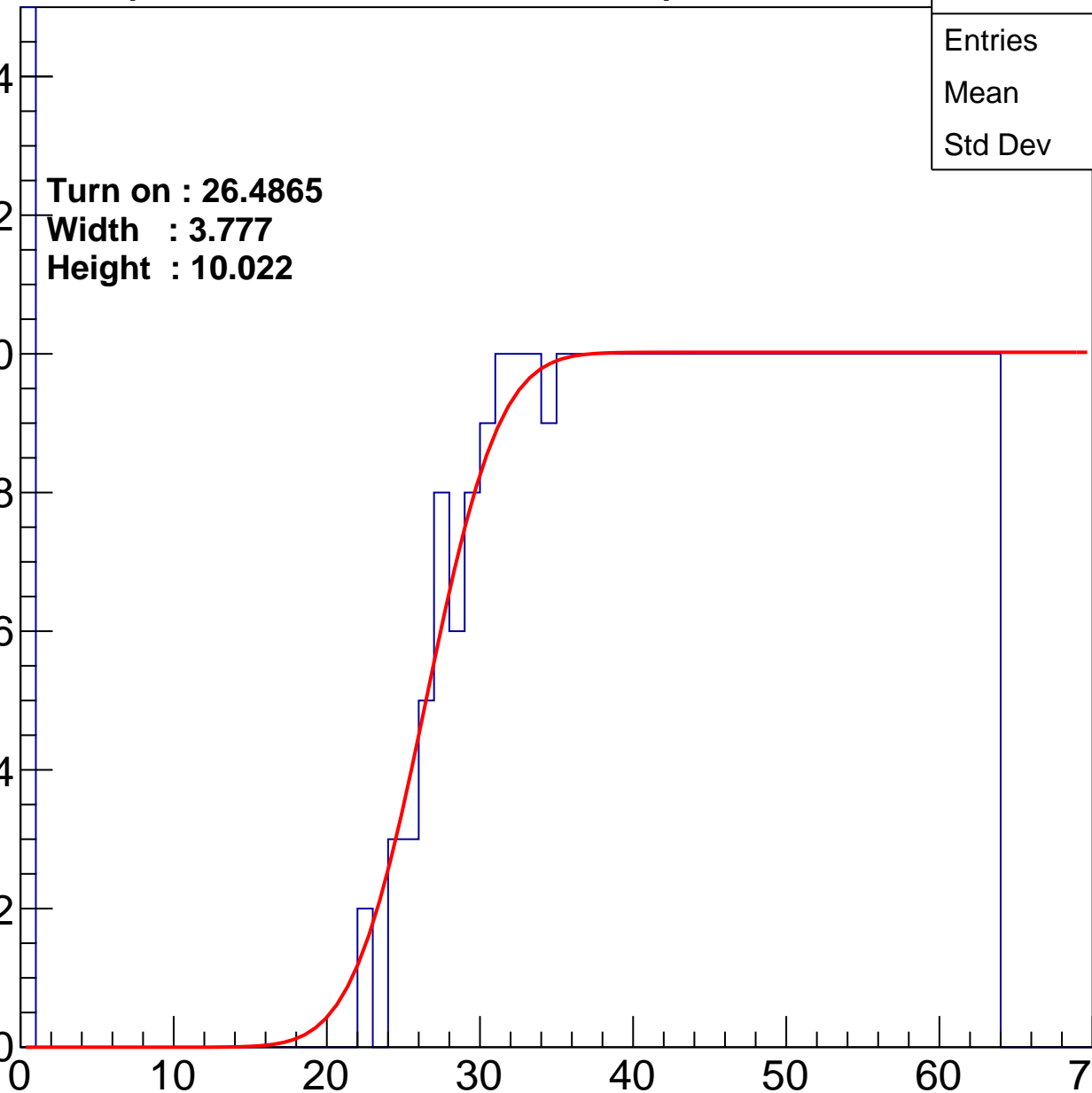
Width : 3.777

Height : 10.022

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch38

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	460
Mean	37.98
Std Dev	17.9

Turn on : 23.9210

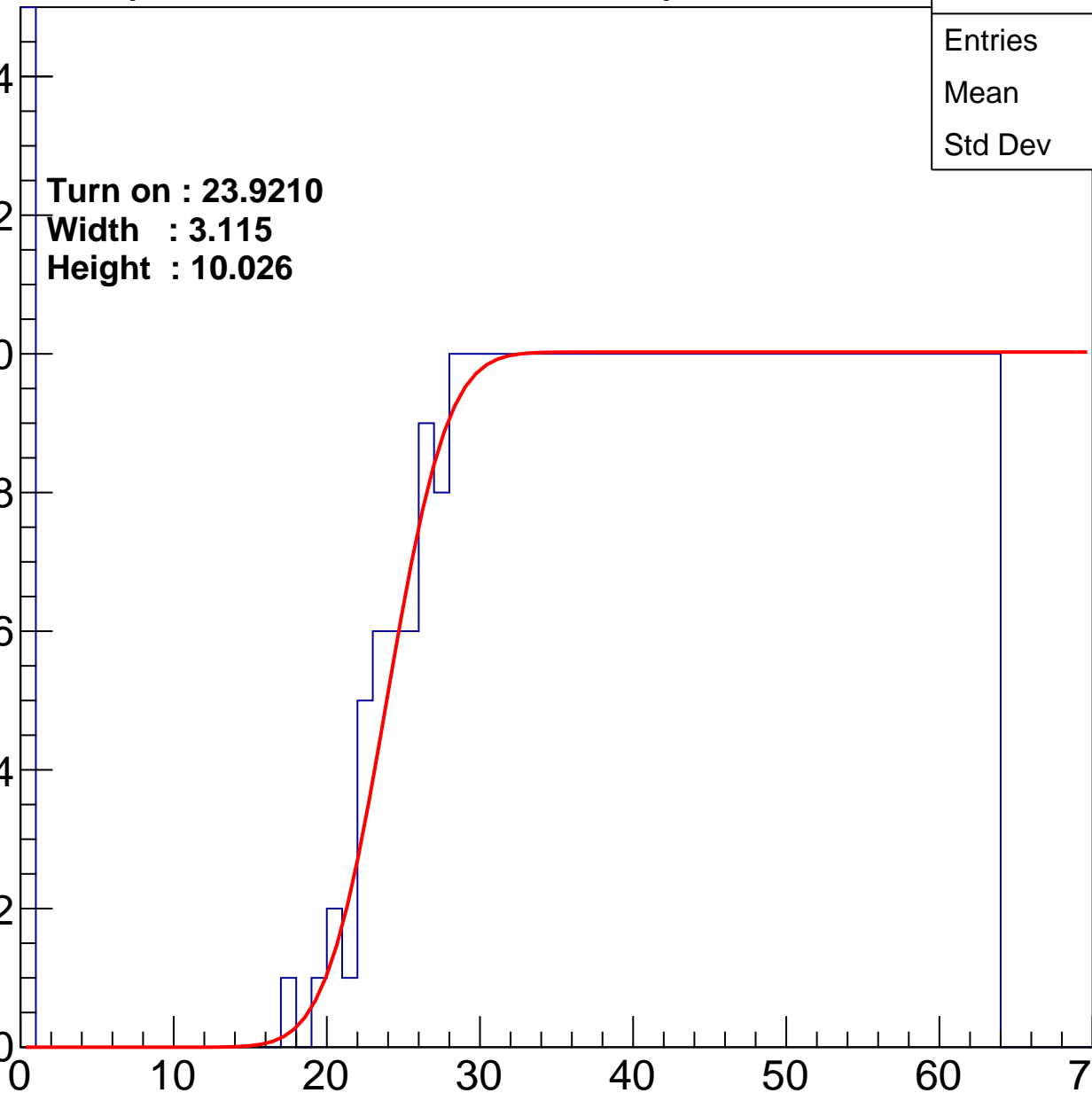
Width : 3.115

Height : 10.026

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L103S, U4-ch39

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	420
Mean	39.41
Std Dev	17.95

Turn on : 27.2480

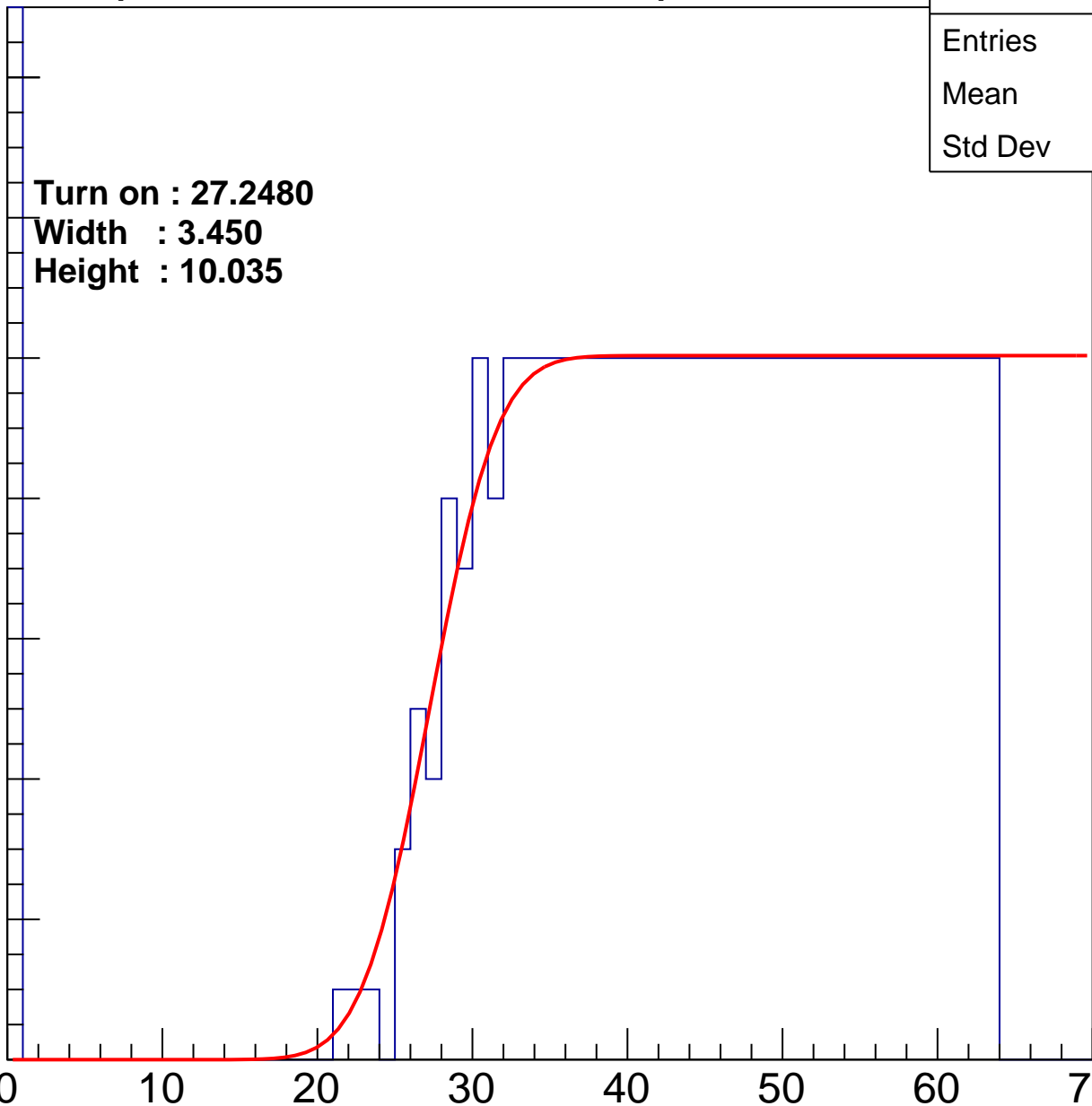
Width : 3.450

Height : 10.035

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch40

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	414
Mean	40.13
Std Dev	17.51

Turn on : 28.3740

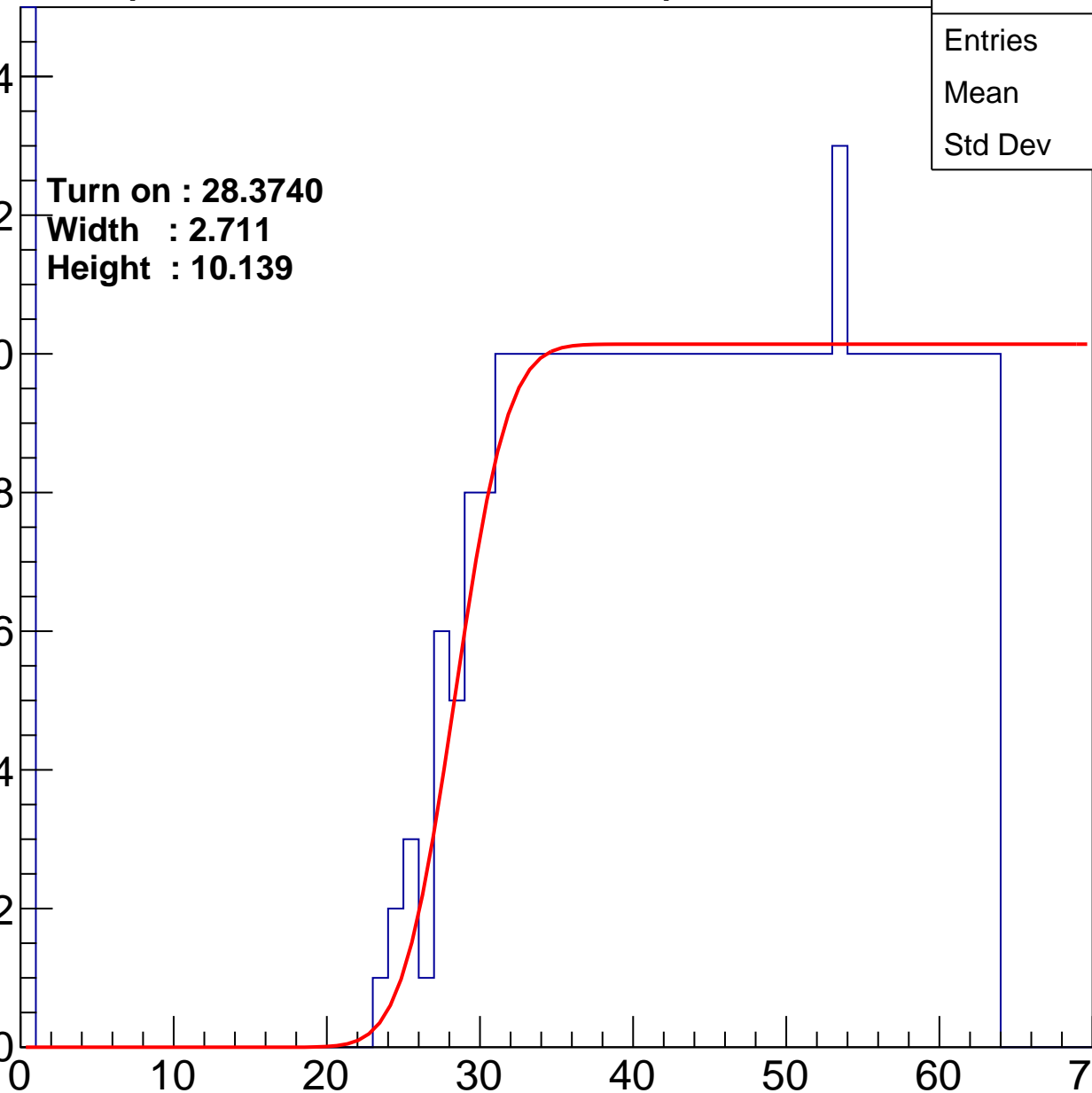
Width : 2.711

Height : 10.139

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch41

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	420
Mean	39.91
Std Dev	17.19

Turn on : 26.5601

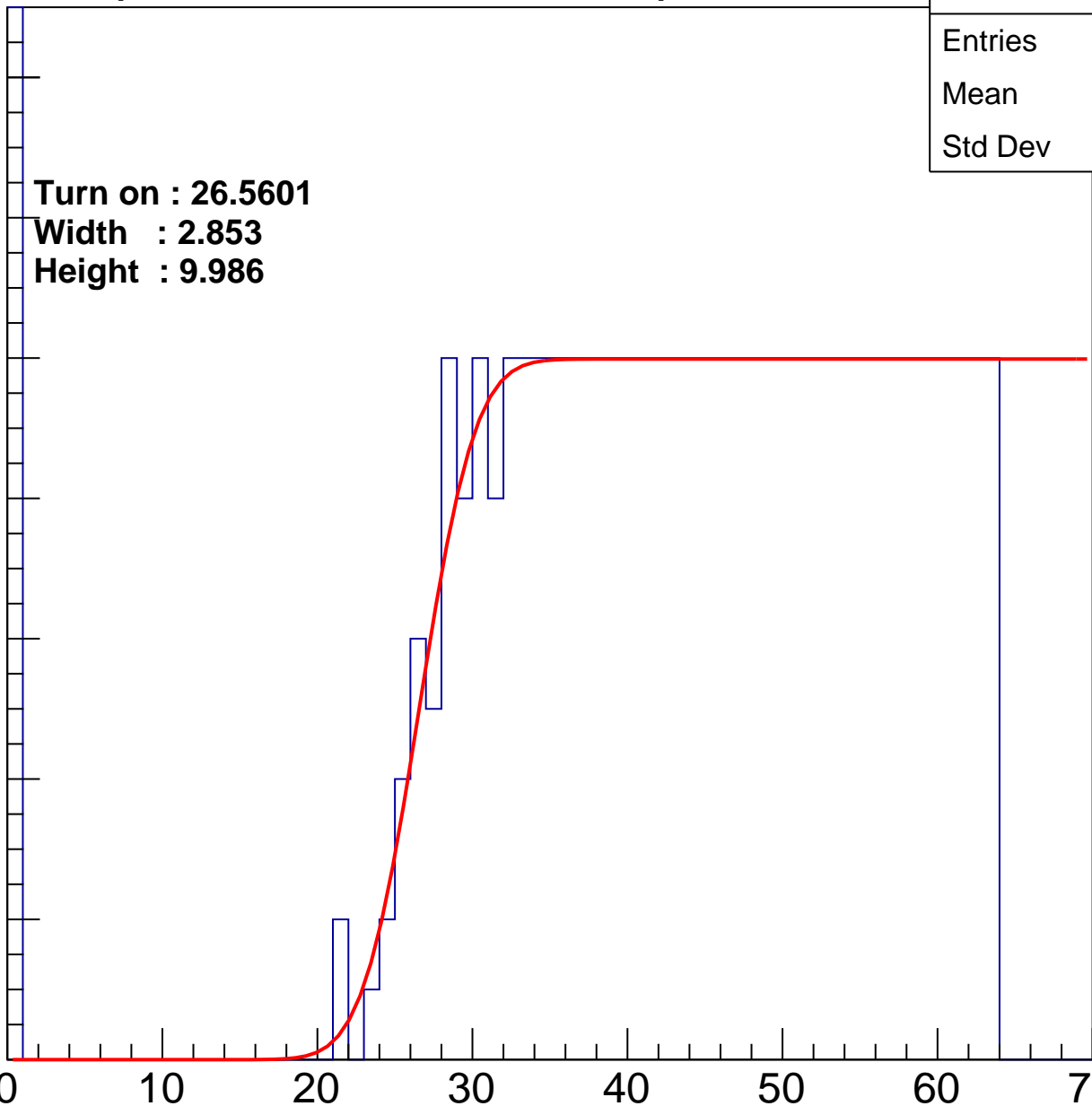
Width : 2.853

Height : 9.986

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch42

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	448
Mean	38.66
Std Dev	17.51

Turn on : 24.2446

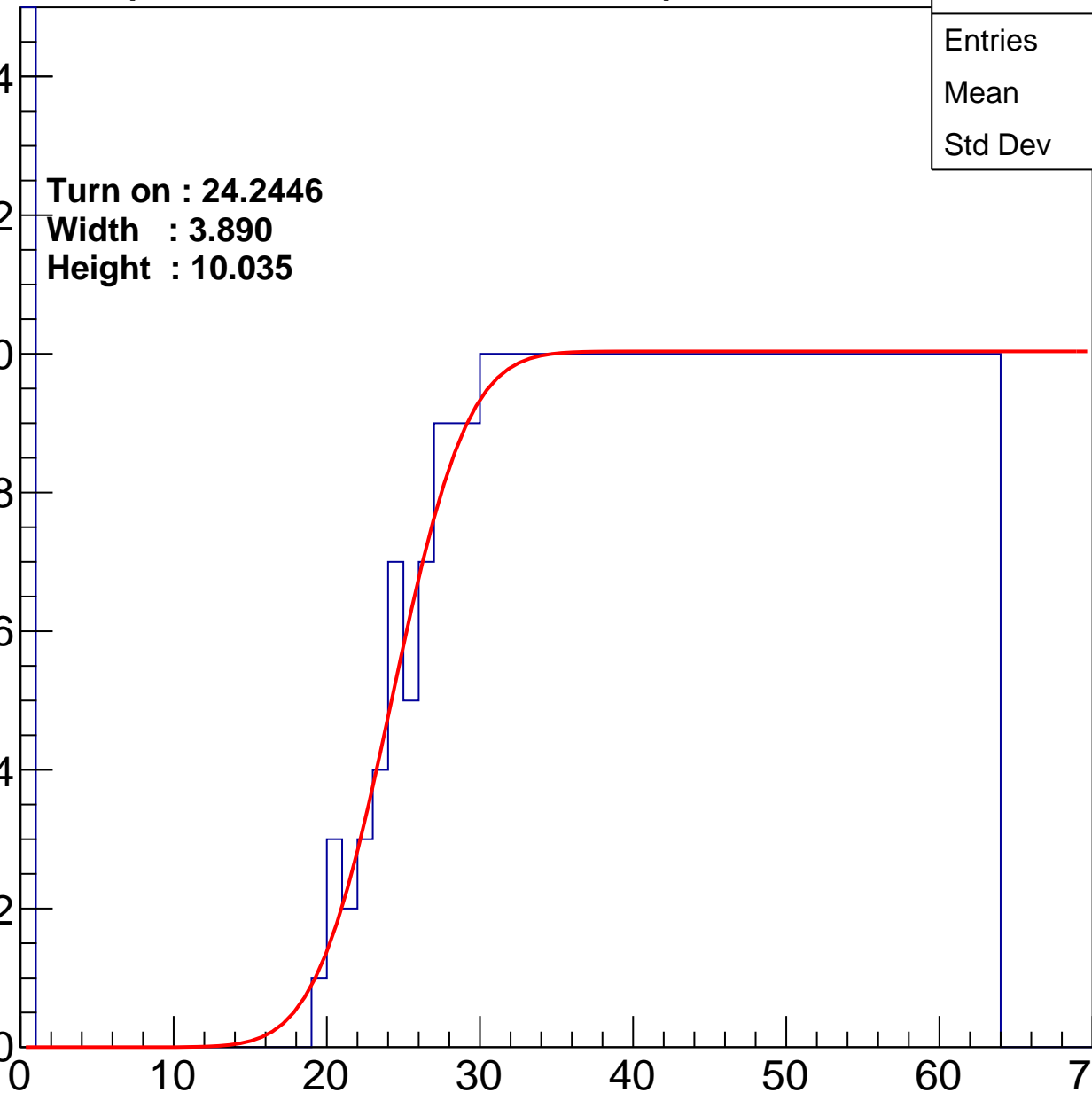
Width : 3.890

Height : 10.035

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch43

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	456
Mean	36.79
Std Dev	19.65

Turn on : 27.1332

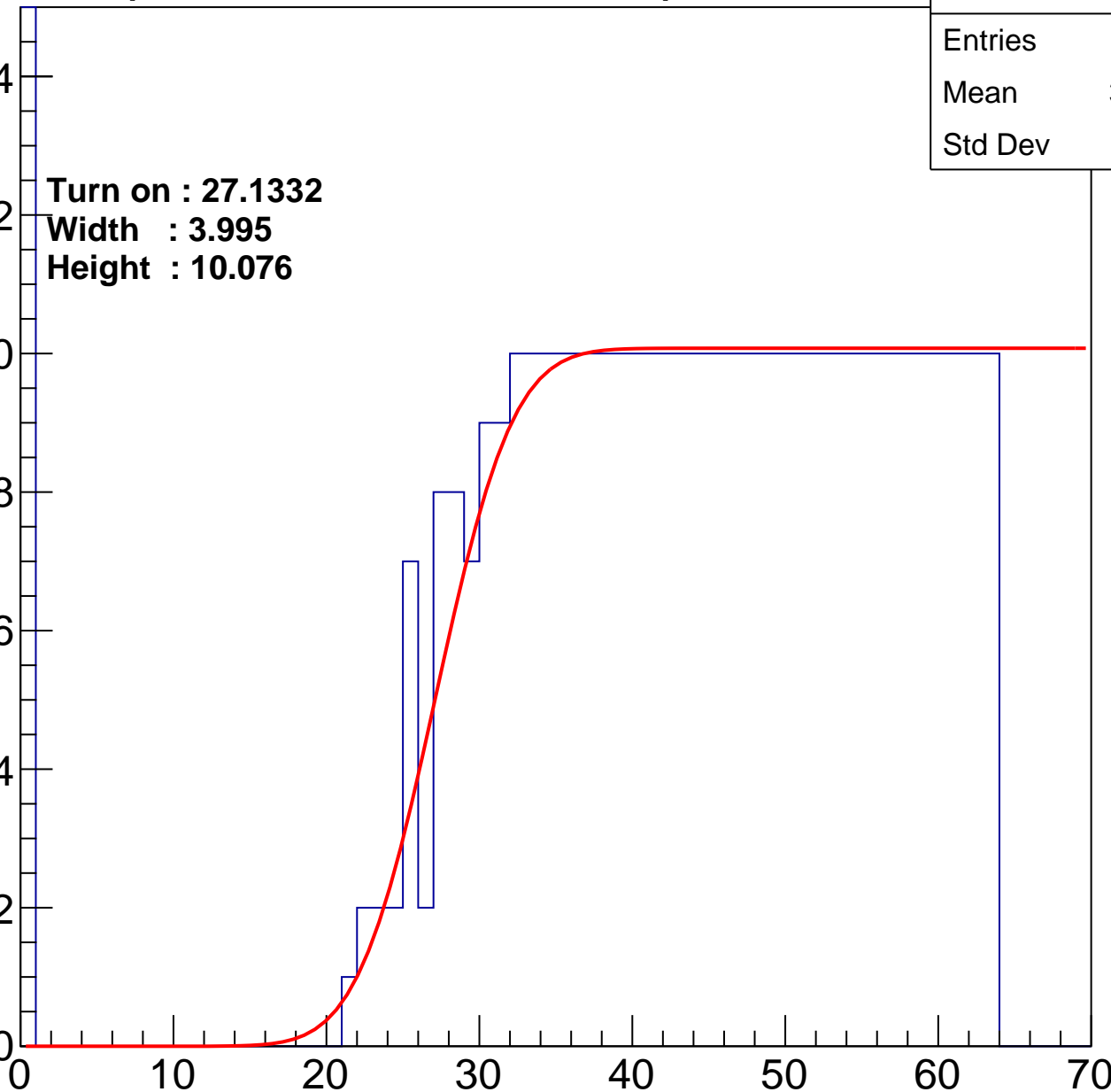
Width : 3.995

Height : 10.076

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch44

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	449
Mean	37.97
Std Dev	18.48

Turn on : 25.4573

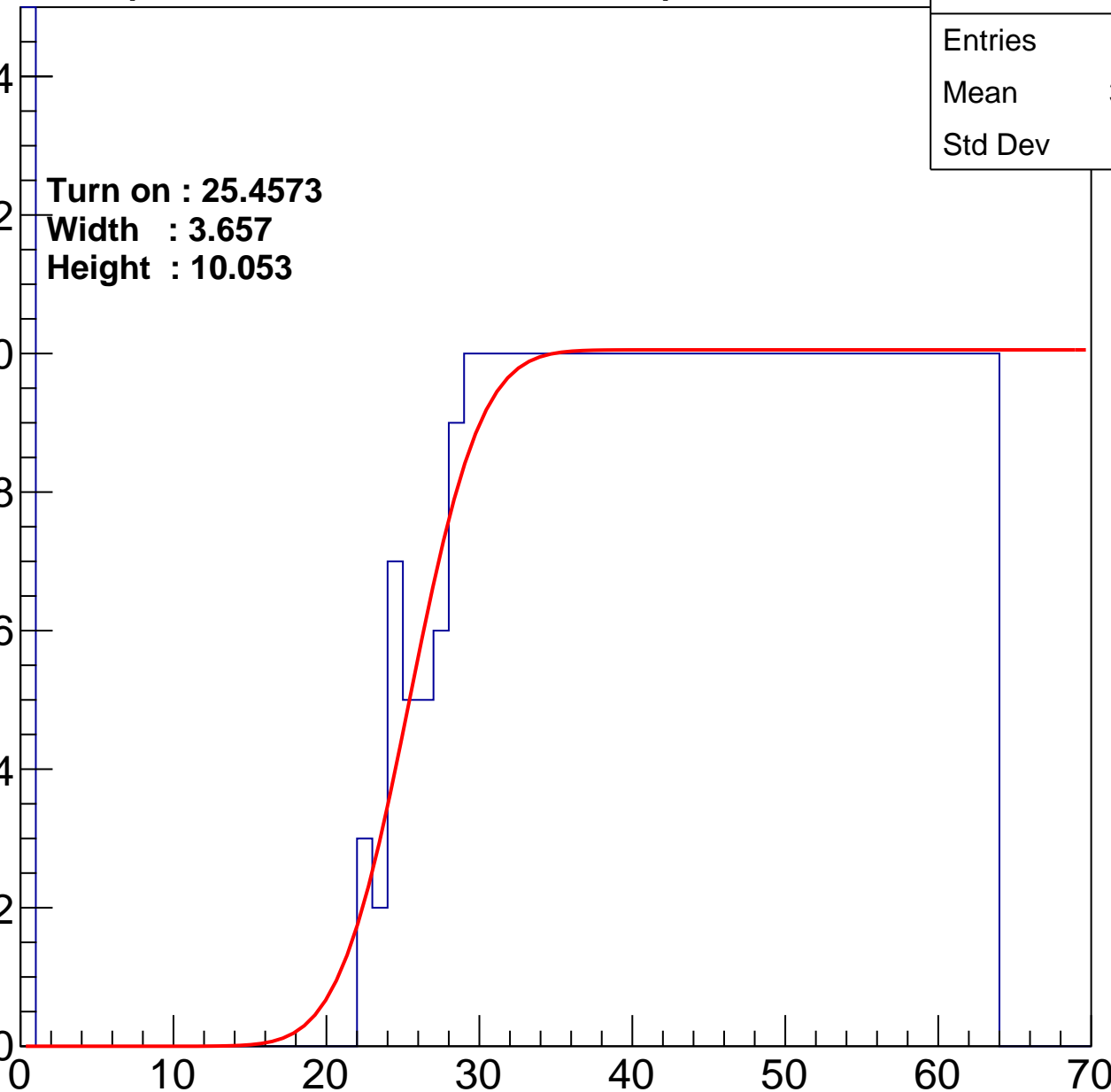
Width : 3.657

Height : 10.053

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch45

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	453
Mean	37.46
Std Dev	18.97

**Turn on : 25.9372**

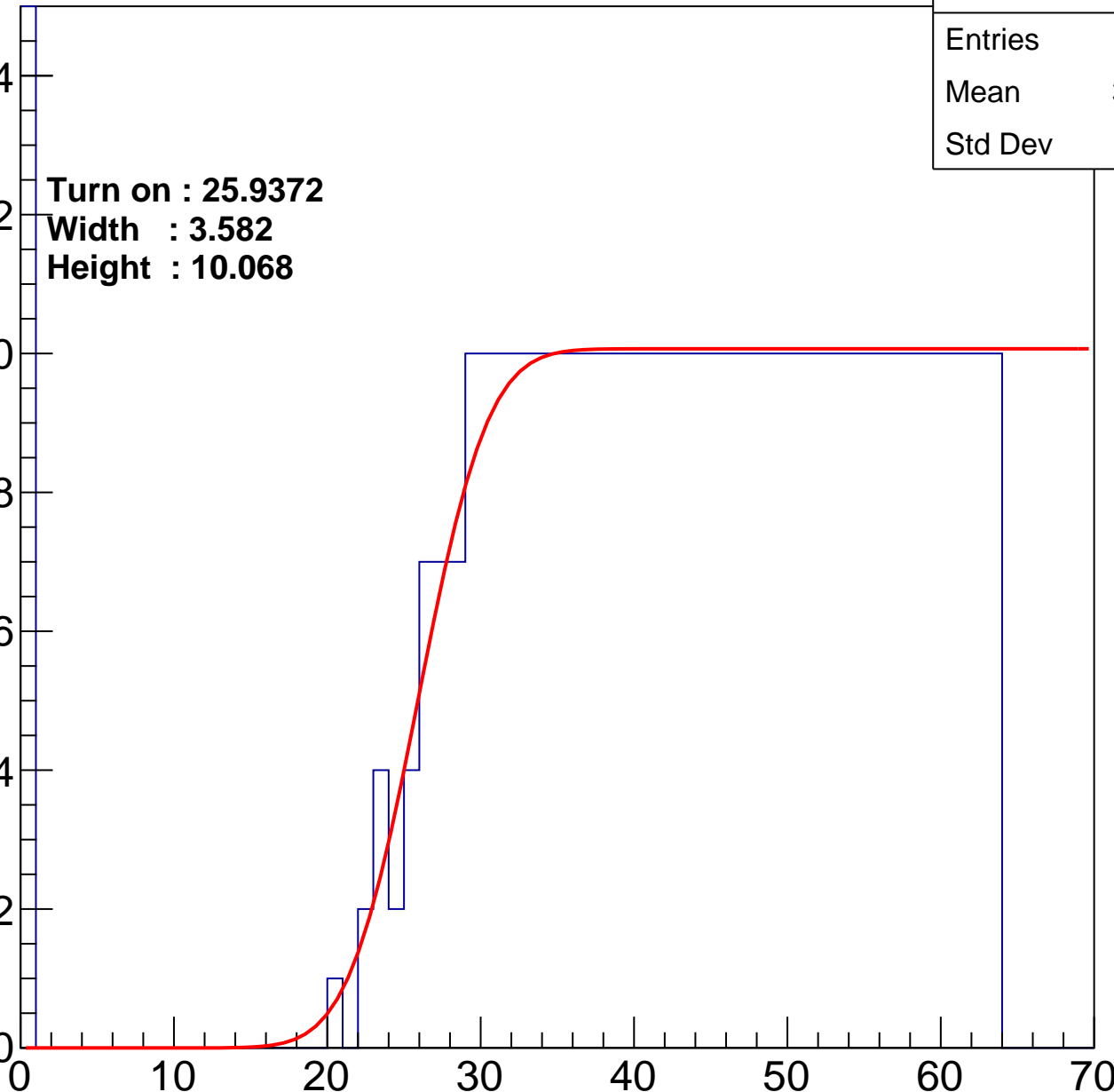
**Width : 3.582**

**Height : 10.068**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch46

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	444
Mean	38.98
Std Dev	17.27

**Turn on : 24.5778**

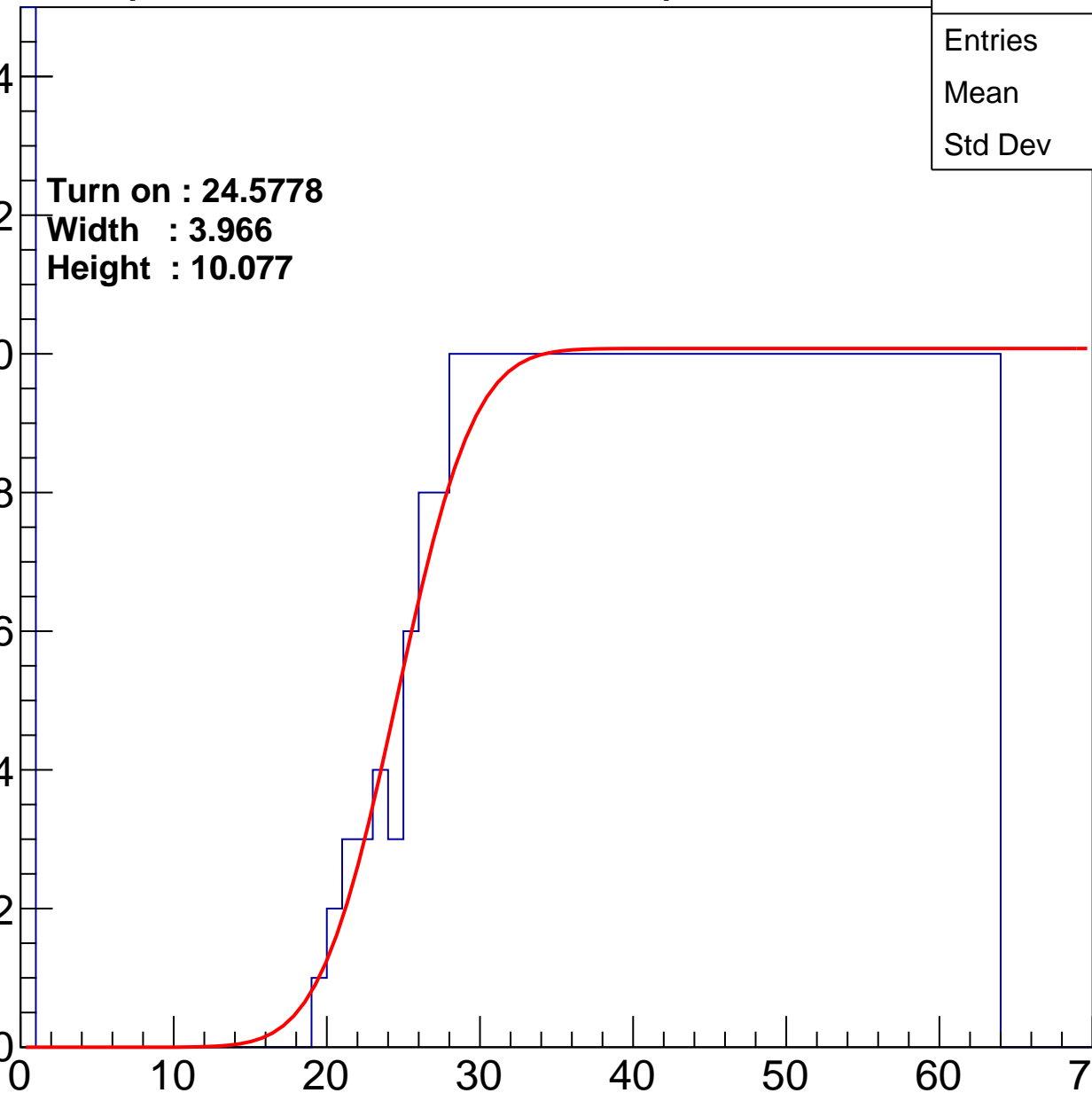
**Width : 3.966**

**Height : 10.077**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L103S, U4-ch47

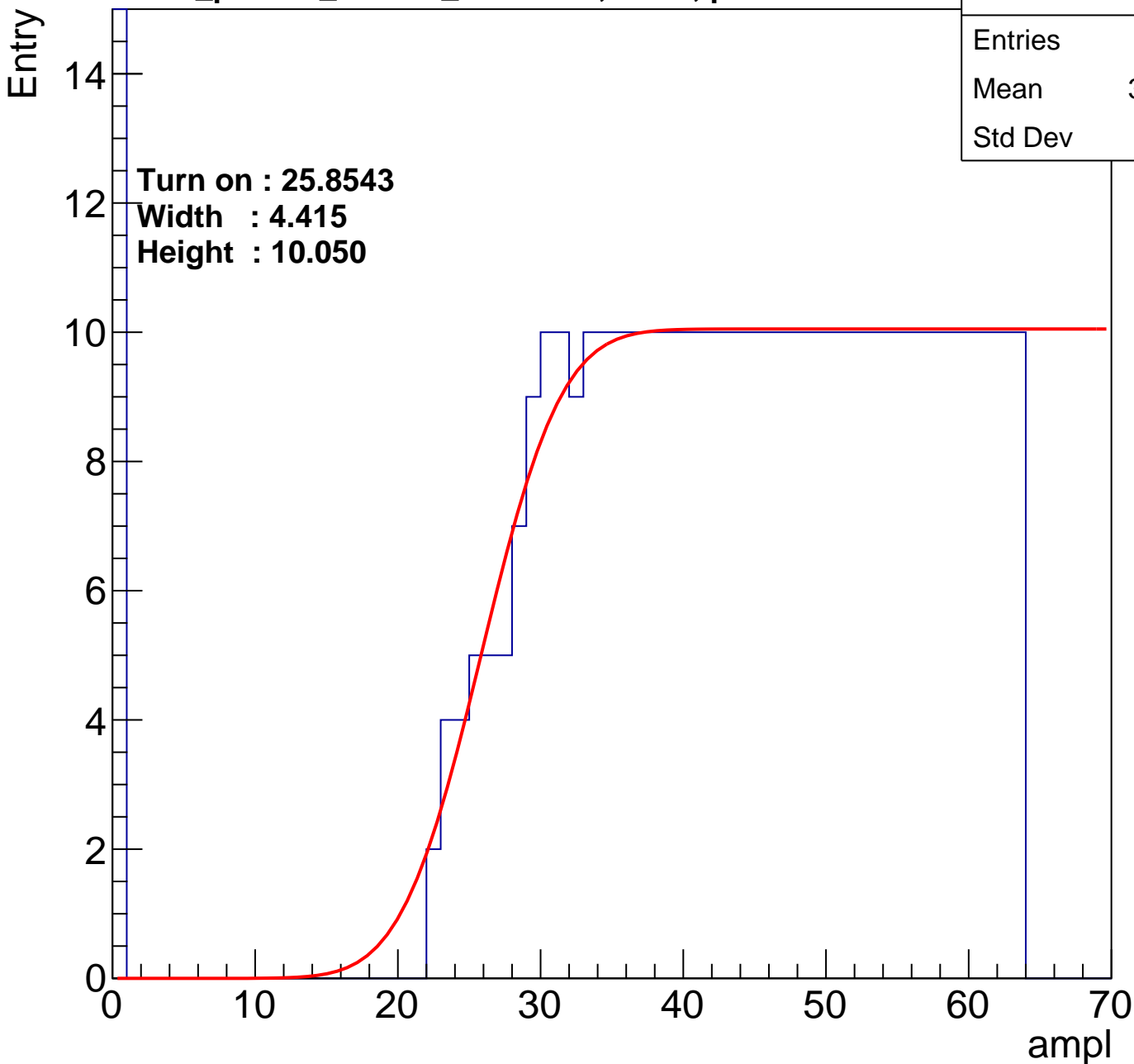
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	429
Mean	39.29
Std Dev	17.61

Turn on : 25.8543

Width : 4.415

Height : 10.050



# B1L103S, U4-ch48

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	443
Mean	38.49
Std Dev	18.07

Turn on : 25.3746

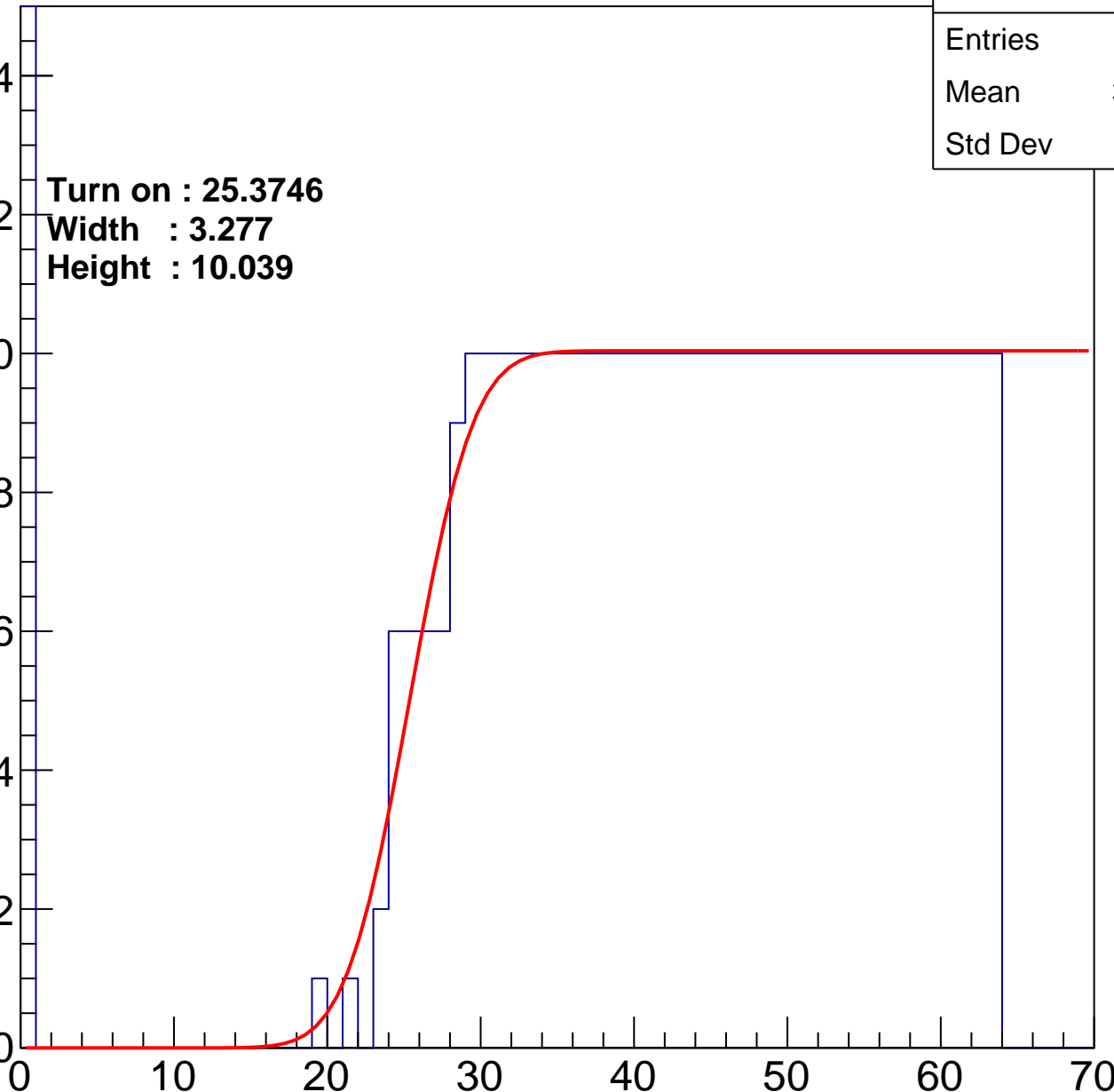
Width : 3.277

Height : 10.039

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch49

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	427
Mean	38.56
Std Dev	18.76

Turn on : 27.7881

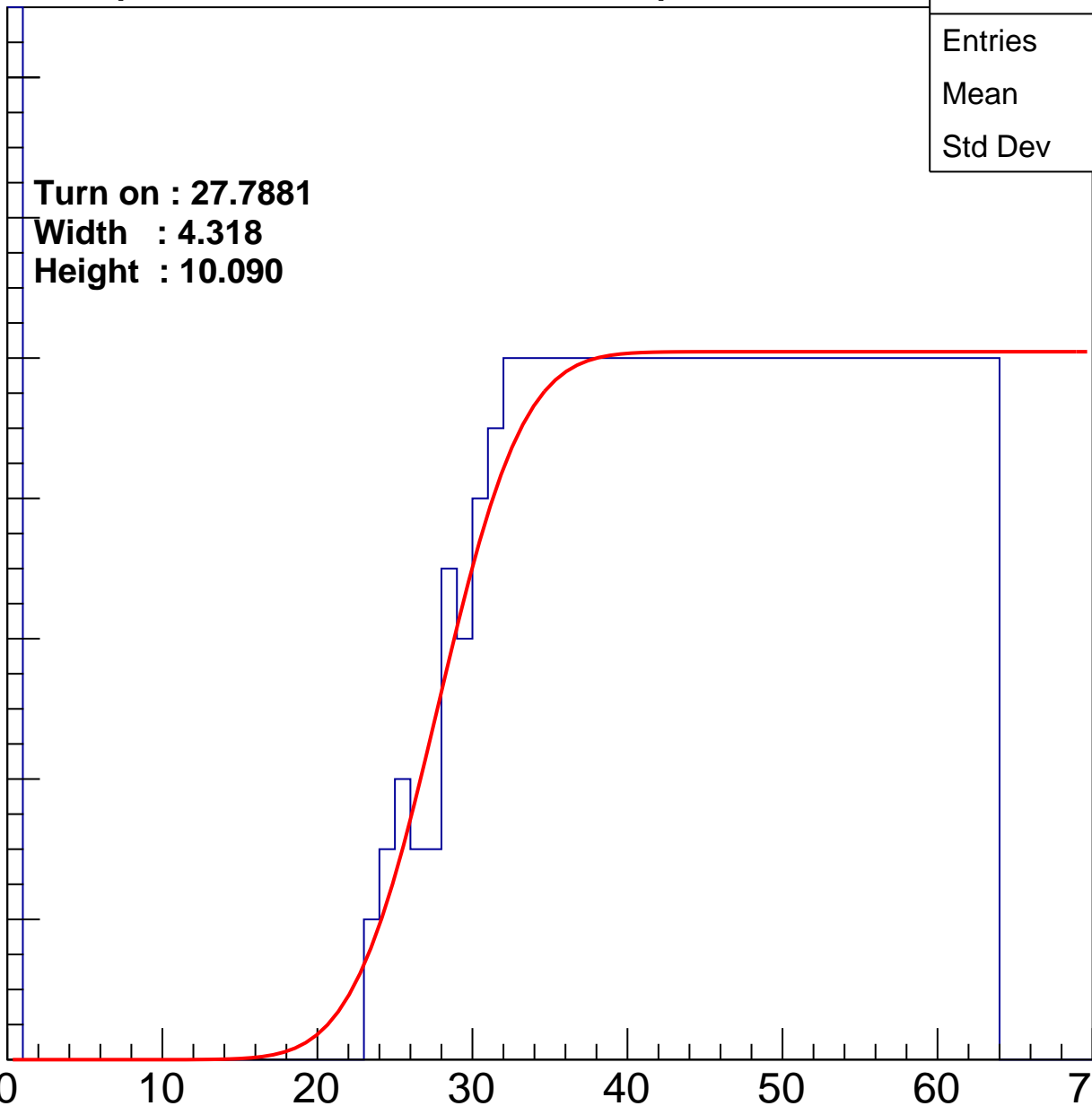
Width : 4.318

Height : 10.090

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch50

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	448
Mean	37.27
Std Dev	19.42

Turn on : 27.0826

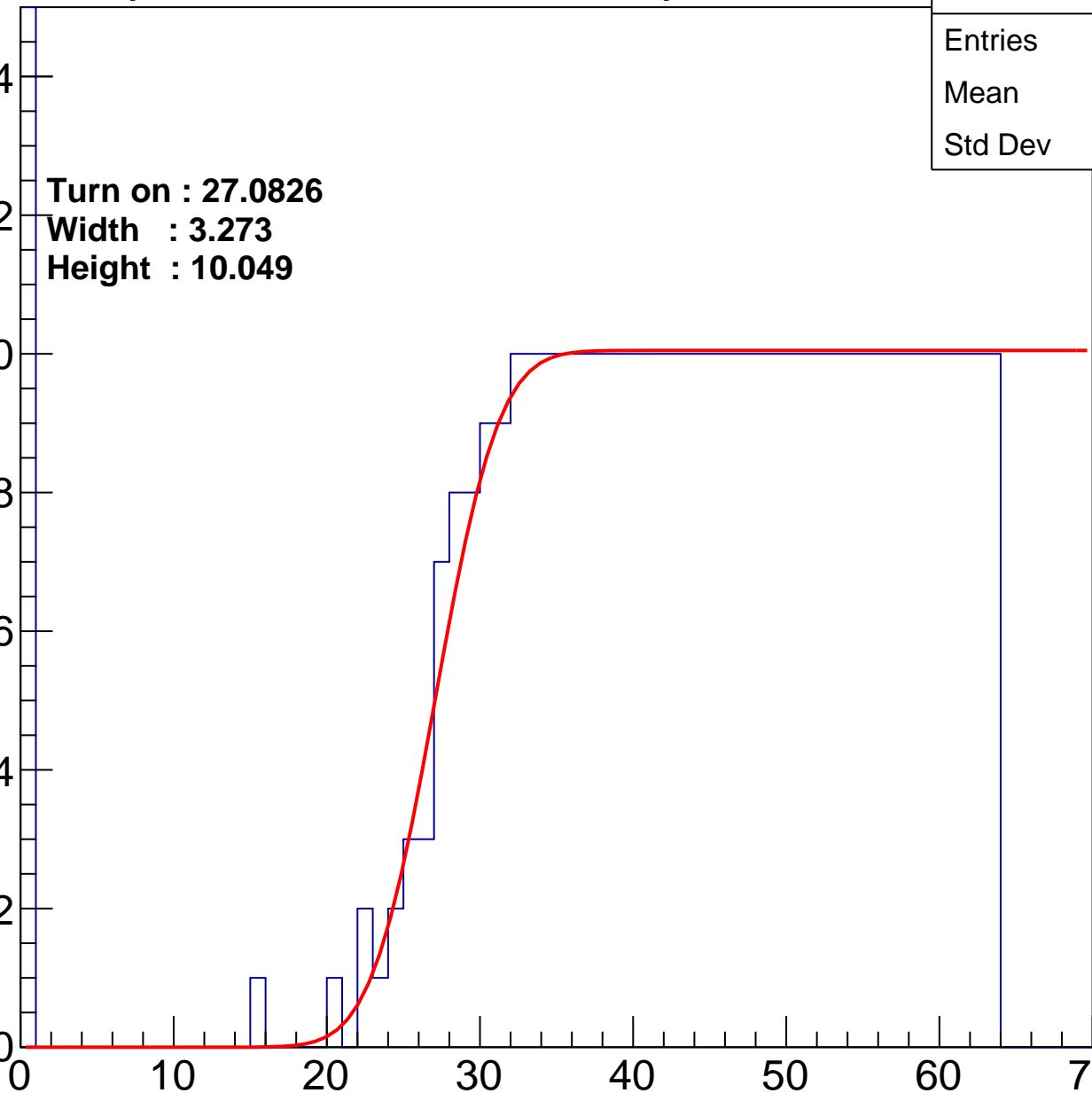
Width : 3.273

Height : 10.049

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch51

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	436
Mean	38.96
Std Dev	17.78

Turn on : 25.7643

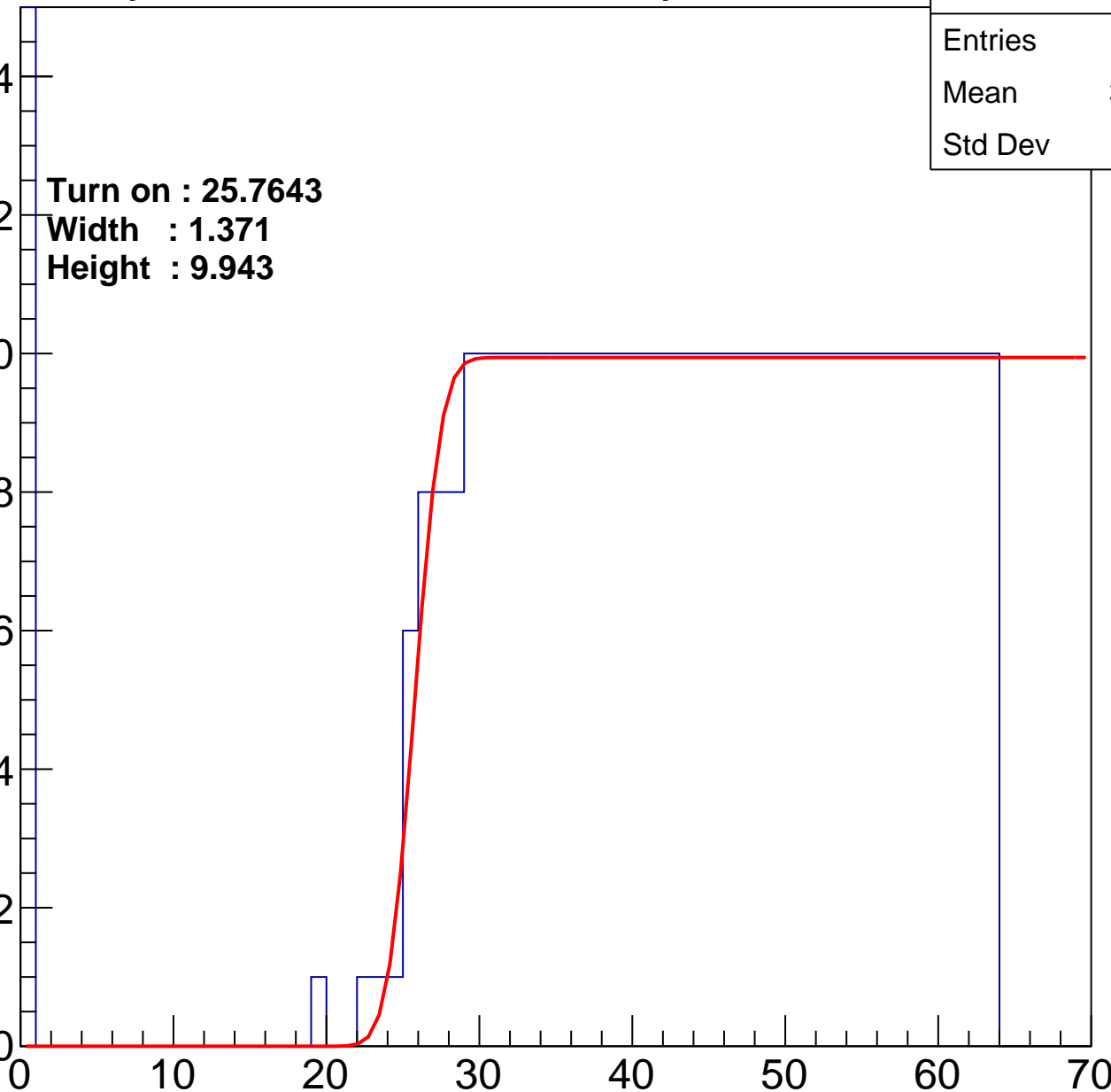
Width : 1.371

Height : 9.943

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch52

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	453
Mean	38.55
Std Dev	17.44

Turn on : 23.8580

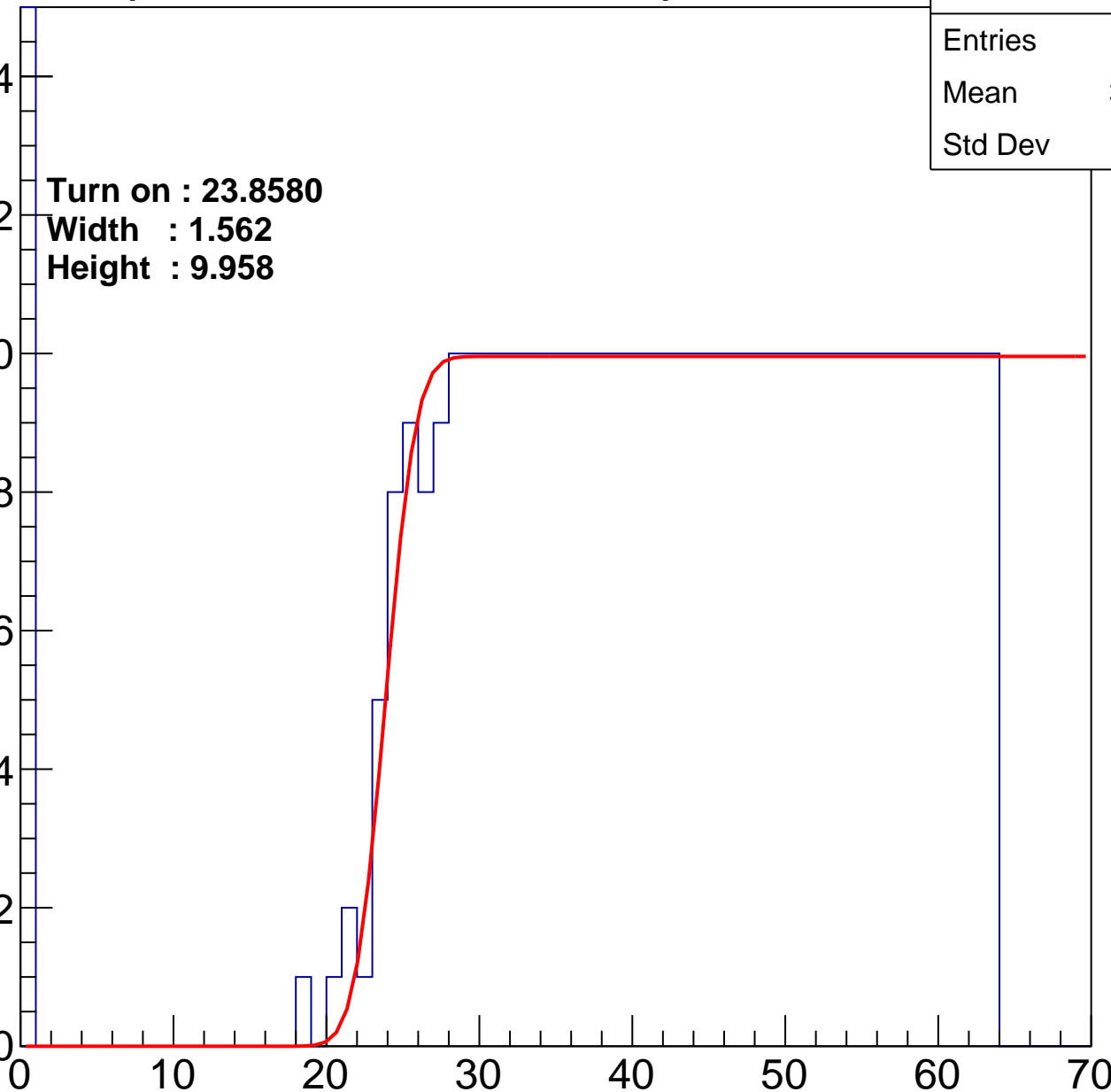
Width : 1.562

Height : 9.958

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch53

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	436
Mean	38.77
Std Dev	18.04

**Turn on : 26.2325**

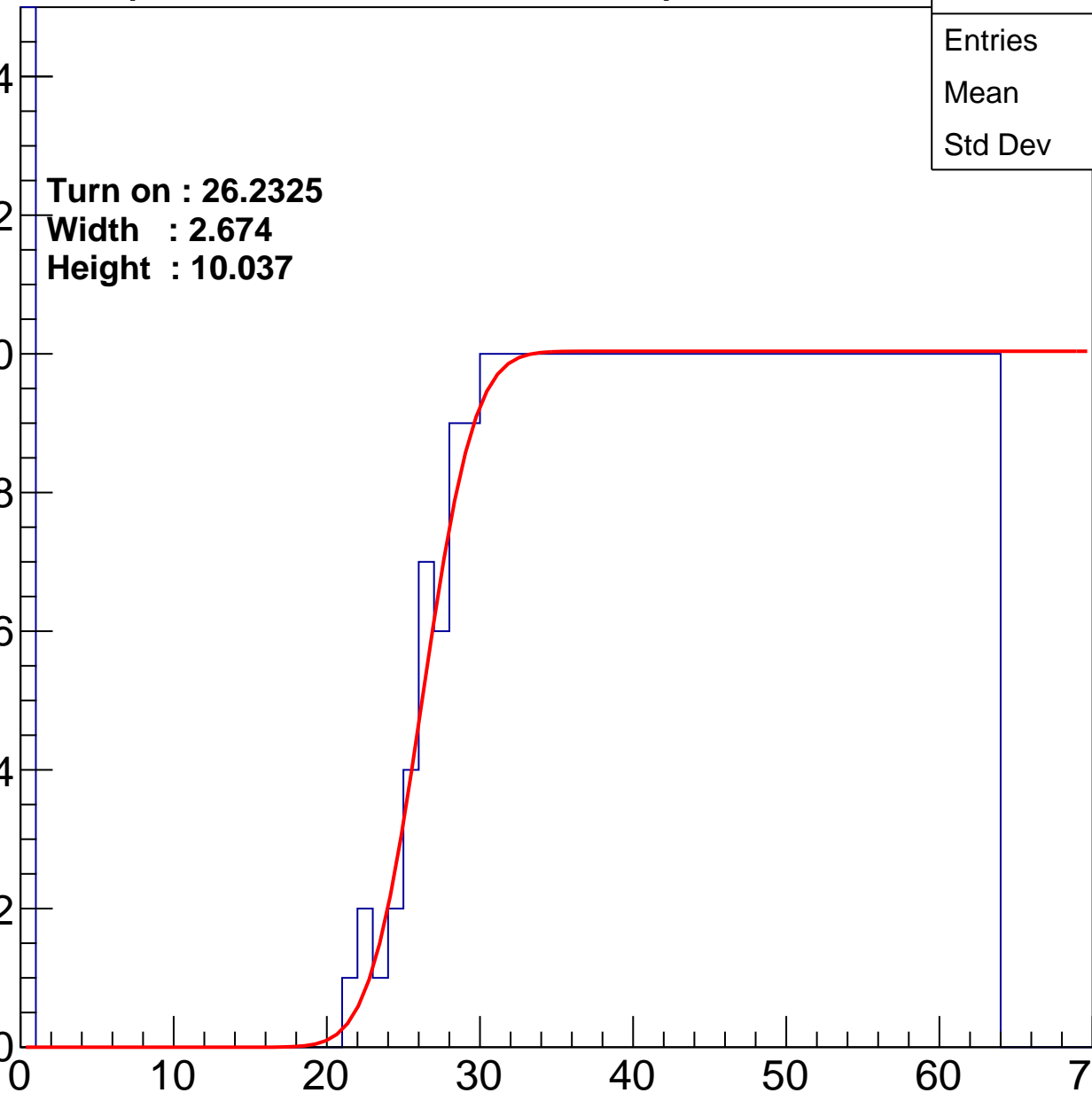
**Width : 2.674**

**Height : 10.037**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch54

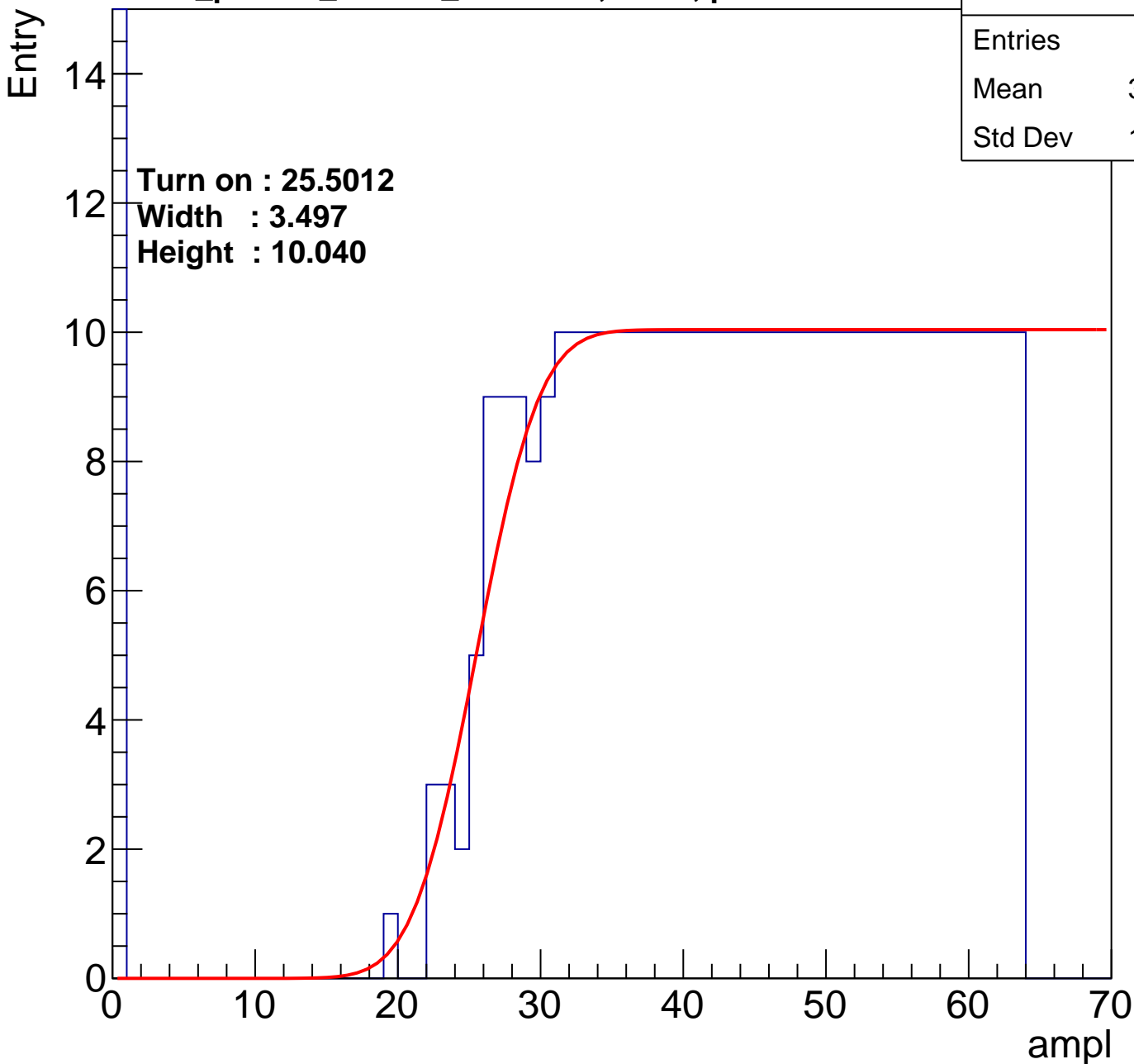
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	440
Mean	38.79
Std Dev	17.77

Turn on : 25.5012

Width : 3.497

Height : 10.040





# B1L103S, U4-ch55

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	430
Mean	38.89
Std Dev	18.19

Turn on : 26.6357

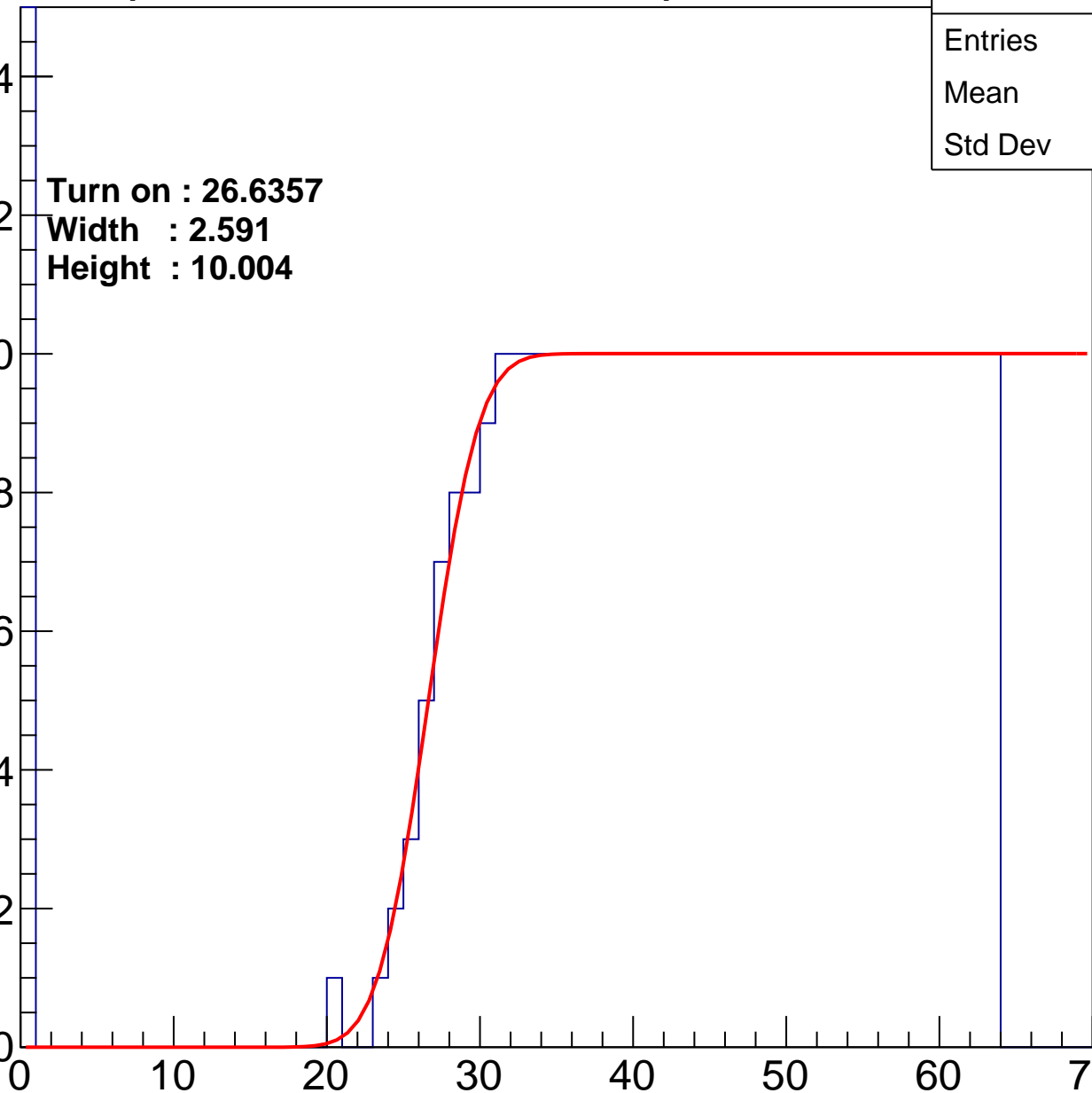
Width : 2.591

Height : 10.004

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch56

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	420
Mean	39.85
Std Dev	17.3

Turn on : 27.2223

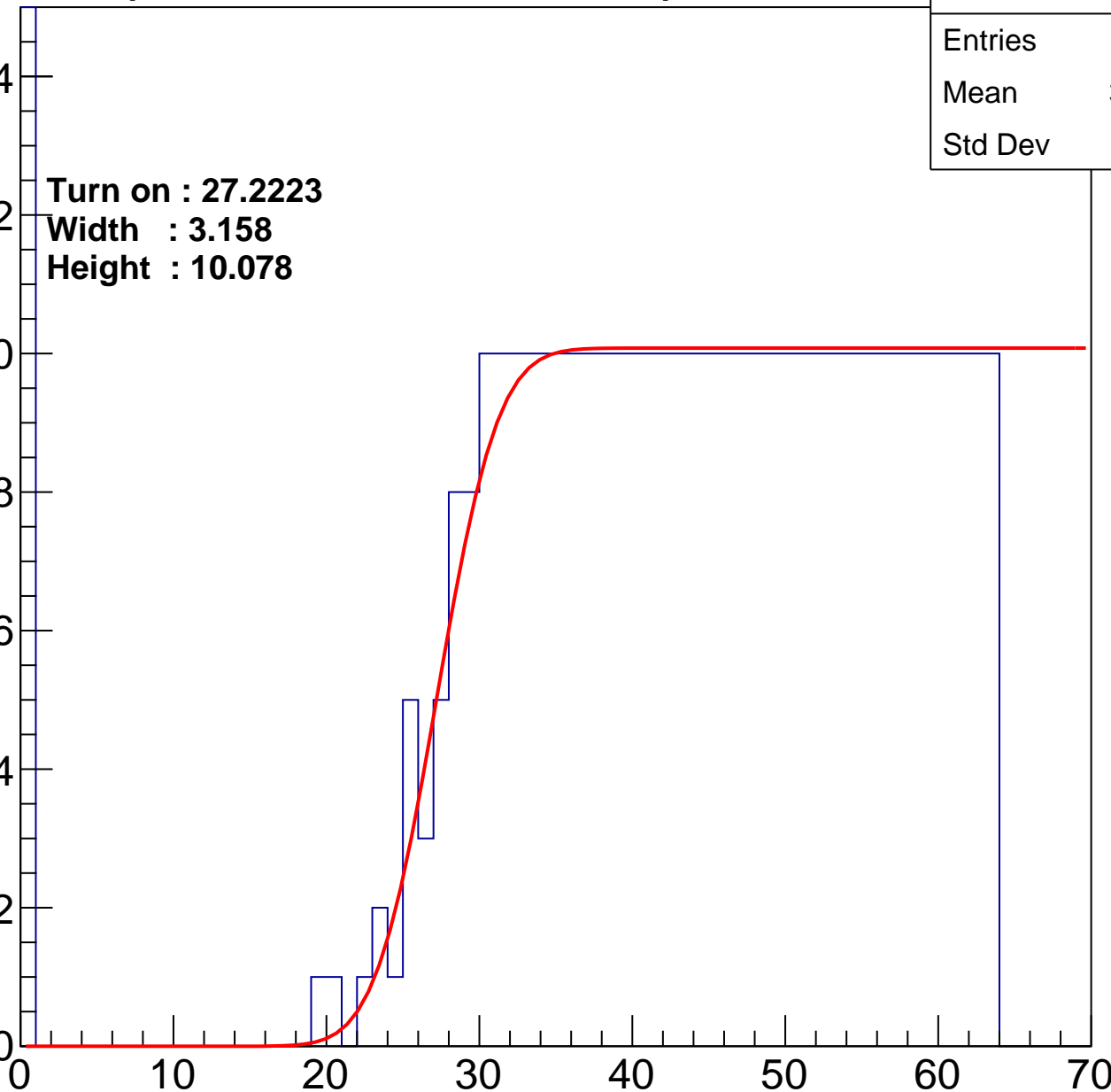
Width : 3.158

Height : 10.078

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch57

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	428
Mean	39.03
Std Dev	18.07

Turn on : 27.4117

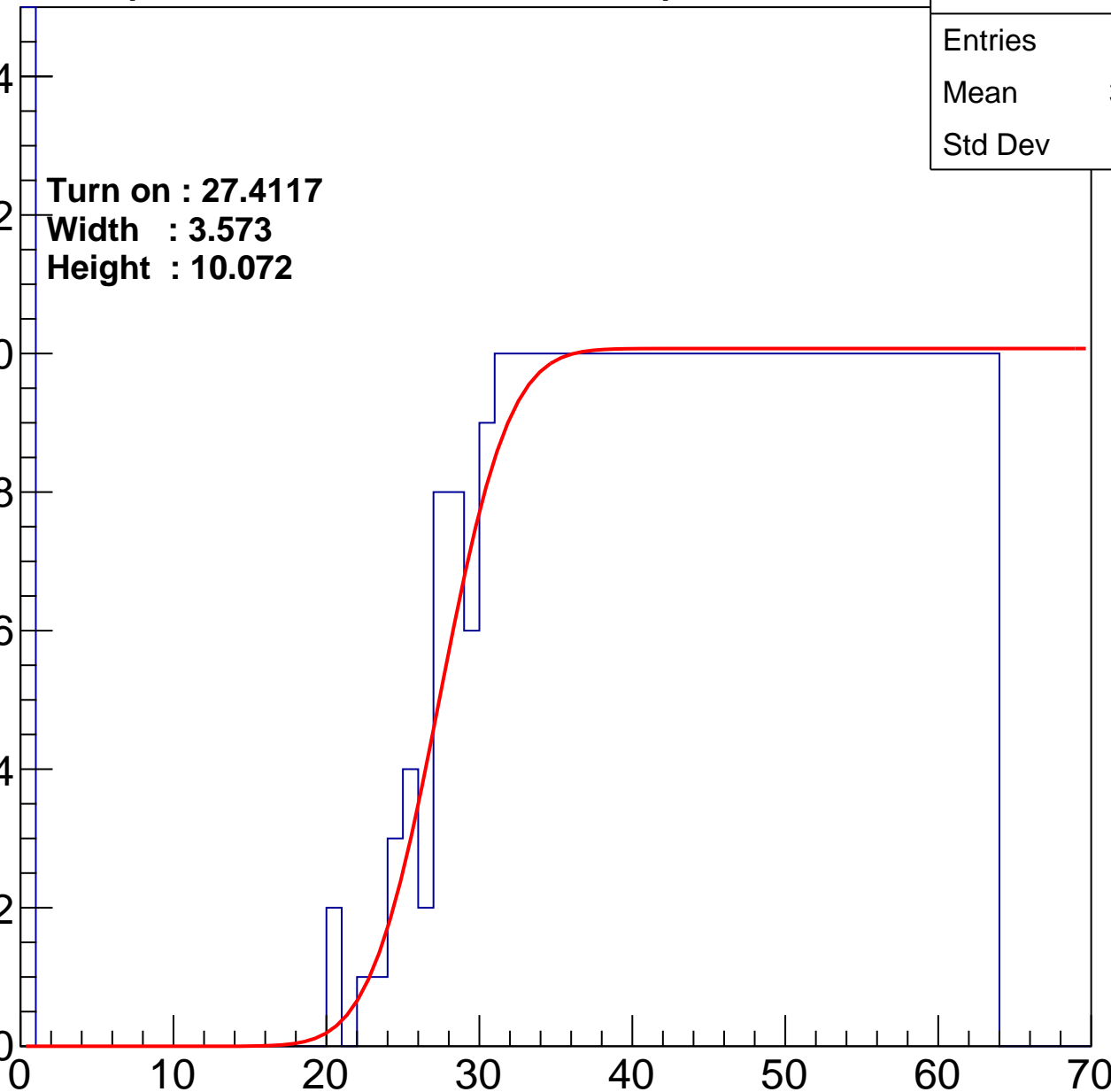
Width : 3.573

Height : 10.072

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch58

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	434
Mean	38.78
Std Dev	18.1

Turn on : 26.7615

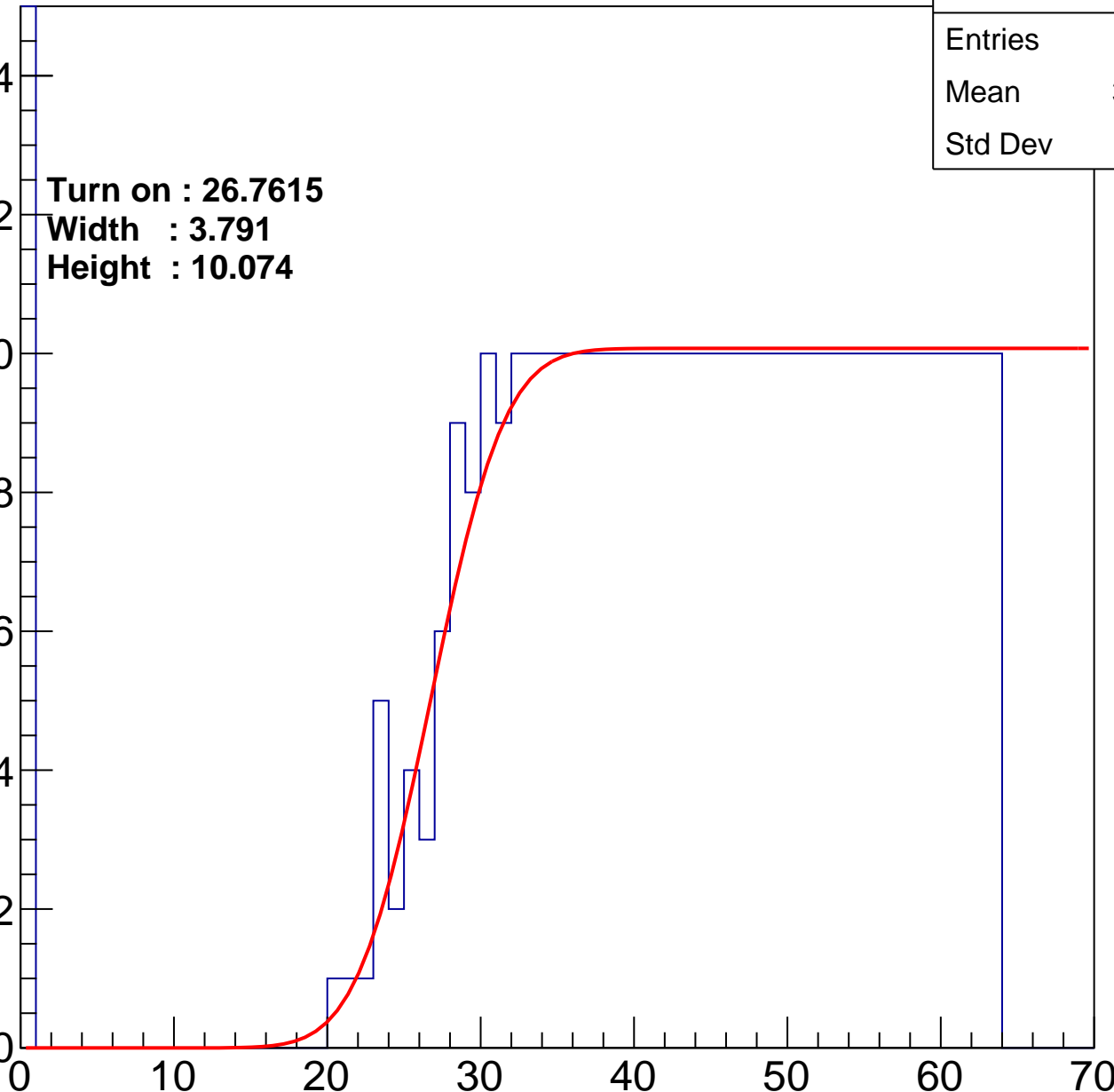
Width : 3.791

Height : 10.074

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch59

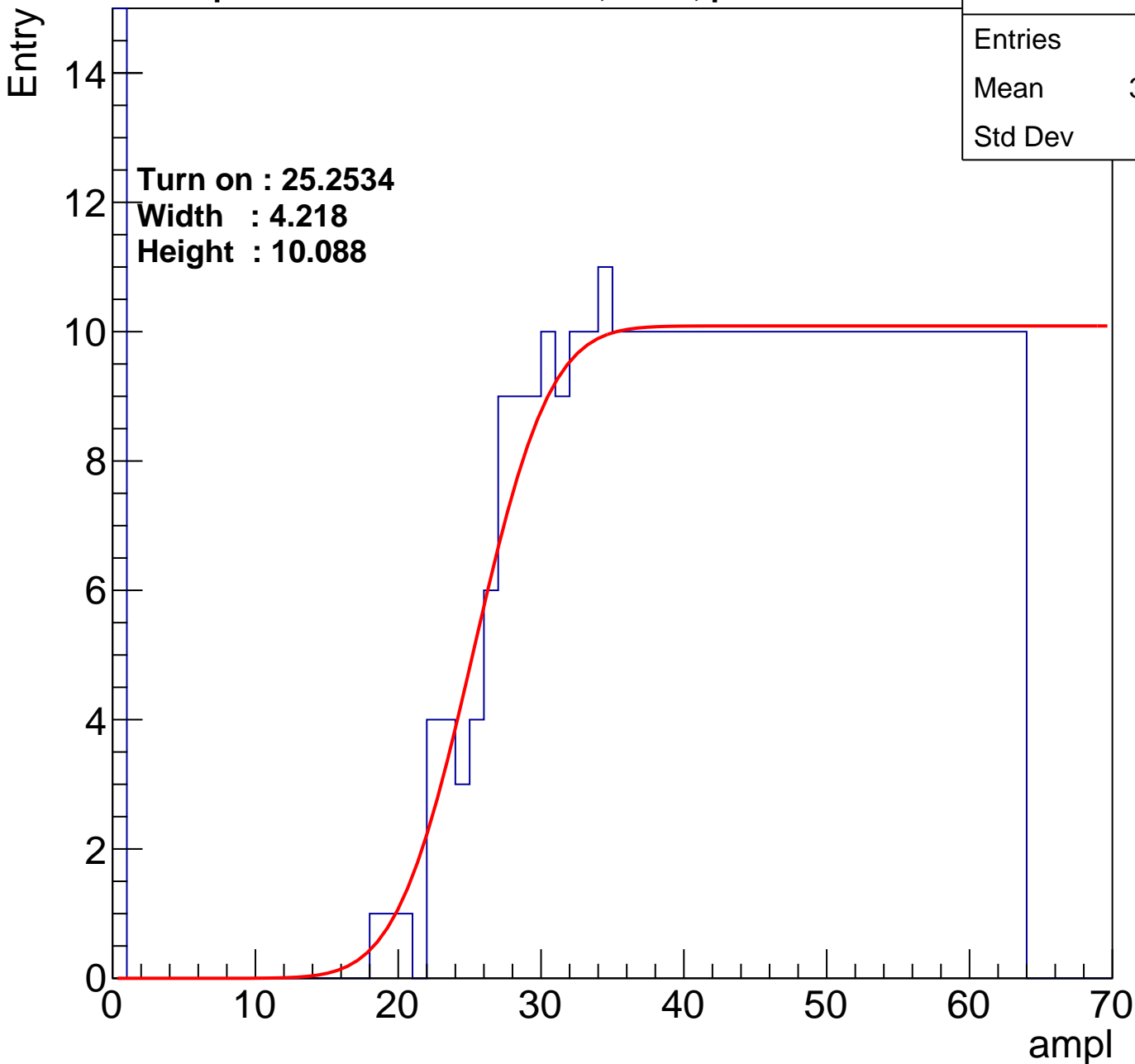
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	446
Mean	38.42
Std Dev	18

Turn on : 25.2534

Width : 4.218

Height : 10.088



# B1L103S, U4-ch60

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	452
Mean	37.9
Std Dev	18.44

Turn on : 25.1361

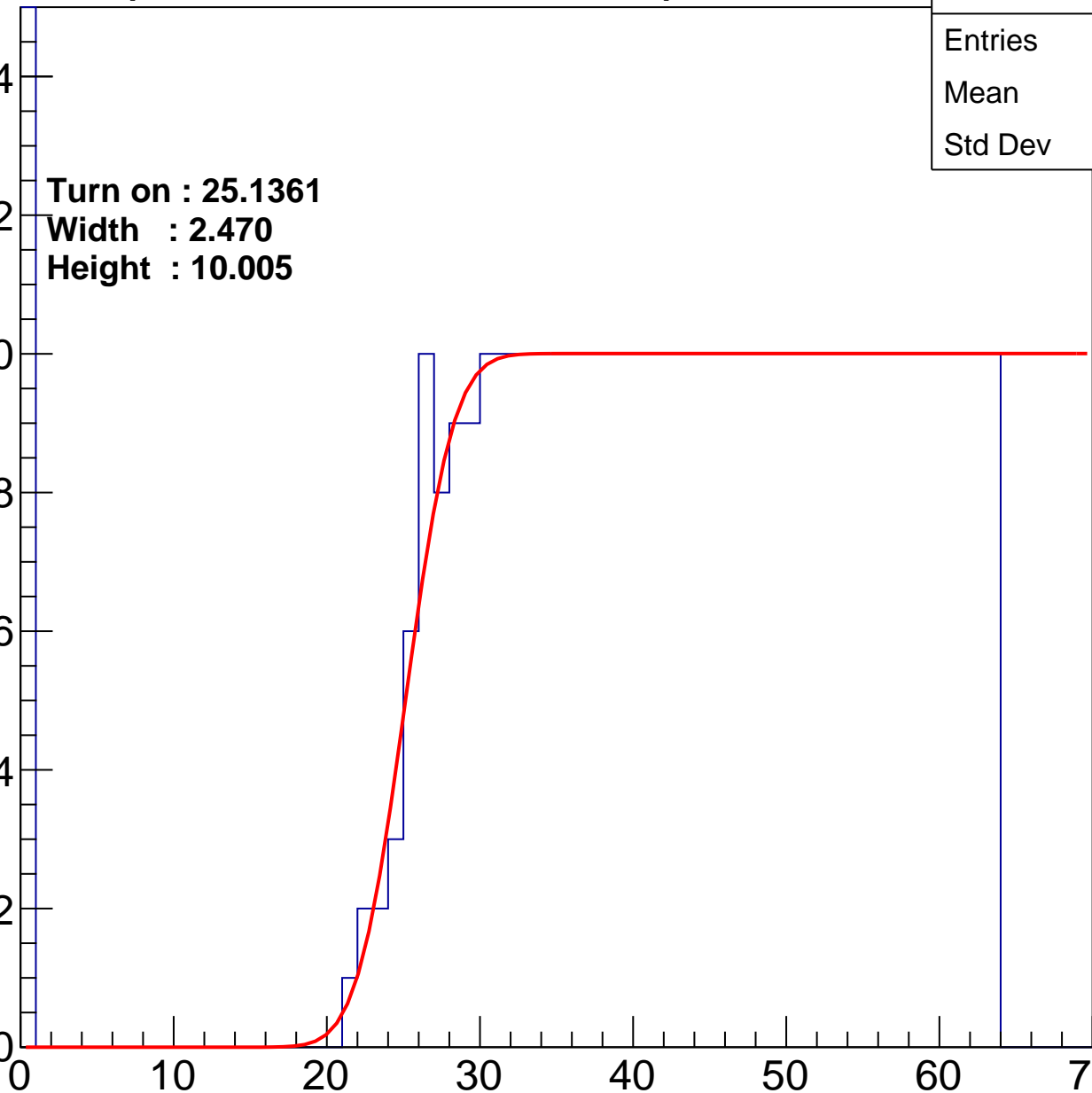
Width : 2.470

Height : 10.005

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch61

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	464
Mean	36.19
Std Dev	20.04

Turn on : 26.1852

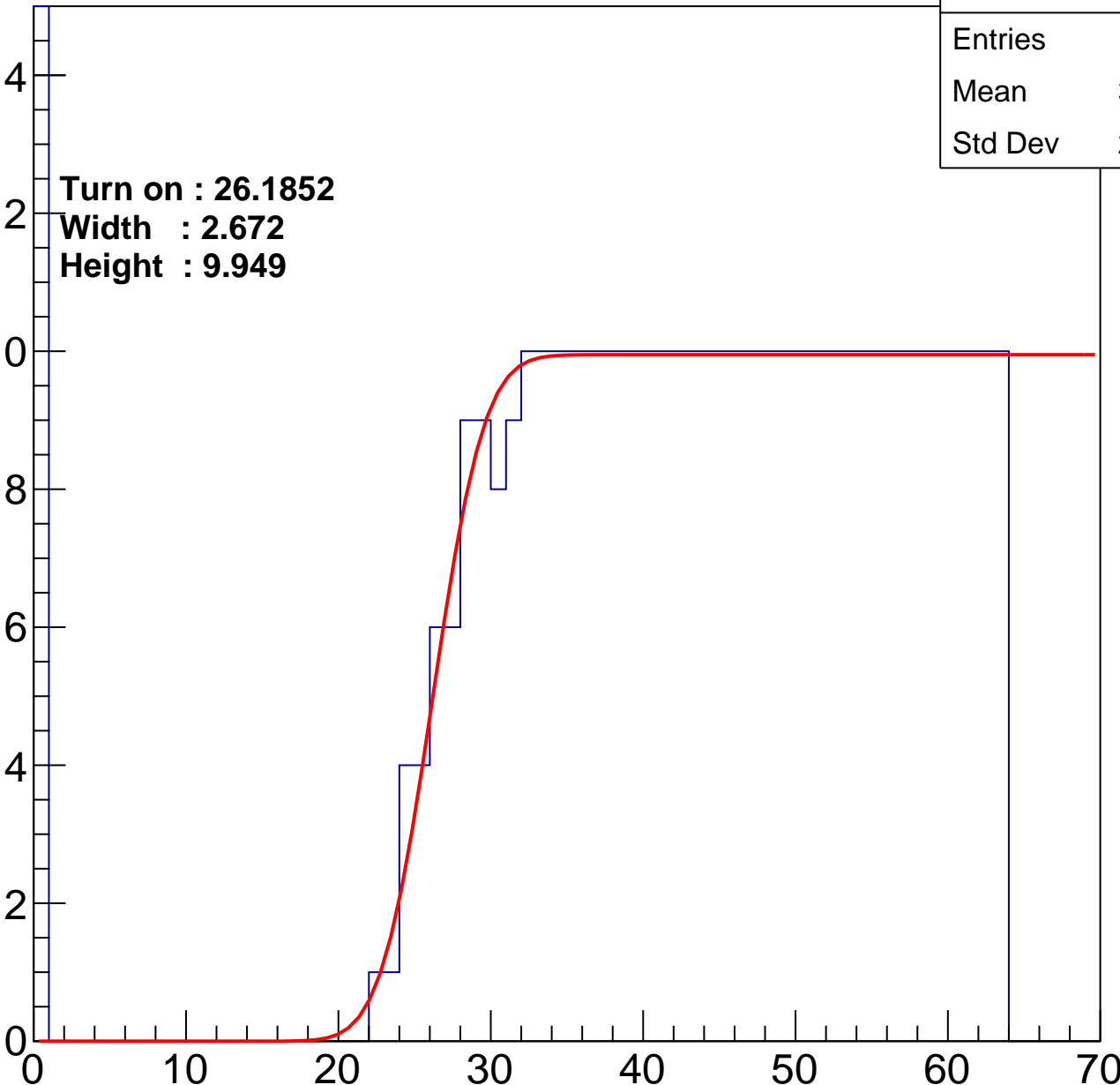
Width : 2.672

Height : 9.949

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch62

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	441
Mean	38.05
Std Dev	18.79

Turn on : 26.2840

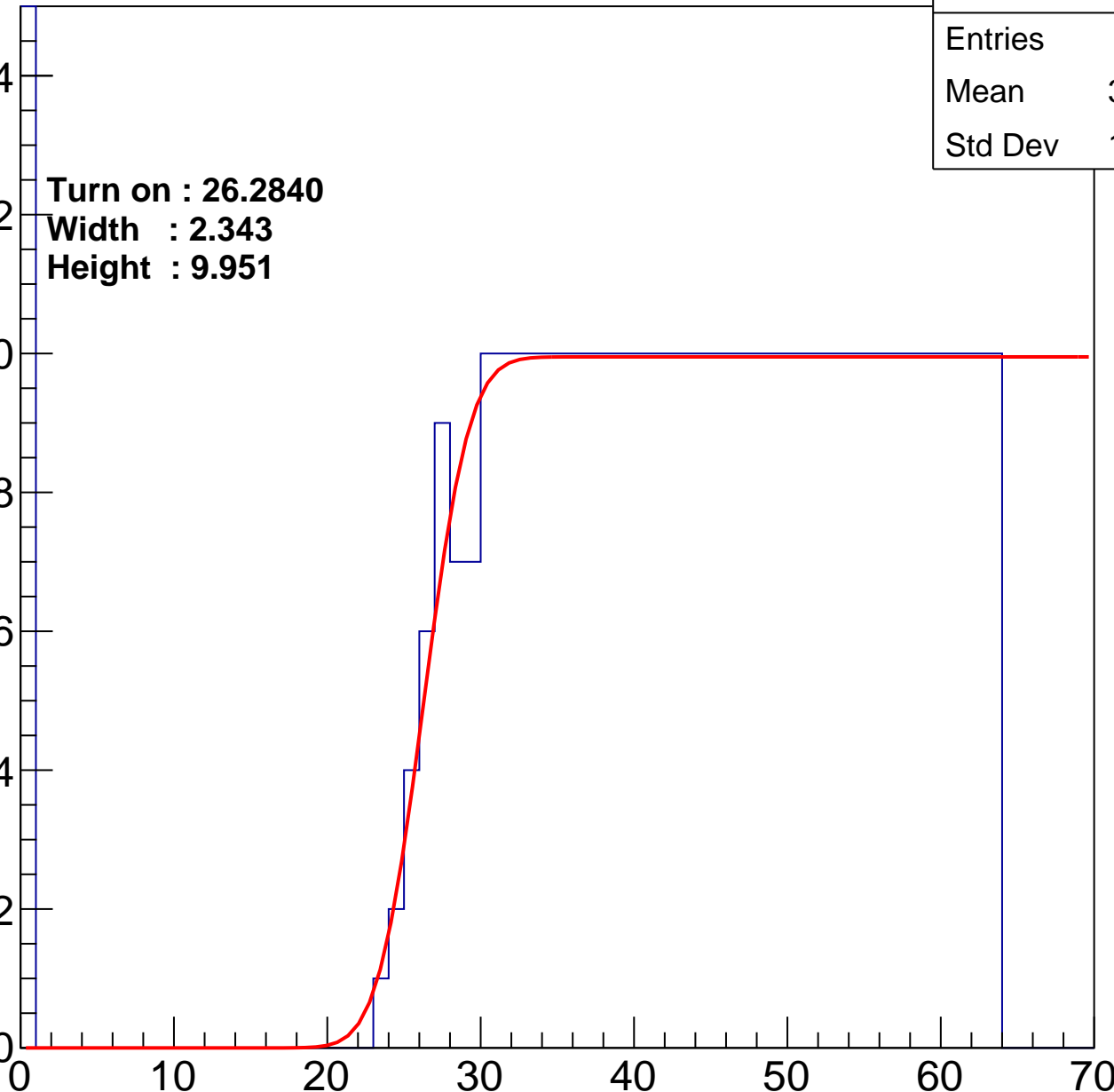
Width : 2.343

Height : 9.951

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L103S, U4-ch63

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	444
Mean	37.63
Std Dev	19.2

Turn on : 27.0160

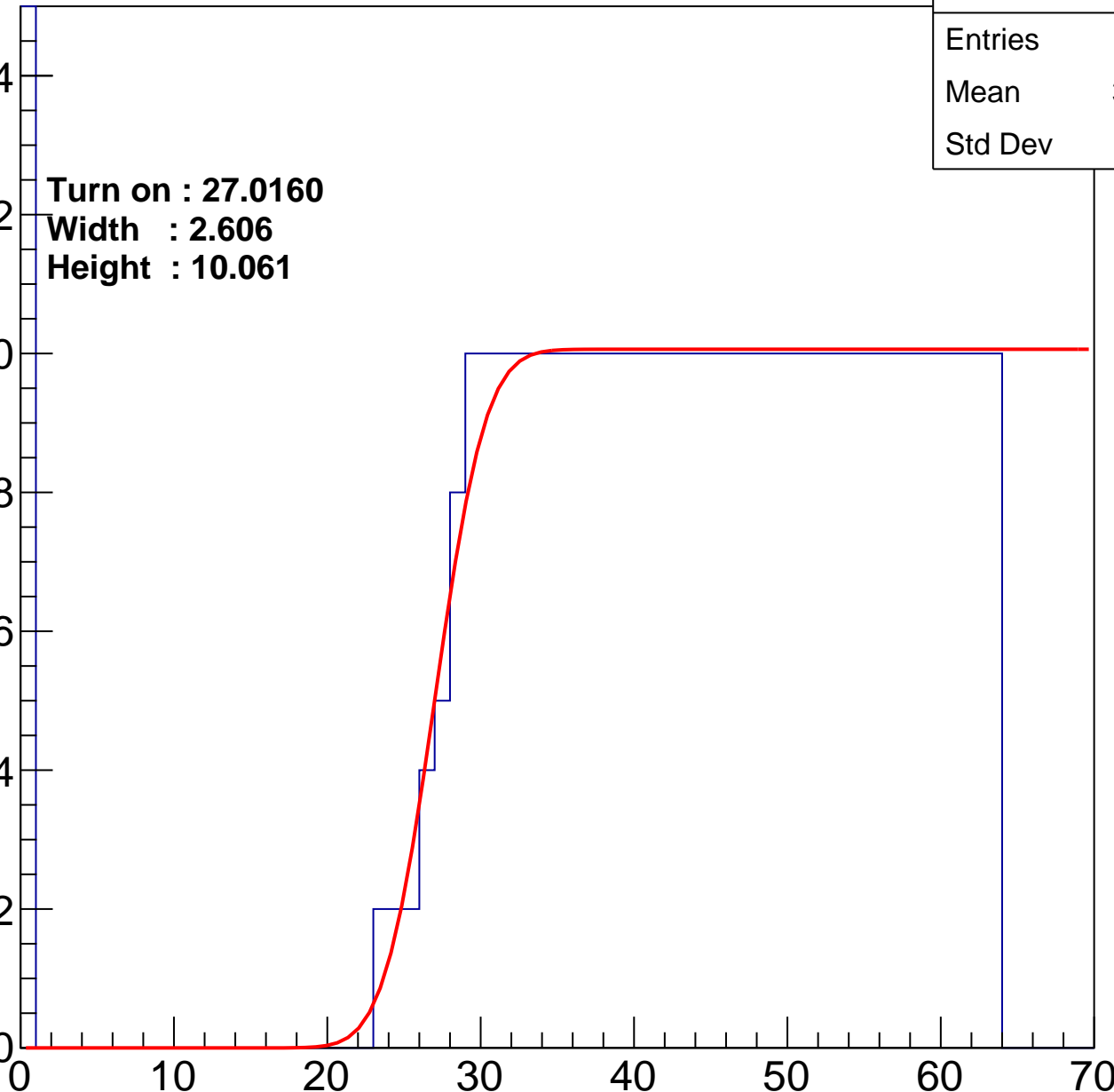
Width : 2.606

Height : 10.061

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch64

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	438
Mean	38.94
Std Dev	17.65

Turn on : 26.0935

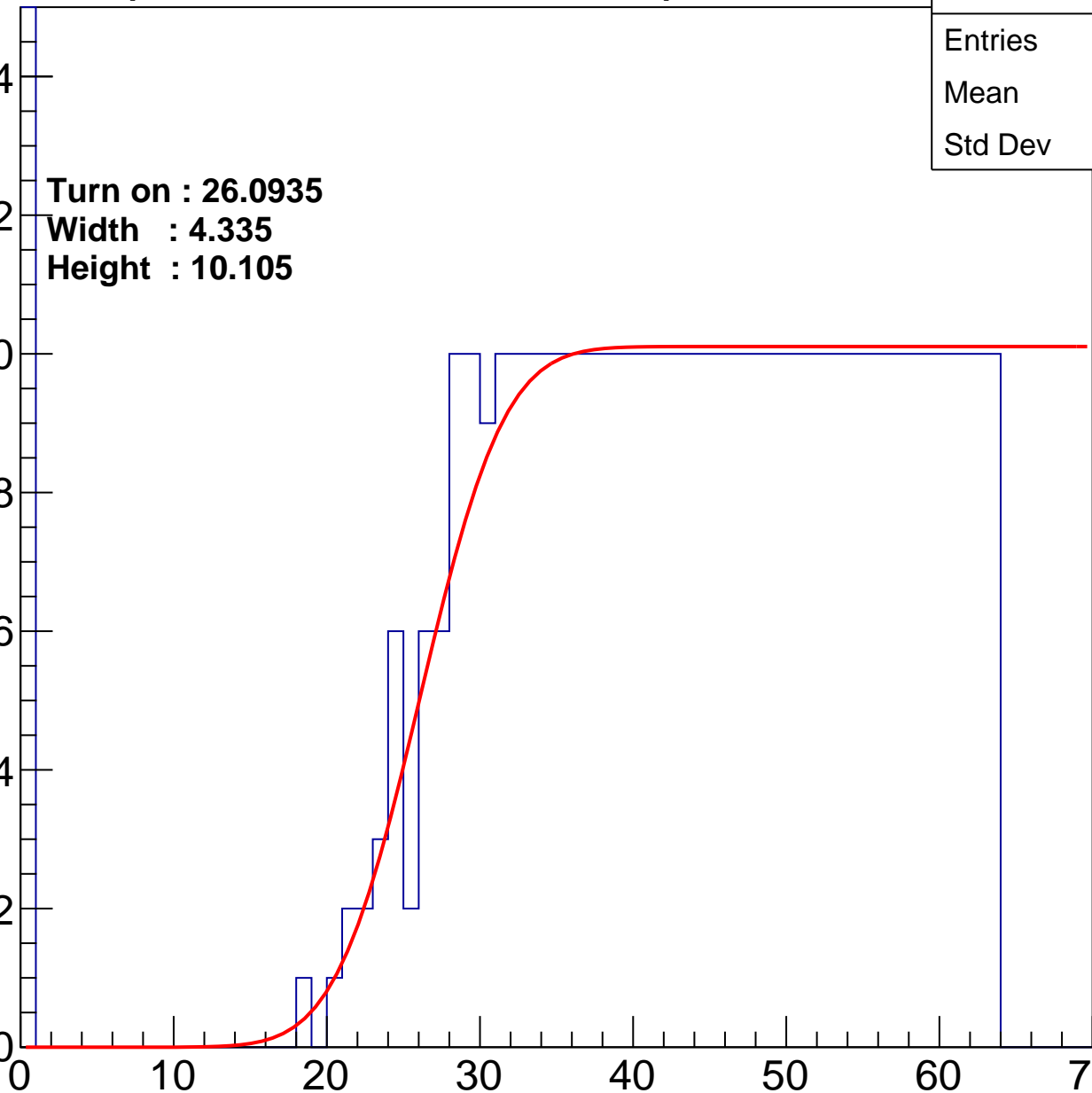
Width : 4.335

Height : 10.105

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch65

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	473
Mean	36.45
Std Dev	19.34

Turn on : 24.5827

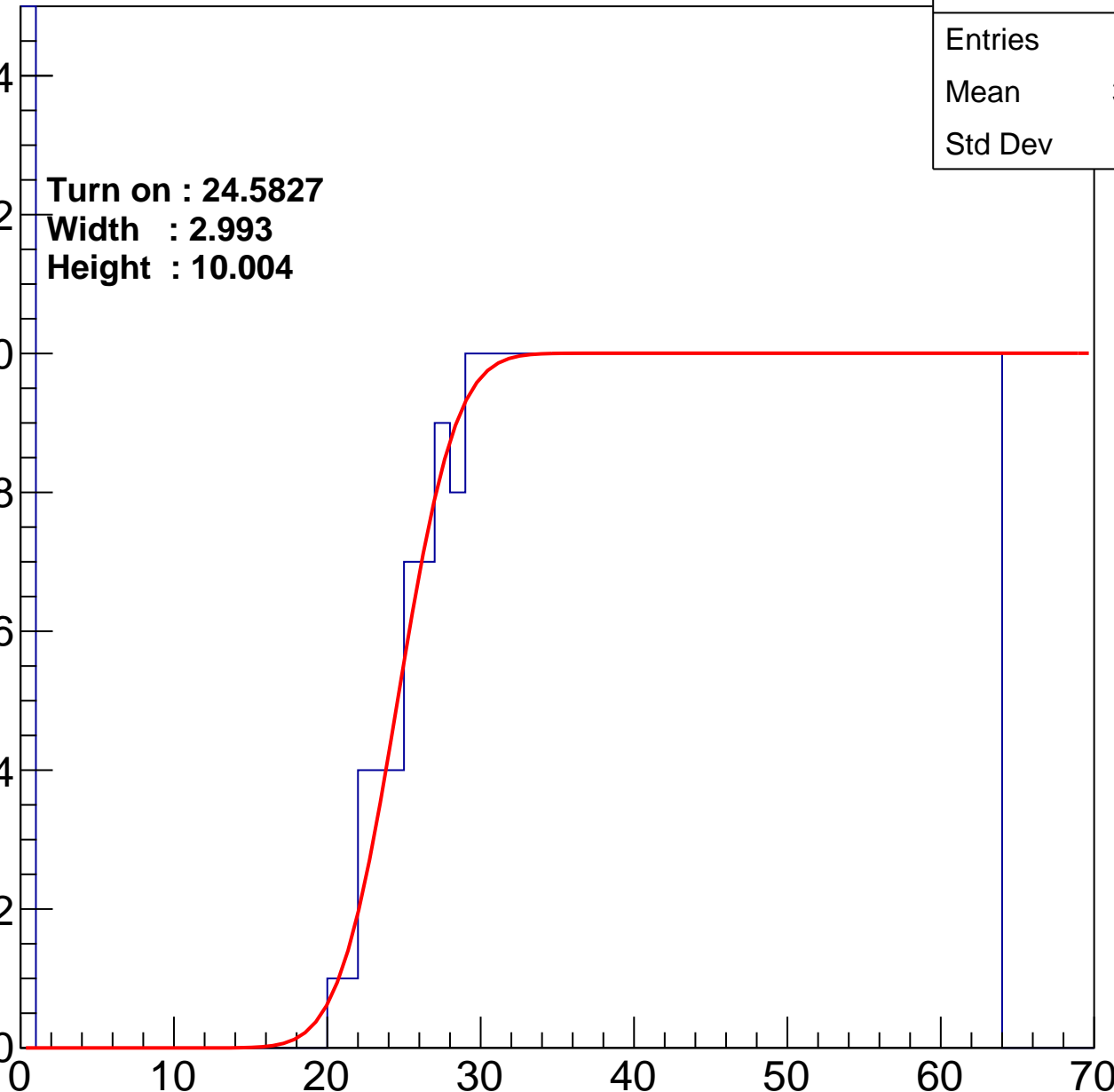
Width : 2.993

Height : 10.004

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch66

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	426
Mean	39.95
Std Dev	16.78

Turn on : 25.5431

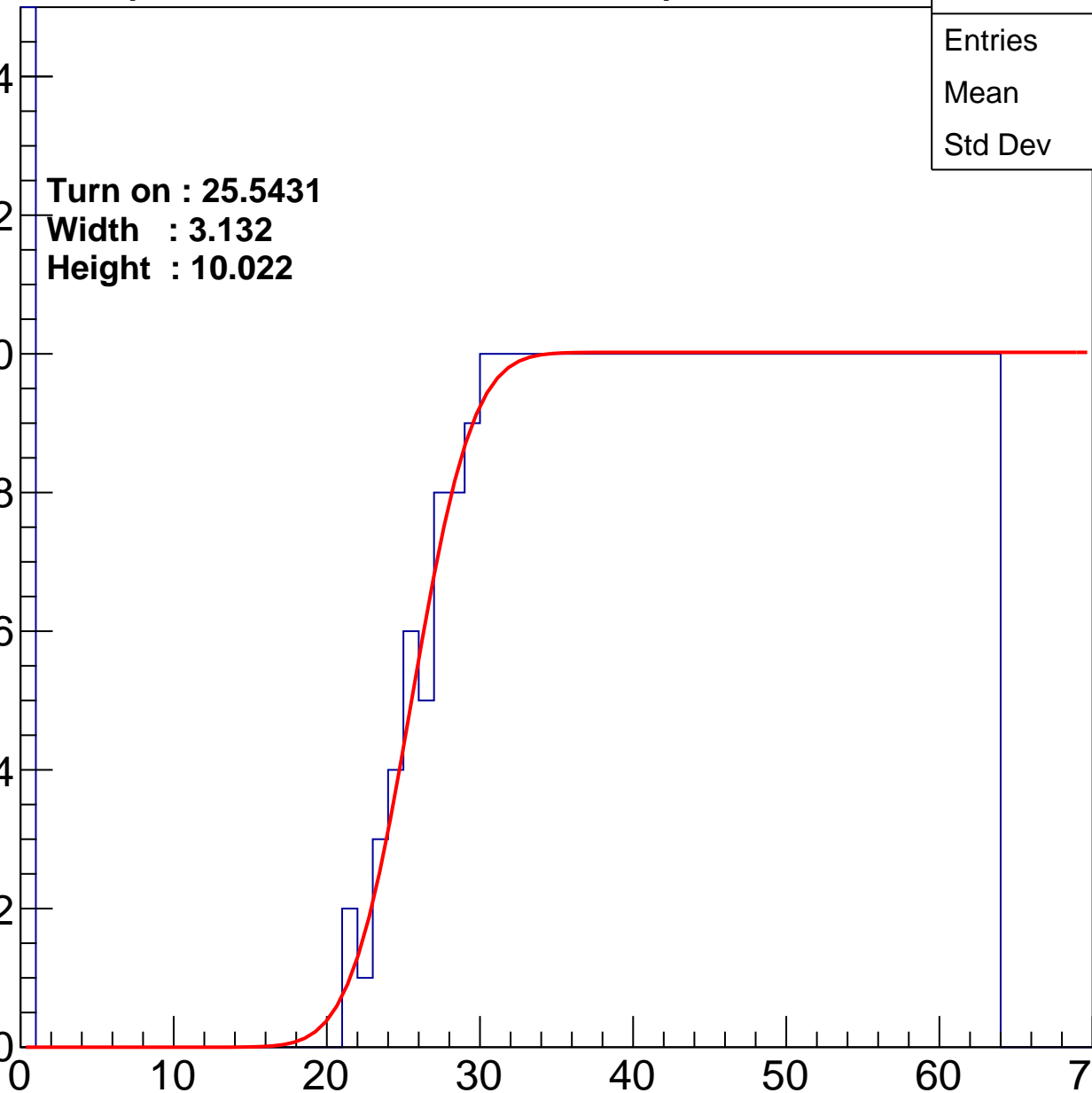
Width : 3.132

Height : 10.022

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch67

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	439
Mean	38.15
Std Dev	18.75

Turn on : 27.1291

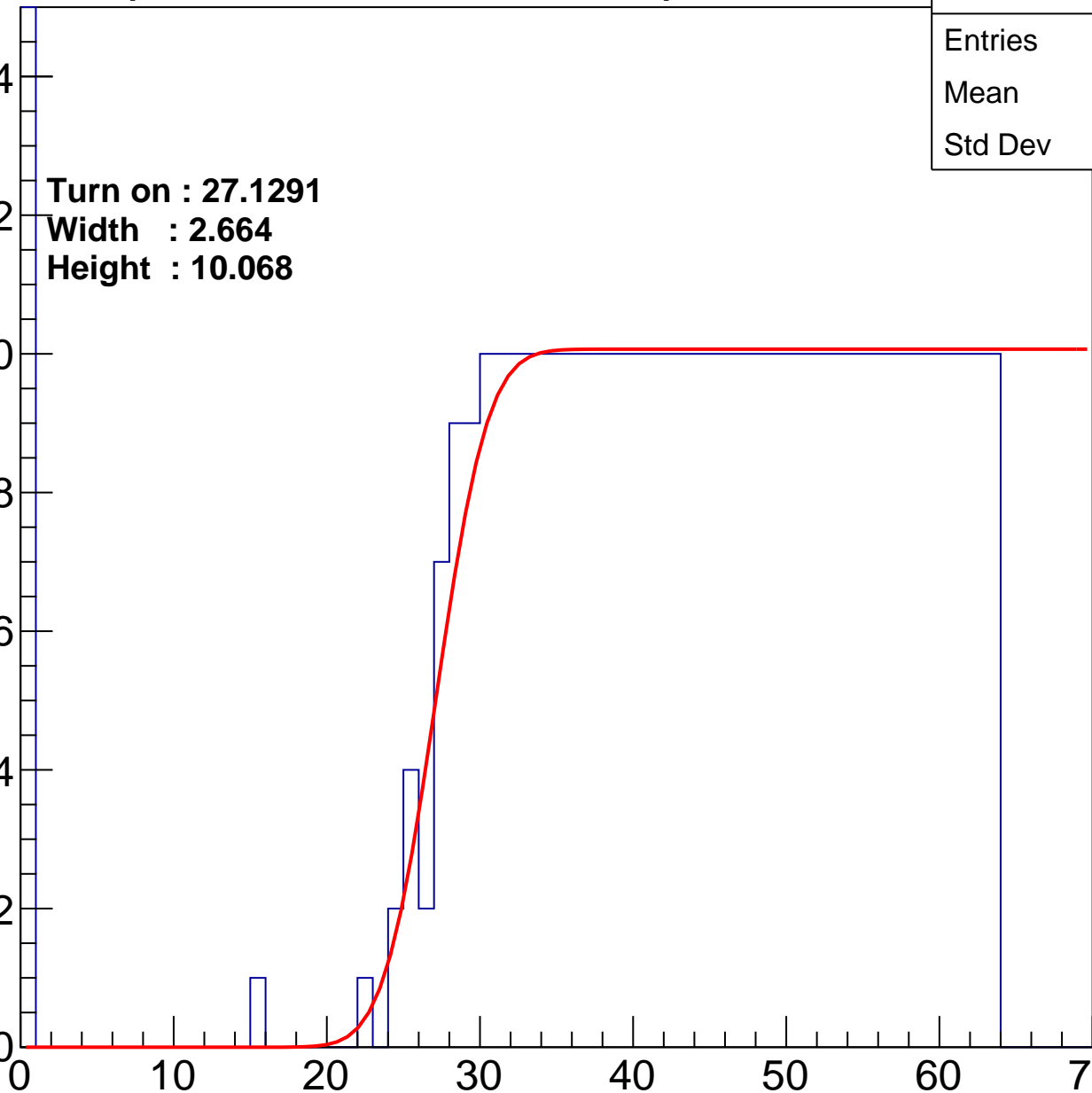
Width : 2.664

Height : 10.068

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch68

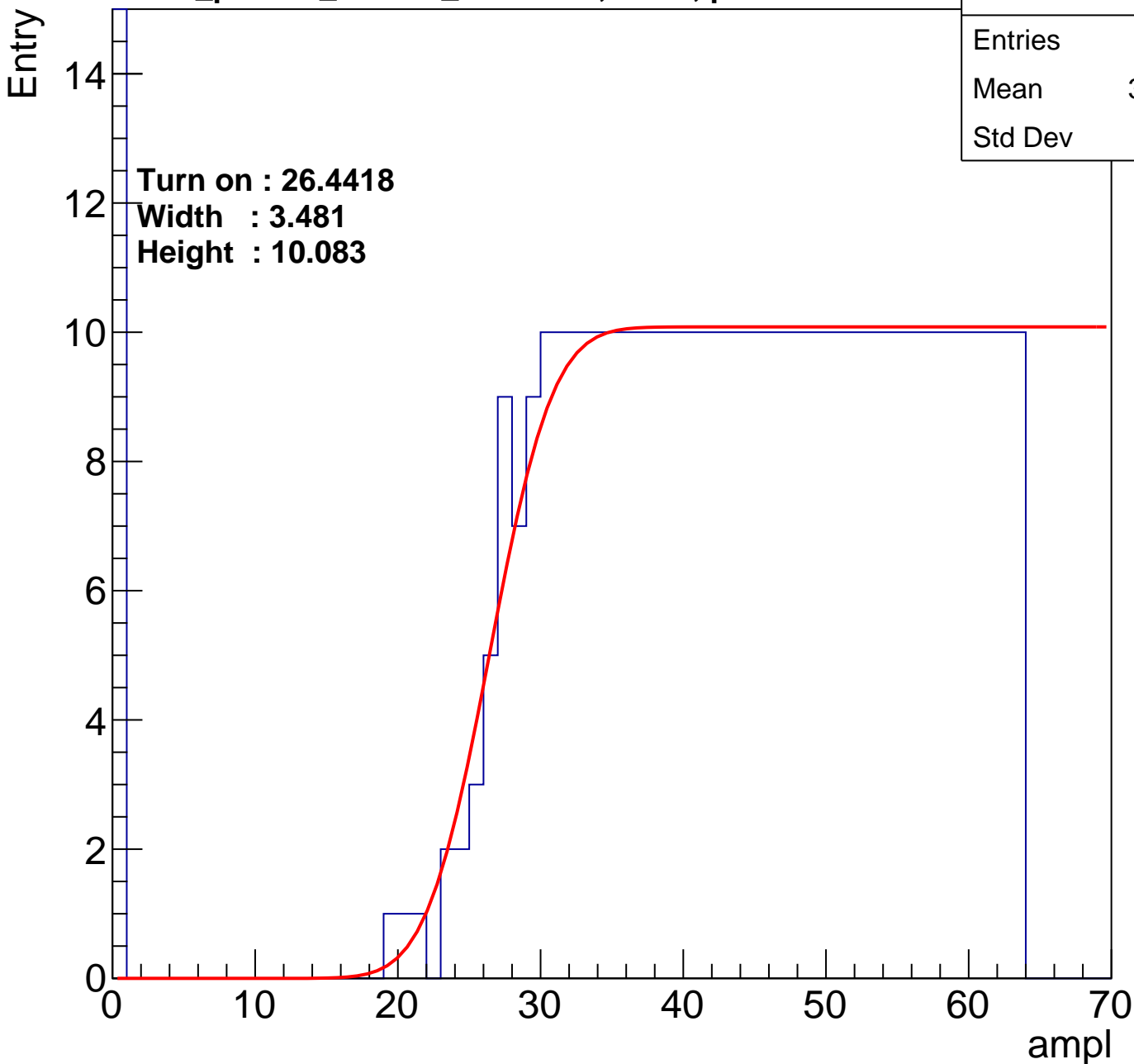
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	429
Mean	39.32
Std Dev	17.6

Turn on : 26.4418

Width : 3.481

Height : 10.083



# B1L103S, U4-ch69

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	446
Mean	37.62
Std Dev	19.11

Turn on : 26.4548

Width : 2.292

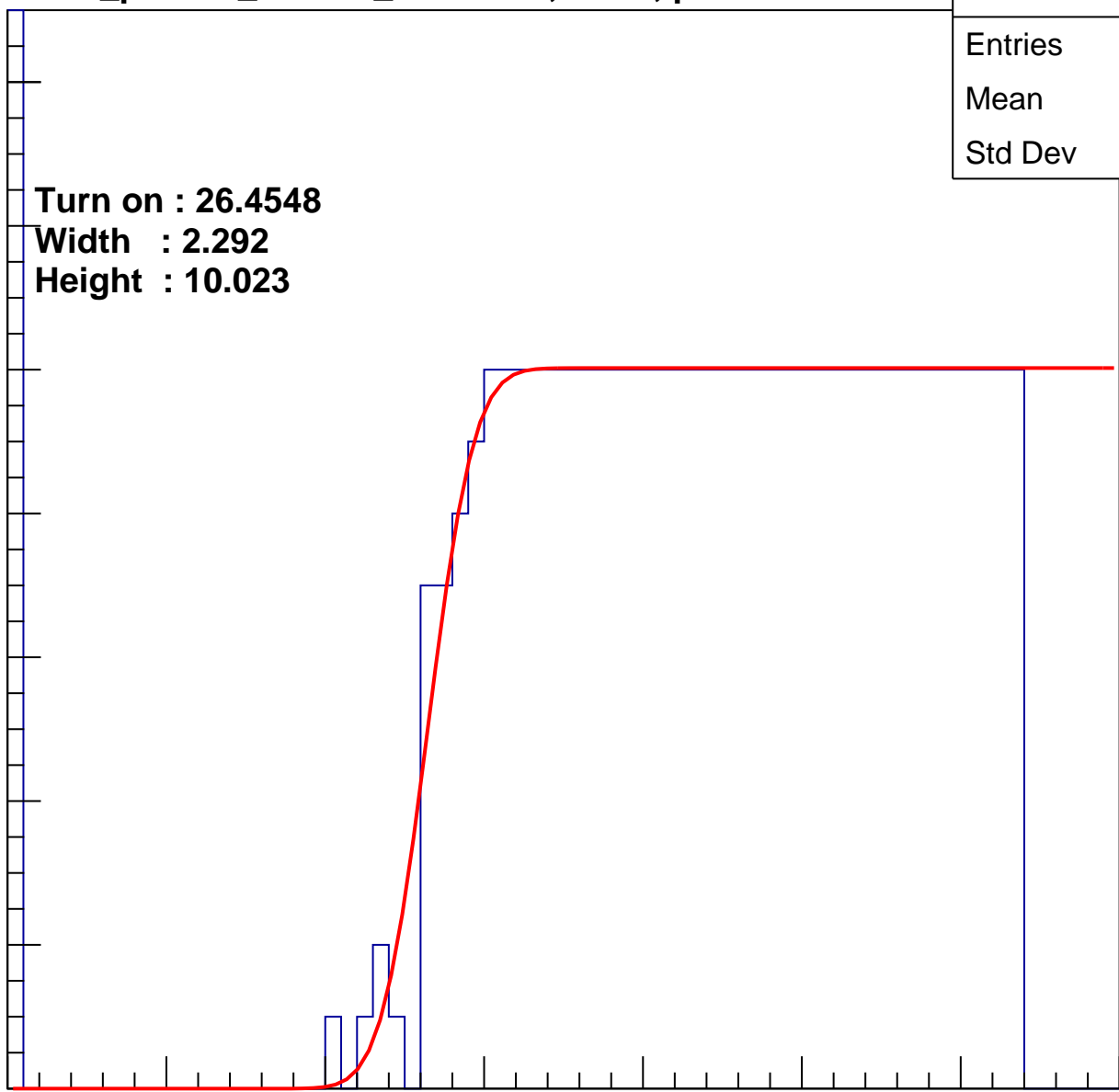
Height : 10.023

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U4-ch70

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	467
Mean	36.33
Std Dev	19.75

Turn on : 25.9109

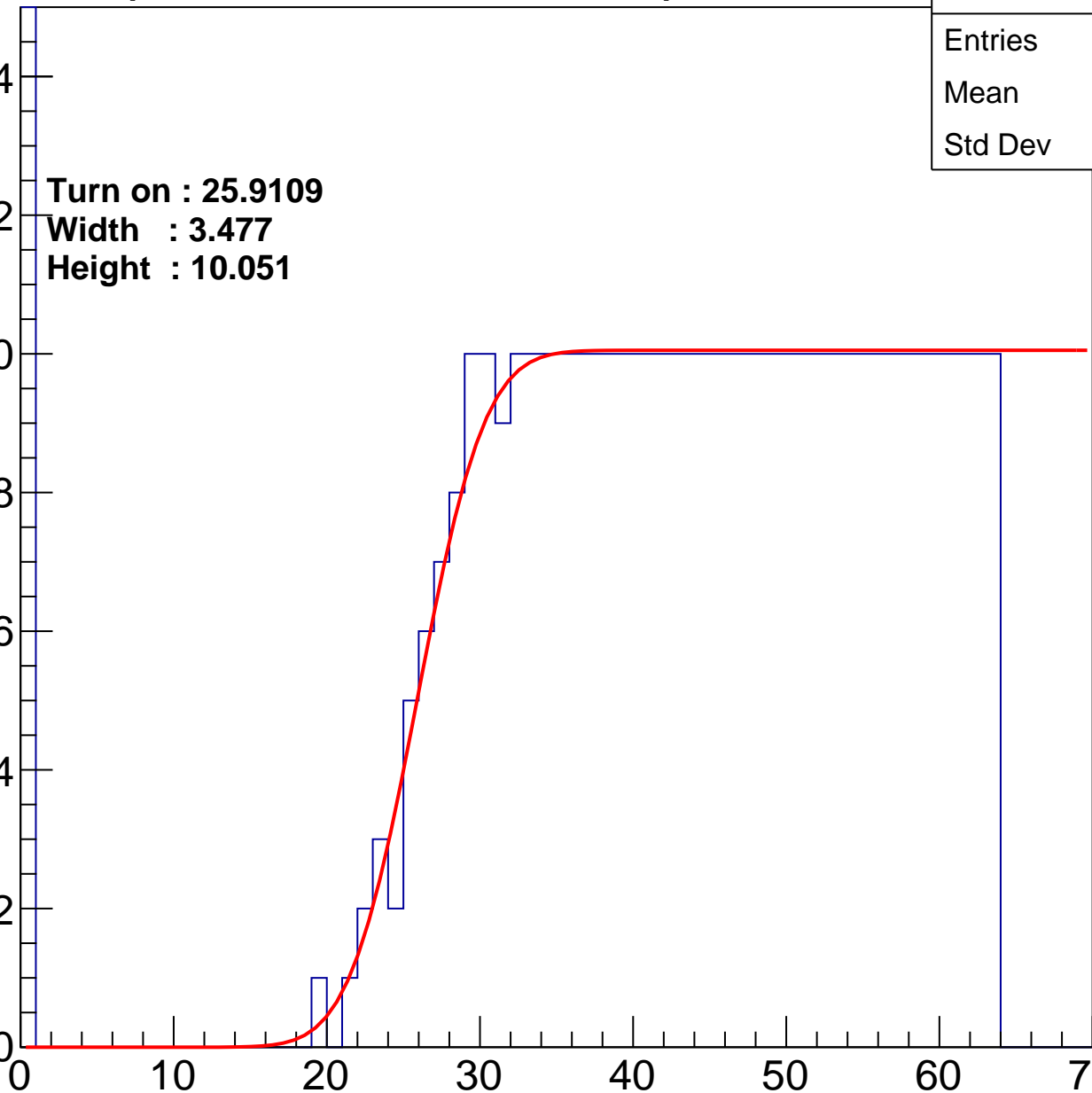
Width : 3.477

Height : 10.051

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L103S, U4-ch71

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	436
Mean	39.01
Std Dev	17.69

Turn on : 25.8665

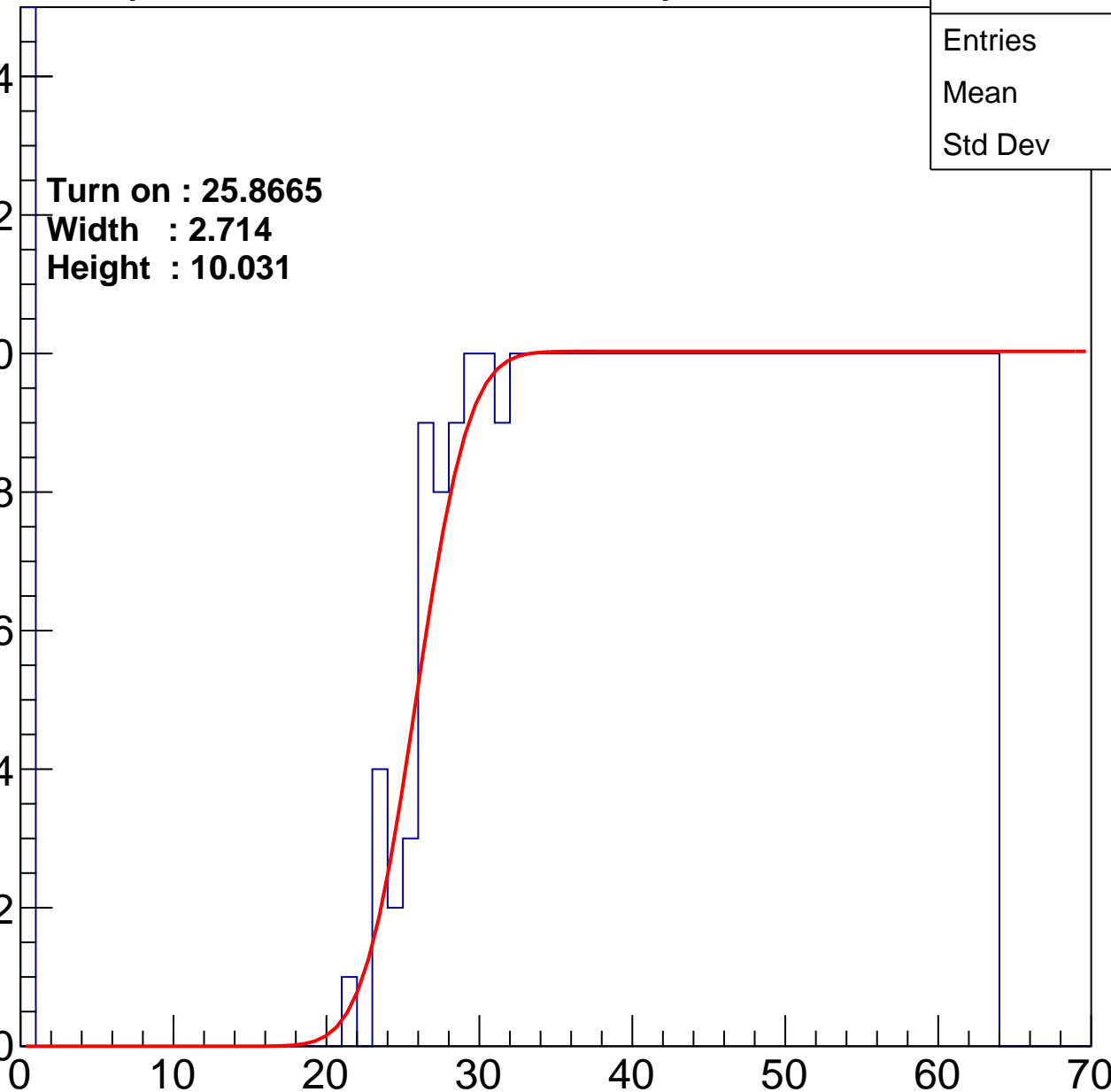
Width : 2.714

Height : 10.031

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch72

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	492
Mean	35.54
Std Dev	19.6

Turn on : 24.7237

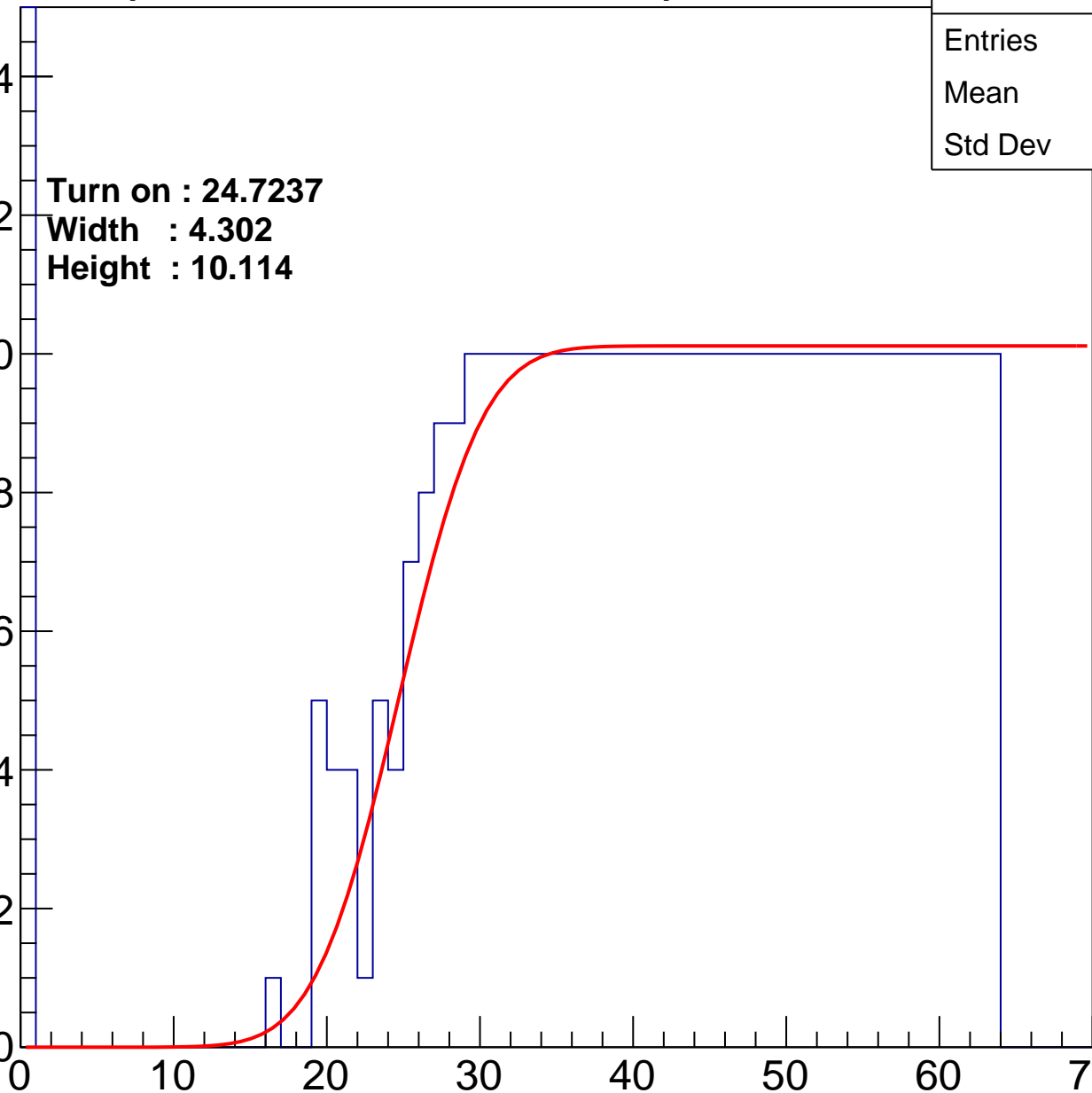
Width : 4.302

Height : 10.114

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch73

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	430
Mean	39.23
Std Dev	17.67

Turn on : 26.3686

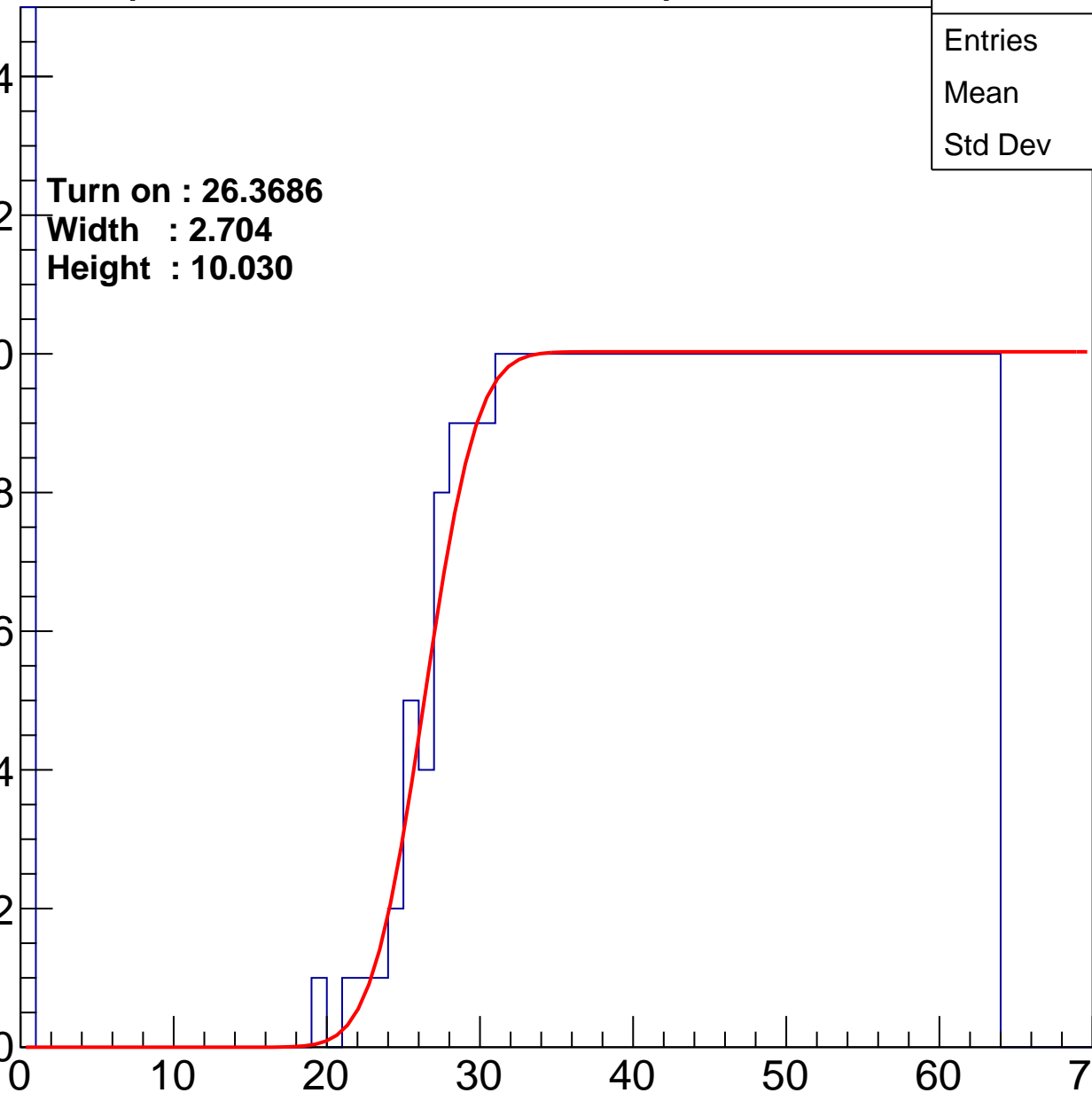
Width : 2.704

Height : 10.030

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch74

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	455
Mean	37.75
Std Dev	18.49

Turn on : 25.0080

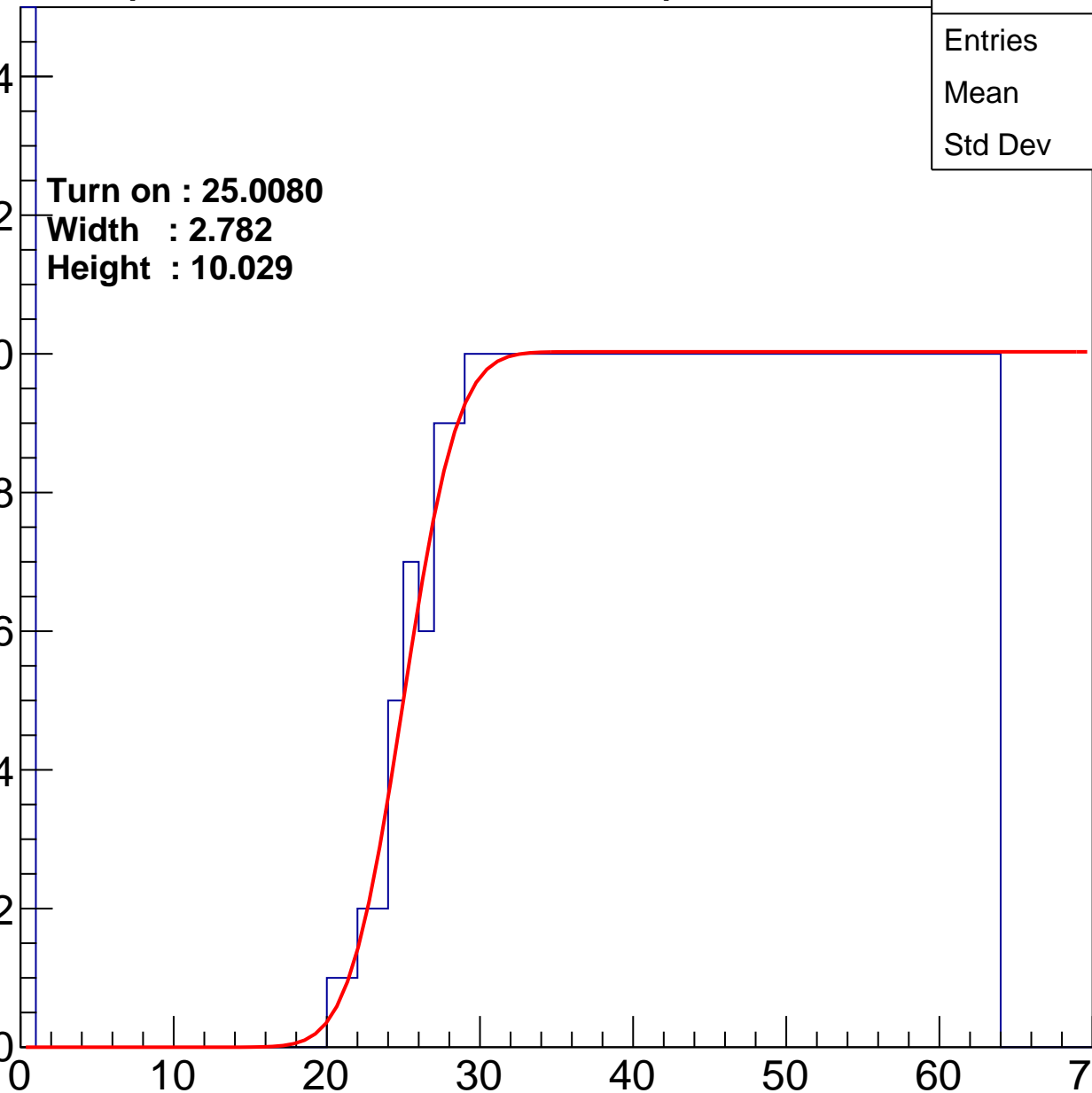
Width : 2.782

Height : 10.029

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch75

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	463
Mean	36.86
Std Dev	19.27

Turn on : 25.0555

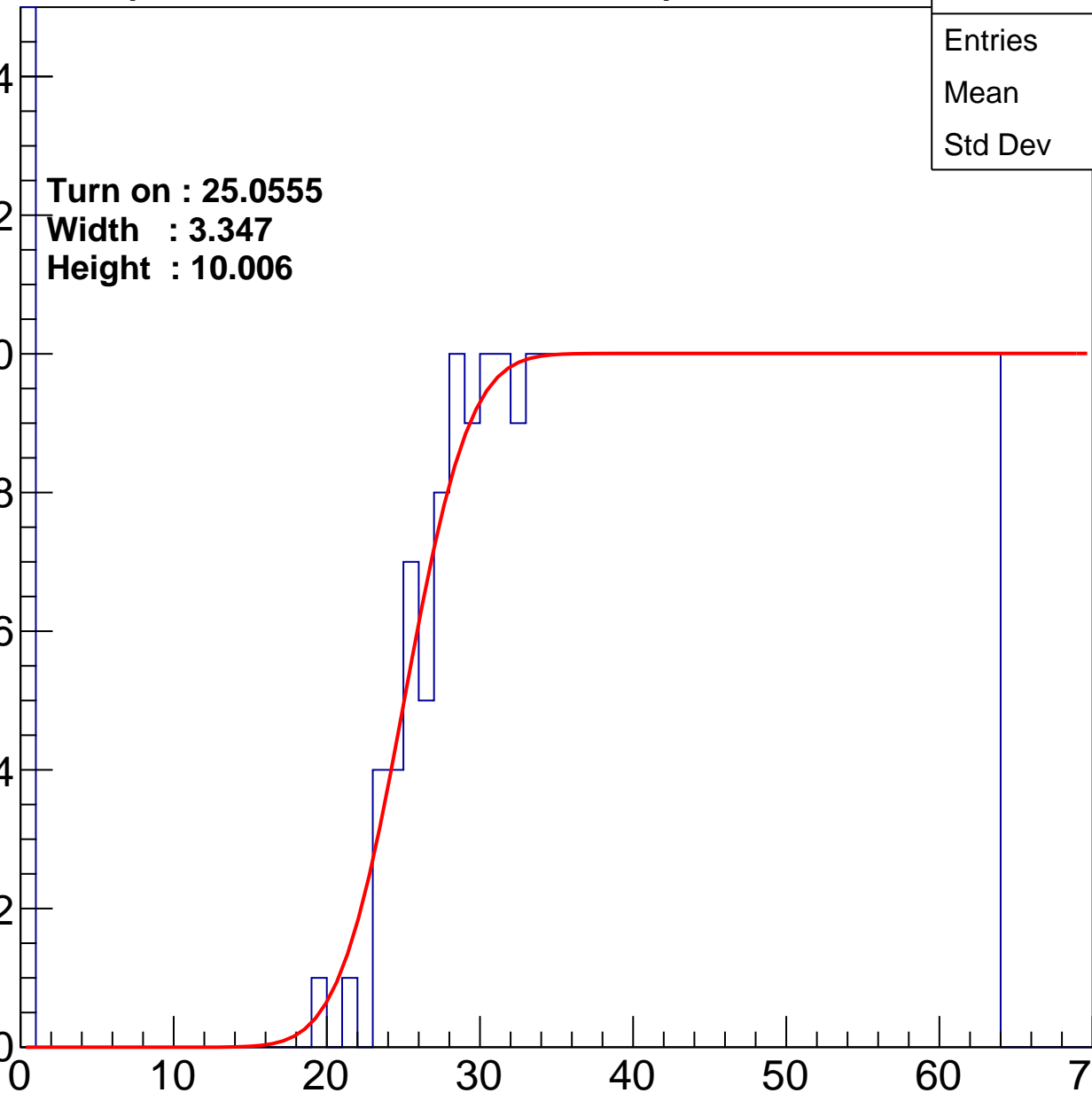
Width : 3.347

Height : 10.006

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch76

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	449
Mean	38.06
Std Dev	18.34

Turn on : 25.4776

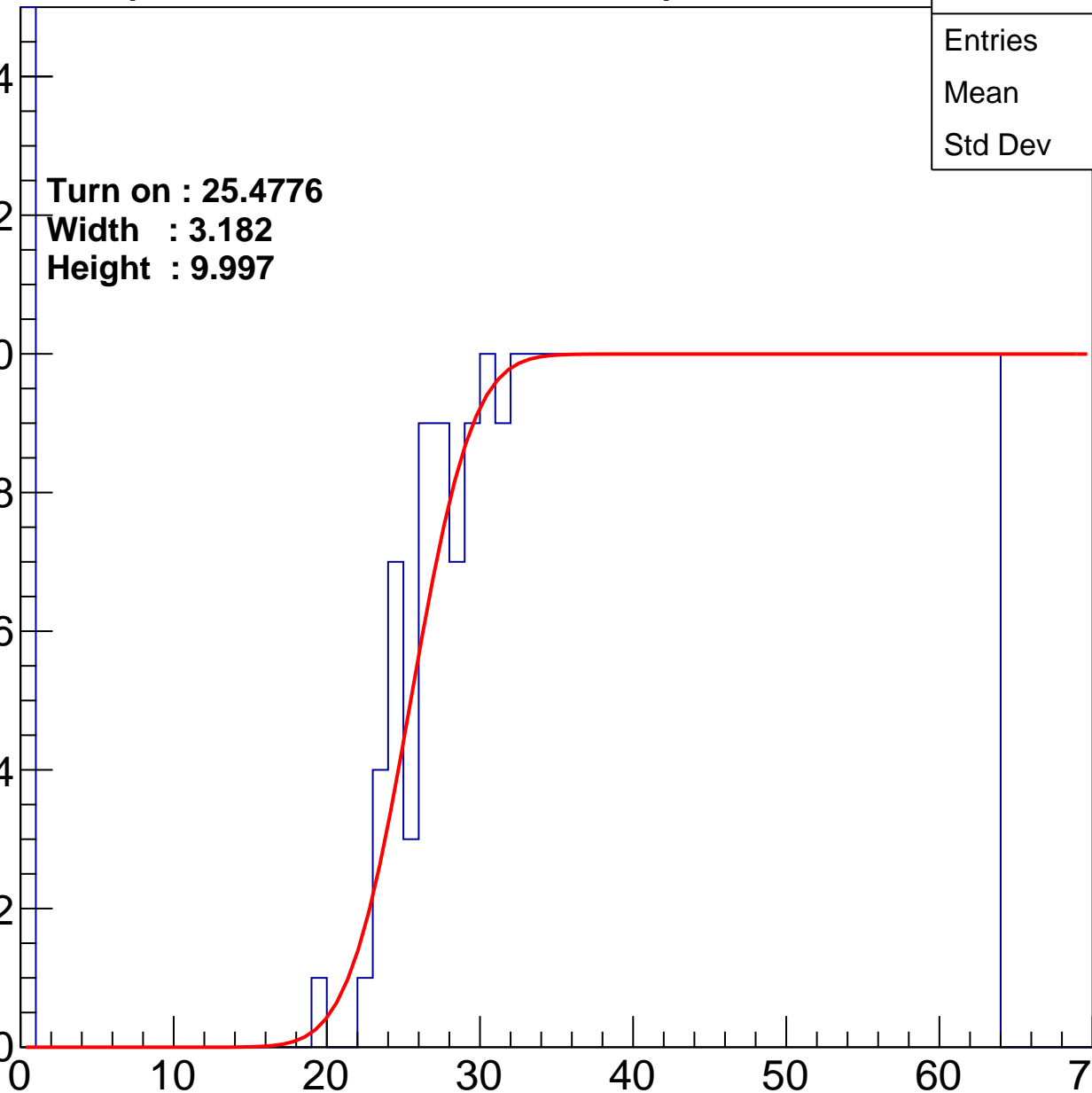
Width : 3.182

Height : 9.997

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch77

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	430
Mean	39.79
Std Dev	16.78

**Turn on : 25.0703**

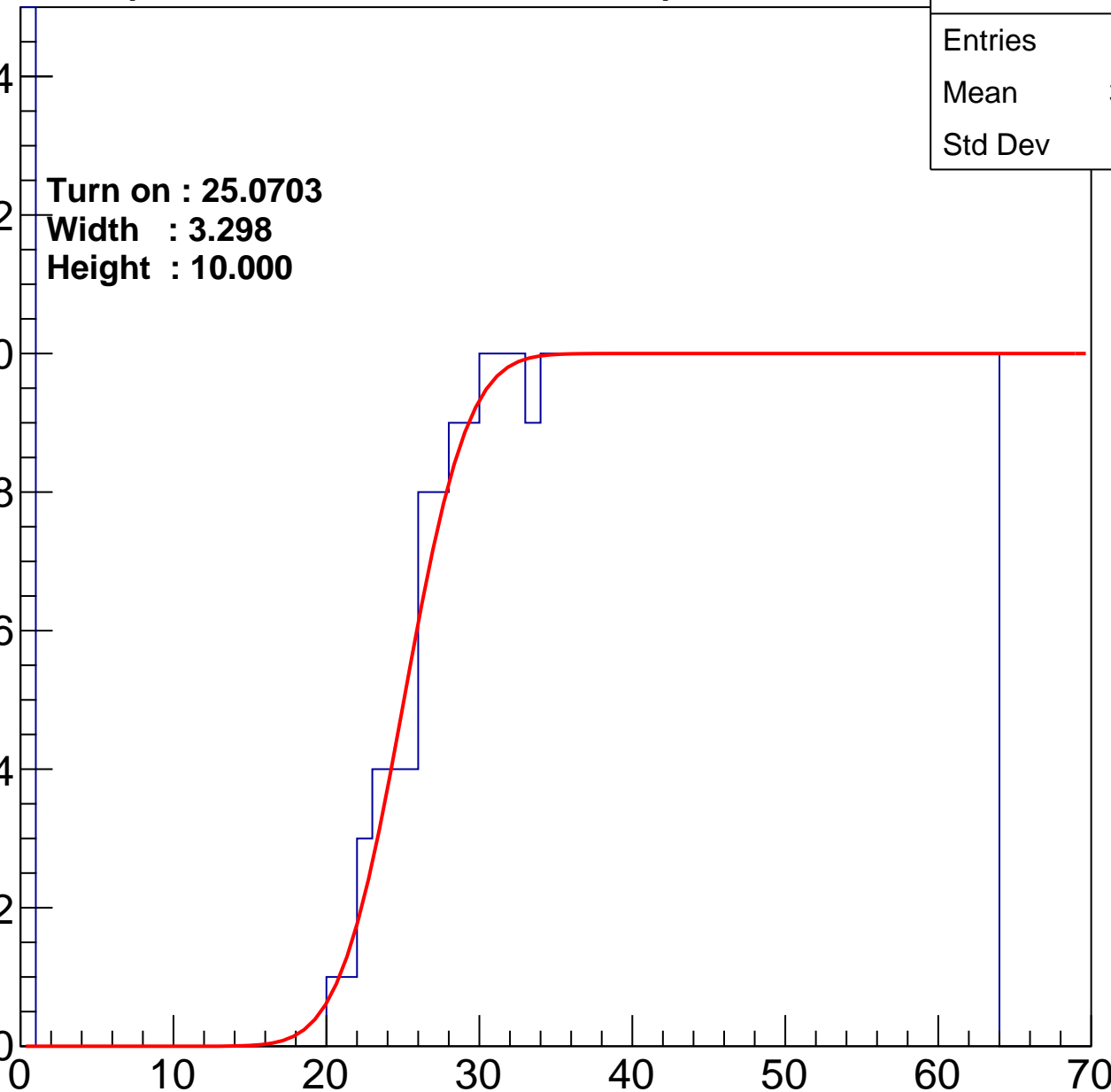
**Width : 3.298**

**Height : 10.000**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch78

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	434
Mean	38.85
Std Dev	18

Turn on : 26.1891

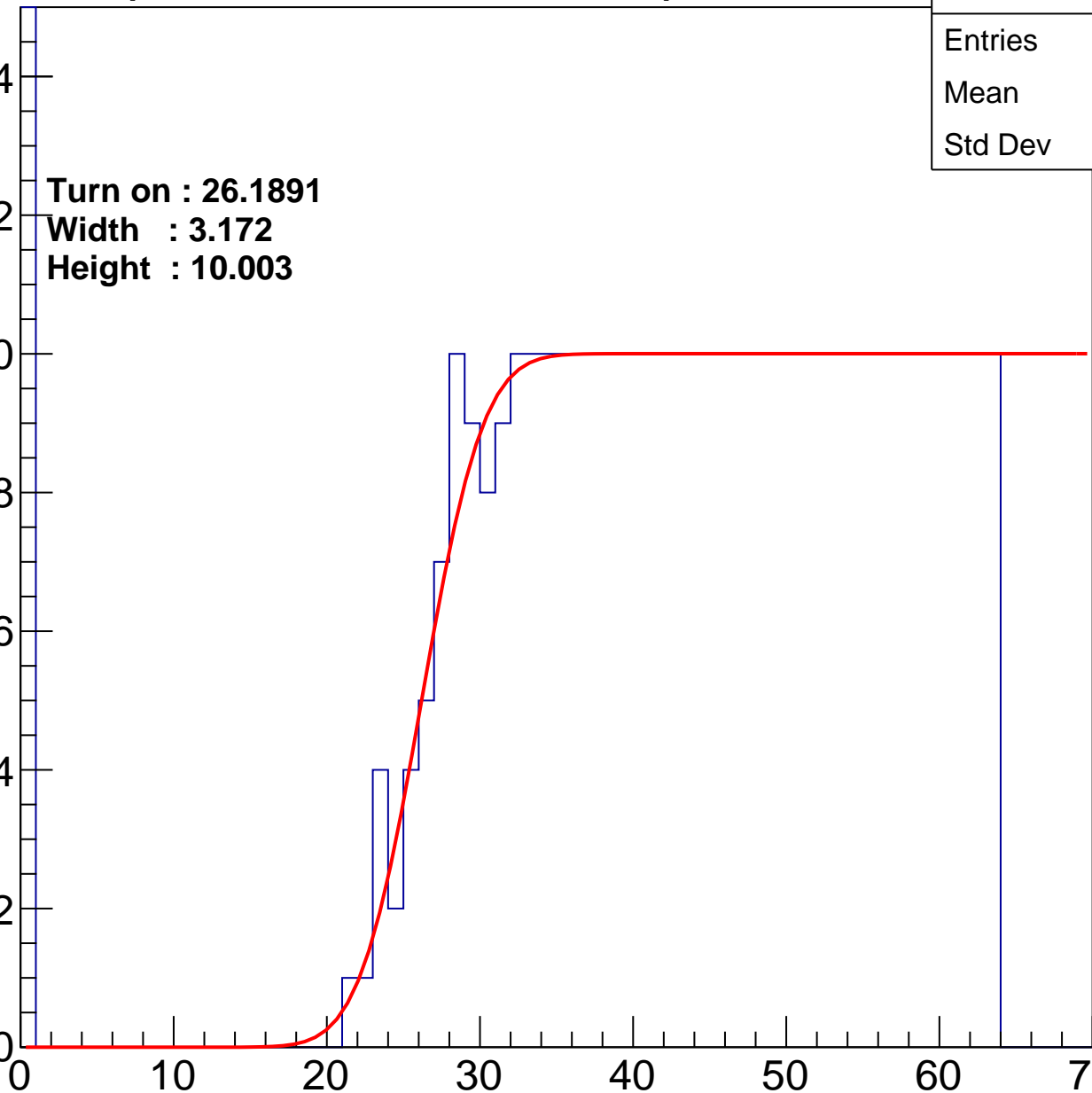
Width : 3.172

Height : 10.003

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L103S, U4-ch79

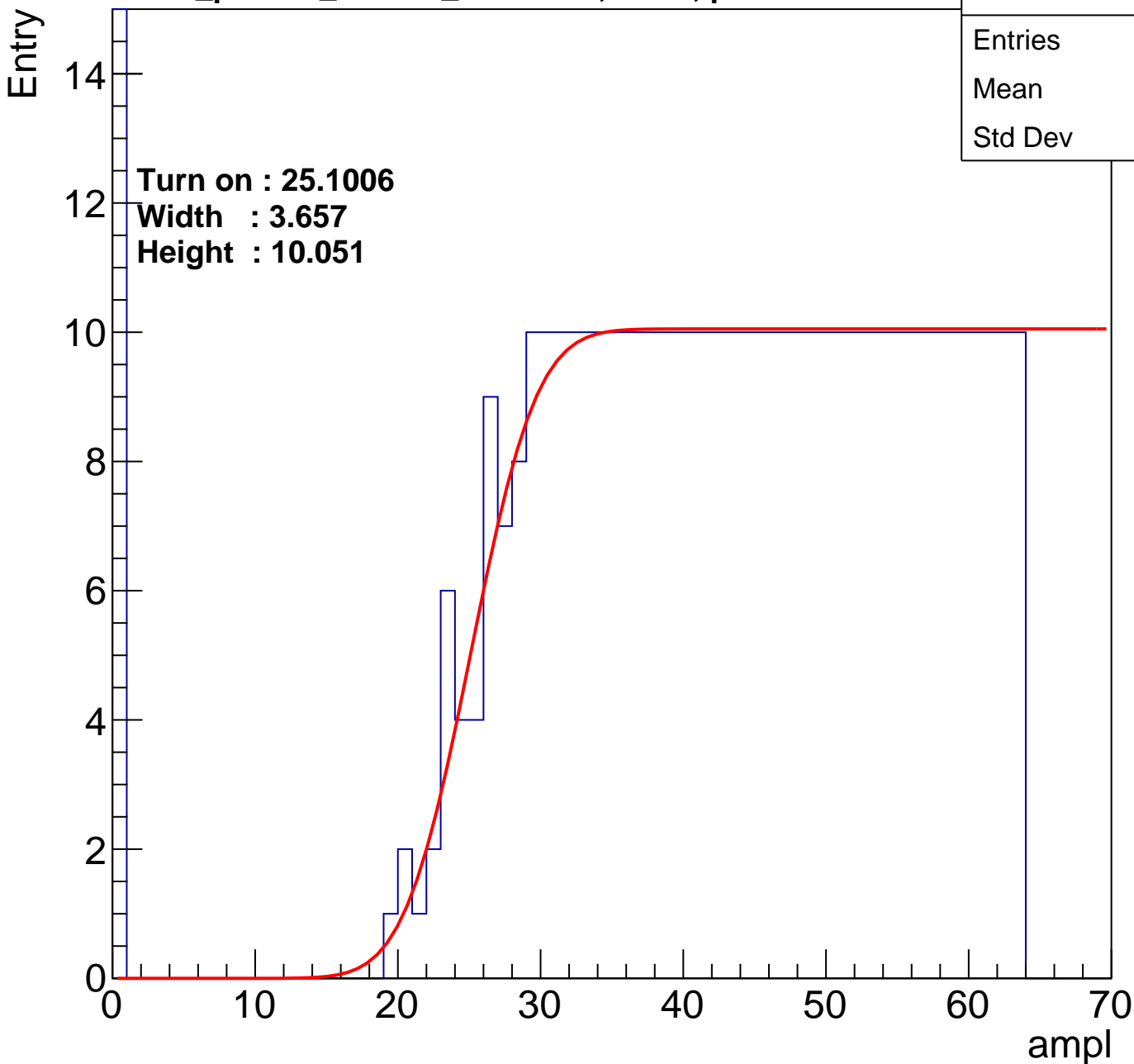
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	460
Mean	37.4
Std Dev	18.7

Turn on : 25.1006

Width : 3.657

Height : 10.051



# B1L103S, U4-ch80

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	459
Mean	37.97
Std Dev	17.97

Turn on : 24.4206

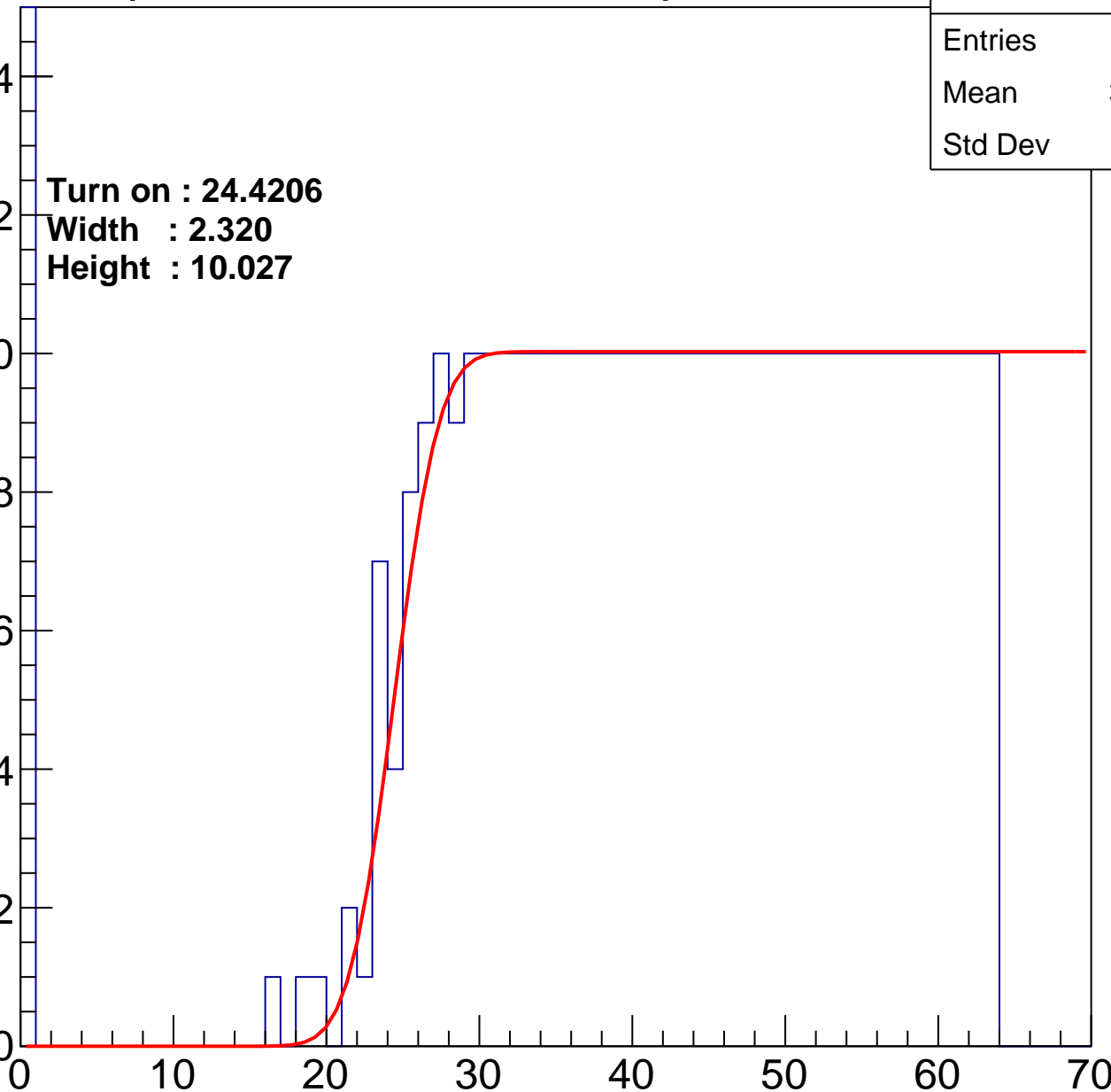
Width : 2.320

Height : 10.027

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch81

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	436
Mean	38.71
Std Dev	18.12

Turn on : 26.1763

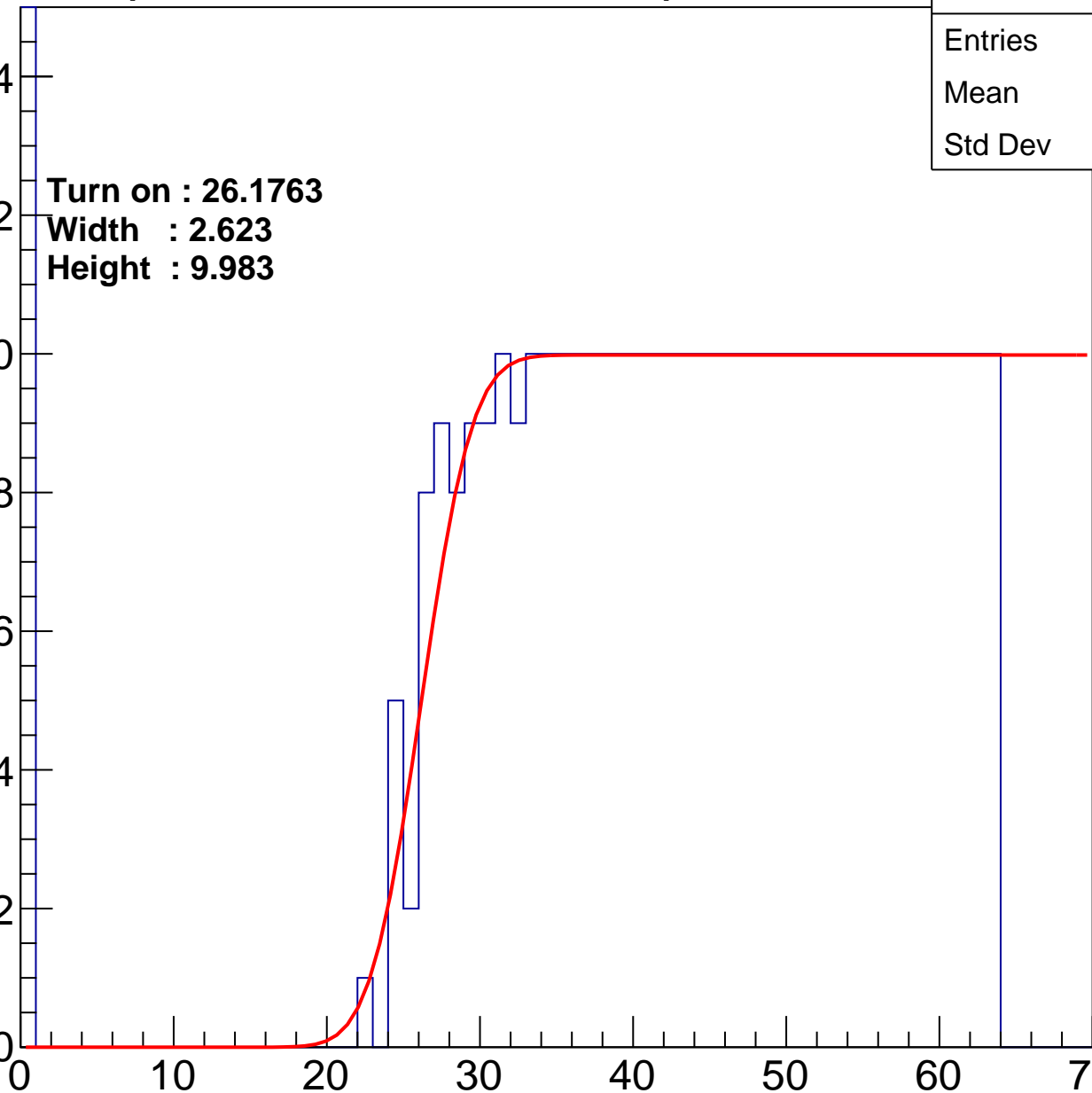
Width : 2.623

Height : 9.983

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch82

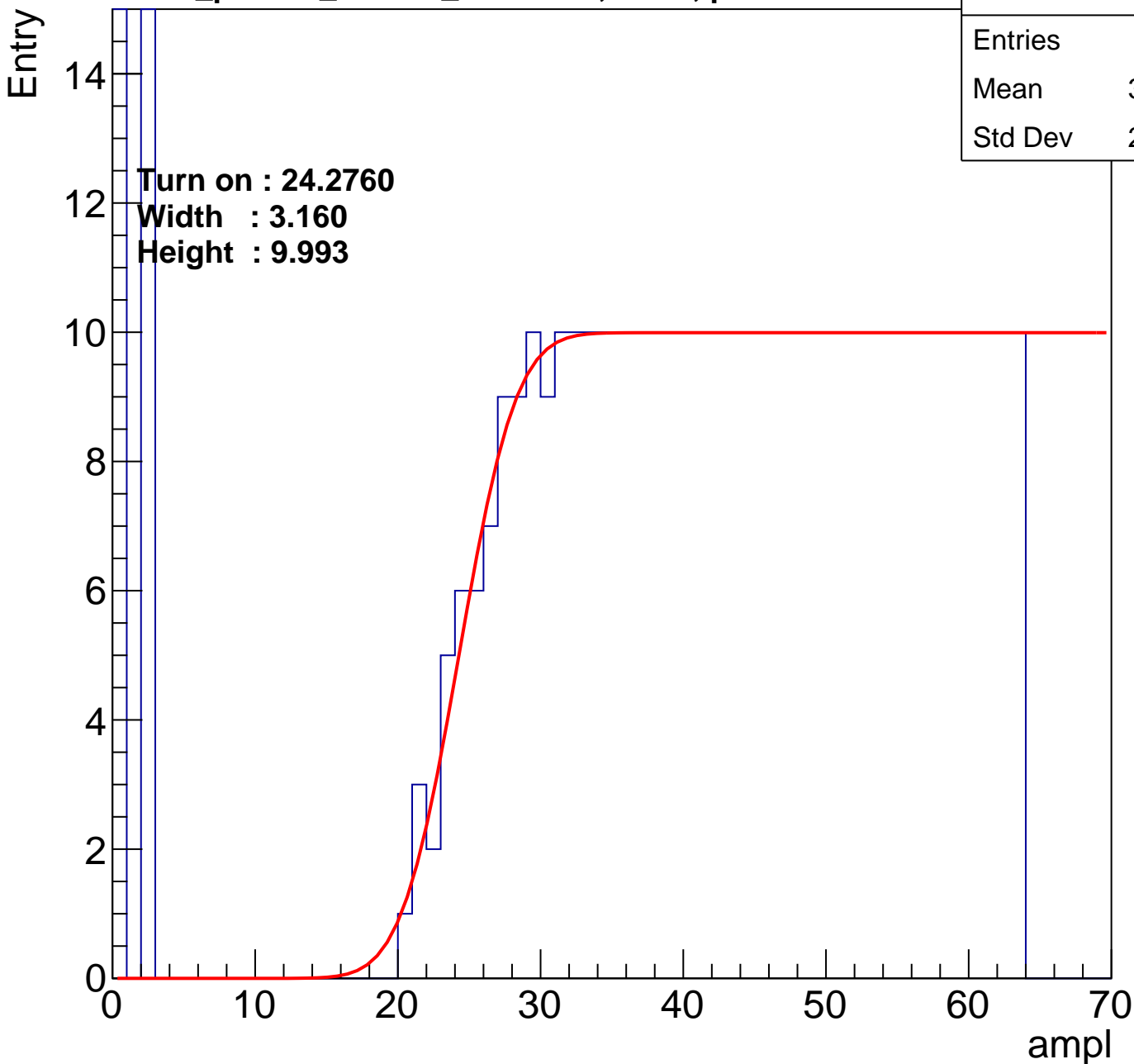
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	537
Mean	32.47
Std Dev	21.16

Turn on : 24.2760

Width : 3.160

Height : 9.993



# B1L103S, U4-ch83

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	414
Mean	39.53
Std Dev	18.11

Turn on : 27.9293

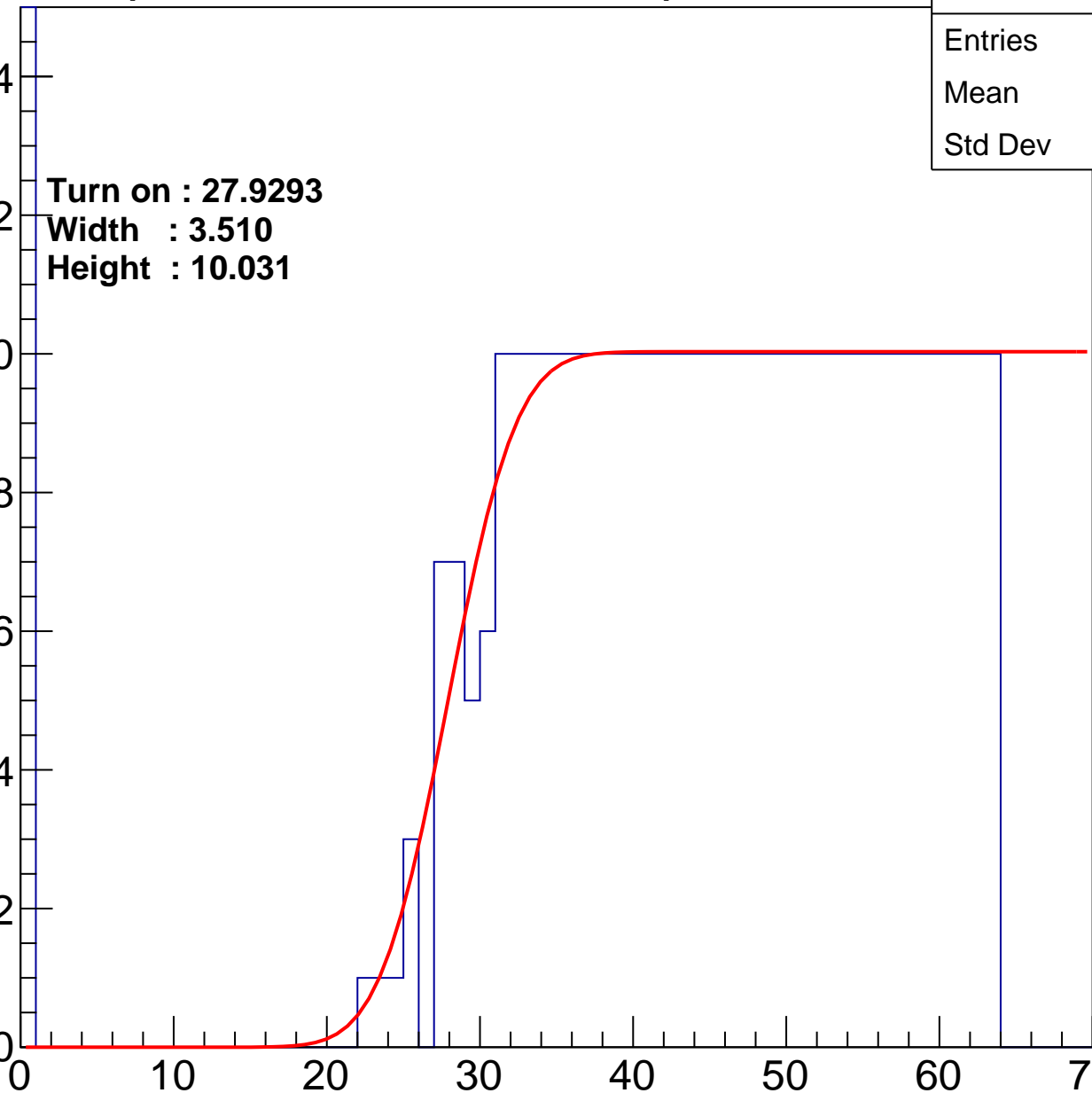
Width : 3.510

Height : 10.031

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch84

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	434
Mean	38.96
Std Dev	17.88

Turn on : 26.4430

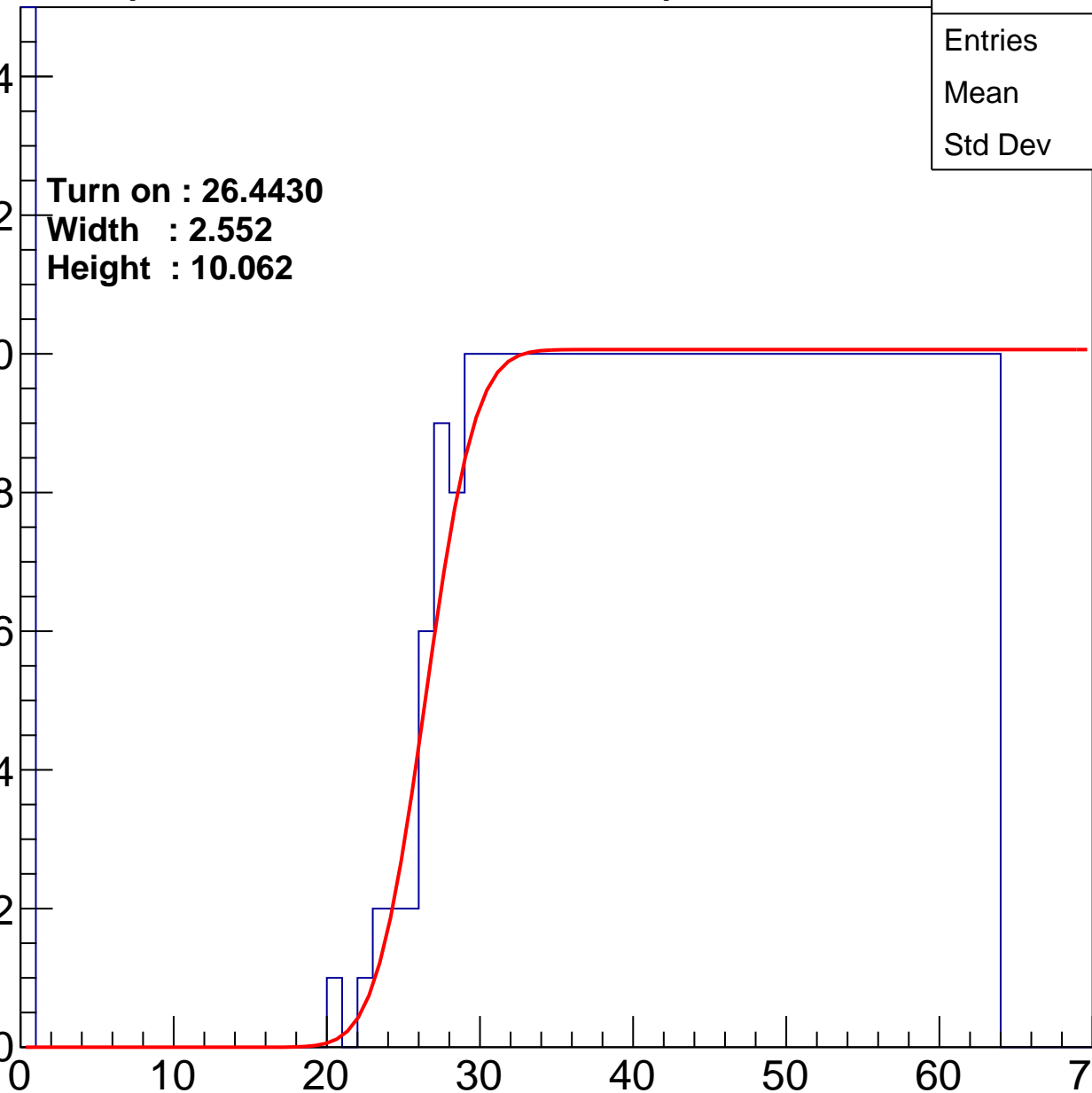
Width : 2.552

Height : 10.062

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch85

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	443
Mean	37.27
Std Dev	19.63

Turn on : 26.9953

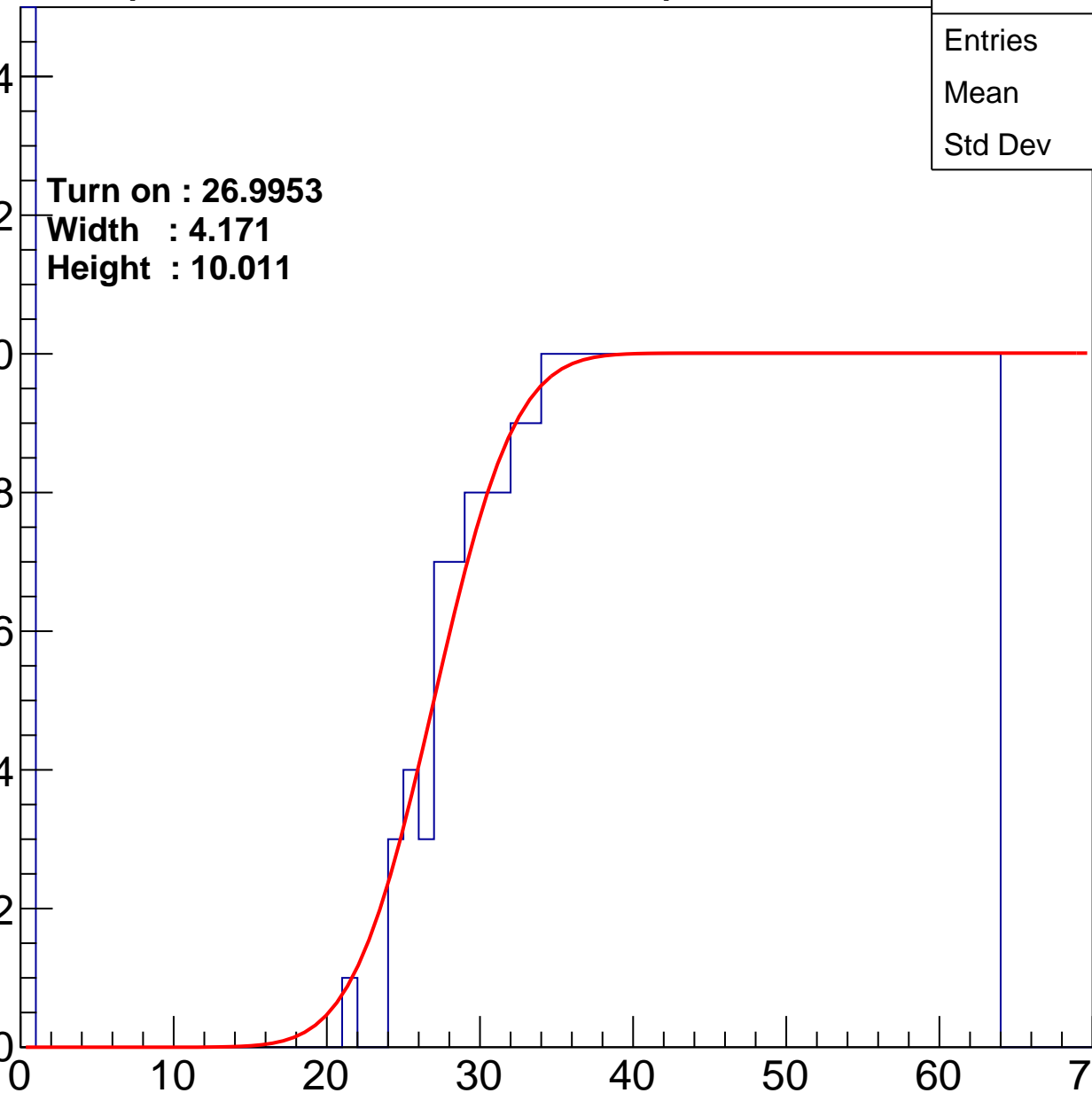
Width : 4.171

Height : 10.011

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch86

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	466
Mean	36.92
Std Dev	19.05

Turn on : 25.1484

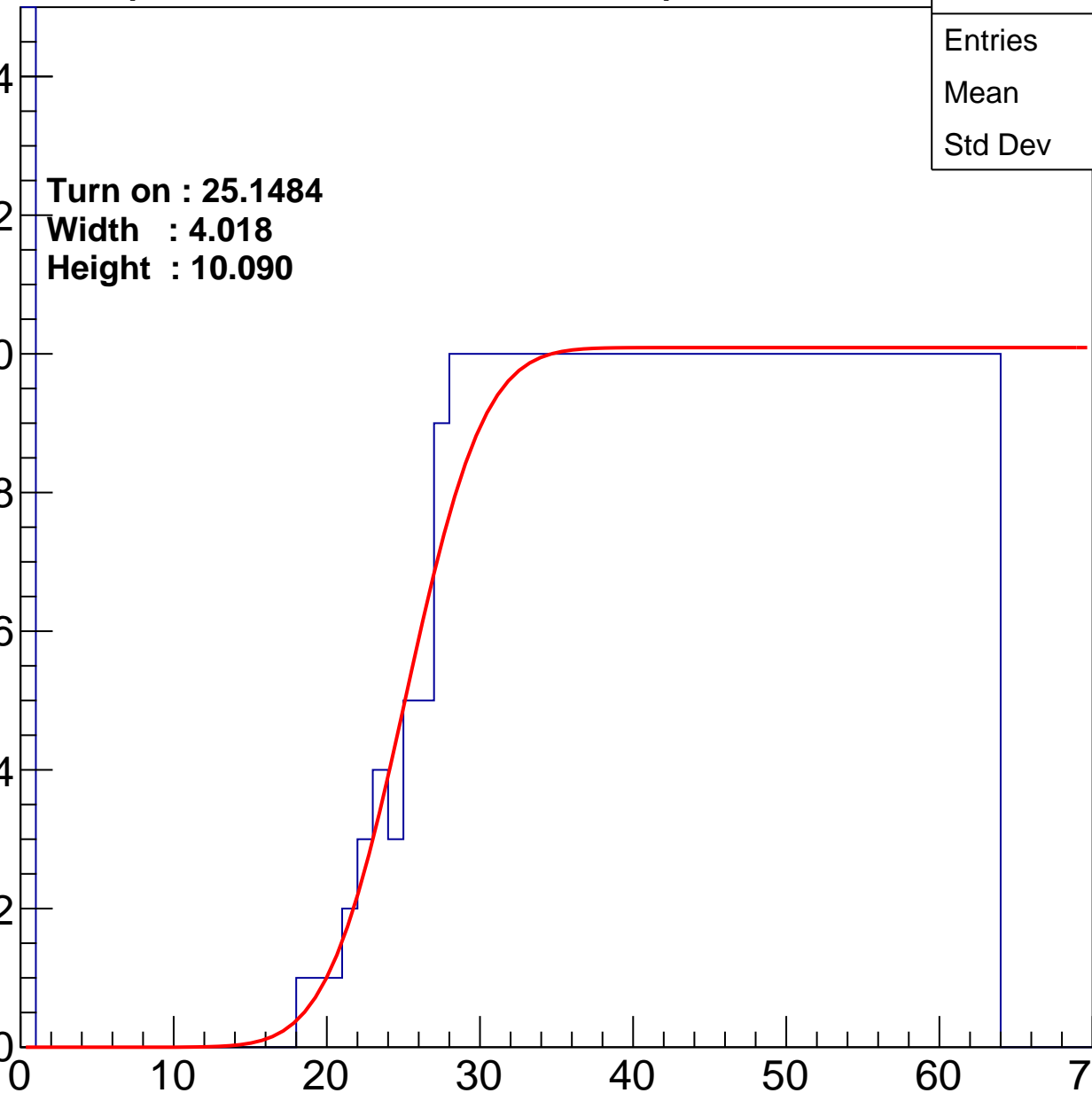
Width : 4.018

Height : 10.090

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L103S, U4-ch87

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	456
Mean	37.26
Std Dev	19.09

Turn on : 26.0856

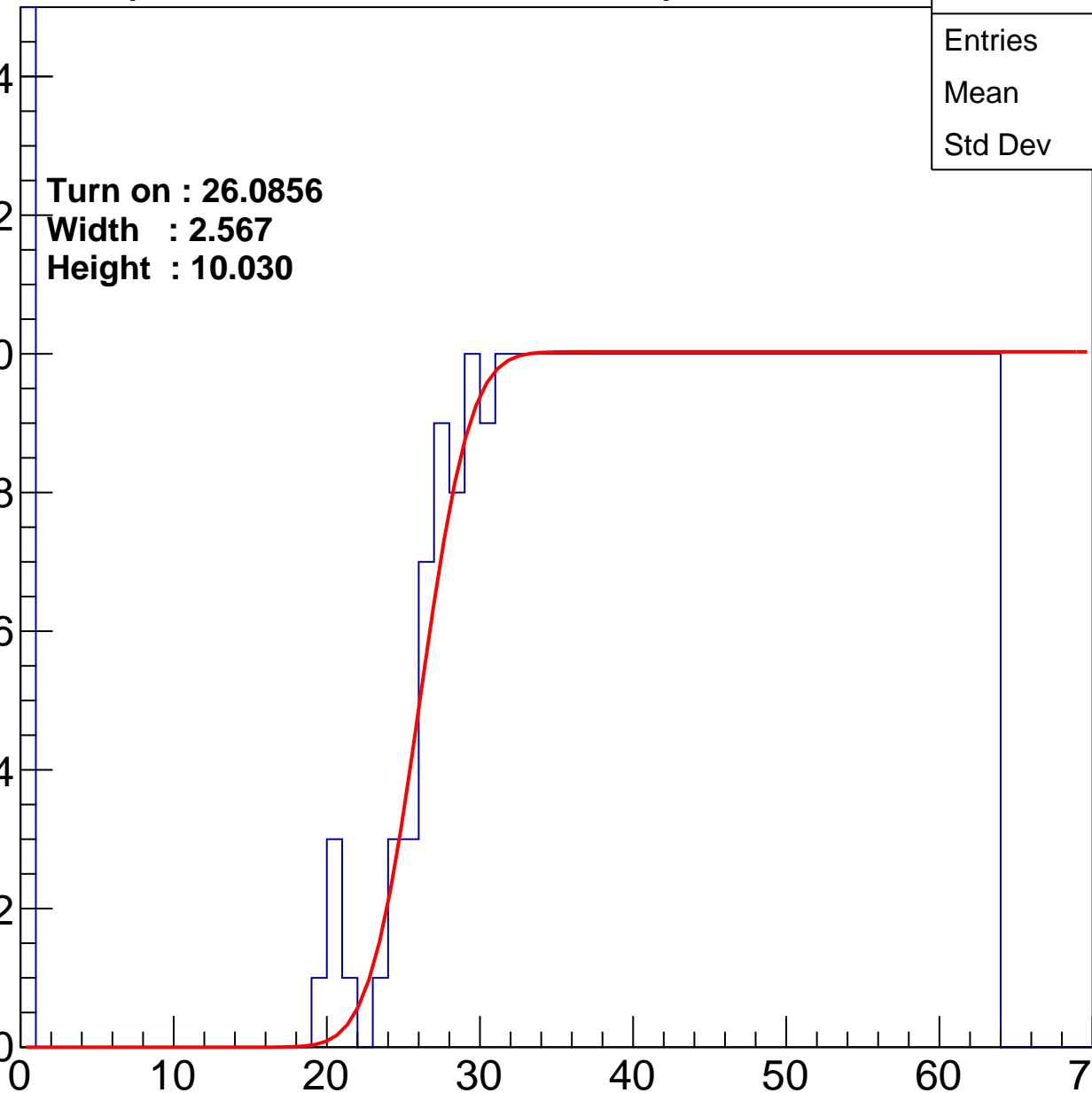
Width : 2.567

Height : 10.030

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch88

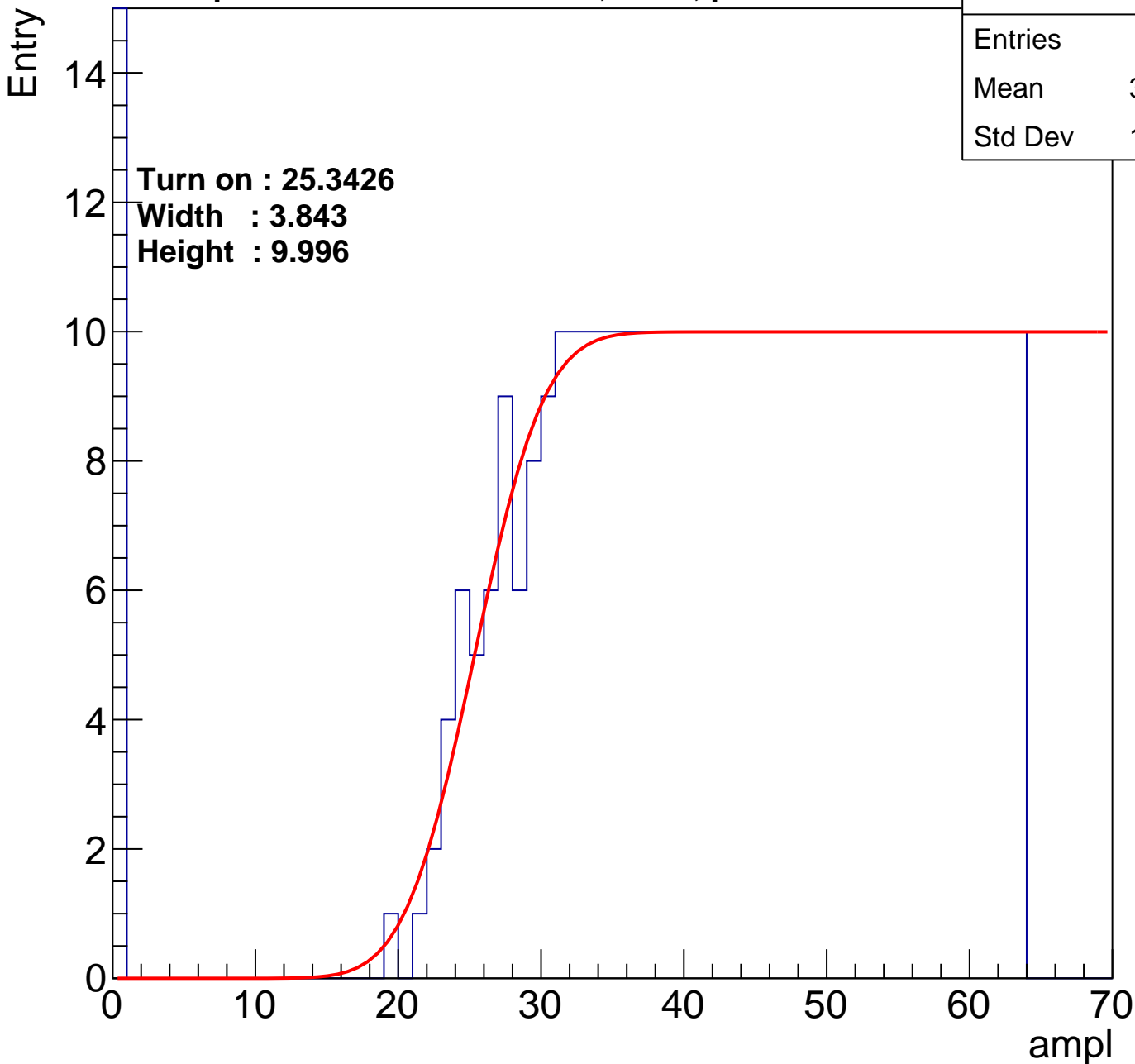
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	459
Mean	37.09
Std Dev	19.14

Turn on : 25.3426

Width : 3.843

Height : 9.996



# B1L103S, U4-ch89

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	434
Mean	39.33
Std Dev	17.3

Turn on : 25.5295

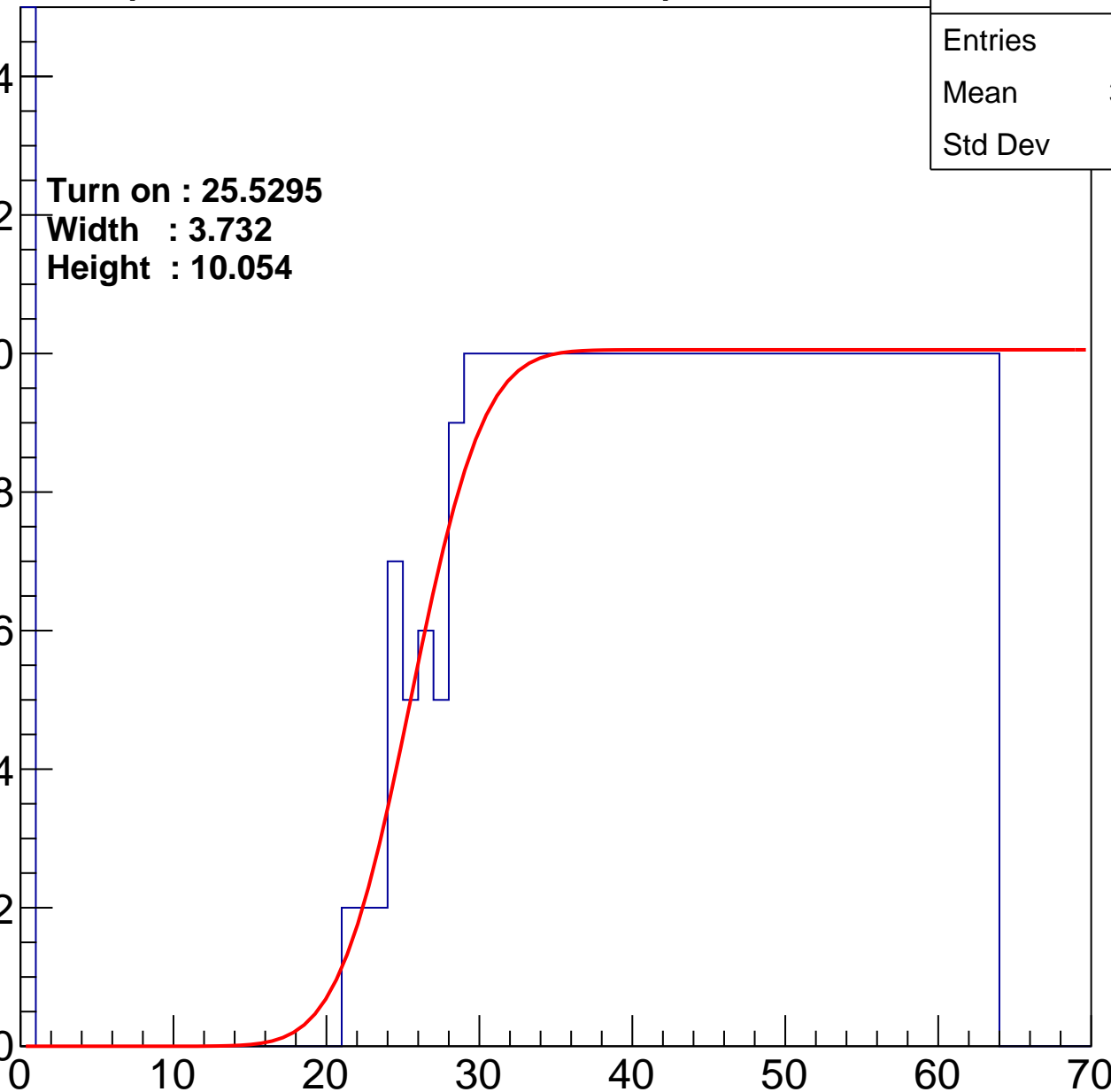
Width : 3.732

Height : 10.054

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch90

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	458
Mean	36.99
Std Dev	19.33

Turn on : 25.3381

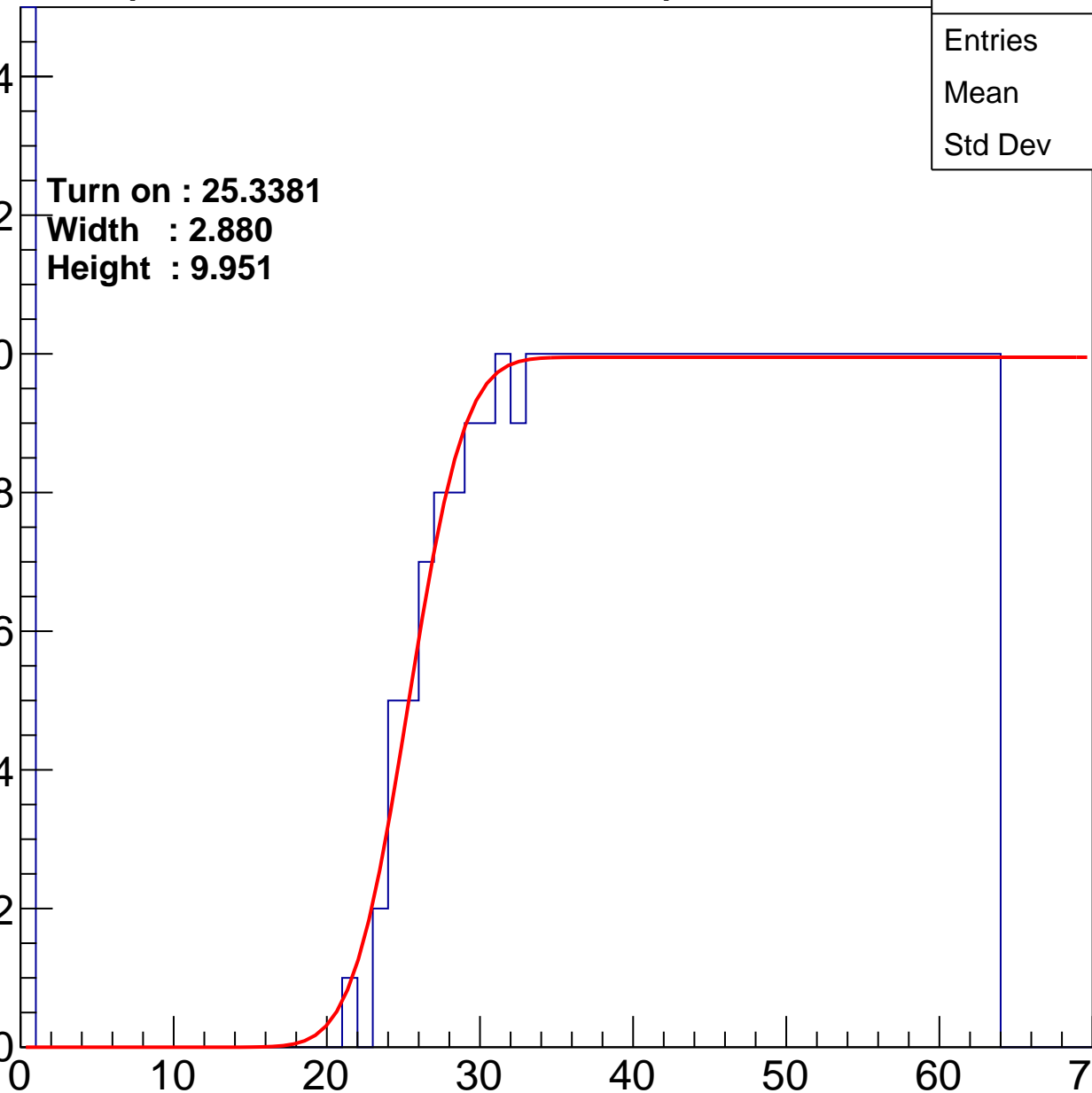
Width : 2.880

Height : 9.951

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch91

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	457
Mean	36.98
Std Dev	19.4

**Turn on : 25.7883**

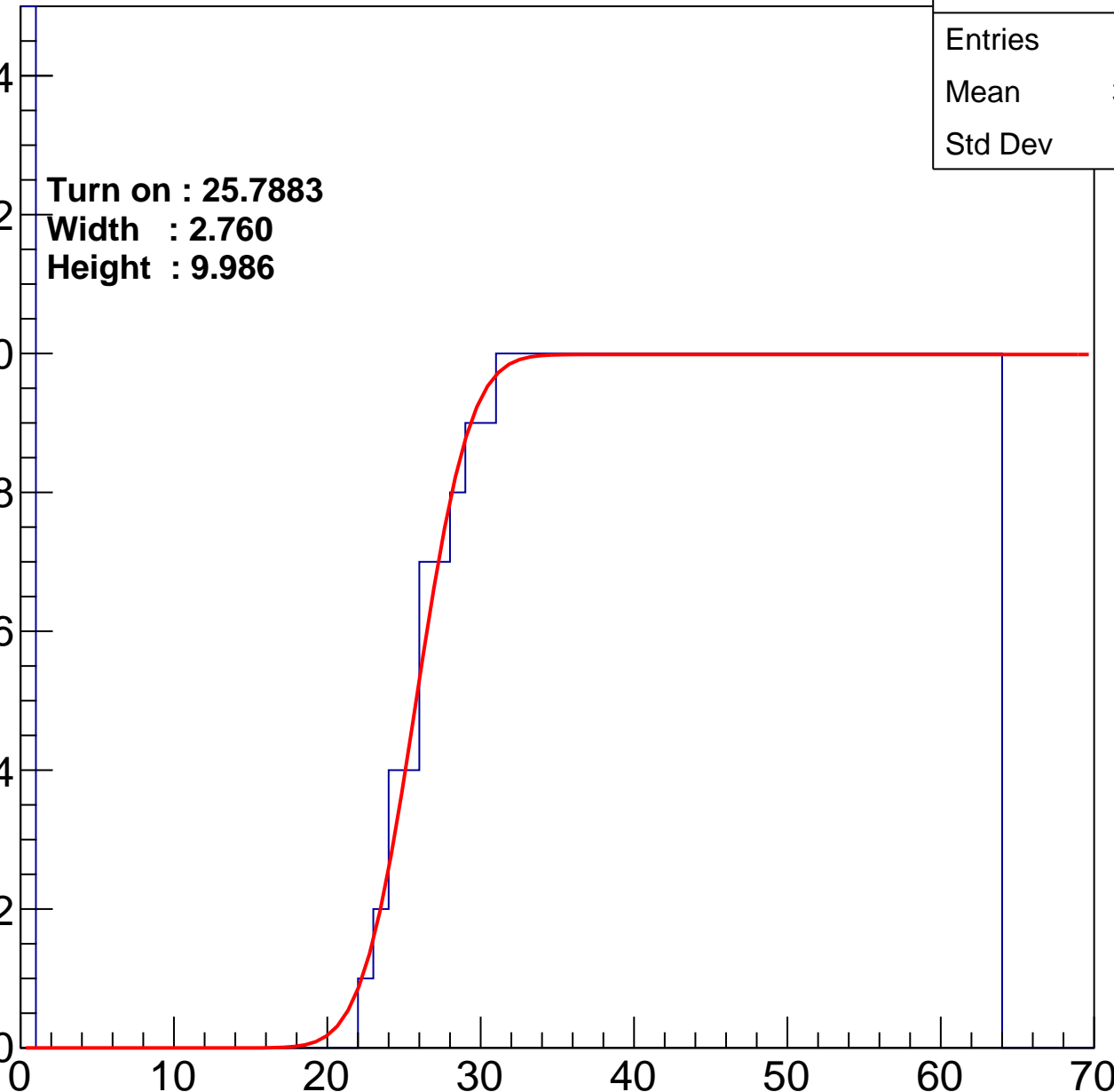
**Width : 2.760**

**Height : 9.986**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch92

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	435
Mean	39.04
Std Dev	17.66

Turn on : 25.3540

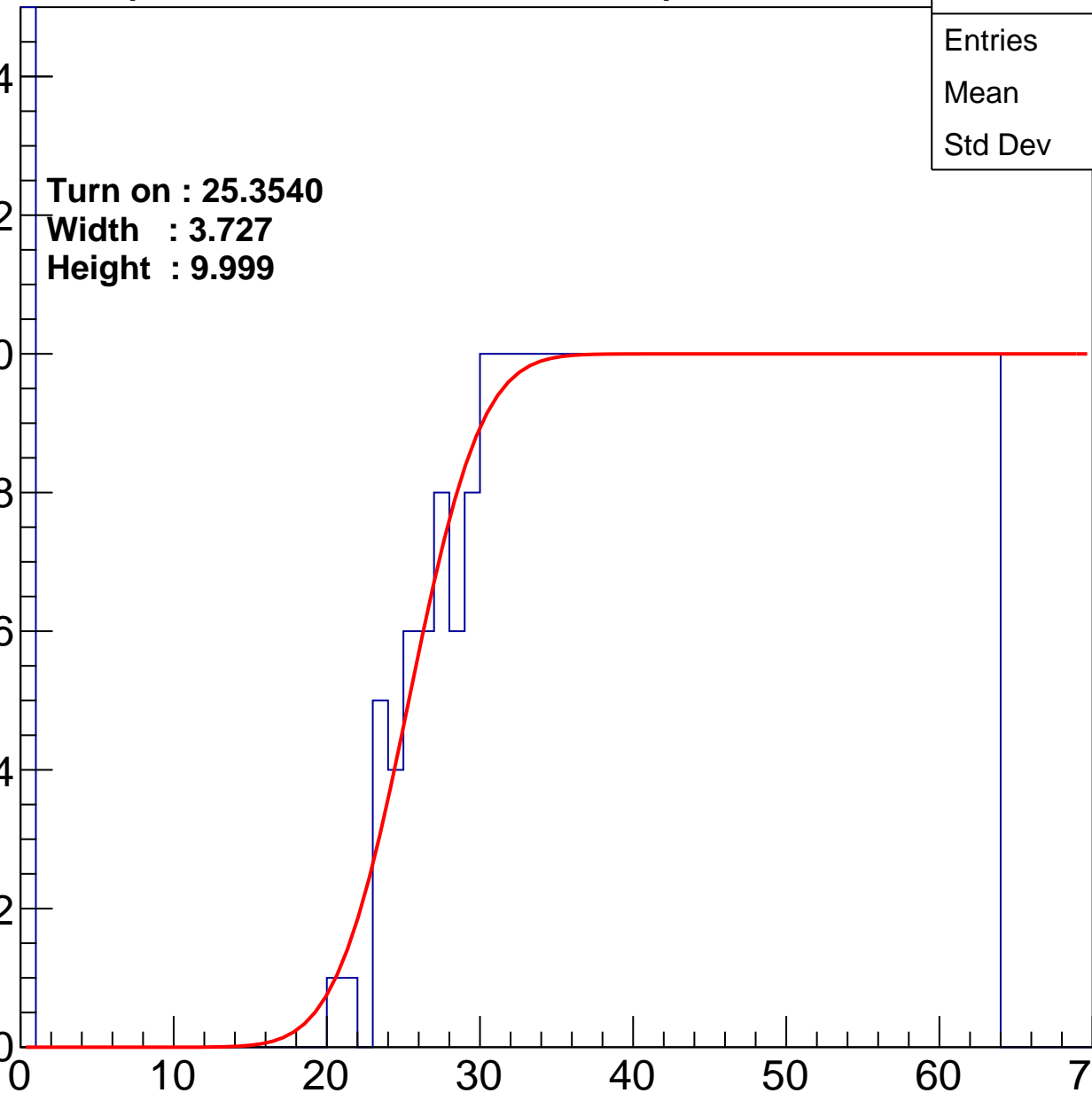
Width : 3.727

Height : 9.999

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch93

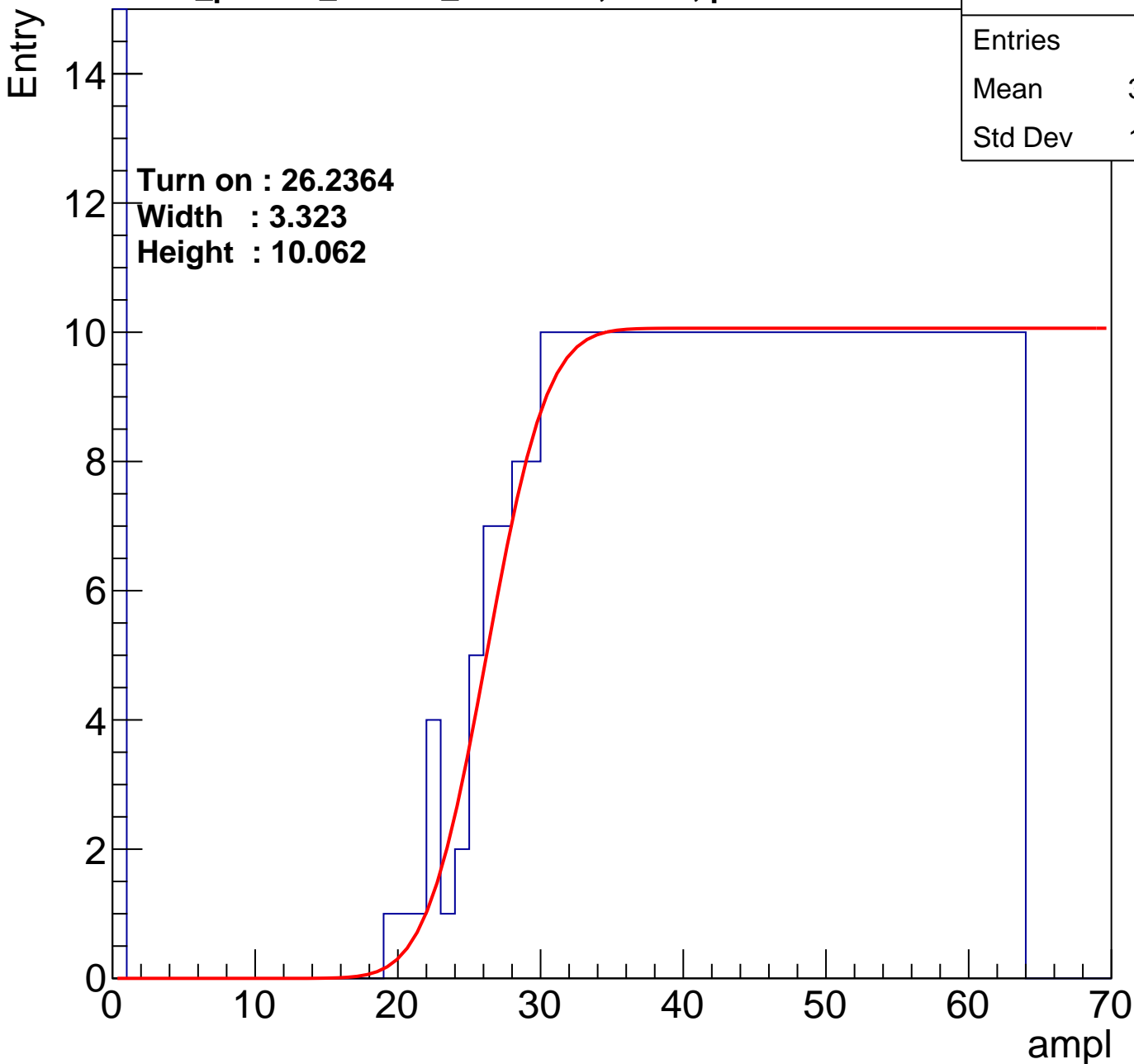
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	450
Mean	37.74
Std Dev	18.73

Turn on : 26.2364

Width : 3.323

Height : 10.062



# B1L103S, U4-ch94

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	421
Mean	39.84
Std Dev	17.27

**Turn on : 26.3497**

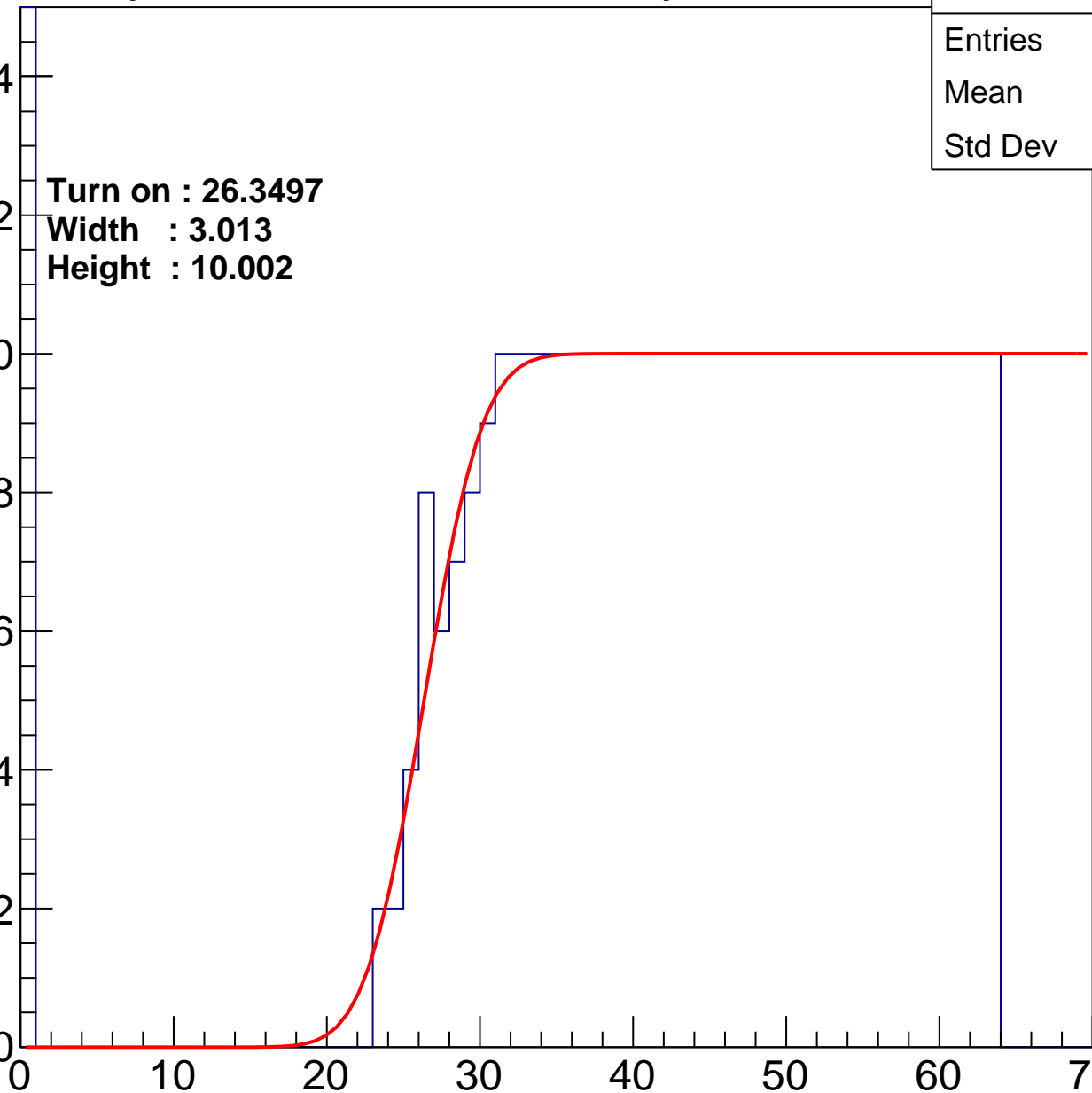
**Width : 3.013**

**Height : 10.002**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L103S, U4-ch95

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	407
Mean	40.42
Std Dev	17.18

**Turn on : 27.7908**

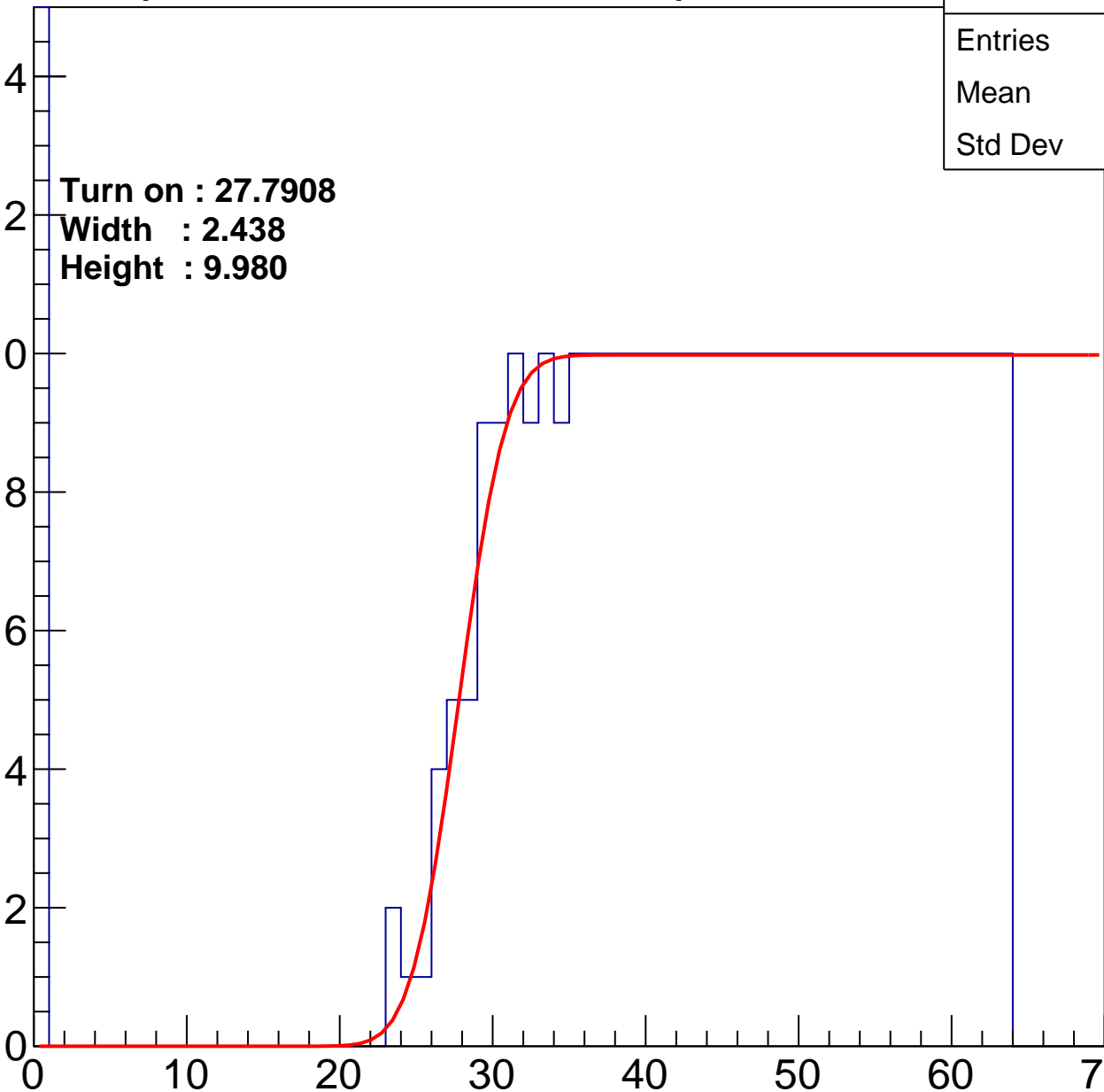
**Width : 2.438**

**Height : 9.980**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch96

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	460
Mean	37.42
Std Dev	18.68

Turn on : 25.5782

Width : 2.568

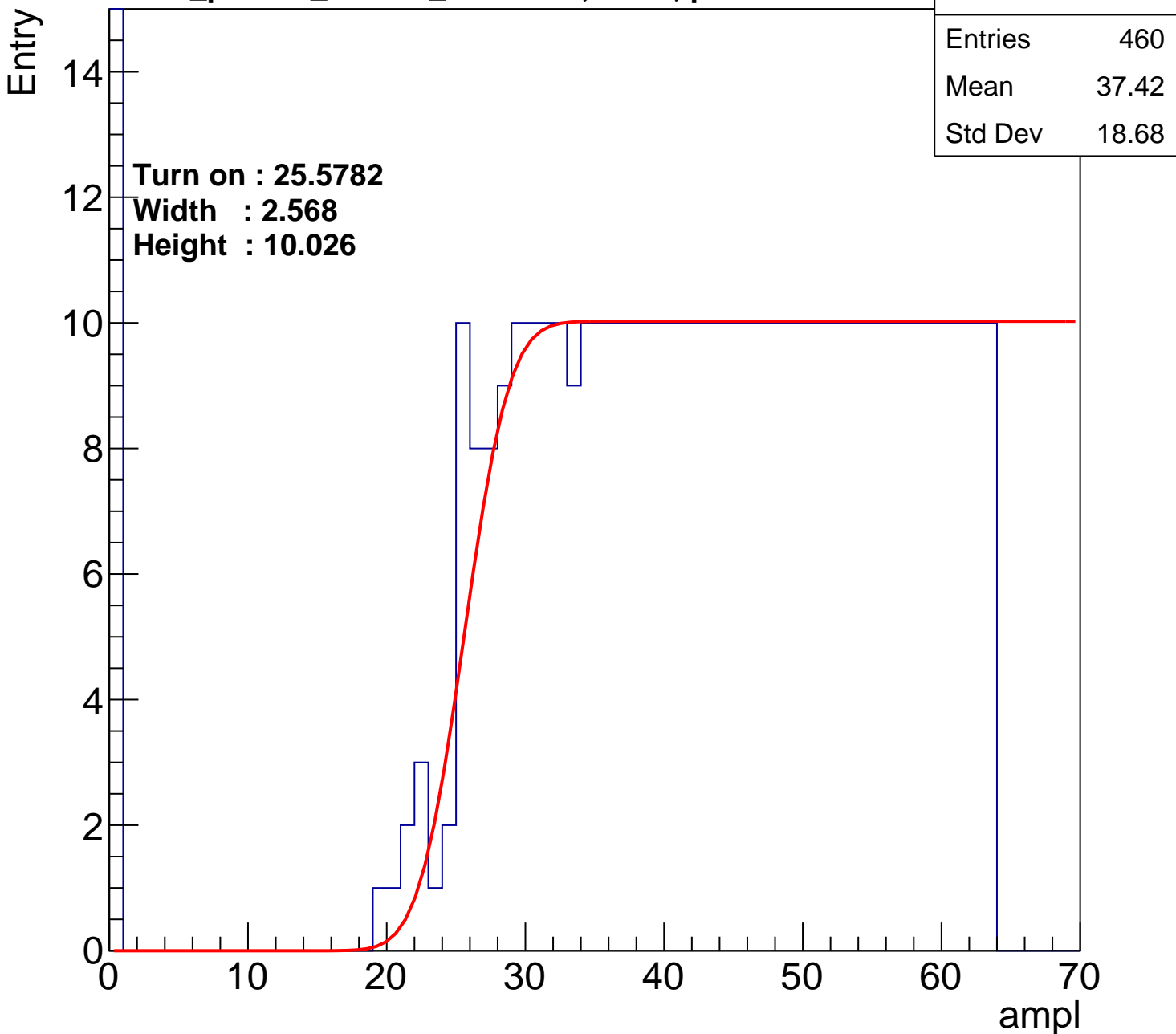
Height : 10.026

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U4-ch97

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	440
Mean	38.55
Std Dev	18.12

Turn on : 26.0211

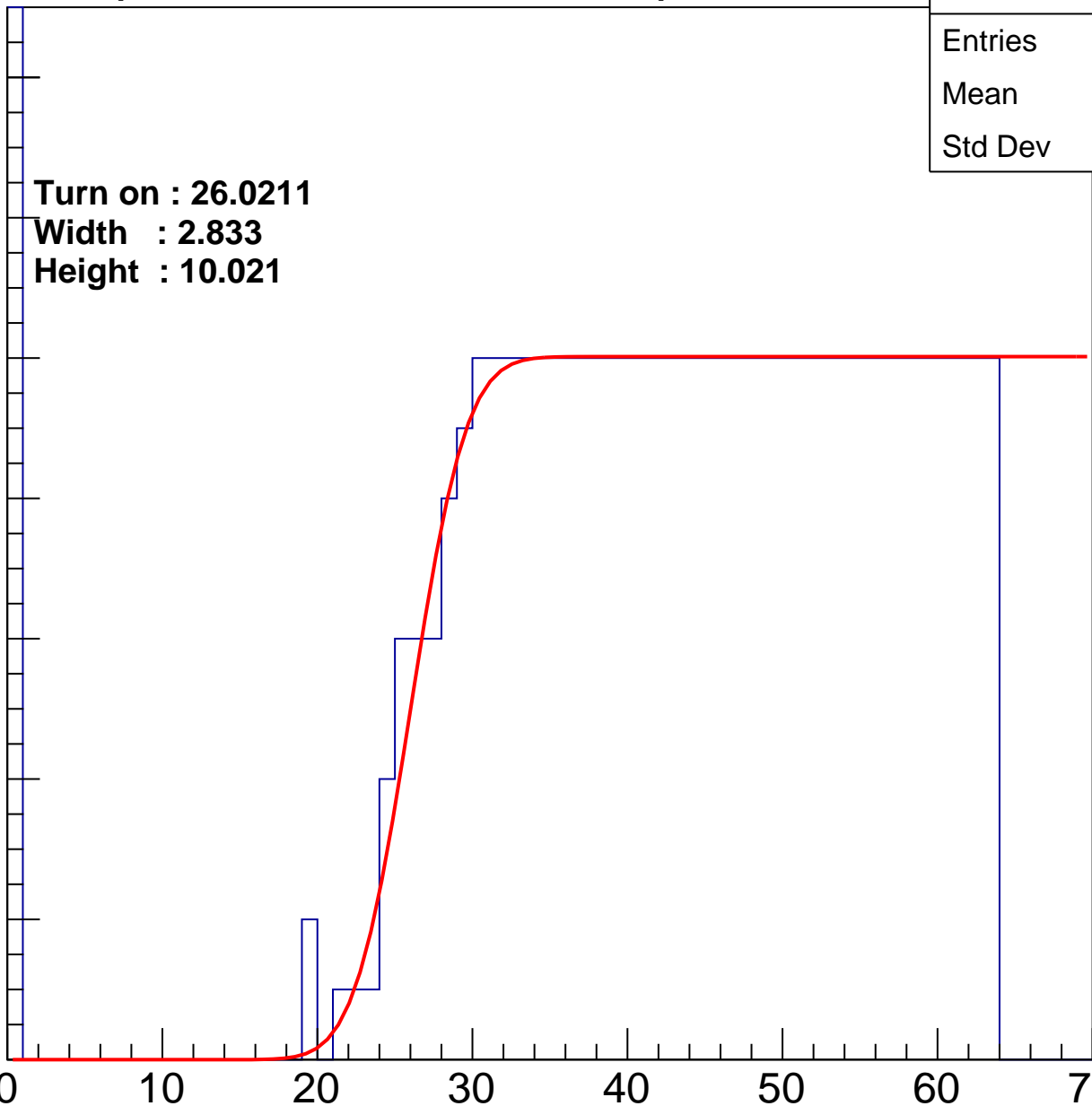
Width : 2.833

Height : 10.021

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch98

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	447
Mean	38.47
Std Dev	17.87

Turn on : 25.0511

Width : 0.822

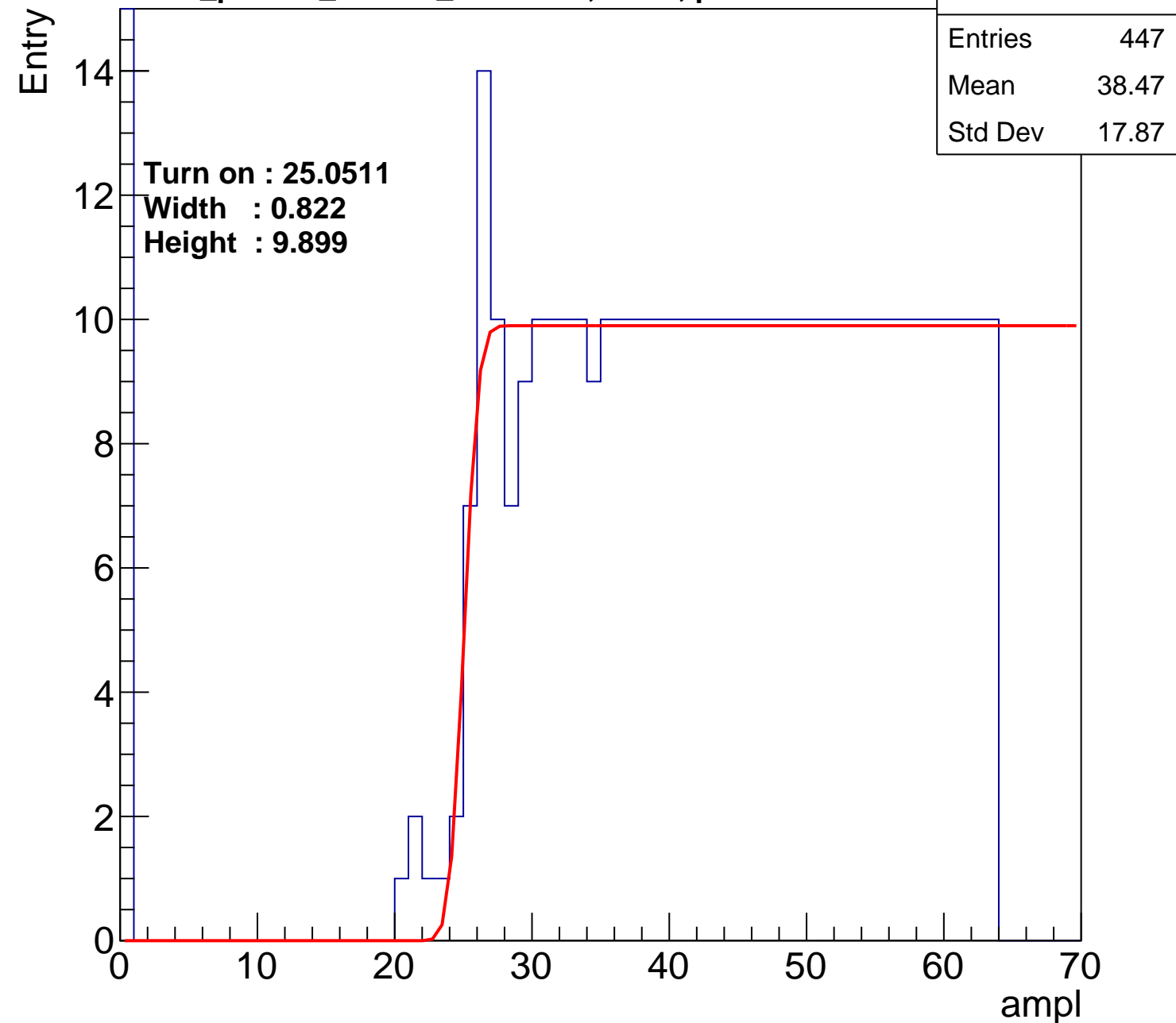
Height : 9.899

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U4-ch99

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	413
Mean	40.43
Std Dev	16.77

Turn on : 26.6805

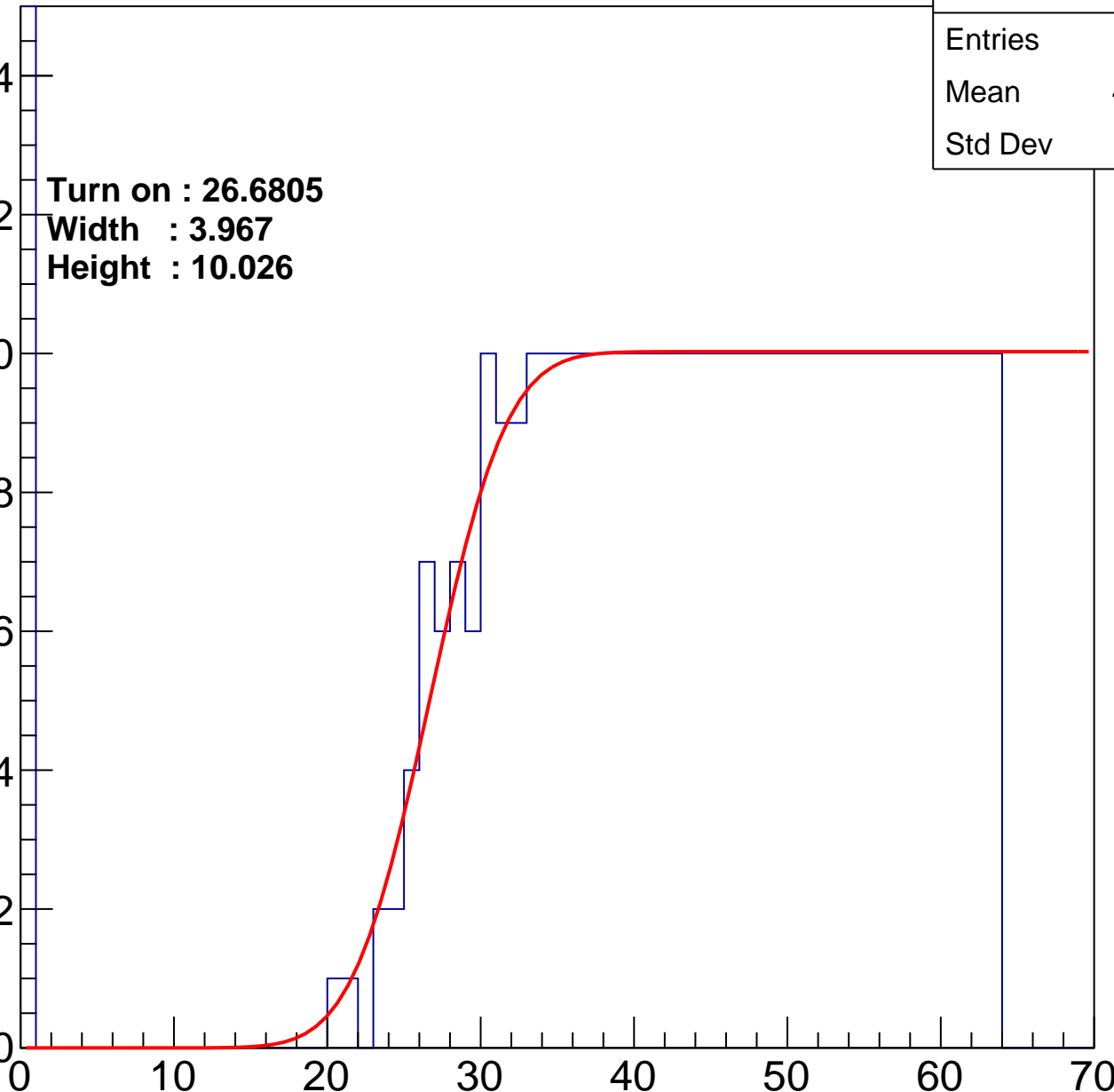
Width : 3.967

Height : 10.026

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch100

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	459
Mean	37.77
Std Dev	18.26

Turn on : 24.1982

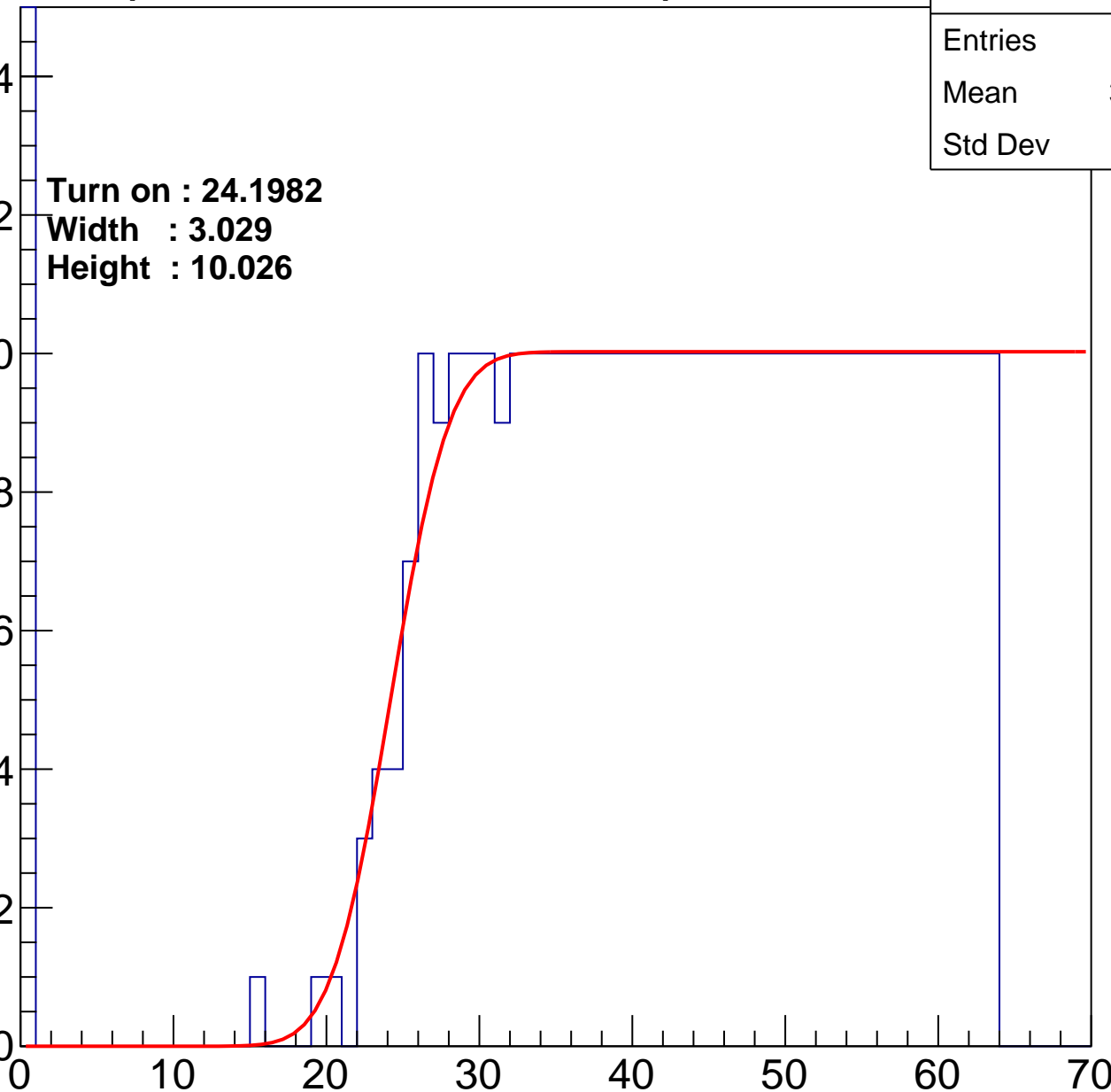
Width : 3.029

Height : 10.026

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch101

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	424
Mean	39.75
Std Dev	17.19

Turn on : 26.3411

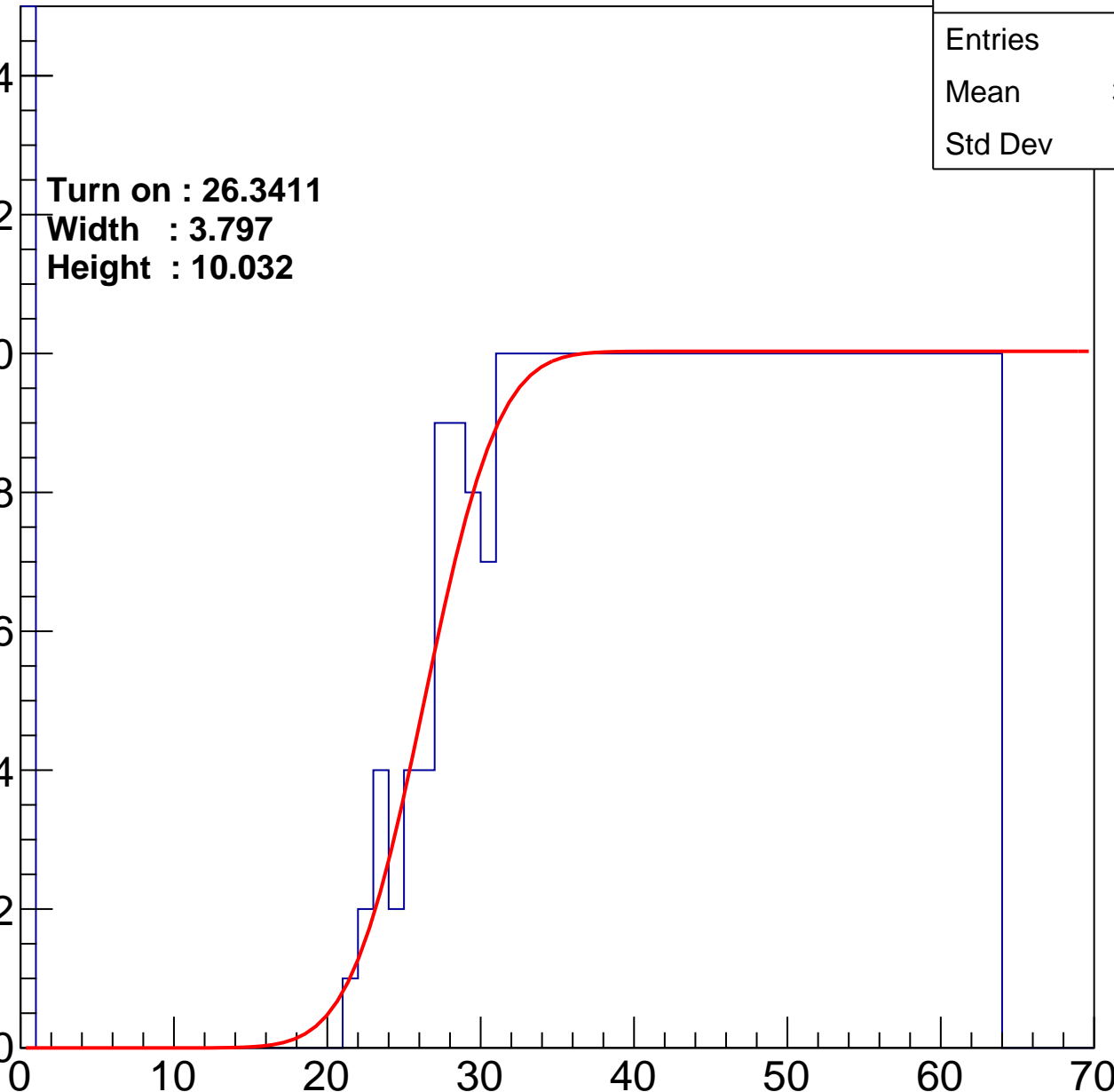
Width : 3.797

Height : 10.032

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch102

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	455
Mean	37.59
Std Dev	18.71

Turn on : 25.4668

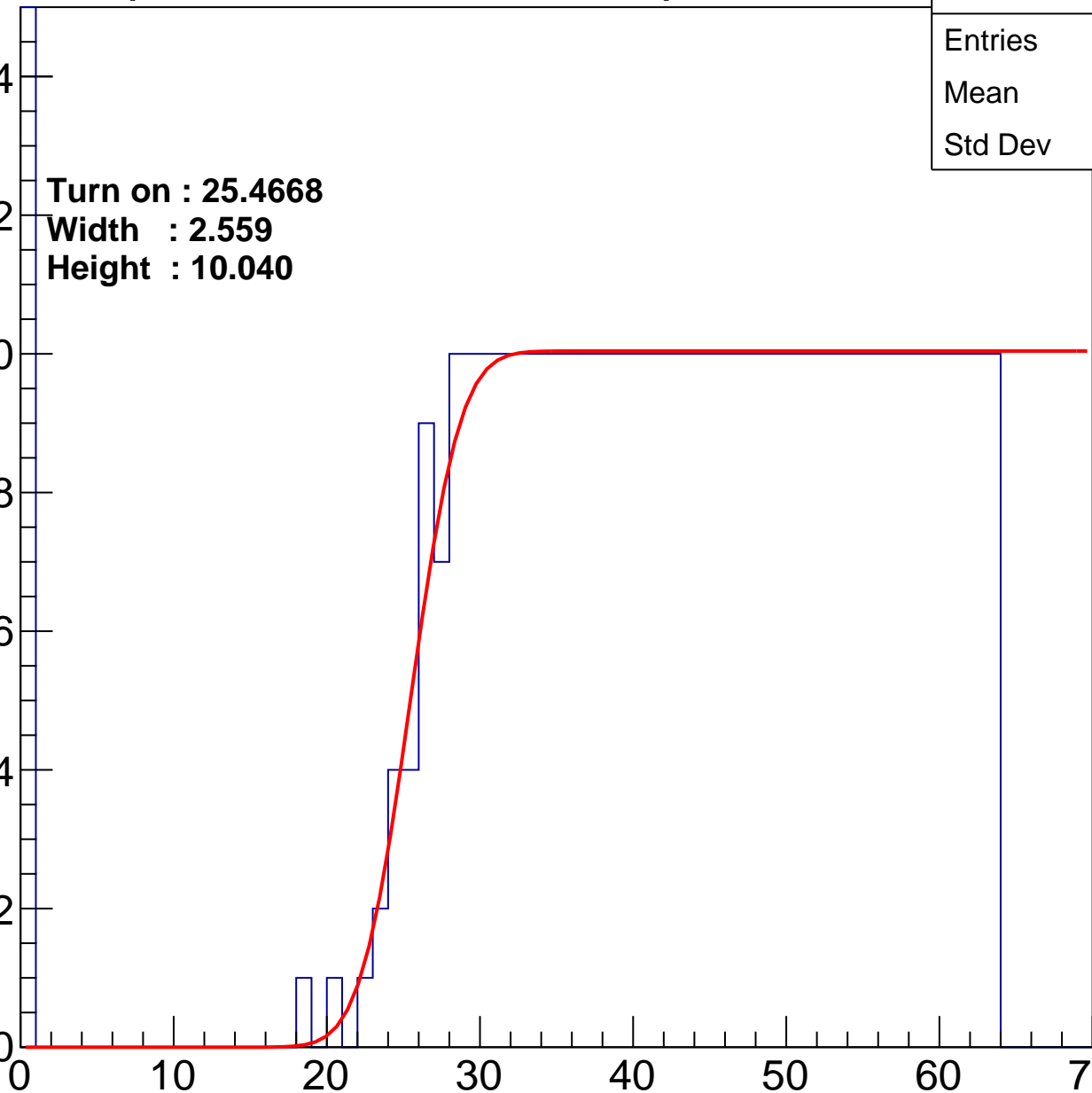
Width : 2.559

Height : 10.040

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L103S, U4-ch103

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	443
Mean	39.26
Std Dev	16.9

Turn on : 24.4117

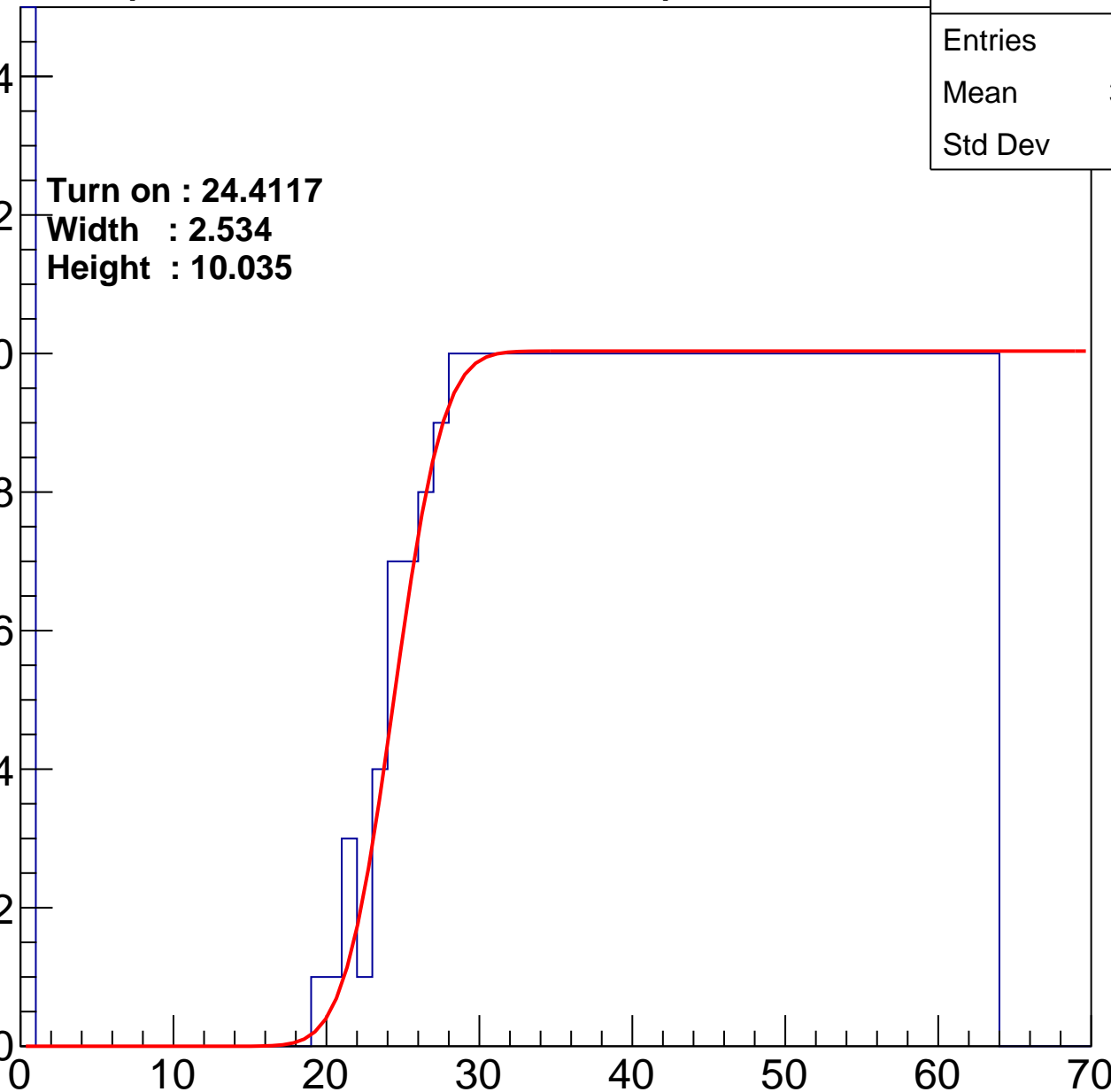
Width : 2.534

Height : 10.035

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch104

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	445
Mean	38.29
Std Dev	18.23

**Turn on : 25.4304**

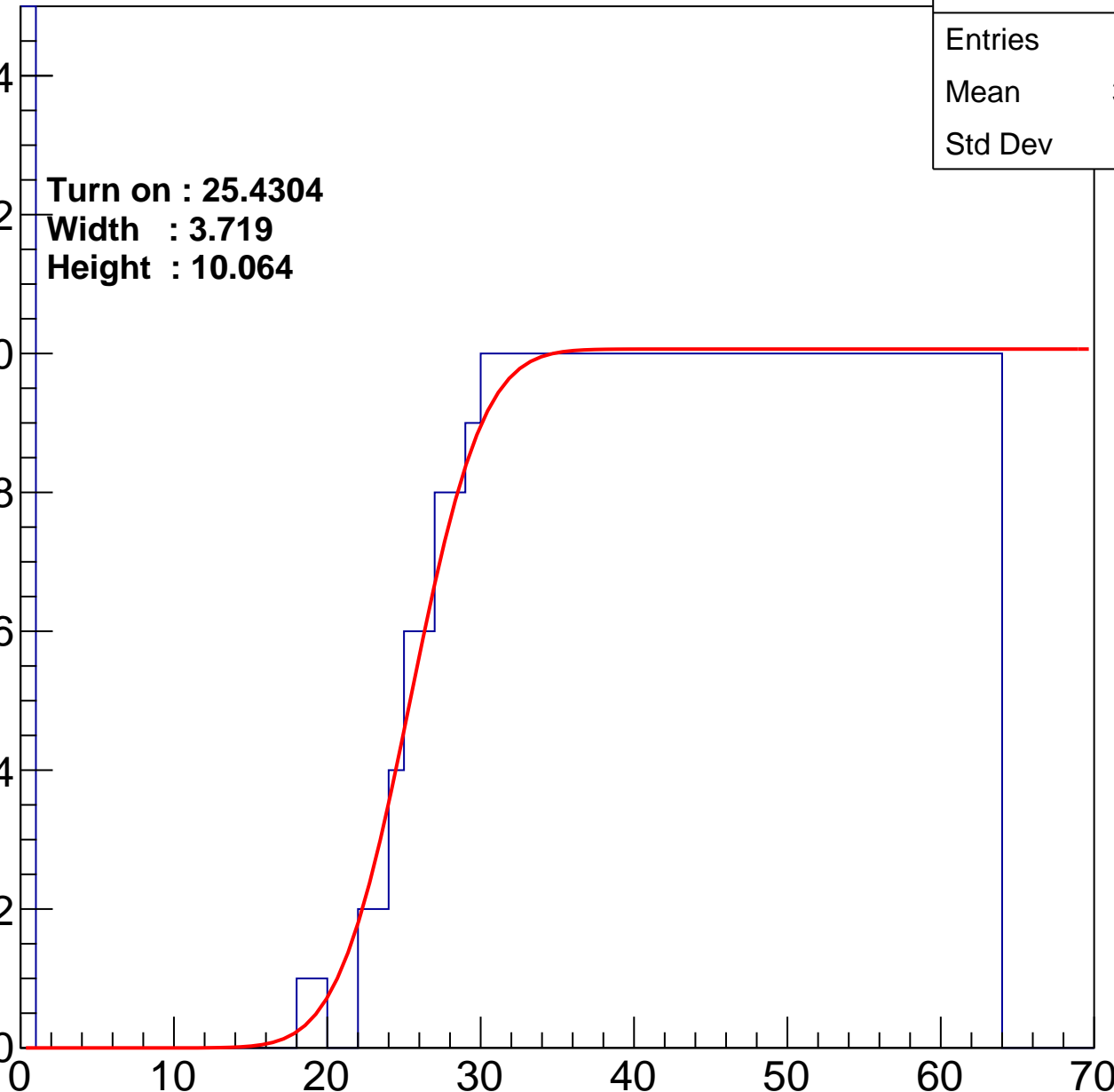
**Width : 3.719**

**Height : 10.064**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch105

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	428
Mean	38.32
Std Dev	19.01

Turn on : 27.8374

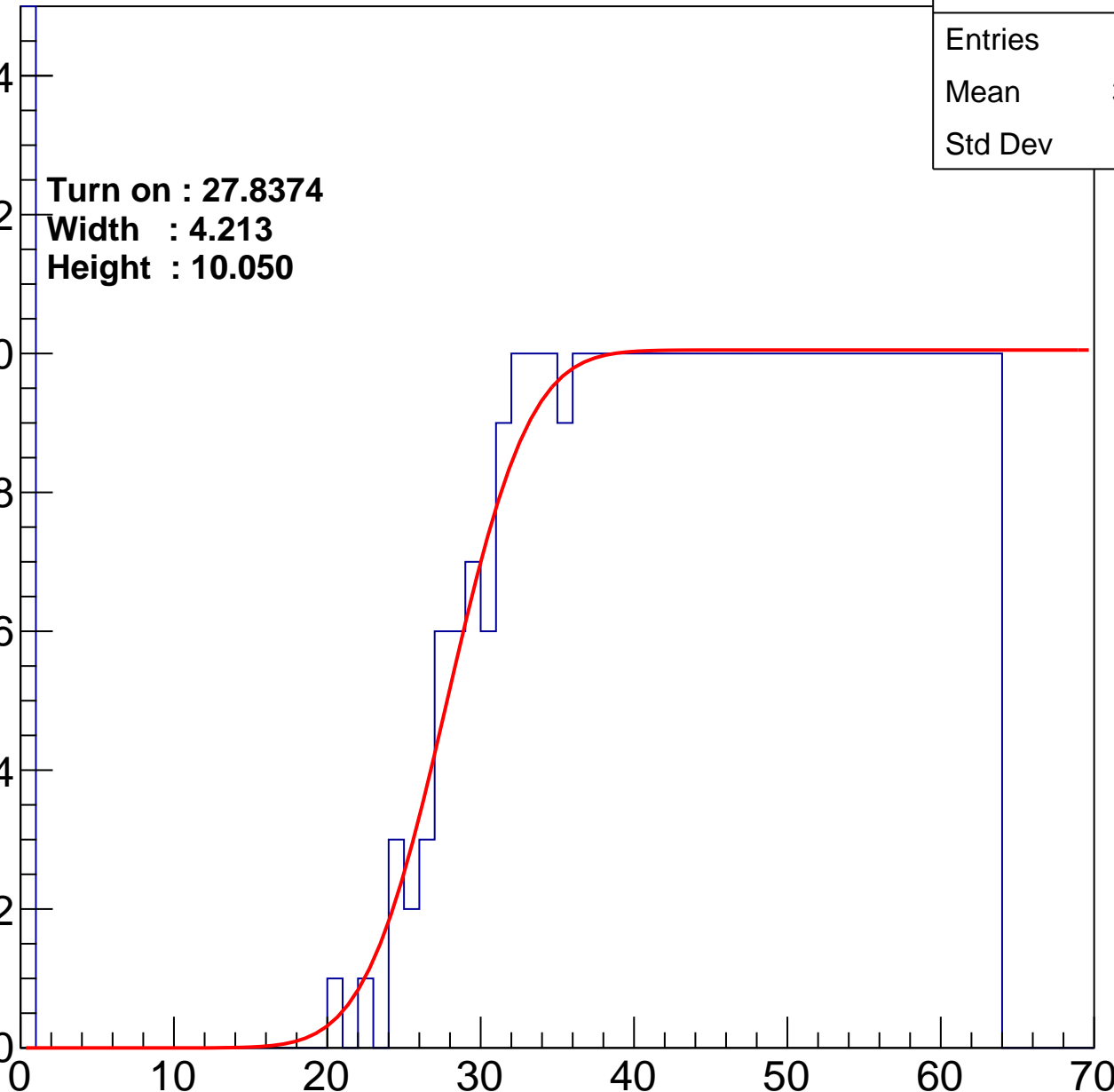
Width : 4.213

Height : 10.050

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch106

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	463
Mean	37.75
Std Dev	18.04

Turn on : 23.8900

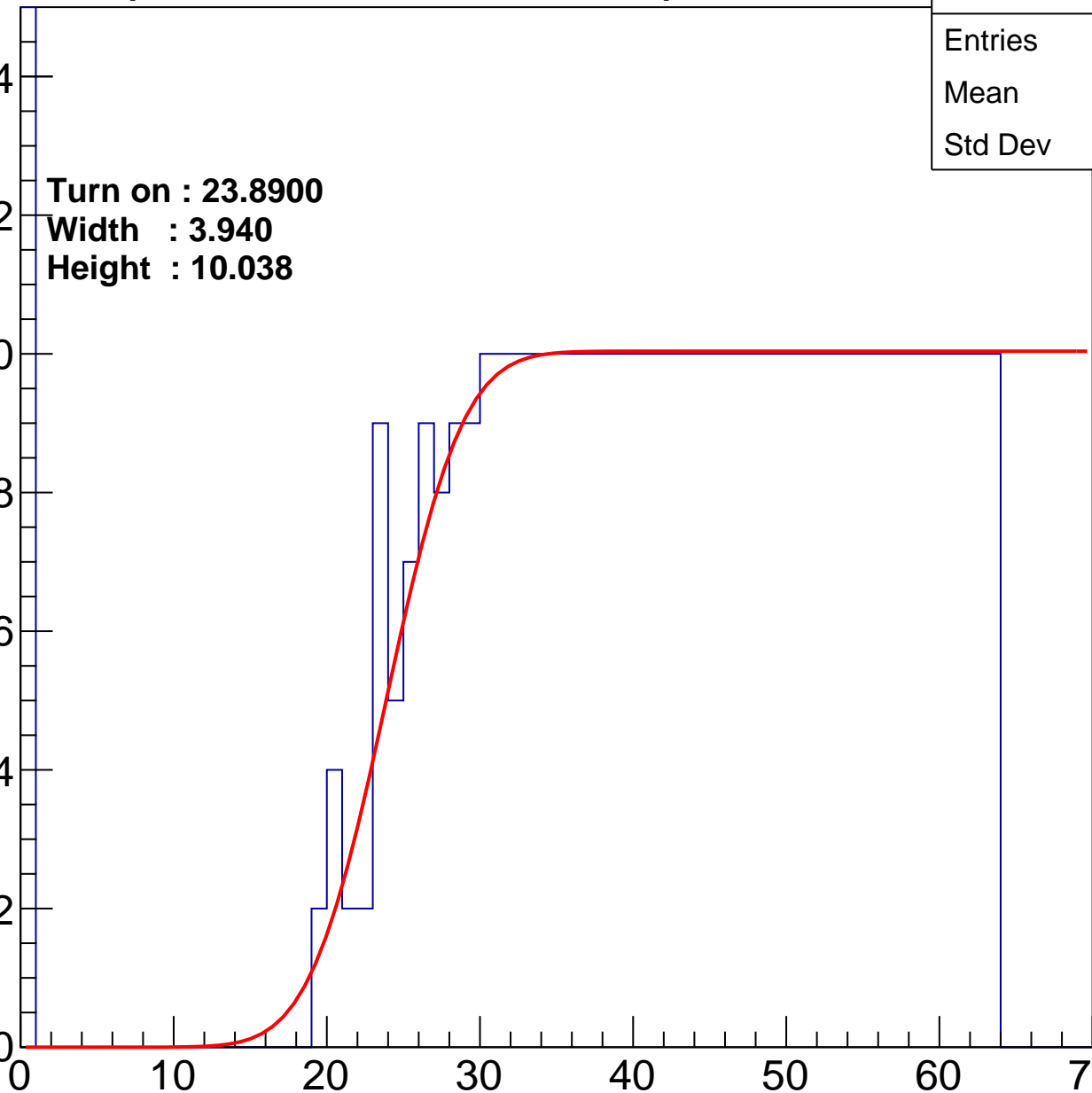
Width : 3.940

Height : 10.038

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch107

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	443
Mean	37.67
Std Dev	19.16

Turn on : 26.7991

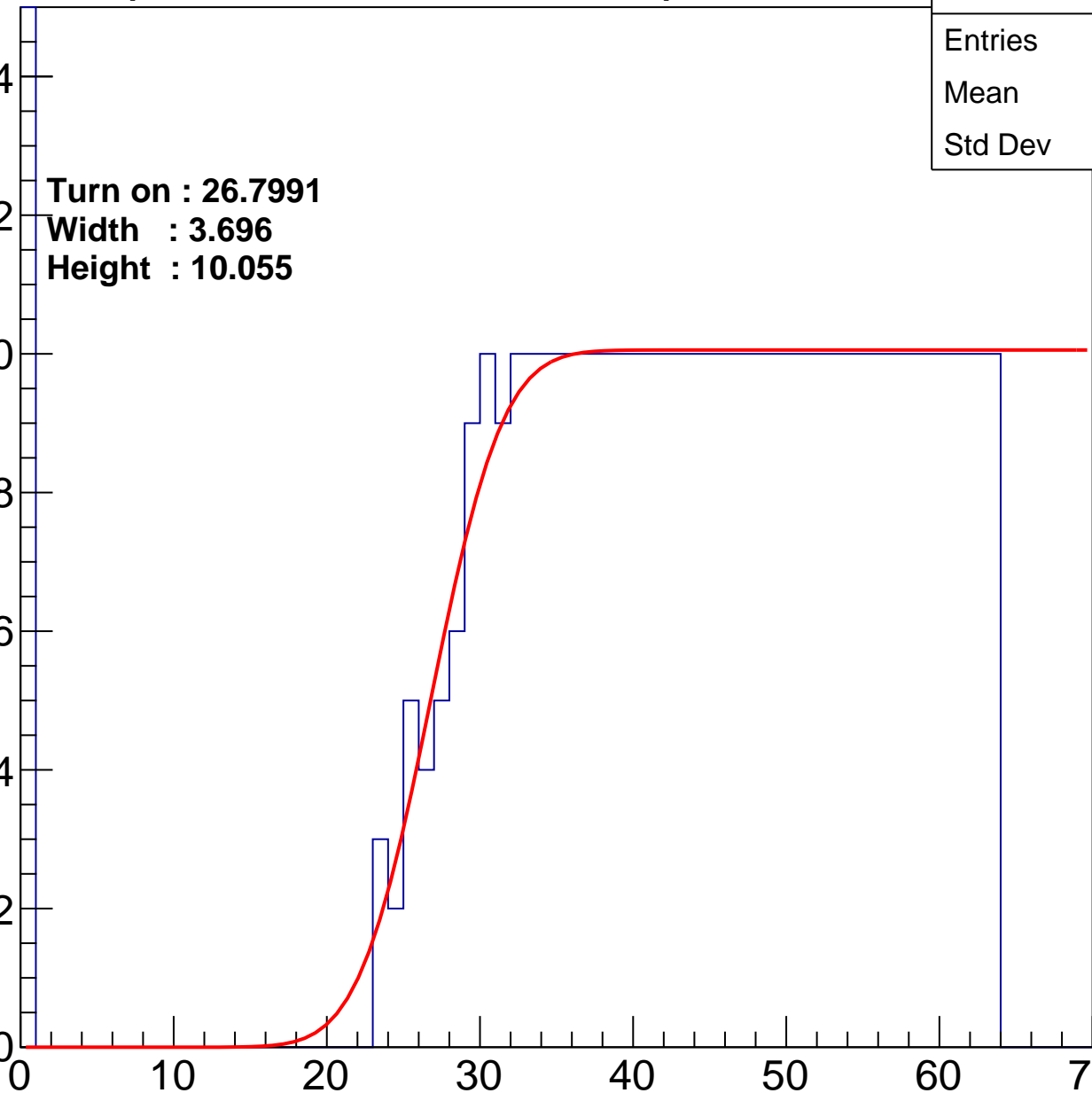
Width : 3.696

Height : 10.055

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch108

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	468
Mean	36.97
Std Dev	18.89

**Turn on : 23.5496**

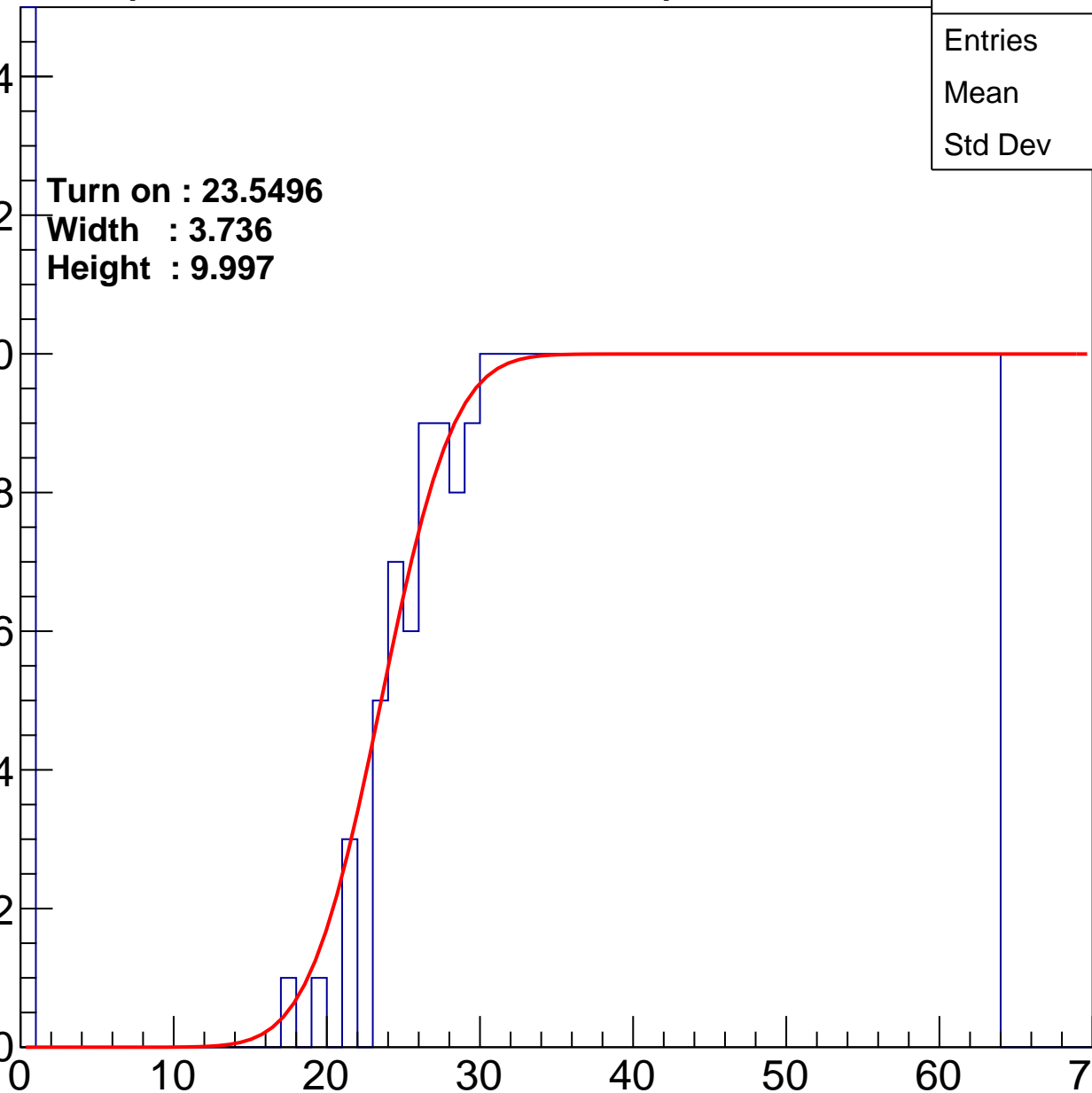
**Width : 3.736**

**Height : 9.997**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch109

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	417
Mean	40.15
Std Dev	17.01

**Turn on : 26.7674**

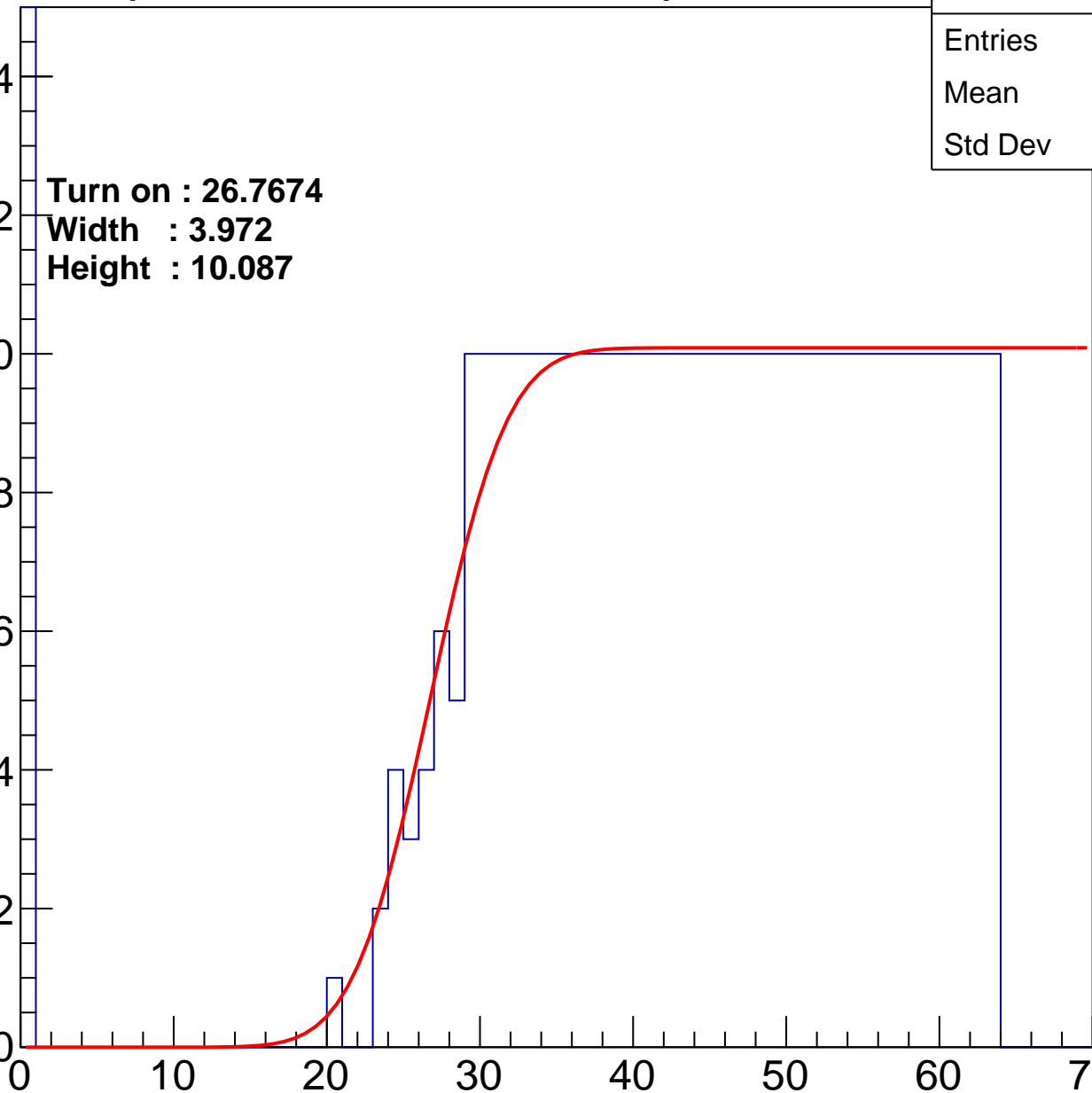
**Width : 3.972**

**Height : 10.087**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch110

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	452
Mean	38.27
Std Dev	17.92

Turn on : 24.3737

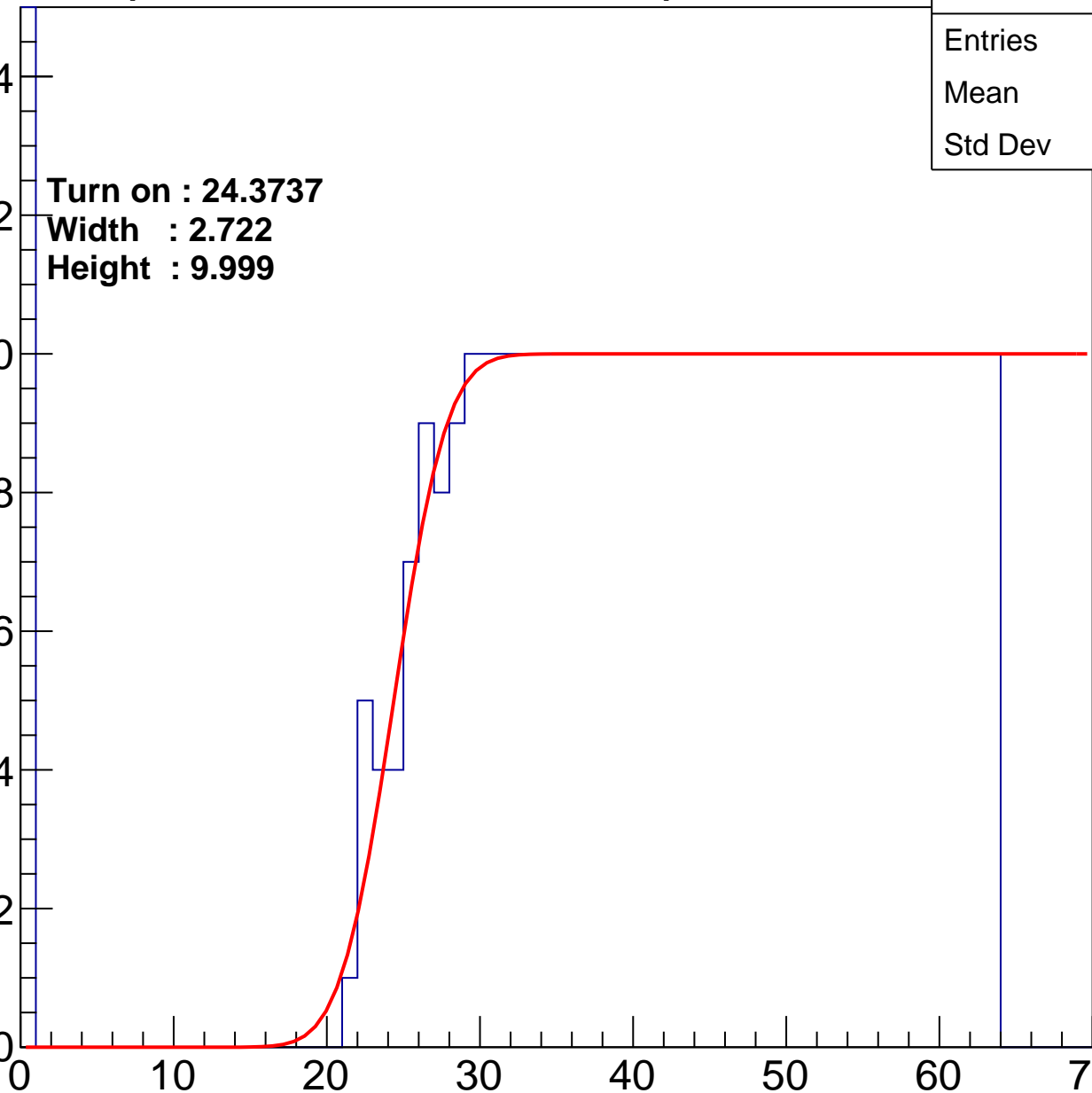
Width : 2.722

Height : 9.999

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L103S, U4-ch111

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	426
Mean	38.92
Std Dev	18.33

**Turn on : 26.8436**

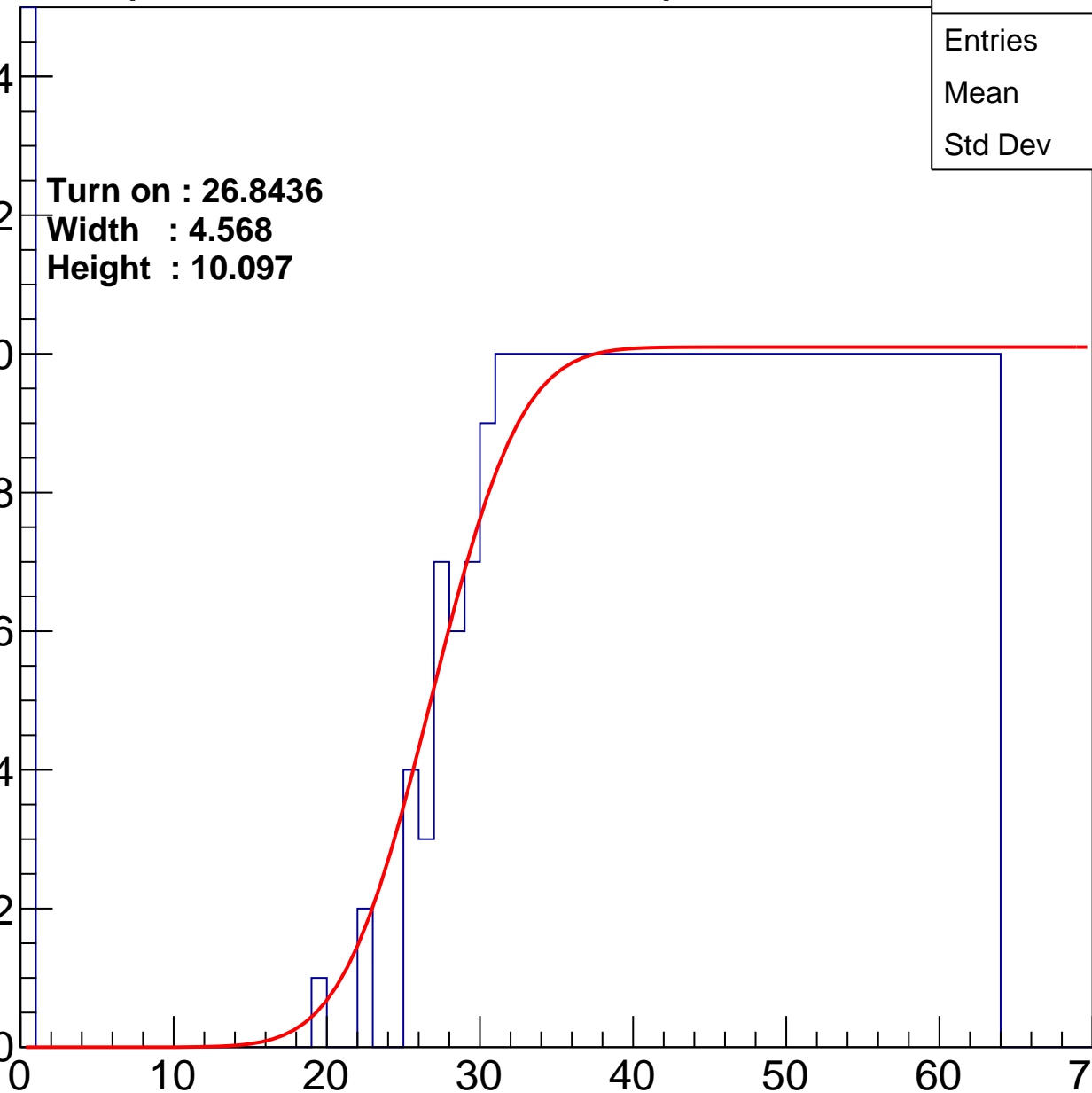
**Width : 4.568**

**Height : 10.097**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch112

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	436
Mean	38.56
Std Dev	18.27

**Turn on : 26.0952**

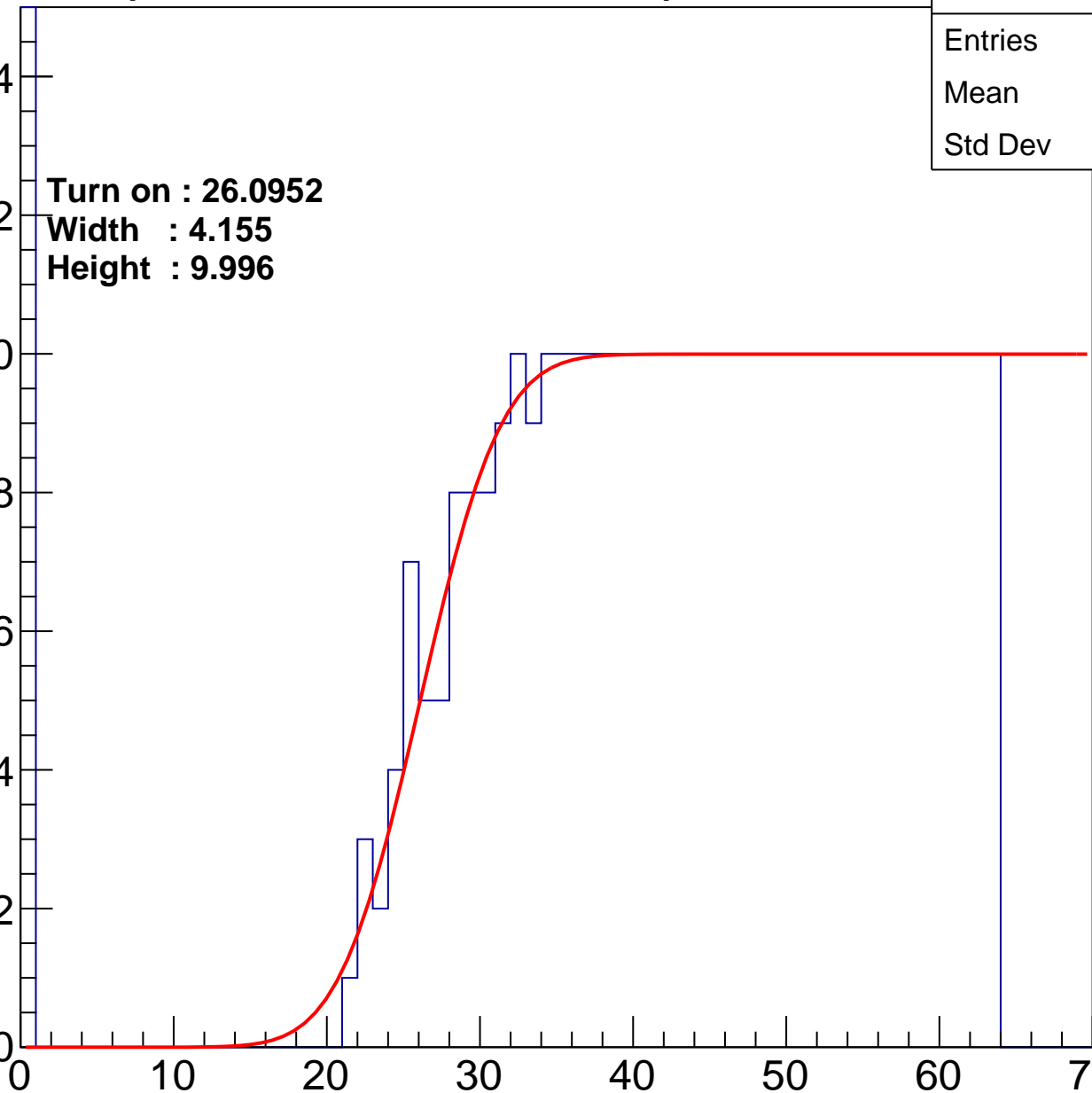
**Width : 4.155**

**Height : 9.996**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch113

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	454
Mean	38
Std Dev	18.17

Turn on : 24.8539

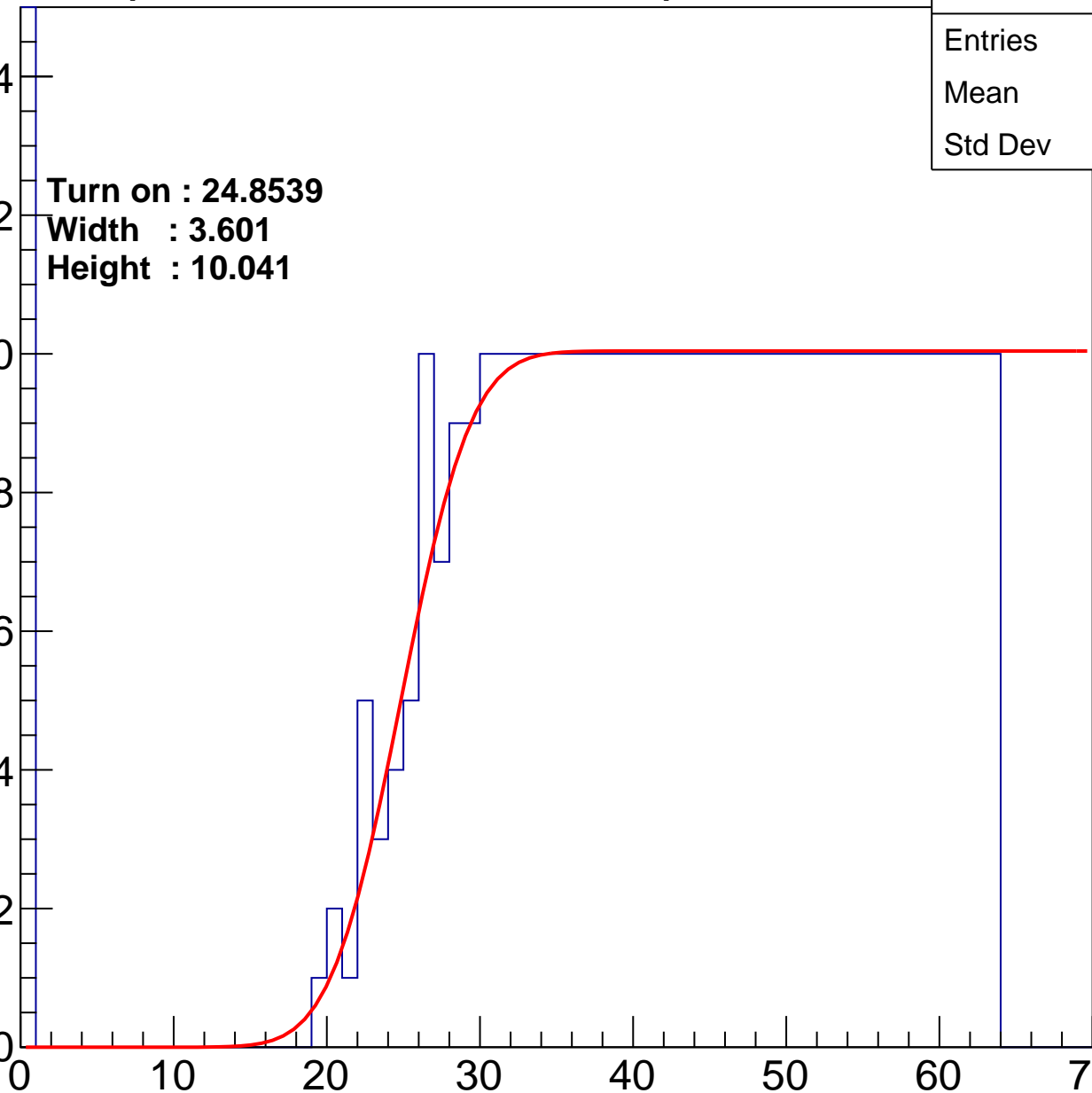
Width : 3.601

Height : 10.041

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch114

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	426
Mean	40.01
Std Dev	16.65

Turn on : 25.4931

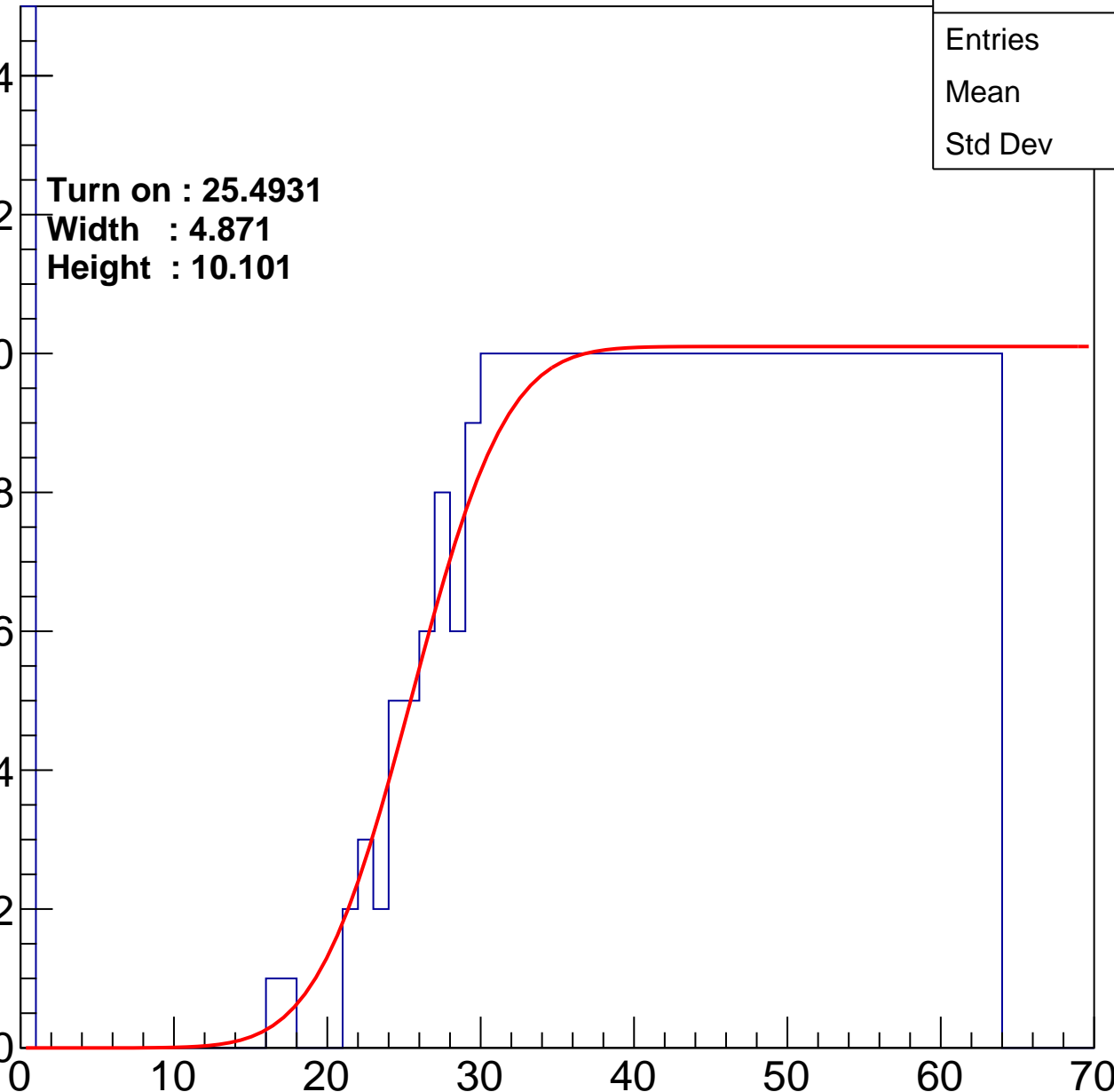
Width : 4.871

Height : 10.101

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch115

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	467
Mean	36.45
Std Dev	19.61

Turn on : 25.7160

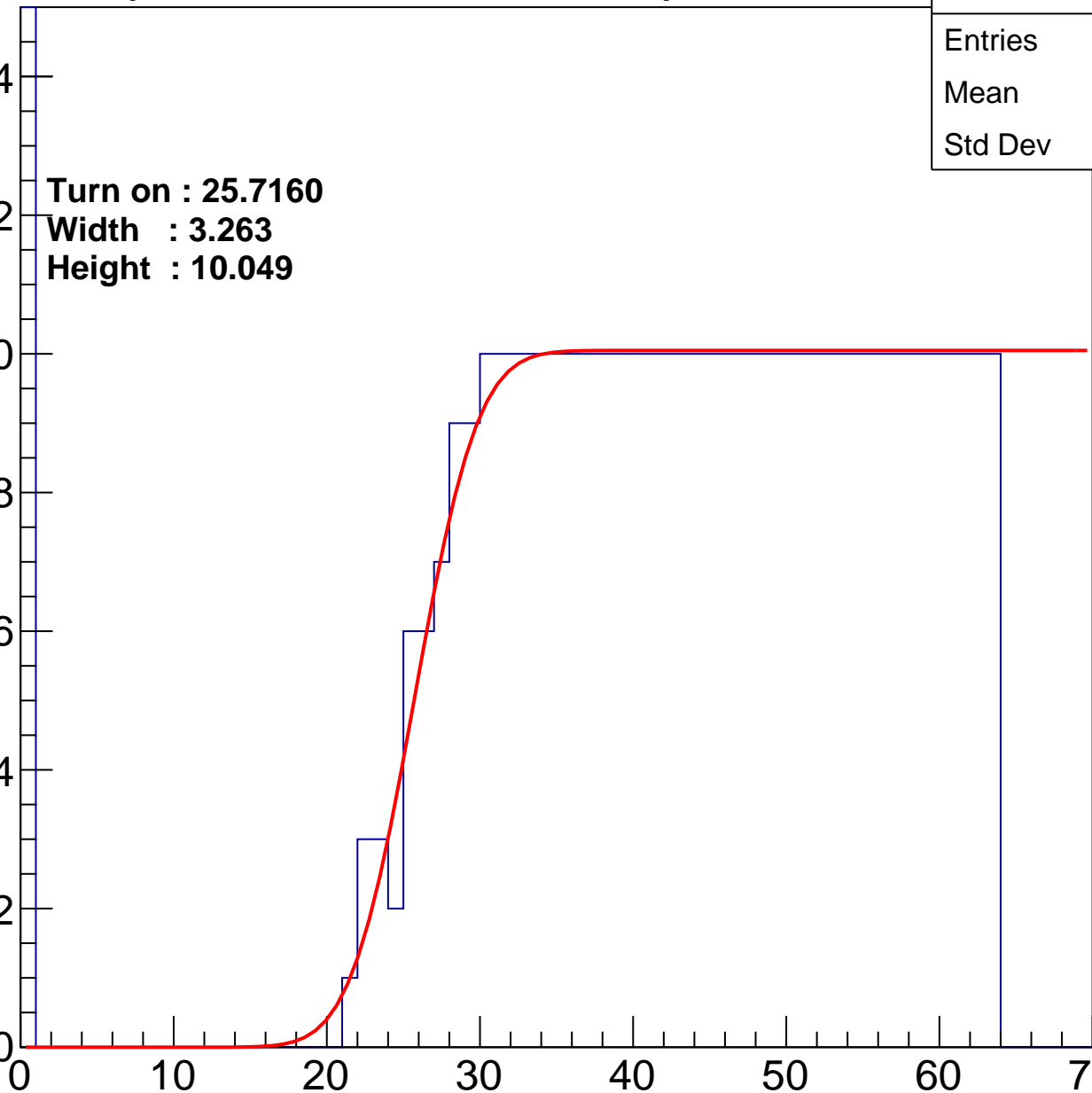
Width : 3.263

Height : 10.049

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch116

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	471
Mean	37.45
Std Dev	18.07

**Turn on : 22.7633**

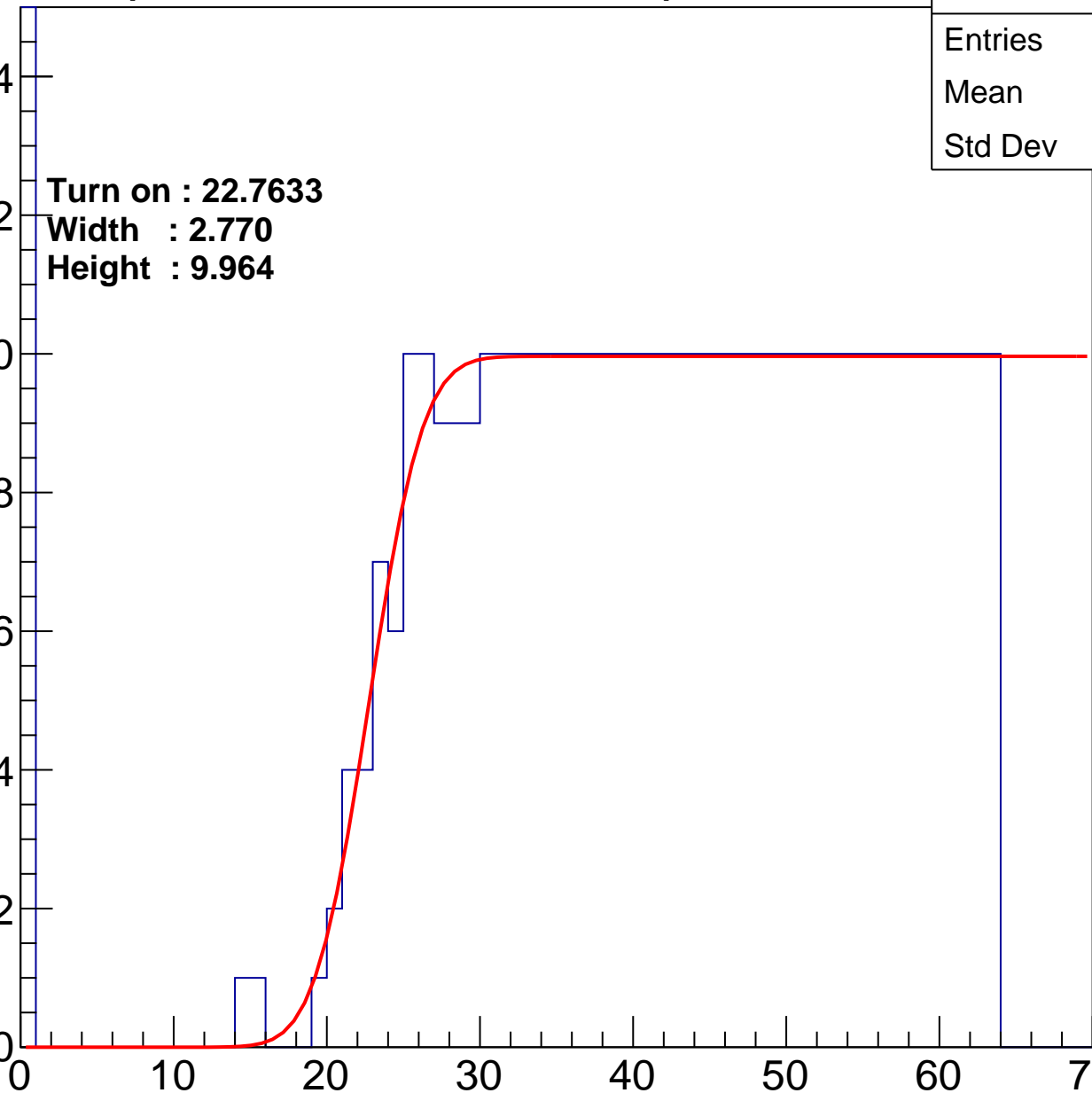
**Width : 2.770**

**Height : 9.964**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch117

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	424
Mean	39.82
Std Dev	17.14

Turn on : 26.1799

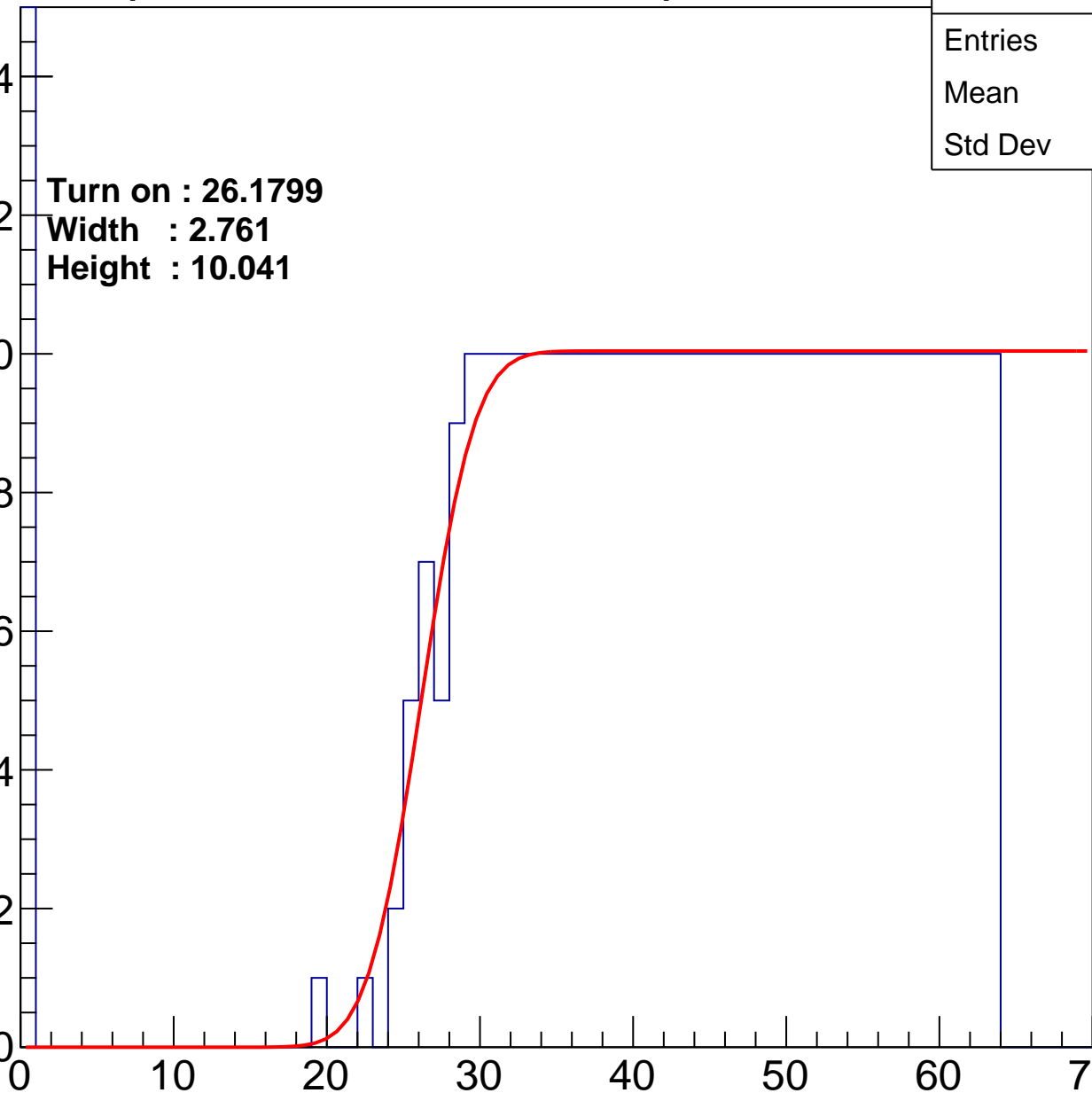
Width : 2.761

Height : 10.041

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch118

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	477
Mean	36.73
Std Dev	18.79

Turn on : 23.6160

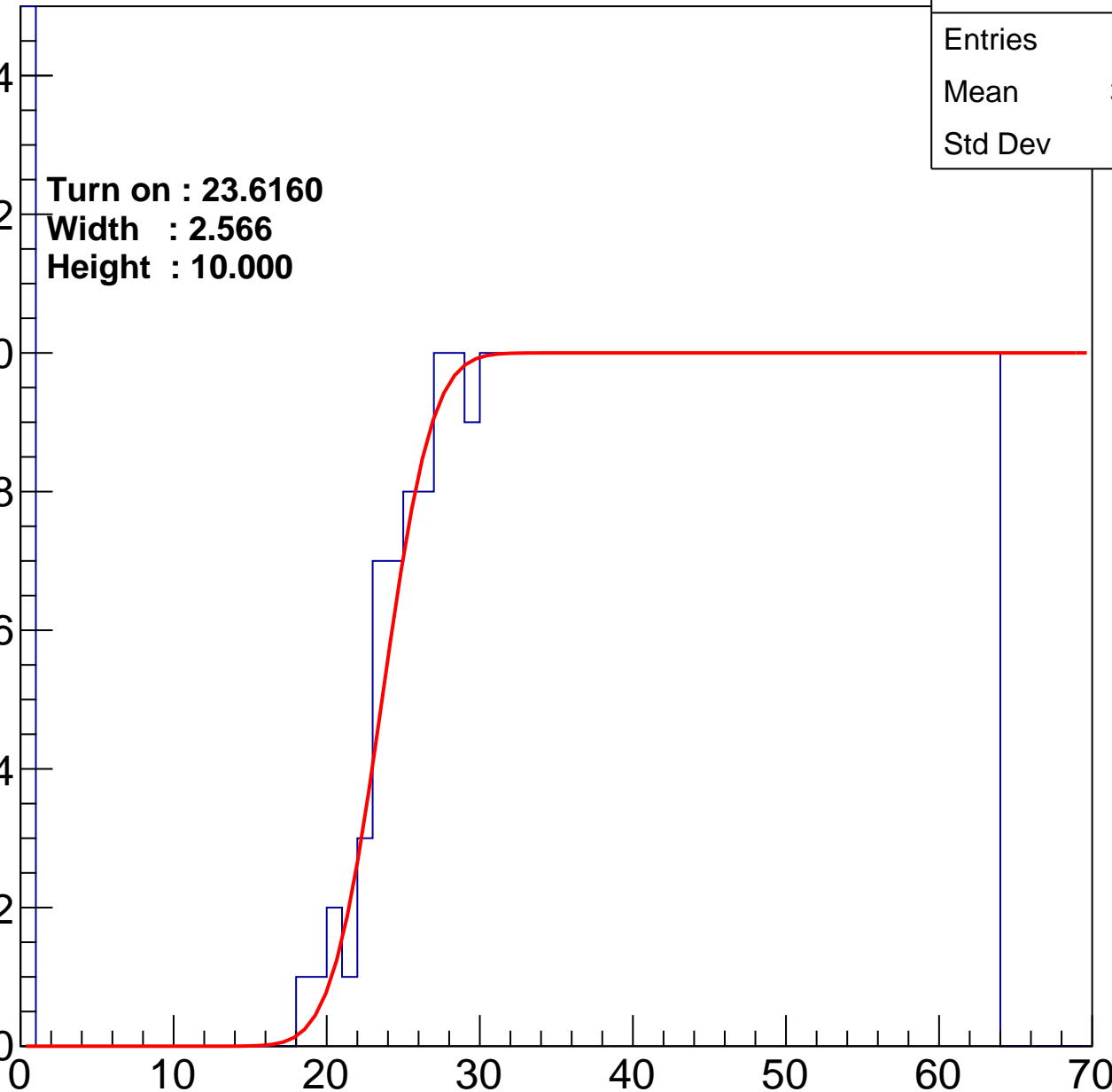
Width : 2.566

Height : 10.000

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L103S, U4-ch119

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	421
Mean	39.94
Std Dev	17.04

**Turn on : 26.0610**

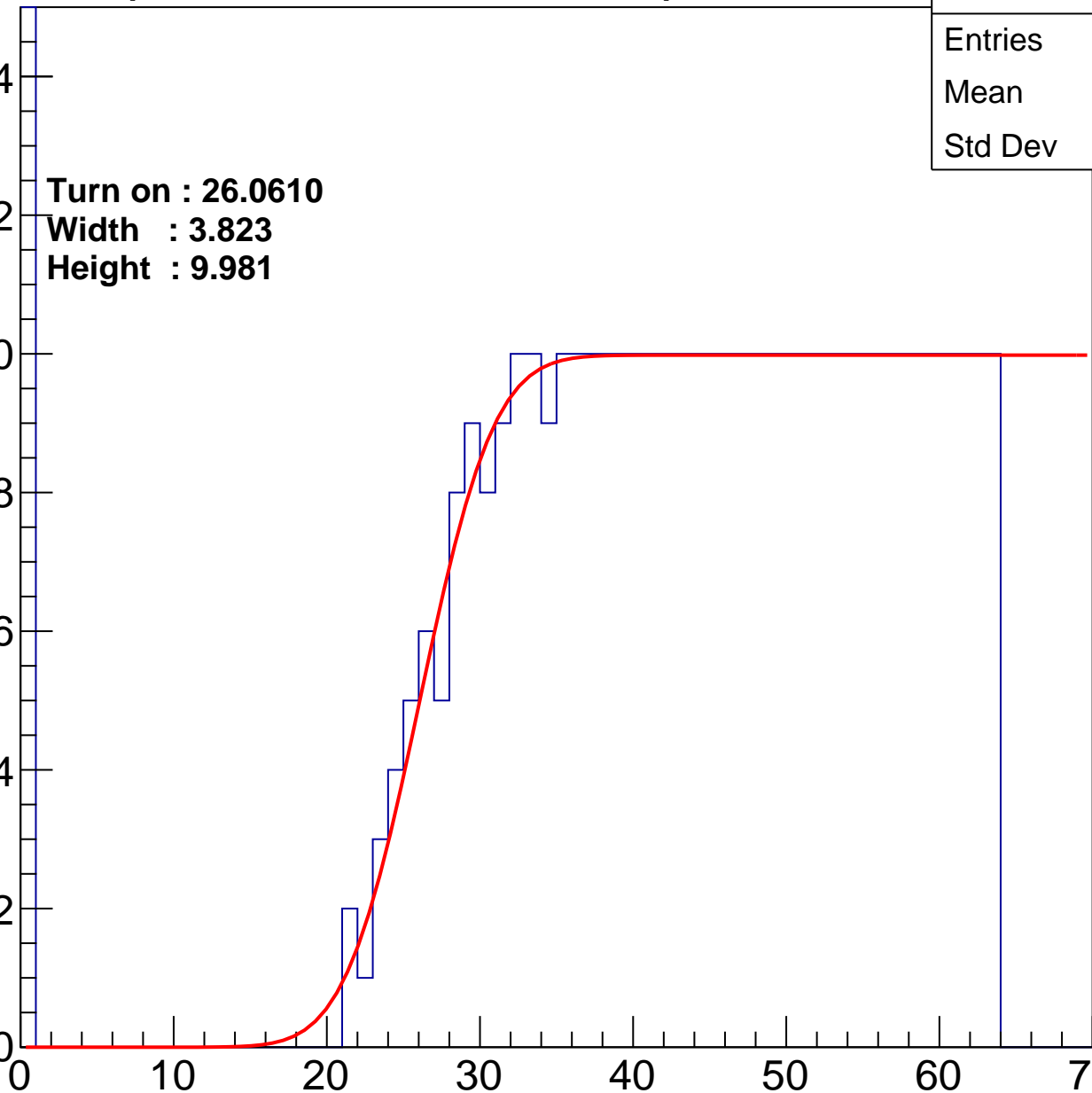
**Width : 3.823**

**Height : 9.981**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch120

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	455
Mean	38.01
Std Dev	18.06

Turn on : 24.5863

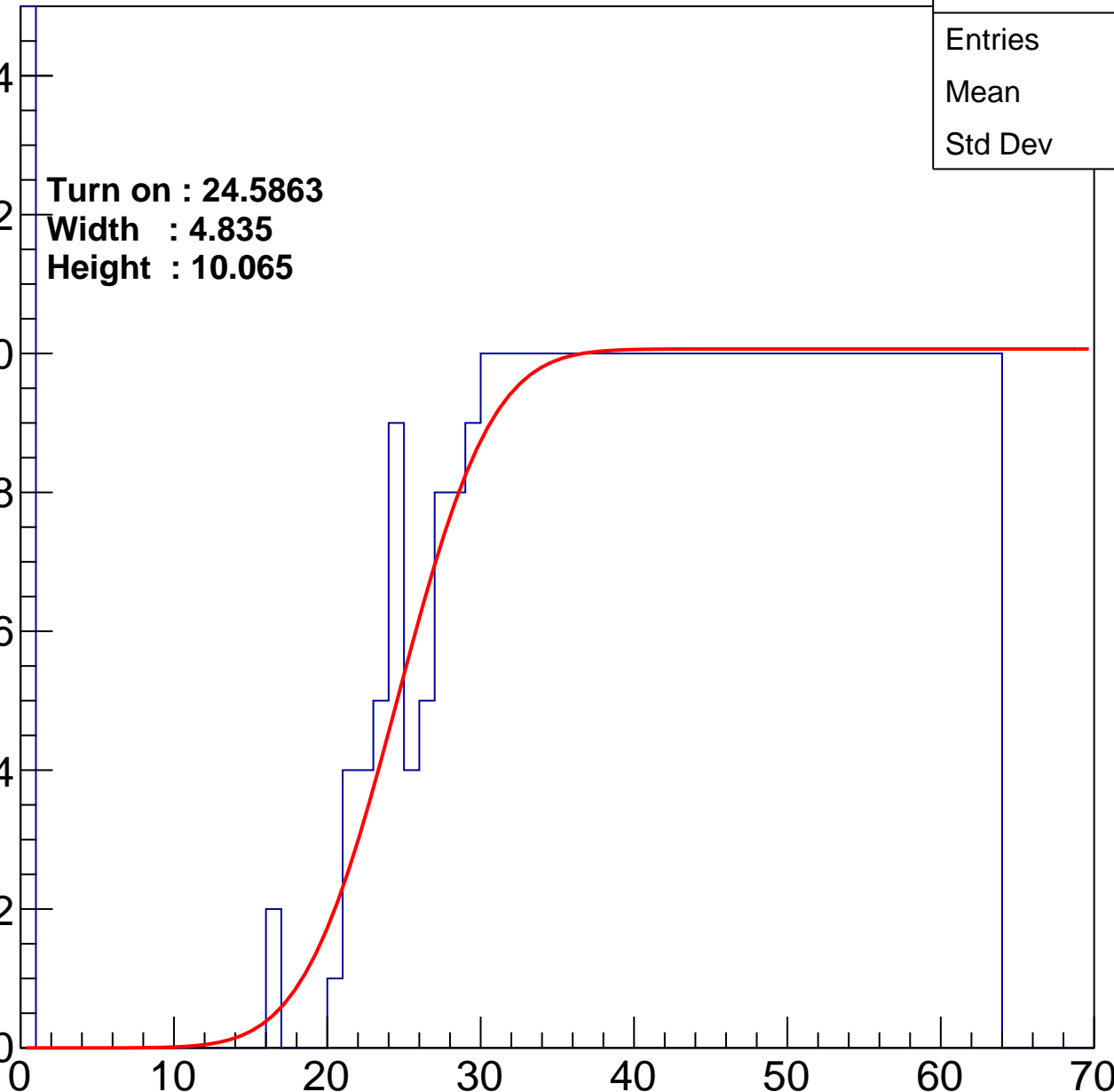
Width : 4.835

Height : 10.065

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch121

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

14

12

10

8

6

4

2

0

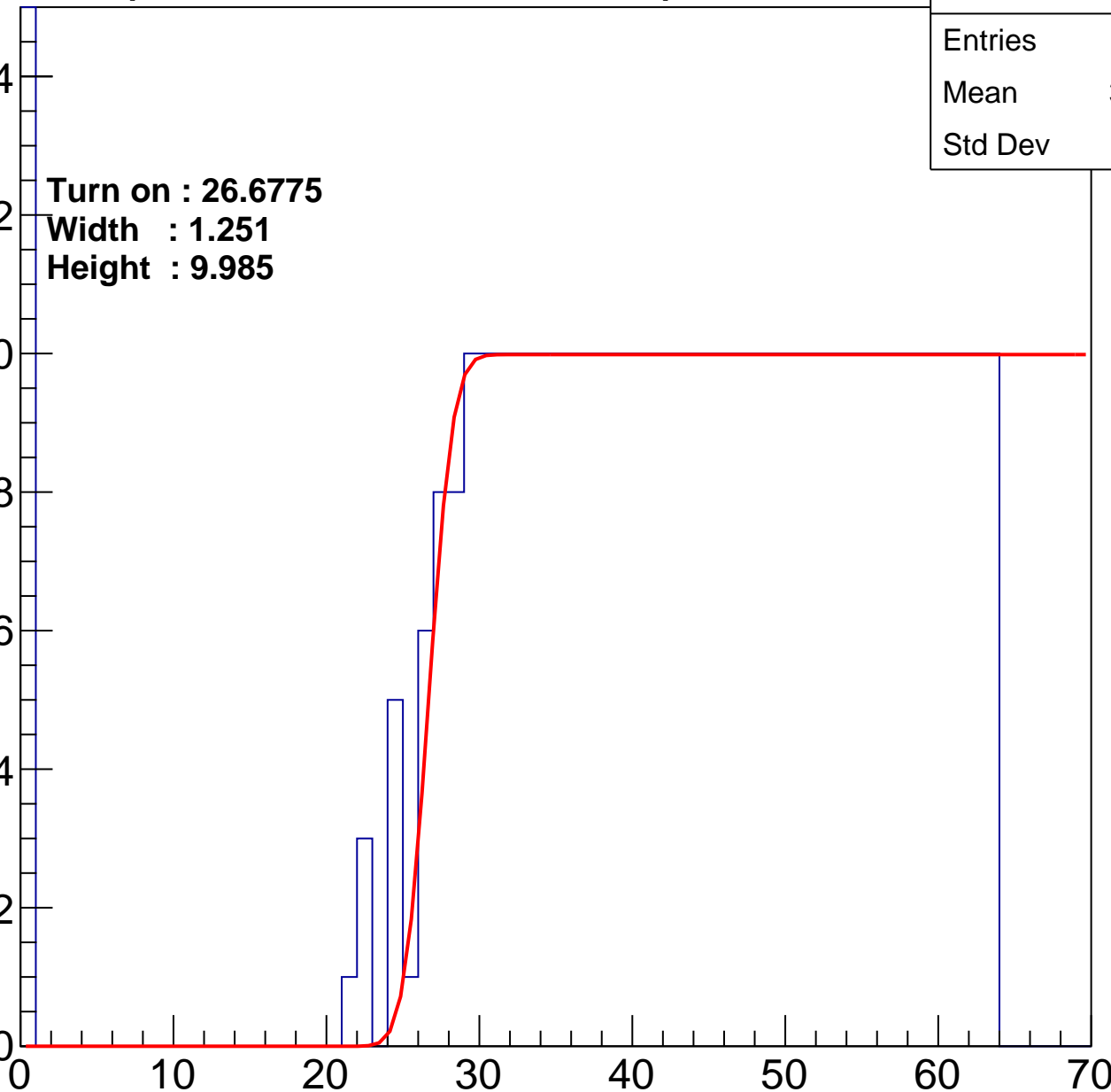
Turn on : 26.6775

Width : 1.251

Height : 9.985

Entries	436
Mean	38.83
Std Dev	17.96

ampl



# B1L103S, U4-ch122

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	468
Mean	37.11
Std Dev	18.76

**Turn on : 24.6655**

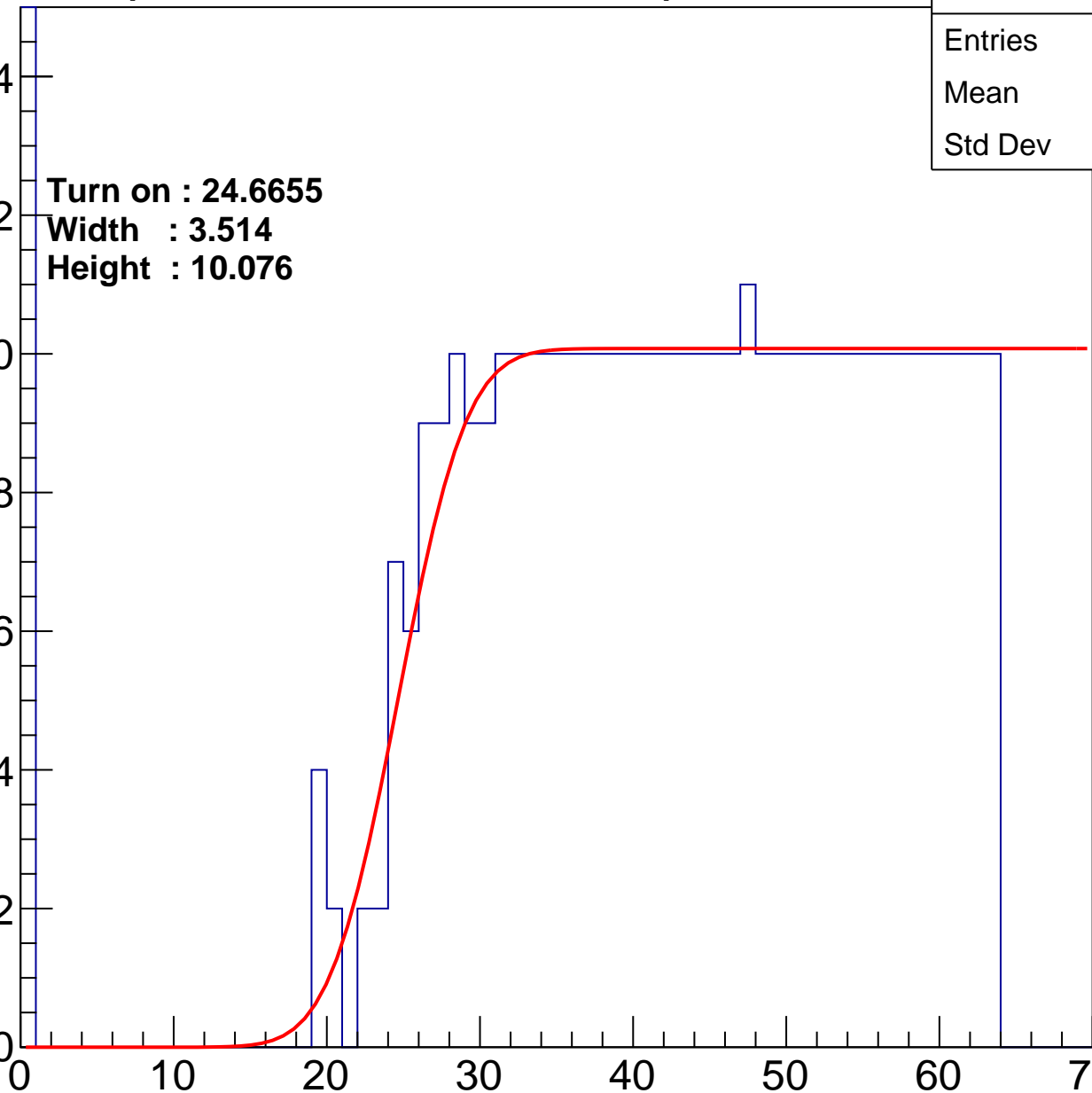
**Width : 3.514**

**Height : 10.076**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch123

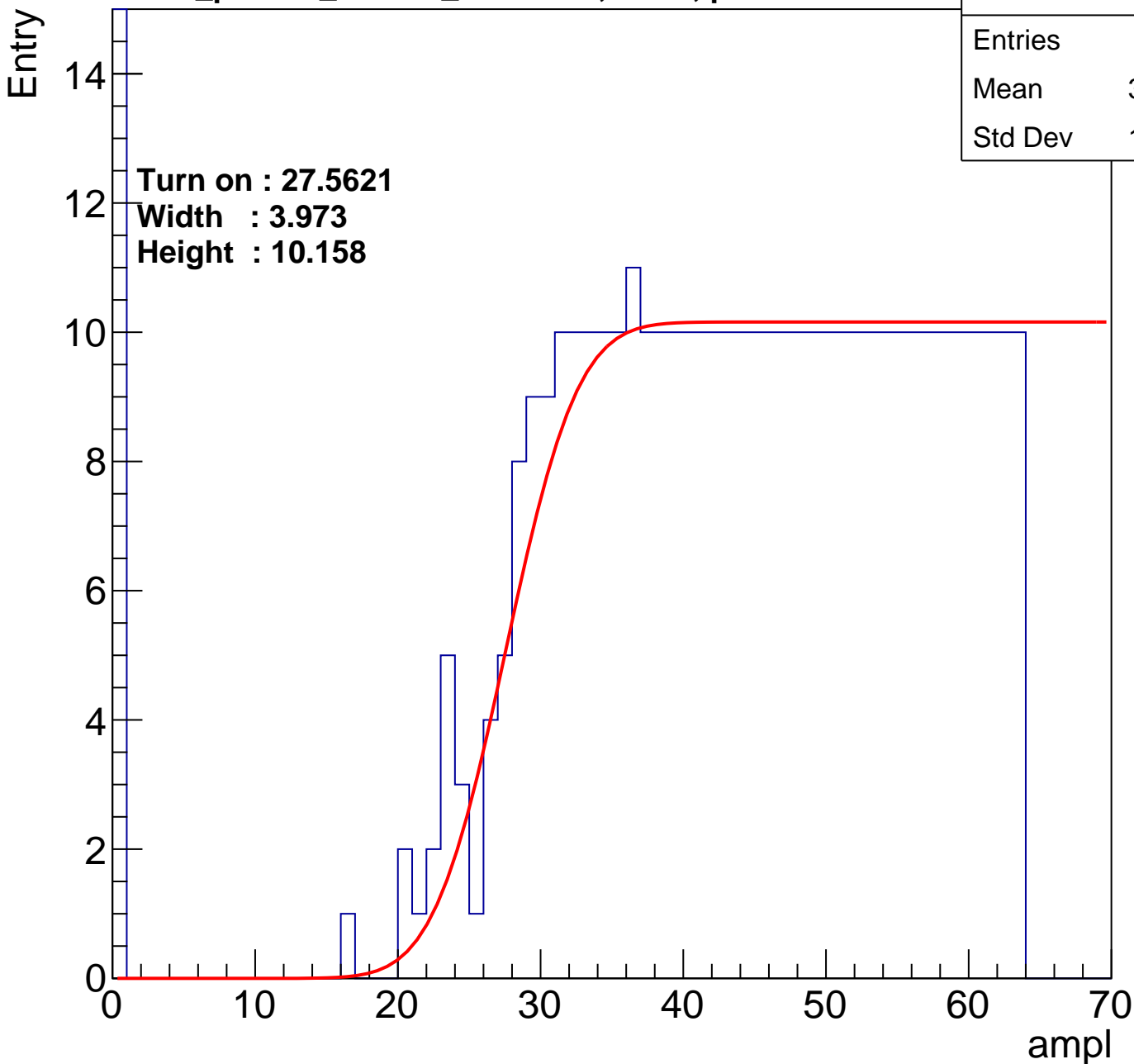
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	453
Mean	37.25
Std Dev	19.23

Turn on : 27.5621

Width : 3.973

Height : 10.158



# B1L103S, U4-ch124

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	481
Mean	36.48
Std Dev	18.95

**Turn on : 22.8673**

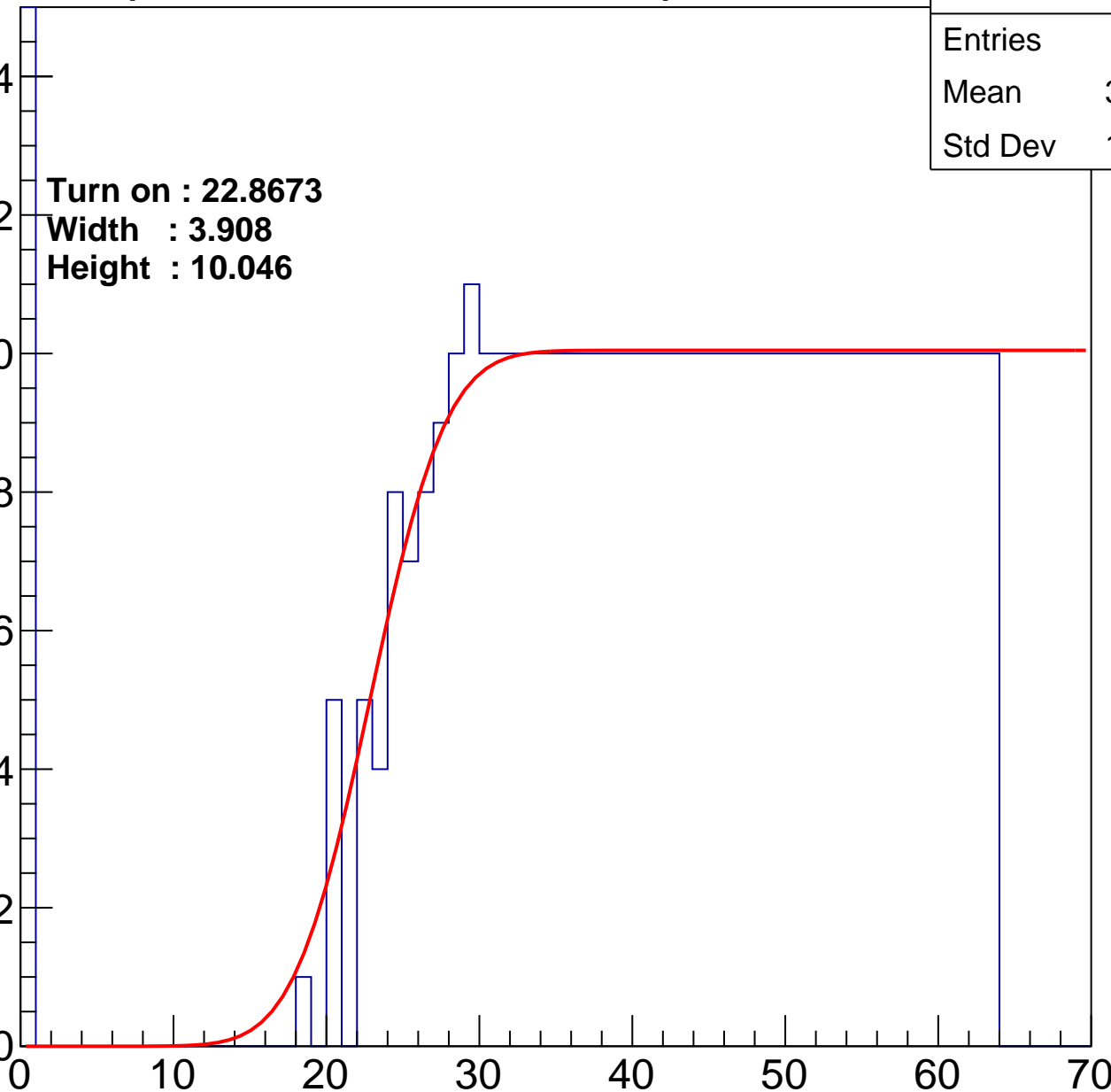
**Width : 3.908**

**Height : 10.046**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch125

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	408
Mean	40.85
Std Dev	16.43

**Turn on : 26.5750**

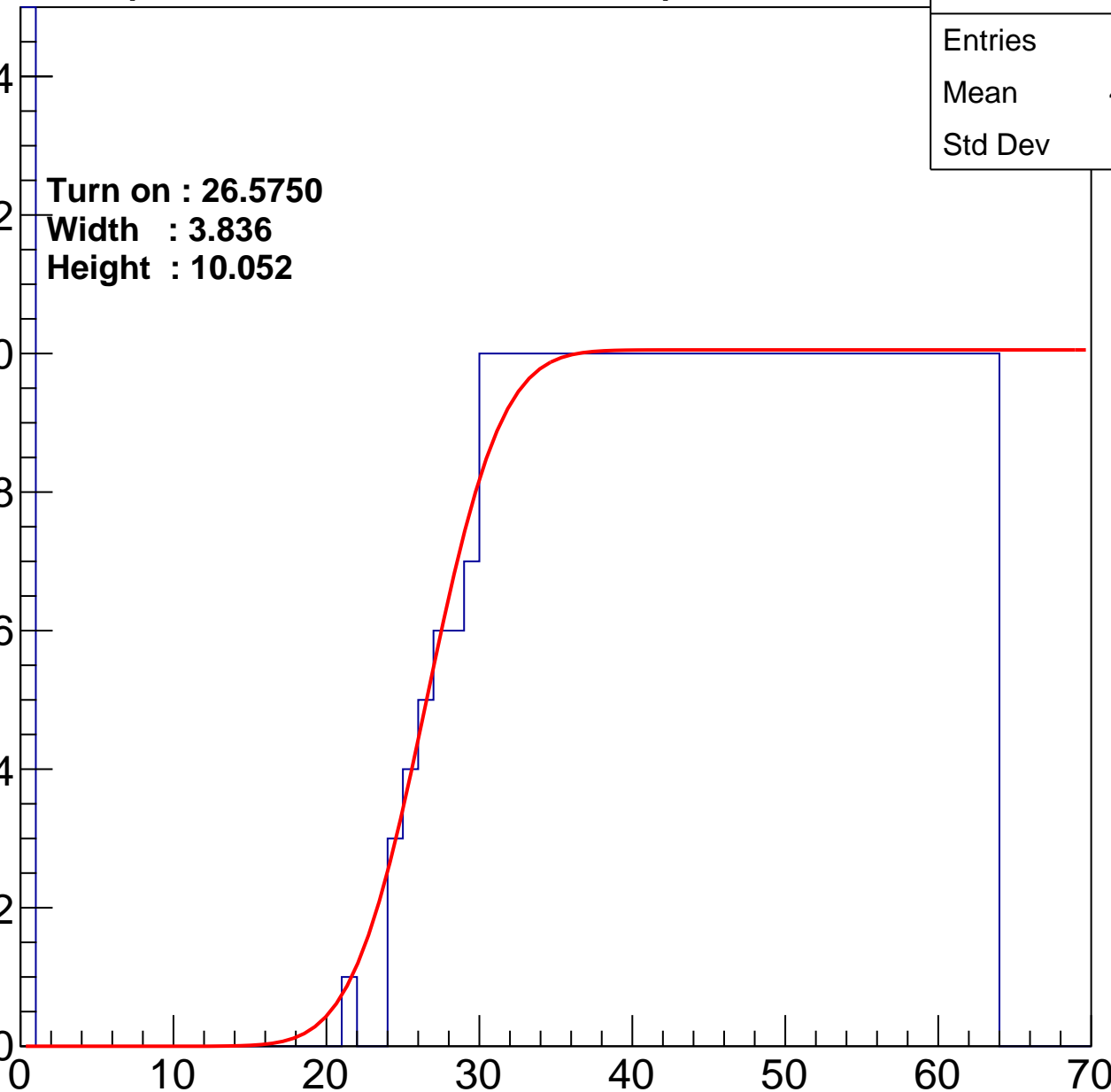
**Width : 3.836**

**Height : 10.052**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch126

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	471
Mean	37.05
Std Dev	18.62

**Turn on : 23.4829**

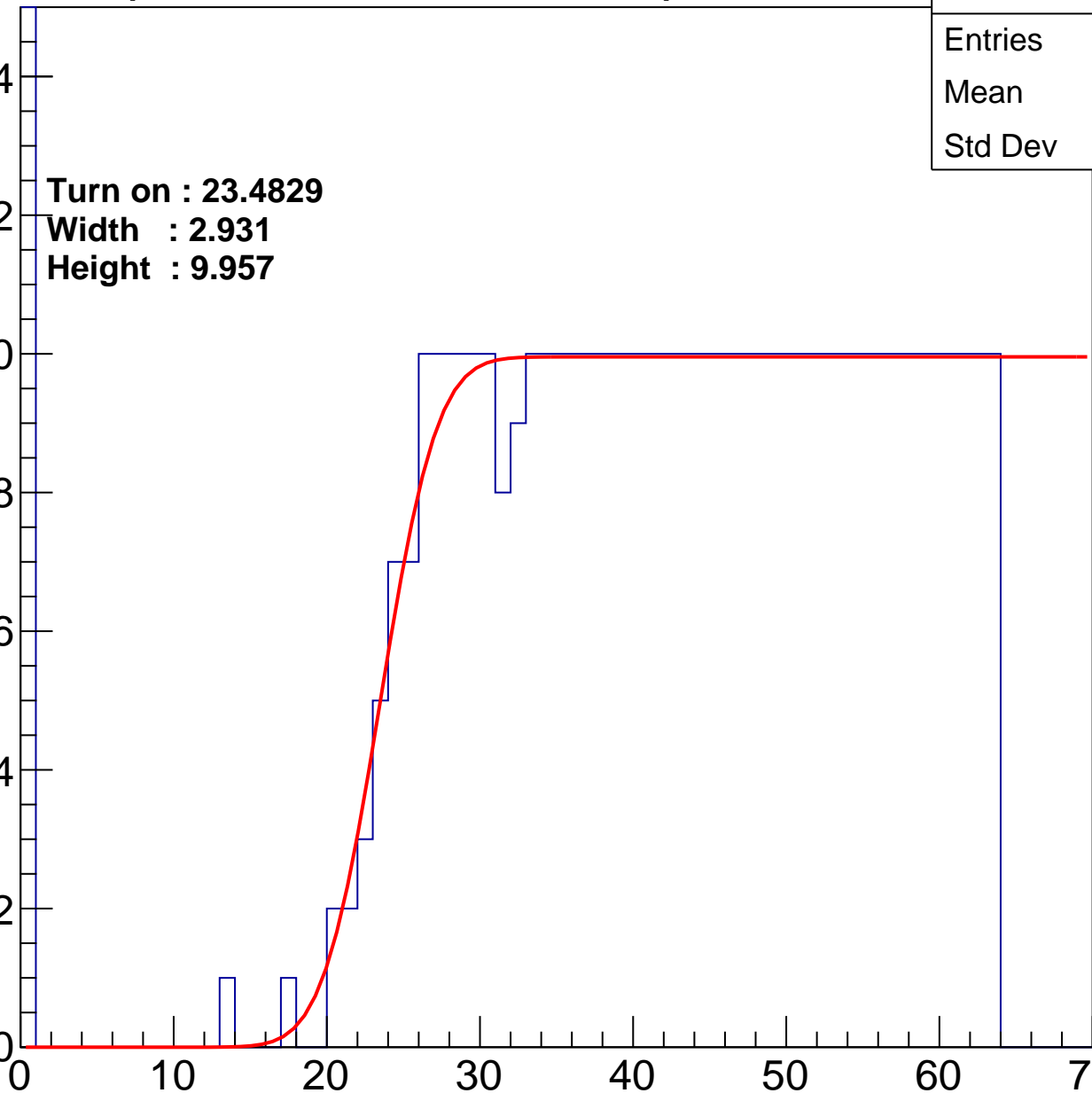
**Width : 2.931**

**Height : 9.957**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L103S, U4-ch127

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	432
Mean	39.44
Std Dev	17.23

Turn on : 25.3289

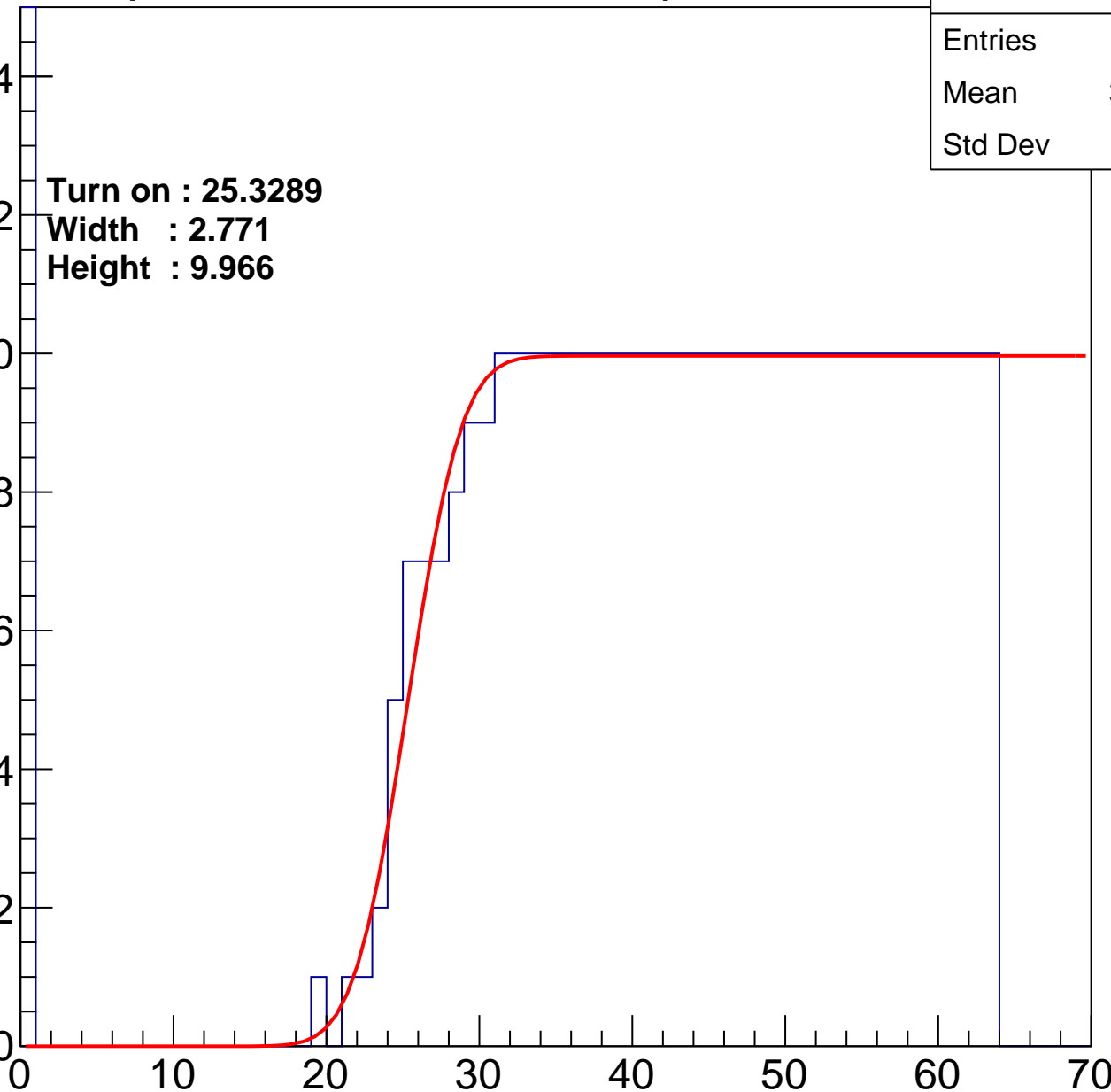
Width : 2.771

Height : 9.966

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch127

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	432
Mean	39.44
Std Dev	17.23

Turn on : 25.3289

Width : 2.771

Height : 9.966

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl

