

B1L003S, U2-ch0

calib_packv5_042523_0143.root, FC#13, port D2

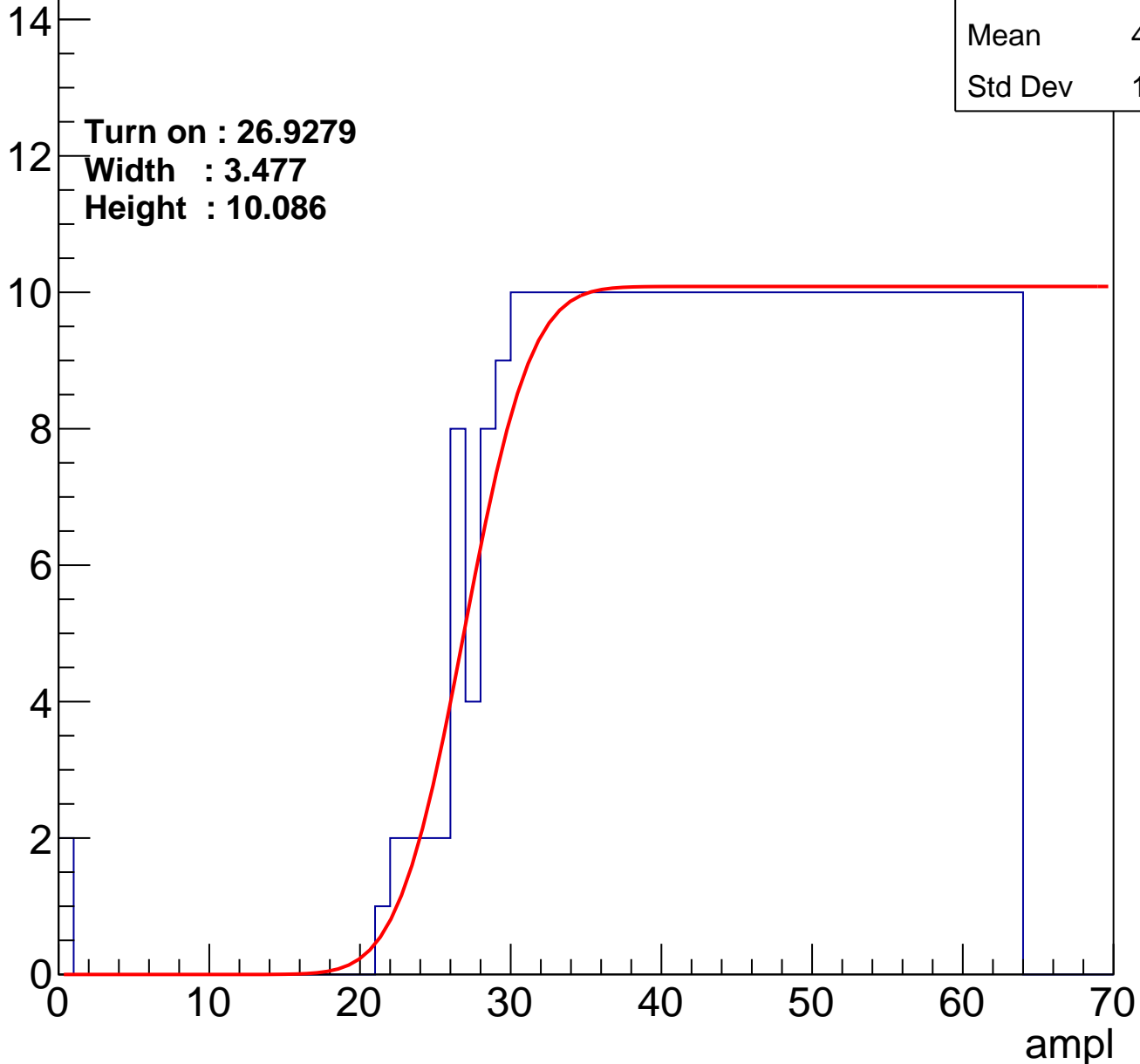
Entries	380
Mean	44.26
Std Dev	11.52

Turn on : 26.9279

Width : 3.477

Height : 10.086

Entry



B1L003S, U2-ch1

calib_packv5_042523_0143.root, FC#13, port D2

Entries	364
Mean	44.93
Std Dev	11.39

Turn on : 28.3200

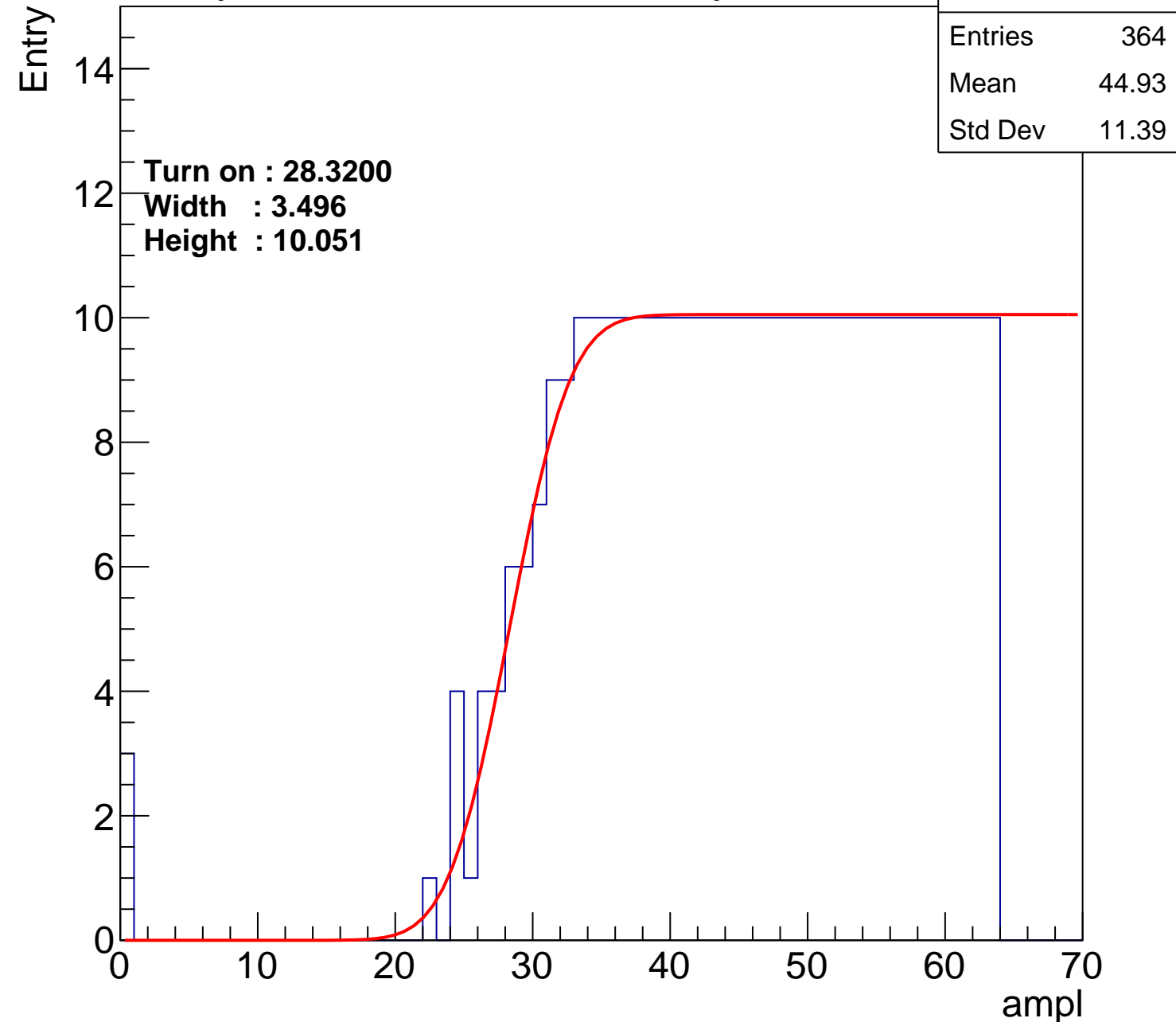
Width : 3.496

Height : 10.051

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch2

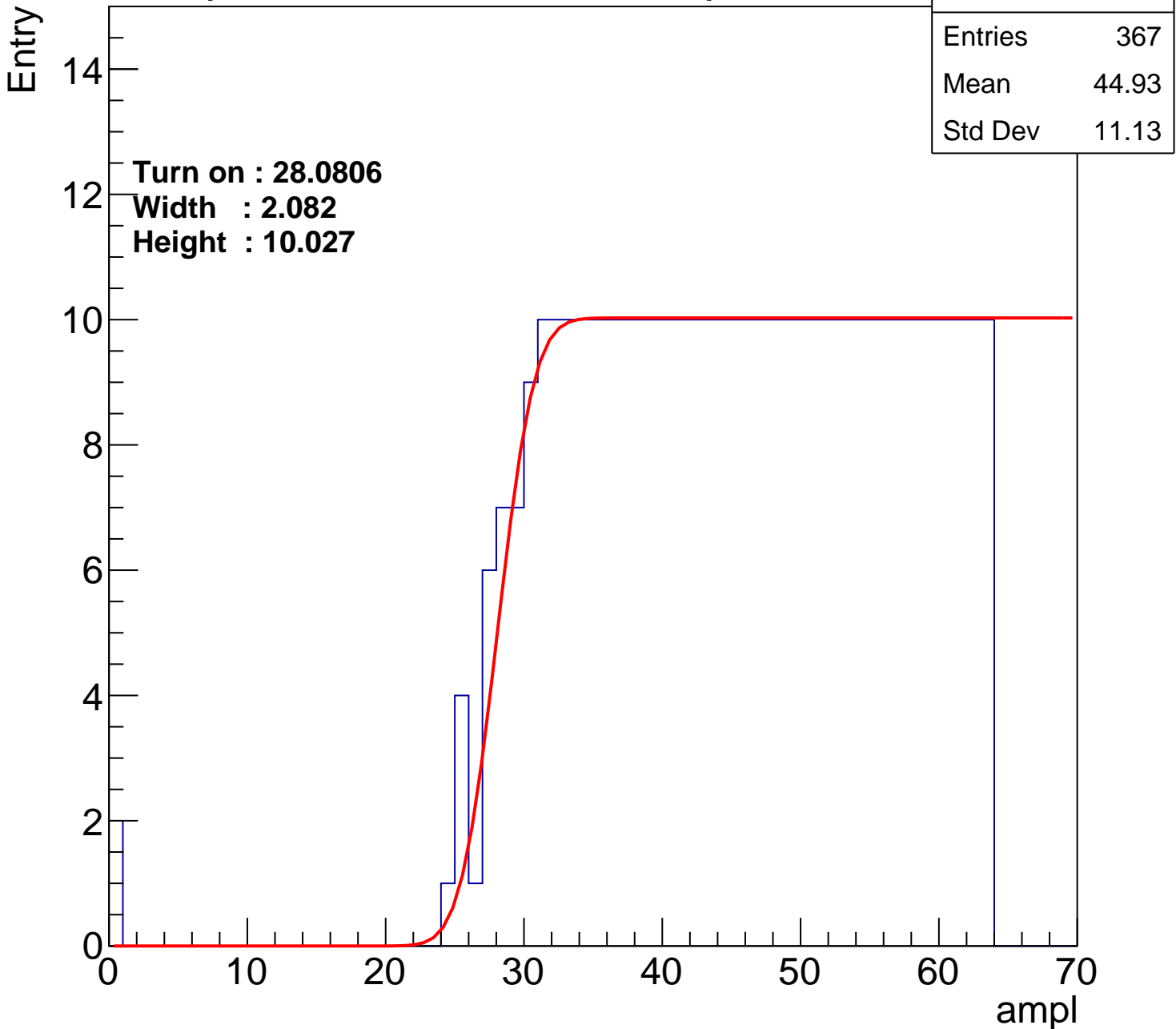
calib_packv5_042523_0143.root, FC#13, port D2

Entries	367
Mean	44.93
Std Dev	11.13

Turn on : 28.0806

Width : 2.082

Height : 10.027



B1L003S, U2-ch3

calib_packv5_042523_0143.root, FC#13, port D2

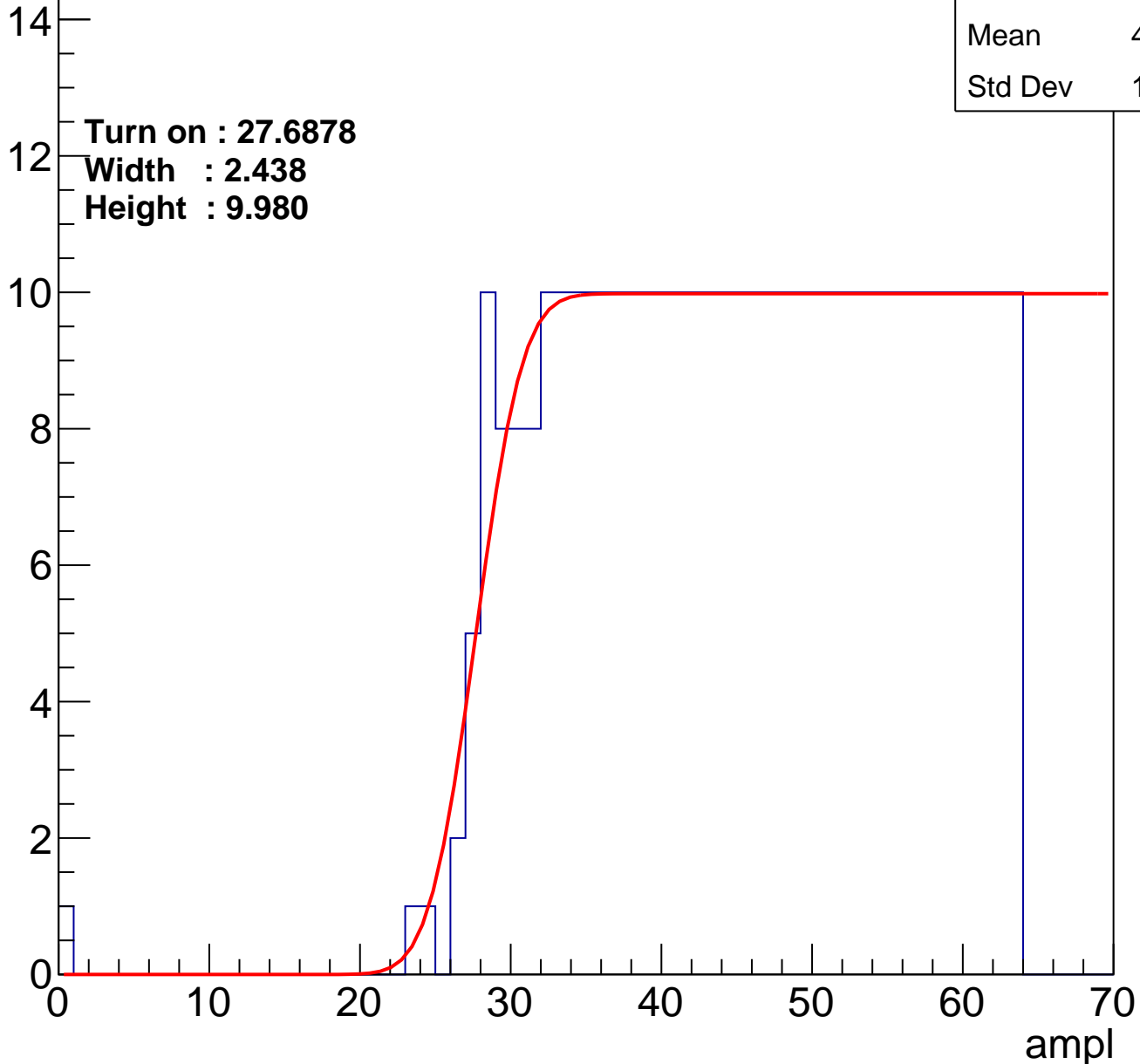
Entries	364
Mean	45.15
Std Dev	10.85

Turn on : 27.6878

Width : 2.438

Height : 9.980

Entry



B1L003S, U2-ch4

calib_packv5_042523_0143.root, FC#13, port D2

Entries	375
Mean	44.41
Std Dev	11.71

Turn on : 27.0791

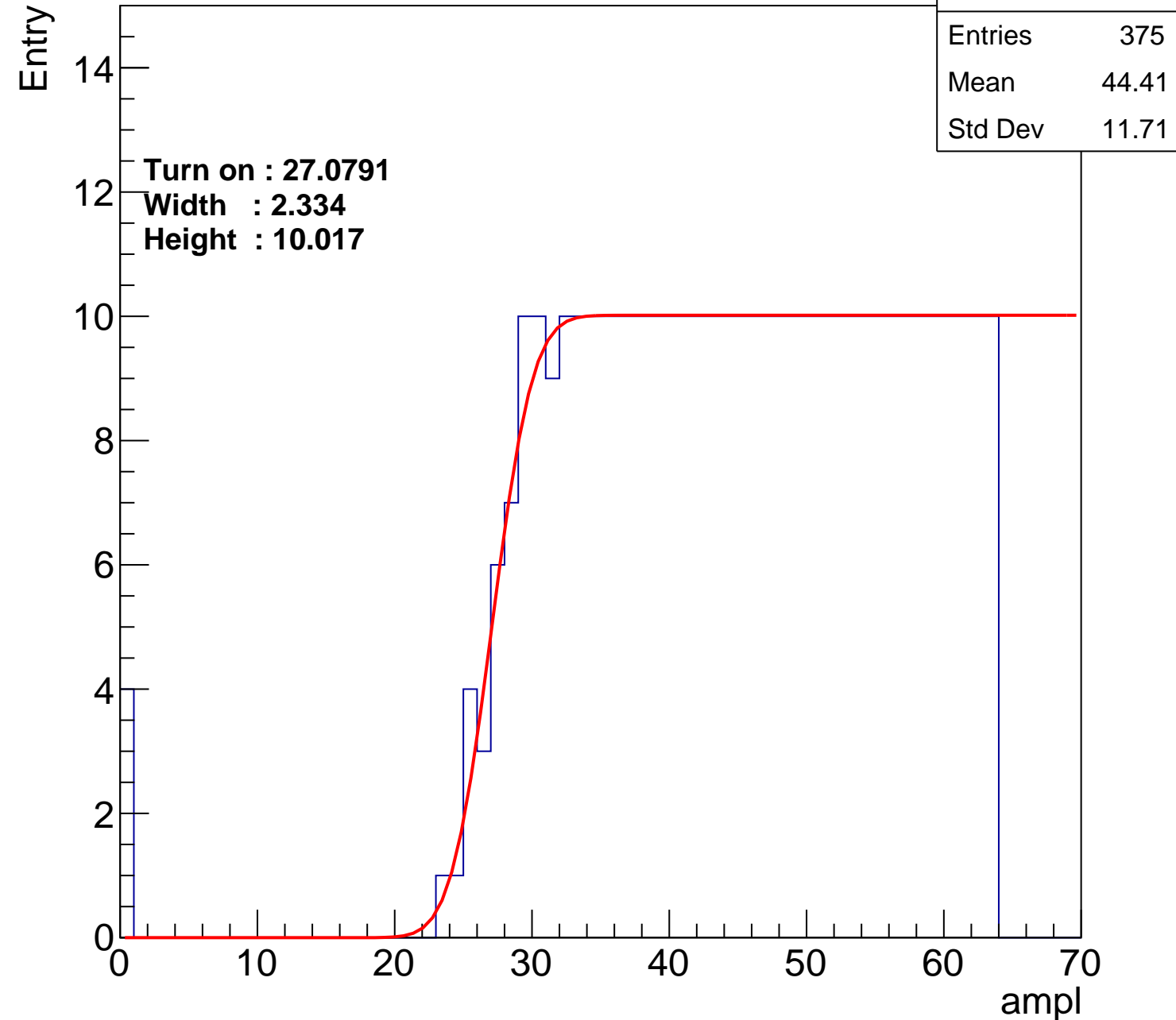
Width : 2.334

Height : 10.017

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch5

calib_packv5_042523_0143.root, FC#13, port D2

Entries	371
Mean	44.8
Std Dev	11.04

Turn on : 27.0087

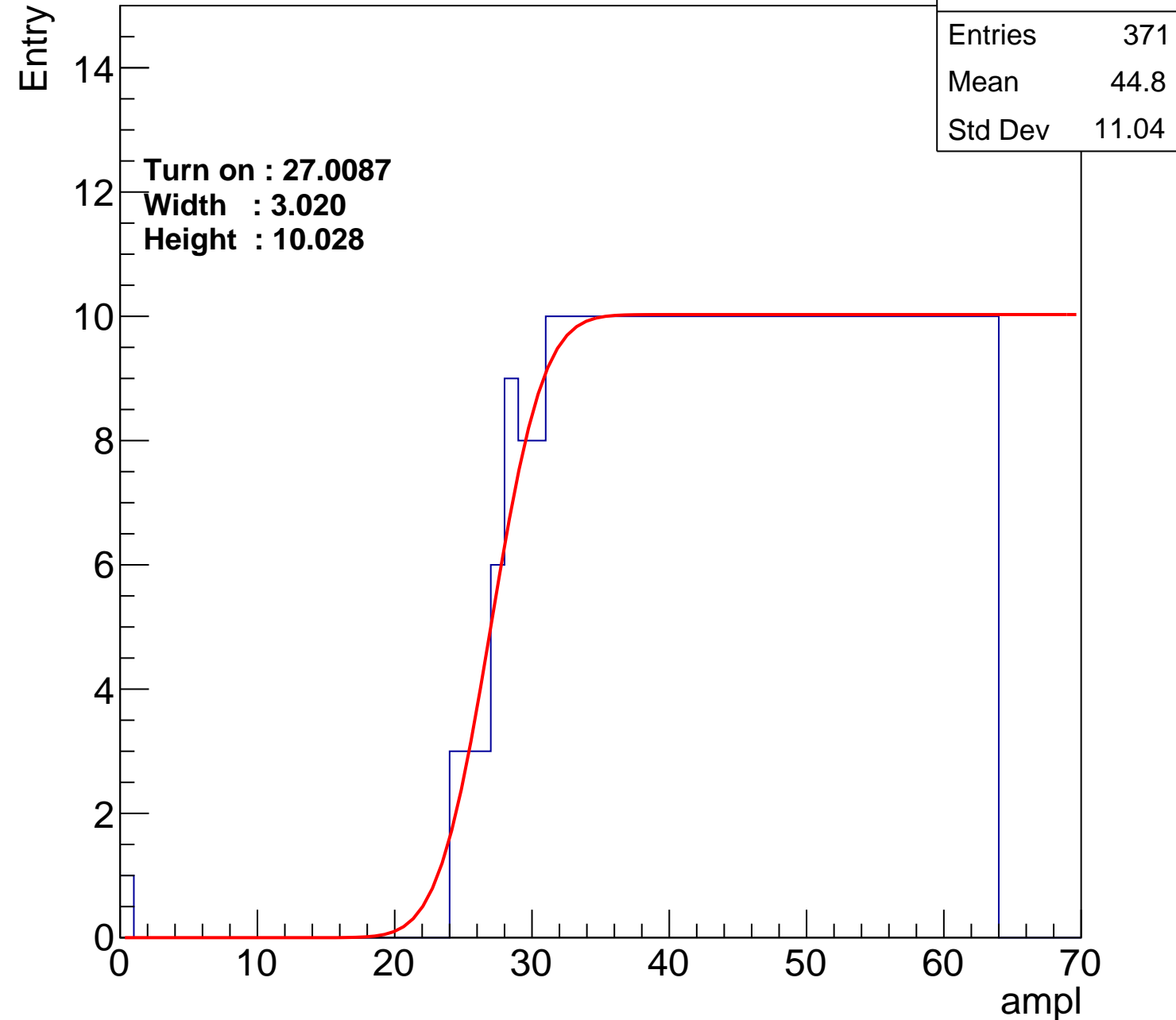
Width : 3.020

Height : 10.028

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch6

calib_packv5_042523_0143.root, FC#13, port D2

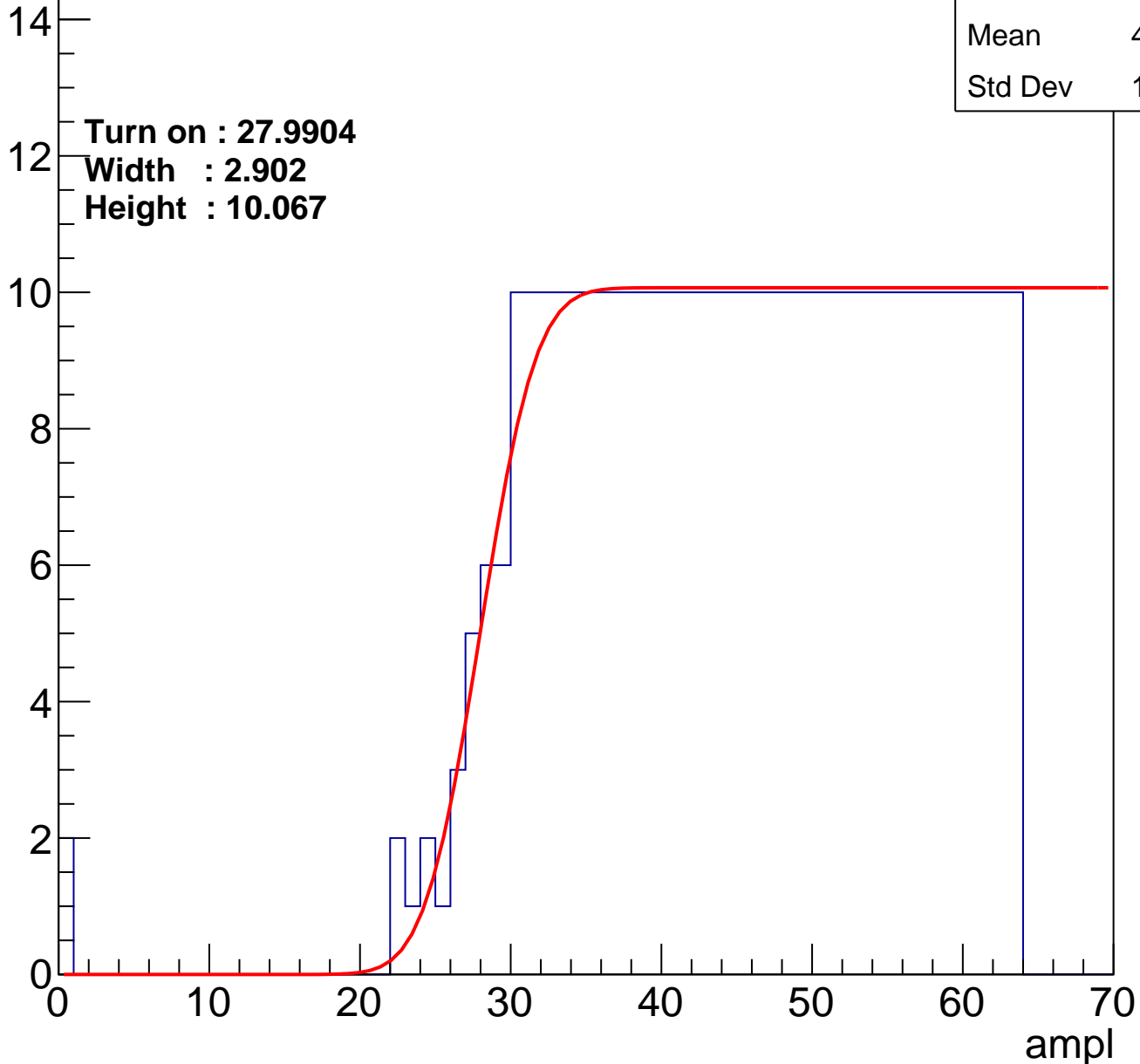
Entries	368
Mean	44.85
Std Dev	11.22

Turn on : 27.9904

Width : 2.902

Height : 10.067

Entry



B1L003S, U2-ch7

calib_packv5_042523_0143.root, FC#13, port D2

Entries	388
Mean	43.81
Std Dev	11.88

Turn on : 25.3774

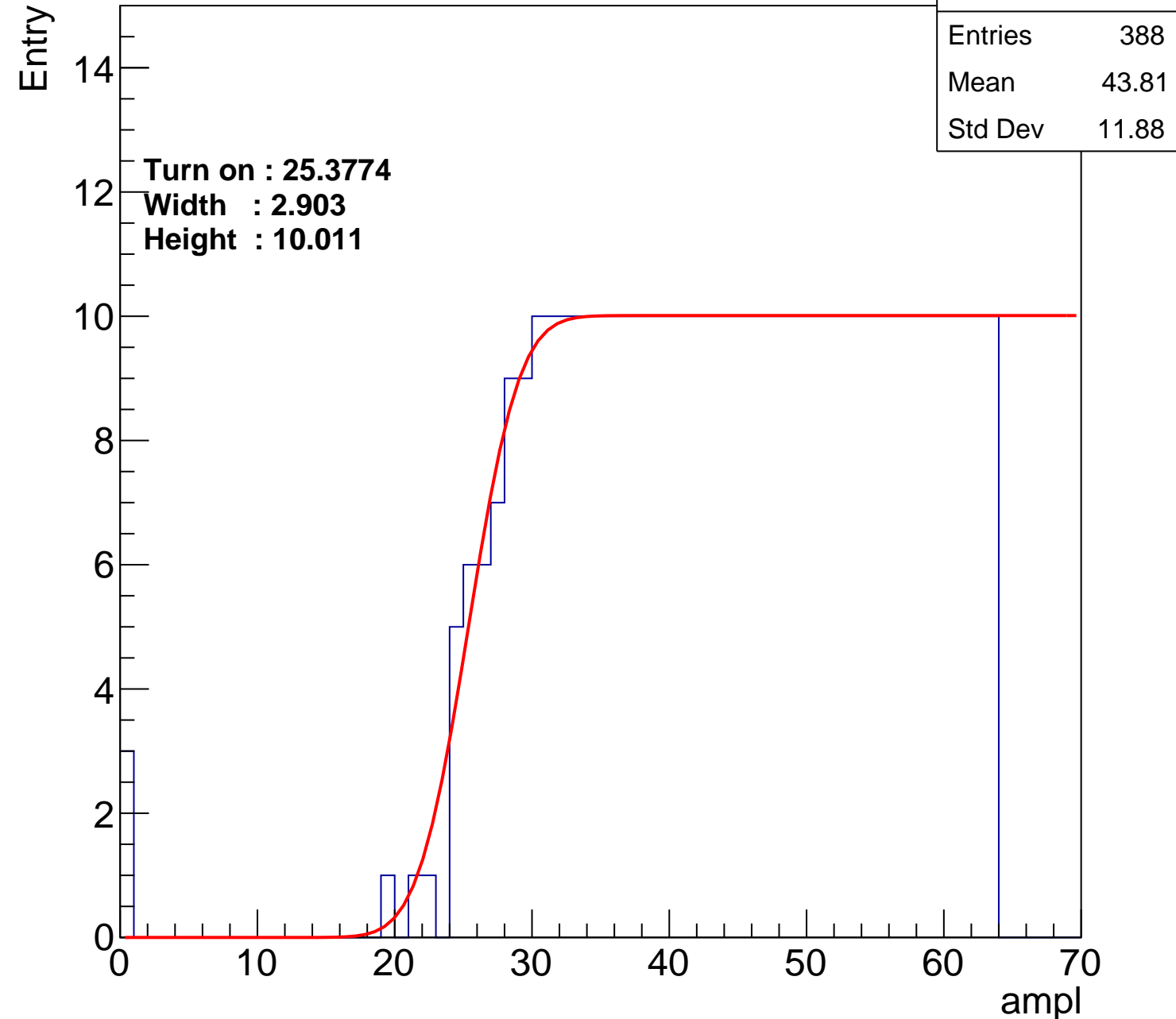
Width : 2.903

Height : 10.011

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch8

calib_packv5_042523_0143.root, FC#13, port D2

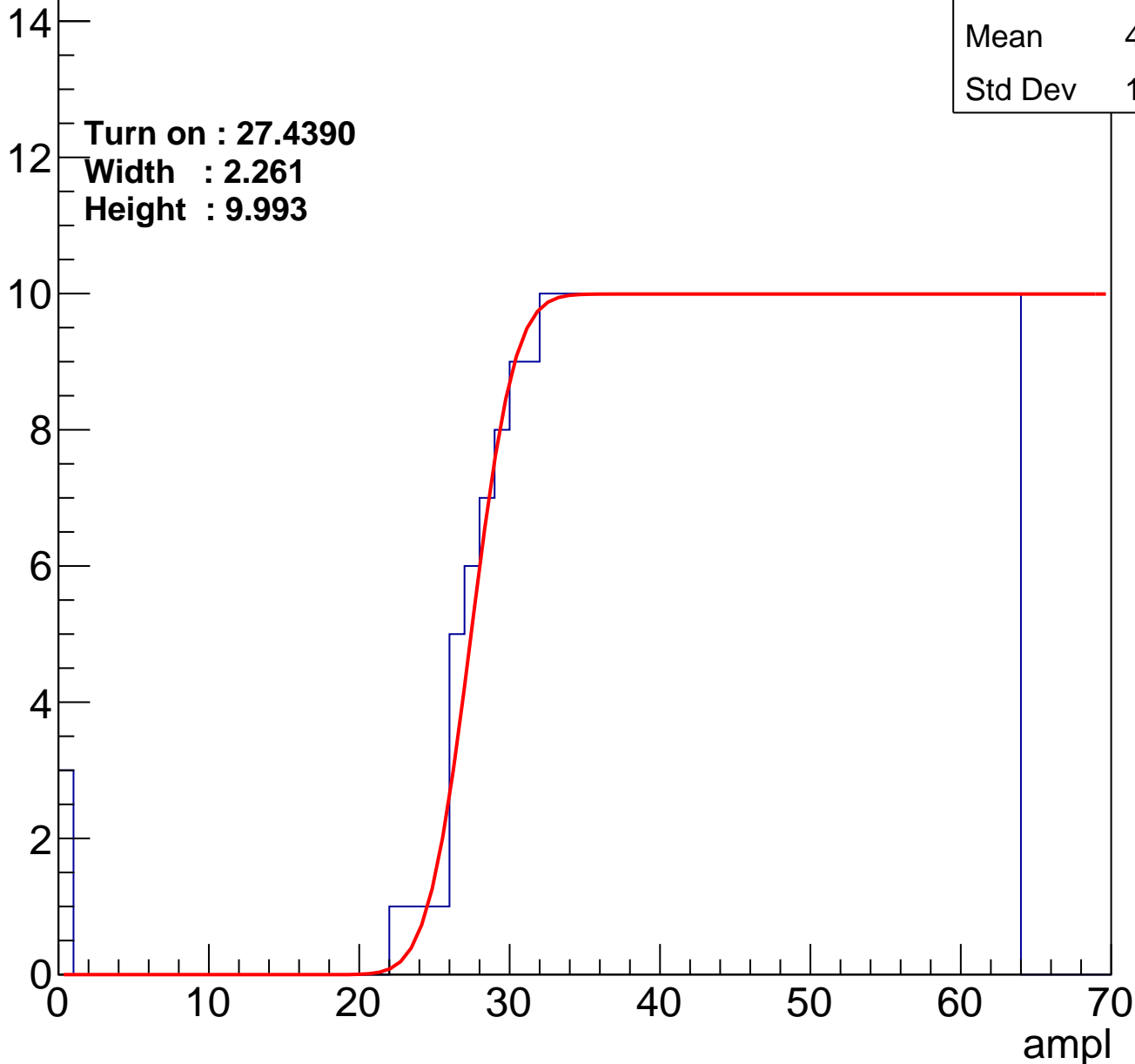
Entry

Entries	371
Mean	44.64
Std Dev	11.47

Turn on : 27.4390

Width : 2.261

Height : 9.993



B1L003S, U2-ch9

calib_packv5_042523_0143.root, FC#13, port D2

Entries	379
Mean	44.28
Std Dev	11.54

Turn on : 26.4775

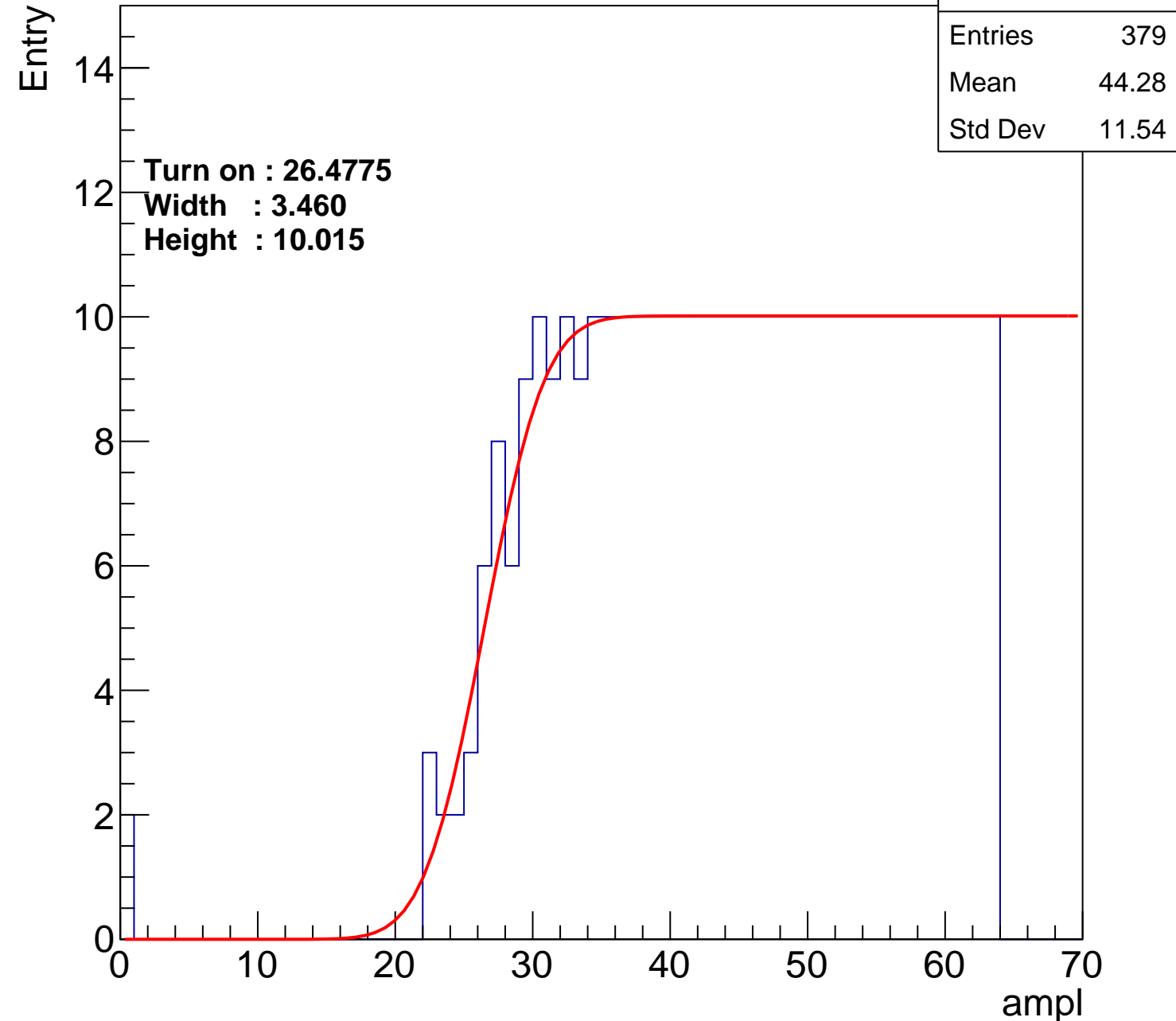
Width : 3.460

Height : 10.015

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch10

calib_packv5_042523_0143.root, FC#13, port D2

Entries	353
Mean	45.5
Std Dev	11.07

Turn on : 28.8707

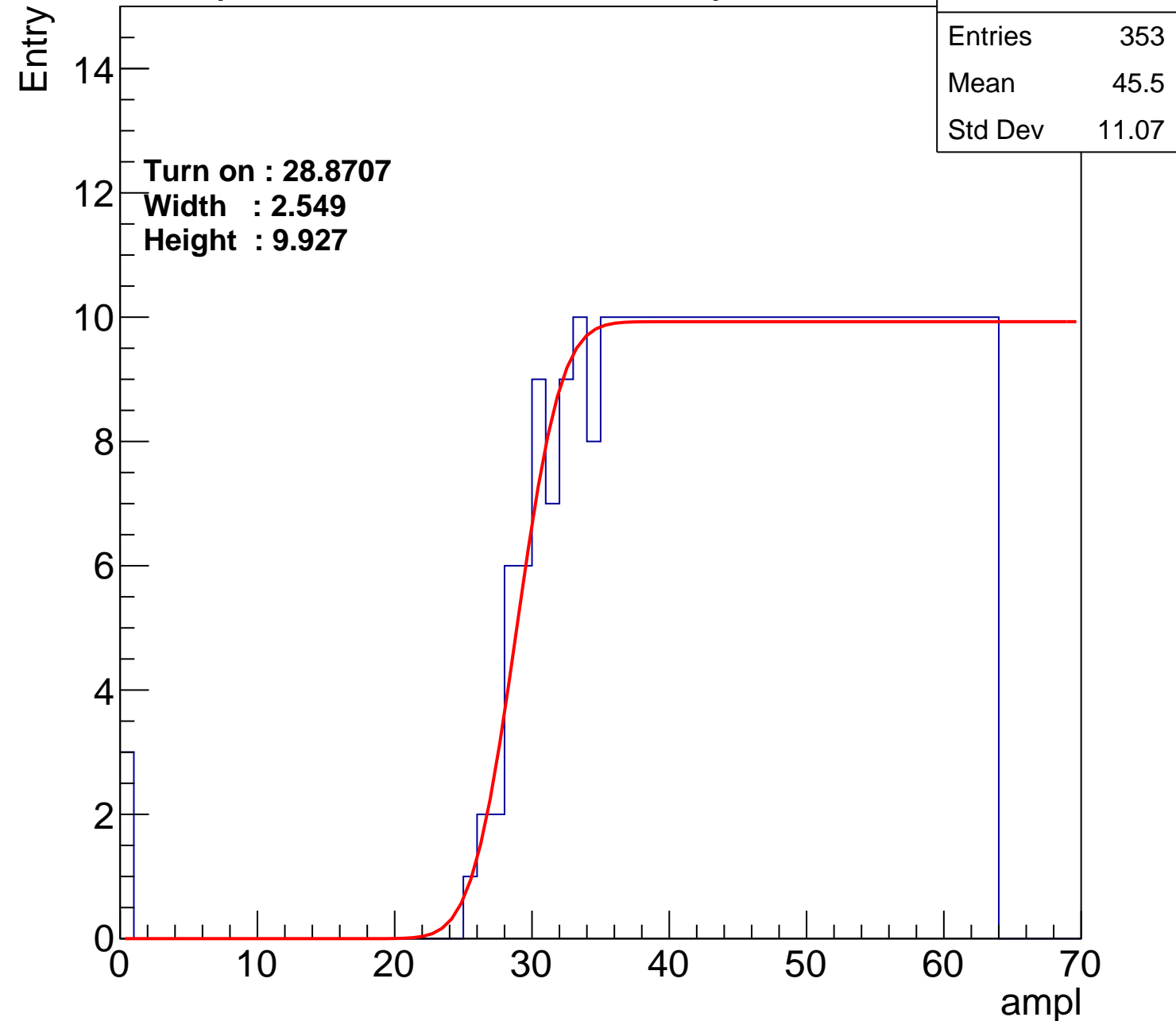
Width : 2.549

Height : 9.927

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch11

calib_packv5_042523_0143.root, FC#13, port D2

Entries	368
Mean	44.81
Std Dev	11.37

Turn on : 28.2124

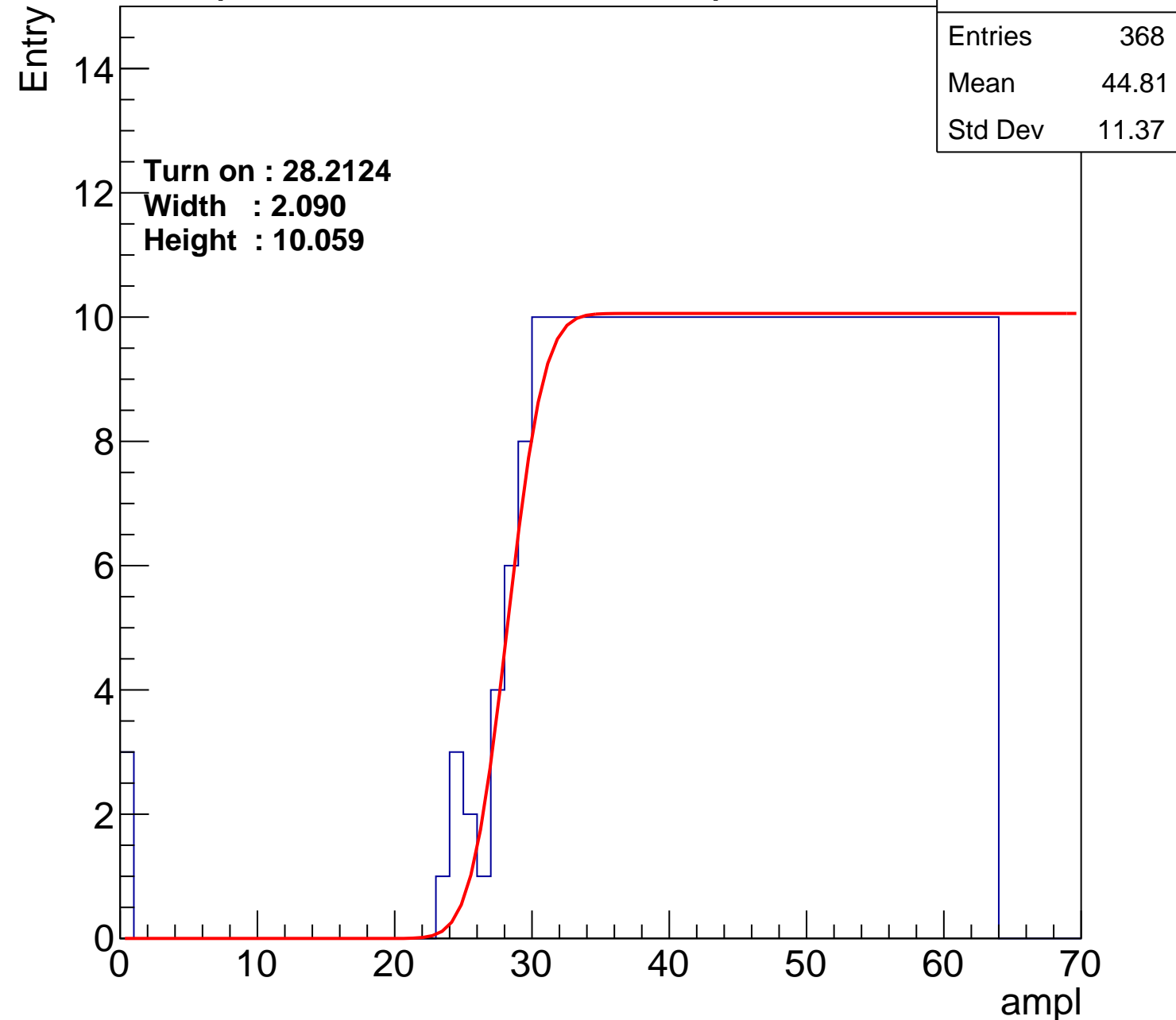
Width : 2.090

Height : 10.059

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch12

calib_packv5_042523_0143.root, FC#13, port D2

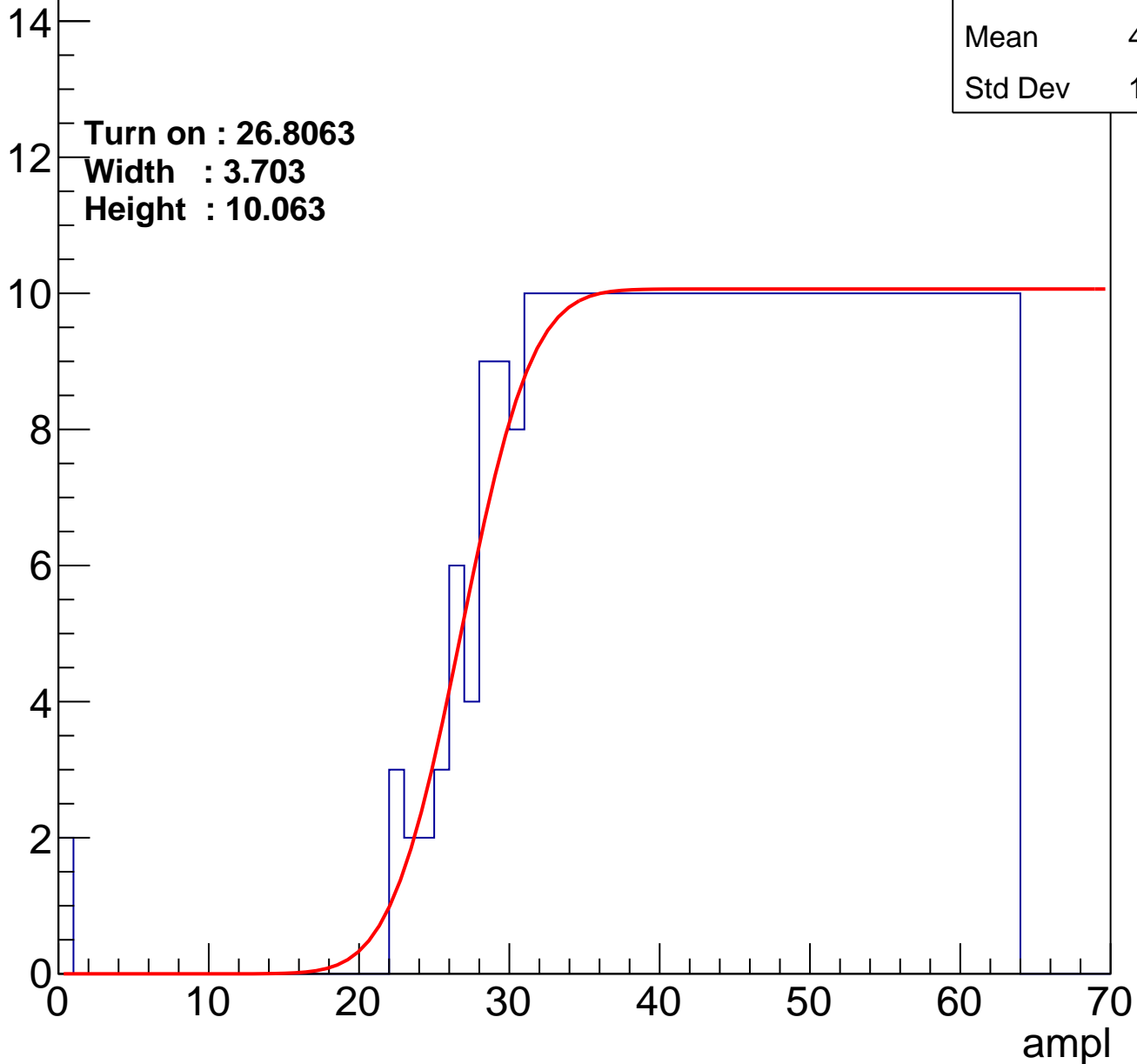
Entries	378
Mean	44.34
Std Dev	11.49

Turn on : 26.8063

Width : 3.703

Height : 10.063

Entry



B1L003S, U2-ch13

calib_packv5_042523_0143.root, FC#13, port D2

Entries	352
Mean	45.62
Std Dev	10.83

Turn on : 29.2766

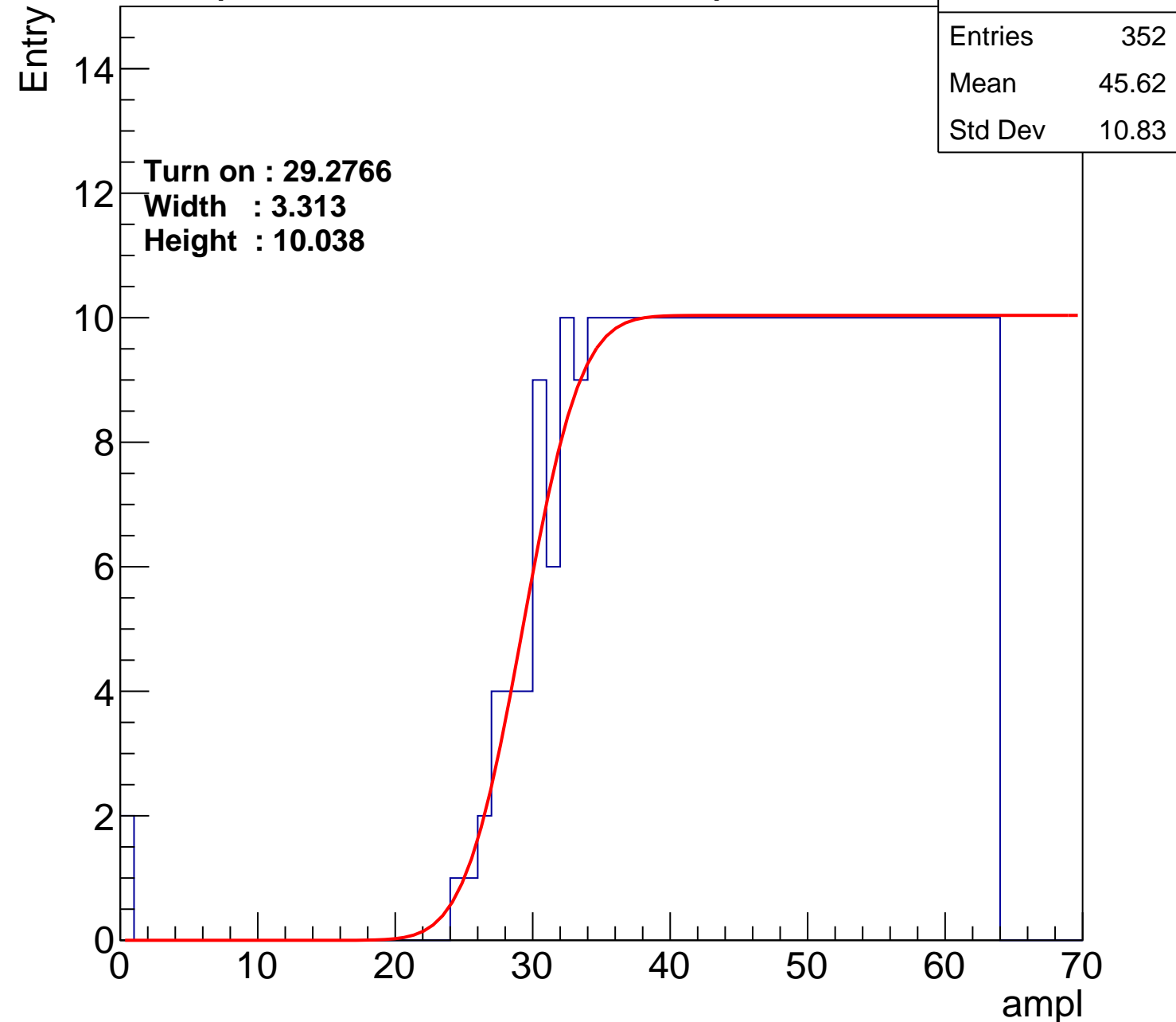
Width : 3.313

Height : 10.038

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch14

calib_packv5_042523_0143.root, FC#13, port D2

Entries	362
Mean	45.21
Std Dev	10.86

Turn on : 27.4613

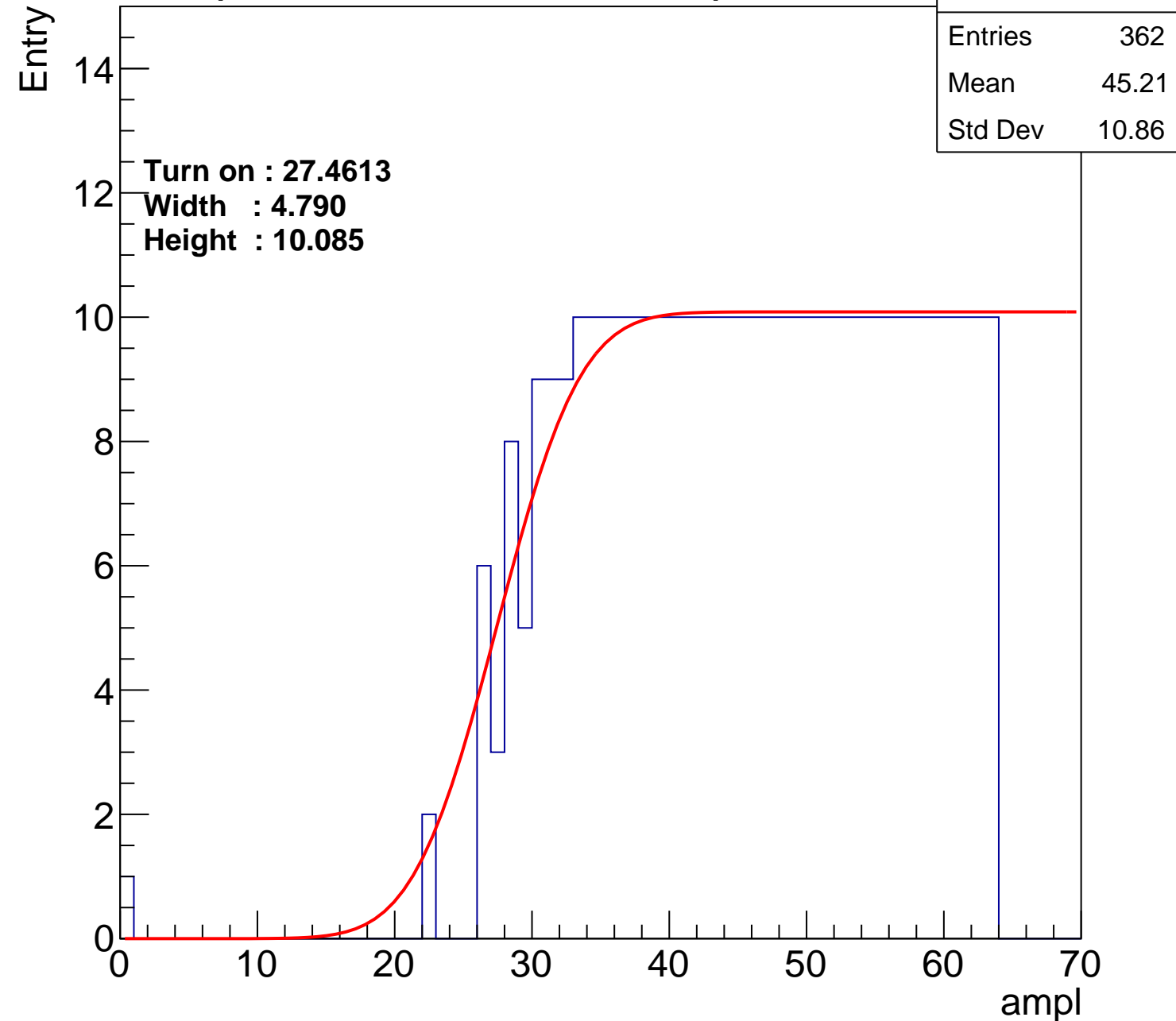
Width : 4.790

Height : 10.085

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch15

calib_packv5_042523_0143.root, FC#13, port D2

Entries	369
Mean	44.92
Std Dev	10.96

Turn on : 26.5056

Width : 3.286

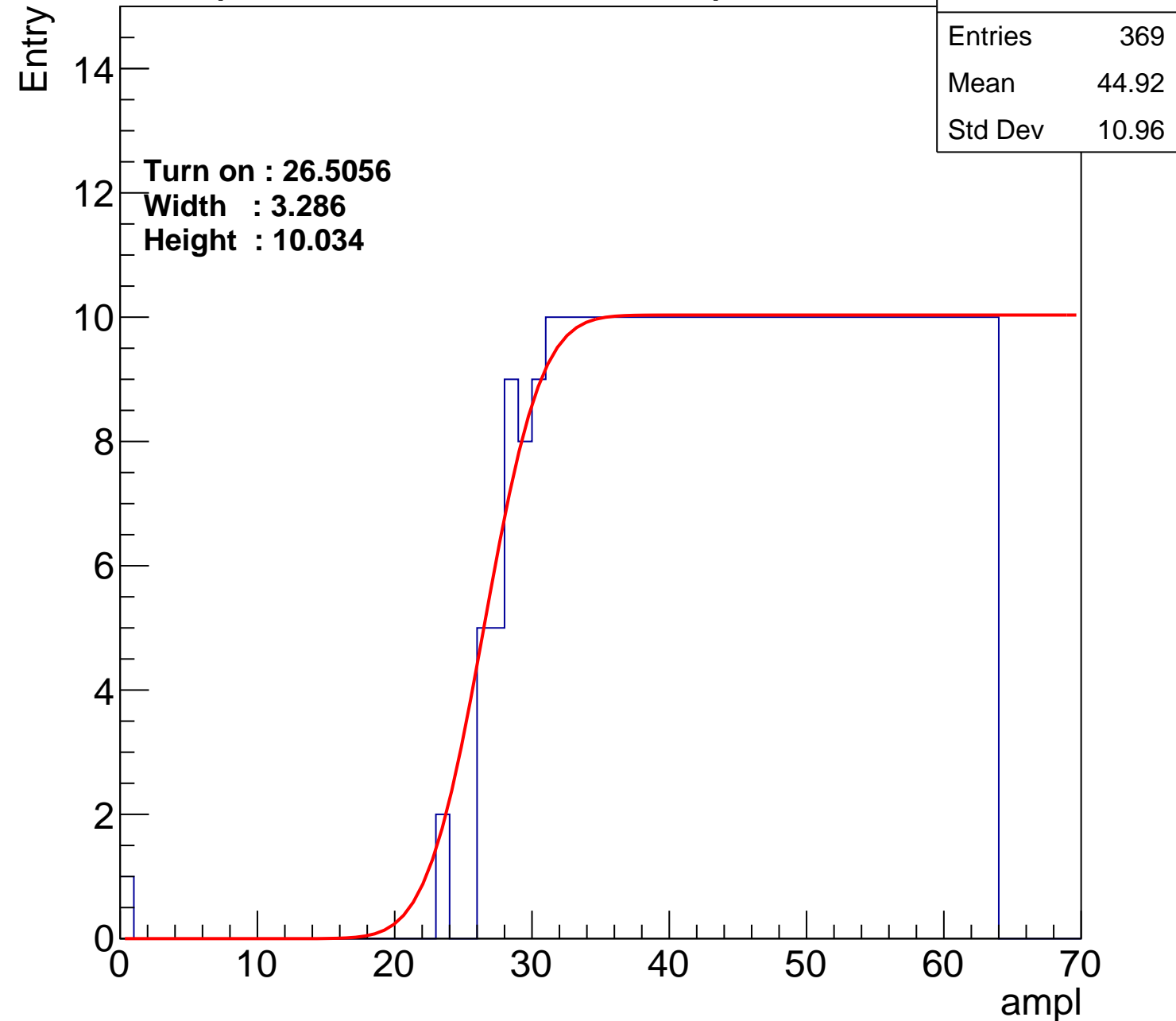
Height : 10.034

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L003S, U2-ch16

calib_packv5_042523_0143.root, FC#13, port D2

Entries	362
Mean	45.16
Std Dev	11.04

Turn on : 28.3745

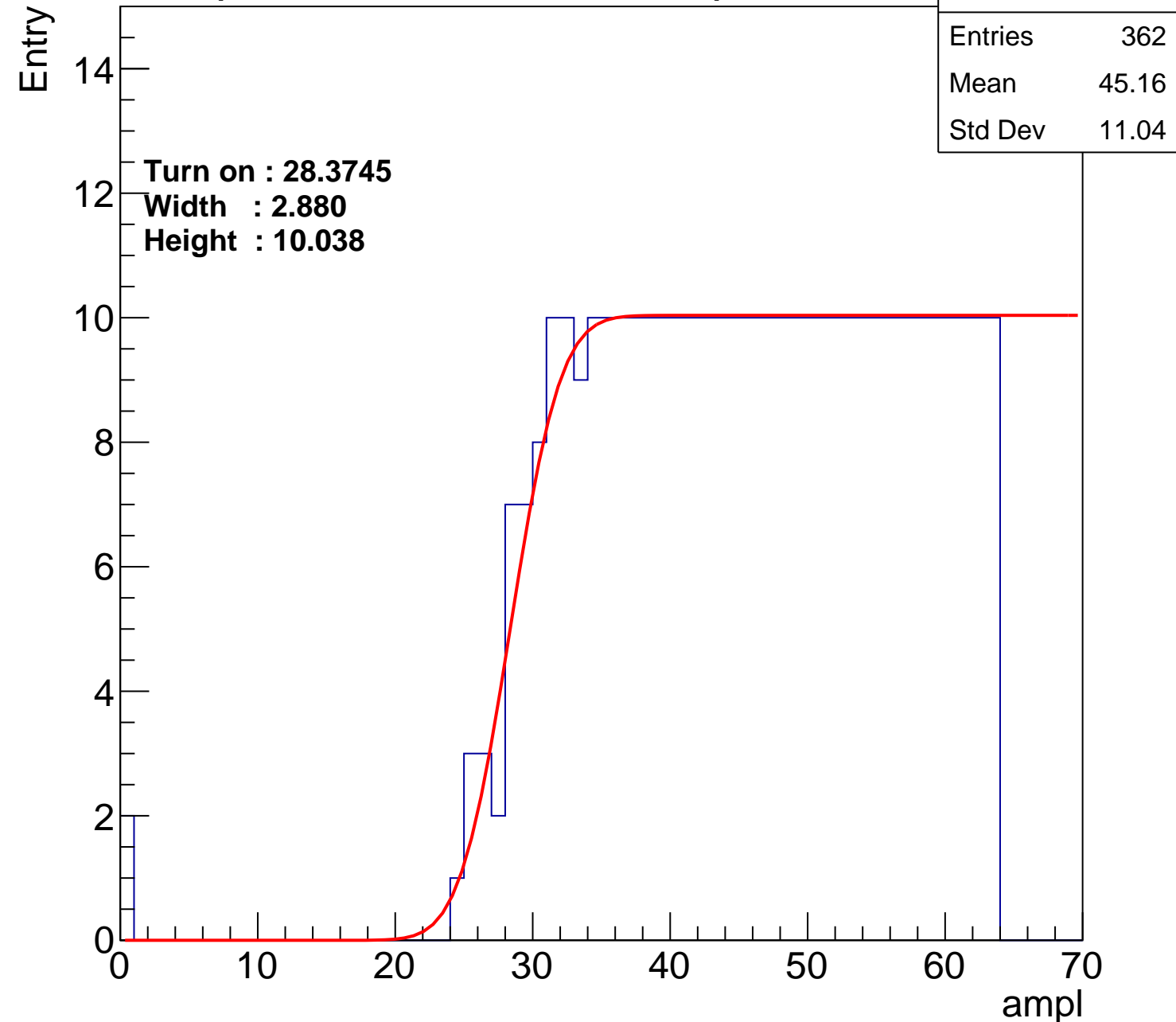
Width : 2.880

Height : 10.038

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch17

calib_packv5_042523_0143.root, FC#13, port D2

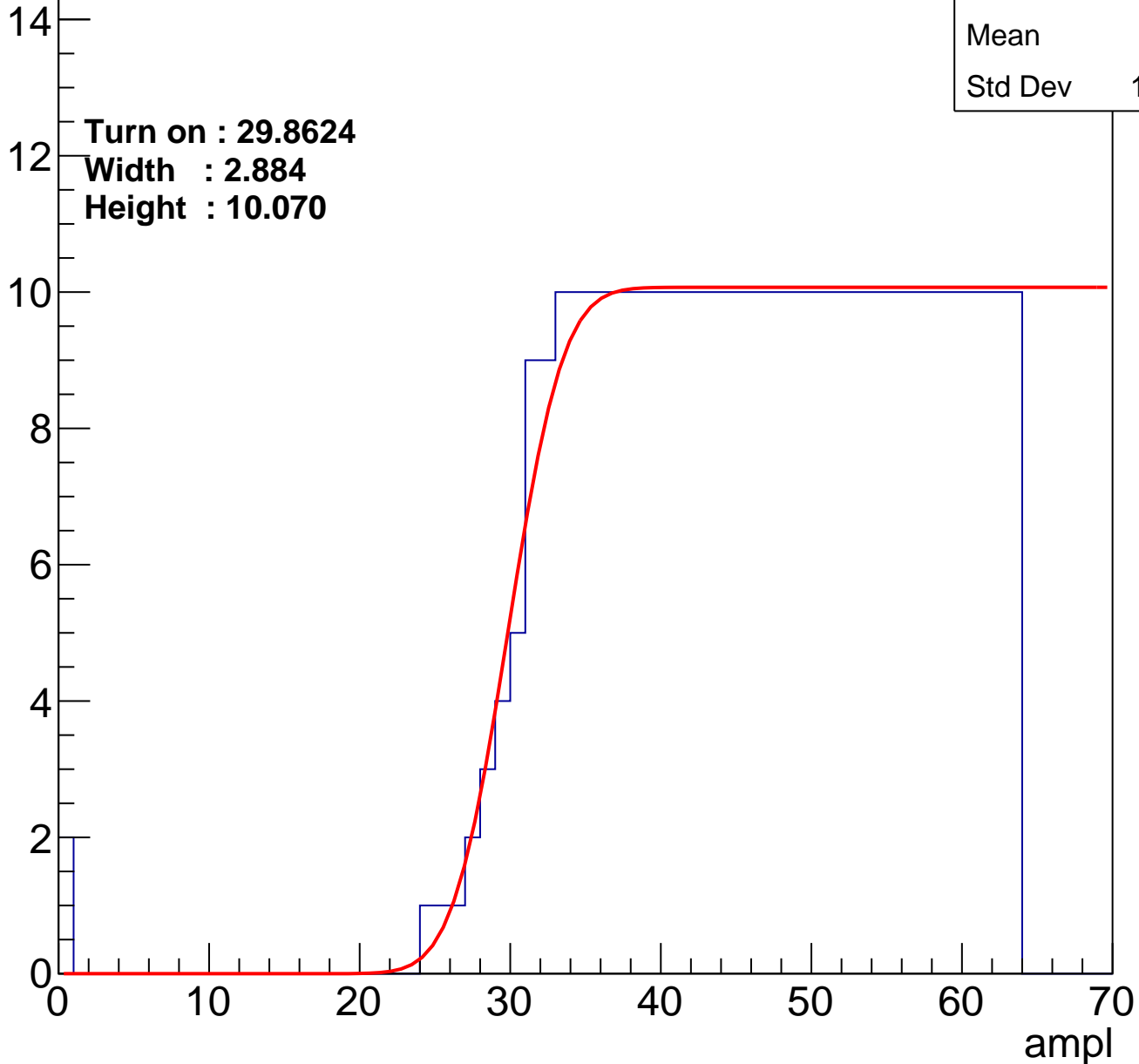
Entries	347
Mean	45.9
Std Dev	10.67

Turn on : 29.8624

Width : 2.884

Height : 10.070

Entry



B1L003S, U2-ch18

calib_packv5_042523_0143.root, FC#13, port D2

Entries	380
Mean	44.36
Std Dev	11.29

Turn on : 26.4201

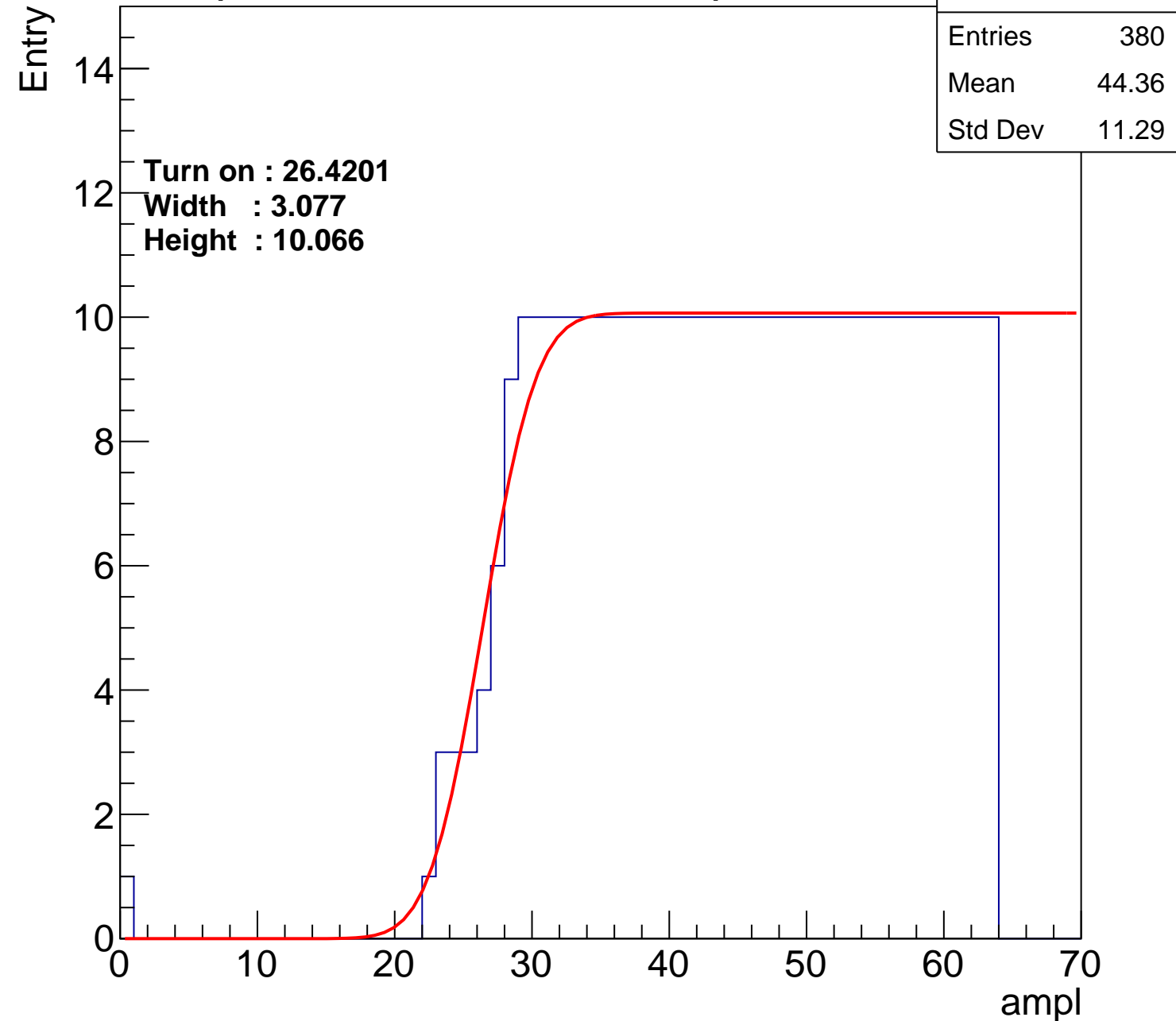
Width : 3.077

Height : 10.066

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch19

calib_packv5_042523_0143.root, FC#13, port D2

Entries	364
Mean	44.99
Std Dev	11.29

Turn on : 28.0978

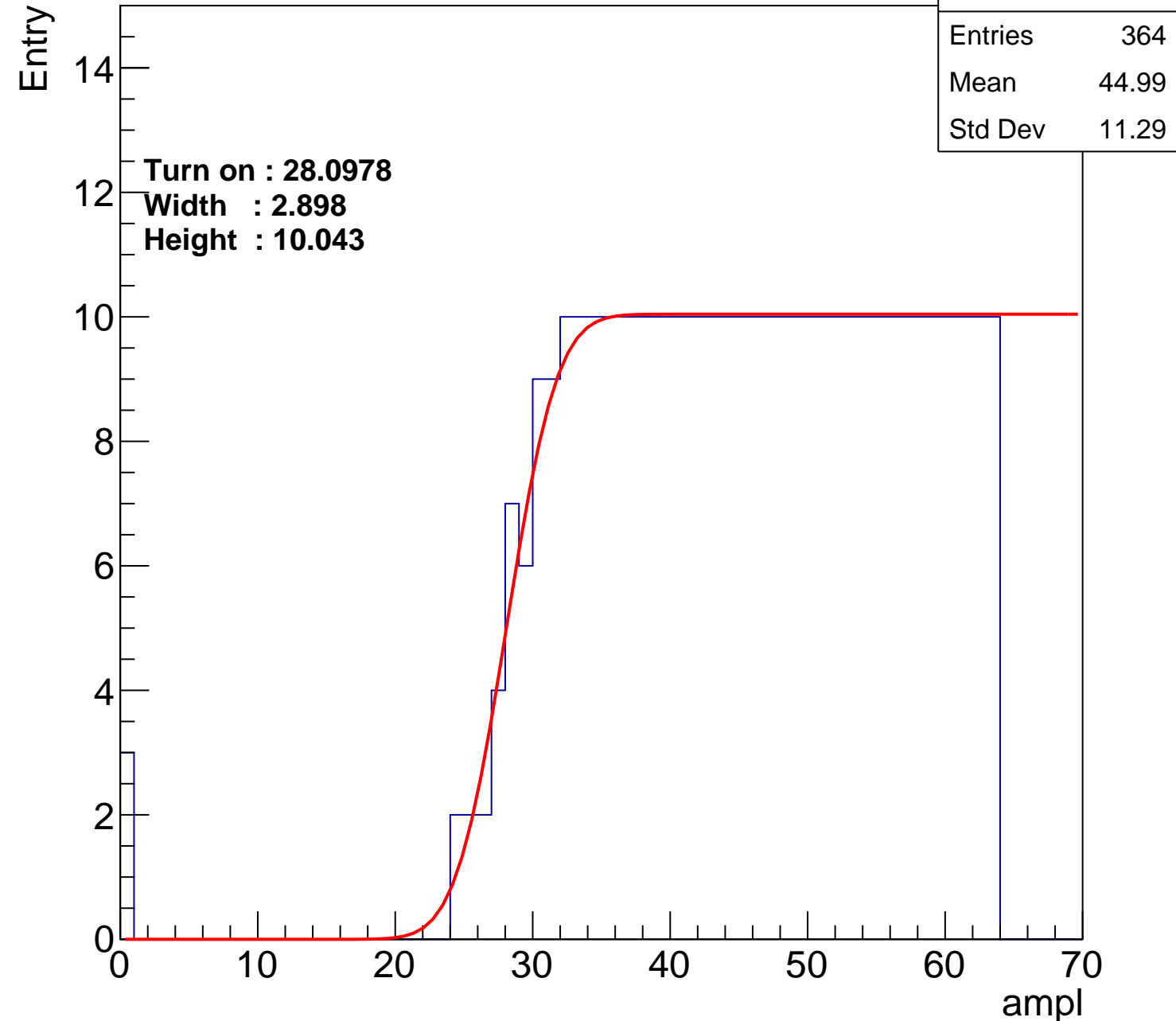
Width : 2.898

Height : 10.043

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch20

calib_packv5_042523_0143.root, FC#13, port D2

Entries	355
Mean	45.38
Std Dev	11.16

Turn on : 29.0387

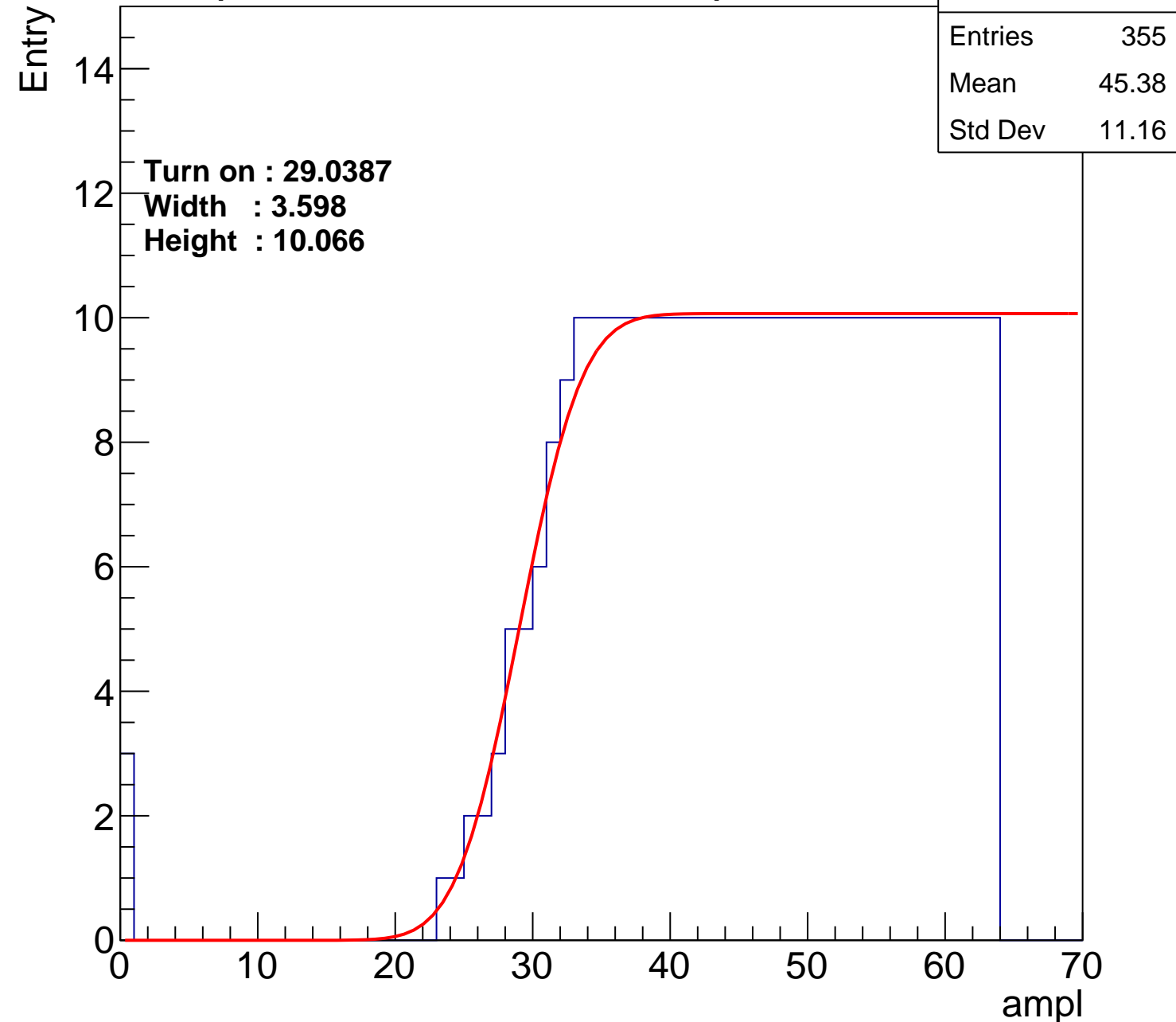
Width : 3.598

Height : 10.066

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch21

calib_packv5_042523_0143.root, FC#13, port D2

Entries	372
Mean	44.63
Std Dev	11.34

Turn on : 27.0588

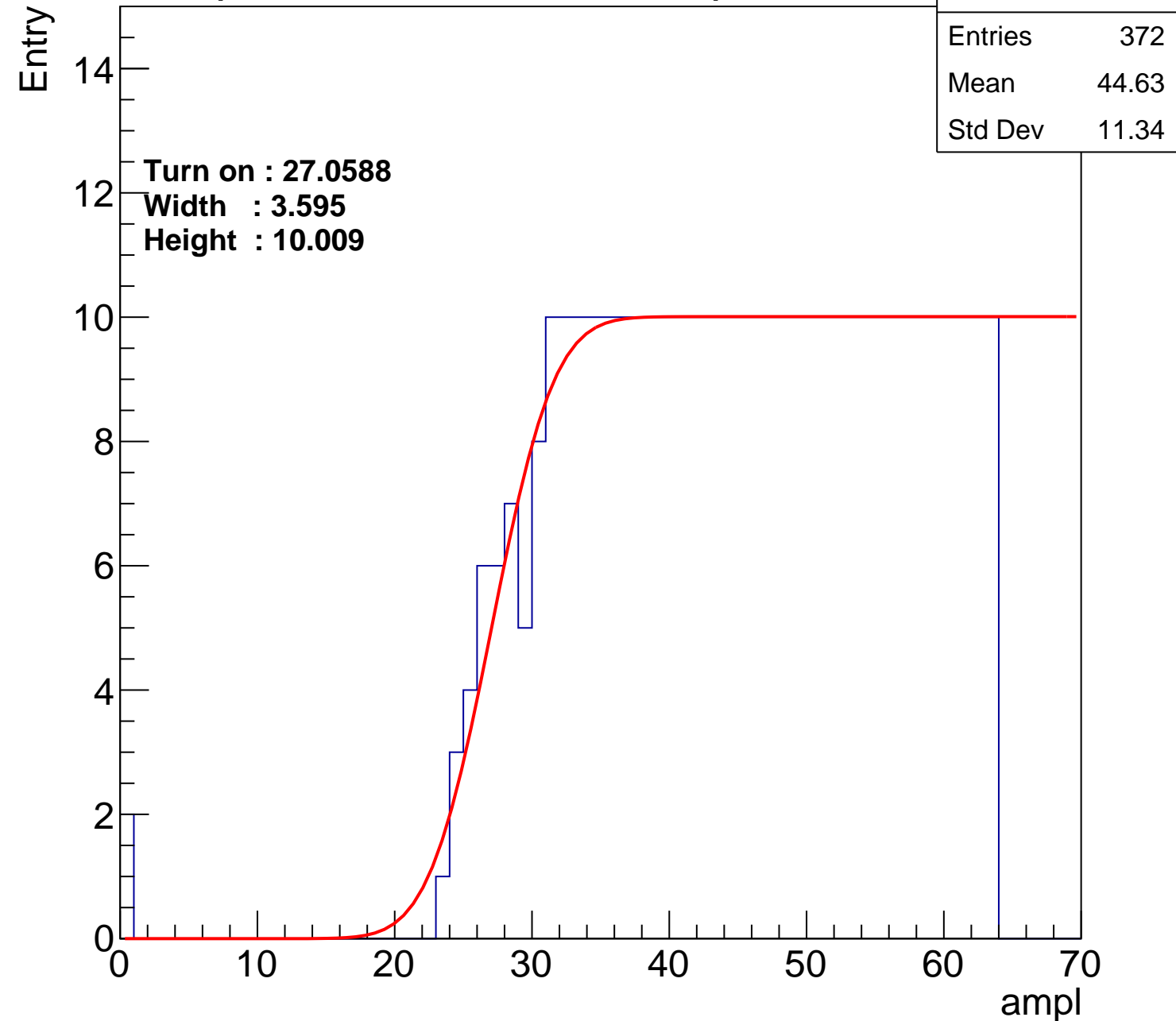
Width : 3.595

Height : 10.009

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch22

calib_packv5_042523_0143.root, FC#13, port D2

Entries	382
Mean	43.9
Std Dev	12.26

Turn on : 26.4368

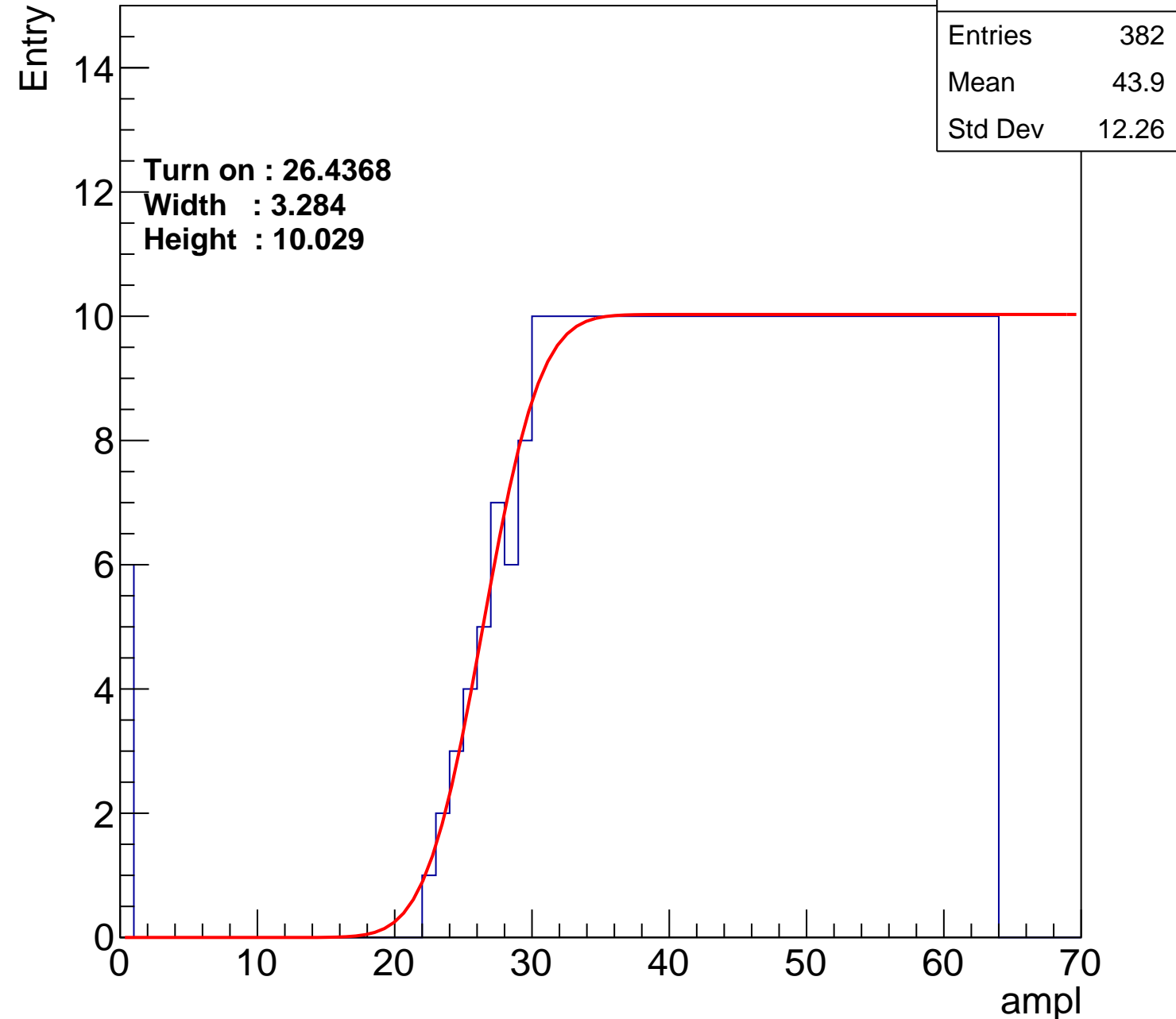
Width : 3.284

Height : 10.029

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch23

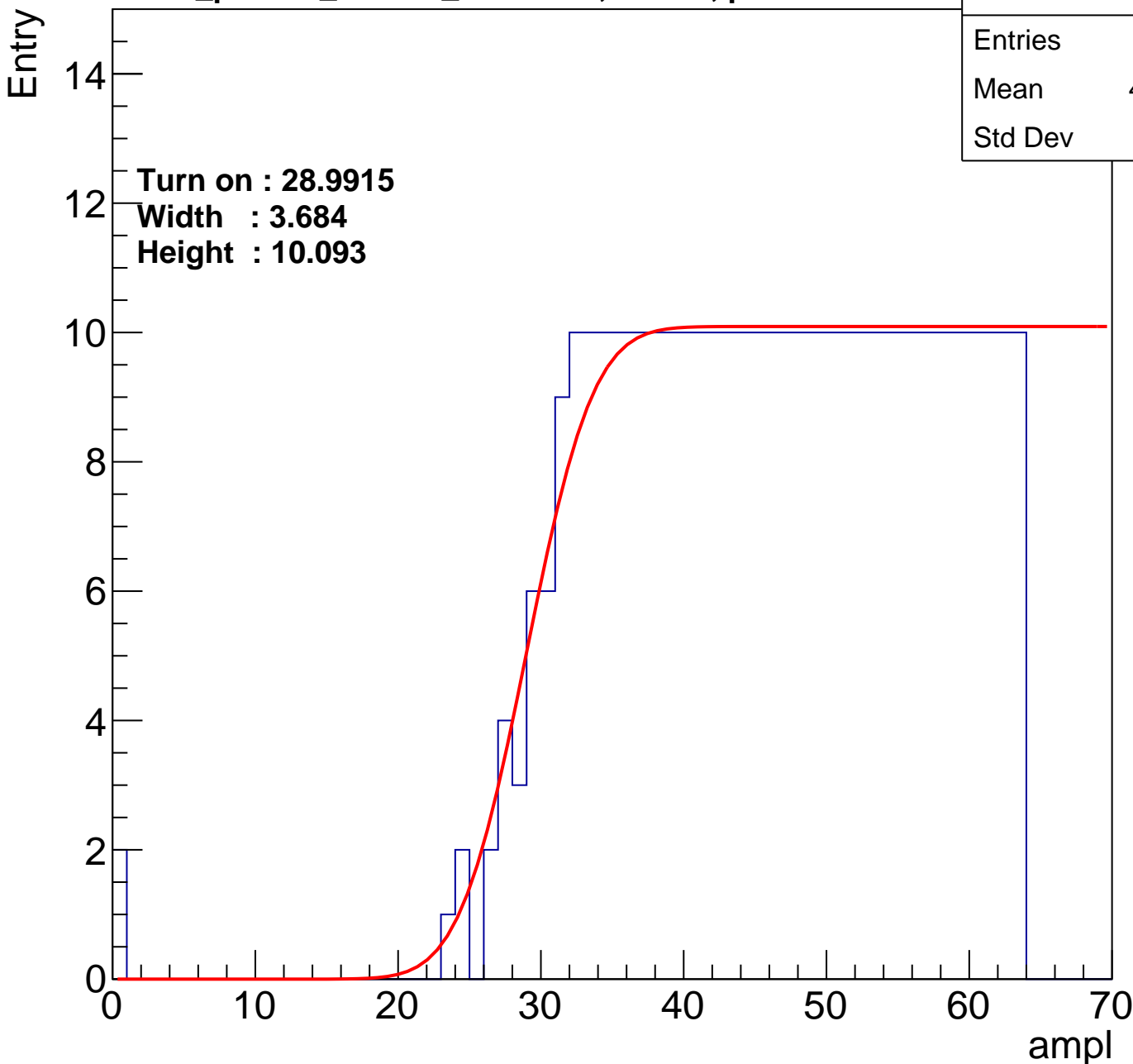
calib_packv5_042523_0143.root, FC#13, port D2

Entries	355
Mean	45.49
Std Dev	10.9

Turn on : 28.9915

Width : 3.684

Height : 10.093



B1L003S, U2-ch24

calib_packv5_042523_0143.root, FC#13, port D2

Entries	363
Mean	45.12
Std Dev	11.06

Turn on : 28.4808

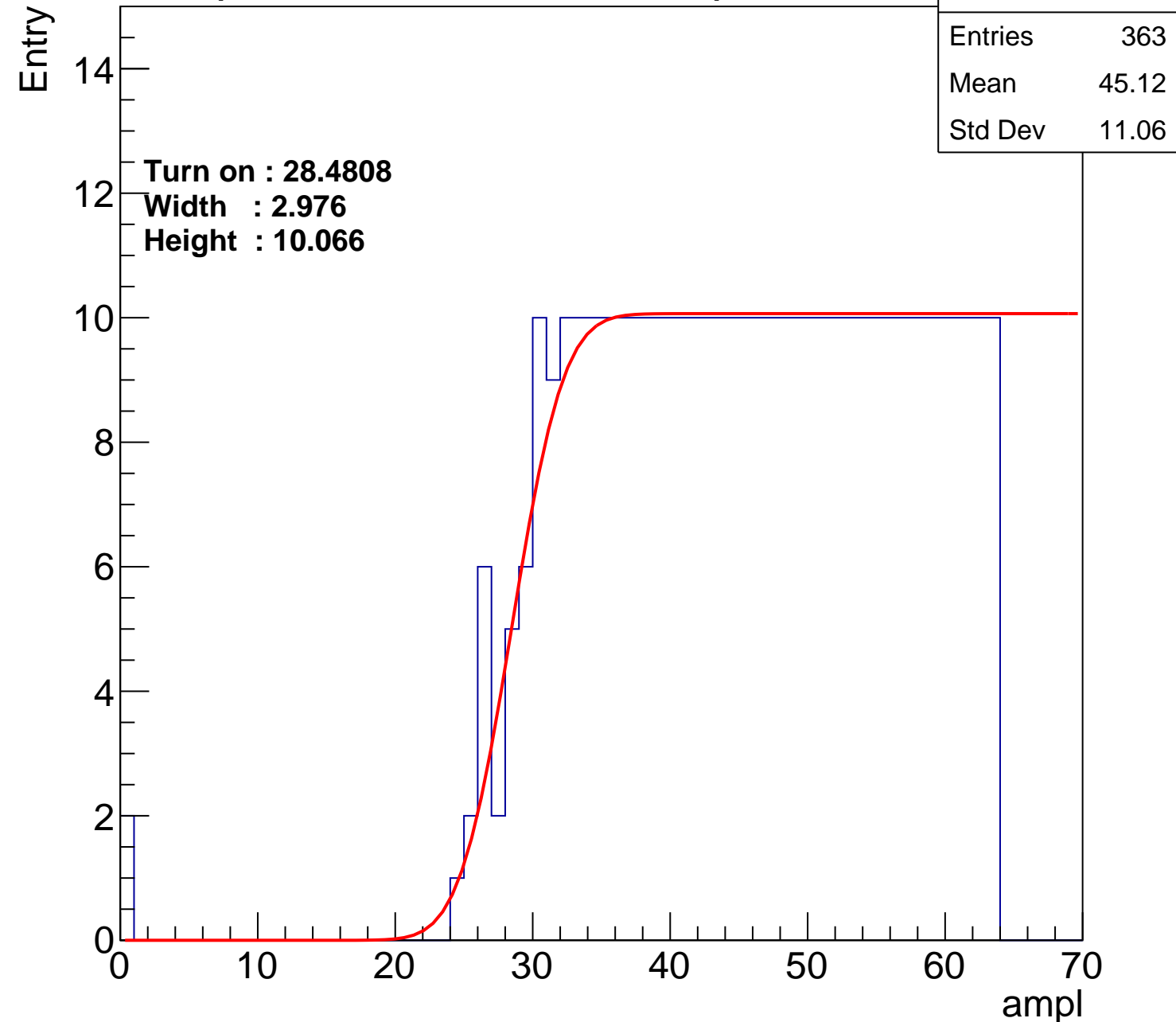
Width : 2.976

Height : 10.066

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch25

calib_packv5_042523_0143.root, FC#13, port D2

Entries	367
Mean	44.84
Std Dev	11.37

Turn on : 27.7986

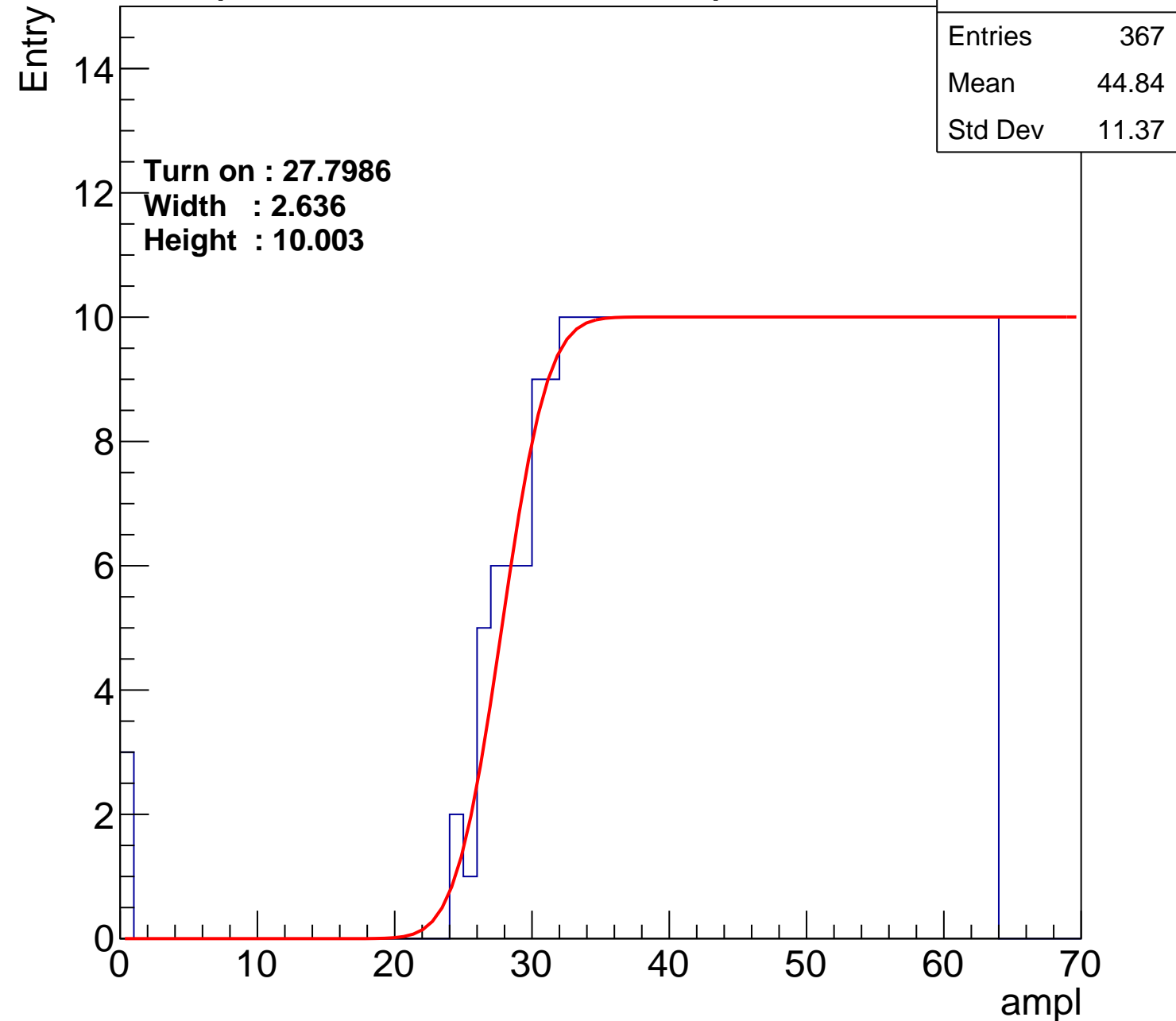
Width : 2.636

Height : 10.003

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch26

calib_packv5_042523_0143.root, FC#13, port D2

Entries	365
Mean	45.06
Std Dev	10.94

Turn on : 27.8922

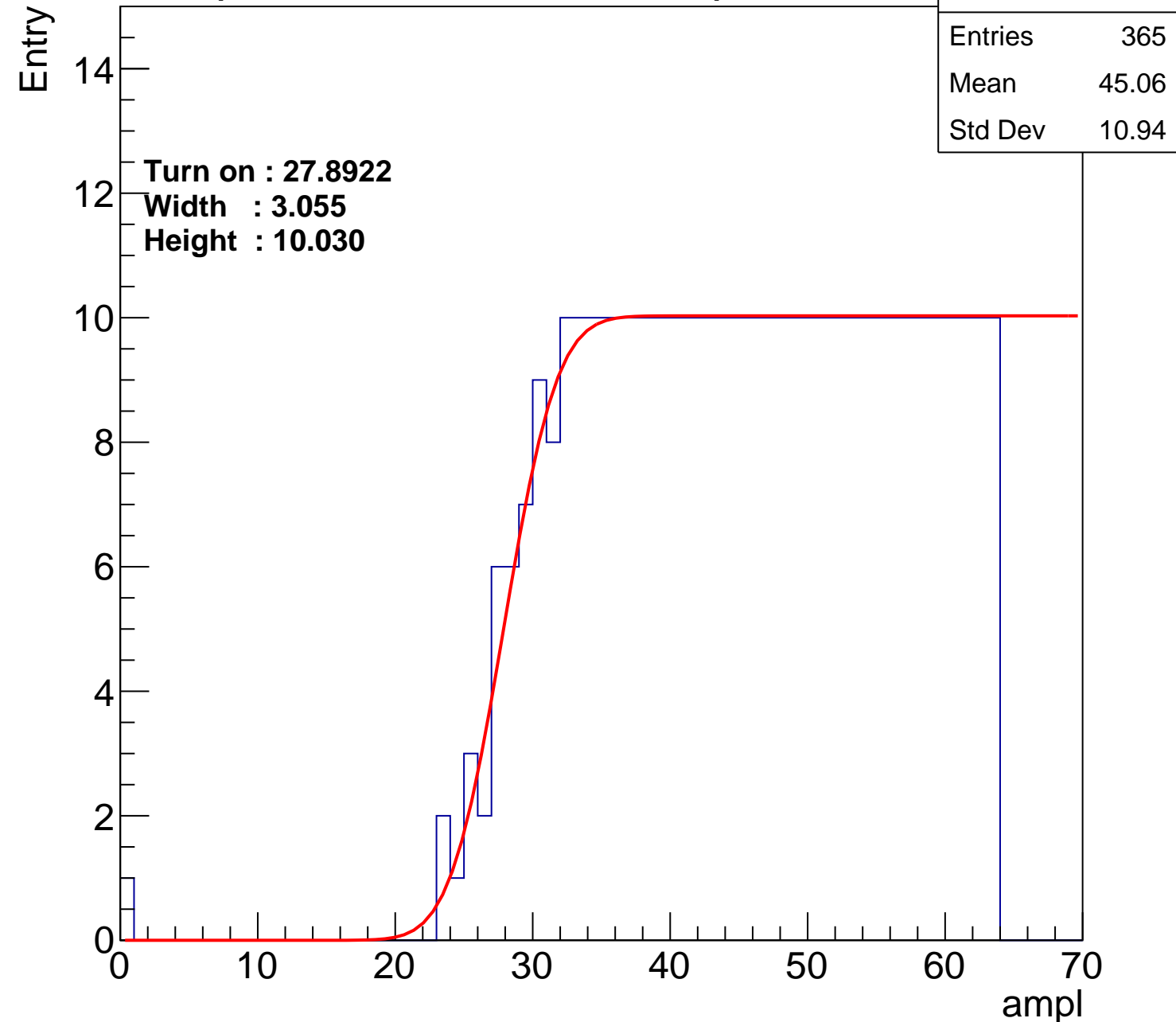
Width : 3.055

Height : 10.030

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch27

calib_packv5_042523_0143.root, FC#13, port D2

Entries	378
Mean	44.13
Std Dev	12.04

Turn on : 27.2591

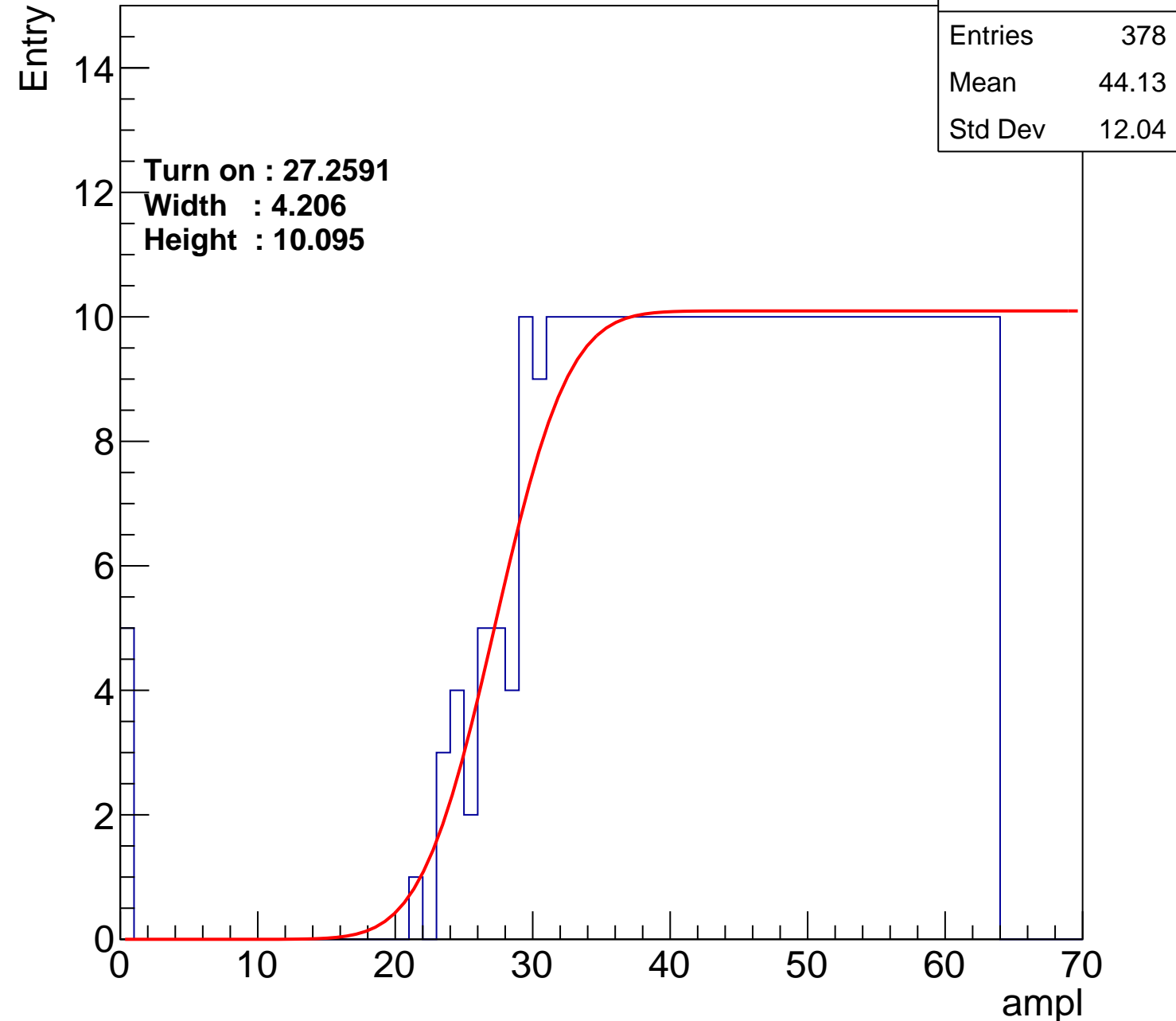
Width : 4.206

Height : 10.095

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch28

calib_packv5_042523_0143.root, FC#13, port D2

Entries	343
Mean	46.11
Std Dev	10.41

Turn on : 29.7530

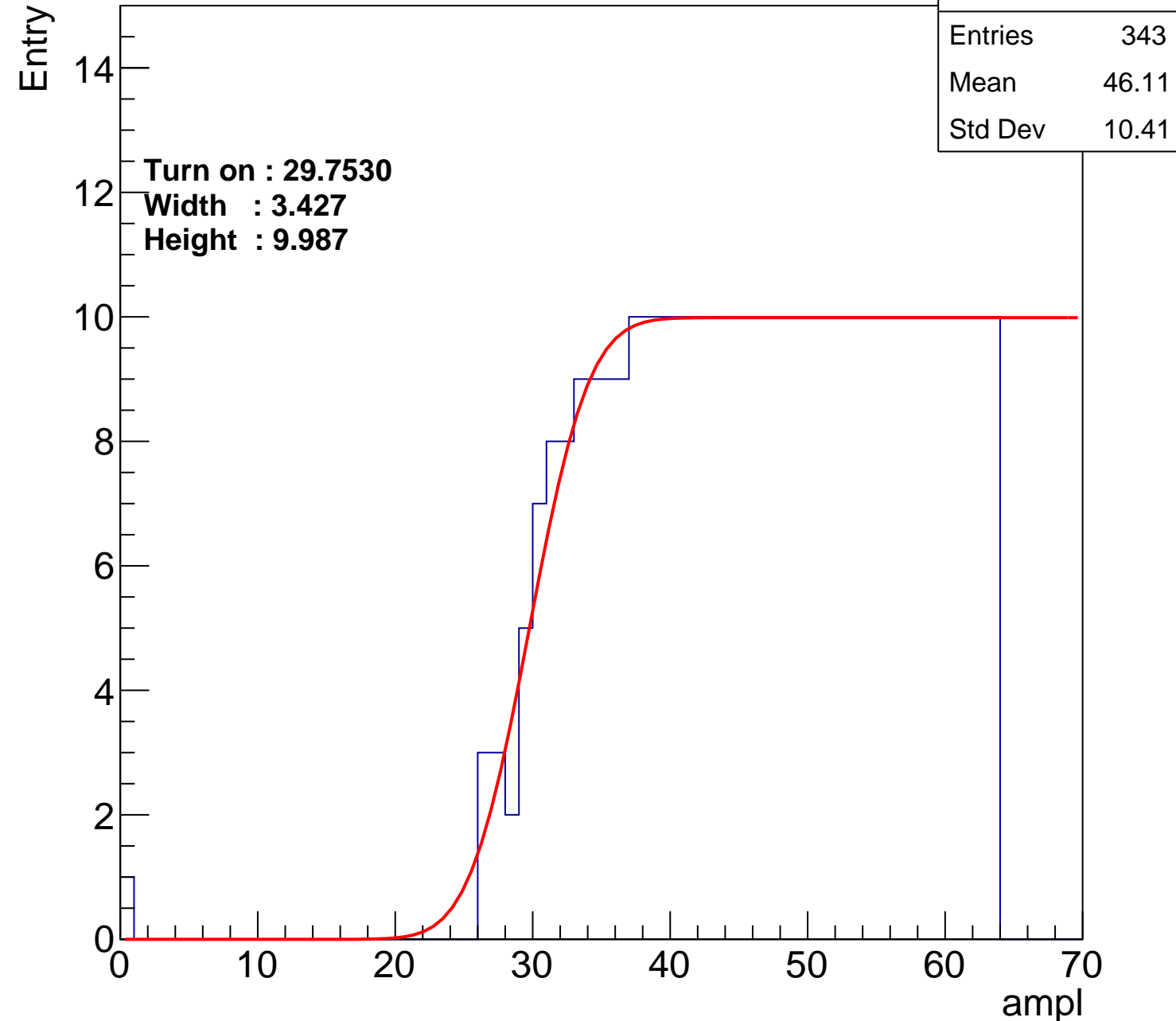
Width : 3.427

Height : 9.987

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch29

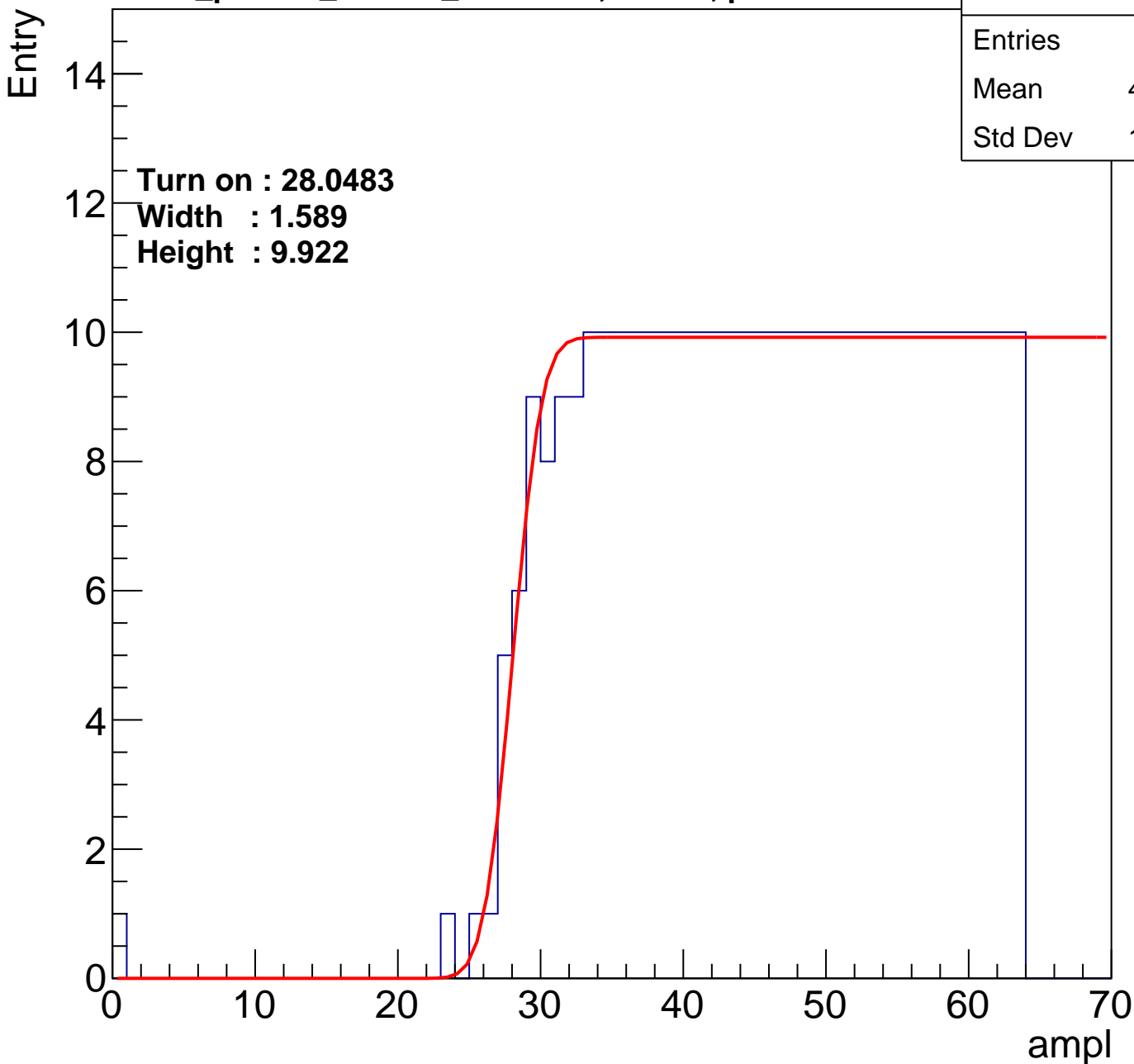
calib_packv5_042523_0143.root, FC#13, port D2

Entries	360
Mean	45.35
Std Dev	10.74

Turn on : 28.0483

Width : 1.589

Height : 9.922



B1L003S, U2-ch30

calib_packv5_042523_0143.root, FC#13, port D2

Entries	380
Mean	44.27
Std Dev	11.5

Turn on : 26.8025

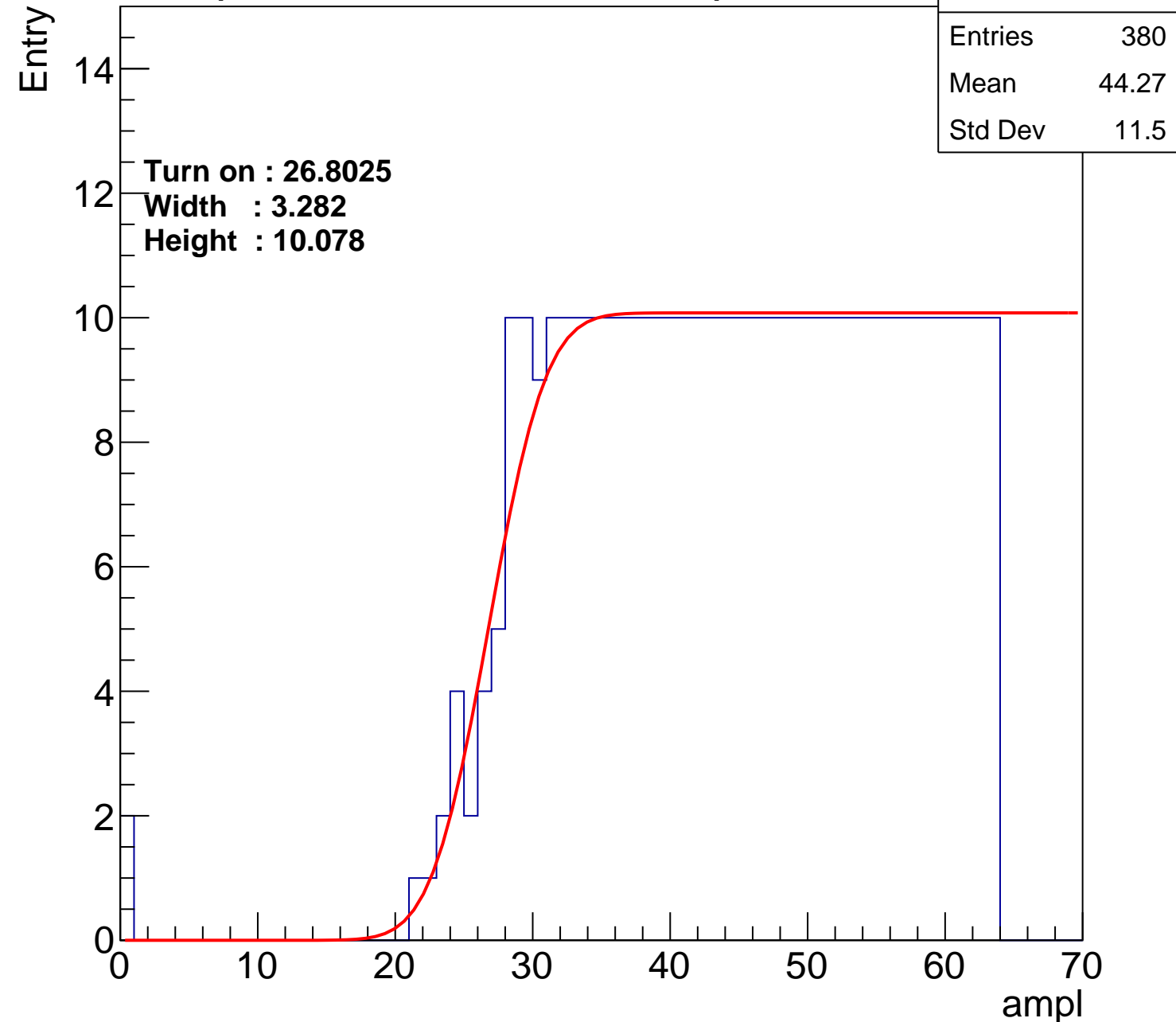
Width : 3.282

Height : 10.078

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch31

calib_packv5_042523_0143.root, FC#13, port D2

Entries	377
Mean	44.42
Std Dev	11.42

Turn on : 26.5762

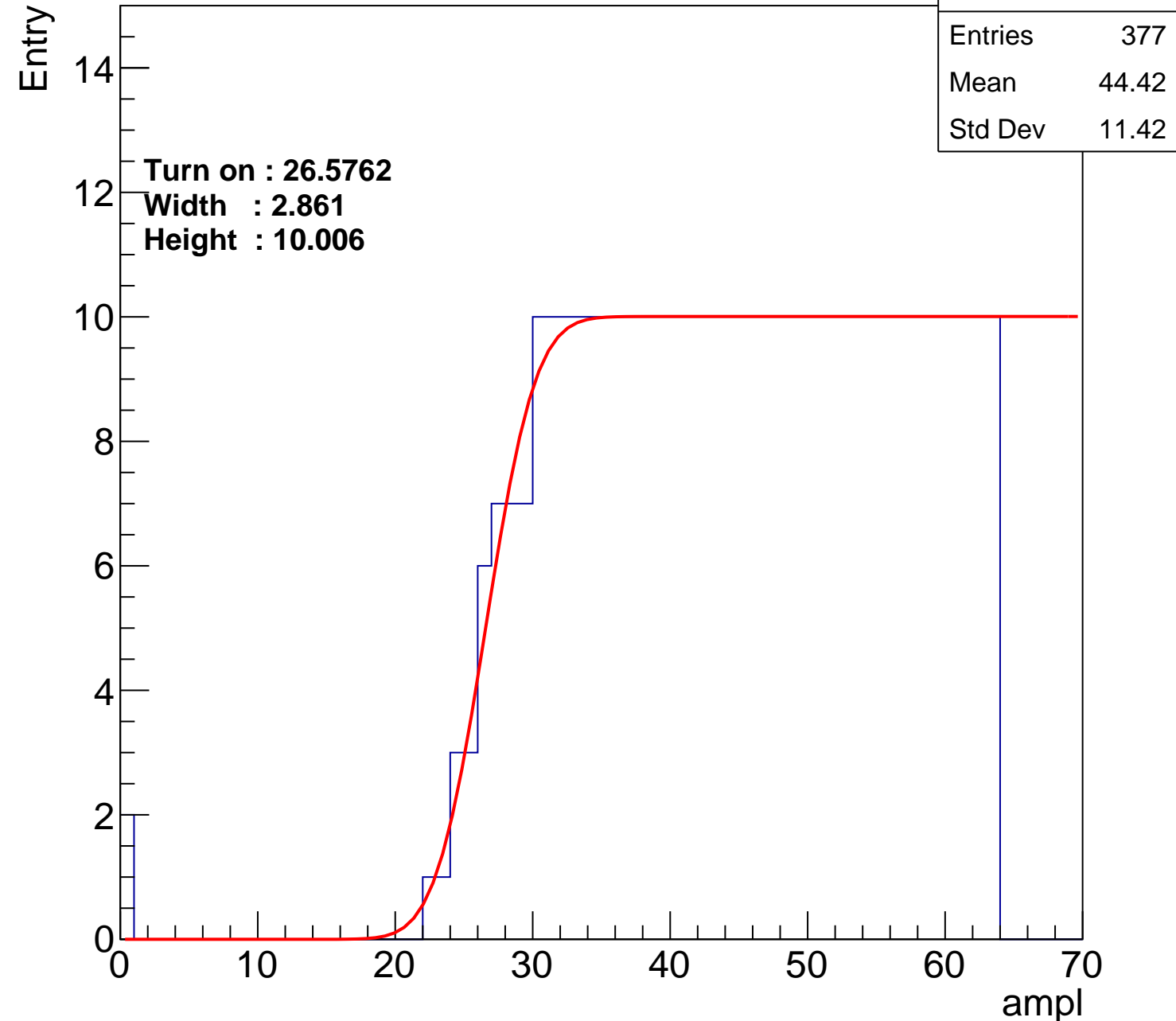
Width : 2.861

Height : 10.006

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch32

calib_packv5_042523_0143.root, FC#13, port D2

Entries	341
Mean	46.11
Std Dev	10.76

Turn on : 30.7684

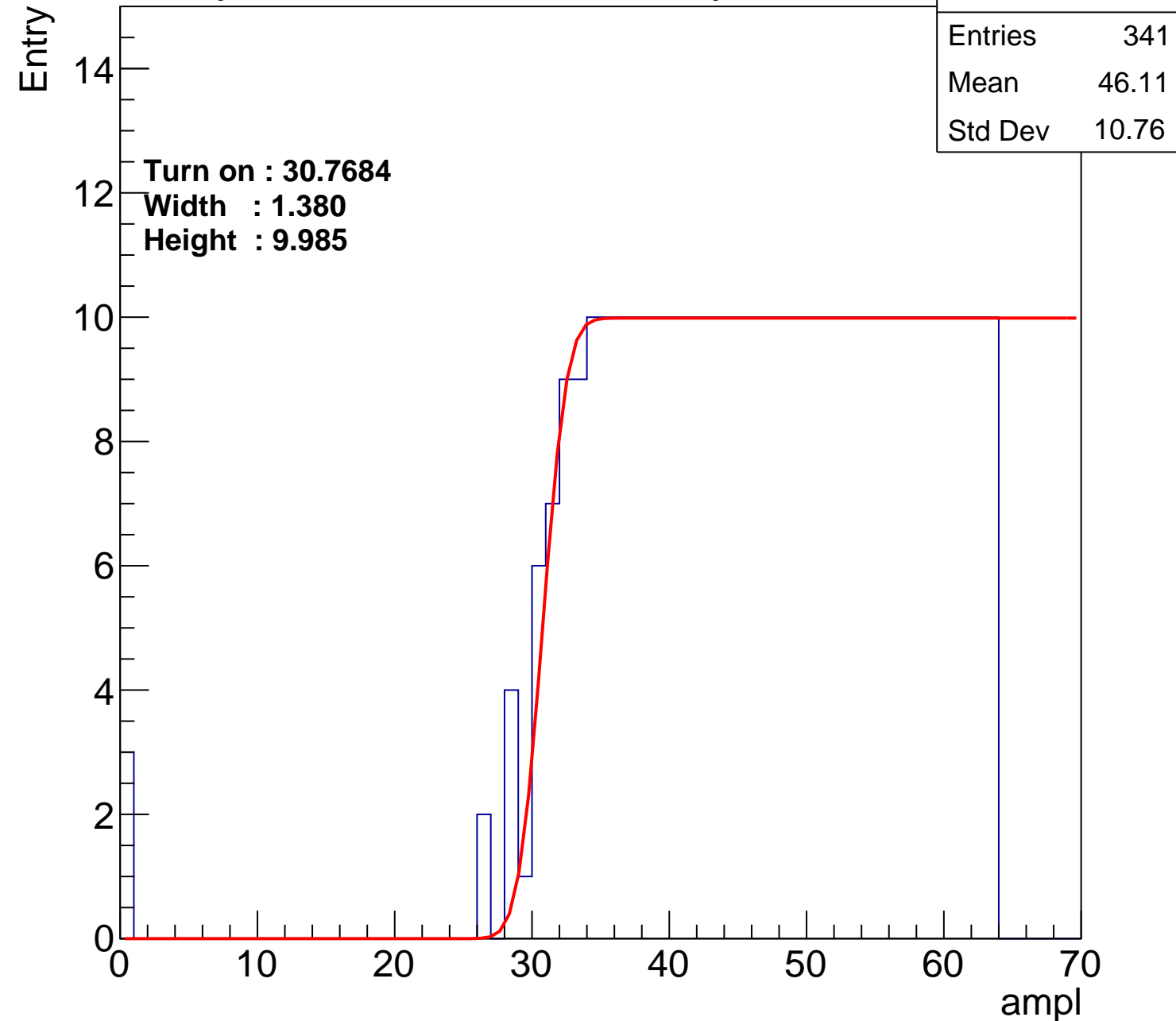
Width : 1.380

Height : 9.985

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch33

calib_packv5_042523_0143.root, FC#13, port D2

Entries	371
Mean	44.75
Std Dev	11.13

Turn on : 27.1202

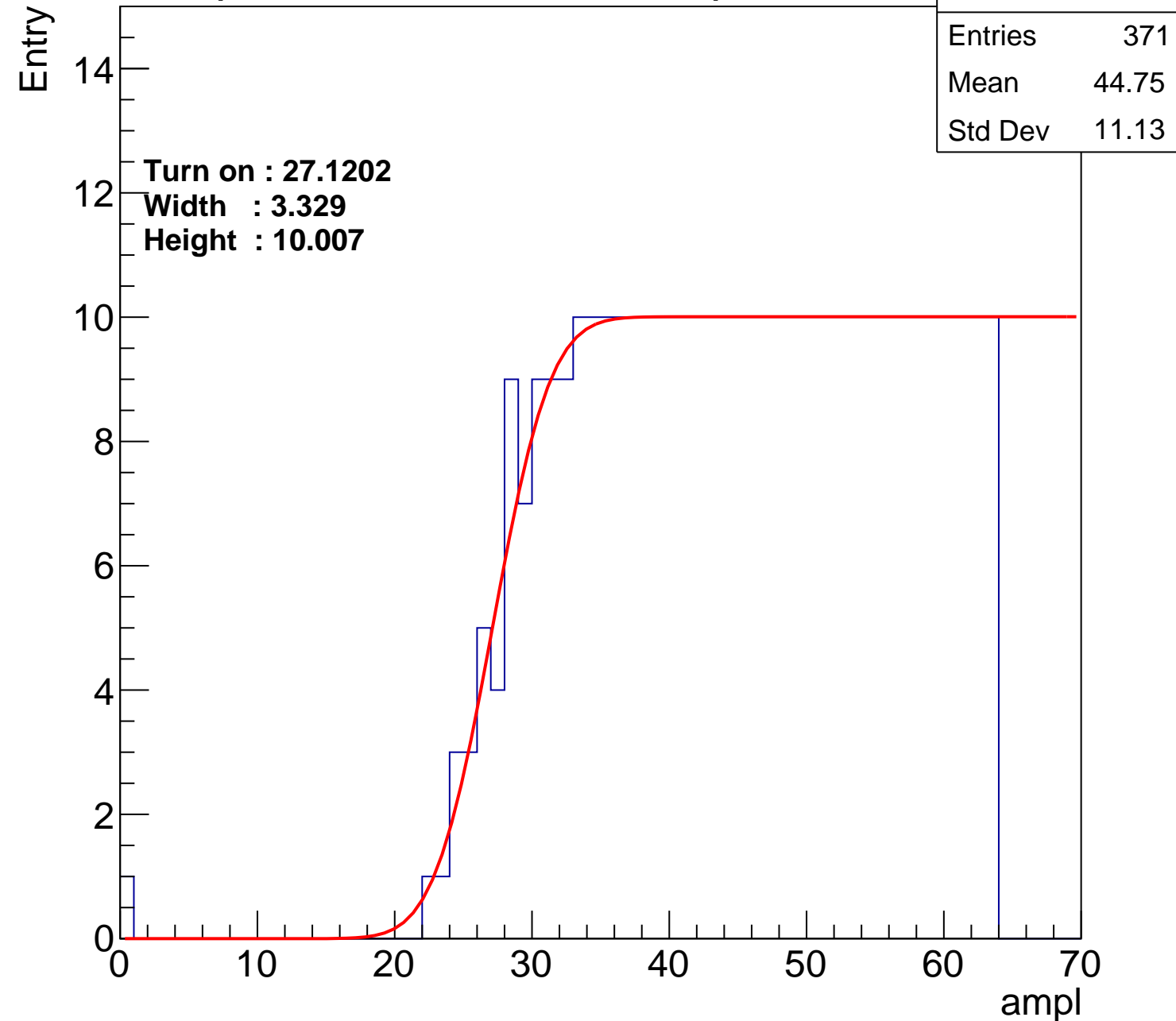
Width : 3.329

Height : 10.007

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch34

calib_packv5_042523_0143.root, FC#13, port D2

Entries	384
Mean	43.85
Std Dev	12.17

Turn on : 25.7735

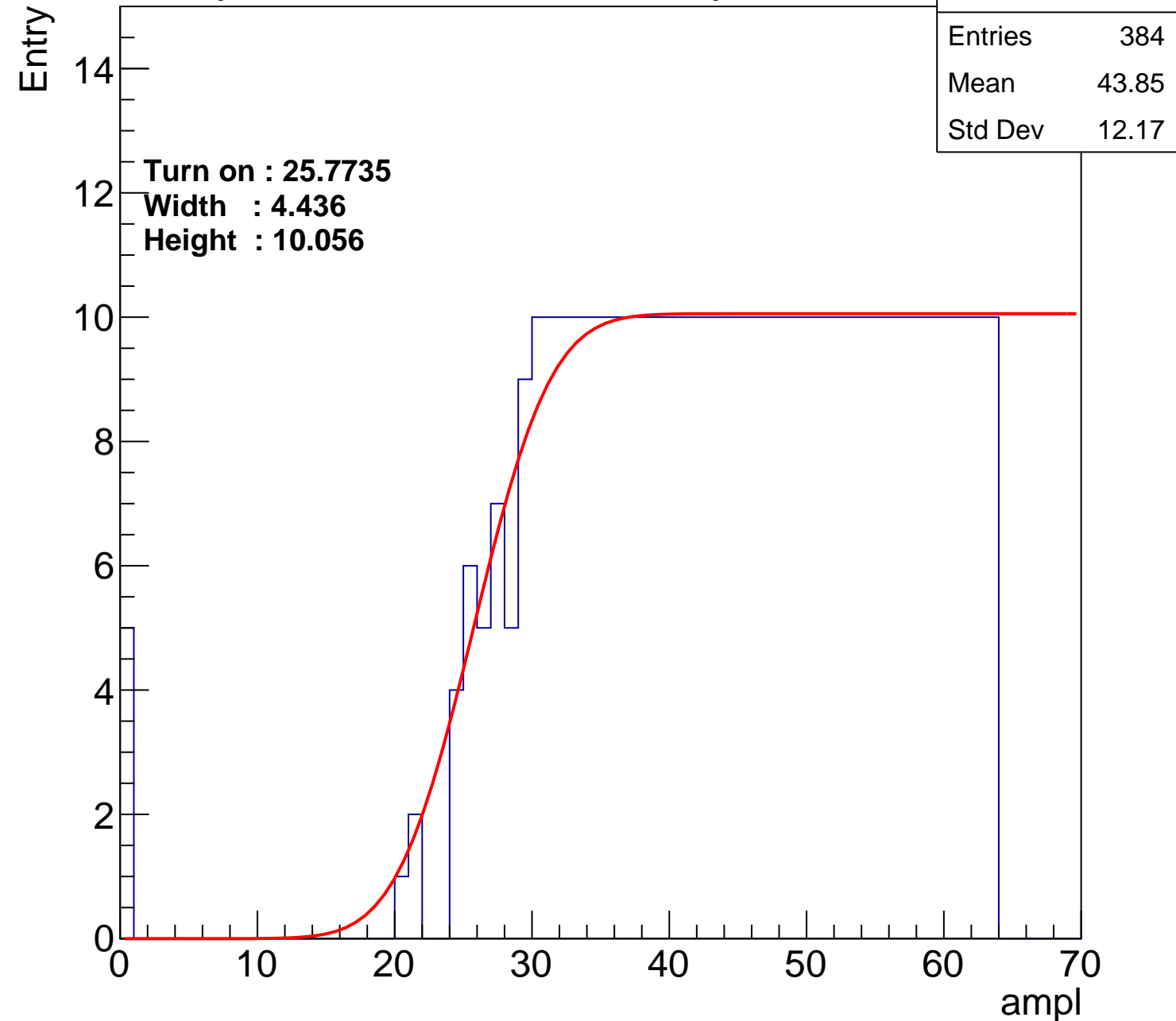
Width : 4.436

Height : 10.056

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch35

calib_packv5_042523_0143.root, FC#13, port D2

Entry

Entries 377

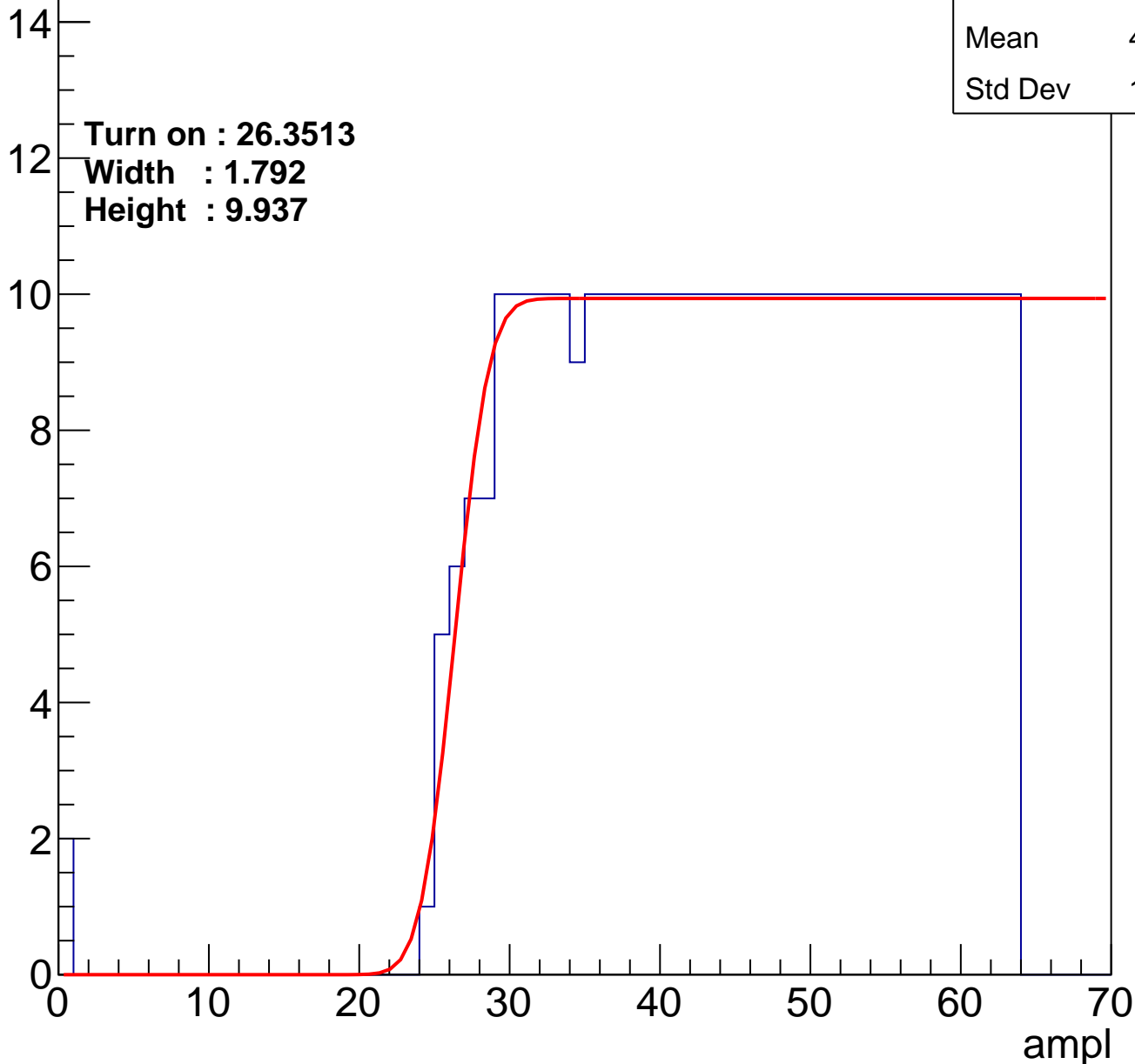
Mean 44.45

Std Dev 11.37

Turn on : 26.3513

Width : 1.792

Height : 9.937



B1L003S, U2-ch36

calib_packv5_042523_0143.root, FC#13, port D2

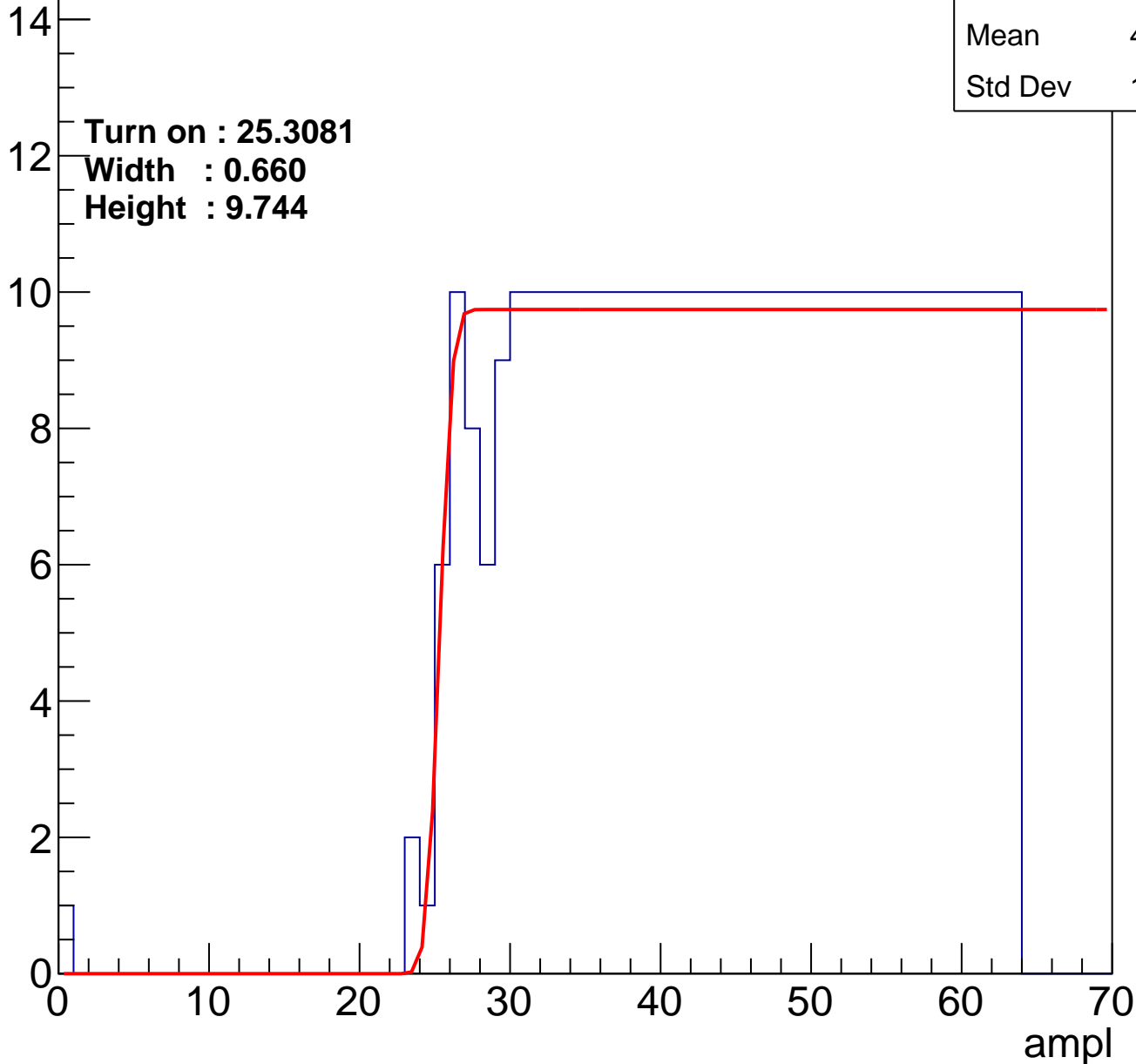
Entry

Entries	383
Mean	44.22
Std Dev	11.35

Turn on : 25.3081

Width : 0.660

Height : 9.744



B1L003S, U2-ch37

calib_packv5_042523_0143.root, FC#13, port D2

Entries	378
Mean	44.29
Std Dev	11.66

Turn on : 26.8328

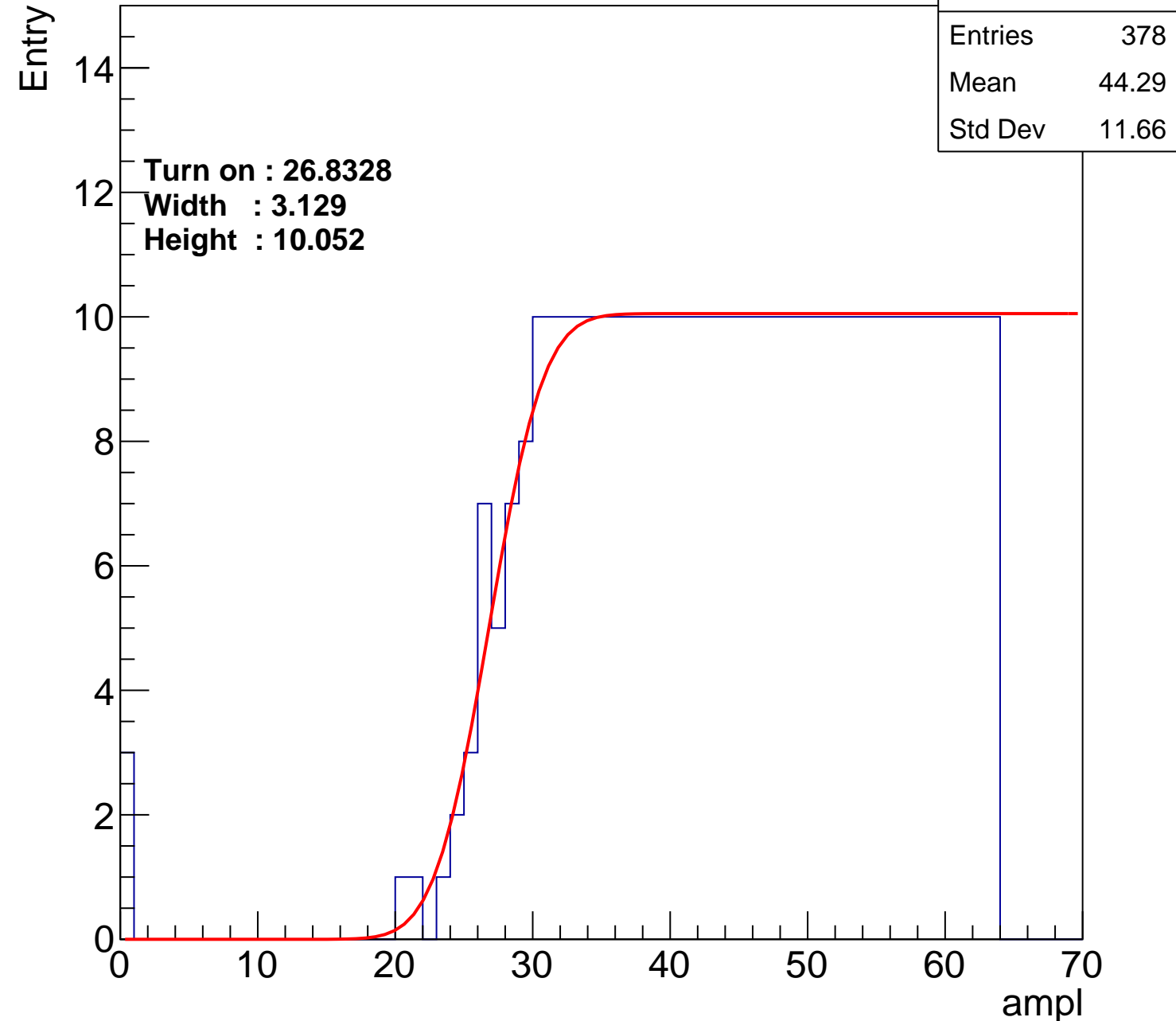
Width : 3.129

Height : 10.052

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch38

calib_packv5_042523_0143.root, FC#13, port D2

Entries	366
Mean	44.95
Std Dev	11.16

Turn on : 27.7707

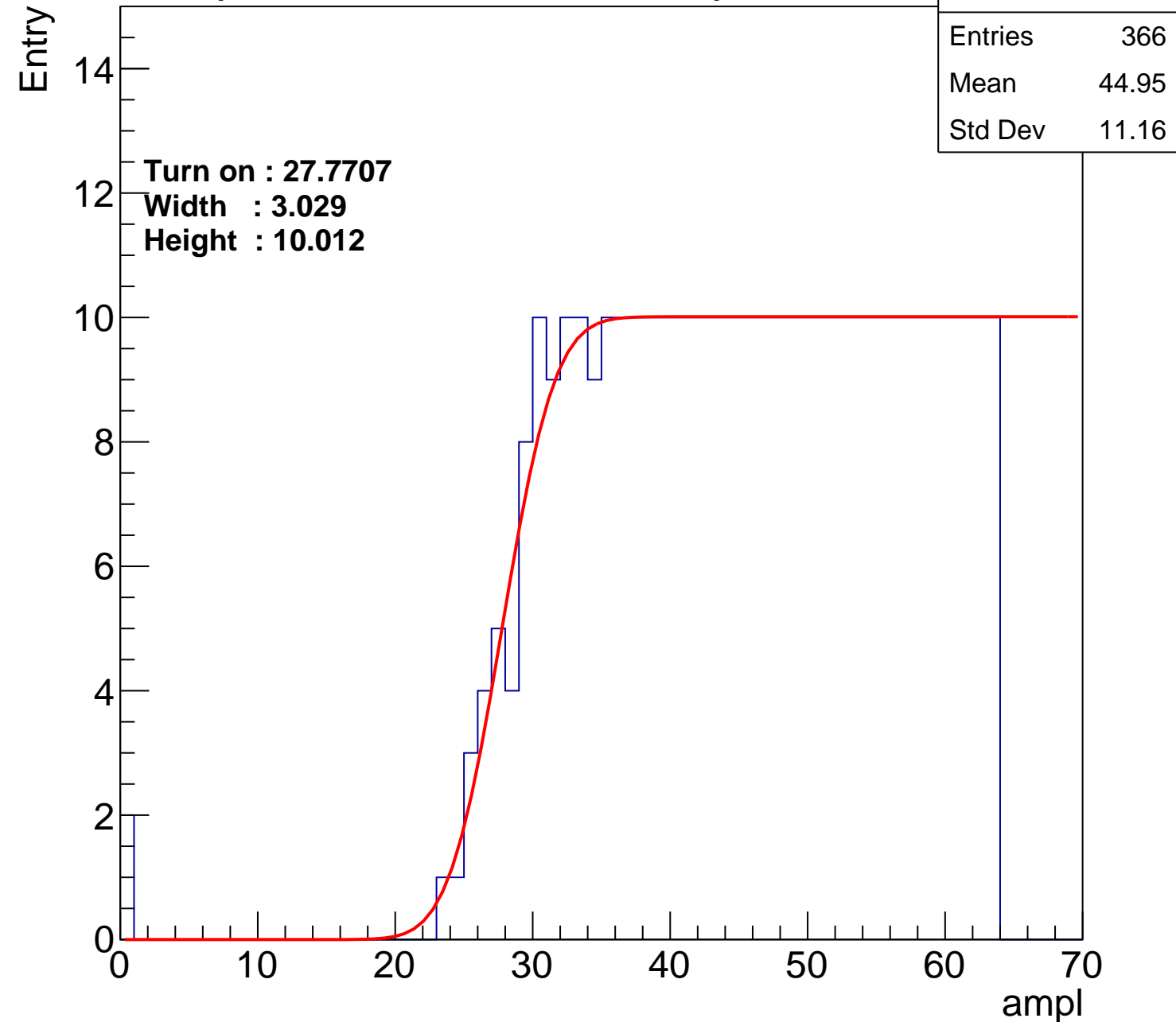
Width : 3.029

Height : 10.012

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch39

calib_packv5_042523_0143.root, FC#13, port D2

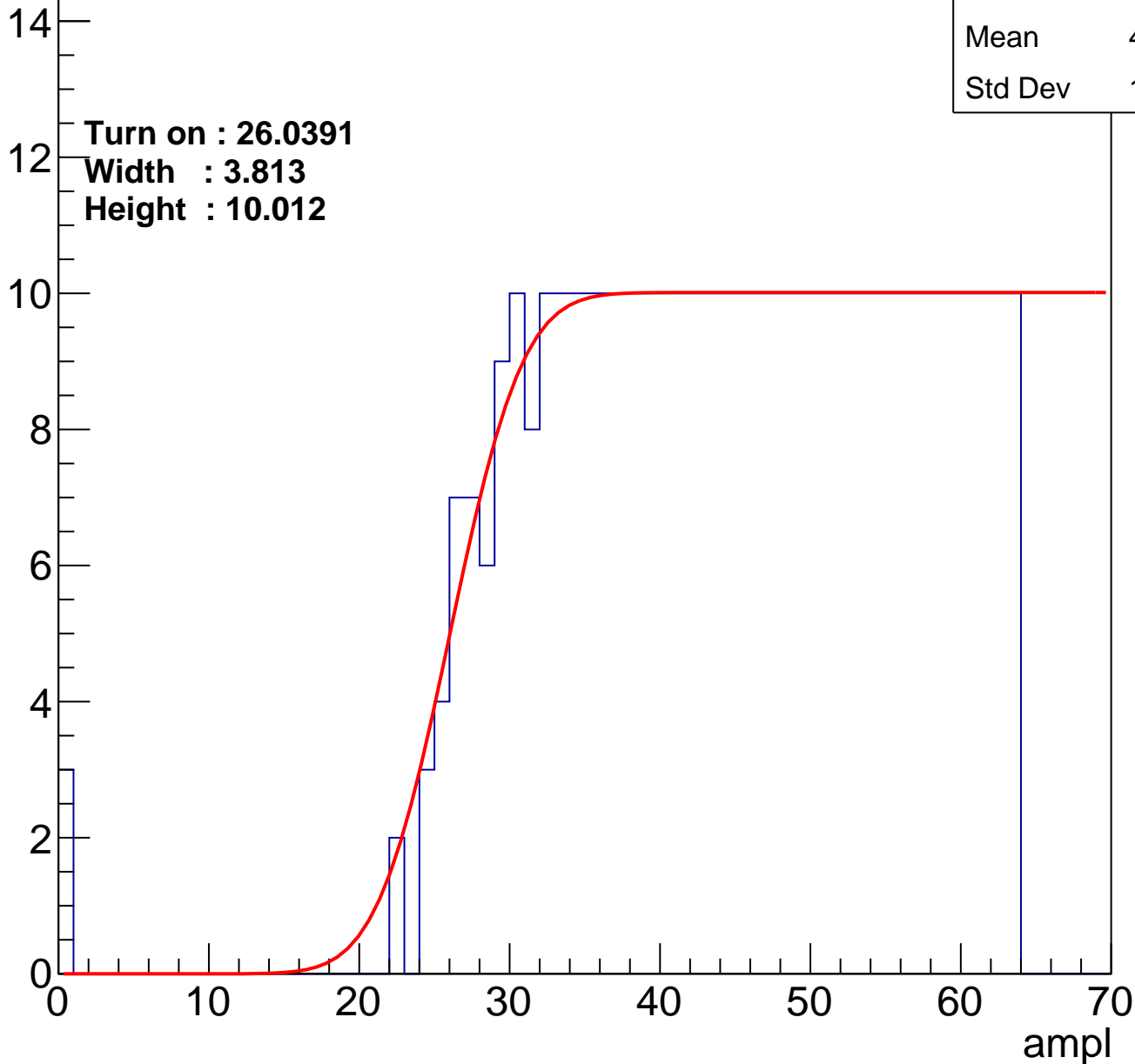
Entry

Entries	379
Mean	44.23
Std Dev	11.69

Turn on : 26.0391

Width : 3.813

Height : 10.012



B1L003S, U2-ch40

calib_packv5_042523_0143.root, FC#13, port D2

Entries	365
Mean	45.13
Std Dev	10.88

Turn on : 27.7331

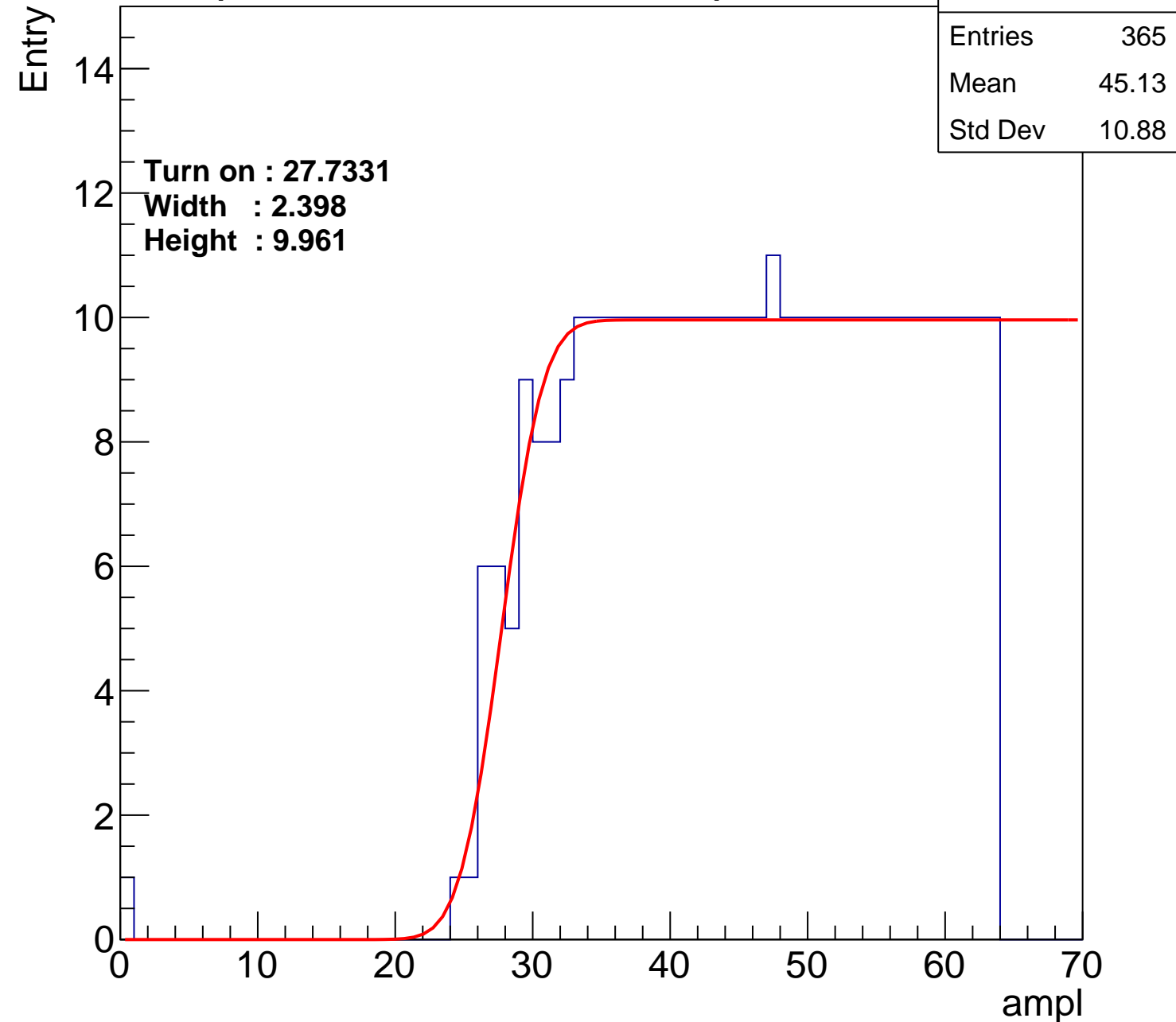
Width : 2.398

Height : 9.961

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch41

calib_packv5_042523_0143.root, FC#13, port D2

Entries	363
Mean	45.12
Std Dev	11.05

Turn on : 27.5641

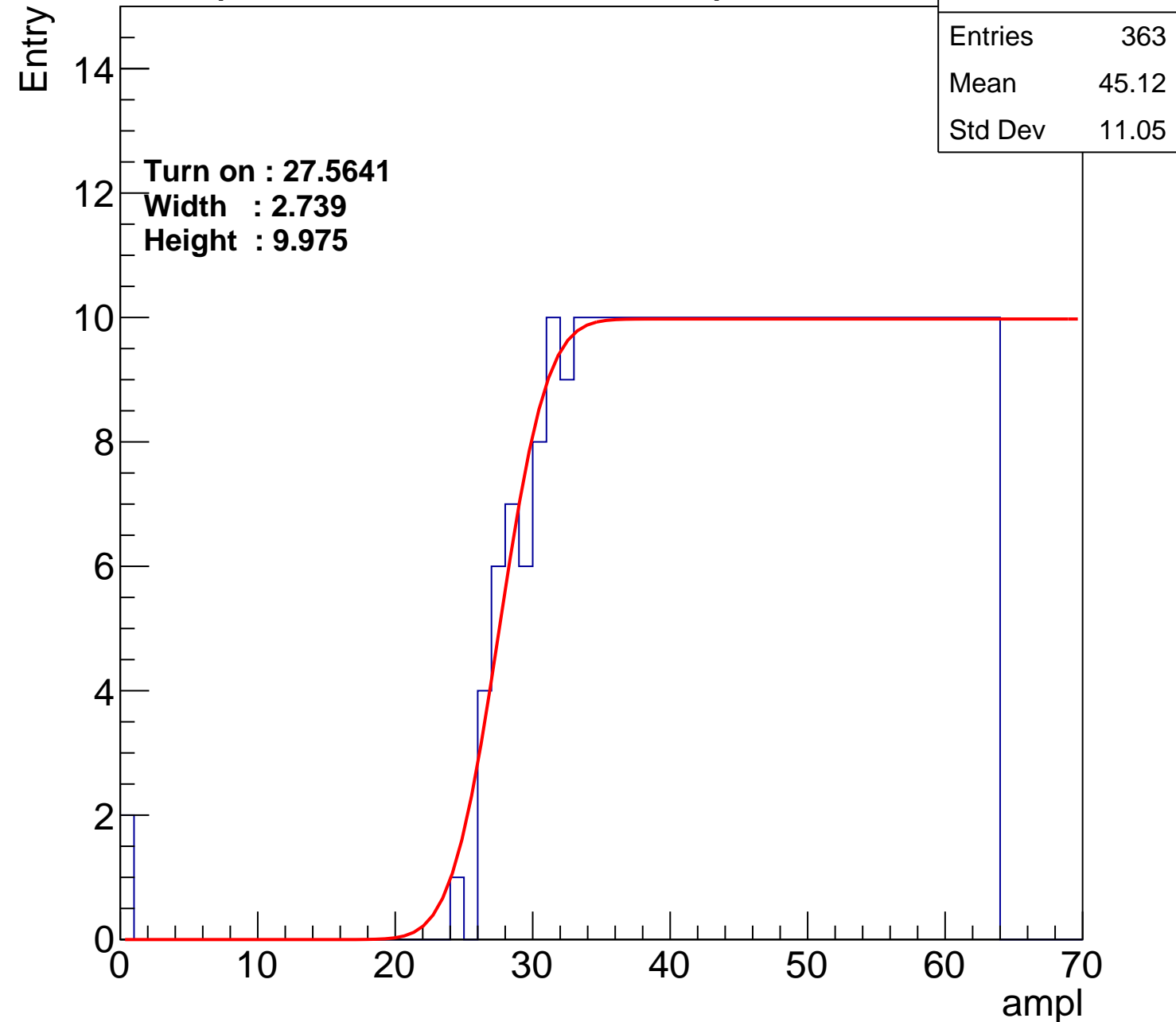
Width : 2.739

Height : 9.975

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch42

calib_packv5_042523_0143.root, FC#13, port D2

Entries	371
Mean	44.65
Std Dev	11.45

Turn on : 27.1344

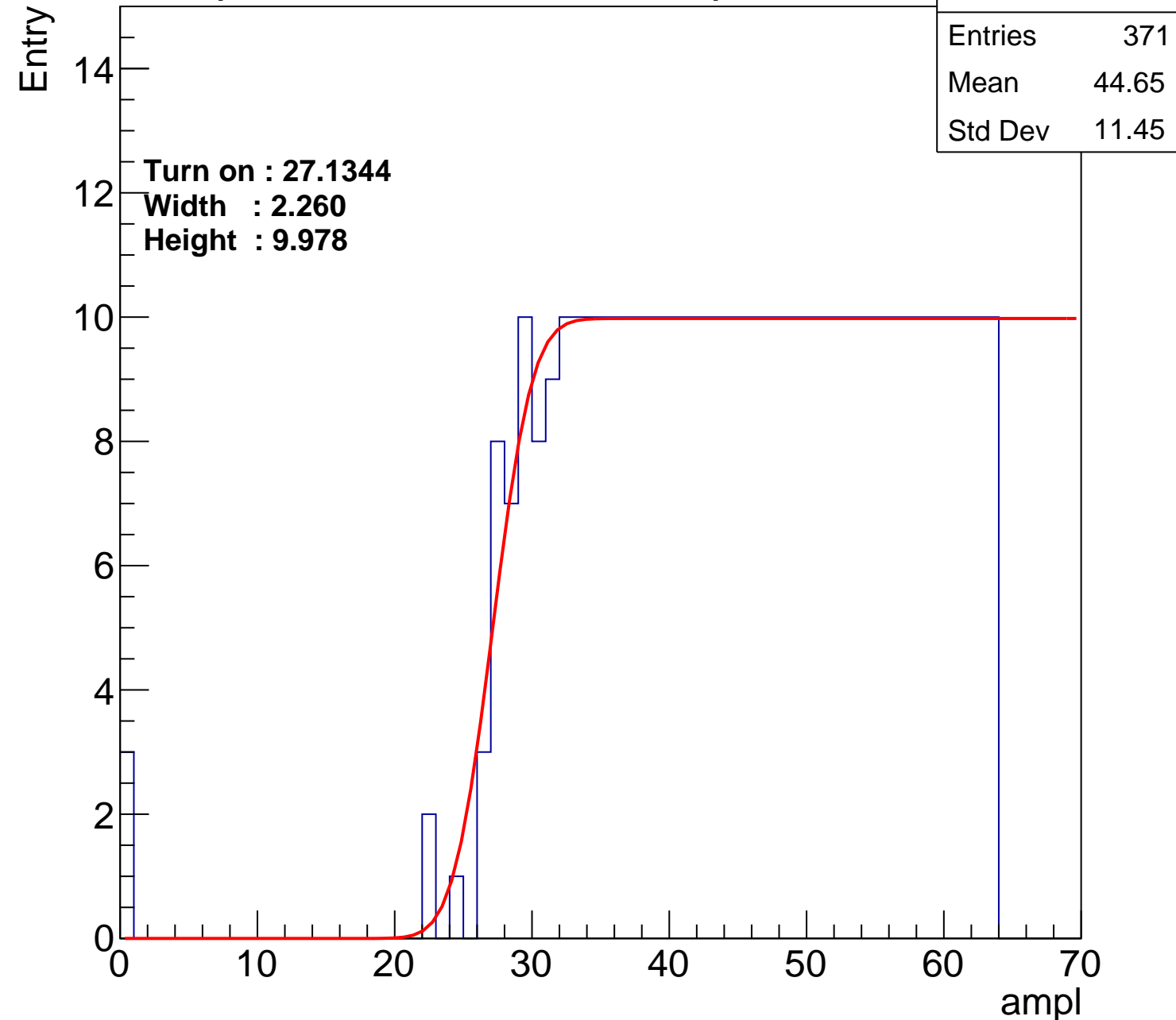
Width : 2.260

Height : 9.978

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch43

calib_packv5_042523_0143.root, FC#13, port D2

Entries	364
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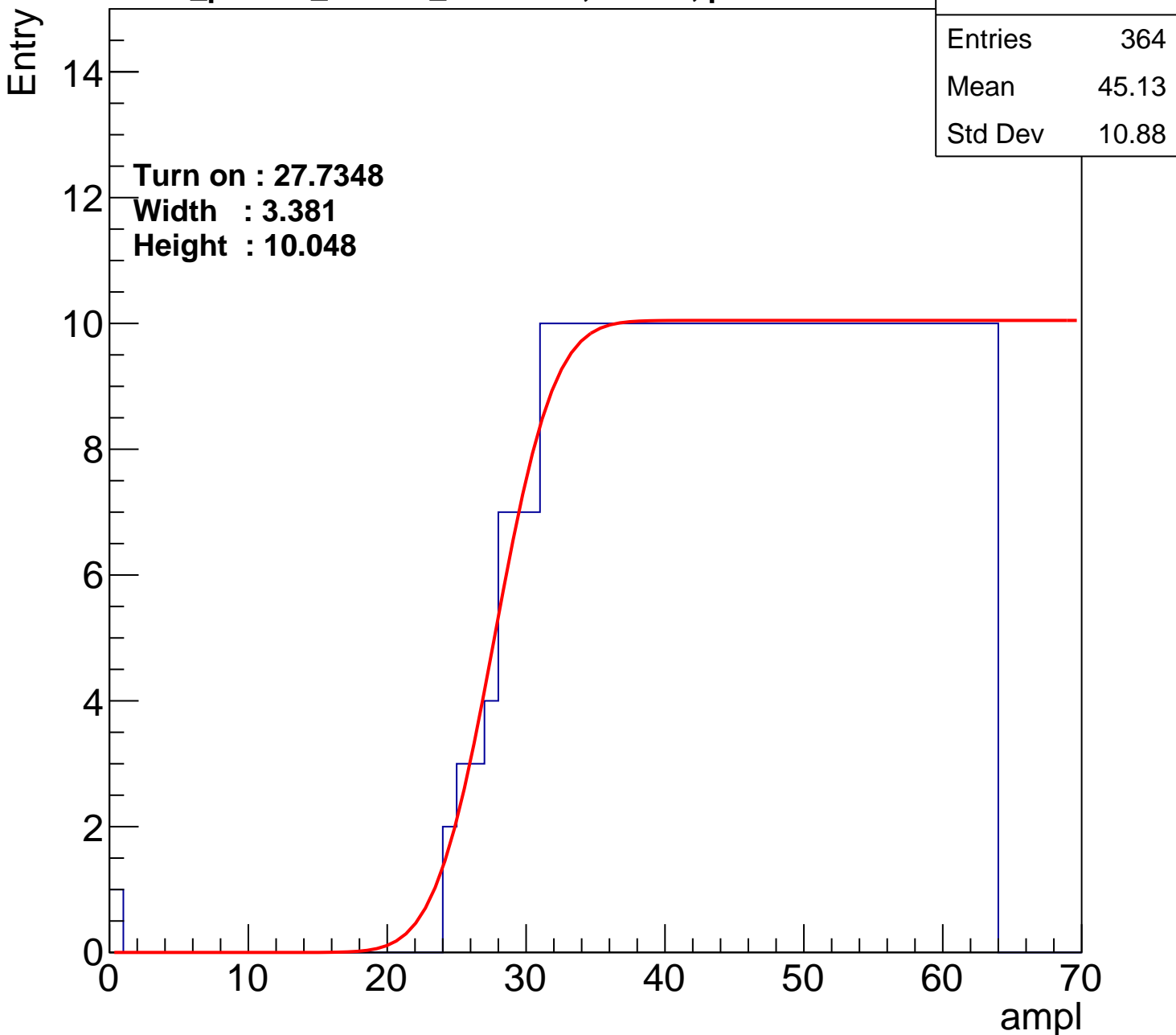
Mean	45.13
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Std Dev	10.88
---------	-------

Turn on : 27.7348

Width : 3.381

Height : 10.048



B1L003S, U2-ch44

calib_packv5_042523_0143.root, FC#13, port D2

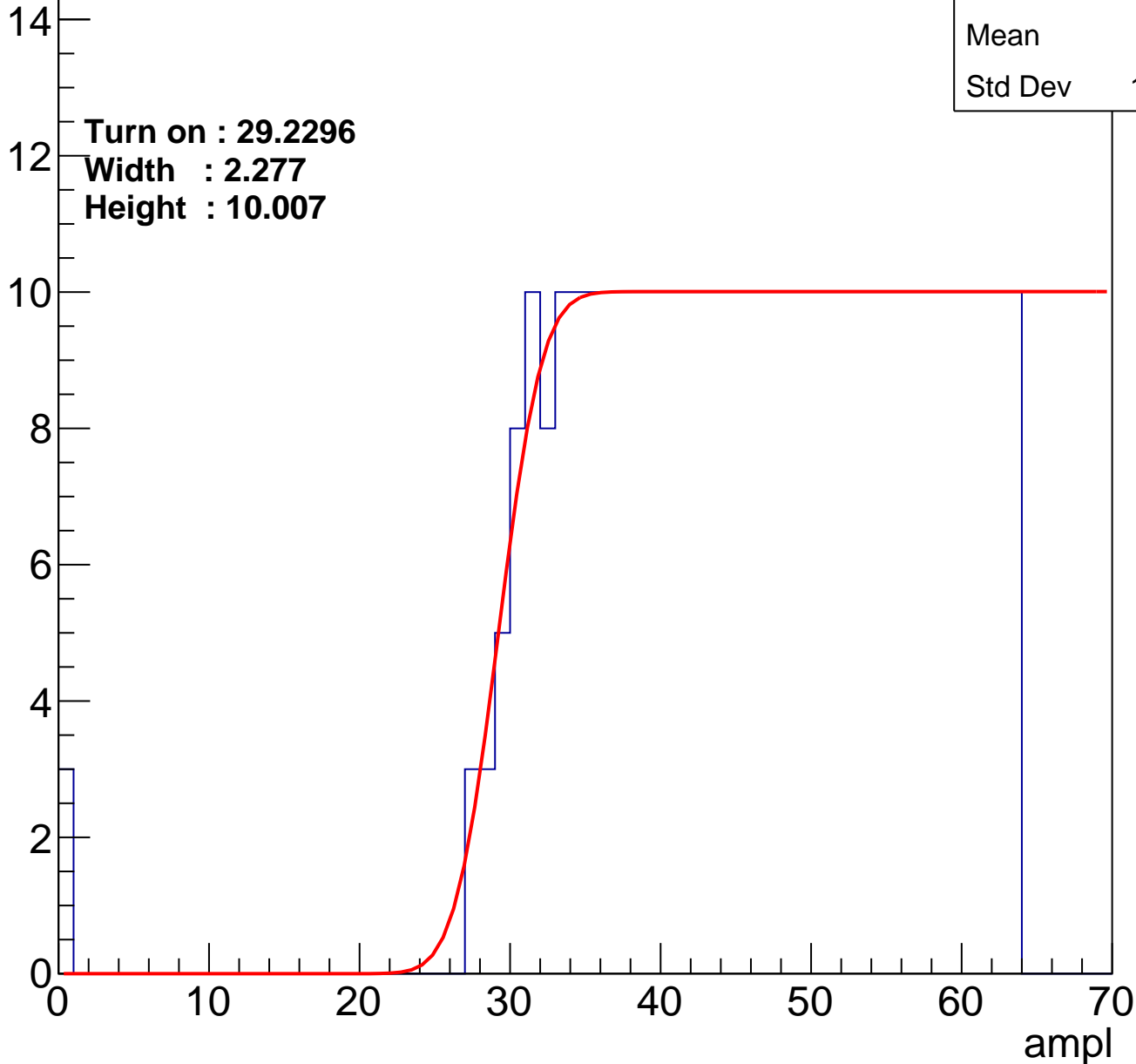
Entry

Entries	350
Mean	45.7
Std Dev	10.92

Turn on : 29.2296

Width : 2.277

Height : 10.007



B1L003S, U2-ch45

calib_packv5_042523_0143.root, FC#13, port D2

Entries	371
Mean	44.49
Std Dev	11.87

Turn on : 27.3572

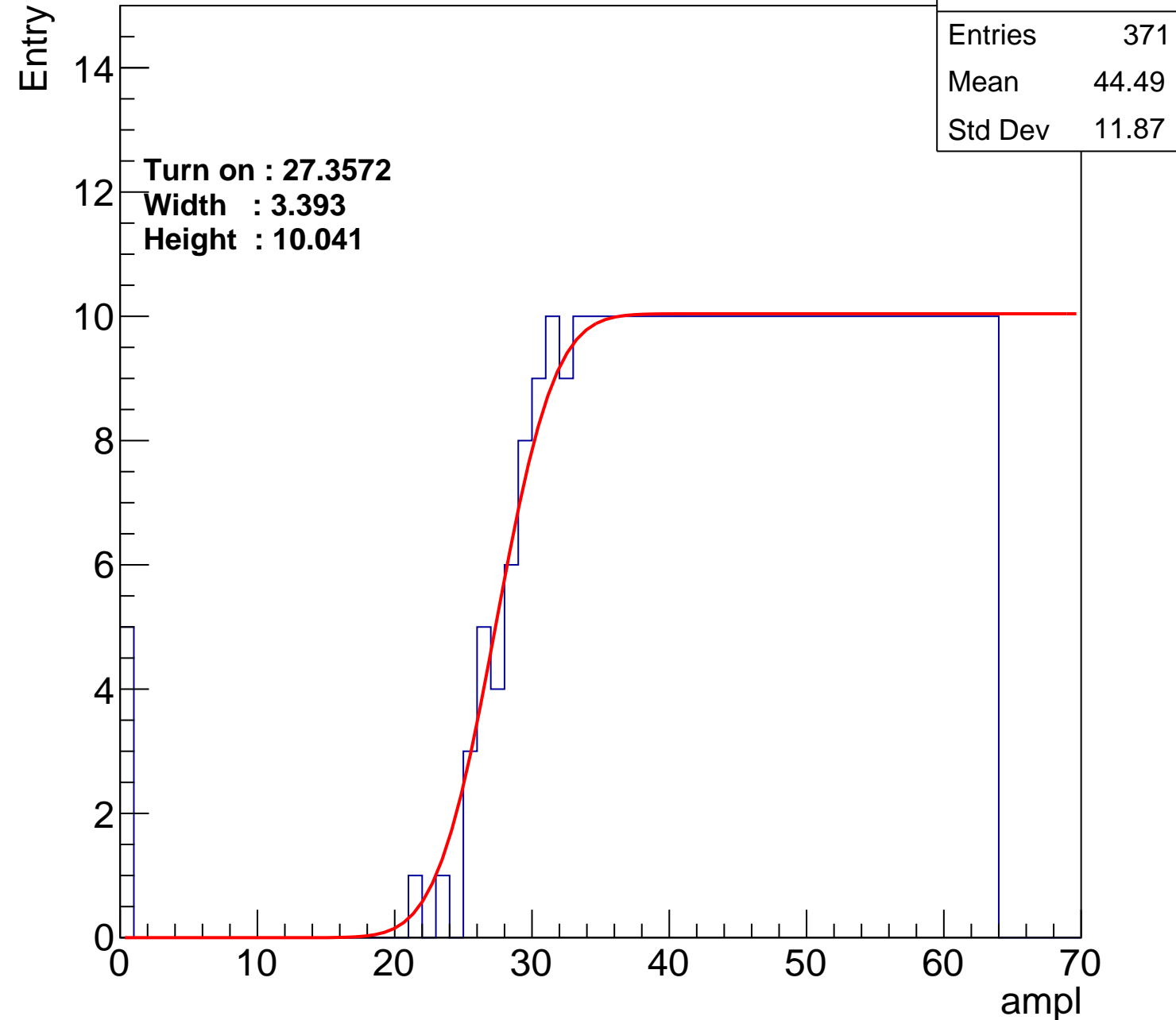
Width : 3.393

Height : 10.041

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch46

calib_packv5_042523_0143.root, FC#13, port D2

Entries	363
Mean	45.18
Std Dev	10.87

Turn on : 28.0261

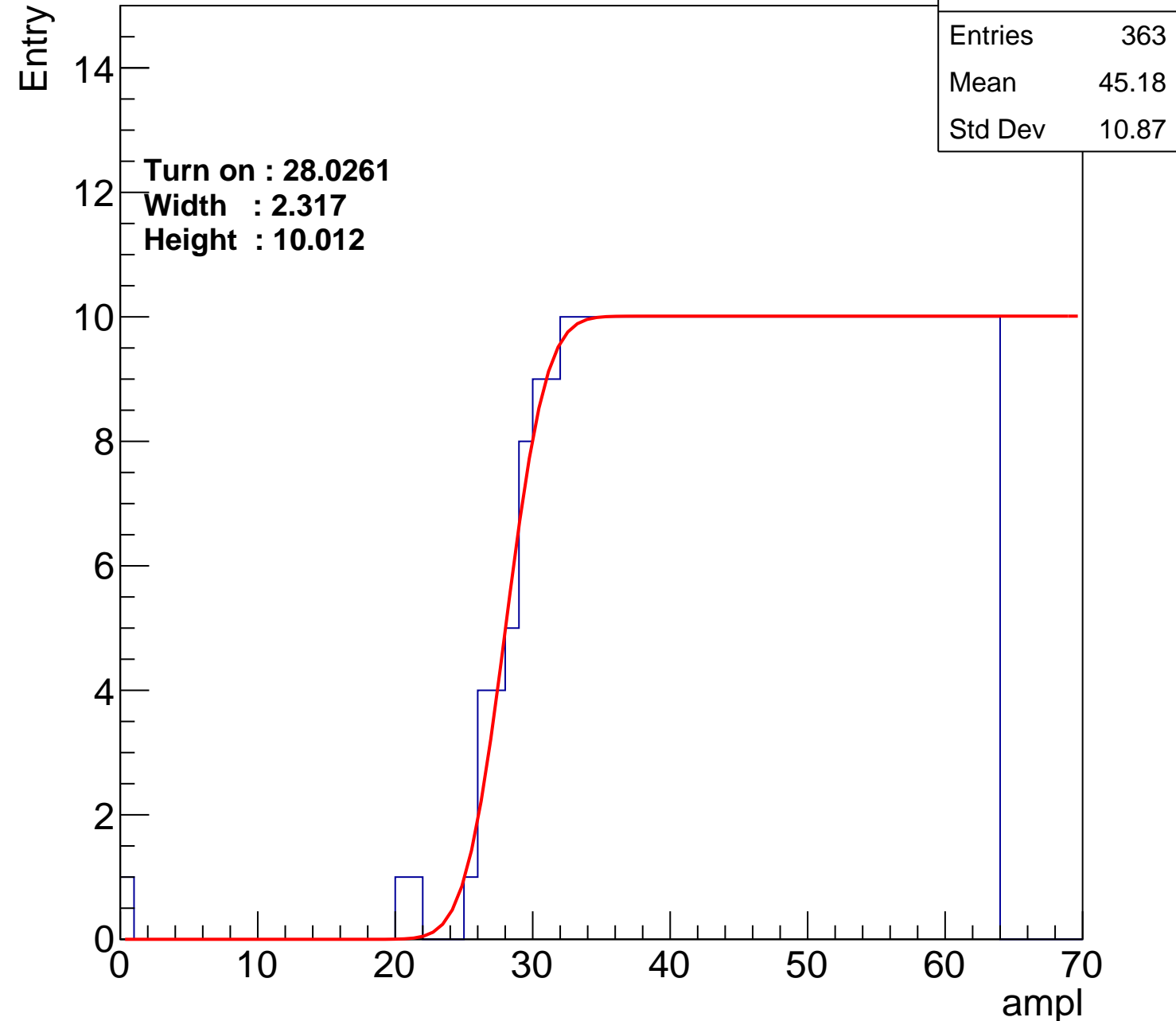
Width : 2.317

Height : 10.012

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch47

calib_packv5_042523_0143.root, FC#13, port D2

Entries	362
Mean	45.12
Std Dev	11.1

Turn on : 28.0425

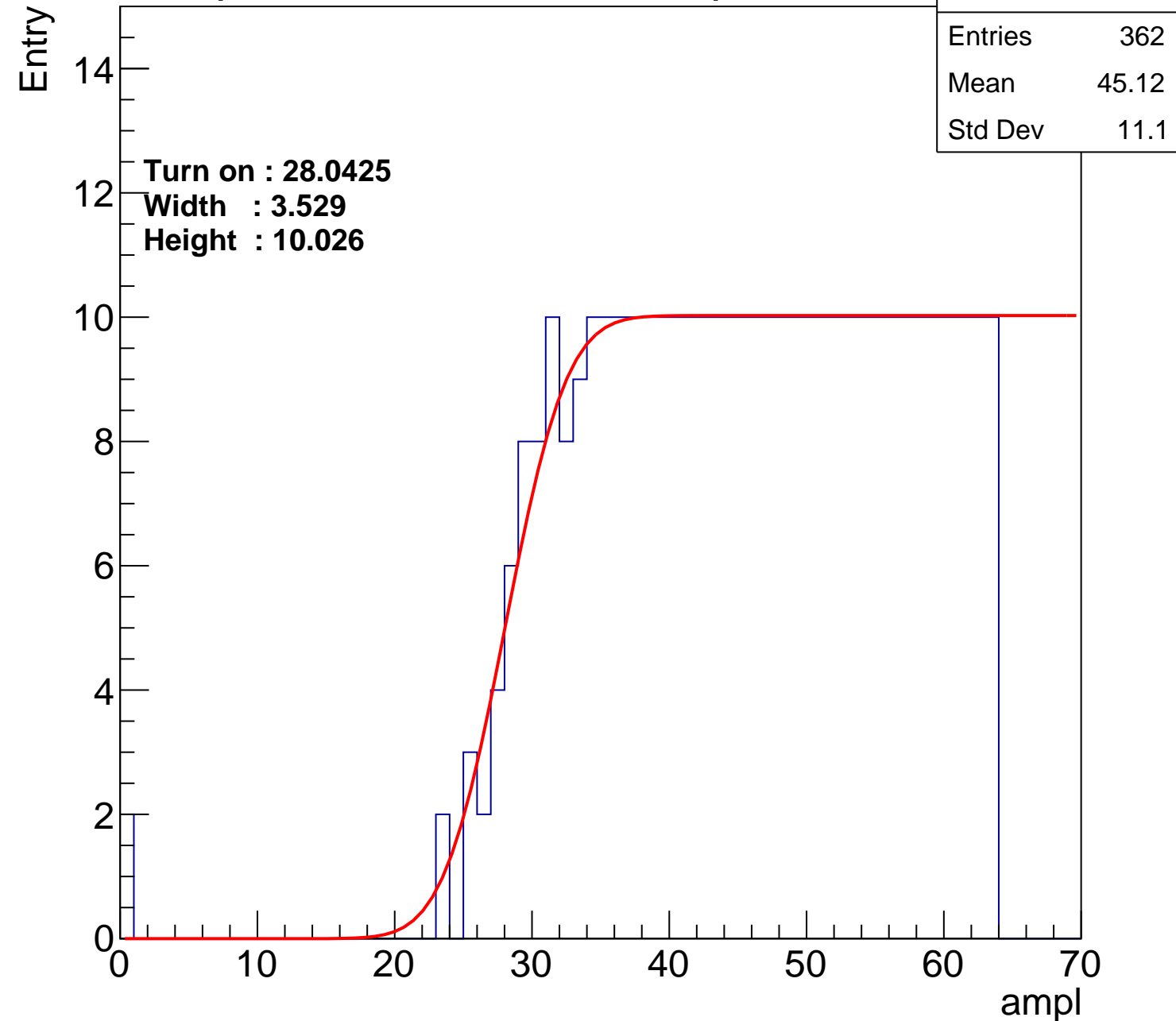
Width : 3.529

Height : 10.026

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch48

calib_packv5_042523_0143.root, FC#13, port D2

Entries	381
Mean	44.1
Std Dev	11.86

Turn on : 26.4082

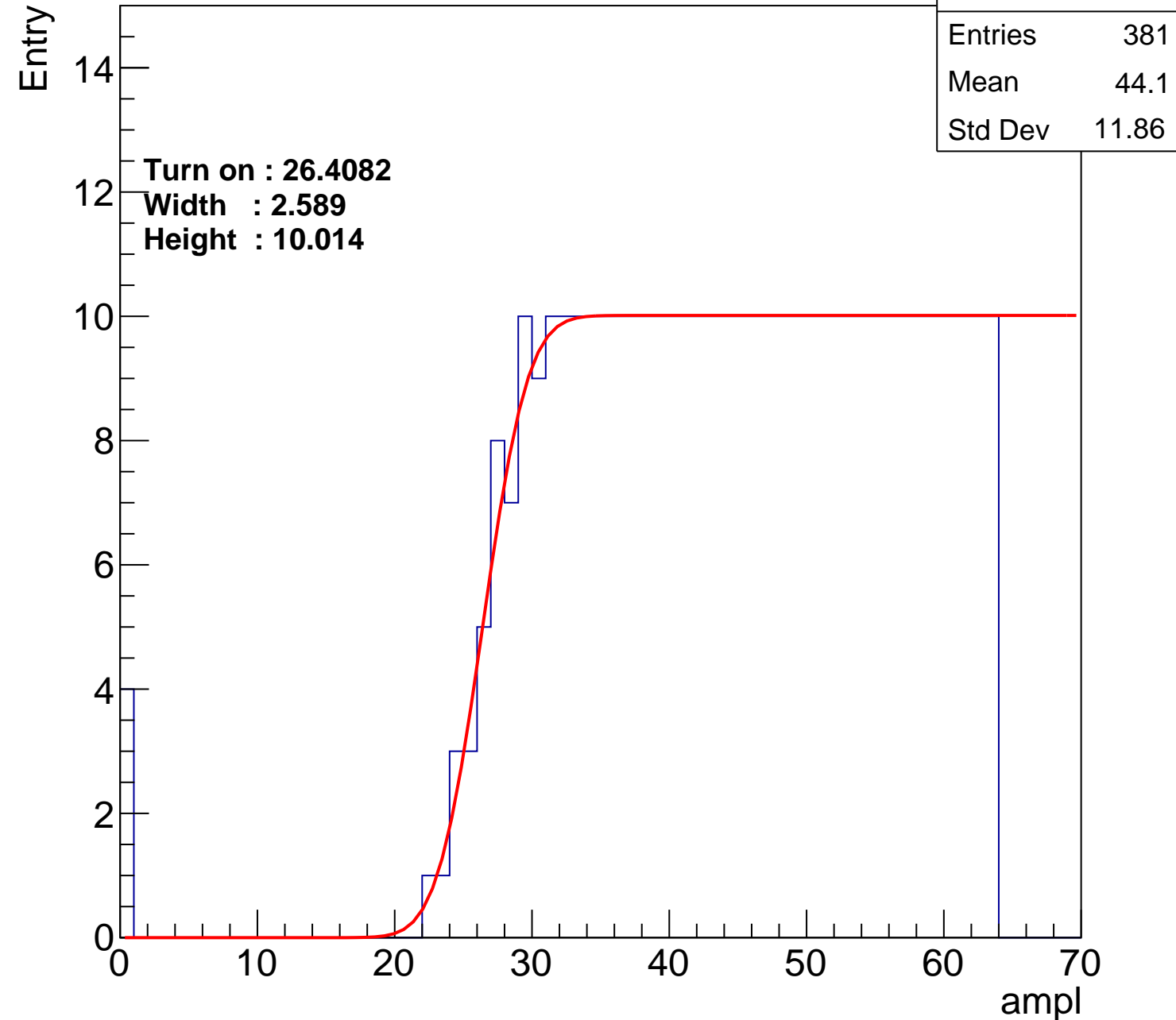
Width : 2.589

Height : 10.014

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch49

calib_packv5_042523_0143.root, FC#13, port D2

Entries	356
Mean	45.54
Std Dev	10.65

Turn on : 28.8032

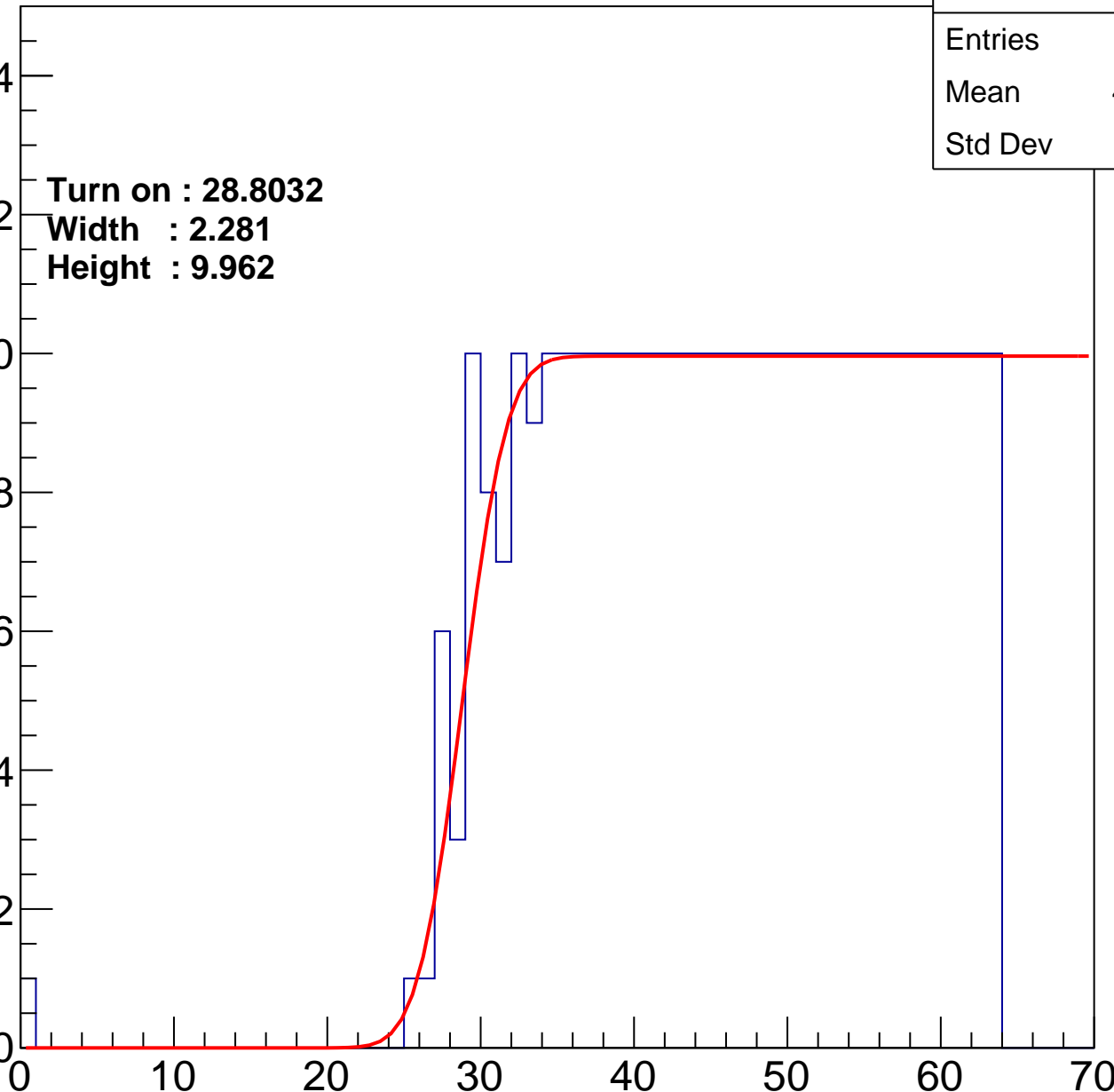
Width : 2.281

Height : 9.962

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch50

calib_packv5_042523_0143.root, FC#13, port D2

Entries	378
Mean	44.08
Std Dev	12.19

Turn on : 26.1503

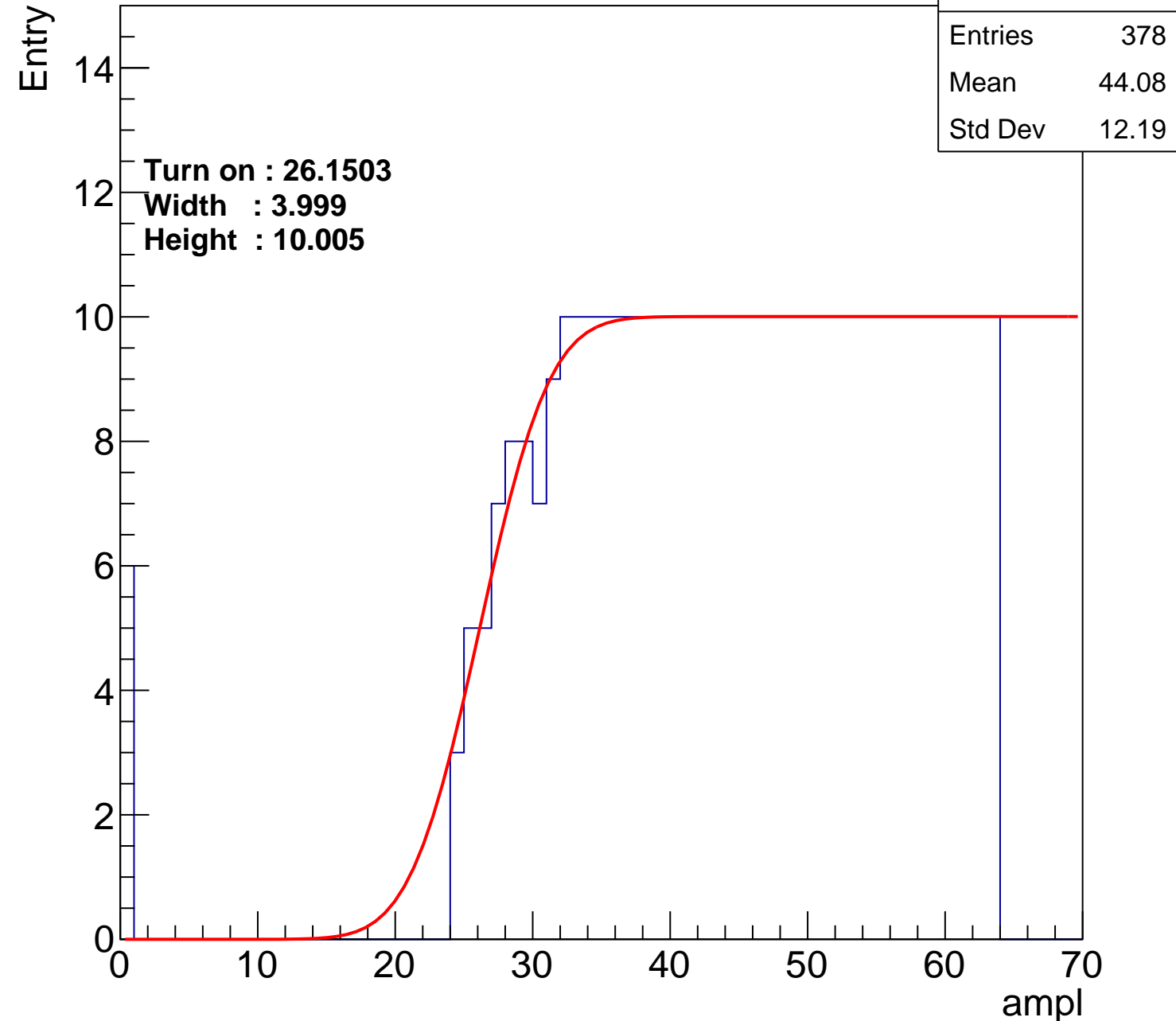
Width : 3.999

Height : 10.005

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch51

calib_packv5_042523_0143.root, FC#13, port D2

Entries	350
Mean	45.75
Std Dev	10.74

Turn on : 29.6975

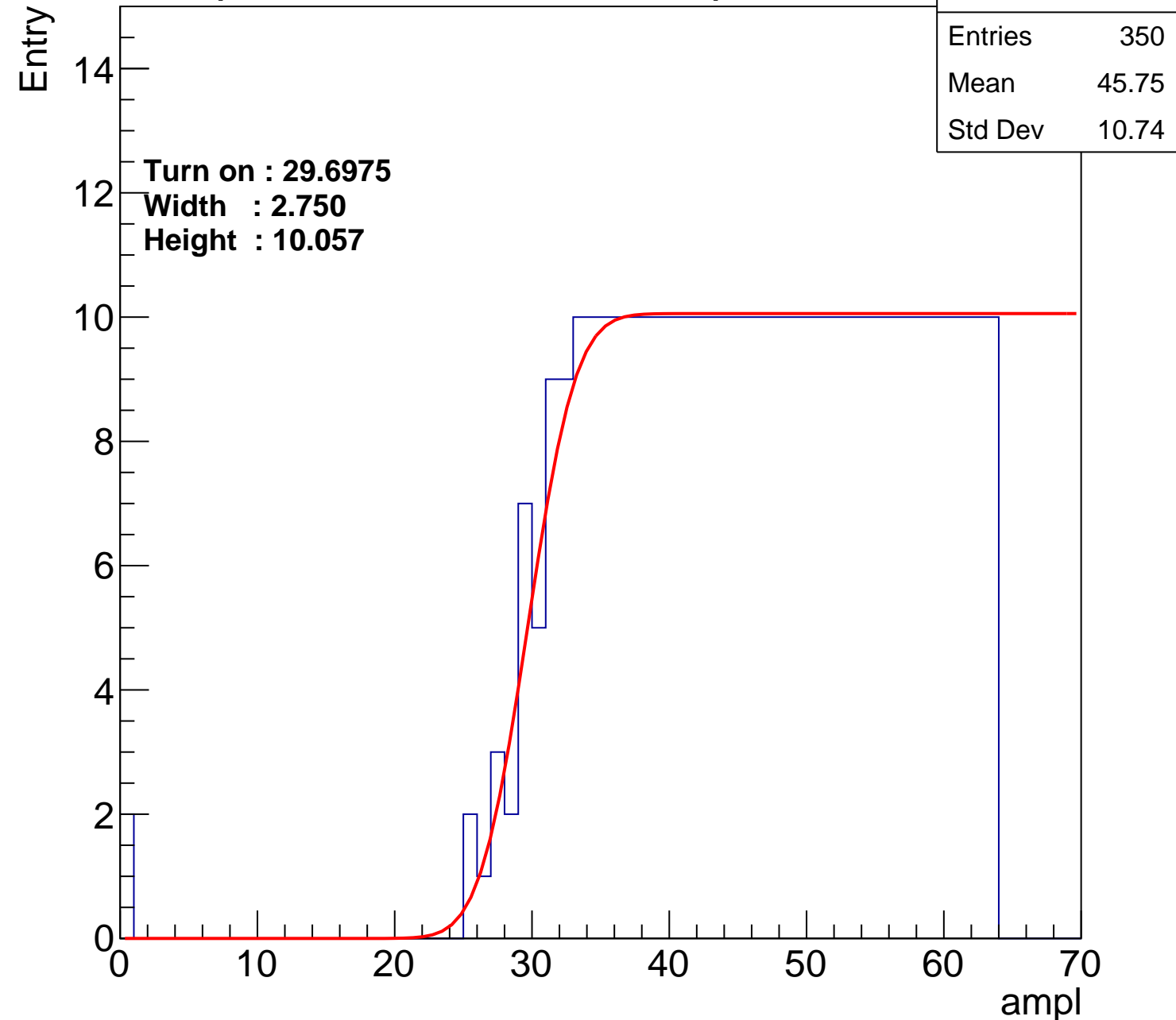
Width : 2.750

Height : 10.057

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch52

calib_packv5_042523_0143.root, FC#13, port D2

Entries	364
Mean	44.89
Std Dev	11.53

Turn on : 28.2849

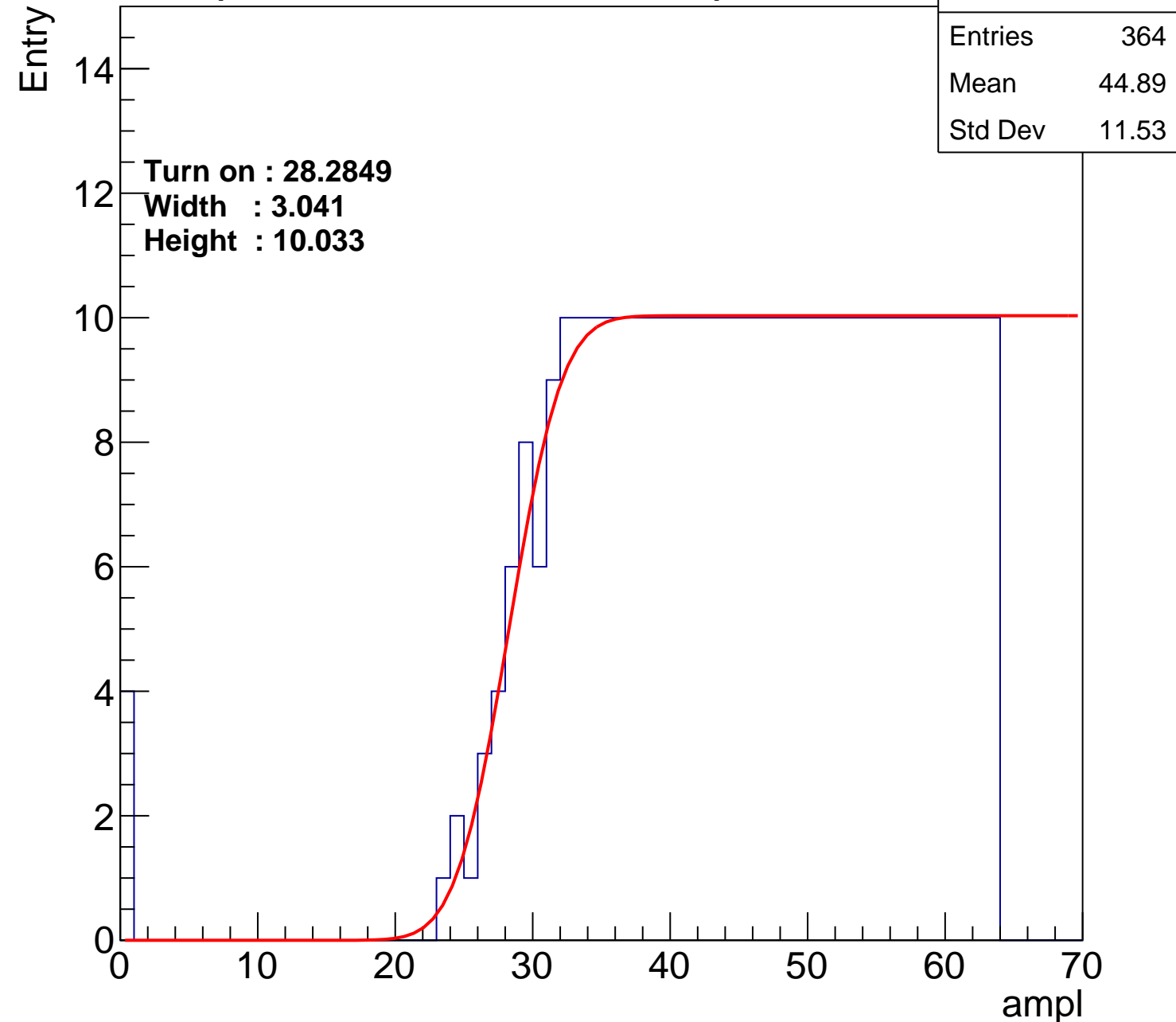
Width : 3.041

Height : 10.033

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch53

calib_packv5_042523_0143.root, FC#13, port D2

Entries	363
Mean	45.16
Std Dev	10.89

Turn on : 27.9997

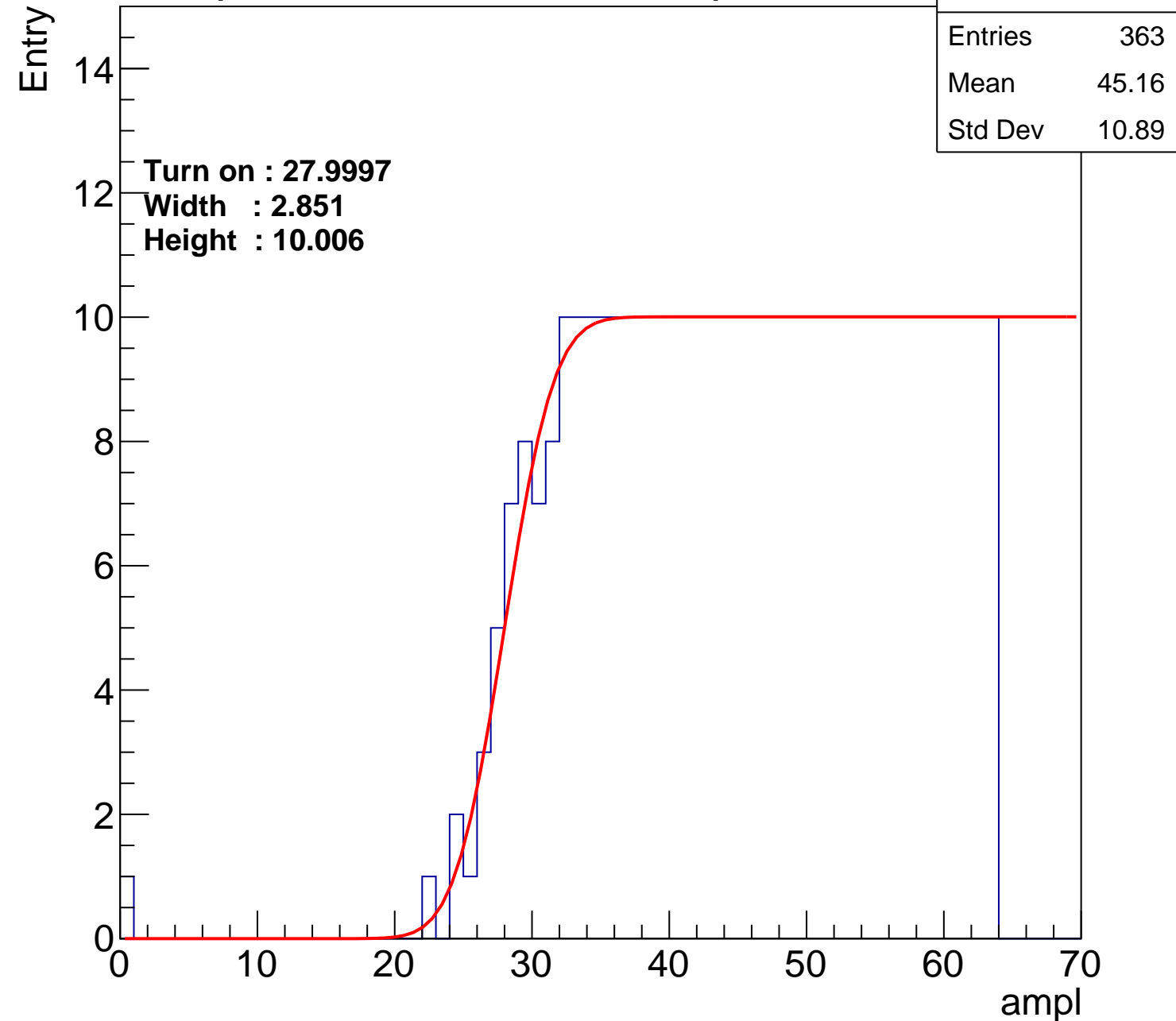
Width : 2.851

Height : 10.006

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch54

calib_packv5_042523_0143.root, FC#13, port D2

Entries	376
Mean	44.39
Std Dev	11.59

Turn on : 27.0701

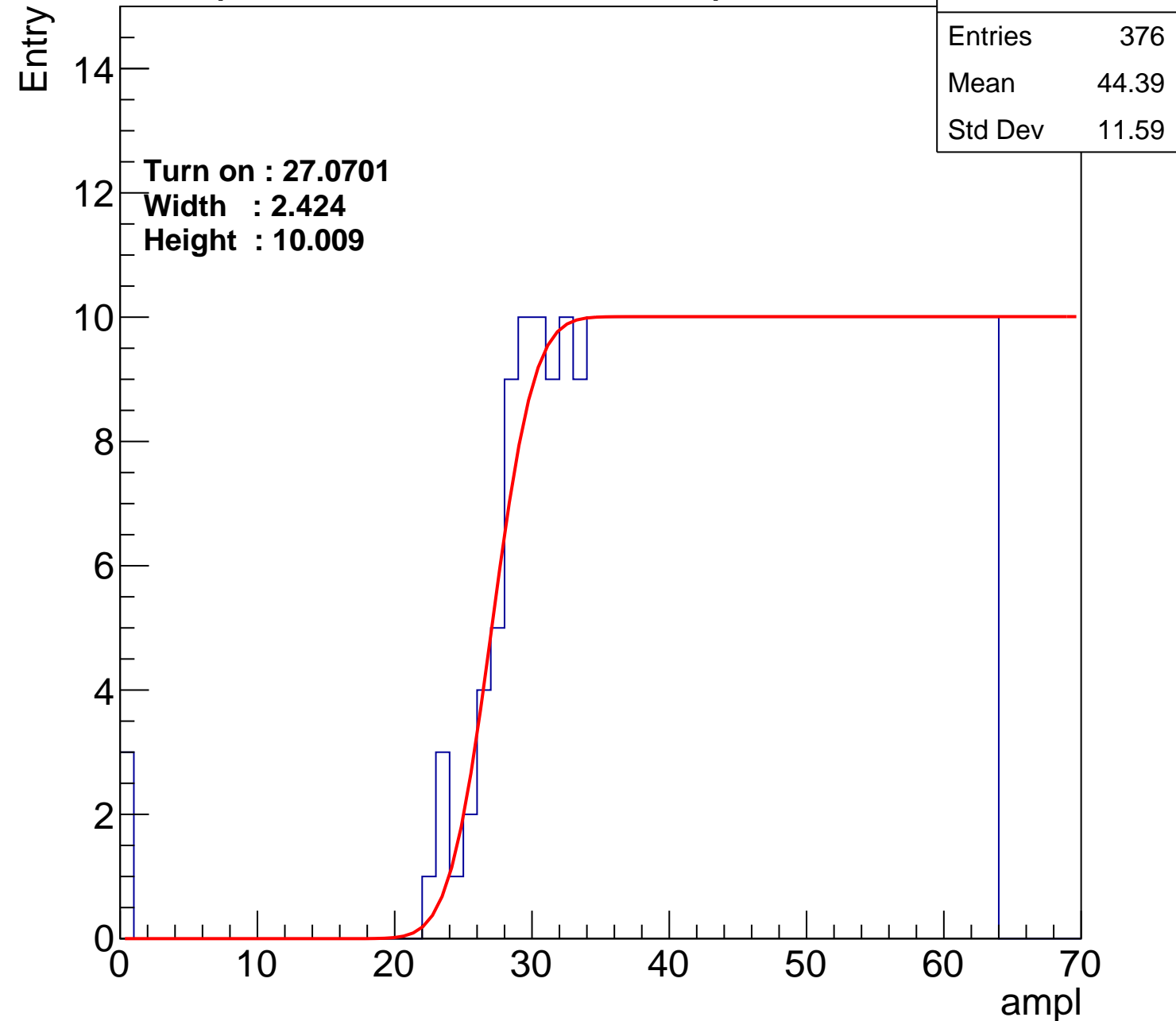
Width : 2.424

Height : 10.009

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch55

calib_packv5_042523_0143.root, FC#13, port D2

Entries	370
Mean	44.82
Std Dev	11.08

Turn on : 27.6407

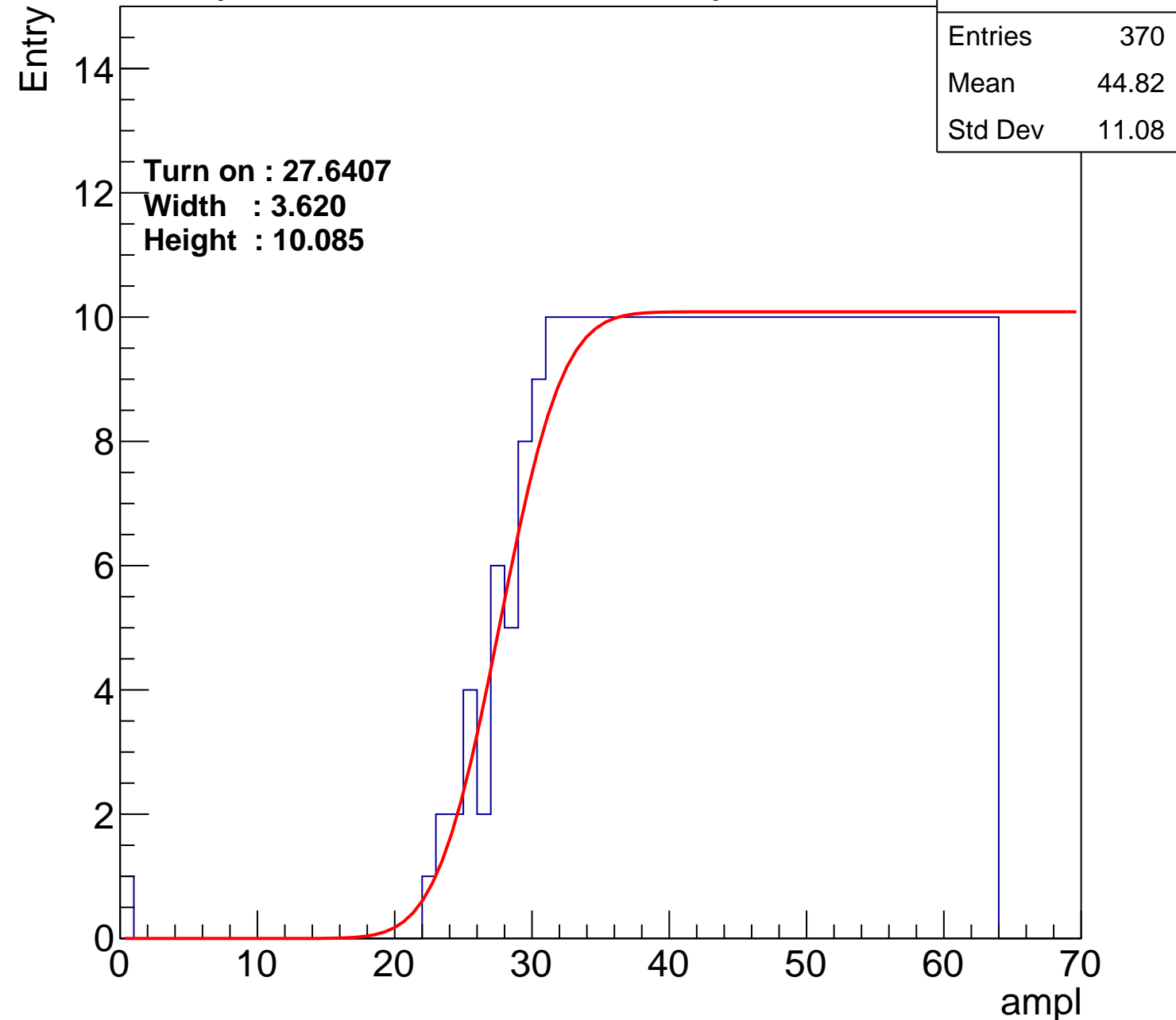
Width : 3.620

Height : 10.085

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch56

calib_packv5_042523_0143.root, FC#13, port D2

Entries	370
Mean	44.59
Std Dev	11.69

Turn on : 27.8589

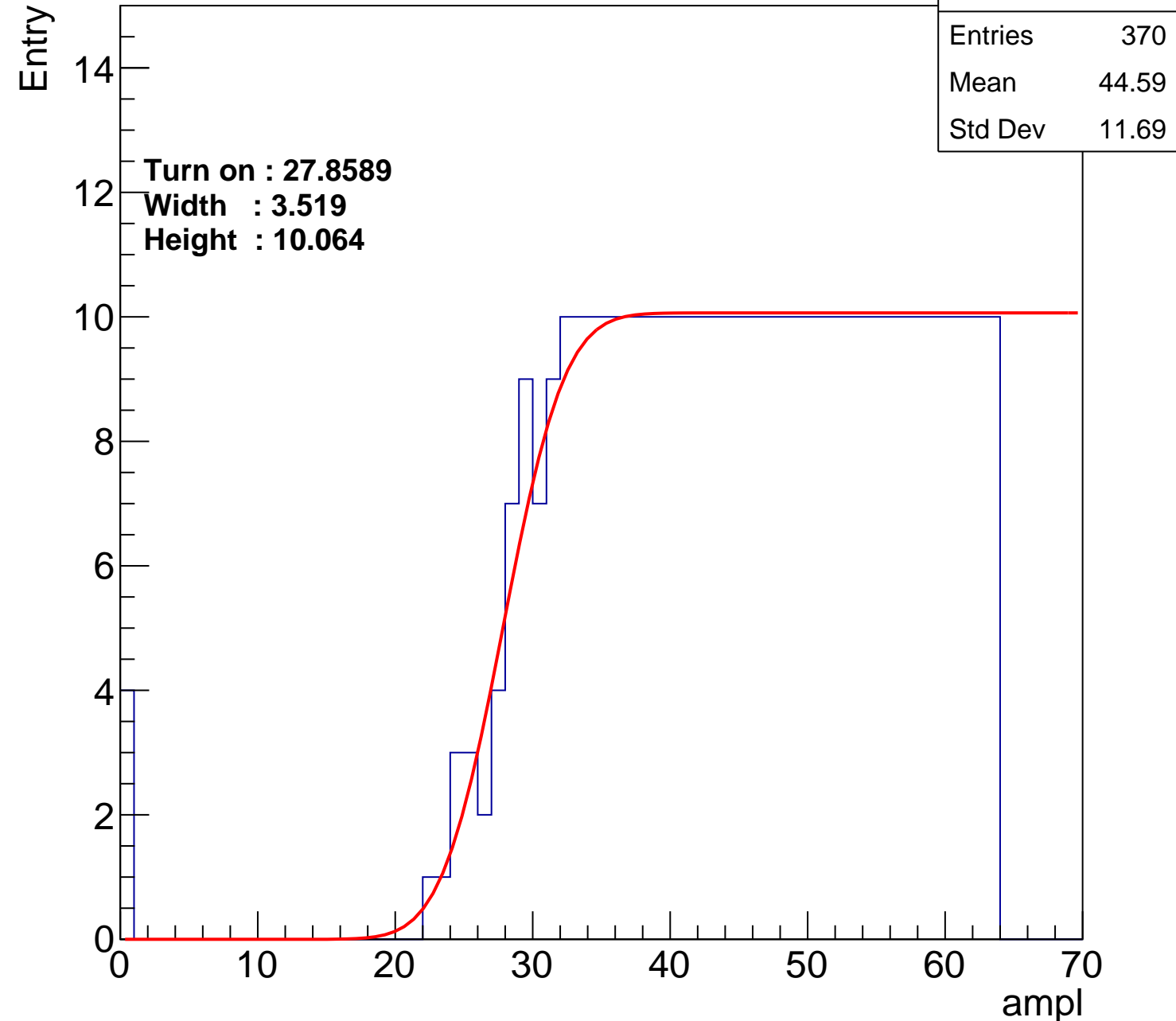
Width : 3.519

Height : 10.064

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch57

calib_packv5_042523_0143.root, FC#13, port D2

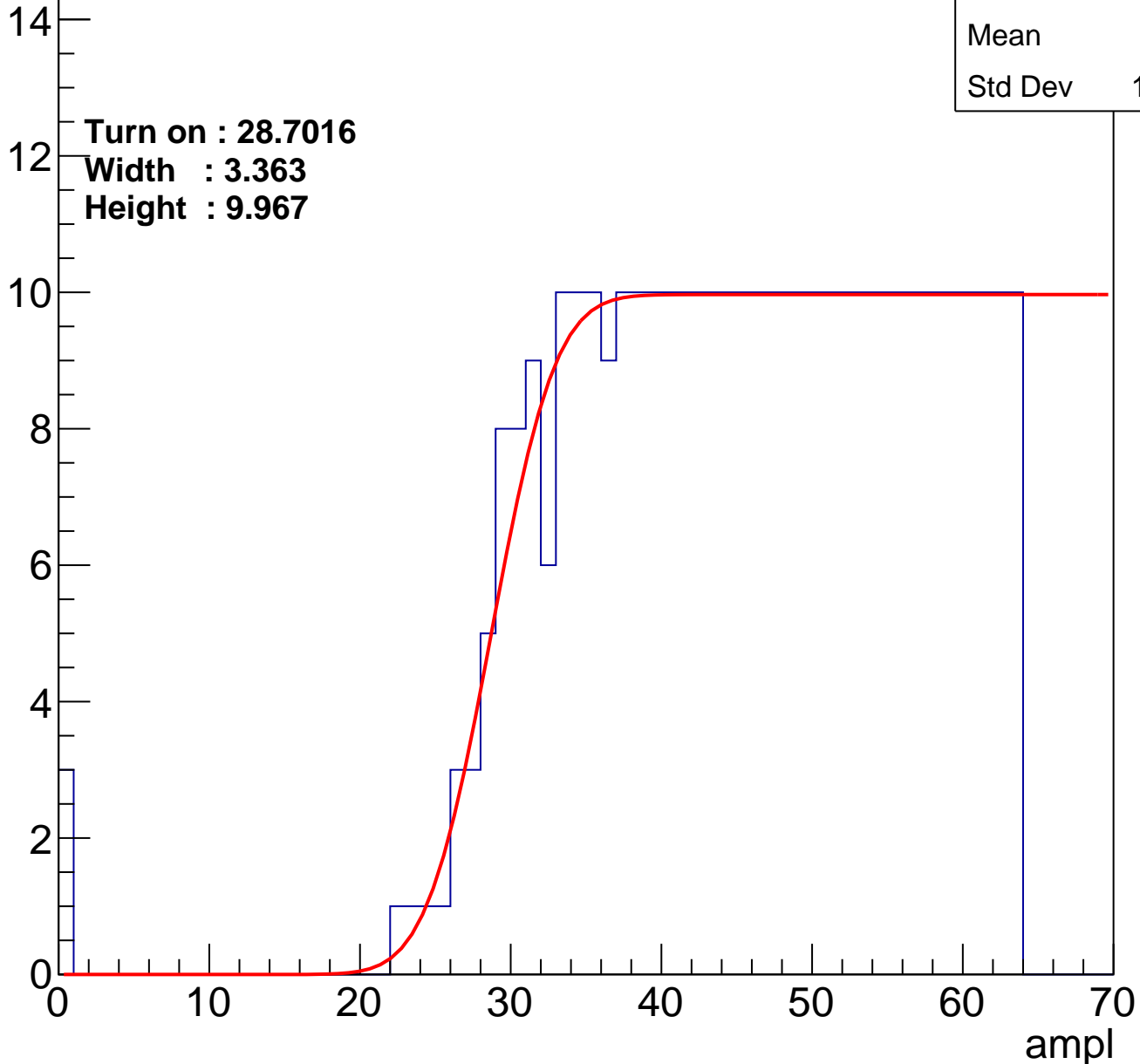
Entries	358
Mean	45.2
Std Dev	11.28

Turn on : 28.7016

Width : 3.363

Height : 9.967

Entry



B1L003S, U2-ch58

calib_packv5_042523_0143.root, FC#13, port D2

Entries	348
Mean	45.81
Std Dev	10.75

Turn on : 29.3799

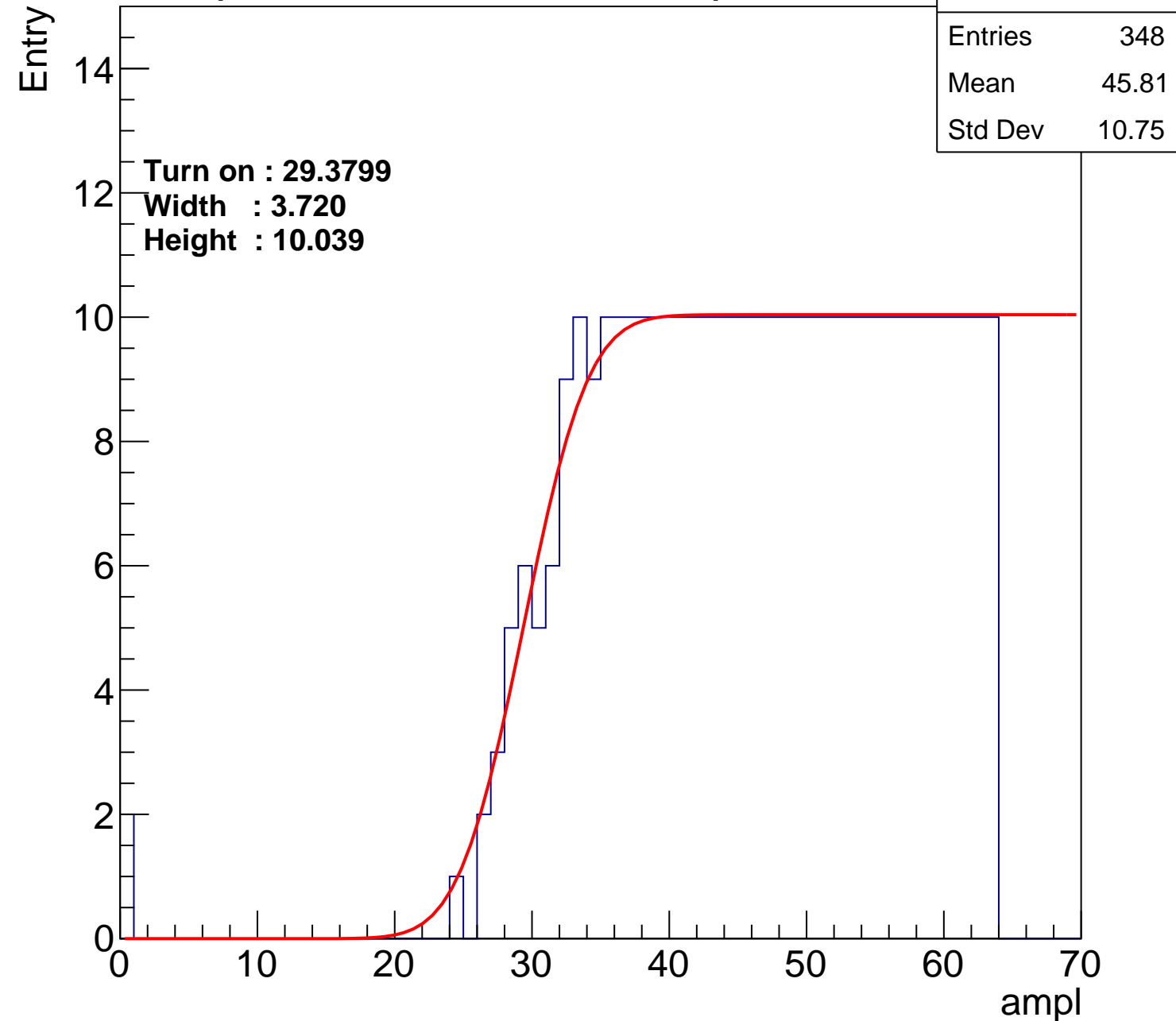
Width : 3.720

Height : 10.039

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch59

calib_packv5_042523_0143.root, FC#13, port D2

Entries	368
Mean	44.91
Std Dev	11.03

Turn on : 27.6918

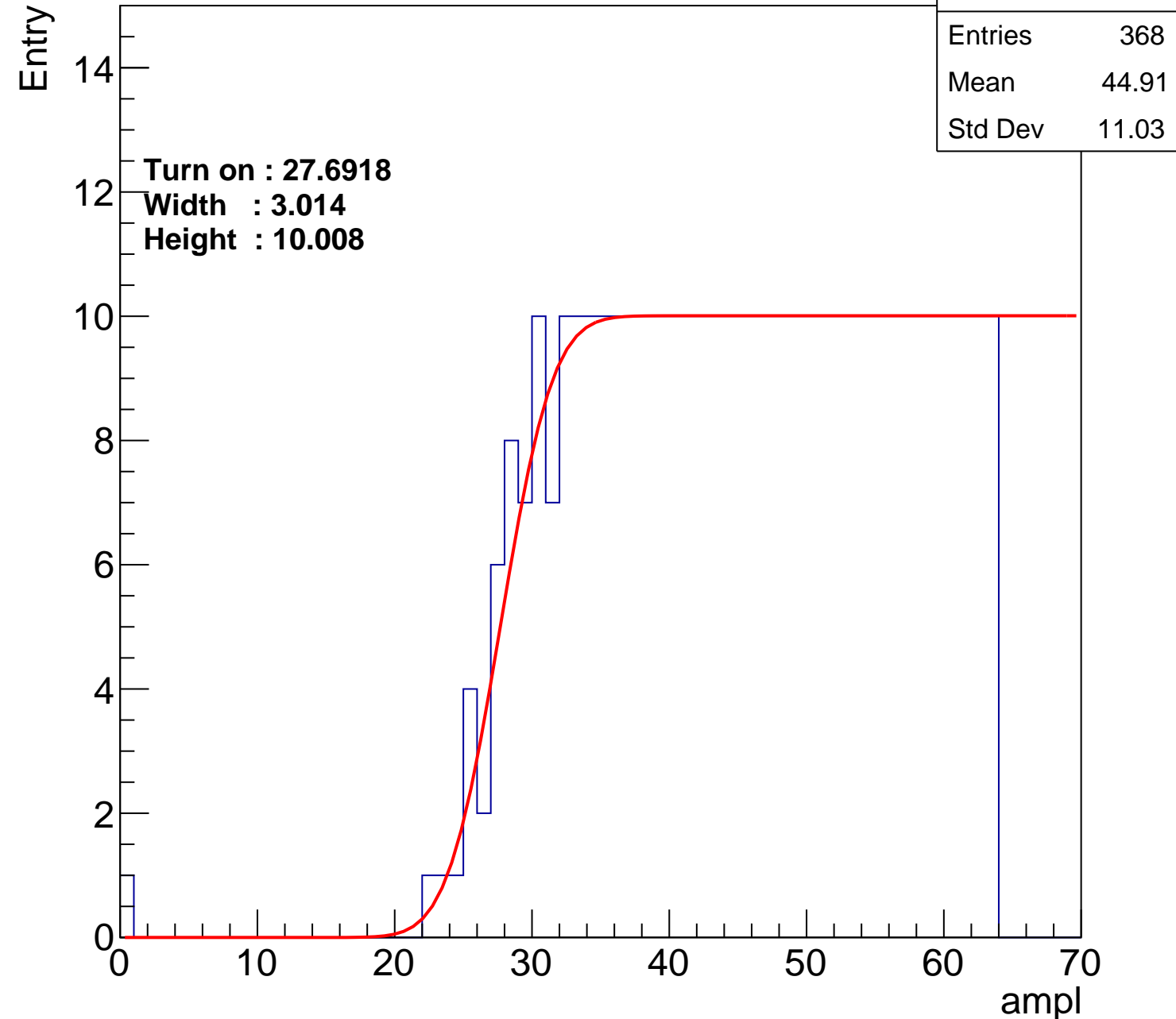
Width : 3.014

Height : 10.008

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch60

calib_packv5_042523_0143.root, FC#13, port D2

Entries	357
Mean	45.38
Std Dev	10.95

Turn on : 28.5461

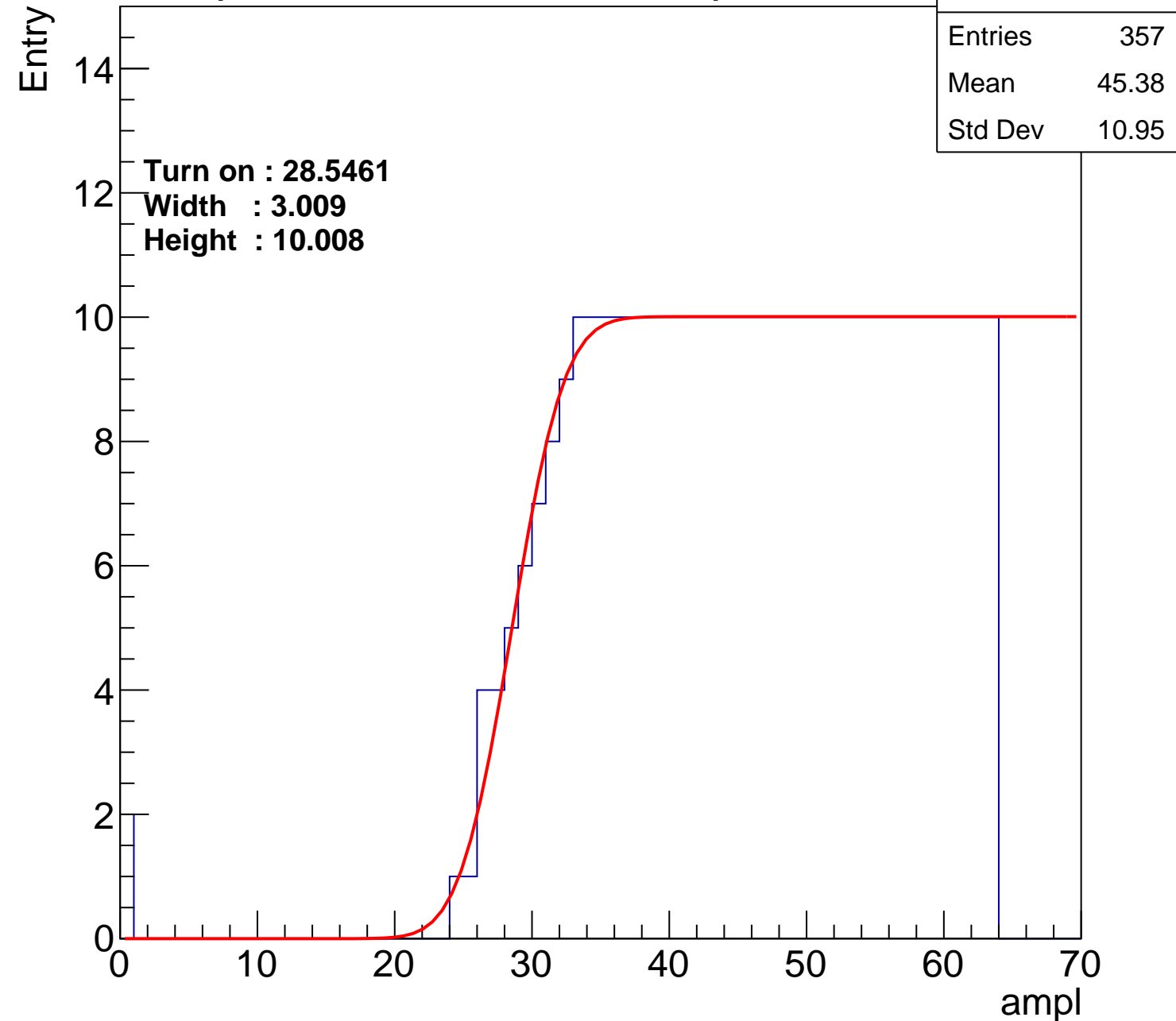
Width : 3.009

Height : 10.008

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch61

calib_packv5_042523_0143.root, FC#13, port D2

Entries	369
Mean	44.66
Std Dev	11.62

Turn on : 27.1093

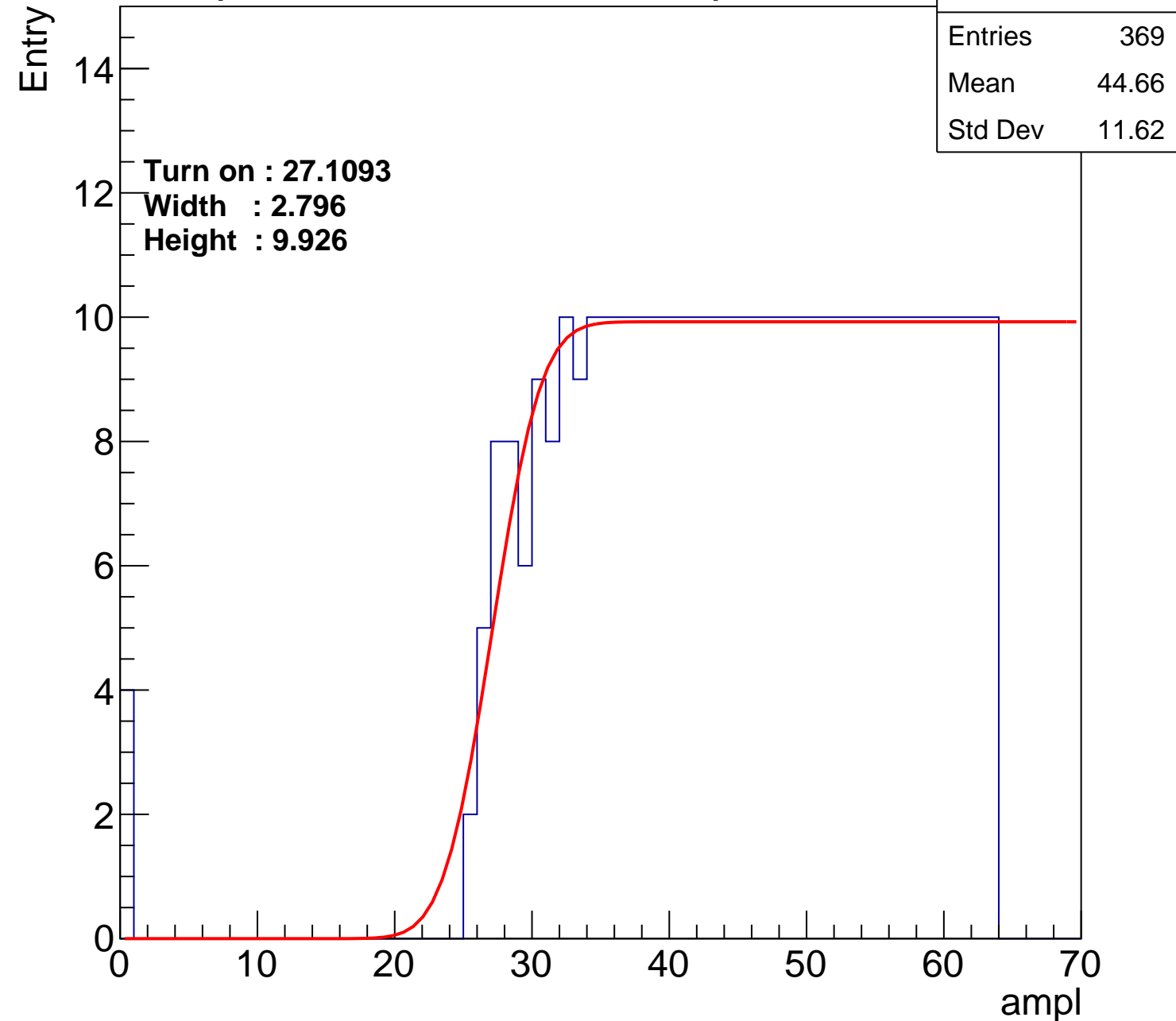
Width : 2.796

Height : 9.926

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch62

calib_packv5_042523_0143.root, FC#13, port D2

Entries	392
Mean	43.67
Std Dev	11.9

Turn on : 25.0632

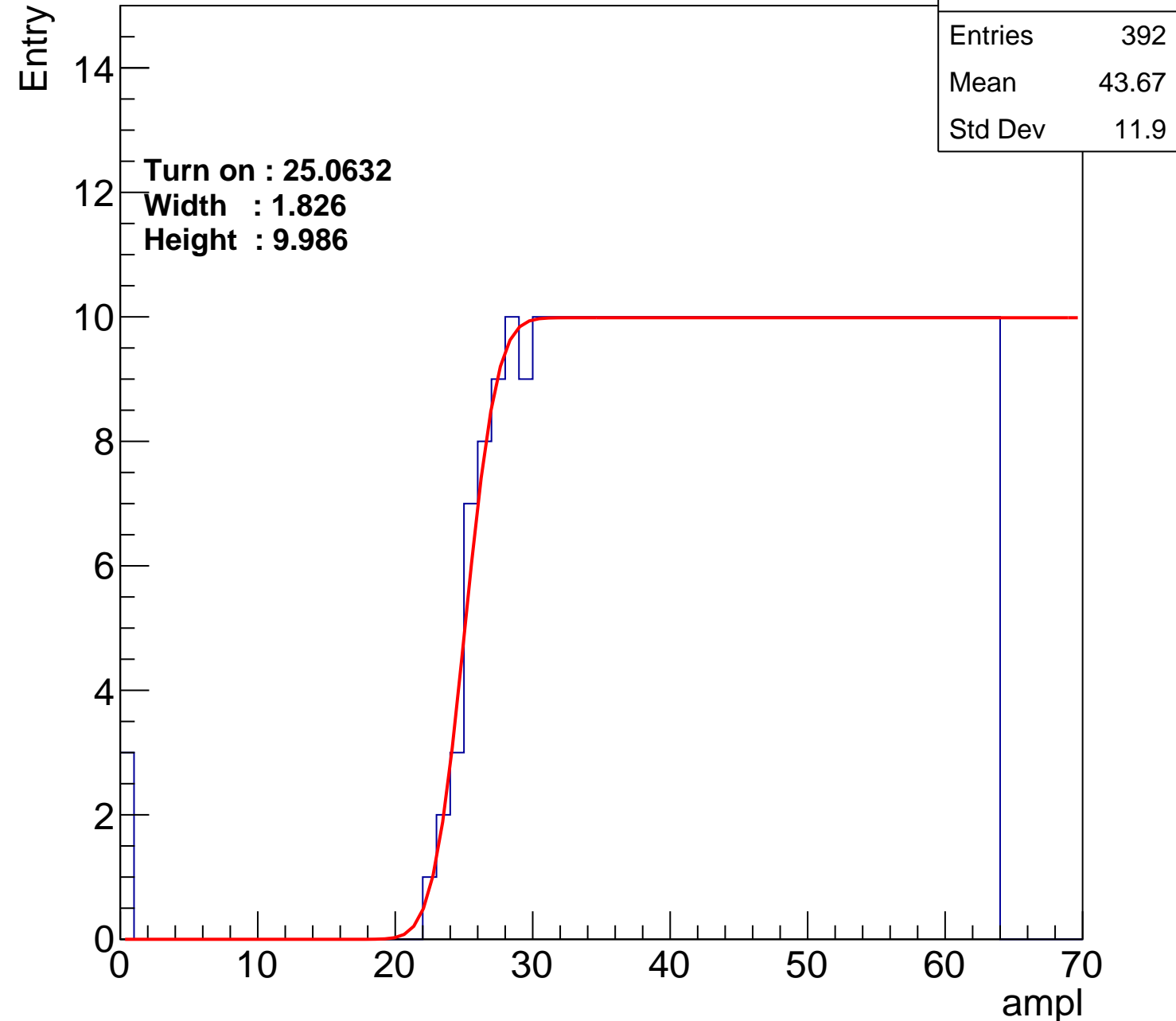
Width : 1.826

Height : 9.986

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch63

calib_packv5_042523_0143.root, FC#13, port D2

Entries	370
Mean	44.85
Std Dev	11.01

Turn on : 27.1001

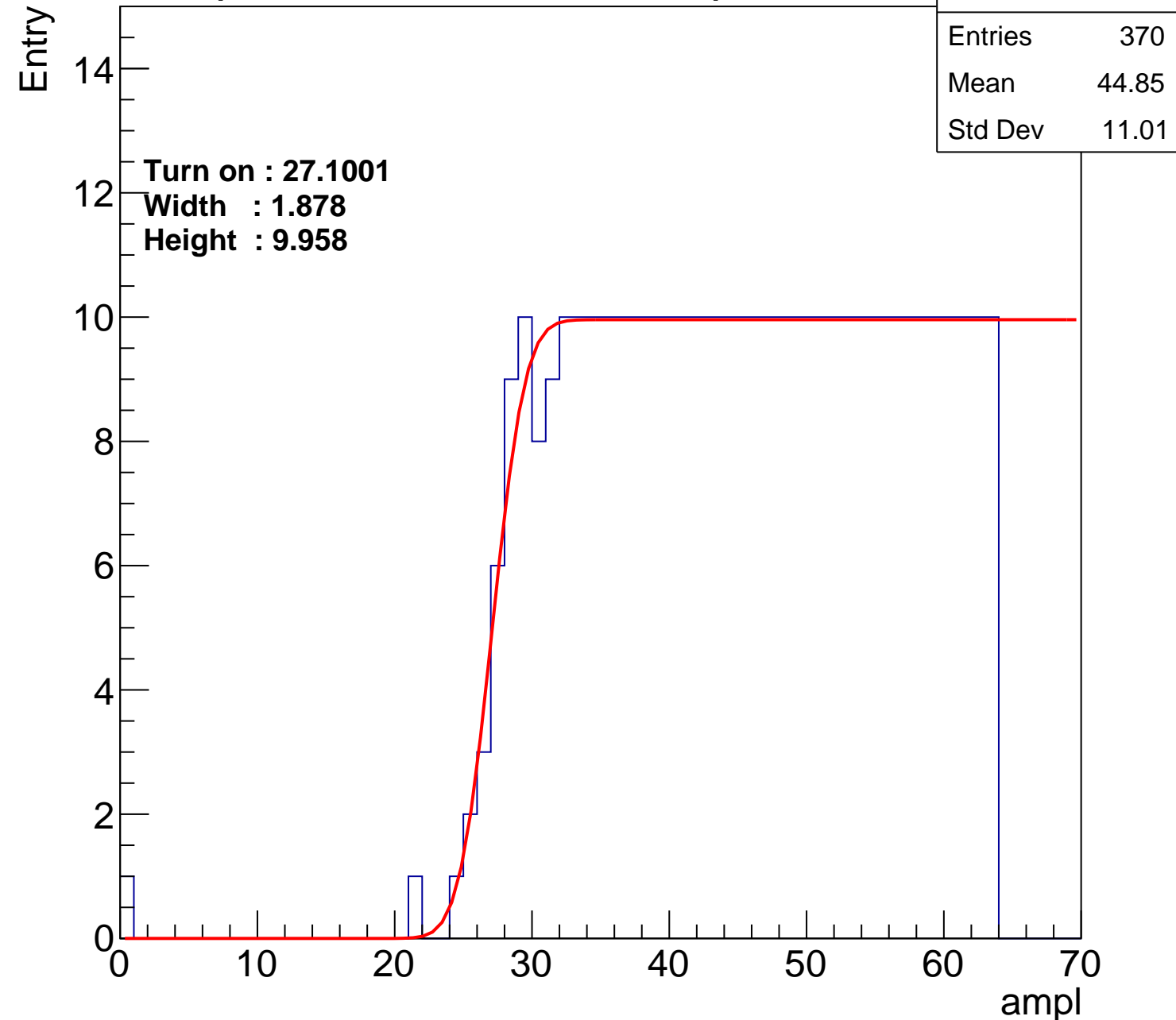
Width : 1.878

Height : 9.958

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch64

calib_packv5_042523_0143.root, FC#13, port D2

Entries	385
Mean	43.75
Std Dev	12.32

Turn on : 26.3056

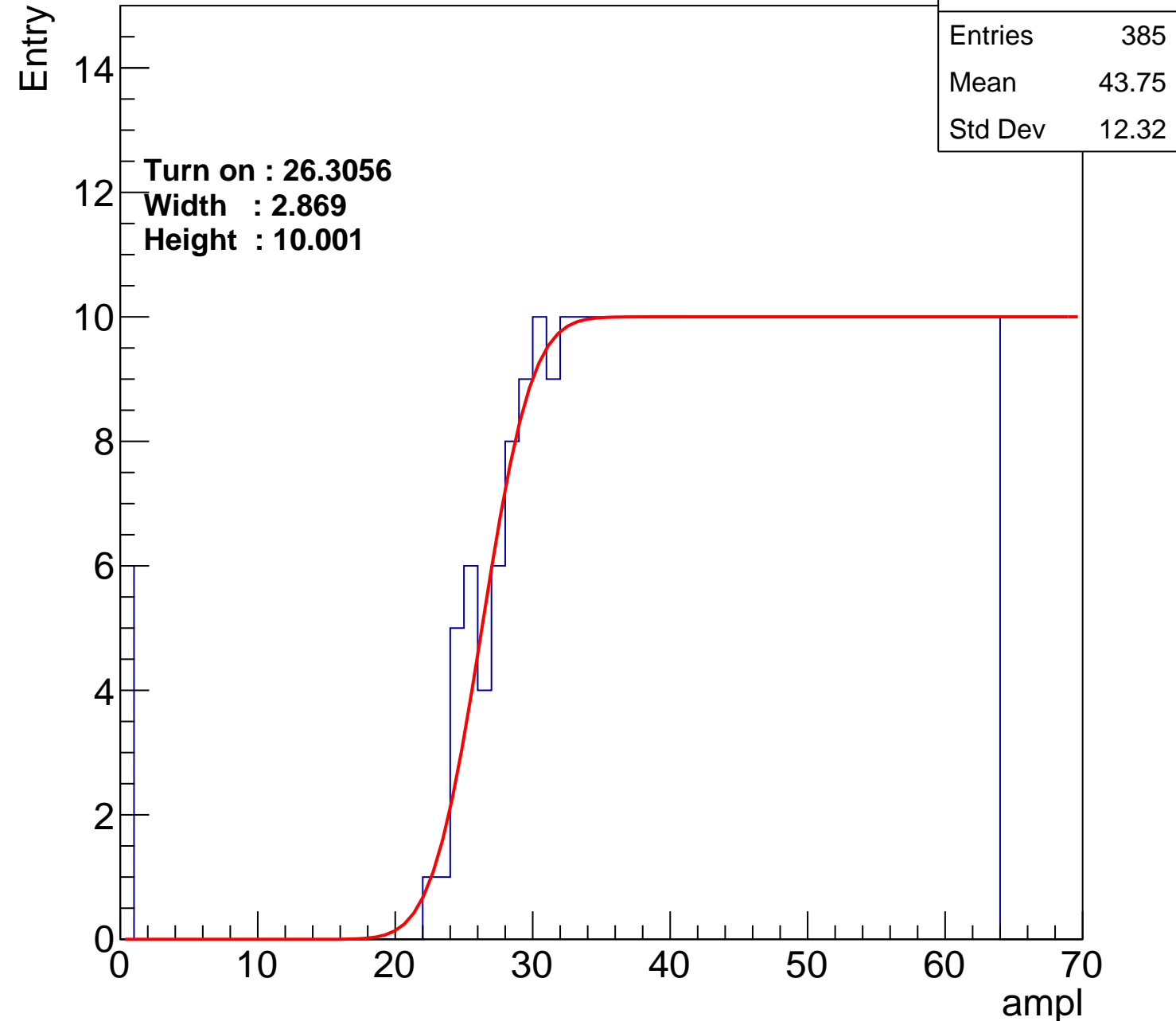
Width : 2.869

Height : 10.001

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch65

calib_packv5_042523_0143.root, FC#13, port D2

Entries	366
Mean	44.77
Std Dev	11.61

Turn on : 27.7255

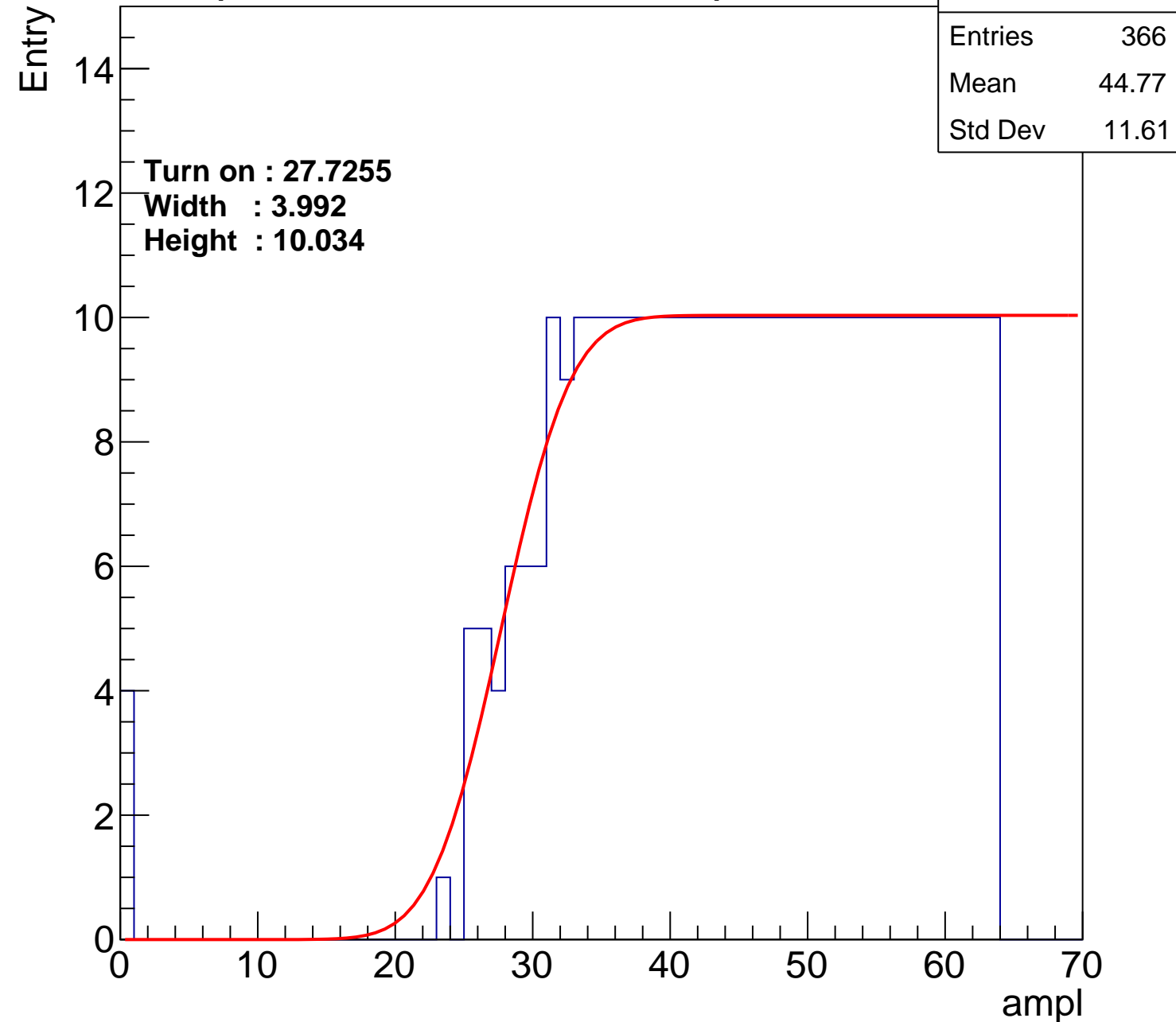
Width : 3.992

Height : 10.034

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch66

calib_packv5_042523_0143.root, FC#13, port D2

Entries	376
Mean	44.29
Std Dev	11.85

Turn on : 27.5111

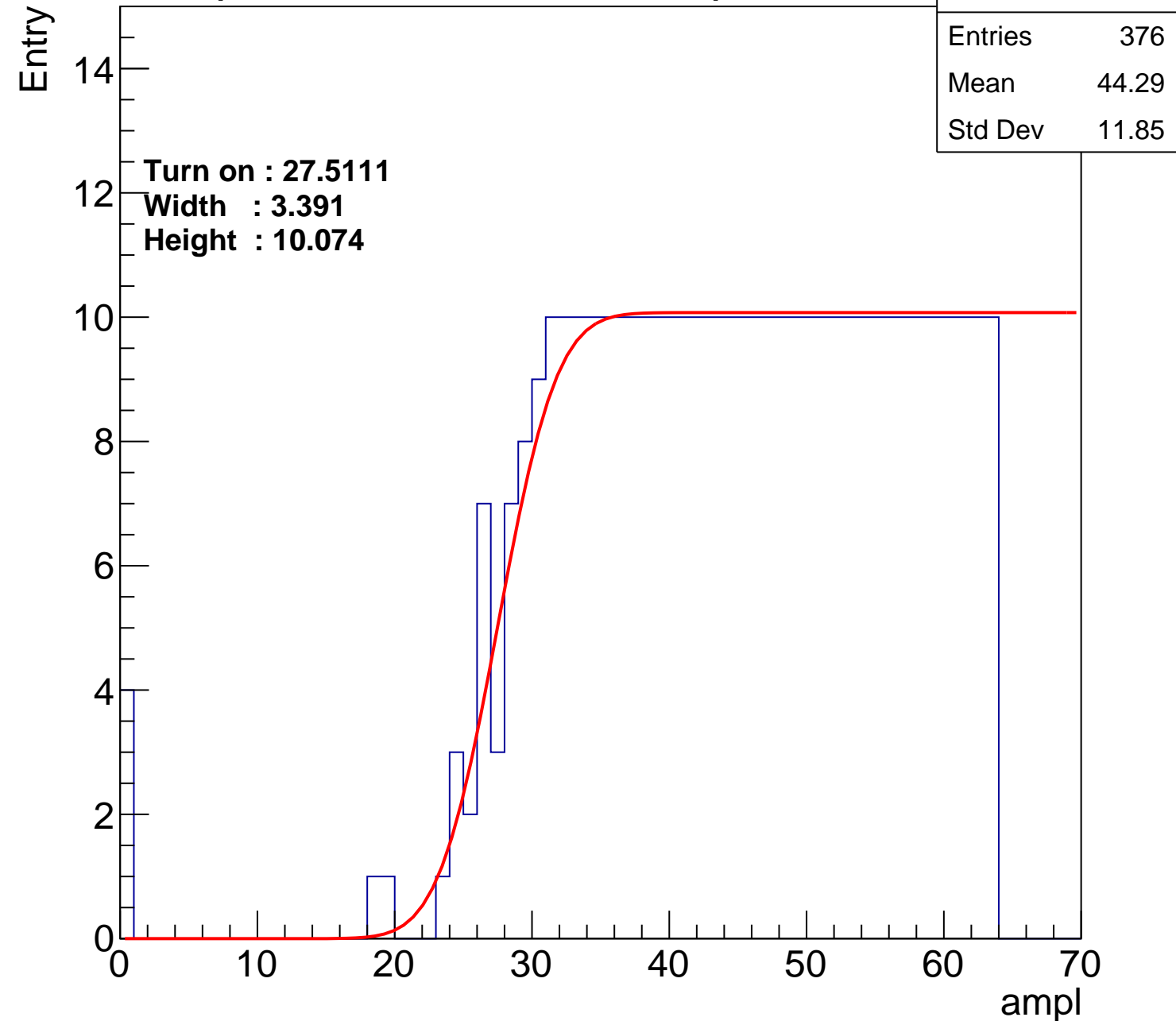
Width : 3.391

Height : 10.074

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch67

calib_packv5_042523_0143.root, FC#13, port D2

Entries	374
Mean	44.54
Std Dev	11.48

Turn on : 27.2061

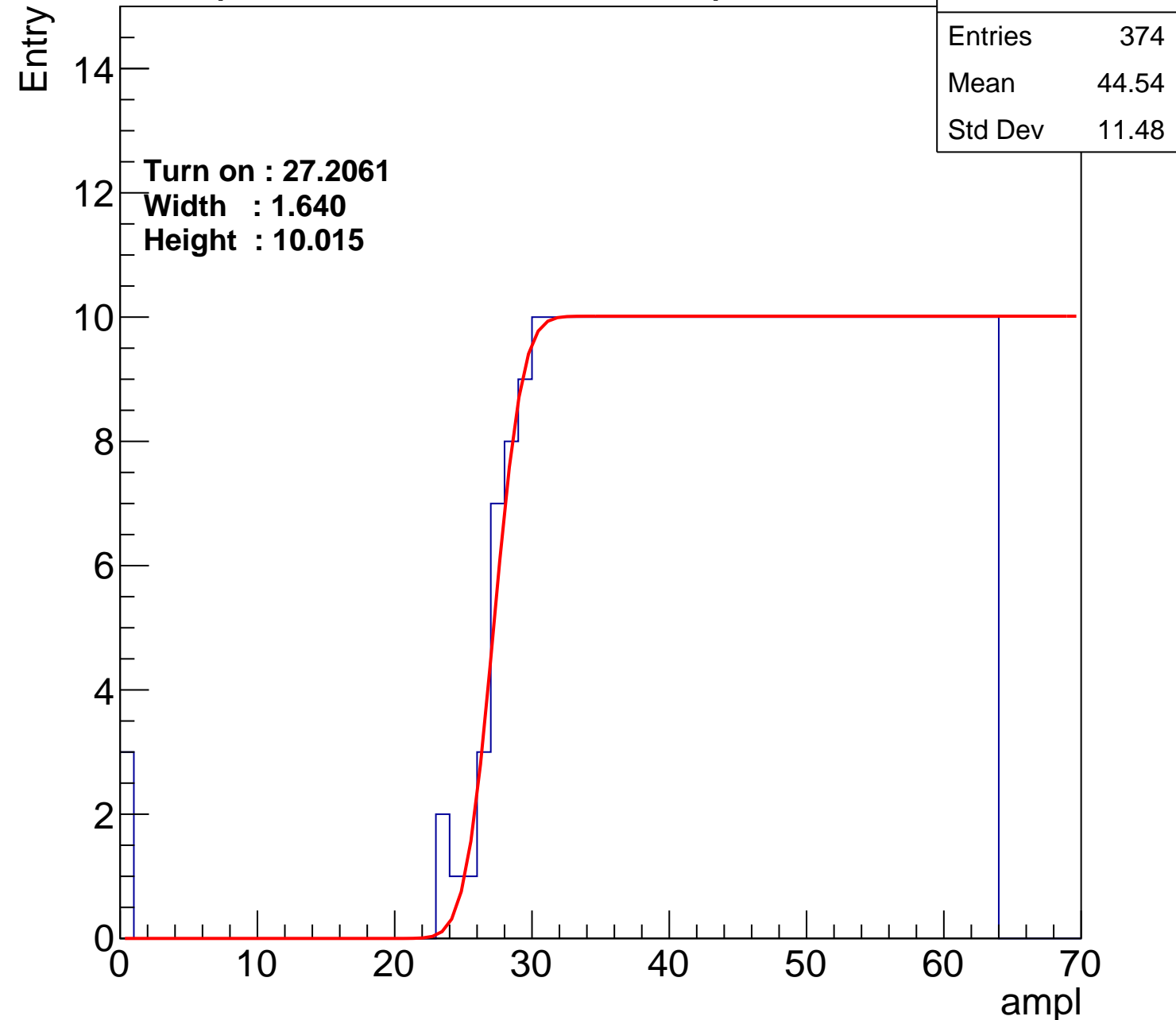
Width : 1.640

Height : 10.015

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch68

calib_packv5_042523_0143.root, FC#13, port D2

Entries	384
Mean	44.01
Std Dev	11.78

Turn on : 26.1676

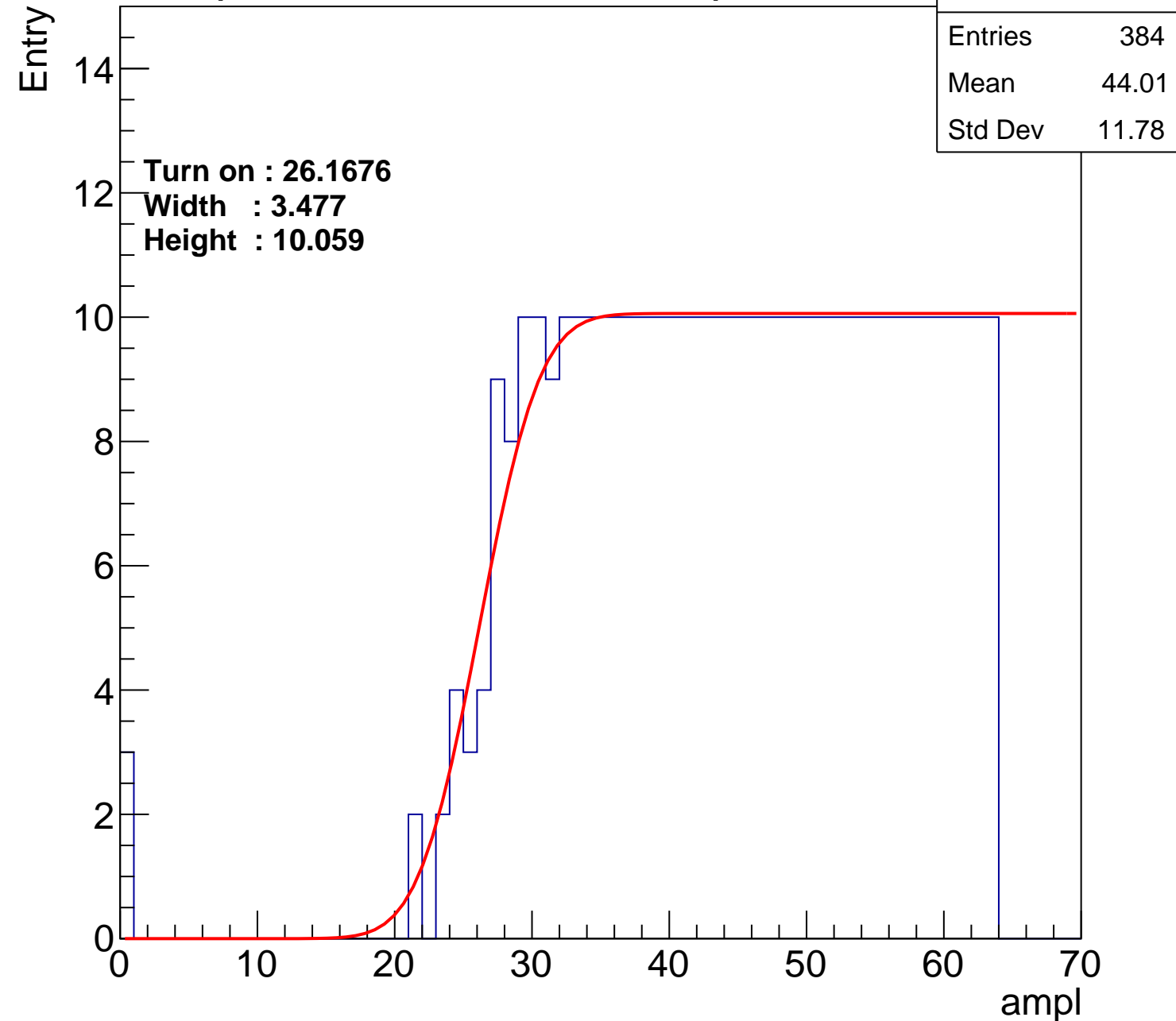
Width : 3.477

Height : 10.059

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch69

calib_packv5_042523_0143.root, FC#13, port D2

Entries	342
Mean	46.17
Std Dev	10.38

Turn on : 30.1809

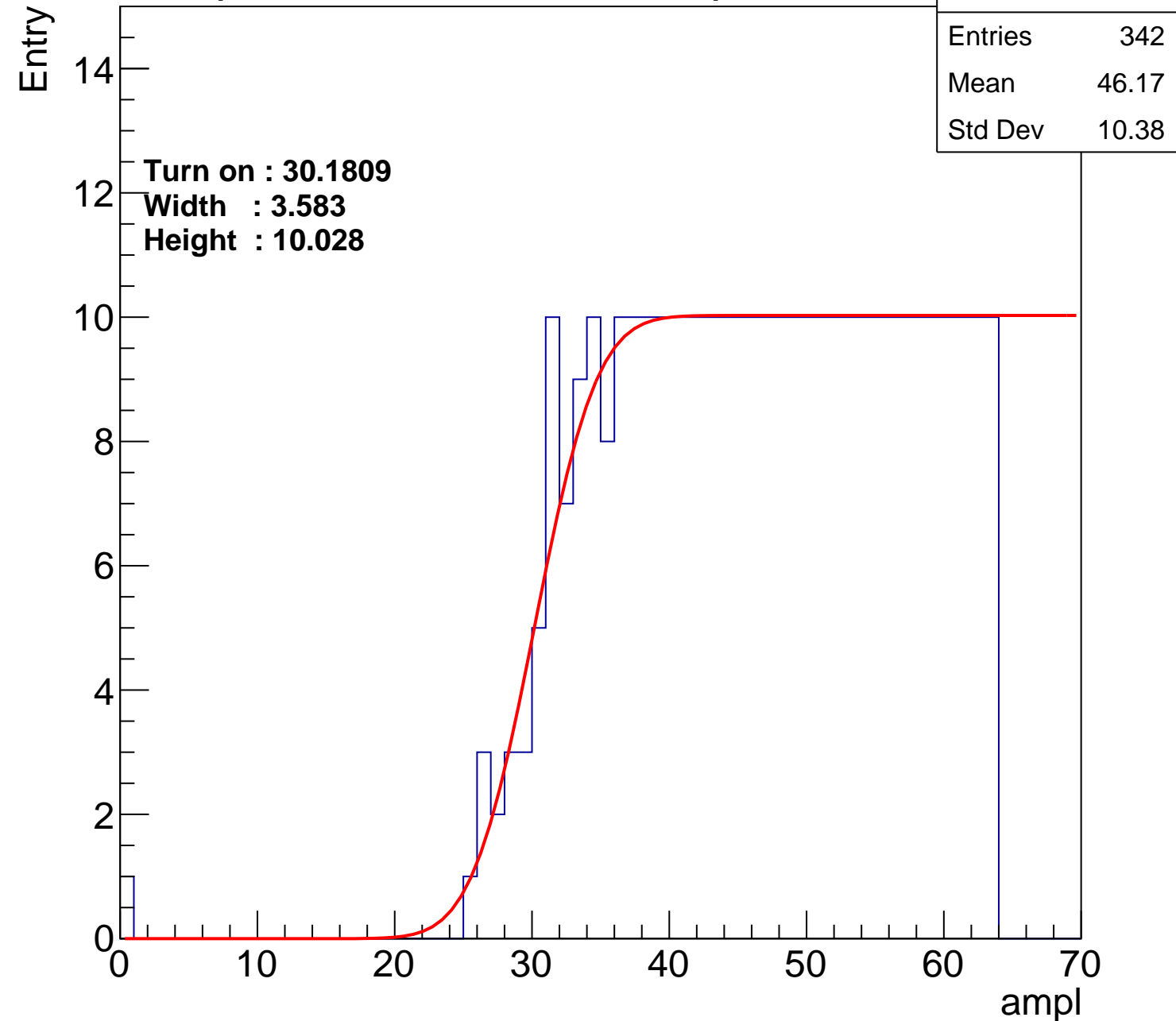
Width : 3.583

Height : 10.028

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch70

calib_packv5_042523_0143.root, FC#13, port D2

Entries	354
Mean	45.49
Std Dev	11.04

Turn on : 29.2134

Width : 2.008

Height : 9.994

Entry

14

12

10

8

6

4

2

0

0

10

20

30

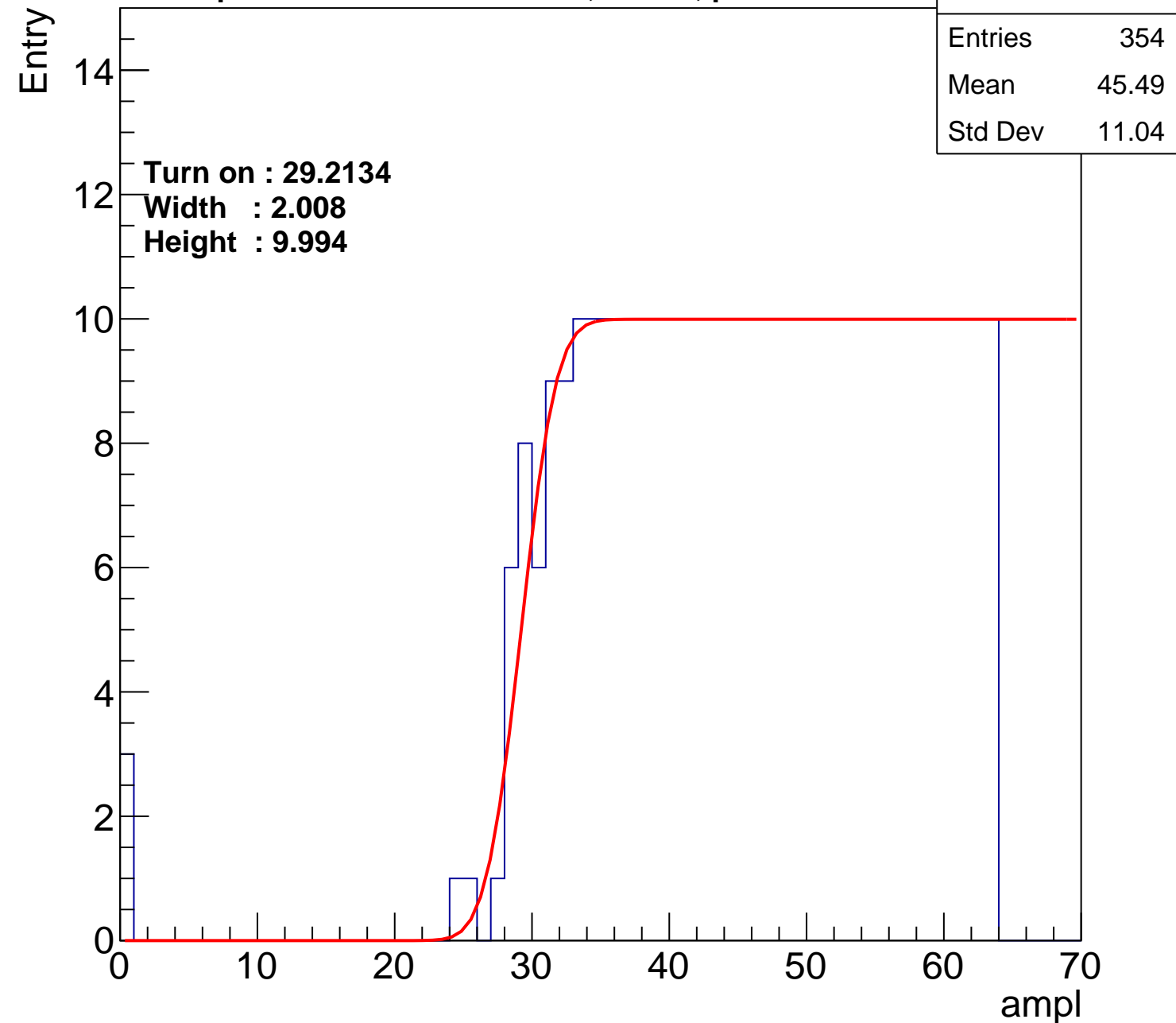
40

50

60

70

ampl



B1L003S, U2-ch71

calib_packv5_042523_0143.root, FC#13, port D2

Entries	374
Mean	44.55
Std Dev	11.38

Turn on : 27.3558

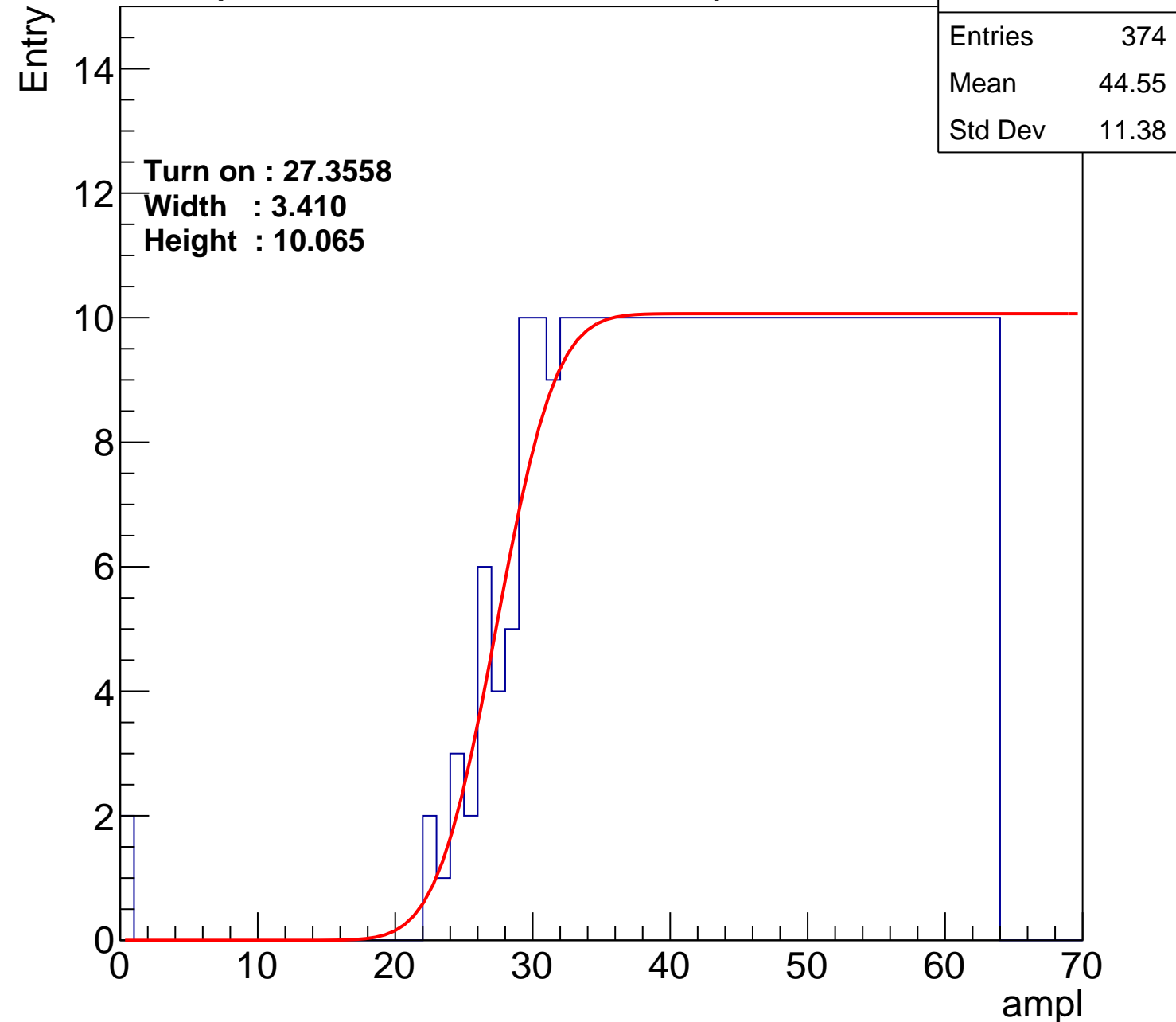
Width : 3.410

Height : 10.065

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch72

calib_packv5_042523_0143.root, FC#13, port D2

Entries	381
Mean	44.21
Std Dev	11.55

Turn on : 26.9024

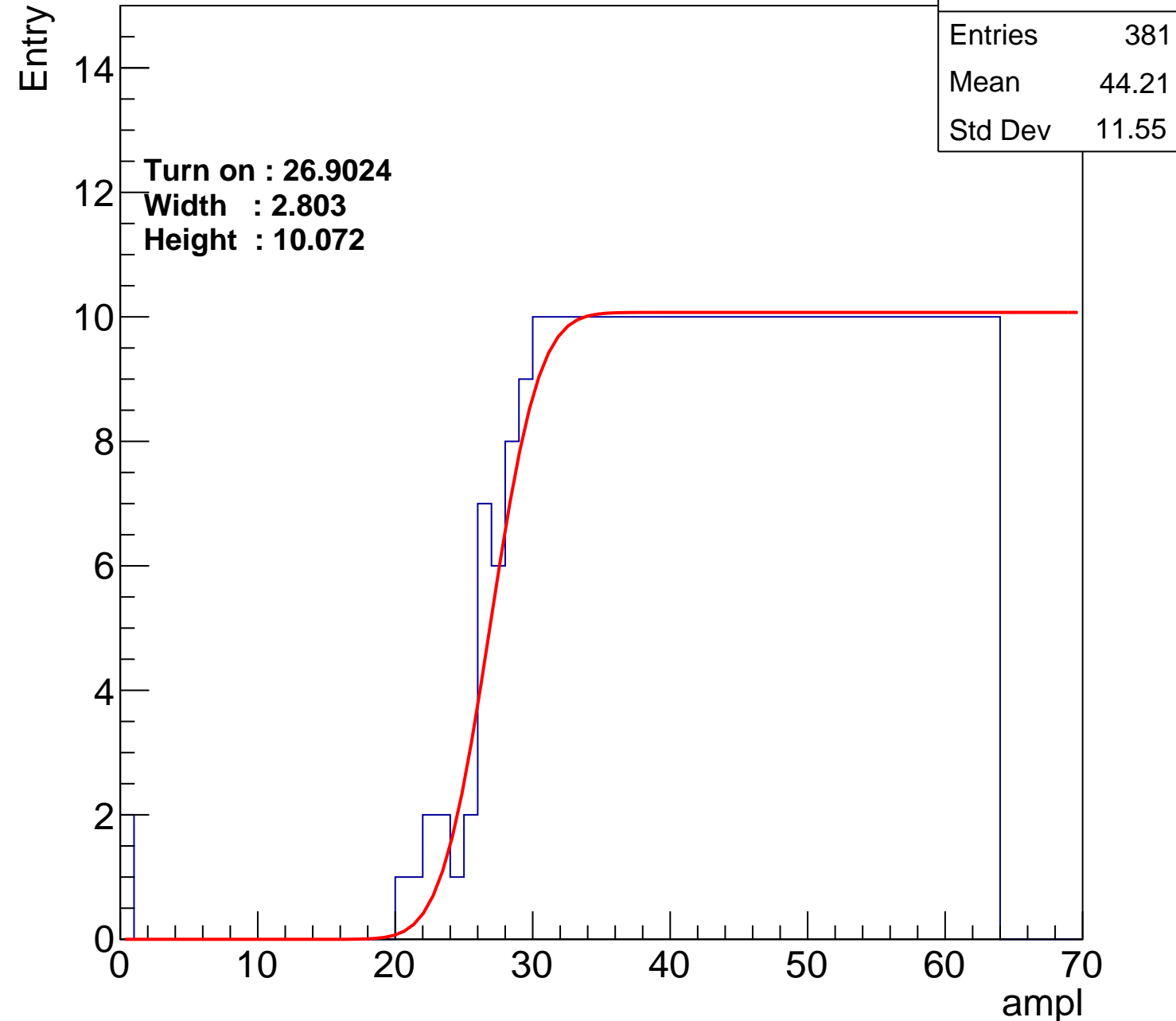
Width : 2.803

Height : 10.072

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch73

calib_packv5_042523_0143.root, FC#13, port D2

Entries	350
Mean	45.78
Std Dev	10.69

Turn on : 29.2710

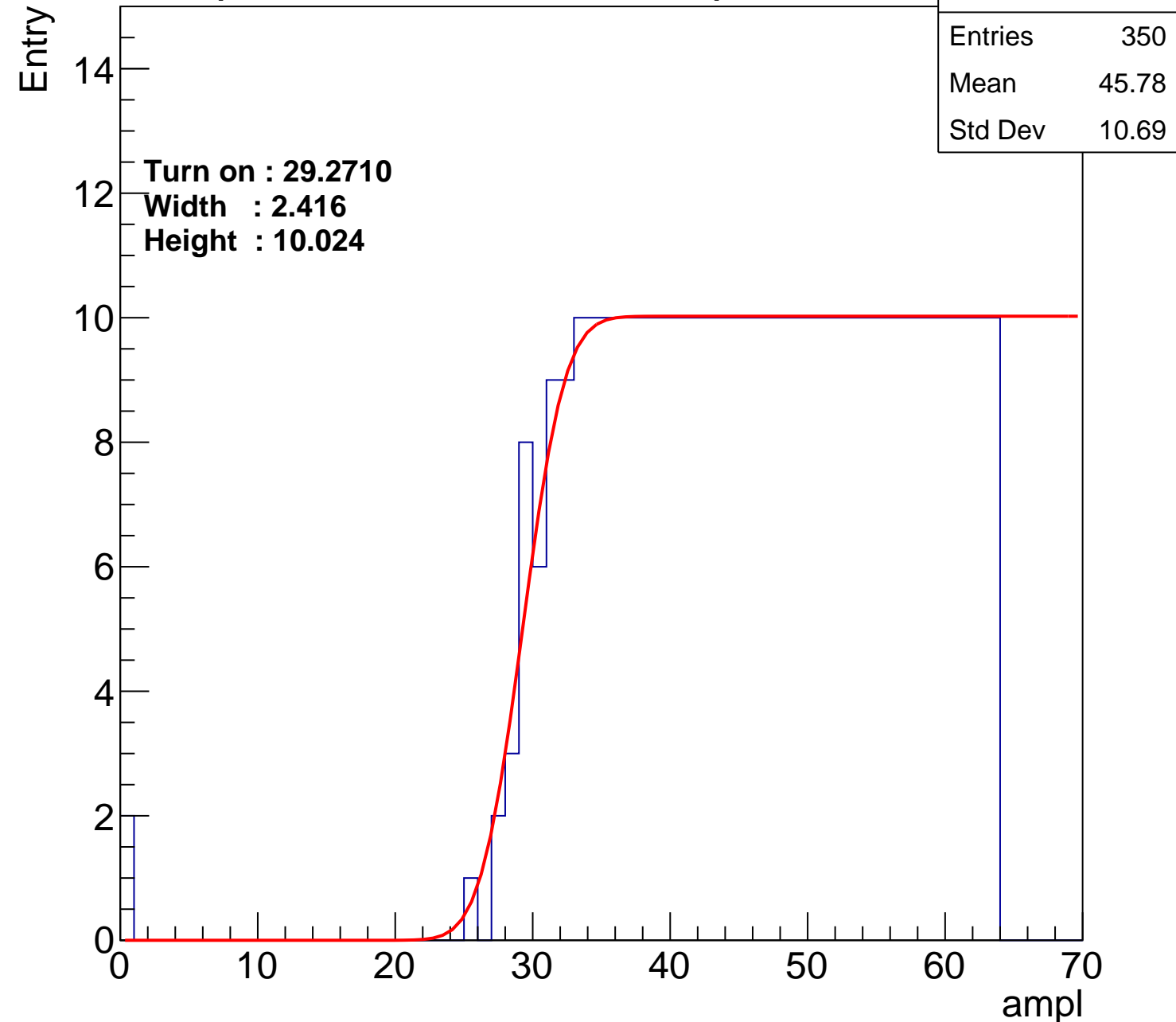
Width : 2.416

Height : 10.024

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch74

calib_packv5_042523_0143.root, FC#13, port D2

Entries	379
Mean	44.28
Std Dev	11.62

Turn on : 26.7381

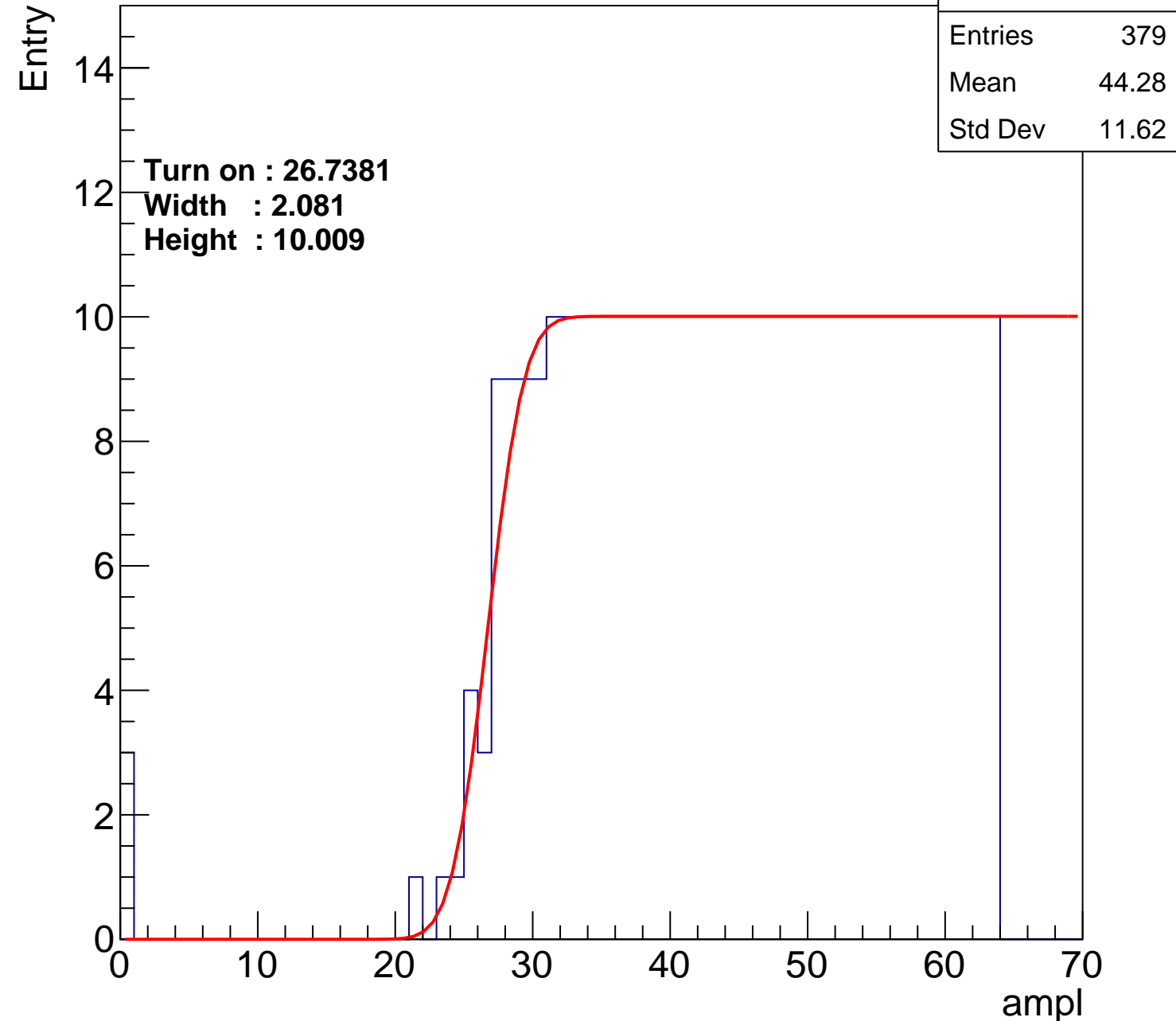
Width : 2.081

Height : 10.009

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch75

calib_packv5_042523_0143.root, FC#13, port D2

Entries	375
Mean	44.5
Std Dev	11.4

Turn on : 26.8224

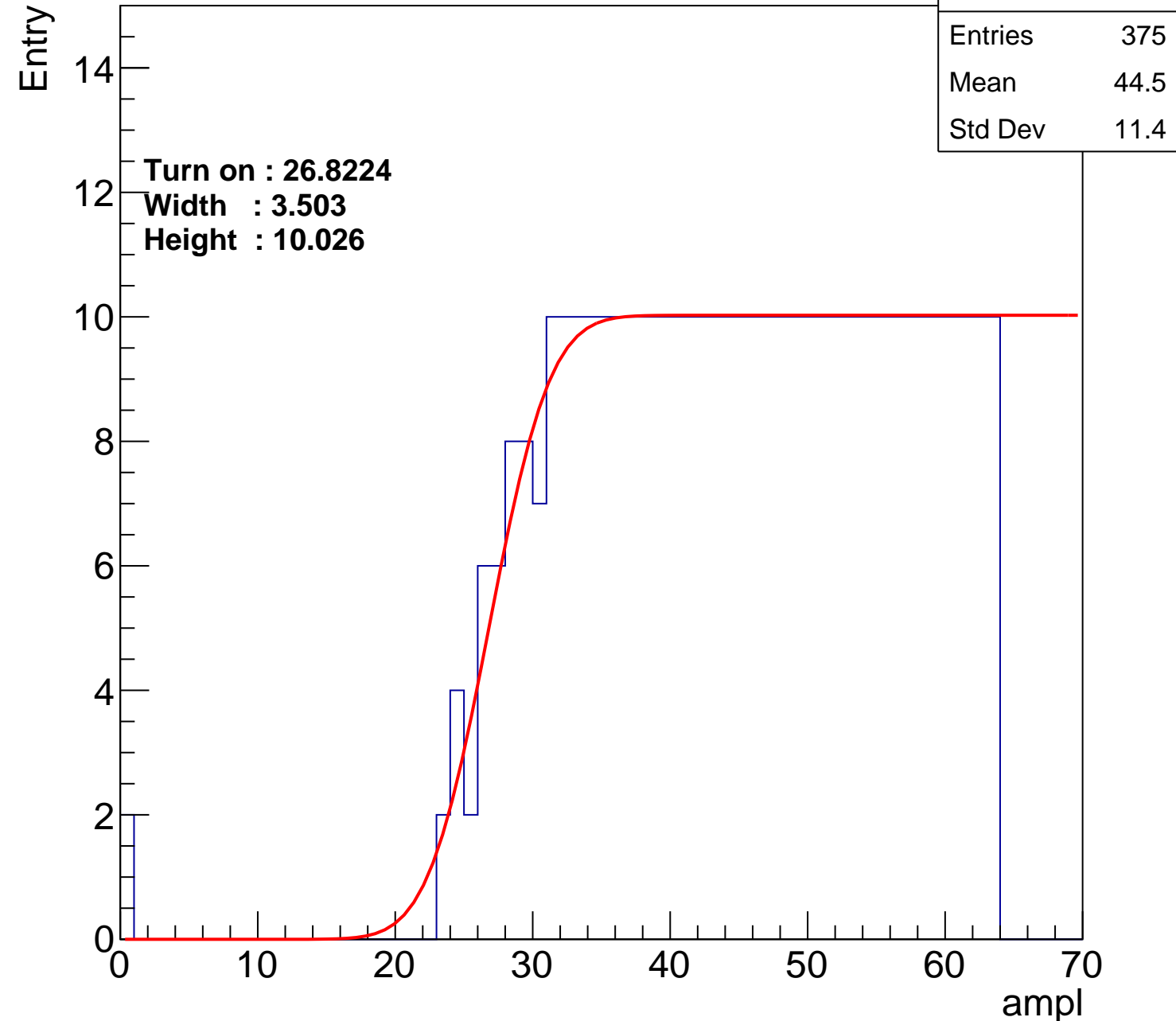
Width : 3.503

Height : 10.026

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch76

calib_packv5_042523_0143.root, FC#13, port D2

Entries	362
Mean	44.97
Std Dev	11.51

Turn on : 28.5049

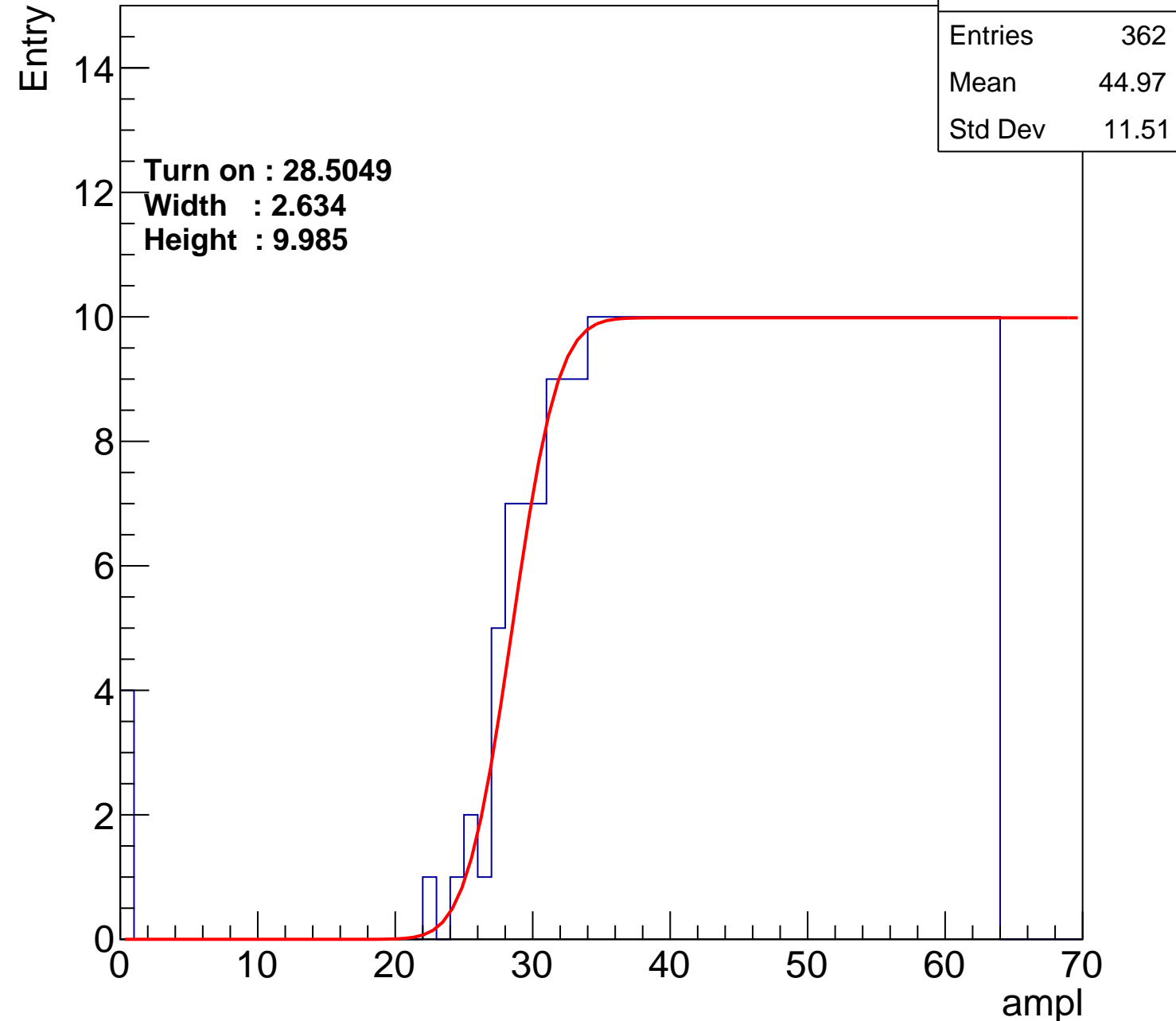
Width : 2.634

Height : 9.985

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch77

calib_packv5_042523_0143.root, FC#13, port D2

Entries	375
Mean	44.51
Std Dev	11.32

Turn on : 27.2716

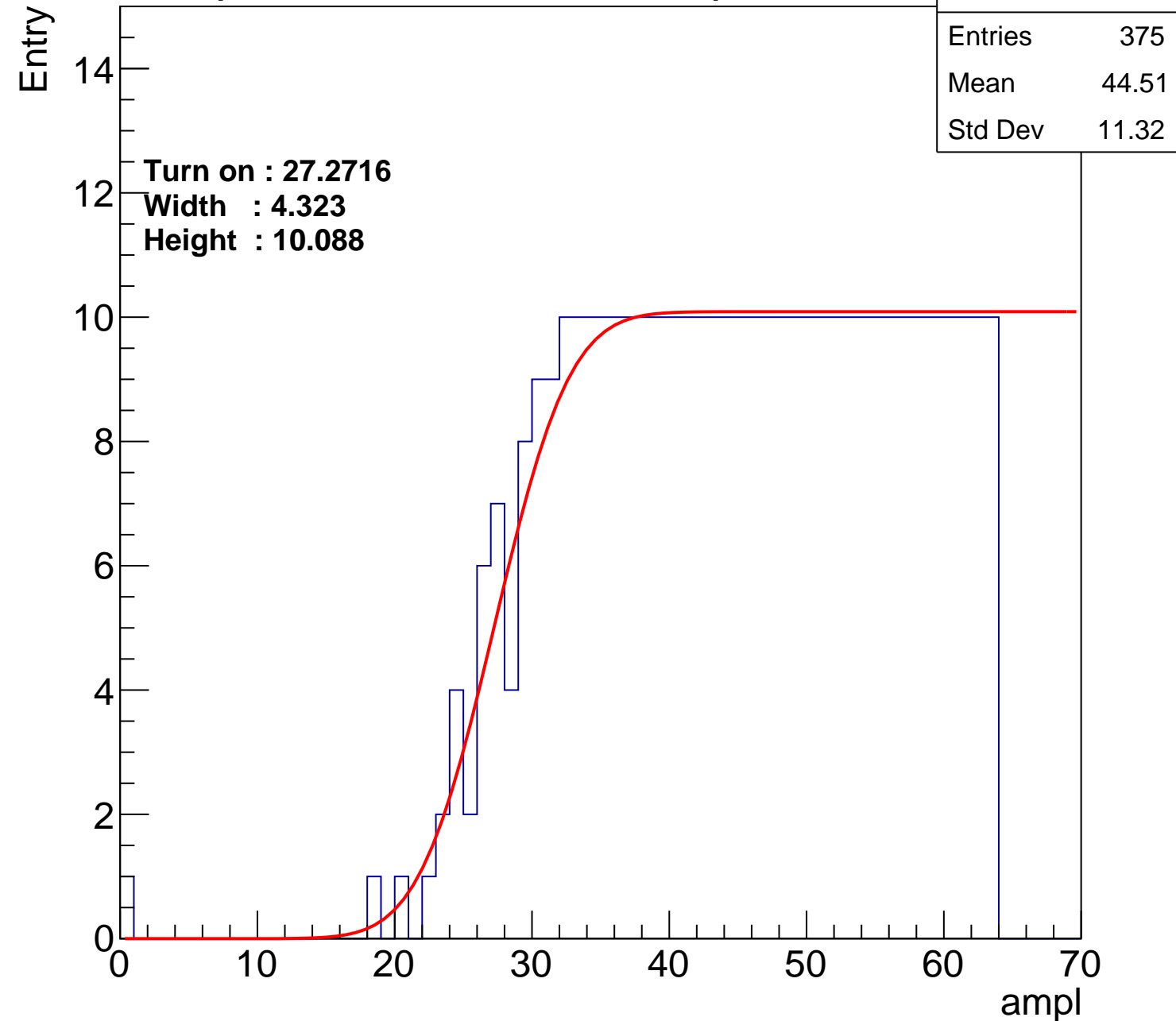
Width : 4.323

Height : 10.088

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch78

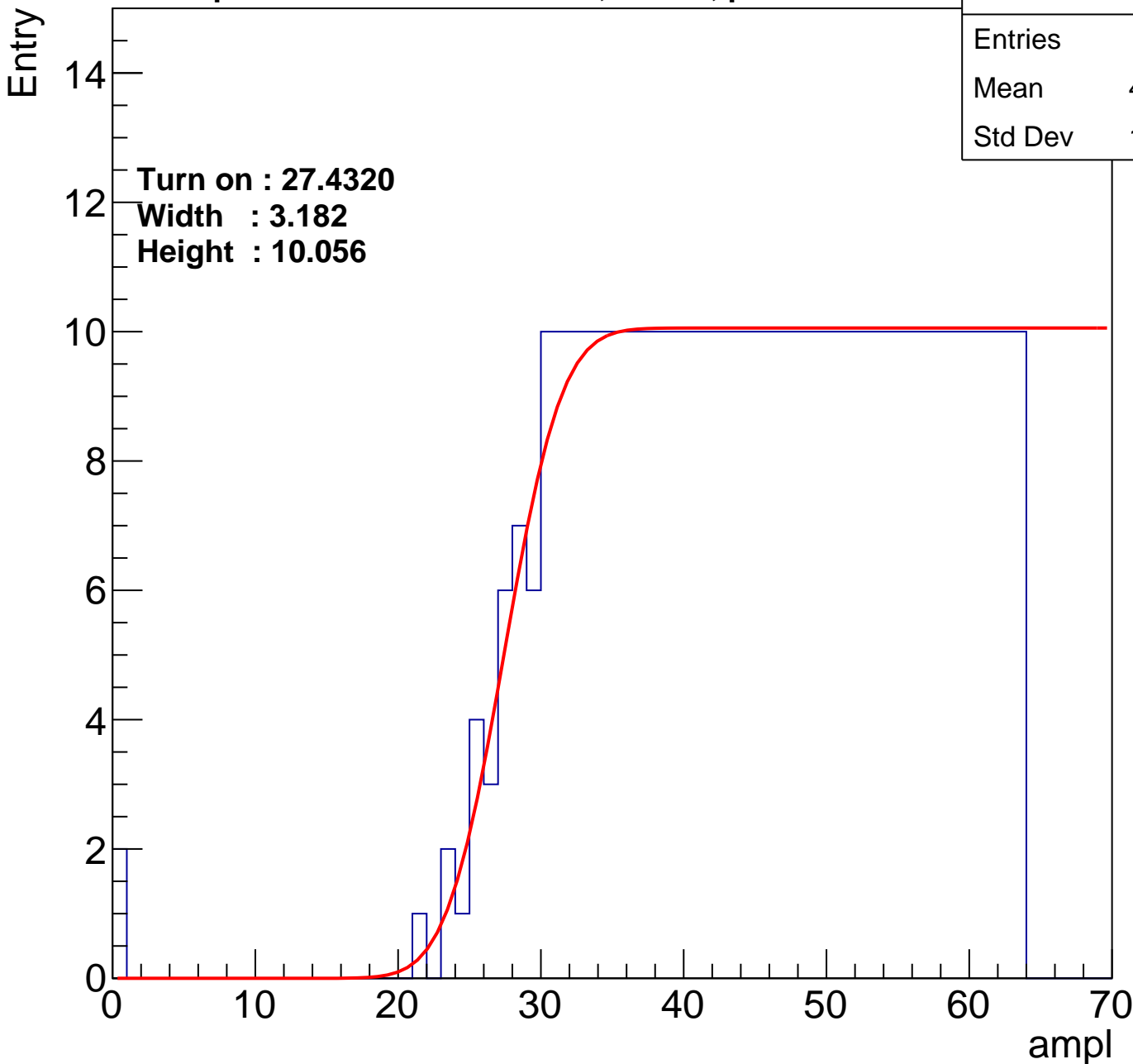
calib_packv5_042523_0143.root, FC#13, port D2

Entries	372
Mean	44.65
Std Dev	11.32

Turn on : 27.4320

Width : 3.182

Height : 10.056



B1L003S, U2-ch79

calib_packv5_042523_0143.root, FC#13, port D2

Entries	377
Mean	44.43
Std Dev	11.41

Turn on : 27.2065

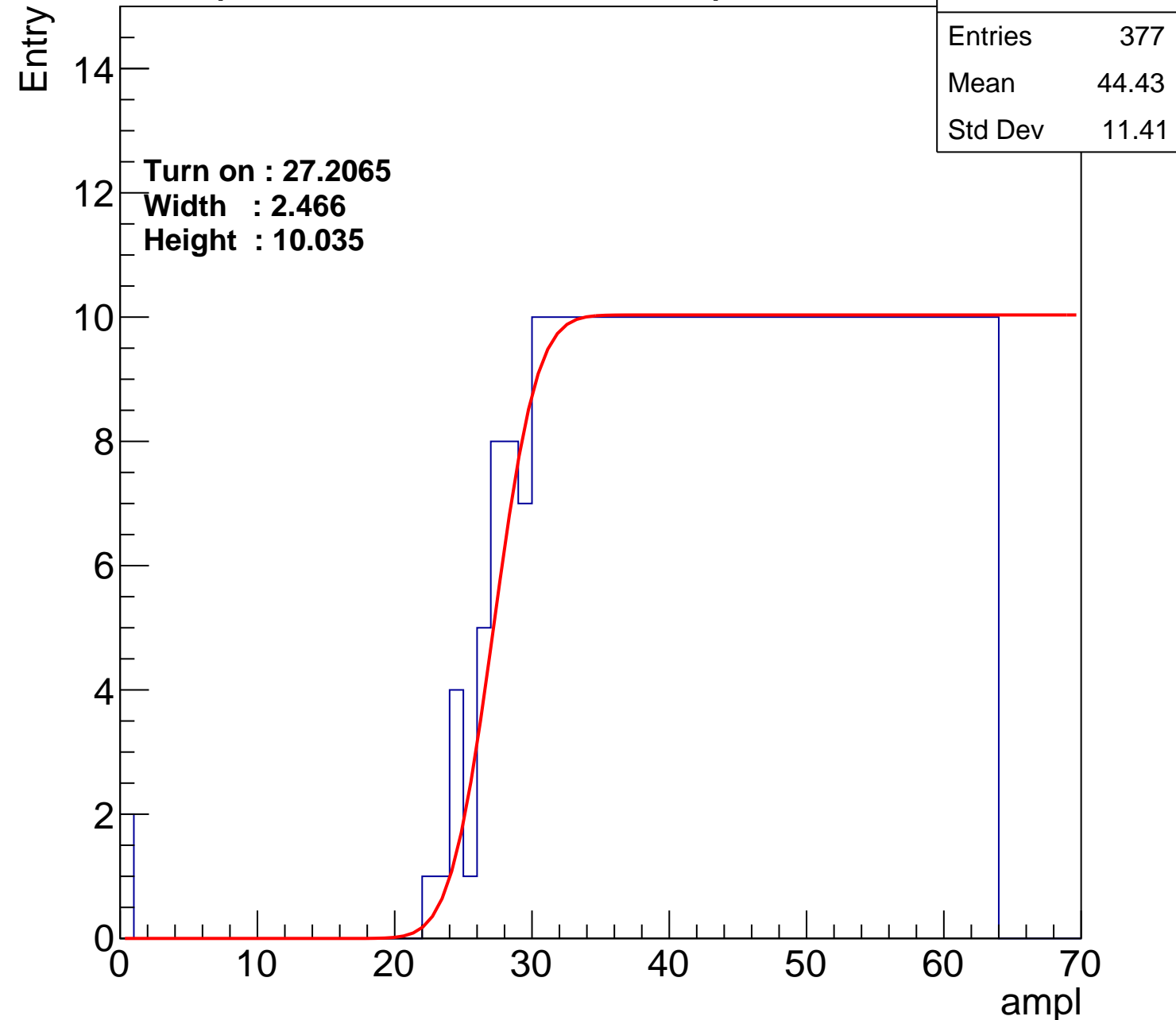
Width : 2.466

Height : 10.035

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch80

calib_packv5_042523_0143.root, FC#13, port D2

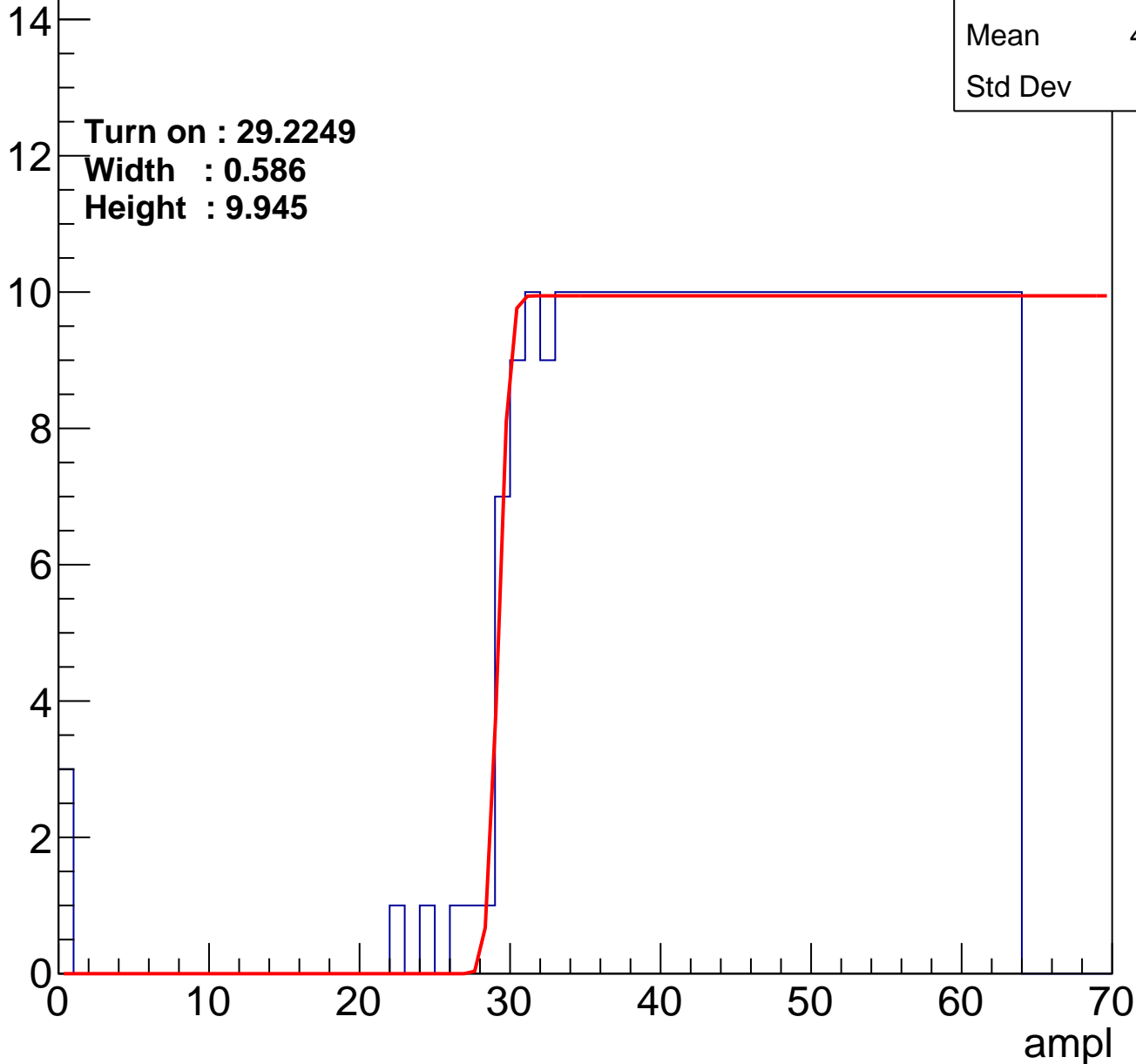
Entry

Entries	353
Mean	45.55
Std Dev	11.01

Turn on : 29.2249

Width : 0.586

Height : 9.945



B1L003S, U2-ch81

calib_packv5_042523_0143.root, FC#13, port D2

Entries	370
Mean	44.77
Std Dev	11.24

Turn on : 27.4359

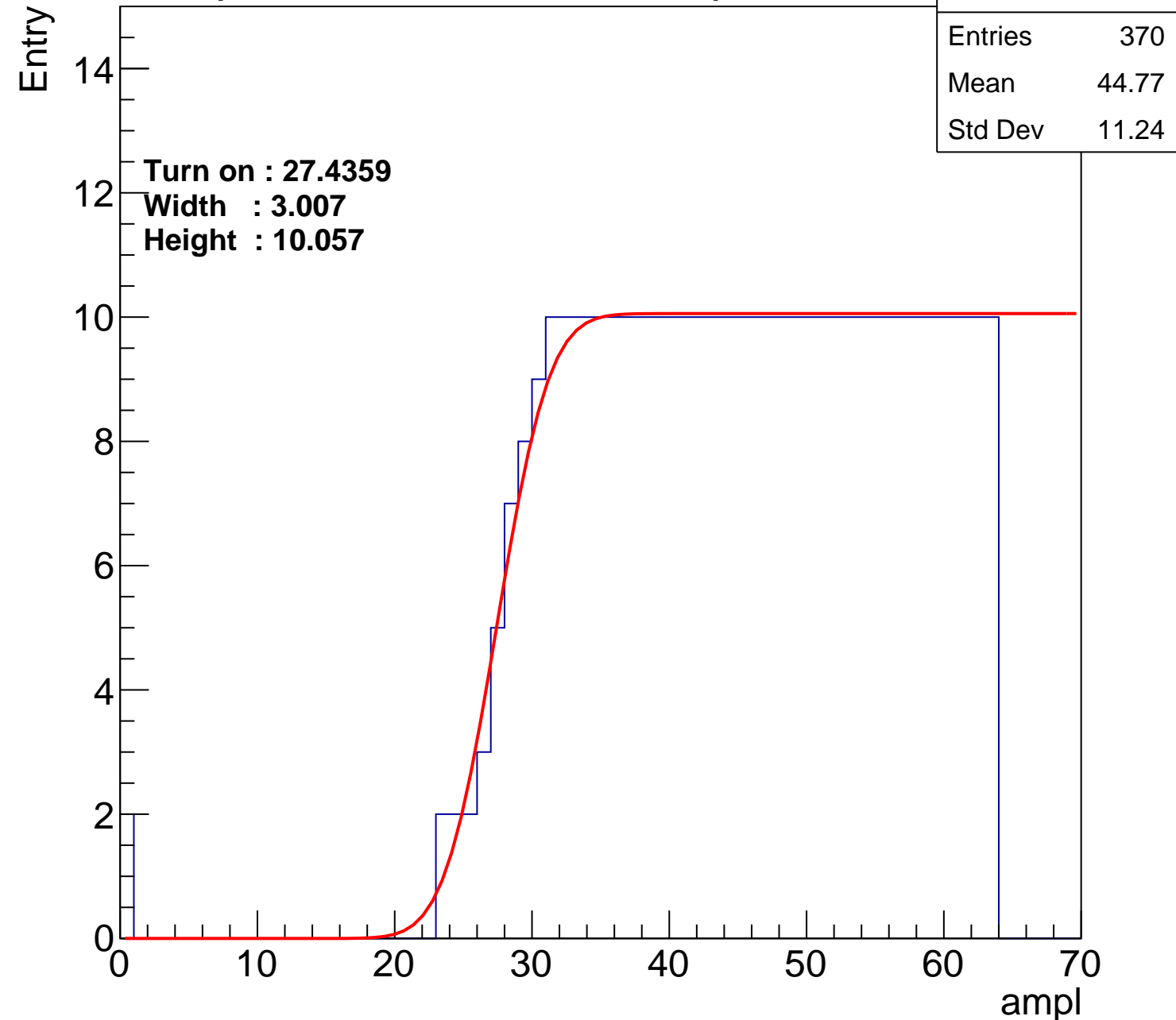
Width : 3.007

Height : 10.057

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch82

calib_packv5_042523_0143.root, FC#13, port D2

Entries	360
Mean	45.25
Std Dev	11

Turn on : 28.3786

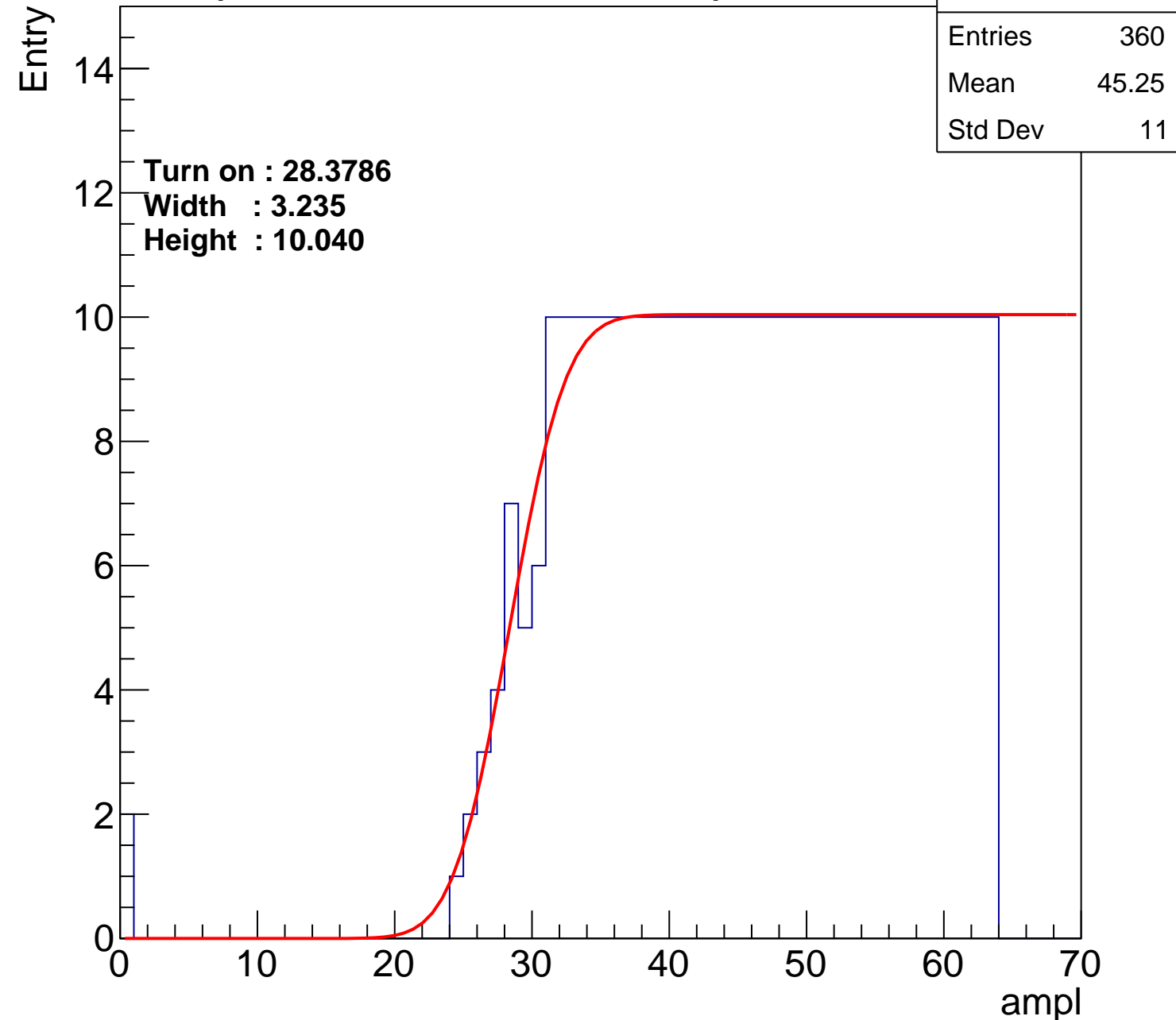
Width : 3.235

Height : 10.040

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch83

calib_packv5_042523_0143.root, FC#13, port D2

Entries	361
Mean	45.08
Std Dev	11.41

Turn on : 28.4598

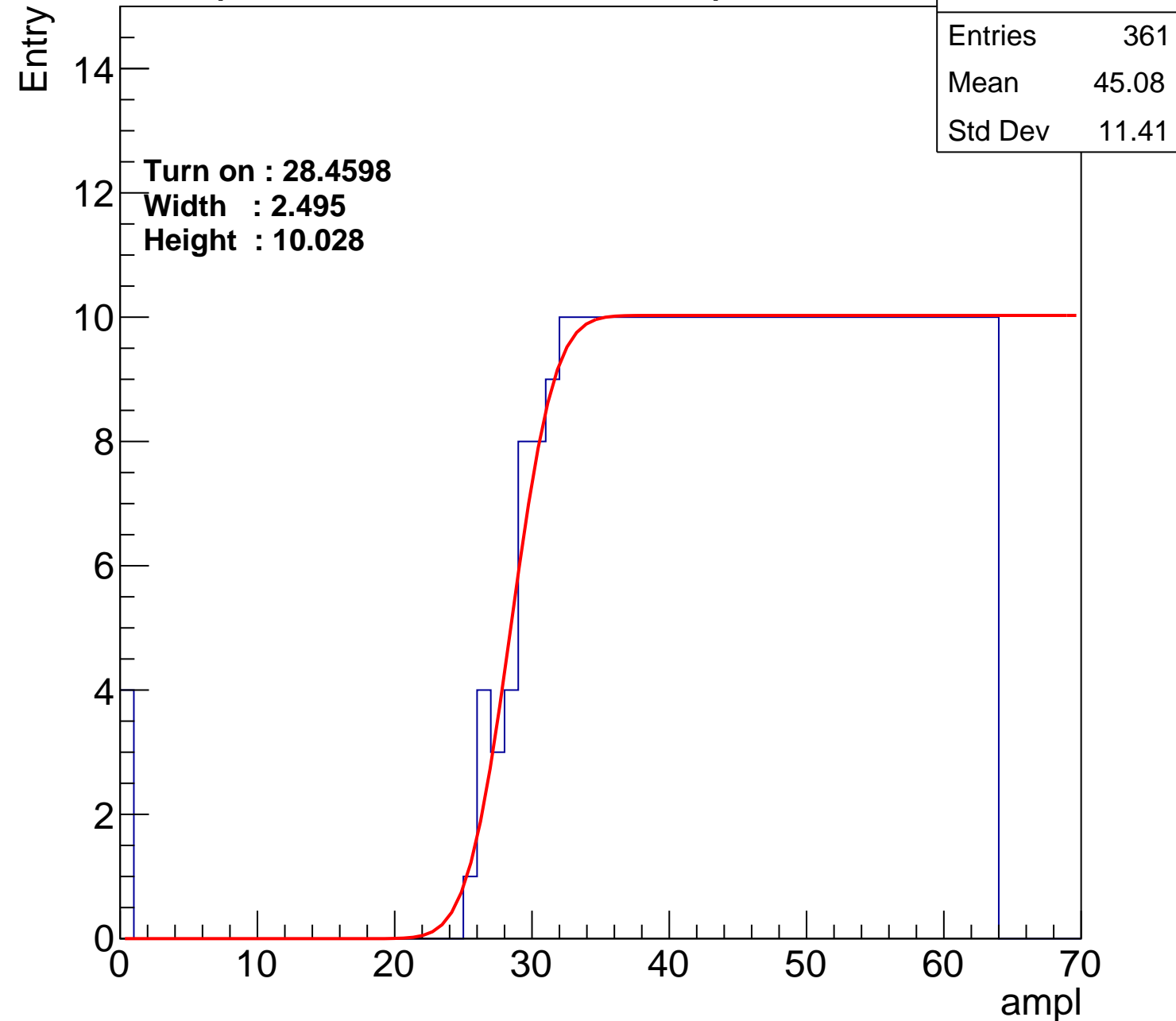
Width : 2.495

Height : 10.028

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch84

calib_packv5_042523_0143.root, FC#13, port D2

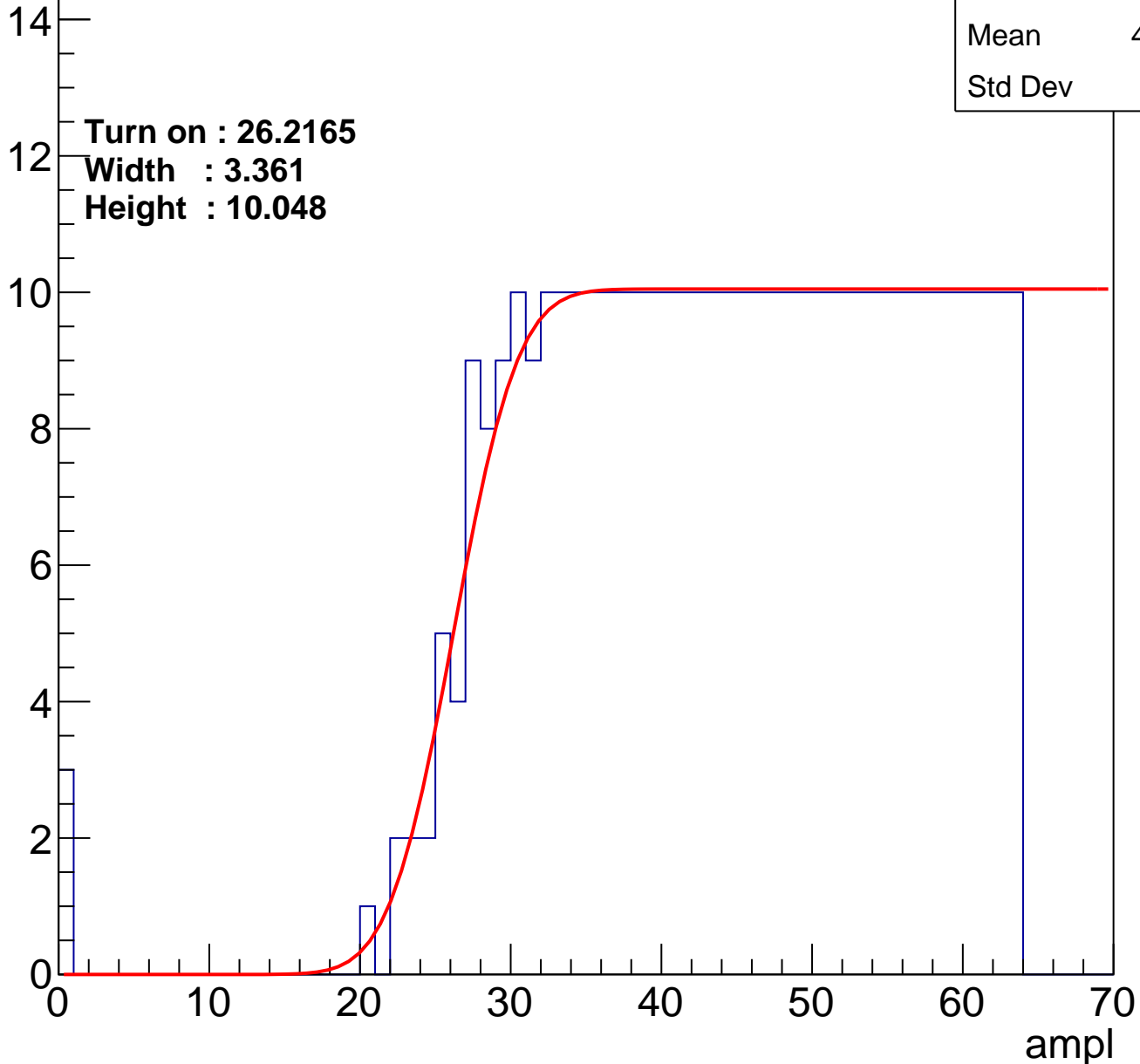
Entries	384
Mean	43.99
Std Dev	11.8

Turn on : 26.2165

Width : 3.361

Height : 10.048

Entry



B1L003S, U2-ch85

calib_packv5_042523_0143.root, FC#13, port D2

Entries	376
Mean	44.49
Std Dev	11.37

Turn on : 27.0718

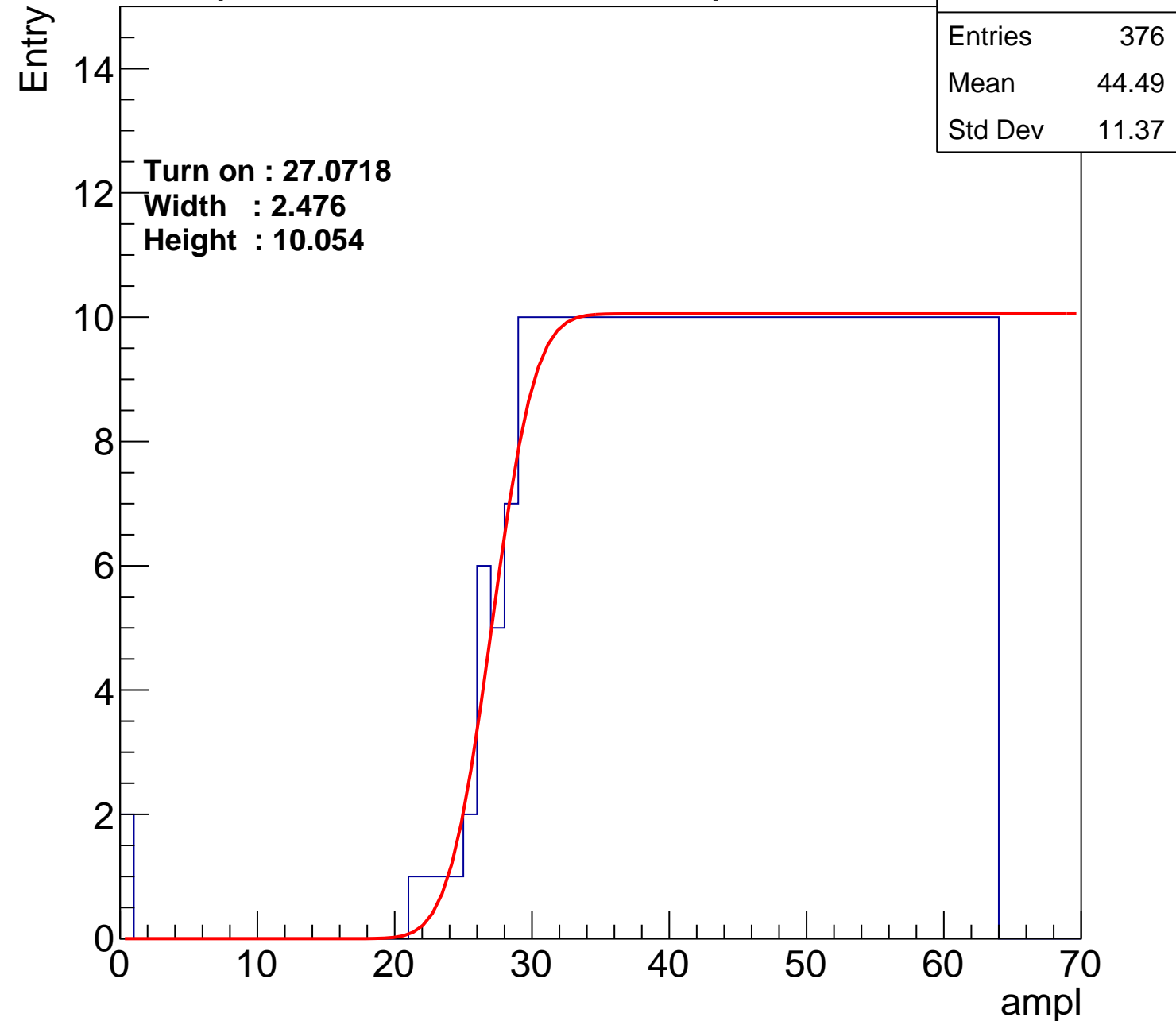
Width : 2.476

Height : 10.054

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch86

calib_packv5_042523_0143.root, FC#13, port D2

Entries	377
Mean	44.32
Std Dev	11.65

Turn on : 26.8570

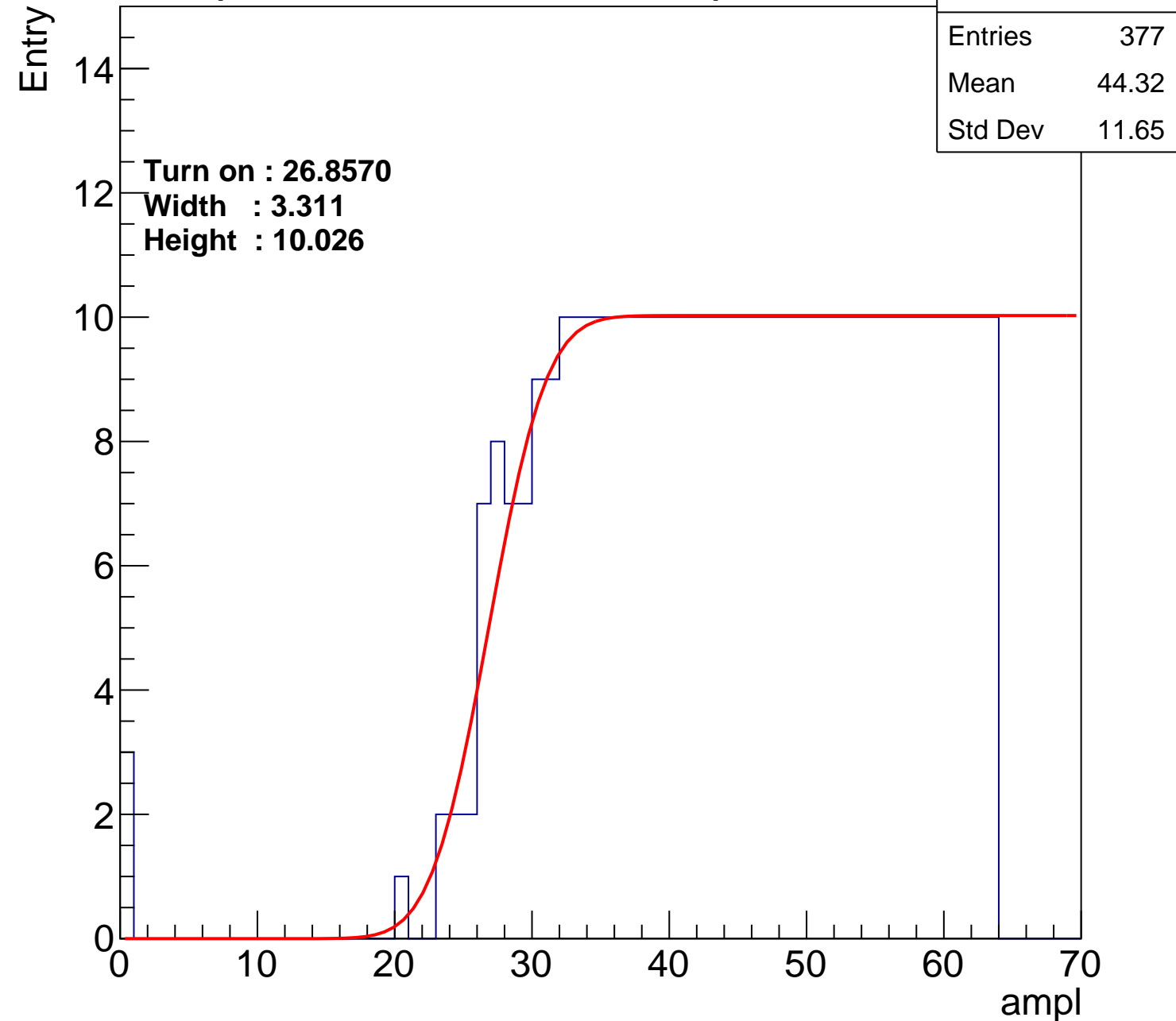
Width : 3.311

Height : 10.026

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch87

calib_packv5_042523_0143.root, FC#13, port D2

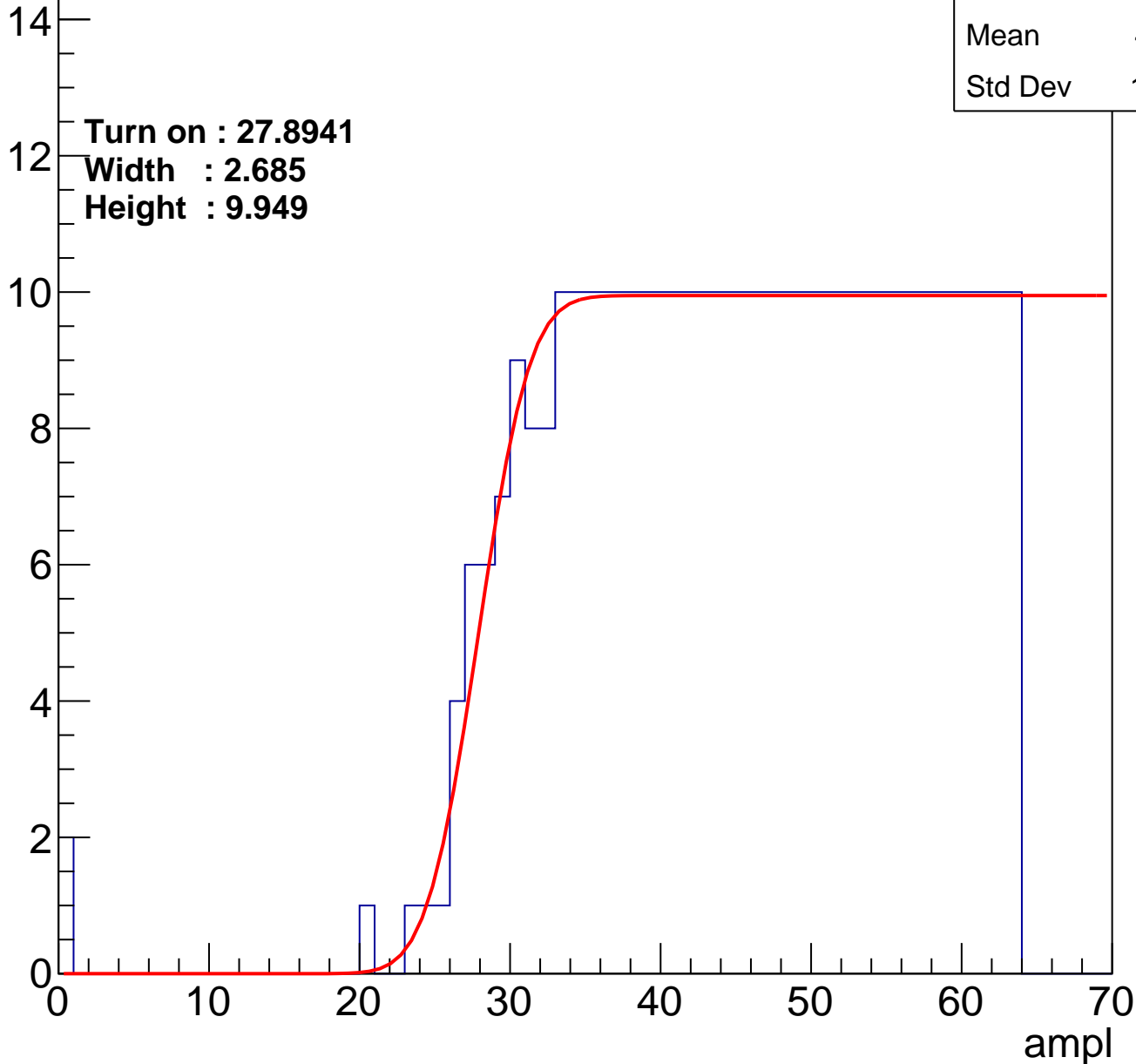
Entry

Entries	364
Mean	45.01
Std Dev	11.17

Turn on : 27.8941

Width : 2.685

Height : 9.949



B1L003S, U2-ch88

calib_packv5_042523_0143.root, FC#13, port D2

Entries	367
Mean	44.77
Std Dev	11.56

Turn on : 28.1604

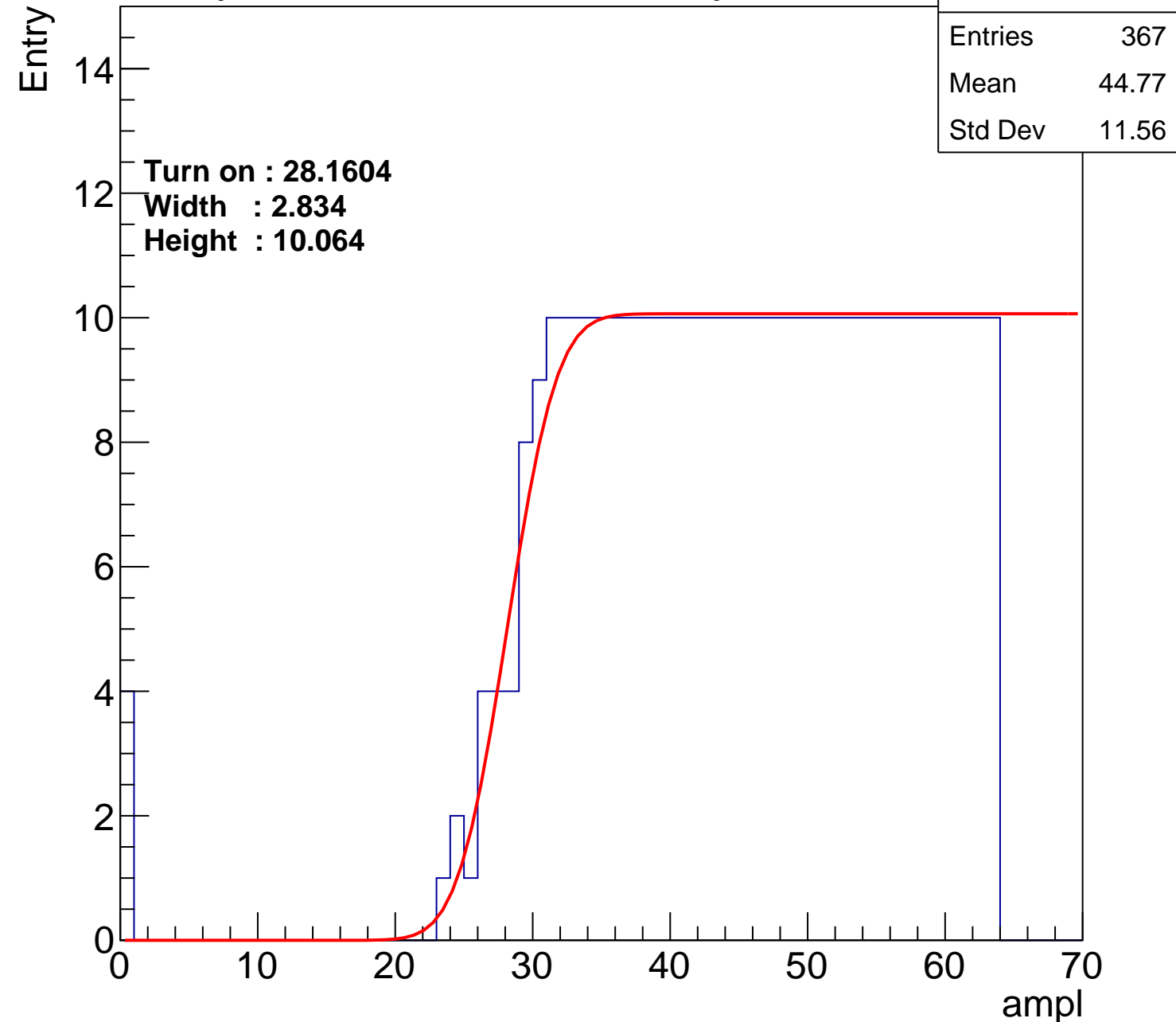
Width : 2.834

Height : 10.064

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch89

calib_packv5_042523_0143.root, FC#13, port D2

Entries	359
Mean	45.3
Std Dev	10.98

Turn on : 28.4739

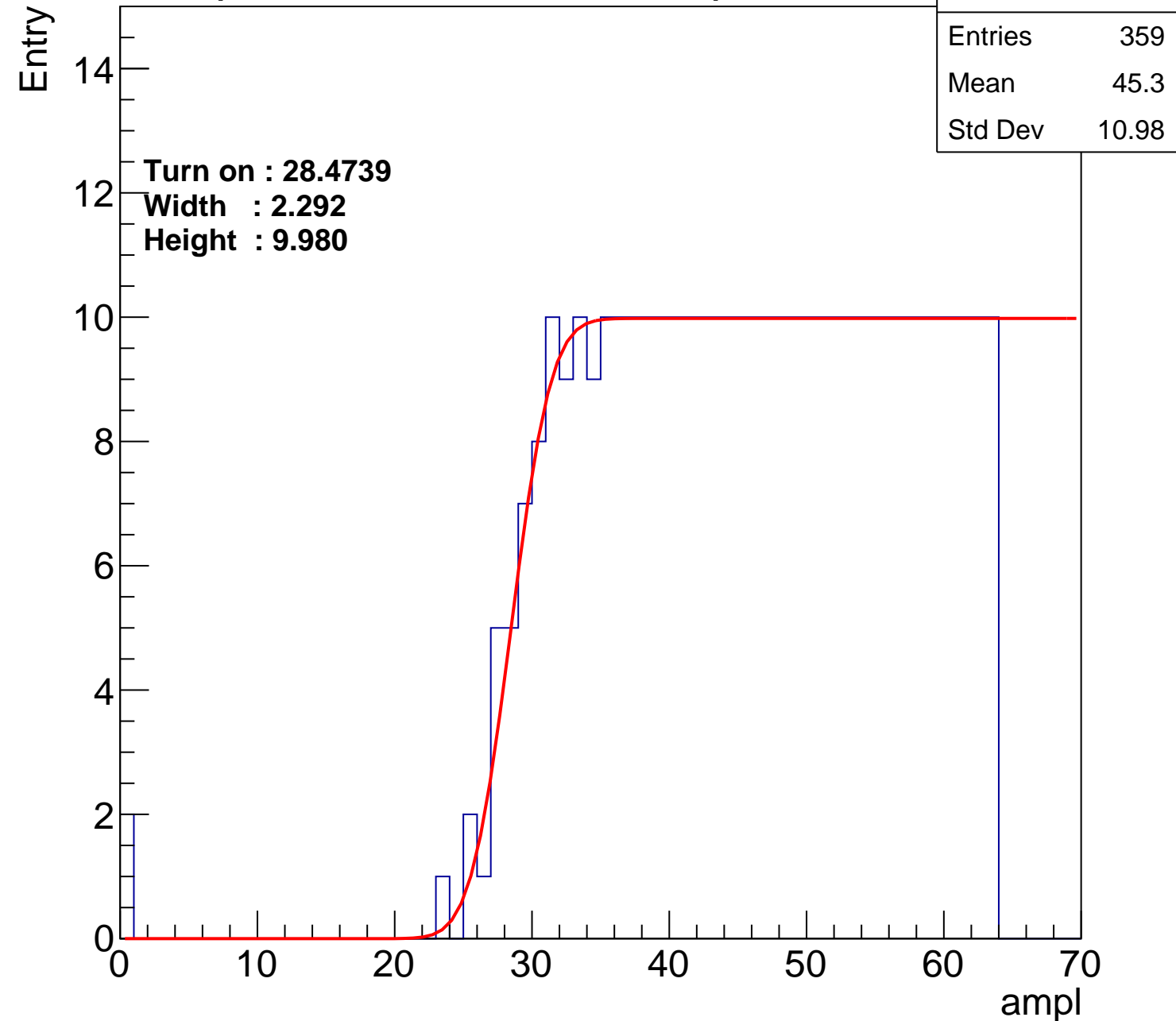
Width : 2.292

Height : 9.980

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch90

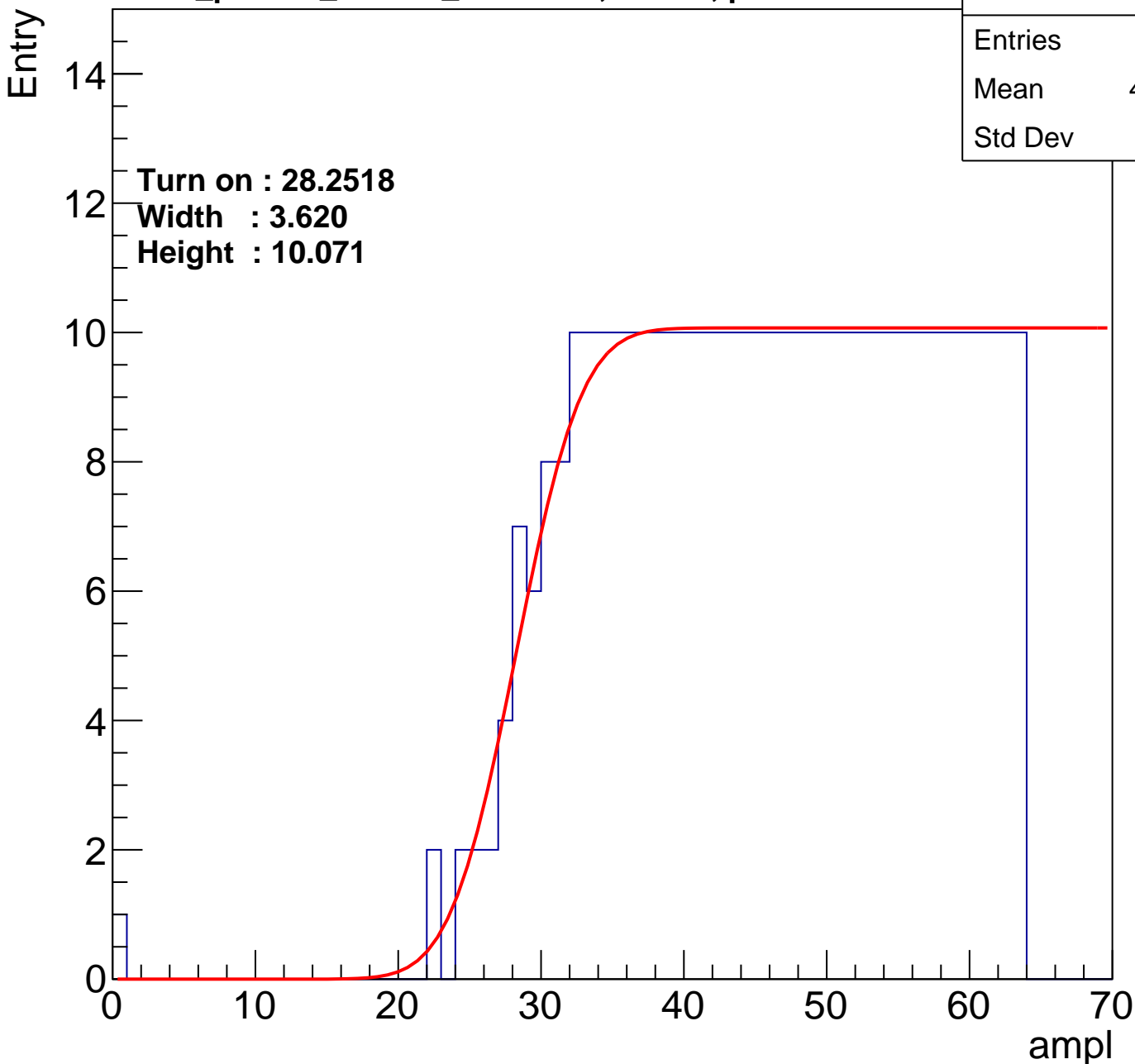
calib_packv5_042523_0143.root, FC#13, port D2

Entries	362
Mean	45.19
Std Dev	10.9

Turn on : 28.2518

Width : 3.620

Height : 10.071



B1L003S, U2-ch91

calib_packv5_042523_0143.root, FC#13, port D2

Entries	371
Mean	44.62
Std Dev	11.51

Turn on : 27.5463

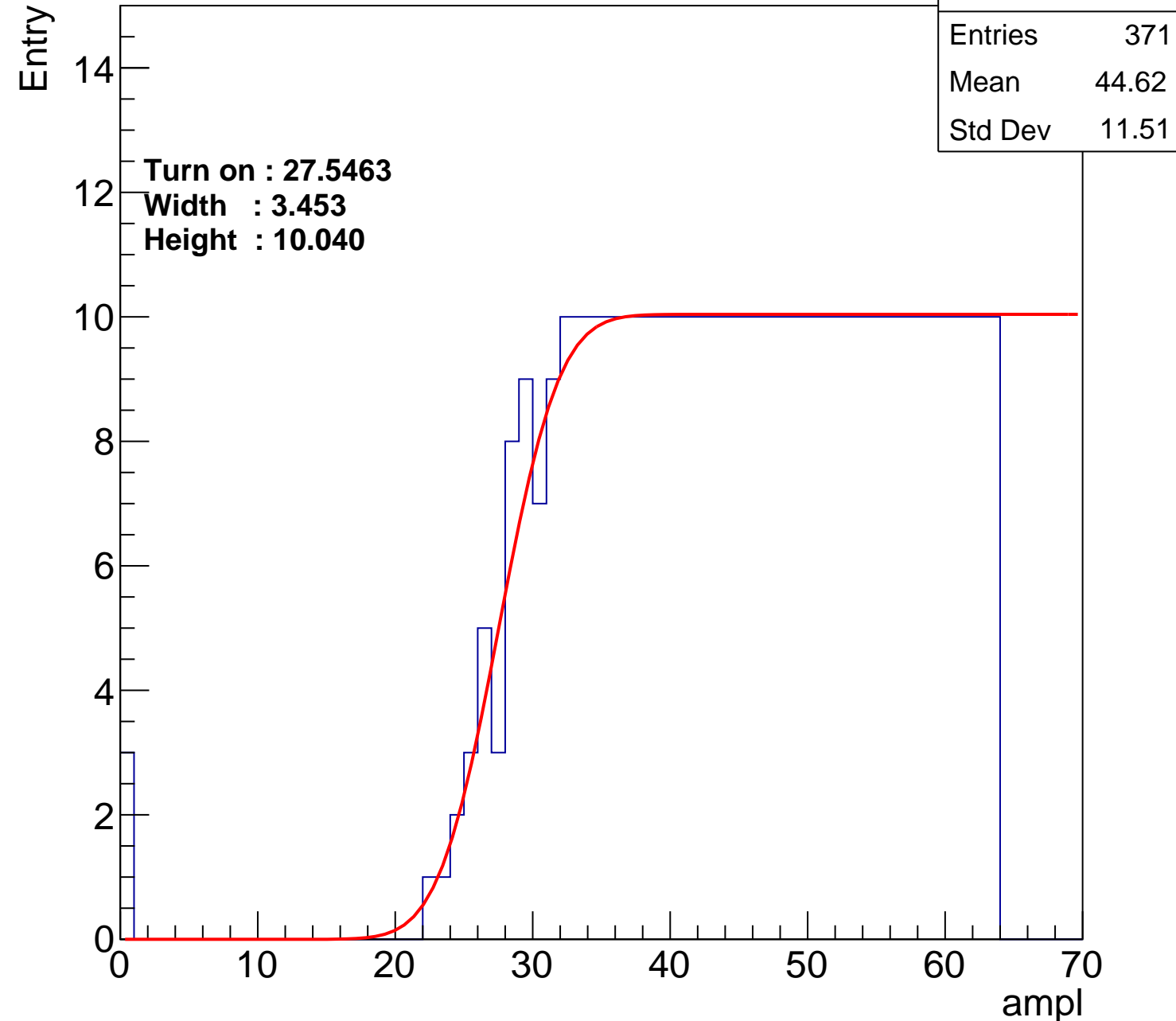
Width : 3.453

Height : 10.040

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch92

calib_packv5_042523_0143.root, FC#13, port D2

Entries	365
Mean	44.9
Std Dev	11.39

Turn on : 28.4212

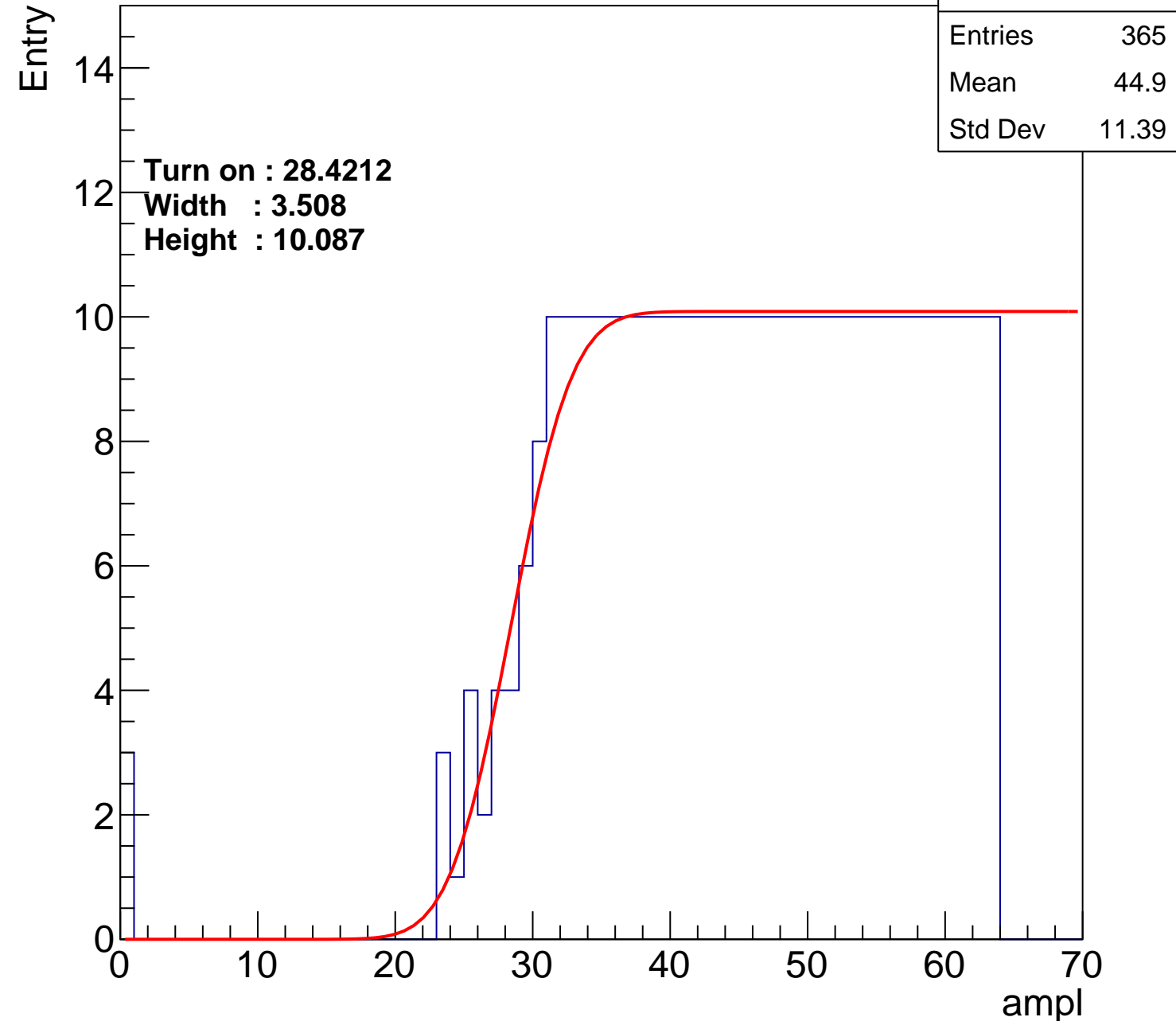
Width : 3.508

Height : 10.087

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch93

calib_packv5_042523_0143.root, FC#13, port D2

Entries	367
Mean	44.61
Std Dev	11.98

Turn on : 27.8974

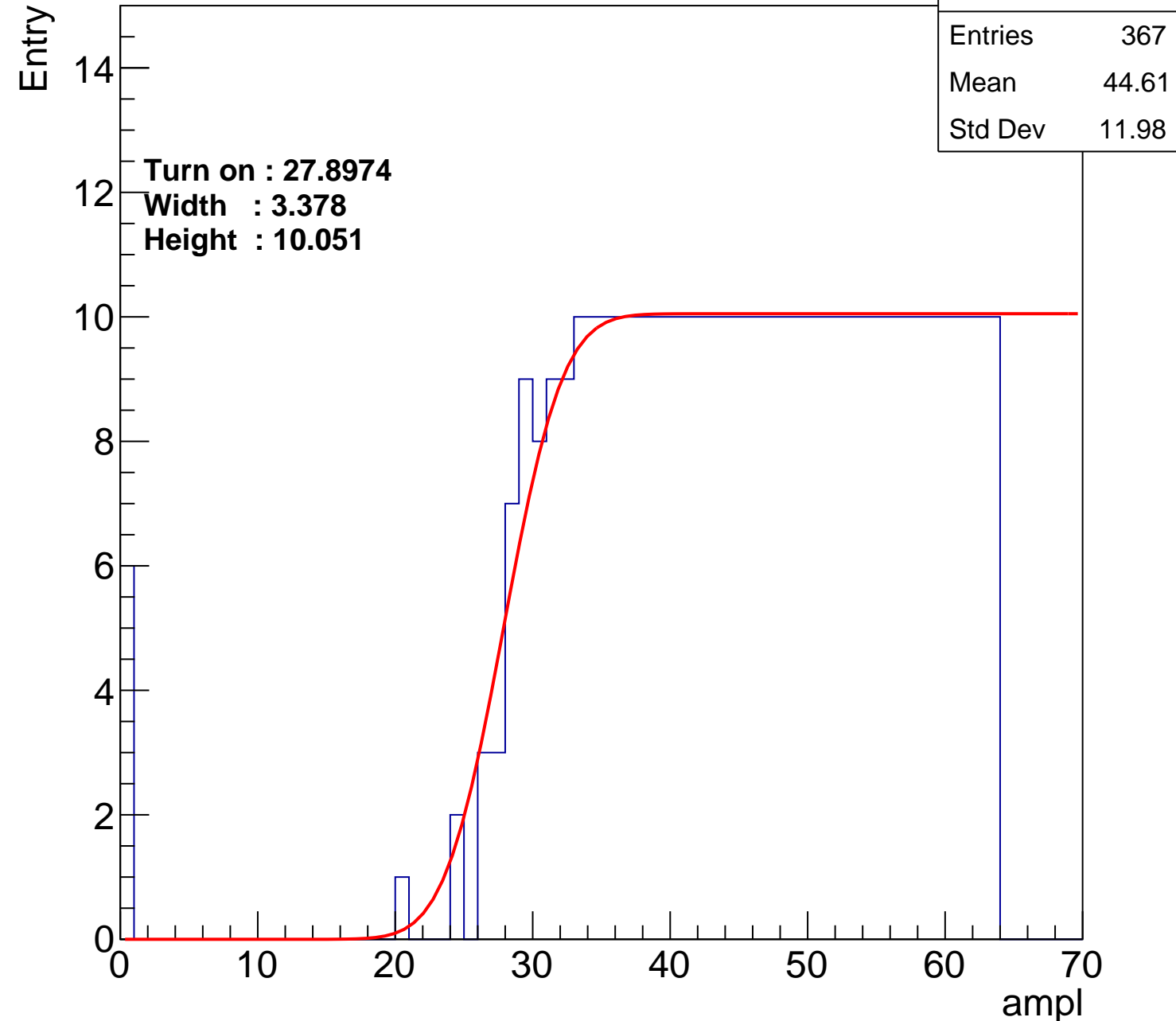
Width : 3.378

Height : 10.051

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch94

calib_packv5_042523_0143.root, FC#13, port D2

Entries	357
Mean	45.43
Std Dev	10.89

Turn on : 29.1440

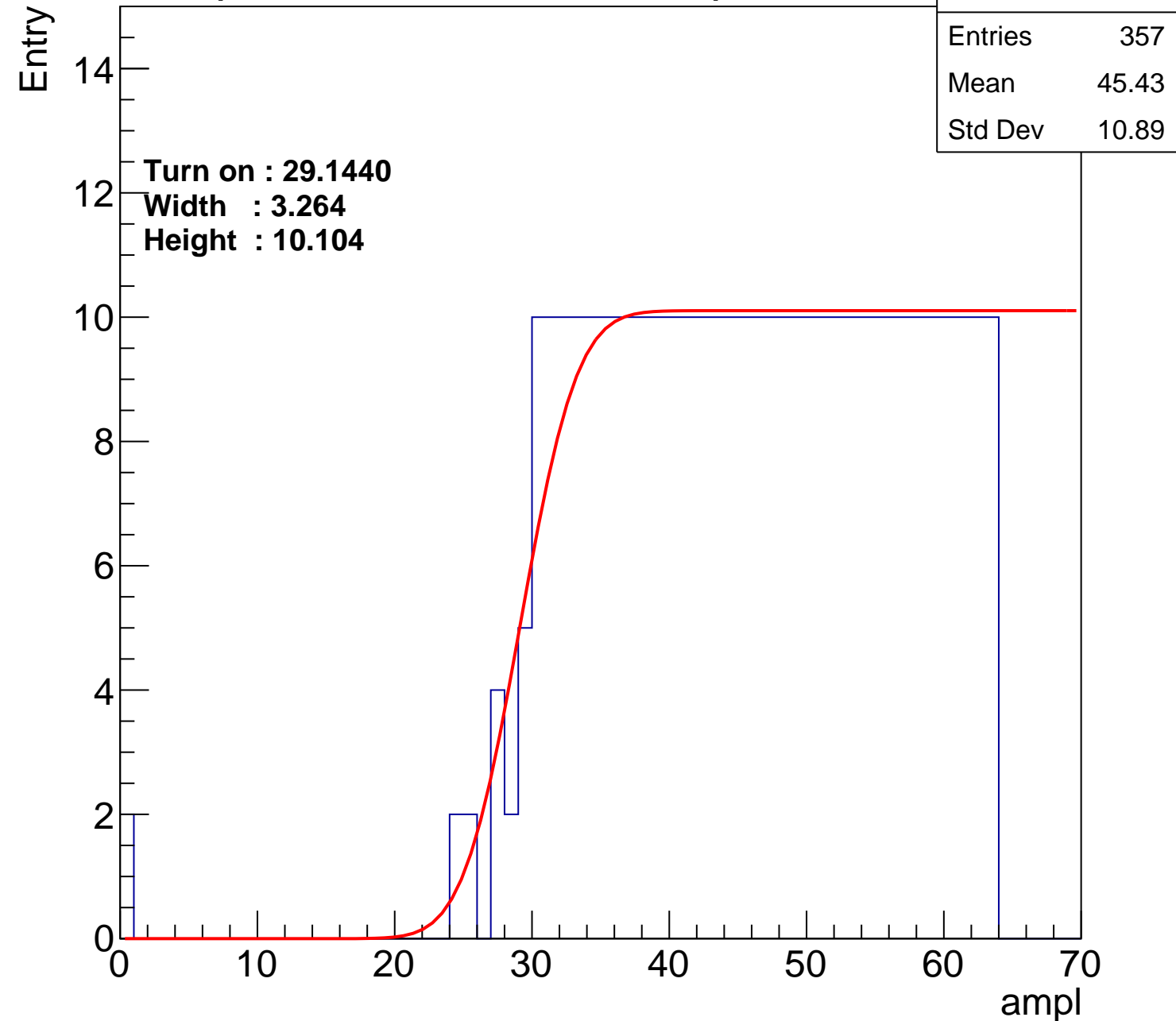
Width : 3.264

Height : 10.104

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch95

calib_packv5_042523_0143.root, FC#13, port D2

Entries	375
Mean	44.51
Std Dev	11.39

Turn on : 26.3633

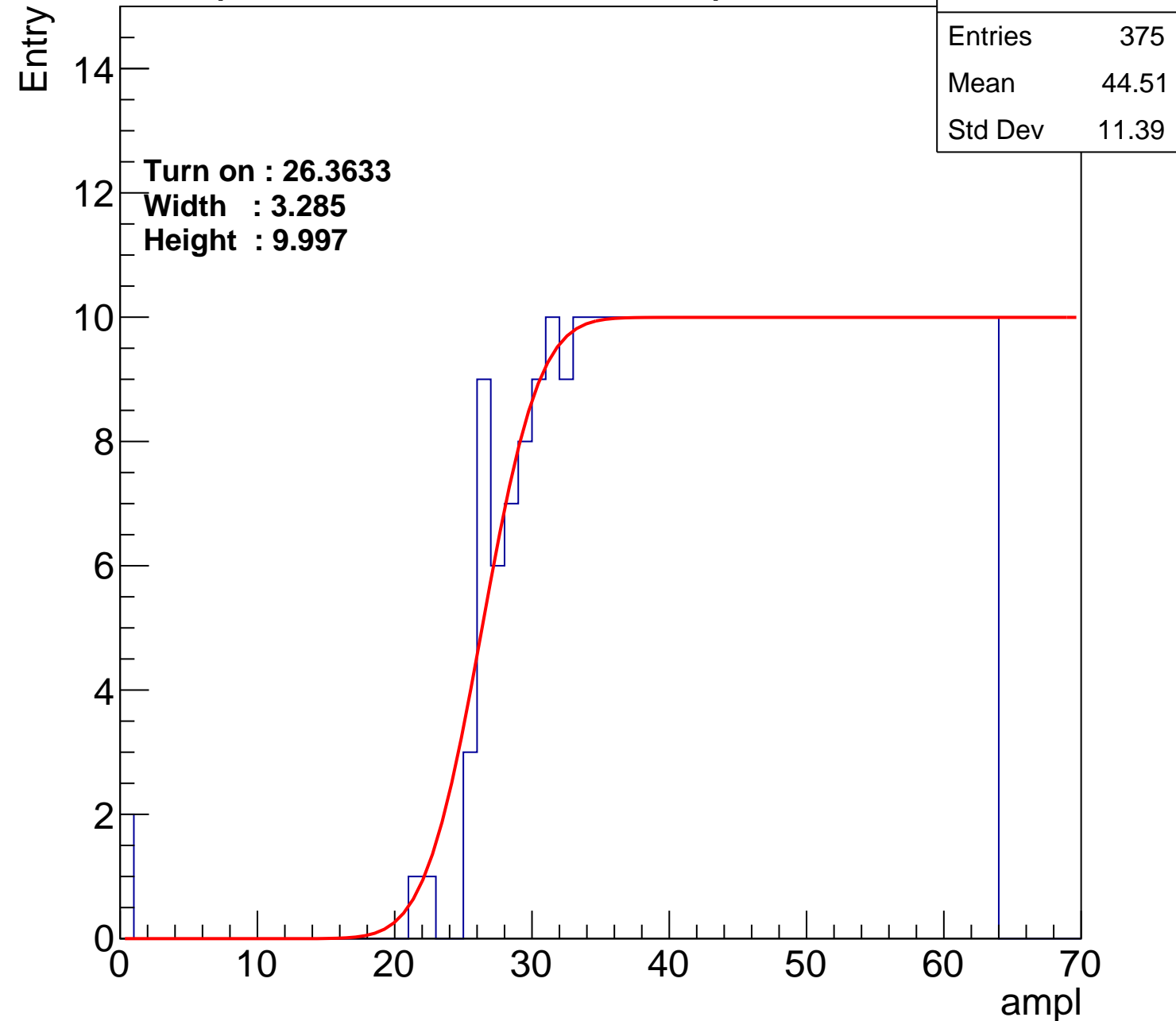
Width : 3.285

Height : 9.997

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch96

calib_packv5_042523_0143.root, FC#13, port D2

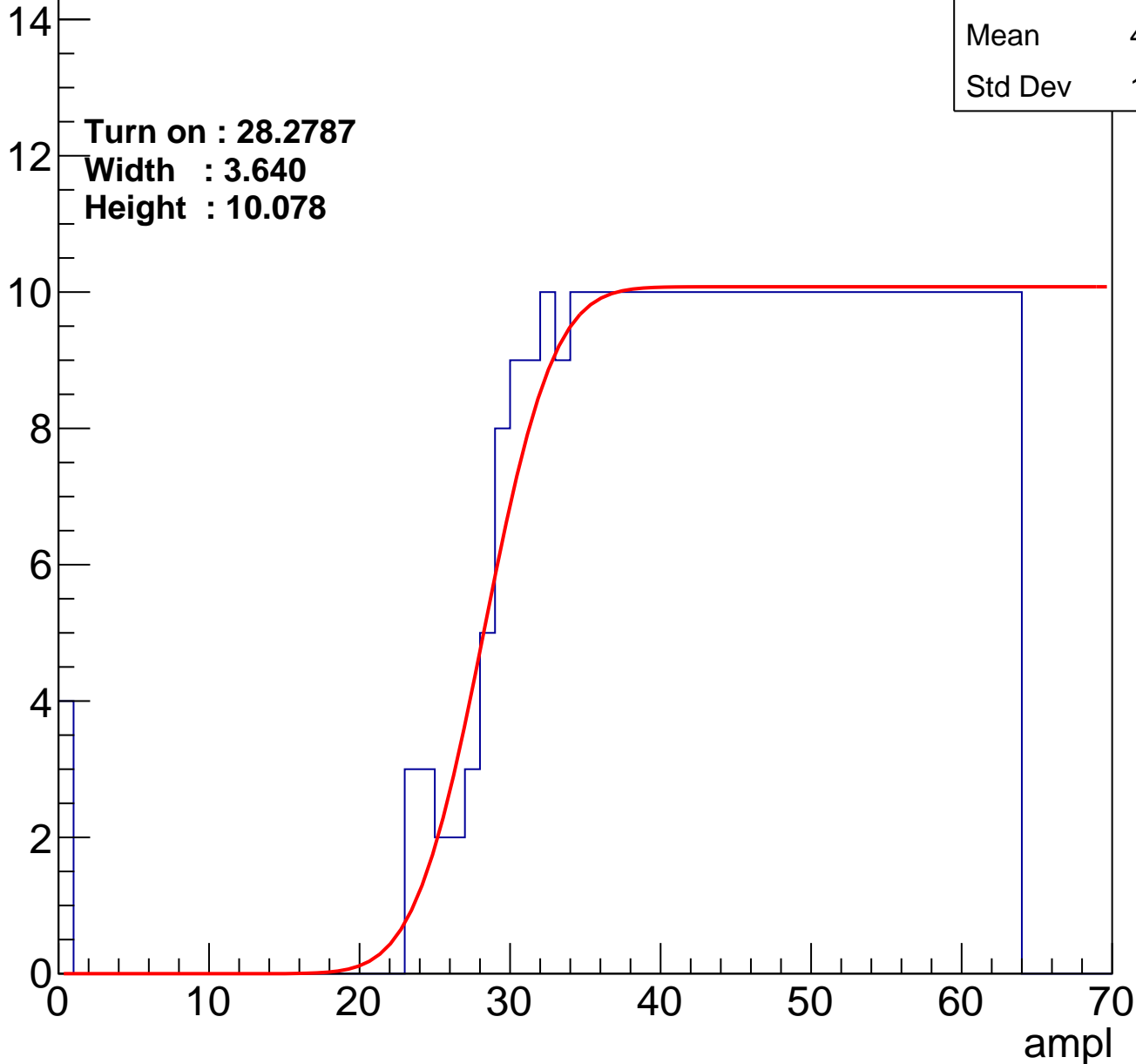
Entry

Entries	367
Mean	44.72
Std Dev	11.64

Turn on : 28.2787

Width : 3.640

Height : 10.078



B1L003S, U2-ch97

calib_packv5_042523_0143.root, FC#13, port D2

Entries	389
Mean	43.74
Std Dev	12

Turn on : 25.3323

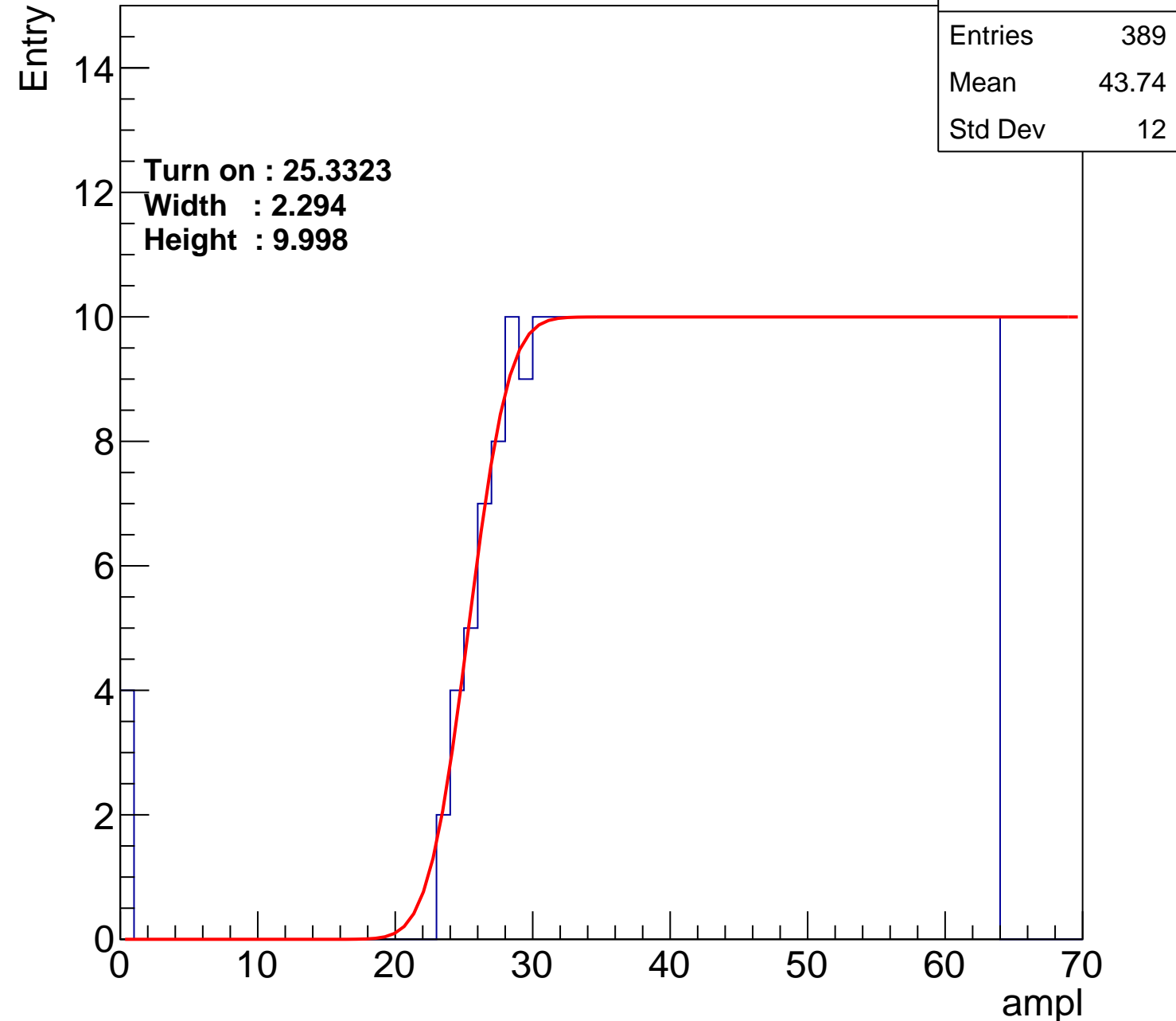
Width : 2.294

Height : 9.998

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch98

calib_packv5_042523_0143.root, FC#13, port D2

Entries	372
Mean	44.68
Std Dev	11.27

Turn on : 27.2848

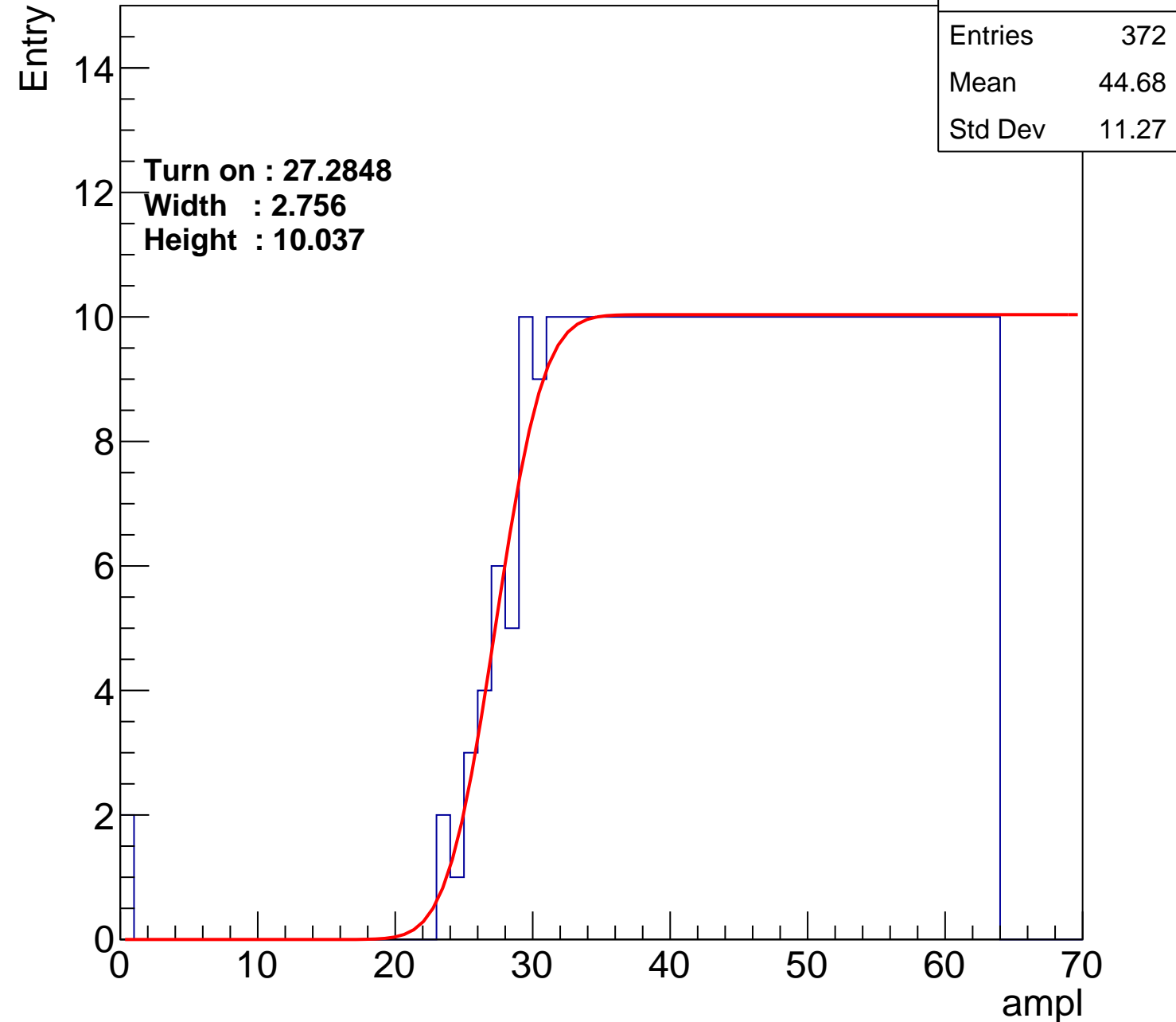
Width : 2.756

Height : 10.037

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch99

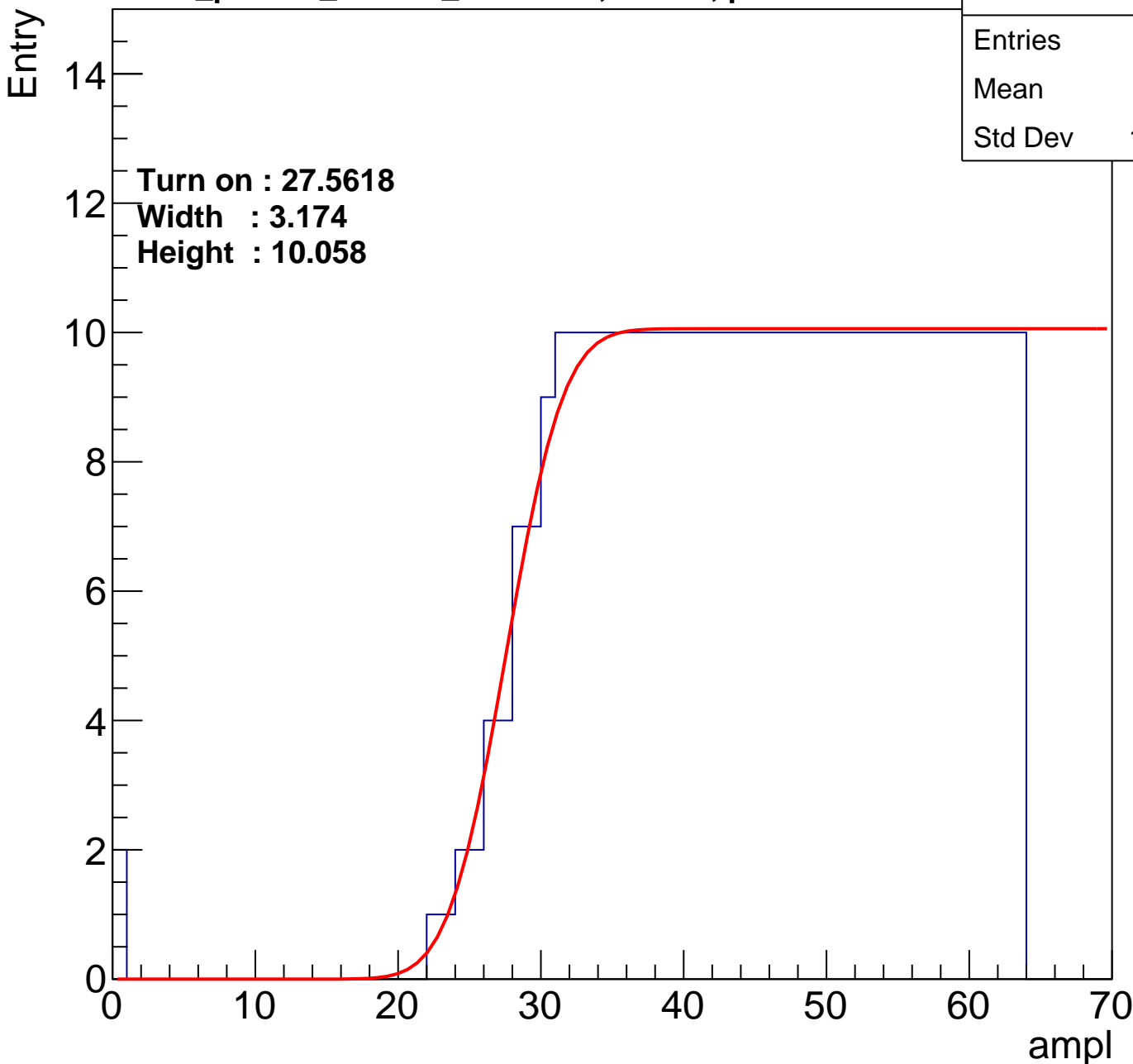
calib_packv5_042523_0143.root, FC#13, port D2

Turn on : 27.5618

Width : 3.174

Height : 10.058

Entries	369
Mean	44.81
Std Dev	11.23



B1L003S, U2-ch100

calib_packv5_042523_0143.root, FC#13, port D2

Entries	342
Mean	45.9
Std Dev	11.15

Turn on : 30.8098

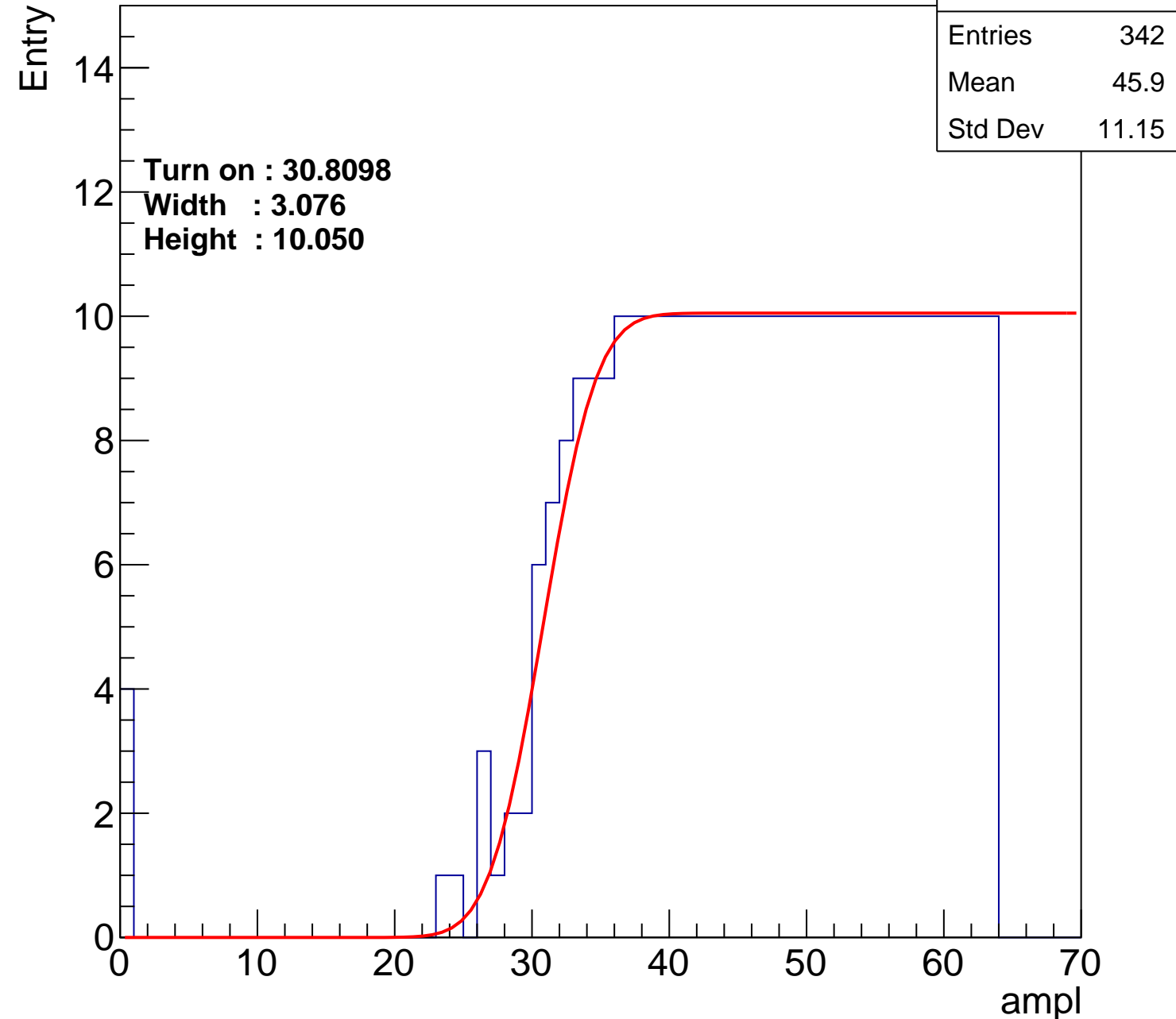
Width : 3.076

Height : 10.050

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch101

calib_packv5_042523_0143.root, FC#13, port D2

Entries	376
Mean	44.56
Std Dev	11.16

Turn on : 26.6684

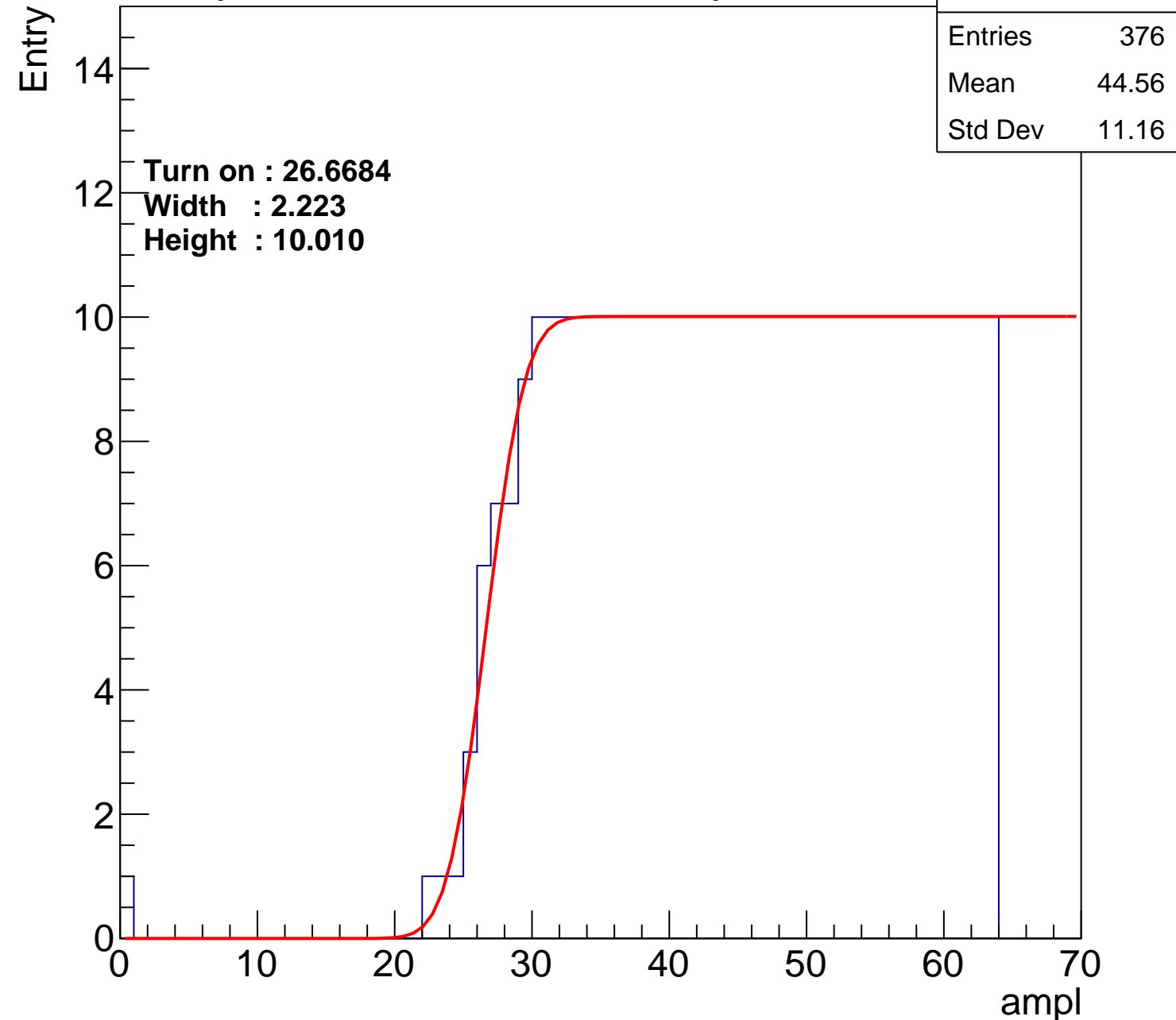
Width : 2.223

Height : 10.010

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch102

calib_packv5_042523_0143.root, FC#13, port D2

Entries	363
Mean	45.12
Std Dev	11.04

Turn on : 28.0493

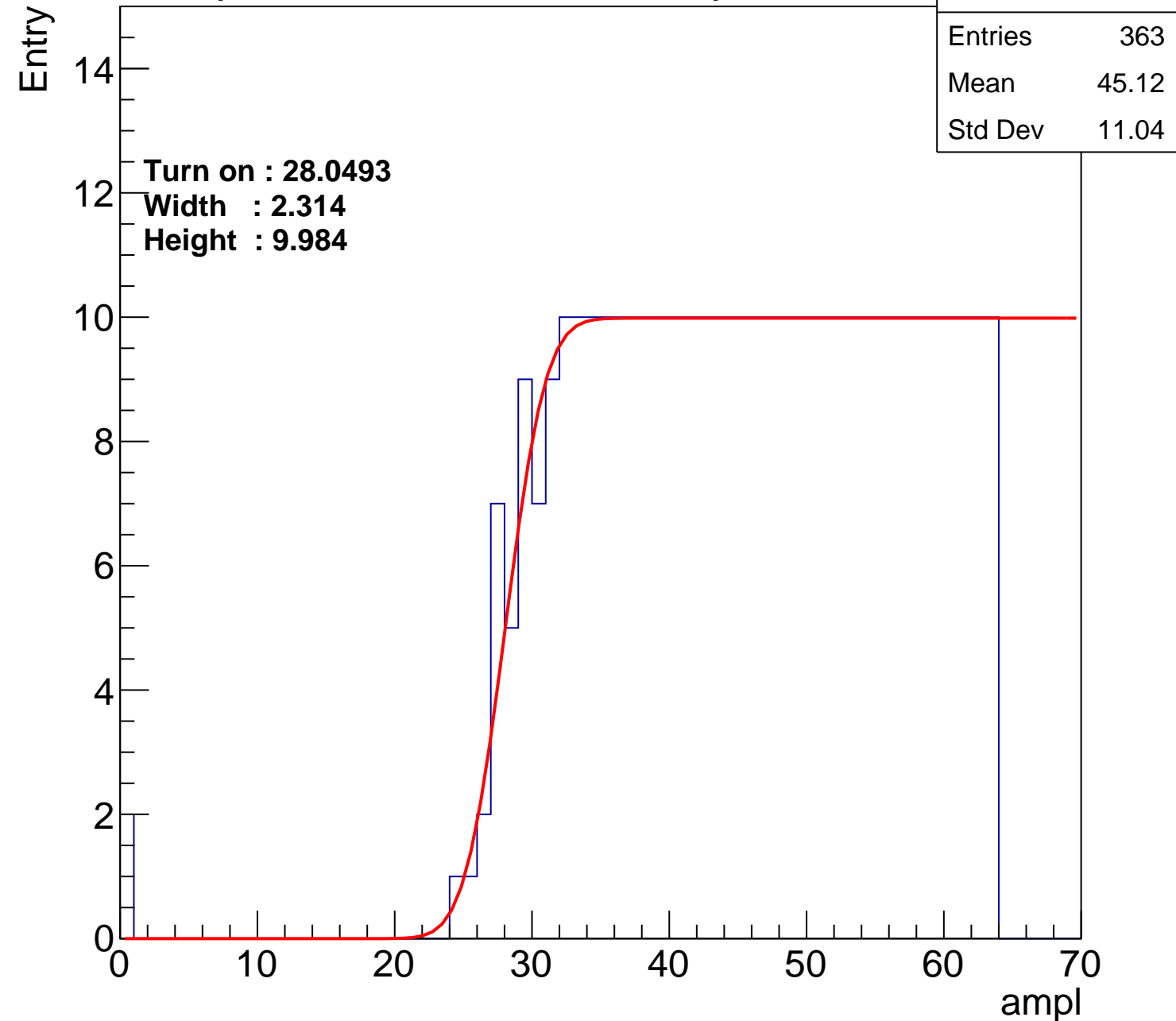
Width : 2.314

Height : 9.984

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch103

calib_packv5_042523_0143.root, FC#13, port D2

Entries	377
Mean	44.37
Std Dev	11.57

Turn on : 26.5926

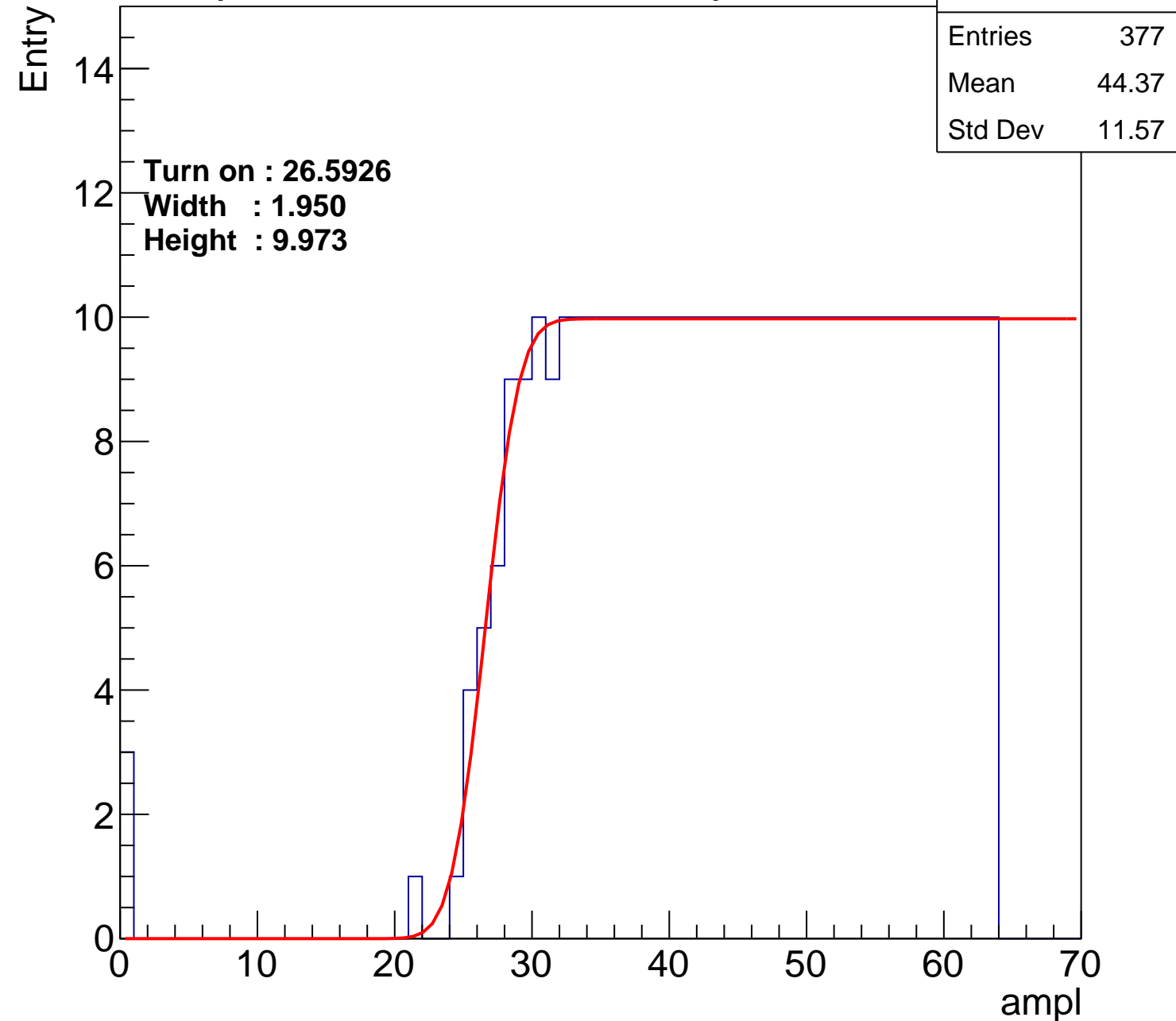
Width : 1.950

Height : 9.973

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch104

calib_packv5_042523_0143.root, FC#13, port D2

Entries	381
Mean	44.11
Std Dev	11.79

Turn on : 26.4475

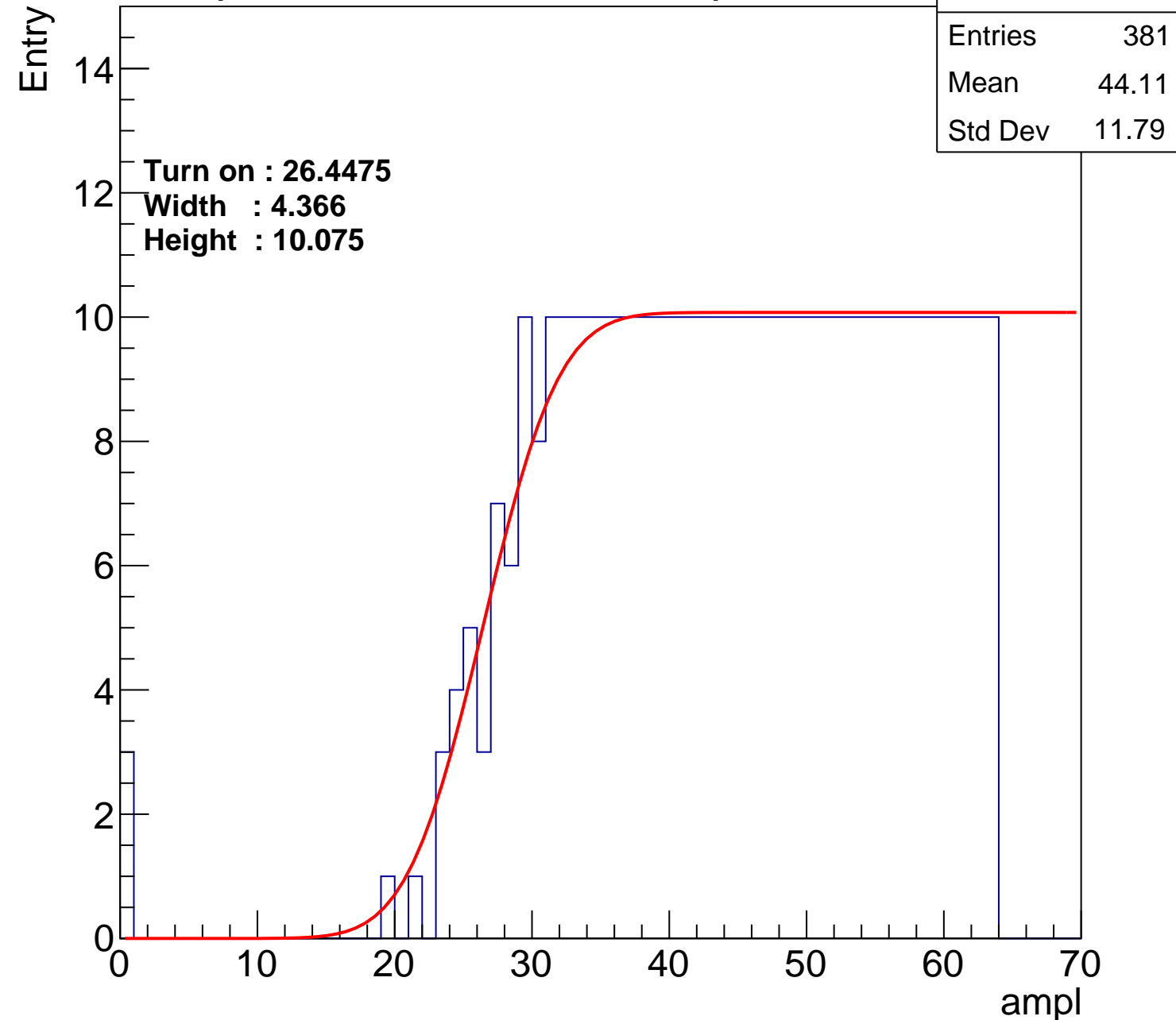
Width : 4.366

Height : 10.075

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch105

calib_packv5_042523_0143.root, FC#13, port D2

Entries	352
Mean	45.43
Std Dev	11.33

Turn on : 29.0456

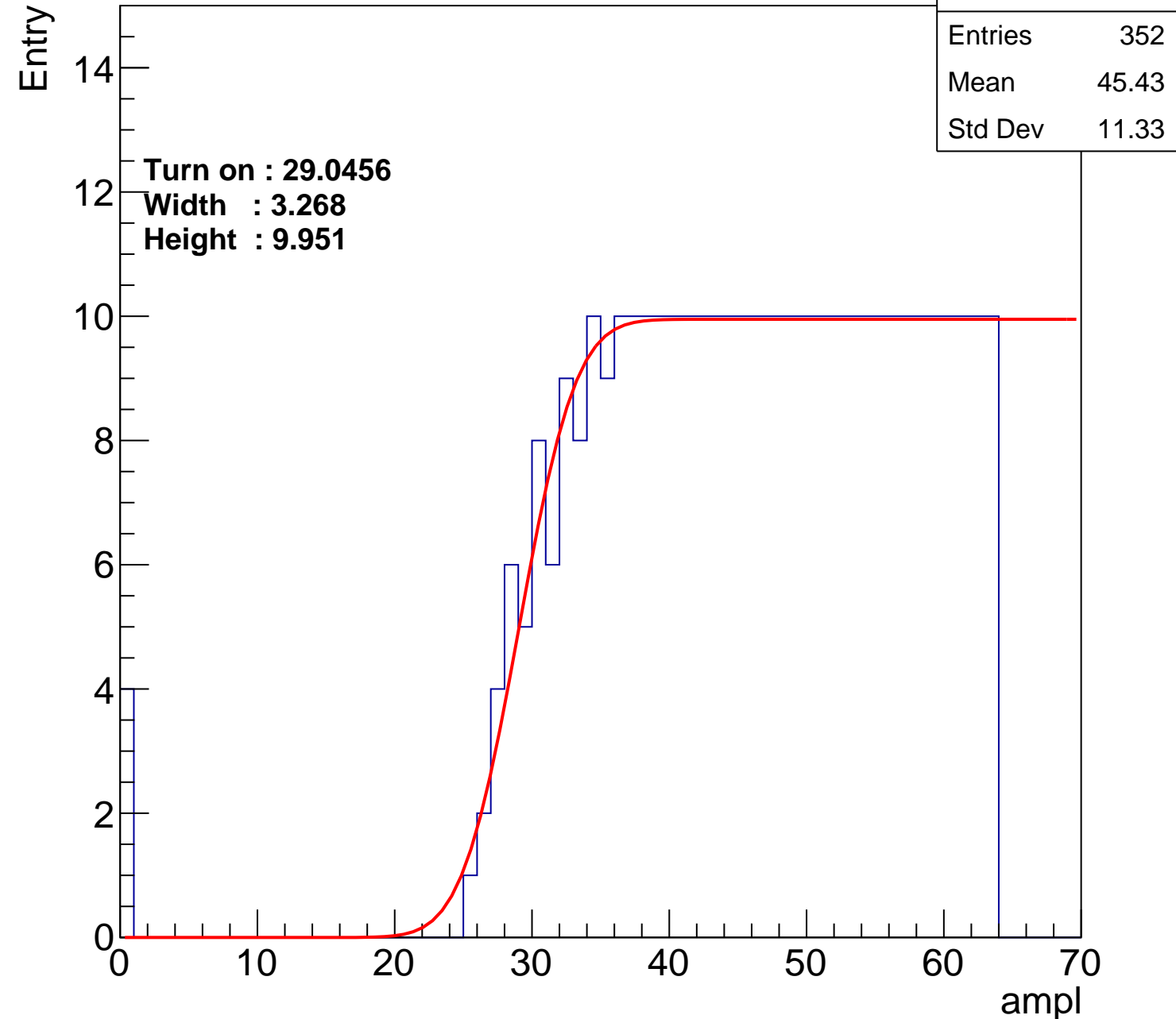
Width : 3.268

Height : 9.951

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch106

calib_packv5_042523_0143.root, FC#13, port D2

Entries	389
Mean	43.81
Std Dev	11.75

Turn on : 25.7797

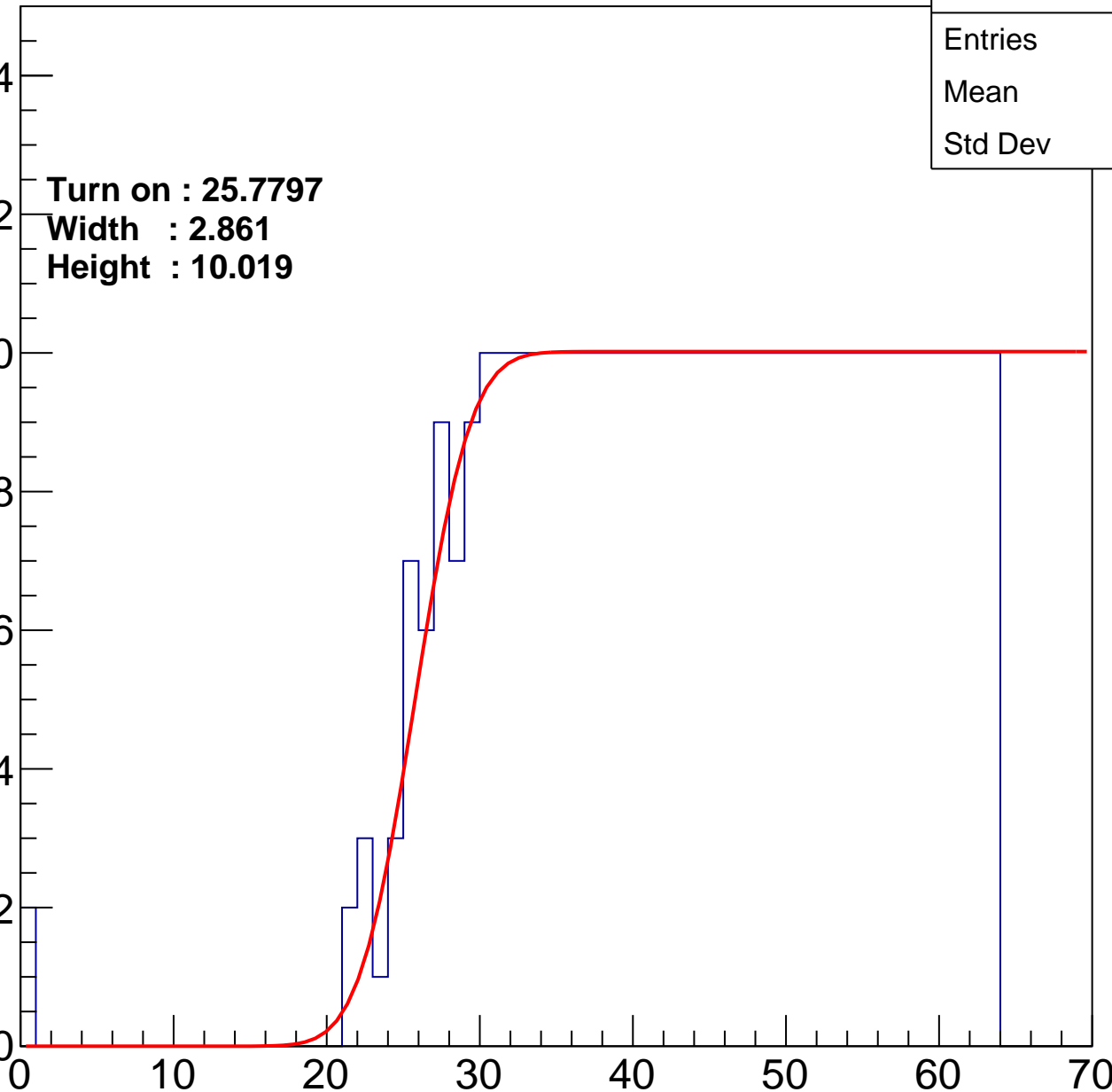
Width : 2.861

Height : 10.019

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch107

calib_packv5_042523_0143.root, FC#13, port D2

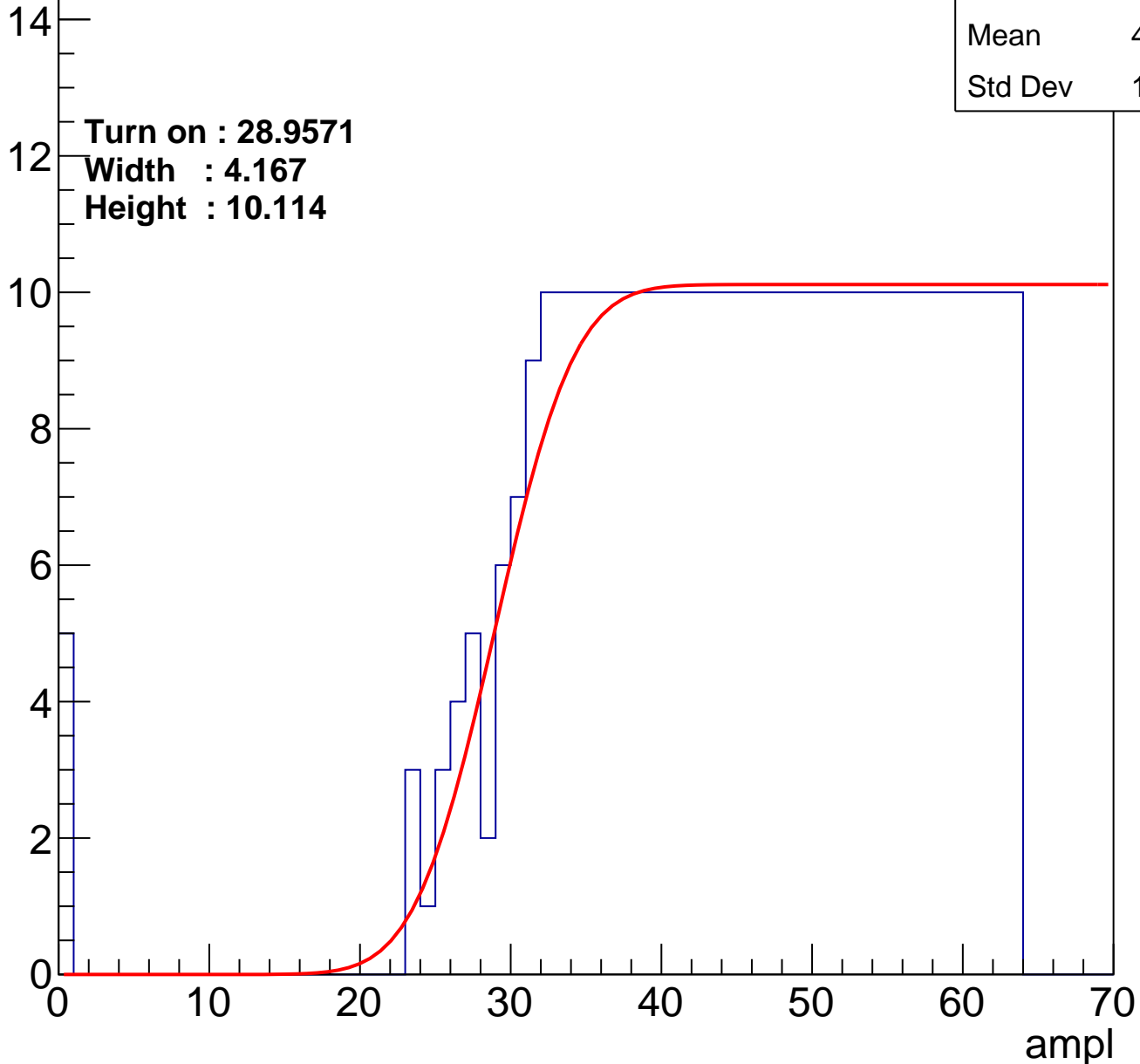
Entries	365
Mean	44.73
Std Dev	11.82

Turn on : 28.9571

Width : 4.167

Height : 10.114

Entry



B1L003S, U2-ch108

calib_packv5_042523_0143.root, FC#13, port D2

Entries	375
Mean	44.49
Std Dev	11.41

Turn on : 26.9302

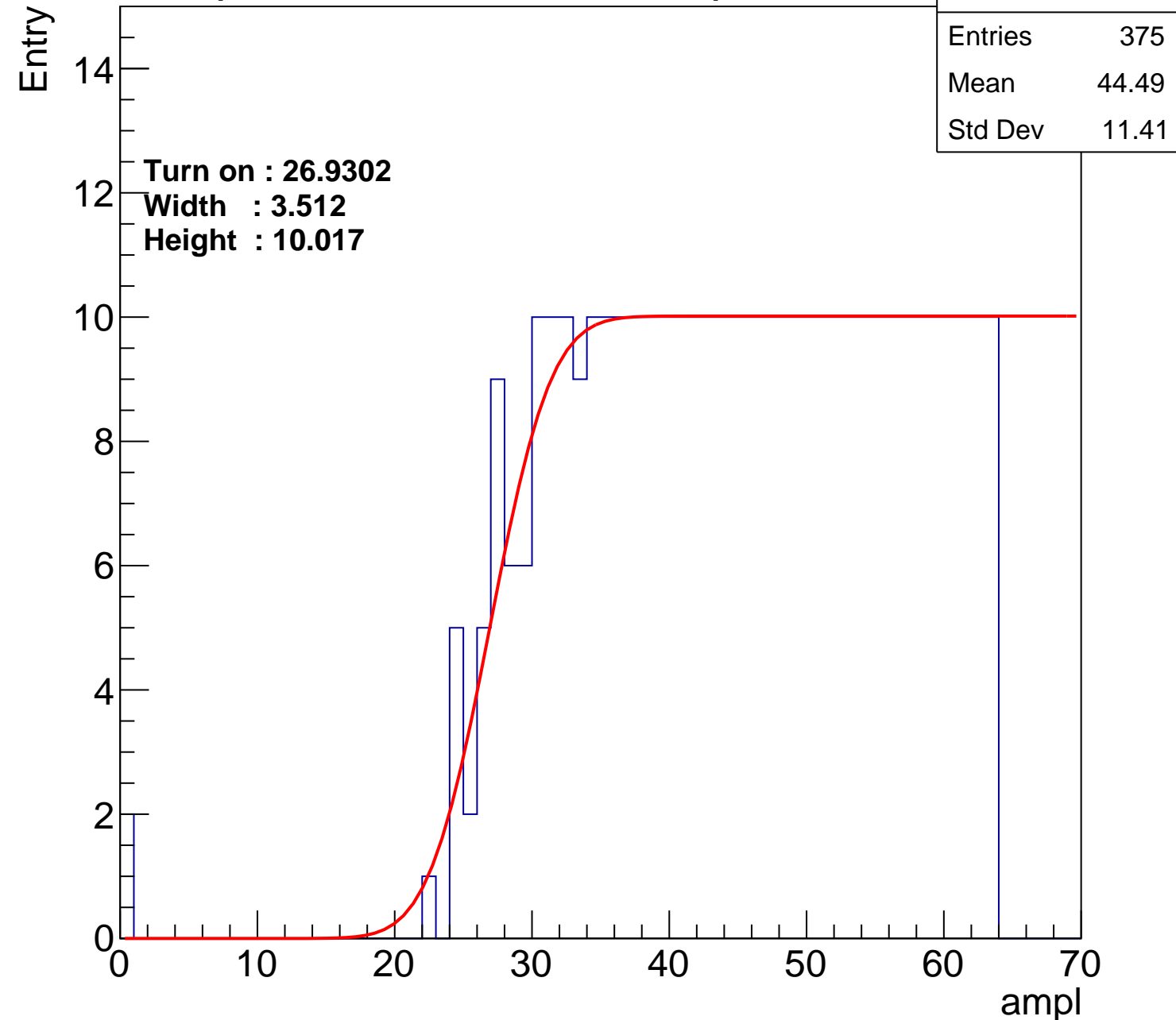
Width : 3.512

Height : 10.017

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch109

calib_packv5_042523_0143.root, FC#13, port D2

Entries	374
Mean	44.44
Std Dev	11.63

Turn on : 26.9901

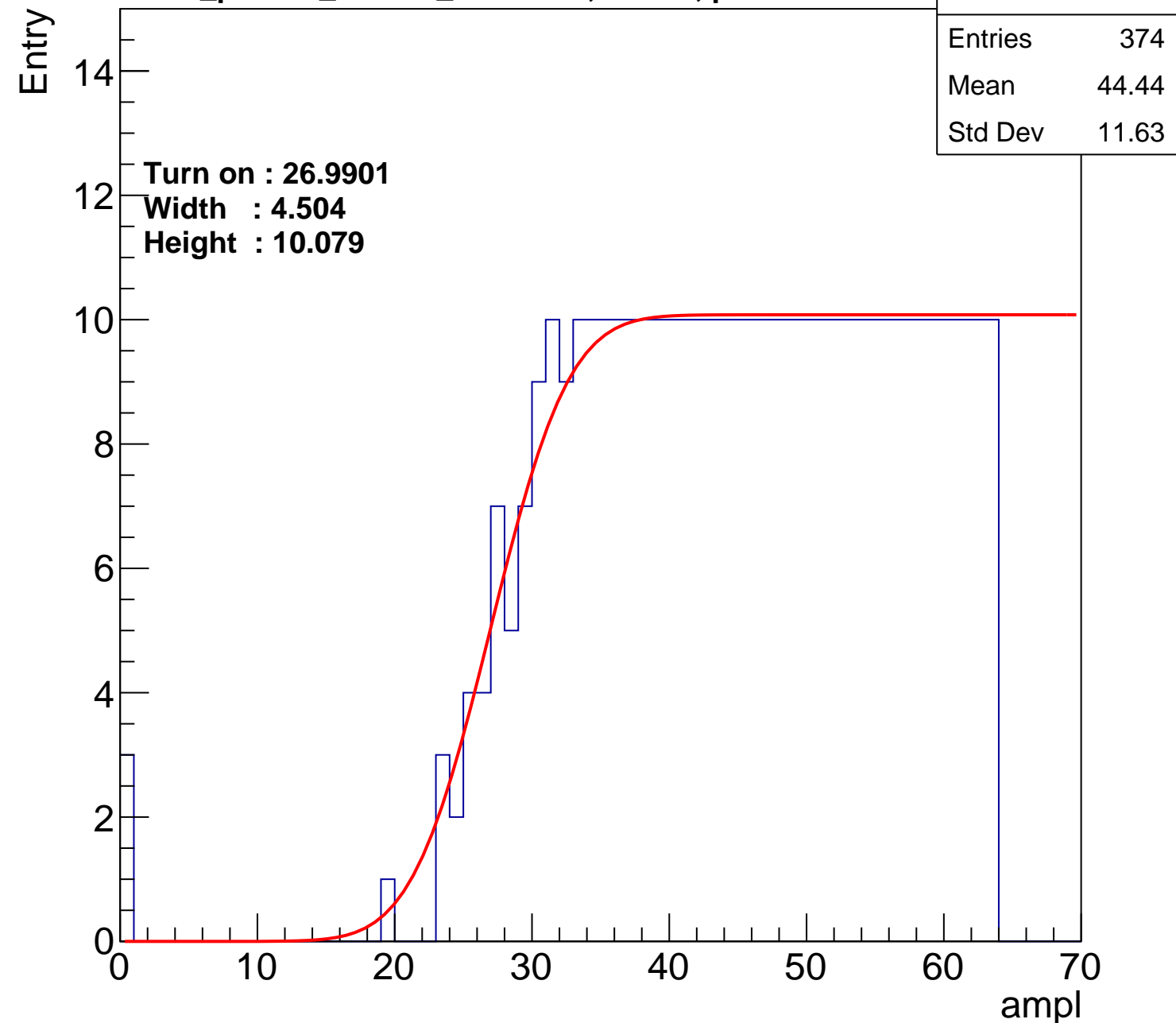
Width : 4.504

Height : 10.079

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch110

calib_packv5_042523_0143.root, FC#13, port D2

Entries	373
Mean	44.61
Std Dev	11.33

Turn on : 27.1506

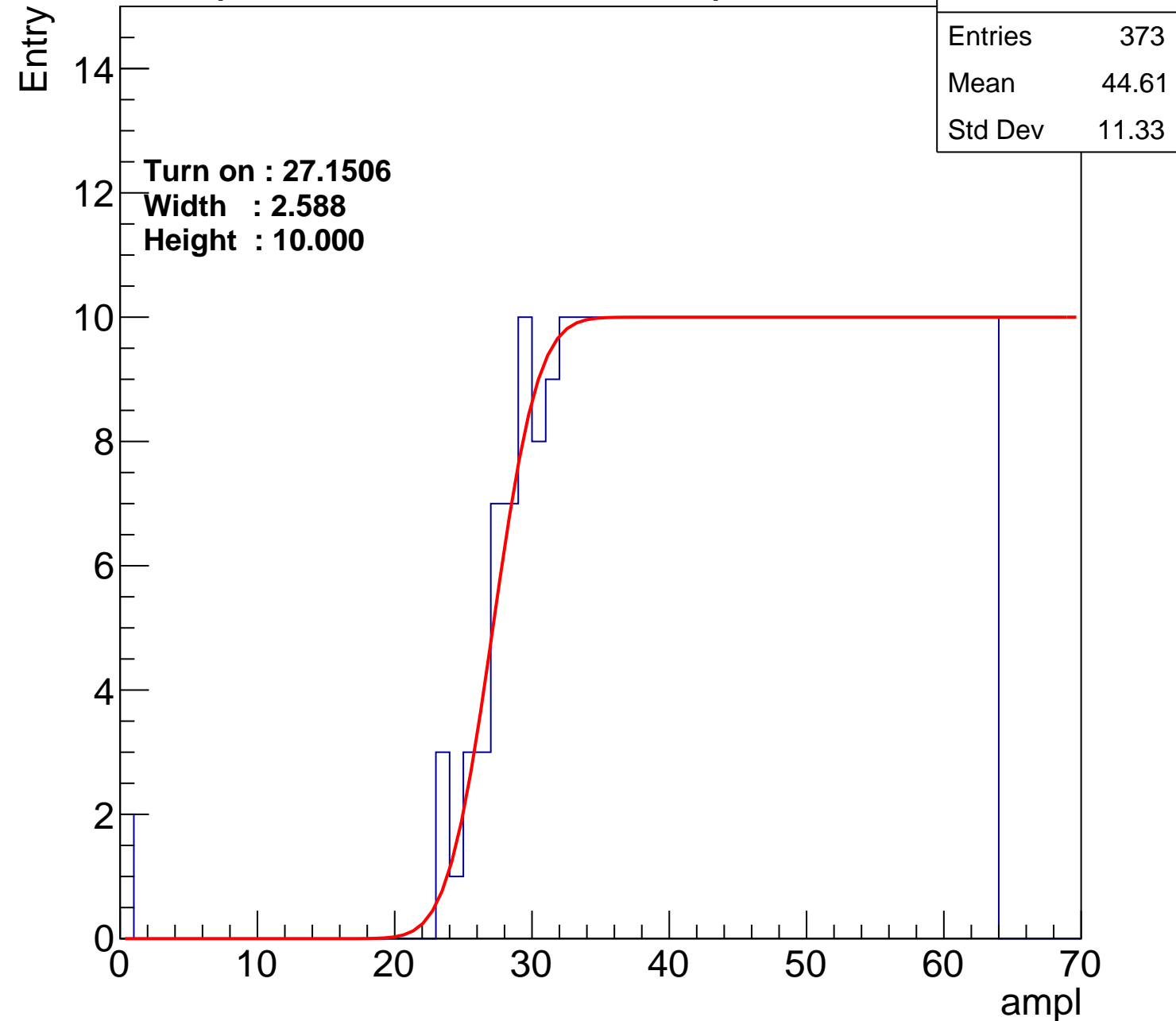
Width : 2.588

Height : 10.000

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch111

calib_packv5_042523_0143.root, FC#13, port D2

Entries	368
Mean	44.75
Std Dev	11.39

Turn on : 28.4408

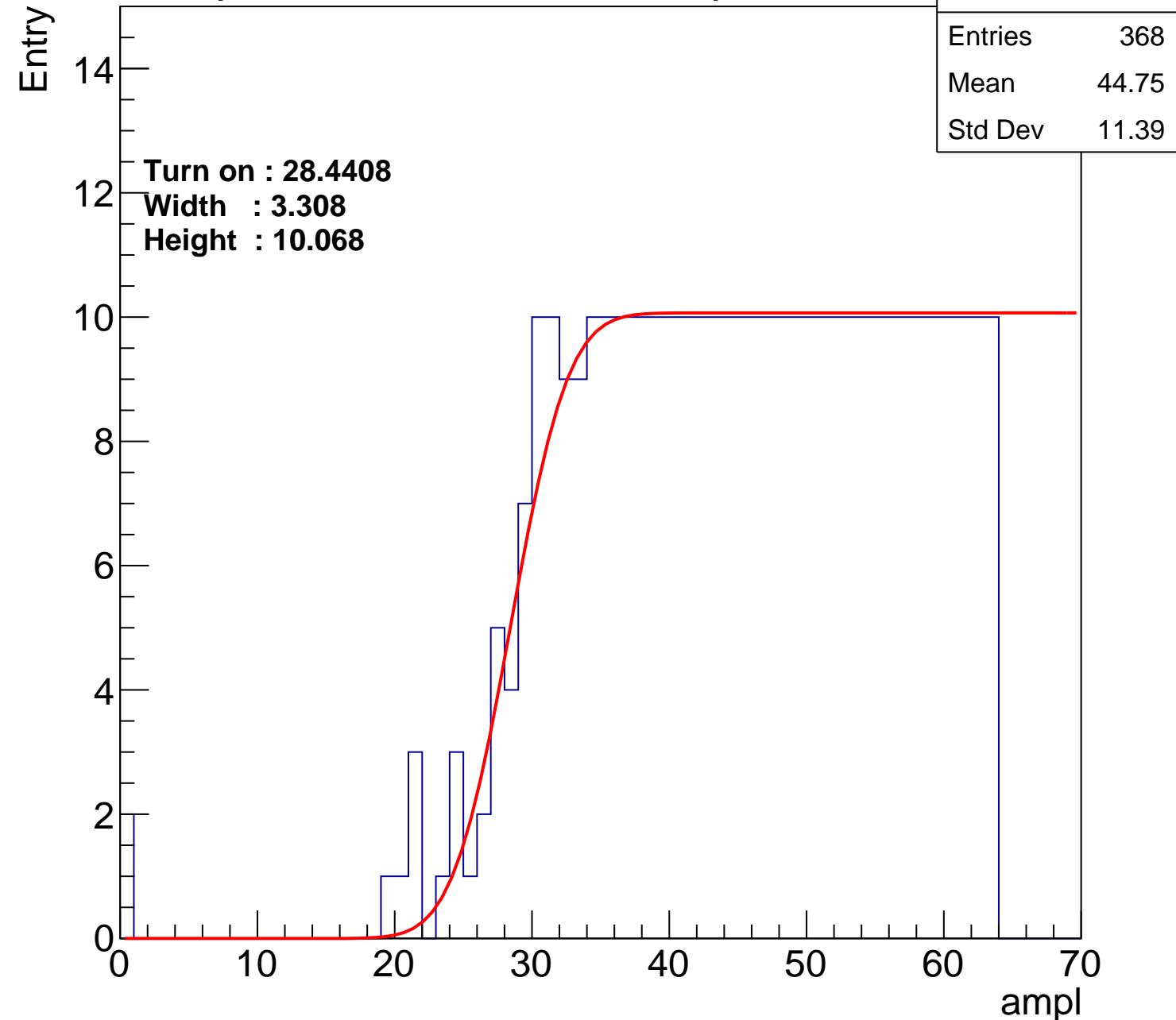
Width : 3.308

Height : 10.068

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch112

calib_packv5_042523_0143.root, FC#13, port D2

Entries	368
Mean	44.91
Std Dev	11.03

Turn on : 27.3595

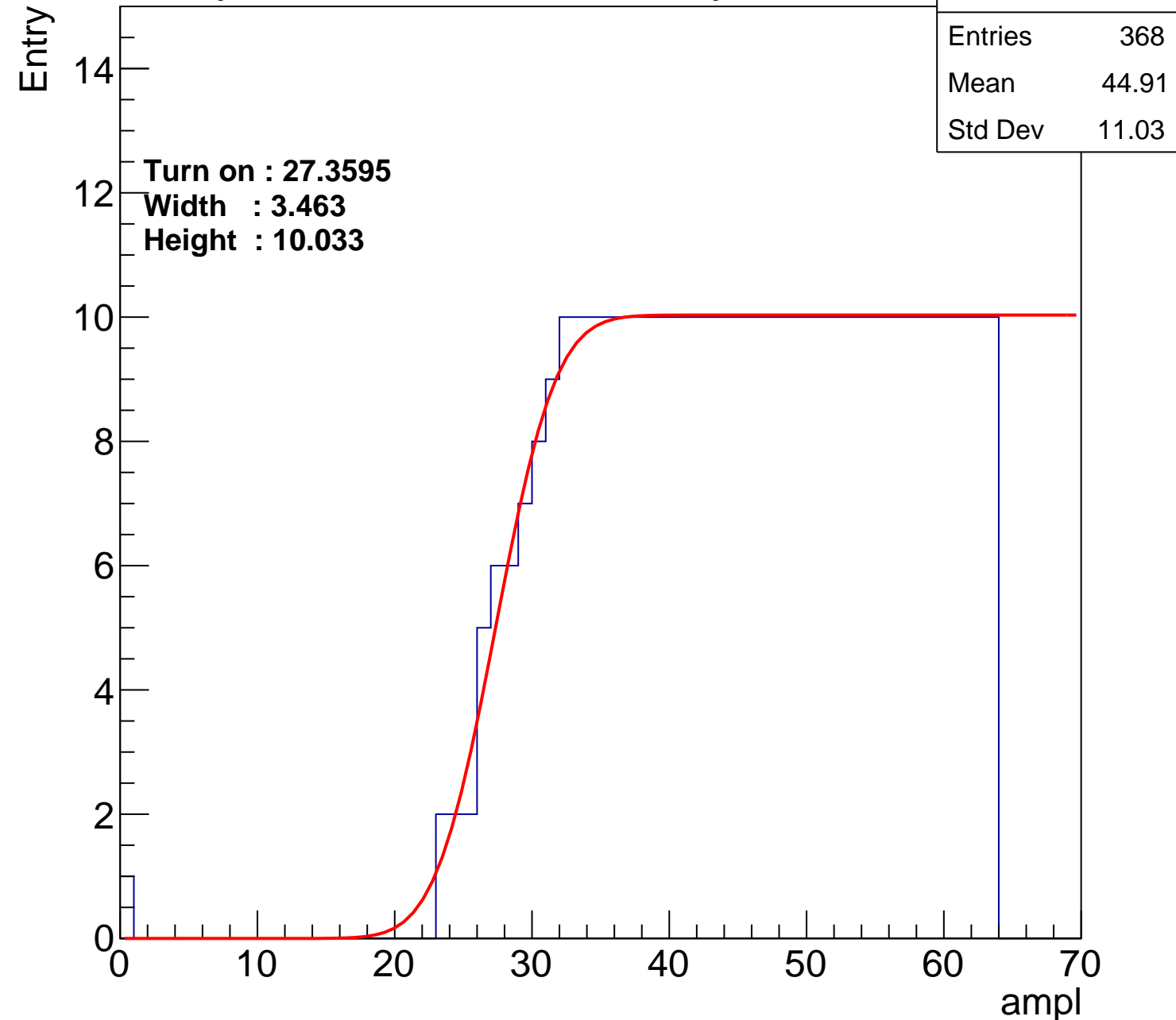
Width : 3.463

Height : 10.033

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch113

calib_packv5_042523_0143.root, FC#13, port D2

Entries	380
Mean	44.11
Std Dev	11.91

Turn on : 26.9863

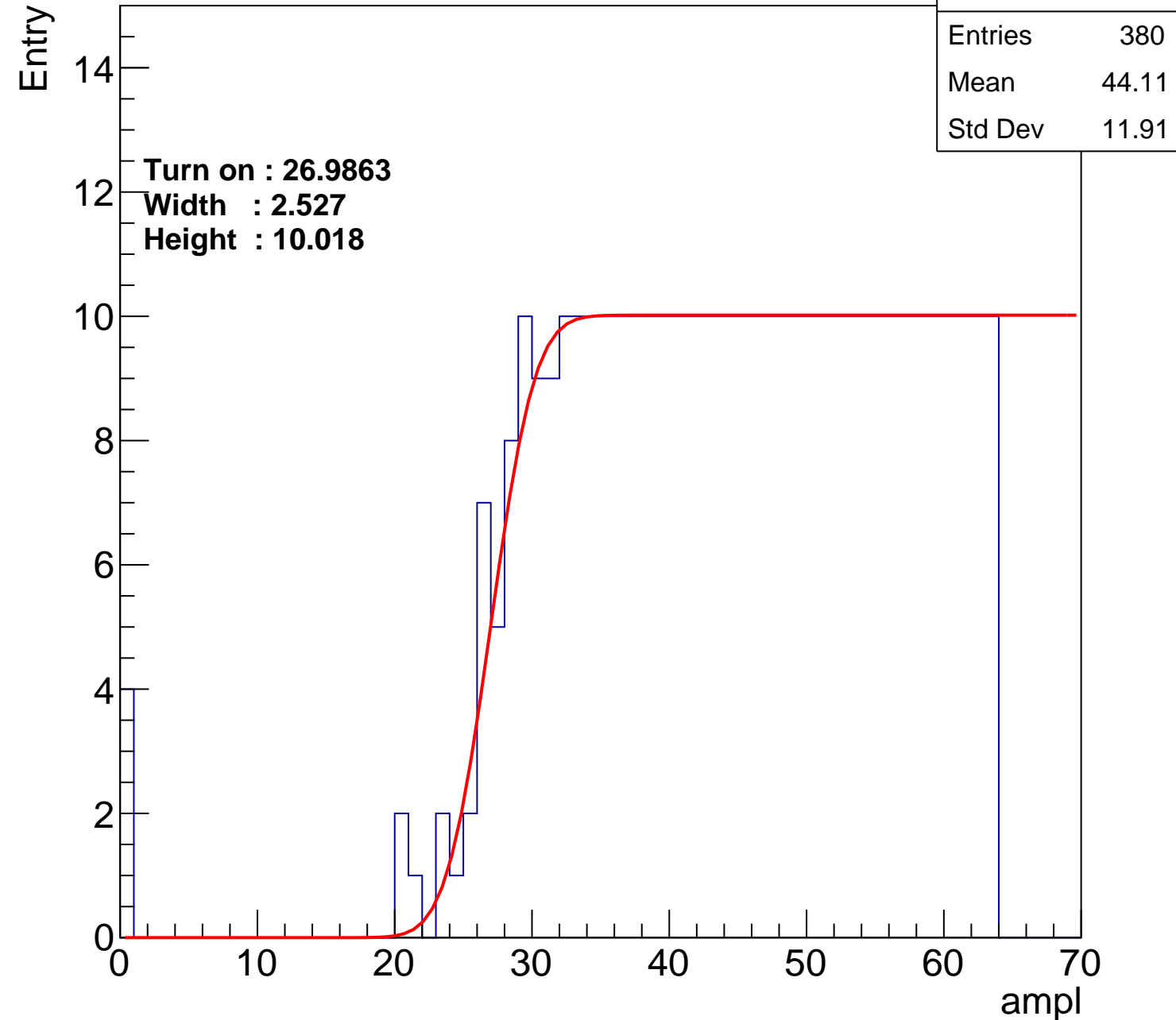
Width : 2.527

Height : 10.018

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch114

calib_packv5_042523_0143.root, FC#13, port D2

Entries	372
Mean	44.59
Std Dev	11.49

Turn on : 27.0623

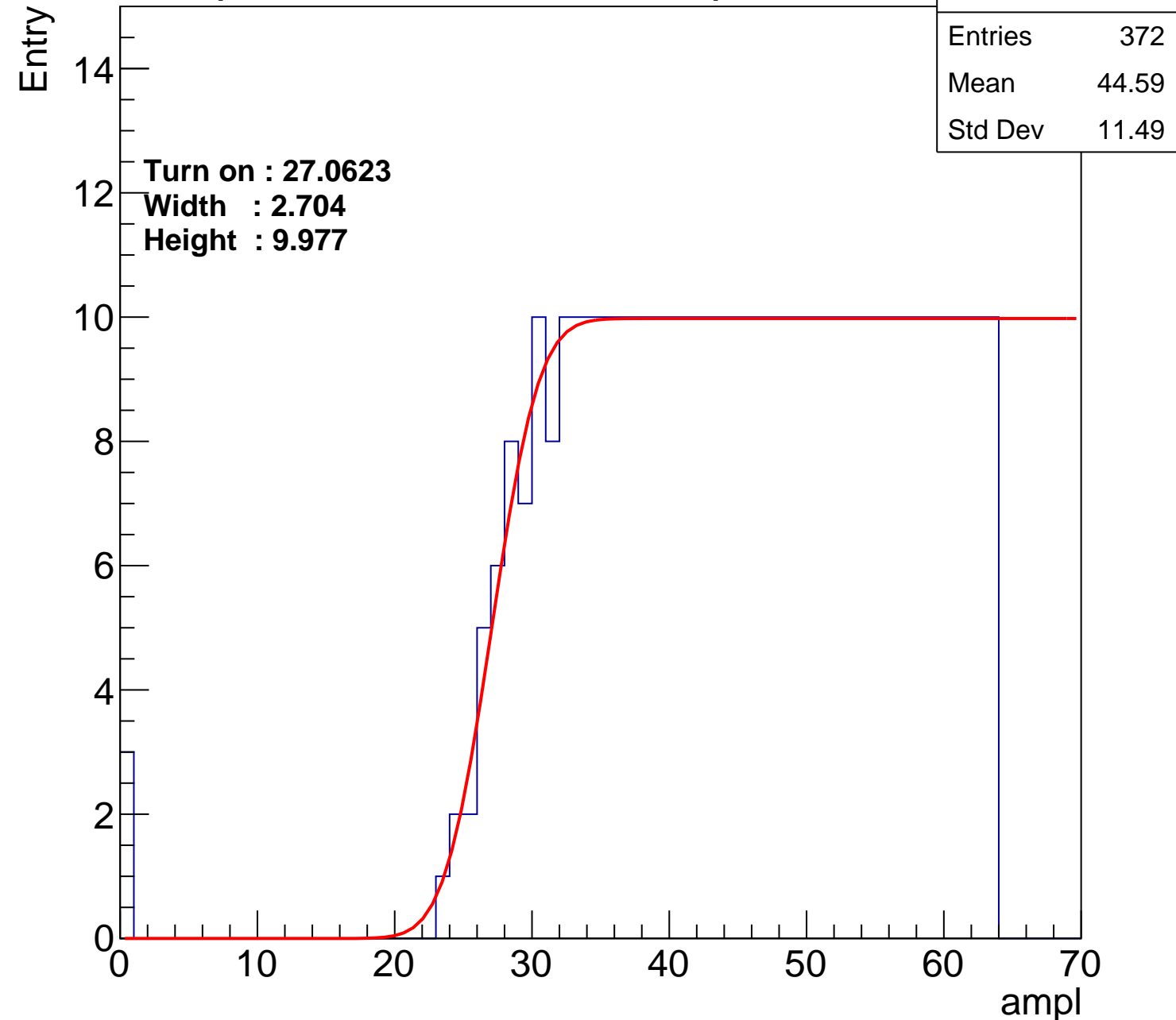
Width : 2.704

Height : 9.977

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch115

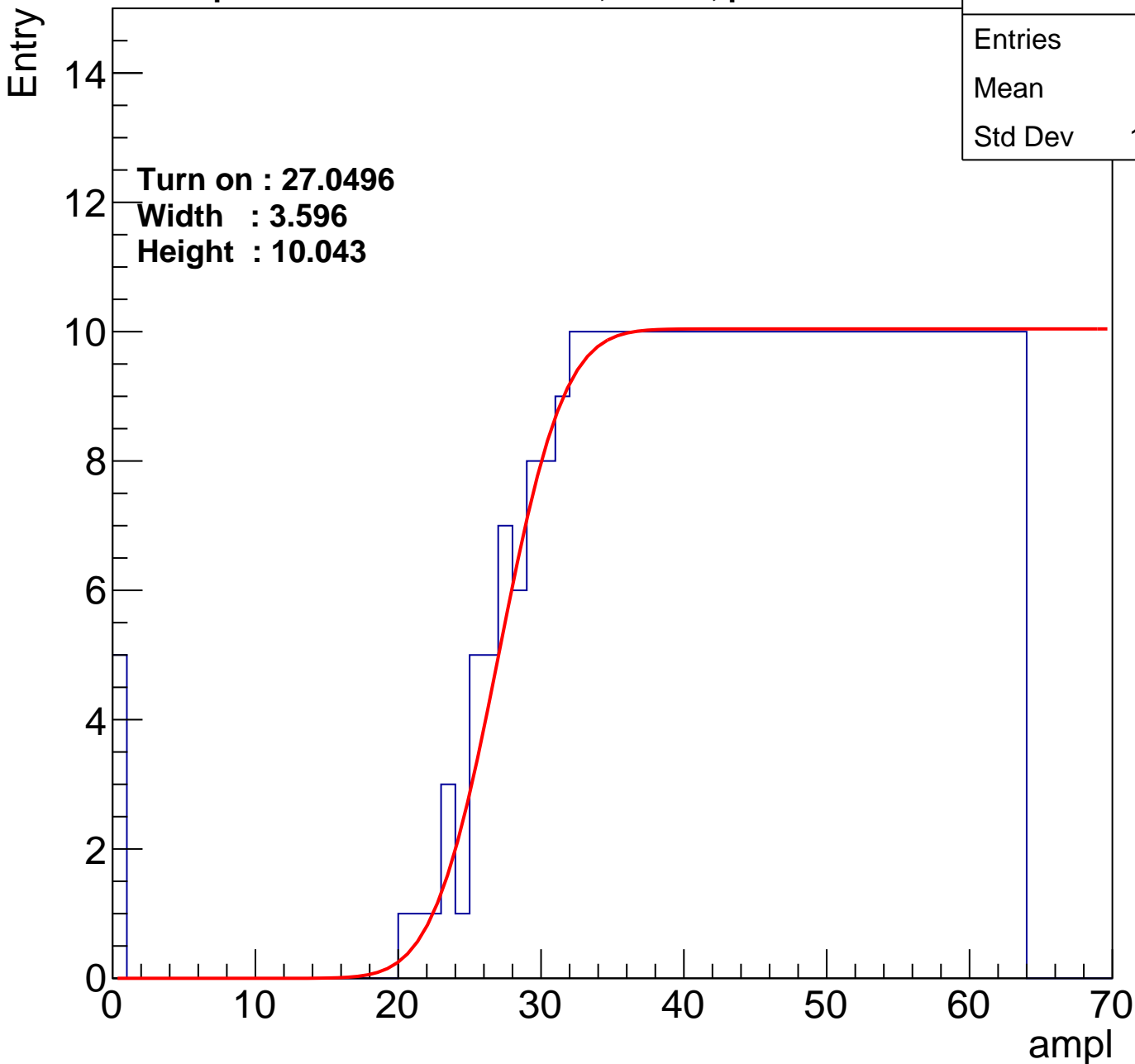
calib_packv5_042523_0143.root, FC#13, port D2

Entries	380
Mean	44
Std Dev	12.15

Turn on : 27.0496

Width : 3.596

Height : 10.043



B1L003S, U2-ch116

calib_packv5_042523_0143.root, FC#13, port D2

Entries	363
Mean	45.09
Std Dev	11.11

Turn on : 28.7081

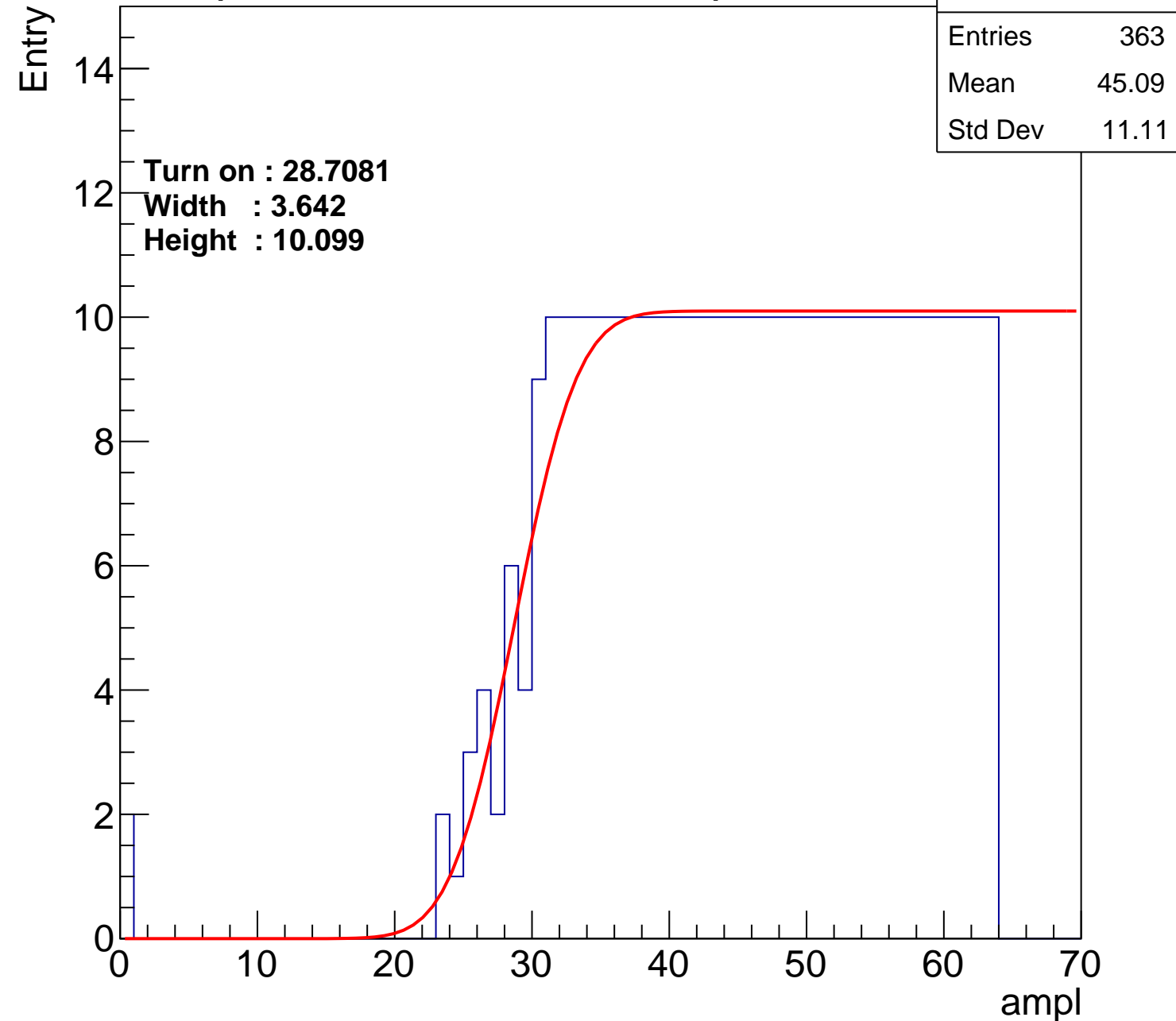
Width : 3.642

Height : 10.099

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch117

calib_packv5_042523_0143.root, FC#13, port D2

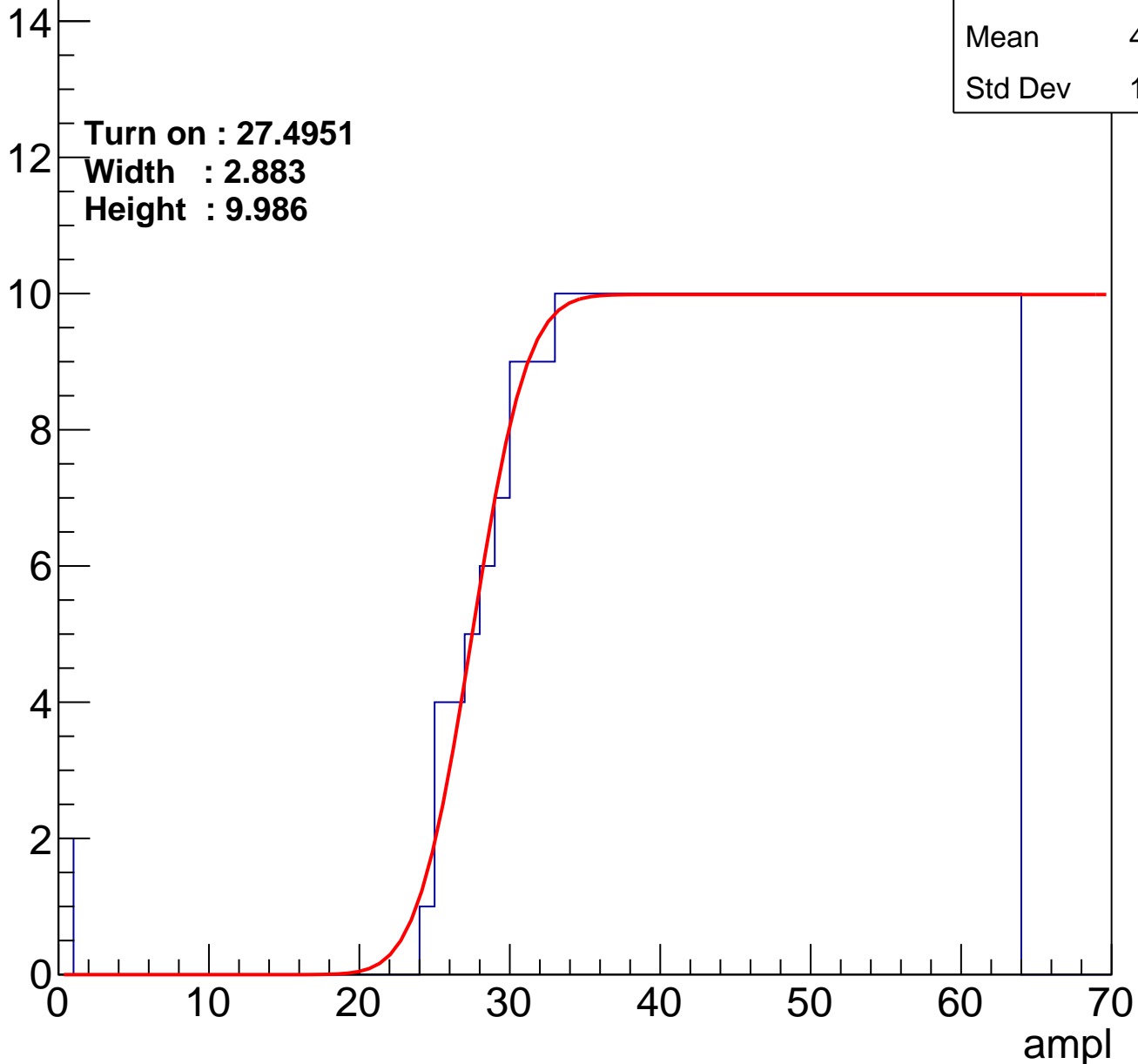
Entries	366
Mean	44.95
Std Dev	11.16

Turn on : 27.4951

Width : 2.883

Height : 9.986

Entry



B1L003S, U2-ch118

calib_packv5_042523_0143.root, FC#13, port D2

Entries	353
Mean	45.55
Std Dev	11

Turn on : 29.3695

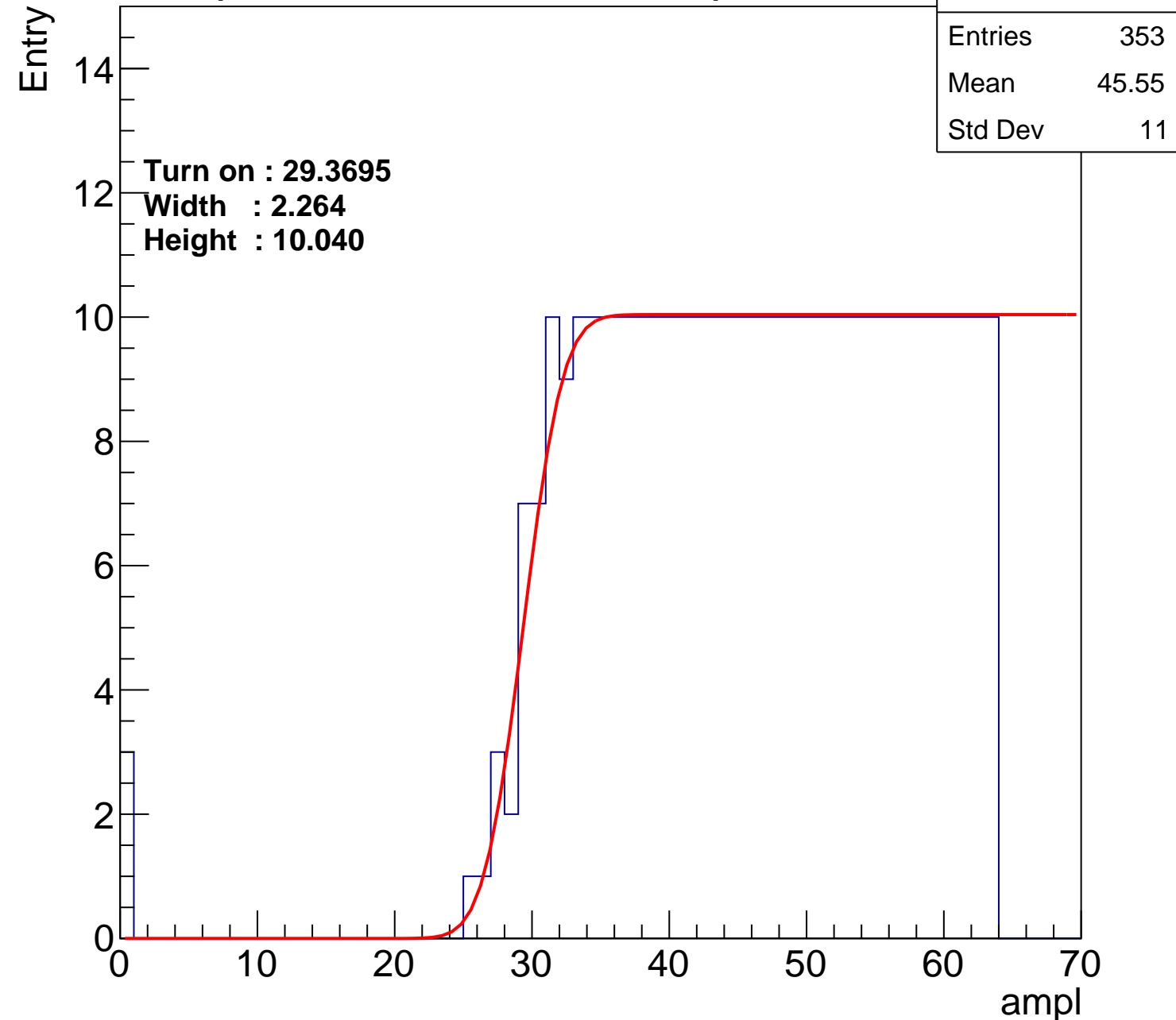
Width : 2.264

Height : 10.040

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch119

calib_packv5_042523_0143.root, FC#13, port D2

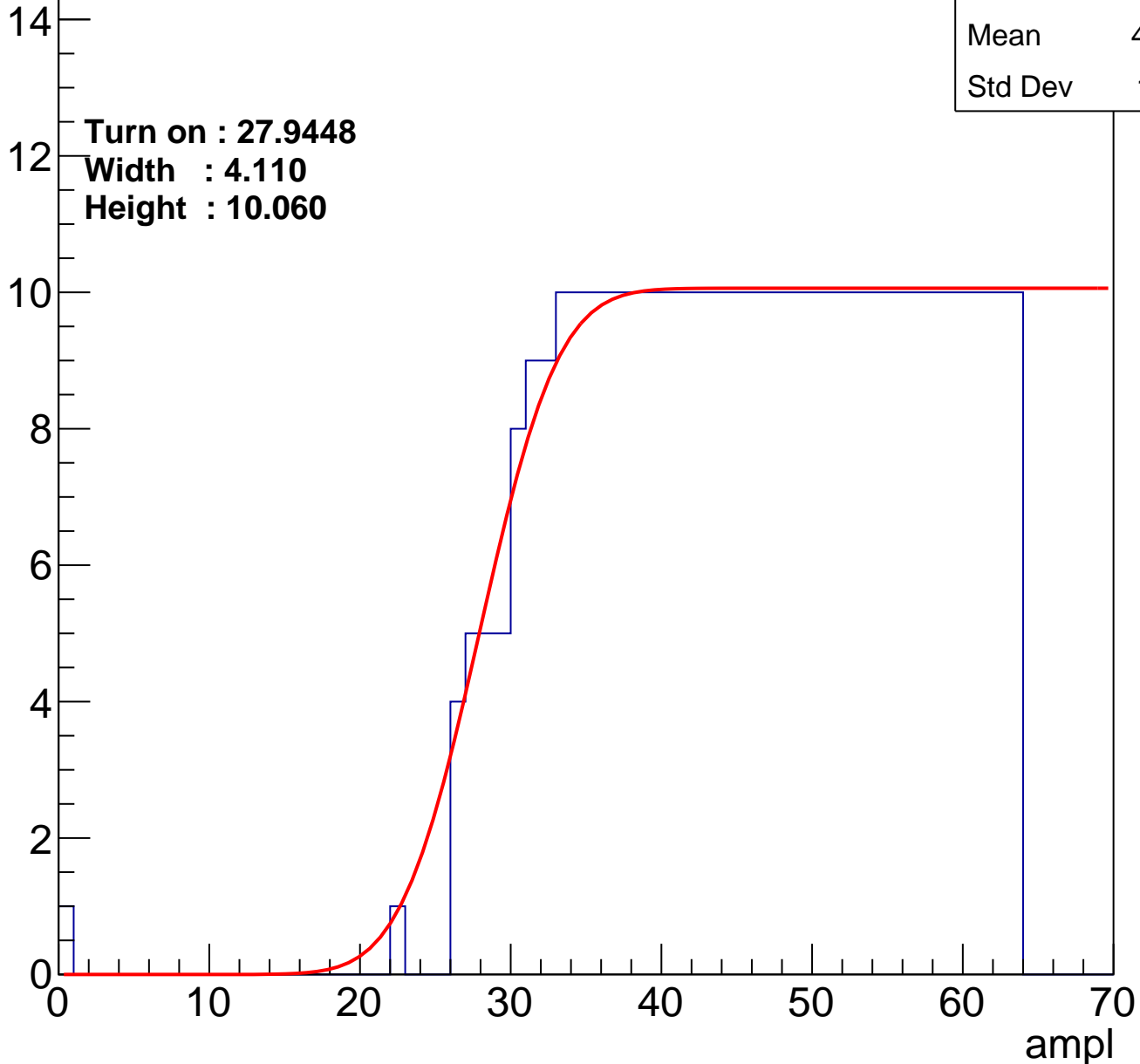
Entries	357
Mean	45.47
Std Dev	10.71

Turn on : 27.9448

Width : 4.110

Height : 10.060

Entry



B1L003S, U2-ch120

calib_packv5_042523_0143.root, FC#13, port D2

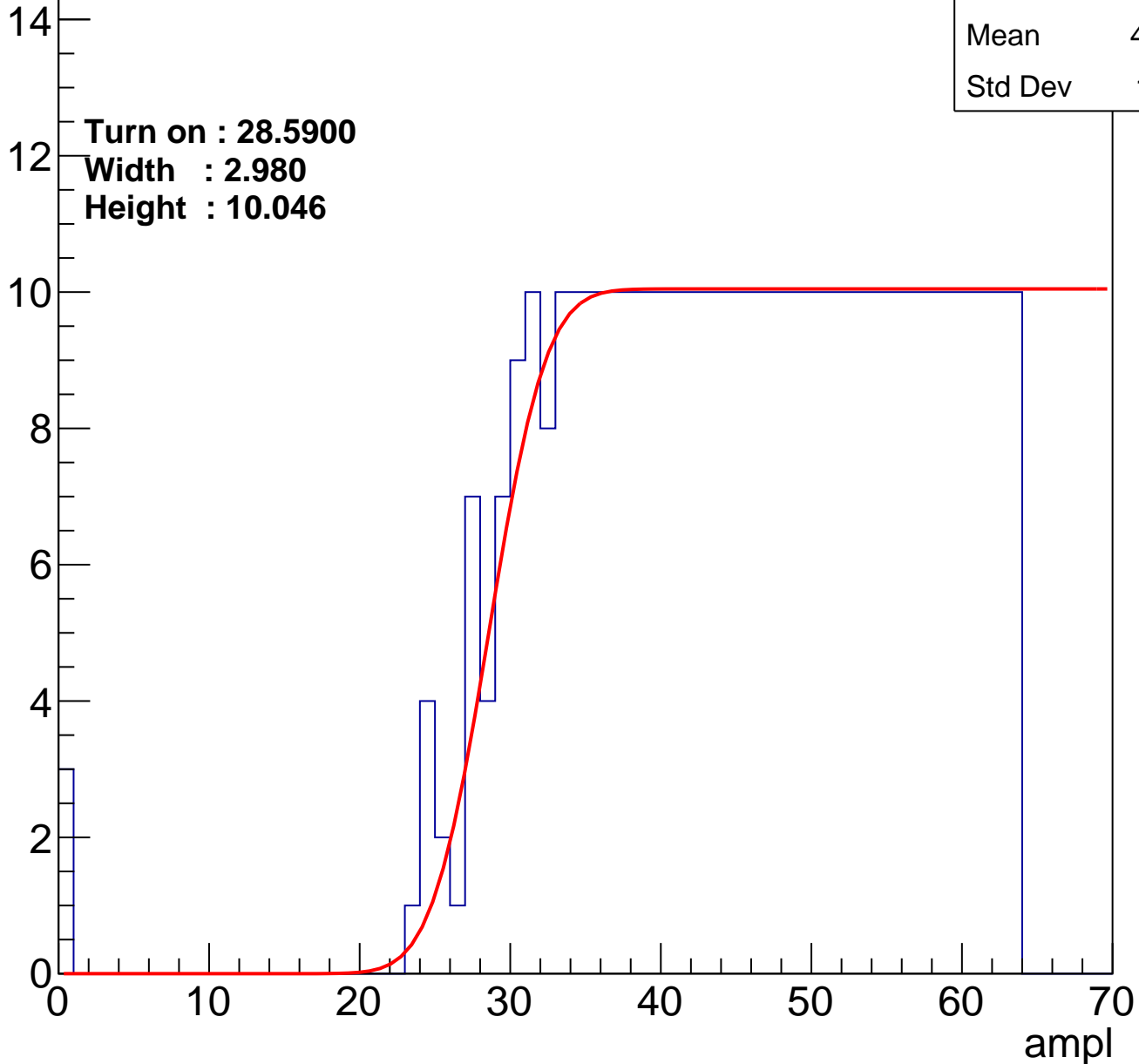
Entries	366
Mean	44.85
Std Dev	11.41

Turn on : 28.5900

Width : 2.980

Height : 10.046

Entry



B1L003S, U2-ch121

calib_packv5_042523_0143.root, FC#13, port D2

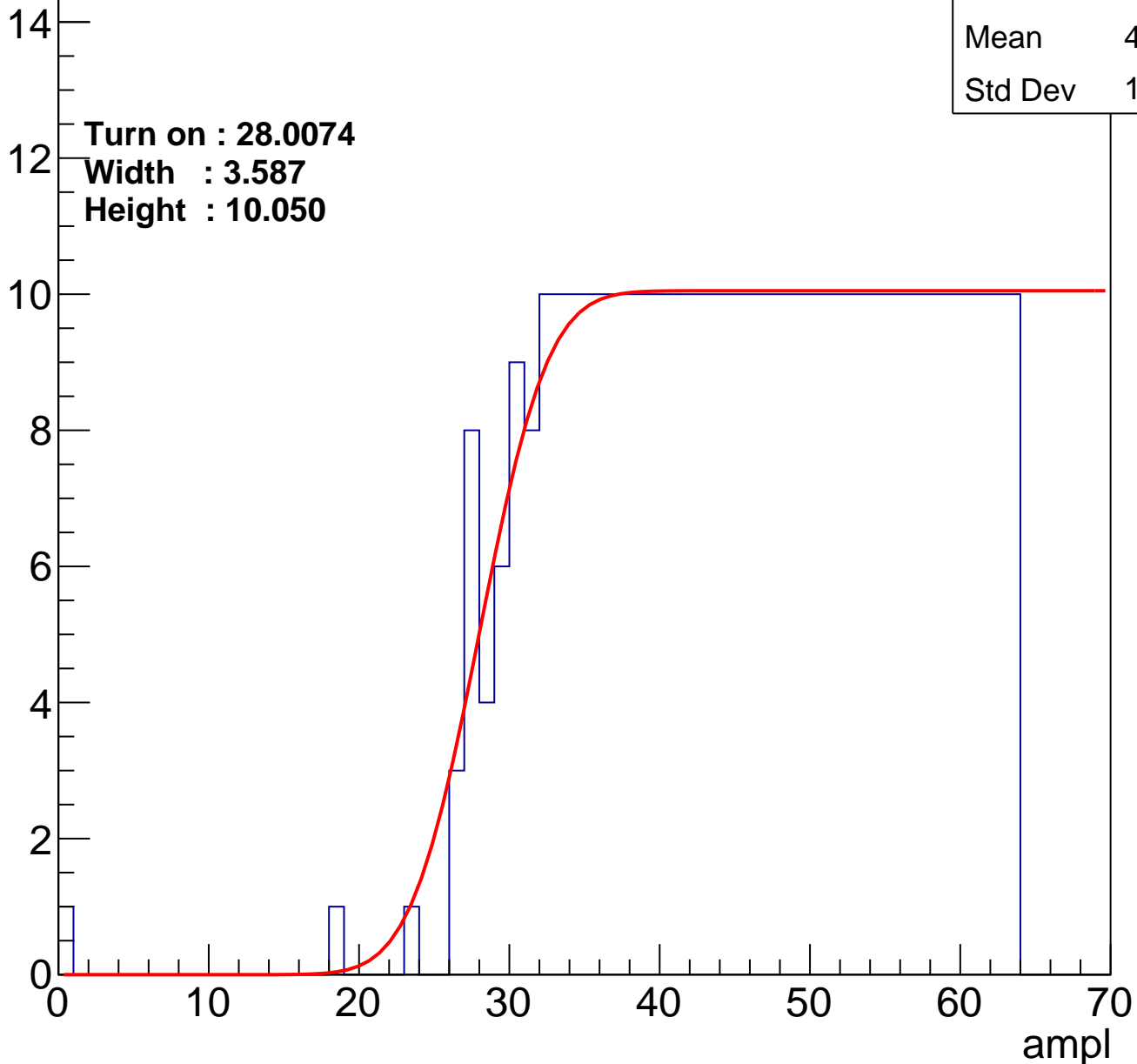
Entries	361
Mean	45.26
Std Dev	10.84

Turn on : 28.0074

Width : 3.587

Height : 10.050

Entry



B1L003S, U2-ch122

calib_packv5_042523_0143.root, FC#13, port D2

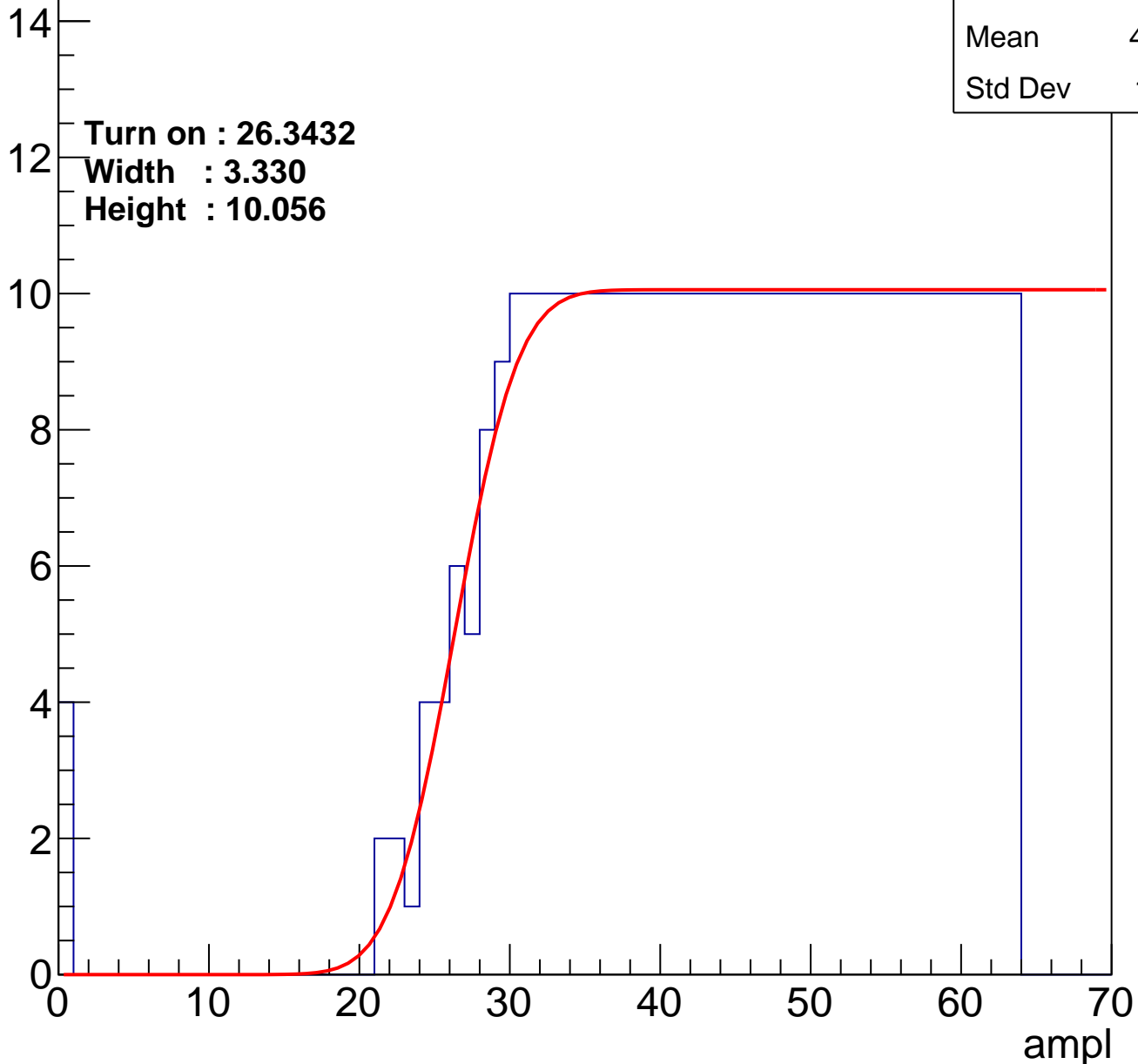
Entries	385
Mean	43.87
Std Dev	12.01

Turn on : 26.3432

Width : 3.330

Height : 10.056

Entry



B1L003S, U2-ch123

calib_packv5_042523_0143.root, FC#13, port D2

Entries	377
Mean	44.44
Std Dev	11.39

Turn on : 26.4653

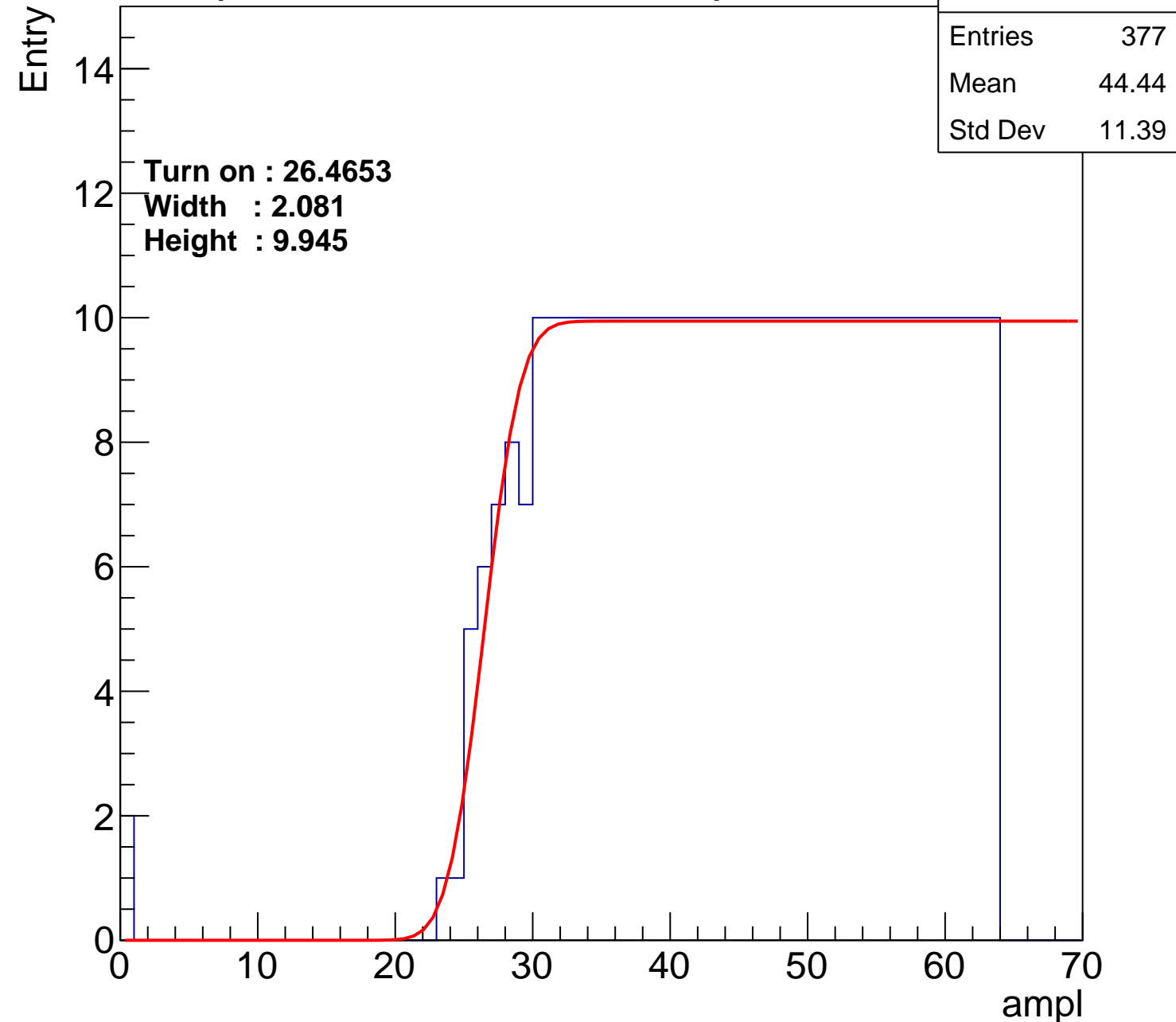
Width : 2.081

Height : 9.945

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch124

calib_packv5_042523_0143.root, FC#13, port D2

Entries	346
Mean	45.79
Std Dev	11.01

Turn on : 30.3928

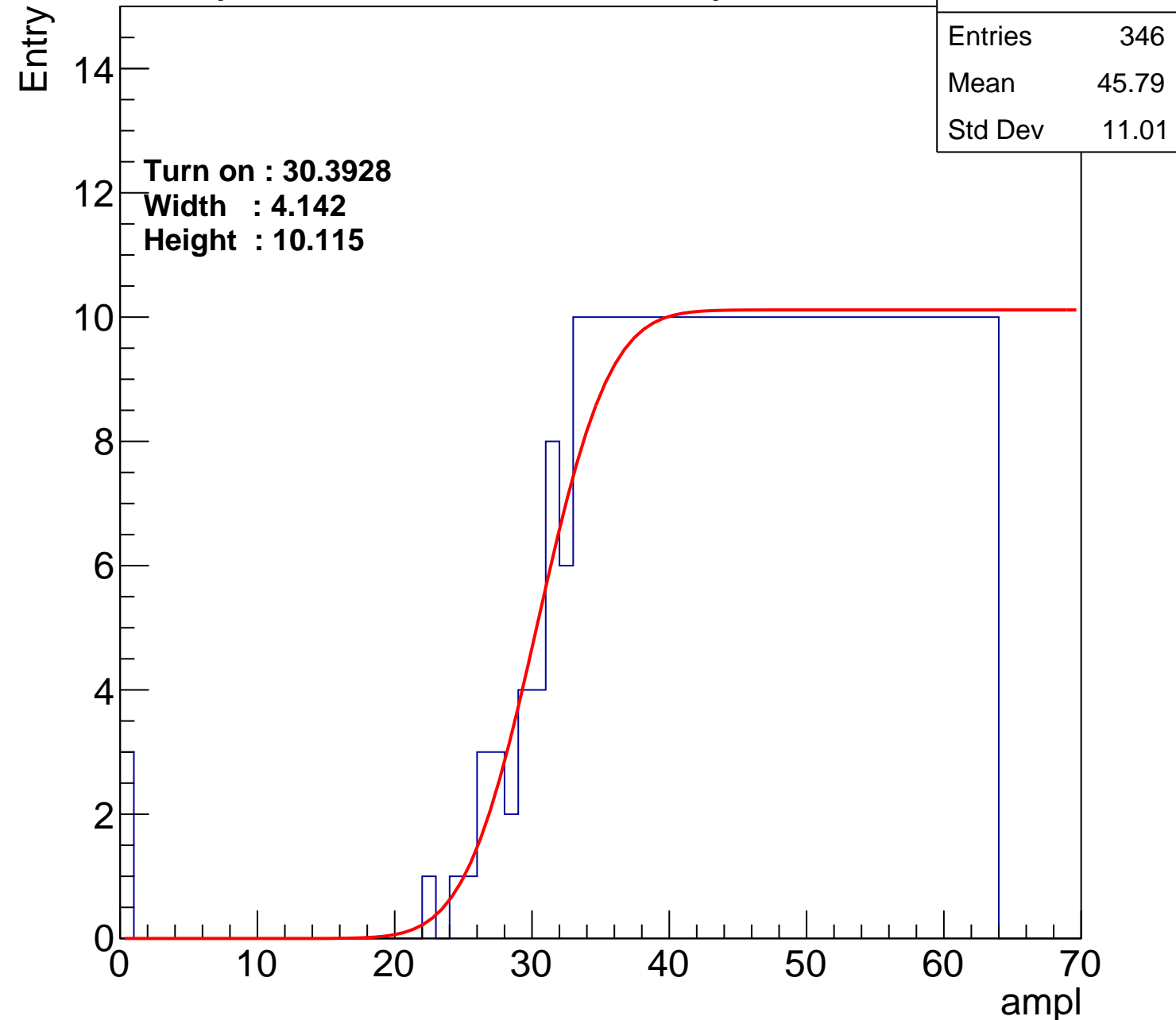
Width : 4.142

Height : 10.115

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch125

calib_packv5_042523_0143.root, FC#13, port D2

Entries	364
Mean	45.08
Std Dev	10.97

Turn on : 27.6197

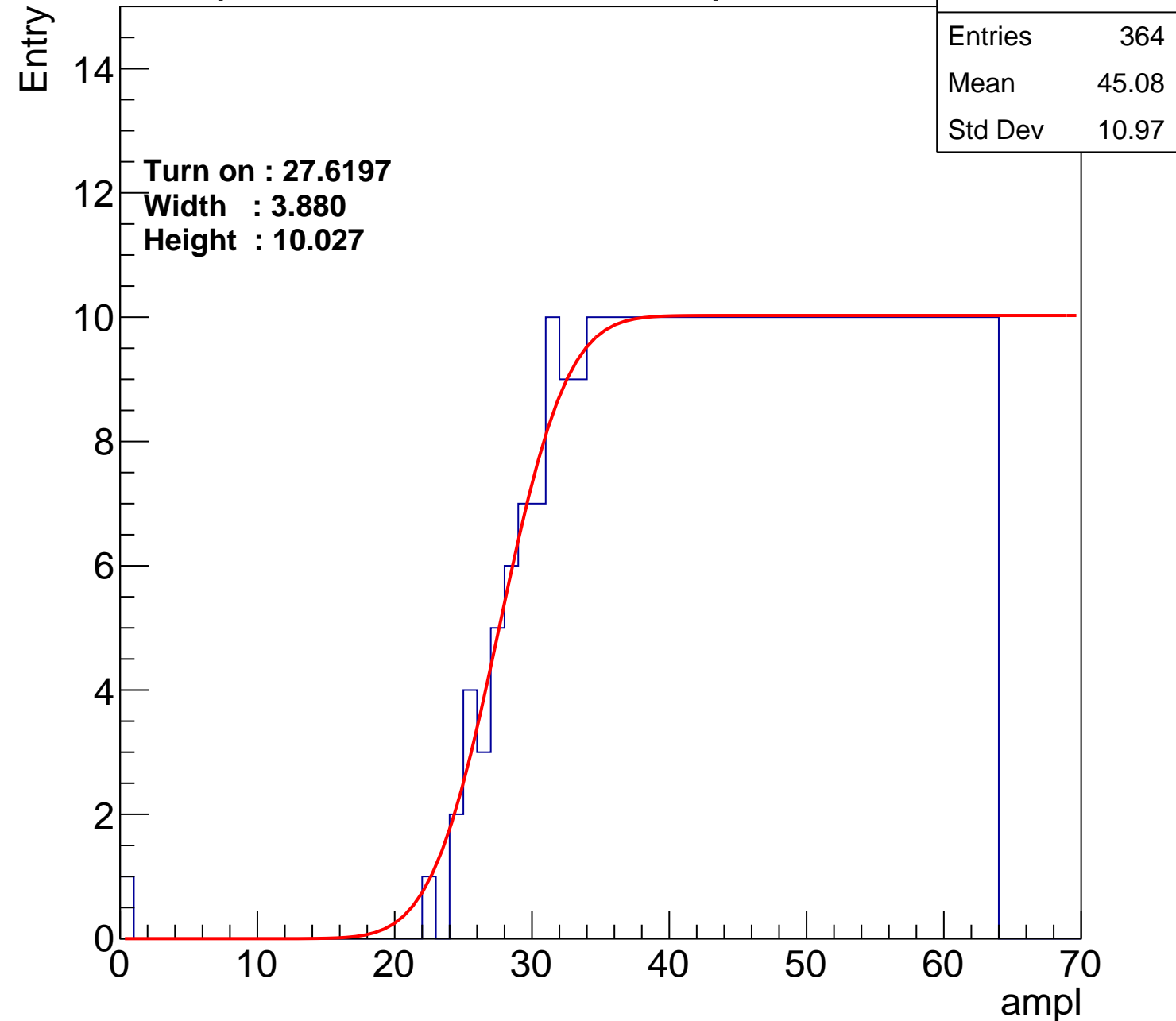
Width : 3.880

Height : 10.027

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch126

calib_packv5_042523_0143.root, FC#13, port D2

Entries	388
Mean	43.84
Std Dev	11.78

Turn on : 25.7918

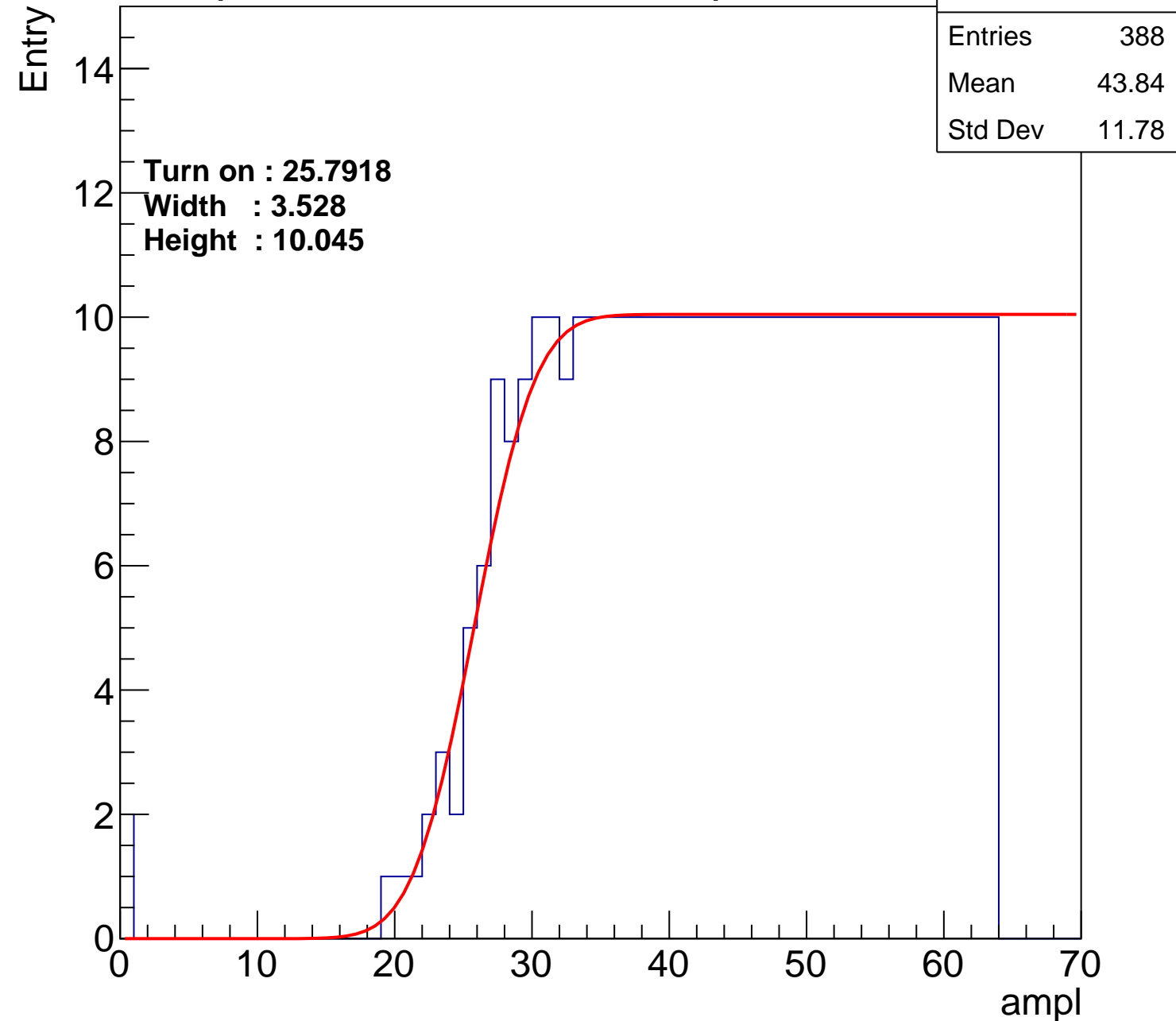
Width : 3.528

Height : 10.045

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch127

calib_packv5_042523_0143.root, FC#13, port D2

Entries	370
Mean	44.74
Std Dev	11.29

Turn on : 27.4453

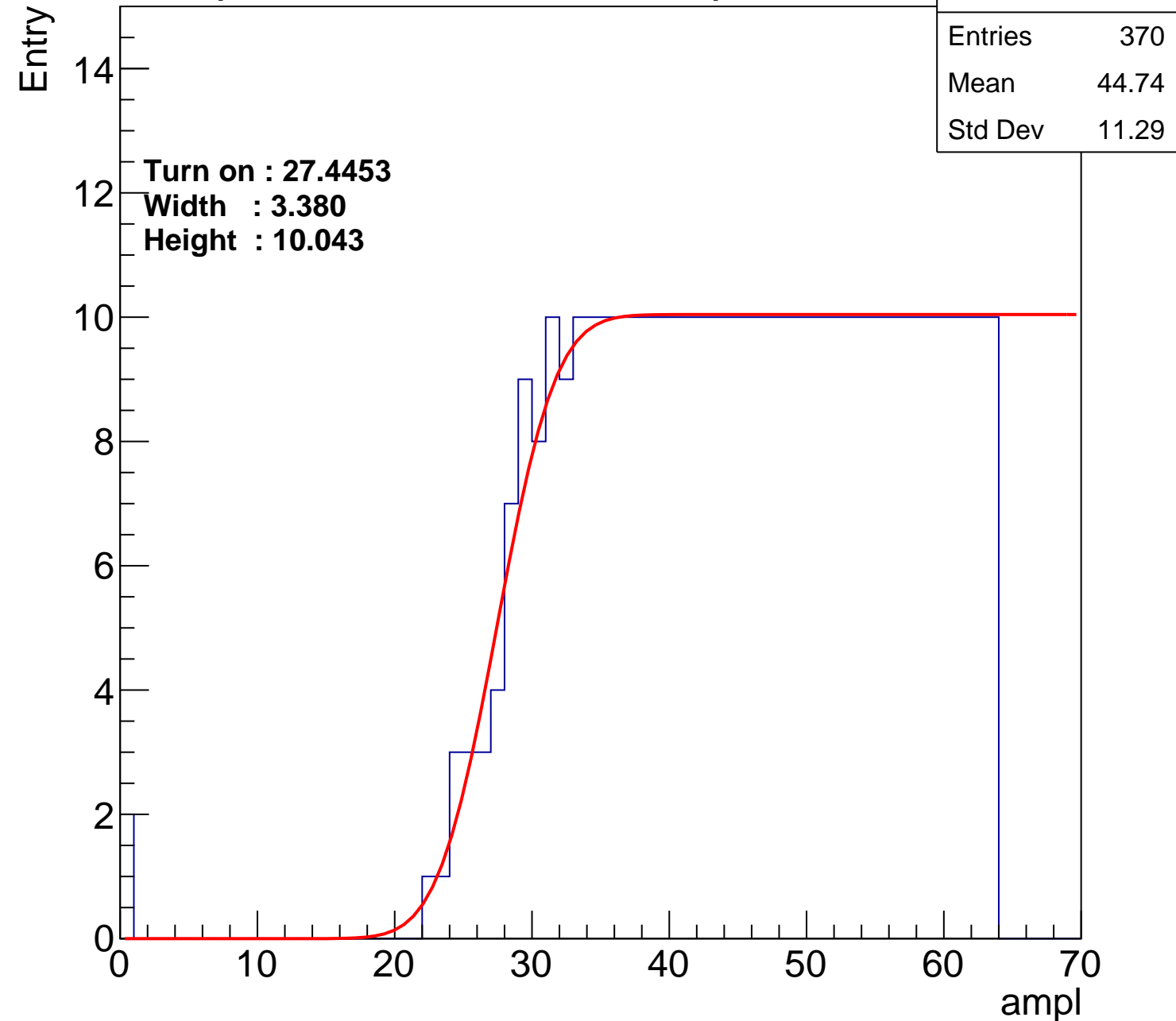
Width : 3.380

Height : 10.043

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U2-ch127

calib_packv5_042523_0143.root, FC#13, port D2

Entries	370
Mean	44.74
Std Dev	11.29

Turn on : 27.4453

Width : 3.380

Height : 10.043

Entry

14
12
10
8
6
4
2
0

ampl

