

B1L102S, U3-ch0

calib_packv5_042523_0143.root, FC#11, port A2

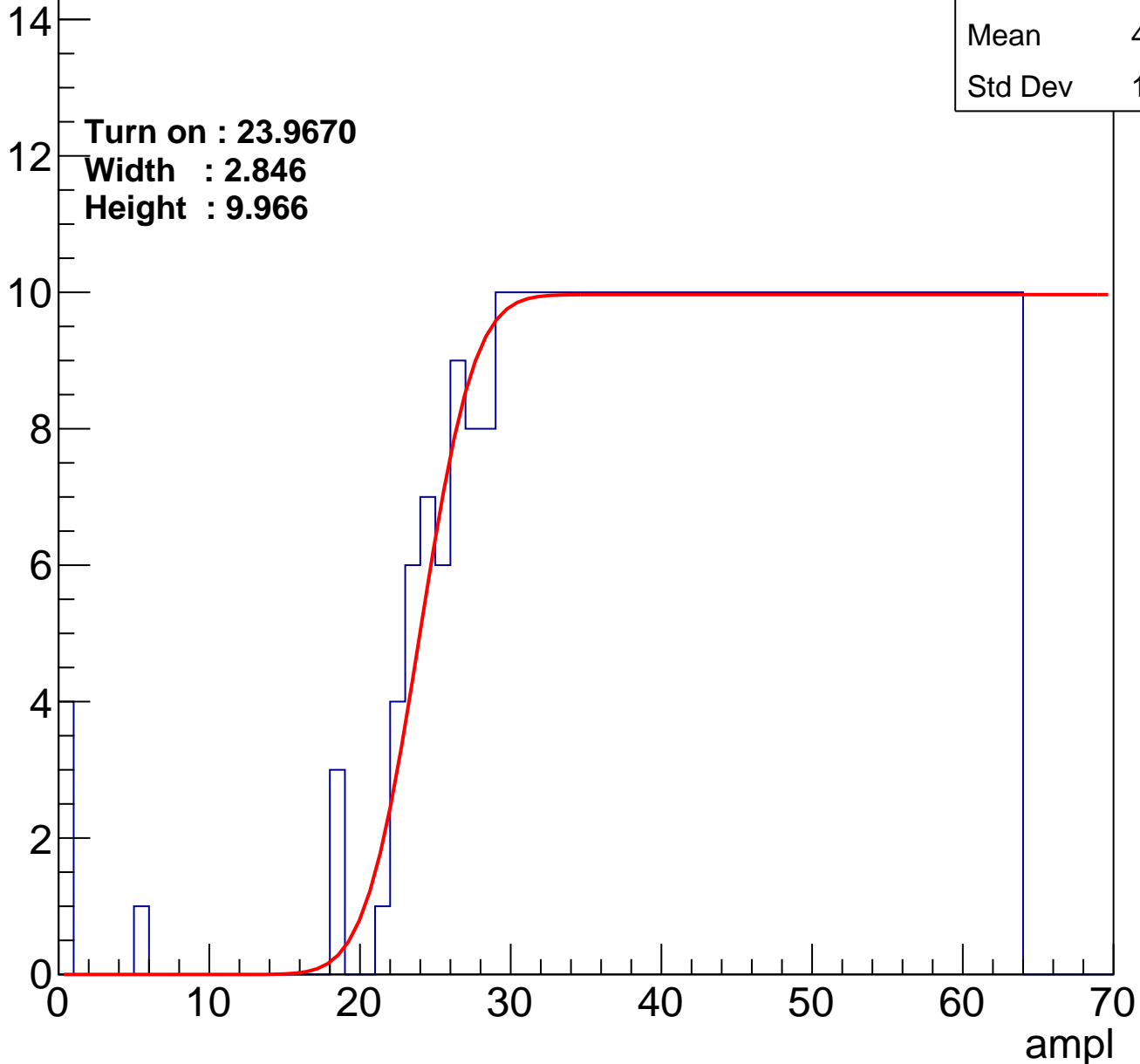
Entries	407
Mean	42.75
Std Dev	12.65

Turn on : 23.9670

Width : 2.846

Height : 9.966

Entry



B1L102S, U3-ch1

calib_packv5_042523_0143.root, FC#11, port A2

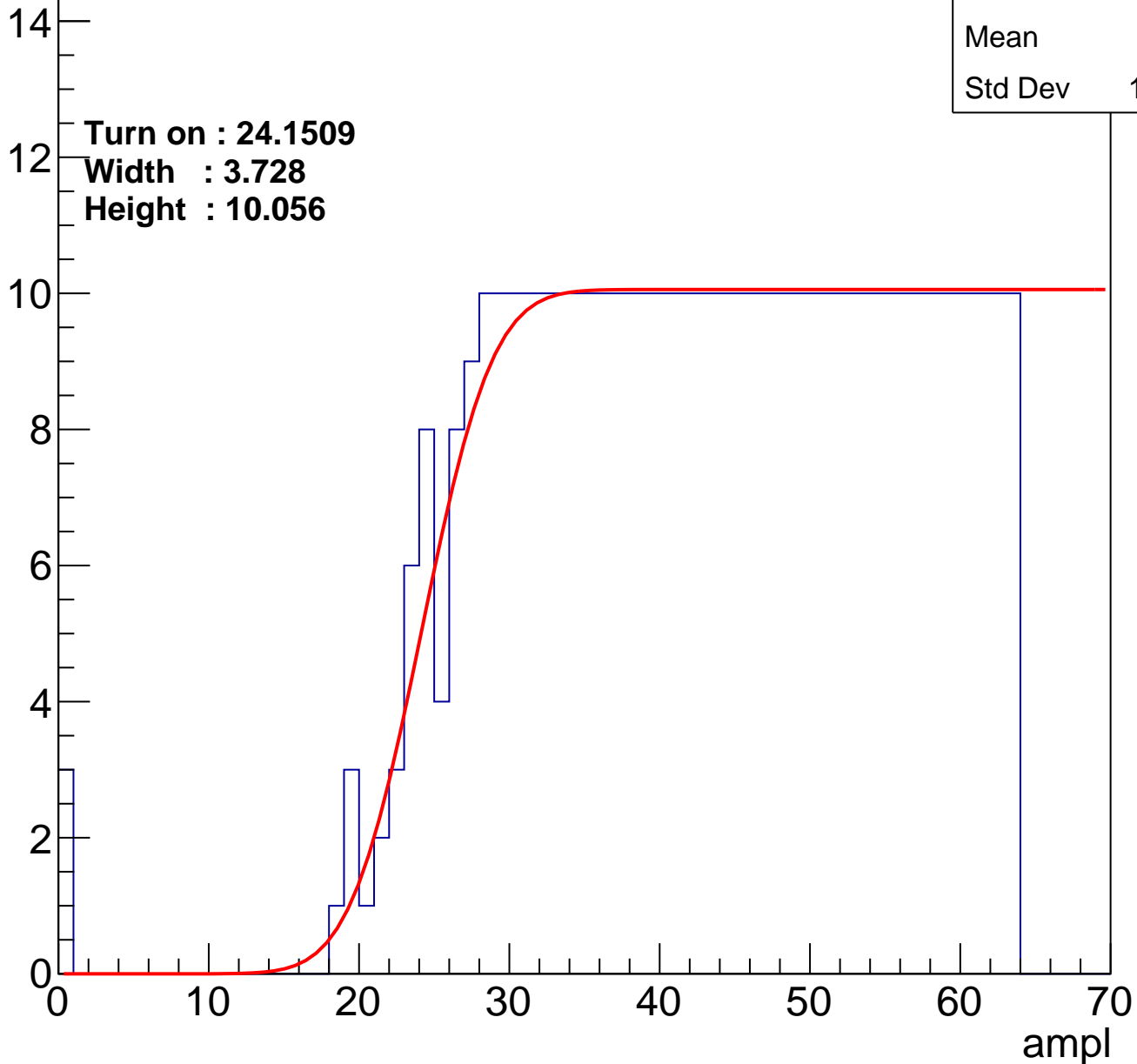
Entries	408
Mean	42.8
Std Dev	12.43

Turn on : 24.1509

Width : 3.728

Height : 10.056

Entry



B1L102S, U3-ch2

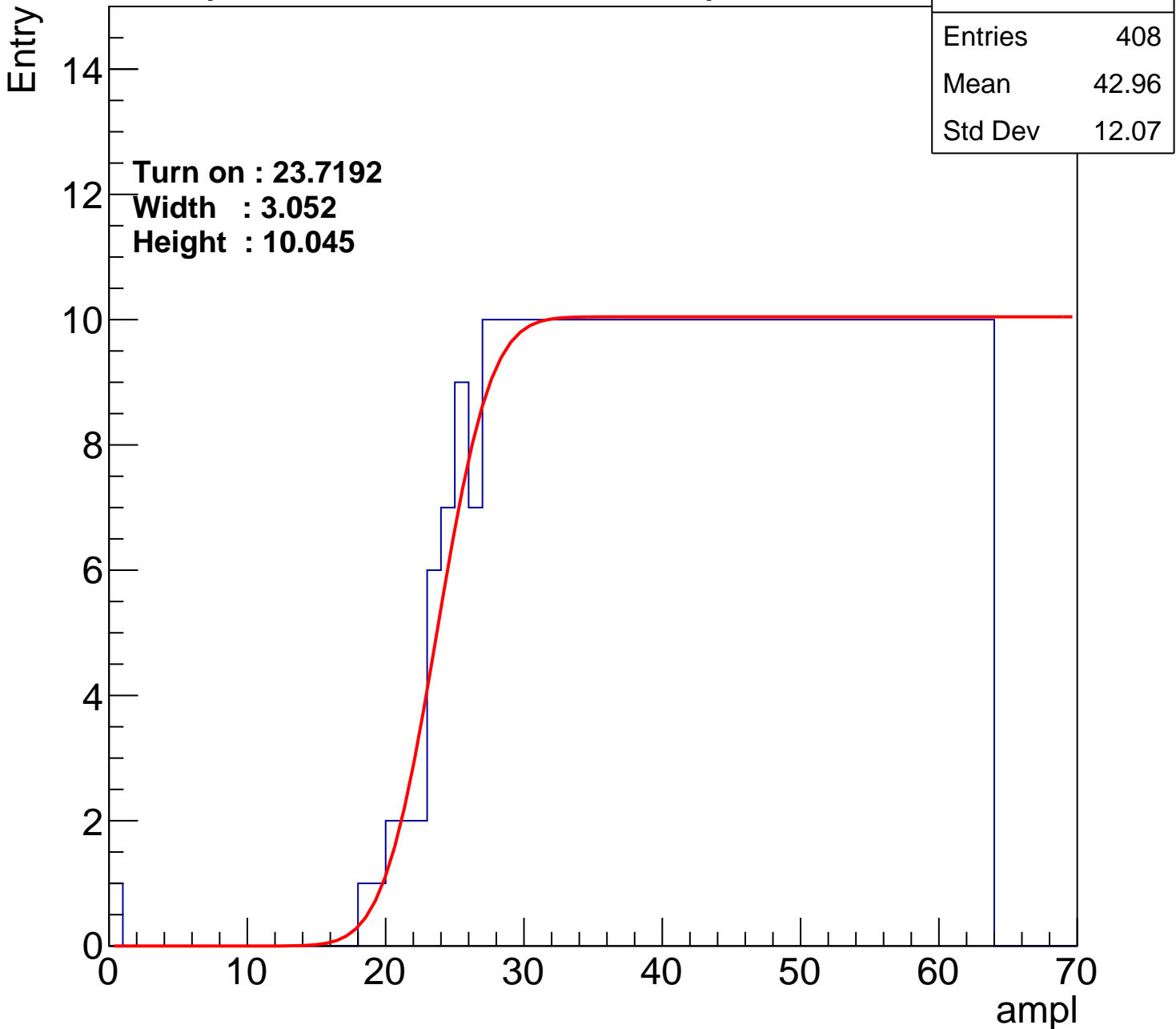
calib_packv5_042523_0143.root, FC#11, port A2

Entries	408
Mean	42.96
Std Dev	12.07

Turn on : 23.7192

Width : 3.052

Height : 10.045



B1L102S, U3-ch3

calib_packv5_042523_0143.root, FC#11, port A2

Entries	378
Mean	44.3
Std Dev	11.56

Turn on : 26.9666

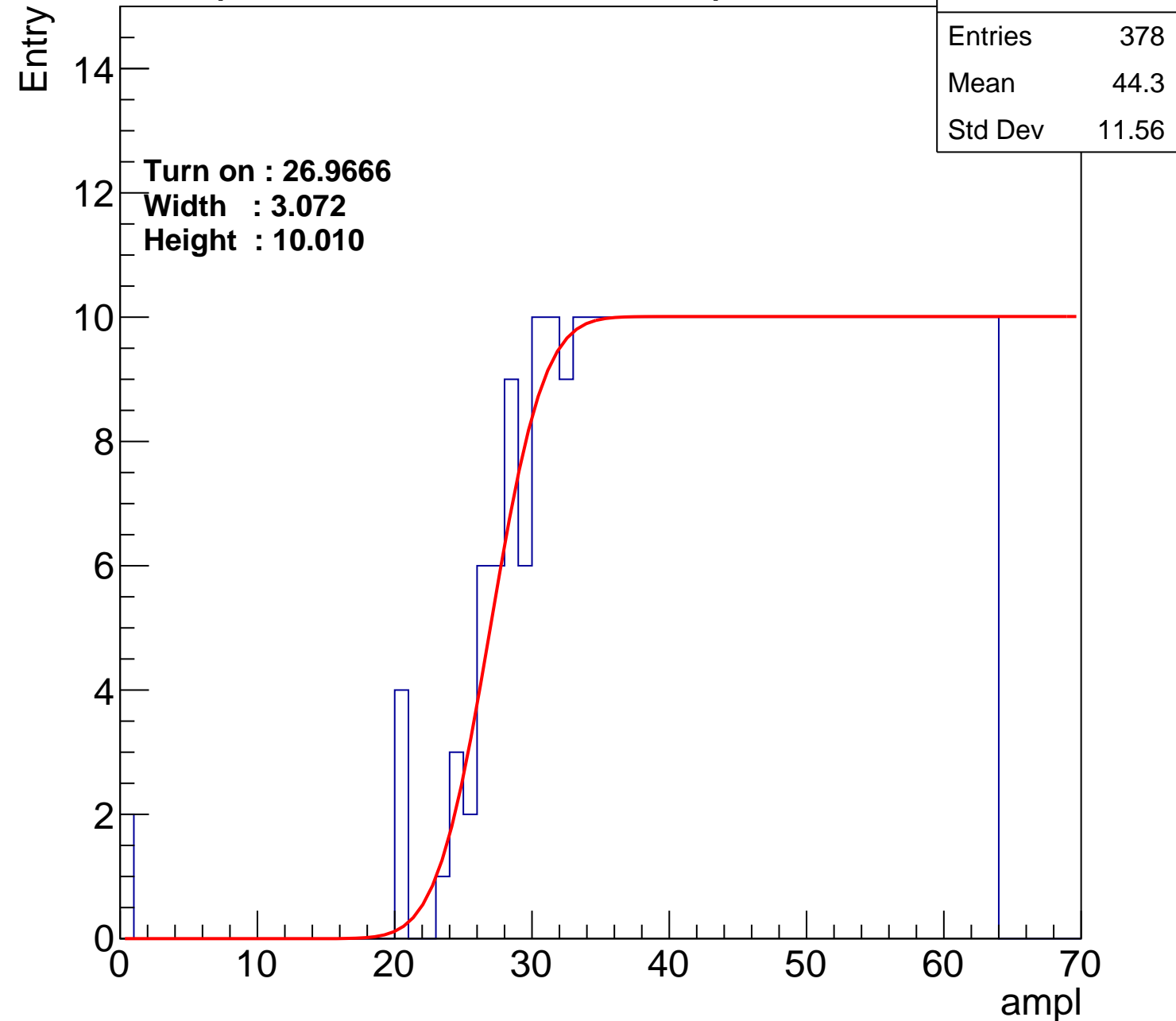
Width : 3.072

Height : 10.010

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch4

calib_packv5_042523_0143.root, FC#11, port A2

Entries	381
Mean	43.99
Std Dev	12.03

Turn on : 26.7759

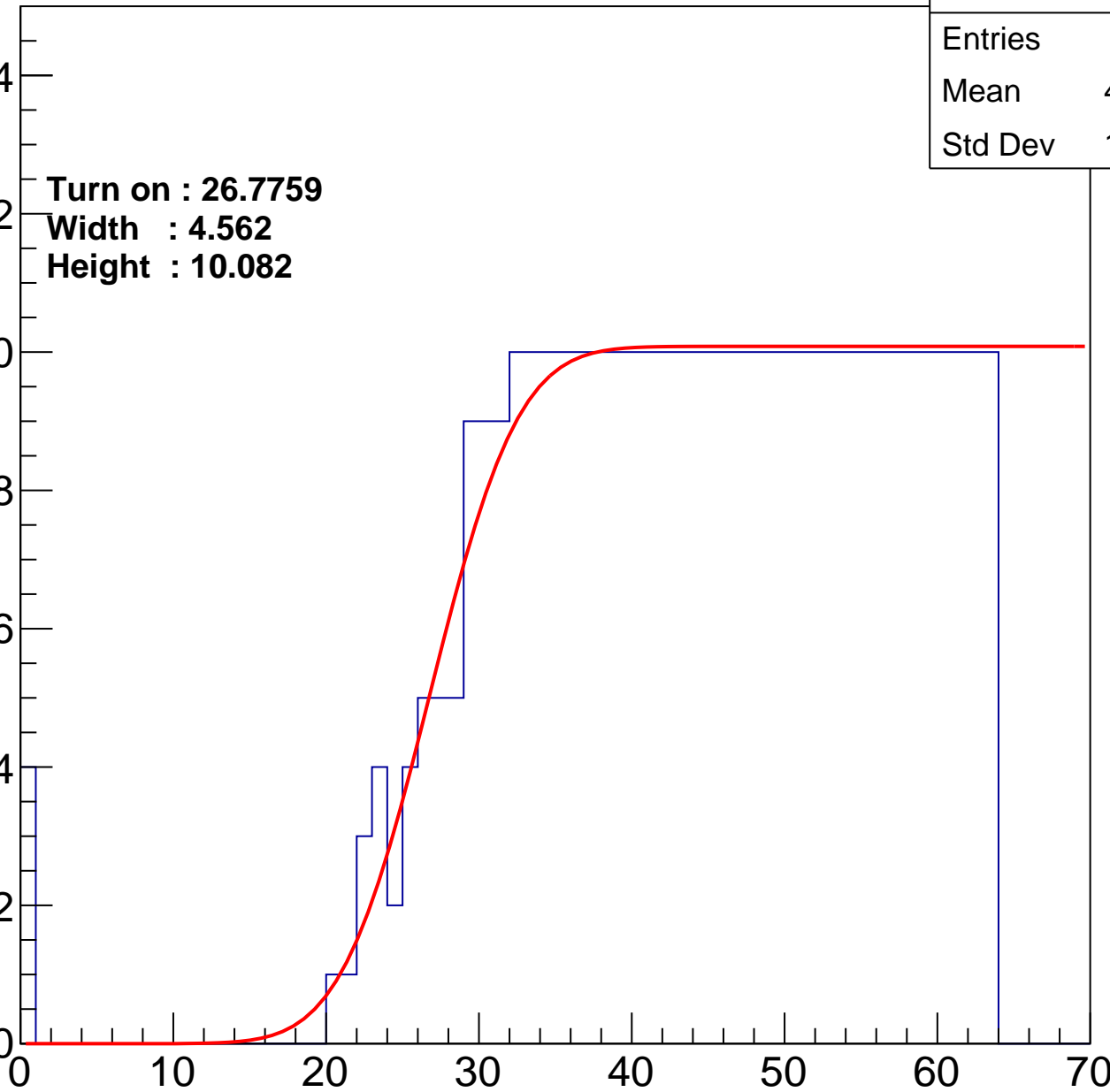
Width : 4.562

Height : 10.082

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch5

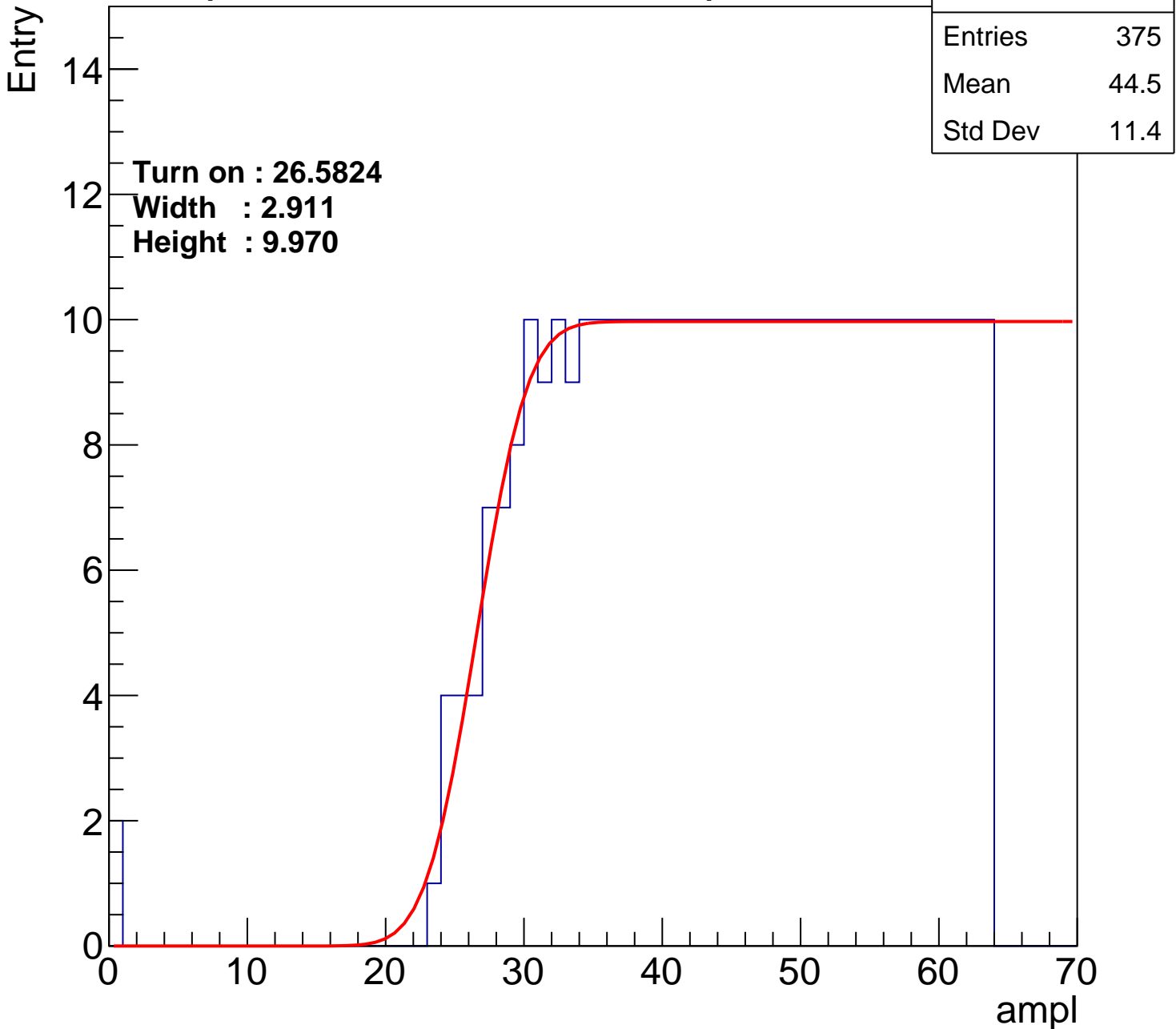
calib_packv5_042523_0143.root, FC#11, port A2

Entries	375
Mean	44.5
Std Dev	11.4

Turn on : 26.5824

Width : 2.911

Height : 9.970



B1L102S, U3-ch6

calib_packv5_042523_0143.root, FC#11, port A2

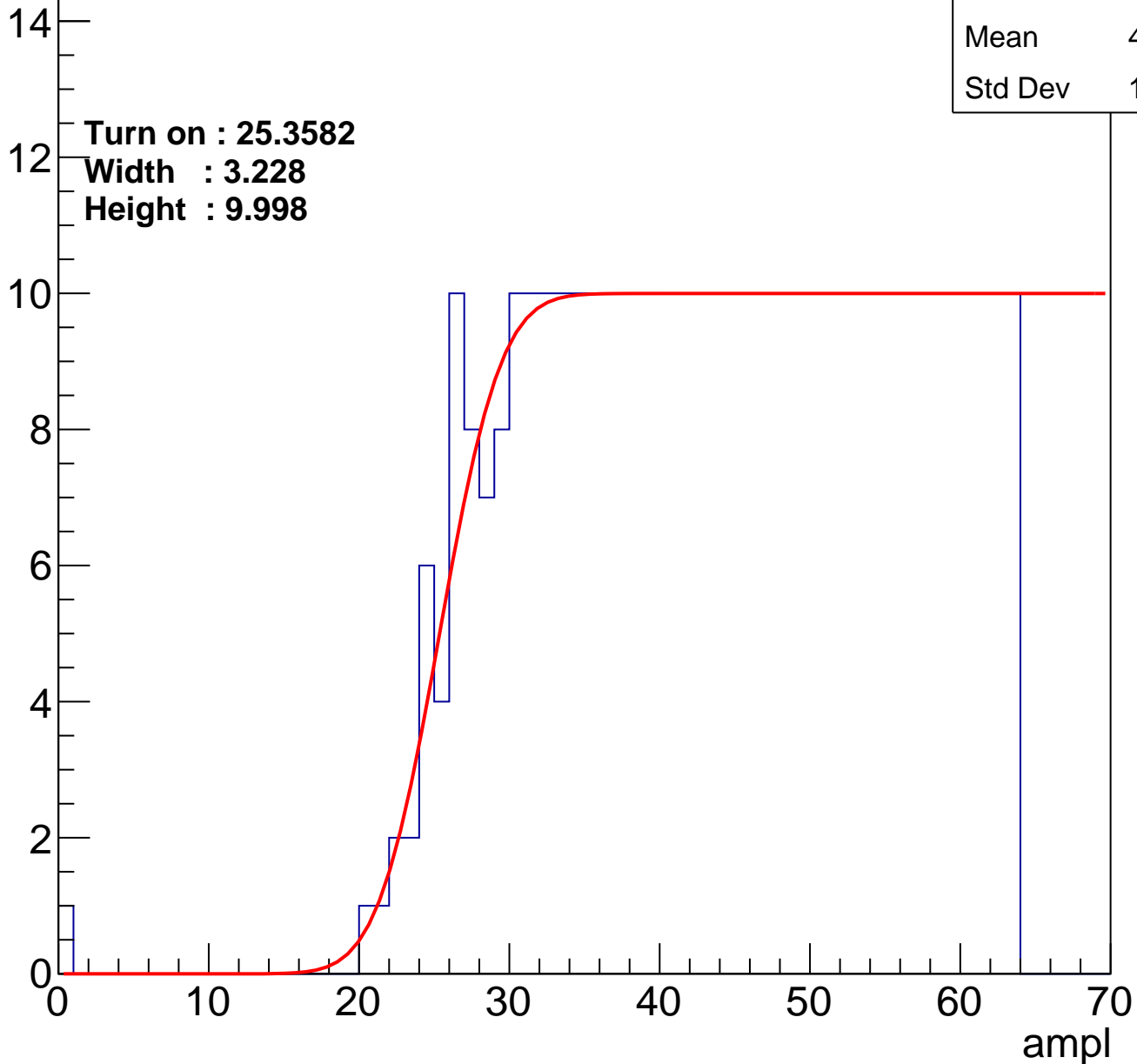
Entries	390
Mean	43.82
Std Dev	11.63

Turn on : 25.3582

Width : 3.228

Height : 9.998

Entry



B1L102S, U3-ch7

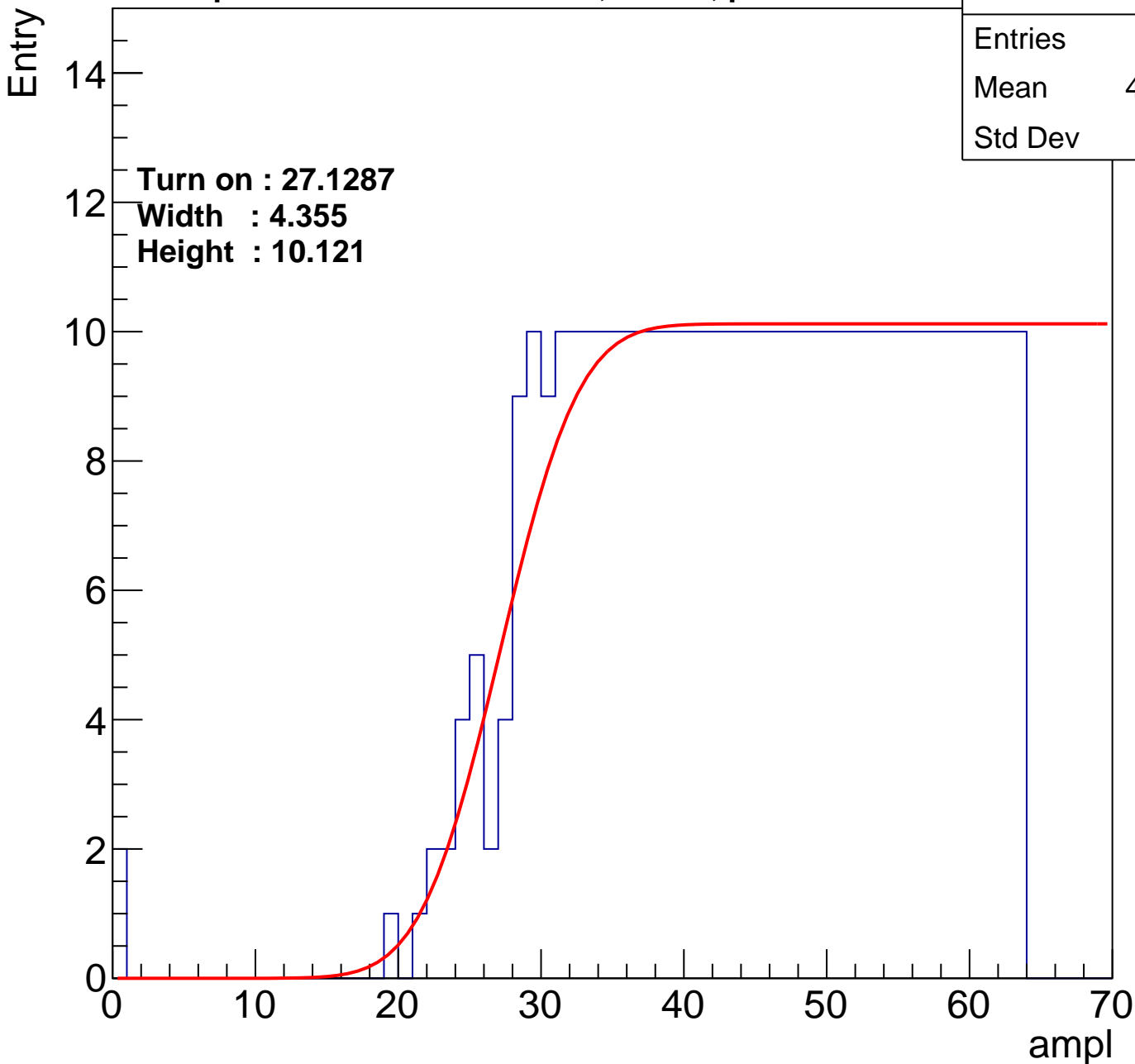
calib_packv5_042523_0143.root, FC#11, port A2

Entries	381
Mean	44.18
Std Dev	11.6

Turn on : 27.1287

Width : 4.355

Height : 10.121



B1L102S, U3-ch8

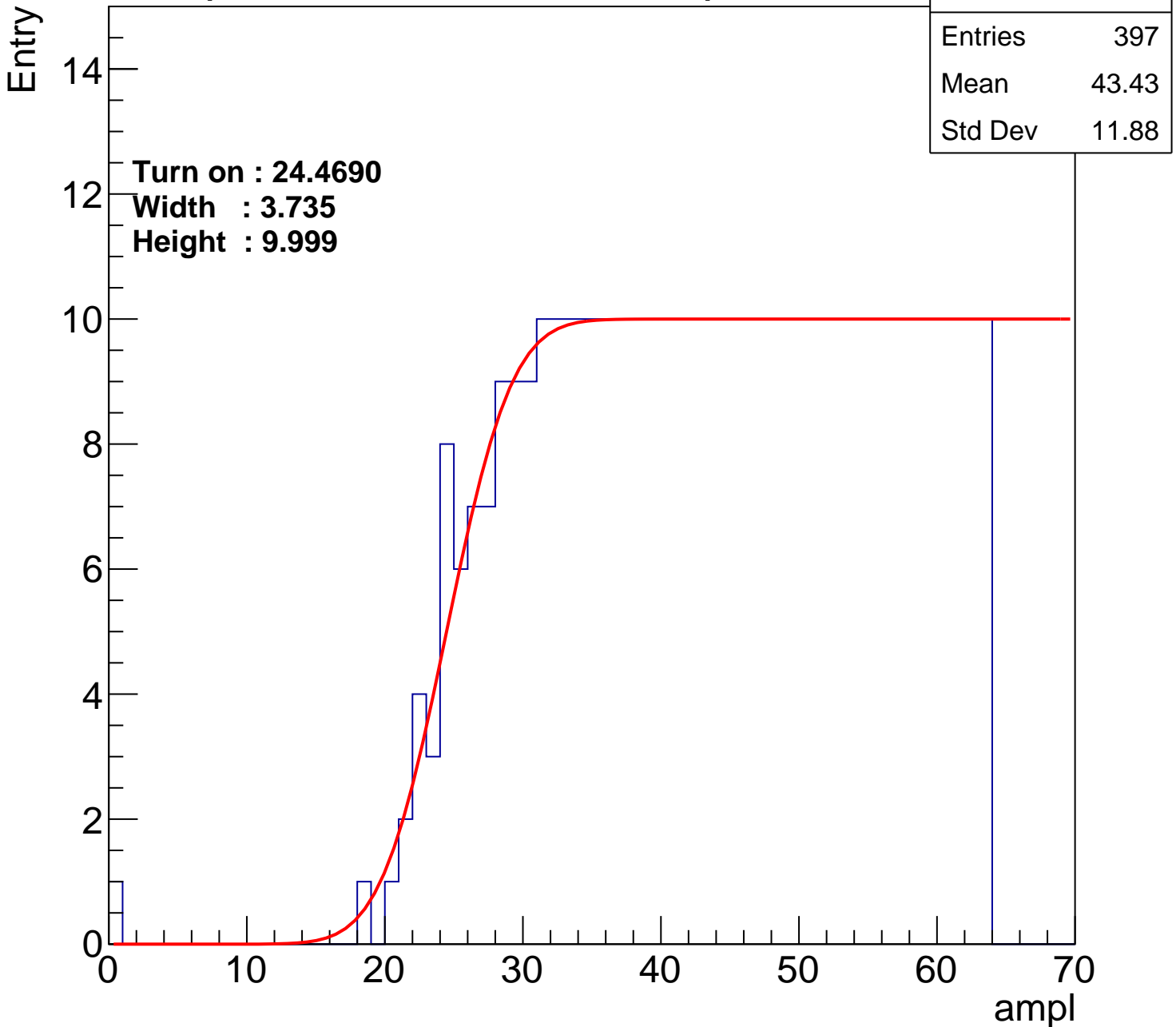
calib_packv5_042523_0143.root, FC#11, port A2

Entries	397
Mean	43.43
Std Dev	11.88

Turn on : 24.4690

Width : 3.735

Height : 9.999



B1L102S, U3-ch9

calib_packv5_042523_0143.root, FC#11, port A2

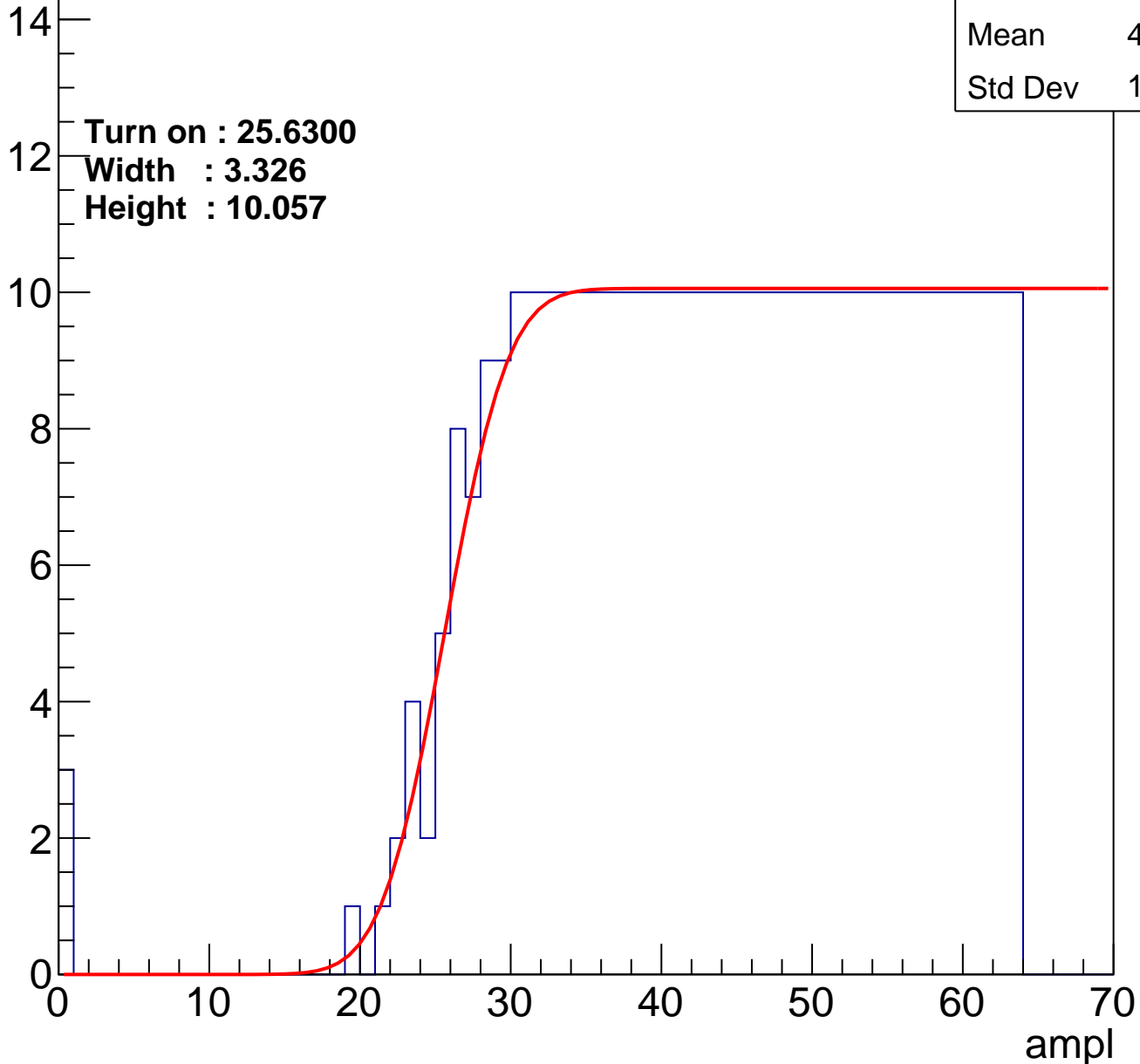
Entries	391
Mean	43.65
Std Dev	11.97

Turn on : 25.6300

Width : 3.326

Height : 10.057

Entry



B1L102S, U3-ch10

calib_packv5_042523_0143.root, FC#11, port A2

Entries	389
Mean	43.84
Std Dev	11.65

Turn on : 25.4080

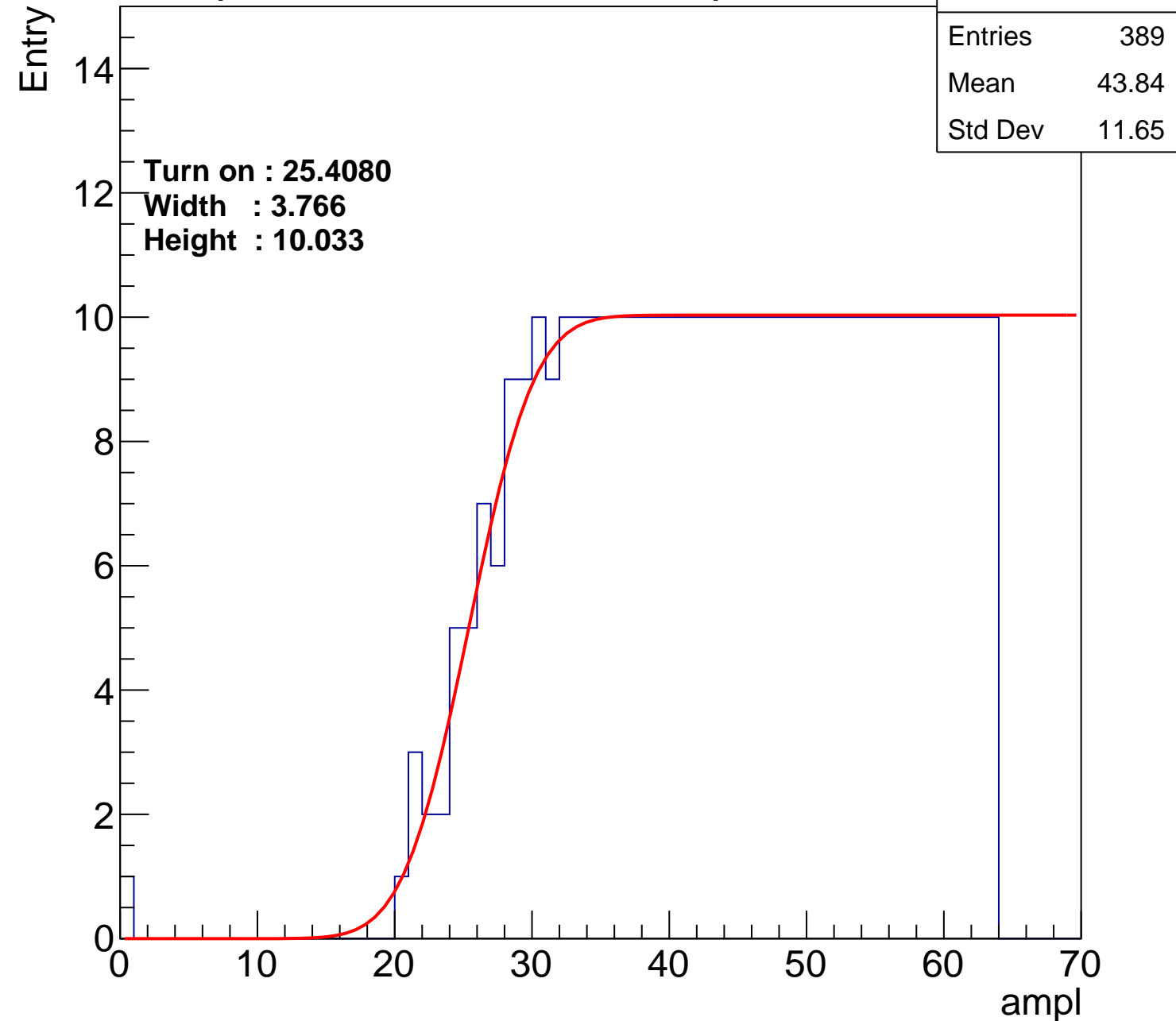
Width : 3.766

Height : 10.033

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch11

calib_packv5_042523_0143.root, FC#11, port A2

Entries	403
Mean	43.17
Std Dev	11.99

Turn on : 24.0373

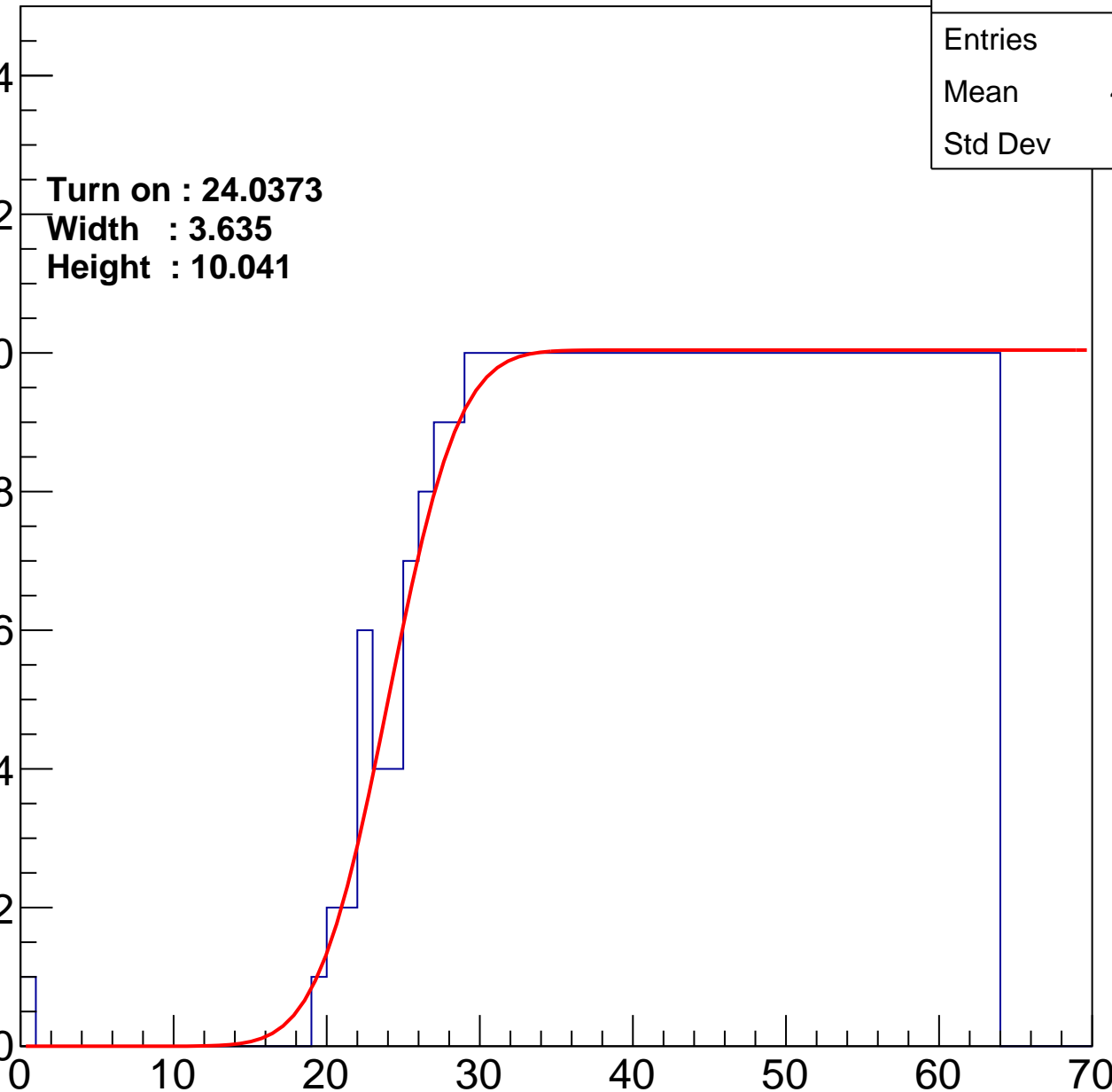
Width : 3.635

Height : 10.041

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch12

calib_packv5_042523_0143.root, FC#11, port A2

Entries	393
Mean	43.77
Std Dev	11.66

Turn on : 25.3858

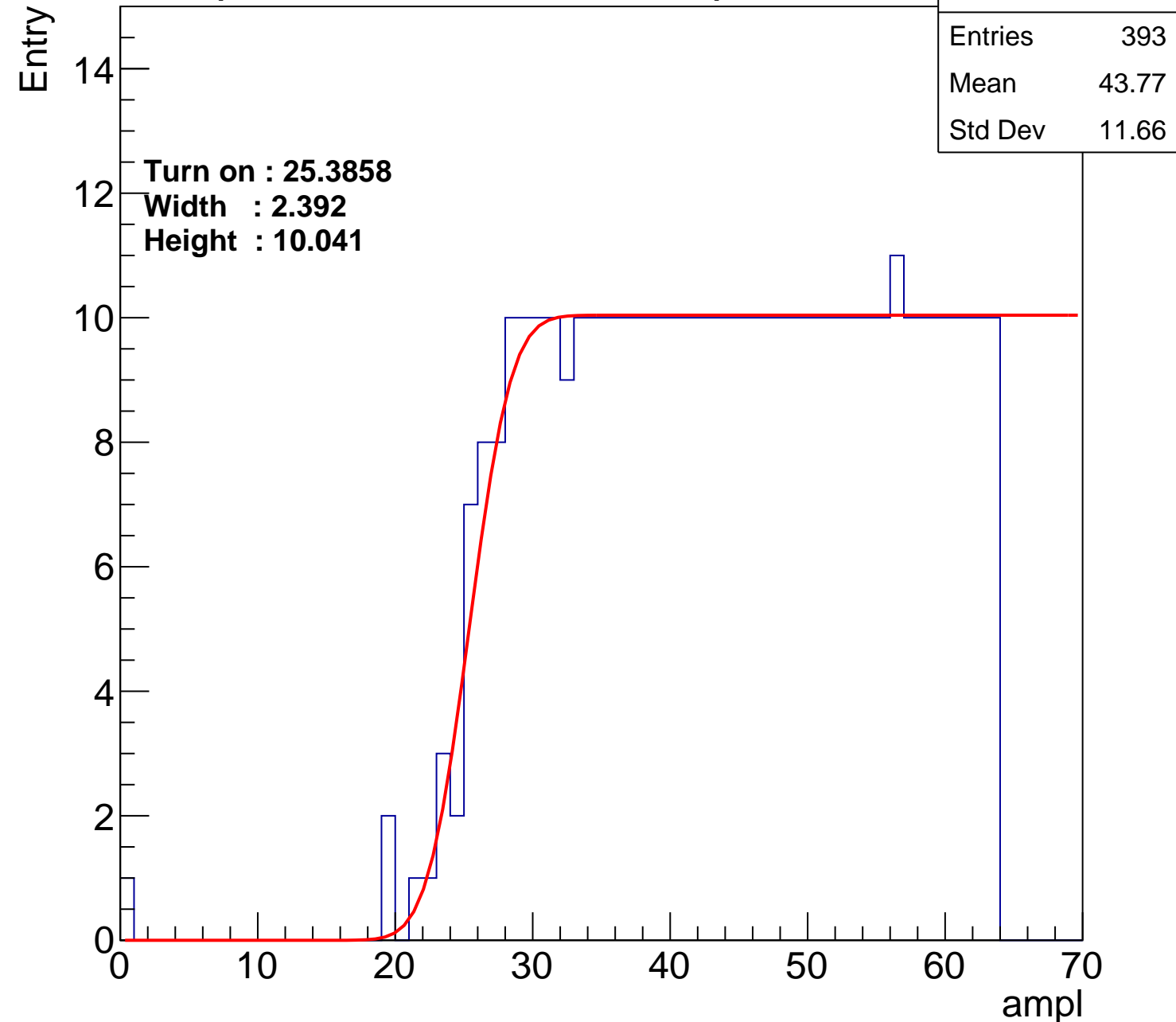
Width : 2.392

Height : 10.041

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch13

calib_packv5_042523_0143.root, FC#11, port A2

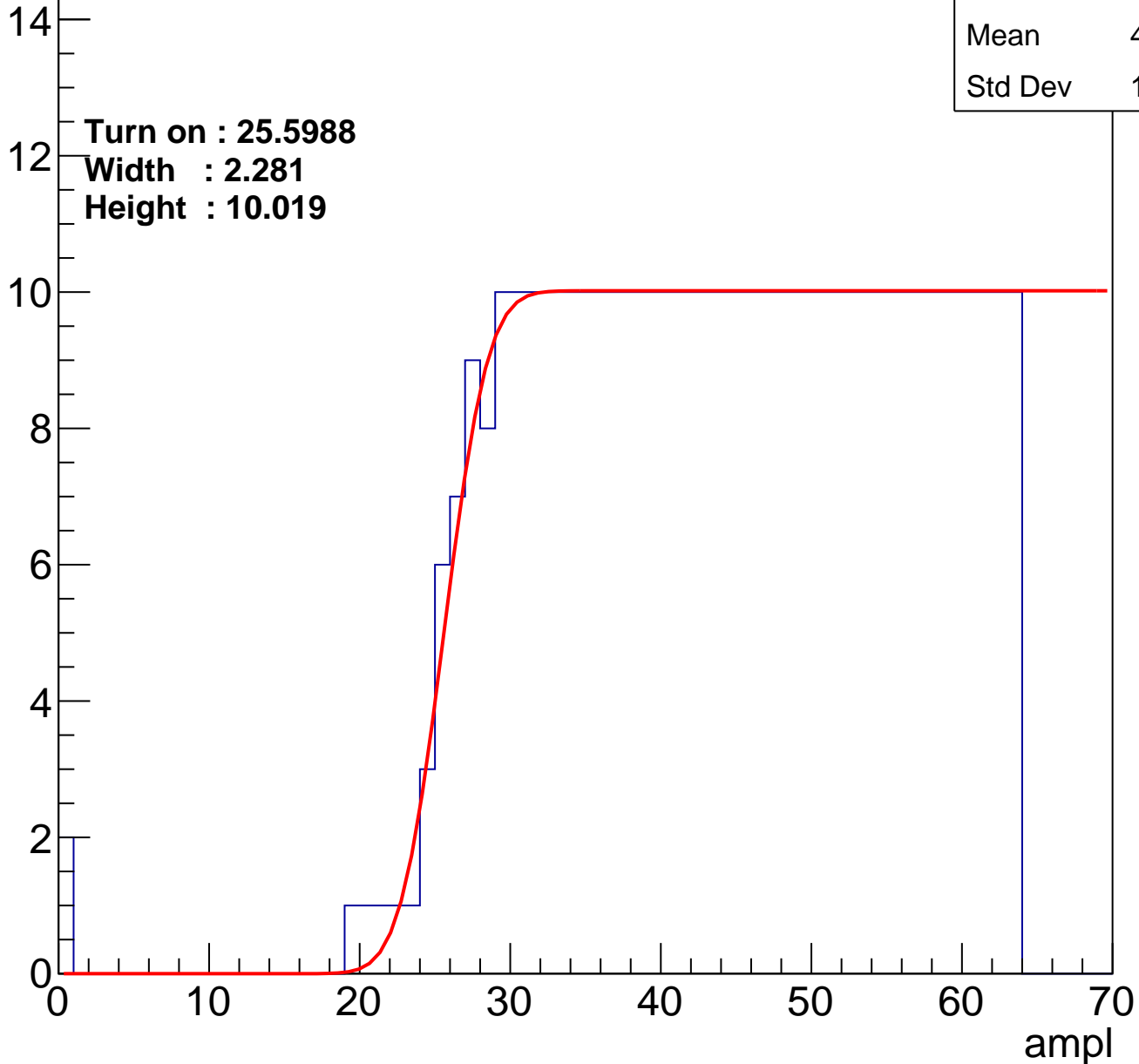
Entries	390
Mean	43.78
Std Dev	11.76

Turn on : 25.5988

Width : 2.281

Height : 10.019

Entry



B1L102S, U3-ch14

calib_packv5_042523_0143.root, FC#11, port A2

Entries	378
Mean	44.35
Std Dev	11.48

Turn on : 26.7354

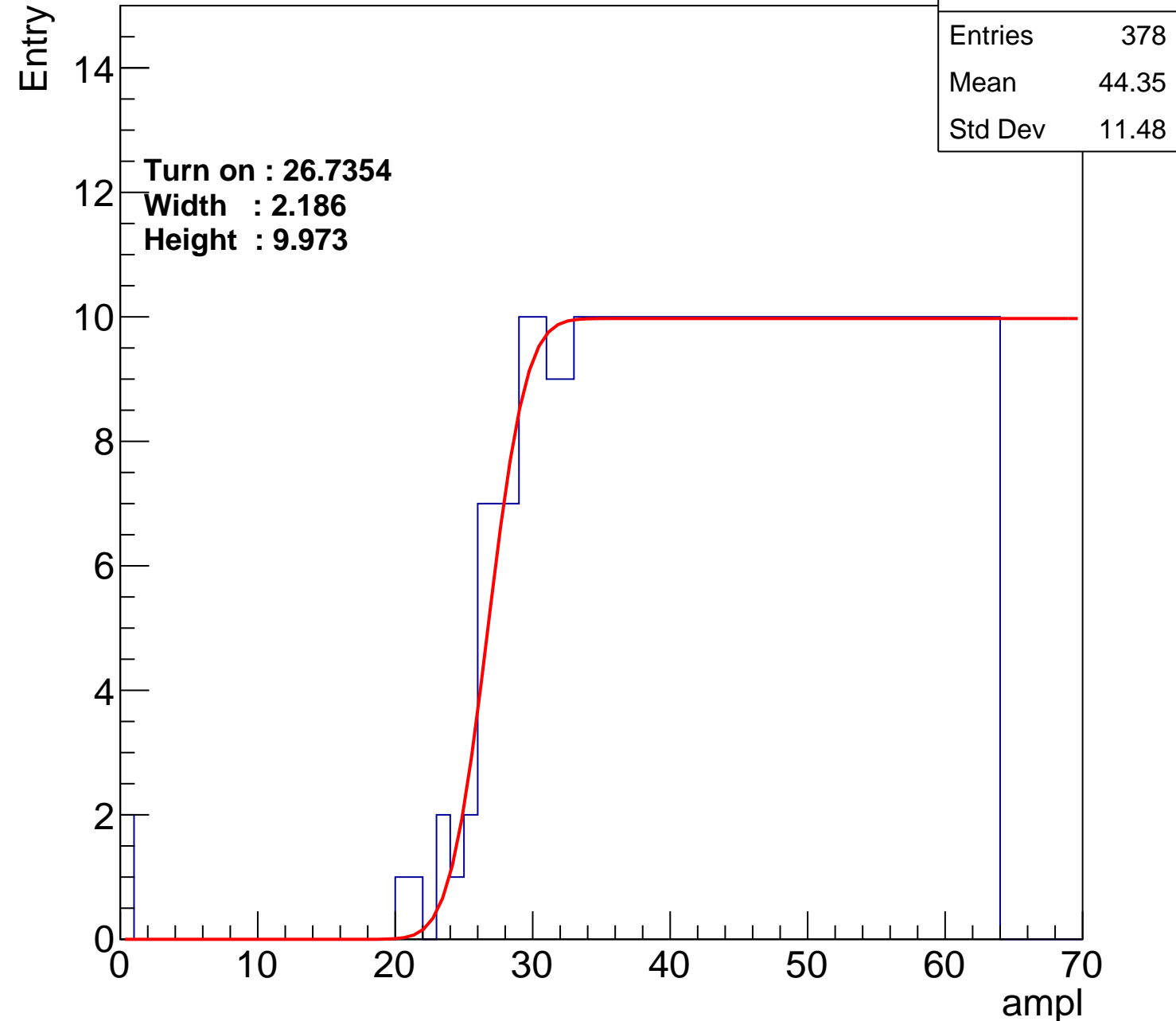
Width : 2.186

Height : 9.973

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch15

calib_packv5_042523_0143.root, FC#11, port A2

Entries	402
Mean	43.07
Std Dev	12.38

Turn on : 24.3849

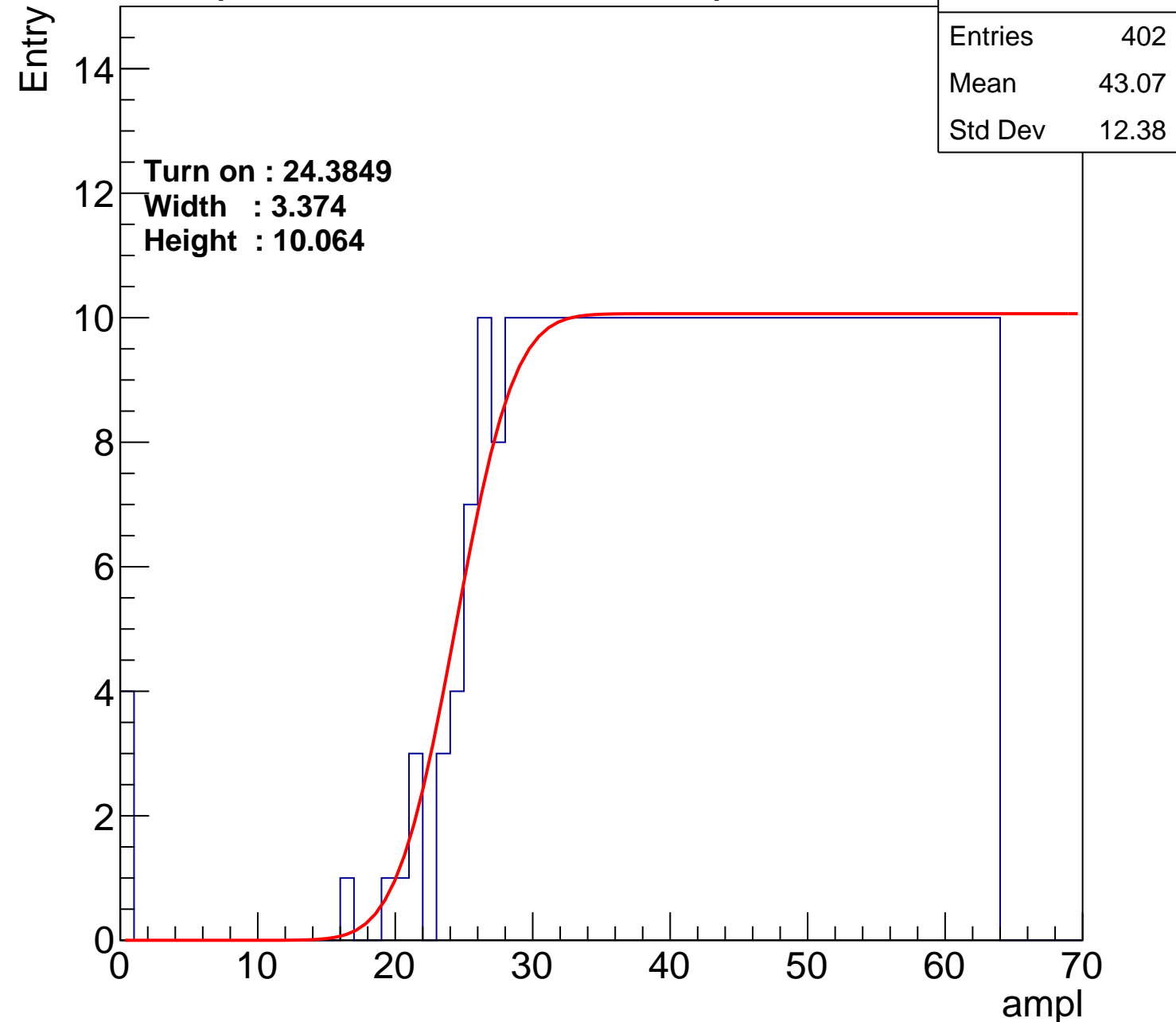
Width : 3.374

Height : 10.064

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch16

calib_packv5_042523_0143.root, FC#11, port A2

Entries	403
Mean	42.98
Std Dev	12.46

Turn on : 24.5233

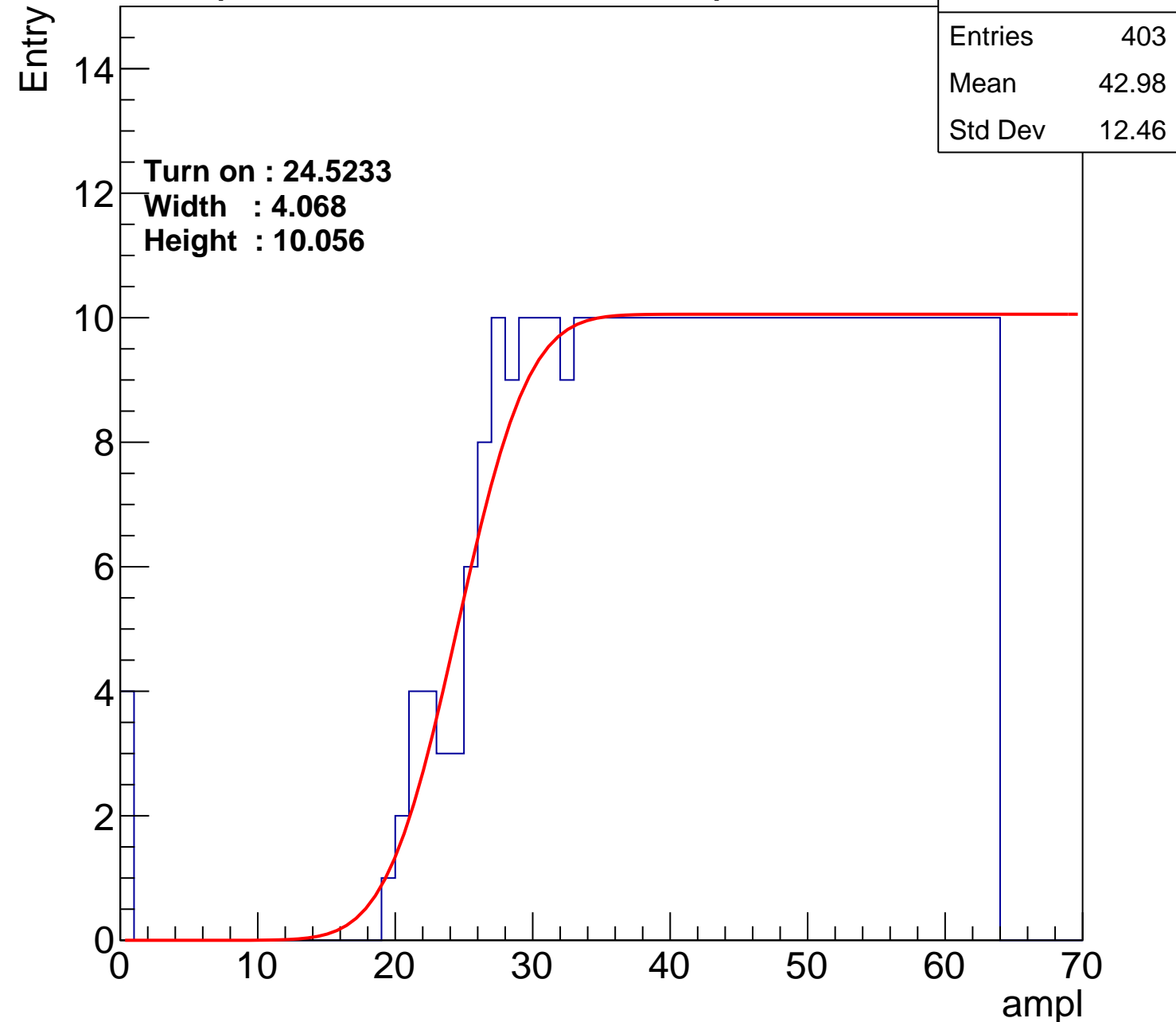
Width : 4.068

Height : 10.056

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch17

calib_packv5_042523_0143.root, FC#11, port A2

Entries	390
Mean	43.74
Std Dev	11.89

Turn on : 26.2737

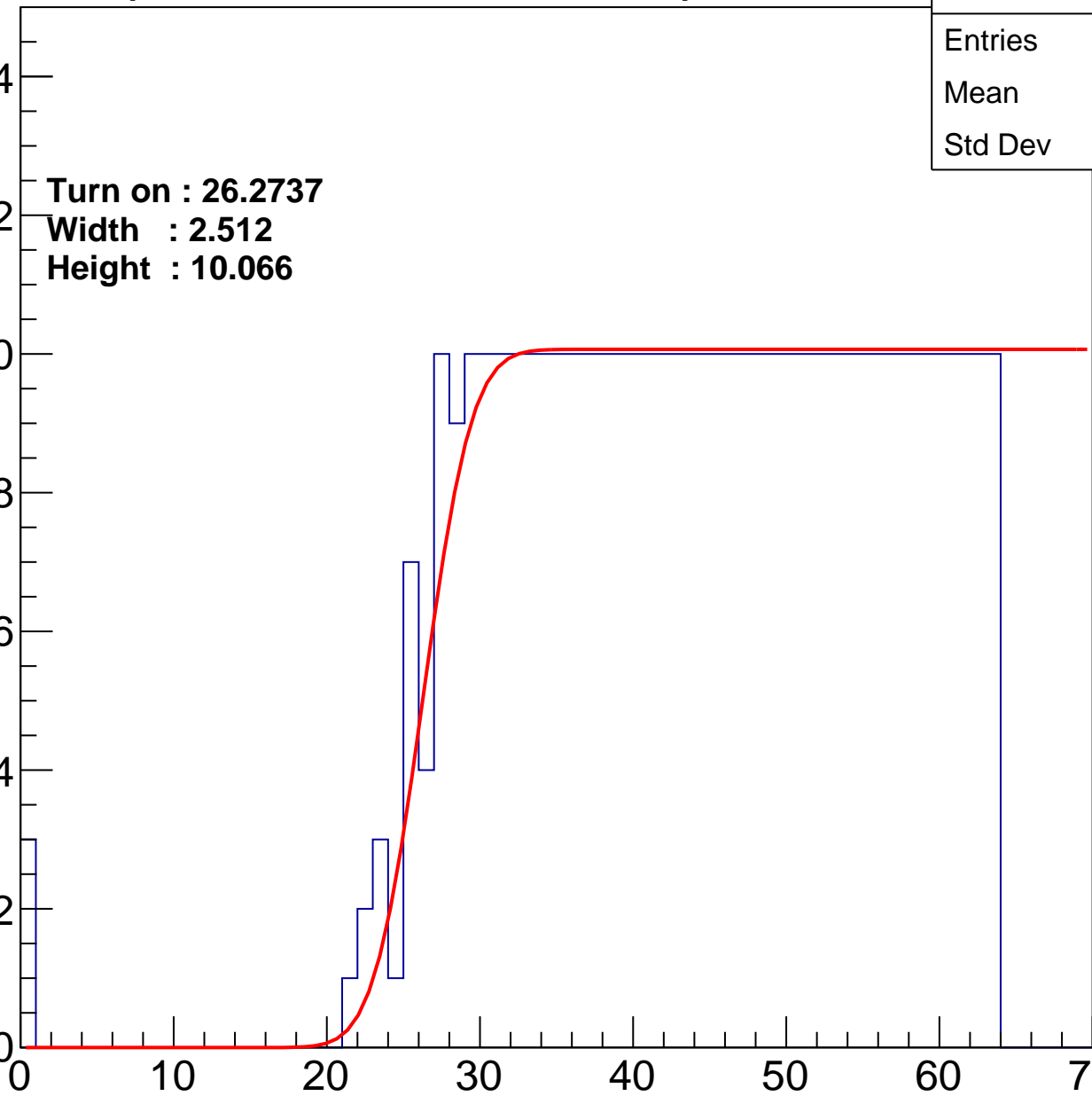
Width : 2.512

Height : 10.066

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch18

calib_packv5_042523_0143.root, FC#11, port A2

Entries	391
Mean	43.65
Std Dev	11.98

Turn on : 25.5793

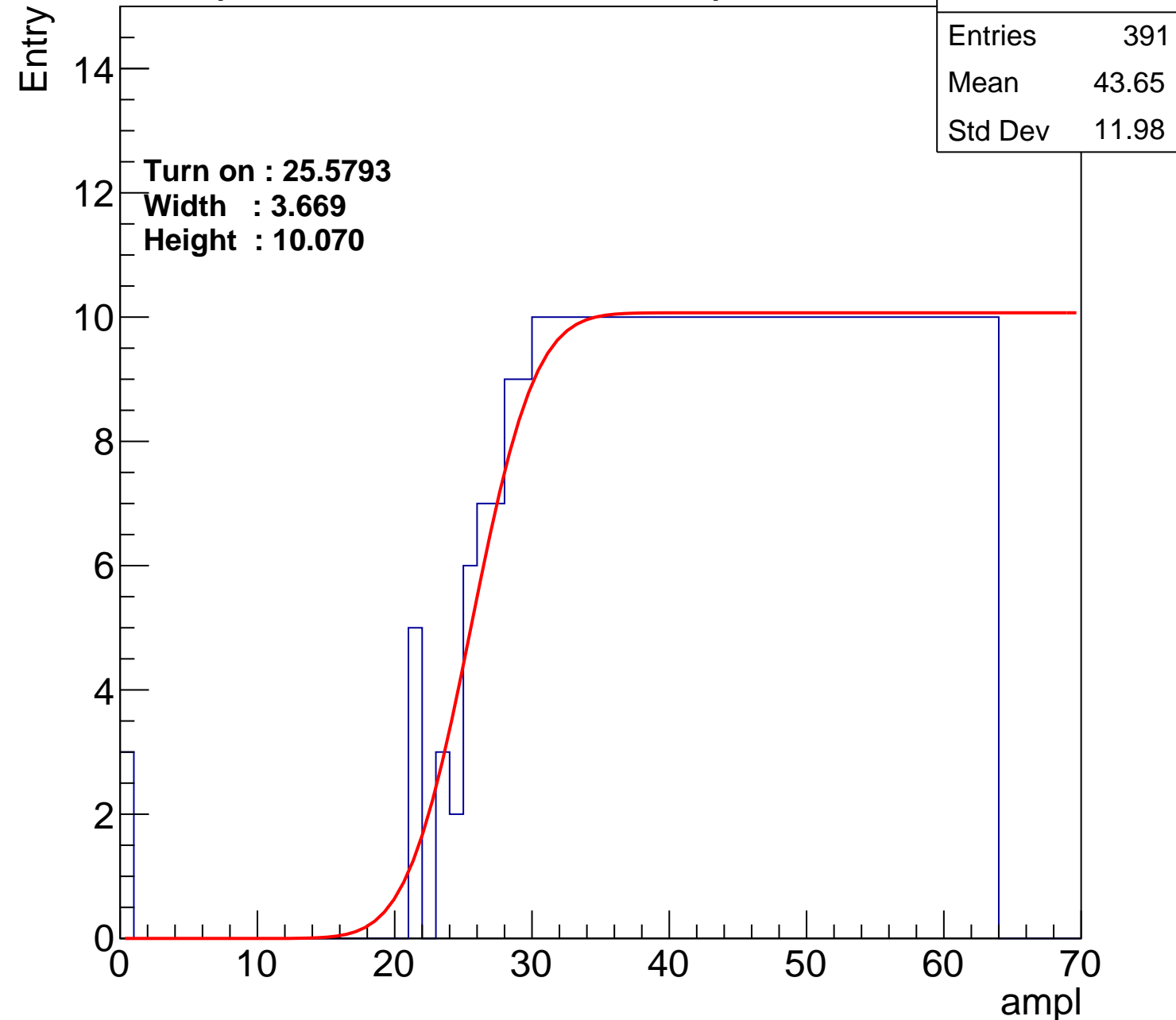
Width : 3.669

Height : 10.070

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch19

calib_packv5_042523_0143.root, FC#11, port A2

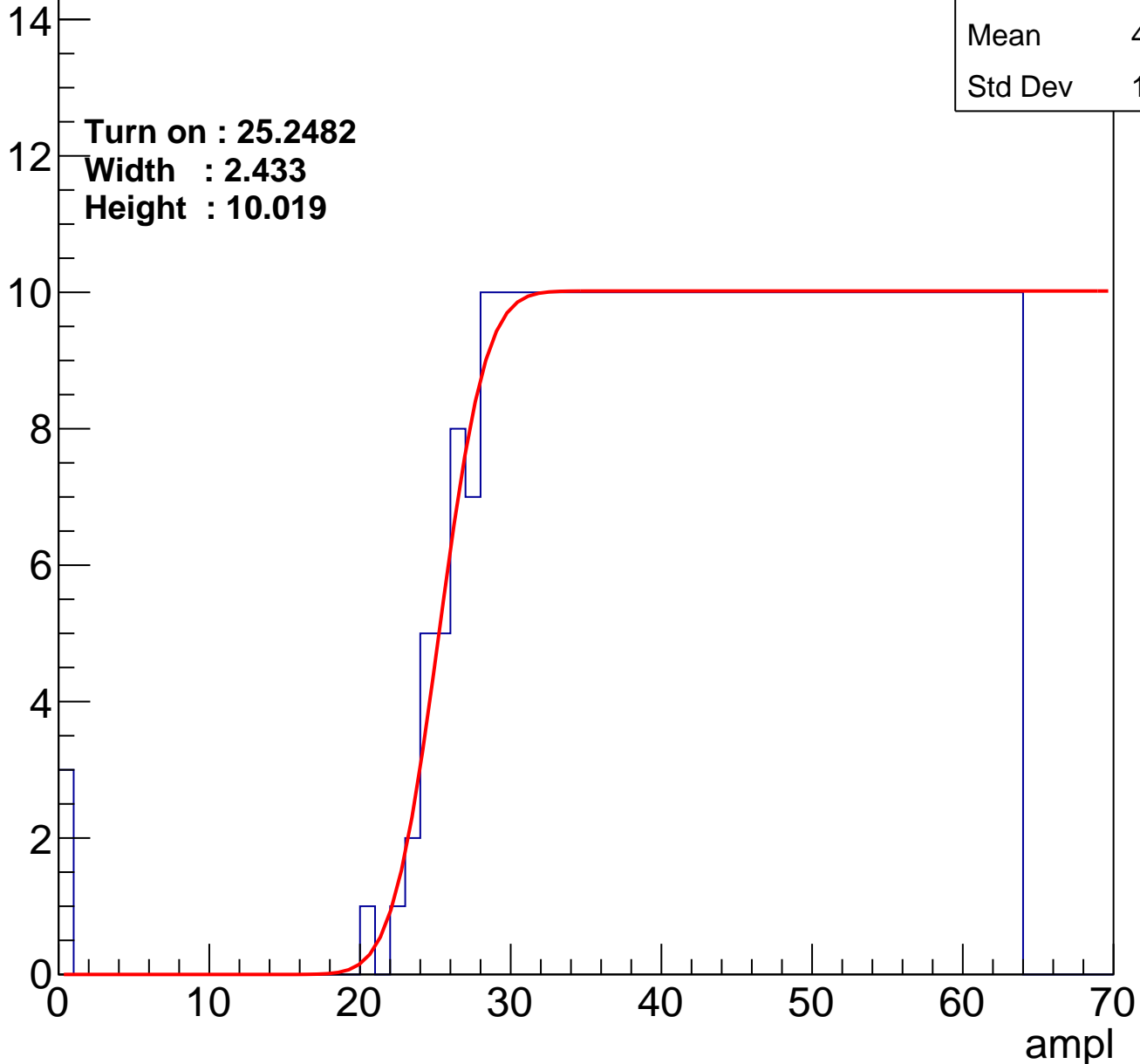
Entries	392
Mean	43.65
Std Dev	11.93

Turn on : 25.2482

Width : 2.433

Height : 10.019

Entry



B1L102S, U3-ch20

calib_packv5_042523_0143.root, FC#11, port A2

Entries	394
Mean	43.44
Std Dev	12.21

Turn on : 24.9307

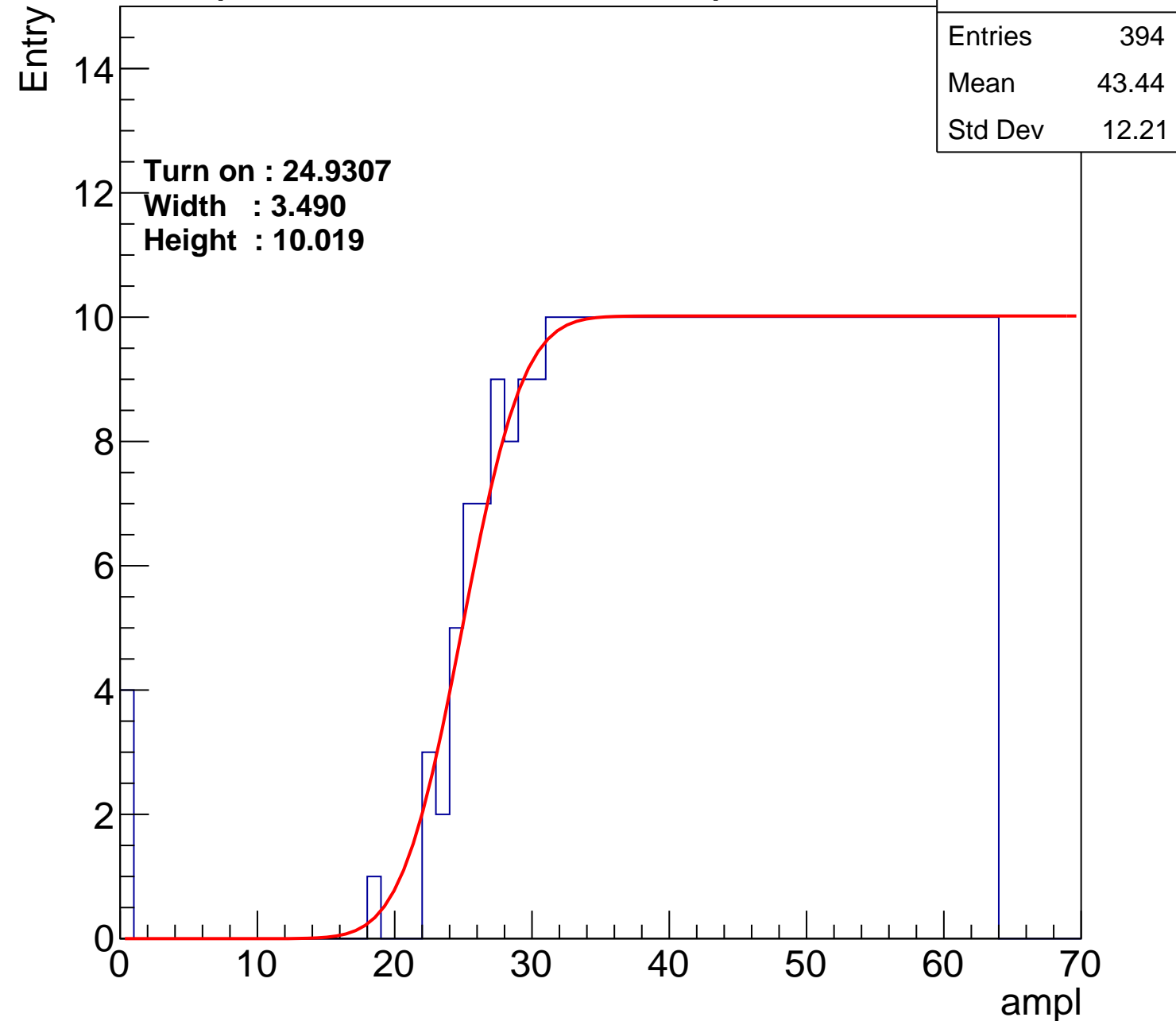
Width : 3.490

Height : 10.019

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch21

calib_packv5_042523_0143.root, FC#11, port A2

Entries	405
Mean	42.97
Std Dev	12.32

Turn on : 24.4452

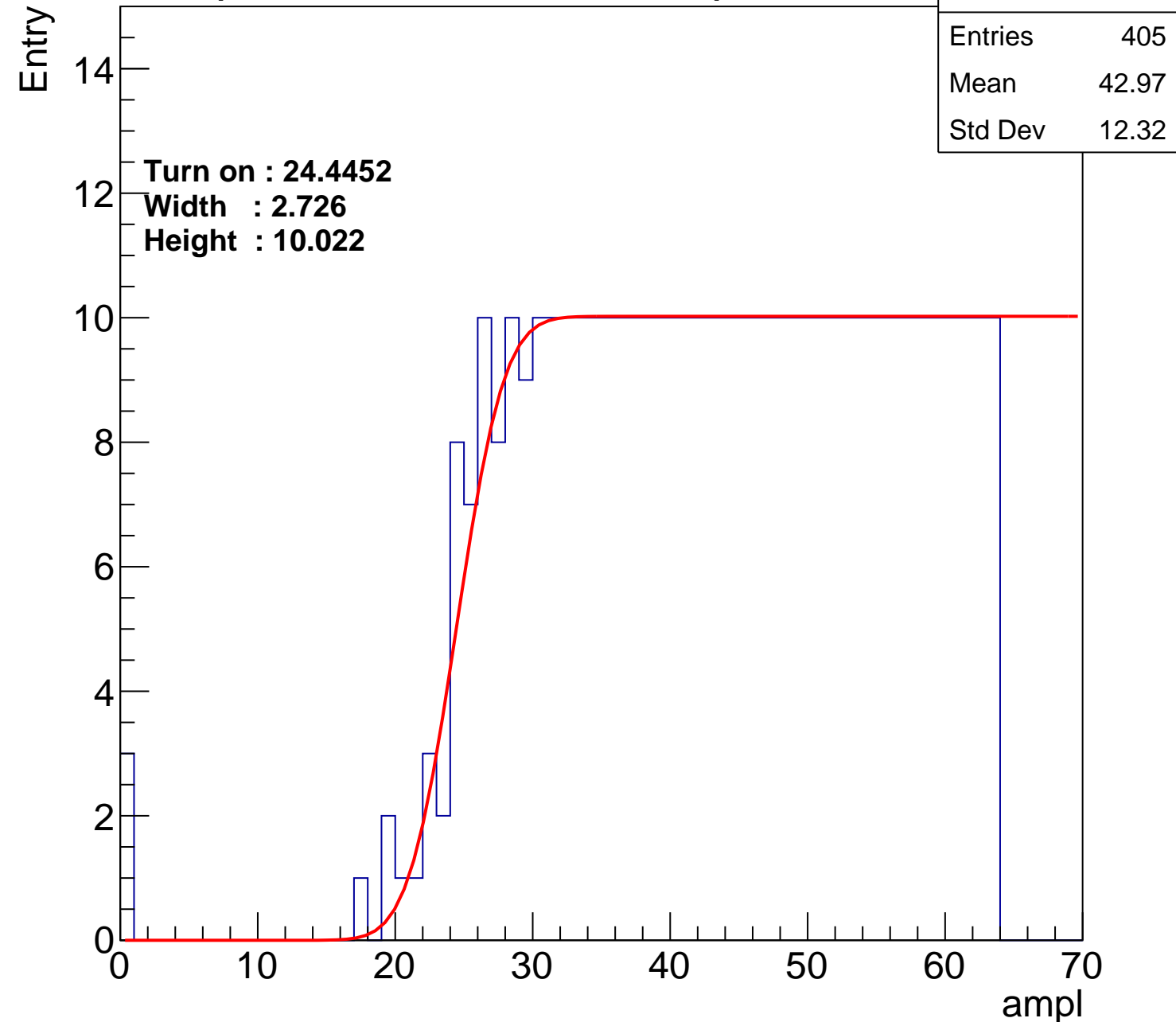
Width : 2.726

Height : 10.022

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch22

calib_packv5_042523_0143.root, FC#11, port A2

Entries	397
Mean	43.3
Std Dev	12.21

Turn on : 24.8675

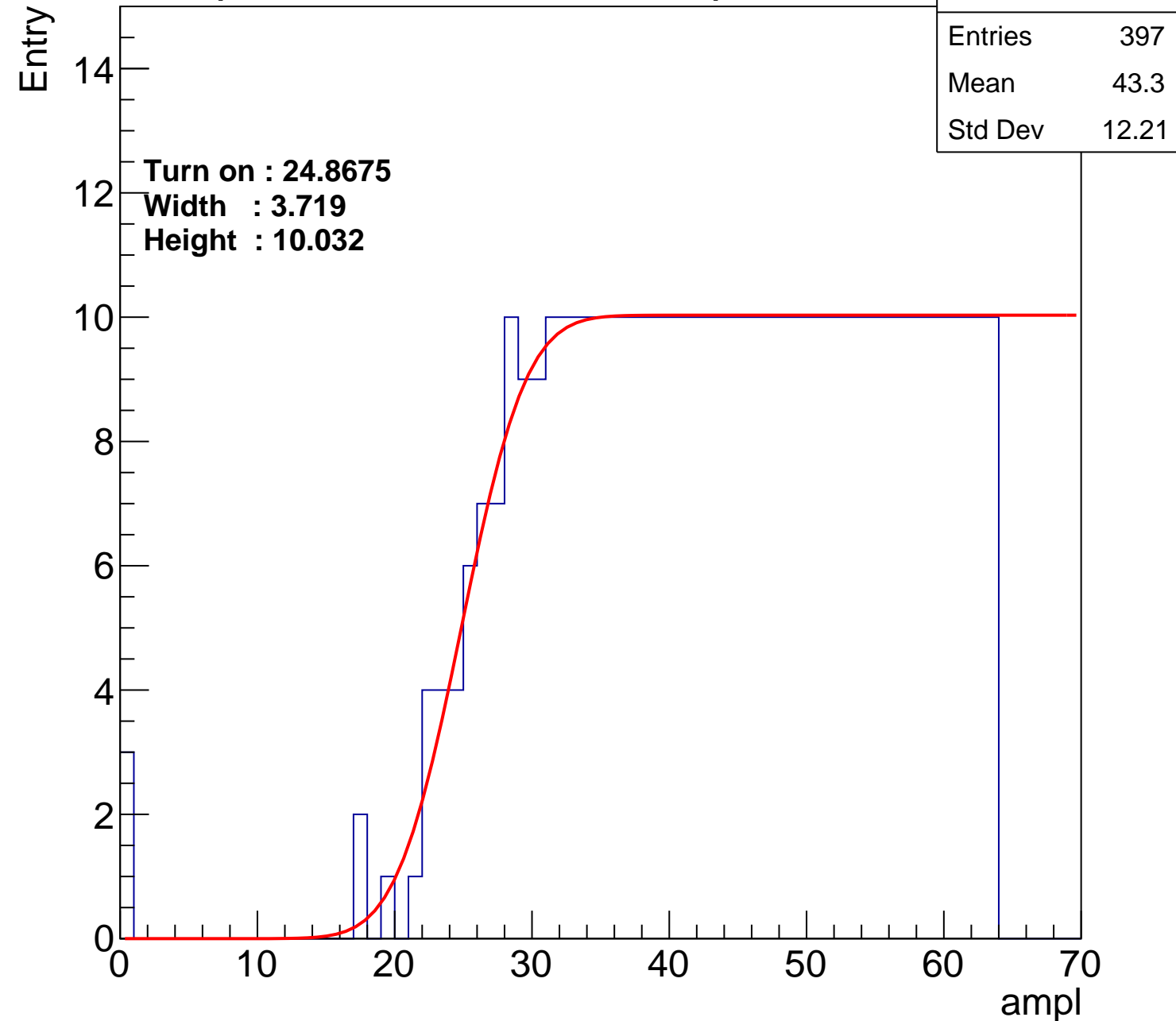
Width : 3.719

Height : 10.032

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch23

calib_packv5_042523_0143.root, FC#11, port A2

Entries	376
Mean	44.35
Std Dev	11.65

Turn on : 26.4184

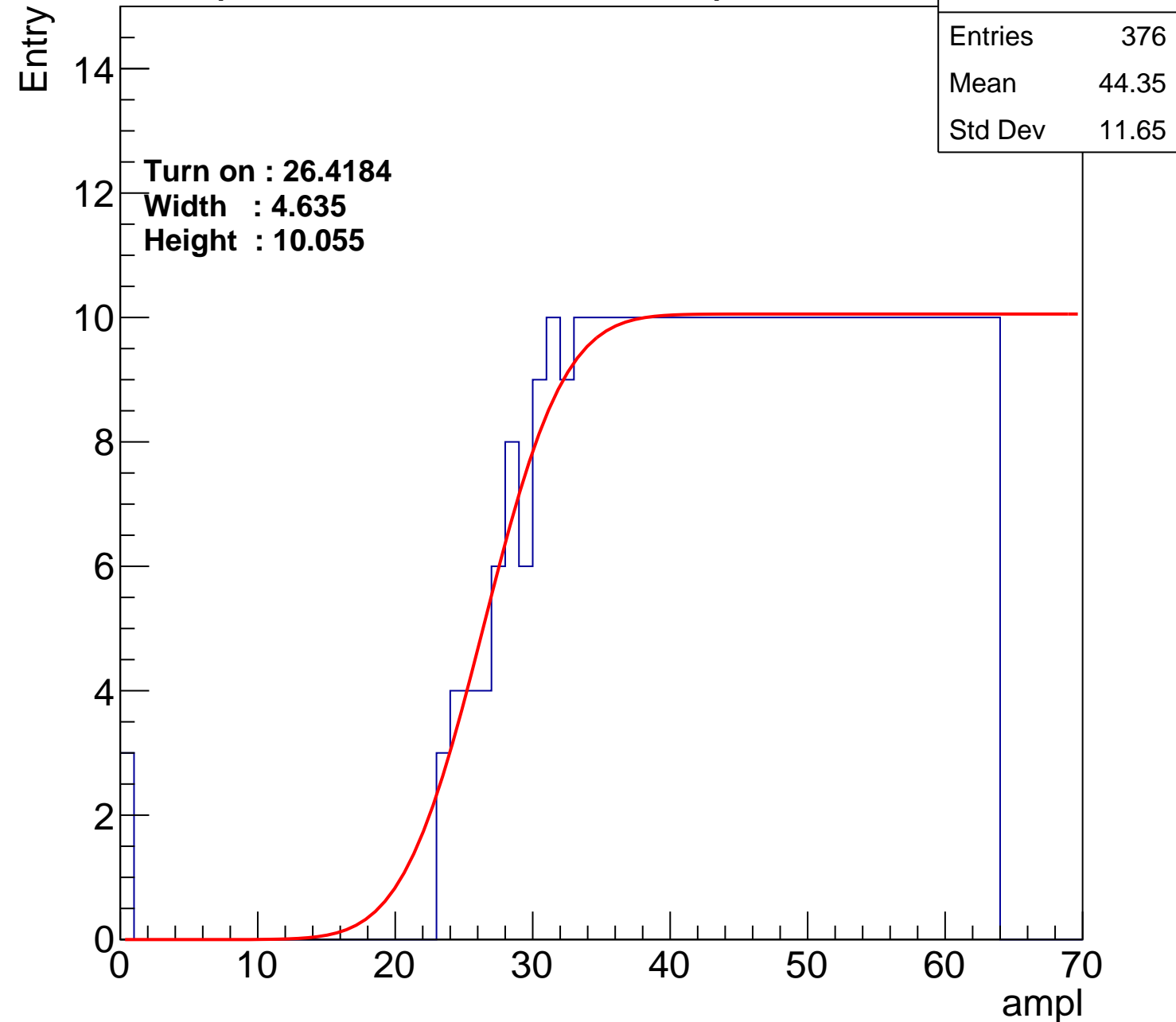
Width : 4.635

Height : 10.055

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch24

calib_packv5_042523_0143.root, FC#11, port A2

Entries	384
Mean	44.09
Std Dev	11.57

Turn on : 25.5196

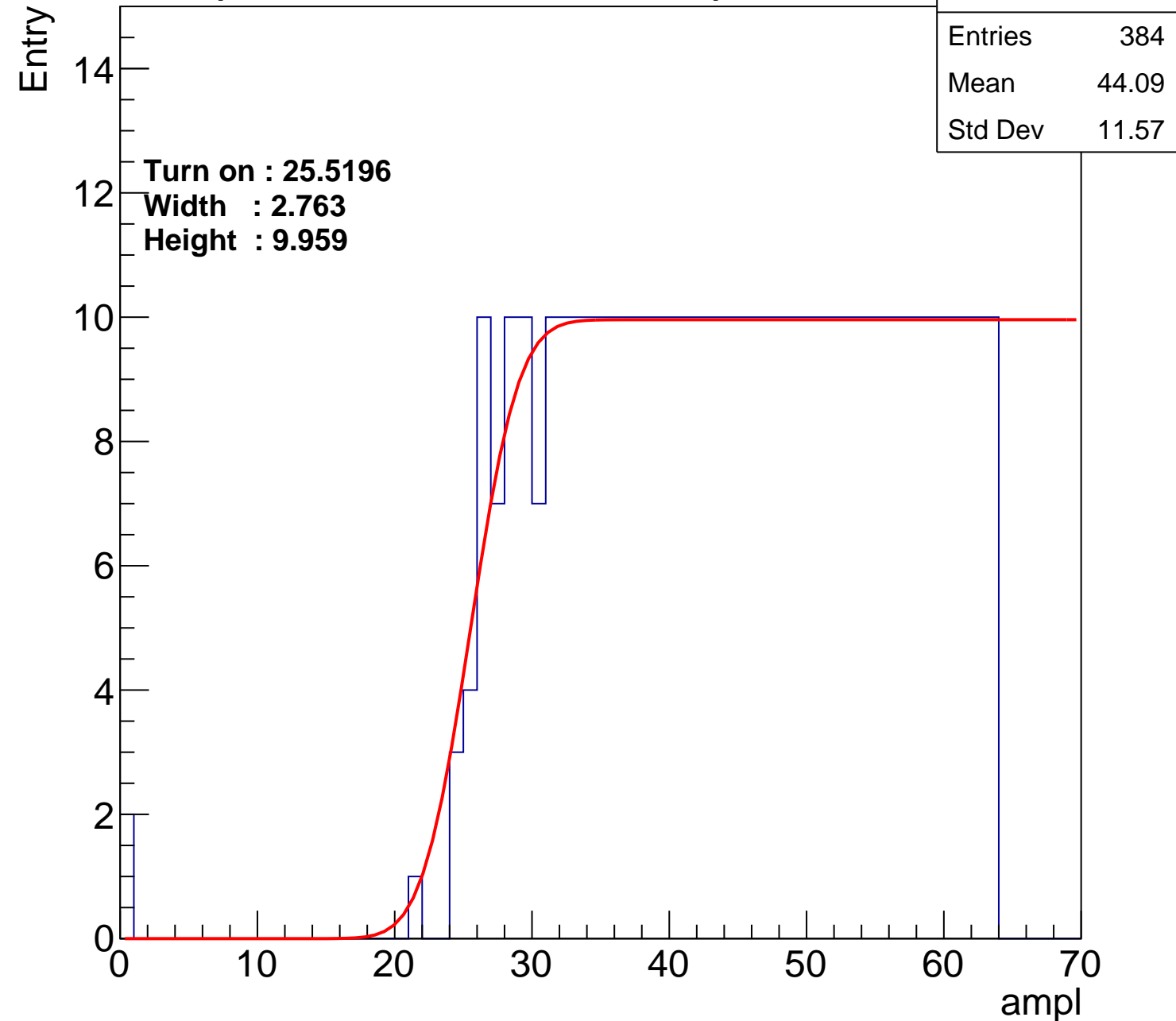
Width : 2.763

Height : 9.959

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch25

calib_packv5_042523_0143.root, FC#11, port A2

Entries	394
Mean	43.39
Std Dev	12.29

Turn on : 25.9409

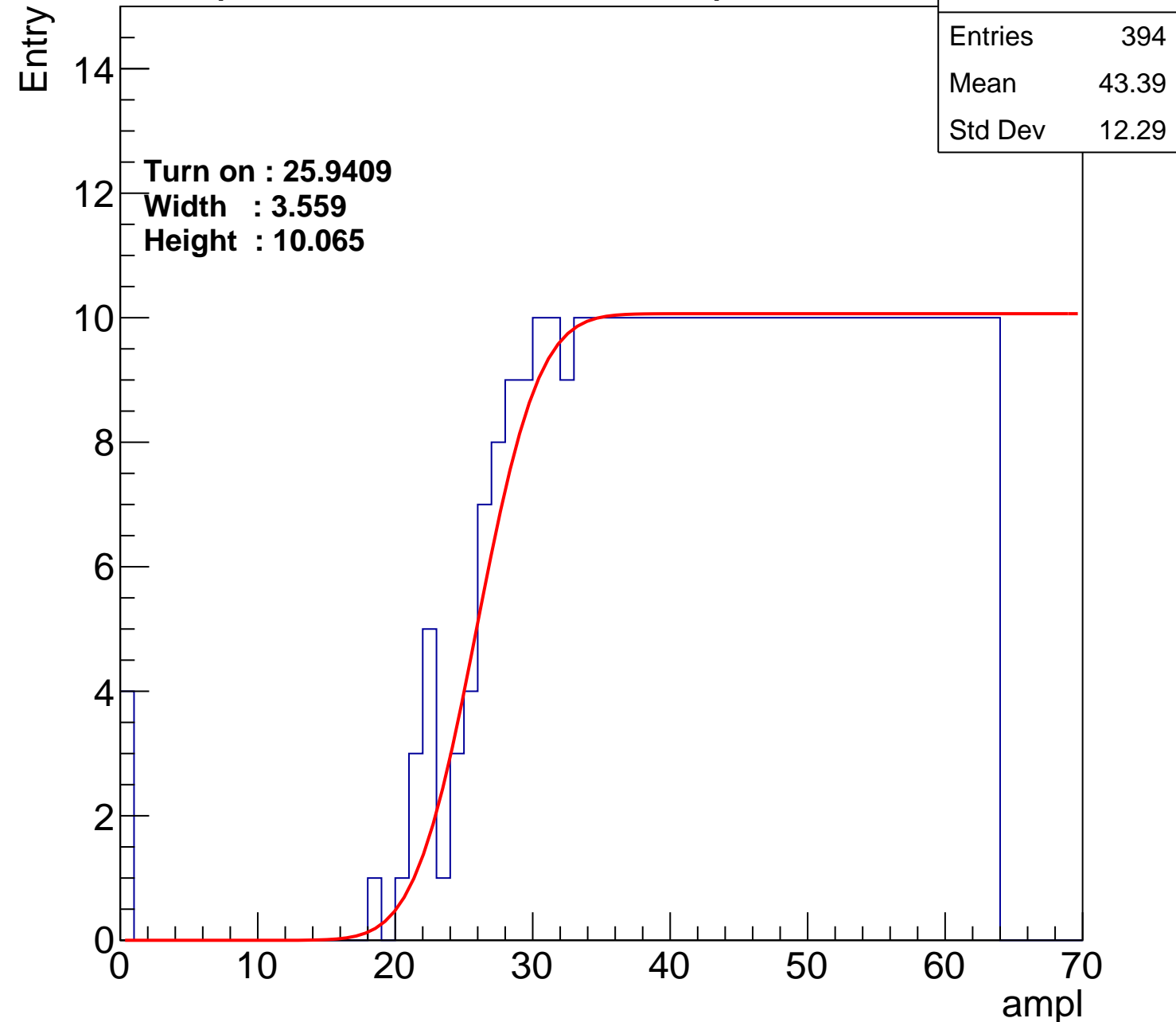
Width : 3.559

Height : 10.065

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch26

calib_packv5_042523_0143.root, FC#11, port A2

Entries	405
Mean	42.94
Std Dev	12.37

Turn on : 24.5404

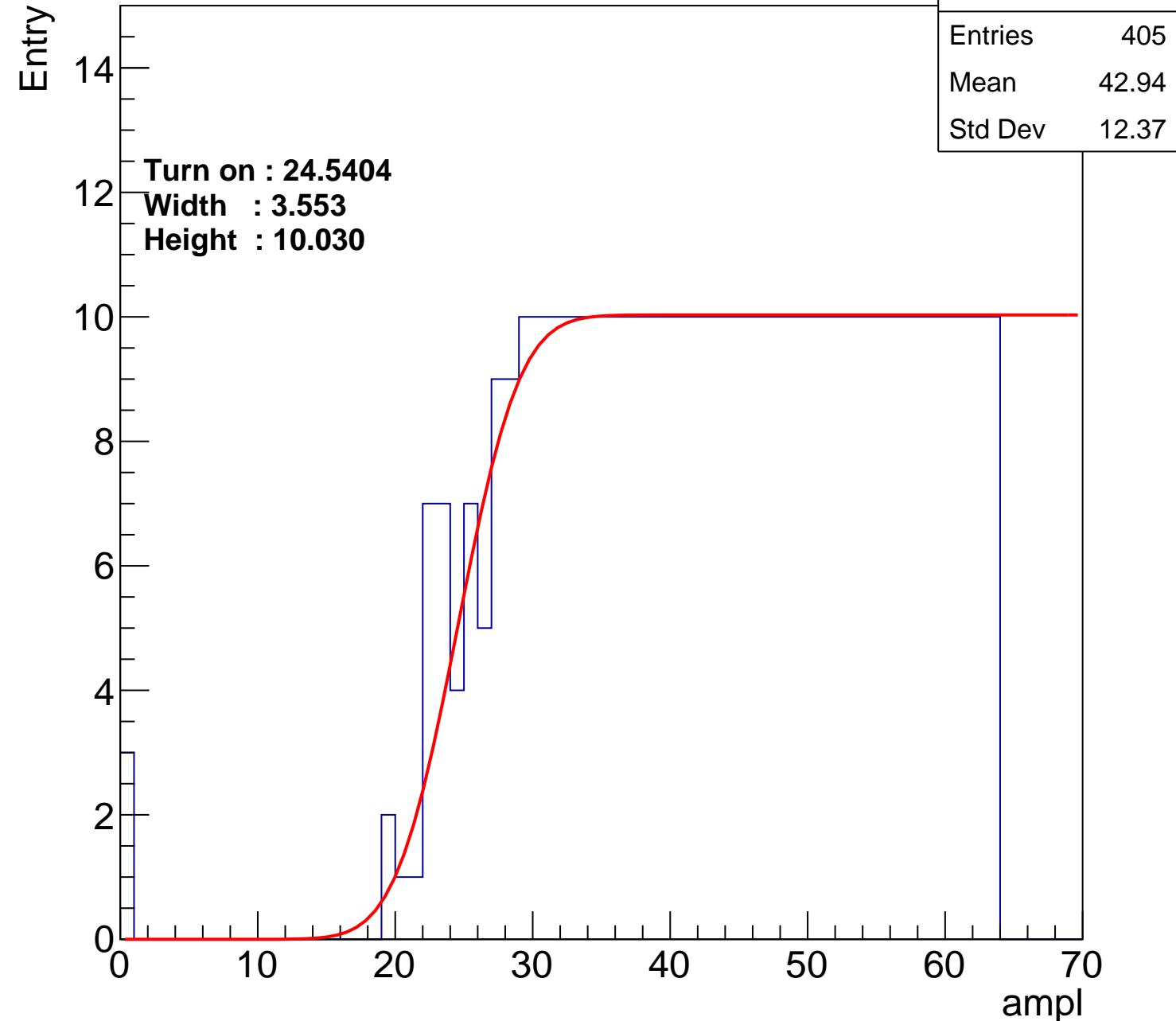
Width : 3.553

Height : 10.030

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch27

calib_packv5_042523_0143.root, FC#11, port A2

Entries	384
Mean	43.92
Std Dev	11.98

Turn on : 26.1112

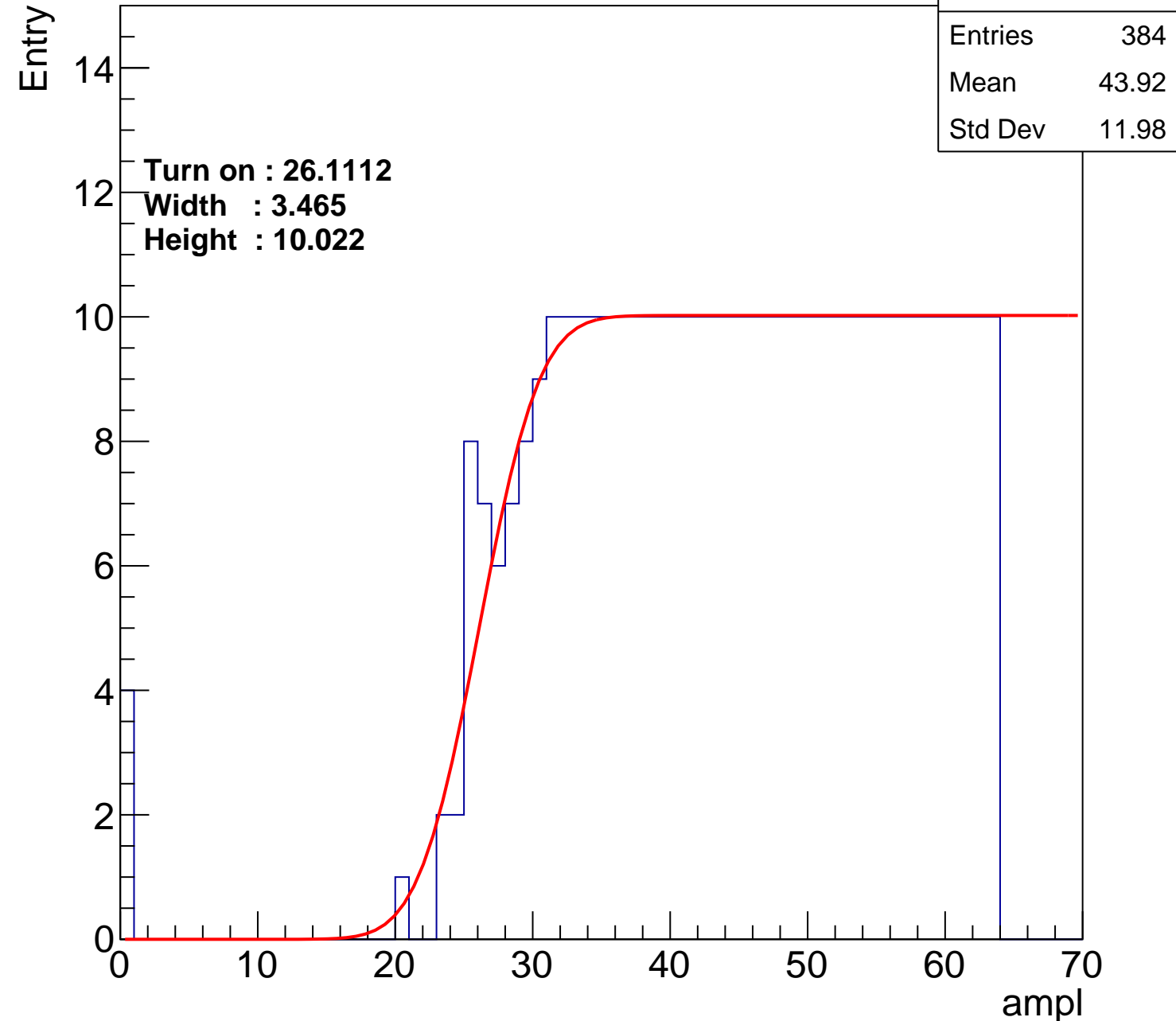
Width : 3.465

Height : 10.022

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch28

calib_packv5_042523_0143.root, FC#11, port A2

Entries	397
Mean	43.47
Std Dev	11.95

Turn on : 24.7357

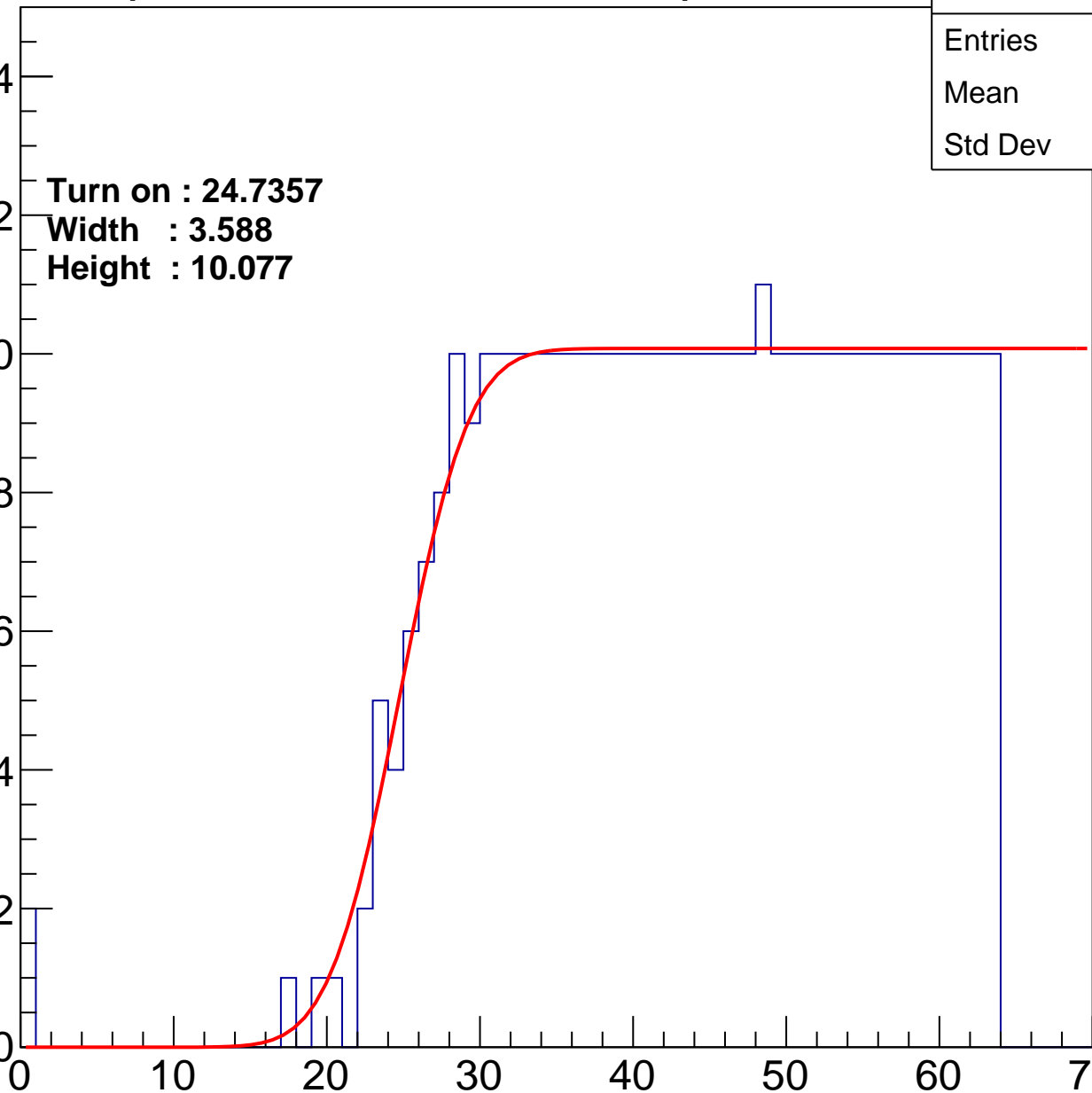
Width : 3.588

Height : 10.077

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch29

calib_packv5_042523_0143.root, FC#11, port A2

Entries	389
Mean	43.81
Std Dev	11.75

Turn on : 25.3435

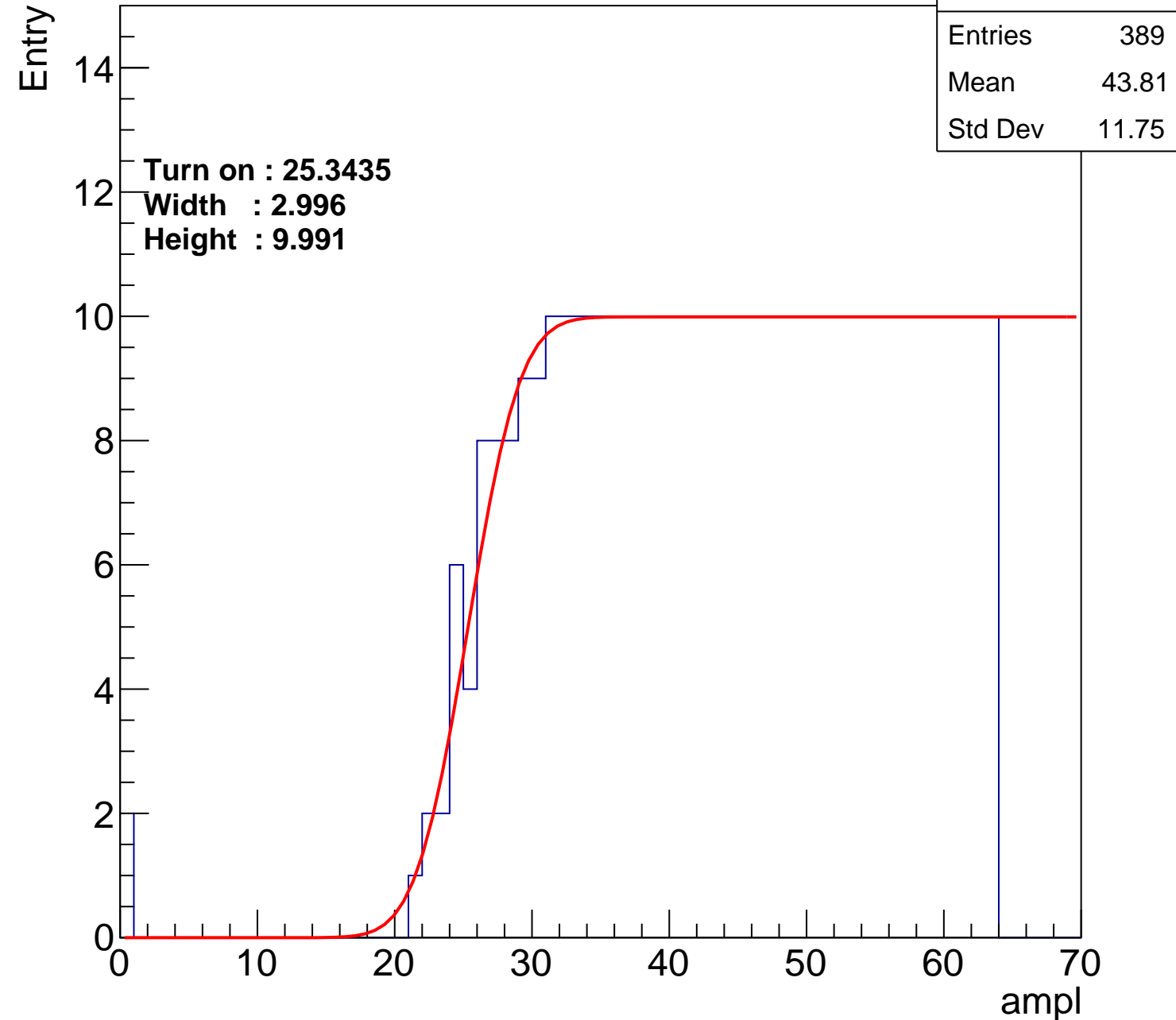
Width : 2.996

Height : 9.991

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch30

calib_packv5_042523_0143.root, FC#11, port A2

Entries	399
Mean	43.24
Std Dev	12.26

Turn on : 24.6225

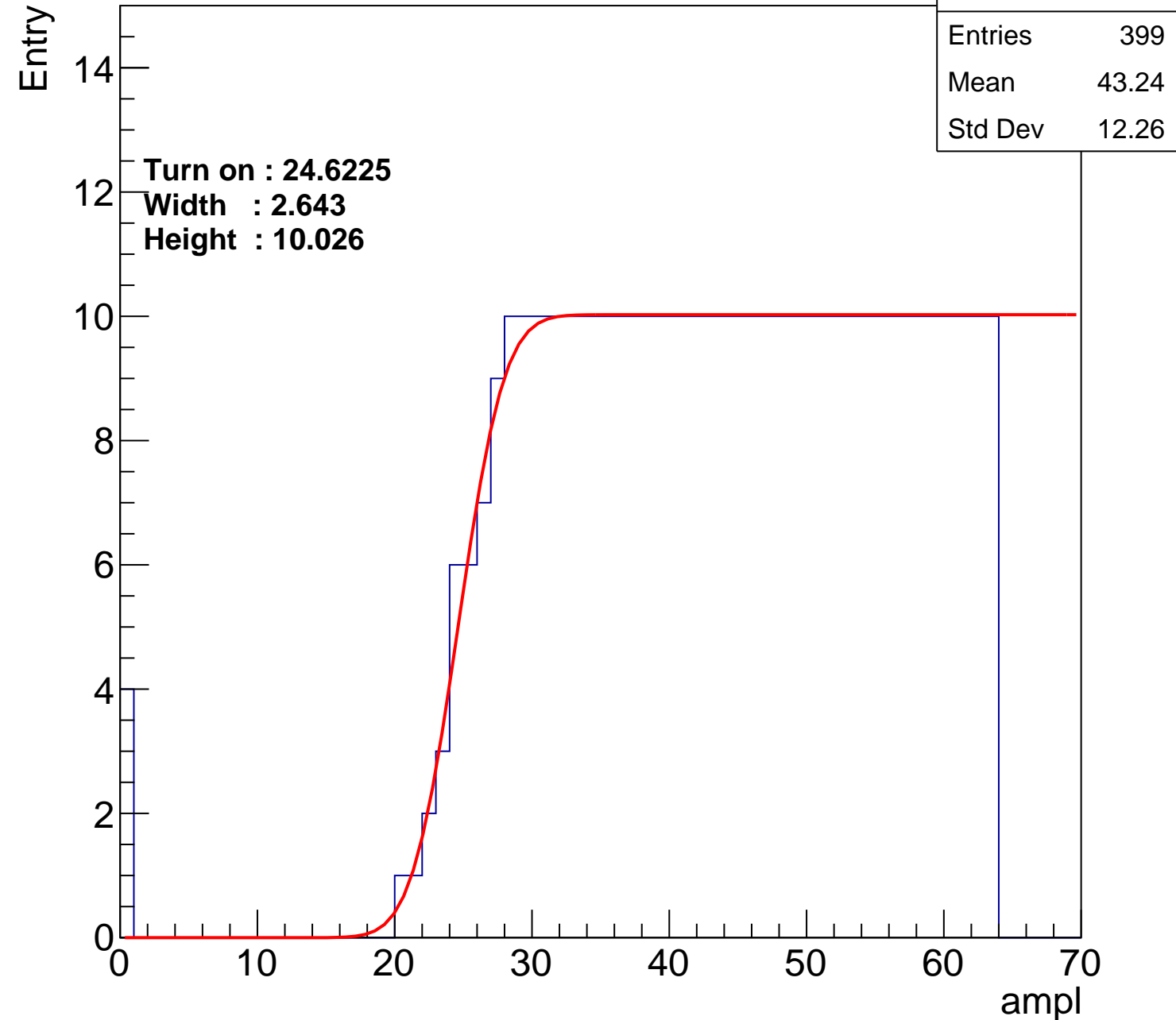
Width : 2.643

Height : 10.026

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch31

calib_packv5_042523_0143.root, FC#11, port A2

Entries	376
Mean	44.43
Std Dev	11.46

Turn on : 27.0481

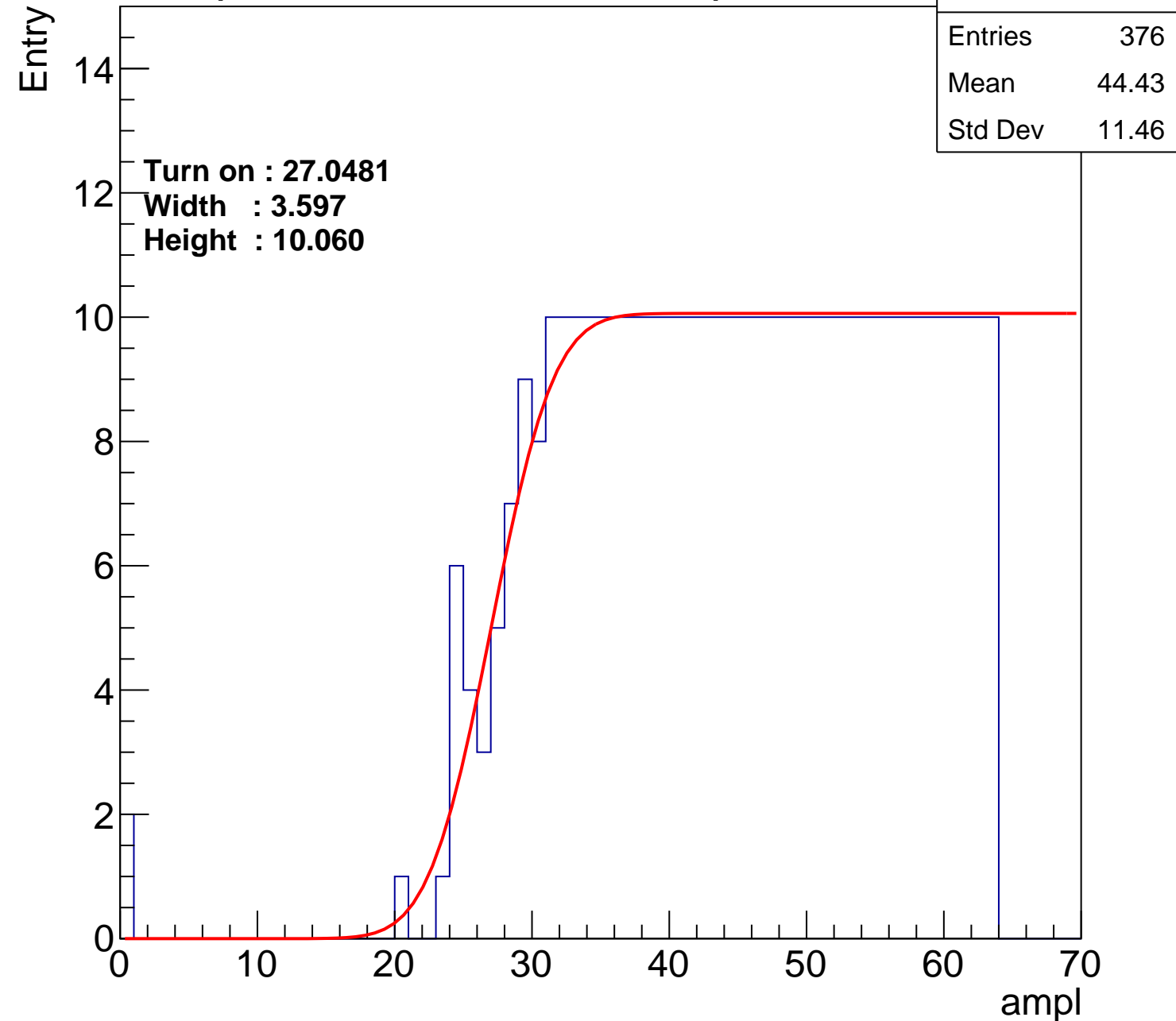
Width : 3.597

Height : 10.060

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch32

calib_packv5_042523_0143.root, FC#11, port A2

Entries	383
Mean	44.07
Std Dev	11.67

Turn on : 26.1463

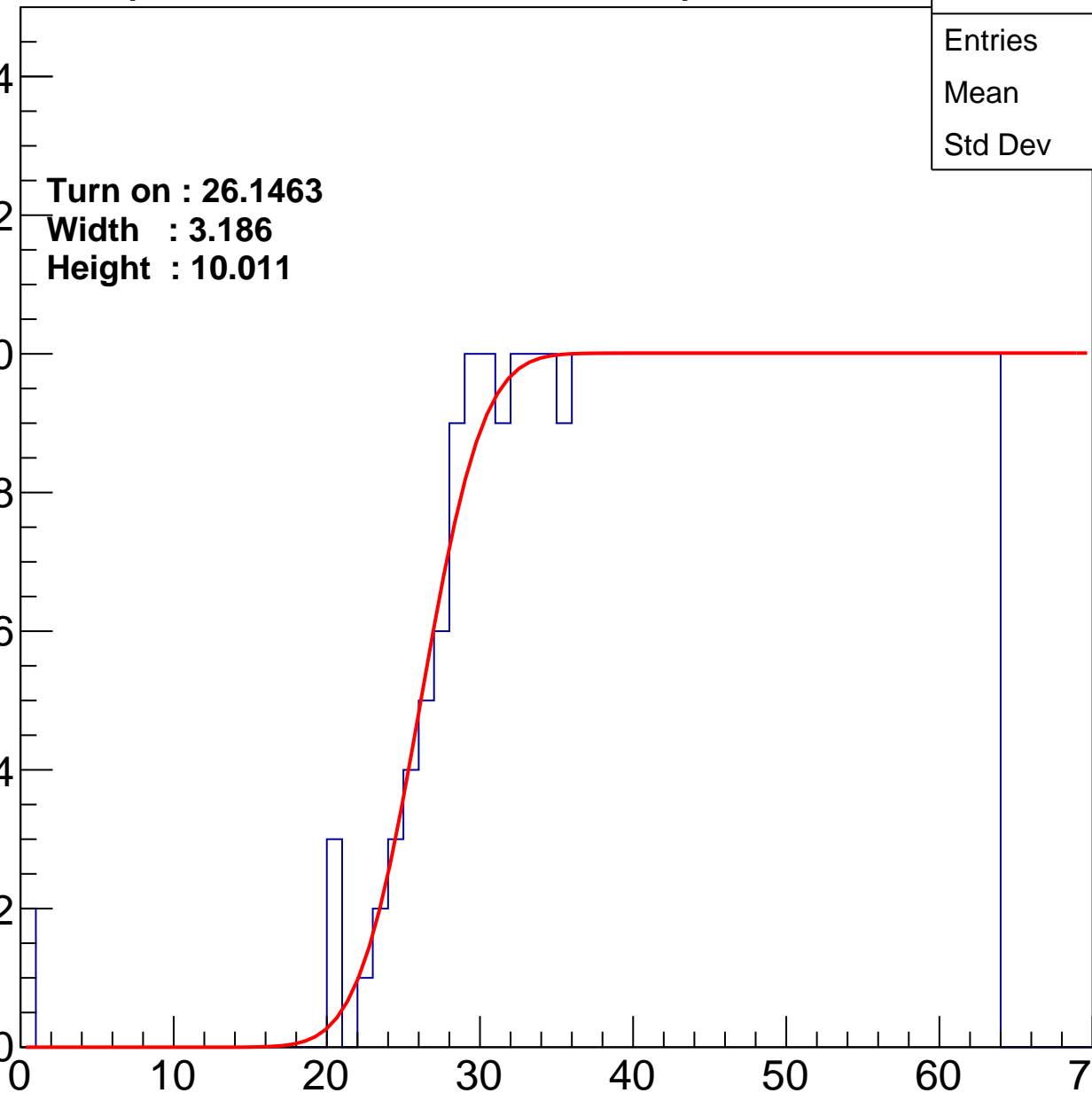
Width : 3.186

Height : 10.011

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch33

calib_packv5_042523_0143.root, FC#11, port A2

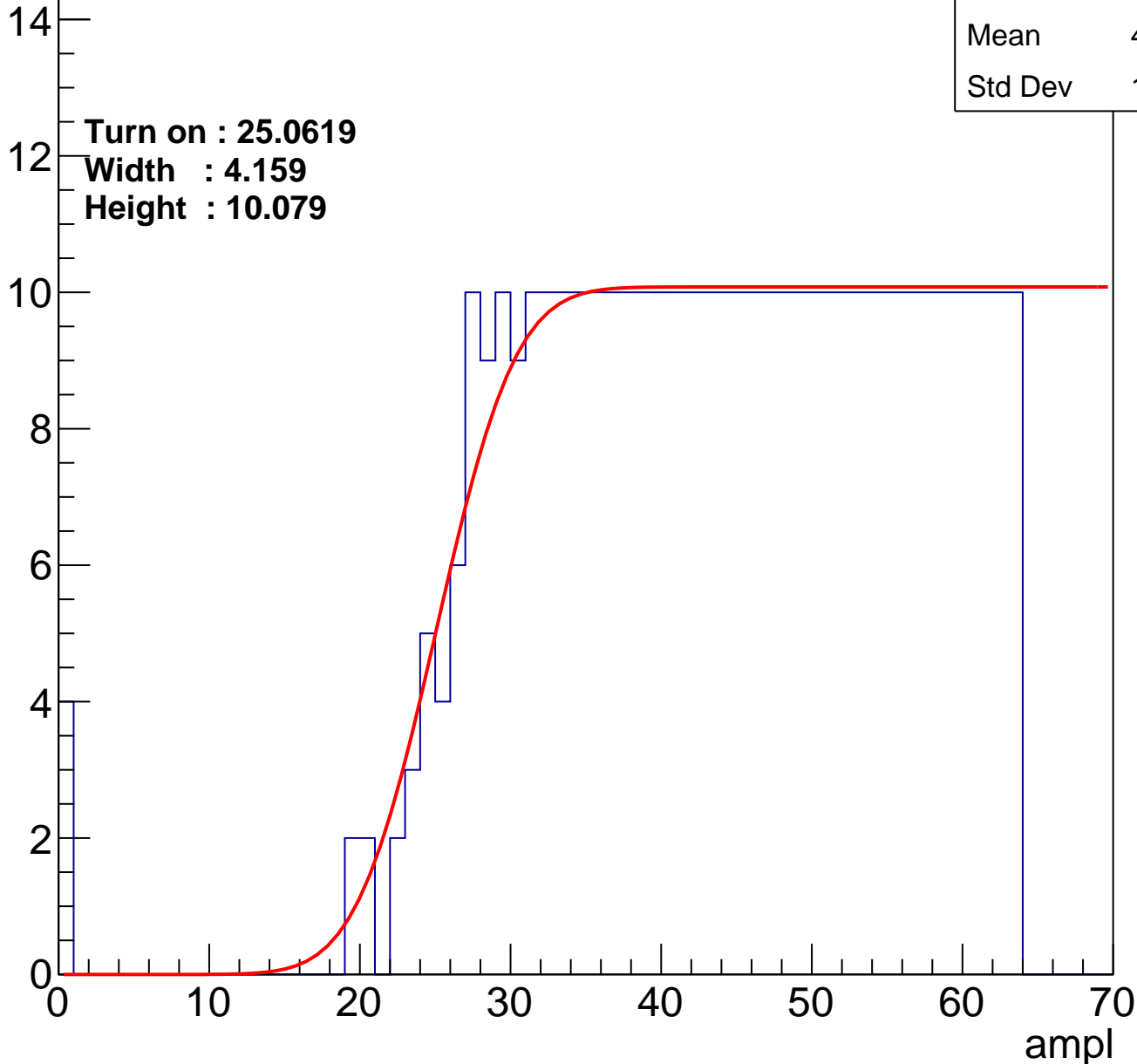
Entries	396
Mean	43.33
Std Dev	12.28

Turn on : 25.0619

Width : 4.159

Height : 10.079

Entry



B1L102S, U3-ch34

calib_packv5_042523_0143.root, FC#11, port A2

Entries	377
Mean	44.3
Std Dev	11.69

Turn on : 27.0228

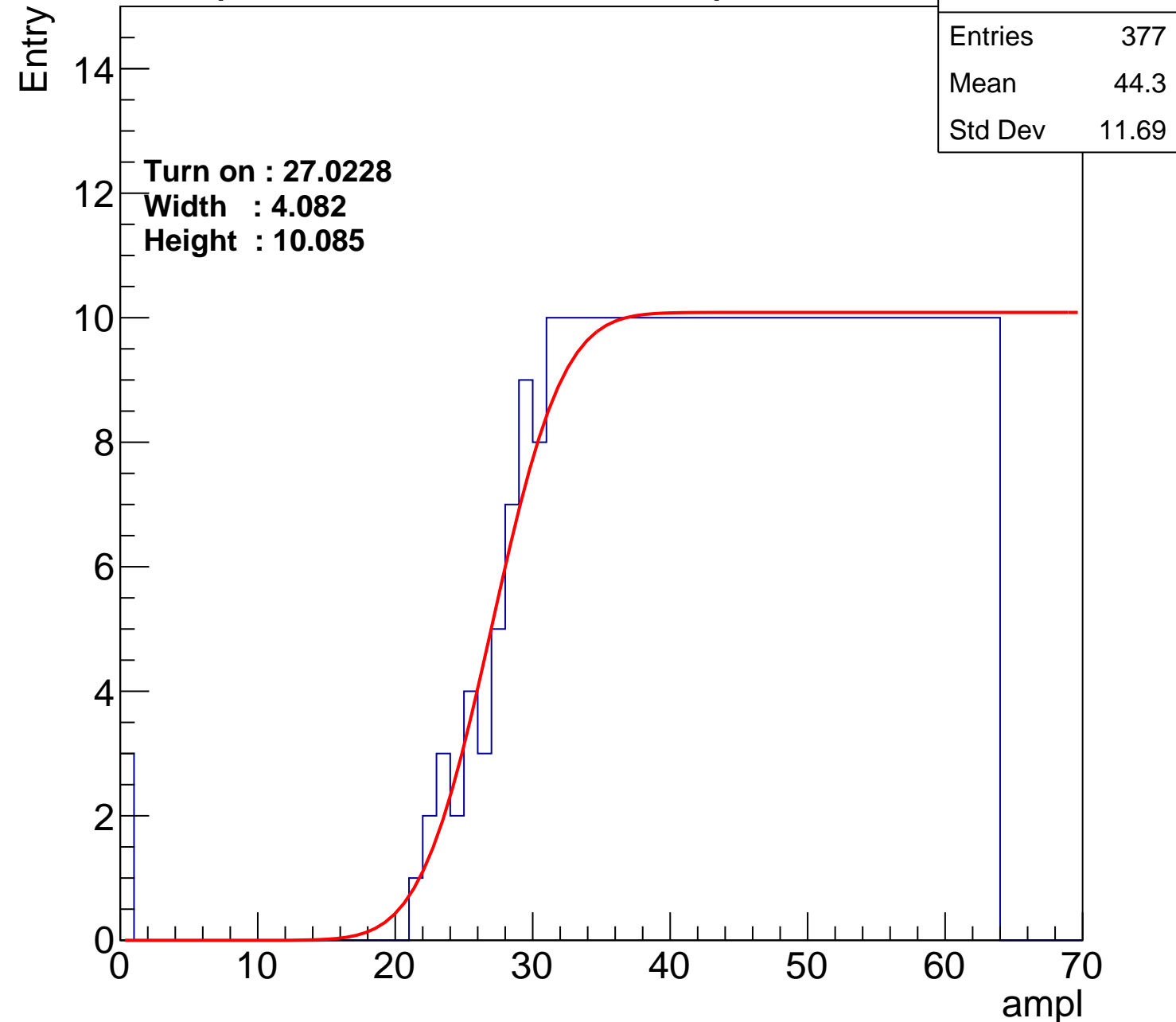
Width : 4.082

Height : 10.085

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch35

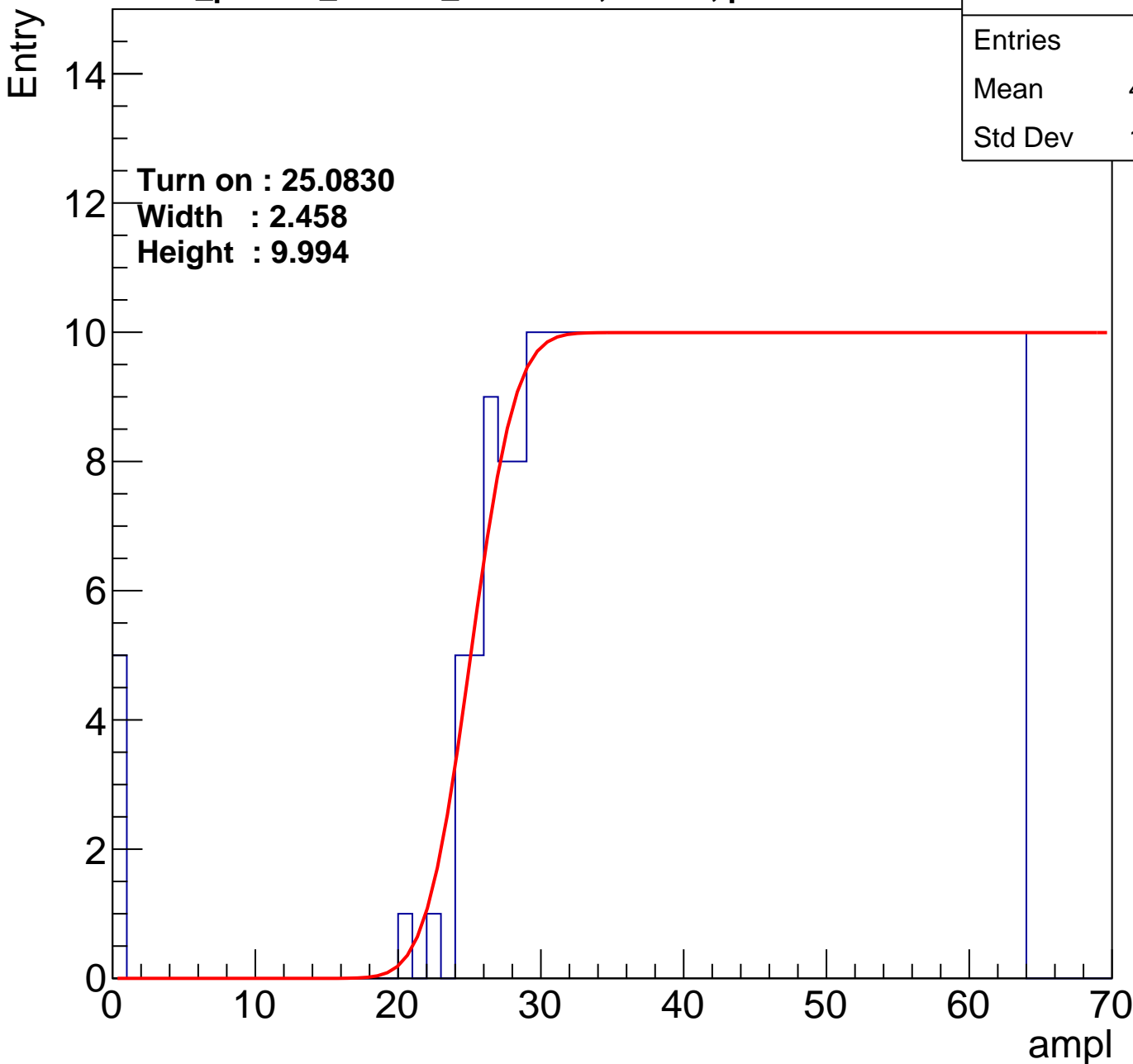
calib_packv5_042523_0143.root, FC#11, port A2

Turn on : 25.0830

Width : 2.458

Height : 9.994

Entries	392
Mean	43.52
Std Dev	12.25



B1L102S, U3-ch36

calib_packv5_042523_0143.root, FC#11, port A2

Entries	399
Mean	43.34
Std Dev	12

Turn on : 24.5578

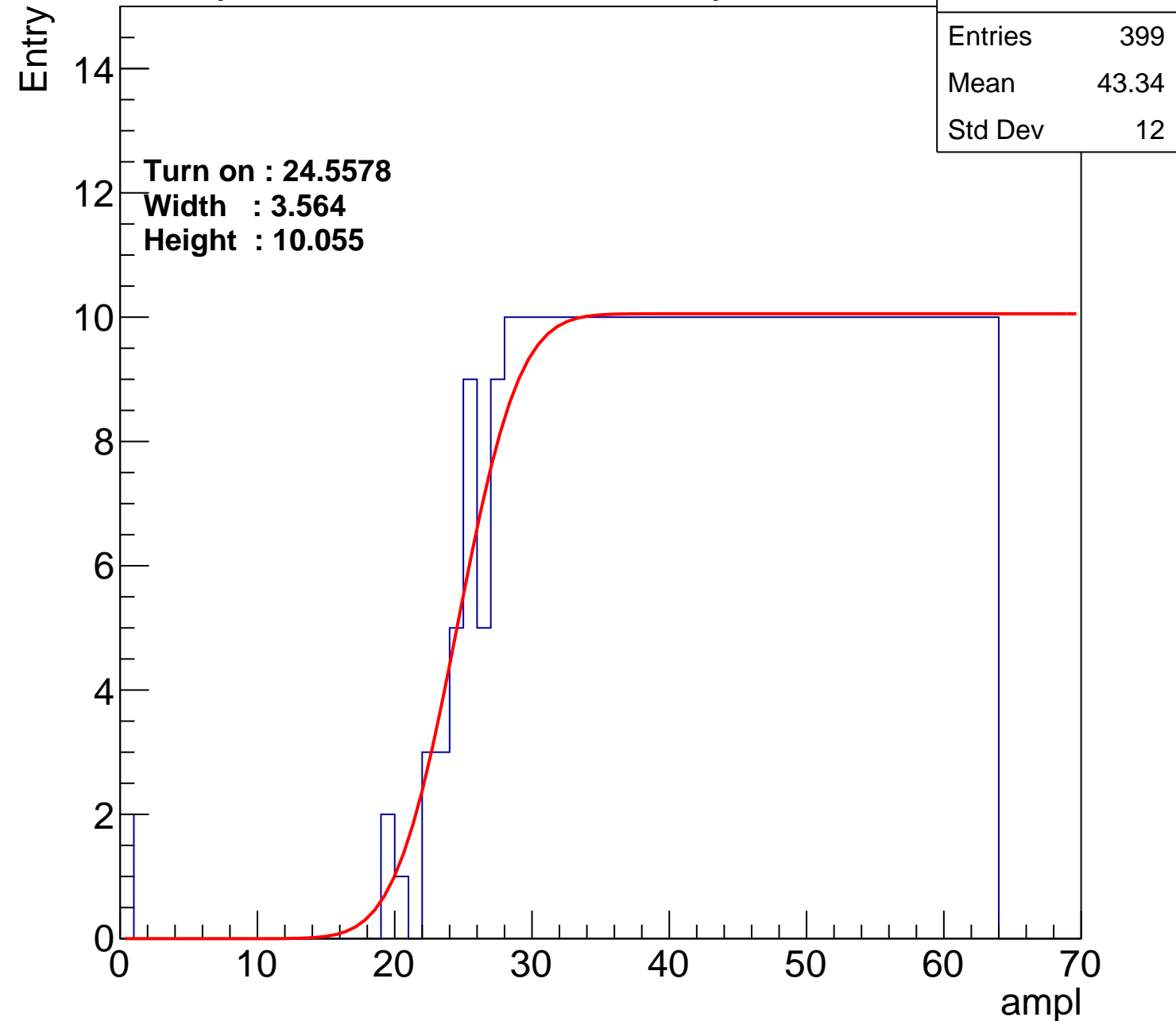
Width : 3.564

Height : 10.055

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch37

calib_packv5_042523_0143.root, FC#11, port A2

Entries	386
Mean	43.89
Std Dev	11.86

Turn on : 25.6957

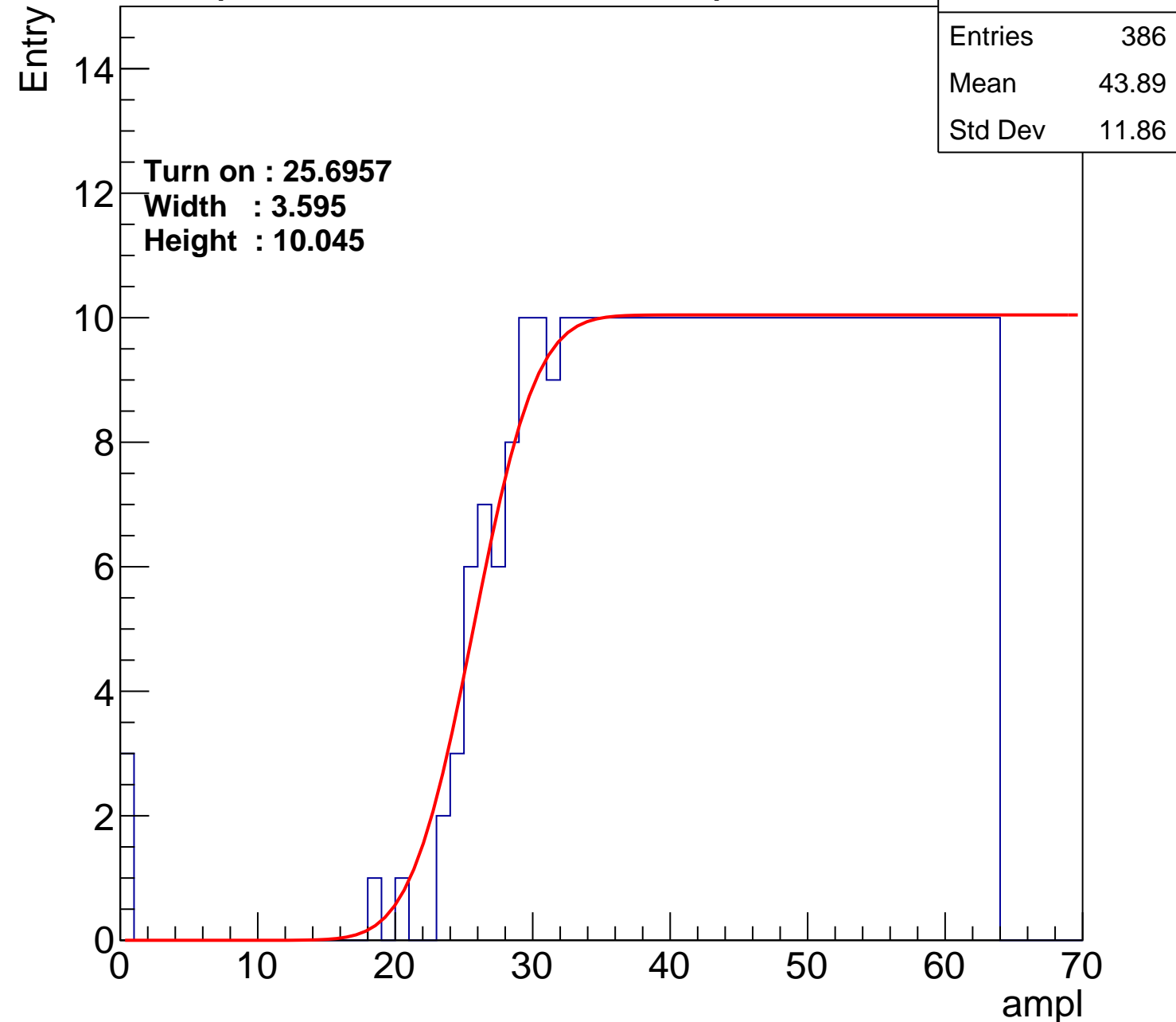
Width : 3.595

Height : 10.045

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch38

calib_packv5_042523_0143.root, FC#11, port A2

Entries	389
Mean	43.76
Std Dev	11.9

Turn on : 25.9276

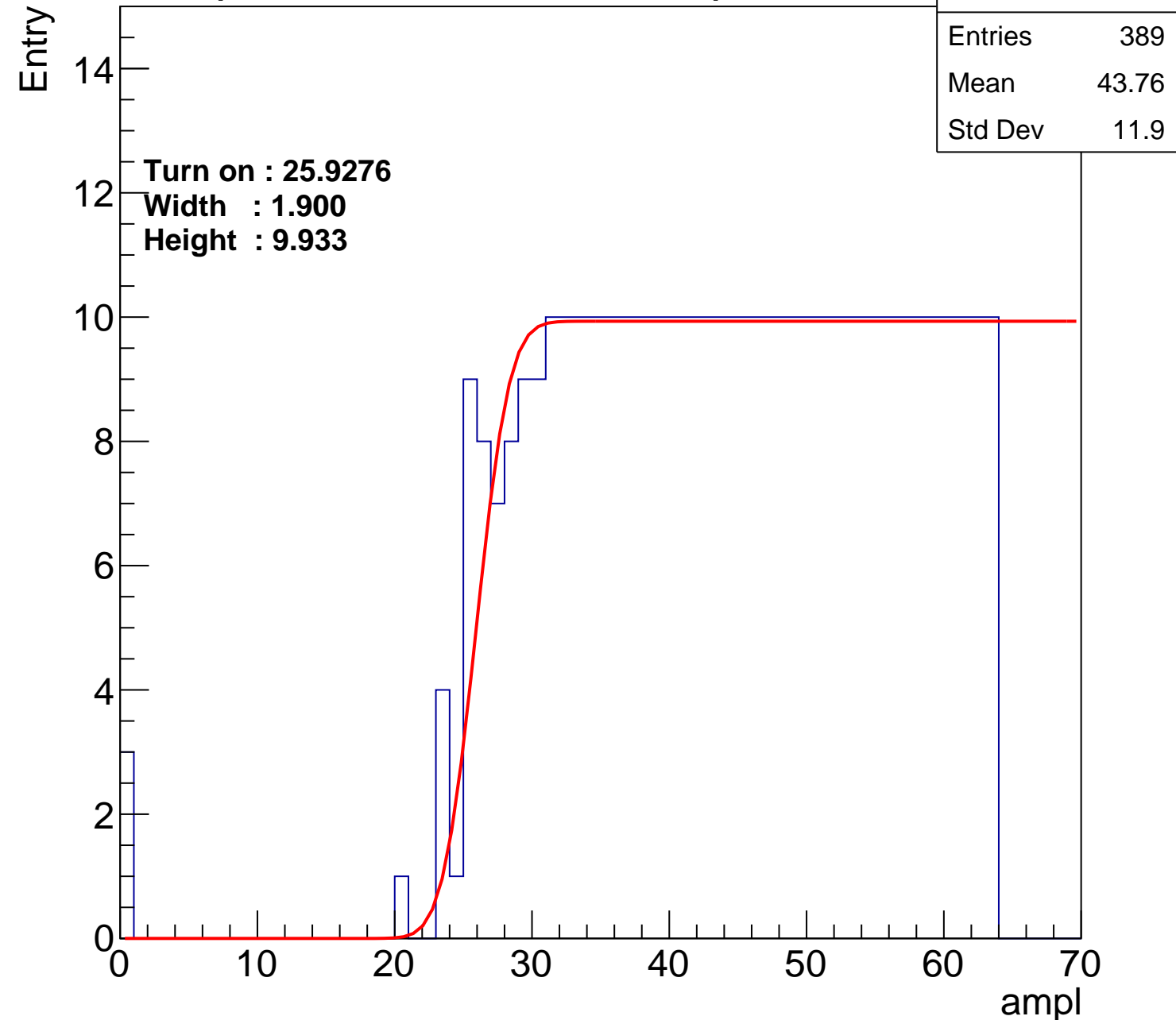
Width : 1.900

Height : 9.933

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch39

calib_packv5_042523_0143.root, FC#11, port A2

Entries	383
Mean	44.08
Std Dev	11.71

Turn on : 25.5848

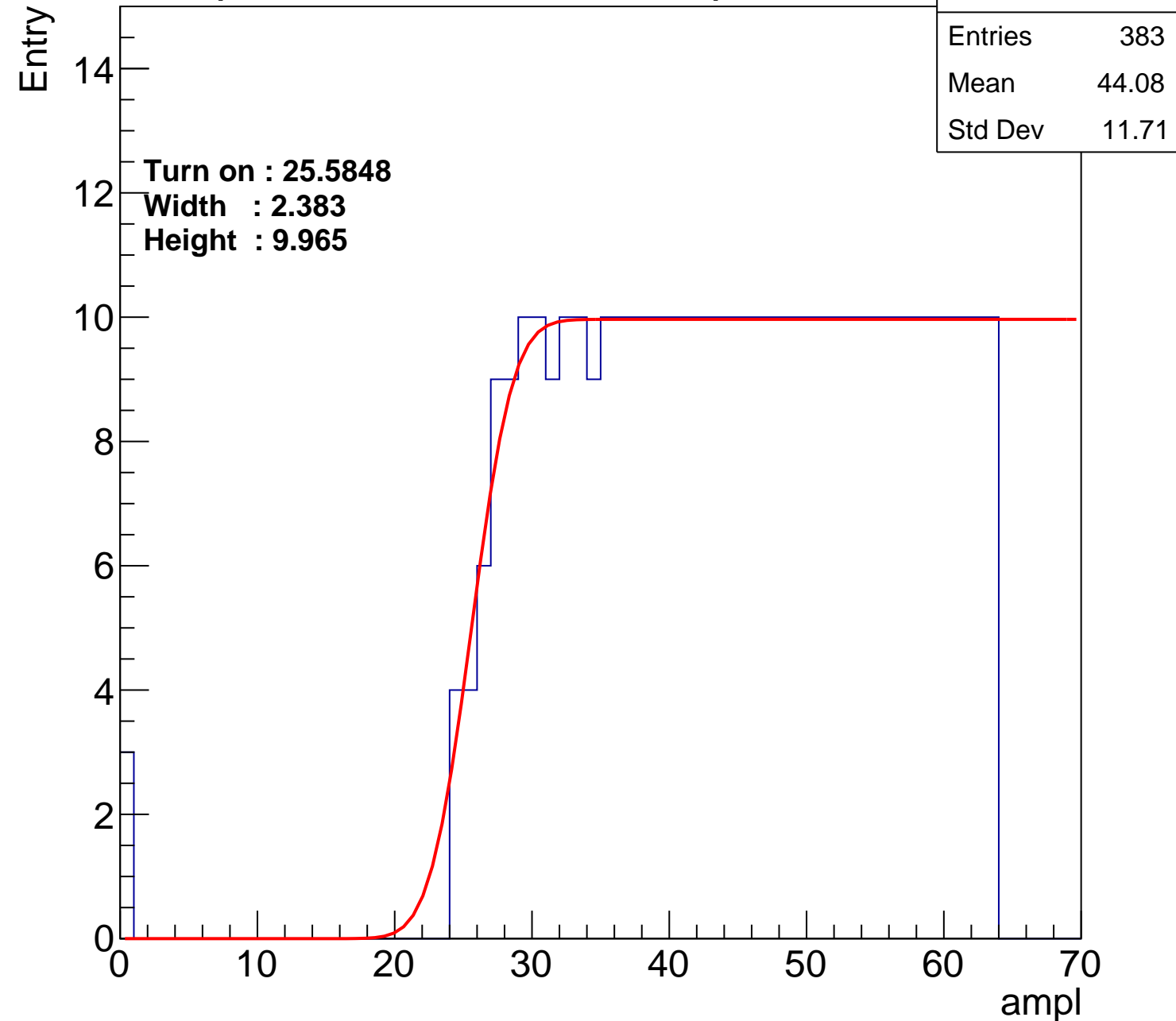
Width : 2.383

Height : 9.965

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch40

calib_packv5_042523_0143.root, FC#11, port A2

Entries	383
Mean	43.93
Std Dev	12.02

Turn on : 25.6876

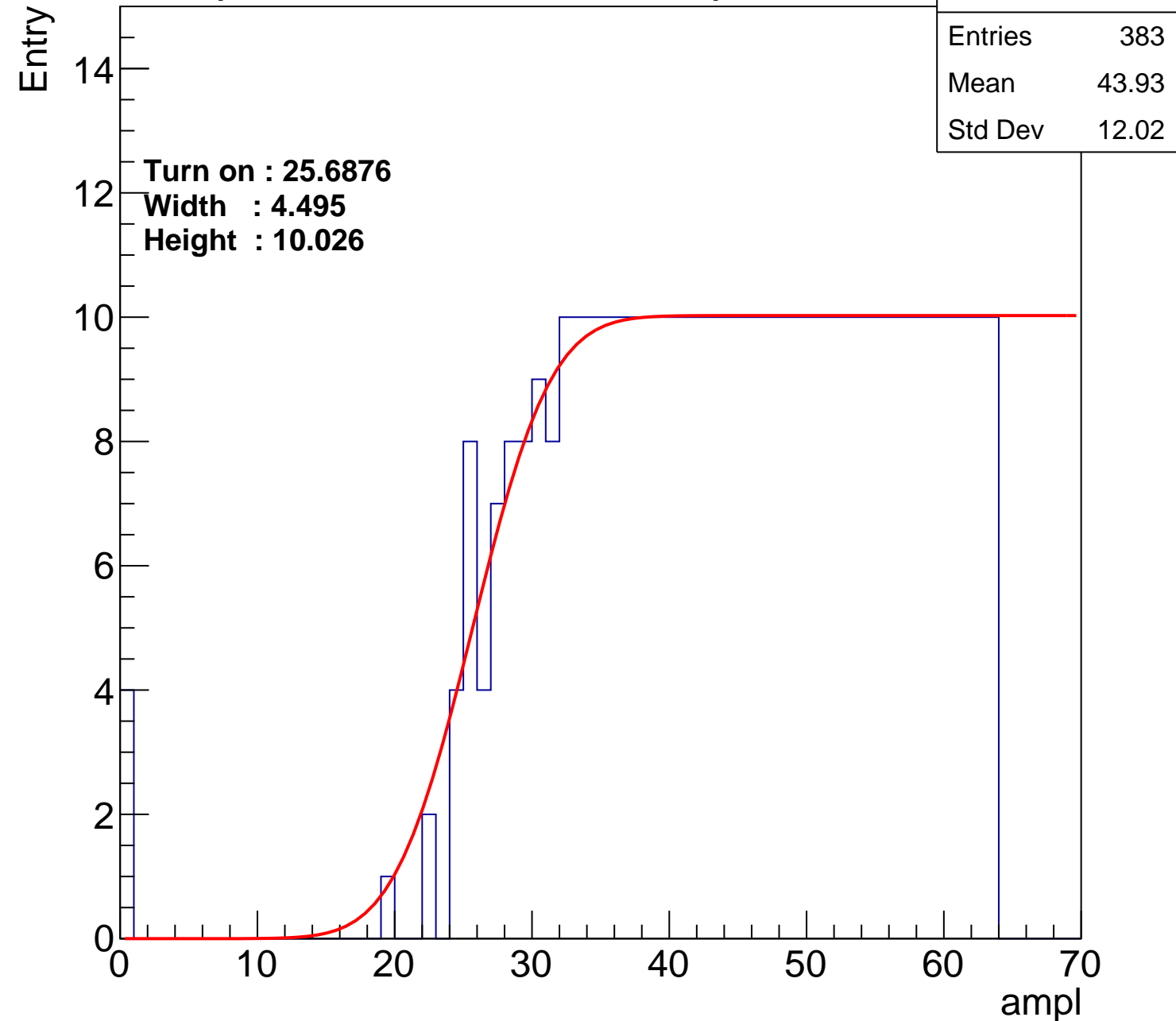
Width : 4.495

Height : 10.026

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch41

calib_packv5_042523_0143.root, FC#11, port A2

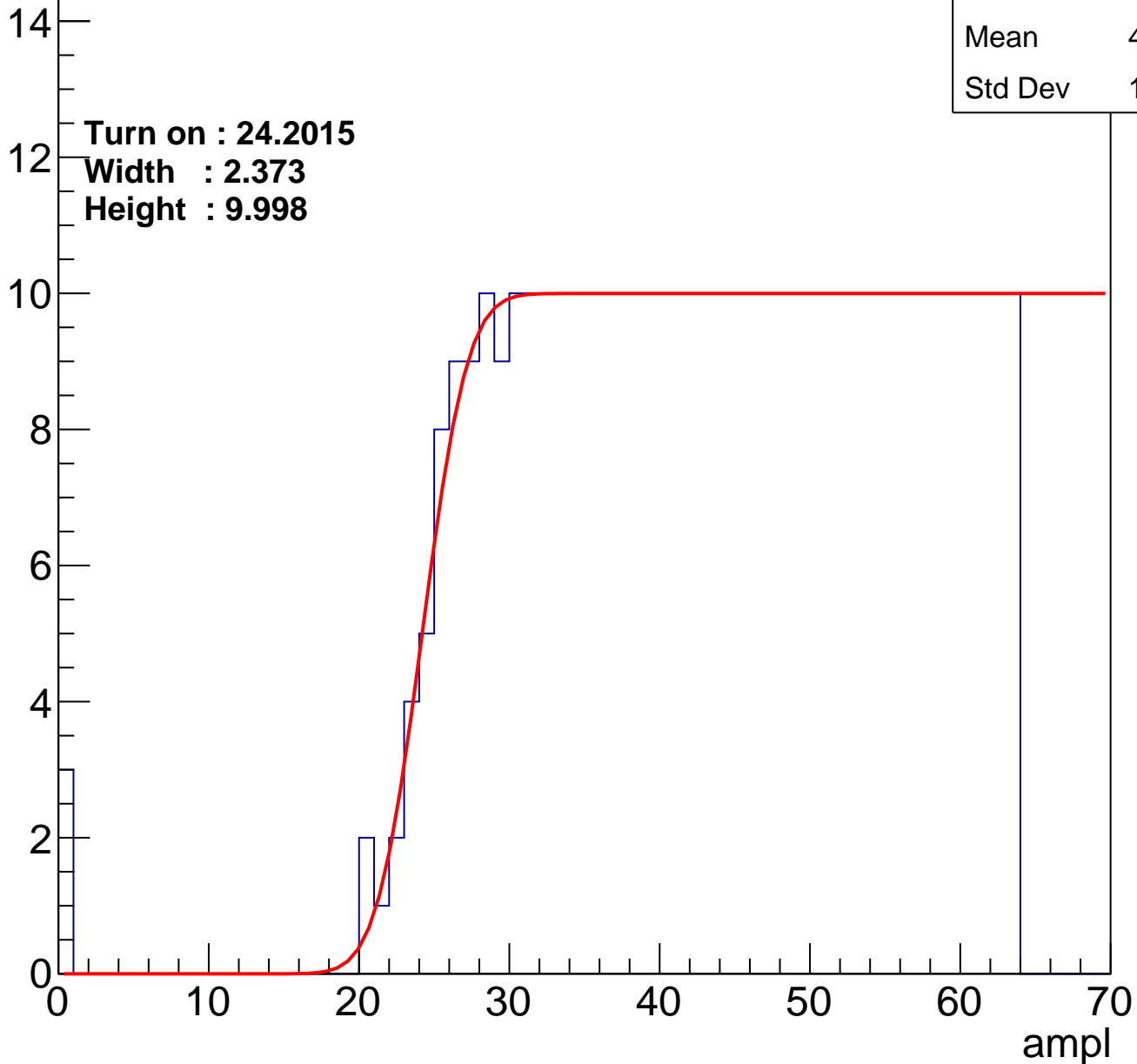
Entries	402
Mean	43.15
Std Dev	12.19

Turn on : 24.2015

Width : 2.373

Height : 9.998

Entry



B1L102S, U3-ch42

calib_packv5_042523_0143.root, FC#11, port A2

Entries	378
Mean	44.36
Std Dev	11.46

Turn on : 26.2413

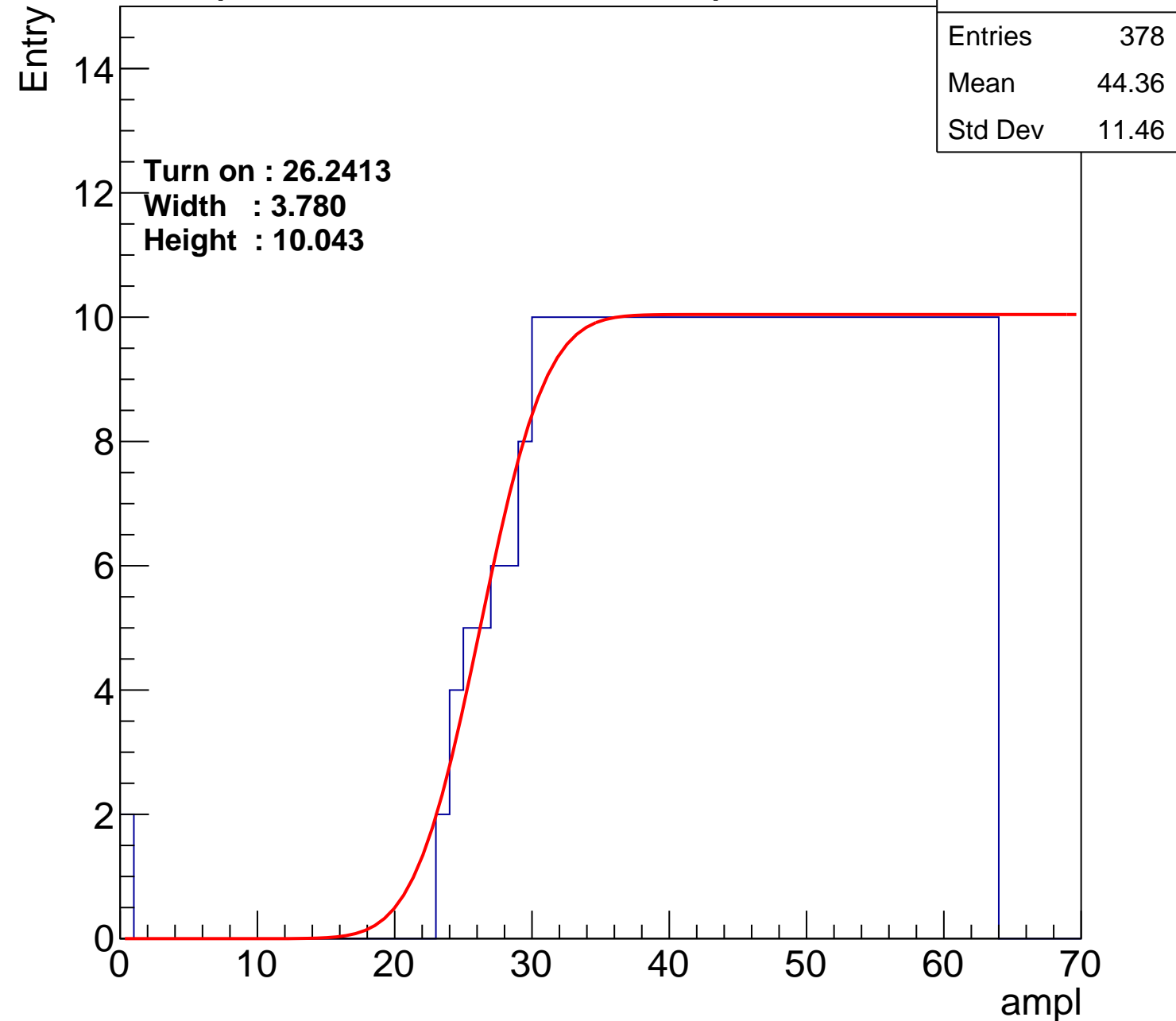
Width : 3.780

Height : 10.043

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch43

calib_packv5_042523_0143.root, FC#11, port A2

Entries	403
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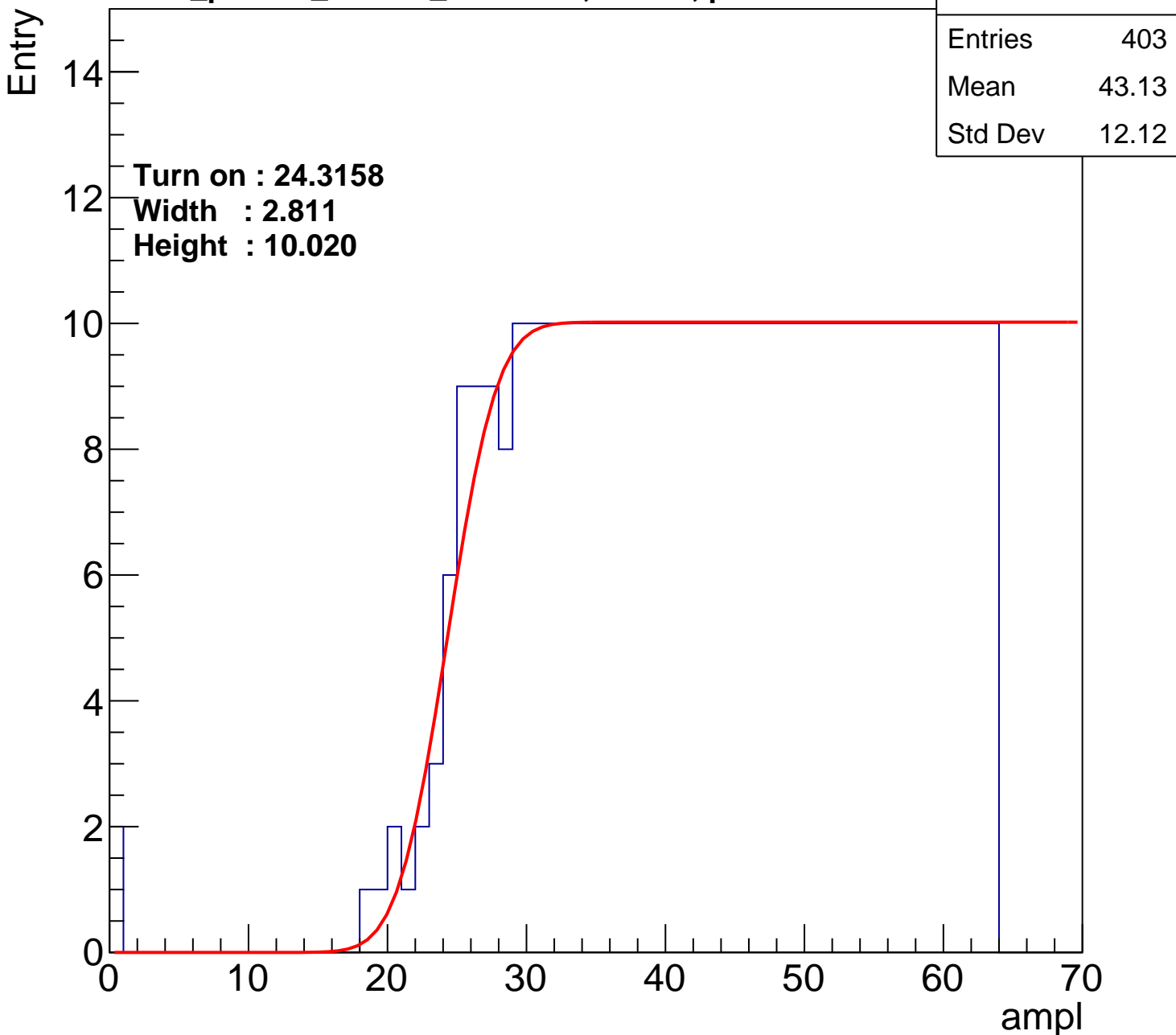
Mean	43.13
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Std Dev	12.12
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Turn on : 24.3158

Width : 2.811

Height : 10.020



B1L102S, U3-ch44

calib_packv5_042523_0143.root, FC#11, port A2

Entries	380
Mean	44.18
Std Dev	11.72

Turn on : 26.5517

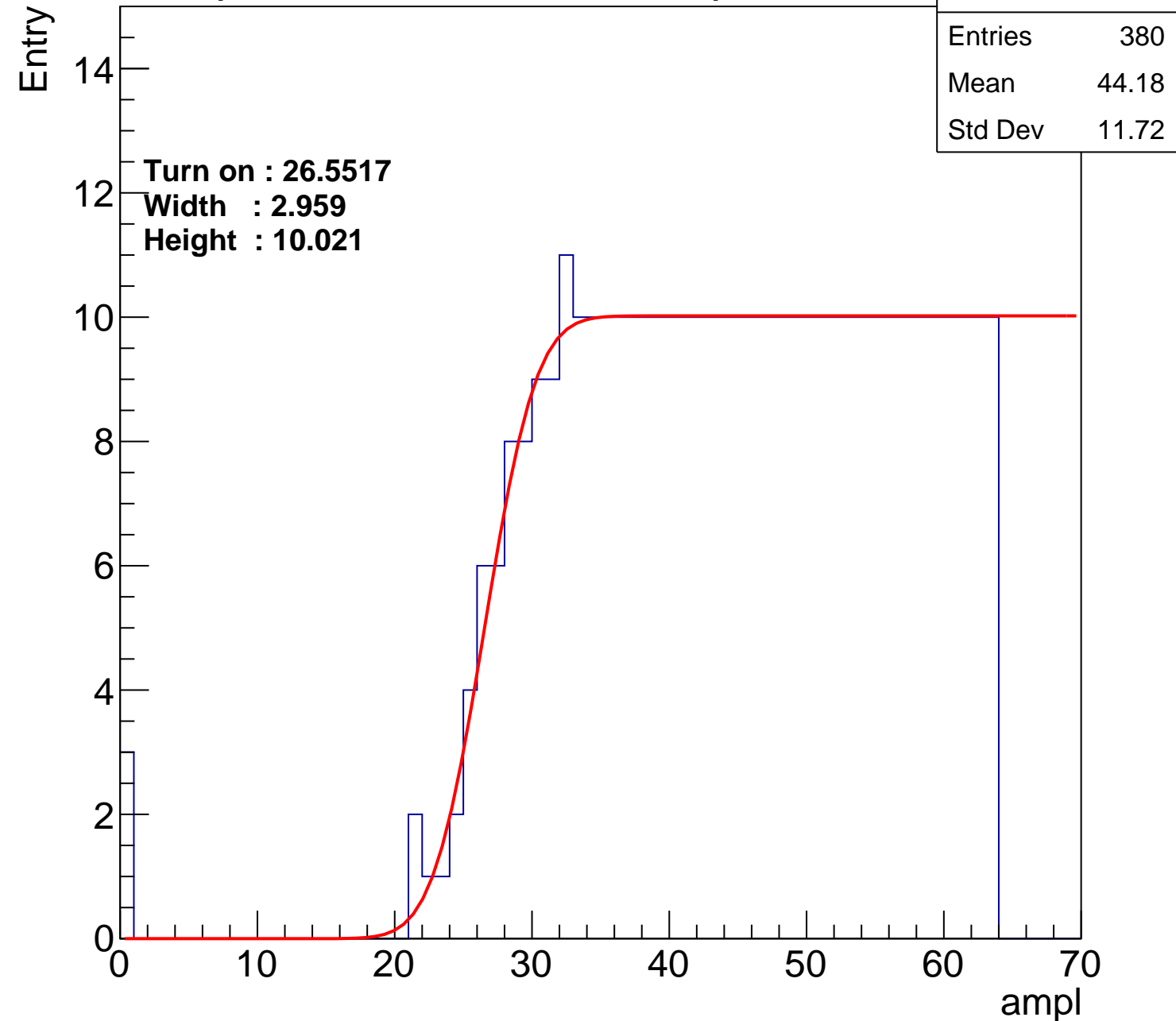
Width : 2.959

Height : 10.021

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch45

calib_packv5_042523_0143.root, FC#11, port A2

Entries	378
Mean	44.24
Std Dev	11.81

Turn on : 26.9809

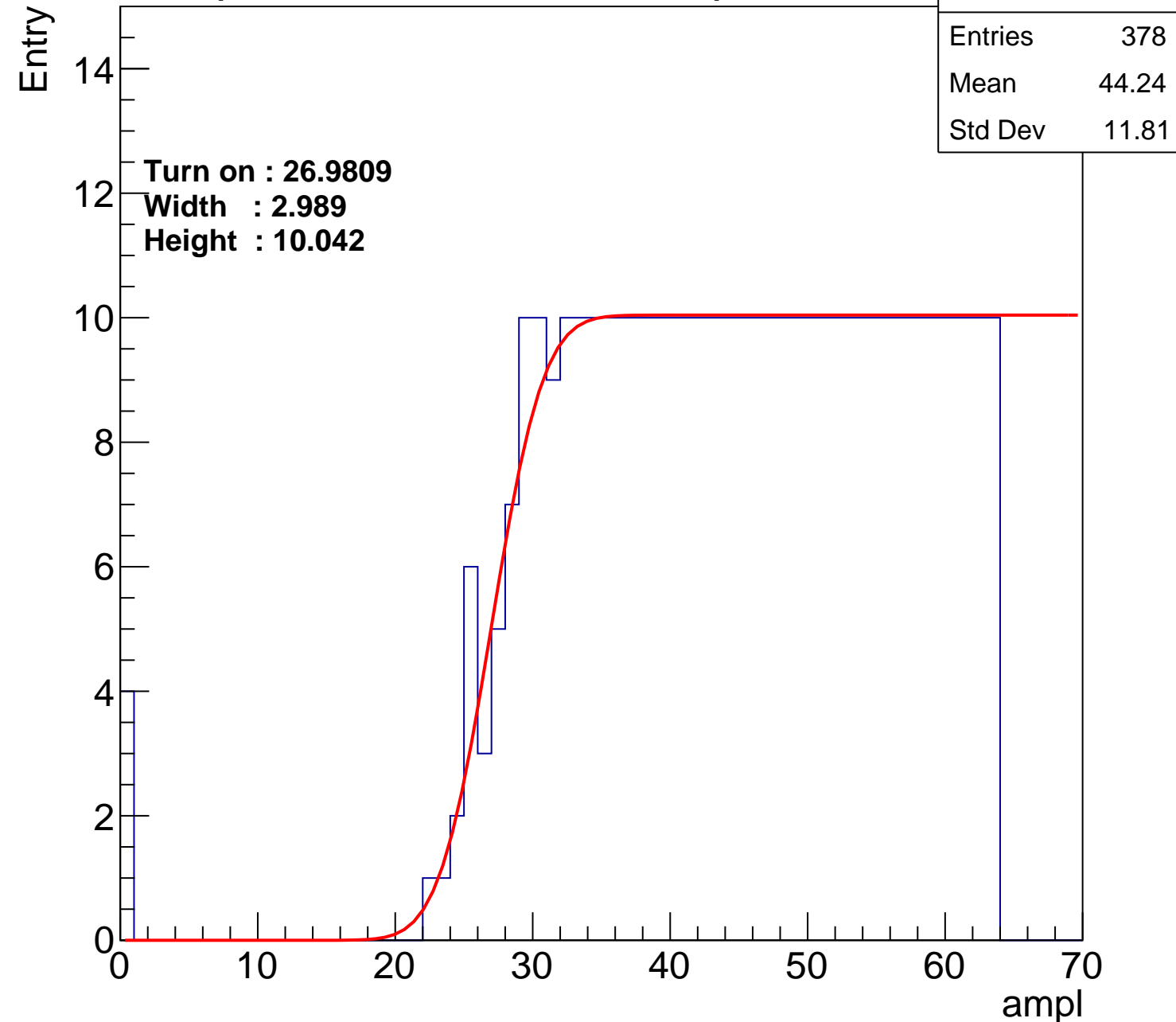
Width : 2.989

Height : 10.042

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch46

calib_packv5_042523_0143.root, FC#11, port A2

Entries	402
Mean	43.22
Std Dev	12.02

Turn on : 24.2522

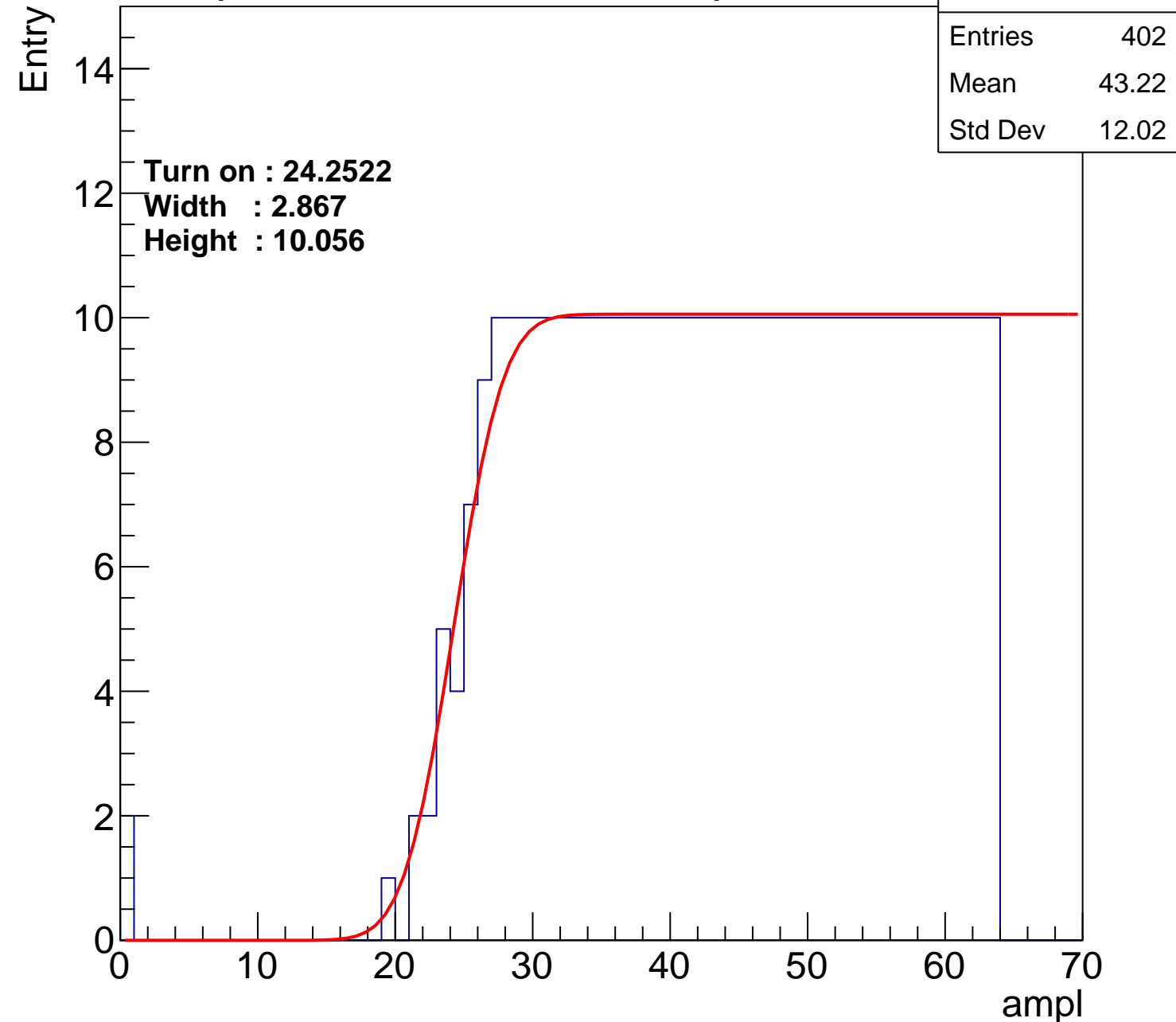
Width : 2.867

Height : 10.056

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch47

calib_packv5_042523_0143.root, FC#11, port A2

Entries	391
Mean	43.66
Std Dev	11.9

Turn on : 25.2528

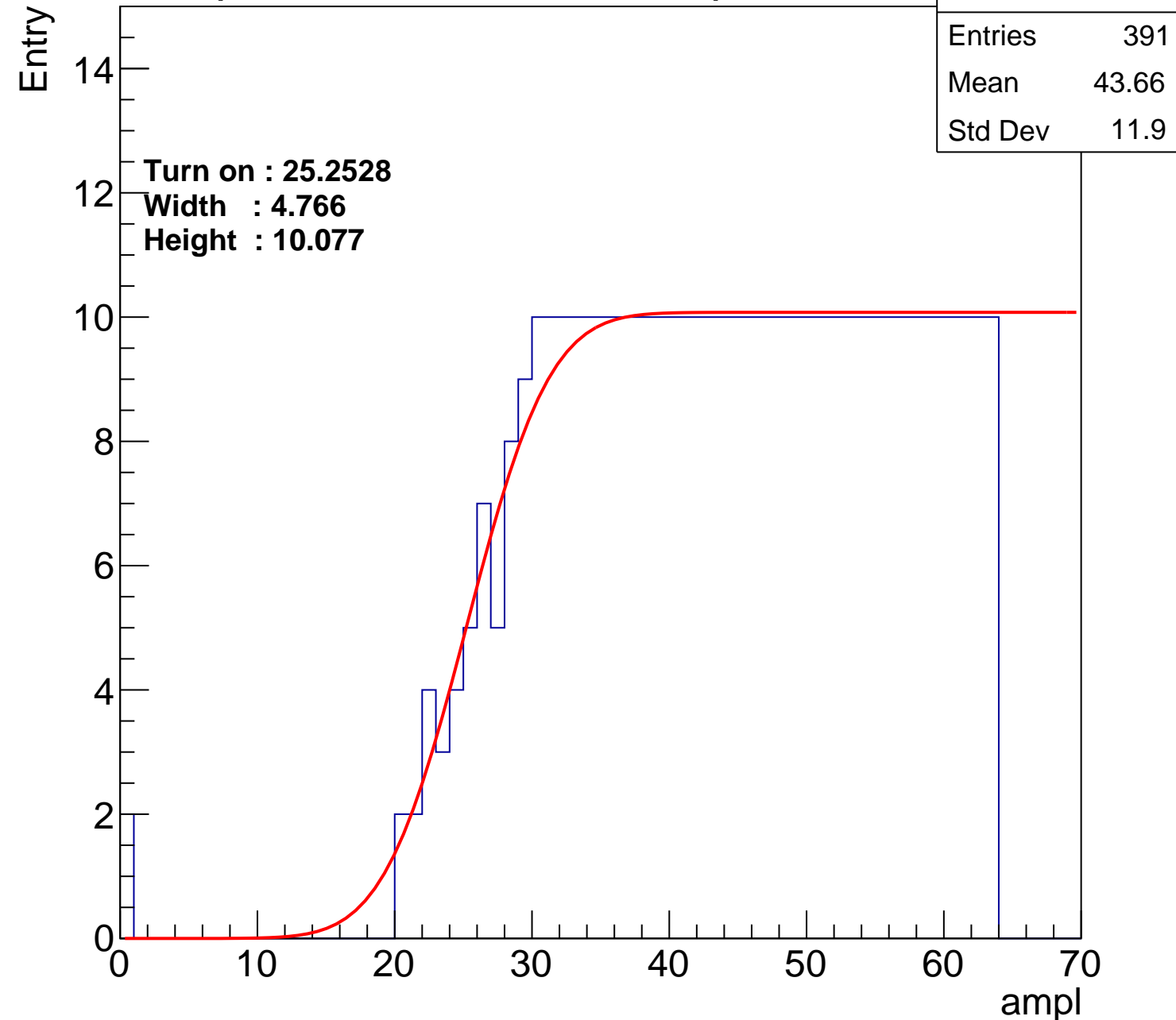
Width : 4.766

Height : 10.077

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch48

calib_packv5_042523_0143.root, FC#11, port A2

Entries	379
Mean	44.18
Std Dev	11.78

Turn on : 26.8207

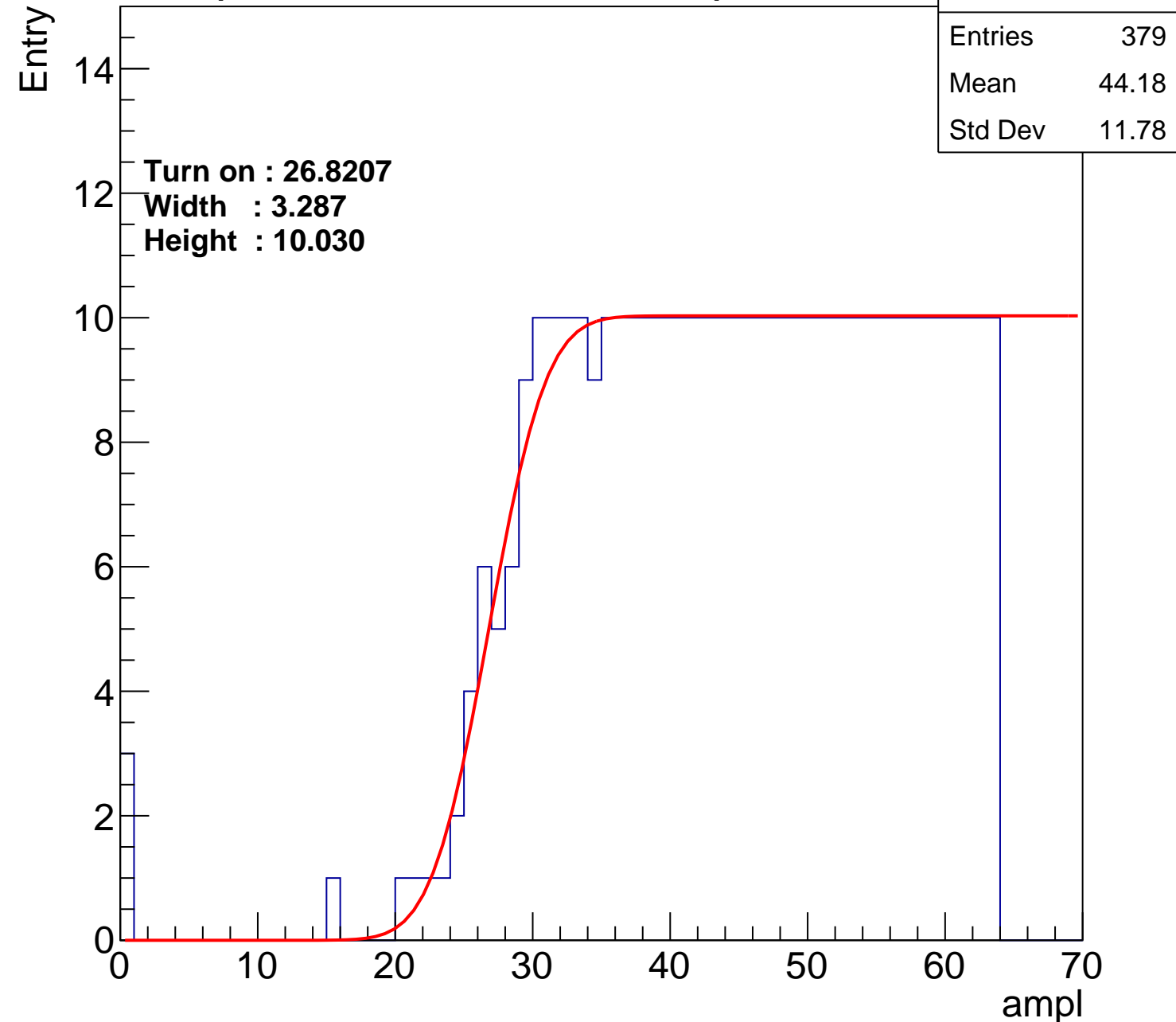
Width : 3.287

Height : 10.030

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch49

calib_packv5_042523_0143.root, FC#11, port A2

Entries	376
Mean	44.43
Std Dev	11.46

Turn on : 26.8419

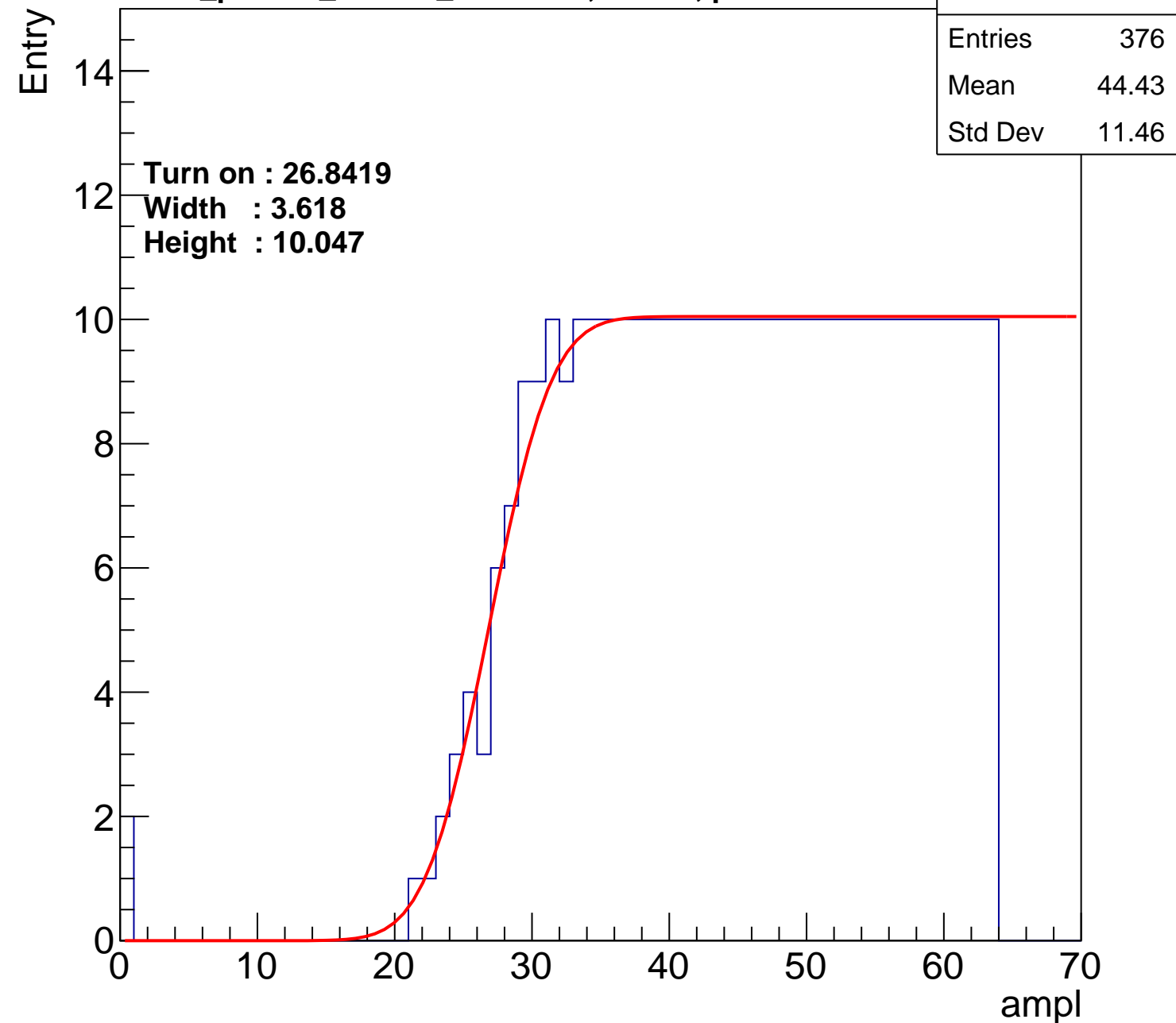
Width : 3.618

Height : 10.047

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch50

calib_packv5_042523_0143.root, FC#11, port A2

Entries	393
Mean	43.49
Std Dev	12.12

Turn on : 24.8307

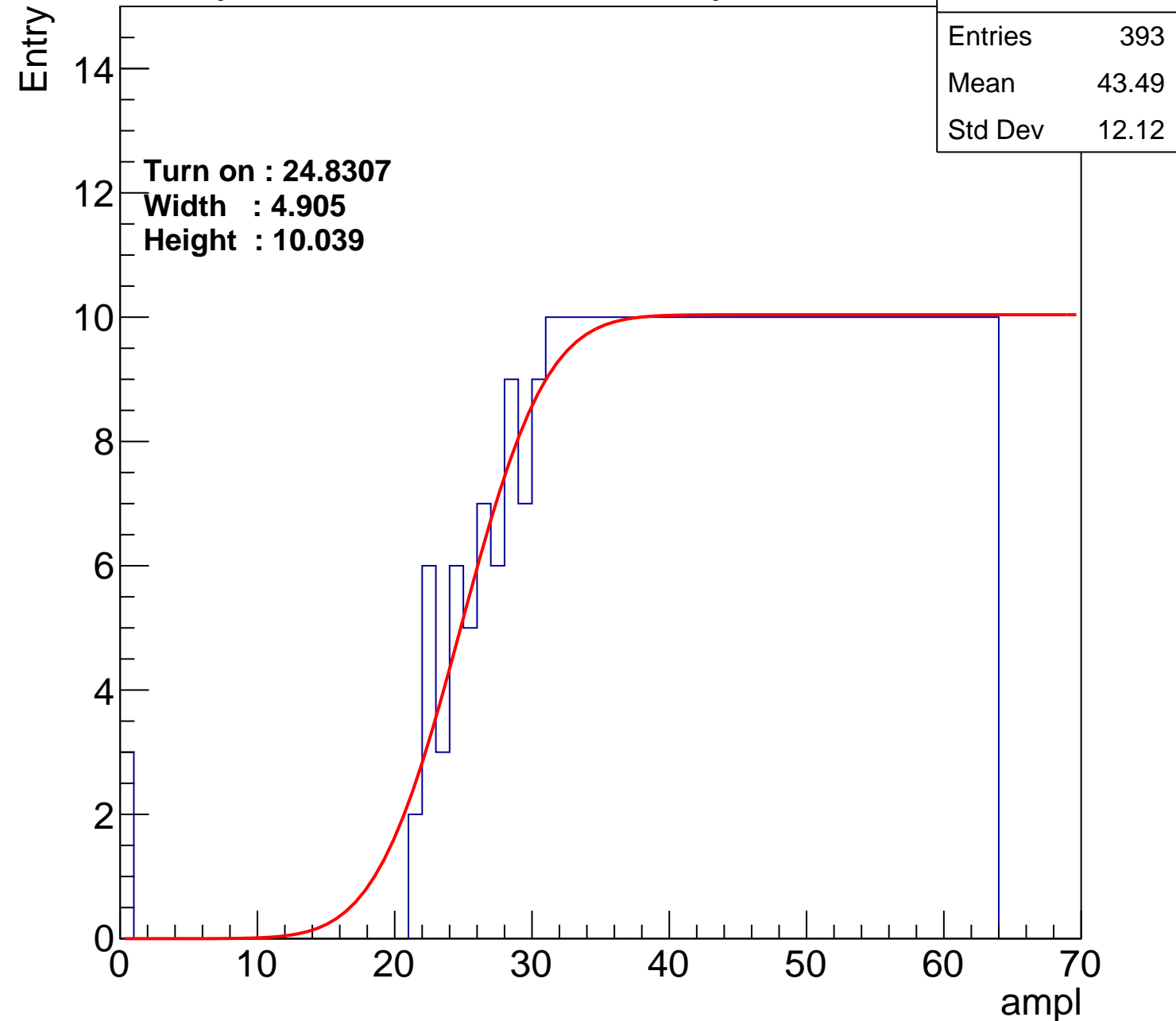
Width : 4.905

Height : 10.039

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch51

calib_packv5_042523_0143.root, FC#11, port A2

Entries	377
Mean	44.46
Std Dev	11.28

Turn on : 26.7282

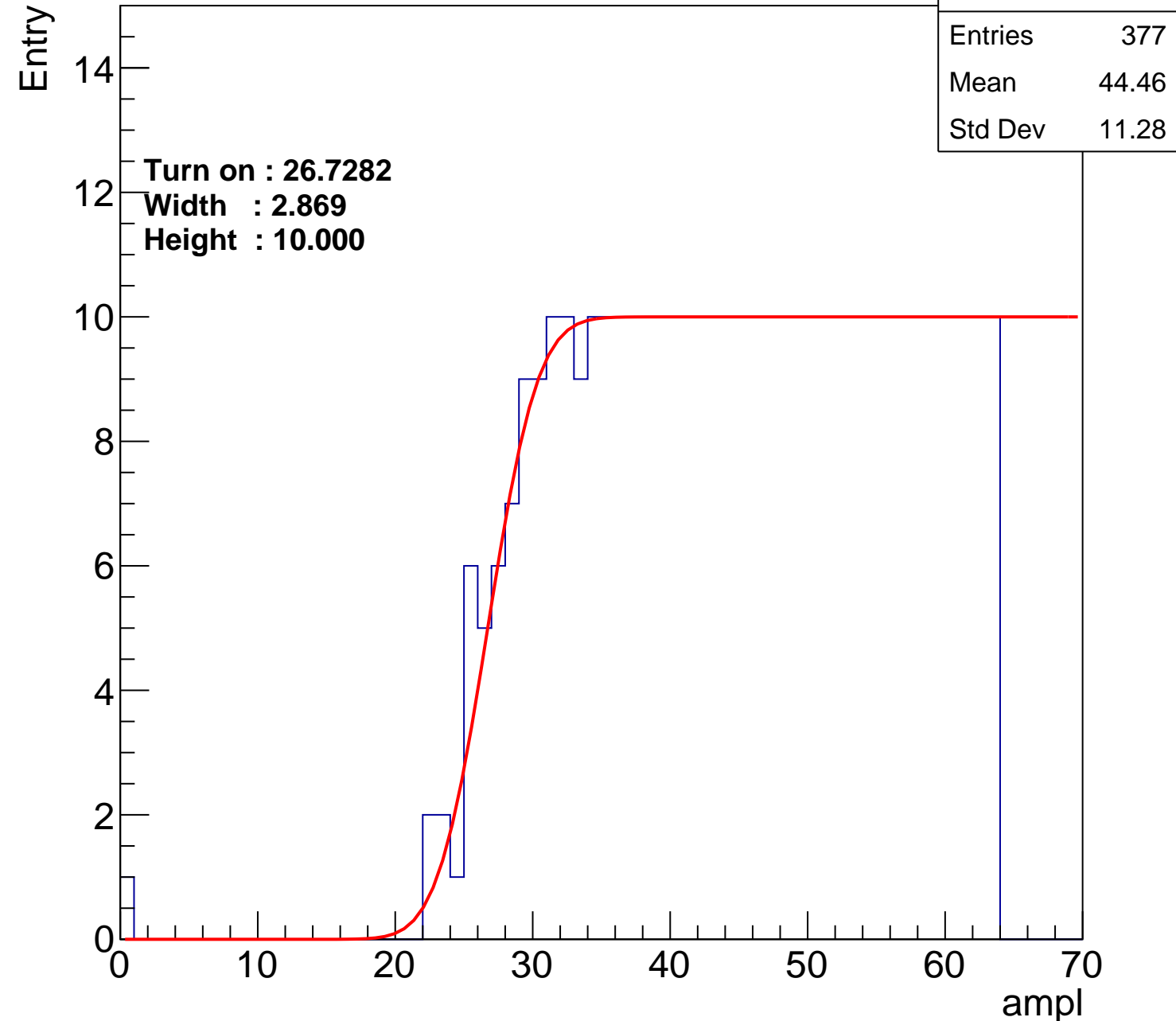
Width : 2.869

Height : 10.000

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch52

calib_packv5_042523_0143.root, FC#11, port A2

Entries	402
Mean	43.05
Std Dev	12.39

Turn on : 24.3310

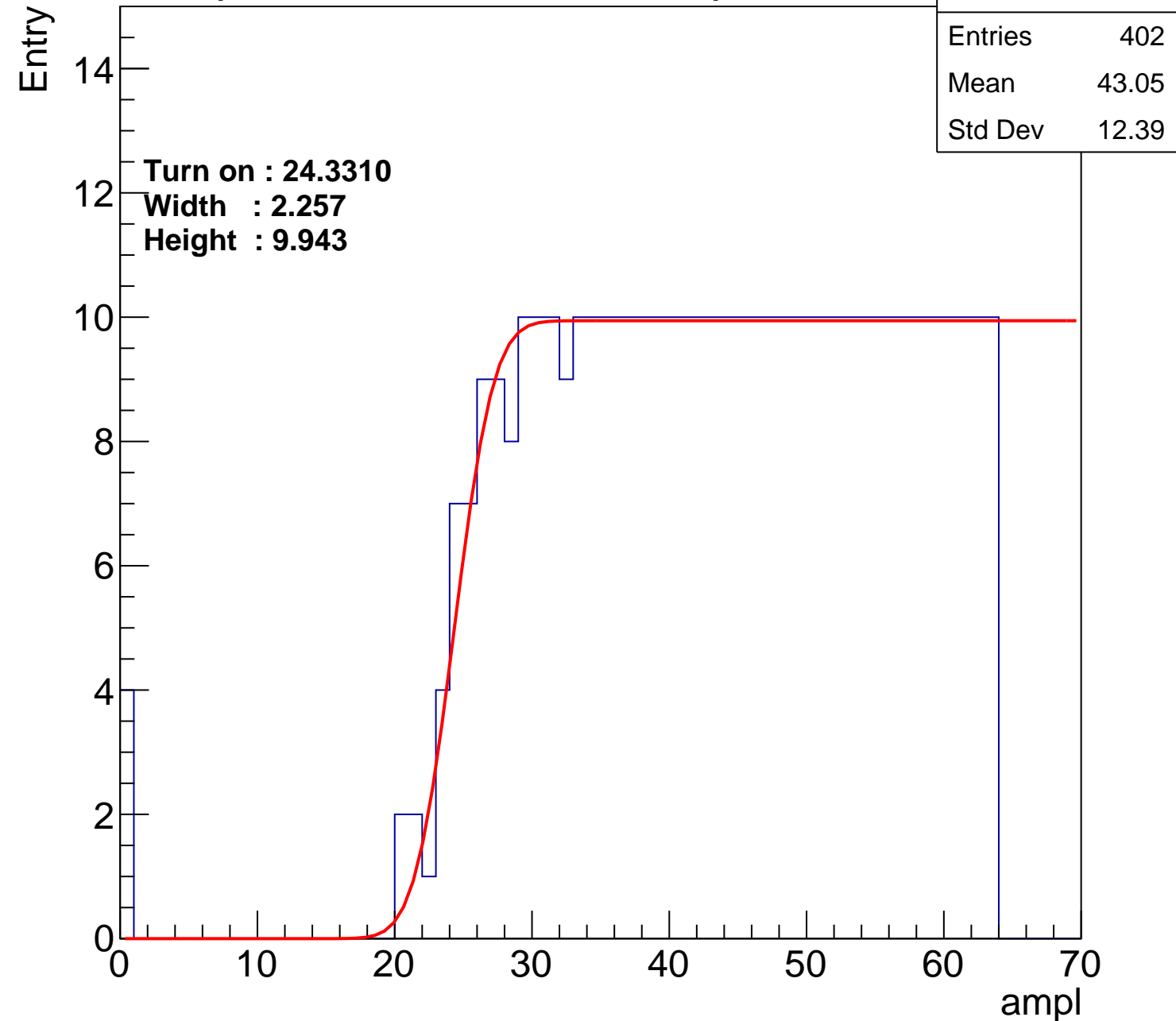
Width : 2.257

Height : 9.943

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch53

calib_packv5_042523_0143.root, FC#11, port A2

Entries	393
Mean	43.63
Std Dev	11.83

Turn on : 25.0414

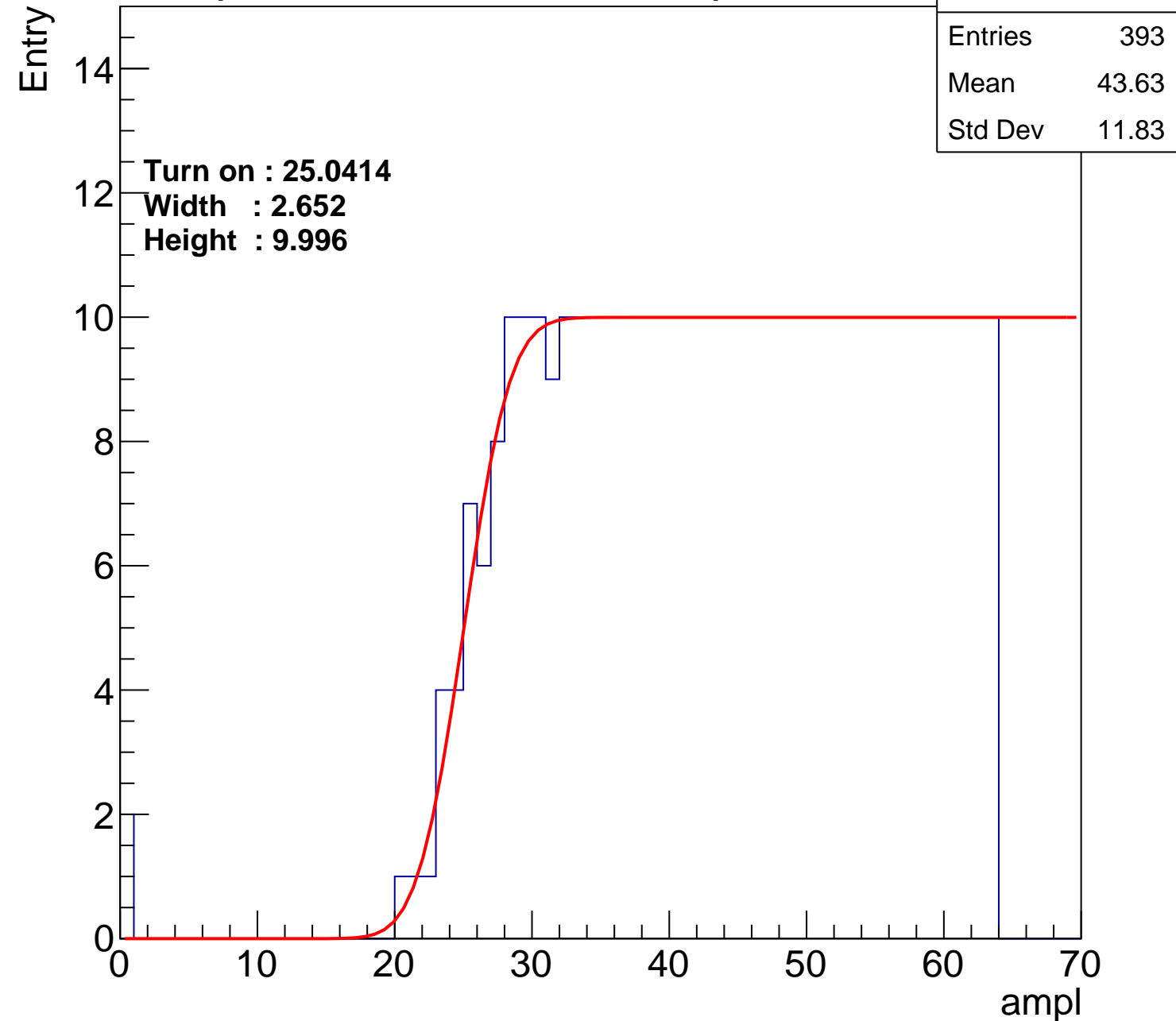
Width : 2.652

Height : 9.996

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch54

calib_packv5_042523_0143.root, FC#11, port A2

Entries	410
Mean	42.59
Std Dev	12.68

Turn on : 23.1120

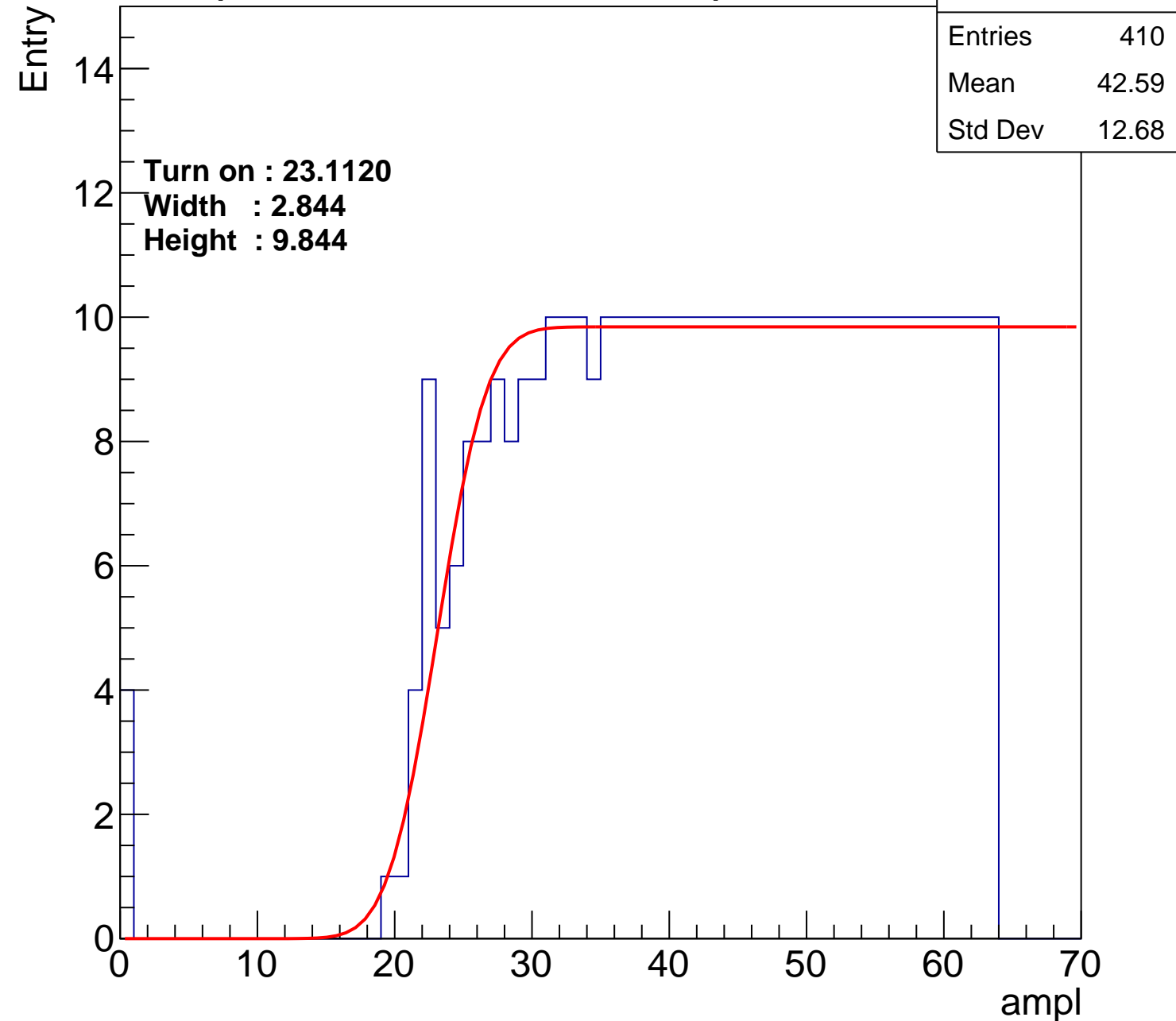
Width : 2.844

Height : 9.844

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch55

calib_packv5_042523_0143.root, FC#11, port A2

Entries	391
Mean	43.57
Std Dev	12.16

Turn on : 25.6473

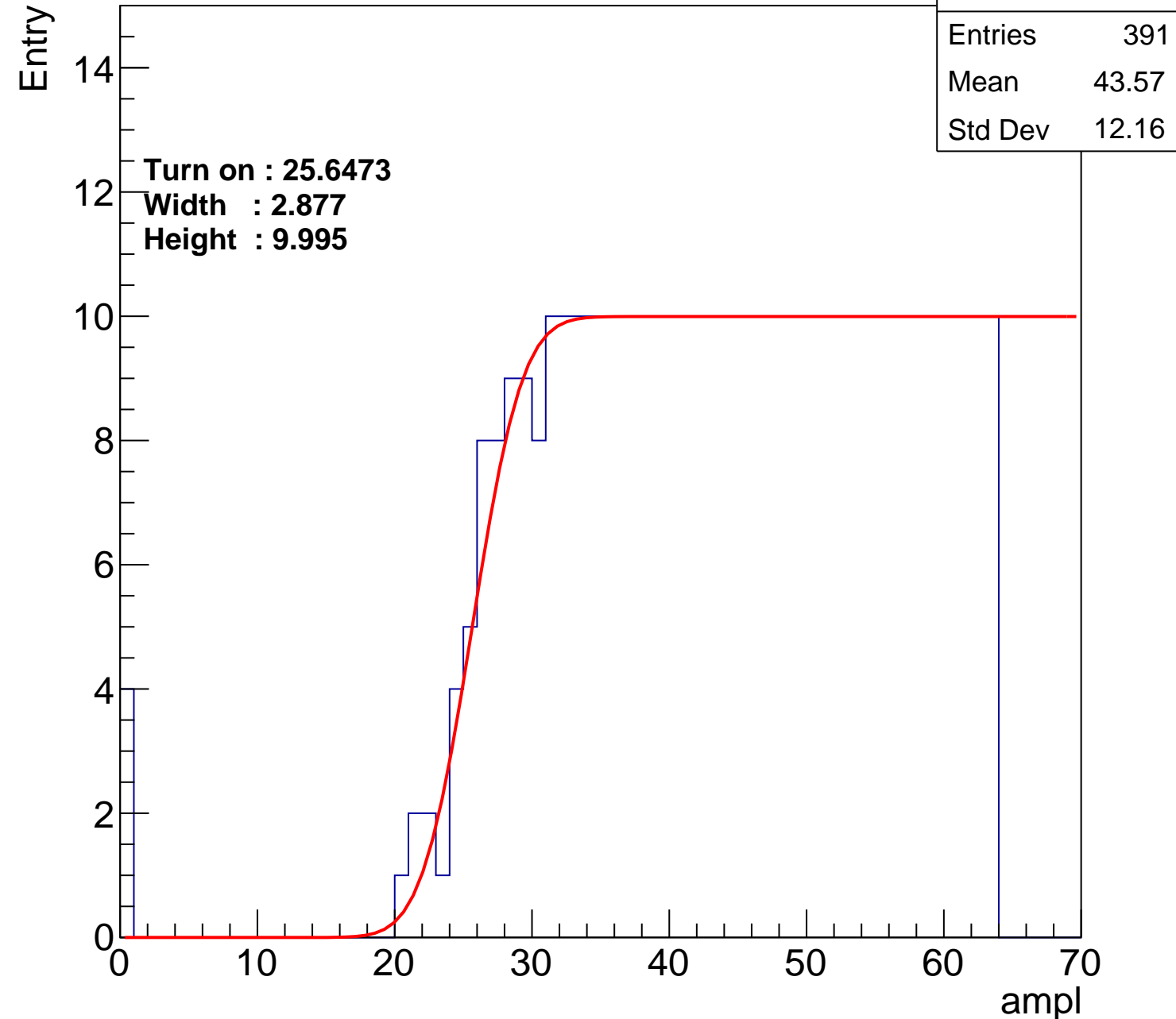
Width : 2.877

Height : 9.995

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch56

calib_packv5_042523_0143.root, FC#11, port A2

Entries	397
Mean	43.49
Std Dev	11.79

Turn on : 24.3971

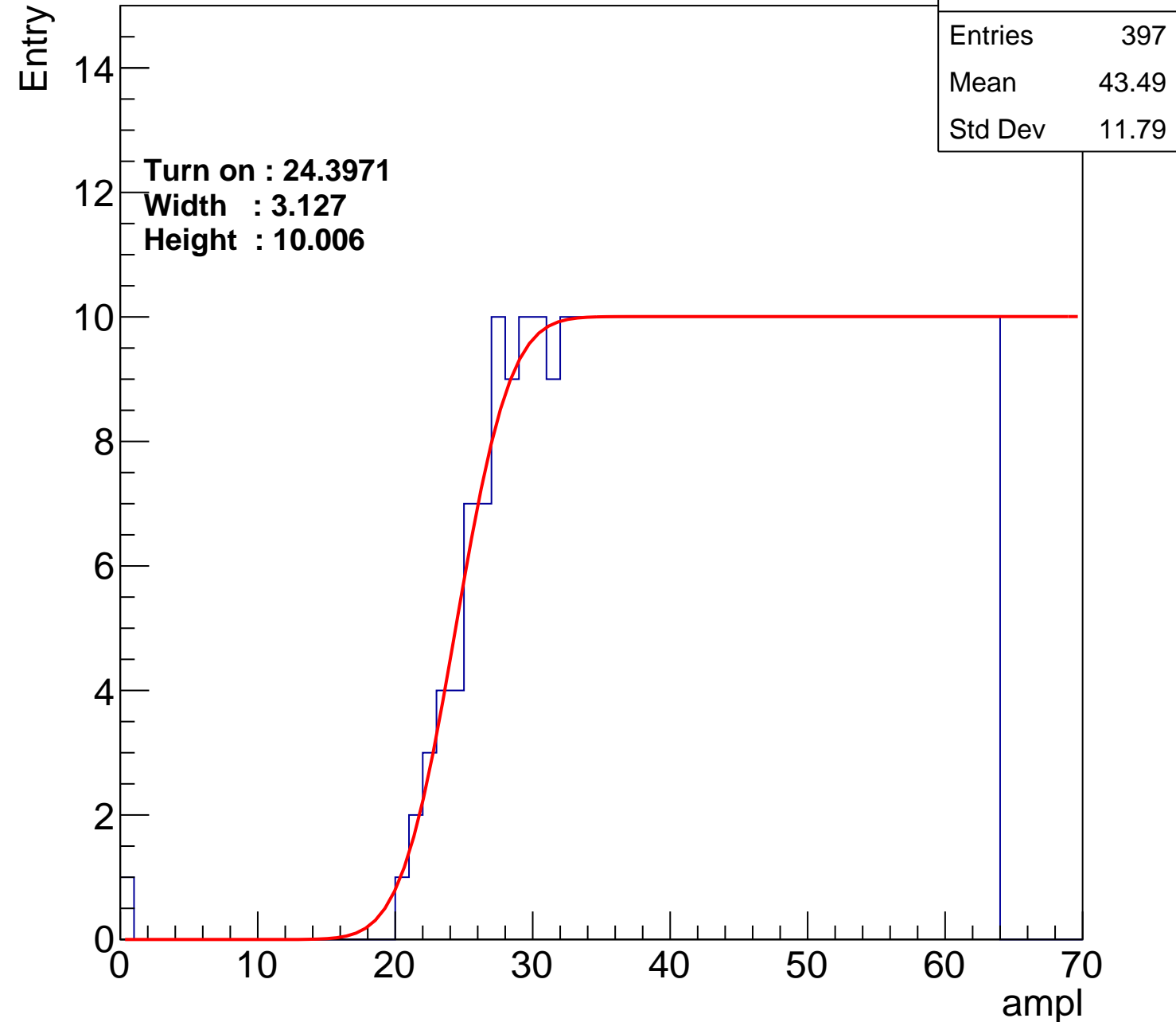
Width : 3.127

Height : 10.006

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch57

calib_packv5_042523_0143.root, FC#11, port A2

Entries	380
Mean	44.14
Std Dev	11.86

Turn on : 26.9918

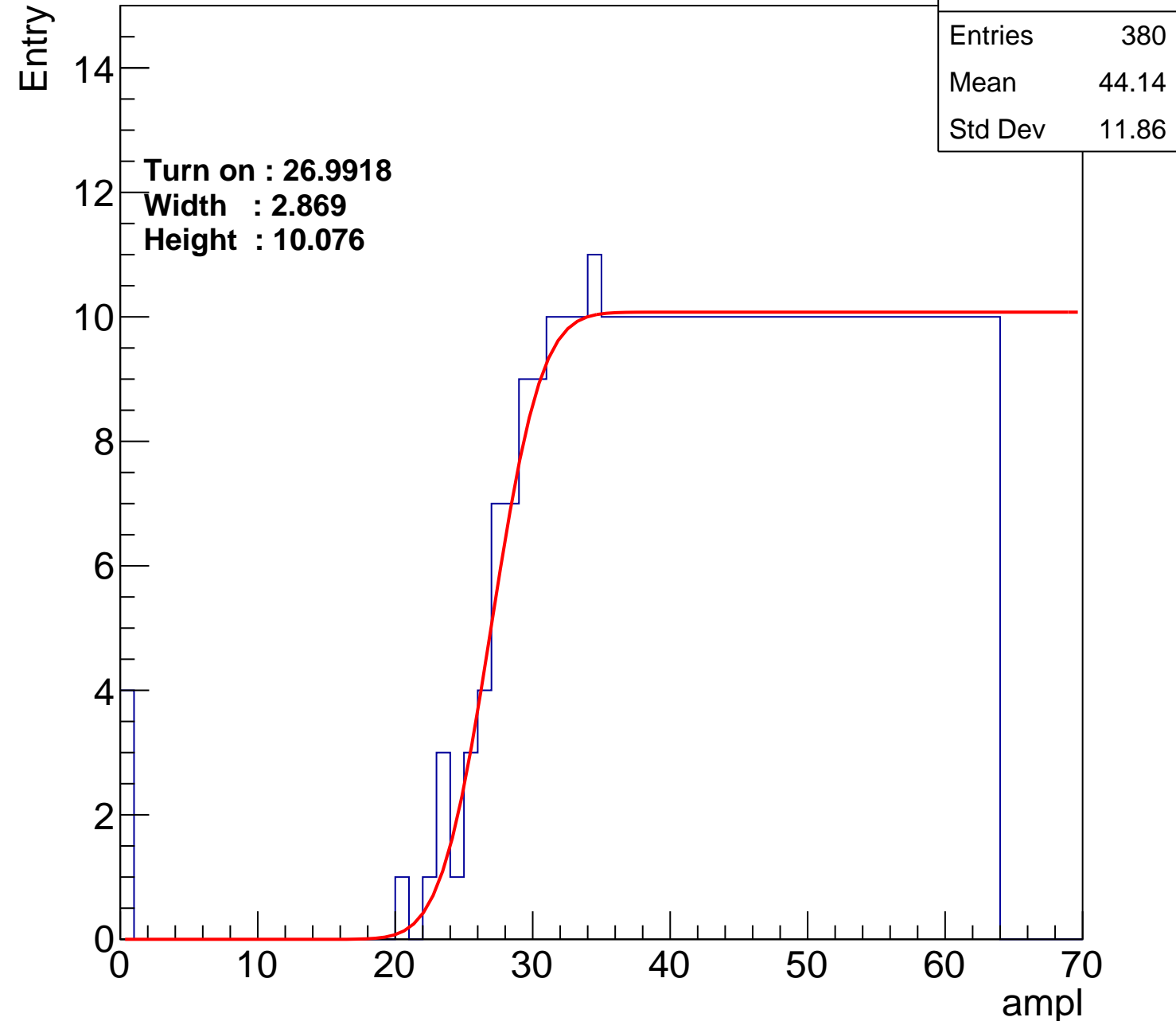
Width : 2.869

Height : 10.076

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch58

calib_packv5_042523_0143.root, FC#11, port A2

Entries	397
Mean	43.23
Std Dev	12.39

Turn on : 25.4469

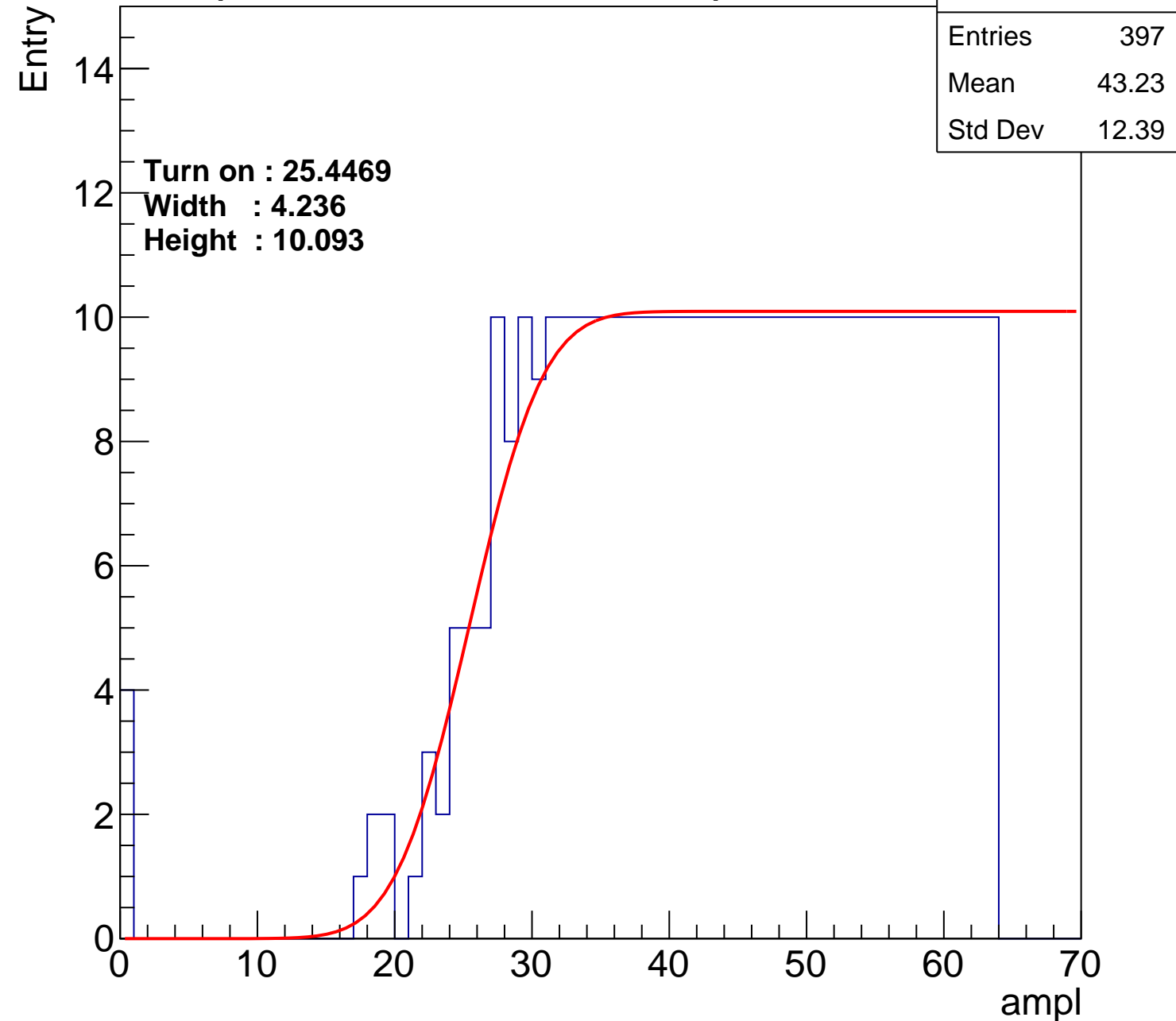
Width : 4.236

Height : 10.093

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch59

calib_packv5_042523_0143.root, FC#11, port A2

Entries	383
Mean	44.04
Std Dev	11.78

Turn on : 26.3256

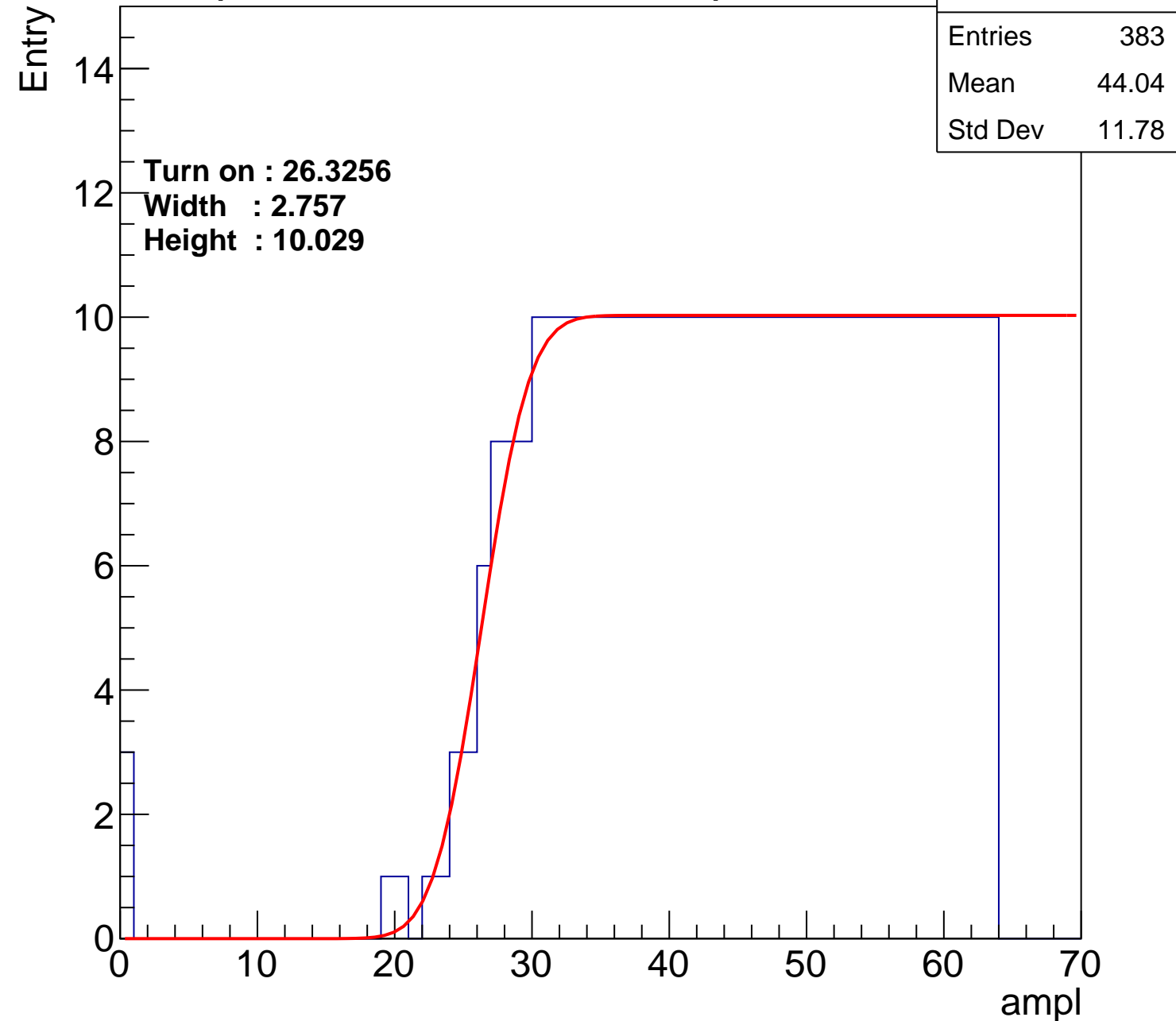
Width : 2.757

Height : 10.029

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch60

calib_packv5_042523_0143.root, FC#11, port A2

Entries	392
Mean	43.67
Std Dev	11.83

Turn on : 24.8679

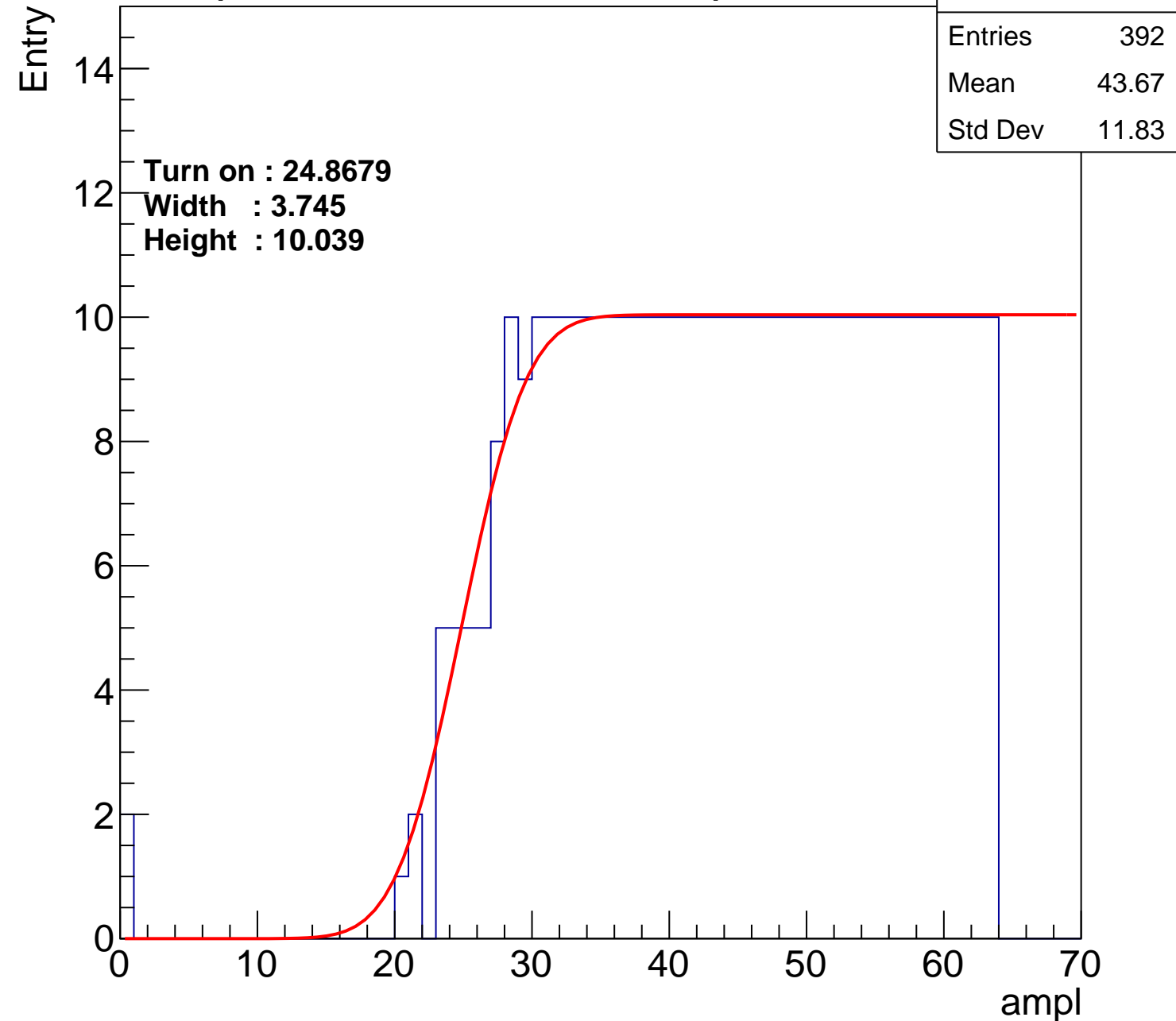
Width : 3.745

Height : 10.039

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch61

calib_packv5_042523_0143.root, FC#11, port A2

Entries	367
Mean	44.73
Std Dev	11.62

Turn on : 27.7995

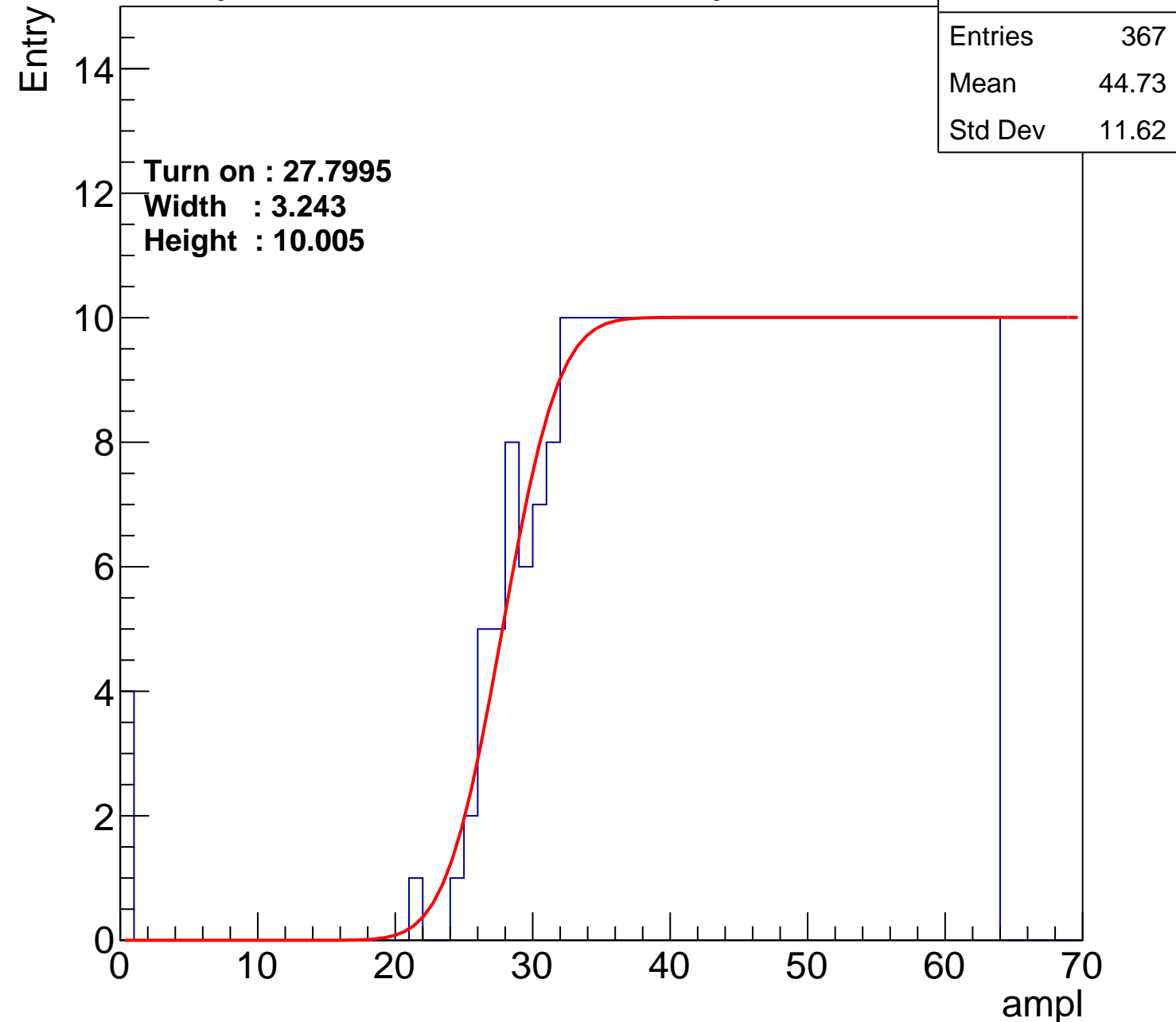
Width : 3.243

Height : 10.005

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch62

calib_packv5_042523_0143.root, FC#11, port A2

Entries	394
Mean	43.47
Std Dev	12.11

Turn on : 25.2568

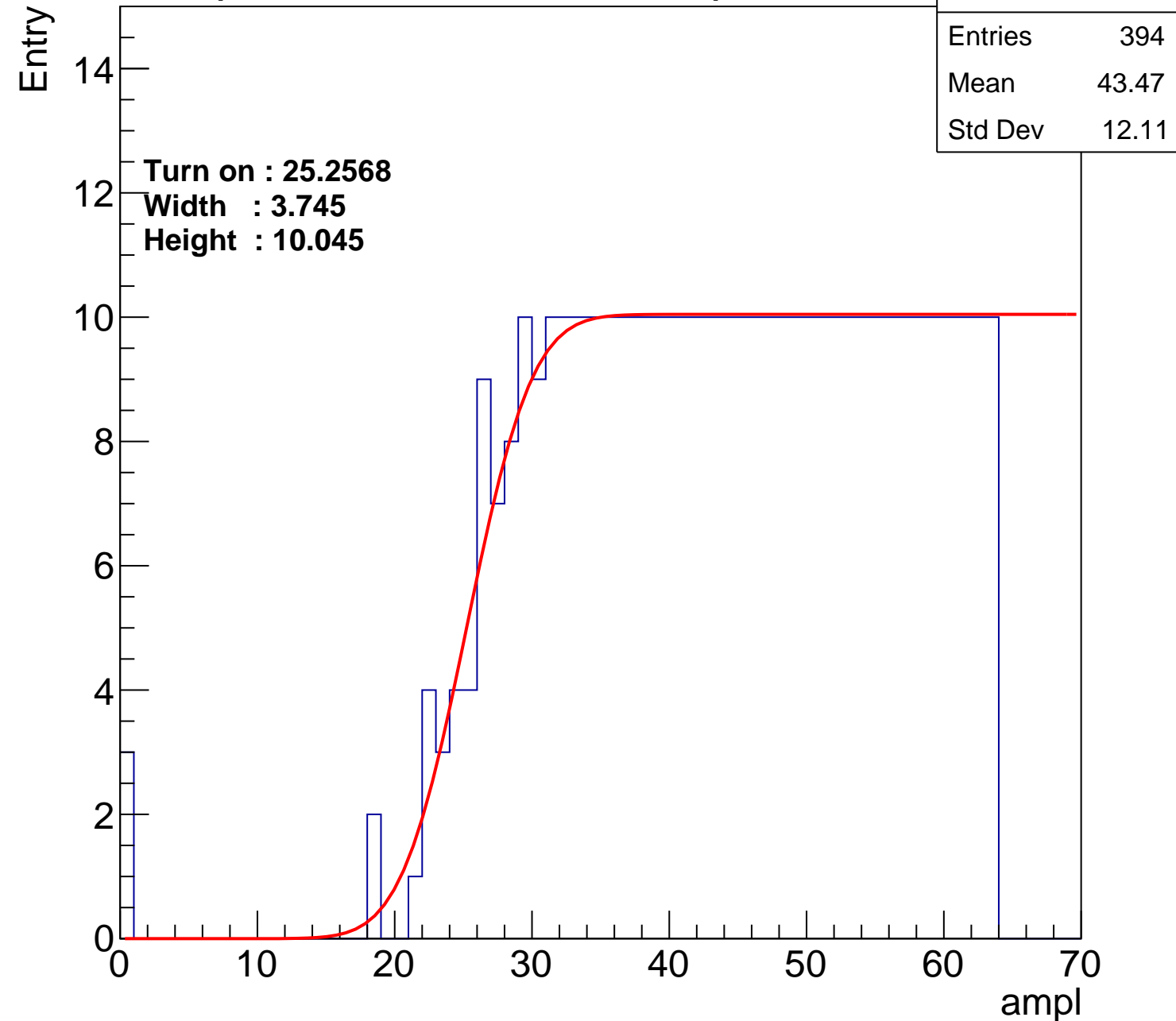
Width : 3.745

Height : 10.045

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch63

calib_packv5_042523_0143.root, FC#11, port A2

Entries	416
Mean	42.31
Std Dev	12.87

Turn on : 22.8997

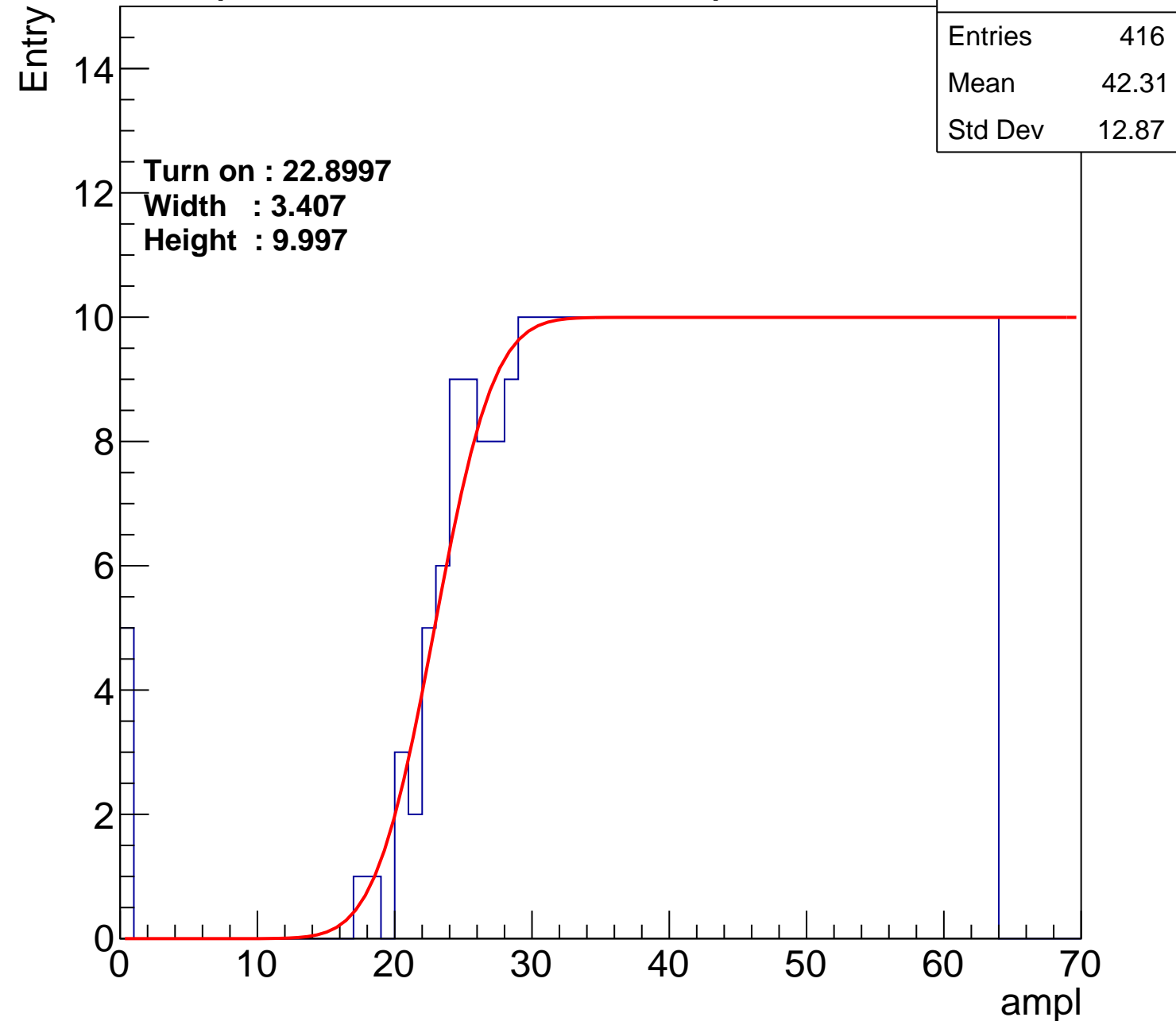
Width : 3.407

Height : 9.997

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch64

calib_packv5_042523_0143.root, FC#11, port A2

Entries	385
Mean	44.02
Std Dev	11.63

Turn on : 25.6866

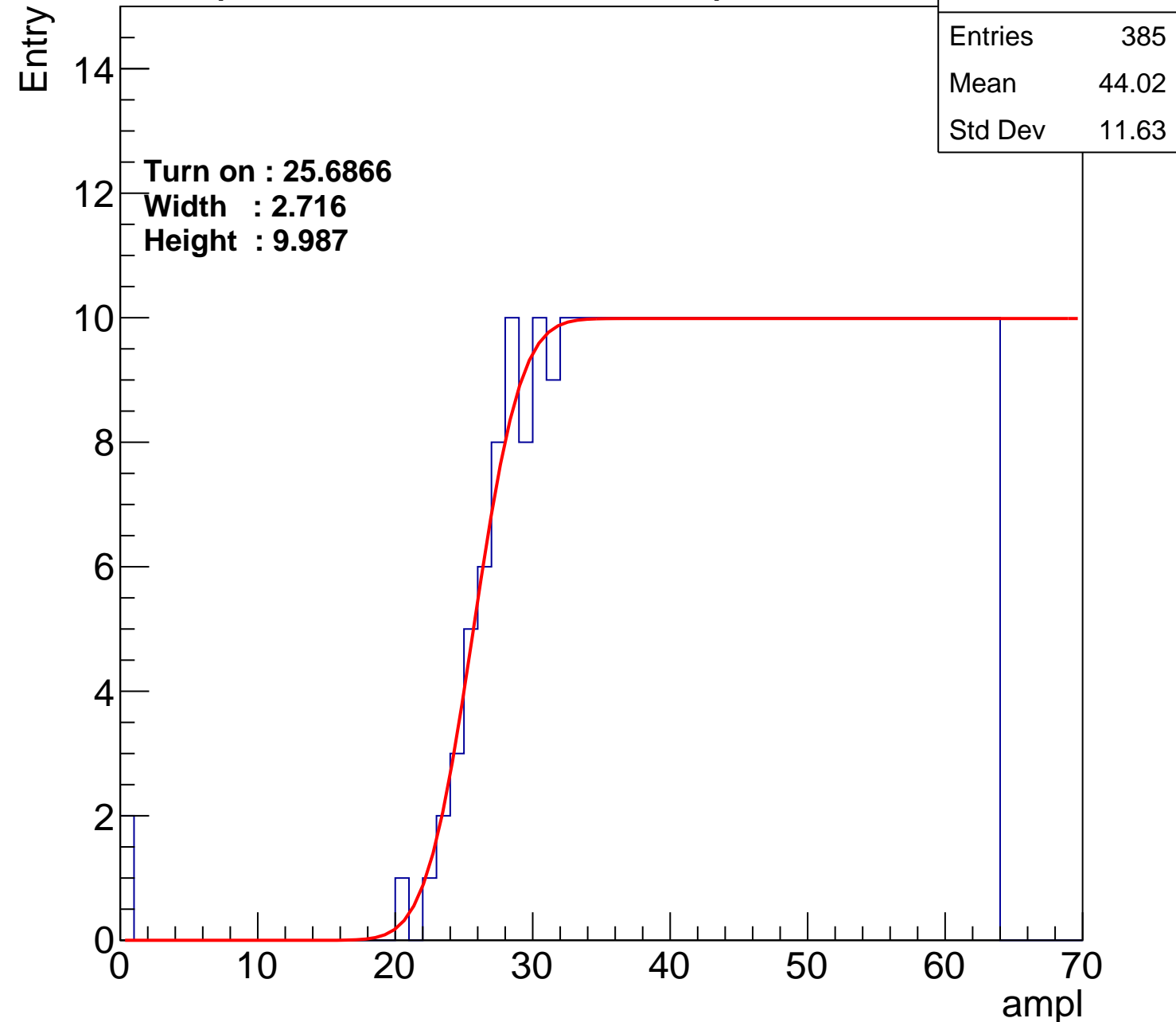
Width : 2.716

Height : 9.987

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch65

calib_packv5_042523_0143.root, FC#11, port A2

Entries	381
Mean	44.28
Std Dev	11.37

Turn on : 26.4996

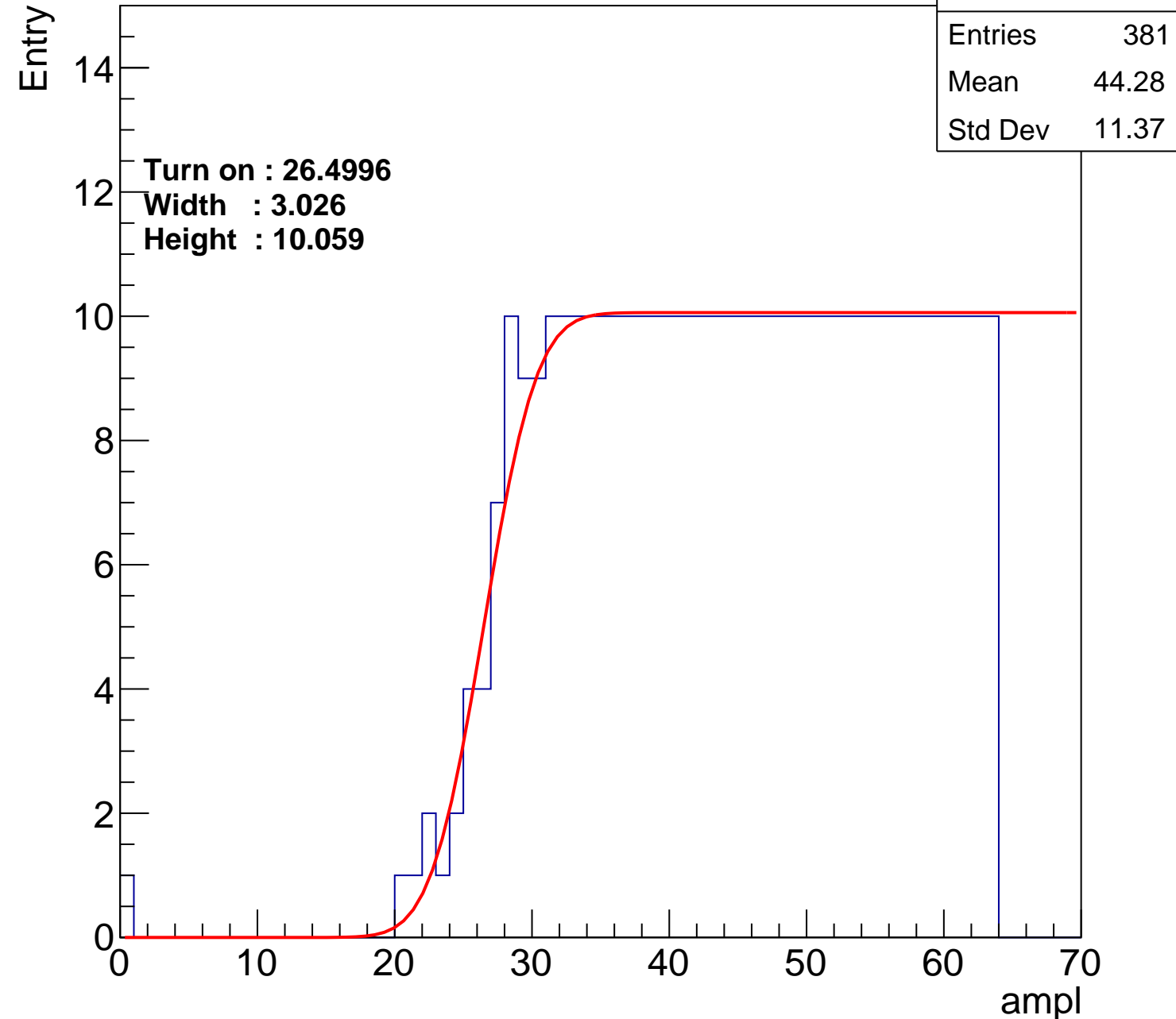
Width : 3.026

Height : 10.059

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch66

calib_packv5_042523_0143.root, FC#11, port A2

Entries	413
Mean	42.21
Std Dev	13.37

Turn on : 24.2649

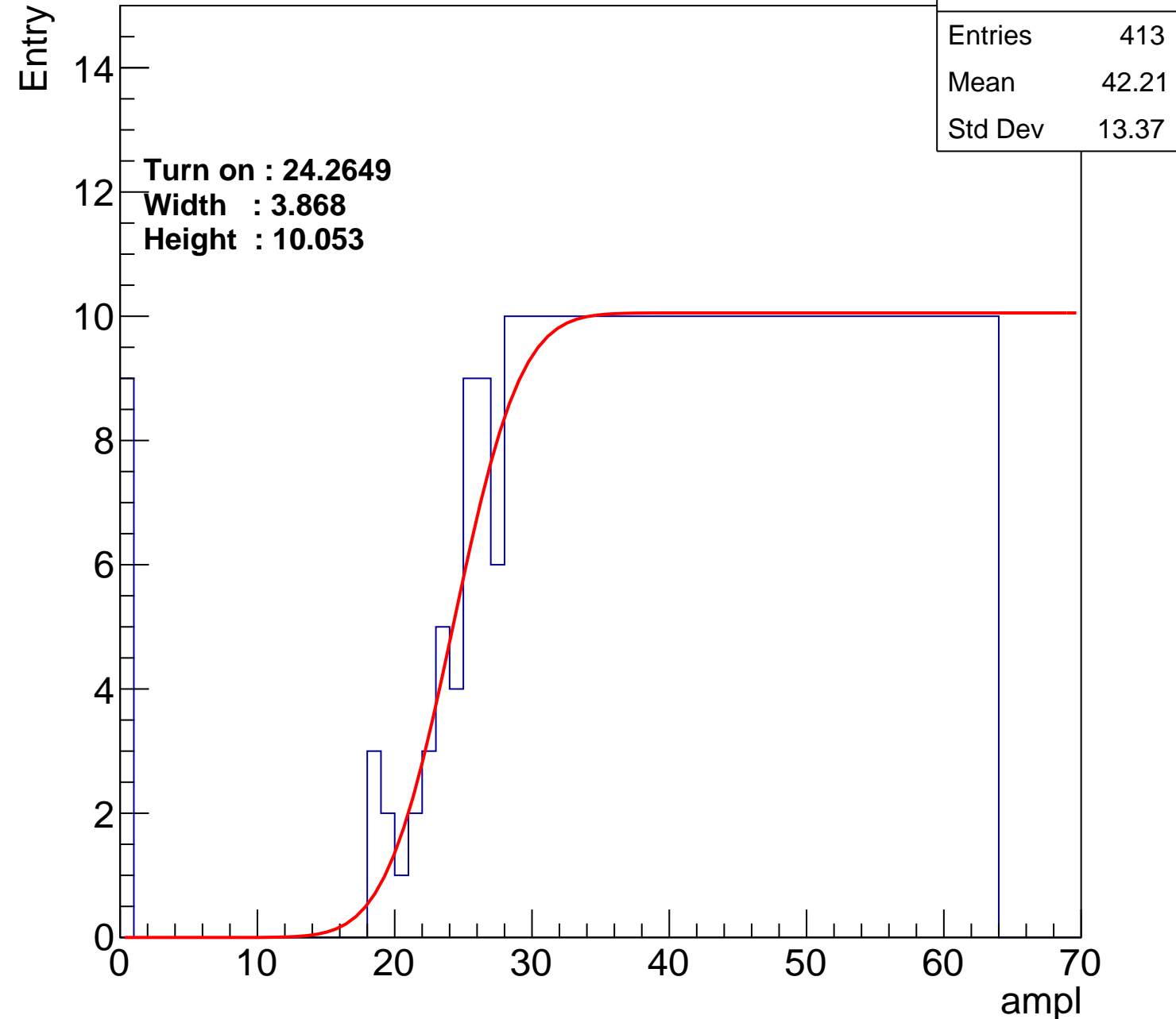
Width : 3.868

Height : 10.053

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch67

calib_packv5_042523_0143.root, FC#11, port A2

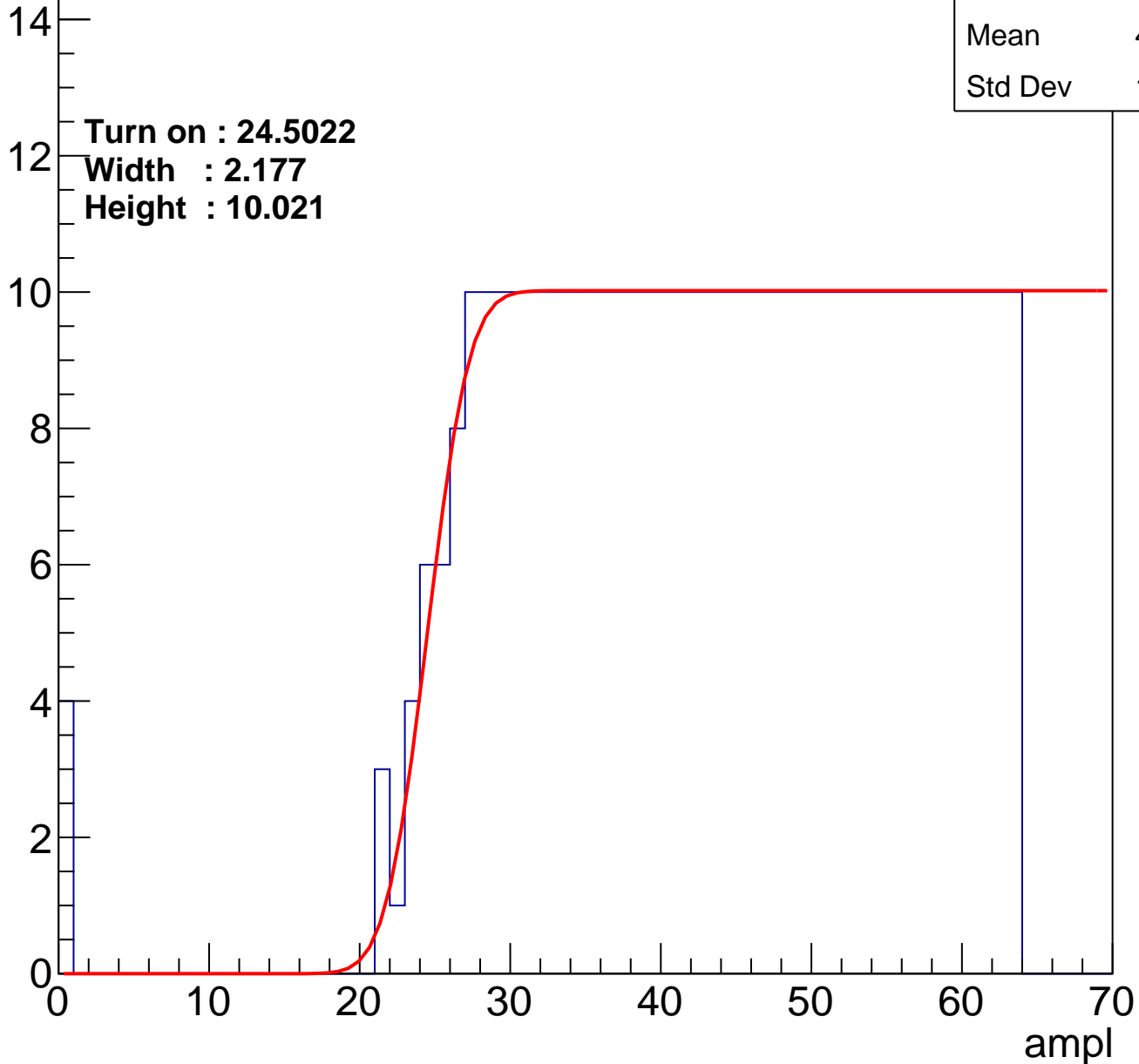
Entries	402
Mean	43.11
Std Dev	12.31

Turn on : 24.5022

Width : 2.177

Height : 10.021

Entry



B1L102S, U3-ch68

calib_packv5_042523_0143.root, FC#11, port A2

Entries	402
Mean	43.11
Std Dev	12.26

Turn on : 24.2863

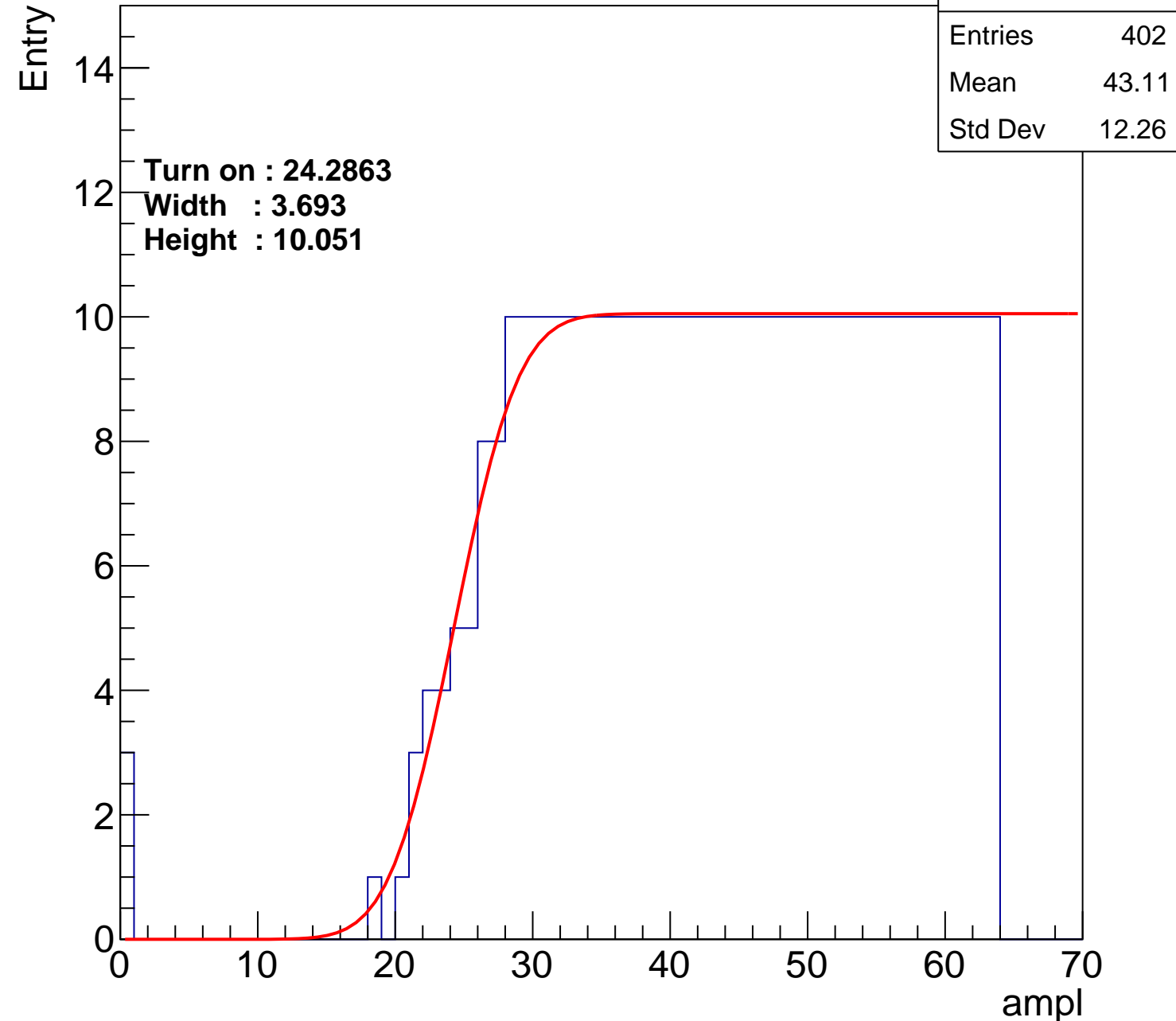
Width : 3.693

Height : 10.051

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch69

calib_packv5_042523_0143.root, FC#11, port A2

Entries	397
Mean	43.39
Std Dev	12.01

Turn on : 24.6528

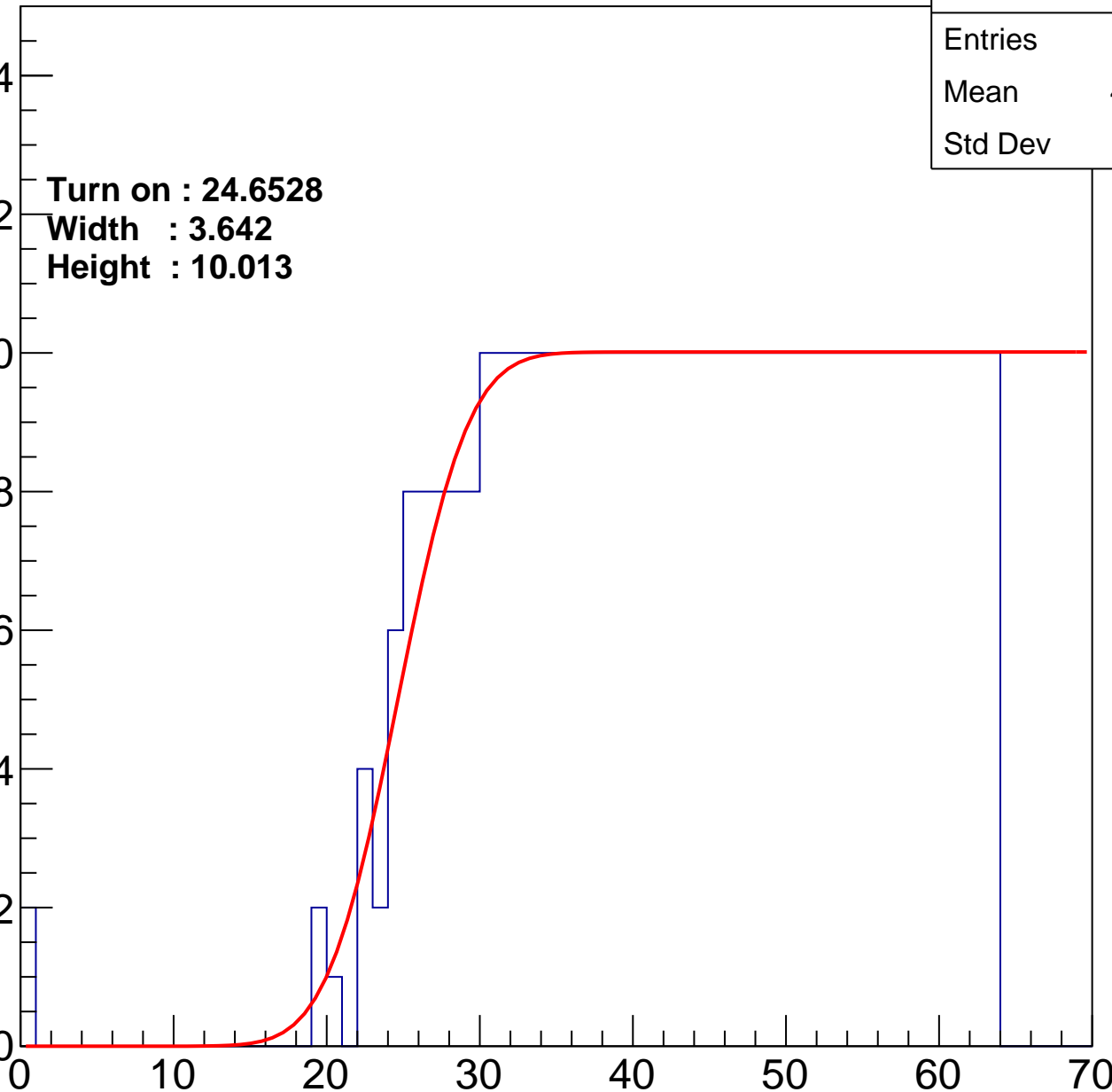
Width : 3.642

Height : 10.013

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch70

calib_packv5_042523_0143.root, FC#11, port A2

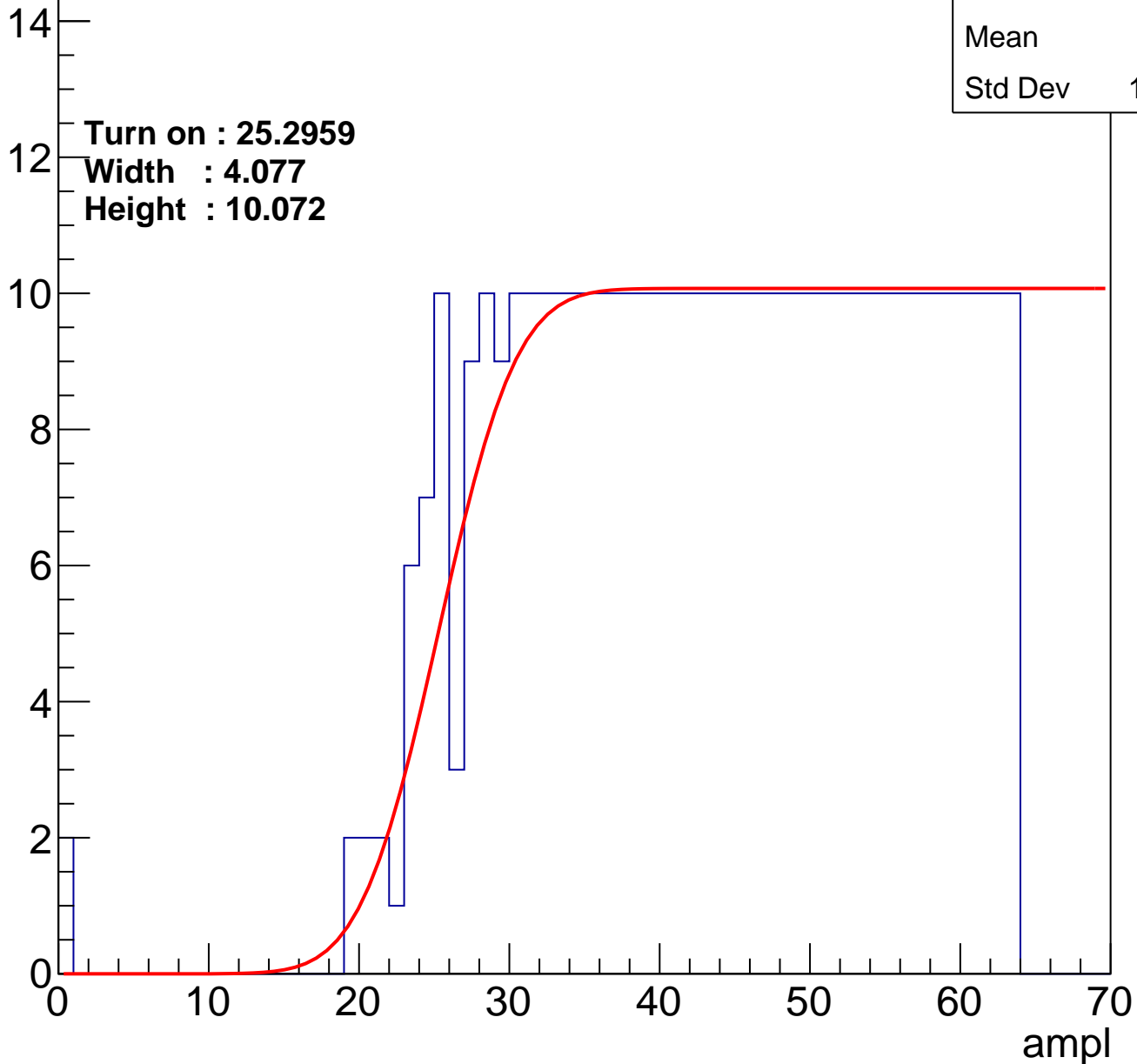
Entries	403
Mean	43.1
Std Dev	12.16

Turn on : 25.2959

Width : 4.077

Height : 10.072

Entry



B1L102S, U3-ch71

calib_packv5_042523_0143.root, FC#11, port A2

Entries	396
Mean	43.37
Std Dev	12.16

Turn on : 24.3153

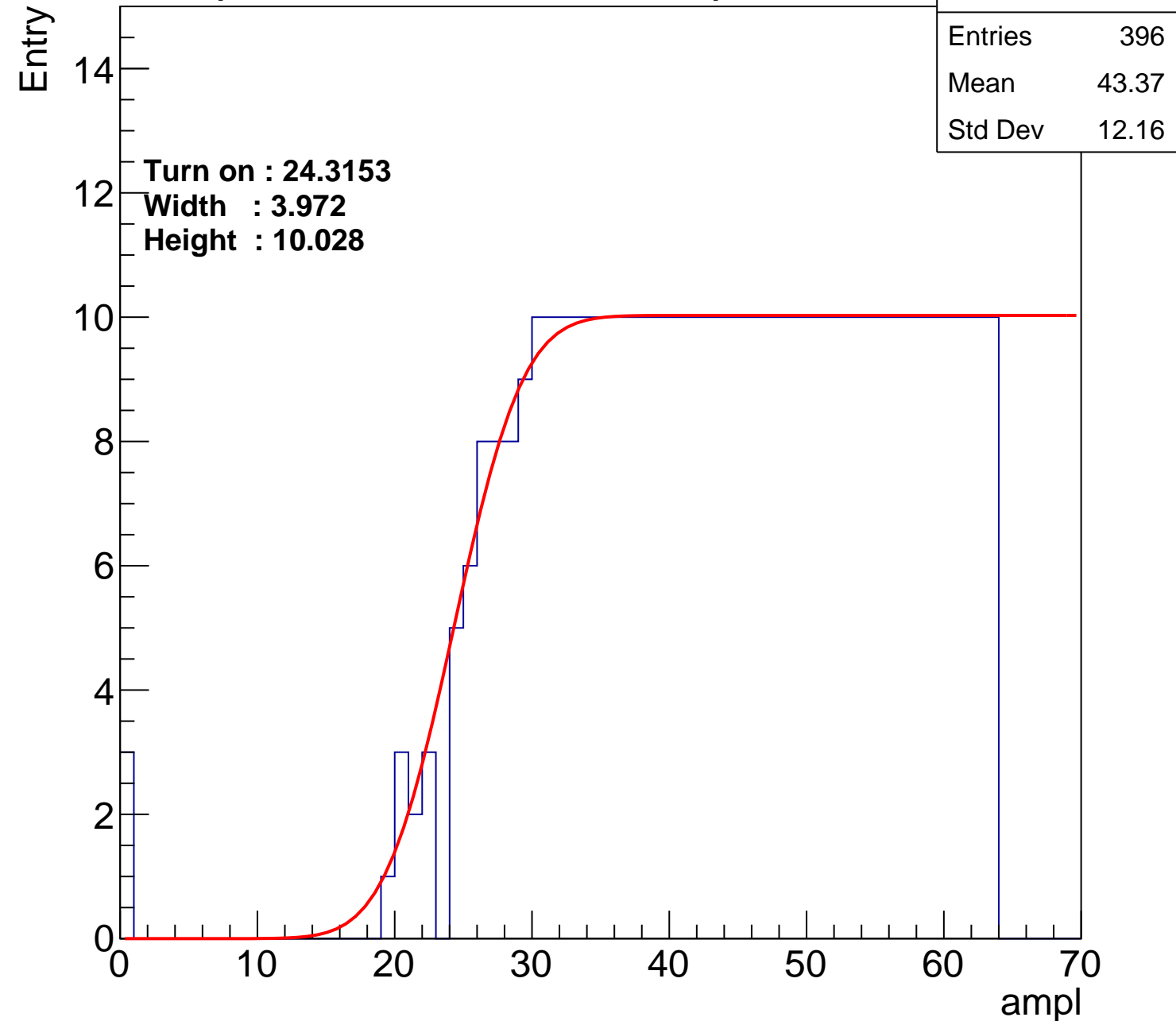
Width : 3.972

Height : 10.028

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch72

calib_packv5_042523_0143.root, FC#11, port A2

Entries	374
Mean	44.42
Std Dev	11.74

Turn on : 27.5467

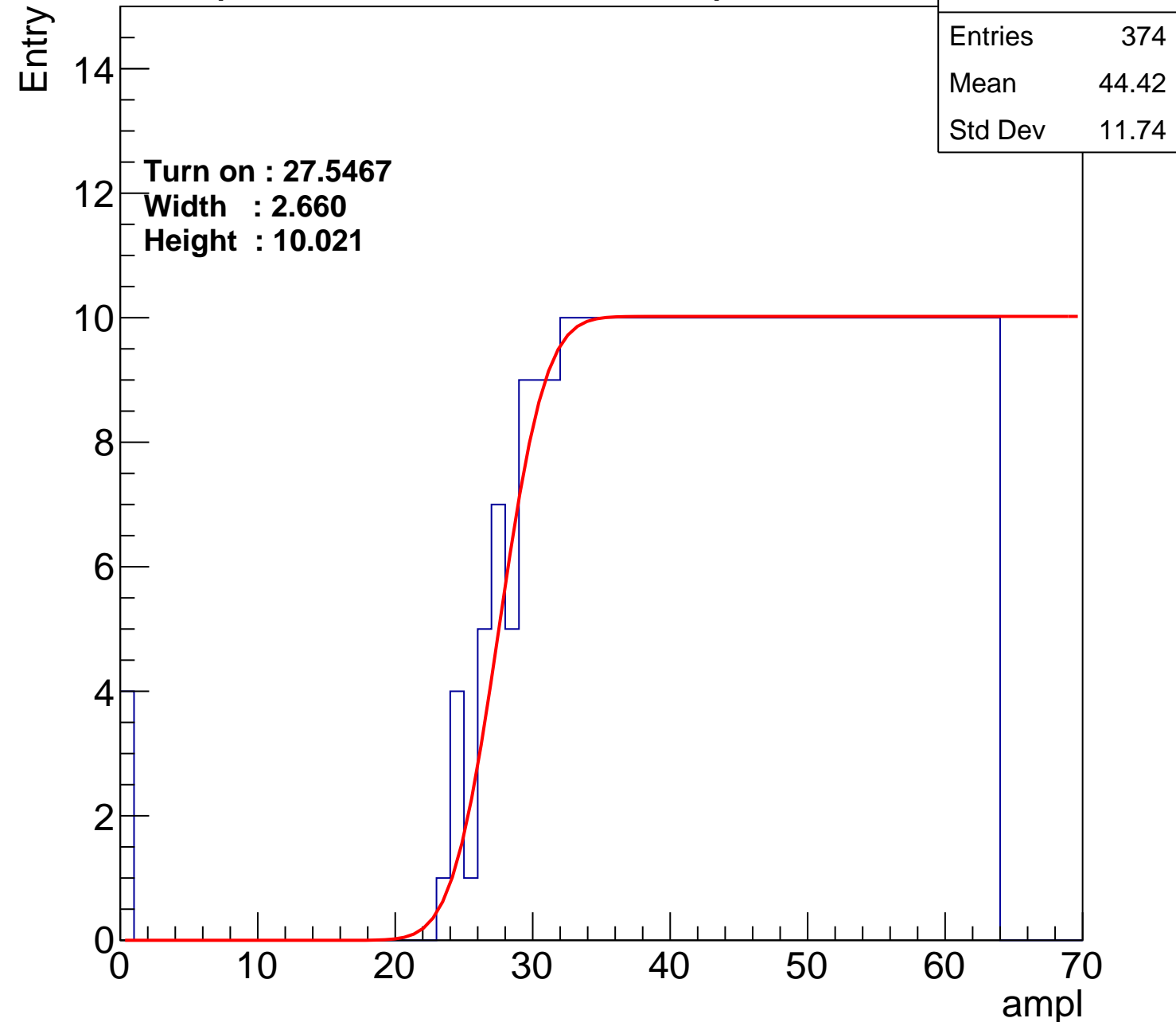
Width : 2.660

Height : 10.021

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch73

calib_packv5_042523_0143.root, FC#11, port A2

Entries	382
Mean	44.05
Std Dev	11.82

Turn on : 26.2367

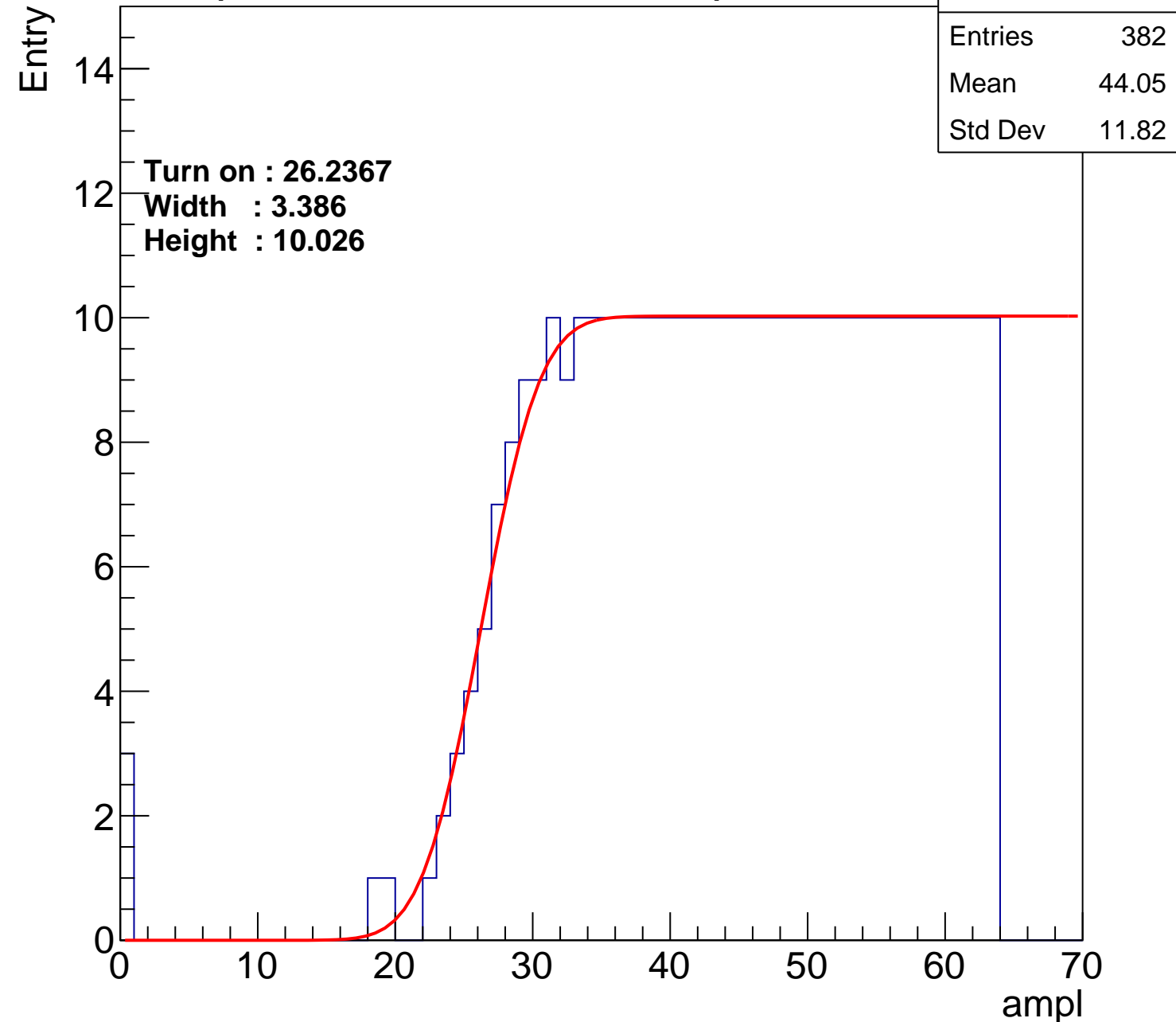
Width : 3.386

Height : 10.026

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch74

calib_packv5_042523_0143.root, FC#11, port A2

Entries	385
Mean	43.99
Std Dev	11.68

Turn on : 25.6888

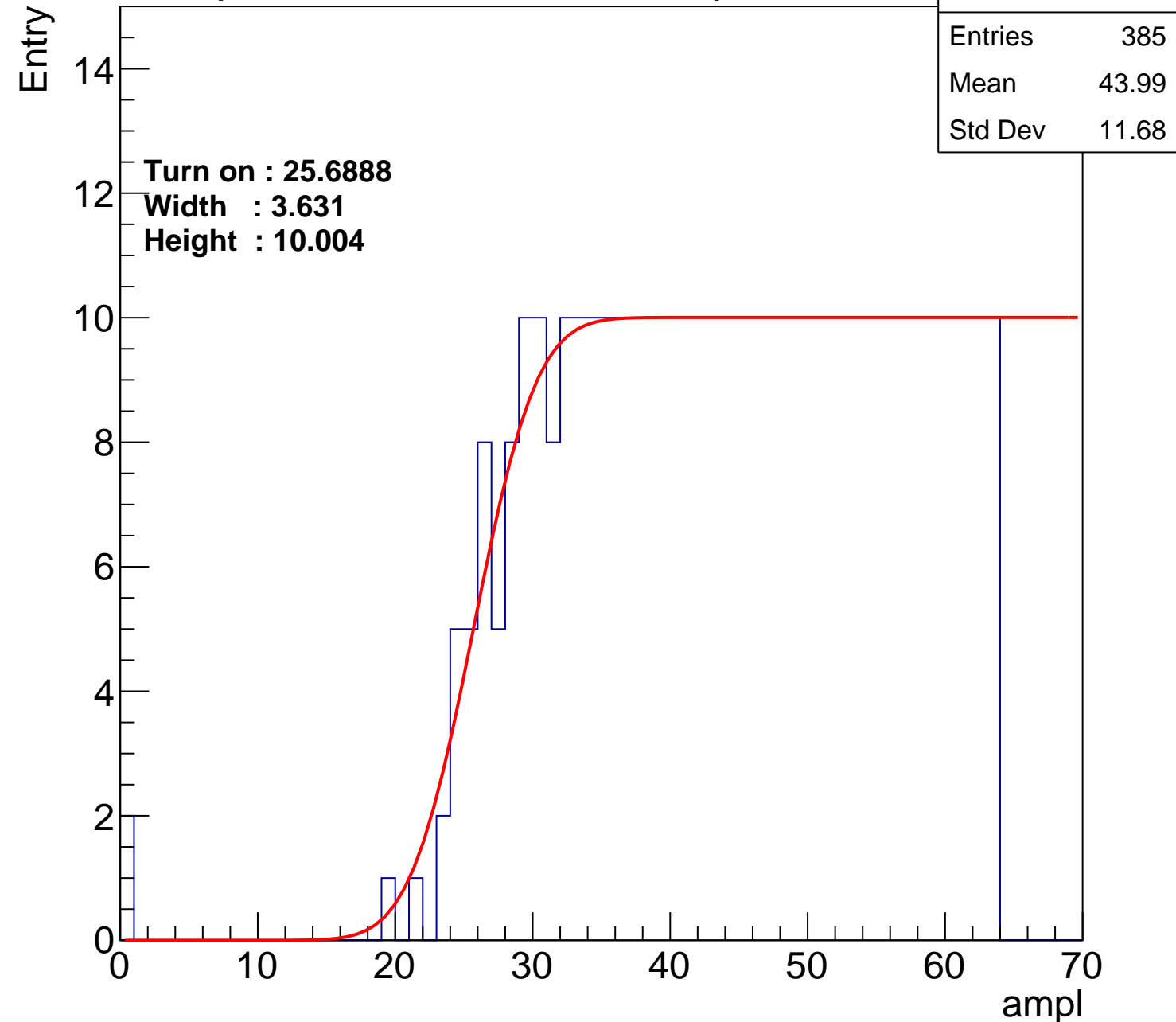
Width : 3.631

Height : 10.004

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch75

calib_packv5_042523_0143.root, FC#11, port A2

Entries	393
Mean	43.64
Std Dev	11.76

Turn on : 25.1197

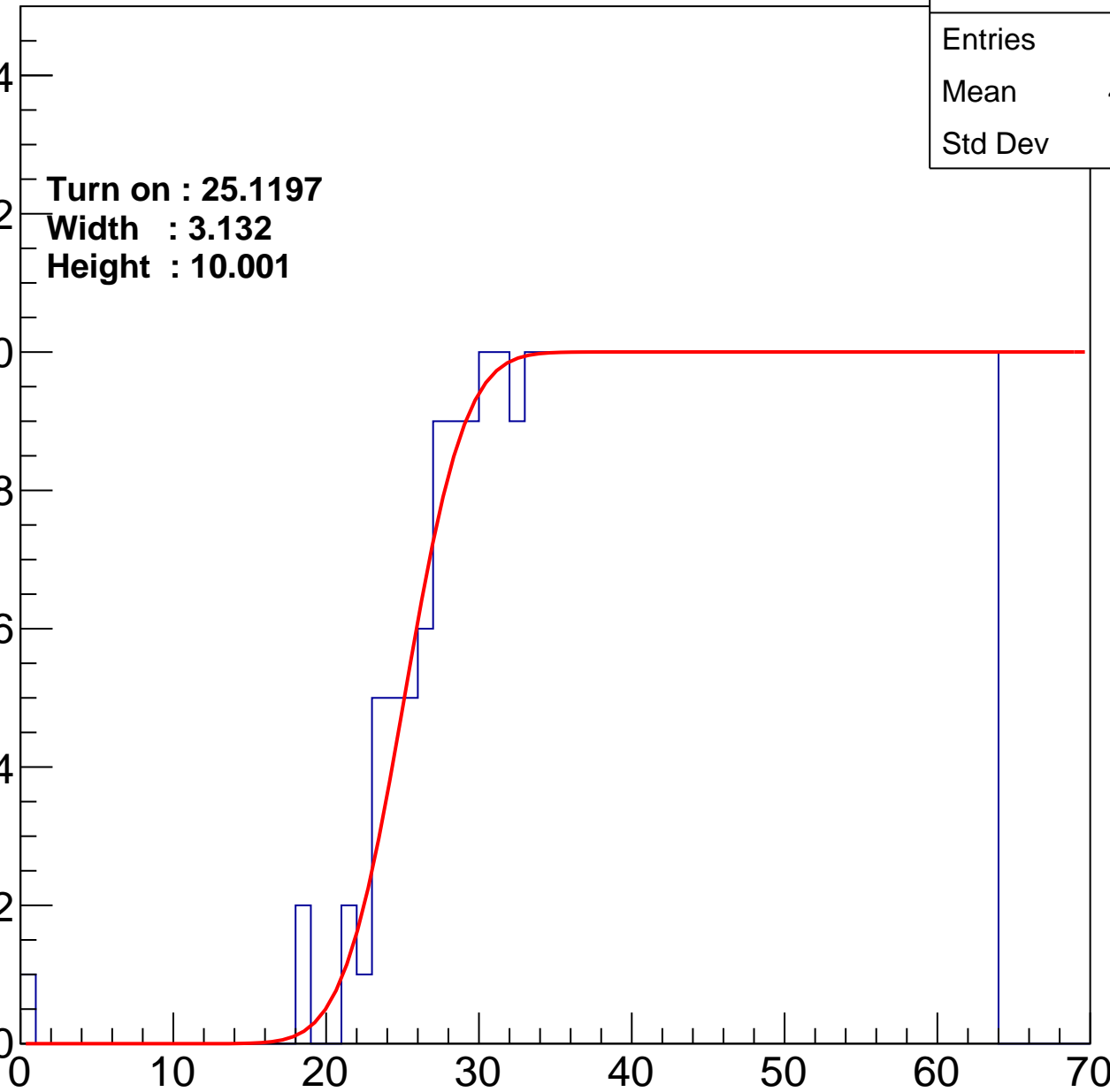
Width : 3.132

Height : 10.001

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch76

calib_packv5_042523_0143.root, FC#11, port A2

Entries	395
Mean	43.4
Std Dev	12.22

Turn on : 25.1682

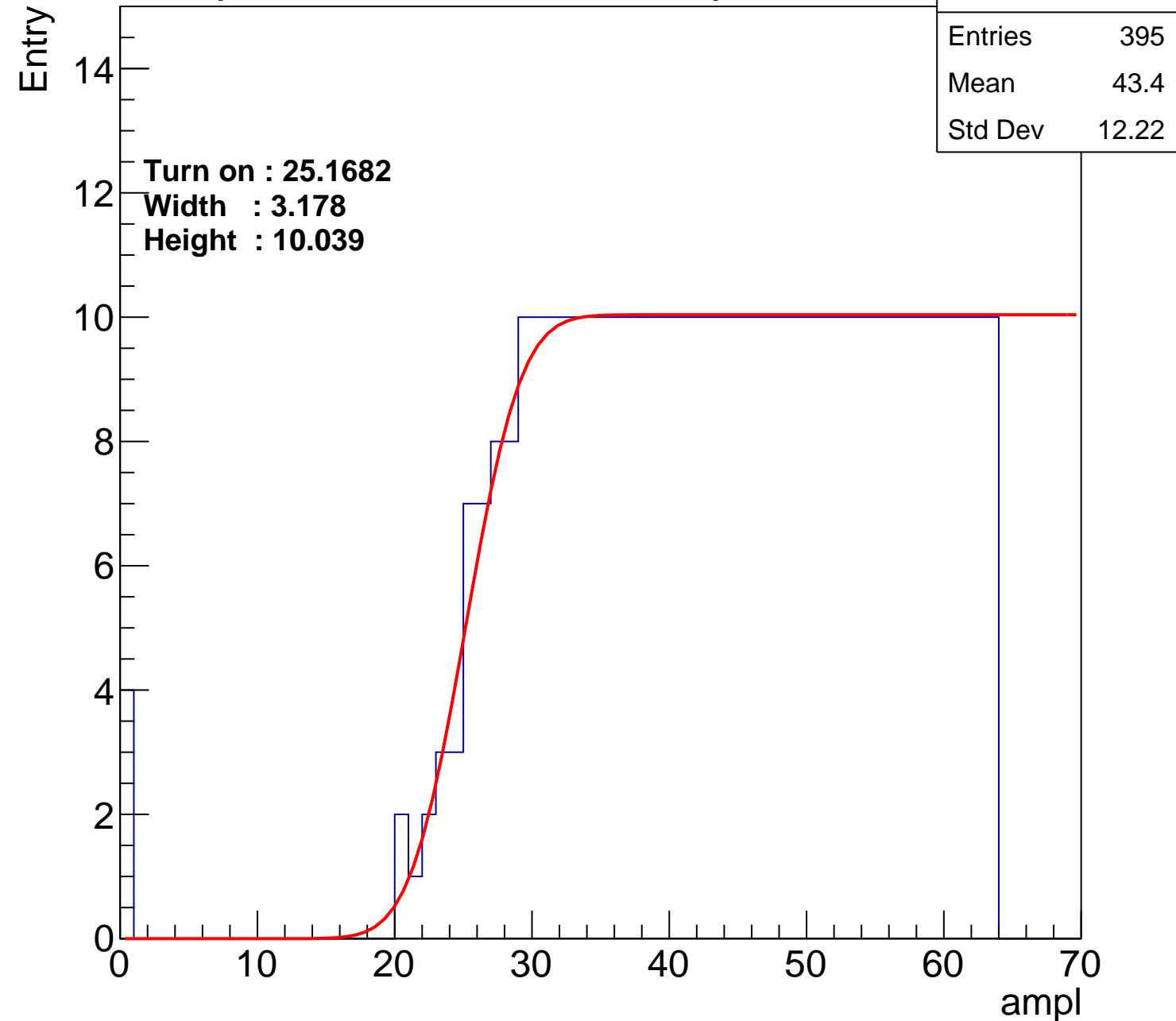
Width : 3.178

Height : 10.039

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch77

calib_packv5_042523_0143.root, FC#11, port A2

Entries	386
Mean	43.95
Std Dev	11.7

Turn on : 25.6171

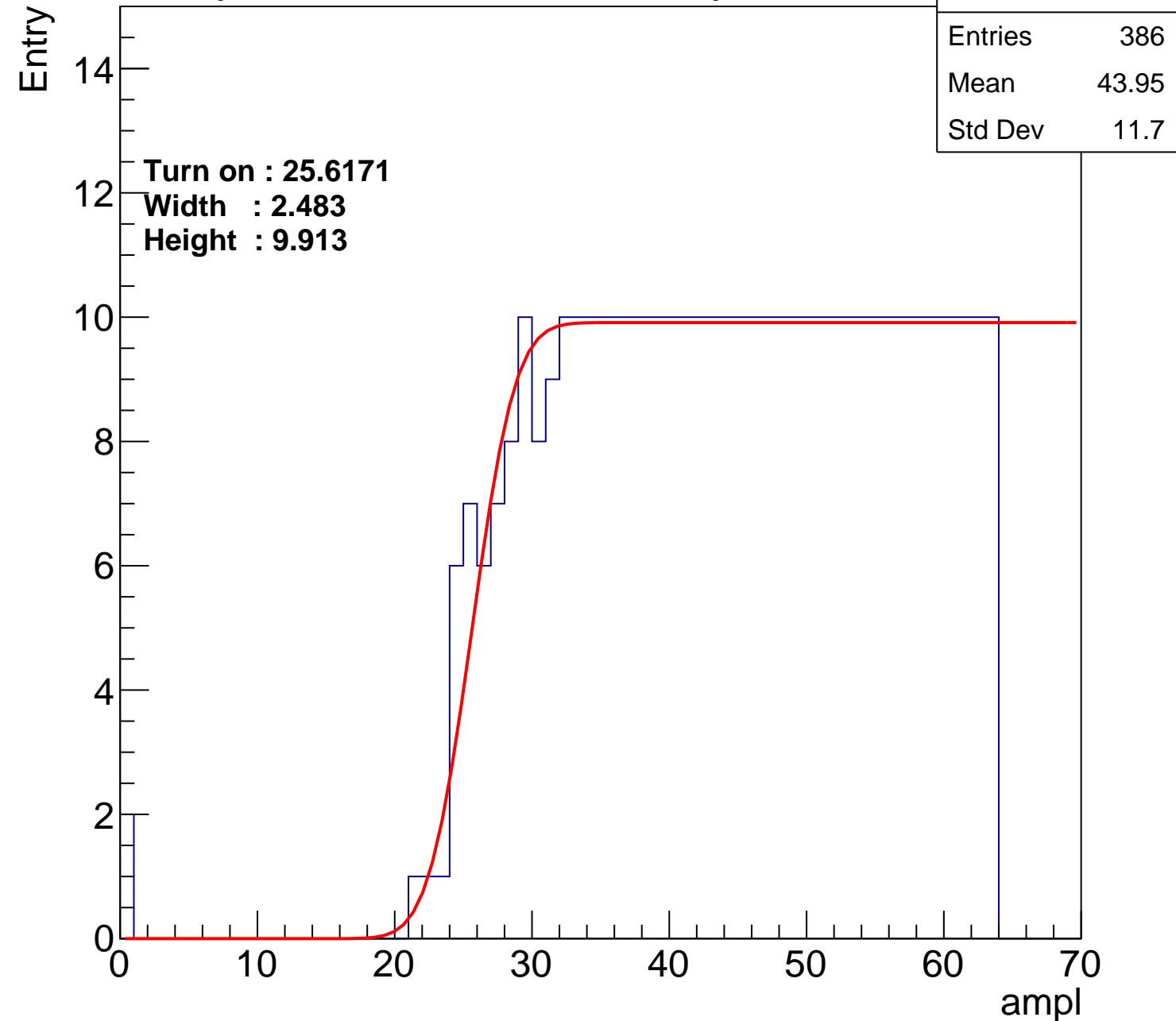
Width : 2.483

Height : 9.913

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch78

calib_packv5_042523_0143.root, FC#11, port A2

Entries	393
Mean	43.49
Std Dev	12.19

Turn on : 25.5424

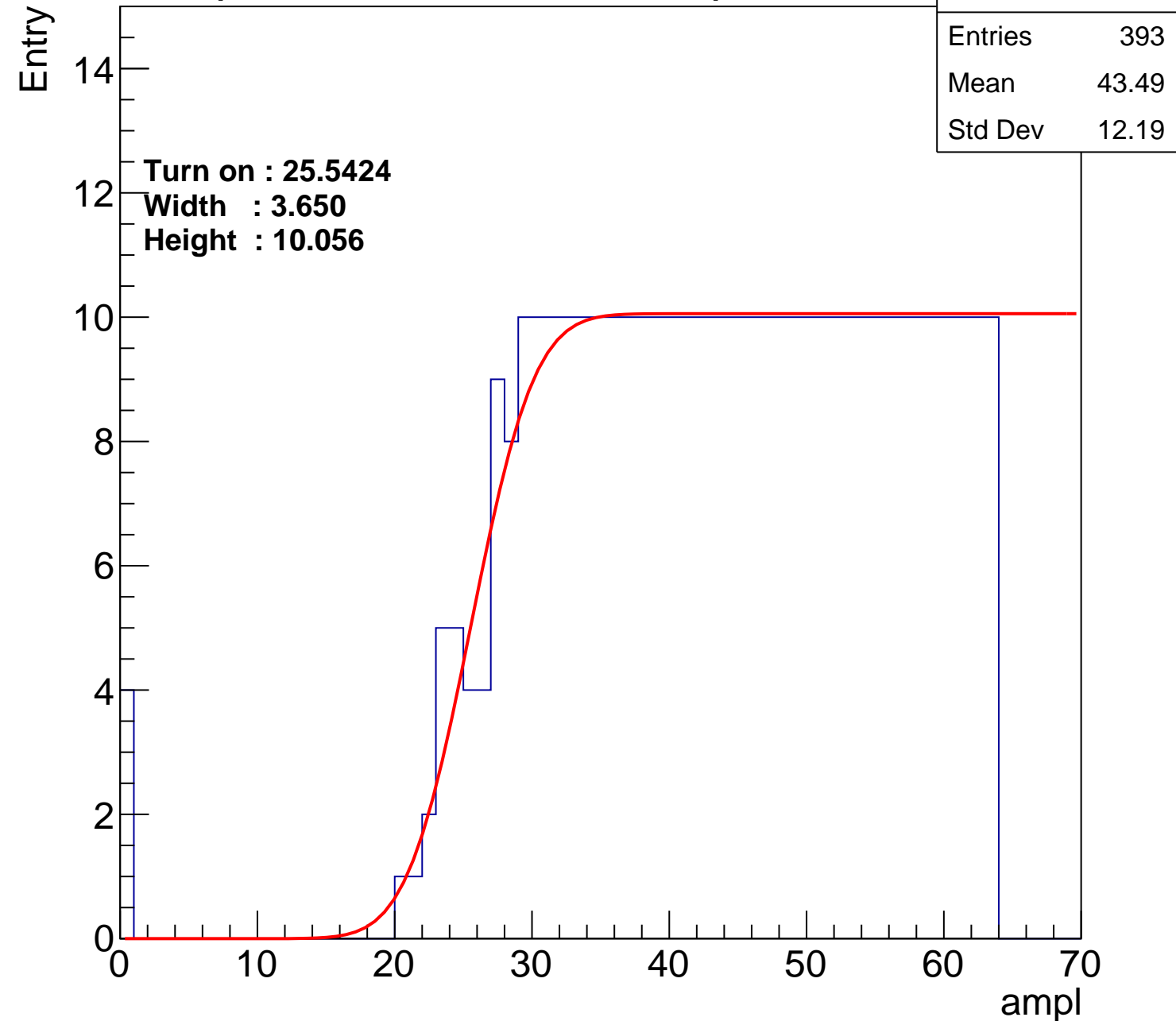
Width : 3.650

Height : 10.056

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch79

calib_packv5_042523_0143.root, FC#11, port A2

Entries	393
Mean	43.68
Std Dev	11.7

Turn on : 24.6145

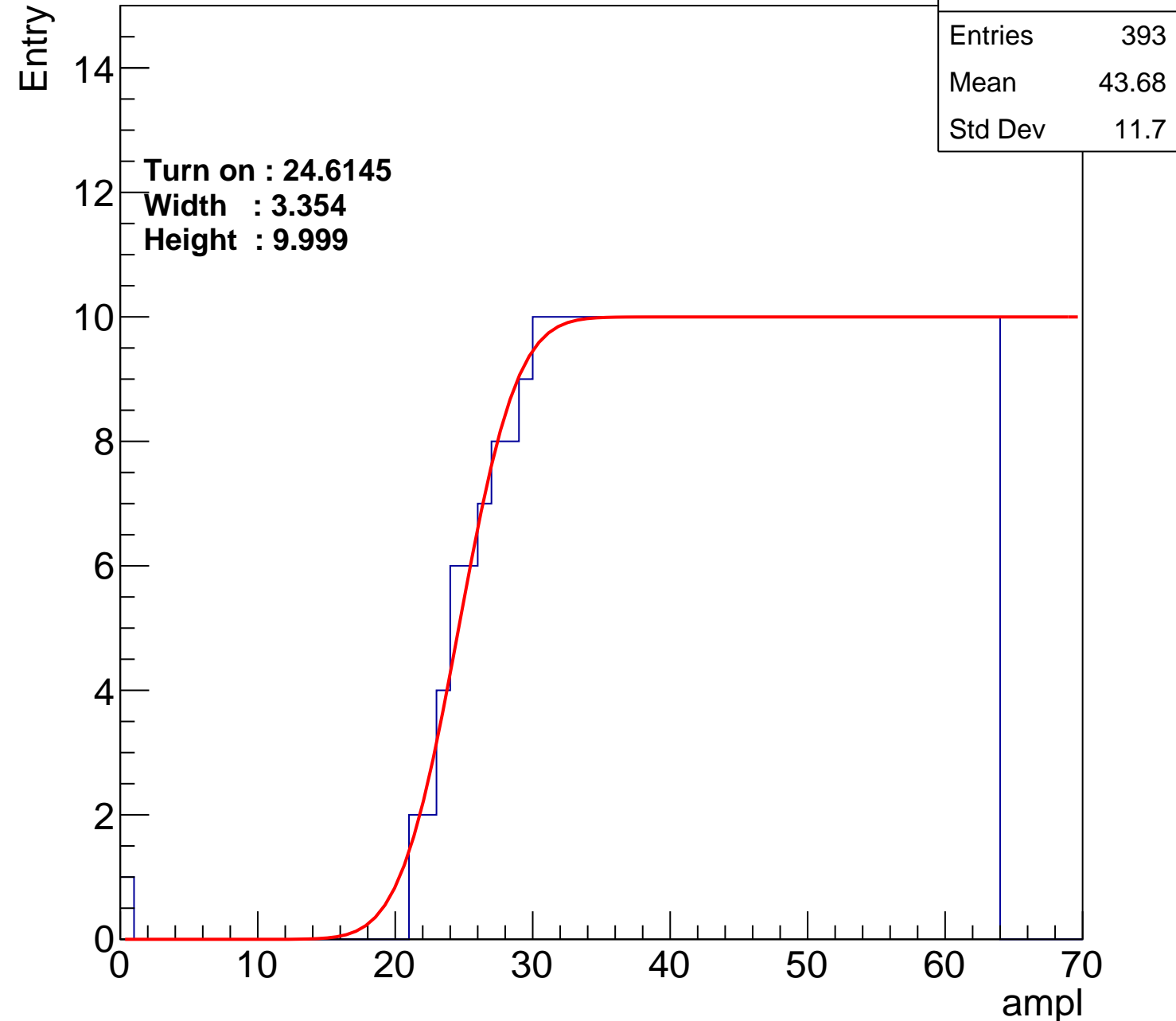
Width : 3.354

Height : 9.999

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch80

calib_packv5_042523_0143.root, FC#11, port A2

Entries	380
Mean	44.28
Std Dev	11.4

Turn on : 26.1936

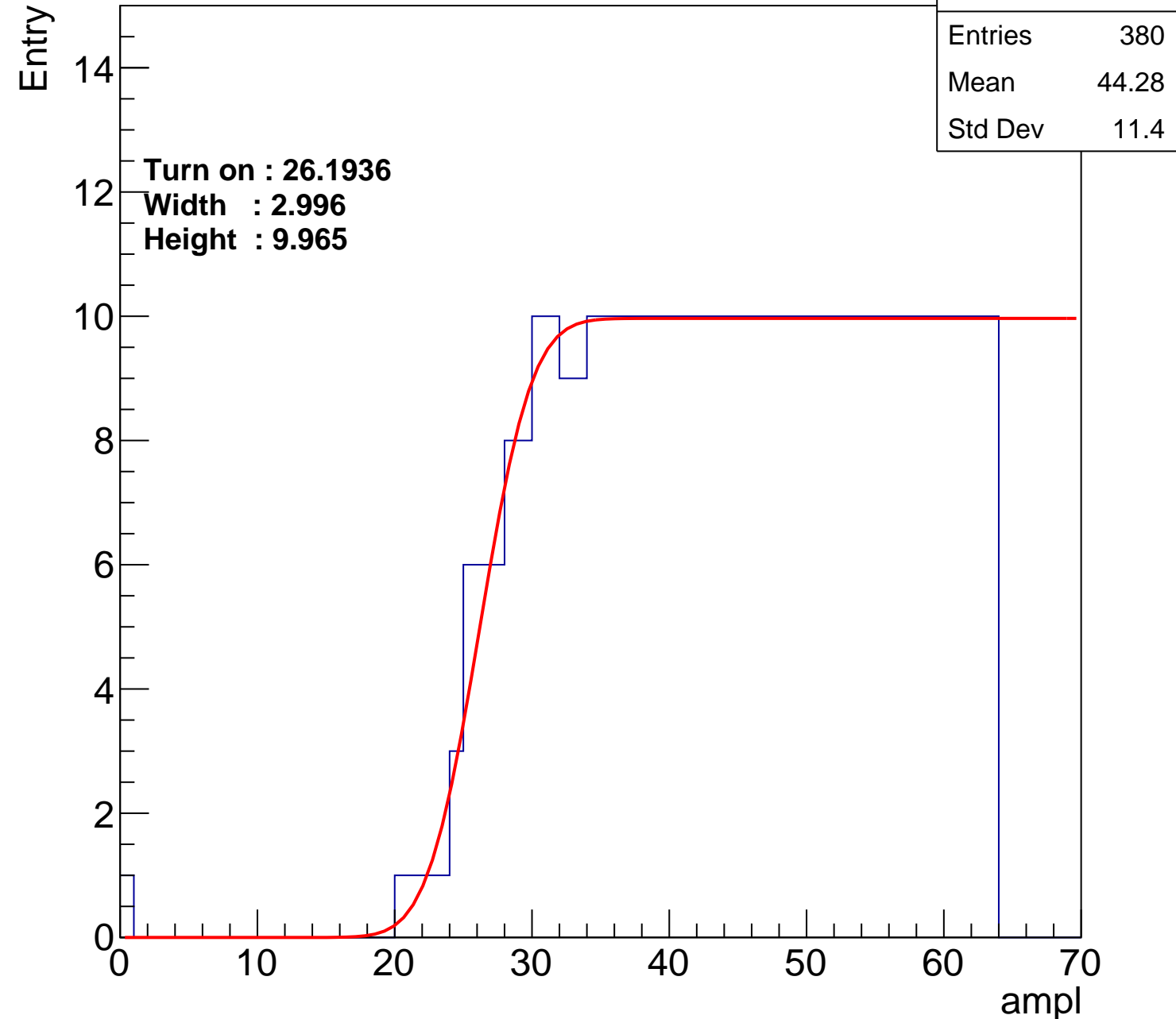
Width : 2.996

Height : 9.965

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch81

calib_packv5_042523_0143.root, FC#11, port A2

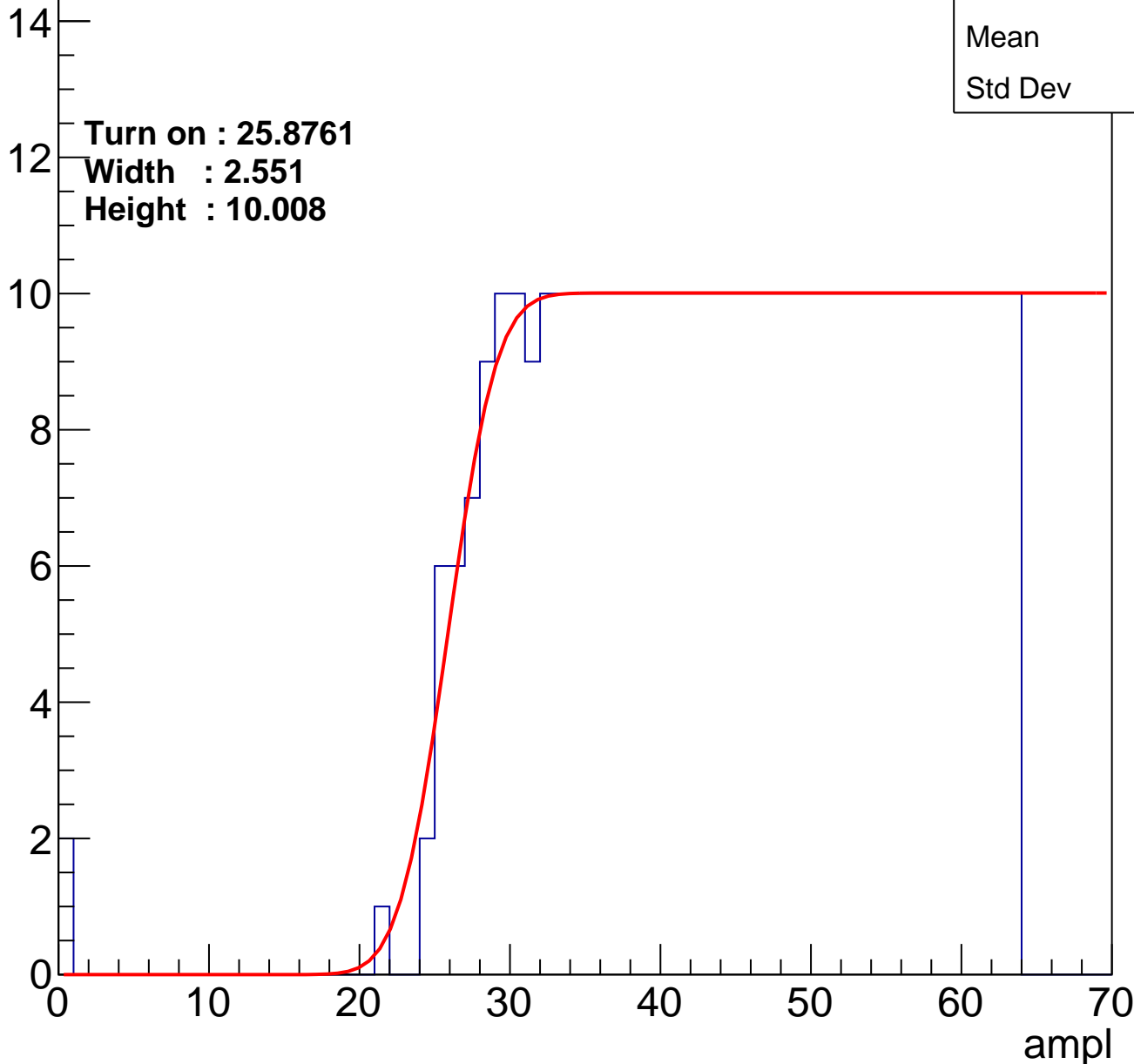
Entries	382
Mean	44.2
Std Dev	11.5

Turn on : 25.8761

Width : 2.551

Height : 10.008

Entry



B1L102S, U3-ch82

calib_packv5_042523_0143.root, FC#11, port A2

Entries	403
Mean	43.06
Std Dev	12.34

Turn on : 24.2127

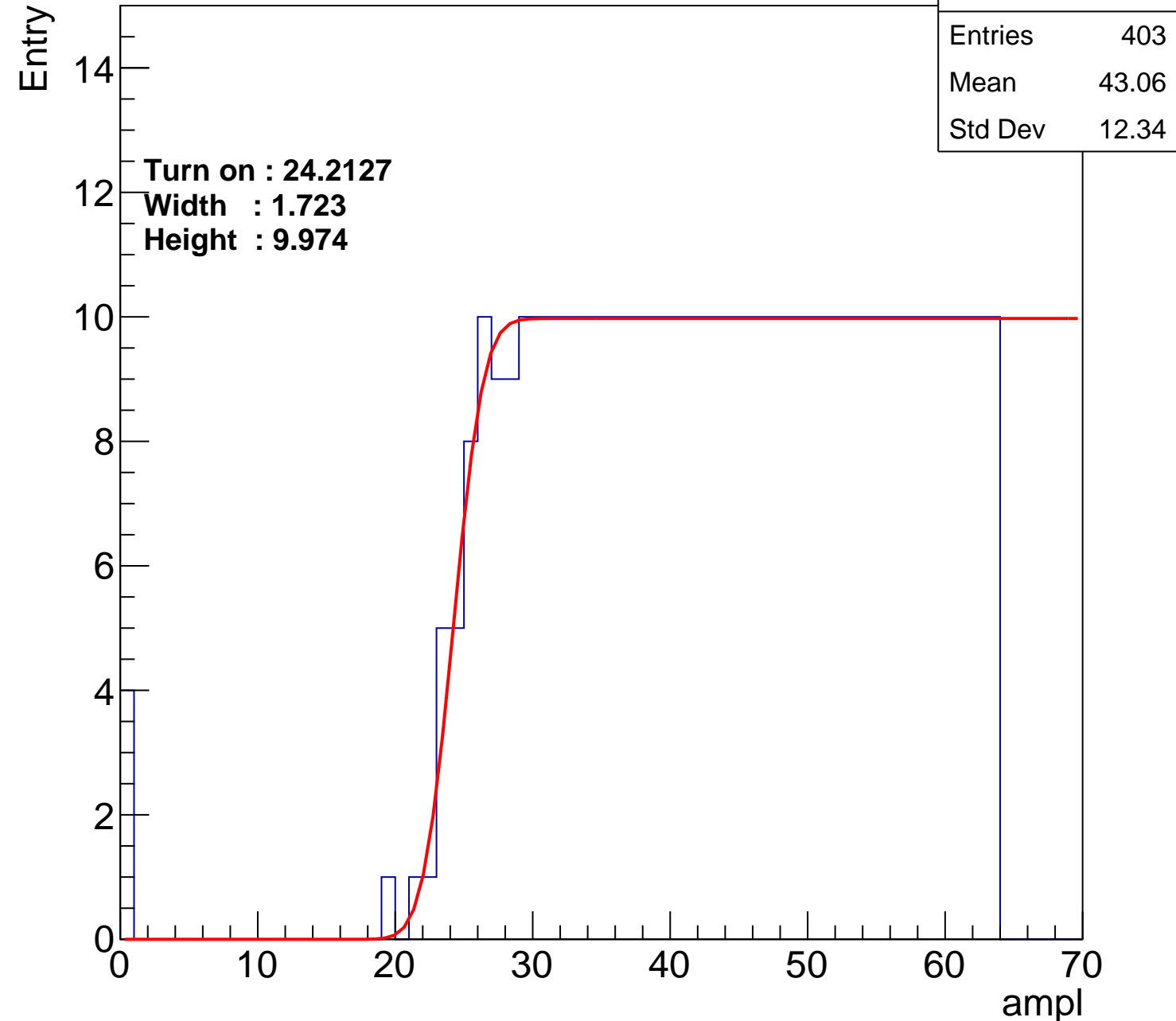
Width : 1.723

Height : 9.974

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch83

calib_packv5_042523_0143.root, FC#11, port A2

Entries	387
Mean	43.75
Std Dev	12.16

Turn on : 25.6108

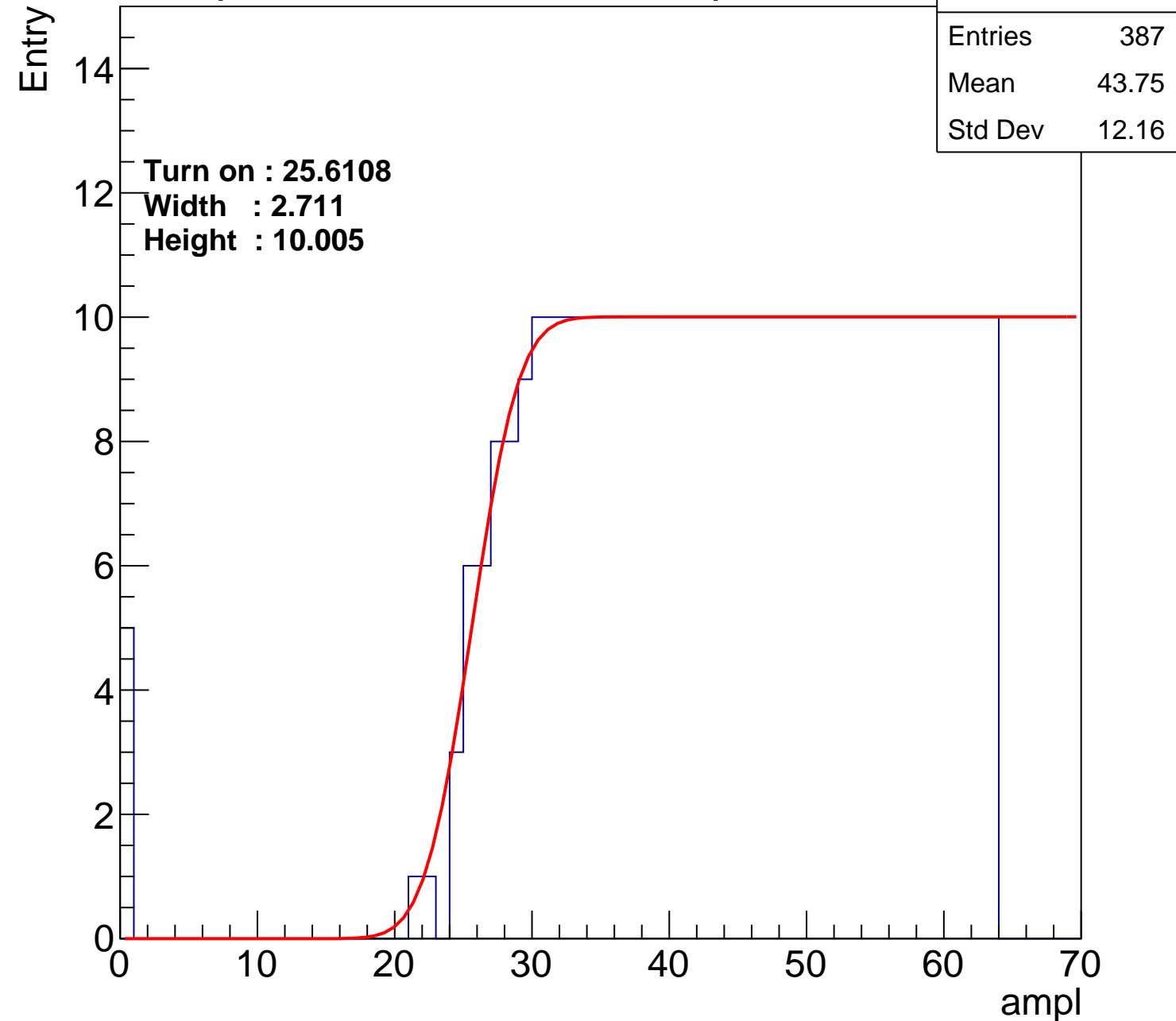
Width : 2.711

Height : 10.005

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch84

calib_packv5_042523_0143.root, FC#11, port A2

Entries	400
Mean	43.16
Std Dev	12.34

Turn on : 24.7573

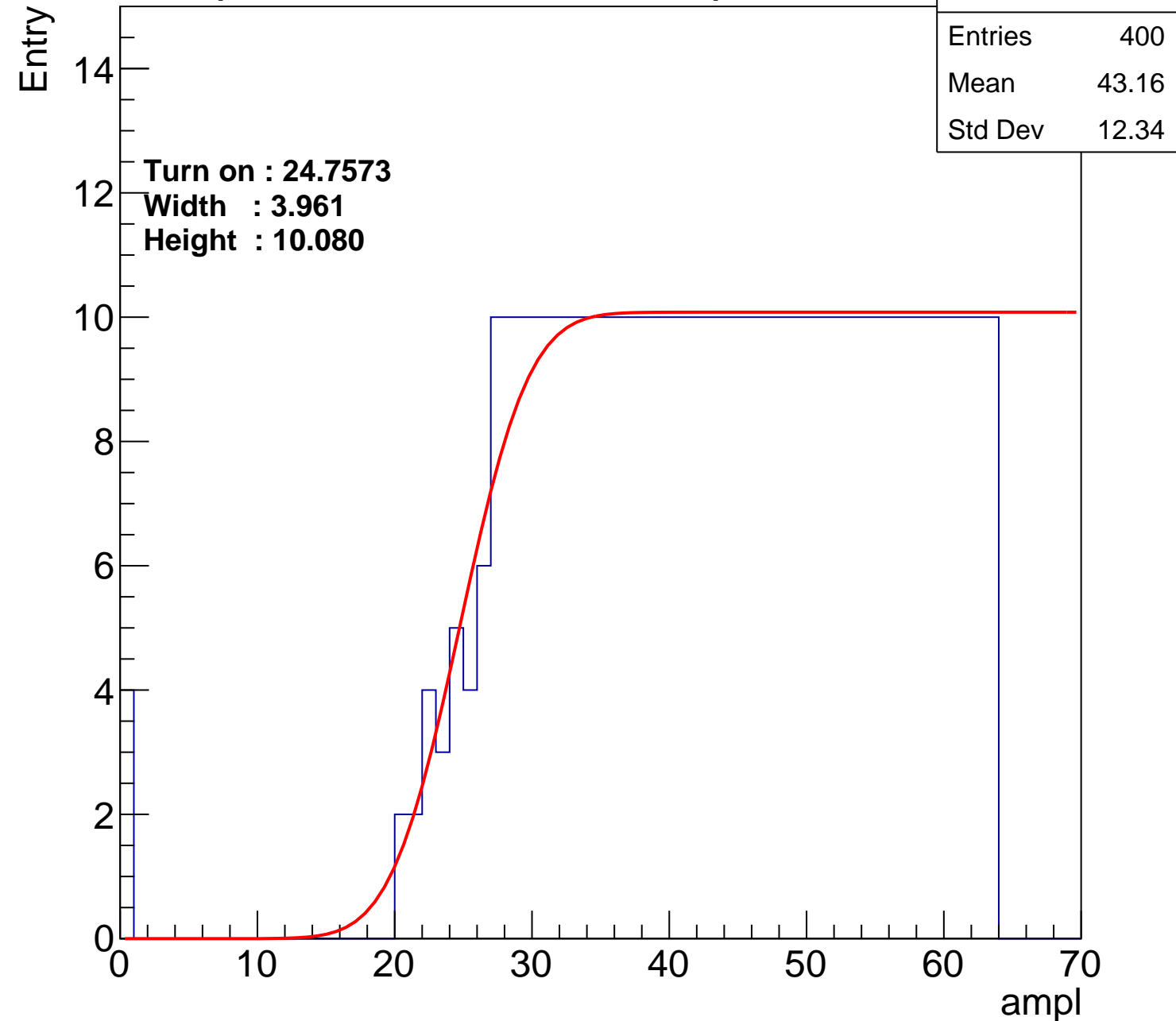
Width : 3.961

Height : 10.080

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch85

calib_packv5_042523_0143.root, FC#11, port A2

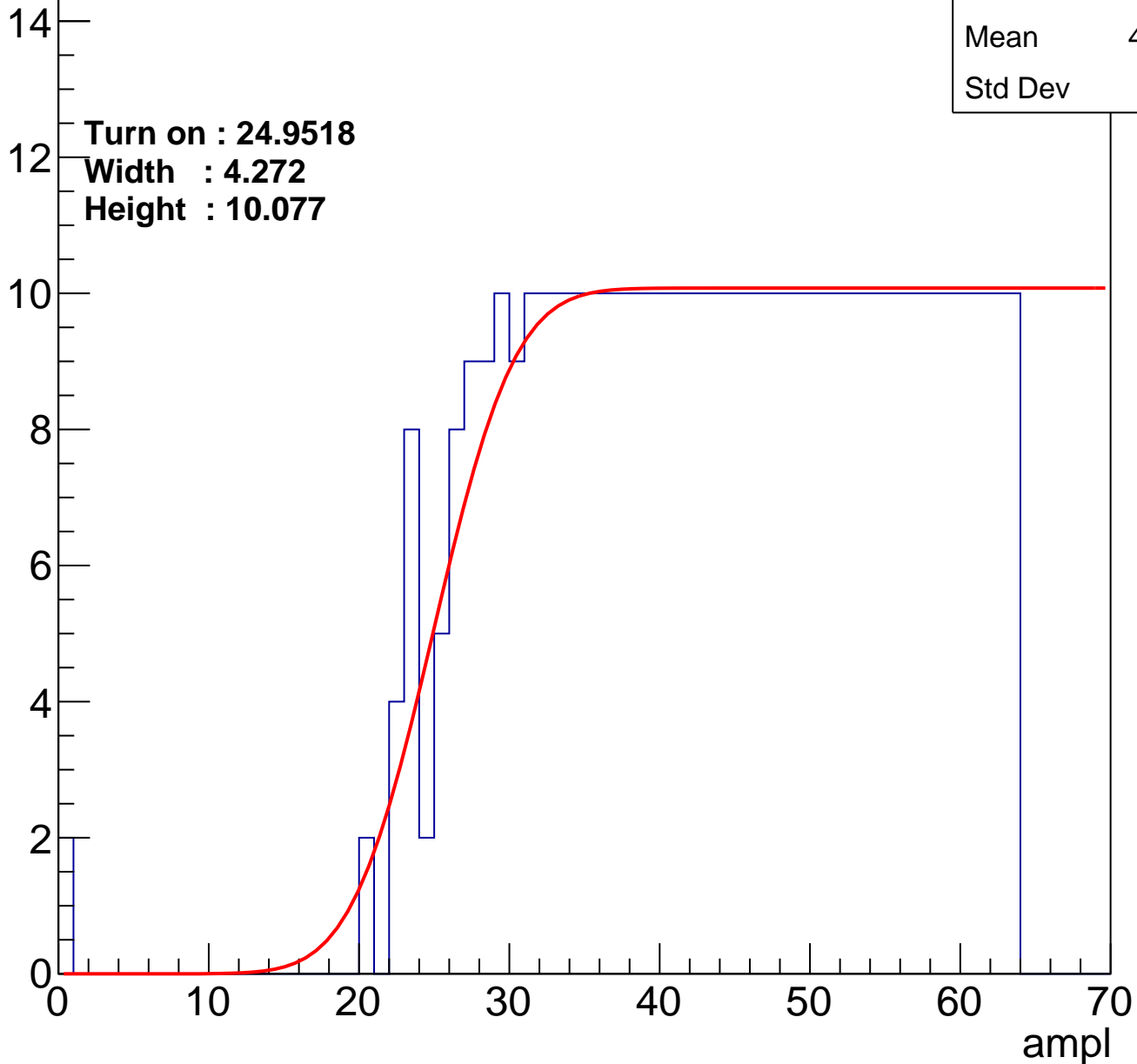
Entries	398
Mean	43.36
Std Dev	12

Turn on : 24.9518

Width : 4.272

Height : 10.077

Entry



B1L102S, U3-ch86

calib_packv5_042523_0143.root, FC#11, port A2

Entries	395
Mean	43.37
Std Dev	12.19

Turn on : 24.8766

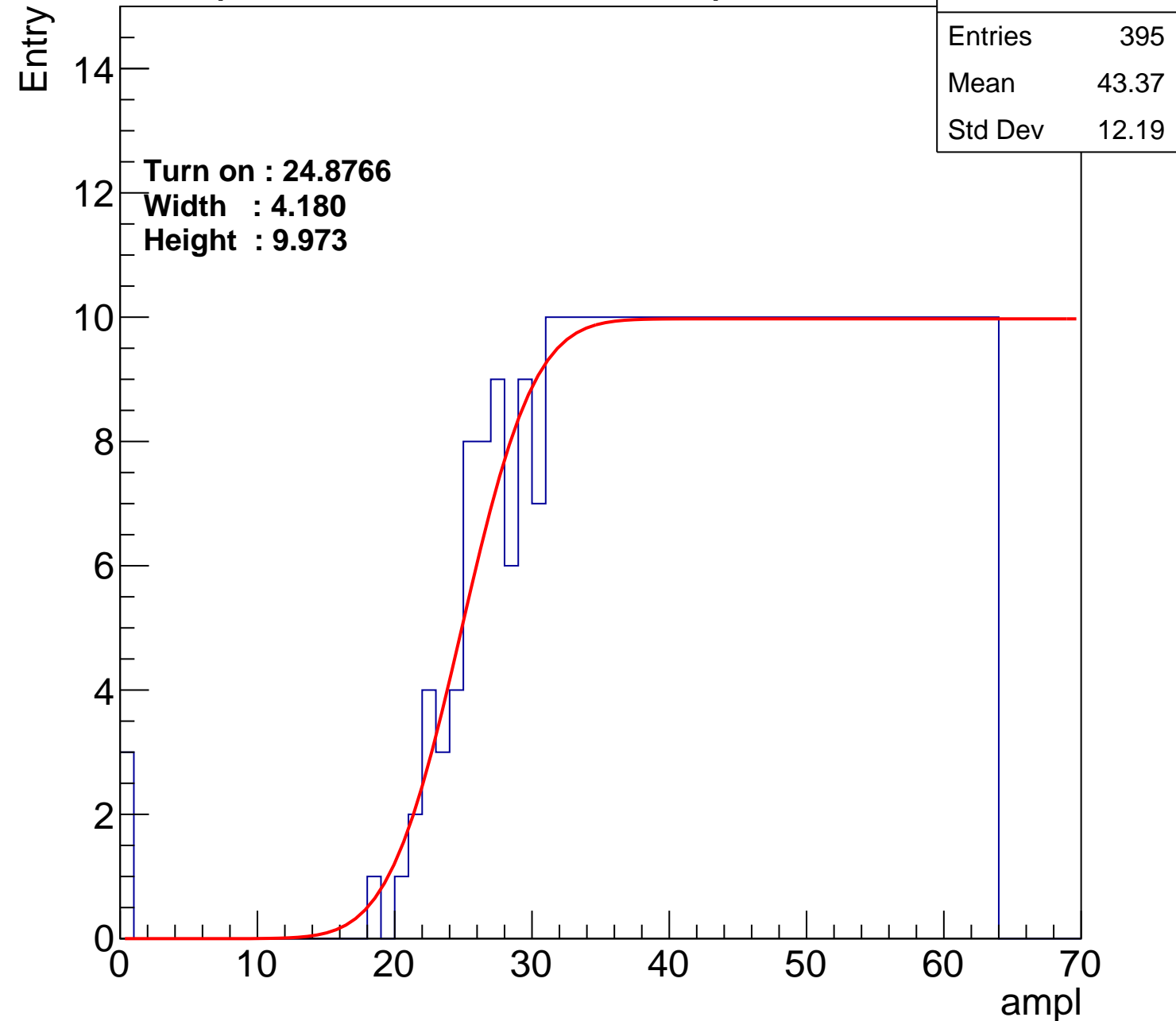
Width : 4.180

Height : 9.973

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch87

calib_packv5_042523_0143.root, FC#11, port A2

Entries	390
Mean	43.75
Std Dev	12.2

Turn on : 26.1432

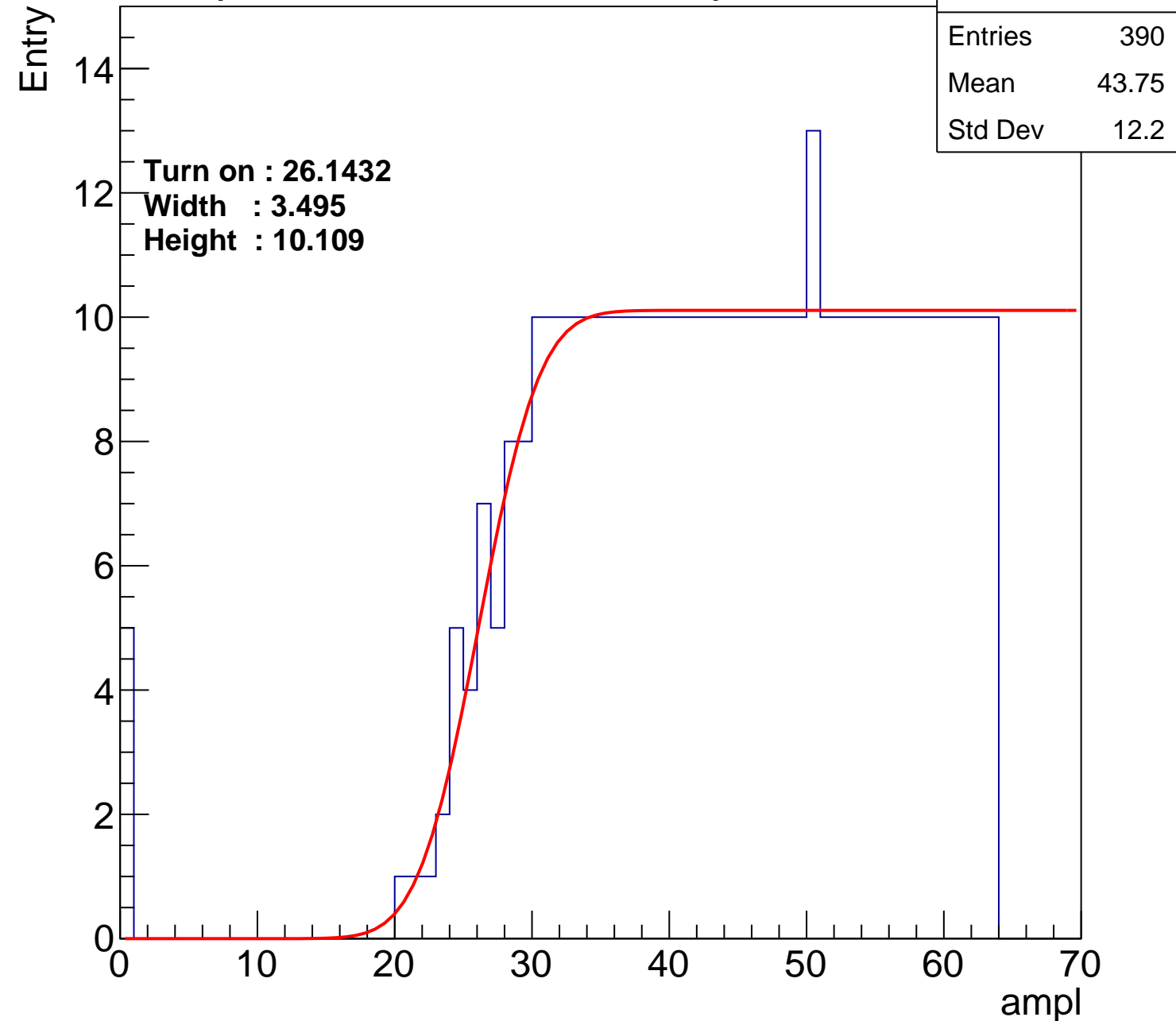
Width : 3.495

Height : 10.109

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch88

calib_packv5_042523_0143.root, FC#11, port A2

Entries	370
Mean	44.8
Std Dev	11.1

Turn on : 27.1962

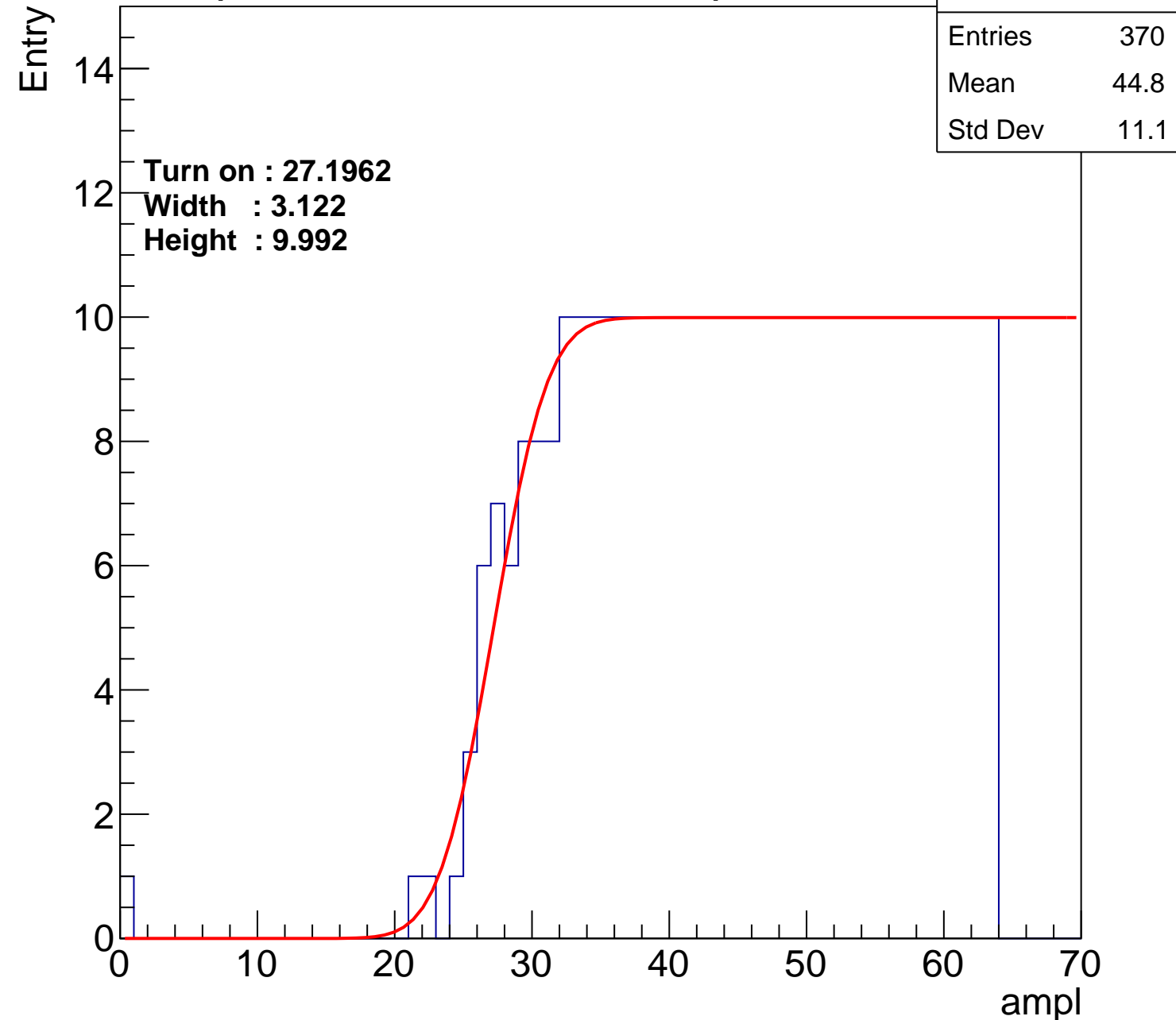
Width : 3.122

Height : 9.992

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch89

calib_packv5_042523_0143.root, FC#11, port A2

Entries	379
Mean	44.25
Std Dev	11.66

Turn on : 26.7425

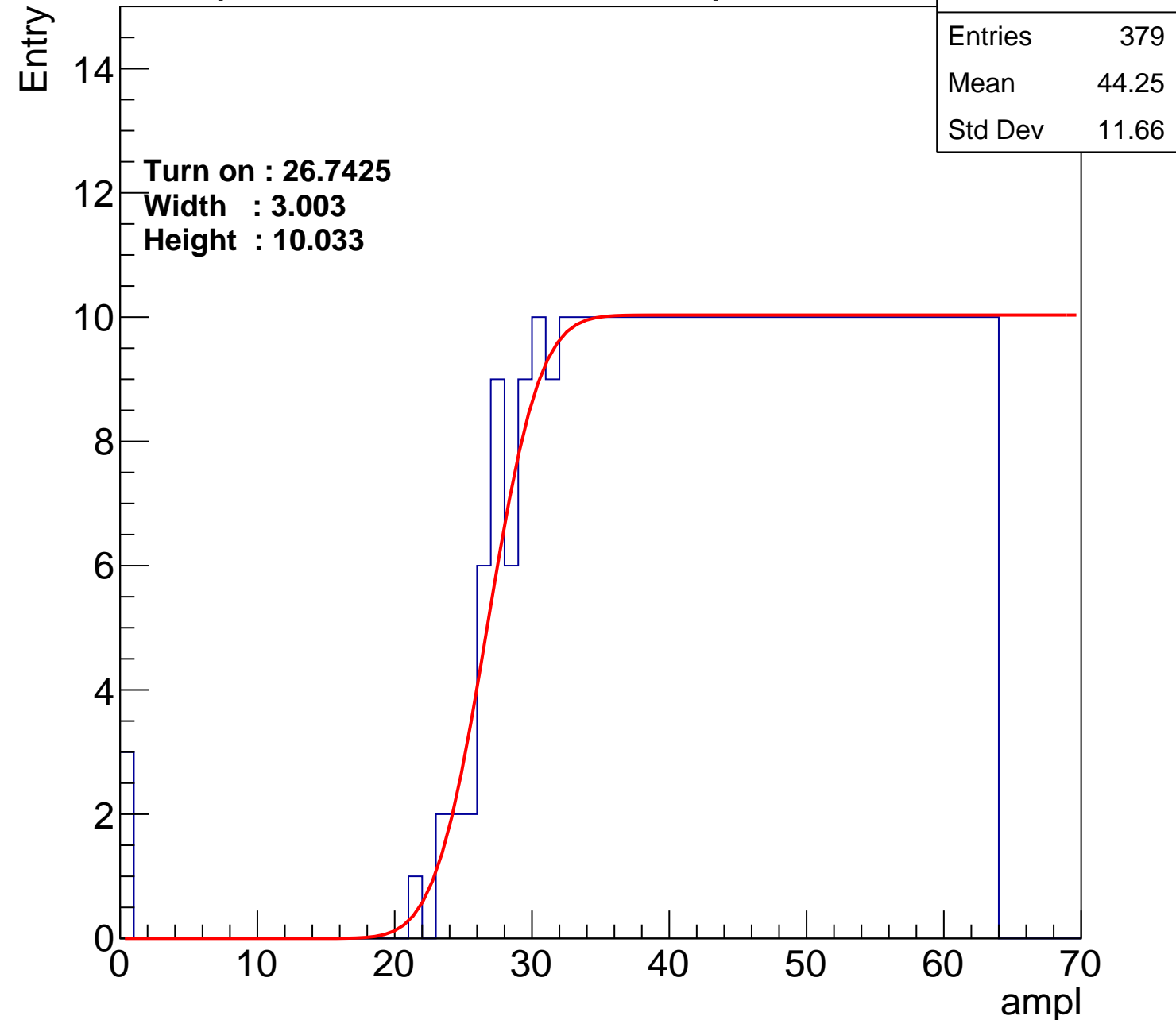
Width : 3.003

Height : 10.033

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch90

calib_packv5_042523_0143.root, FC#11, port A2

Entries	401
Mean	43.21
Std Dev	12.09

Turn on : 24.9238

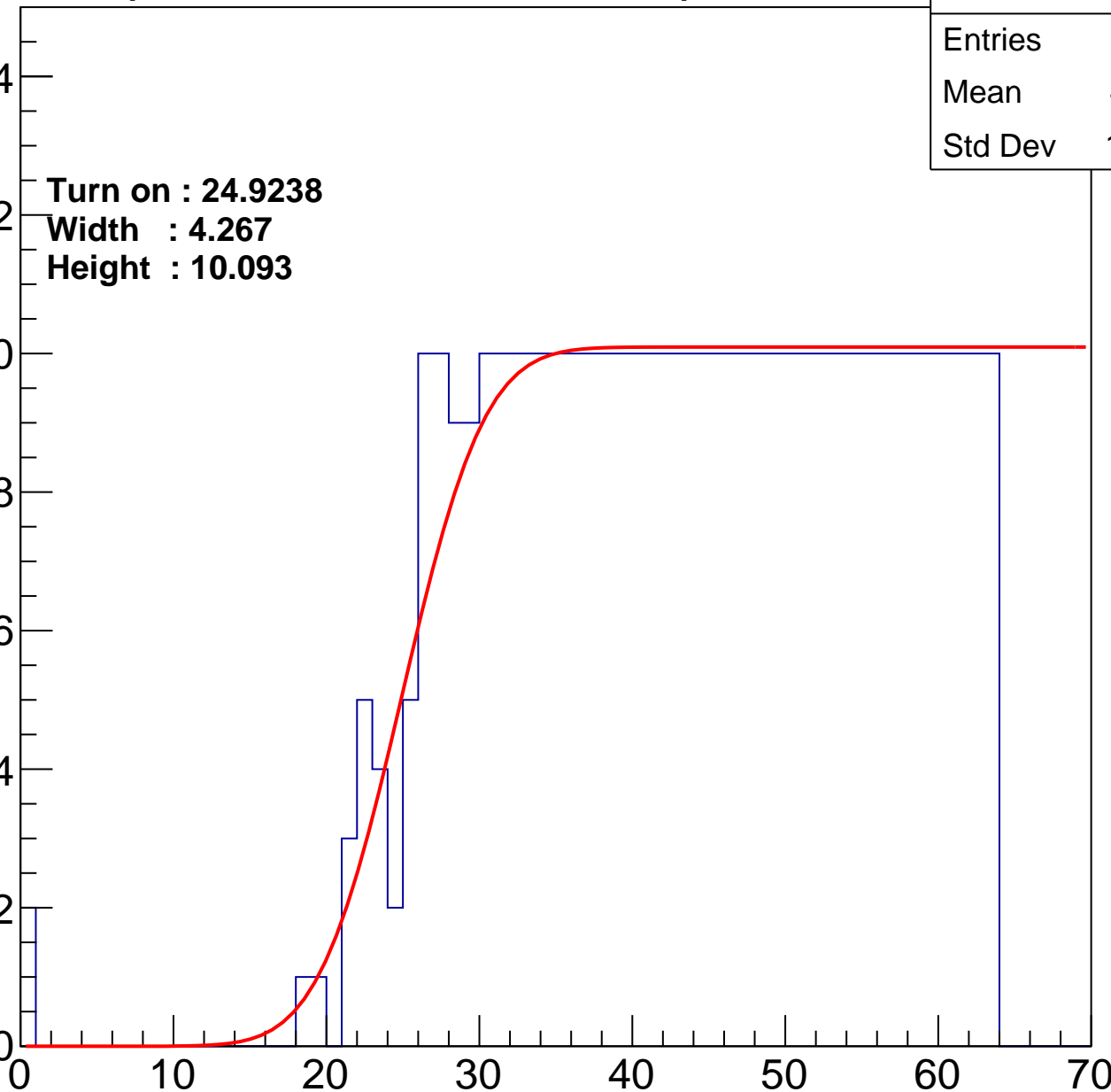
Width : 4.267

Height : 10.093

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch91

calib_packv5_042523_0143.root, FC#11, port A2

Entries	379
Mean	44.33
Std Dev	11.37

Turn on : 26.3504

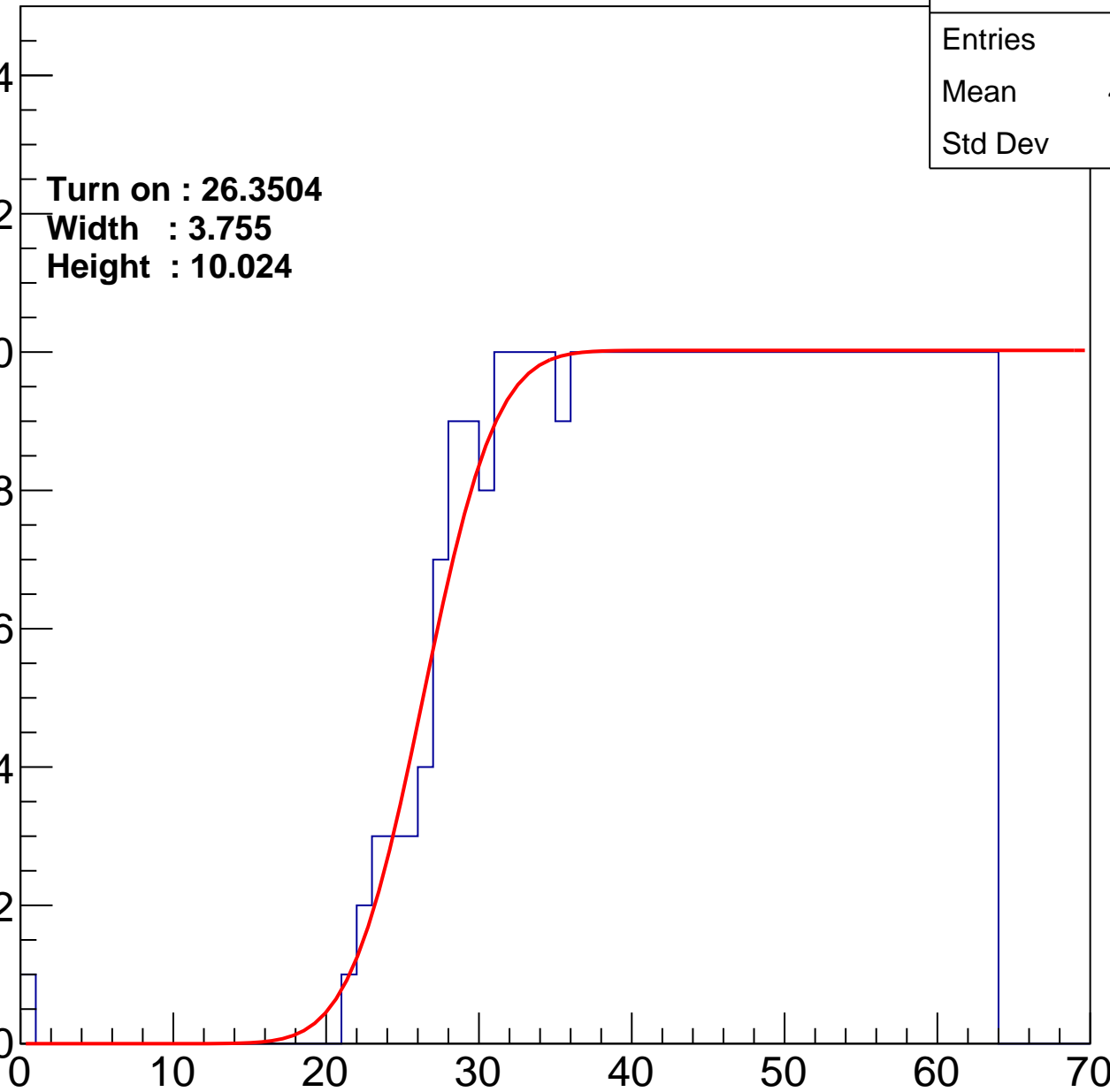
Width : 3.755

Height : 10.024

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch92

calib_packv5_042523_0143.root, FC#11, port A2

Entries	400
Mean	43.18
Std Dev	12.2

Turn on : 25.2119

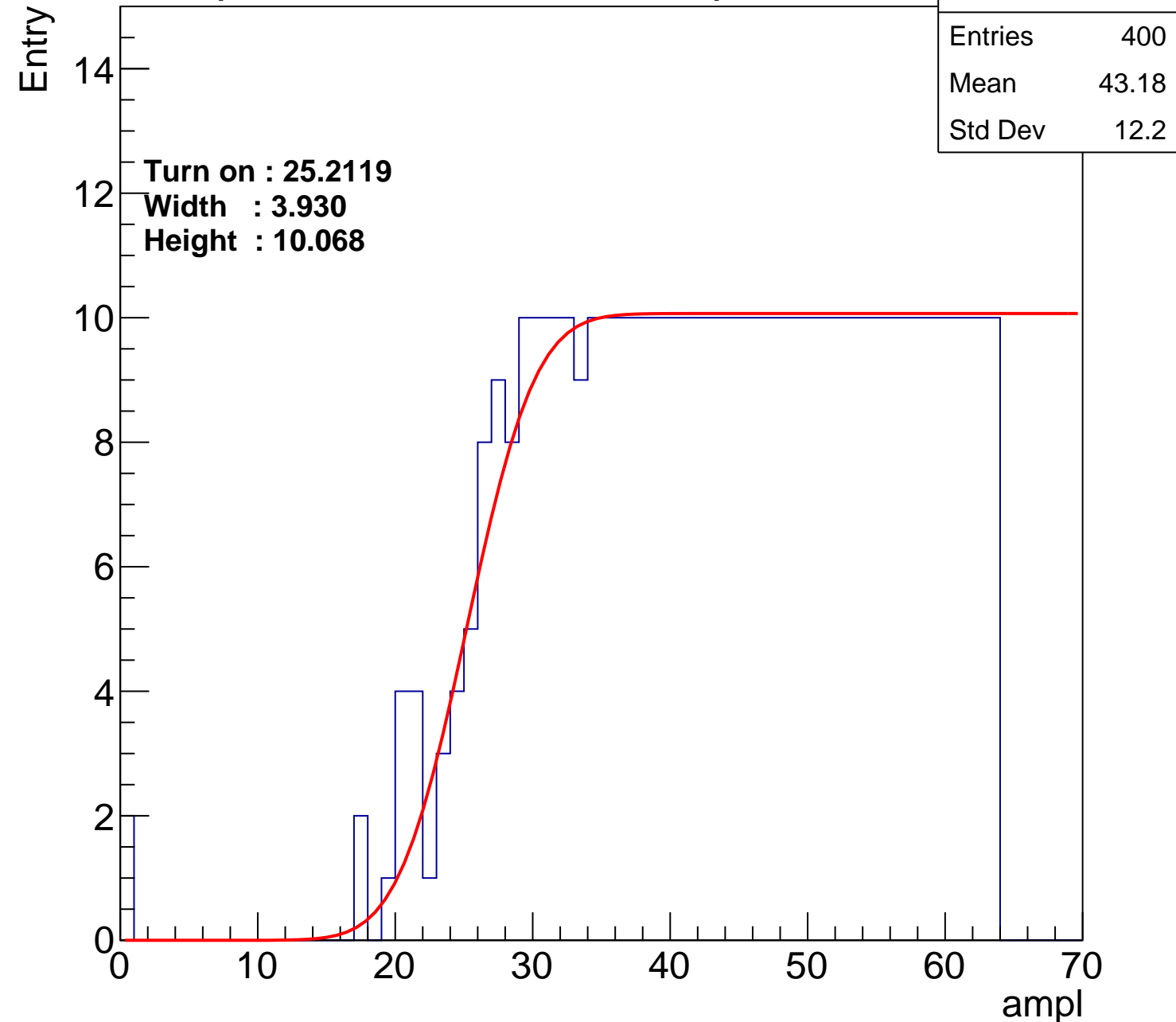
Width : 3.930

Height : 10.068

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch93

calib_packv5_042523_0143.root, FC#11, port A2

Entries	400
Mean	43.25
Std Dev	12.08

Turn on : 24.6991

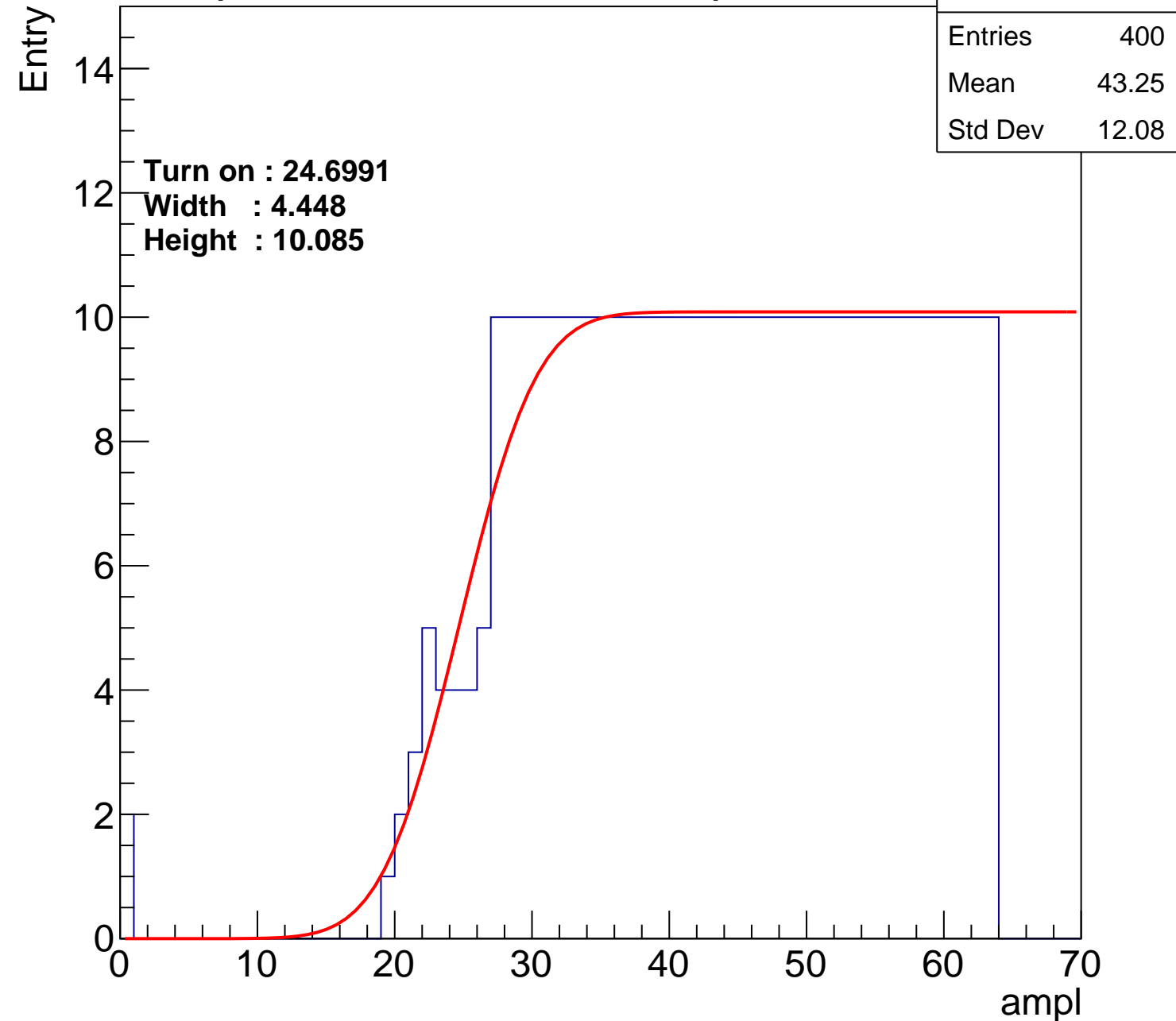
Width : 4.448

Height : 10.085

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch94

calib_packv5_042523_0143.root, FC#11, port A2

Entries	379
Mean	44.17
Std Dev	12.08

Turn on : 26.6964

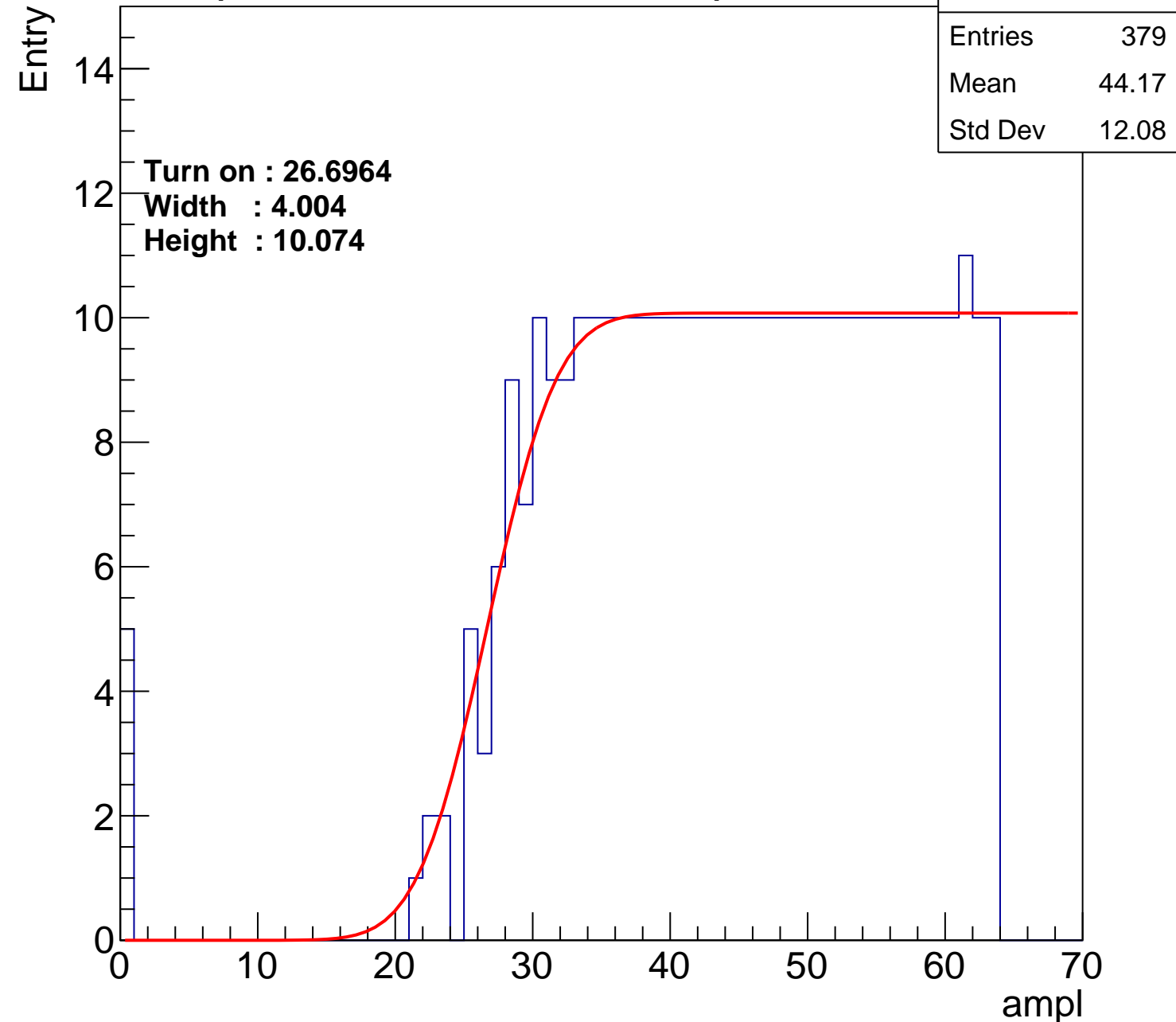
Width : 4.004

Height : 10.074

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch95

calib_packv5_042523_0143.root, FC#11, port A2

Entries	380
Mean	44.31
Std Dev	11.37

Turn on : 25.2793

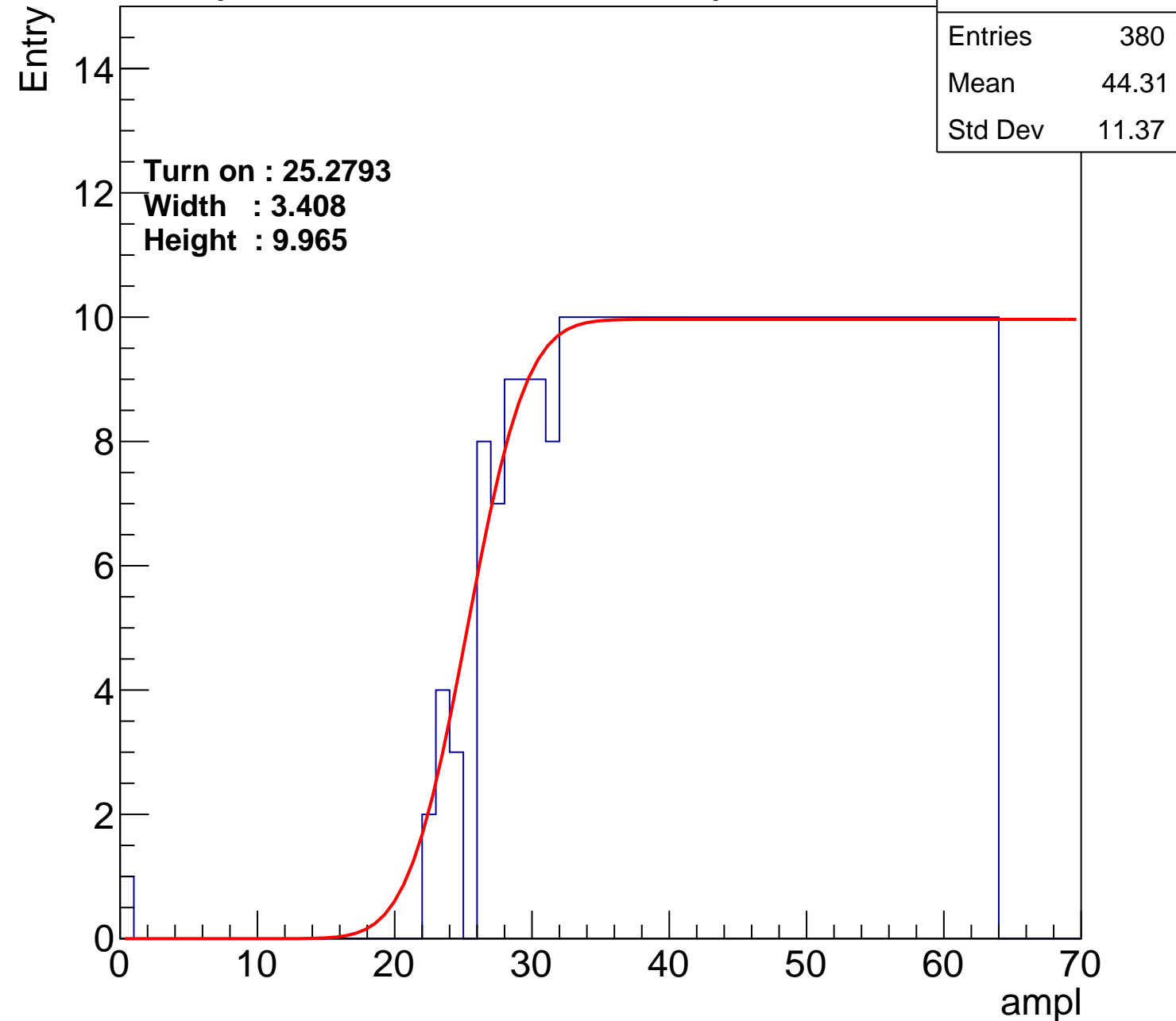
Width : 3.408

Height : 9.965

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch96

calib_packv5_042523_0143.root, FC#11, port A2

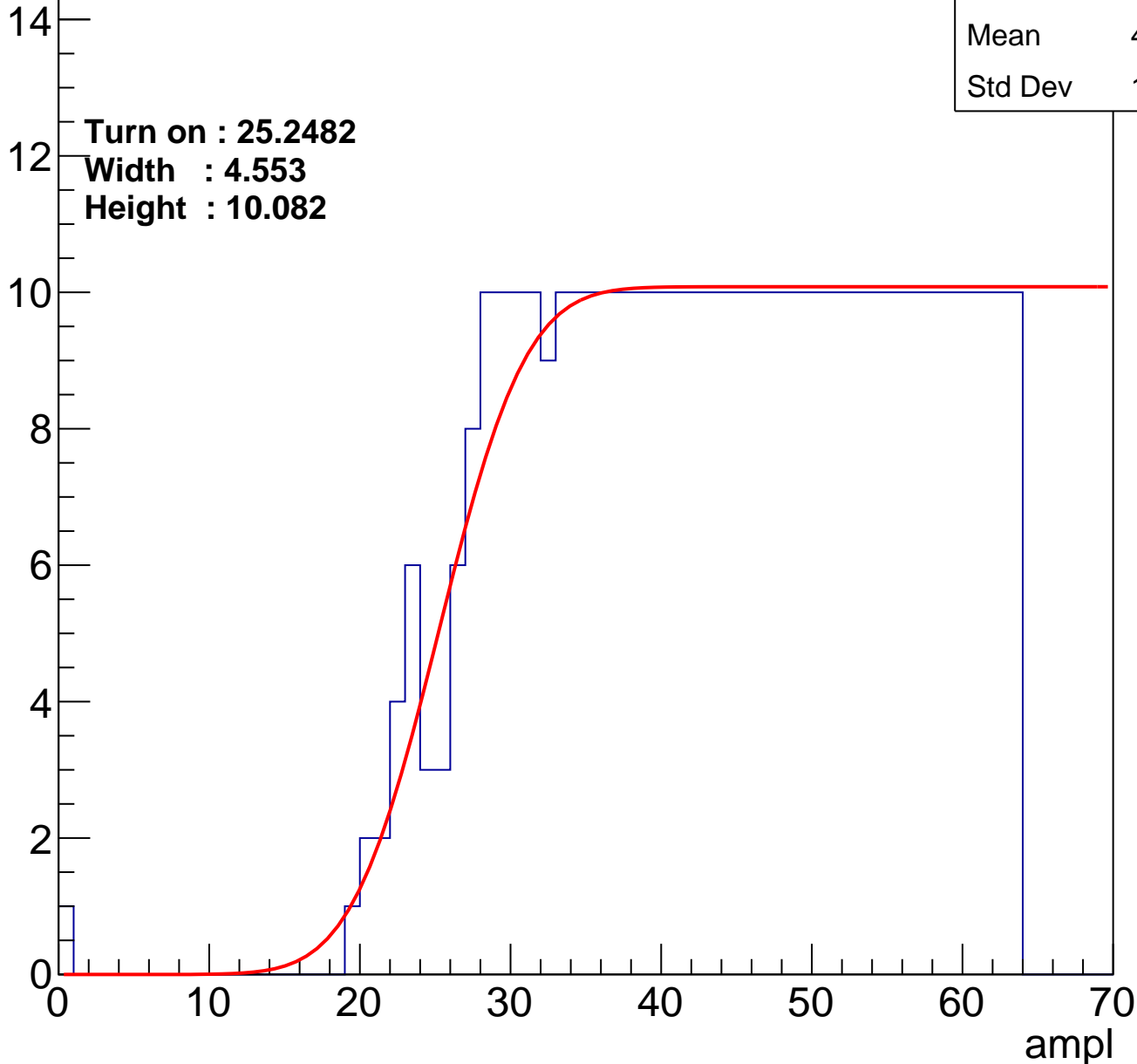
Entries	395
Mean	43.53
Std Dev	11.83

Turn on : 25.2482

Width : 4.553

Height : 10.082

Entry



B1L102S, U3-ch97

calib_packv5_042523_0143.root, FC#11, port A2

Entries	381
Mean	44.25
Std Dev	11.49

Turn on : 26.2509

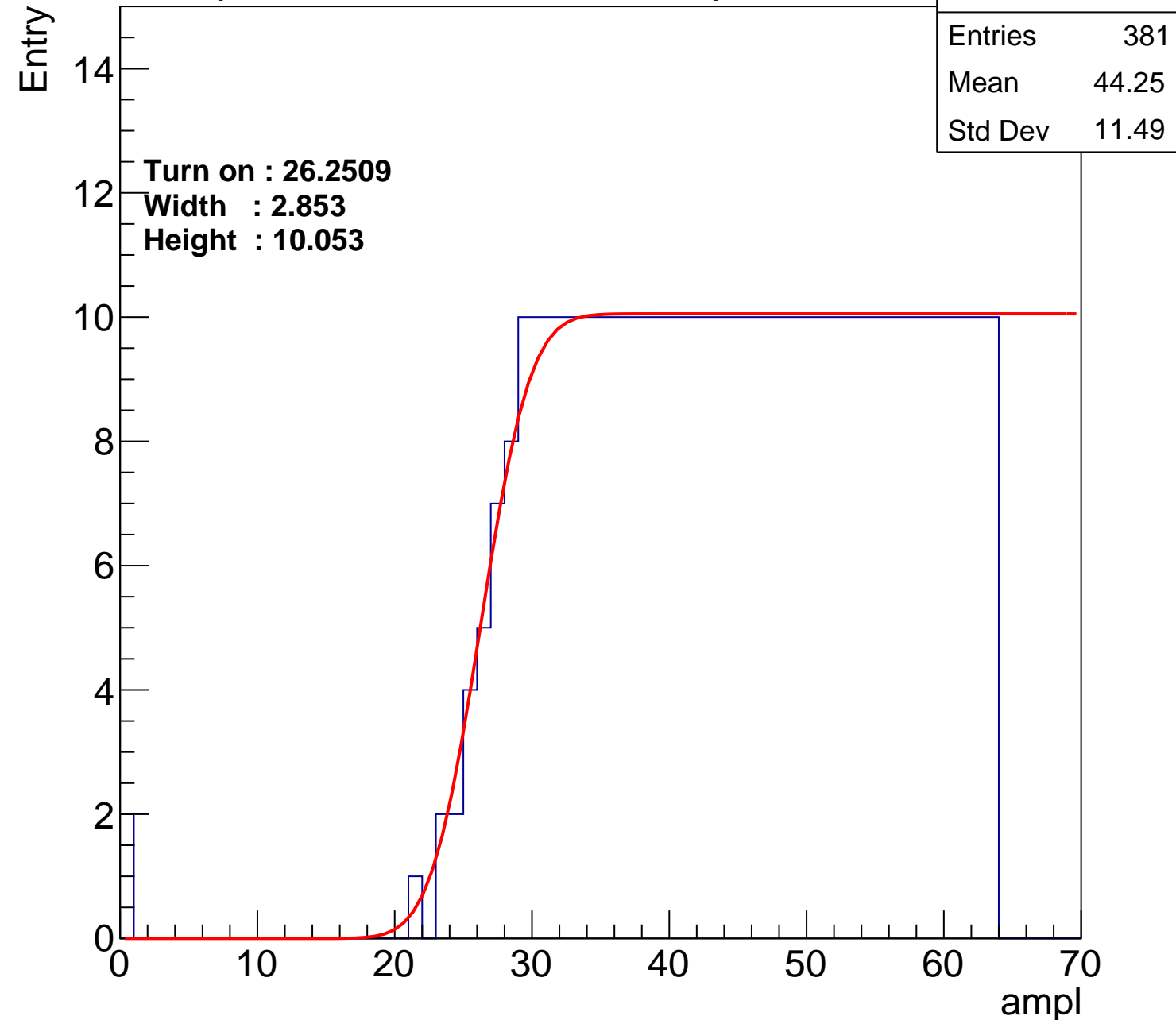
Width : 2.853

Height : 10.053

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch98

calib_packv5_042523_0143.root, FC#11, port A2

Entries	407
Mean	42.74
Std Dev	12.63

Turn on : 24.3413

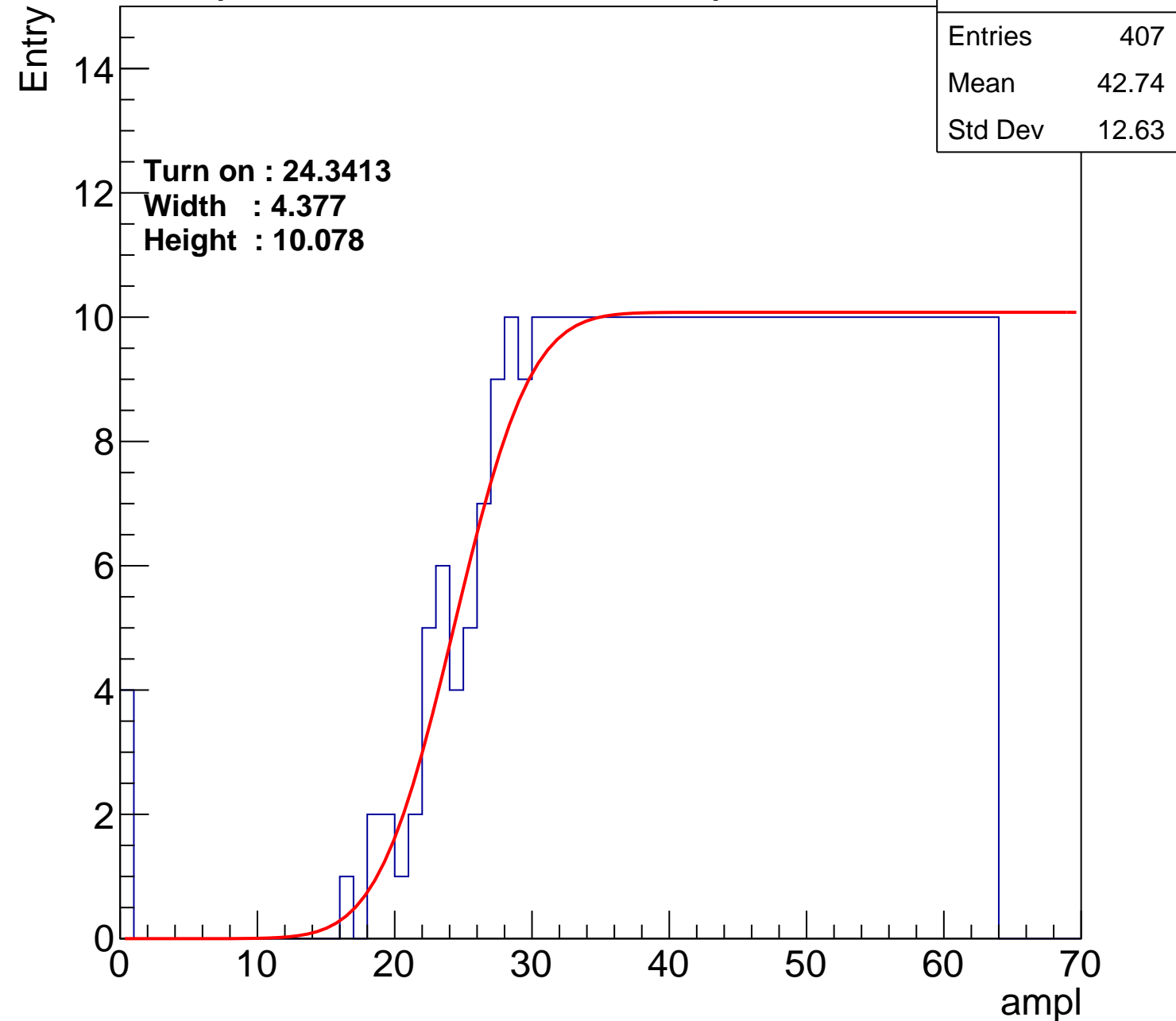
Width : 4.377

Height : 10.078

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch99

calib_packv5_042523_0143.root, FC#11, port A2

Entries	367
Mean	44.9
Std Dev	11.19

Turn on : 27.7291

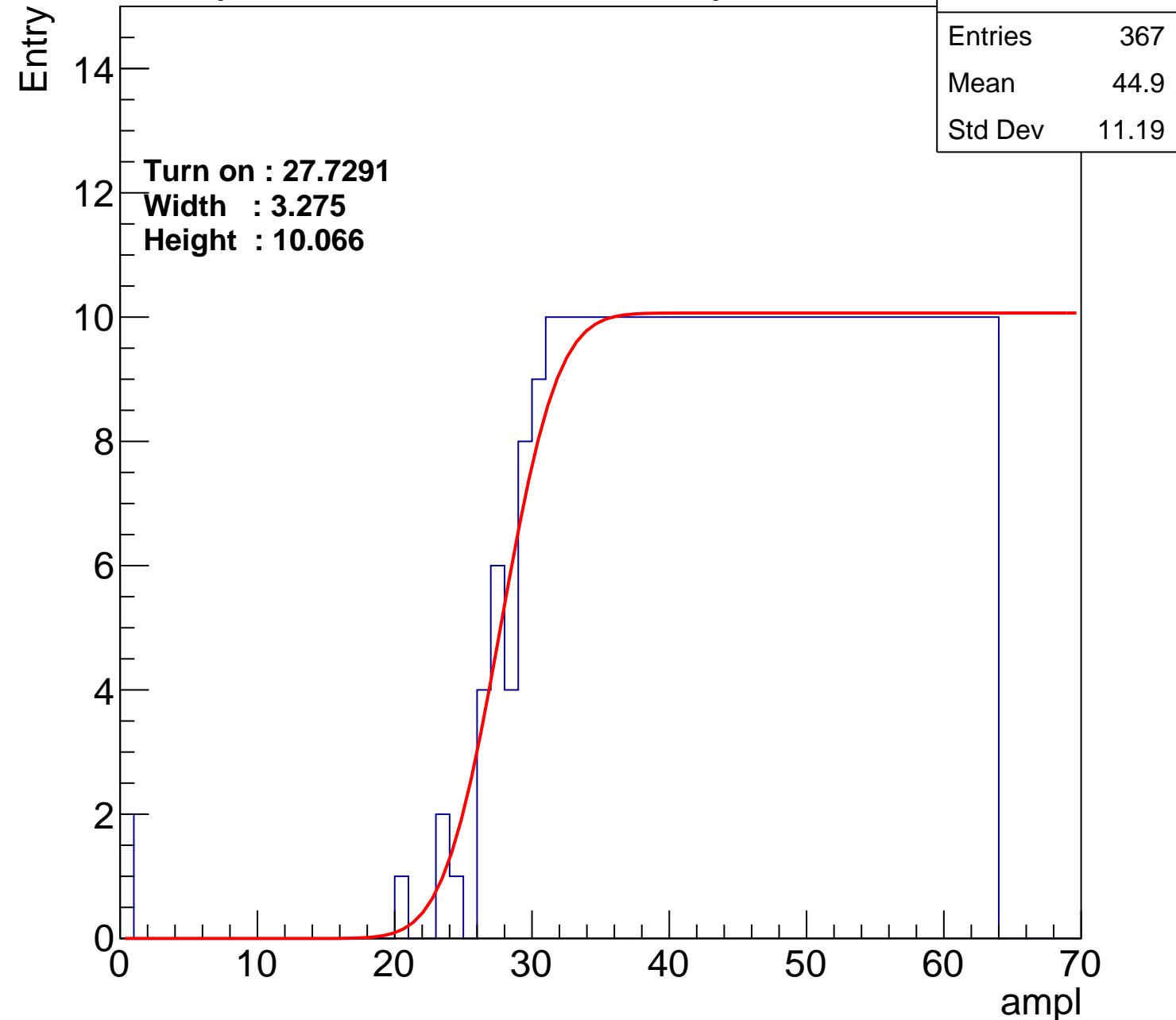
Width : 3.275

Height : 10.066

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch100

calib_packv5_042523_0143.root, FC#11, port A2

Entries	383
Mean	44.08
Std Dev	11.66

Turn on : 26.7398

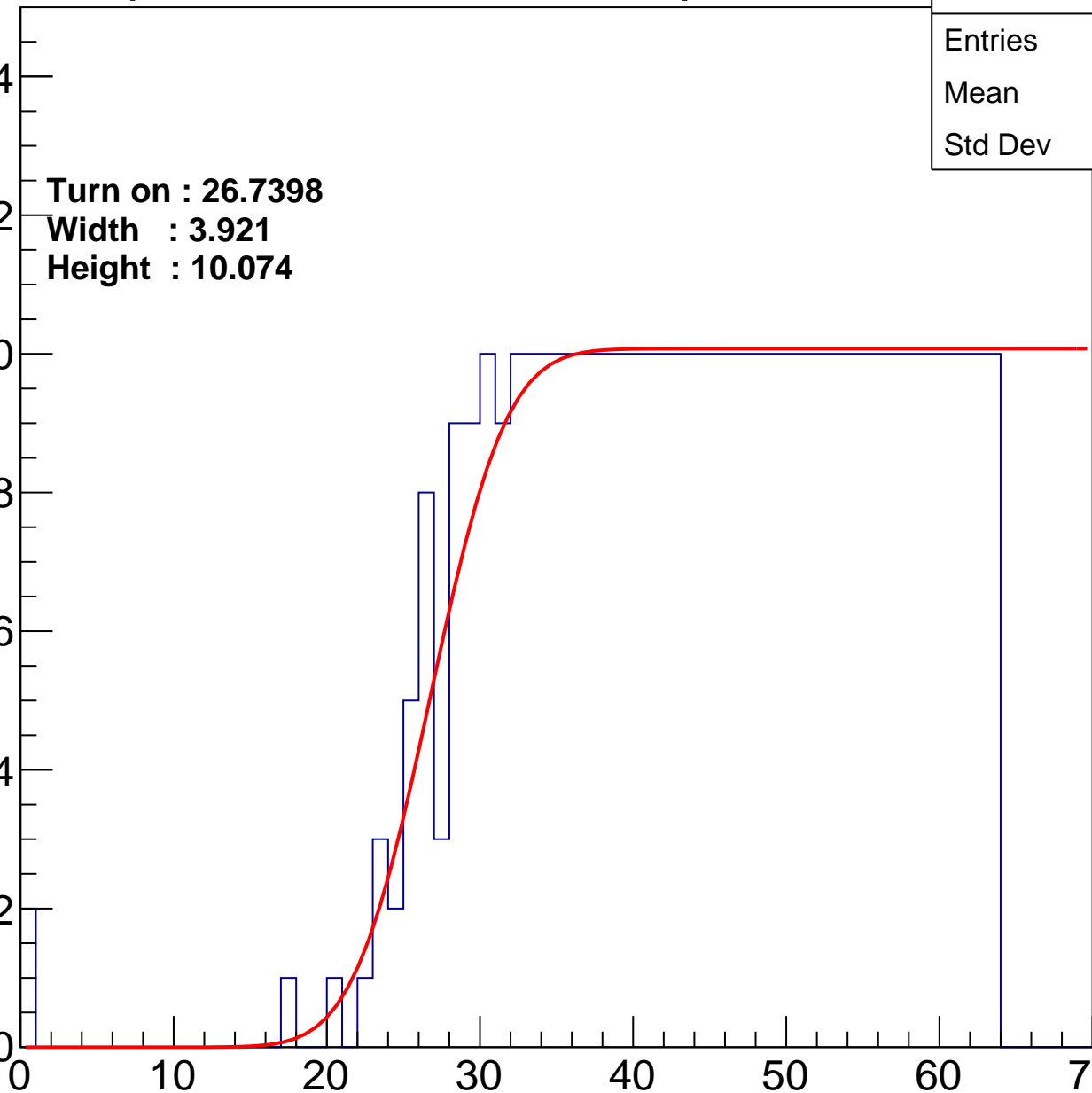
Width : 3.921

Height : 10.074

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch101

calib_packv5_042523_0143.root, FC#11, port A2

Entries	392
Mean	43.73
Std Dev	11.66

Turn on : 25.2117

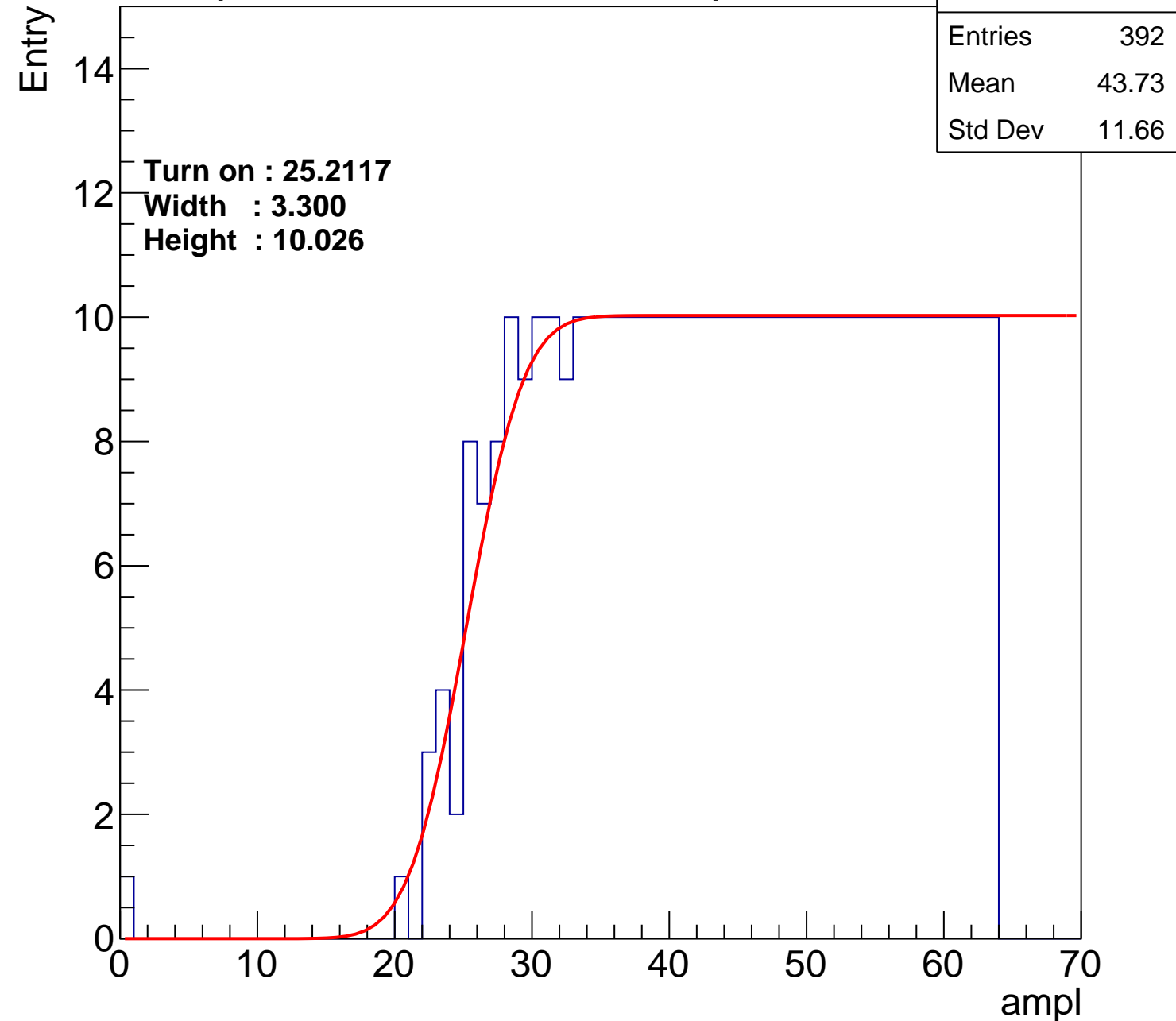
Width : 3.300

Height : 10.026

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch102

calib_packv5_042523_0143.root, FC#11, port A2

Entries	384
Mean	43.91
Std Dev	12.01

Turn on : 26.6537

Width : 3.876

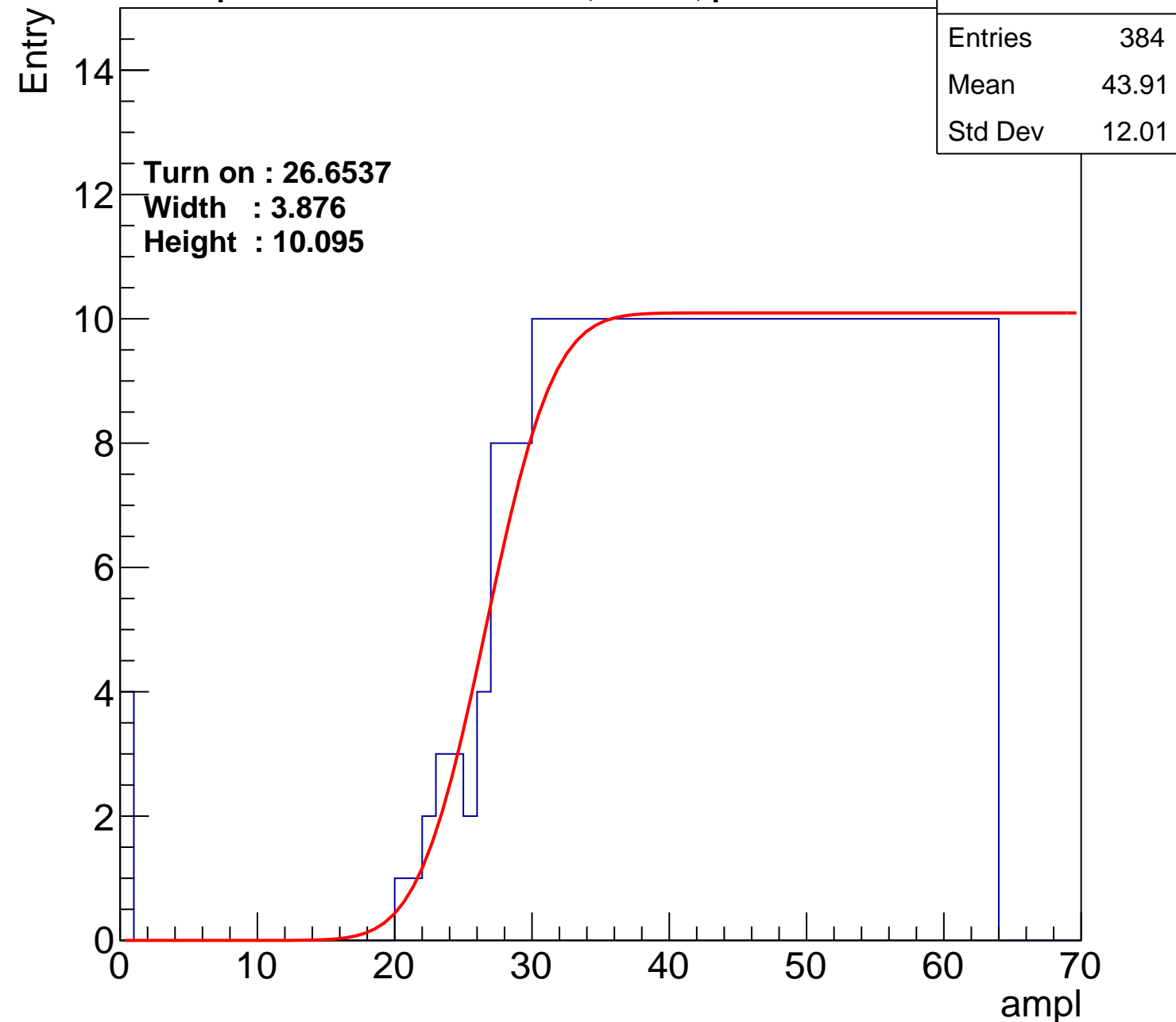
Height : 10.095

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L102S, U3-ch103

calib_packv5_042523_0143.root, FC#11, port A2

Entries	373
Mean	44.54
Std Dev	11.51

Turn on : 27.2823

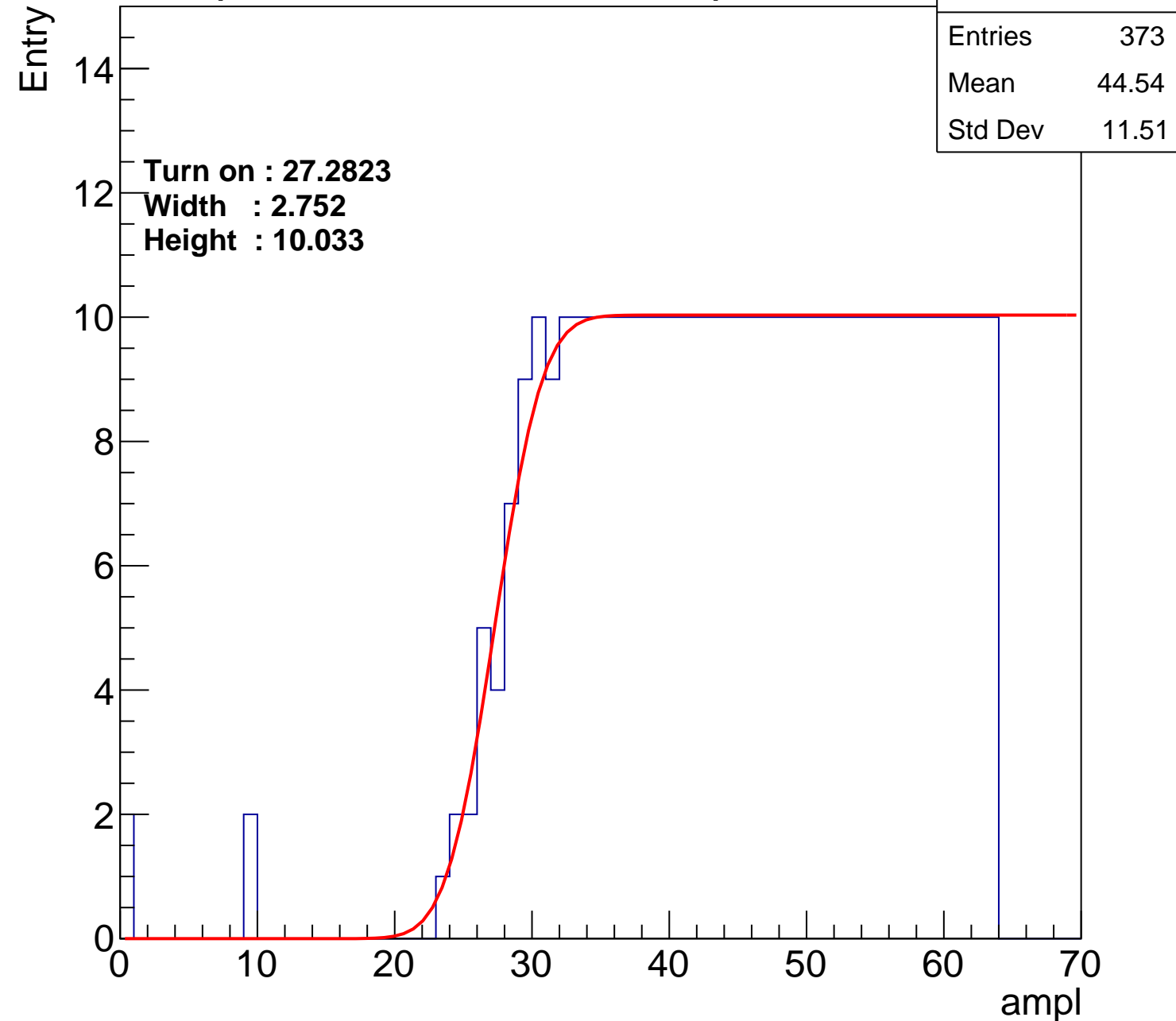
Width : 2.752

Height : 10.033

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch104

calib_packv5_042523_0143.root, FC#11, port A2

Entries	396
Mean	43.36
Std Dev	12.24

Turn on : 25.0730

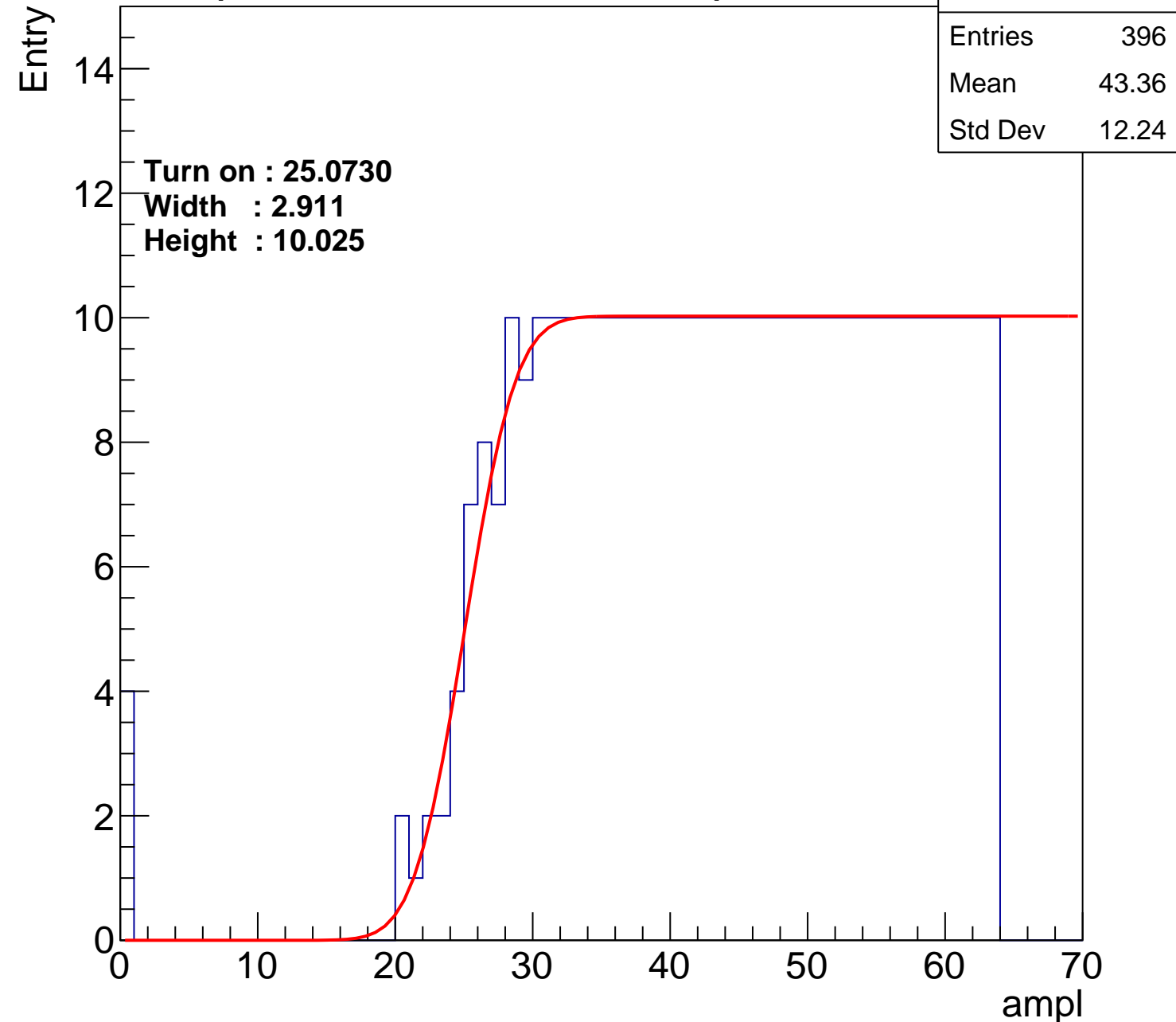
Width : 2.911

Height : 10.025

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch105

calib_packv5_042523_0143.root, FC#11, port A2

Entries	386
Mean	43.99
Std Dev	11.55

Turn on : 25.0685

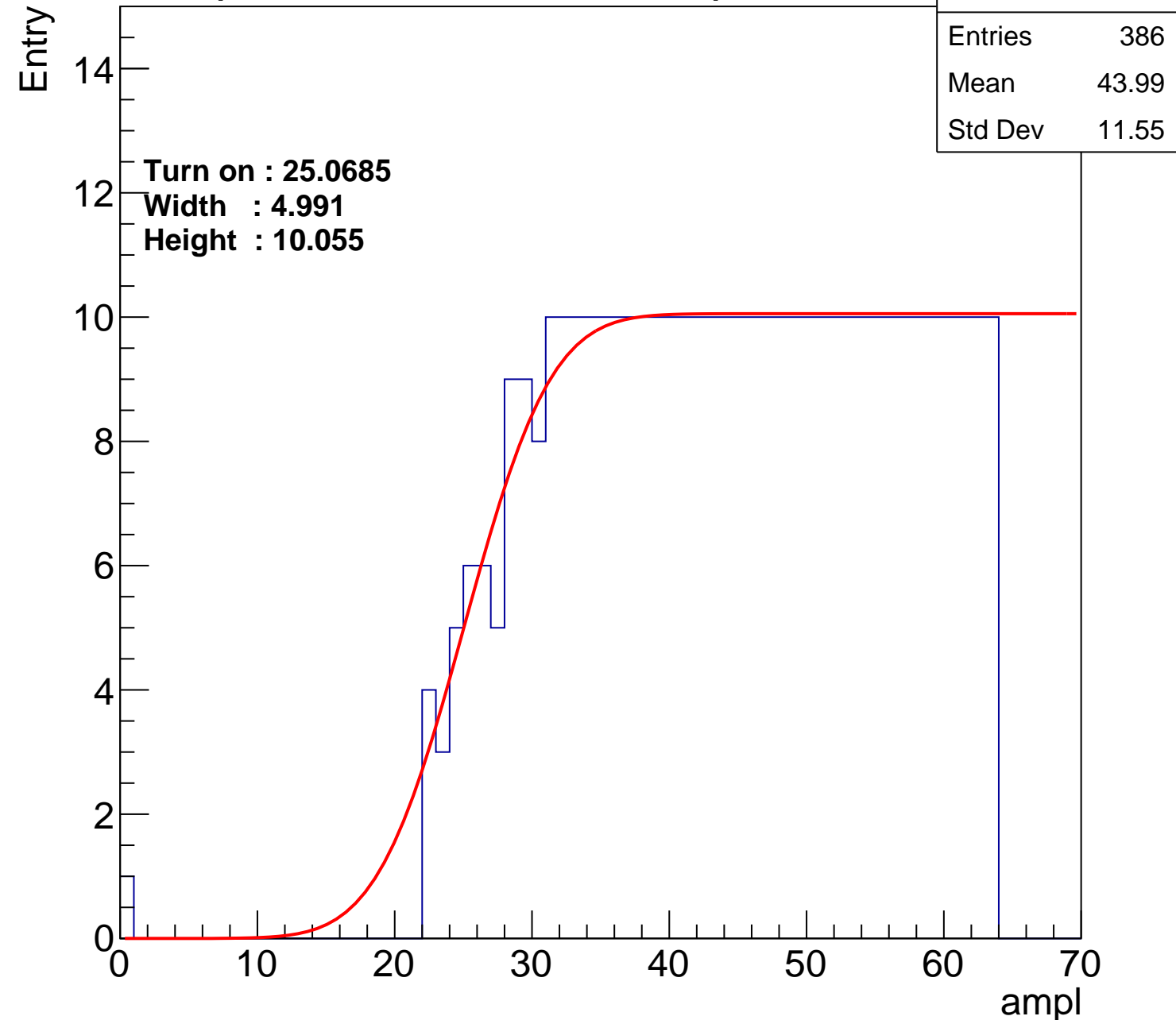
Width : 4.991

Height : 10.055

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch106

calib_packv5_042523_0143.root, FC#11, port A2

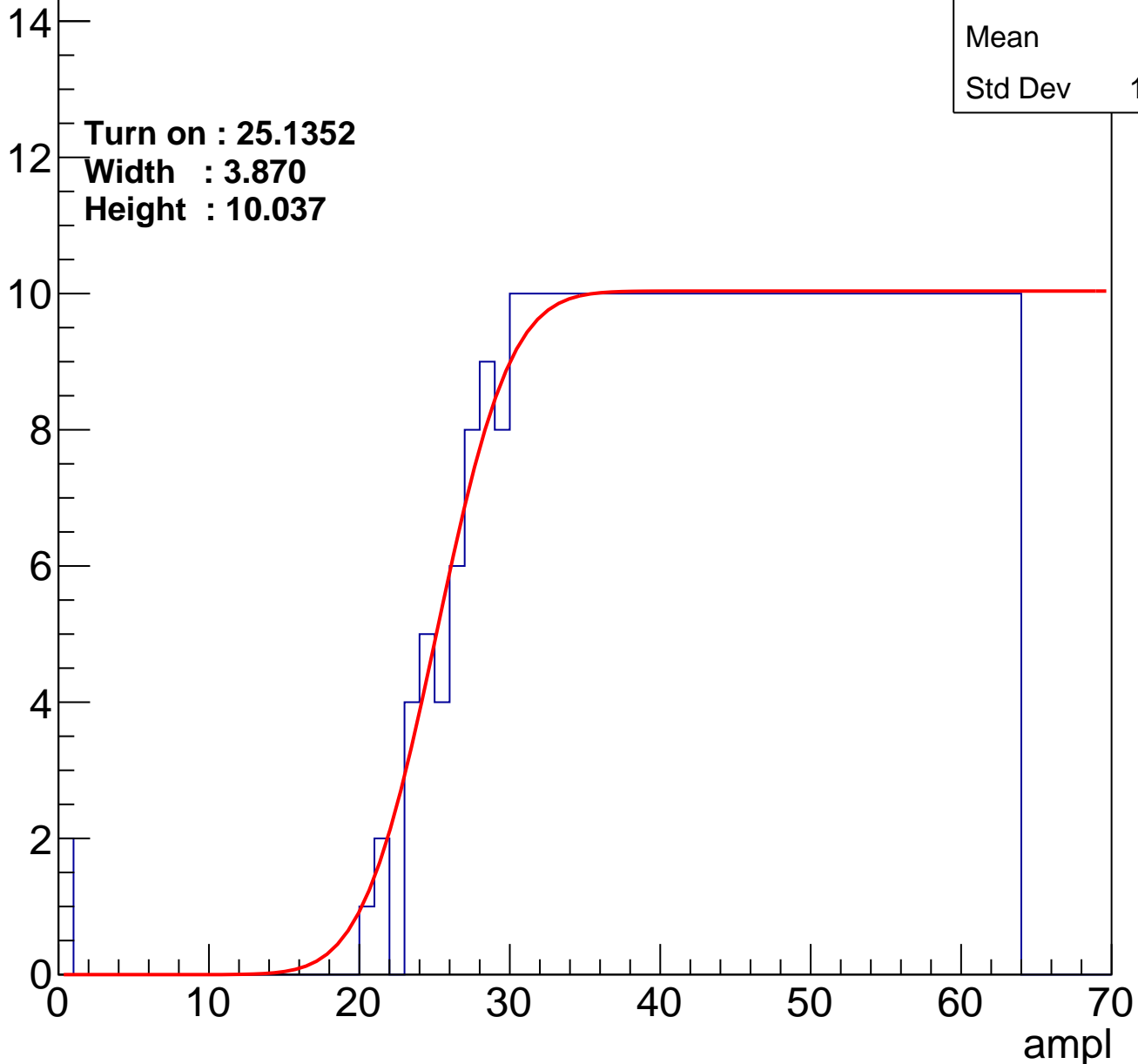
Entries	389
Mean	43.8
Std Dev	11.77

Turn on : 25.1352

Width : 3.870

Height : 10.037

Entry



B1L102S, U3-ch107

calib_packv5_042523_0143.root, FC#11, port A2

Entries	371
Mean	44.78
Std Dev	11.07

Turn on : 27.2008

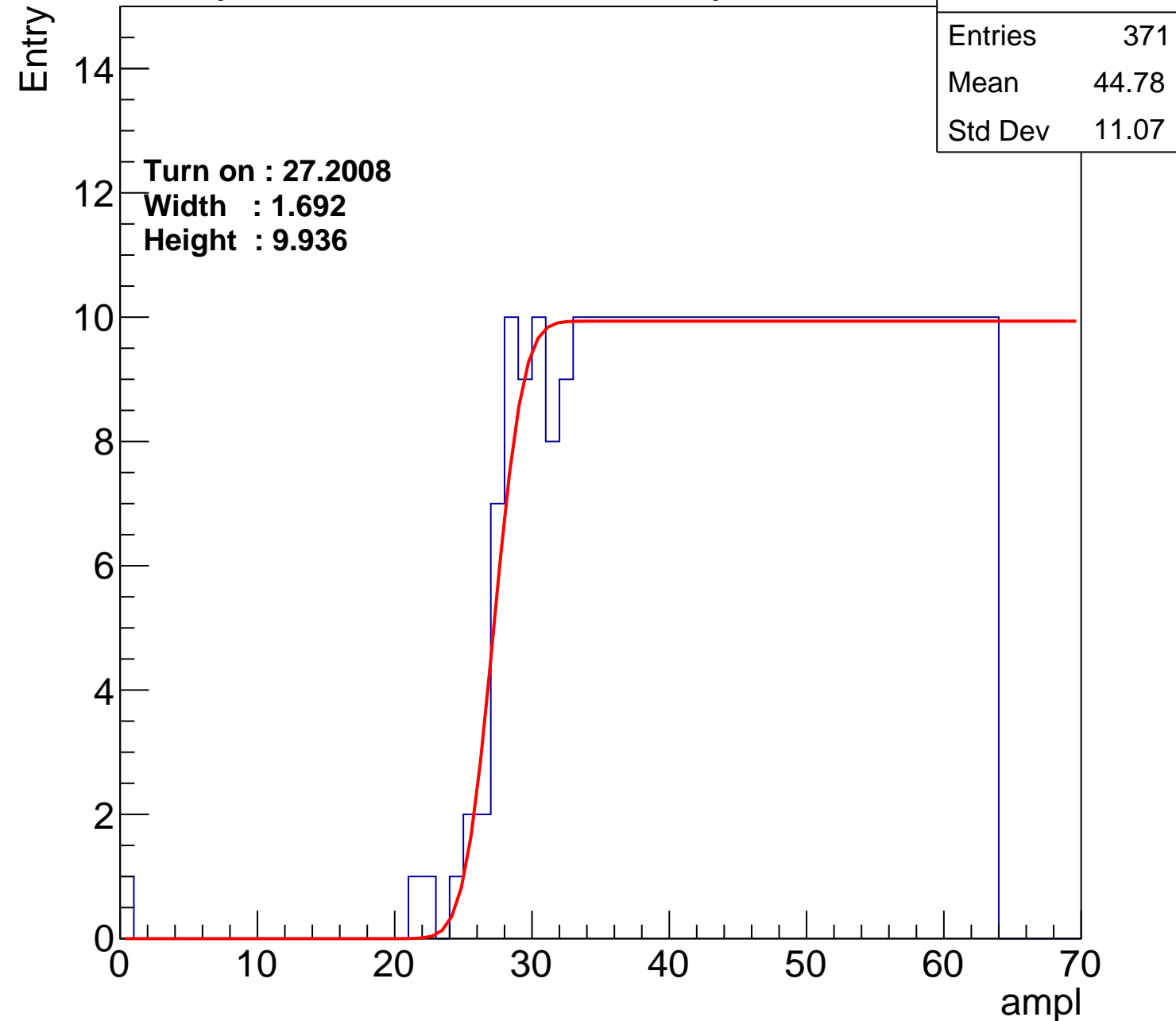
Width : 1.692

Height : 9.936

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch108

calib_packv5_042523_0143.root, FC#11, port A2

Entries	375
Mean	44.58
Std Dev	11.21

Turn on : 27.0086

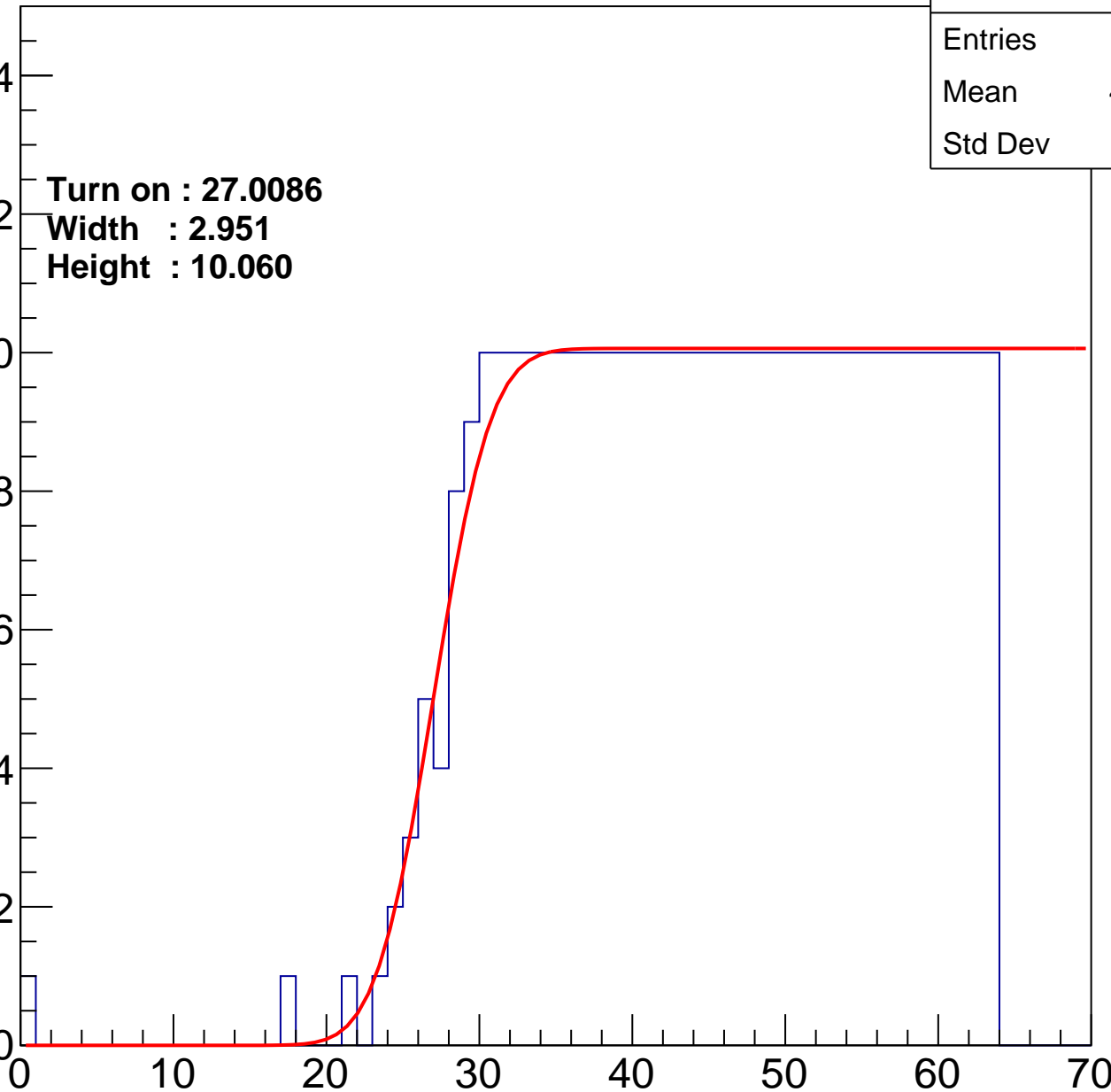
Width : 2.951

Height : 10.060

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch109

calib_packv5_042523_0143.root, FC#11, port A2

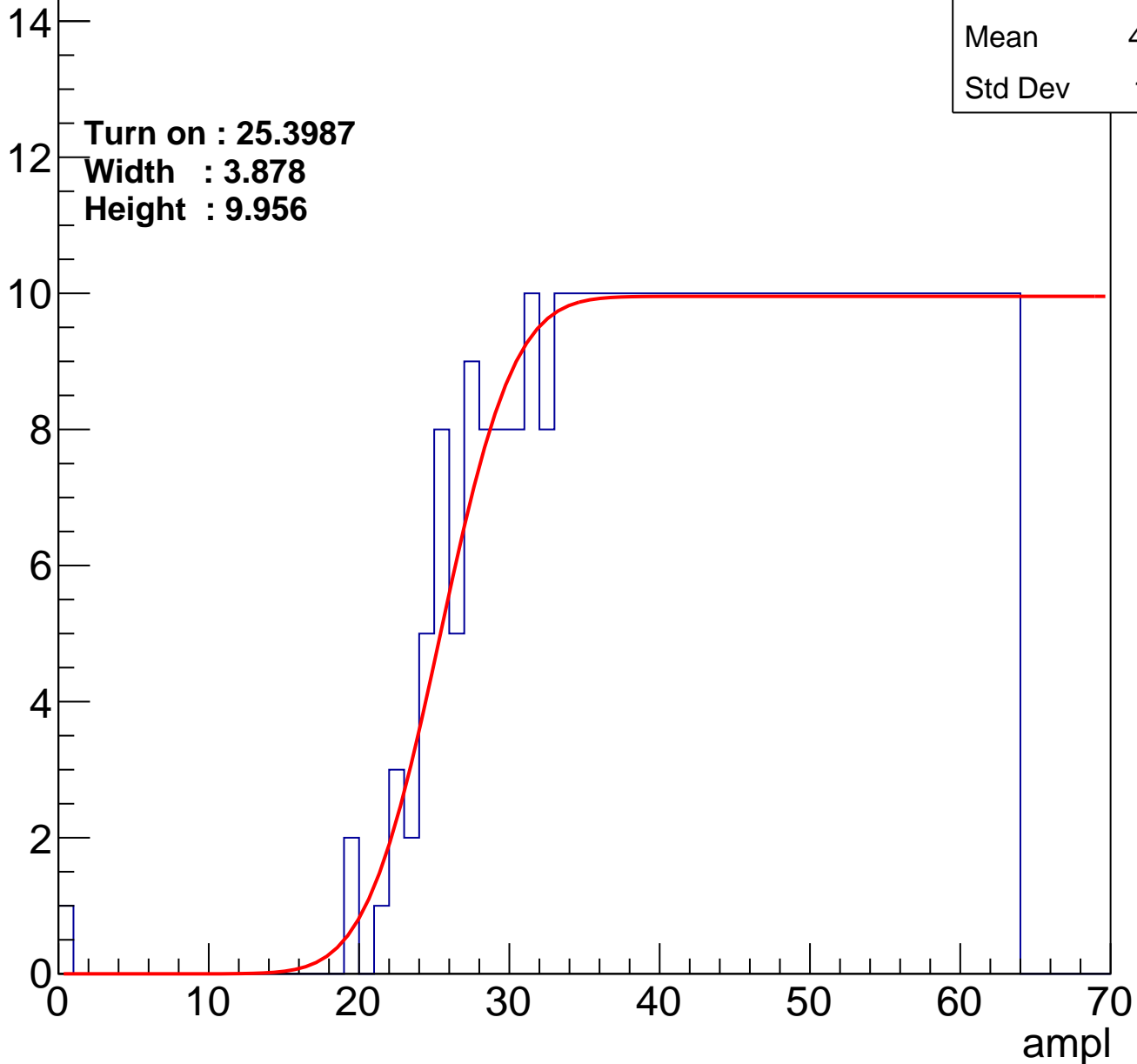
Entries	388
Mean	43.83
Std Dev	11.71

Turn on : 25.3987

Width : 3.878

Height : 9.956

Entry



B1L102S, U3-ch110

calib_packv5_042523_0143.root, FC#11, port A2

Entries	371
Mean	44.76
Std Dev	11.1

Turn on : 26.6400

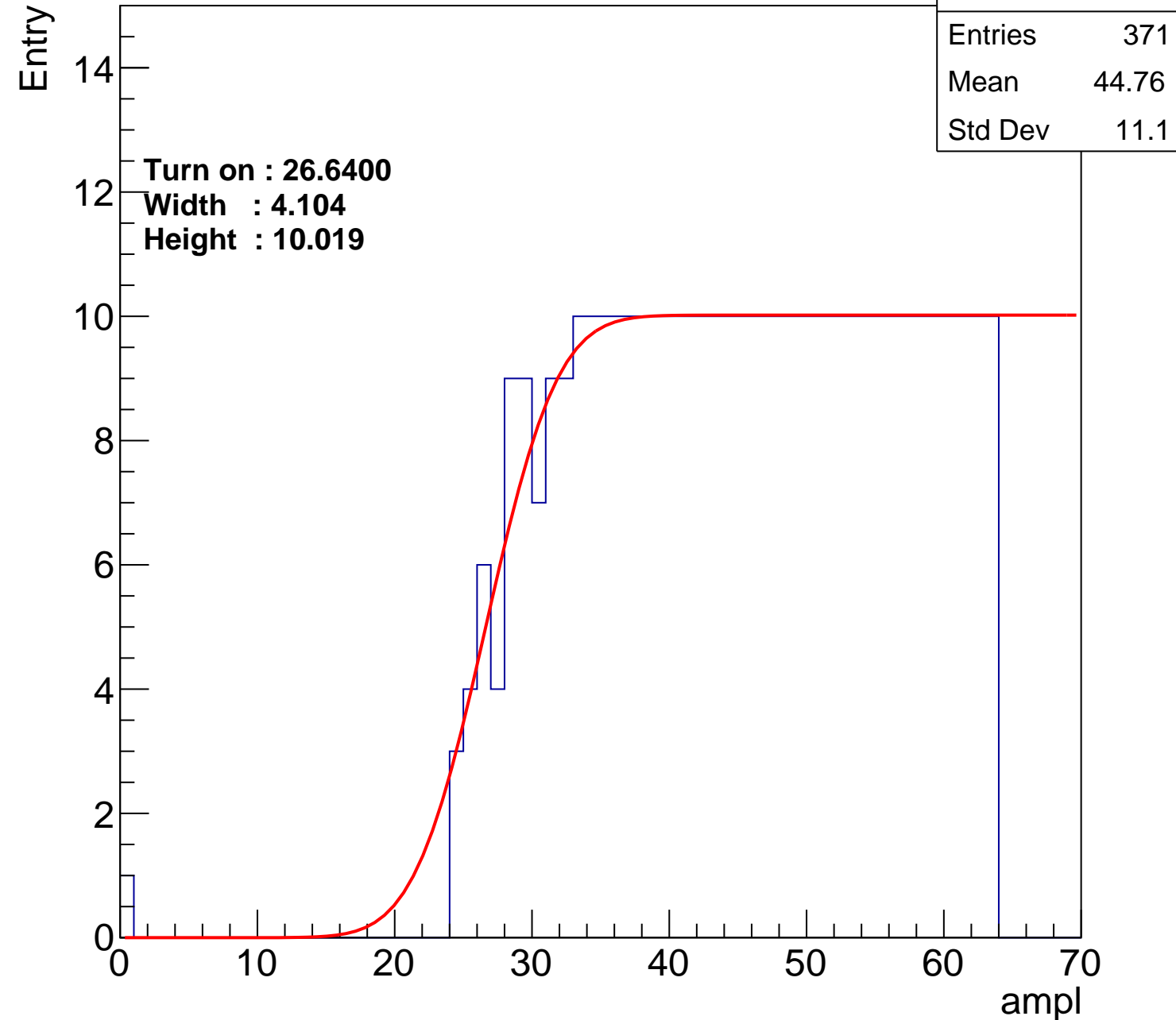
Width : 4.104

Height : 10.019

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch111

calib_packv5_042523_0143.root, FC#11, port A2

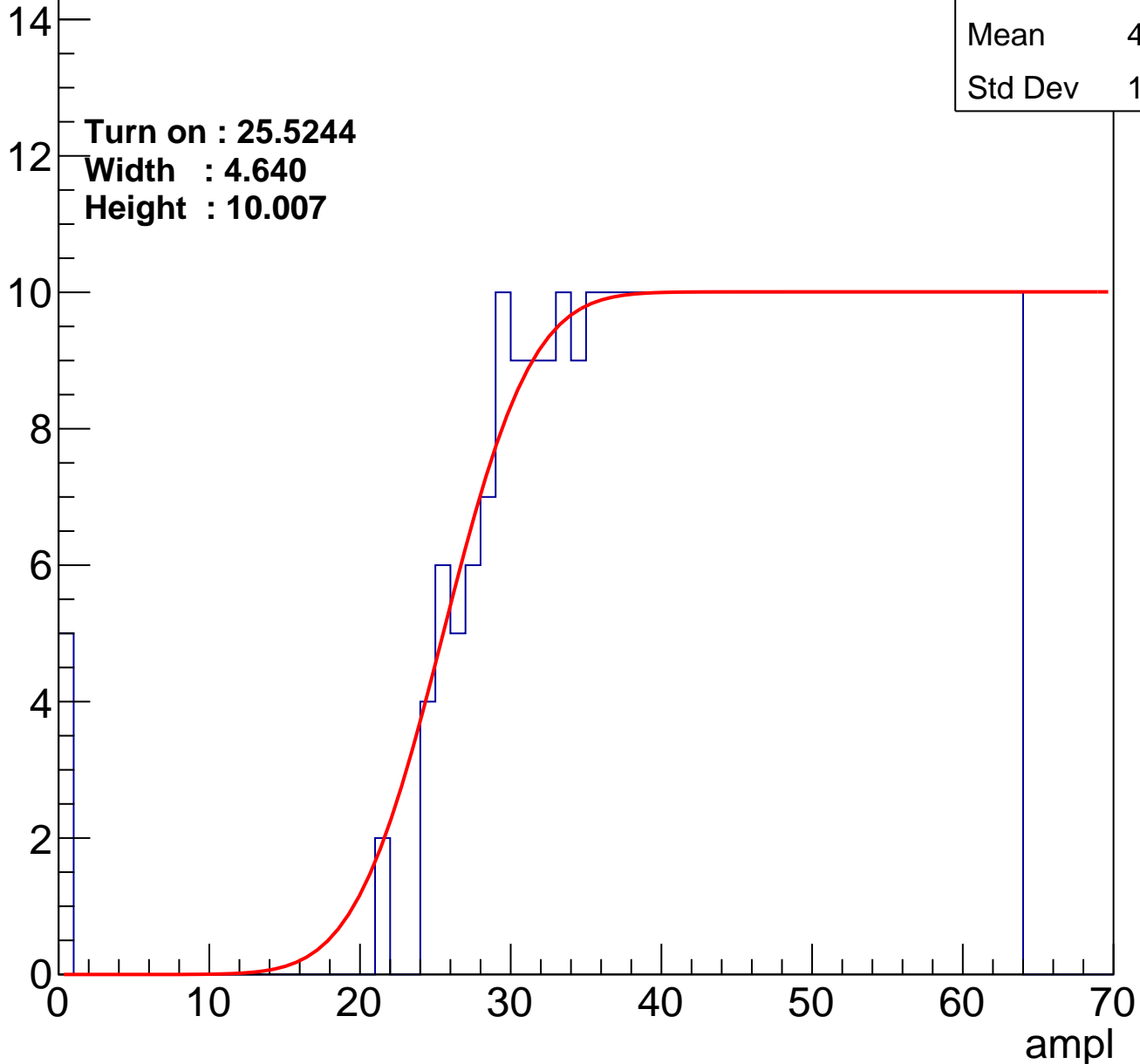
Entries	381
Mean	43.96
Std Dev	12.14

Turn on : 25.5244

Width : 4.640

Height : 10.007

Entry



B1L102S, U3-ch112

calib_packv5_042523_0143.root, FC#11, port A2

Entries	392
Mean	43.53
Std Dev	12.18

Turn on : 26.0450

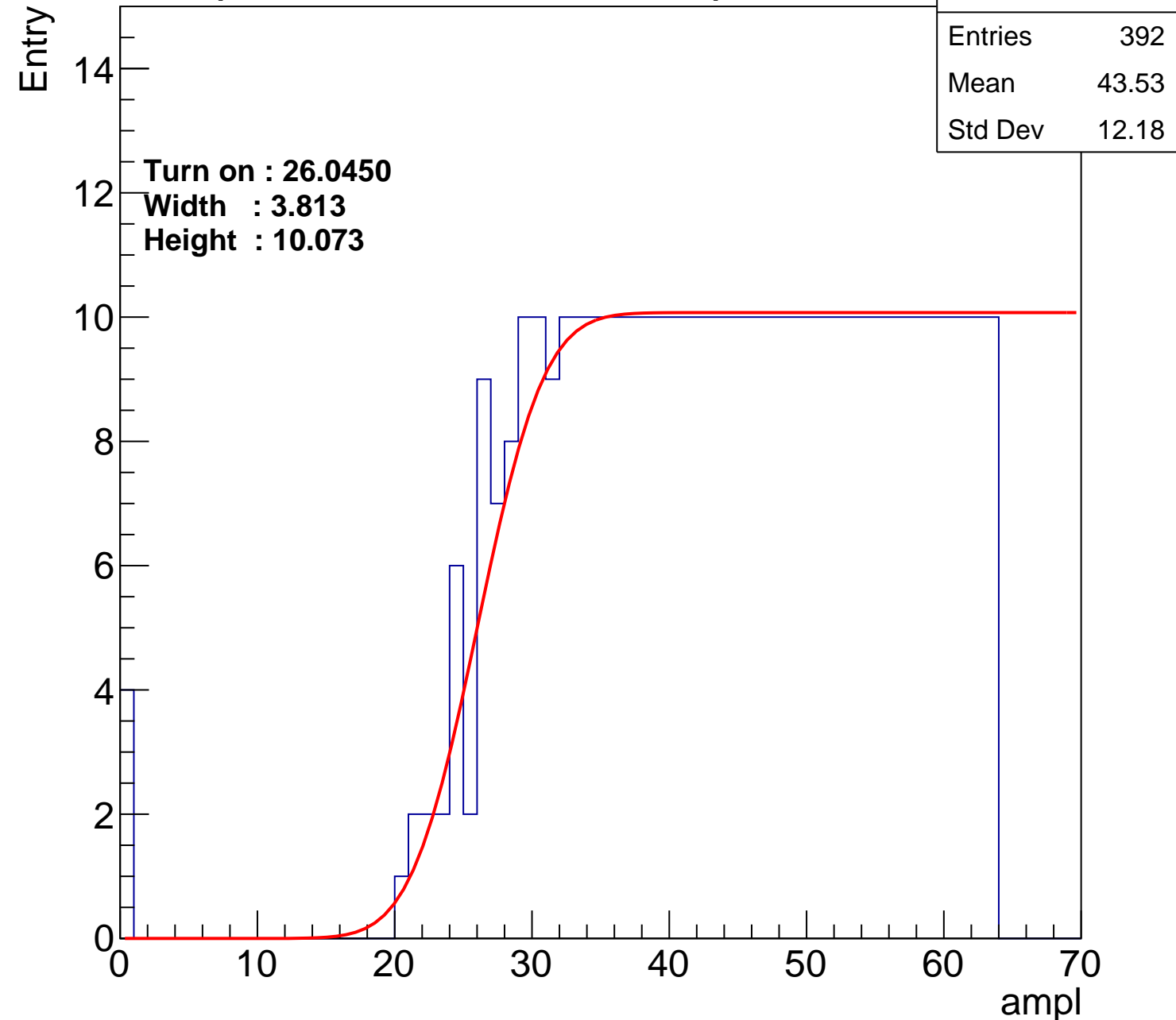
Width : 3.813

Height : 10.073

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch113

calib_packv5_042523_0143.root, FC#11, port A2

Entries	373
Mean	44.43
Std Dev	11.79

Turn on : 27.8855

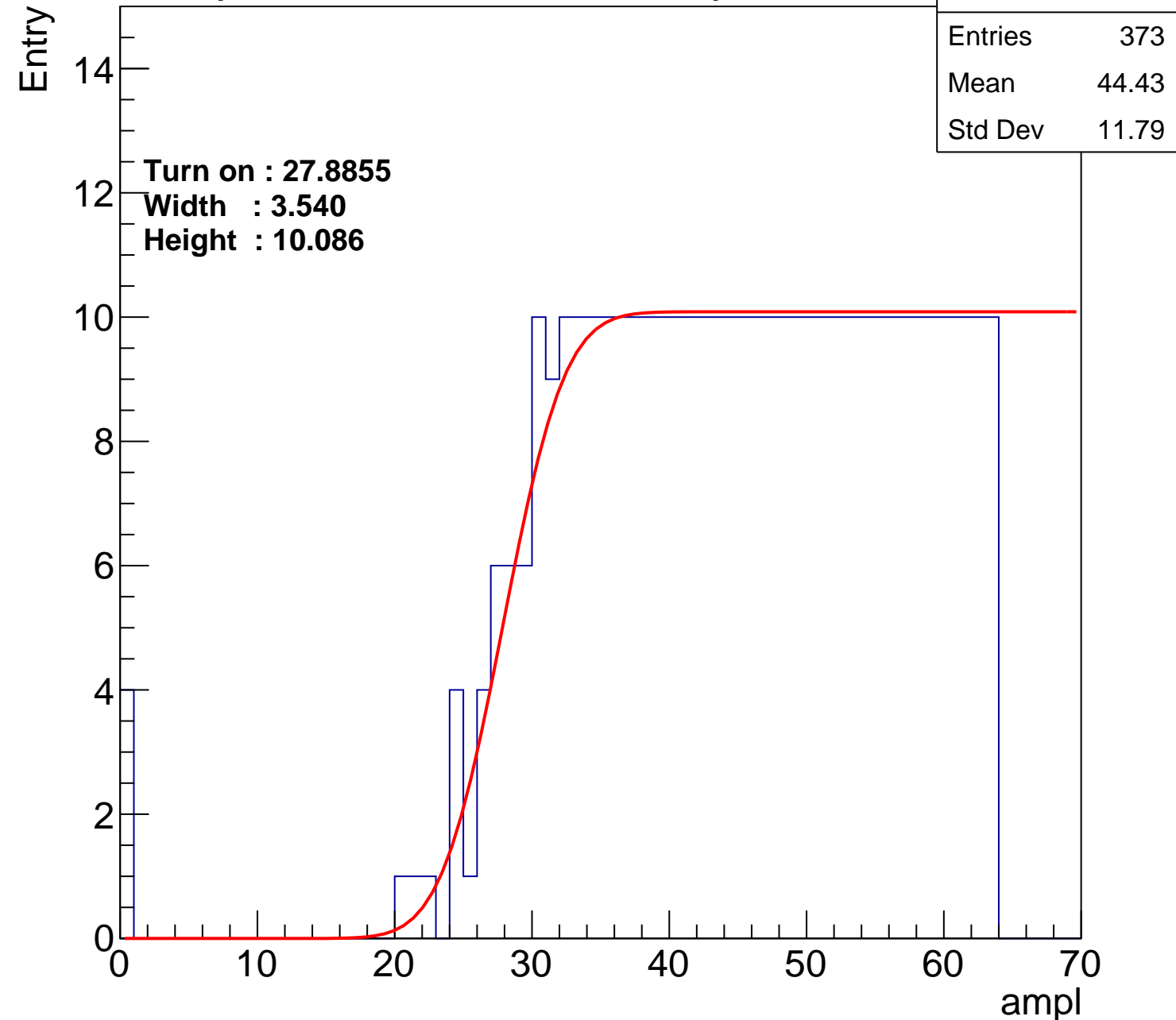
Width : 3.540

Height : 10.086

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch114

calib_packv5_042523_0143.root, FC#11, port A2

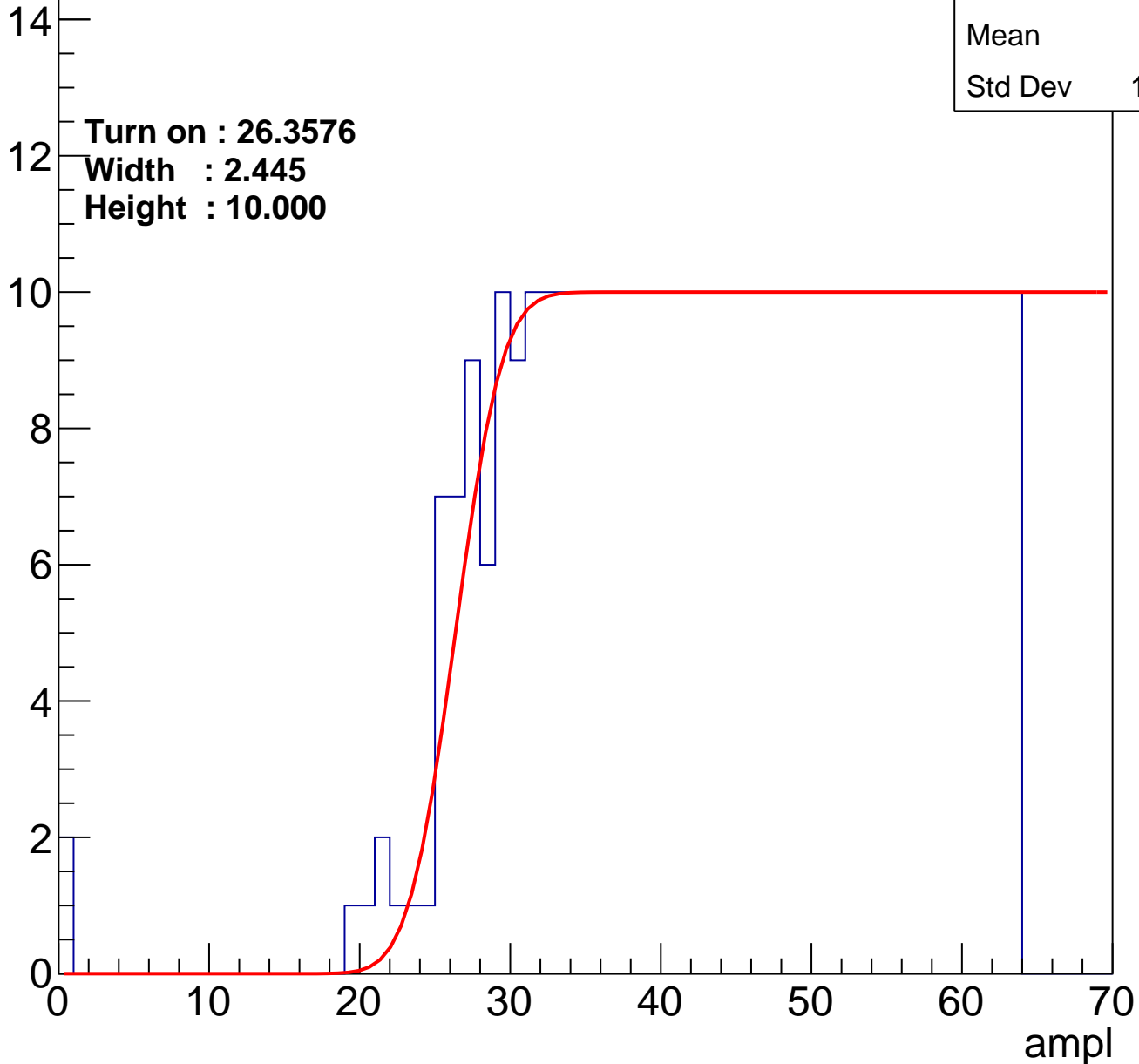
Entries	387
Mean	43.9
Std Dev	11.73

Turn on : 26.3576

Width : 2.445

Height : 10.000

Entry



B1L102S, U3-ch115

calib_packv5_042523_0143.root, FC#11, port A2

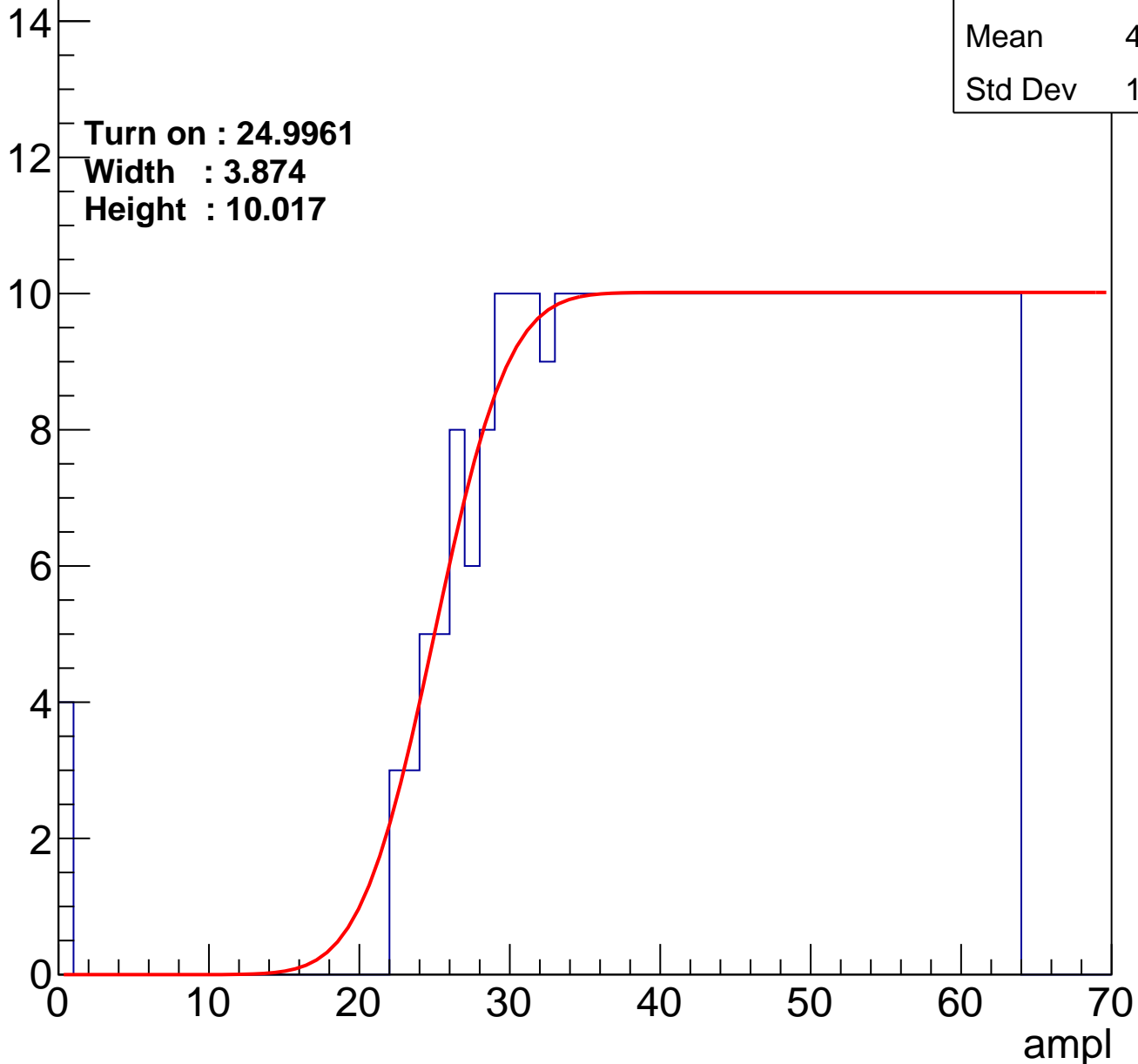
Entries	391
Mean	43.59
Std Dev	12.14

Turn on : 24.9961

Width : 3.874

Height : 10.017

Entry



B1L102S, U3-ch116

calib_packv5_042523_0143.root, FC#11, port A2

Entries	404
Mean	43.02
Std Dev	12.29

Turn on : 24.5230

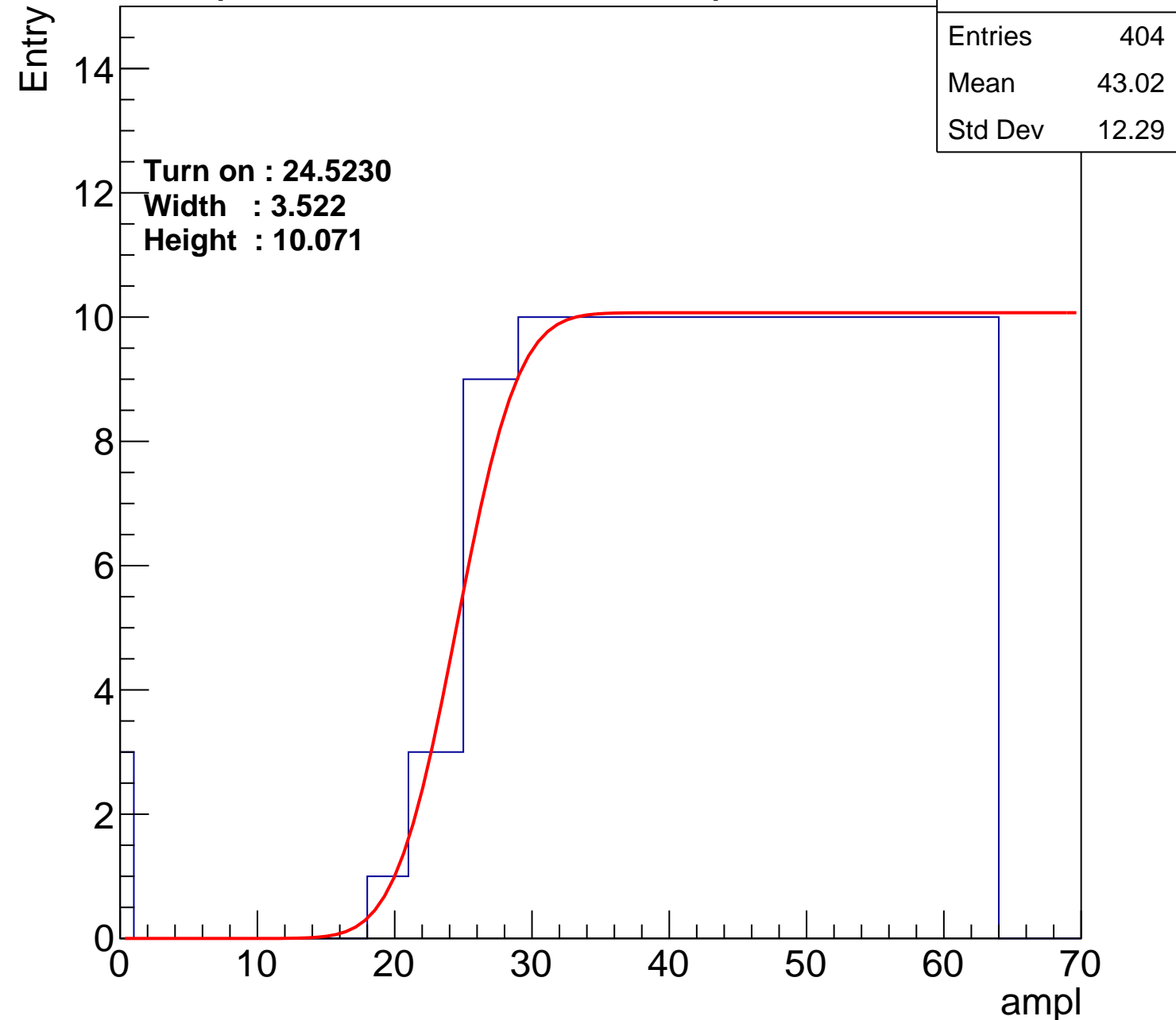
Width : 3.522

Height : 10.071

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch117

calib_packv5_042523_0143.root, FC#11, port A2

Entries	384
Mean	44.05
Std Dev	11.64

Turn on : 25.8358

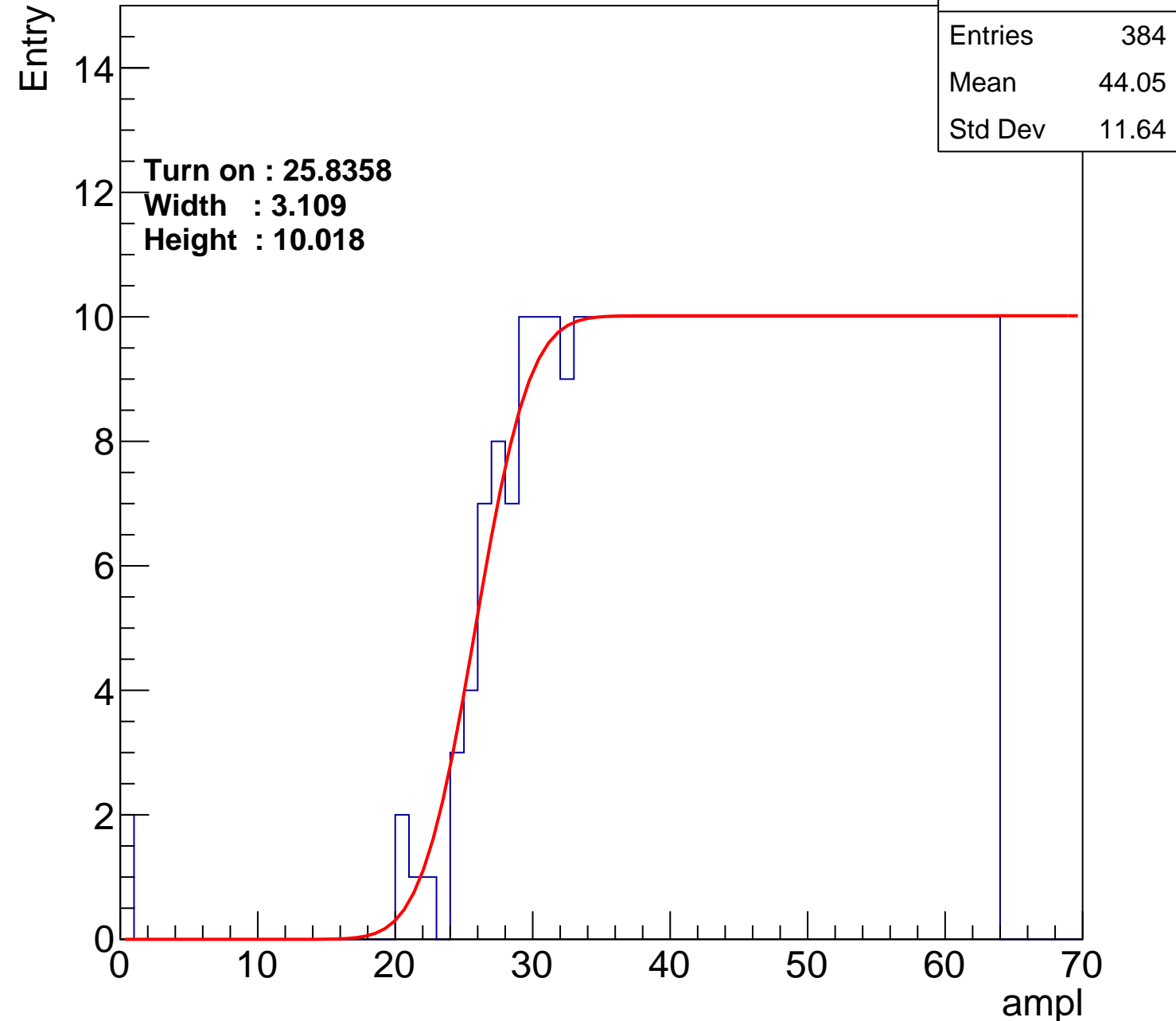
Width : 3.109

Height : 10.018

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch118

calib_packv5_042523_0143.root, FC#11, port A2

Entries	397
Mean	43.3
Std Dev	12.22

Turn on : 25.5888

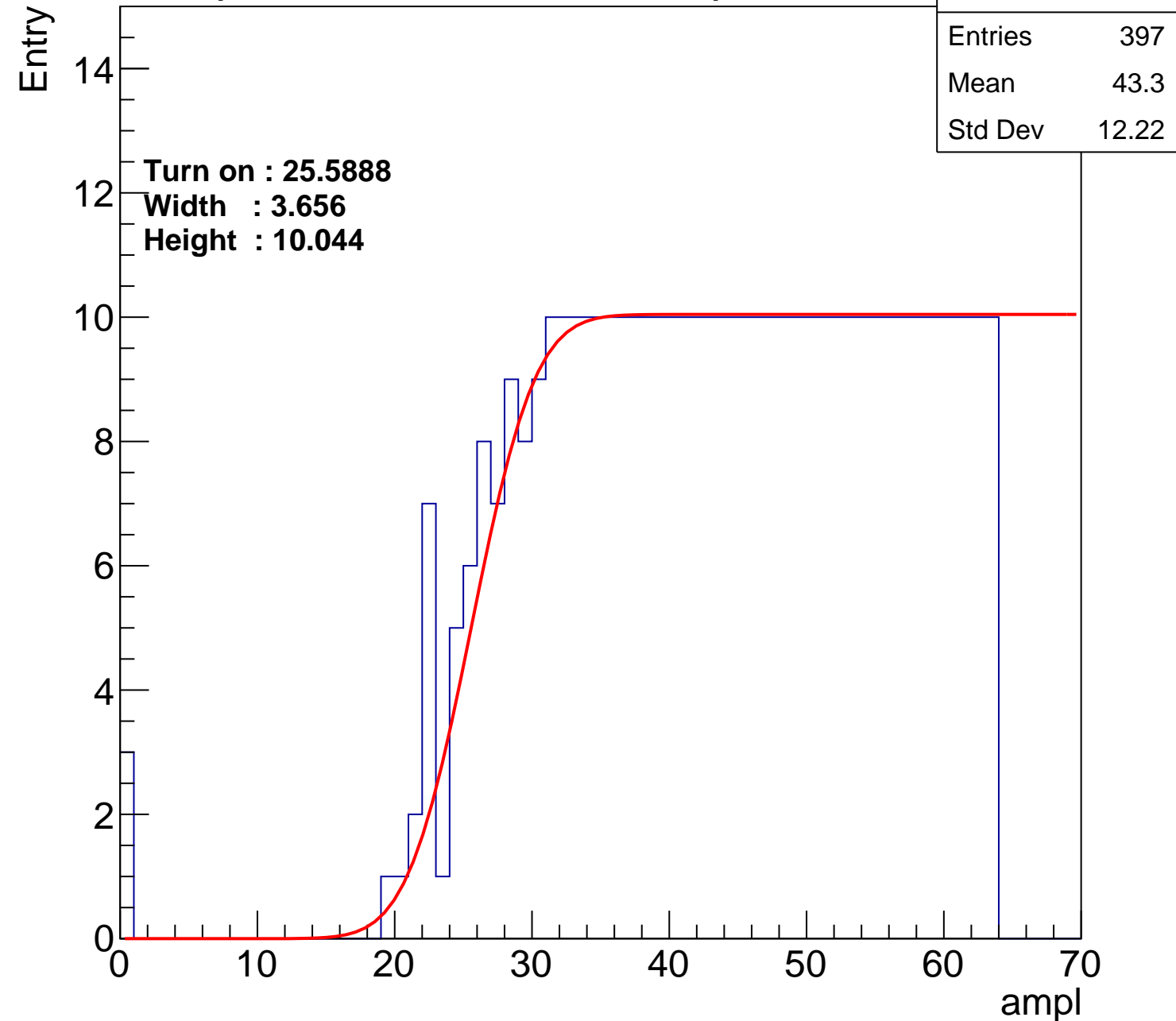
Width : 3.656

Height : 10.044

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch119

calib_packv5_042523_0143.root, FC#11, port A2

Entries	393
Mean	43.48
Std Dev	12.19

Turn on : 25.2455

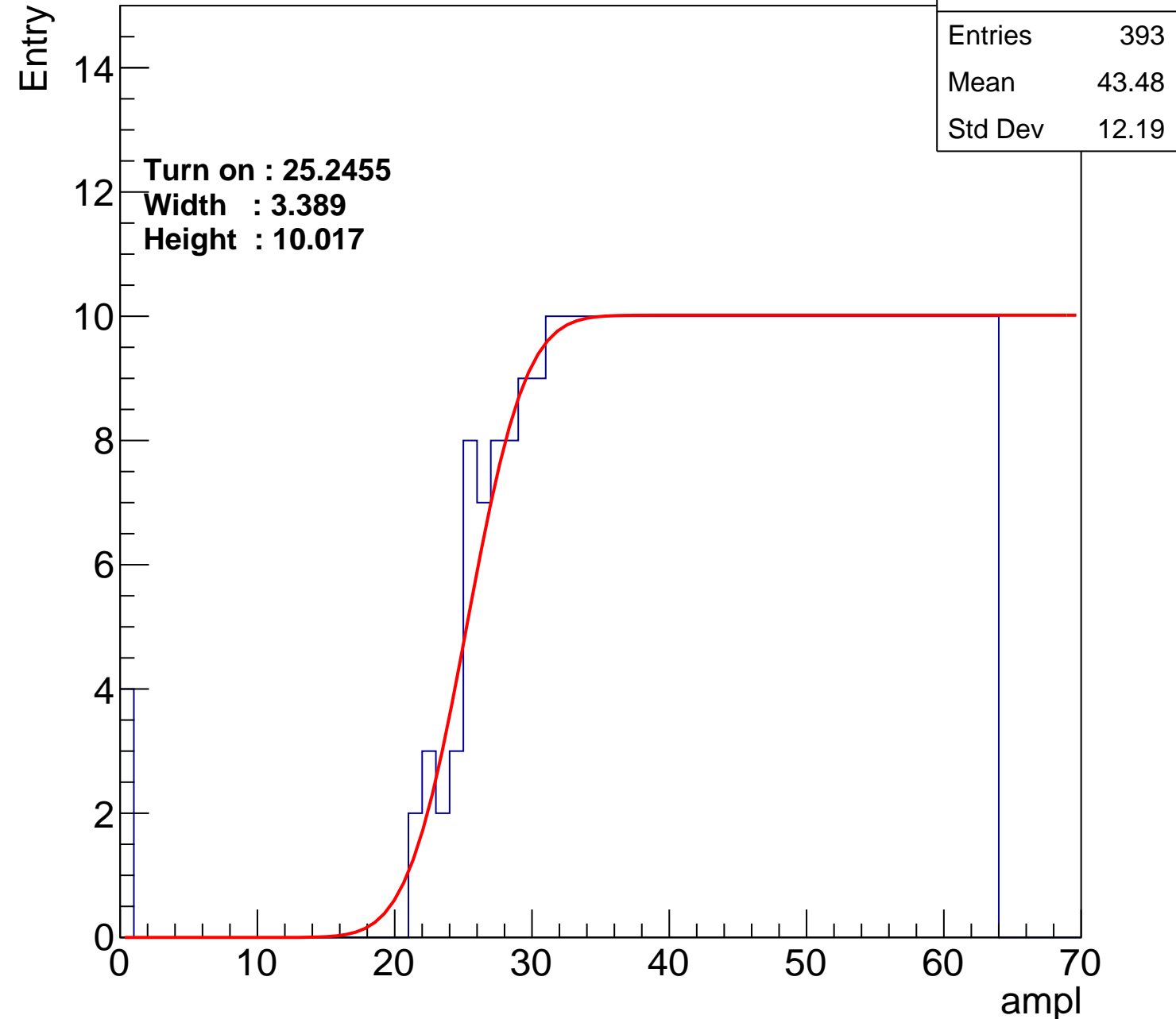
Width : 3.389

Height : 10.017

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch120

calib_packv5_042523_0143.root, FC#11, port A2

Entries	385
Mean	43.91
Std Dev	11.88

Turn on : 25.8331

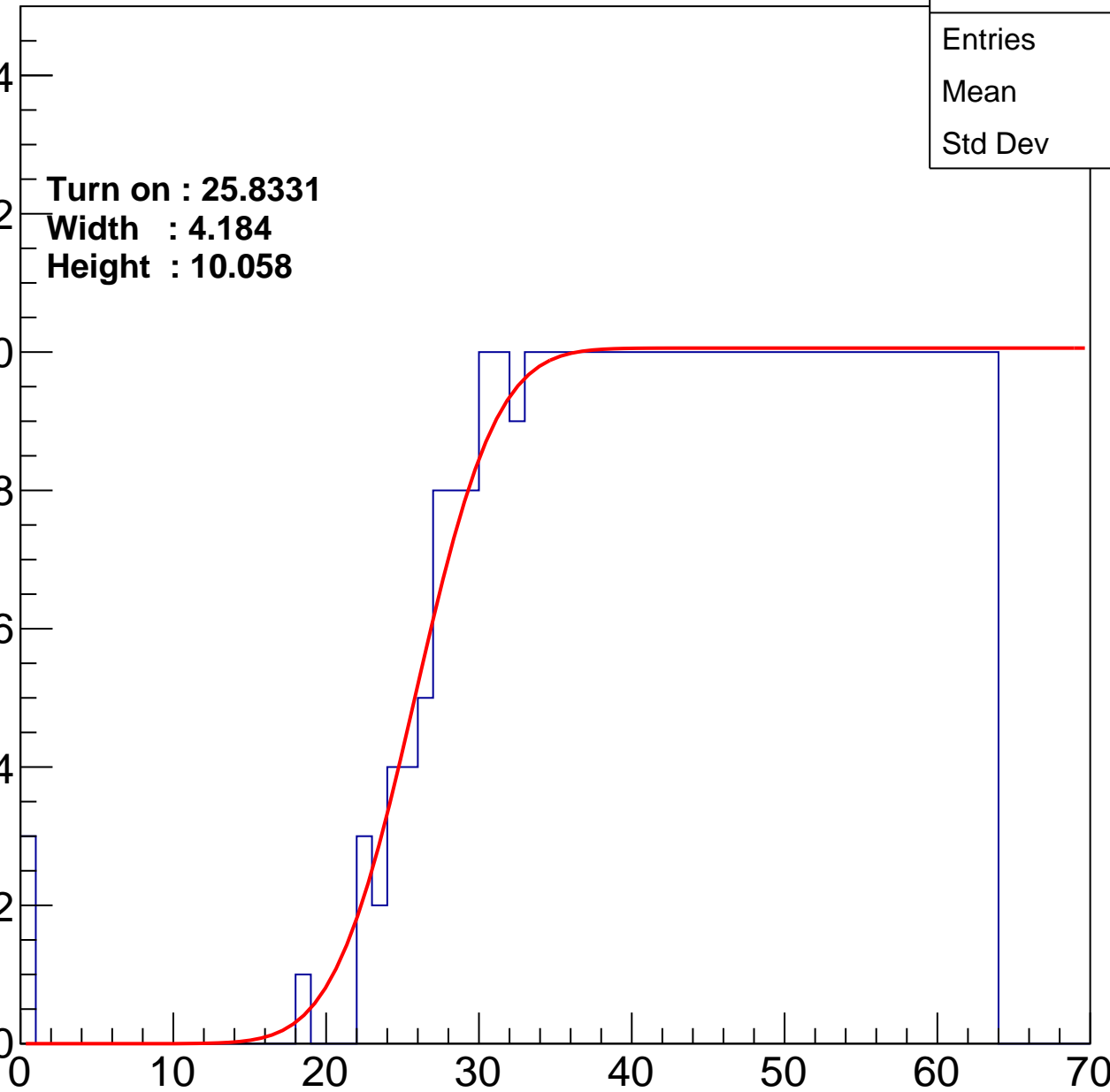
Width : 4.184

Height : 10.058

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch121

calib_packv5_042523_0143.root, FC#11, port A2

Entries	382
Mean	44.07
Std Dev	11.79

Turn on : 26.4749

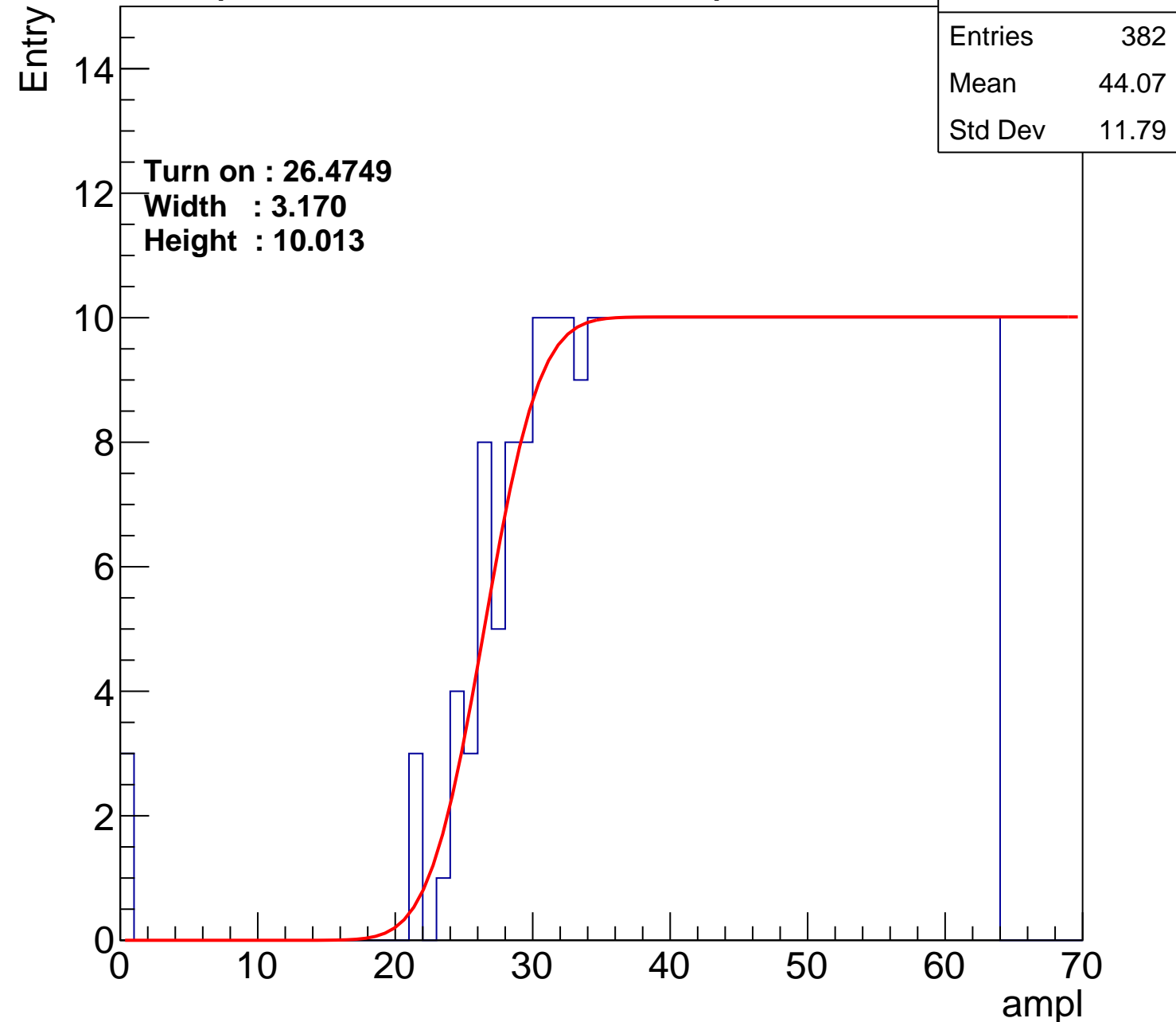
Width : 3.170

Height : 10.013

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch122

calib_packv5_042523_0143.root, FC#11, port A2

Entries	371
Mean	44.54
Std Dev	11.62

Turn on : 27.4923

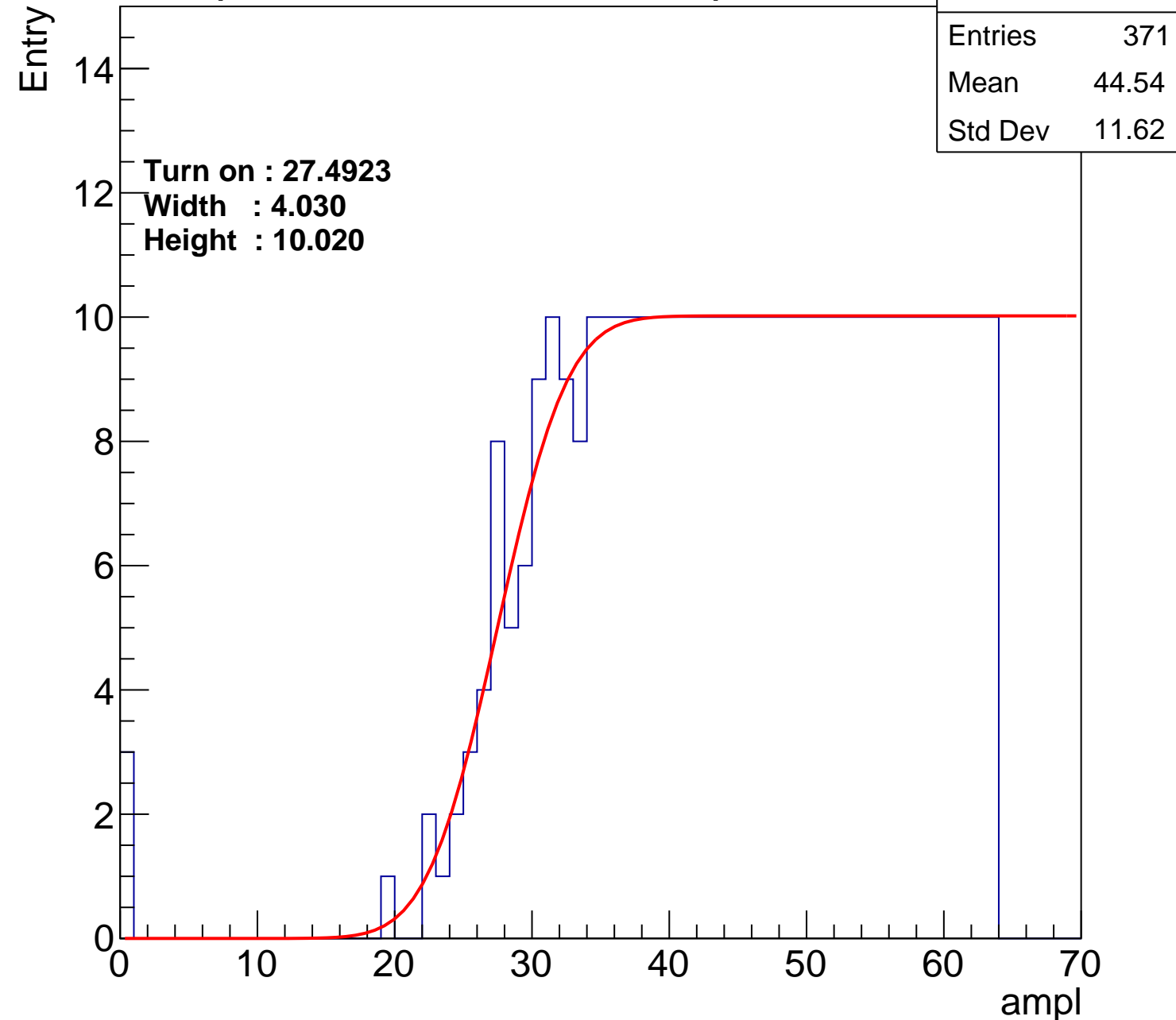
Width : 4.030

Height : 10.020

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch123

calib_packv5_042523_0143.root, FC#11, port A2

Entries	372
Mean	44.55
Std Dev	11.58

Turn on : 27.8907

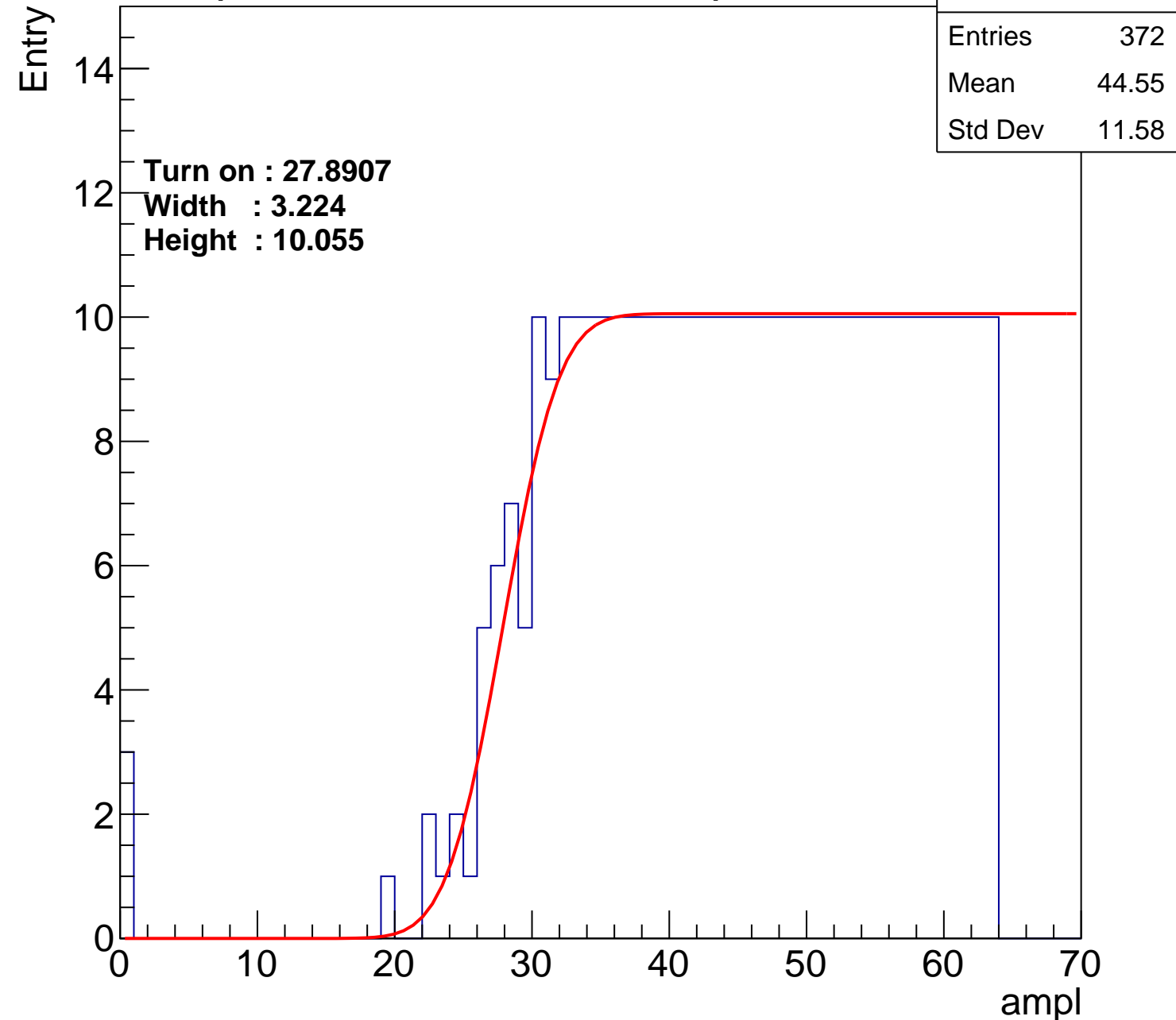
Width : 3.224

Height : 10.055

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch124

calib_packv5_042523_0143.root, FC#11, port A2

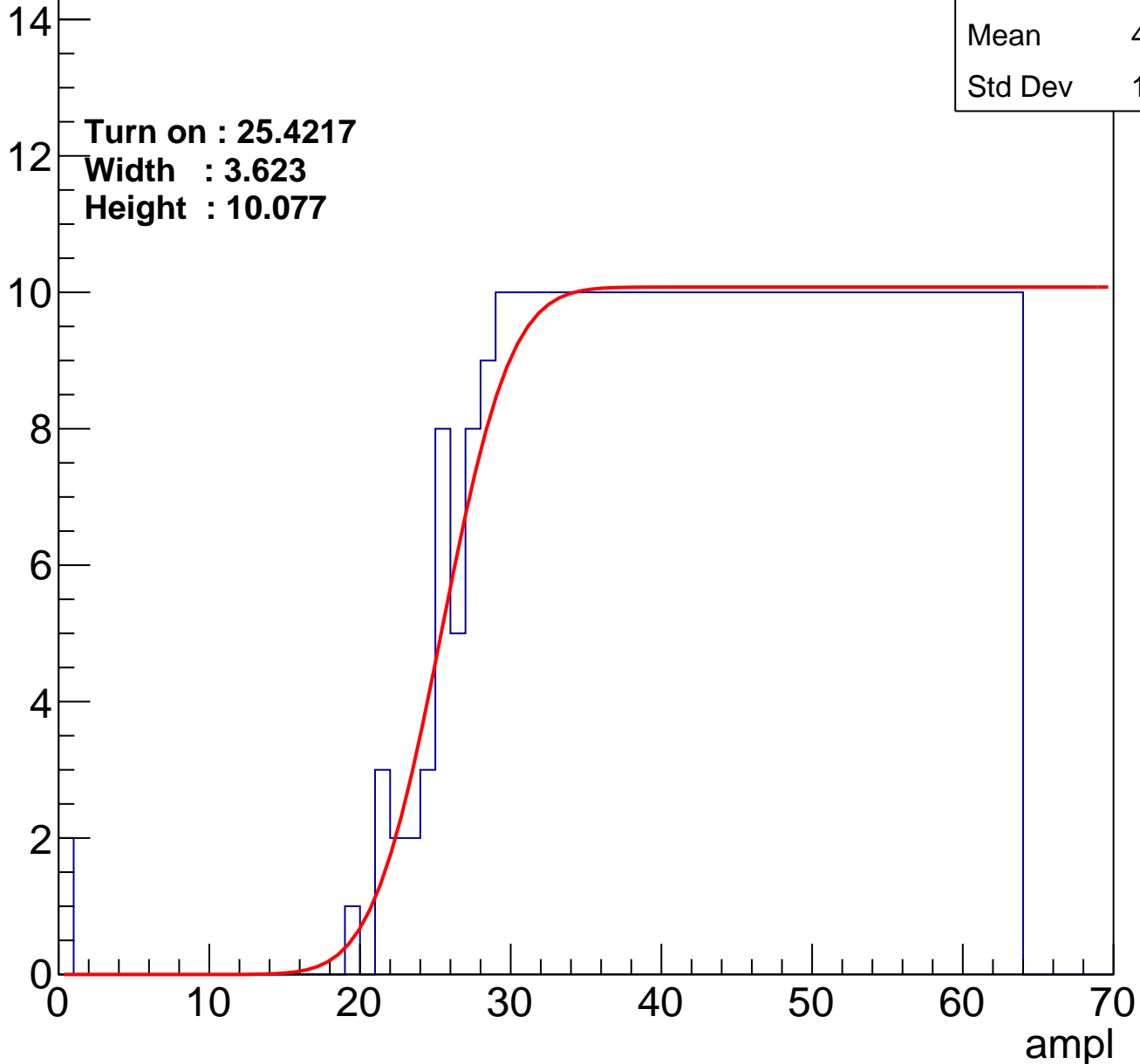
Entries	393
Mean	43.62
Std Dev	11.86

Turn on : 25.4217

Width : 3.623

Height : 10.077

Entry



B1L102S, U3-ch125

calib_packv5_042523_0143.root, FC#11, port A2

Entries	392
Mean	43.68
Std Dev	11.74

Turn on : 24.9576

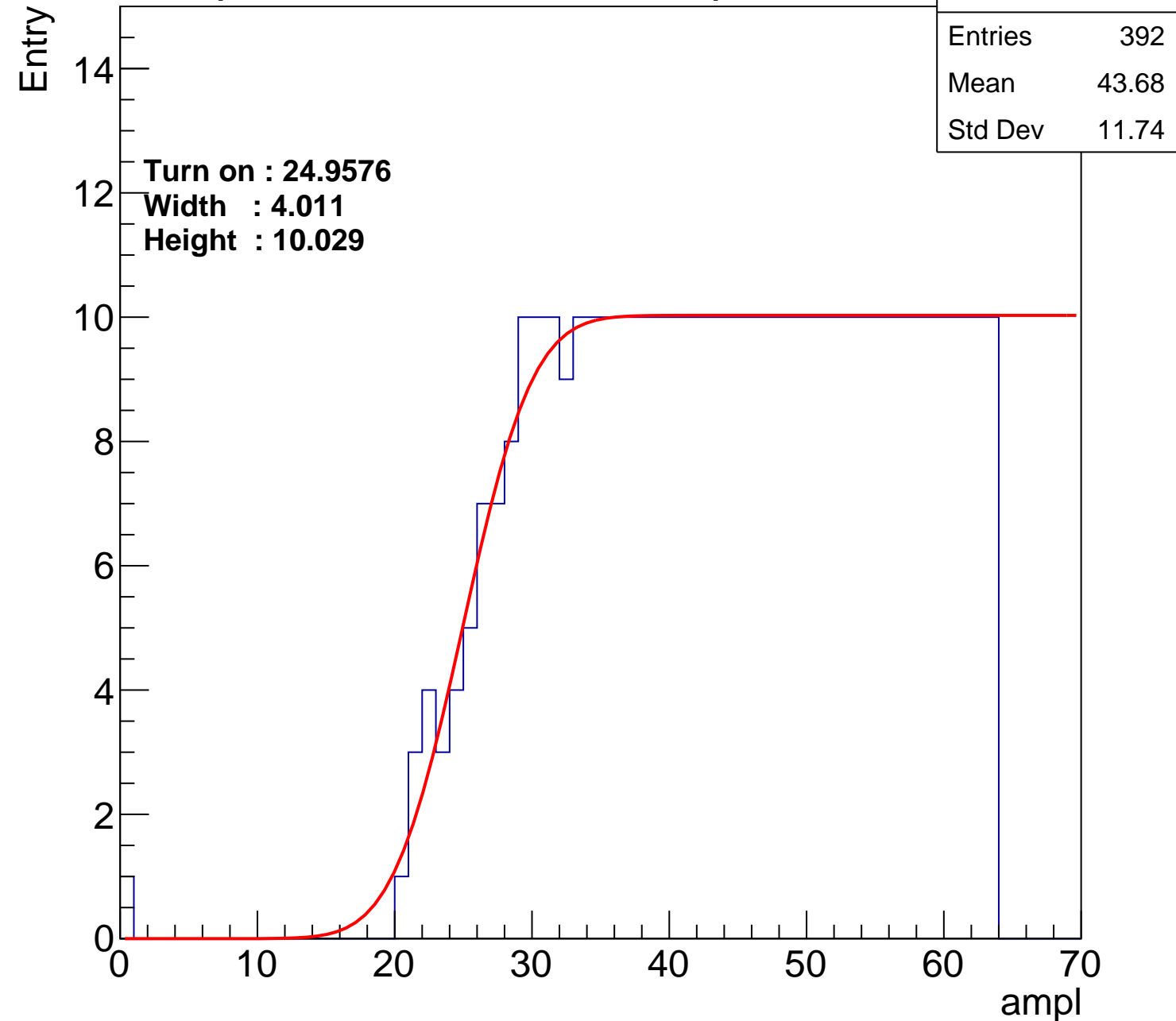
Width : 4.011

Height : 10.029

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch126

calib_packv5_042523_0143.root, FC#11, port A2

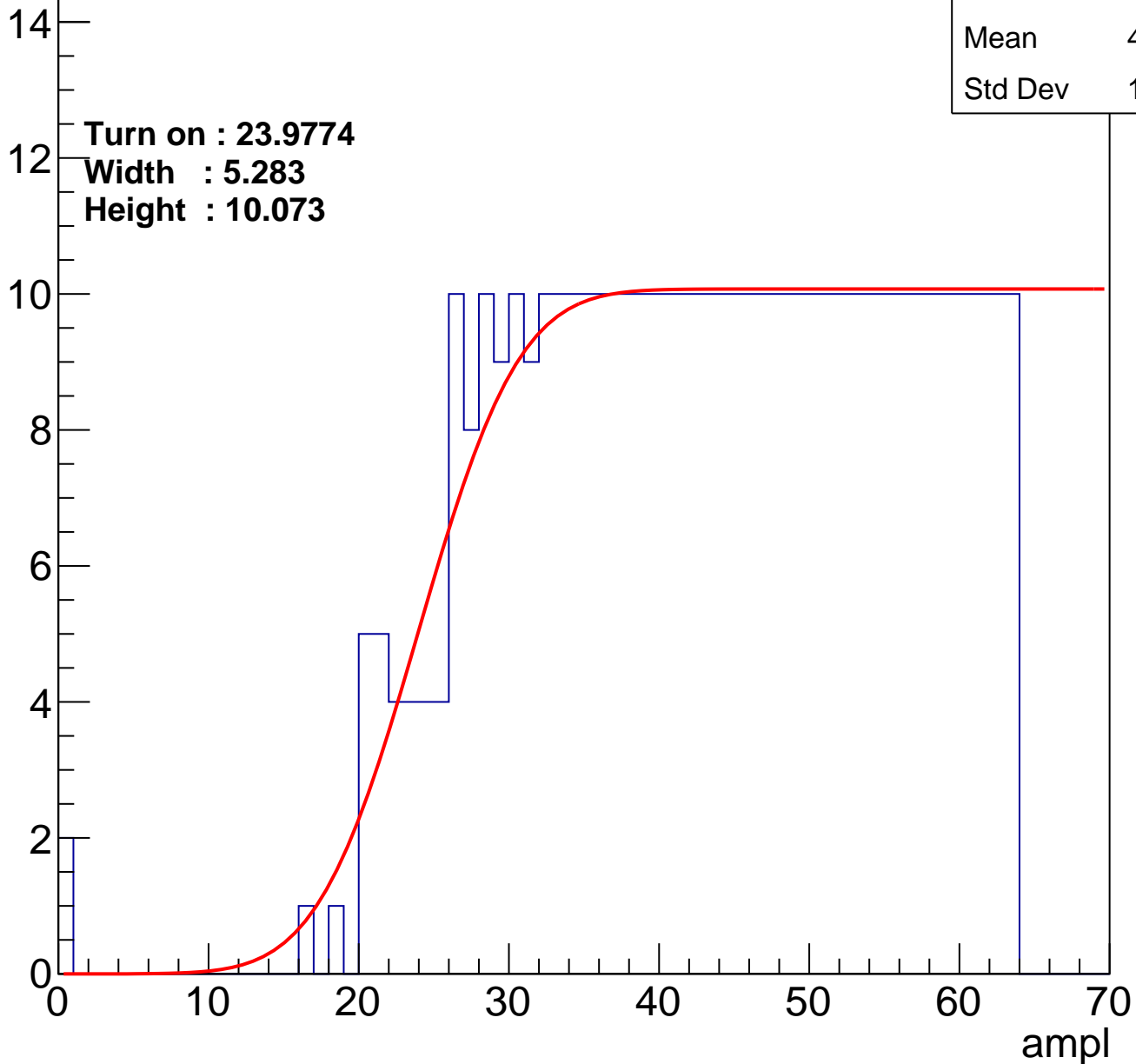
Entries	406
Mean	42.88
Std Dev	12.35

Turn on : 23.9774

Width : 5.283

Height : 10.073

Entry



B1L102S, U3-ch127

calib_packv5_042523_0143.root, FC#11, port A2

Entries	377
Mean	44.29
Std Dev	11.78

Turn on : 26.6613

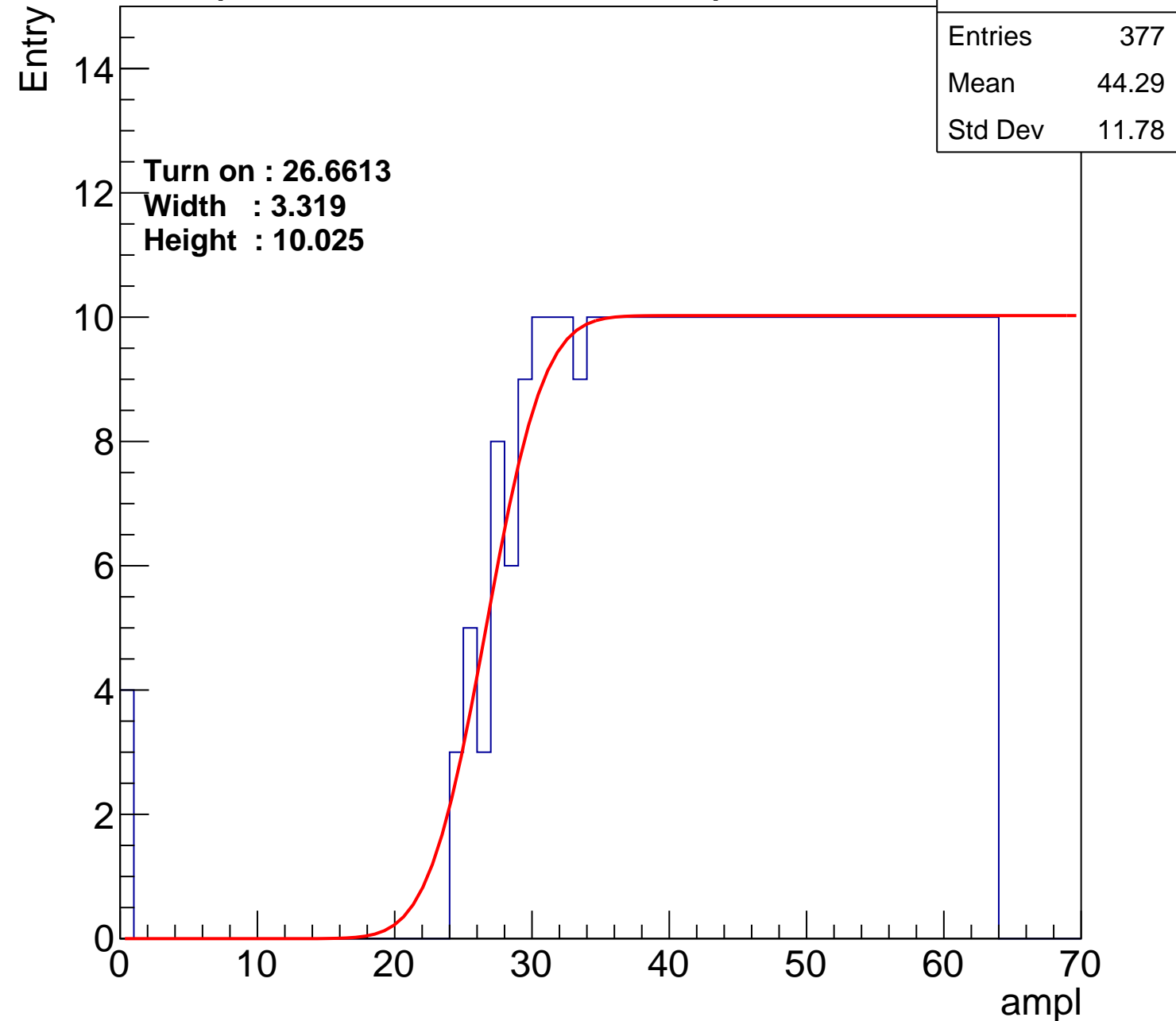
Width : 3.319

Height : 10.025

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U3-ch127

calib_packv5_042523_0143.root, FC#11, port A2

Entries	377
Mean	44.29
Std Dev	11.78

Turn on : 26.6613

Width : 3.319

Height : 10.025

Entry

14
12
10
8
6
4
2
0

ampl

