

B1L101S, U3-ch0

calib_packv5_042523_0143.root, FC#0, port D2

Entries	396
Mean	43.14
Std Dev	12.74

Turn on : 25.0284

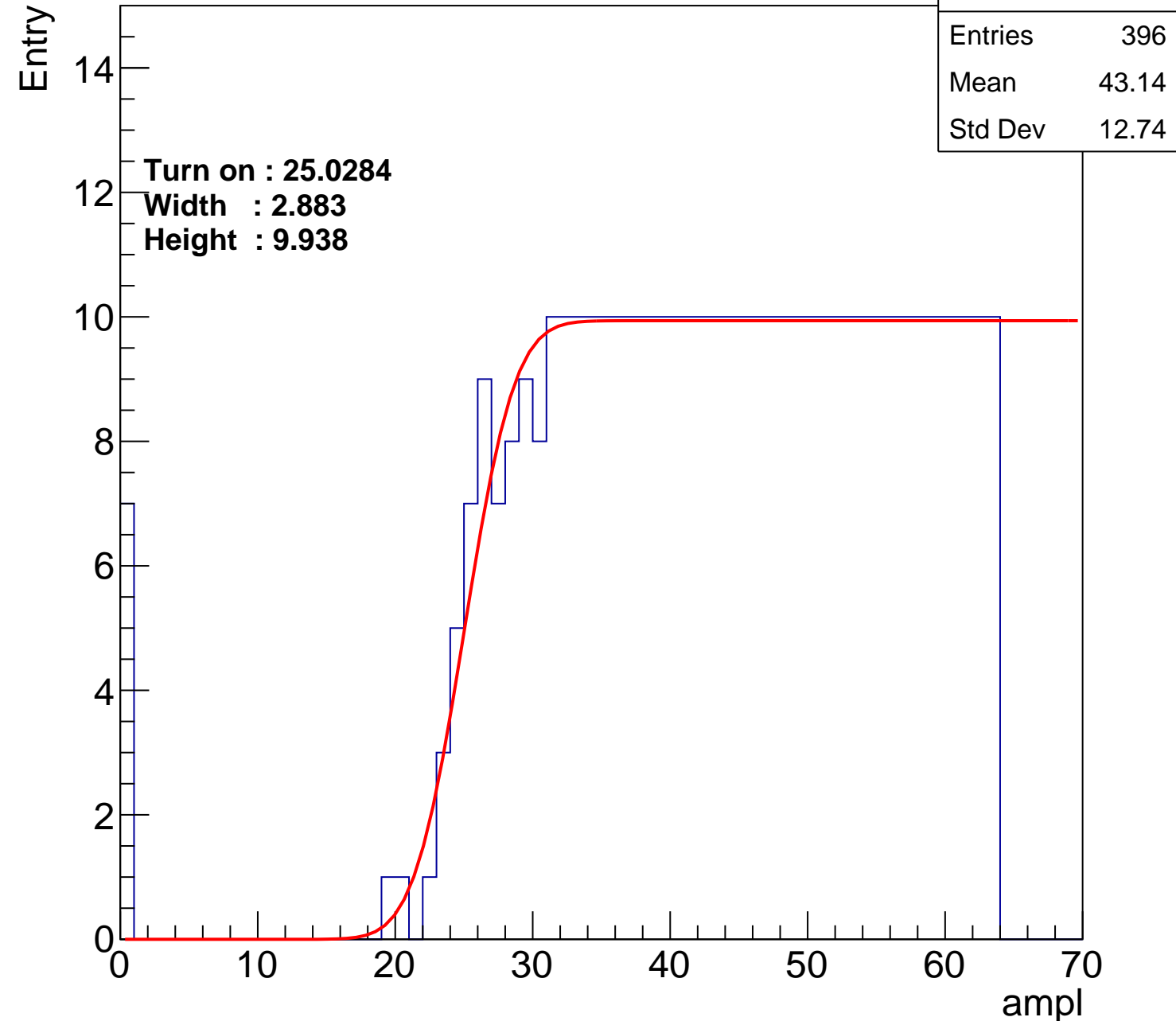
Width : 2.883

Height : 9.938

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch1

calib_packv5_042523_0143.root, FC#0, port D2

Entries	373
Mean	44.33
Std Dev	12.08

Turn on : 27.2757

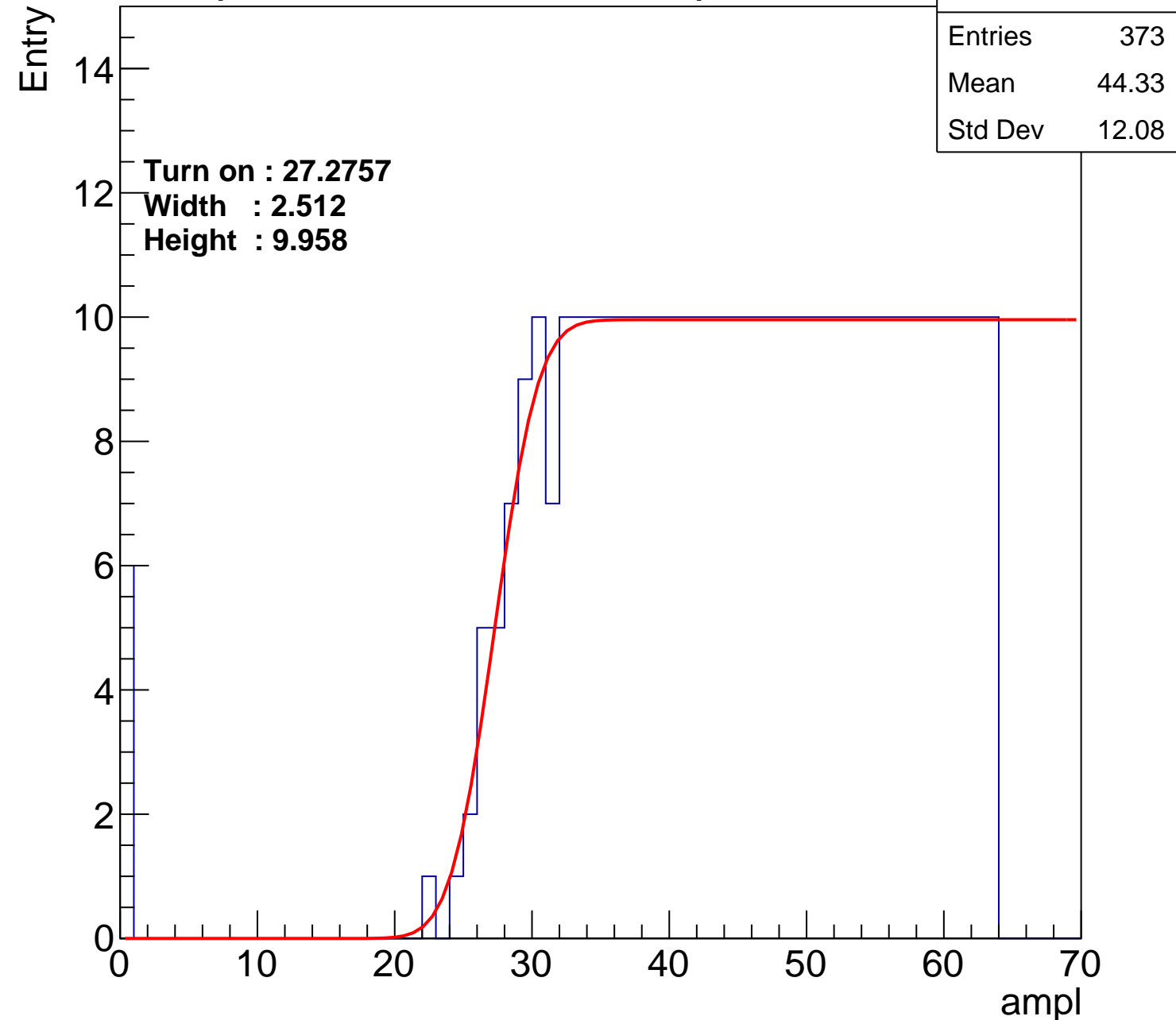
Width : 2.512

Height : 9.958

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch2

calib_packv5_042523_0143.root, FC#0, port D2

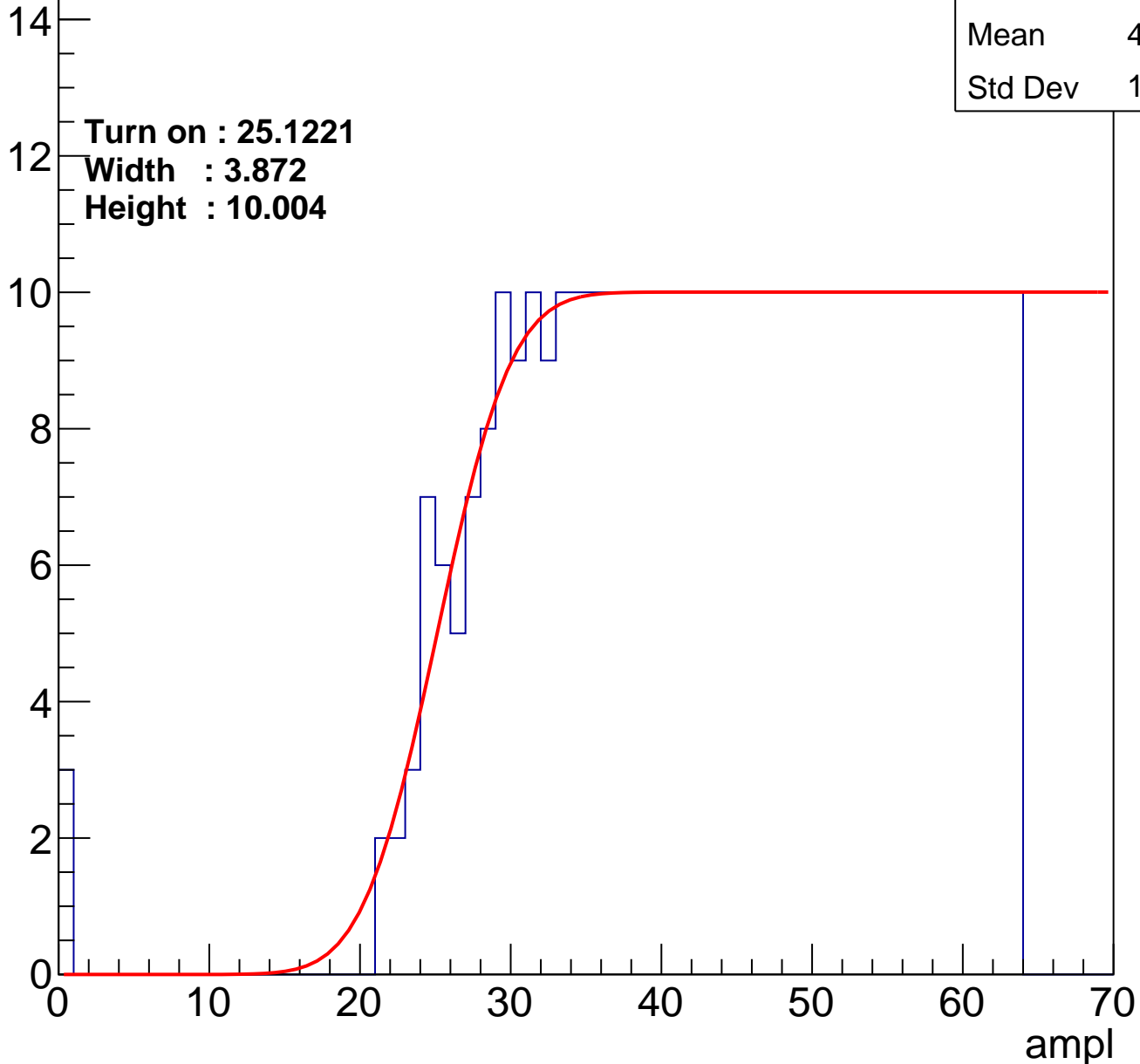
Entries	391
Mean	43.62
Std Dev	12.02

Turn on : 25.1221

Width : 3.872

Height : 10.004

Entry



B1L101S, U3-ch3

calib_packv5_042523_0143.root, FC#0, port D2

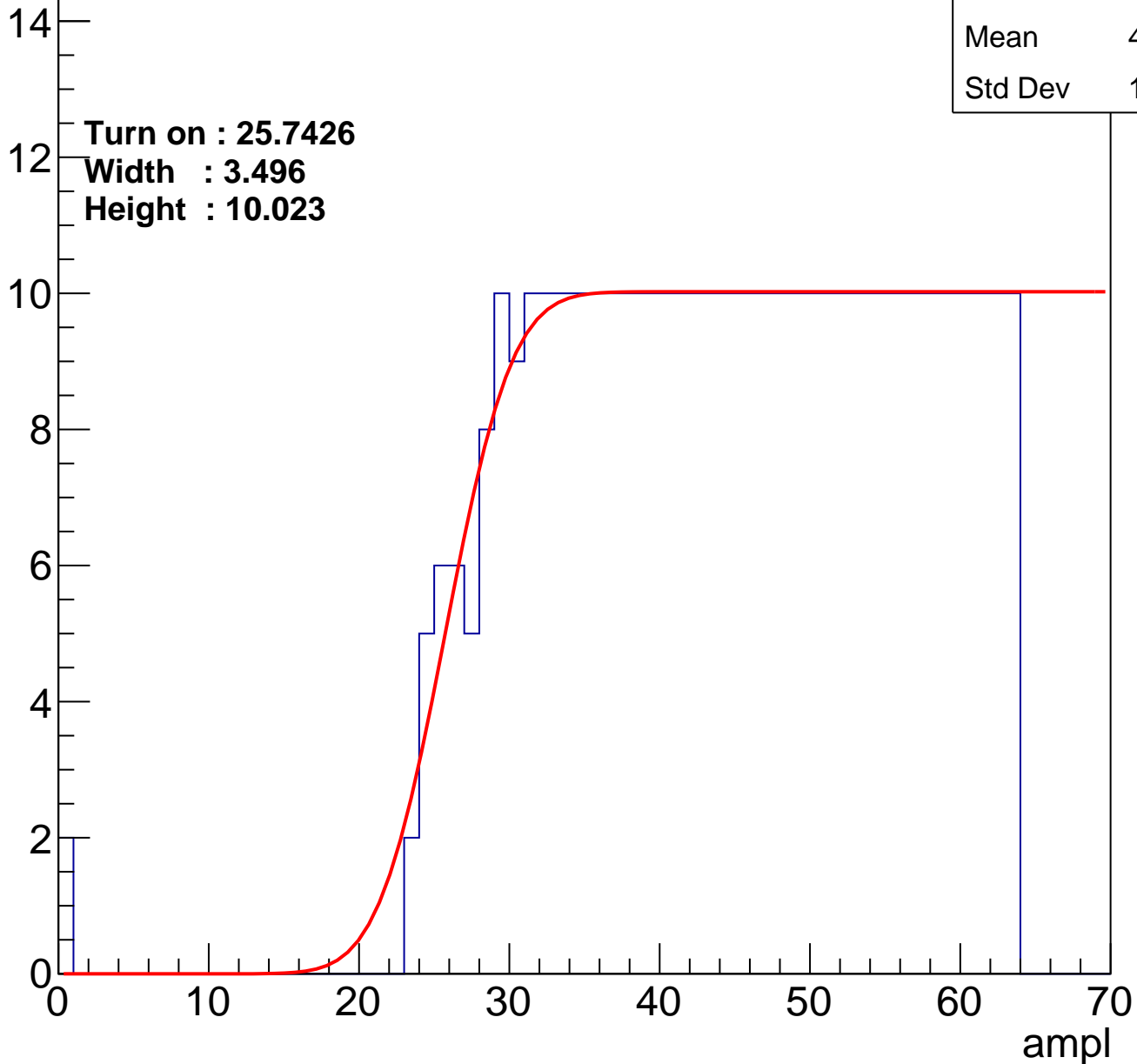
Entries	383
Mean	44.13
Std Dev	11.57

Turn on : 25.7426

Width : 3.496

Height : 10.023

Entry



B1L101S, U3-ch4

calib_packv5_042523_0143.root, FC#0, port D2

Entries	392
Mean	43.17
Std Dev	13.07

Turn on : 26.0520

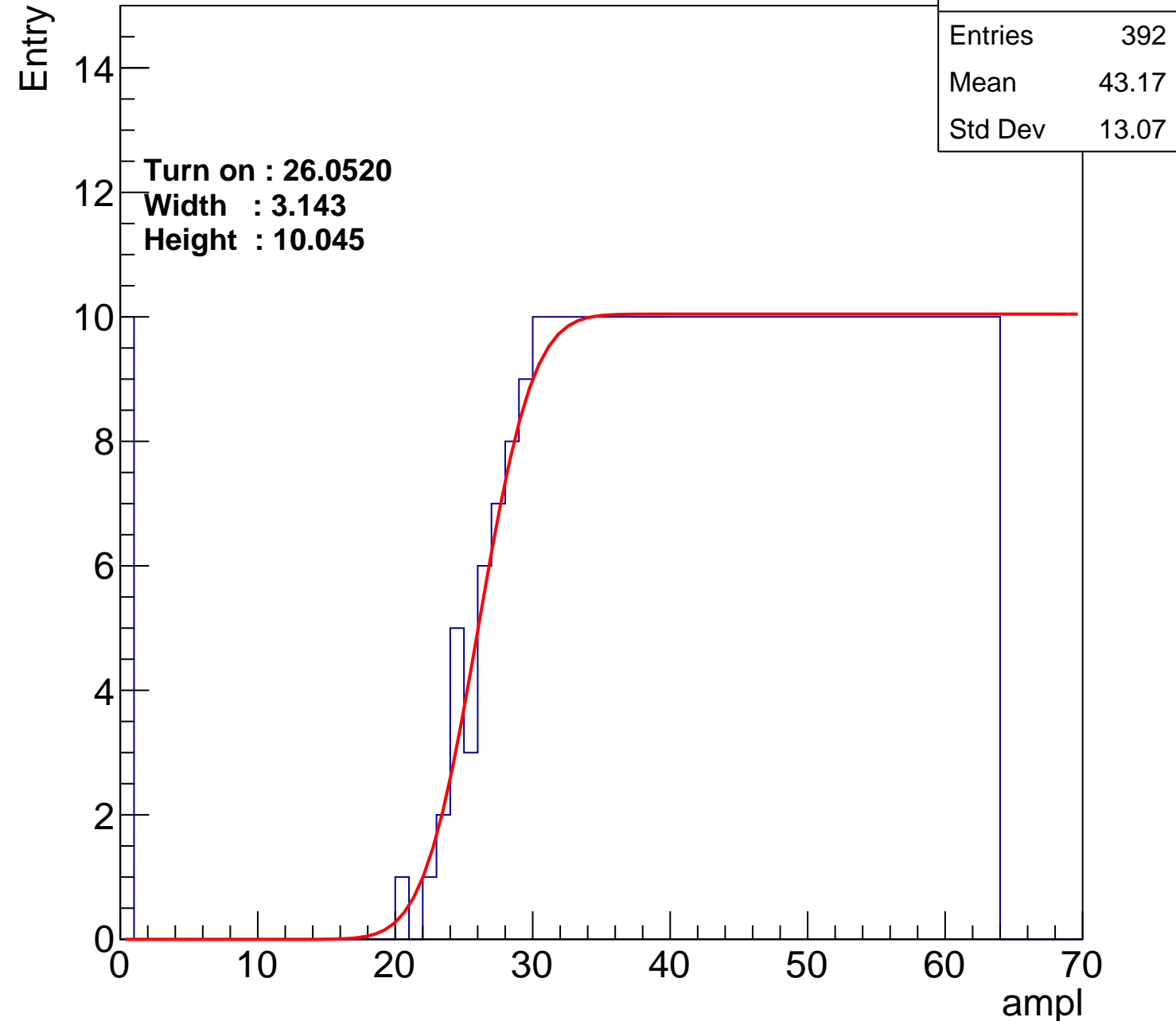
Width : 3.143

Height : 10.045

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch5

calib_packv5_042523_0143.root, FC#0, port D2

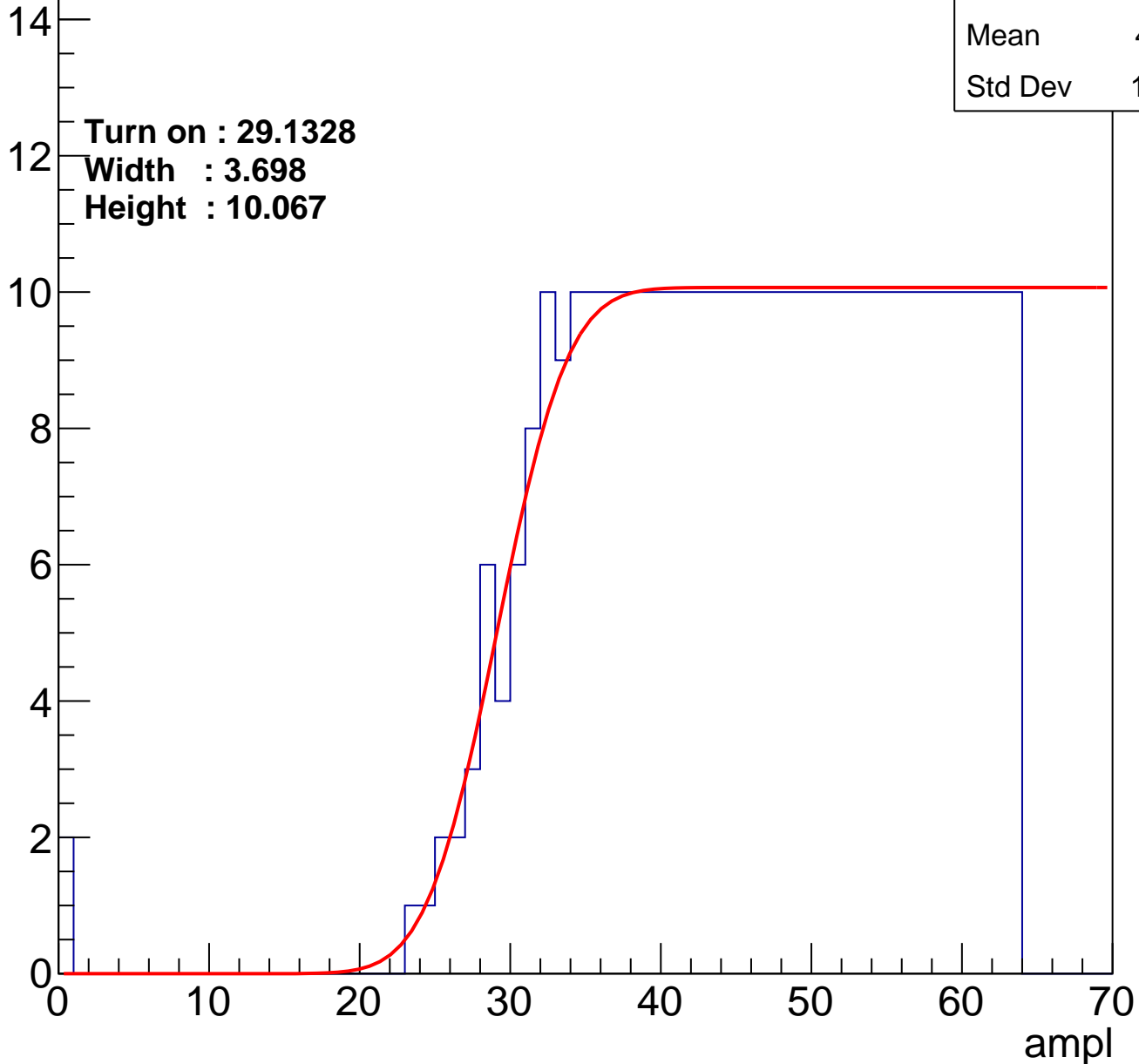
Entries	354
Mean	45.51
Std Dev	10.92

Turn on : 29.1328

Width : 3.698

Height : 10.067

Entry



B1L101S, U3-ch6

calib_packv5_042523_0143.root, FC#0, port D2

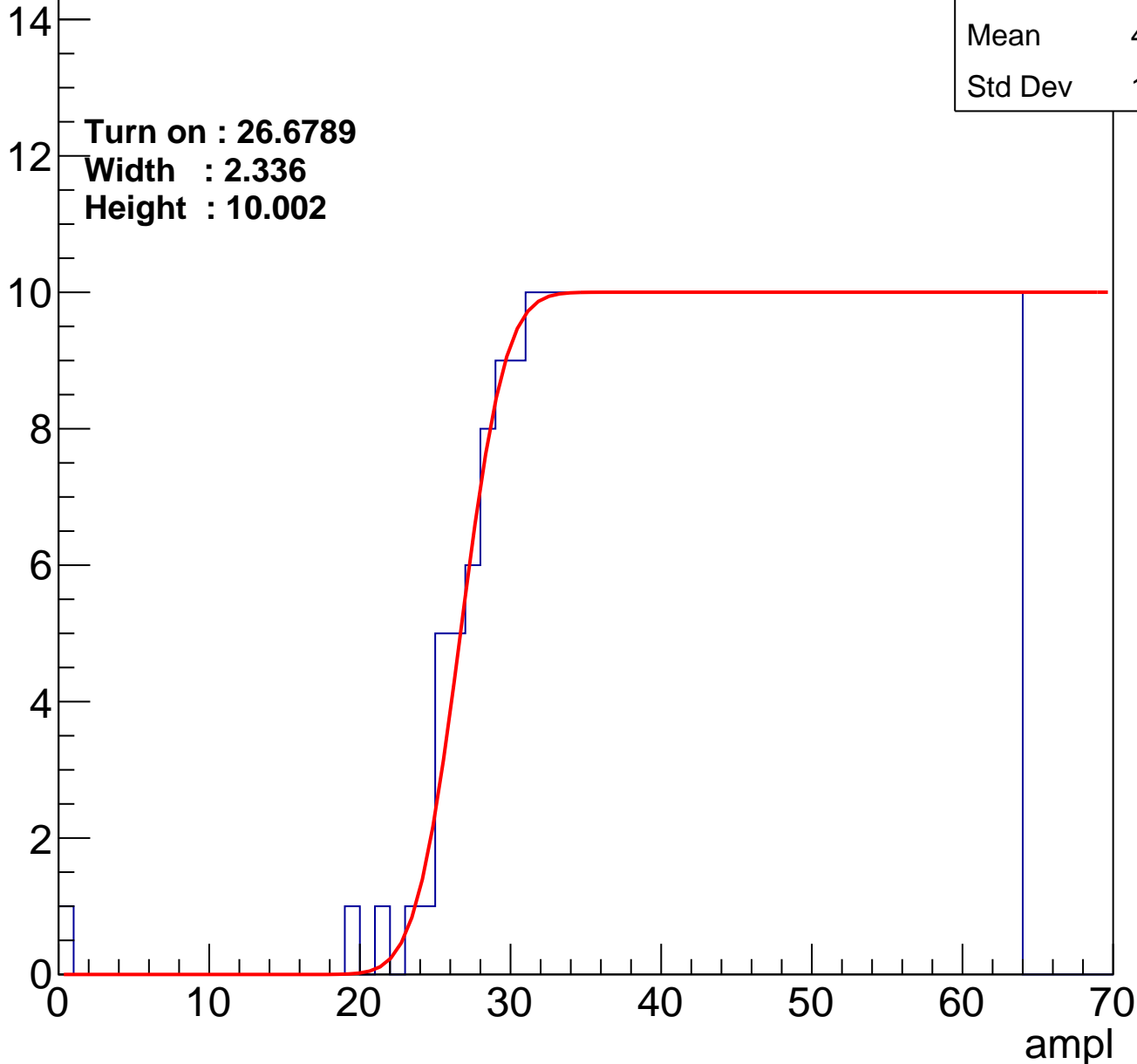
Entries	377
Mean	44.48
Std Dev	11.25

Turn on : 26.6789

Width : 2.336

Height : 10.002

Entry



B1L101S, U3-ch7

calib_packv5_042523_0143.root, FC#0, port D2

Entries	386
Mean	43.77
Std Dev	12.19

Turn on : 26.7005

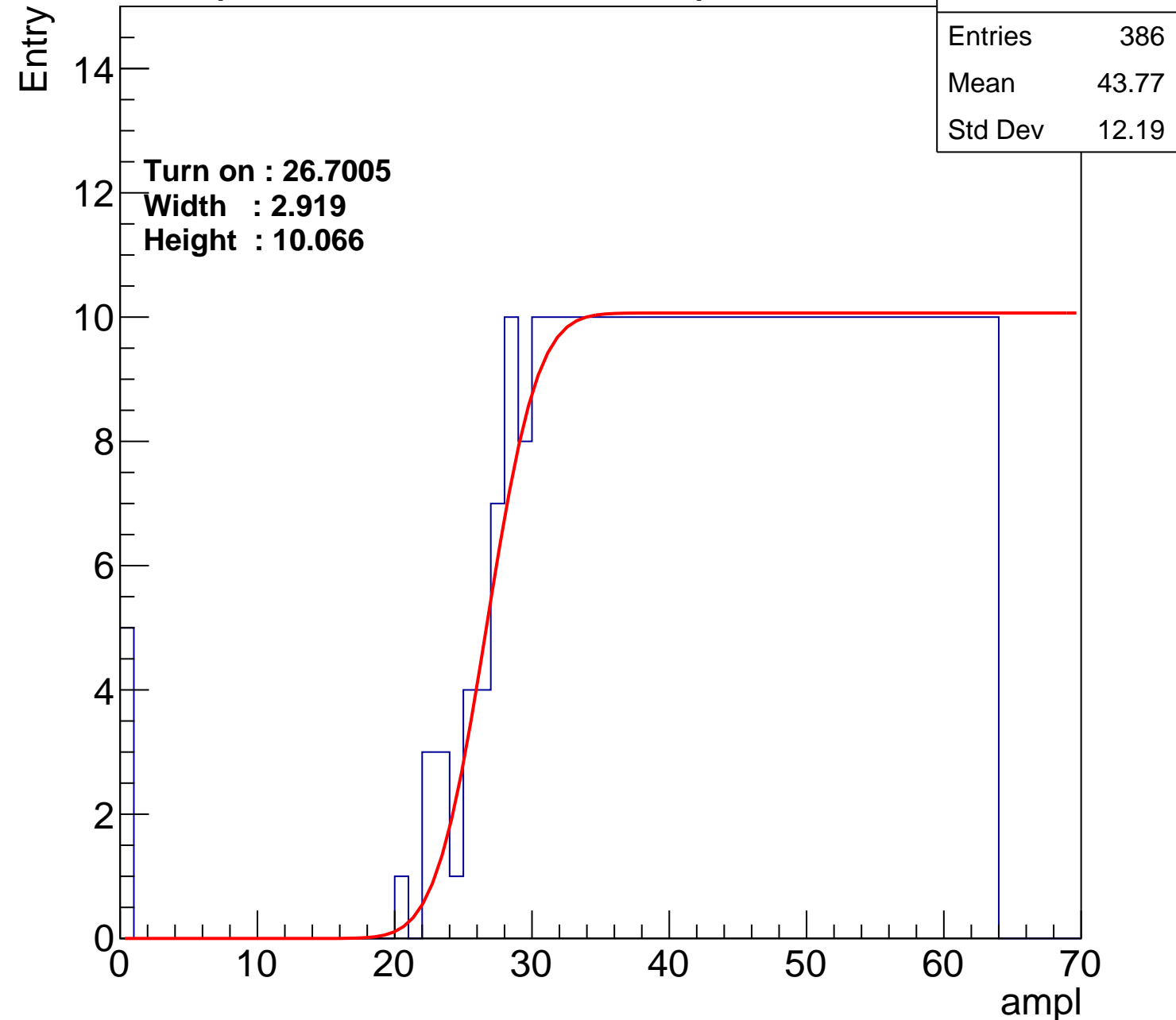
Width : 2.919

Height : 10.066

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch8

calib_packv5_042523_0143.root, FC#0, port D2

Entries	392
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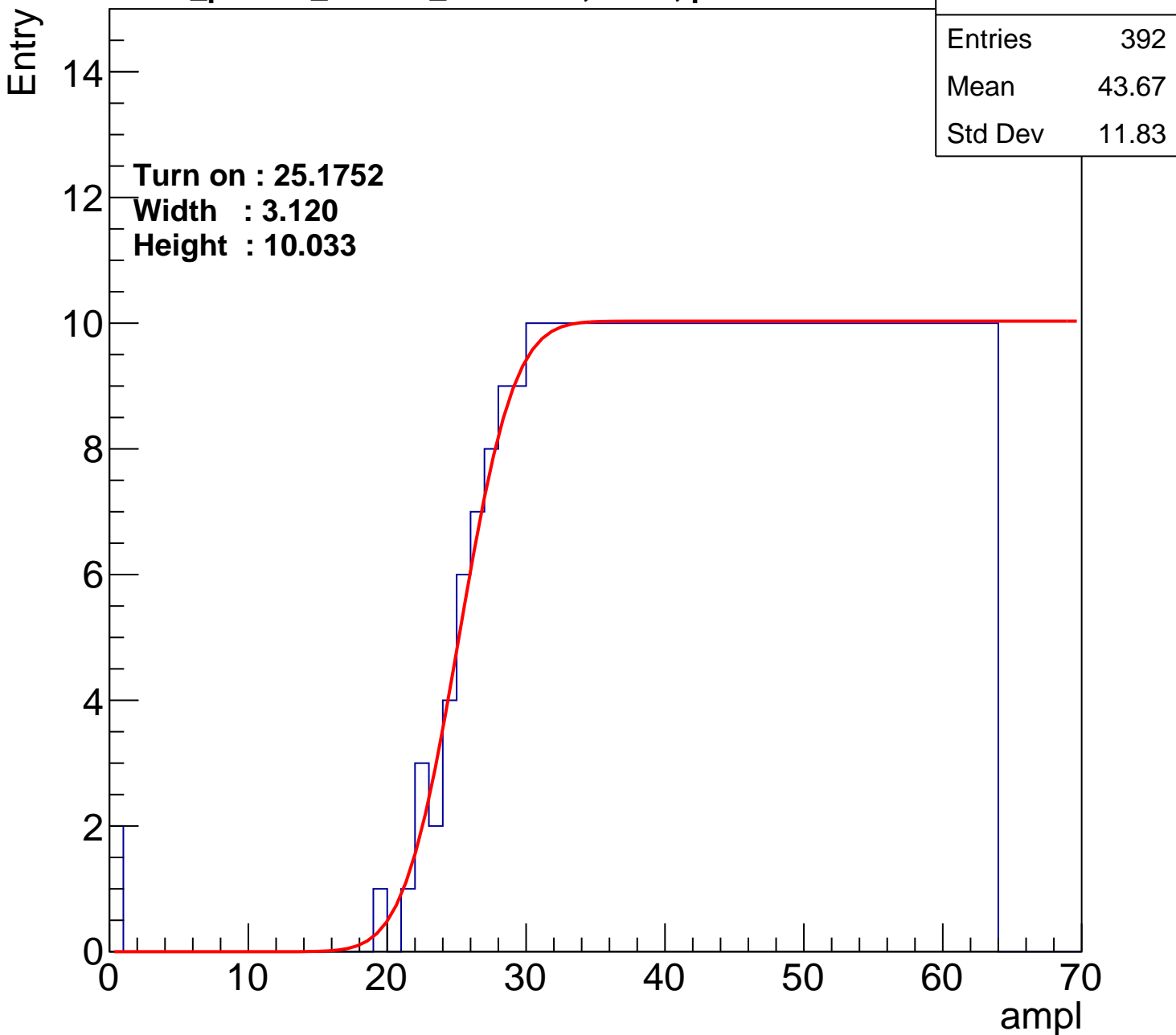
Mean	43.67
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Std Dev	11.83
---------	-------

Turn on : 25.1752

Width : 3.120

Height : 10.033



B1L101S, U3-ch9

calib_packv5_042523_0143.root, FC#0, port D2

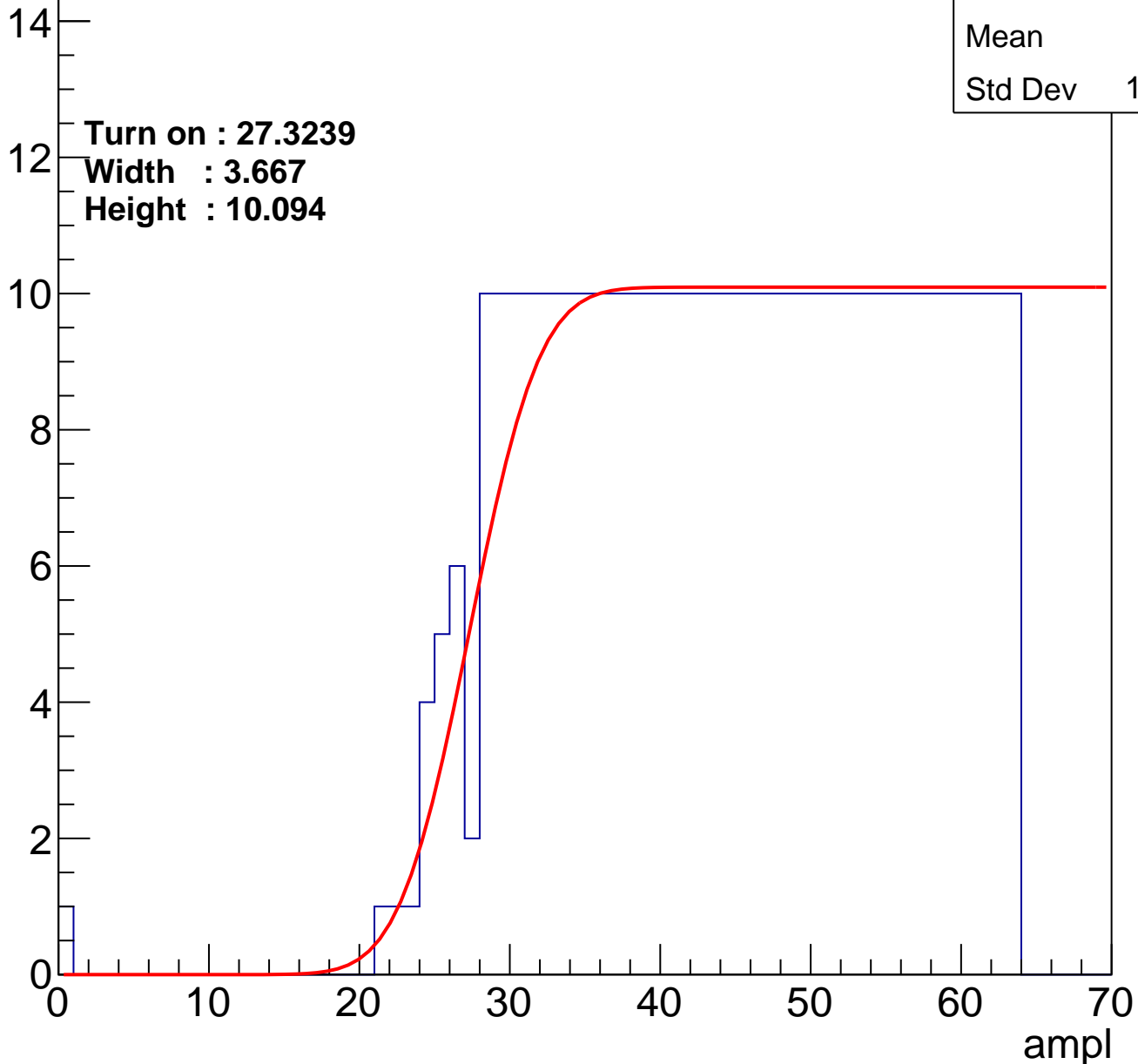
Entries	381
Mean	44.3
Std Dev	11.33

Turn on : 27.3239

Width : 3.667

Height : 10.094

Entry



B1L101S, U3-ch10

calib_packv5_042523_0143.root, FC#0, port D2

Entries	387
Mean	43.71
Std Dev	12.22

Turn on : 26.0441

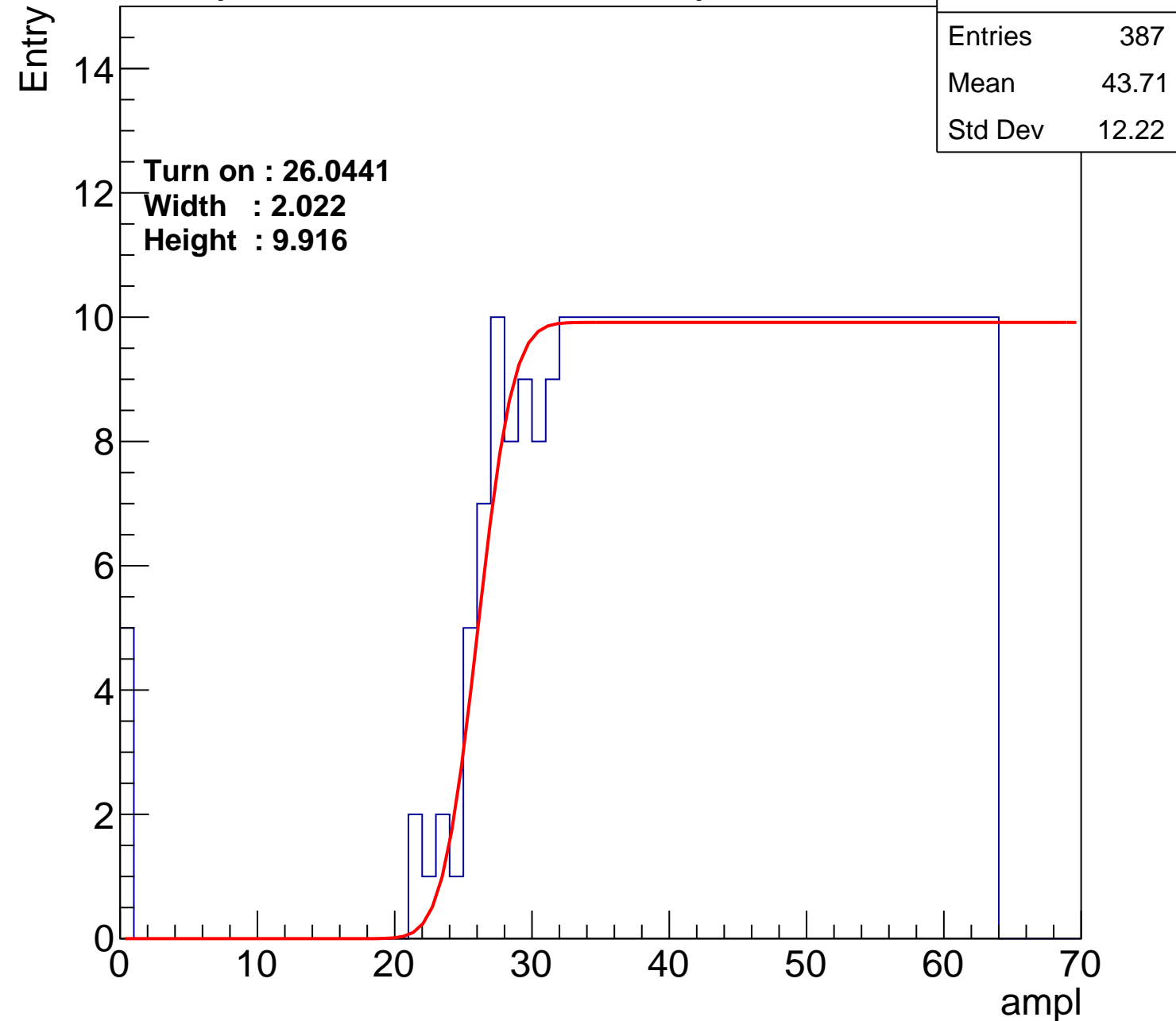
Width : 2.022

Height : 9.916

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch11

calib_packv5_042523_0143.root, FC#0, port D2

Entries	384
Mean	43.71
Std Dev	12.51

Turn on : 26.8333

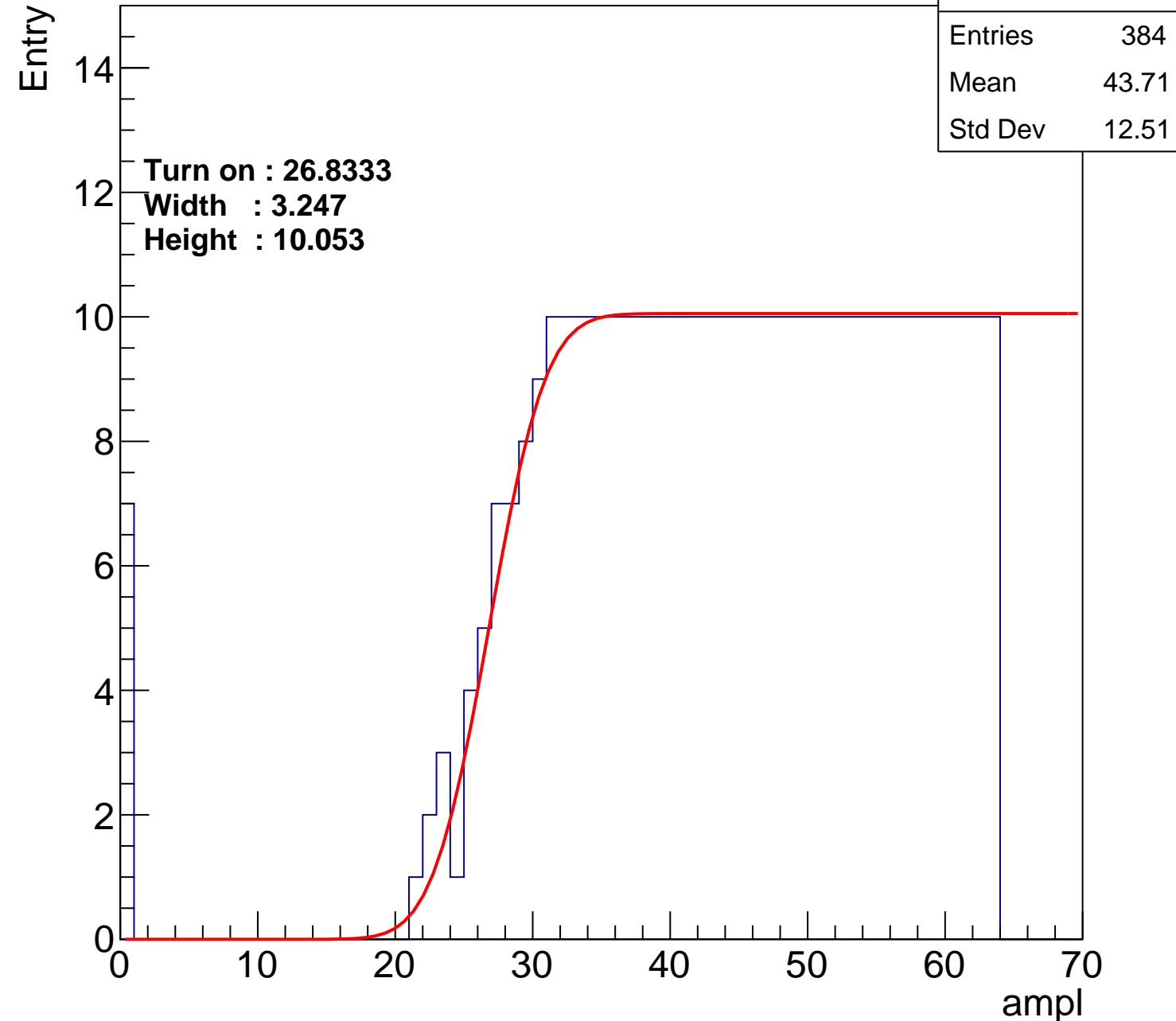
Width : 3.247

Height : 10.053

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch12

calib_packv5_042523_0143.root, FC#0, port D2

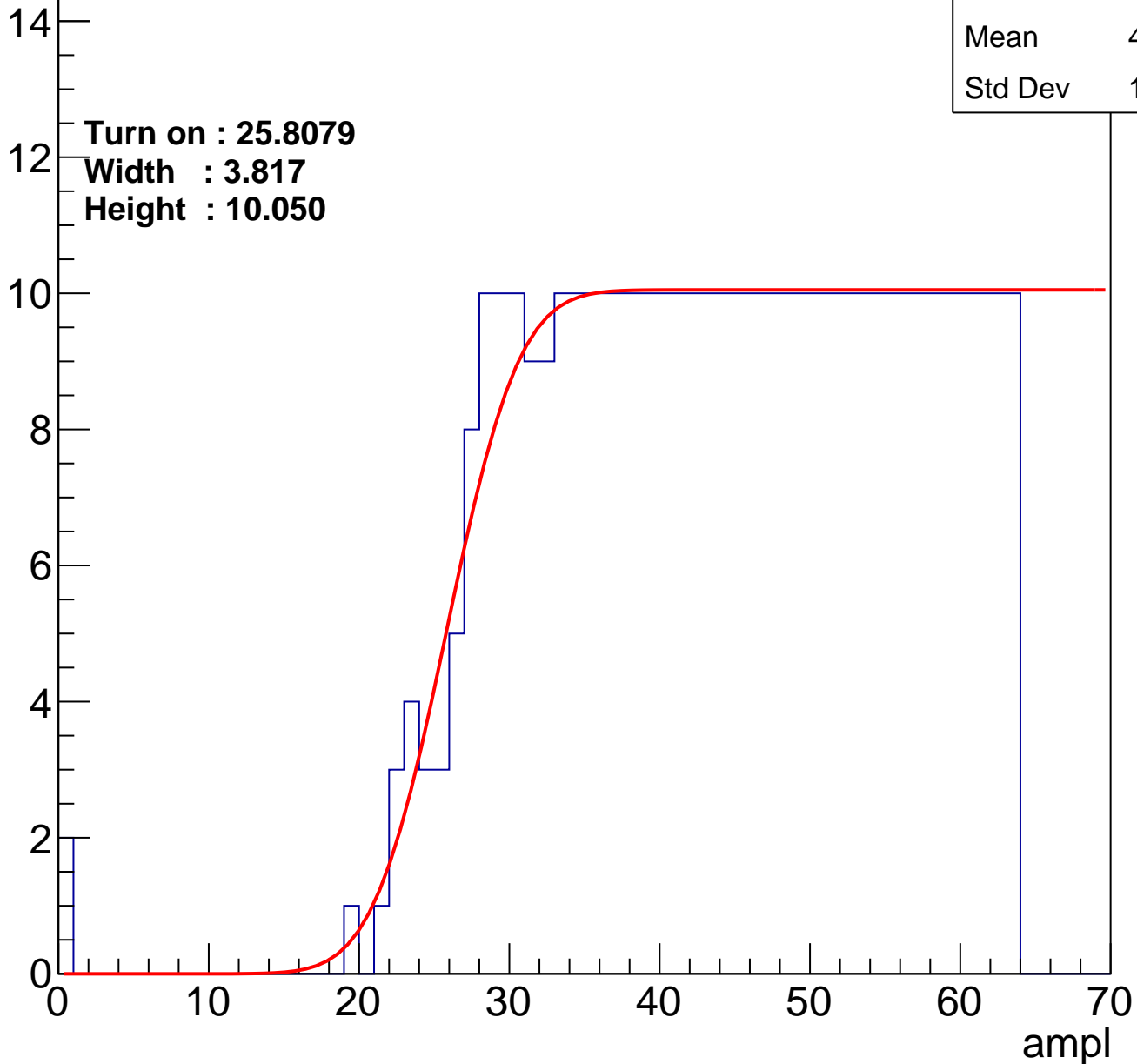
Entries	388
Mean	43.84
Std Dev	11.77

Turn on : 25.8079

Width : 3.817

Height : 10.050

Entry



B1L101S, U3-ch13

calib_packv5_042523_0143.root, FC#0, port D2

Entries	359
Mean	45.15
Std Dev	11.4

Turn on : 28.7662

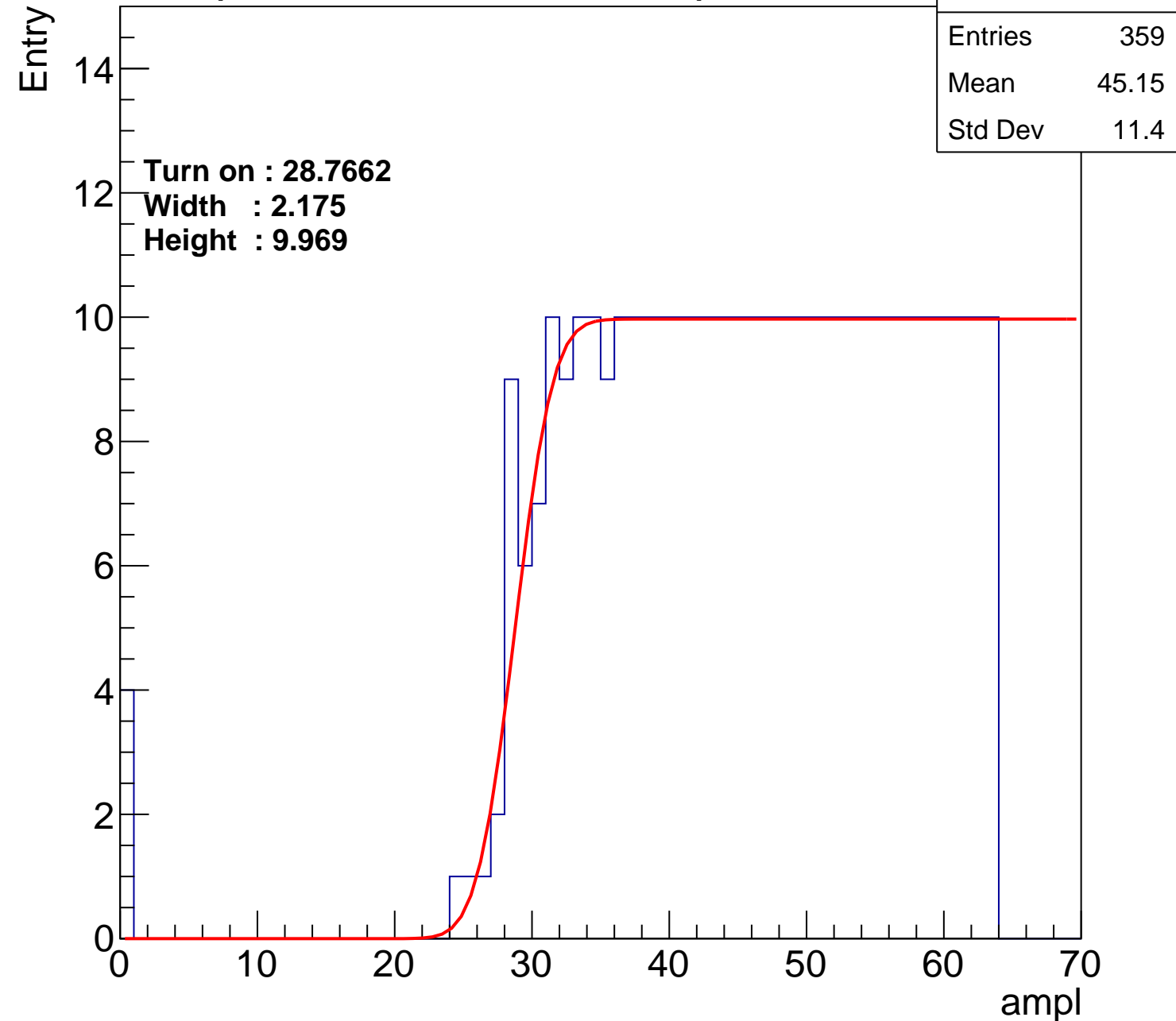
Width : 2.175

Height : 9.969

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch14

calib_packv5_042523_0143.root, FC#0, port D2

Entries	375
Mean	44.32
Std Dev	11.85

Turn on : 27.8472

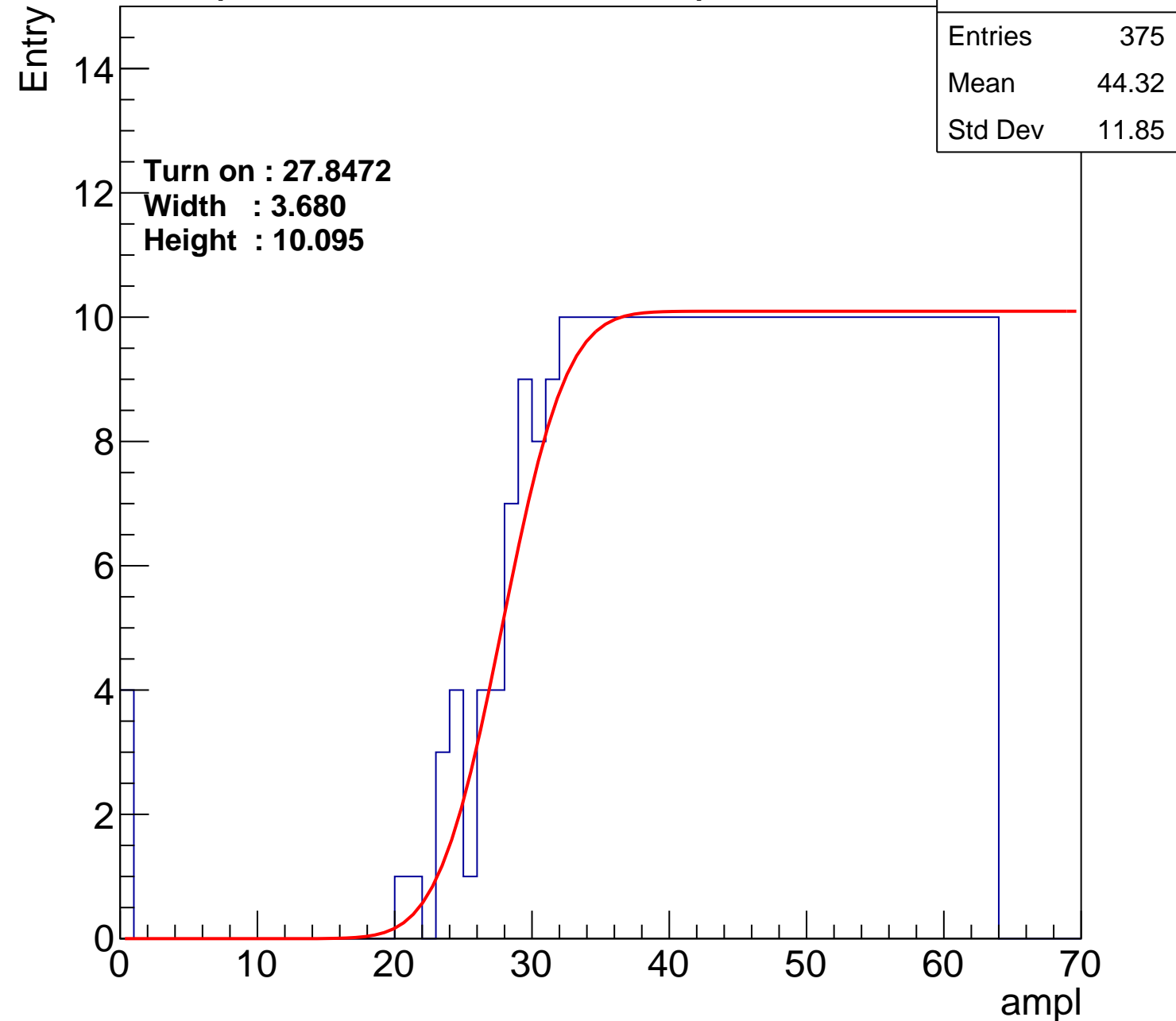
Width : 3.680

Height : 10.095

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch15

calib_packv5_042523_0143.root, FC#0, port D2

Entries	399
Mean	43.37
Std Dev	12.41

Turn on : 25.3889

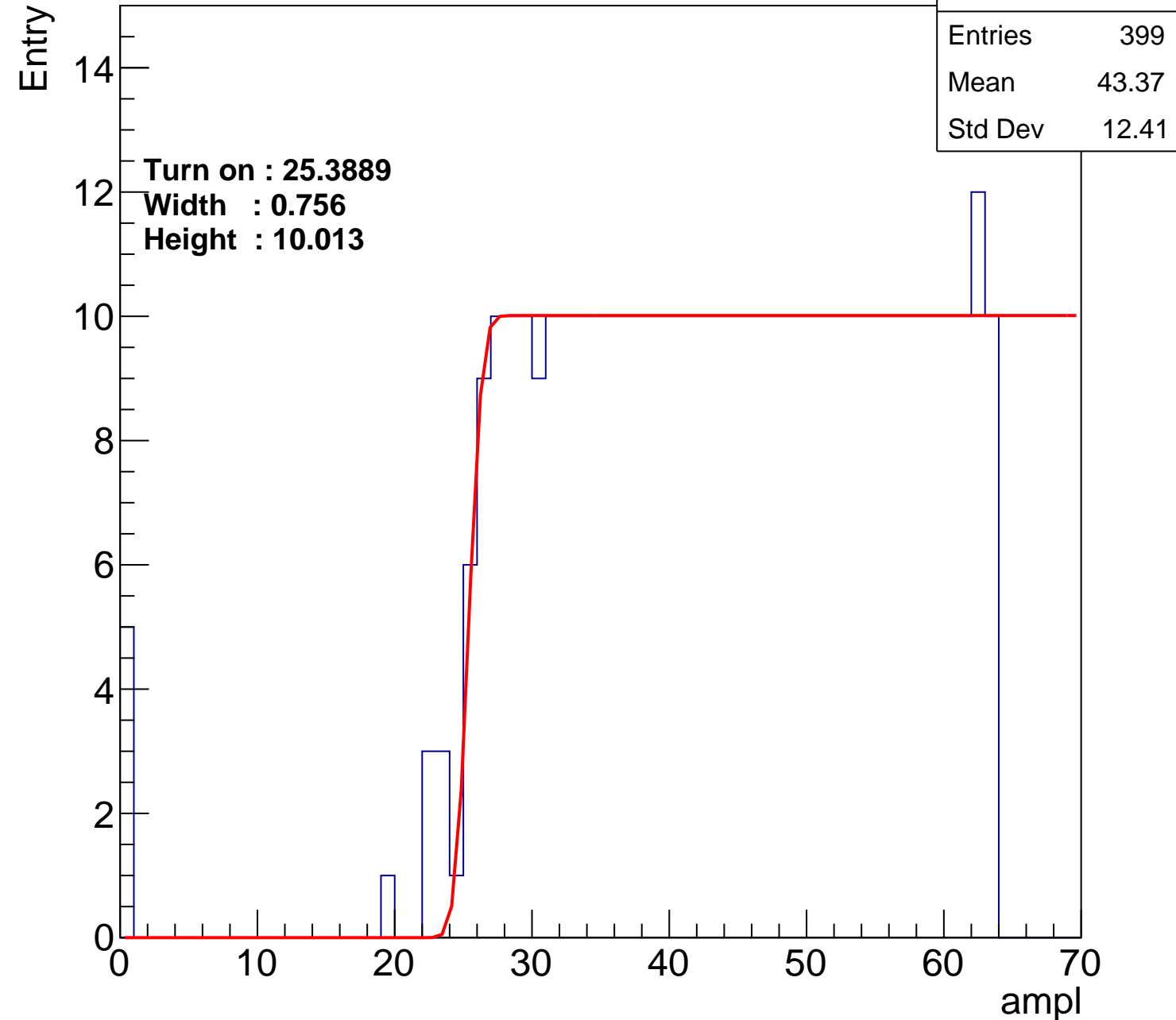
Width : 0.756

Height : 10.013

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch16

calib_packv5_042523_0143.root, FC#0, port D2

Entries	386
Mean	43.78
Std Dev	12.17

Turn on : 25.9511

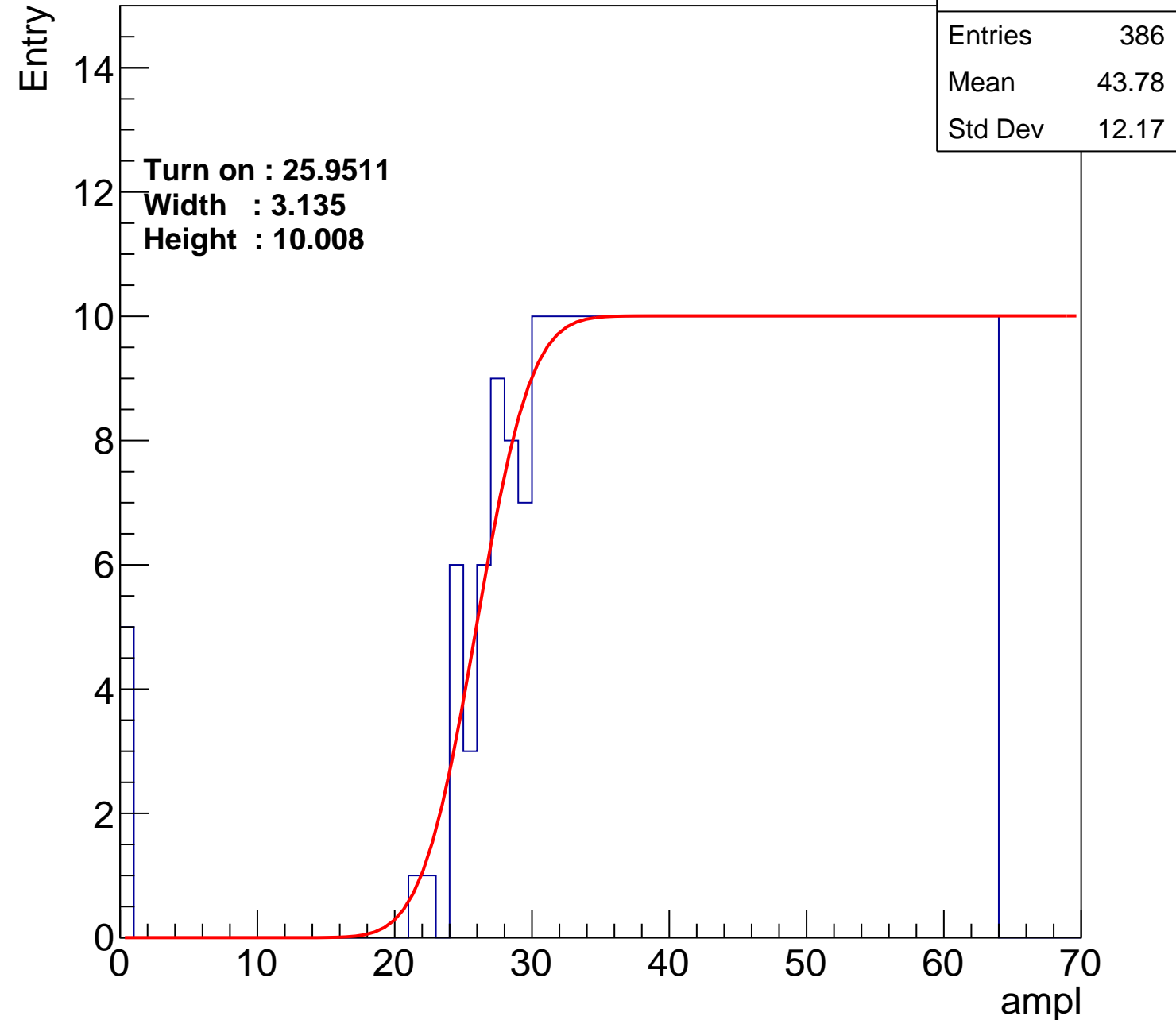
Width : 3.135

Height : 10.008

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch17

calib_packv5_042523_0143.root, FC#0, port D2

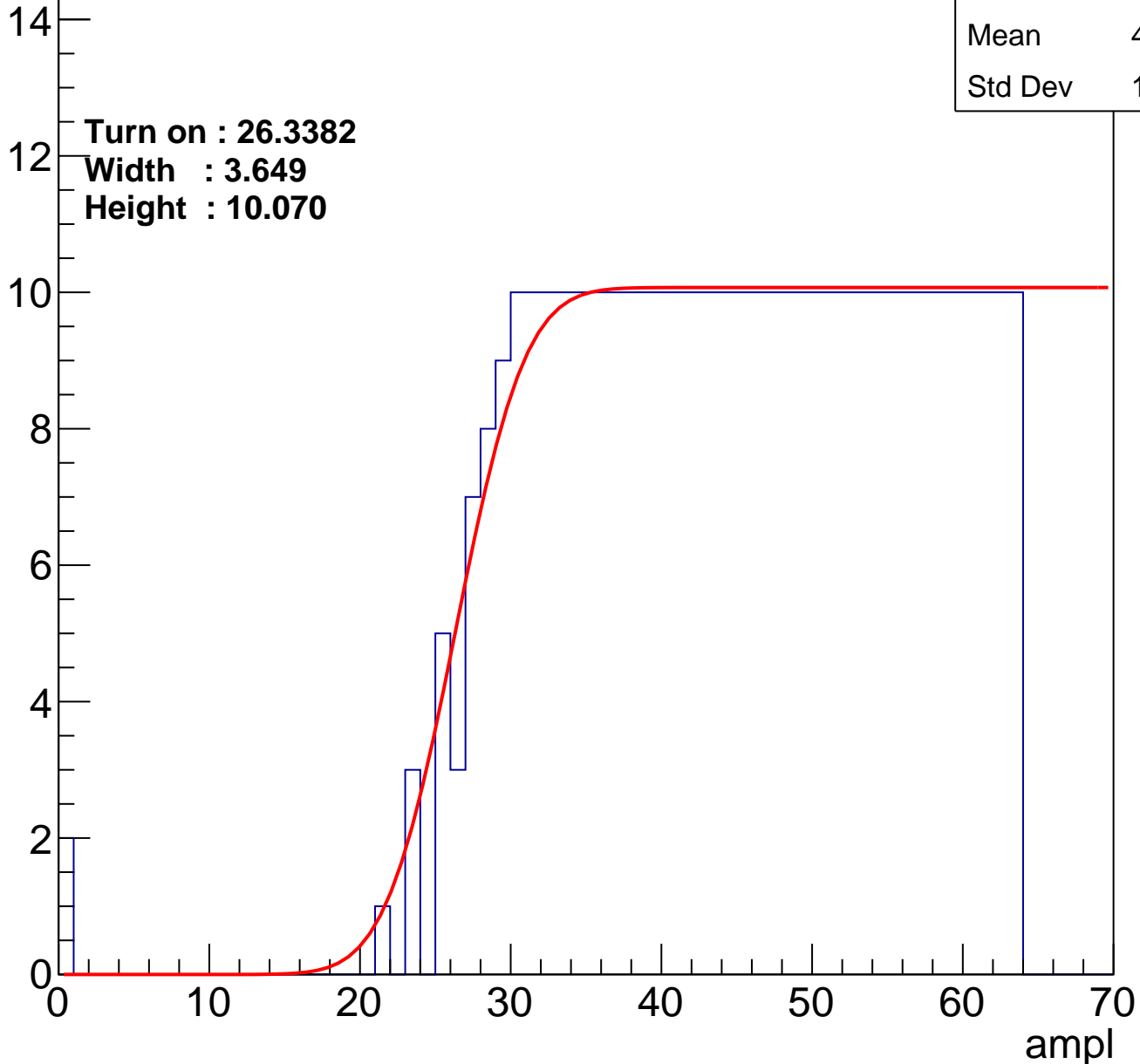
Entries	378
Mean	44.38
Std Dev	11.43

Turn on : 26.3382

Width : 3.649

Height : 10.070

Entry



B1L101S, U3-ch18

calib_packv5_042523_0143.root, FC#0, port D2

Entries	364
Mean	44.75
Std Dev	11.92

Turn on : 28.5683

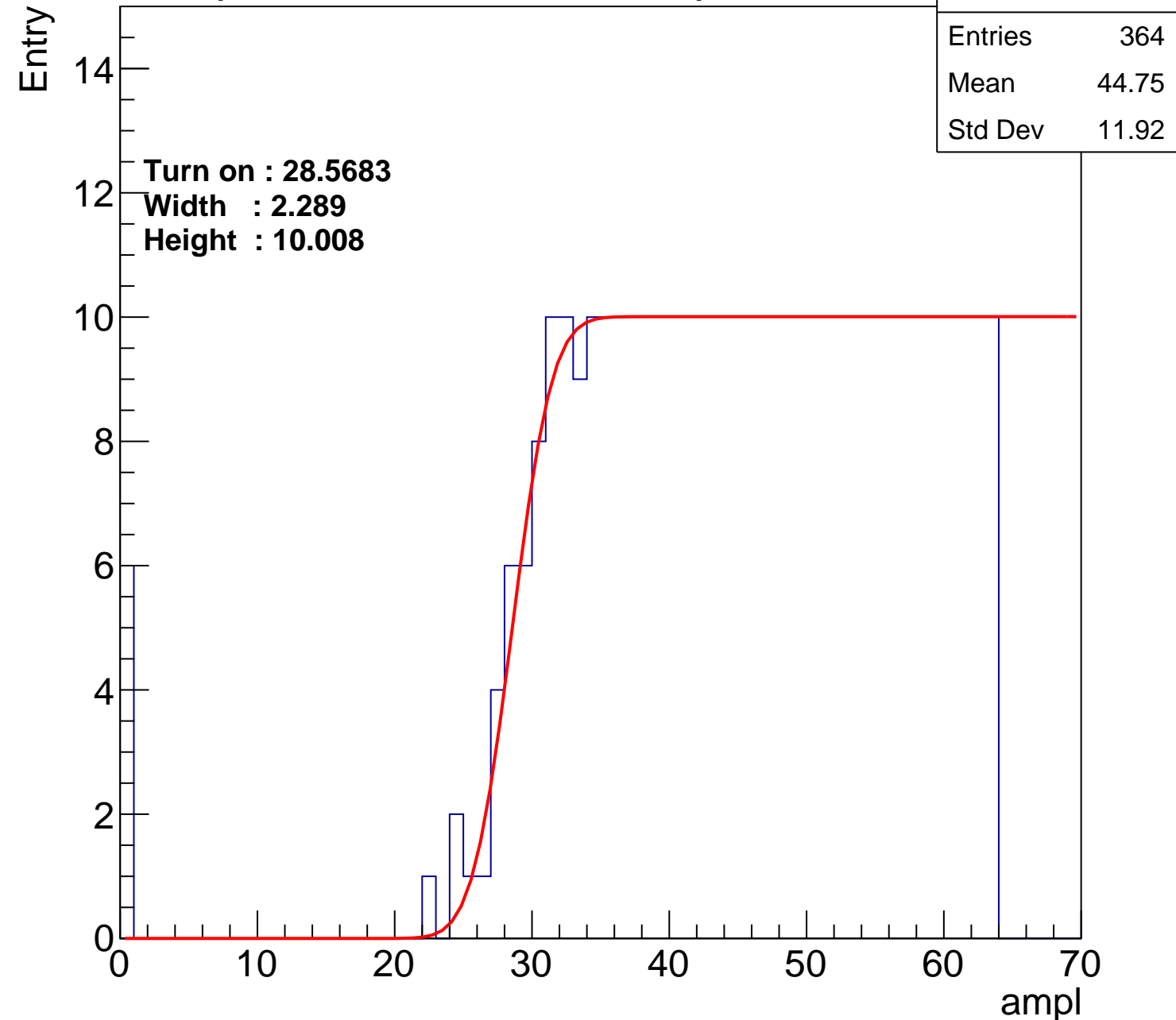
Width : 2.289

Height : 10.008

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch19

calib_packv5_042523_0143.root, FC#0, port D2

Entries	384
Mean	43.98
Std Dev	11.83

Turn on : 25.9937

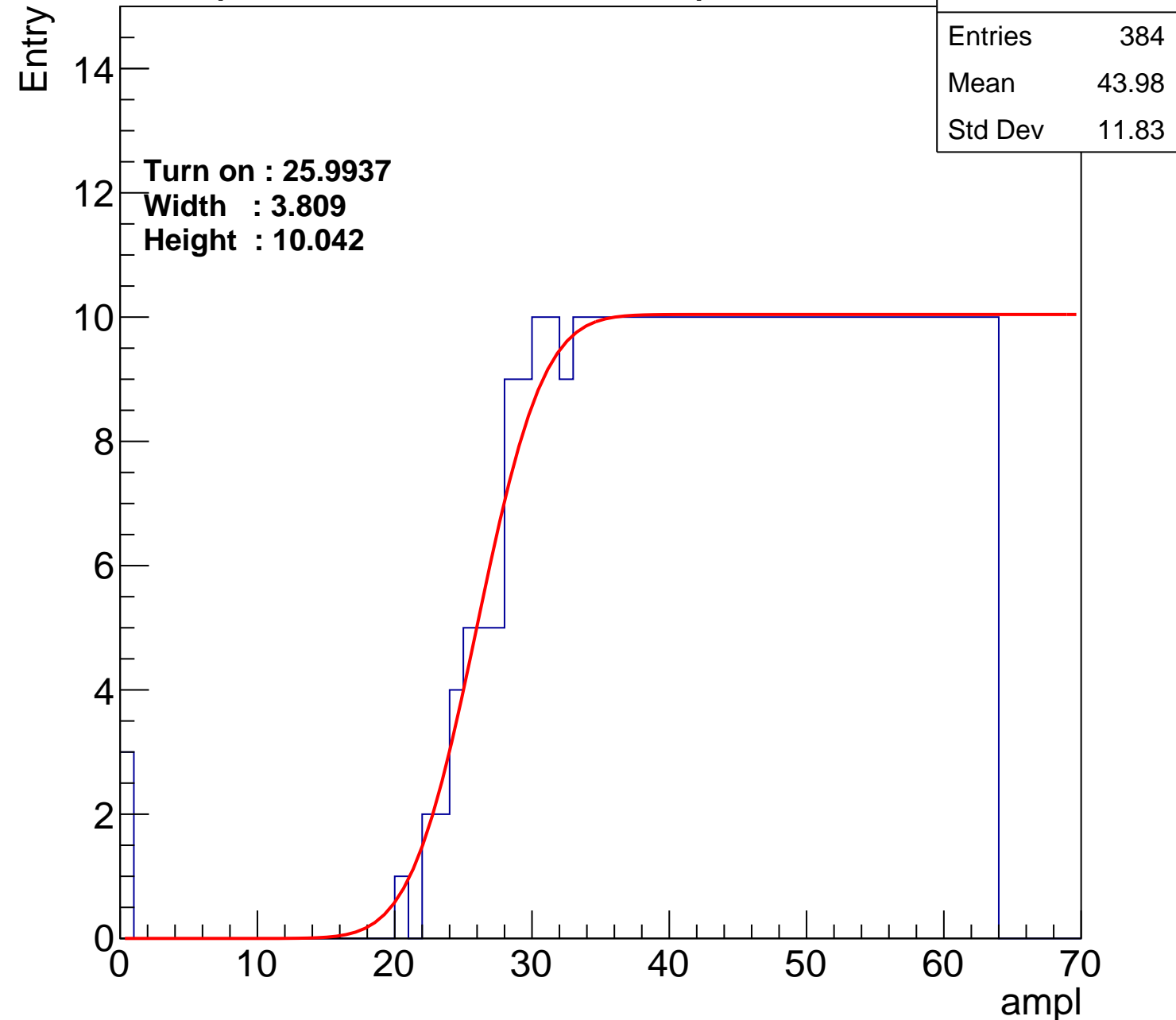
Width : 3.809

Height : 10.042

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch20

calib_packv5_042523_0143.root, FC#0, port D2

Entries	388
Mean	43.47
Std Dev	12.66

Turn on : 26.3408

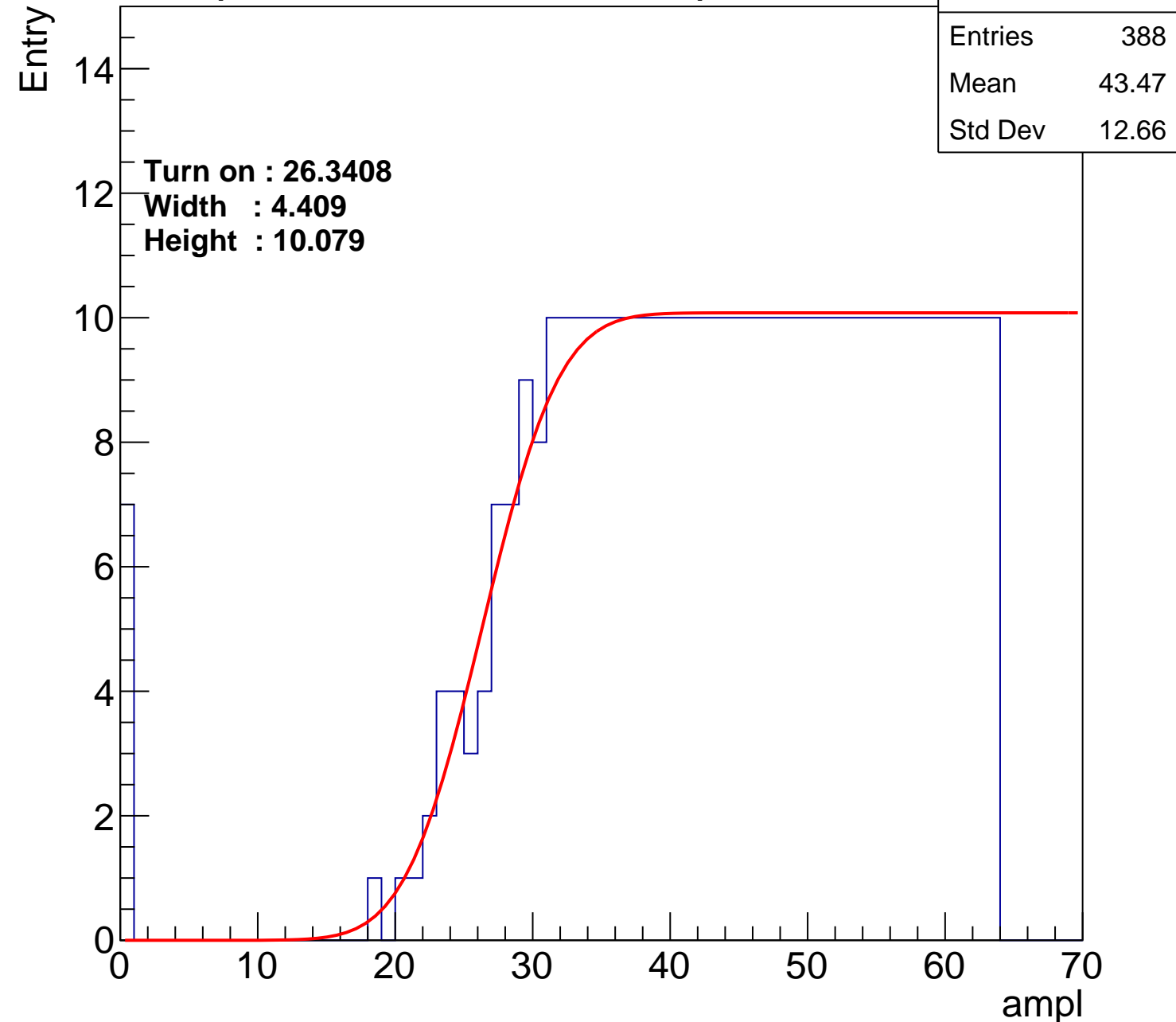
Width : 4.409

Height : 10.079

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch21

calib_packv5_042523_0143.root, FC#0, port D2

Entries	387
Mean	44
Std Dev	11.5

Turn on : 25.9624

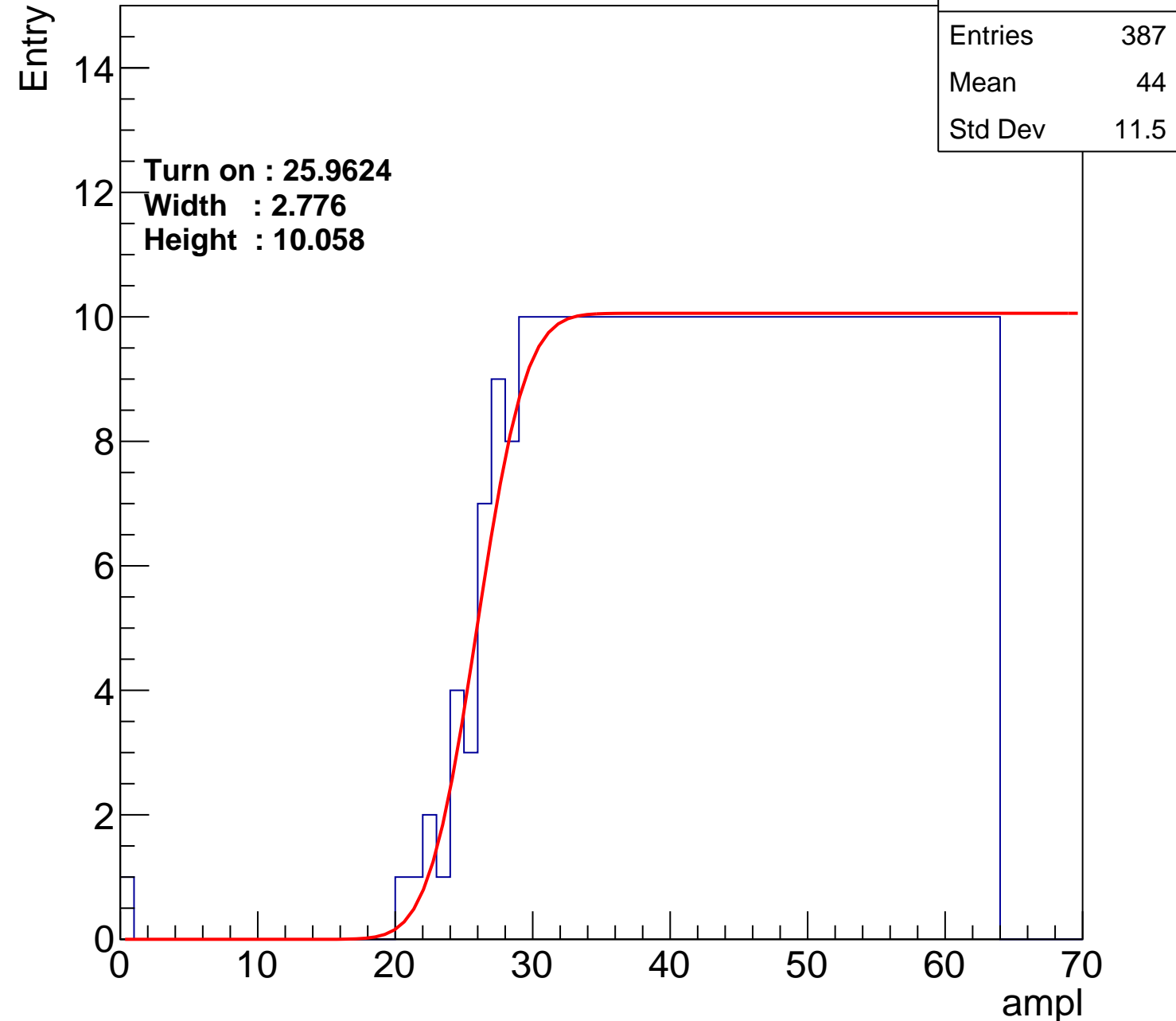
Width : 2.776

Height : 10.058

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch22

calib_packv5_042523_0143.root, FC#0, port D2

Entries	382
Mean	44
Std Dev	11.97

Turn on : 26.7003

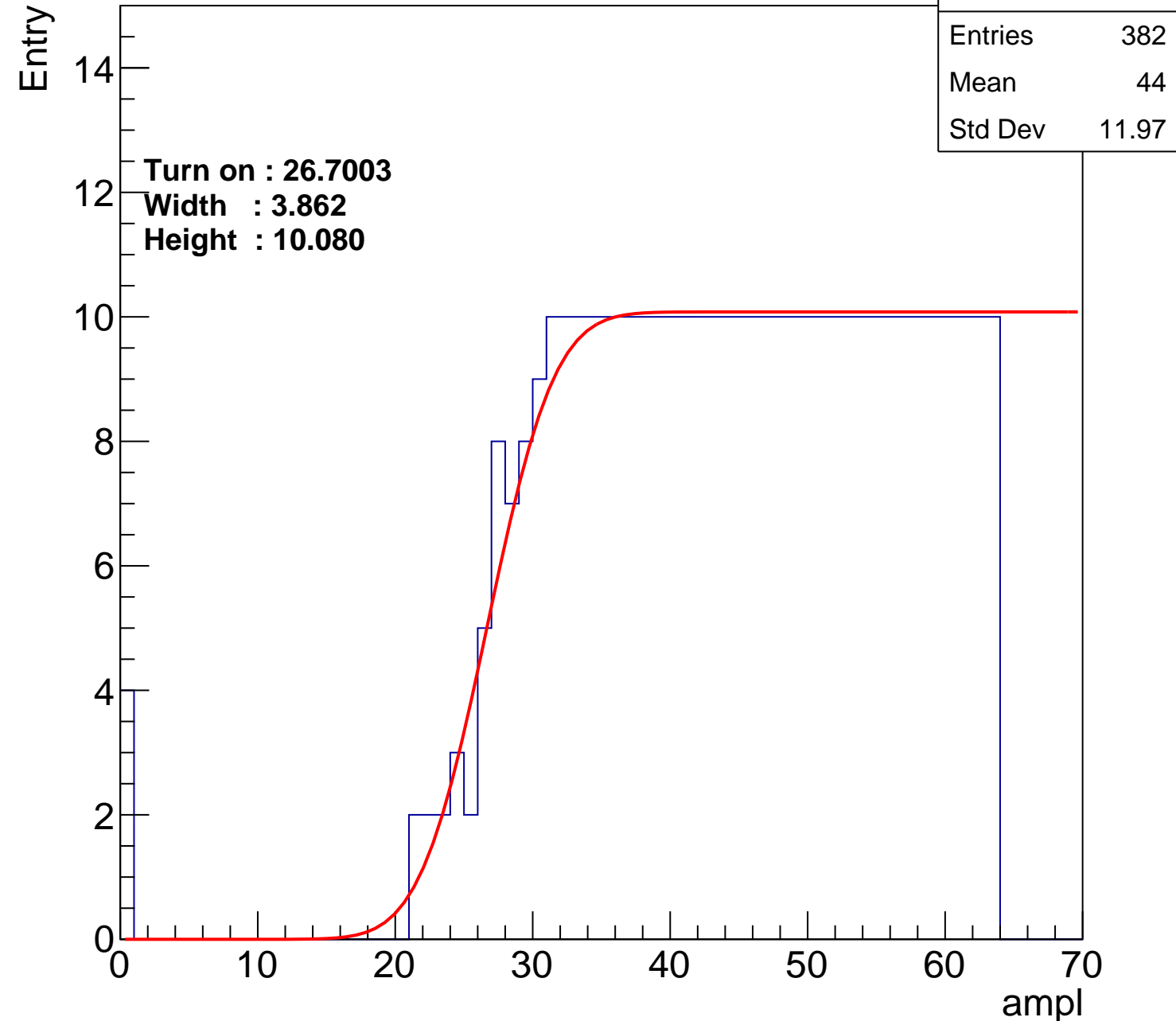
Width : 3.862

Height : 10.080

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch23

calib_packv5_042523_0143.root, FC#0, port D2

Entries	360
Mean	45.18
Std Dev	11.12

Turn on : 28.7844

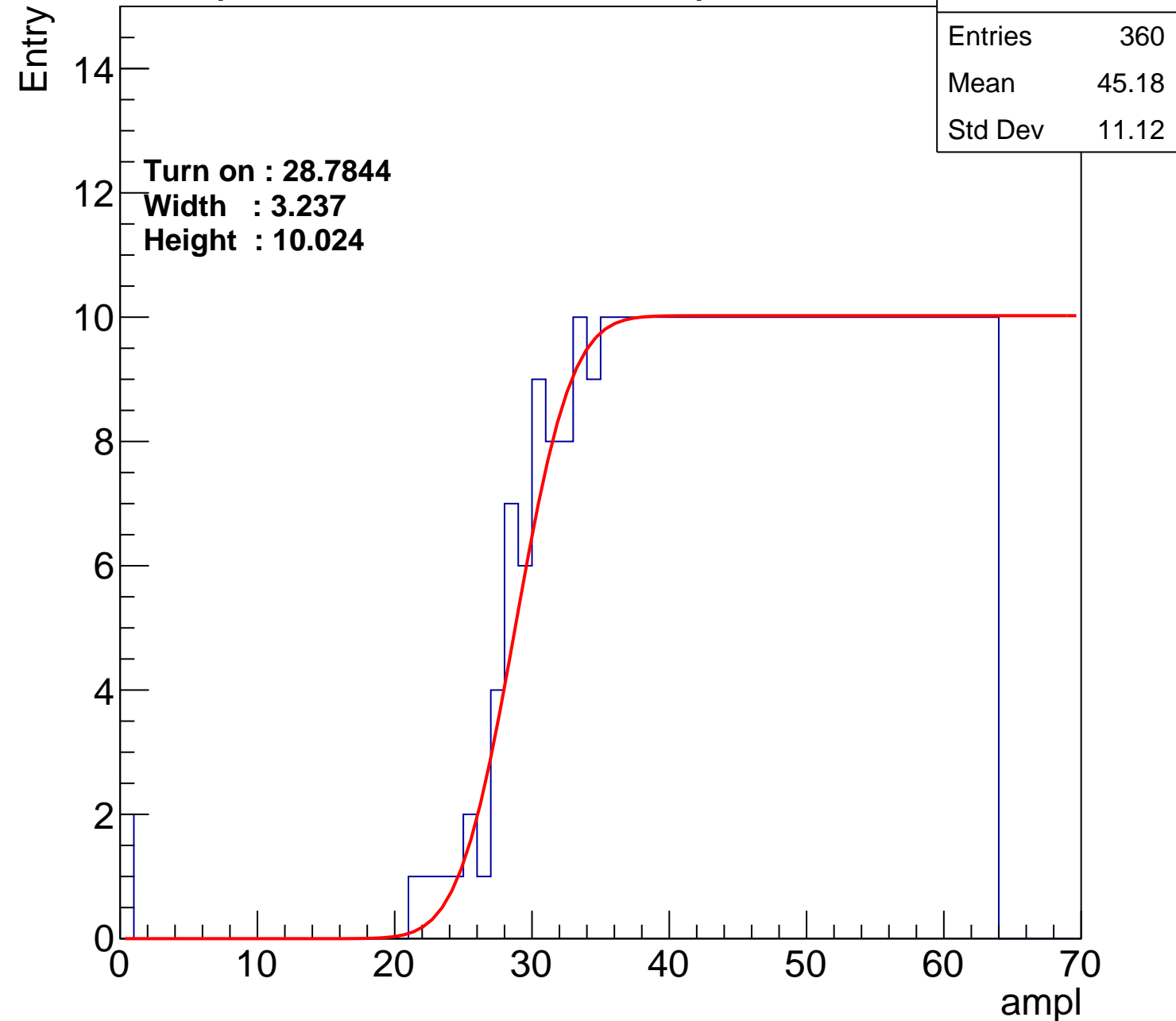
Width : 3.237

Height : 10.024

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch24

calib_packv5_042523_0143.root, FC#0, port D2

Entries	394
Mean	43.55
Std Dev	11.92

Turn on : 25.2733

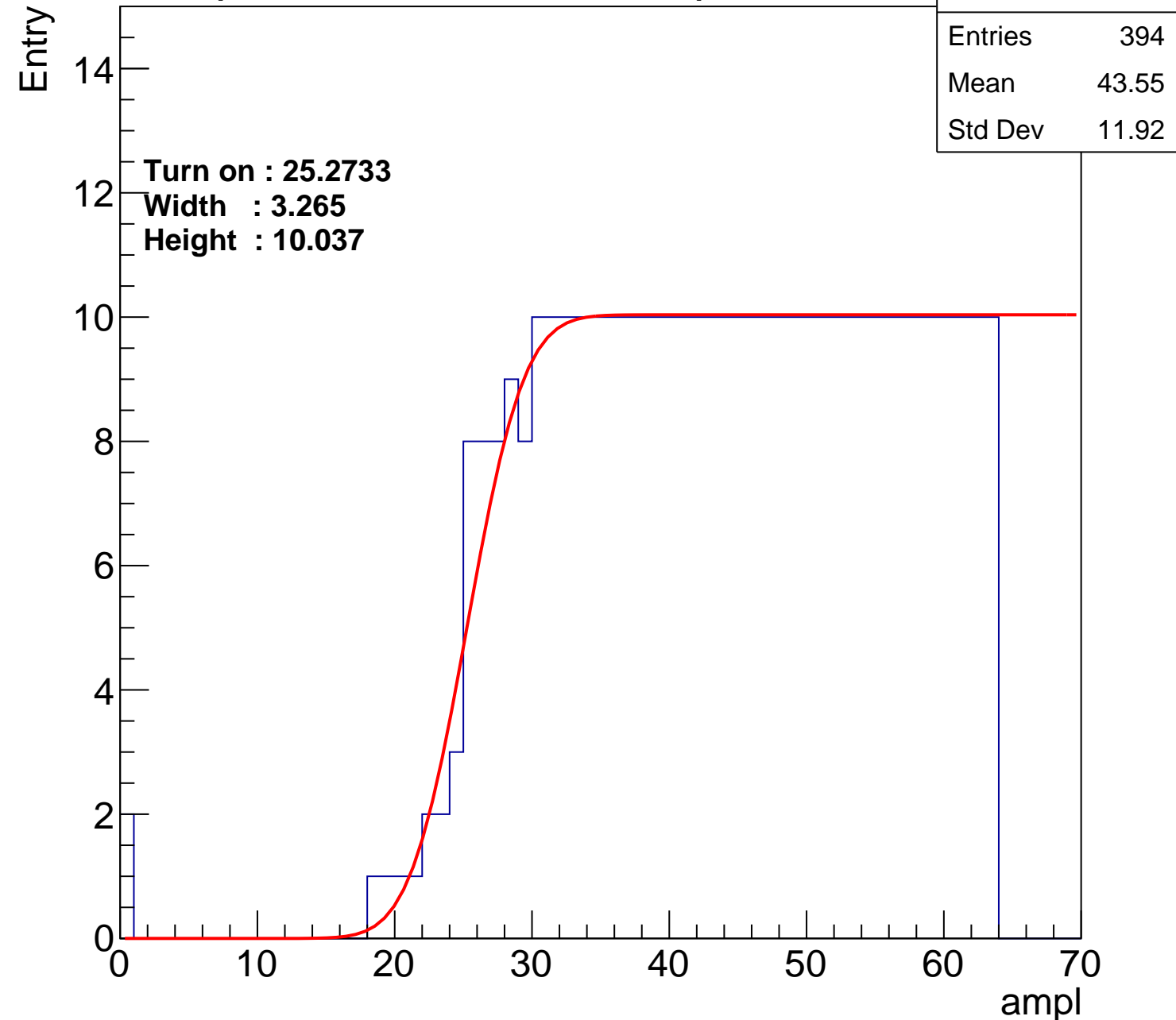
Width : 3.265

Height : 10.037

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch25

calib_packv5_042523_0143.root, FC#0, port D2

Entries	383
Mean	43.9
Std Dev	12.13

Turn on : 26.1088

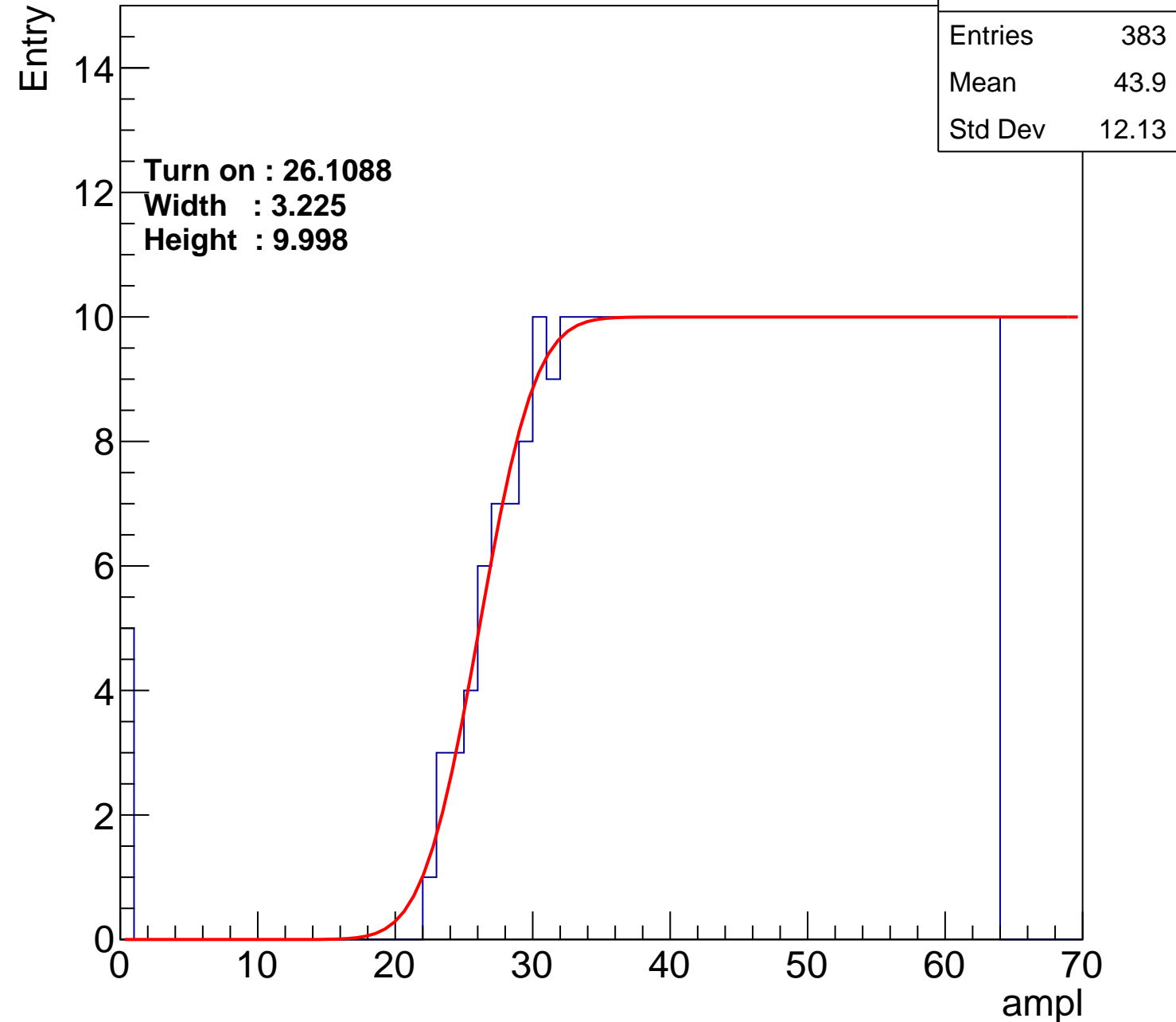
Width : 3.225

Height : 9.998

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch26

calib_packv5_042523_0143.root, FC#0, port D2

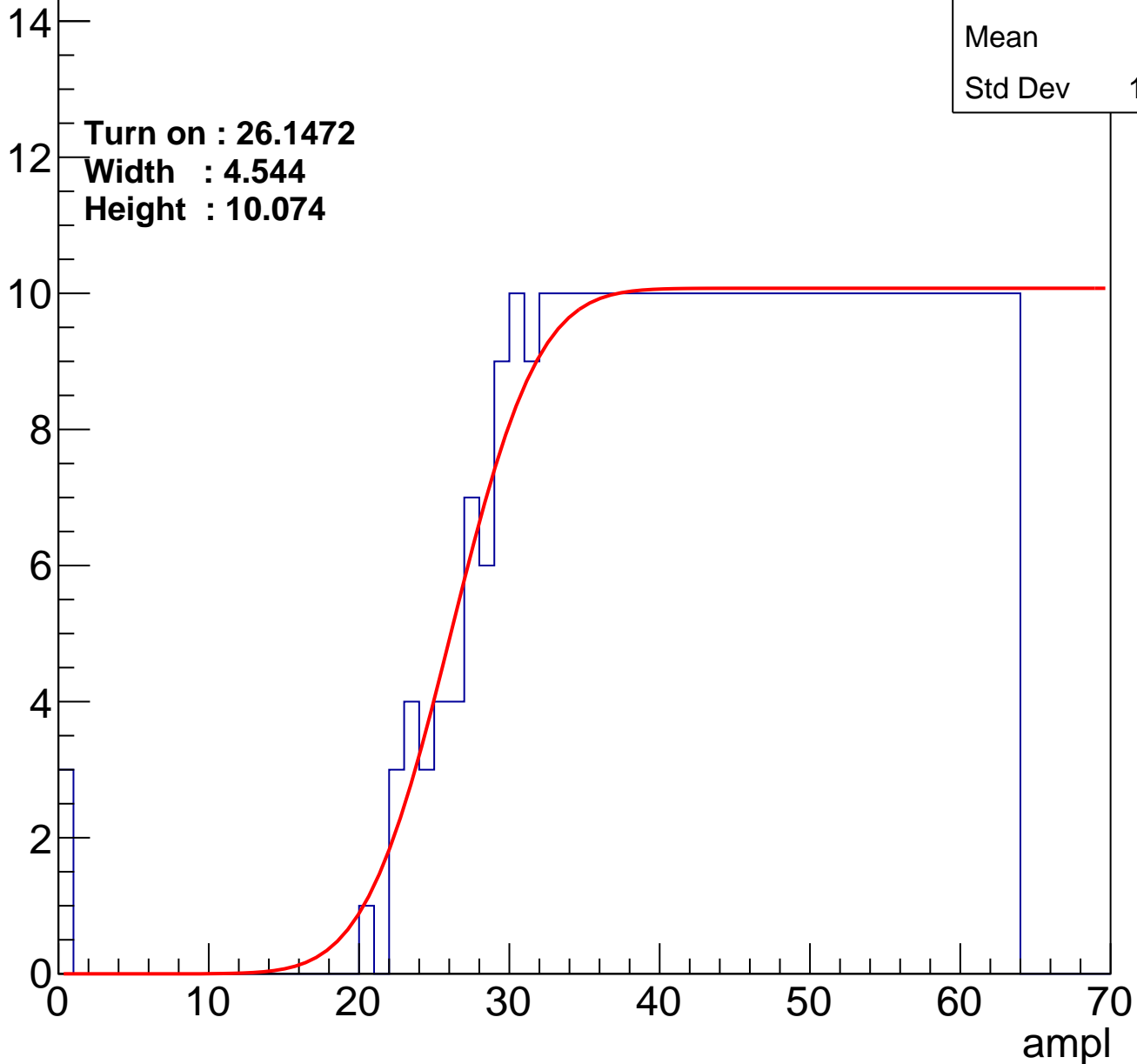
Entries	383
Mean	44
Std Dev	11.85

Turn on : 26.1472

Width : 4.544

Height : 10.074

Entry



B1L101S, U3-ch27

calib_packv5_042523_0143.root, FC#0, port D2

Entries	380
Mean	44.23
Std Dev	11.63

Turn on : 26.3725

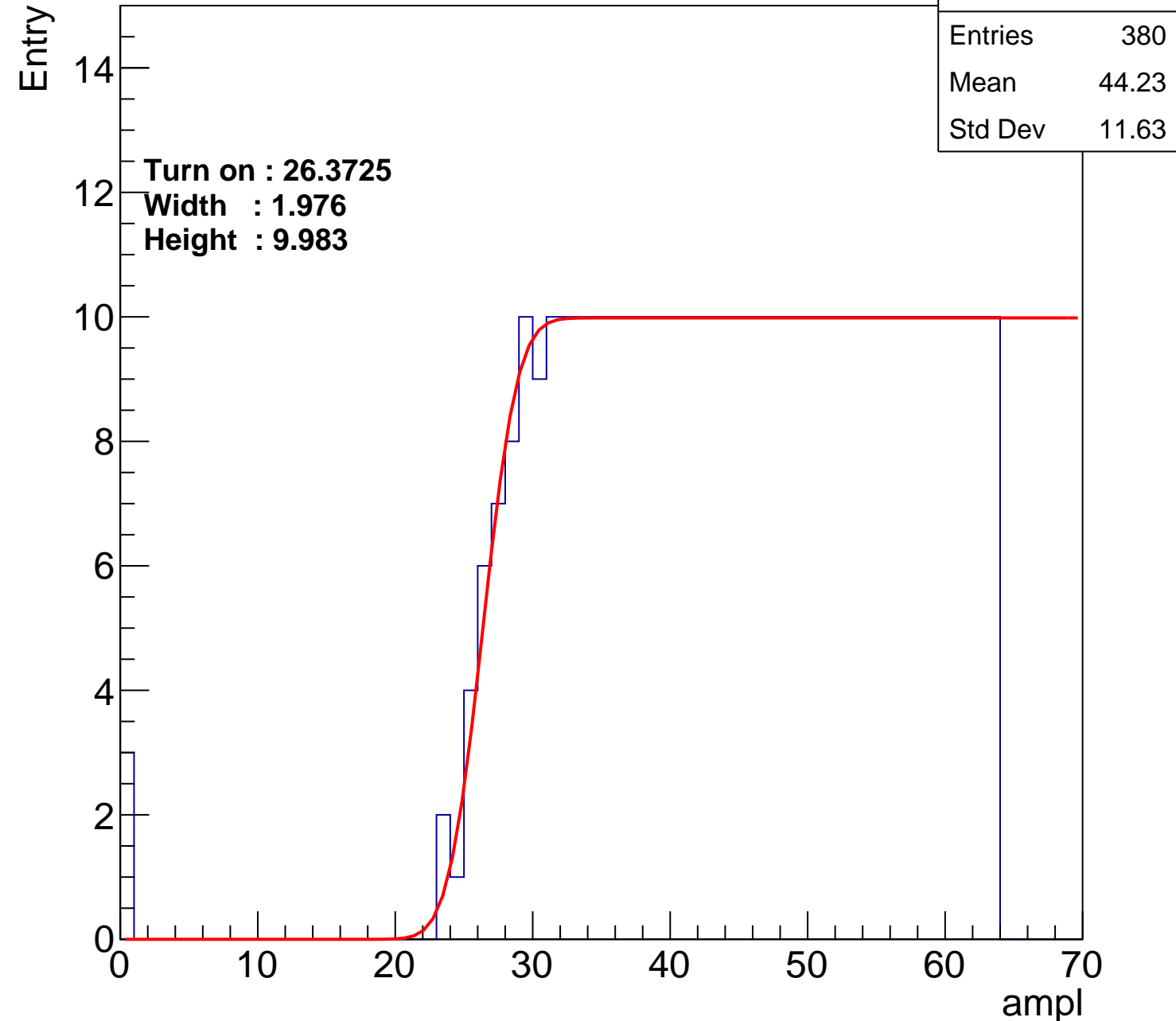
Width : 1.976

Height : 9.983

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch28

calib_packv5_042523_0143.root, FC#0, port D2

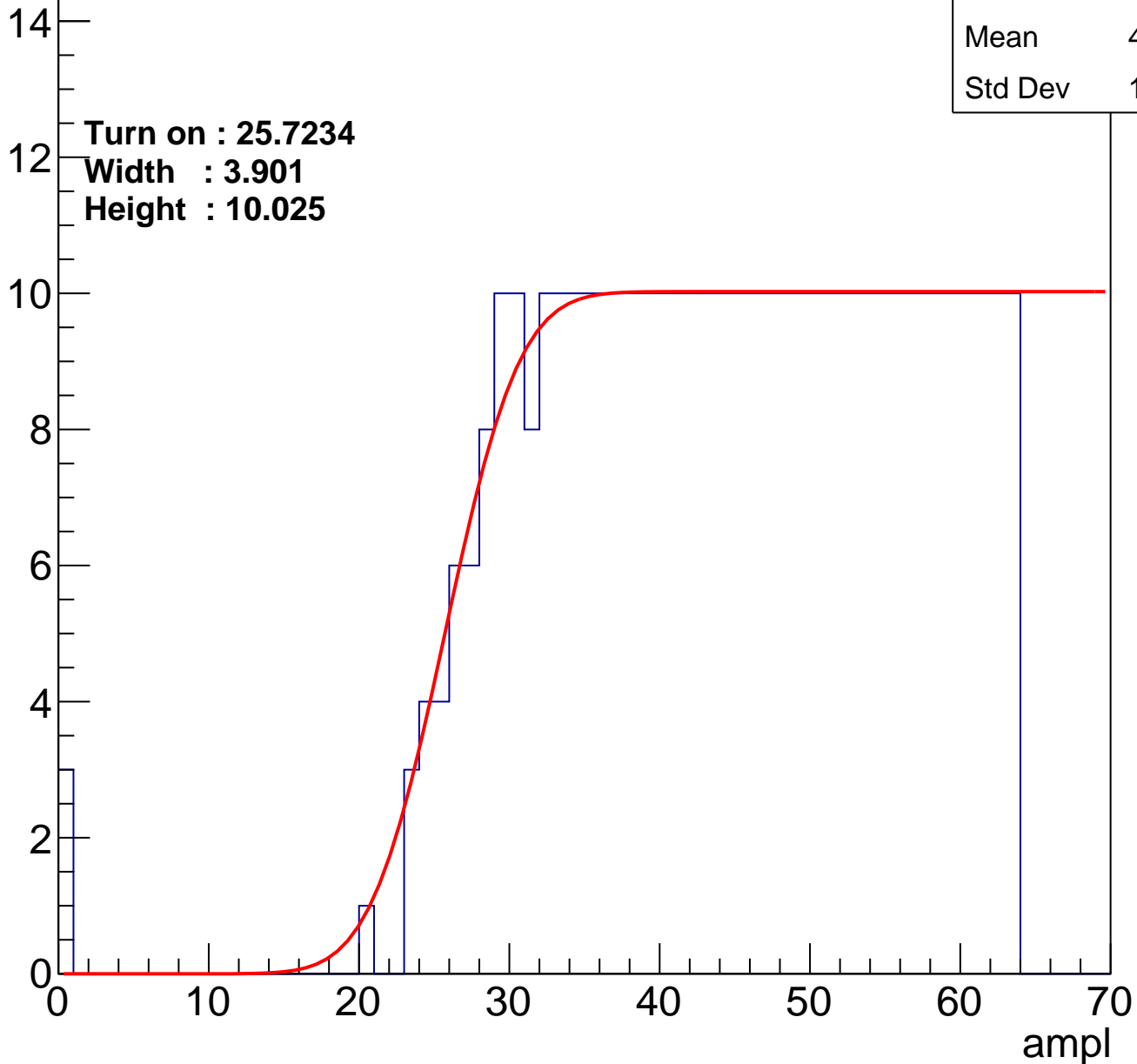
Entries	383
Mean	44.03
Std Dev	11.79

Turn on : 25.7234

Width : 3.901

Height : 10.025

Entry



B1L101S, U3-ch29

calib_packv5_042523_0143.root, FC#0, port D2

Entries	381
Mean	43.91
Std Dev	12.31

Turn on : 27.2222

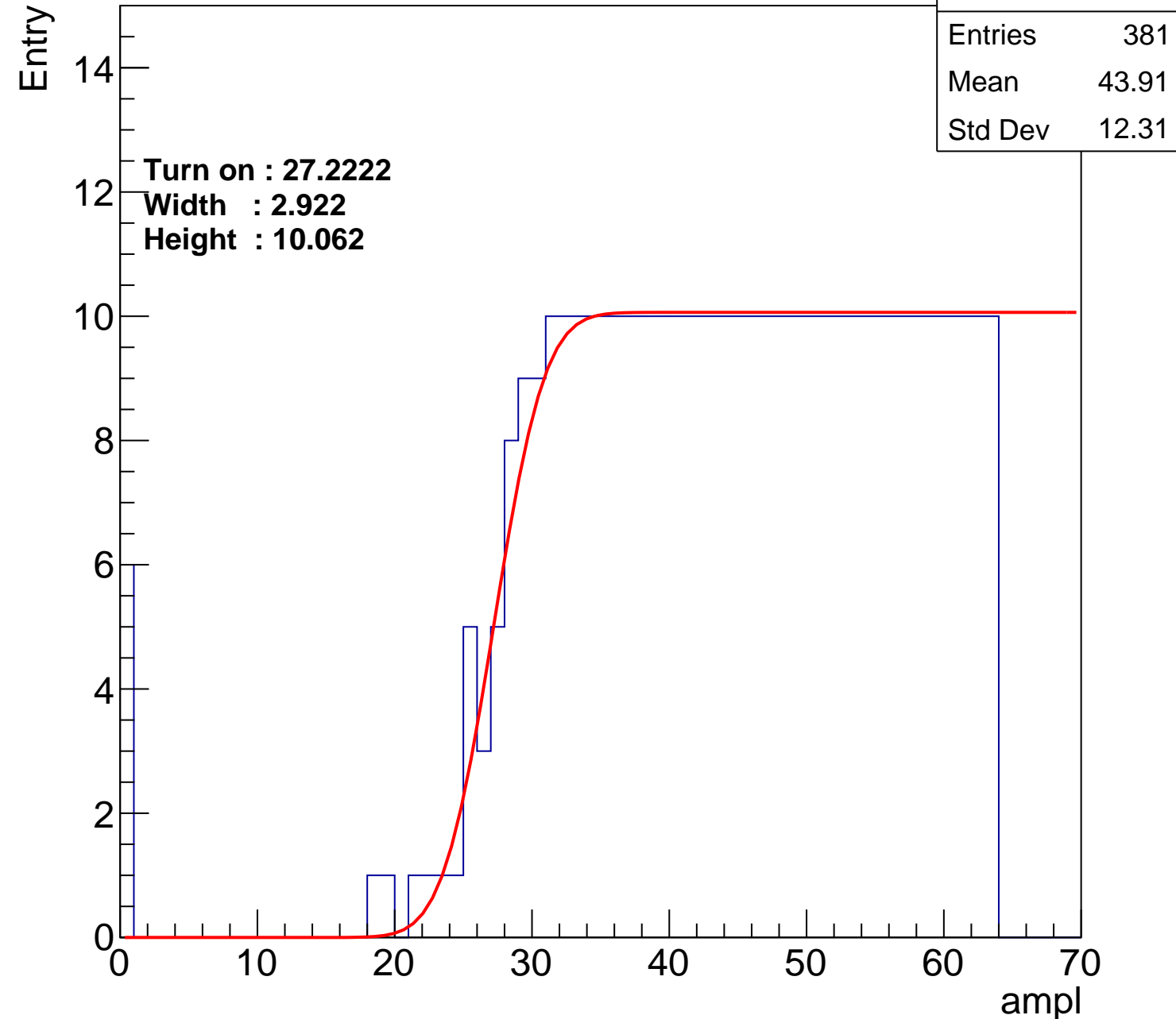
Width : 2.922

Height : 10.062

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch30

calib_packv5_042523_0143.root, FC#0, port D2

Entries	360
Mean	45.16
Std Dev	11.25

Turn on : 28.5827

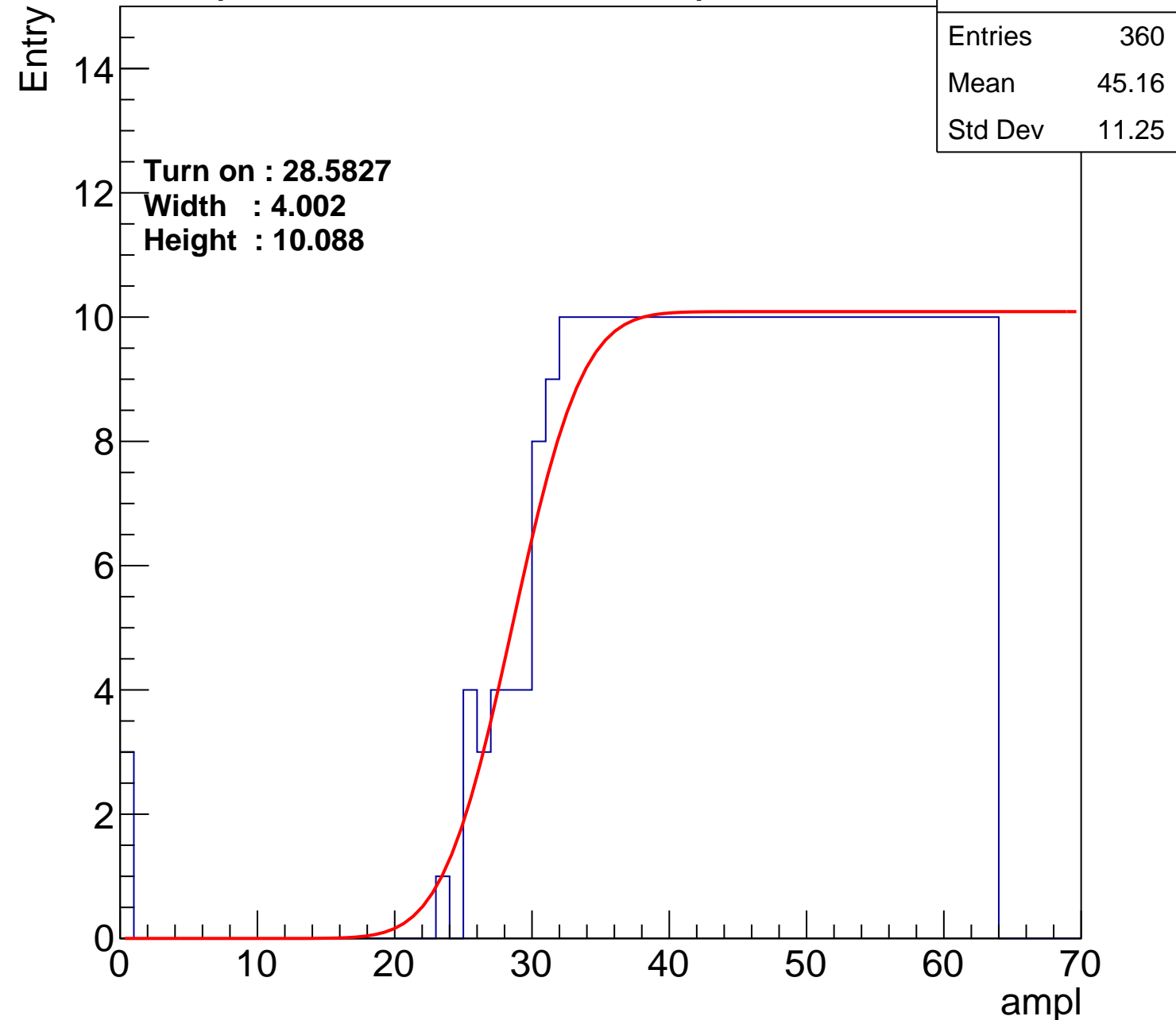
Width : 4.002

Height : 10.088

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch31

calib_packv5_042523_0143.root, FC#0, port D2

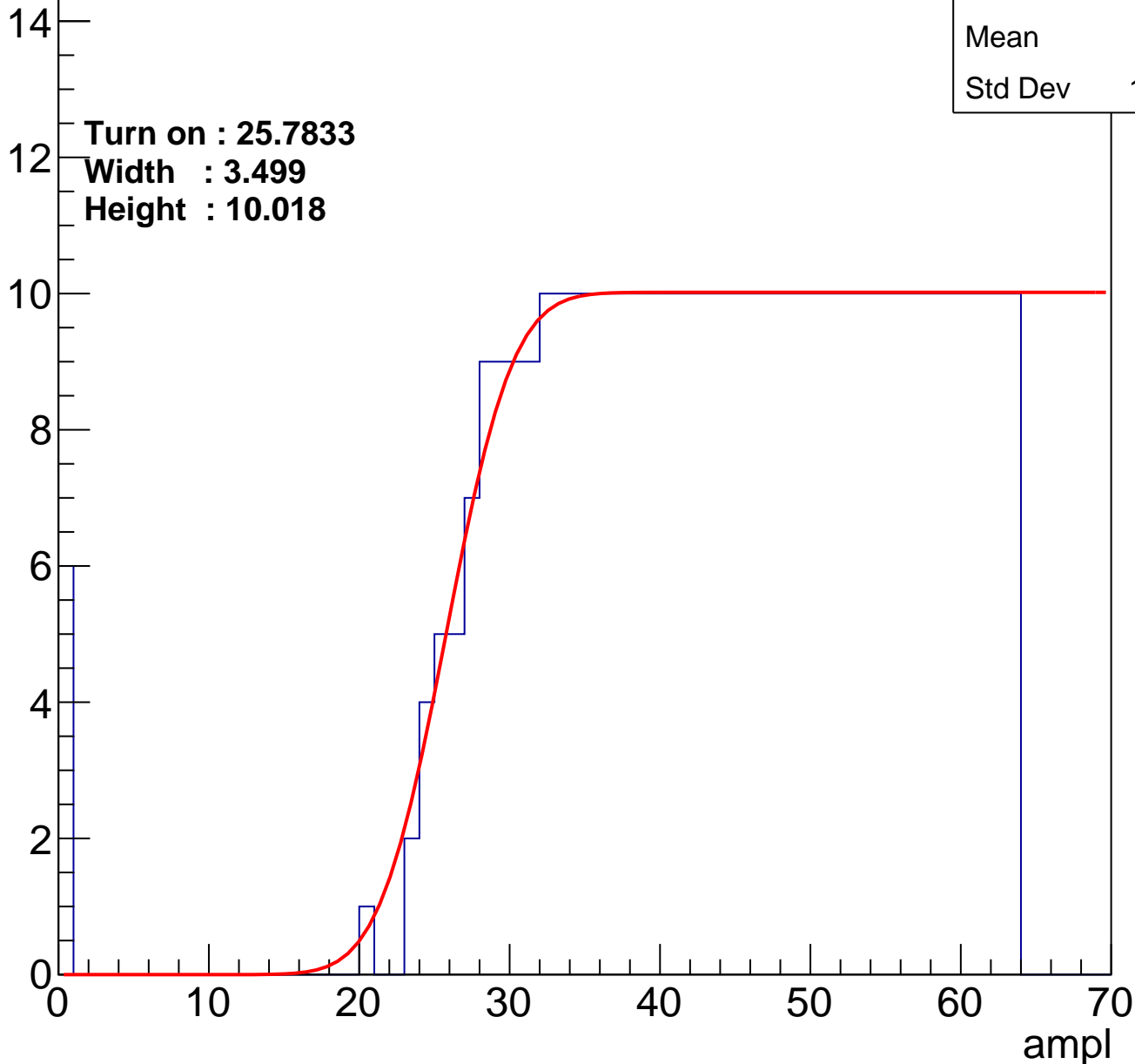
Entries	386
Mean	43.7
Std Dev	12.35

Turn on : 25.7833

Width : 3.499

Height : 10.018

Entry



B1L101S, U3-ch32

calib_packv5_042523_0143.root, FC#0, port D2

Entries	383
Mean	44.03
Std Dev	11.8

Turn on : 25.9831

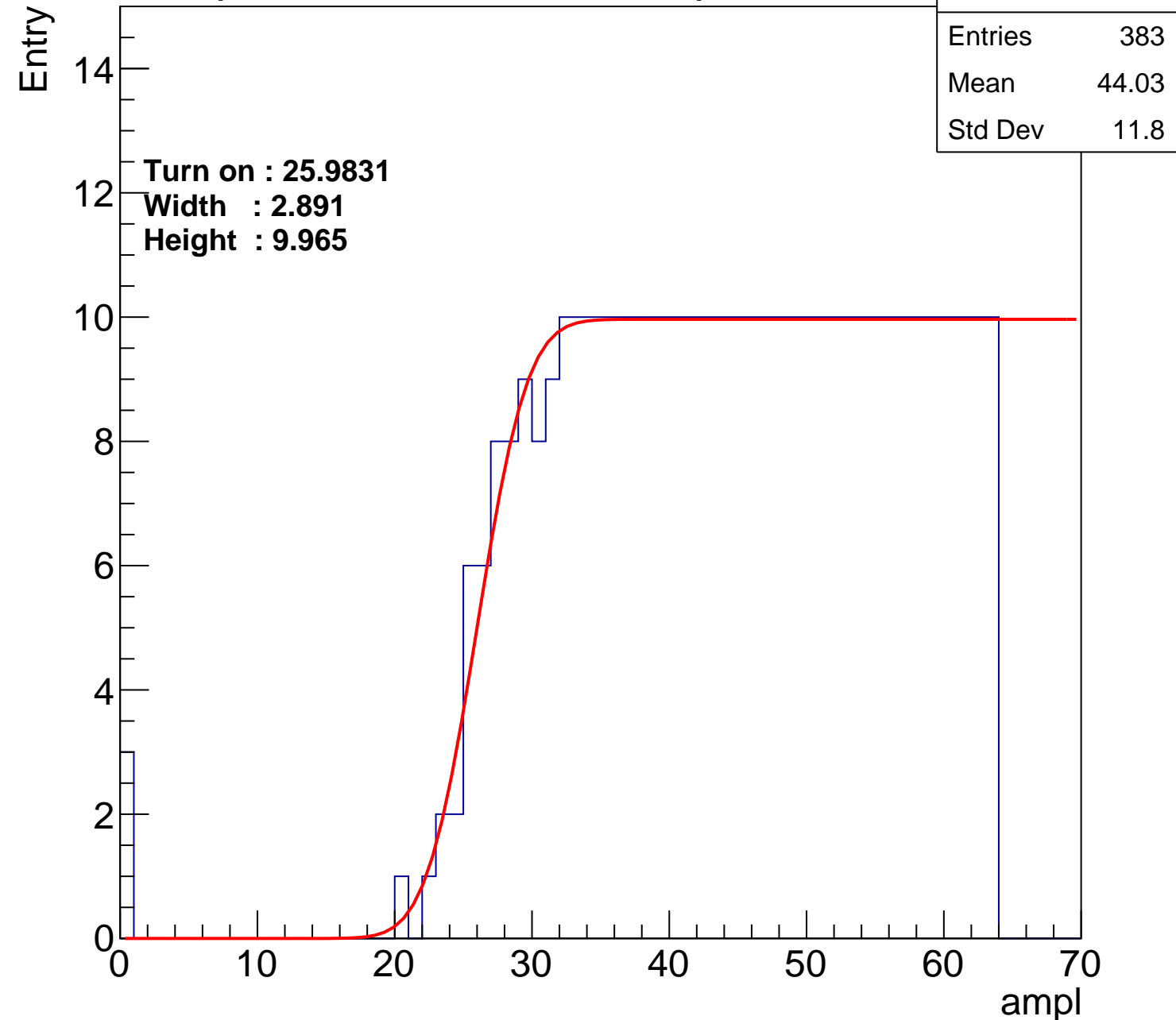
Width : 2.891

Height : 9.965

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch33

calib_packv5_042523_0143.root, FC#0, port D2

Entries	400
Mean	43.04
Std Dev	12.57

Turn on : 24.5430

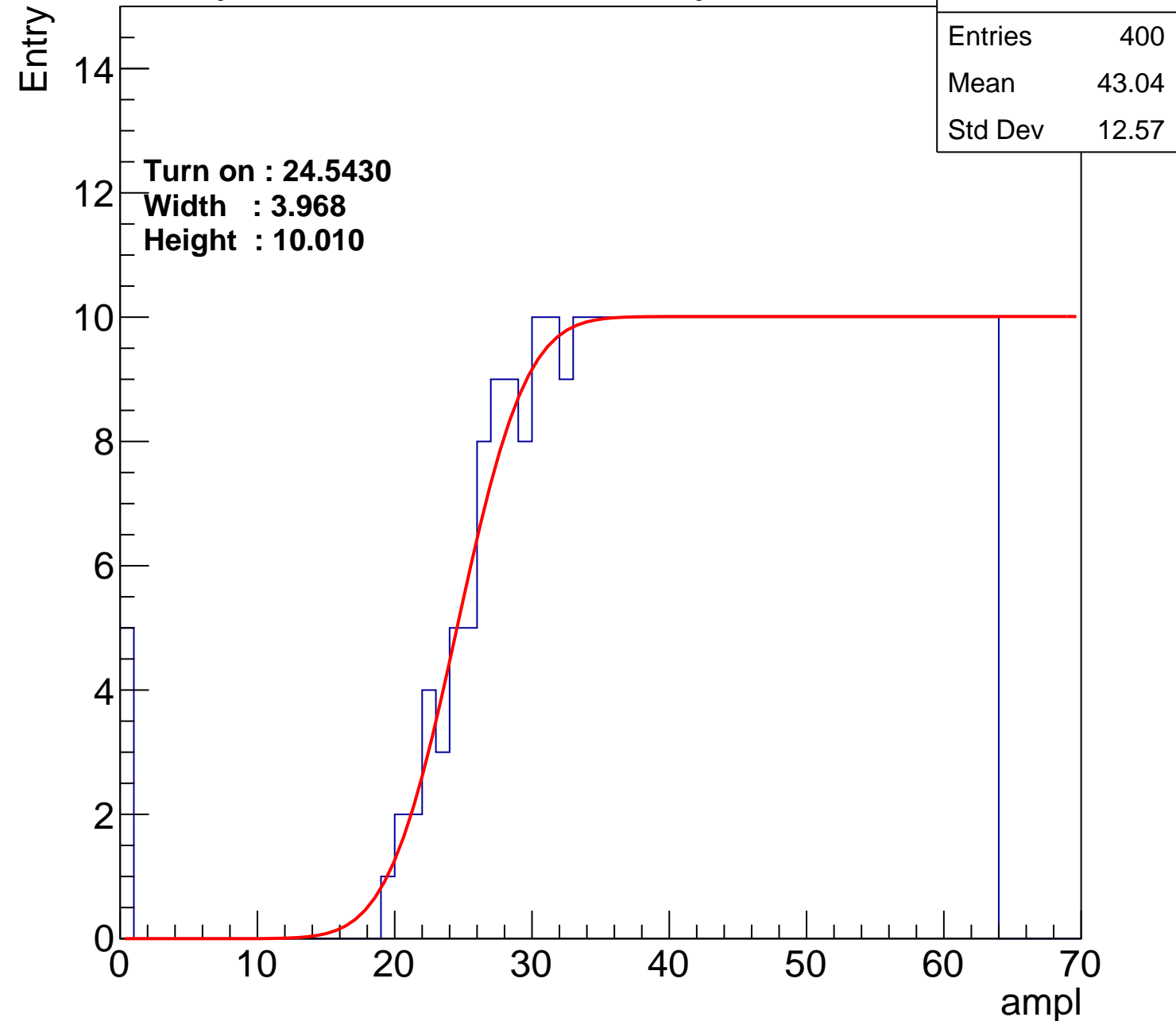
Width : 3.968

Height : 10.010

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch34

calib_packv5_042523_0143.root, FC#0, port D2

Entries	378
Mean	44.02
Std Dev	12.3

Turn on : 27.9203

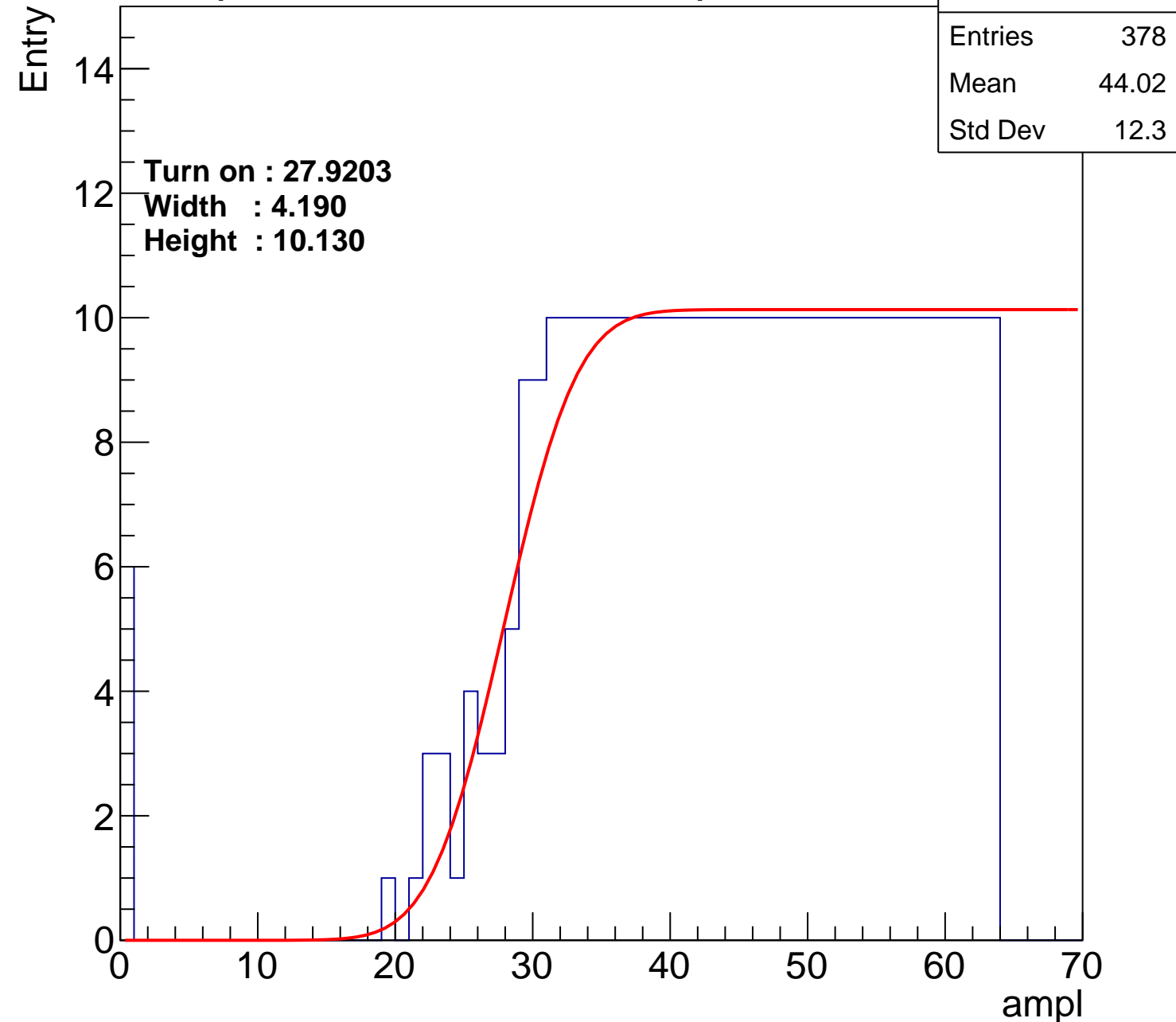
Width : 4.190

Height : 10.130

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch35

calib_packv5_042523_0143.root, FC#0, port D2

Entries	373
Mean	44.44
Std Dev	11.92

Turn on : 28.0229

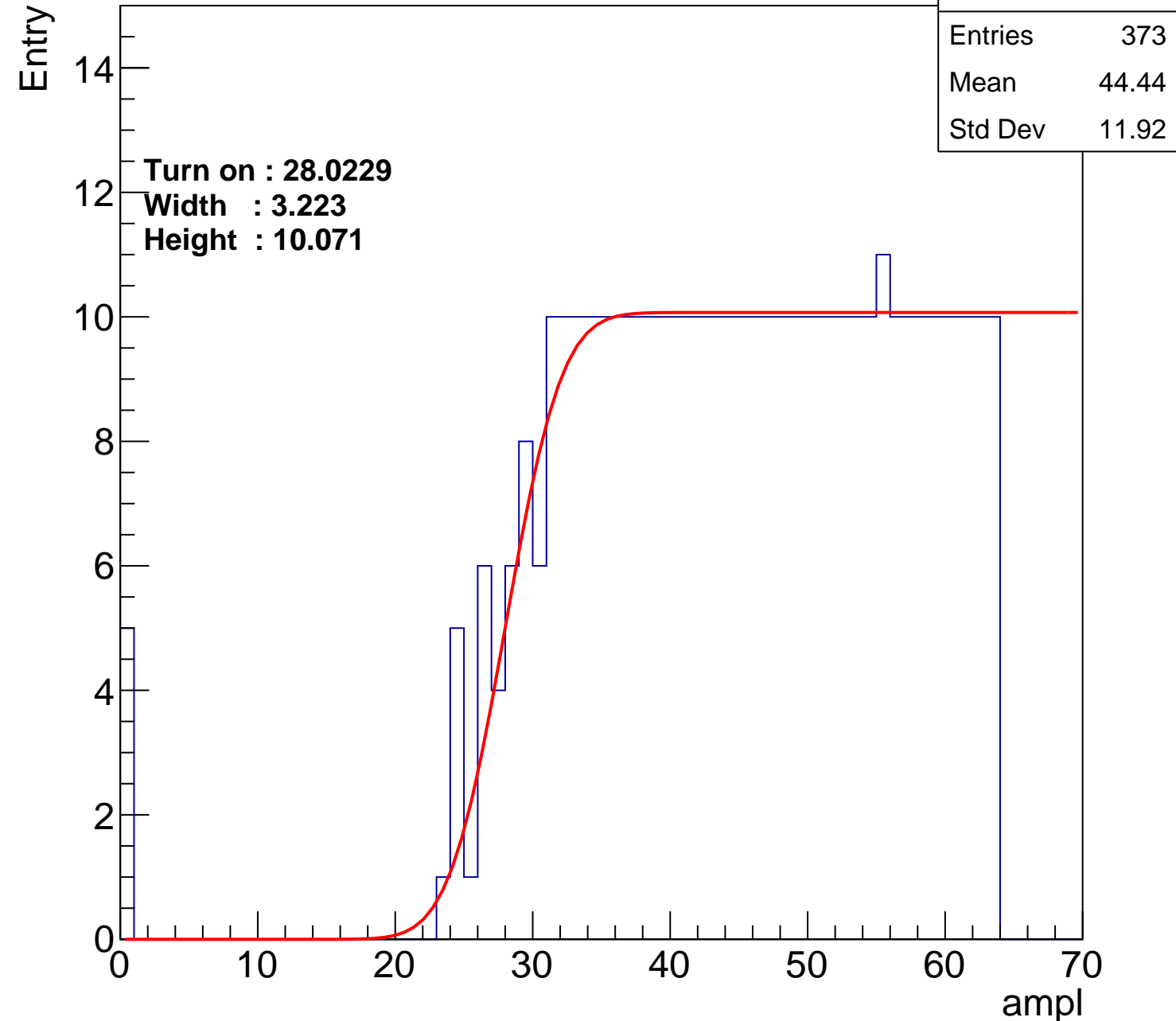
Width : 3.223

Height : 10.071

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch36

calib_packv5_042523_0143.root, FC#0, port D2

Entries	381
Mean	44.1
Std Dev	11.87

Turn on : 26.7810

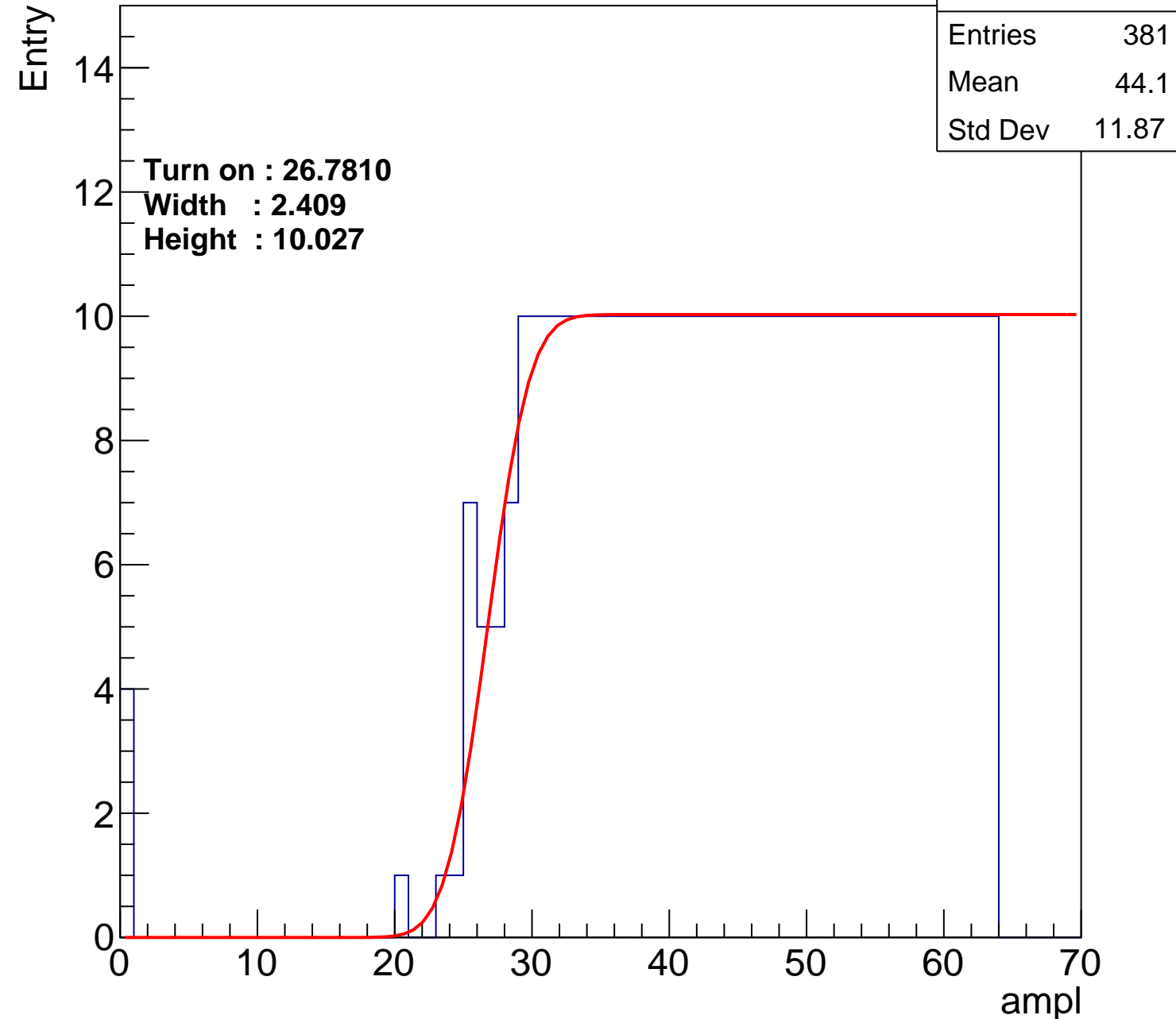
Width : 2.409

Height : 10.027

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch37

calib_packv5_042523_0143.root, FC#0, port D2

Entries	372
Mean	44.49
Std Dev	11.73

Turn on : 27.4853

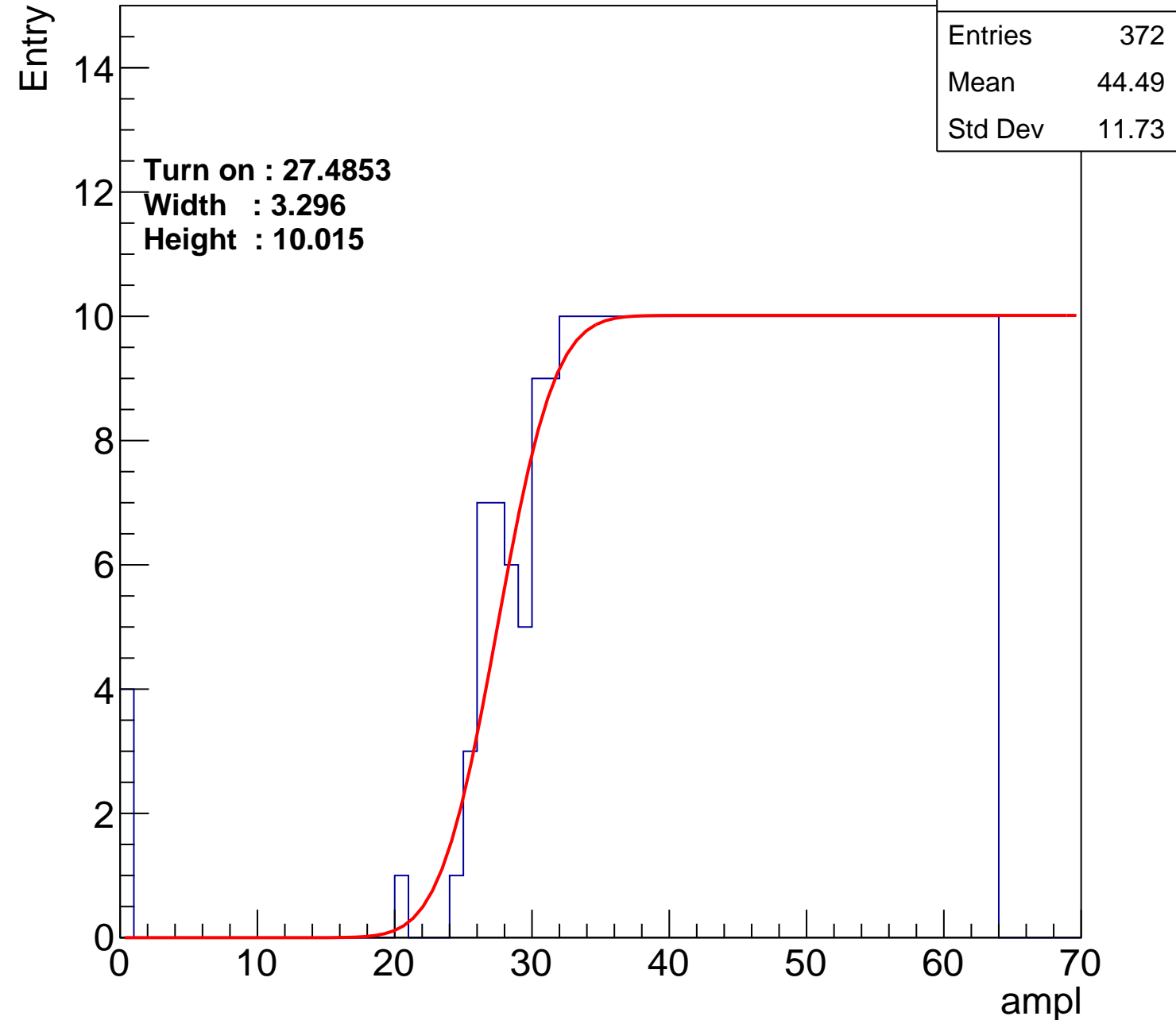
Width : 3.296

Height : 10.015

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch38

calib_packv5_042523_0143.root, FC#0, port D2

Entries	379
Mean	44.15
Std Dev	11.97

Turn on : 26.5416

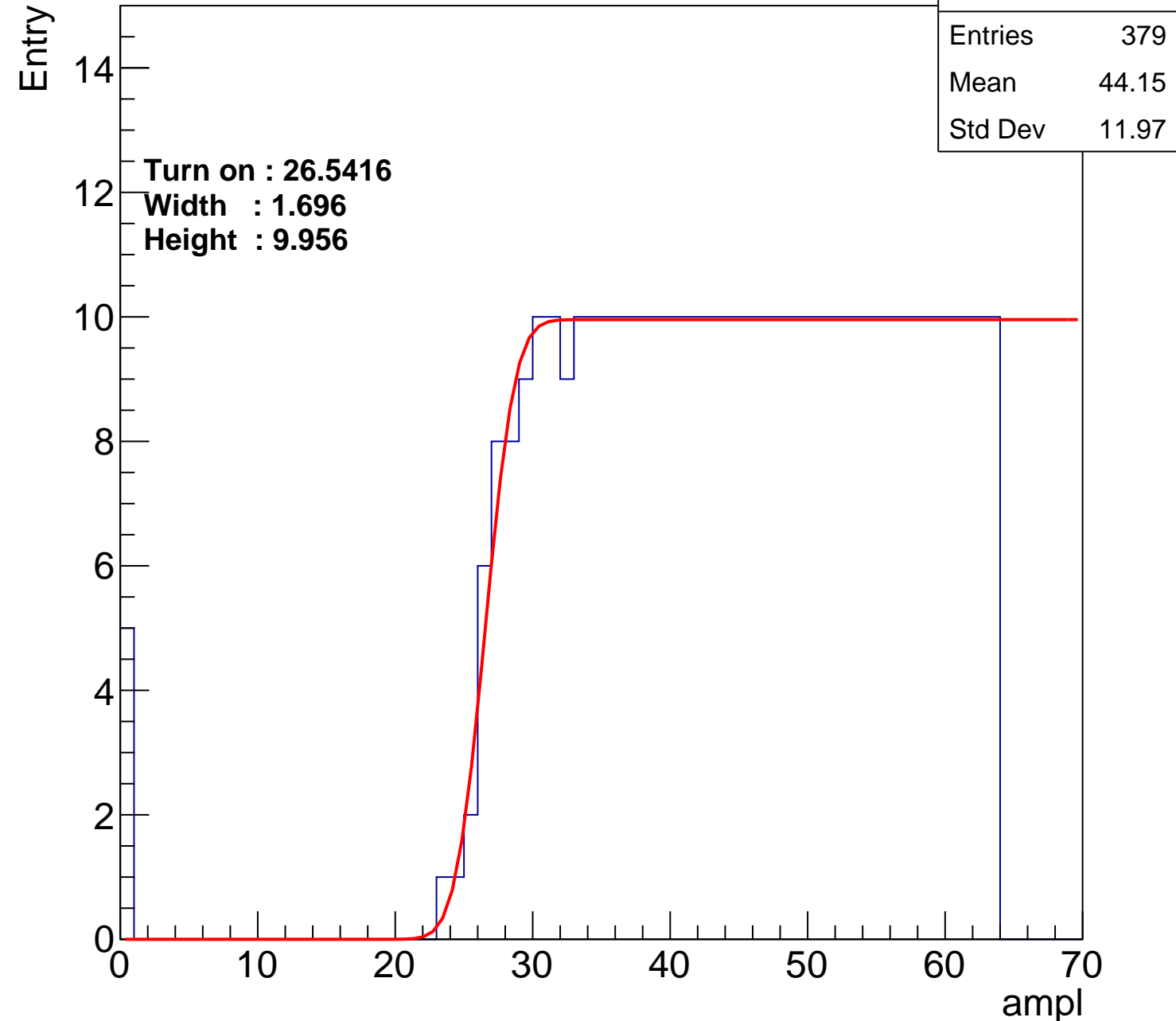
Width : 1.696

Height : 9.956

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch39

calib_packv5_042523_0143.root, FC#0, port D2

Entries	374
Mean	44.44
Std Dev	11.7

Turn on : 27.1124

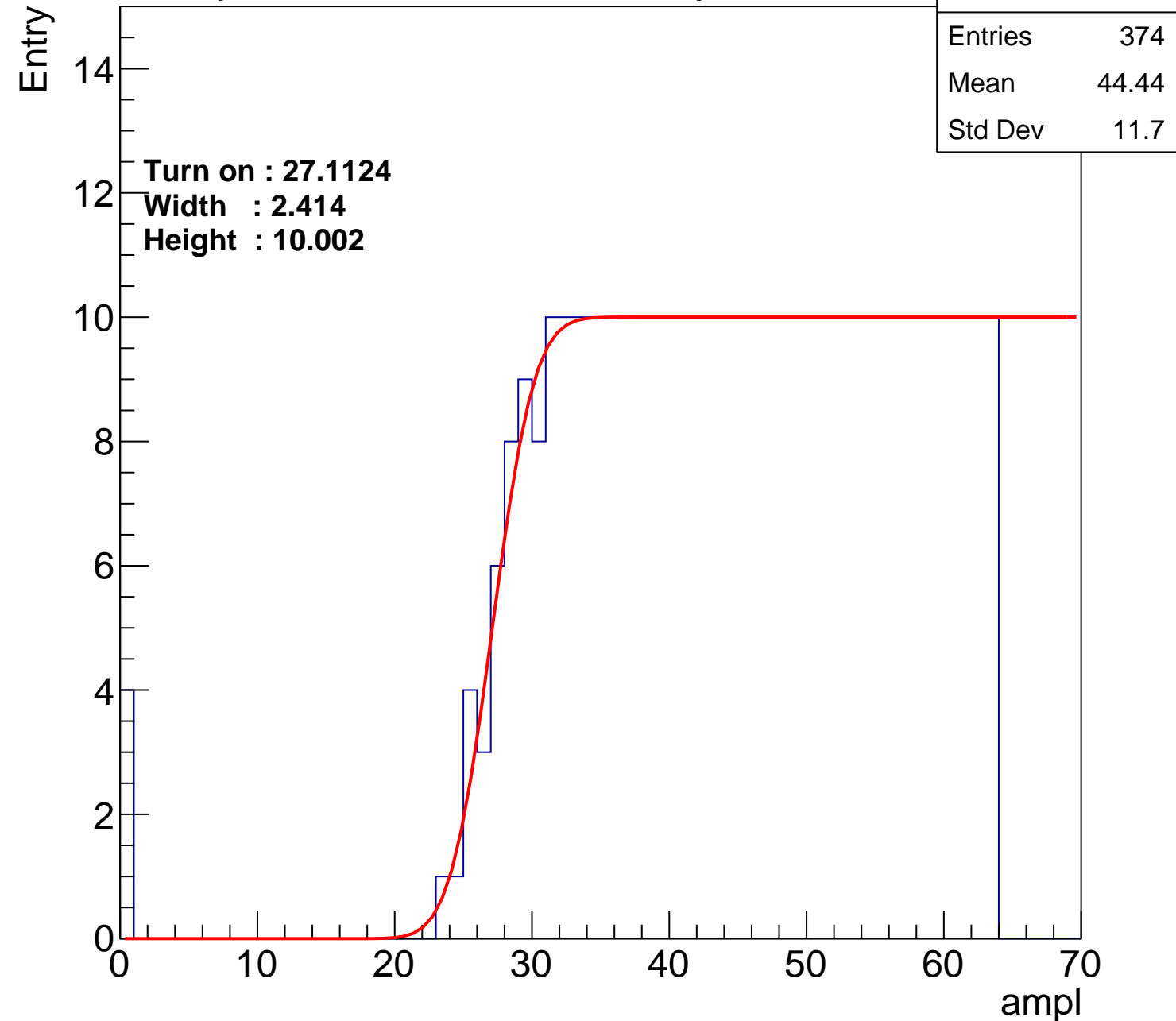
Width : 2.414

Height : 10.002

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch40

calib_packv5_042523_0143.root, FC#0, port D2

Entries	386
Mean	43.88
Std Dev	11.88

Turn on : 26.3644

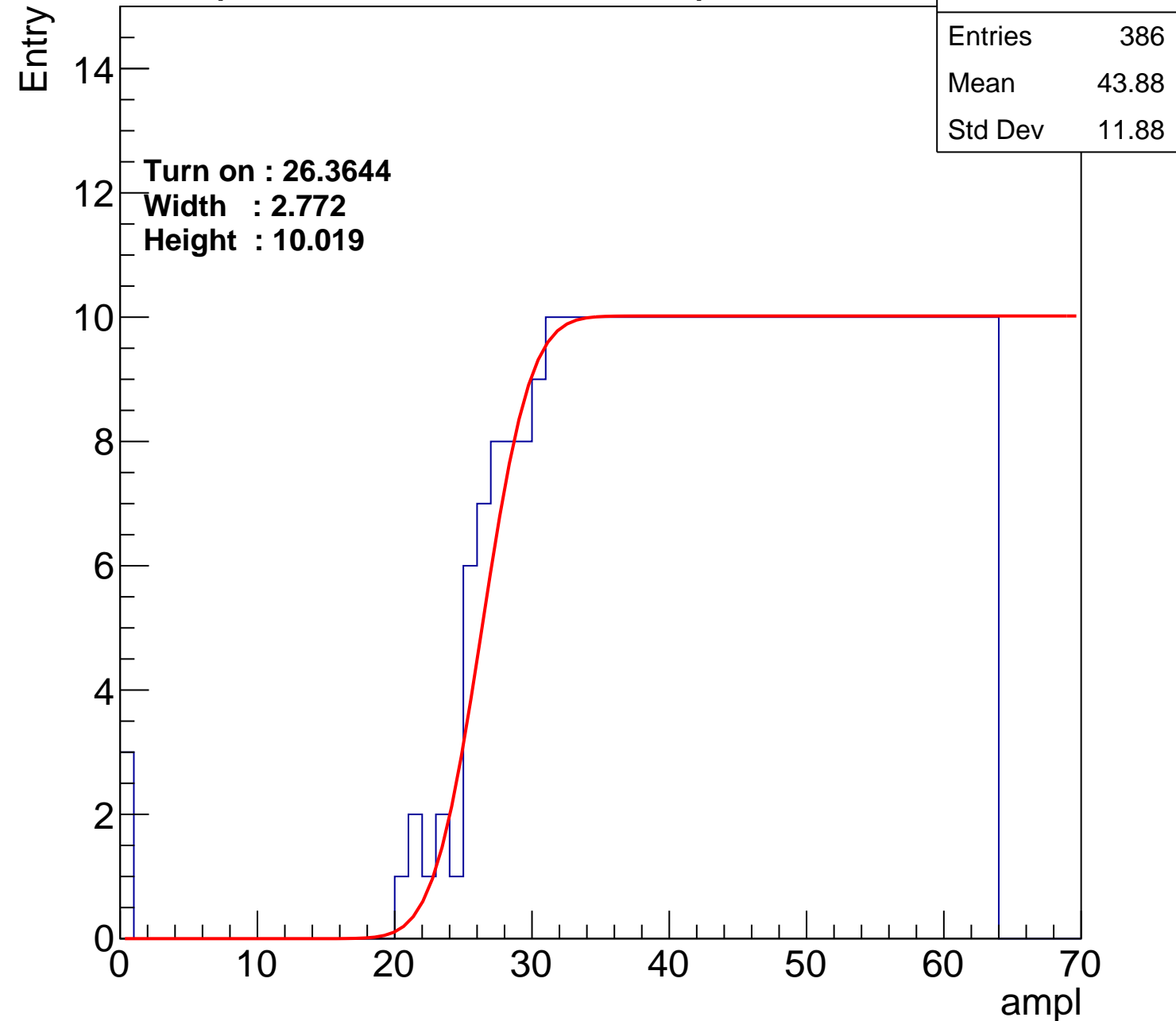
Width : 2.772

Height : 10.019

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch41

calib_packv5_042523_0143.root, FC#0, port D2

Entries	381
Mean	44.06
Std Dev	11.92

Turn on : 26.1464

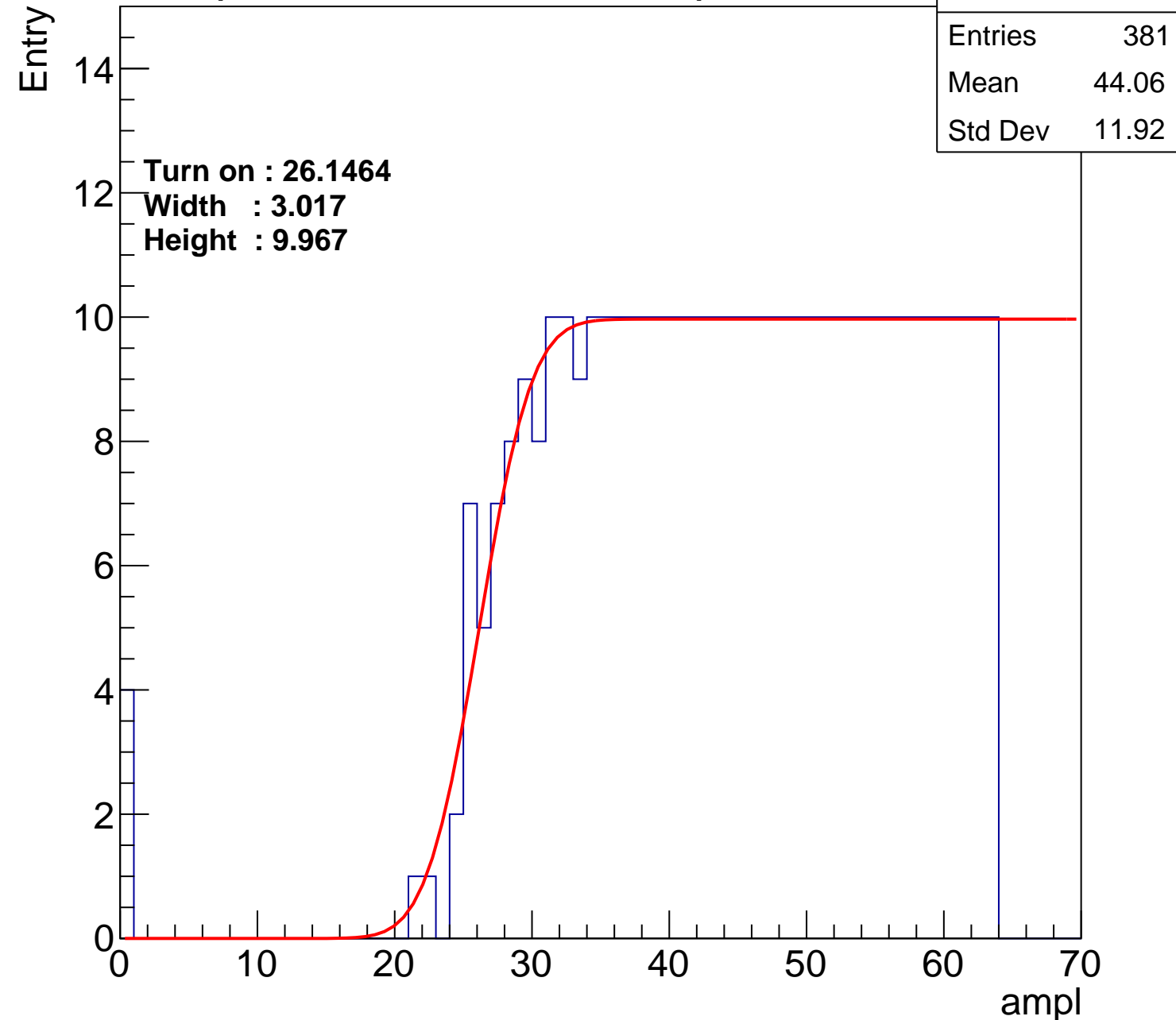
Width : 3.017

Height : 9.967

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch42

calib_packv5_042523_0143.root, FC#0, port D2

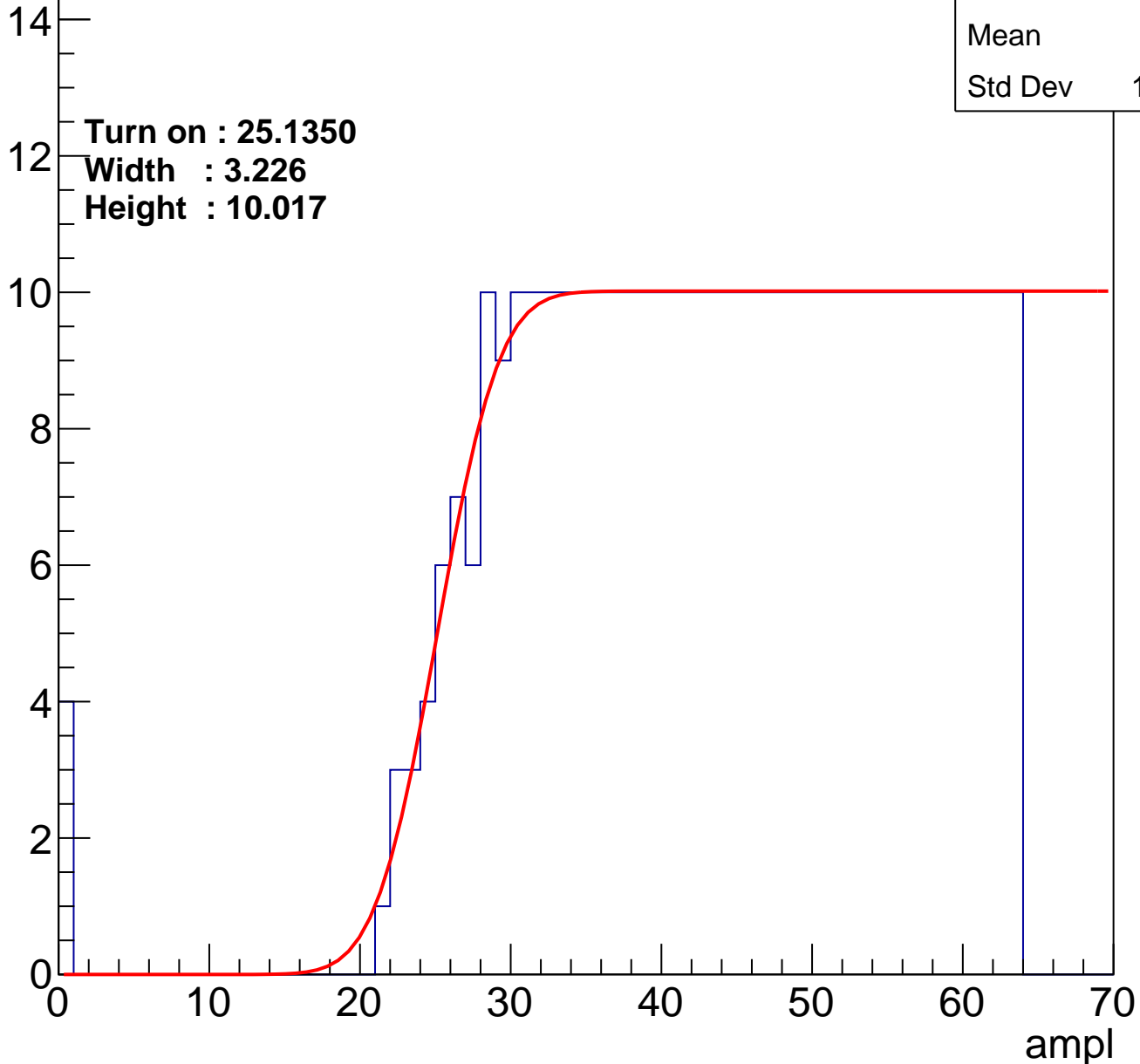
Entries	393
Mean	43.5
Std Dev	12.16

Turn on : 25.1350

Width : 3.226

Height : 10.017

Entry



B1L101S, U3-ch43

calib_packv5_042523_0143.root, FC#0, port D2

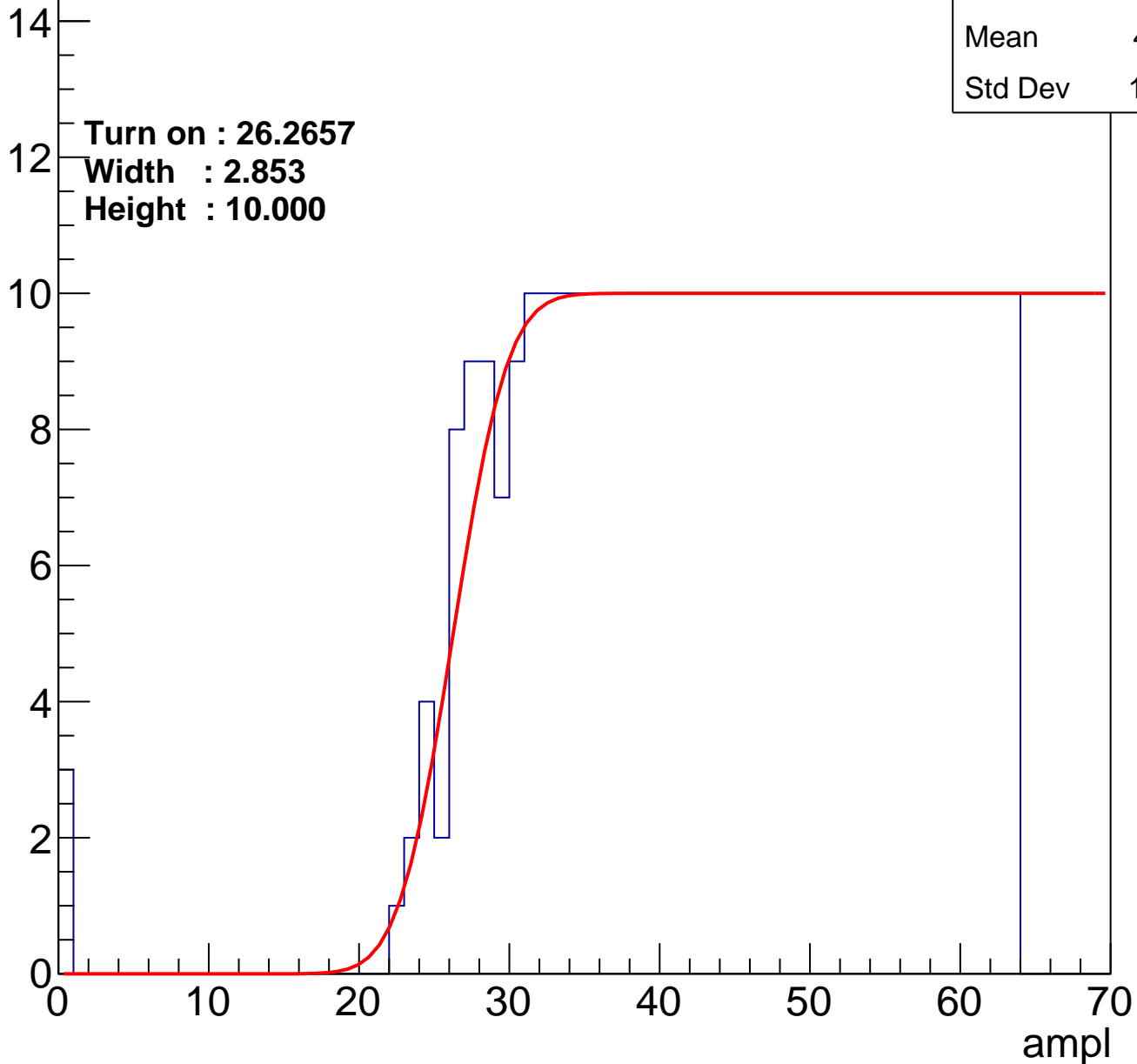
Entries	384
Mean	44.01
Std Dev	11.77

Turn on : 26.2657

Width : 2.853

Height : 10.000

Entry



B1L101S, U3-ch44

calib_packv5_042523_0143.root, FC#0, port D2

Entries	389
Mean	43.56
Std Dev	12.41

Turn on : 26.0953

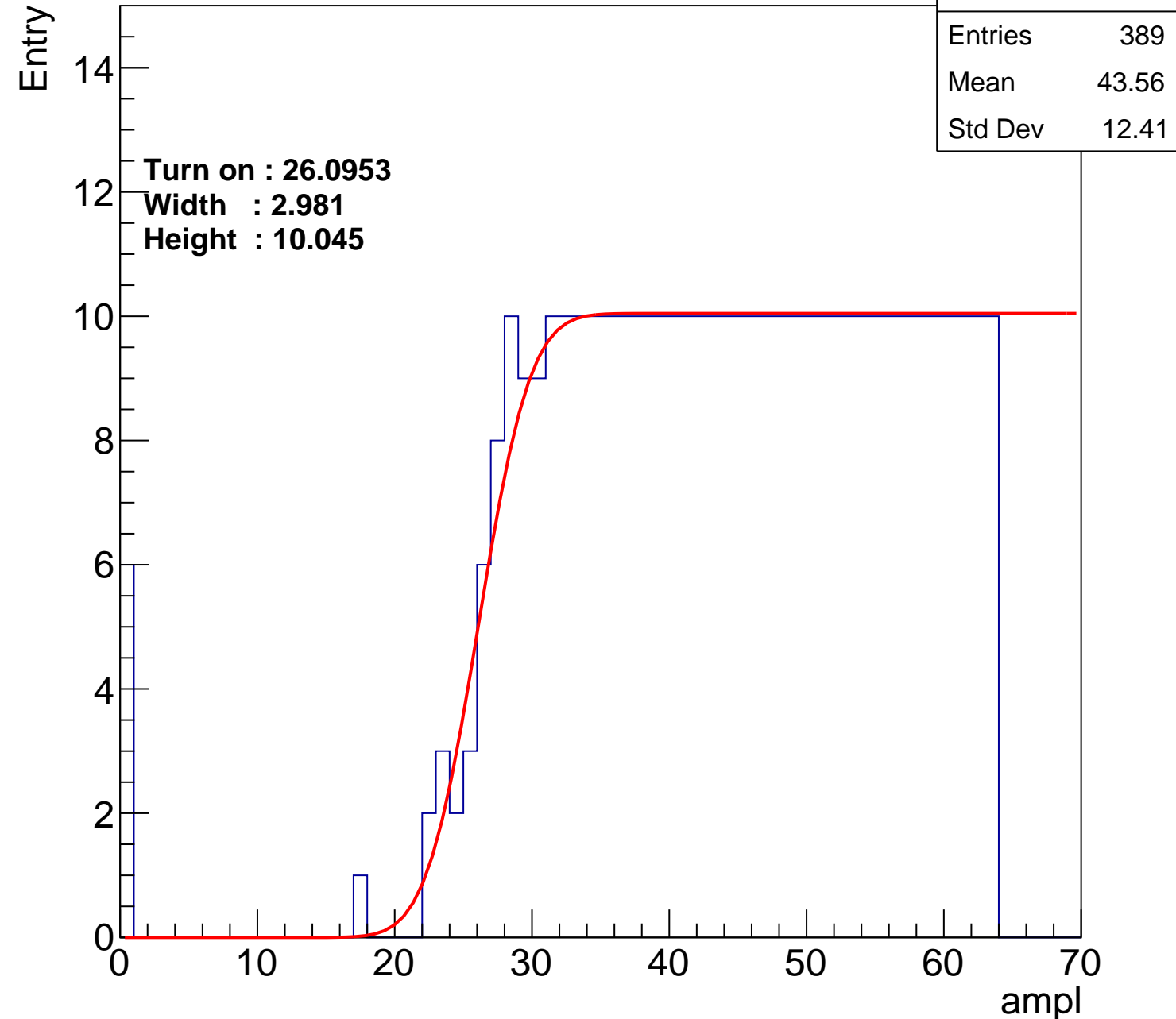
Width : 2.981

Height : 10.045

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch45

calib_packv5_042523_0143.root, FC#0, port D2

Entries	380
Mean	44.17
Std Dev	11.75

Turn on : 27.1714

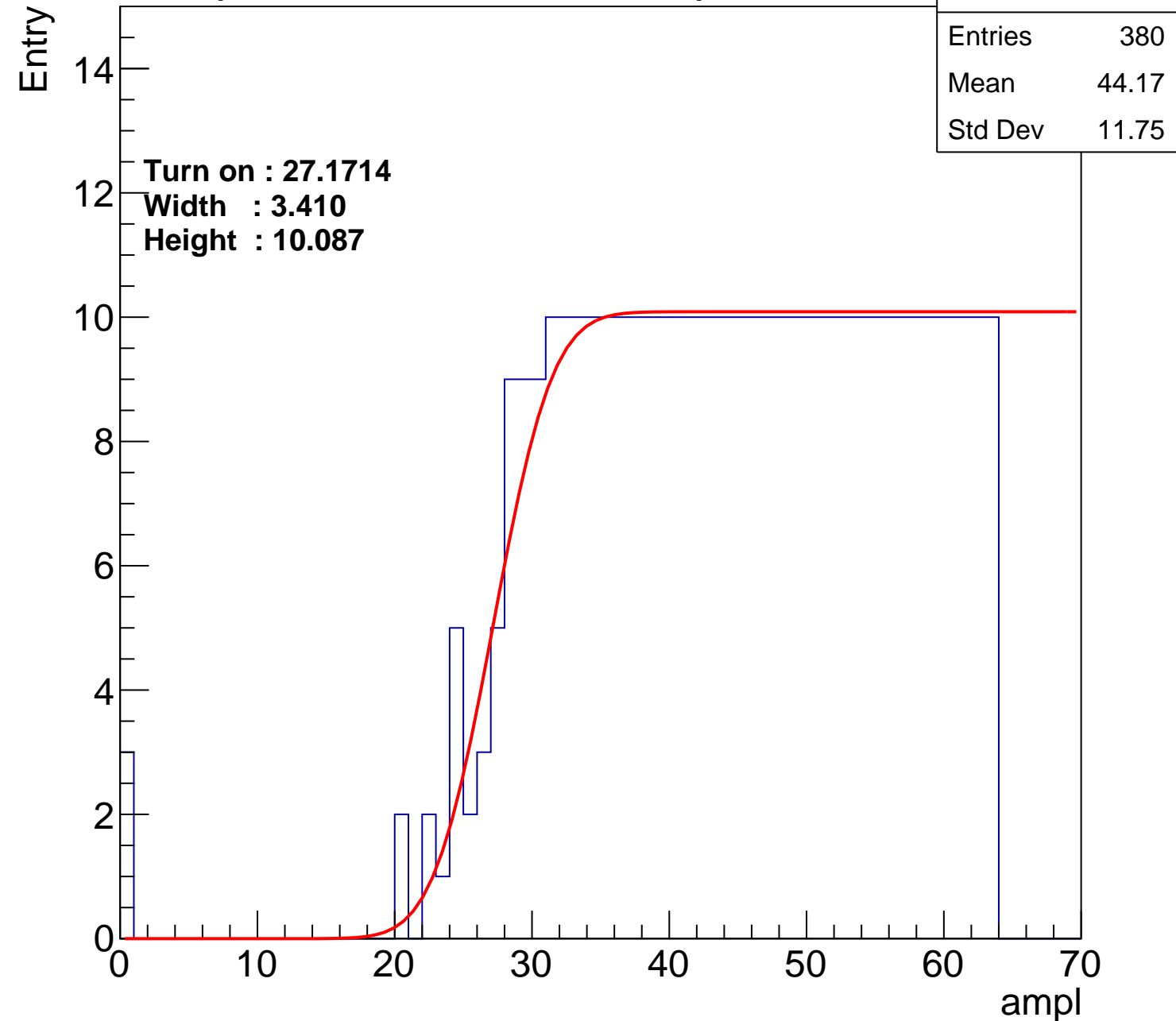
Width : 3.410

Height : 10.087

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch46

calib_packv5_042523_0143.root, FC#0, port D2

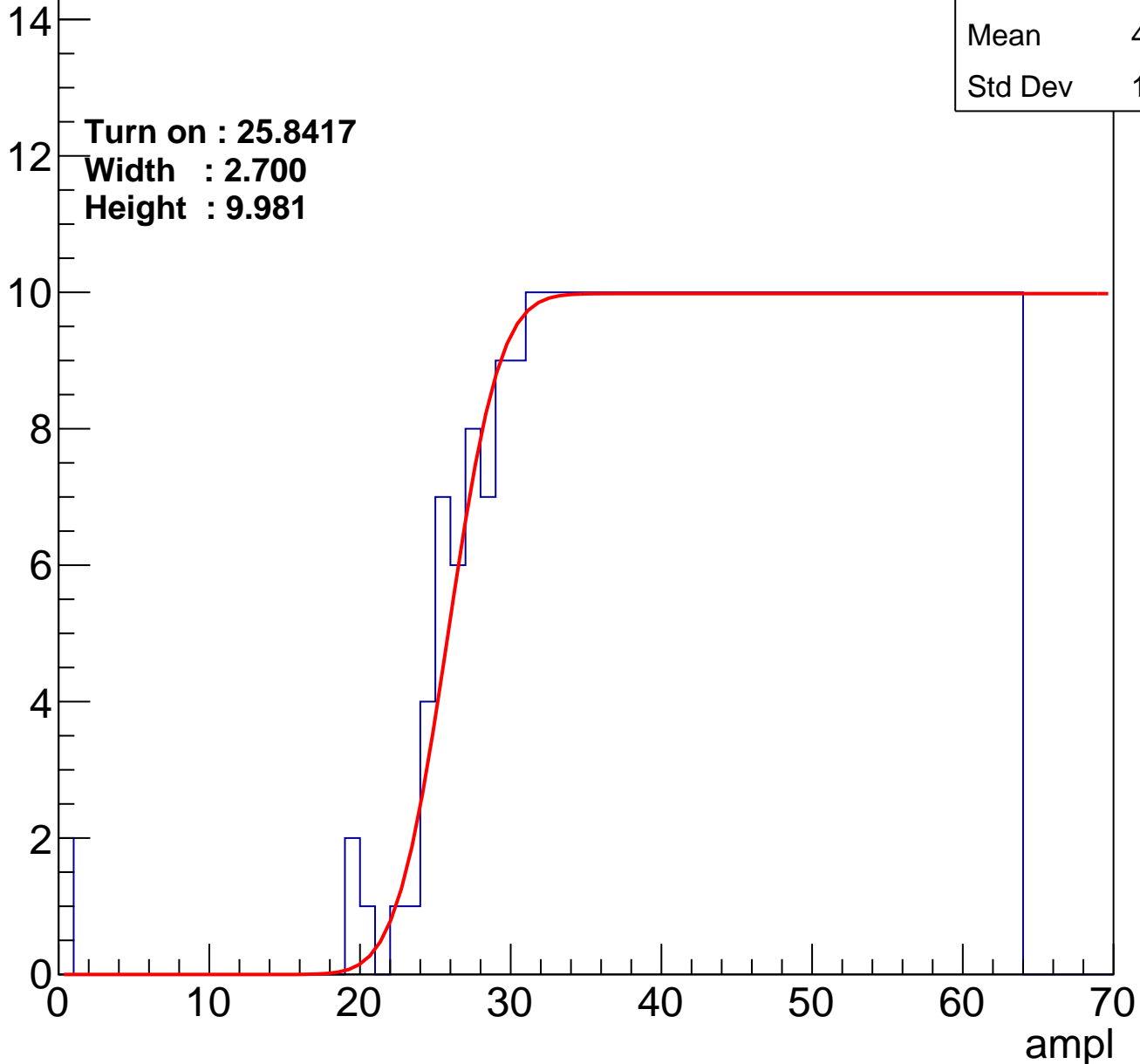
Entries	387
Mean	43.88
Std Dev	11.75

Turn on : 25.8417

Width : 2.700

Height : 9.981

Entry



B1L101S, U3-ch47

calib_packv5_042523_0143.root, FC#0, port D2

Entries	378
Mean	44.29
Std Dev	11.65

Turn on : 26.3787

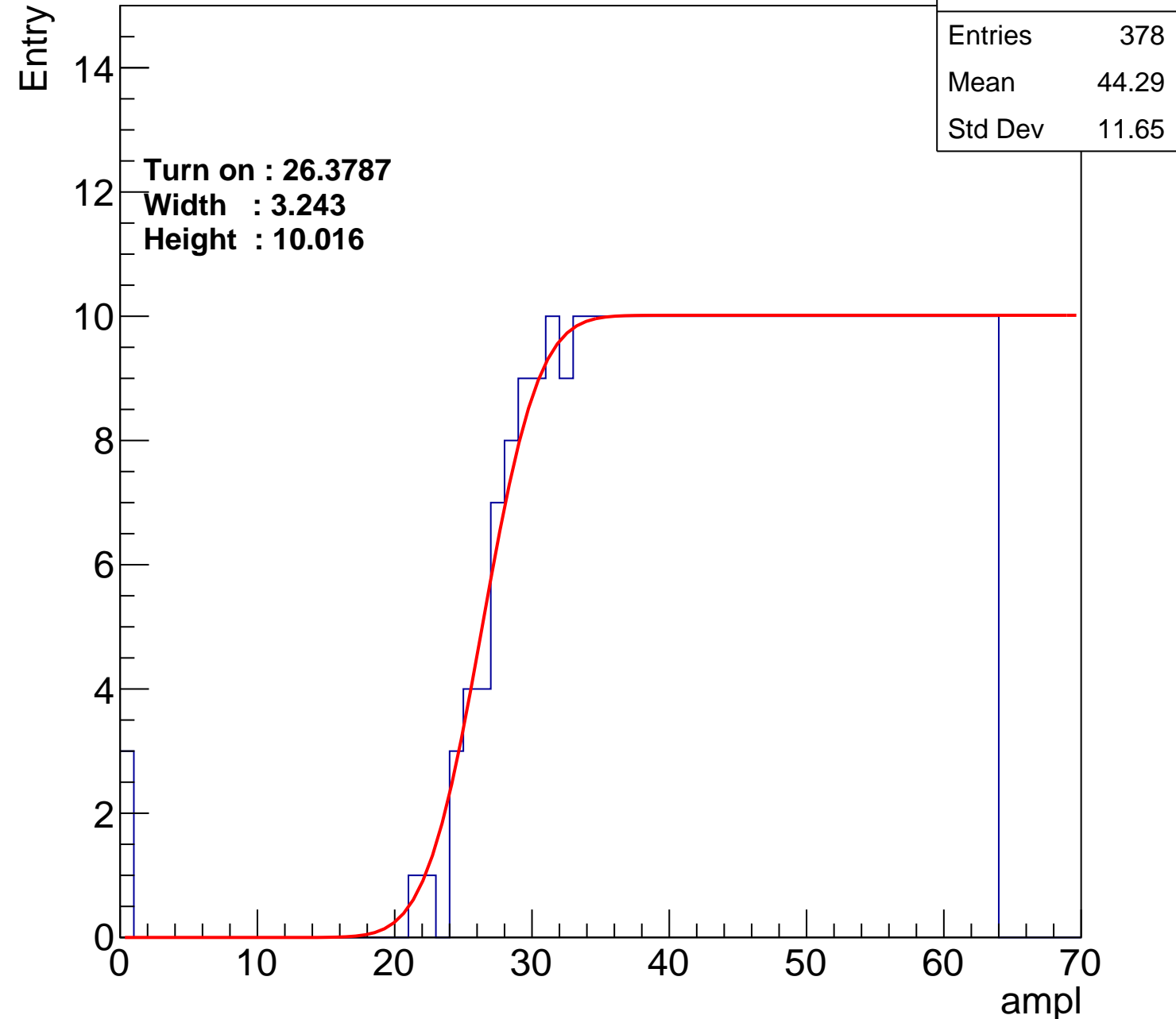
Width : 3.243

Height : 10.016

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch48

calib_packv5_042523_0143.root, FC#0, port D2

Entries	377
Mean	44.33
Std Dev	11.65

Turn on : 27.2006

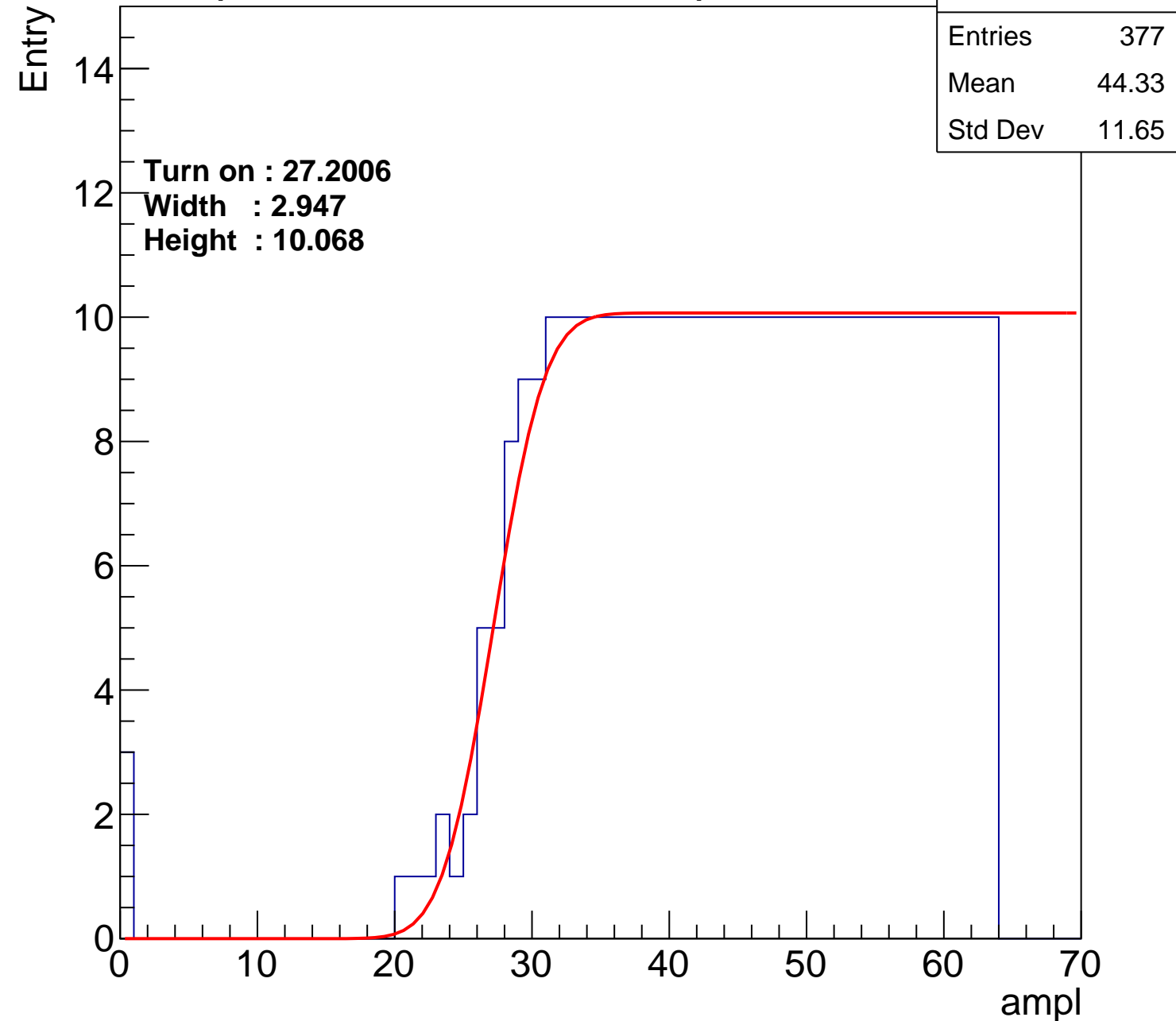
Width : 2.947

Height : 10.068

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch49

calib_packv5_042523_0143.root, FC#0, port D2

Entries	369
Mean	44.79
Std Dev	11.26

Turn on : 28.3426

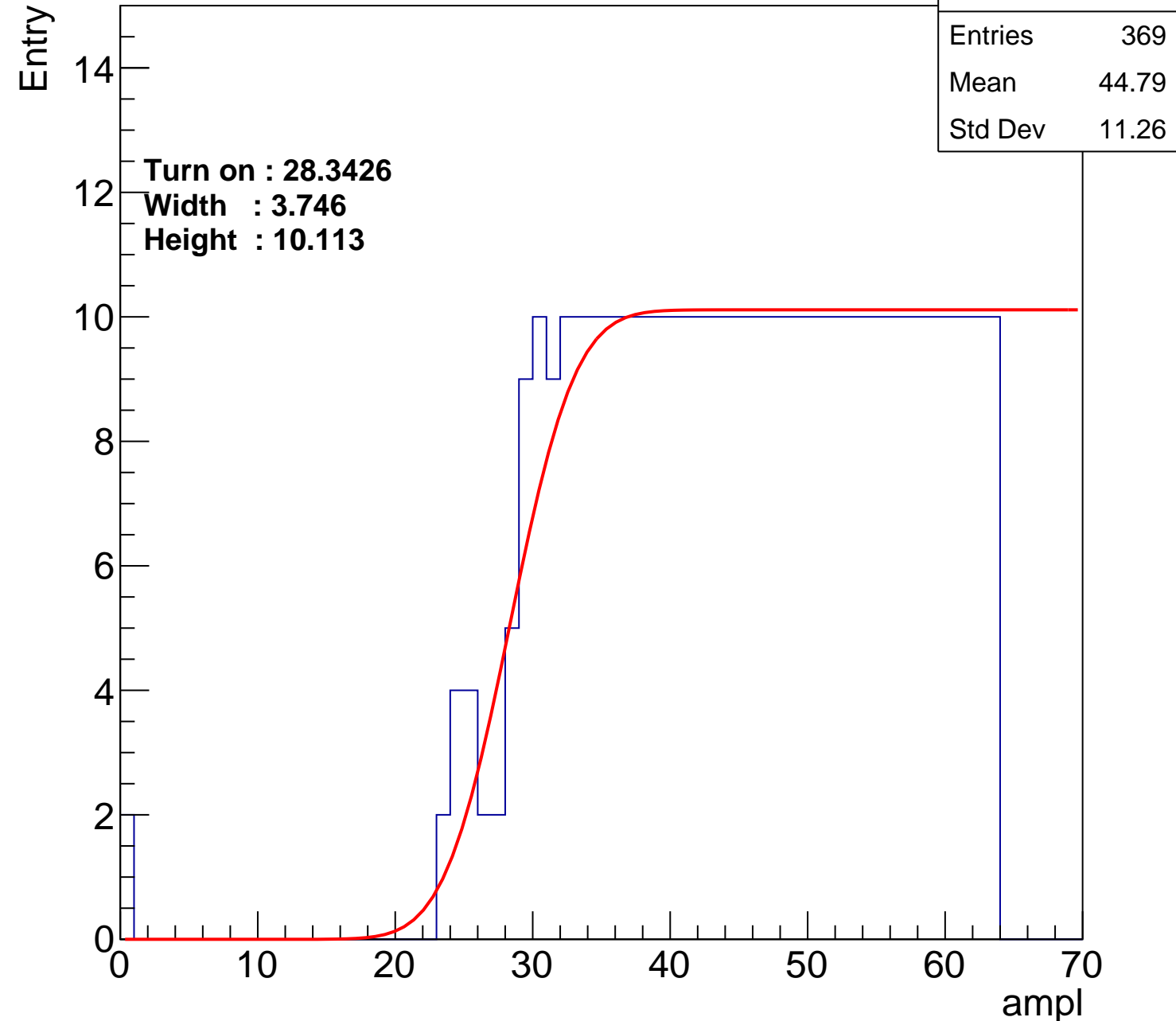
Width : 3.746

Height : 10.113

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch50

calib_packv5_042523_0143.root, FC#0, port D2

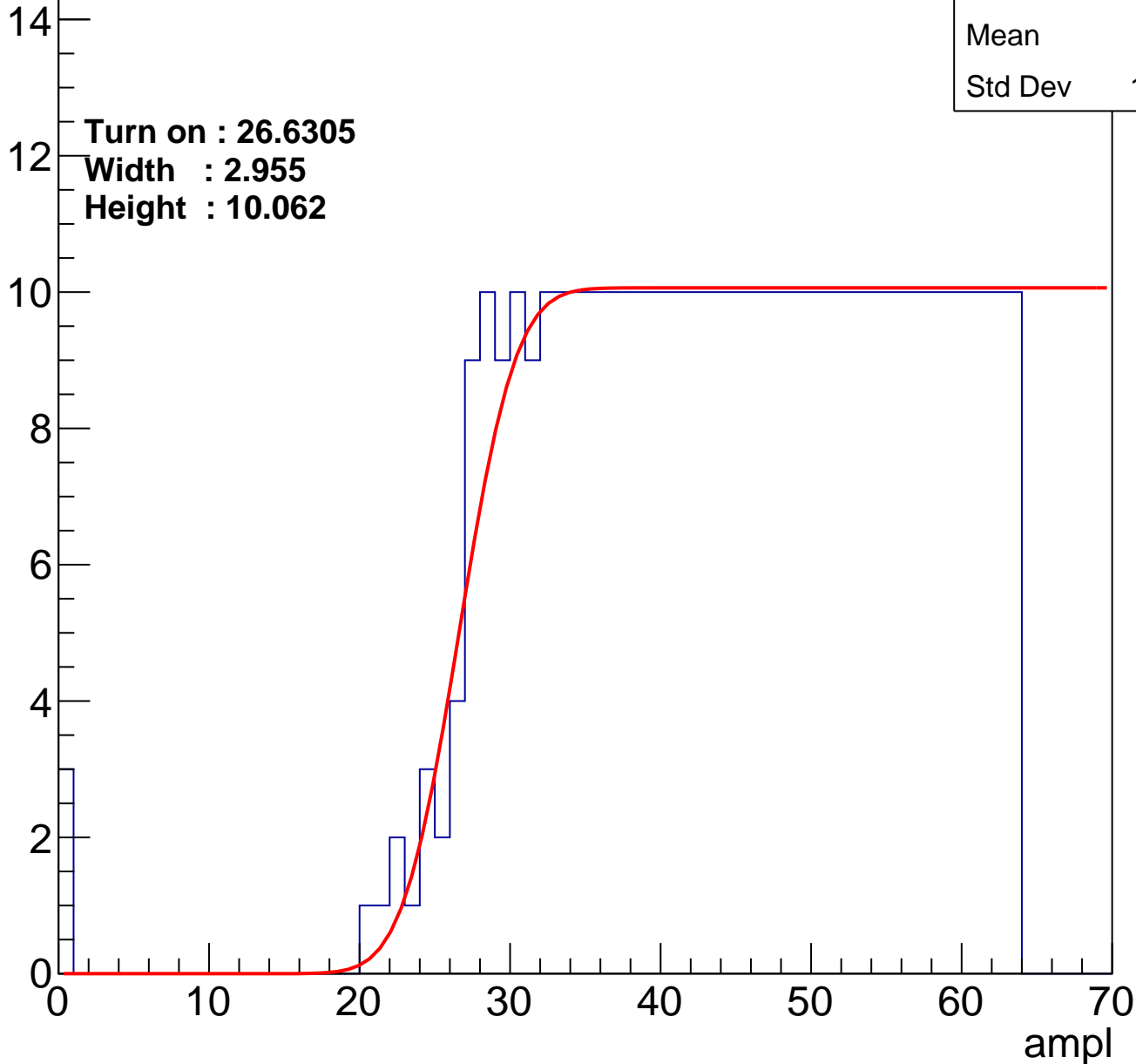
Entries	384
Mean	44
Std Dev	11.79

Turn on : 26.6305

Width : 2.955

Height : 10.062

Entry



B1L101S, U3-ch51

calib_packv5_042523_0143.root, FC#0, port D2

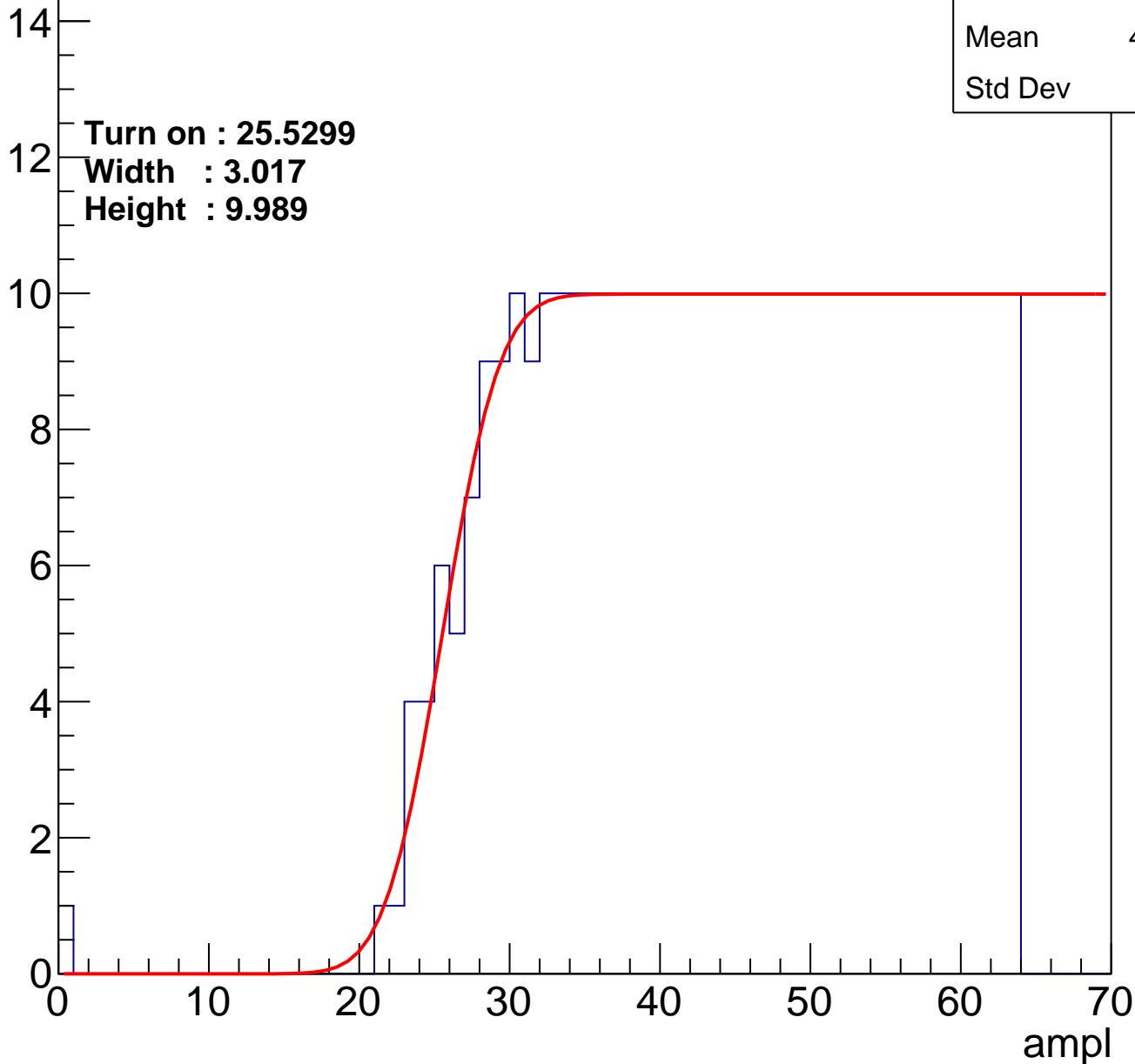
Entries	386
Mean	44.02
Std Dev	11.51

Turn on : 25.5299

Width : 3.017

Height : 9.989

Entry



B1L101S, U3-ch52

calib_packv5_042523_0143.root, FC#0, port D2

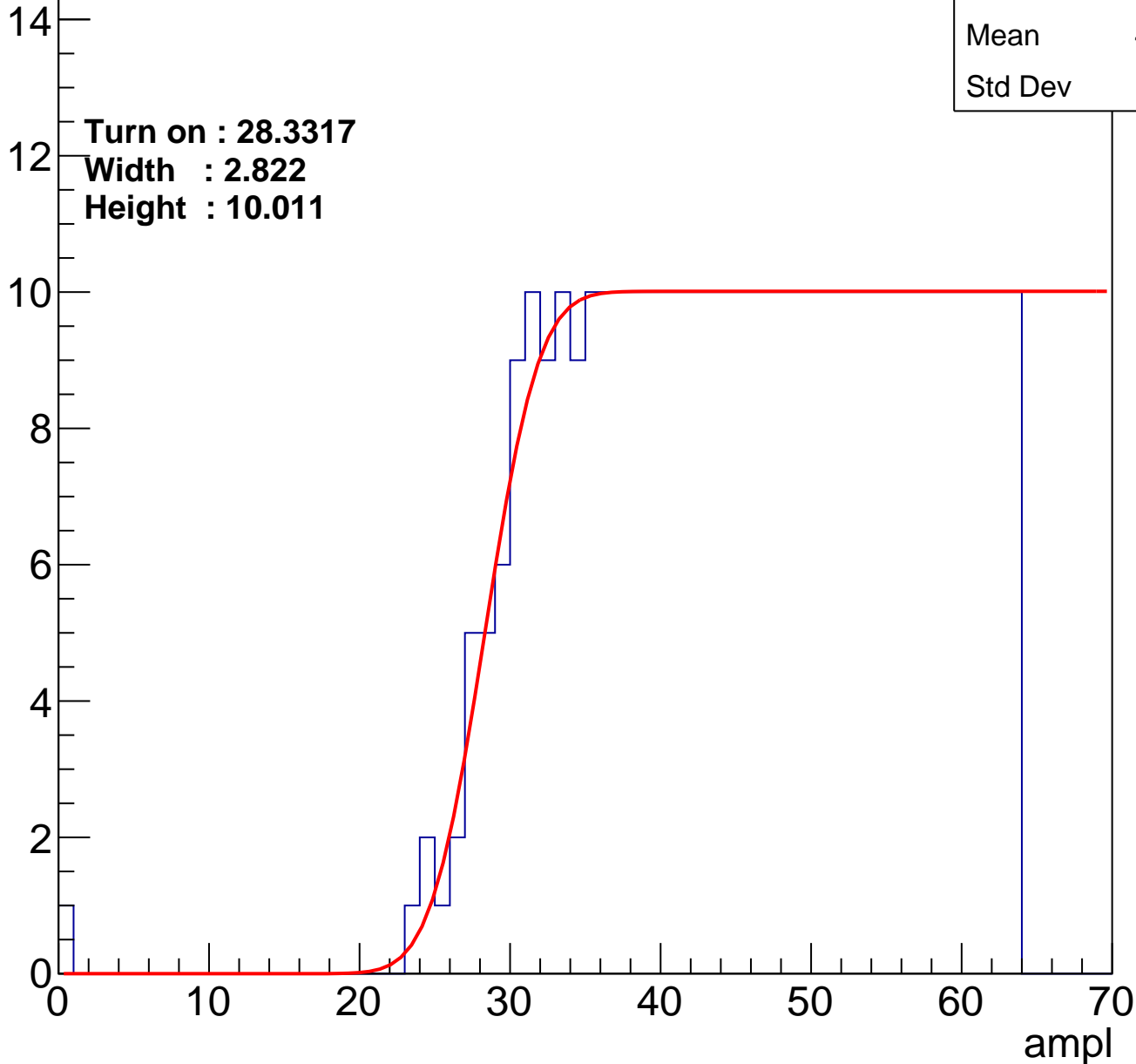
Entries	360
Mean	45.31
Std Dev	10.81

Turn on : 28.3317

Width : 2.822

Height : 10.011

Entry



B1L101S, U3-ch53

calib_packv5_042523_0143.root, FC#0, port D2

Entries	387
Mean	43.72
Std Dev	12.14

Turn on : 25.8924

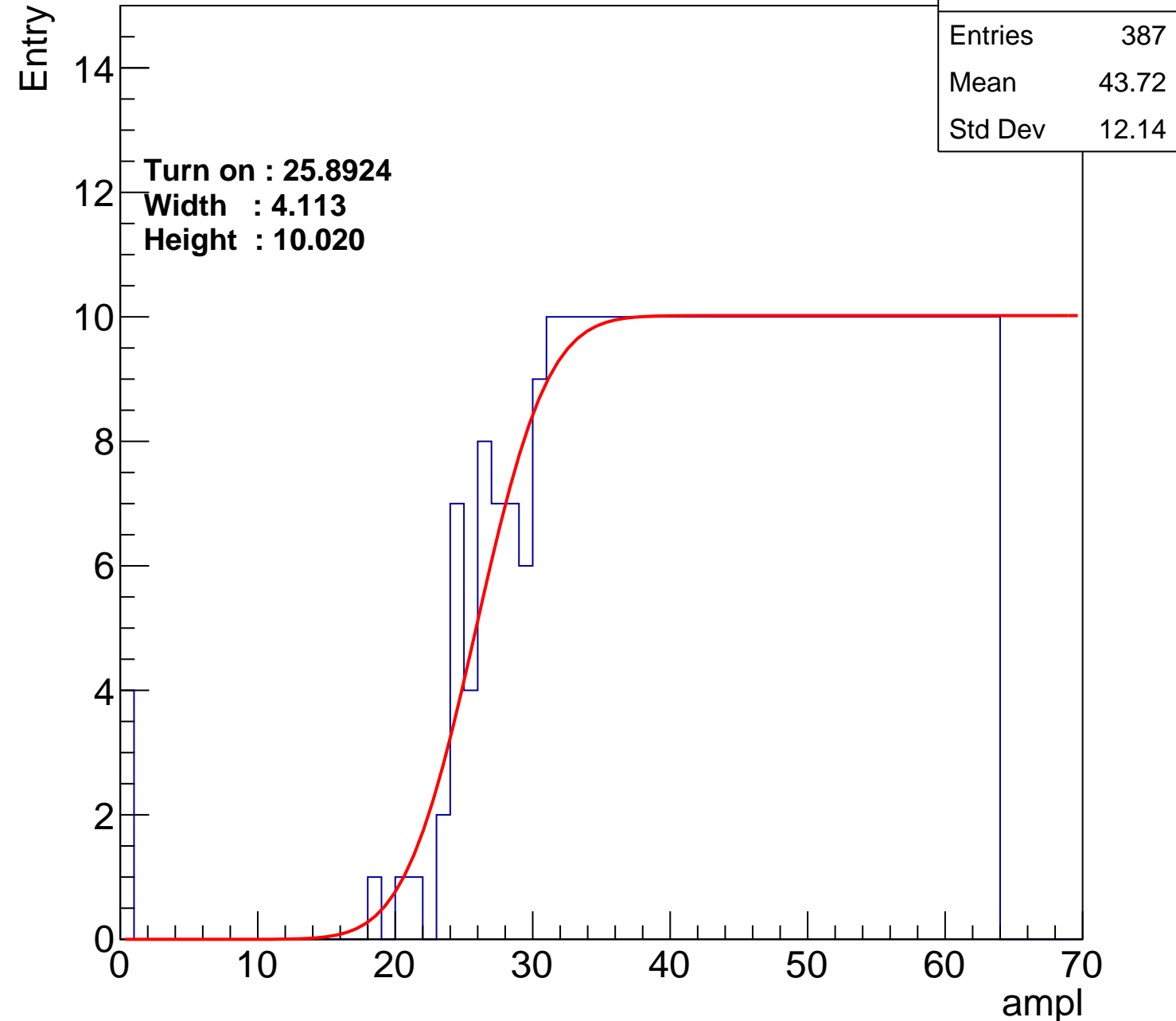
Width : 4.113

Height : 10.020

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch54

calib_packv5_042523_0143.root, FC#0, port D2

Entries	387
Mean	43.66
Std Dev	12.36

Turn on : 25.7066

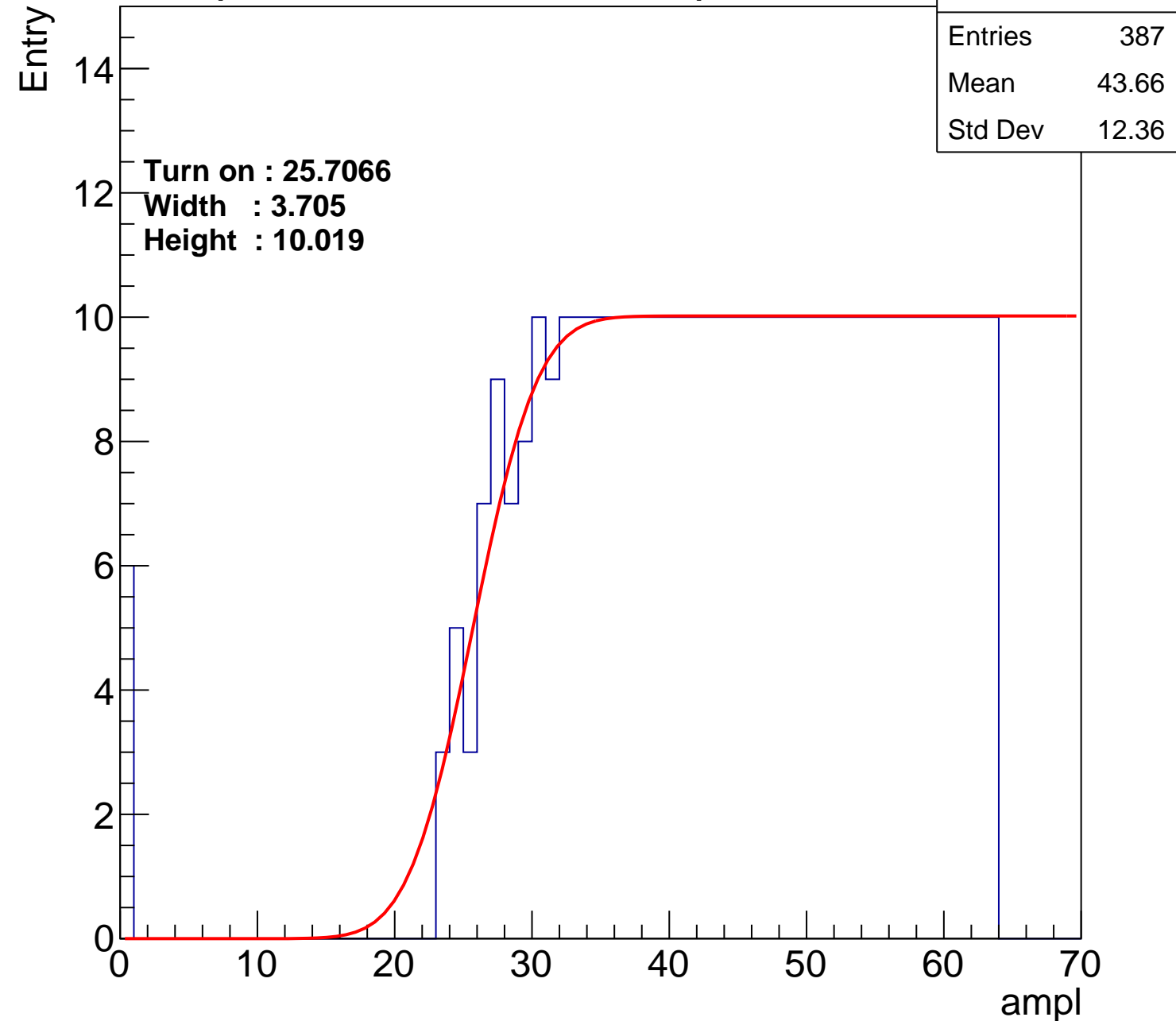
Width : 3.705

Height : 10.019

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch55

calib_packv5_042523_0143.root, FC#0, port D2

Entries	381
Mean	44.23
Std Dev	11.51

Turn on : 26.1030

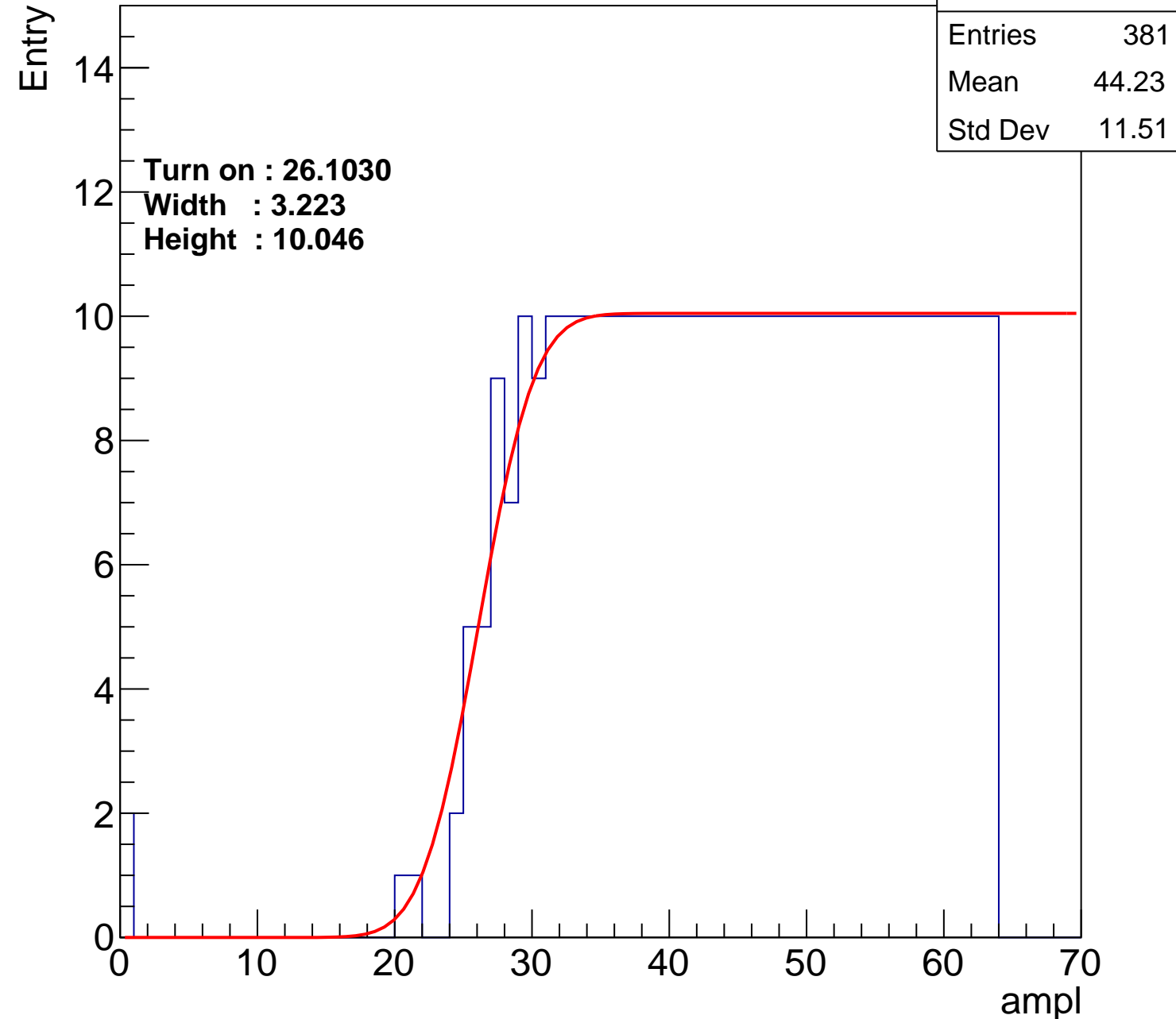
Width : 3.223

Height : 10.046

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch56

calib_packv5_042523_0143.root, FC#0, port D2

Entries	382
Mean	43.97
Std Dev	12.03

Turn on : 26.5776

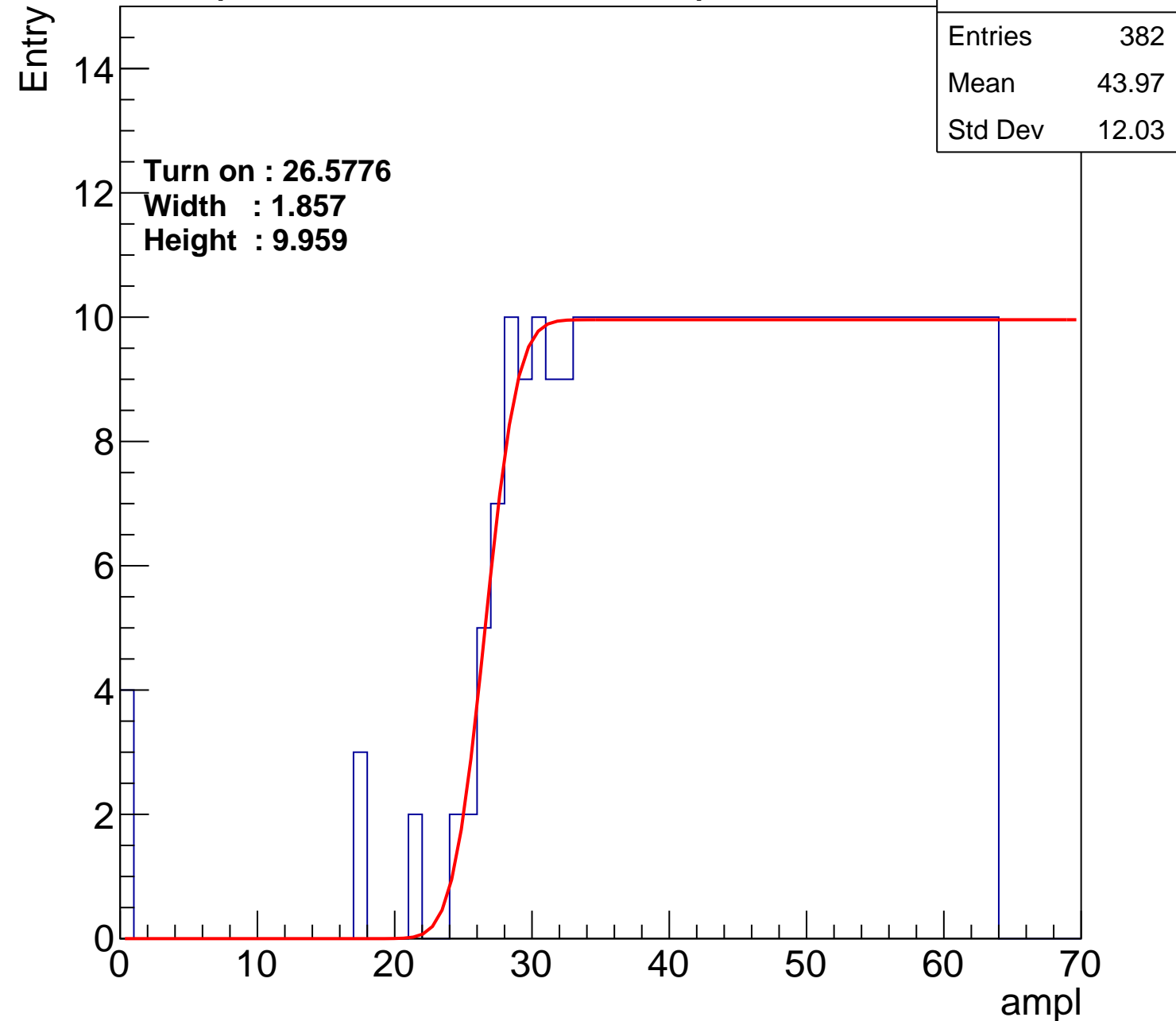
Width : 1.857

Height : 9.959

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch57

calib_packv5_042523_0143.root, FC#0, port D2

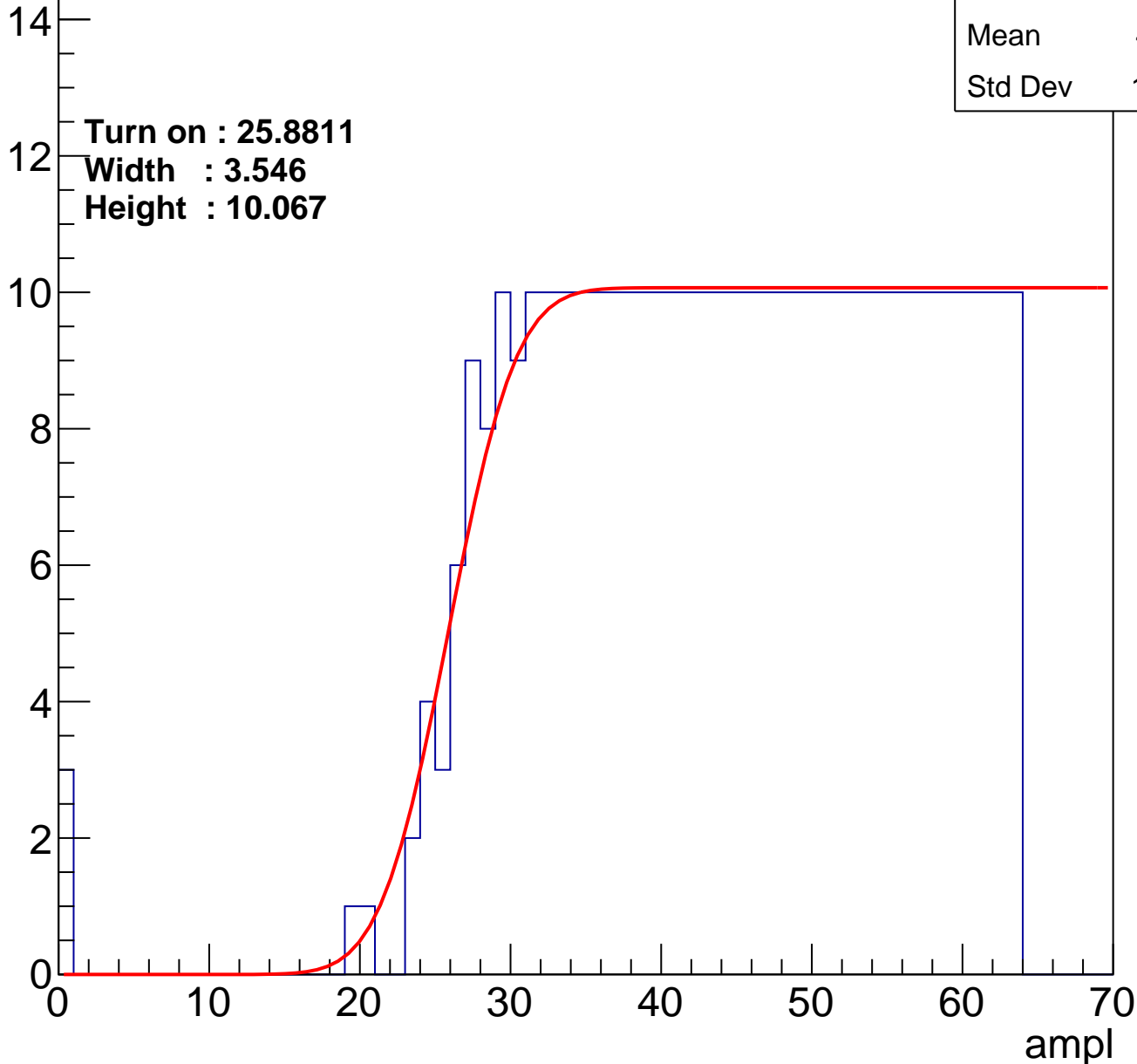
Entries	386
Mean	43.91
Std Dev	11.84

Turn on : 25.8811

Width : 3.546

Height : 10.067

Entry



B1L101S, U3-ch58

calib_packv5_042523_0143.root, FC#0, port D2

Entries	392
Mean	43.64
Std Dev	11.95

Turn on : 25.6260

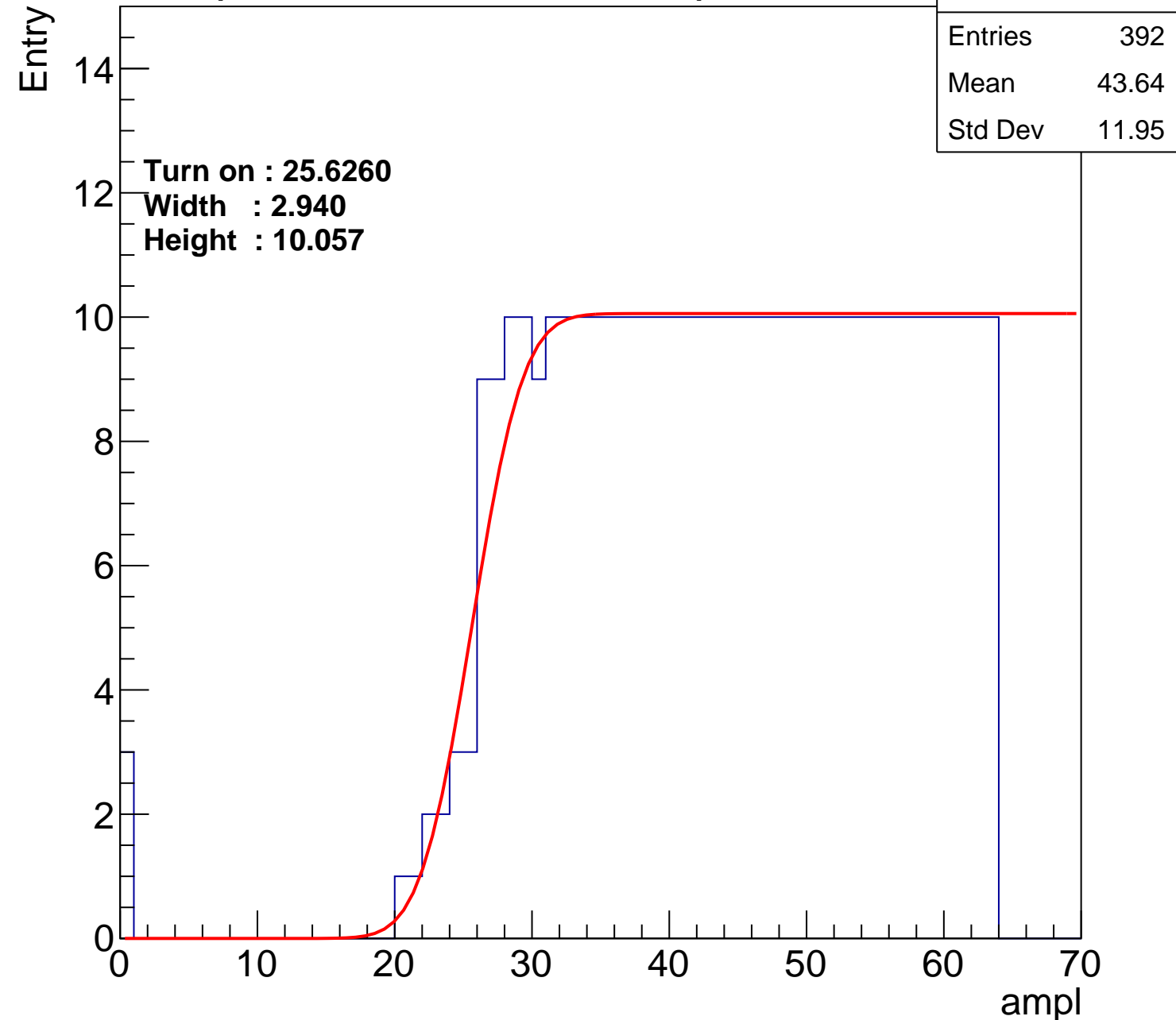
Width : 2.940

Height : 10.057

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch59

calib_packv5_042523_0143.root, FC#0, port D2

Entries	377
Mean	44.4
Std Dev	11.46

Turn on : 26.5437

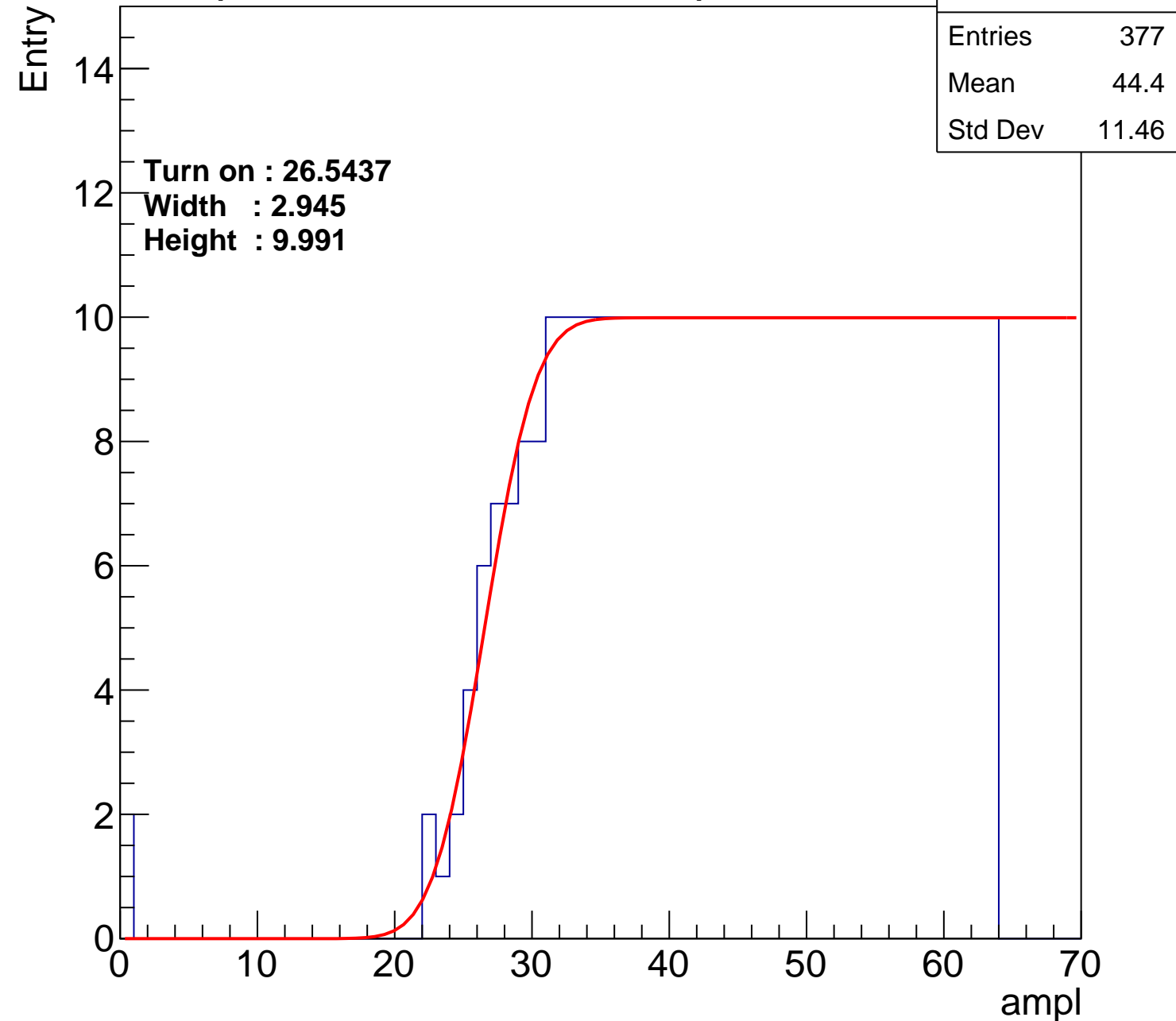
Width : 2.945

Height : 9.991

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch60

calib_packv5_042523_0143.root, FC#0, port D2

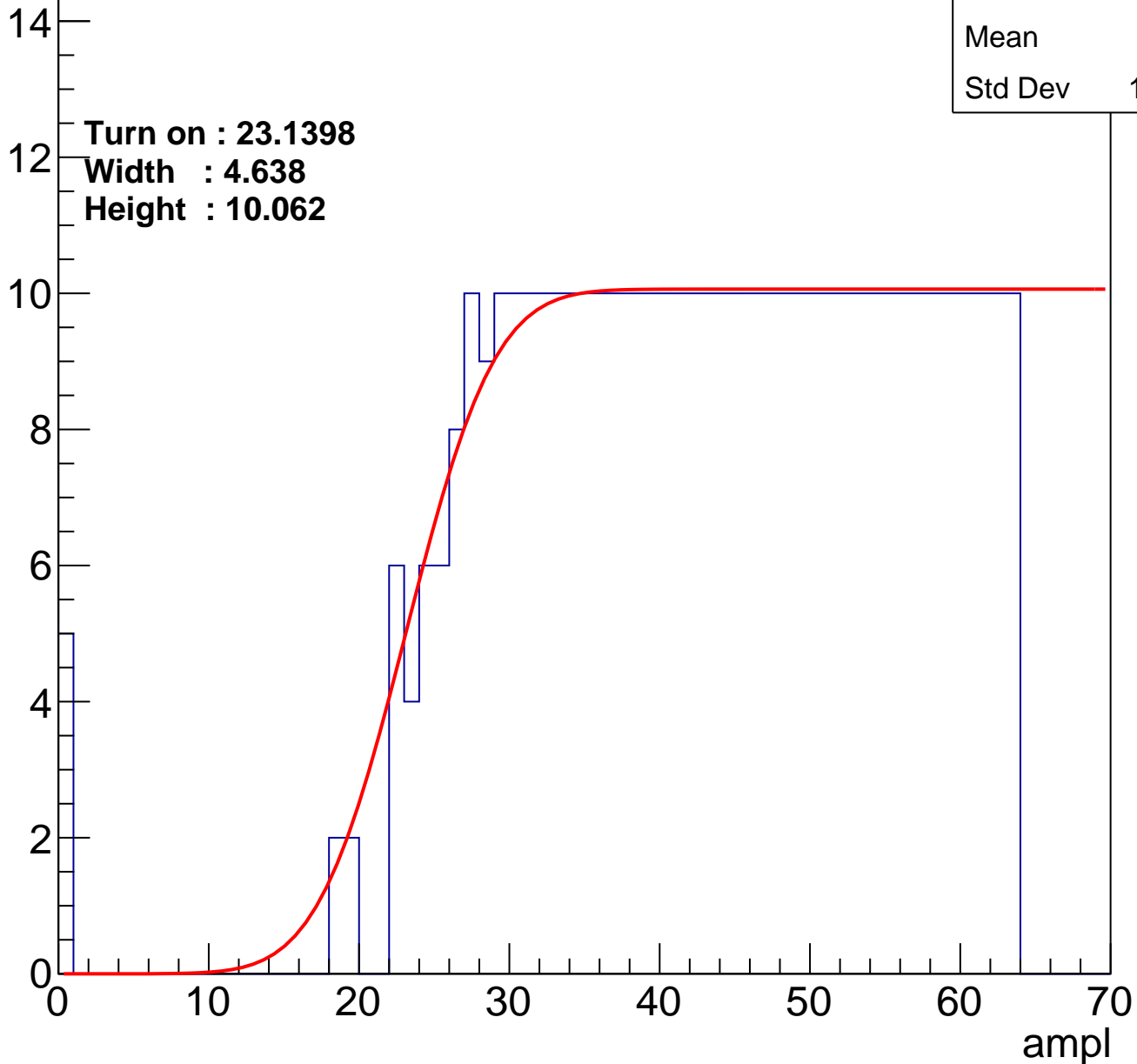
Entries	408
Mean	42.7
Std Dev	12.69

Turn on : 23.1398

Width : 4.638

Height : 10.062

Entry



B1L101S, U3-ch61

calib_packv5_042523_0143.root, FC#0, port D2

Entries	382
Mean	44.08
Std Dev	11.7

Turn on : 26.6359

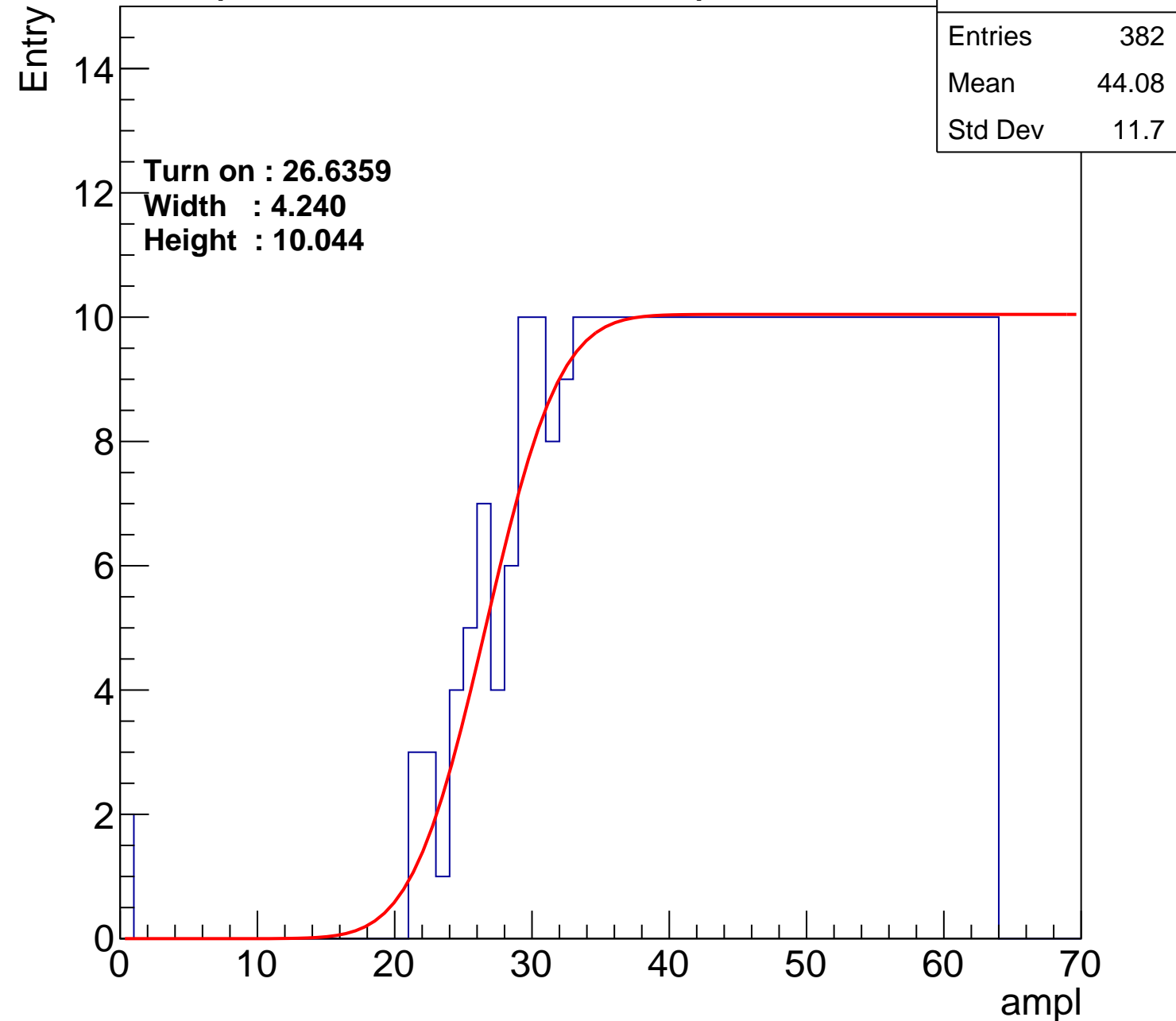
Width : 4.240

Height : 10.044

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch62

calib_packv5_042523_0143.root, FC#0, port D2

Entries	394
Mean	43.51
Std Dev	12.05

Turn on : 24.8967

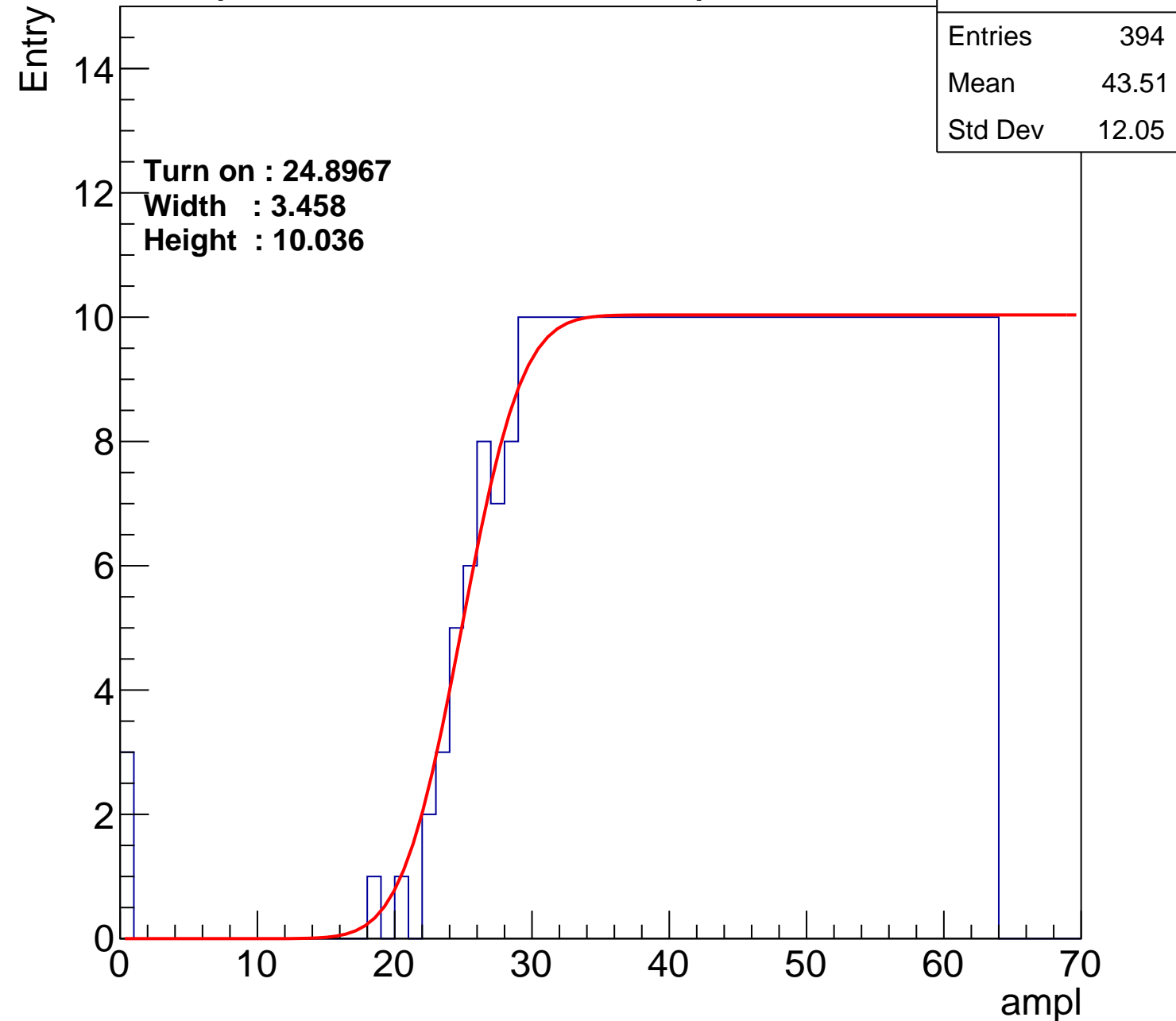
Width : 3.458

Height : 10.036

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch63

calib_packv5_042523_0143.root, FC#0, port D2

Entries	399
Mean	42.99
Std Dev	12.88

Turn on : 25.5020

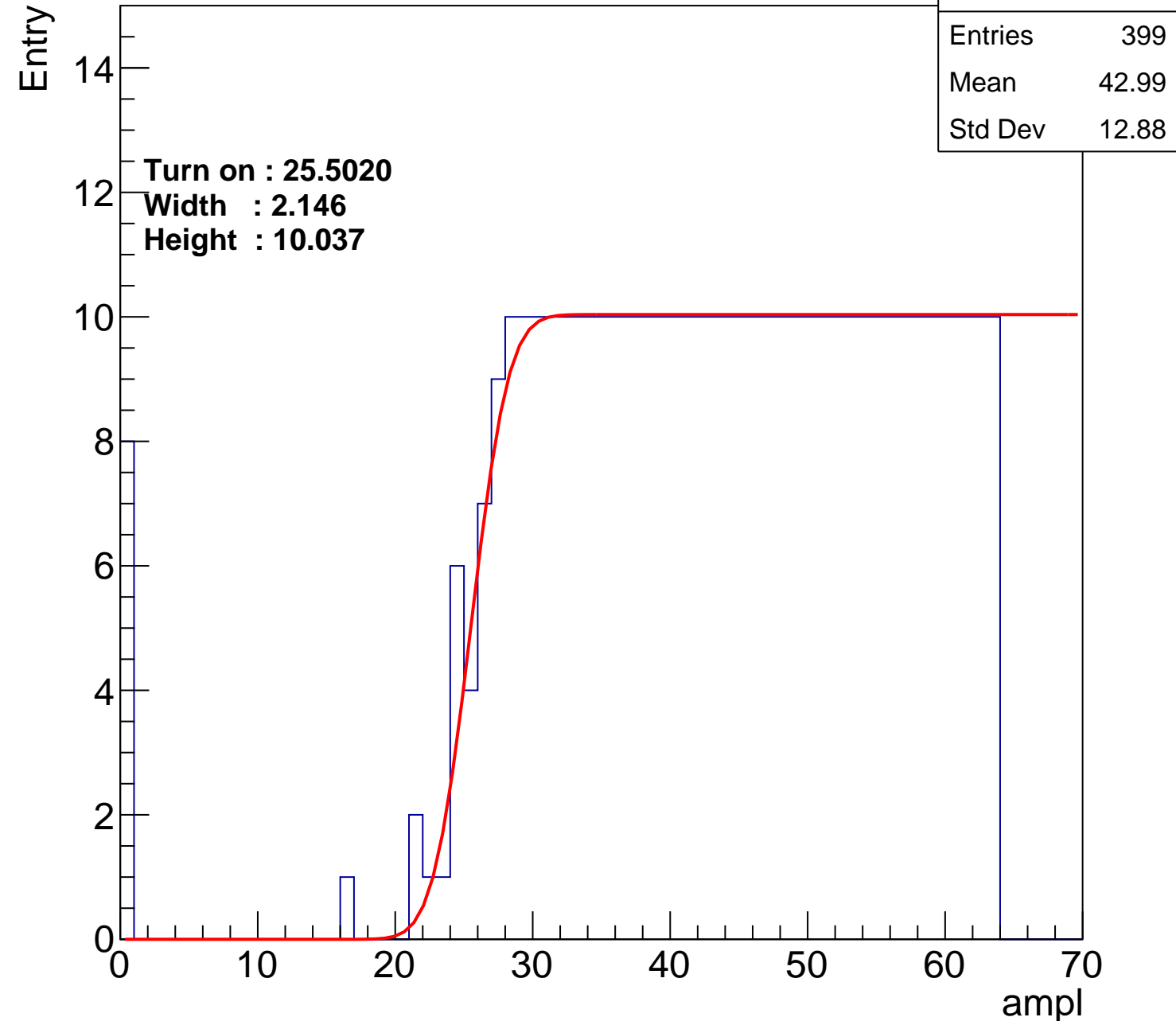
Width : 2.146

Height : 10.037

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch64

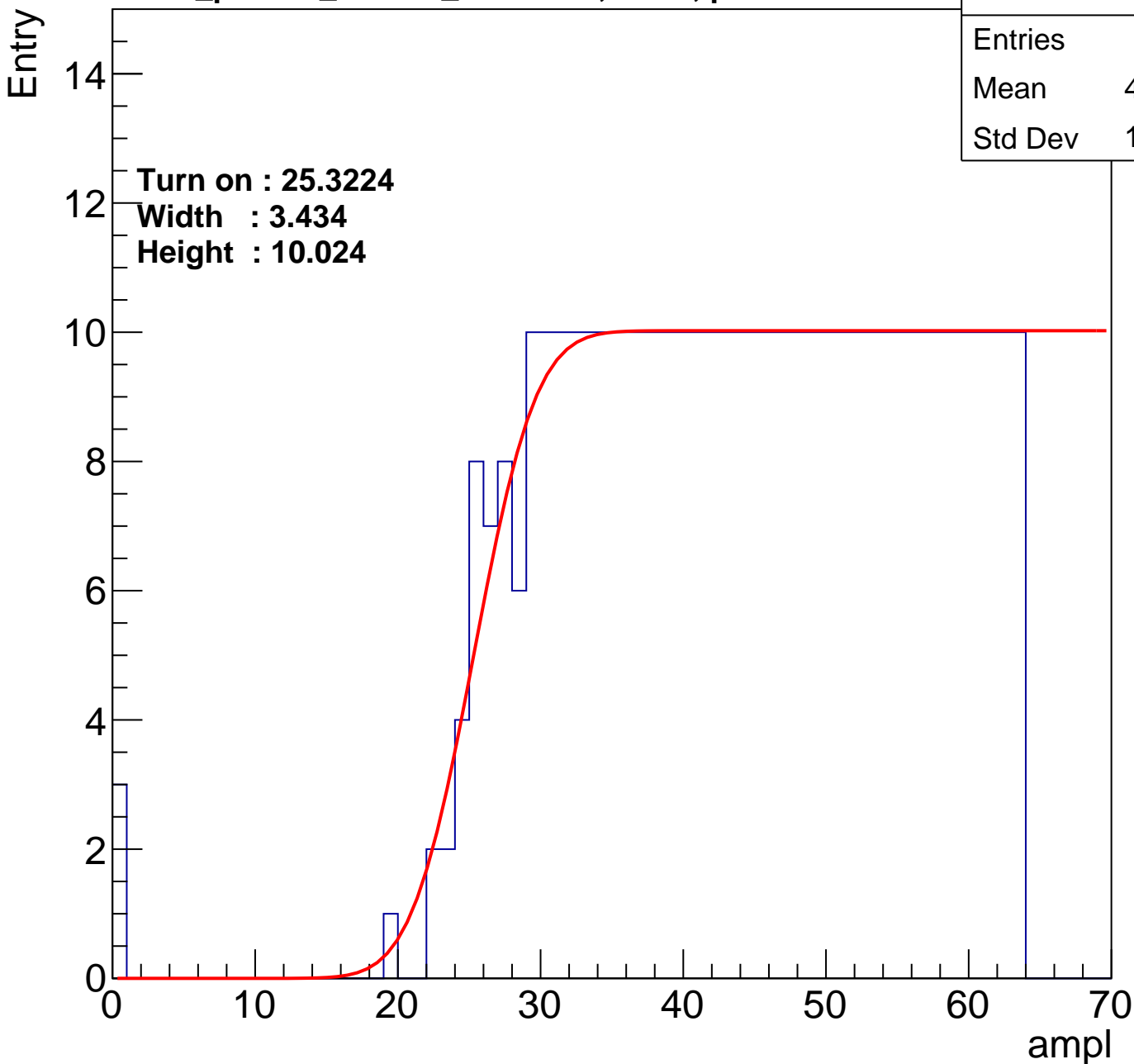
calib_packv5_042523_0143.root, FC#0, port D2

Entries	391
Mean	43.66
Std Dev	11.96

Turn on : 25.3224

Width : 3.434

Height : 10.024



B1L101S, U3-ch65

calib_packv5_042523_0143.root, FC#0, port D2

Entries	381
Mean	44.21
Std Dev	11.53

Turn on : 25.9526

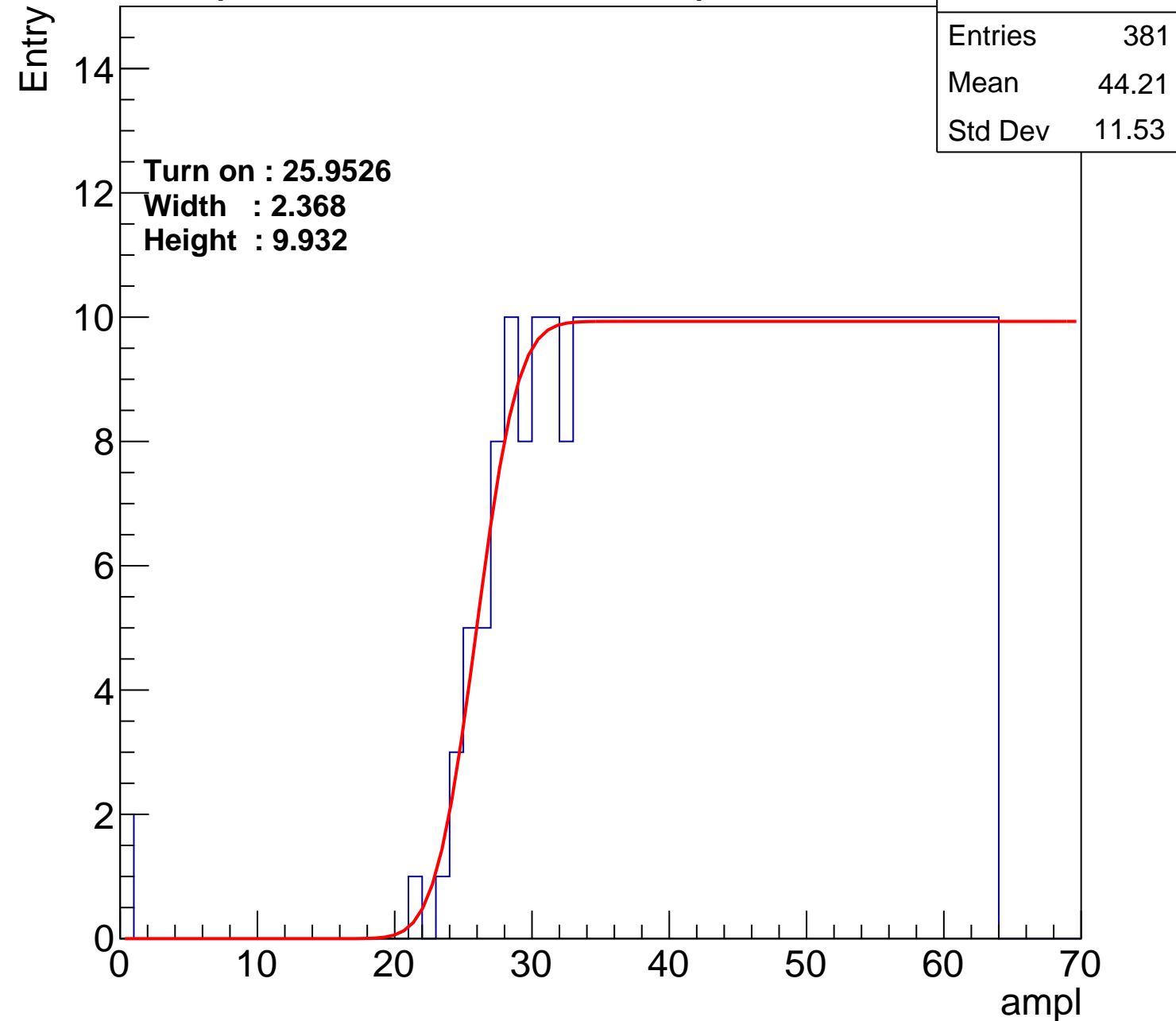
Width : 2.368

Height : 9.932

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch66

calib_packv5_042523_0143.root, FC#0, port D2

Entries	360
Mean	45.11
Std Dev	11.31

Turn on : 28.3761

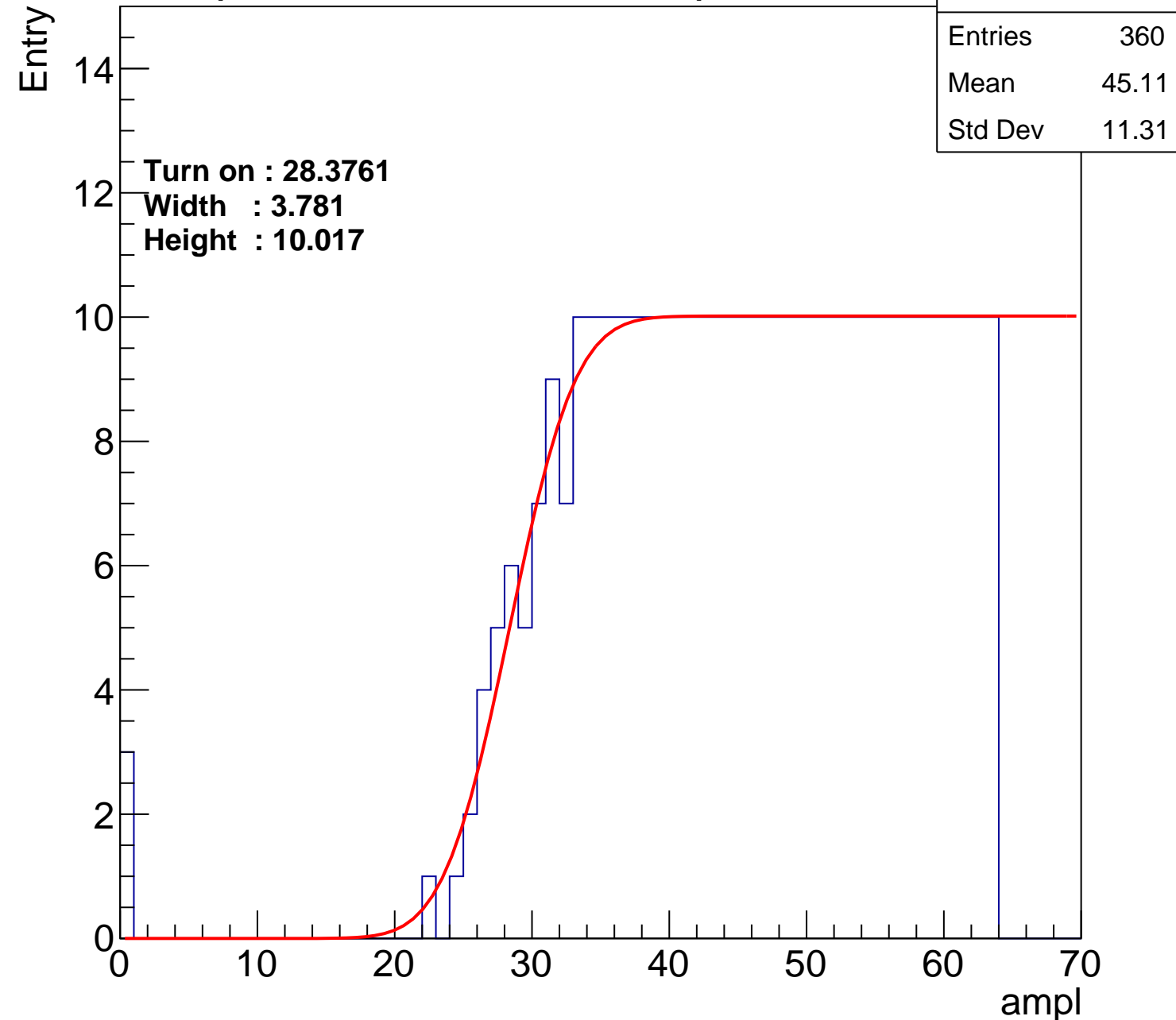
Width : 3.781

Height : 10.017

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch67

calib_packv5_042523_0143.root, FC#0, port D2

Entries	382
Mean	44.23
Std Dev	11.39

Turn on : 26.0484

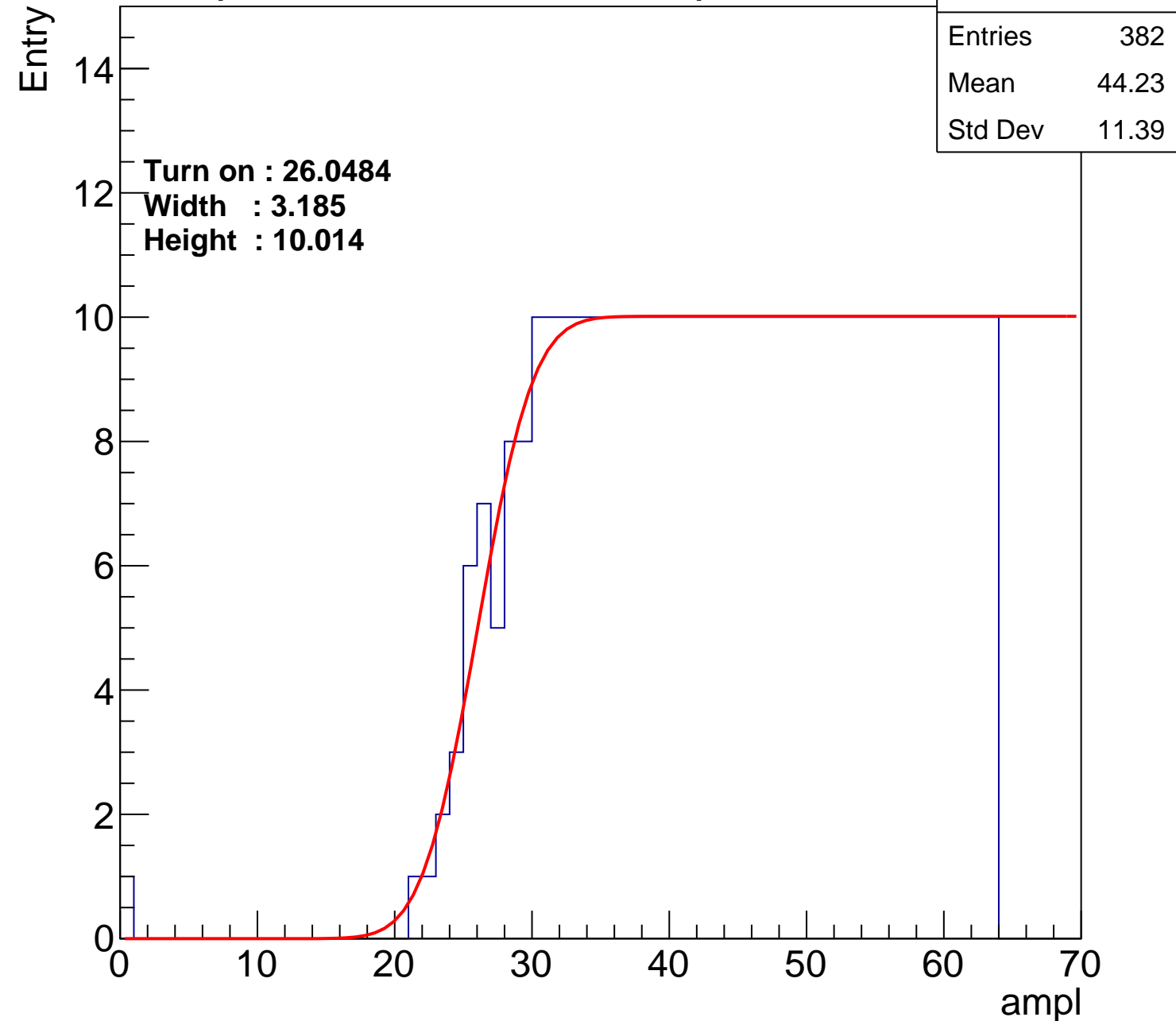
Width : 3.185

Height : 10.014

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch68

calib_packv5_042523_0143.root, FC#0, port D2

Entries	389
Mean	43.79
Std Dev	11.79

Turn on : 25.9534

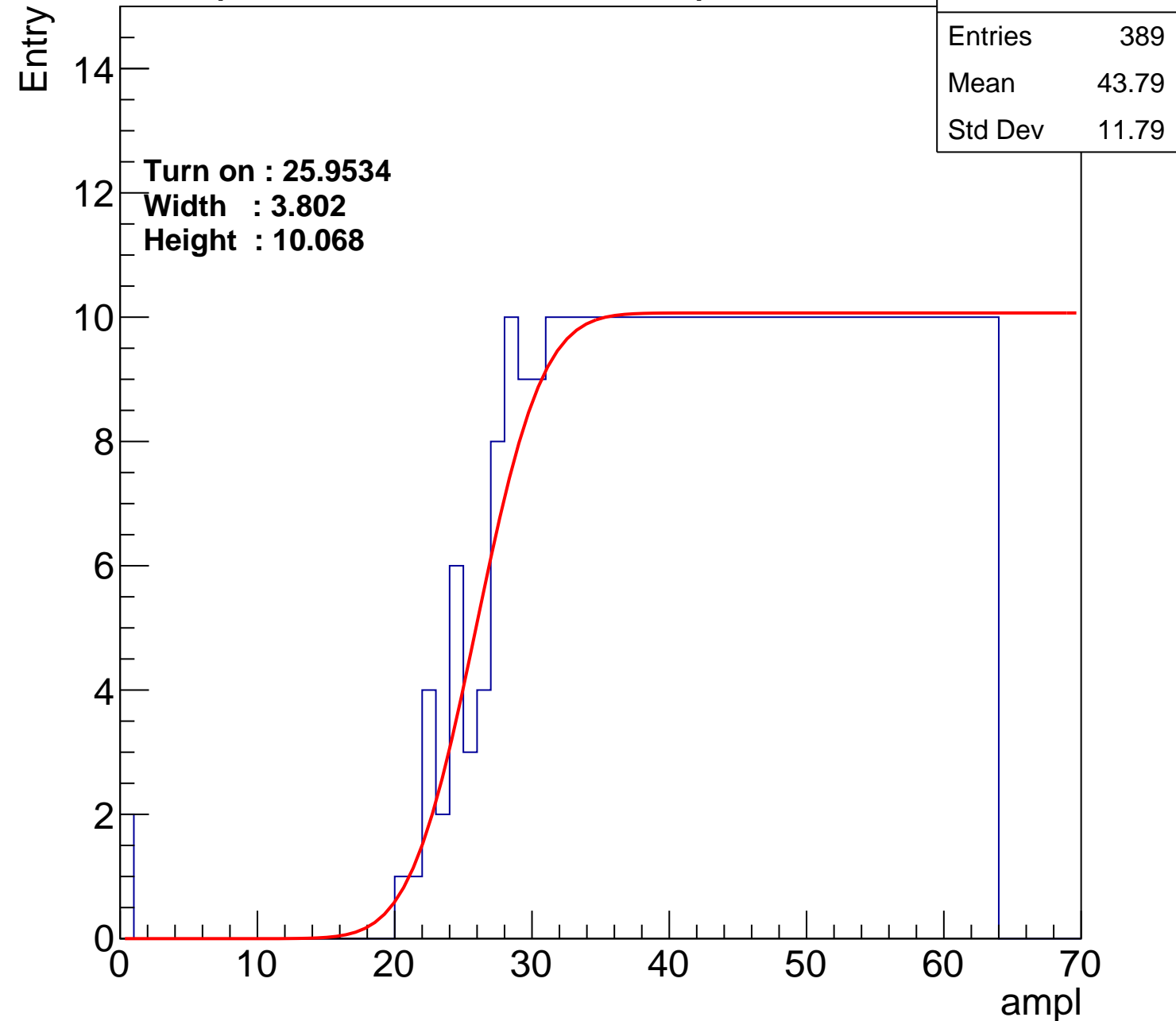
Width : 3.802

Height : 10.068

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch69

calib_packv5_042523_0143.root, FC#0, port D2

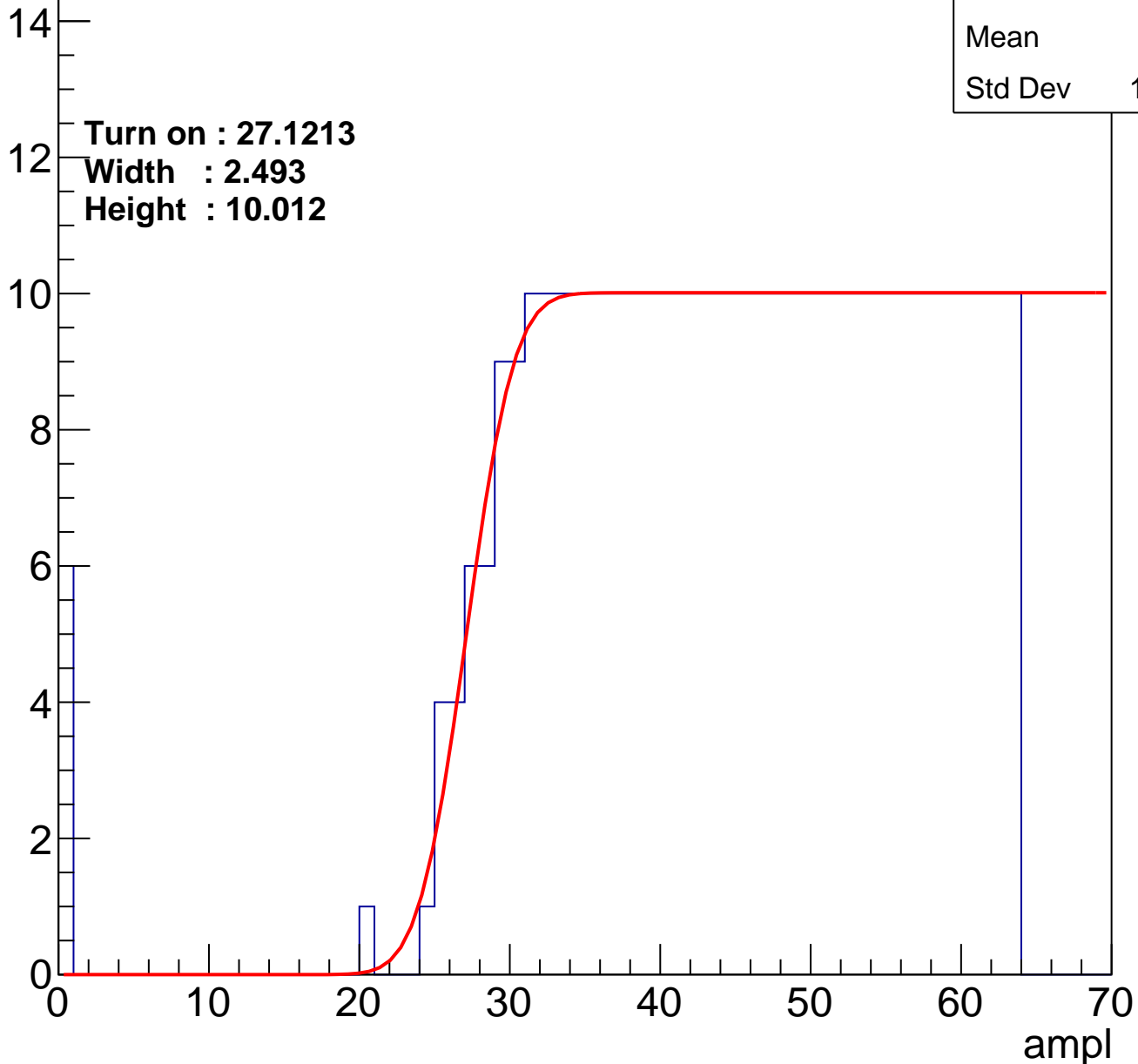
Entries	376
Mean	44.2
Std Dev	12.12

Turn on : 27.1213

Width : 2.493

Height : 10.012

Entry



B1L101S, U3-ch70

calib_packv5_042523_0143.root, FC#0, port D2

Entries	397
Mean	43.13
Std Dev	12.72

Turn on : 24.9468

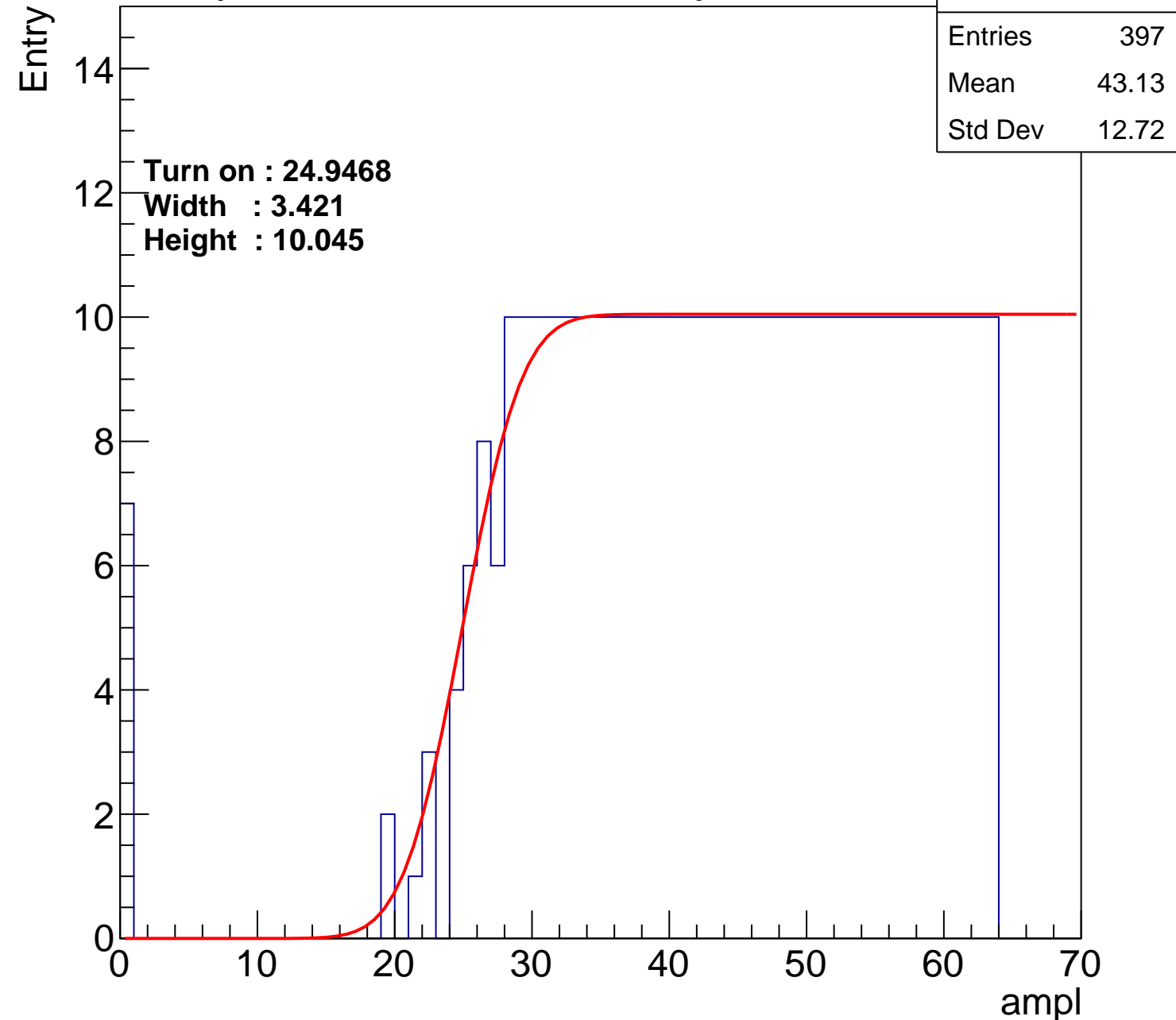
Width : 3.421

Height : 10.045

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch71

calib_packv5_042523_0143.root, FC#0, port D2

Entries	391
Mean	43.55
Std Dev	12.18

Turn on : 25.4336

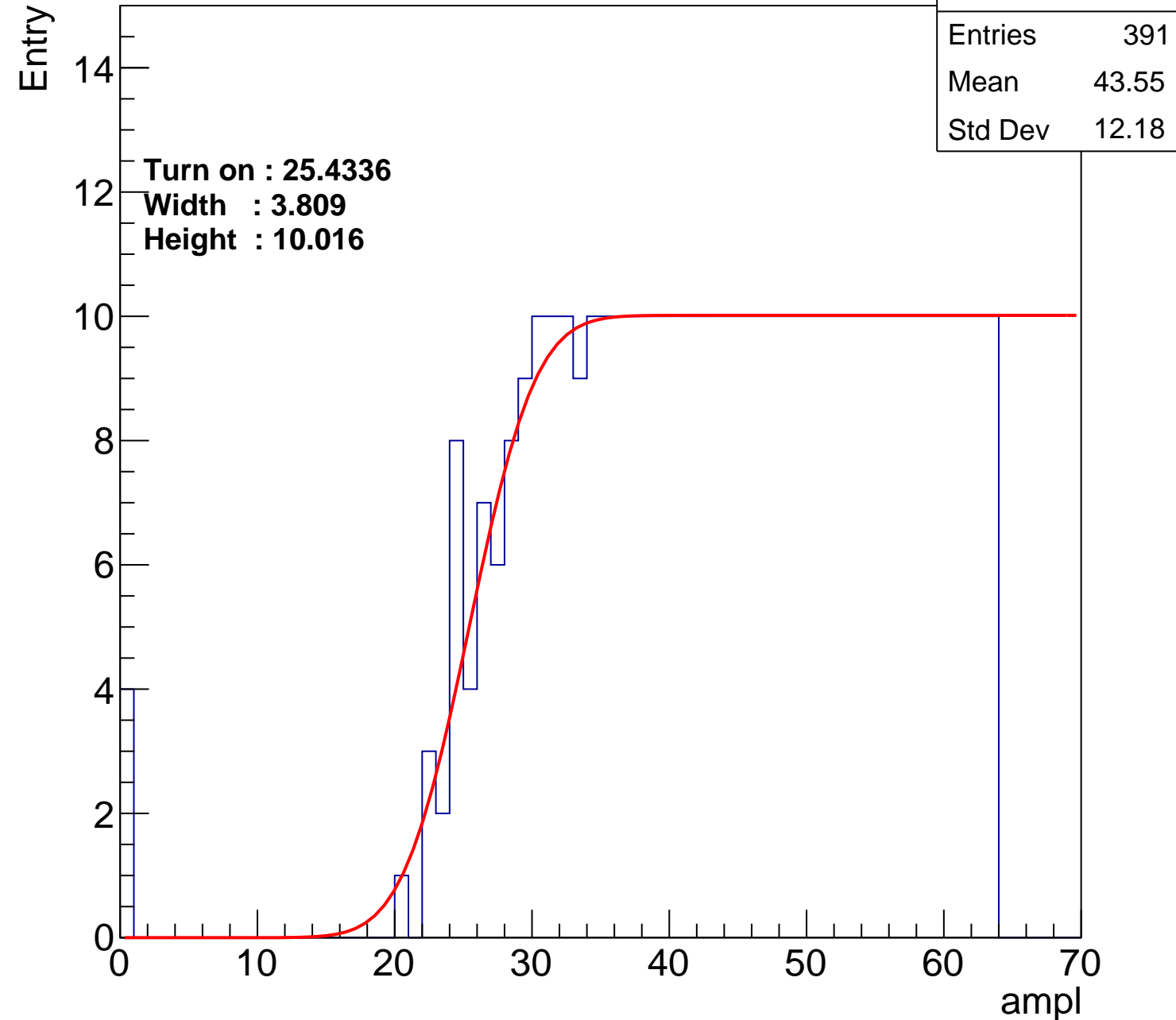
Width : 3.809

Height : 10.016

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch72

calib_packv5_042523_0143.root, FC#0, port D2

Entries	377
Mean	44.05
Std Dev	12.36

Turn on : 26.3071

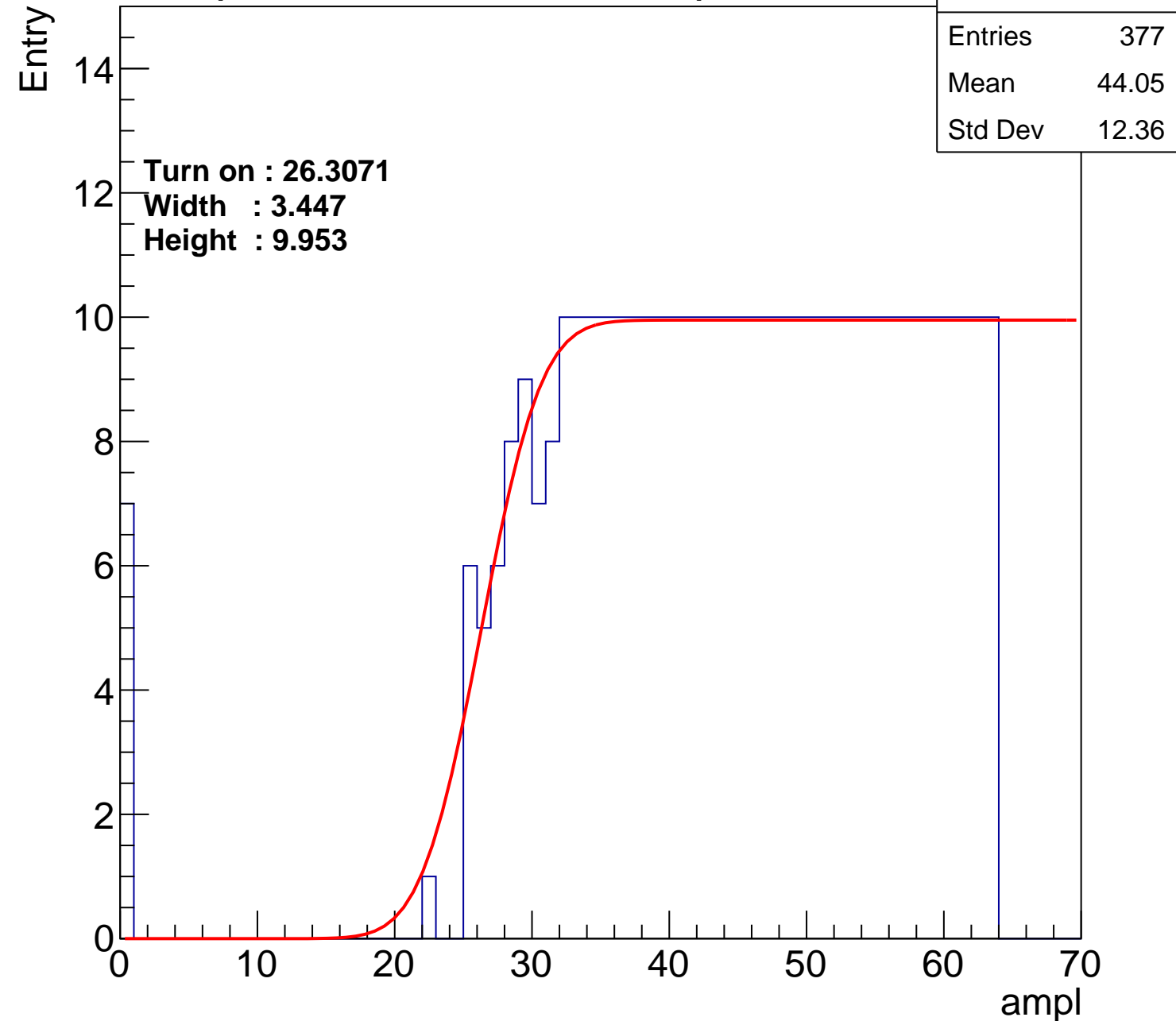
Width : 3.447

Height : 9.953

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch73

calib_packv5_042523_0143.root, FC#0, port D2

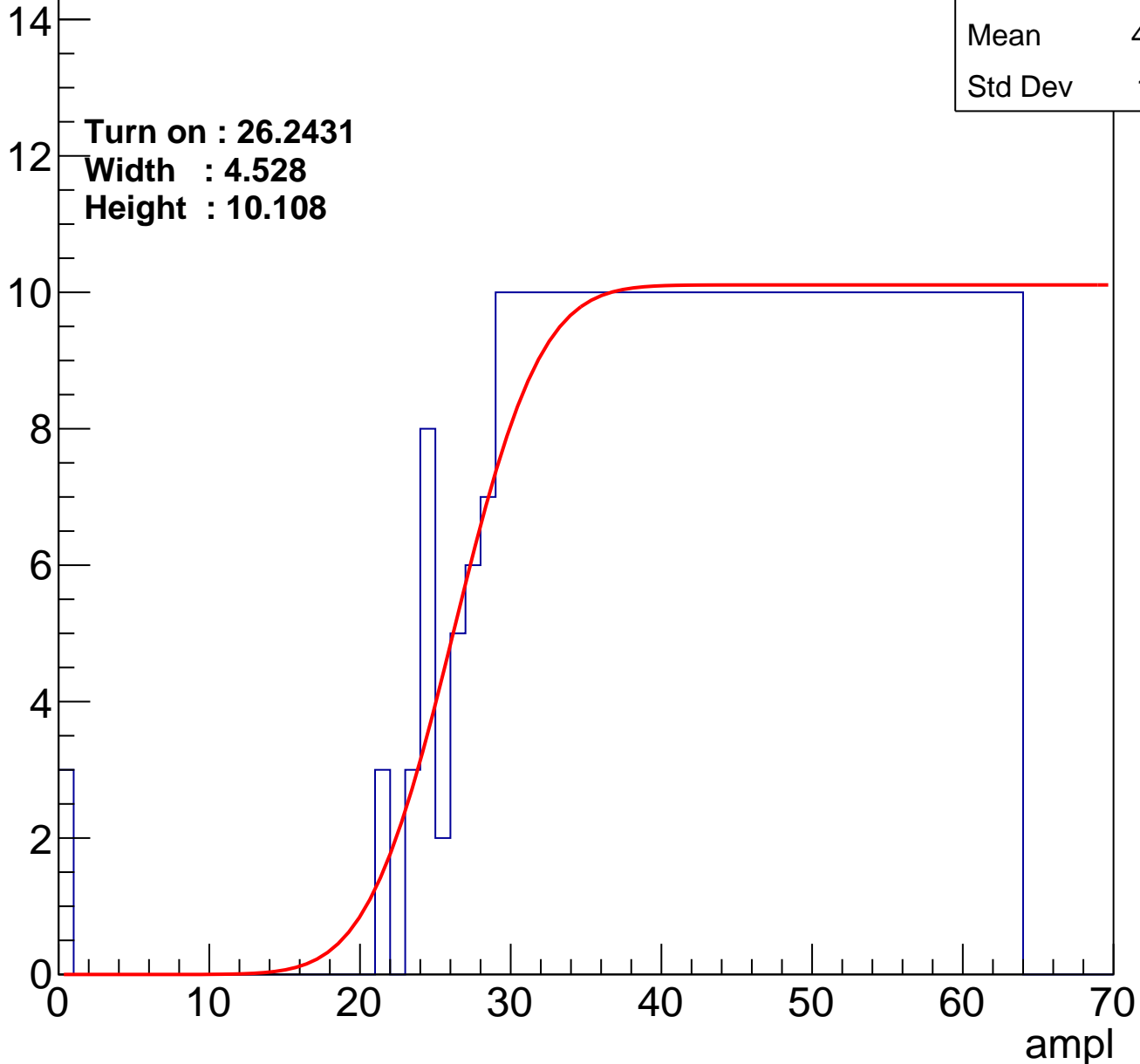
Entries	387
Mean	43.83
Std Dev	11.91

Turn on : 26.2431

Width : 4.528

Height : 10.108

Entry



B1L101S, U3-ch74

calib_packv5_042523_0143.root, FC#0, port D2

Entries	389
Mean	43.58
Std Dev	12.31

Turn on : 25.5184

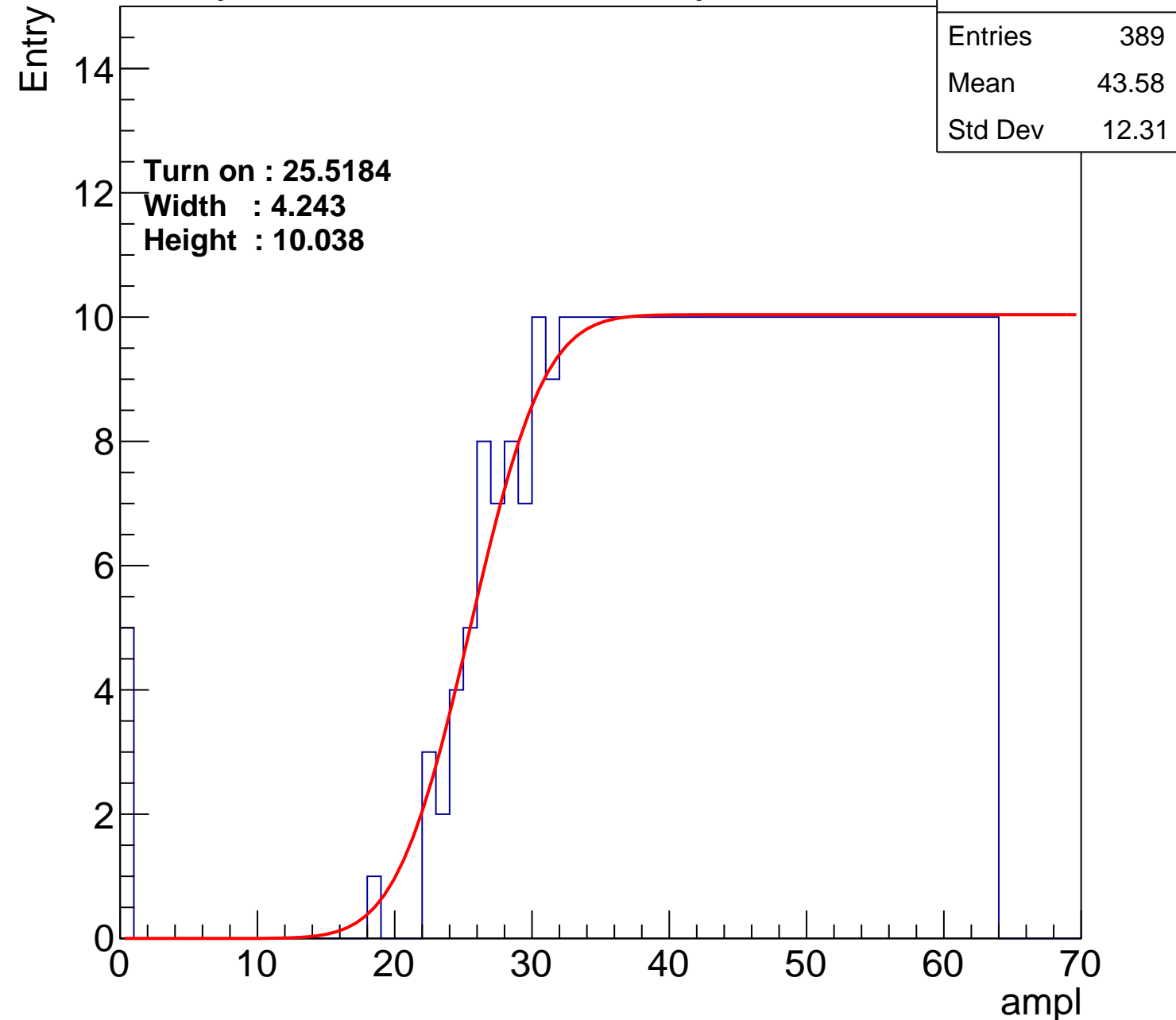
Width : 4.243

Height : 10.038

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch75

calib_packv5_042523_0143.root, FC#0, port D2

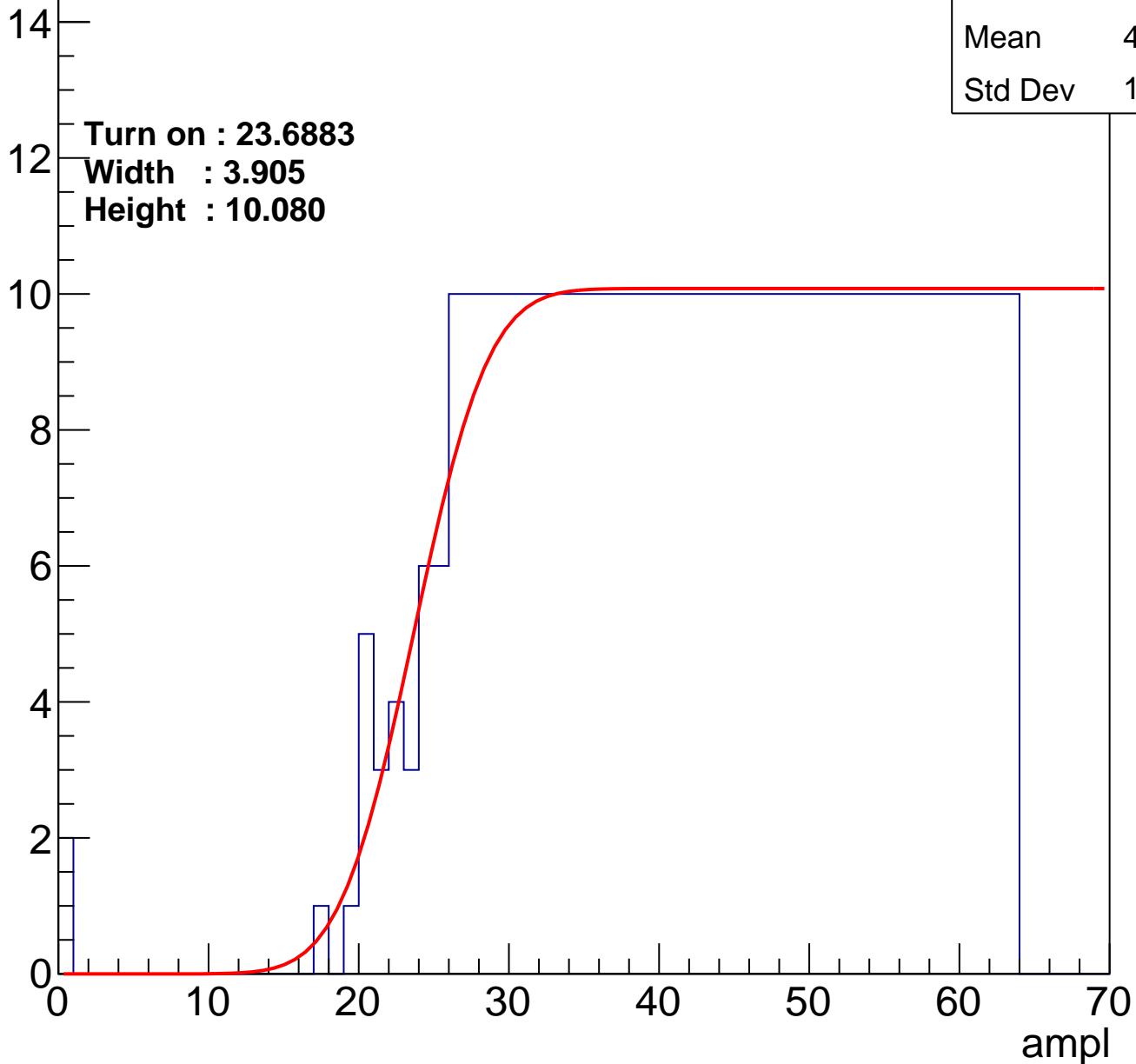
Entries	411
Mean	42.73
Std Dev	12.35

Turn on : 23.6883

Width : 3.905

Height : 10.080

Entry



B1L101S, U3-ch76

calib_packv5_042523_0143.root, FC#0, port D2

Entries	390
Mean	43.4
Std Dev	12.73

Turn on : 26.1295

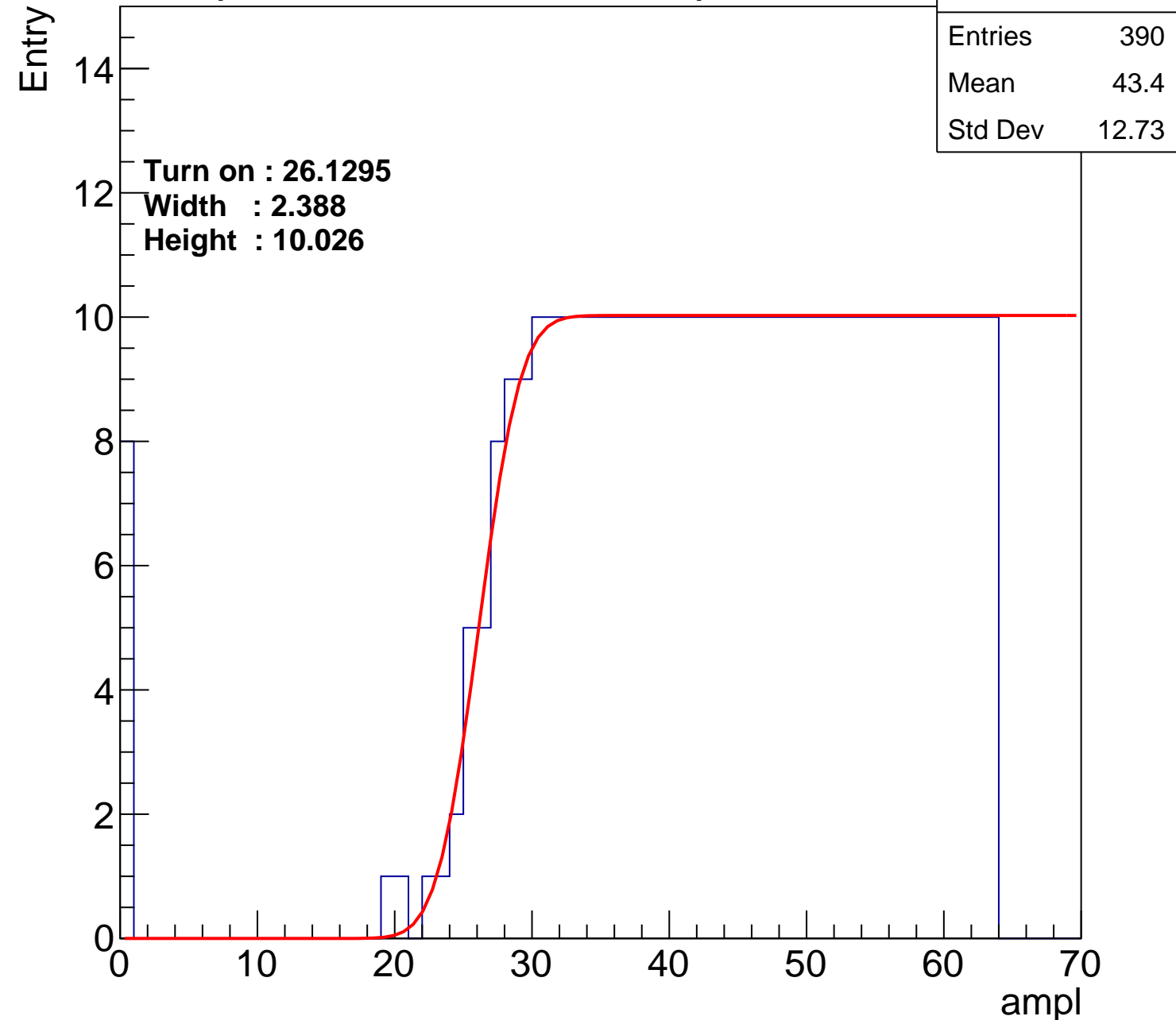
Width : 2.388

Height : 10.026

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch77

calib_packv5_042523_0143.root, FC#0, port D2

Entries	382
Mean	44.05
Std Dev	11.9

Turn on : 25.9533

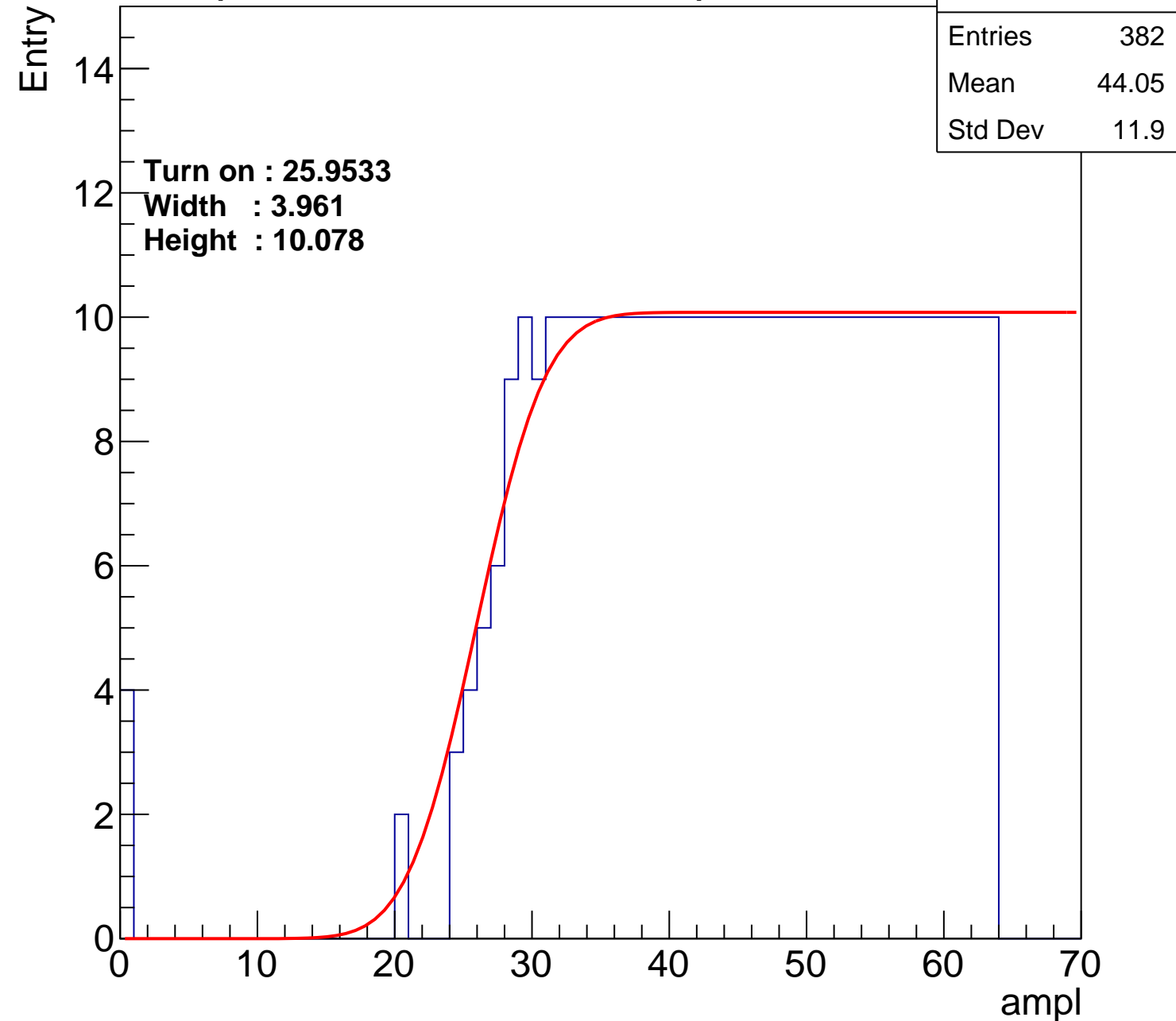
Width : 3.961

Height : 10.078

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch78

calib_packv5_042523_0143.root, FC#0, port D2

Entries	398
Mean	43.18
Std Dev	12.47

Turn on : 25.2785

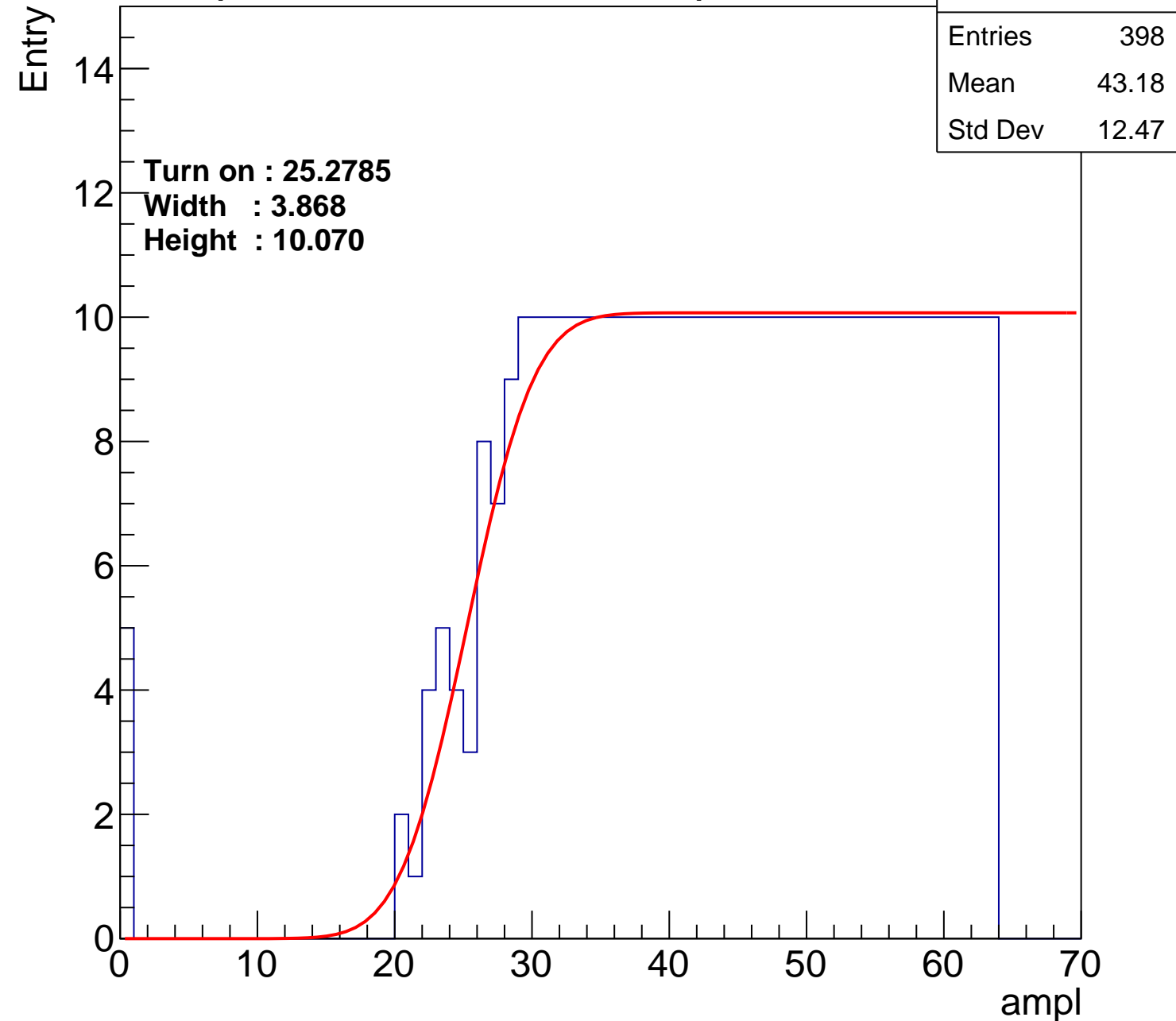
Width : 3.868

Height : 10.070

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch79

calib_packv5_042523_0143.root, FC#0, port D2

Entries	384
Mean	44.06
Std Dev	11.63

Turn on : 25.8387

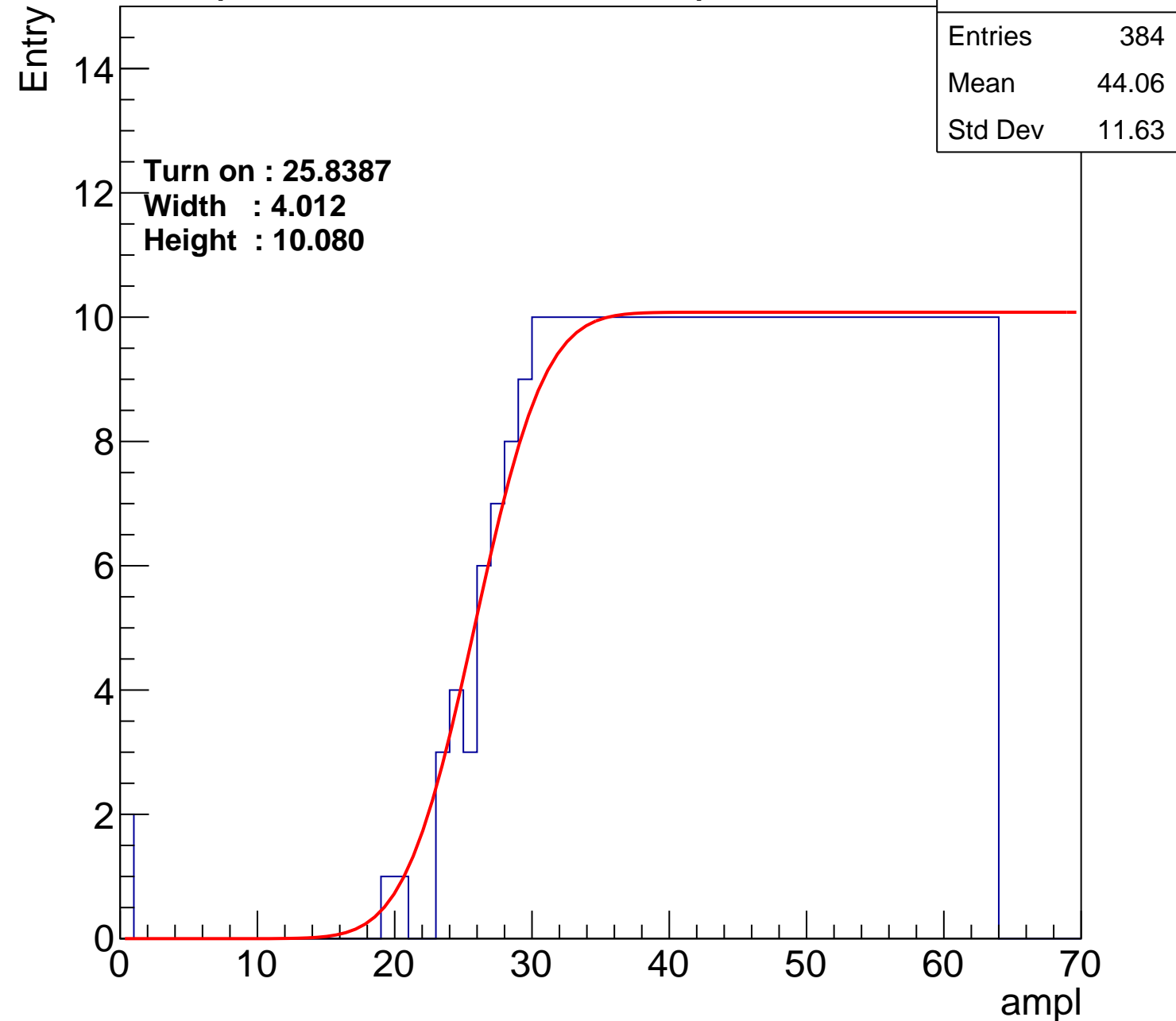
Width : 4.012

Height : 10.080

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch80

calib_packv5_042523_0143.root, FC#0, port D2

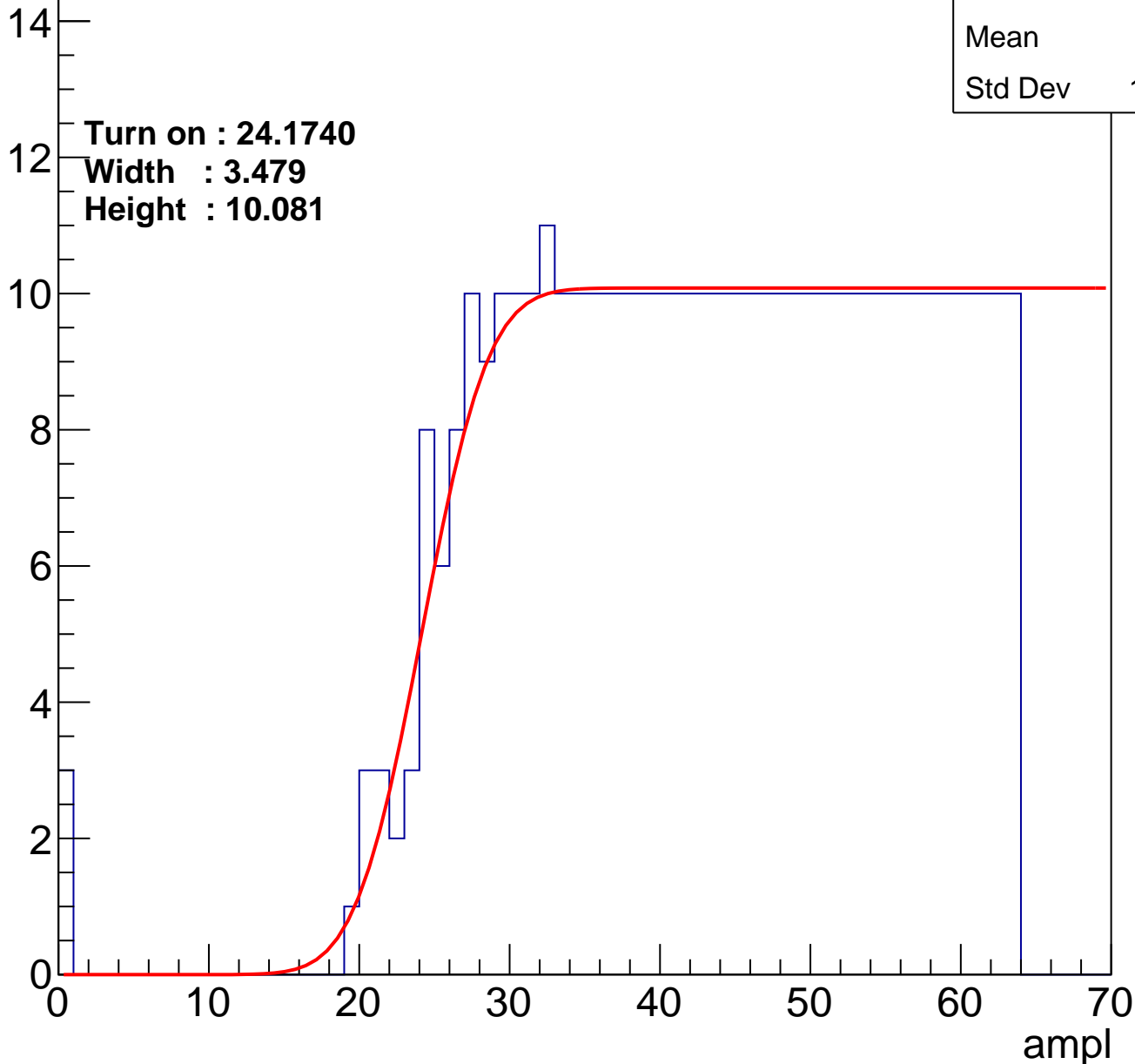
Entries	407
Mean	42.9
Std Dev	12.34

Turn on : 24.1740

Width : 3.479

Height : 10.081

Entry



B1L101S, U3-ch81

calib_packv5_042523_0143.root, FC#0, port D2

Entries	382
Mean	43.92
Std Dev	12.17

Turn on : 26.8326

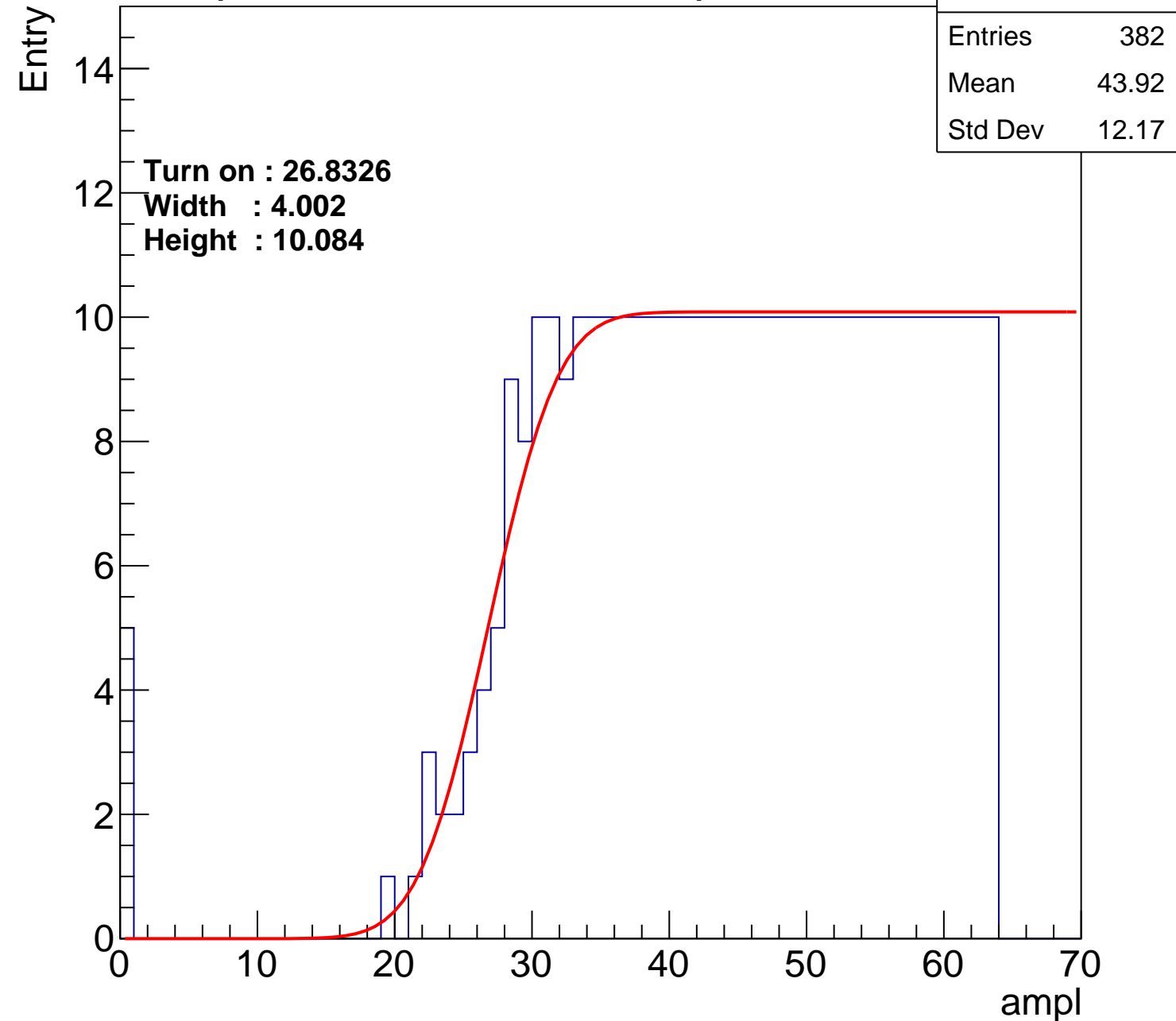
Width : 4.002

Height : 10.084

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch82

calib_packv5_042523_0143.root, FC#0, port D2

Entries	388
Mean	43.49
Std Dev	12.63

Turn on : 26.3248

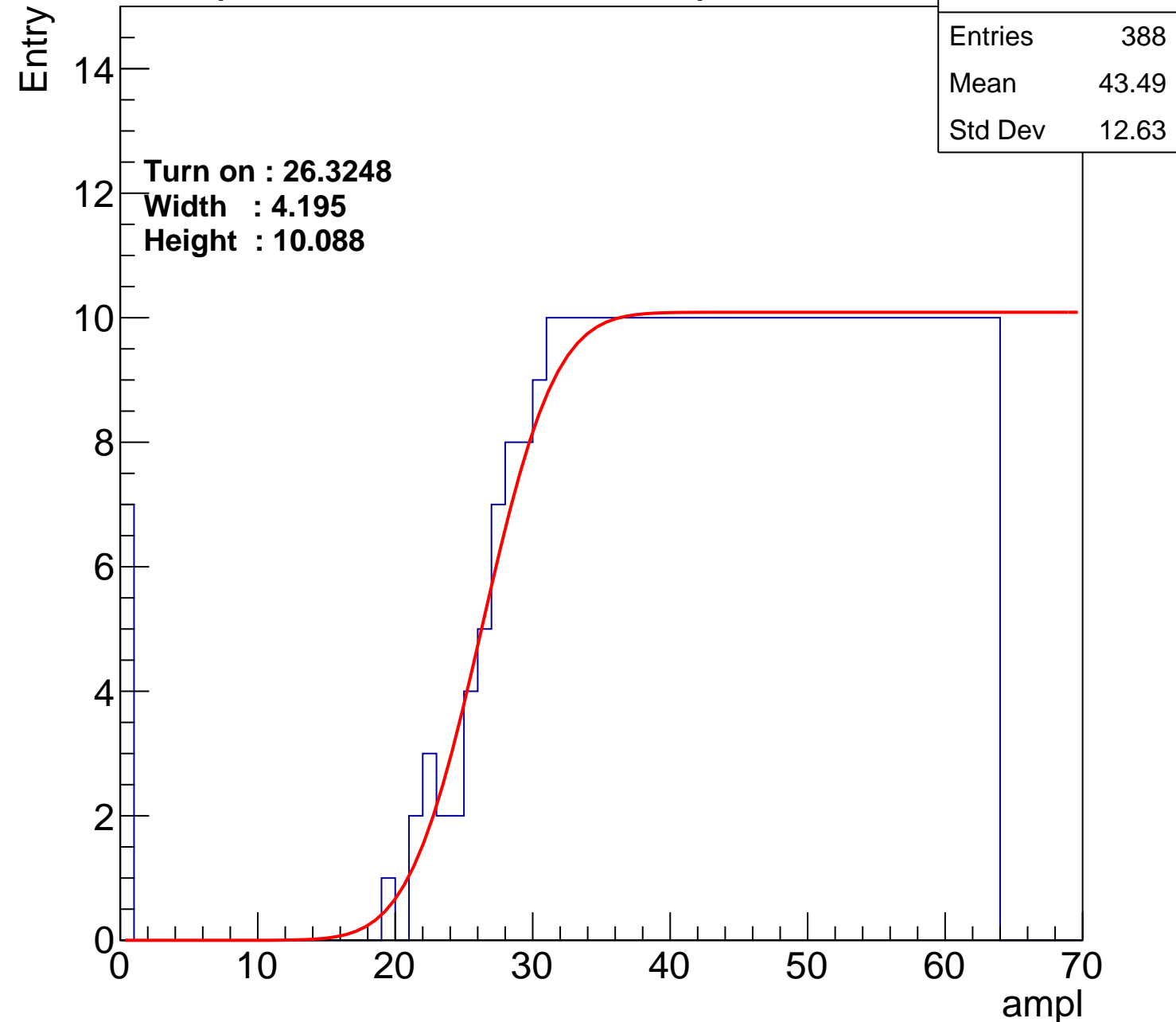
Width : 4.195

Height : 10.088

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch83

calib_packv5_042523_0143.root, FC#0, port D2

Entries	380
Mean	44.15
Std Dev	11.76

Turn on : 26.8636

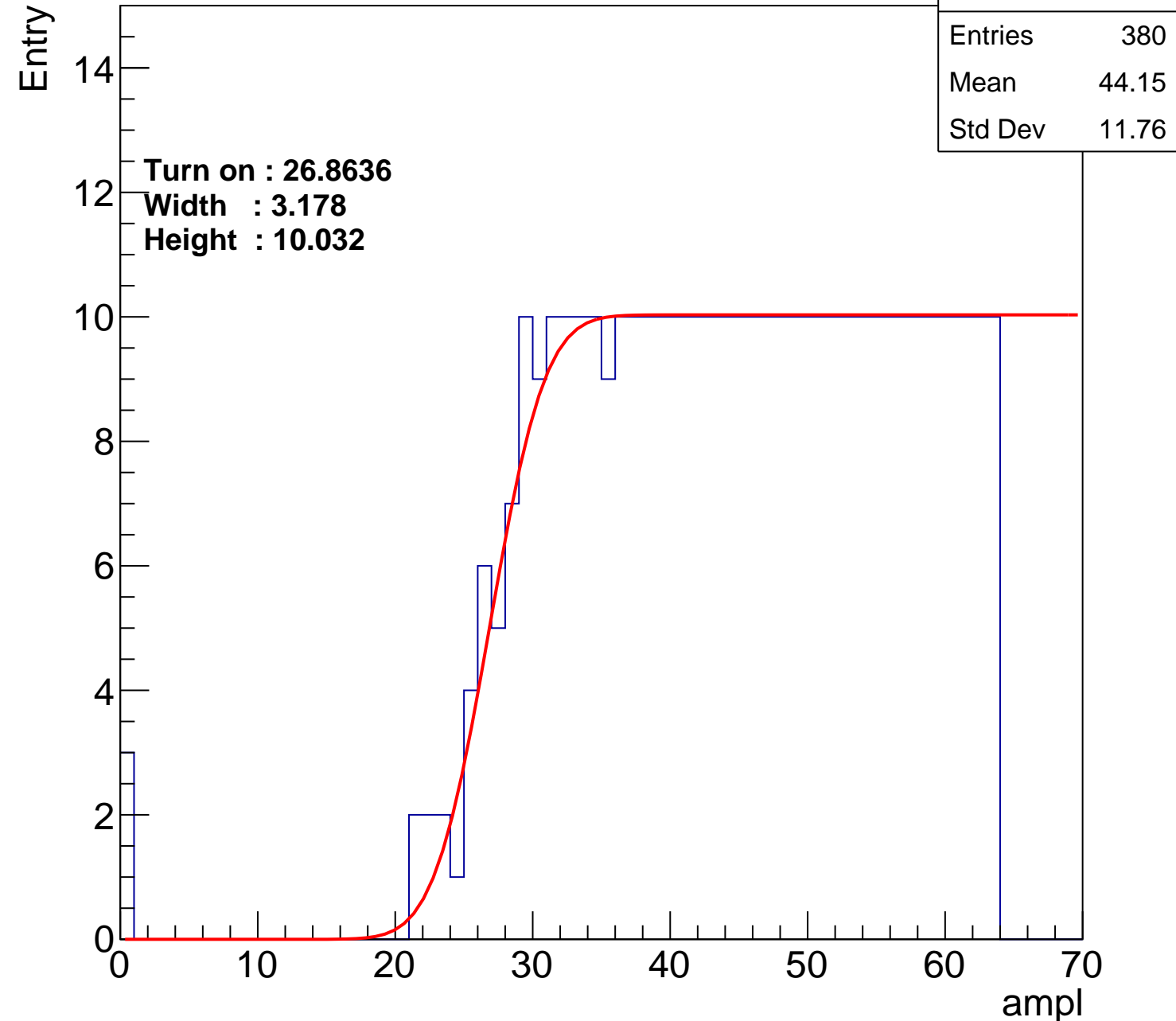
Width : 3.178

Height : 10.032

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch84

calib_packv5_042523_0143.root, FC#0, port D2

Entries	392
Mean	43.43
Std Dev	12.46

Turn on : 26.1110

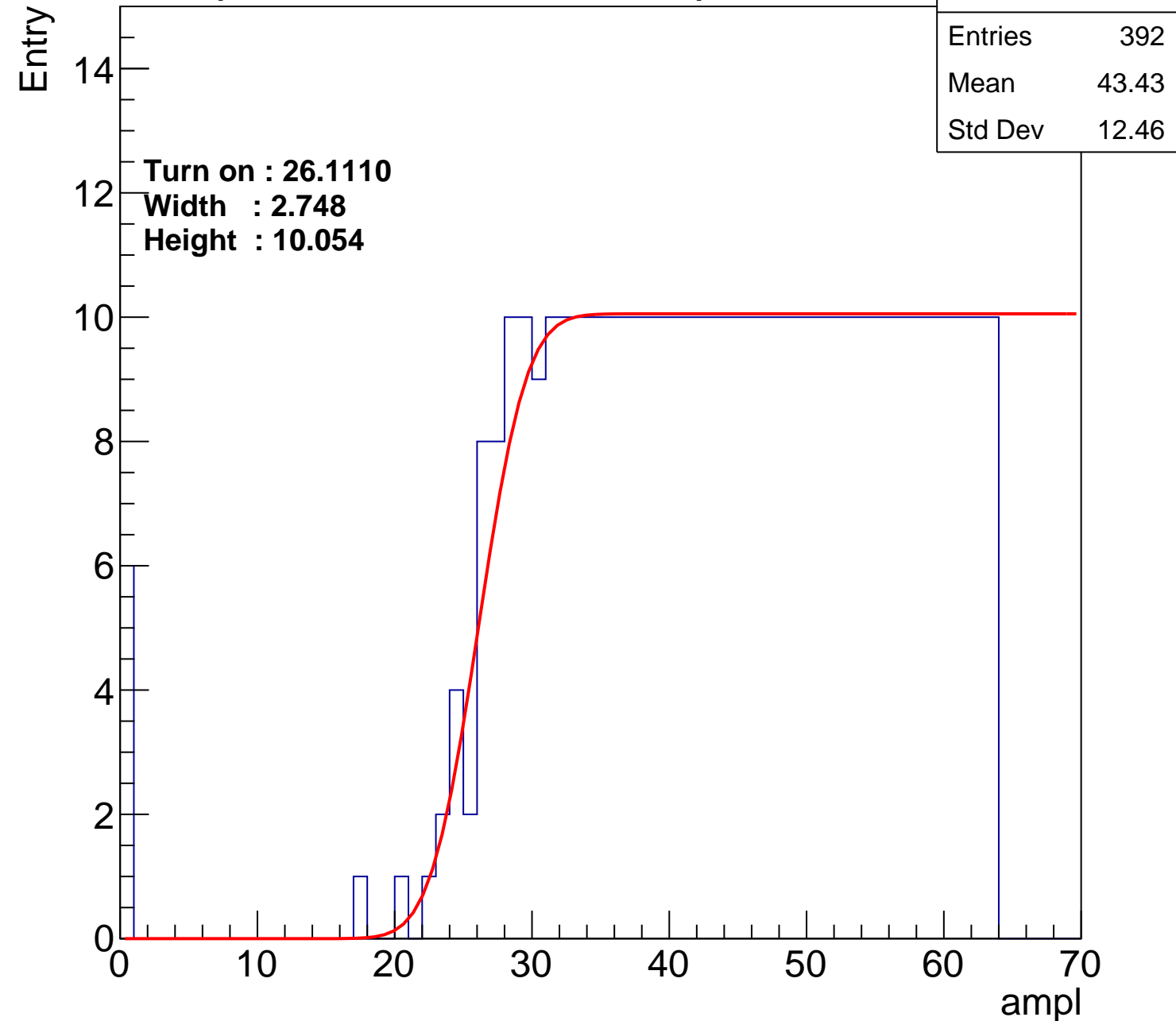
Width : 2.748

Height : 10.054

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch85

calib_packv5_042523_0143.root, FC#0, port D2

Entries	385
Mean	43.81
Std Dev	12.1

Turn on : 26.7158

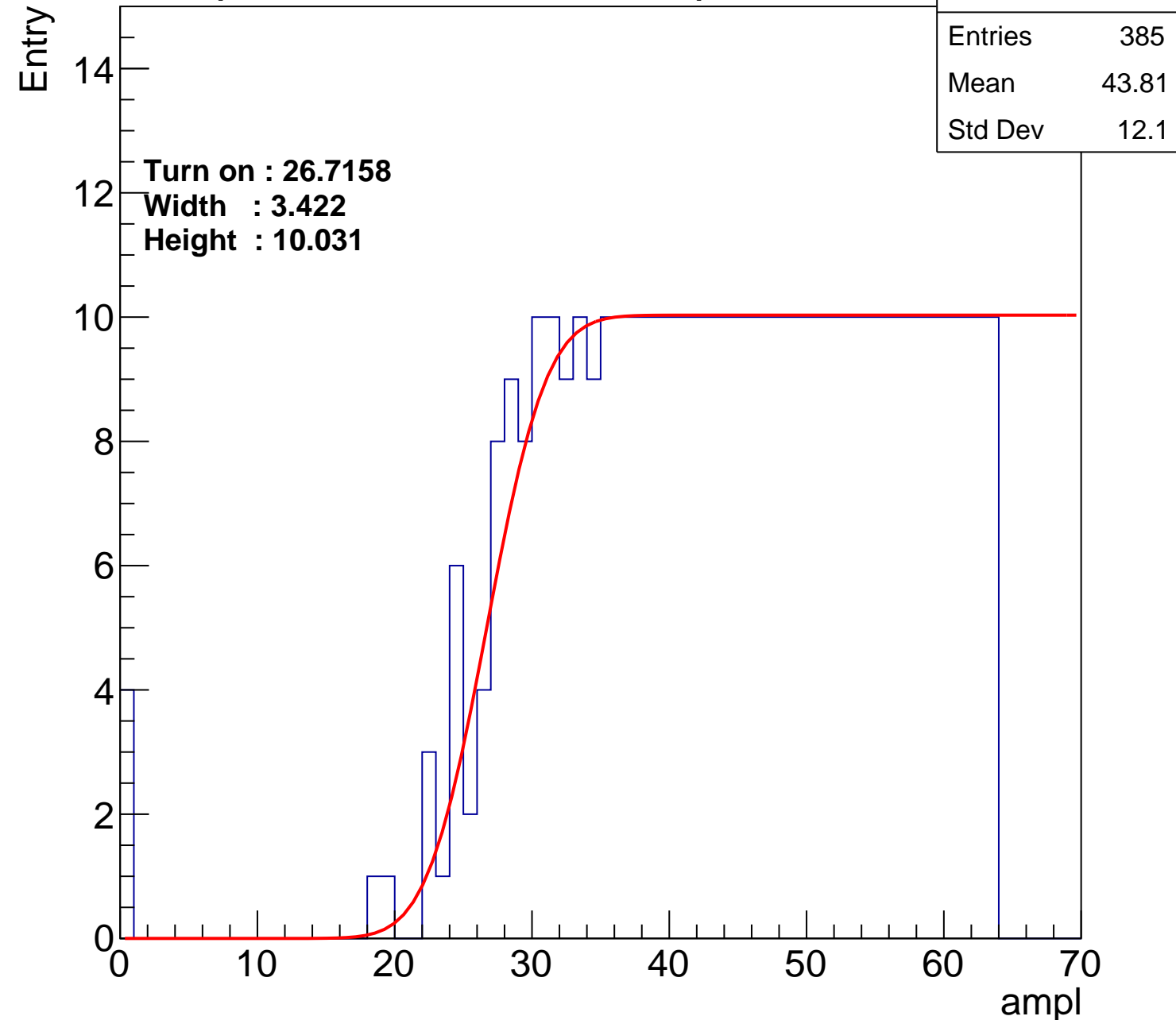
Width : 3.422

Height : 10.031

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch86

calib_packv5_042523_0143.root, FC#0, port D2

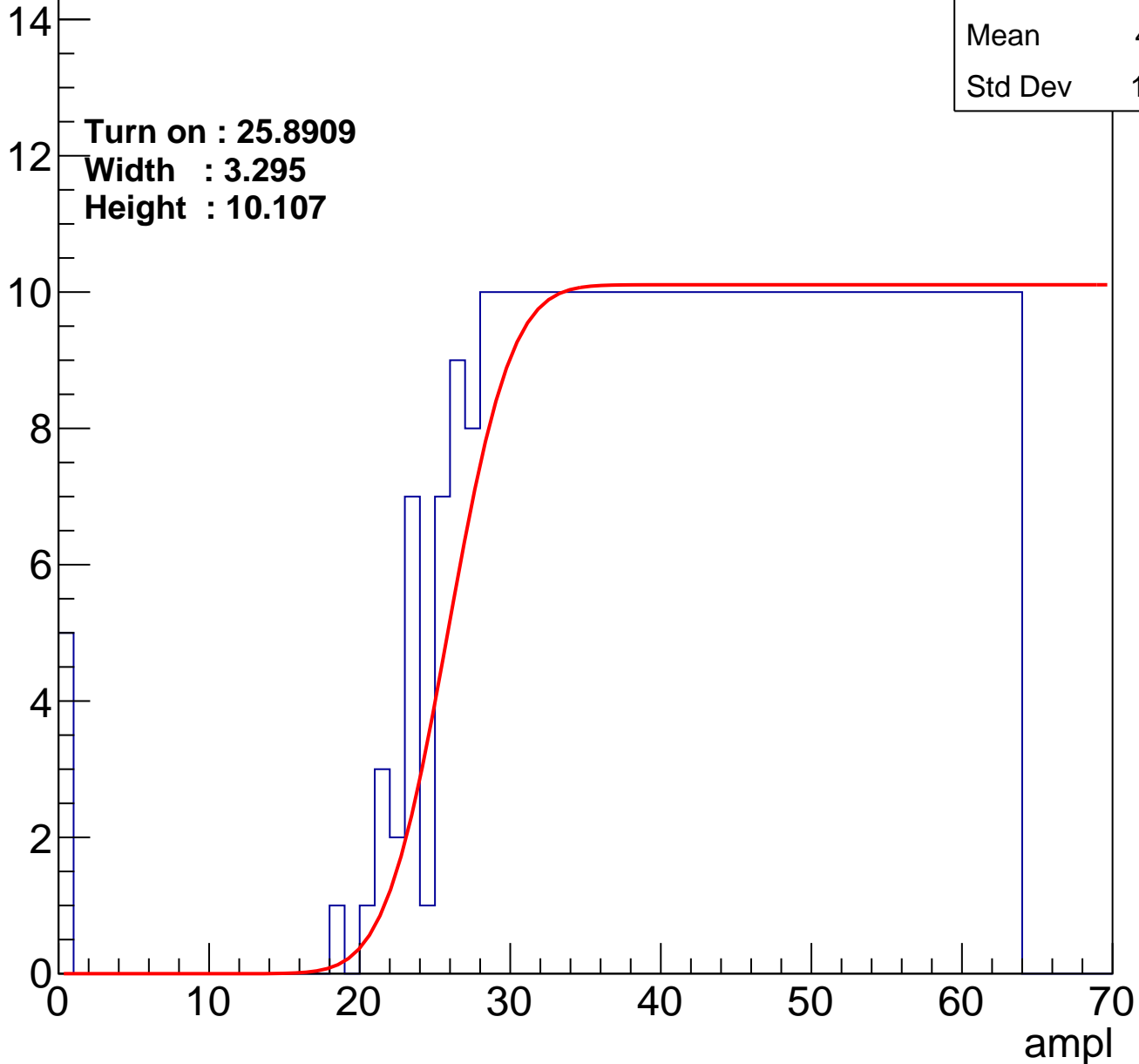
Entries	404
Mean	42.91
Std Dev	12.58

Turn on : 25.8909

Width : 3.295

Height : 10.107

Entry



B1L101S, U3-ch87

calib_packv5_042523_0143.root, FC#0, port D2

Entries	403
Mean	42.87
Std Dev	12.74

Turn on : 24.6535

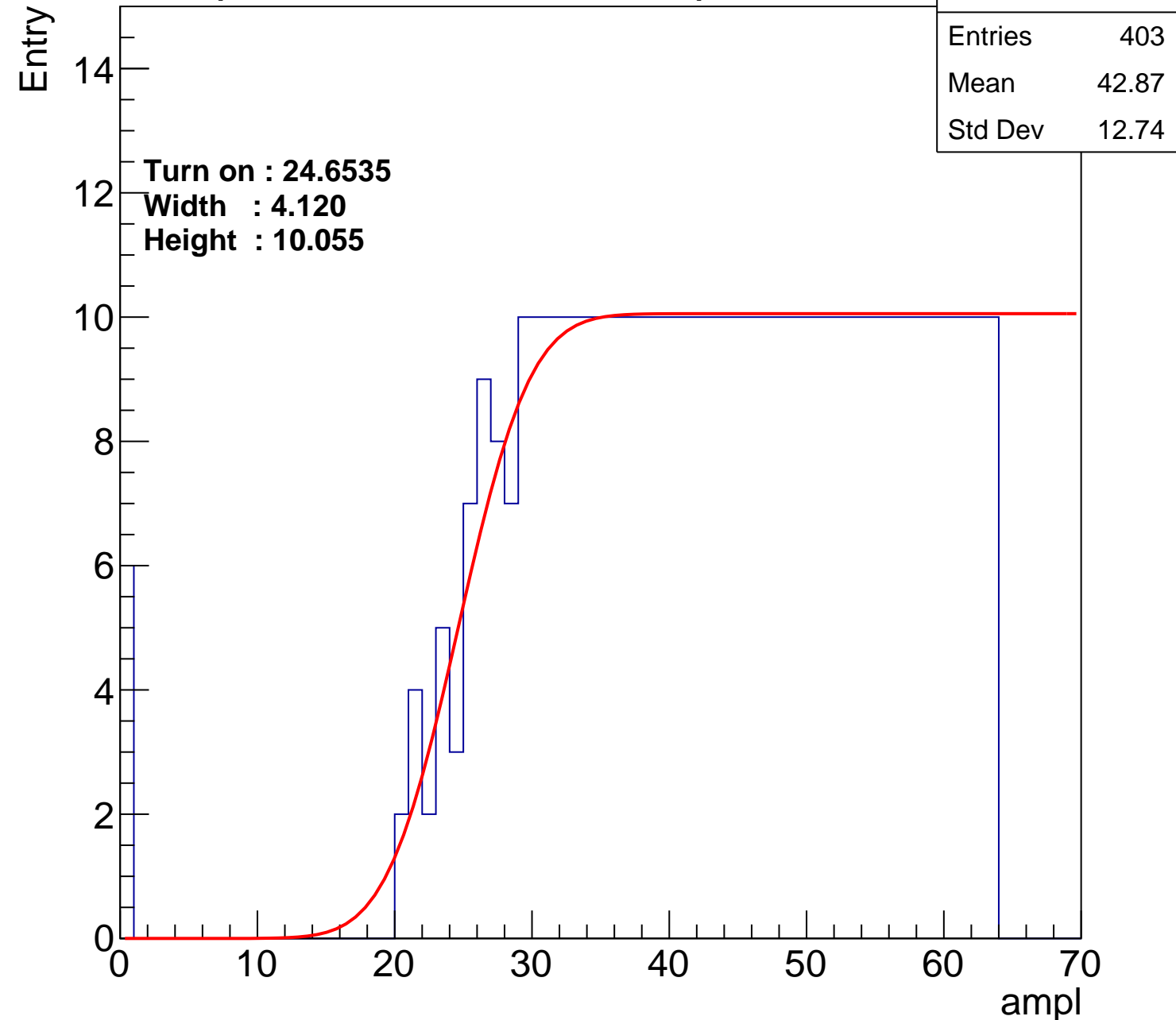
Width : 4.120

Height : 10.055

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch88

calib_packv5_042523_0143.root, FC#0, port D2

Entries	391
Mean	43.67
Std Dev	11.89

Turn on : 25.3834

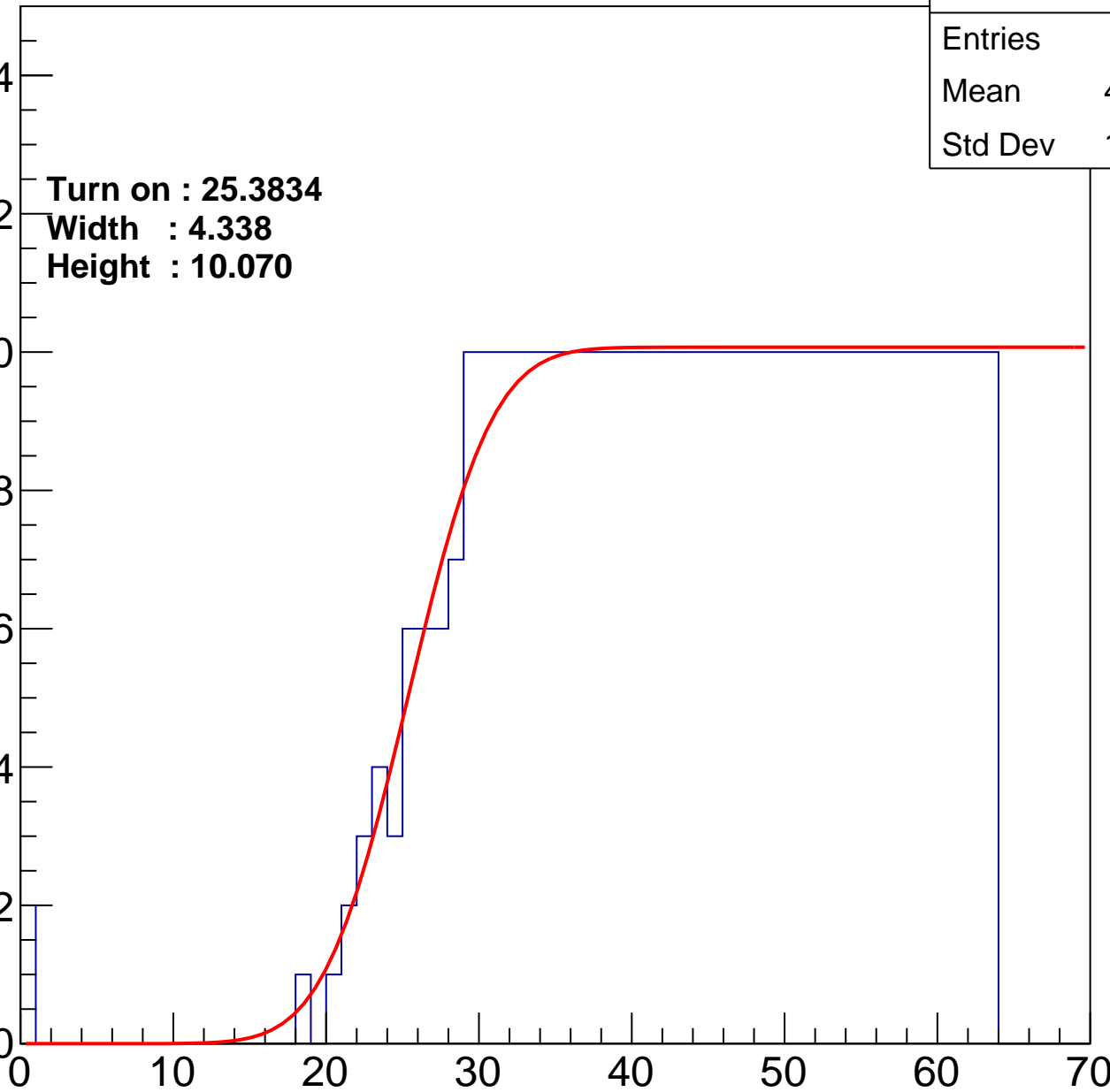
Width : 4.338

Height : 10.070

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch89

calib_packv5_042523_0143.root, FC#0, port D2

Entries	386
Mean	43.89
Std Dev	11.85

Turn on : 25.1557

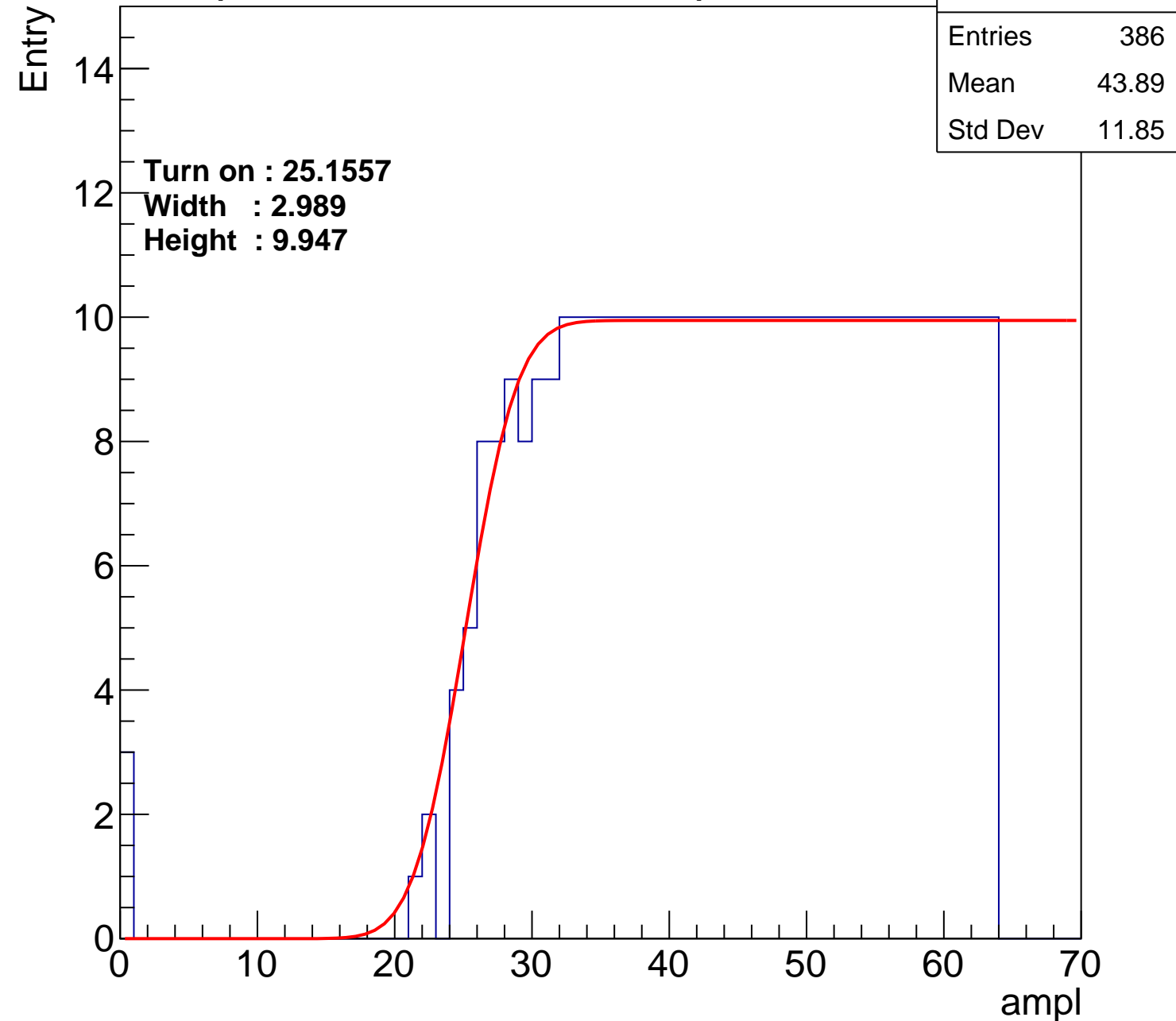
Width : 2.989

Height : 9.947

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch90

calib_packv5_042523_0143.root, FC#0, port D2

Entries	375
Mean	44.33
Std Dev	11.83

Turn on : 27.6205

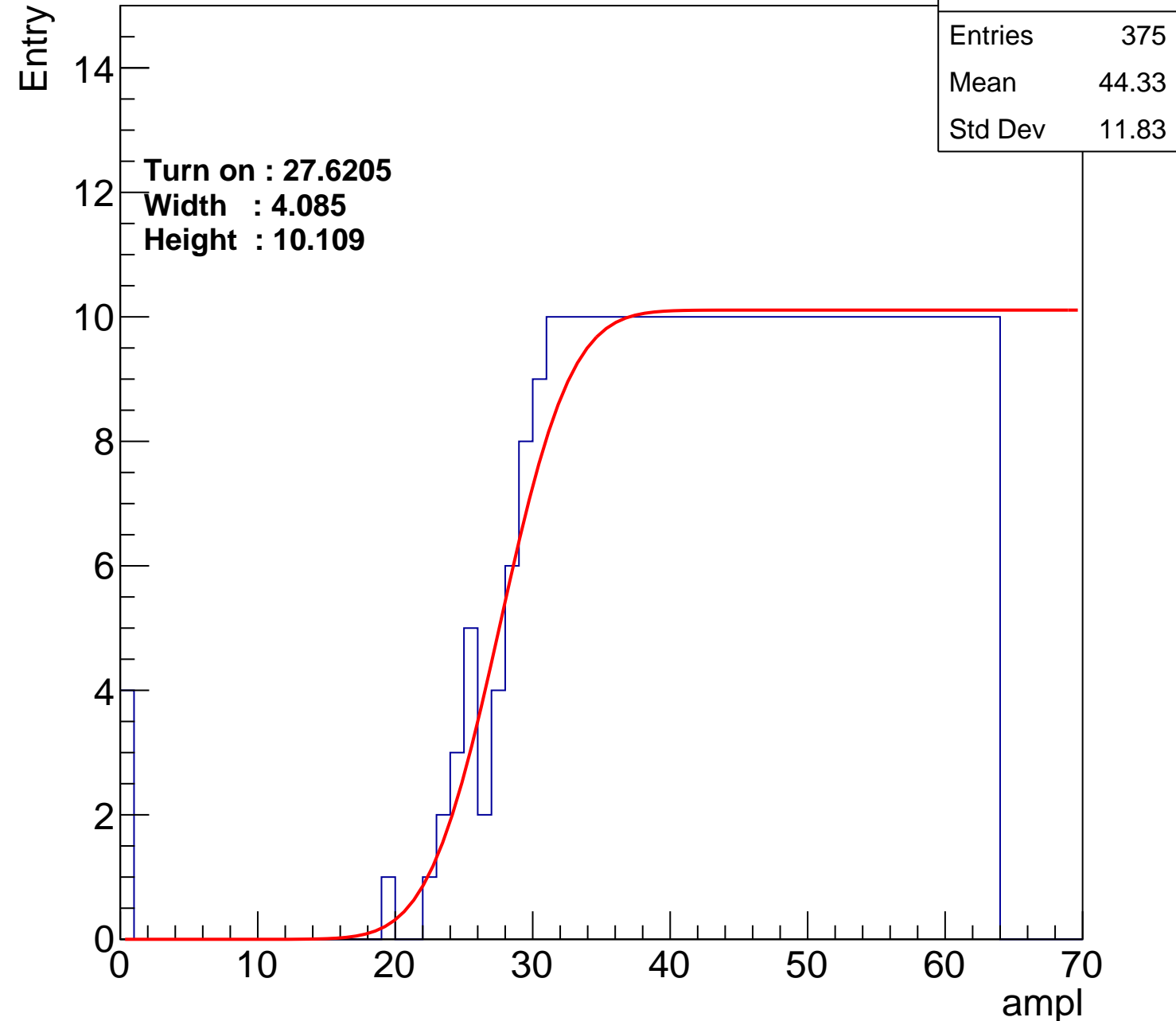
Width : 4.085

Height : 10.109

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch91

calib_packv5_042523_0143.root, FC#0, port D2

Entries	374
Mean	44.34
Std Dev	11.84

Turn on : 26.9305

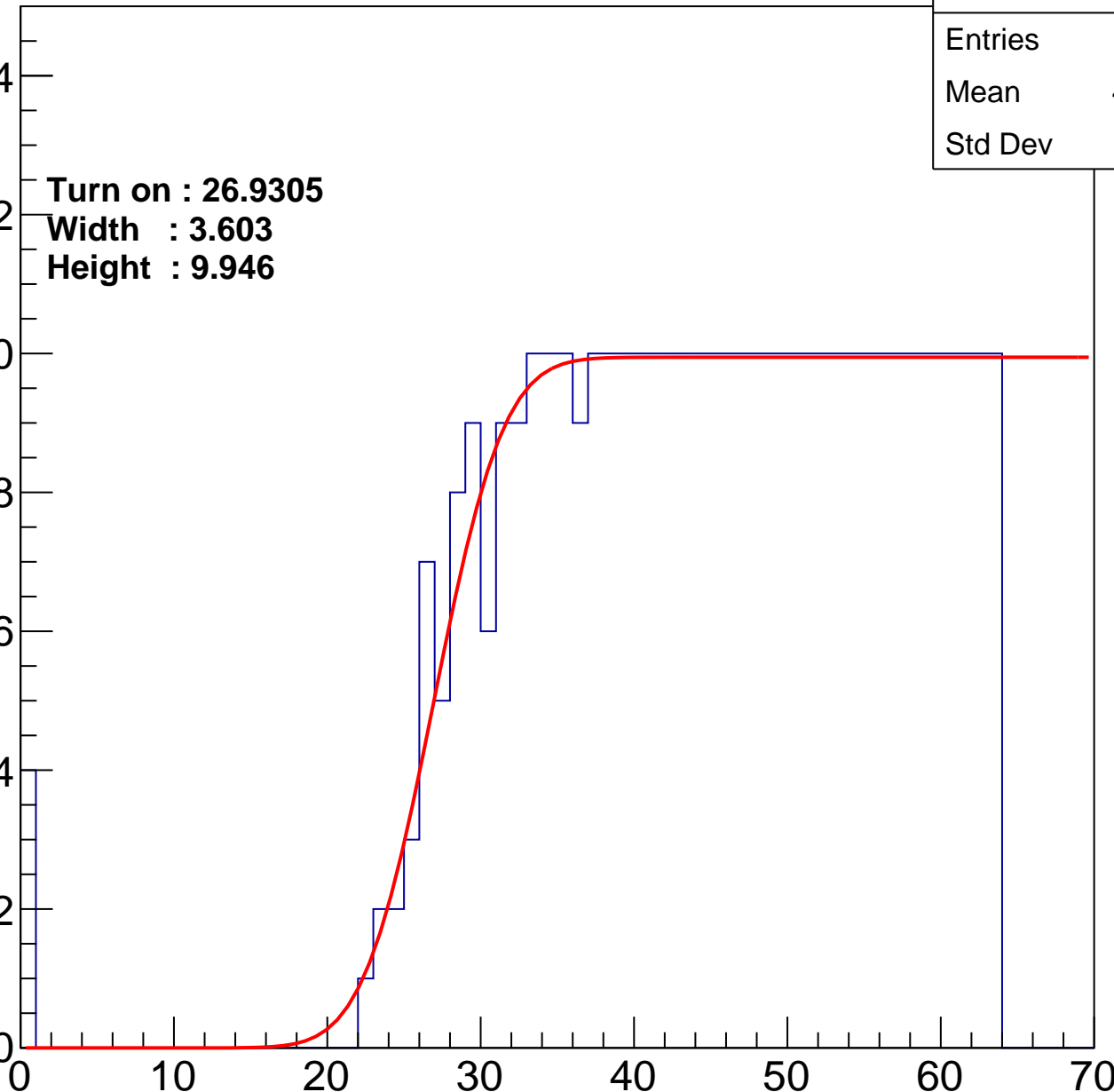
Width : 3.603

Height : 9.946

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch92

calib_packv5_042523_0143.root, FC#0, port D2

Entries	380
Mean	44.12
Std Dev	11.88

Turn on : 26.2798

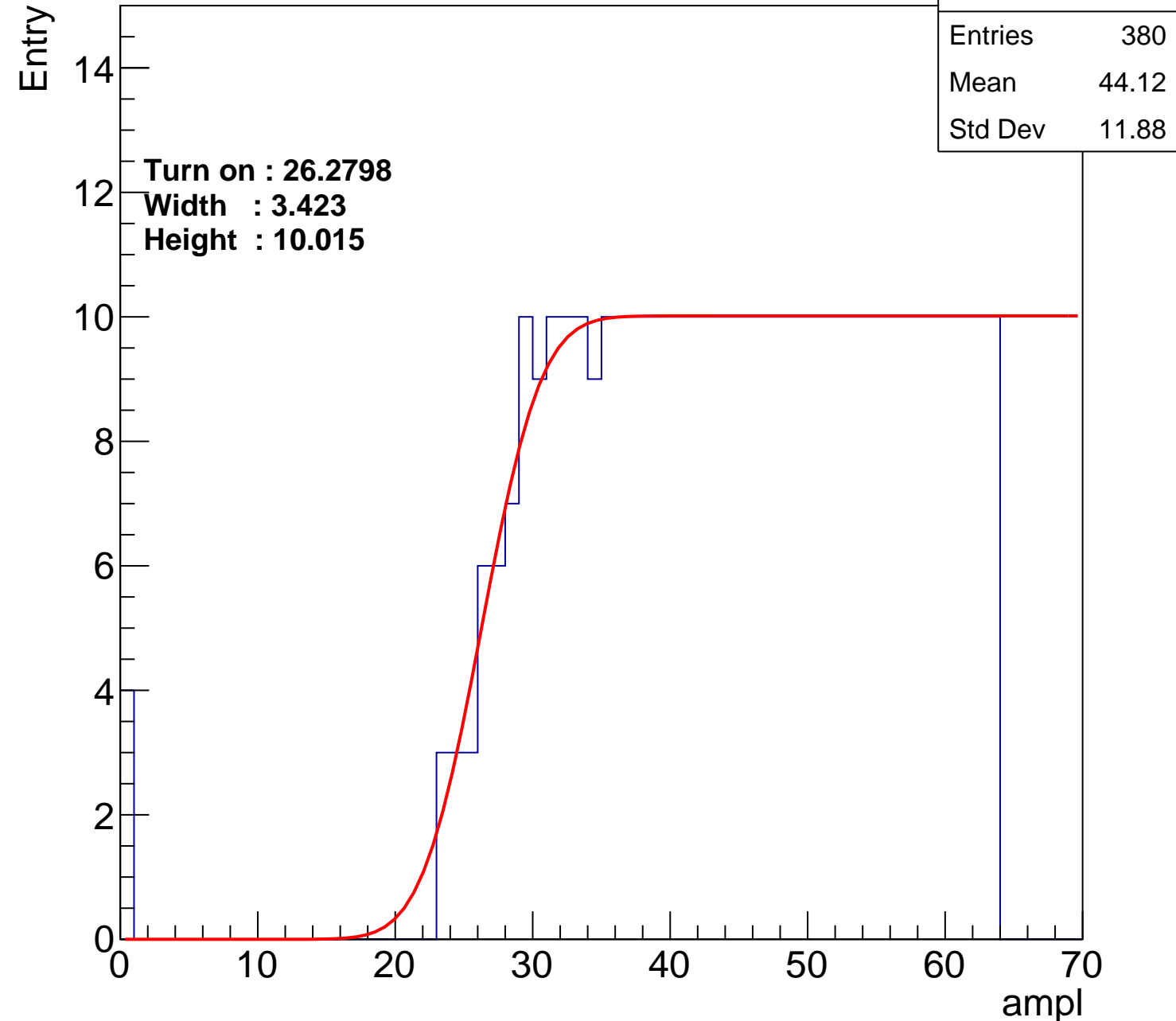
Width : 3.423

Height : 10.015

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch93

calib_packv5_042523_0143.root, FC#0, port D2

Entries	372
Mean	44.47
Std Dev	11.84

Turn on : 27.4737

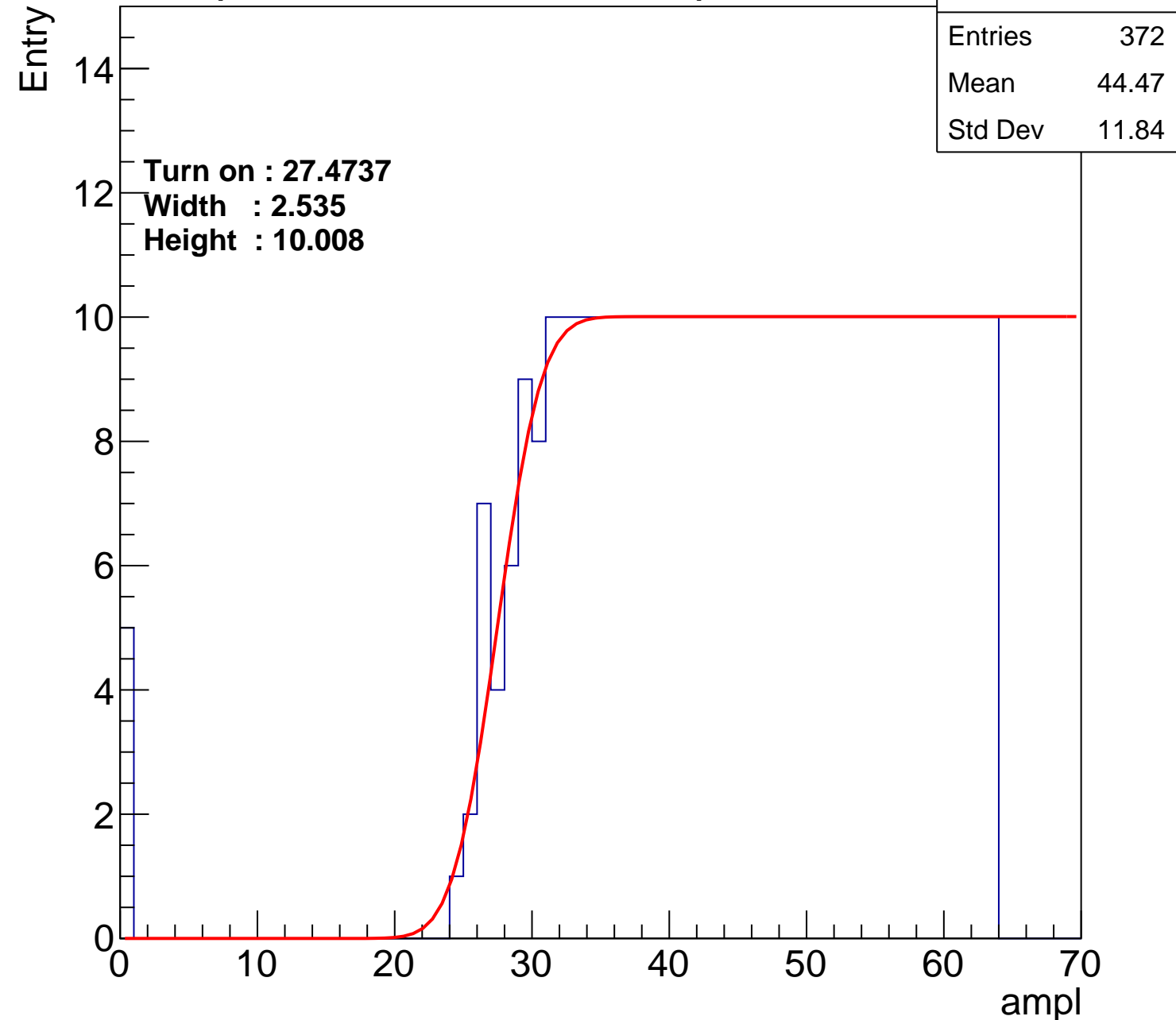
Width : 2.535

Height : 10.008

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch94

calib_packv5_042523_0143.root, FC#0, port D2

Entries	393
Mean	43.4
Std Dev	12.39

Turn on : 25.5490

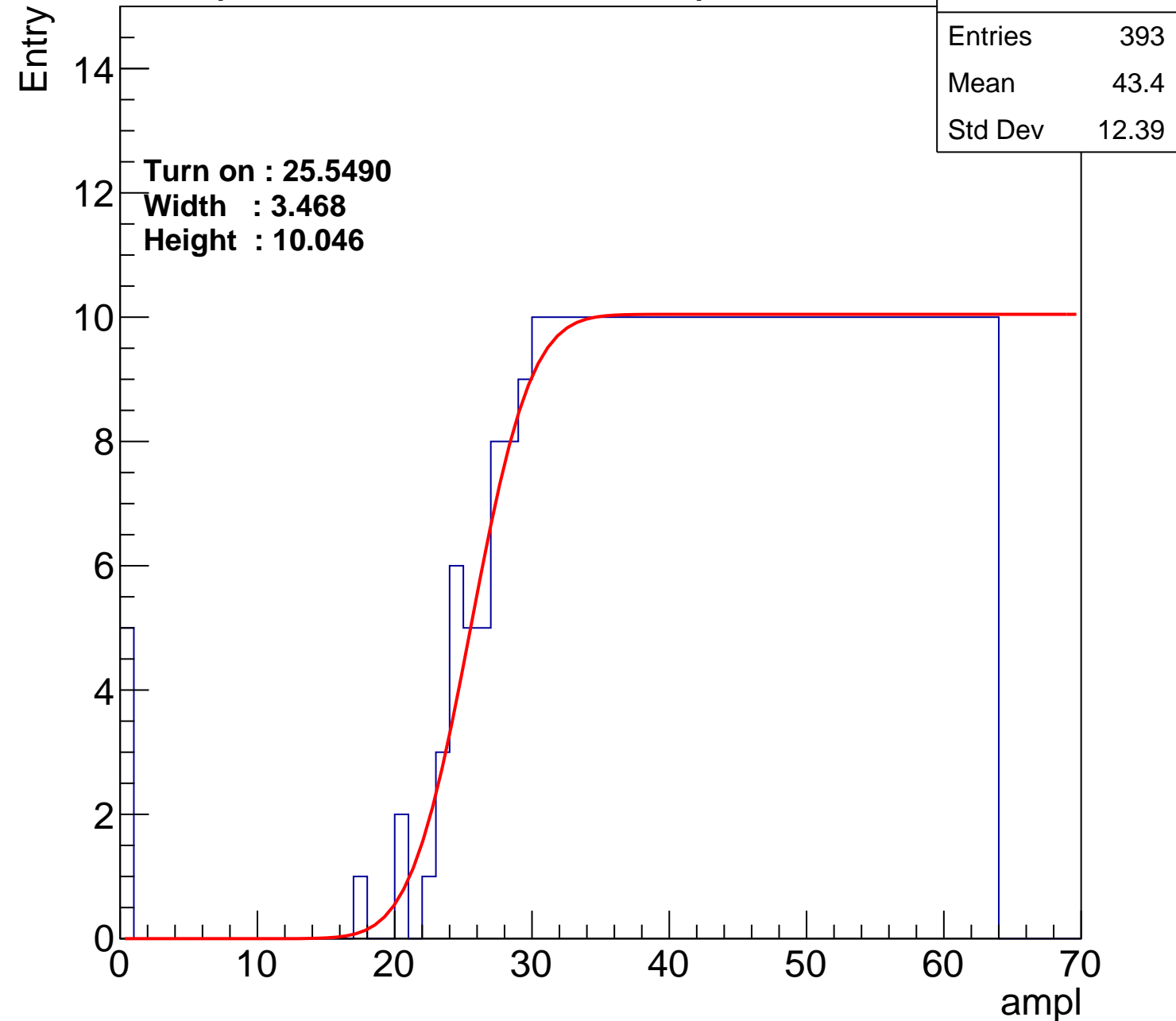
Width : 3.468

Height : 10.046

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch95

calib_packv5_042523_0143.root, FC#0, port D2

Entries	387
Mean	43.82
Std Dev	11.91

Turn on : 25.4403

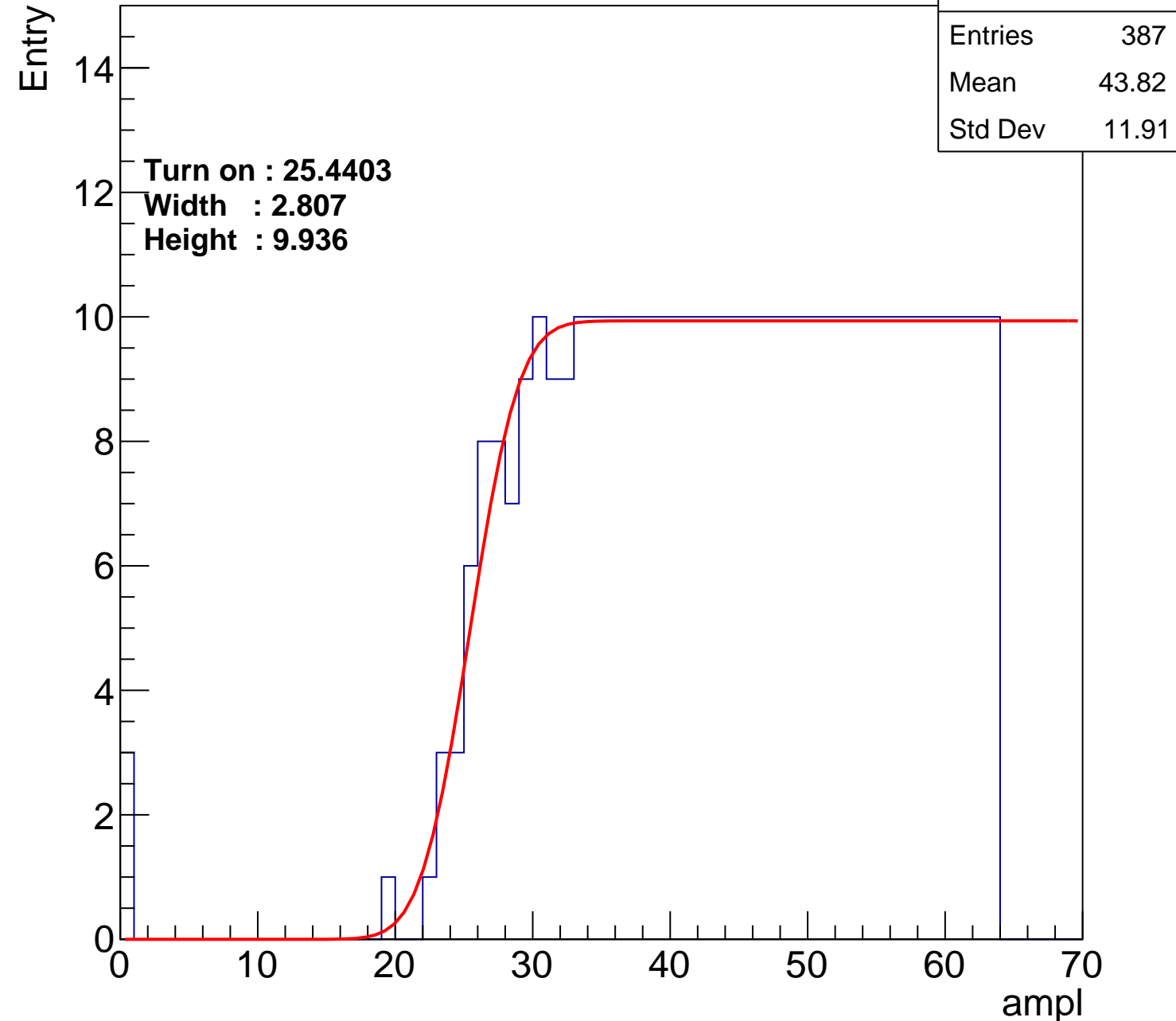
Width : 2.807

Height : 9.936

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch96

calib_packv5_042523_0143.root, FC#0, port D2

Entries	374
Mean	44.48
Std Dev	11.57

Turn on : 27.3191

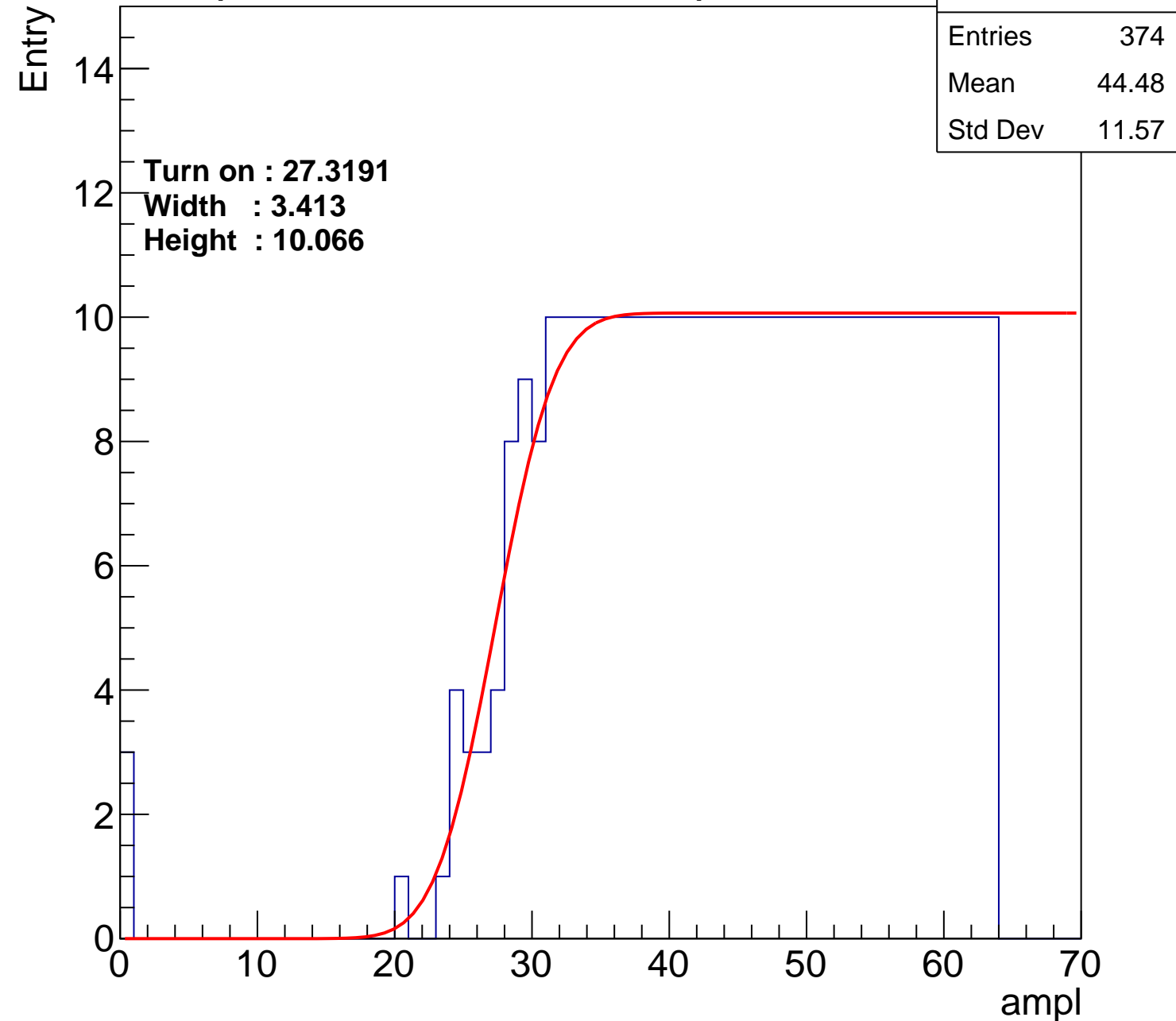
Width : 3.413

Height : 10.066

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch97

calib_packv5_042523_0143.root, FC#0, port D2

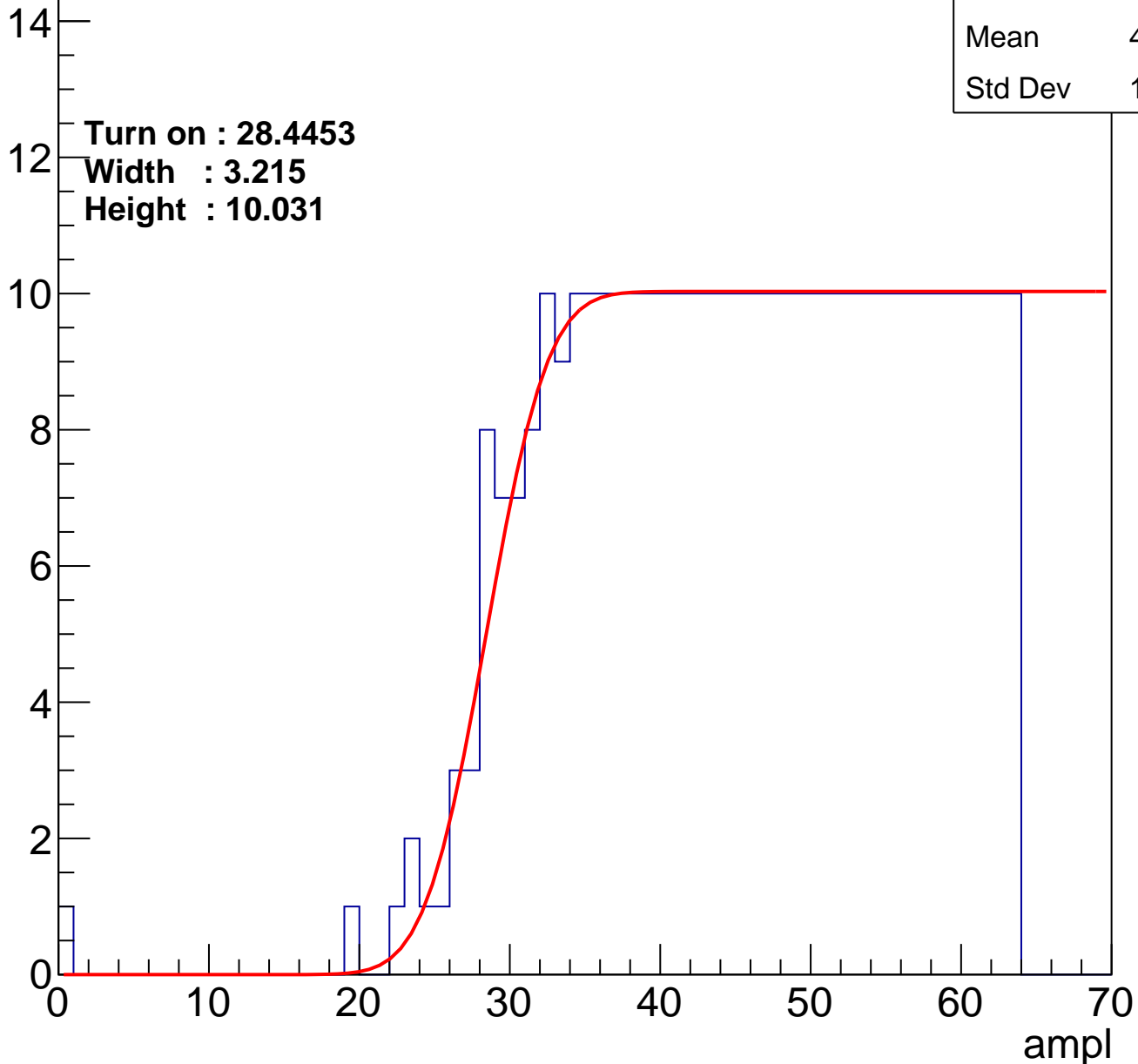
Entries	362
Mean	45.16
Std Dev	10.96

Turn on : 28.4453

Width : 3.215

Height : 10.031

Entry



B1L101S, U3-ch98

calib_packv5_042523_0143.root, FC#0, port D2

Entries	398
Mean	43.18
Std Dev	12.46

Turn on : 24.7926

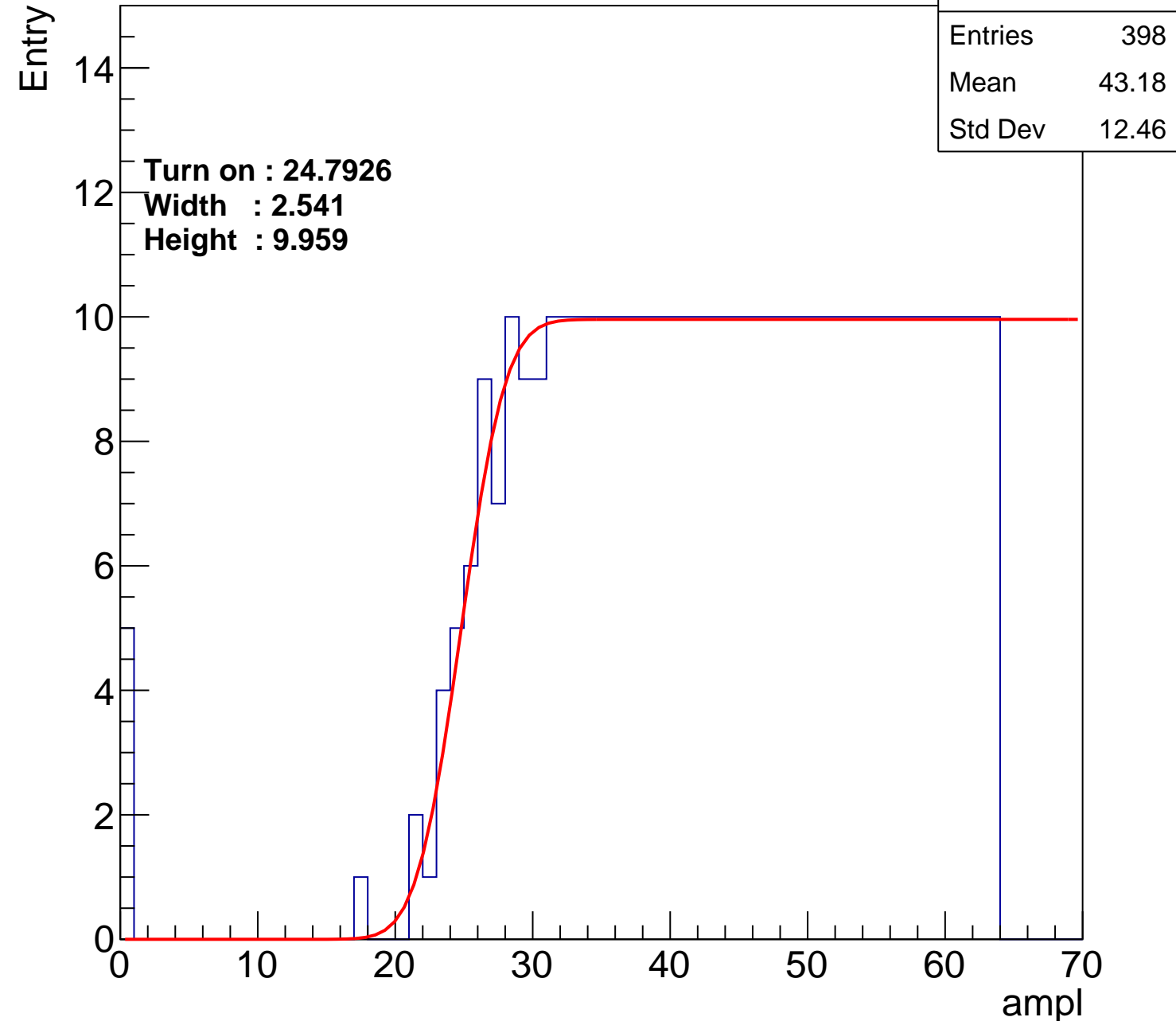
Width : 2.541

Height : 9.959

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch99

calib_packv5_042523_0143.root, FC#0, port D2

Entries	383
Mean	43.84
Std Dev	12.3

Turn on : 26.2998

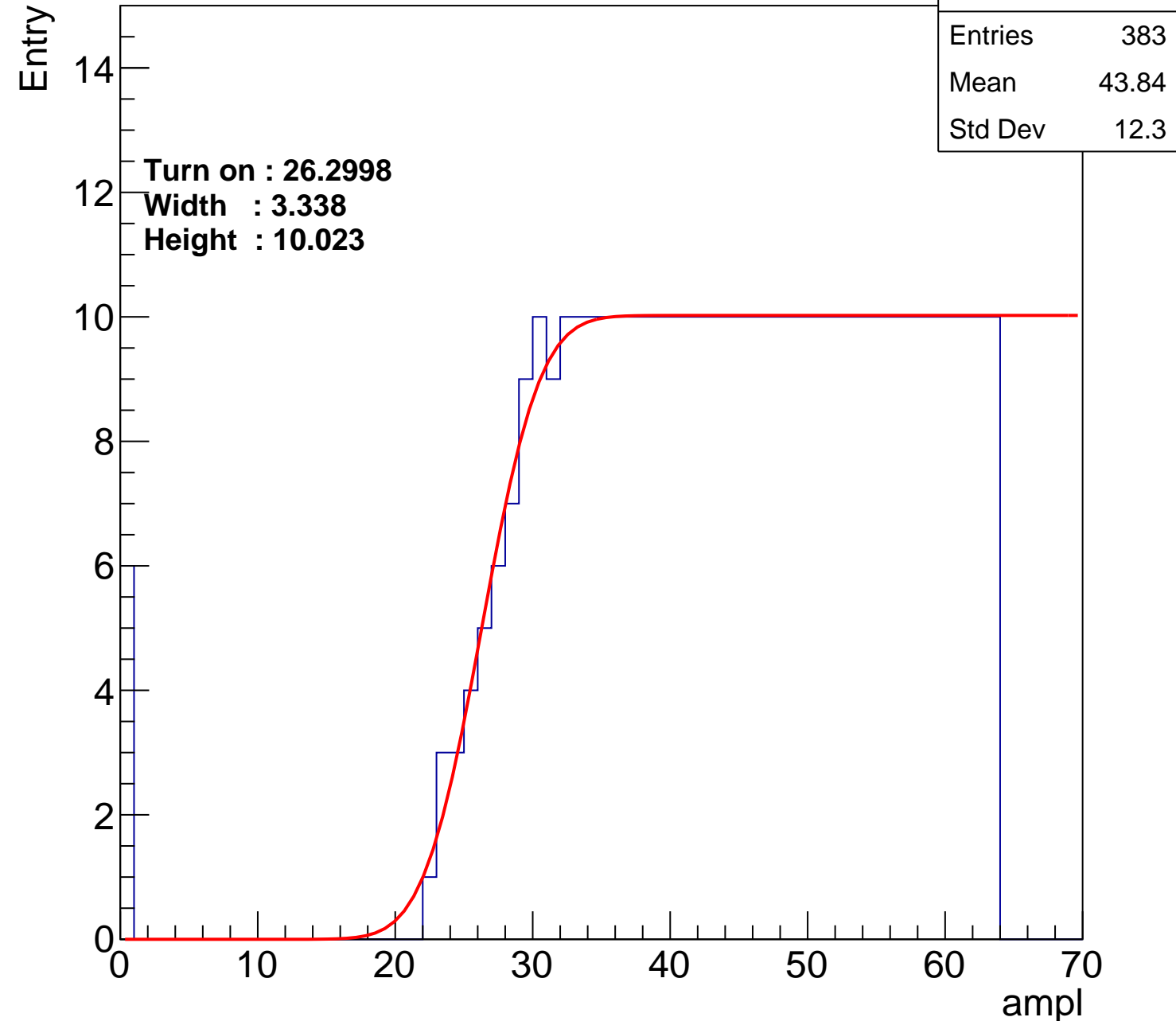
Width : 3.338

Height : 10.023

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch100

calib_packv5_042523_0143.root, FC#0, port D2

Entries	412
Mean	42.51
Std Dev	12.78

Turn on : 23.7181

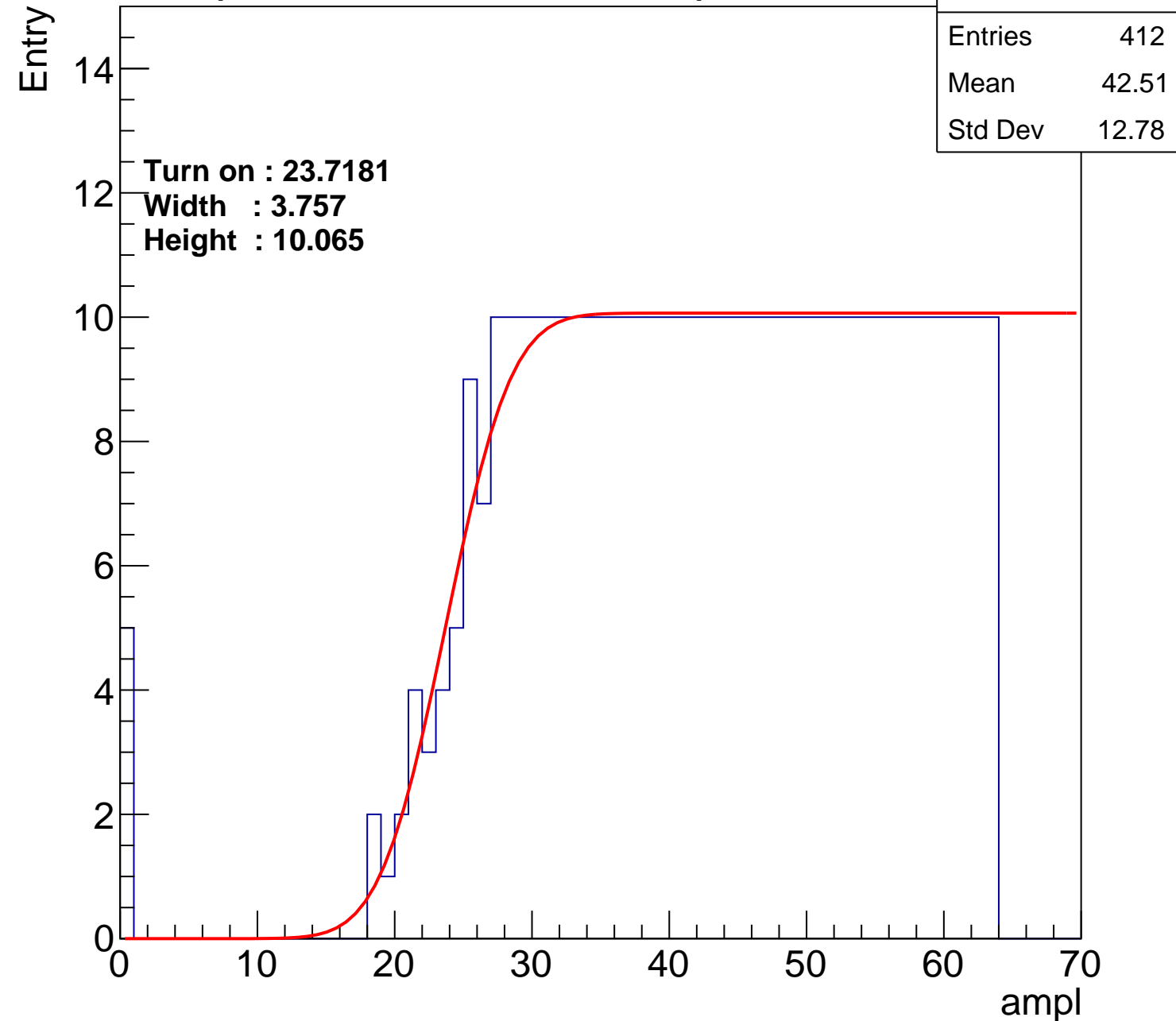
Width : 3.757

Height : 10.065

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch101

calib_packv5_042523_0143.root, FC#0, port D2

Entries	376
Mean	44.23
Std Dev	12

Turn on : 27.2698

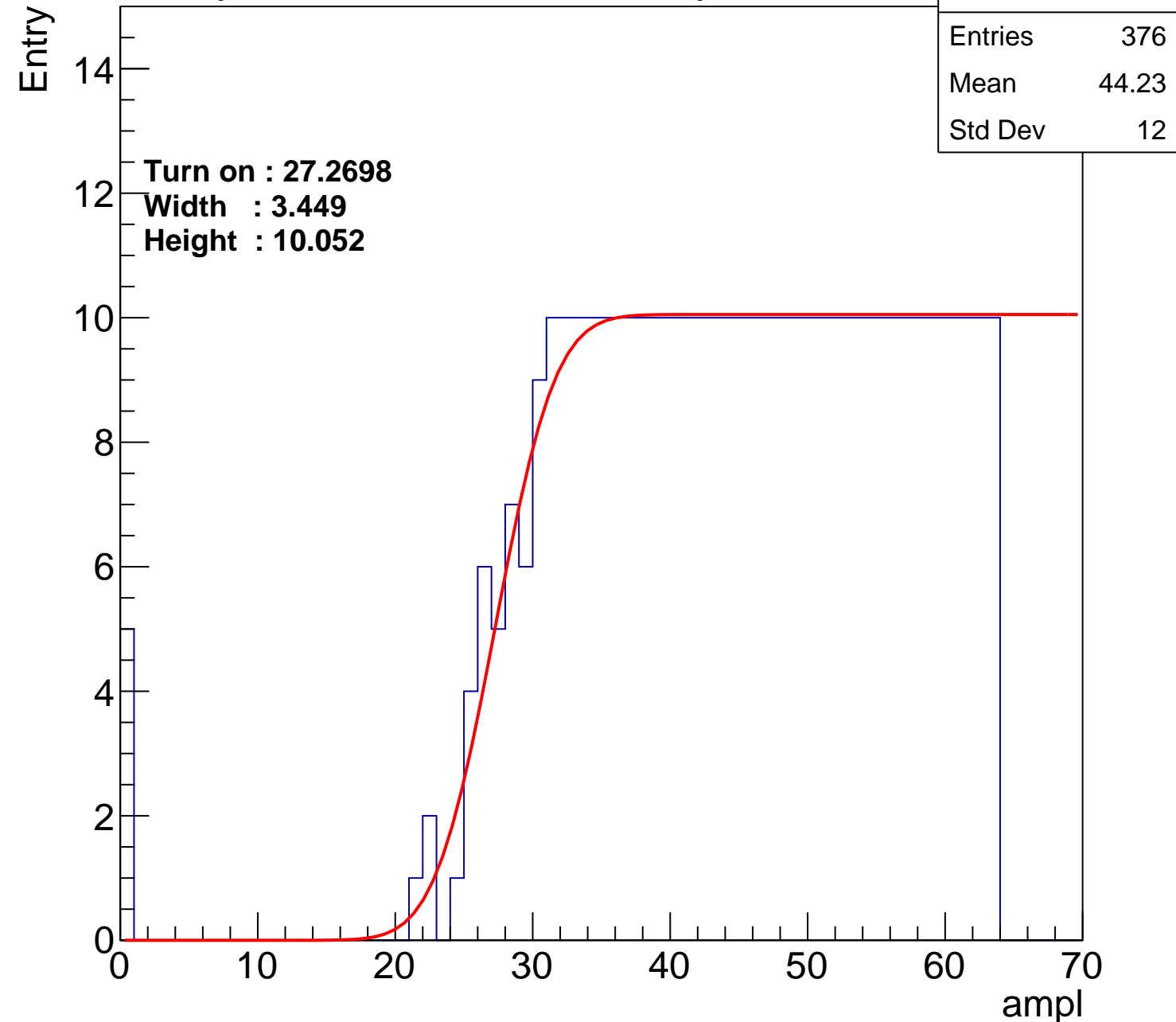
Width : 3.449

Height : 10.052

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch102

calib_packv5_042523_0143.root, FC#0, port D2

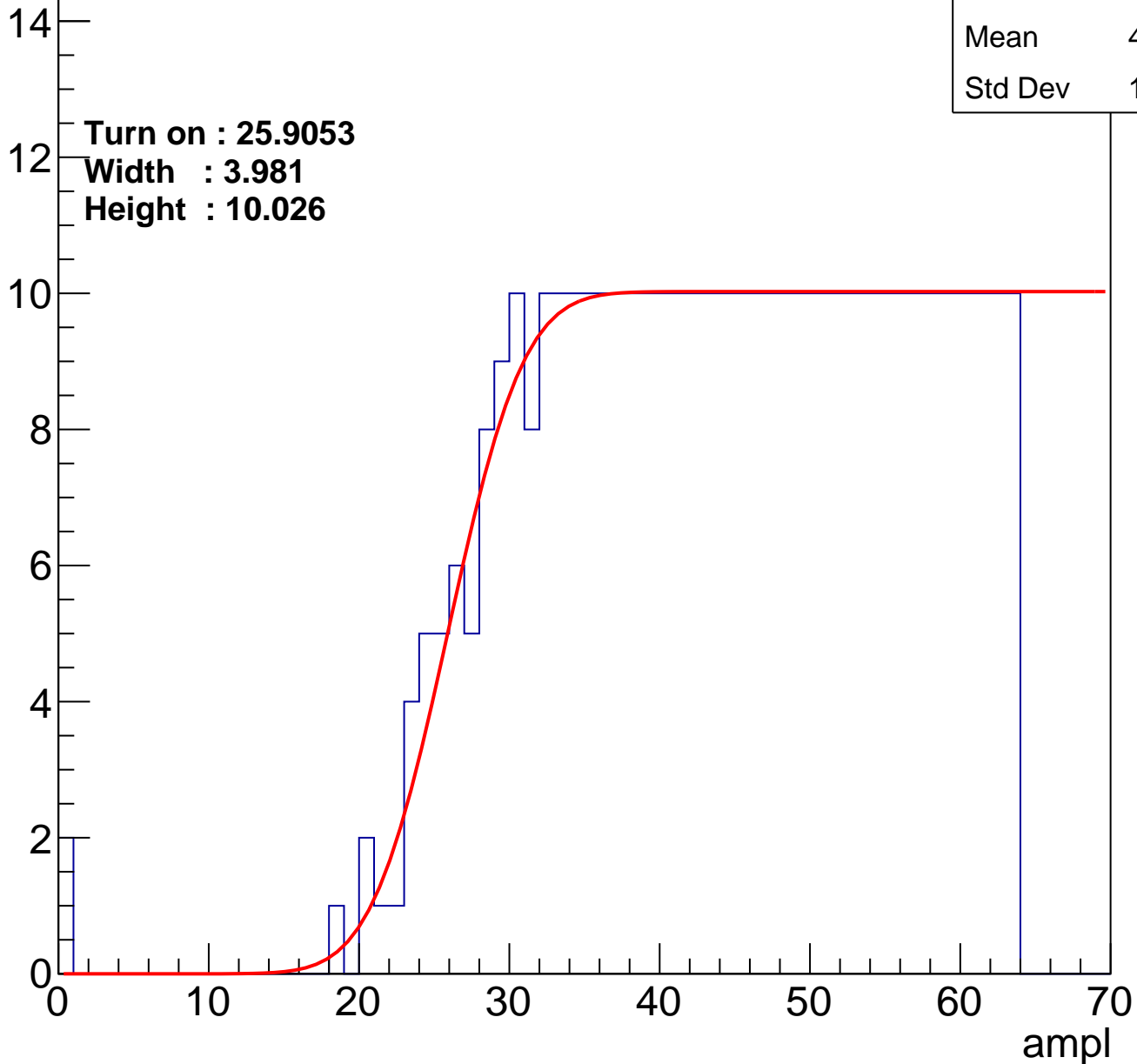
Entries	387
Mean	43.83
Std Dev	11.84

Turn on : 25.9053

Width : 3.981

Height : 10.026

Entry



B1L101S, U3-ch103

calib_packv5_042523_0143.root, FC#0, port D2

Entries	371
Mean	44.3
Std Dev	12.3

Turn on : 27.7103

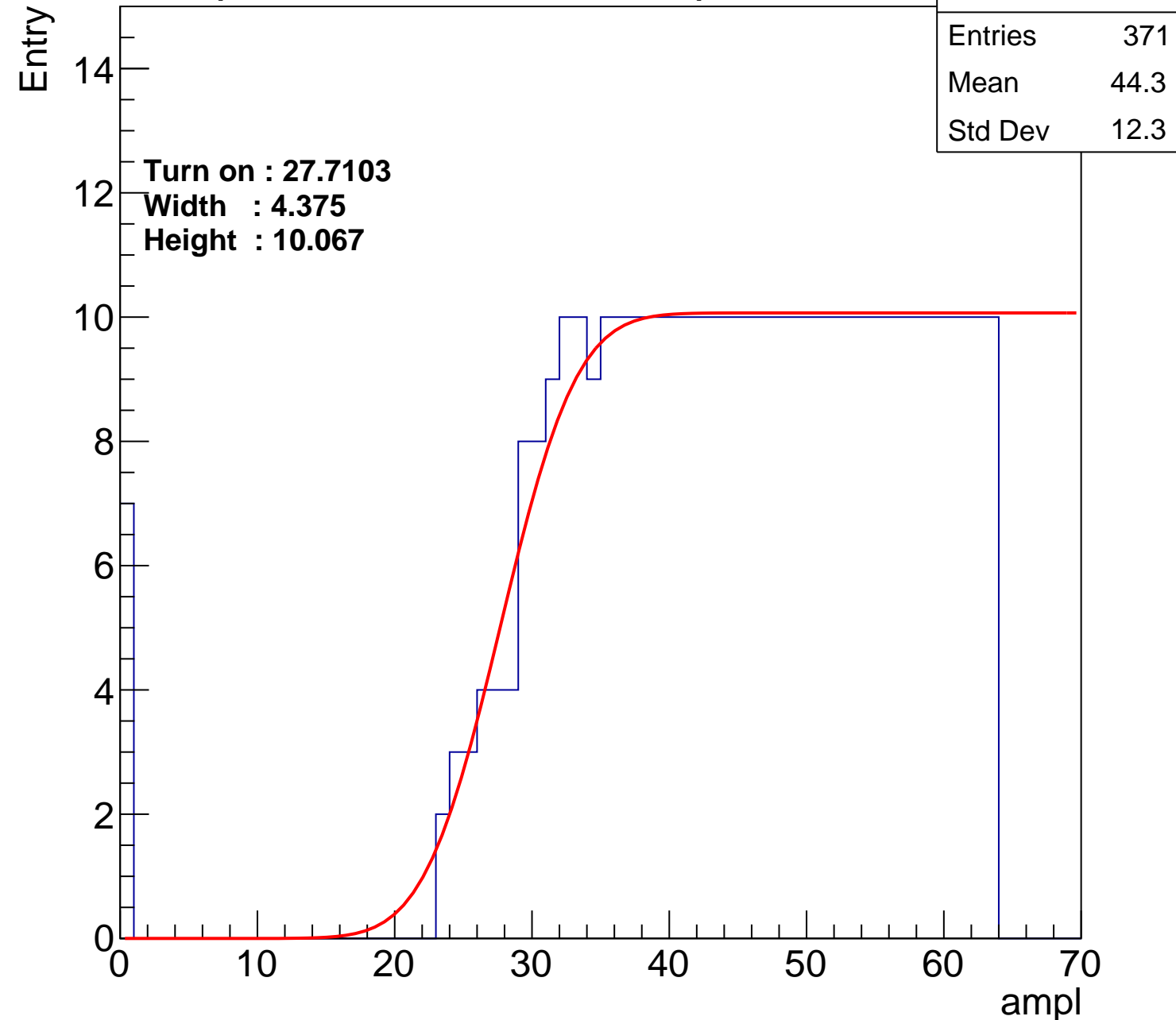
Width : 4.375

Height : 10.067

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch104

calib_packv5_042523_0143.root, FC#0, port D2

Entries	378
Mean	44.17
Std Dev	11.9

Turn on : 26.9635

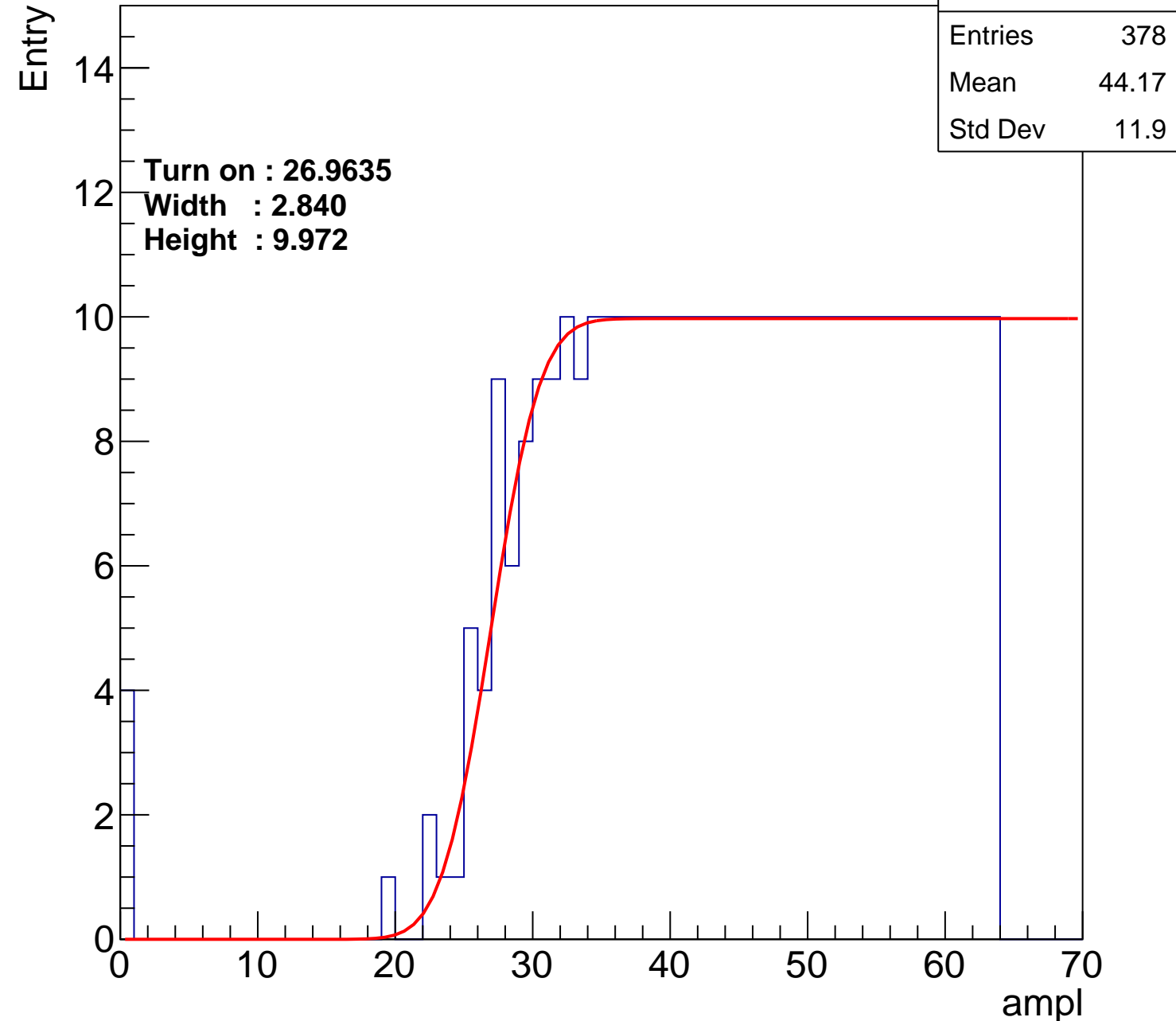
Width : 2.840

Height : 9.972

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch105

calib_packv5_042523_0143.root, FC#0, port D2

Entries	387
Mean	43.84
Std Dev	11.89

Turn on : 26.0827

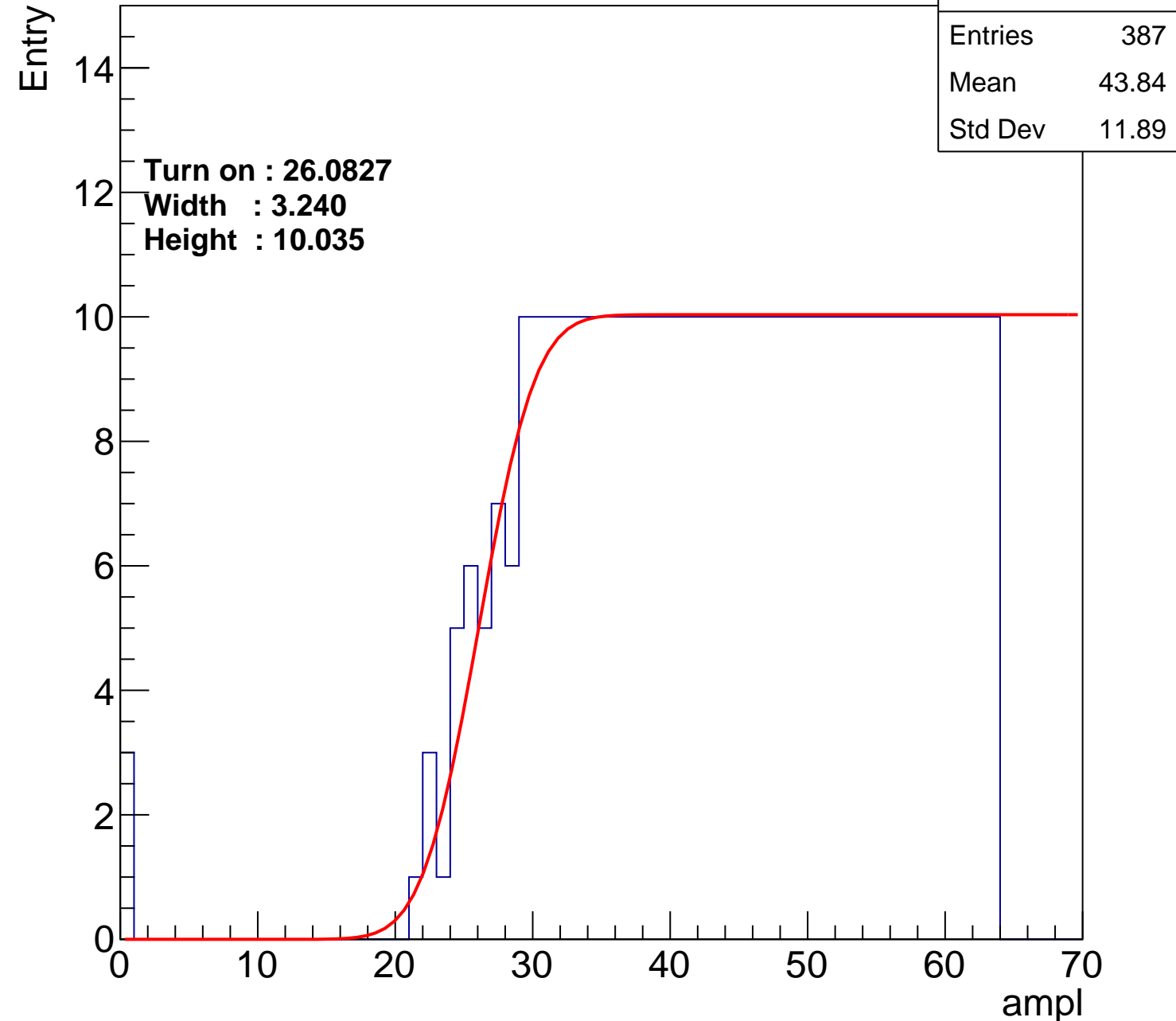
Width : 3.240

Height : 10.035

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch106

calib_packv5_042523_0143.root, FC#0, port D2

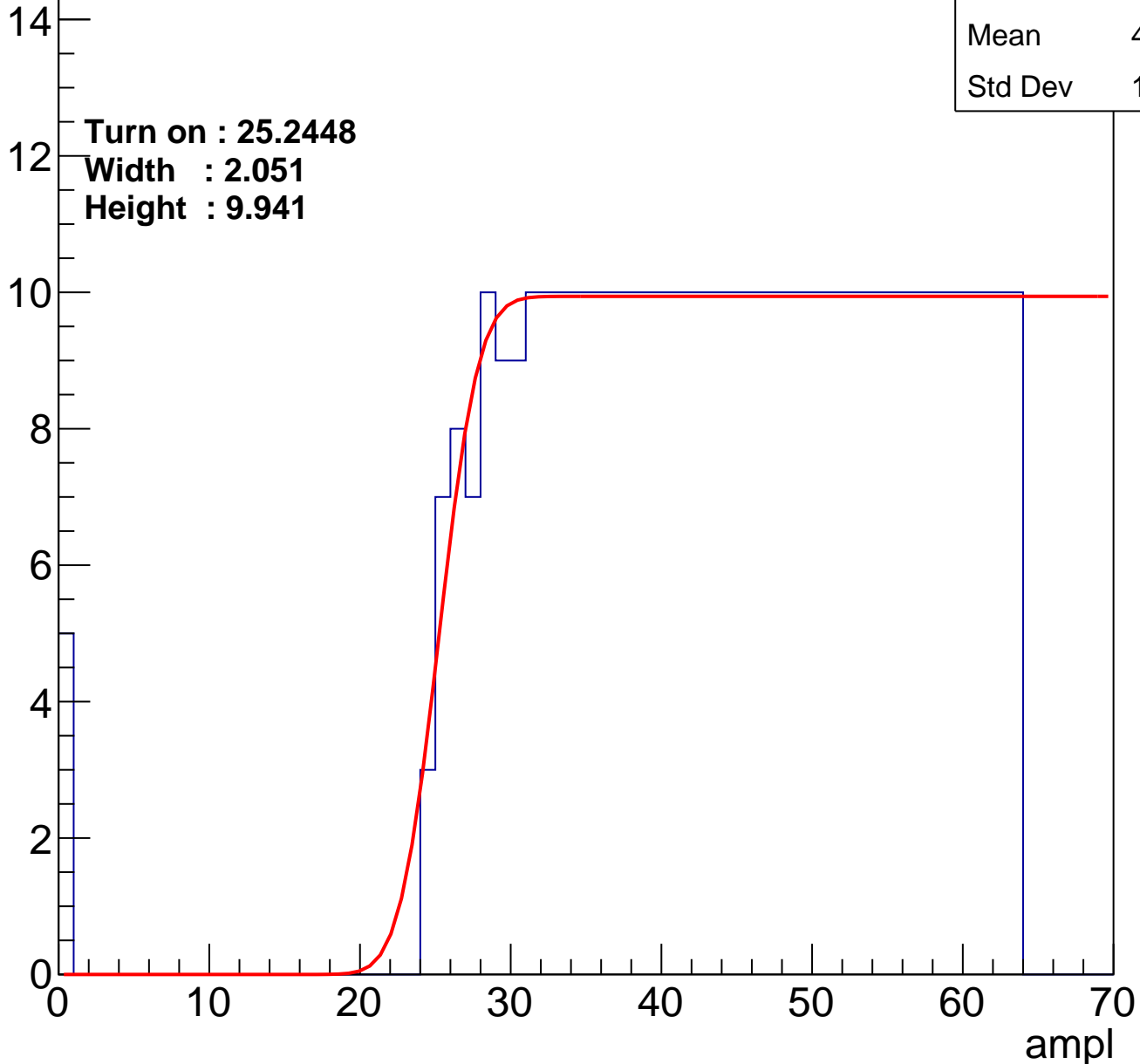
Entries	388
Mean	43.72
Std Dev	12.15

Turn on : 25.2448

Width : 2.051

Height : 9.941

Entry



B1L101S, U3-ch107

calib_packv5_042523_0143.root, FC#0, port D2

Entries	389
Mean	43.58
Std Dev	12.31

Turn on : 25.6179

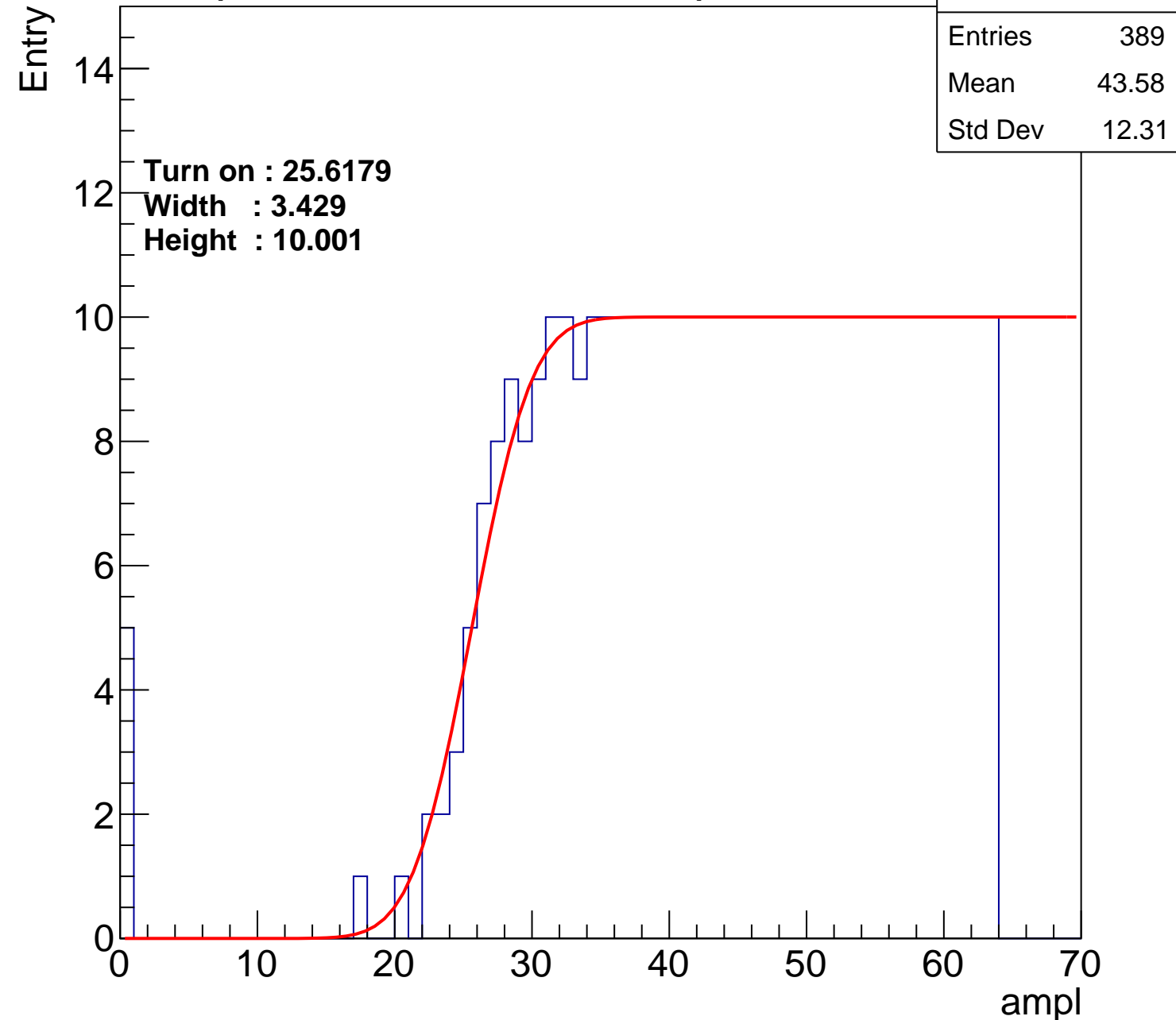
Width : 3.429

Height : 10.001

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch108

calib_packv5_042523_0143.root, FC#0, port D2

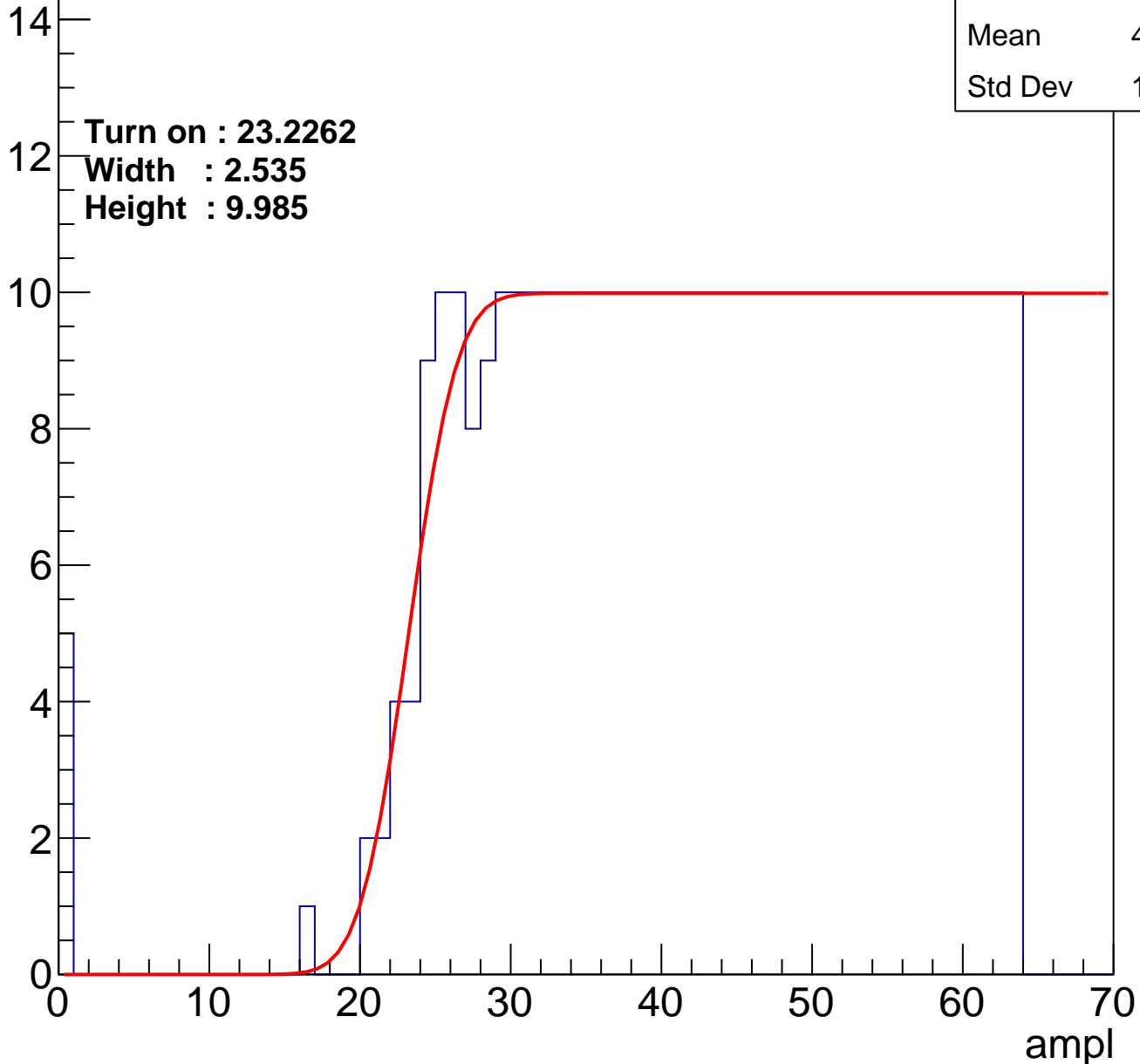
Entries	414
Mean	42.44
Std Dev	12.77

Turn on : 23.2262

Width : 2.535

Height : 9.985

Entry



B1L101S, U3-ch109

calib_packv5_042523_0143.root, FC#0, port D2

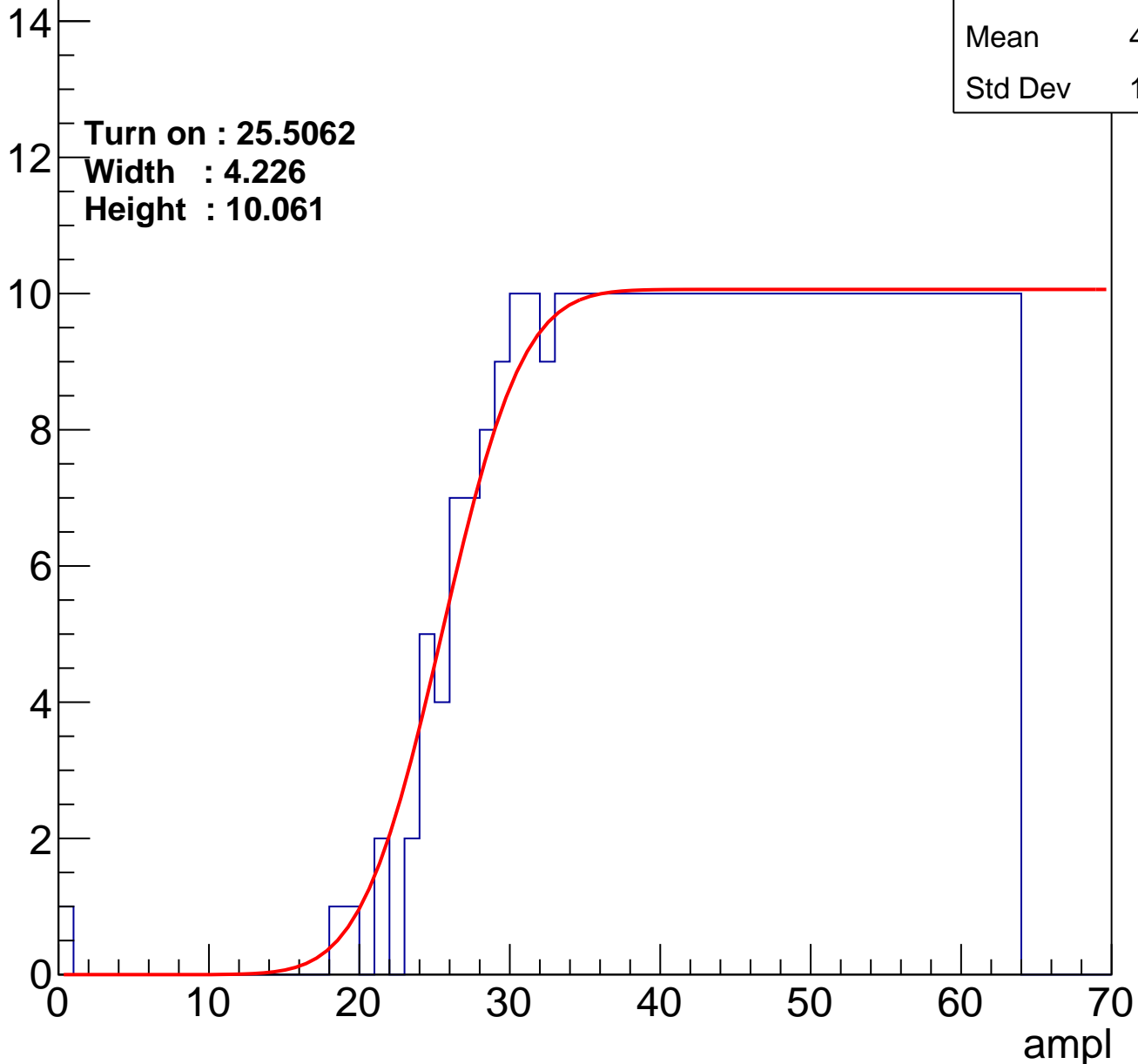
Entries	386
Mean	43.99
Std Dev	11.57

Turn on : 25.5062

Width : 4.226

Height : 10.061

Entry



B1L101S, U3-ch110

calib_packv5_042523_0143.root, FC#0, port D2

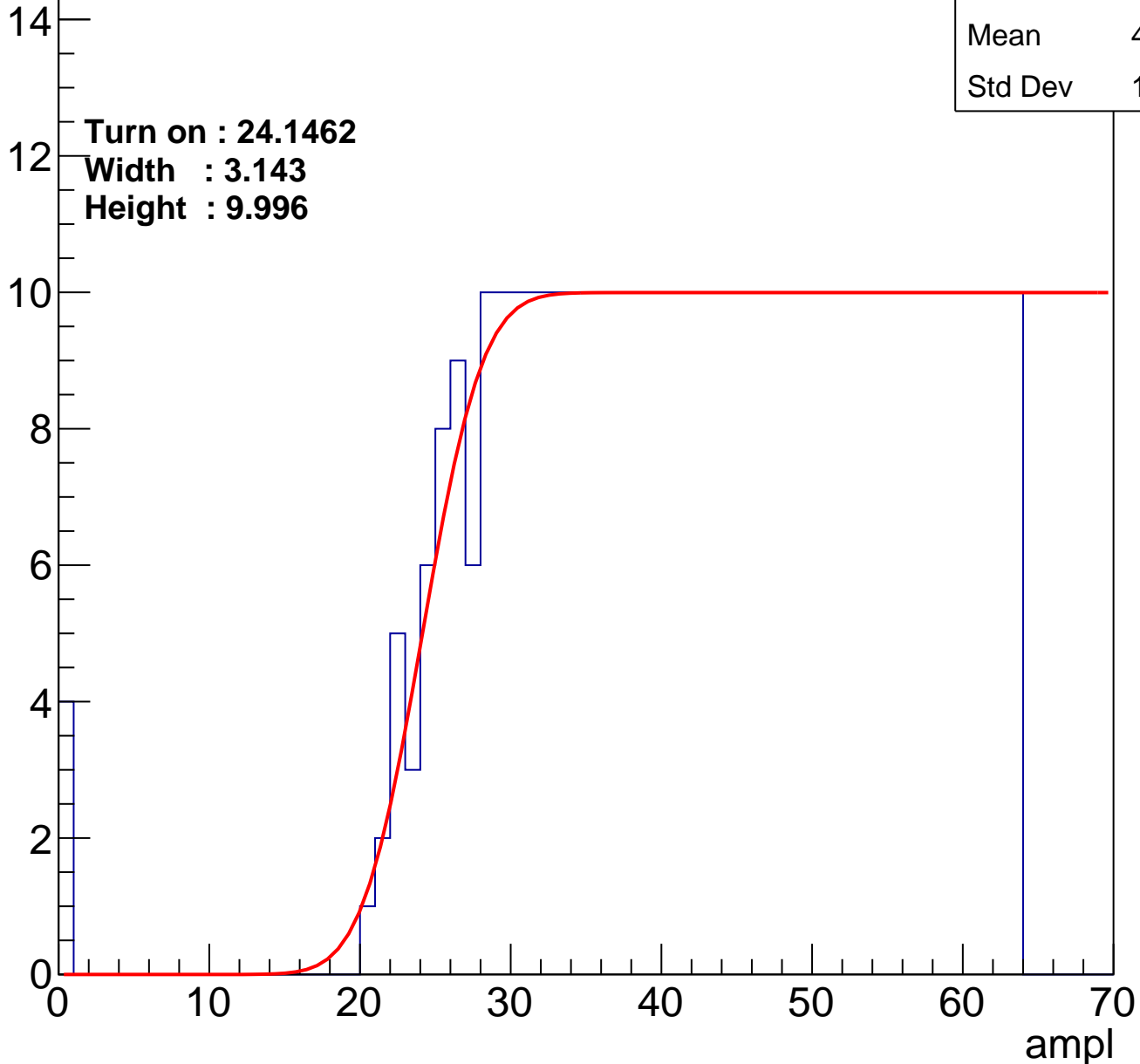
Entries	404
Mean	42.97
Std Dev	12.42

Turn on : 24.1462

Width : 3.143

Height : 9.996

Entry



B1L101S, U3-ch111

calib_packv5_042523_0143.root, FC#0, port D2

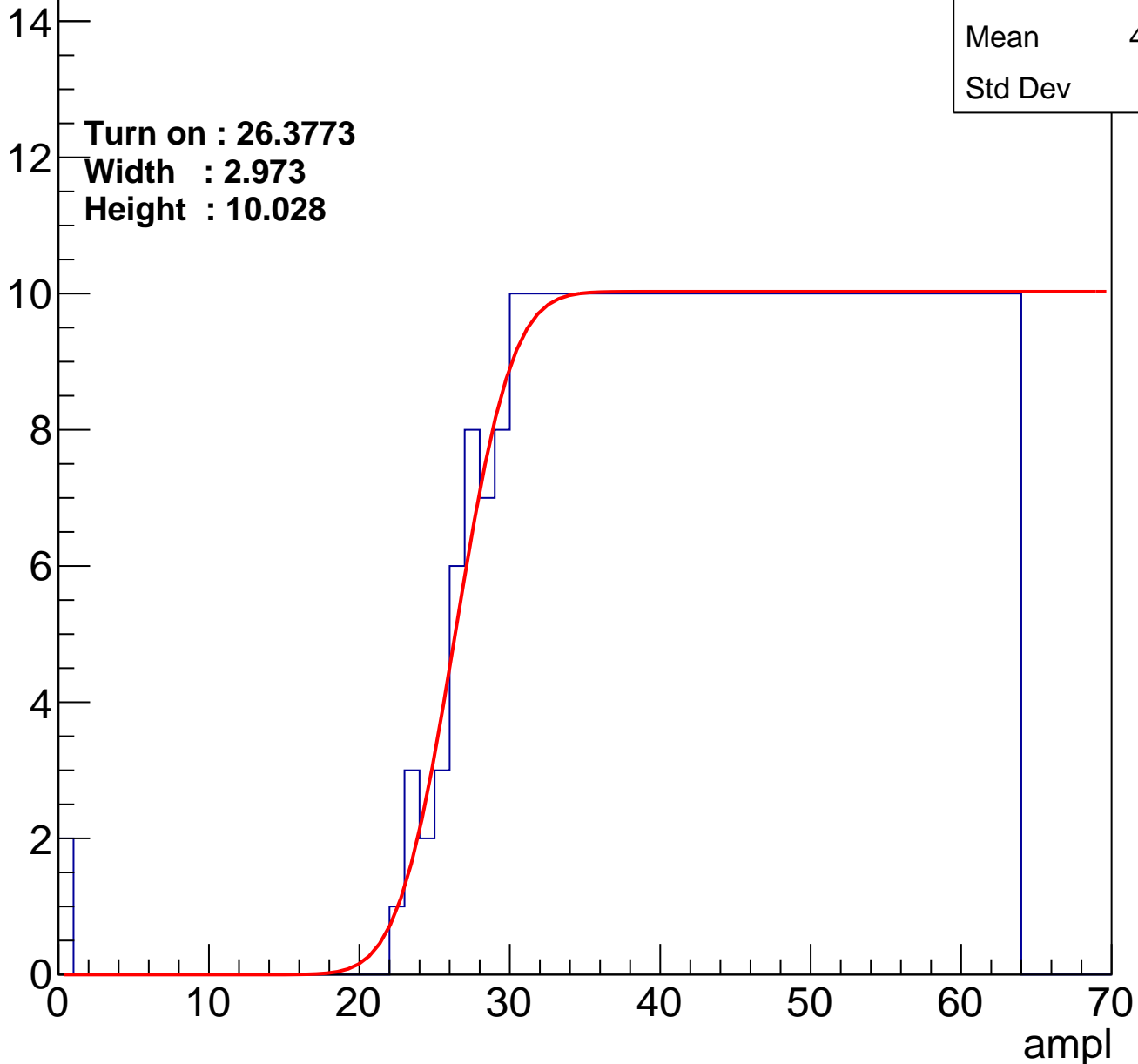
Entries	380
Mean	44.27
Std Dev	11.5

Turn on : 26.3773

Width : 2.973

Height : 10.028

Entry



B1L101S, U3-ch112

calib_packv5_042523_0143.root, FC#0, port D2

Entries	389
Mean	43.63
Std Dev	12.23

Turn on : 25.6801

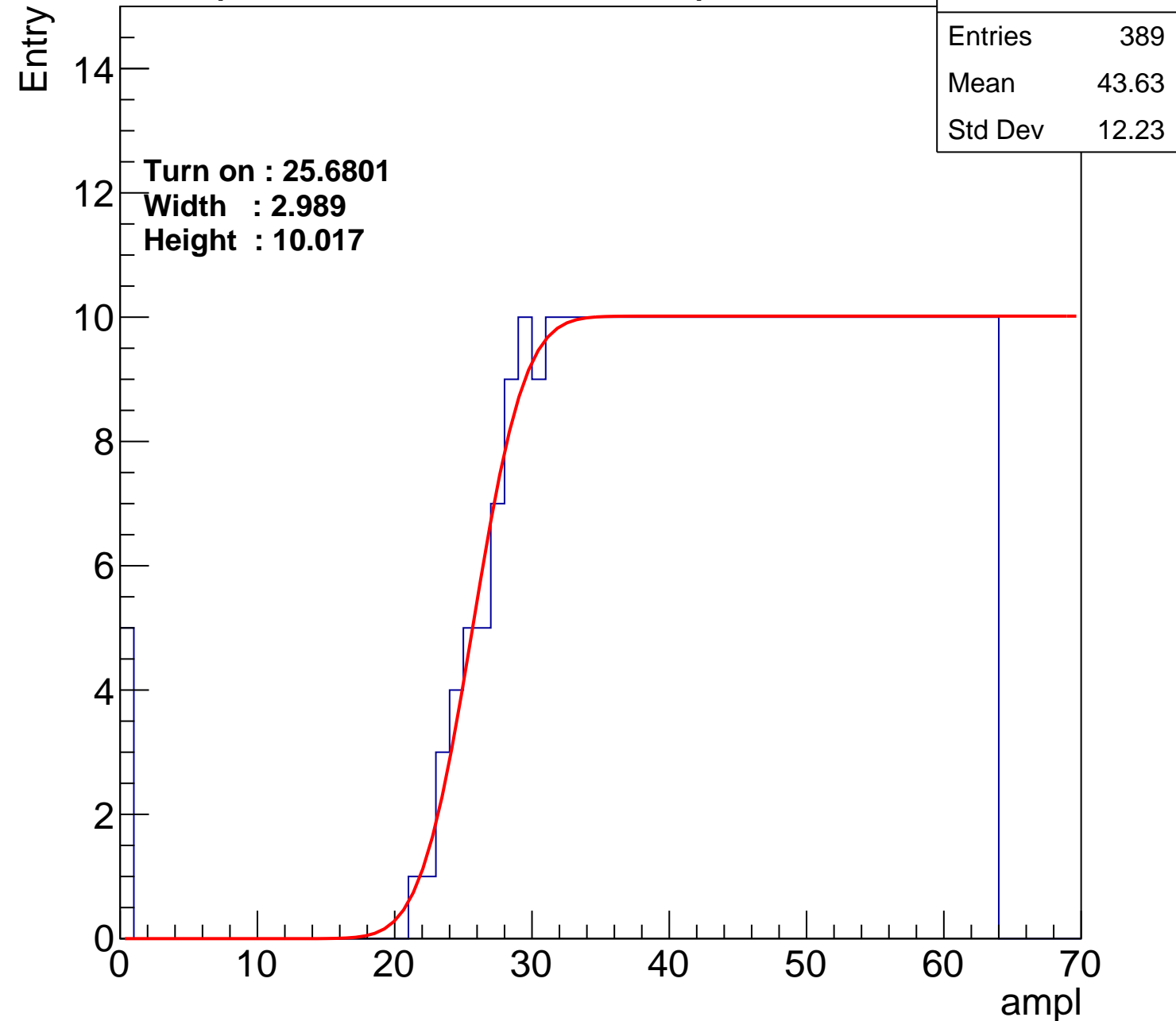
Width : 2.989

Height : 10.017

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch113

calib_packv5_042523_0143.root, FC#0, port D2

Entries	353
Mean	45.36
Std Dev	11.48

Turn on : 29.4186

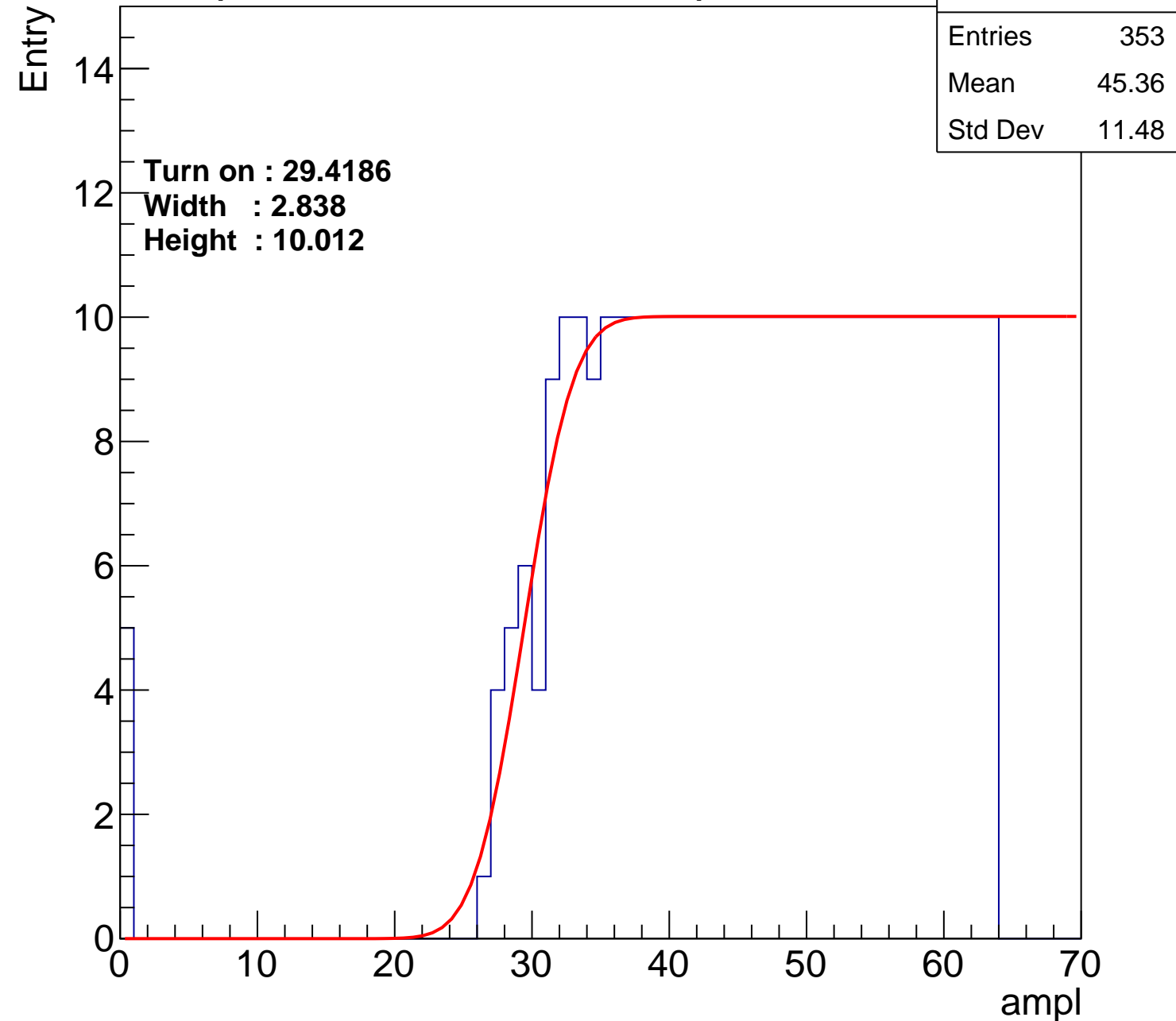
Width : 2.838

Height : 10.012

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch114

calib_packv5_042523_0143.root, FC#0, port D2

Entries	400
Mean	42.88
Std Dev	13.04

Turn on : 24.8261

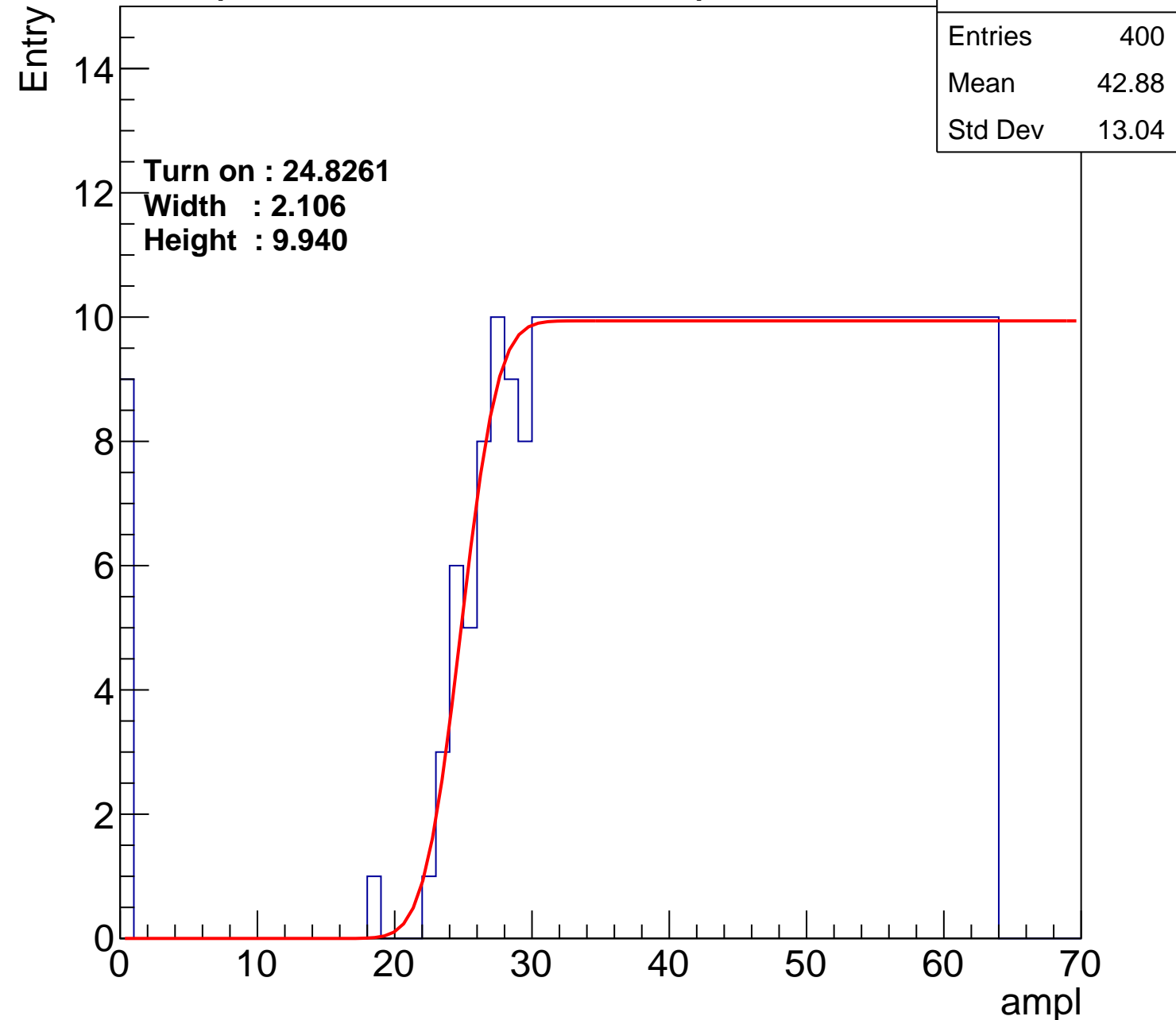
Width : 2.106

Height : 9.940

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch115

calib_packv5_042523_0143.root, FC#0, port D2

Entries	390
Mean	43.61
Std Dev	12.15

Turn on : 25.3290

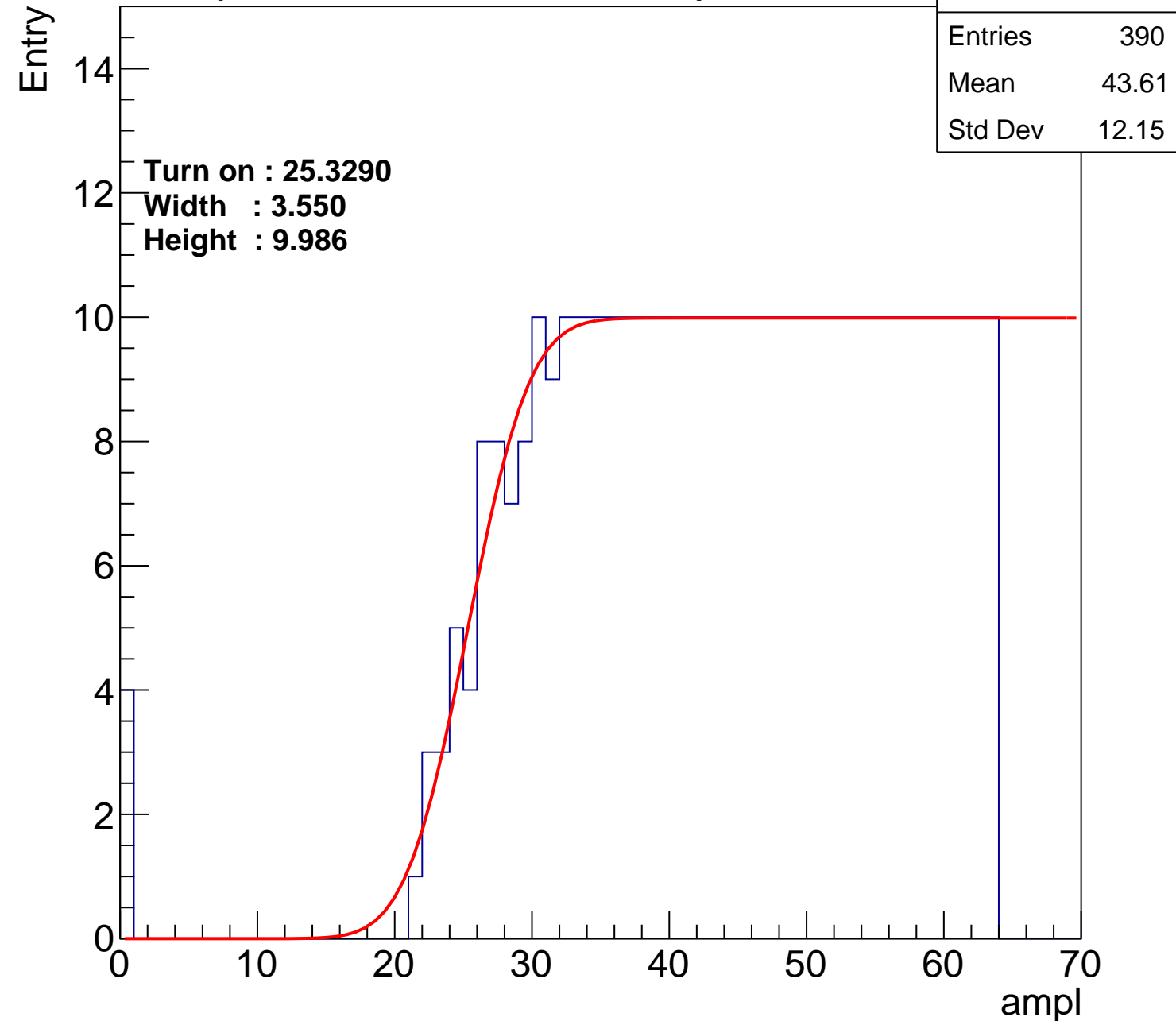
Width : 3.550

Height : 9.986

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch116

calib_packv5_042523_0143.root, FC#0, port D2

Entries	385
Mean	43.98
Std Dev	11.69

Turn on : 25.7724

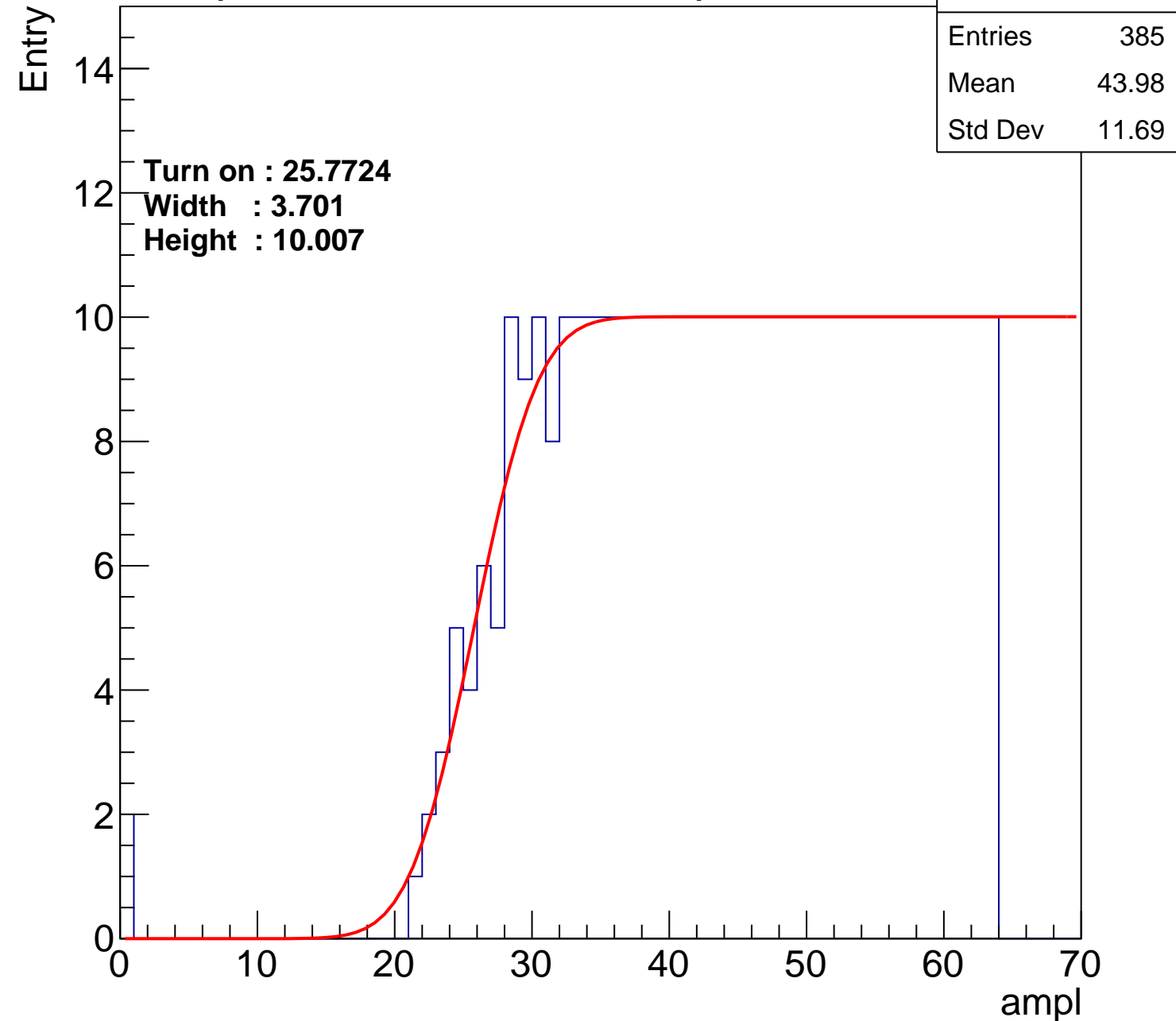
Width : 3.701

Height : 10.007

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch117

calib_packv5_042523_0143.root, FC#0, port D2

Entries	377
Mean	44.46
Std Dev	11.4

Turn on : 26.4560

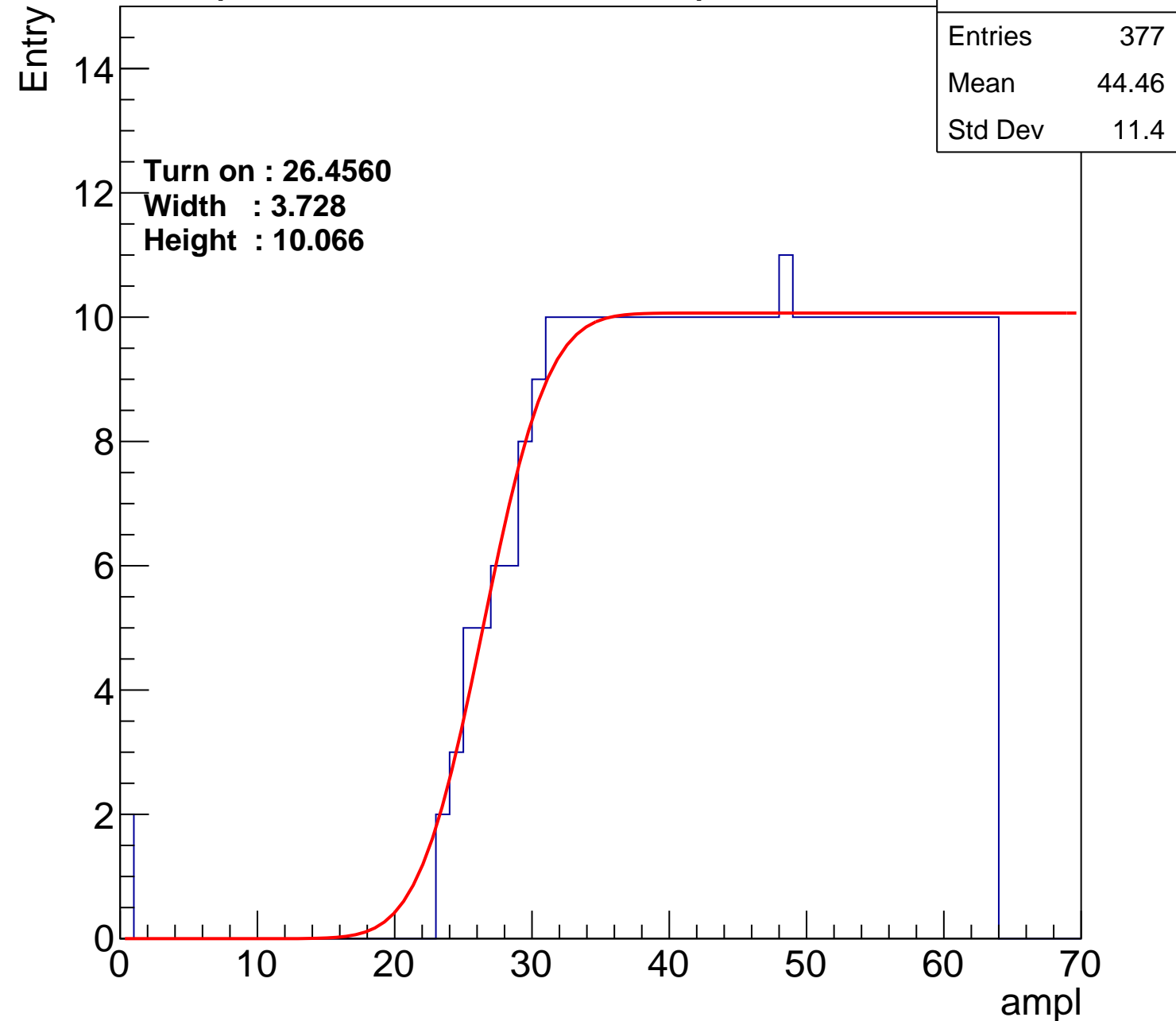
Width : 3.728

Height : 10.066

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch118

calib_packv5_042523_0143.root, FC#0, port D2

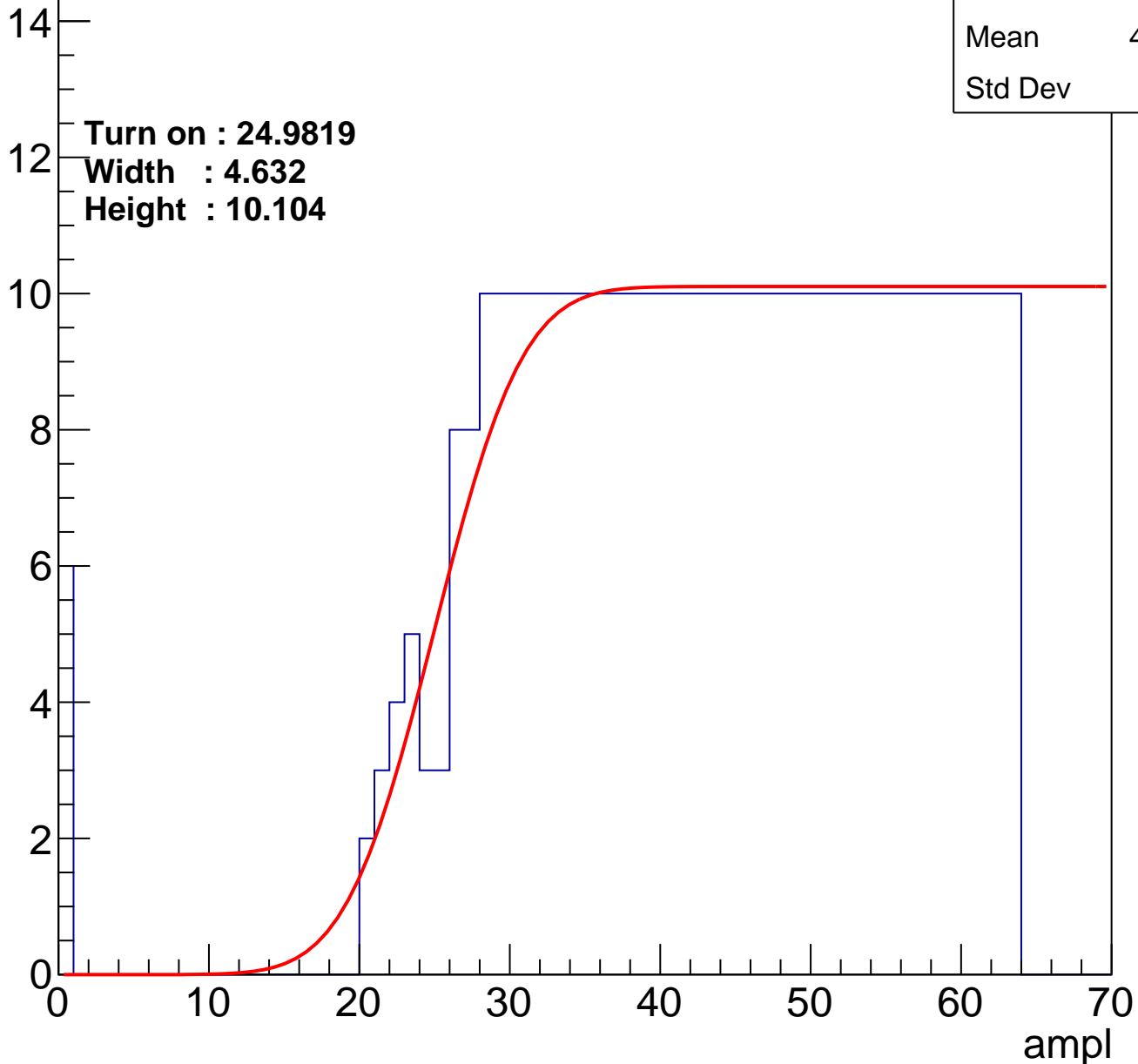
Entries	402
Mean	42.93
Std Dev	12.7

Turn on : 24.9819

Width : 4.632

Height : 10.104

Entry



B1L101S, U3-ch119

calib_packv5_042523_0143.root, FC#0, port D2

Entries	401
Mean	42.99
Std Dev	12.66

Turn on : 24.8634

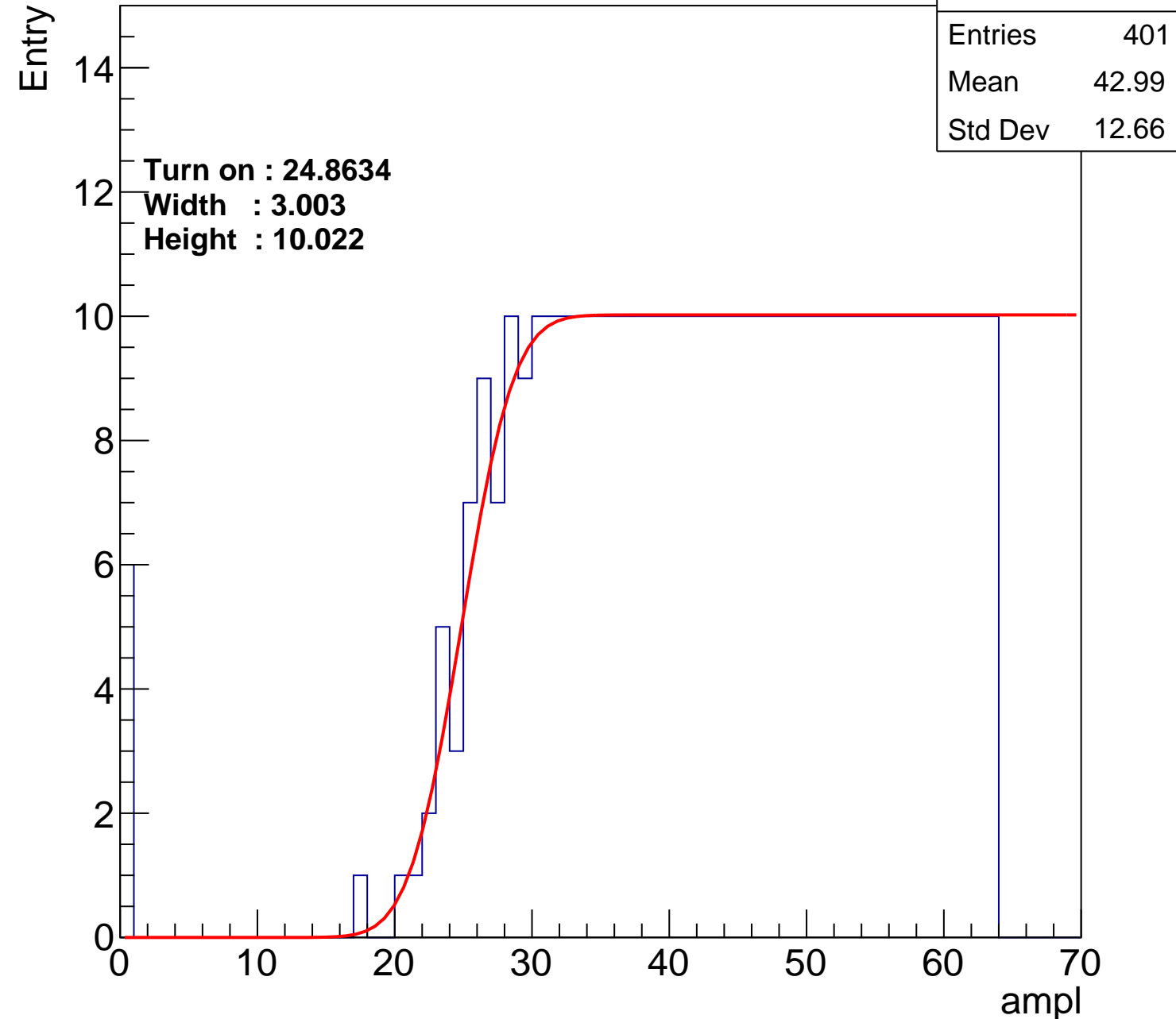
Width : 3.003

Height : 10.022

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch120

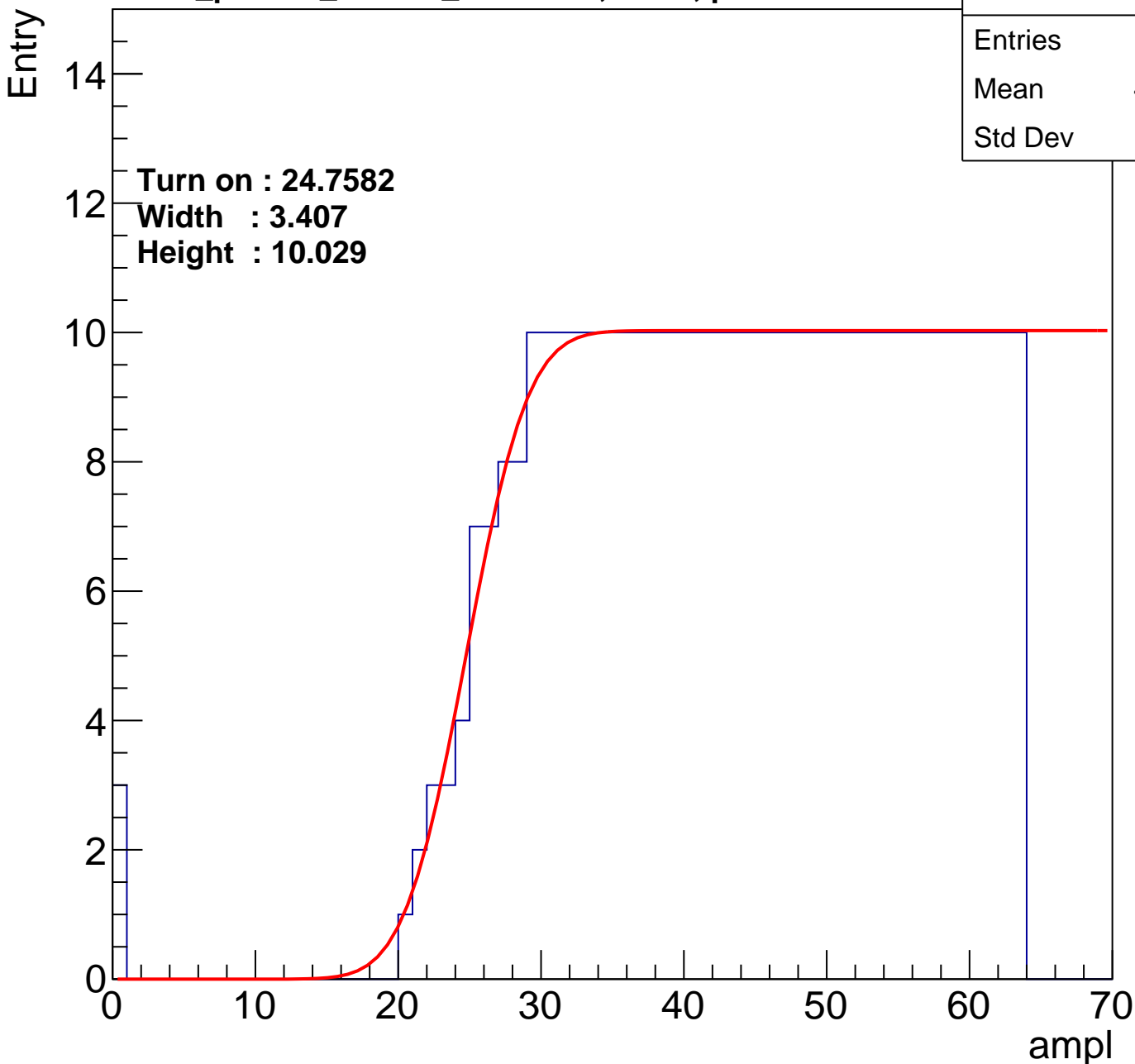
calib_packv5_042523_0143.root, FC#0, port D2

Entries	396
Mean	43.41
Std Dev	12.1

Turn on : 24.7582

Width : 3.407

Height : 10.029



B1L101S, U3-ch121

calib_packv5_042523_0143.root, FC#0, port D2

Entries	390
Mean	43.75
Std Dev	11.87

Turn on : 25.2108

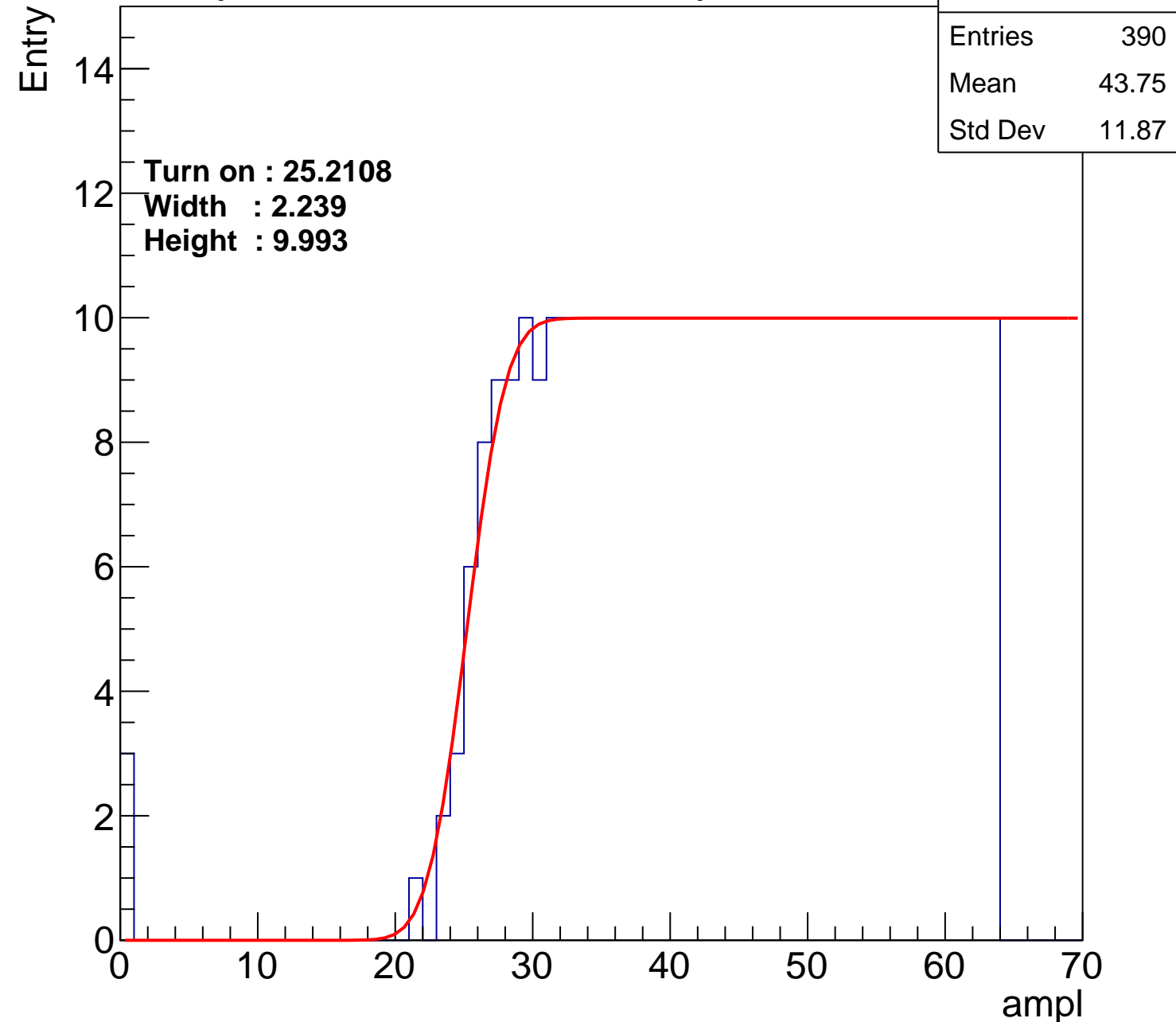
Width : 2.239

Height : 9.993

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch122

calib_packv5_042523_0143.root, FC#0, port D2

Entries	384
Mean	43.99
Std Dev	11.81

Turn on : 26.0798

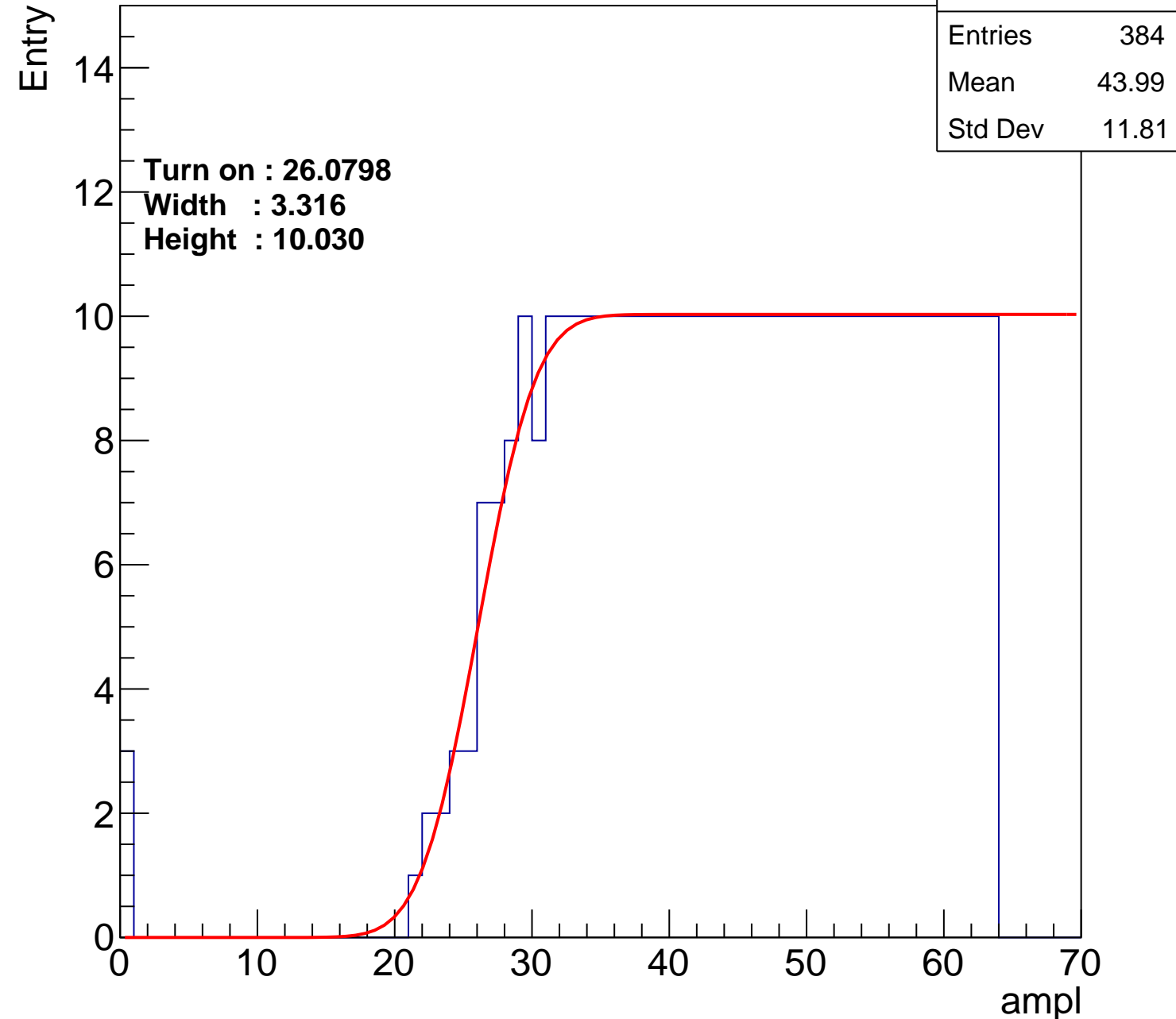
Width : 3.316

Height : 10.030

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch123

calib_packv5_042523_0143.root, FC#0, port D2

Entries	389
Mean	43.71
Std Dev	12.13

Turn on : 25.9151

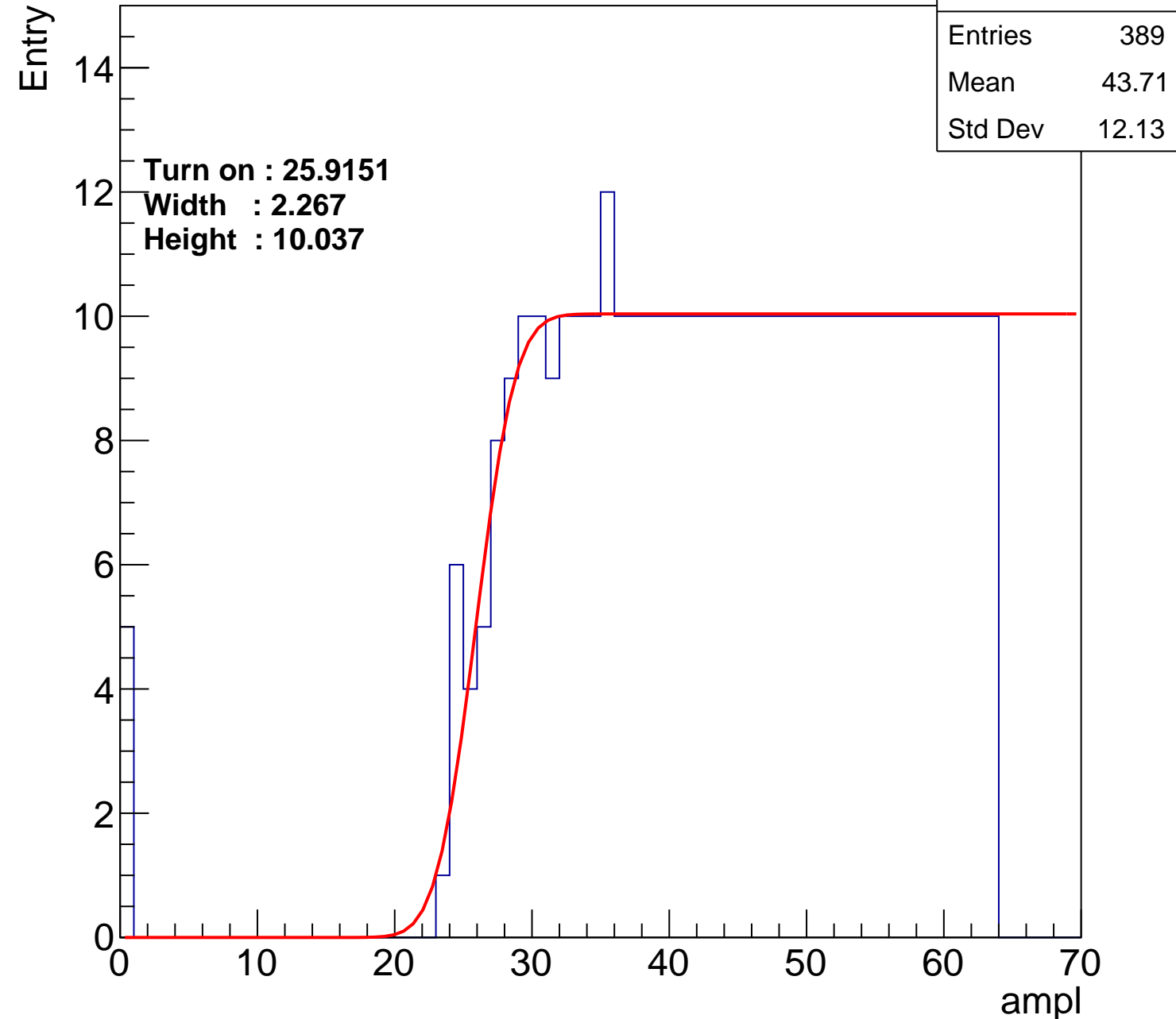
Width : 2.267

Height : 10.037

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch124

calib_packv5_042523_0143.root, FC#0, port D2

Entries	406
Mean	42.92
Std Dev	12.34

Turn on : 23.8854

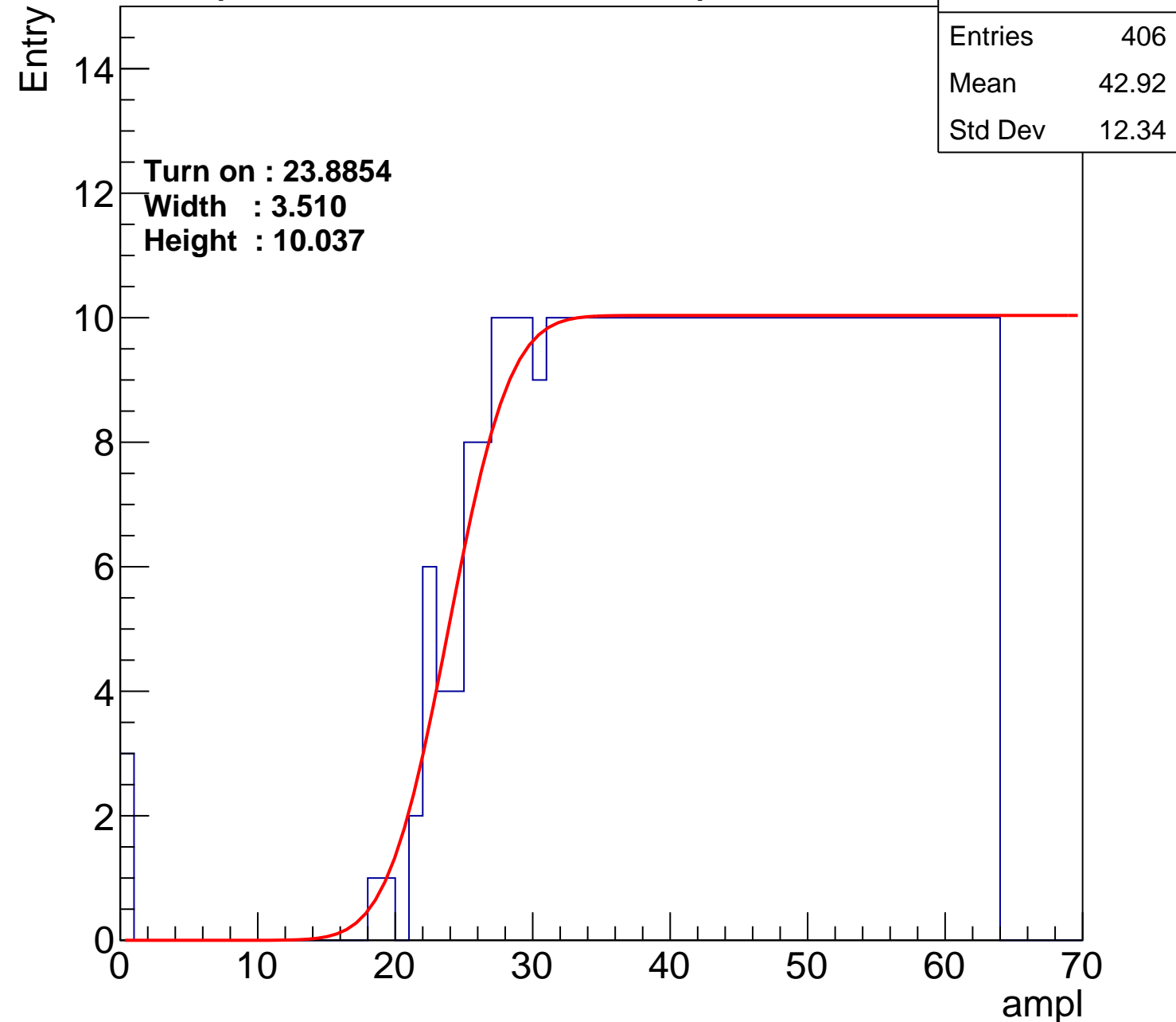
Width : 3.510

Height : 10.037

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch125

calib_packv5_042523_0143.root, FC#0, port D2

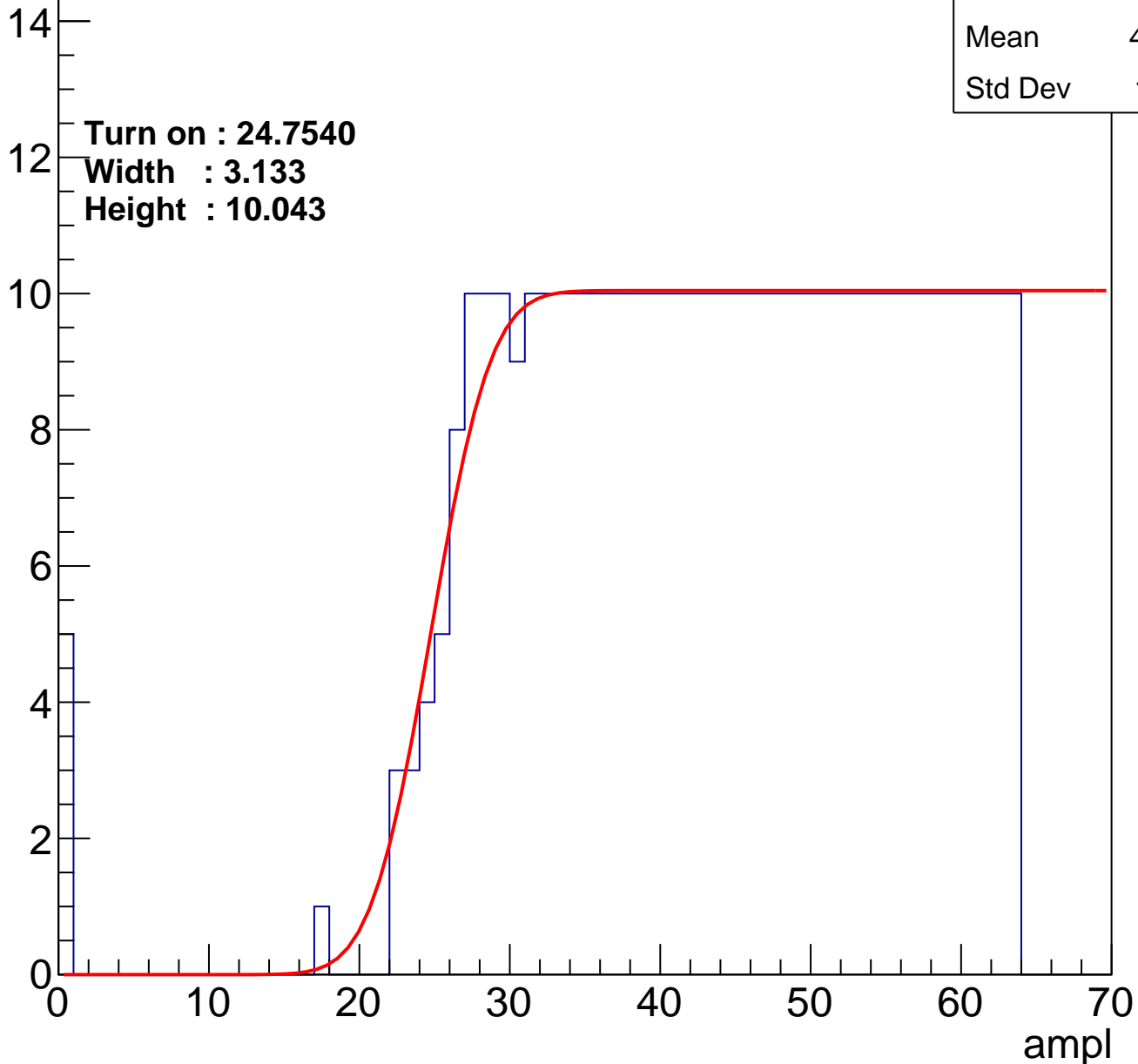
Entries	398
Mean	43.22
Std Dev	12.41

Turn on : 24.7540

Width : 3.133

Height : 10.043

Entry



B1L101S, U3-ch126

calib_packv5_042523_0143.root, FC#0, port D2

Entries	396
Mean	43.28
Std Dev	12.35

Turn on : 25.0948

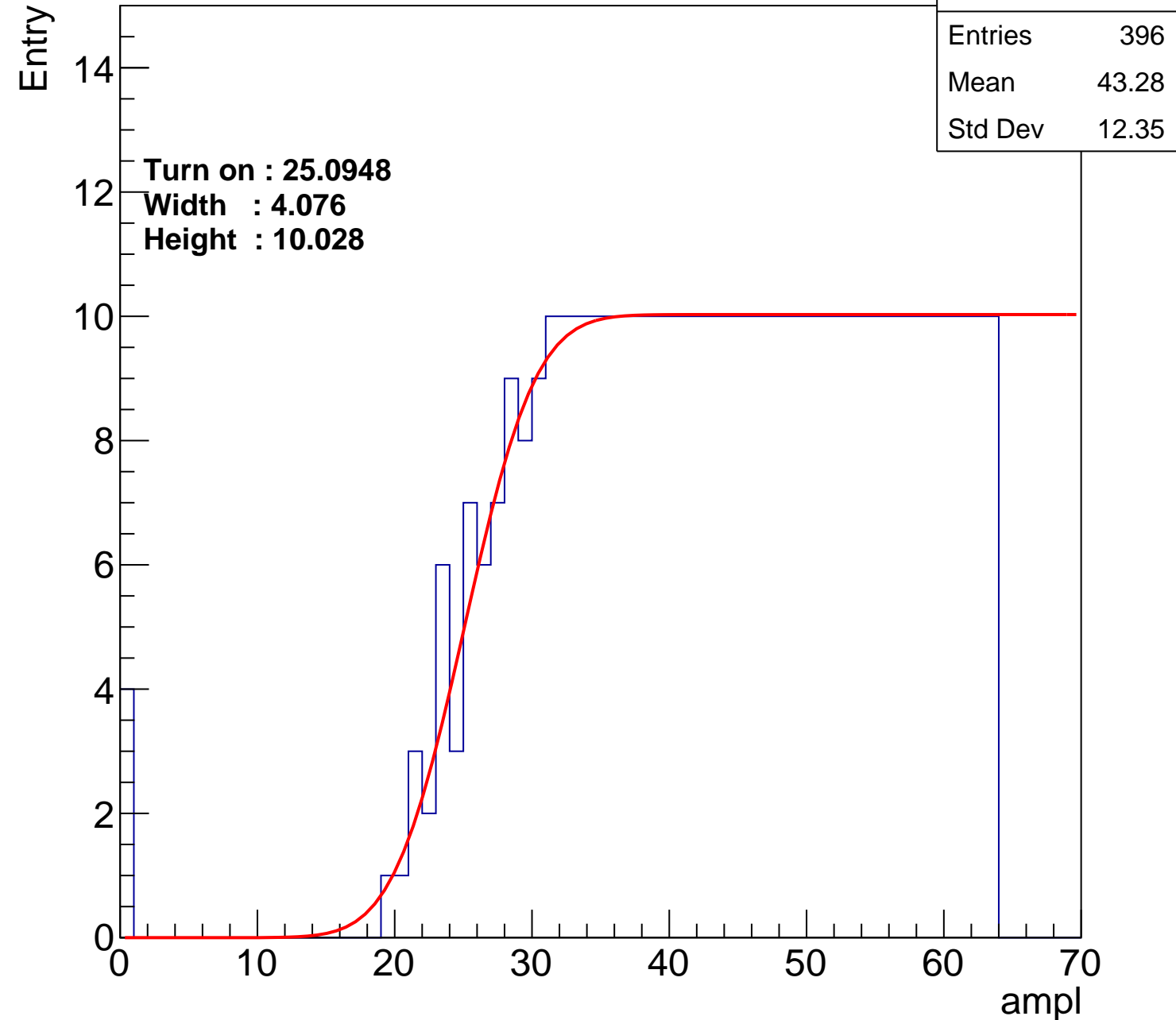
Width : 4.076

Height : 10.028

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch127

calib_packv5_042523_0143.root, FC#0, port D2

Entries	383
Mean	43.97
Std Dev	11.97

Turn on : 26.6531

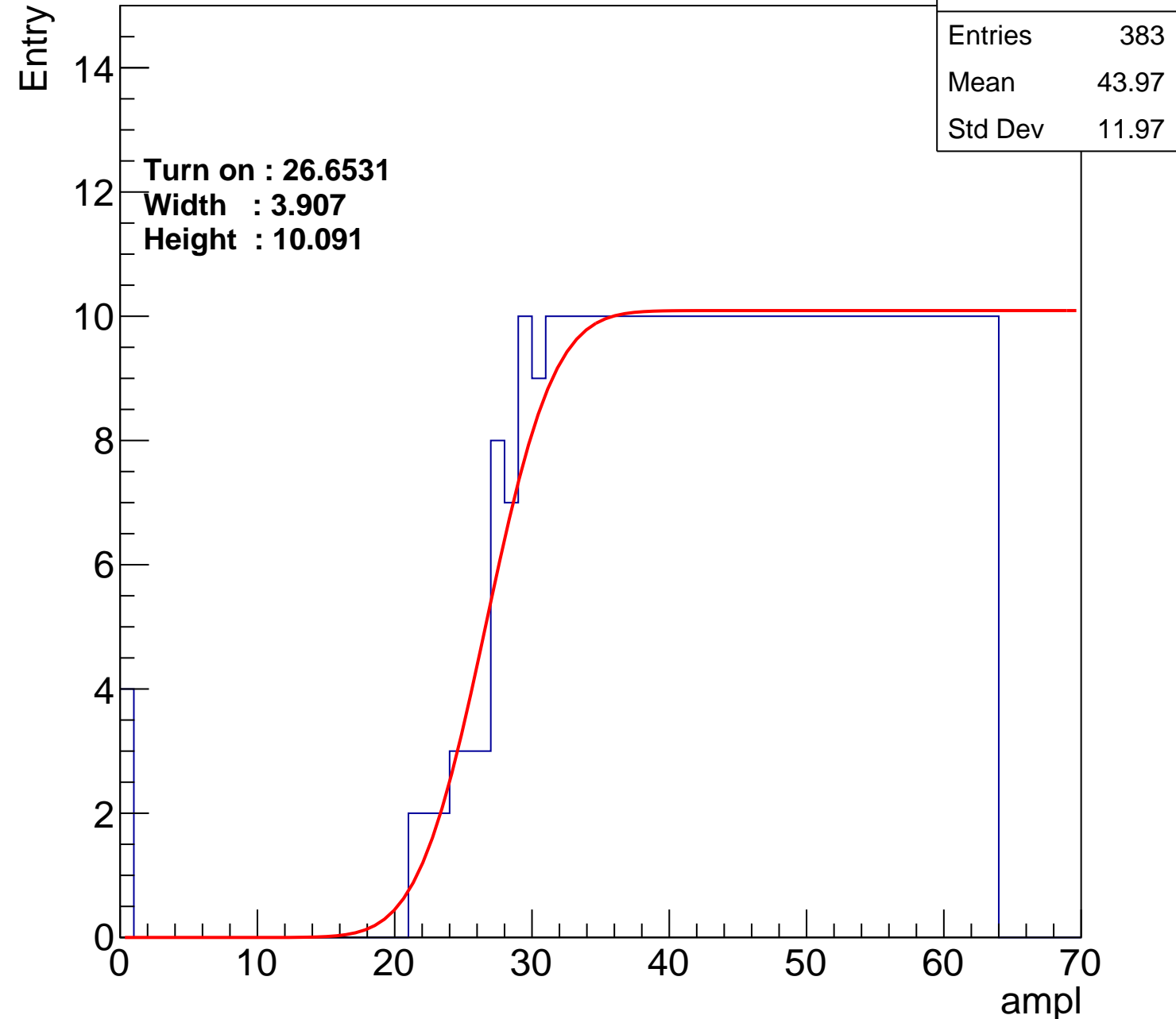
Width : 3.907

Height : 10.091

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U3-ch127

calib_packv5_042523_0143.root, FC#0, port D2

Entries	383
Mean	43.97
Std Dev	11.97

Turn on : 26.6531

Width : 3.907

Height : 10.091

Entry

14
12
10
8
6
4
2
0

ampl

