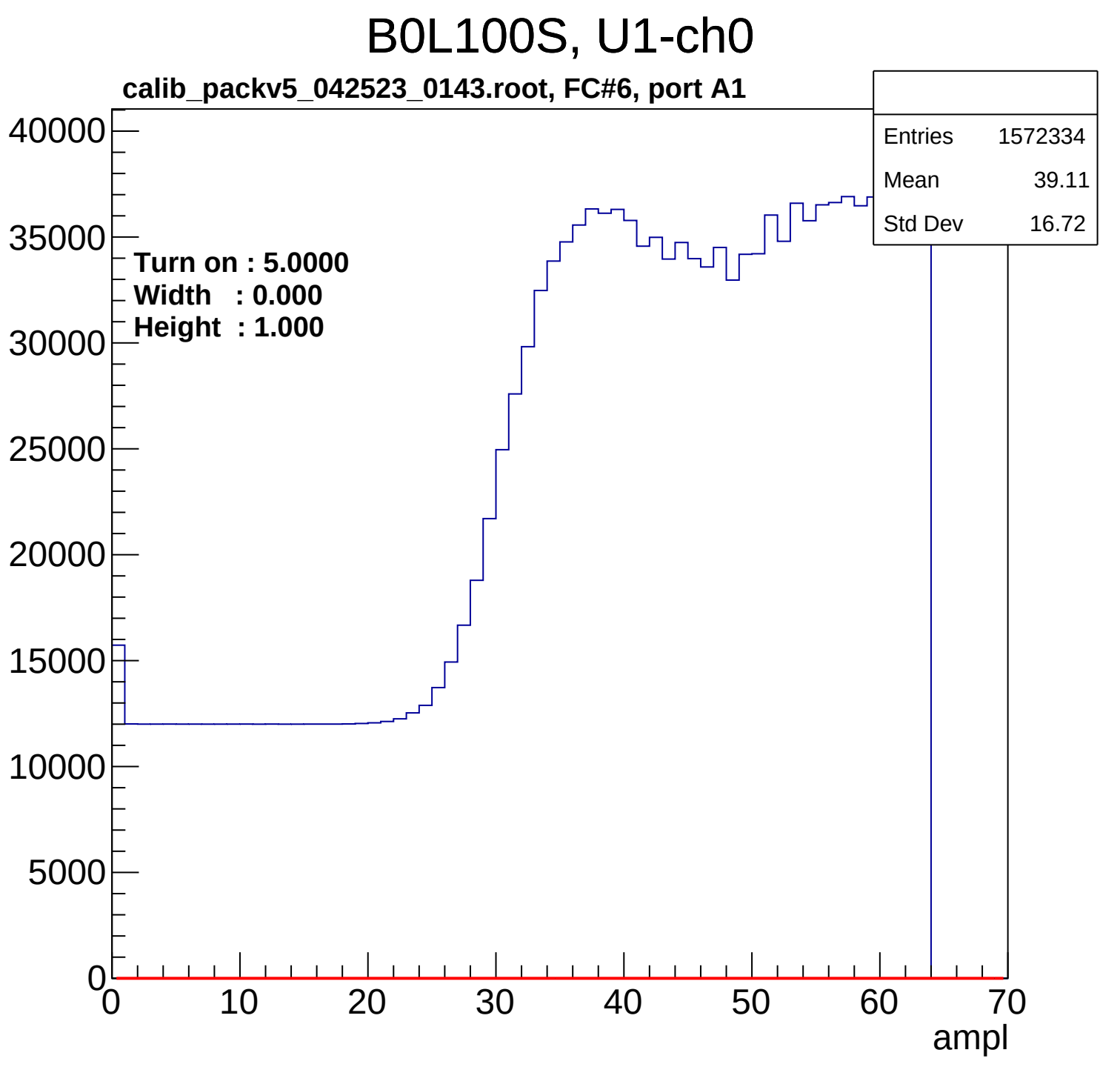
B0L100S, U1-ch0
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1572334
Mean 39.11
Std Dev 16.72
Turn on : 5.0000
Width : 0.000
Height : 1.000
40000
35000
30000
25000
20000
15000
10000
5000
0
0
10
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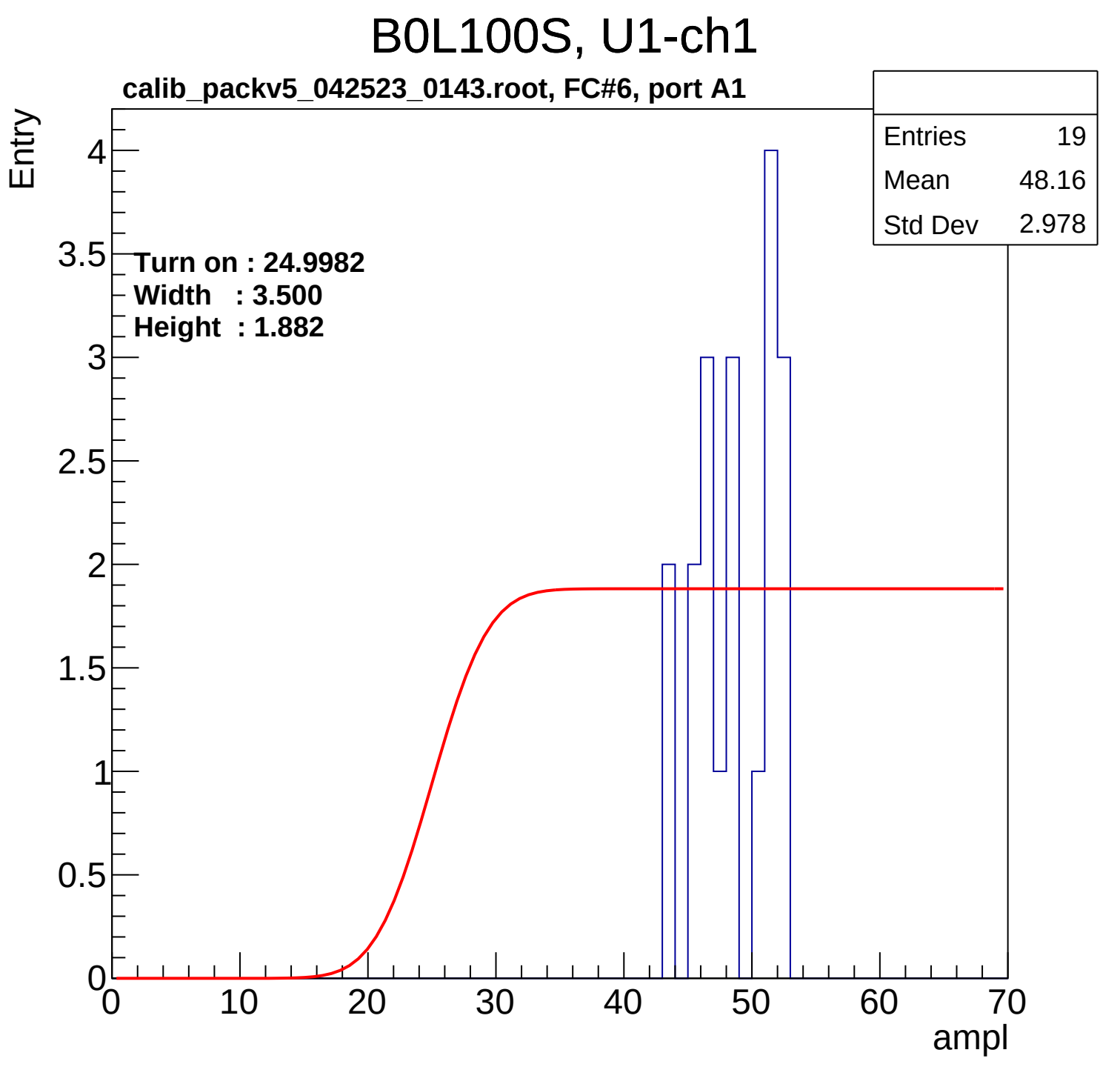
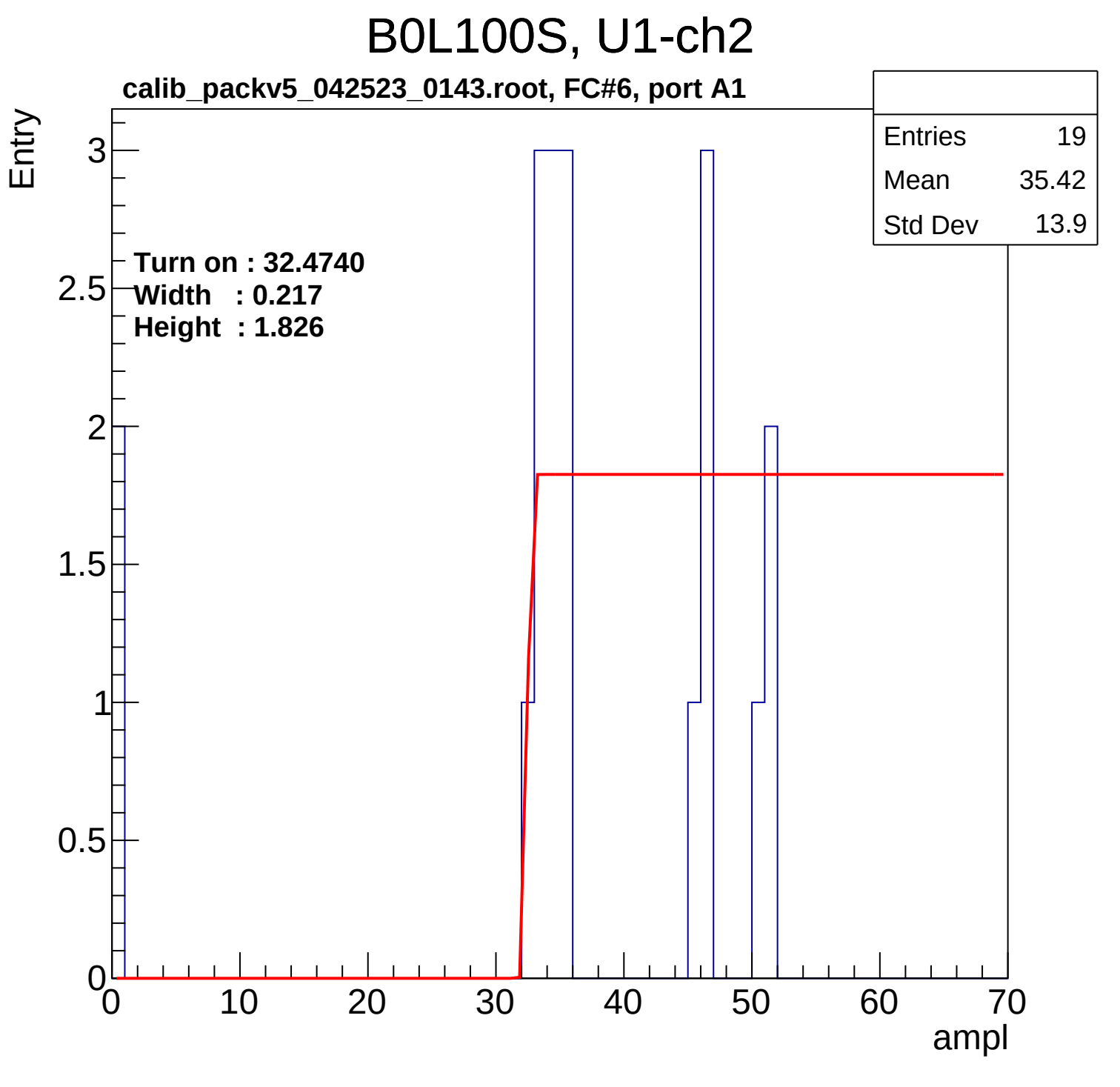
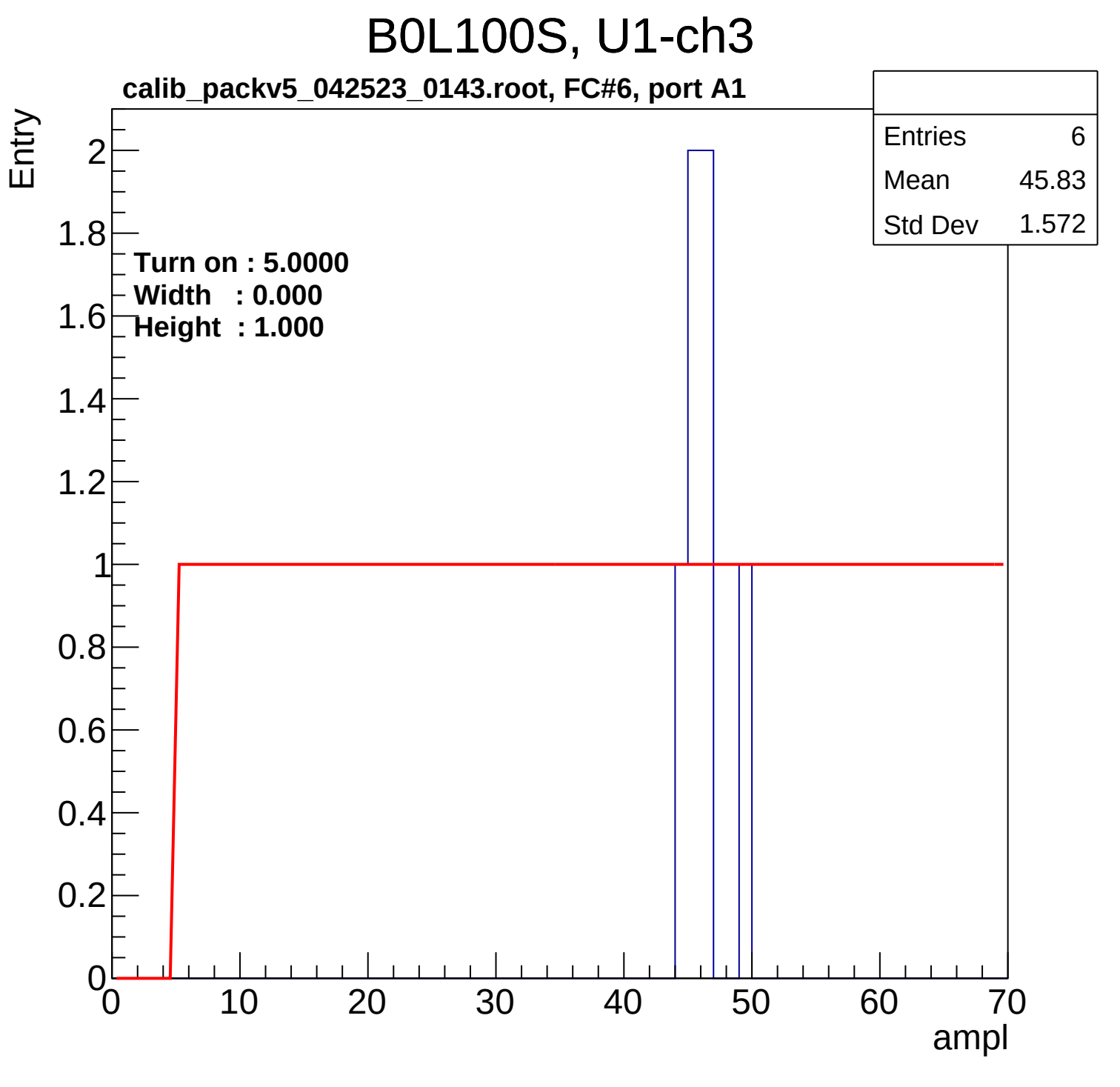
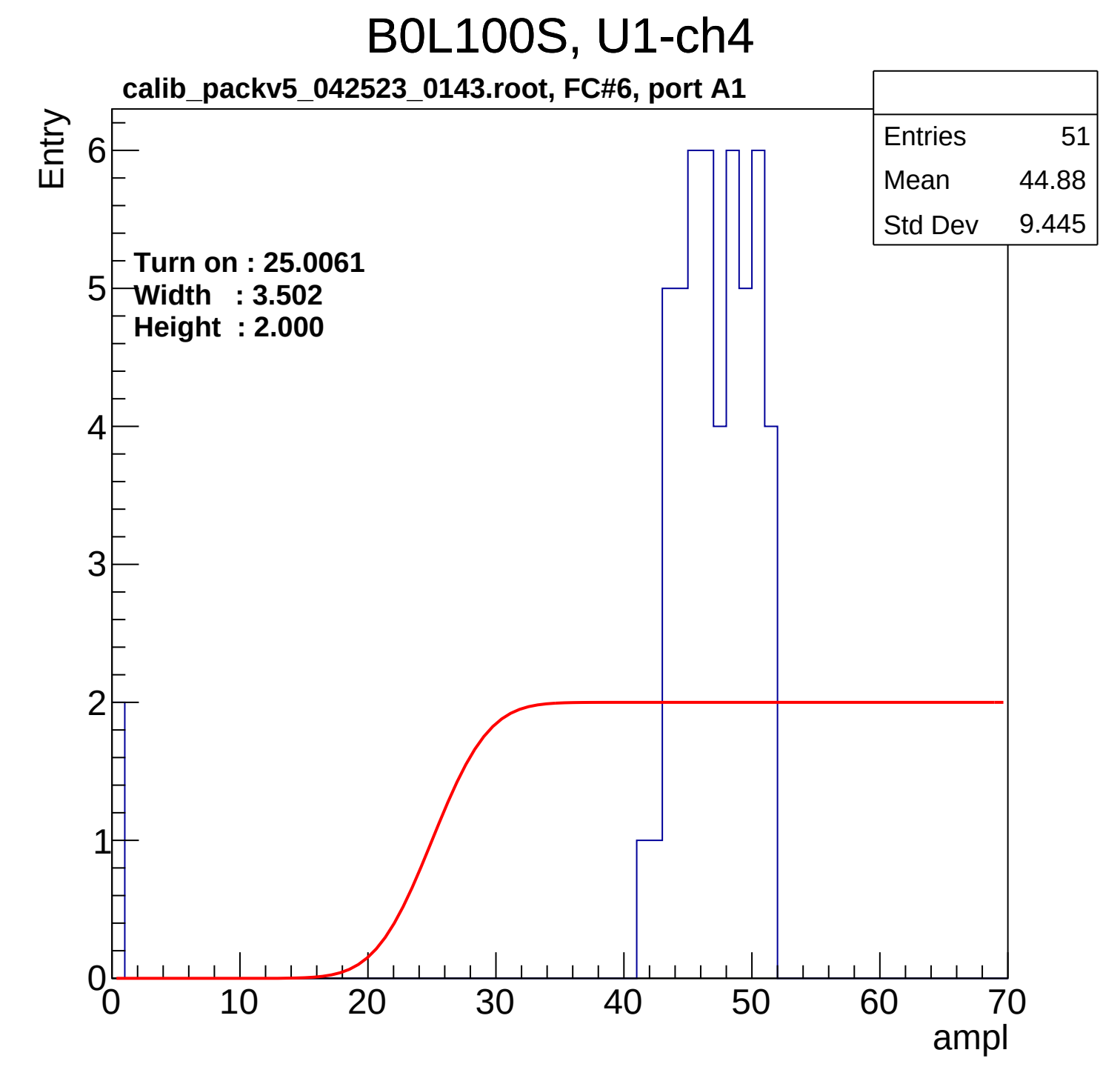
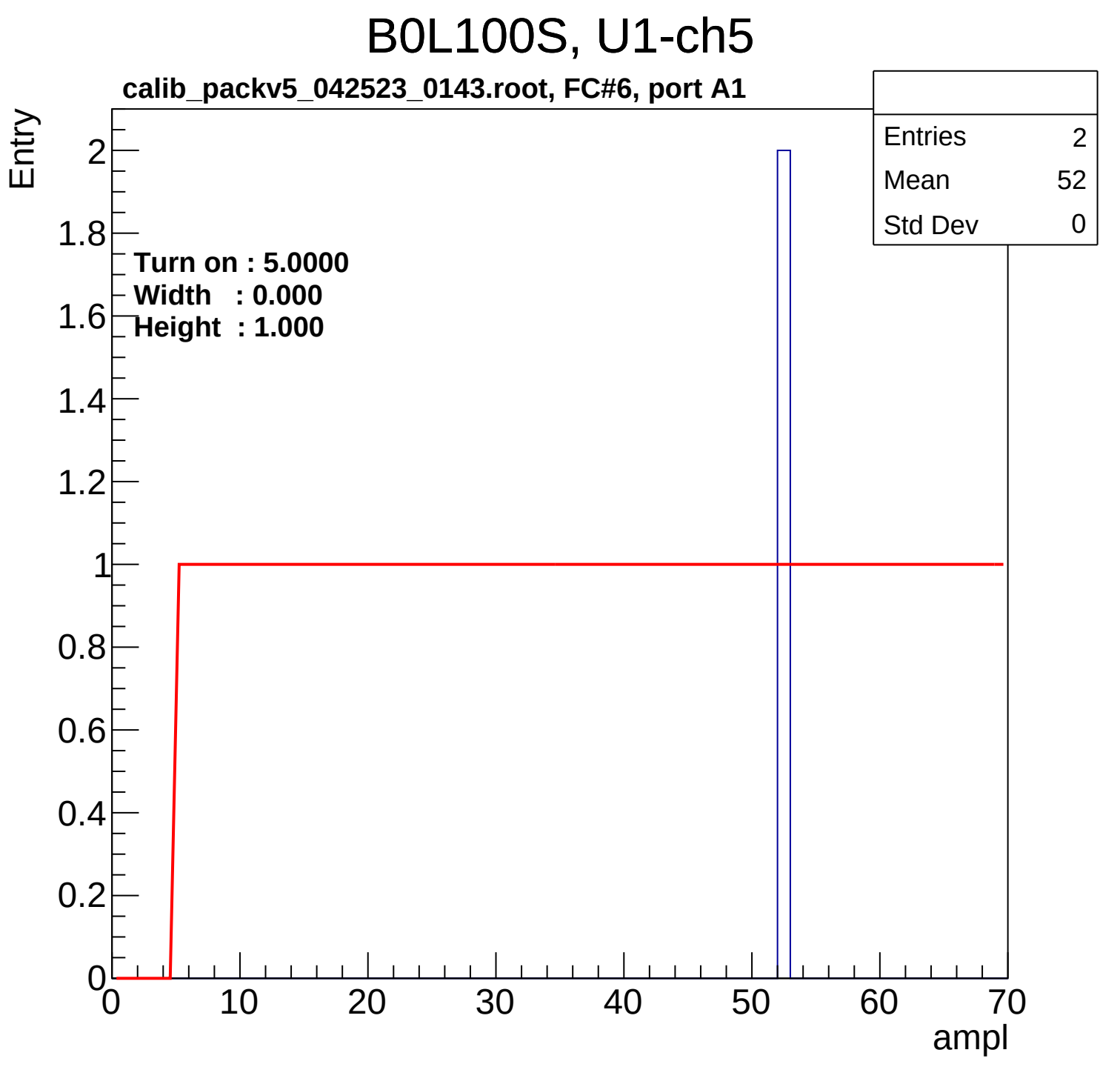
50
60
70
ampl


B0L100S, U1-ch1
calib_packv5_042523_0143.root, FC#6, port A1
Entries 19
Mean 48.16
Std Dev 2.978
Turn on : 24.9982
Width : 3.500
Height : 1.882
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B0L100S, U1-ch2
calib_packv5_042523_0143.root, FC#6, port A1
Entries 19
Mean 35.42
Std Dev 13.9
Turn on : 32.4740
Width : 0.217
Height : 1.826
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B0L100S, U1-ch3
calib_packv5_042523_0143.root, FC#6, port A1
Entries 6
Mean 45.83
Std Dev 1.572
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B0L100S, U1-ch4
calib_packv5_042523_0143.root, FC#6, port A1
Entries 51
Mean 44.88
Std Dev 9.445
Turn on : 25.0061
Width : 3.502
Height : 2.000
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B0L100S, U1-ch5
calib_packv5_042523_0143.root, FC#6, port A1
Entries 2
Mean 52
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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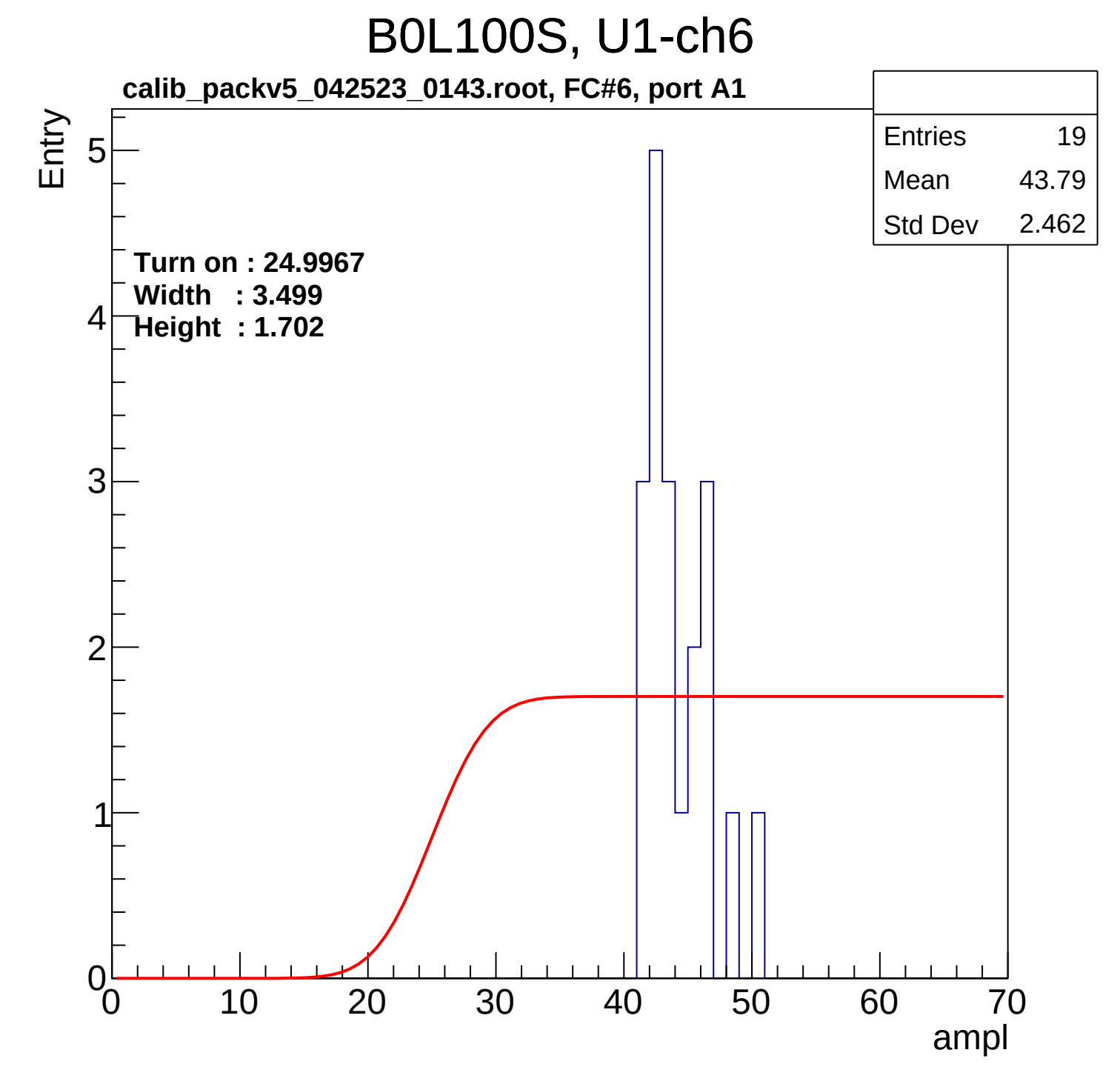
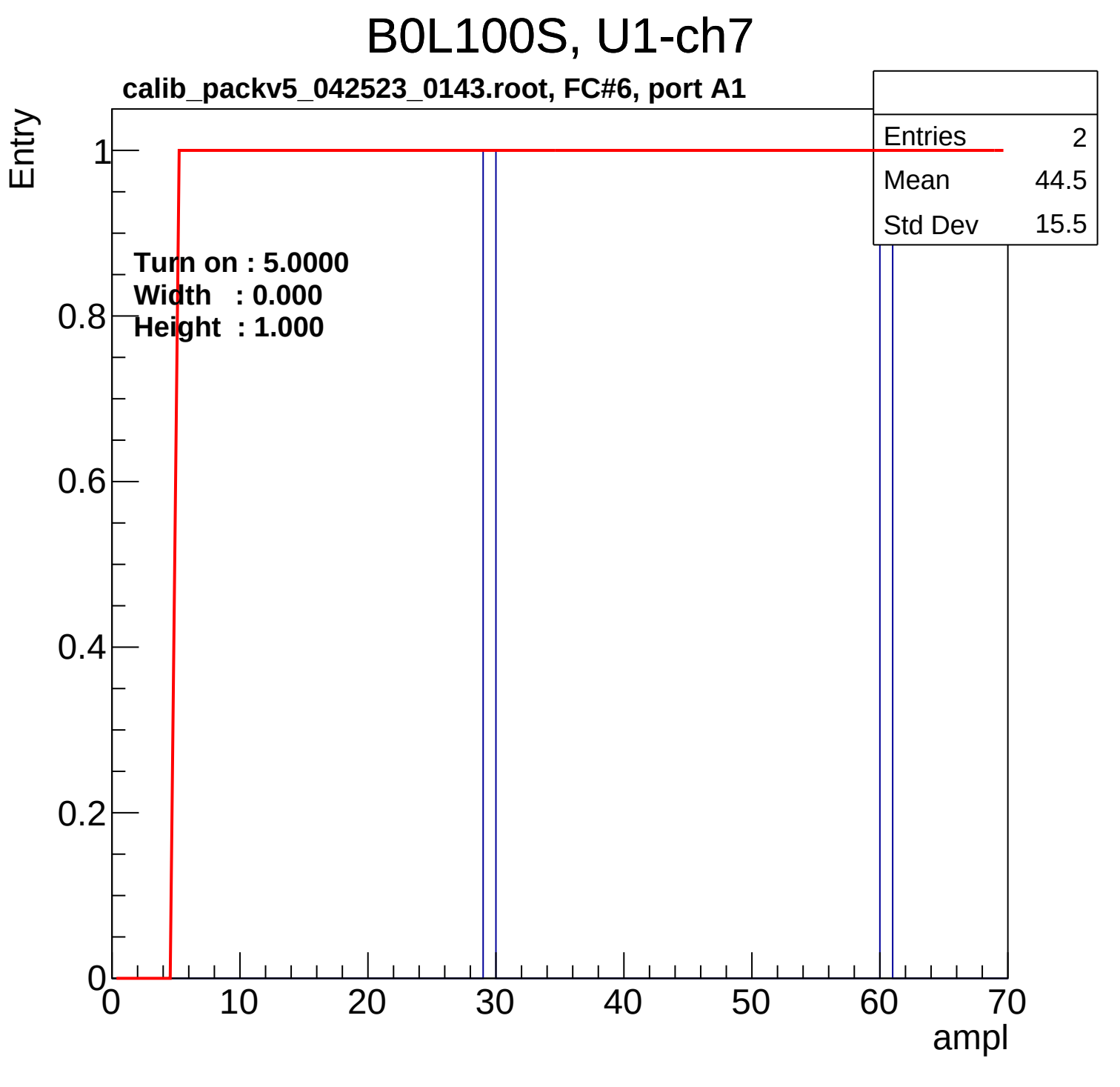
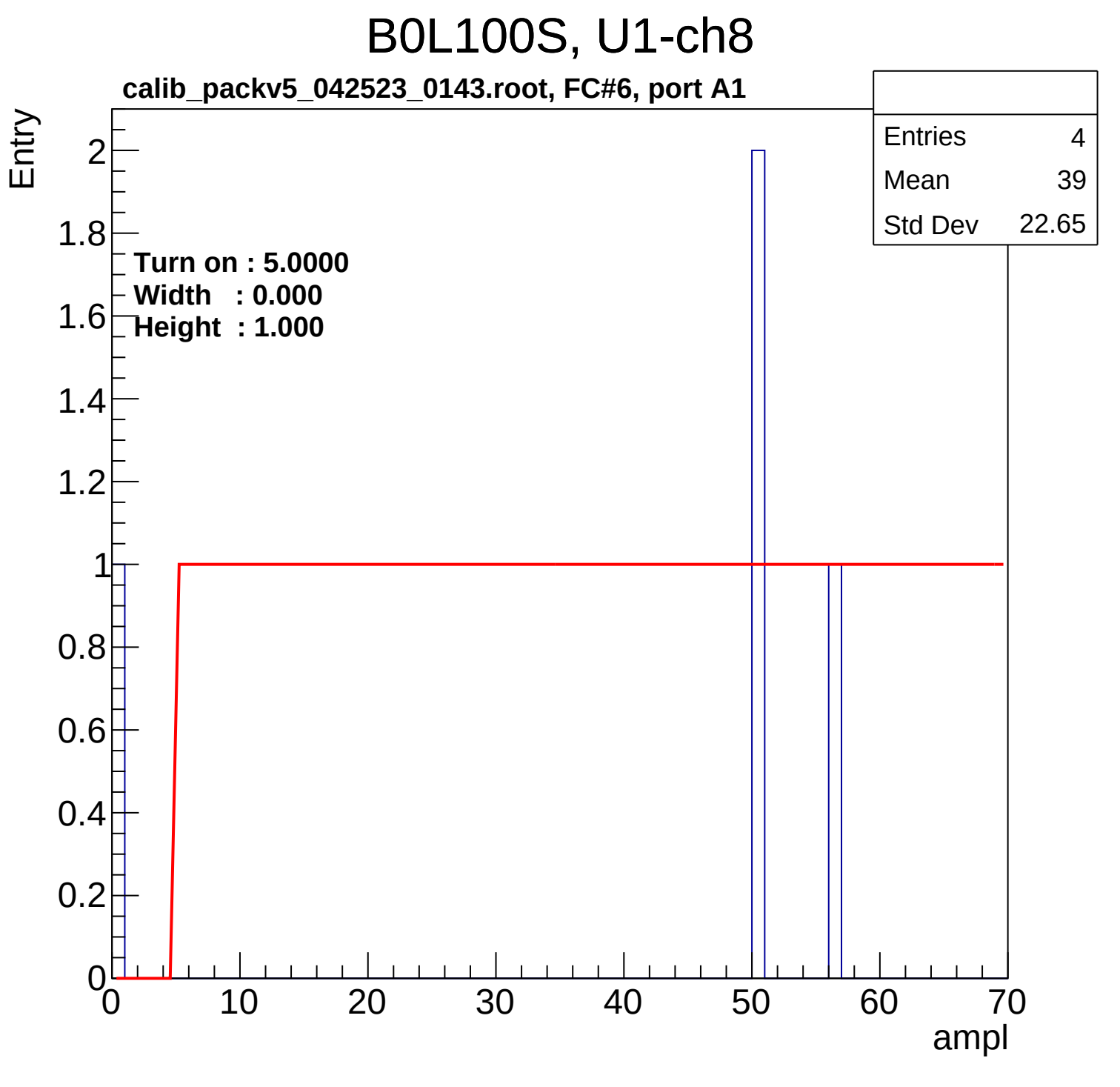
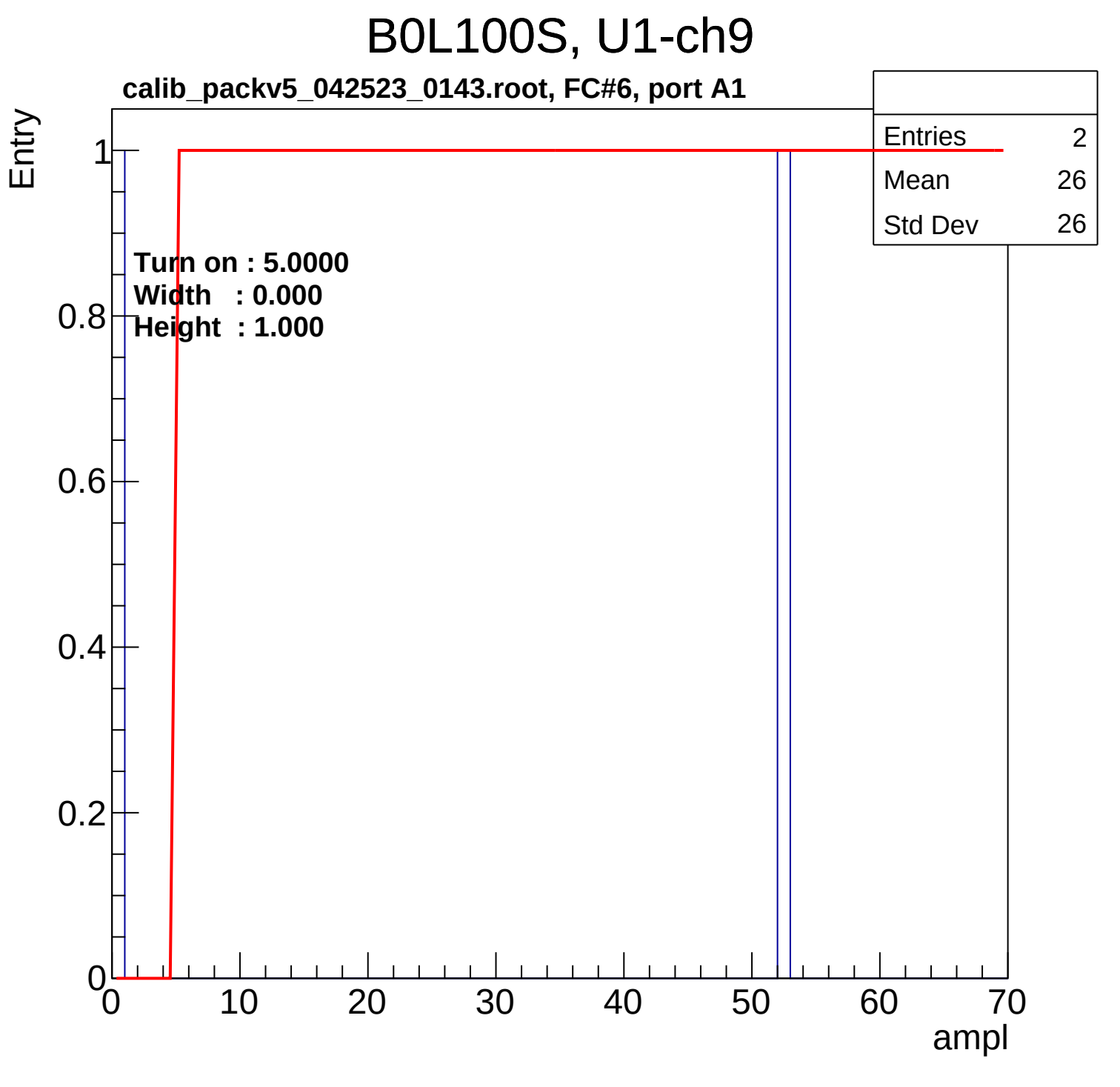
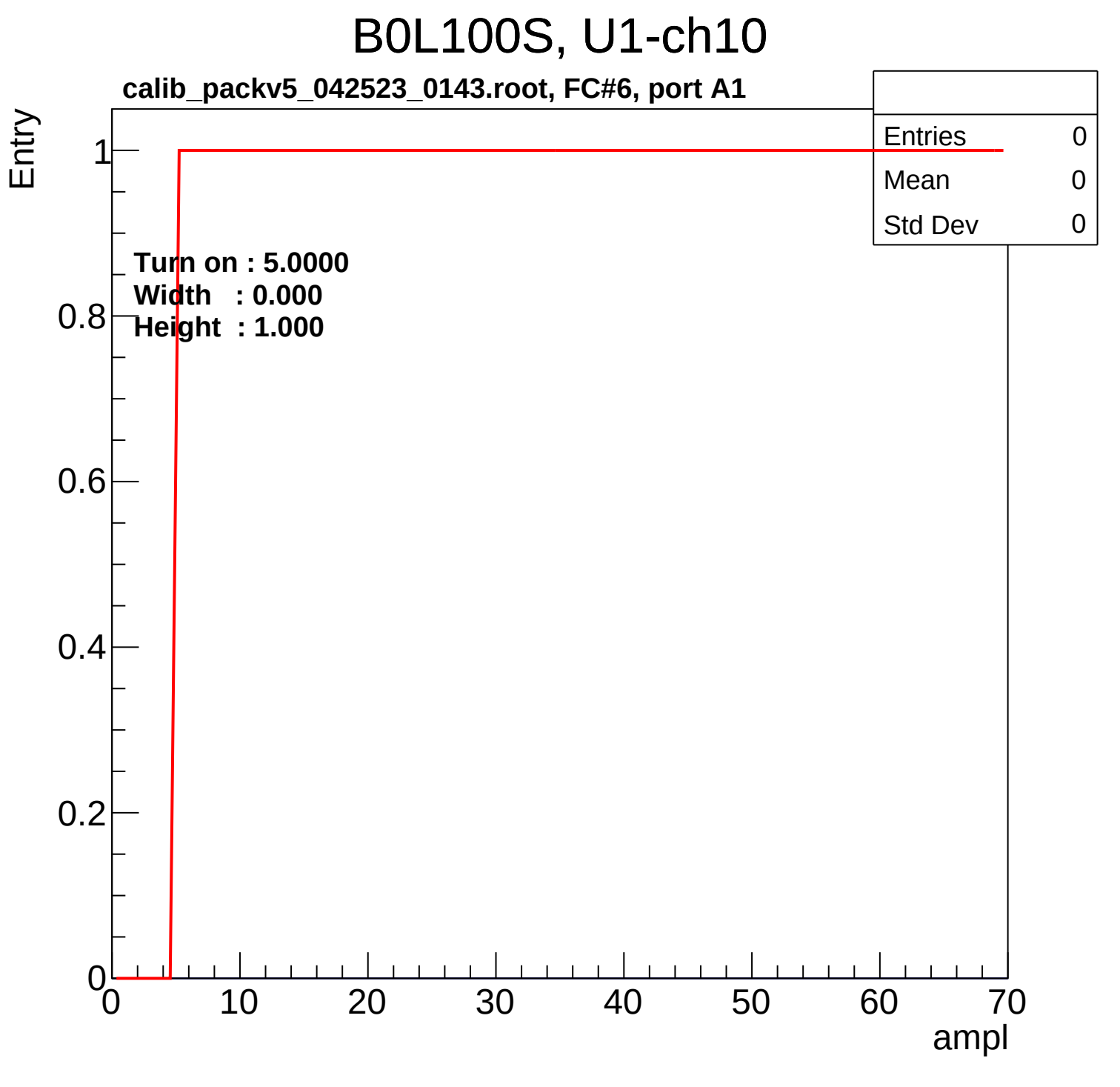
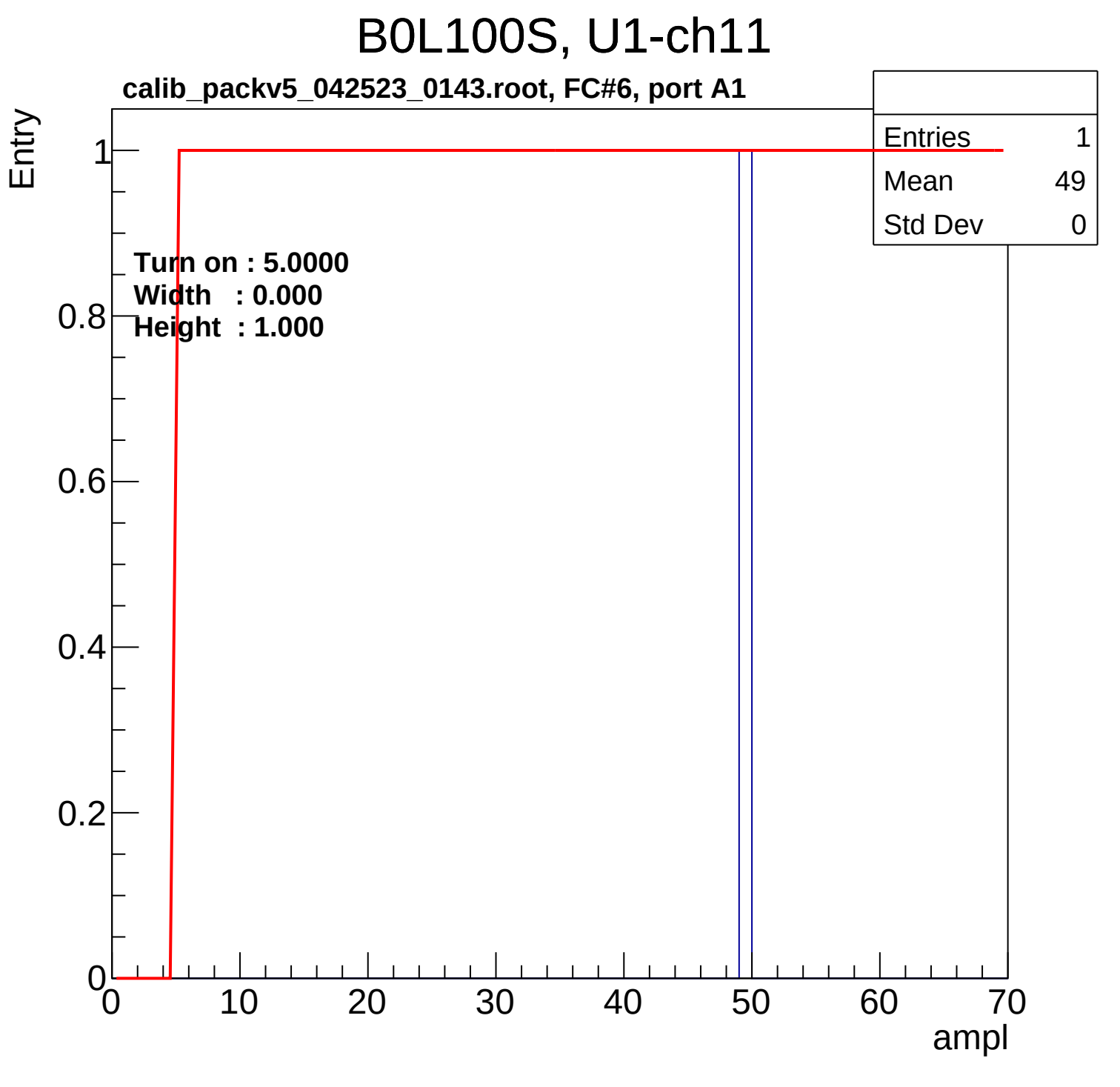

B0L100S, U1-ch6
calib_packv5_042523_0143.root, FC#6, port A1
Entries 19
Mean 43.79
Std Dev 2.462
Turn on : 24.9967
Width : 3.499
Height : 1.702
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B0L100S, U1-ch7
calib_packv5_042523_0143.root, FC#6, port A1
Entries 2
Mean 44.5
Std Dev 15.5
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B0L100S, U1-ch8
calib_packv5_042523_0143.root, FC#6, port A1
Entries 4
Mean 39
Std Dev 22.65
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B0L100S, U1-ch9
calib_packv5_042523_0143.root, FC#6, port A1
Entries 2
Mean 26
Std Dev 26
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U1-ch10
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U1-ch11
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 49
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
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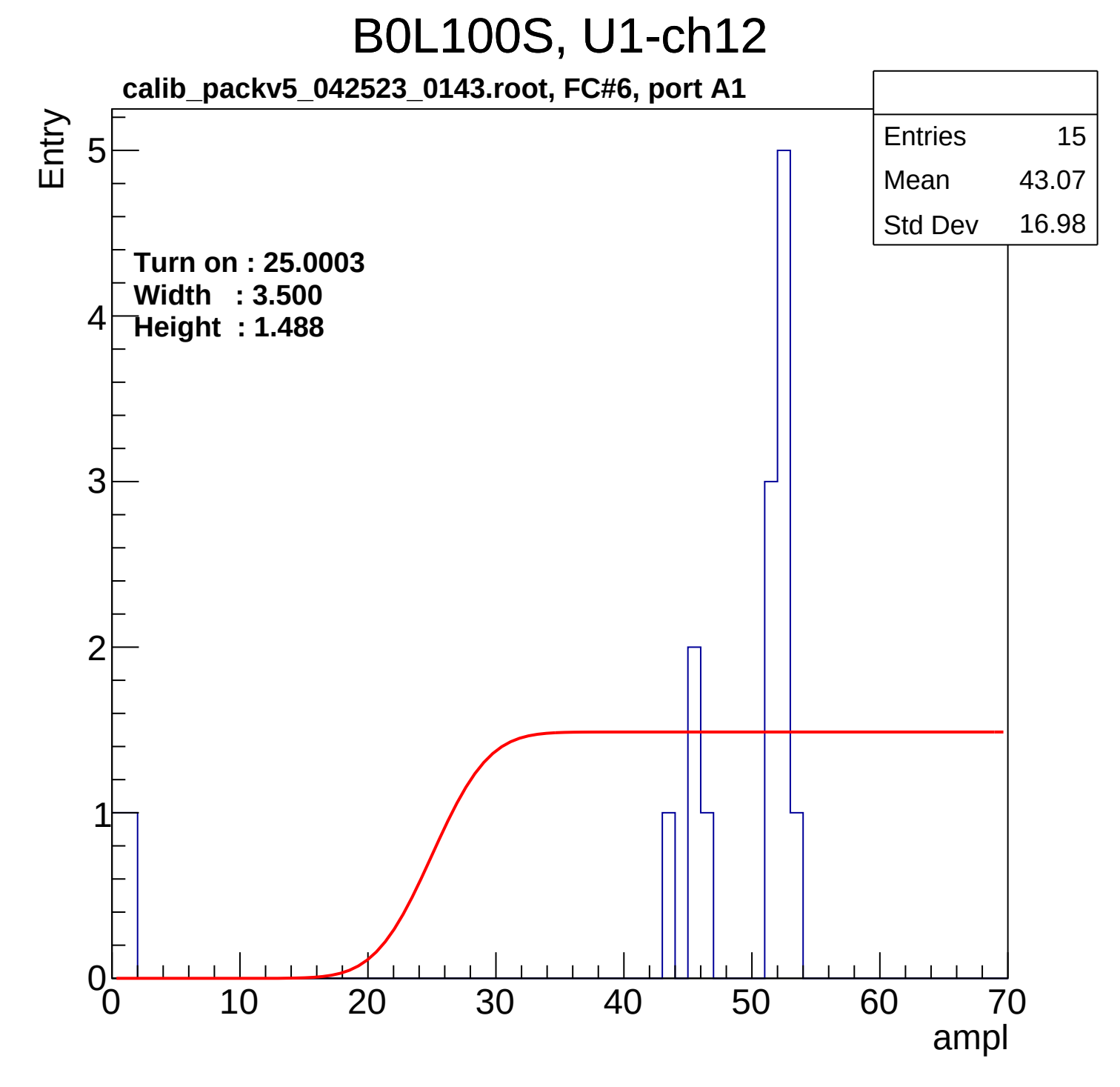
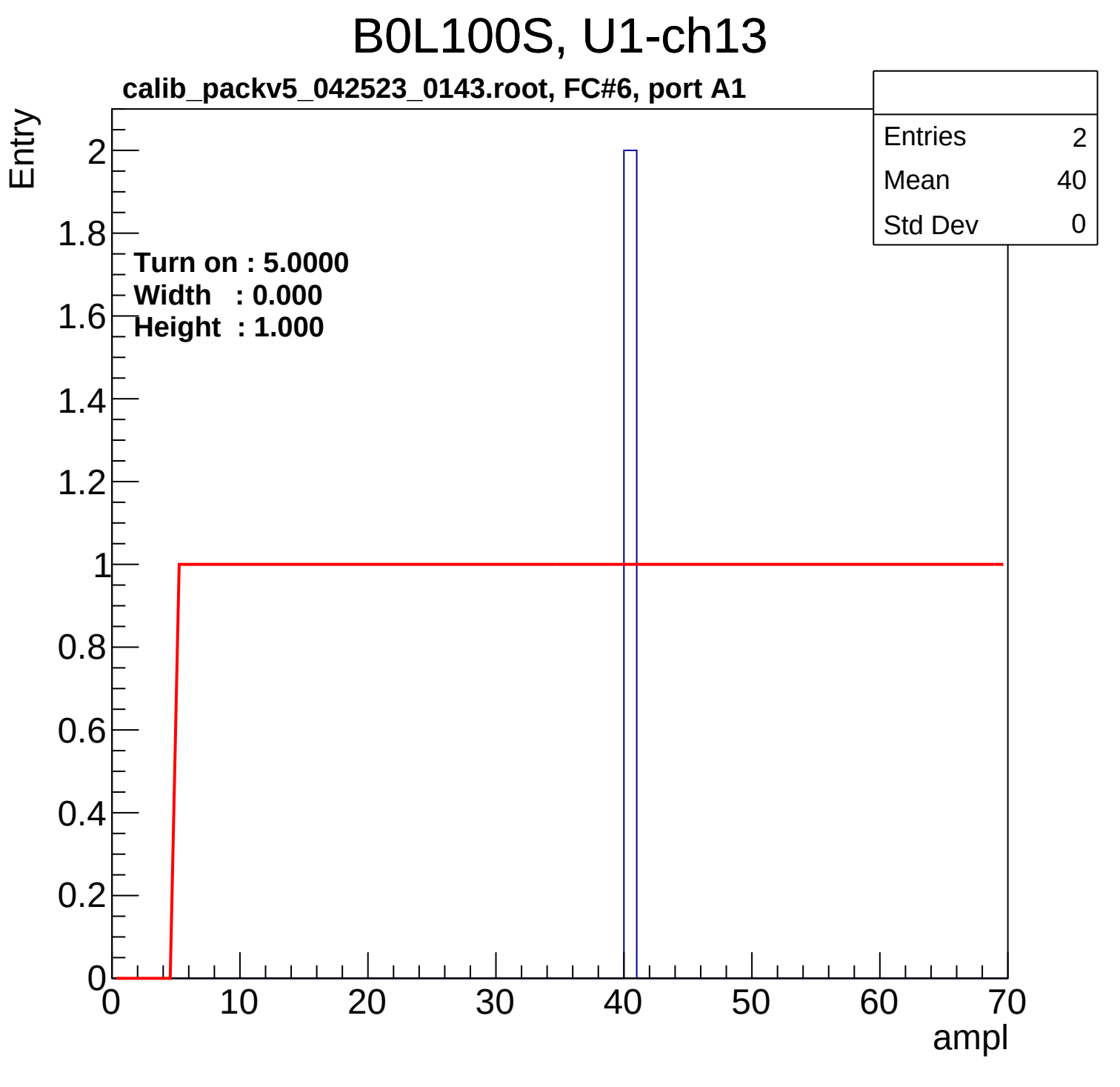
20
30
40
50
60
70


B0L100S, U1-ch12
calib_packv5_042523_0143.root, FC#6, port A1
Entries 15
Mean 43.07
Std Dev 16.98
Turn on : 25.0003
Width : 3.500
Height : 1.488
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5


B0L100S, U1-ch13
calib_packv5_042523_0143.root, FC#6, port A1
Entries 2
Mean 40
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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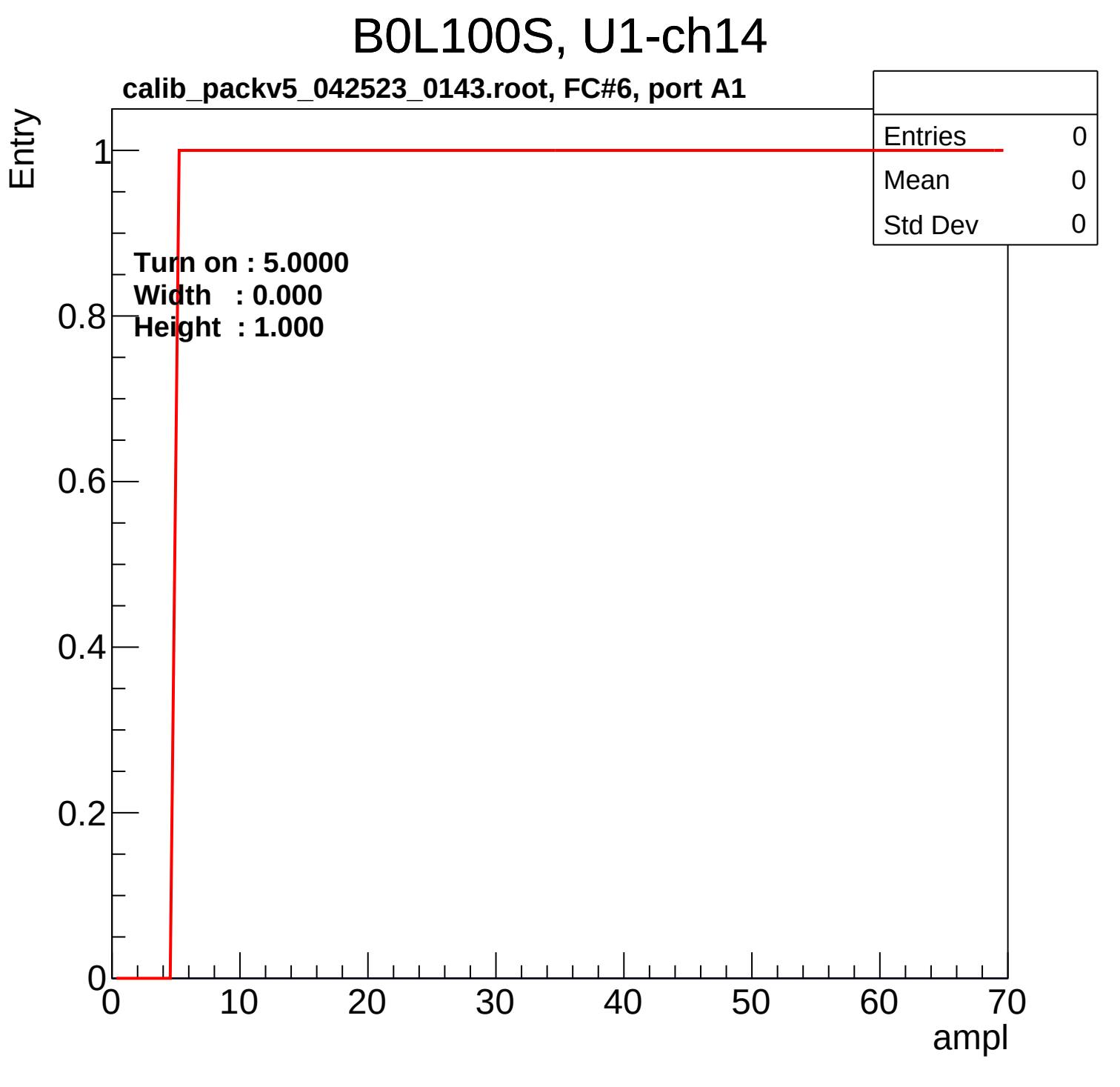
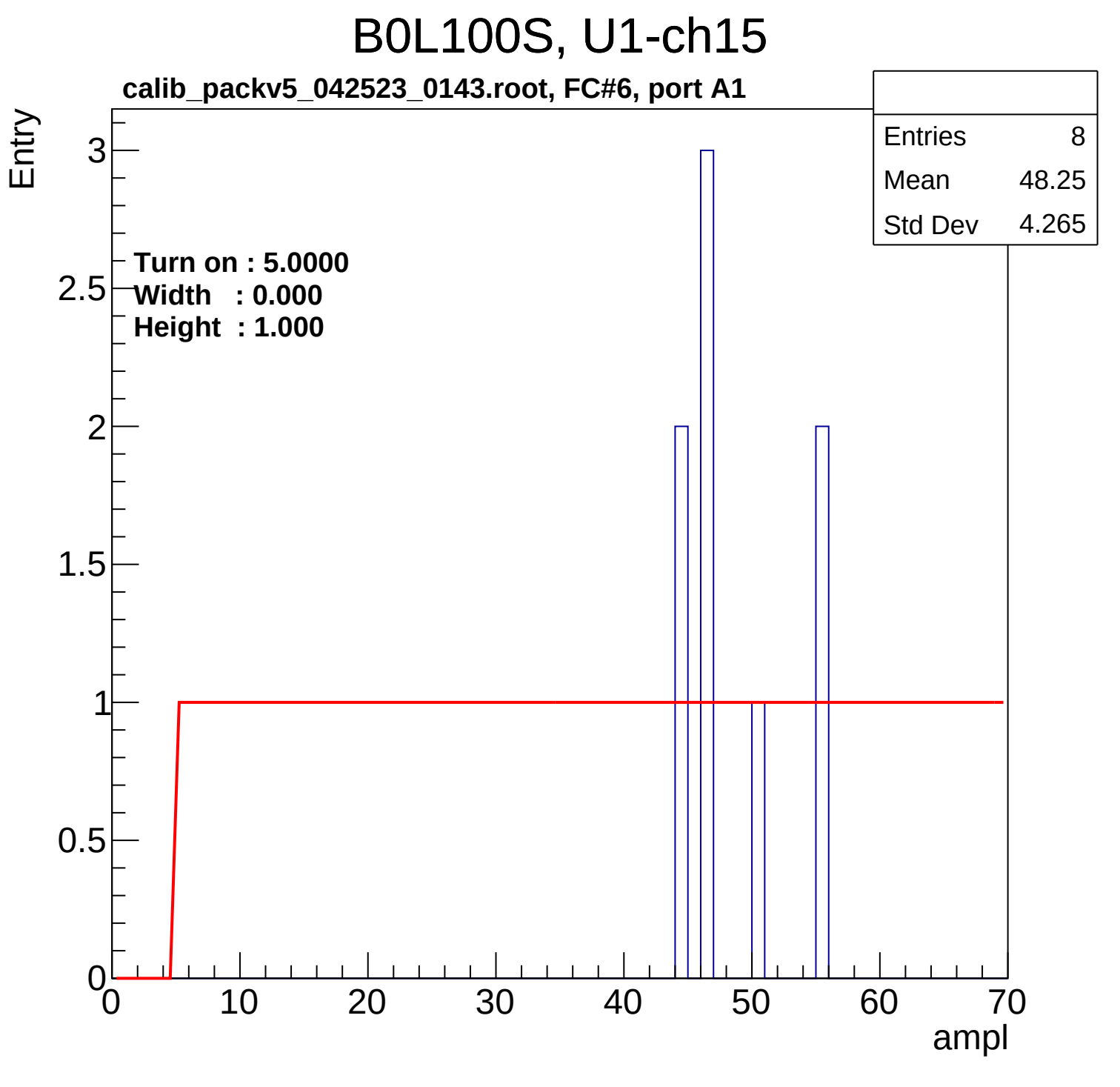

B0L100S, U1-ch14
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U1-ch15
calib_packv5_042523_0143.root, FC#6, port A1
Entries 8
Mean 48.25
Std Dev 4.265
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
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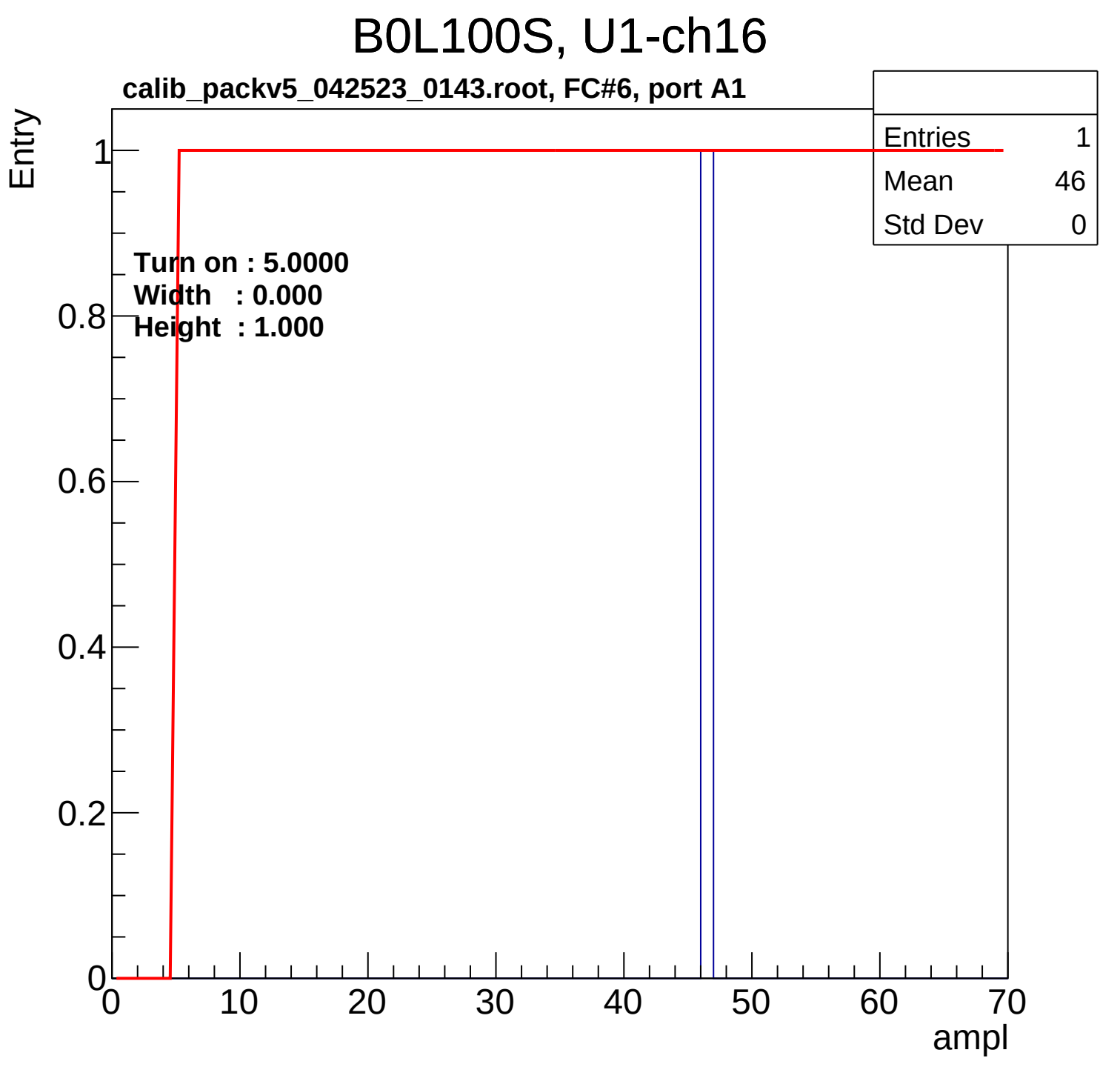
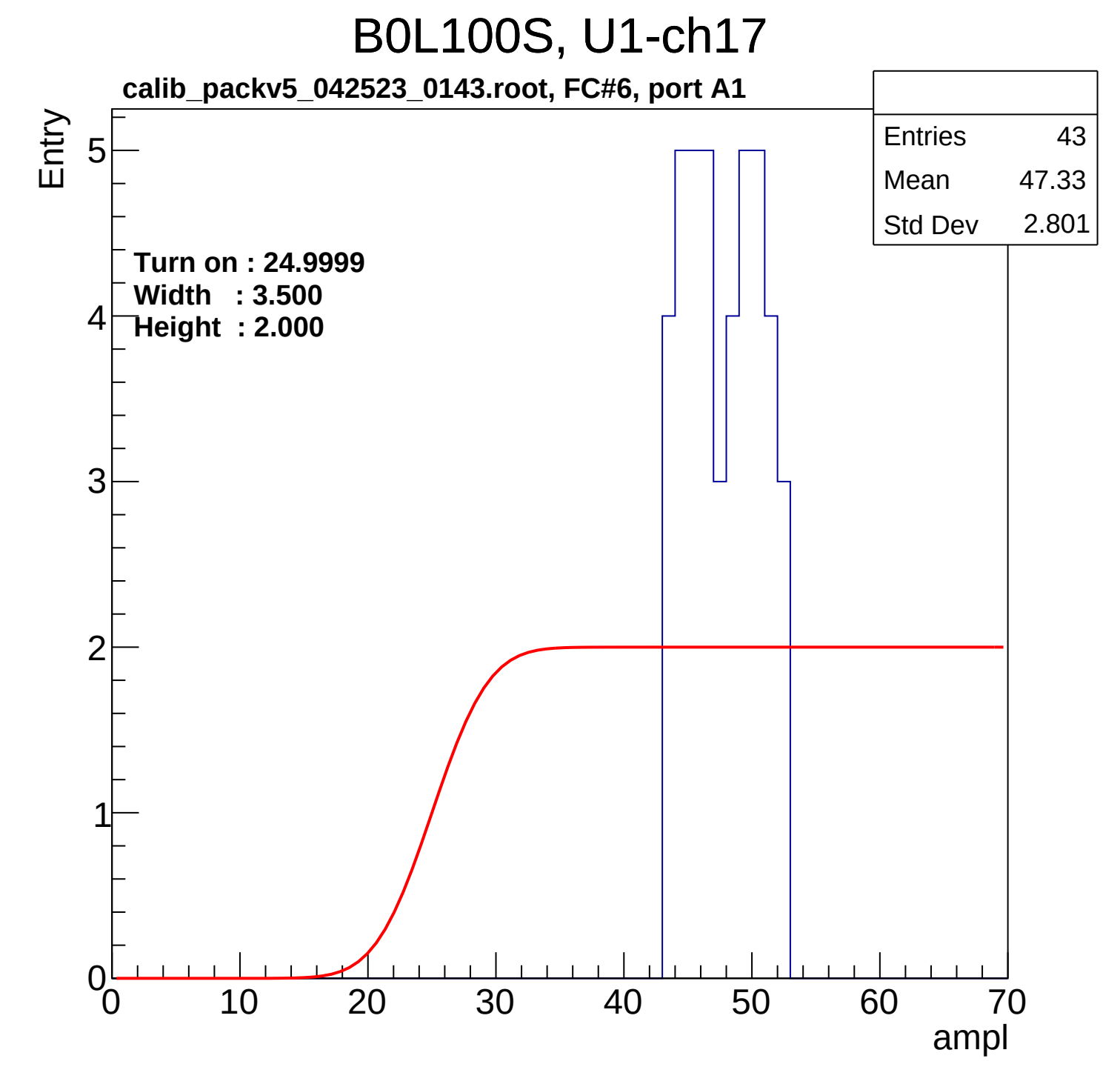
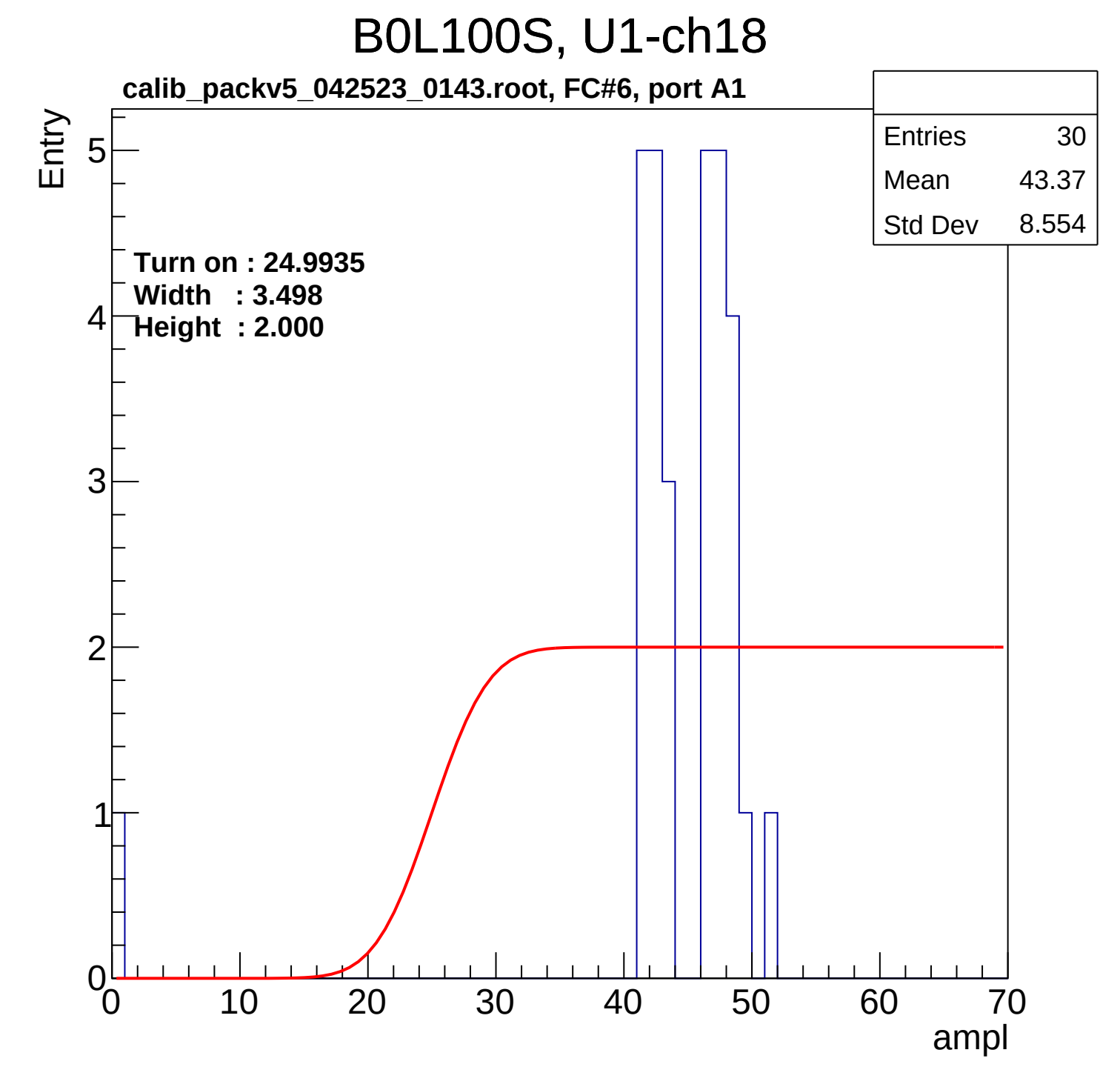
20
30
40
50
60
70


B0L100S, U1-ch16
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 46
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B0L100S, U1-ch17
calib_packv5_042523_0143.root, FC#6, port A1
Entries 43
Mean 47.33
Std Dev 2.801
Turn on : 24.9999
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B0L100S, U1-ch18
calib_packv5_042523_0143.root, FC#6, port A1
Entries 30
Mean 43.37
Std Dev 8.554
Turn on : 24.9935
Width : 3.498
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
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40
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60
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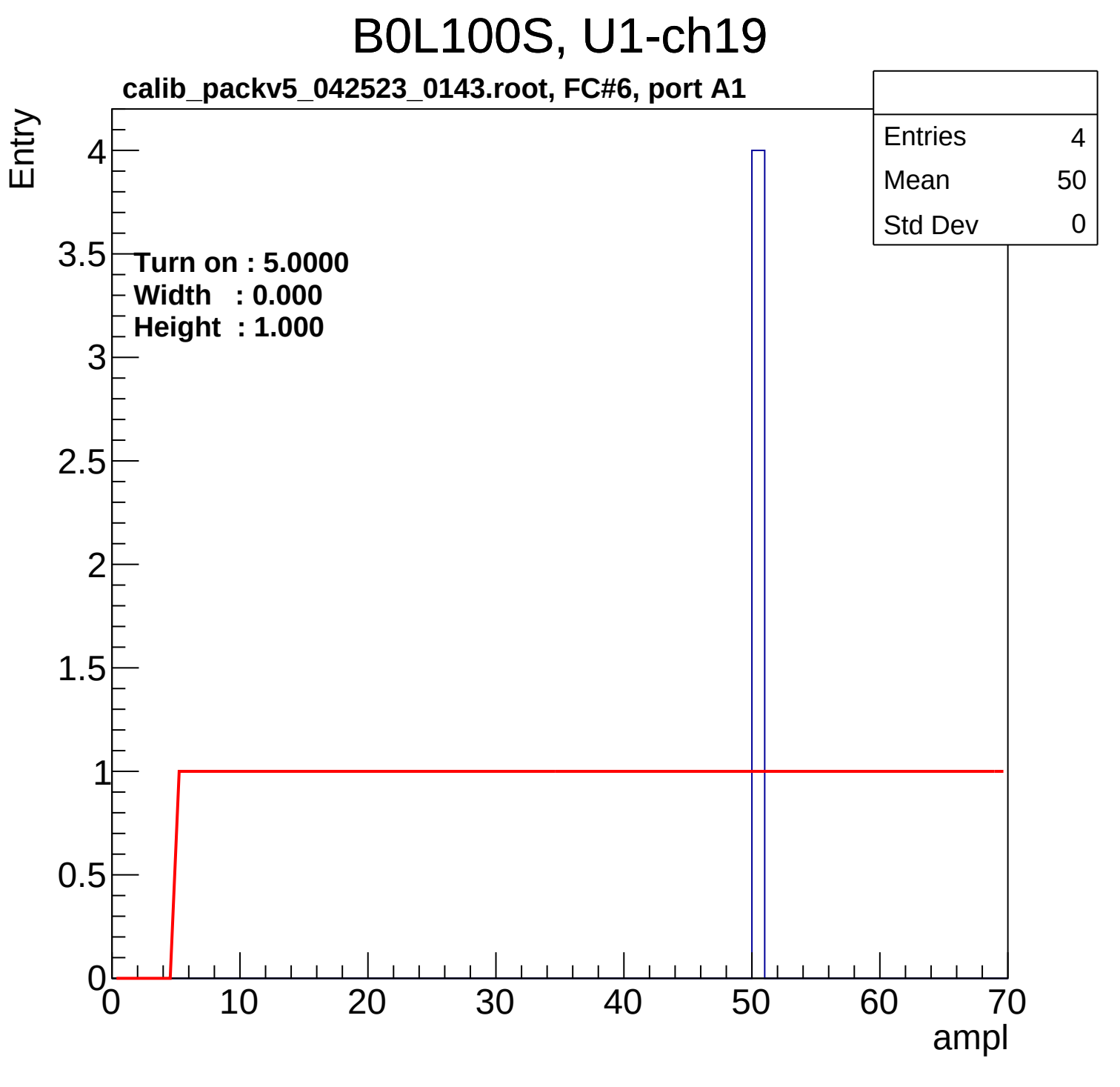
B0L100S, U1-ch19
calib_packv5_042523_0143.root, FC#6, port A1
Entries 4
Mean 50
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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40
50
60
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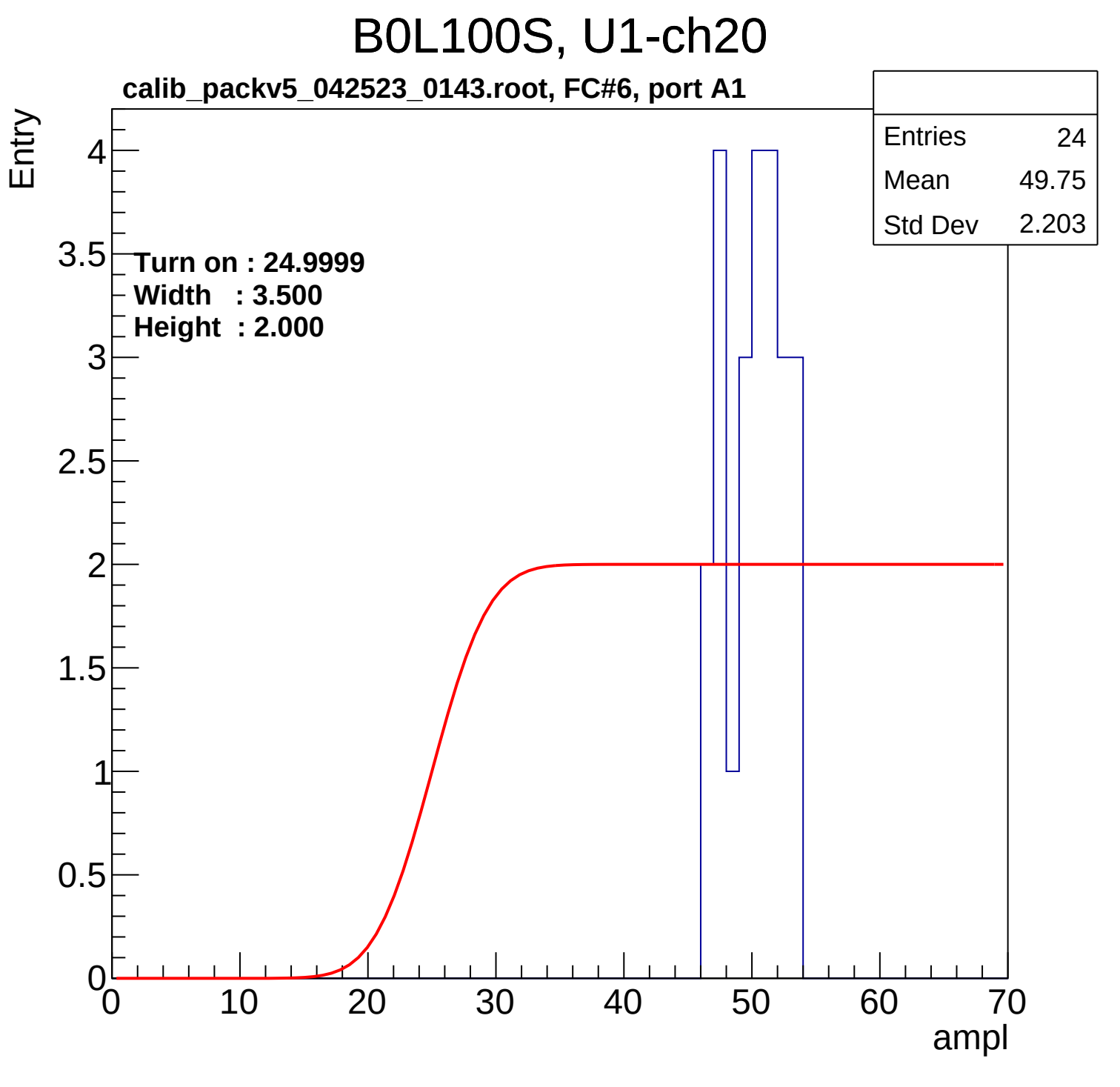
B0L100S, U1-ch20
calib_packv5_042523_0143.root, FC#6, port A1
Entries 24
Mean 49.75
Std Dev 2.203
Turn on : 24.9999
Width : 3.500
Height : 2.000
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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40
50
60
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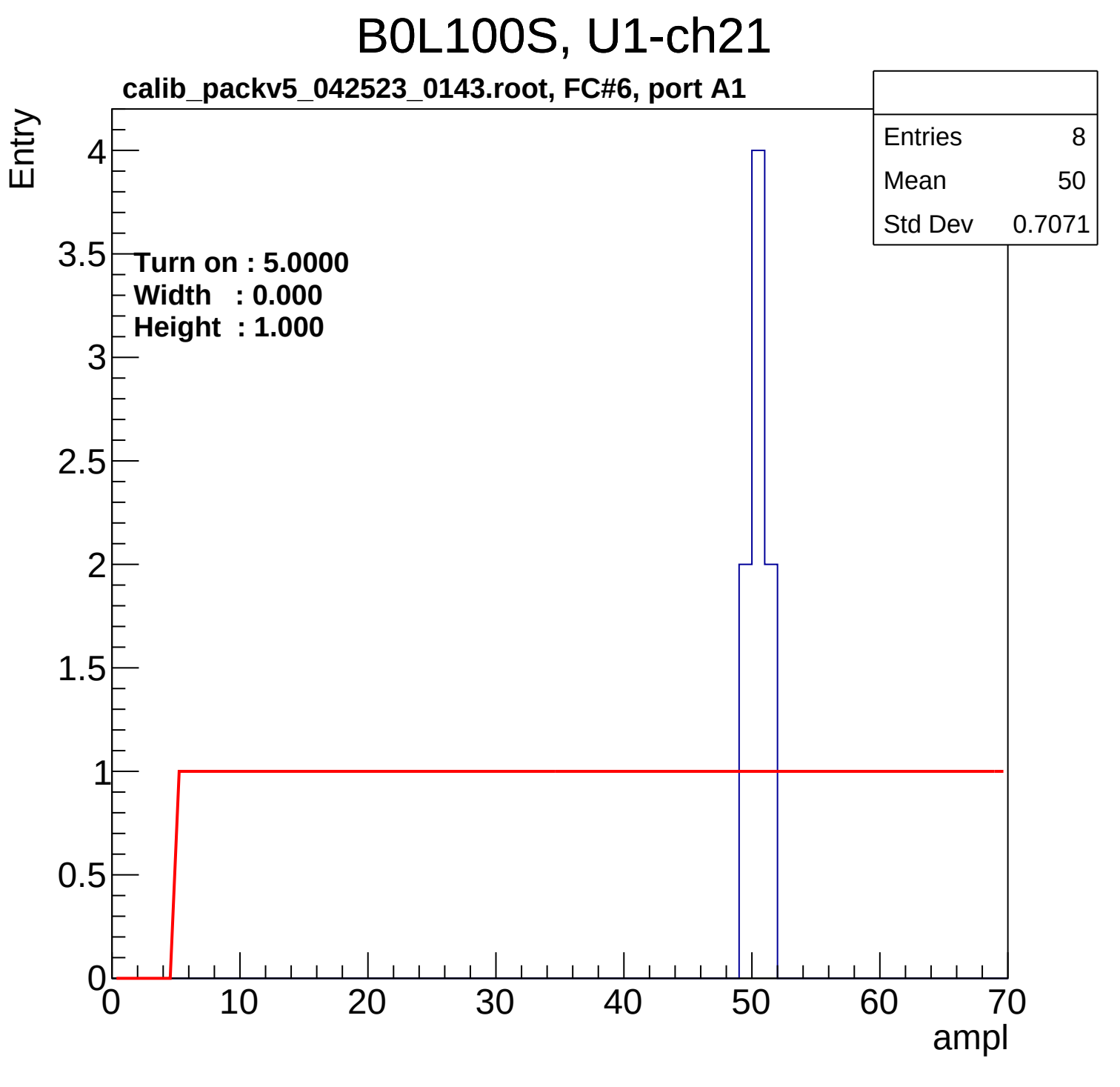
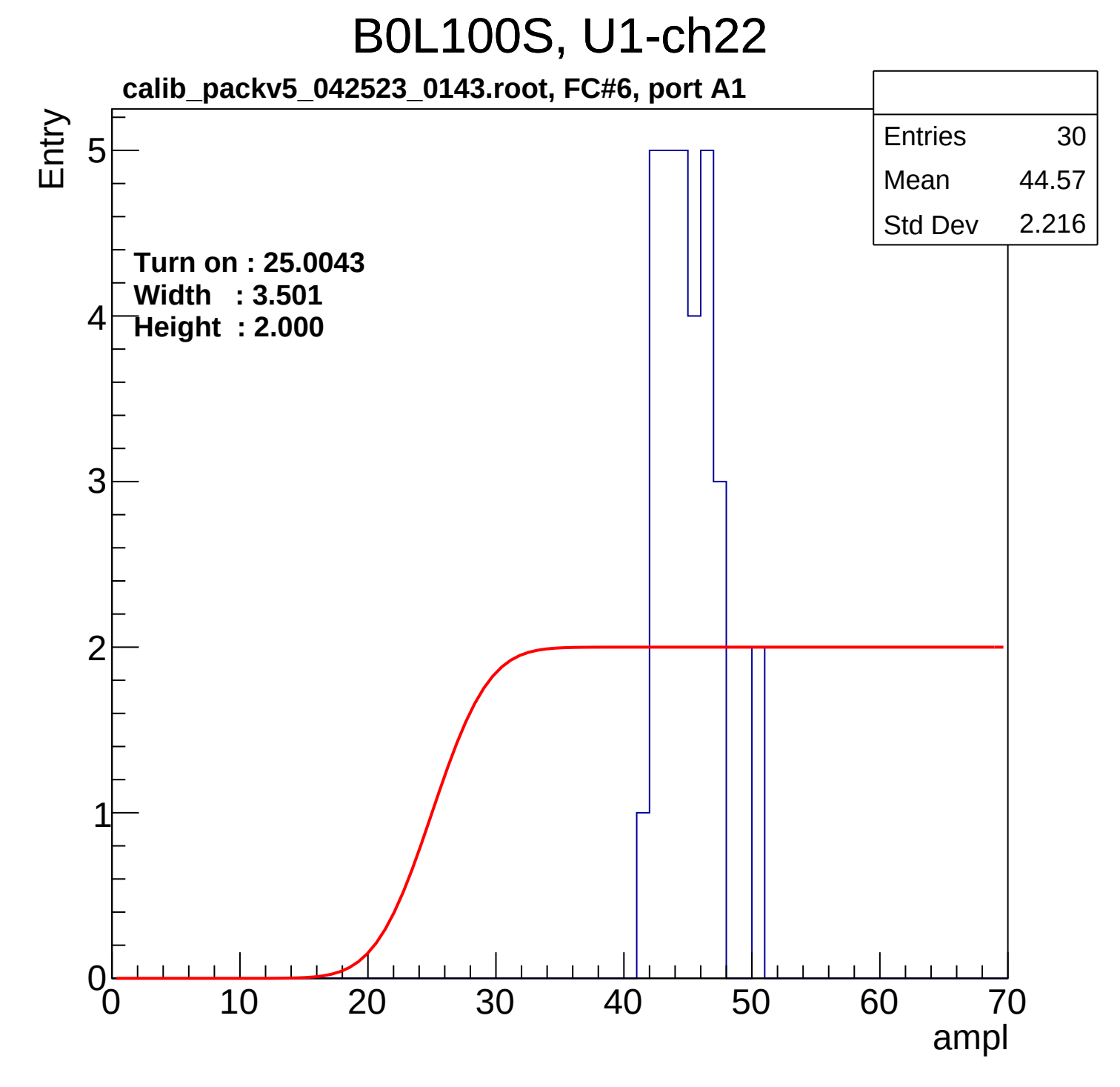

B0L100S, U1-ch21
calib_packv5_042523_0143.root, FC#6, port A1
Entries 8
Mean 50
Std Dev 0.7071
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B0L100S, U1-ch22
calib_packv5_042523_0143.root, FC#6, port A1
Entries 30
Mean 44.57
Std Dev 2.216
Turn on : 25.0043
Width : 3.501
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
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40
50
60
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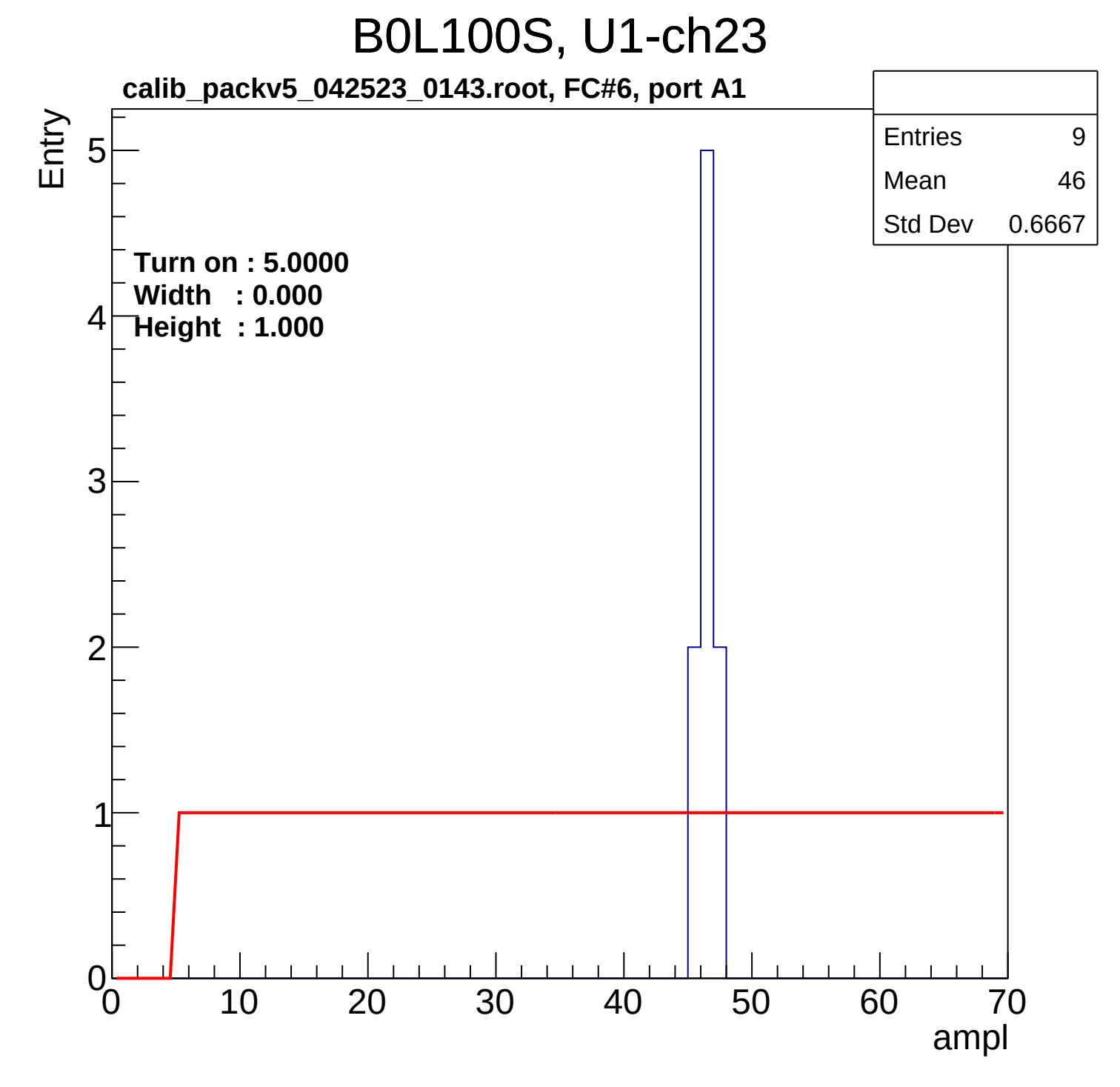
B0L100S, U1-ch23
calib_packv5_042523_0143.root, FC#6, port A1
Entries 9
Mean 46
Std Dev 0.6667
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
1
2
3
4
5
0
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20
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40
50
60
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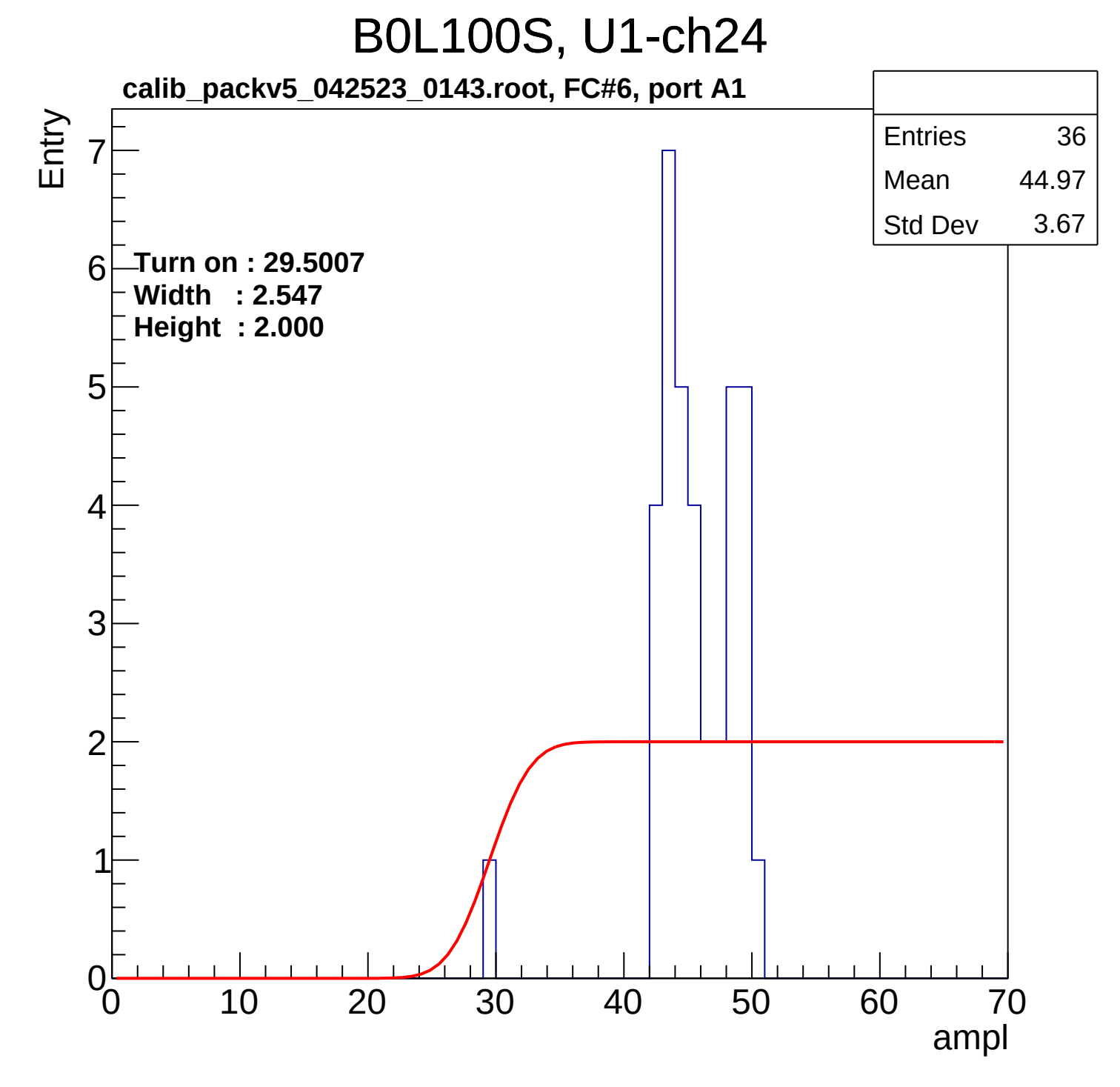
B0L100S, U1-ch24
calib_packv5_042523_0143.root, FC#6, port A1
Entries 36
Mean 44.97
Std Dev 3.67
Turn on : 29.5007
Width : 2.547
Height : 2.000
Entry
ampl
0
1
2
3
4
5
6
7
0
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40
50
60
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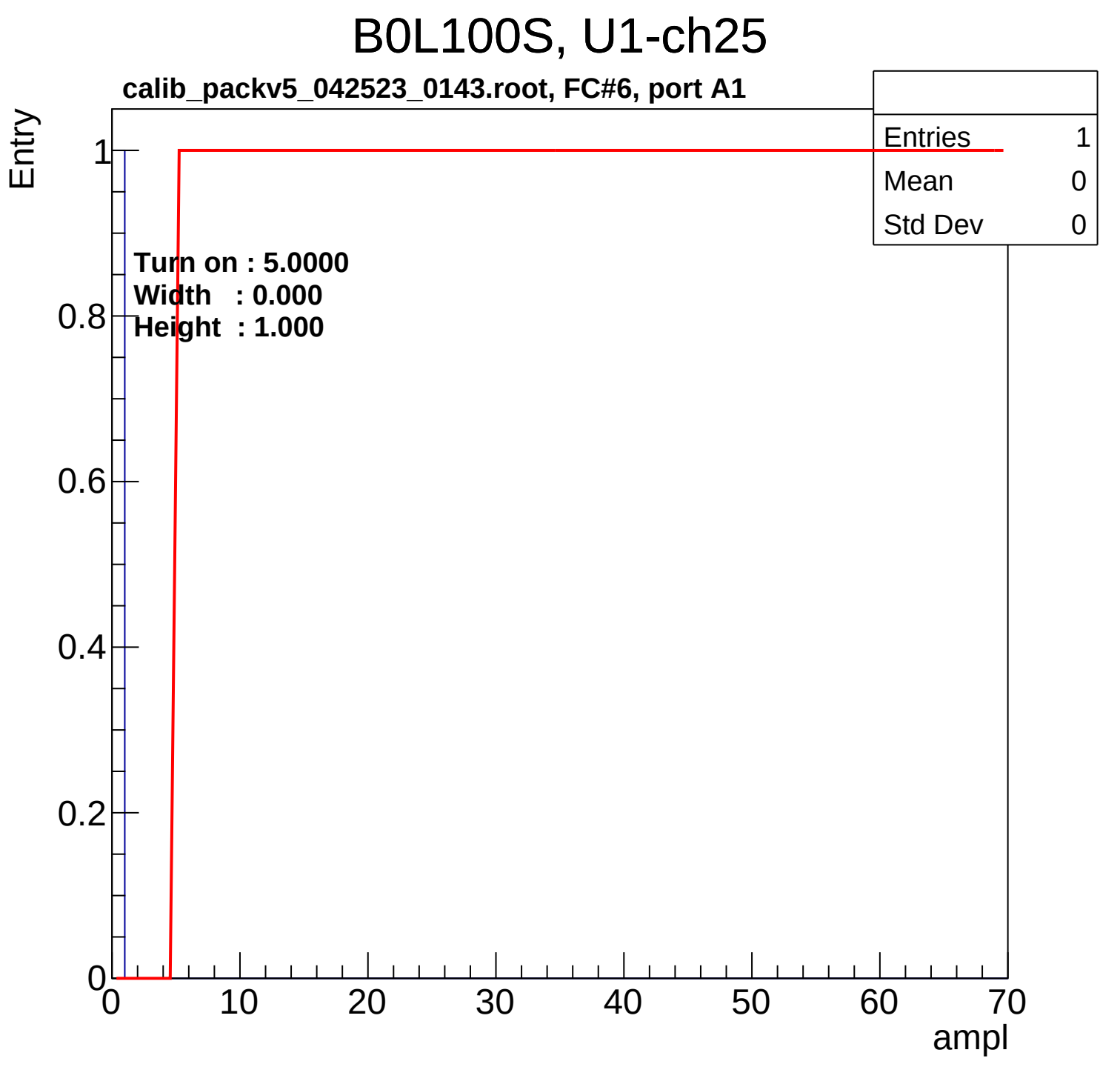
B0L100S, U1-ch25
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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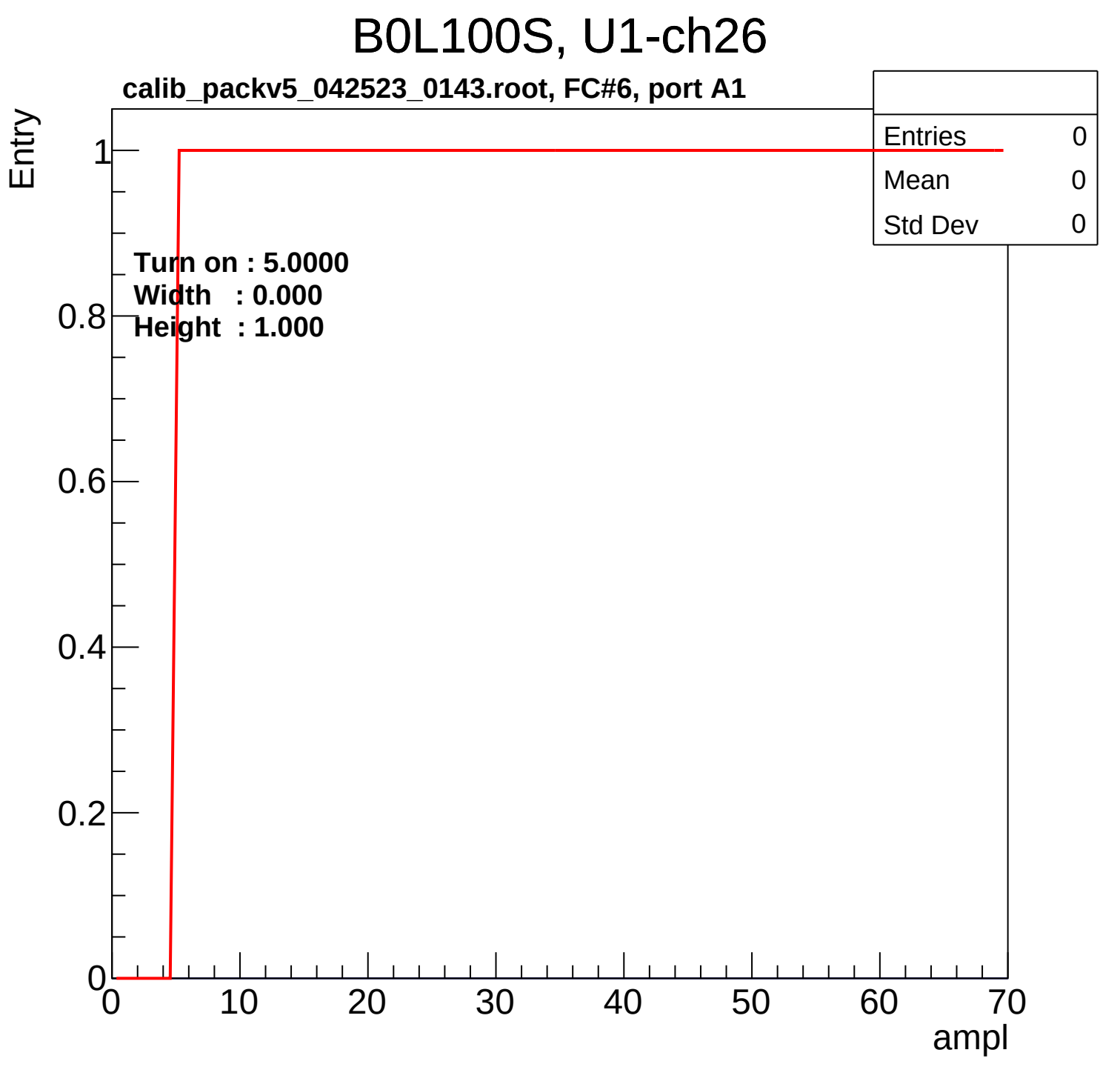
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U1-ch26
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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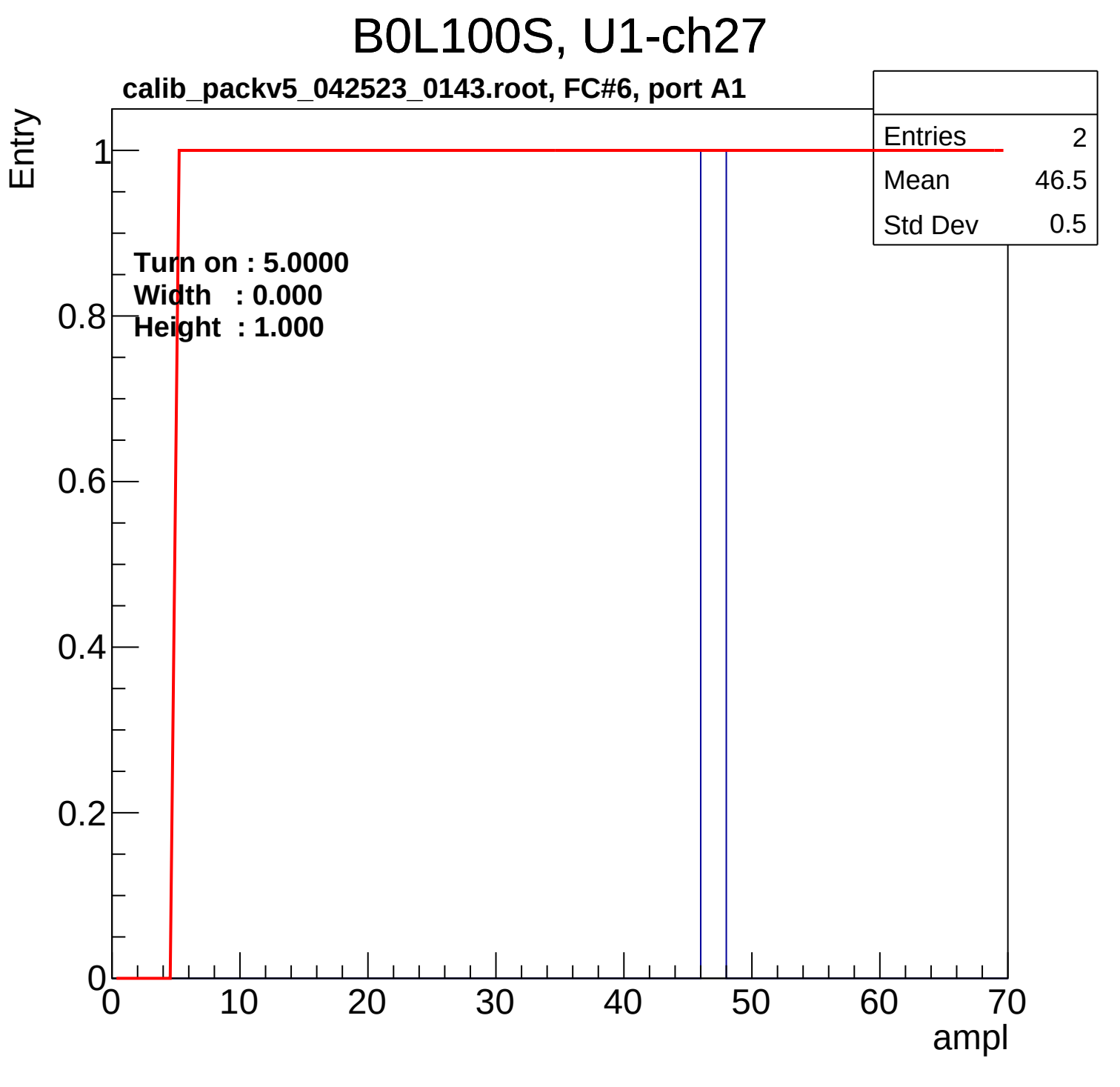
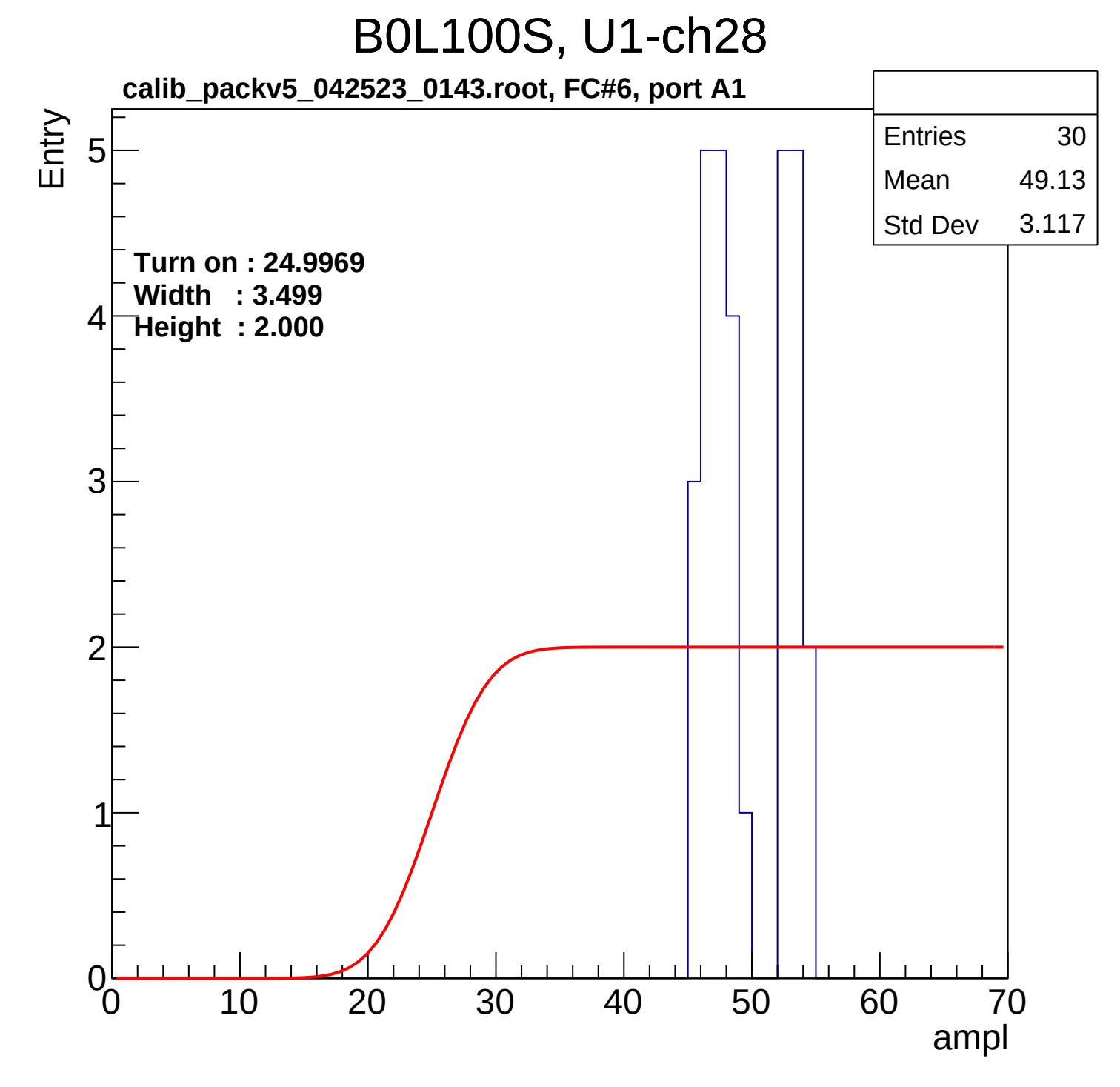
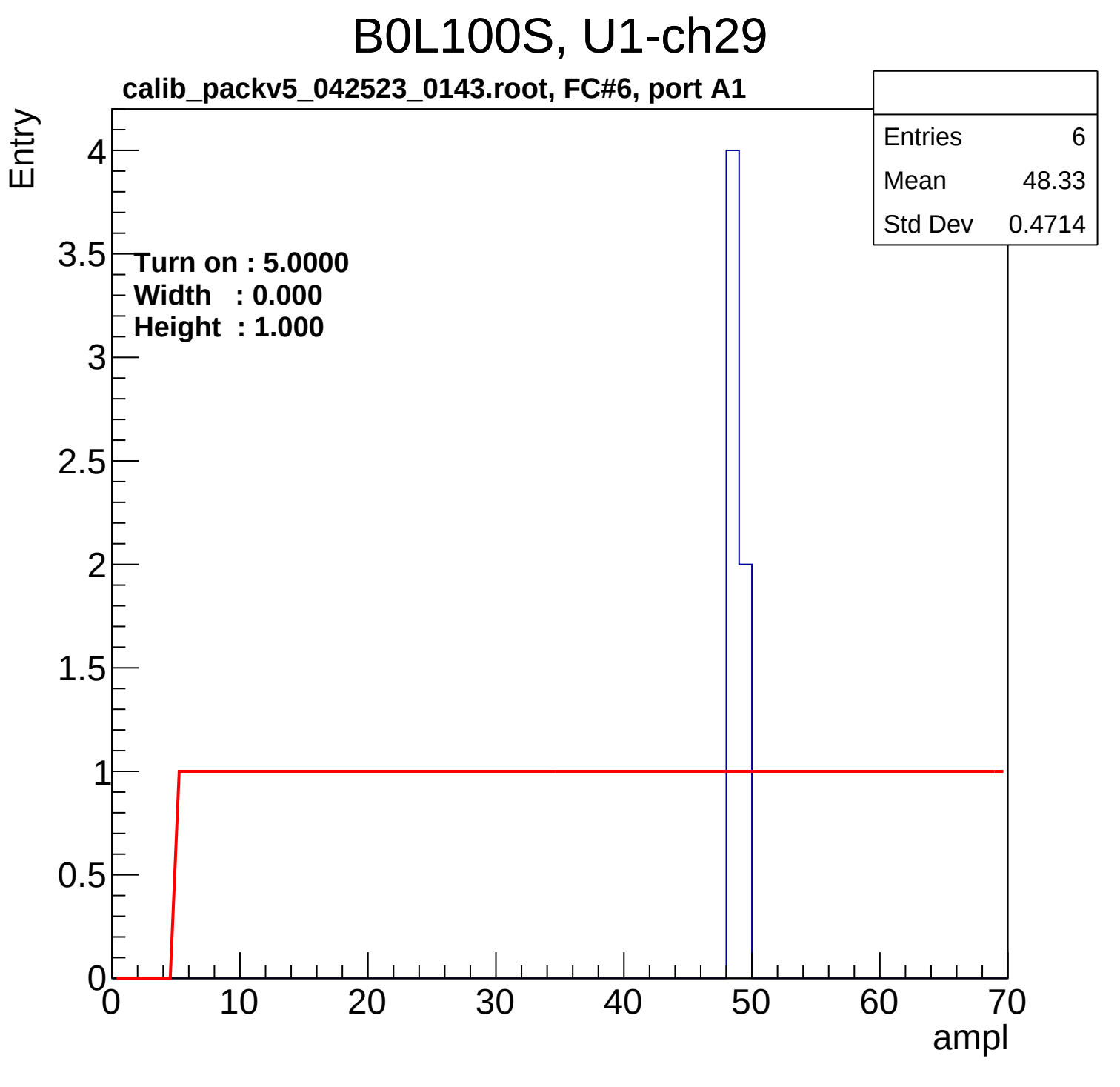
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U1-ch27
calib_packv5_042523_0143.root, FC#6, port A1
Entries 2
Mean 46.5
Std Dev 0.5
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B0L100S, U1-ch28
calib_packv5_042523_0143.root, FC#6, port A1
Entries 30
Mean 49.13
Std Dev 3.117
Turn on : 24.9969
Width : 3.499
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B0L100S, U1-ch29
calib_packv5_042523_0143.root, FC#6, port A1
Entries 6
Mean 48.33
Std Dev 0.4714
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
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0
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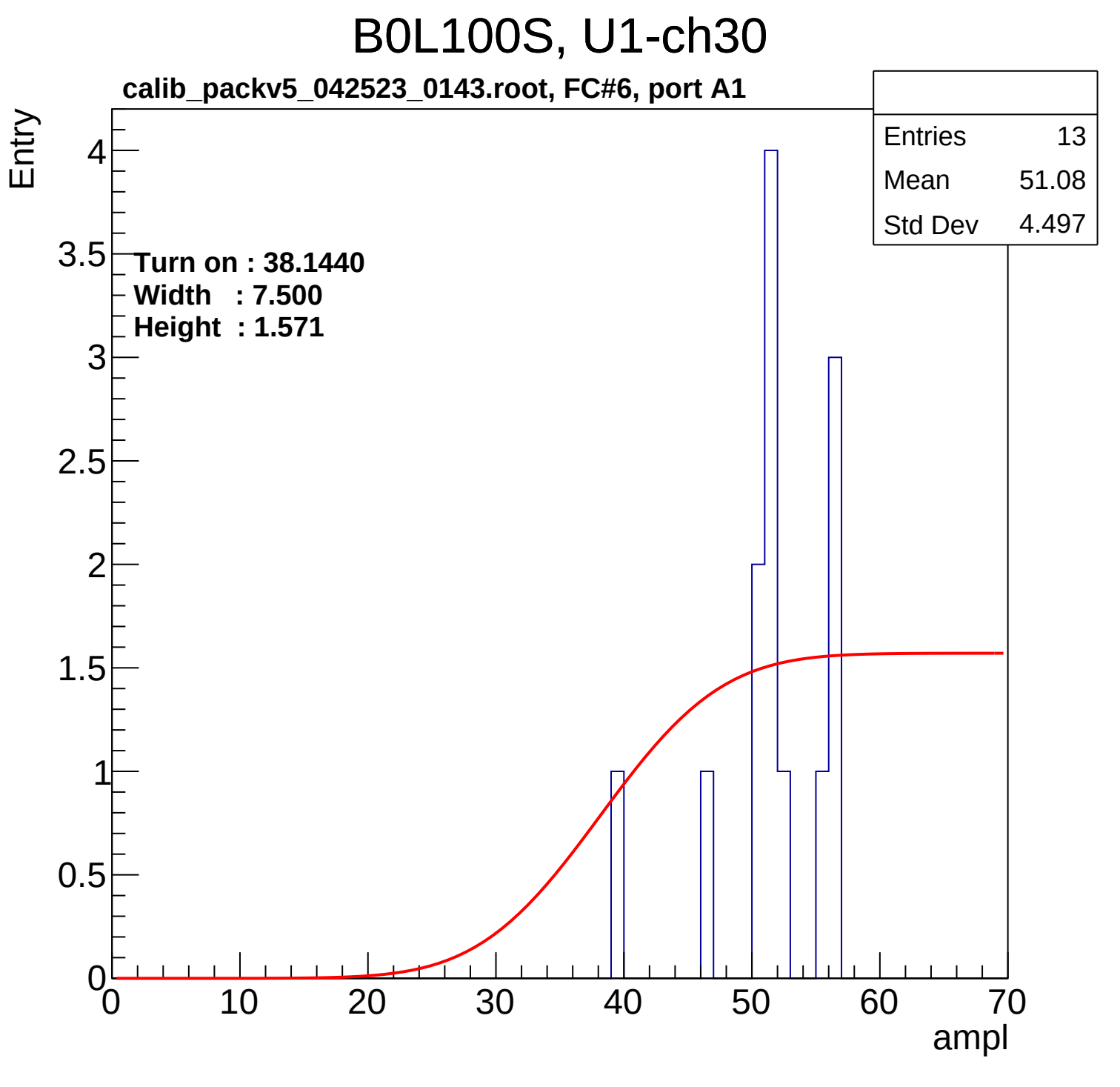
B0L100S, U1-ch30
calib_packv5_042523_0143.root, FC#6, port A1
Entries 13
Mean 51.08
Std Dev 4.497
Turn on : 38.1440
Width : 7.500
Height : 1.571
Entry
ampl
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0.5
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1.5
2
2.5
3
3.5
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0
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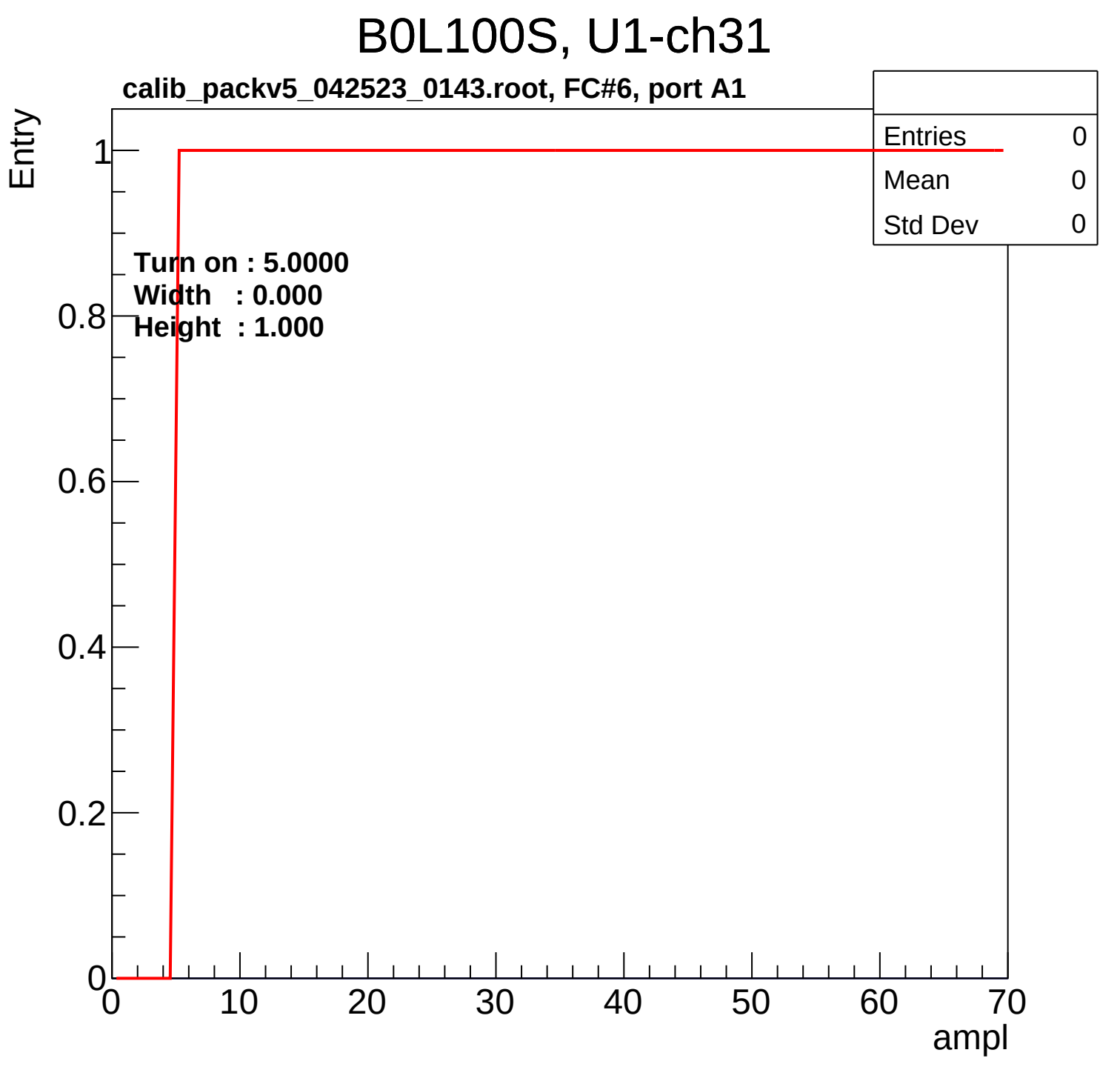
B0L100S, U1-ch31
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
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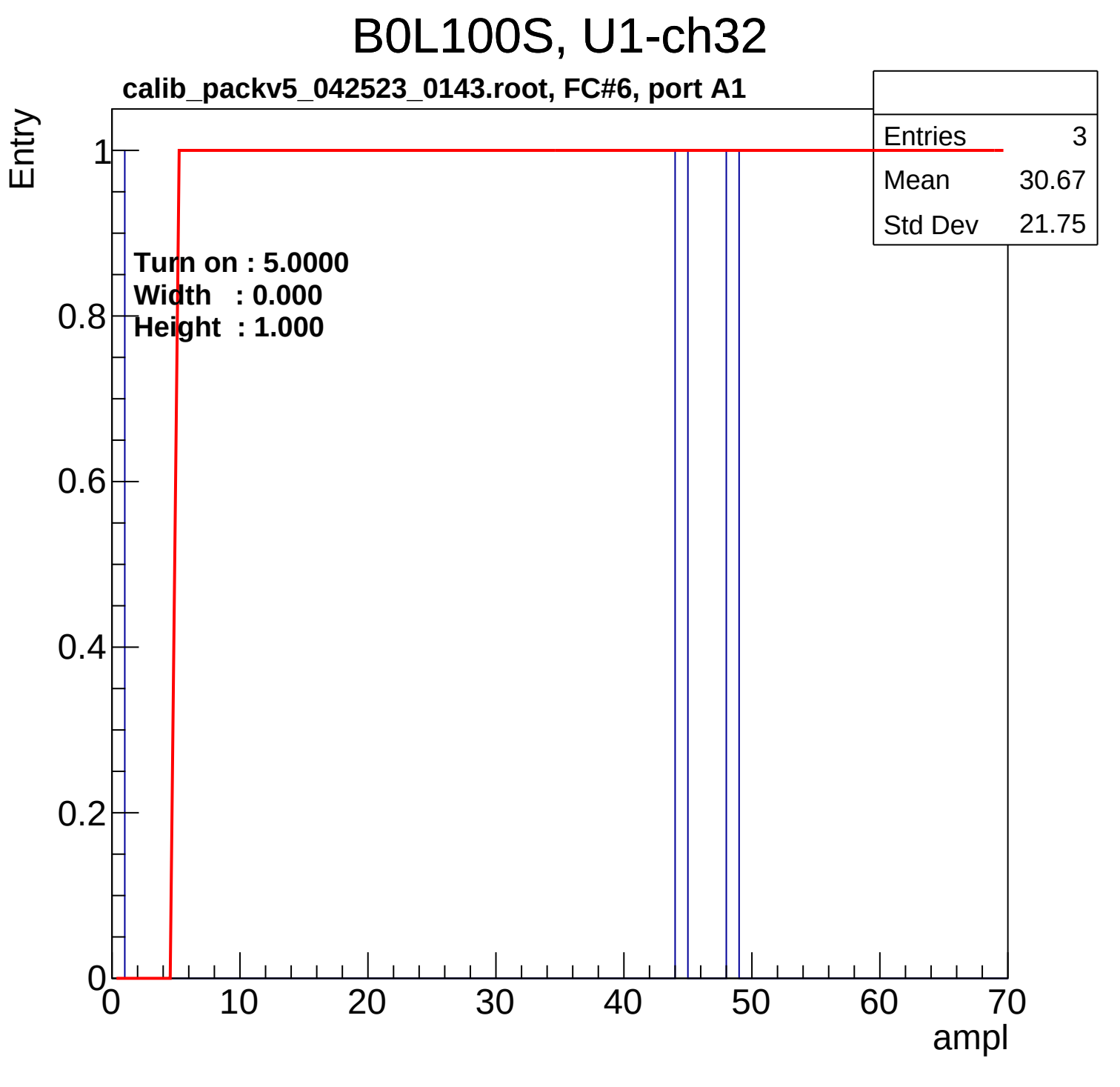
B0L100S, U1-ch32
calib_packv5_042523_0143.root, FC#6, port A1
Entries 3
Mean 30.67
Std Dev 21.75
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
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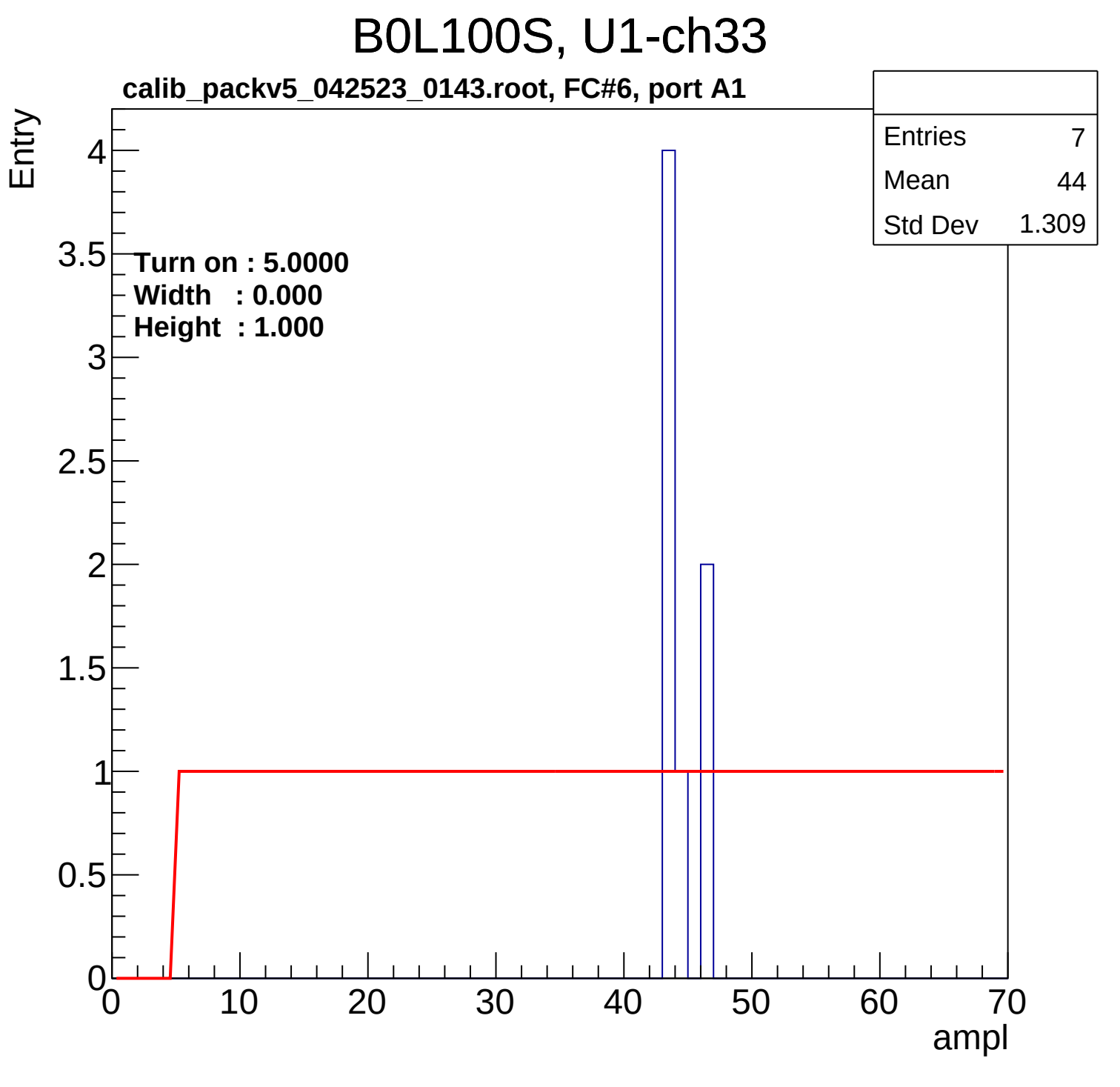
B0L100S, U1-ch33
calib_packv5_042523_0143.root, FC#6, port A1
Entries 7
Mean 44
Std Dev 1.309
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
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0
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40
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60
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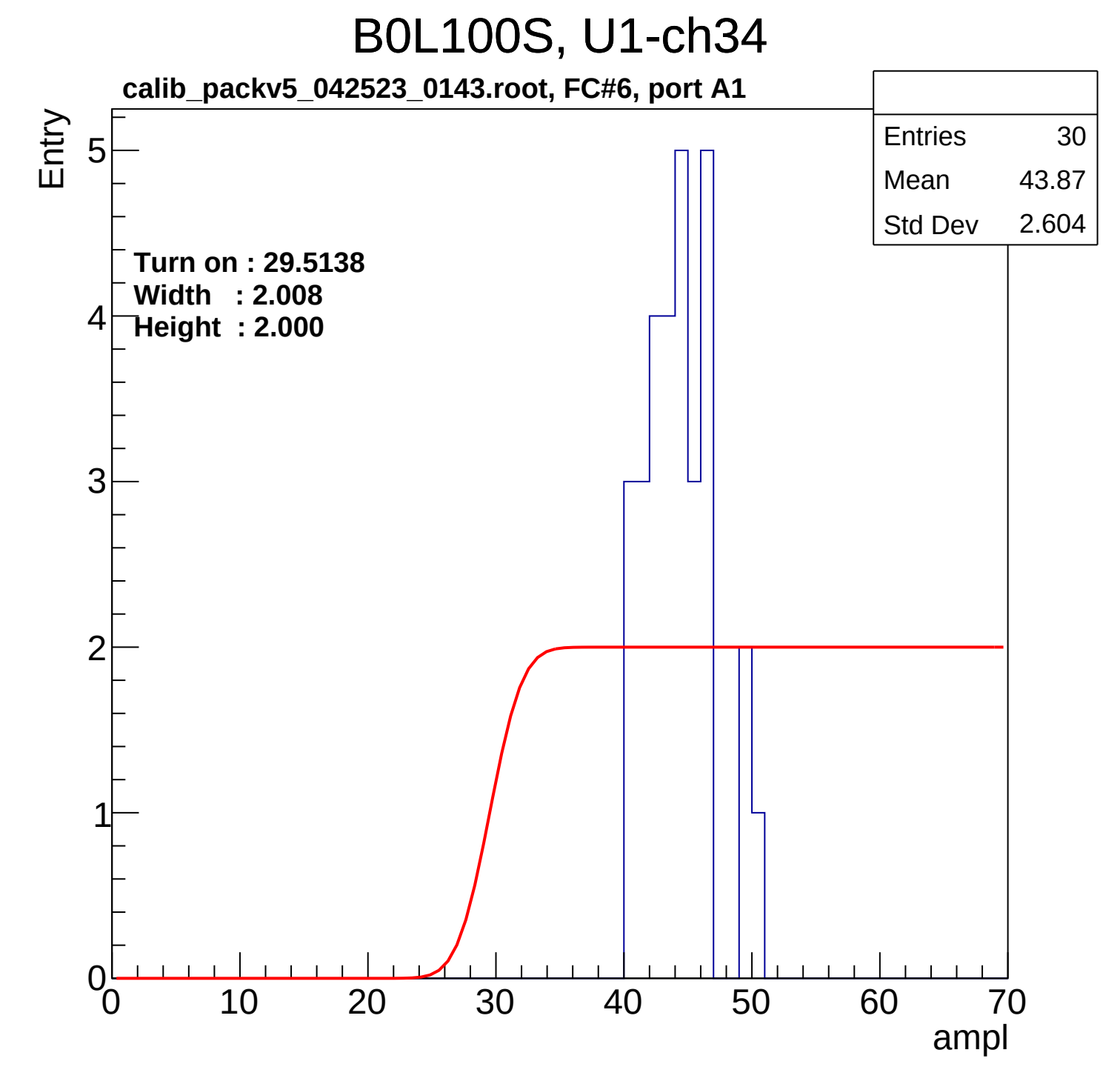
B0L100S, U1-ch34
calib_packv5_042523_0143.root, FC#6, port A1
Entries 30
Mean 43.87
Std Dev 2.604
Turn on : 29.5138
Width : 2.008
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
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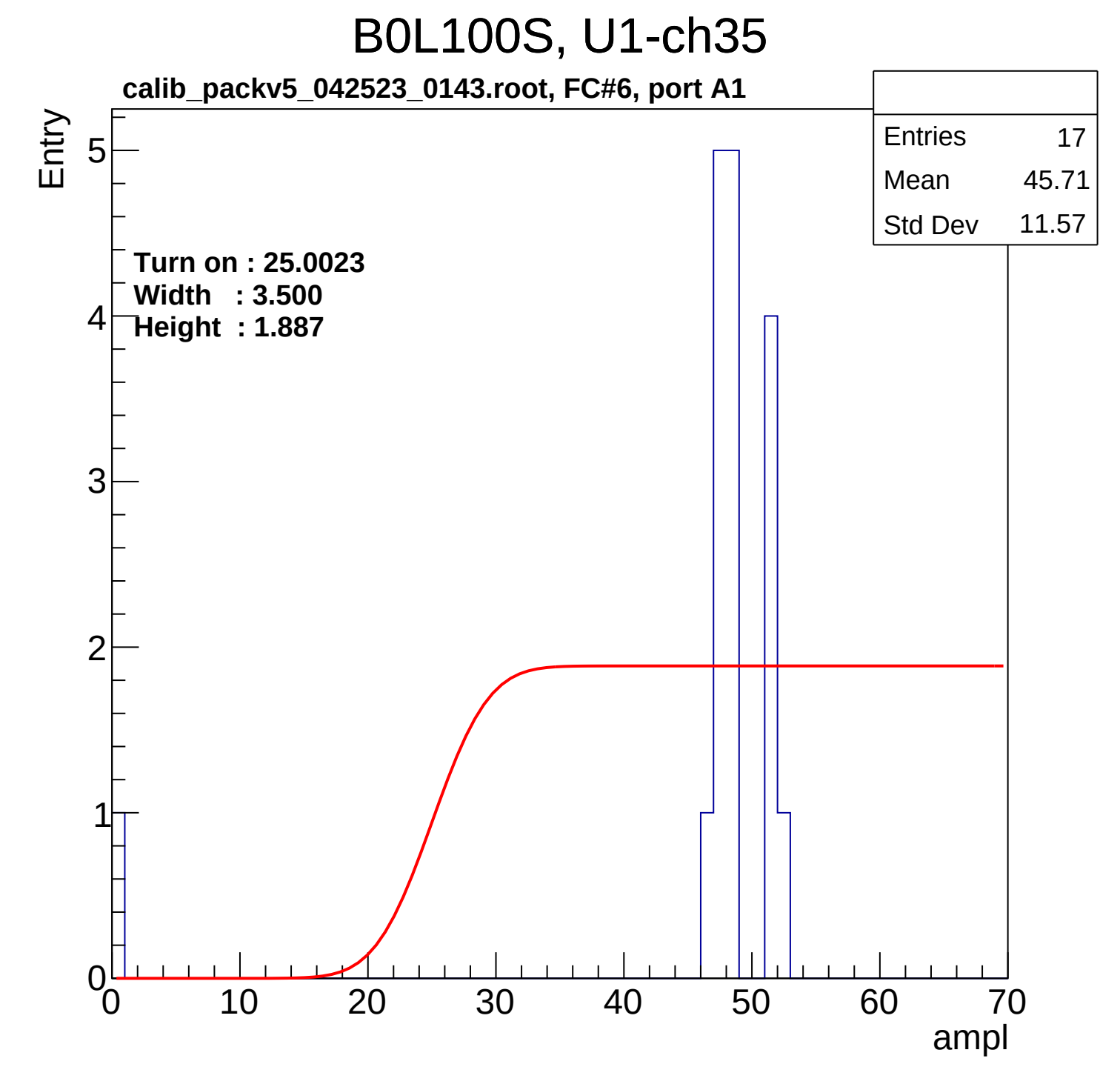
B0L100S, U1-ch35
calib_packv5_042523_0143.root, FC#6, port A1
Entries 17
Mean 45.71
Std Dev 11.57
Turn on : 25.0023
Width : 3.500
Height : 1.887
Entry
ampl
0
1
2
3
4
5
0
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40
50
60
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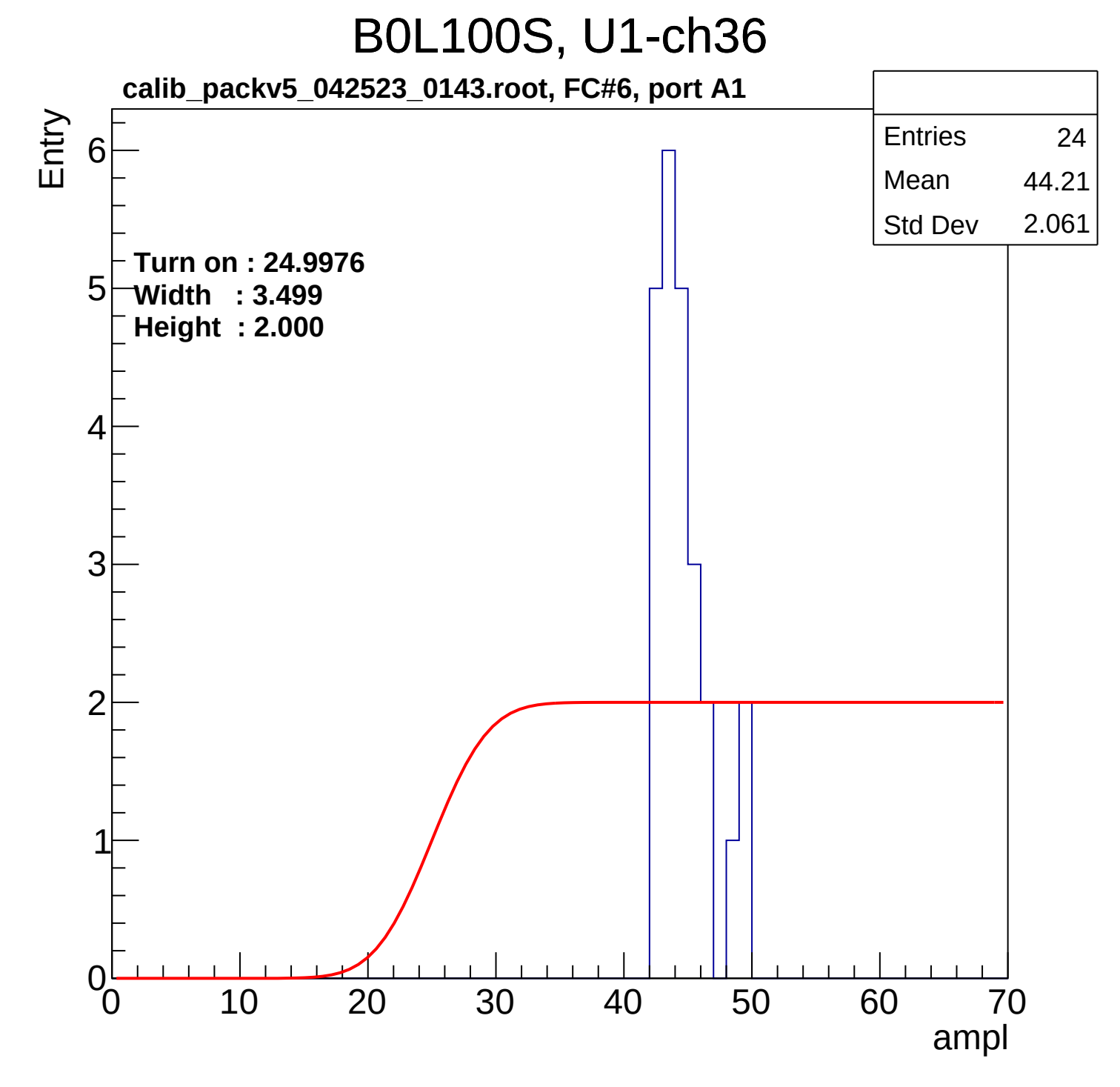
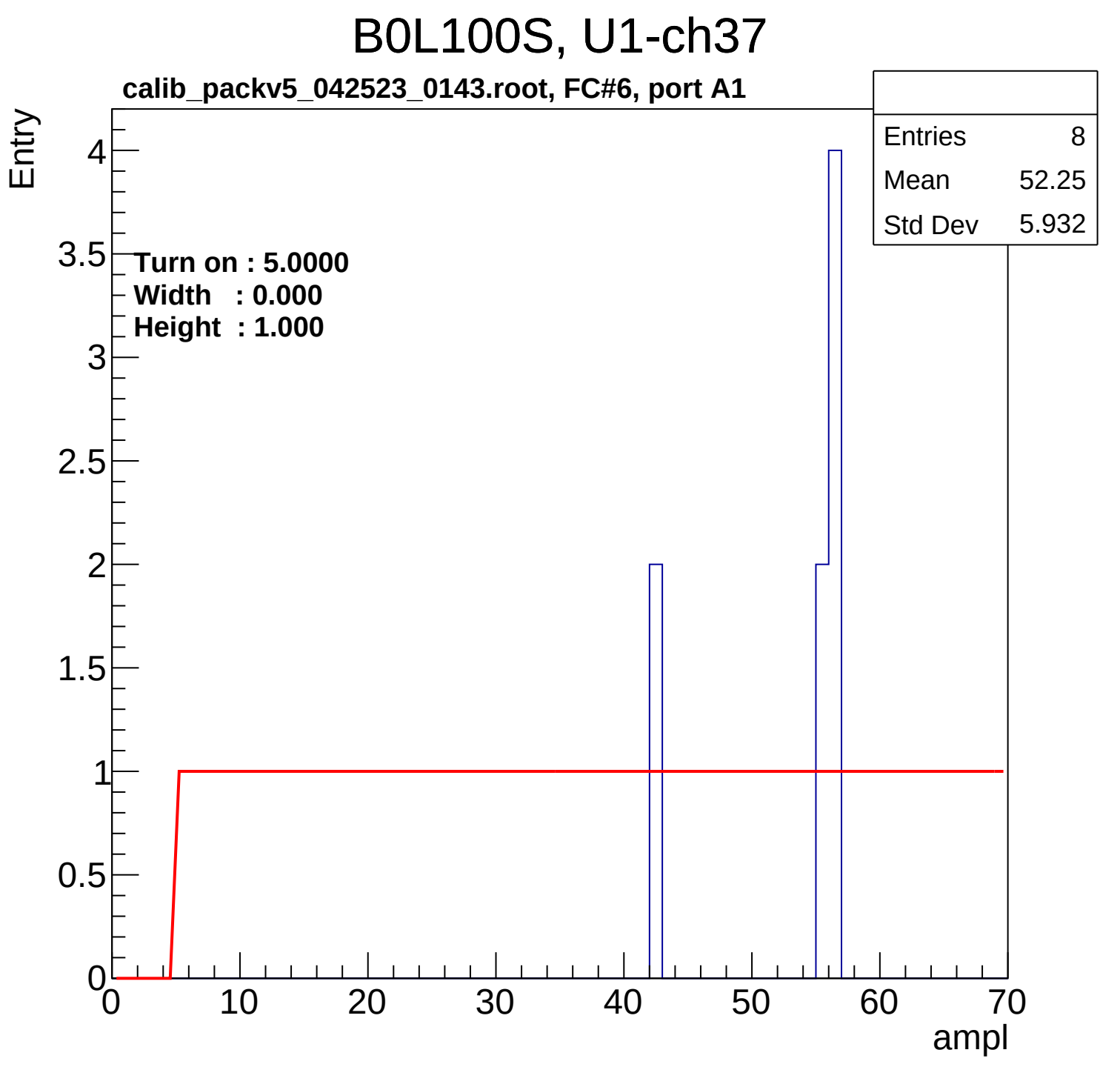
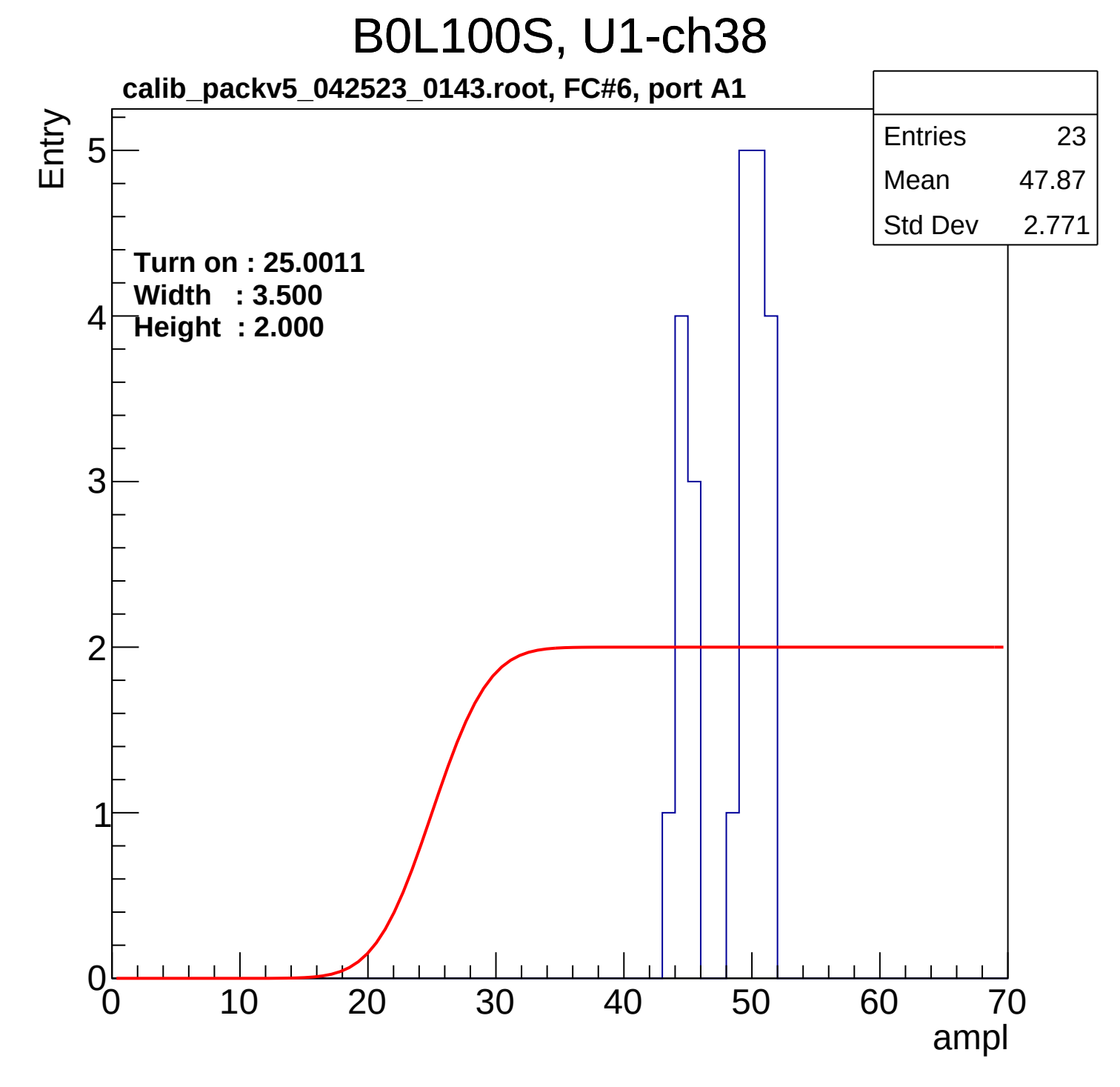

B0L100S, U1-ch36
calib_packv5_042523_0143.root, FC#6, port A1
Entries 24
Mean 44.21
Std Dev 2.061
Turn on : 24.9976
Width : 3.499
Height : 2.000
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B0L100S, U1-ch37
calib_packv5_042523_0143.root, FC#6, port A1
Entries 8
Mean 52.25
Std Dev 5.932
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B0L100S, U1-ch38
calib_packv5_042523_0143.root, FC#6, port A1
Entries 23
Mean 47.87
Std Dev 2.771
Turn on : 25.0011
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
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20
30
40
50
60
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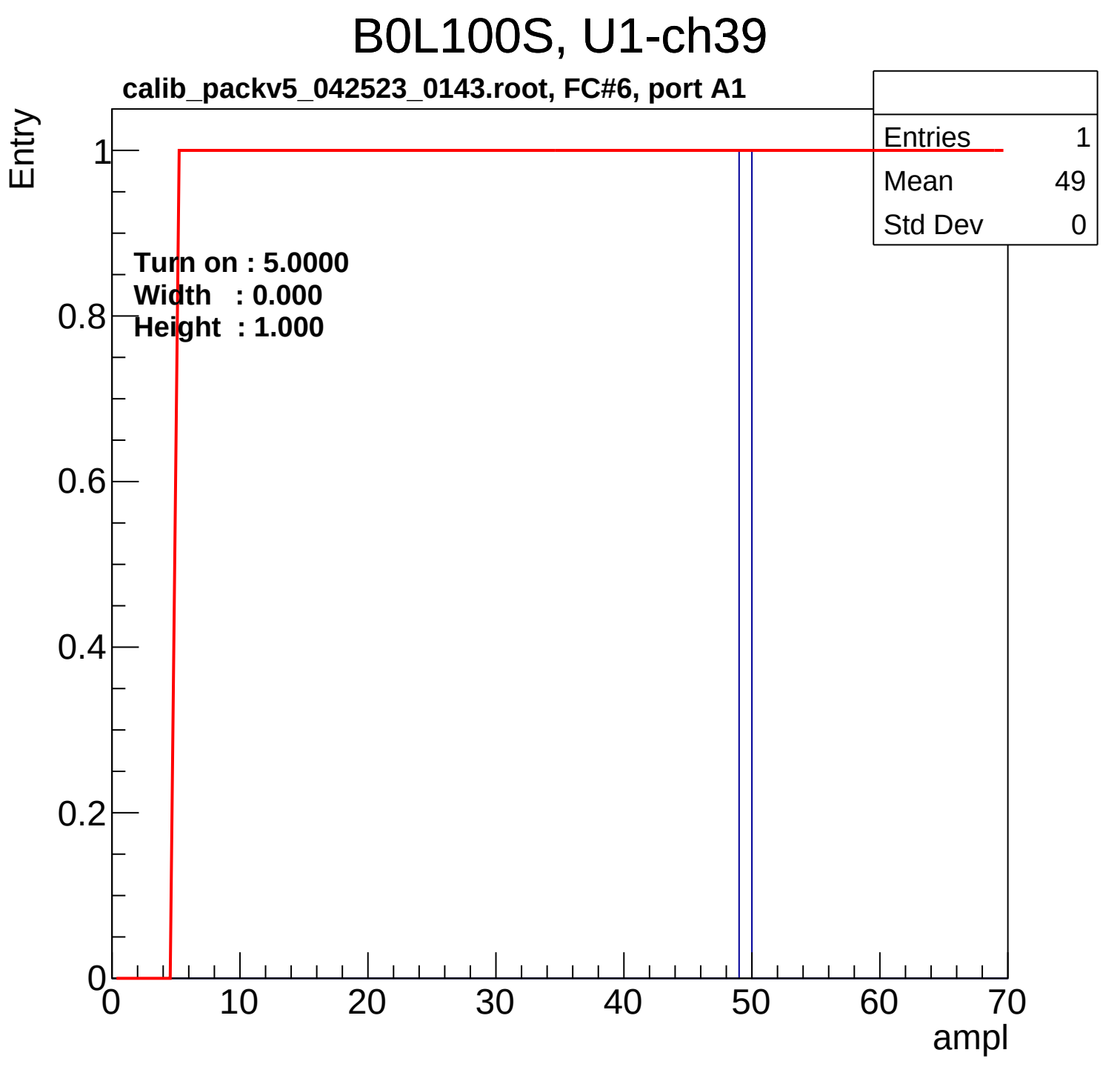
B0L100S, U1-ch39
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 49
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
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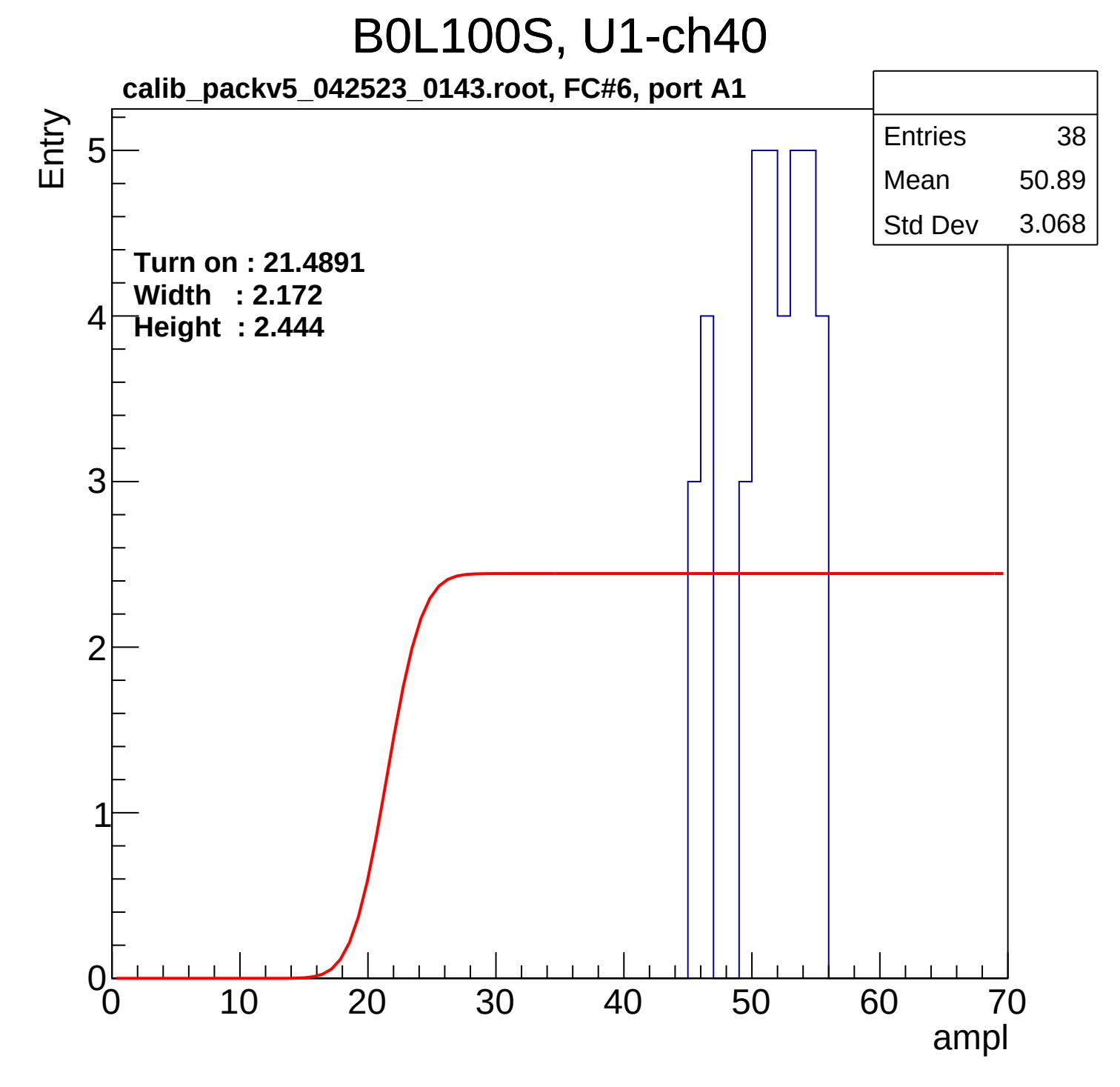
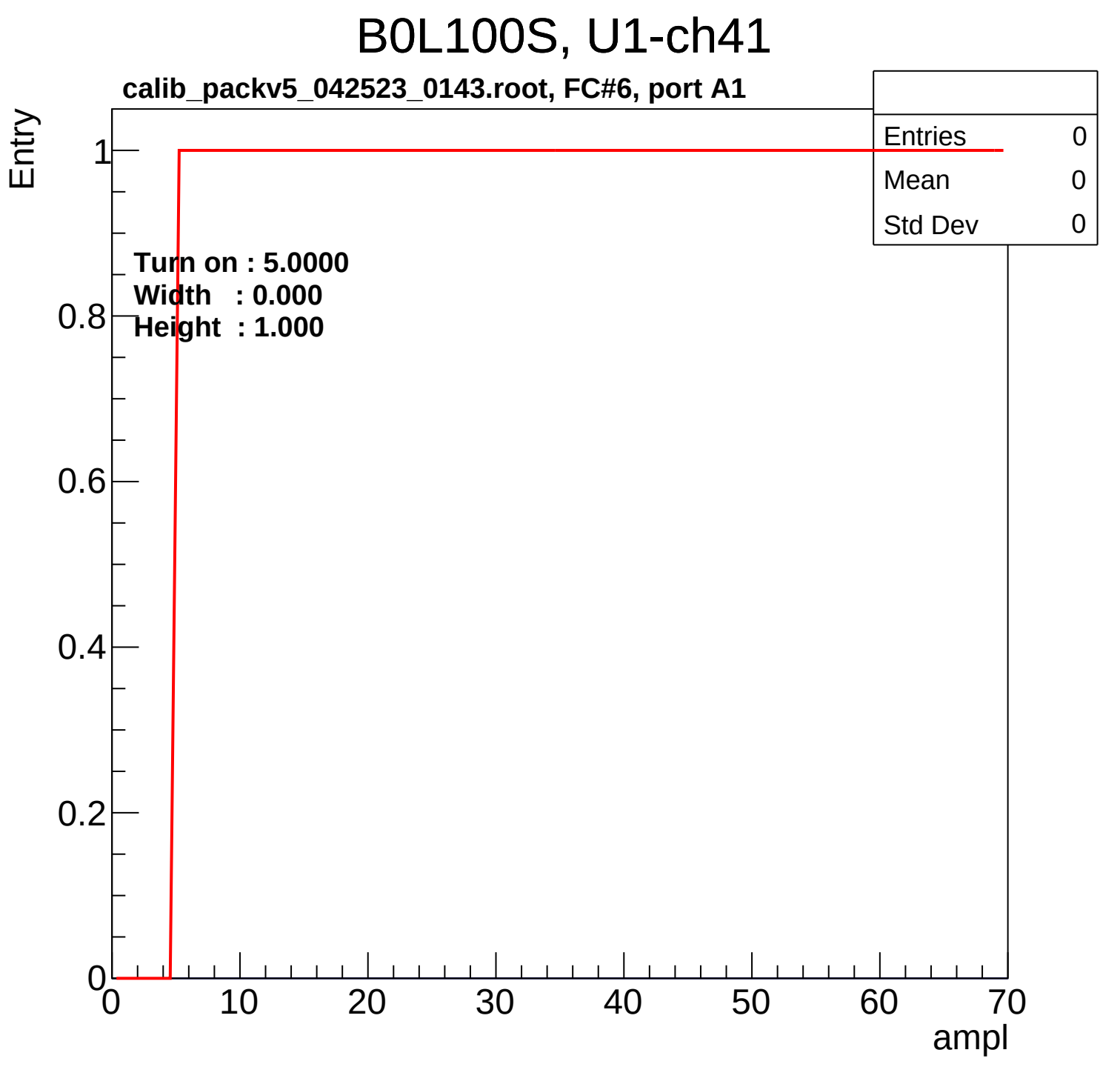
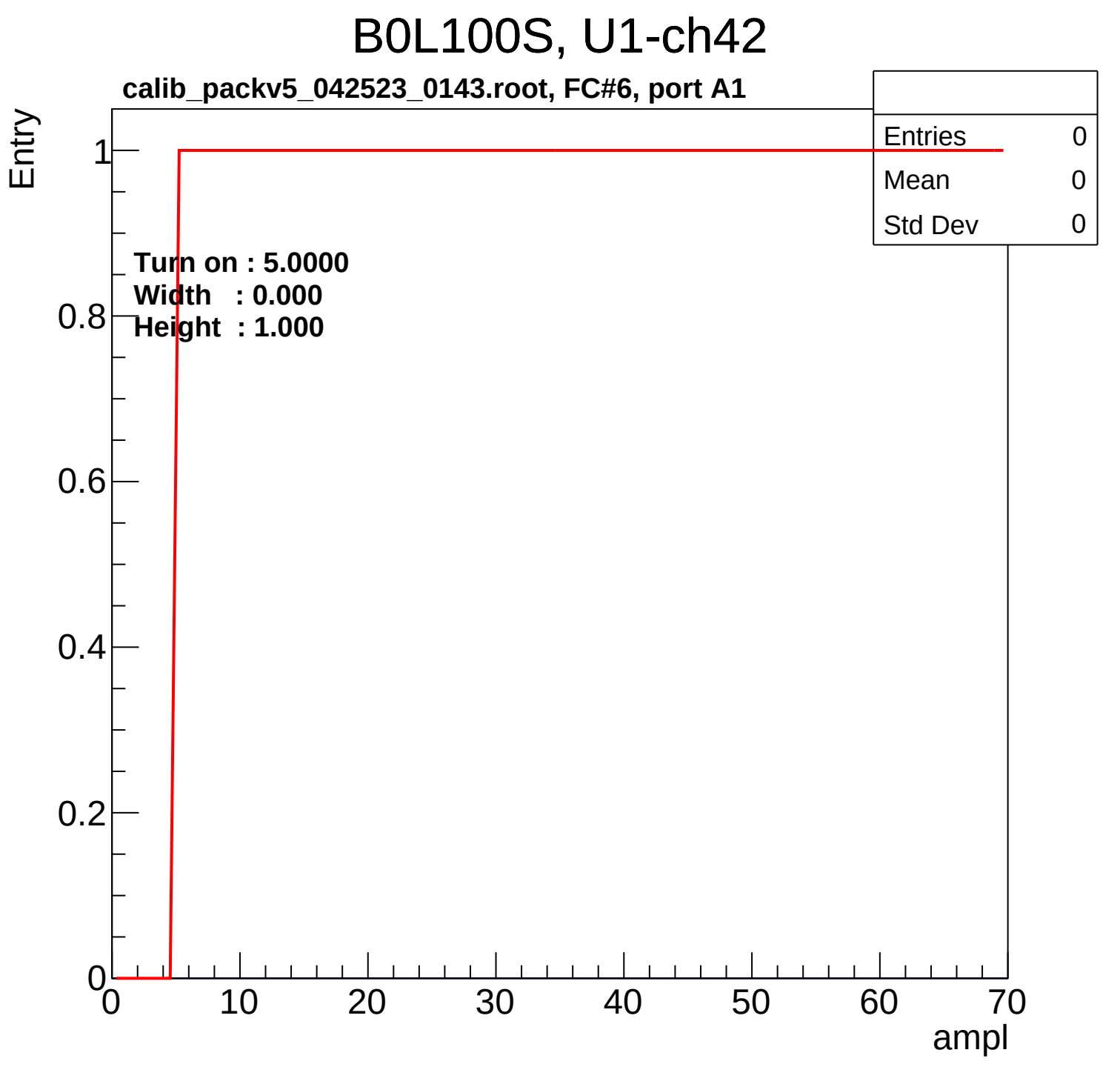
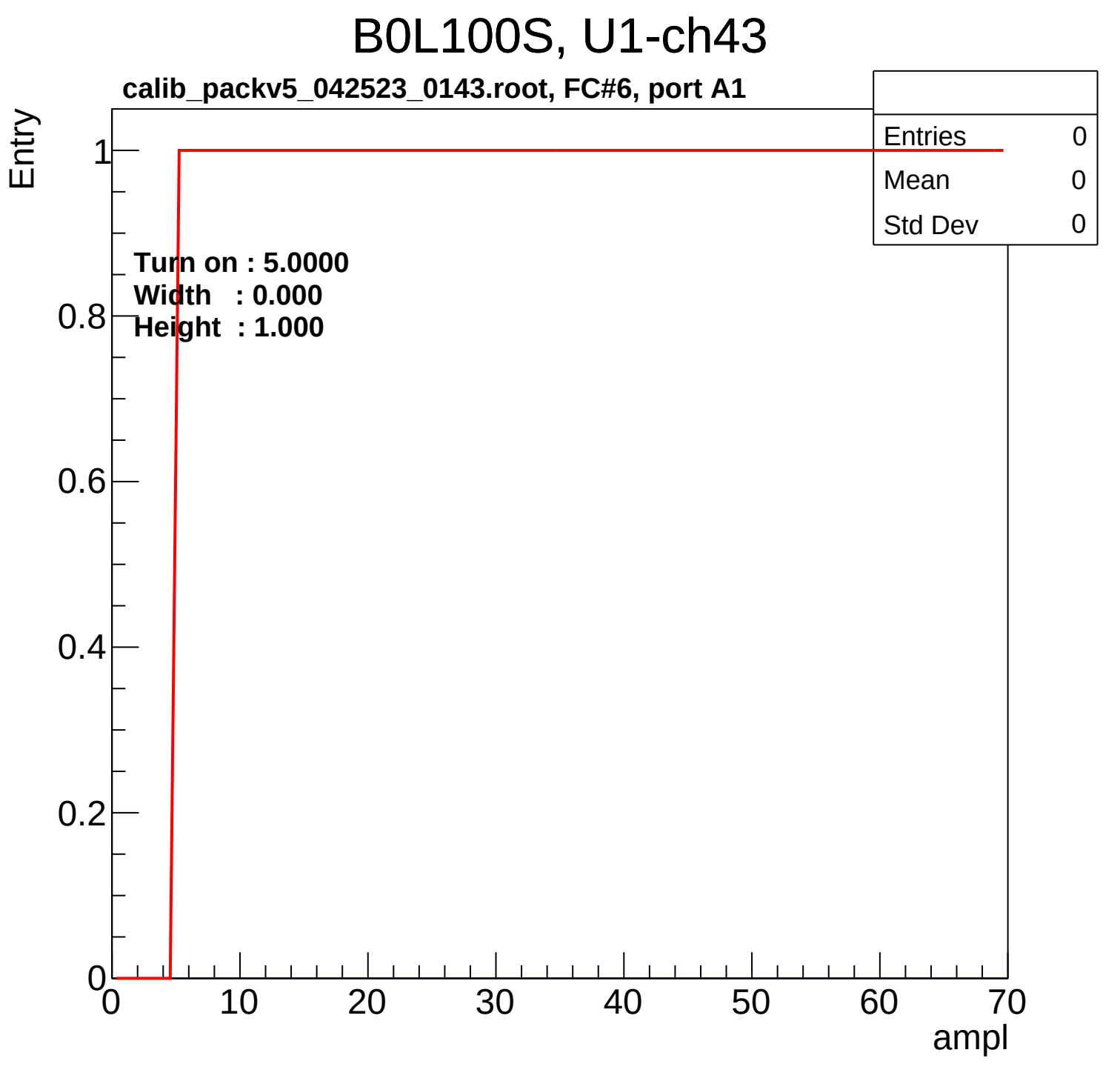
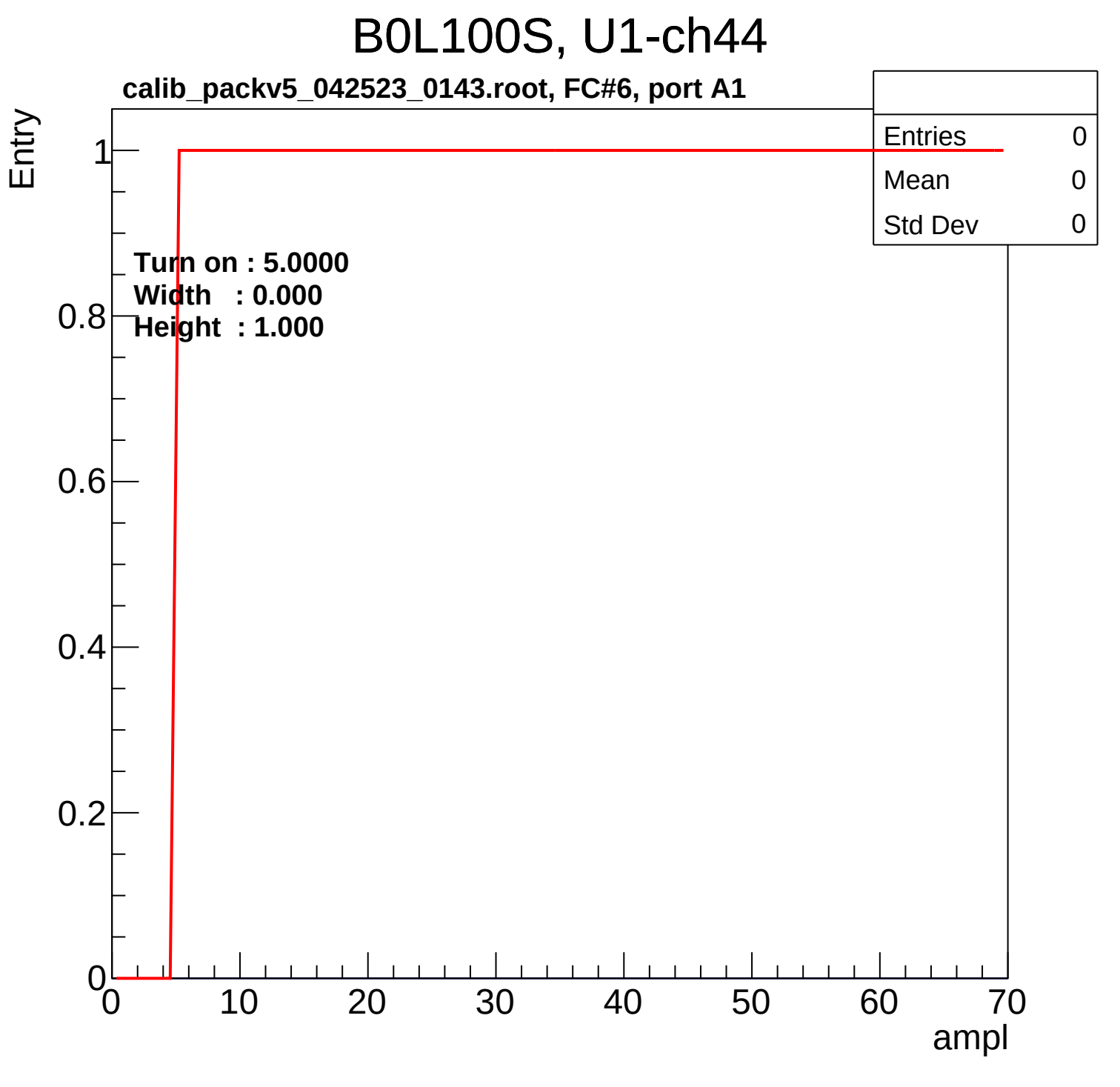
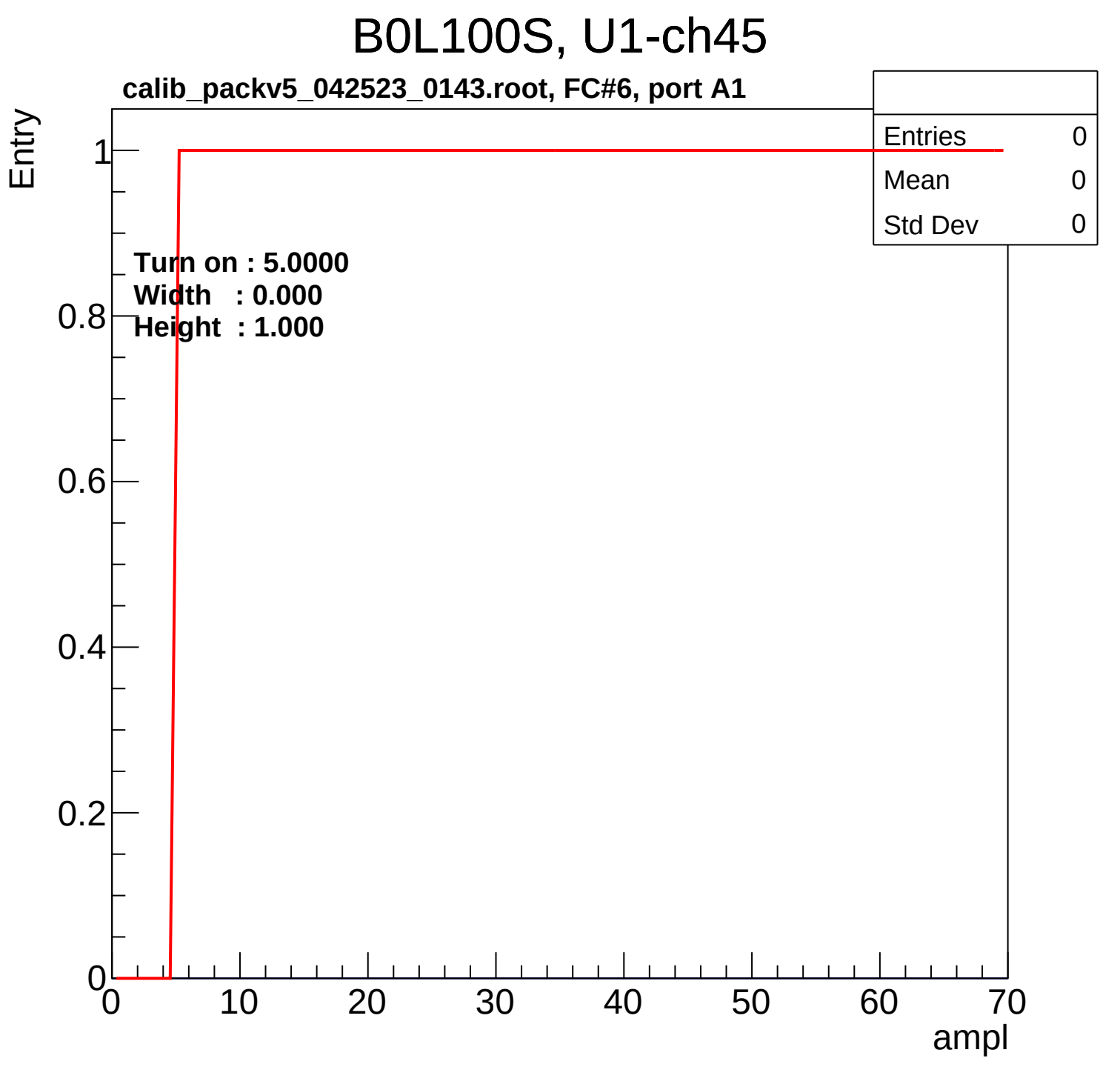

B0L100S, U1-ch40
calib_packv5_042523_0143.root, FC#6, port A1
Entries 38
Mean 50.89
Std Dev 3.068
Turn on : 21.4891
Width : 2.172
Height : 2.444
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

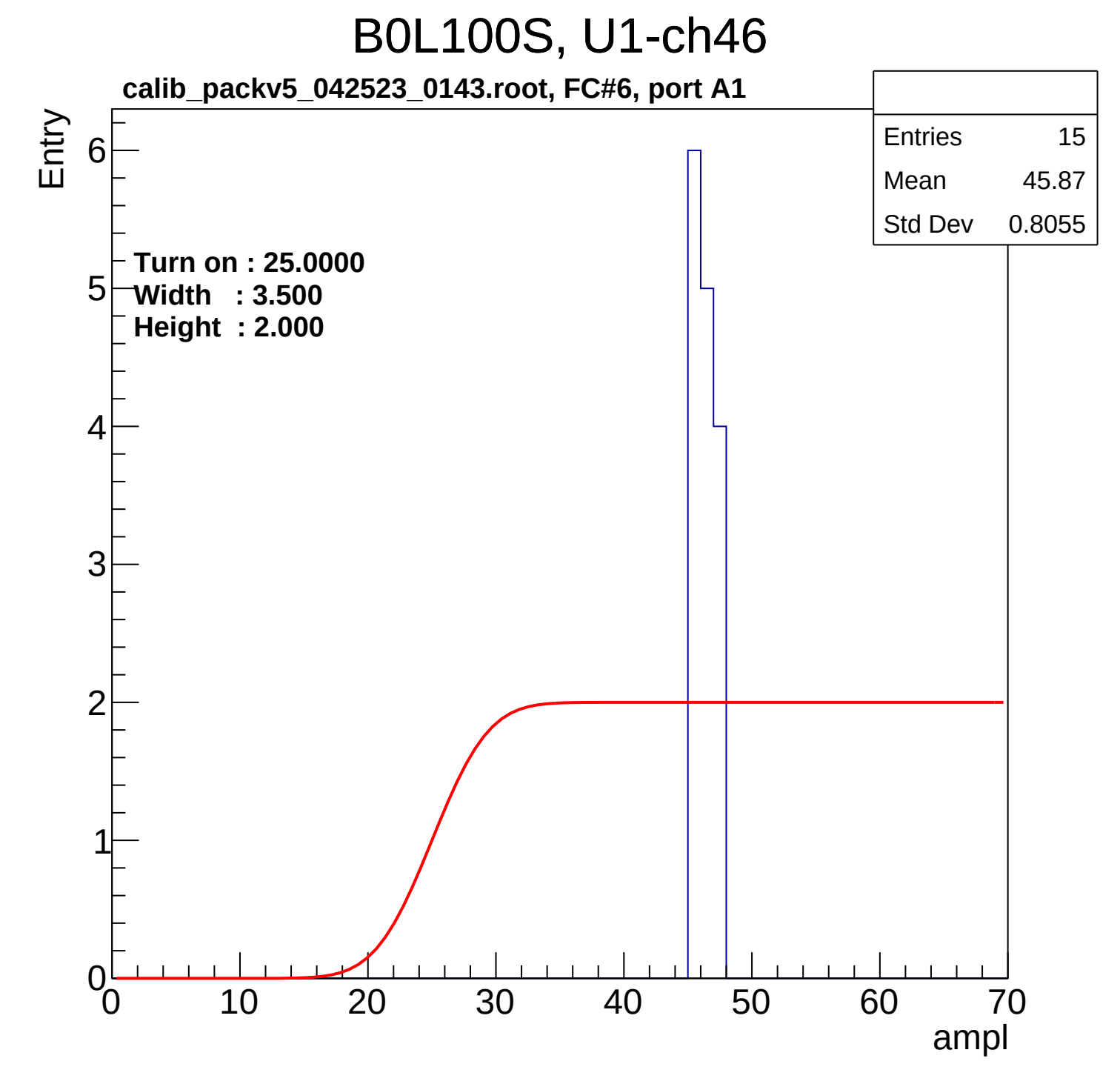

B0L100S, U1-ch41
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U1-ch42
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U1-ch43
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U1-ch44
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B0L100S, U1-ch45
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U1-ch46
calib_packv5_042523_0143.root, FC#6, port A1
Entries 15
Mean 45.87
Std Dev 0.8055
Turn on : 25.0000
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
6
0
10
20
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40
50
60
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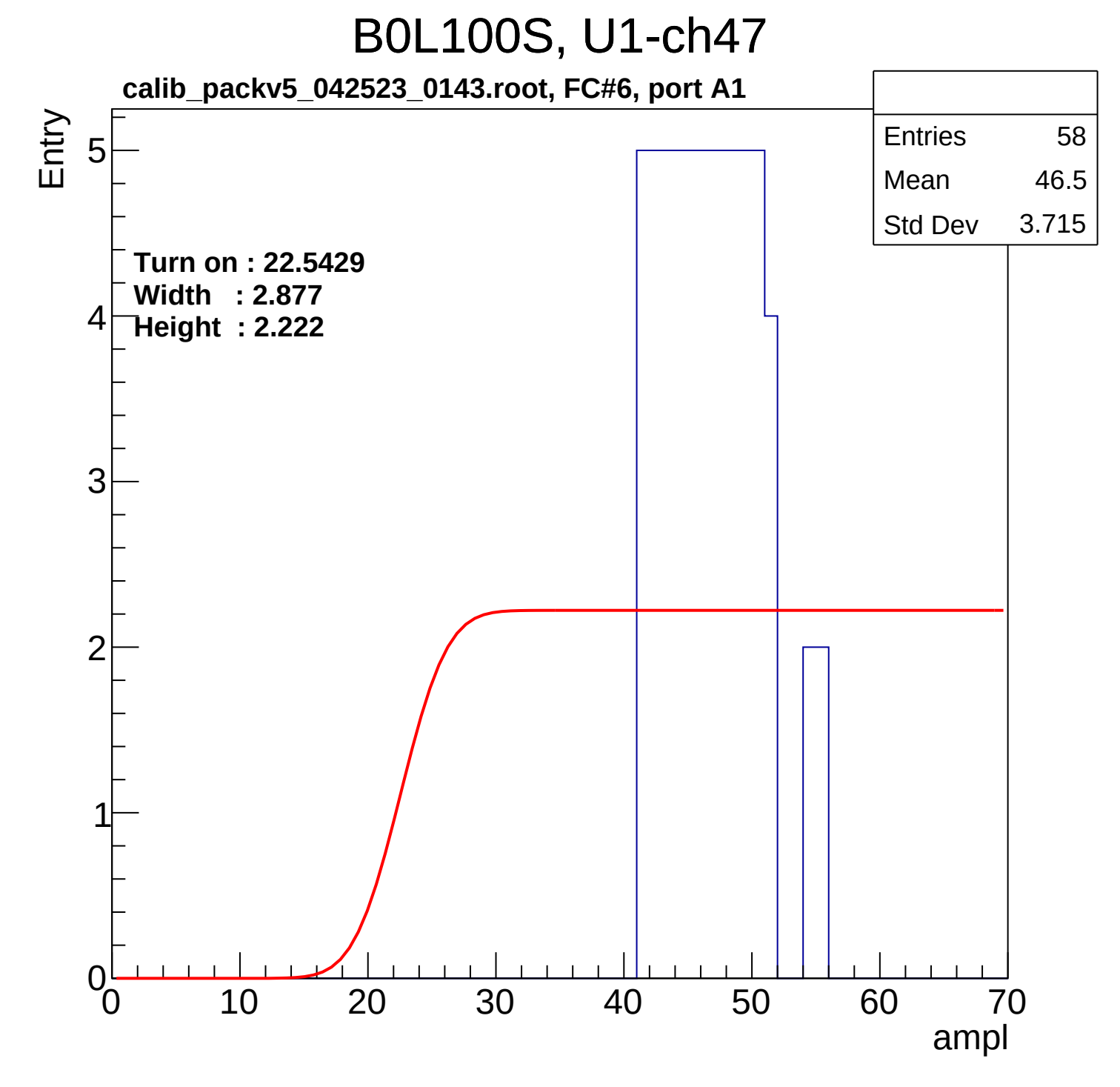
B0L100S, U1-ch47
calib_packv5_042523_0143.root, FC#6, port A1
Entries 58
Mean 46.5
Std Dev 3.715
Turn on : 22.5429
Width : 2.877
Height : 2.222
Entry
ampl
0
1
2
3
4
5
0
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20
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40
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60
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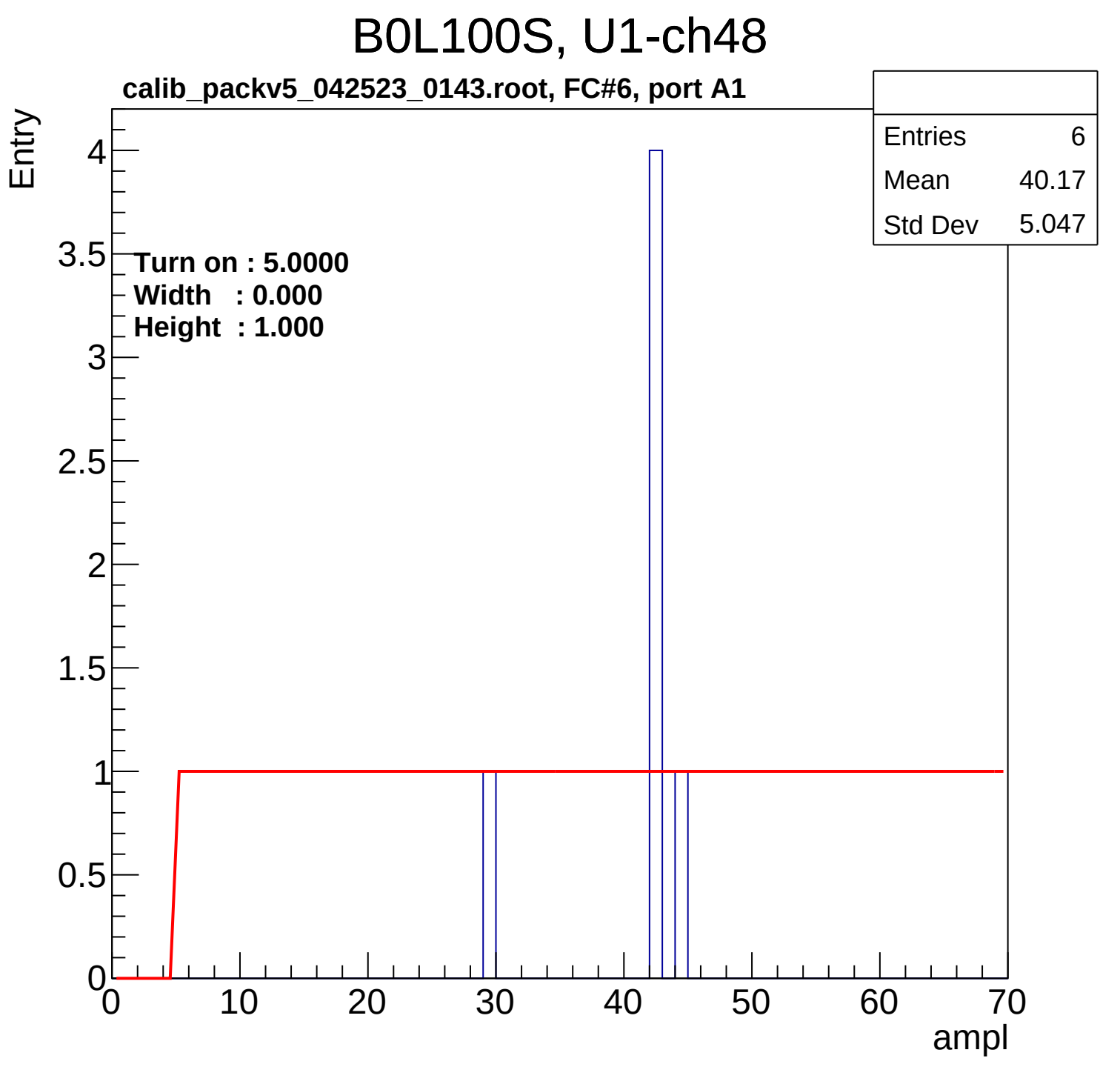
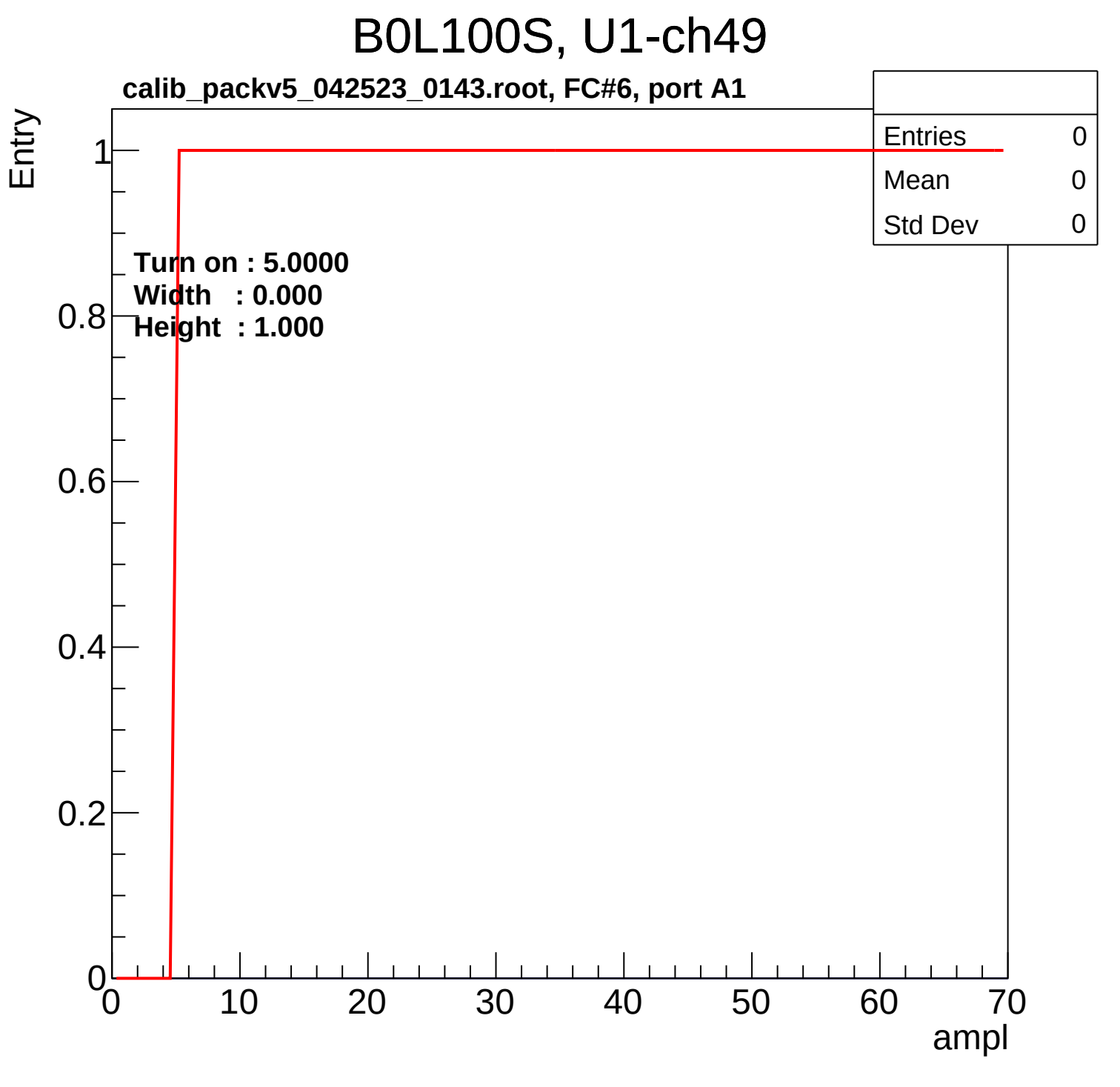
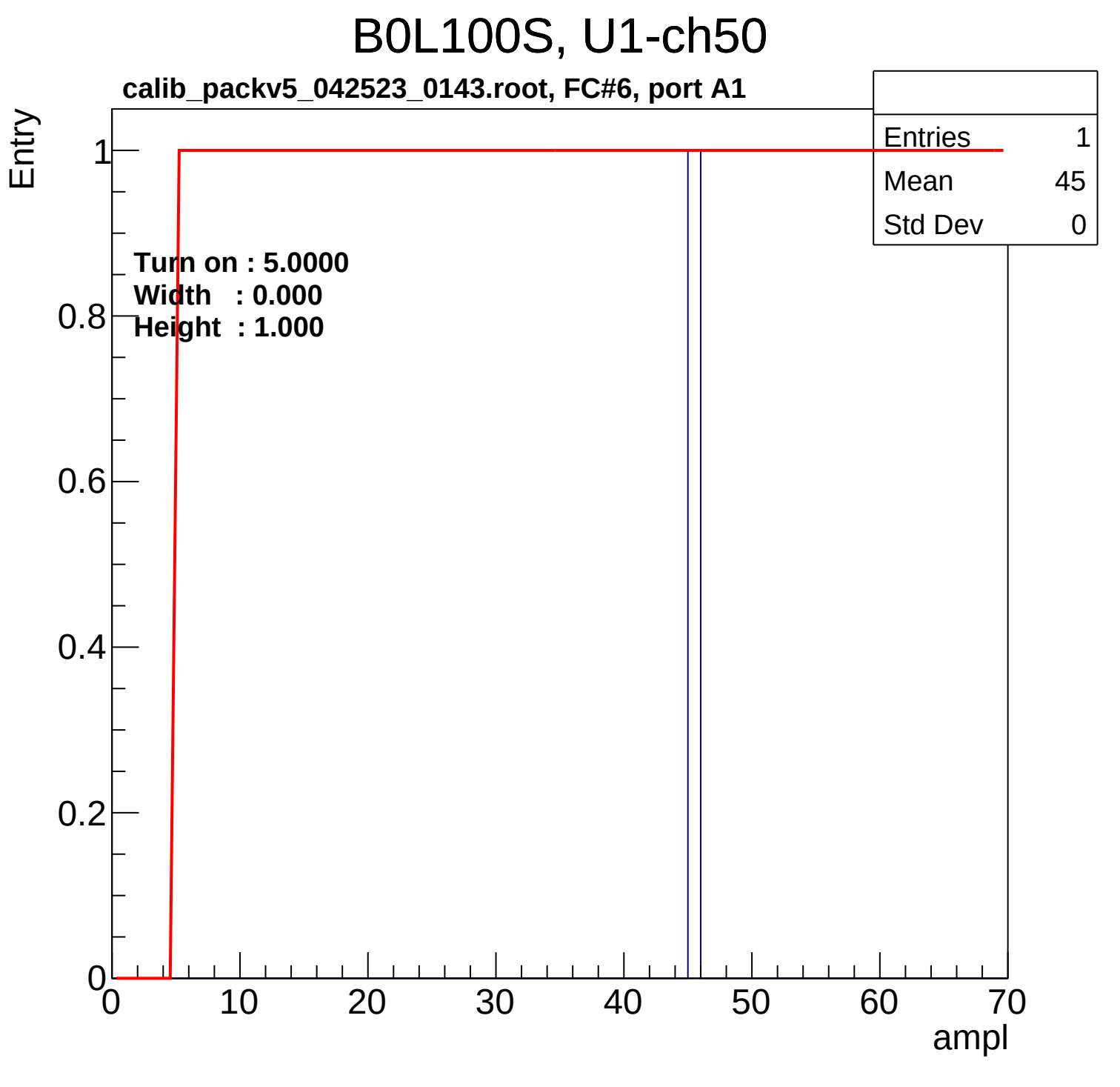
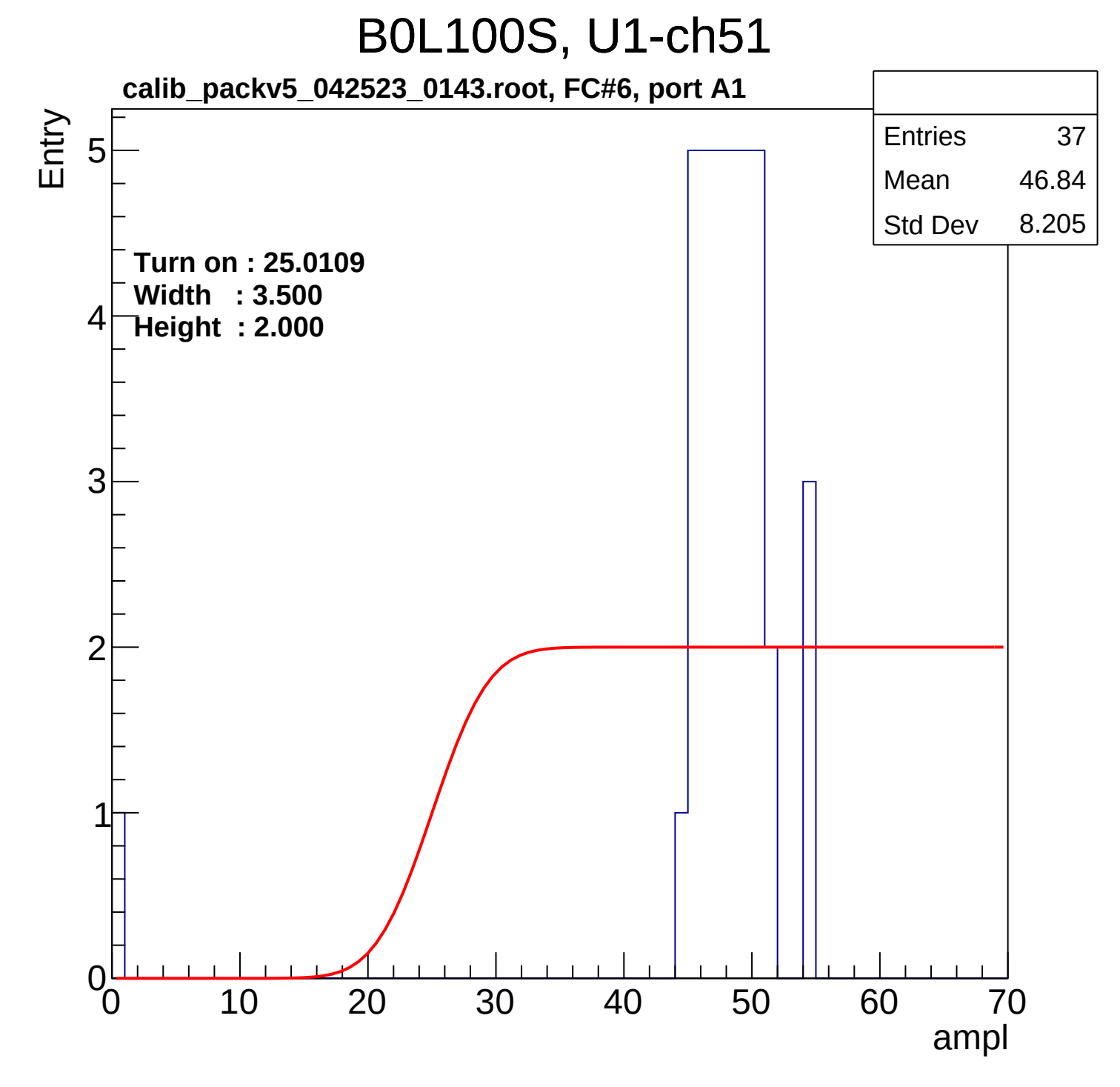
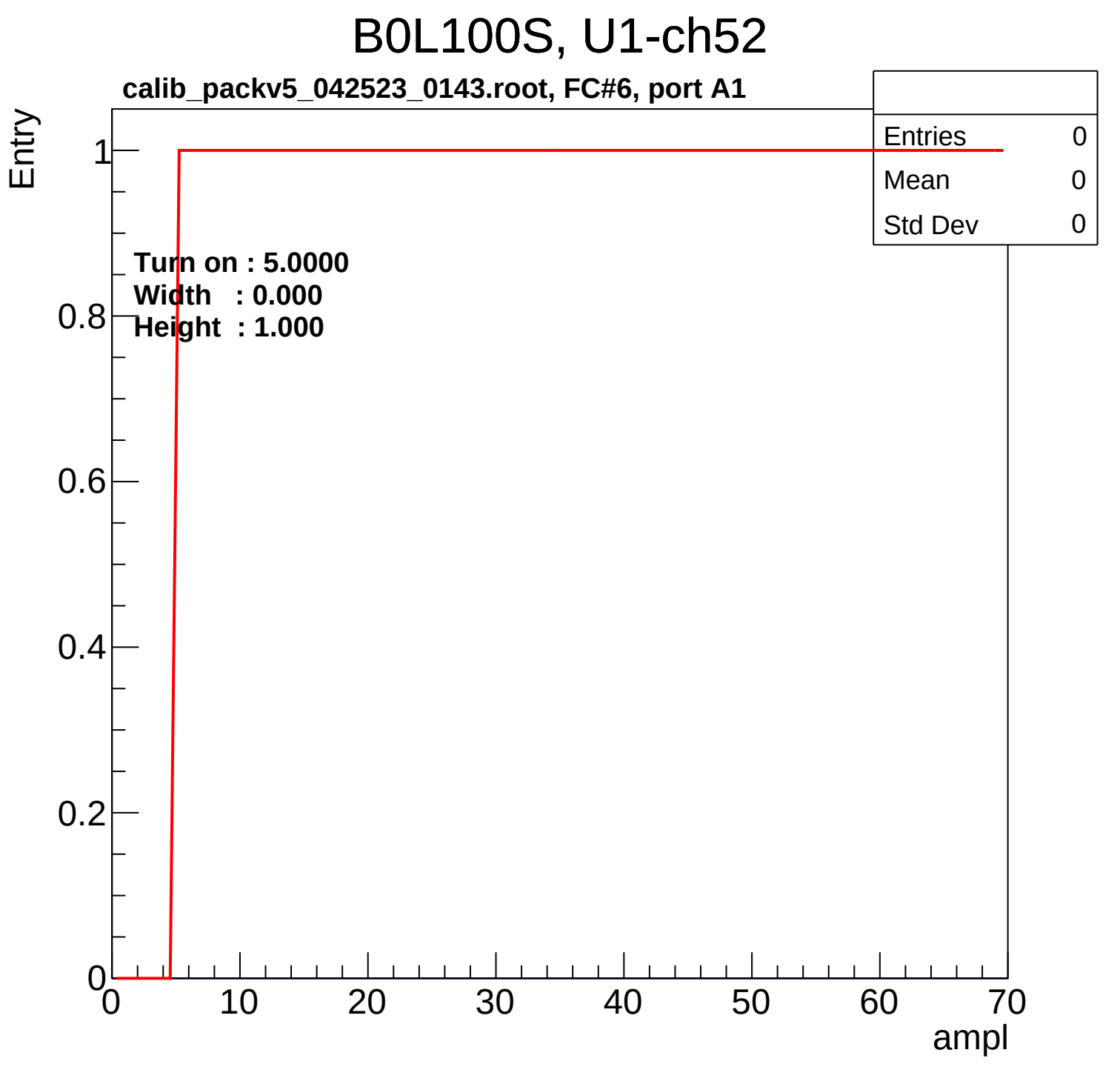
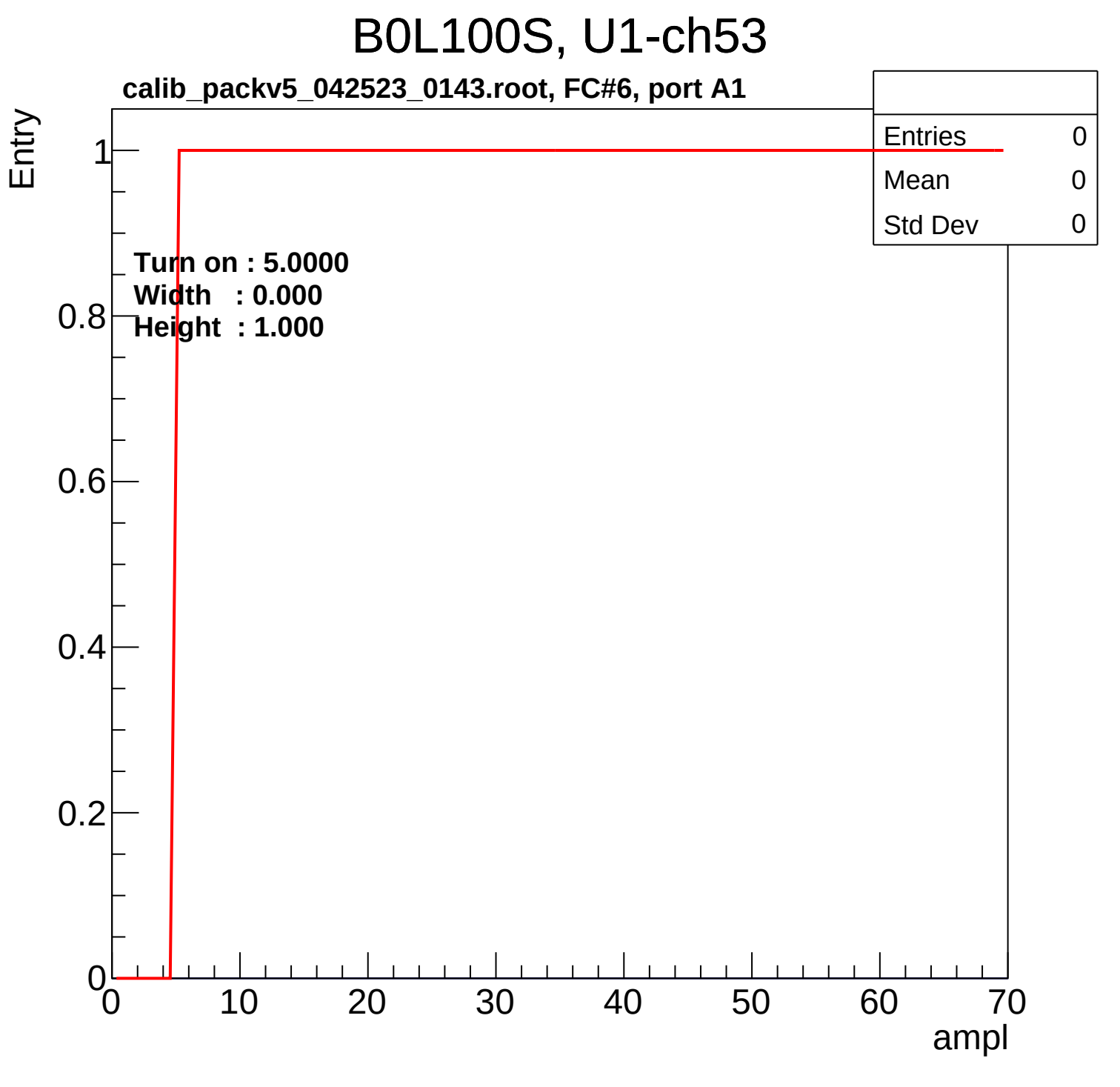

B0L100S, U1-ch48
calib_packv5_042523_0143.root, FC#6, port A1
Entries 6
Mean 40.17
Std Dev 5.047
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B0L100S, U1-ch49
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U1-ch50
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 45
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B0L100S, U1-ch51
calib_packv5_042523_0143.root, FC#6, port A1
Entries 37
Mean 46.84
Std Dev 8.205
Turn on : 25.0109
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B0L100S, U1-ch52
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U1-ch53
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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0.8
0.6
0.4
0.2
0
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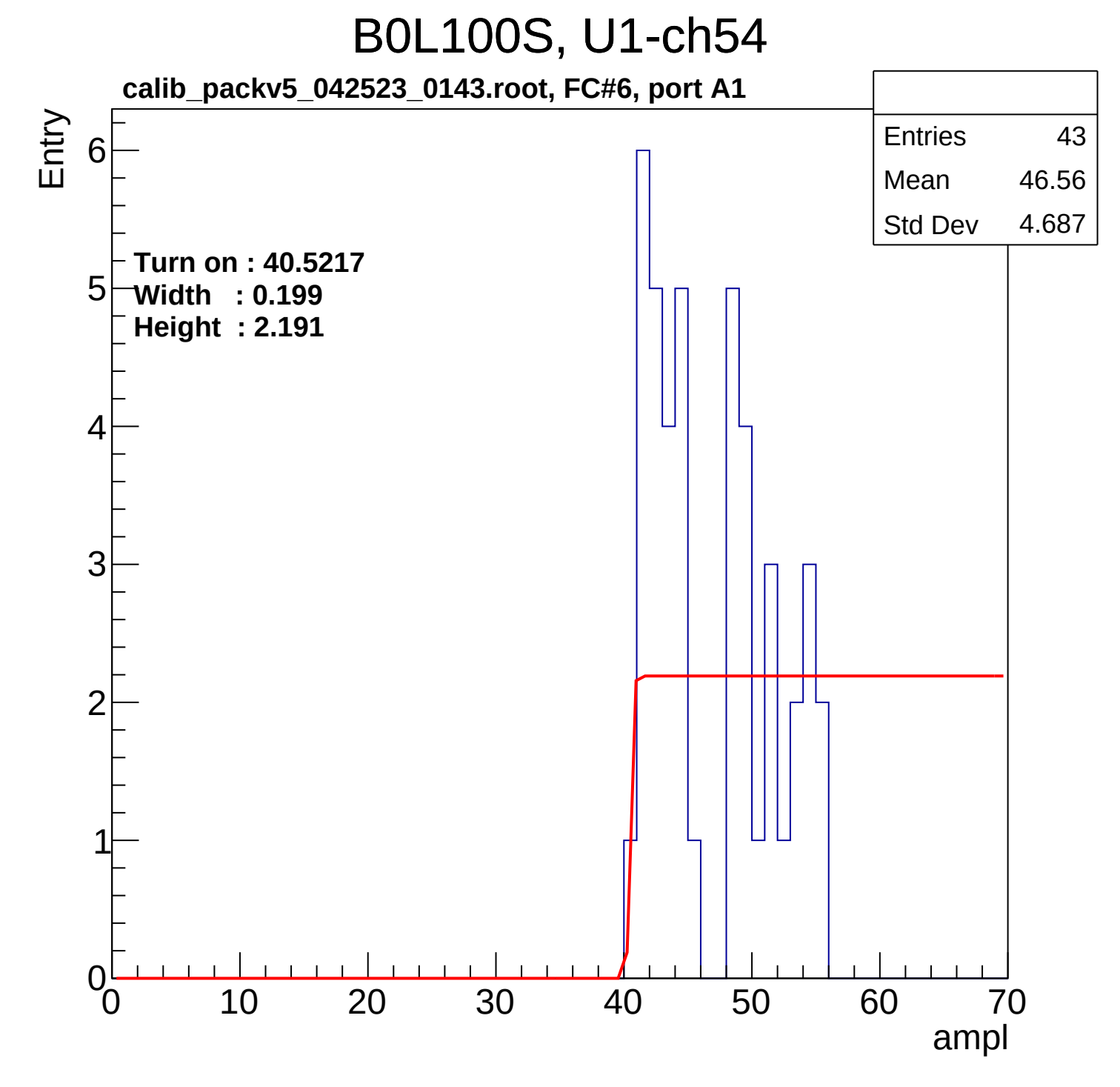
10
20
30
40
50
60
70
ampl


B0L100S, U1-ch54
calib_packv5_042523_0143.root, FC#6, port A1
Entries 43
Mean 46.56
Std Dev 4.687
Turn on : 40.5217
Width : 0.199
Height : 2.191
Entry
ampl
0
1
2
3
4
5
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0
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60
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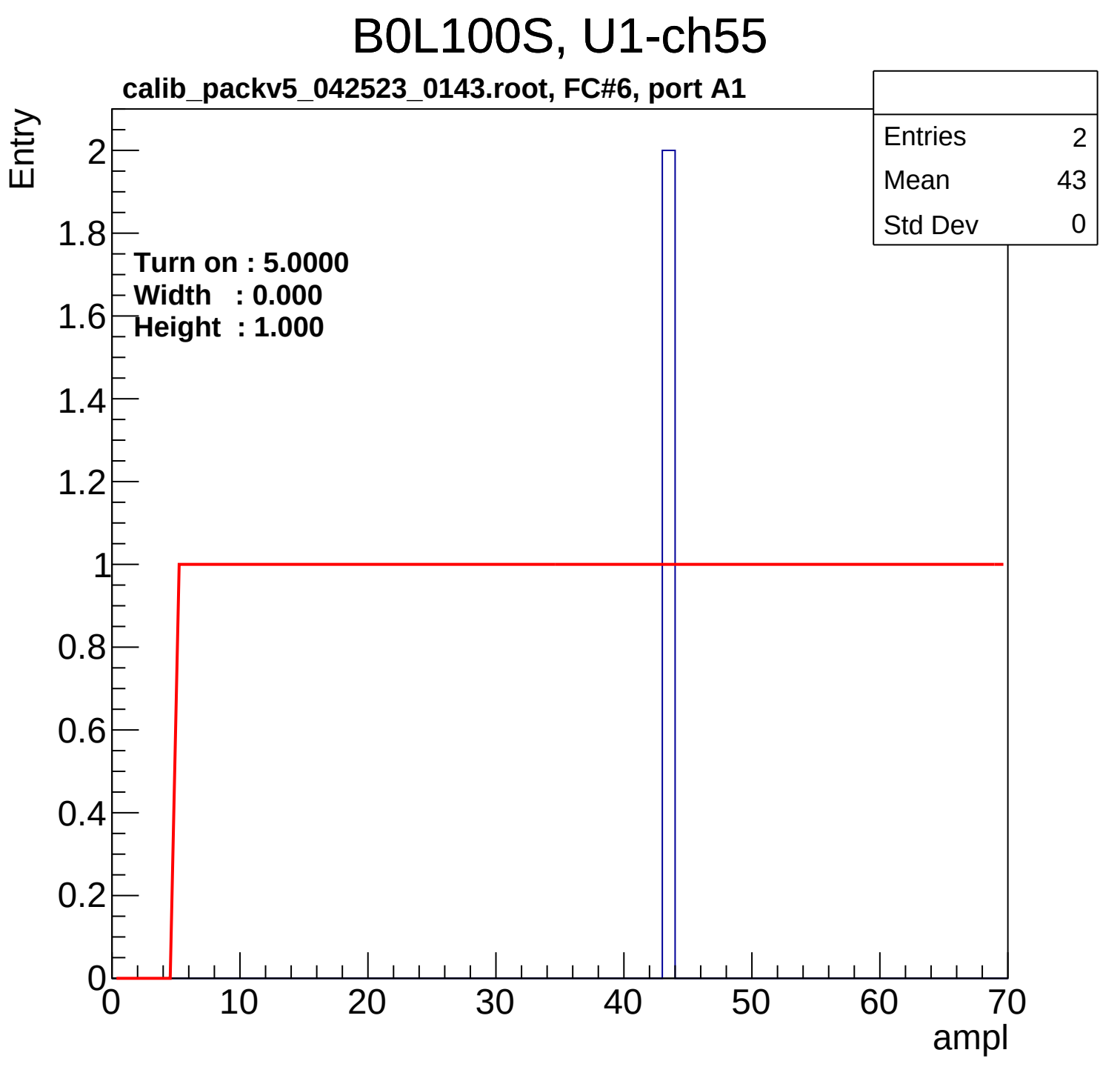
B0L100S, U1-ch55
calib_packv5_042523_0143.root, FC#6, port A1
Entries 2
Mean 43
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
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1.2
1.4
1.6
1.8
2
0
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40
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60
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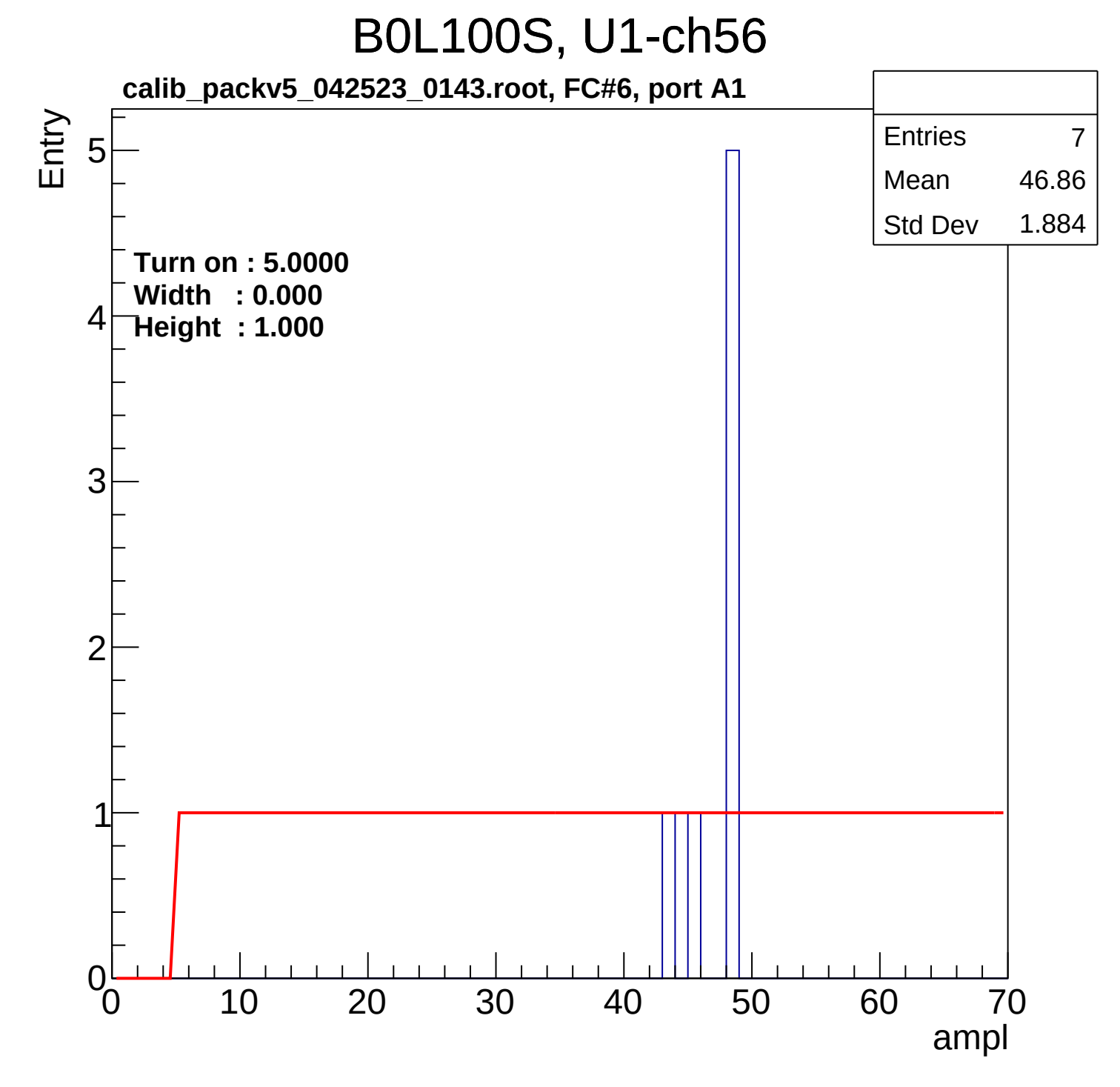
B0L100S, U1-ch56
calib_packv5_042523_0143.root, FC#6, port A1
Entries 7
Mean 46.86
Std Dev 1.884
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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4
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60
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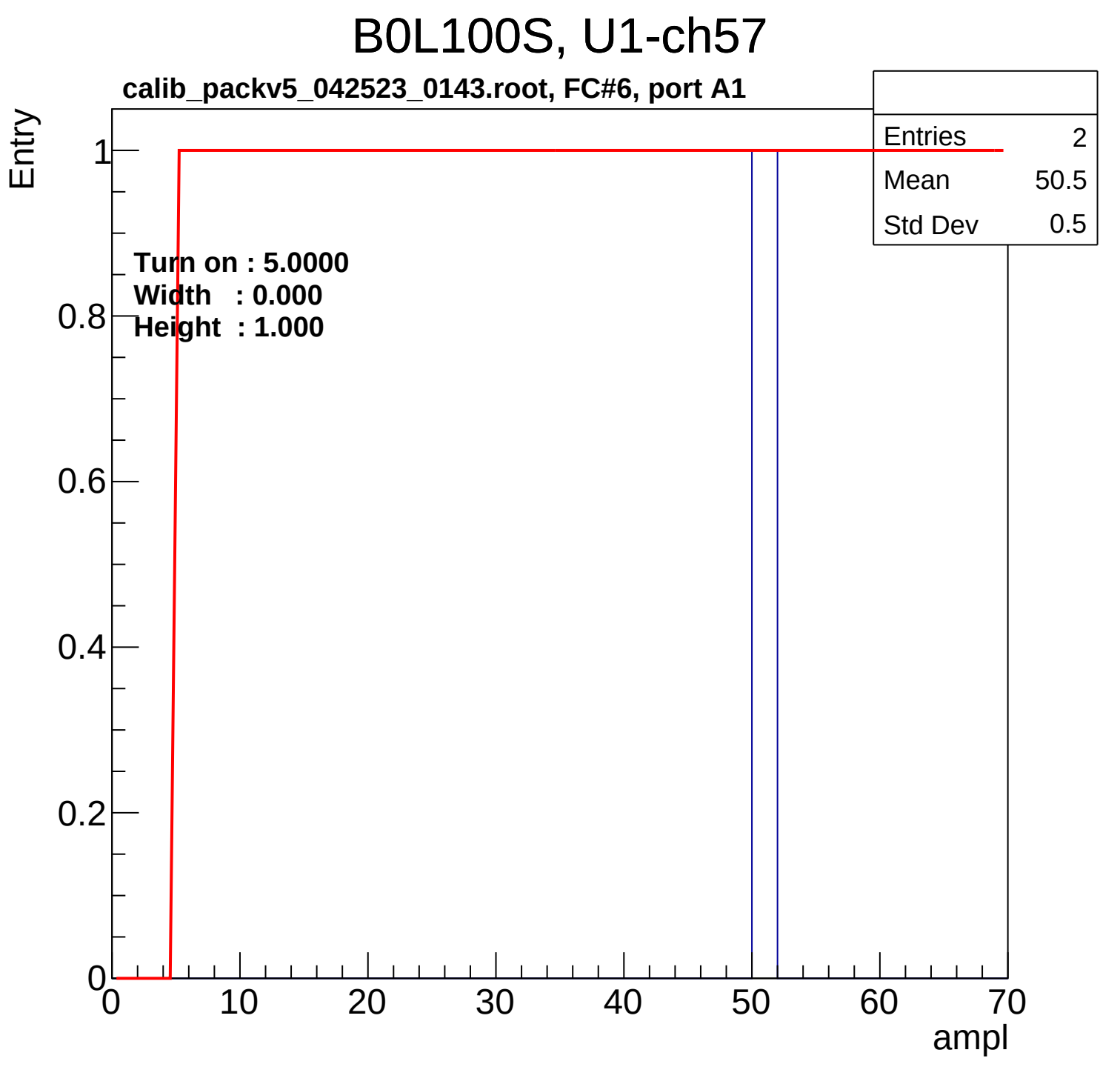
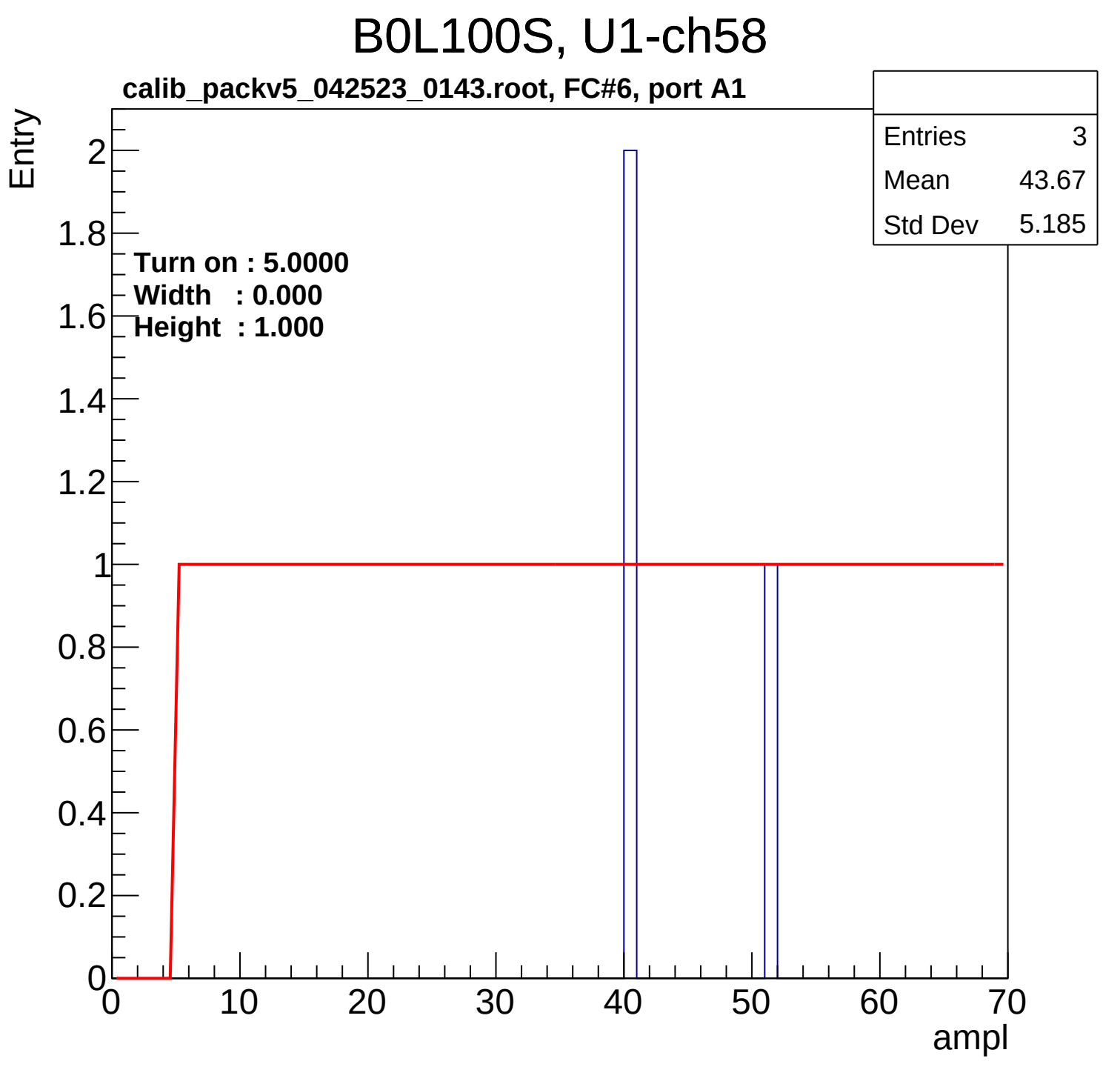

B0L100S, U1-ch57
calib_packv5_042523_0143.root, FC#6, port A1
Entries 2
Mean 50.5
Std Dev 0.5
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B0L100S, U1-ch58
calib_packv5_042523_0143.root, FC#6, port A1
Entries 3
Mean 43.67
Std Dev 5.185
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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60
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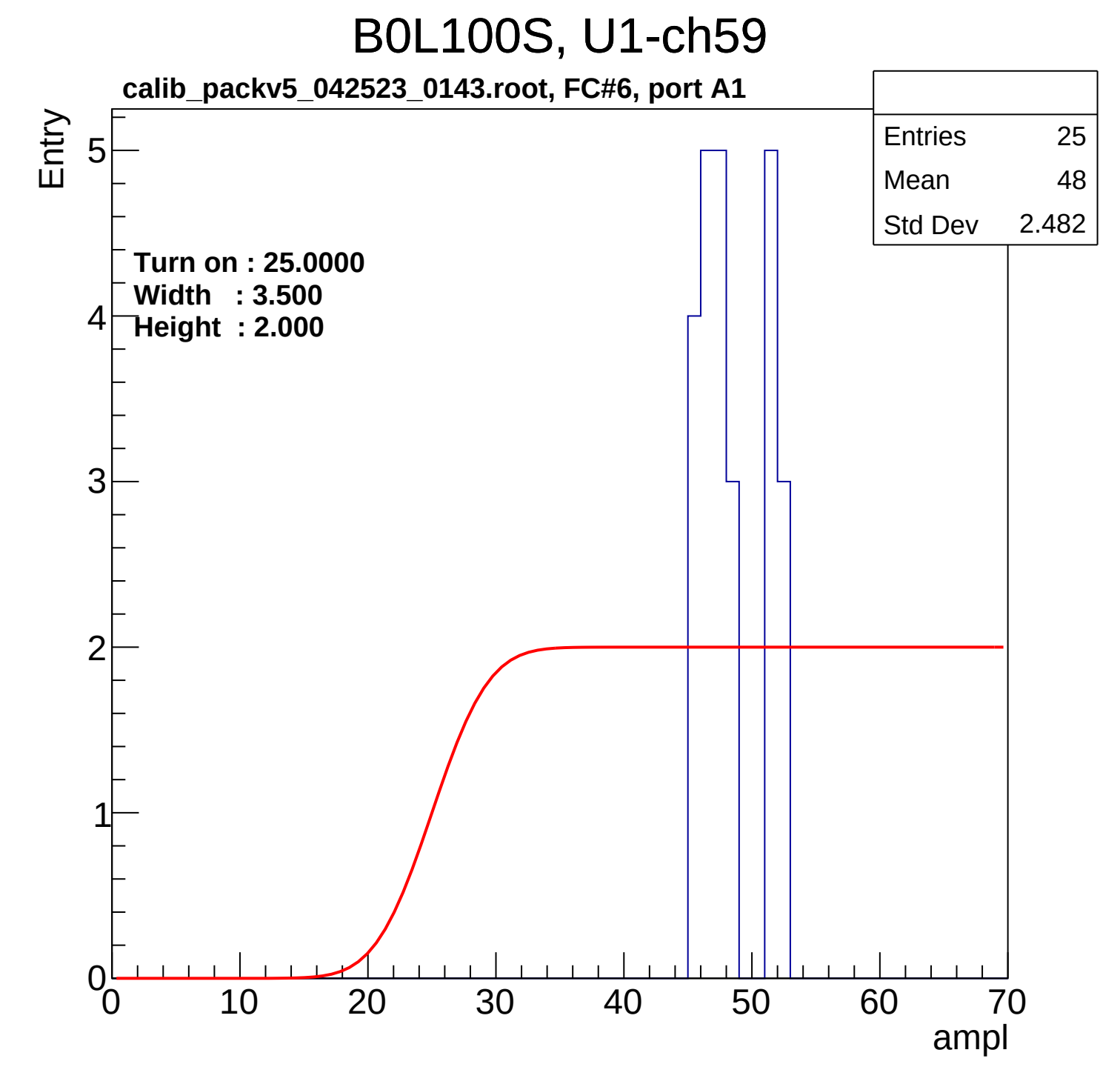
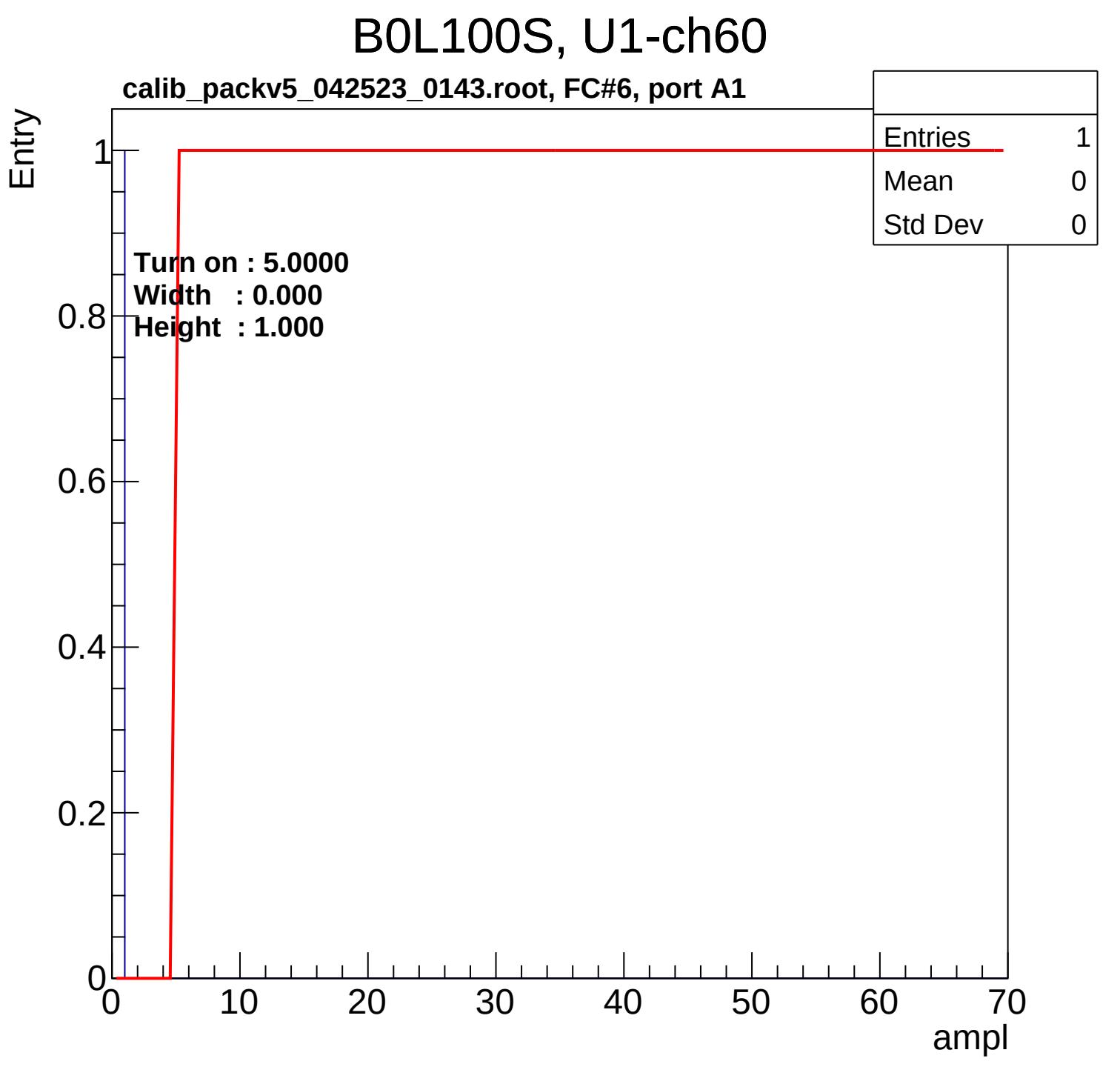
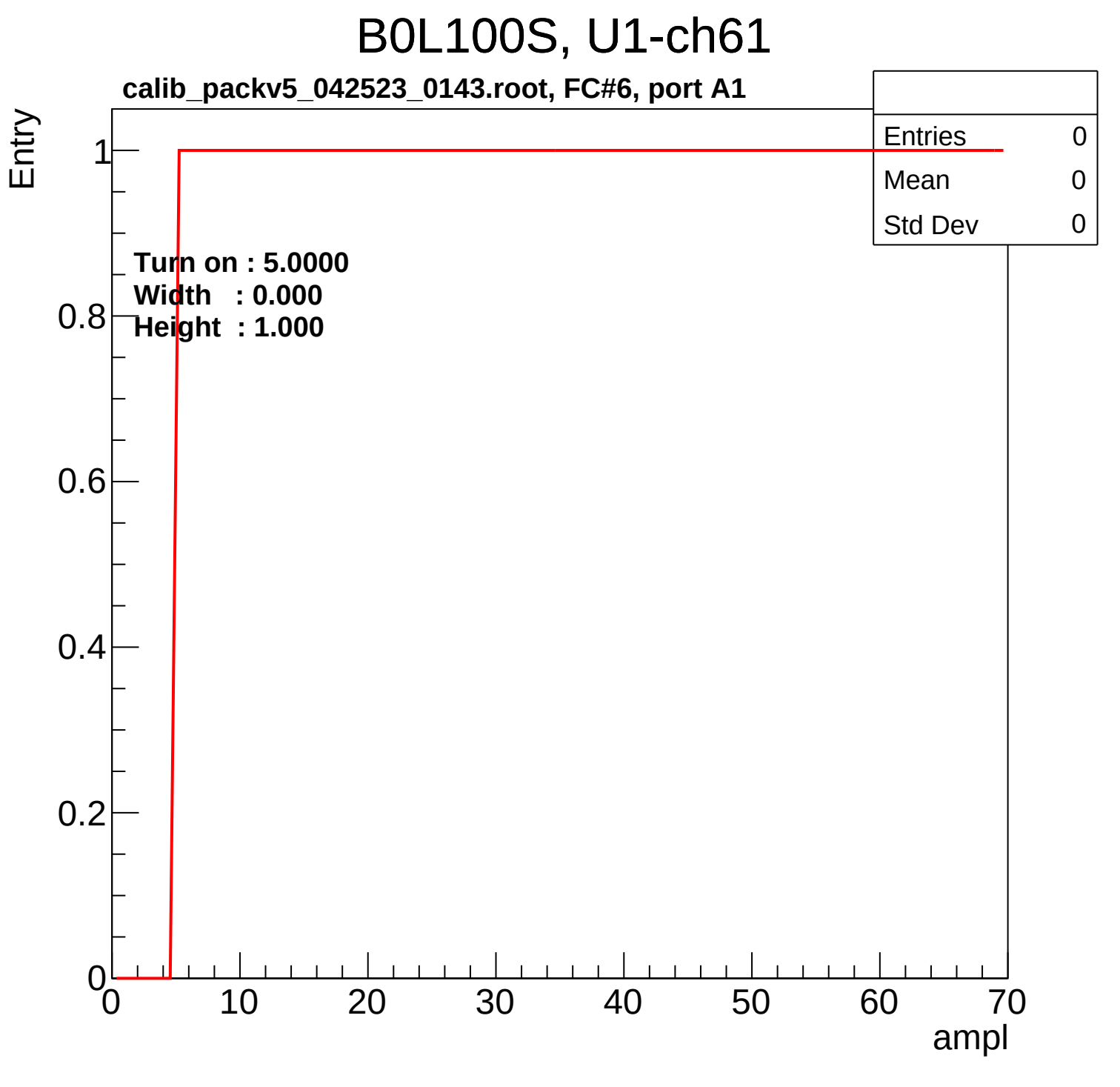
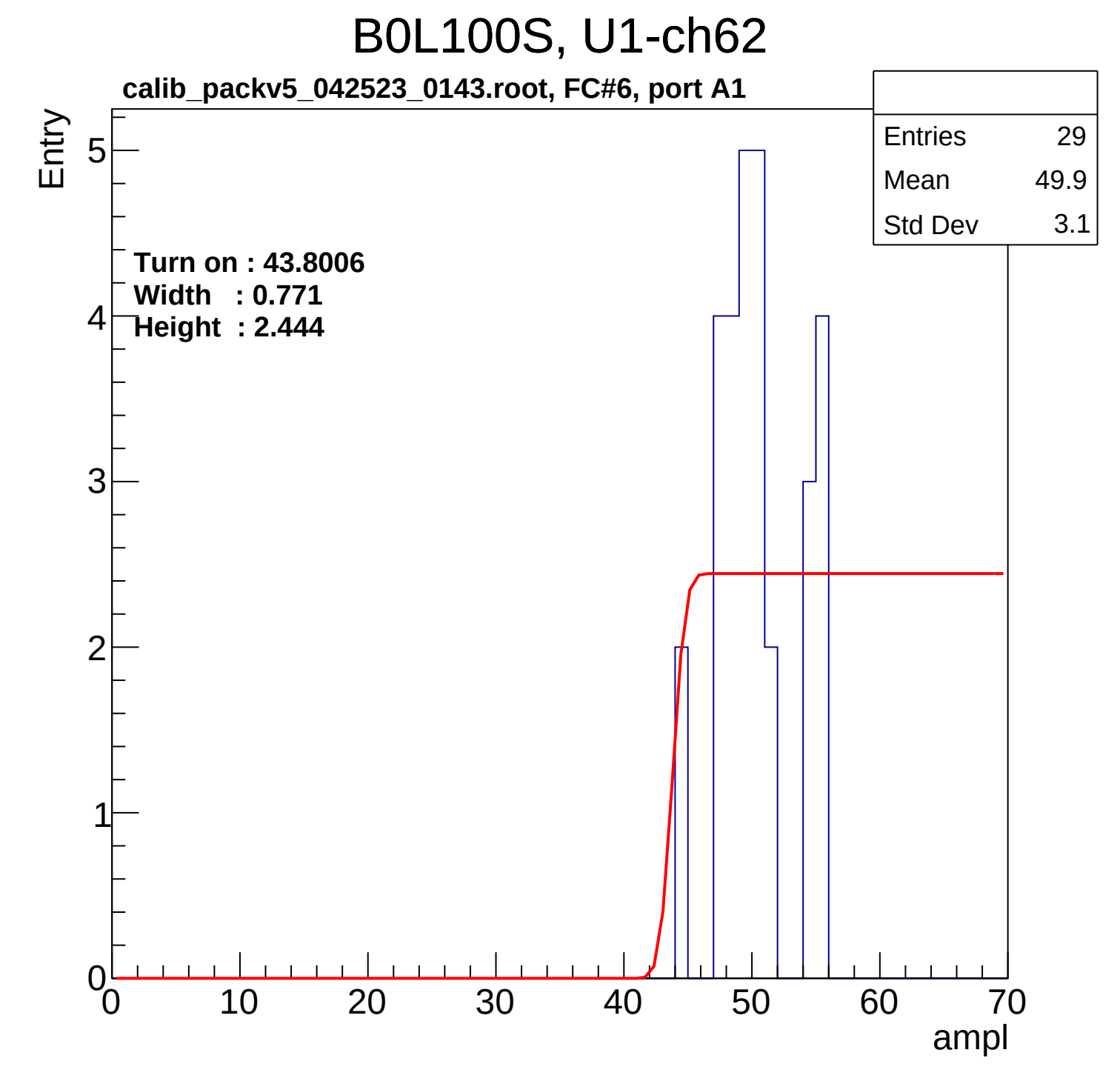
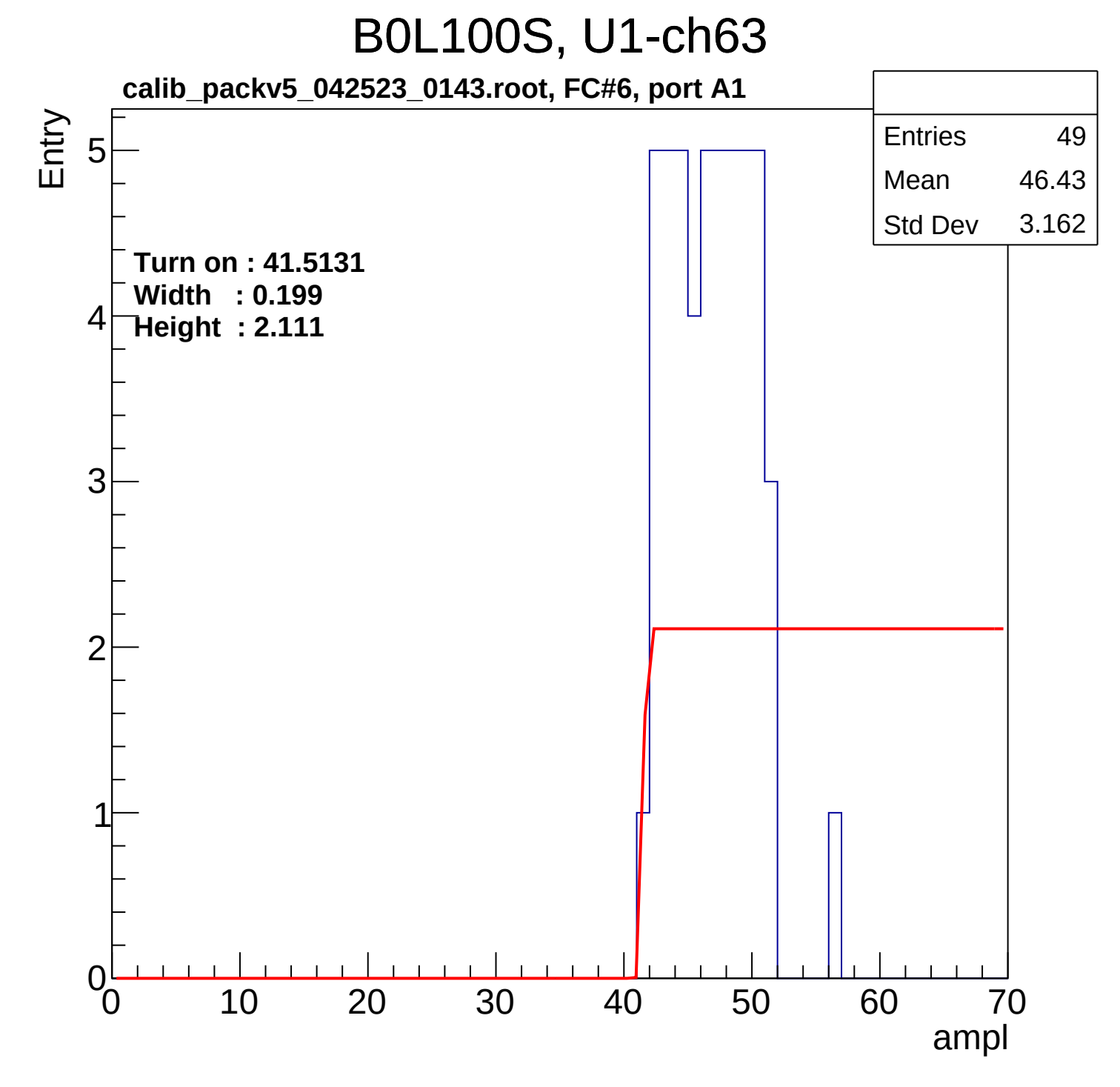
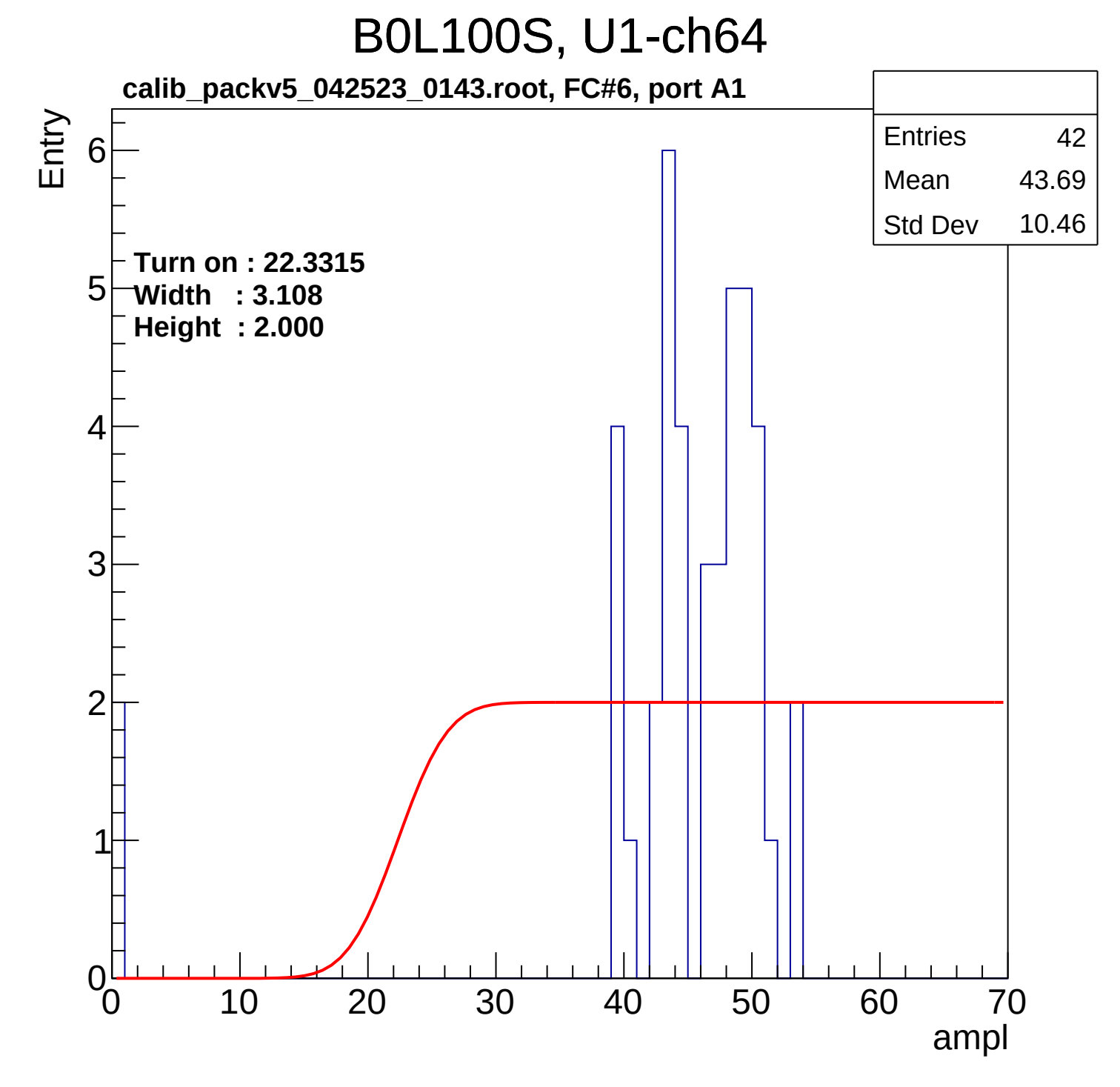

B0L100S, U1-ch59
calib_packv5_042523_0143.root, FC#6, port A1
Entries 25
Mean 48
Std Dev 2.482
Turn on : 25.0000
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B0L100S, U1-ch60
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B0L100S, U1-ch61
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U1-ch62
calib_packv5_042523_0143.root, FC#6, port A1
Entries 29
Mean 49.9
Std Dev 3.1
Turn on : 43.8006
Width : 0.771
Height : 2.444
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B0L100S, U1-ch63
calib_packv5_042523_0143.root, FC#6, port A1
Entries 49
Mean 46.43
Std Dev 3.162
Turn on : 41.5131
Width : 0.199
Height : 2.111
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B0L100S, U1-ch64
calib_packv5_042523_0143.root, FC#6, port A1
Entries 42
Mean 43.69
Std Dev 10.46
Turn on : 22.3315
Width : 3.108
Height : 2.000
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
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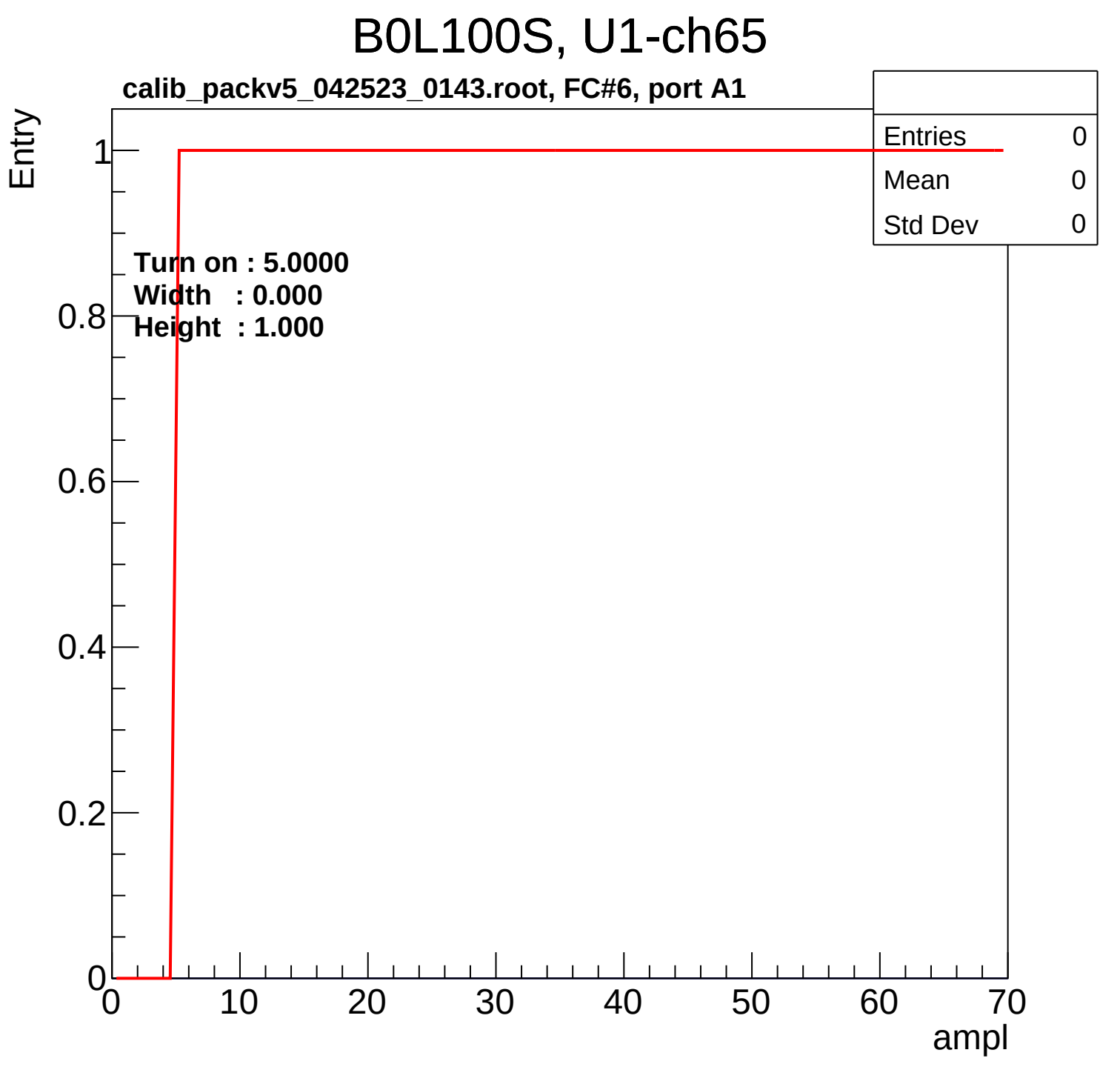
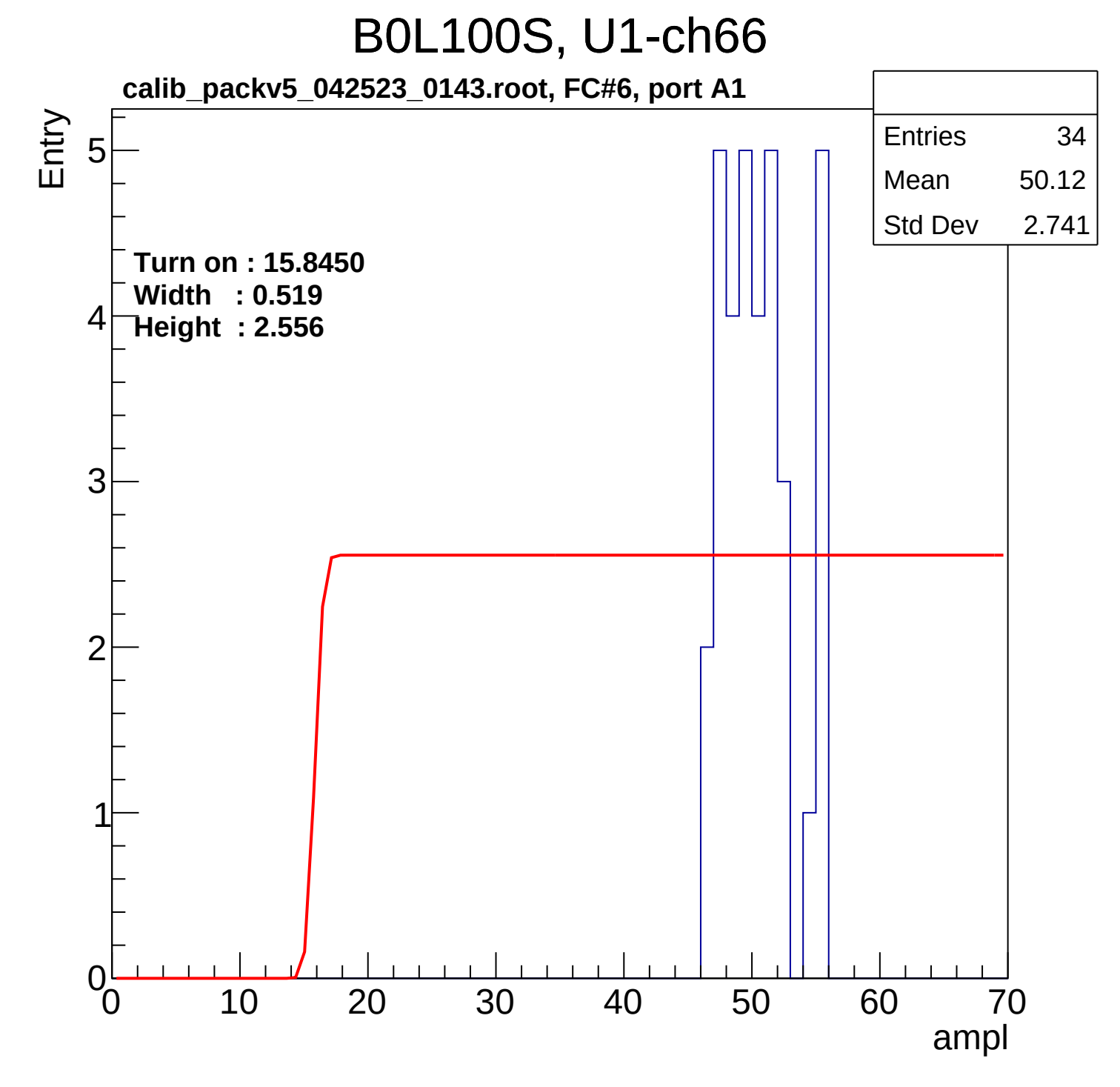
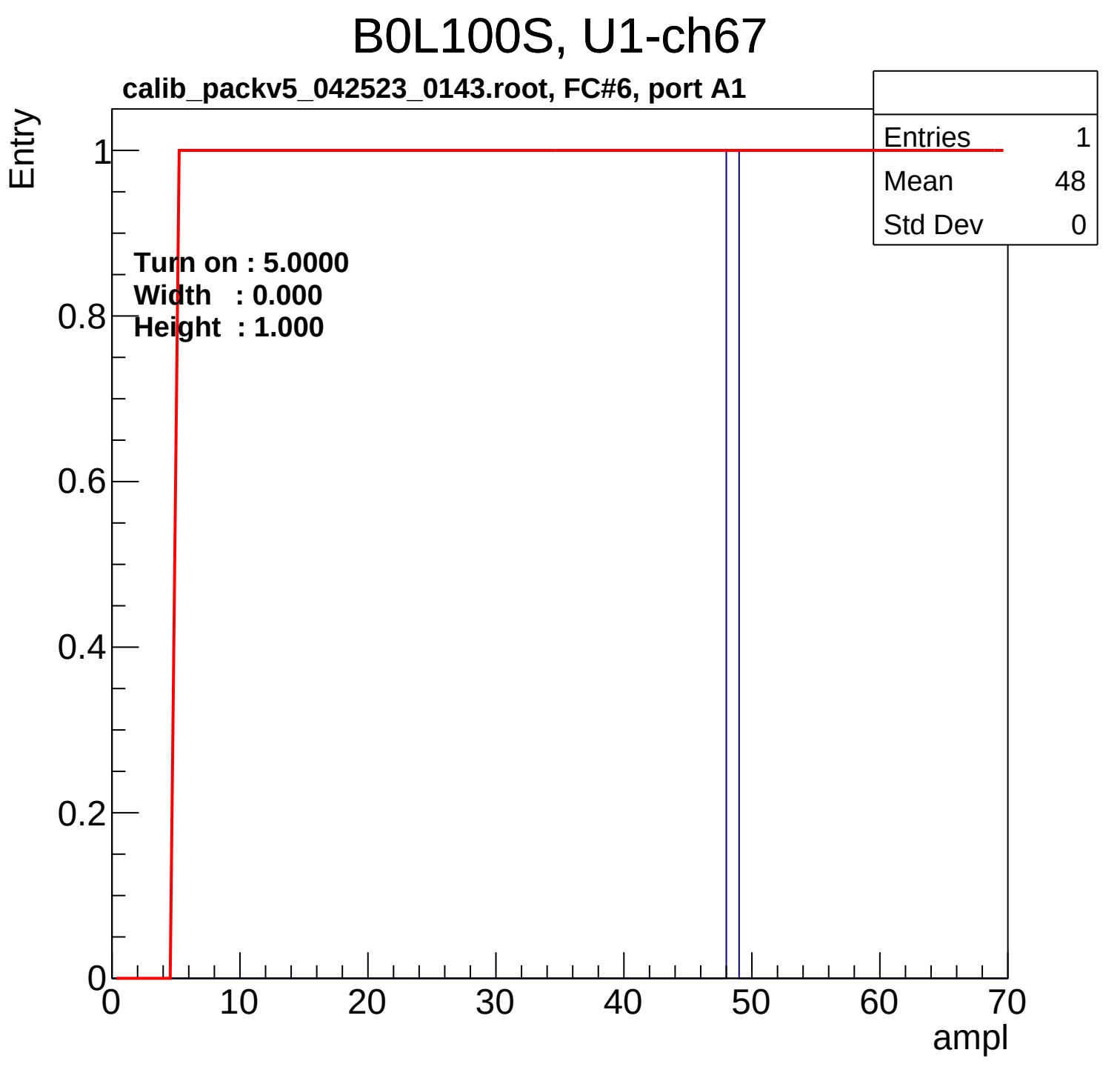
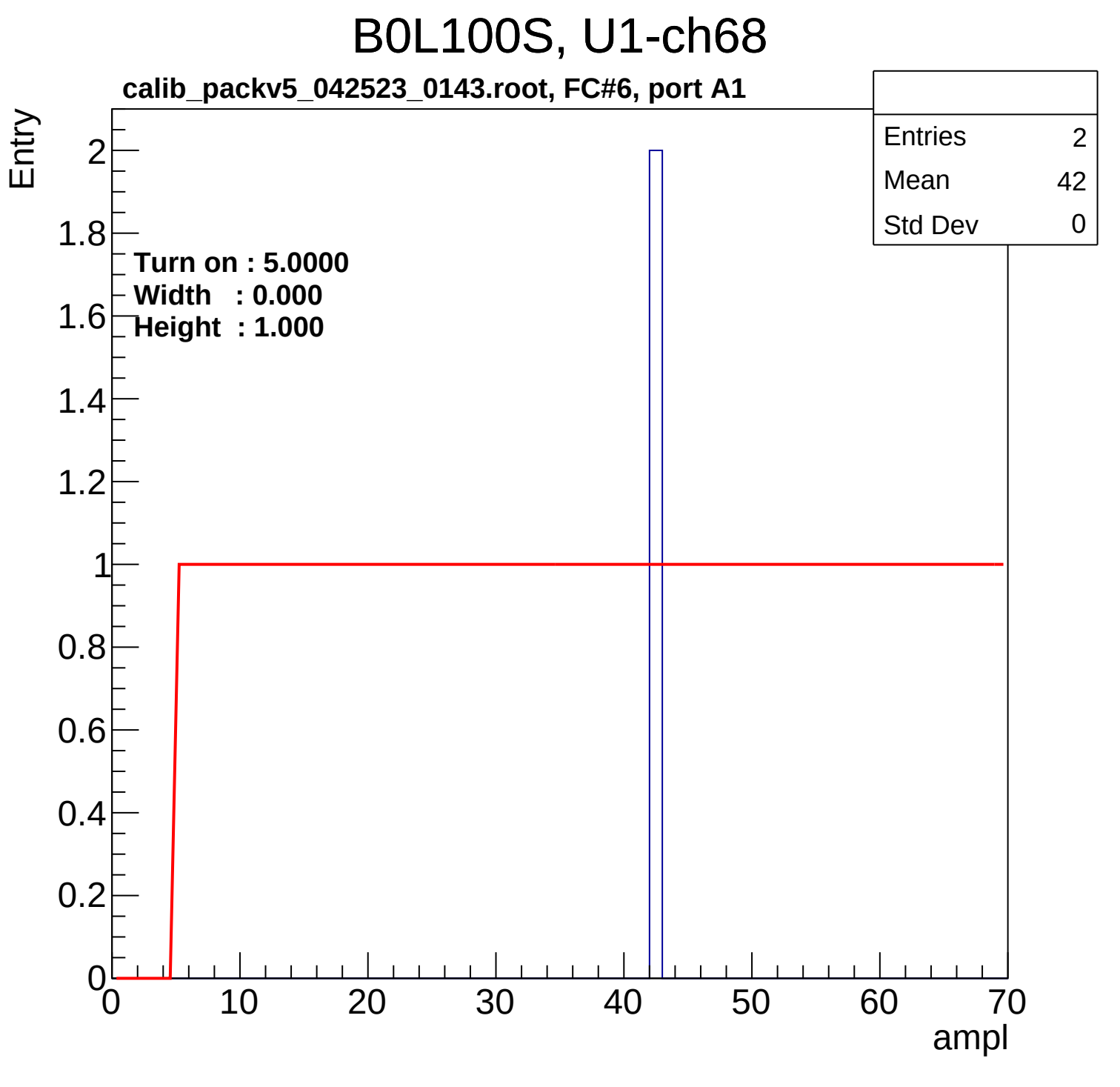
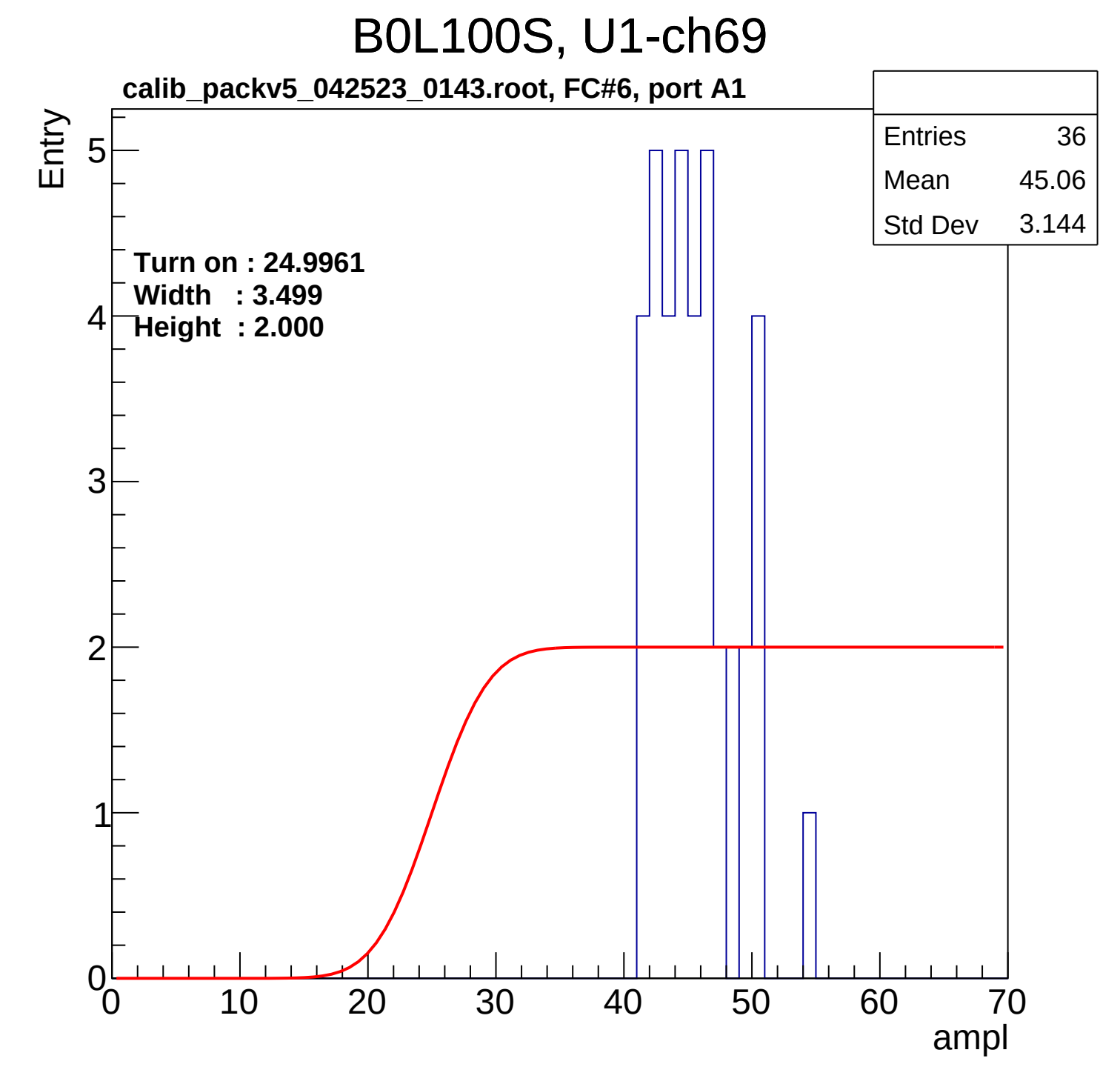
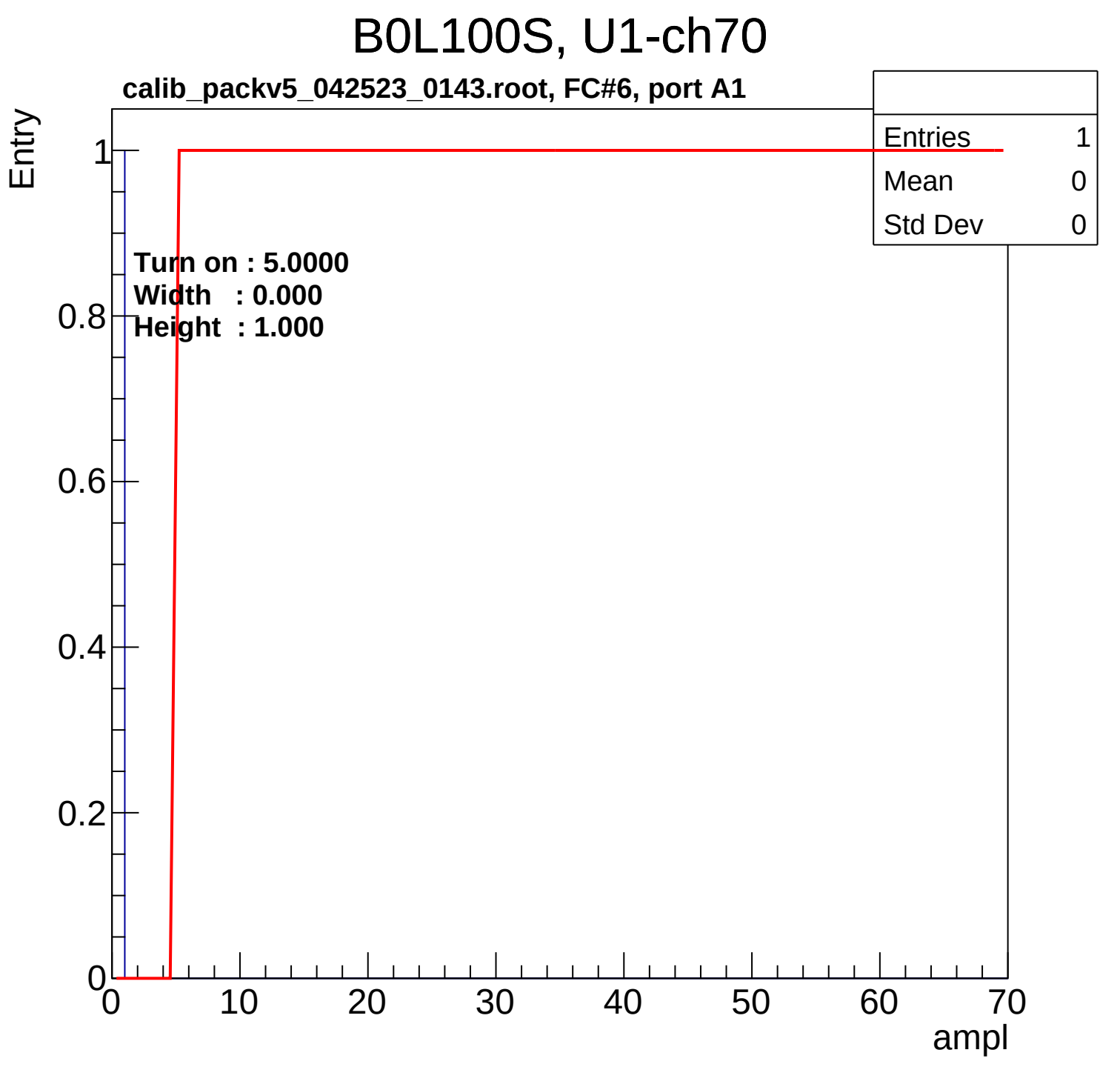

B0L100S, U1-ch65
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

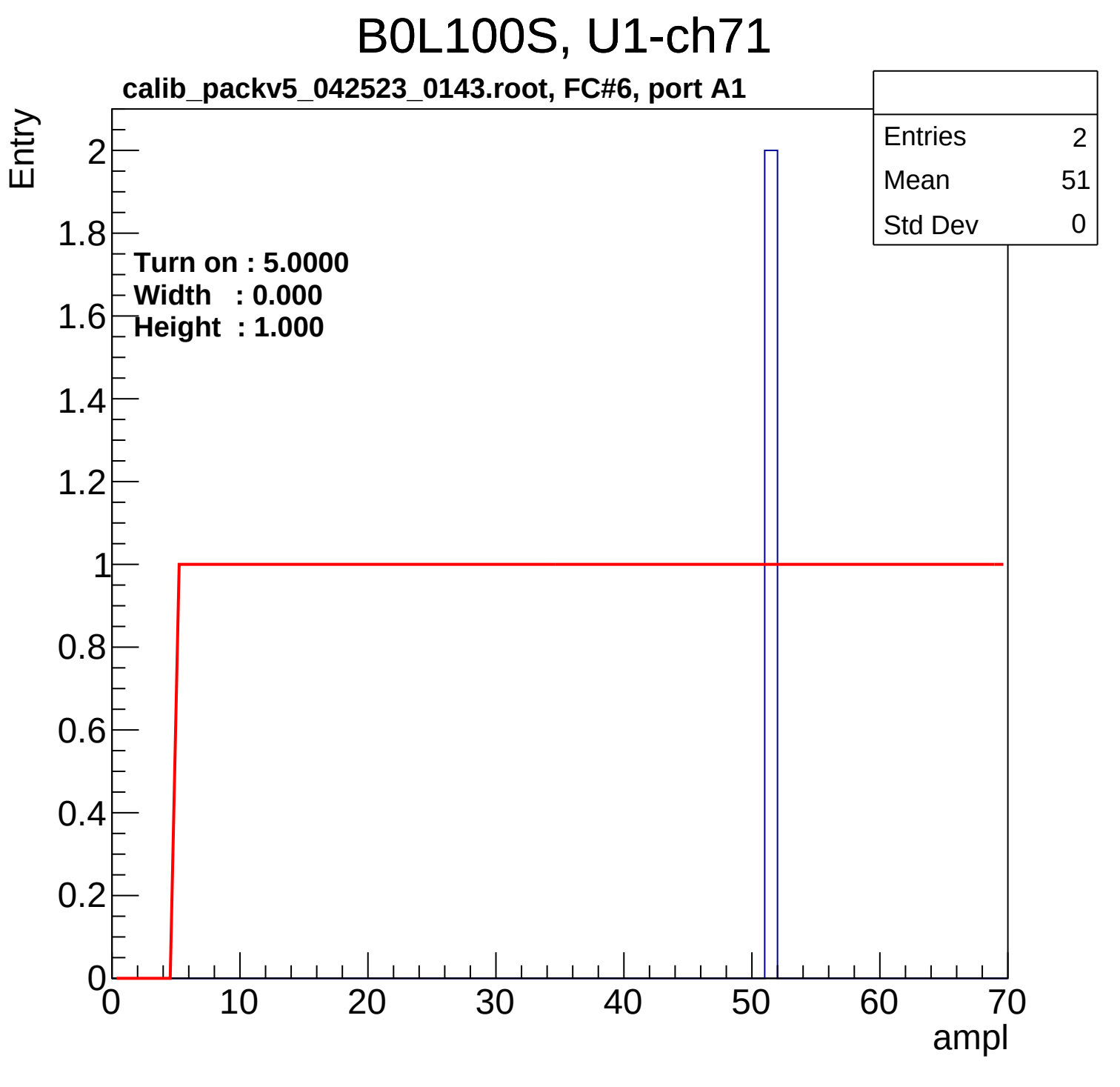

B0L100S, U1-ch66
calib_packv5_042523_0143.root, FC#6, port A1
Entries 34
Mean 50.12
Std Dev 2.741
Turn on : 15.8450
Width : 0.519
Height : 2.556
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

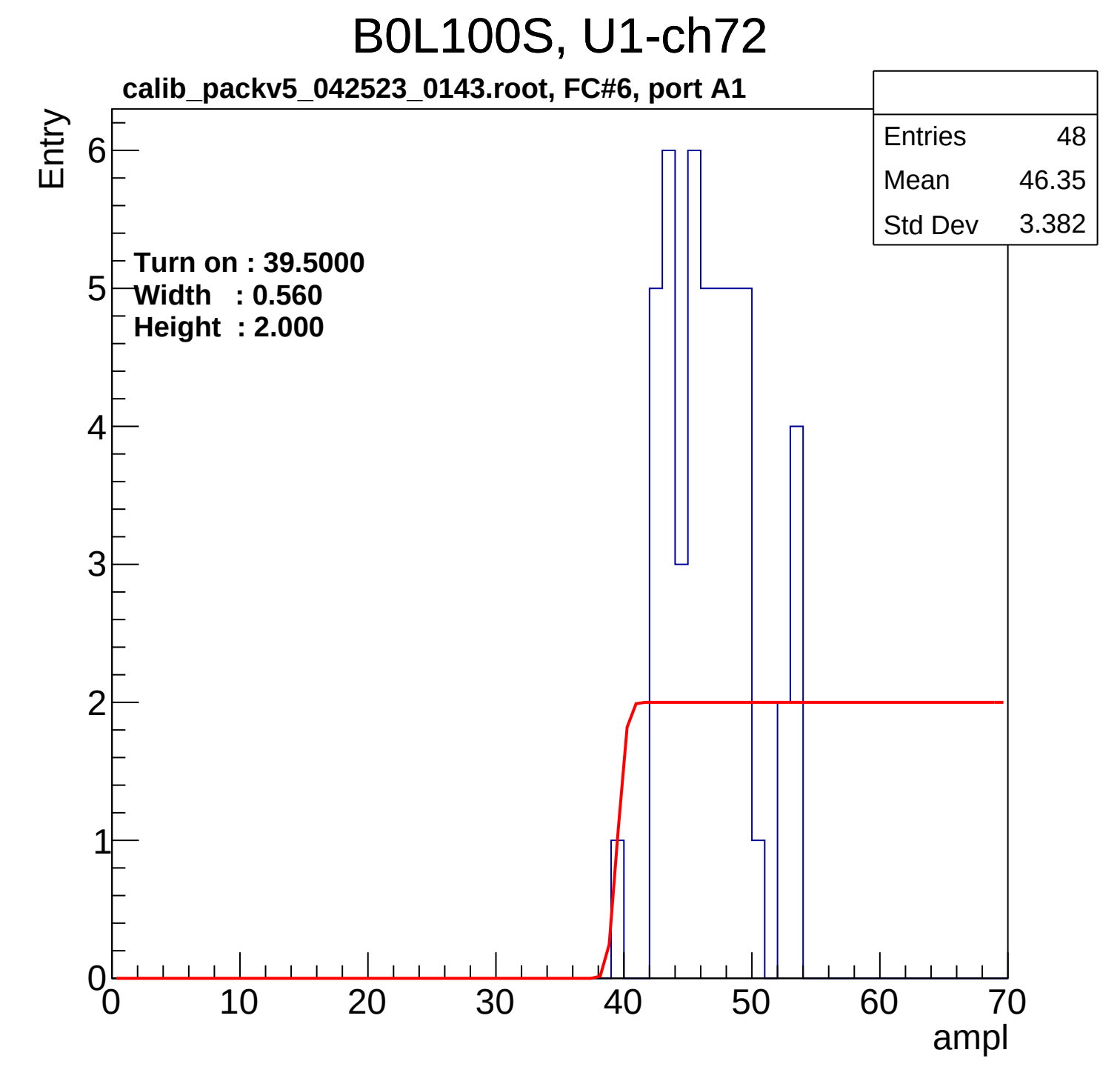

B0L100S, U1-ch67
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 48
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B0L100S, U1-ch68
calib_packv5_042523_0143.root, FC#6, port A1
Entries 2
Mean 42
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B0L100S, U1-ch69
calib_packv5_042523_0143.root, FC#6, port A1
Entries 36
Mean 45.06
Std Dev 3.144
Turn on : 24.9961
Width : 3.499
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B0L100S, U1-ch70
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U1-ch71
calib_packv5_042523_0143.root, FC#6, port A1
Entries 2
Mean 51
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B0L100S, U1-ch72
calib_packv5_042523_0143.root, FC#6, port A1
Entries 48
Mean 46.35
Std Dev 3.382
Turn on : 39.5000
Width : 0.560
Height : 2.000
Entry
ampl
0
1
2
3
4
5
6
0
10
20
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40
50
60
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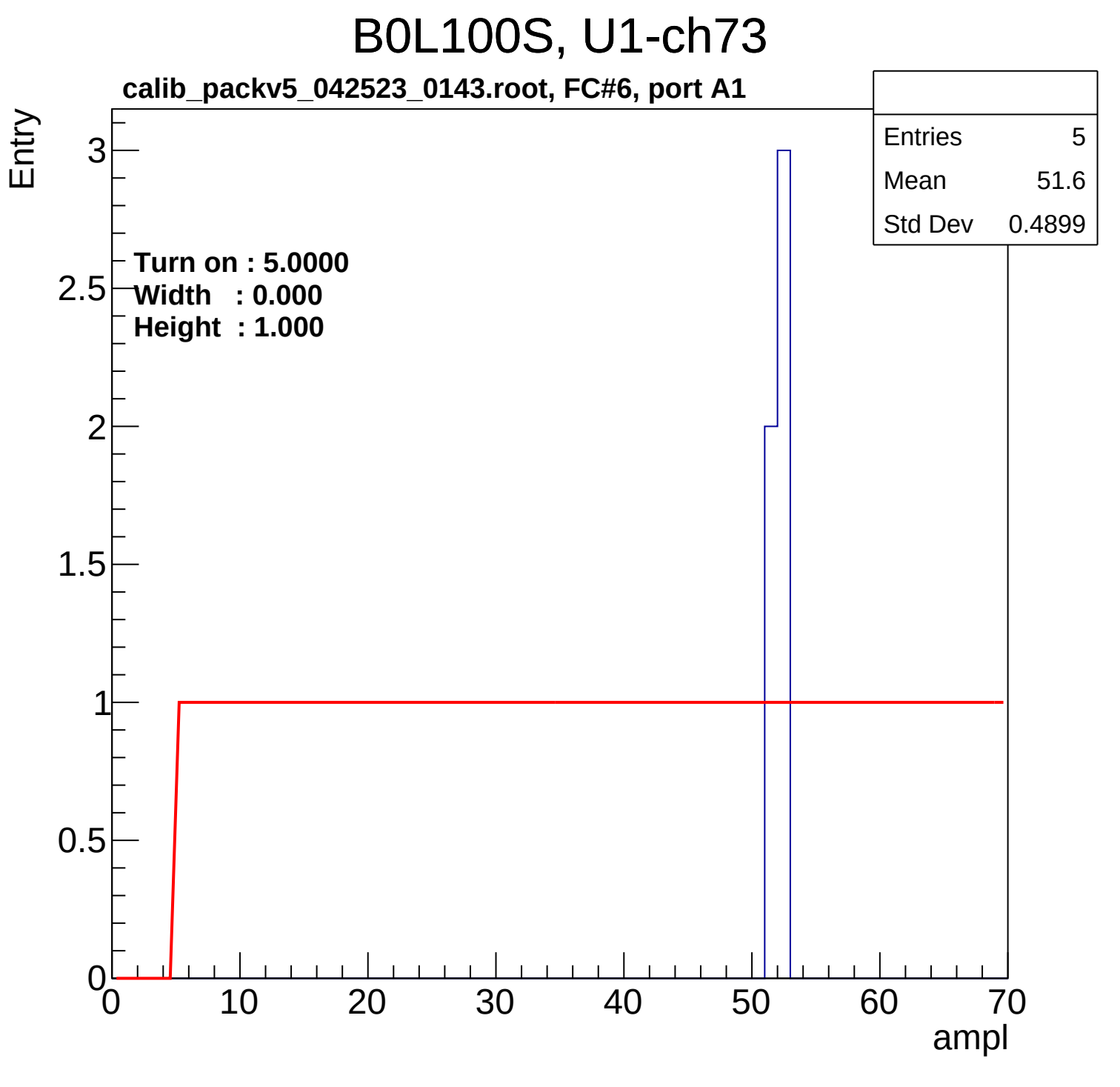
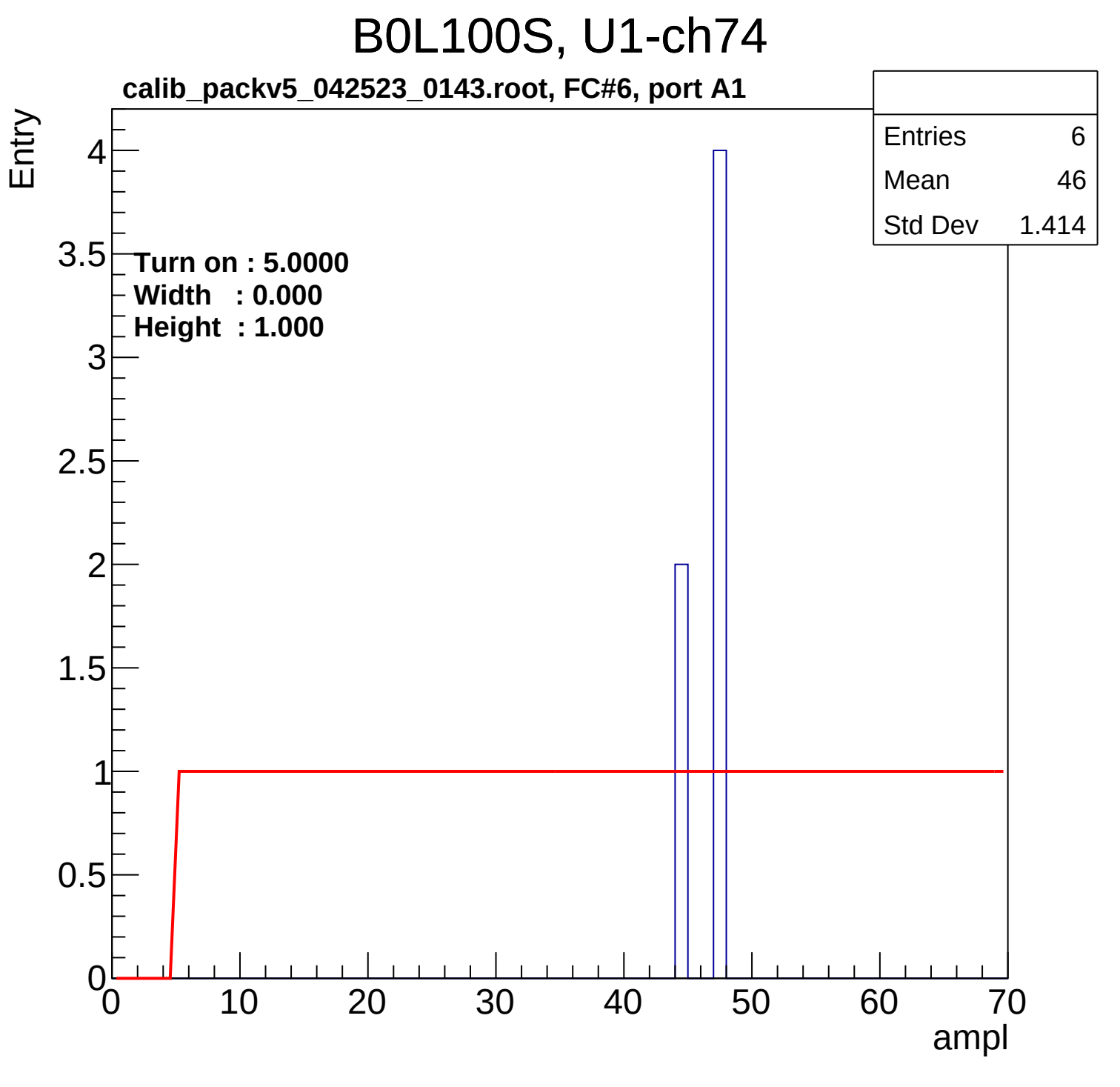
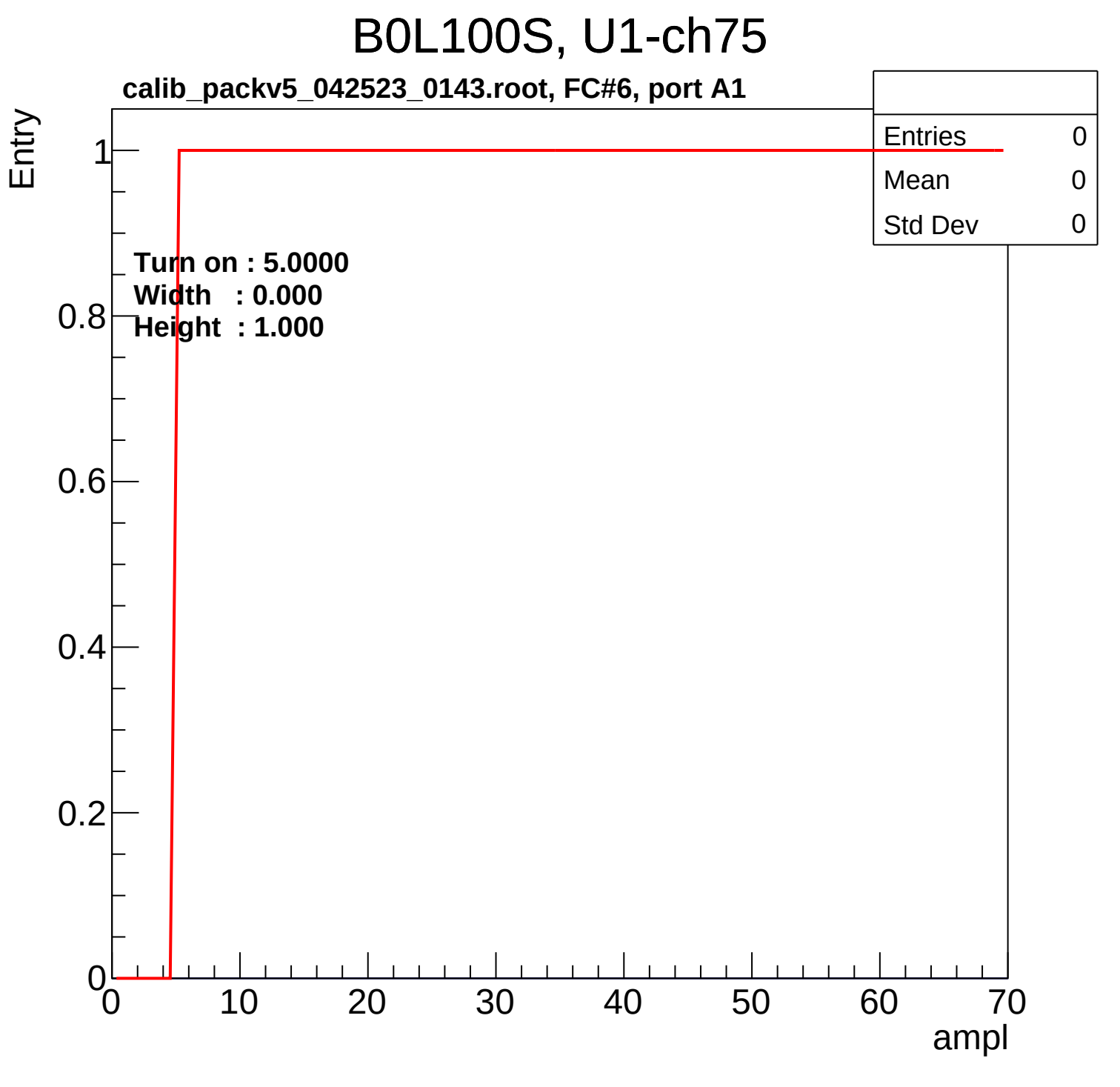
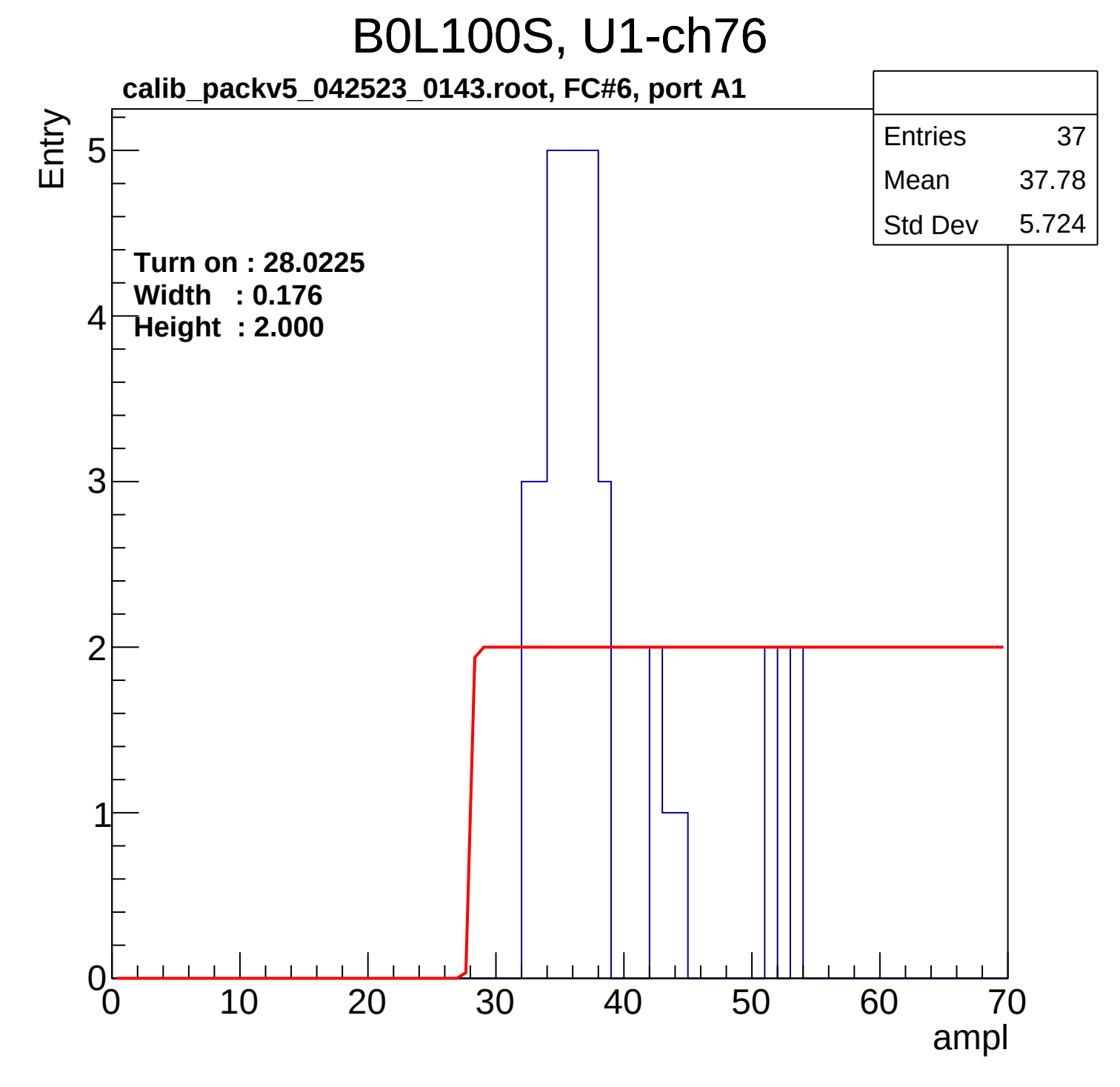

B0L100S, U1-ch73
calib_packv5_042523_0143.root, FC#6, port A1
Entries 5
Mean 51.6
Std Dev 0.4899
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B0L100S, U1-ch74
calib_packv5_042523_0143.root, FC#6, port A1
Entries 6
Mean 46
Std Dev 1.414
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B0L100S, U1-ch75
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U1-ch76
calib_packv5_042523_0143.root, FC#6, port A1
Entries 37
Mean 37.78
Std Dev 5.724
Turn on : 28.0225
Width : 0.176
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
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40
50
60
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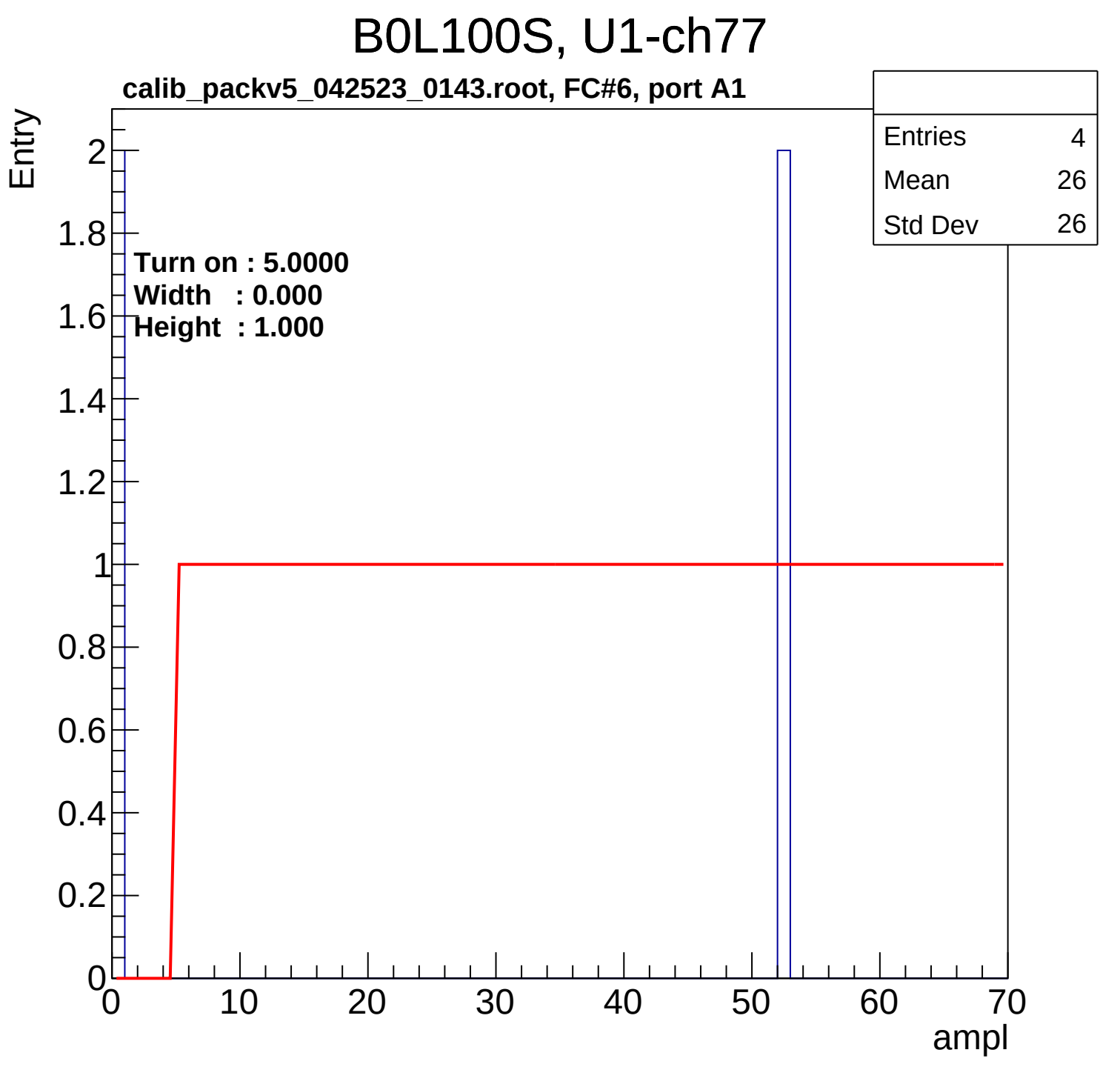
B0L100S, U1-ch77
calib_packv5_042523_0143.root, FC#6, port A1
Entries 4
Mean 26
Std Dev 26
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
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60
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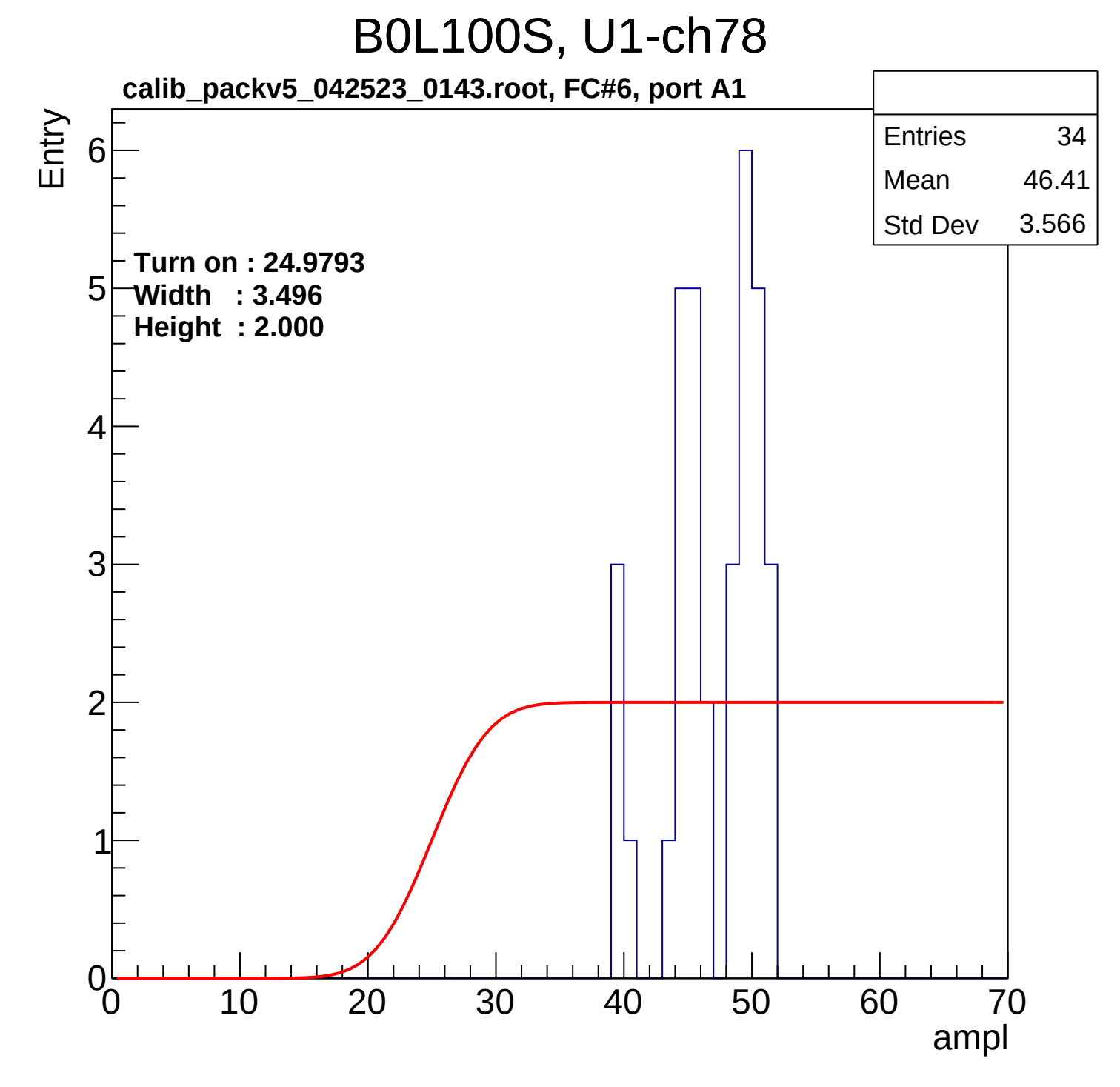
B0L100S, U1-ch78
calib_packv5_042523_0143.root, FC#6, port A1
Entries 34
Mean 46.41
Std Dev 3.566
Turn on : 24.9793
Width : 3.496
Height : 2.000
Entry
ampl
0
1
2
3
4
5
6
0
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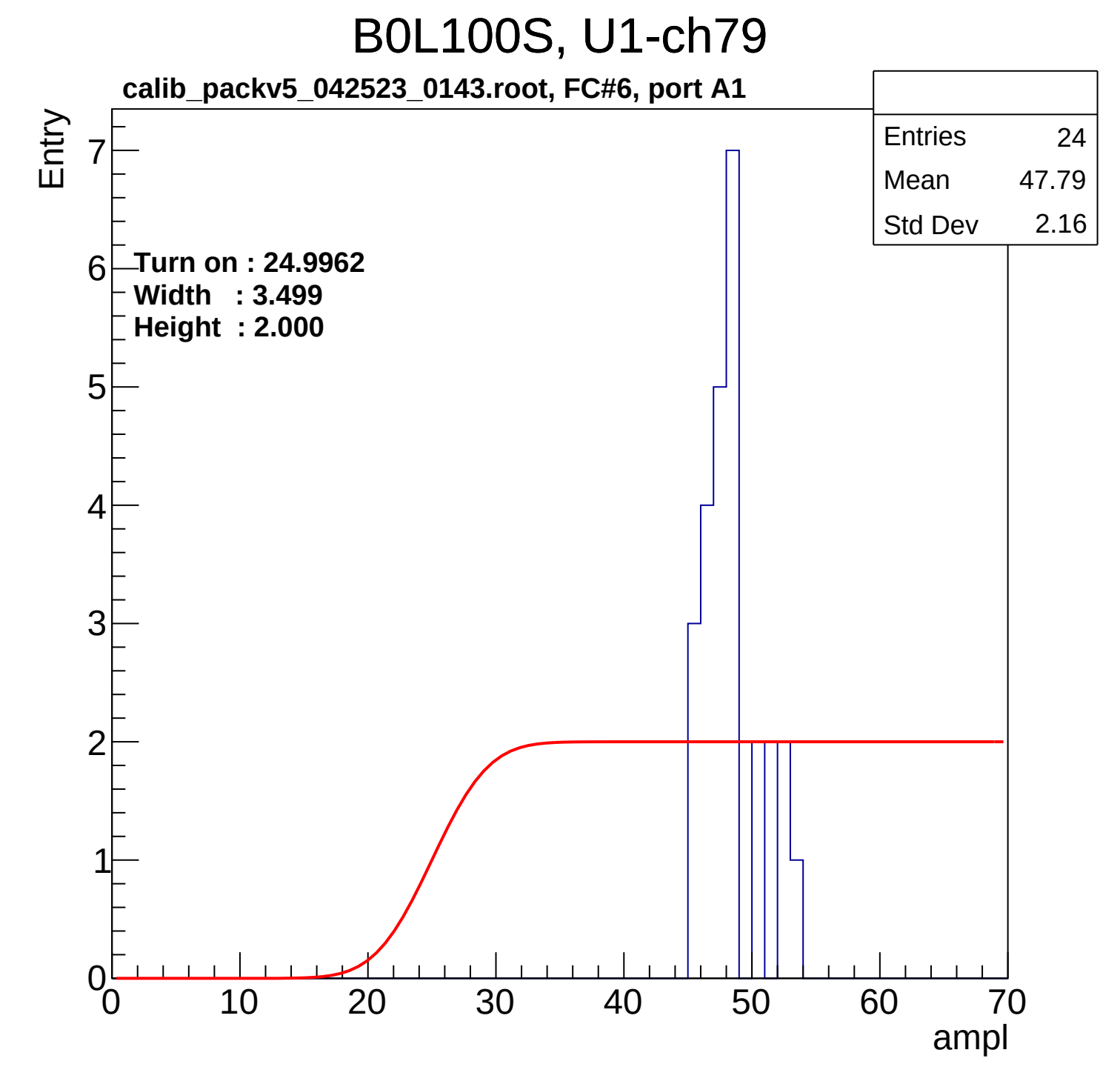
20
30
40
50
60
70


B0L100S, U1-ch79
calib_packv5_042523_0143.root, FC#6, port A1
Entries 24
Mean 47.79
Std Dev 2.16
Turn on : 24.9962
Width : 3.499
Height : 2.000
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
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40
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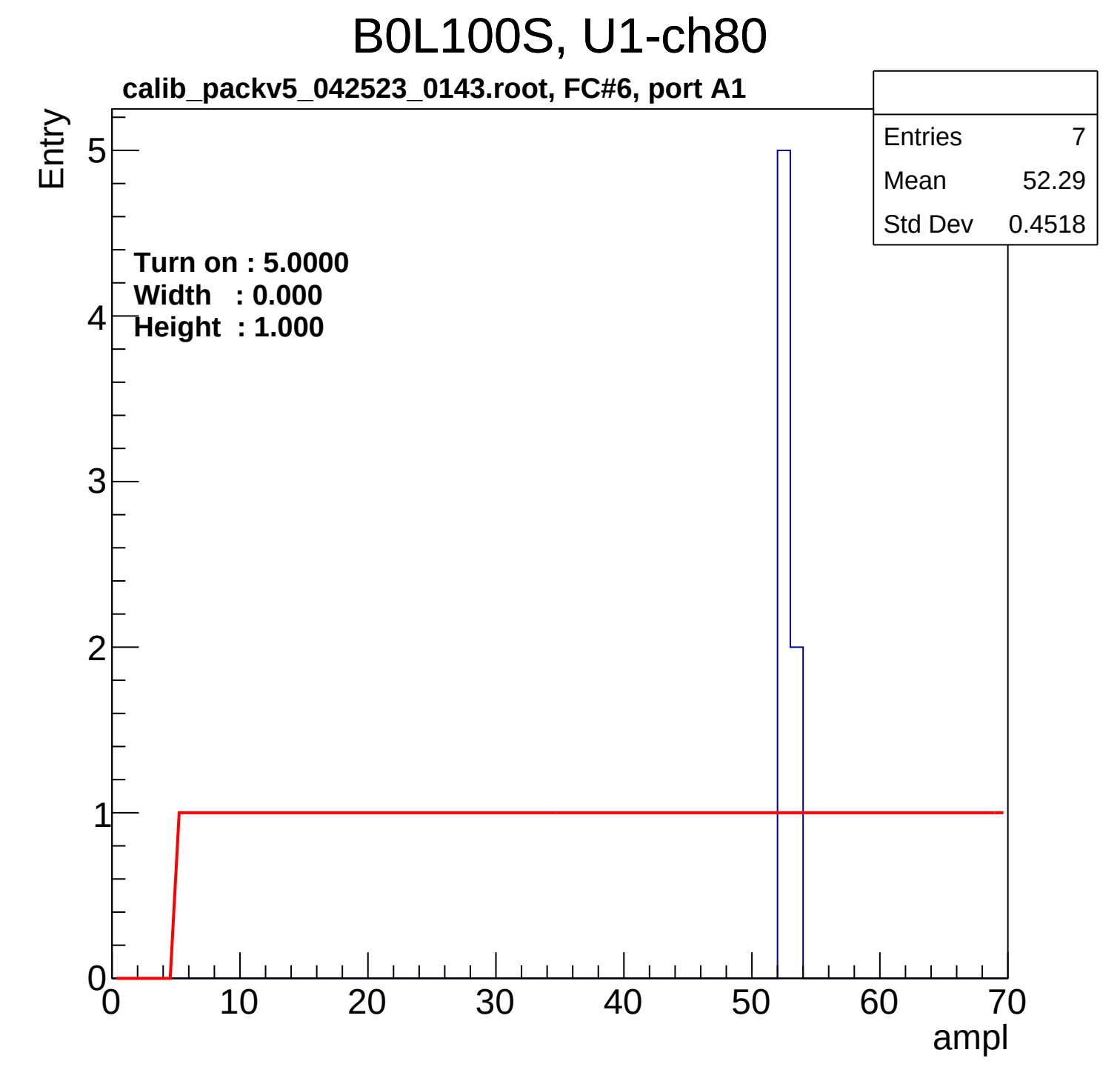
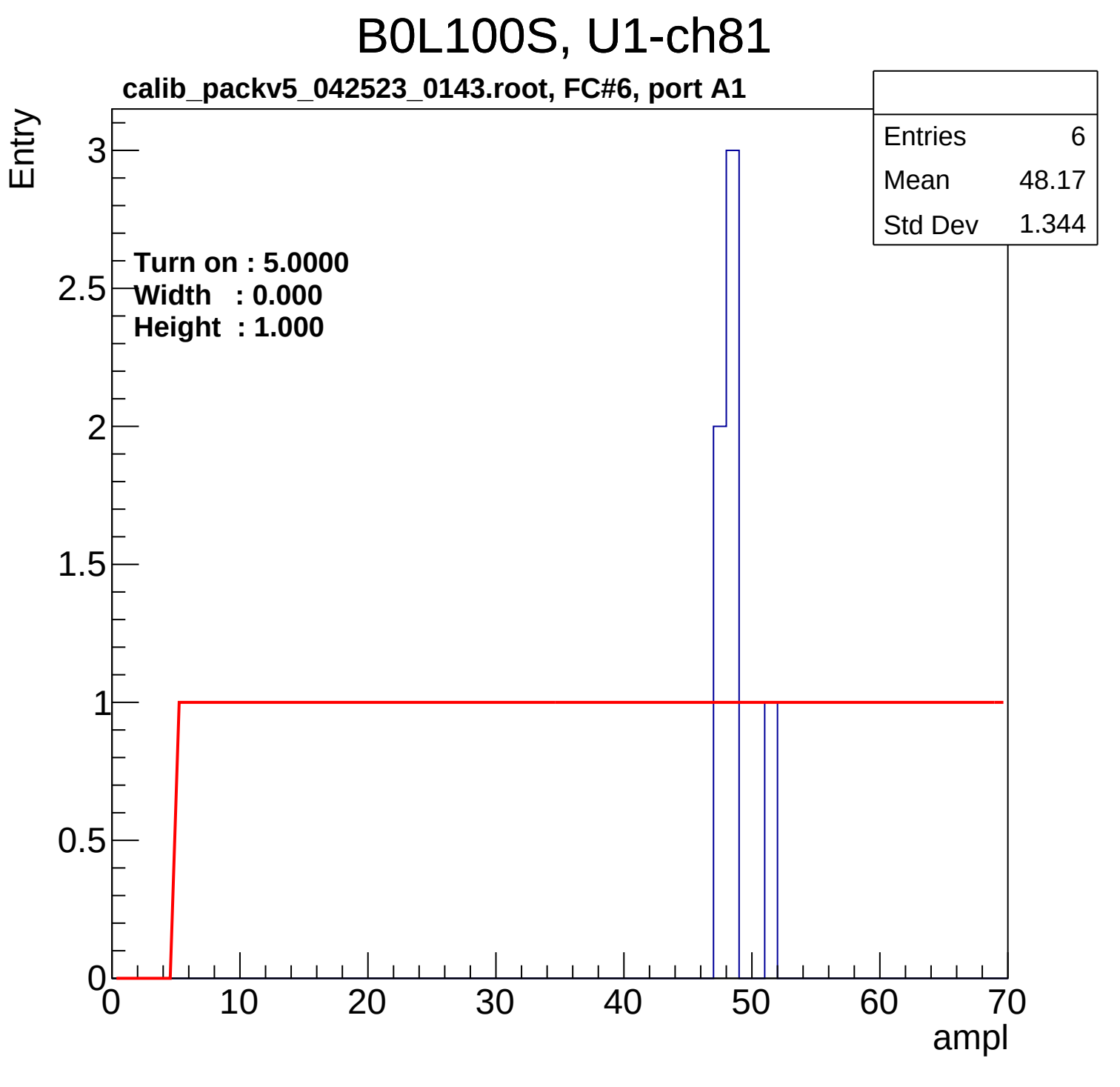
60
70


B0L100S, U1-ch80
calib_packv5_042523_0143.root, FC#6, port A1
Entries 7
Mean 52.29
Std Dev 0.4518
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B0L100S, U1-ch81
calib_packv5_042523_0143.root, FC#6, port A1
Entries 6
Mean 48.17
Std Dev 1.344
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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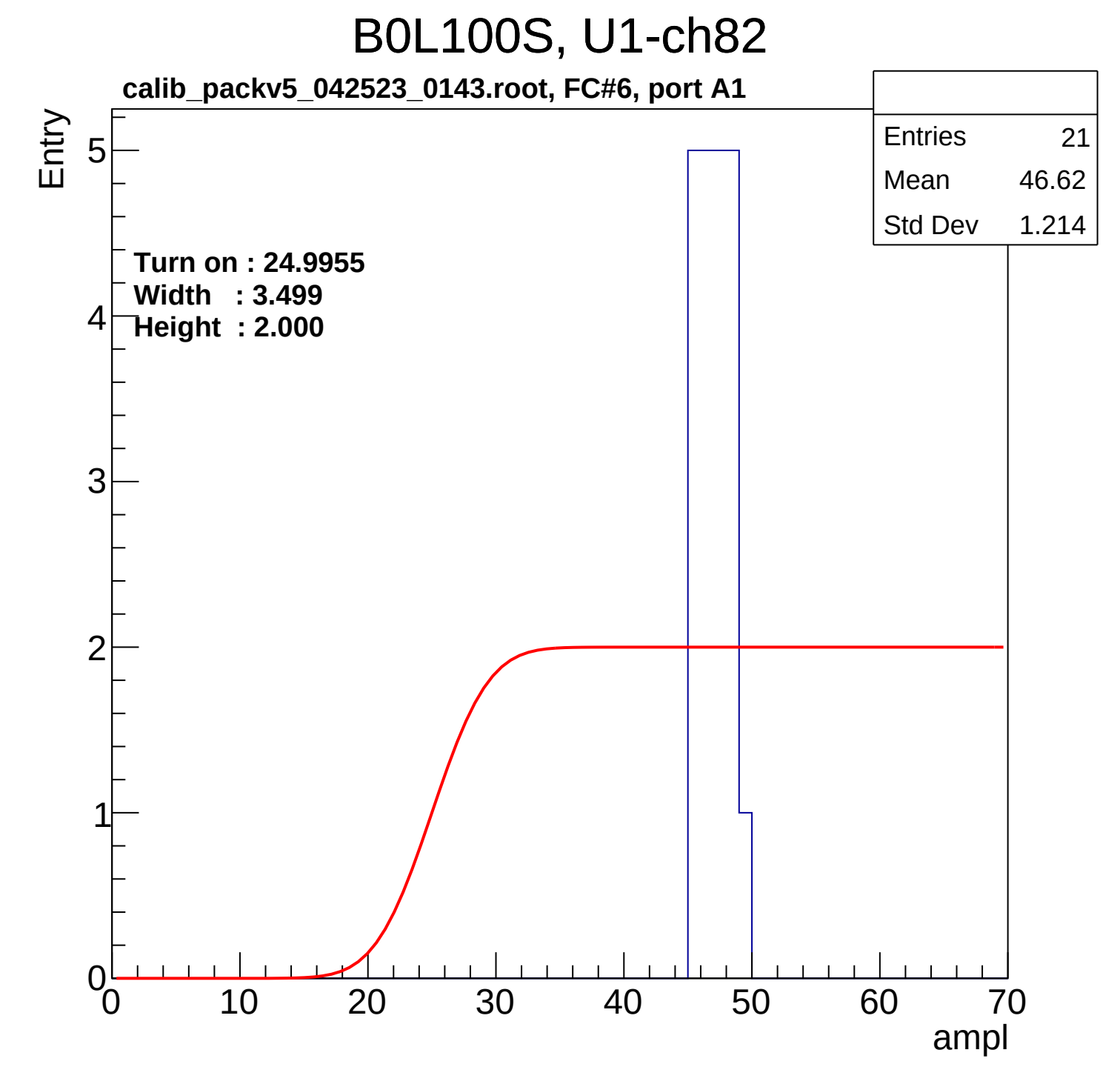
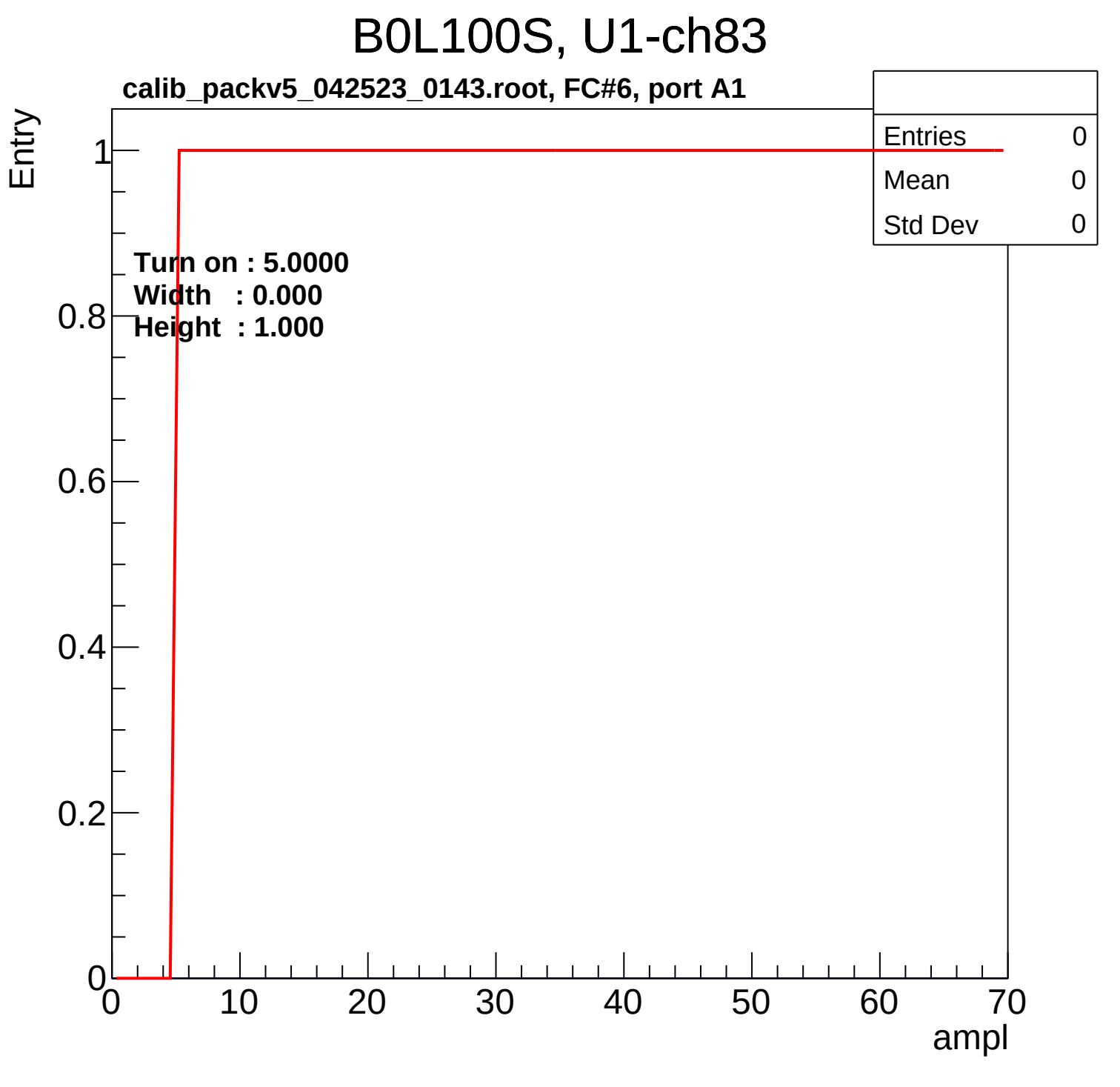
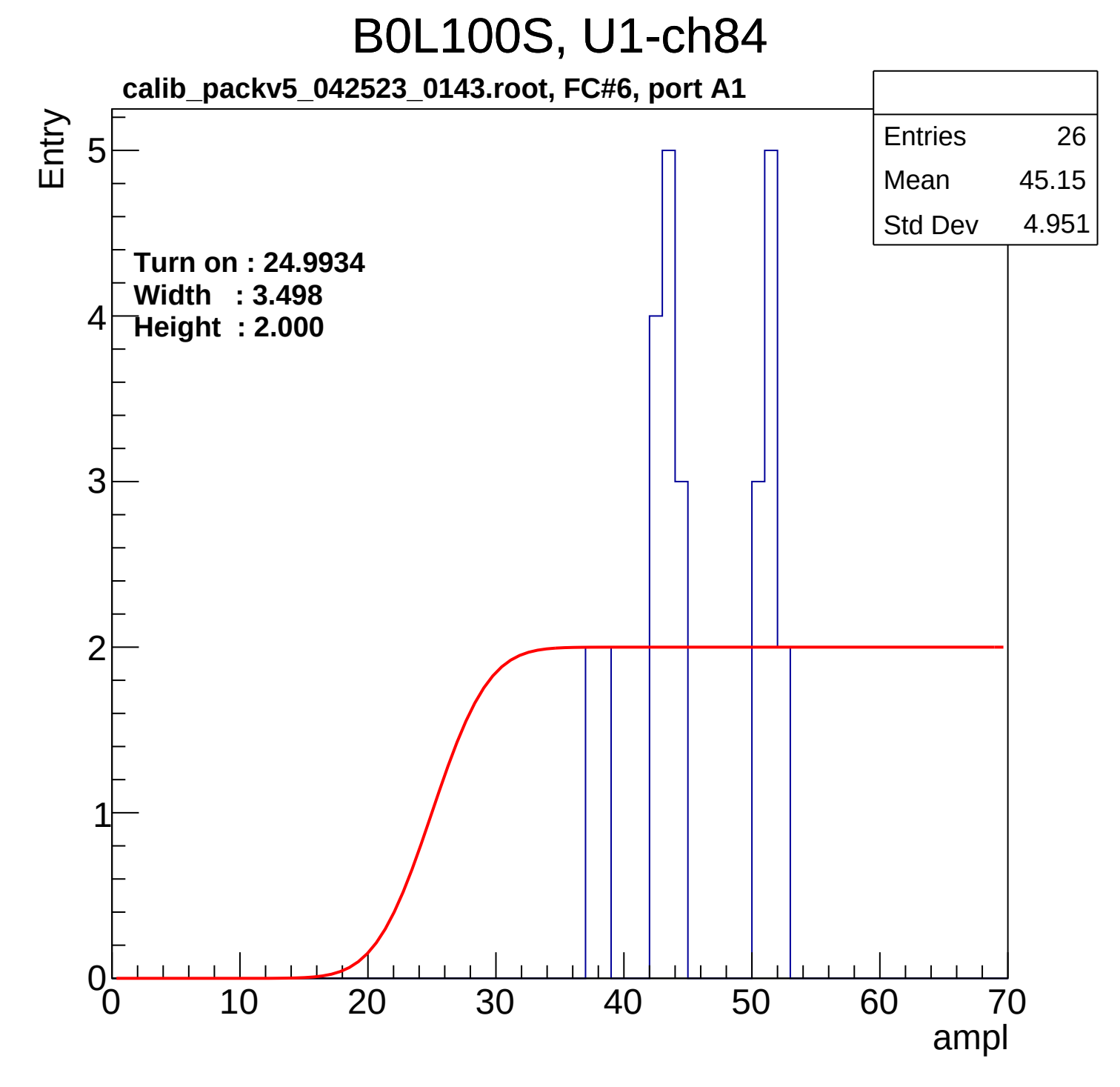
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B0L100S, U1-ch82
calib_packv5_042523_0143.root, FC#6, port A1
Entries 21
Mean 46.62
Std Dev 1.214
Turn on : 24.9955
Width : 3.499
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B0L100S, U1-ch83
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U1-ch84
calib_packv5_042523_0143.root, FC#6, port A1
Entries 26
Mean 45.15
Std Dev 4.951
Turn on : 24.9934
Width : 3.498
Height : 2.000
Entry
ampl
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1
2
3
4
5
0
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40
50
60
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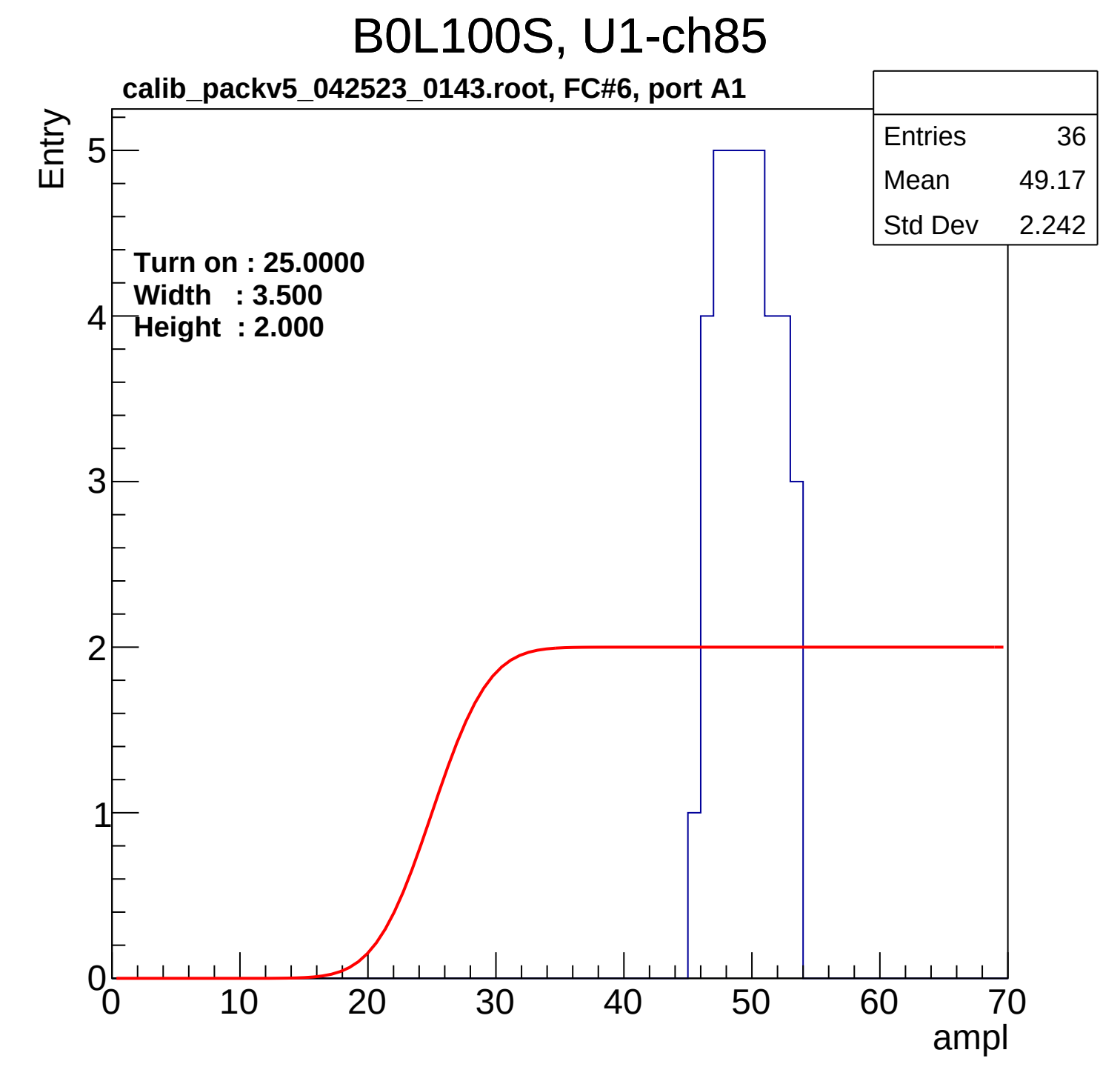
B0L100S, U1-ch85
calib_packv5_042523_0143.root, FC#6, port A1
Entries 36
Mean 49.17
Std Dev 2.242
Turn on : 25.0000
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
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40
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60
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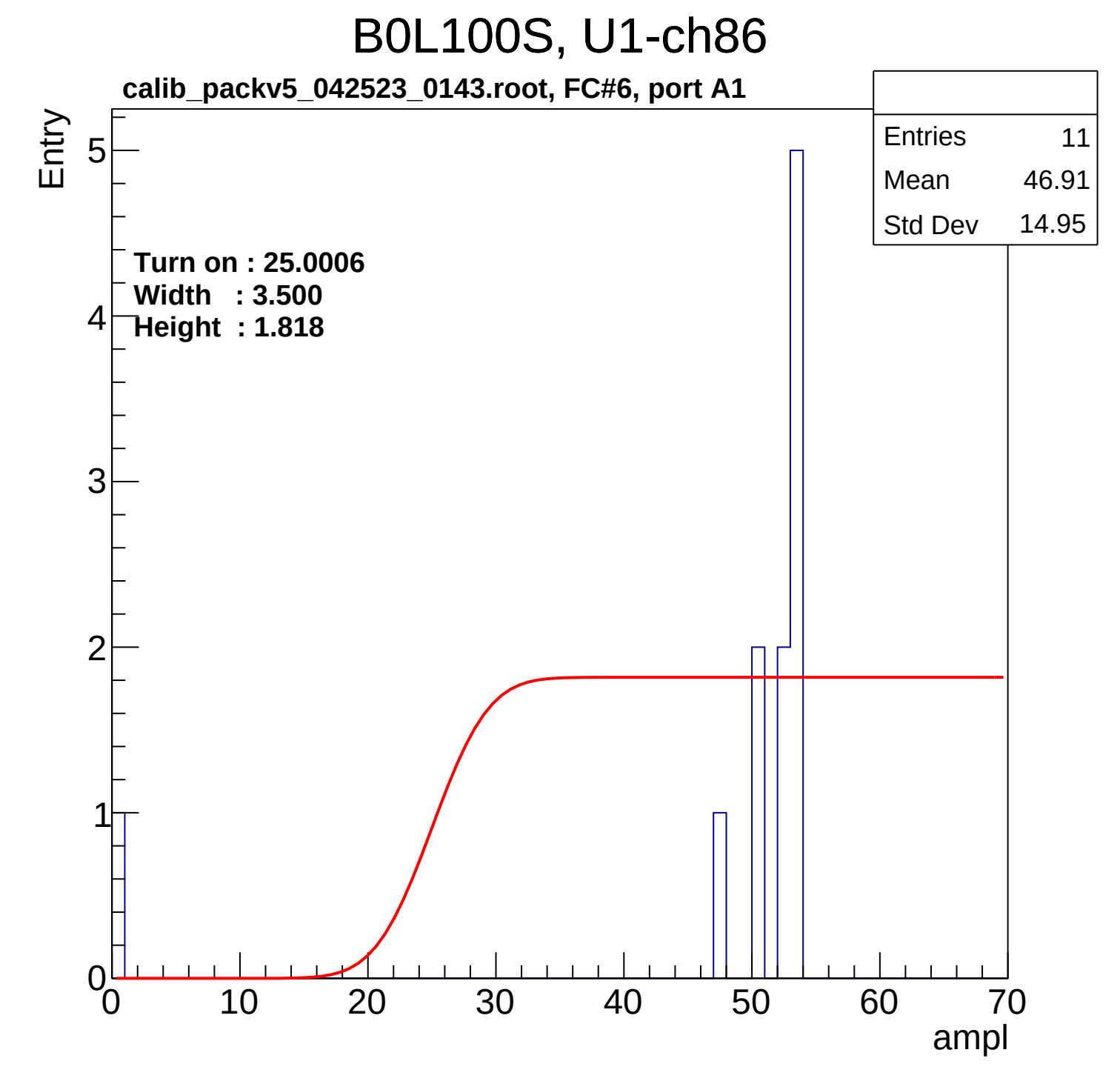
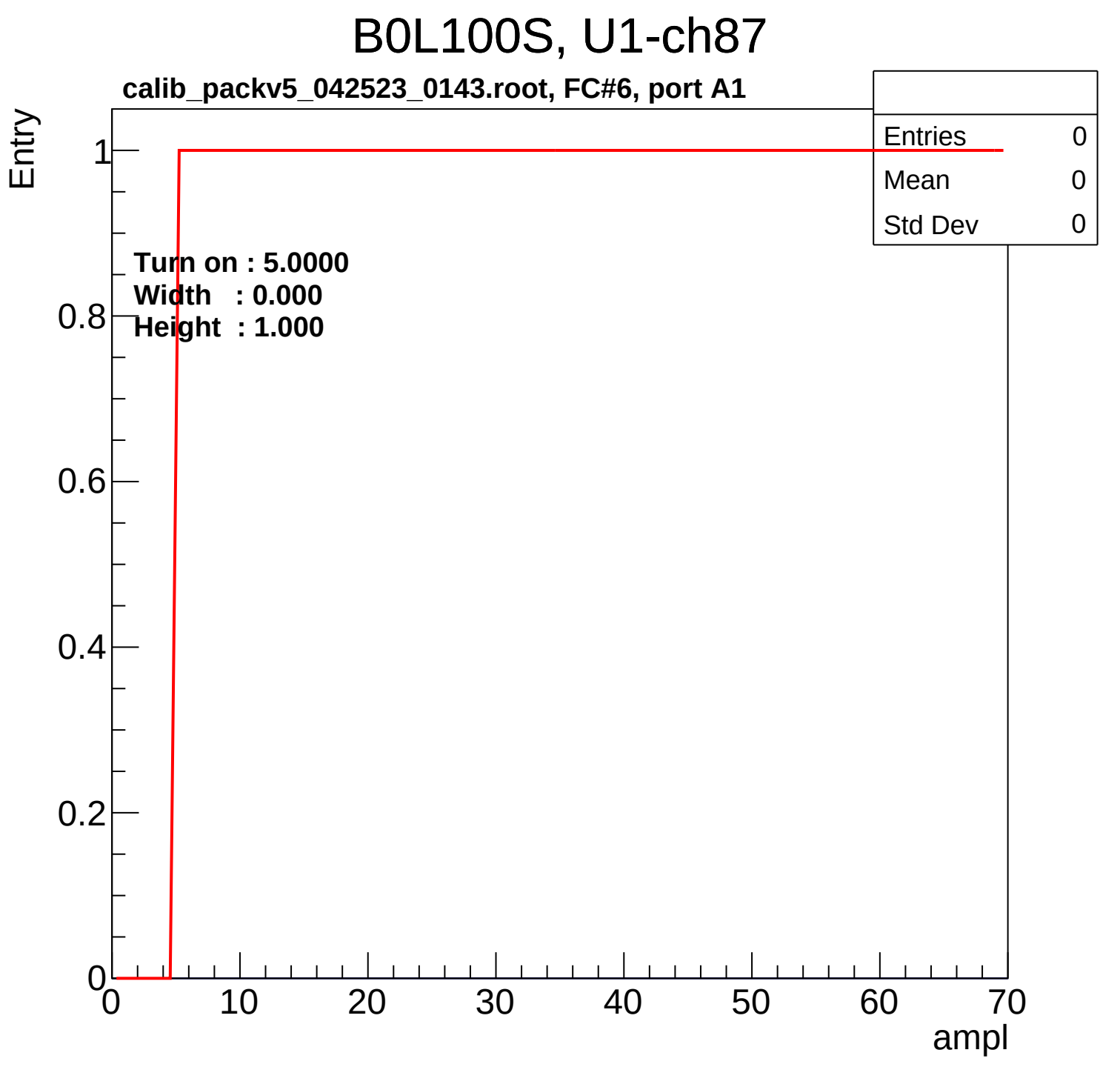

B0L100S, U1-ch86
calib_packv5_042523_0143.root, FC#6, port A1
Entries 11
Mean 46.91
Std Dev 14.95
Turn on : 25.0006
Width : 3.500
Height : 1.818
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B0L100S, U1-ch87
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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0.6
0.4
0.2
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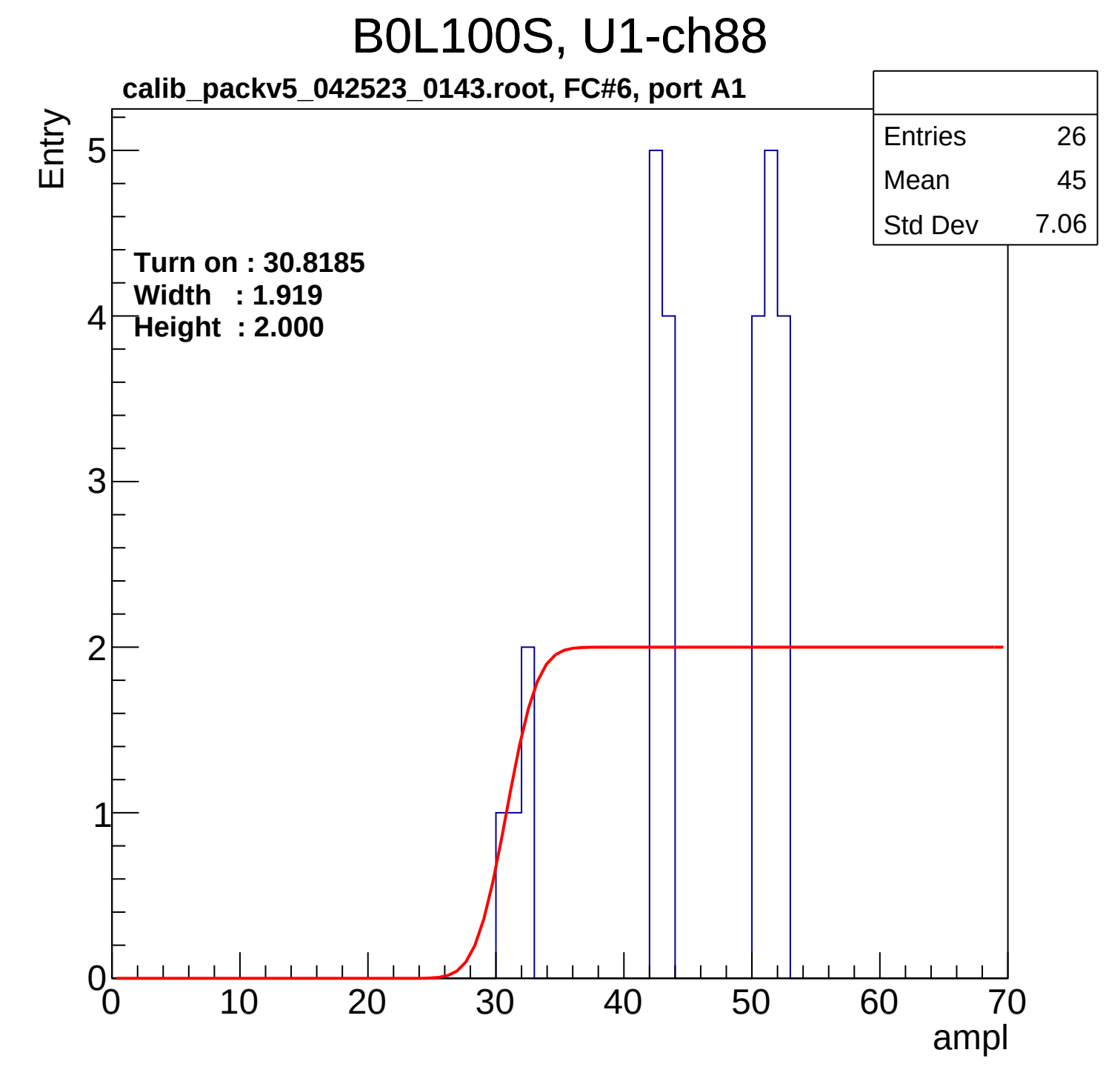
ampl


B0L100S, U1-ch88
calib_packv5_042523_0143.root, FC#6, port A1
Entries 26
Mean 45
Std Dev 7.06
Turn on : 30.8185
Width : 1.919
Height : 2.000
Entry
ampl
0
1
2
3
4
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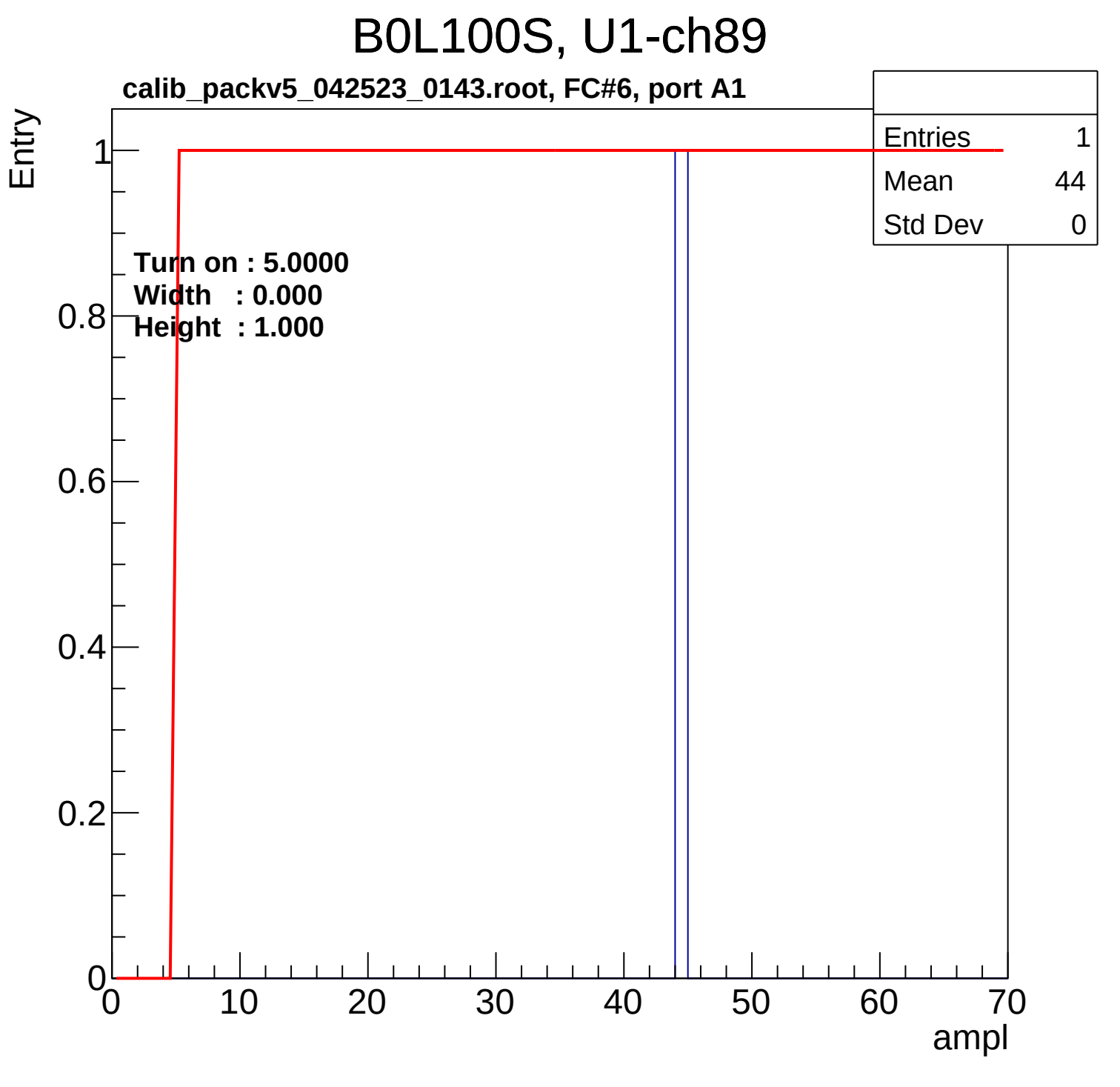
B0L100S, U1-ch89
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 44
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.2
0.4
0.6
0.8
1
0
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60
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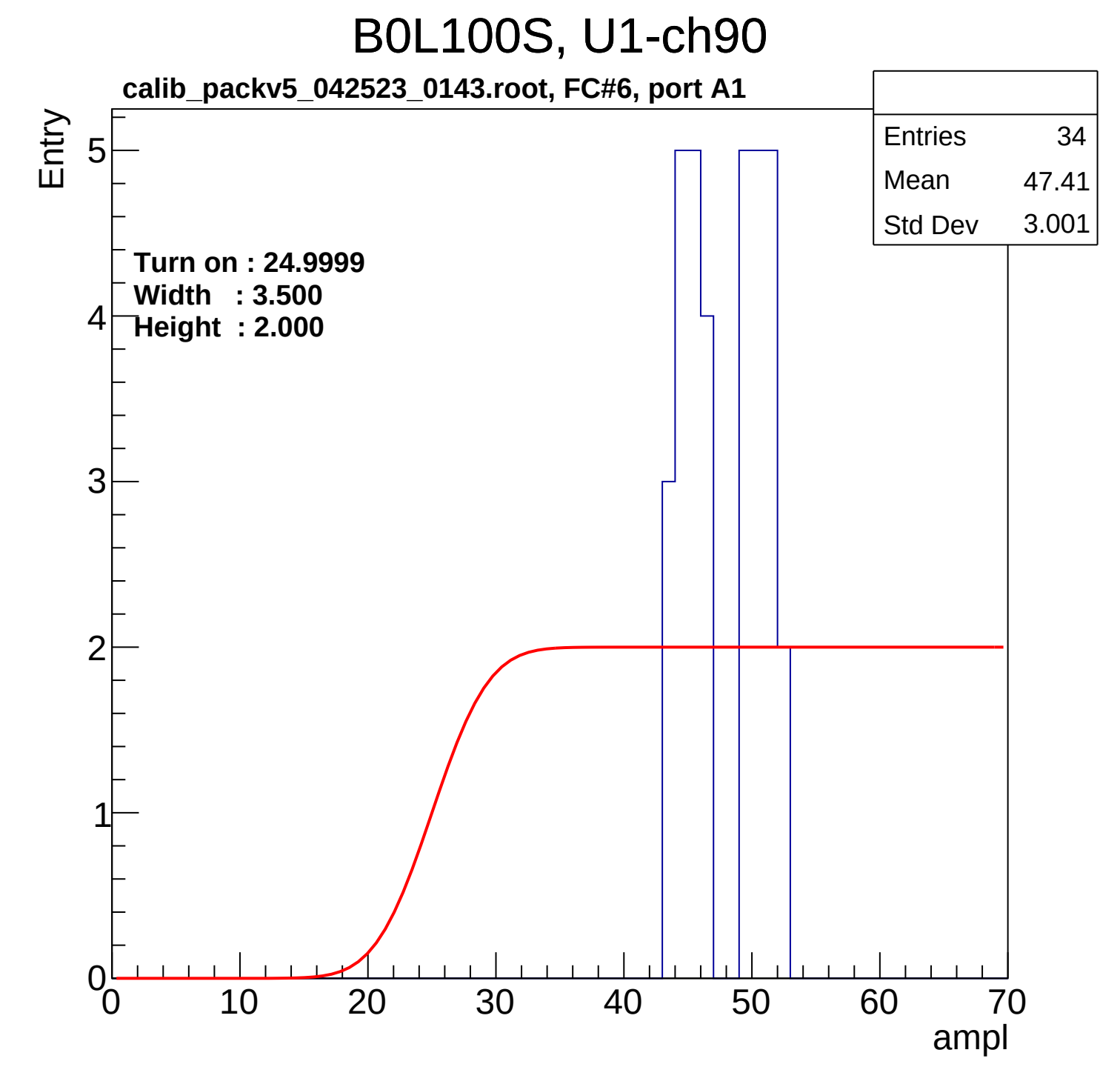
B0L100S, U1-ch90
calib_packv5_042523_0143.root, FC#6, port A1
Entries 34
Mean 47.41
Std Dev 3.001
Turn on : 24.9999
Width : 3.500
Height : 2.000
Entry
ampl
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1
2
3
4
5
0
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40
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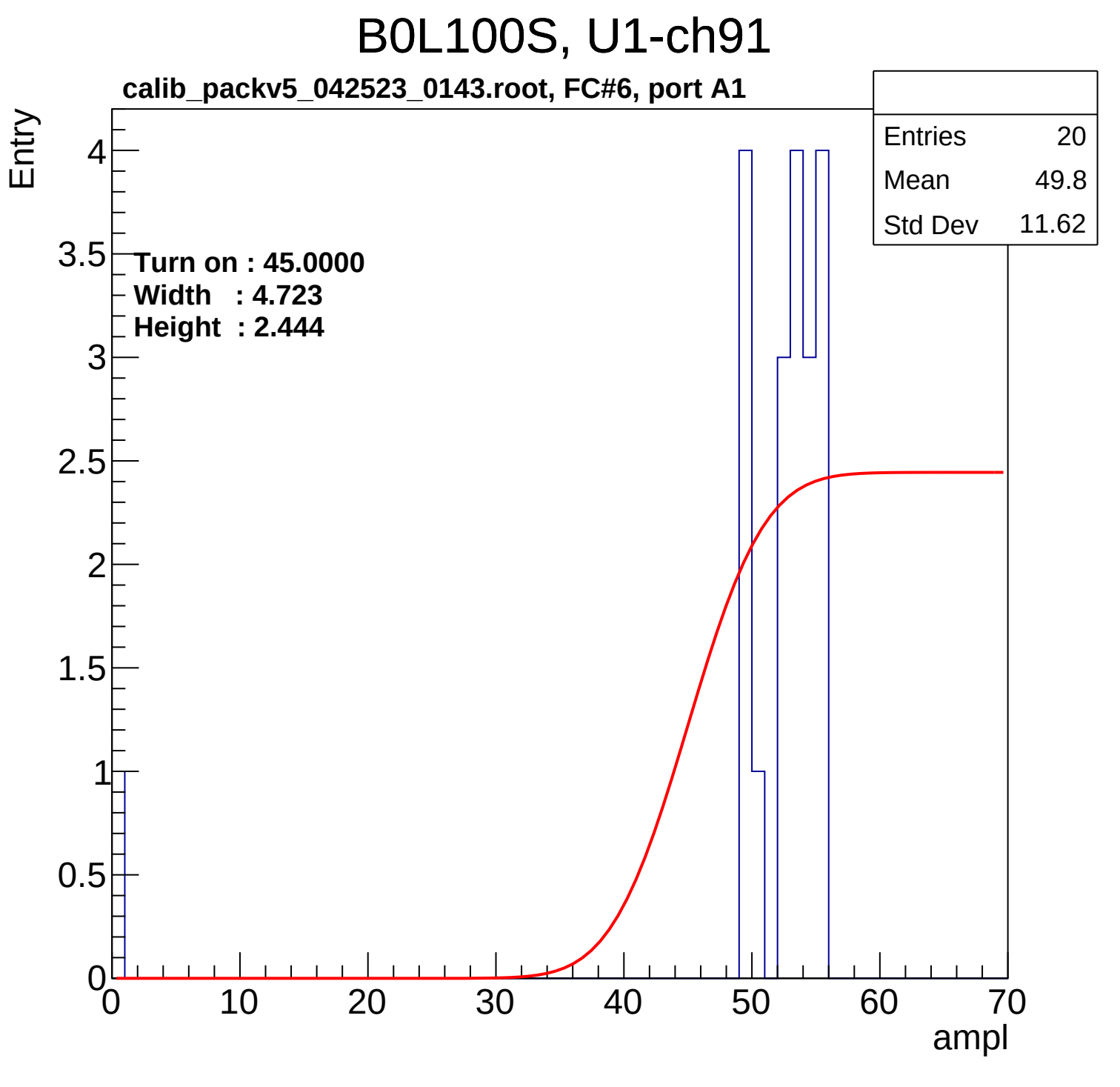
B0L100S, U1-ch91
calib_packv5_042523_0143.root, FC#6, port A1
Entries 20
Mean 49.8
Std Dev 11.62
Turn on : 45.0000
Width : 4.723
Height : 2.444
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
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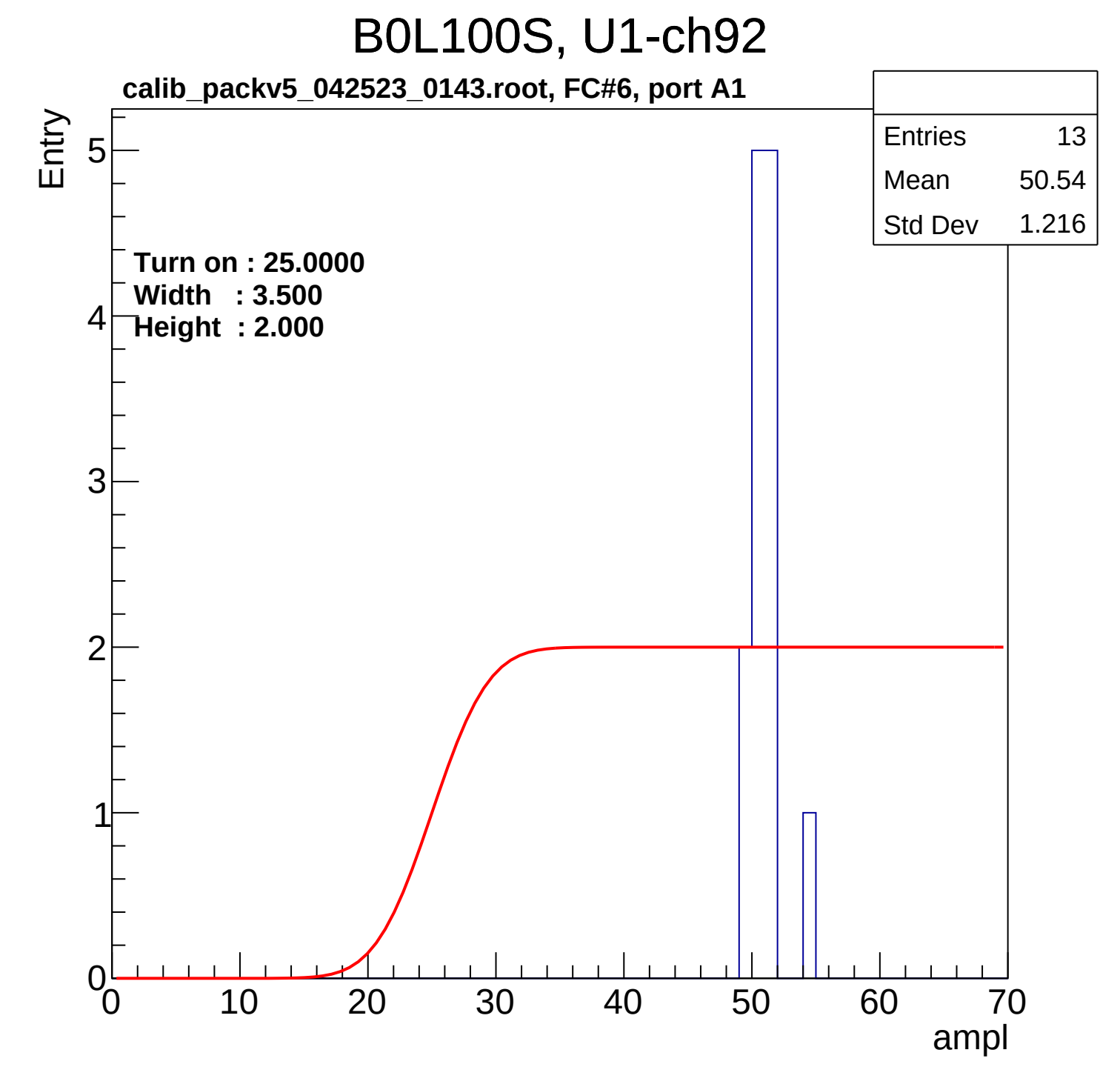
B0L100S, U1-ch92
calib_packv5_042523_0143.root, FC#6, port A1
Entries 13
Mean 50.54
Std Dev 1.216
Turn on : 25.0000
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
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40
50
60
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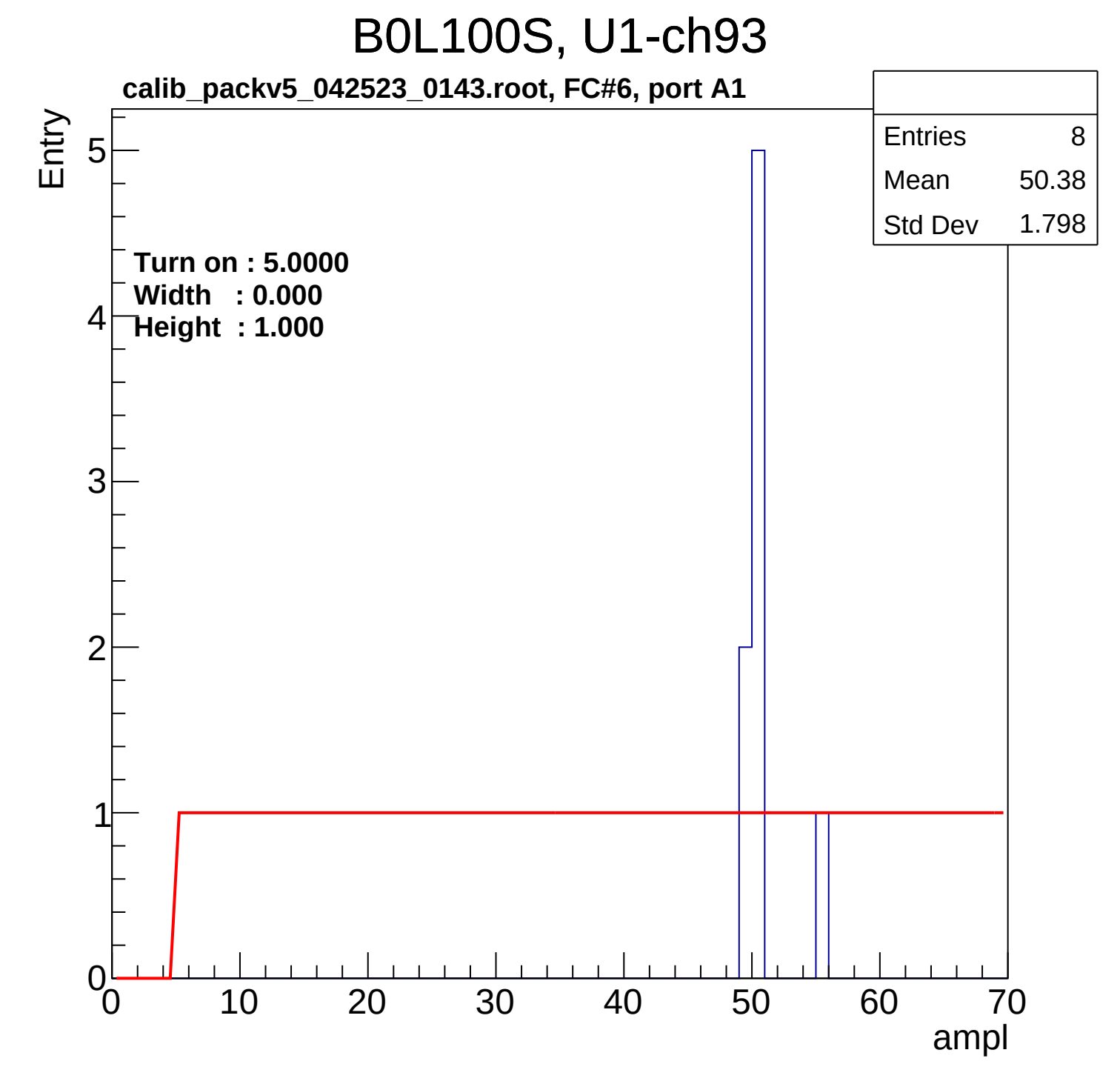
B0L100S, U1-ch93
calib_packv5_042523_0143.root, FC#6, port A1
Entries 8
Mean 50.38
Std Dev 1.798
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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1
2
3
4
5
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50
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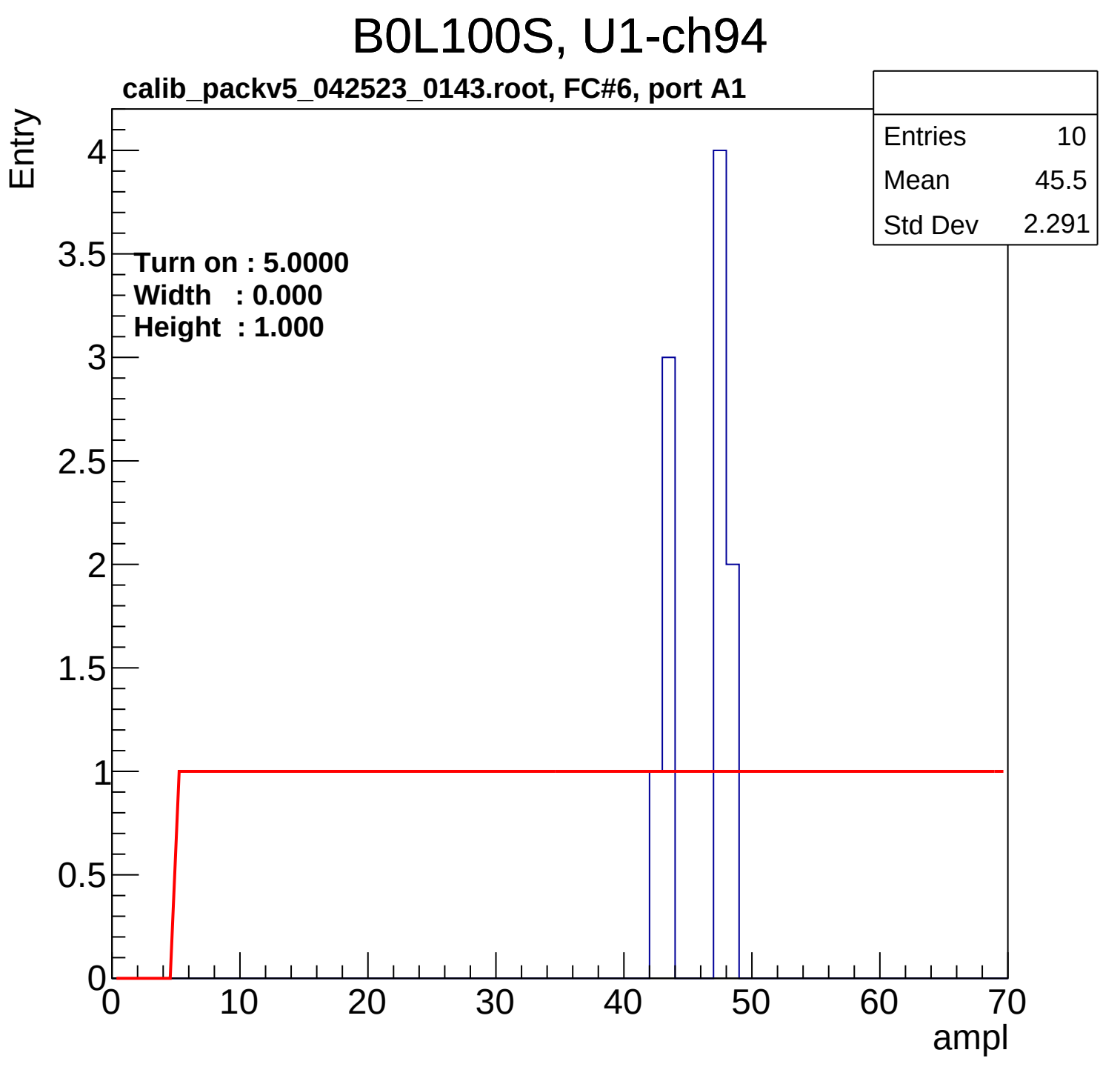
70
ampl


B0L100S, U1-ch94
calib_packv5_042523_0143.root, FC#6, port A1
Entries 10
Mean 45.5
Std Dev 2.291
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
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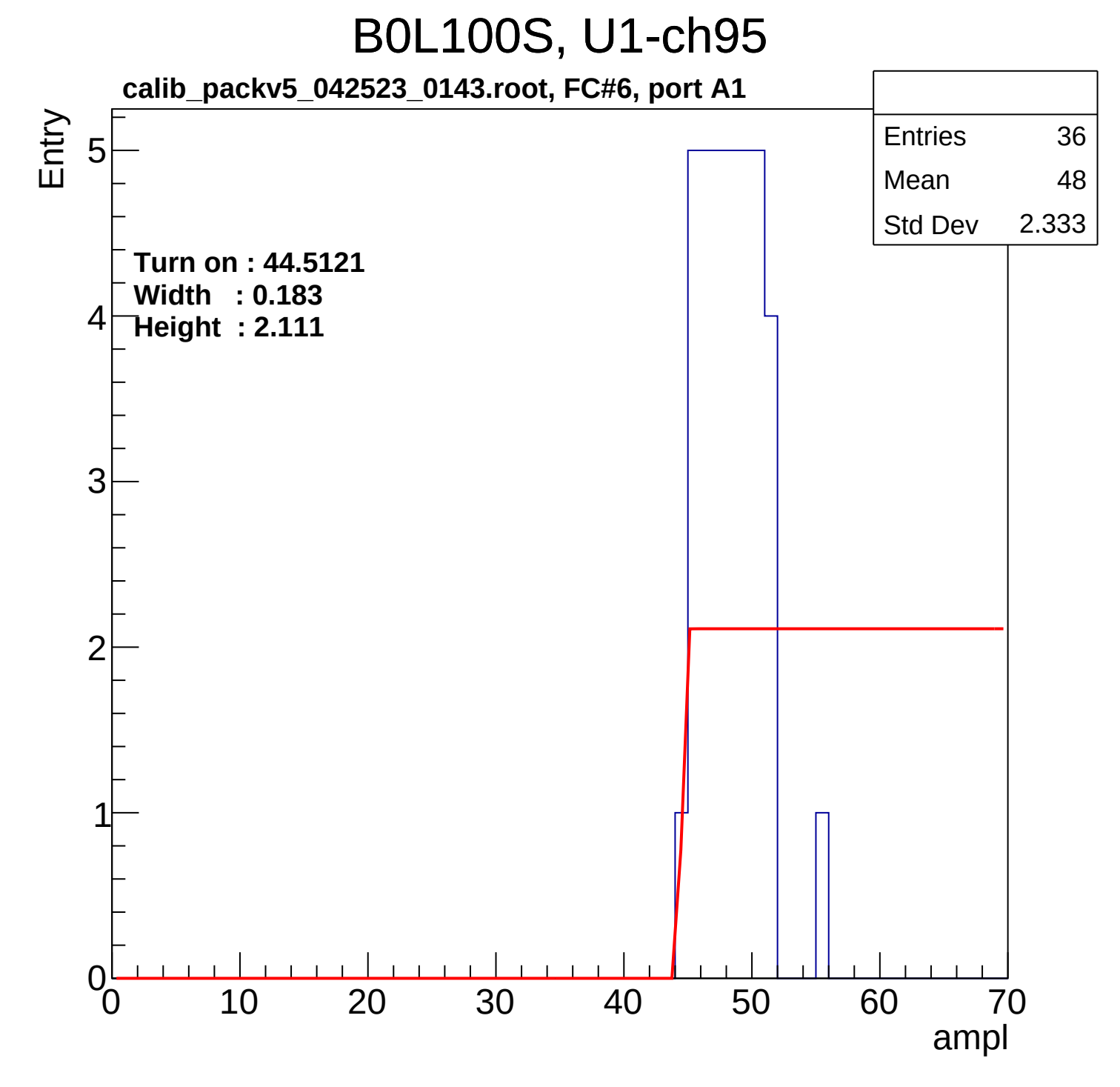
40
50
60
70


B0L100S, U1-ch95
calib_packv5_042523_0143.root, FC#6, port A1
Entries 36
Mean 48
Std Dev 2.333
Turn on : 44.5121
Width : 0.183
Height : 2.111
Entry
ampl
0
1
2
3
4
5
0
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40
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60
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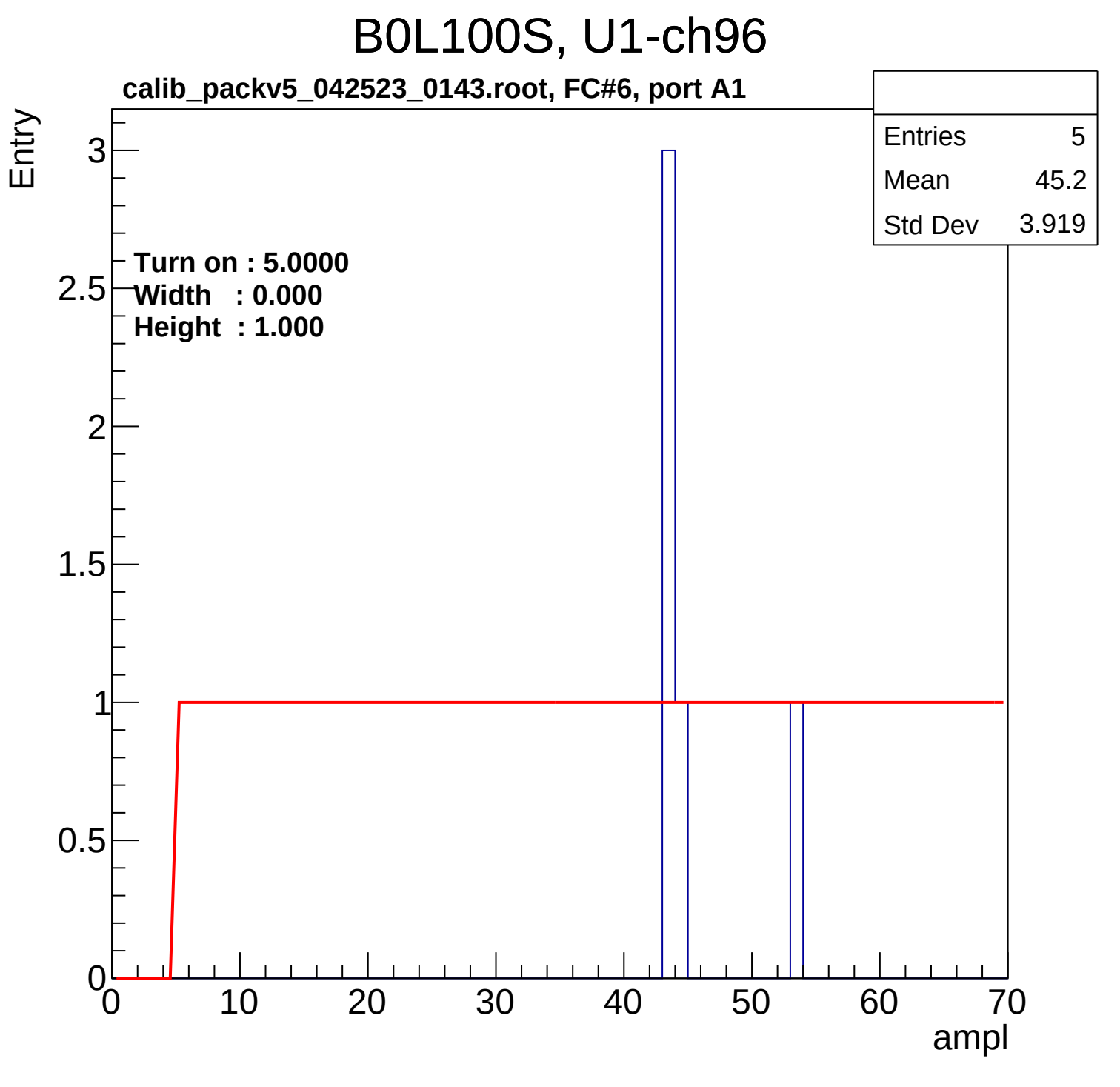
B0L100S, U1-ch96
calib_packv5_042523_0143.root, FC#6, port A1
Entries 5
Mean 45.2
Std Dev 3.919
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
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20
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40
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60
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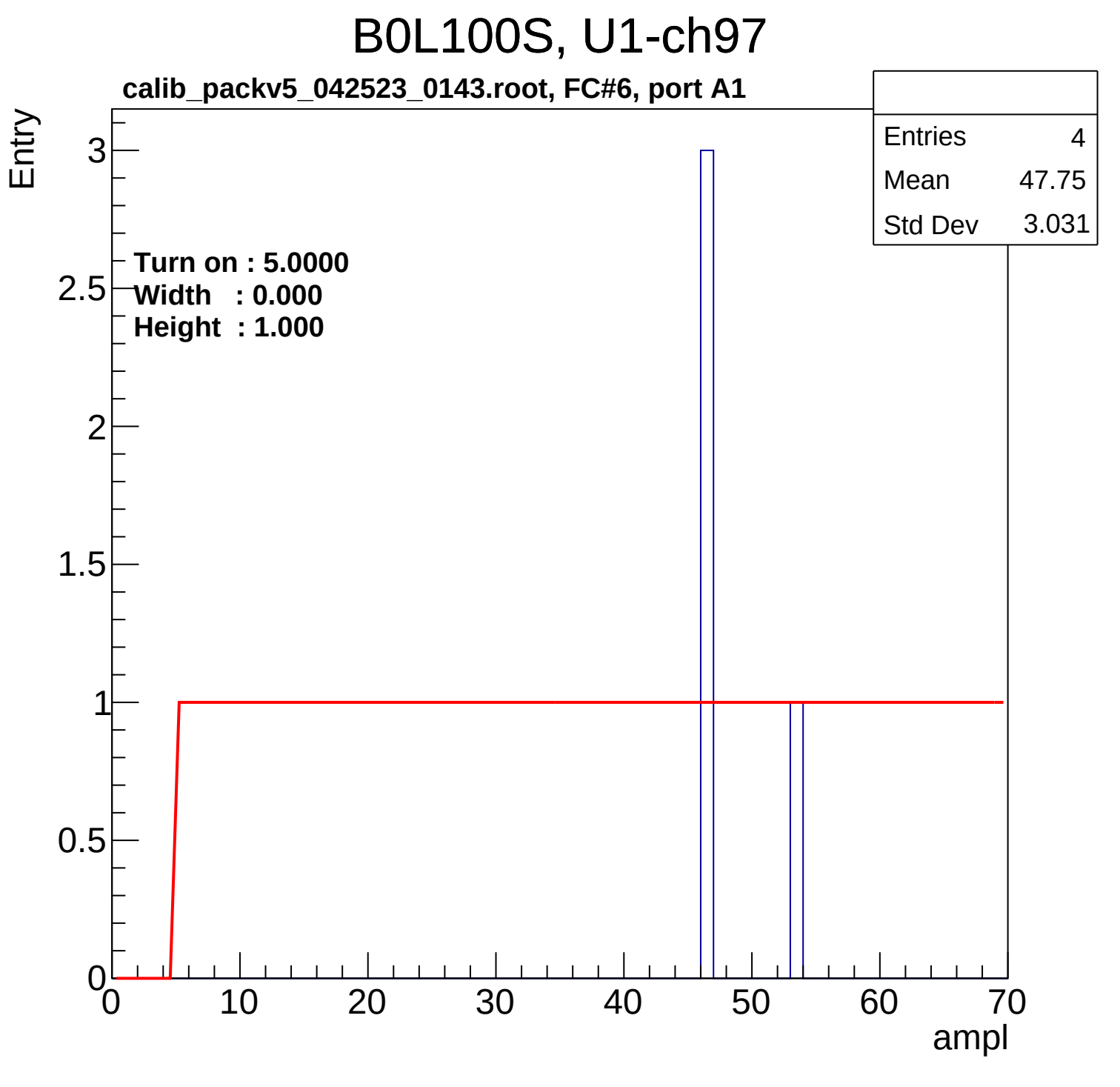
B0L100S, U1-ch97
calib_packv5_042523_0143.root, FC#6, port A1
Entries 4
Mean 47.75
Std Dev 3.031
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.5
1
1.5
2
2.5
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0
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40
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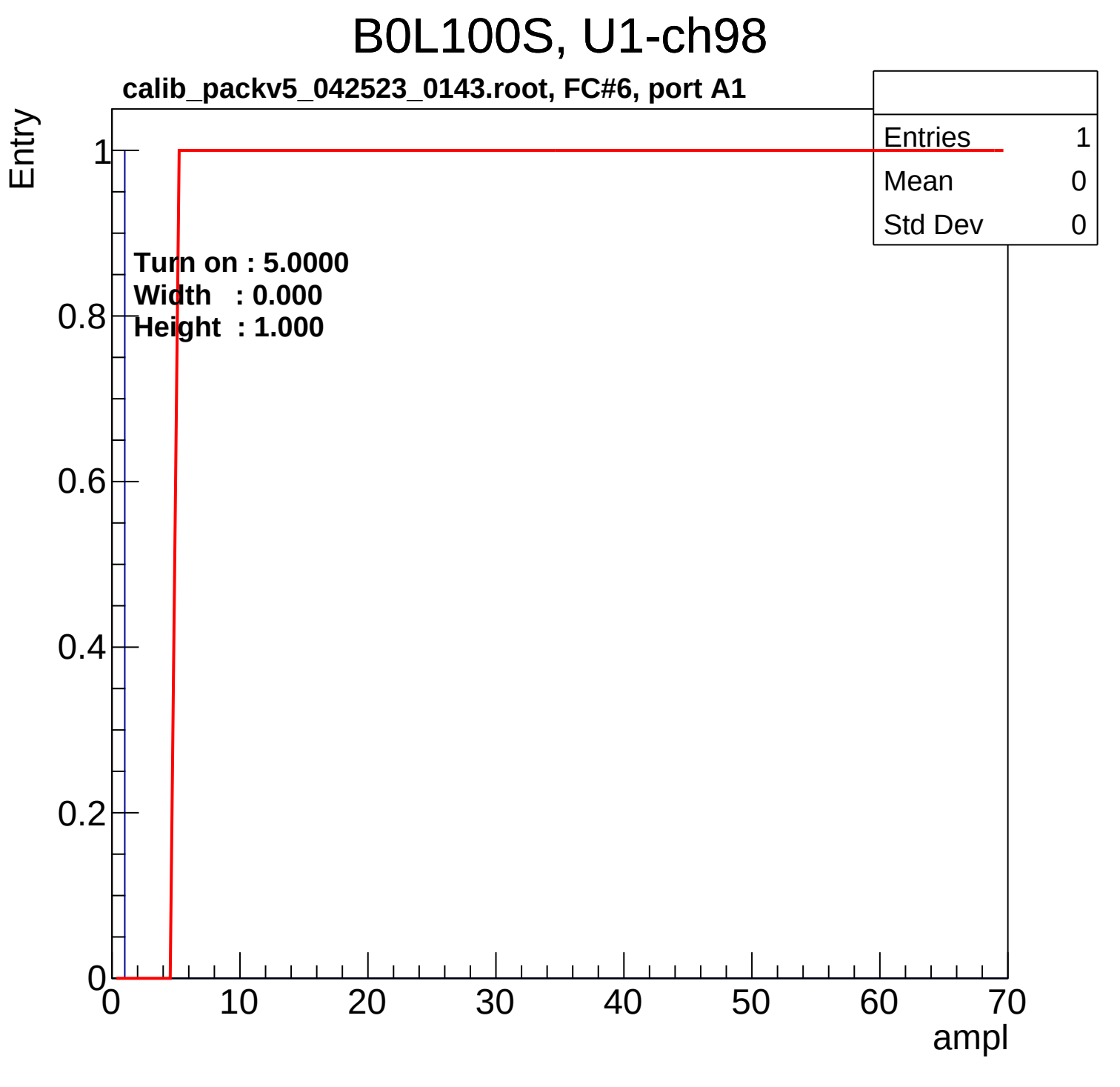
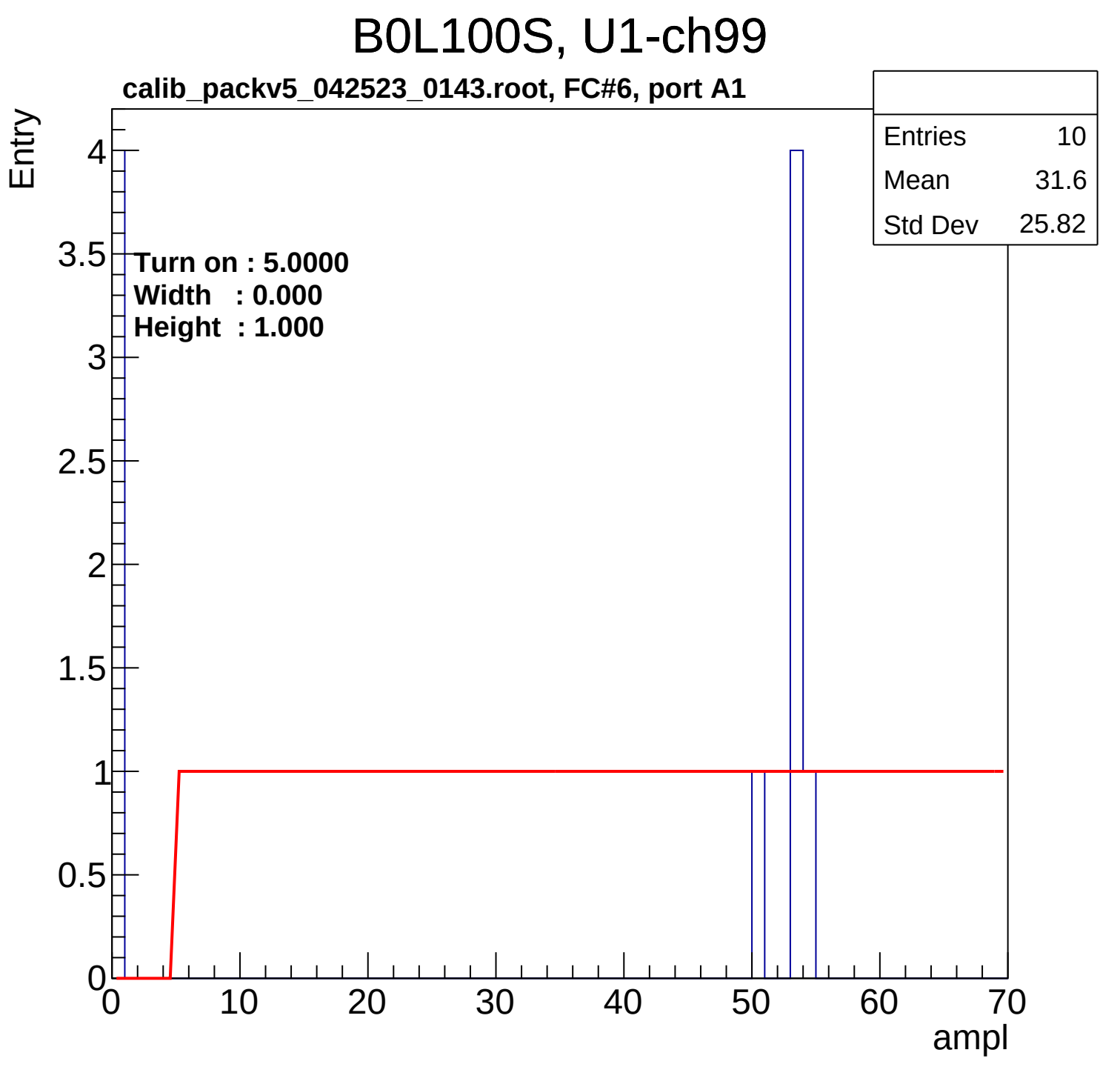

B0L100S, U1-ch98
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U1-ch99
calib_packv5_042523_0143.root, FC#6, port A1
Entries 10
Mean 31.6
Std Dev 25.82
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
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60
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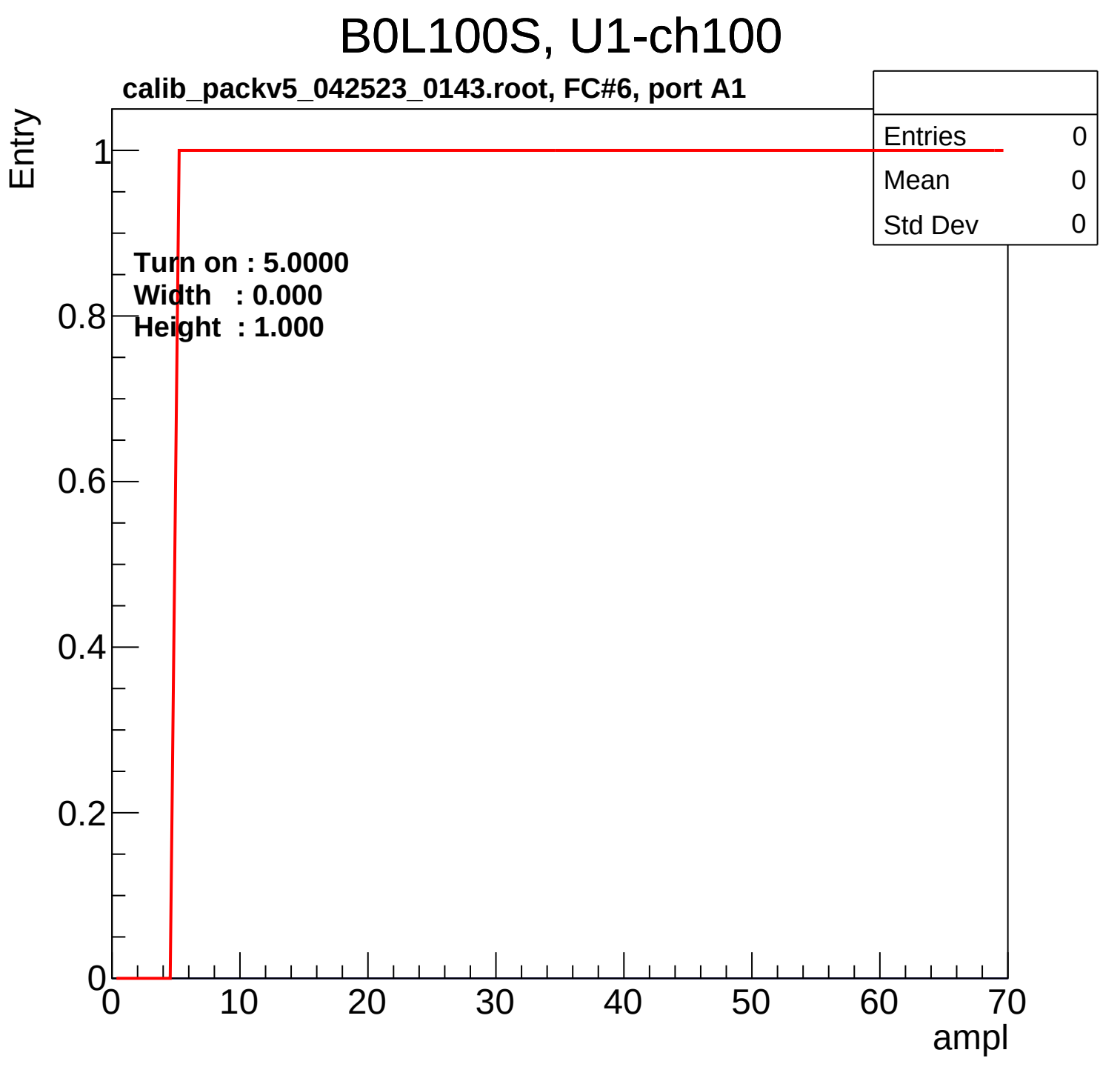
B0L100S, U1-ch100
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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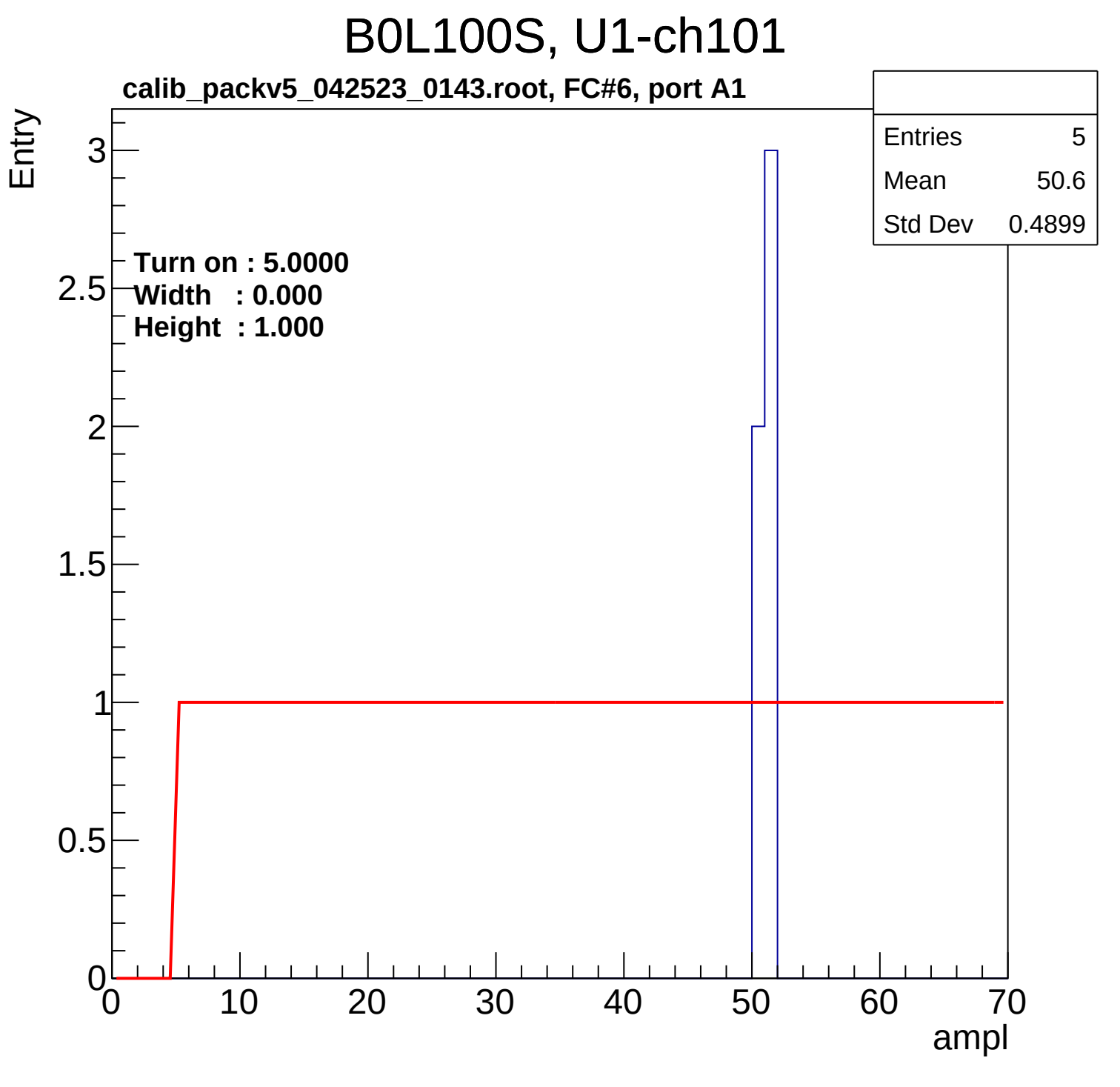
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U1-ch101
calib_packv5_042523_0143.root, FC#6, port A1
Entries 5
Mean 50.6
Std Dev 0.4899
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.5
1
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2.5
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0
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60
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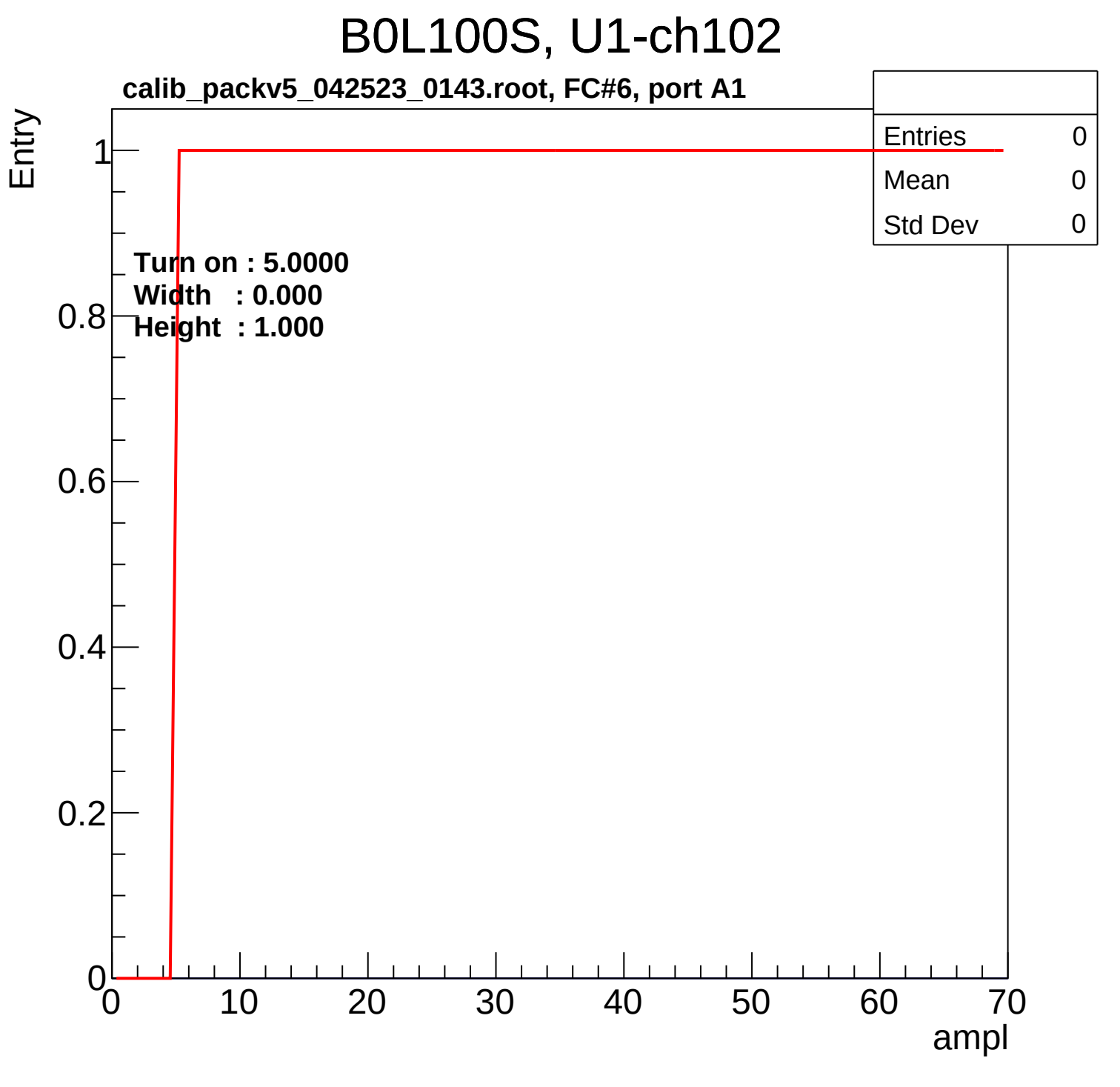
B0L100S, U1-ch102
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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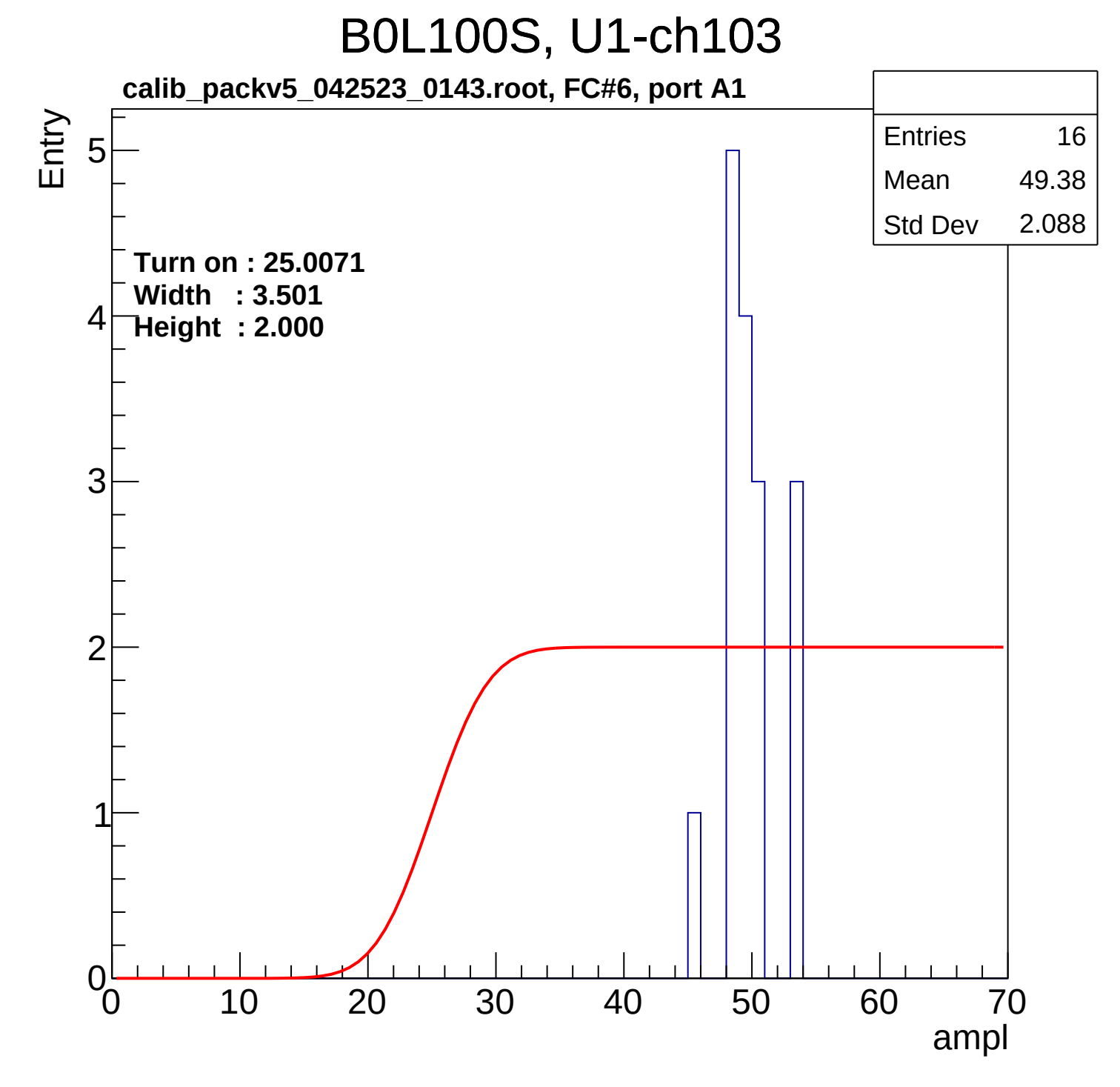
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U1-ch103
calib_packv5_042523_0143.root, FC#6, port A1
Entries 16
Mean 49.38
Std Dev 2.088
Turn on : 25.0071
Width : 3.501
Height : 2.000
Entry
ampl
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1
2
3
4
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0
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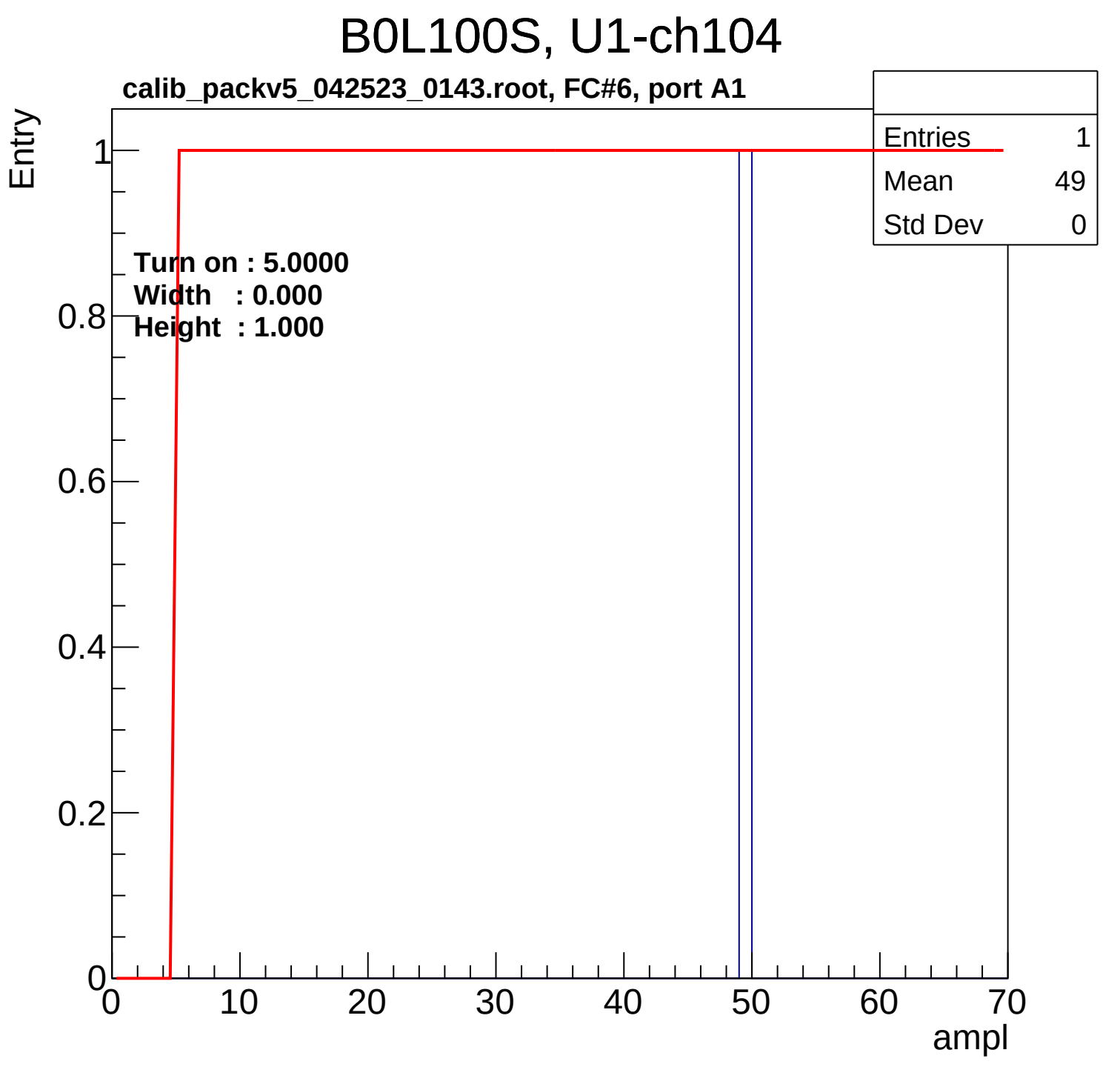
B0L100S, U1-ch104
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 49
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.2
0.4
0.6
0.8
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0
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60
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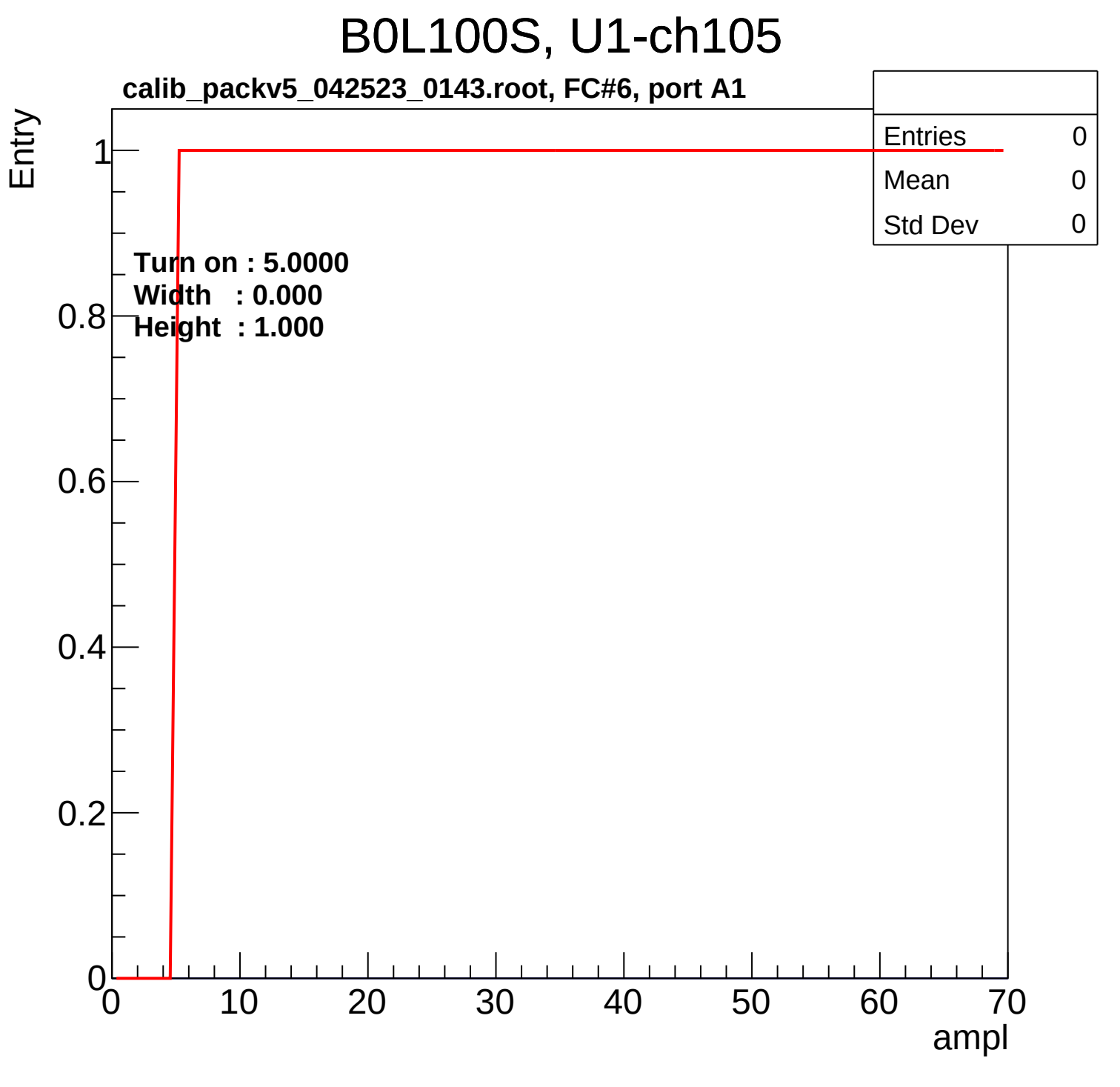
B0L100S, U1-ch105
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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0.6
0.4
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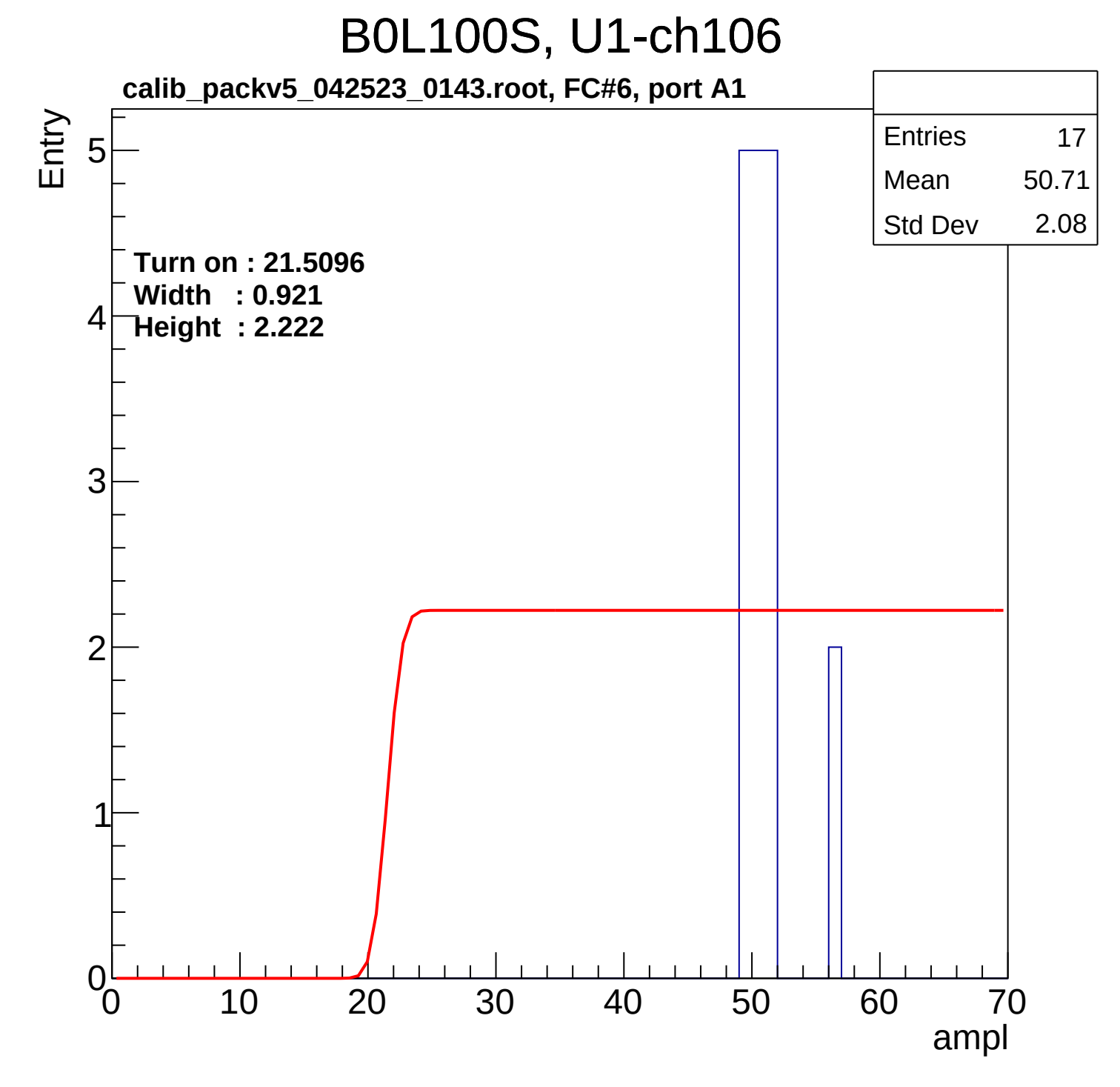
ampl


B0L100S, U1-ch106
calib_packv5_042523_0143.root, FC#6, port A1
Entries 17
Mean 50.71
Std Dev 2.08
Turn on : 21.5096
Width : 0.921
Height : 2.222
Entry
ampl
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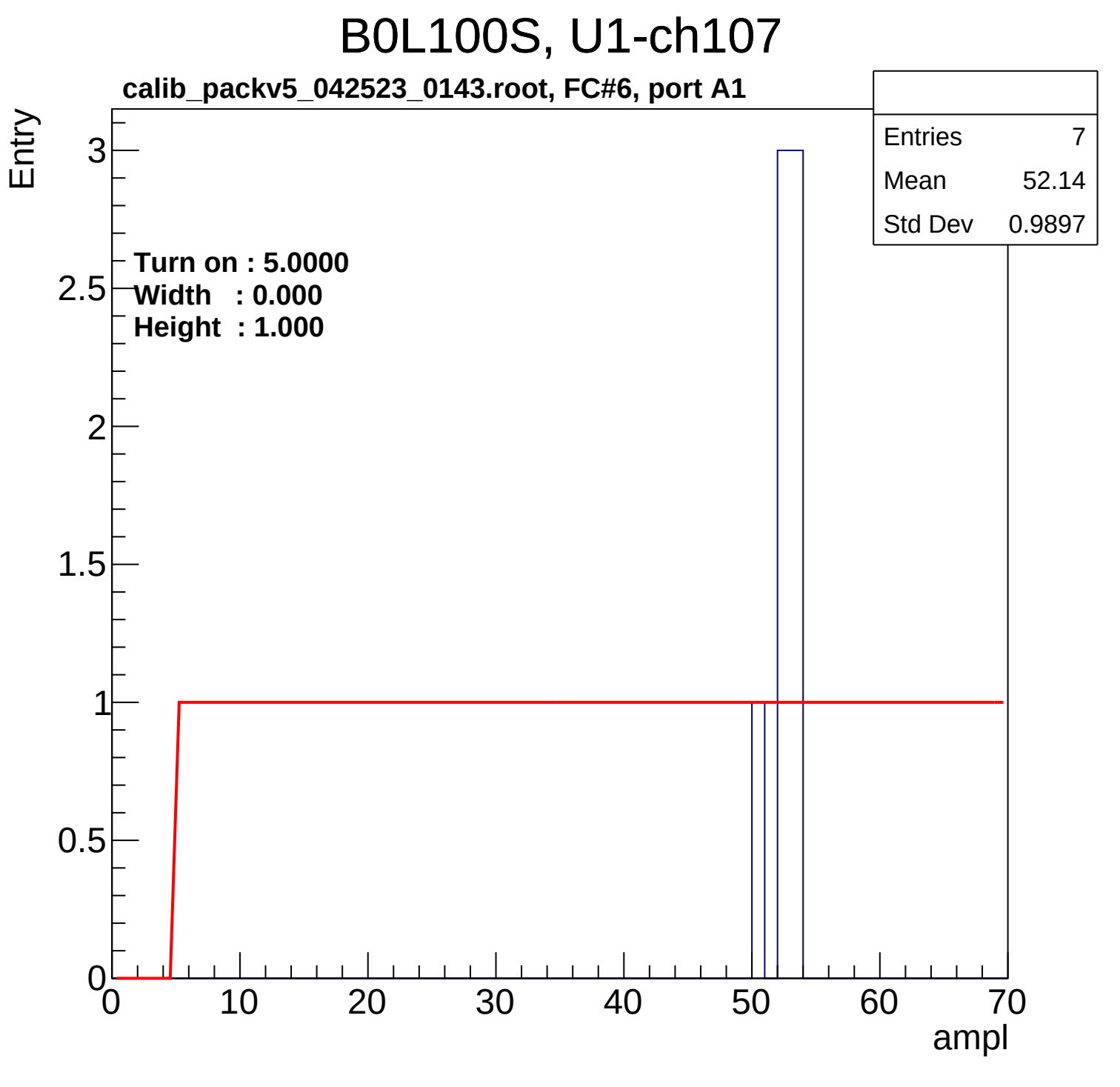
B0L100S, U1-ch107
calib_packv5_042523_0143.root, FC#6, port A1
Entries 7
Mean 52.14
Std Dev 0.9897
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.5
1
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2.5
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0
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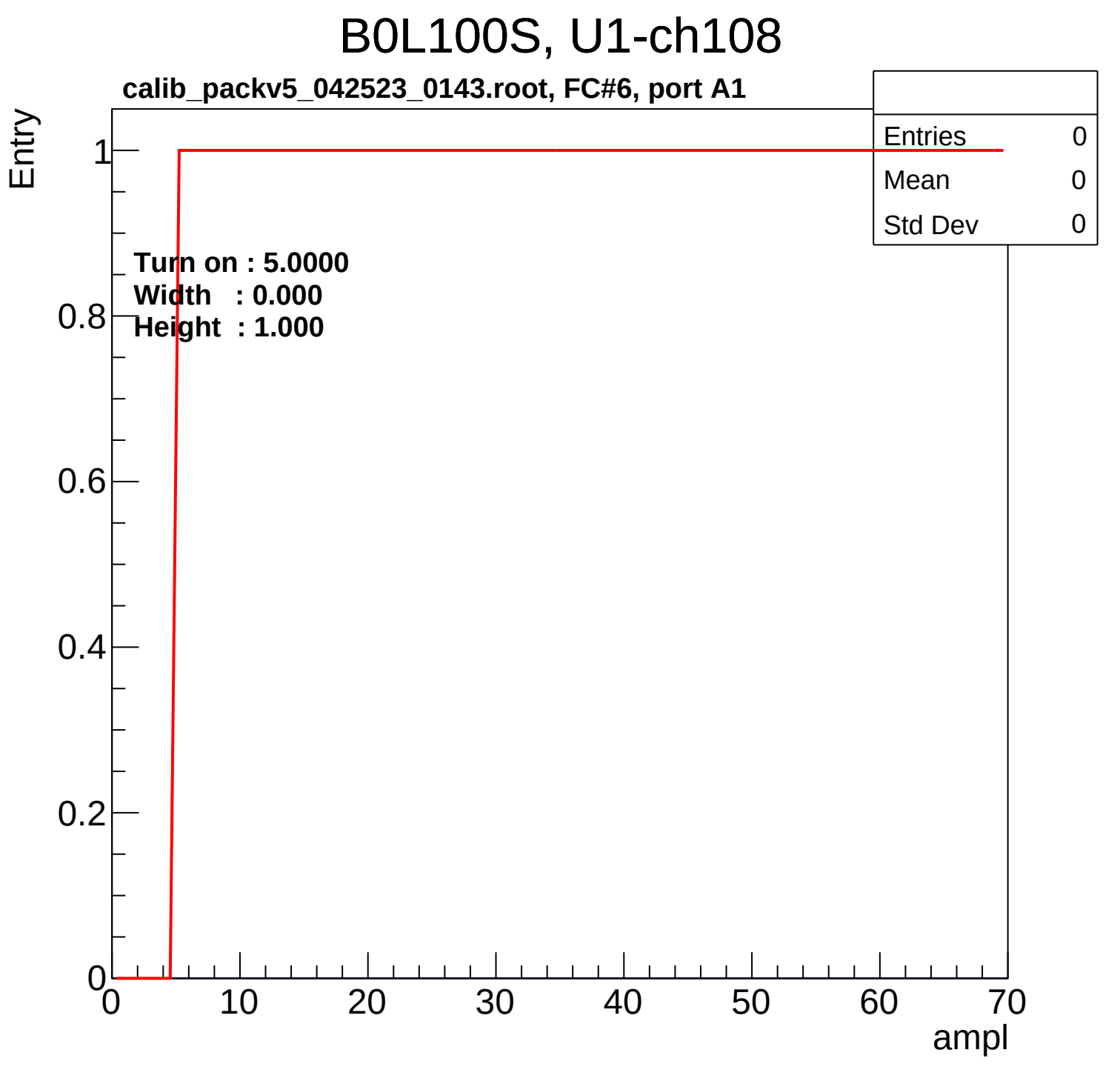
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Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
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0.6
0.4
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10
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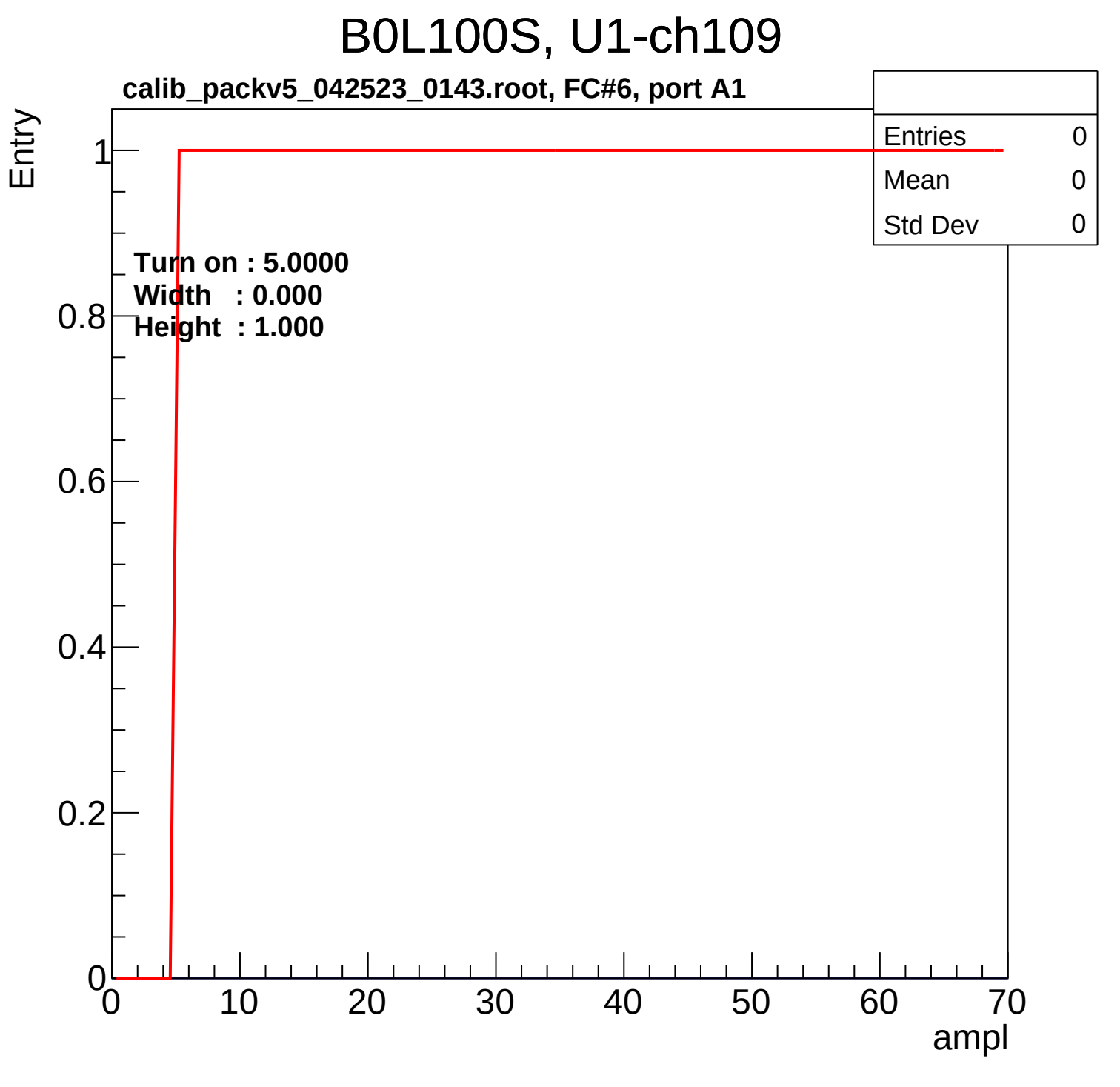
70
ampl


B0L100S, U1-ch109
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
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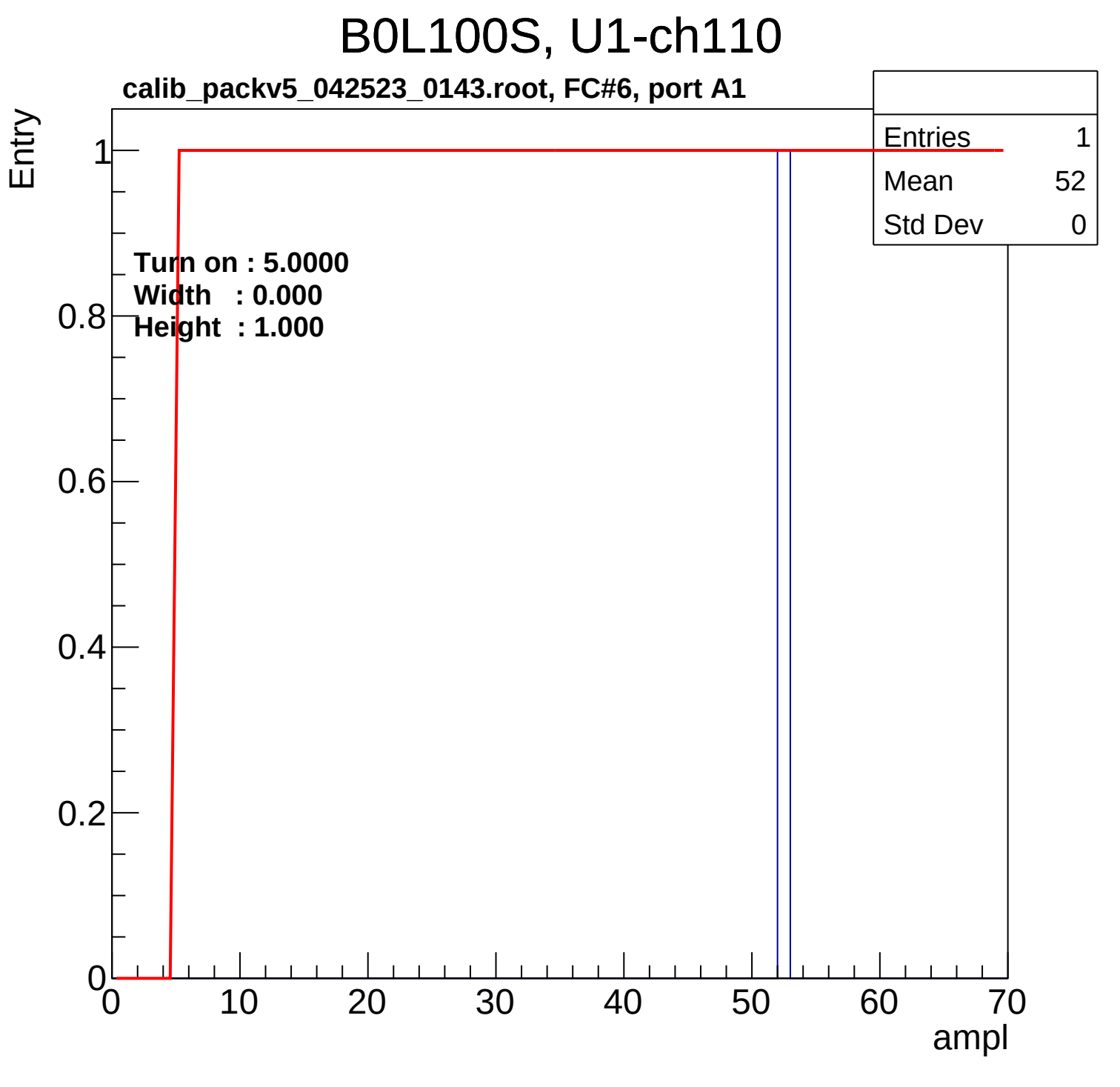
70
ampl


B0L100S, U1-ch110
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 52
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
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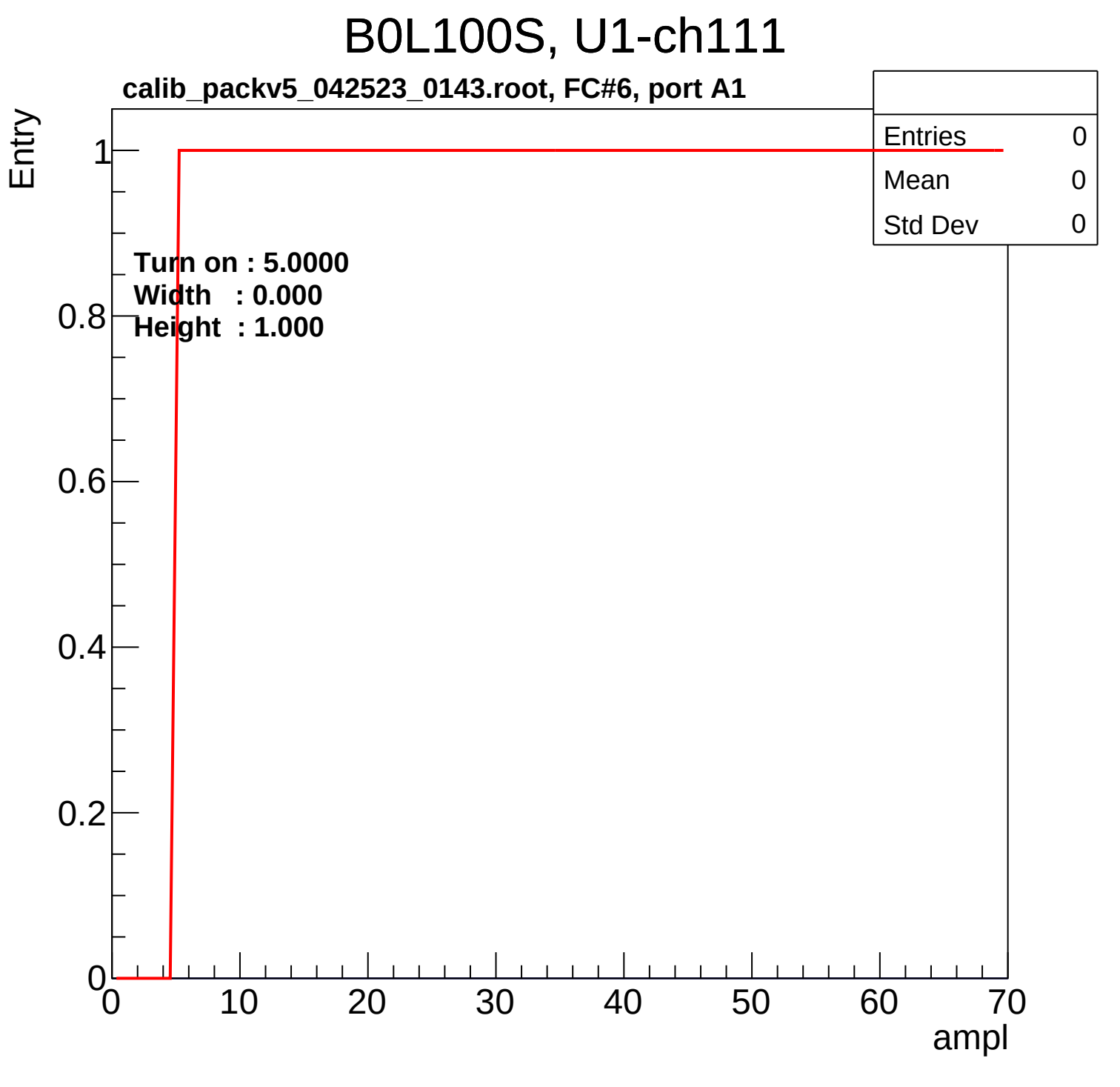
B0L100S, U1-ch111
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
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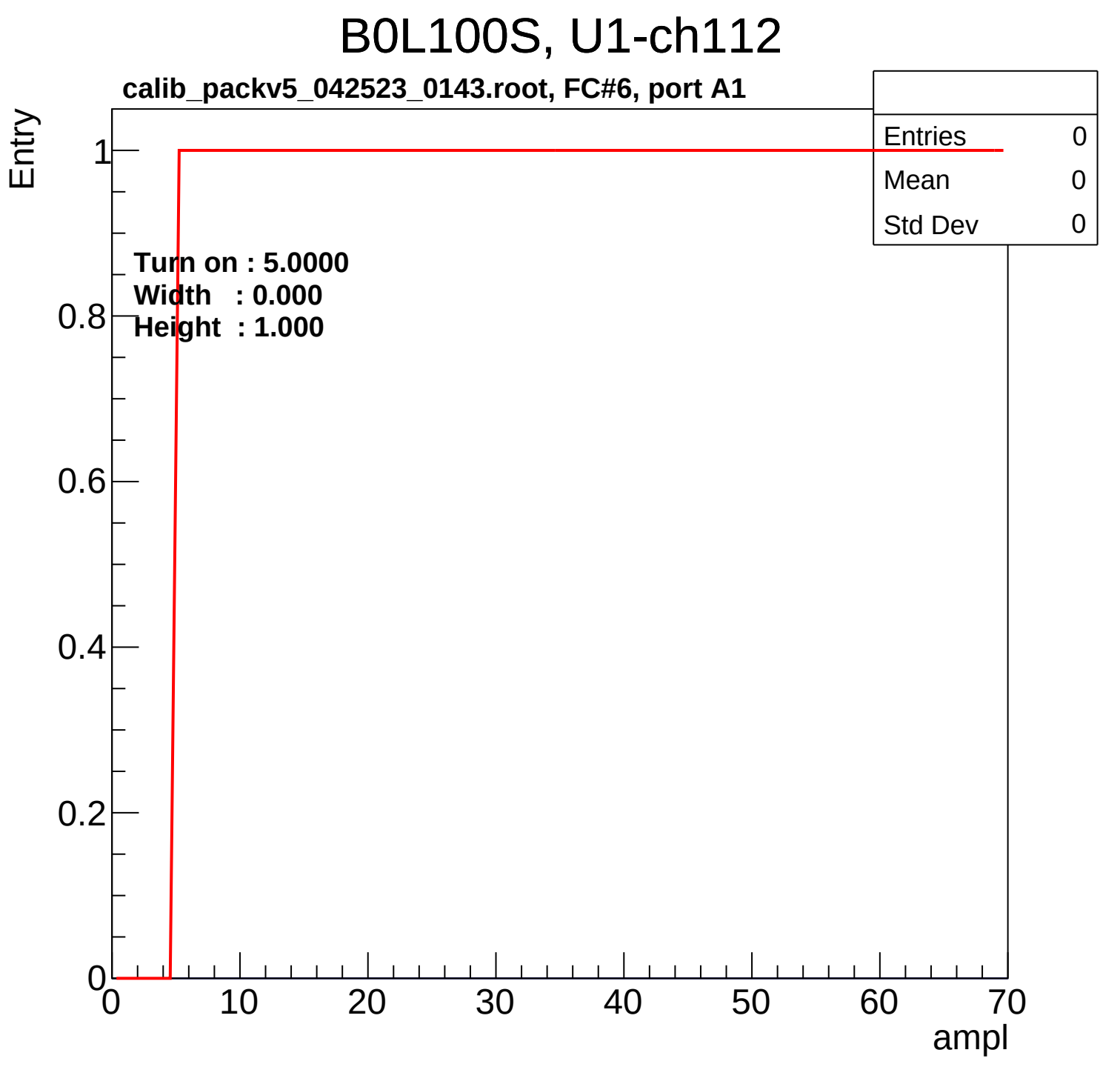
ampl


B0L100S, U1-ch112
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
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0.2
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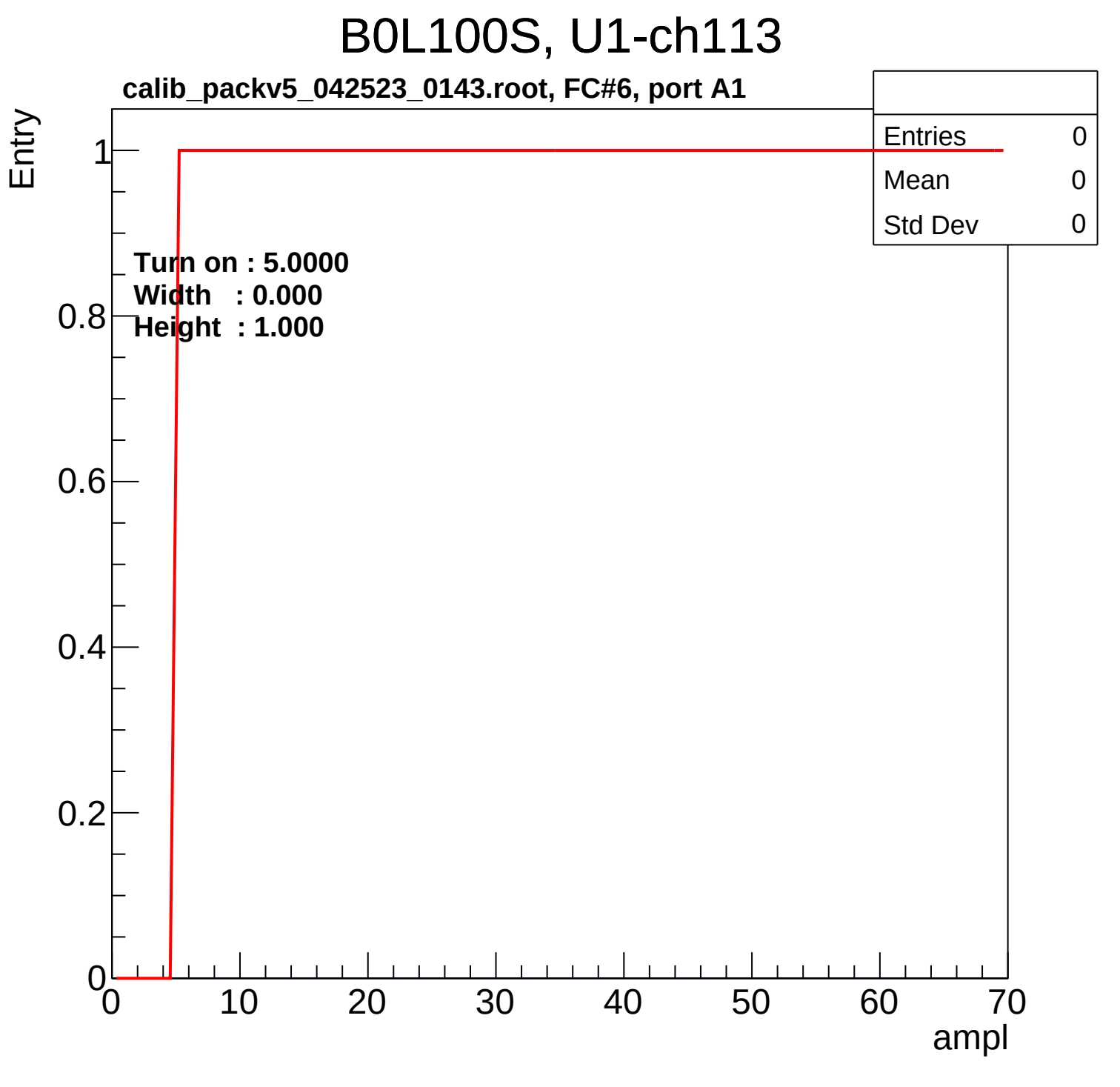
ampl


B0L100S, U1-ch113
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
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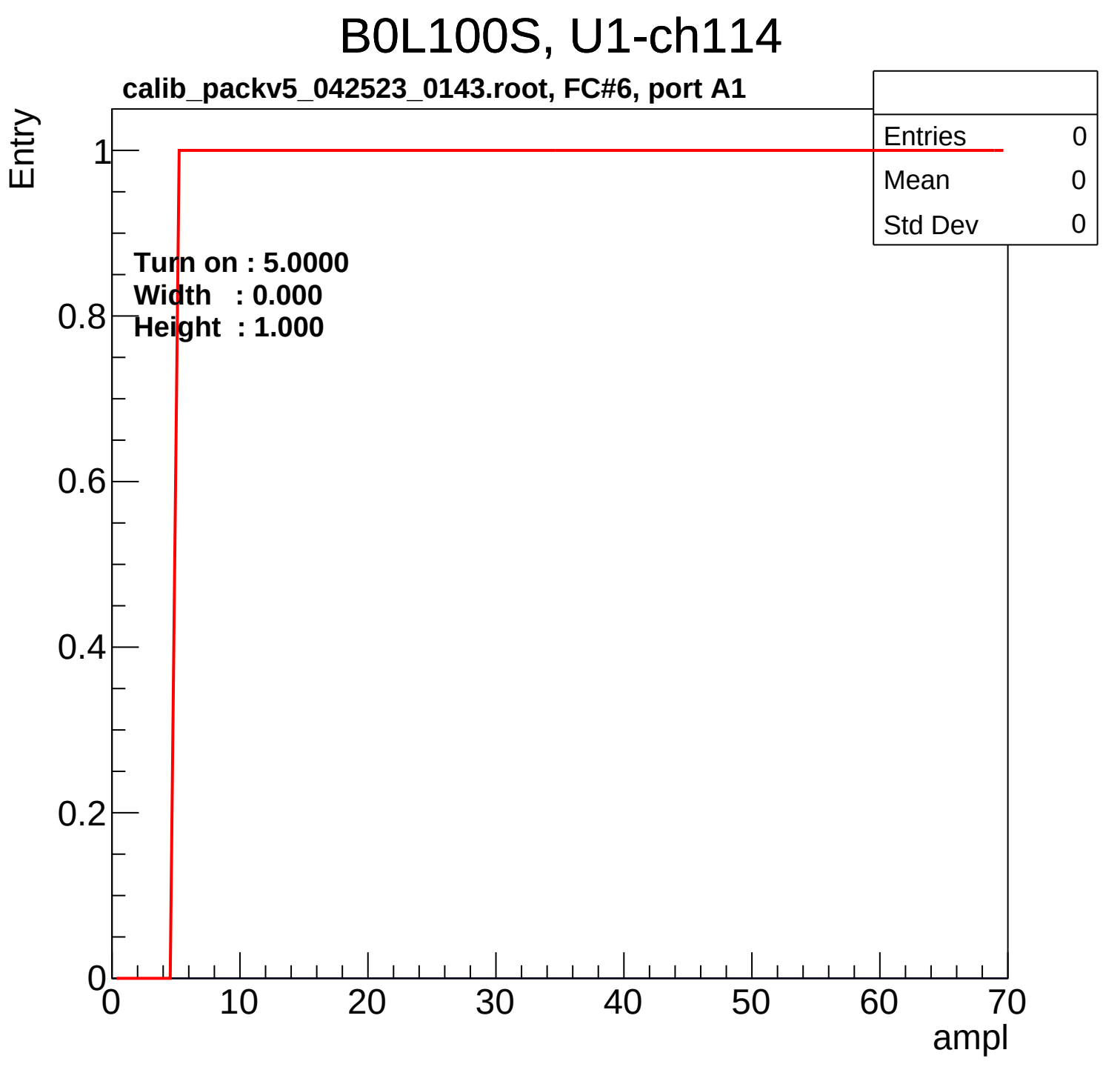
ampl


B0L100S, U1-ch114
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
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0.4
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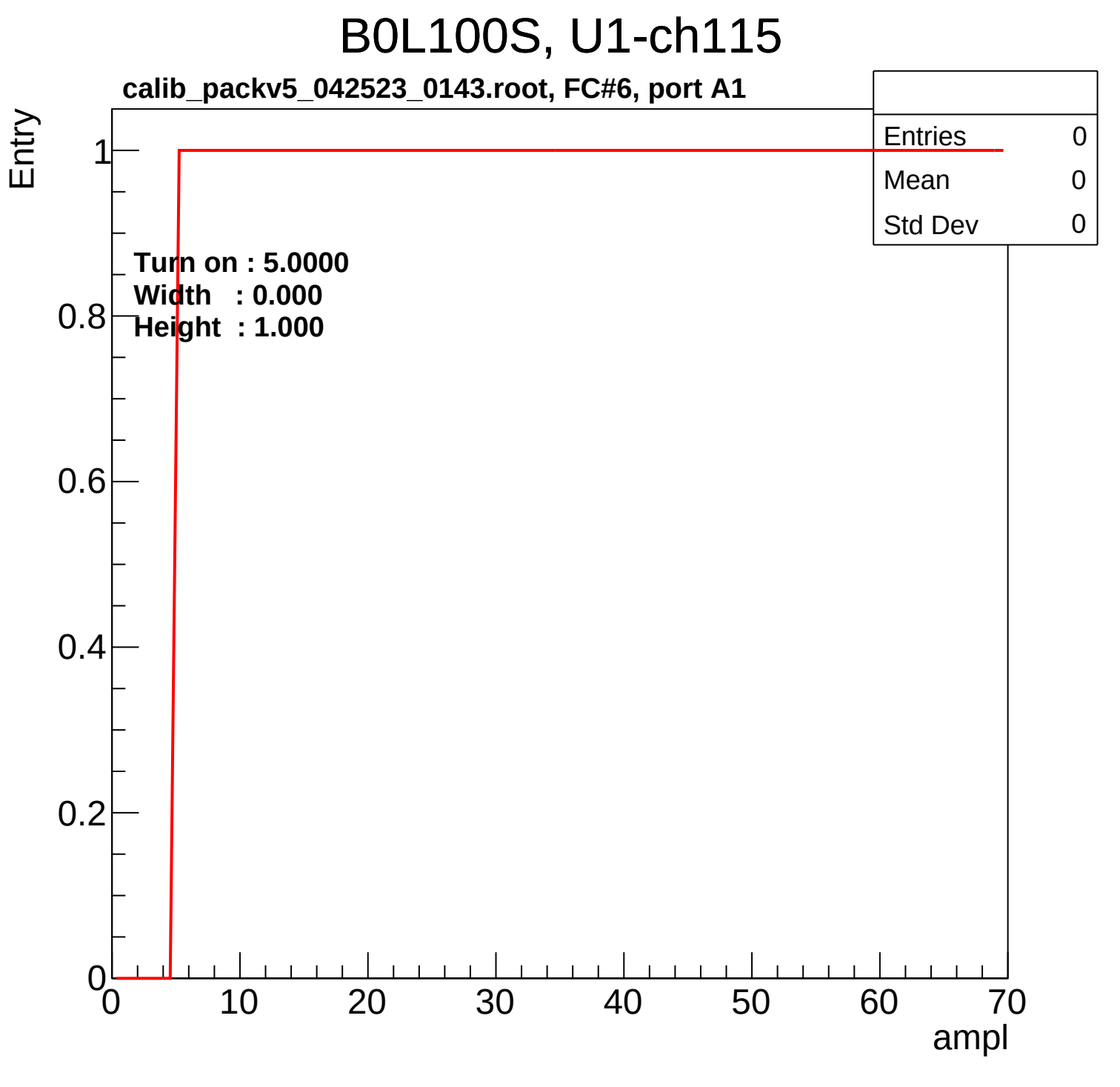
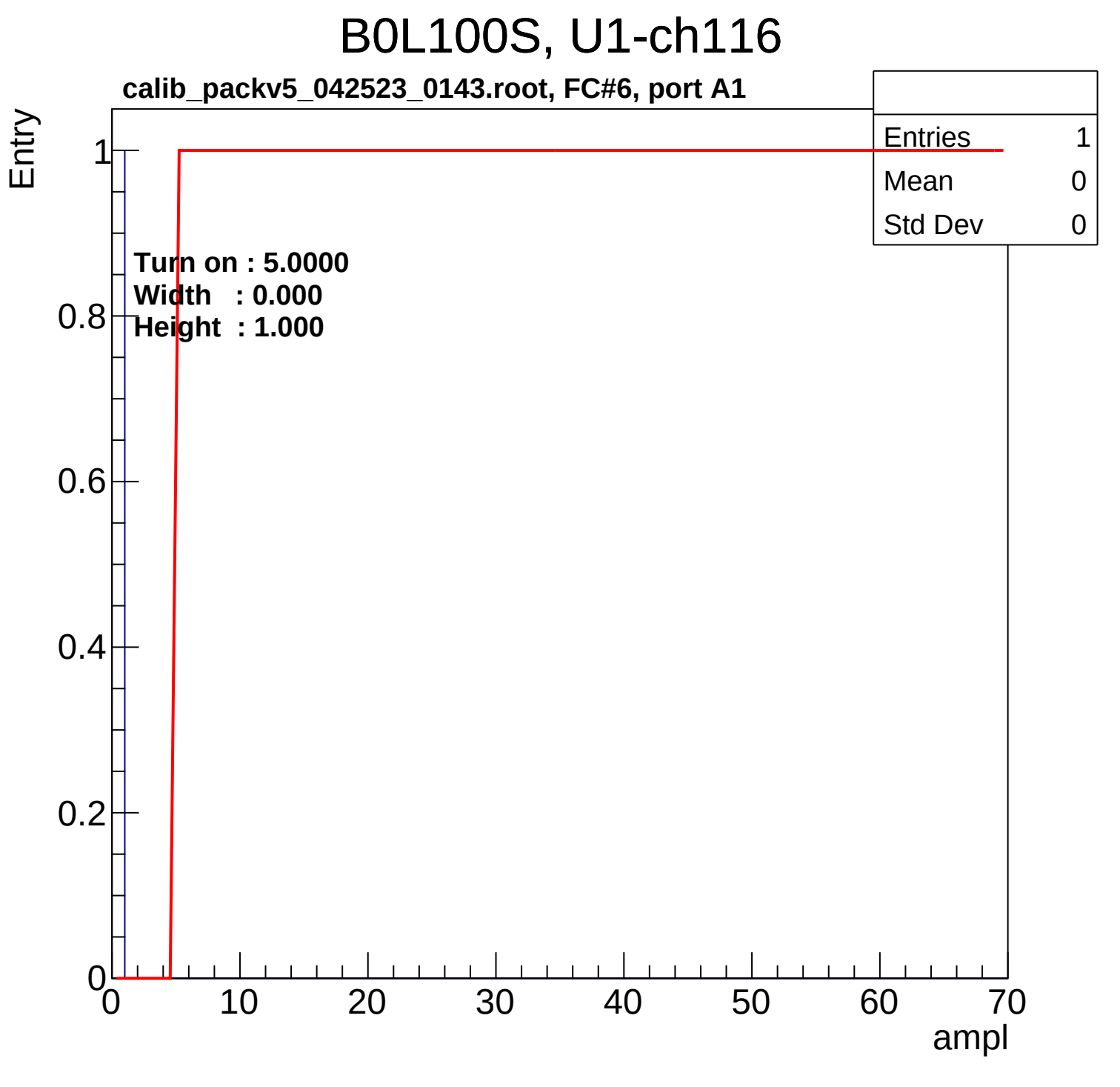
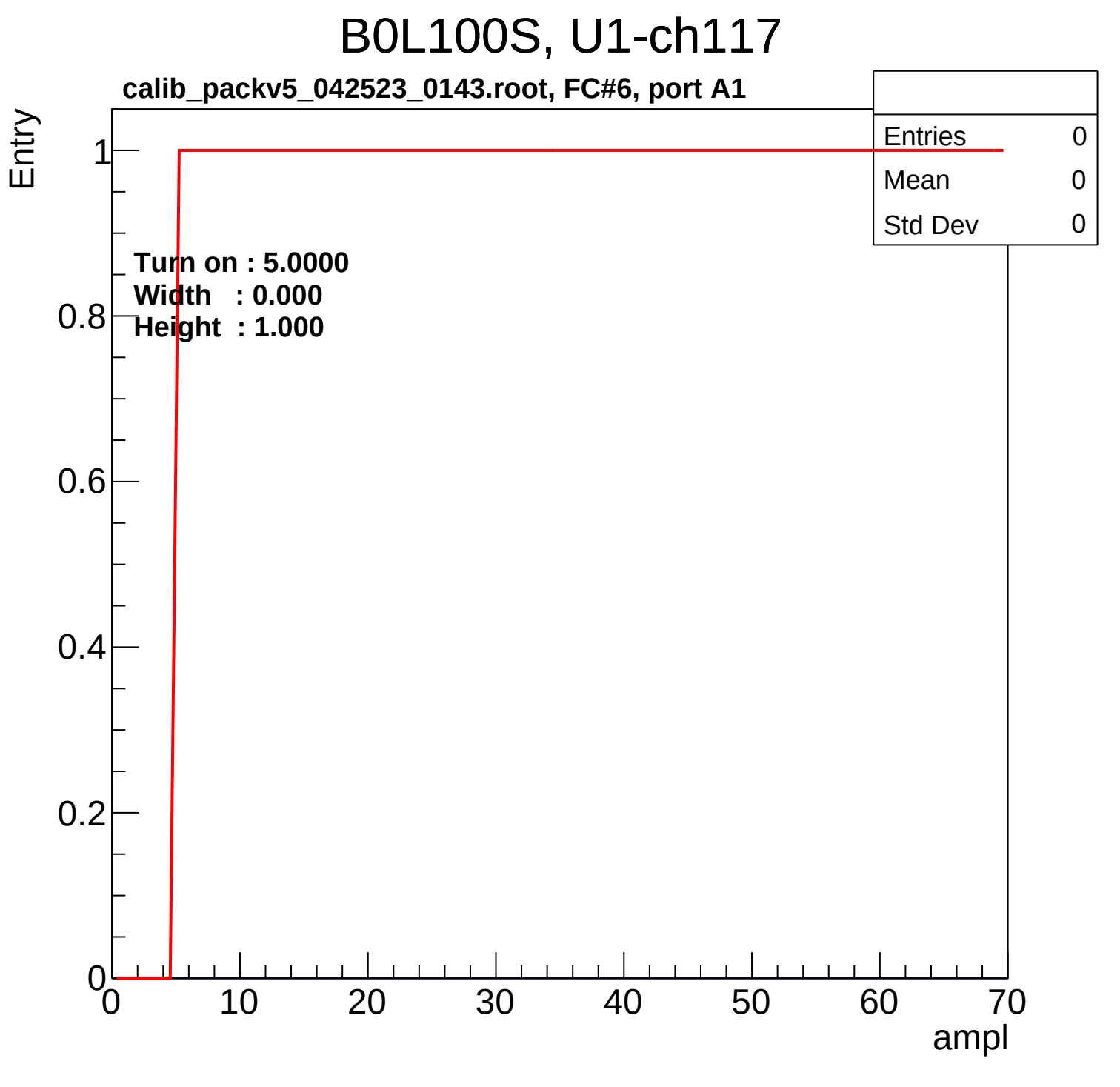
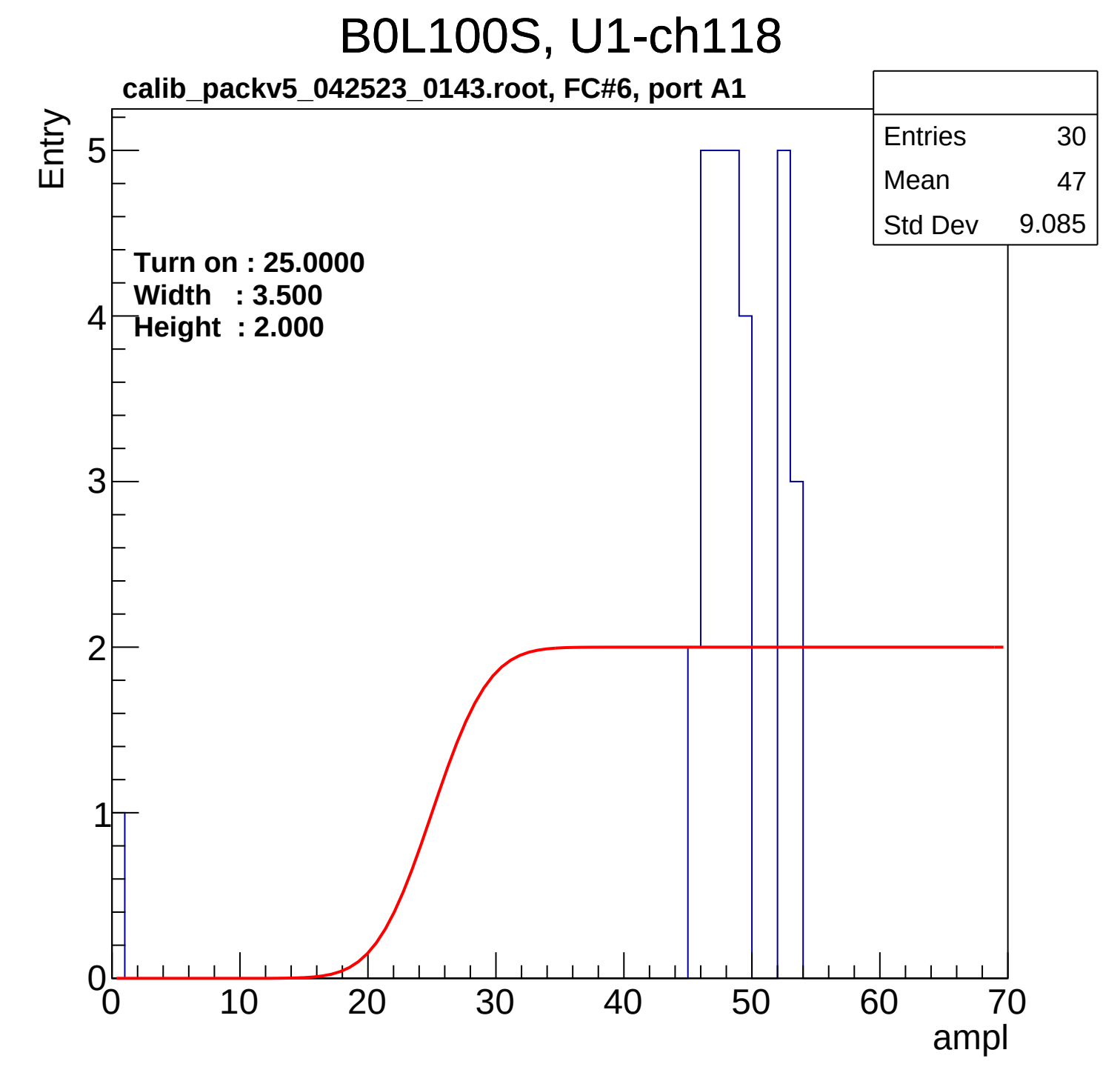
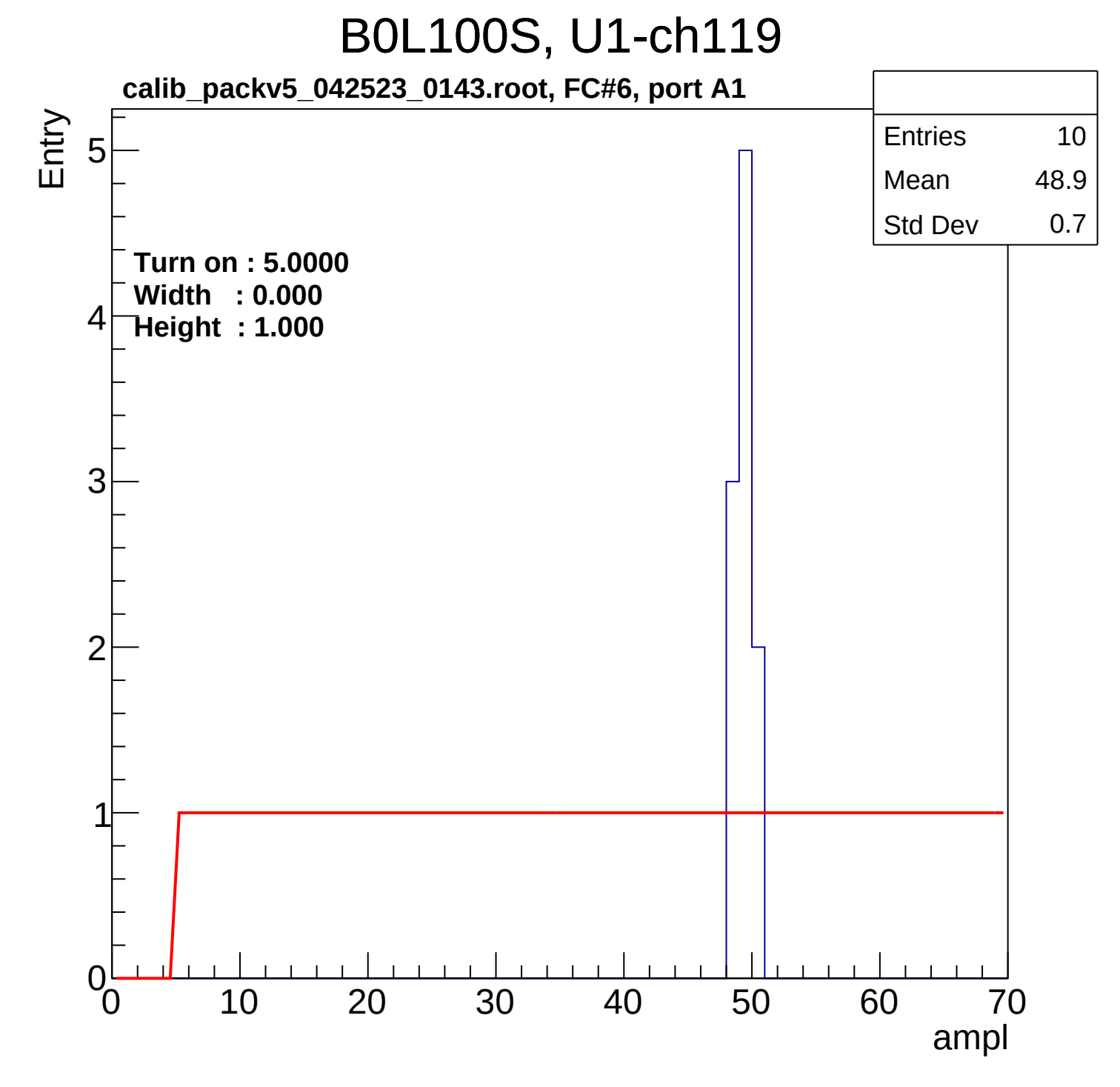
ampl

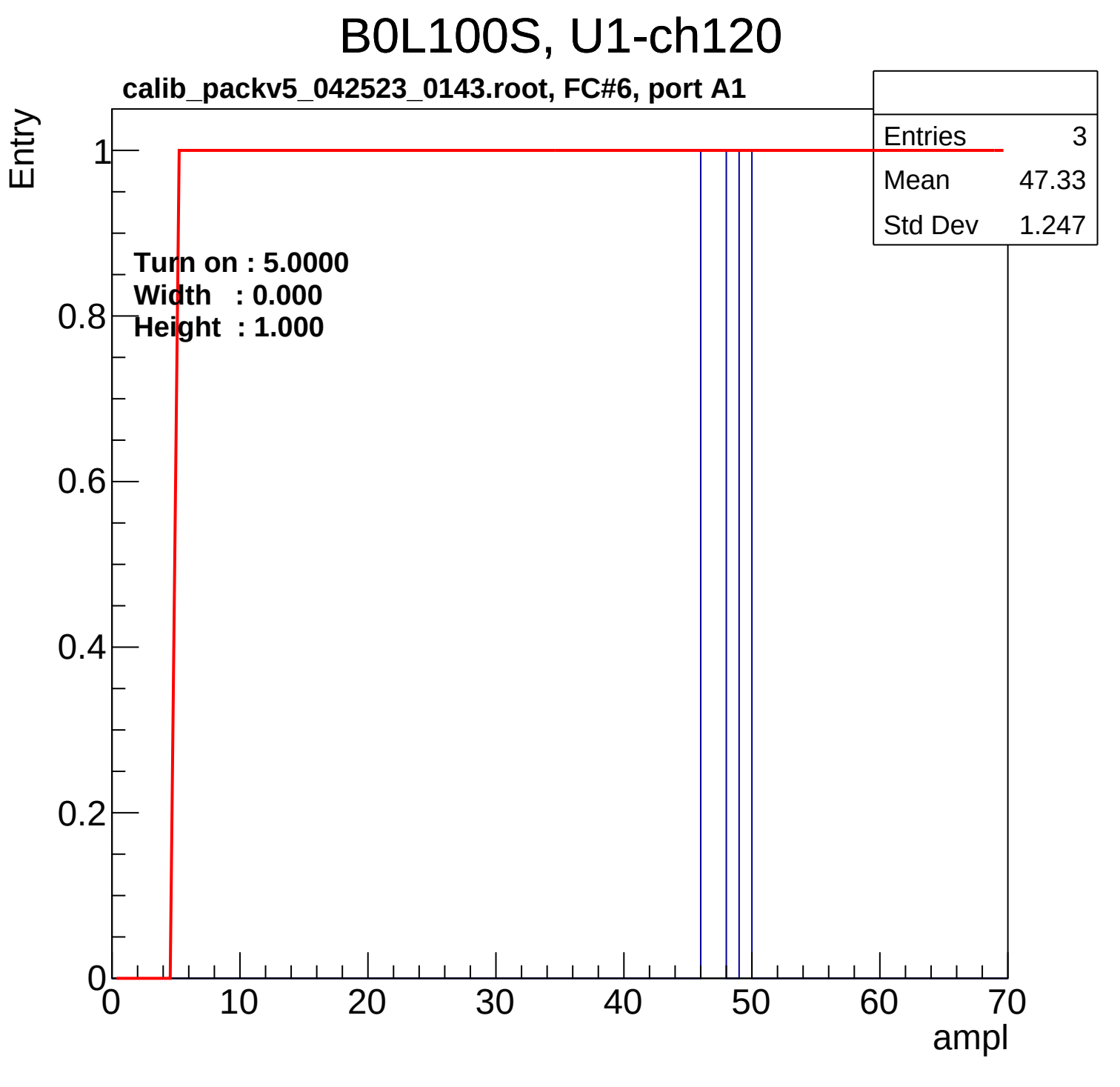

B0L100S, U1-ch115
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

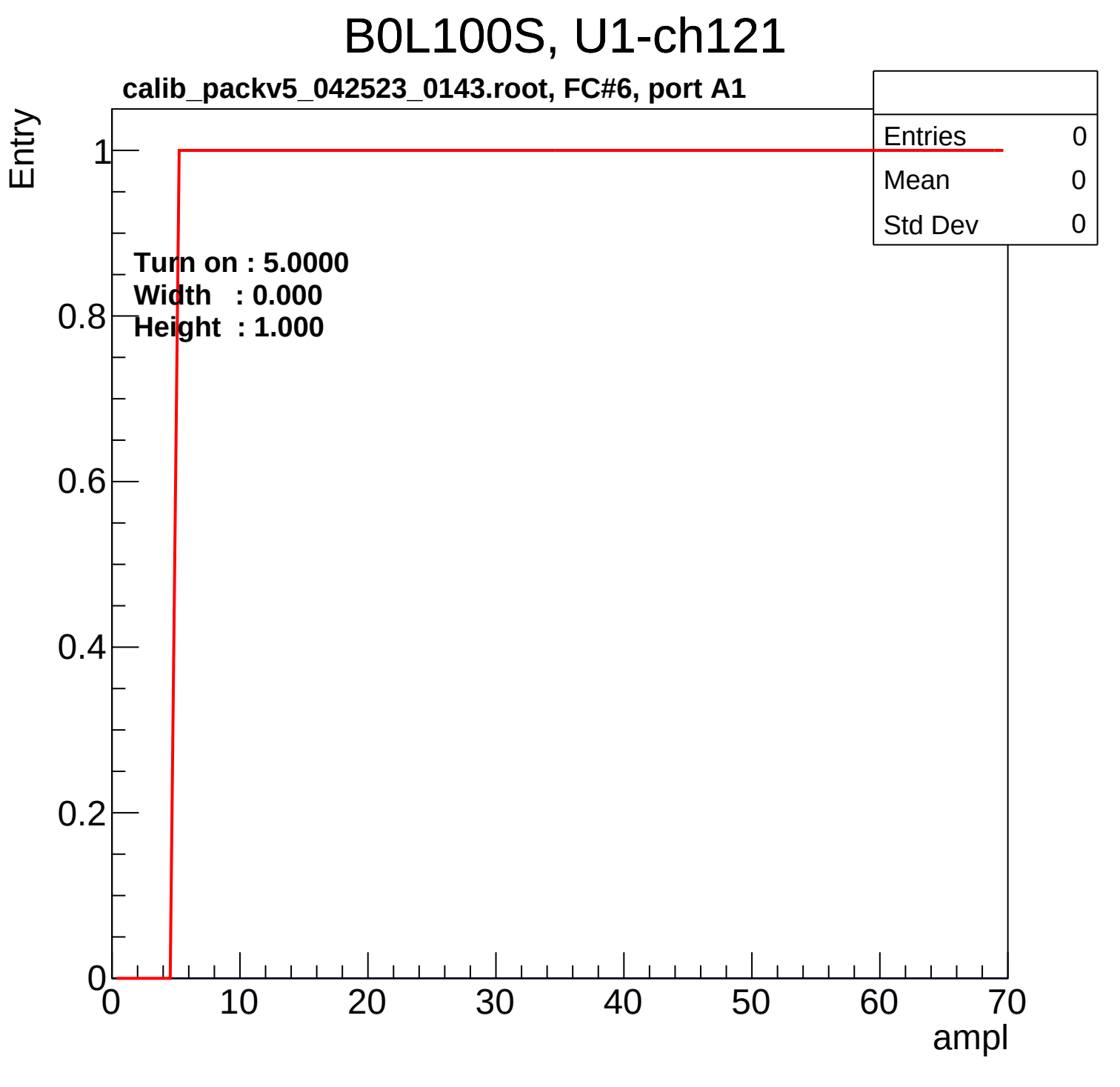

B0L100S, U1-ch116
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

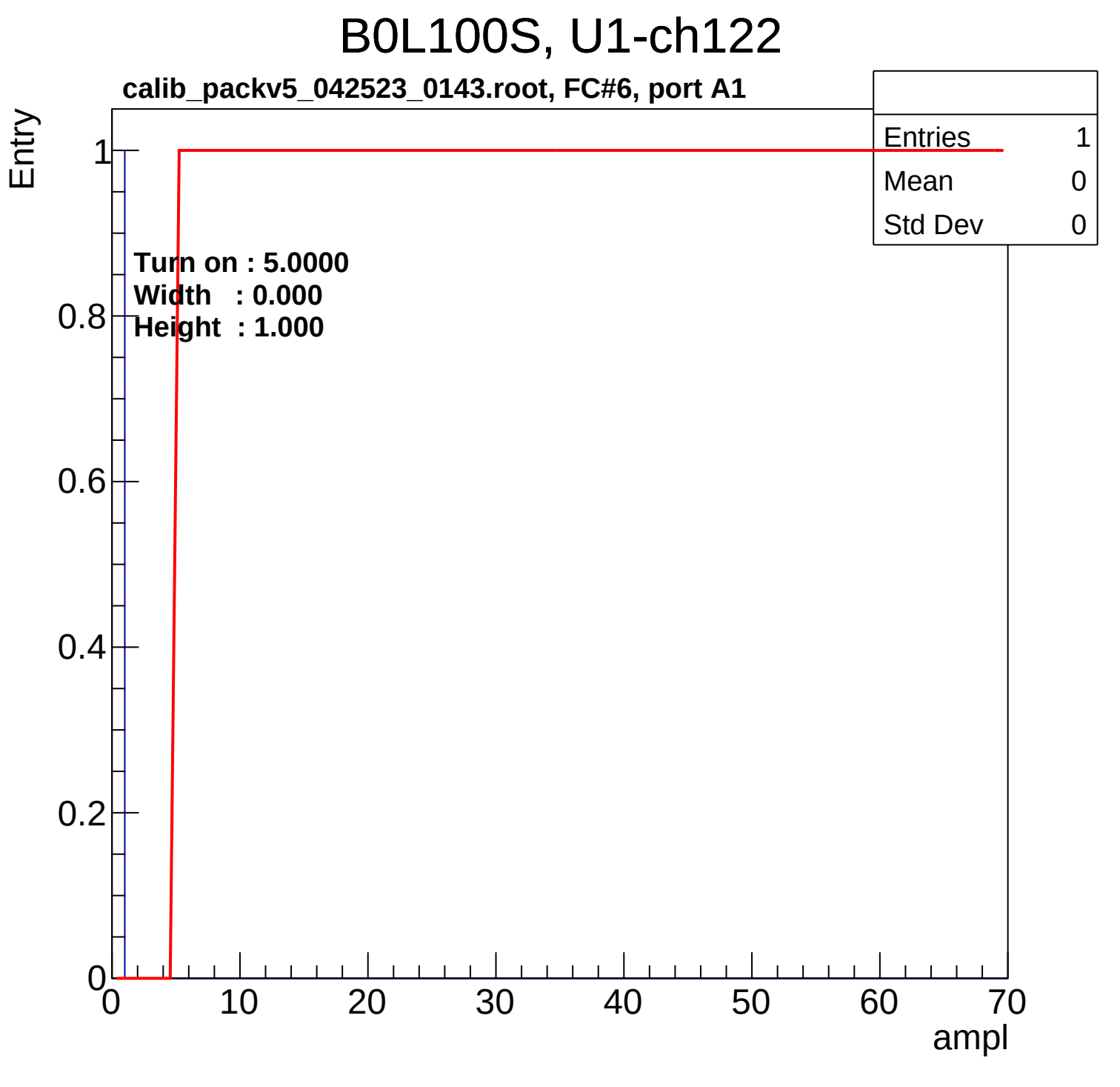

B0L100S, U1-ch117
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

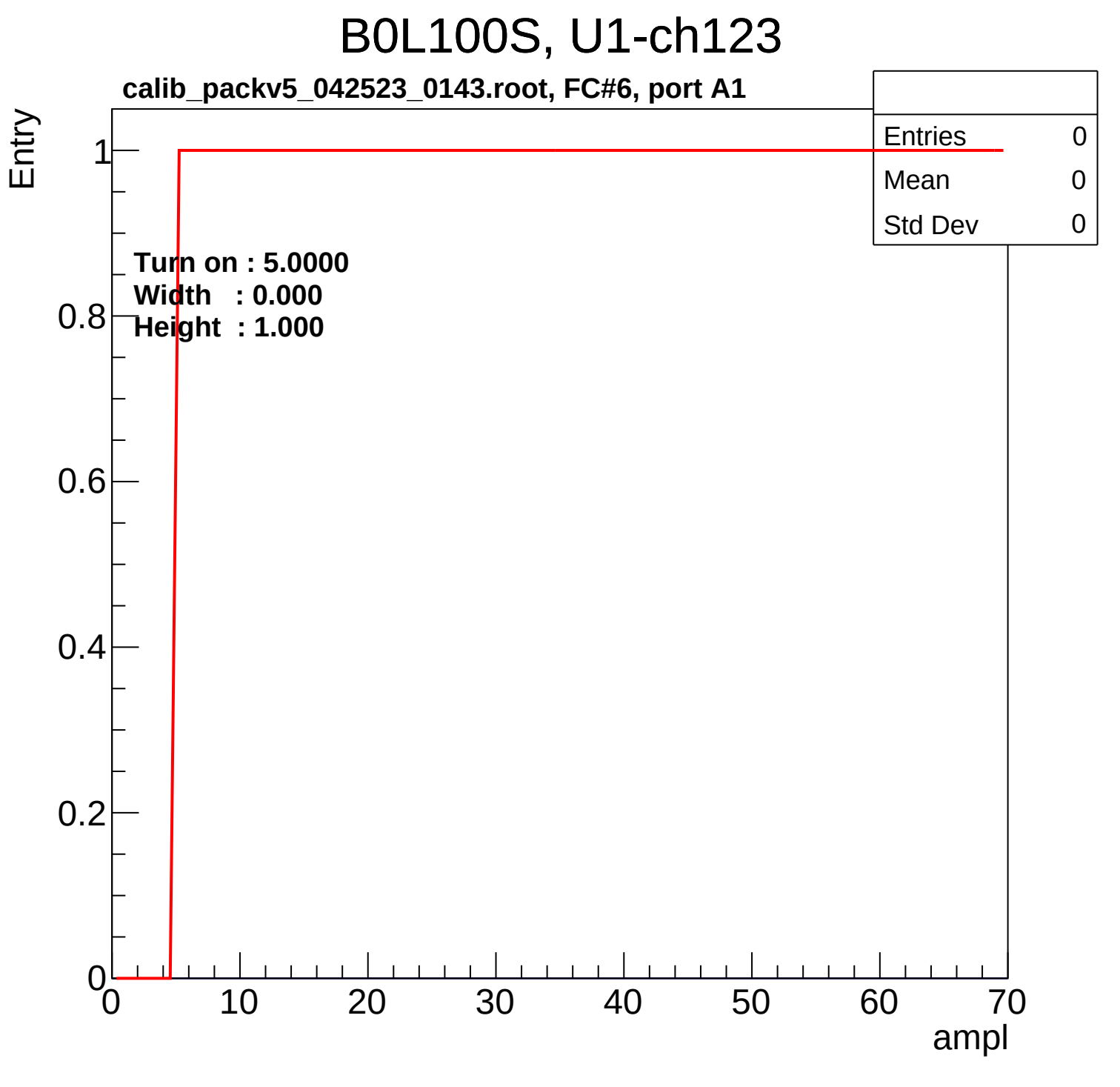

B0L100S, U1-ch118
calib_packv5_042523_0143.root, FC#6, port A1
Entries 30
Mean 47
Std Dev 9.085
Turn on : 25.0000
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

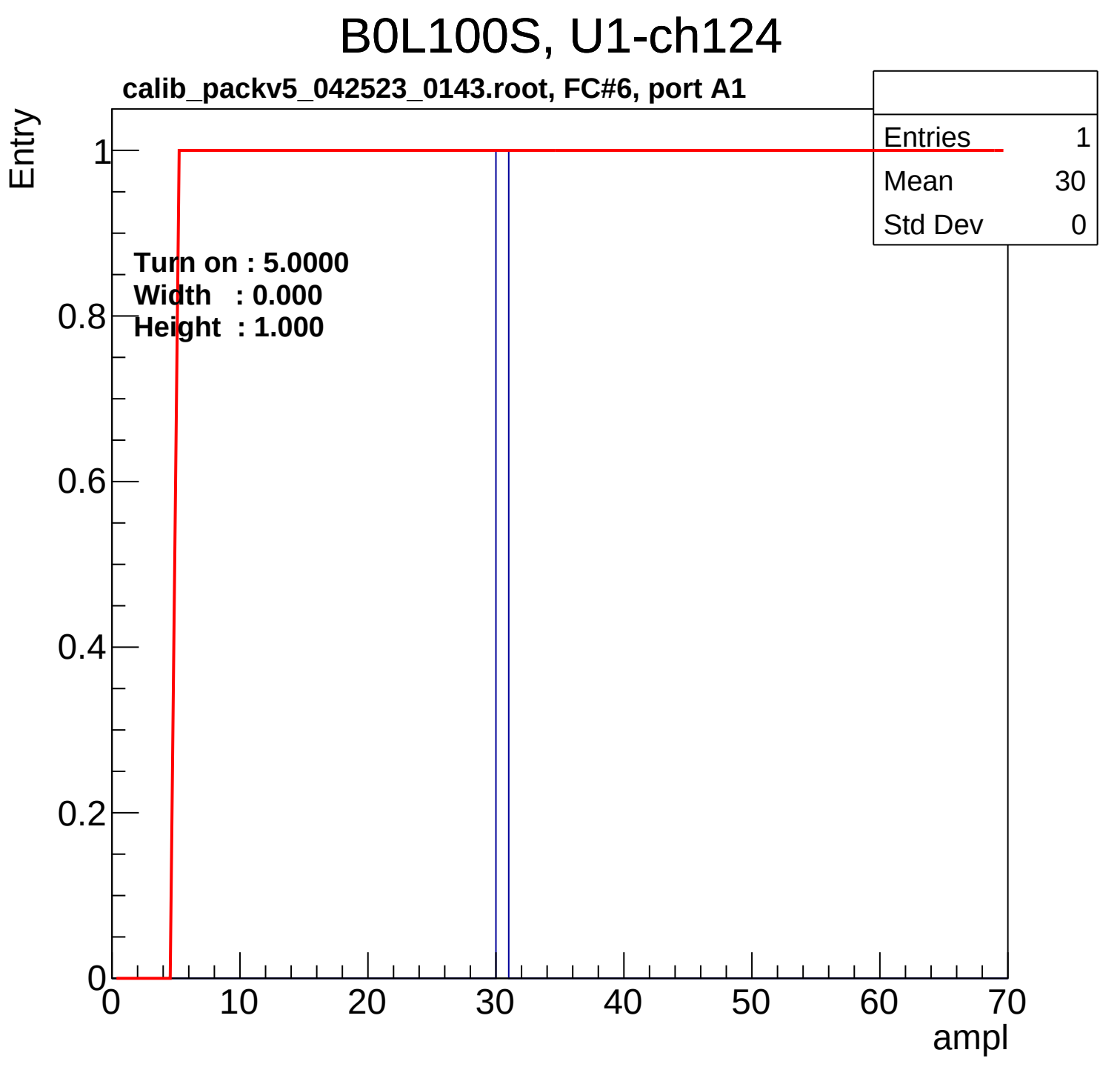

B0L100S, U1-ch119
calib_packv5_042523_0143.root, FC#6, port A1
Entries 10
Mean 48.9
Std Dev 0.7
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

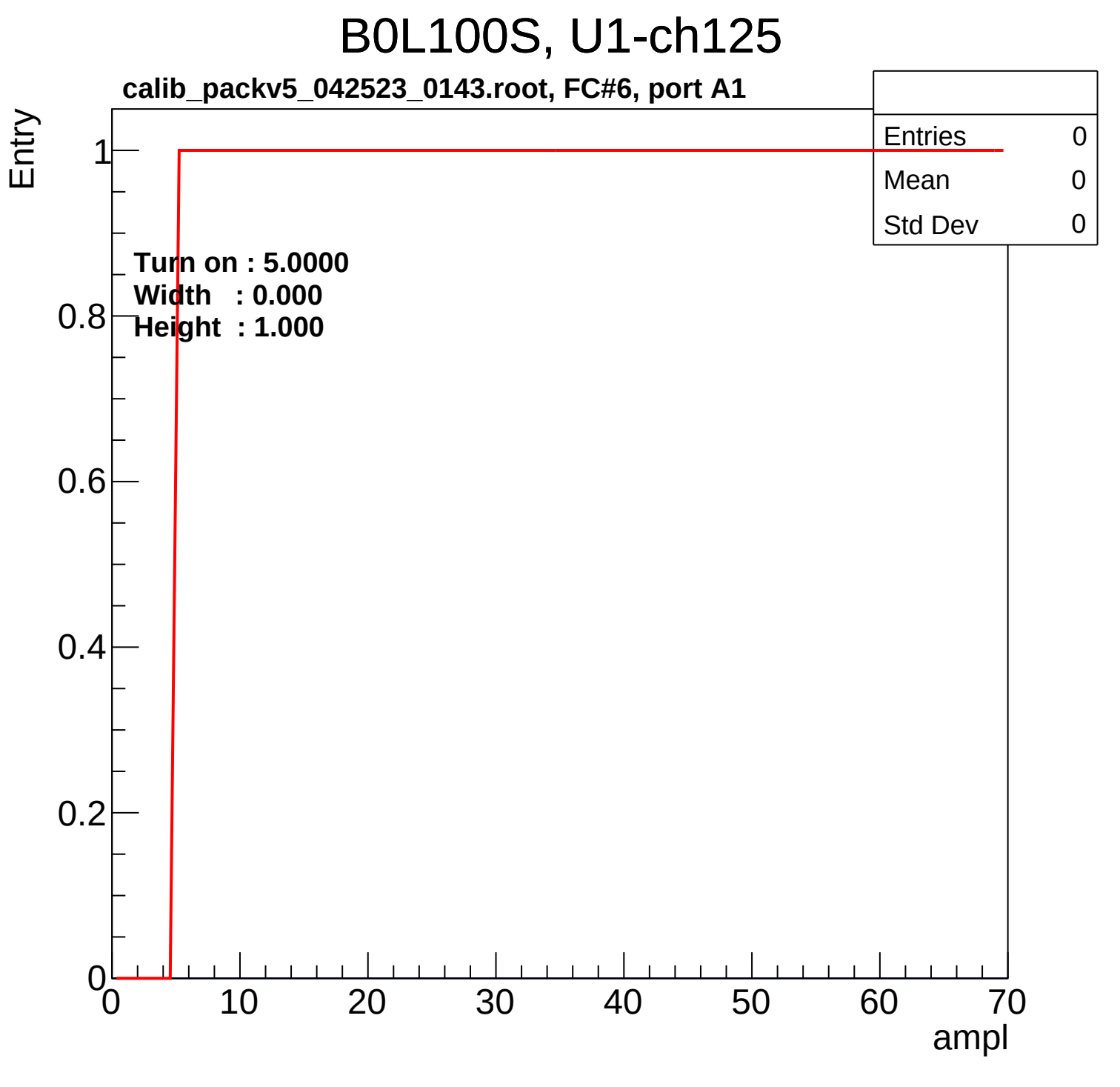

B0L100S, U1-ch120
calib_packv5_042523_0143.root, FC#6, port A1
Entries 3
Mean 47.33
Std Dev 1.247
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

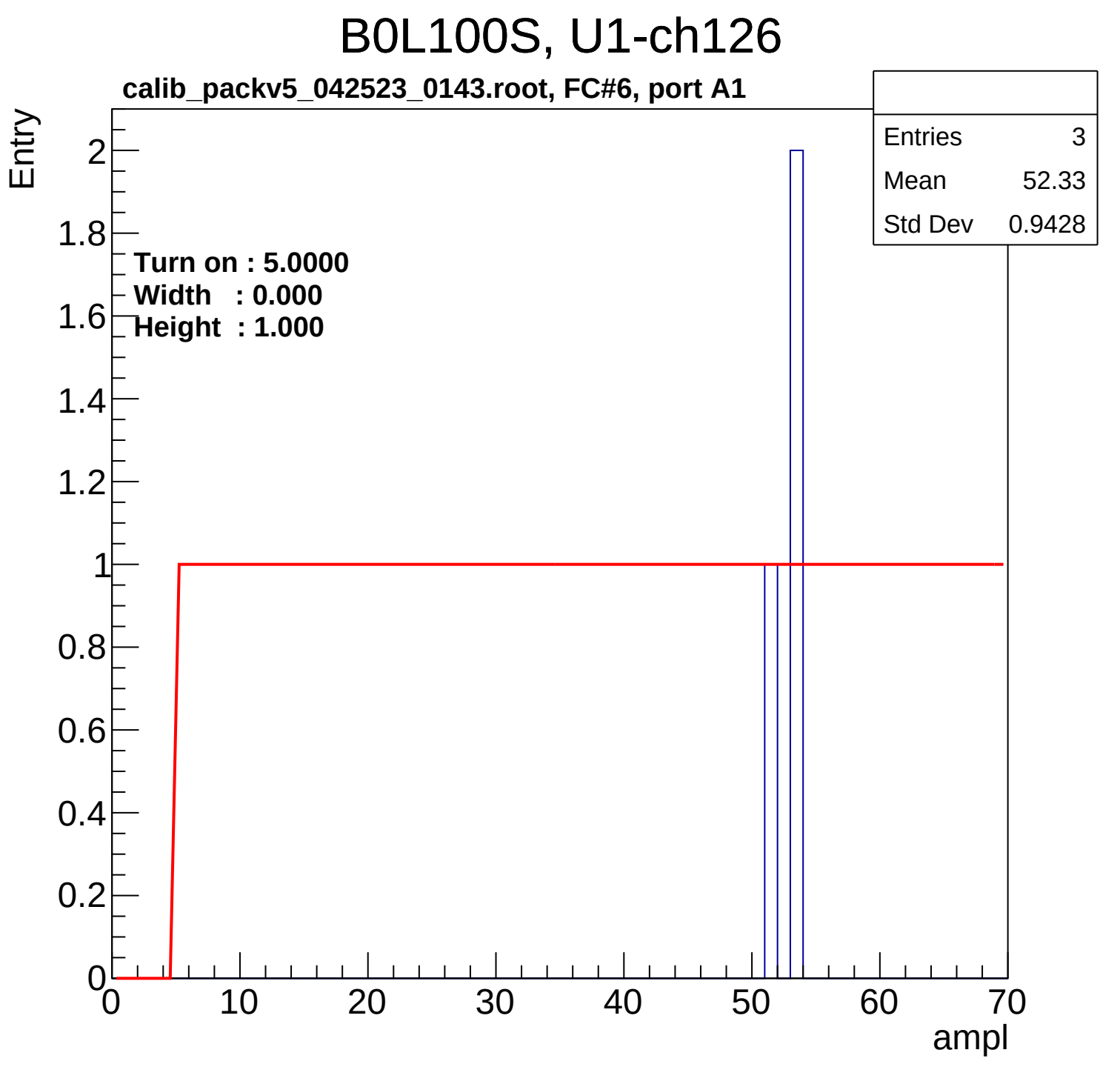

B0L100S, U1-ch121
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

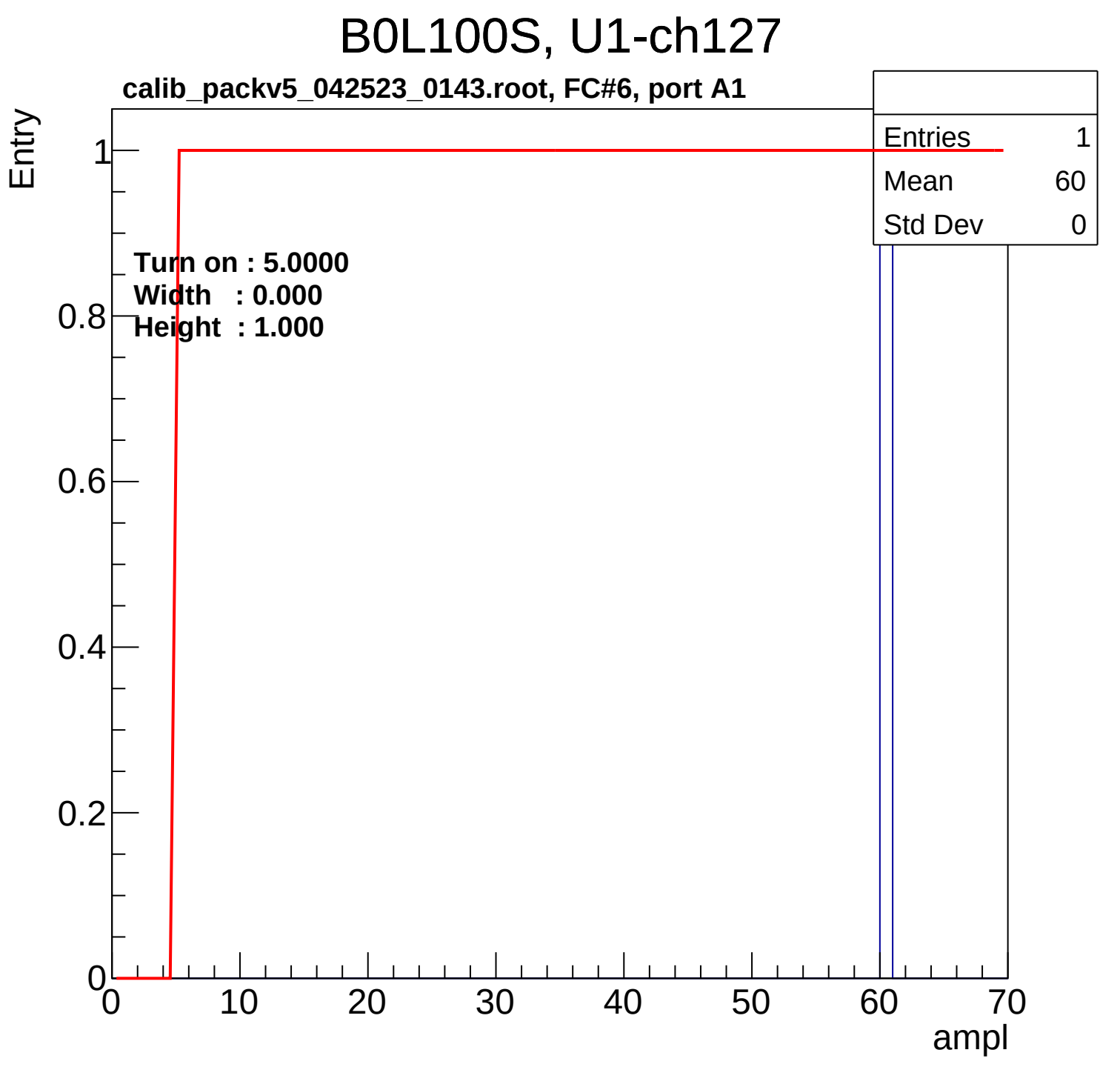

B0L100S, U1-ch122
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

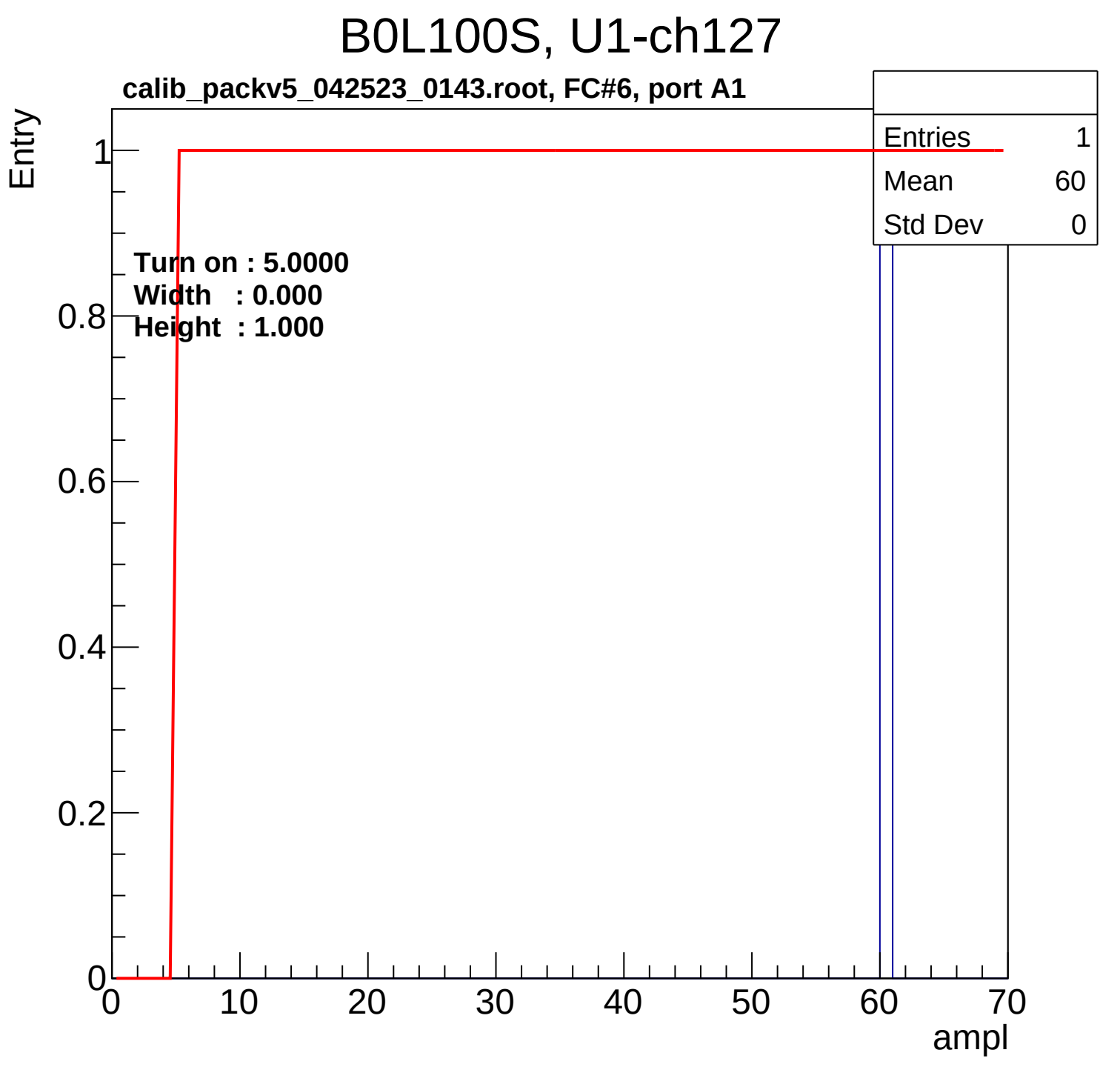

B0L100S, U1-ch123
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U1-ch124
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 30
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B0L100S, U1-ch125
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B0L100S, U1-ch126
calib_packv5_042523_0143.root, FC#6, port A1
Entries 3
Mean 52.33
Std Dev 0.9428
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B0L100S, U1-ch127
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 60
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B0L100S, U1-ch127
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 60
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70