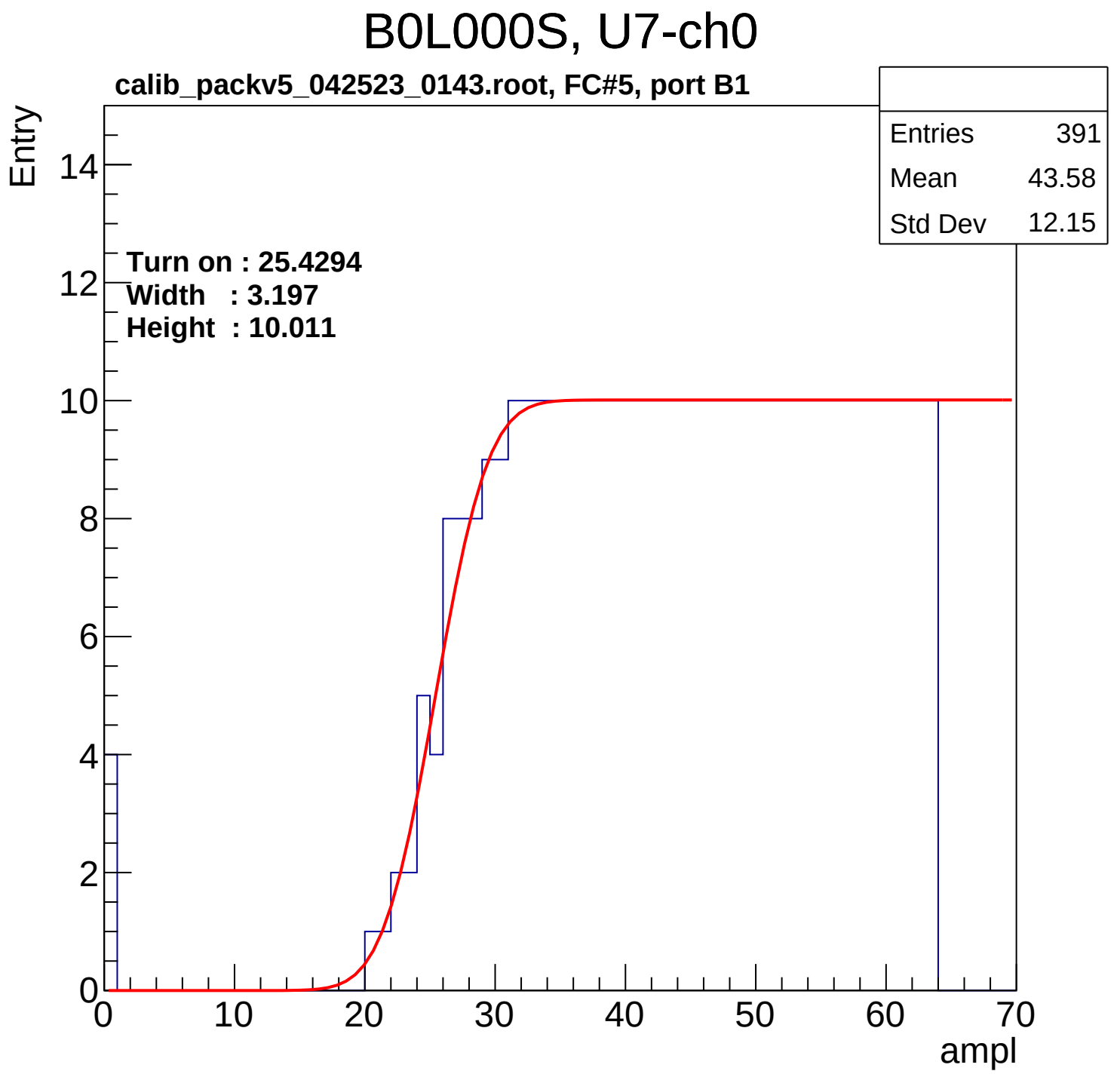
B0L000S, U7-ch0
calib_packv5_042523_0143.root, FC#5, port B1
Entries 391
Mean 43.58
Std Dev 12.15
Turn on : 25.4294
Width : 3.197
Height : 10.011
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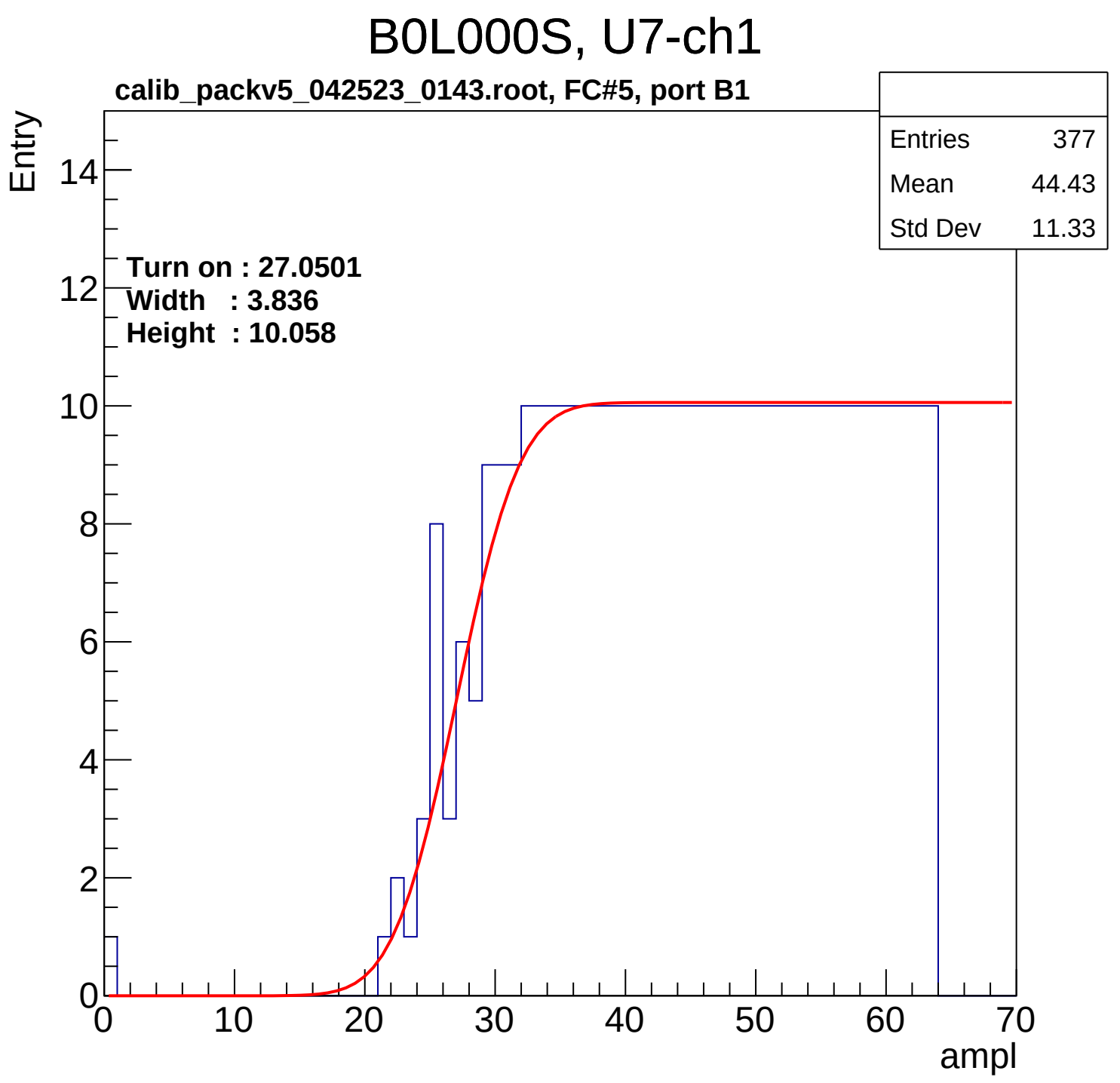
B0L000S, U7-ch1
calib_packv5_042523_0143.root, FC#5, port B1
Entries 377
Mean 44.43
Std Dev 11.33
Turn on : 27.0501
Width : 3.836
Height : 10.058
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ampl
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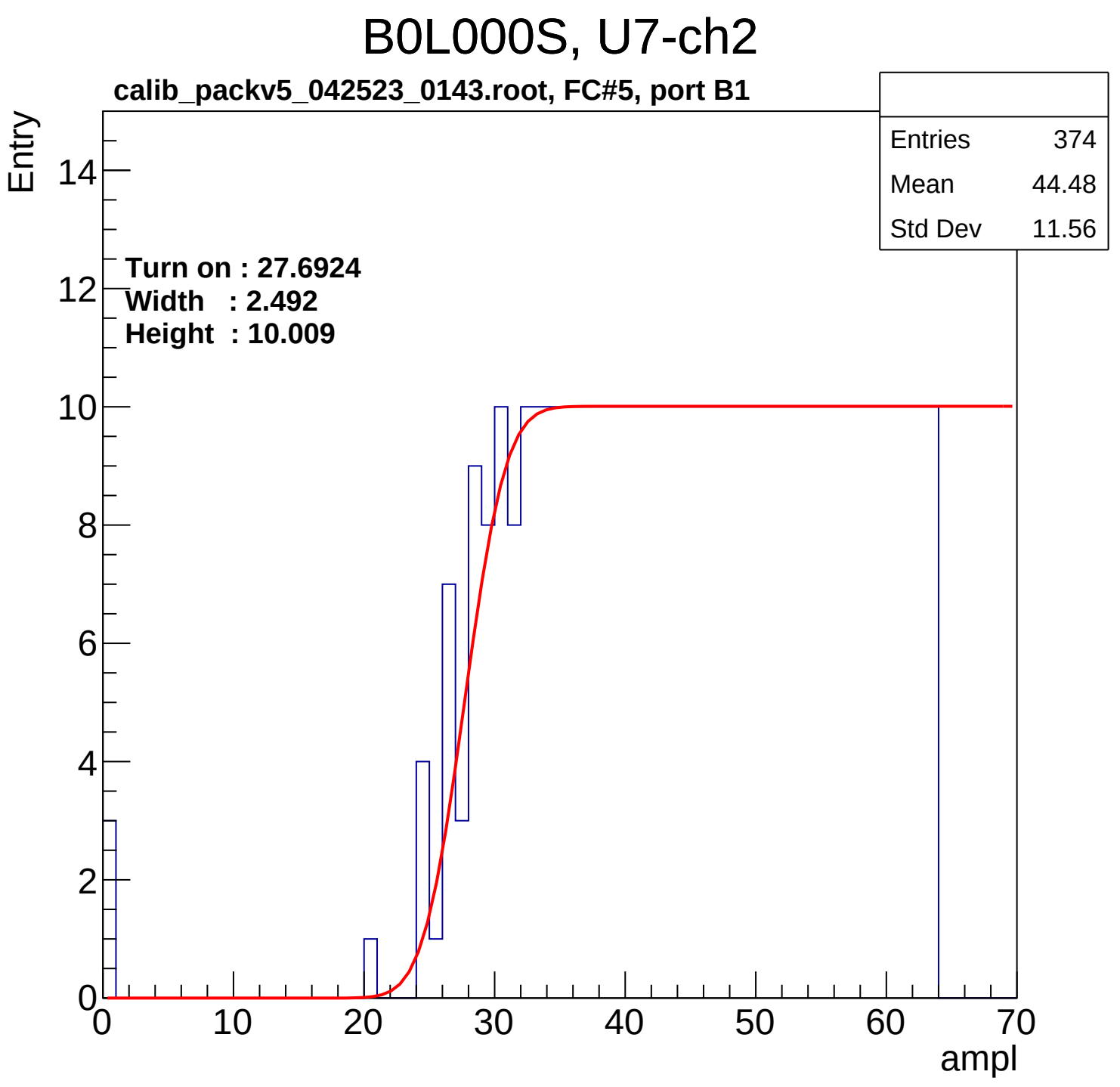
B0L000S, U7-ch2
calib_packv5_042523_0143.root, FC#5, port B1
Entries 374
Mean 44.48
Std Dev 11.56
Turn on : 27.6924
Width : 2.492
Height : 10.009
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ampl
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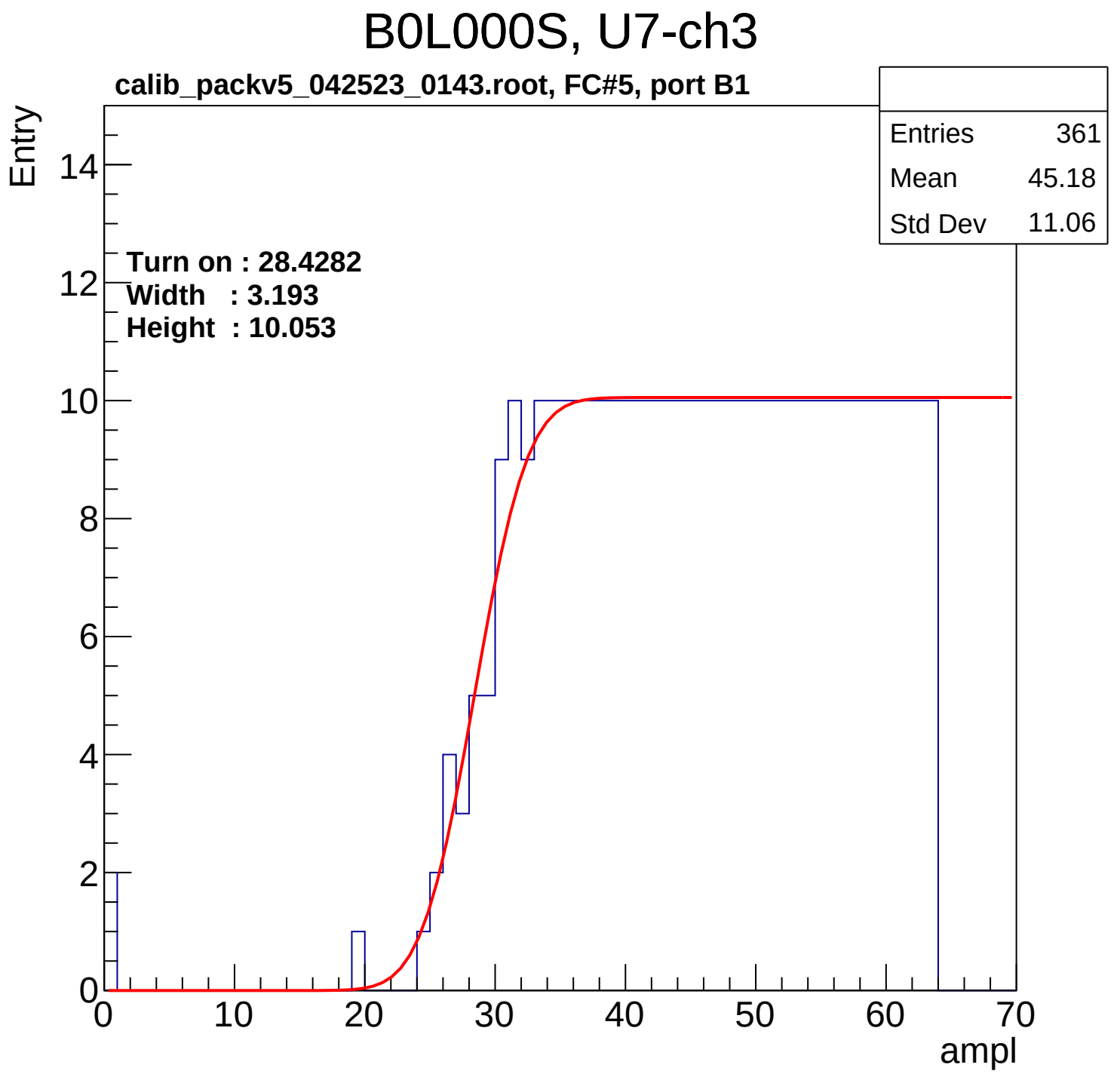
B0L000S, U7-ch3
calib_packv5_042523_0143.root, FC#5, port B1
Entries 361
Mean 45.18
Std Dev 11.06
Turn on : 28.4282
Width : 3.193
Height : 10.053
Entry
ampl
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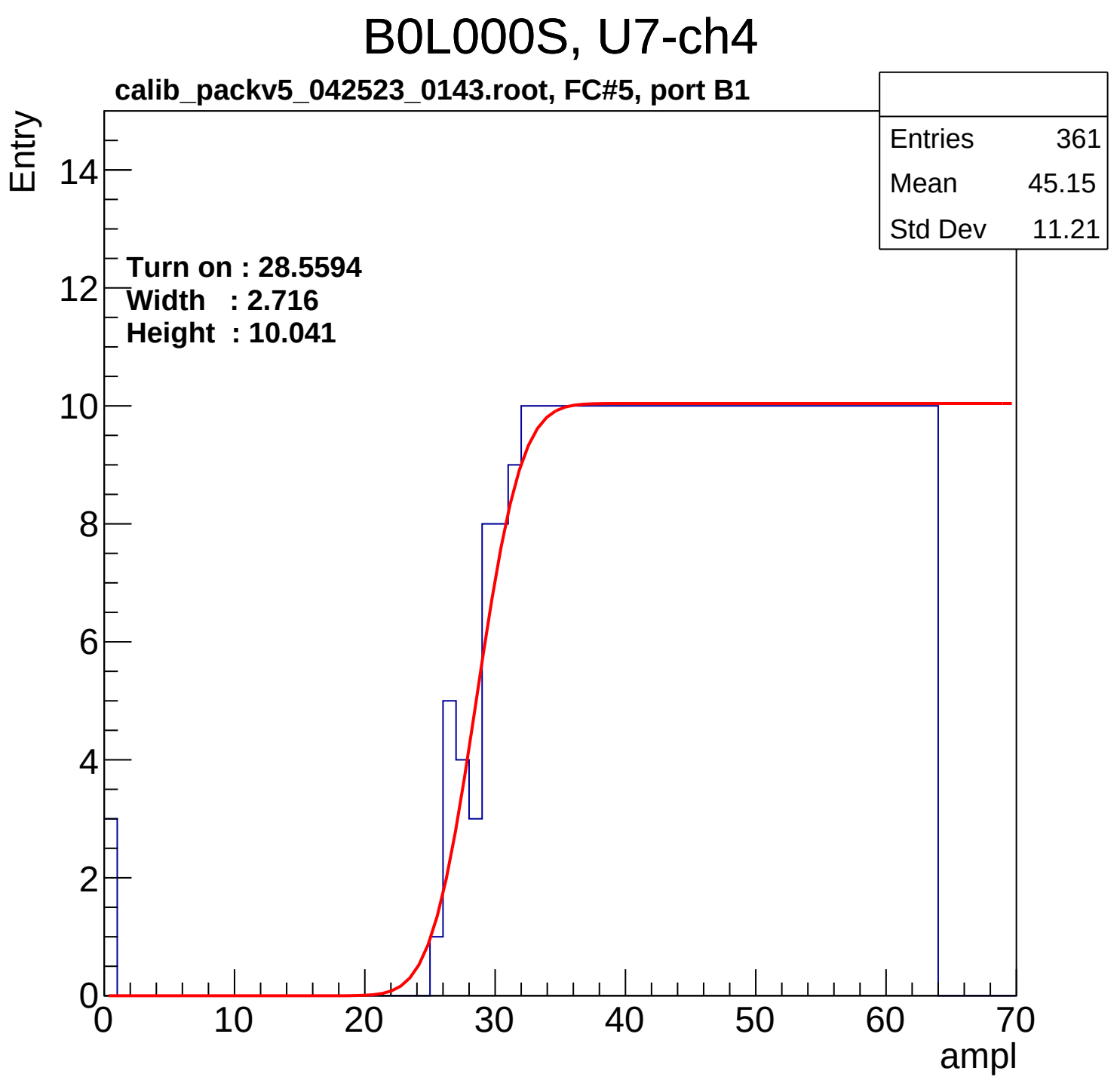
B0L000S, U7-ch4
calib_packv5_042523_0143.root, FC#5, port B1
Entries 361
Mean 45.15
Std Dev 11.21
Turn on : 28.5594
Width : 2.716
Height : 10.041
Entry
ampl
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6
8
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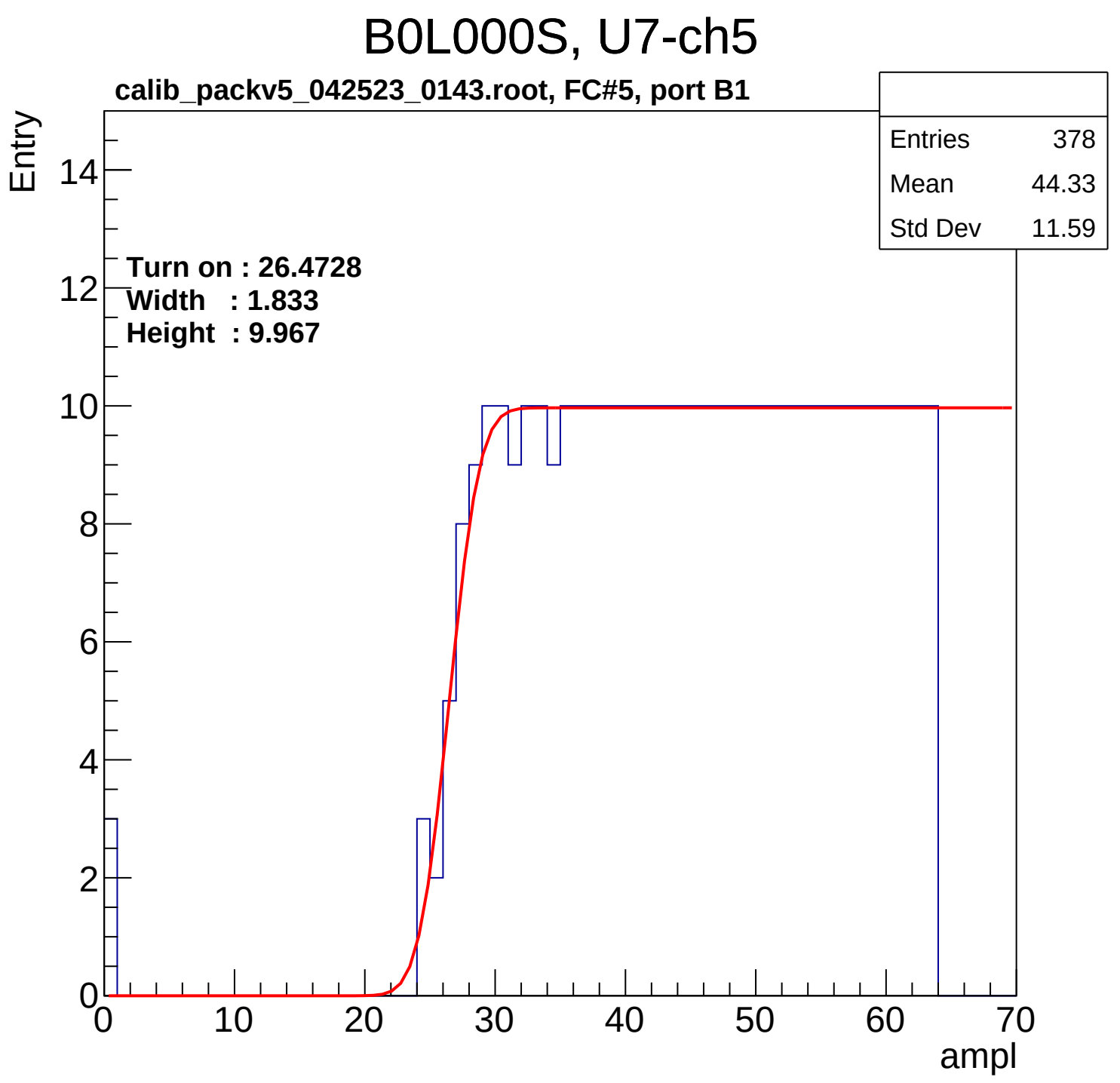
B0L000S, U7-ch5
calib_packv5_042523_0143.root, FC#5, port B1
Entries 378
Mean 44.33
Std Dev 11.59
Turn on : 26.4728
Width : 1.833
Height : 9.967
Entry
ampl
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2
4
6
8
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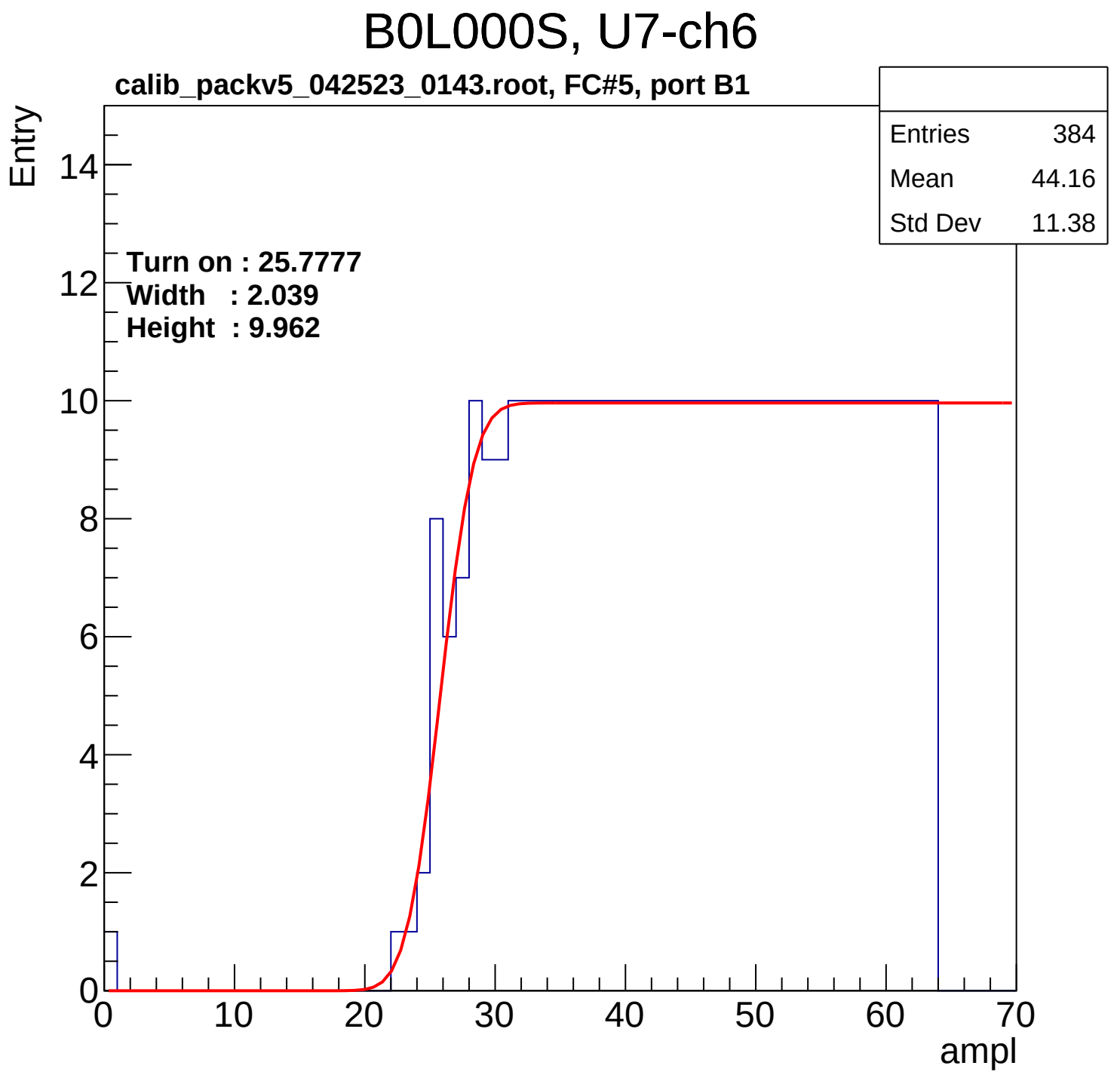
B0L000S, U7-ch6
calib_packv5_042523_0143.root, FC#5, port B1
Entries 384
Mean 44.16
Std Dev 11.38
Turn on : 25.7777
Width : 2.039
Height : 9.962
Entry
ampl
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2
4
6
8
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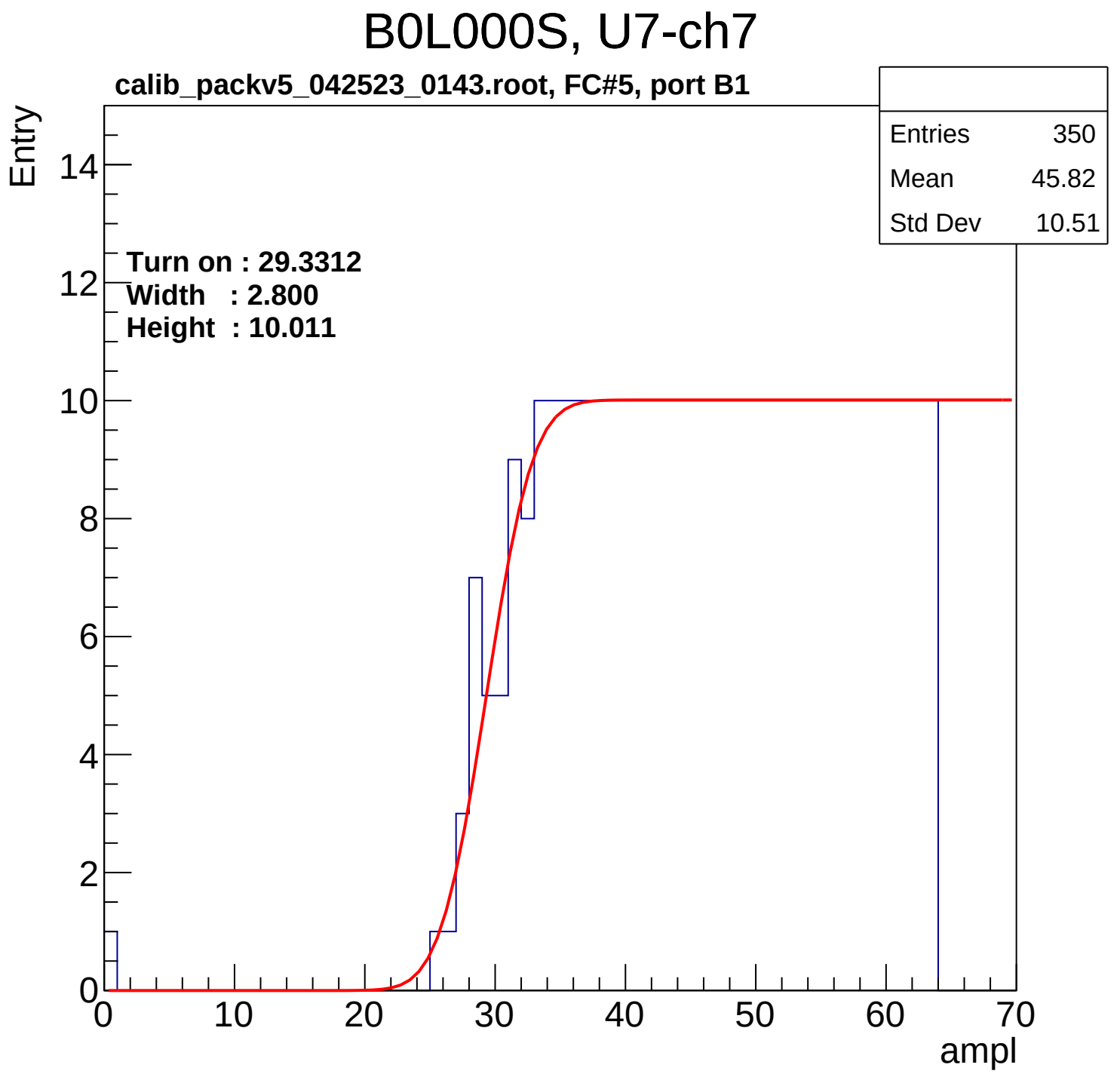
B0L000S, U7-ch7
calib_packv5_042523_0143.root, FC#5, port B1
Entries 350
Mean 45.82
Std Dev 10.51
Turn on : 29.3312
Width : 2.800
Height : 10.011
Entry
ampl
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2
4
6
8
10
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0
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60
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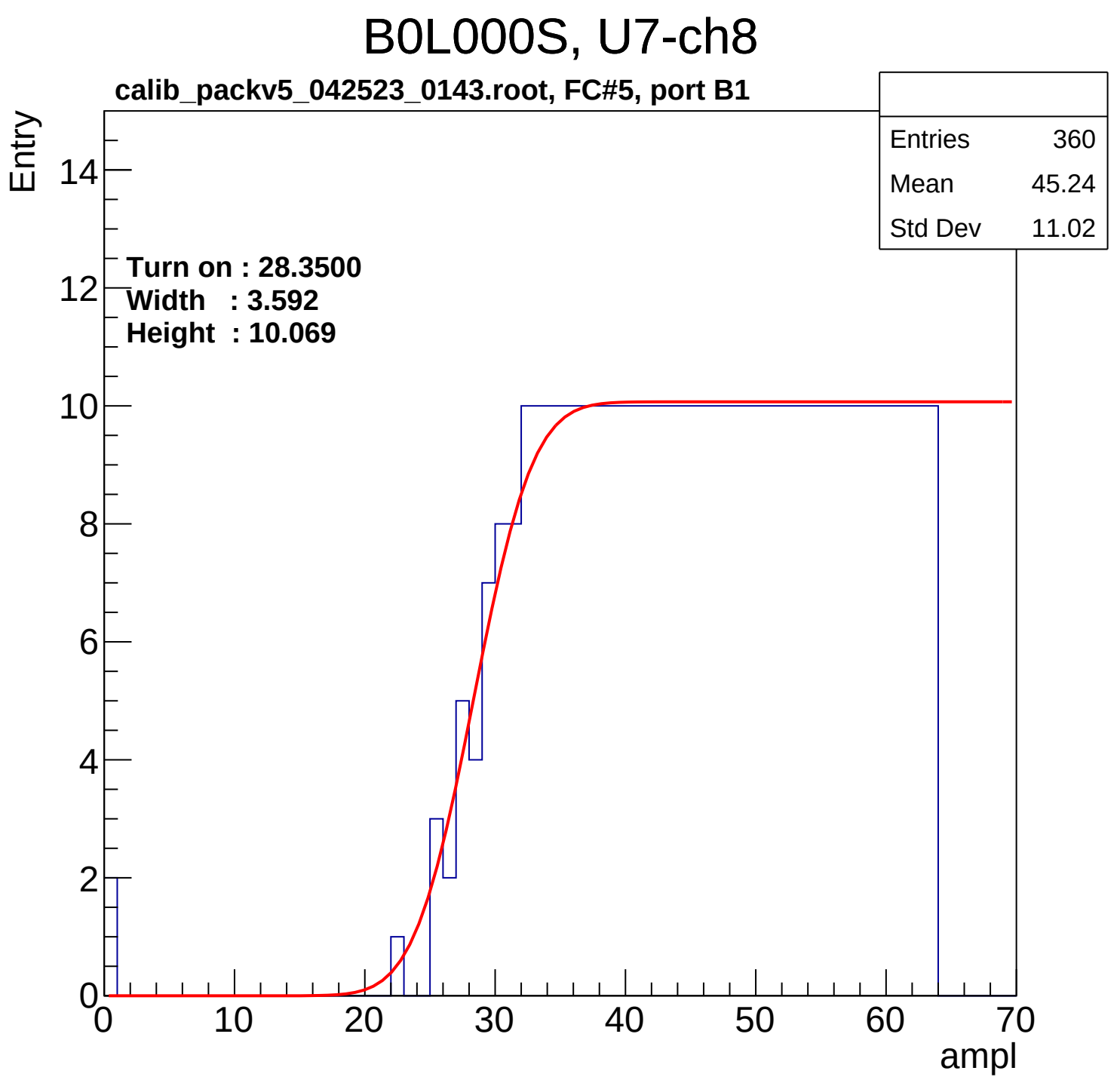
B0L000S, U7-ch8
calib_packv5_042523_0143.root, FC#5, port B1
Entries 360
Mean 45.24
Std Dev 11.02
Turn on : 28.3500
Width : 3.592
Height : 10.069
Entry
ampl
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2
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6
8
10
12
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0
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60
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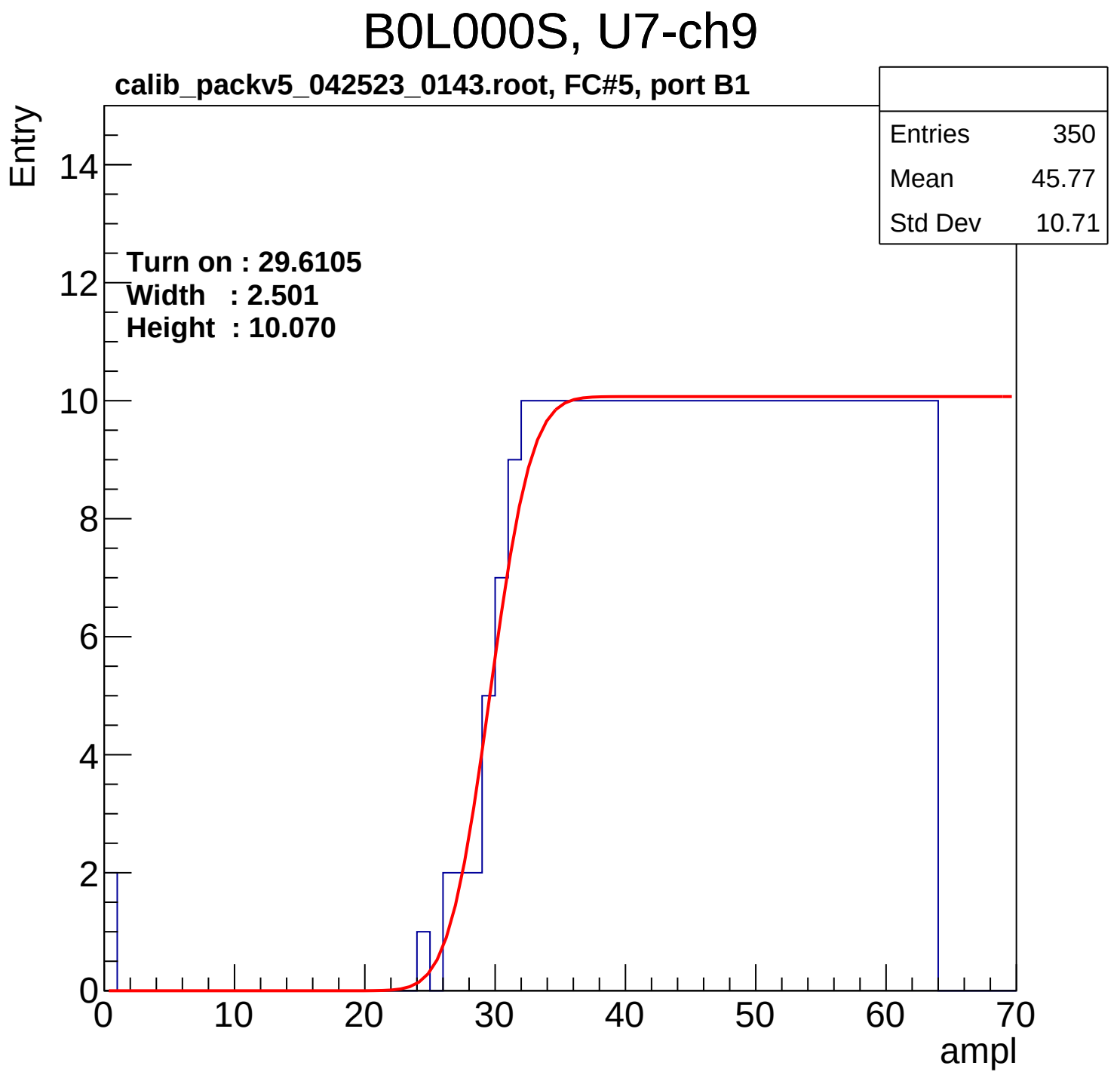
B0L000S, U7-ch9
calib_packv5_042523_0143.root, FC#5, port B1
Entries 350
Mean 45.77
Std Dev 10.71
Turn on : 29.6105
Width : 2.501
Height : 10.070
Entry
ampl
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6
8
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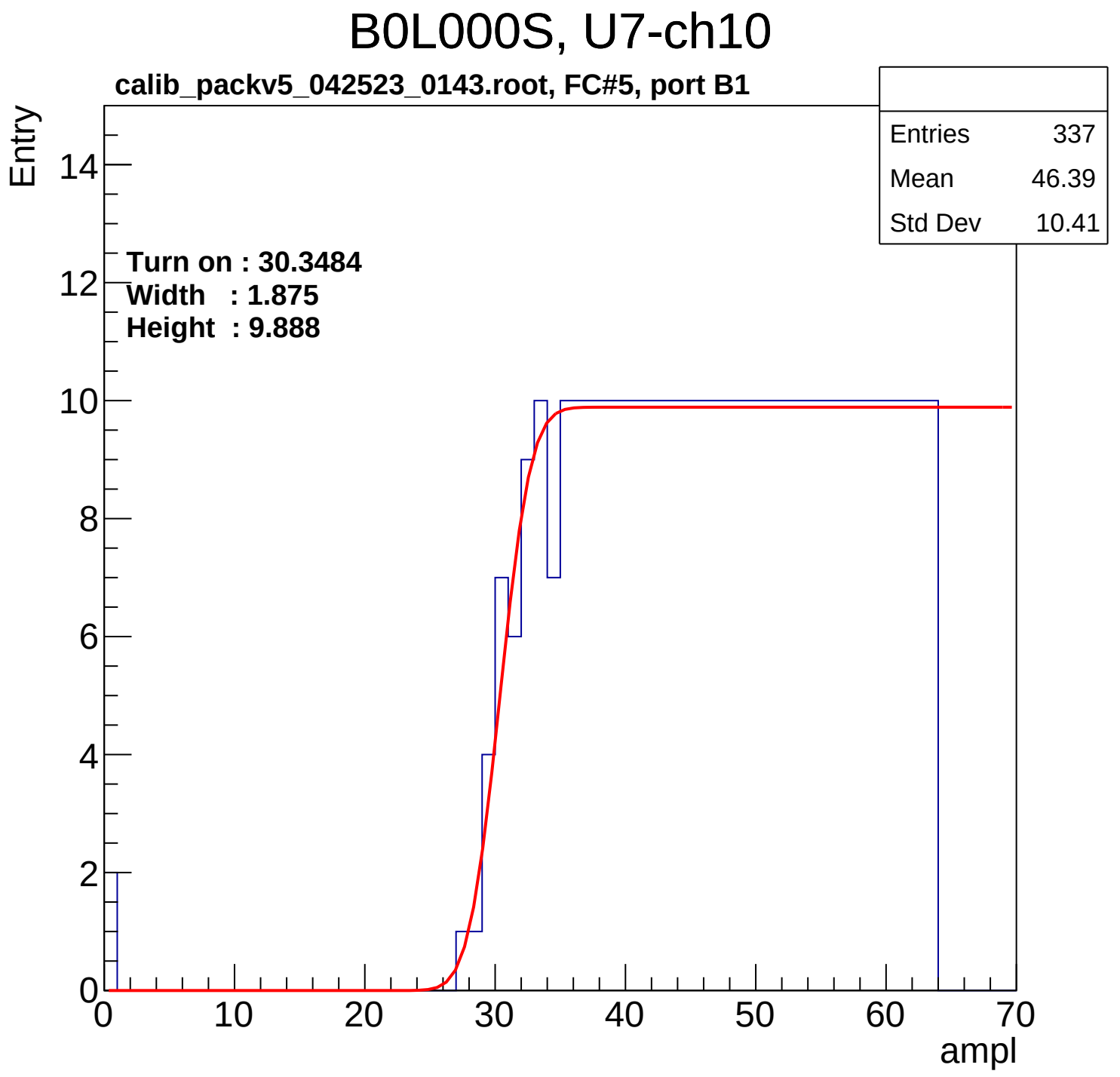
B0L000S, U7-ch10
calib_packv5_042523_0143.root, FC#5, port B1
Entries 337
Mean 46.39
Std Dev 10.41
Turn on : 30.3484
Width : 1.875
Height : 9.888
Entry
ampl
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6
8
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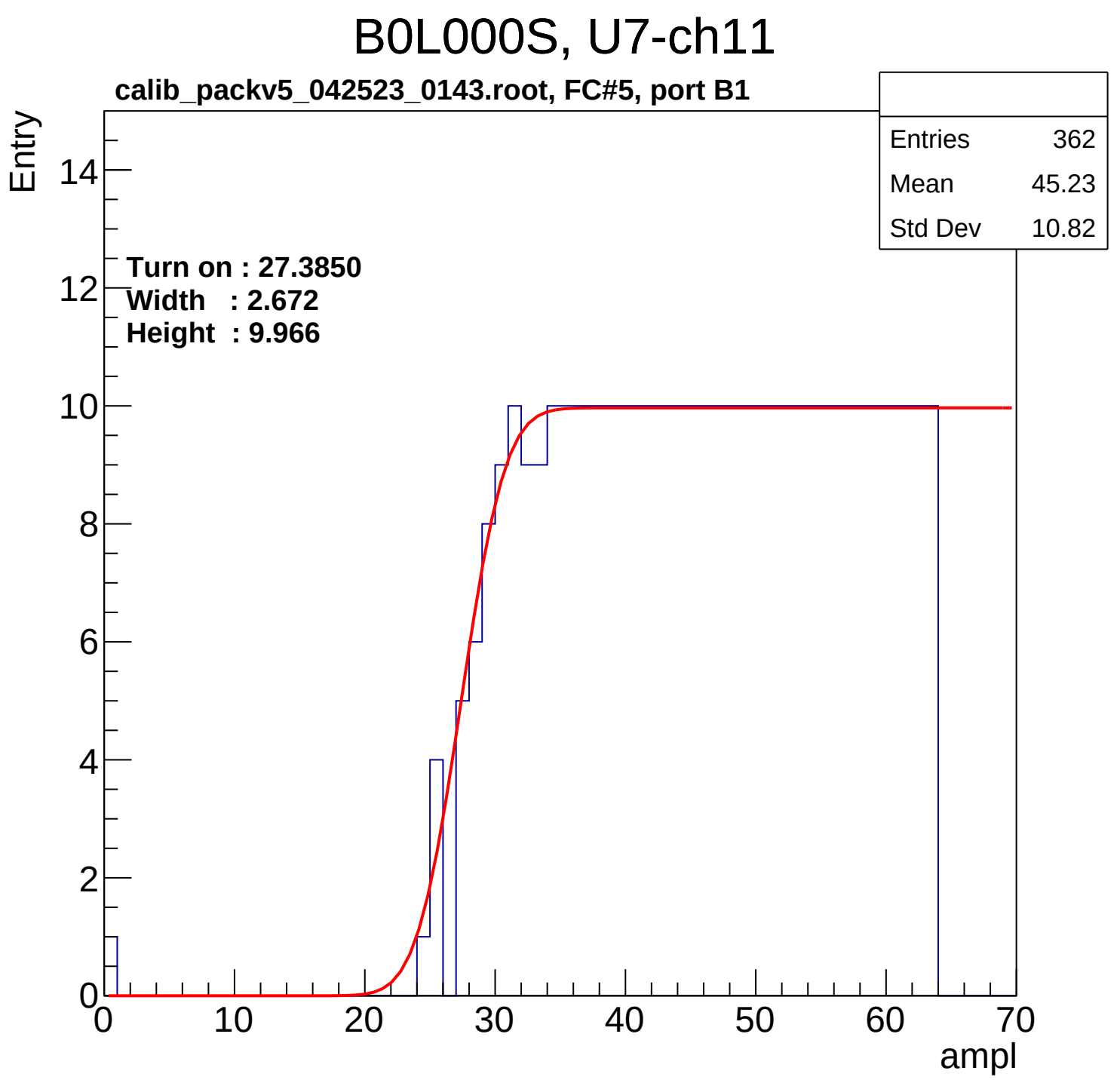
B0L000S, U7-ch11
calib_packv5_042523_0143.root, FC#5, port B1
Entries 362
Mean 45.23
Std Dev 10.82
Turn on : 27.3850
Width : 2.672
Height : 9.966
Entry
ampl
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6
8
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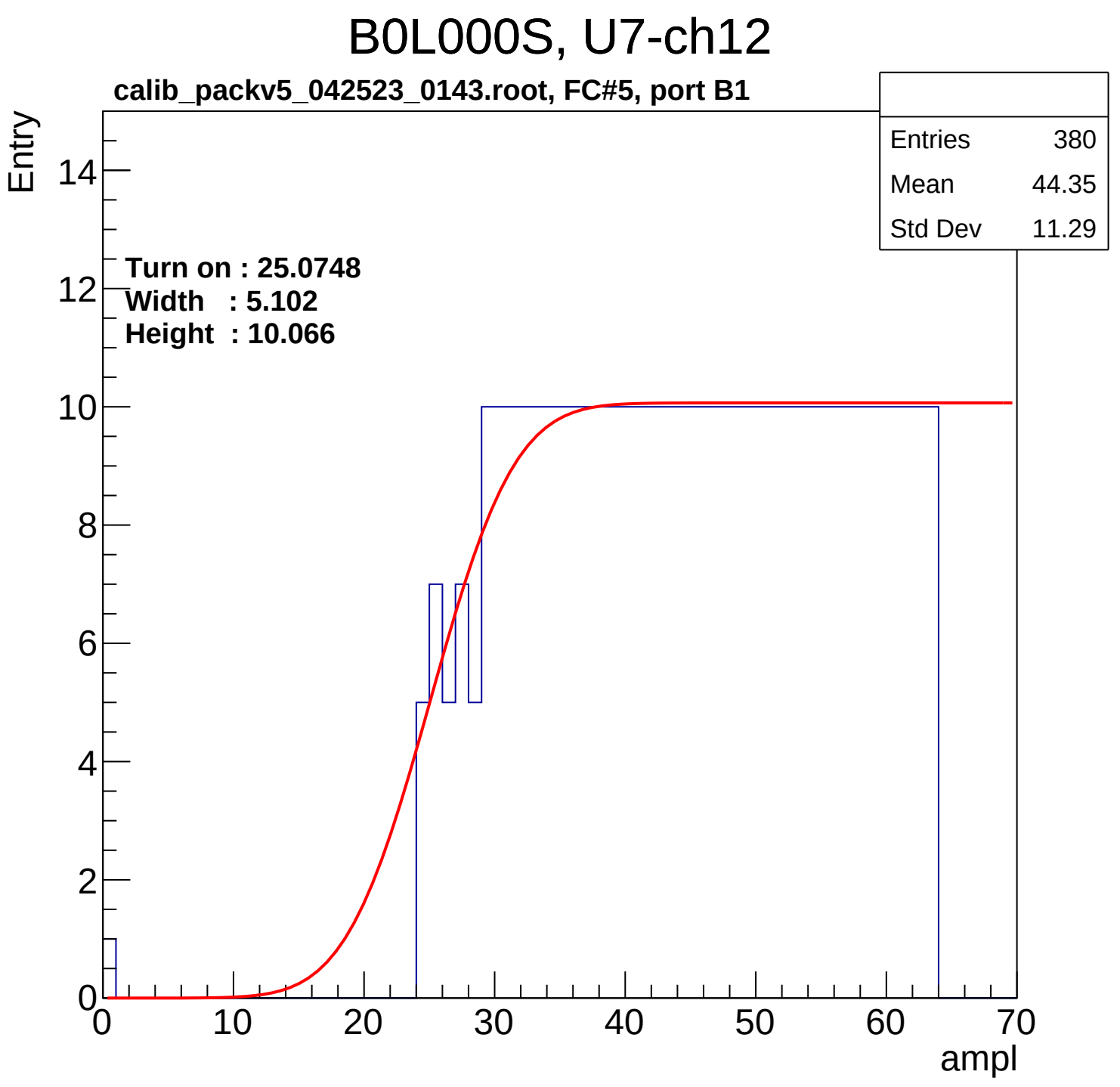
B0L000S, U7-ch12
calib_packv5_042523_0143.root, FC#5, port B1
Entries 380
Mean 44.35
Std Dev 11.29
Turn on : 25.0748
Width : 5.102
Height : 10.066
Entry
ampl
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8
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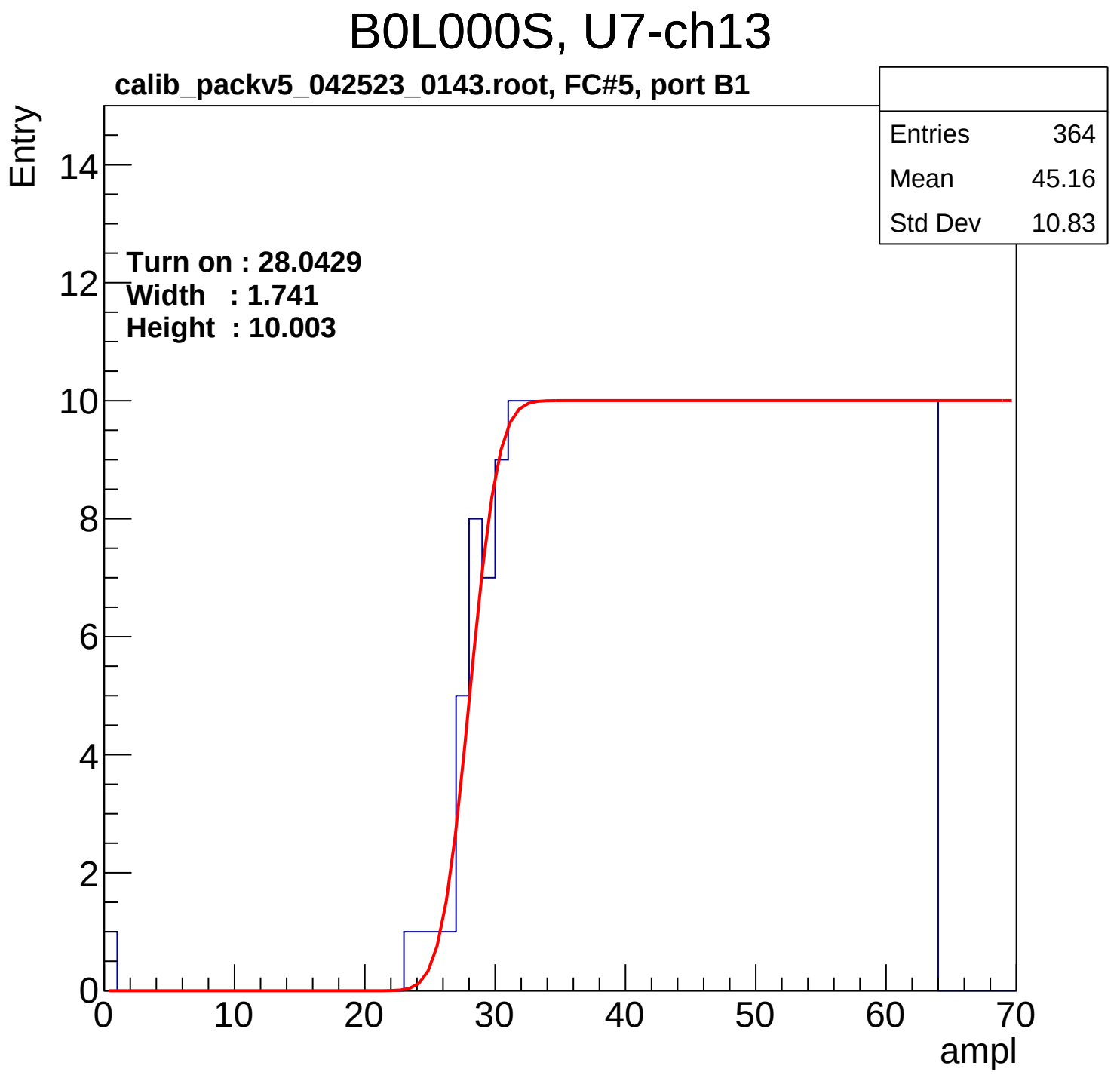
B0L000S, U7-ch13
calib_packv5_042523_0143.root, FC#5, port B1
Entries 364
Mean 45.16
Std Dev 10.83
Turn on : 28.0429
Width : 1.741
Height : 10.003
Entry
ampl
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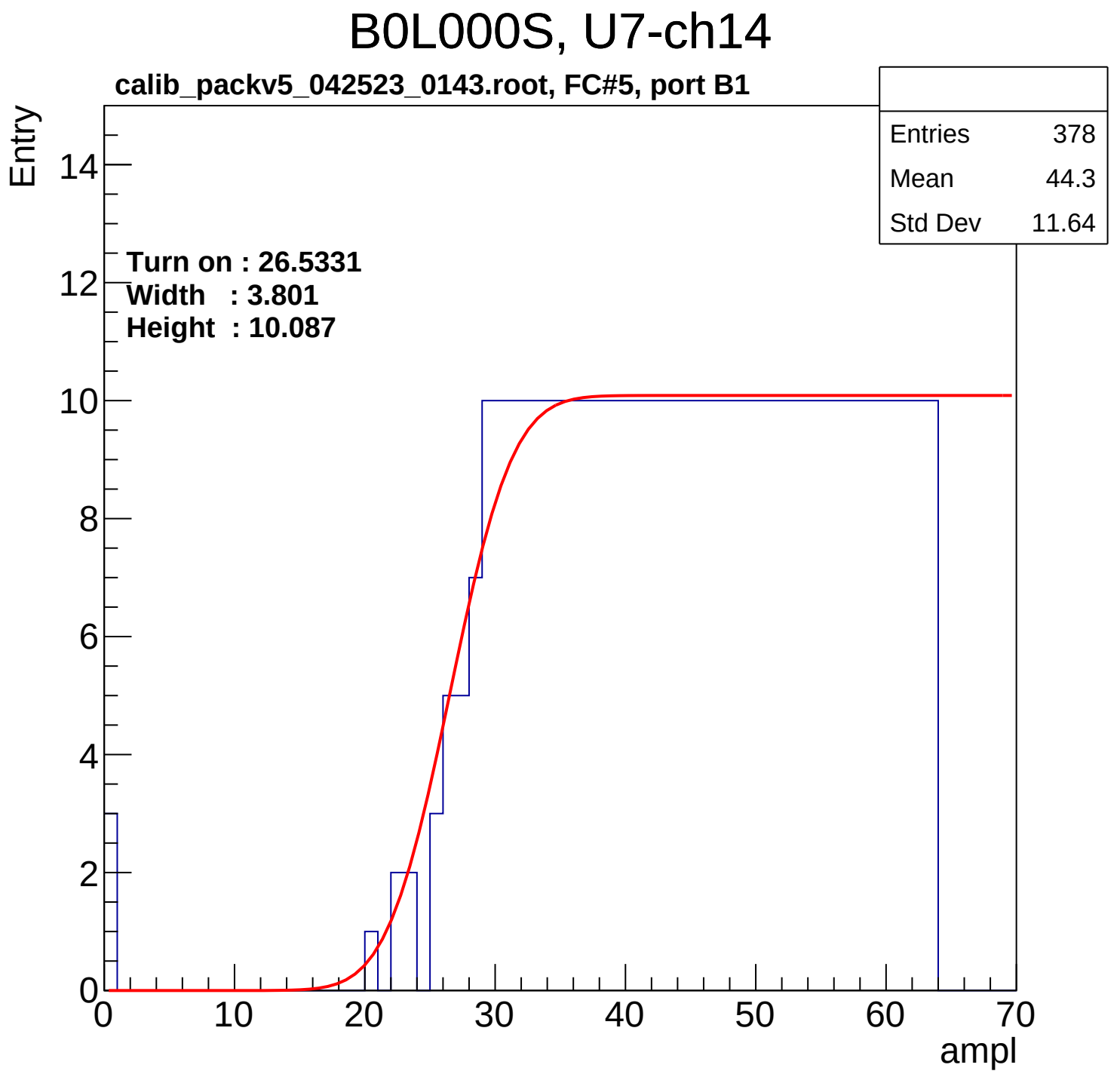
B0L000S, U7-ch14
calib_packv5_042523_0143.root, FC#5, port B1
Entries 378
Mean 44.3
Std Dev 11.64
Turn on : 26.5331
Width : 3.801
Height : 10.087
Entry
ampl
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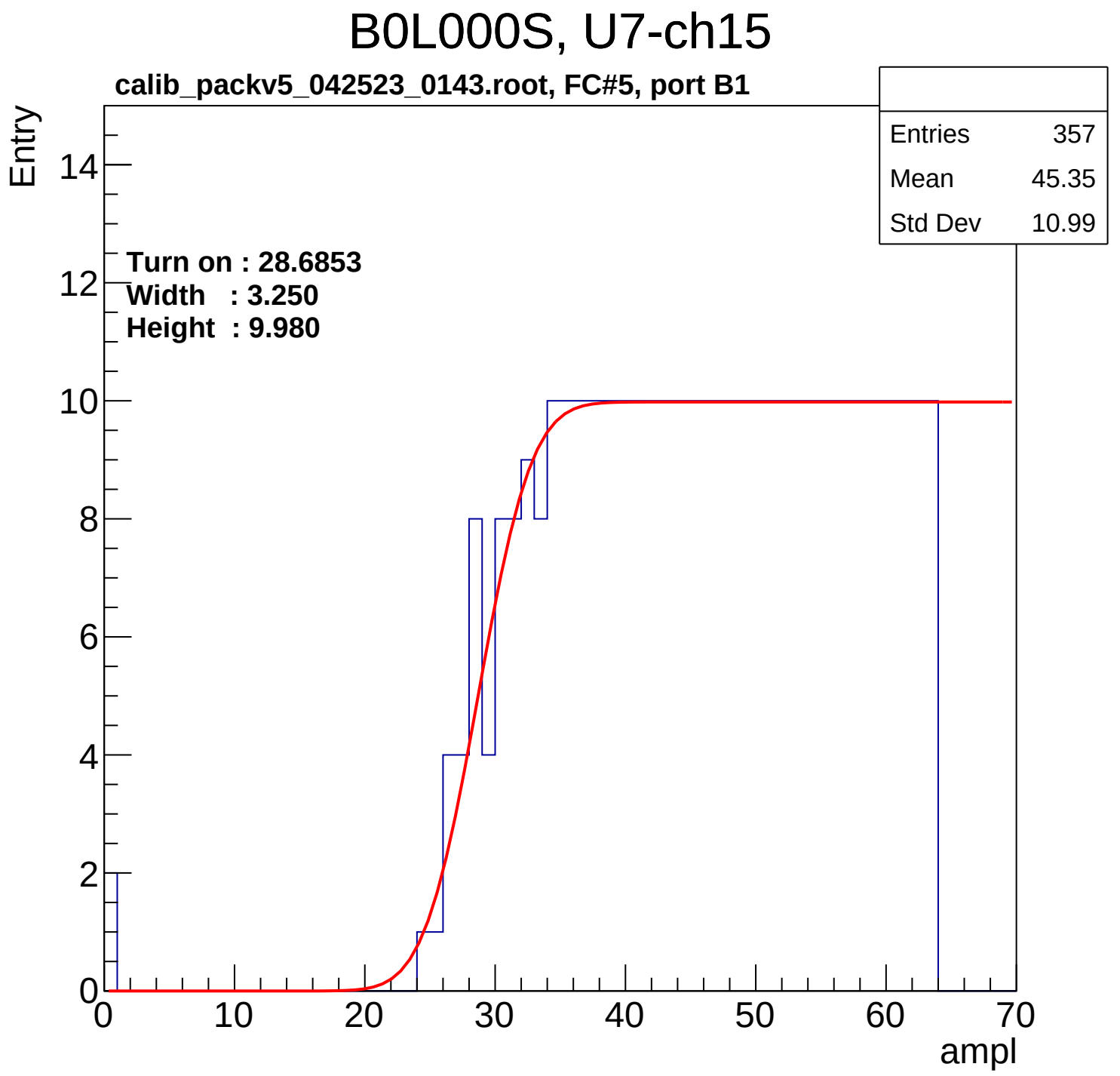
B0L000S, U7-ch15
calib_packv5_042523_0143.root, FC#5, port B1
Entries 357
Mean 45.35
Std Dev 10.99
Turn on : 28.6853
Width : 3.250
Height : 9.980
Entry
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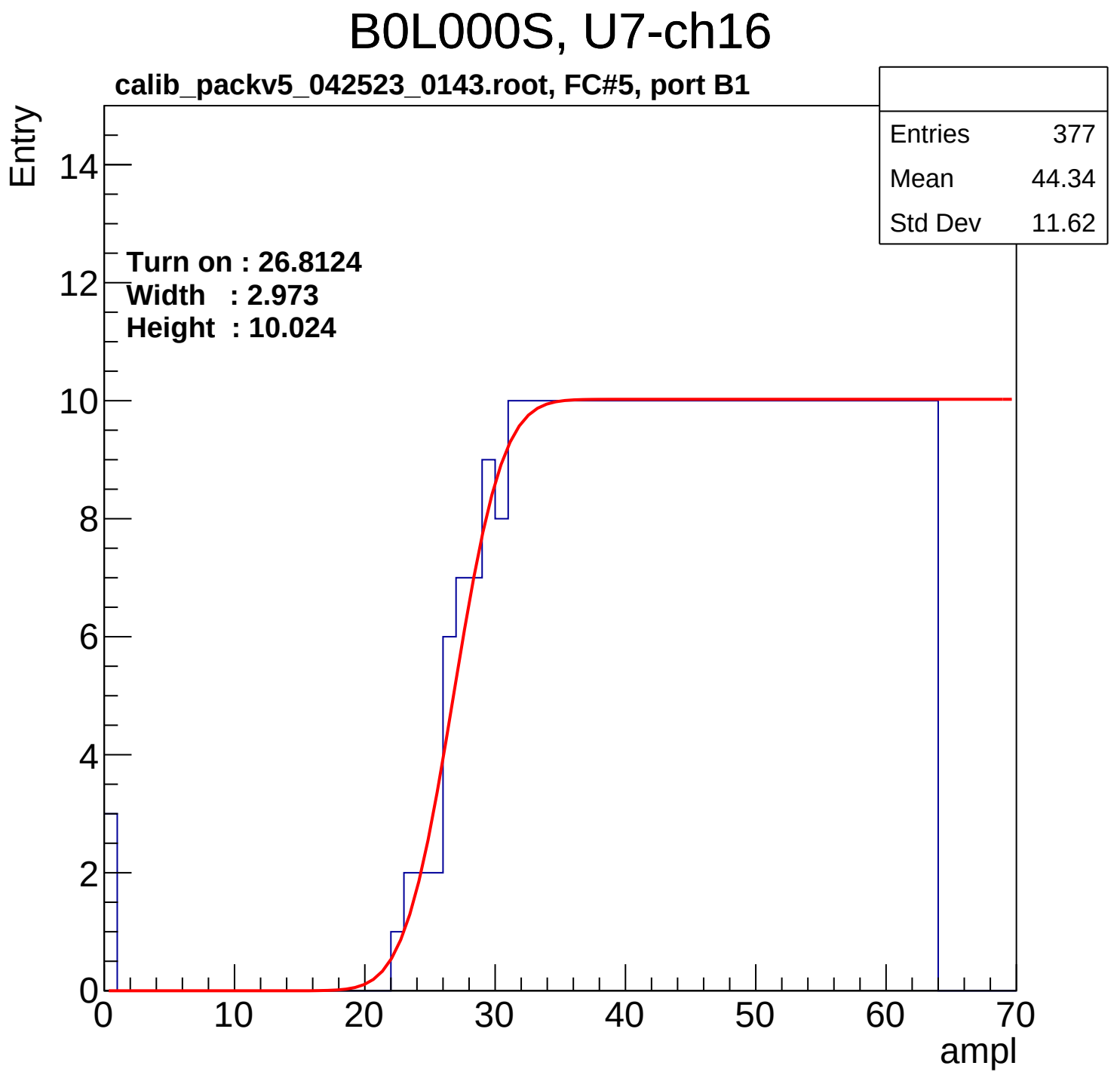
B0L000S, U7-ch16
calib_packv5_042523_0143.root, FC#5, port B1
Entries 377
Mean 44.34
Std Dev 11.62
Turn on : 26.8124
Width : 2.973
Height : 10.024
Entry
ampl
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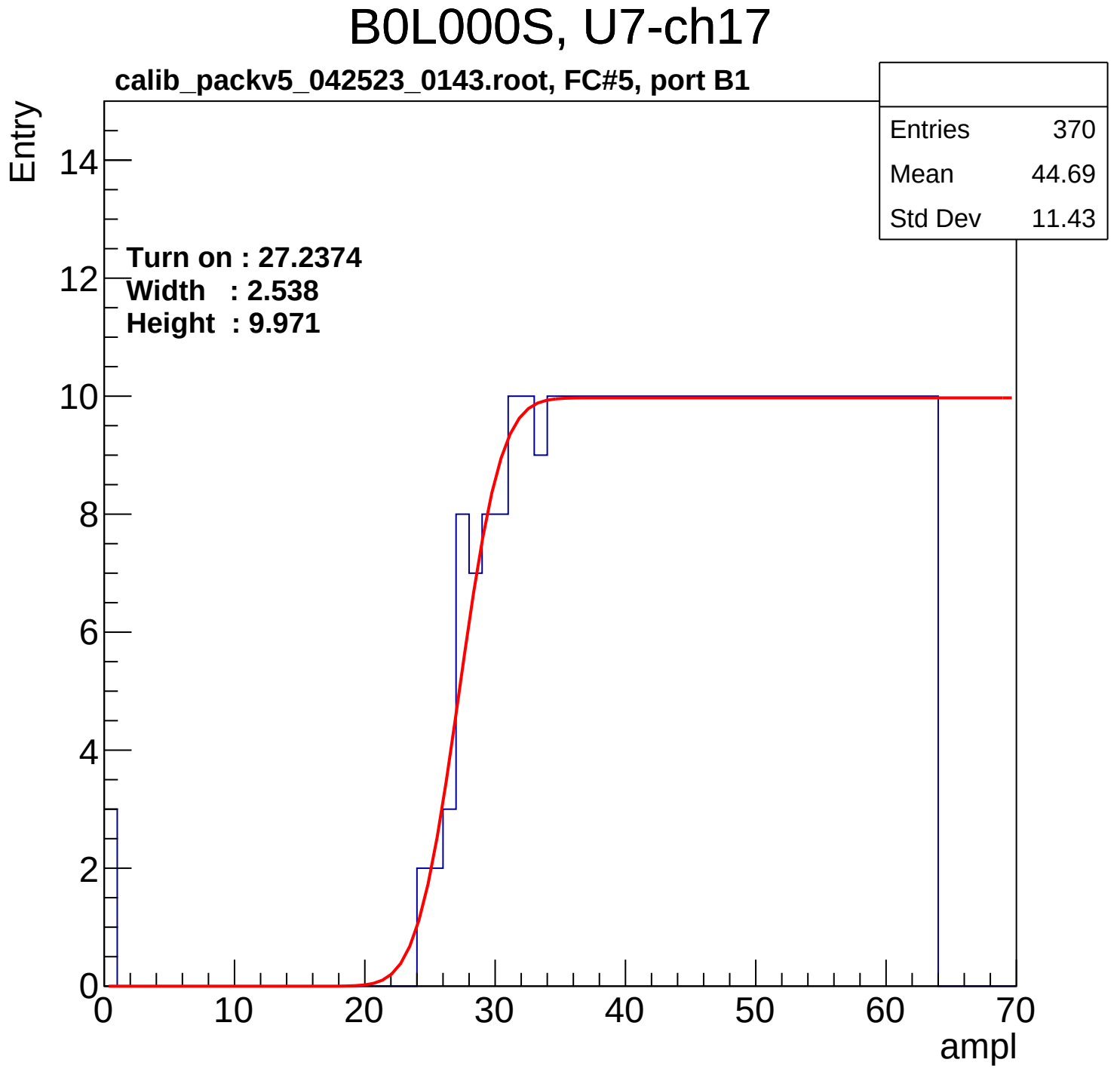
B0L000S, U7-ch17
calib_packv5_042523_0143.root, FC#5, port B1
Entries 370
Mean 44.69
Std Dev 11.43
Turn on : 27.2374
Width : 2.538
Height : 9.971
Entry
ampl
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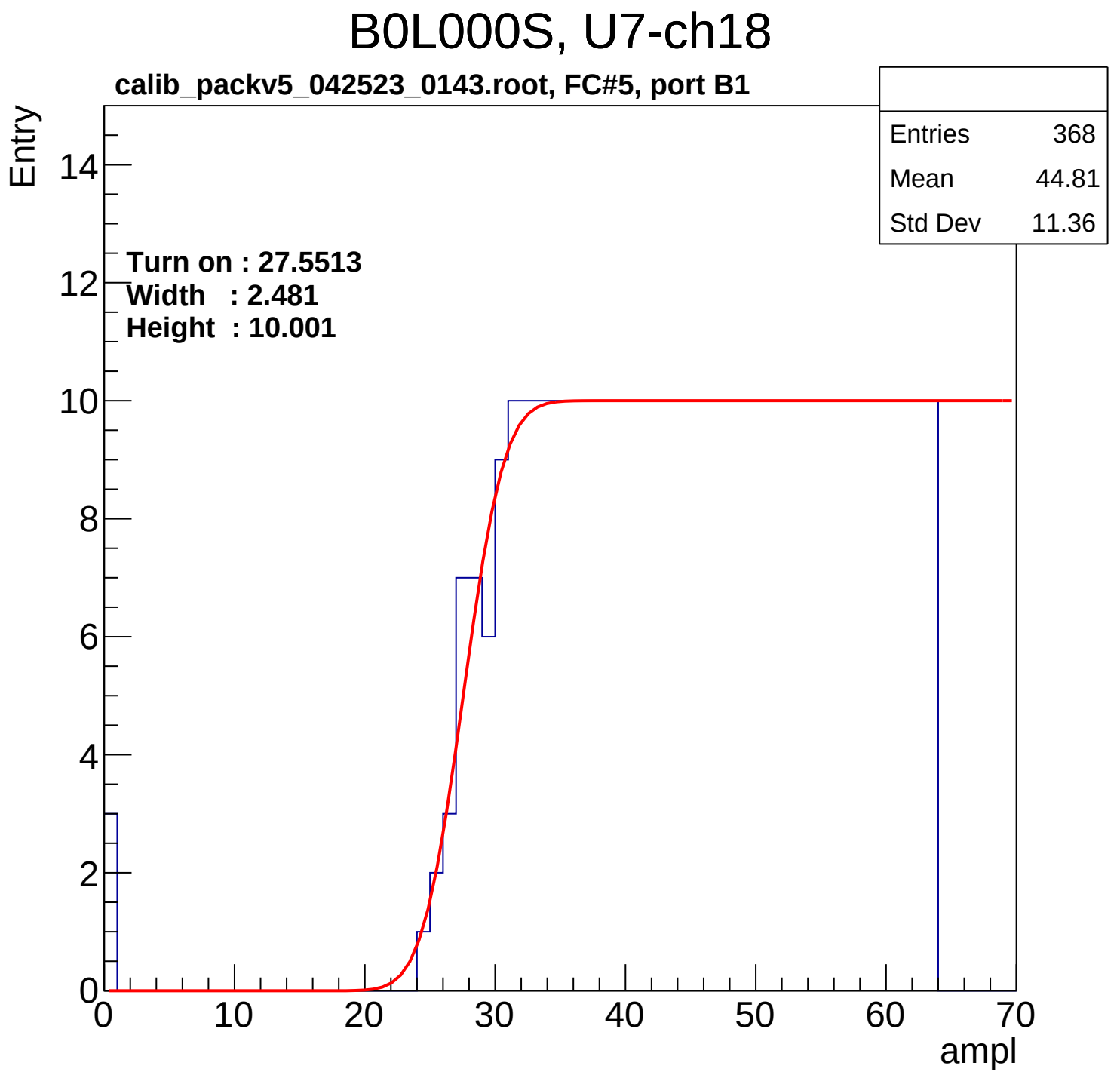
B0L000S, U7-ch18
calib_packv5_042523_0143.root, FC#5, port B1
Entries 368
Mean 44.81
Std Dev 11.36
Turn on : 27.5513
Width : 2.481
Height : 10.001
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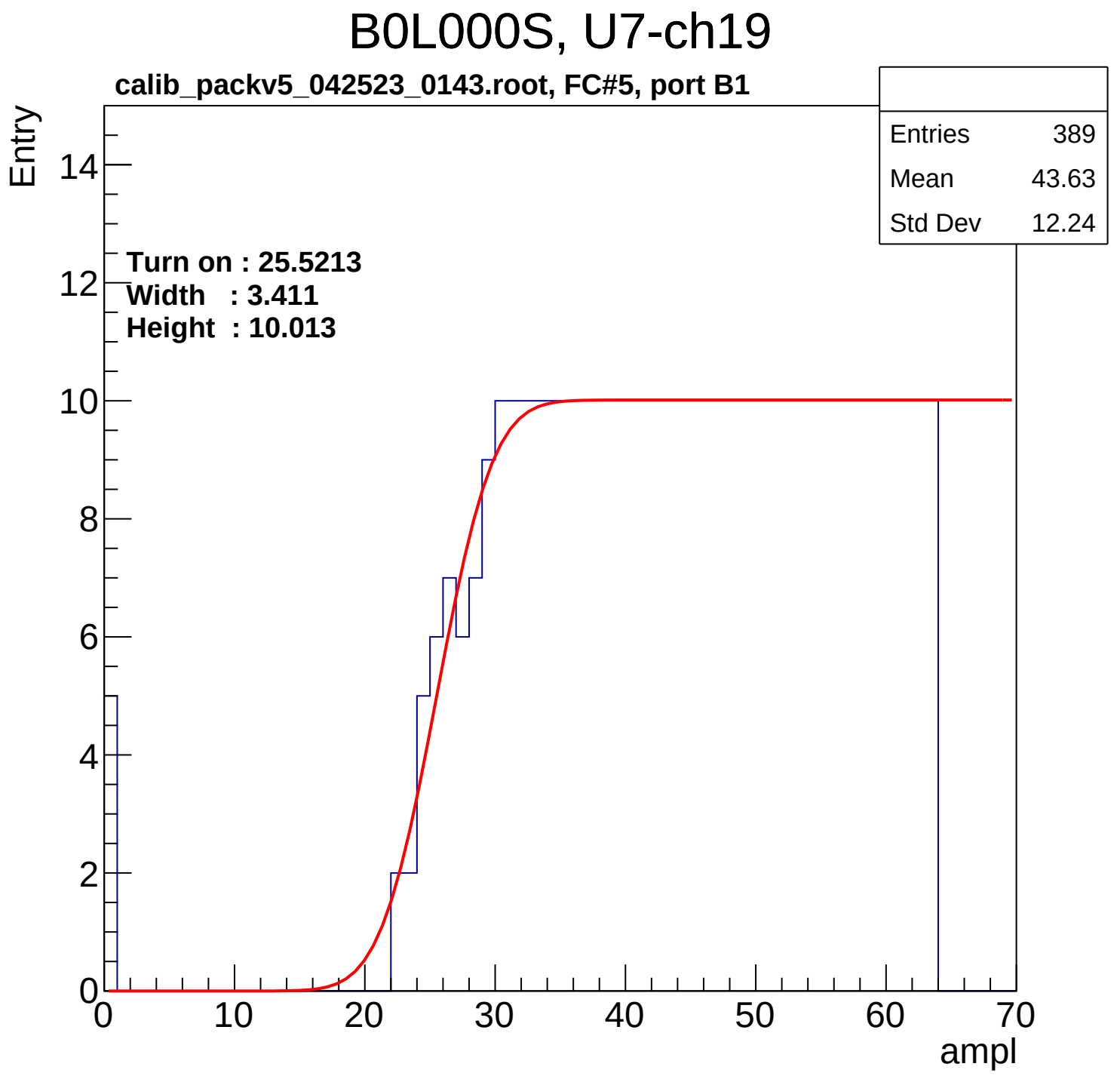
B0L000S, U7-ch19
calib_packv5_042523_0143.root, FC#5, port B1
Entries 389
Mean 43.63
Std Dev 12.24
Turn on : 25.5213
Width : 3.411
Height : 10.013
Entry
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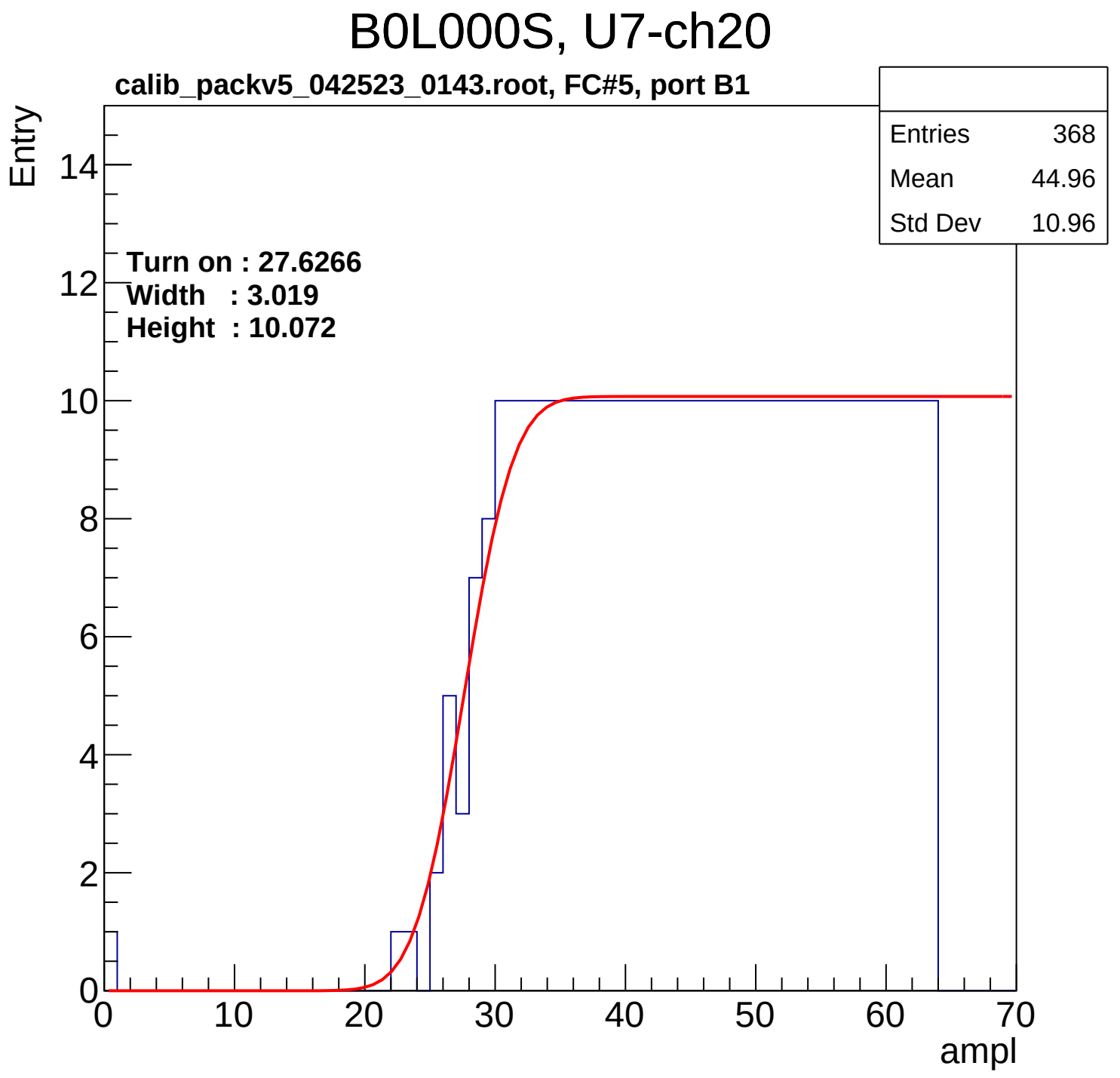
B0L000S, U7-ch20
calib_packv5_042523_0143.root, FC#5, port B1
Entries 368
Mean 44.96
Std Dev 10.96
Turn on : 27.6266
Width : 3.019
Height : 10.072
Entry
ampl
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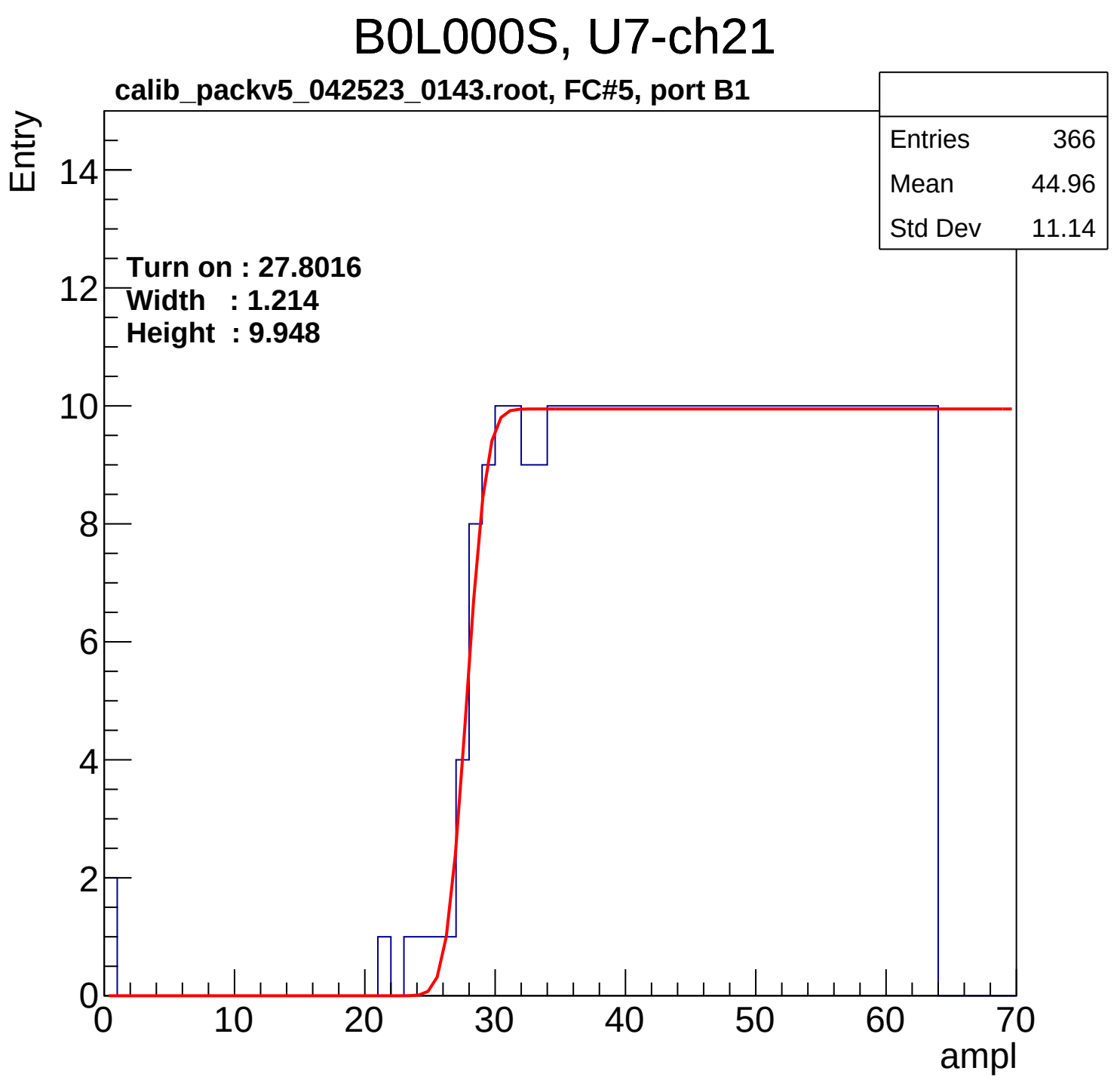
B0L000S, U7-ch21
calib_packv5_042523_0143.root, FC#5, port B1
Entries 366
Mean 44.96
Std Dev 11.14
Turn on : 27.8016
Width : 1.214
Height : 9.948
Entry
ampl
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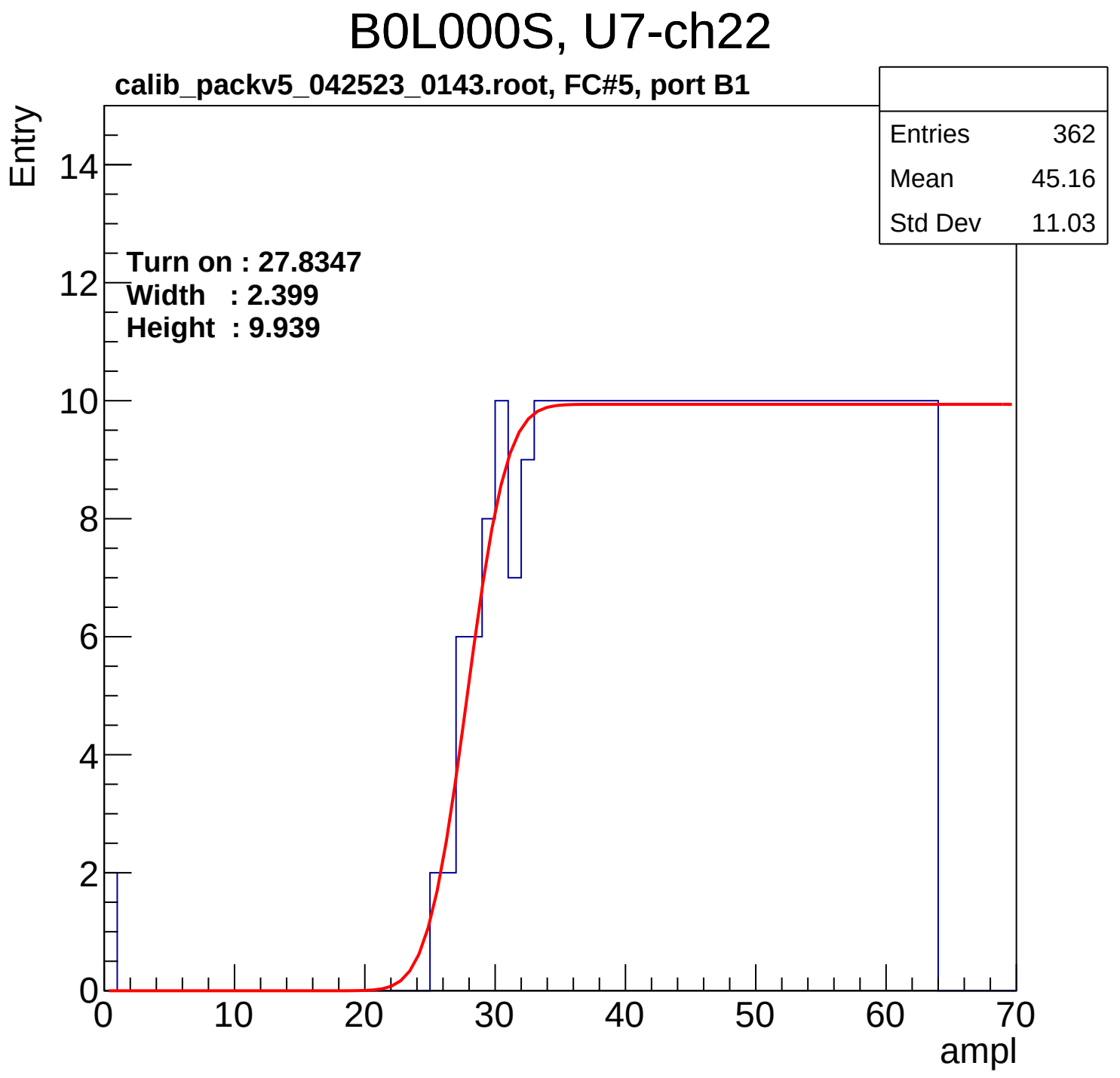
B0L000S, U7-ch22
calib_packv5_042523_0143.root, FC#5, port B1
Entries 362
Mean 45.16
Std Dev 11.03
Turn on : 27.8347
Width : 2.399
Height : 9.939
Entry
ampl
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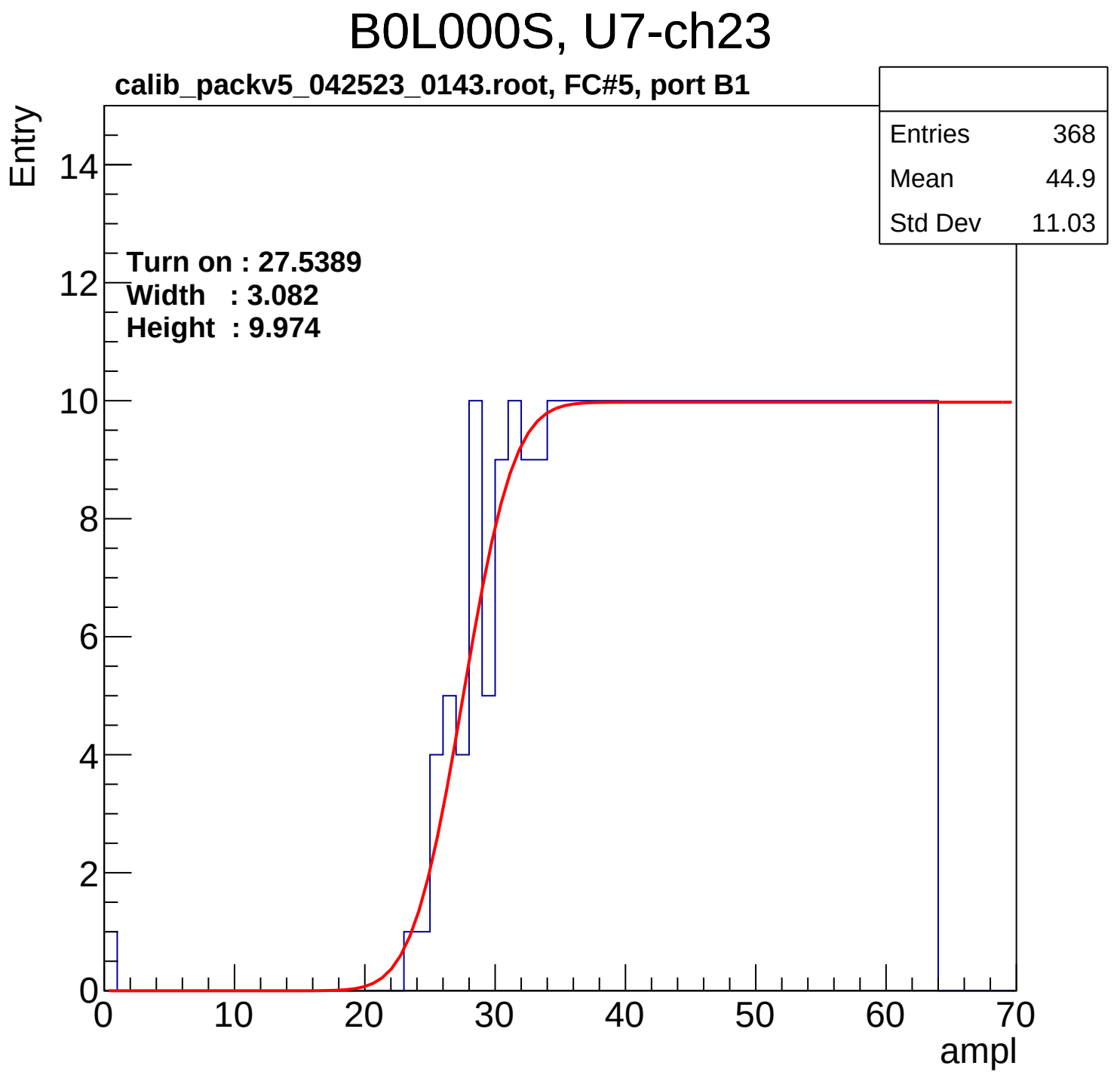
B0L000S, U7-ch23
calib_packv5_042523_0143.root, FC#5, port B1
Entries 368
Mean 44.9
Std Dev 11.03
Turn on : 27.5389
Width : 3.082
Height : 9.974
Entry
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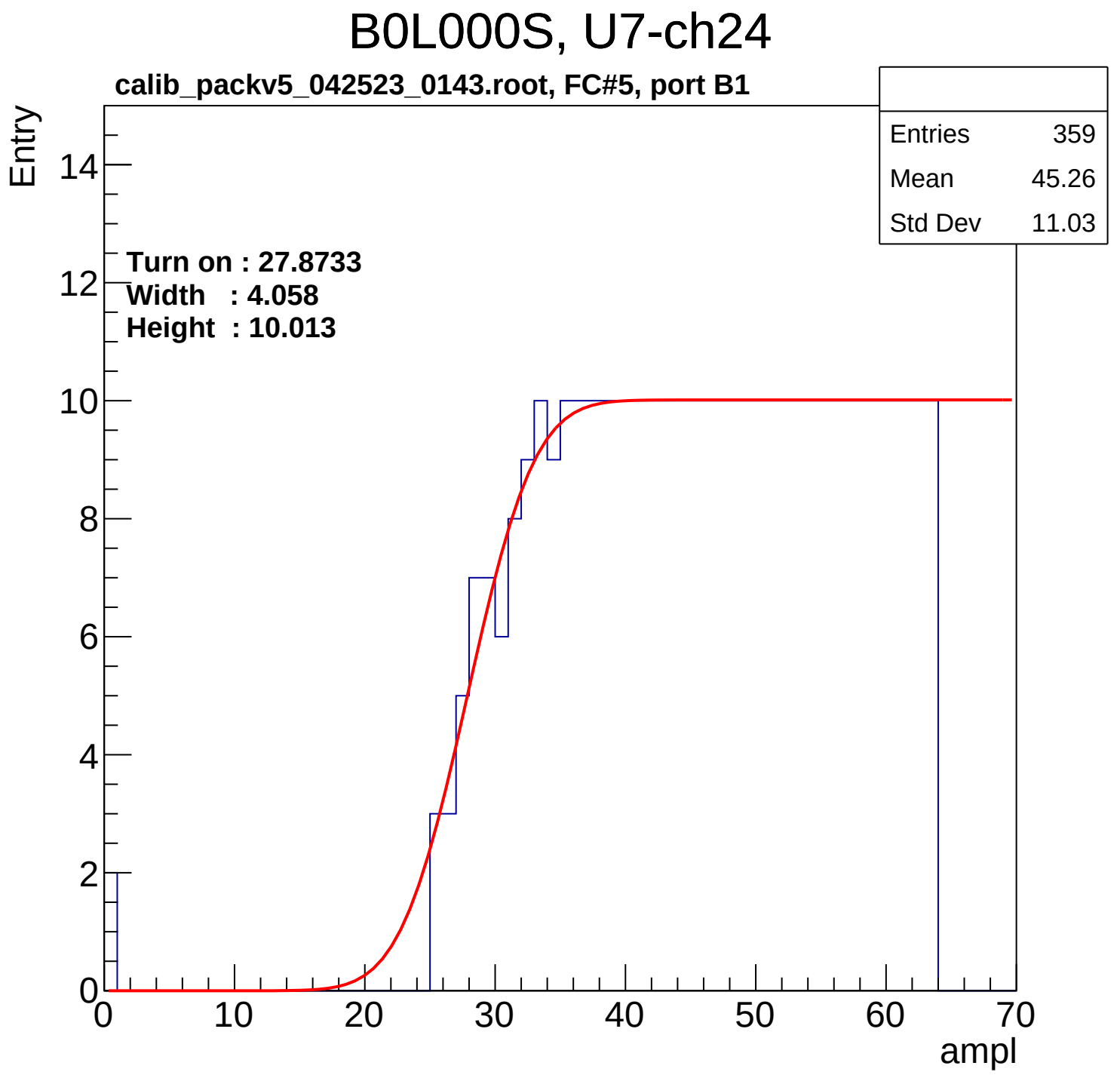
B0L000S, U7-ch24
calib_packv5_042523_0143.root, FC#5, port B1
Entries 359
Mean 45.26
Std Dev 11.03
Turn on : 27.8733
Width : 4.058
Height : 10.013
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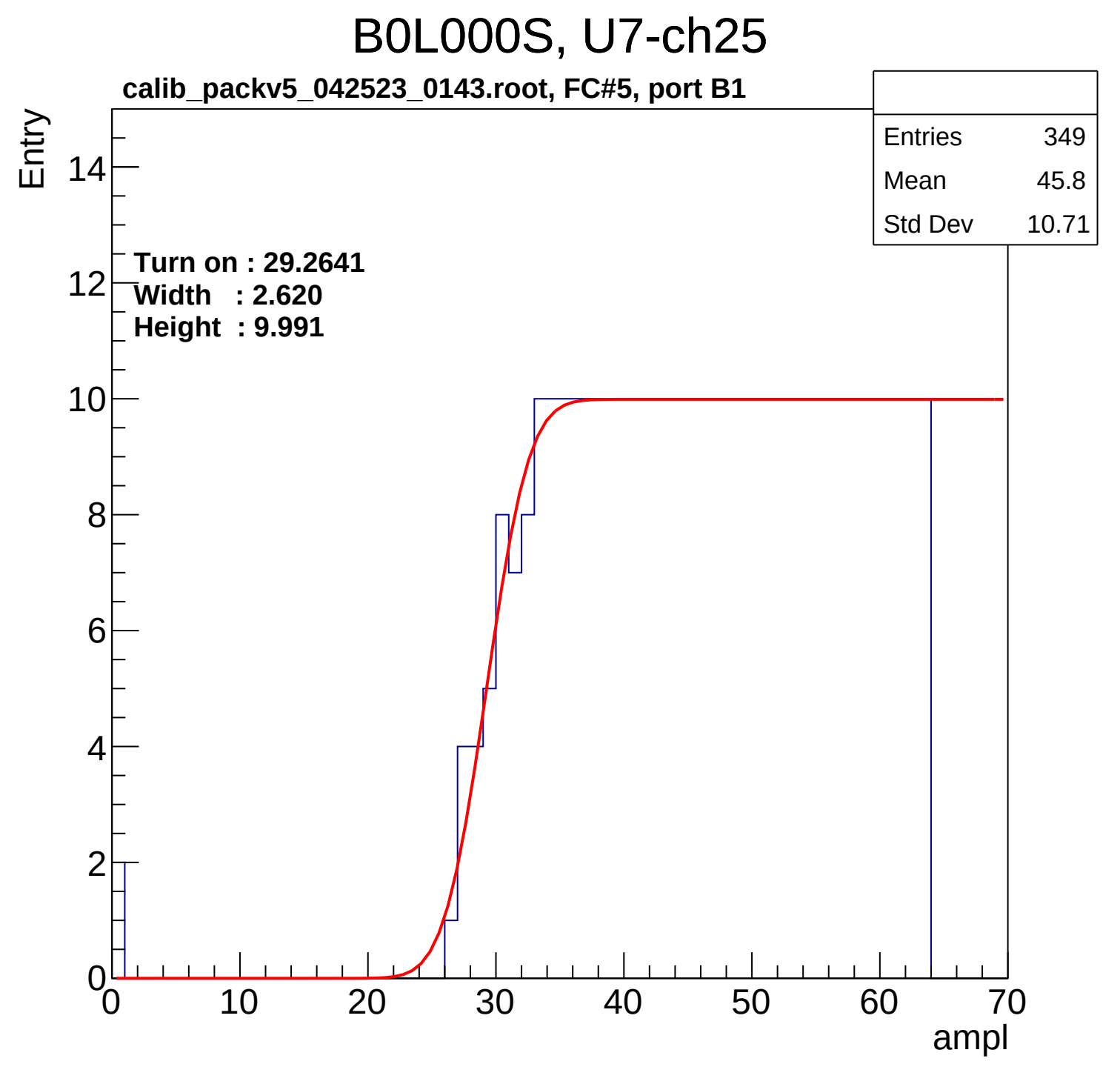
B0L000S, U7-ch25
calib_packv5_042523_0143.root, FC#5, port B1
Entries 349
Mean 45.8
Std Dev 10.71
Turn on : 29.2641
Width : 2.620
Height : 9.991
Entry
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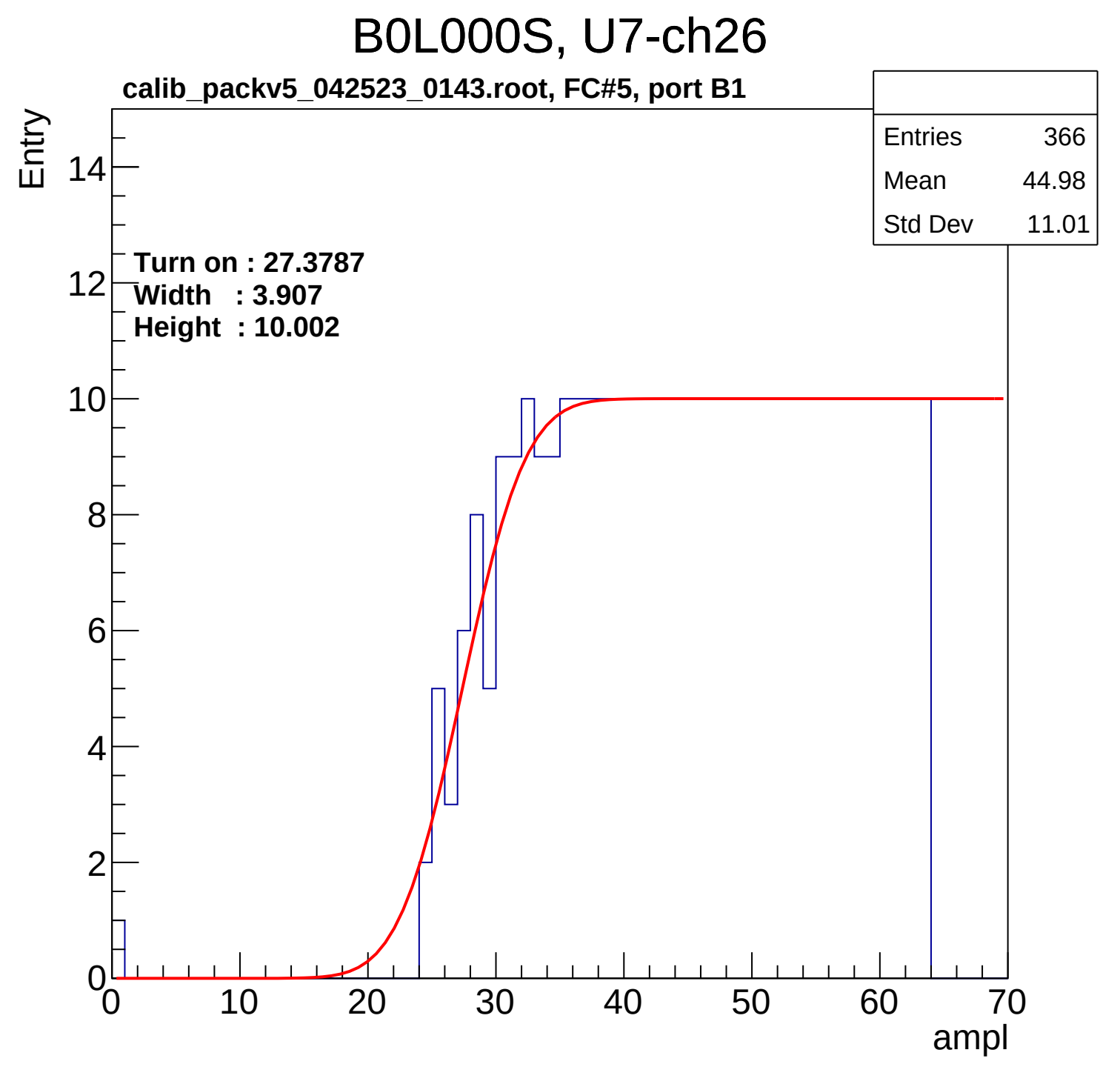
B0L000S, U7-ch26
calib_packv5_042523_0143.root, FC#5, port B1
Entries 366
Mean 44.98
Std Dev 11.01
Turn on : 27.3787
Width : 3.907
Height : 10.002
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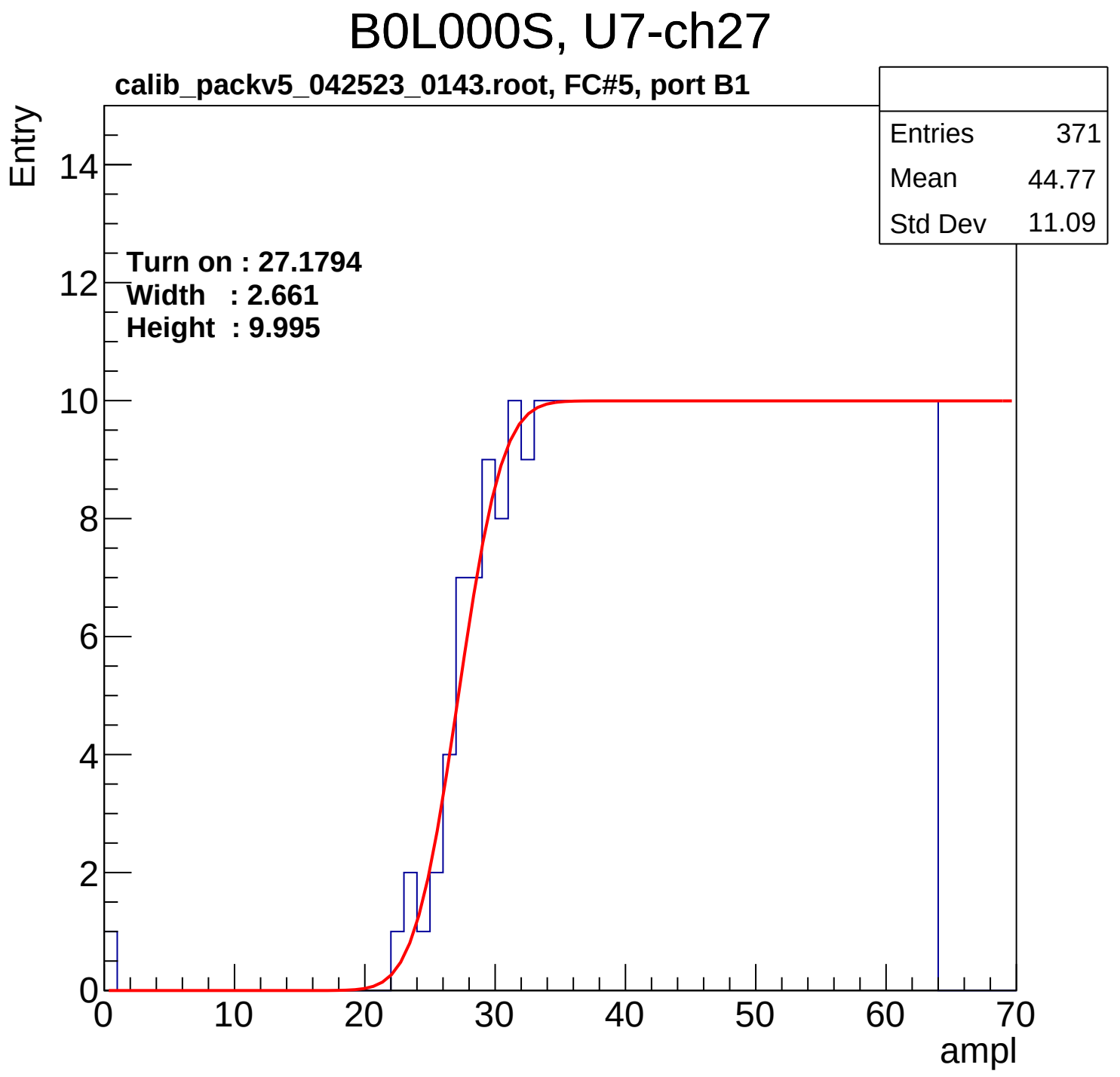
B0L000S, U7-ch27
calib_packv5_042523_0143.root, FC#5, port B1
Entries 371
Mean 44.77
Std Dev 11.09
Turn on : 27.1794
Width : 2.661
Height : 9.995
Entry
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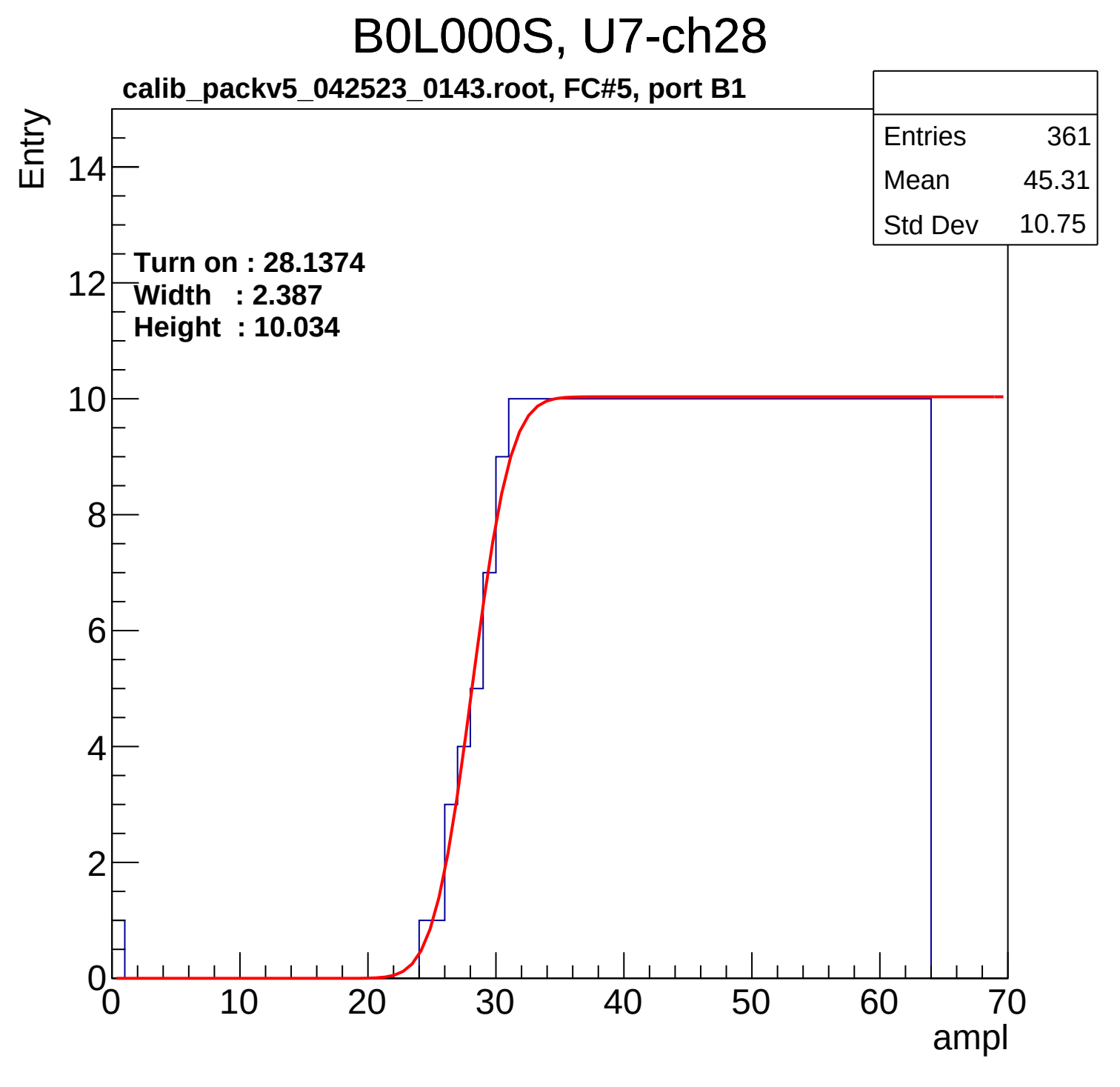
B0L000S, U7-ch28
calib_packv5_042523_0143.root, FC#5, port B1
Entries 361
Mean 45.31
Std Dev 10.75
Turn on : 28.1374
Width : 2.387
Height : 10.034
Entry
ampl
0
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4
6
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12
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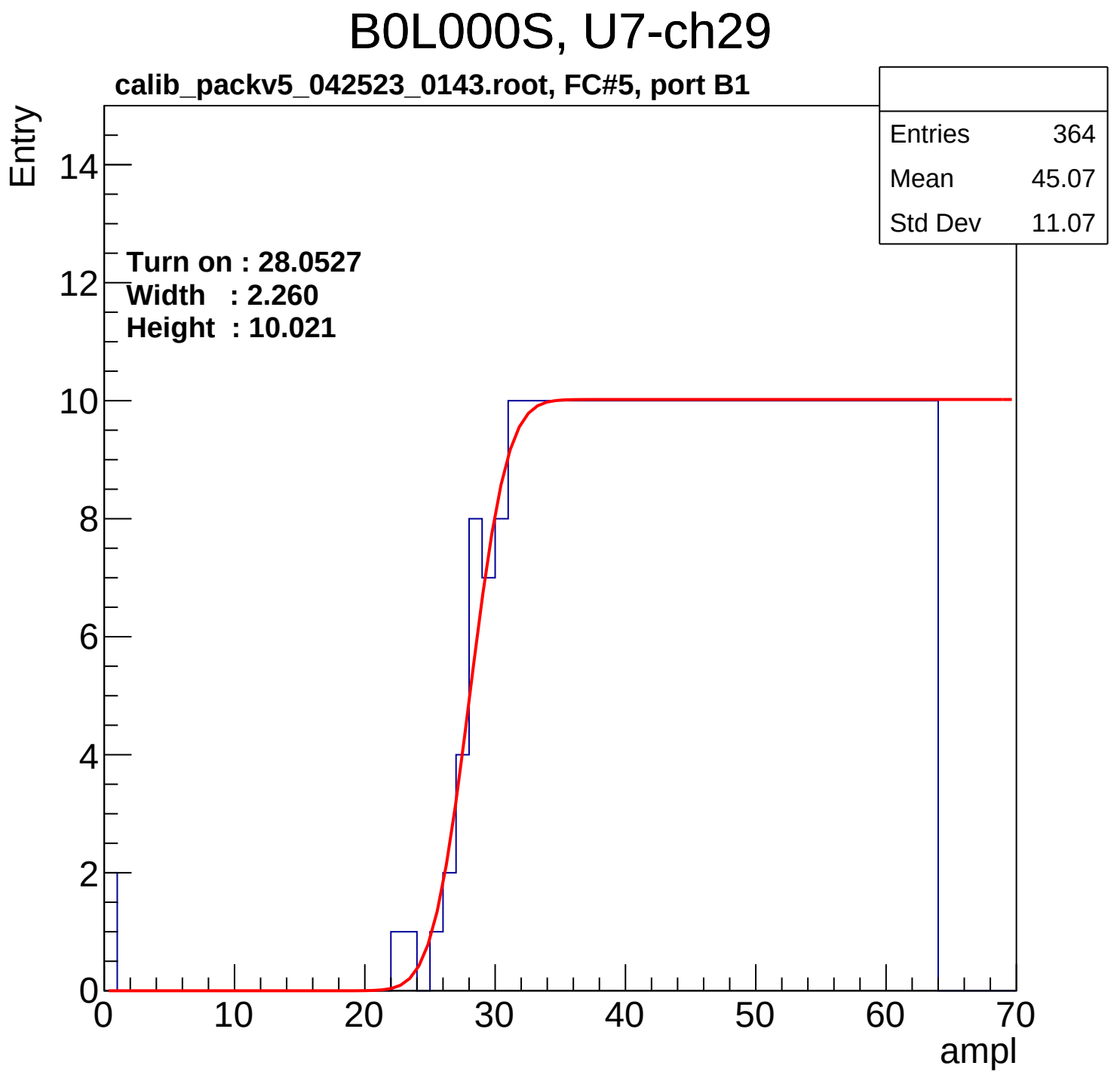
B0L000S, U7-ch29
calib_packv5_042523_0143.root, FC#5, port B1
Entries 364
Mean 45.07
Std Dev 11.07
Turn on : 28.0527
Width : 2.260
Height : 10.021
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ampl
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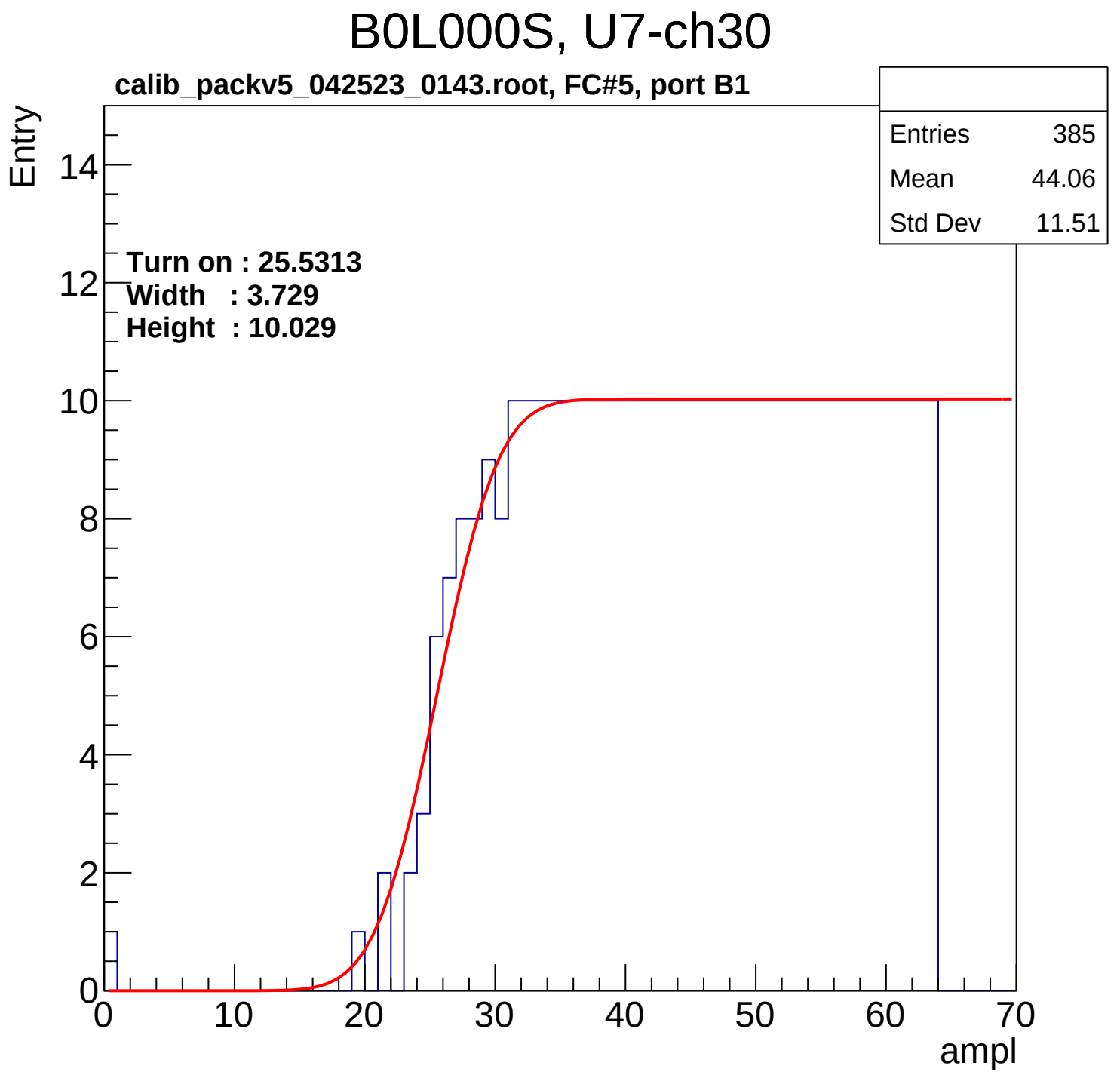
B0L000S, U7-ch30
calib_packv5_042523_0143.root, FC#5, port B1
Entries 385
Mean 44.06
Std Dev 11.51
Turn on : 25.5313
Width : 3.729
Height : 10.029
Entry
ampl
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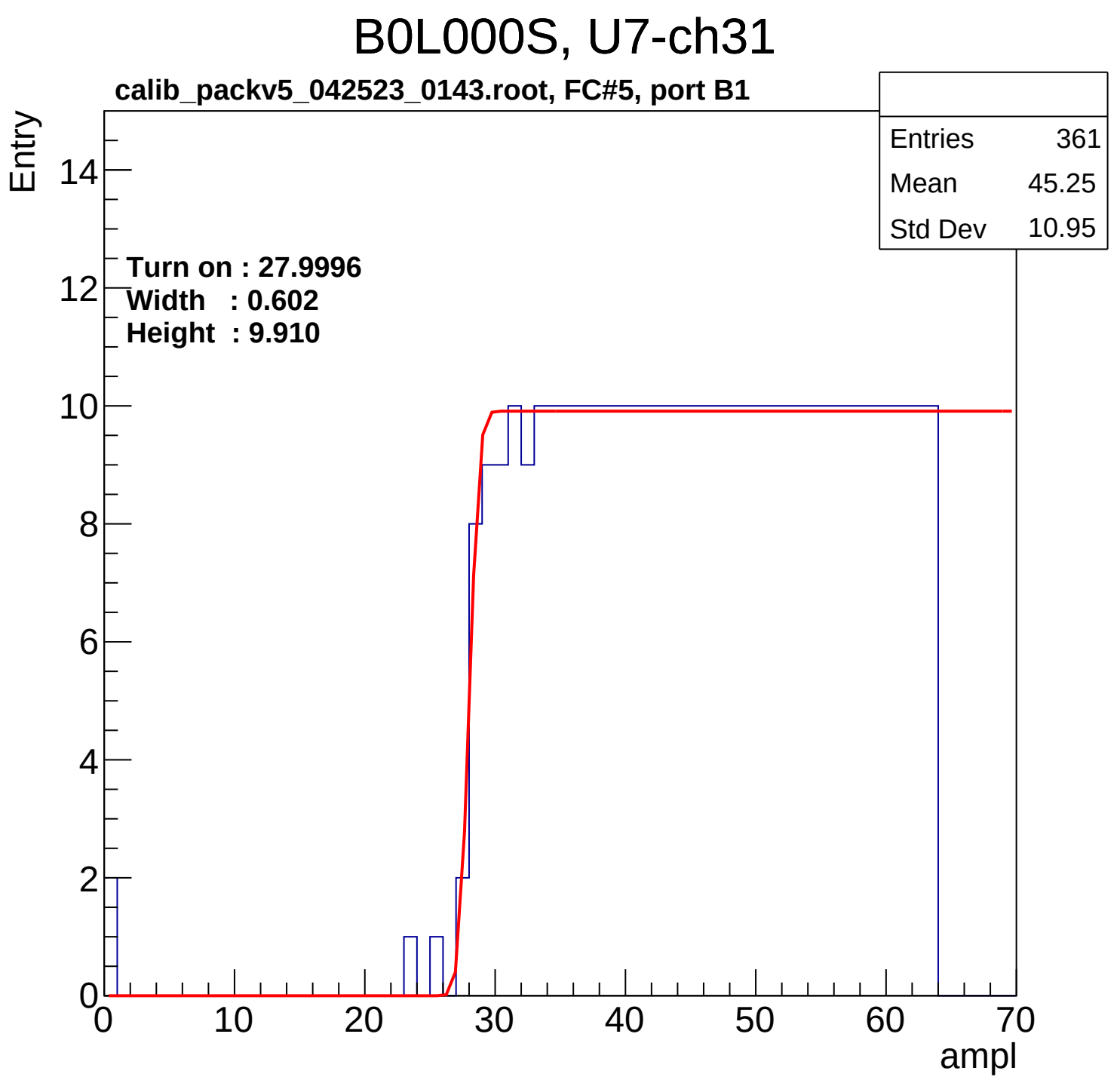
B0L000S, U7-ch31
calib_packv5_042523_0143.root, FC#5, port B1
Entries 361
Mean 45.25
Std Dev 10.95
Turn on : 27.9996
Width : 0.602
Height : 9.910
Entry
ampl
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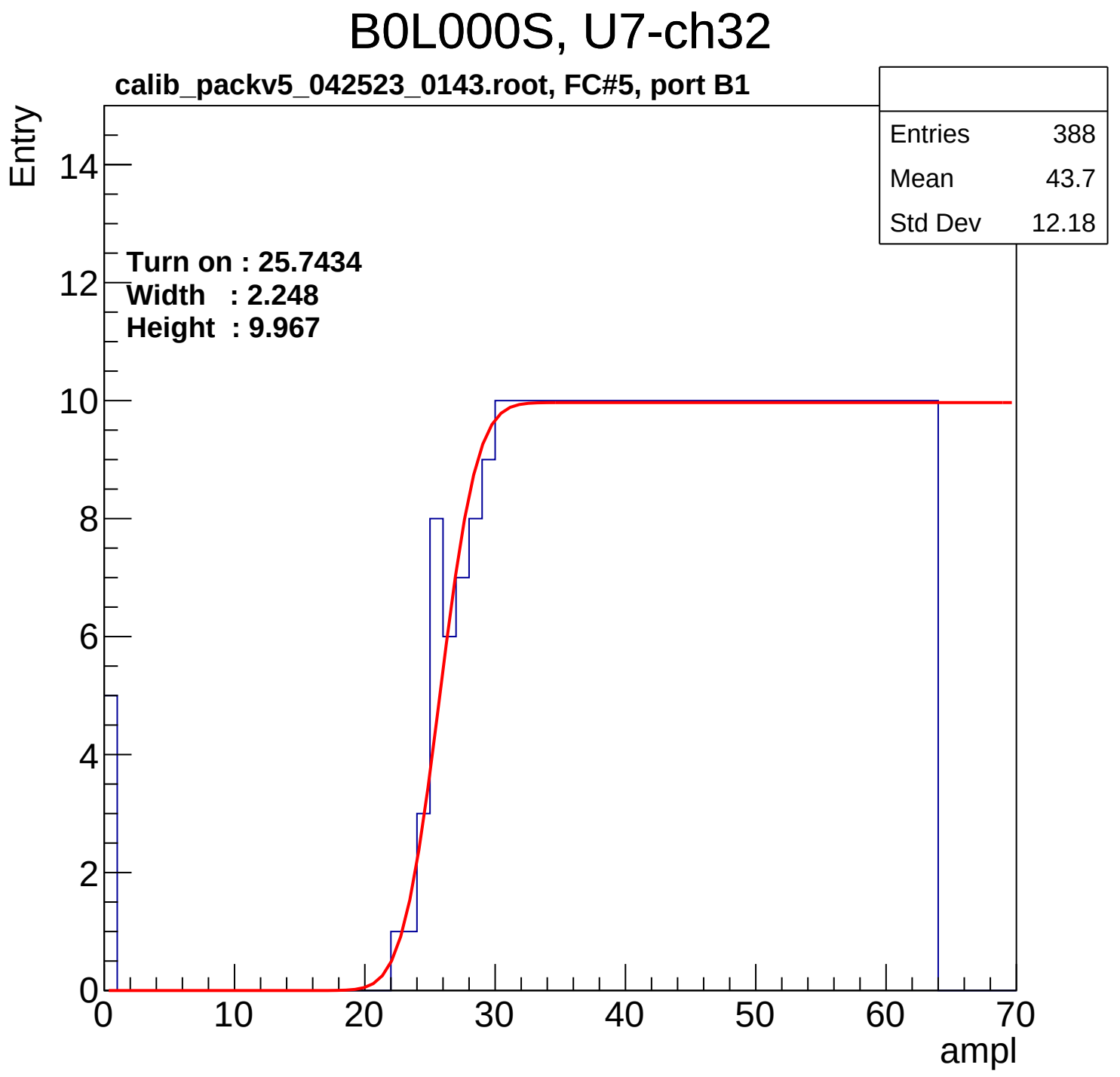
B0L000S, U7-ch32
calib_packv5_042523_0143.root, FC#5, port B1
Entries 388
Mean 43.7
Std Dev 12.18
Turn on : 25.7434
Width : 2.248
Height : 9.967
Entry
ampl
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2
4
6
8
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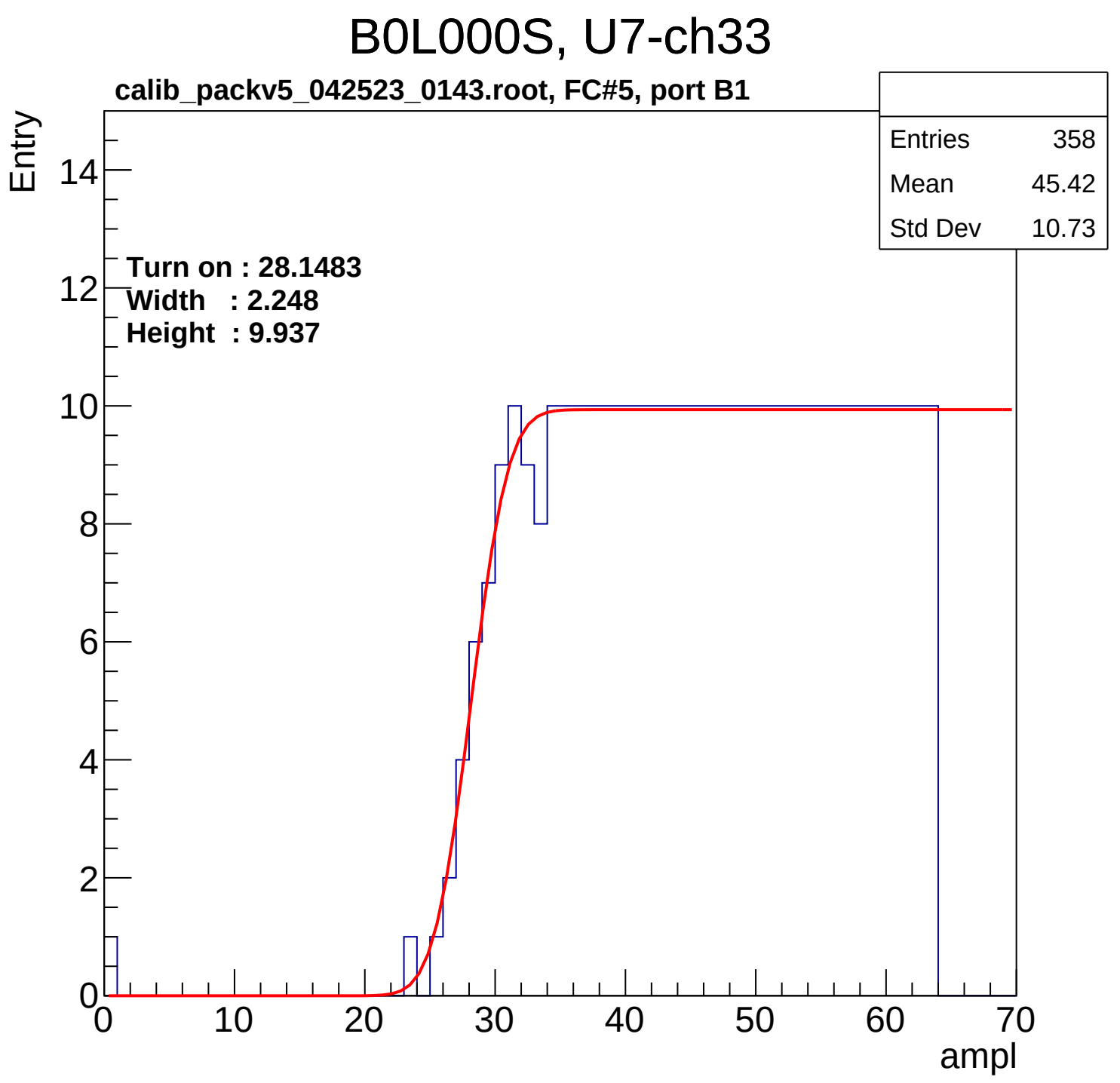
B0L000S, U7-ch33
calib_packv5_042523_0143.root, FC#5, port B1
Entries 358
Mean 45.42
Std Dev 10.73
Turn on : 28.1483
Width : 2.248
Height : 9.937
Entry
ampl
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2
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6
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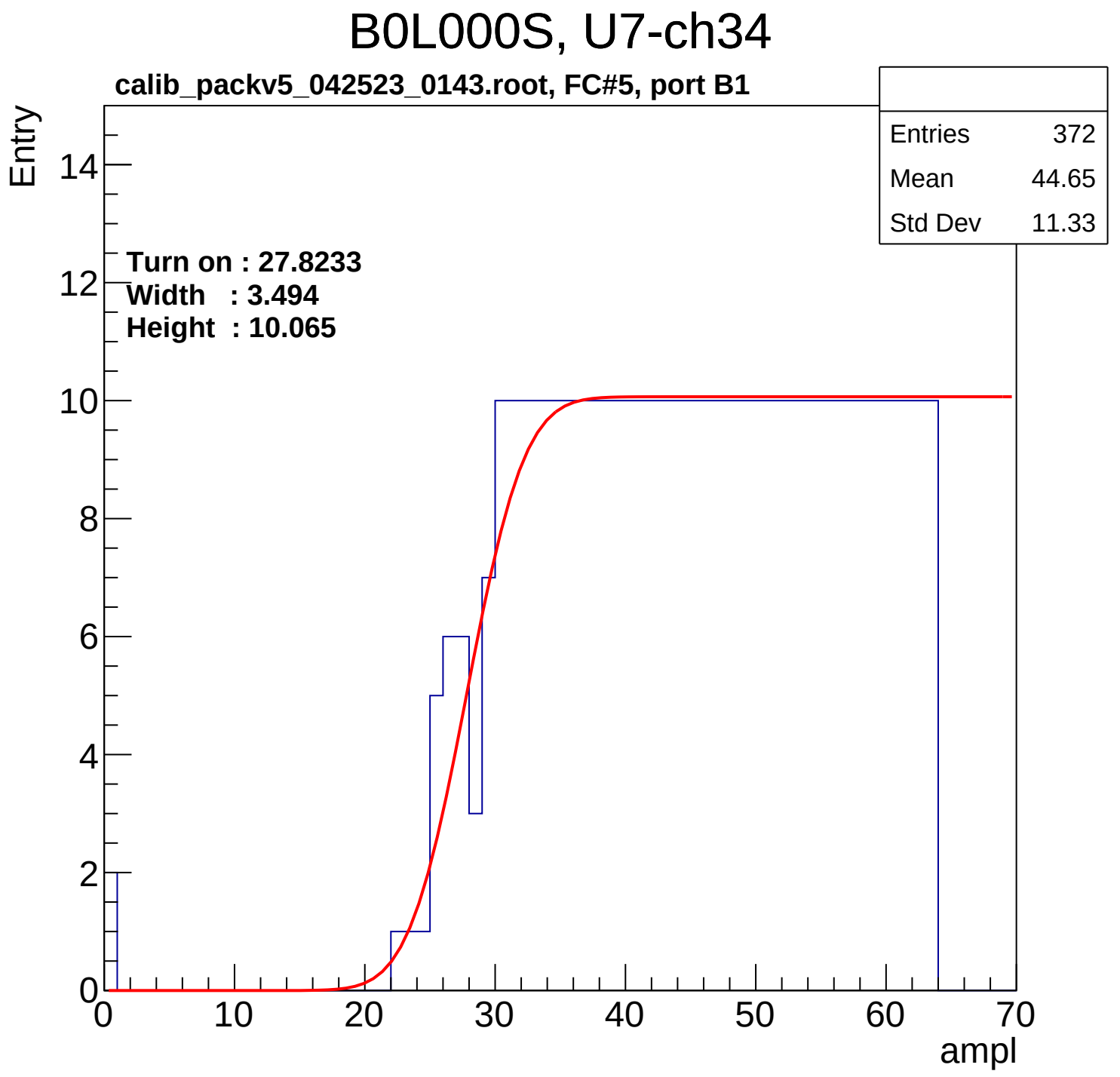
B0L000S, U7-ch34
calib_packv5_042523_0143.root, FC#5, port B1
Entries 372
Mean 44.65
Std Dev 11.33
Turn on : 27.8233
Width : 3.494
Height : 10.065
Entry
ampl
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2
4
6
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0
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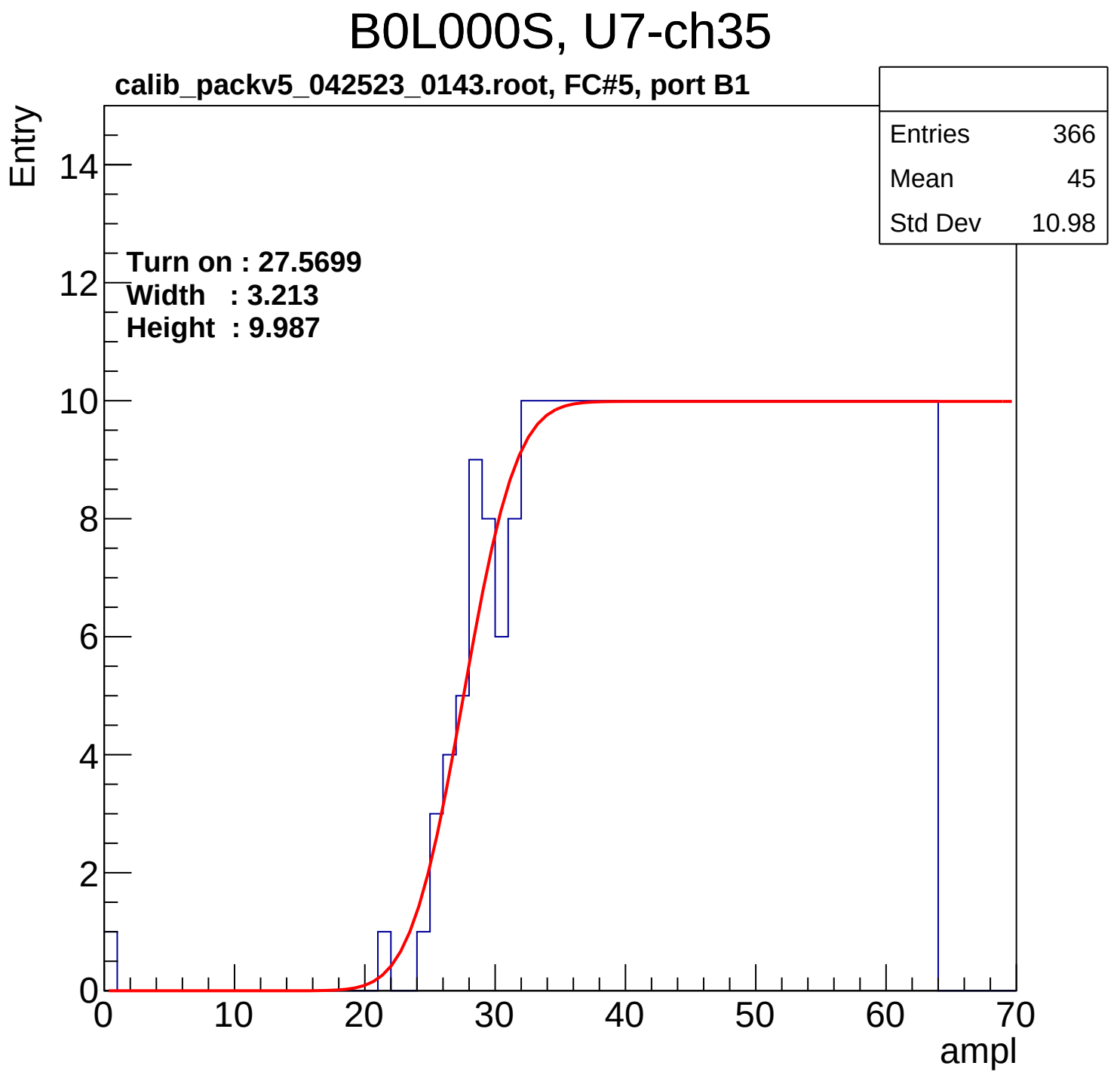
B0L000S, U7-ch35
calib_packv5_042523_0143.root, FC#5, port B1
Entries 366
Mean 45
Std Dev 10.98
Turn on : 27.5699
Width : 3.213
Height : 9.987
Entry
ampl
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2
4
6
8
10
12
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0
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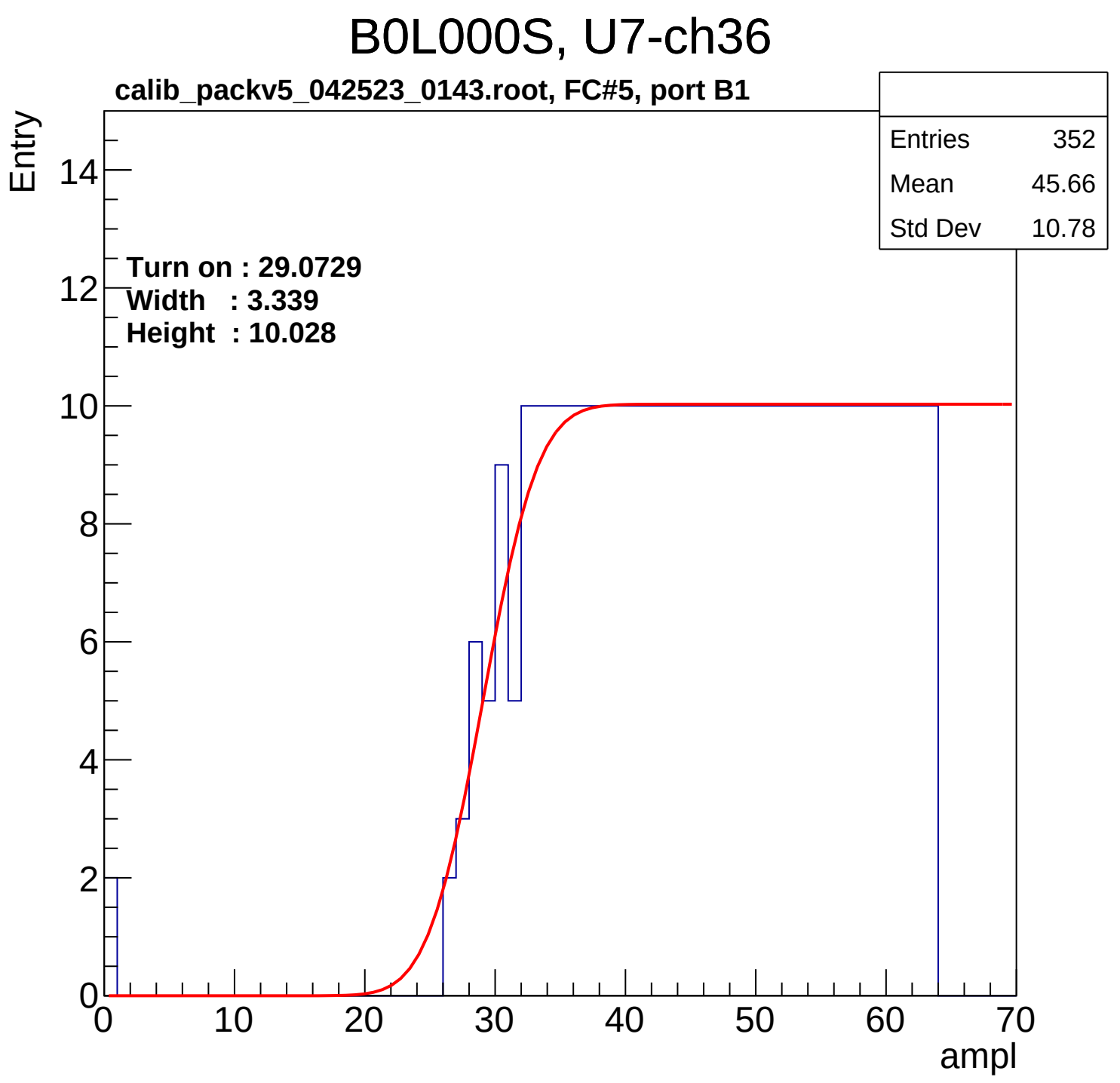
B0L000S, U7-ch36
calib_packv5_042523_0143.root, FC#5, port B1
Entries 352
Mean 45.66
Std Dev 10.78
Turn on : 29.0729
Width : 3.339
Height : 10.028
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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60
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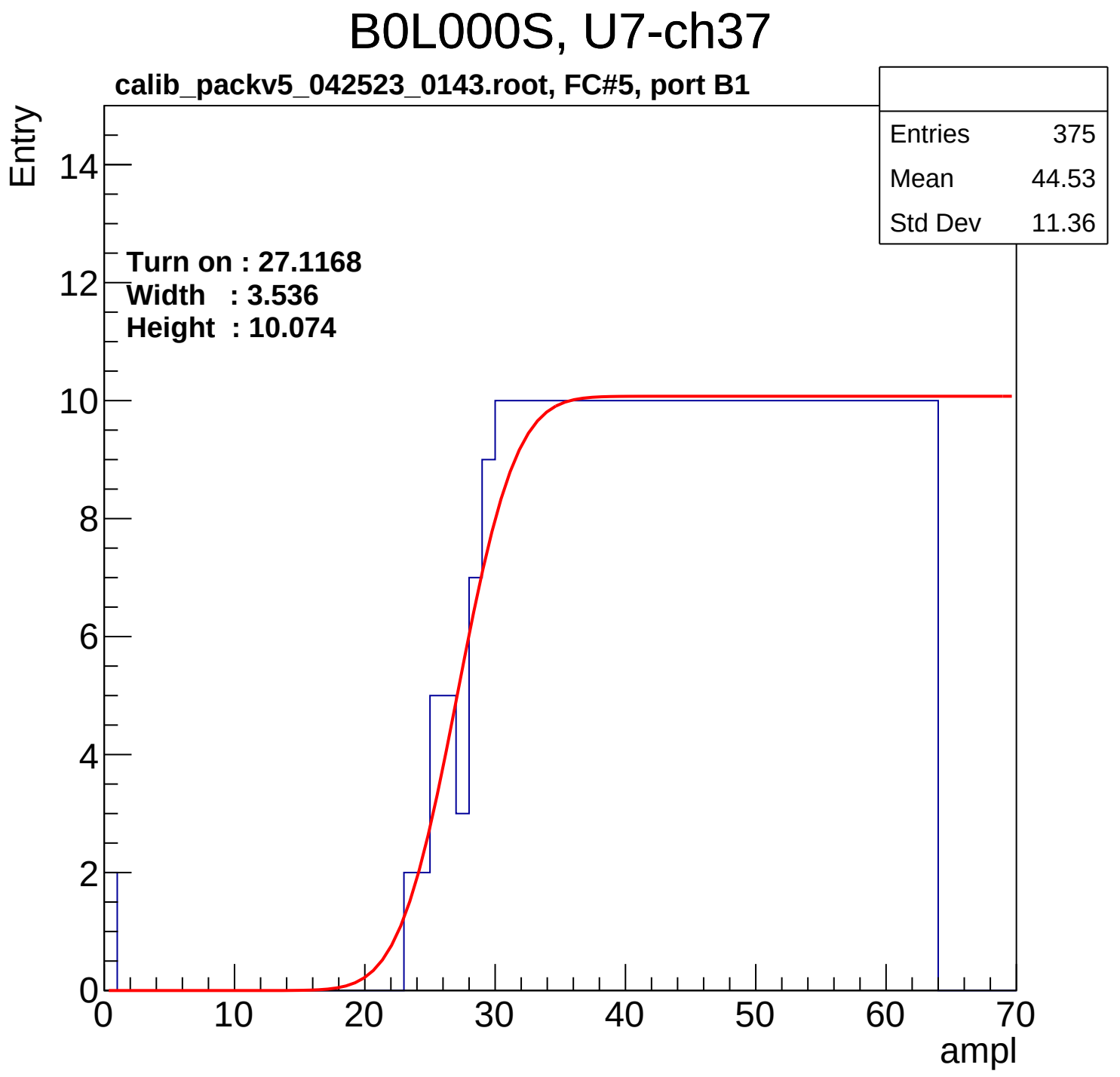
B0L000S, U7-ch37
calib_packv5_042523_0143.root, FC#5, port B1
Entries 375
Mean 44.53
Std Dev 11.36
Turn on : 27.1168
Width : 3.536
Height : 10.074
Entry
ampl
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6
8
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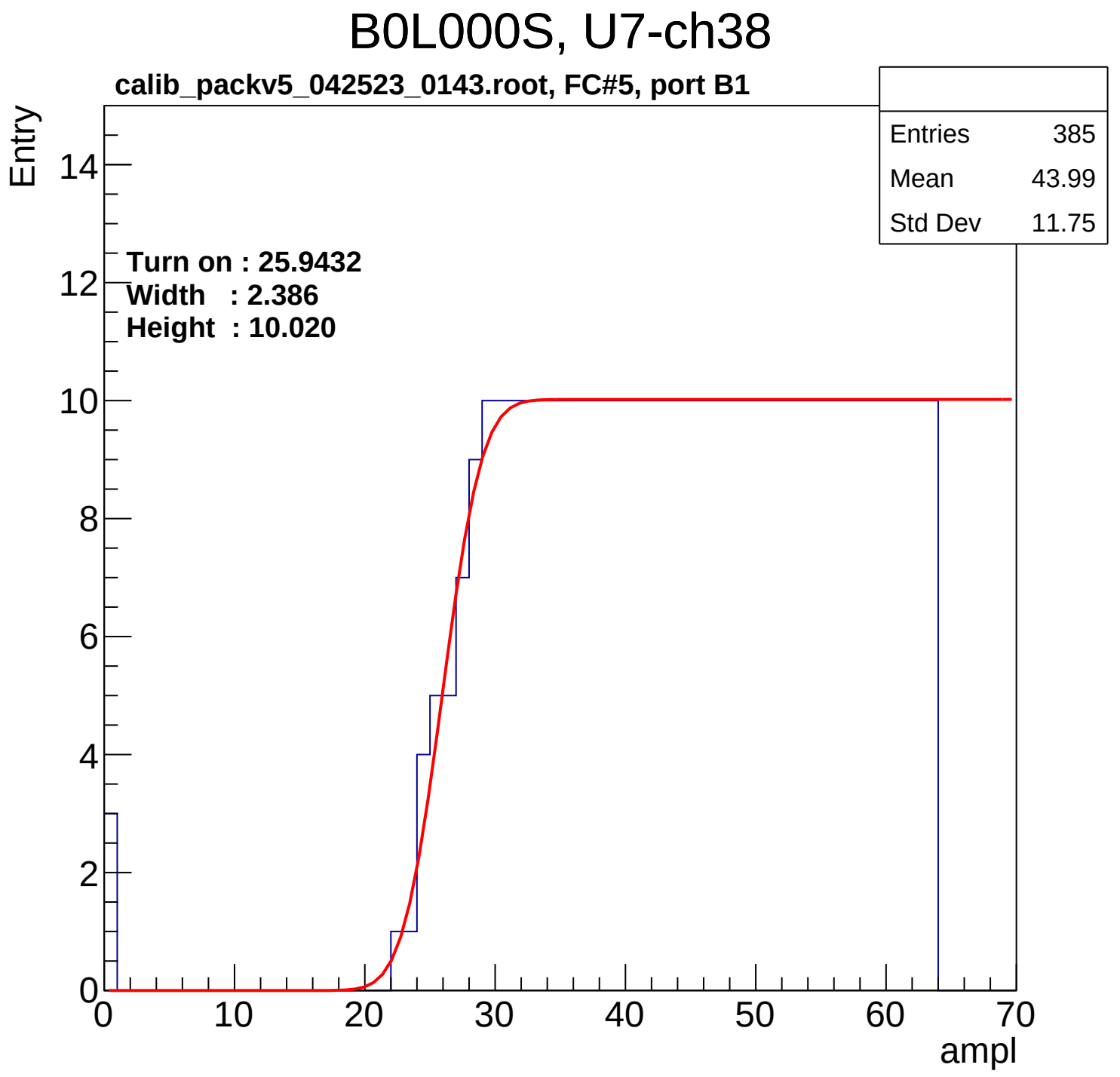
B0L000S, U7-ch38
calib_packv5_042523_0143.root, FC#5, port B1
Entries 385
Mean 43.99
Std Dev 11.75
Turn on : 25.9432
Width : 2.386
Height : 10.020
Entry
ampl
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6
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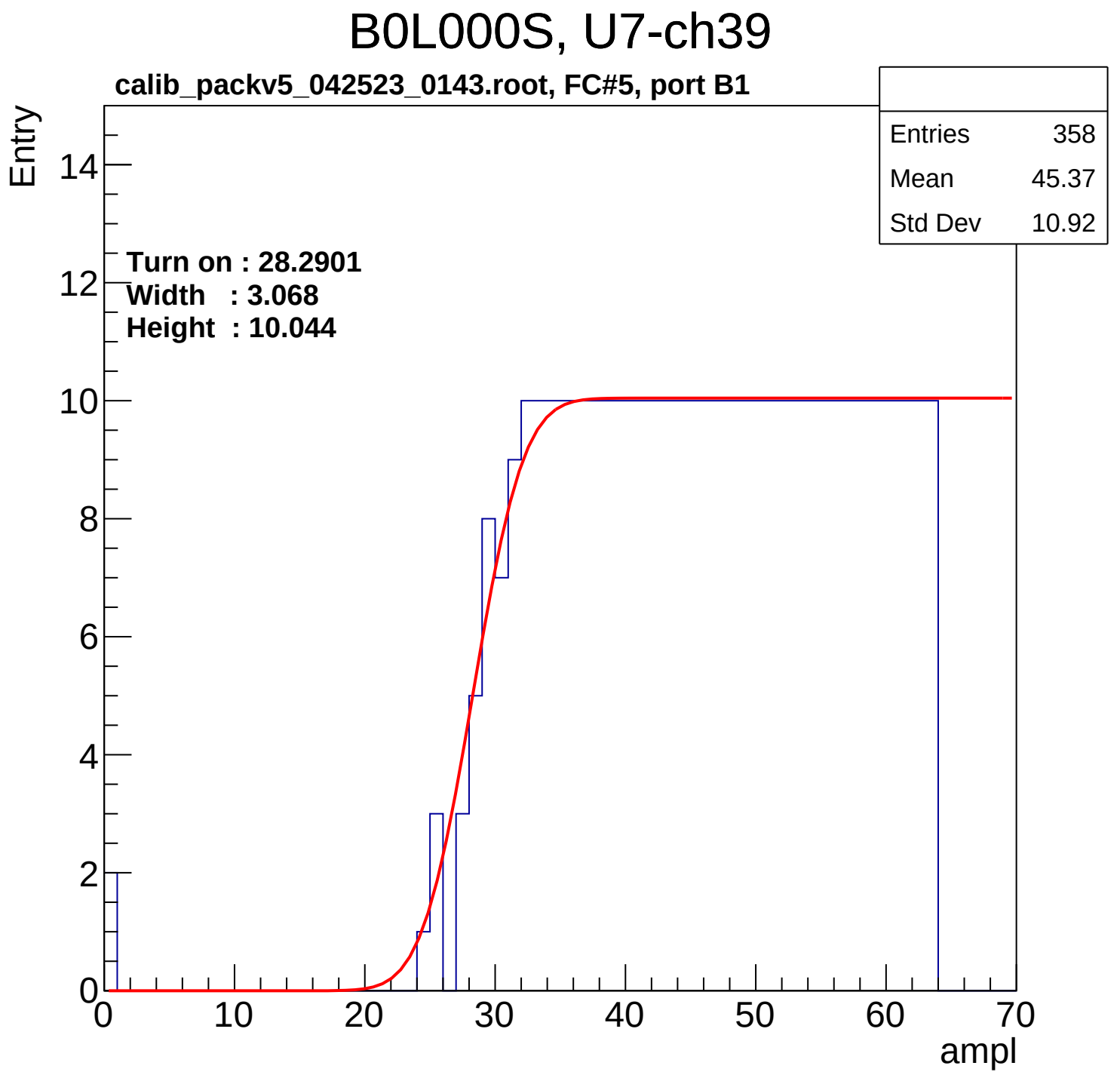
B0L000S, U7-ch39
calib_packv5_042523_0143.root, FC#5, port B1
Entries 358
Mean 45.37
Std Dev 10.92
Turn on : 28.2901
Width : 3.068
Height : 10.044
Entry
ampl
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6
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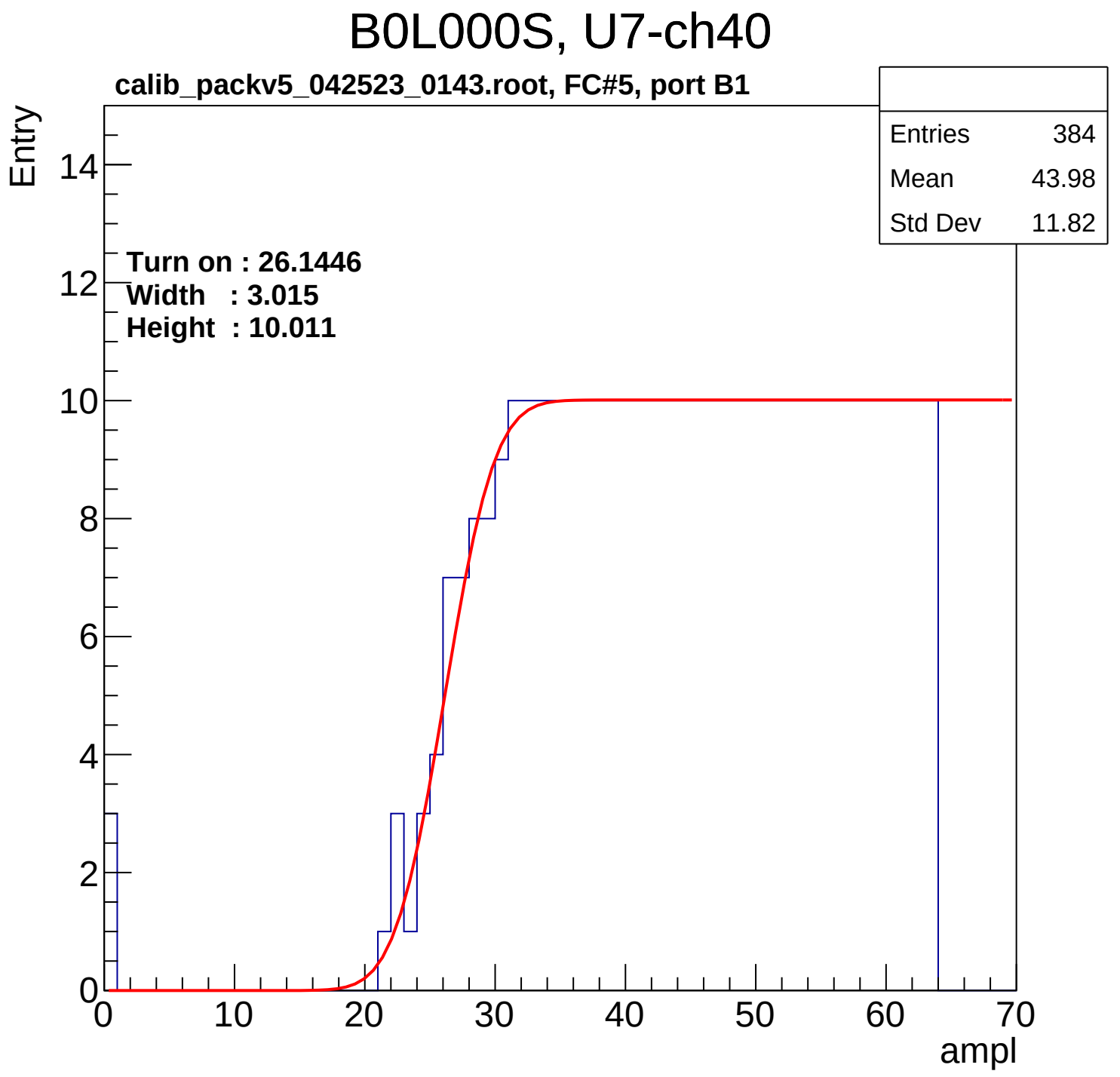
B0L000S, U7-ch40
calib_packv5_042523_0143.root, FC#5, port B1
Entries 384
Mean 43.98
Std Dev 11.82
Turn on : 26.1446
Width : 3.015
Height : 10.011
Entry
ampl
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6
8
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12
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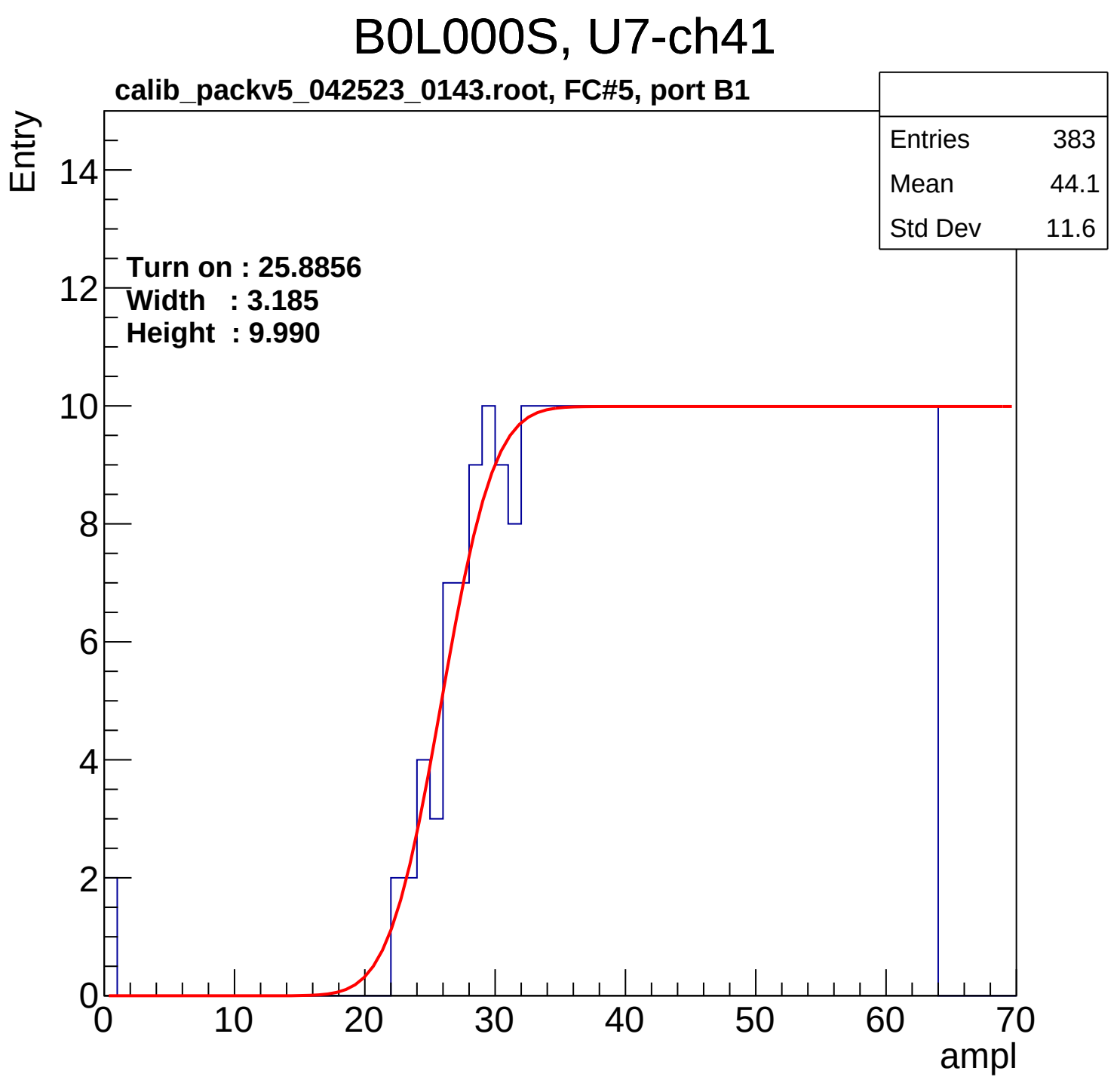
B0L000S, U7-ch41
calib_packv5_042523_0143.root, FC#5, port B1
Entries 383
Mean 44.1
Std Dev 11.6
Turn on : 25.8856
Width : 3.185
Height : 9.990
Entry
ampl
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6
8
10
12
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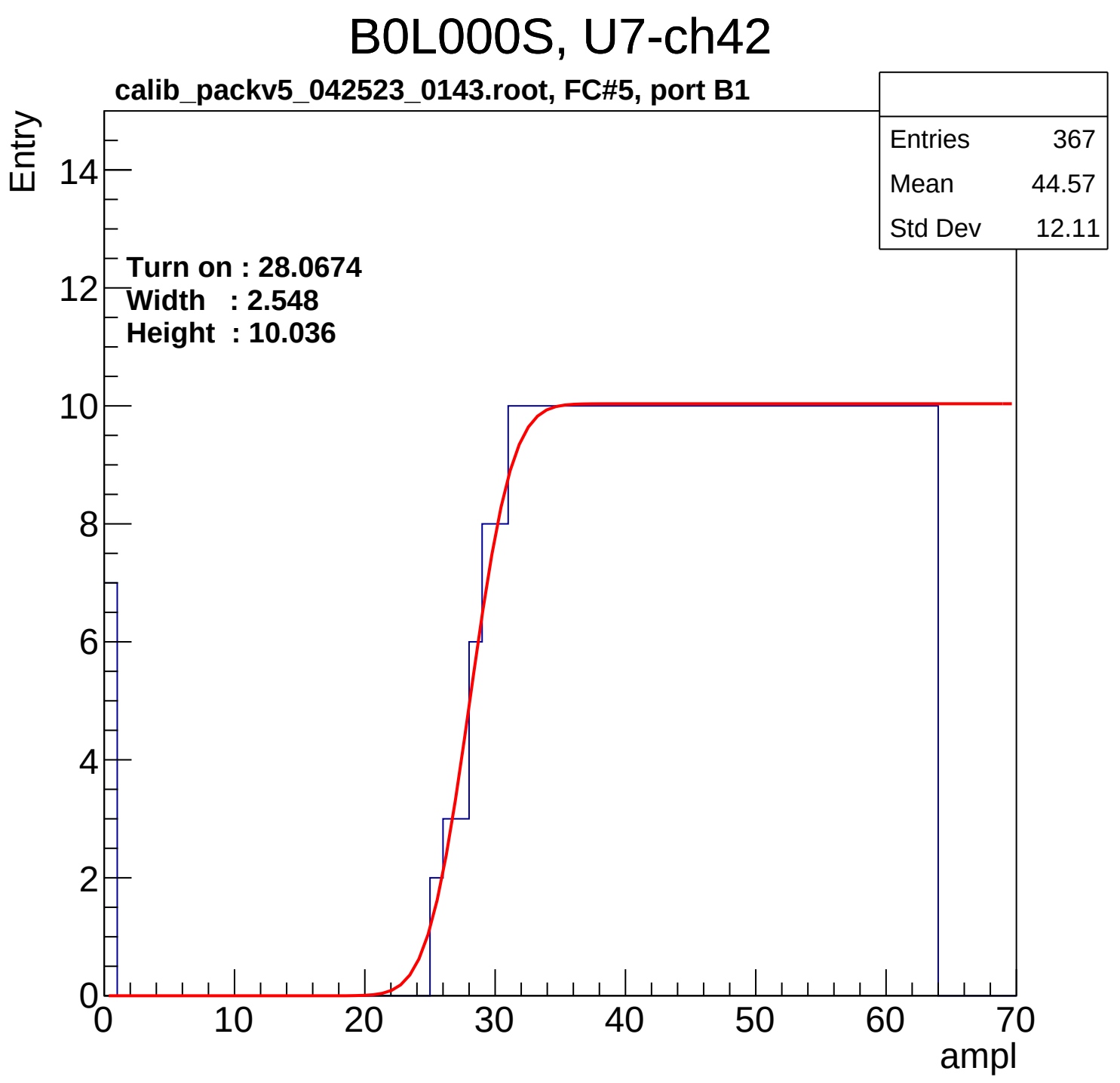
B0L000S, U7-ch42
calib_packv5_042523_0143.root, FC#5, port B1
Entries 367
Mean 44.57
Std Dev 12.11
Turn on : 28.0674
Width : 2.548
Height : 10.036
Entry
ampl
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4
6
8
10
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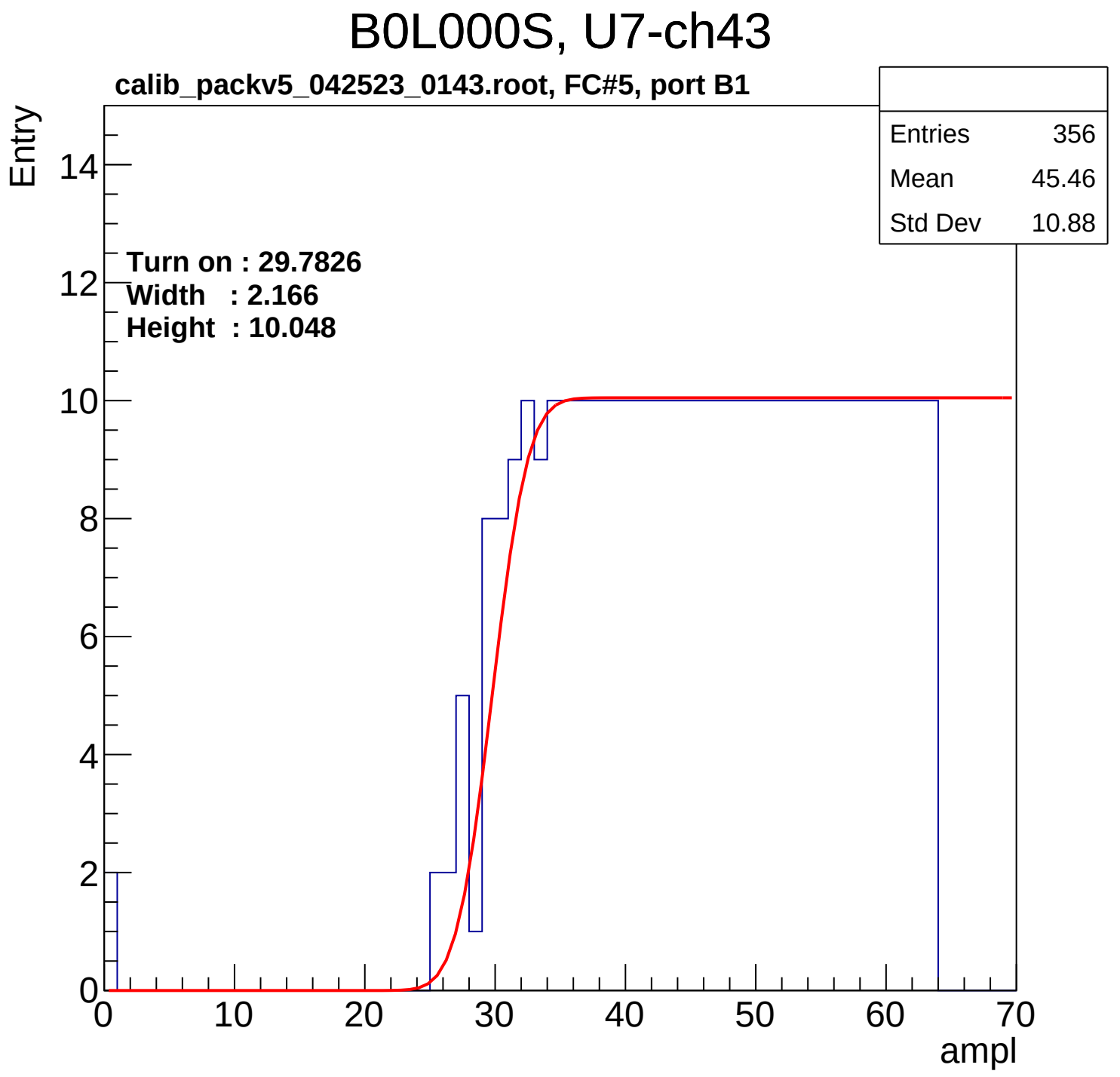
B0L000S, U7-ch43
calib_packv5_042523_0143.root, FC#5, port B1
Entries 356
Mean 45.46
Std Dev 10.88
Turn on : 29.7826
Width : 2.166
Height : 10.048
Entry
ampl
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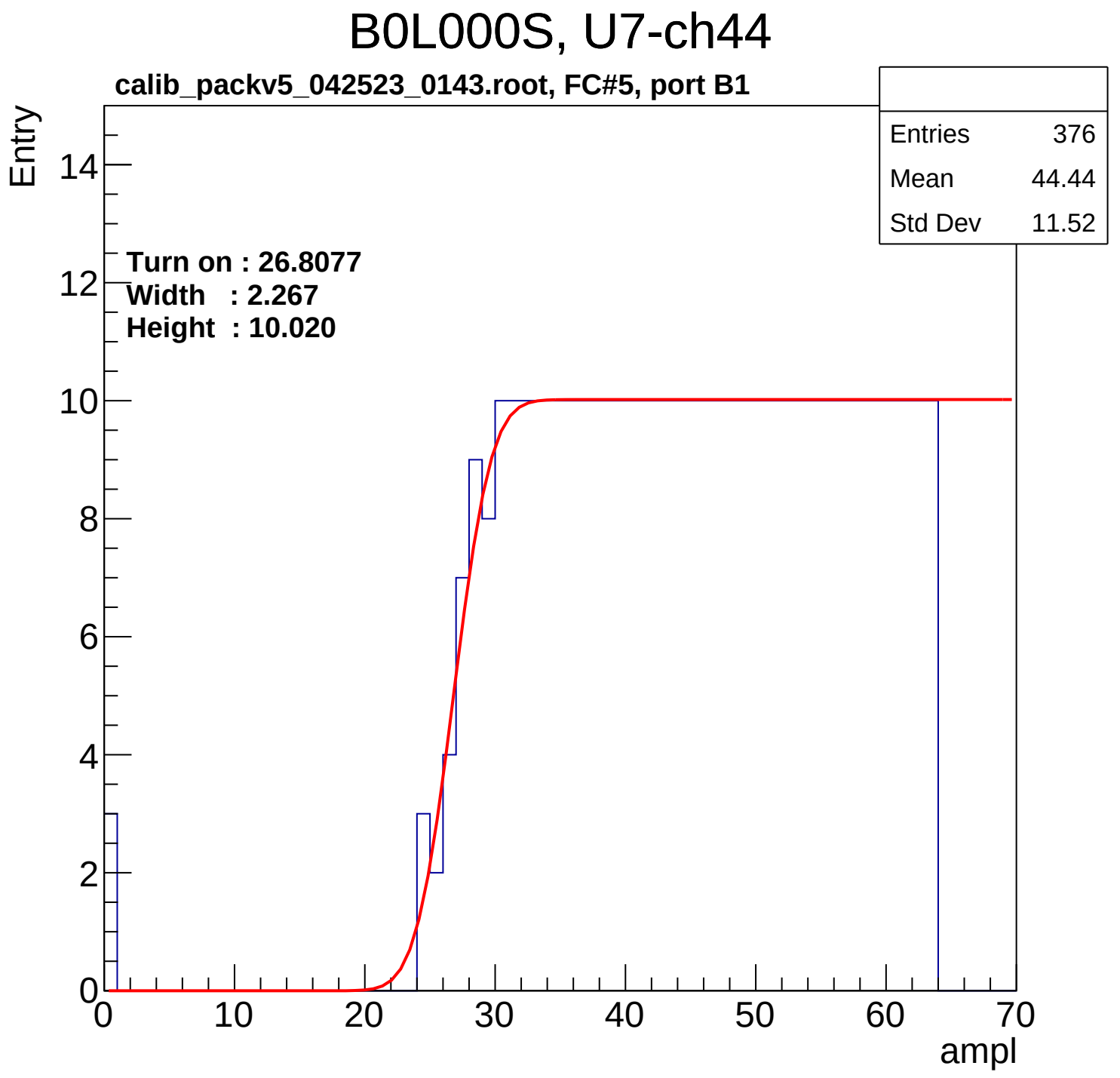
B0L000S, U7-ch44
calib_packv5_042523_0143.root, FC#5, port B1
Entries 376
Mean 44.44
Std Dev 11.52
Turn on : 26.8077
Width : 2.267
Height : 10.020
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ampl
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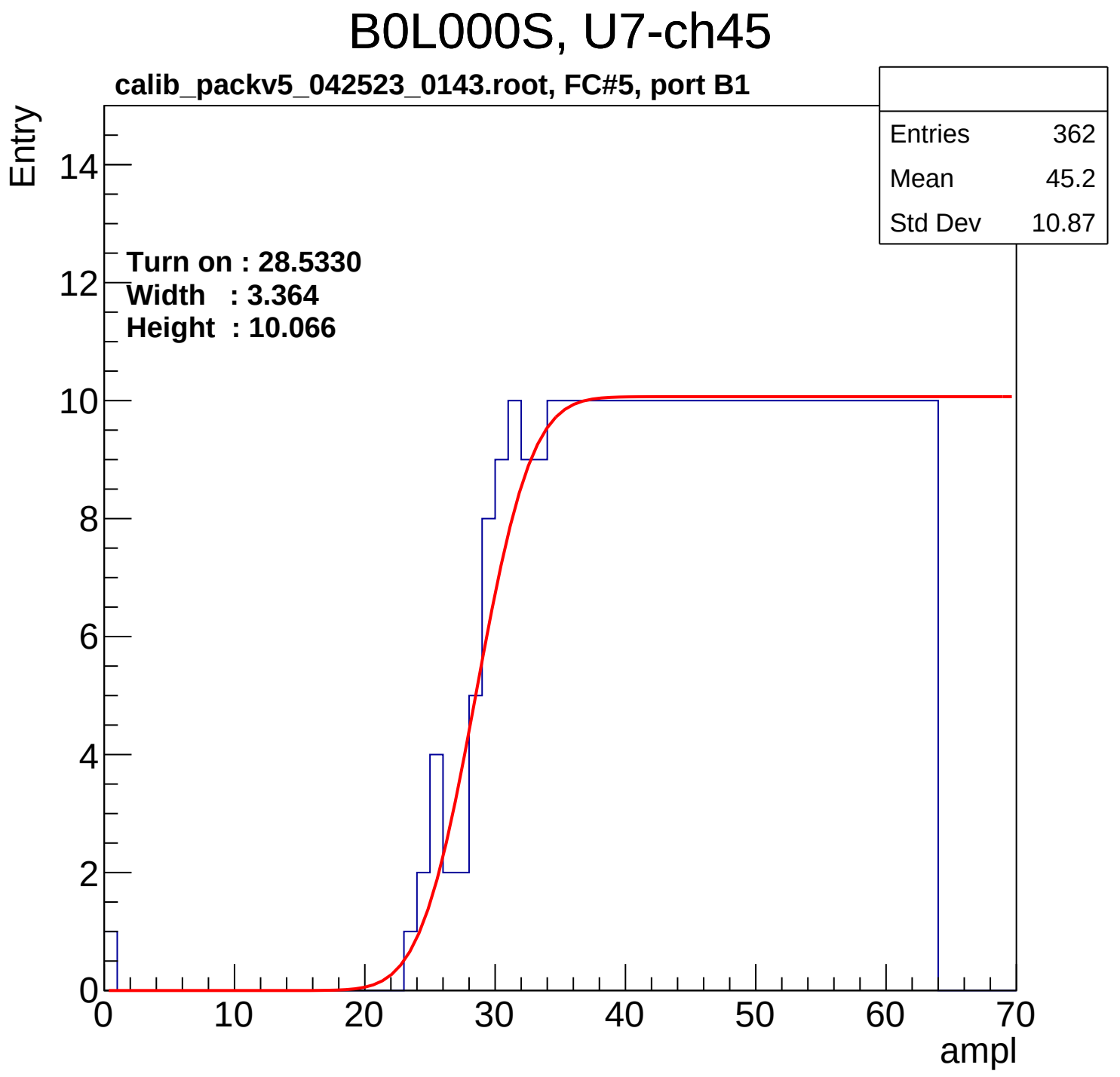
B0L000S, U7-ch45
calib_packv5_042523_0143.root, FC#5, port B1
Entries 362
Mean 45.2
Std Dev 10.87
Turn on : 28.5330
Width : 3.364
Height : 10.066
Entry
ampl
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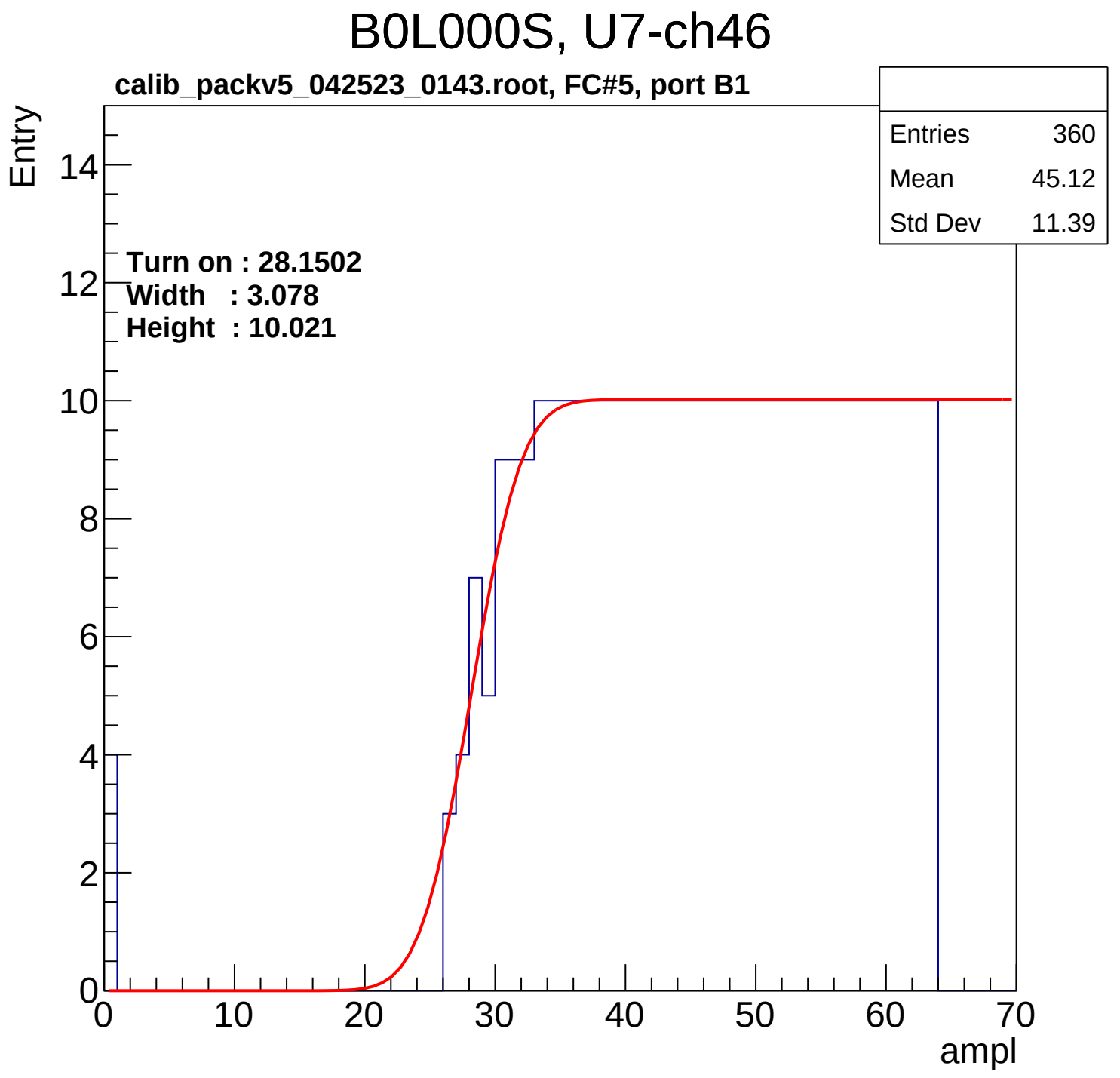
B0L000S, U7-ch46
calib_packv5_042523_0143.root, FC#5, port B1
Entries 360
Mean 45.12
Std Dev 11.39
Turn on : 28.1502
Width : 3.078
Height : 10.021
Entry
ampl
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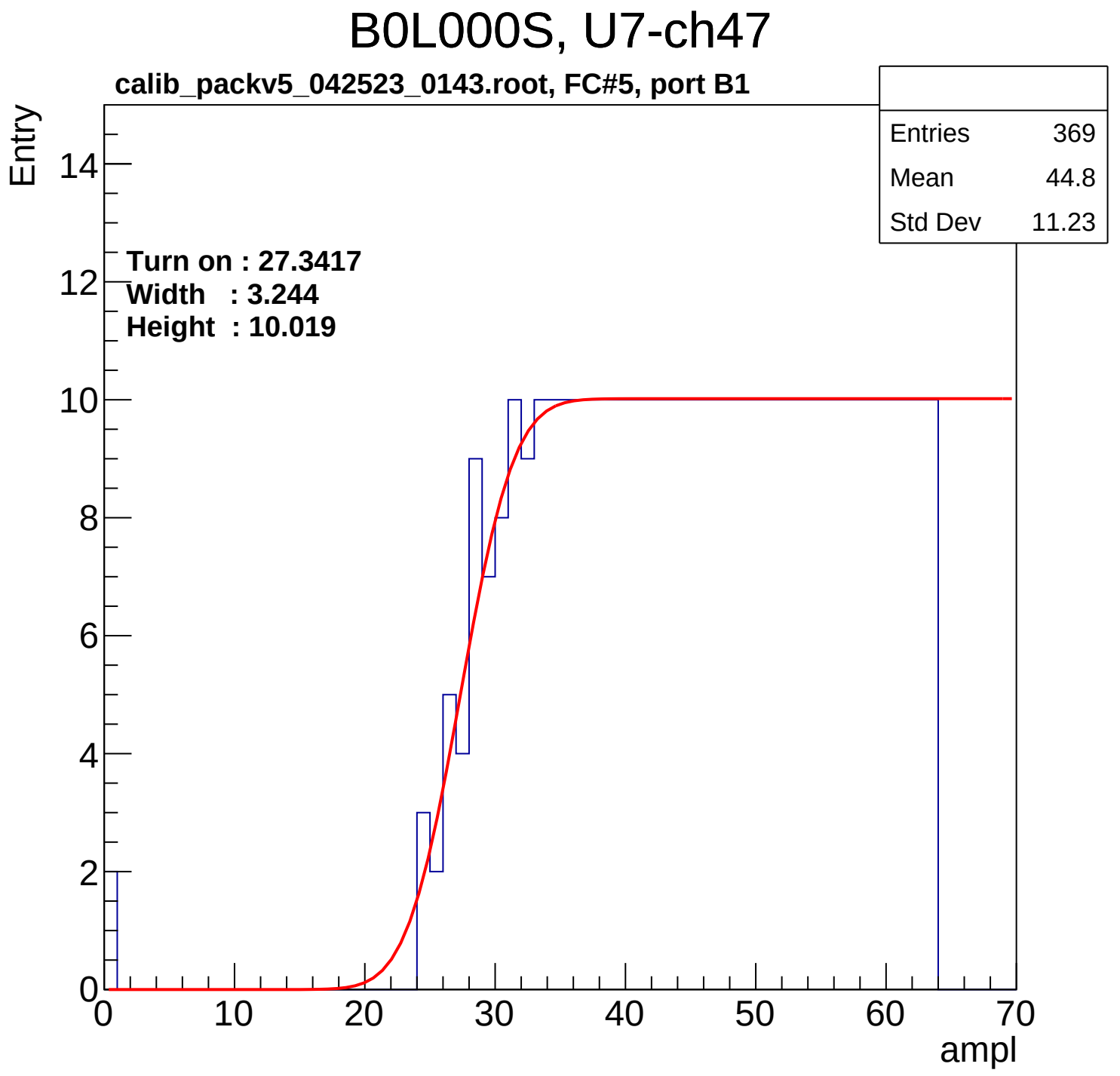
B0L000S, U7-ch47
calib_packv5_042523_0143.root, FC#5, port B1
Entries 369
Mean 44.8
Std Dev 11.23
Turn on : 27.3417
Width : 3.244
Height : 10.019
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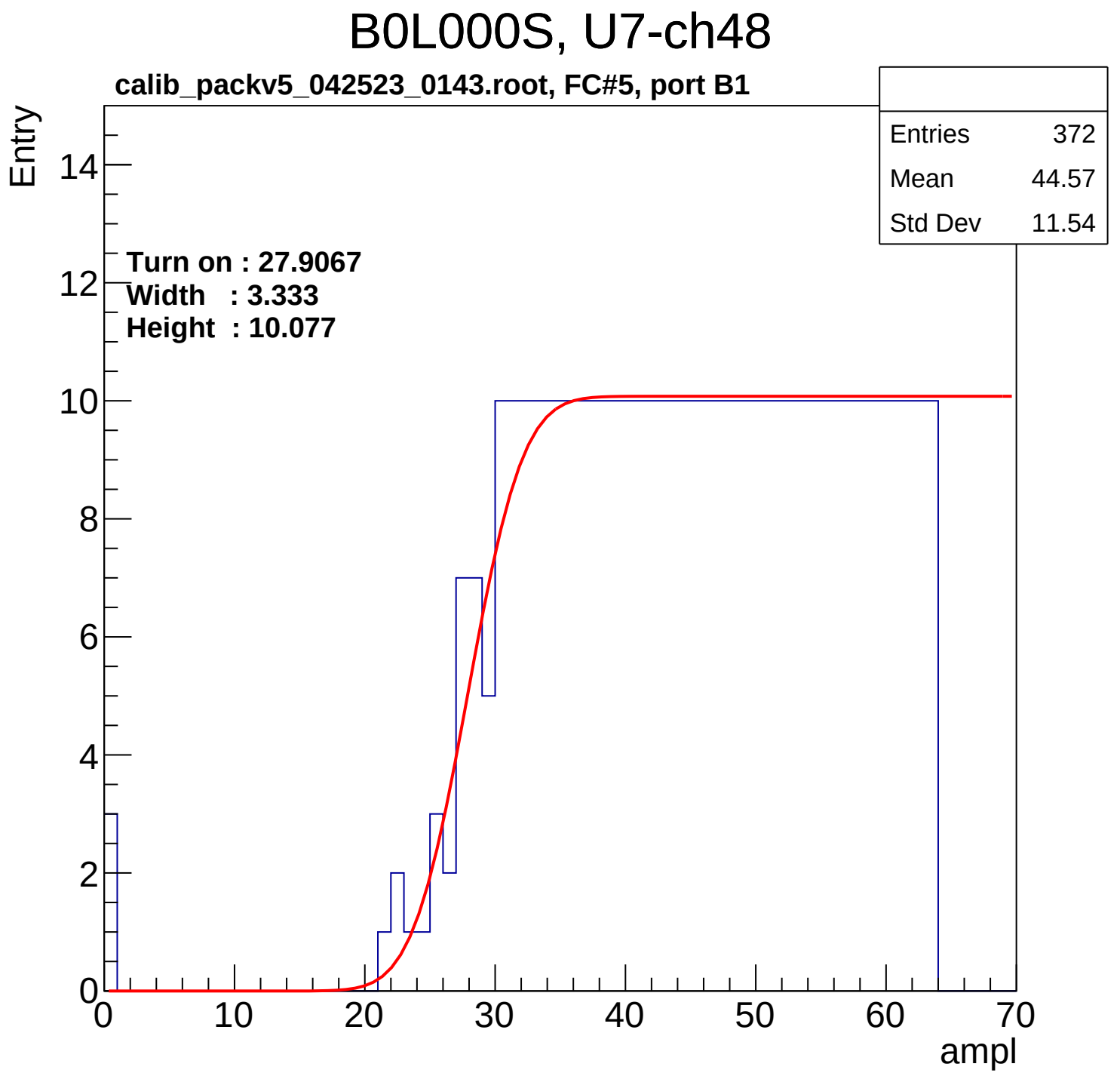
B0L000S, U7-ch48
calib_packv5_042523_0143.root, FC#5, port B1
Entries 372
Mean 44.57
Std Dev 11.54
Turn on : 27.9067
Width : 3.333
Height : 10.077
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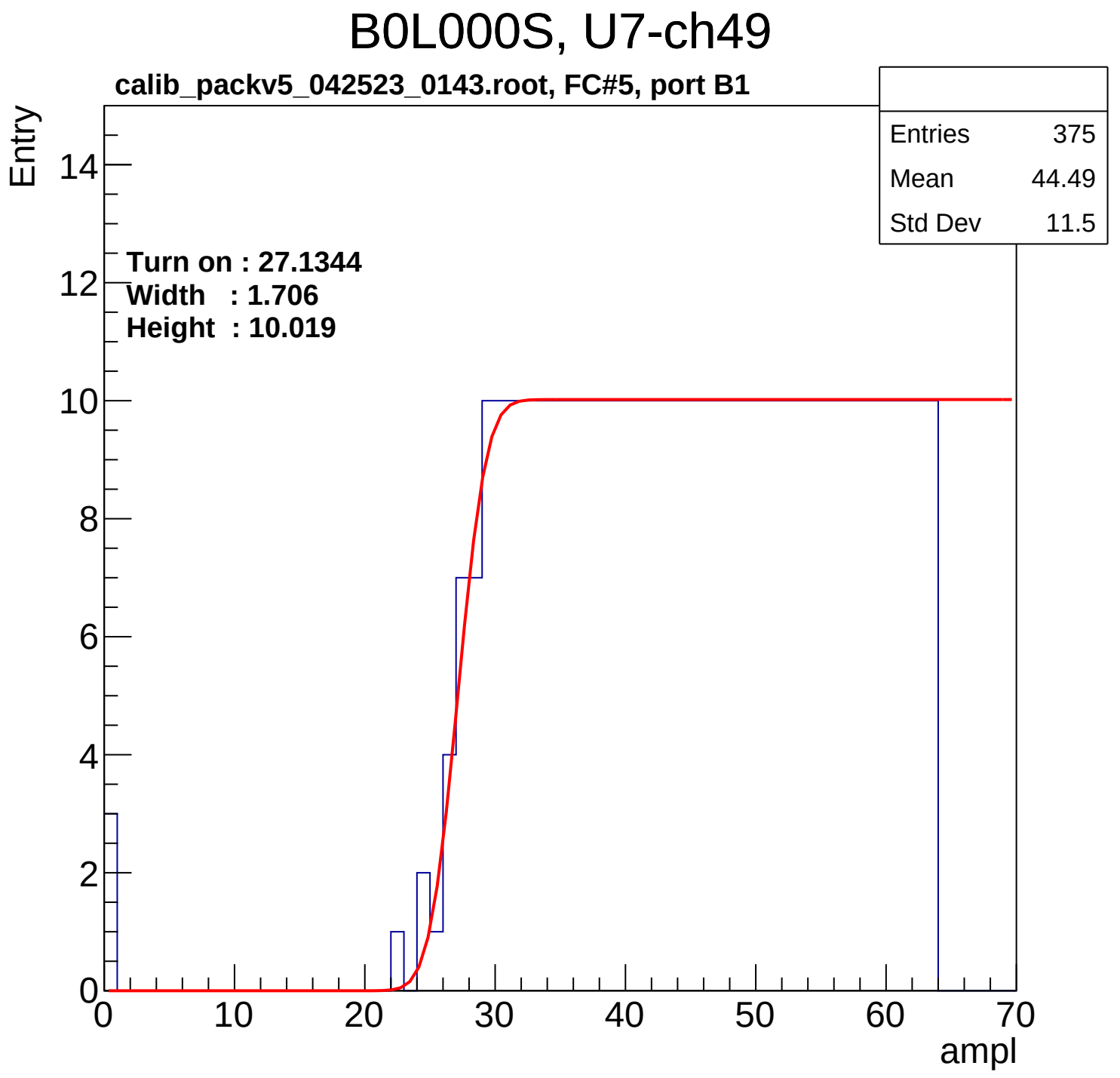
B0L000S, U7-ch49
calib_packv5_042523_0143.root, FC#5, port B1
Entries 375
Mean 44.49
Std Dev 11.5
Turn on : 27.1344
Width : 1.706
Height : 10.019
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ampl
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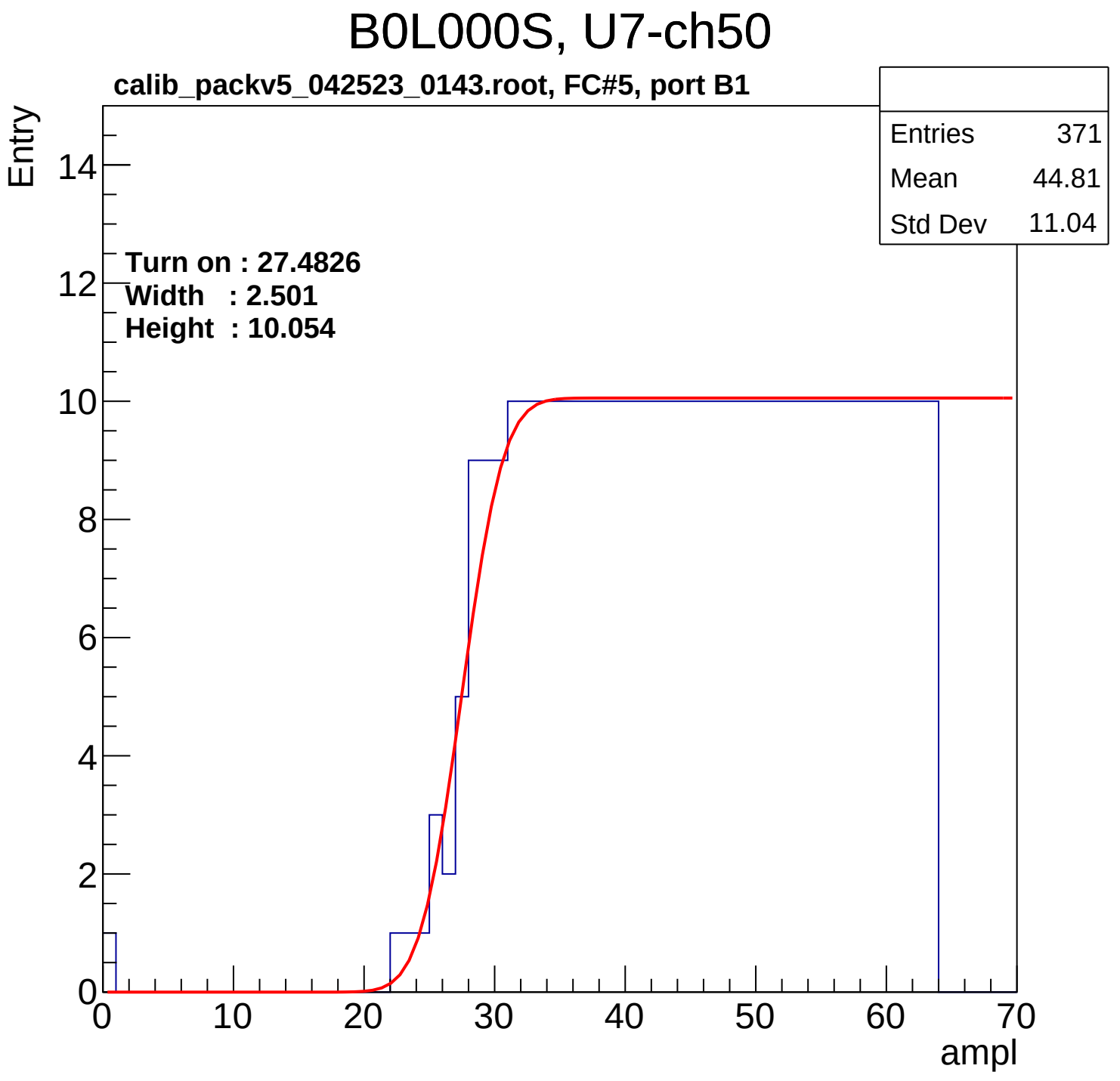
B0L000S, U7-ch50
calib_packv5_042523_0143.root, FC#5, port B1
Entries 371
Mean 44.81
Std Dev 11.04
Turn on : 27.4826
Width : 2.501
Height : 10.054
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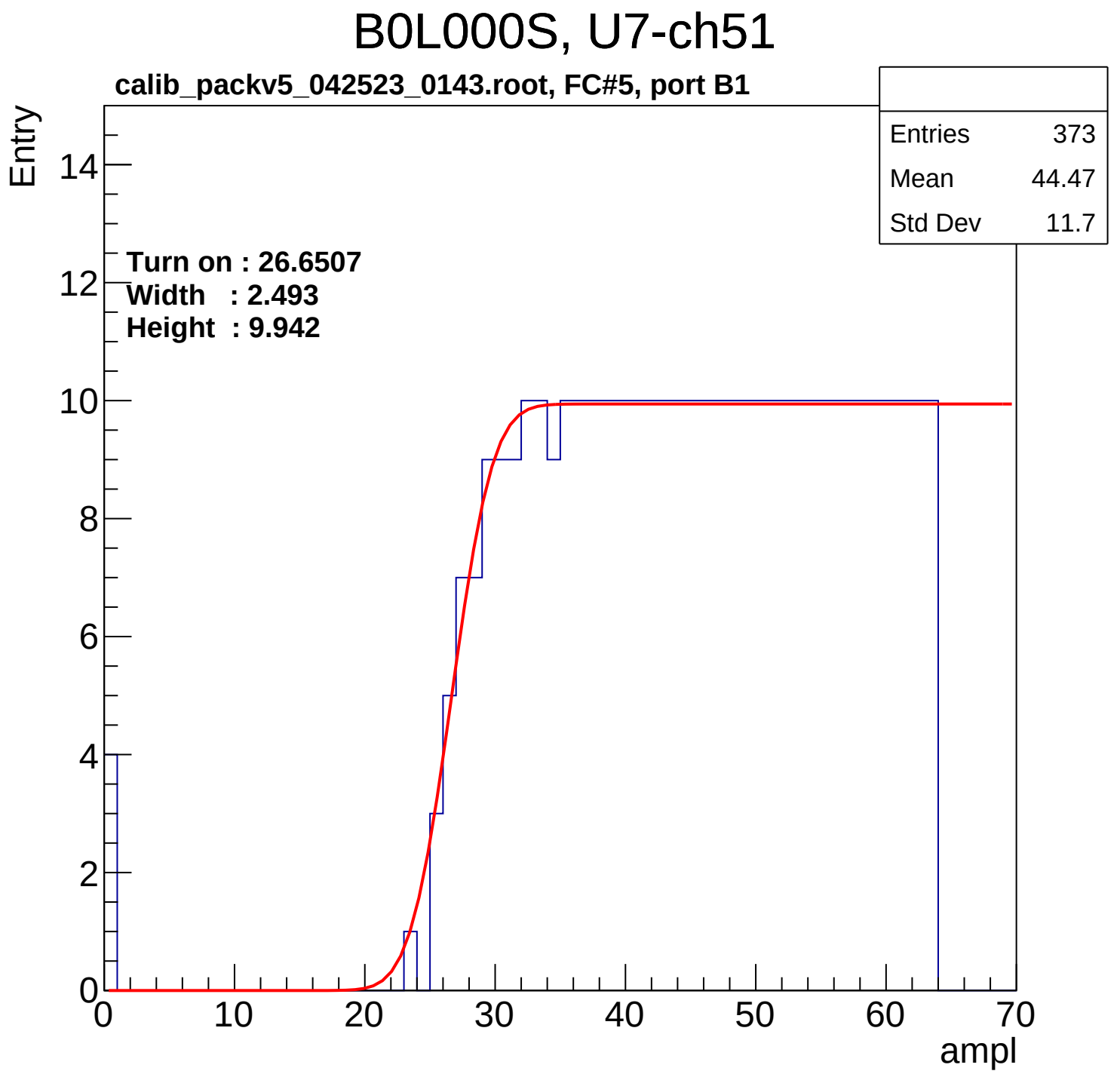
B0L000S, U7-ch51
calib_packv5_042523_0143.root, FC#5, port B1
Entries 373
Mean 44.47
Std Dev 11.7
Turn on : 26.6507
Width : 2.493
Height : 9.942
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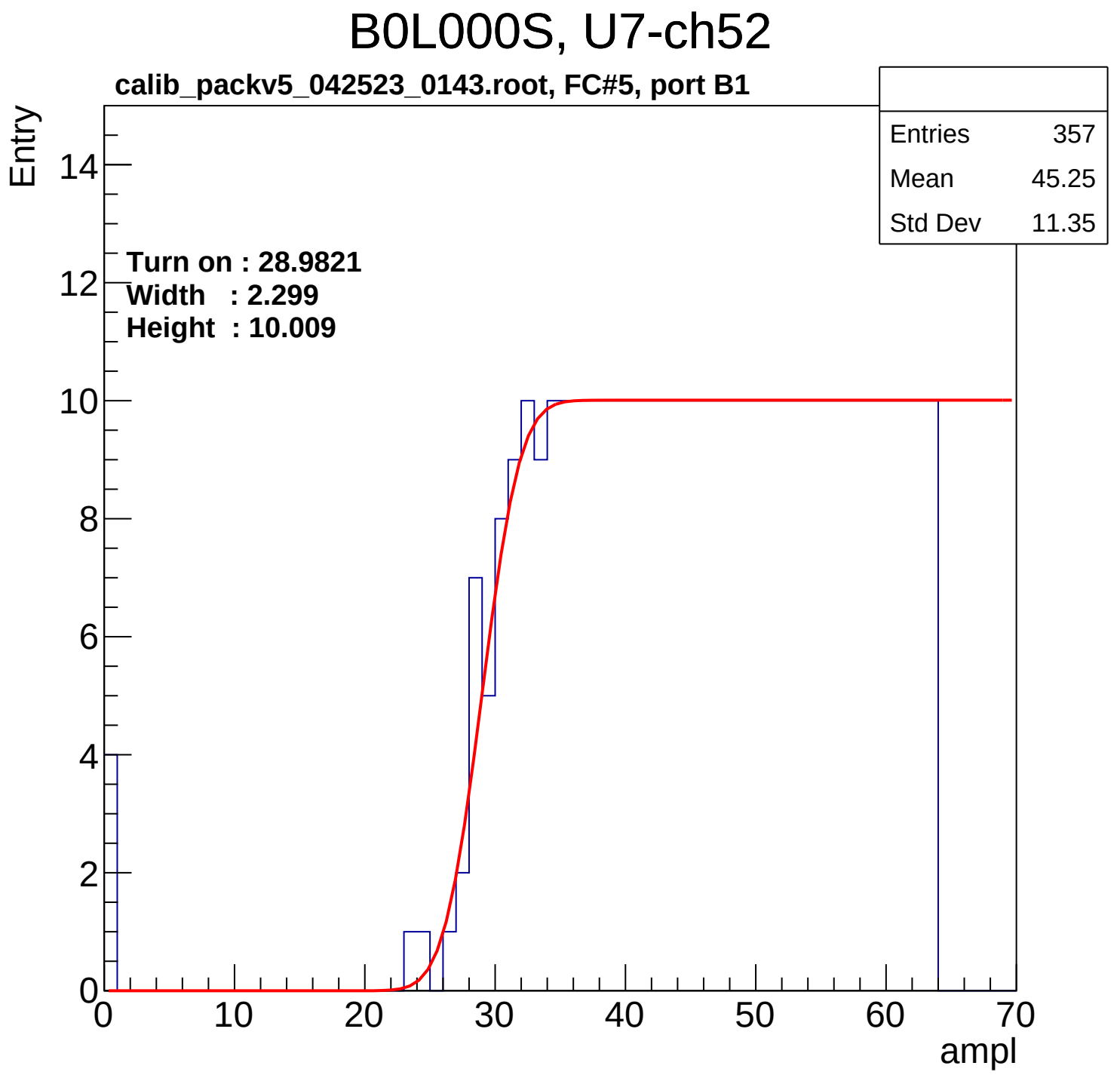
B0L000S, U7-ch52
calib_packv5_042523_0143.root, FC#5, port B1
Entries 357
Mean 45.25
Std Dev 11.35
Turn on : 28.9821
Width : 2.299
Height : 10.009
Entry
ampl
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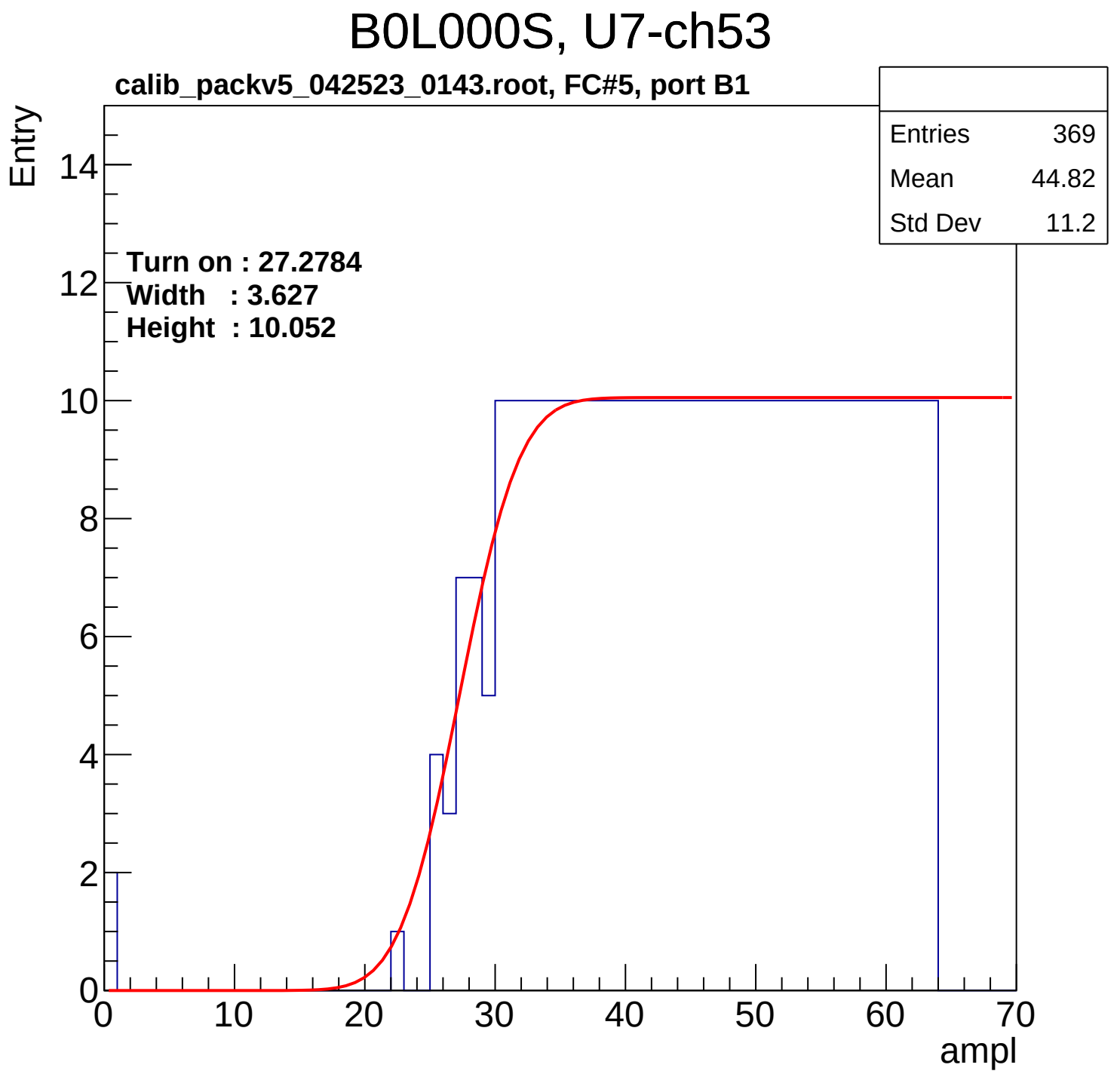
B0L000S, U7-ch53
calib_packv5_042523_0143.root, FC#5, port B1
Entries 369
Mean 44.82
Std Dev 11.2
Turn on : 27.2784
Width : 3.627
Height : 10.052
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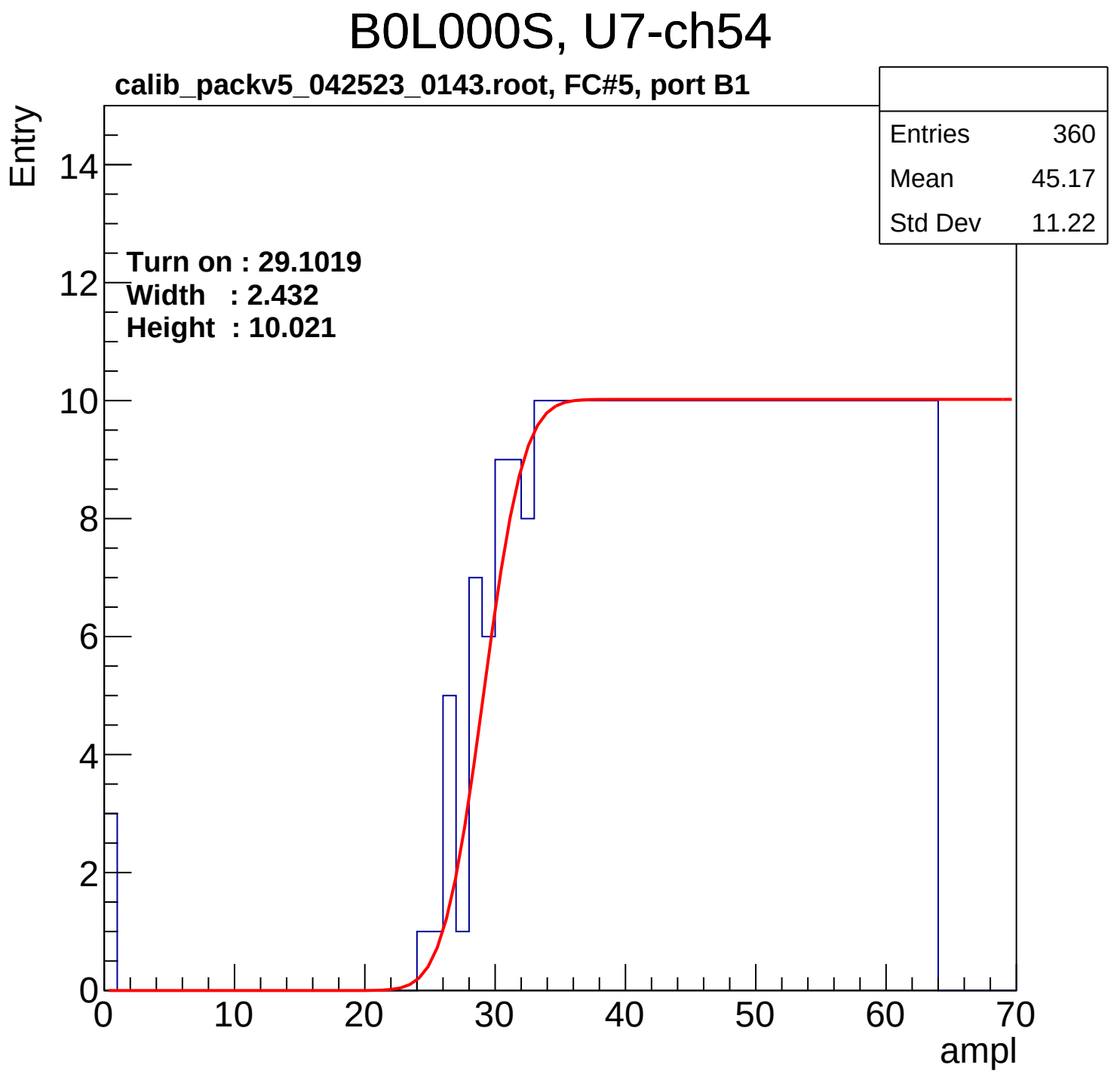
B0L000S, U7-ch54
calib_packv5_042523_0143.root, FC#5, port B1
Entries 360
Mean 45.17
Std Dev 11.22
Turn on : 29.1019
Width : 2.432
Height : 10.021
Entry
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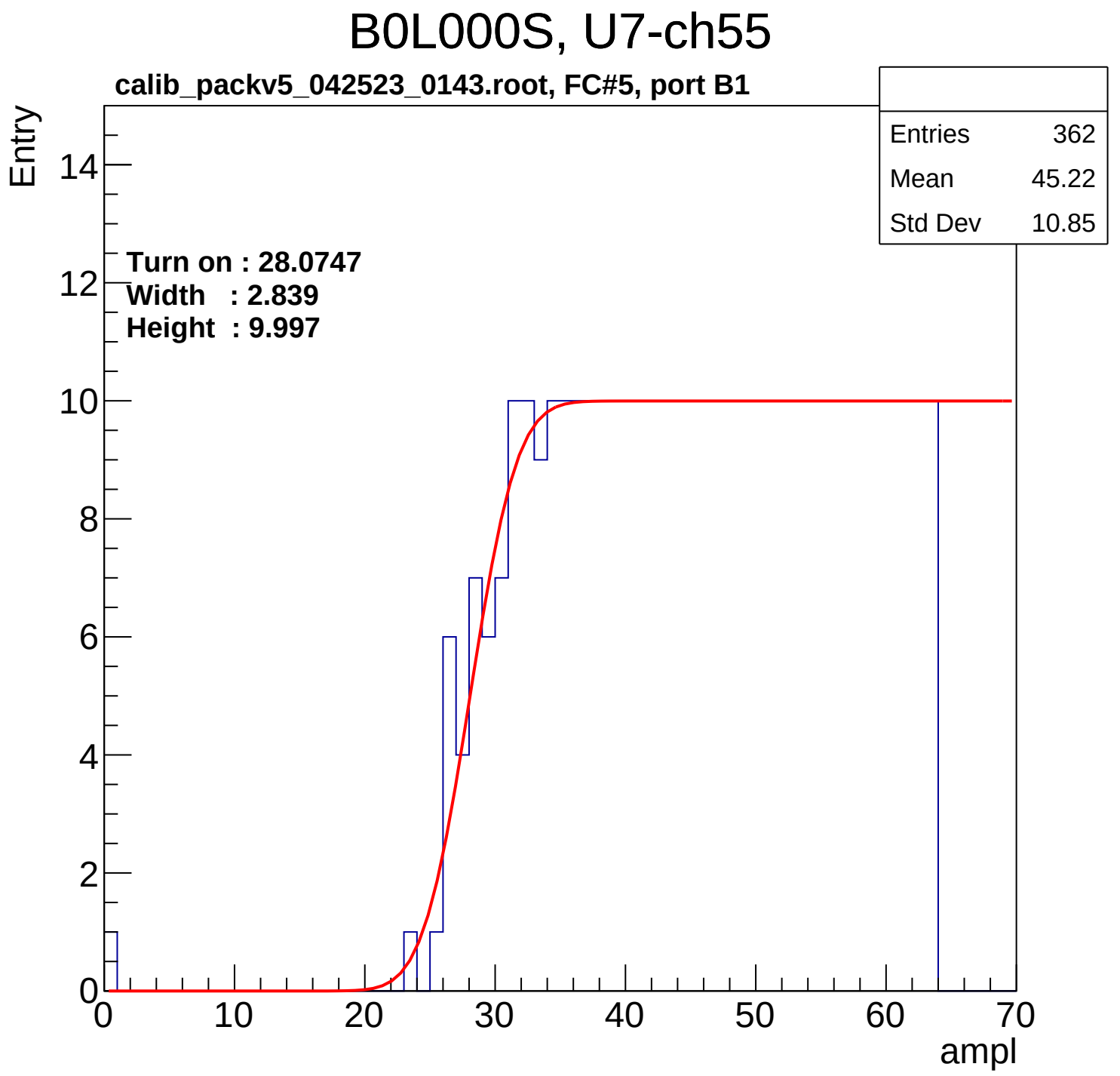
B0L000S, U7-ch55
calib_packv5_042523_0143.root, FC#5, port B1
Entries 362
Mean 45.22
Std Dev 10.85
Turn on : 28.0747
Width : 2.839
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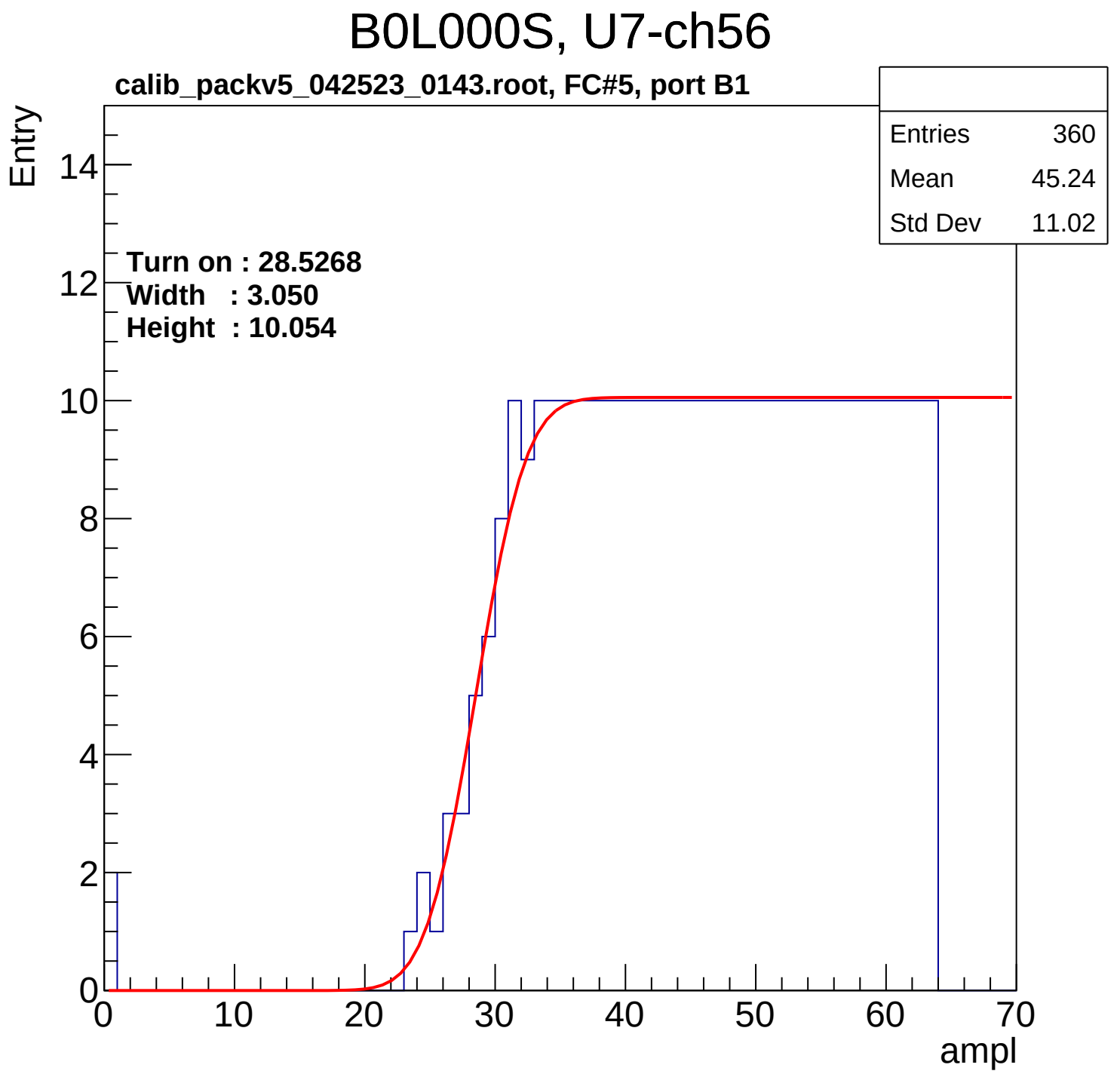
B0L000S, U7-ch56
calib_packv5_042523_0143.root, FC#5, port B1
Entries 360
Mean 45.24
Std Dev 11.02
Turn on : 28.5268
Width : 3.050
Height : 10.054
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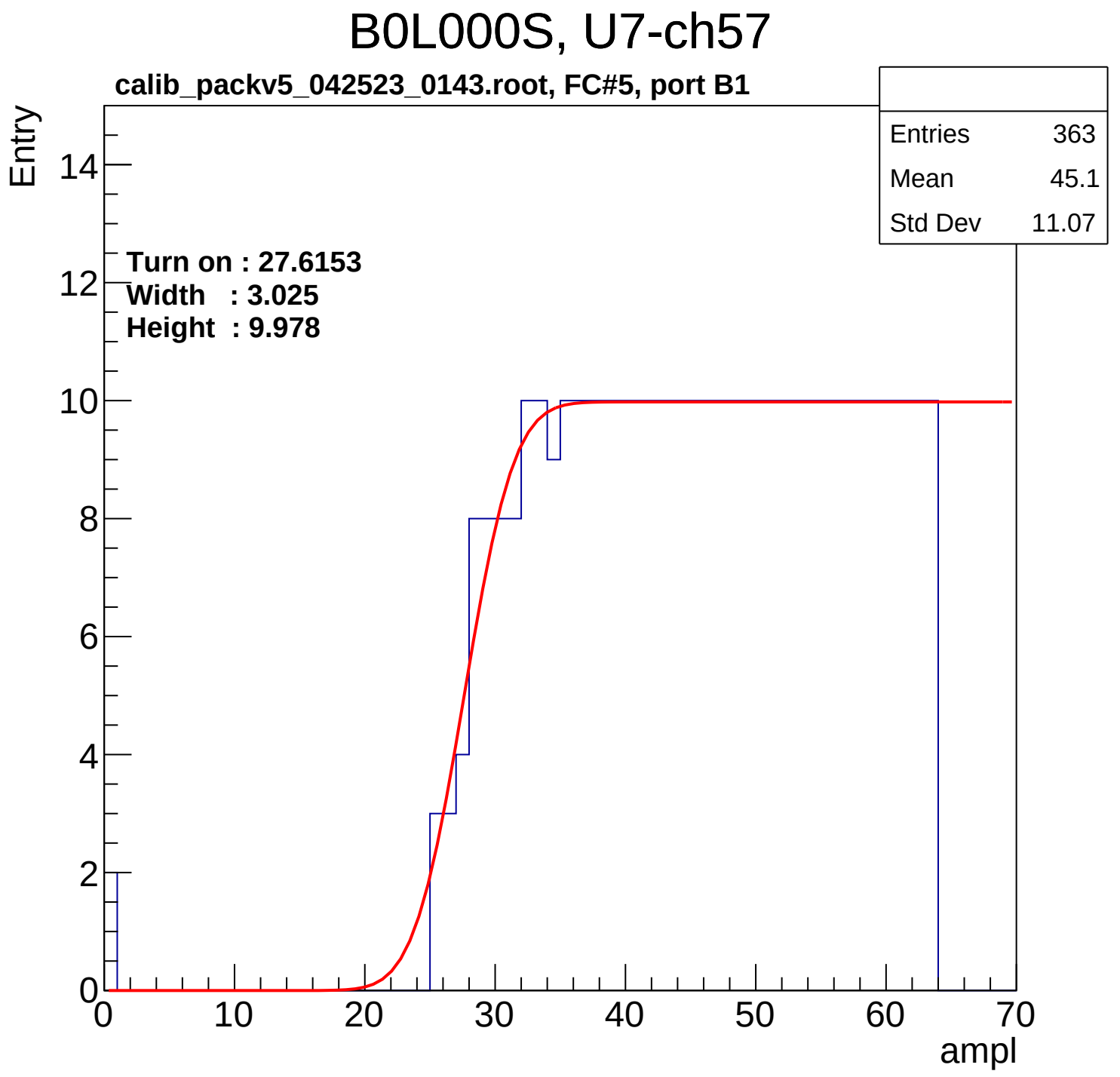
B0L000S, U7-ch57
calib_packv5_042523_0143.root, FC#5, port B1
Entries 363
Mean 45.1
Std Dev 11.07
Turn on : 27.6153
Width : 3.025
Height : 9.978
Entry
ampl
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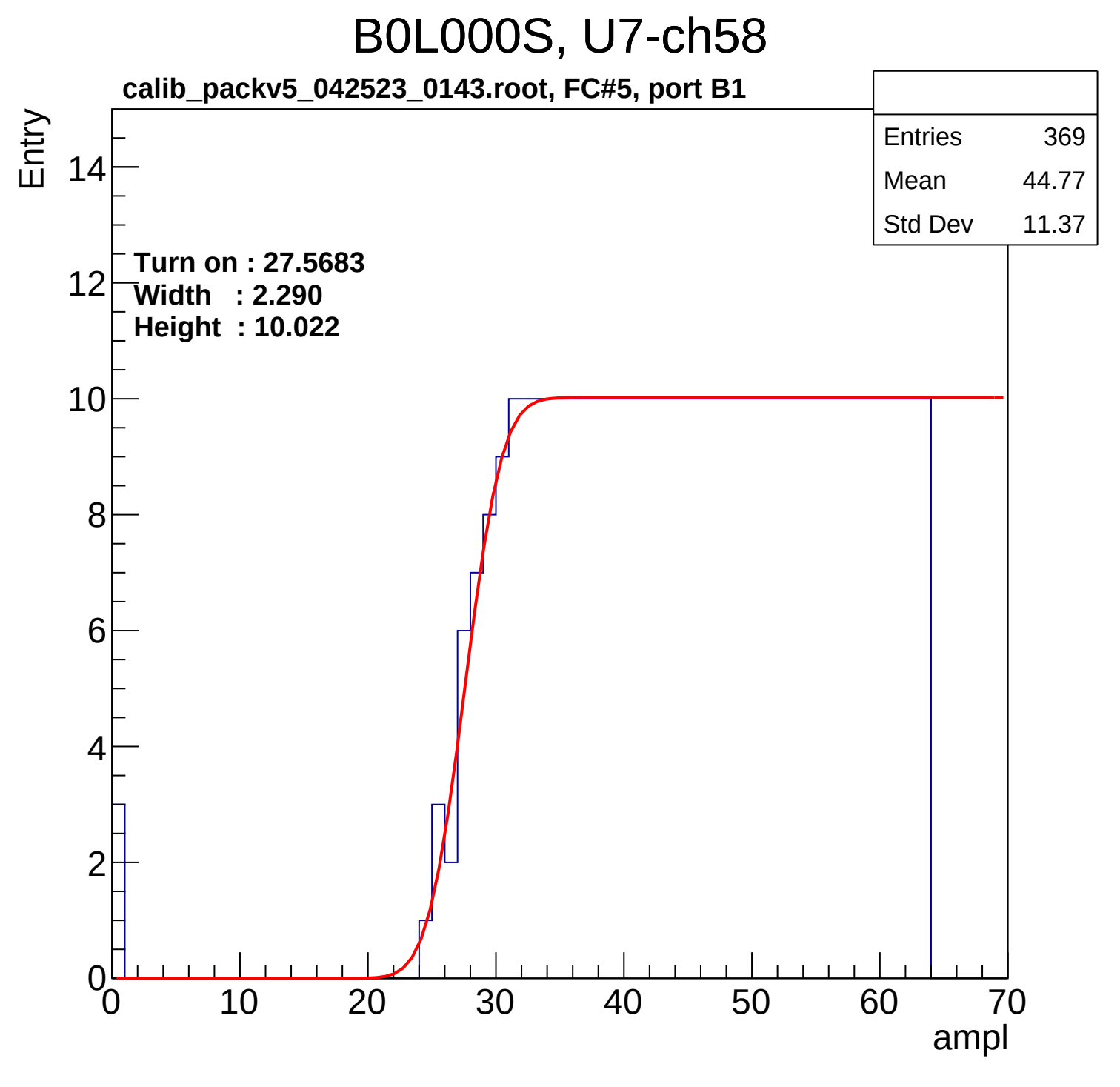
B0L000S, U7-ch58
calib_packv5_042523_0143.root, FC#5, port B1
Entries 369
Mean 44.77
Std Dev 11.37
Turn on : 27.5683
Width : 2.290
Height : 10.022
Entry
ampl
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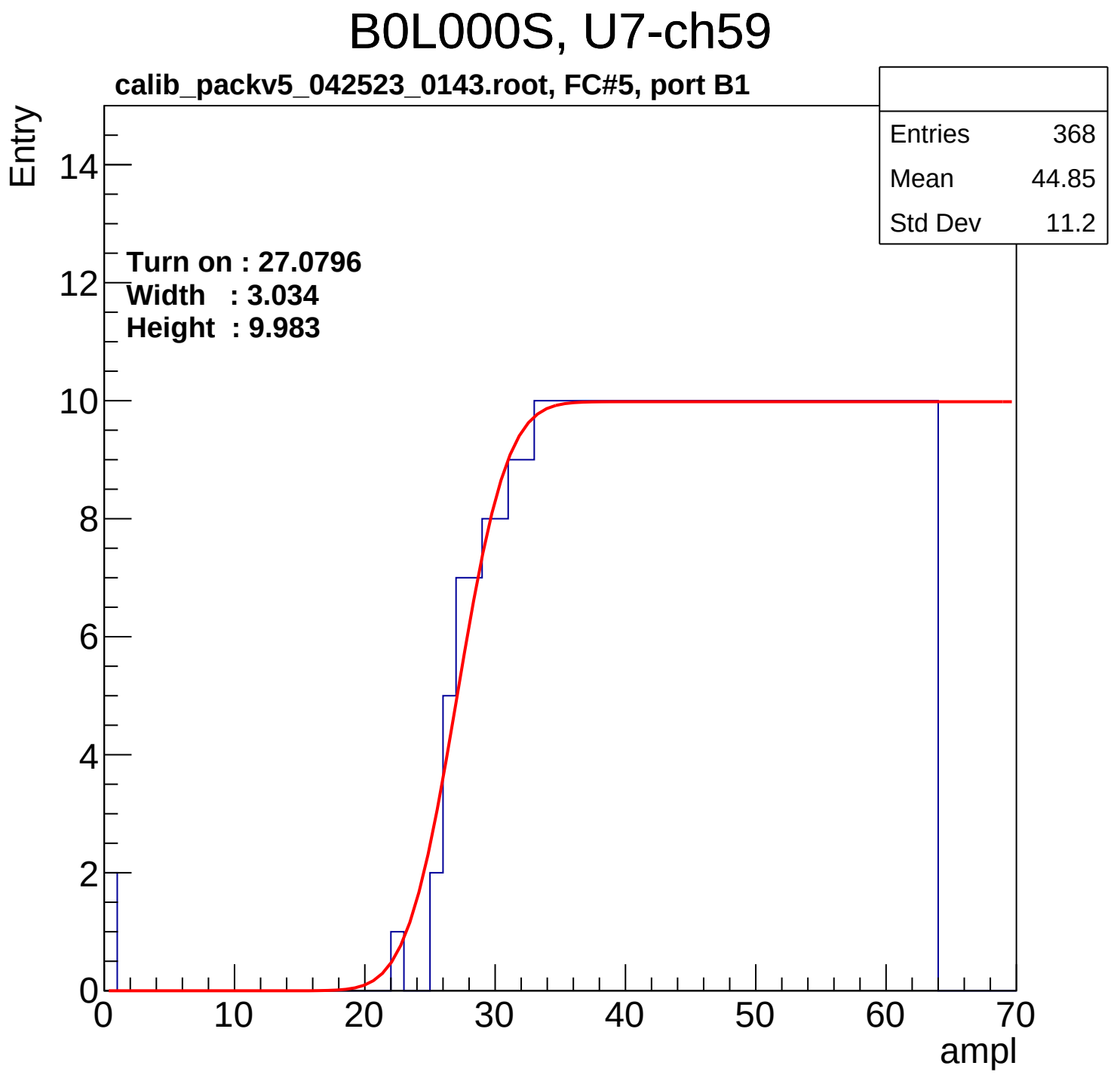
B0L000S, U7-ch59
calib_packv5_042523_0143.root, FC#5, port B1
Entries 368
Mean 44.85
Std Dev 11.2
Turn on : 27.0796
Width : 3.034
Height : 9.983
Entry
ampl
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2
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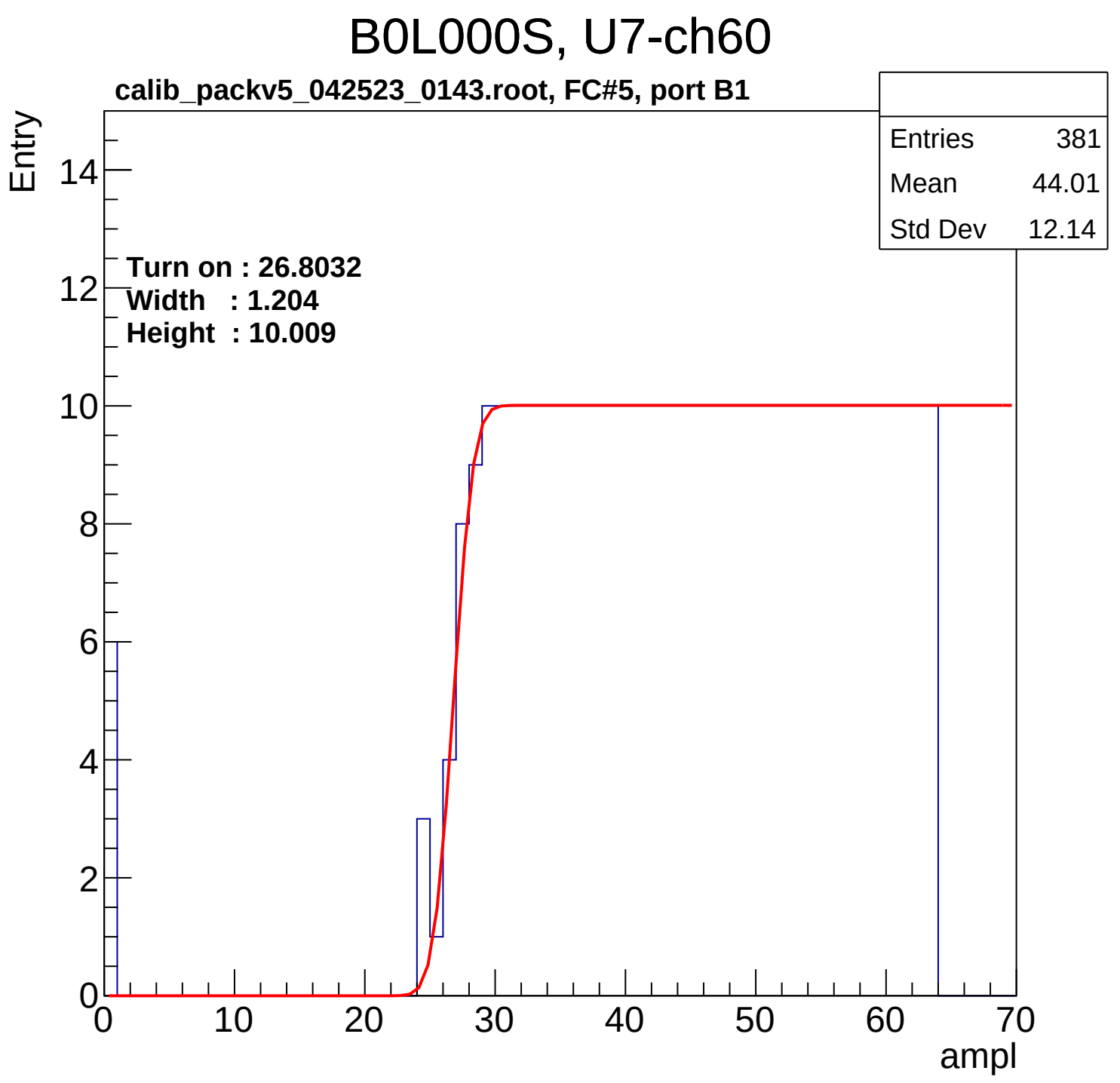
B0L000S, U7-ch60
calib_packv5_042523_0143.root, FC#5, port B1
Entries 381
Mean 44.01
Std Dev 12.14
Turn on : 26.8032
Width : 1.204
Height : 10.009
Entry
ampl
0
2
4
6
8
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12
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0
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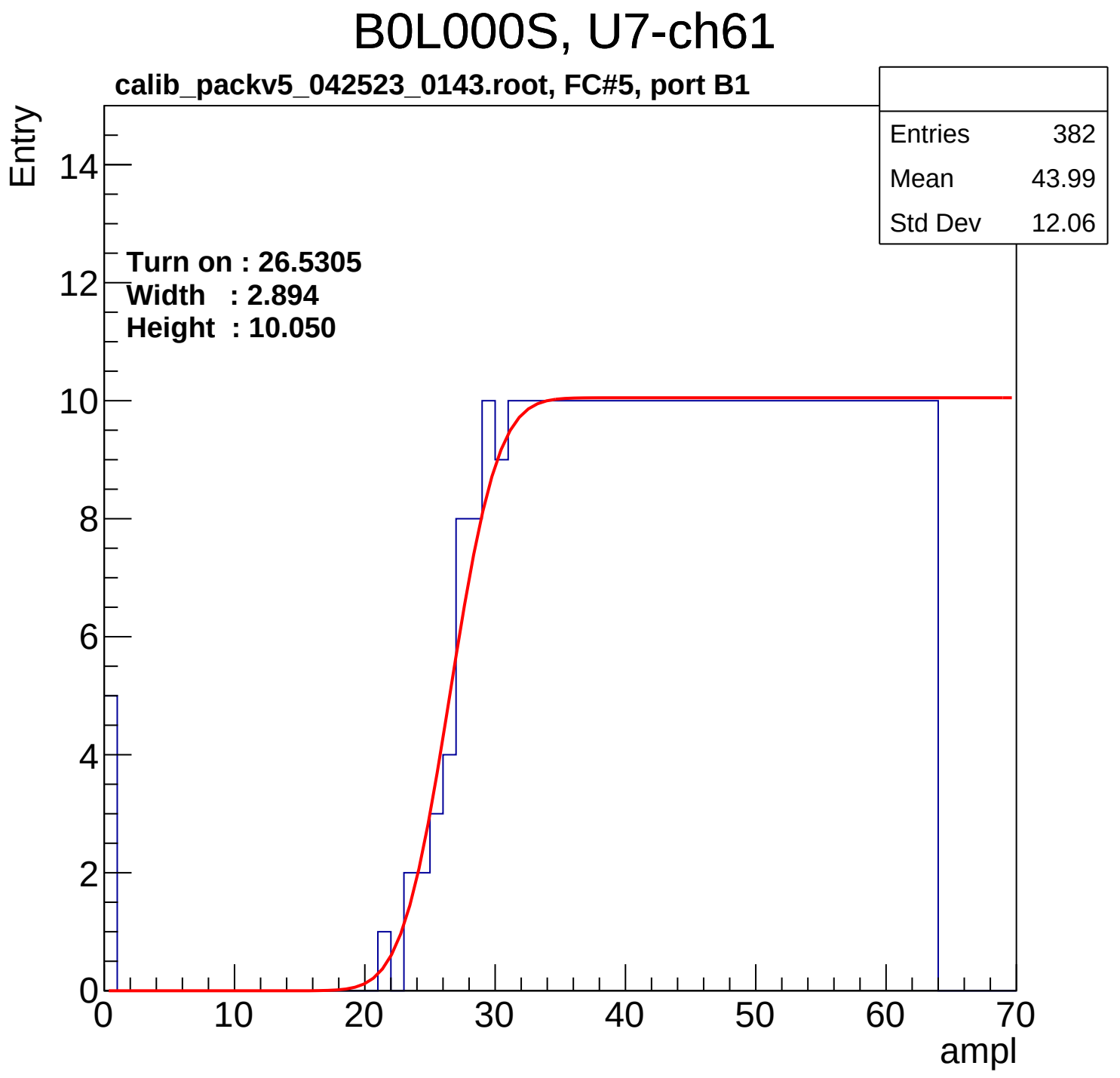
B0L000S, U7-ch61
calib_packv5_042523_0143.root, FC#5, port B1
Entries 382
Mean 43.99
Std Dev 12.06
Turn on : 26.5305
Width : 2.894
Height : 10.050
Entry
ampl
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4
6
8
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14
0
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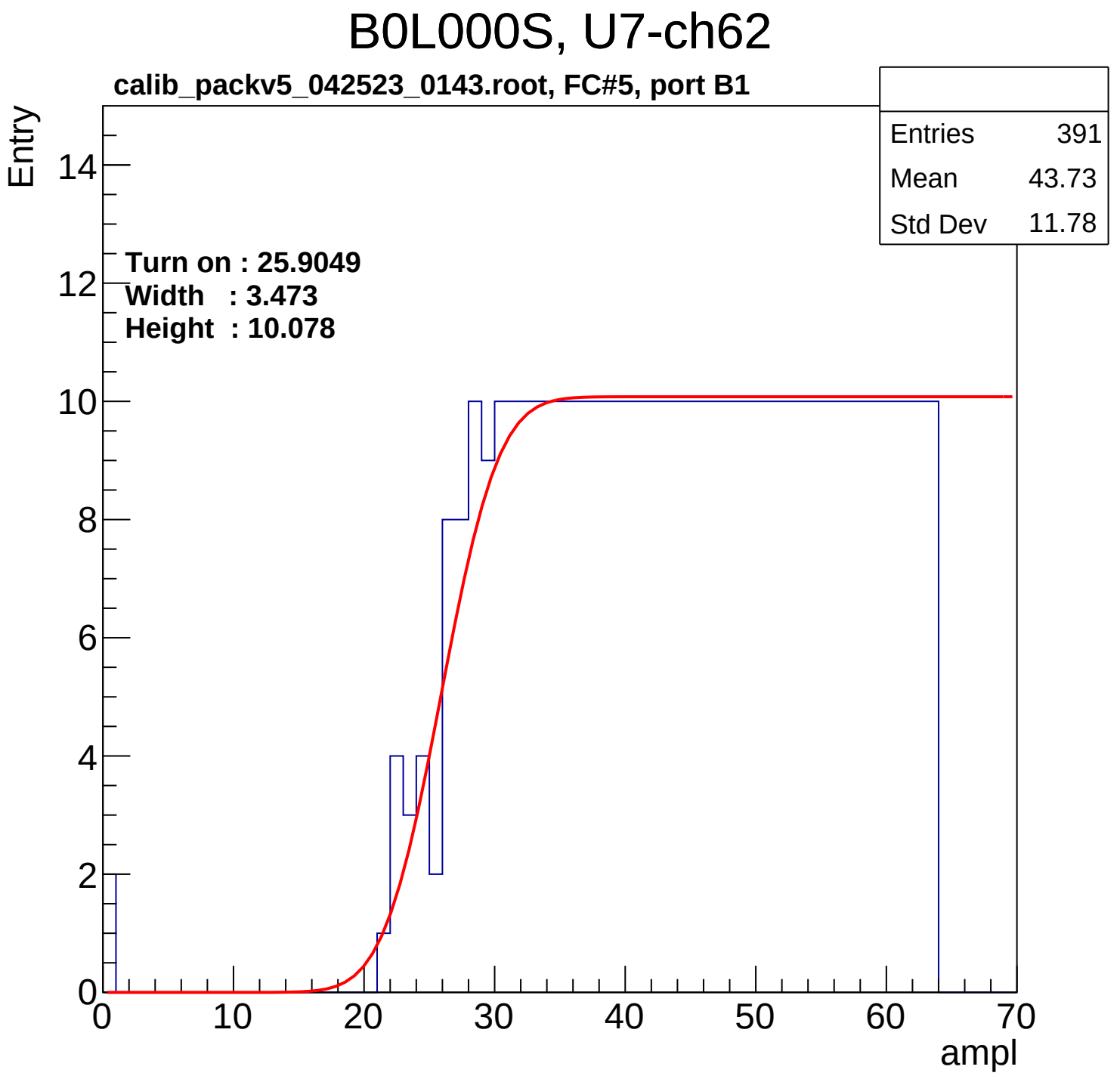
B0L000S, U7-ch62
calib_packv5_042523_0143.root, FC#5, port B1
Entries 391
Mean 43.73
Std Dev 11.78
Turn on : 25.9049
Width : 3.473
Height : 10.078
Entry
ampl
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2
4
6
8
10
12
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0
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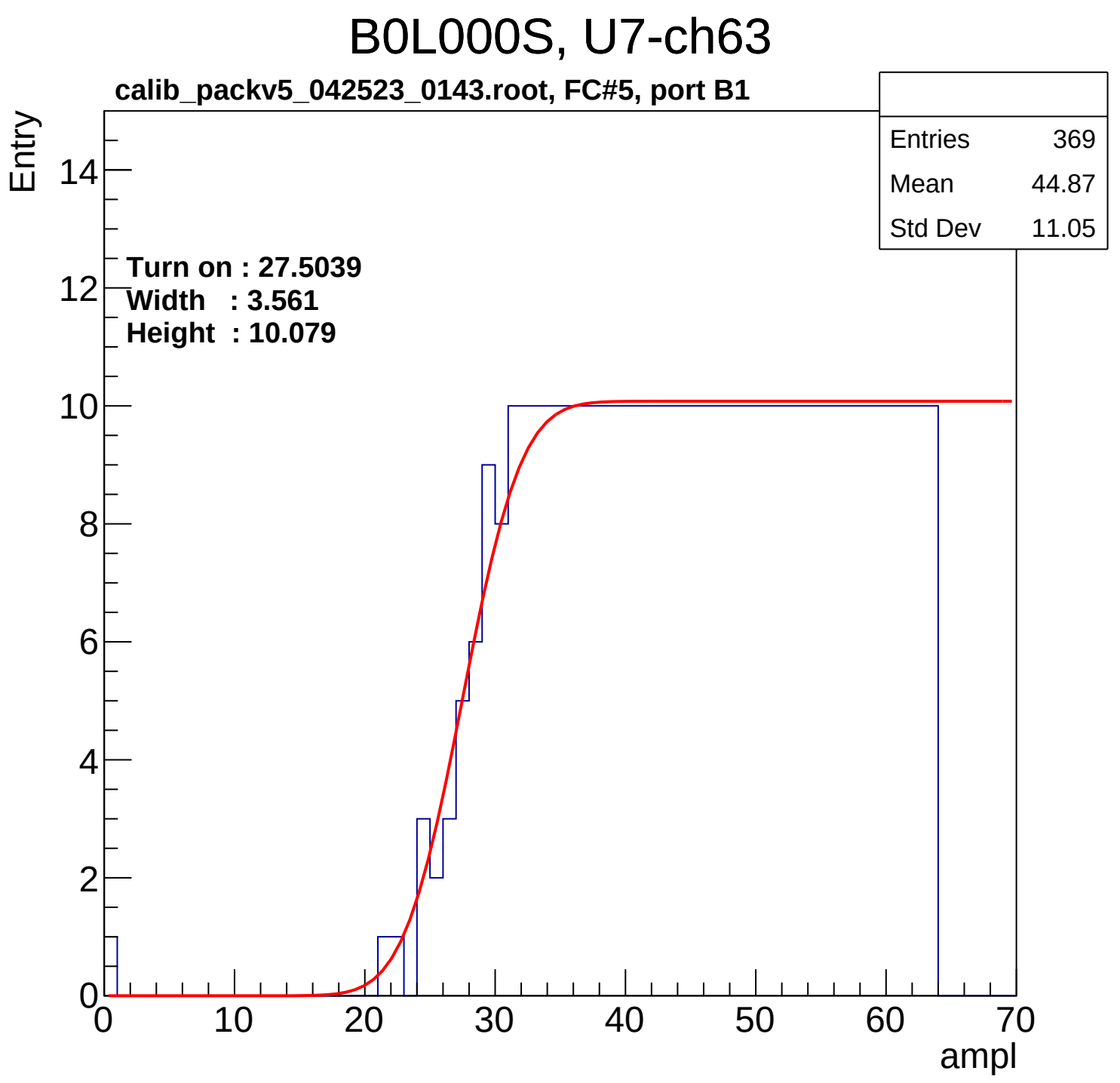
B0L000S, U7-ch63
calib_packv5_042523_0143.root, FC#5, port B1
Entries 369
Mean 44.87
Std Dev 11.05
Turn on : 27.5039
Width : 3.561
Height : 10.079
Entry
ampl
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2
4
6
8
10
12
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0
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40
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60
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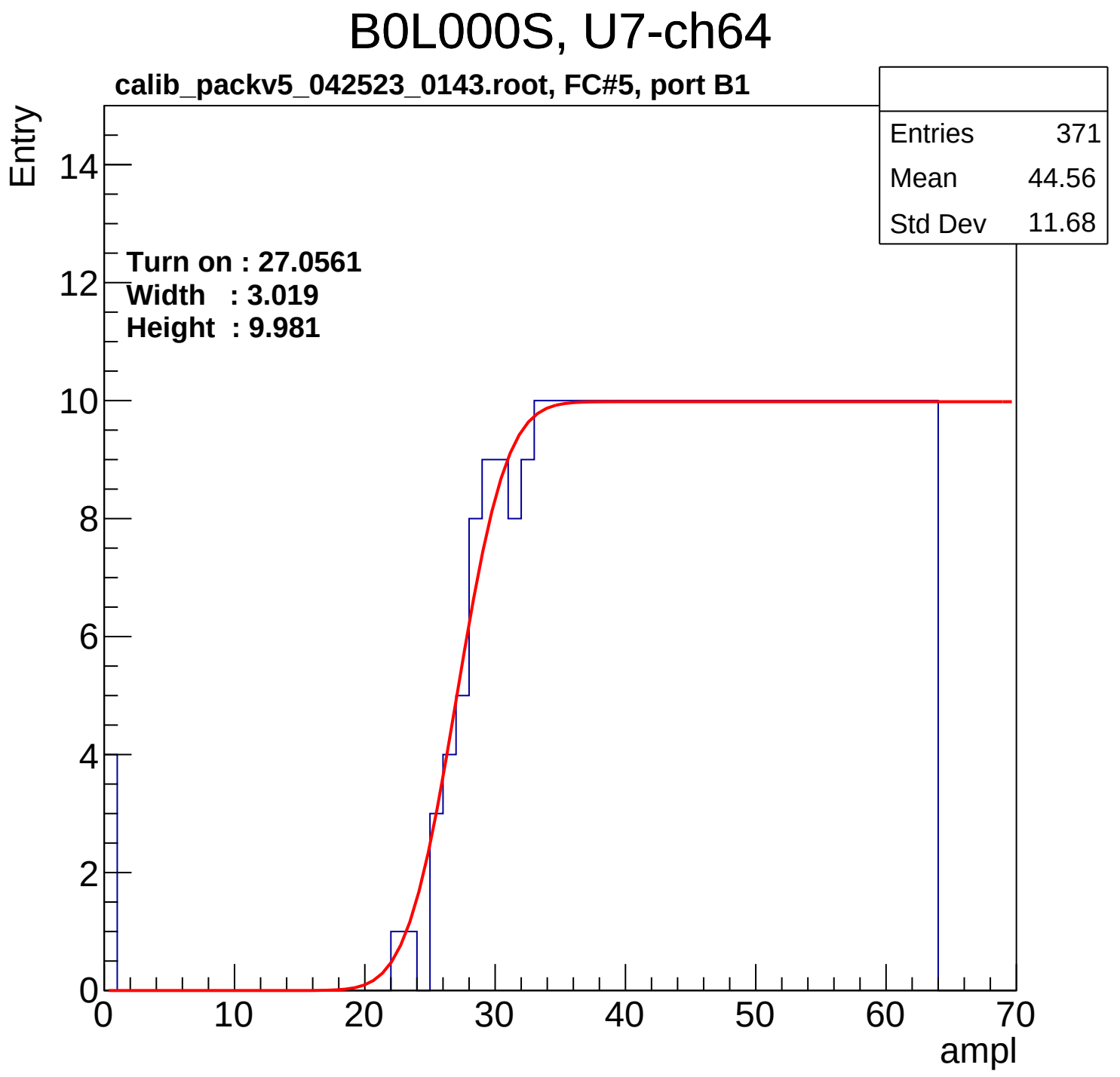
B0L000S, U7-ch64
calib_packv5_042523_0143.root, FC#5, port B1
Entries 371
Mean 44.56
Std Dev 11.68
Turn on : 27.0561
Width : 3.019
Height : 9.981
Entry
ampl
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2
4
6
8
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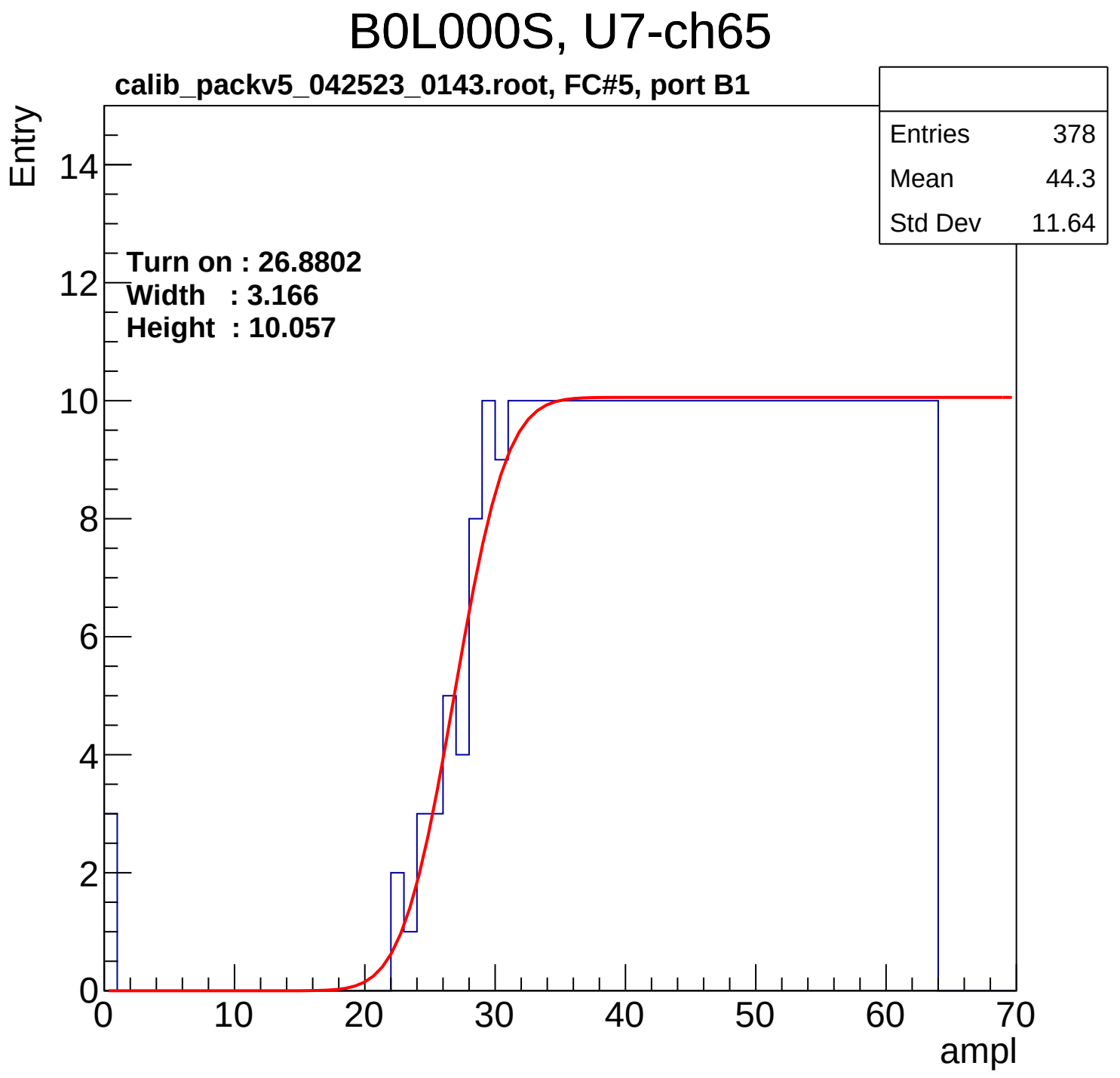
B0L000S, U7-ch65
calib_packv5_042523_0143.root, FC#5, port B1
Entries 378
Mean 44.3
Std Dev 11.64
Turn on : 26.8802
Width : 3.166
Height : 10.057
Entry
ampl
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2
4
6
8
10
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0
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40
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60
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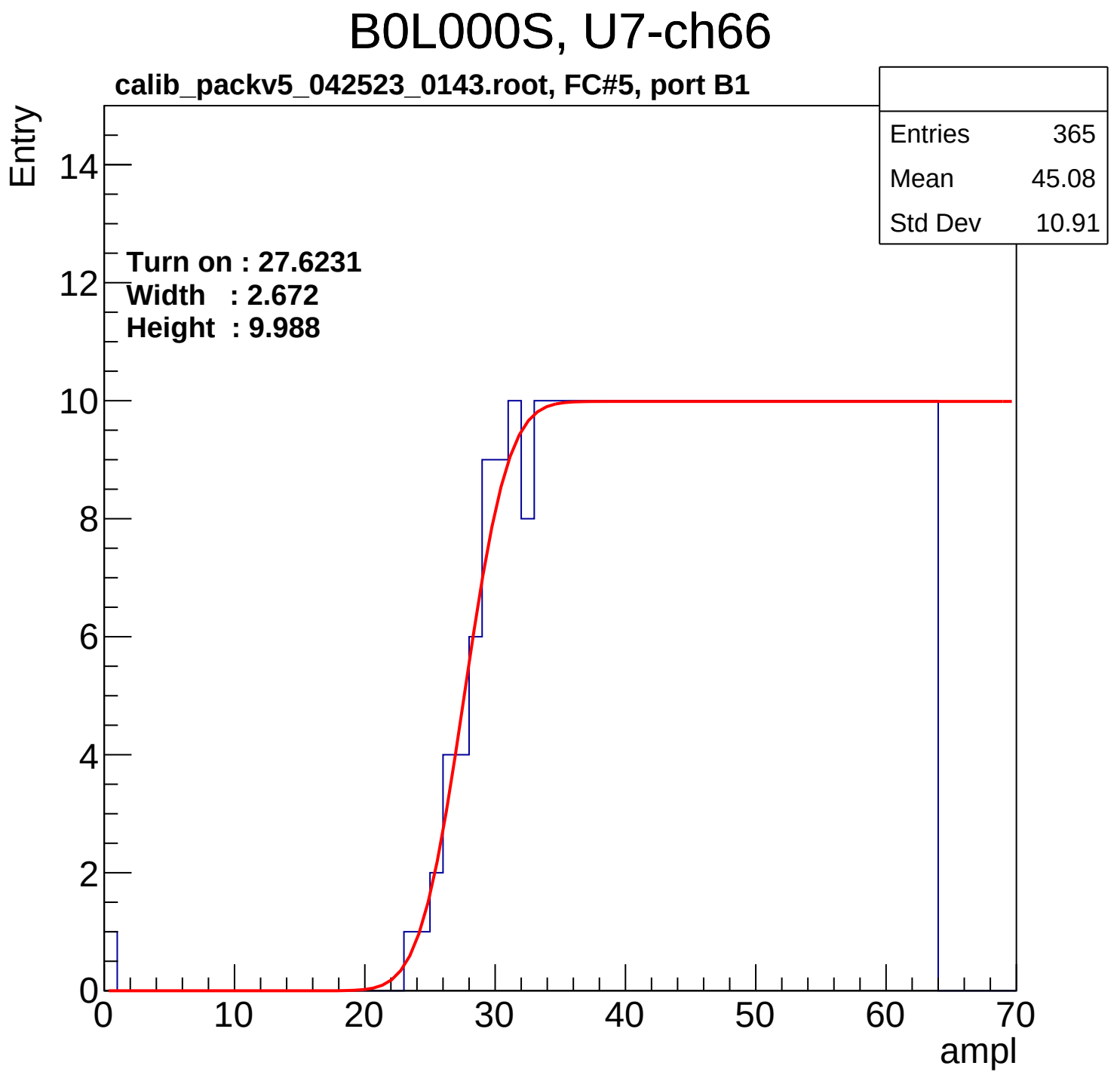
B0L000S, U7-ch66
calib_packv5_042523_0143.root, FC#5, port B1
Entries 365
Mean 45.08
Std Dev 10.91
Turn on : 27.6231
Width : 2.672
Height : 9.988
Entry
ampl
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2
4
6
8
10
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0
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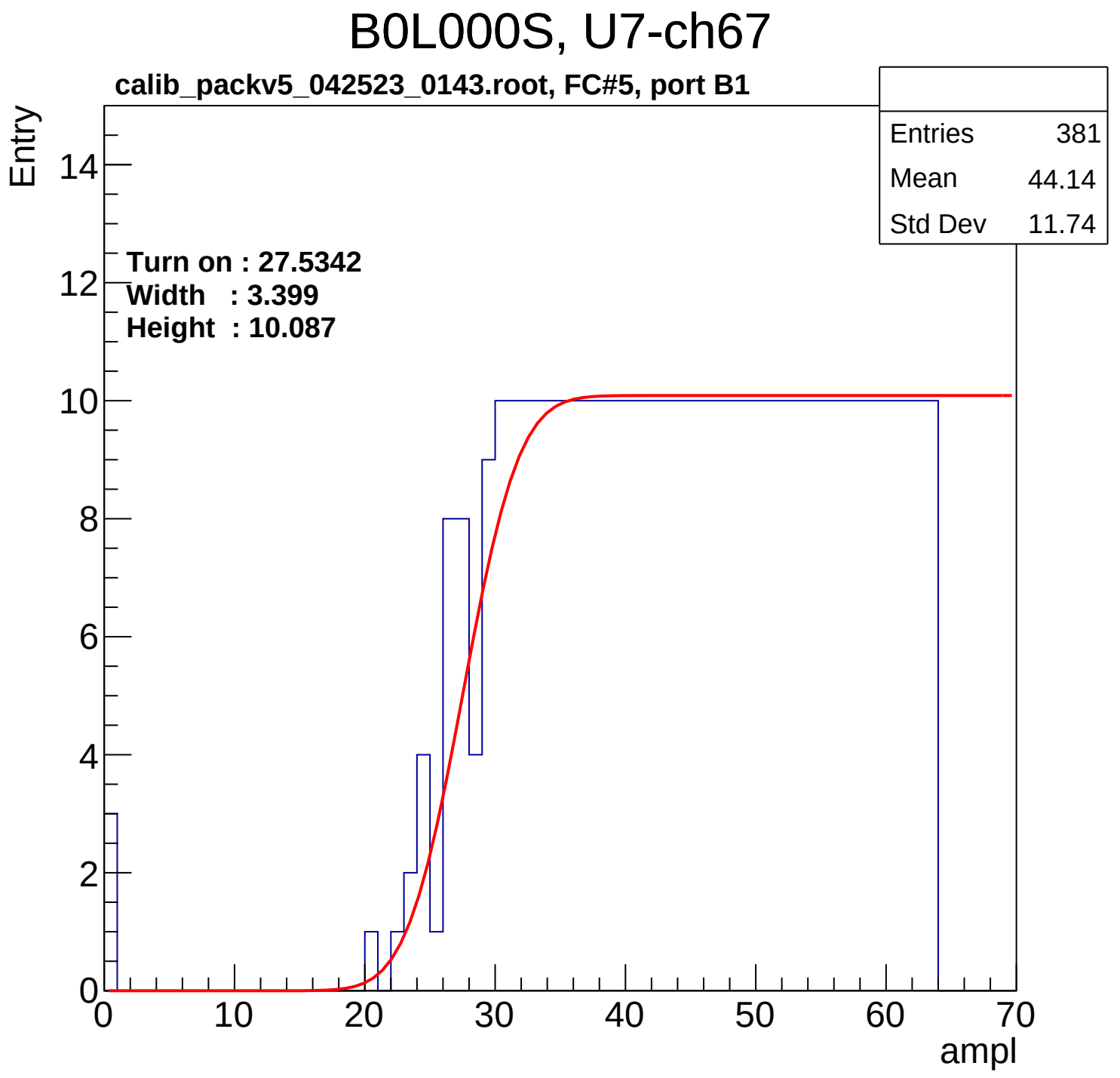
B0L000S, U7-ch67
calib_packv5_042523_0143.root, FC#5, port B1
Entries 381
Mean 44.14
Std Dev 11.74
Turn on : 27.5342
Width : 3.399
Height : 10.087
Entry
ampl
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4
6
8
10
12
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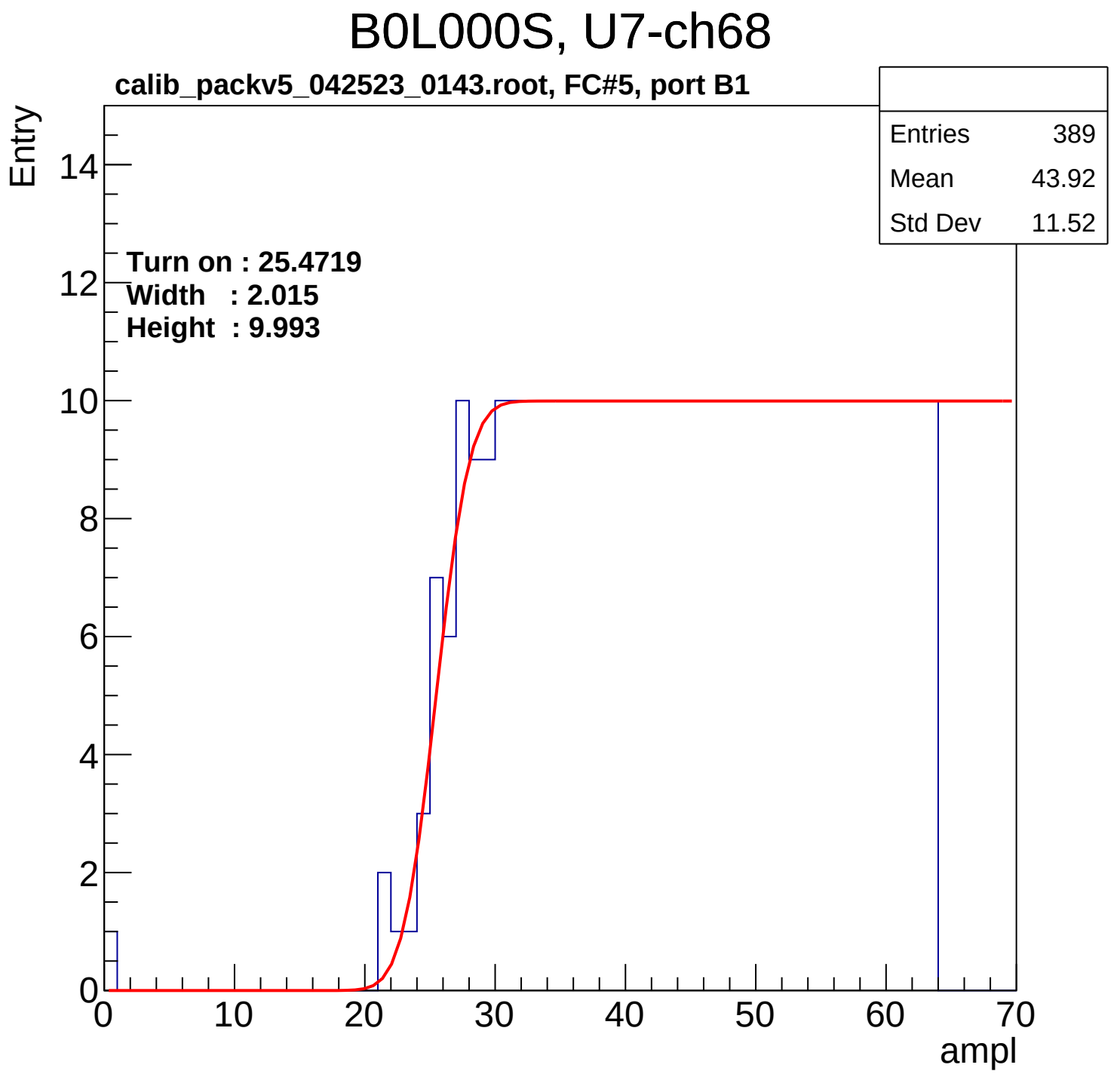
B0L000S, U7-ch68
calib_packv5_042523_0143.root, FC#5, port B1
Entries 389
Mean 43.92
Std Dev 11.52
Turn on : 25.4719
Width : 2.015
Height : 9.993
Entry
ampl
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2
4
6
8
10
12
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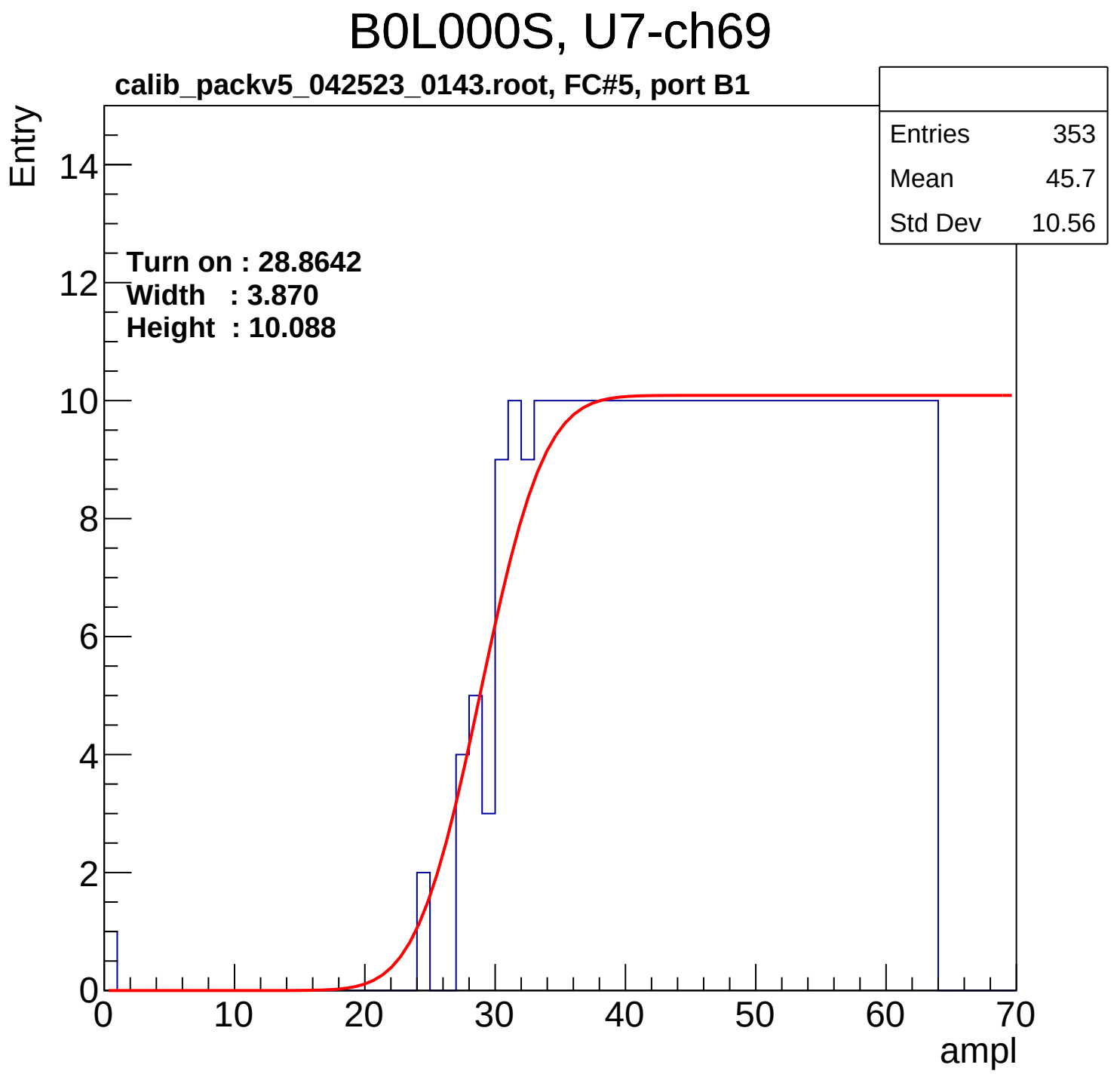
B0L000S, U7-ch69
calib_packv5_042523_0143.root, FC#5, port B1
Entries 353
Mean 45.7
Std Dev 10.56
Turn on : 28.8642
Width : 3.870
Height : 10.088
Entry
ampl
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2
4
6
8
10
12
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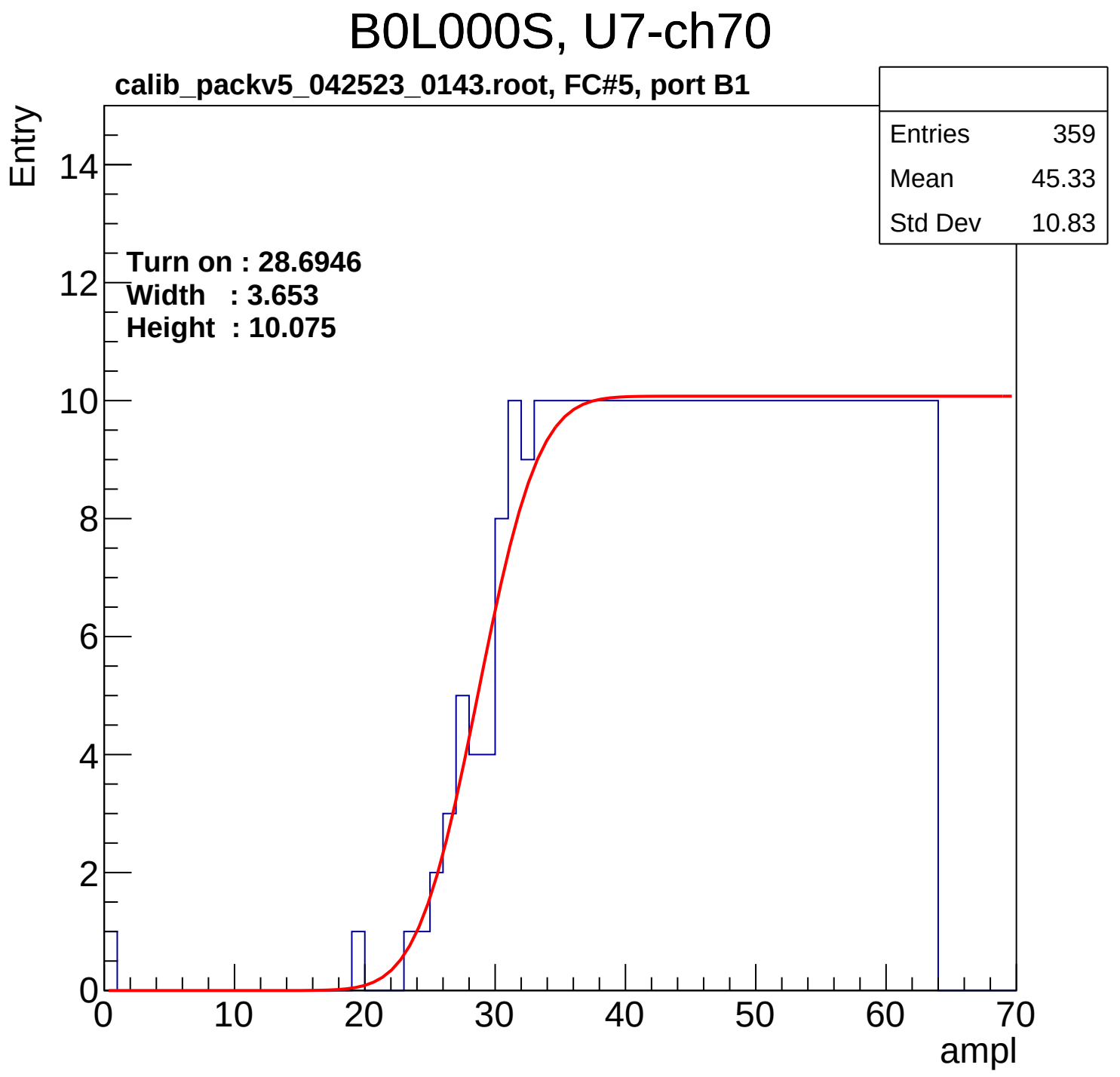
B0L000S, U7-ch70
calib_packv5_042523_0143.root, FC#5, port B1
Entries 359
Mean 45.33
Std Dev 10.83
Turn on : 28.6946
Width : 3.653
Height : 10.075
Entry
ampl
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2
4
6
8
10
12
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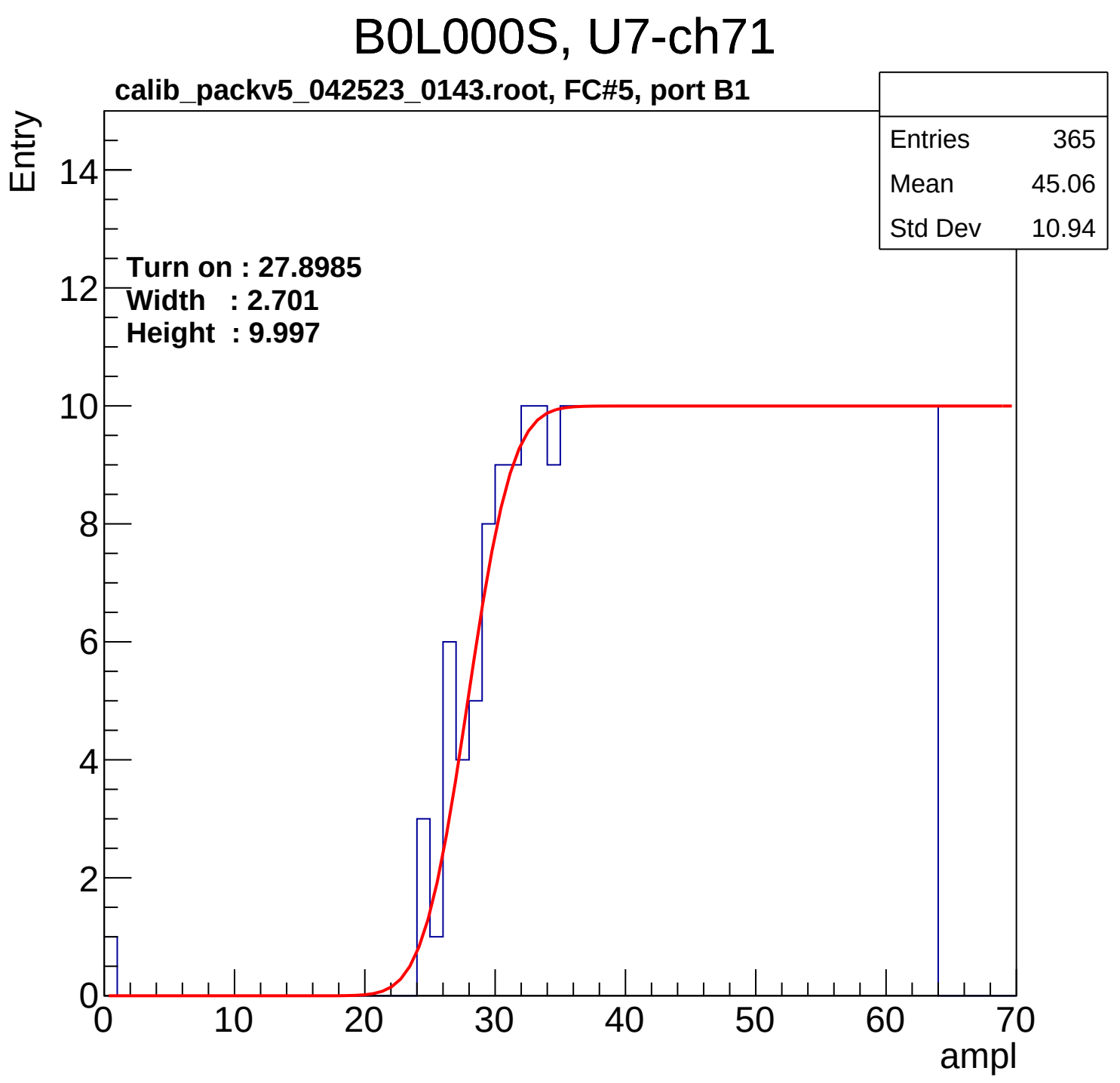
B0L000S, U7-ch71
calib_packv5_042523_0143.root, FC#5, port B1
Entries 365
Mean 45.06
Std Dev 10.94
Turn on : 27.8985
Width : 2.701
Height : 9.997
Entry
ampl
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4
6
8
10
12
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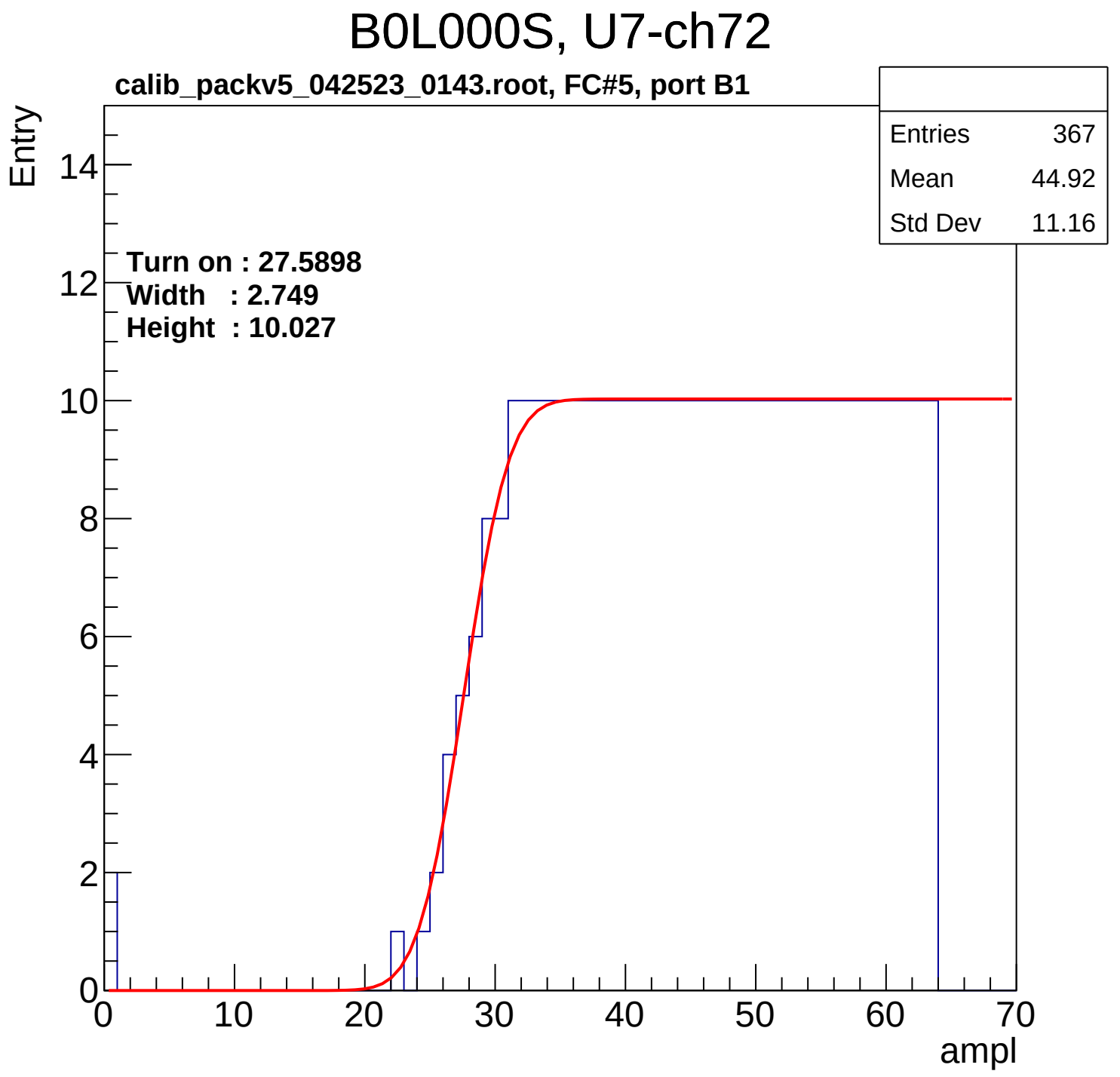
B0L000S, U7-ch72
calib_packv5_042523_0143.root, FC#5, port B1
Entries 367
Mean 44.92
Std Dev 11.16
Turn on : 27.5898
Width : 2.749
Height : 10.027
Entry
ampl
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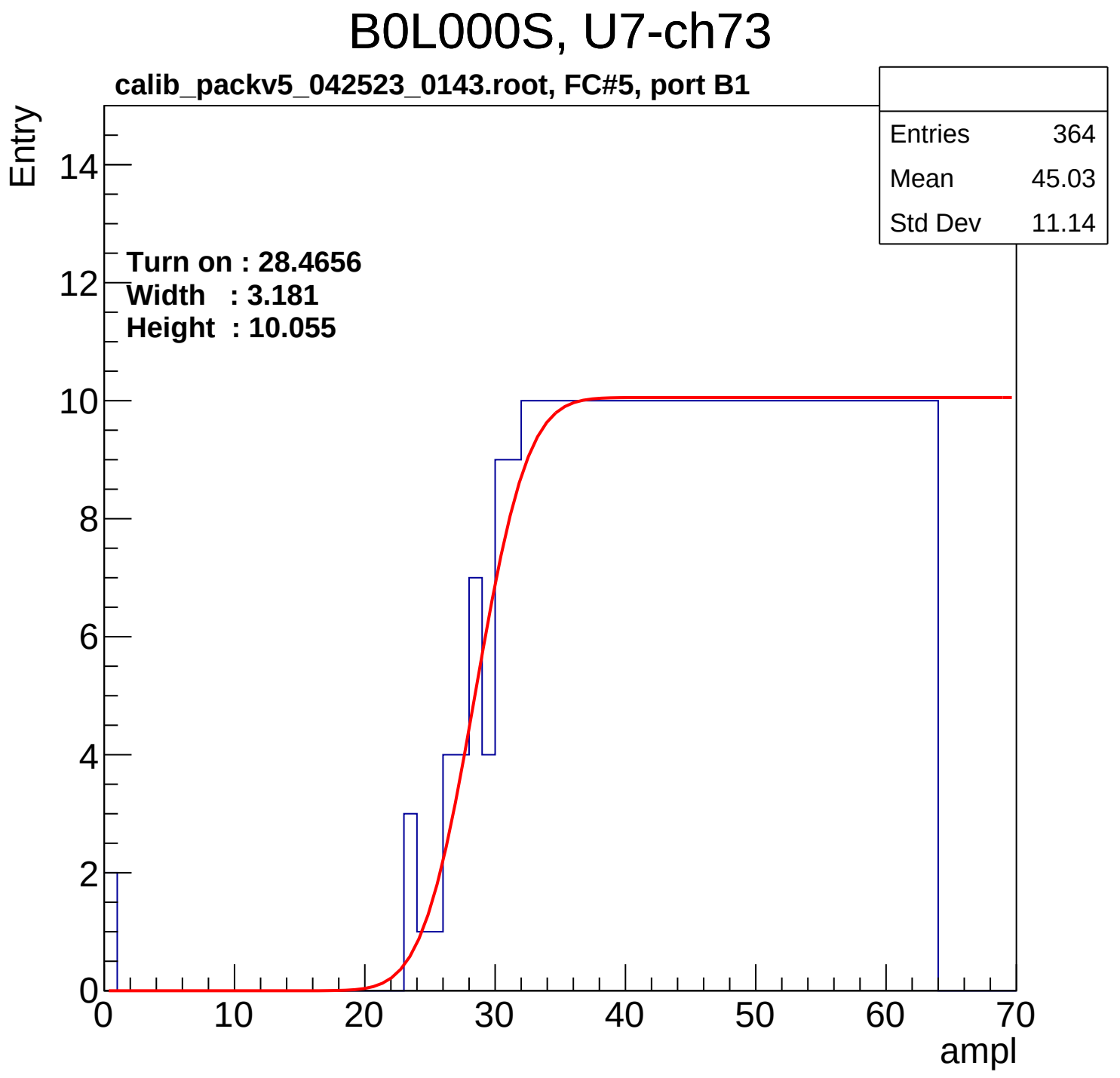
B0L000S, U7-ch73
calib_packv5_042523_0143.root, FC#5, port B1
Entries 364
Mean 45.03
Std Dev 11.14
Turn on : 28.4656
Width : 3.181
Height : 10.055
Entry
ampl
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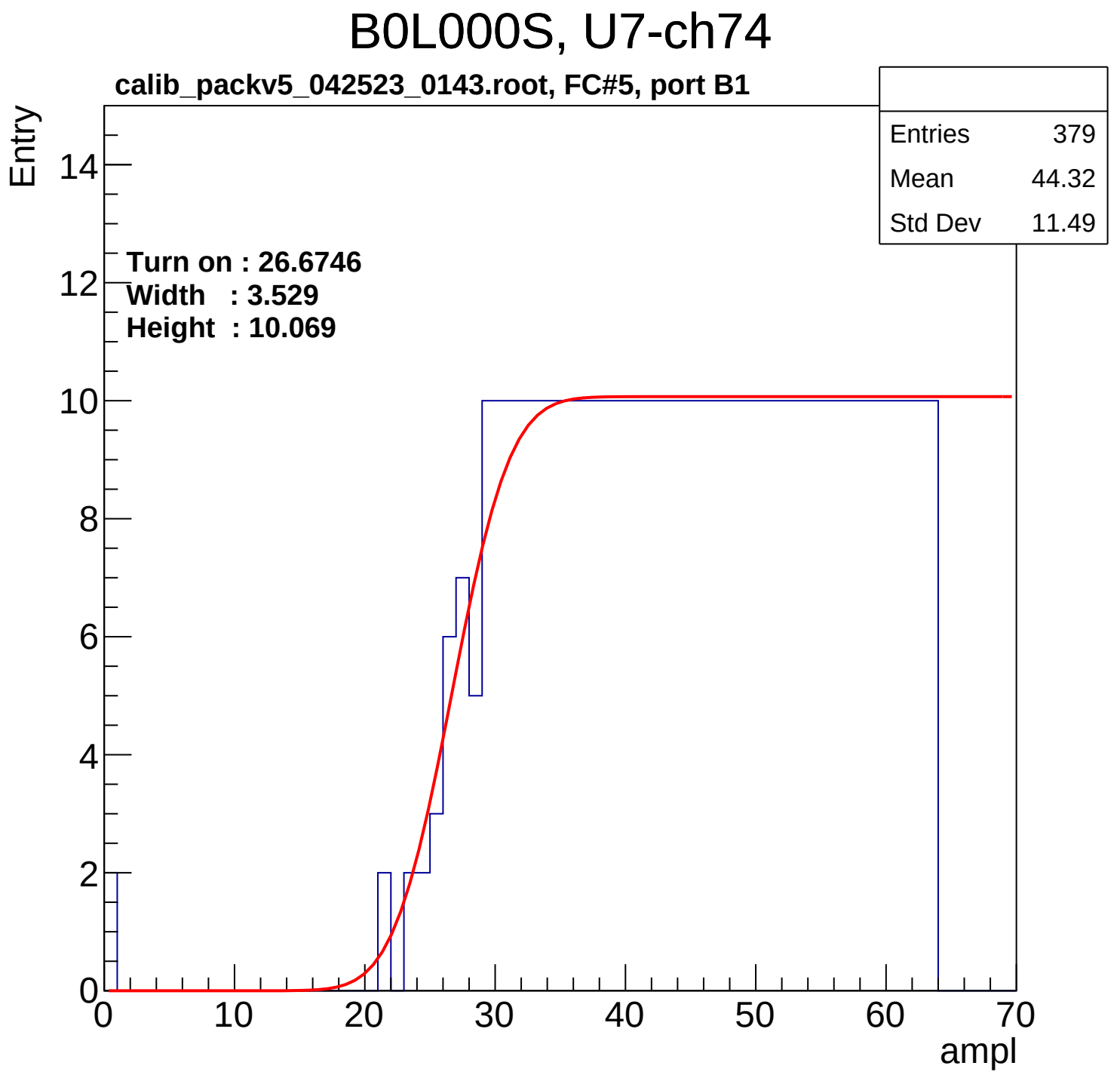
B0L000S, U7-ch74
calib_packv5_042523_0143.root, FC#5, port B1
Entries 379
Mean 44.32
Std Dev 11.49
Turn on : 26.6746
Width : 3.529
Height : 10.069
Entry
ampl
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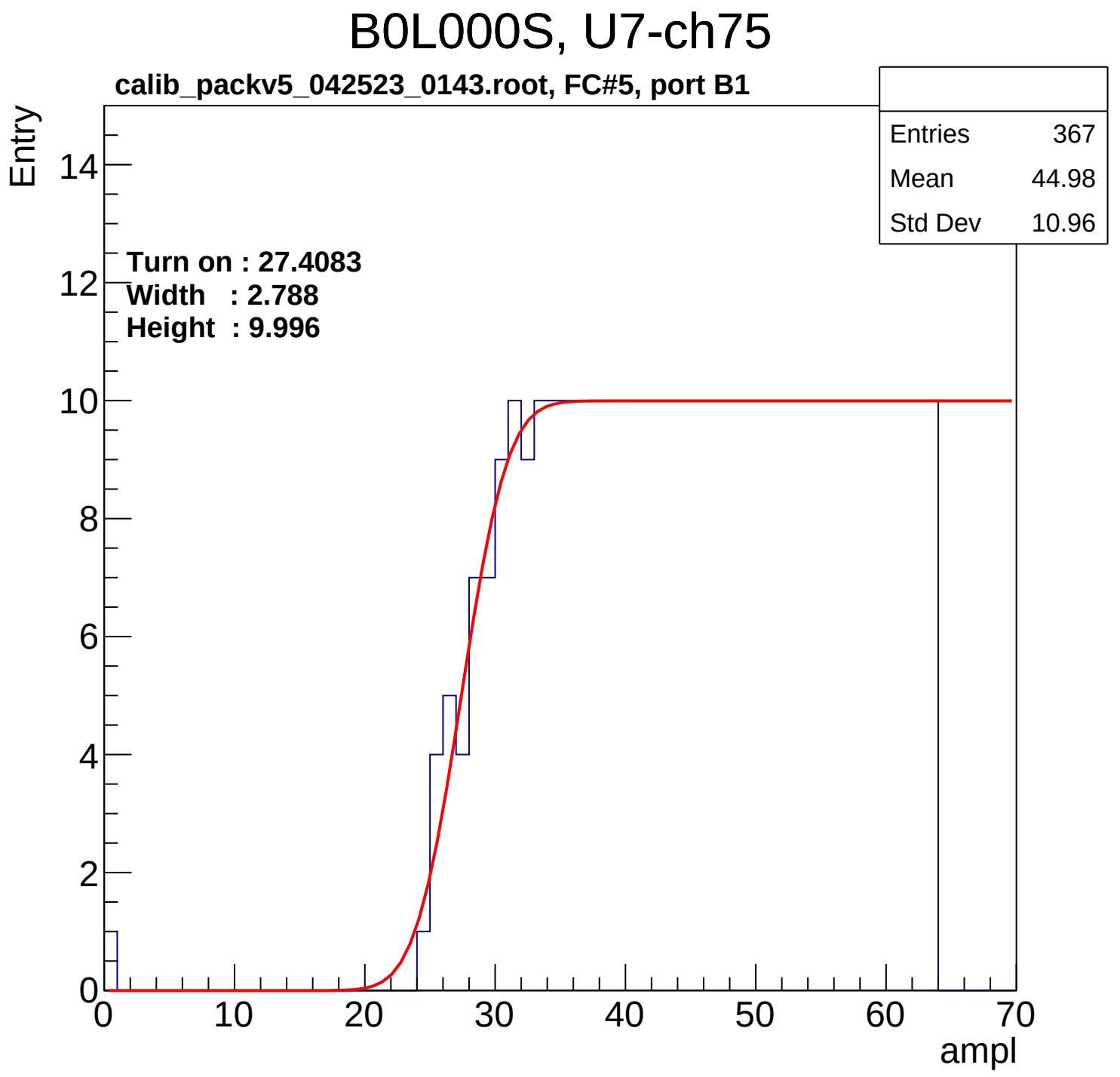
B0L000S, U7-ch75
calib_packv5_042523_0143.root, FC#5, port B1
Entries 367
Mean 44.98
Std Dev 10.96
Turn on : 27.4083
Width : 2.788
Height : 9.996
Entry
ampl
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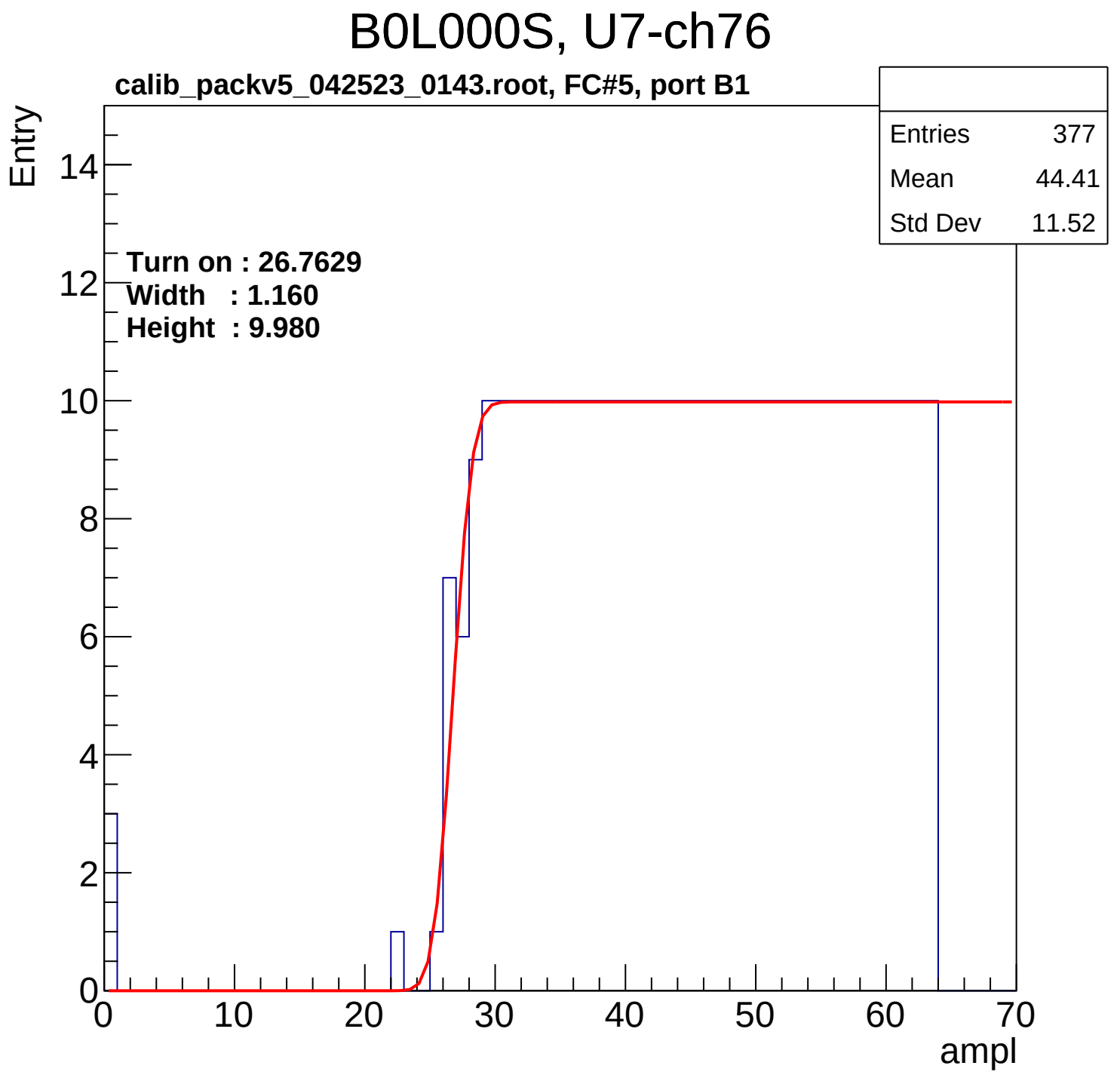
B0L000S, U7-ch76
calib_packv5_042523_0143.root, FC#5, port B1
Entries 377
Mean 44.41
Std Dev 11.52
Turn on : 26.7629
Width : 1.160
Height : 9.980
Entry
ampl
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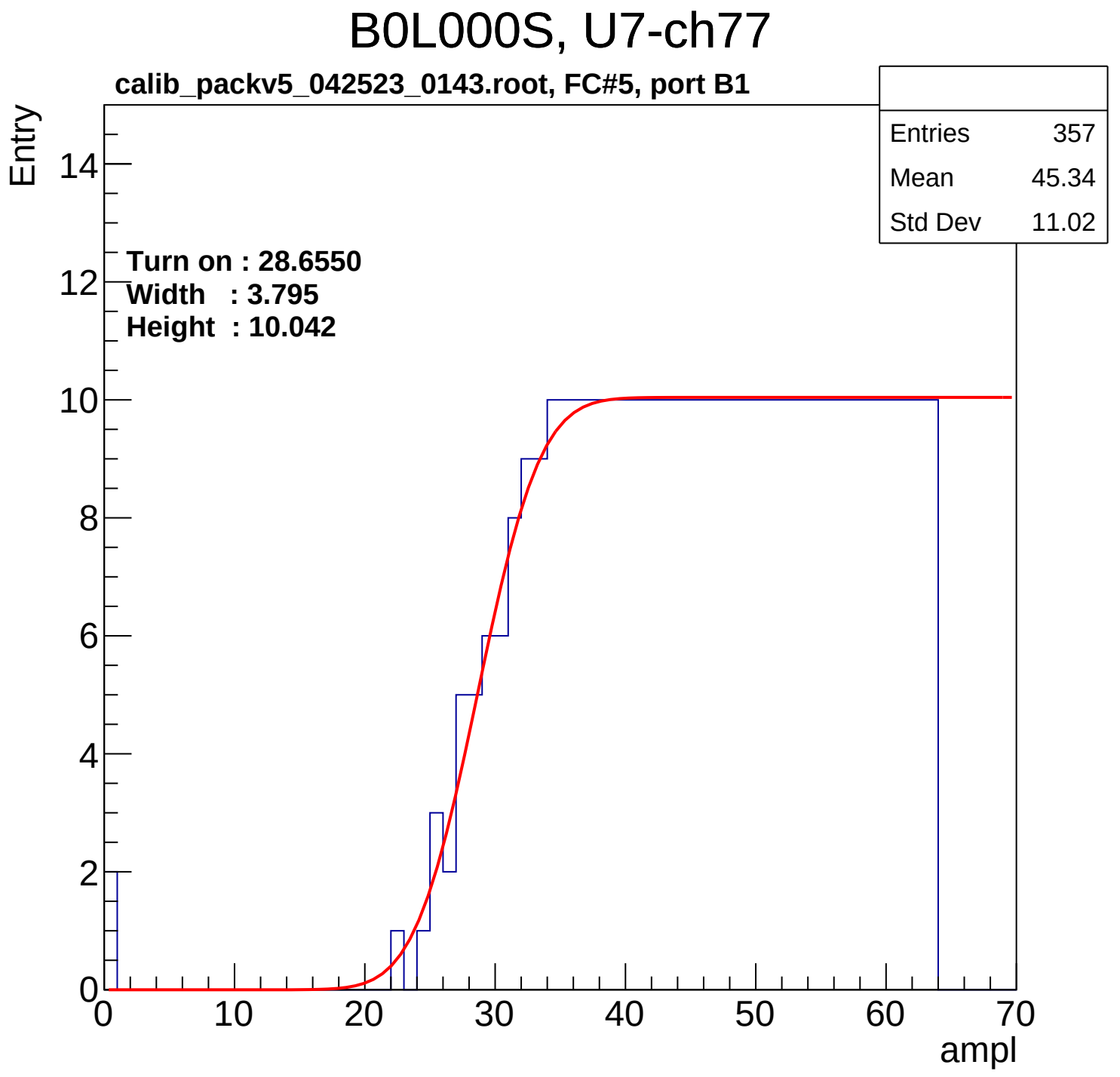
B0L000S, U7-ch77
calib_packv5_042523_0143.root, FC#5, port B1
Entries 357
Mean 45.34
Std Dev 11.02
Turn on : 28.6550
Width : 3.795
Height : 10.042
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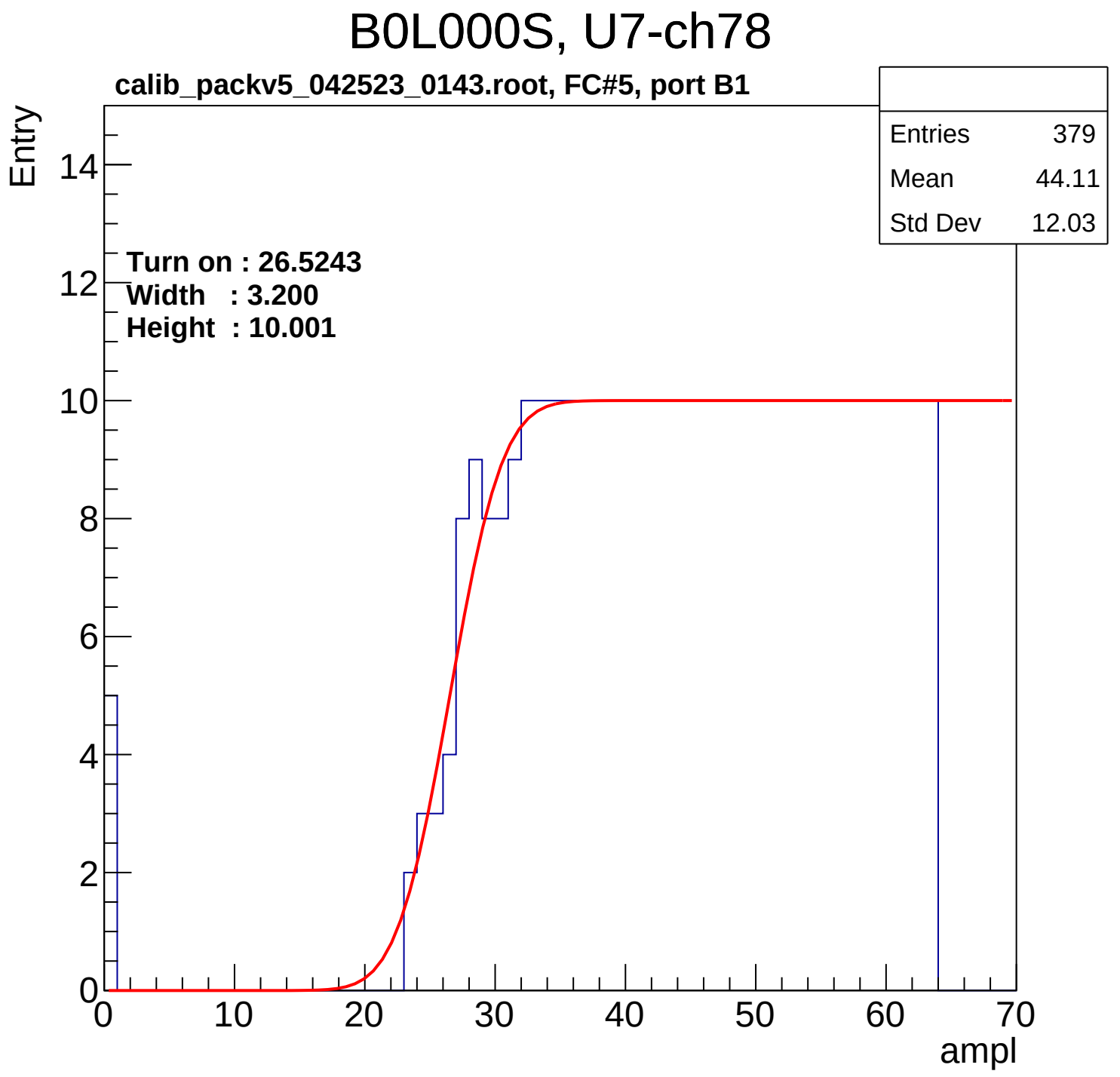
B0L000S, U7-ch78
calib_packv5_042523_0143.root, FC#5, port B1
Entries 379
Mean 44.11
Std Dev 12.03
Turn on : 26.5243
Width : 3.200
Height : 10.001
Entry
ampl
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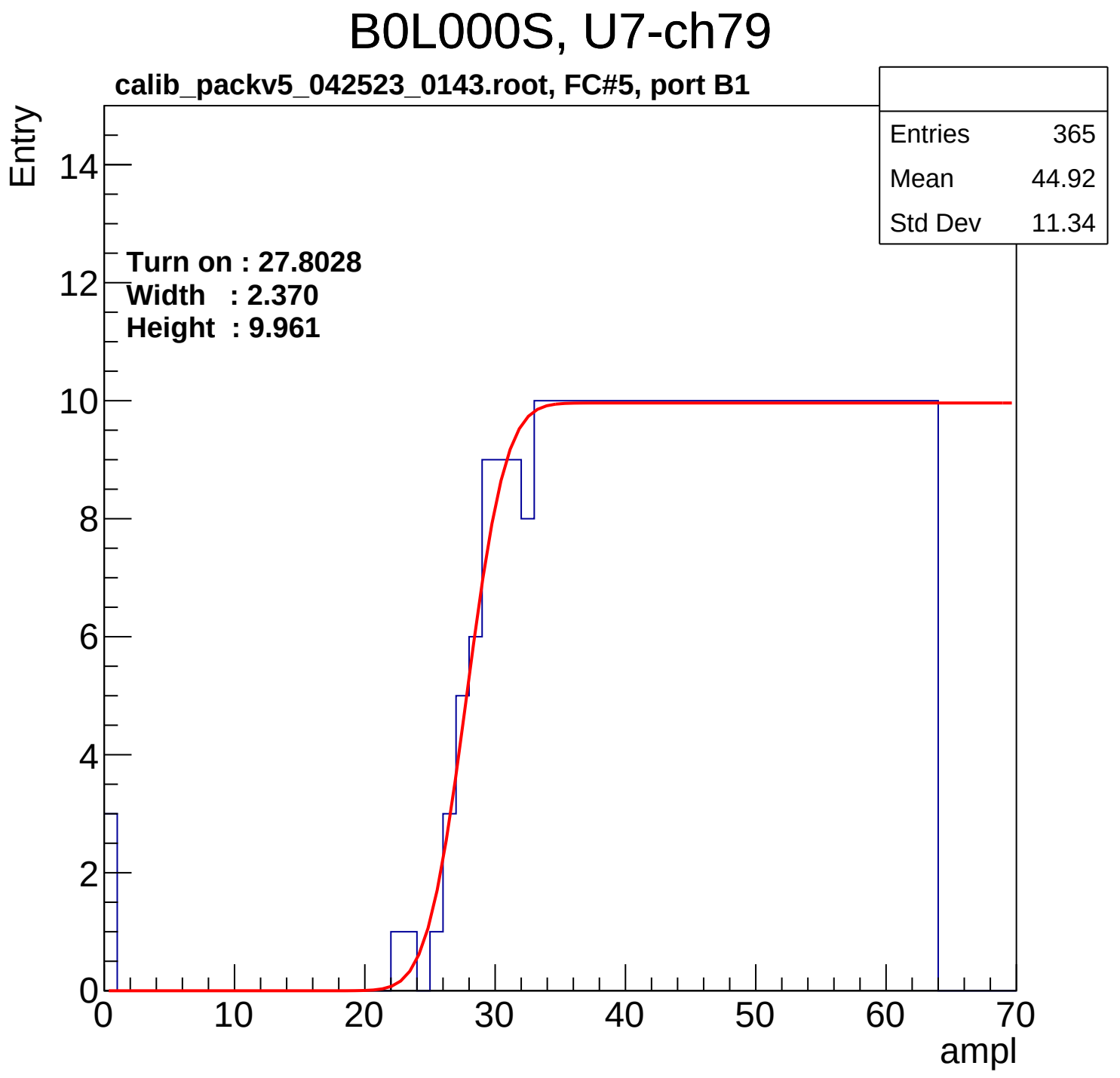
B0L000S, U7-ch79
calib_packv5_042523_0143.root, FC#5, port B1
Entries 365
Mean 44.92
Std Dev 11.34
Turn on : 27.8028
Width : 2.370
Height : 9.961
Entry
ampl
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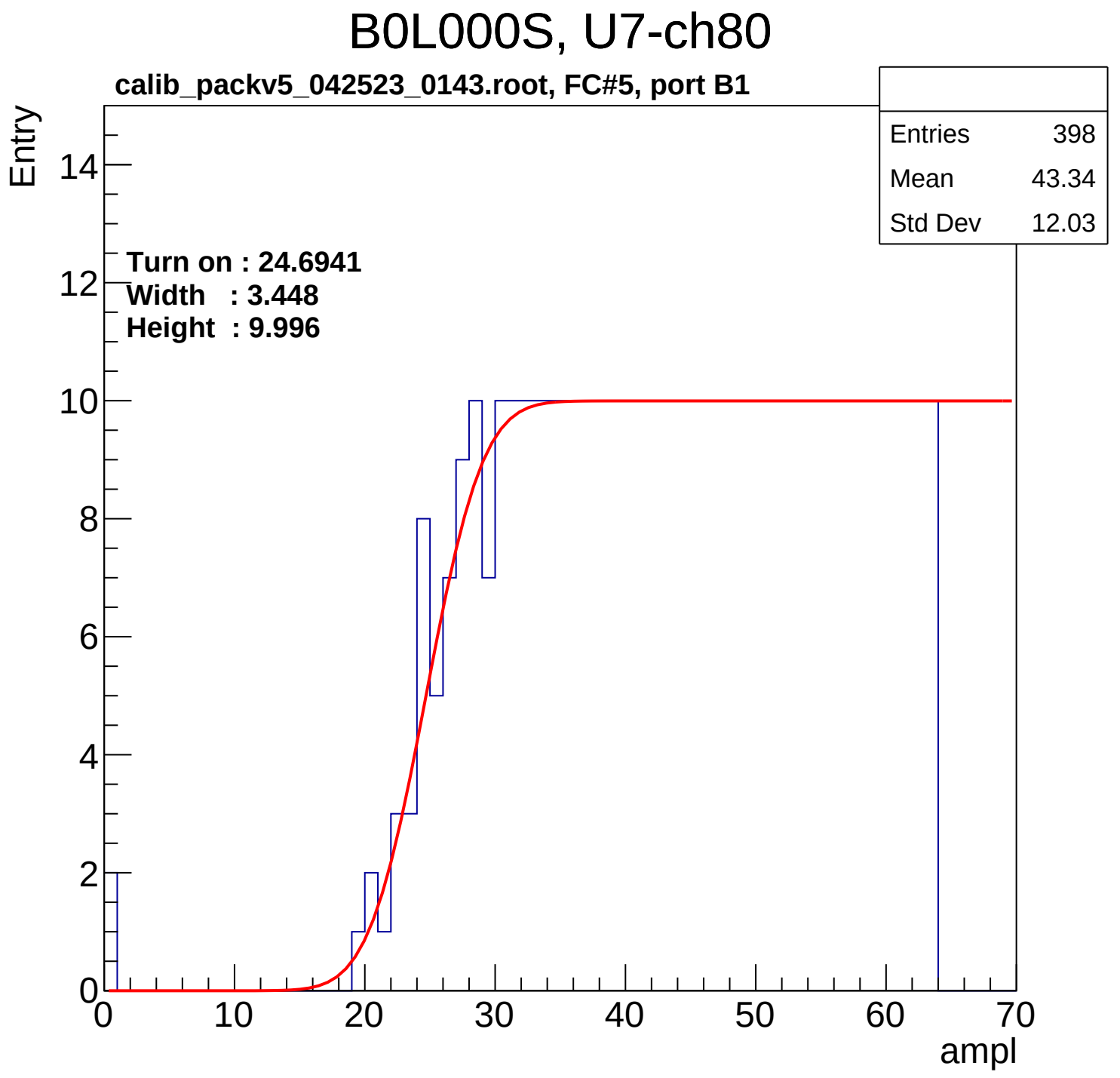
B0L000S, U7-ch80
calib_packv5_042523_0143.root, FC#5, port B1
Entries 398
Mean 43.34
Std Dev 12.03
Turn on : 24.6941
Width : 3.448
Height : 9.996
Entry
ampl
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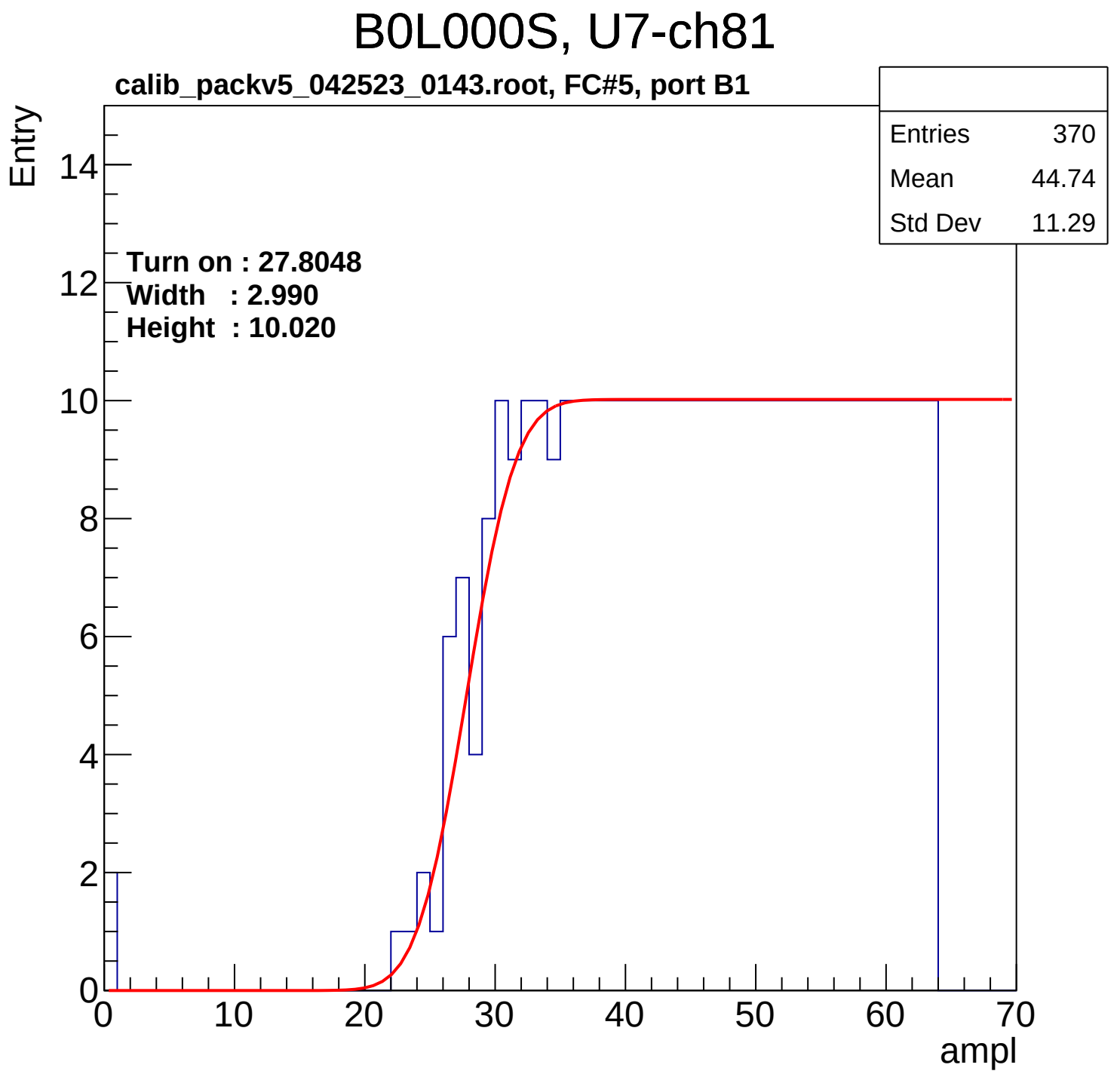
B0L000S, U7-ch81
calib_packv5_042523_0143.root, FC#5, port B1
Entries 370
Mean 44.74
Std Dev 11.29
Turn on : 27.8048
Width : 2.990
Height : 10.020
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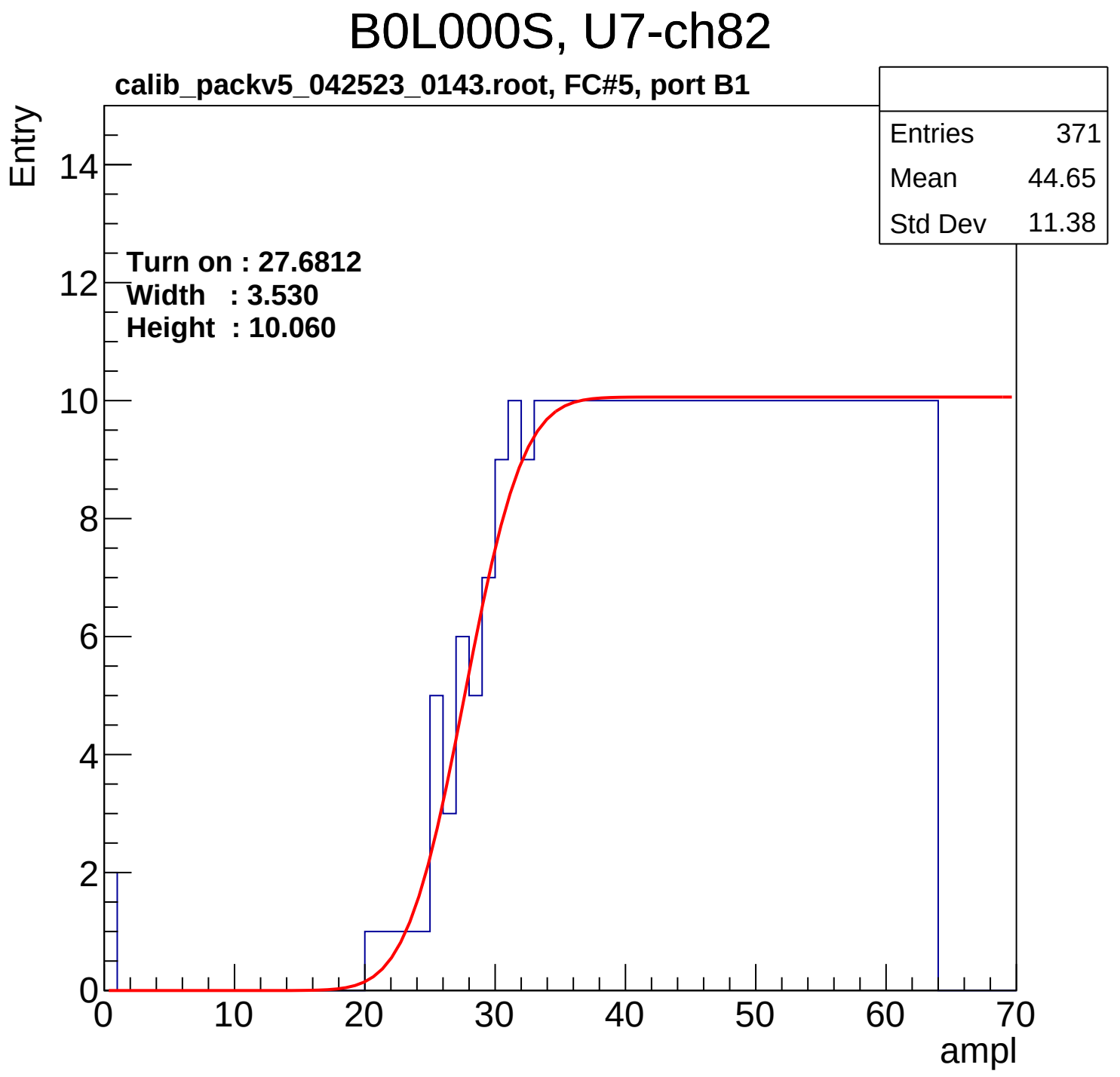
B0L000S, U7-ch82
calib_packv5_042523_0143.root, FC#5, port B1
Entries 371
Mean 44.65
Std Dev 11.38
Turn on : 27.6812
Width : 3.530
Height : 10.060
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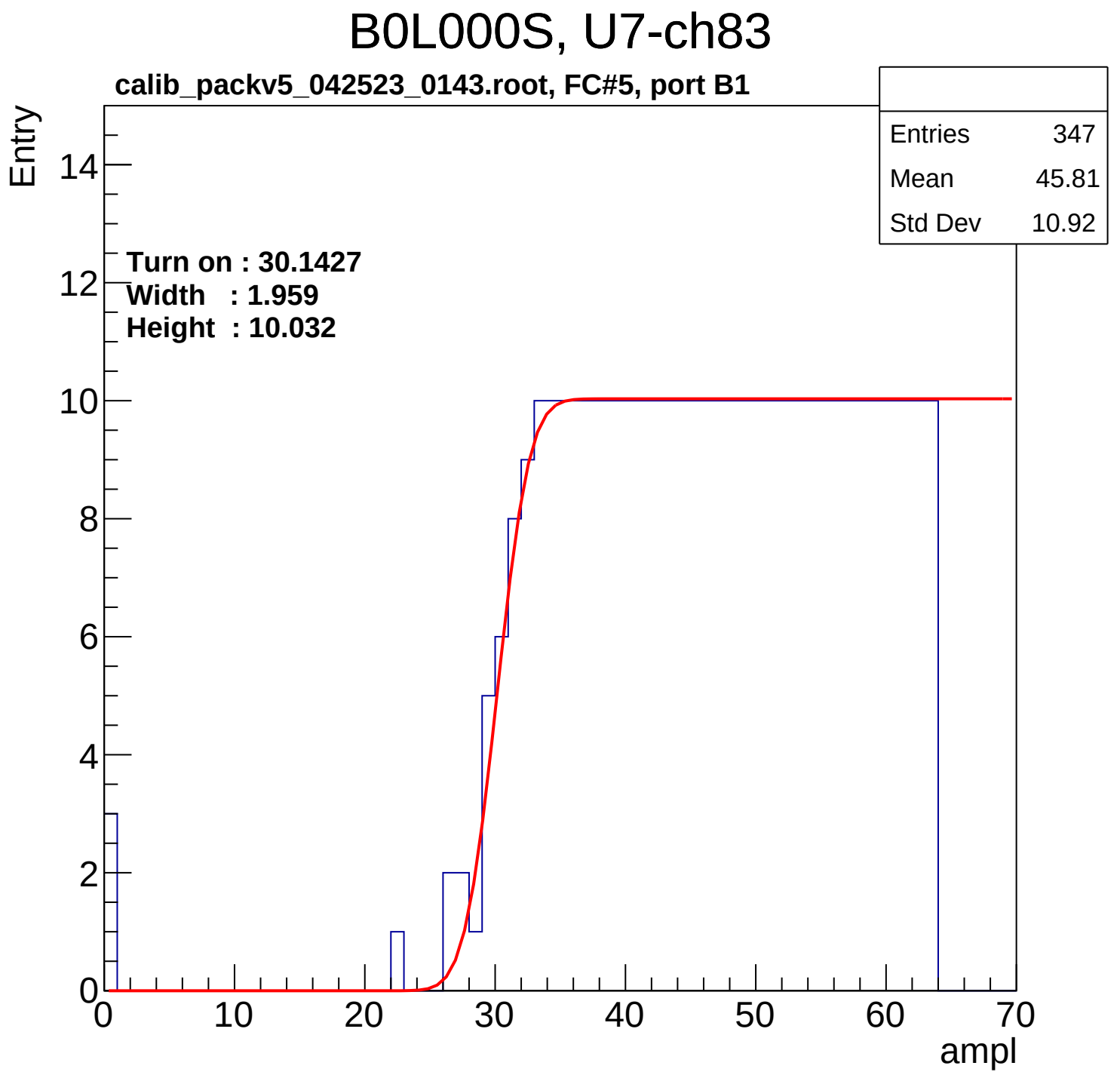
B0L000S, U7-ch83
calib_packv5_042523_0143.root, FC#5, port B1
Entries 347
Mean 45.81
Std Dev 10.92
Turn on : 30.1427
Width : 1.959
Height : 10.032
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ampl
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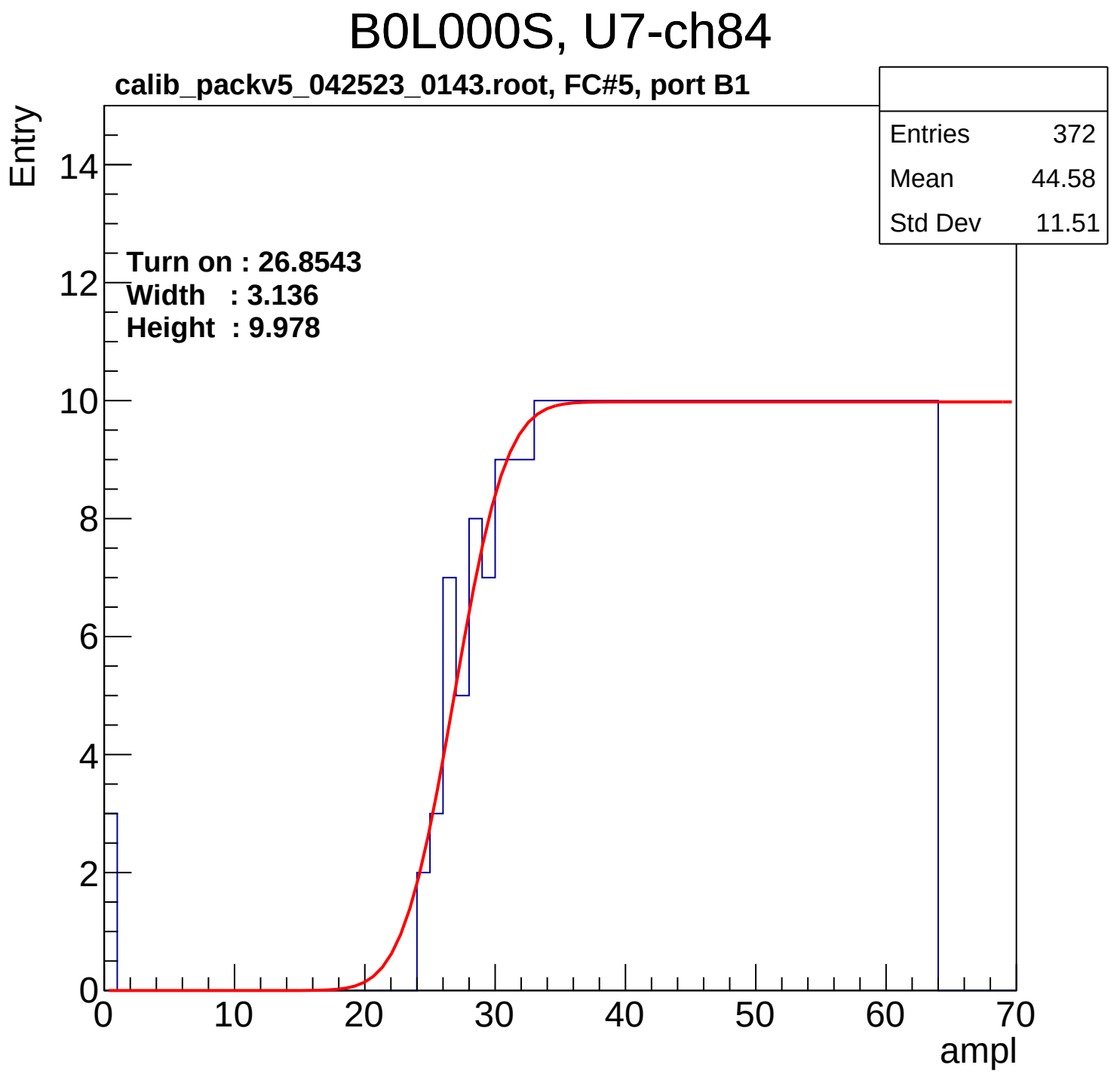
B0L000S, U7-ch84
calib_packv5_042523_0143.root, FC#5, port B1
Entries 372
Mean 44.58
Std Dev 11.51
Turn on : 26.8543
Width : 3.136
Height : 9.978
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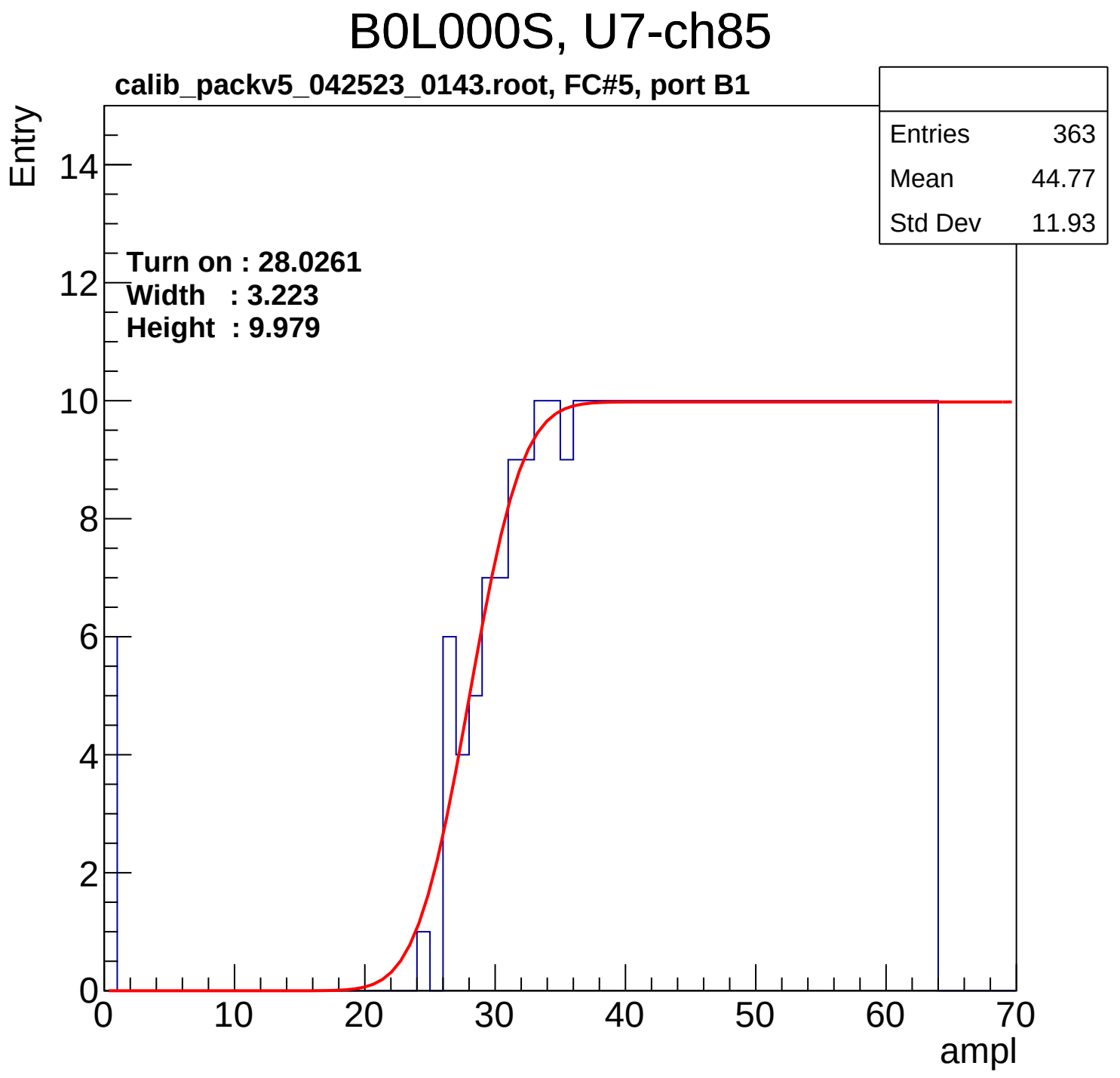
B0L000S, U7-ch85
calib_packv5_042523_0143.root, FC#5, port B1
Entries 363
Mean 44.77
Std Dev 11.93
Turn on : 28.0261
Width : 3.223
Height : 9.979
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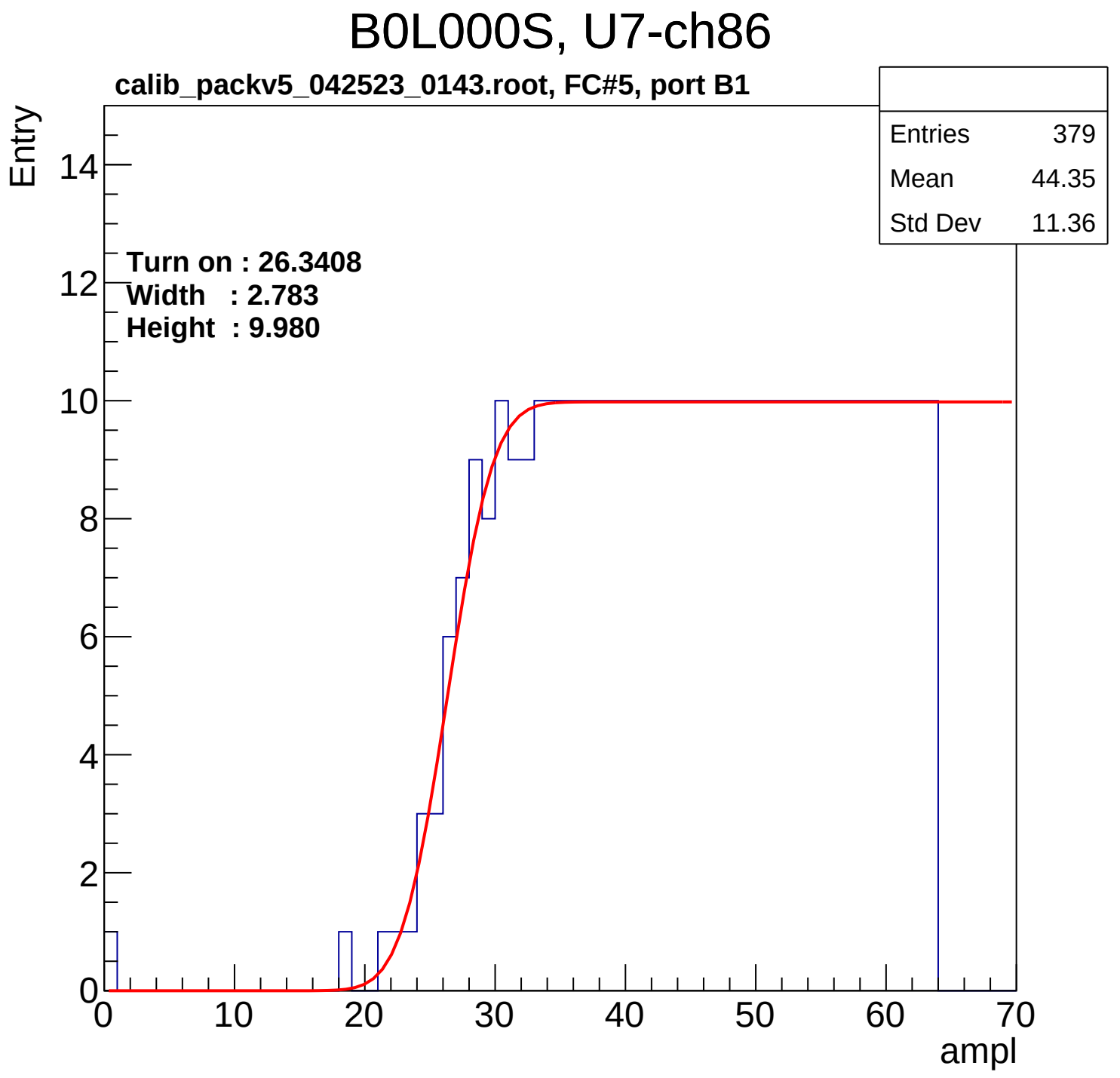
B0L000S, U7-ch86
calib_packv5_042523_0143.root, FC#5, port B1
Entries 379
Mean 44.35
Std Dev 11.36
Turn on : 26.3408
Width : 2.783
Height : 9.980
Entry
ampl
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6
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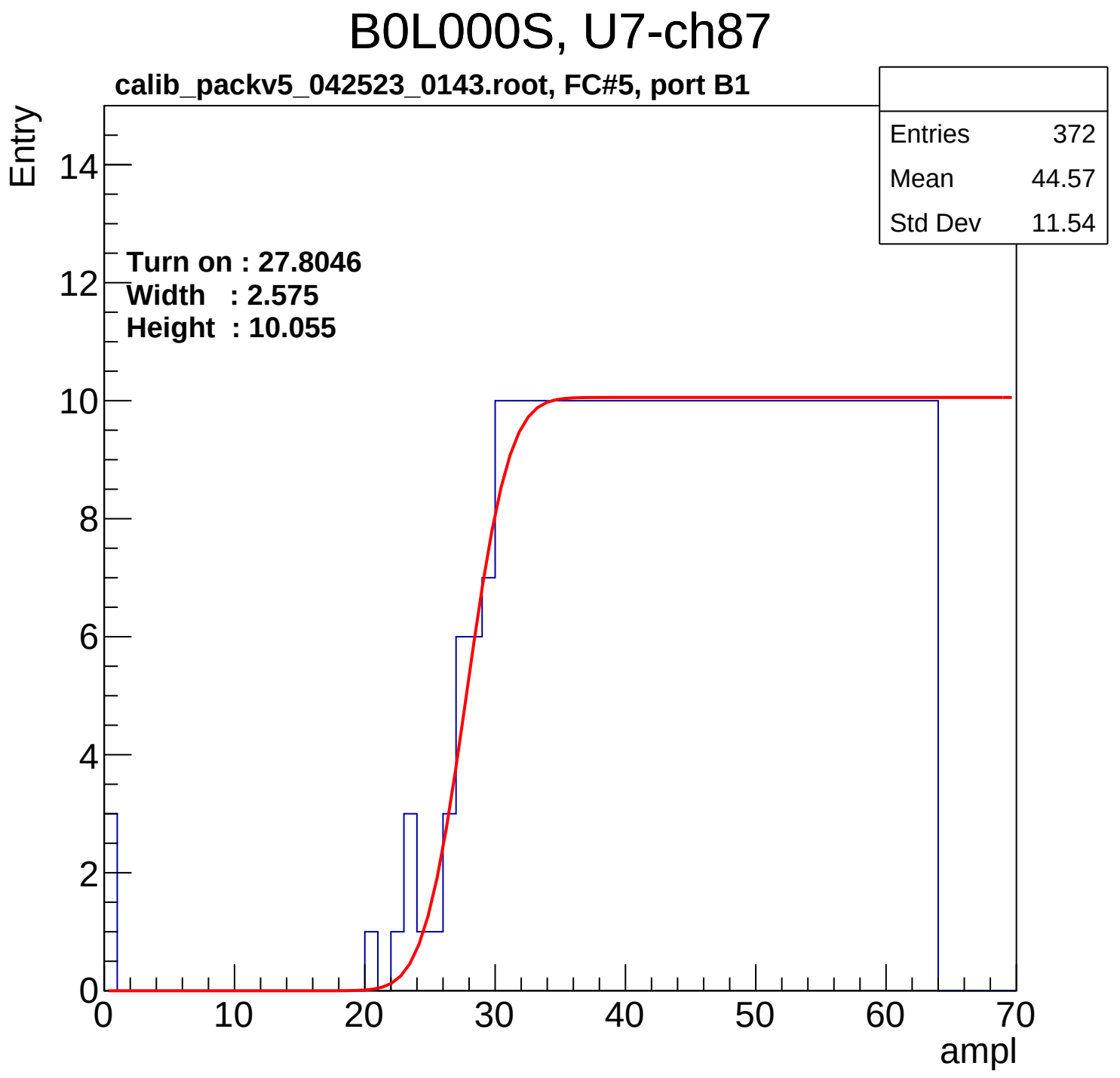
B0L000S, U7-ch87
calib_packv5_042523_0143.root, FC#5, port B1
Entries 372
Mean 44.57
Std Dev 11.54
Turn on : 27.8046
Width : 2.575
Height : 10.055
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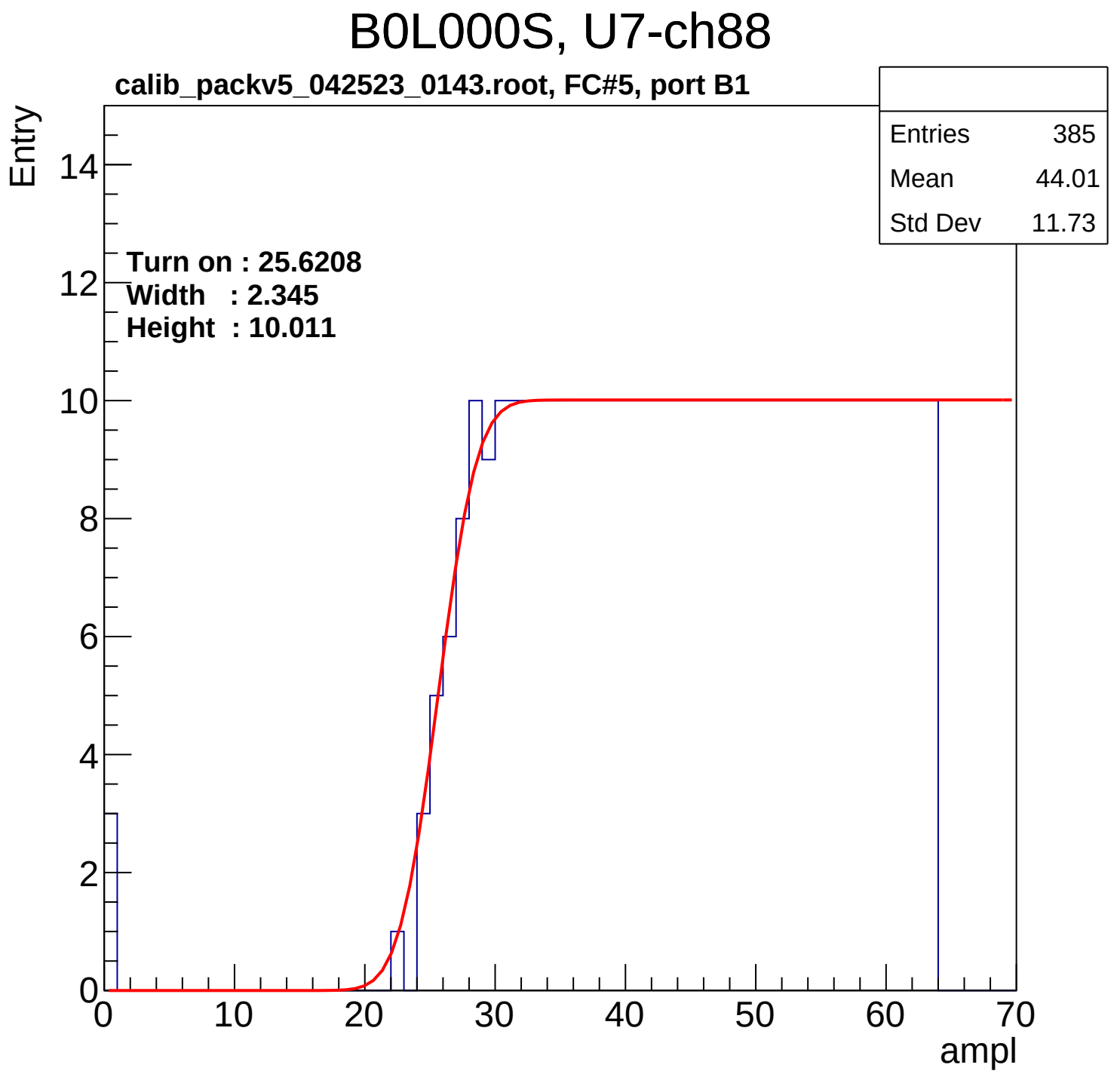
B0L000S, U7-ch88
calib_packv5_042523_0143.root, FC#5, port B1
Entries 385
Mean 44.01
Std Dev 11.73
Turn on : 25.6208
Width : 2.345
Height : 10.011
Entry
ampl
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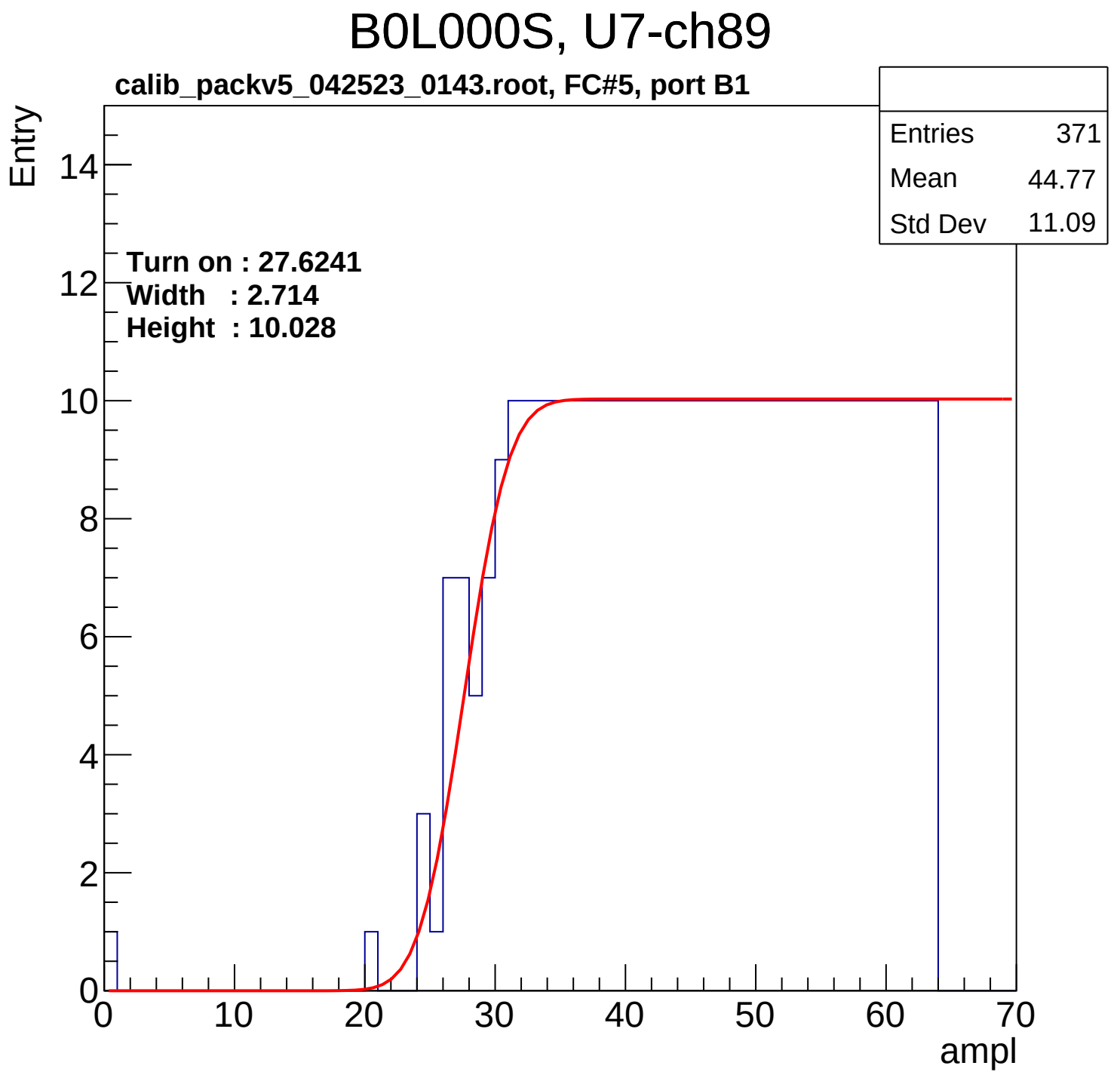
B0L000S, U7-ch89
calib_packv5_042523_0143.root, FC#5, port B1
Entries 371
Mean 44.77
Std Dev 11.09
Turn on : 27.6241
Width : 2.714
Height : 10.028
Entry
ampl
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4
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8
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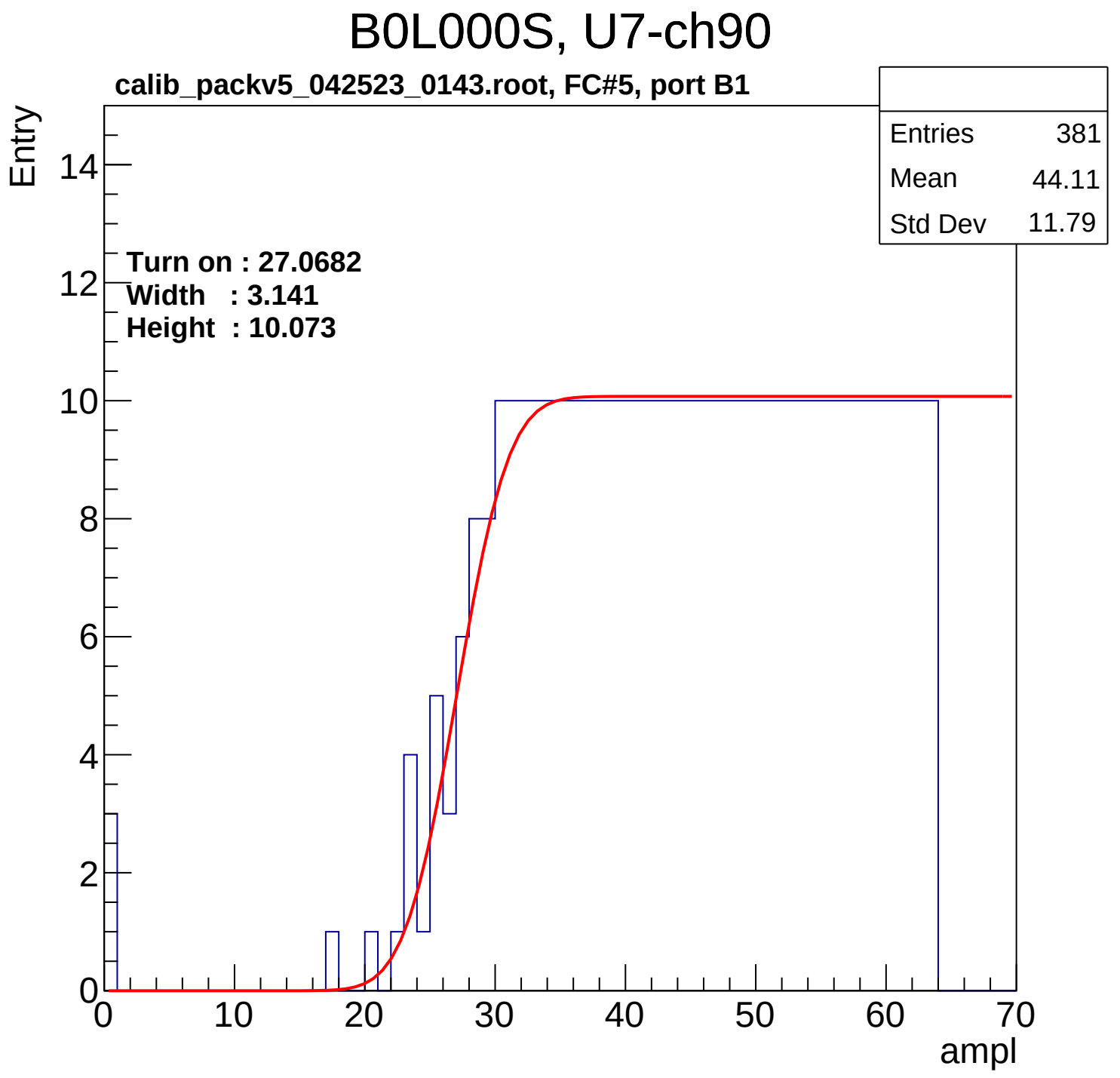
B0L000S, U7-ch90
calib_packv5_042523_0143.root, FC#5, port B1
Entries 381
Mean 44.11
Std Dev 11.79
Turn on : 27.0682
Width : 3.141
Height : 10.073
Entry
ampl
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4
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8
10
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14
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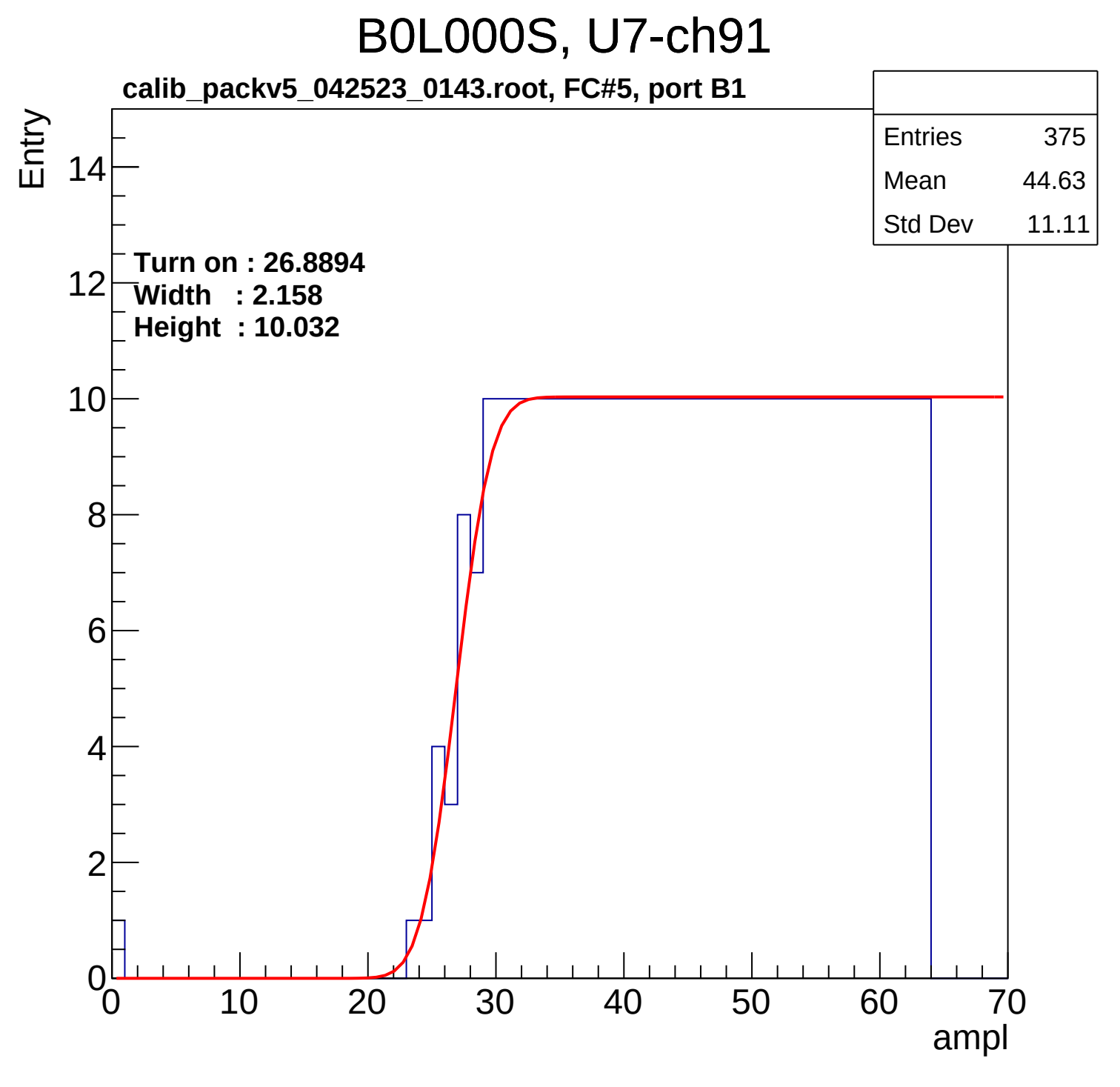
B0L000S, U7-ch91
calib_packv5_042523_0143.root, FC#5, port B1
Entries 375
Mean 44.63
Std Dev 11.11
Turn on : 26.8894
Width : 2.158
Height : 10.032
Entry
ampl
0
2
4
6
8
10
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0
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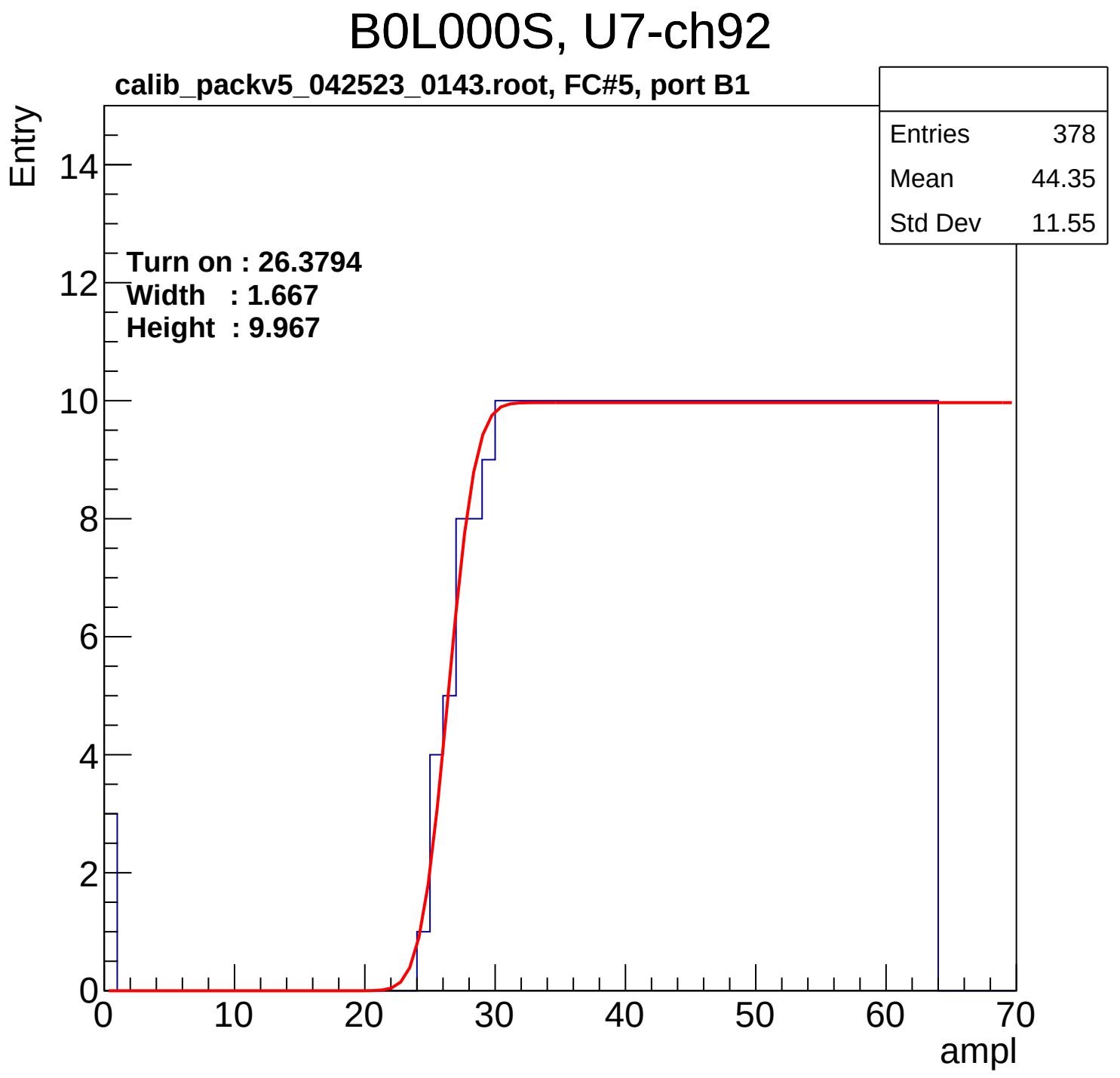
B0L000S, U7-ch92
calib_packv5_042523_0143.root, FC#5, port B1
Entries 378
Mean 44.35
Std Dev 11.55
Turn on : 26.3794
Width : 1.667
Height : 9.967
Entry
ampl
0
2
4
6
8
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12
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0
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40
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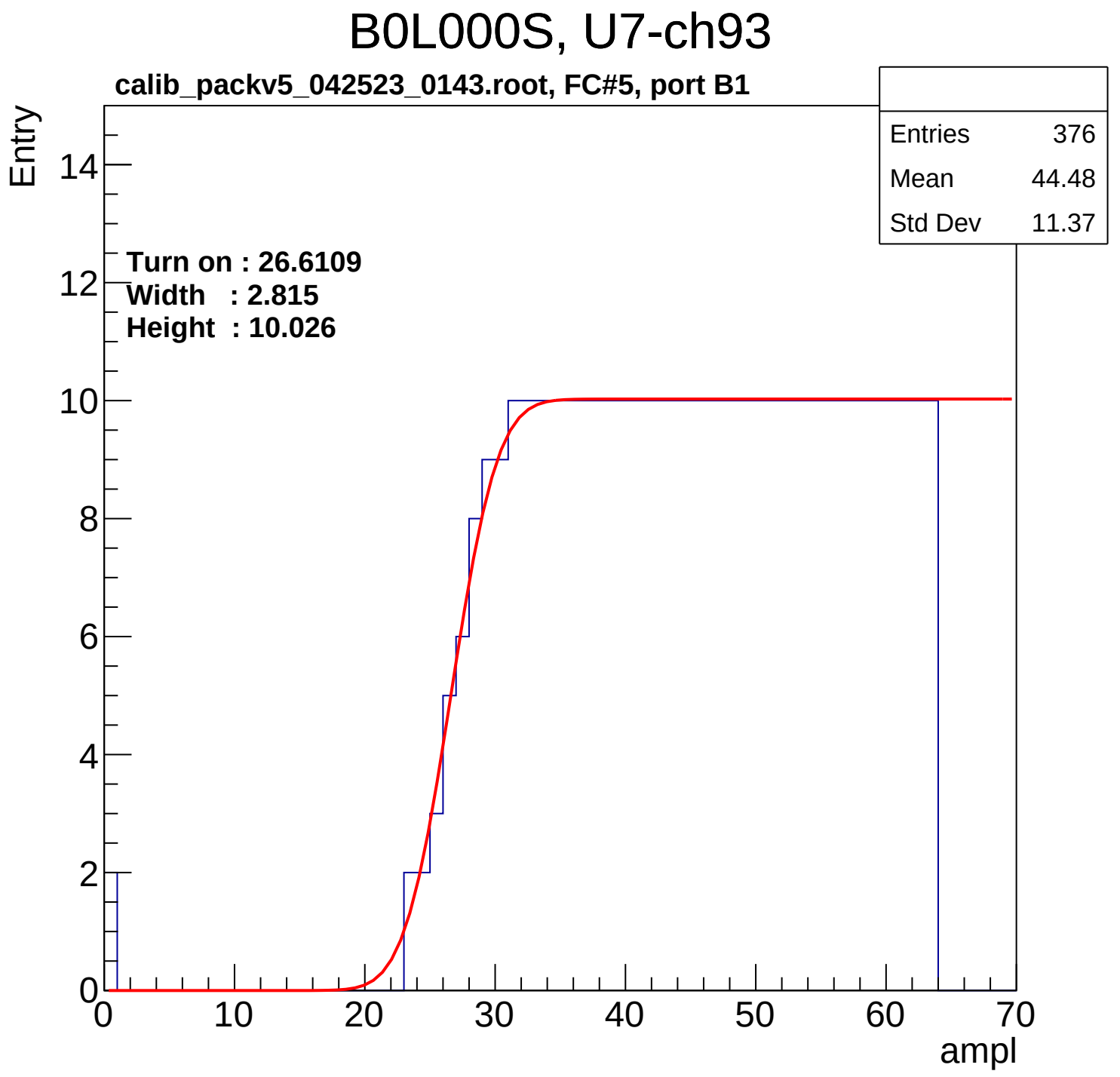
B0L000S, U7-ch93
calib_packv5_042523_0143.root, FC#5, port B1
Entries 376
Mean 44.48
Std Dev 11.37
Turn on : 26.6109
Width : 2.815
Height : 10.026
Entry
ampl
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2
4
6
8
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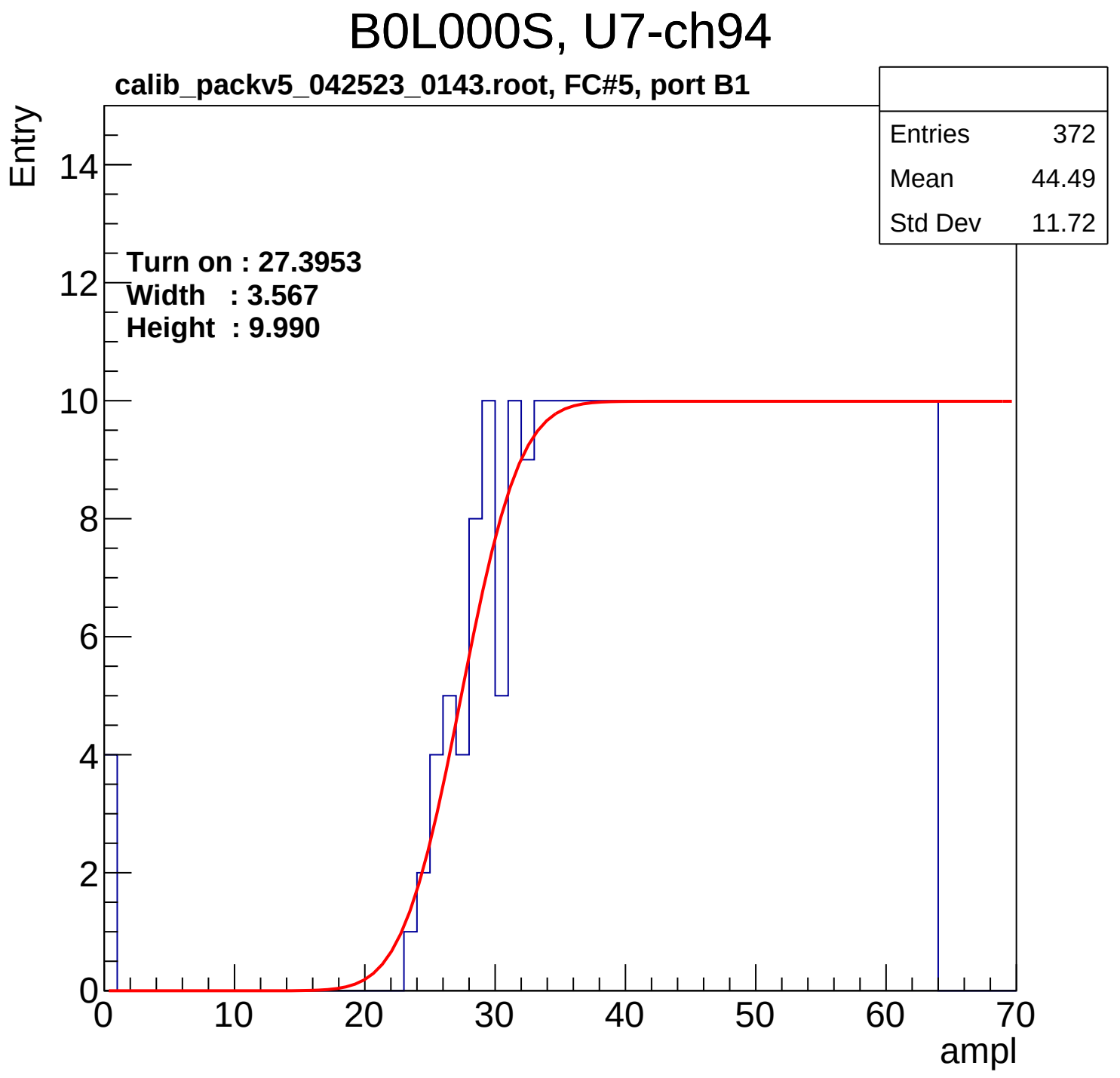
B0L000S, U7-ch94
calib_packv5_042523_0143.root, FC#5, port B1
Entries 372
Mean 44.49
Std Dev 11.72
Turn on : 27.3953
Width : 3.567
Height : 9.990
Entry
ampl
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2
4
6
8
10
12
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0
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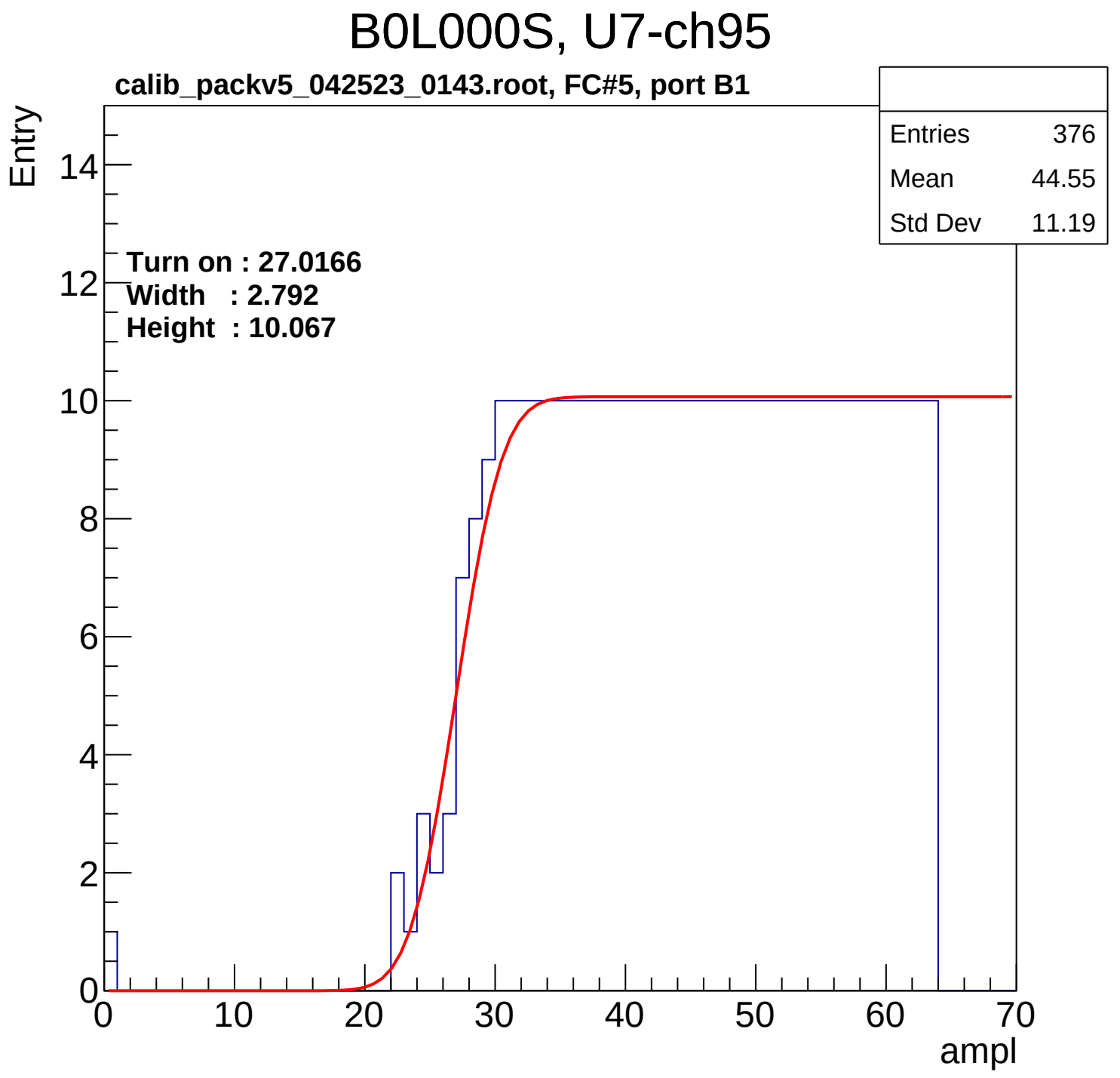
B0L000S, U7-ch95
calib_packv5_042523_0143.root, FC#5, port B1
Entries 376
Mean 44.55
Std Dev 11.19
Turn on : 27.0166
Width : 2.792
Height : 10.067
Entry
ampl
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2
4
6
8
10
12
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0
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20
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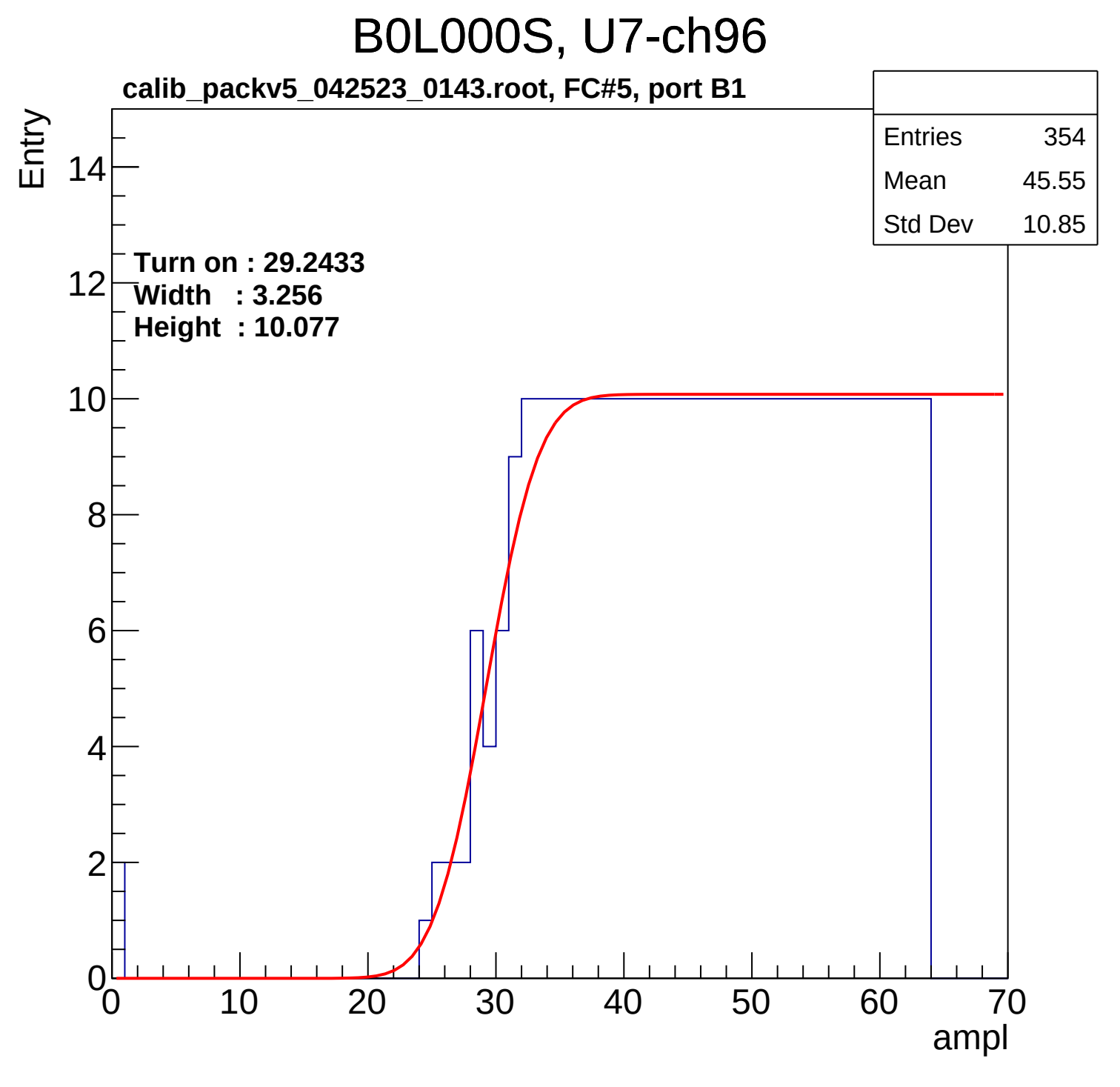
B0L000S, U7-ch96
calib_packv5_042523_0143.root, FC#5, port B1
Entries 354
Mean 45.55
Std Dev 10.85
Turn on : 29.2433
Width : 3.256
Height : 10.077
Entry
ampl
0
2
4
6
8
10
12
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0
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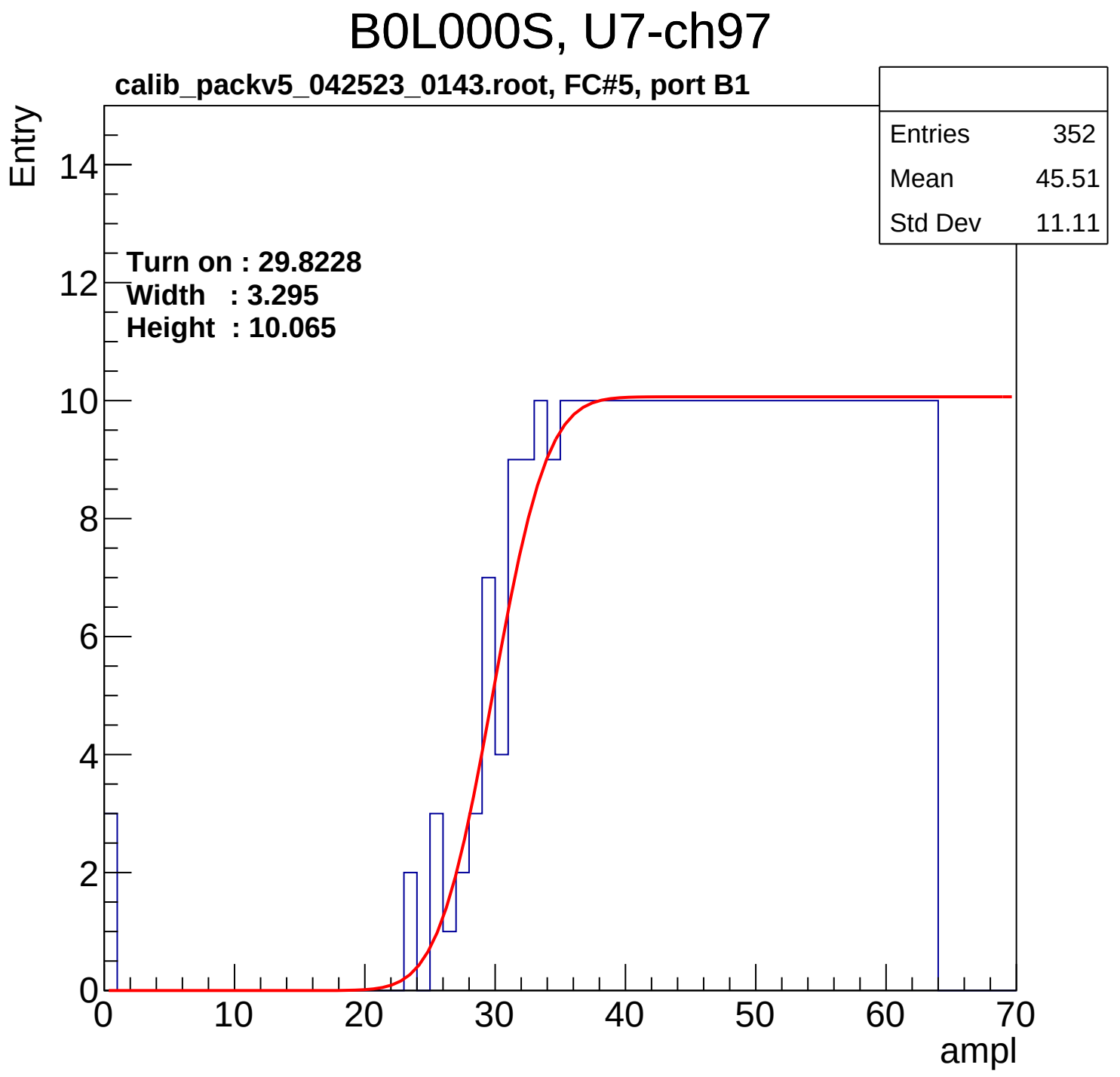
B0L000S, U7-ch97
calib_packv5_042523_0143.root, FC#5, port B1
Entries 352
Mean 45.51
Std Dev 11.11
Turn on : 29.8228
Width : 3.295
Height : 10.065
Entry
ampl
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8
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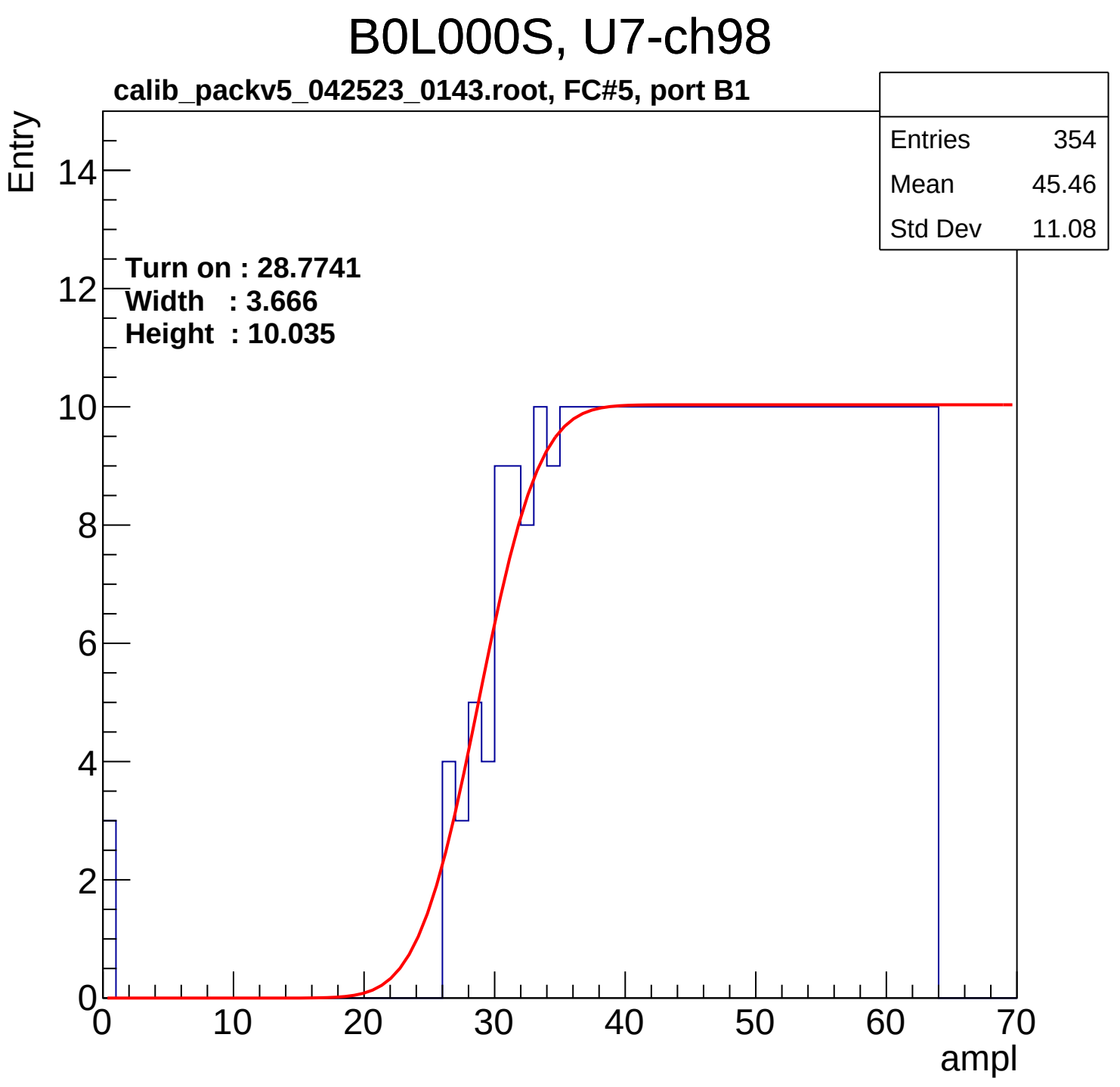
B0L000S, U7-ch98
calib_packv5_042523_0143.root, FC#5, port B1
Entries 354
Mean 45.46
Std Dev 11.08
Turn on : 28.7741
Width : 3.666
Height : 10.035
Entry
ampl
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6
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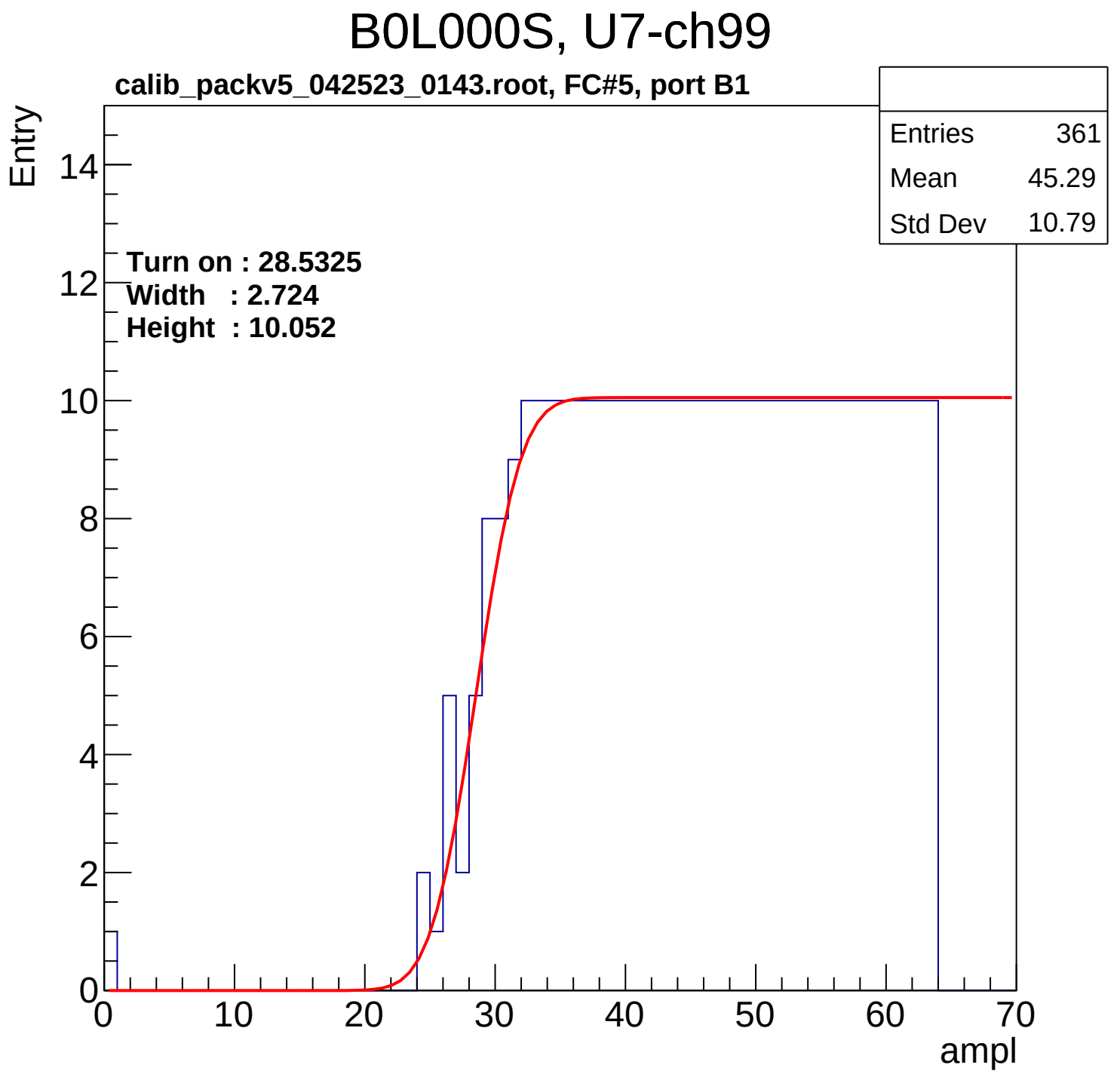
B0L000S, U7-ch99
calib_packv5_042523_0143.root, FC#5, port B1
Entries 361
Mean 45.29
Std Dev 10.79
Turn on : 28.5325
Width : 2.724
Height : 10.052
Entry
ampl
0
2
4
6
8
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12
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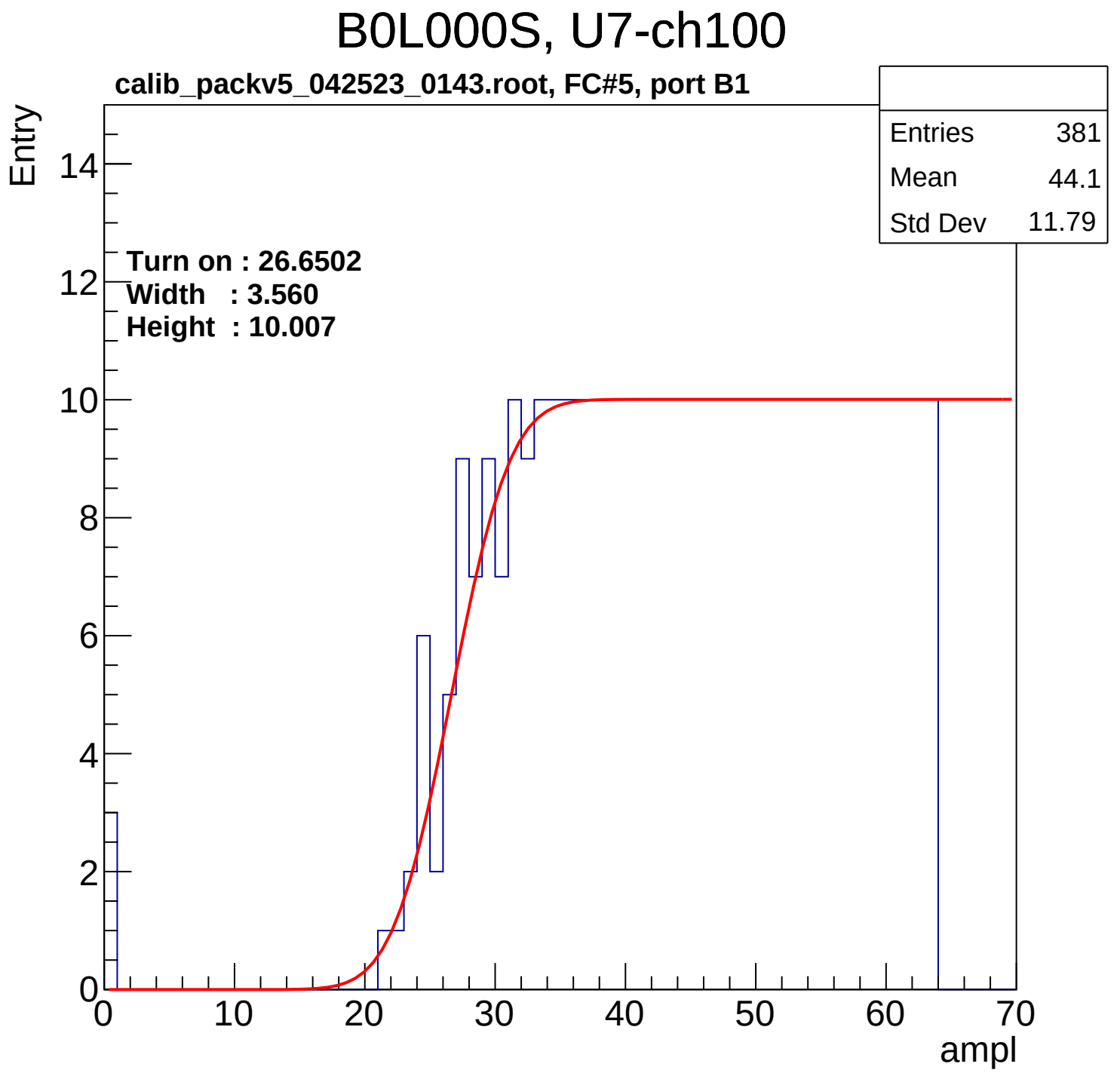
B0L000S, U7-ch100
calib_packv5_042523_0143.root, FC#5, port B1
Entries 381
Mean 44.1
Std Dev 11.79
Turn on : 26.6502
Width : 3.560
Height : 10.007
Entry
ampl
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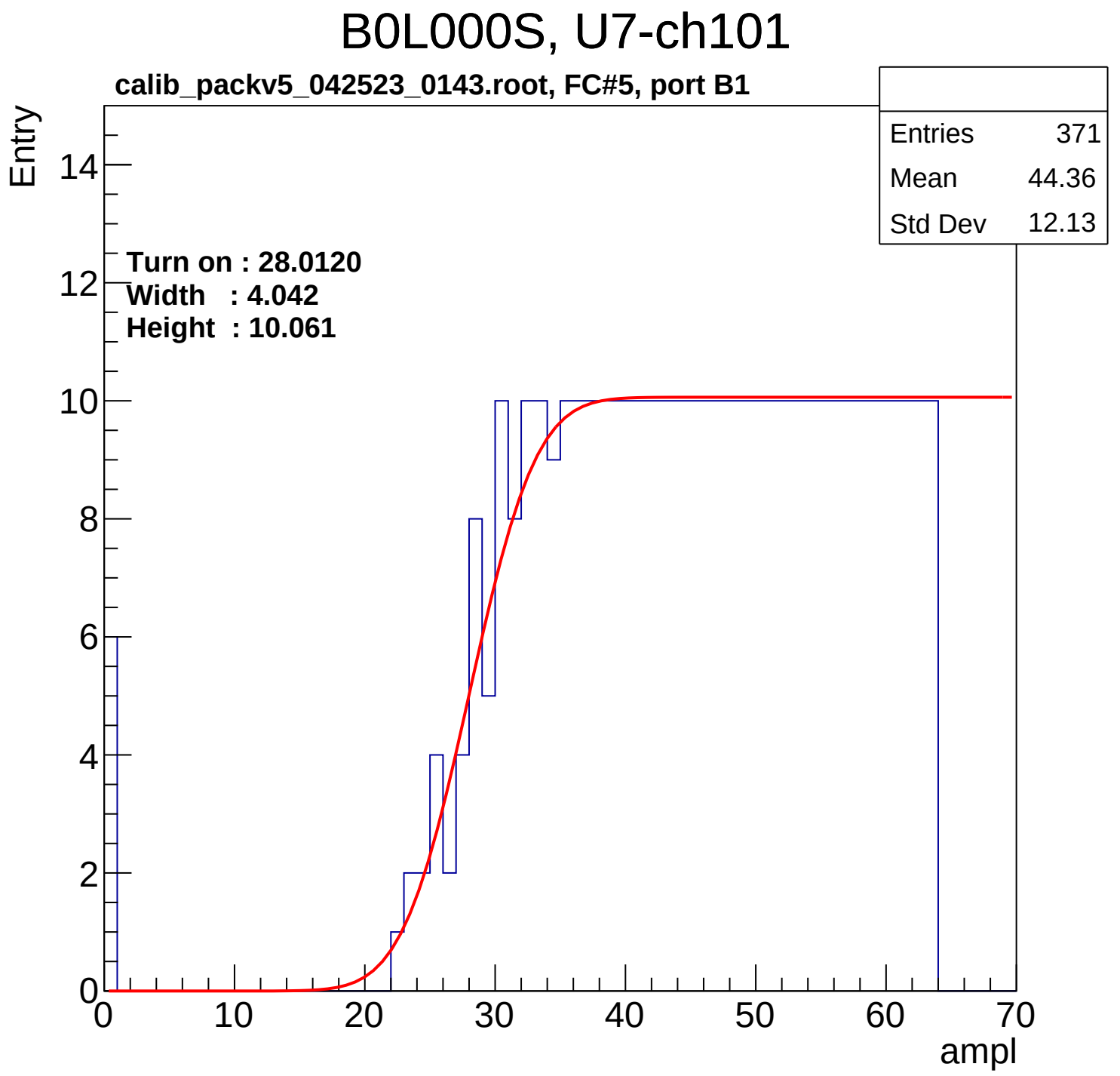
B0L000S, U7-ch101
calib_packv5_042523_0143.root, FC#5, port B1
Entries 371
Mean 44.36
Std Dev 12.13
Turn on : 28.0120
Width : 4.042
Height : 10.061
Entry
ampl
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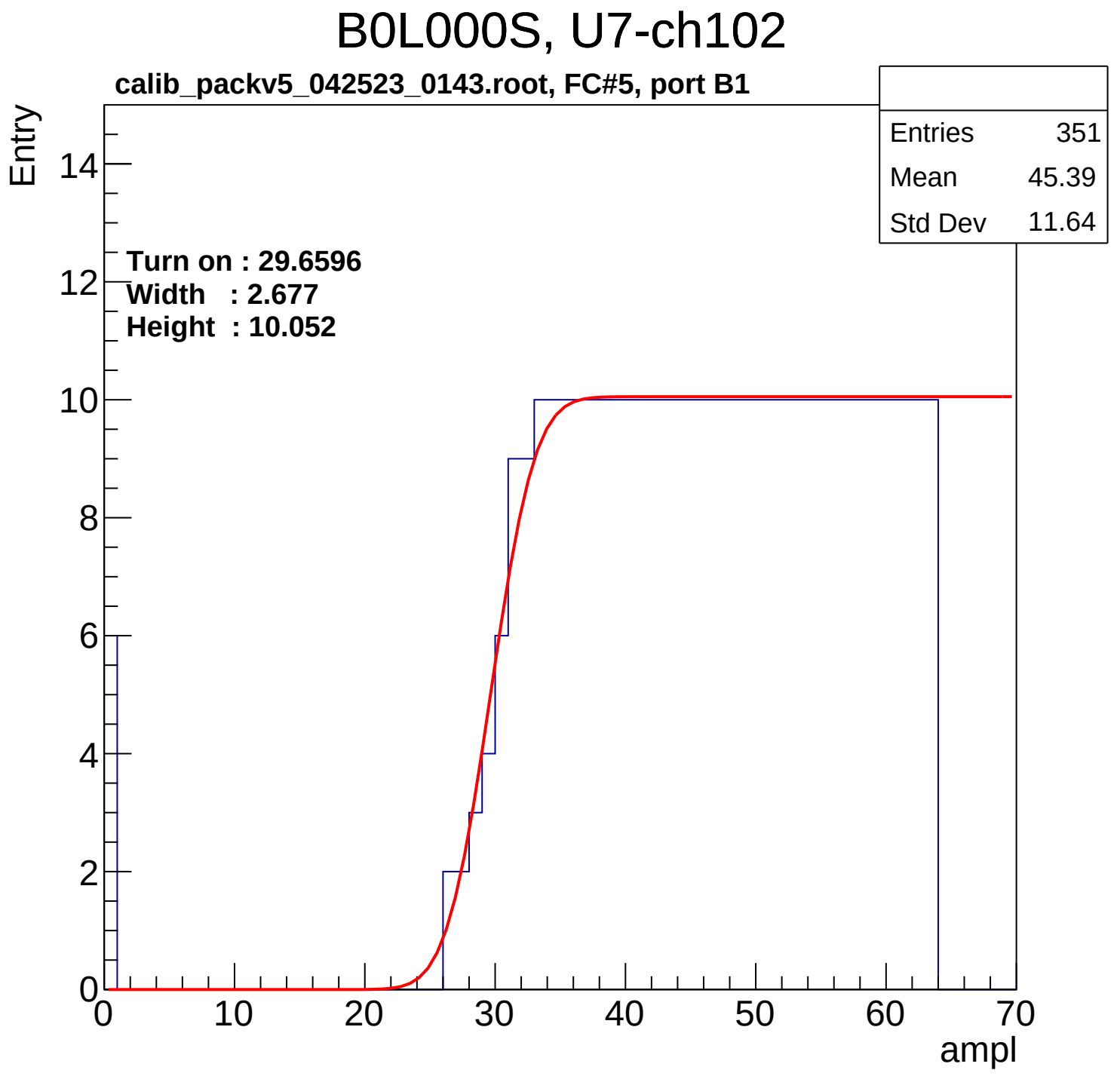
B0L000S, U7-ch102
calib_packv5_042523_0143.root, FC#5, port B1
Entries 351
Mean 45.39
Std Dev 11.64
Turn on : 29.6596
Width : 2.677
Height : 10.052
Entry
ampl
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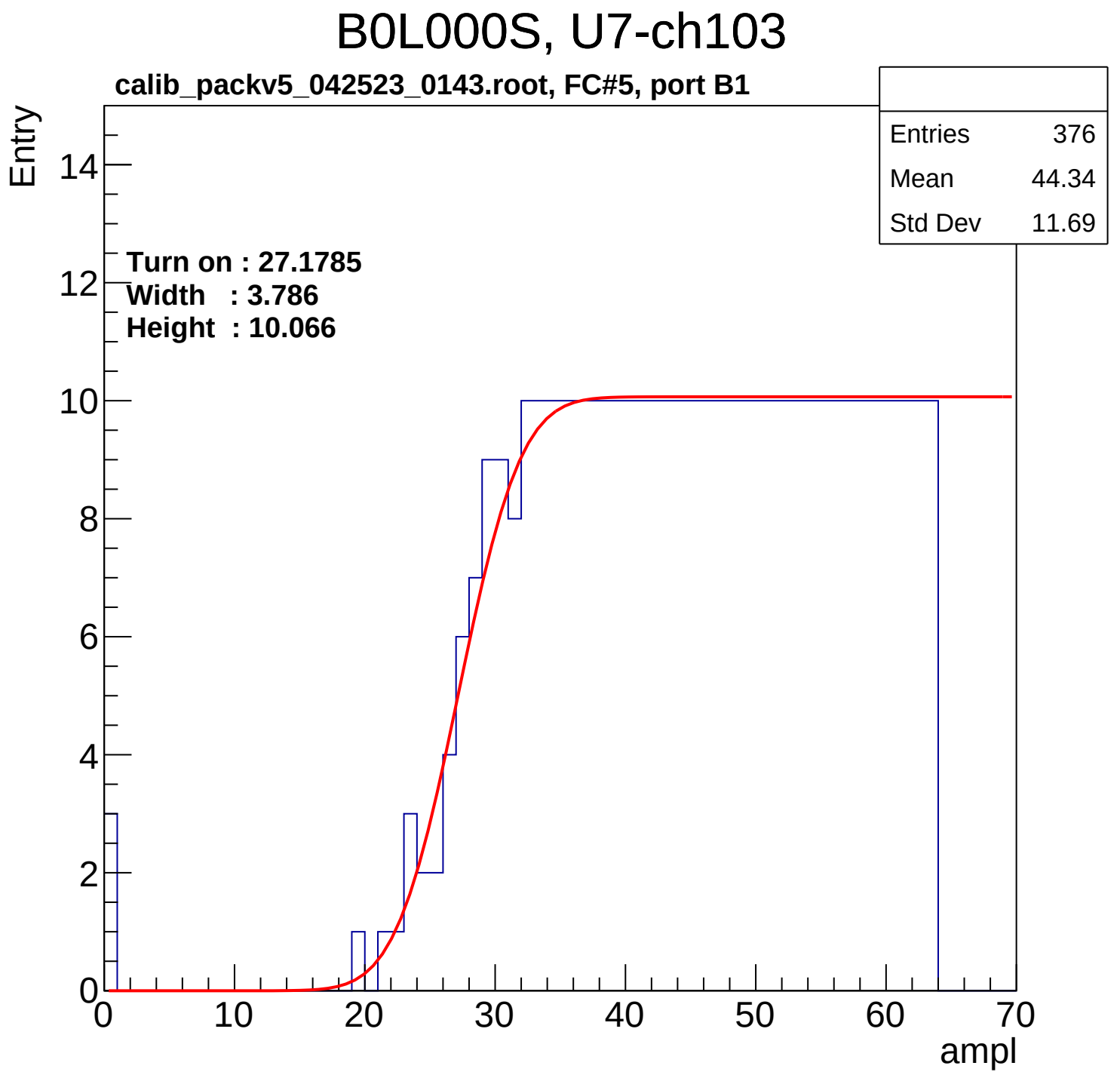
B0L000S, U7-ch103
calib_packv5_042523_0143.root, FC#5, port B1
Entries 376
Mean 44.34
Std Dev 11.69
Turn on : 27.1785
Width : 3.786
Height : 10.066
Entry
ampl
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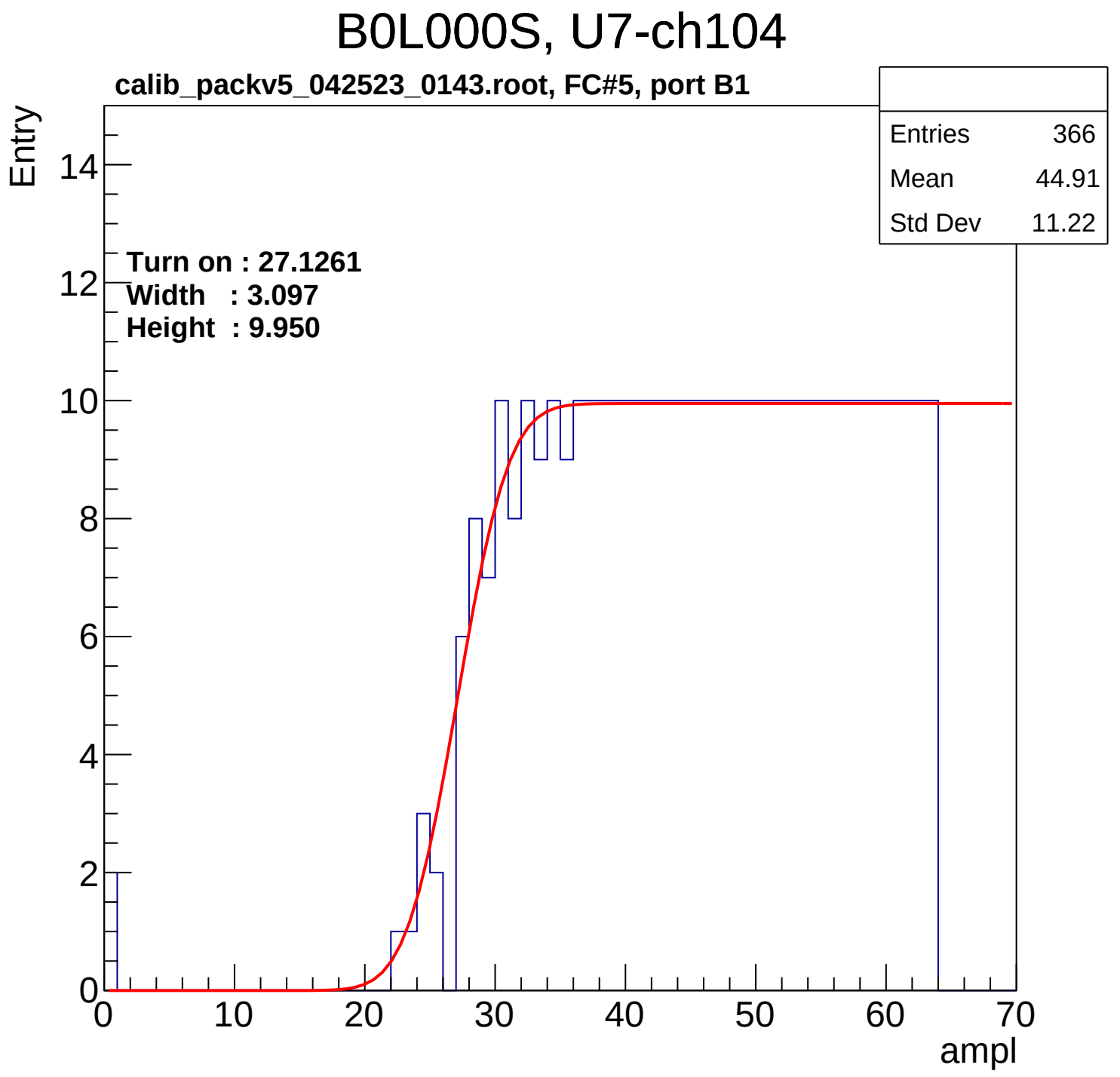
B0L000S, U7-ch104
calib_packv5_042523_0143.root, FC#5, port B1
Entries 366
Mean 44.91
Std Dev 11.22
Turn on : 27.1261
Width : 3.097
Height : 9.950
Entry
ampl
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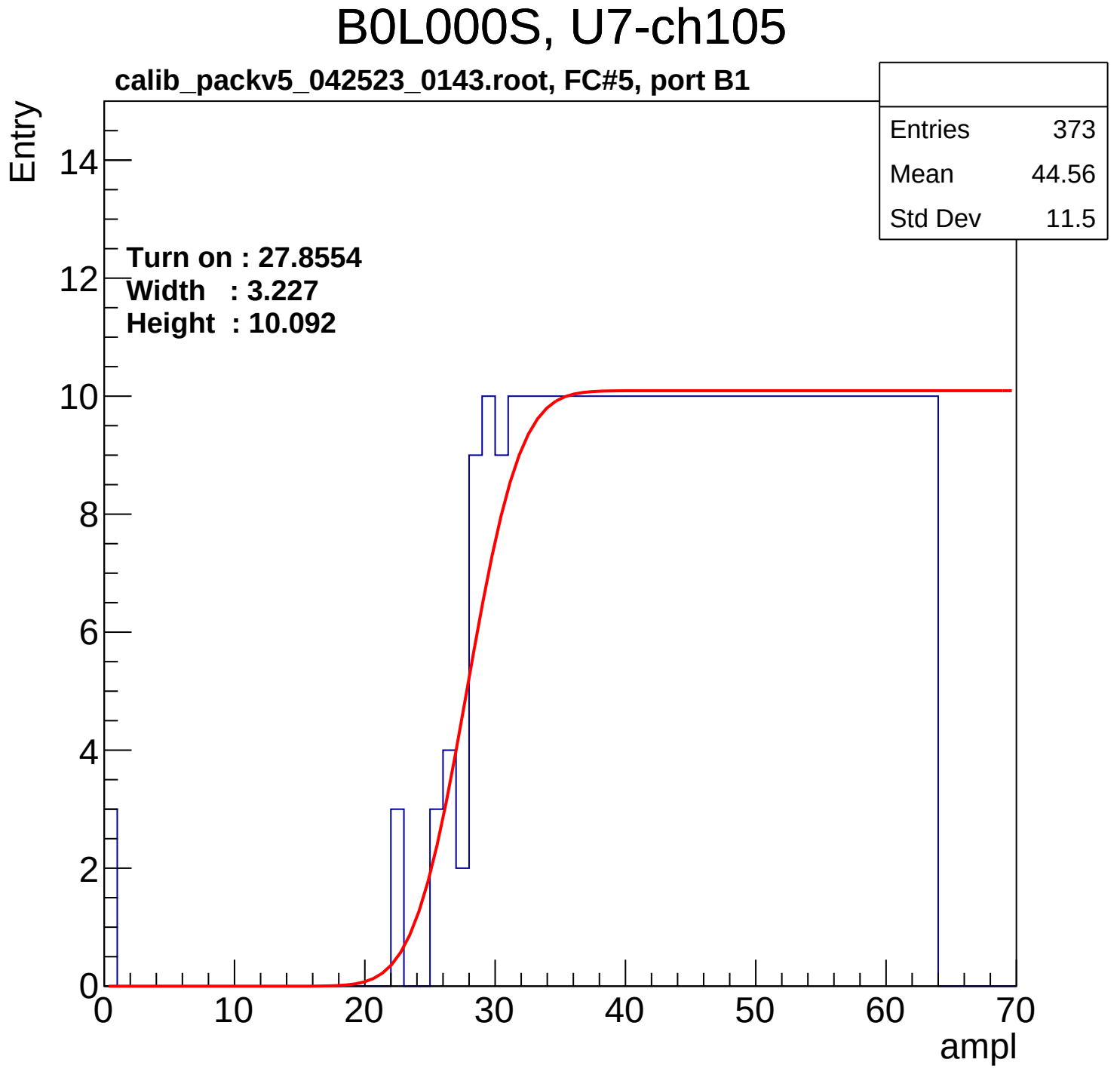
B0L000S, U7-ch105
calib_packv5_042523_0143.root, FC#5, port B1
Entries 373
Mean 44.56
Std Dev 11.5
Turn on : 27.8554
Width : 3.227
Height : 10.092
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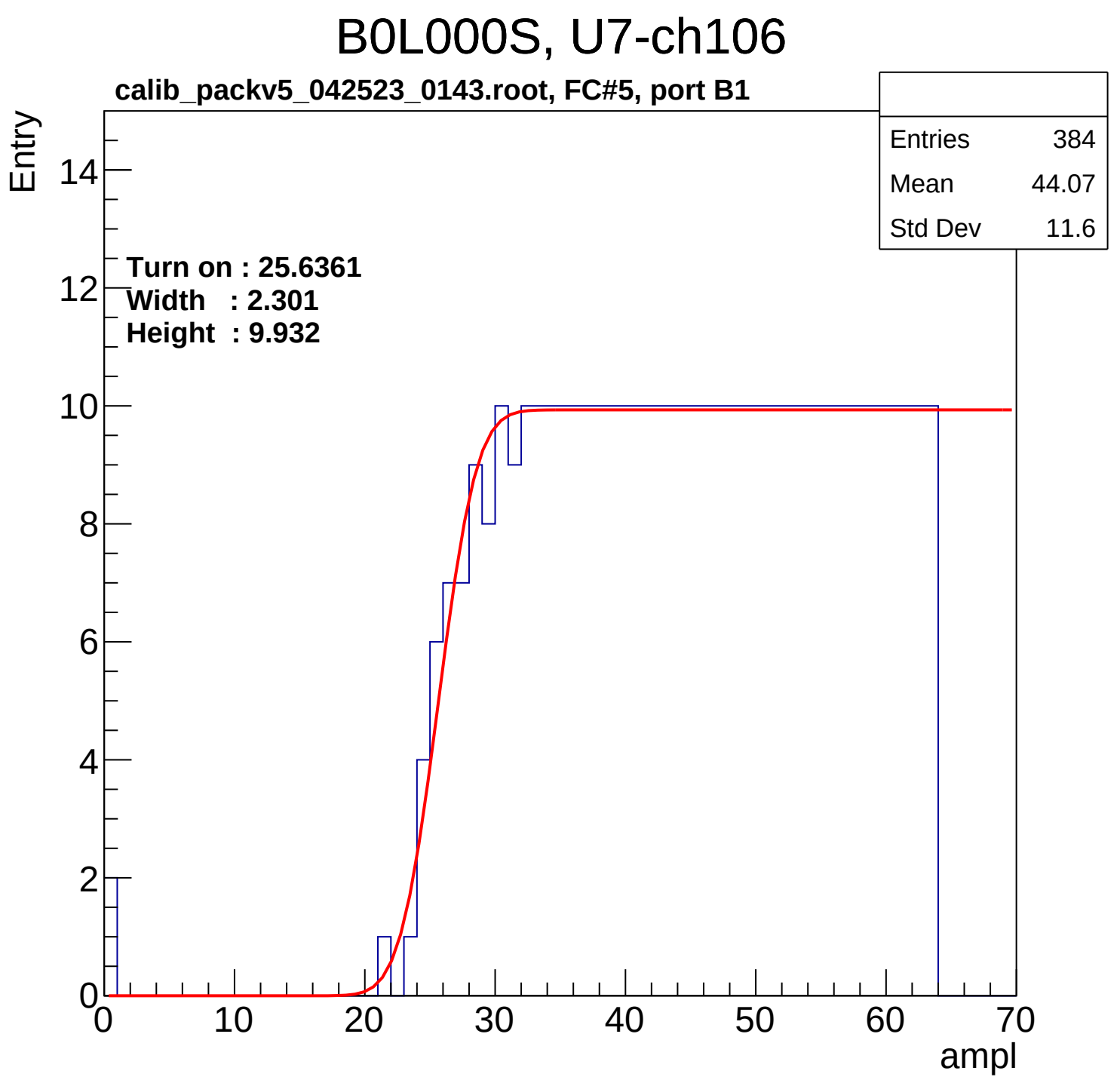
B0L000S, U7-ch106
calib_packv5_042523_0143.root, FC#5, port B1
Entries 384
Mean 44.07
Std Dev 11.6
Turn on : 25.6361
Width : 2.301
Height : 9.932
Entry
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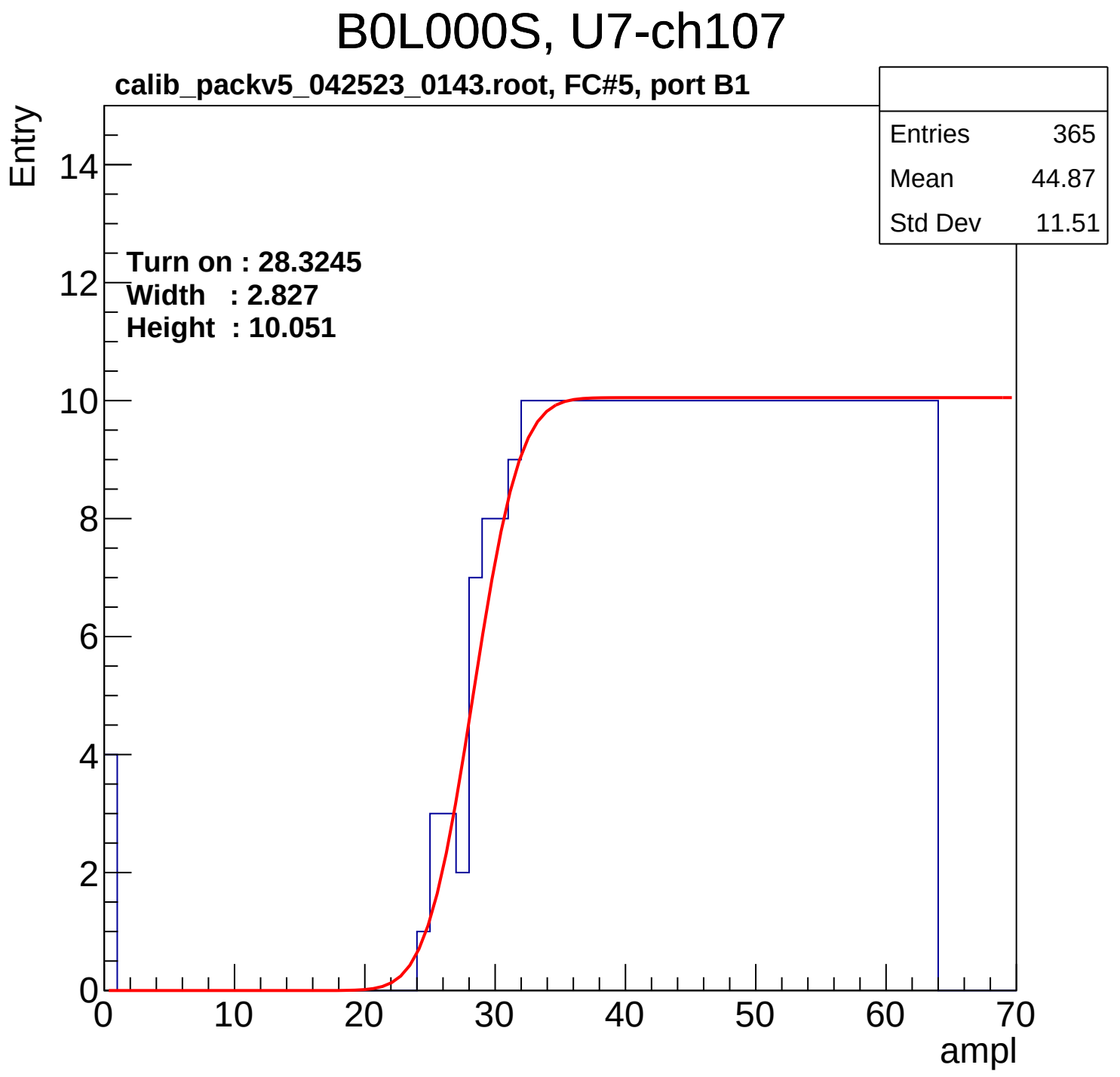
B0L000S, U7-ch107
calib_packv5_042523_0143.root, FC#5, port B1
Entries 365
Mean 44.87
Std Dev 11.51
Turn on : 28.3245
Width : 2.827
Height : 10.051
Entry
ampl
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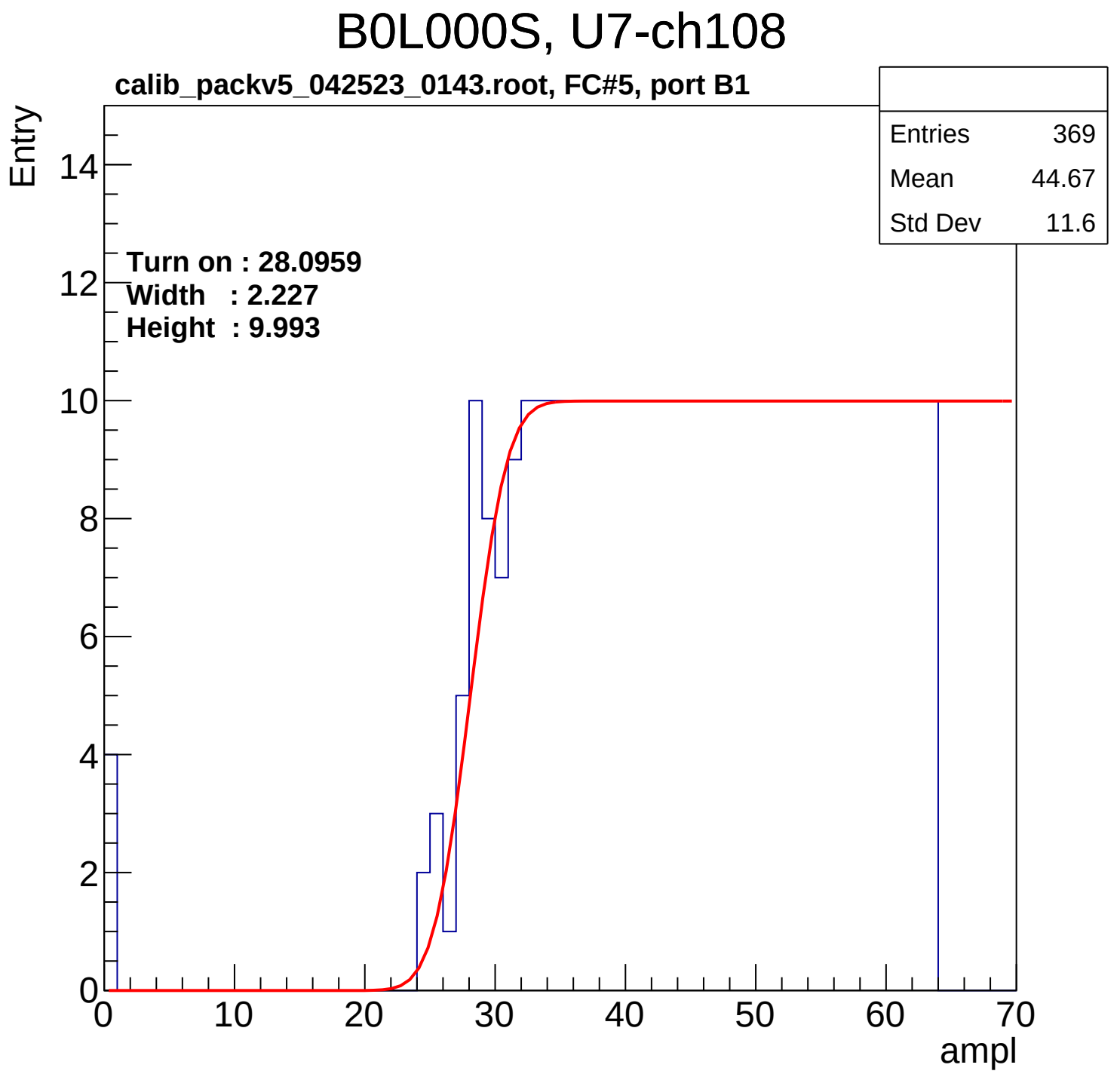
B0L000S, U7-ch108
calib_packv5_042523_0143.root, FC#5, port B1
Entries 369
Mean 44.67
Std Dev 11.6
Turn on : 28.0959
Width : 2.227
Height : 9.993
Entry
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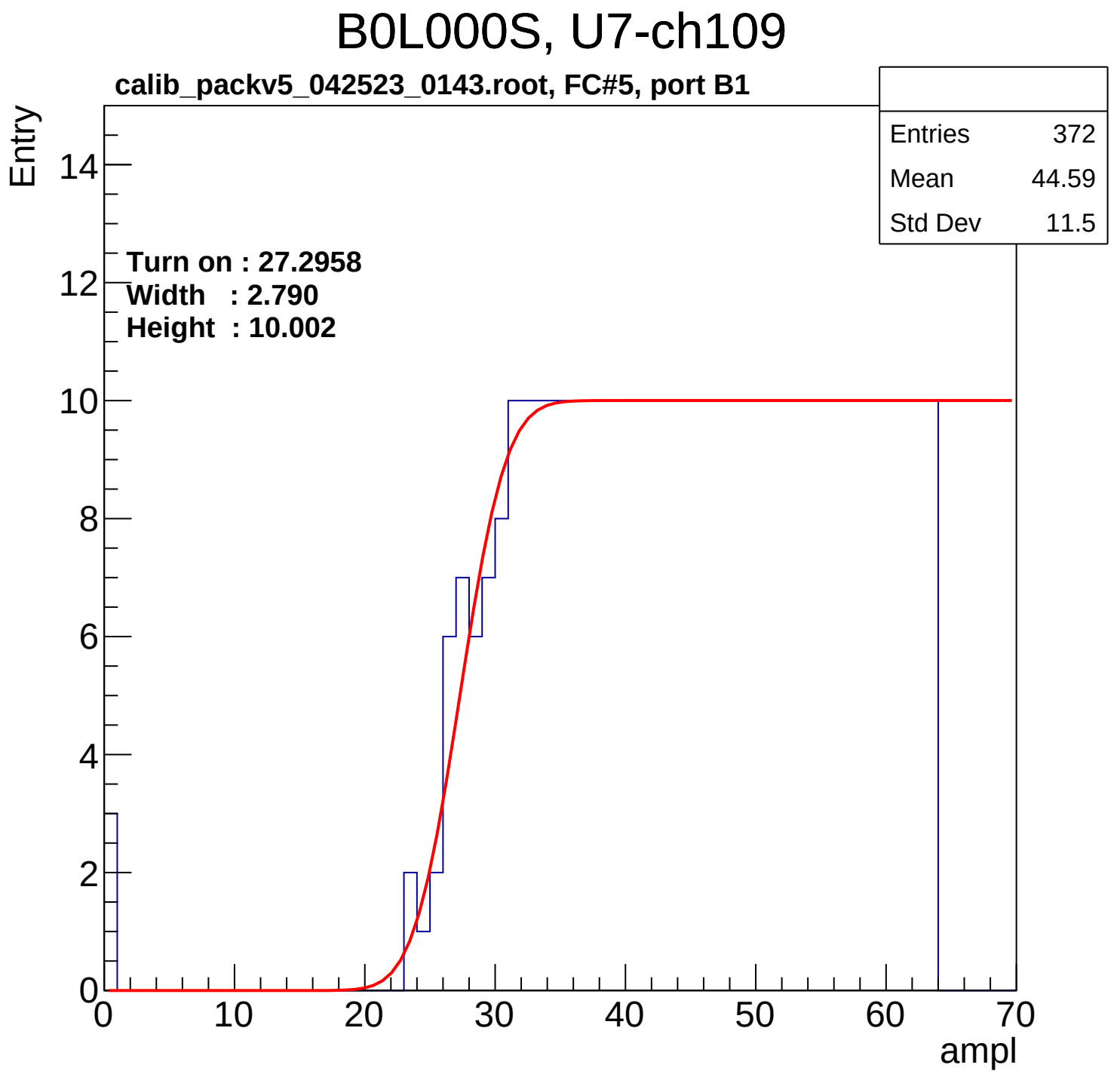
B0L000S, U7-ch109
calib_packv5_042523_0143.root, FC#5, port B1
Entries 372
Mean 44.59
Std Dev 11.5
Turn on : 27.2958
Width : 2.790
Height : 10.002
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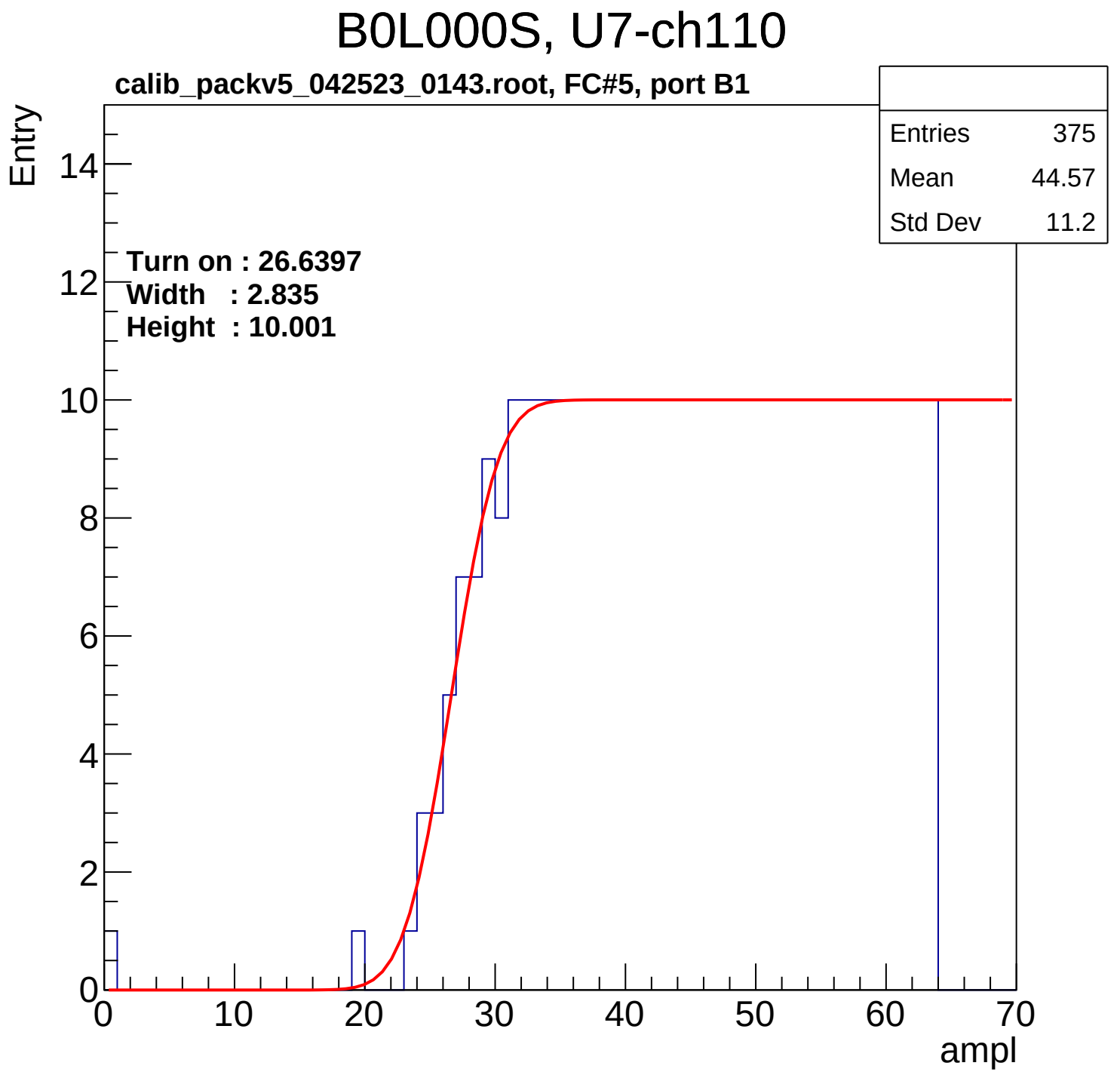
B0L000S, U7-ch110
calib_packv5_042523_0143.root, FC#5, port B1
Entries 375
Mean 44.57
Std Dev 11.2
Turn on : 26.6397
Width : 2.835
Height : 10.001
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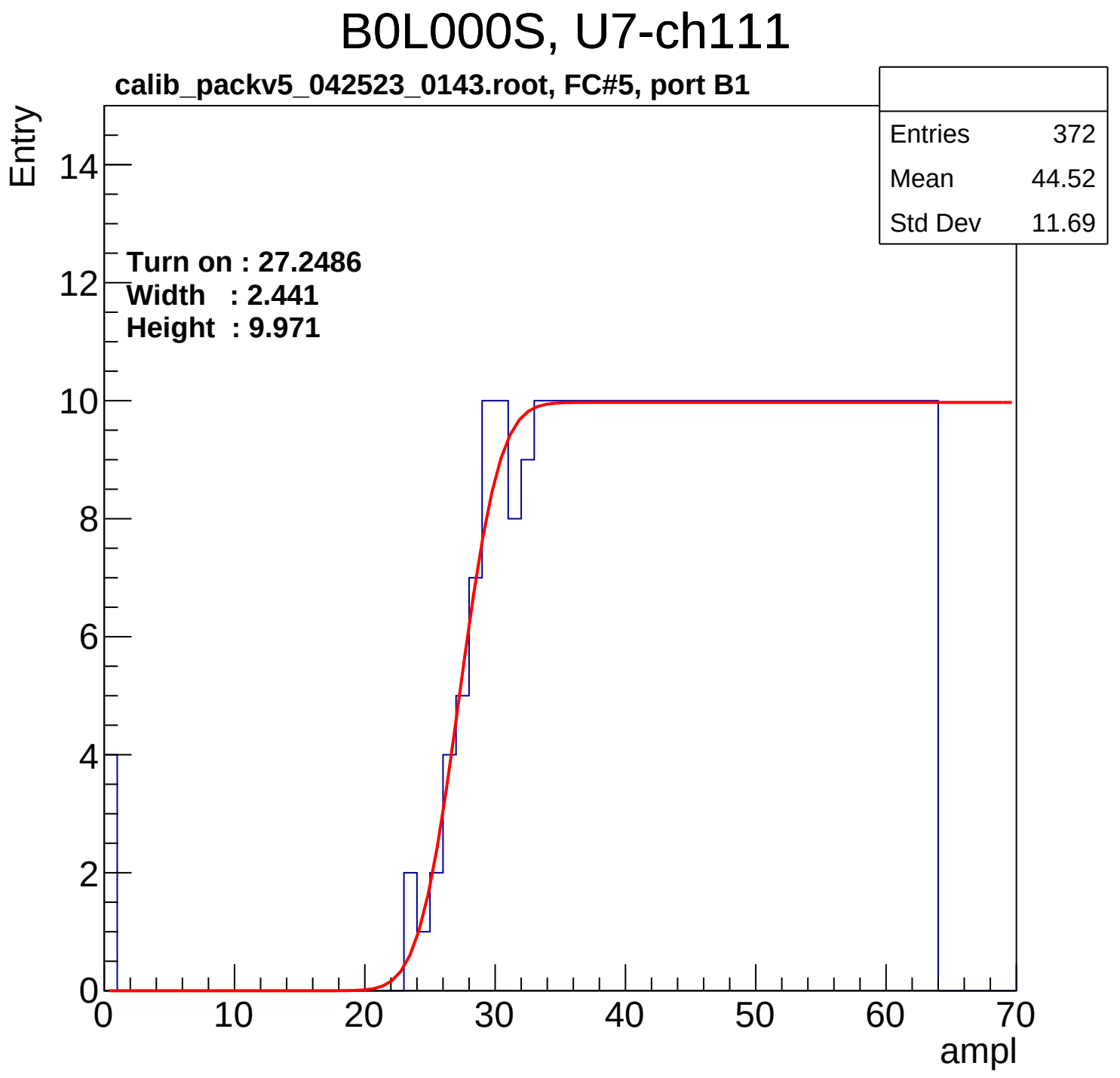
B0L000S, U7-ch111
calib_packv5_042523_0143.root, FC#5, port B1
Entries 372
Mean 44.52
Std Dev 11.69
Turn on : 27.2486
Width : 2.441
Height : 9.971
Entry
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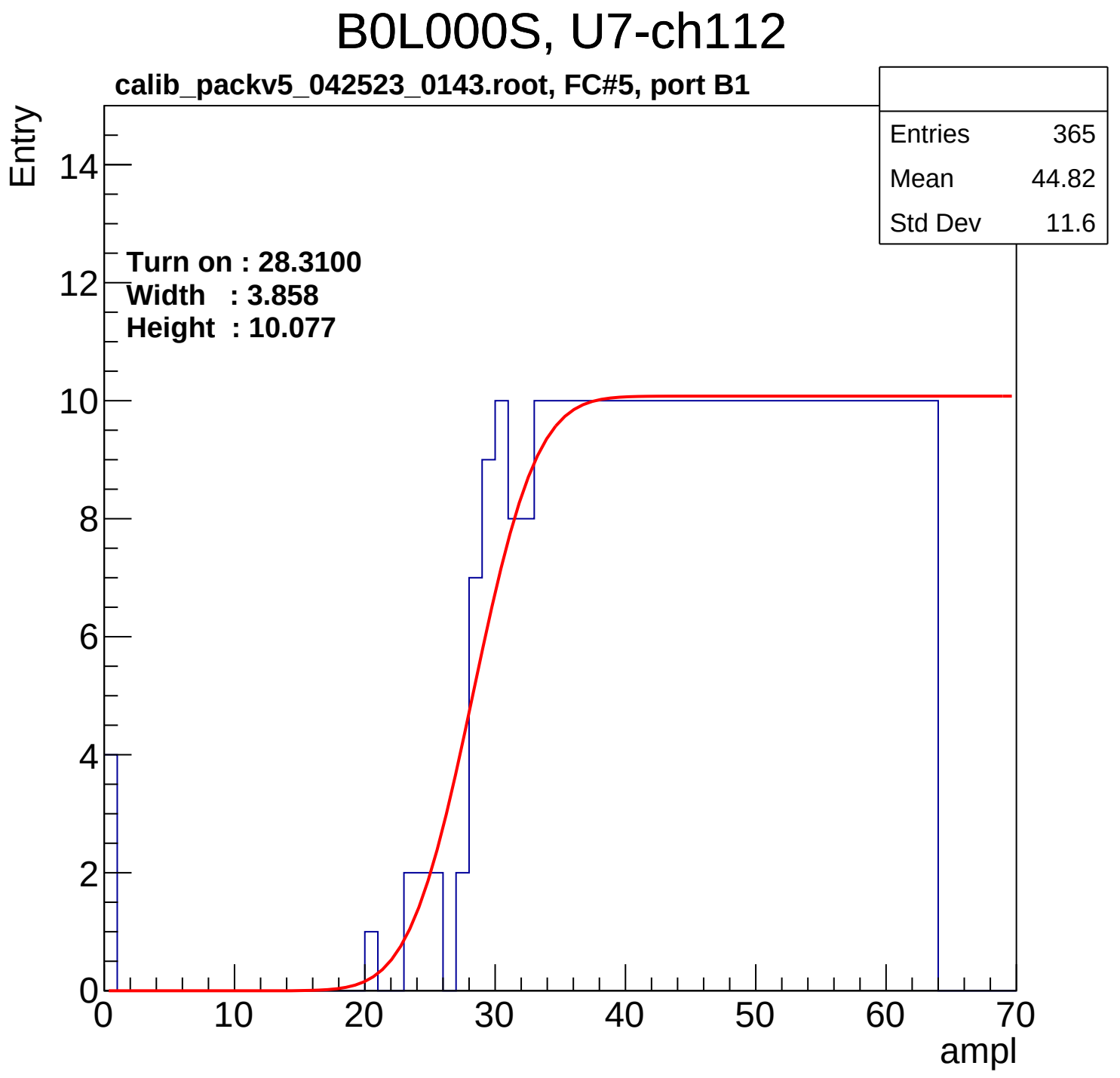
B0L000S, U7-ch112
calib_packv5_042523_0143.root, FC#5, port B1
Entries 365
Mean 44.82
Std Dev 11.6
Turn on : 28.3100
Width : 3.858
Height : 10.077
Entry
ampl
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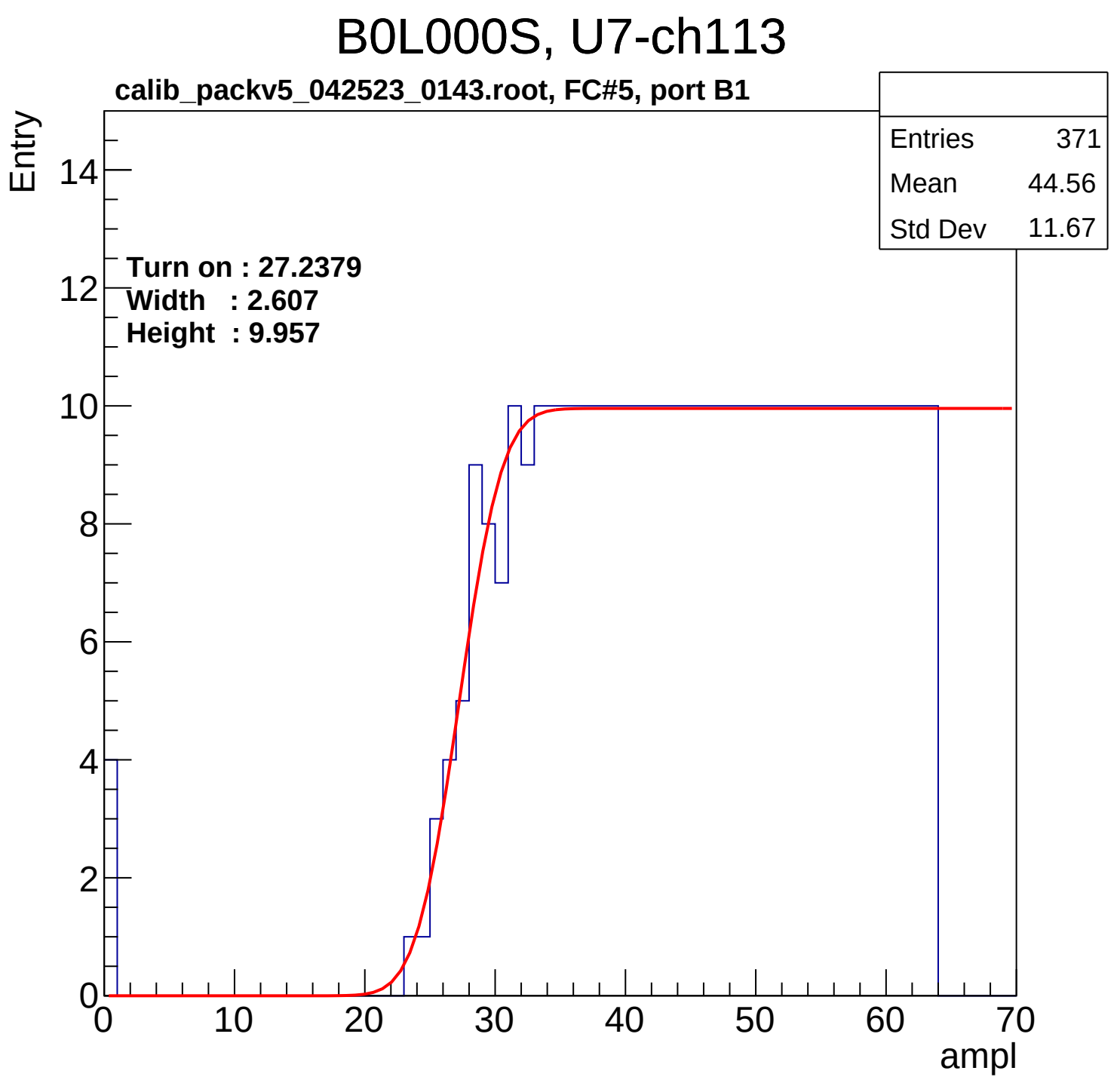
B0L000S, U7-ch113
calib_packv5_042523_0143.root, FC#5, port B1
Entries 371
Mean 44.56
Std Dev 11.67
Turn on : 27.2379
Width : 2.607
Height : 9.957
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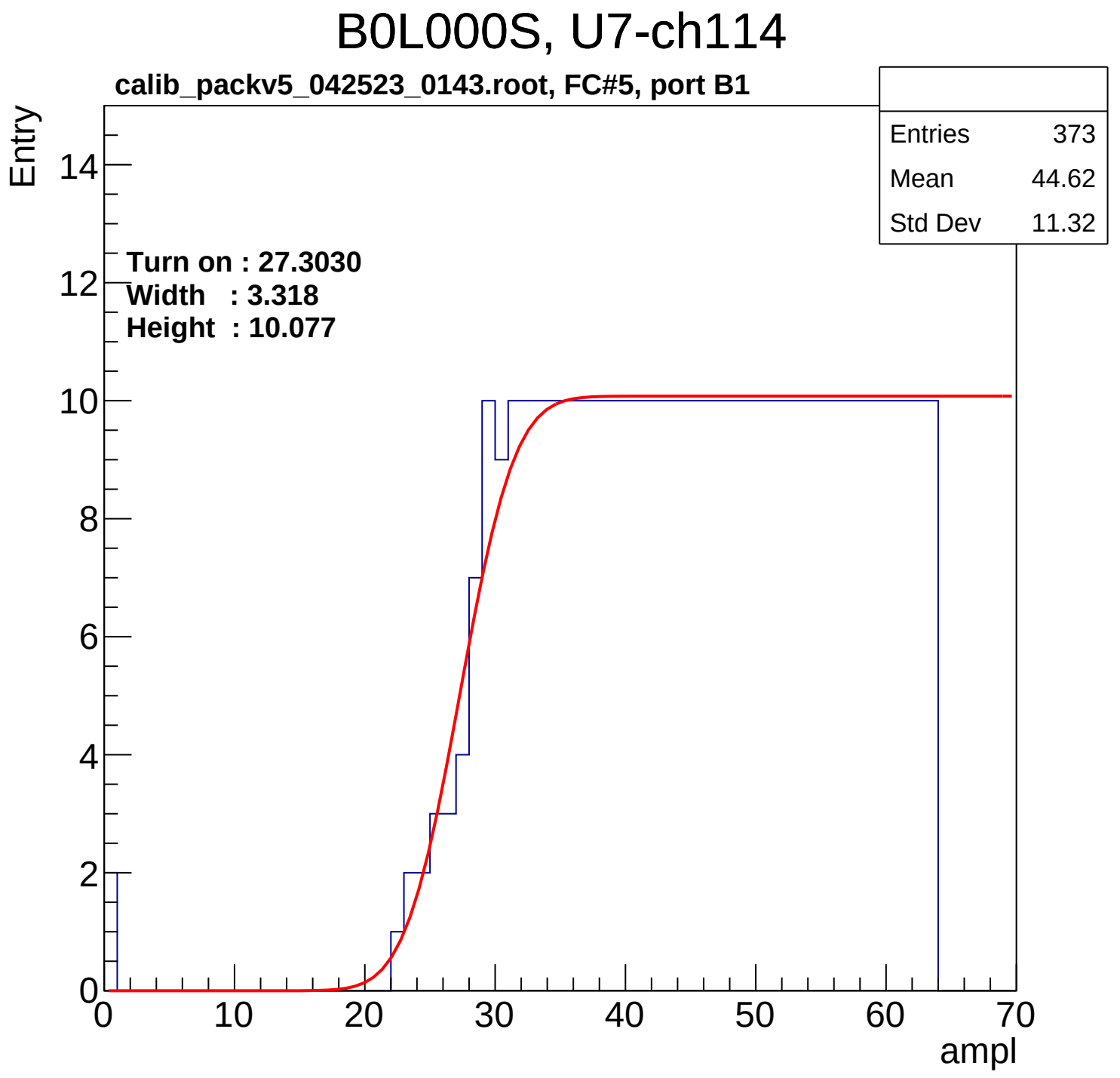
B0L000S, U7-ch114
calib_packv5_042523_0143.root, FC#5, port B1
Entries 373
Mean 44.62
Std Dev 11.32
Turn on : 27.3030
Width : 3.318
Height : 10.077
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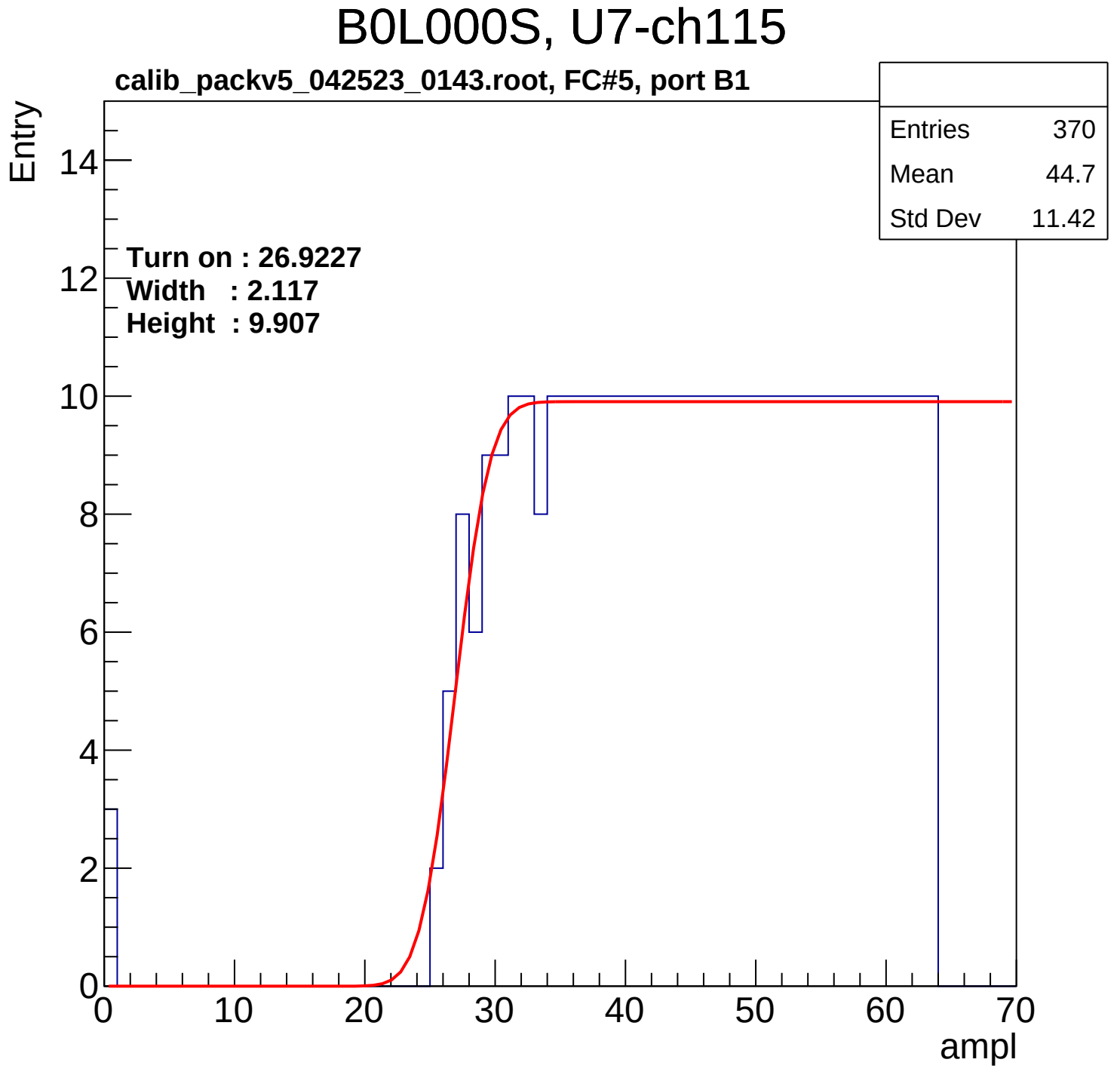
B0L000S, U7-ch115
calib_packv5_042523_0143.root, FC#5, port B1
Entries 370
Mean 44.7
Std Dev 11.42
Turn on : 26.9227
Width : 2.117
Height : 9.907
Entry
ampl
0
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4
6
8
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10
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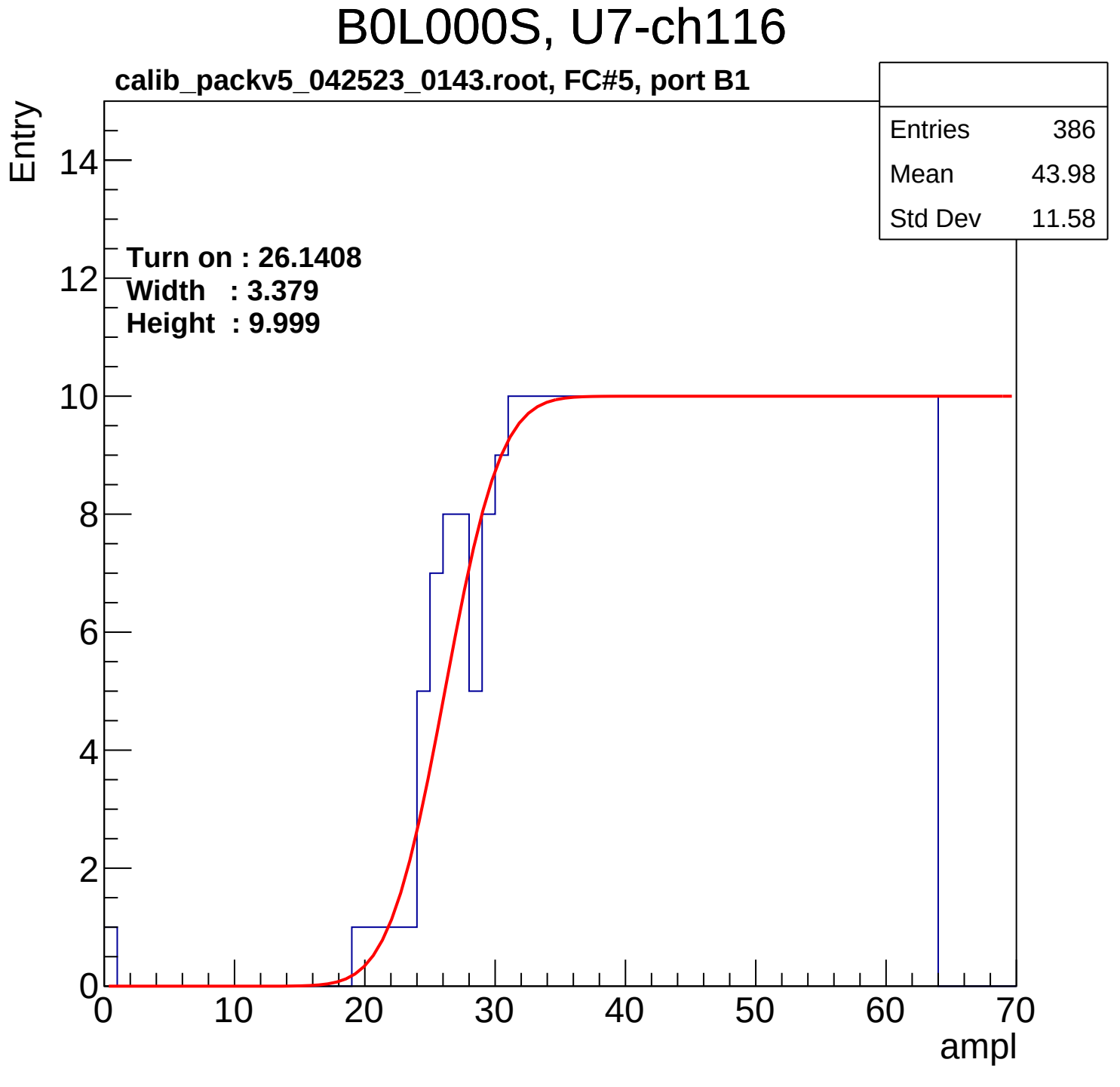
B0L000S, U7-ch116
calib_packv5_042523_0143.root, FC#5, port B1
Entries 386
Mean 43.98
Std Dev 11.58
Turn on : 26.1408
Width : 3.379
Height : 9.999
Entry
ampl
0
2
4
6
8
10
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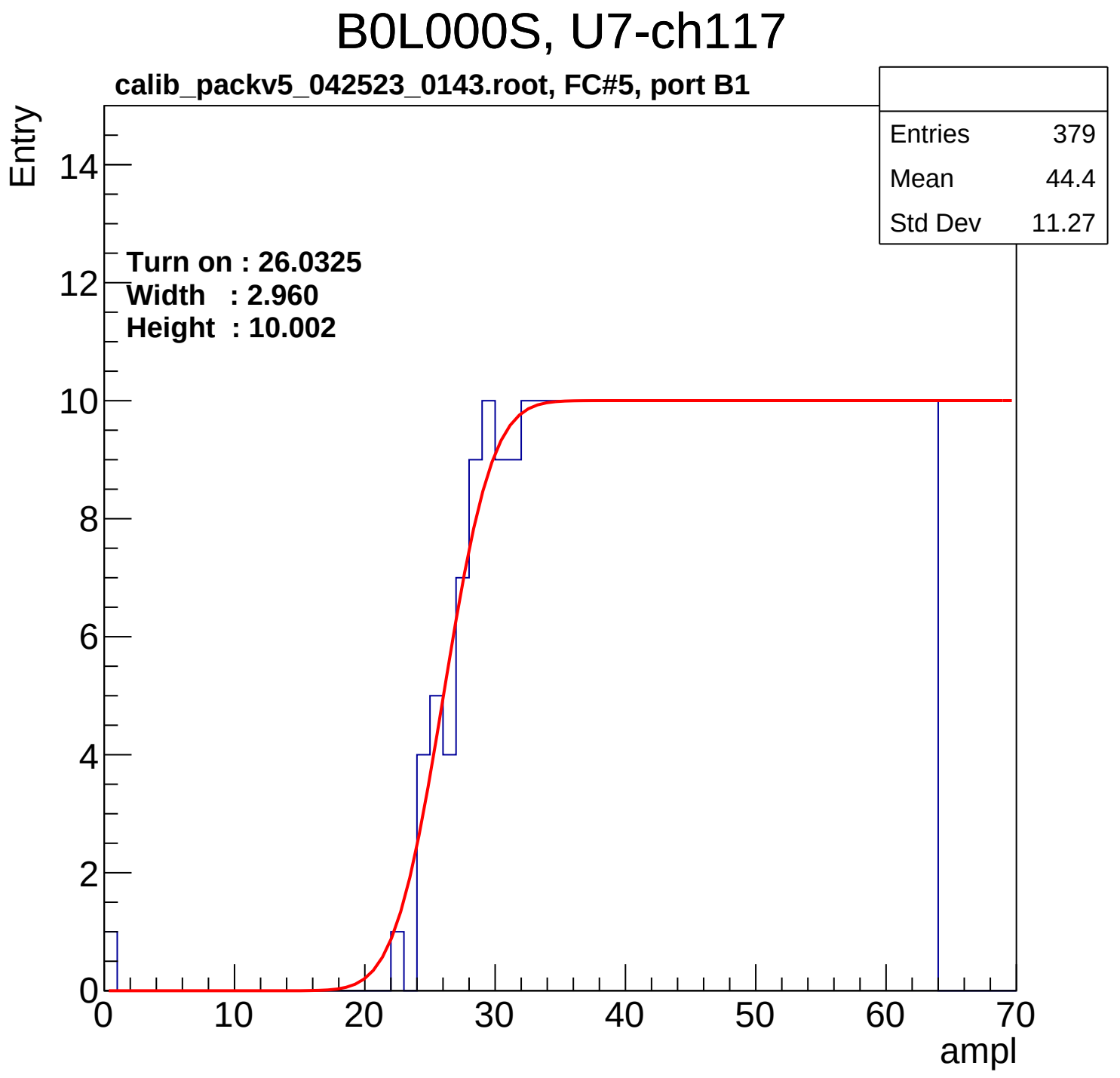
B0L000S, U7-ch117
calib_packv5_042523_0143.root, FC#5, port B1
Entries 379
Mean 44.4
Std Dev 11.27
Turn on : 26.0325
Width : 2.960
Height : 10.002
Entry
ampl
0
2
4
6
8
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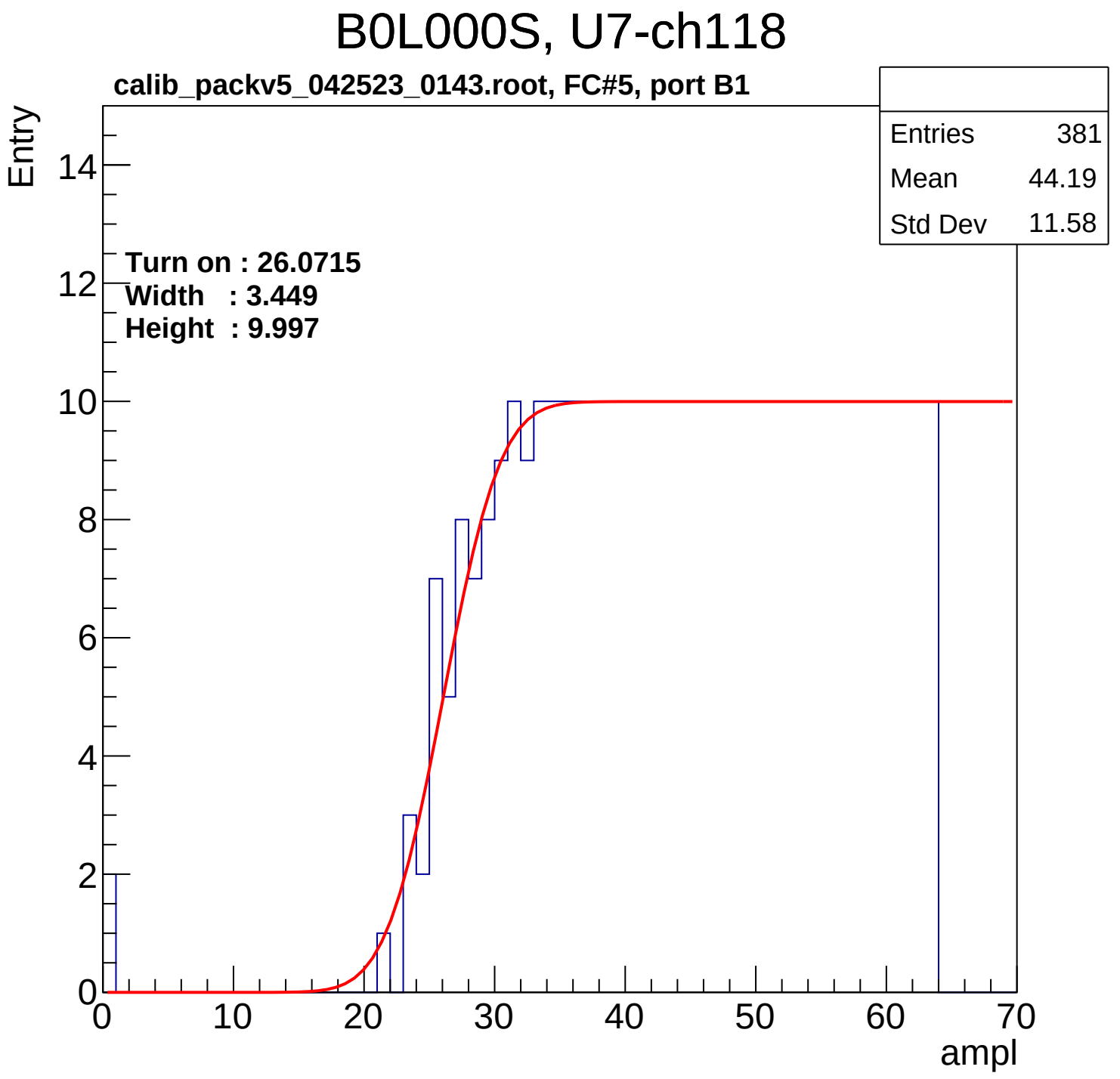
B0L000S, U7-ch118
calib_packv5_042523_0143.root, FC#5, port B1
Entries 381
Mean 44.19
Std Dev 11.58
Turn on : 26.0715
Width : 3.449
Height : 9.997
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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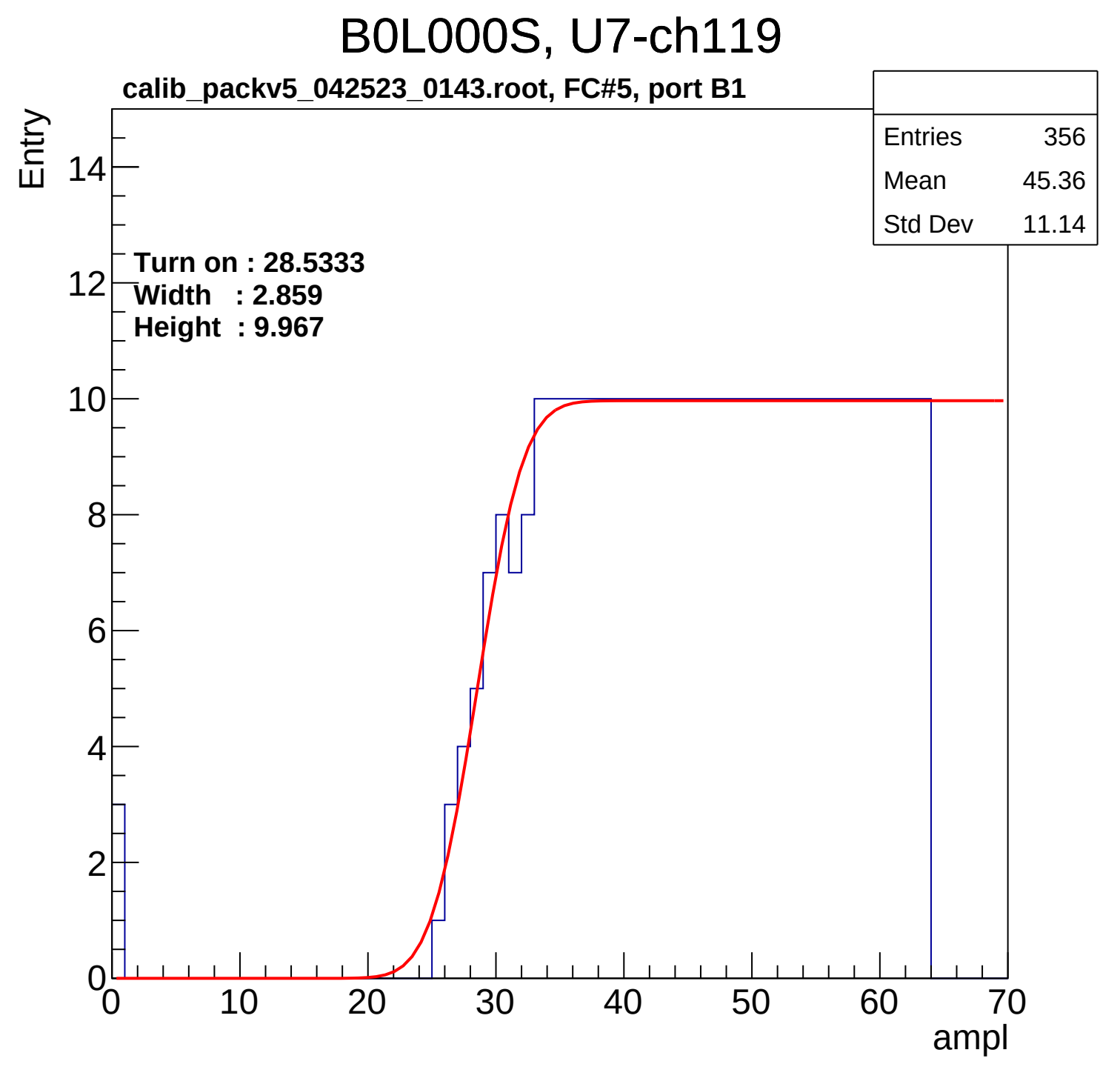
B0L000S, U7-ch119
calib_packv5_042523_0143.root, FC#5, port B1
Entries 356
Mean 45.36
Std Dev 11.14
Turn on : 28.5333
Width : 2.859
Height : 9.967
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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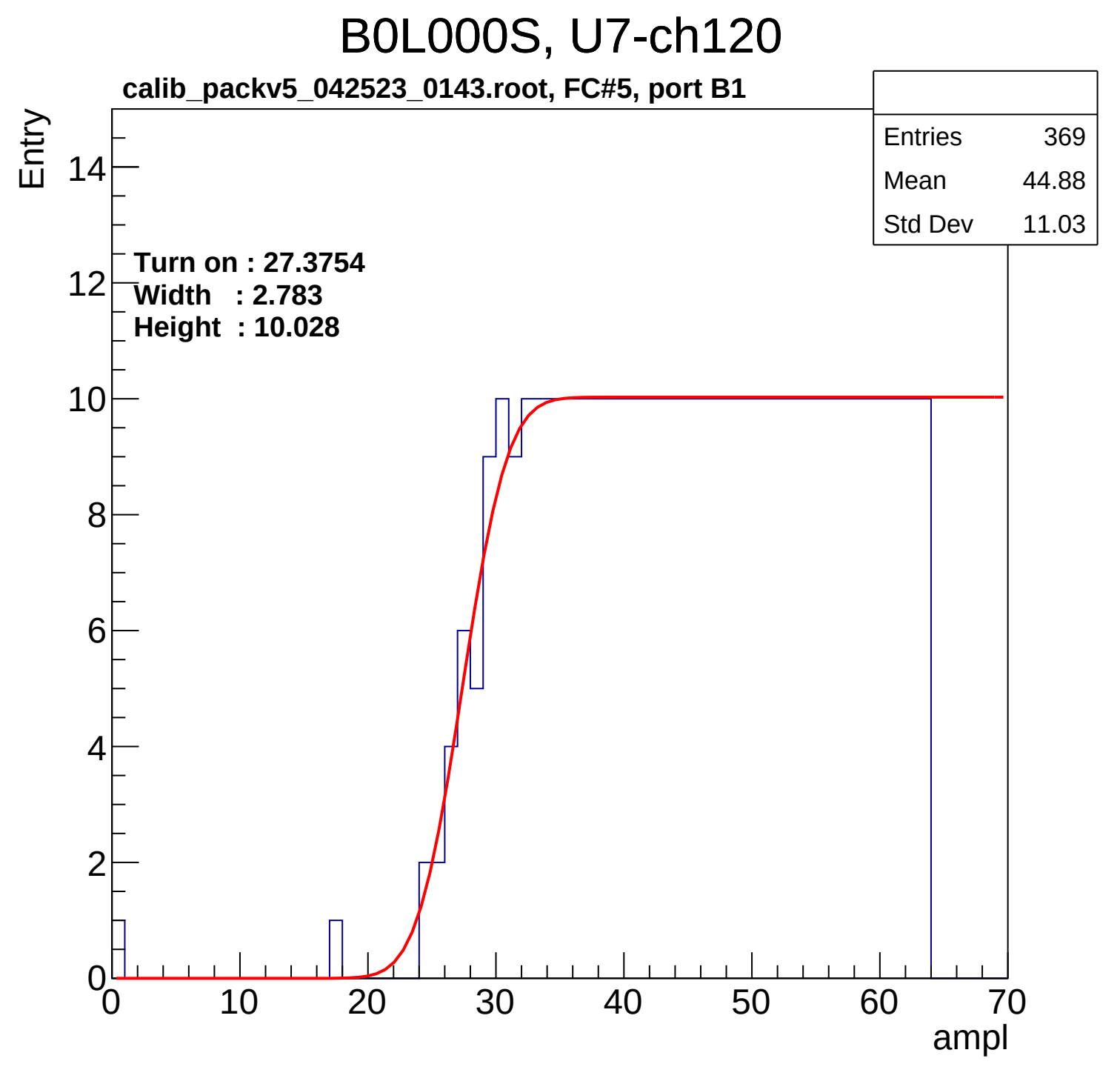
B0L000S, U7-ch120
calib_packv5_042523_0143.root, FC#5, port B1
Entries 369
Mean 44.88
Std Dev 11.03
Turn on : 27.3754
Width : 2.783
Height : 10.028
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
50
60
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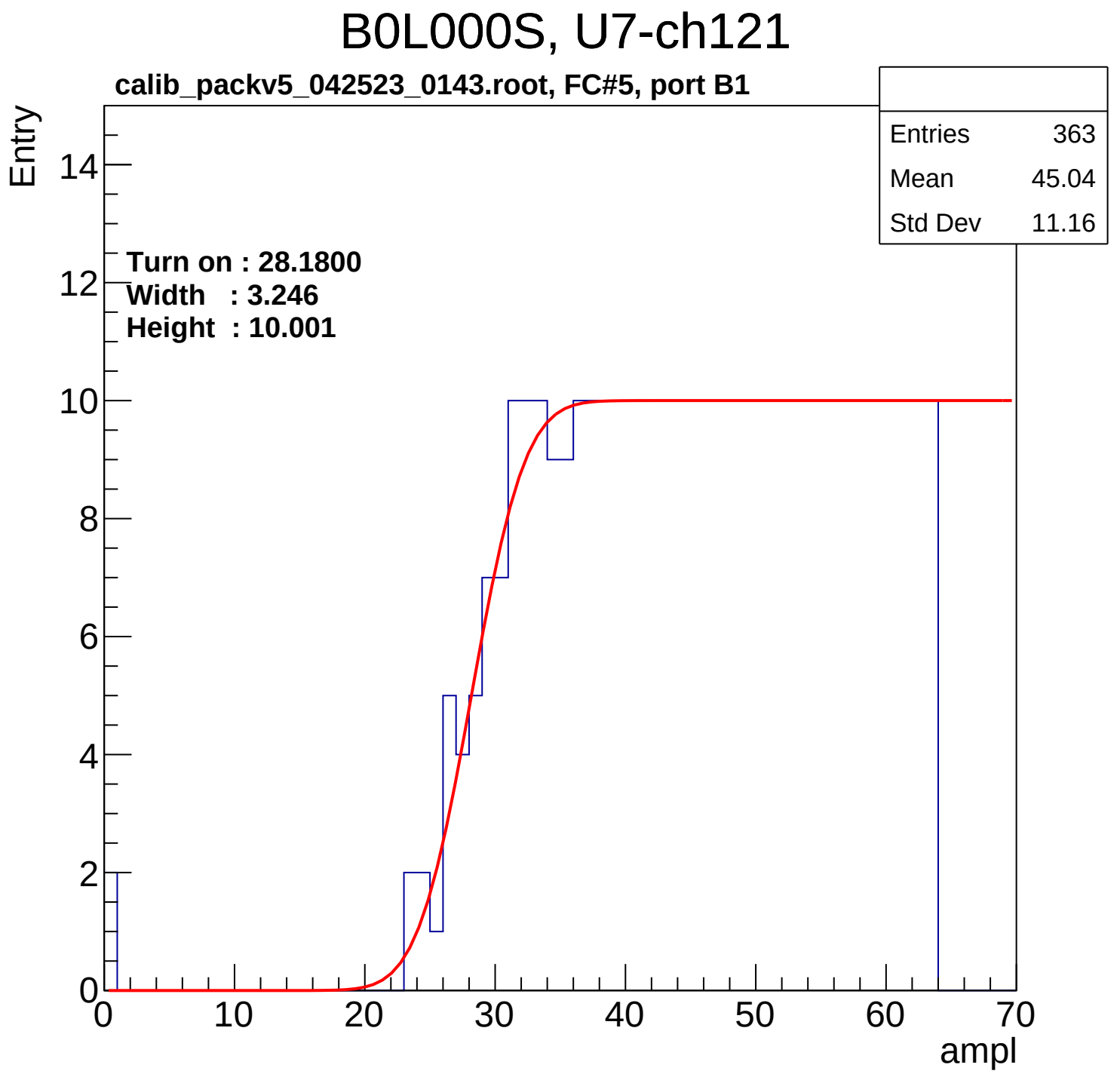
B0L000S, U7-ch121
calib_packv5_042523_0143.root, FC#5, port B1
Entries 363
Mean 45.04
Std Dev 11.16
Turn on : 28.1800
Width : 3.246
Height : 10.001
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
50
60
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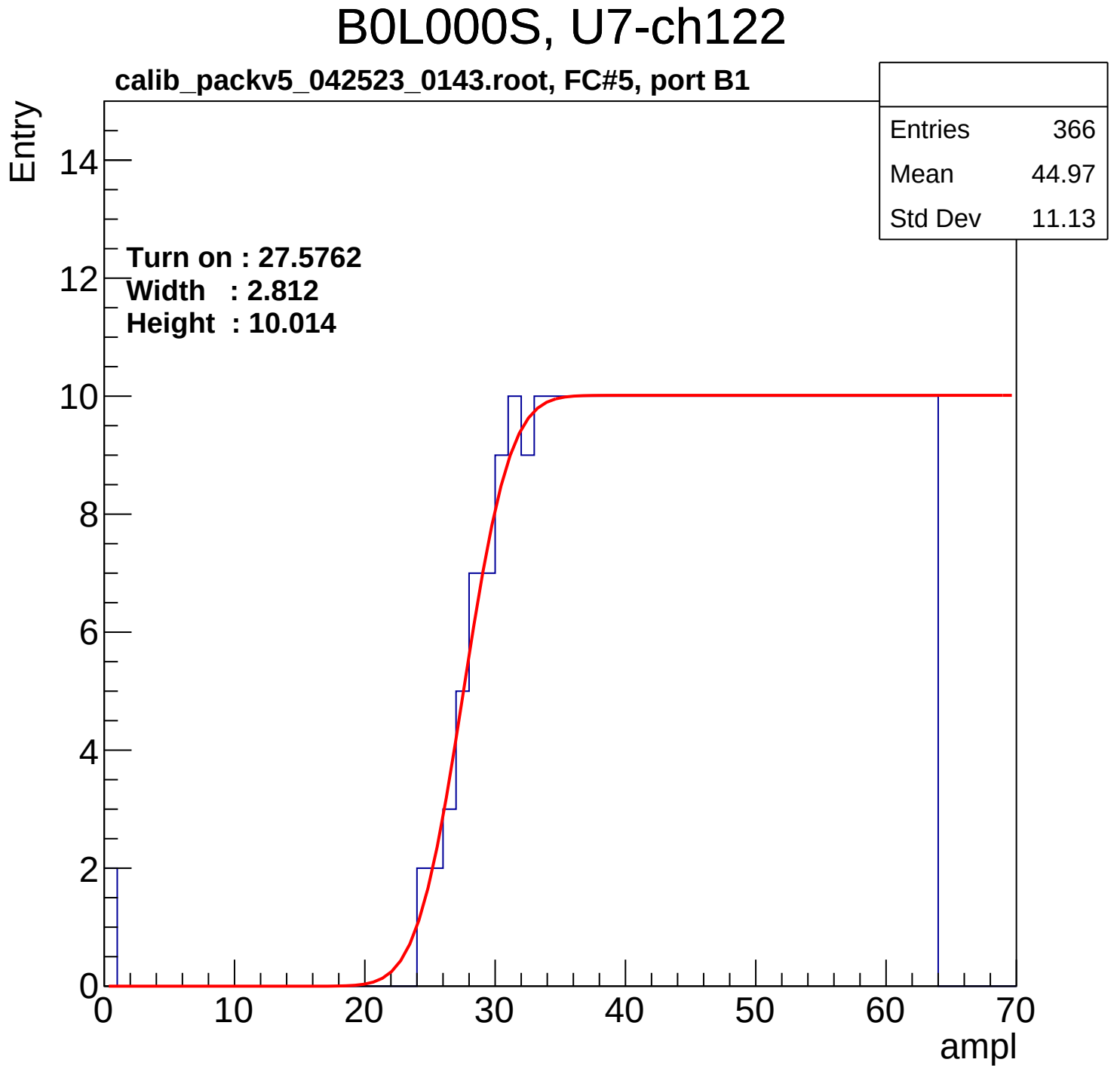
B0L000S, U7-ch122
calib_packv5_042523_0143.root, FC#5, port B1
Entries 366
Mean 44.97
Std Dev 11.13
Turn on : 27.5762
Width : 2.812
Height : 10.014
Entry
ampl
0
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4
6
8
10
12
14
0
10
20
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40
50
60
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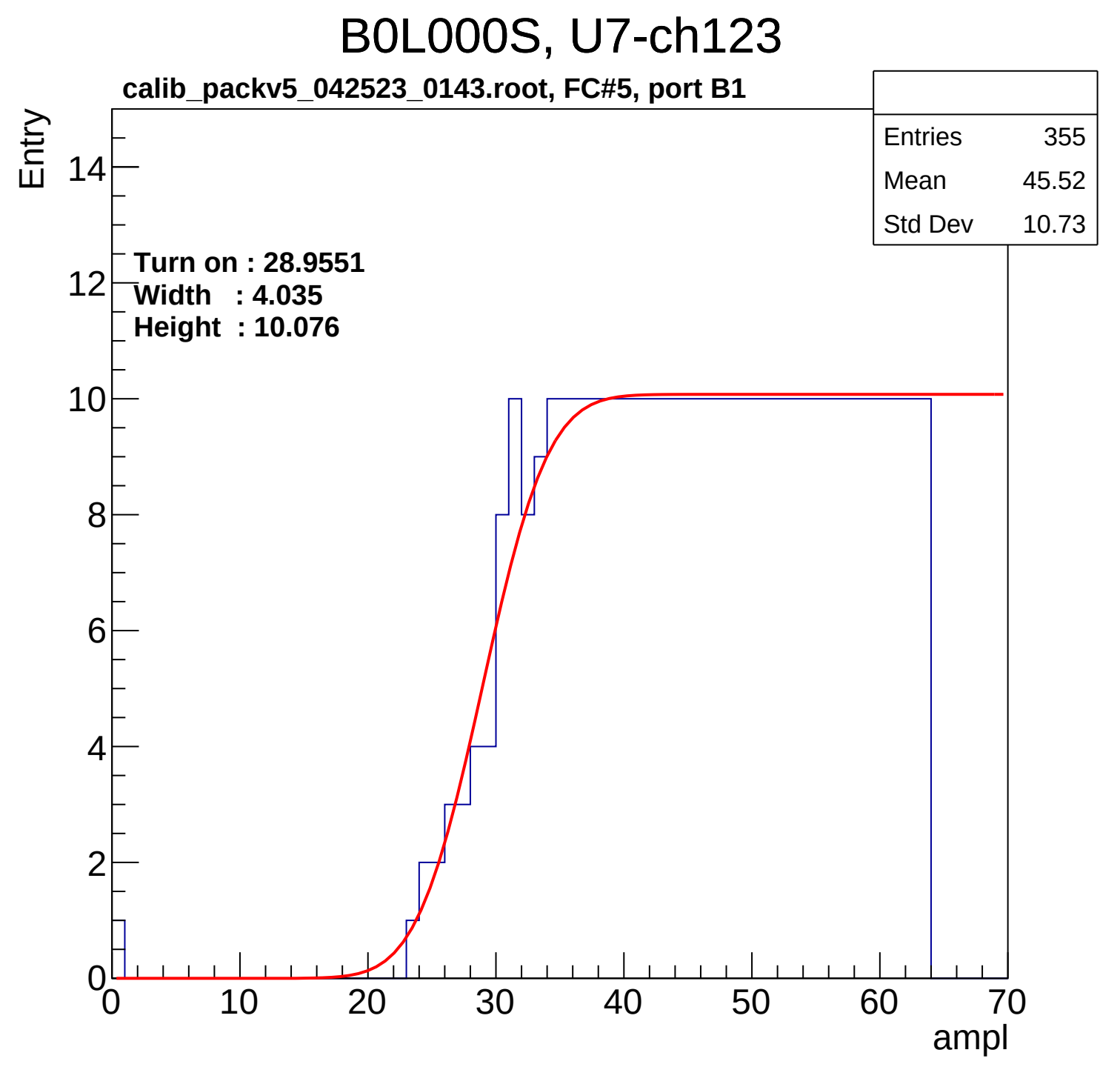
B0L000S, U7-ch123
calib_packv5_042523_0143.root, FC#5, port B1
Entries 355
Mean 45.52
Std Dev 10.73
Turn on : 28.9551
Width : 4.035
Height : 10.076
Entry
ampl
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2
4
6
8
10
12
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0
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20
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40
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60
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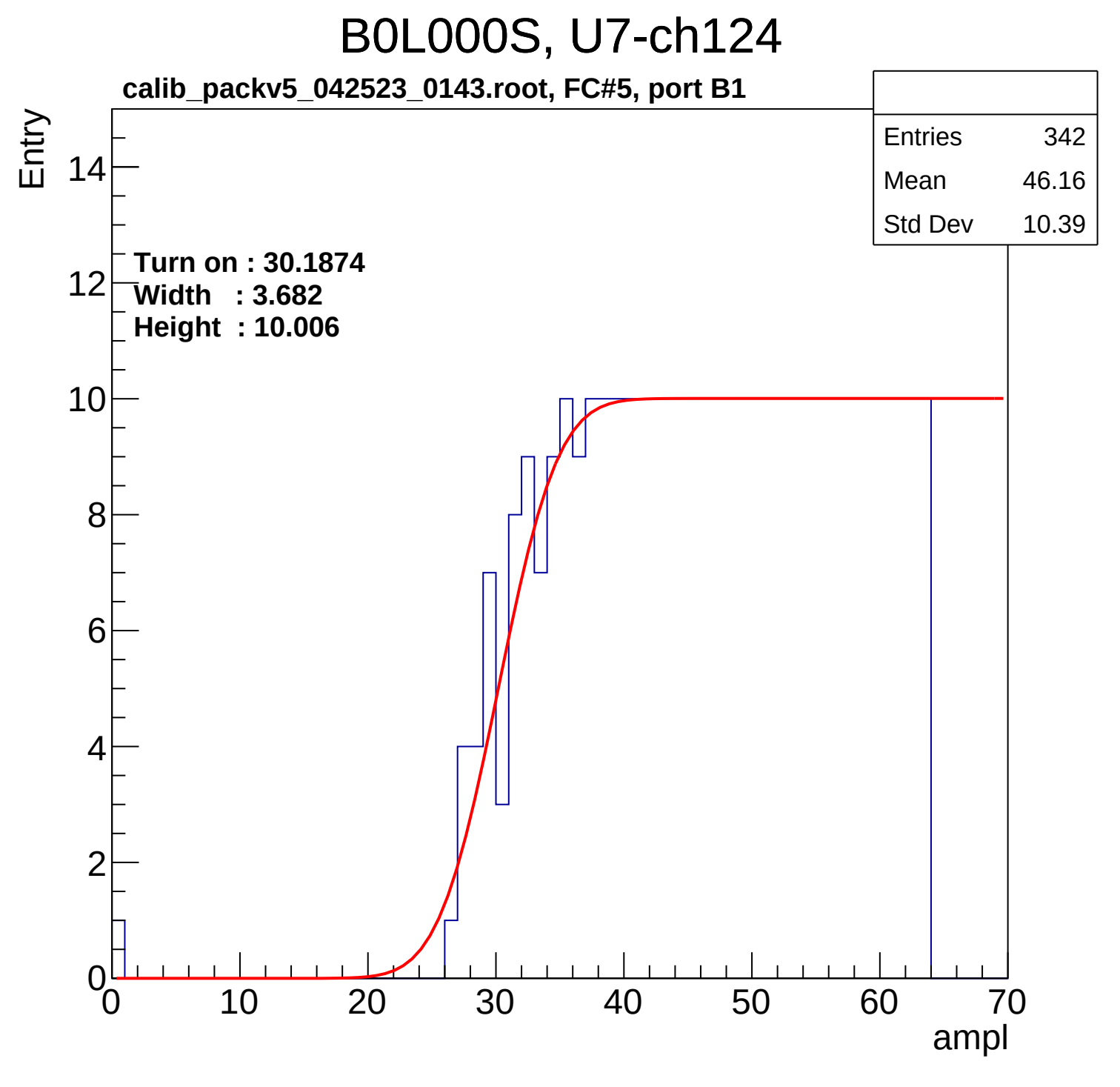
B0L000S, U7-ch124
calib_packv5_042523_0143.root, FC#5, port B1
Entries 342
Mean 46.16
Std Dev 10.39
Turn on : 30.1874
Width : 3.682
Height : 10.006
Entry
ampl
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4
6
8
10
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14
0
10
20
30
40
50
60
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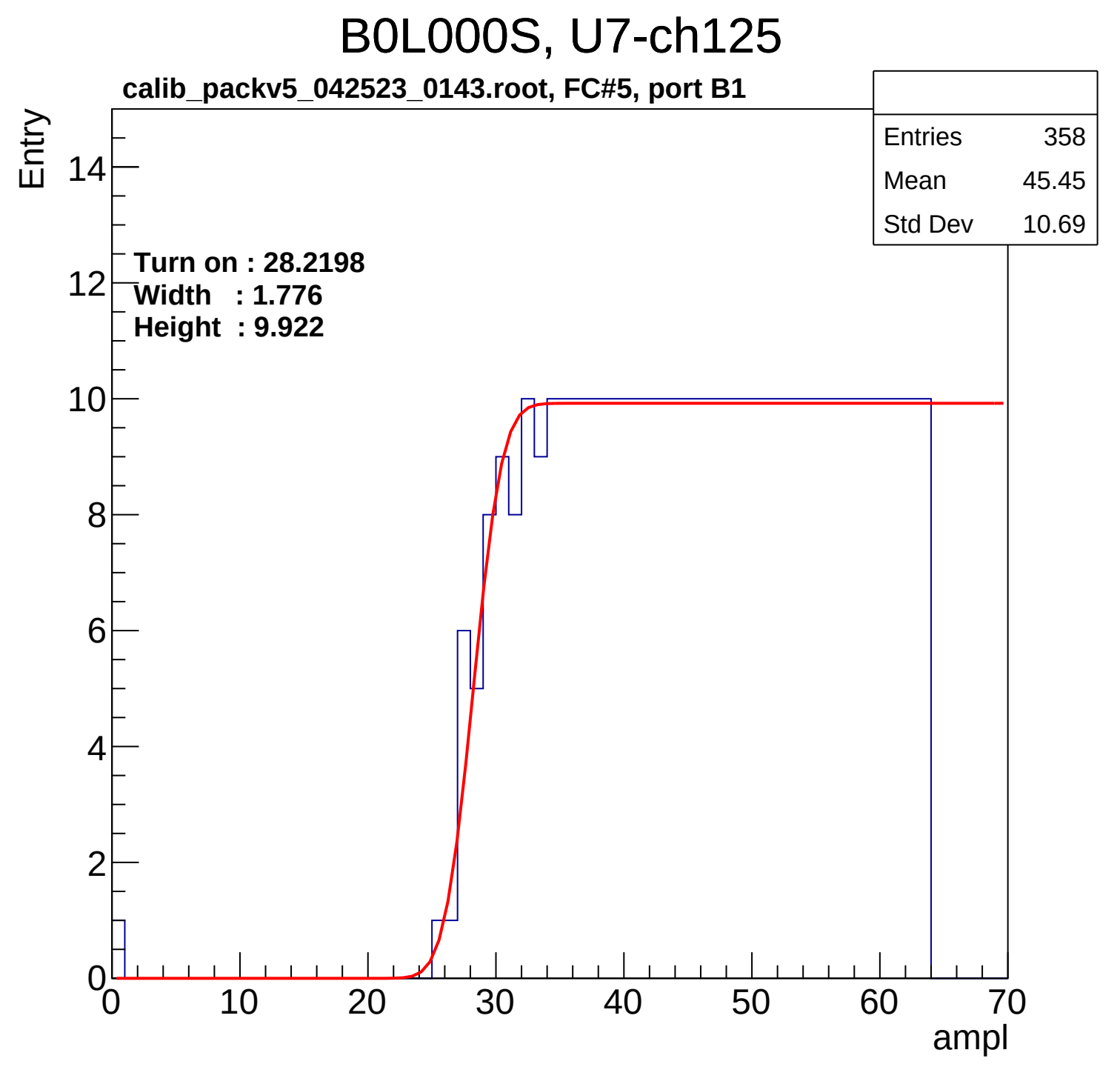
B0L000S, U7-ch125
calib_packv5_042523_0143.root, FC#5, port B1
Entries 358
Mean 45.45
Std Dev 10.69
Turn on : 28.2198
Width : 1.776
Height : 9.922
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
50
60
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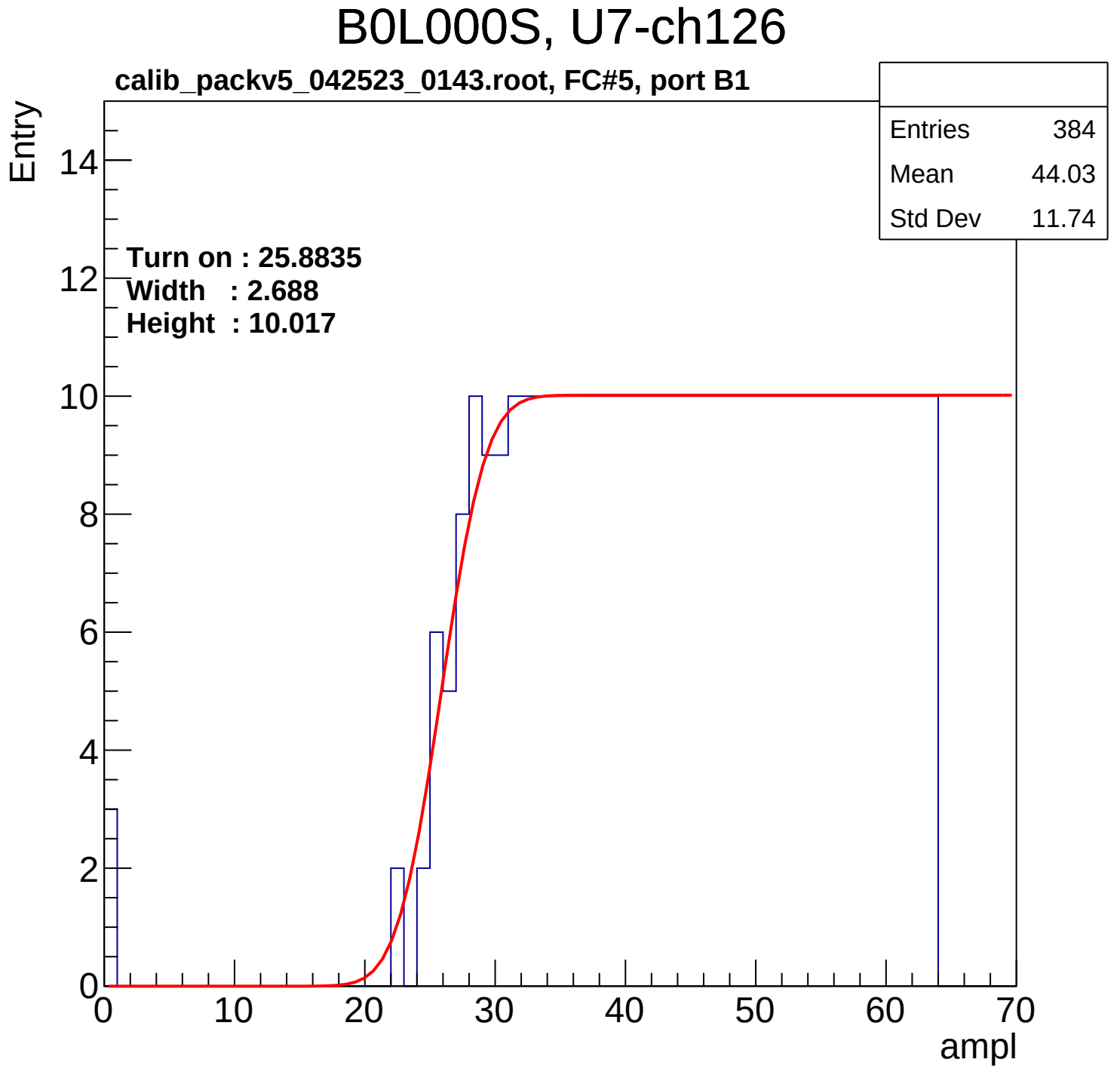
B0L000S, U7-ch126
calib_packv5_042523_0143.root, FC#5, port B1
Entries 384
Mean 44.03
Std Dev 11.74
Turn on : 25.8835
Width : 2.688
Height : 10.017
Entry
ampl
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4
6
8
10
12
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0
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20
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40
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60
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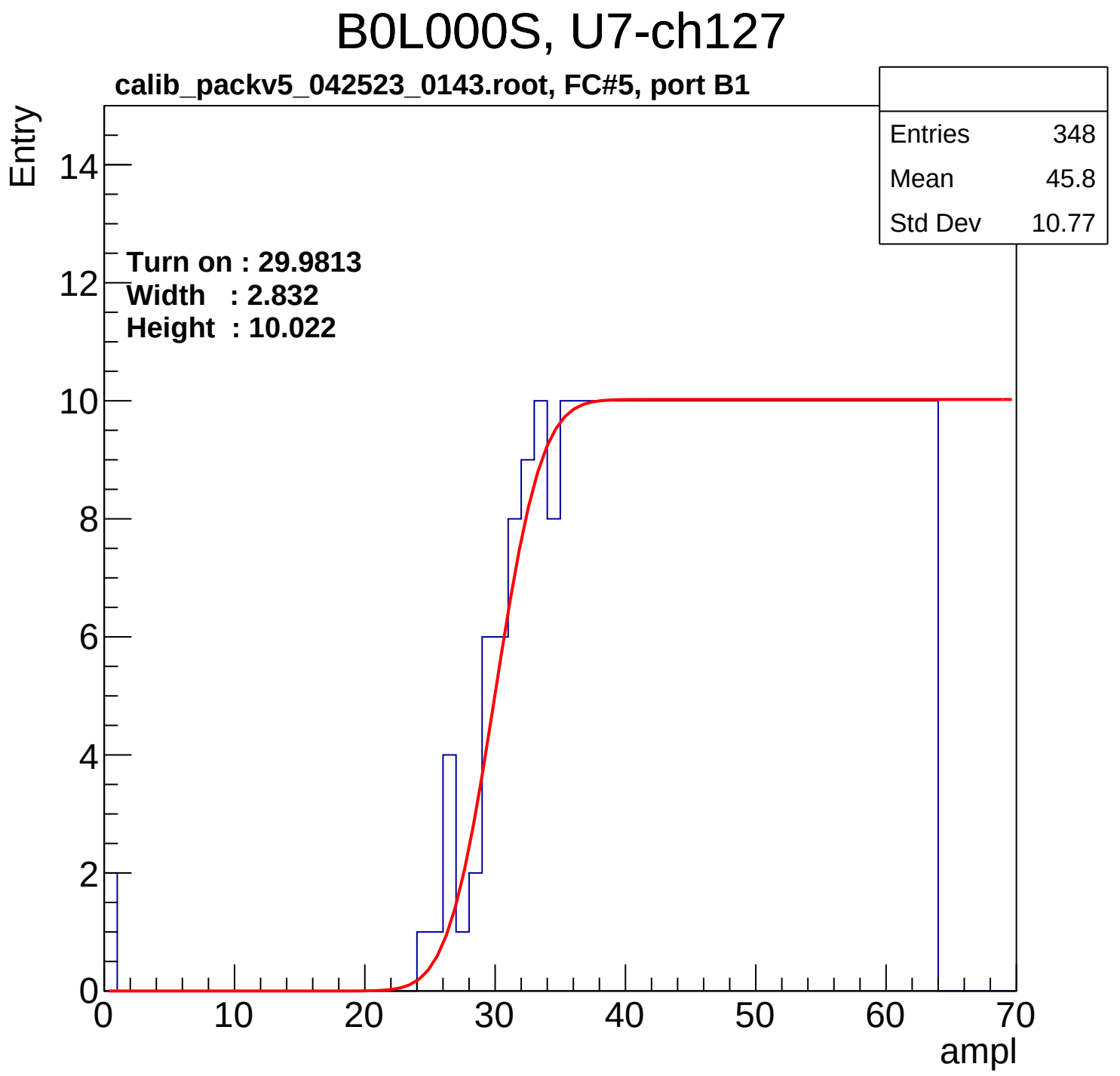
B0L000S, U7-ch127
calib_packv5_042523_0143.root, FC#5, port B1
Entries 348
Mean 45.8
Std Dev 10.77
Turn on : 29.9813
Width : 2.832
Height : 10.022
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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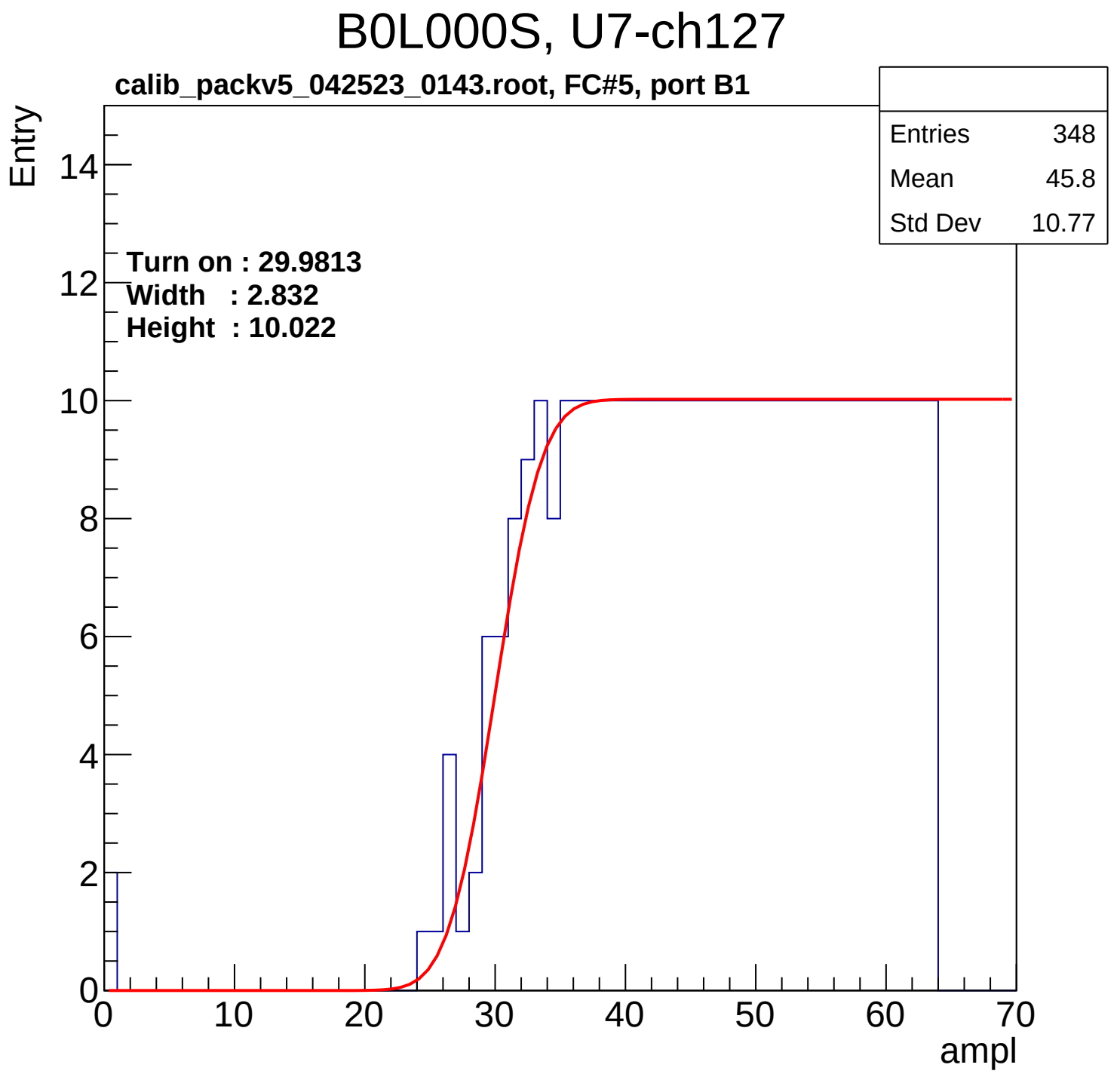
70


B0L000S, U7-ch127
calib_packv5_042523_0143.root, FC#5, port B1
Entries 348
Mean 45.8
Std Dev 10.77
Turn on : 29.9813
Width : 2.832
Height : 10.022
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70