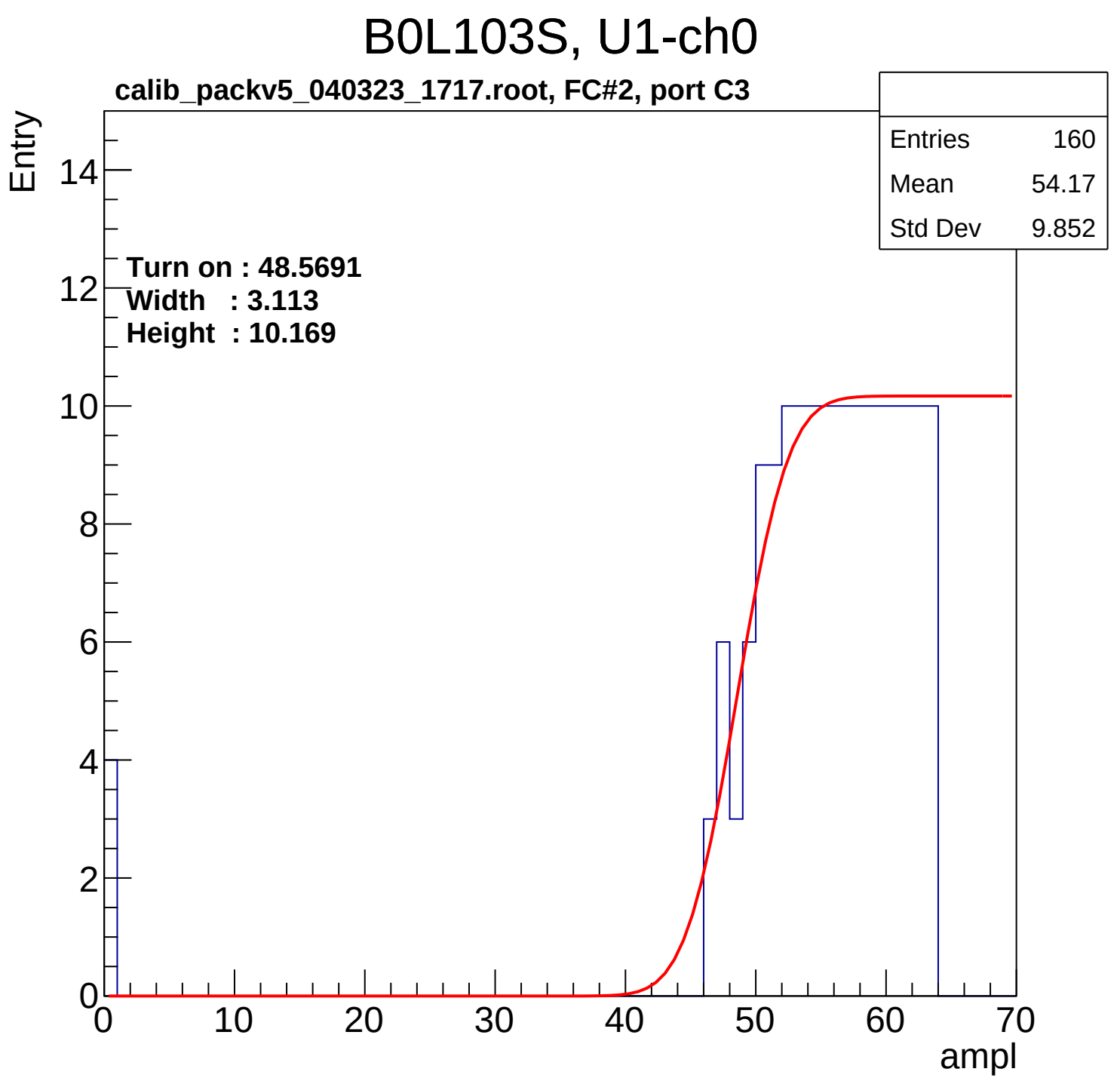
B0L103S, U1-ch0
calib_packv5_040323_1717.root, FC#2, port C3
Entries 160
Mean 54.17
Std Dev 9.852
Turn on : 48.5691
Width : 3.113
Height : 10.169
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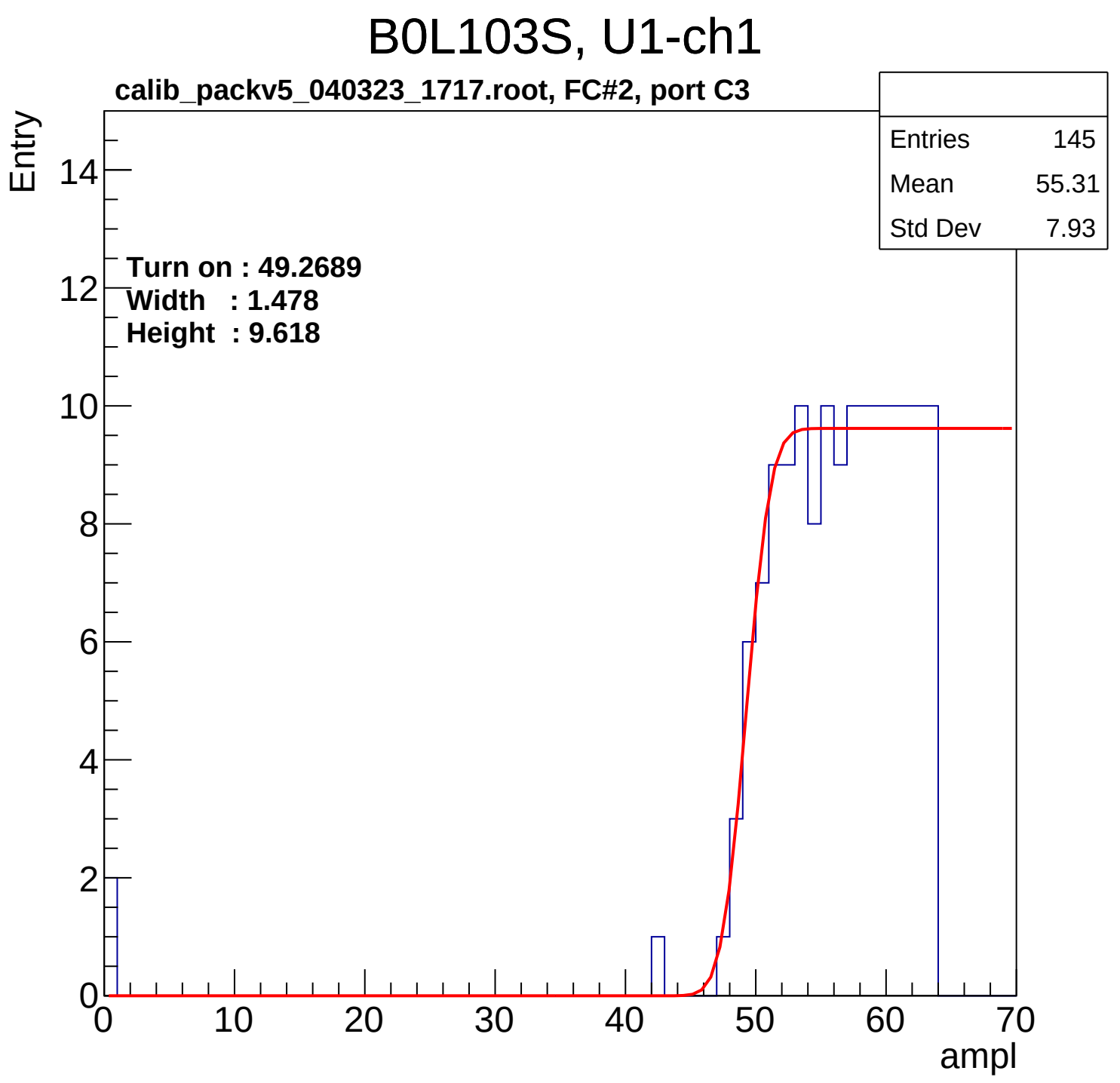
B0L103S, U1-ch1
calib_packv5_040323_1717.root, FC#2, port C3
Entries 145
Mean 55.31
Std Dev 7.93
Turn on : 49.2689
Width : 1.478
Height : 9.618
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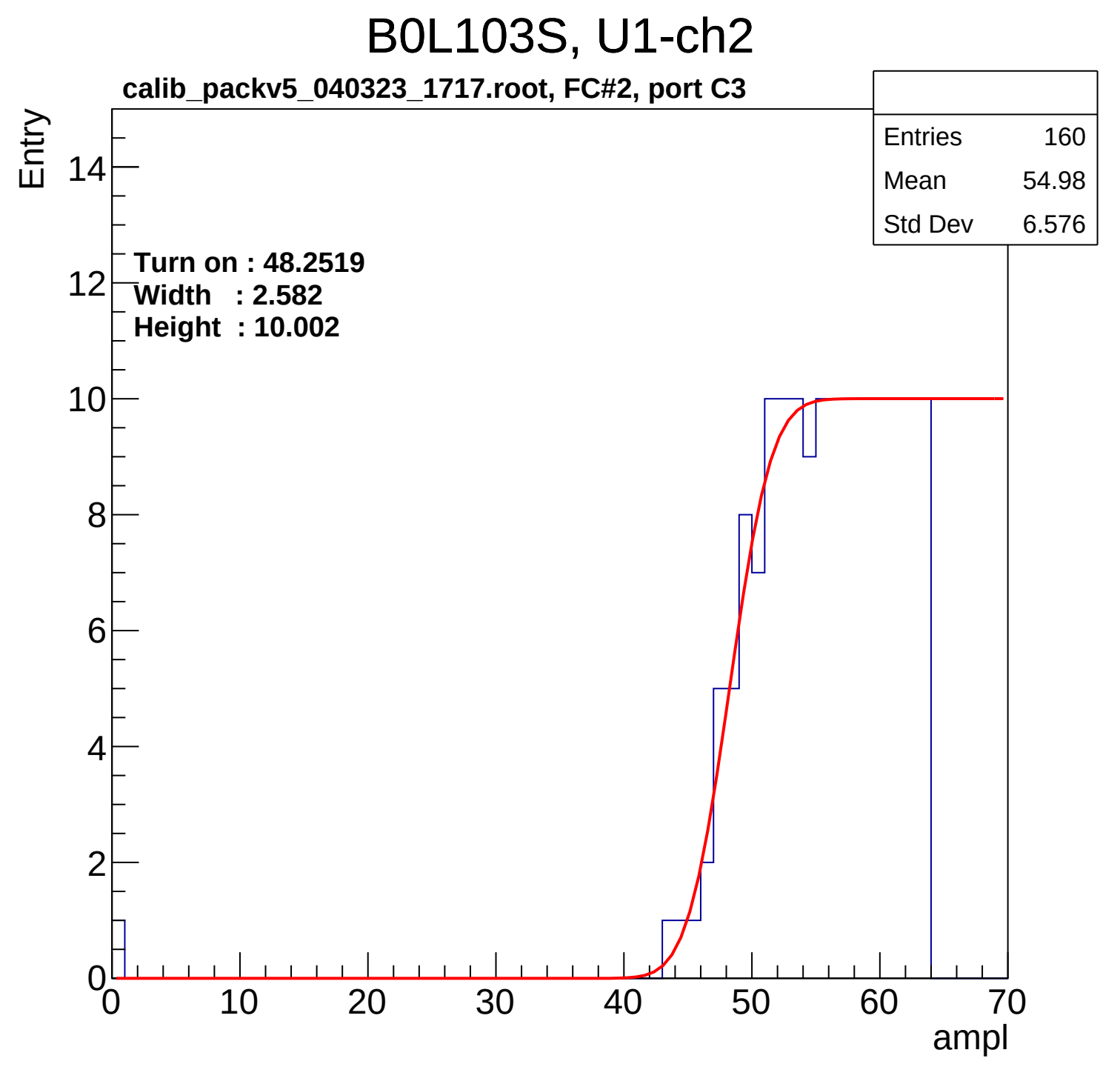
B0L103S, U1-ch2
calib_packv5_040323_1717.root, FC#2, port C3
Entries 160
Mean 54.98
Std Dev 6.576
Turn on : 48.2519
Width : 2.582
Height : 10.002
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ampl
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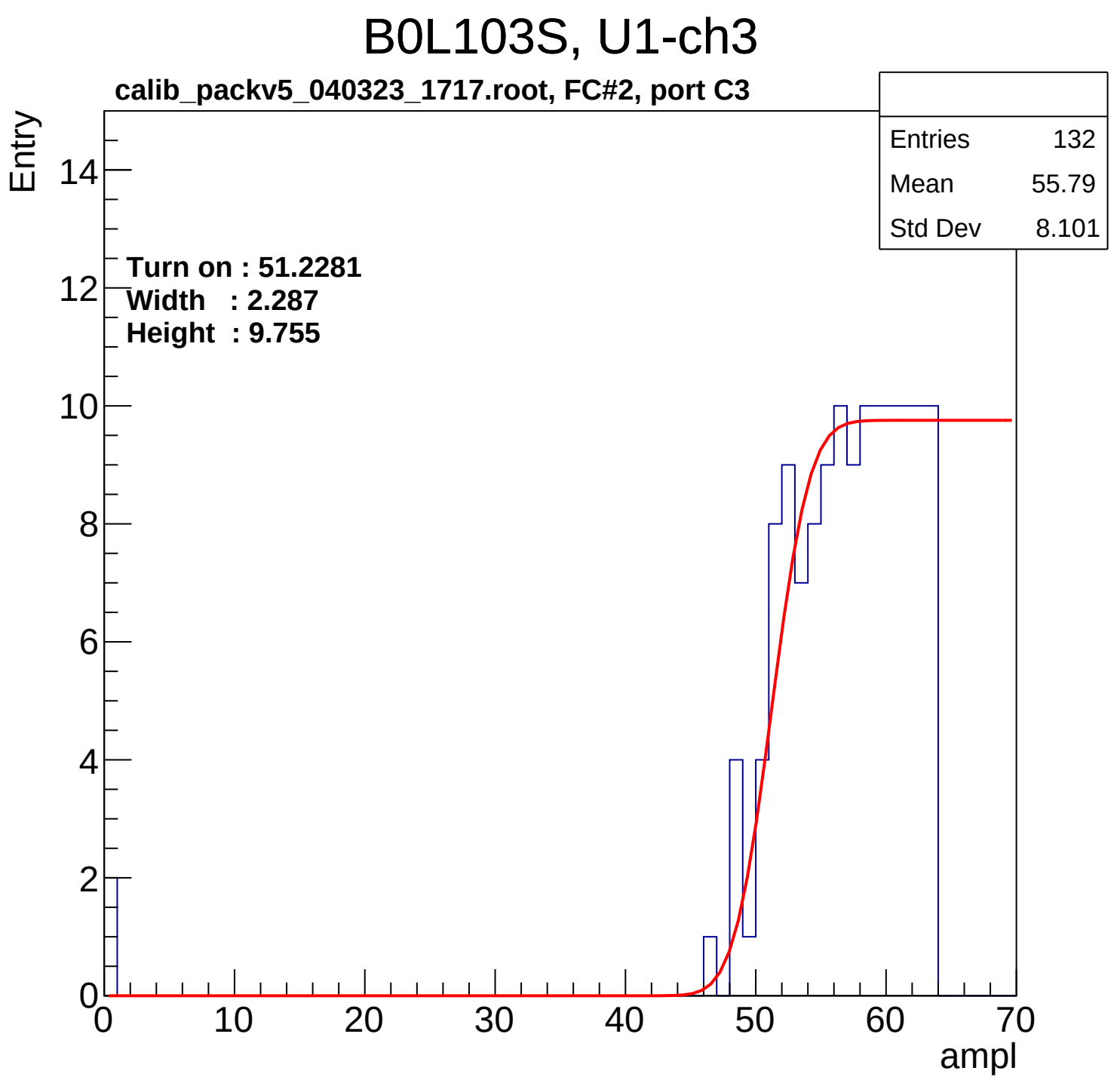
B0L103S, U1-ch3
calib_packv5_040323_1717.root, FC#2, port C3
Entries 132
Mean 55.79
Std Dev 8.101
Turn on : 51.2281
Width : 2.287
Height : 9.755
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ampl
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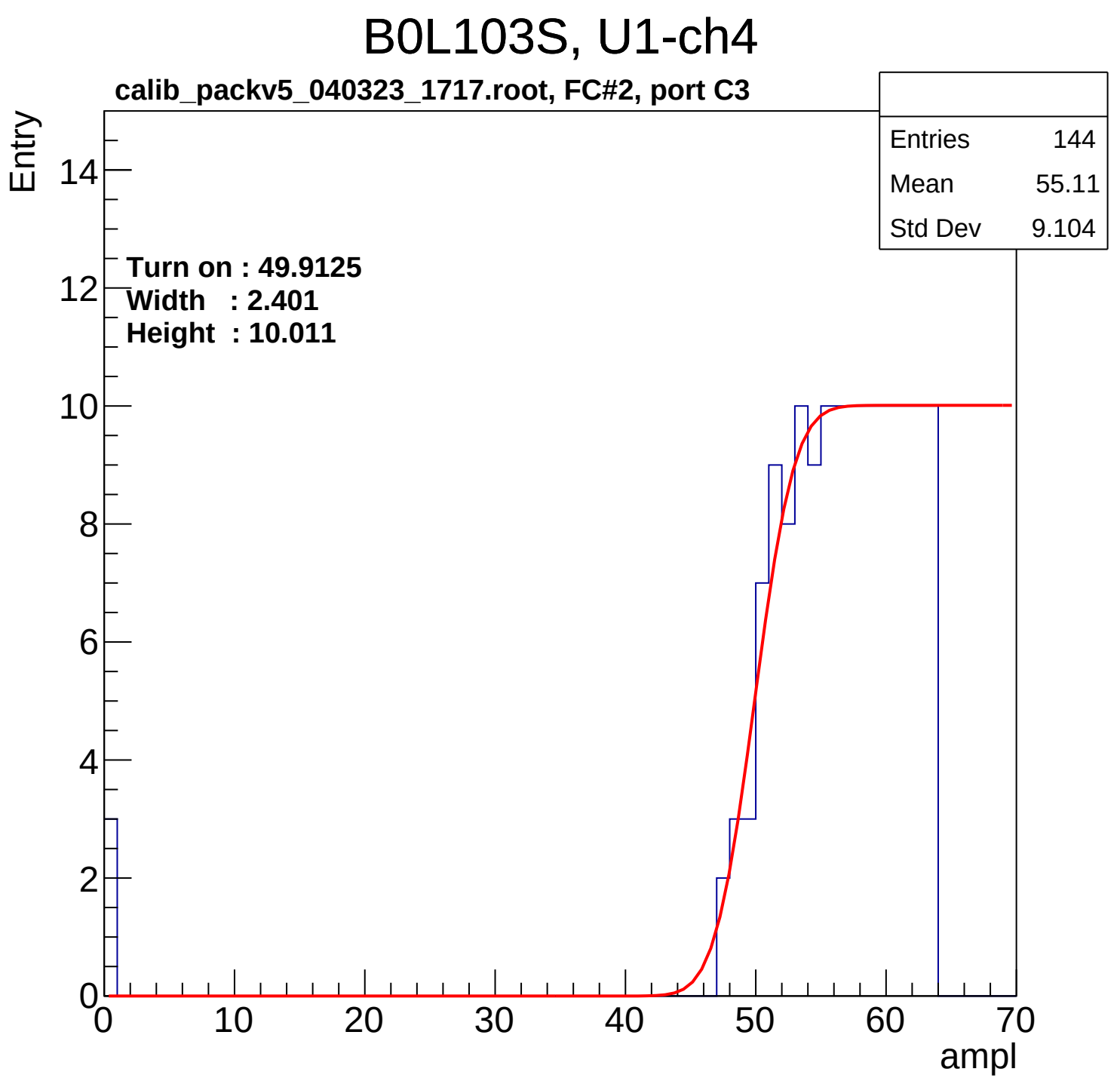
B0L103S, U1-ch4
calib_packv5_040323_1717.root, FC#2, port C3
Entries 144
Mean 55.11
Std Dev 9.104
Turn on : 49.9125
Width : 2.401
Height : 10.011
Entry
ampl
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6
8
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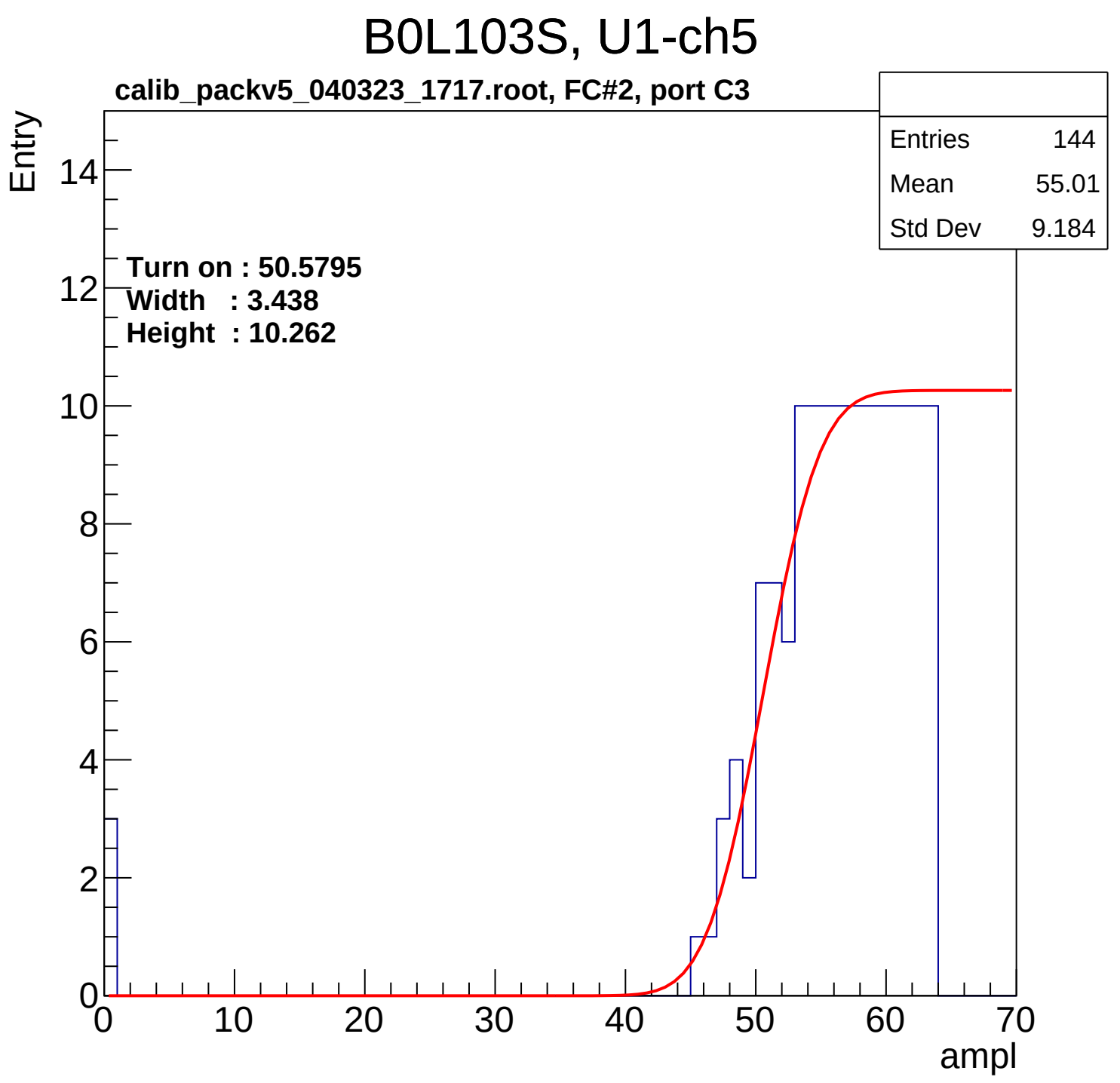
B0L103S, U1-ch5
calib_packv5_040323_1717.root, FC#2, port C3
Entries 144
Mean 55.01
Std Dev 9.184
Turn on : 50.5795
Width : 3.438
Height : 10.262
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ampl
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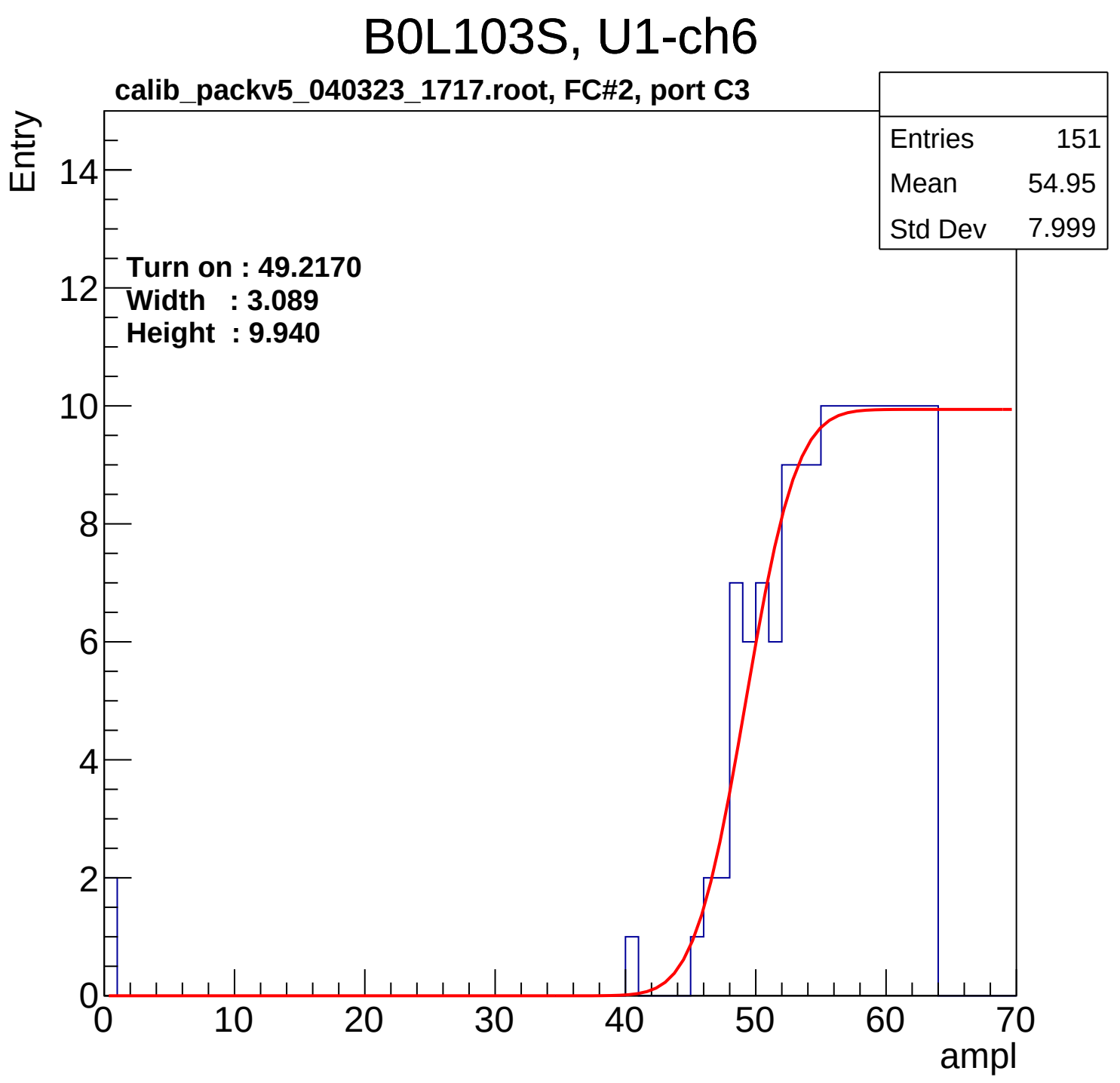
B0L103S, U1-ch6
calib_packv5_040323_1717.root, FC#2, port C3
Entries 151
Mean 54.95
Std Dev 7.999
Turn on : 49.2170
Width : 3.089
Height : 9.940
Entry
ampl
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6
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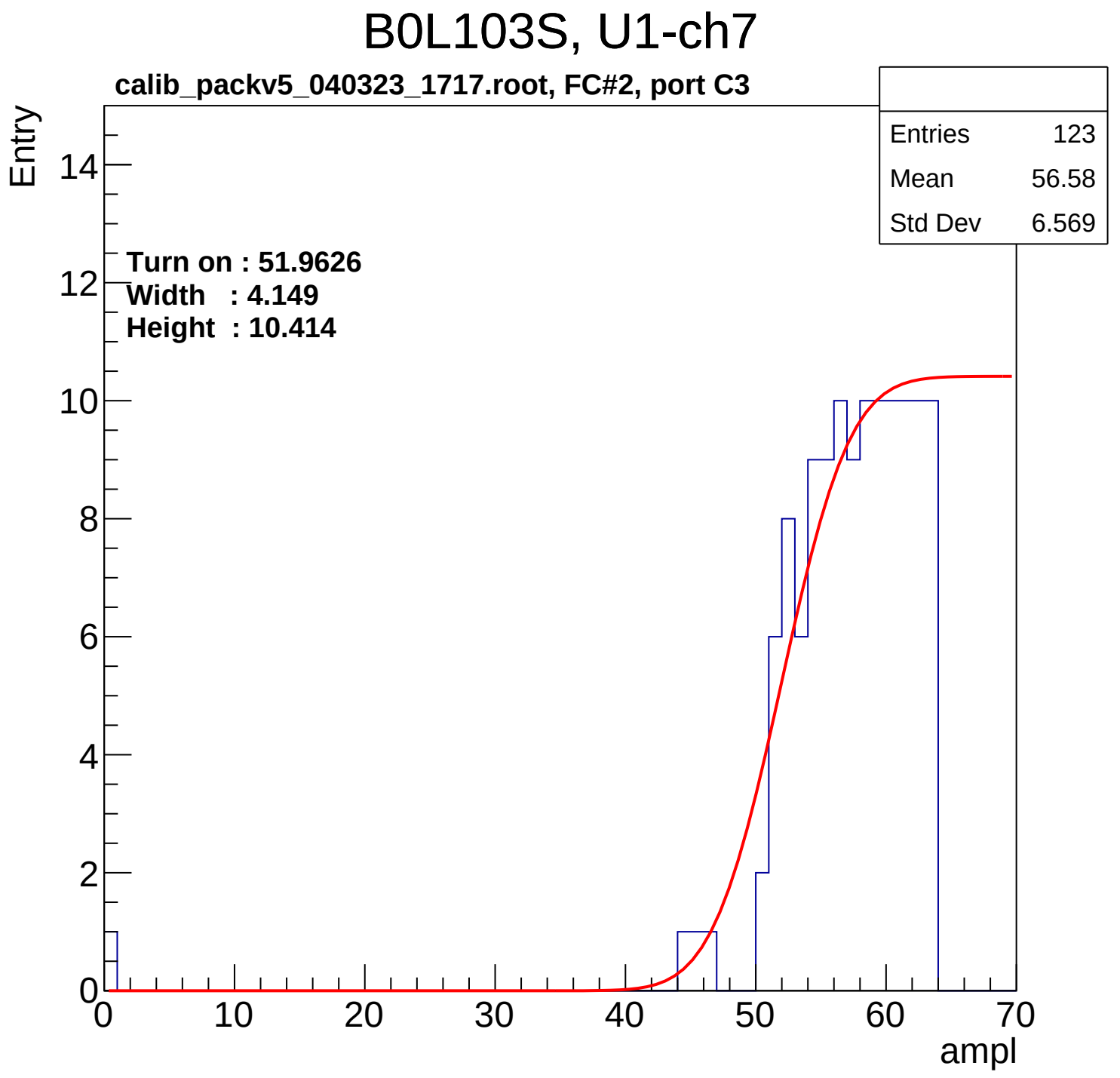
B0L103S, U1-ch7
calib_packv5_040323_1717.root, FC#2, port C3
Entries 123
Mean 56.58
Std Dev 6.569
Turn on : 51.9626
Width : 4.149
Height : 10.414
Entry
ampl
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2
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6
8
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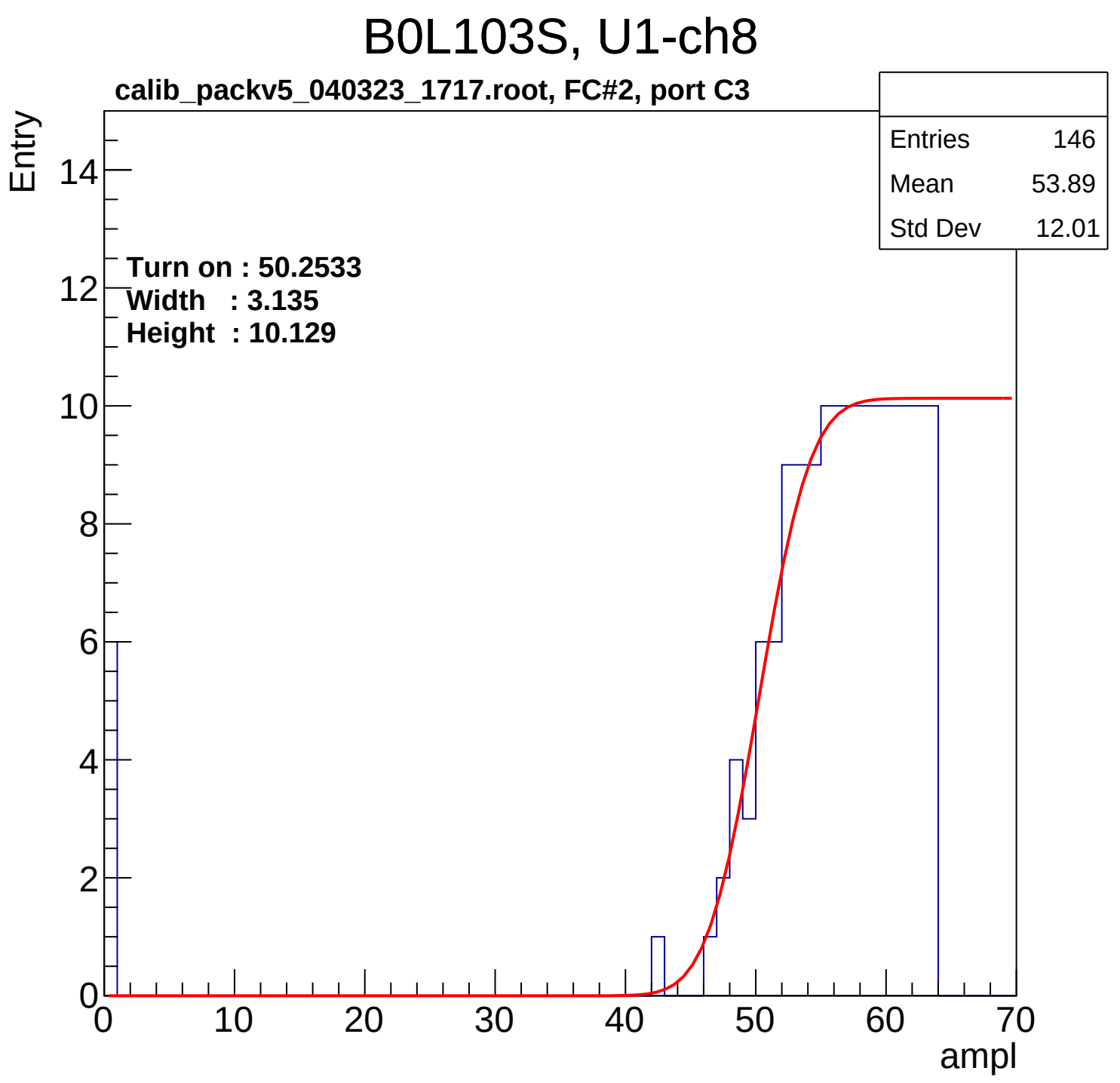
B0L103S, U1-ch8
calib_packv5_040323_1717.root, FC#2, port C3
Entries 146
Mean 53.89
Std Dev 12.01
Turn on : 50.2533
Width : 3.135
Height : 10.129
Entry
ampl
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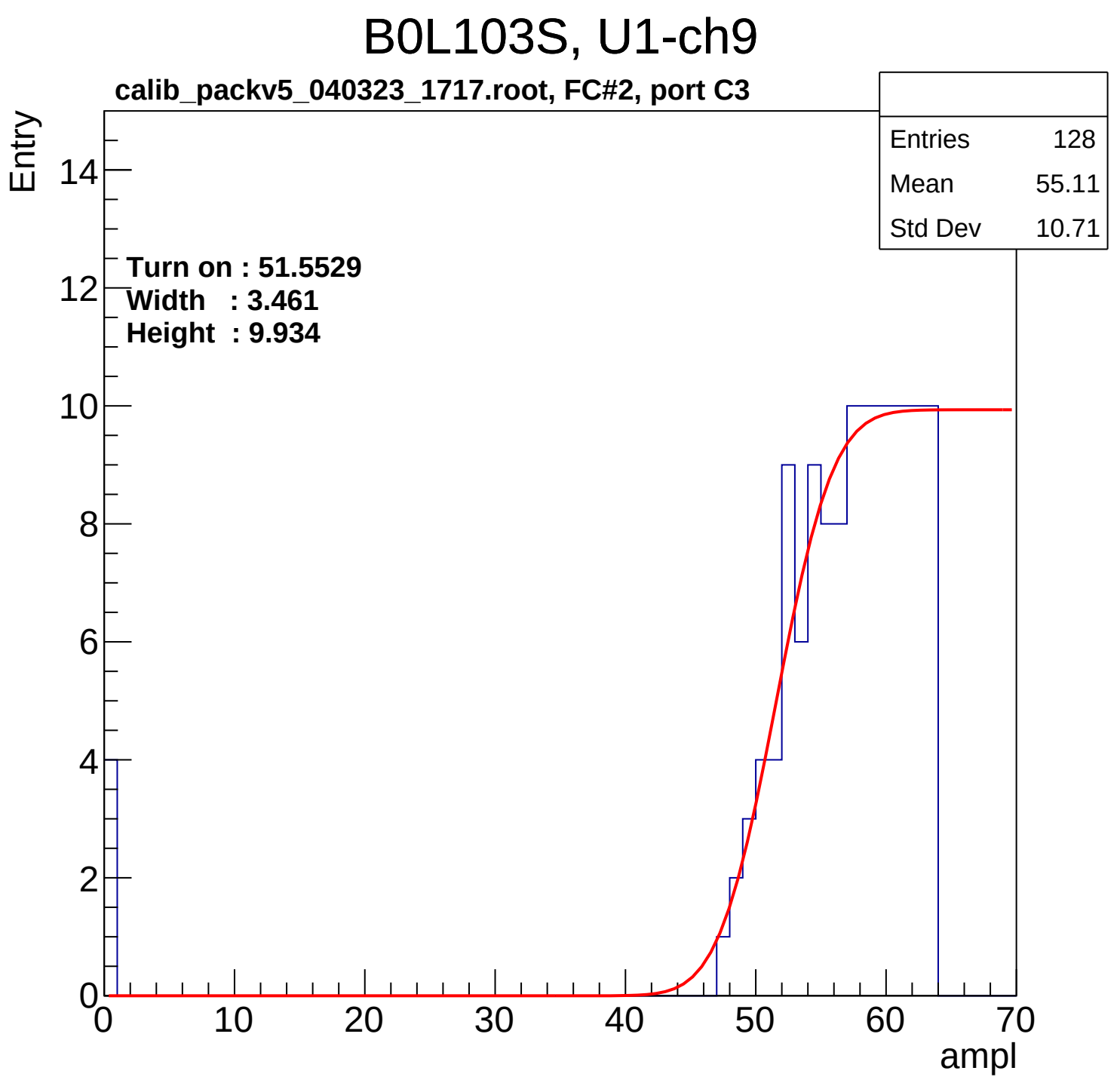
B0L103S, U1-ch9
calib_packv5_040323_1717.root, FC#2, port C3
Entries 128
Mean 55.11
Std Dev 10.71
Turn on : 51.5529
Width : 3.461
Height : 9.934
Entry
ampl
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6
8
10
12
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0
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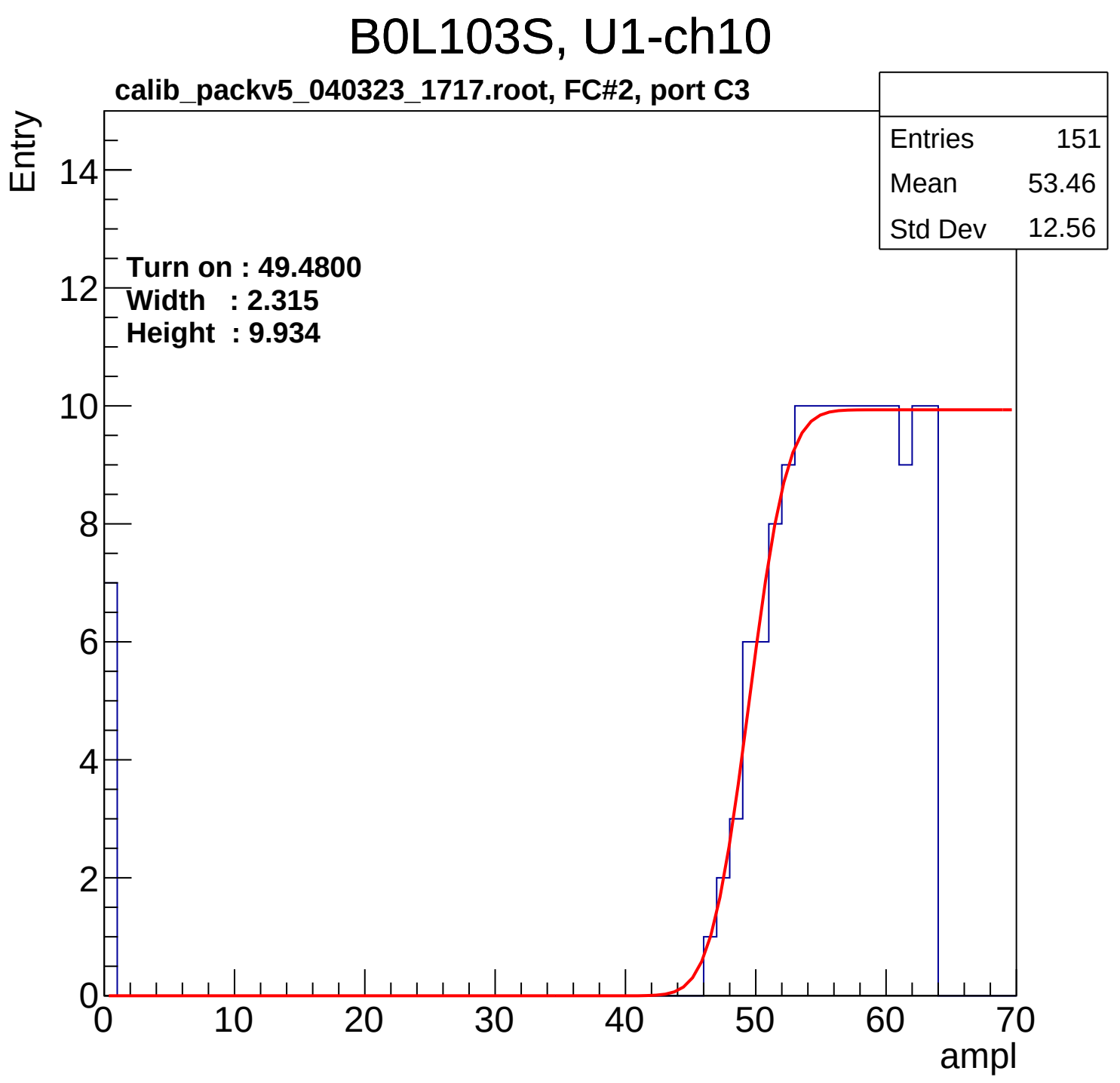
B0L103S, U1-ch10
calib_packv5_040323_1717.root, FC#2, port C3
Entries 151
Mean 53.46
Std Dev 12.56
Turn on : 49.4800
Width : 2.315
Height : 9.934
Entry
ampl
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6
8
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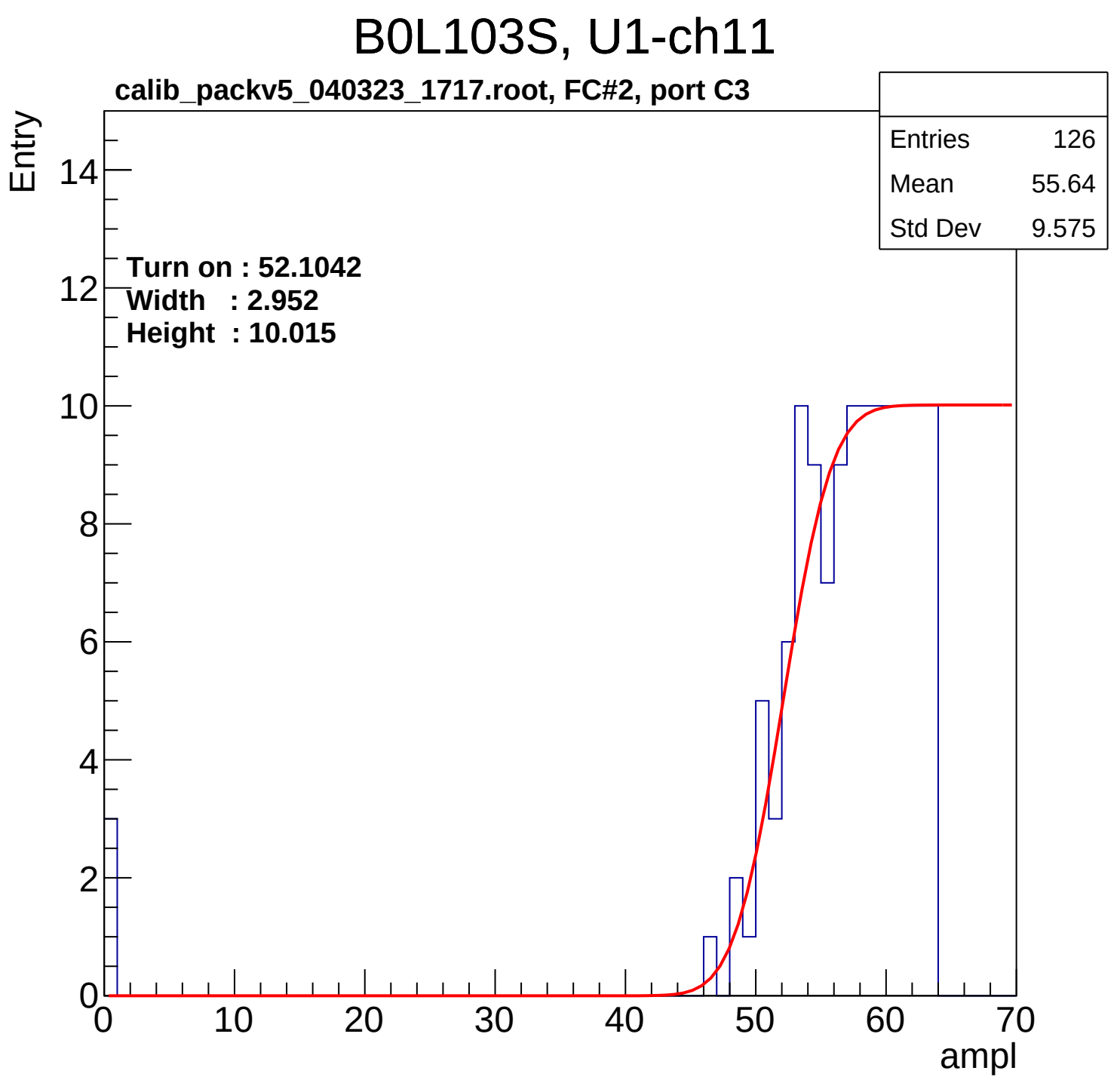
B0L103S, U1-ch11
calib_packv5_040323_1717.root, FC#2, port C3
Entries 126
Mean 55.64
Std Dev 9.575
Turn on : 52.1042
Width : 2.952
Height : 10.015
Entry
ampl
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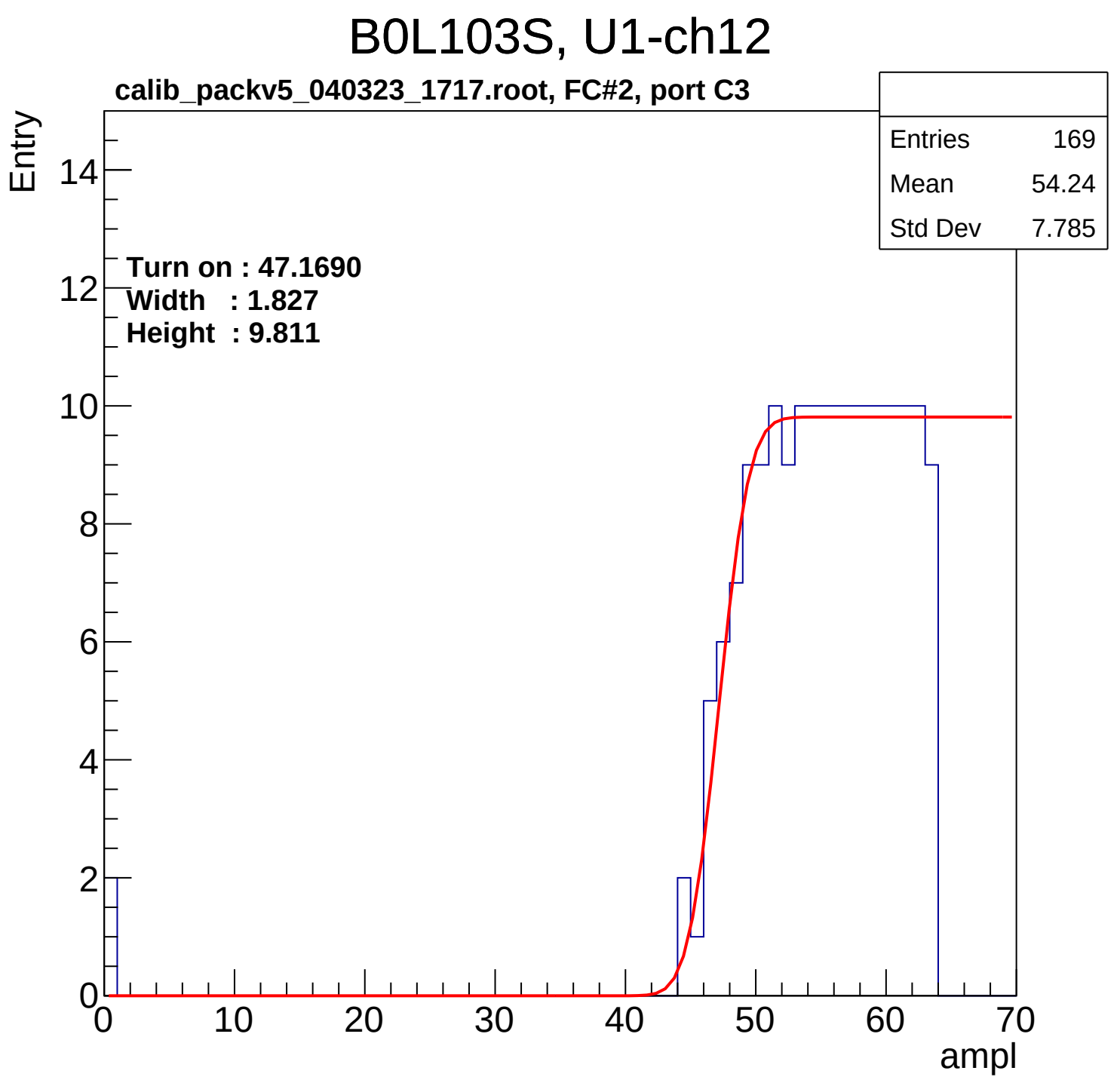
B0L103S, U1-ch12
calib_packv5_040323_1717.root, FC#2, port C3
Entries 169
Mean 54.24
Std Dev 7.785
Turn on : 47.1690
Width : 1.827
Height : 9.811
Entry
ampl
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6
8
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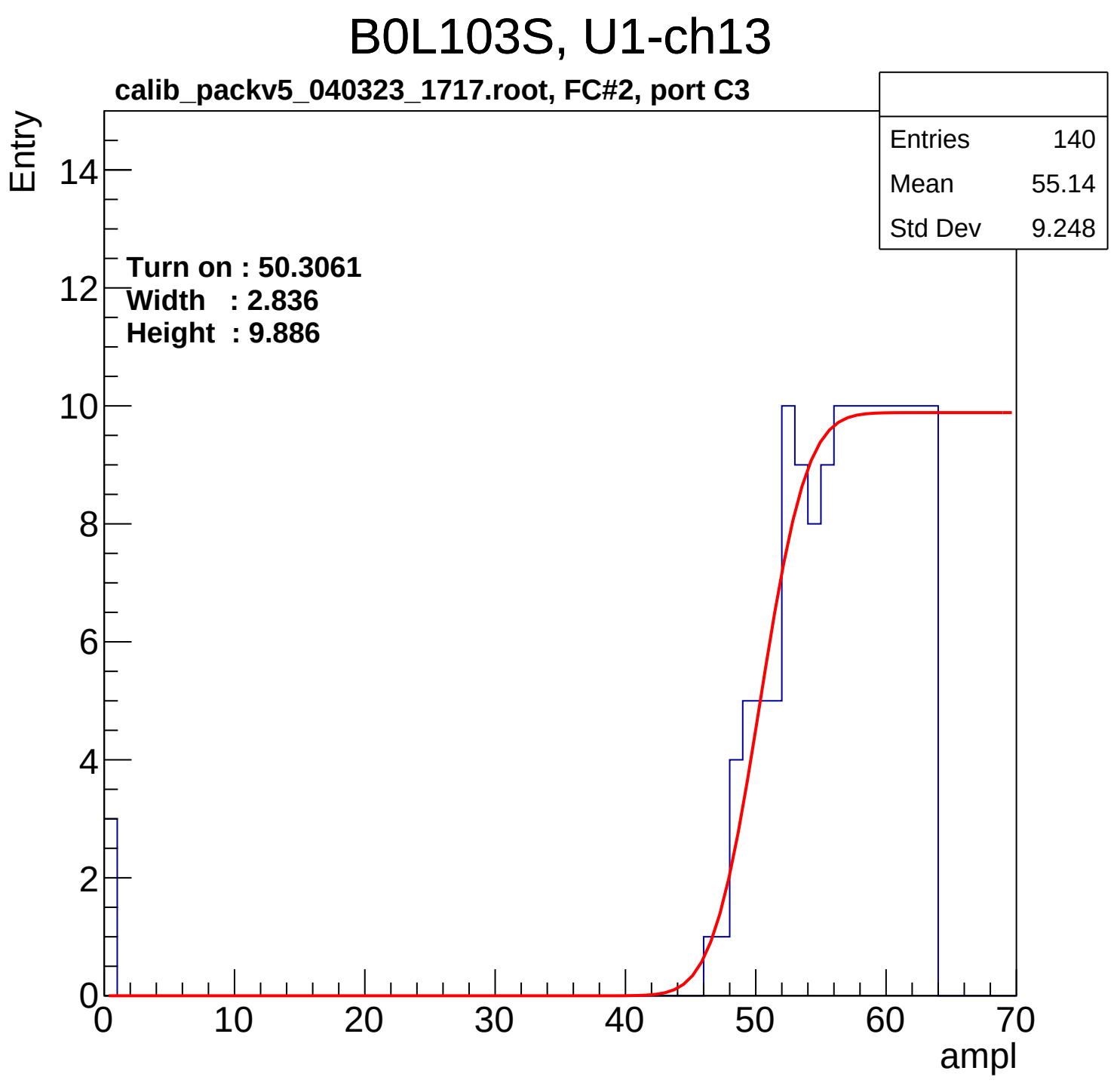
B0L103S, U1-ch13
calib_packv5_040323_1717.root, FC#2, port C3
Entries 140
Mean 55.14
Std Dev 9.248
Turn on : 50.3061
Width : 2.836
Height : 9.886
Entry
ampl
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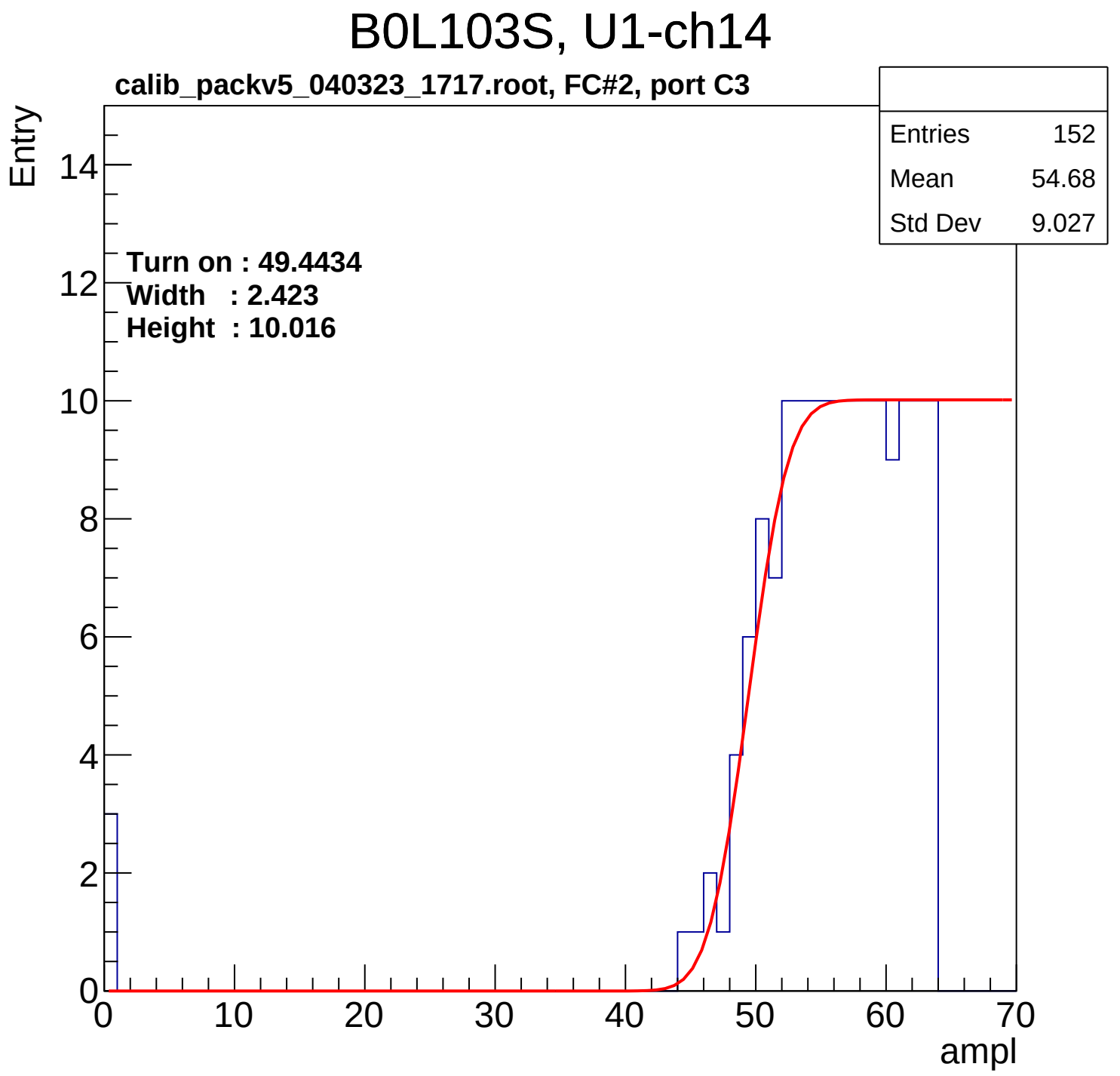
B0L103S, U1-ch14
calib_packv5_040323_1717.root, FC#2, port C3
Entries 152
Mean 54.68
Std Dev 9.027
Turn on : 49.4434
Width : 2.423
Height : 10.016
Entry
ampl
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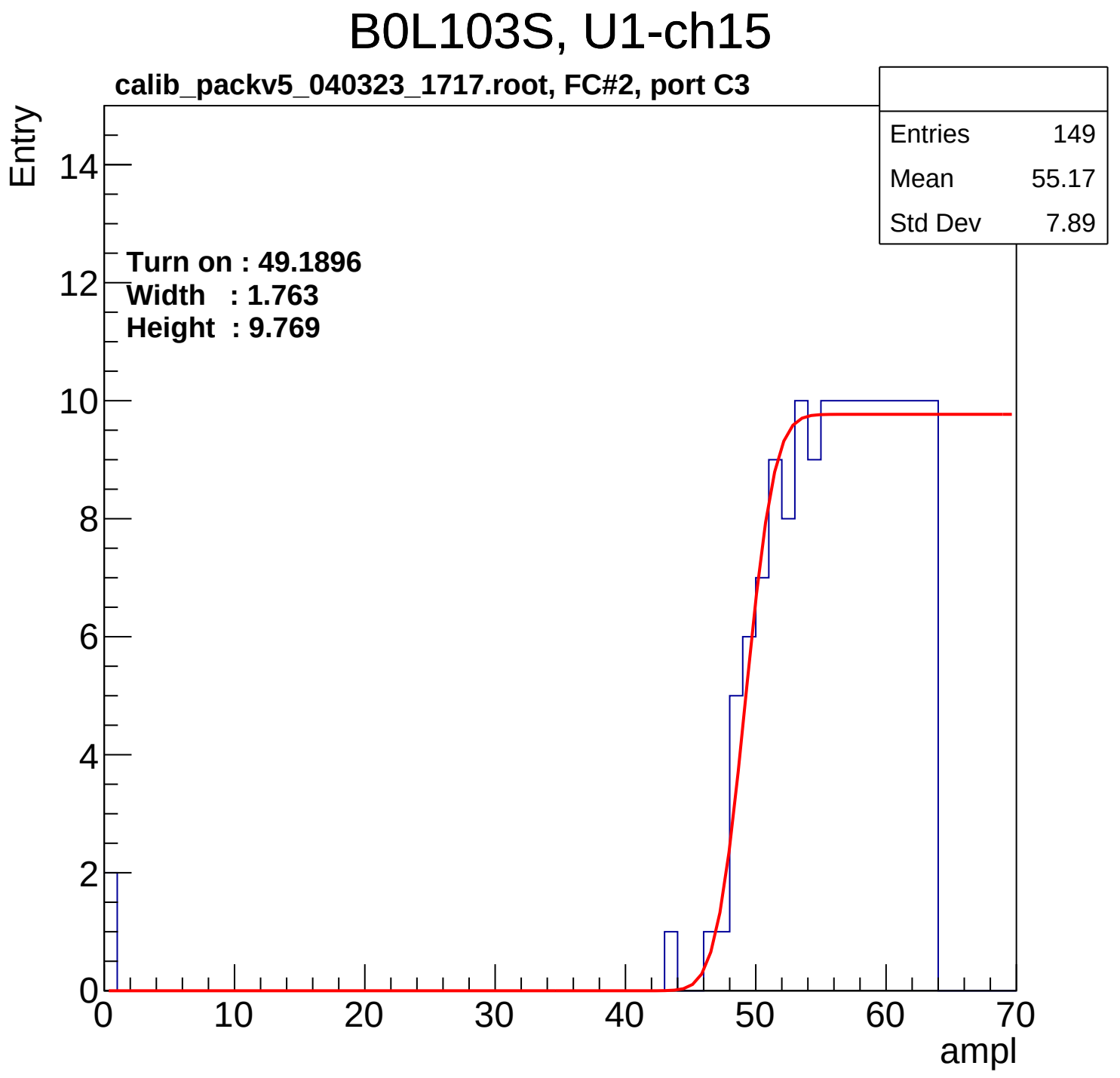
B0L103S, U1-ch15
calib_packv5_040323_1717.root, FC#2, port C3
Entries 149
Mean 55.17
Std Dev 7.89
Turn on : 49.1896
Width : 1.763
Height : 9.769
Entry
ampl
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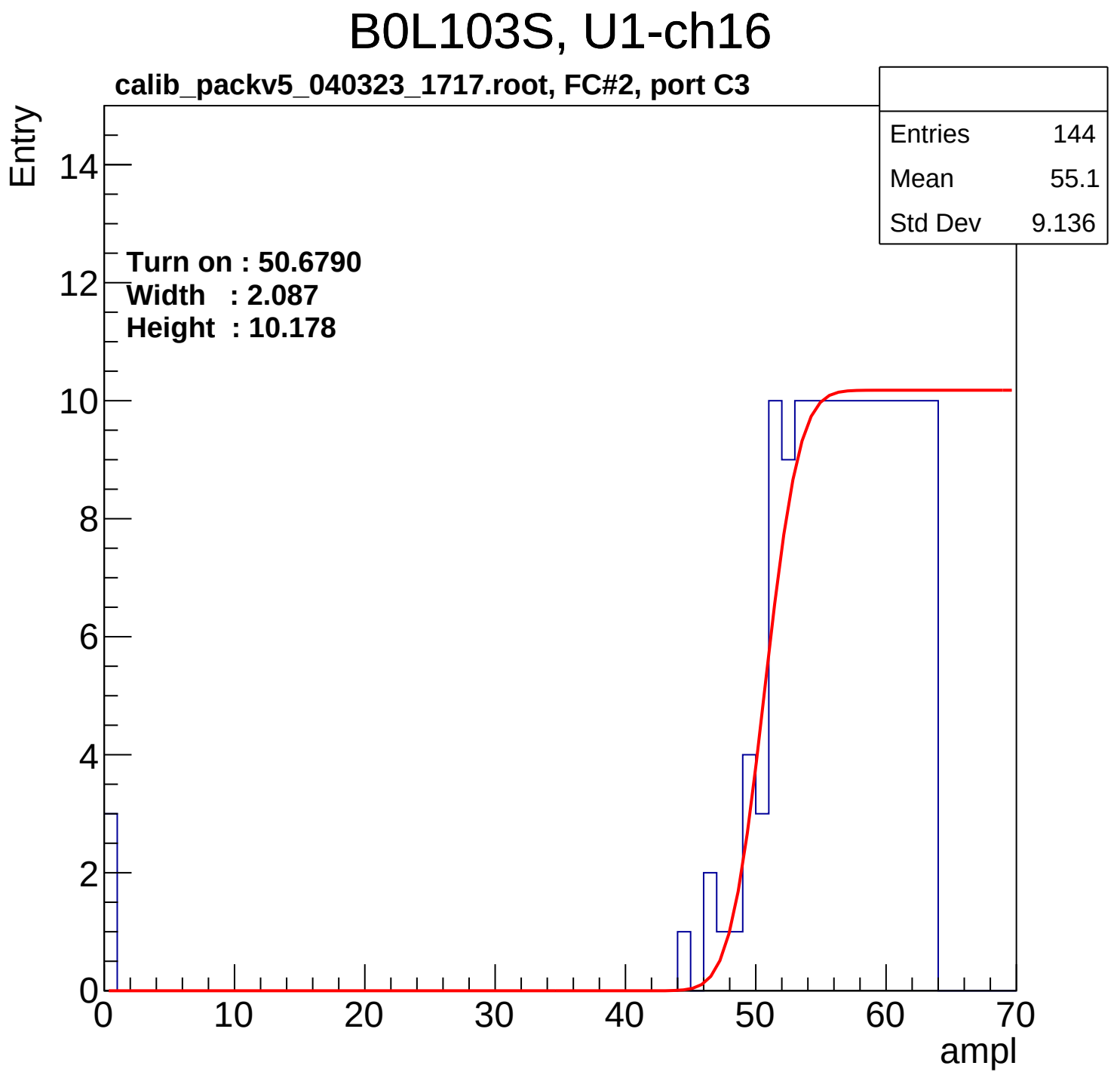
B0L103S, U1-ch16
calib_packv5_040323_1717.root, FC#2, port C3
Entries 144
Mean 55.1
Std Dev 9.136
Turn on : 50.6790
Width : 2.087
Height : 10.178
Entry
ampl
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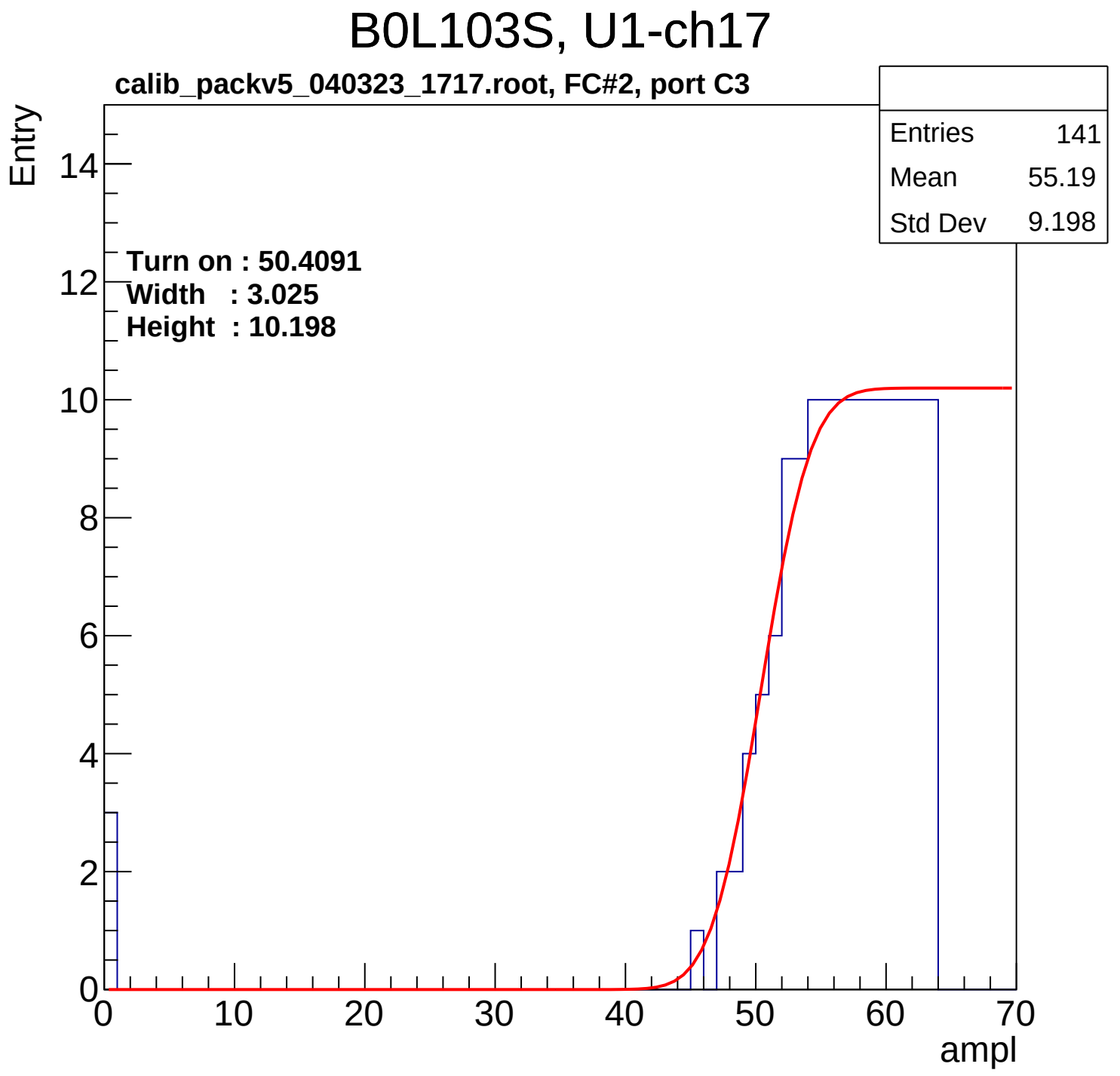
B0L103S, U1-ch17
calib_packv5_040323_1717.root, FC#2, port C3
Entries 141
Mean 55.19
Std Dev 9.198
Turn on : 50.4091
Width : 3.025
Height : 10.198
Entry
ampl
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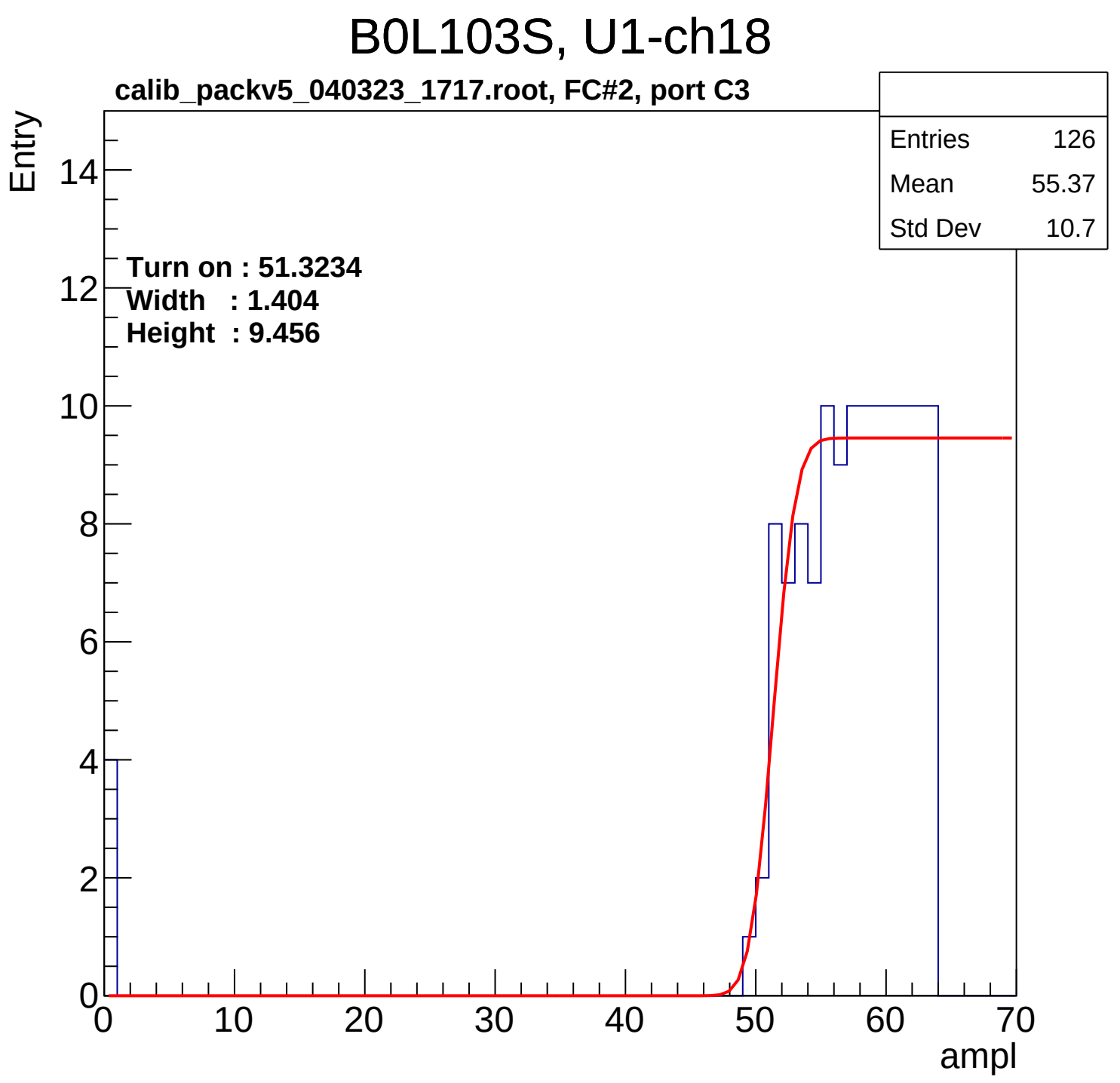
B0L103S, U1-ch18
calib_packv5_040323_1717.root, FC#2, port C3
Entries 126
Mean 55.37
Std Dev 10.7
Turn on : 51.3234
Width : 1.404
Height : 9.456
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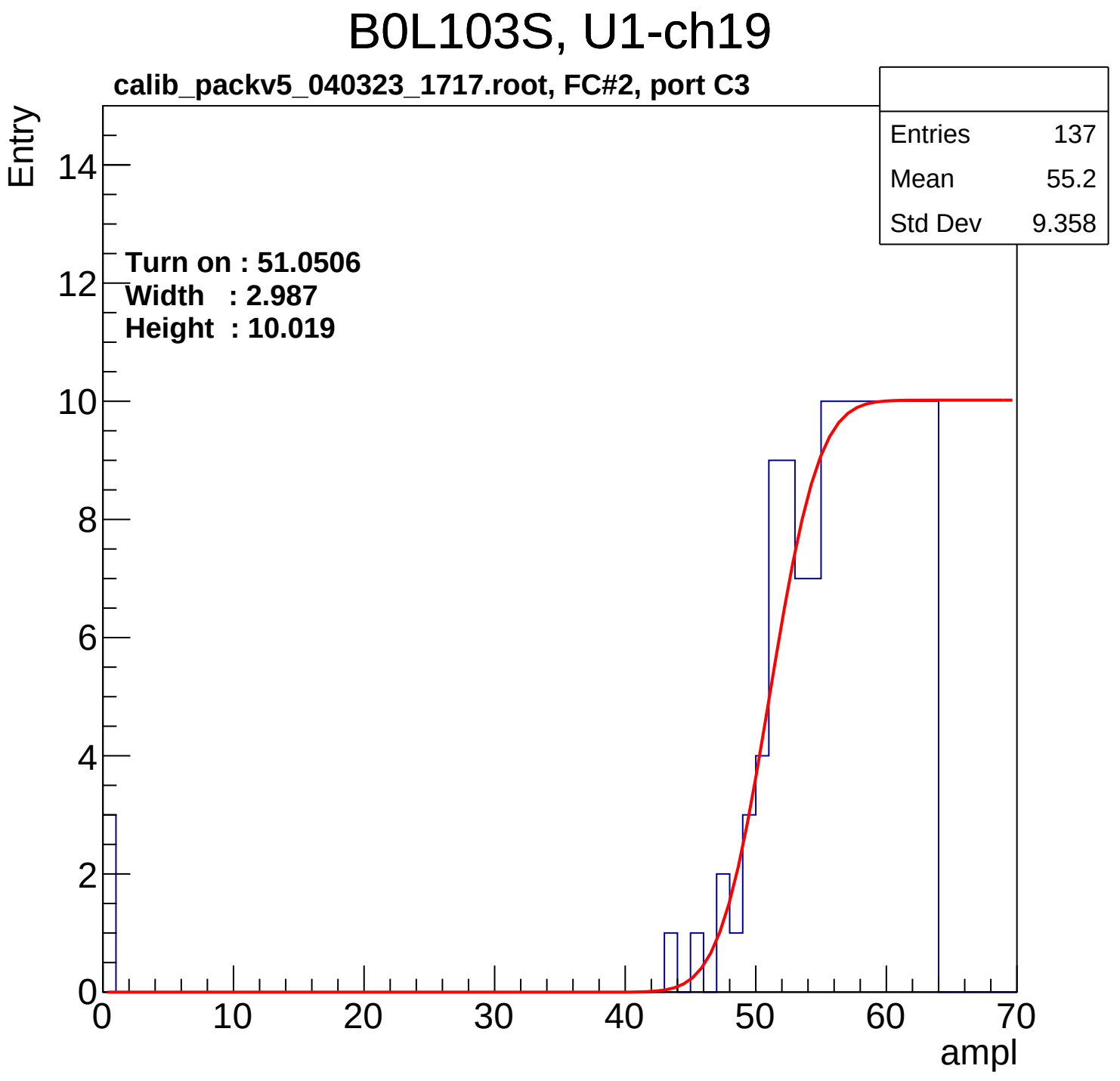
B0L103S, U1-ch19
calib_packv5_040323_1717.root, FC#2, port C3
Entries 137
Mean 55.2
Std Dev 9.358
Turn on : 51.0506
Width : 2.987
Height : 10.019
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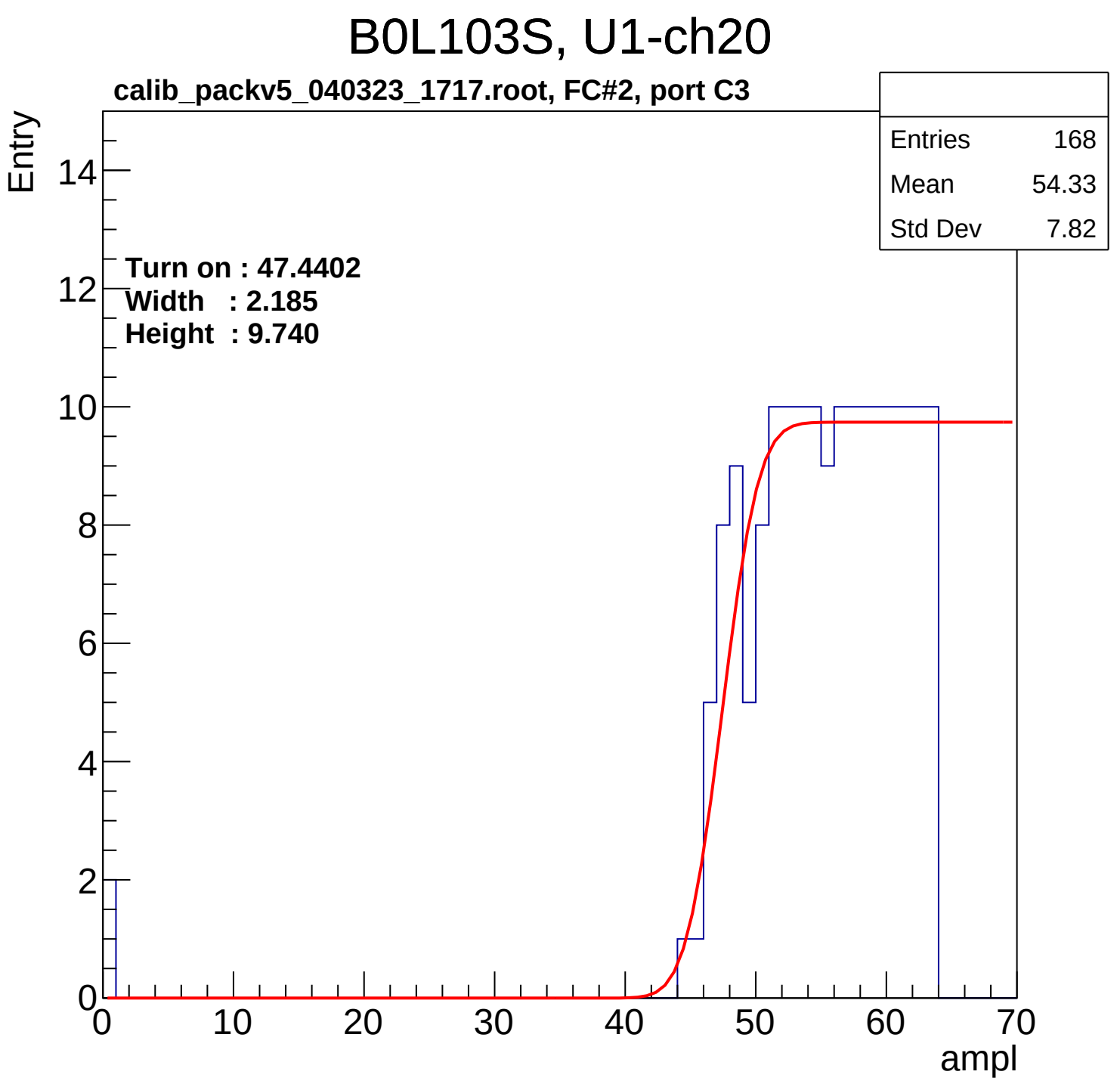
B0L103S, U1-ch20
calib_packv5_040323_1717.root, FC#2, port C3
Entries 168
Mean 54.33
Std Dev 7.82
Turn on : 47.4402
Width : 2.185
Height : 9.740
Entry
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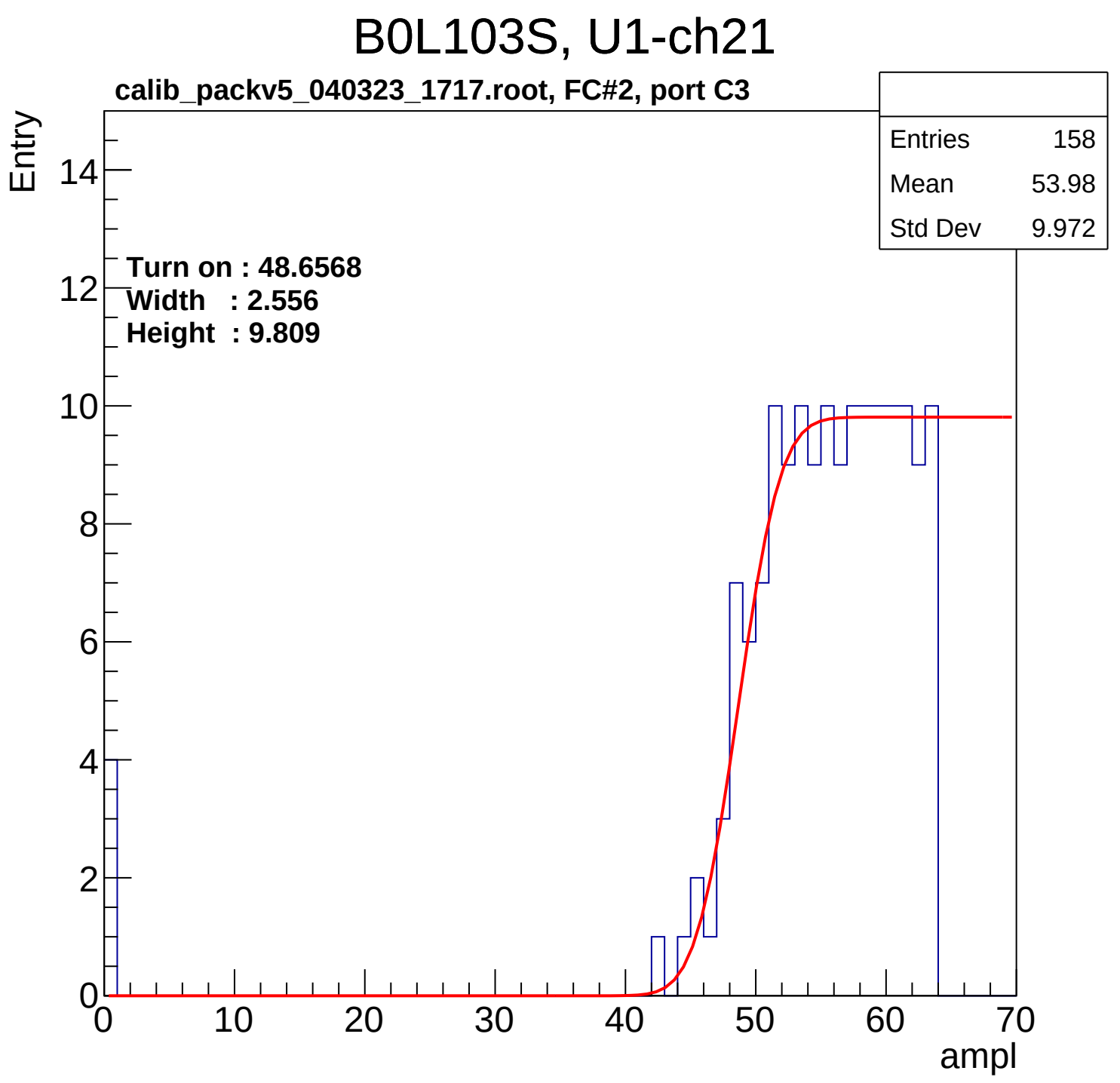
B0L103S, U1-ch21
calib_packv5_040323_1717.root, FC#2, port C3
Entries 158
Mean 53.98
Std Dev 9.972
Turn on : 48.6568
Width : 2.556
Height : 9.809
Entry
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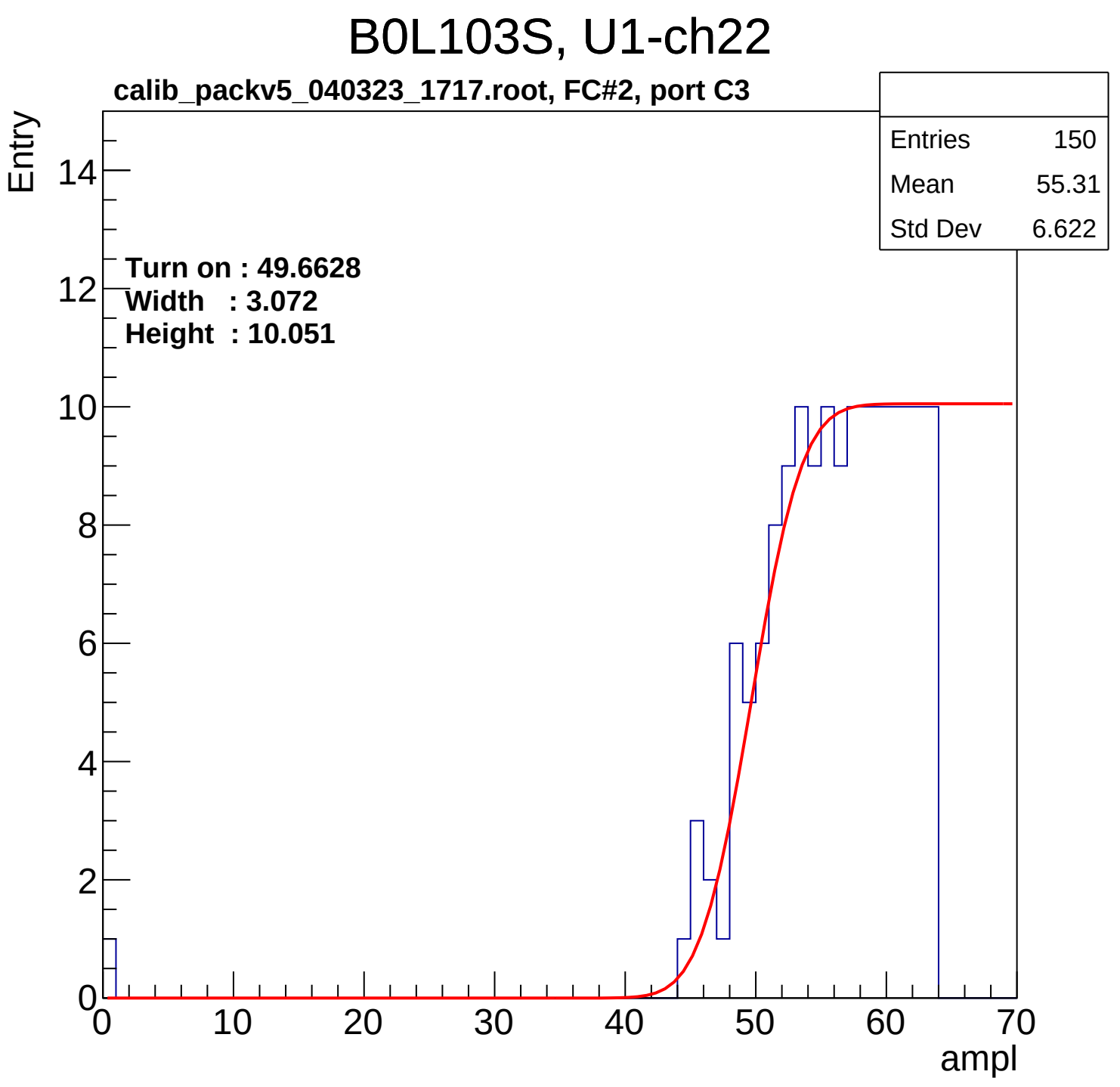
B0L103S, U1-ch22
calib_packv5_040323_1717.root, FC#2, port C3
Entries 150
Mean 55.31
Std Dev 6.622
Turn on : 49.6628
Width : 3.072
Height : 10.051
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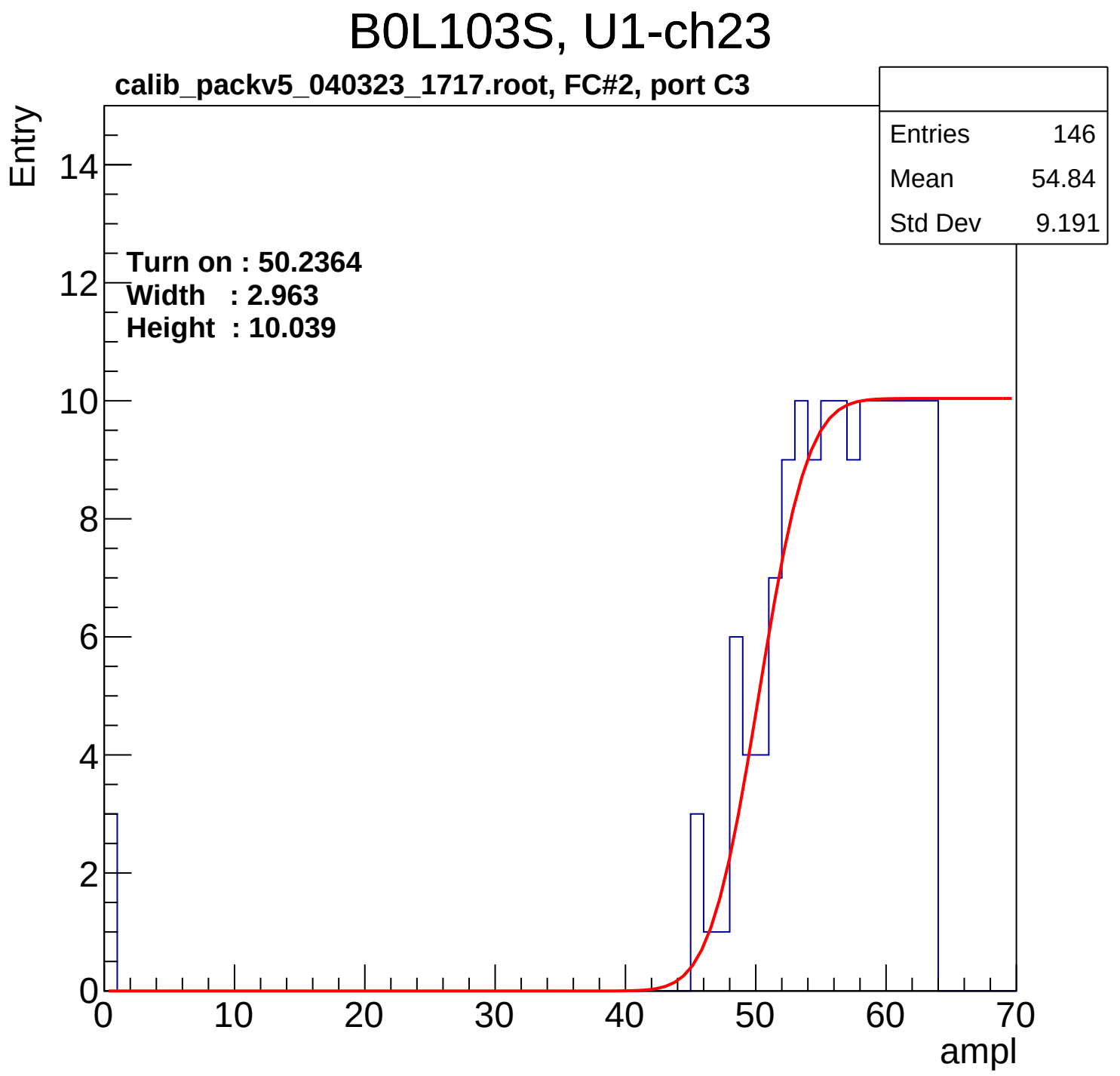
B0L103S, U1-ch23
calib_packv5_040323_1717.root, FC#2, port C3
Entries 146
Mean 54.84
Std Dev 9.191
Turn on : 50.2364
Width : 2.963
Height : 10.039
Entry
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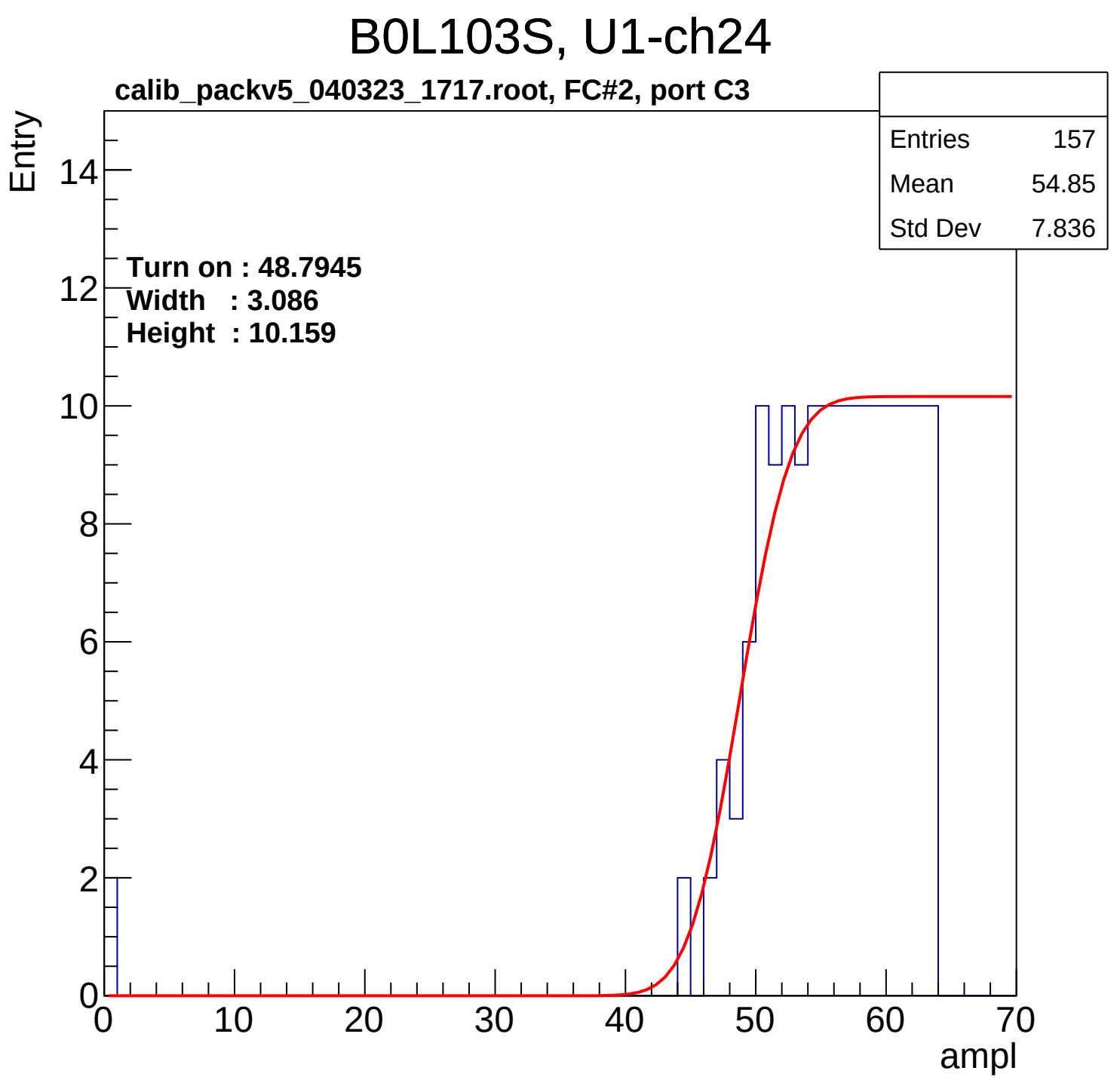
B0L103S, U1-ch24
calib_packv5_040323_1717.root, FC#2, port C3
Entries 157
Mean 54.85
Std Dev 7.836
Turn on : 48.7945
Width : 3.086
Height : 10.159
Entry
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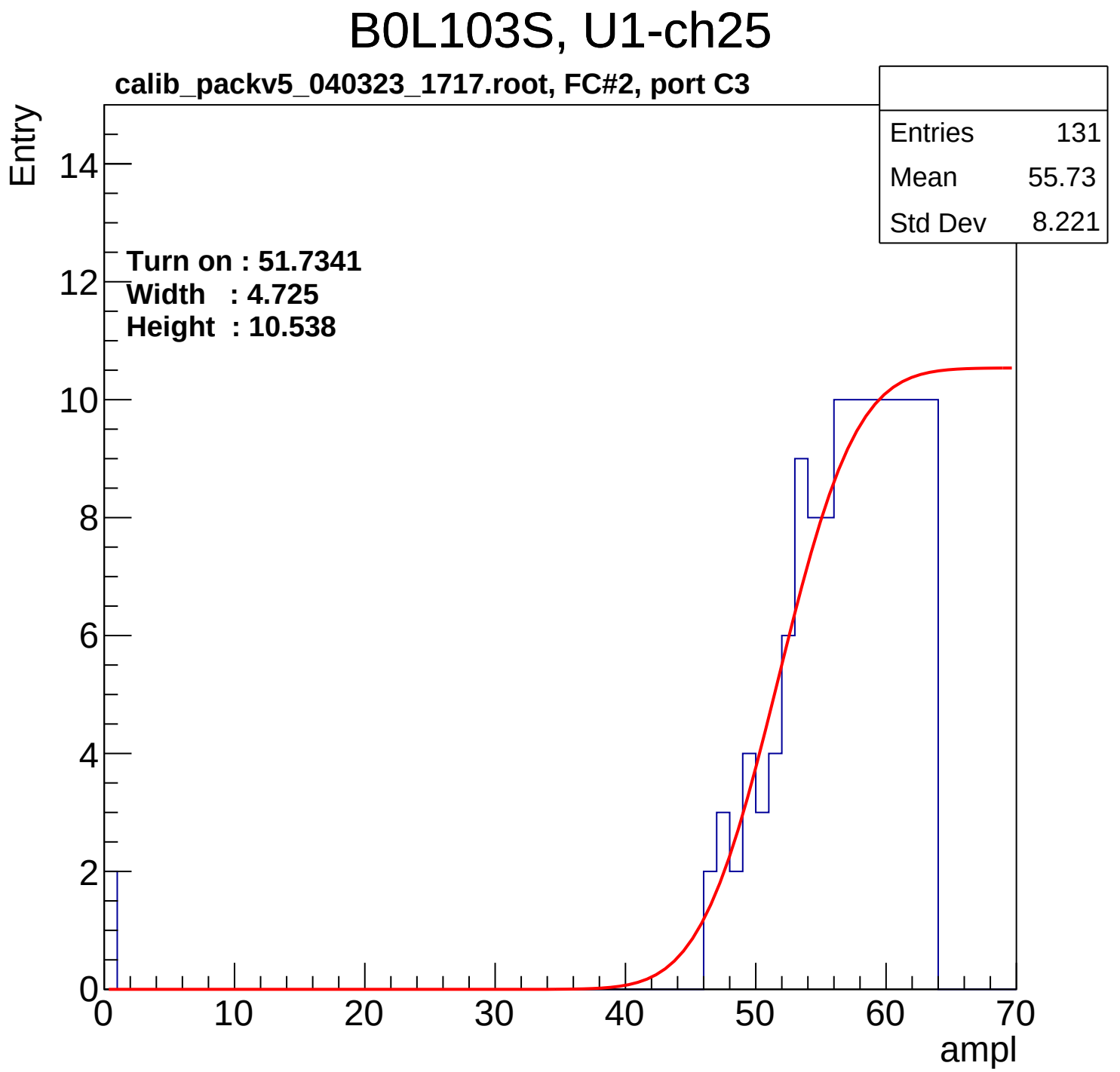
B0L103S, U1-ch25
calib_packv5_040323_1717.root, FC#2, port C3
Entries 131
Mean 55.73
Std Dev 8.221
Turn on : 51.7341
Width : 4.725
Height : 10.538
Entry
ampl
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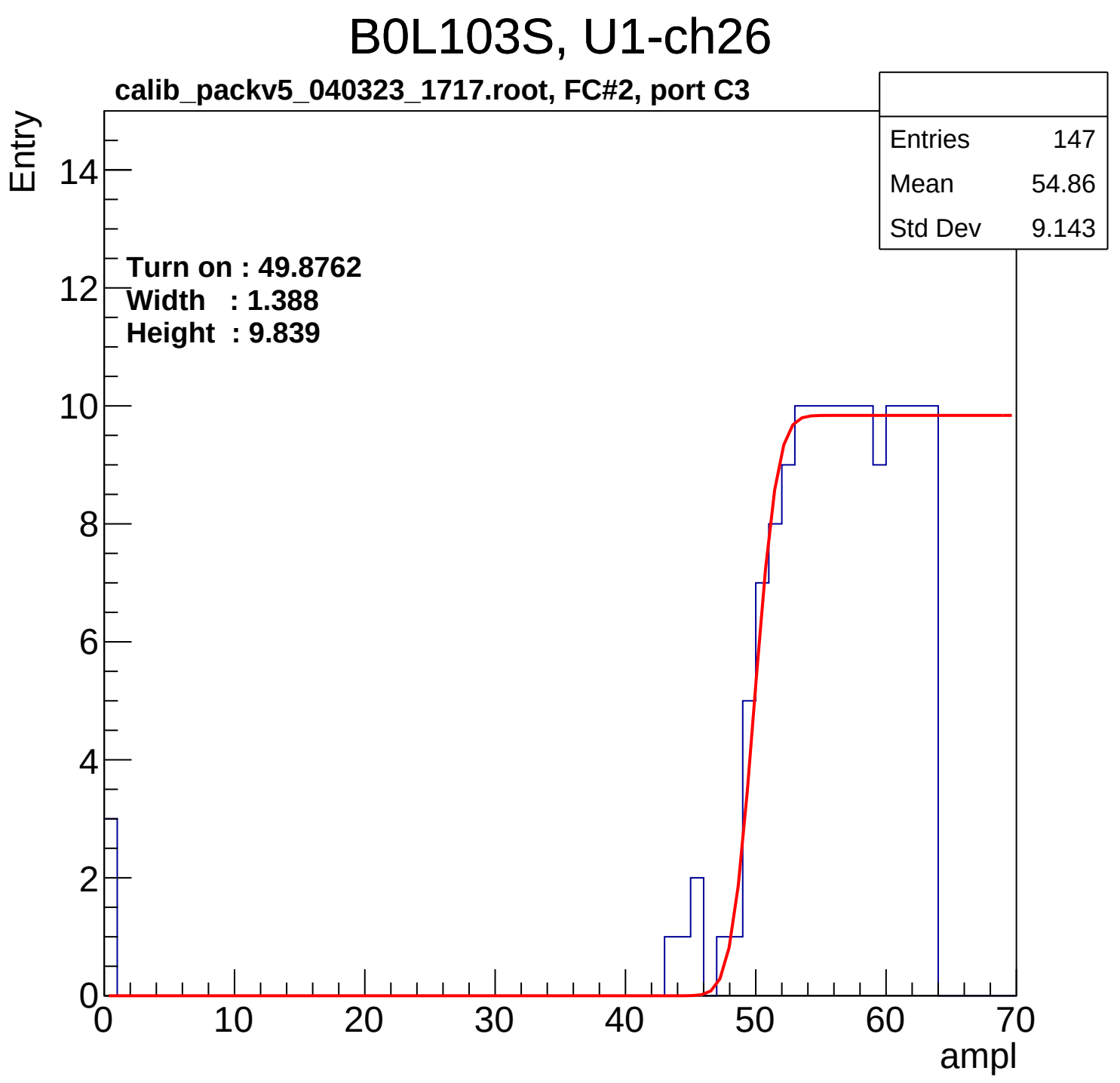
B0L103S, U1-ch26
calib_packv5_040323_1717.root, FC#2, port C3
Entries 147
Mean 54.86
Std Dev 9.143
Turn on : 49.8762
Width : 1.388
Height : 9.839
Entry
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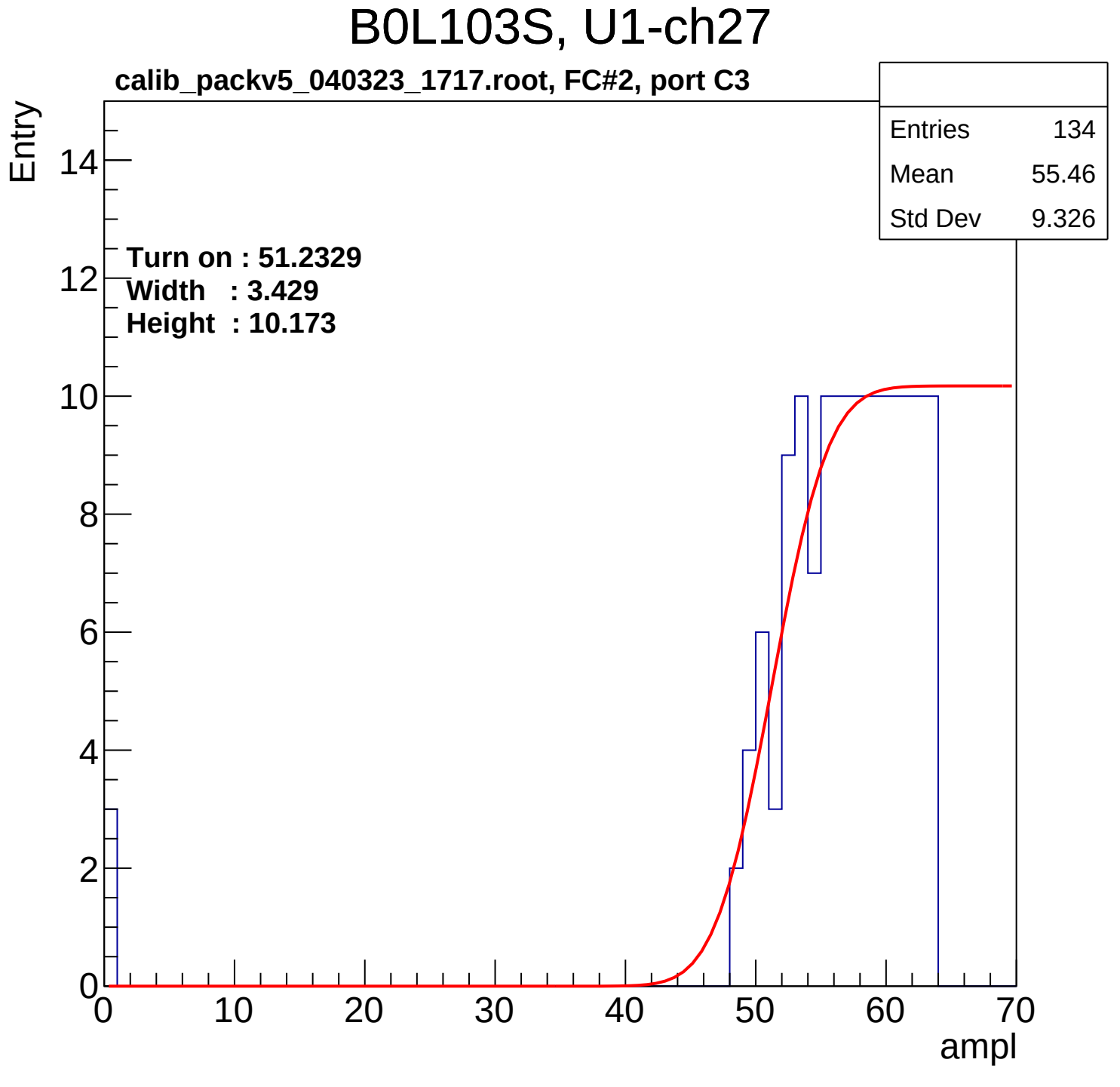
B0L103S, U1-ch27
calib_packv5_040323_1717.root, FC#2, port C3
Entries 134
Mean 55.46
Std Dev 9.326
Turn on : 51.2329
Width : 3.429
Height : 10.173
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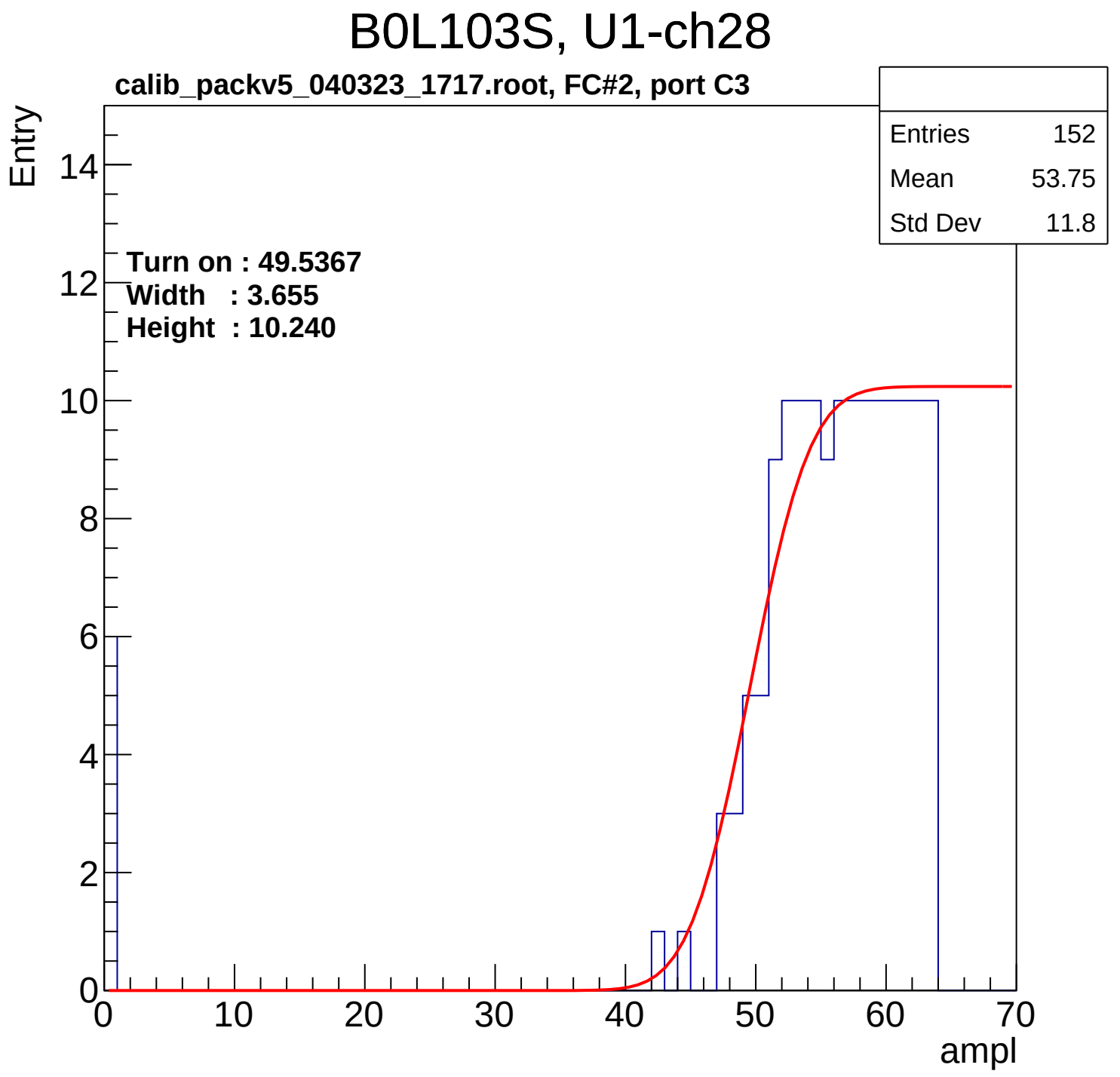
B0L103S, U1-ch28
calib_packv5_040323_1717.root, FC#2, port C3
Entries 152
Mean 53.75
Std Dev 11.8
Turn on : 49.5367
Width : 3.655
Height : 10.240
Entry
ampl
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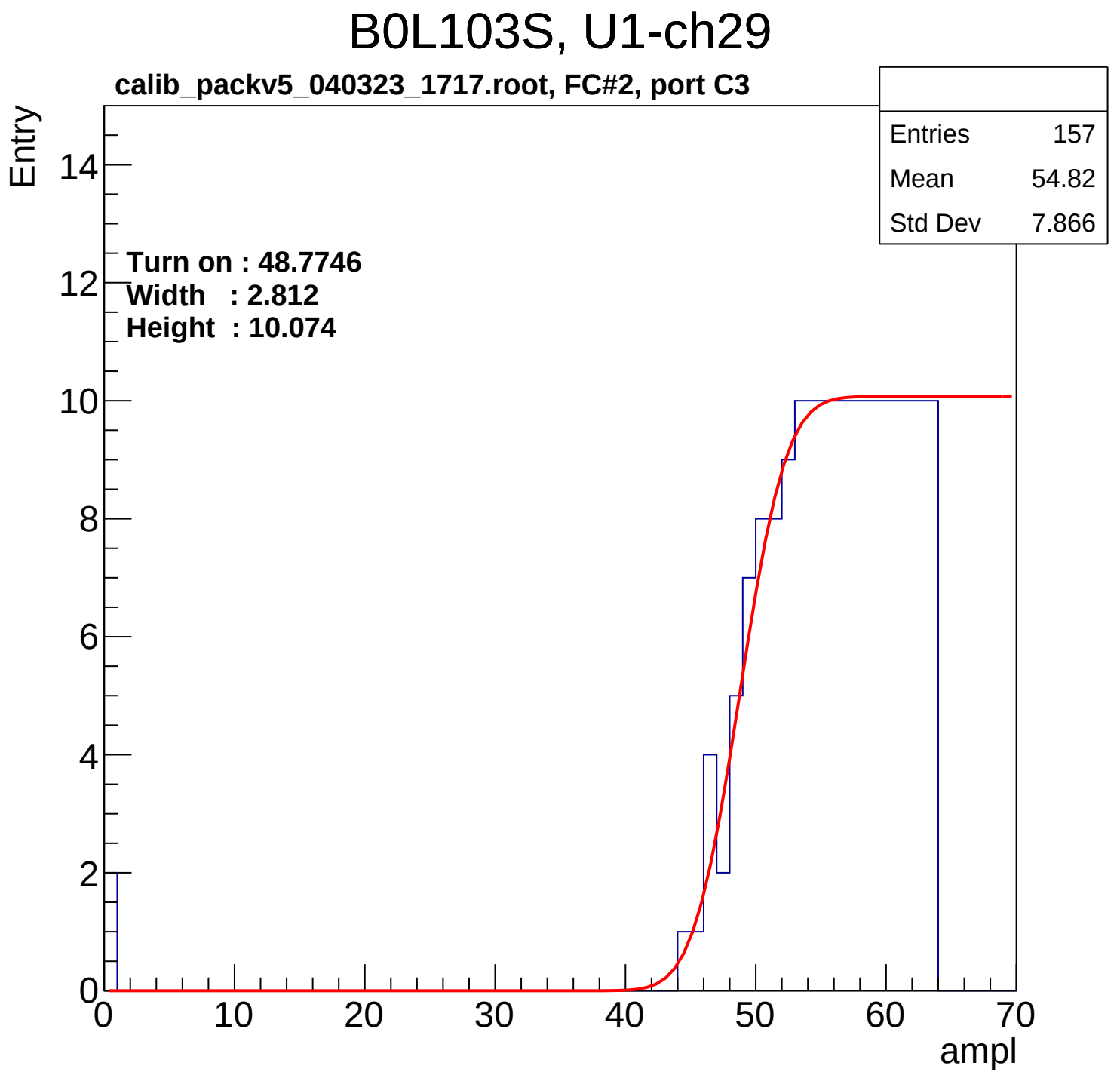
B0L103S, U1-ch29
calib_packv5_040323_1717.root, FC#2, port C3
Entries 157
Mean 54.82
Std Dev 7.866
Turn on : 48.7746
Width : 2.812
Height : 10.074
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ampl
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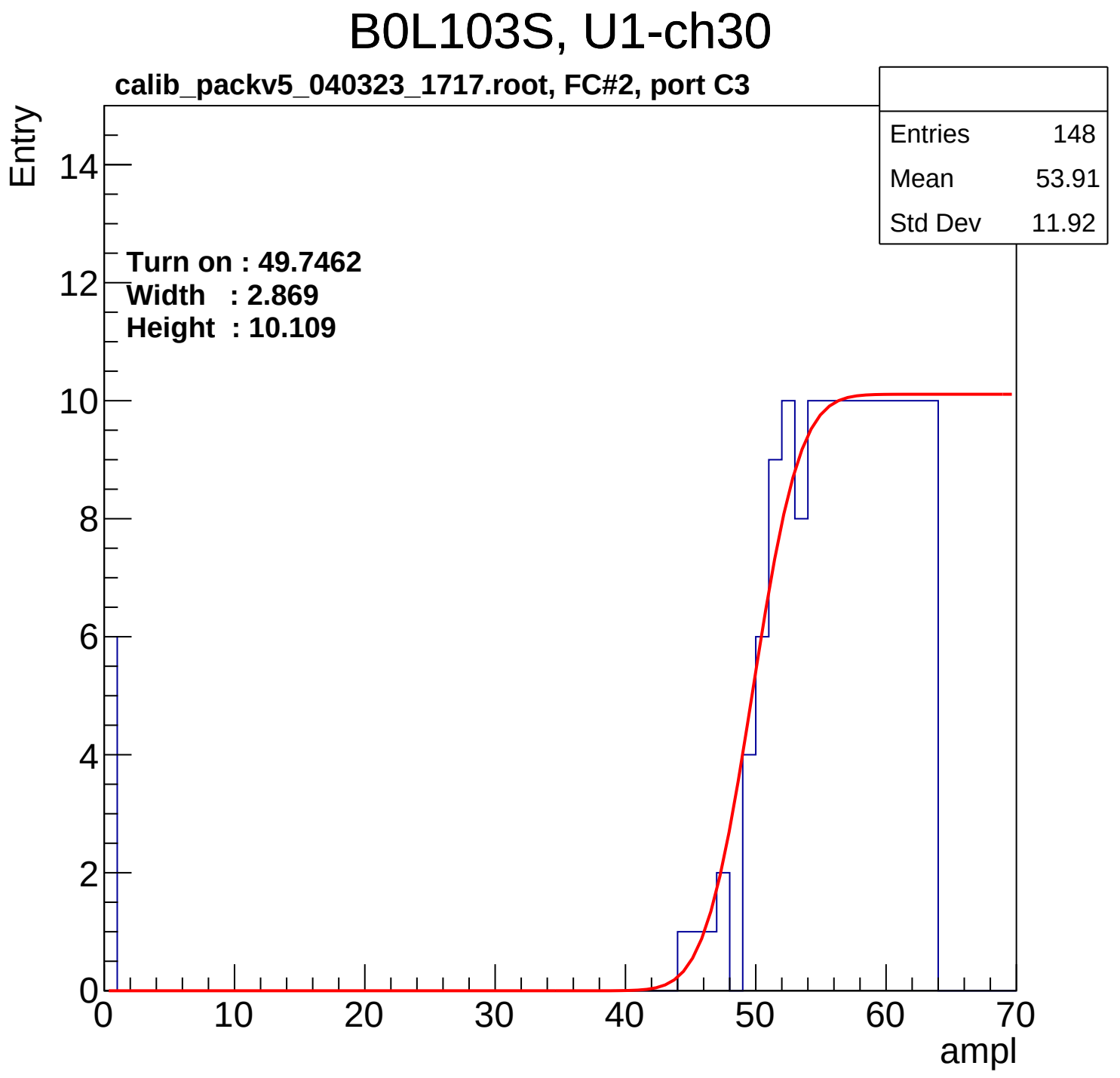
B0L103S, U1-ch30
calib_packv5_040323_1717.root, FC#2, port C3
Entries 148
Mean 53.91
Std Dev 11.92
Turn on : 49.7462
Width : 2.869
Height : 10.109
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ampl
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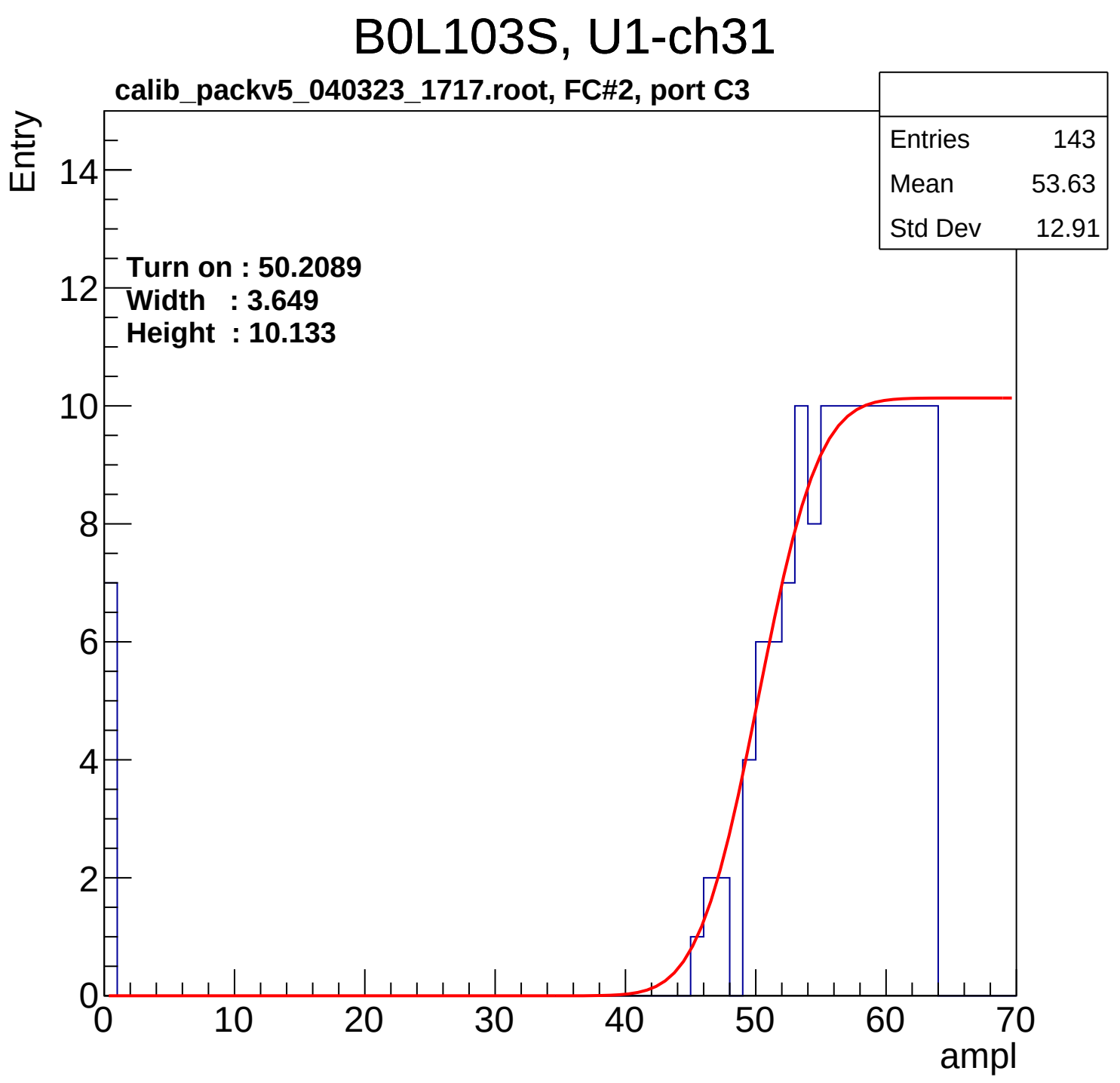
B0L103S, U1-ch31
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 53.63
Std Dev 12.91
Turn on : 50.2089
Width : 3.649
Height : 10.133
Entry
ampl
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4
6
8
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12
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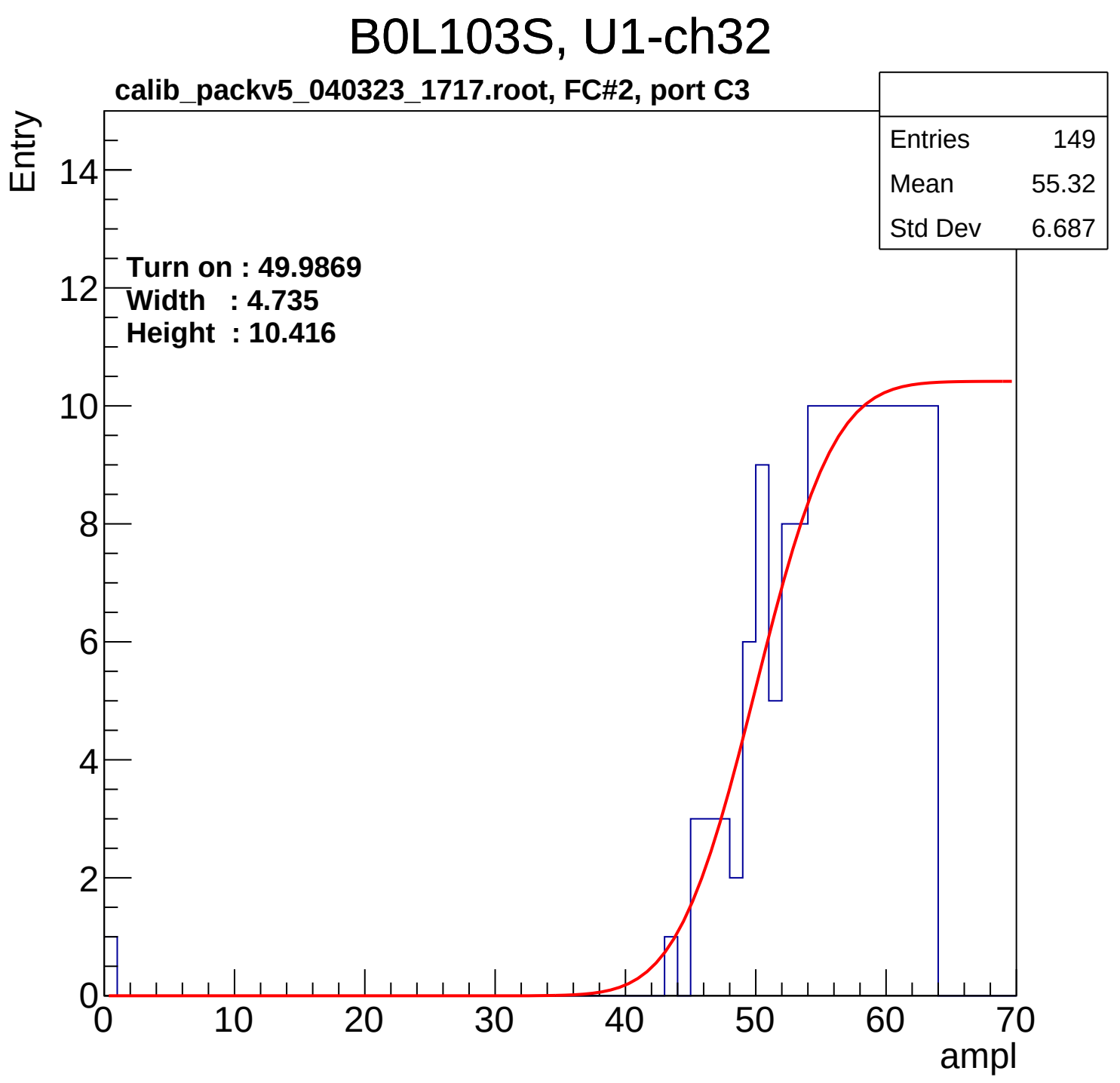
B0L103S, U1-ch32
calib_packv5_040323_1717.root, FC#2, port C3
Entries 149
Mean 55.32
Std Dev 6.687
Turn on : 49.9869
Width : 4.735
Height : 10.416
Entry
ampl
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6
8
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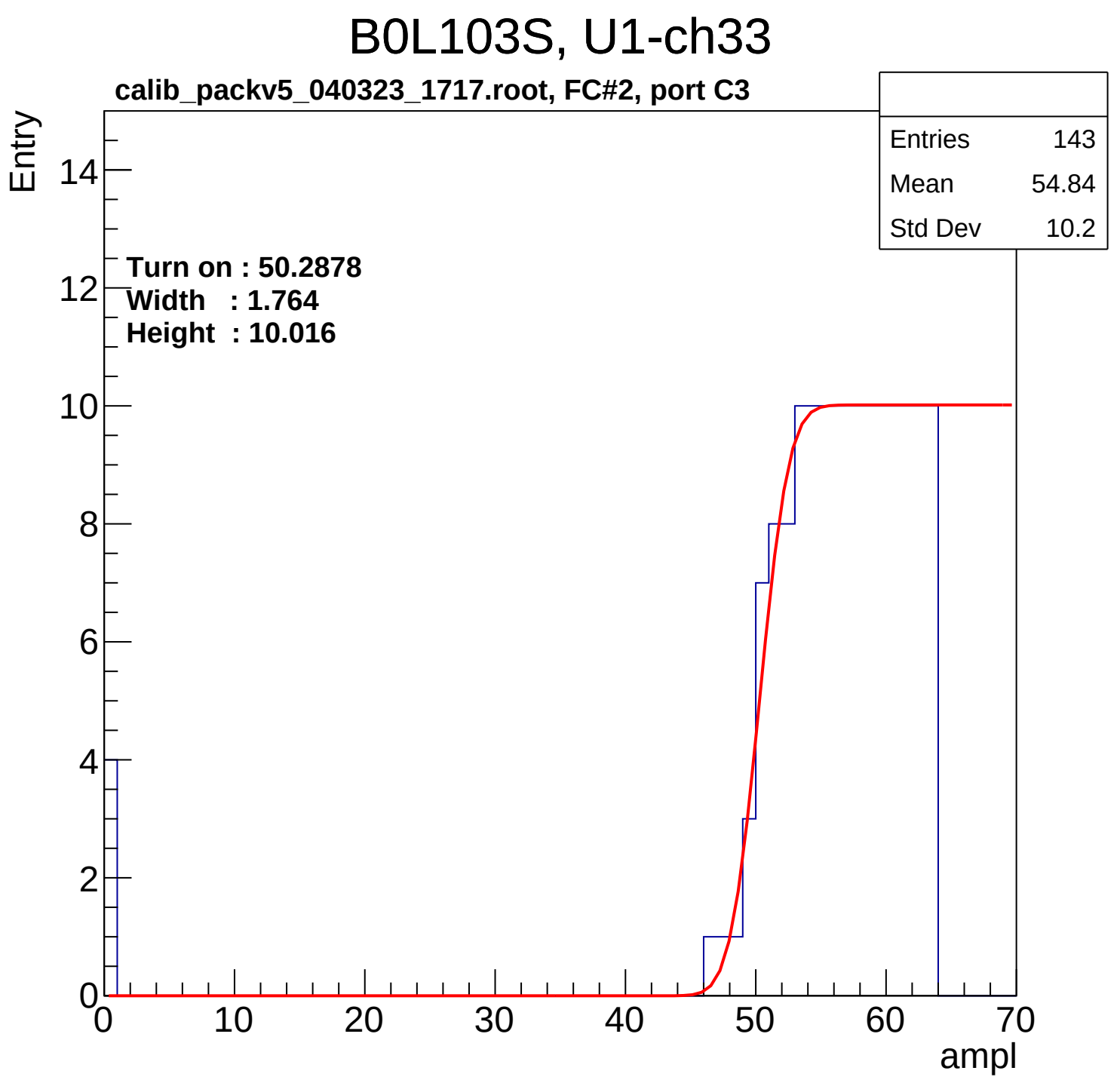
B0L103S, U1-ch33
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 54.84
Std Dev 10.2
Turn on : 50.2878
Width : 1.764
Height : 10.016
Entry
ampl
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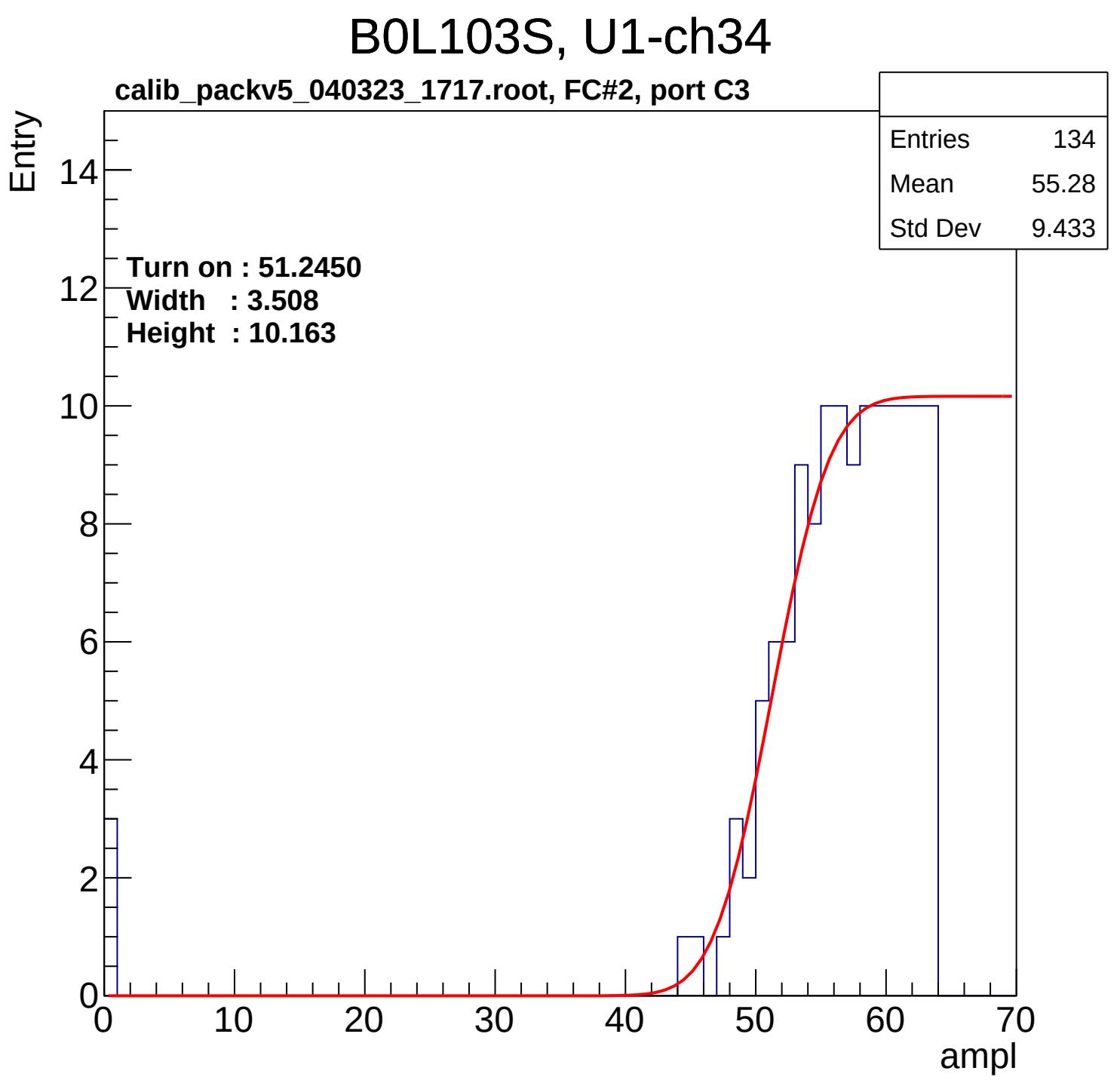
B0L103S, U1-ch34
calib_packv5_040323_1717.root, FC#2, port C3
Entries 134
Mean 55.28
Std Dev 9.433
Turn on : 51.2450
Width : 3.508
Height : 10.163
Entry
ampl
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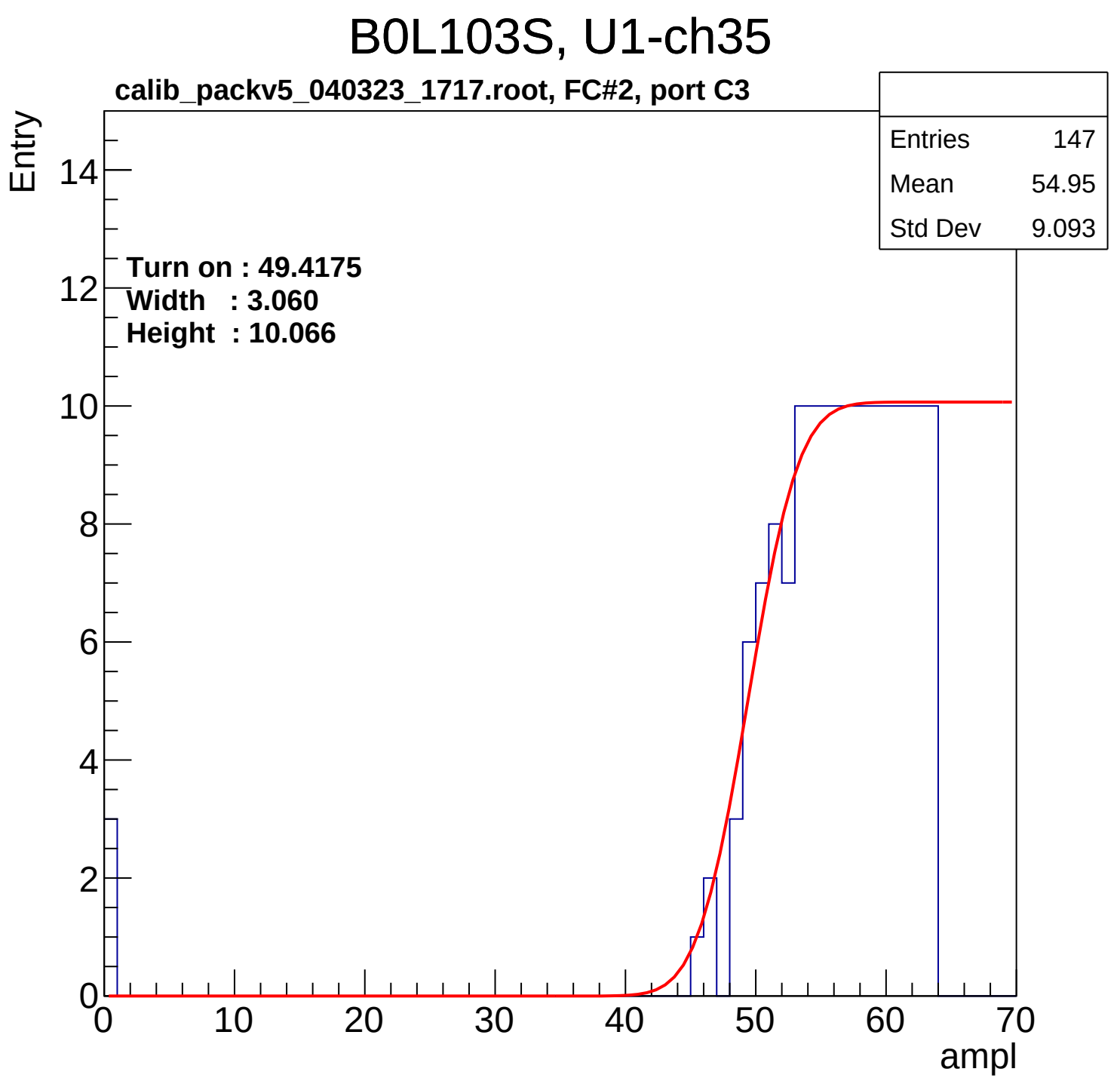
B0L103S, U1-ch35
calib_packv5_040323_1717.root, FC#2, port C3
Entries 147
Mean 54.95
Std Dev 9.093
Turn on : 49.4175
Width : 3.060
Height : 10.066
Entry
ampl
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6
8
10
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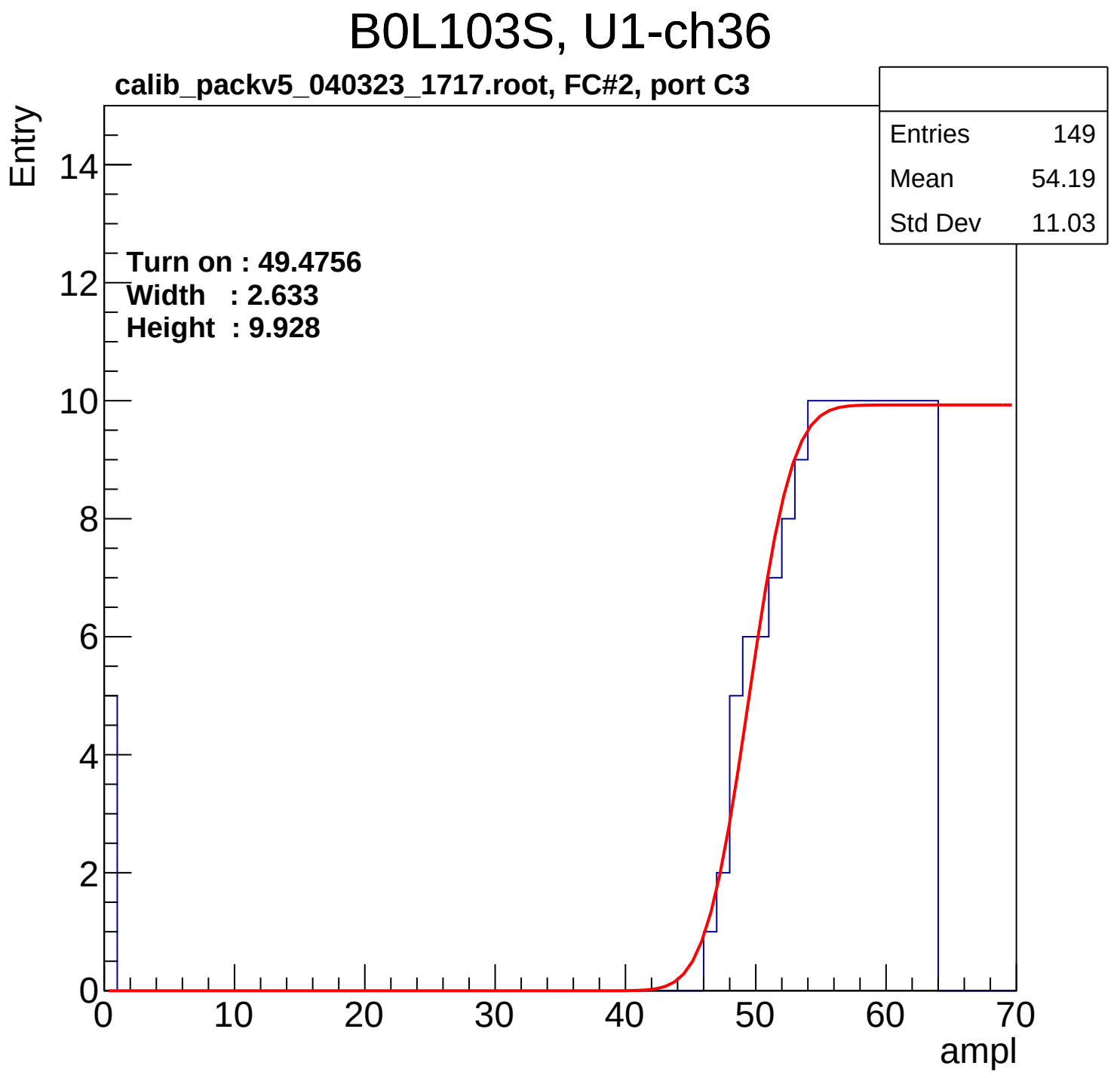
B0L103S, U1-ch36
calib_packv5_040323_1717.root, FC#2, port C3
Entries 149
Mean 54.19
Std Dev 11.03
Turn on : 49.4756
Width : 2.633
Height : 9.928
Entry
ampl
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2
4
6
8
10
12
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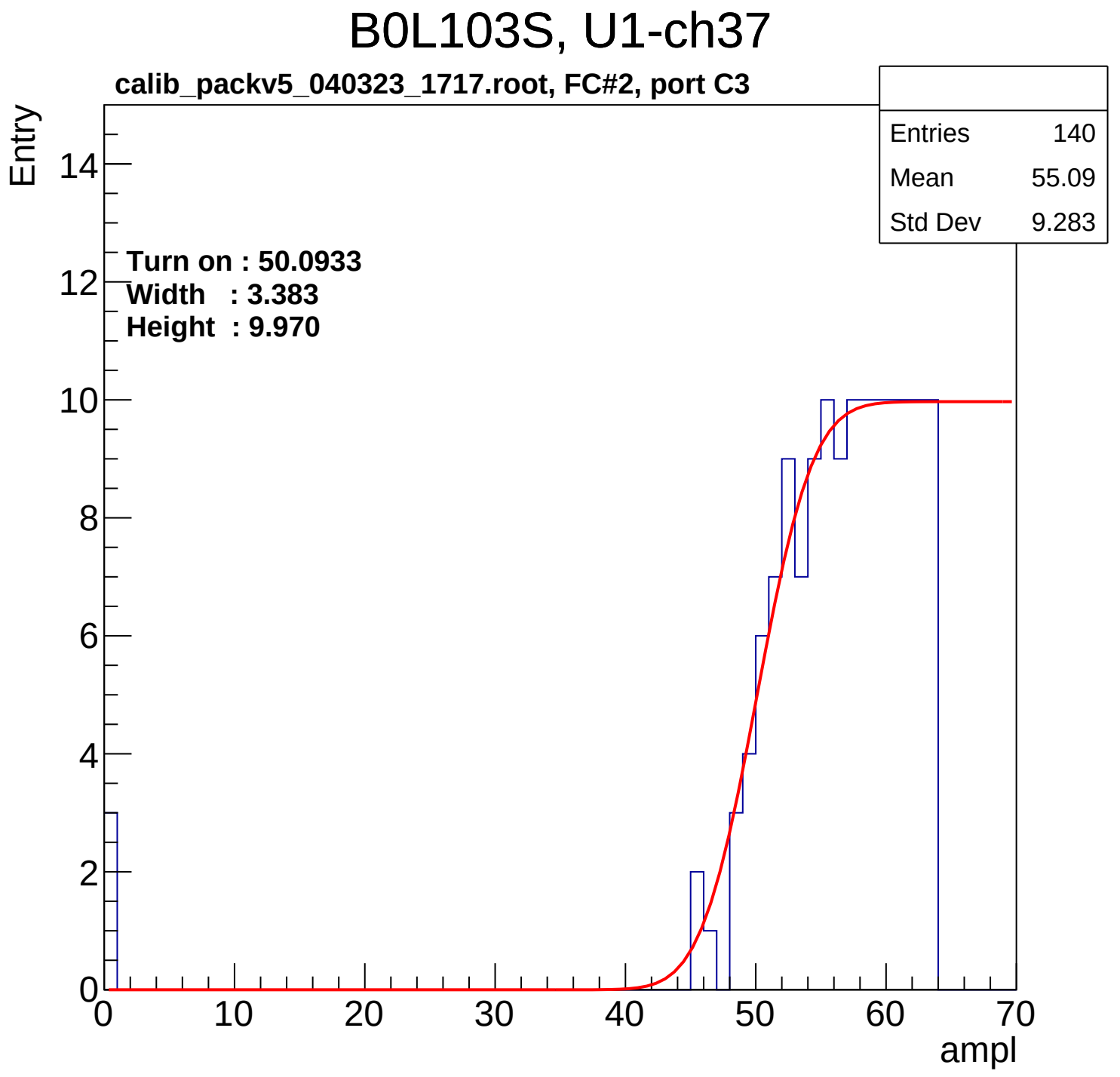
B0L103S, U1-ch37
calib_packv5_040323_1717.root, FC#2, port C3
Entries 140
Mean 55.09
Std Dev 9.283
Turn on : 50.0933
Width : 3.383
Height : 9.970
Entry
ampl
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6
8
10
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0
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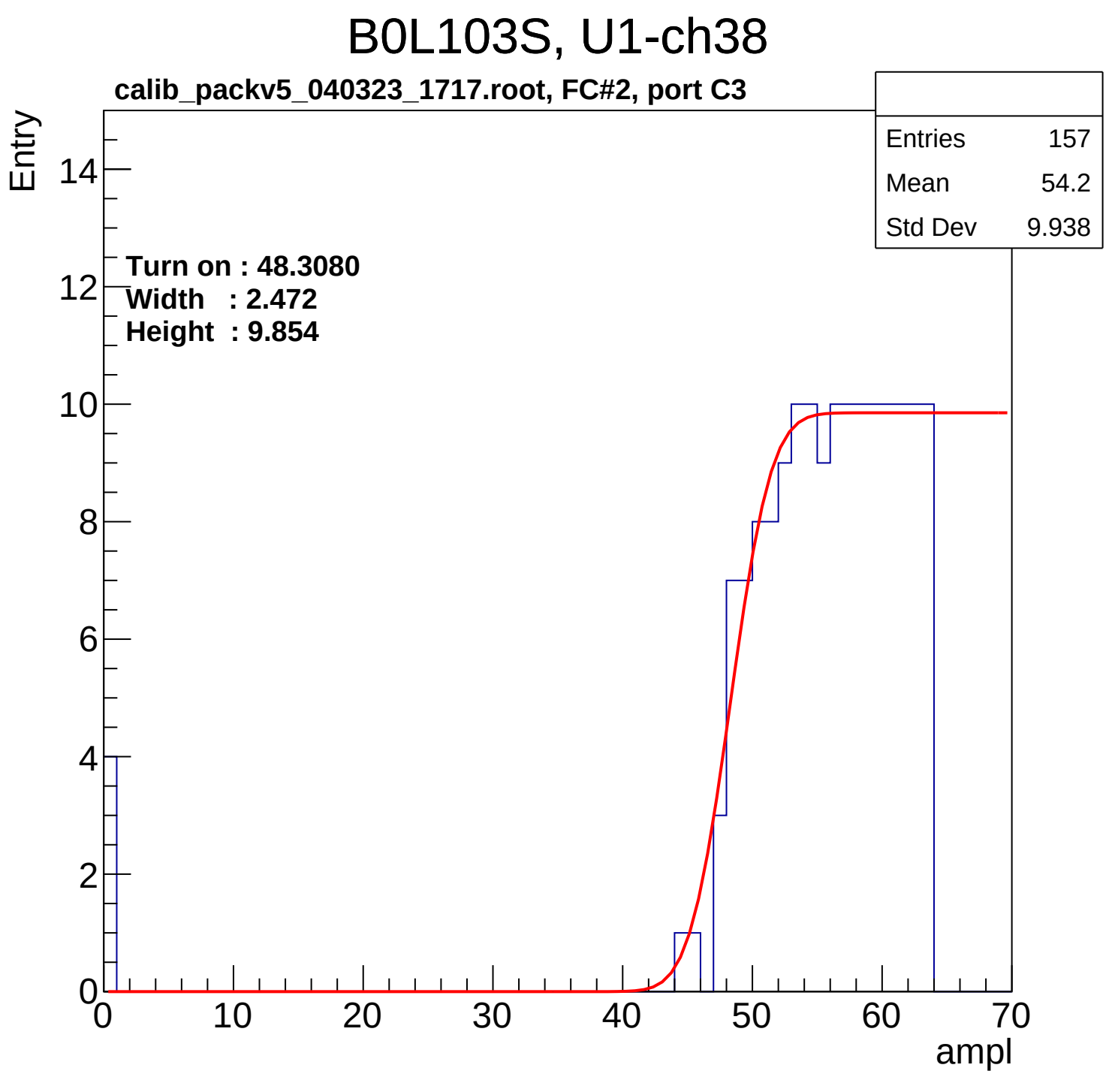
B0L103S, U1-ch38
calib_packv5_040323_1717.root, FC#2, port C3
Entries 157
Mean 54.2
Std Dev 9.938
Turn on : 48.3080
Width : 2.472
Height : 9.854
Entry
ampl
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6
8
10
12
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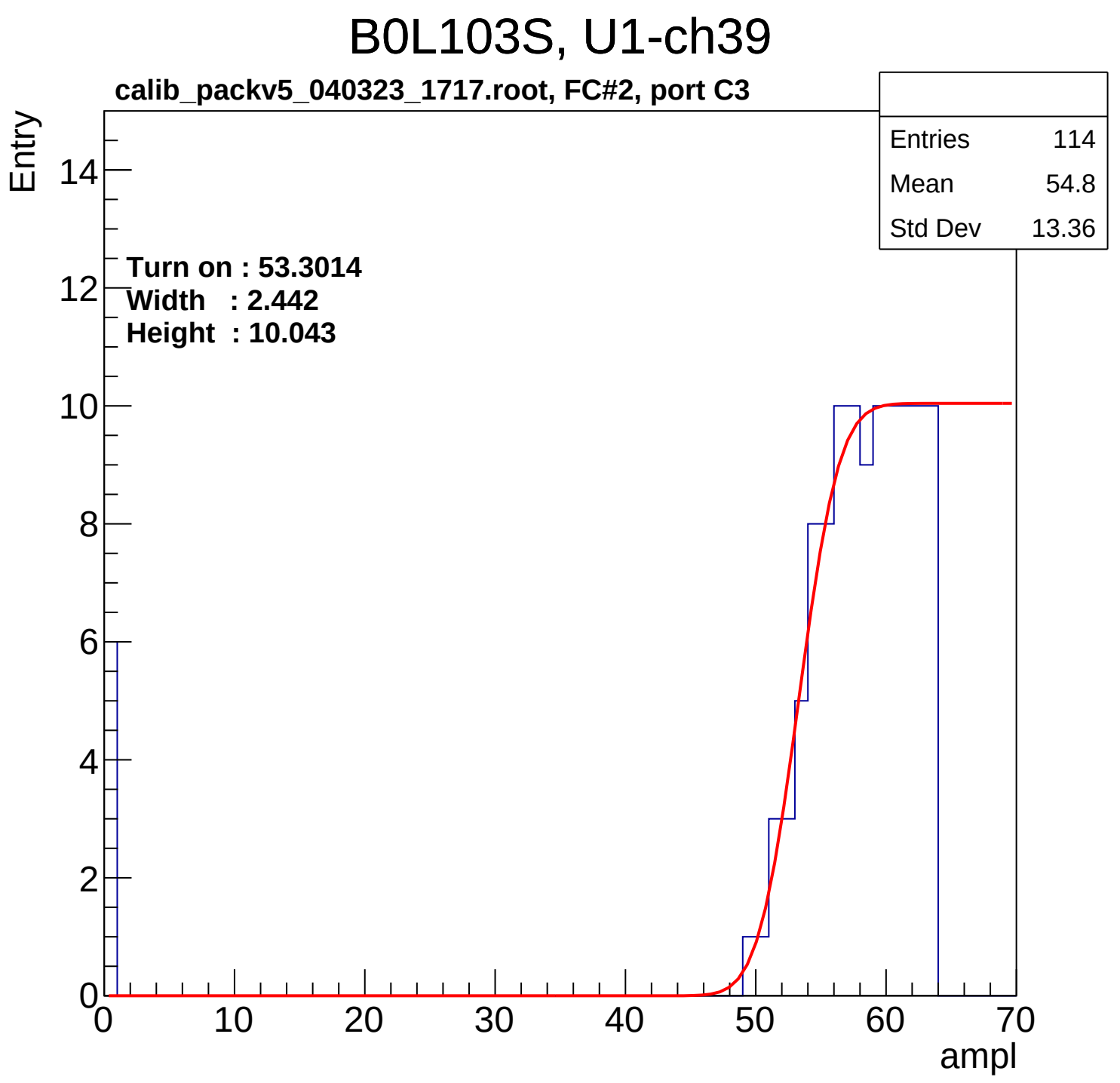
B0L103S, U1-ch39
calib_packv5_040323_1717.root, FC#2, port C3
Entries 114
Mean 54.8
Std Dev 13.36
Turn on : 53.3014
Width : 2.442
Height : 10.043
Entry
ampl
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6
8
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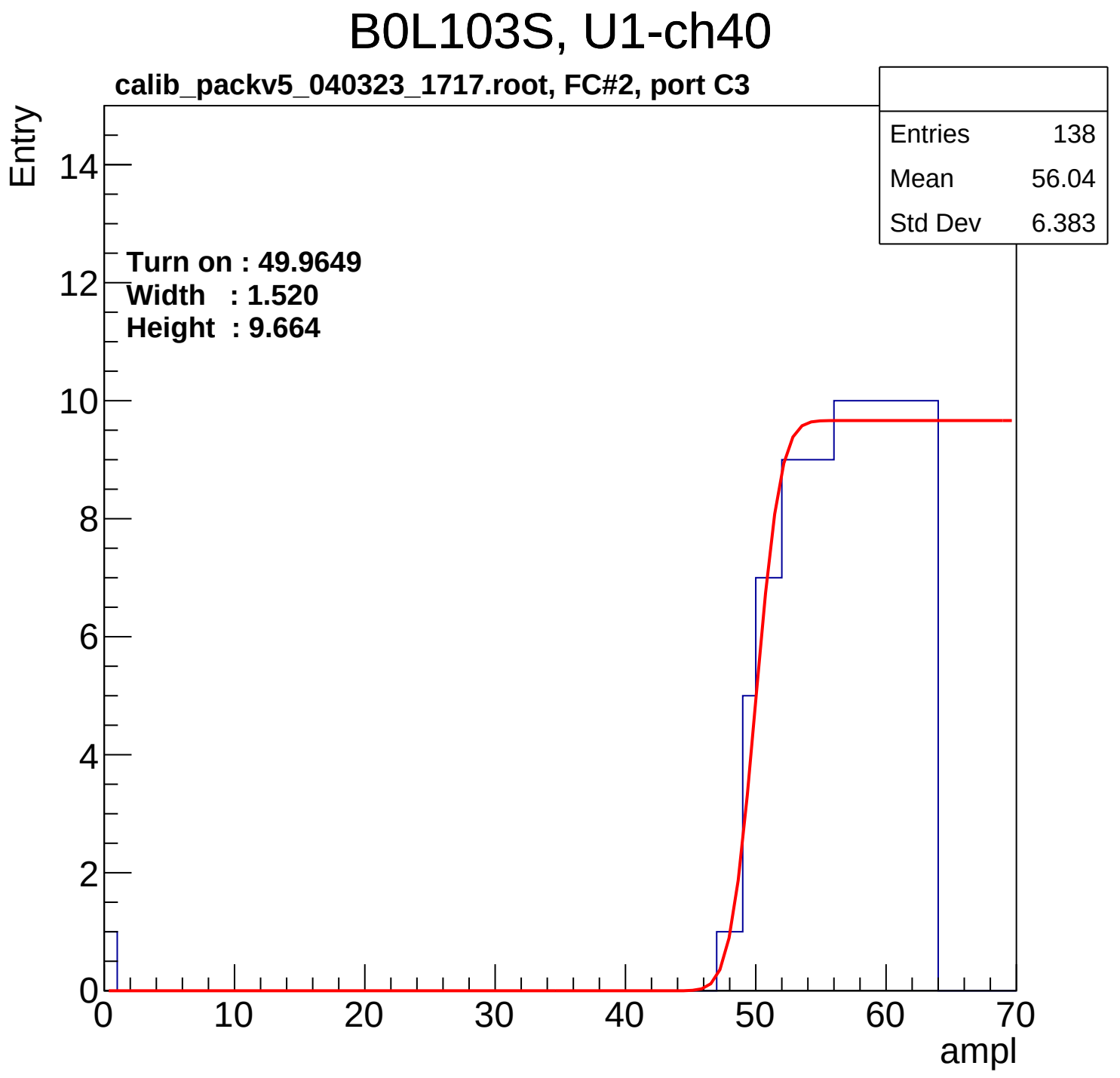
B0L103S, U1-ch40
calib_packv5_040323_1717.root, FC#2, port C3
Entries 138
Mean 56.04
Std Dev 6.383
Turn on : 49.9649
Width : 1.520
Height : 9.664
Entry
ampl
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6
8
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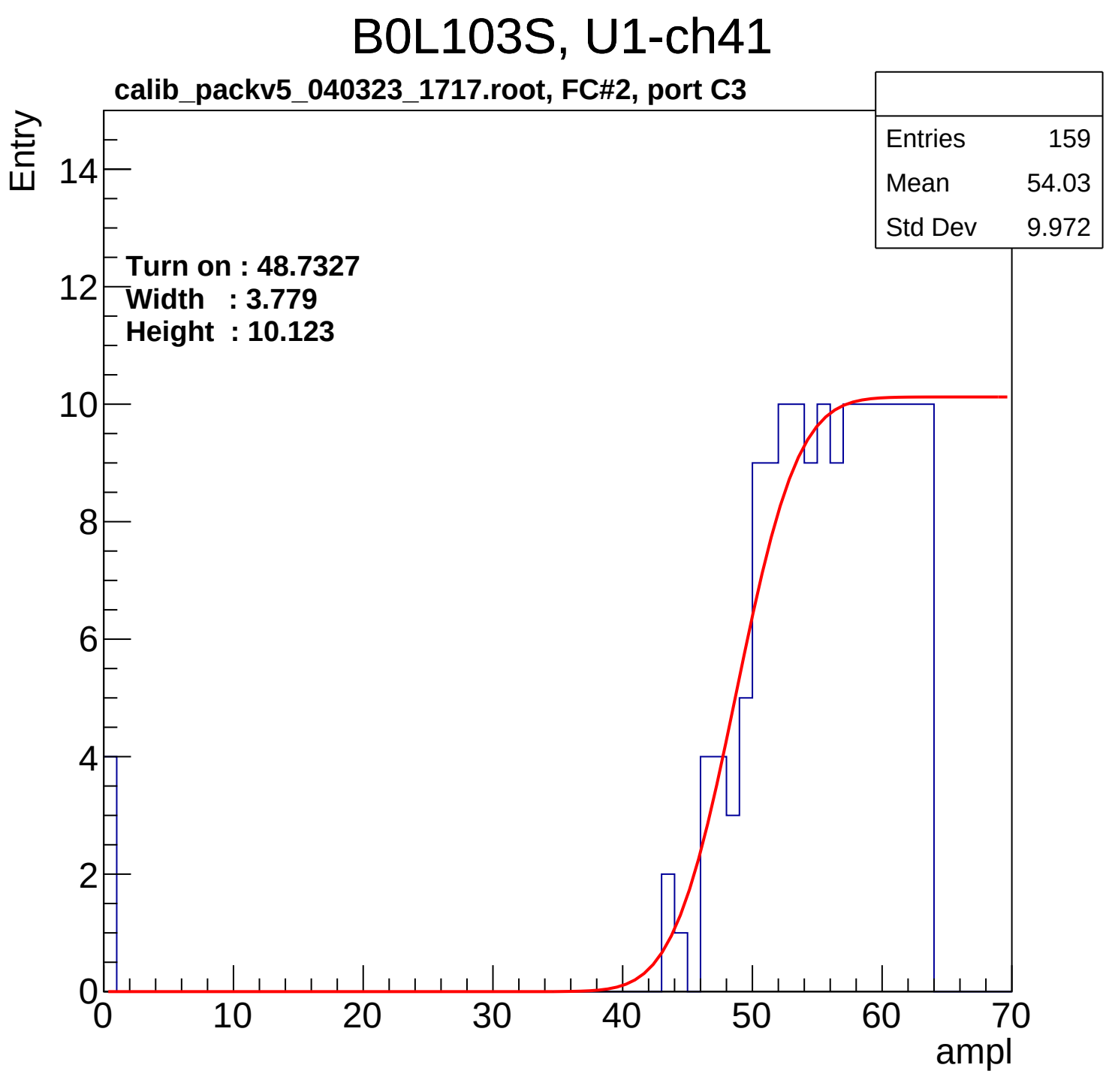
B0L103S, U1-ch41
calib_packv5_040323_1717.root, FC#2, port C3
Entries 159
Mean 54.03
Std Dev 9.972
Turn on : 48.7327
Width : 3.779
Height : 10.123
Entry
ampl
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6
8
10
12
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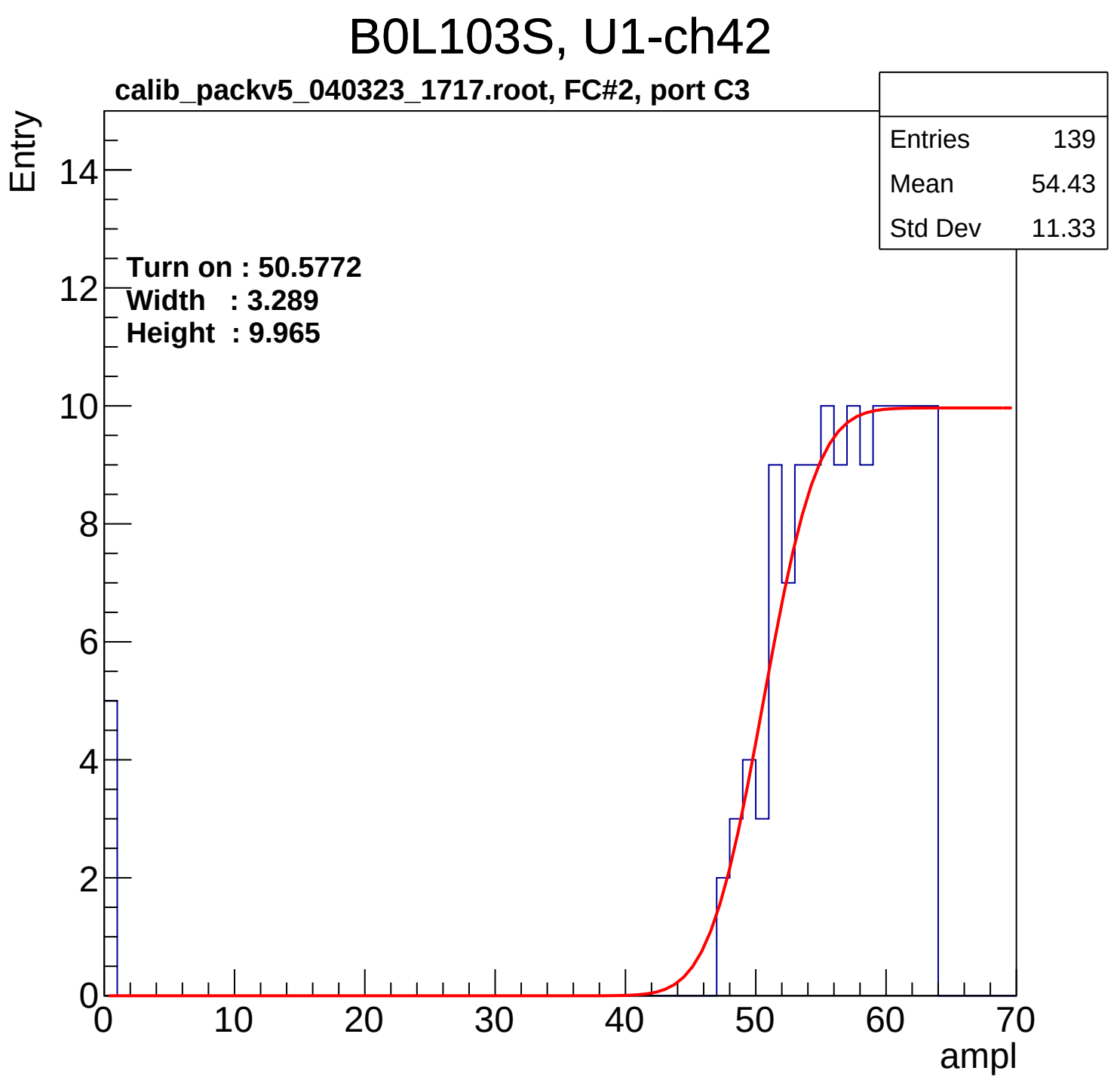
B0L103S, U1-ch42
calib_packv5_040323_1717.root, FC#2, port C3
Entries 139
Mean 54.43
Std Dev 11.33
Turn on : 50.5772
Width : 3.289
Height : 9.965
Entry
ampl
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6
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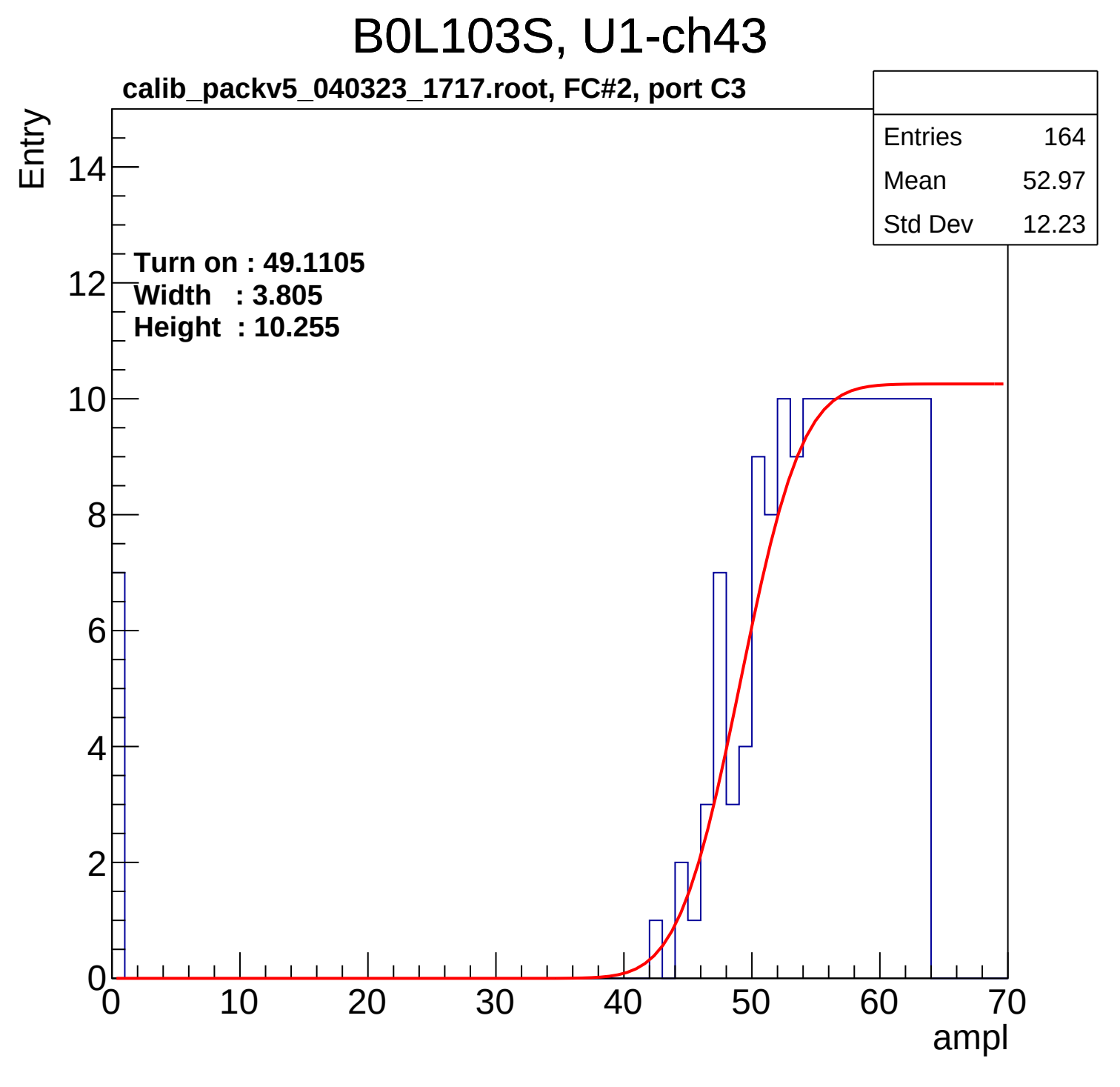
B0L103S, U1-ch43
calib_packv5_040323_1717.root, FC#2, port C3
Entries 164
Mean 52.97
Std Dev 12.23
Turn on : 49.1105
Width : 3.805
Height : 10.255
Entry
ampl
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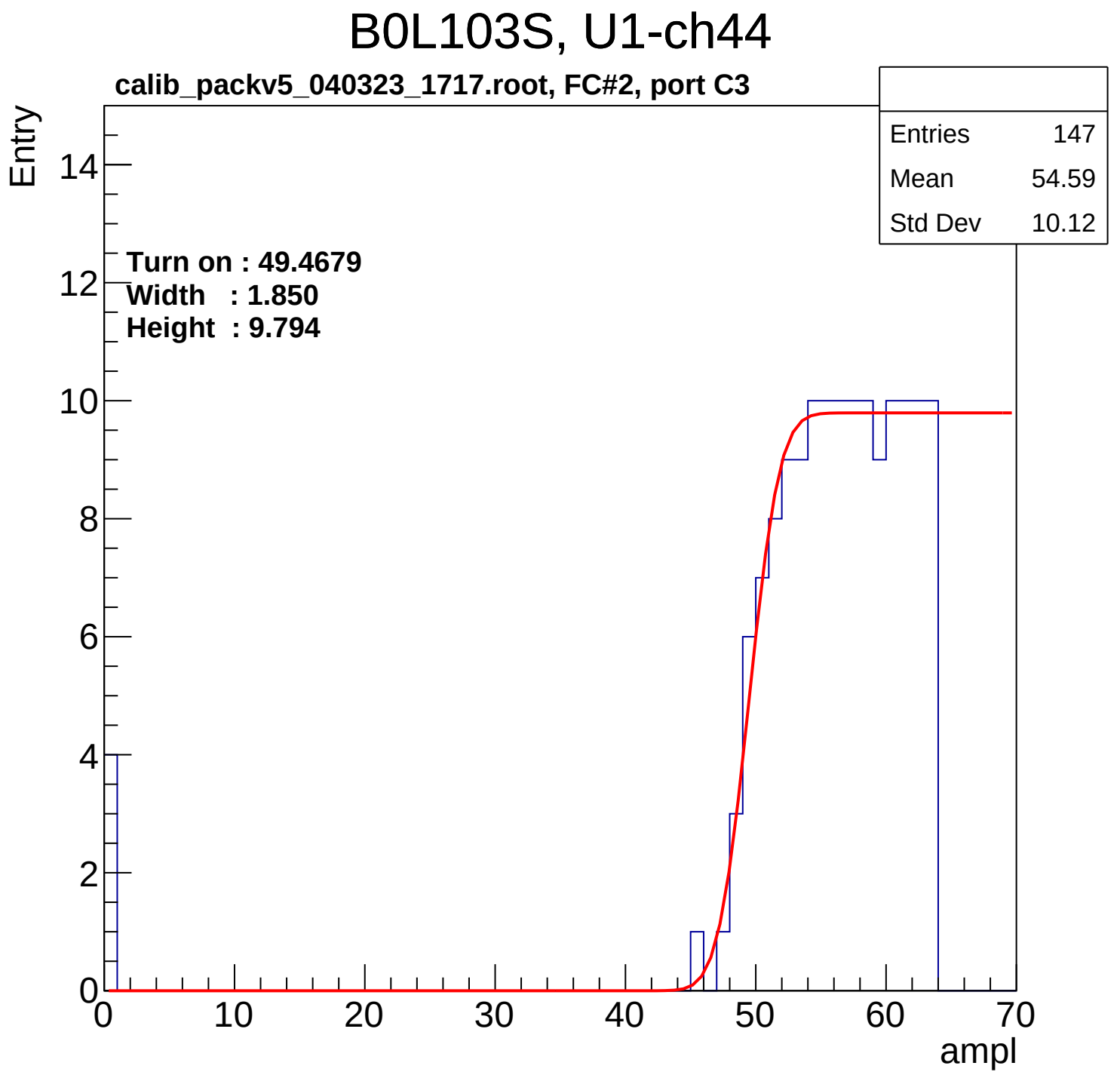
B0L103S, U1-ch44
calib_packv5_040323_1717.root, FC#2, port C3
Entries 147
Mean 54.59
Std Dev 10.12
Turn on : 49.4679
Width : 1.850
Height : 9.794
Entry
ampl
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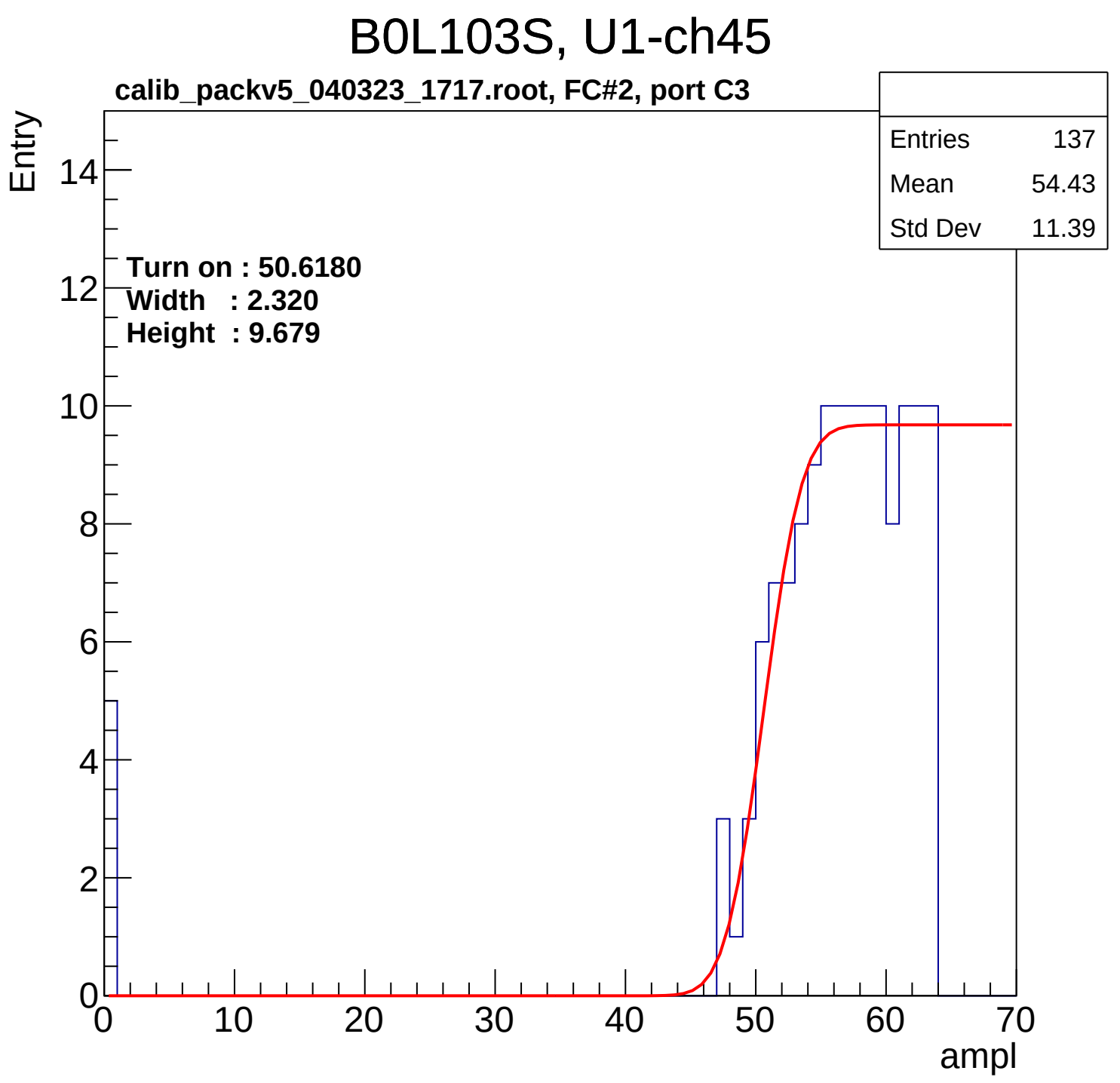
B0L103S, U1-ch45
calib_packv5_040323_1717.root, FC#2, port C3
Entries 137
Mean 54.43
Std Dev 11.39
Turn on : 50.6180
Width : 2.320
Height : 9.679
Entry
ampl
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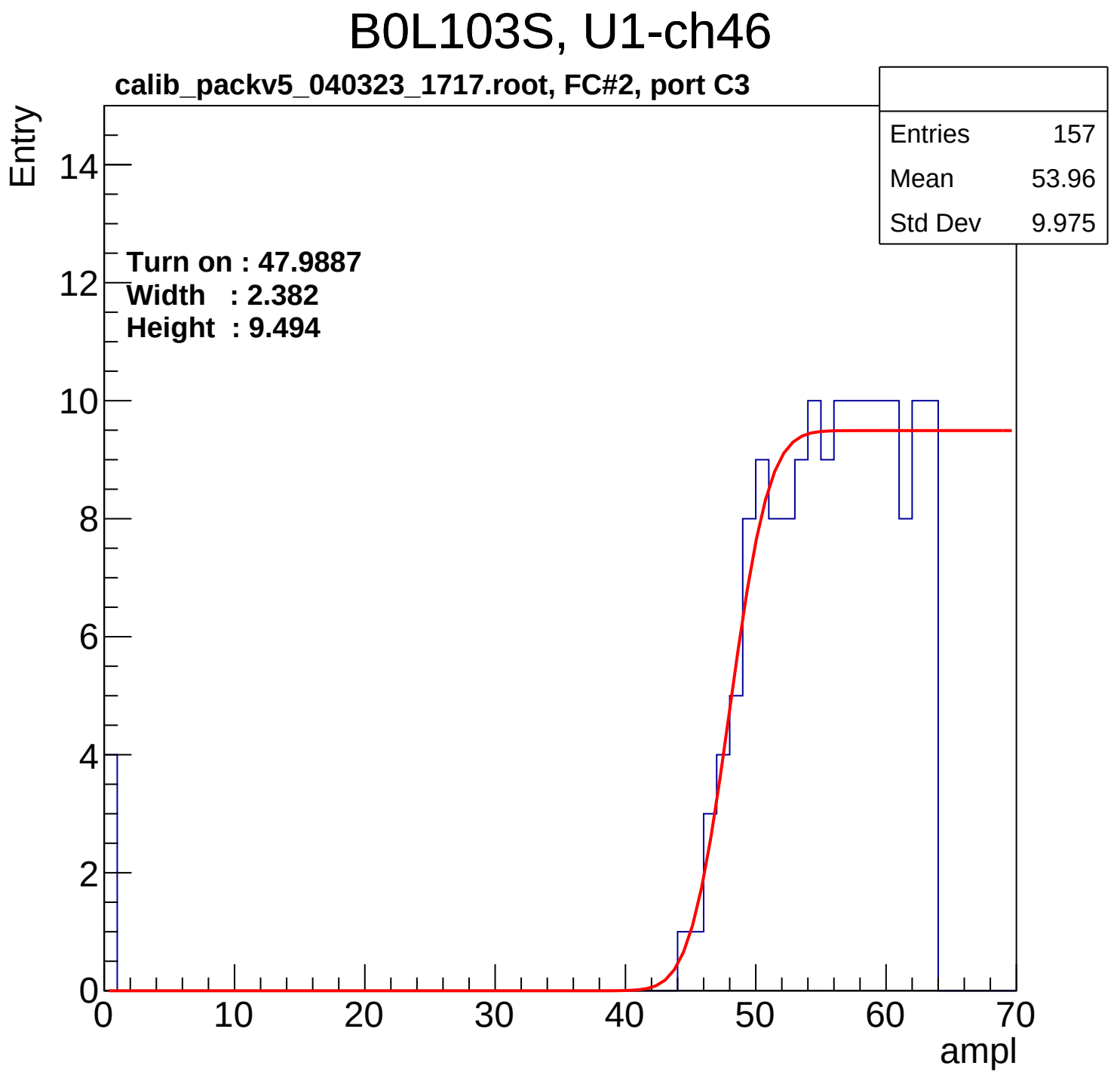
B0L103S, U1-ch46
calib_packv5_040323_1717.root, FC#2, port C3
Entries 157
Mean 53.96
Std Dev 9.975
Turn on : 47.9887
Width : 2.382
Height : 9.494
Entry
ampl
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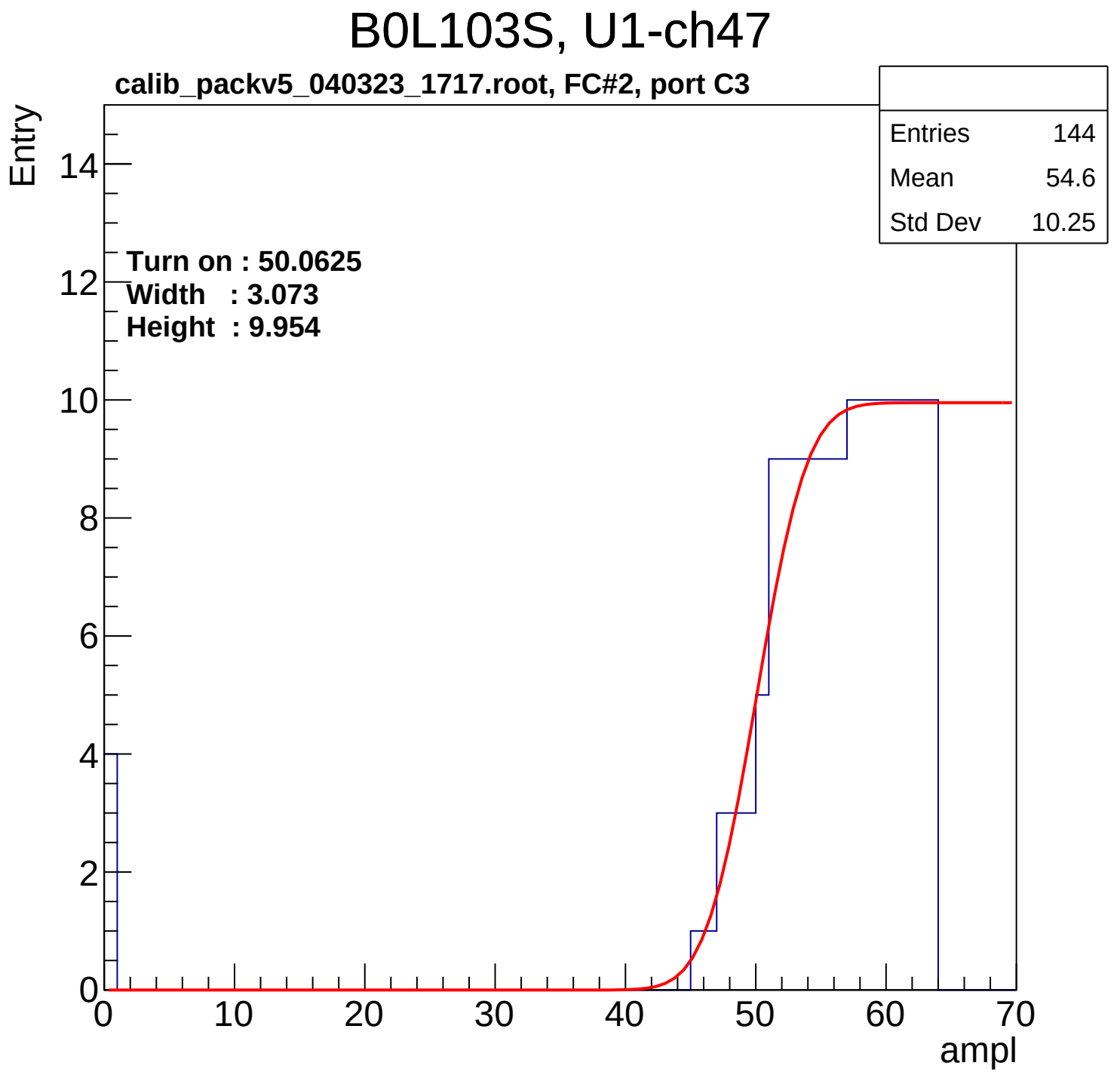
B0L103S, U1-ch47
calib_packv5_040323_1717.root, FC#2, port C3
Entries 144
Mean 54.6
Std Dev 10.25
Turn on : 50.0625
Width : 3.073
Height : 9.954
Entry
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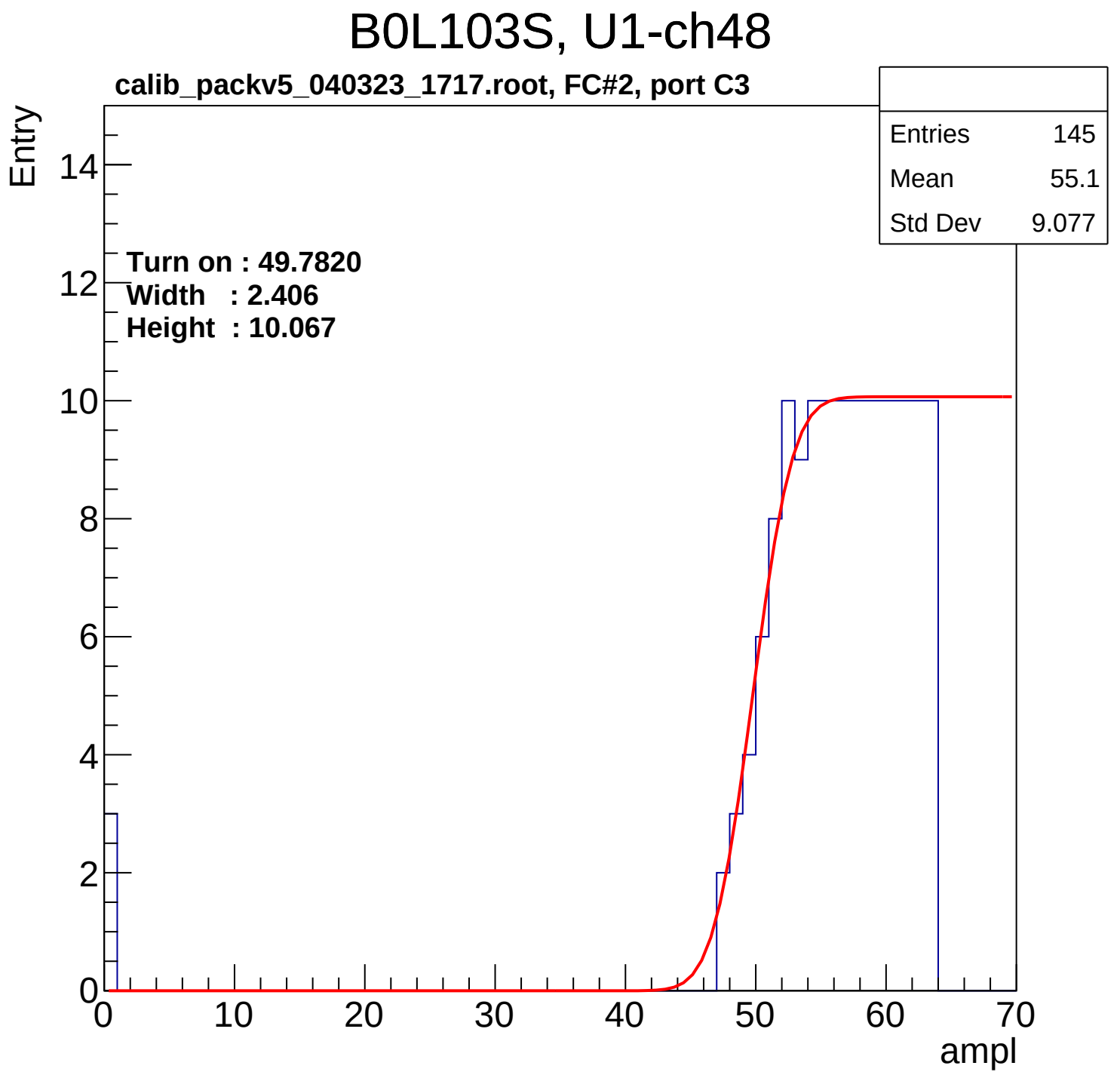
B0L103S, U1-ch48
calib_packv5_040323_1717.root, FC#2, port C3
Entries 145
Mean 55.1
Std Dev 9.077
Turn on : 49.7820
Width : 2.406
Height : 10.067
Entry
ampl
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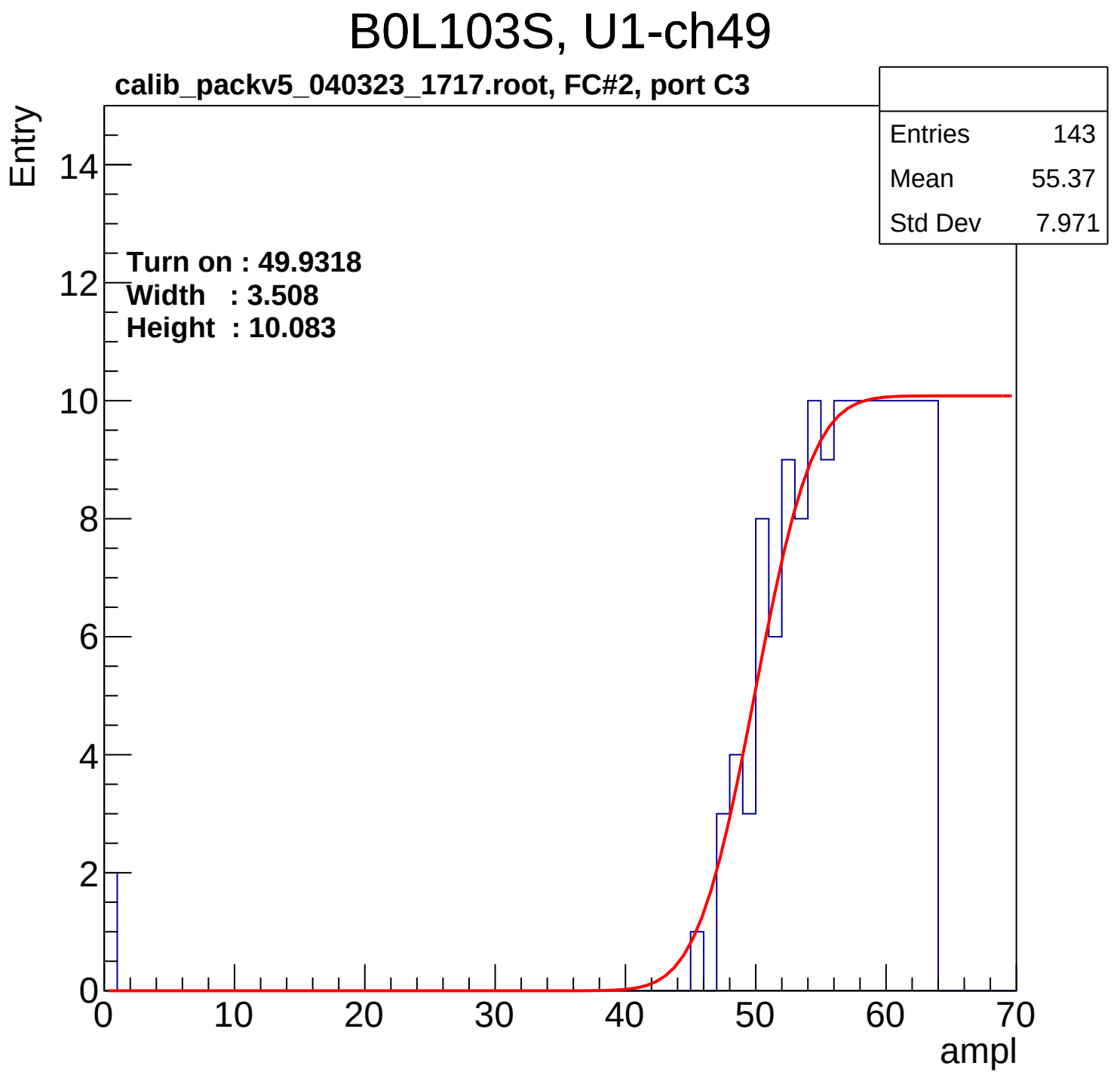
B0L103S, U1-ch49
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 55.37
Std Dev 7.971
Turn on : 49.9318
Width : 3.508
Height : 10.083
Entry
ampl
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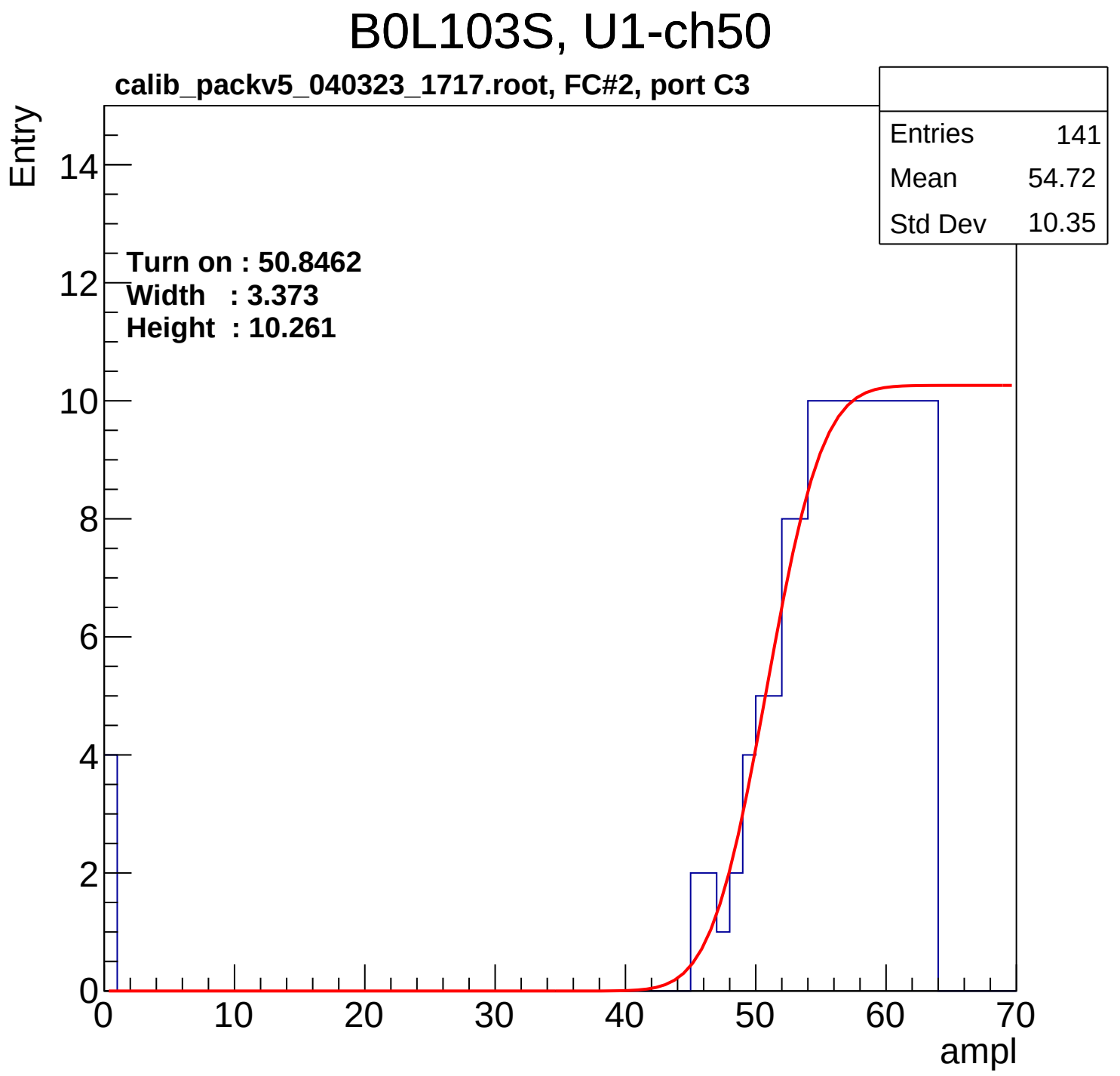
B0L103S, U1-ch50
calib_packv5_040323_1717.root, FC#2, port C3
Entries 141
Mean 54.72
Std Dev 10.35
Turn on : 50.8462
Width : 3.373
Height : 10.261
Entry
ampl
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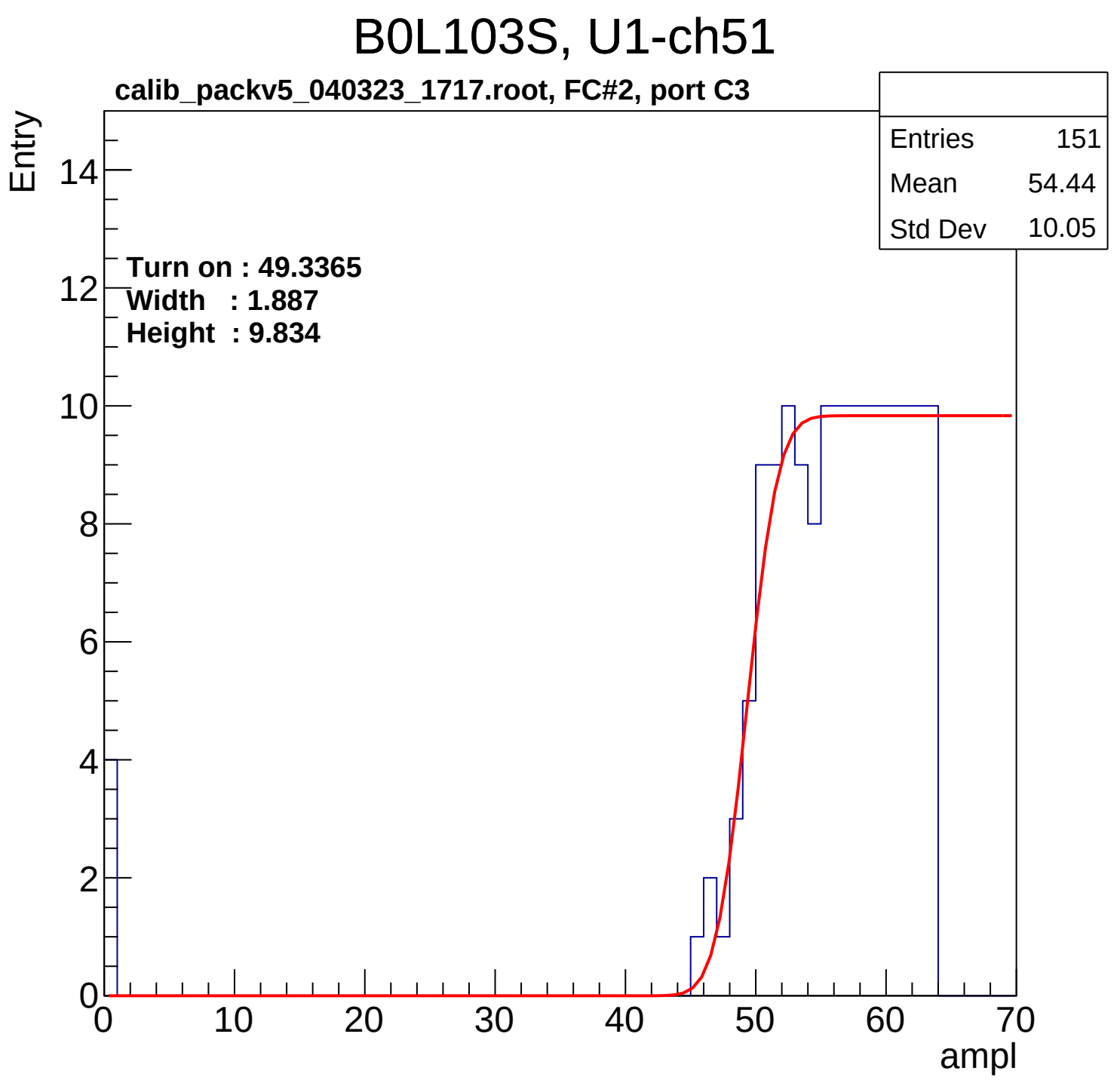
B0L103S, U1-ch51
calib_packv5_040323_1717.root, FC#2, port C3
Entries 151
Mean 54.44
Std Dev 10.05
Turn on : 49.3365
Width : 1.887
Height : 9.834
Entry
ampl
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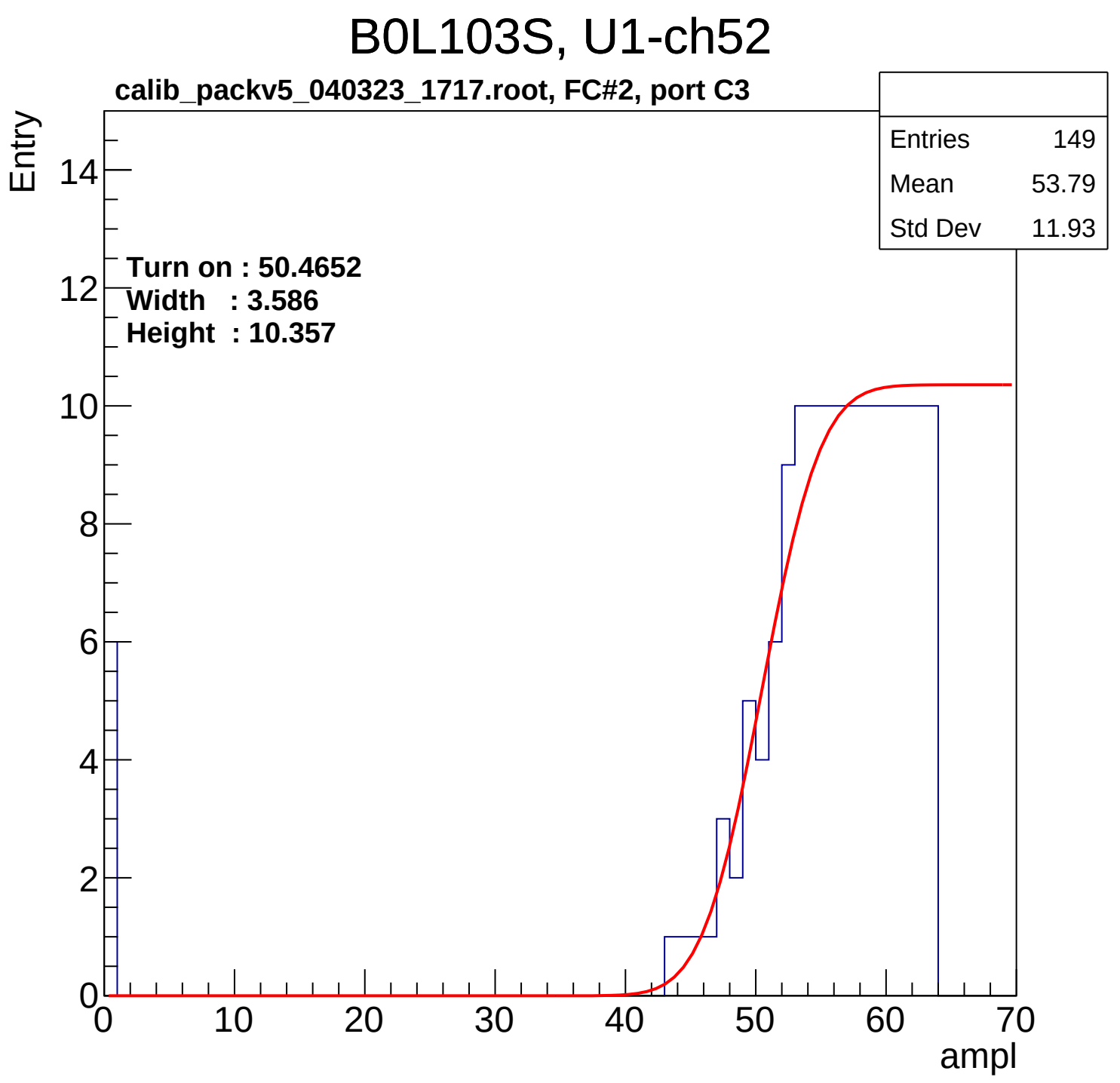
B0L103S, U1-ch52
calib_packv5_040323_1717.root, FC#2, port C3
Entries 149
Mean 53.79
Std Dev 11.93
Turn on : 50.4652
Width : 3.586
Height : 10.357
Entry
ampl
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6
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10
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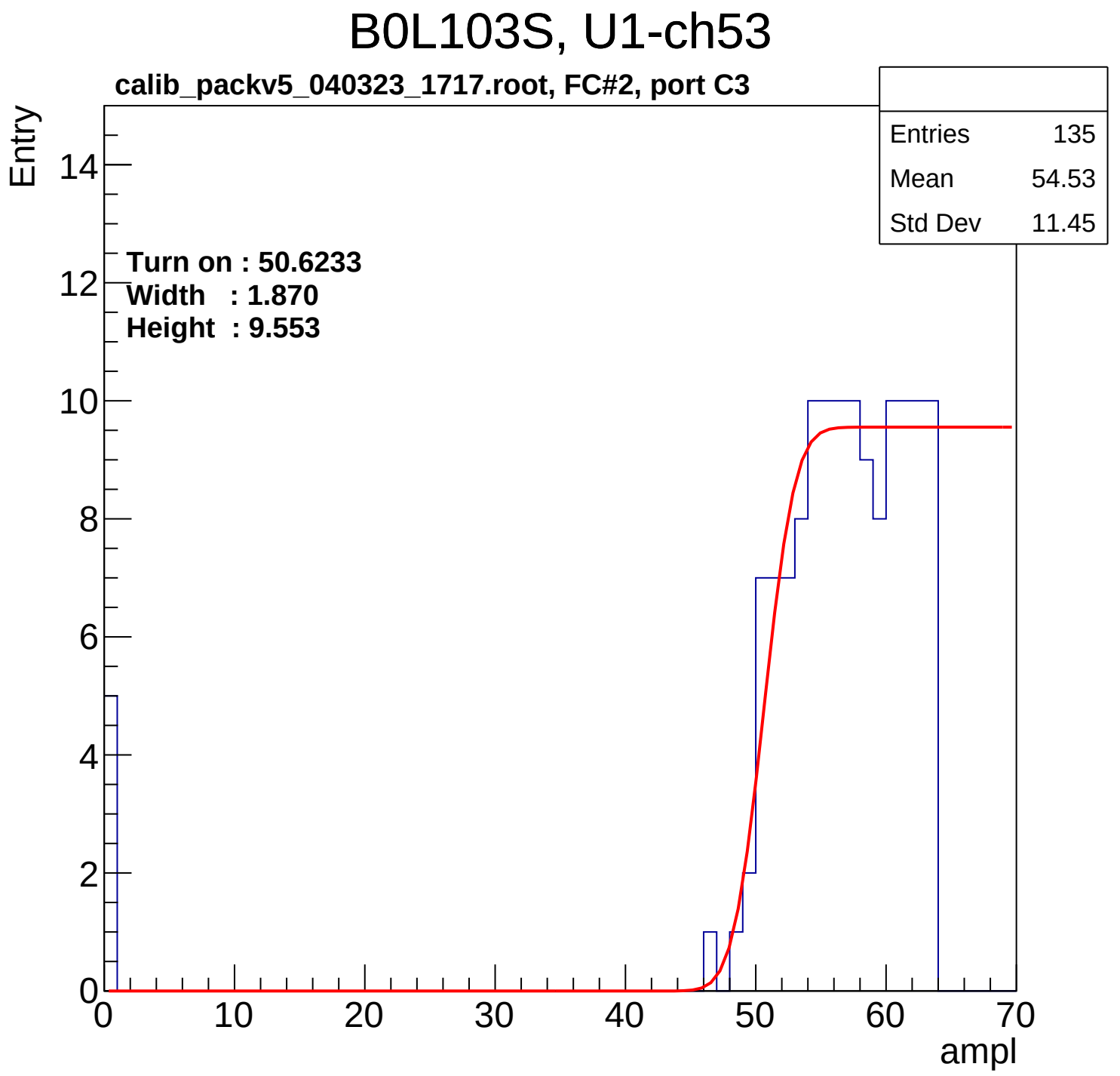
B0L103S, U1-ch53
calib_packv5_040323_1717.root, FC#2, port C3
Entries 135
Mean 54.53
Std Dev 11.45
Turn on : 50.6233
Width : 1.870
Height : 9.553
Entry
ampl
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6
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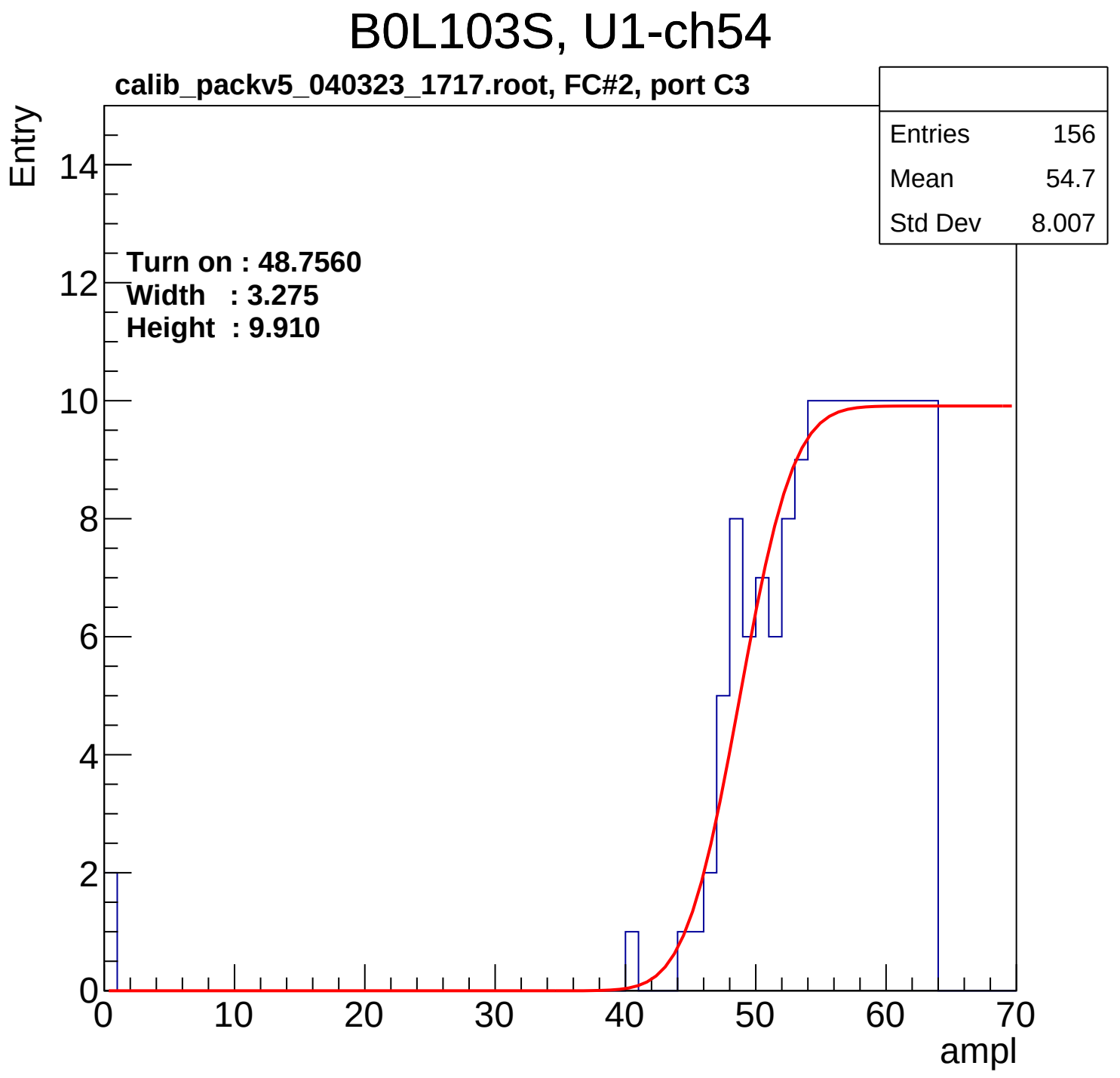
B0L103S, U1-ch54
calib_packv5_040323_1717.root, FC#2, port C3
Entries 156
Mean 54.7
Std Dev 8.007
Turn on : 48.7560
Width : 3.275
Height : 9.910
Entry
ampl
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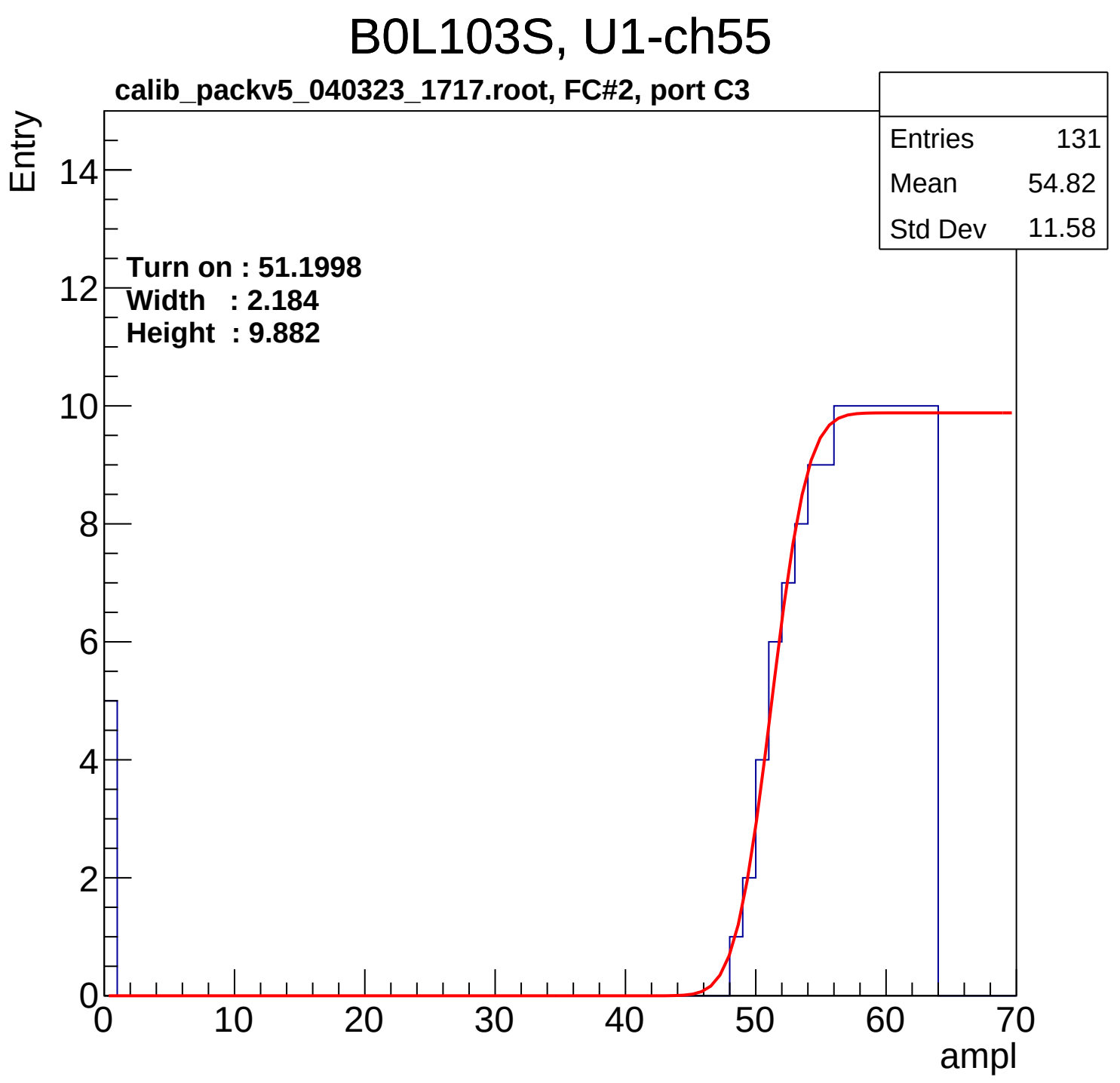
B0L103S, U1-ch55
calib_packv5_040323_1717.root, FC#2, port C3
Entries 131
Mean 54.82
Std Dev 11.58
Turn on : 51.1998
Width : 2.184
Height : 9.882
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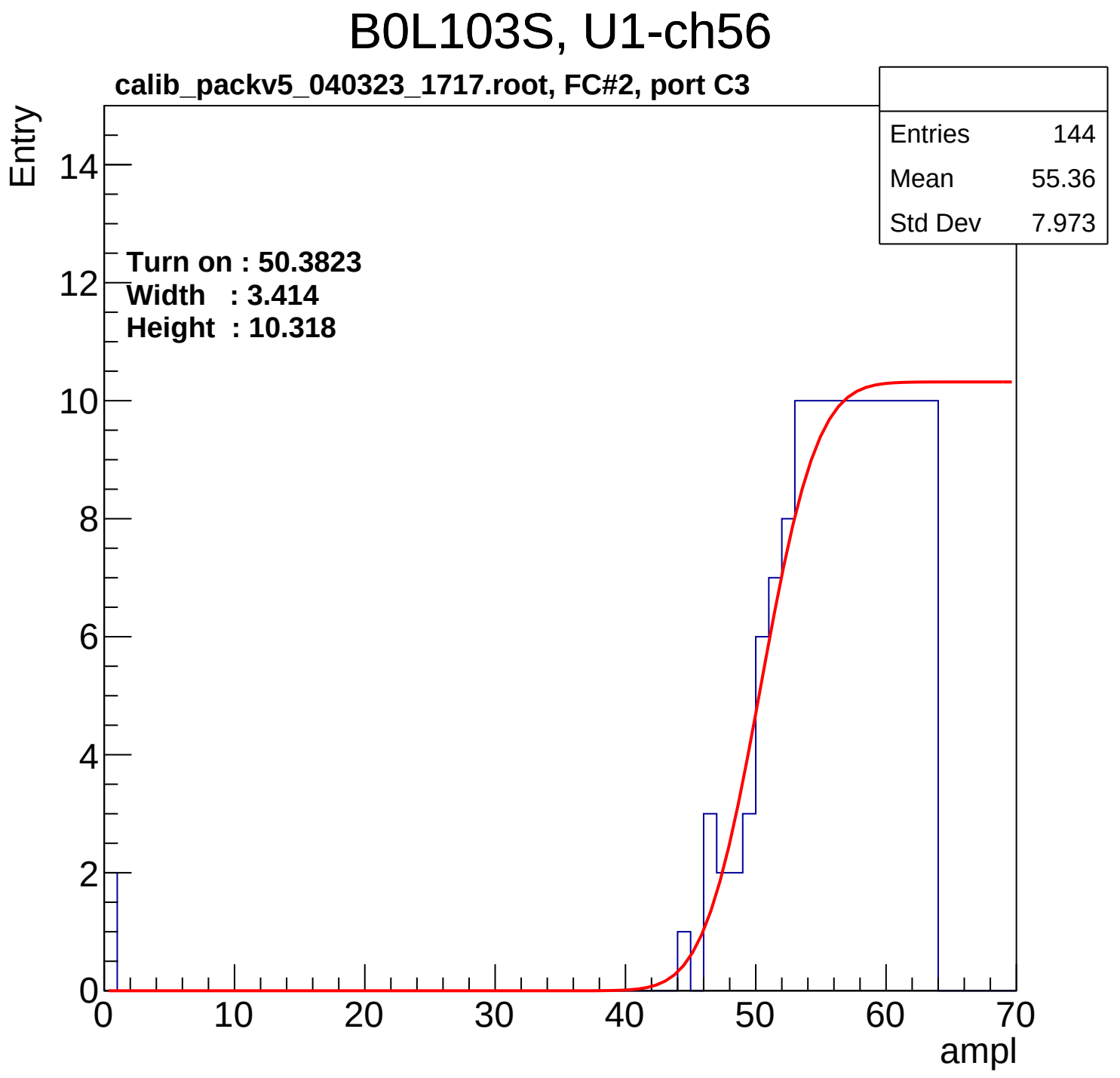
B0L103S, U1-ch56
calib_packv5_040323_1717.root, FC#2, port C3
Entries 144
Mean 55.36
Std Dev 7.973
Turn on : 50.3823
Width : 3.414
Height : 10.318
Entry
ampl
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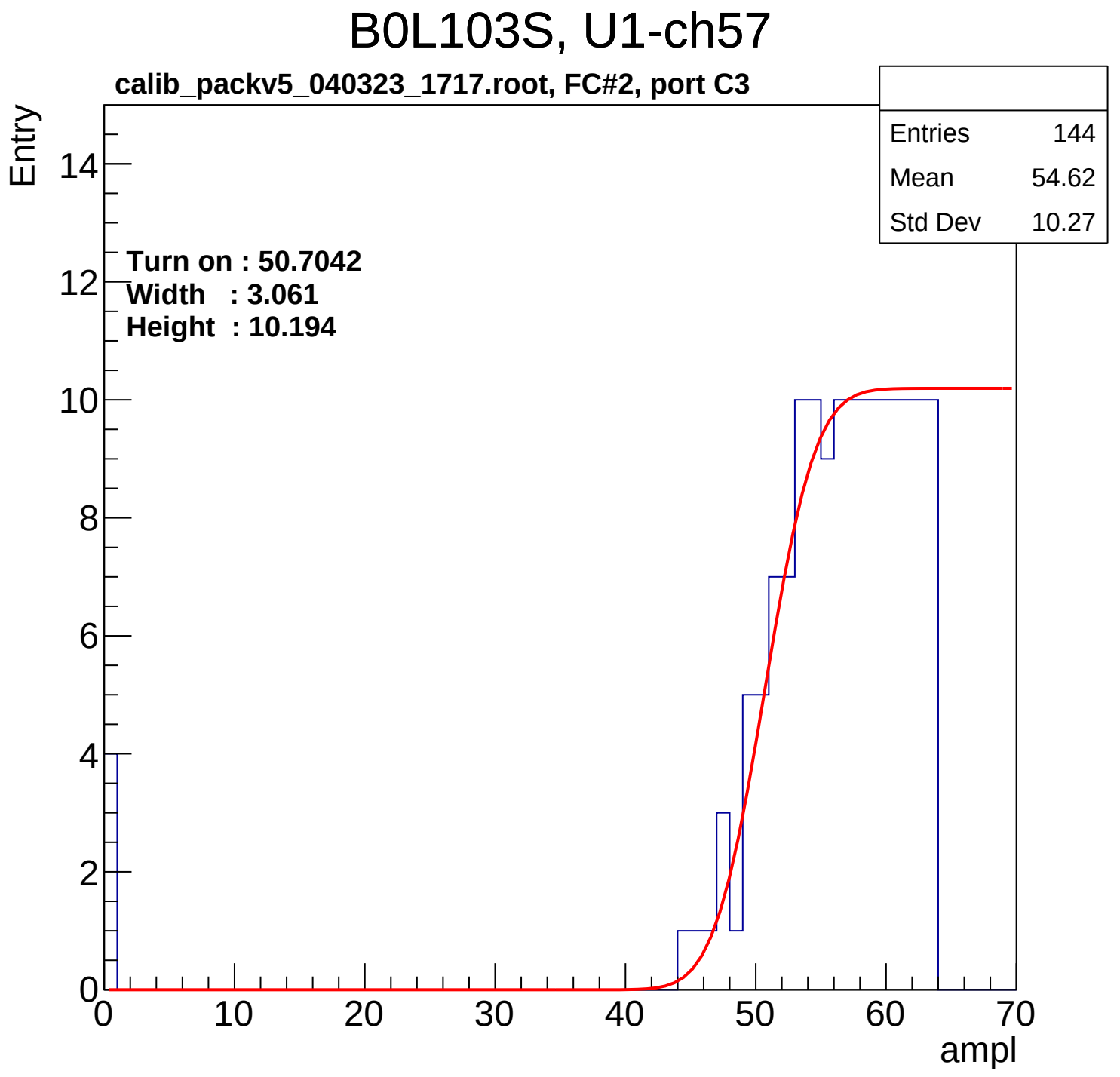
B0L103S, U1-ch57
calib_packv5_040323_1717.root, FC#2, port C3
Entries 144
Mean 54.62
Std Dev 10.27
Turn on : 50.7042
Width : 3.061
Height : 10.194
Entry
ampl
0
2
4
6
8
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12
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20
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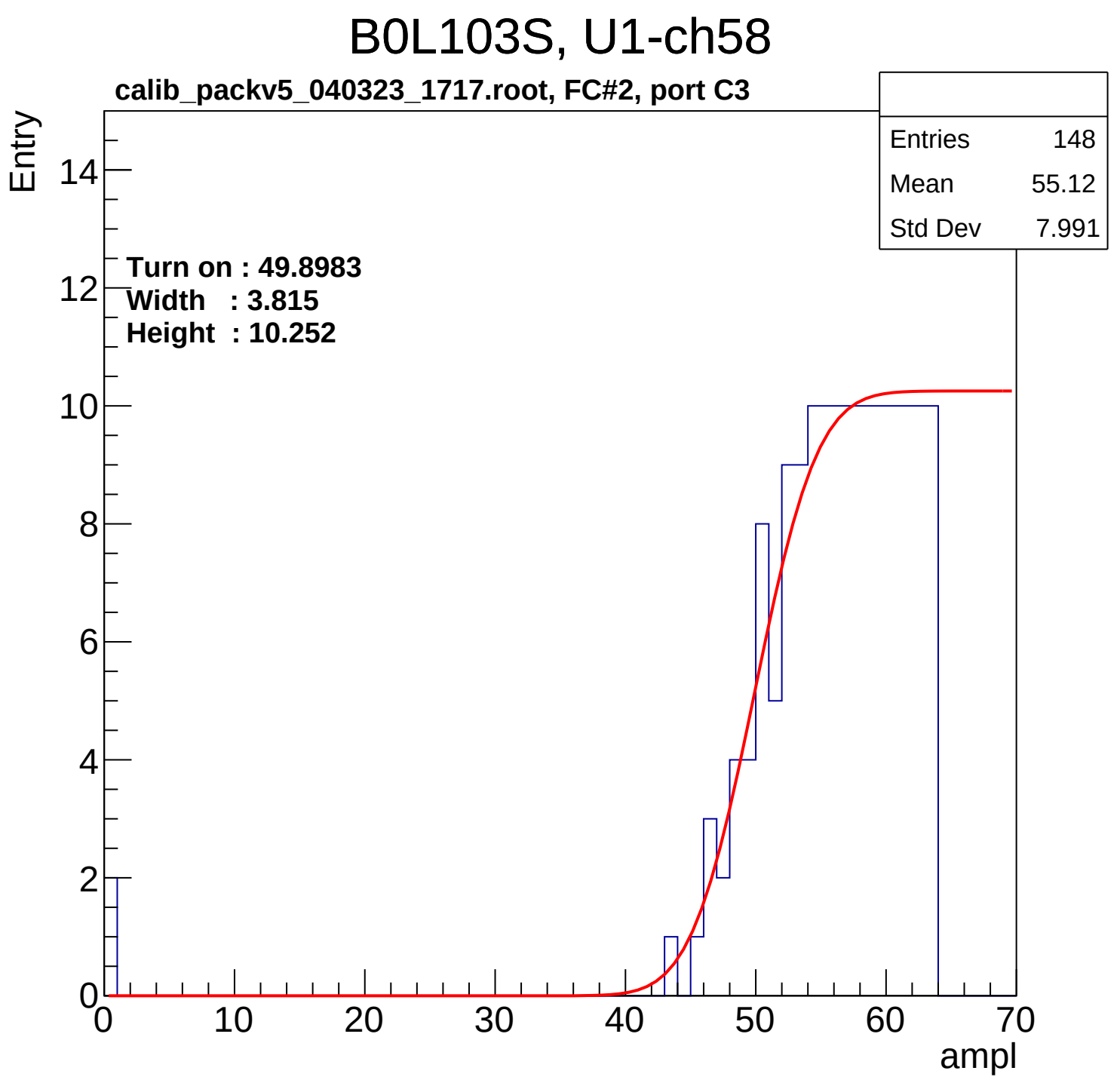
B0L103S, U1-ch58
calib_packv5_040323_1717.root, FC#2, port C3
Entries 148
Mean 55.12
Std Dev 7.991
Turn on : 49.8983
Width : 3.815
Height : 10.252
Entry
ampl
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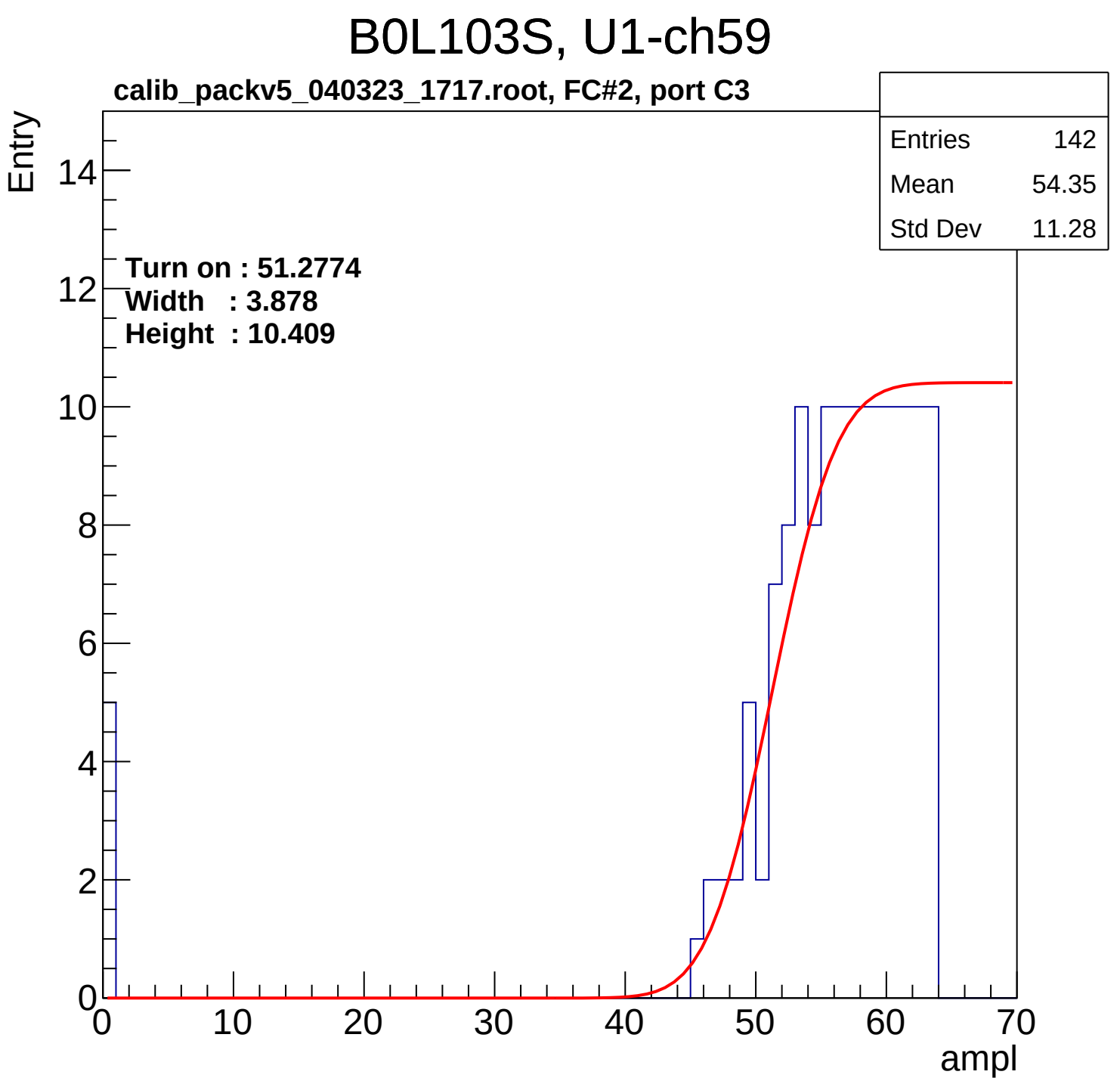
B0L103S, U1-ch59
calib_packv5_040323_1717.root, FC#2, port C3
Entries 142
Mean 54.35
Std Dev 11.28
Turn on : 51.2774
Width : 3.878
Height : 10.409
Entry
ampl
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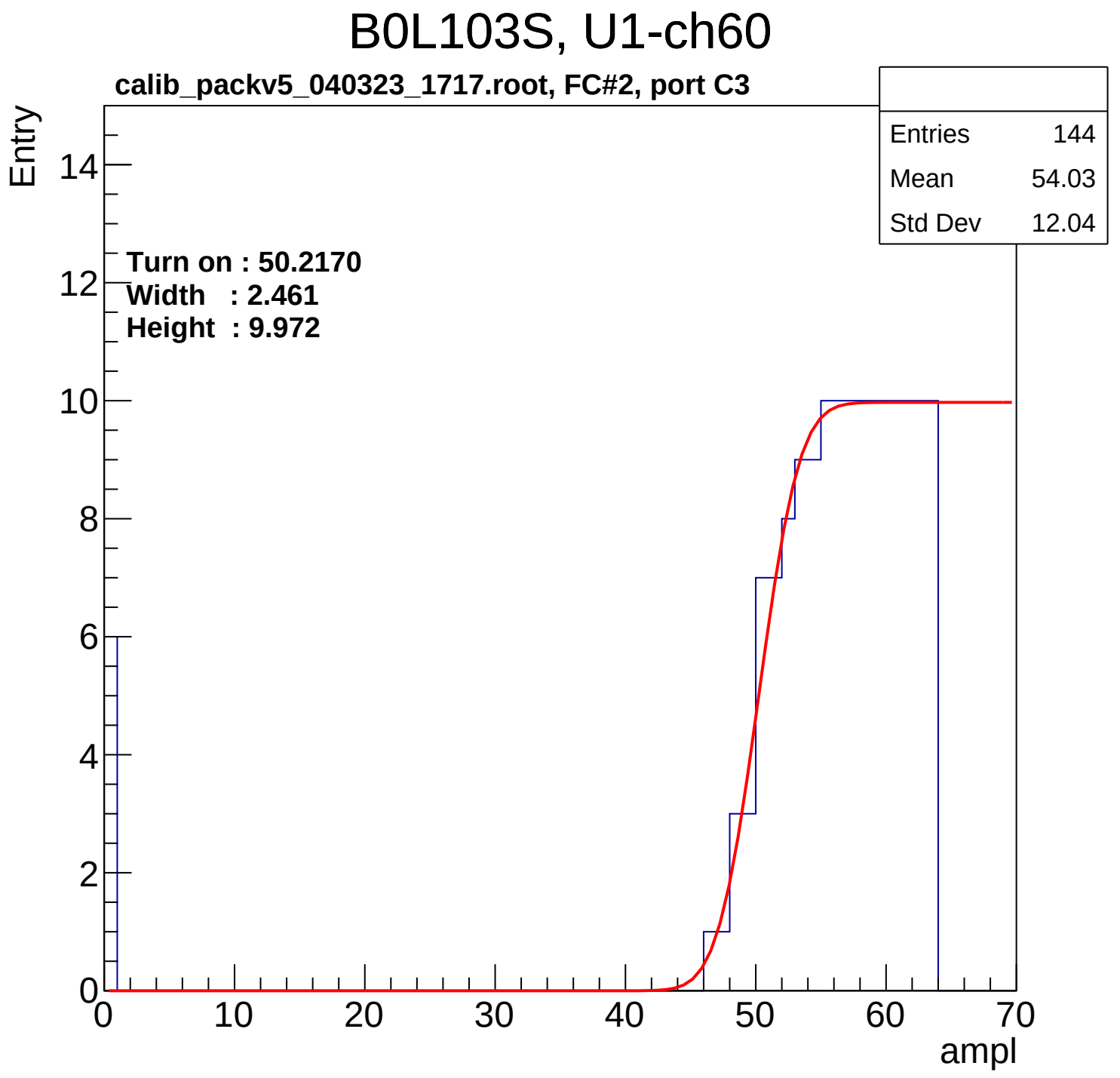
B0L103S, U1-ch60
calib_packv5_040323_1717.root, FC#2, port C3
Entries 144
Mean 54.03
Std Dev 12.04
Turn on : 50.2170
Width : 2.461
Height : 9.972
Entry
ampl
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6
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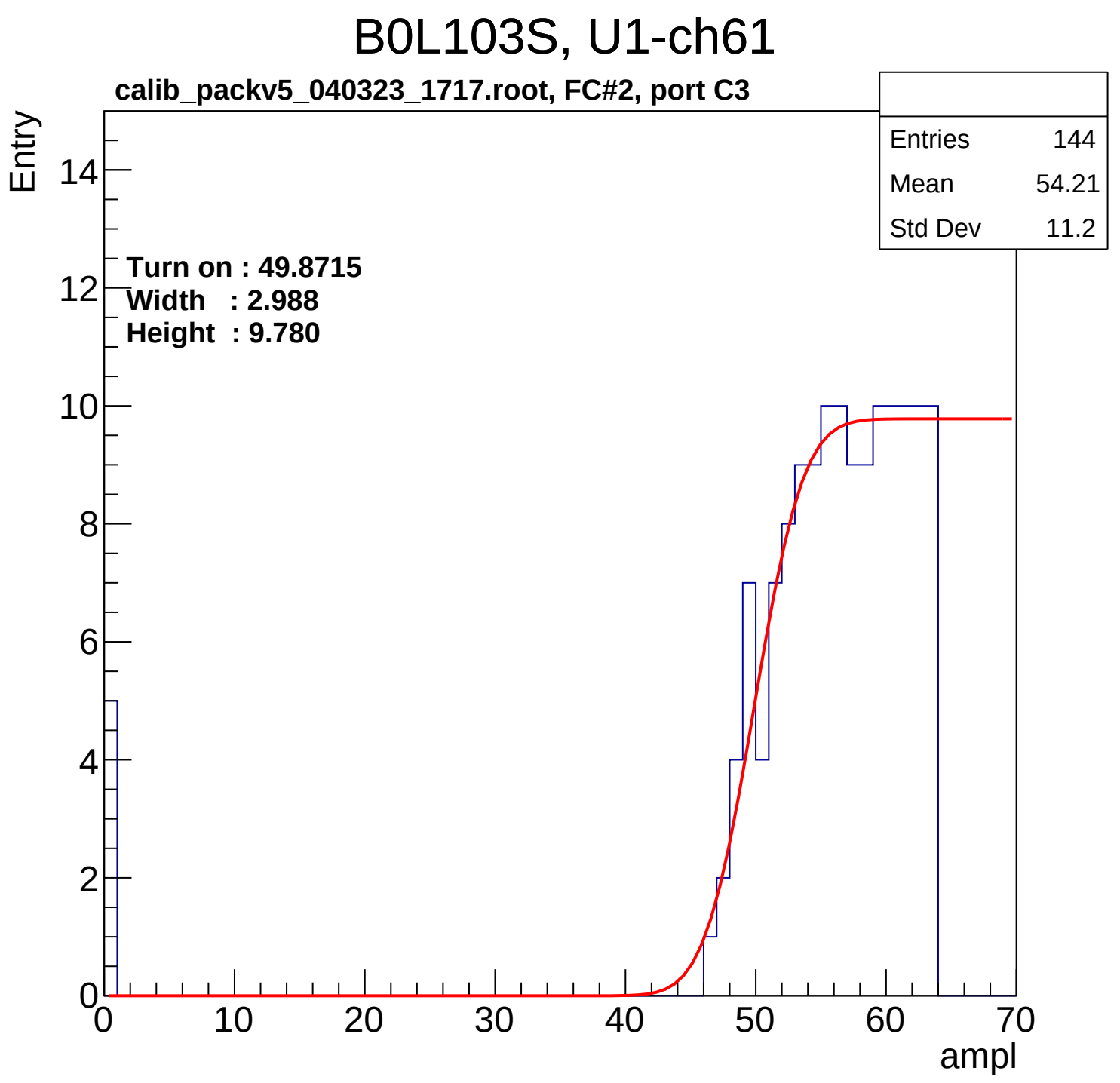
B0L103S, U1-ch61
calib_packv5_040323_1717.root, FC#2, port C3
Entries 144
Mean 54.21
Std Dev 11.2
Turn on : 49.8715
Width : 2.988
Height : 9.780
Entry
ampl
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2
4
6
8
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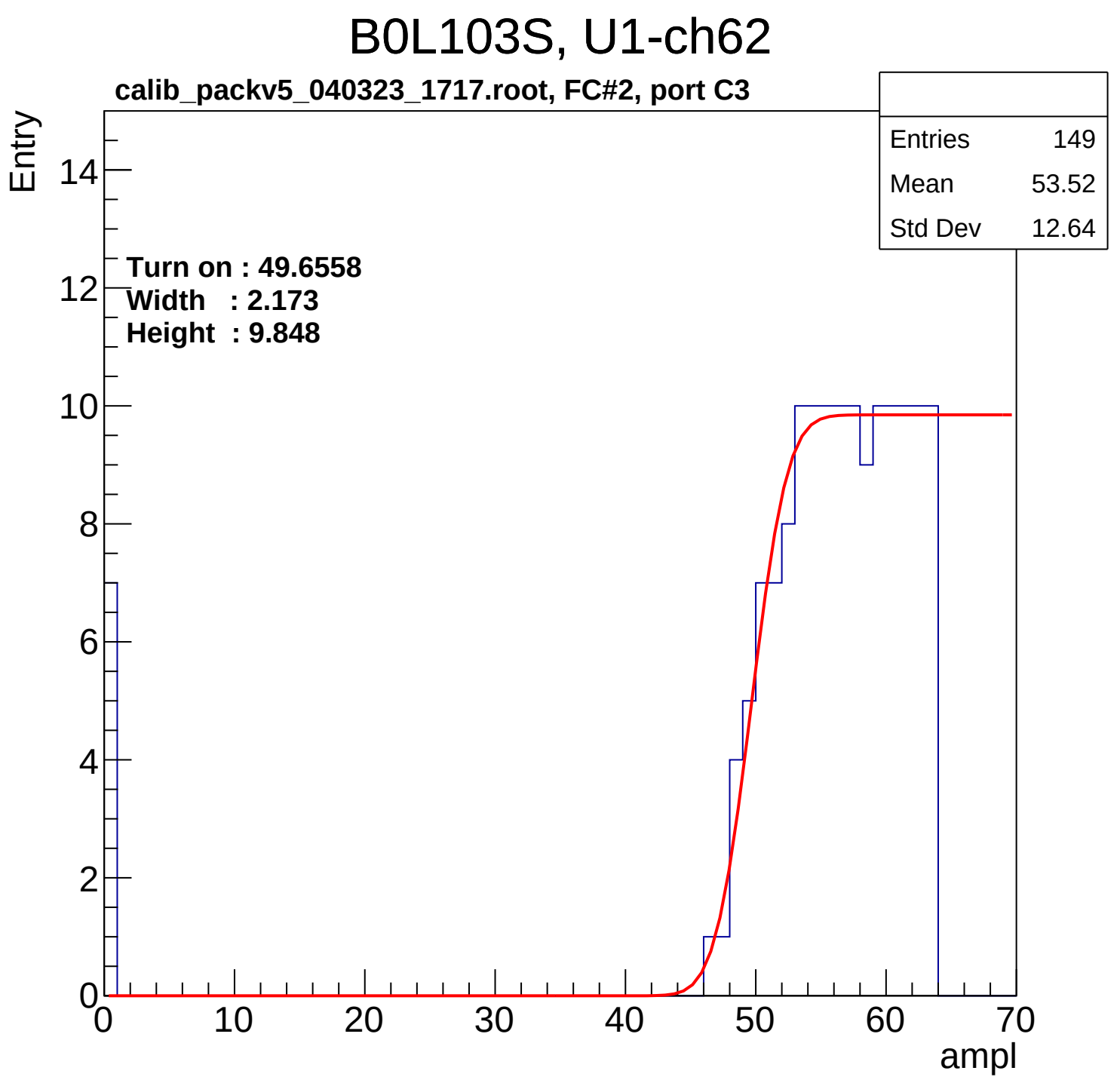
B0L103S, U1-ch62
calib_packv5_040323_1717.root, FC#2, port C3
Entries 149
Mean 53.52
Std Dev 12.64
Turn on : 49.6558
Width : 2.173
Height : 9.848
Entry
ampl
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2
4
6
8
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12
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0
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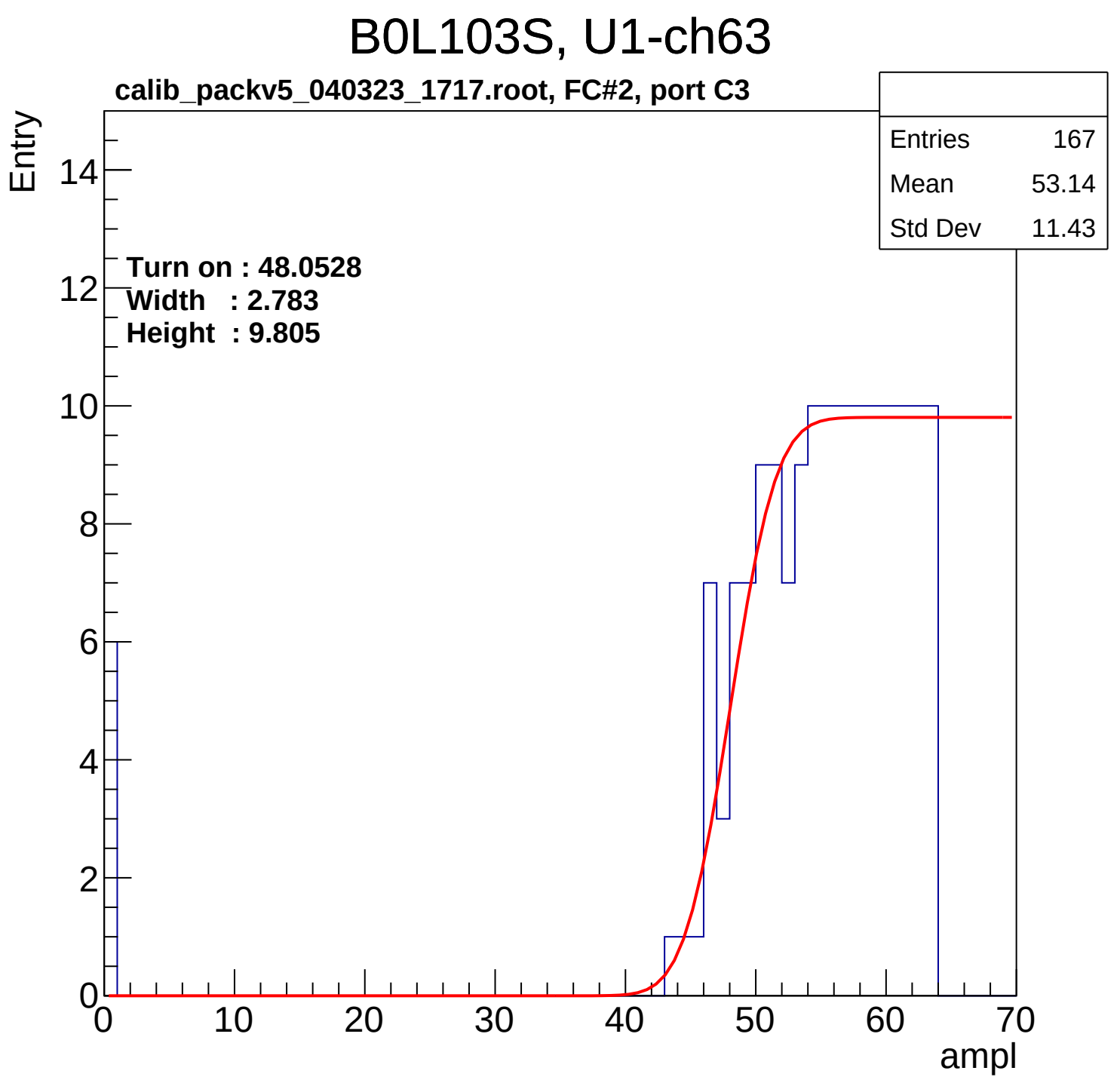
B0L103S, U1-ch63
calib_packv5_040323_1717.root, FC#2, port C3
Entries 167
Mean 53.14
Std Dev 11.43
Turn on : 48.0528
Width : 2.783
Height : 9.805
Entry
ampl
0
2
4
6
8
10
12
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0
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20
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40
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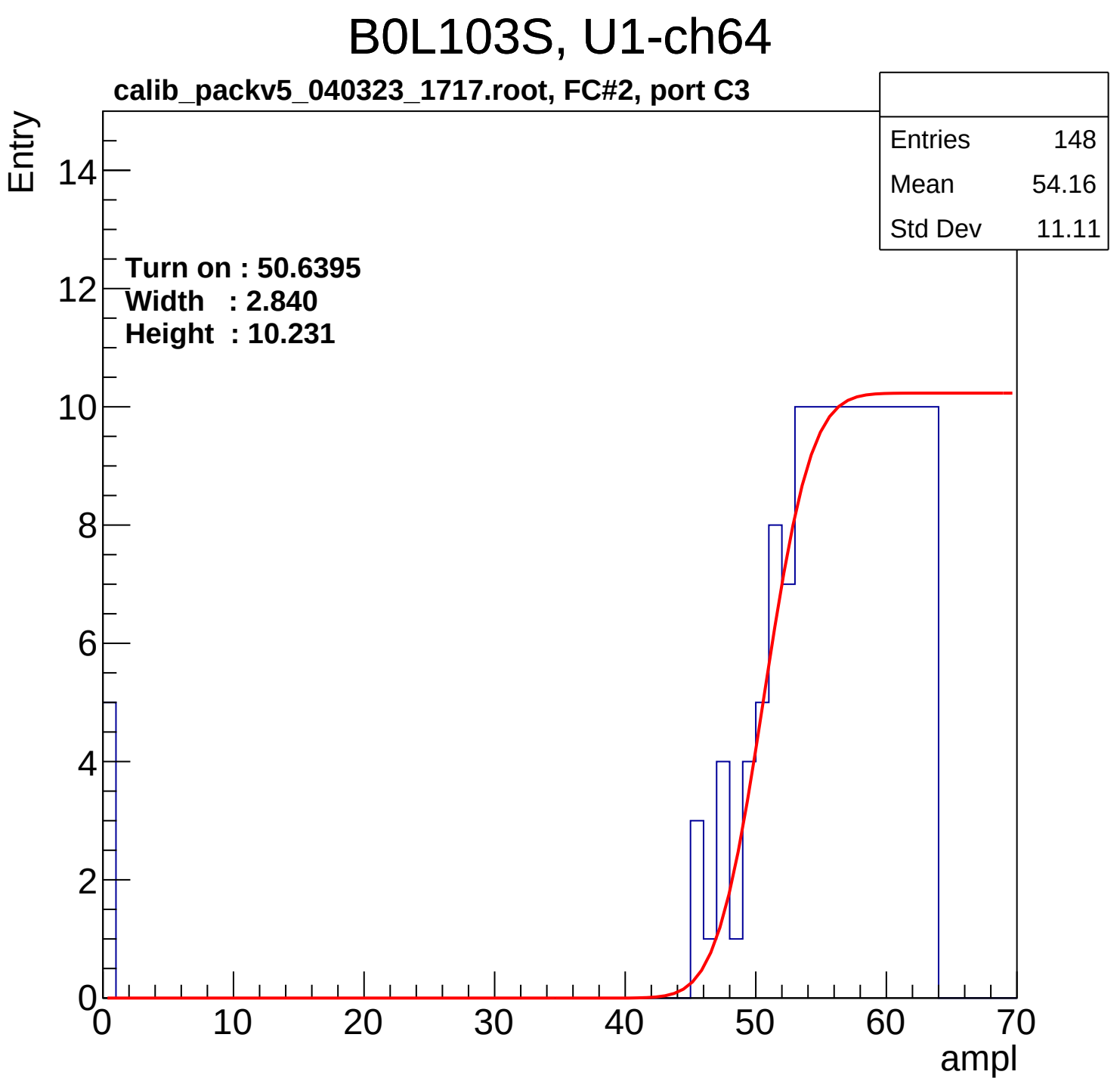
B0L103S, U1-ch64
calib_packv5_040323_1717.root, FC#2, port C3
Entries 148
Mean 54.16
Std Dev 11.11
Turn on : 50.6395
Width : 2.840
Height : 10.231
Entry
ampl
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2
4
6
8
10
12
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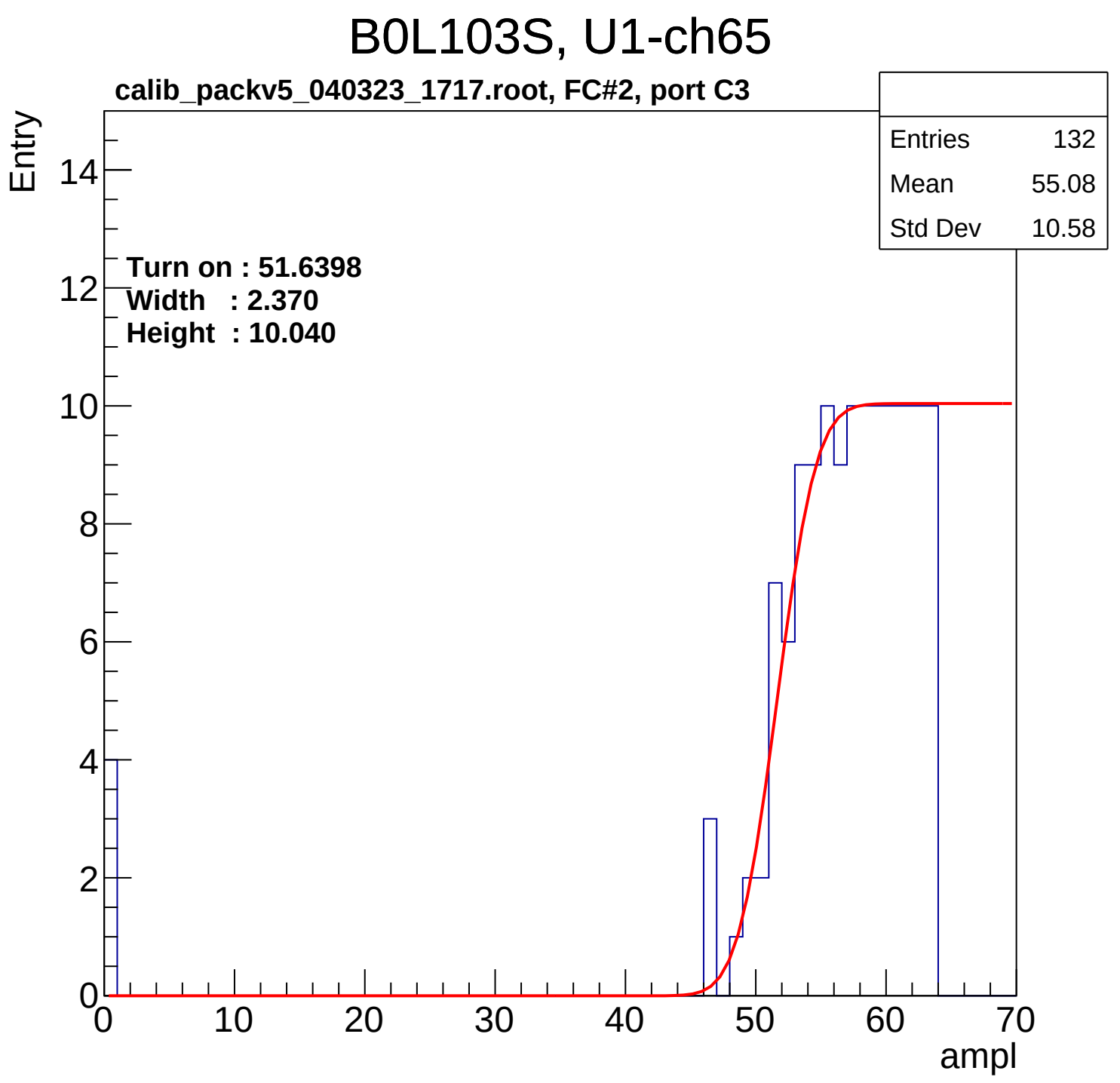
B0L103S, U1-ch65
calib_packv5_040323_1717.root, FC#2, port C3
Entries 132
Mean 55.08
Std Dev 10.58
Turn on : 51.6398
Width : 2.370
Height : 10.040
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
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60
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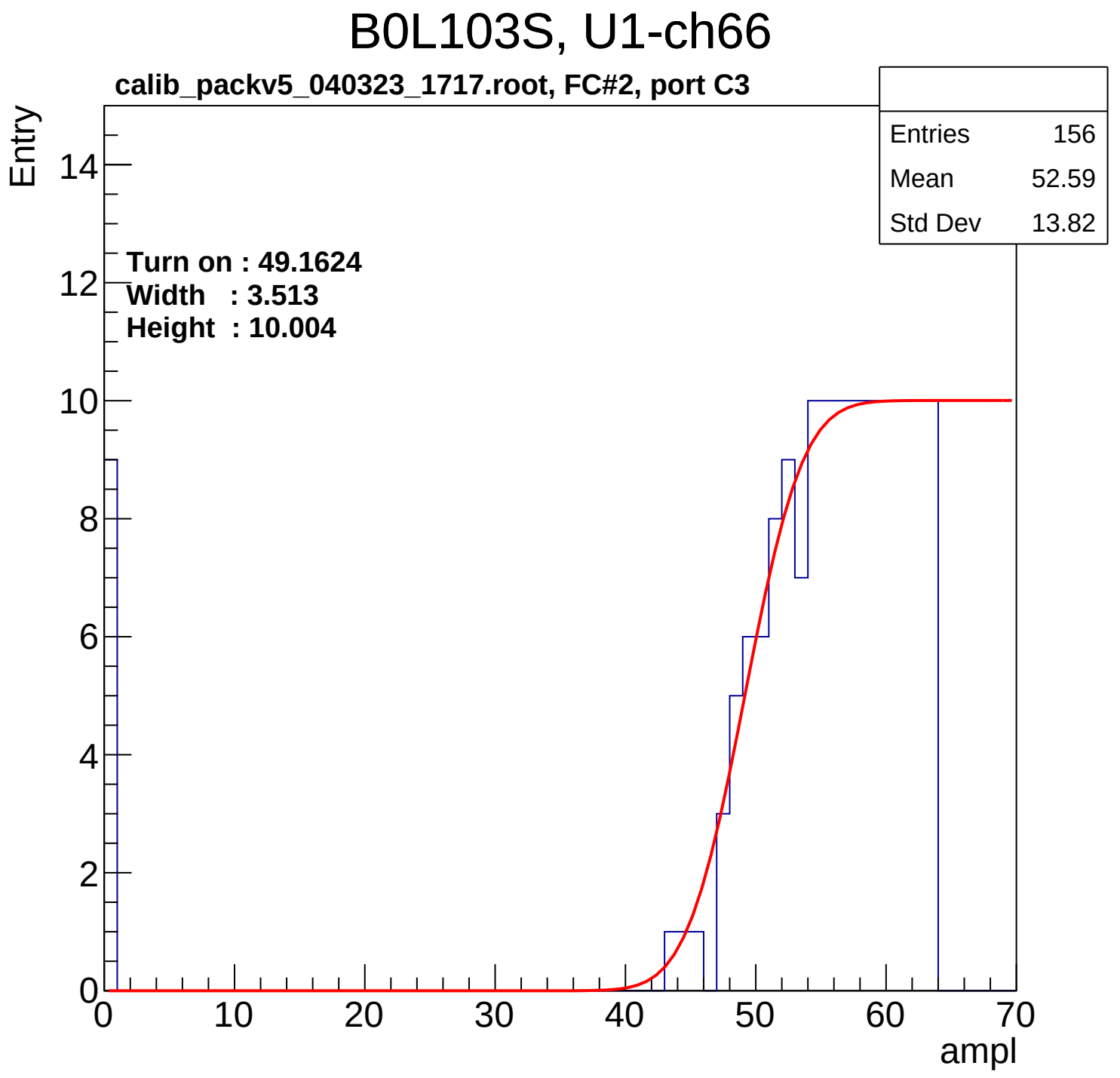
B0L103S, U1-ch66
calib_packv5_040323_1717.root, FC#2, port C3
Entries 156
Mean 52.59
Std Dev 13.82
Turn on : 49.1624
Width : 3.513
Height : 10.004
Entry
ampl
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2
4
6
8
10
12
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0
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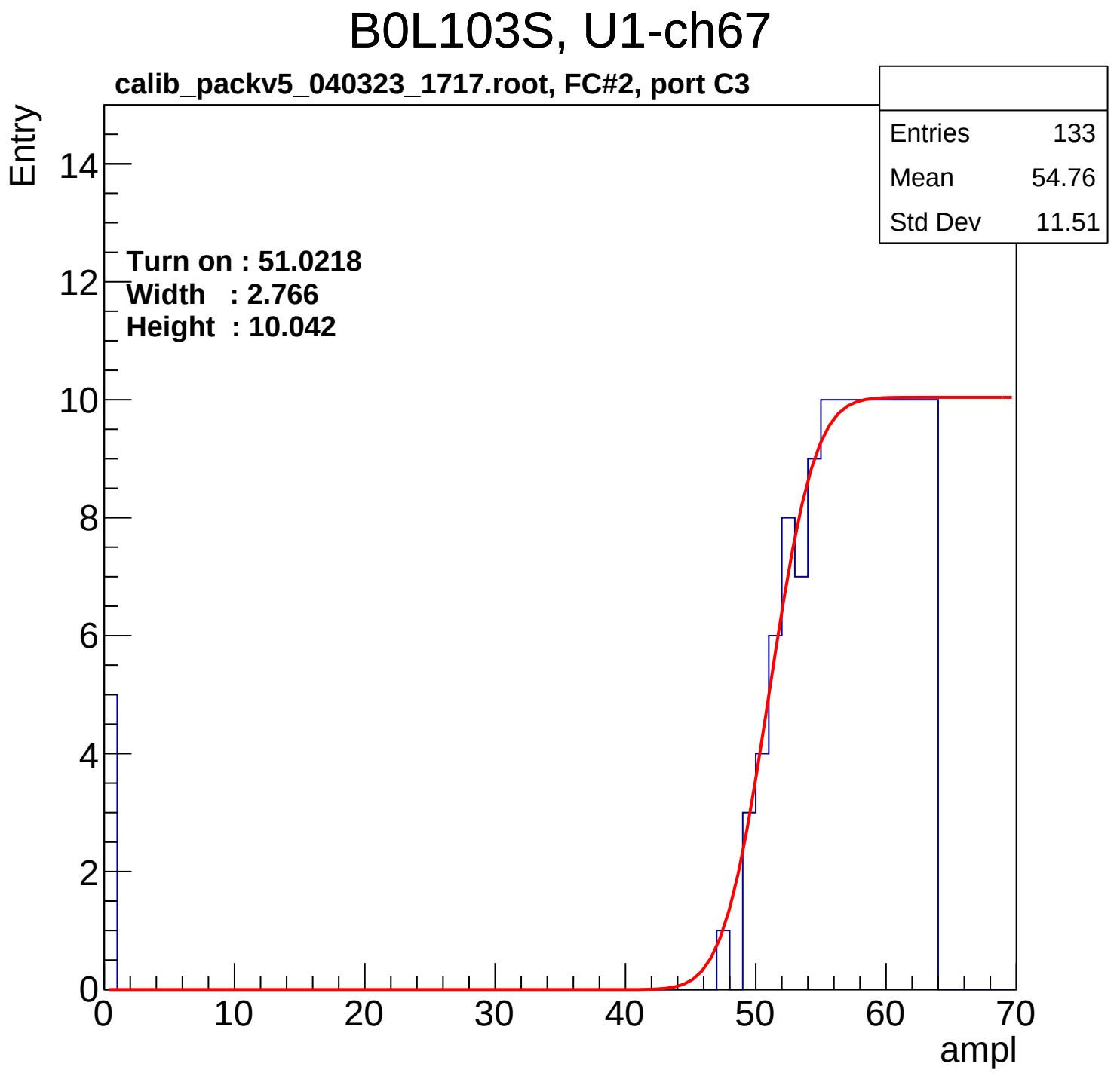
B0L103S, U1-ch67
calib_packv5_040323_1717.root, FC#2, port C3
Entries 133
Mean 54.76
Std Dev 11.51
Turn on : 51.0218
Width : 2.766
Height : 10.042
Entry
ampl
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6
8
10
12
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60
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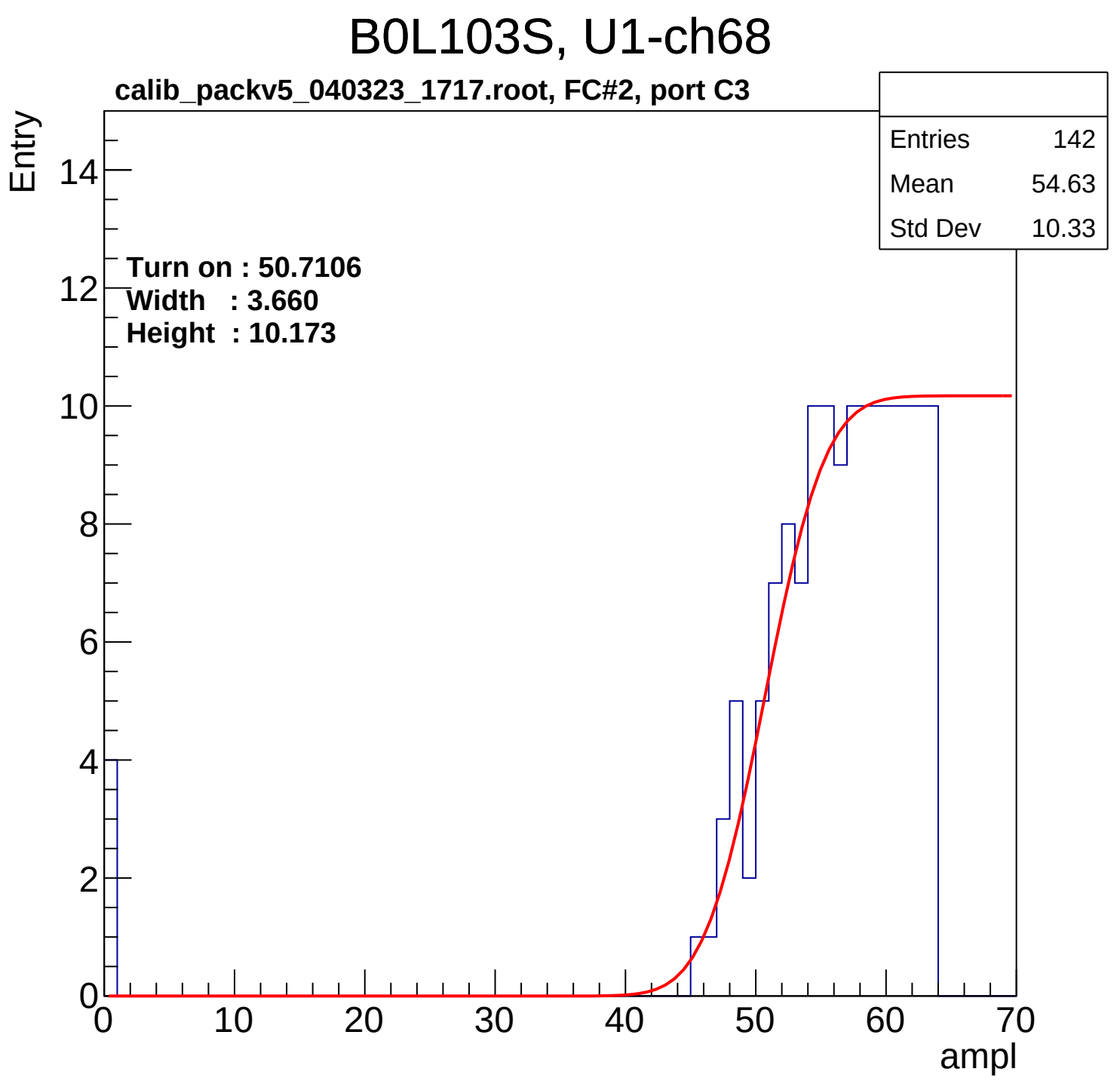
B0L103S, U1-ch68
calib_packv5_040323_1717.root, FC#2, port C3
Entries 142
Mean 54.63
Std Dev 10.33
Turn on : 50.7106
Width : 3.660
Height : 10.173
Entry
ampl
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4
6
8
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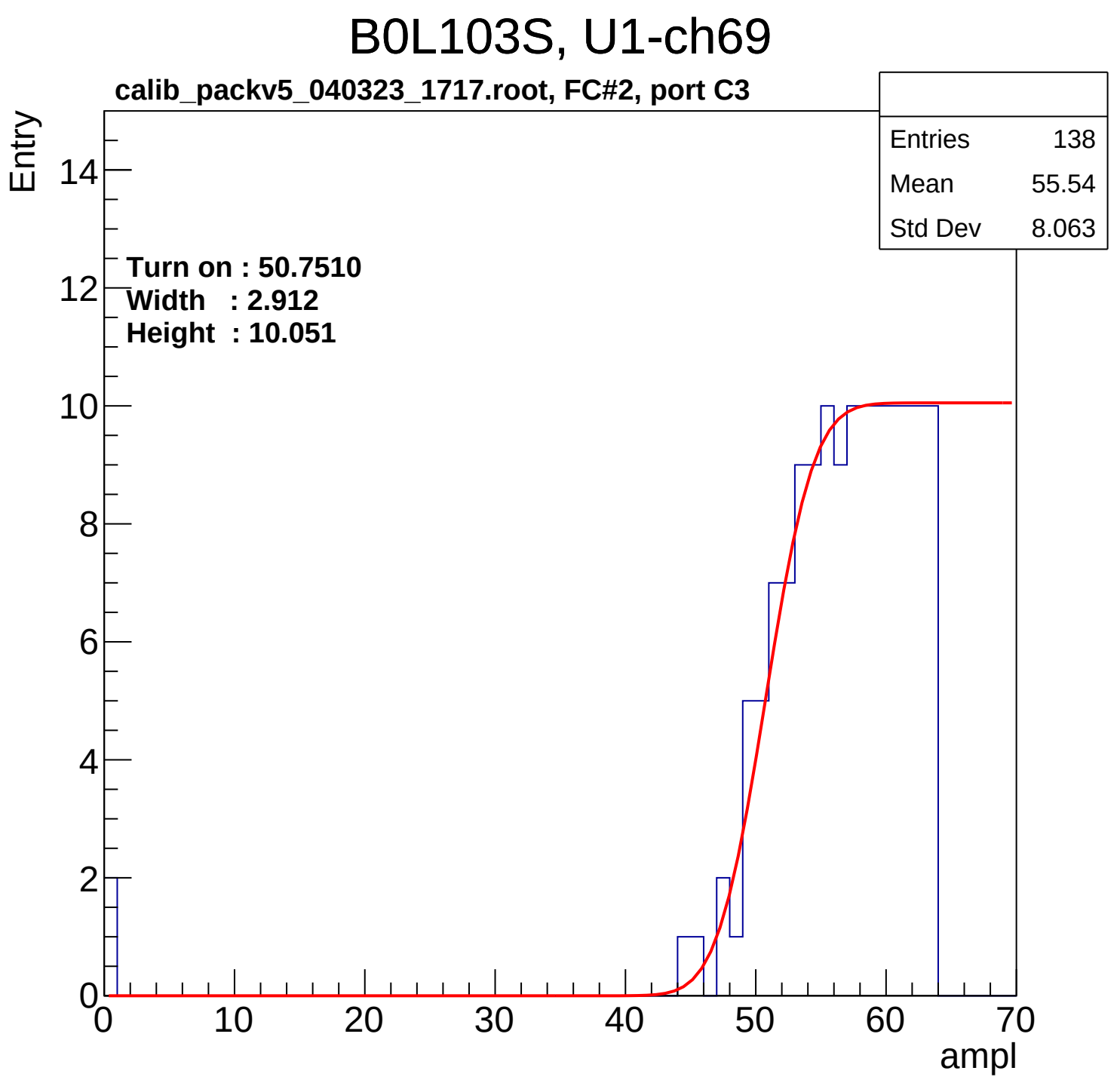
B0L103S, U1-ch69
calib_packv5_040323_1717.root, FC#2, port C3
Entries 138
Mean 55.54
Std Dev 8.063
Turn on : 50.7510
Width : 2.912
Height : 10.051
Entry
ampl
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6
8
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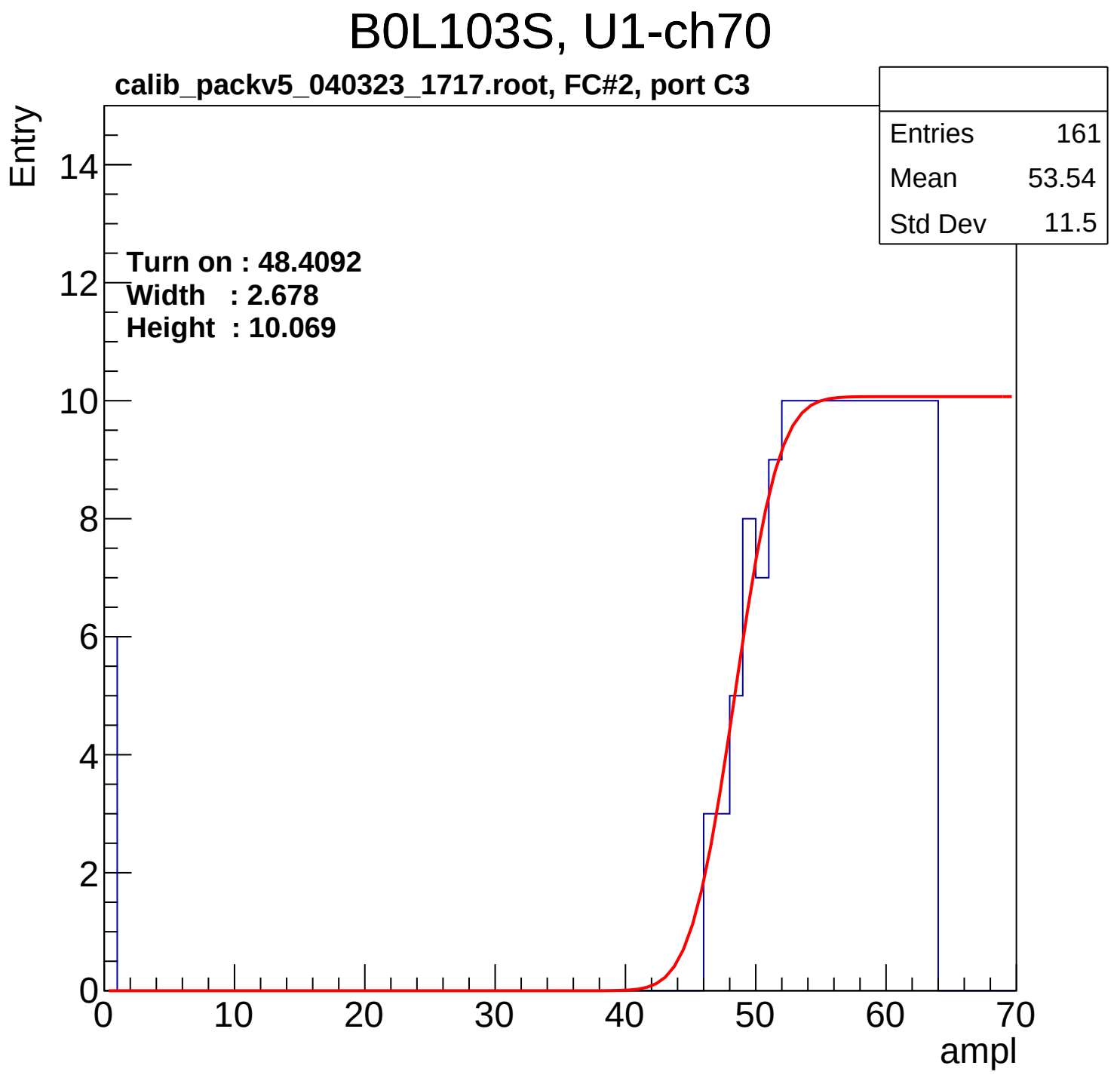
B0L103S, U1-ch70
calib_packv5_040323_1717.root, FC#2, port C3
Entries 161
Mean 53.54
Std Dev 11.5
Turn on : 48.4092
Width : 2.678
Height : 10.069
Entry
ampl
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6
8
10
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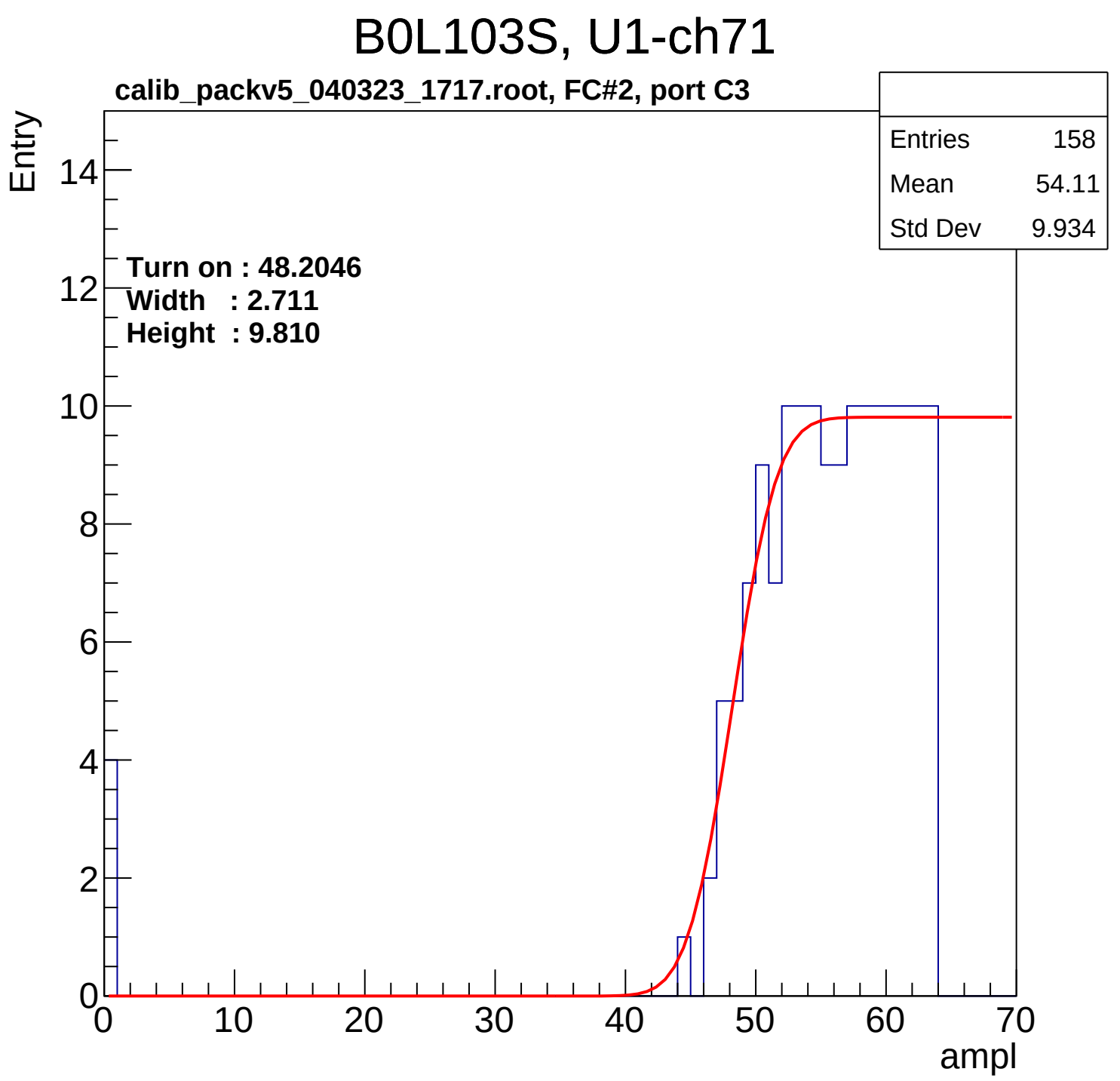
B0L103S, U1-ch71
calib_packv5_040323_1717.root, FC#2, port C3
Entries 158
Mean 54.11
Std Dev 9.934
Turn on : 48.2046
Width : 2.711
Height : 9.810
Entry
ampl
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6
8
10
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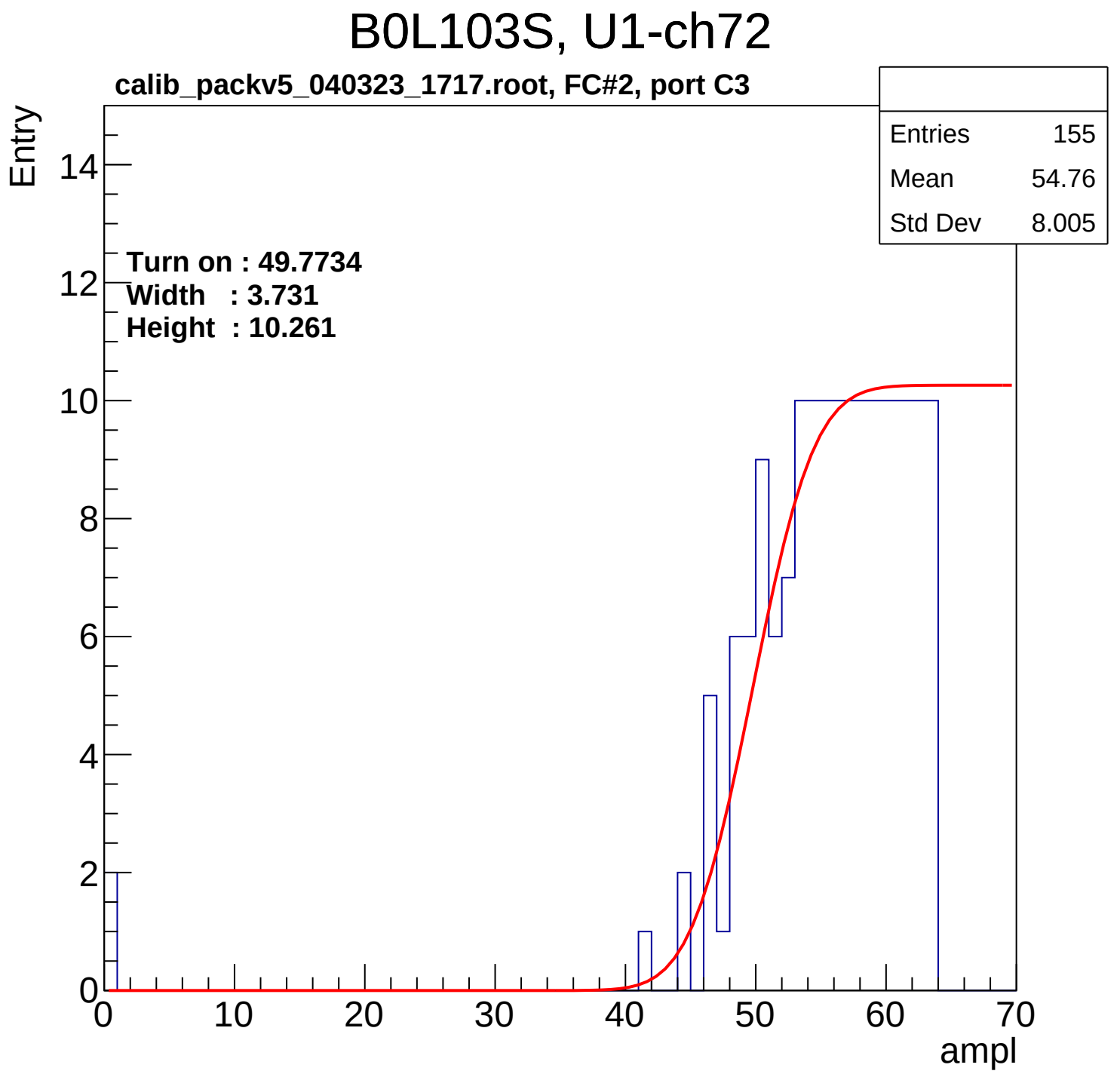
B0L103S, U1-ch72
calib_packv5_040323_1717.root, FC#2, port C3
Entries 155
Mean 54.76
Std Dev 8.005
Turn on : 49.7734
Width : 3.731
Height : 10.261
Entry
ampl
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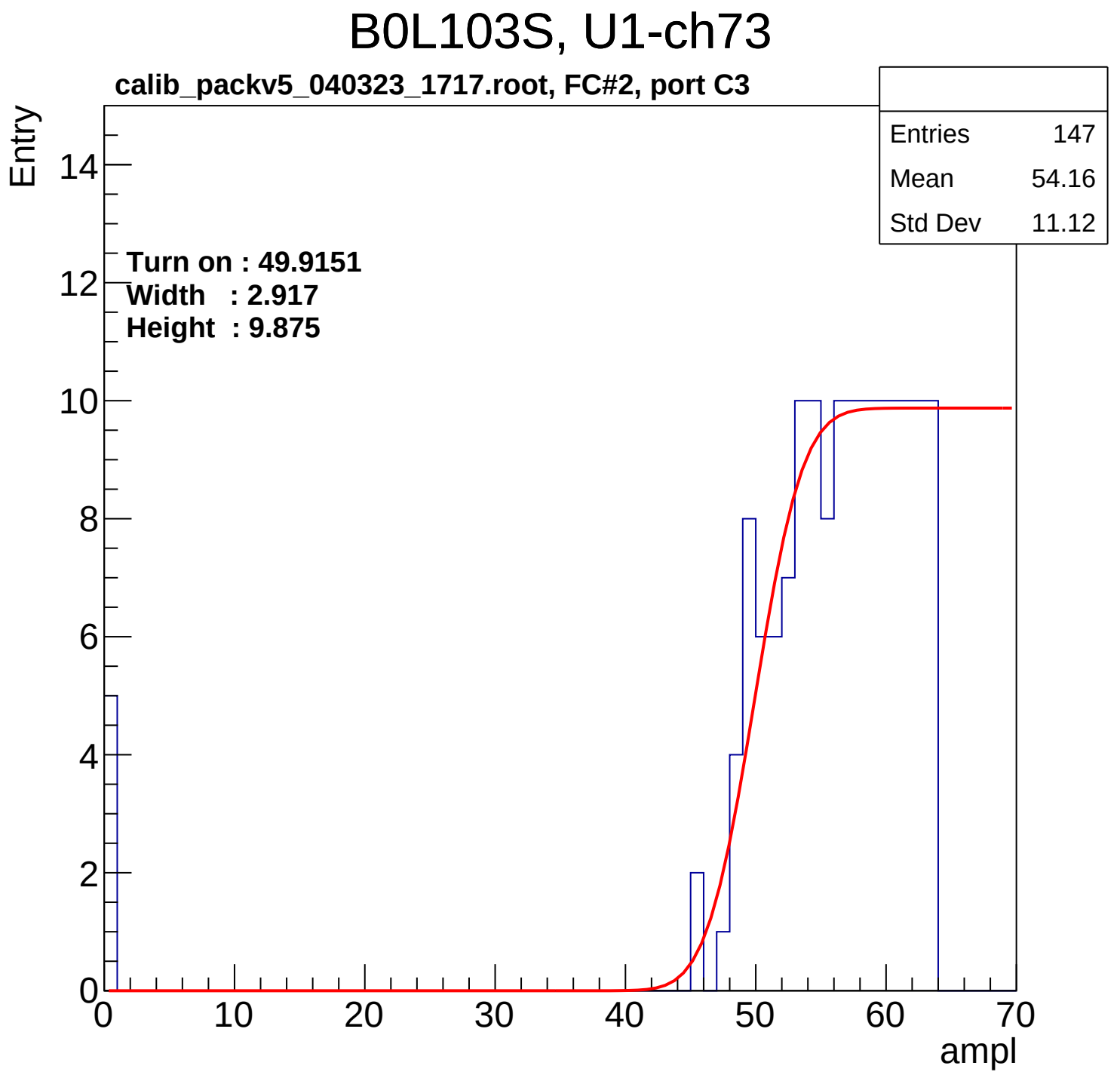
B0L103S, U1-ch73
calib_packv5_040323_1717.root, FC#2, port C3
Entries 147
Mean 54.16
Std Dev 11.12
Turn on : 49.9151
Width : 2.917
Height : 9.875
Entry
ampl
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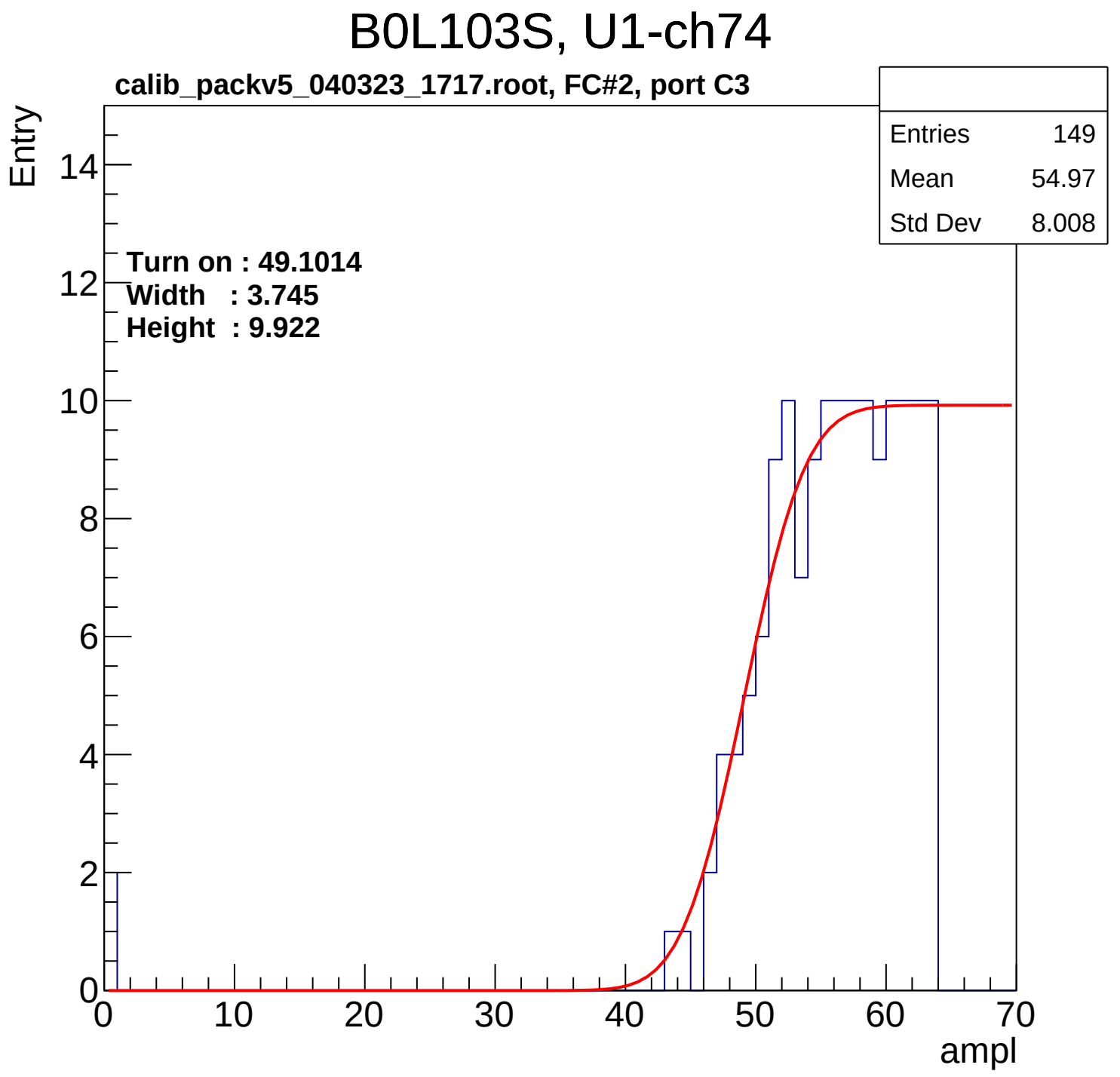
B0L103S, U1-ch74
calib_packv5_040323_1717.root, FC#2, port C3
Entries 149
Mean 54.97
Std Dev 8.008
Turn on : 49.1014
Width : 3.745
Height : 9.922
Entry
ampl
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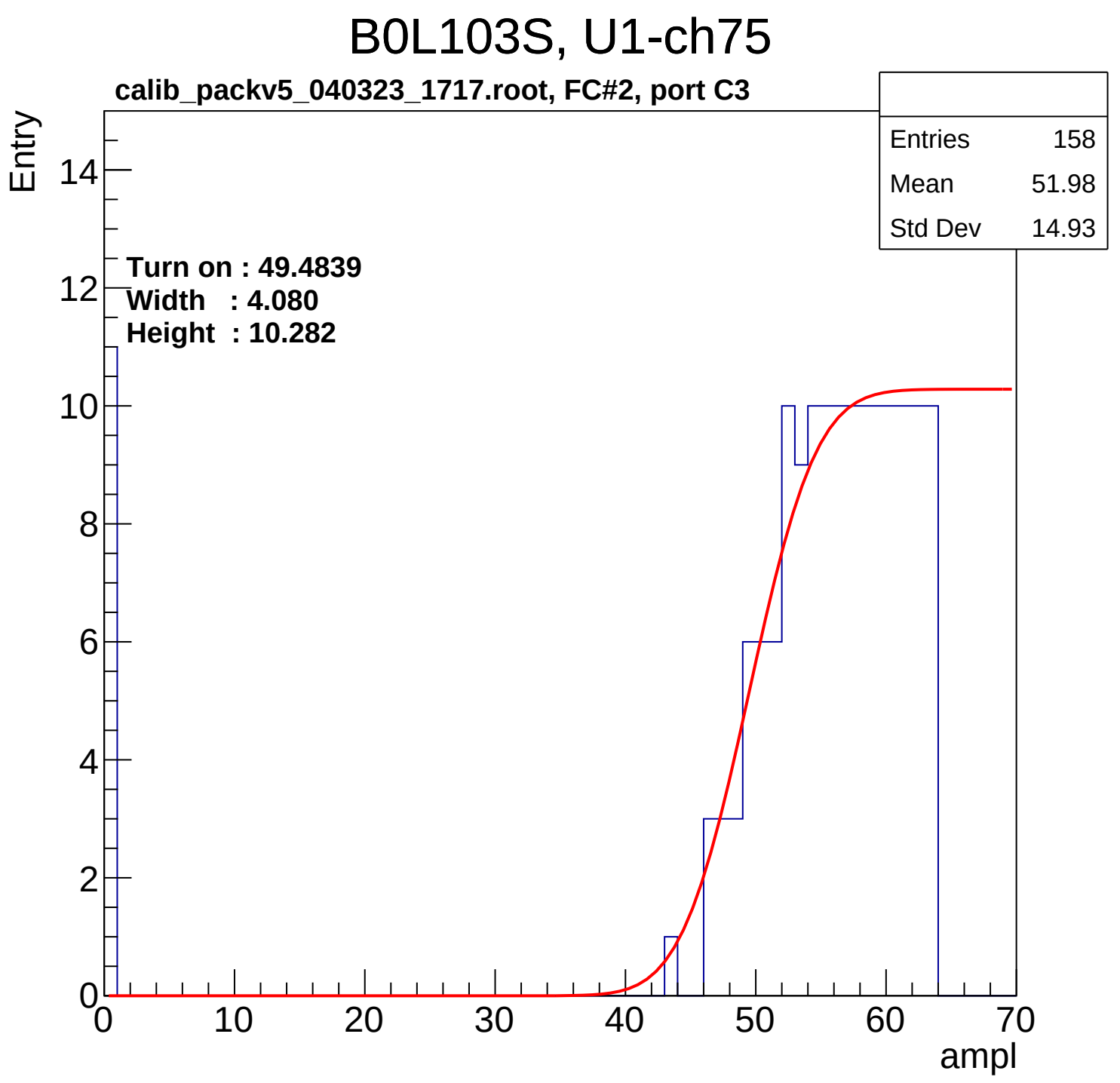
B0L103S, U1-ch75
calib_packv5_040323_1717.root, FC#2, port C3
Entries 158
Mean 51.98
Std Dev 14.93
Turn on : 49.4839
Width : 4.080
Height : 10.282
Entry
ampl
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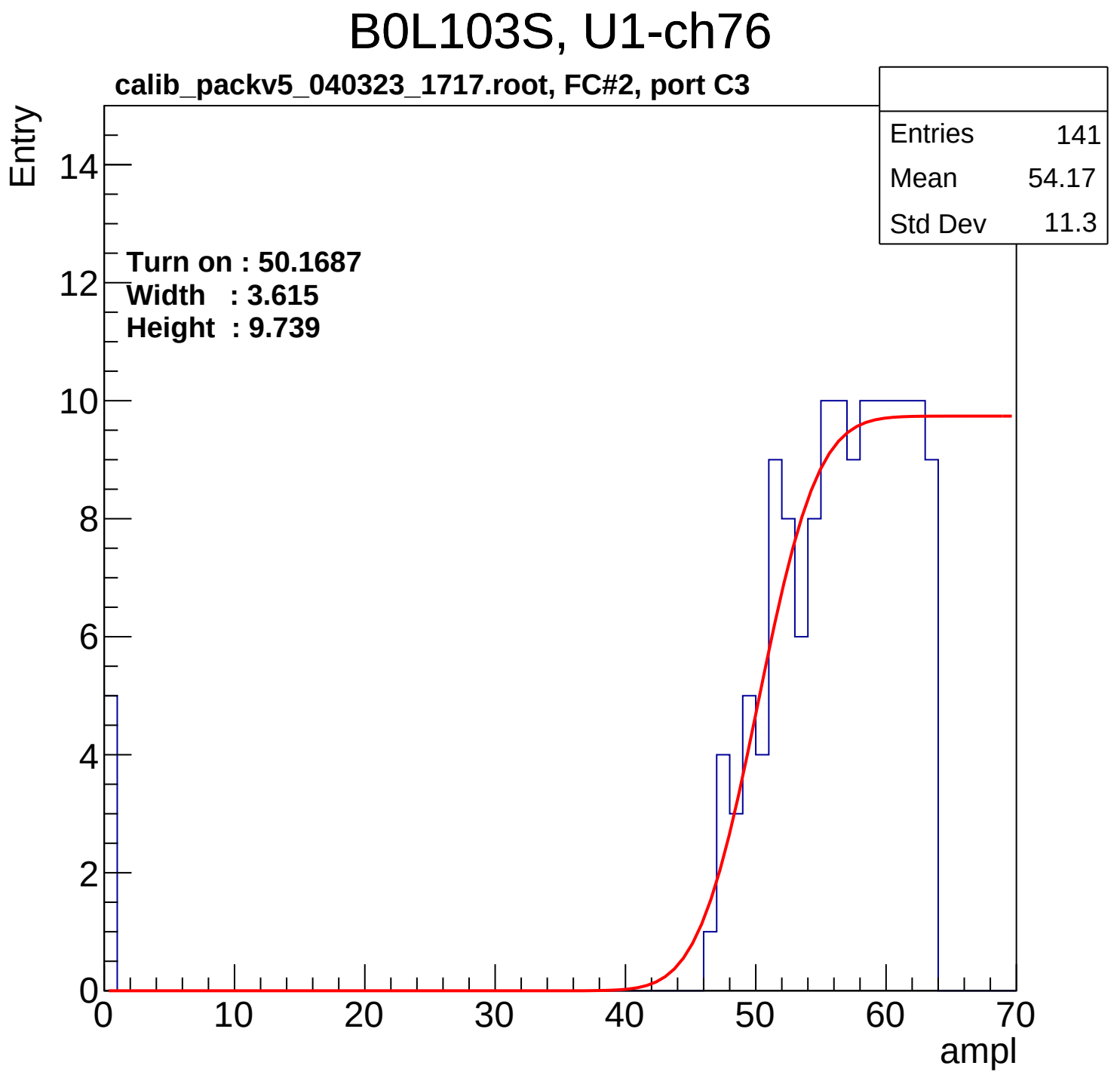
B0L103S, U1-ch76
calib_packv5_040323_1717.root, FC#2, port C3
Entries 141
Mean 54.17
Std Dev 11.3
Turn on : 50.1687
Width : 3.615
Height : 9.739
Entry
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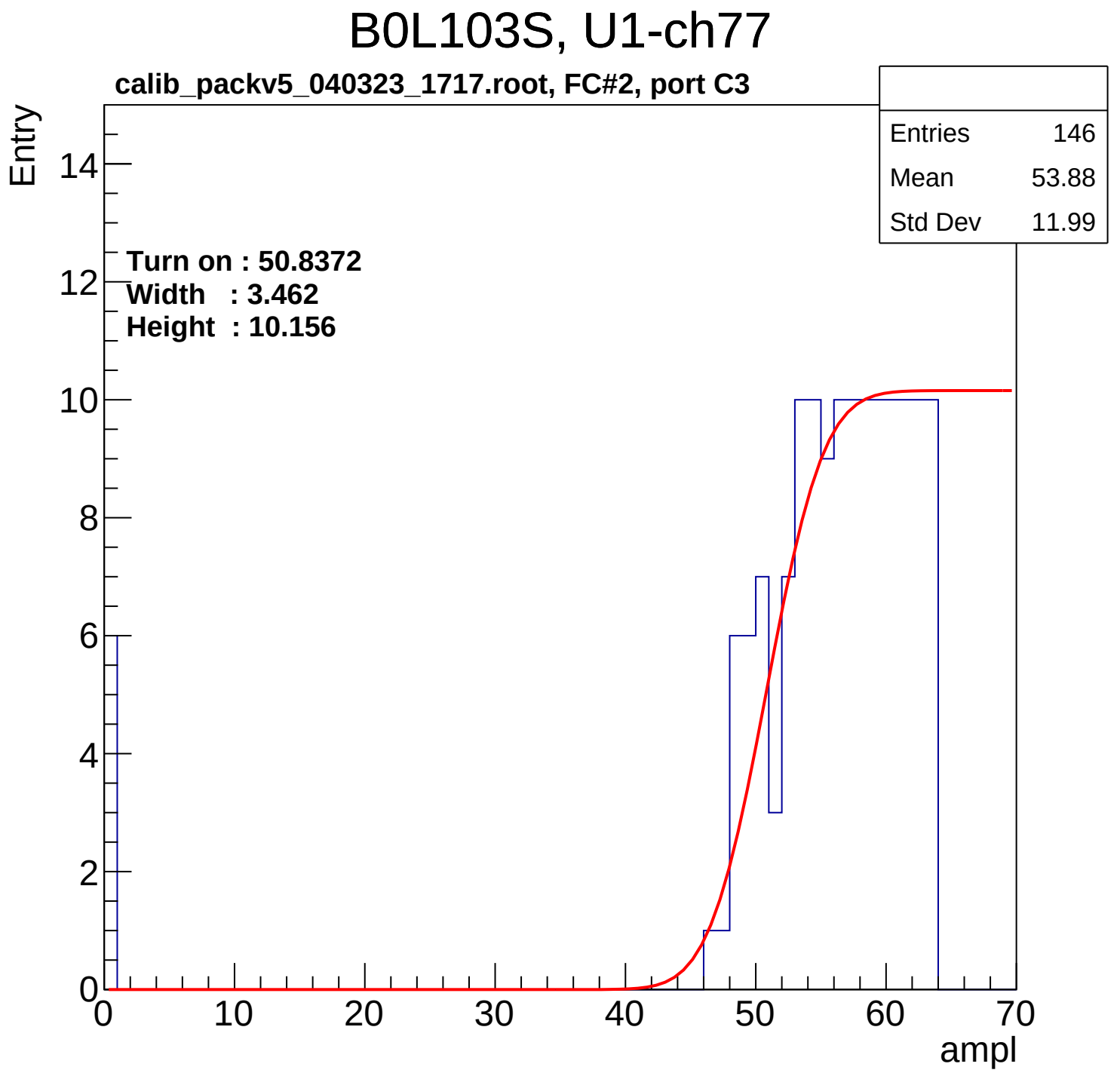
B0L103S, U1-ch77
calib_packv5_040323_1717.root, FC#2, port C3
Entries 146
Mean 53.88
Std Dev 11.99
Turn on : 50.8372
Width : 3.462
Height : 10.156
Entry
ampl
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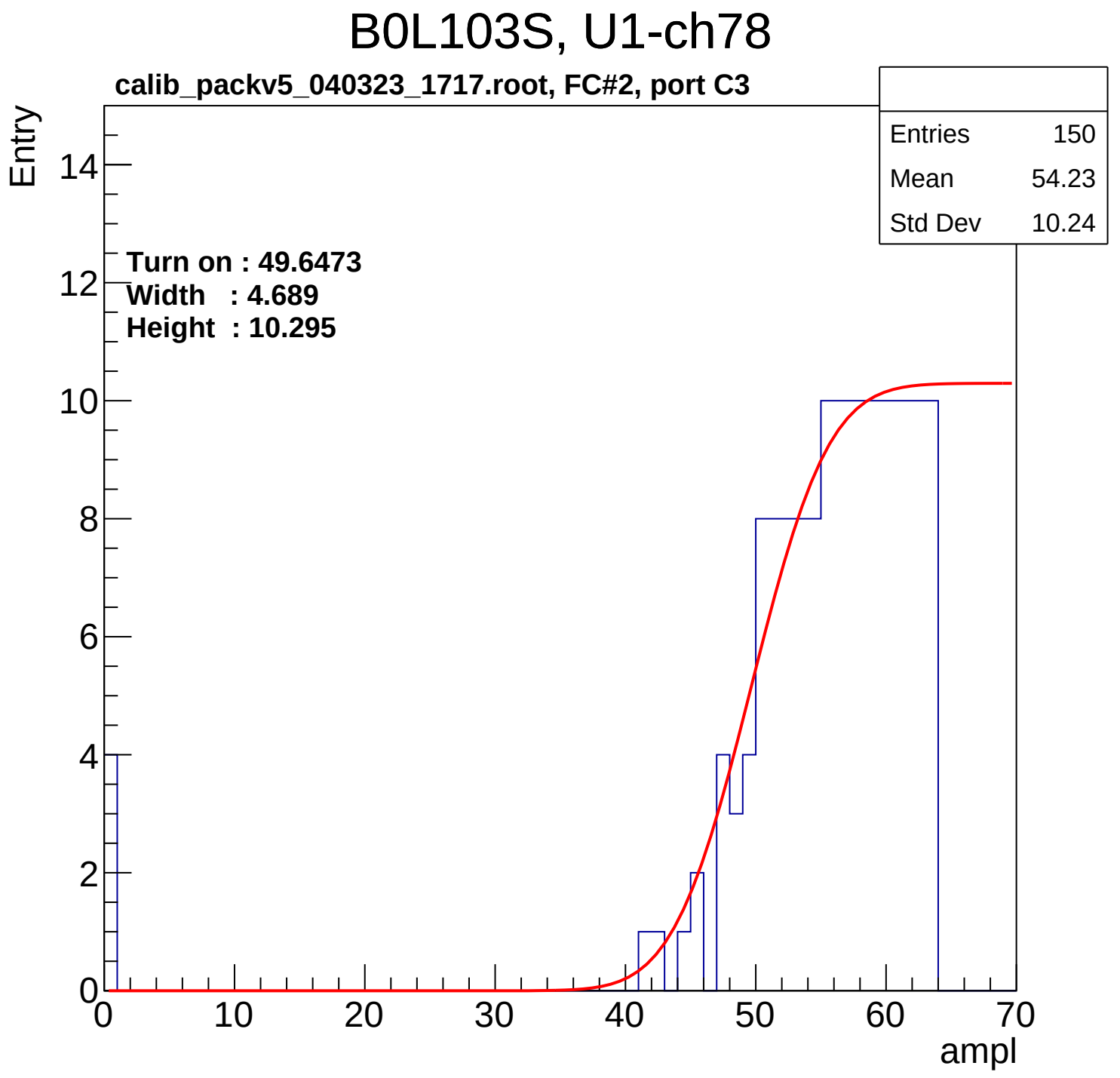
B0L103S, U1-ch78
calib_packv5_040323_1717.root, FC#2, port C3
Entries 150
Mean 54.23
Std Dev 10.24
Turn on : 49.6473
Width : 4.689
Height : 10.295
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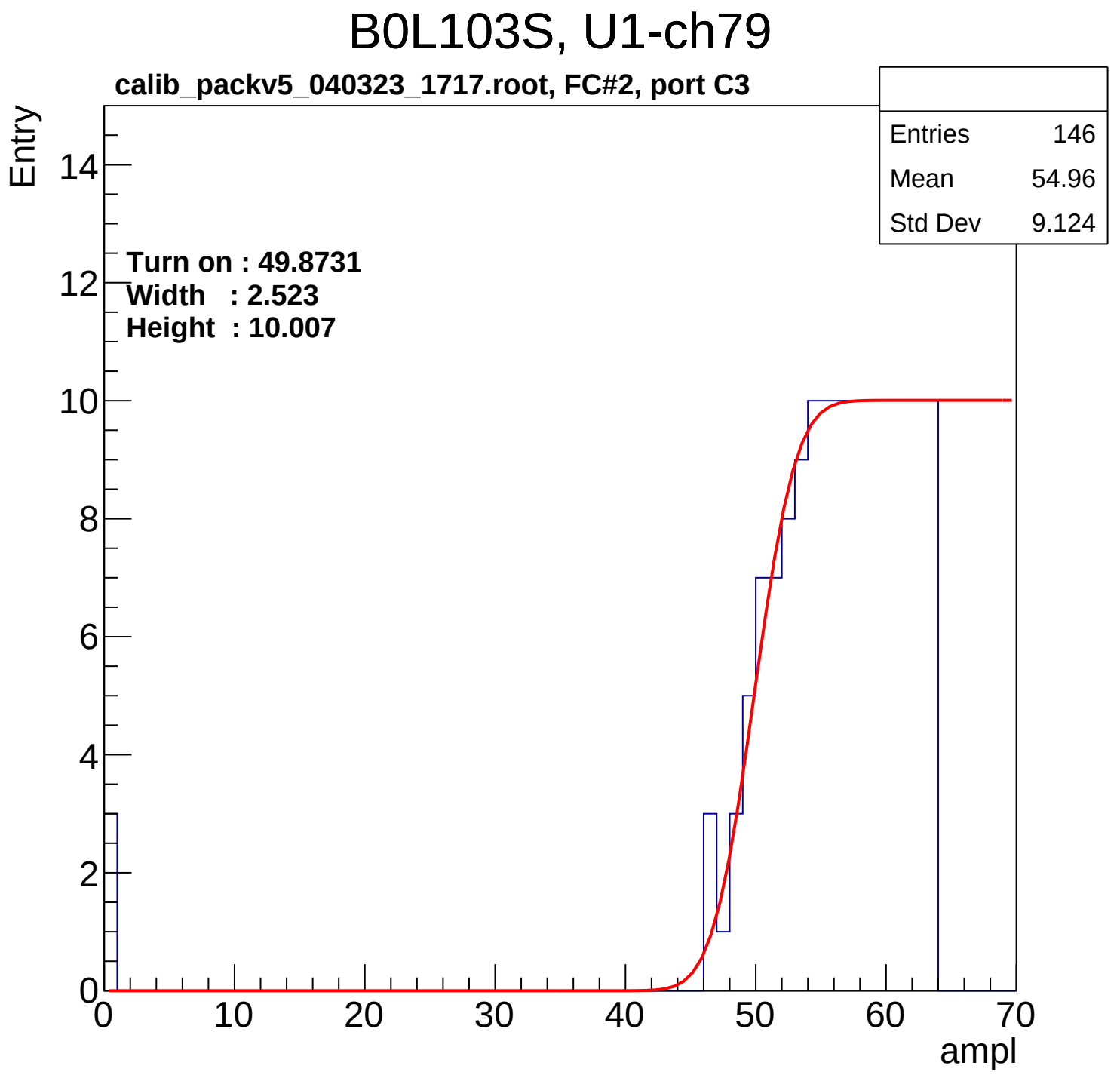
B0L103S, U1-ch79
calib_packv5_040323_1717.root, FC#2, port C3
Entries 146
Mean 54.96
Std Dev 9.124
Turn on : 49.8731
Width : 2.523
Height : 10.007
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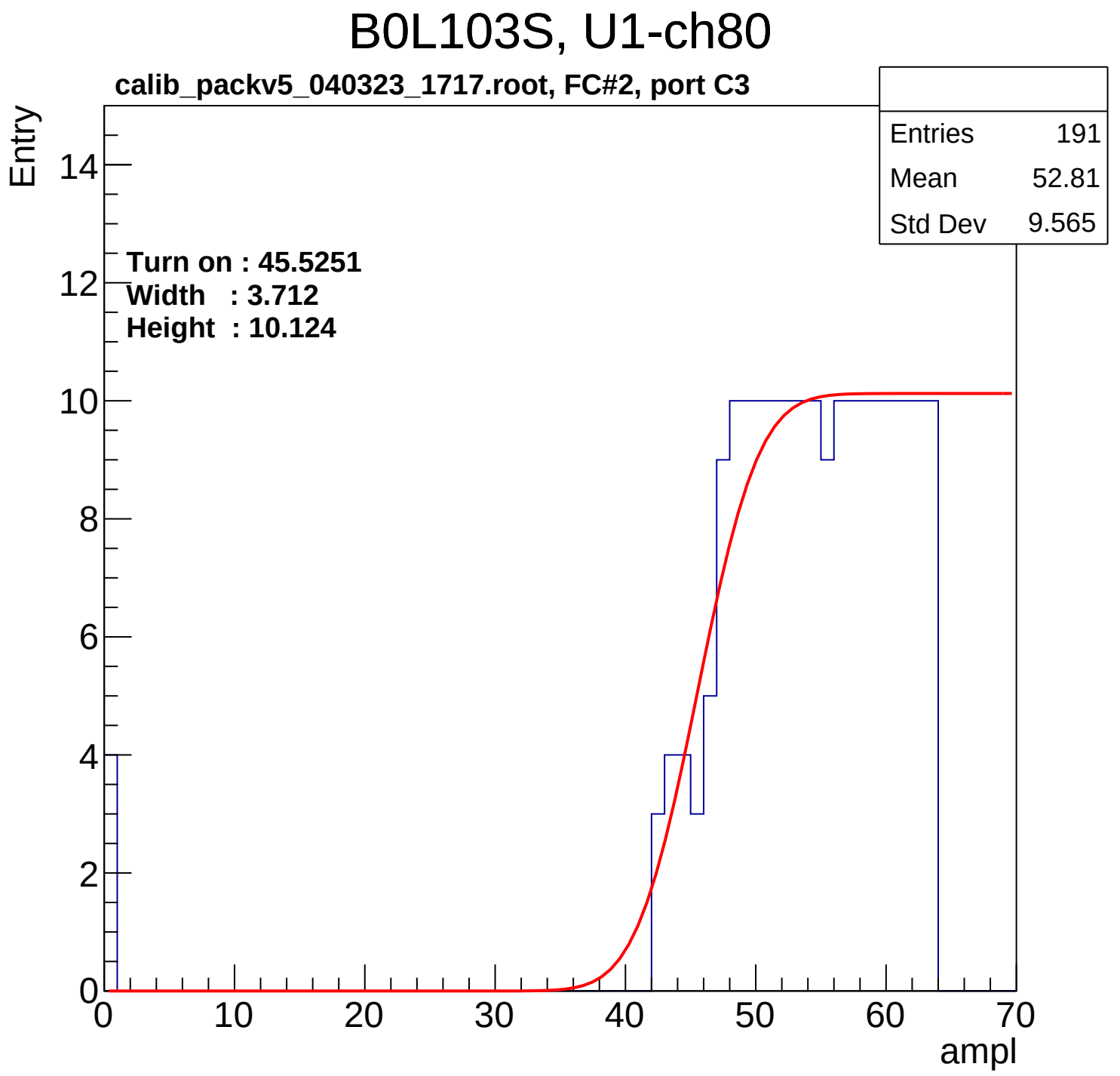
B0L103S, U1-ch80
calib_packv5_040323_1717.root, FC#2, port C3
Entries 191
Mean 52.81
Std Dev 9.565
Turn on : 45.5251
Width : 3.712
Height : 10.124
Entry
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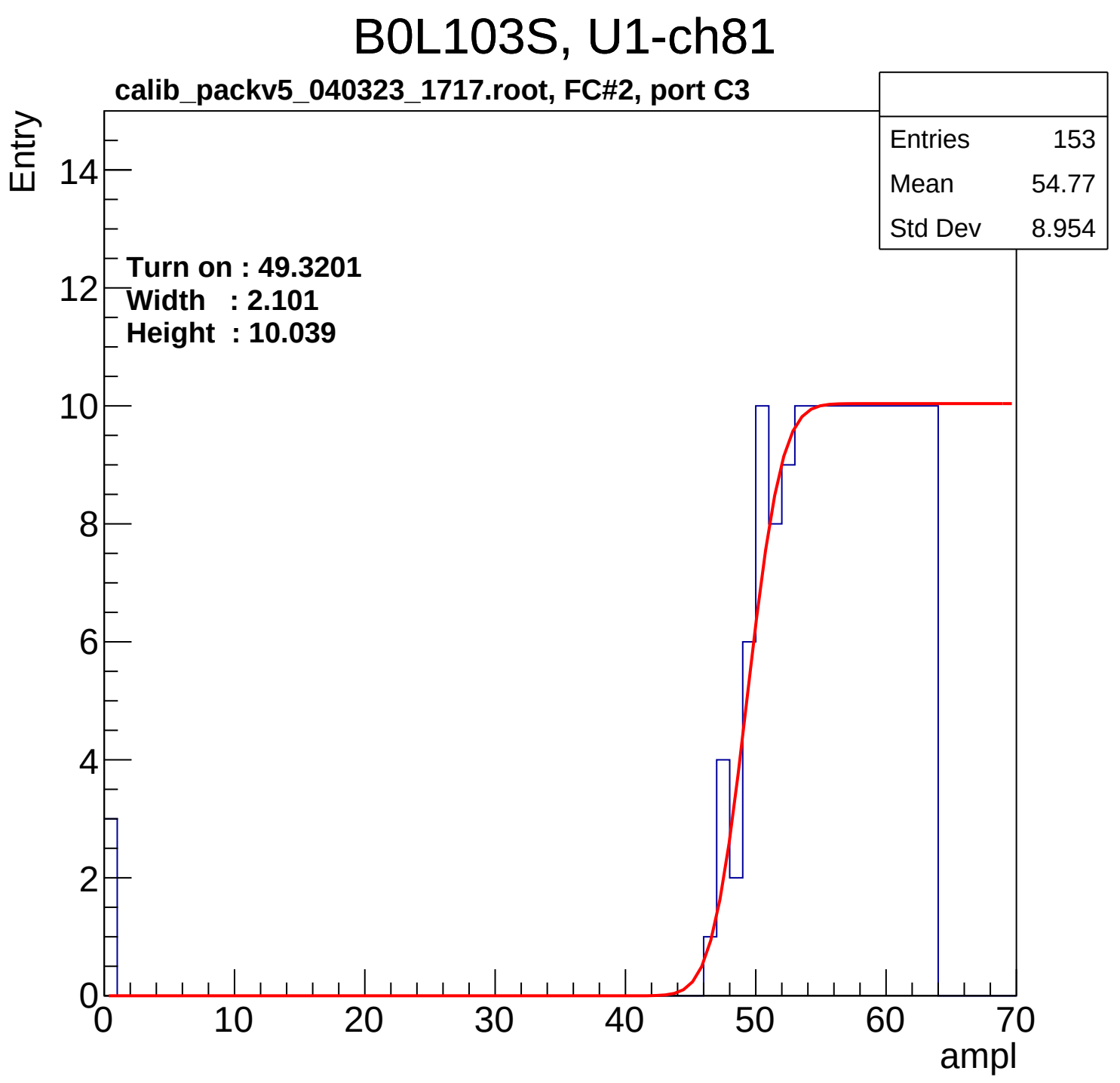
B0L103S, U1-ch81
calib_packv5_040323_1717.root, FC#2, port C3
Entries 153
Mean 54.77
Std Dev 8.954
Turn on : 49.3201
Width : 2.101
Height : 10.039
Entry
ampl
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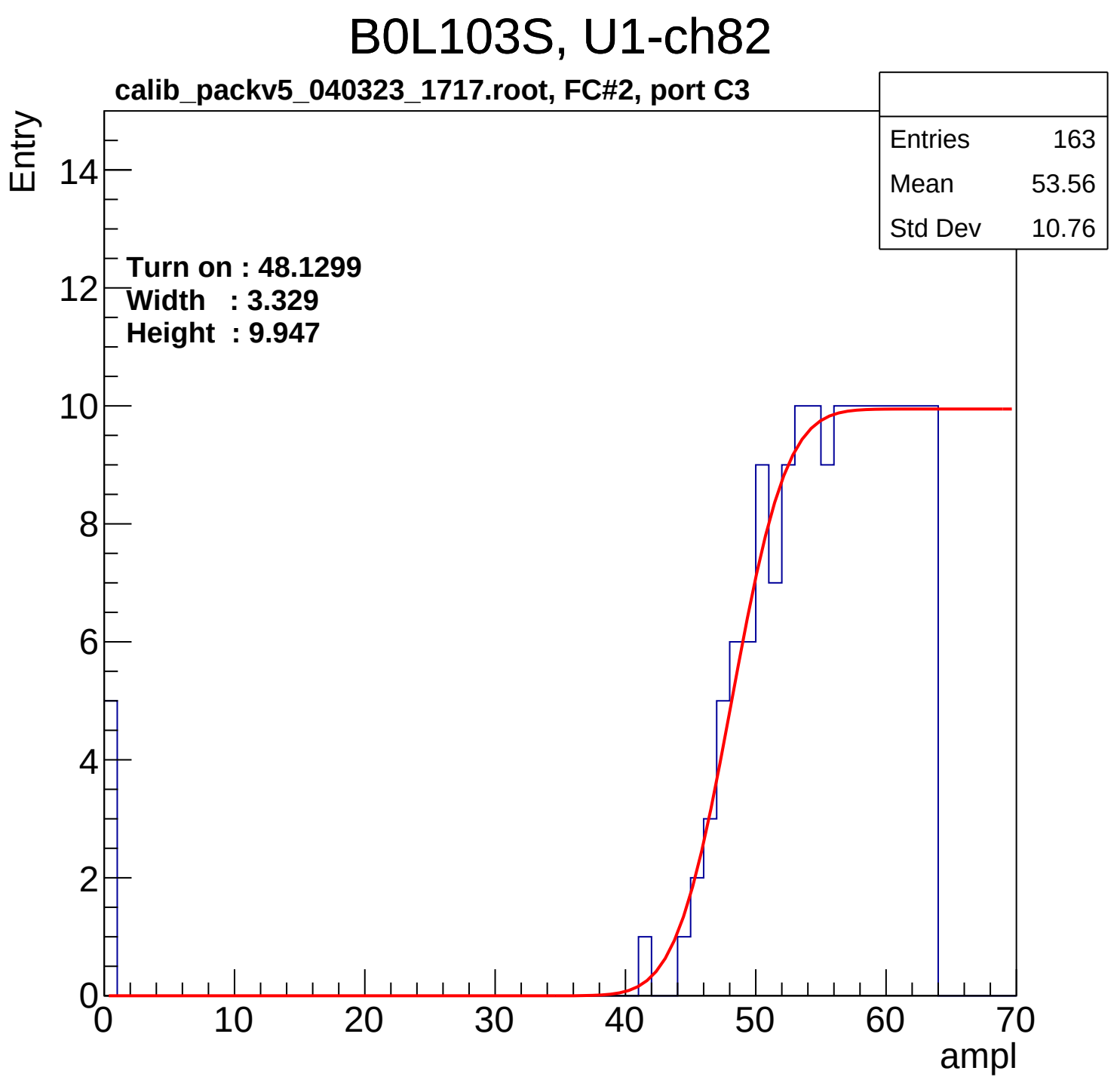
B0L103S, U1-ch82
calib_packv5_040323_1717.root, FC#2, port C3
Entries 163
Mean 53.56
Std Dev 10.76
Turn on : 48.1299
Width : 3.329
Height : 9.947
Entry
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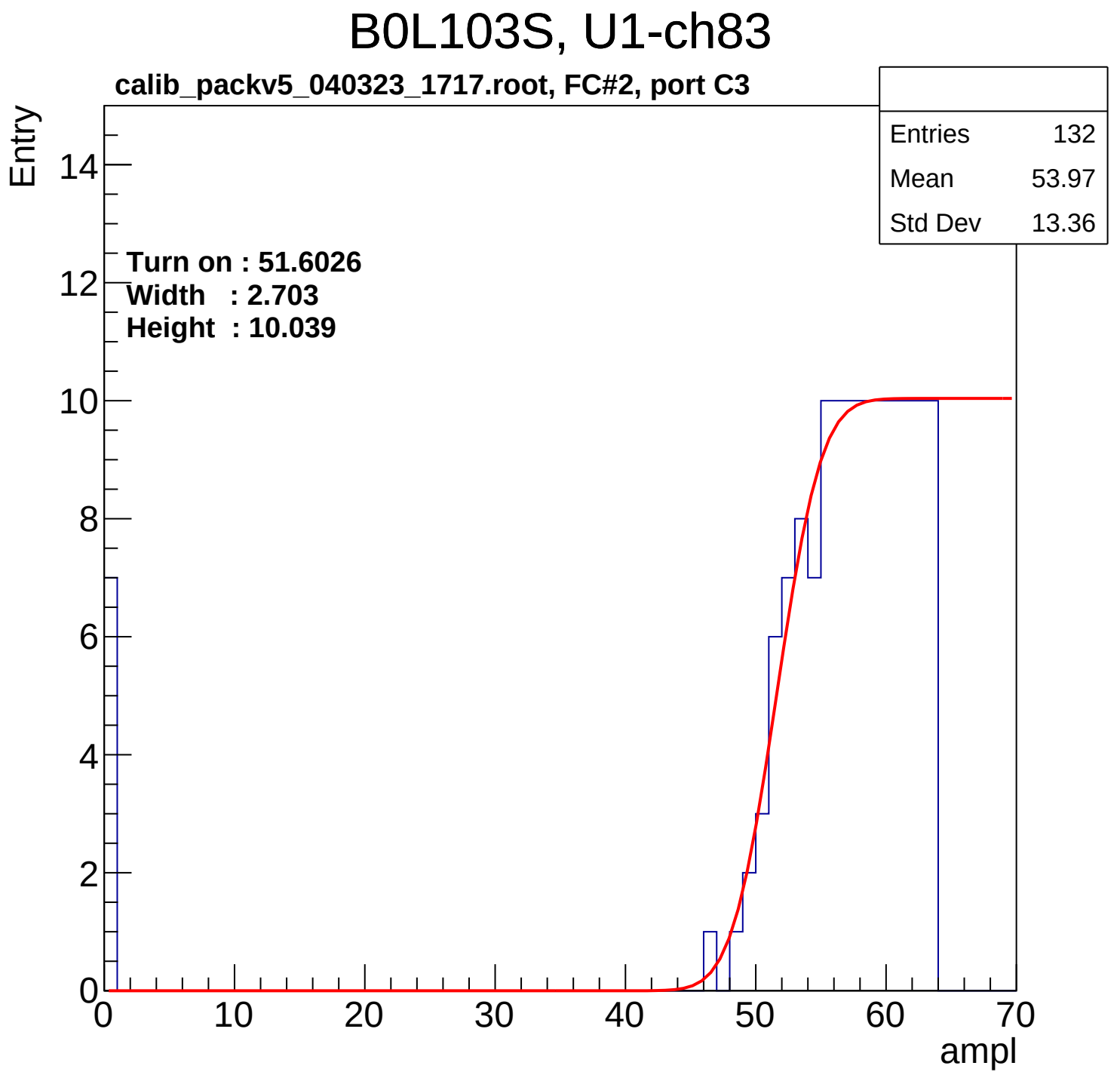
B0L103S, U1-ch83
calib_packv5_040323_1717.root, FC#2, port C3
Entries 132
Mean 53.97
Std Dev 13.36
Turn on : 51.6026
Width : 2.703
Height : 10.039
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ampl
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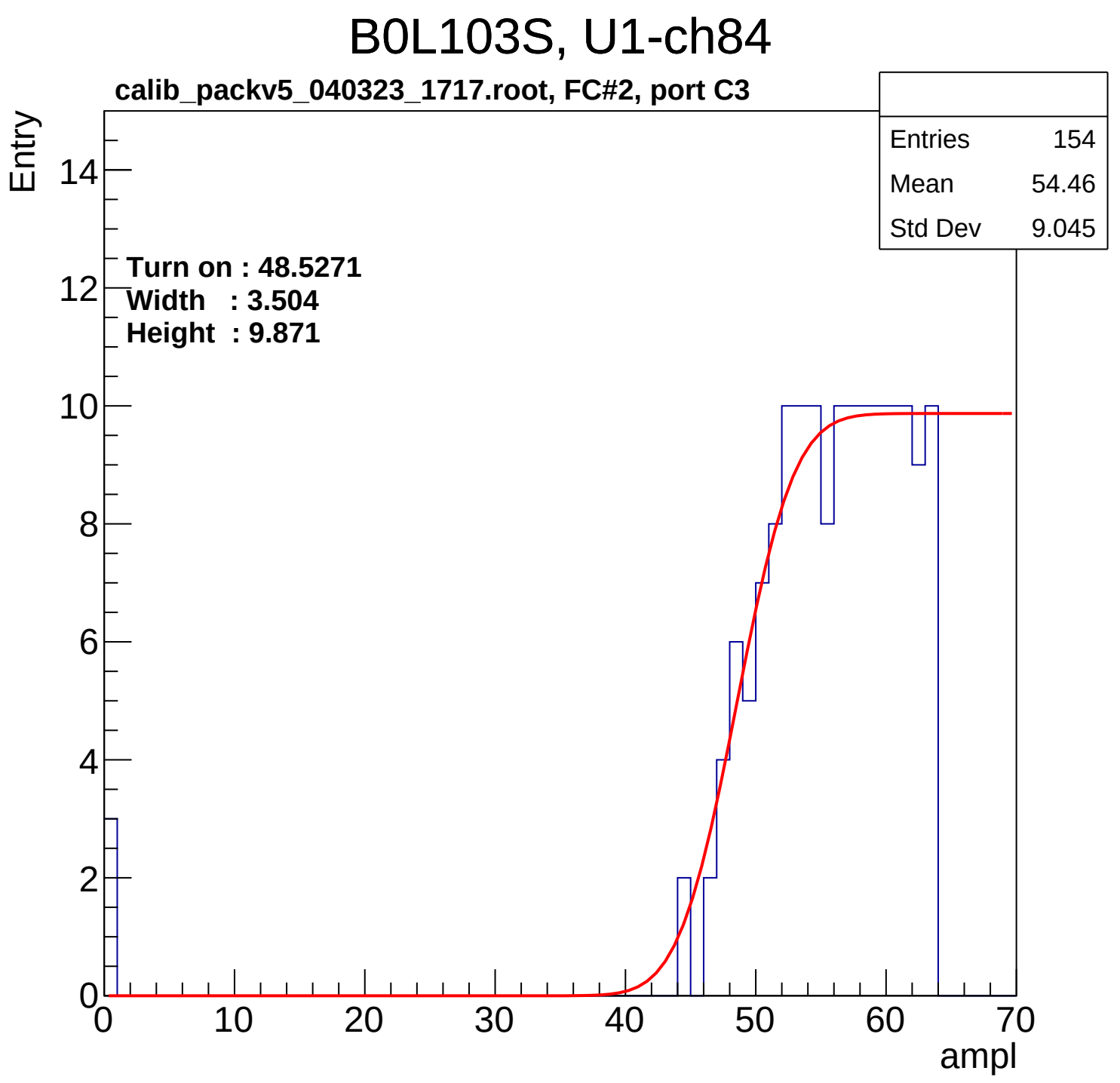
B0L103S, U1-ch84
calib_packv5_040323_1717.root, FC#2, port C3
Entries 154
Mean 54.46
Std Dev 9.045
Turn on : 48.5271
Width : 3.504
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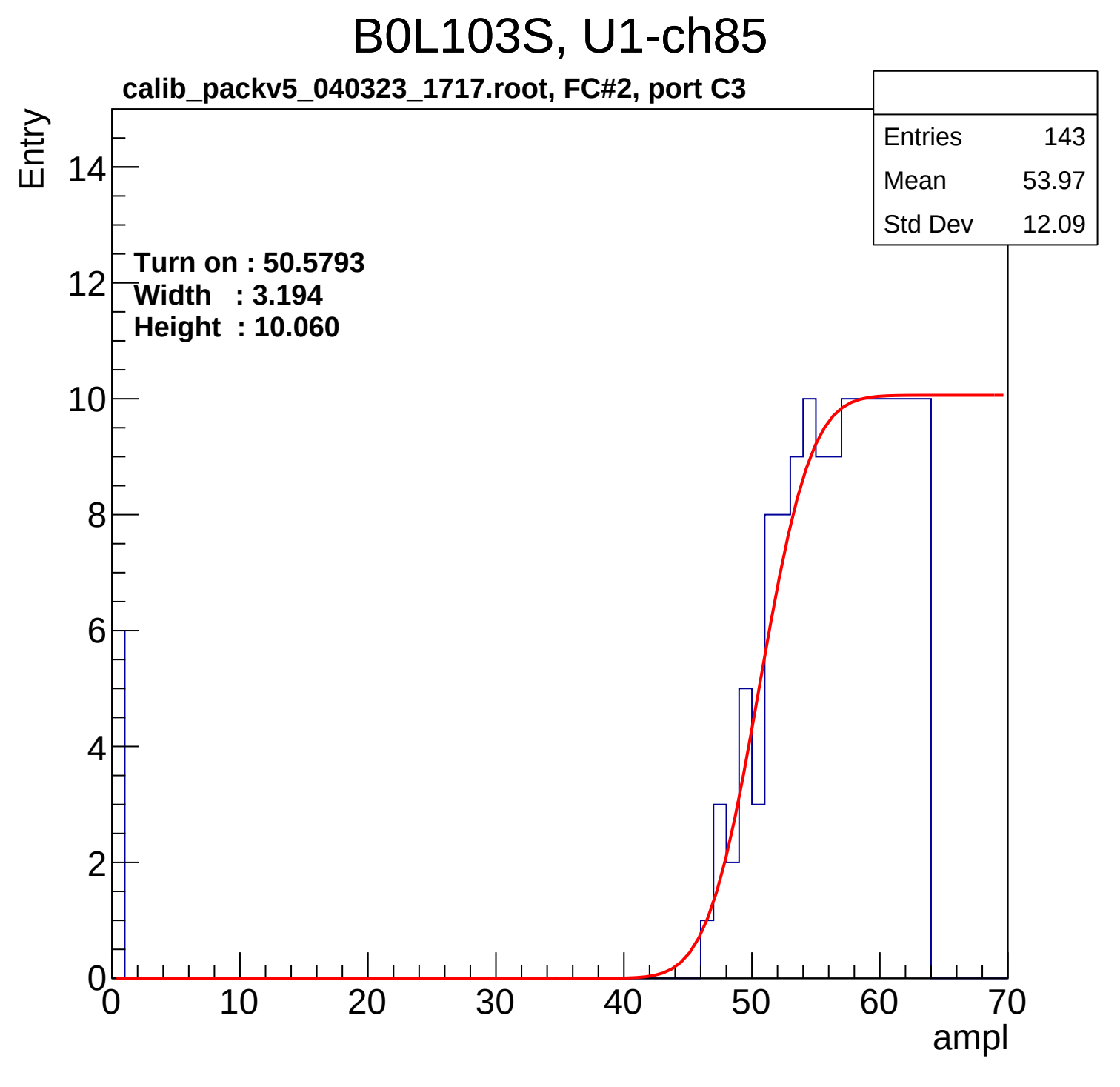
B0L103S, U1-ch85
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 53.97
Std Dev 12.09
Turn on : 50.5793
Width : 3.194
Height : 10.060
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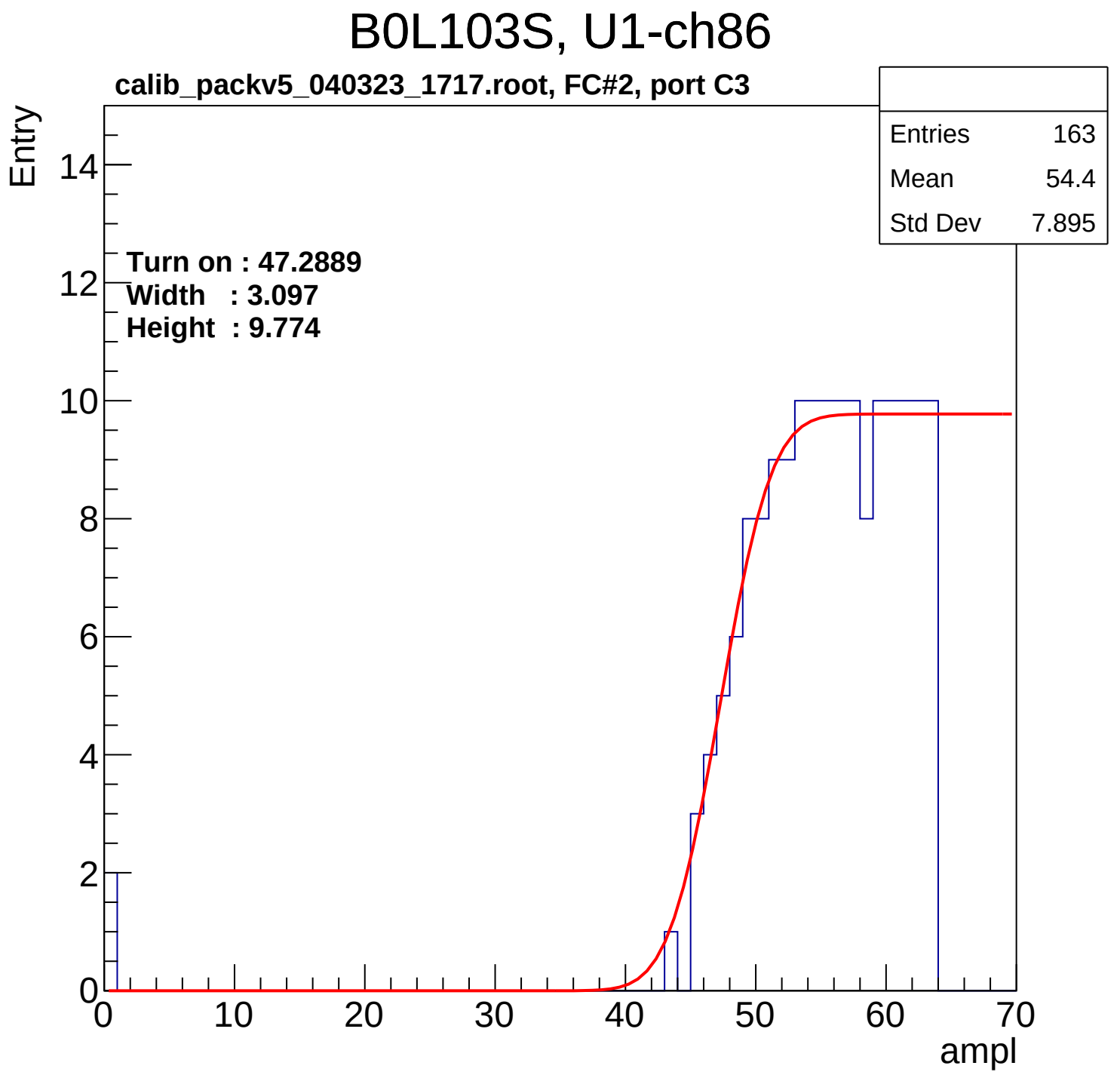
B0L103S, U1-ch86
calib_packv5_040323_1717.root, FC#2, port C3
Entries 163
Mean 54.4
Std Dev 7.895
Turn on : 47.2889
Width : 3.097
Height : 9.774
Entry
ampl
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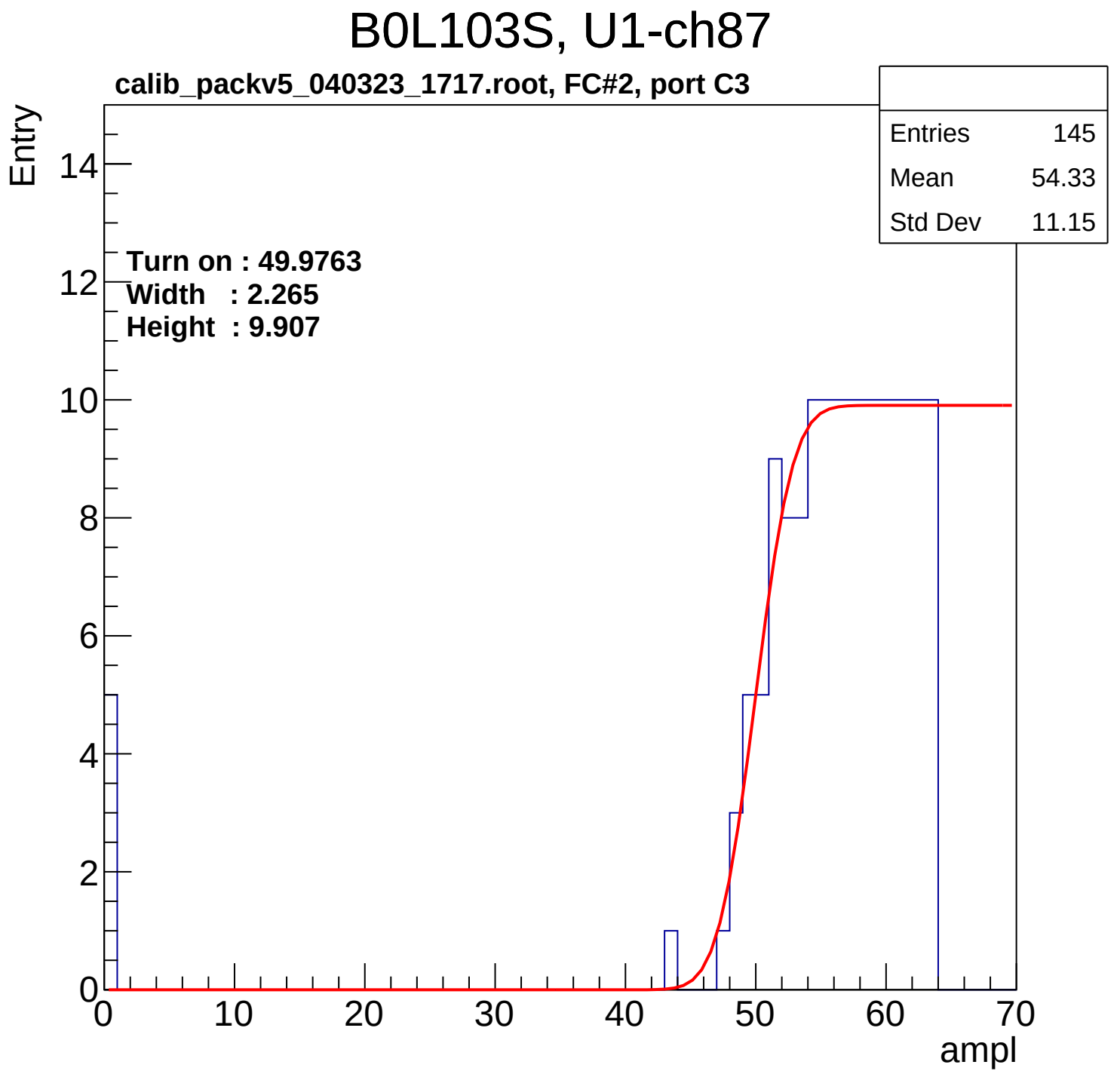
B0L103S, U1-ch87
calib_packv5_040323_1717.root, FC#2, port C3
Entries 145
Mean 54.33
Std Dev 11.15
Turn on : 49.9763
Width : 2.265
Height : 9.907
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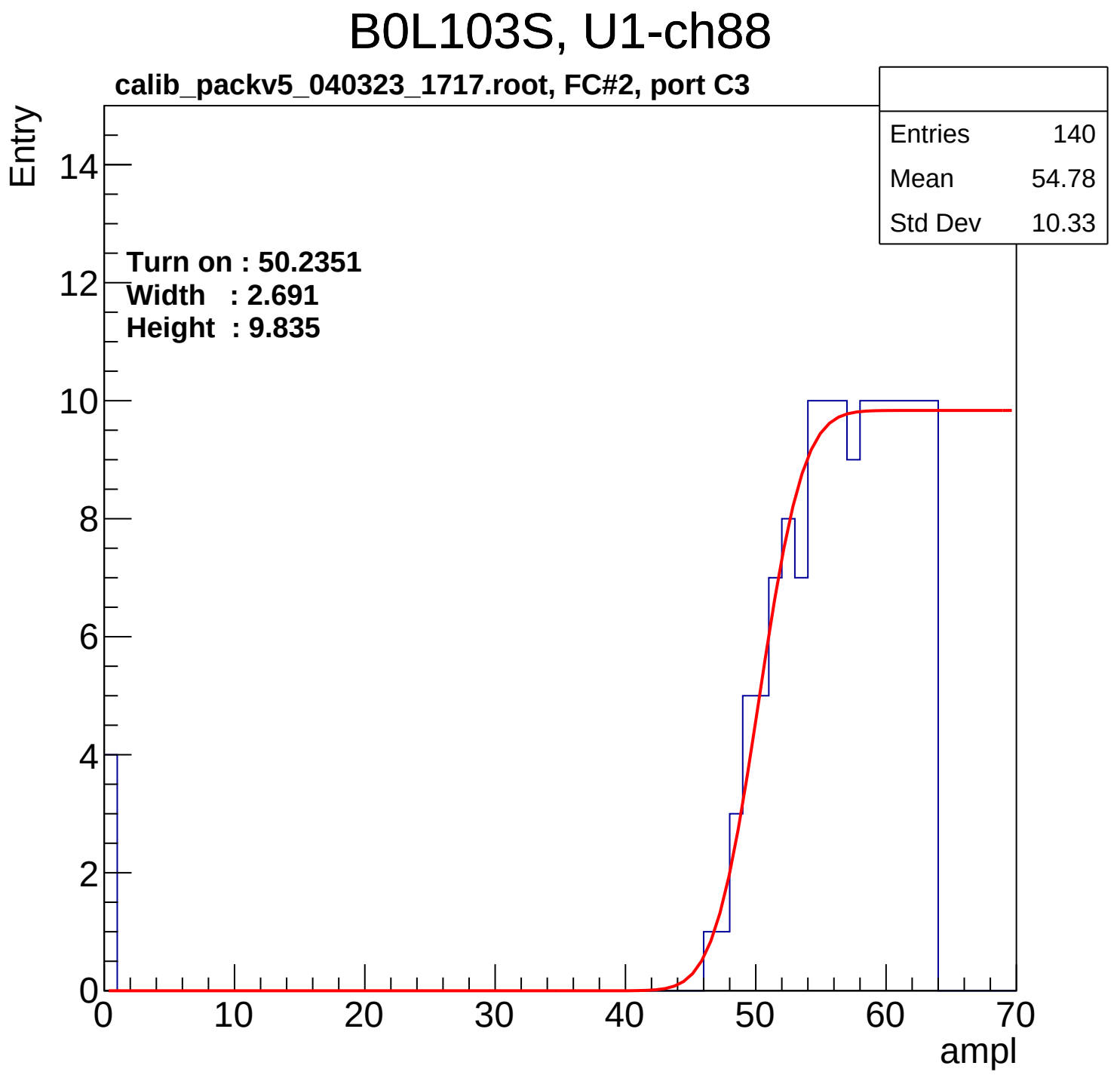
B0L103S, U1-ch88
calib_packv5_040323_1717.root, FC#2, port C3
Entries 140
Mean 54.78
Std Dev 10.33
Turn on : 50.2351
Width : 2.691
Height : 9.835
Entry
ampl
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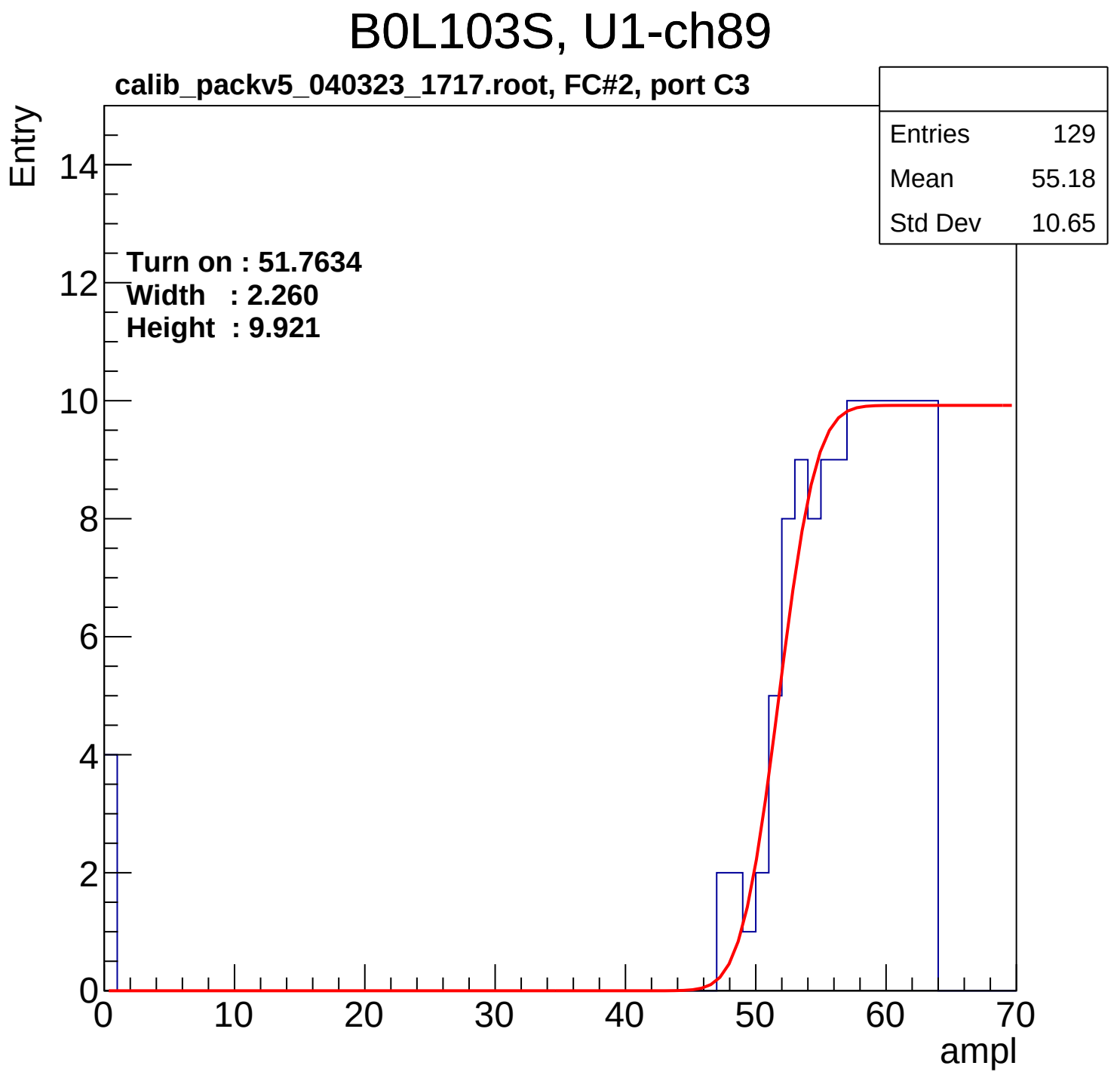
B0L103S, U1-ch89
calib_packv5_040323_1717.root, FC#2, port C3
Entries 129
Mean 55.18
Std Dev 10.65
Turn on : 51.7634
Width : 2.260
Height : 9.921
Entry
ampl
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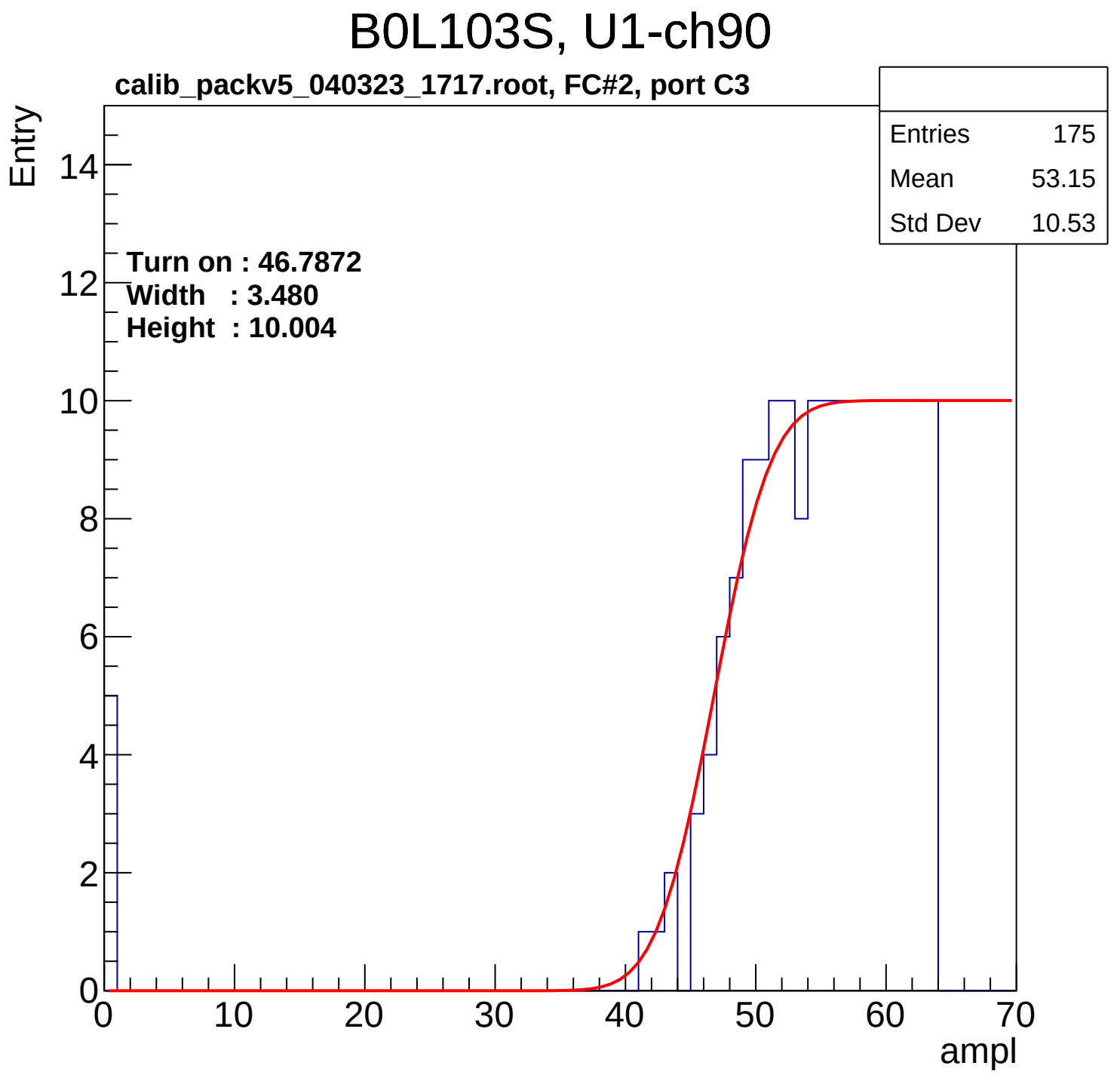
B0L103S, U1-ch90
calib_packv5_040323_1717.root, FC#2, port C3
Entries 175
Mean 53.15
Std Dev 10.53
Turn on : 46.7872
Width : 3.480
Height : 10.004
Entry
ampl
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8
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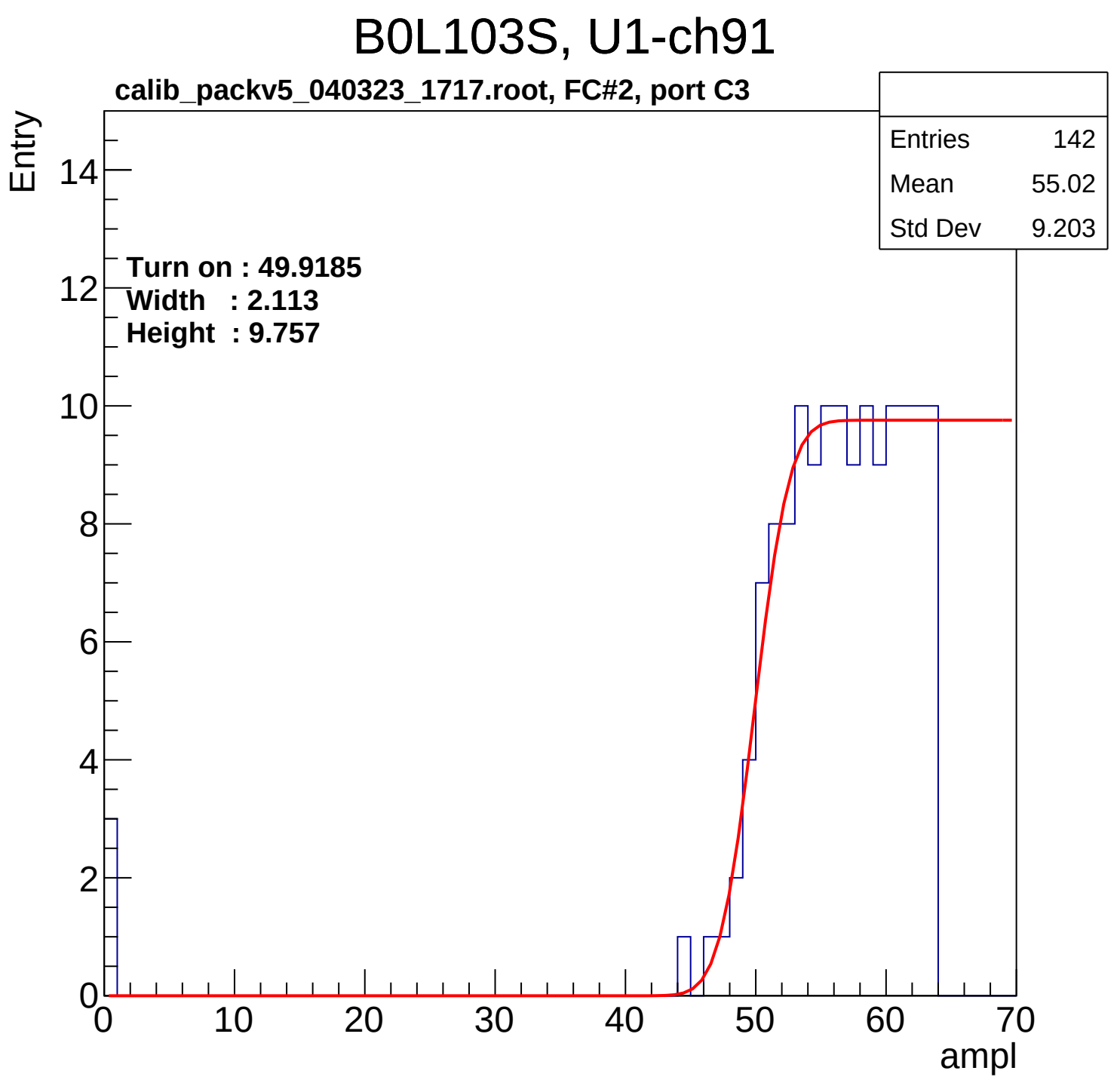
B0L103S, U1-ch91
calib_packv5_040323_1717.root, FC#2, port C3
Entries 142
Mean 55.02
Std Dev 9.203
Turn on : 49.9185
Width : 2.113
Height : 9.757
Entry
ampl
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8
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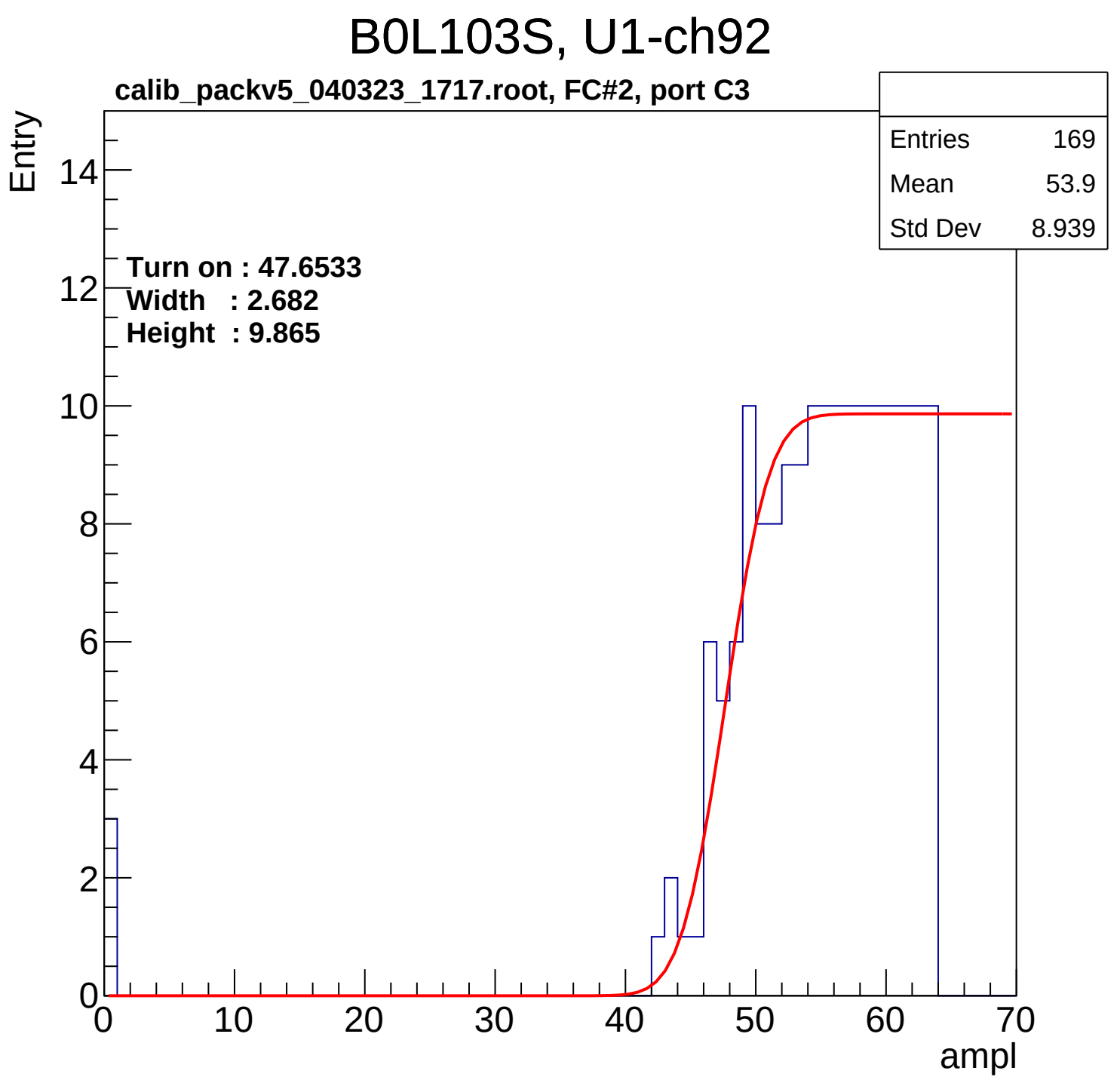
B0L103S, U1-ch92
calib_packv5_040323_1717.root, FC#2, port C3
Entries 169
Mean 53.9
Std Dev 8.939
Turn on : 47.6533
Width : 2.682
Height : 9.865
Entry
ampl
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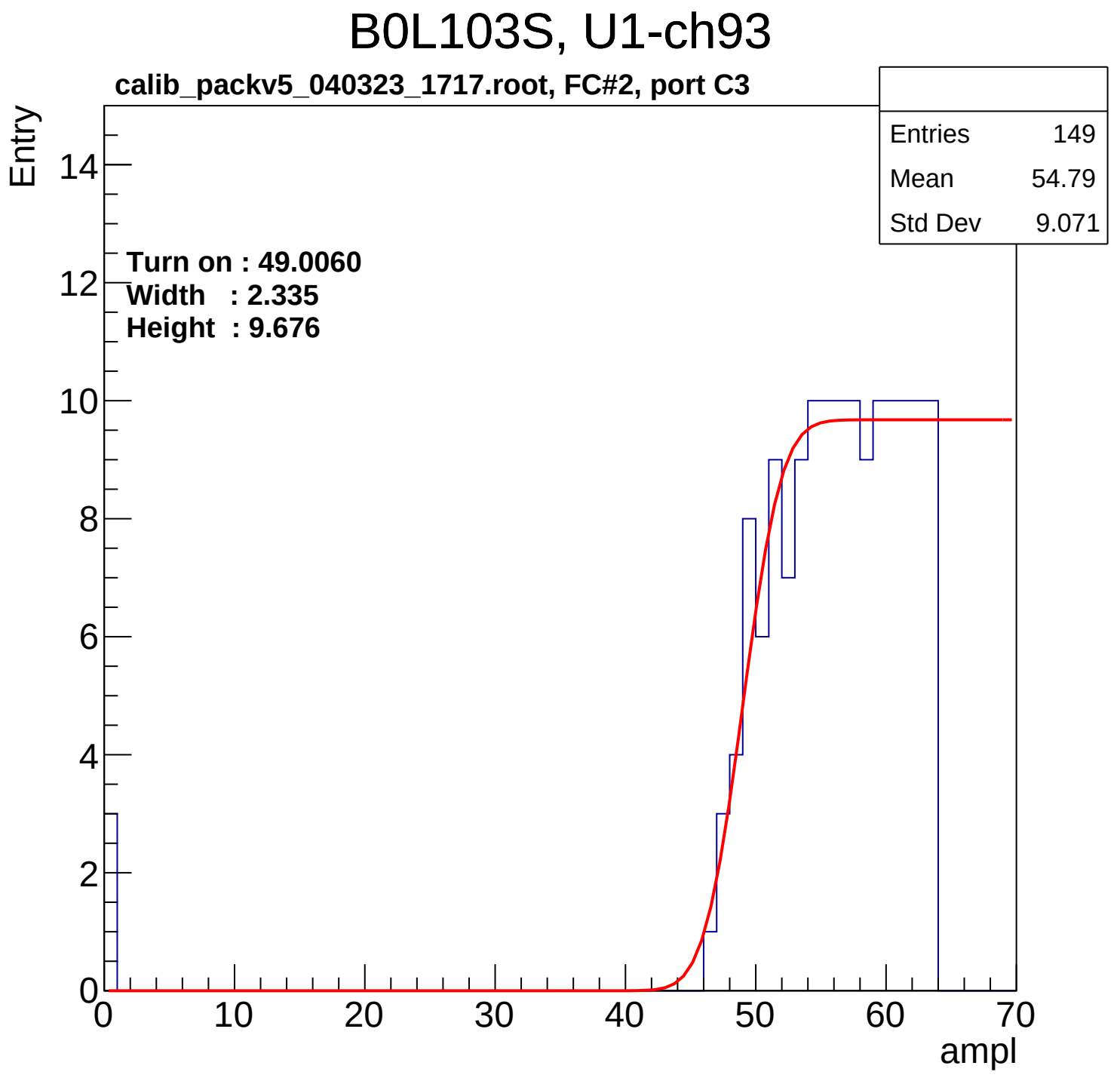
B0L103S, U1-ch93
calib_packv5_040323_1717.root, FC#2, port C3
Entries 149
Mean 54.79
Std Dev 9.071
Turn on : 49.0060
Width : 2.335
Height : 9.676
Entry
ampl
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6
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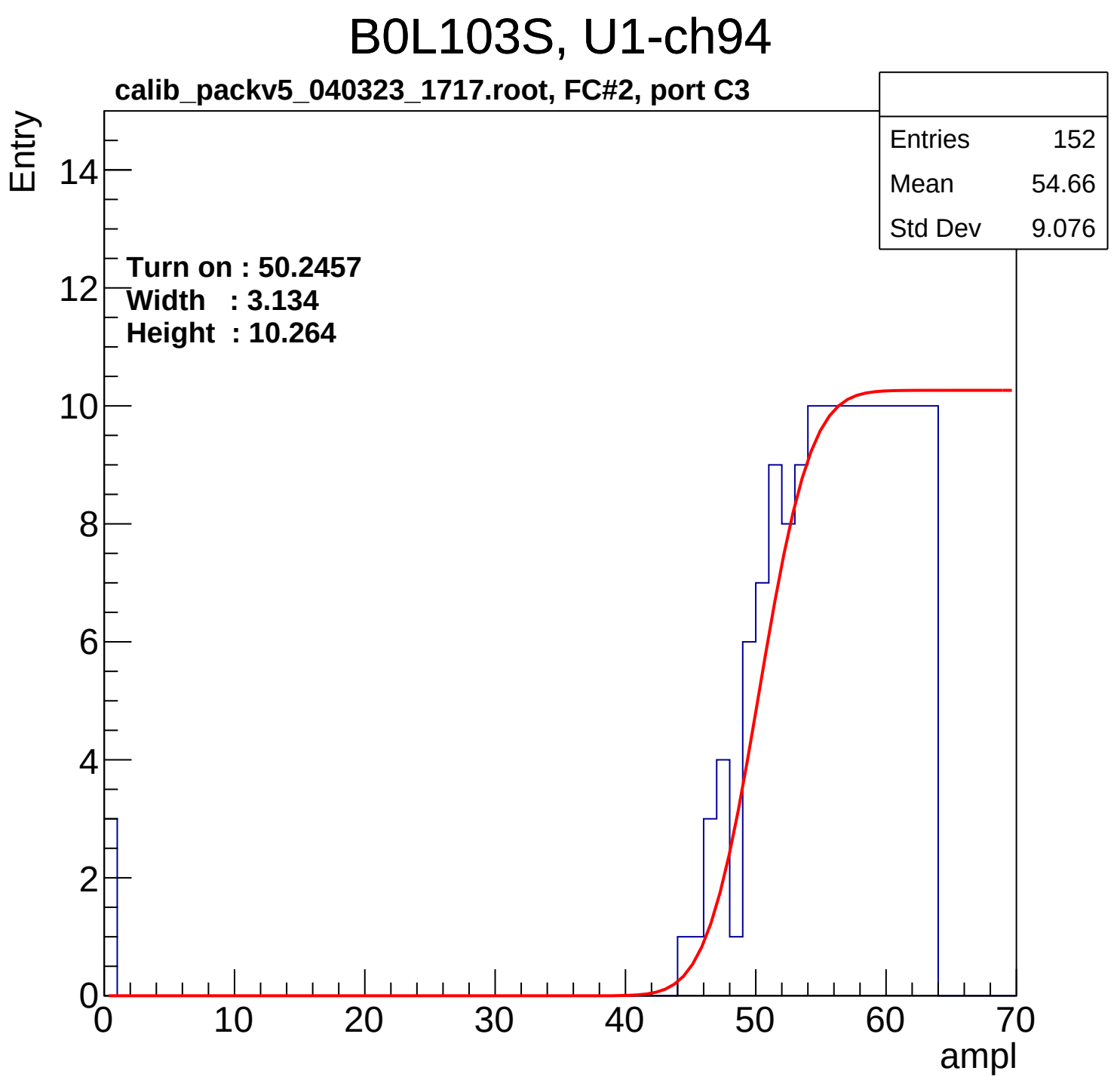
B0L103S, U1-ch94
calib_packv5_040323_1717.root, FC#2, port C3
Entries 152
Mean 54.66
Std Dev 9.076
Turn on : 50.2457
Width : 3.134
Height : 10.264
Entry
ampl
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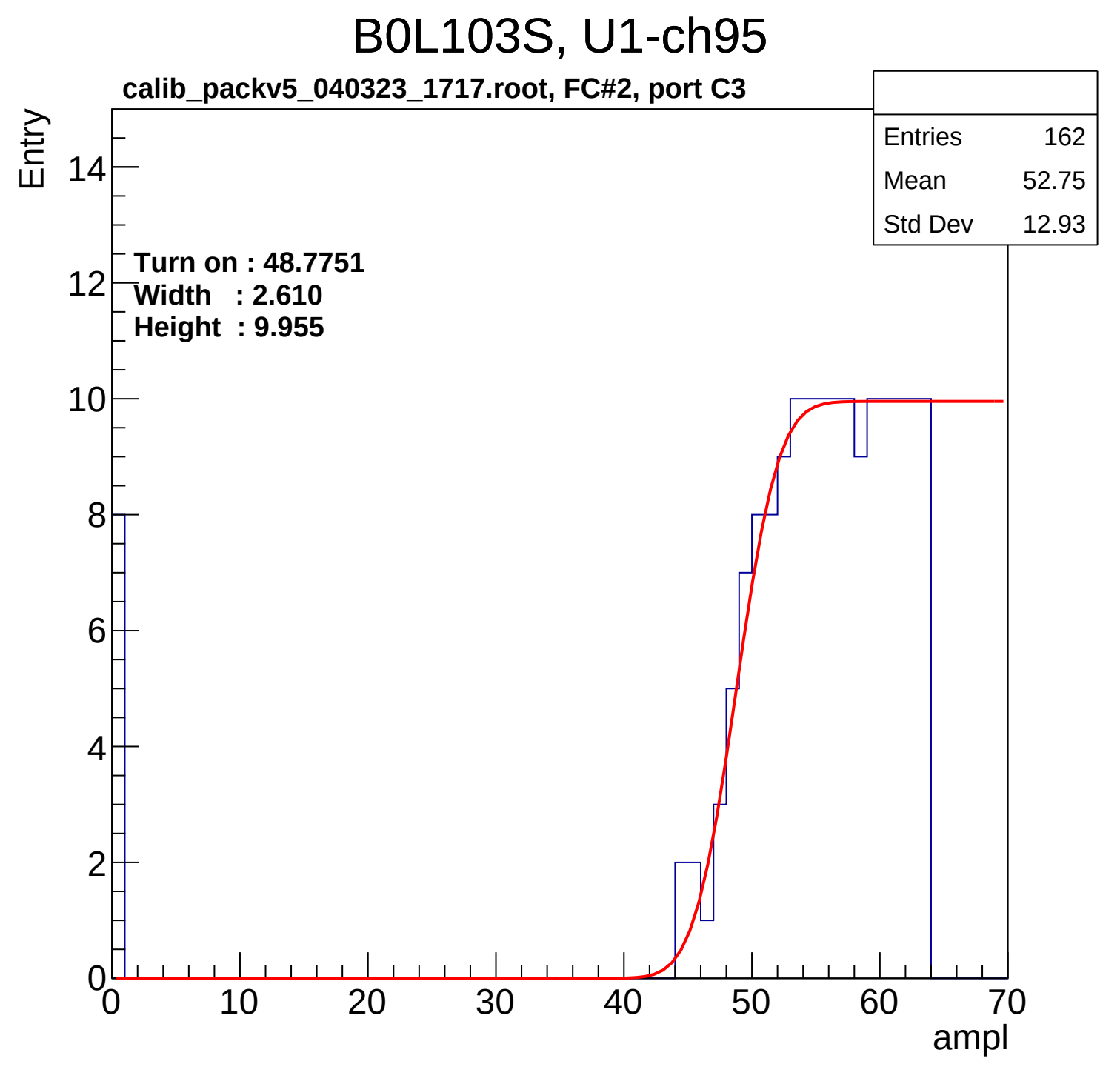
B0L103S, U1-ch95
calib_packv5_040323_1717.root, FC#2, port C3
Entries 162
Mean 52.75
Std Dev 12.93
Turn on : 48.7751
Width : 2.610
Height : 9.955
Entry
ampl
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6
8
10
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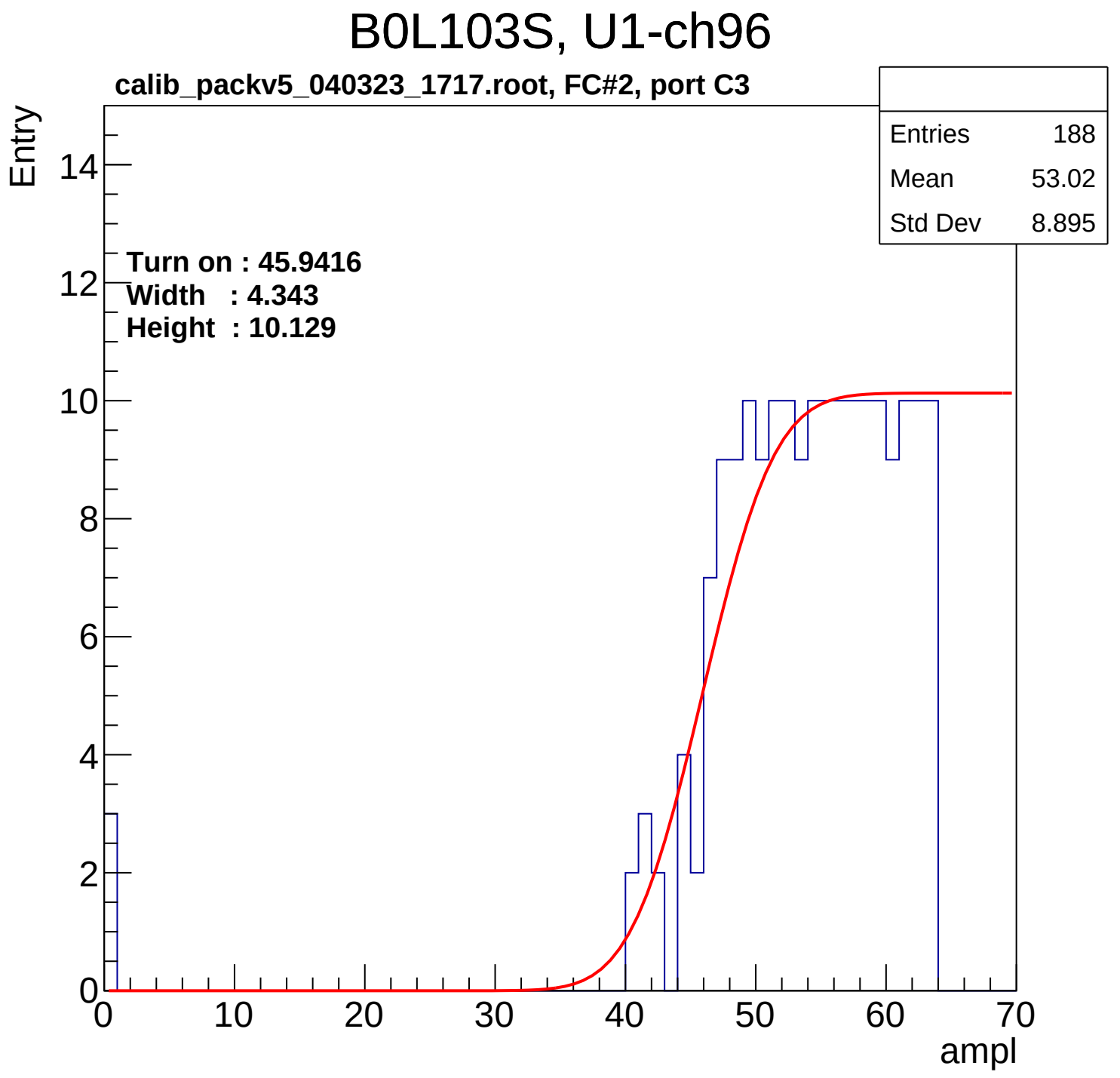
B0L103S, U1-ch96
calib_packv5_040323_1717.root, FC#2, port C3
Entries 188
Mean 53.02
Std Dev 8.895
Turn on : 45.9416
Width : 4.343
Height : 10.129
Entry
ampl
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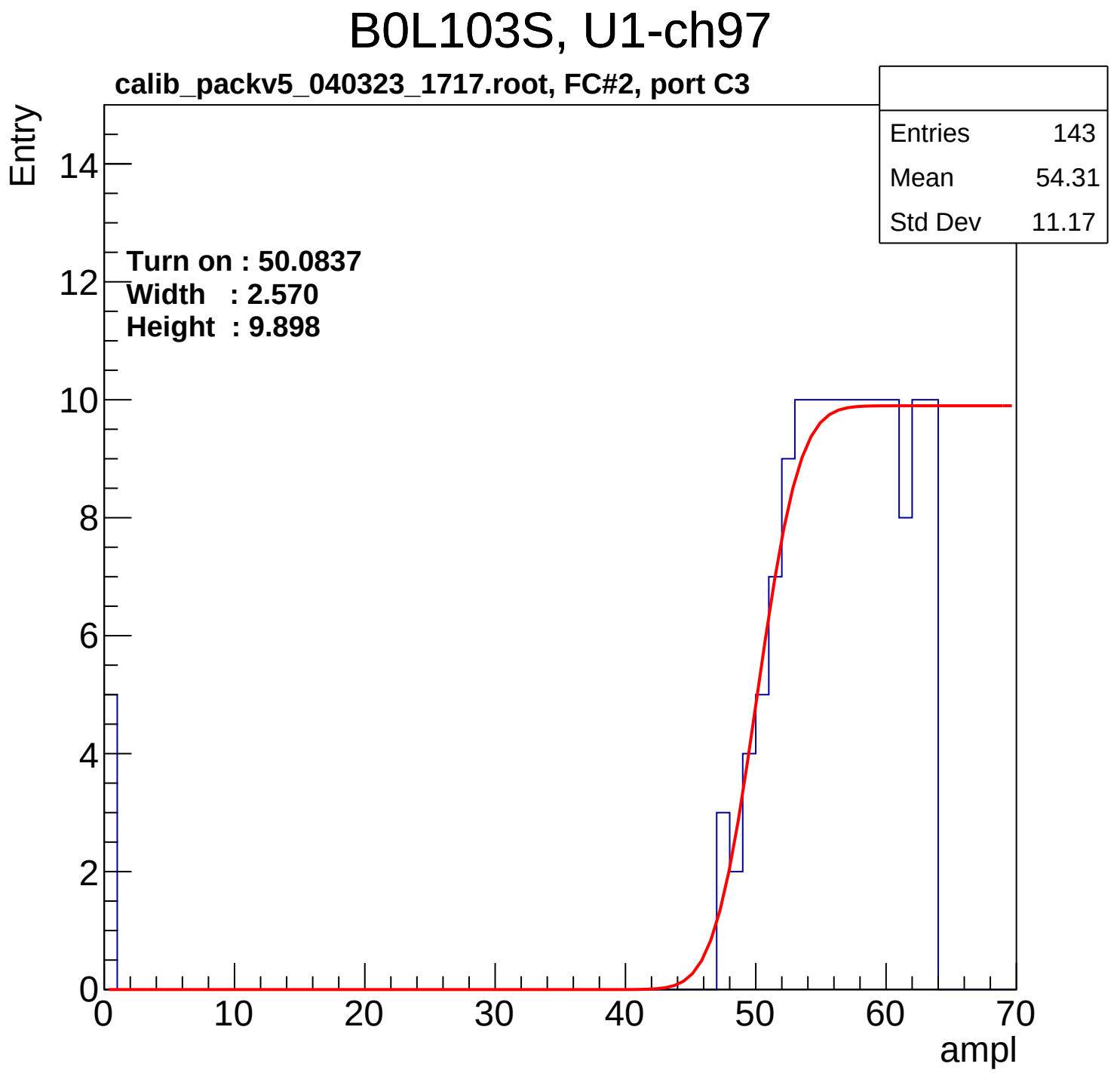
B0L103S, U1-ch97
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 54.31
Std Dev 11.17
Turn on : 50.0837
Width : 2.570
Height : 9.898
Entry
ampl
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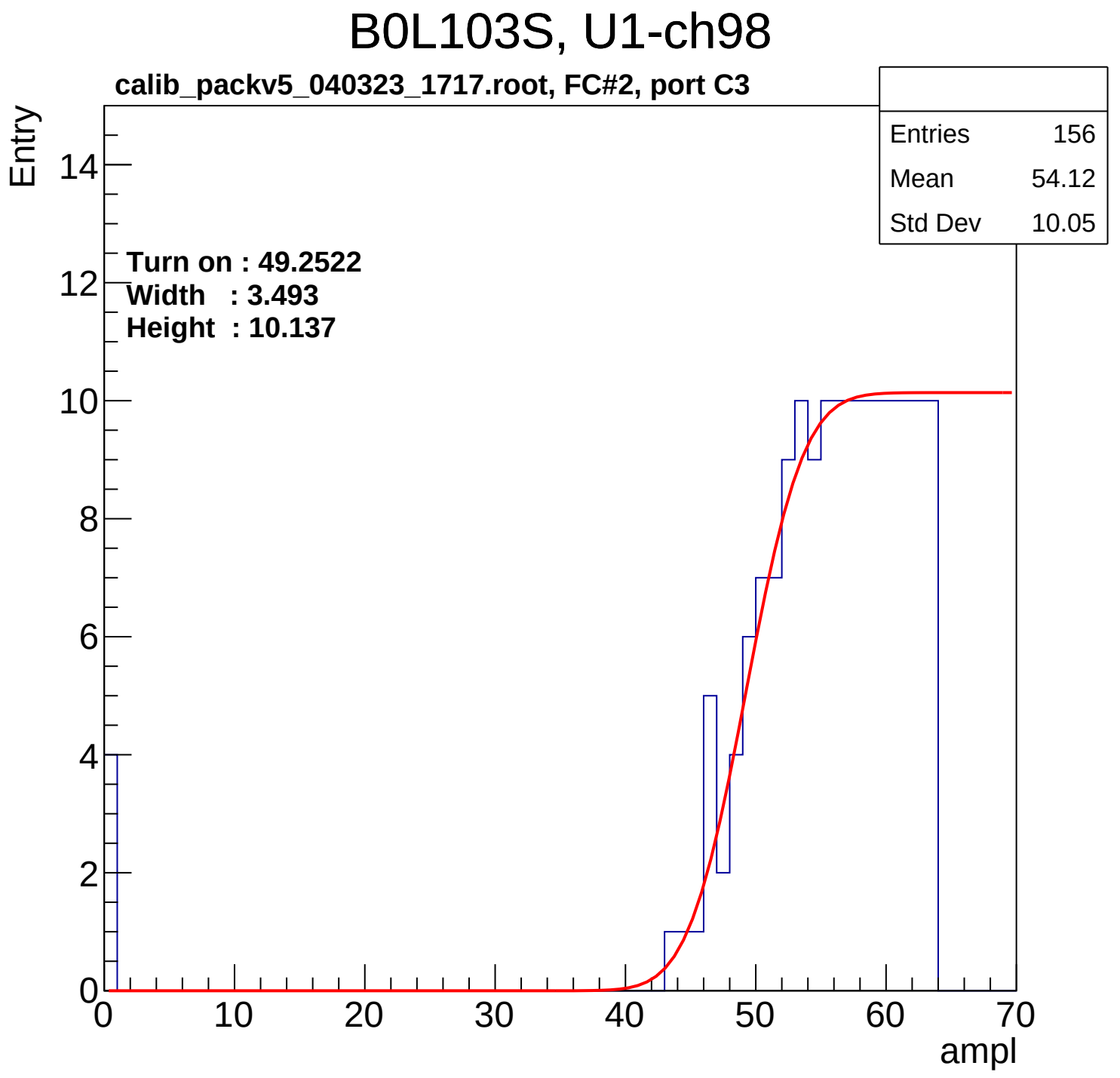
B0L103S, U1-ch98
calib_packv5_040323_1717.root, FC#2, port C3
Entries 156
Mean 54.12
Std Dev 10.05
Turn on : 49.2522
Width : 3.493
Height : 10.137
Entry
ampl
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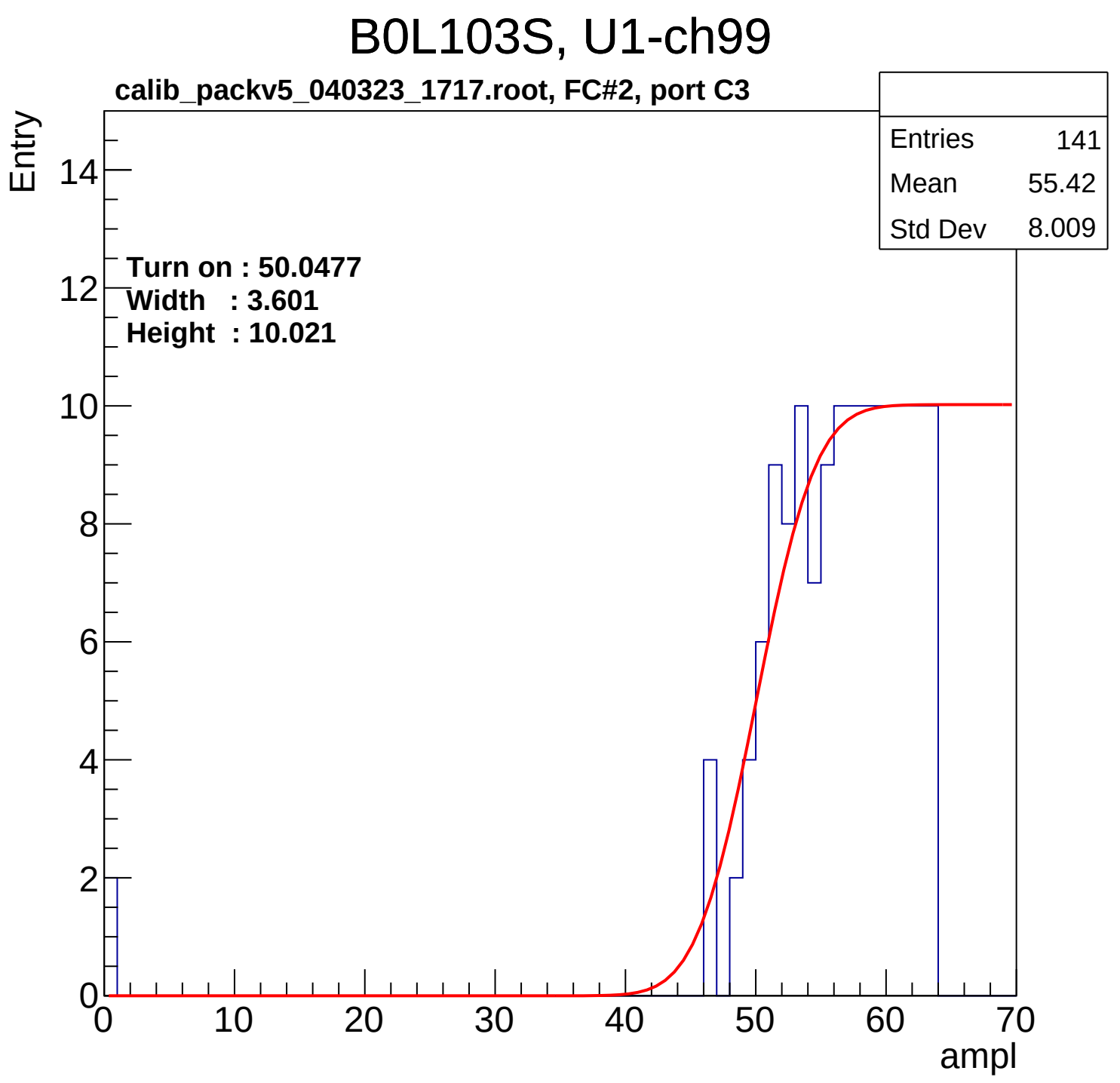
B0L103S, U1-ch99
calib_packv5_040323_1717.root, FC#2, port C3
Entries 141
Mean 55.42
Std Dev 8.009
Turn on : 50.0477
Width : 3.601
Height : 10.021
Entry
ampl
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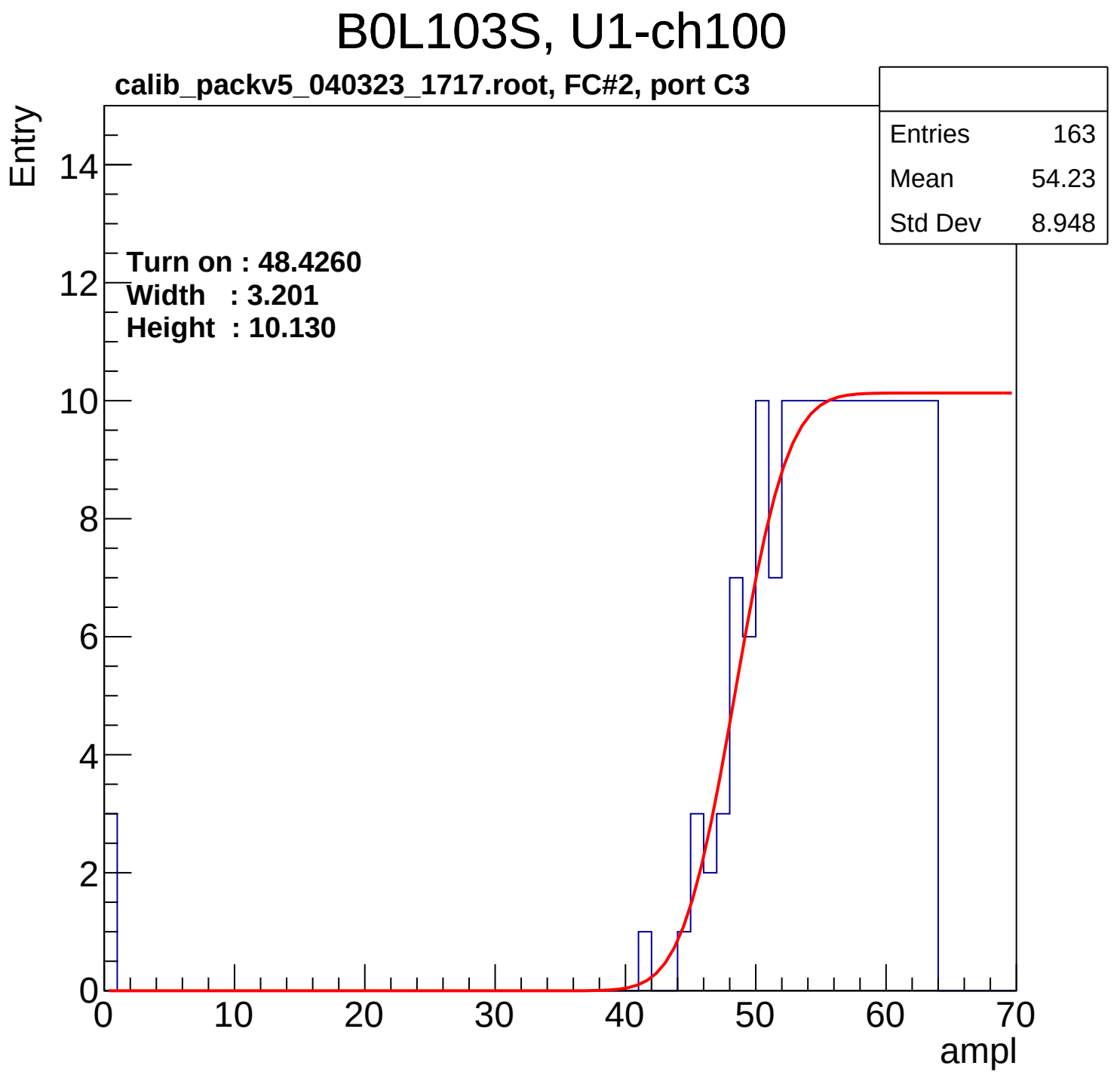
B0L103S, U1-ch100
calib_packv5_040323_1717.root, FC#2, port C3
Entries 163
Mean 54.23
Std Dev 8.948
Turn on : 48.4260
Width : 3.201
Height : 10.130
Entry
ampl
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6
8
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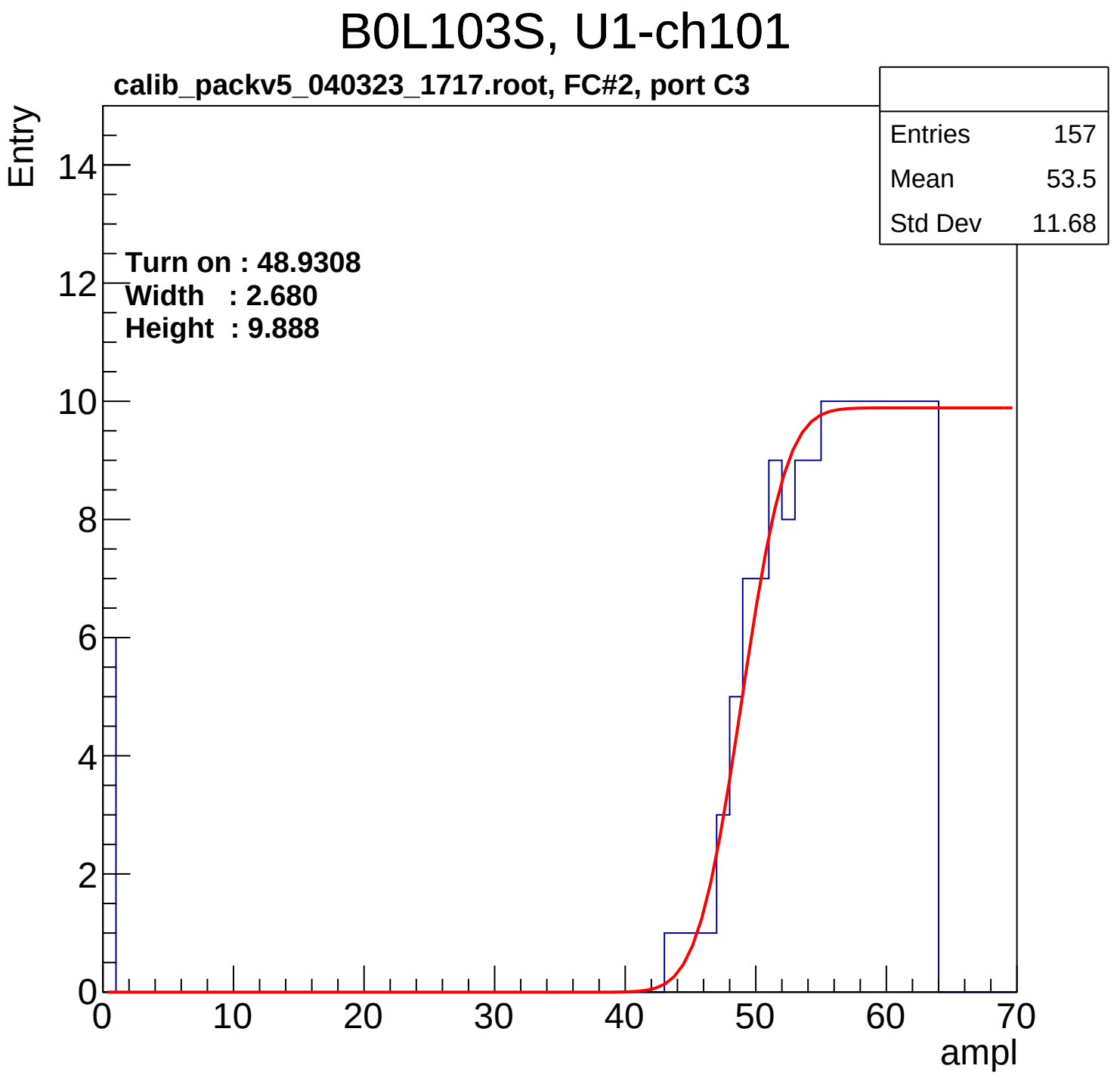
B0L103S, U1-ch101
calib_packv5_040323_1717.root, FC#2, port C3
Entries 157
Mean 53.5
Std Dev 11.68
Turn on : 48.9308
Width : 2.680
Height : 9.888
Entry
ampl
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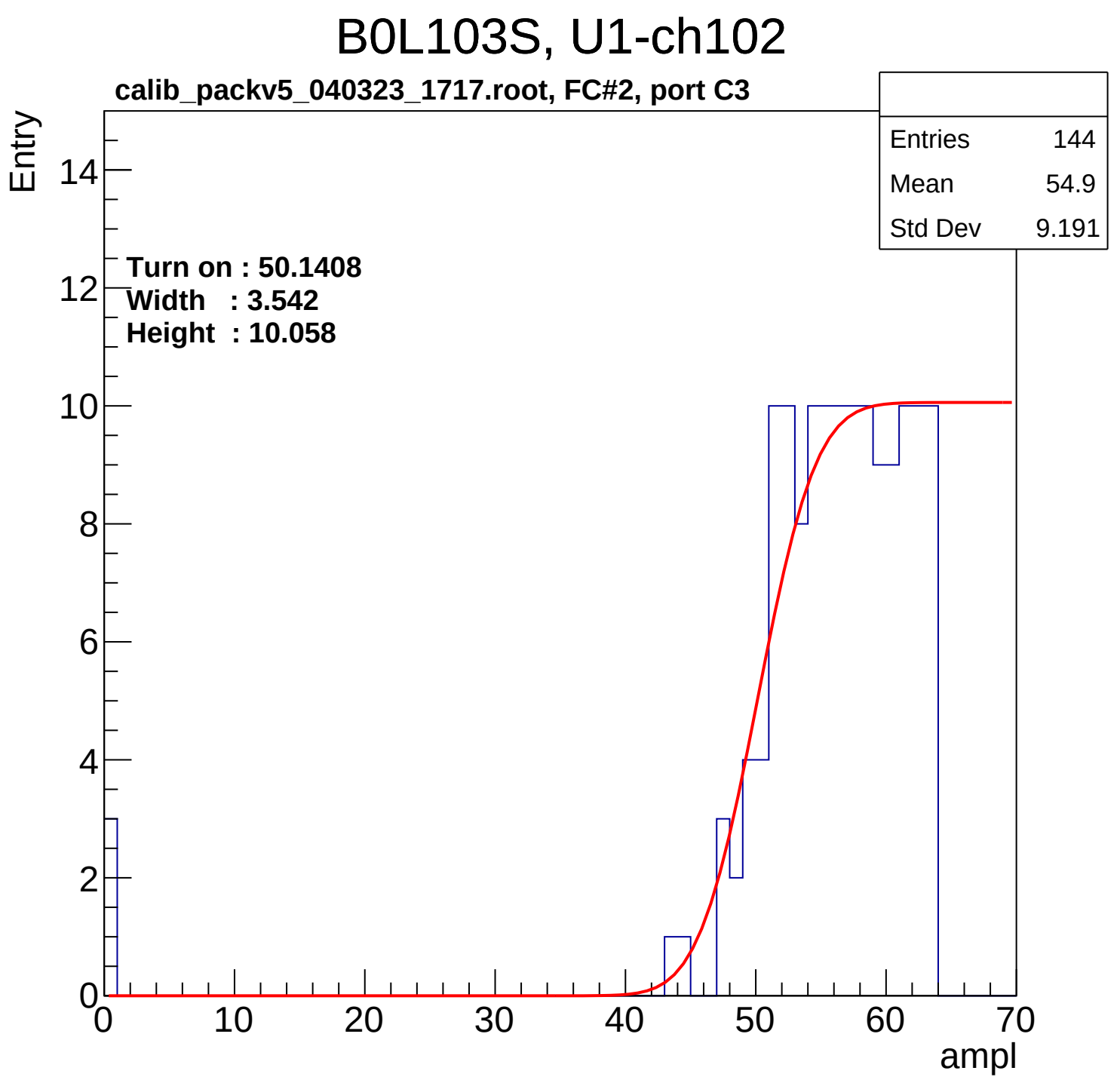
B0L103S, U1-ch102
calib_packv5_040323_1717.root, FC#2, port C3
Entries 144
Mean 54.9
Std Dev 9.191
Turn on : 50.1408
Width : 3.542
Height : 10.058
Entry
ampl
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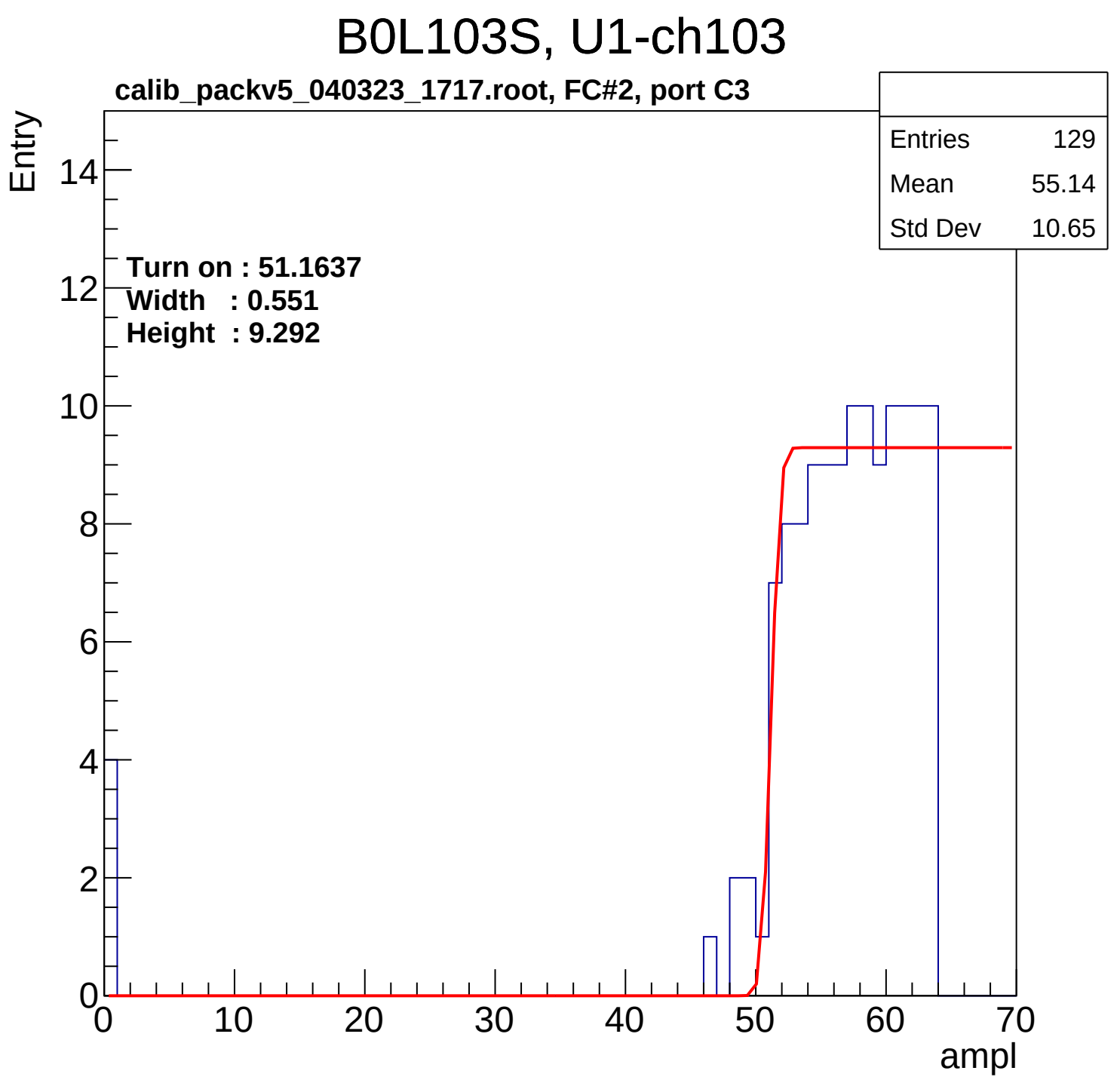
B0L103S, U1-ch103
calib_packv5_040323_1717.root, FC#2, port C3
Entries 129
Mean 55.14
Std Dev 10.65
Turn on : 51.1637
Width : 0.551
Height : 9.292
Entry
ampl
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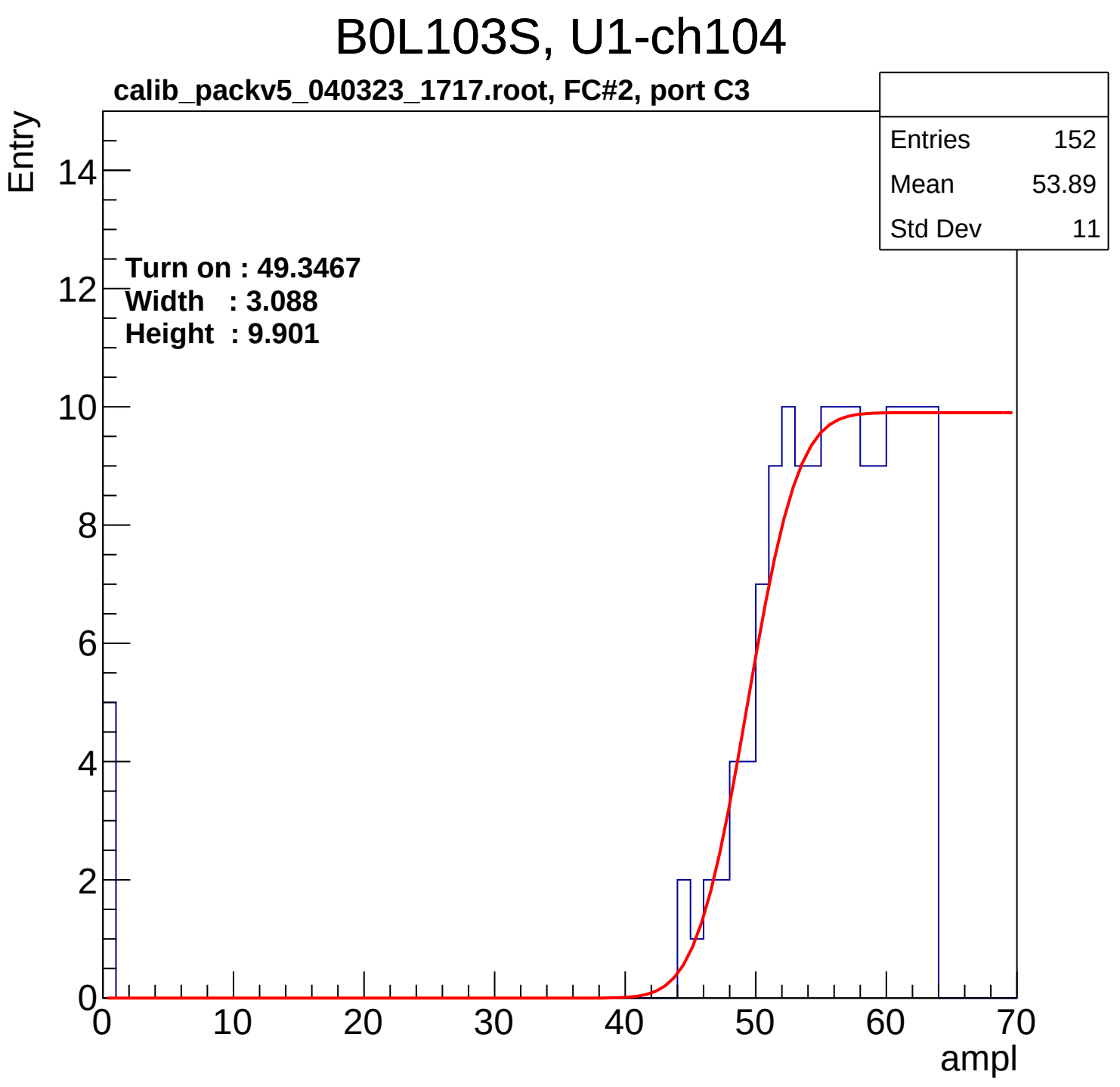
B0L103S, U1-ch104
calib_packv5_040323_1717.root, FC#2, port C3
Entries 152
Mean 53.89
Std Dev 11
Turn on : 49.3467
Width : 3.088
Height : 9.901
Entry
ampl
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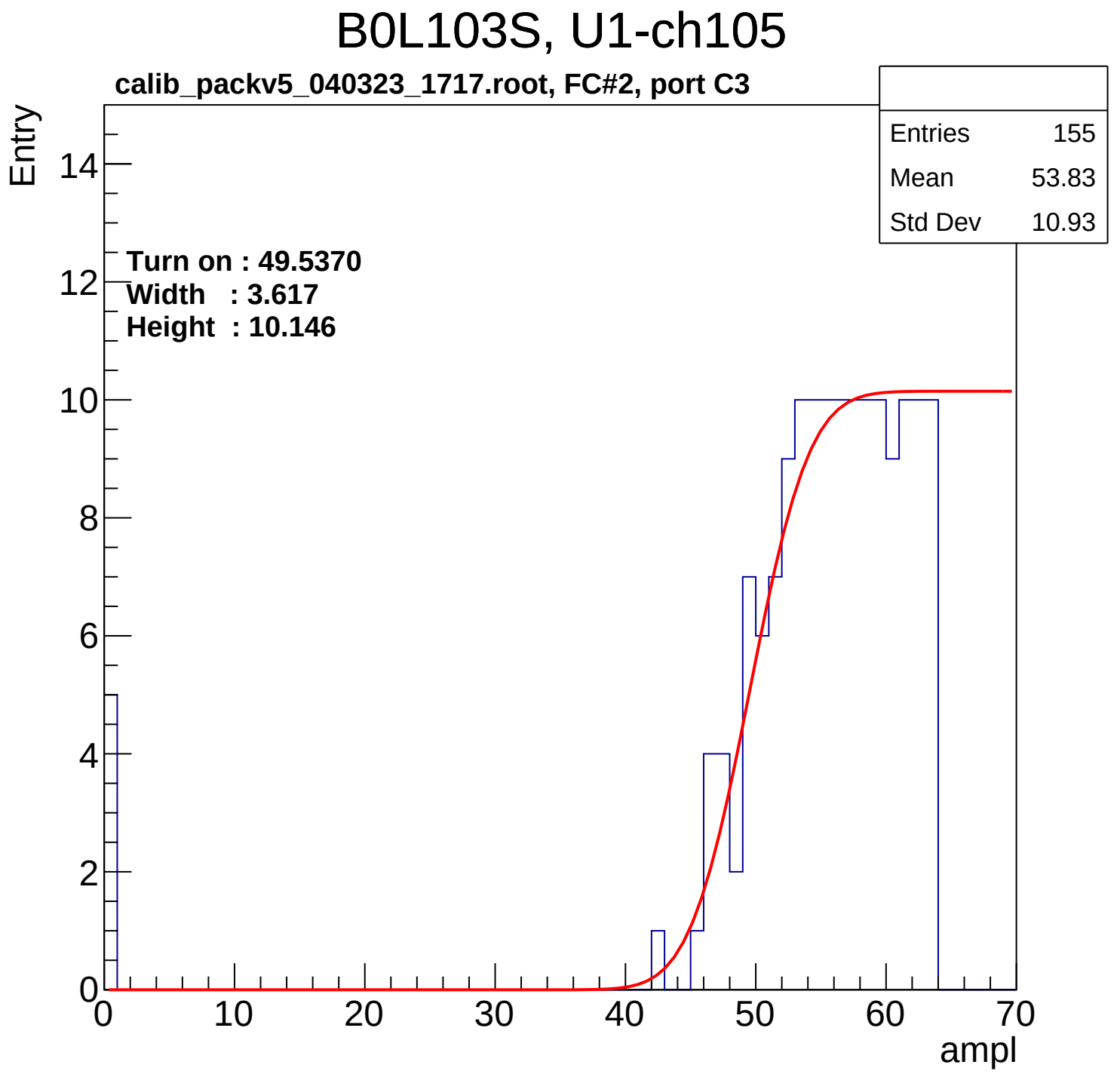
B0L103S, U1-ch105
calib_packv5_040323_1717.root, FC#2, port C3
Entries 155
Mean 53.83
Std Dev 10.93
Turn on : 49.5370
Width : 3.617
Height : 10.146
Entry
ampl
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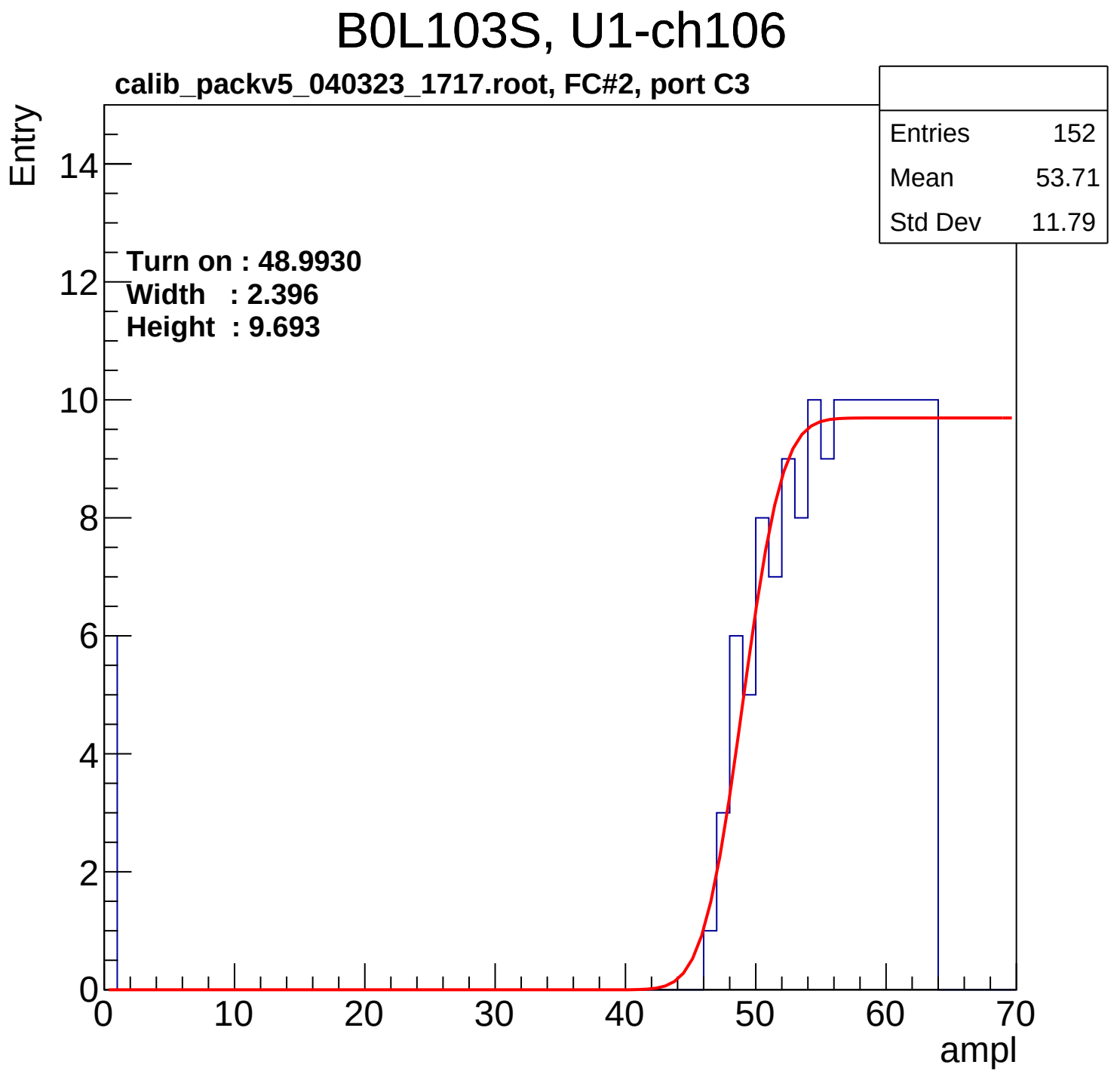
B0L103S, U1-ch106
calib_packv5_040323_1717.root, FC#2, port C3
Entries 152
Mean 53.71
Std Dev 11.79
Turn on : 48.9930
Width : 2.396
Height : 9.693
Entry
ampl
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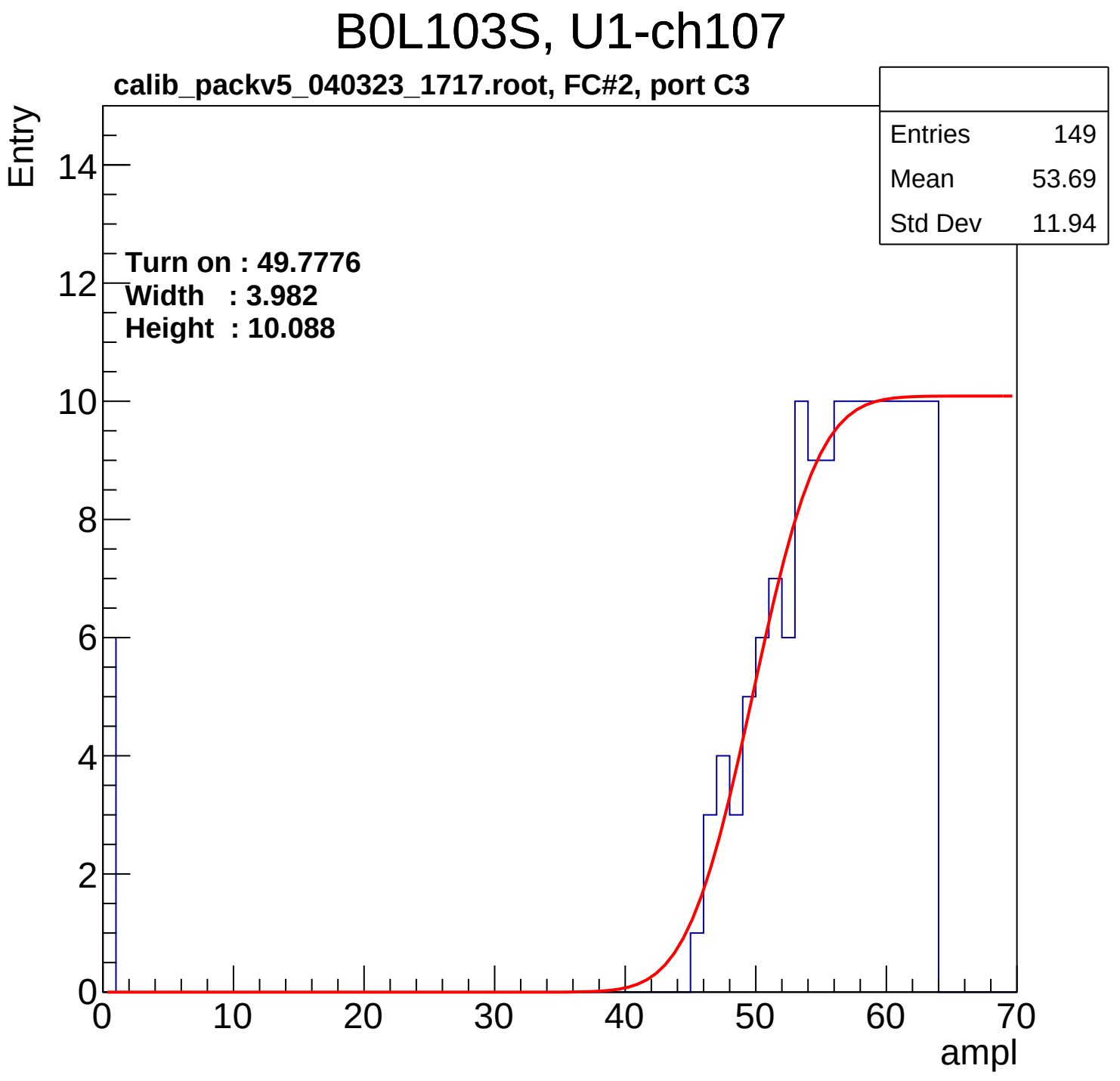
B0L103S, U1-ch107
calib_packv5_040323_1717.root, FC#2, port C3
Entries 149
Mean 53.69
Std Dev 11.94
Turn on : 49.7776
Width : 3.982
Height : 10.088
Entry
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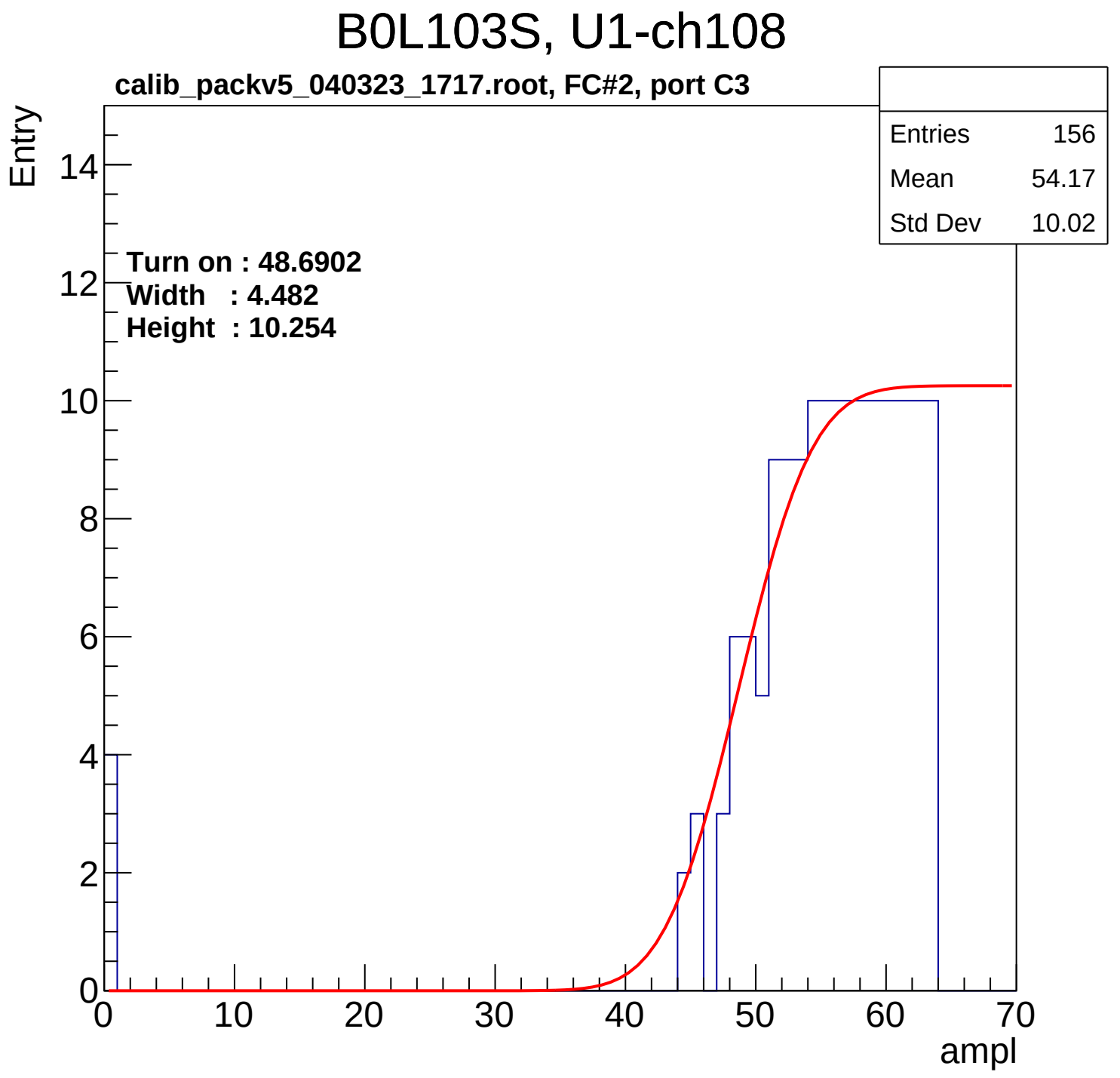
B0L103S, U1-ch108
calib_packv5_040323_1717.root, FC#2, port C3
Entries 156
Mean 54.17
Std Dev 10.02
Turn on : 48.6902
Width : 4.482
Height : 10.254
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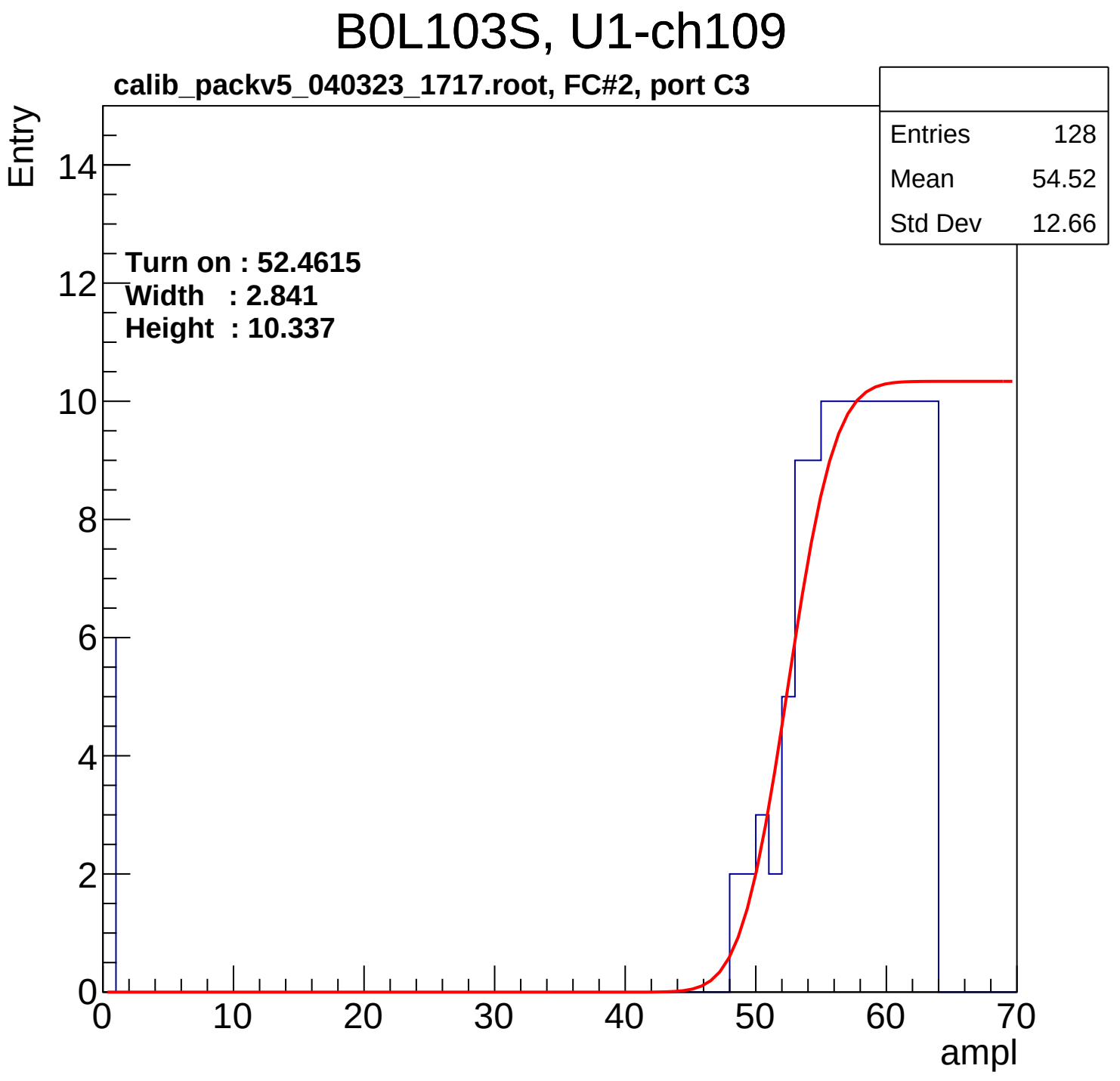
B0L103S, U1-ch109
calib_packv5_040323_1717.root, FC#2, port C3
Entries 128
Mean 54.52
Std Dev 12.66
Turn on : 52.4615
Width : 2.841
Height : 10.337
Entry
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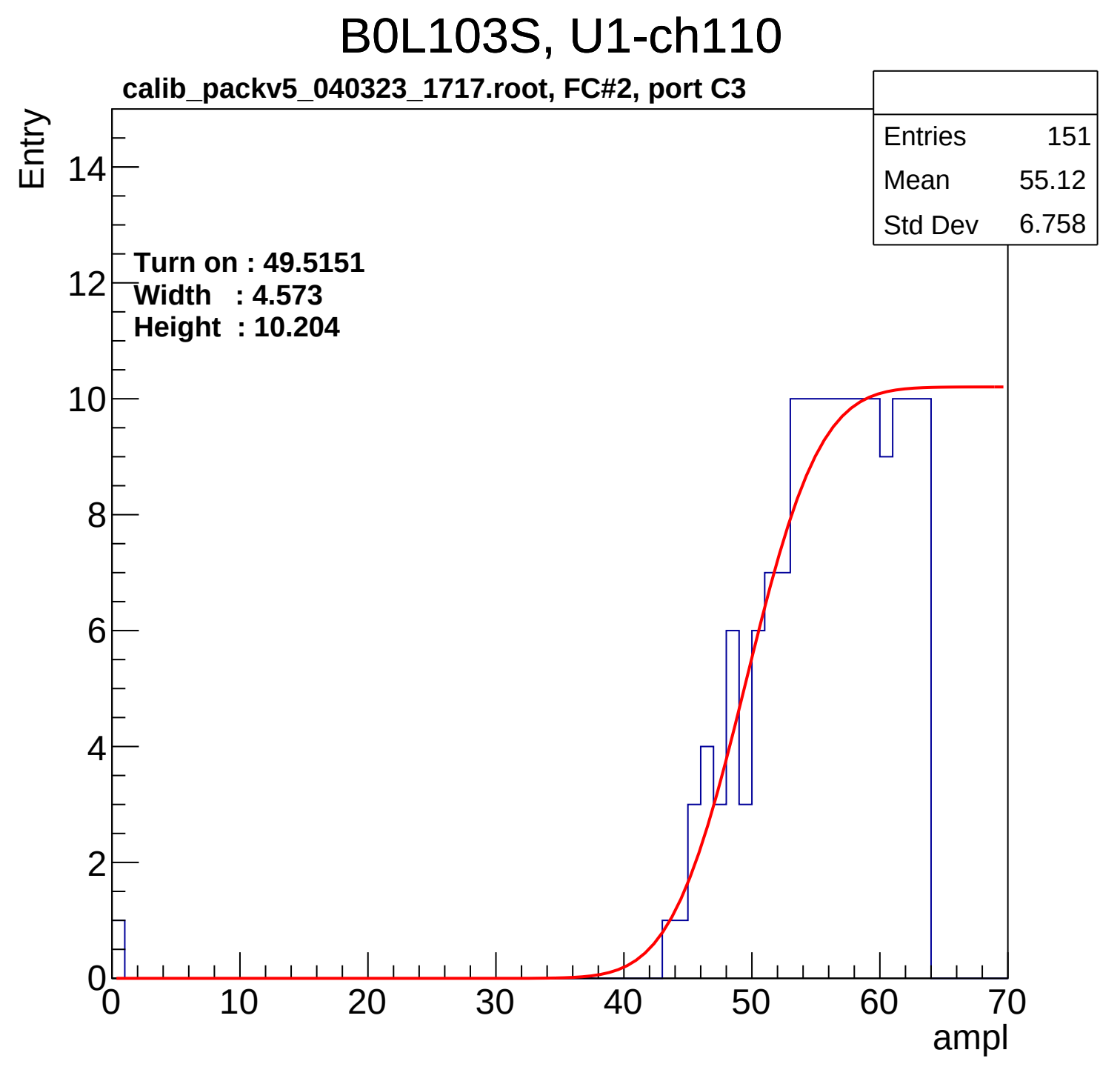
B0L103S, U1-ch110
calib_packv5_040323_1717.root, FC#2, port C3
Entries 151
Mean 55.12
Std Dev 6.758
Turn on : 49.5151
Width : 4.573
Height : 10.204
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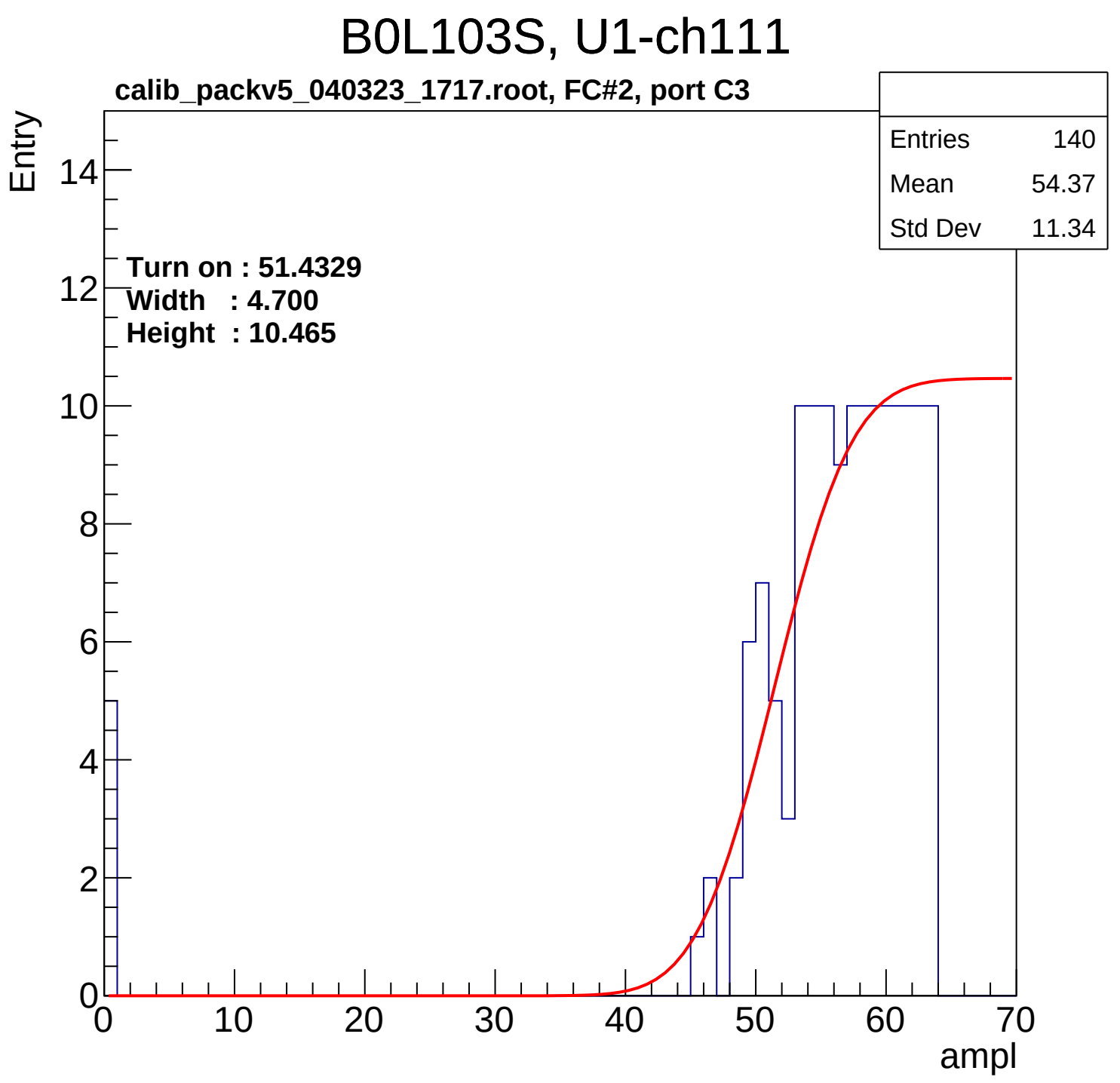
B0L103S, U1-ch111
calib_packv5_040323_1717.root, FC#2, port C3
Entries 140
Mean 54.37
Std Dev 11.34
Turn on : 51.4329
Width : 4.700
Height : 10.465
Entry
ampl
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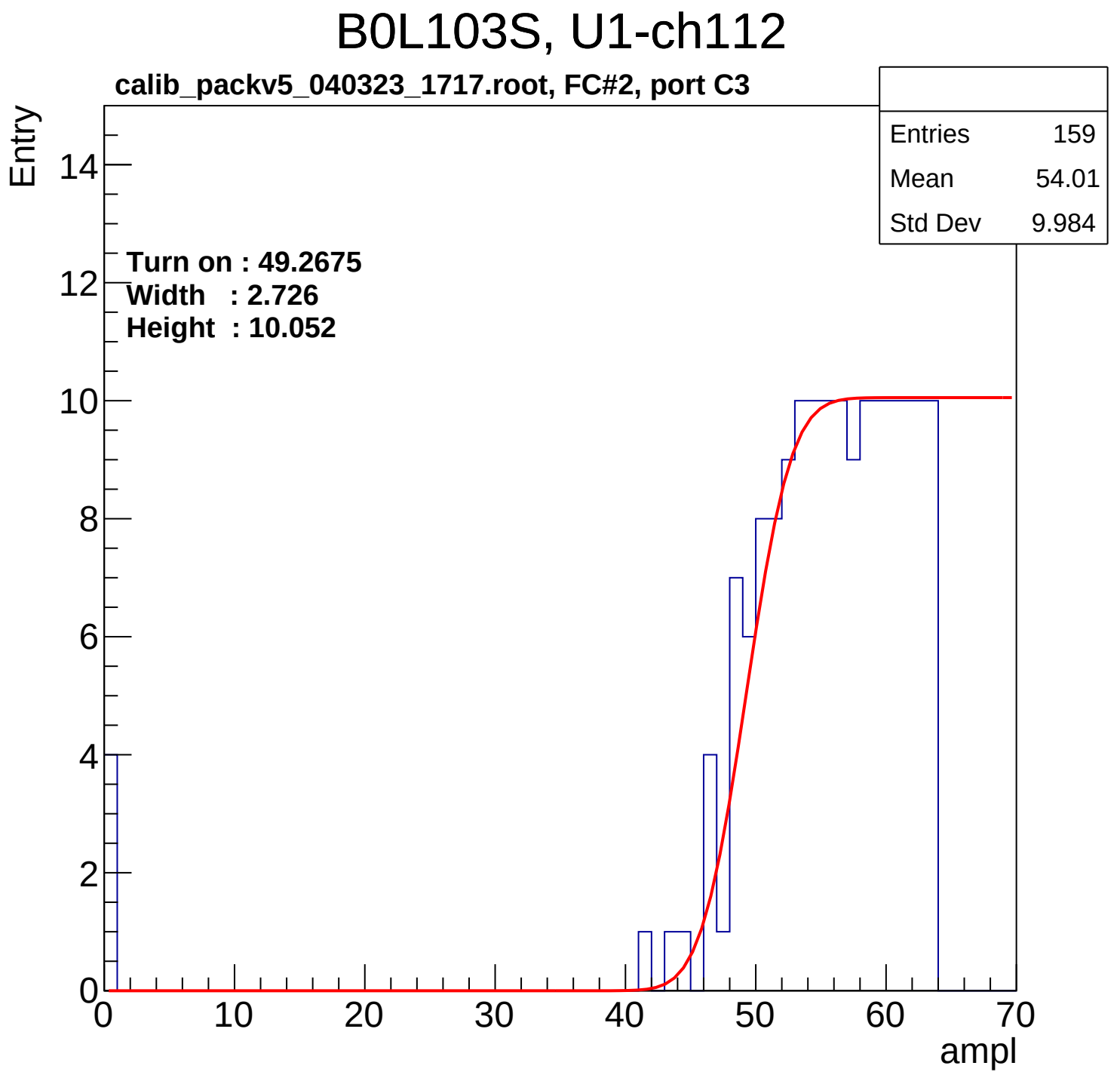
B0L103S, U1-ch112
calib_packv5_040323_1717.root, FC#2, port C3
Entries 159
Mean 54.01
Std Dev 9.984
Turn on : 49.2675
Width : 2.726
Height : 10.052
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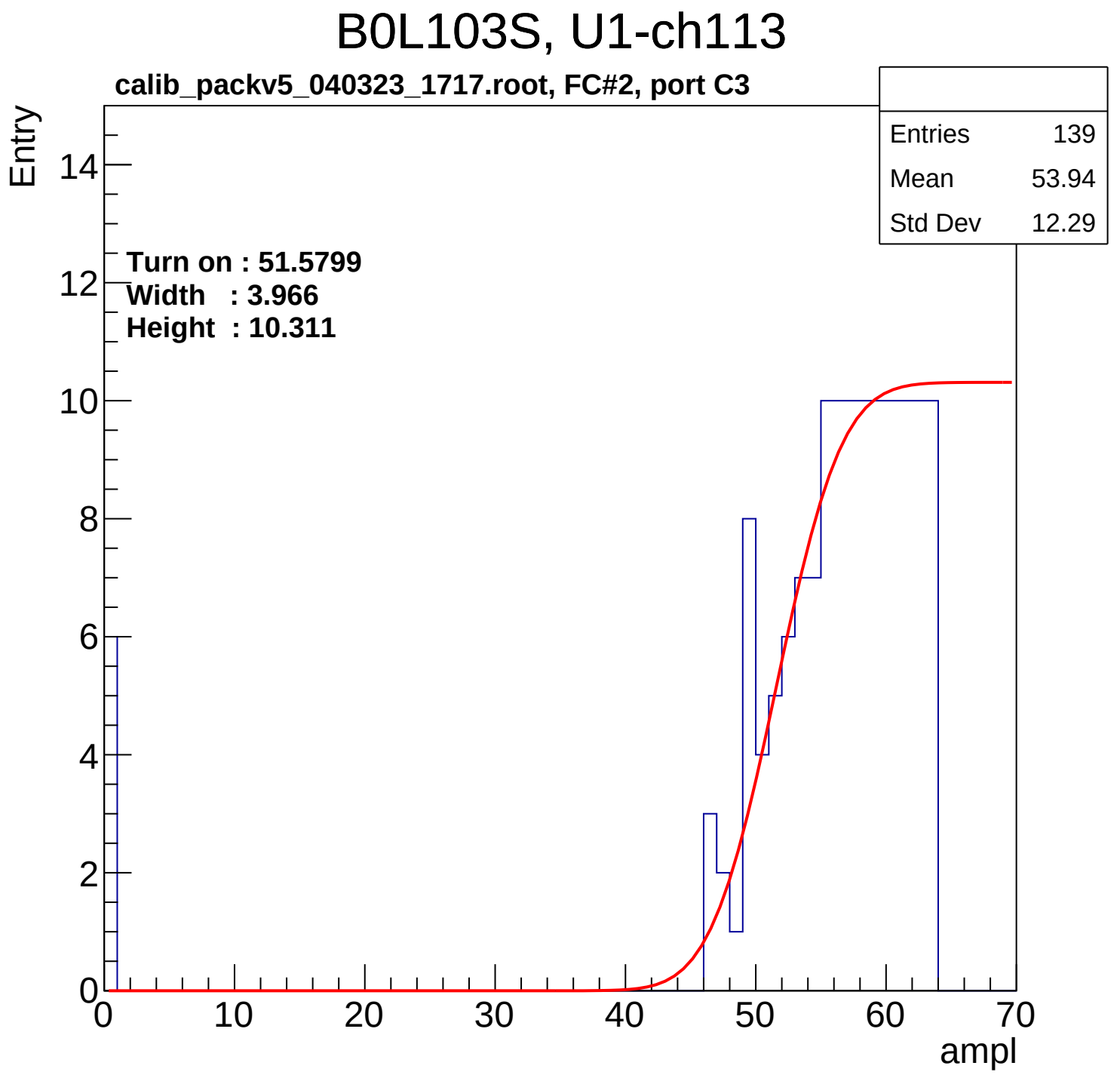
B0L103S, U1-ch113
calib_packv5_040323_1717.root, FC#2, port C3
Entries 139
Mean 53.94
Std Dev 12.29
Turn on : 51.5799
Width : 3.966
Height : 10.311
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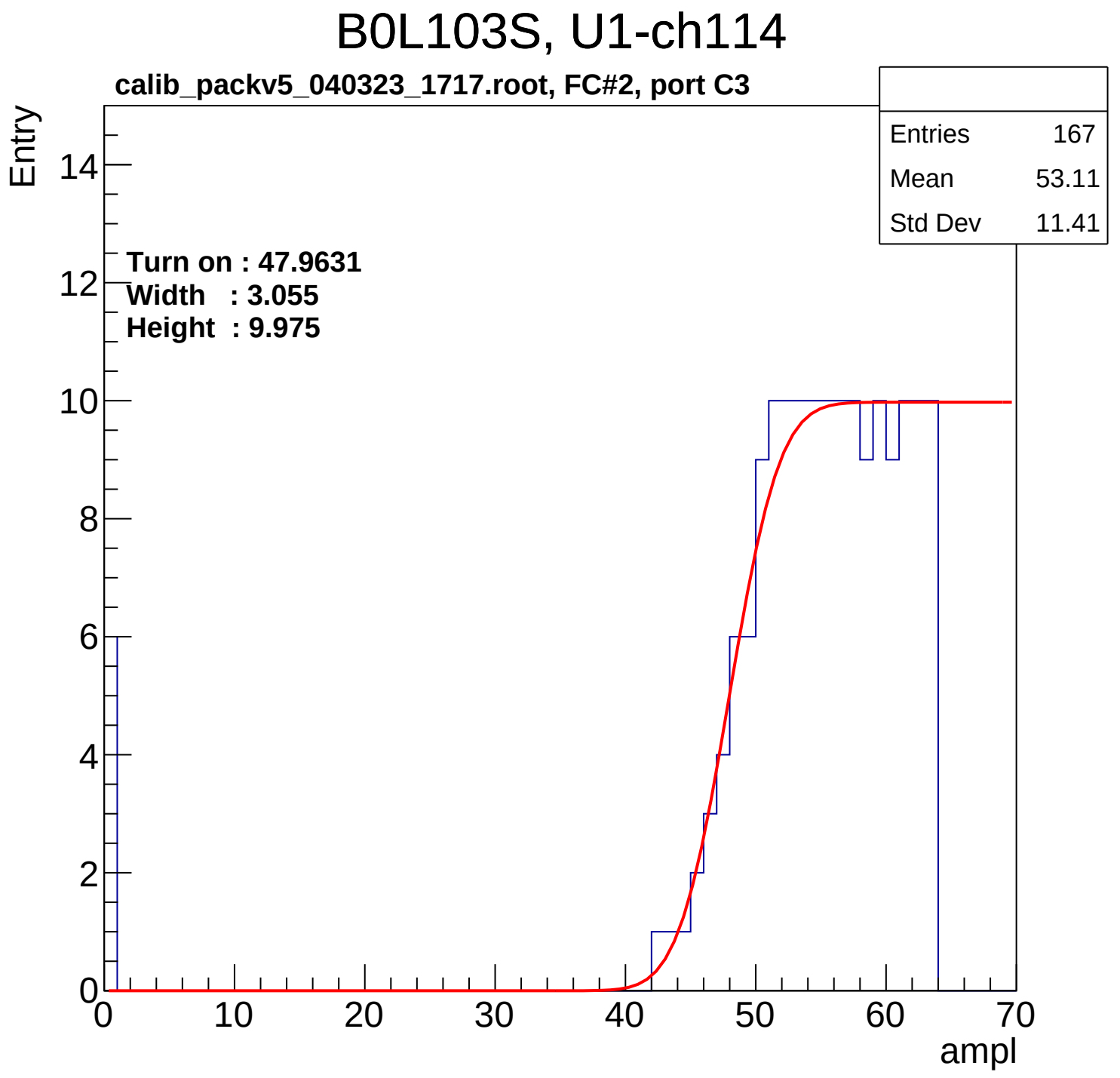
B0L103S, U1-ch114
calib_packv5_040323_1717.root, FC#2, port C3
Entries 167
Mean 53.11
Std Dev 11.41
Turn on : 47.9631
Width : 3.055
Height : 9.975
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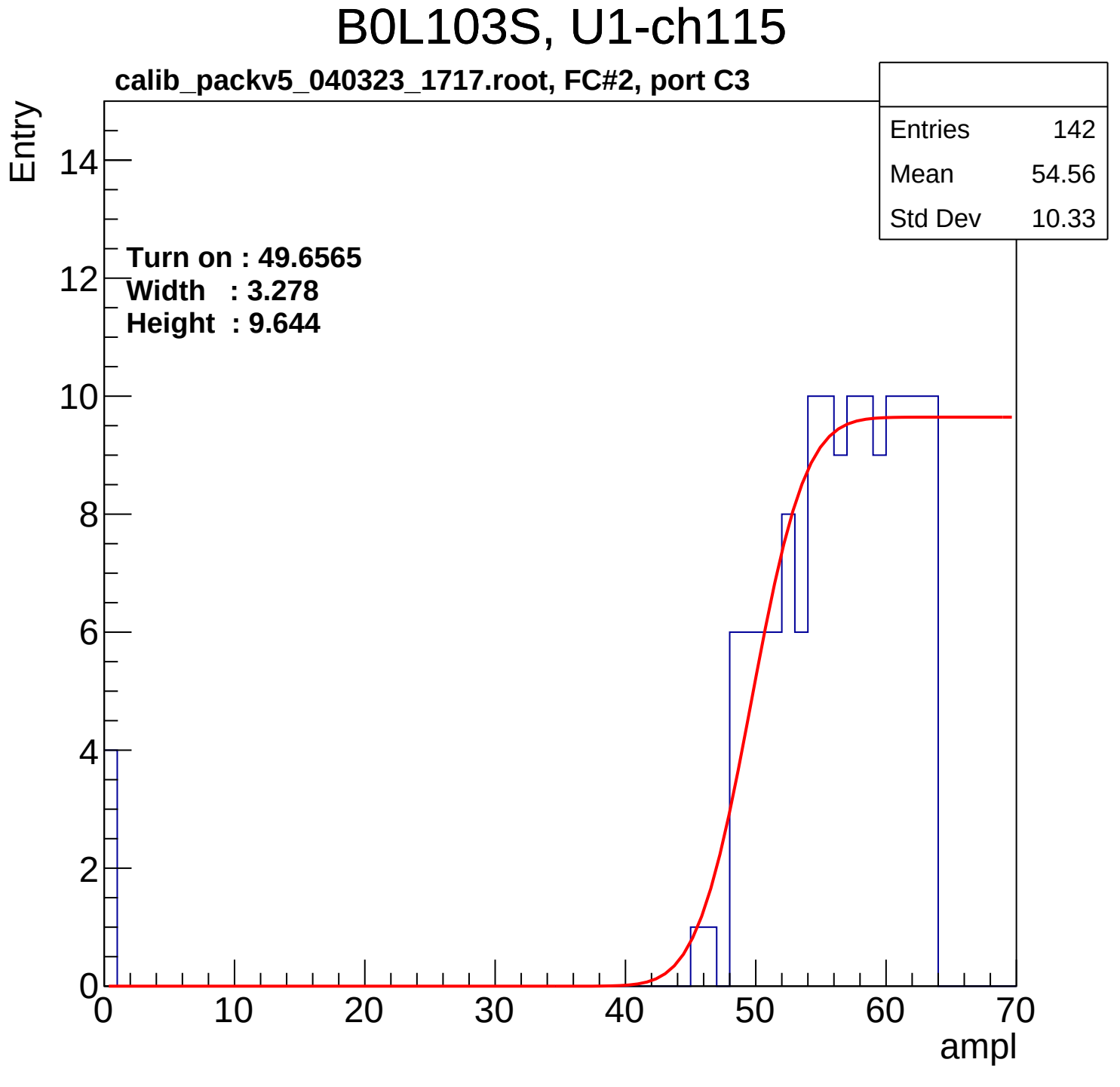
B0L103S, U1-ch115
calib_packv5_040323_1717.root, FC#2, port C3
Entries 142
Mean 54.56
Std Dev 10.33
Turn on : 49.6565
Width : 3.278
Height : 9.644
Entry
ampl
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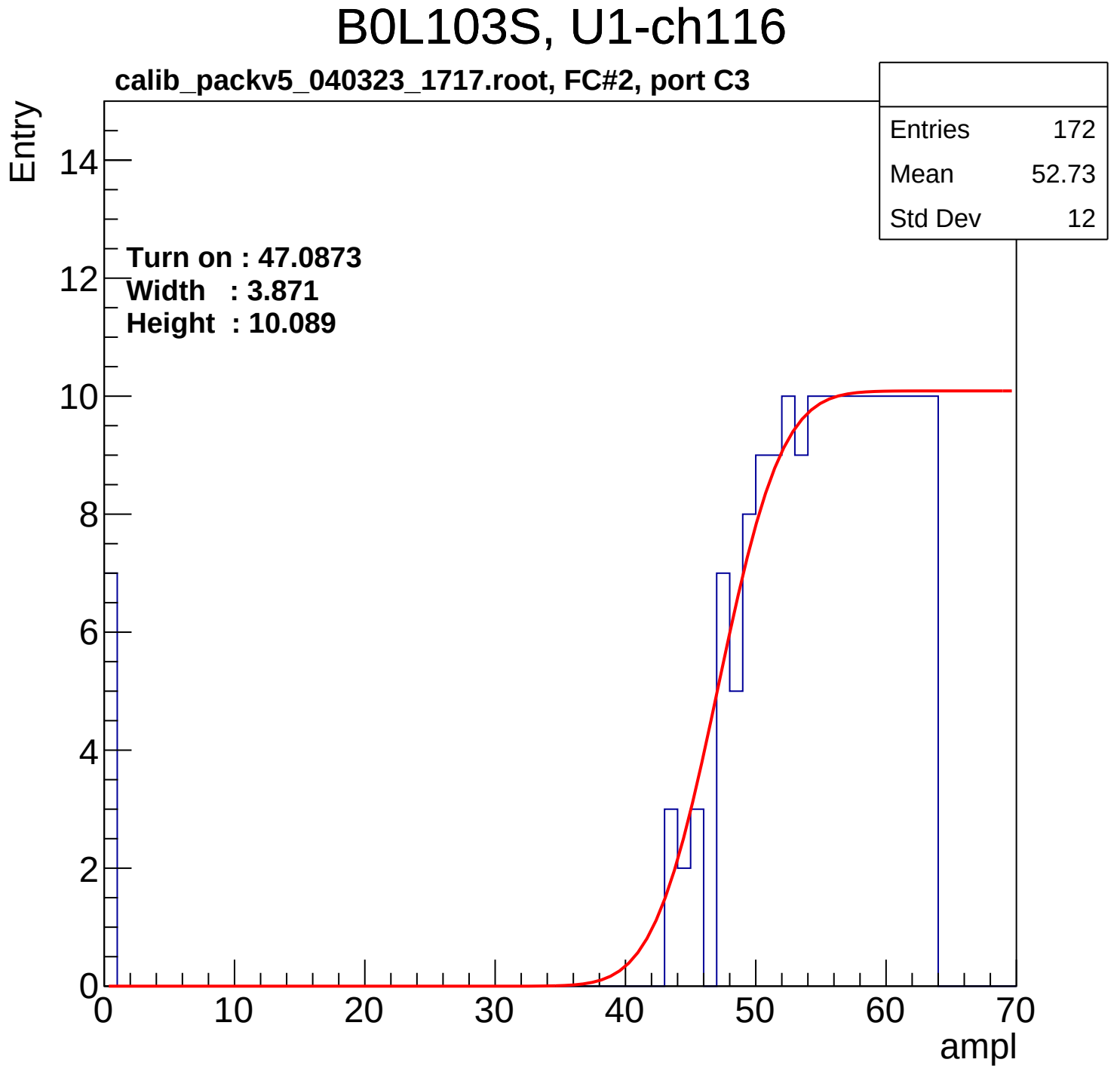
B0L103S, U1-ch116
calib_packv5_040323_1717.root, FC#2, port C3
Entries 172
Mean 52.73
Std Dev 12
Turn on : 47.0873
Width : 3.871
Height : 10.089
Entry
ampl
0
2
4
6
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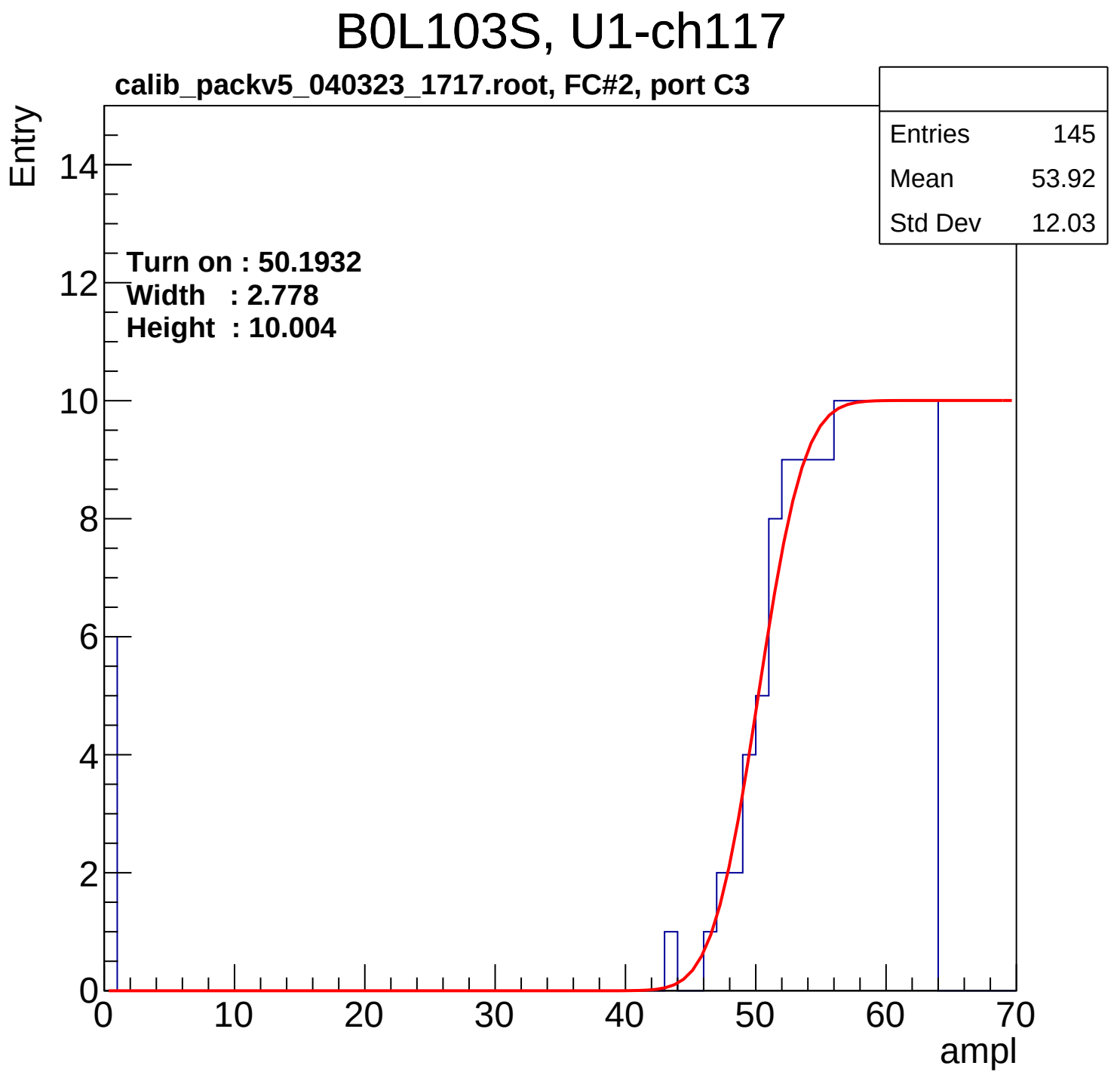
B0L103S, U1-ch117
calib_packv5_040323_1717.root, FC#2, port C3
Entries 145
Mean 53.92
Std Dev 12.03
Turn on : 50.1932
Width : 2.778
Height : 10.004
Entry
ampl
0
2
4
6
8
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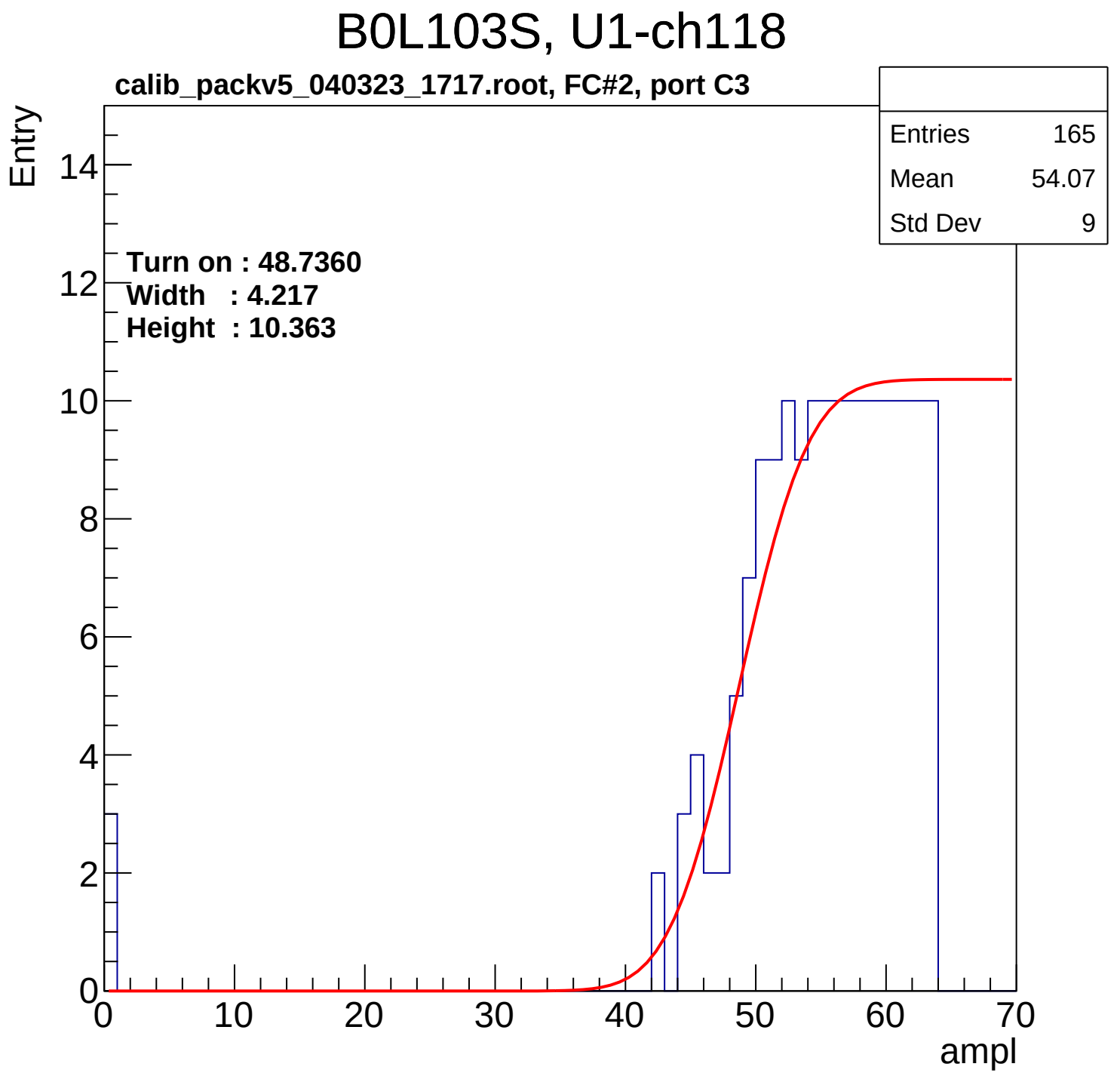
B0L103S, U1-ch118
calib_packv5_040323_1717.root, FC#2, port C3
Entries 165
Mean 54.07
Std Dev 9
Turn on : 48.7360
Width : 4.217
Height : 10.363
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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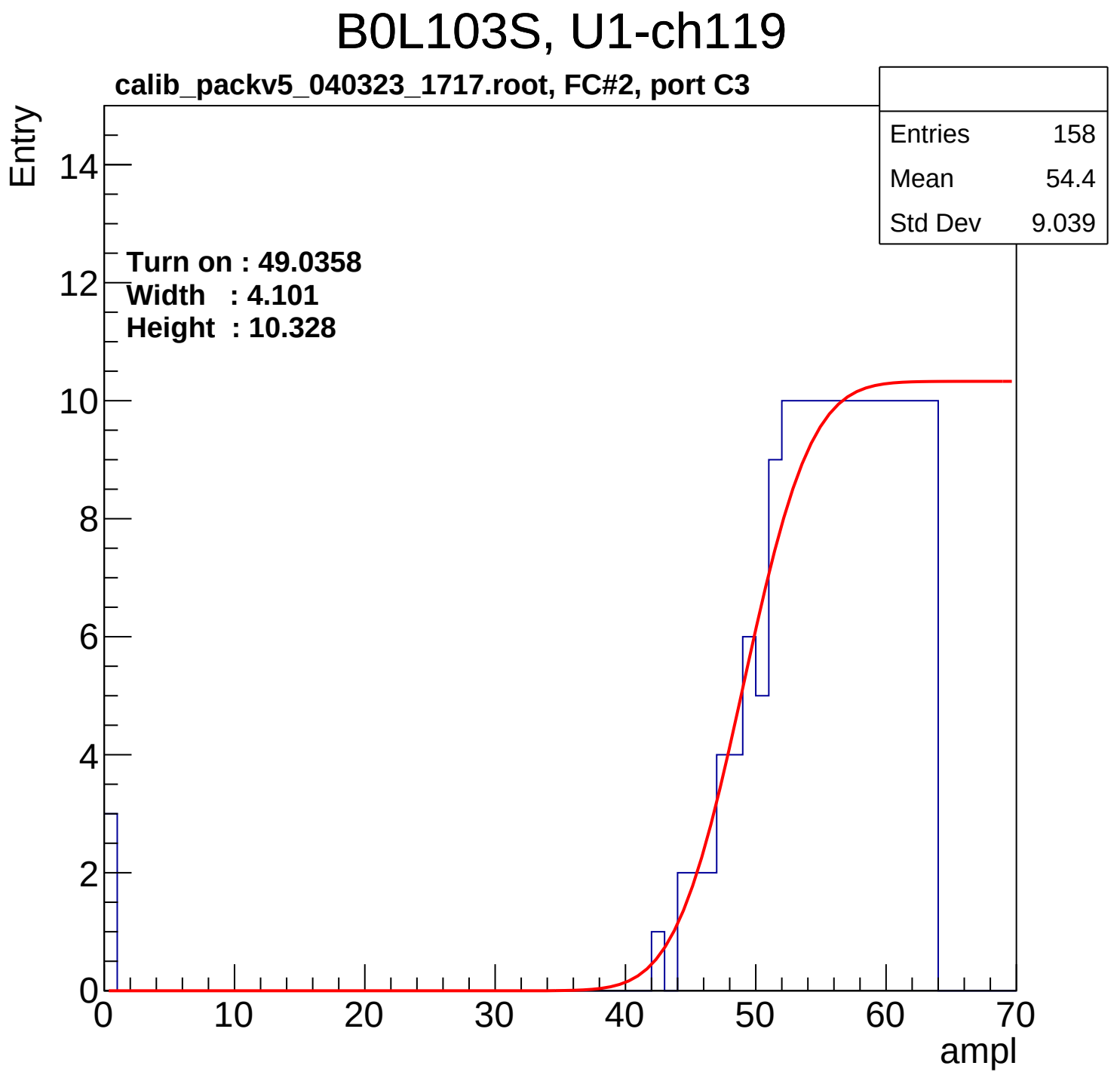
B0L103S, U1-ch119
calib_packv5_040323_1717.root, FC#2, port C3
Entries 158
Mean 54.4
Std Dev 9.039
Turn on : 49.0358
Width : 4.101
Height : 10.328
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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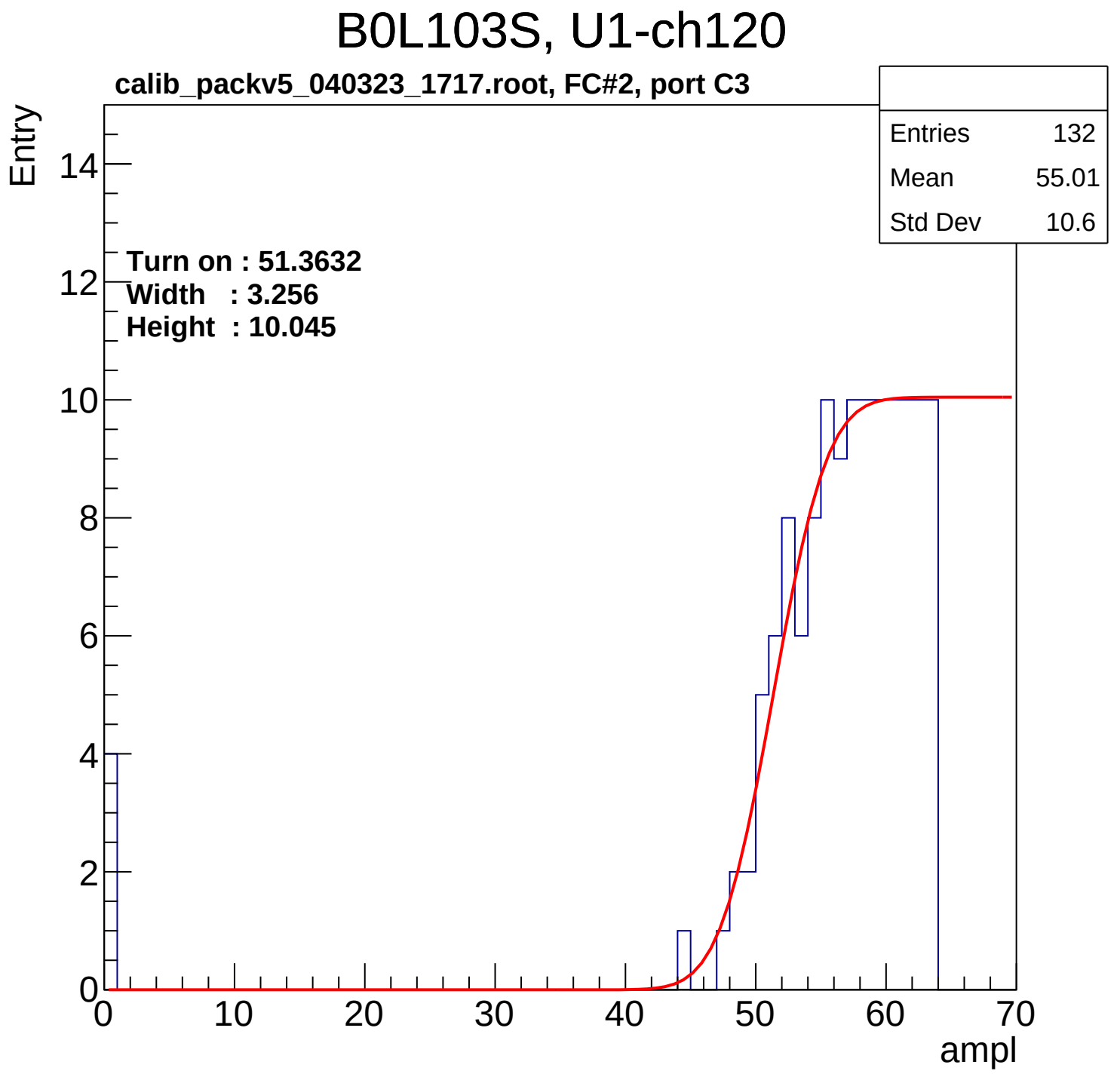
B0L103S, U1-ch120
calib_packv5_040323_1717.root, FC#2, port C3
Entries 132
Mean 55.01
Std Dev 10.6
Turn on : 51.3632
Width : 3.256
Height : 10.045
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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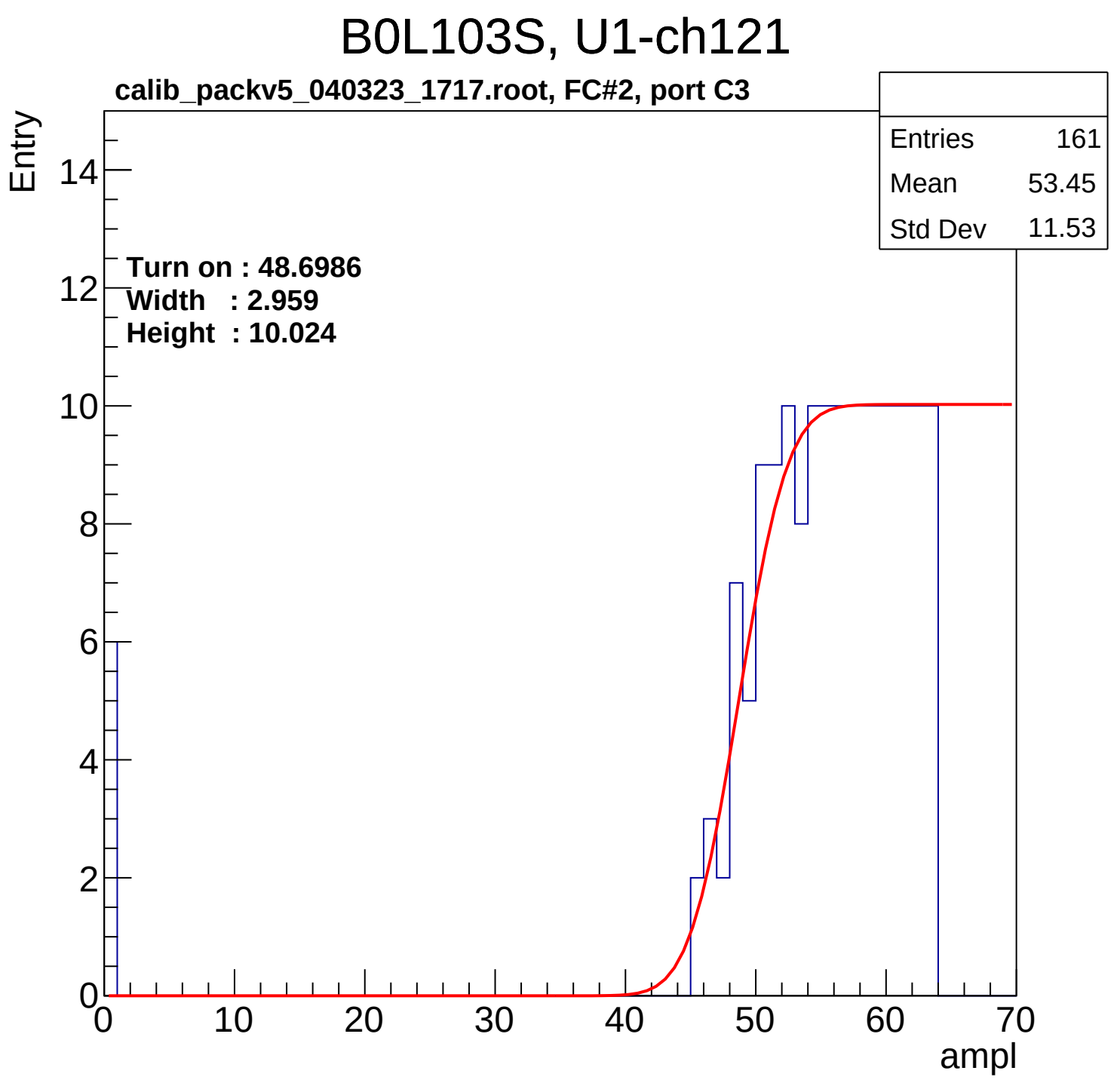
B0L103S, U1-ch121
calib_packv5_040323_1717.root, FC#2, port C3
Entries 161
Mean 53.45
Std Dev 11.53
Turn on : 48.6986
Width : 2.959
Height : 10.024
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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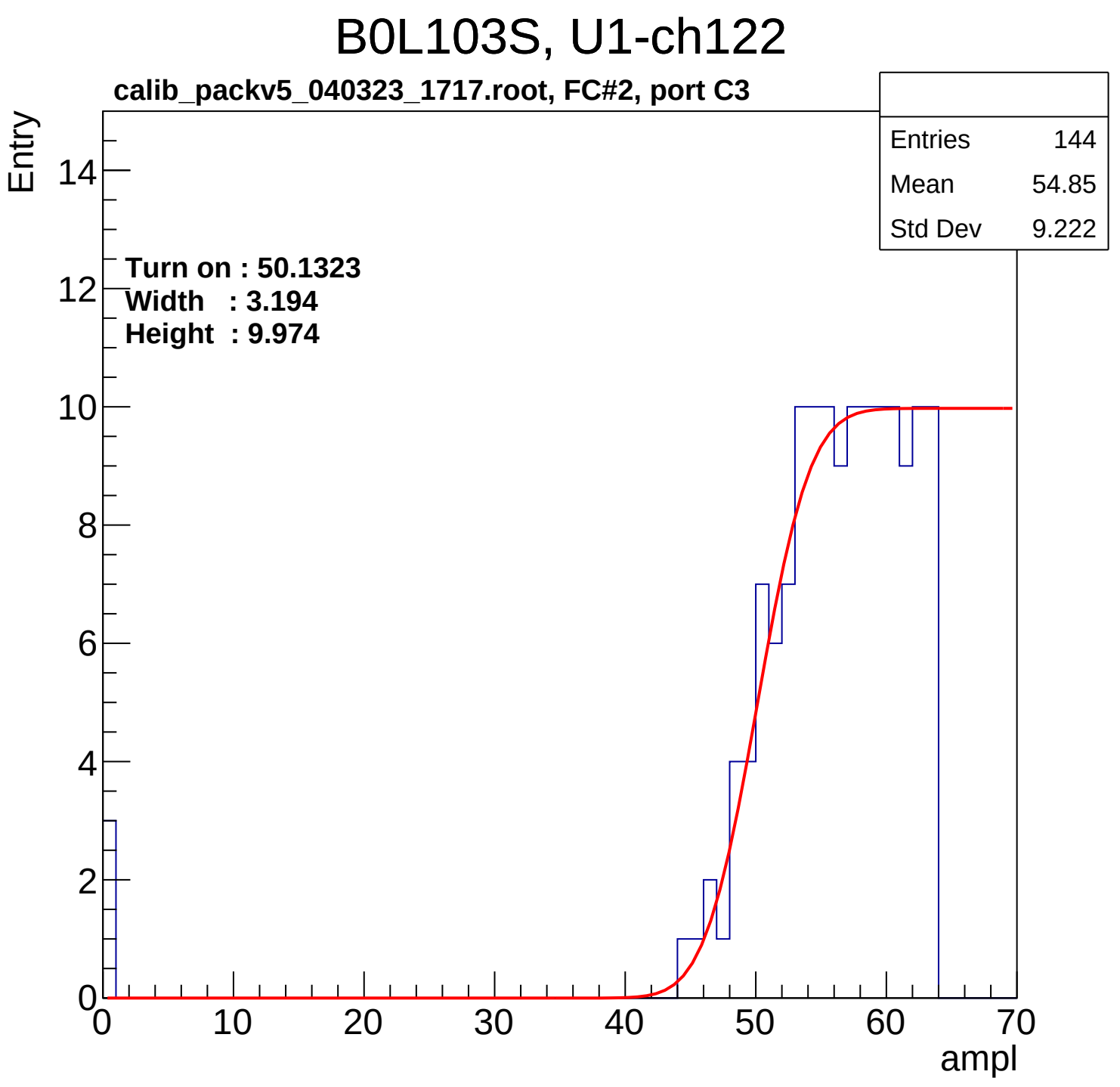
B0L103S, U1-ch122
calib_packv5_040323_1717.root, FC#2, port C3
Entries 144
Mean 54.85
Std Dev 9.222
Turn on : 50.1323
Width : 3.194
Height : 9.974
Entry
ampl
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2
4
6
8
10
12
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0
10
20
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40
50
60
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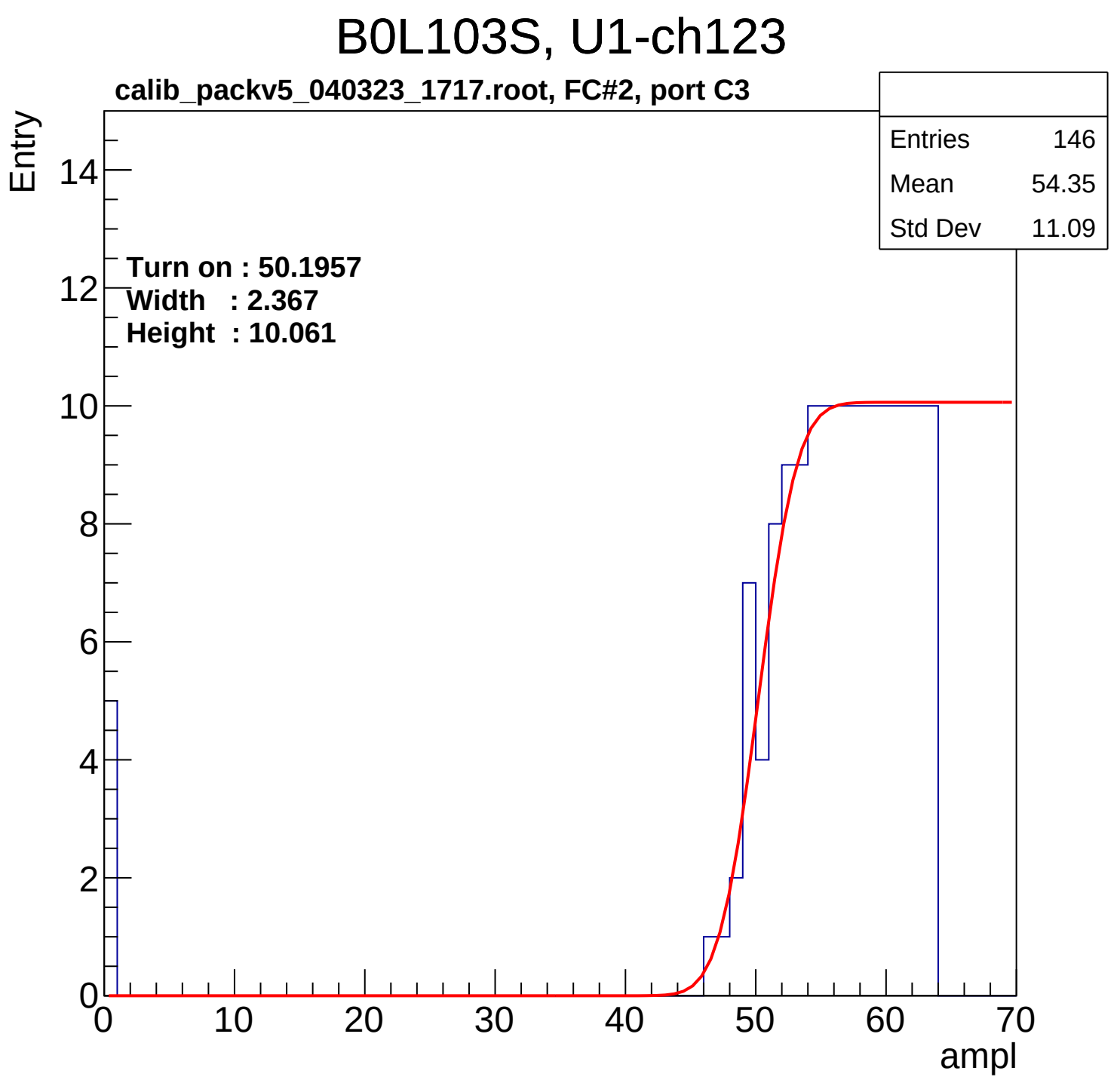
B0L103S, U1-ch123
calib_packv5_040323_1717.root, FC#2, port C3
Entries 146
Mean 54.35
Std Dev 11.09
Turn on : 50.1957
Width : 2.367
Height : 10.061
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
50
60
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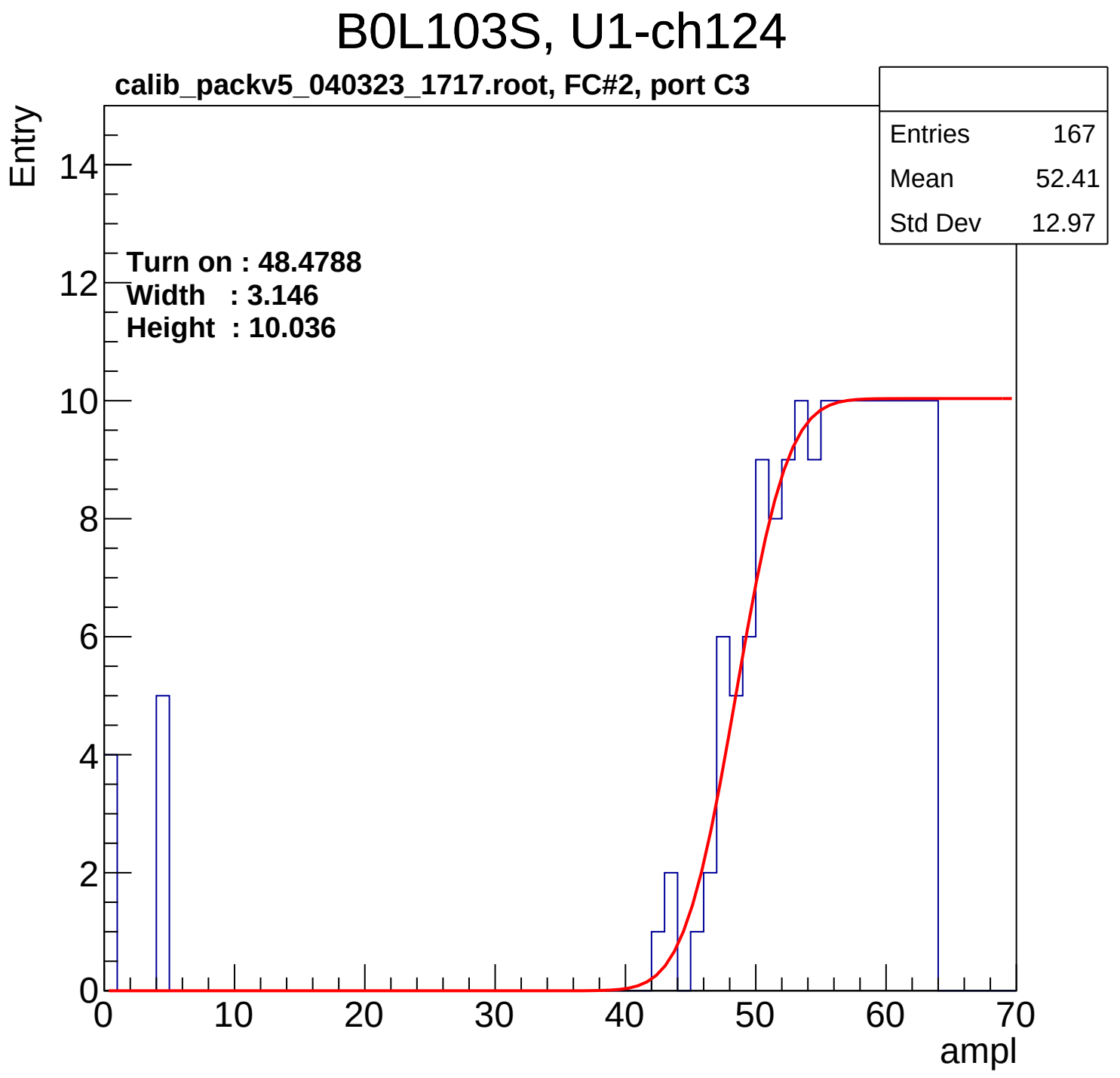
B0L103S, U1-ch124
calib_packv5_040323_1717.root, FC#2, port C3
Entries 167
Mean 52.41
Std Dev 12.97
Turn on : 48.4788
Width : 3.146
Height : 10.036
Entry
ampl
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2
4
6
8
10
12
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10
20
30
40
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60
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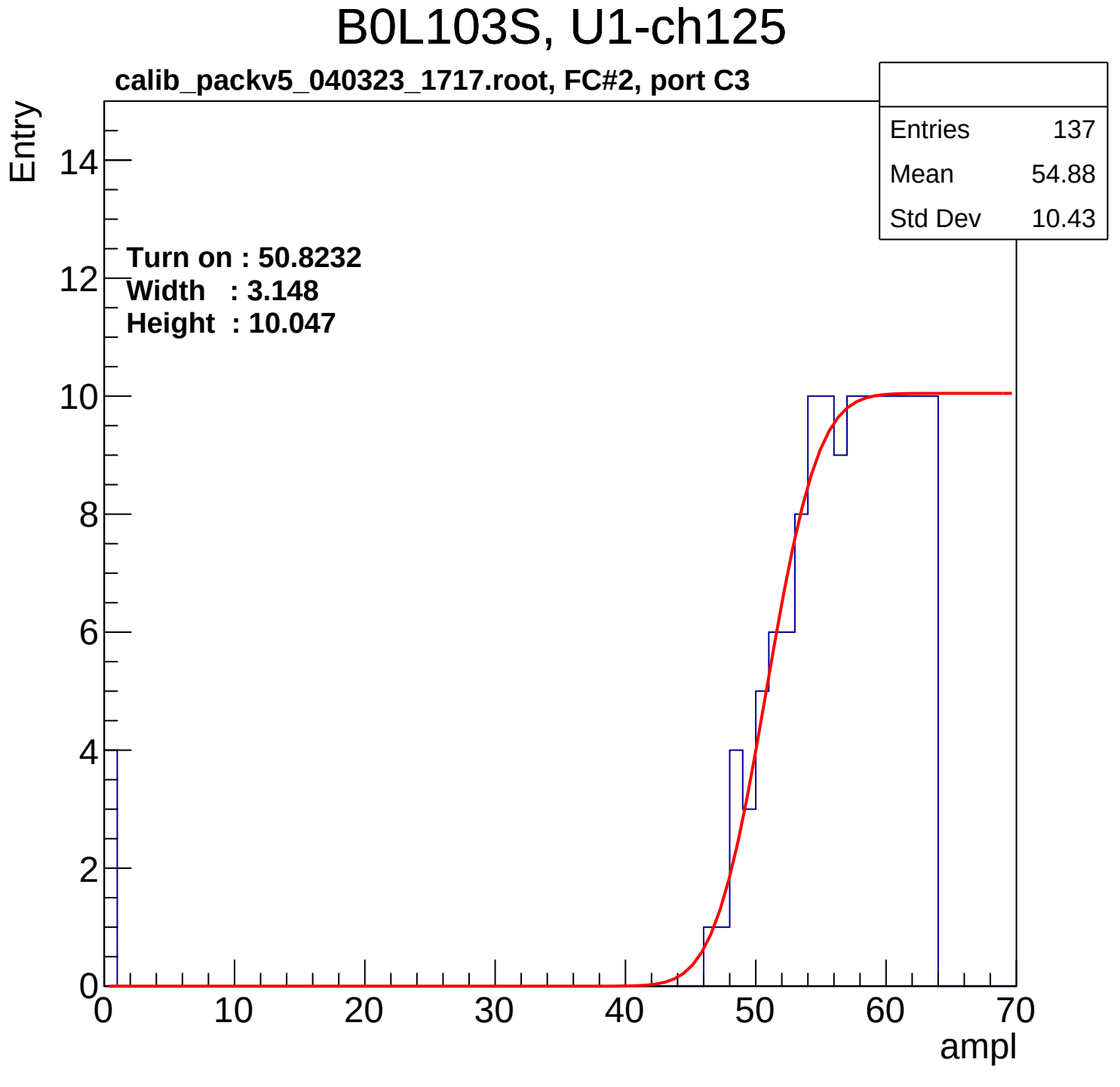
B0L103S, U1-ch125
calib_packv5_040323_1717.root, FC#2, port C3
Entries 137
Mean 54.88
Std Dev 10.43
Turn on : 50.8232
Width : 3.148
Height : 10.047
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
50
60
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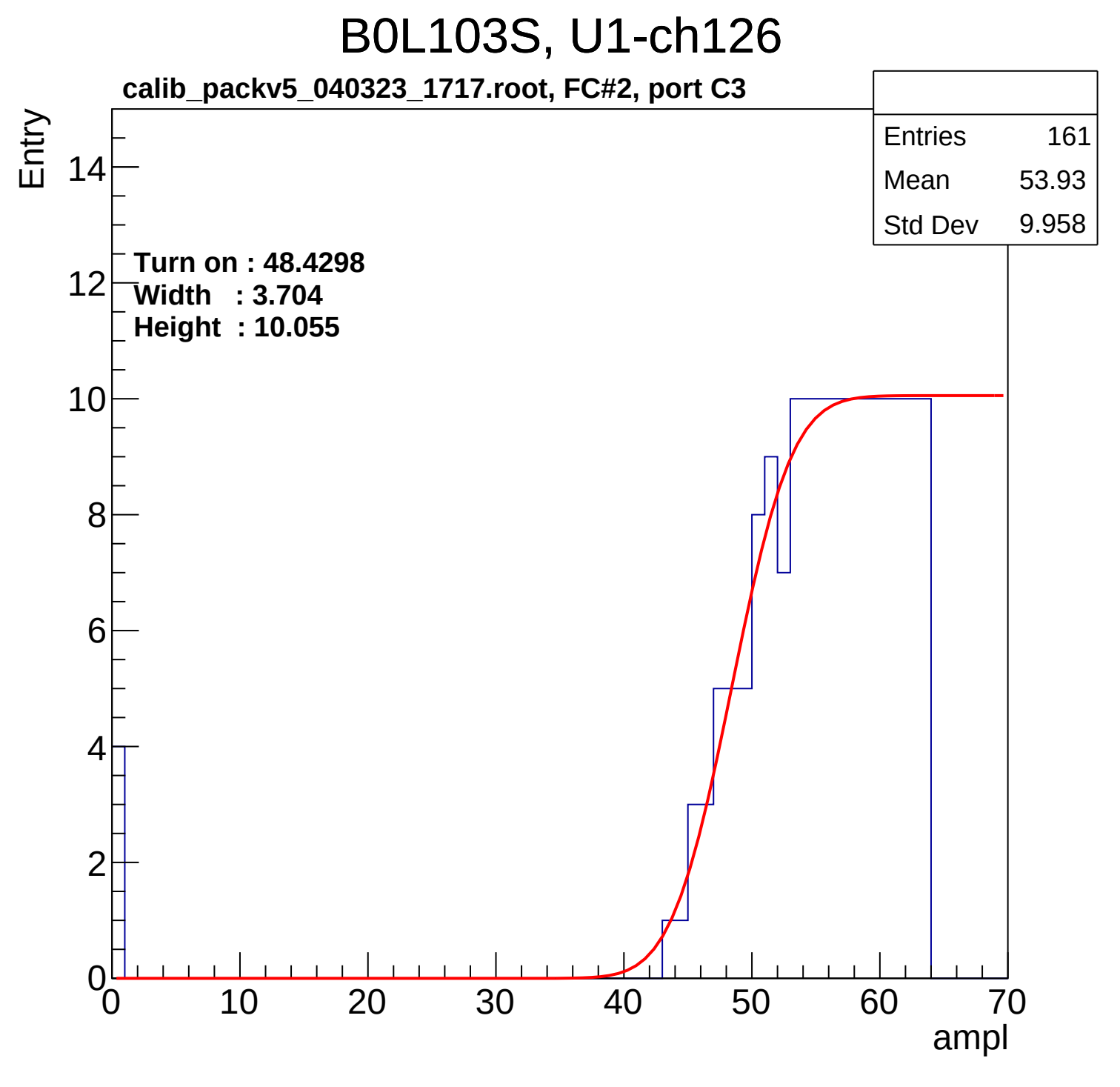
B0L103S, U1-ch126
calib_packv5_040323_1717.root, FC#2, port C3
Entries 161
Mean 53.93
Std Dev 9.958
Turn on : 48.4298
Width : 3.704
Height : 10.055
Entry
ampl
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4
6
8
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0
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60
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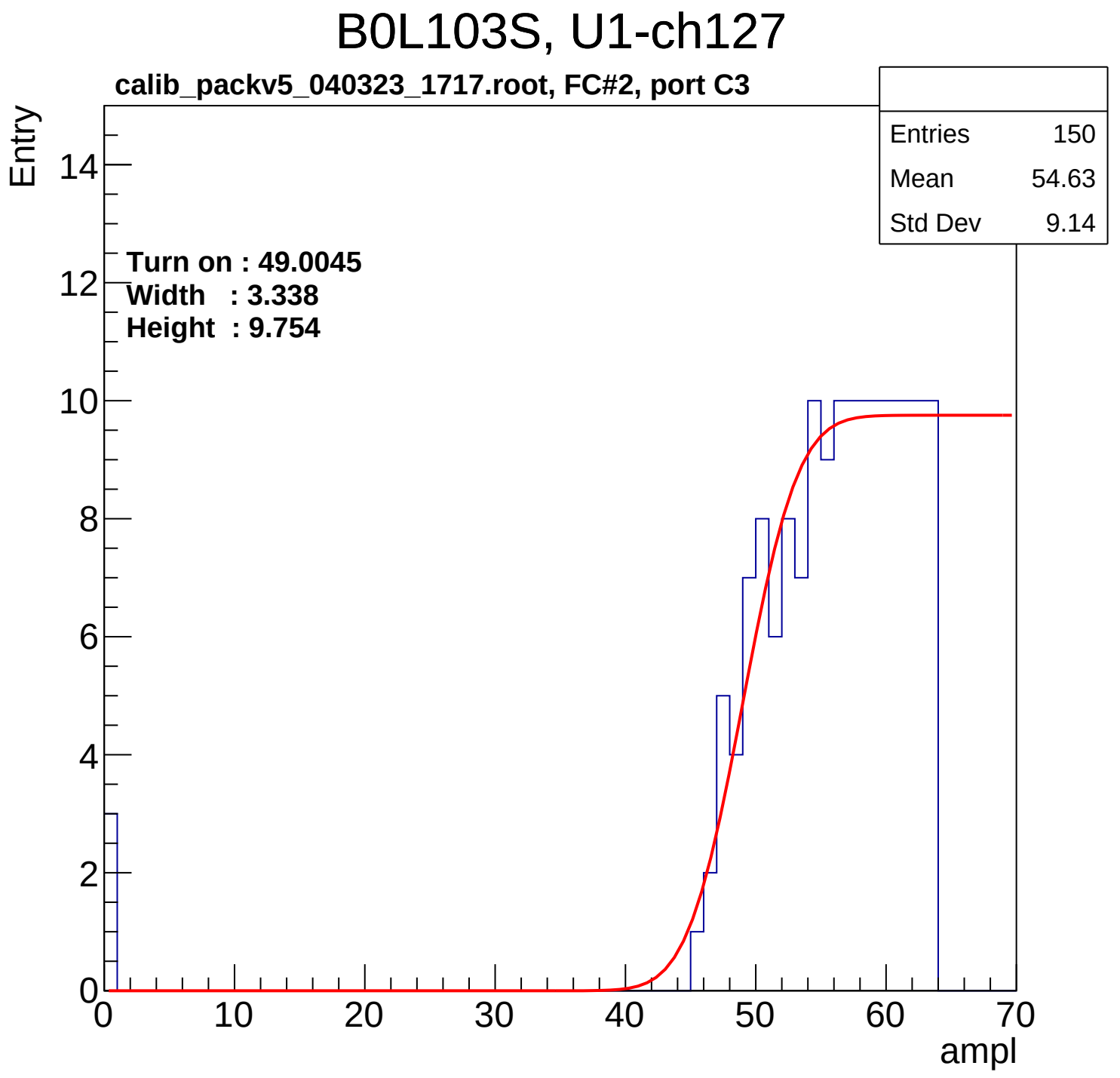
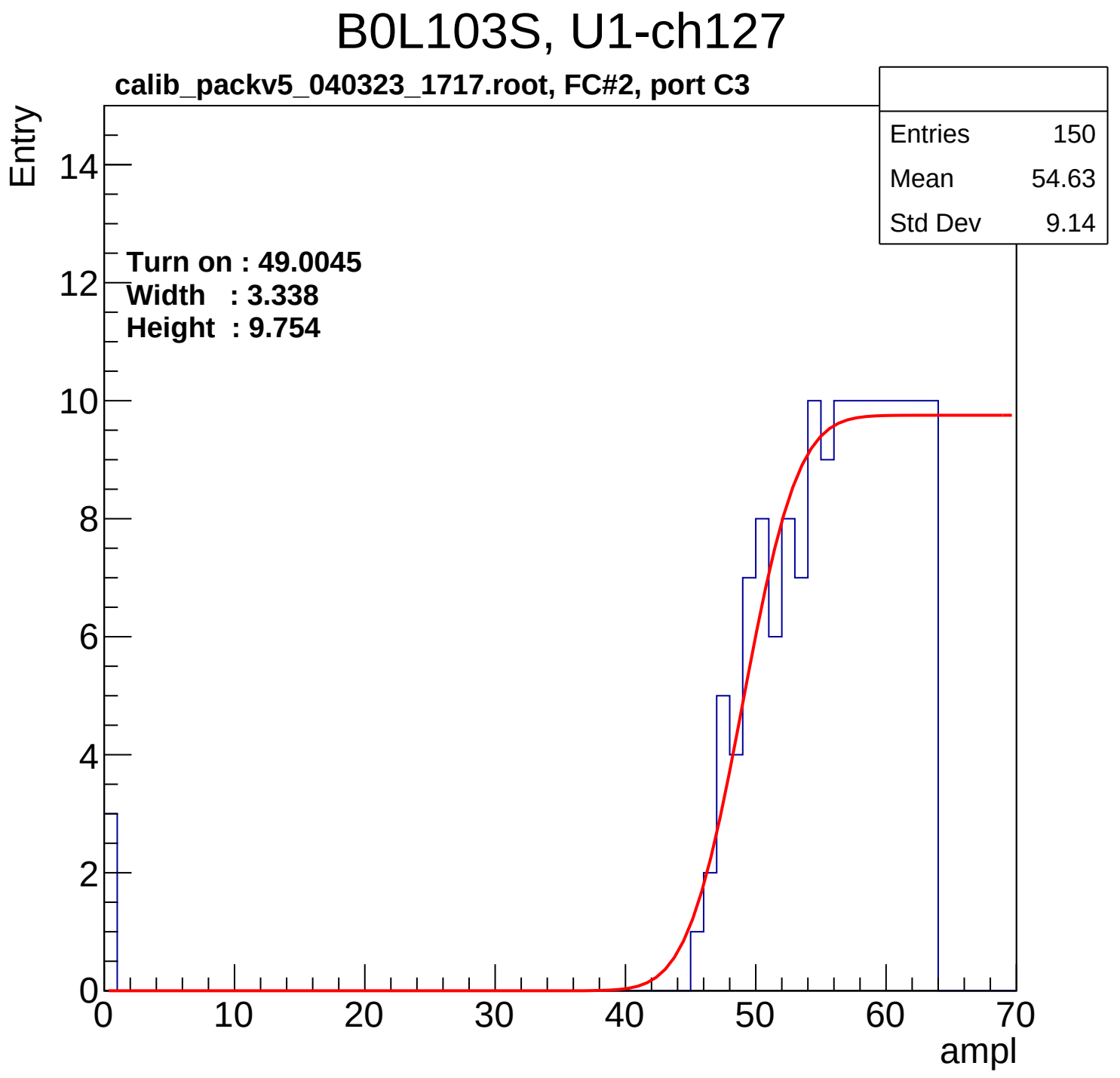

B0L103S, U1-ch127
calib_packv5_040323_1717.root, FC#2, port C3
Entries 150
Mean 54.63
Std Dev 9.14
Turn on : 49.0045
Width : 3.338
Height : 9.754
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L103S, U1-ch127
calib_packv5_040323_1717.root, FC#2, port C3
Entries 150
Mean 54.63
Std Dev 9.14
Turn on : 49.0045
Width : 3.338
Height : 9.754
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70