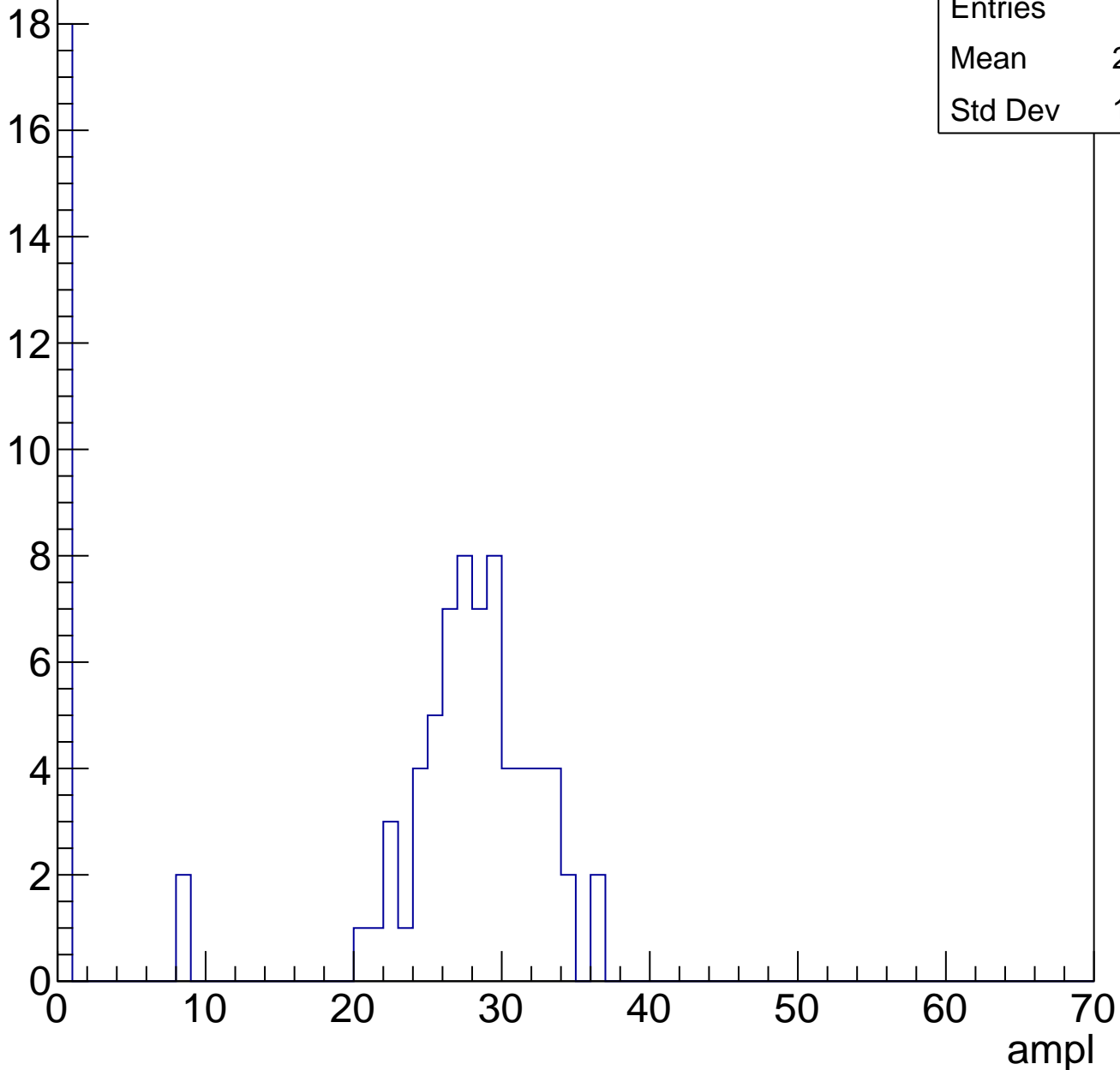


B1L103S, U23-ch0, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	85
Mean	21.61
Std Dev	12.01

Entry



B1L103S, U23-ch0, adc1

calib_packv5_041523_1651.root, FC#0, port C2

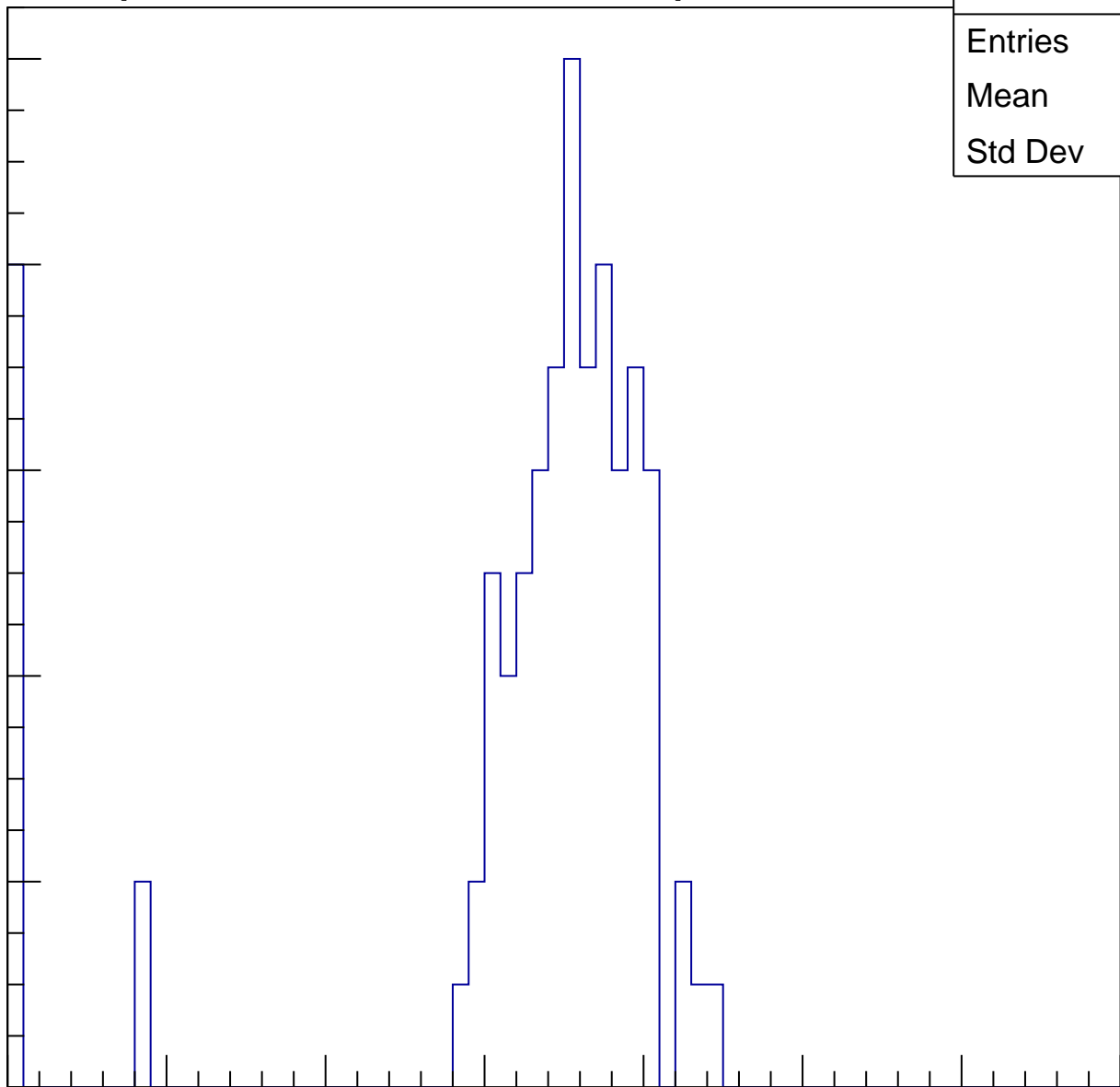
Entries	88
Mean	31.61
Std Dev	11.3

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

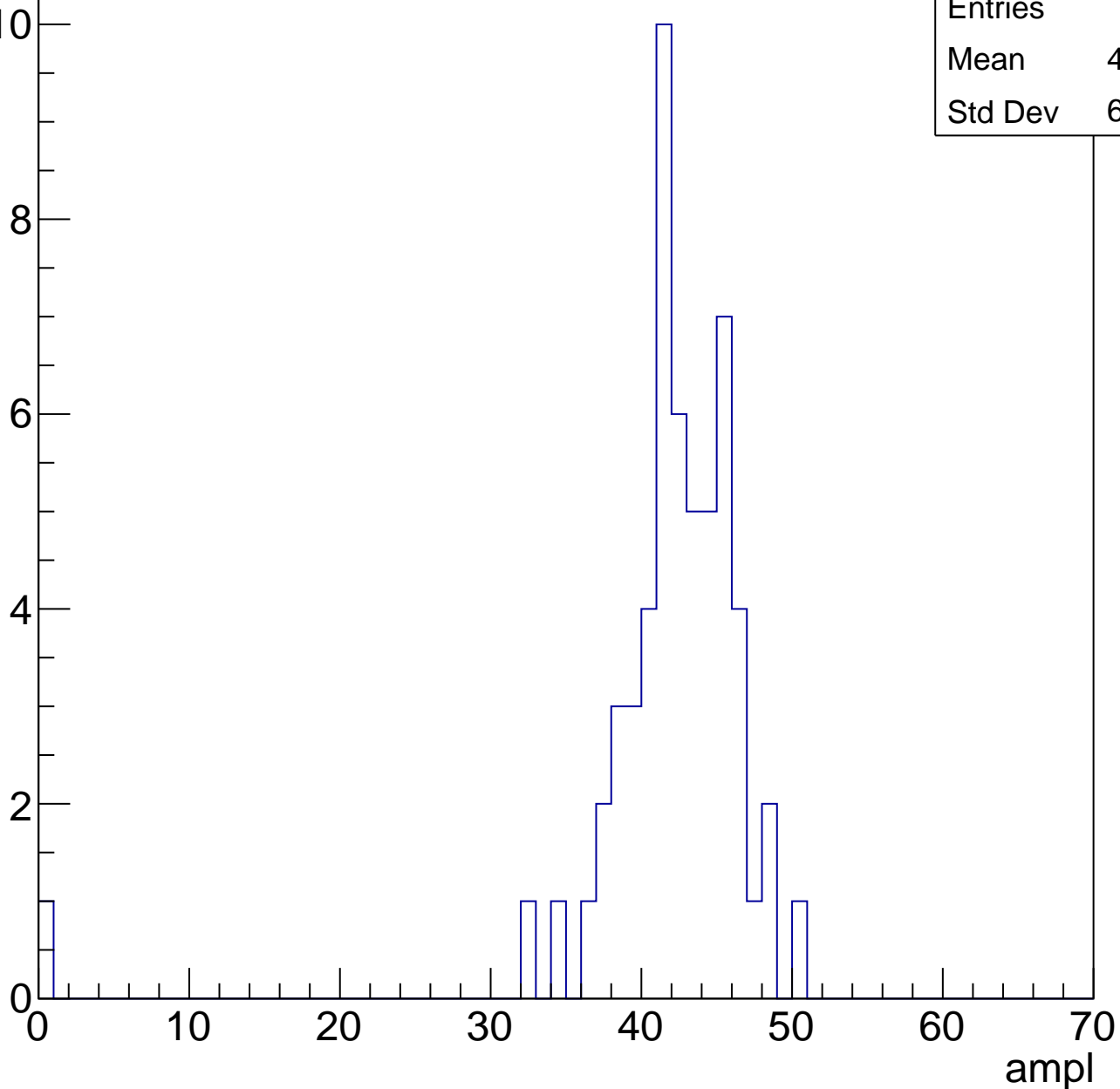


B1L103S, U23-ch0, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	57
Mean	41.33
Std Dev	6.492

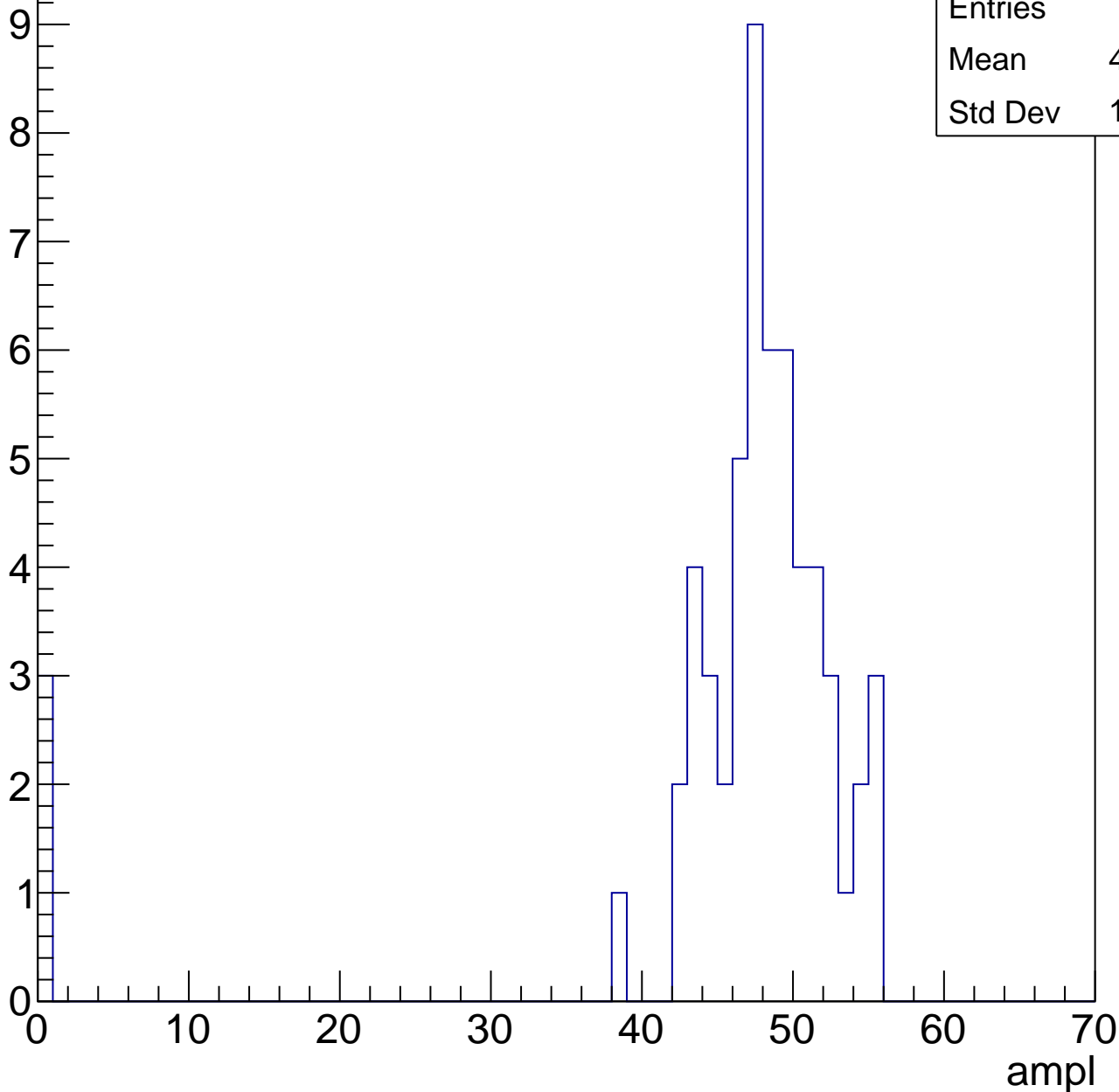


B1L103S, U23-ch0, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	45.47
Std Dev	11.19

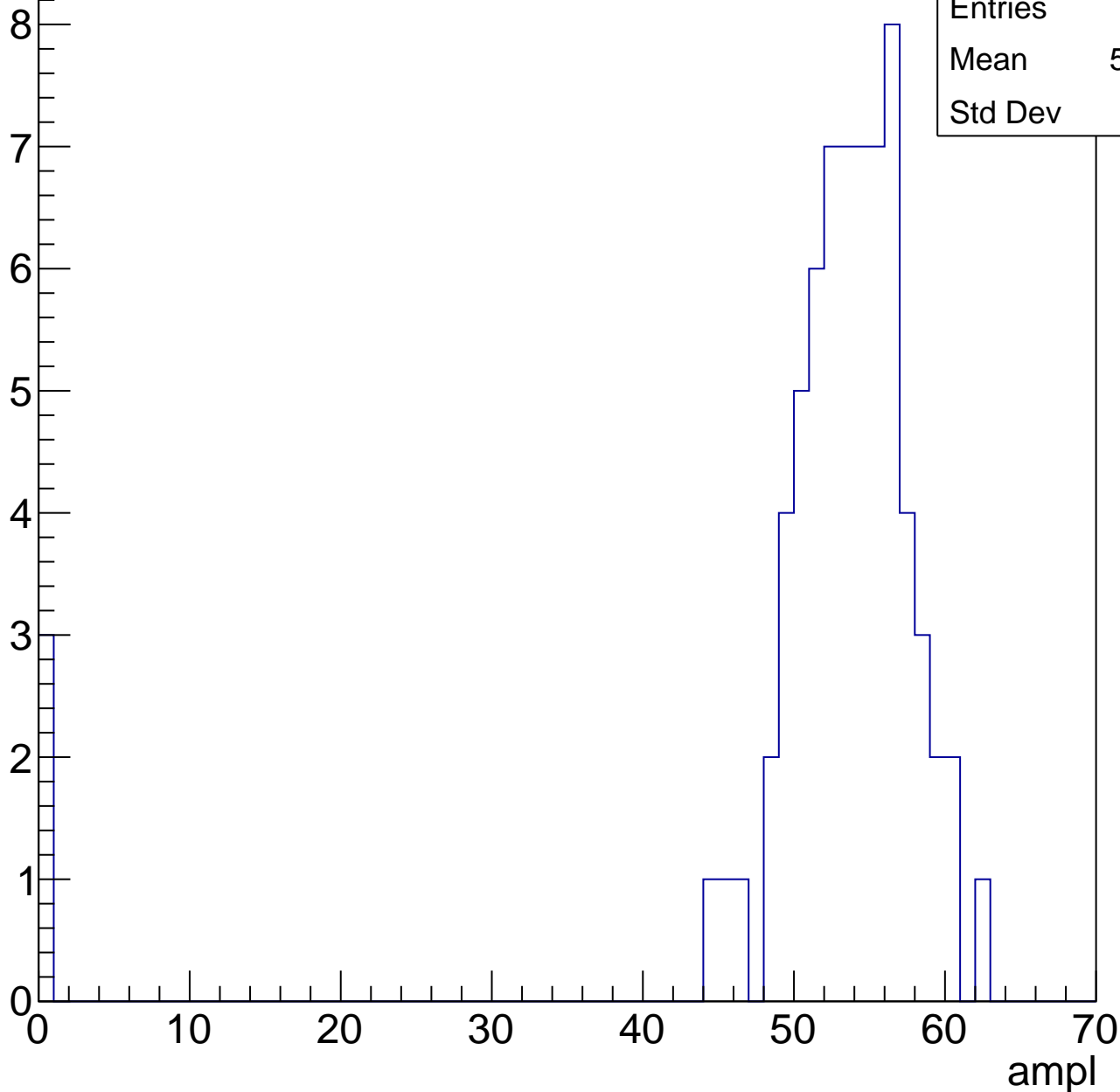


B1L103S, U23-ch0, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	51.14
Std Dev	11.3

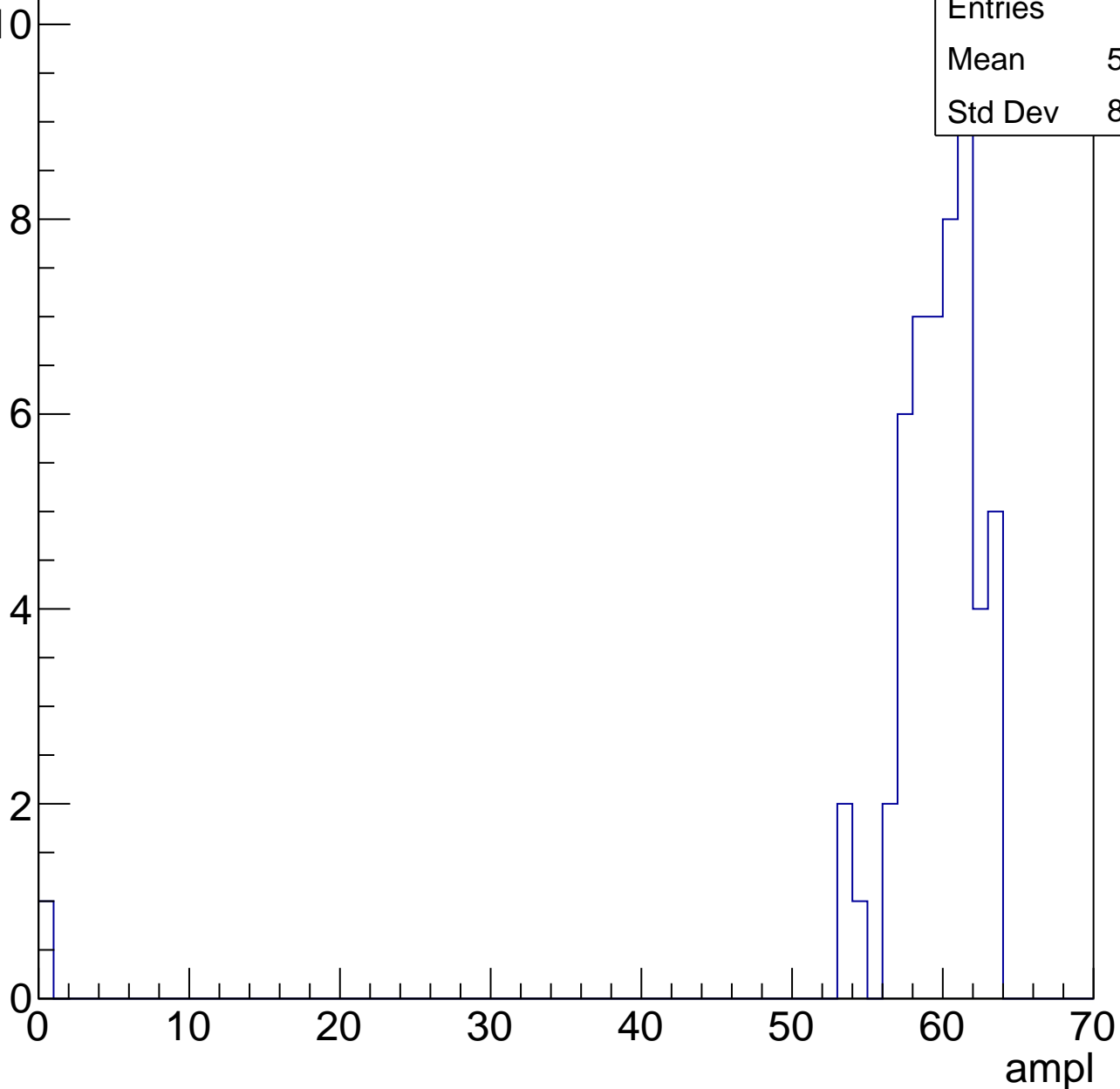


B1L103S, U23-ch0, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	53
Mean	58.23
Std Dev	8.422

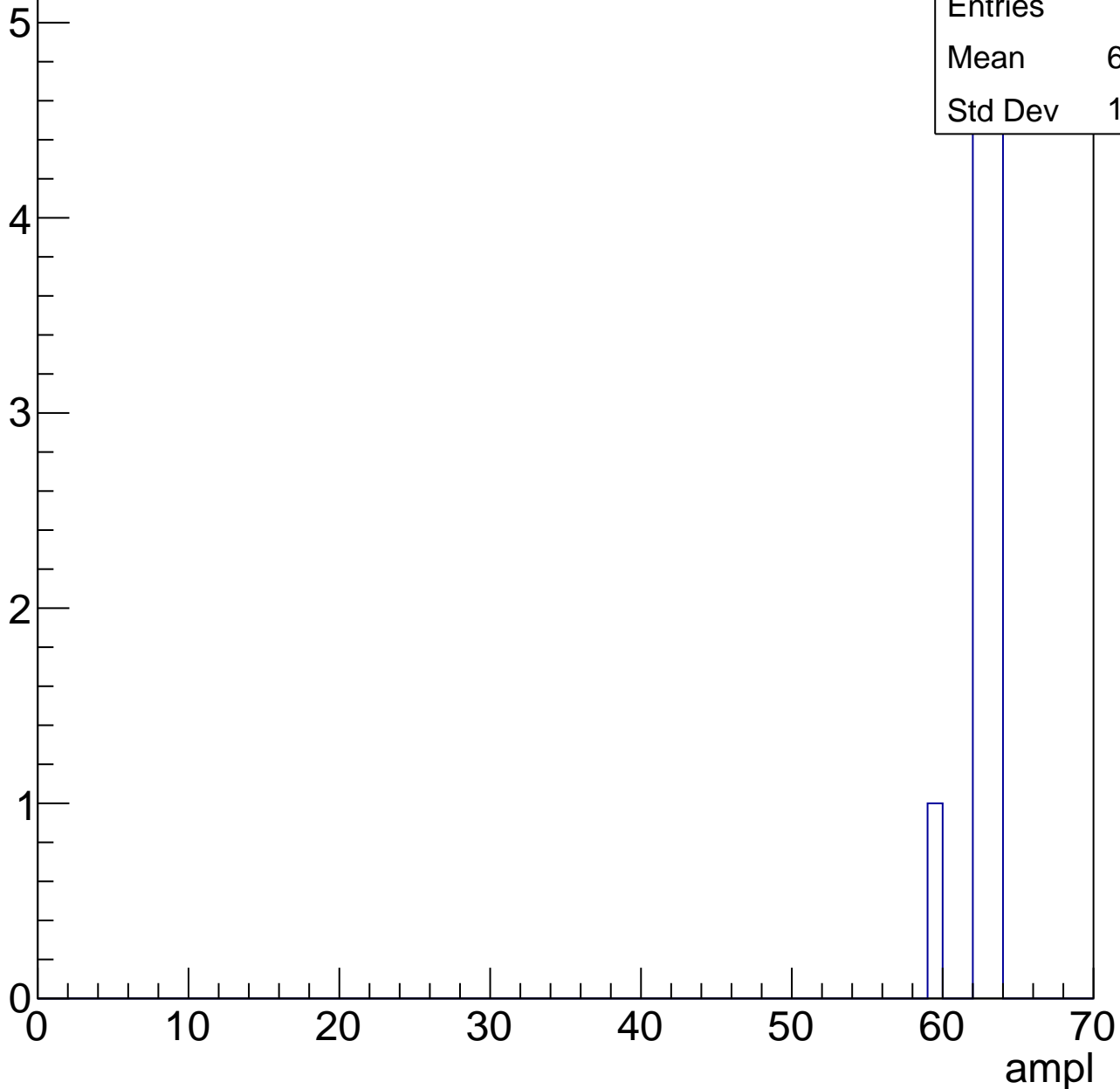


B1L103S, U23-ch0, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	11
Mean	62.18
Std Dev	1.113



B1L103S, U23-ch0, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

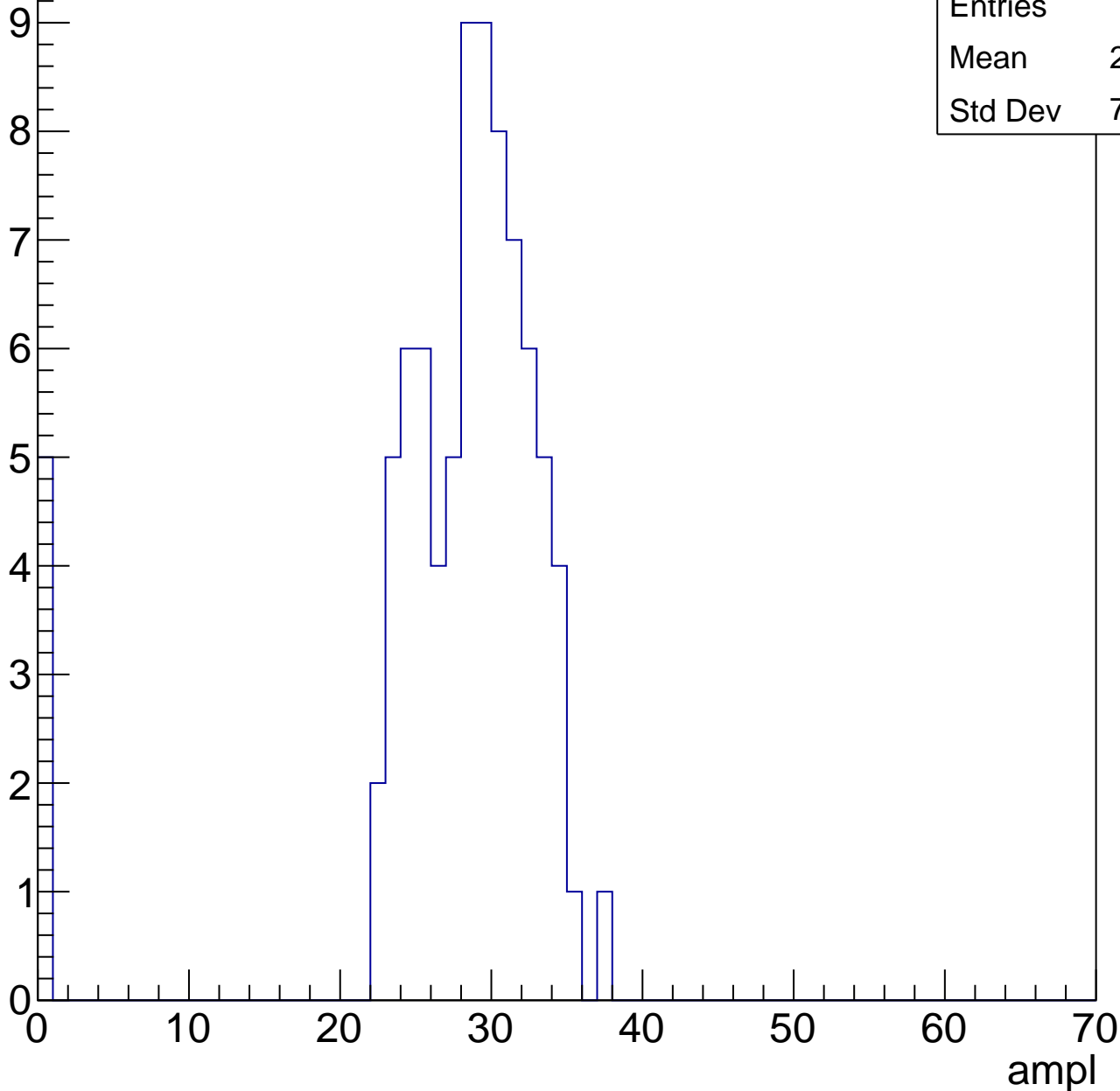
ampl

B1L103S, U23-ch1, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	83
Mean	26.83
Std Dev	7.584

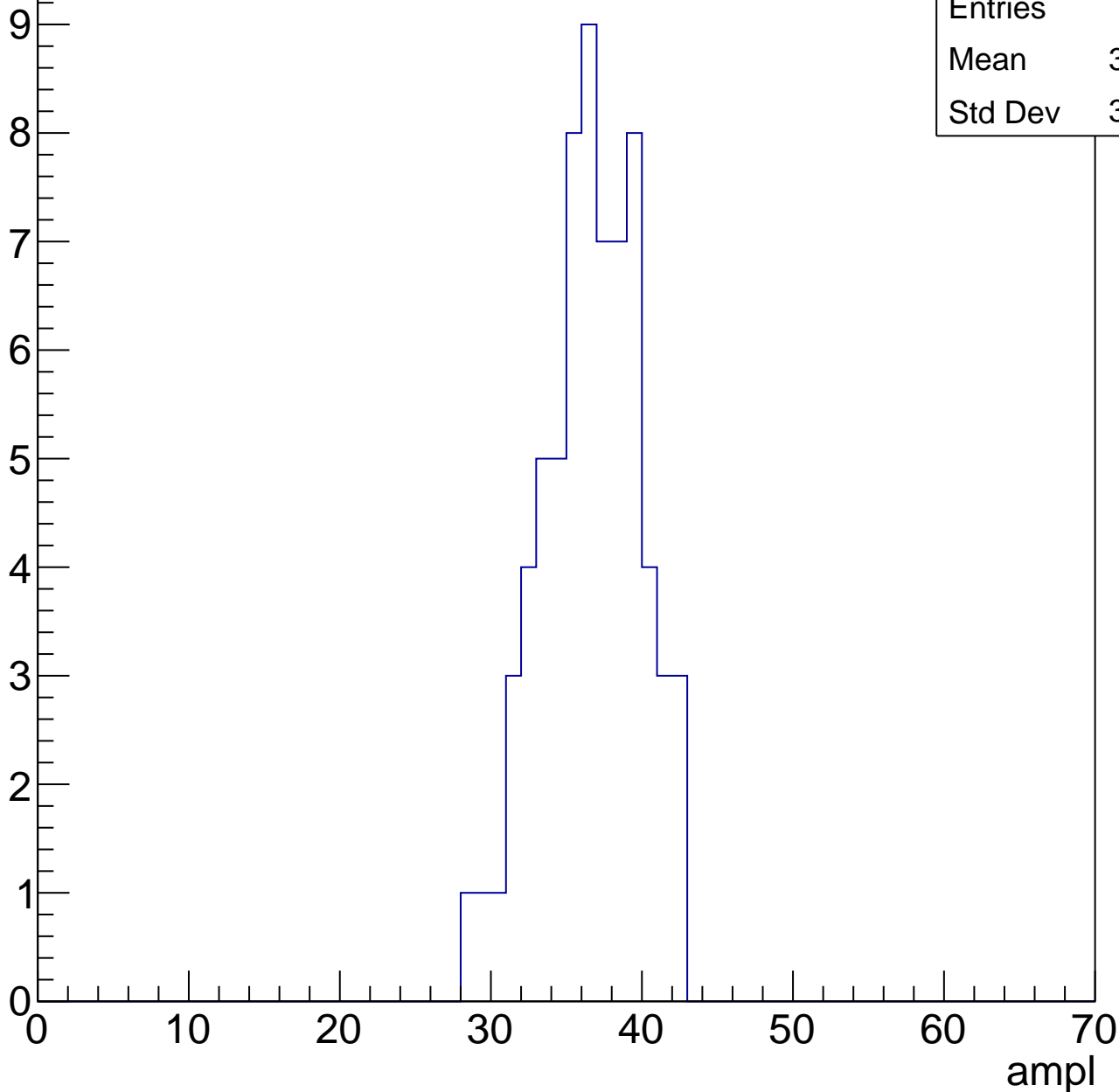


B1L103S, U23-ch1, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	36.13
Std Dev	3.216

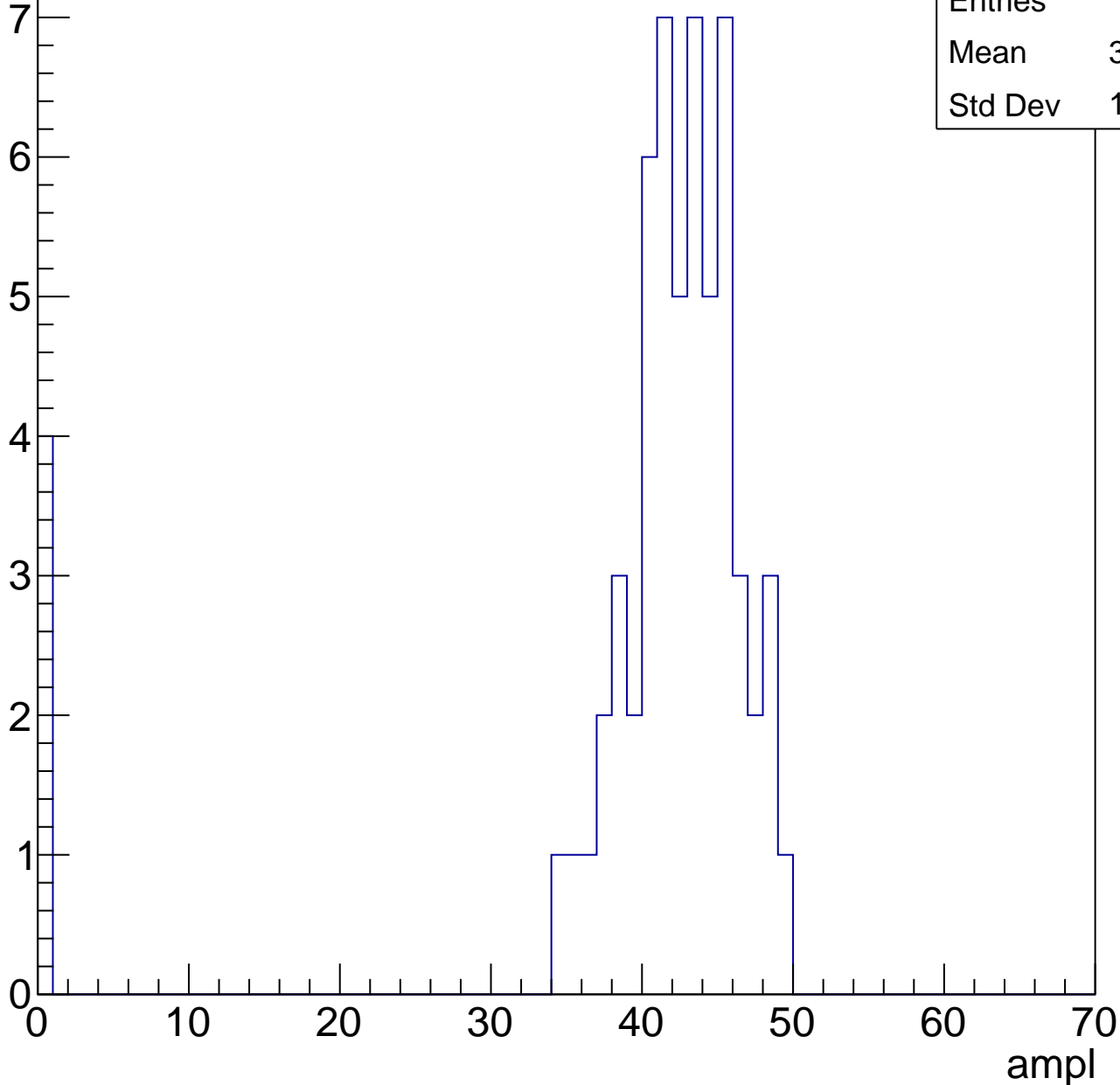


B1L103S, U23-ch1, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	39.48
Std Dev	11.04

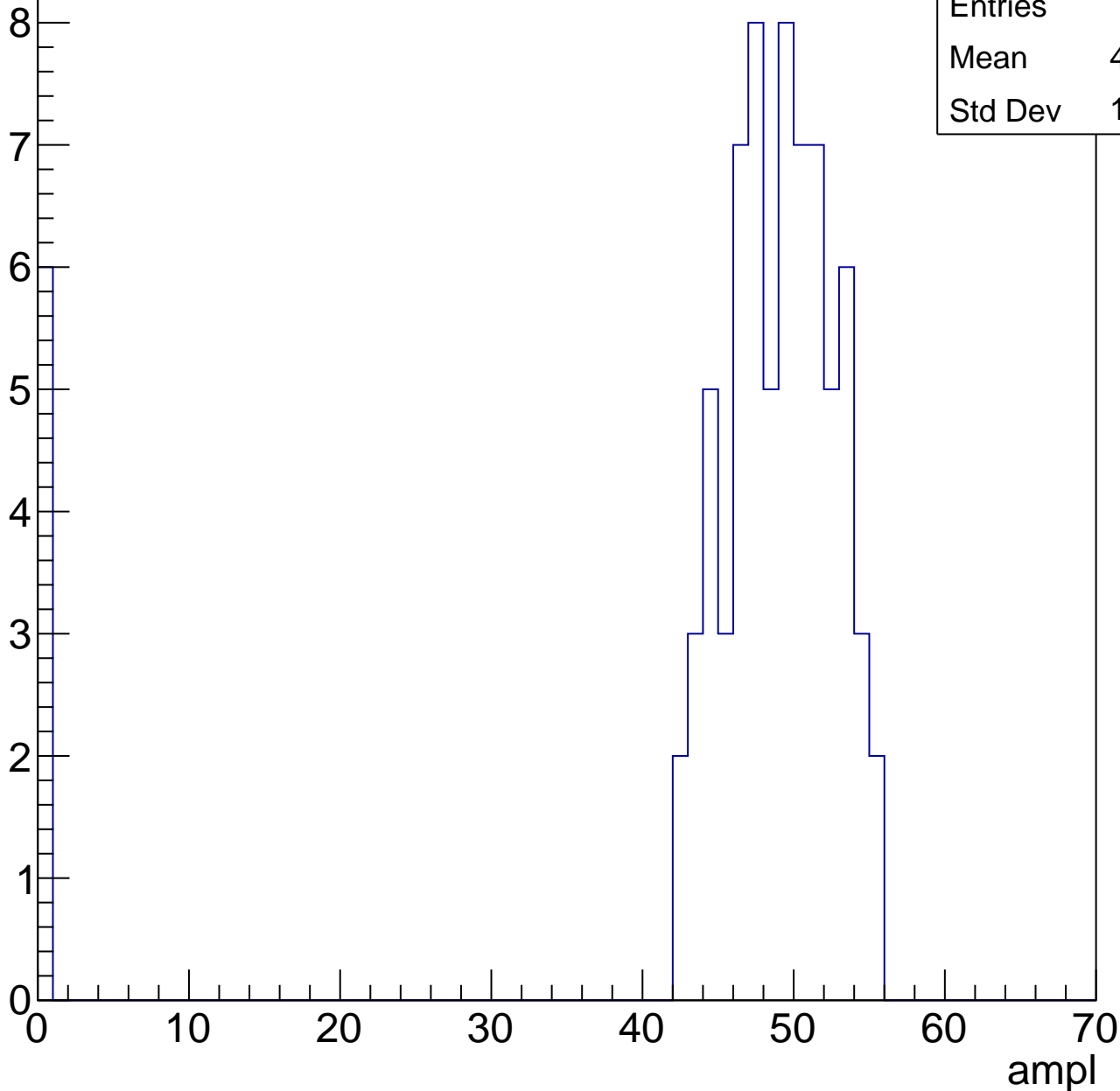


B1L103S, U23-ch1, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	77
Mean	44.87
Std Dev	13.43

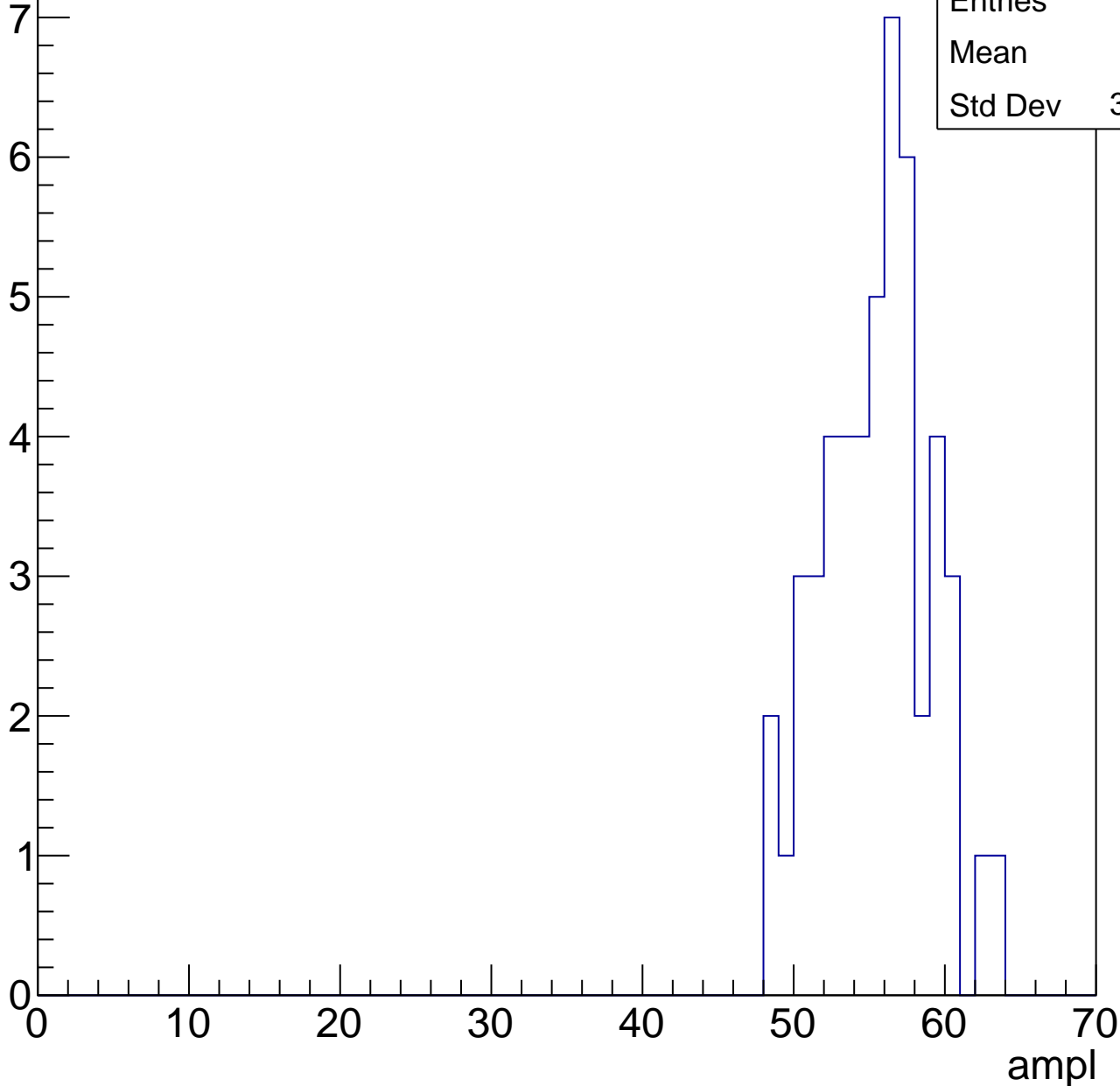


B1L103S, U23-ch1, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	50
Mean	55
Std Dev	3.504

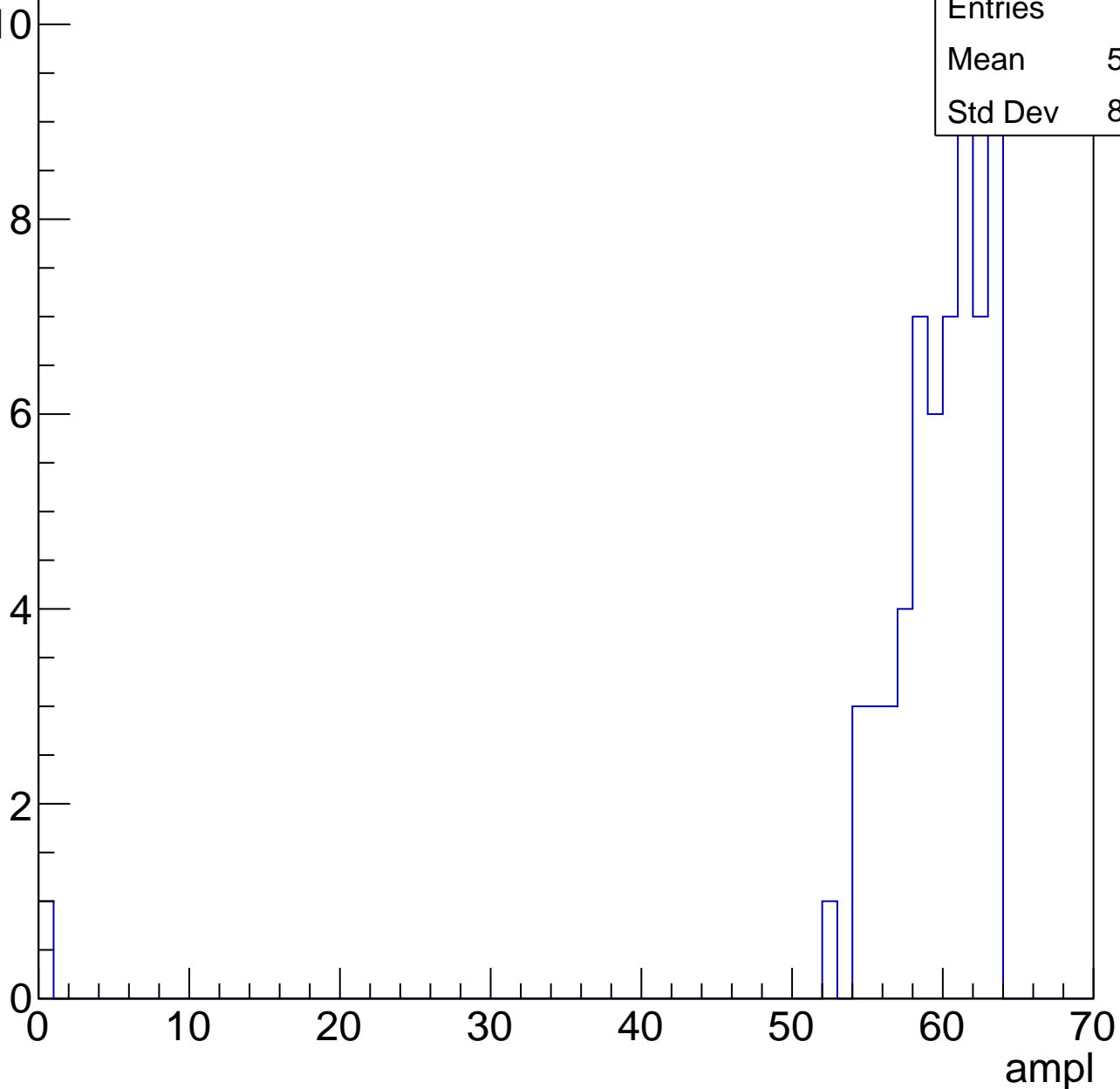


B1L103S, U23-ch1, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	58.46
Std Dev	8.036



B1L103S, U23-ch1, adc6

calib_packv5_041523_1651.root, FC#0, port C2

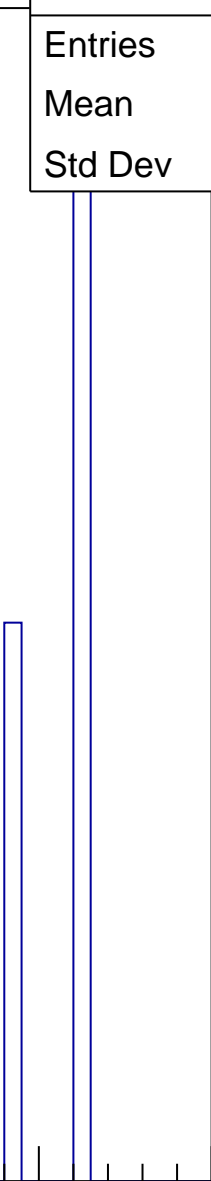
Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	3
Mean	60.67
Std Dev	1.886

0 10 20 30 40 50 60 70

ampl

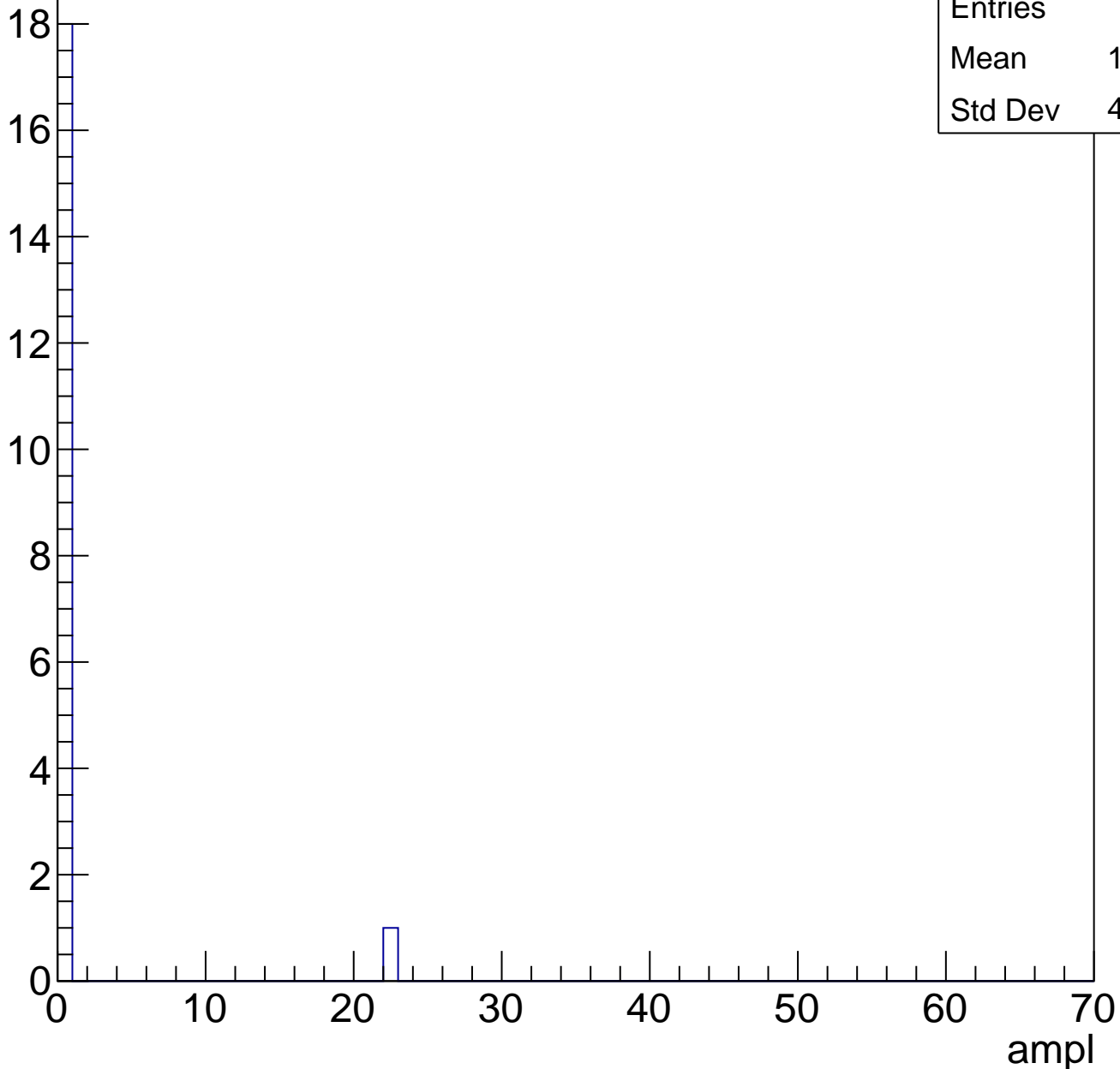


B1L103S, U23-ch1, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.158
Std Dev	4.913

Entry



B1L103S, U23-ch2, adc0

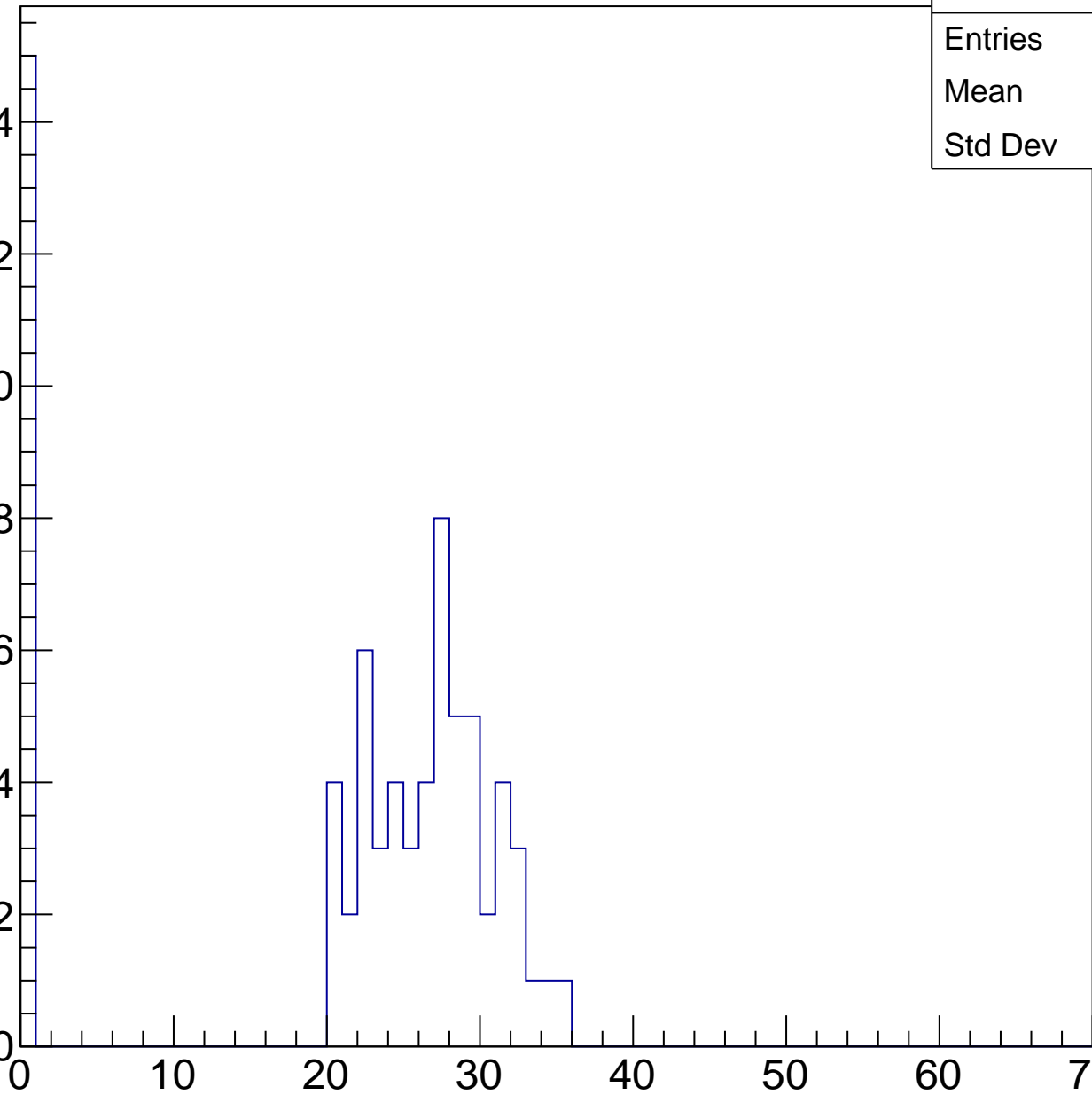
calib_packv5_041523_1651.root, FC#0, port C2

Entries	71
Mean	20.86
Std Dev	11.33

Entry

14
12
10
8
6
4
2
0

ampl

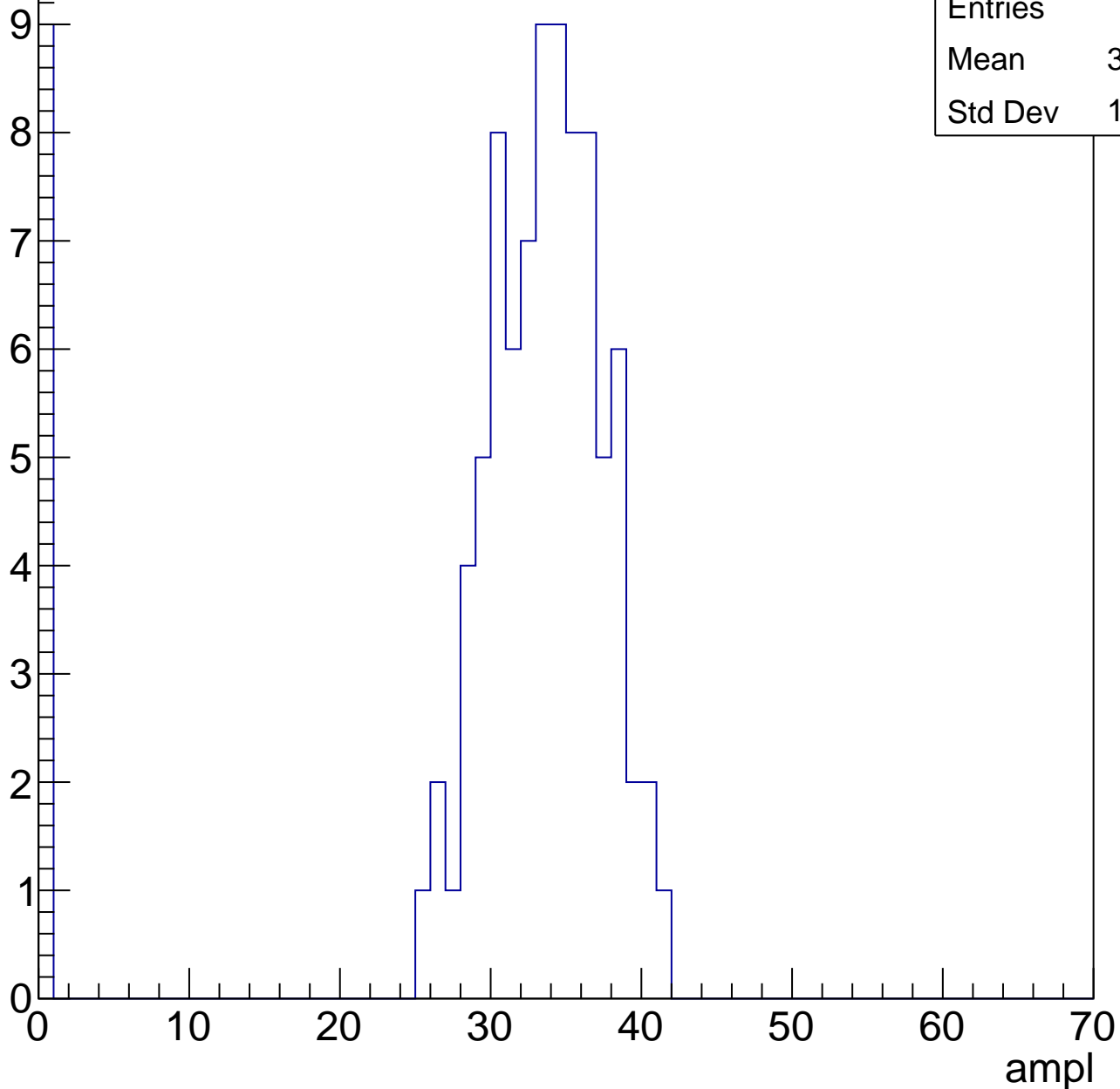


B1L103S, U23-ch2, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	93
Mean	30.04
Std Dev	10.39

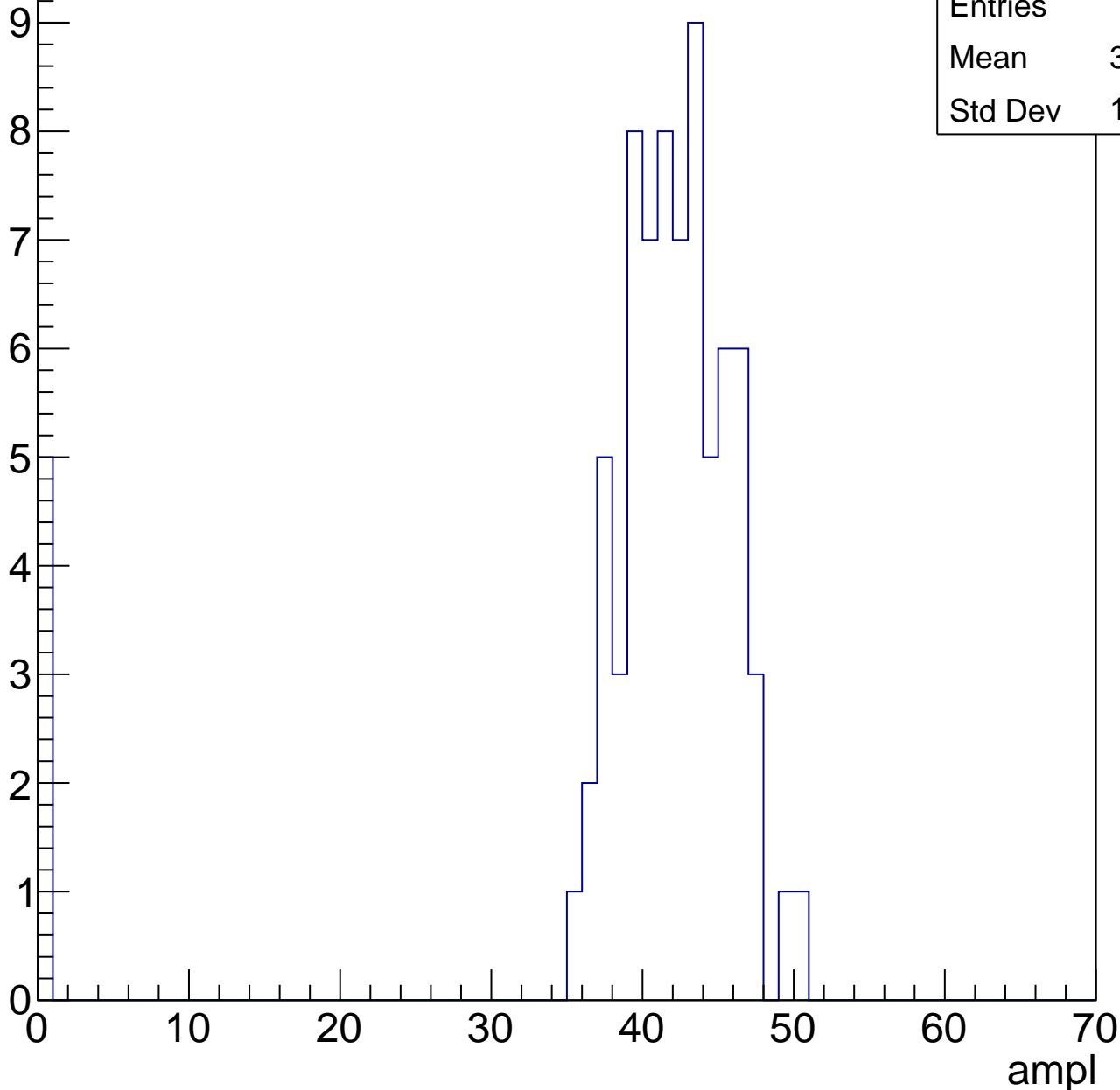


B1L103S, U23-ch2, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	77
Mean	39.13
Std Dev	10.78



B1L103S, U23-ch2, adc3

calib_packv5_041523_1651.root, FC#0, port C2

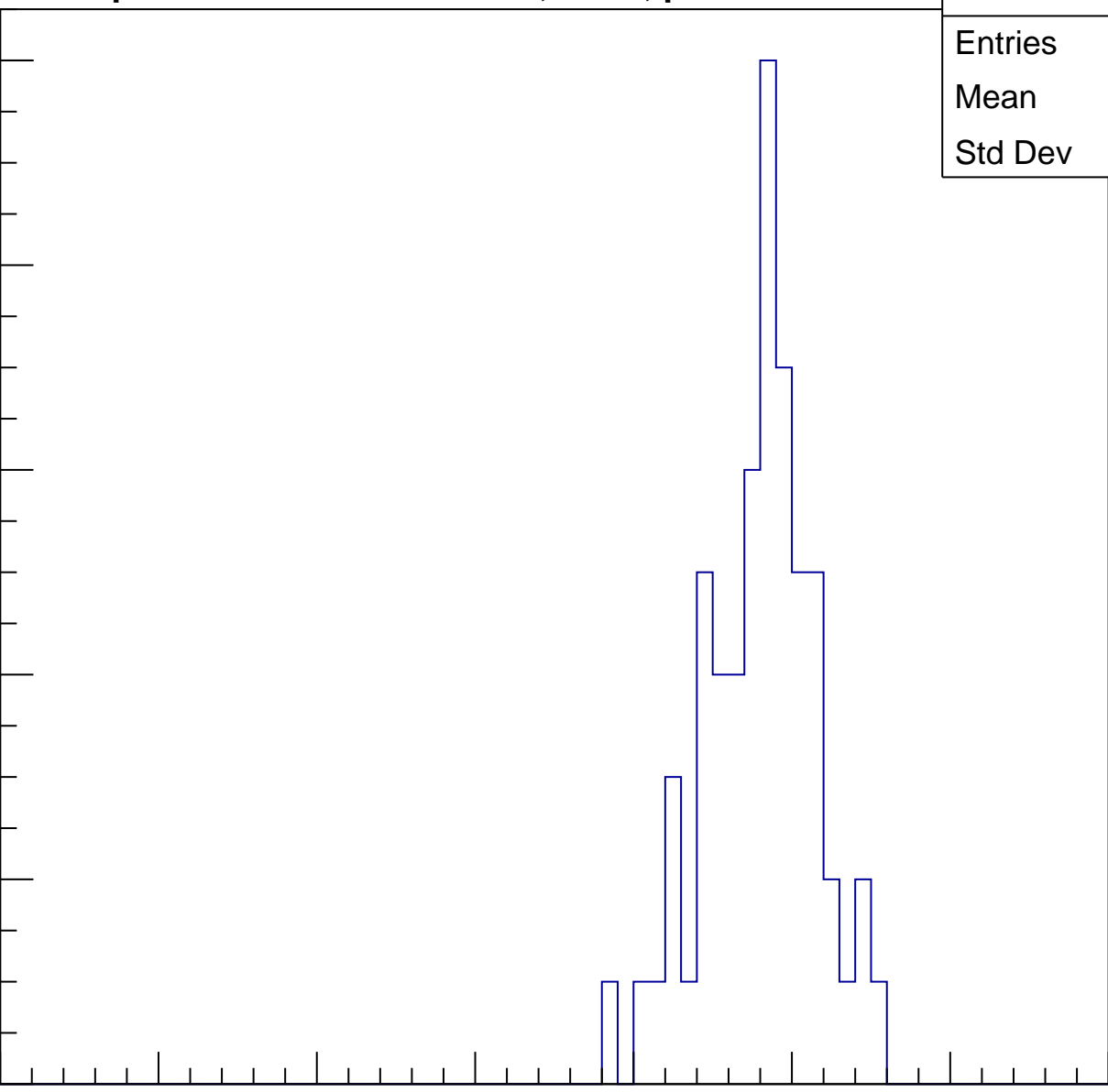
Entries	59
Mean	47.49
Std Dev	3.49

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

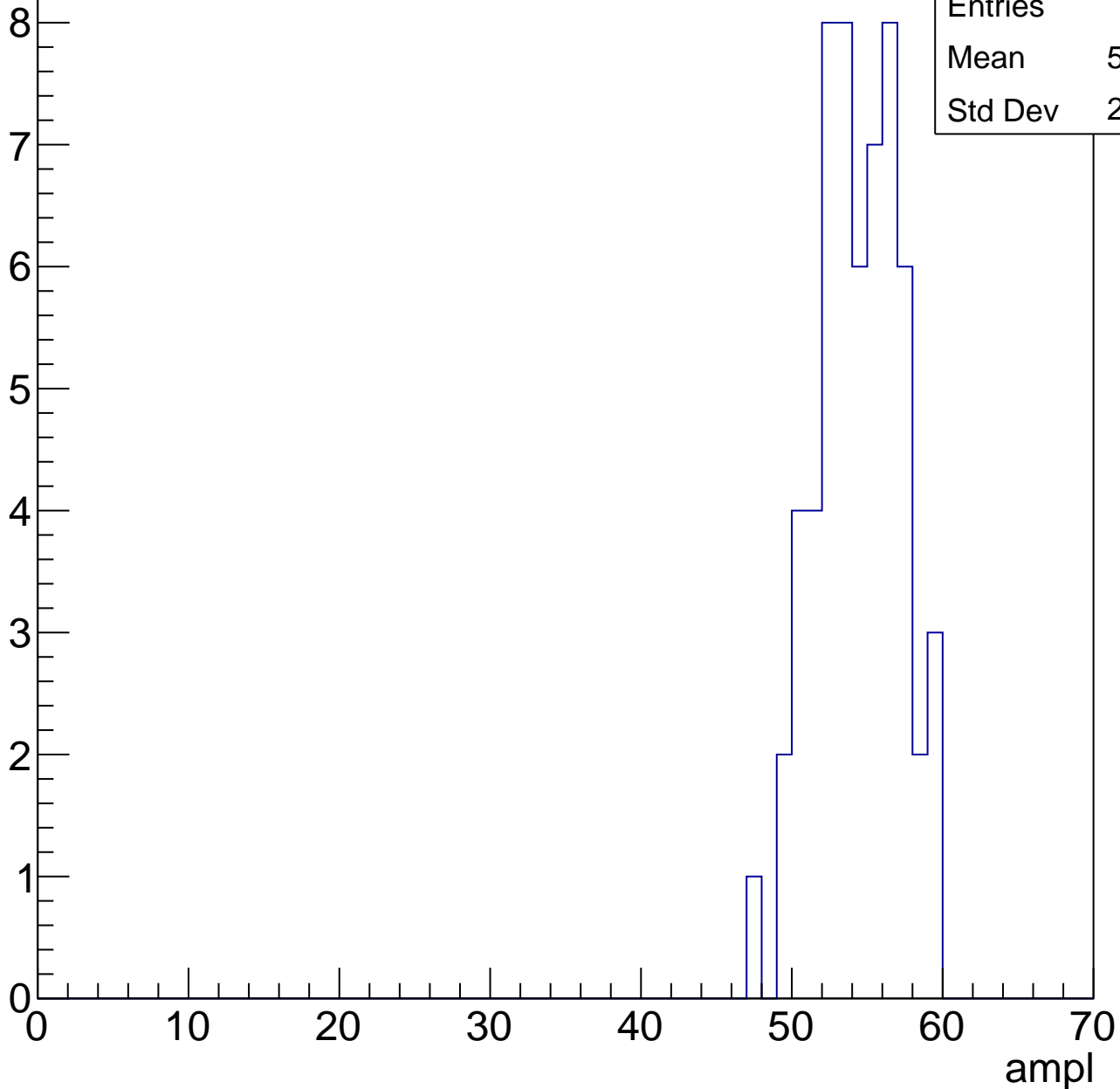


B1L103S, U23-ch2, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	53.92
Std Dev	2.726

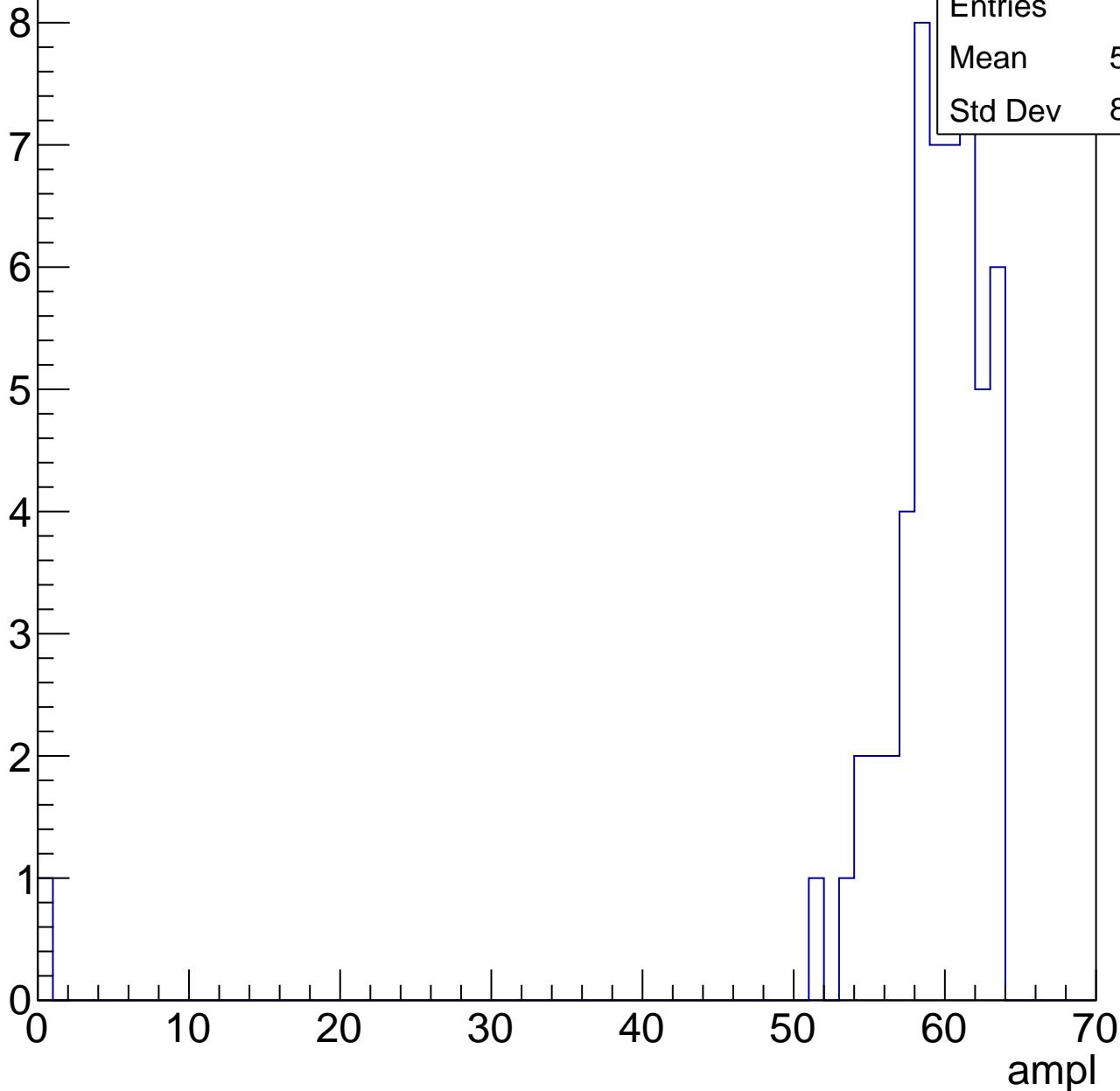


B1L103S, U23-ch2, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	54
Mean	58.06
Std Dev	8.429

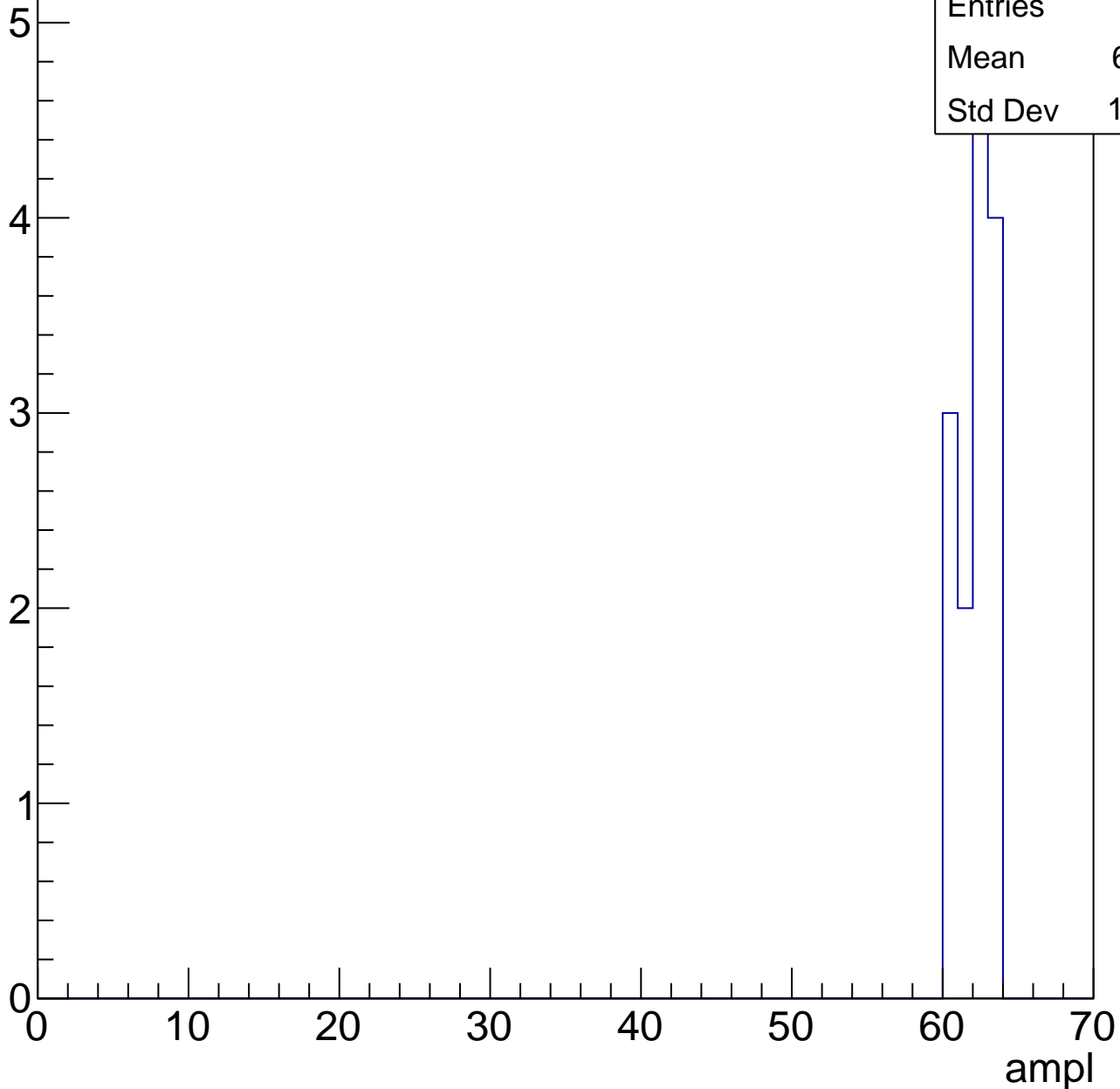


B1L103S, U23-ch2, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	14
Mean	61.71
Std Dev	1.097



B1L103S, U23-ch2, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

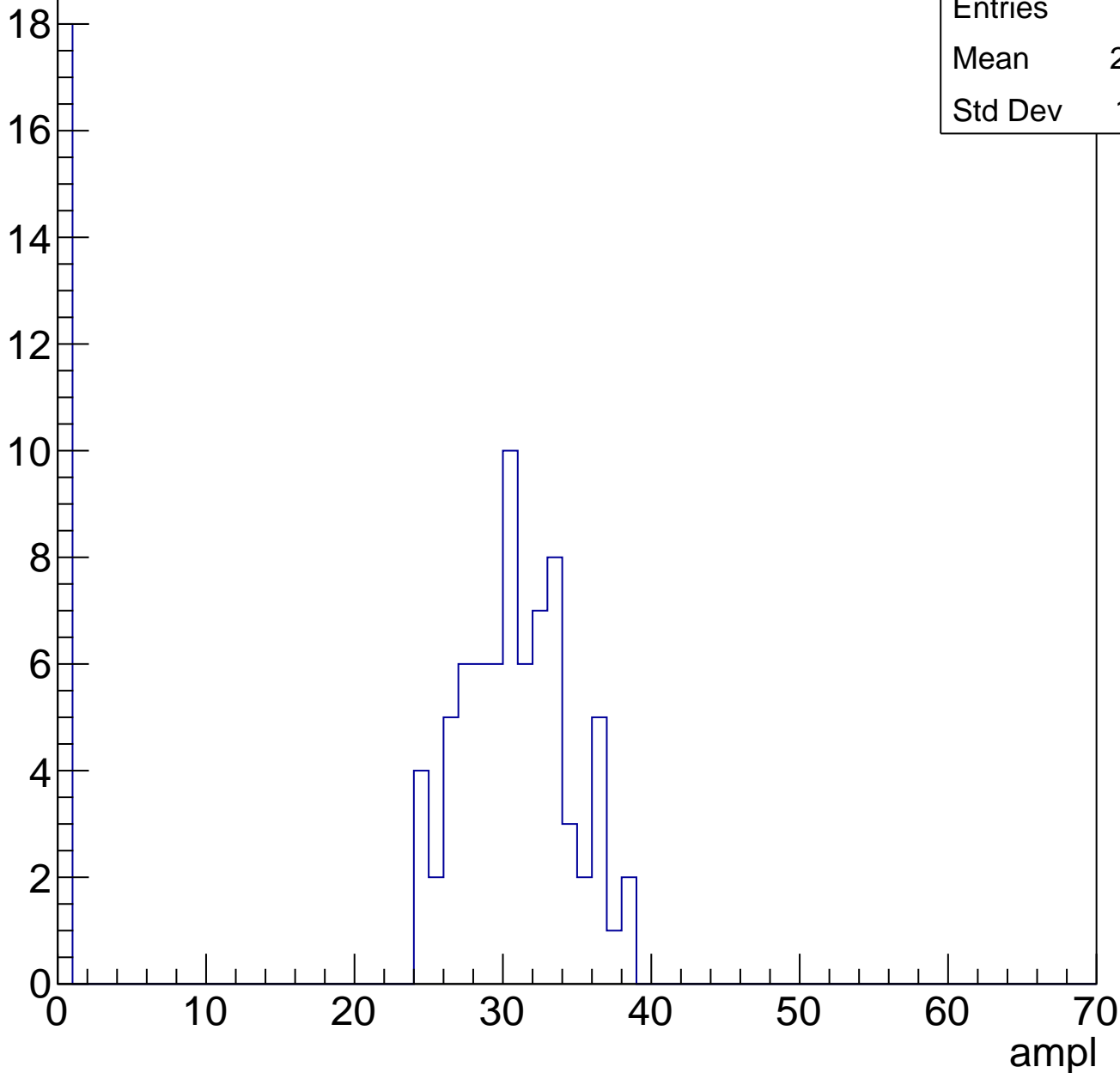
ampl

B1L103S, U23-ch3, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	91
Mean	24.38
Std Dev	12.51

Entry

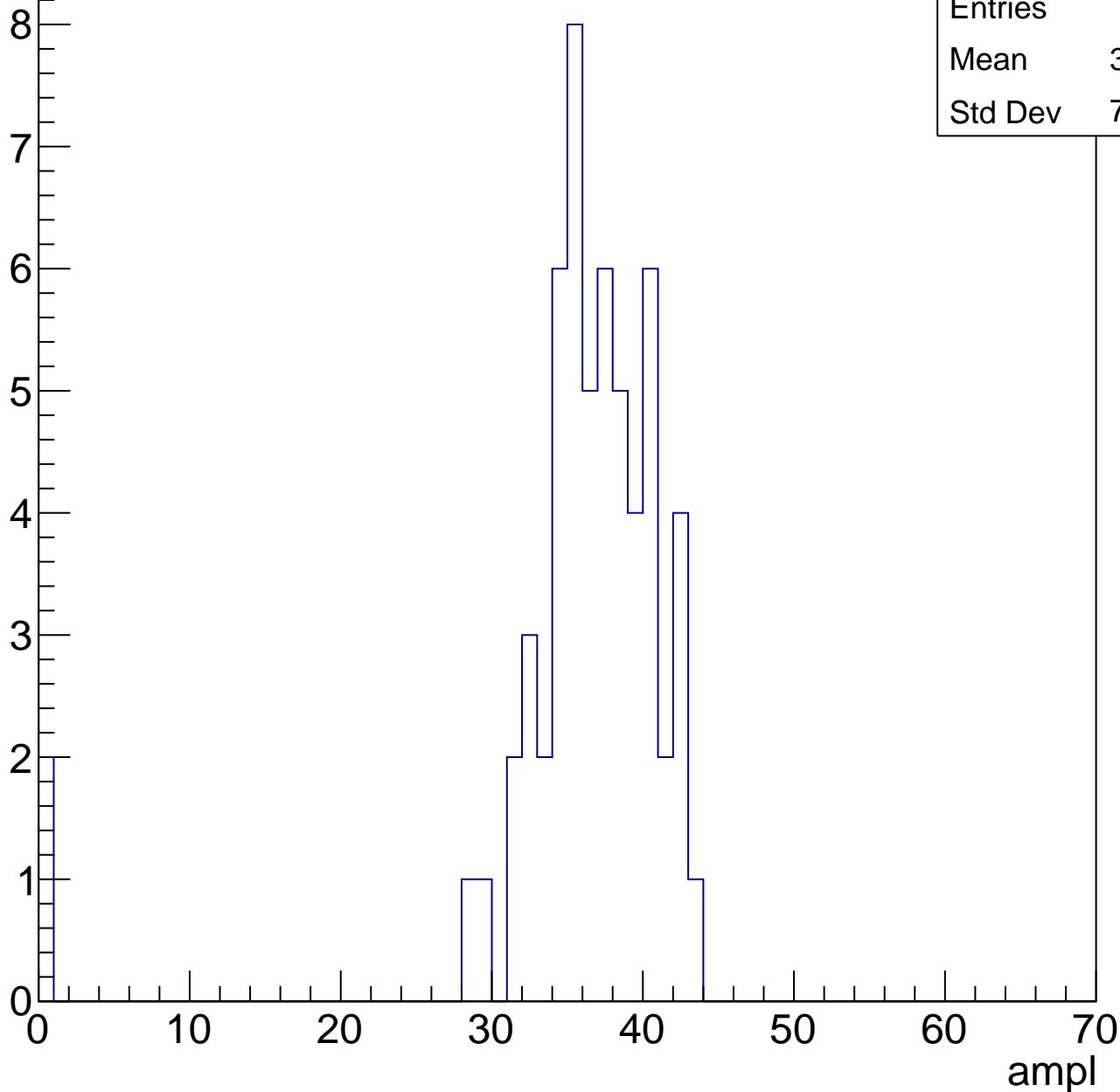


B1L103S, U23-ch3, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	35.28
Std Dev	7.455

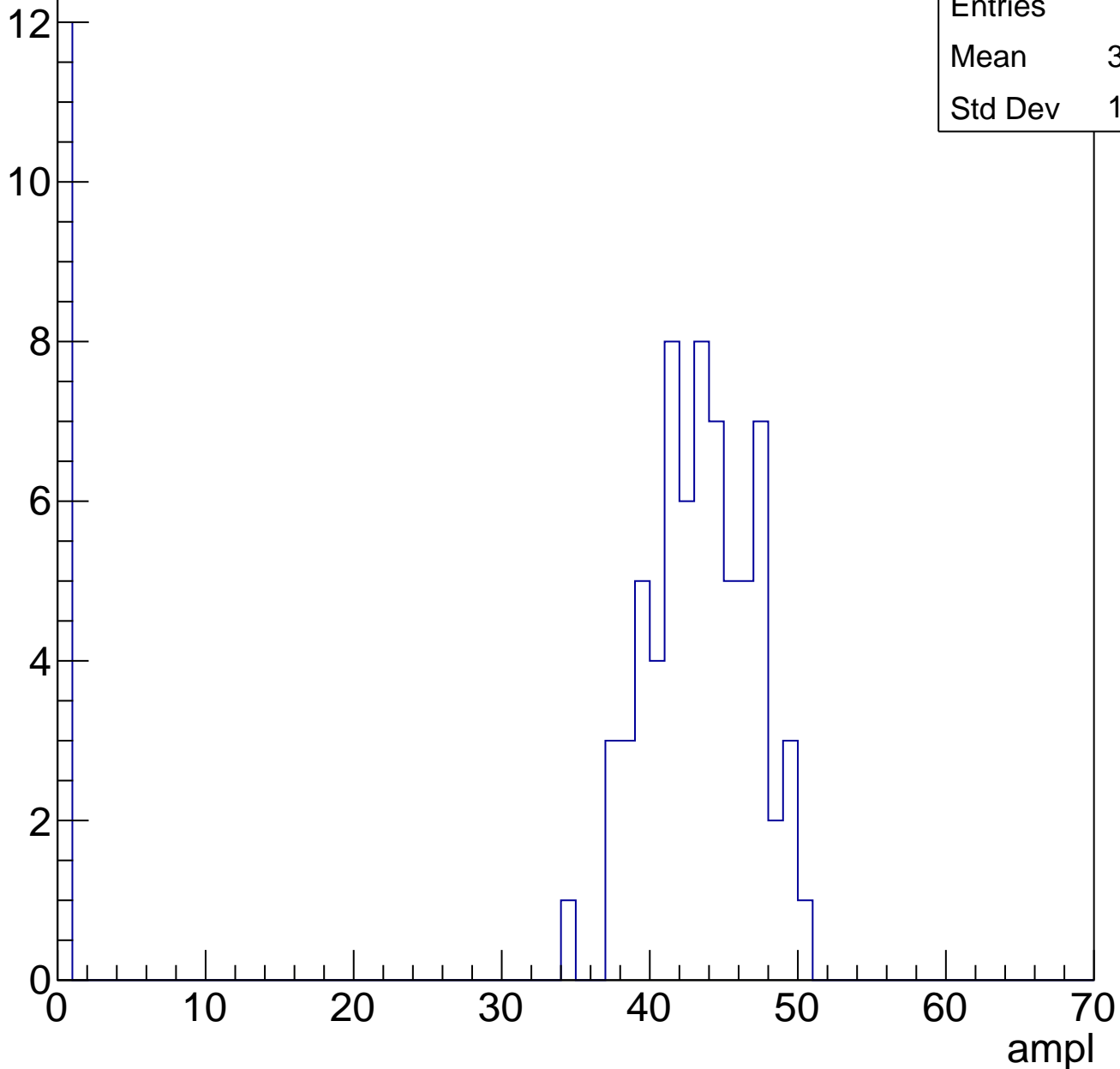


B1L103S, U23-ch3, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	80
Mean	36.54
Std Dev	15.67

Entry

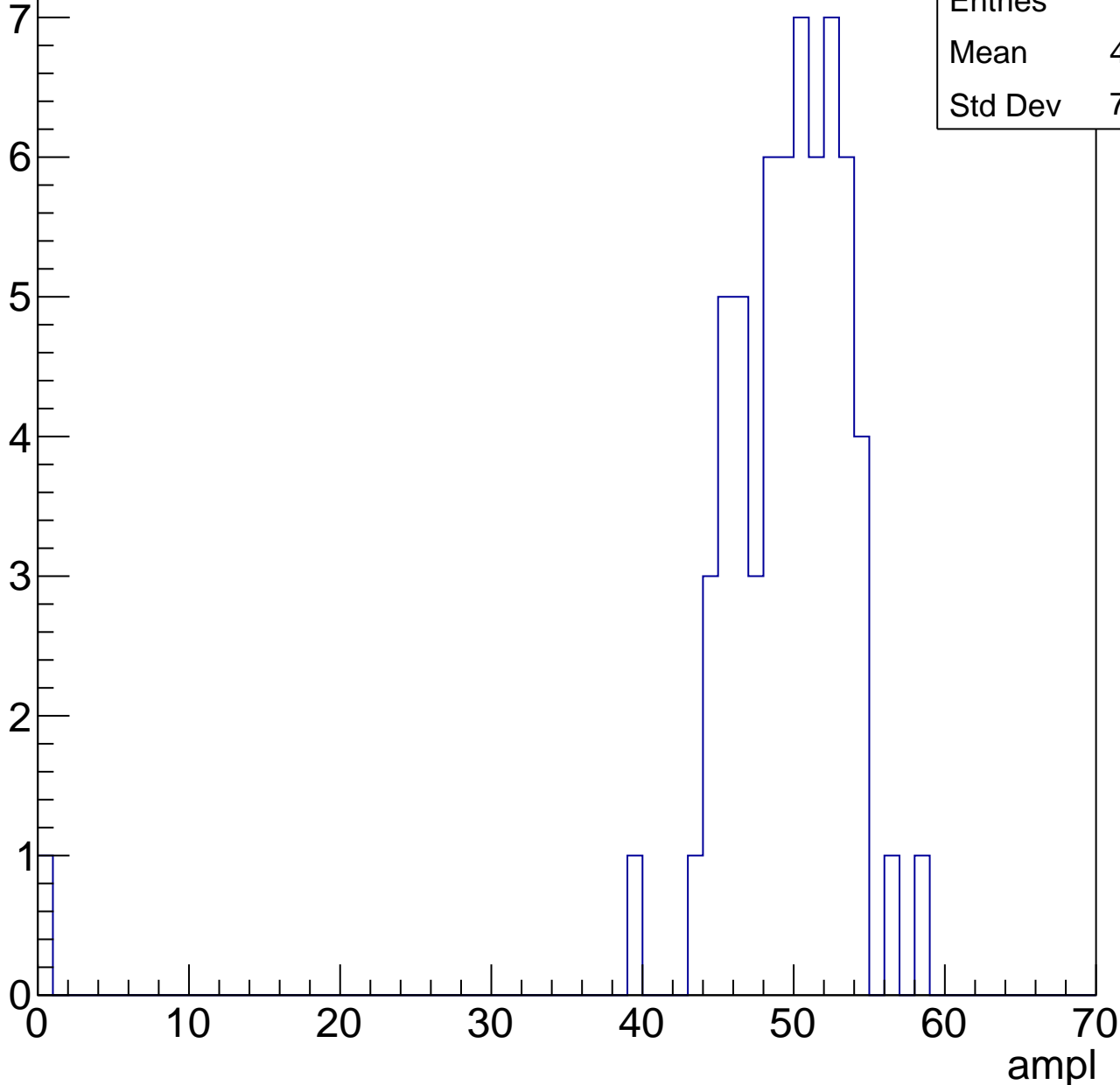


B1L103S, U23-ch3, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	63
Mean	48.57
Std Dev	7.086

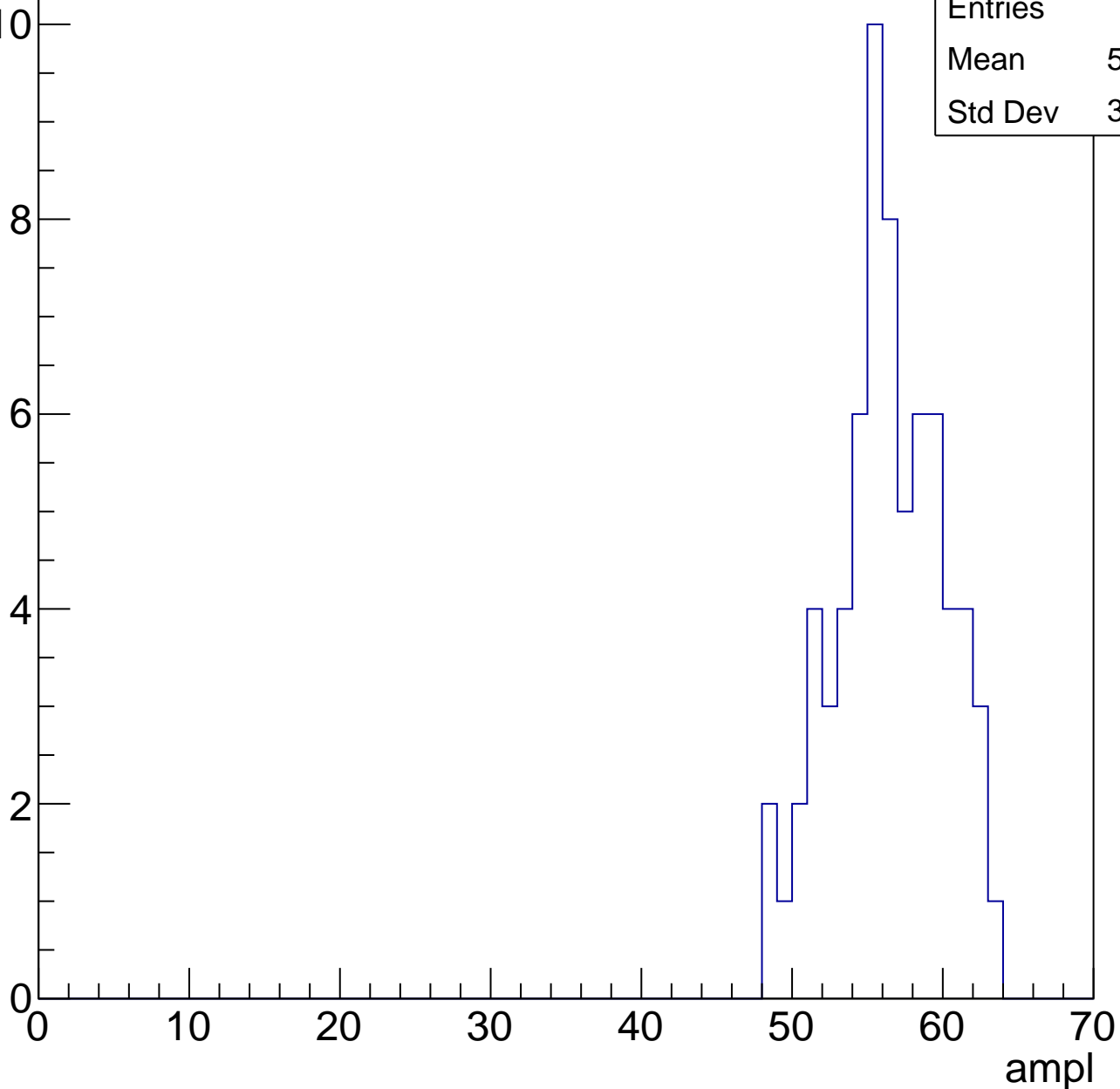


B1L103S, U23-ch3, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	55.93
Std Dev	3.552

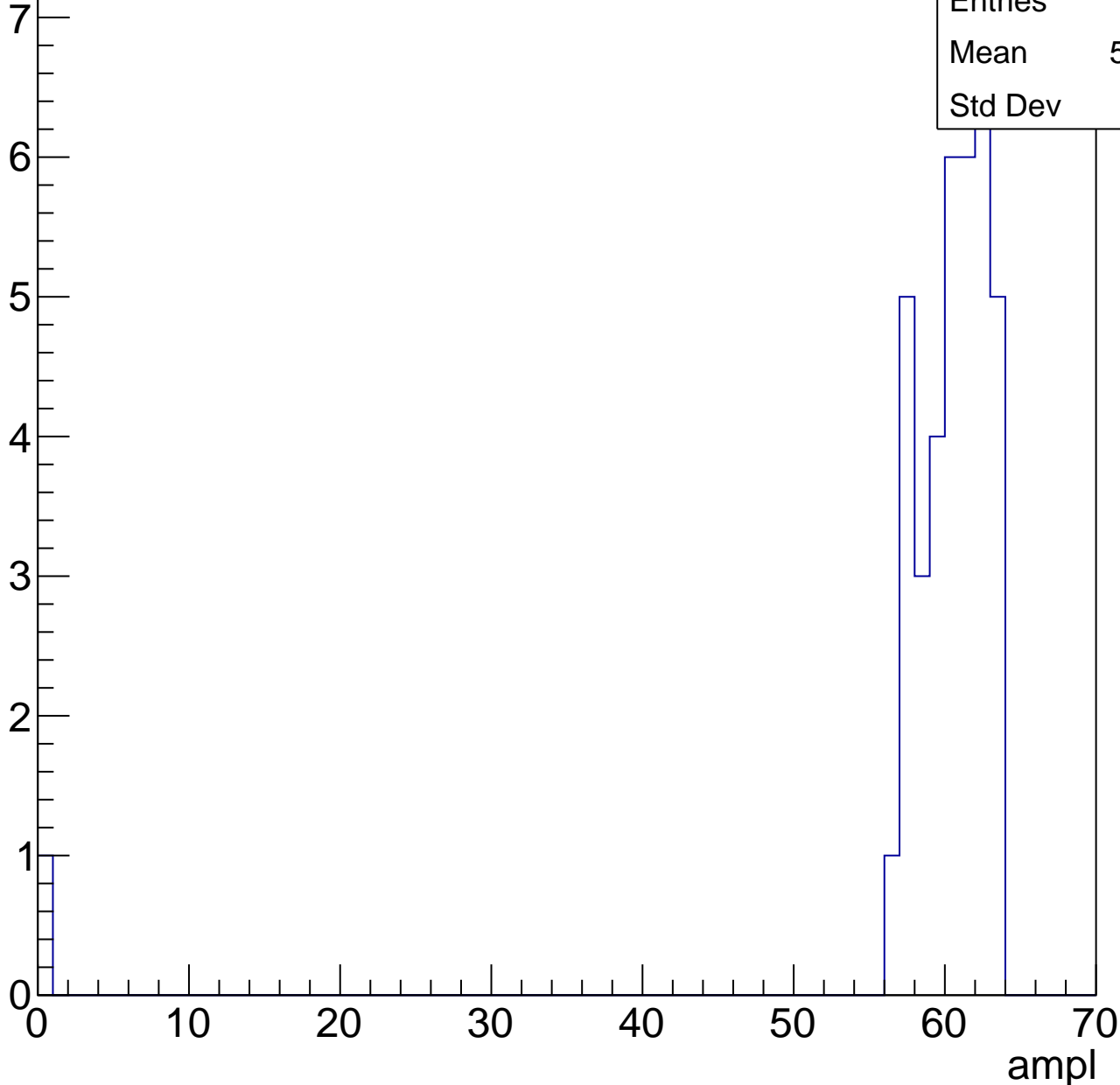


B1L103S, U23-ch3, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

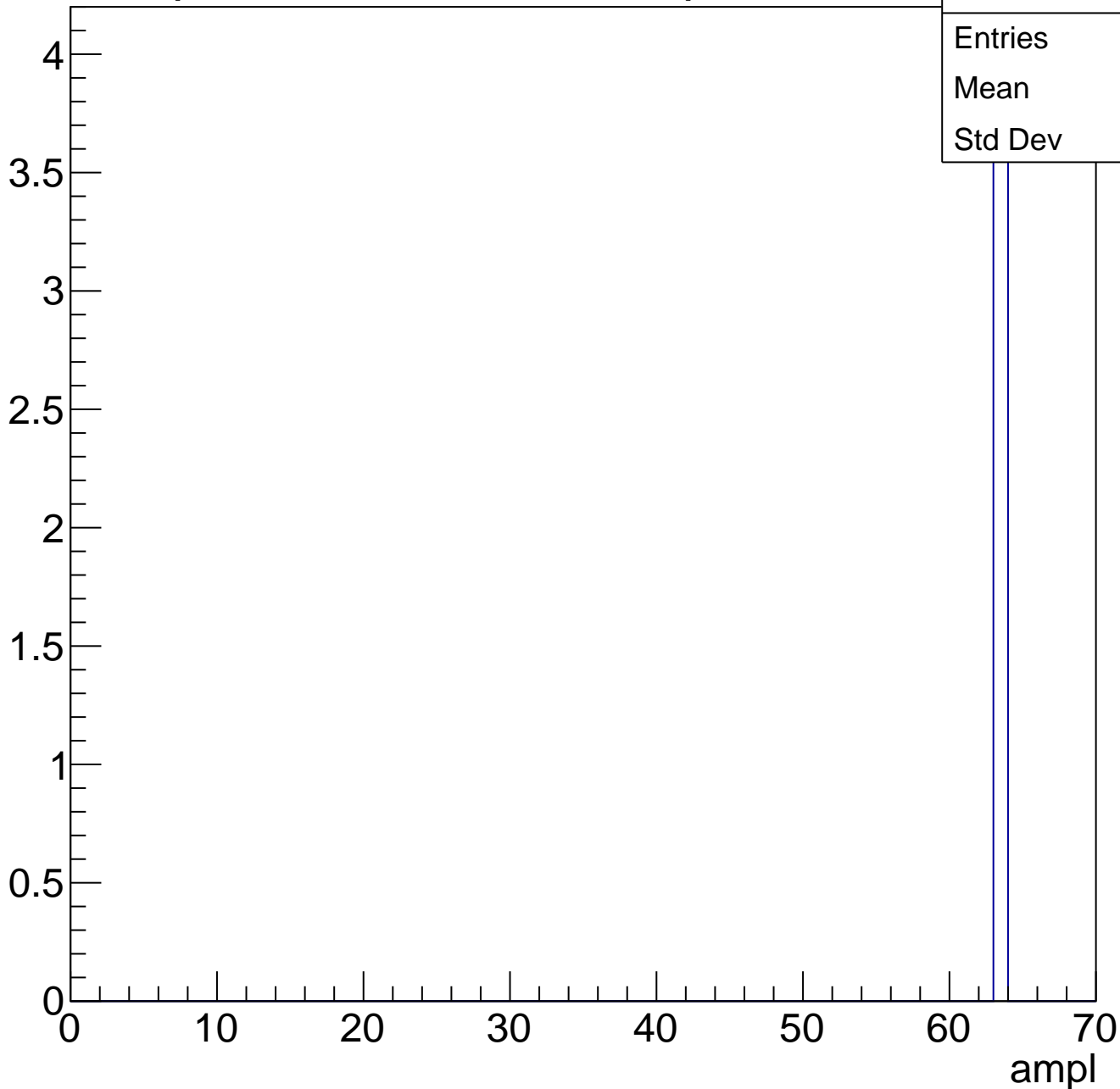
Entries	38
Mean	58.58
Std Dev	9.84



B1L103S, U23-ch3, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch3, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

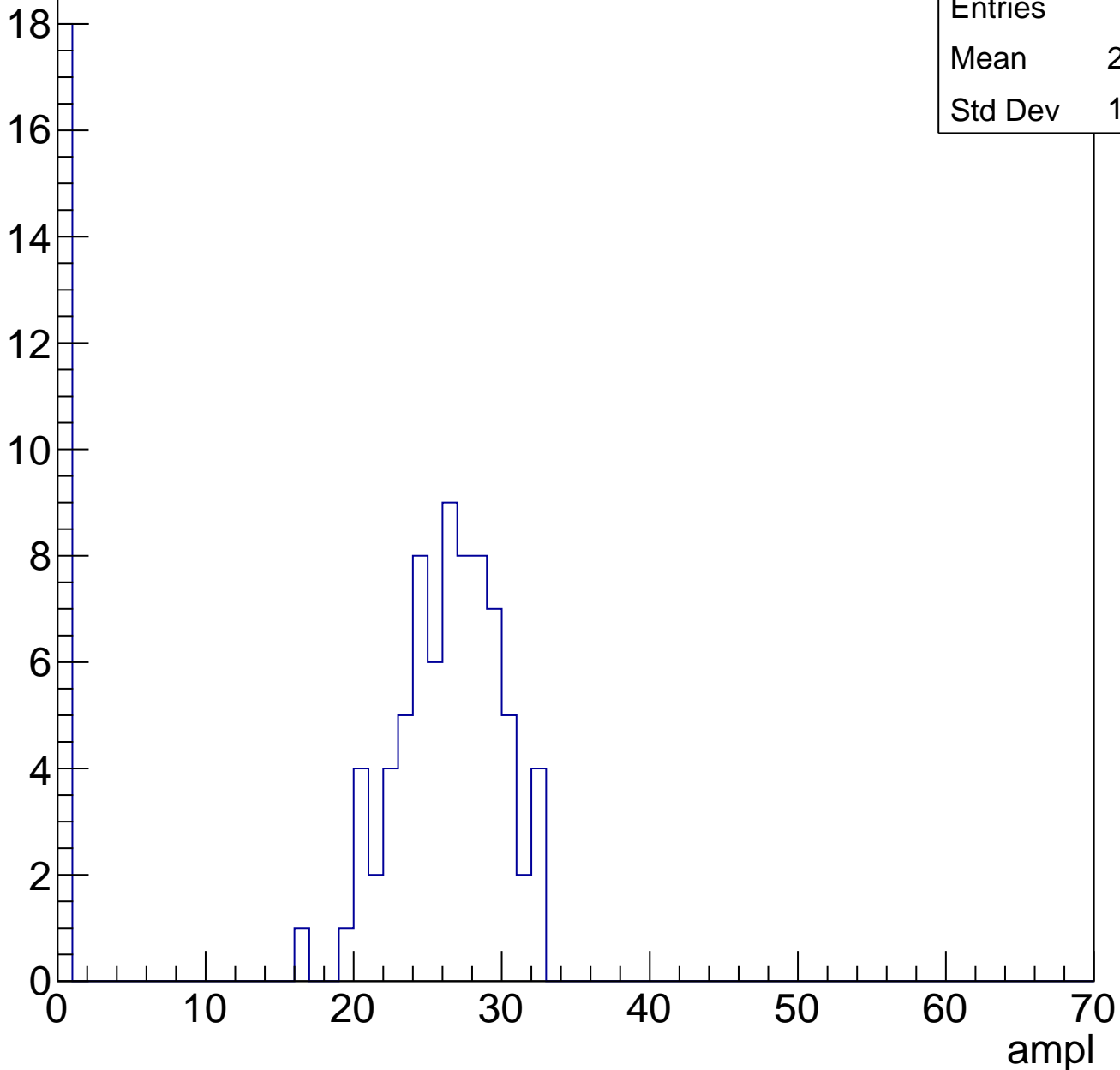
ampl

B1L103S, U23-ch4, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	92
Mean	20.86
Std Dev	10.74

Entry



B1L103S, U23-ch4, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	99
Mean	29.94
Std Dev	12.19

Entry

12

10

8

6

4

2

0

0

10

20

30

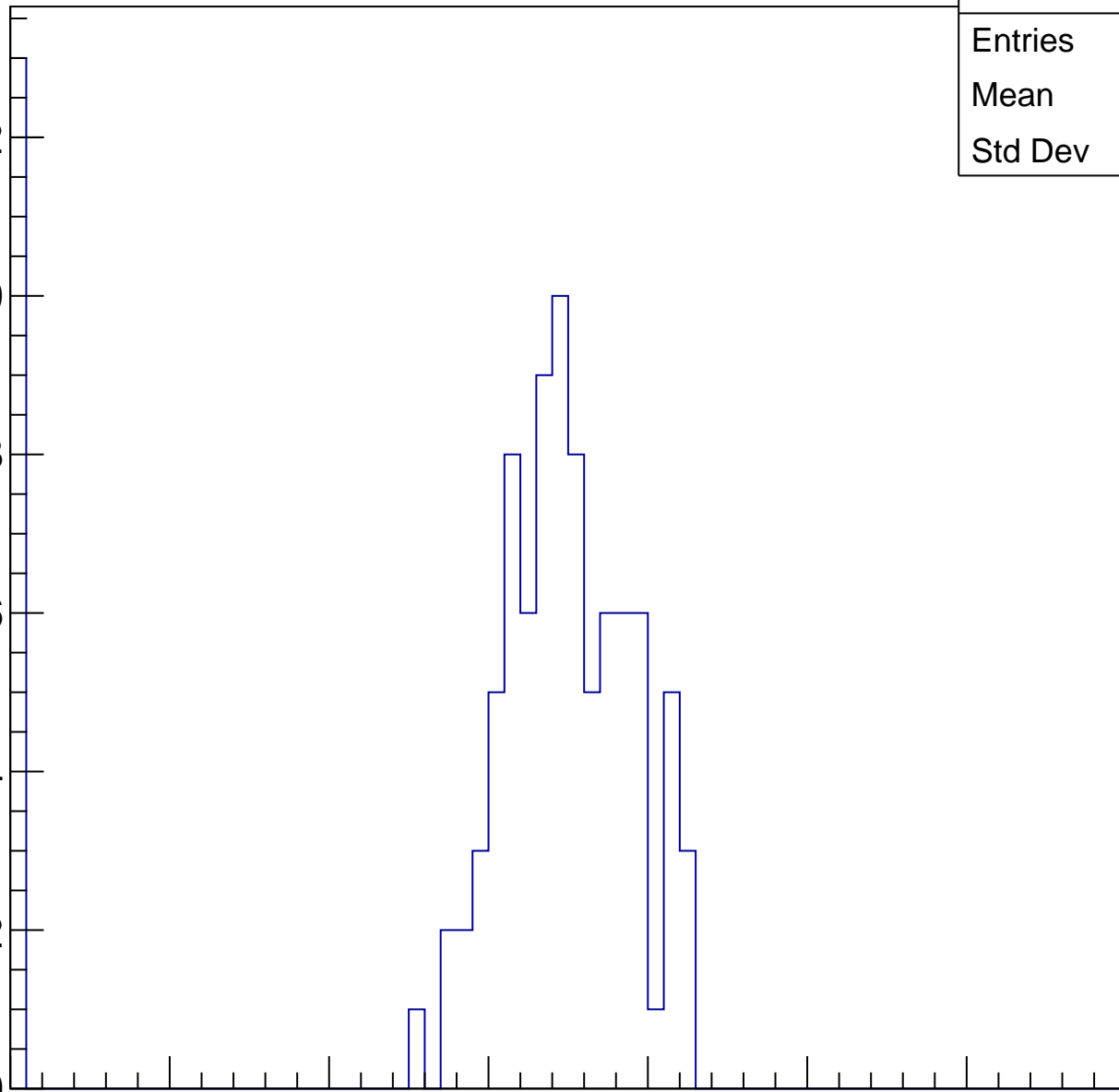
40

50

60

70

ampl

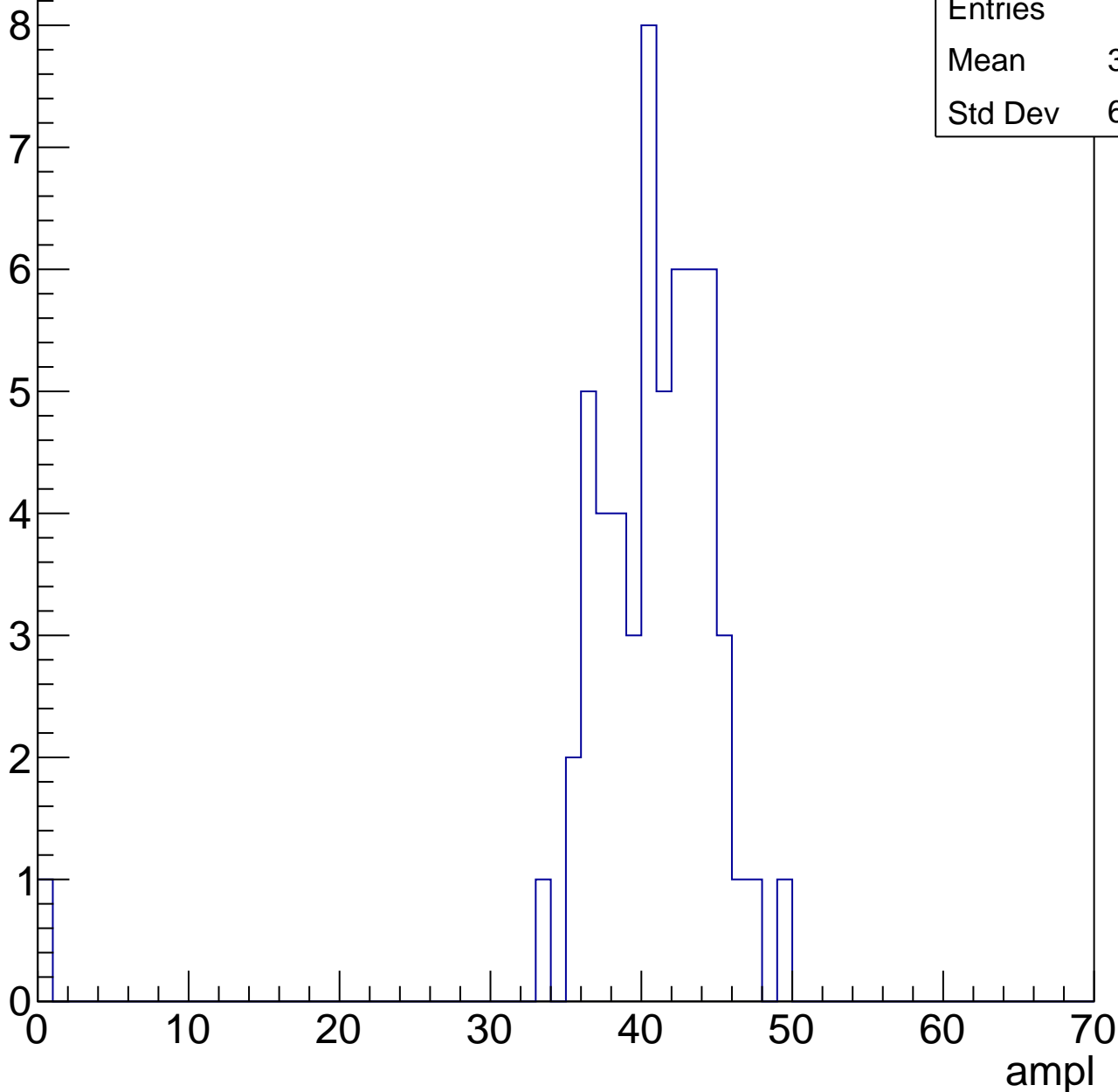


B1L103S, U23-ch4, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	57
Mean	39.93
Std Dev	6.288

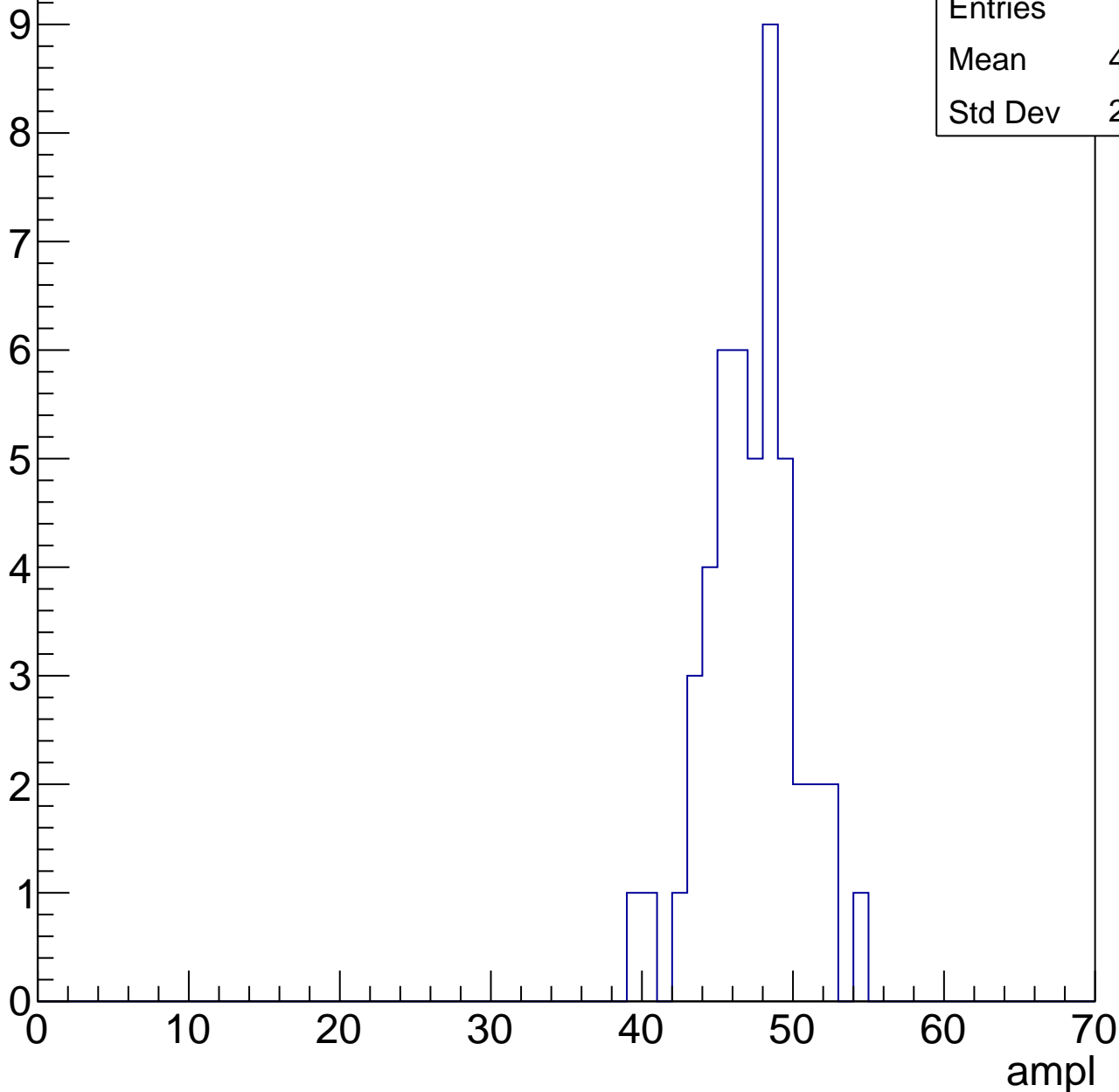


B1L103S, U23-ch4, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	48
Mean	46.75
Std Dev	2.983

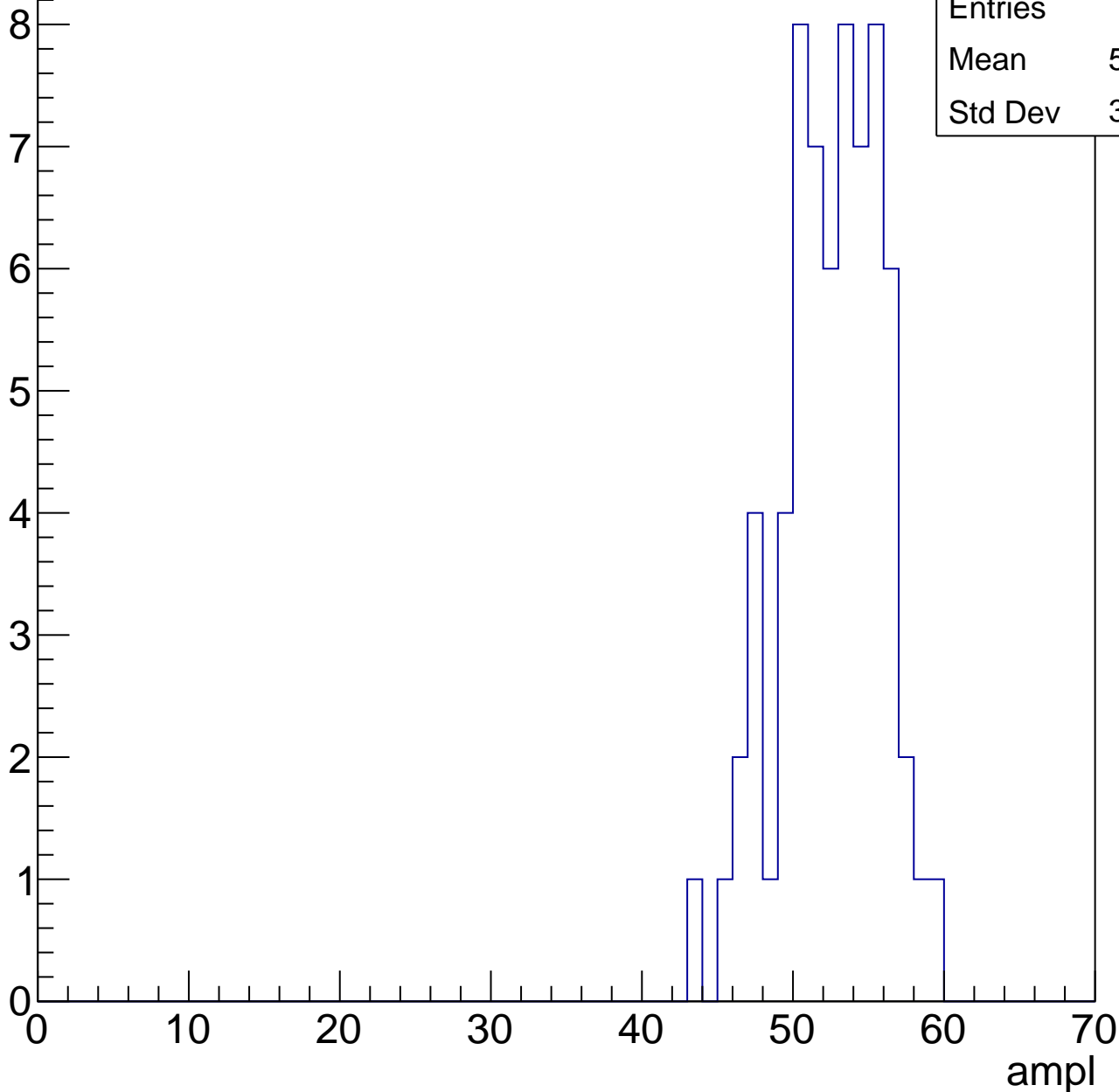


B1L103S, U23-ch4, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

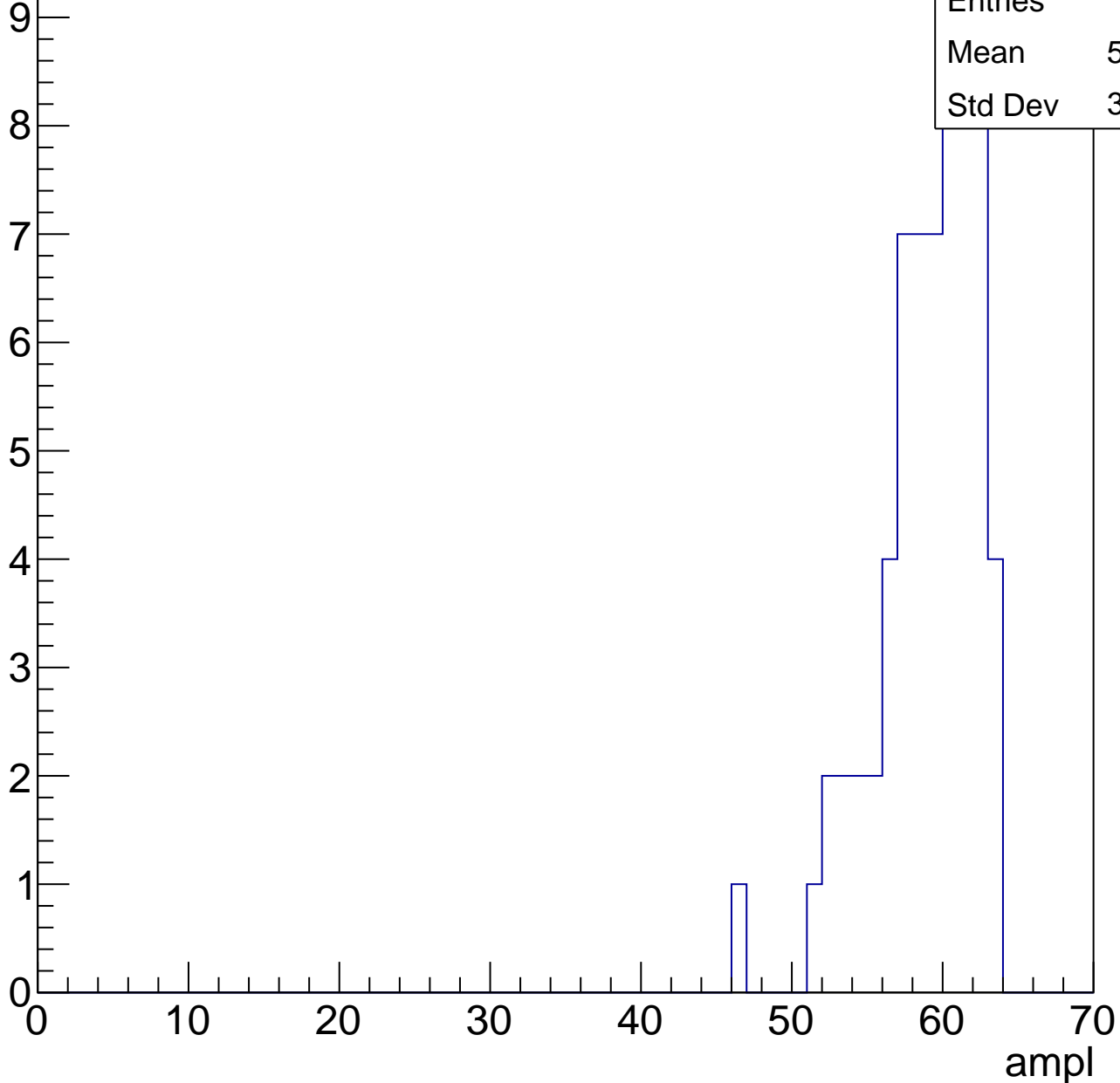
Entries	67
Mean	52.09
Std Dev	3.304



B1L103S, U23-ch4, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

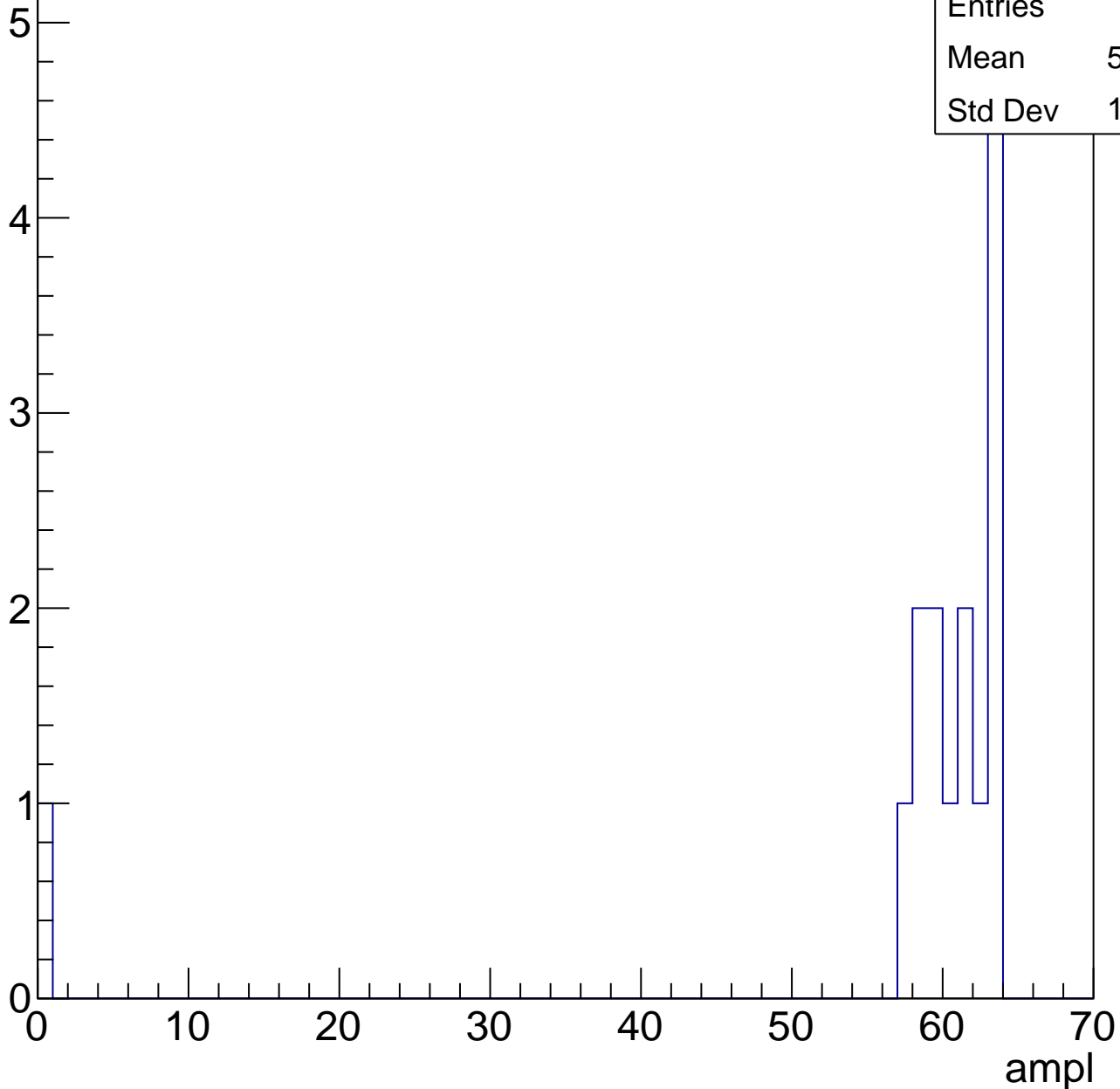


B1L103S, U23-ch4, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	15
Mean	56.67
Std Dev	15.28

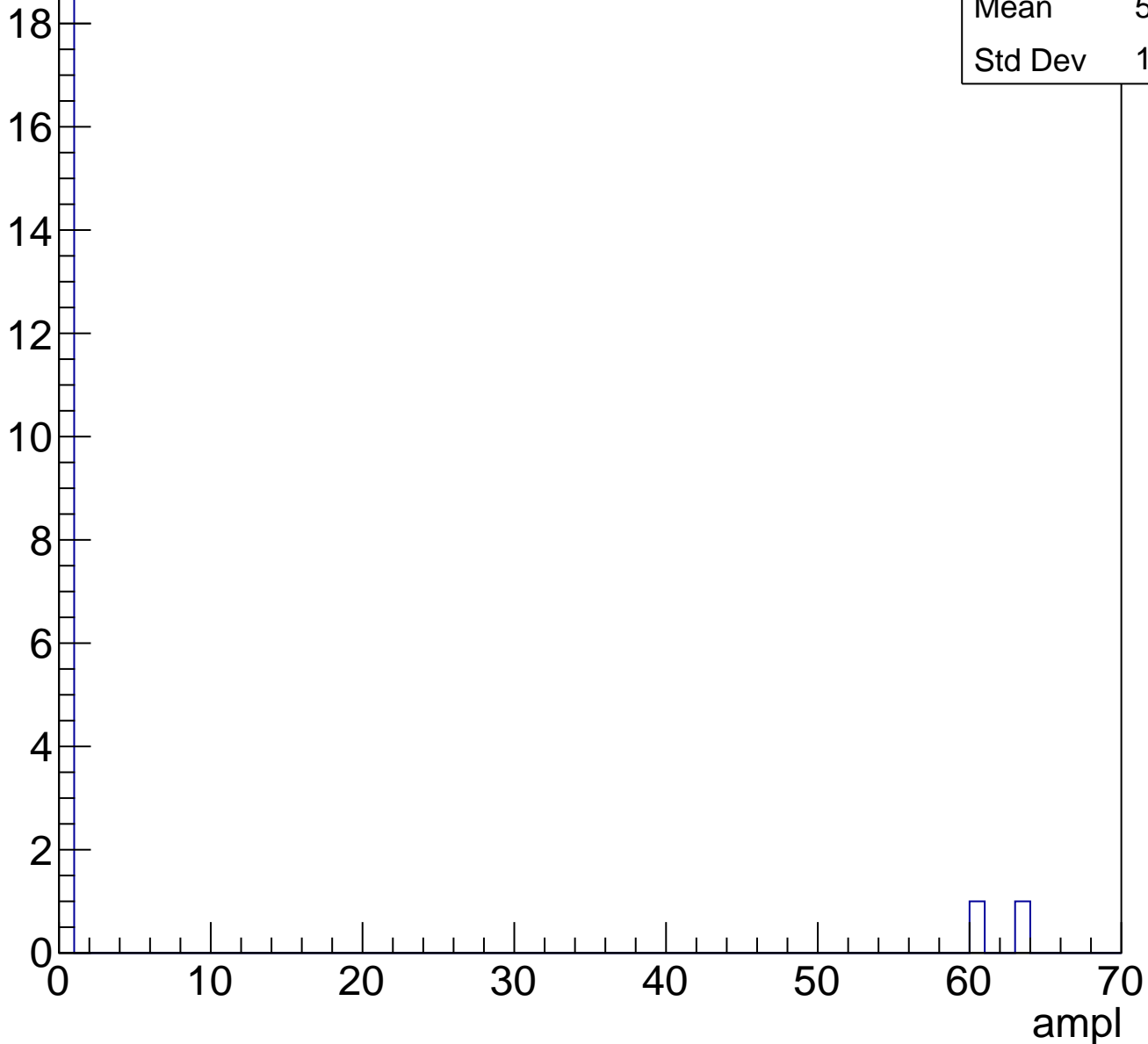


B1L103S, U23-ch4, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	21
Mean	5.857
Std Dev	18.06

Entry

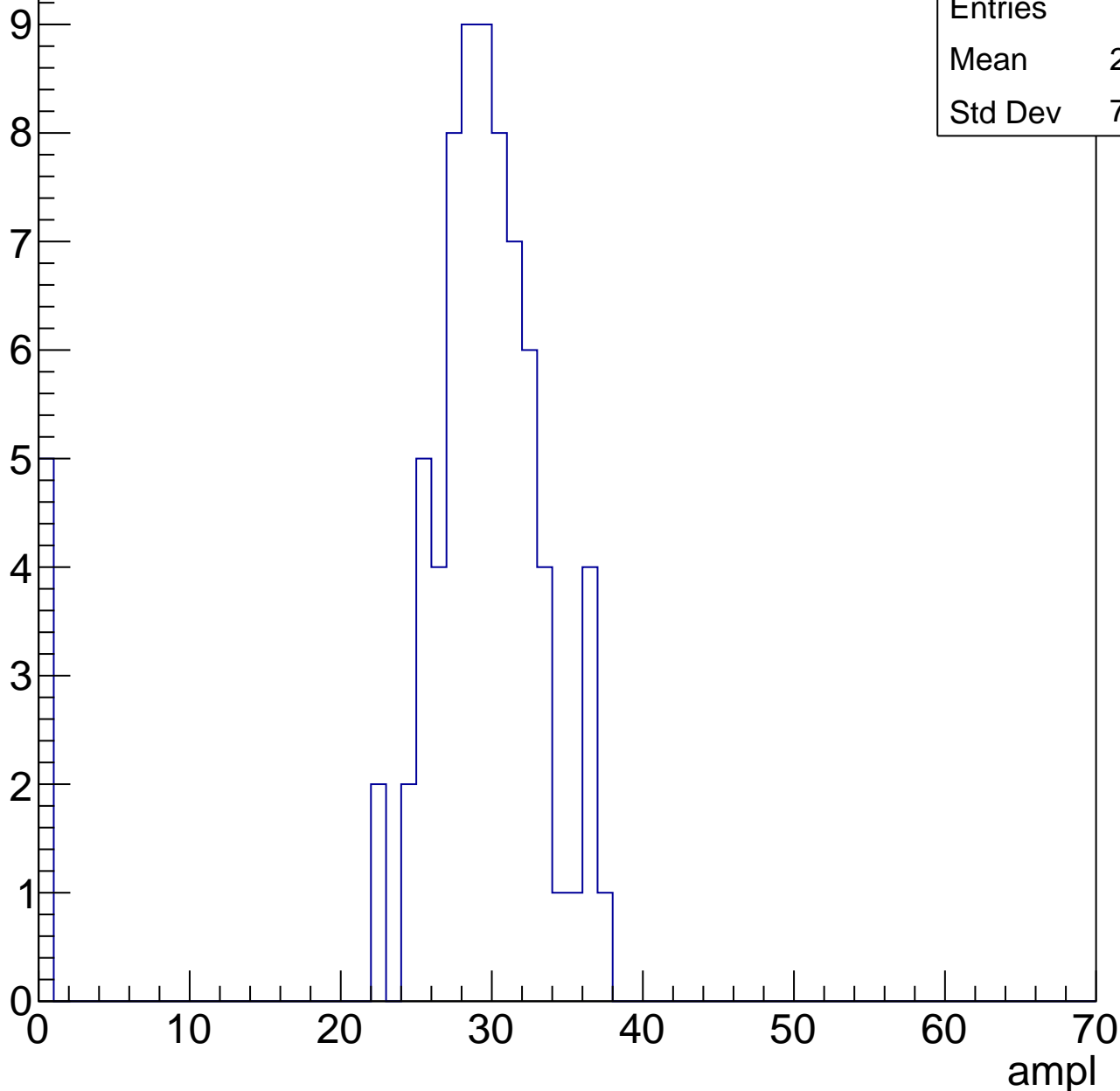


B1L103S, U23-ch5, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

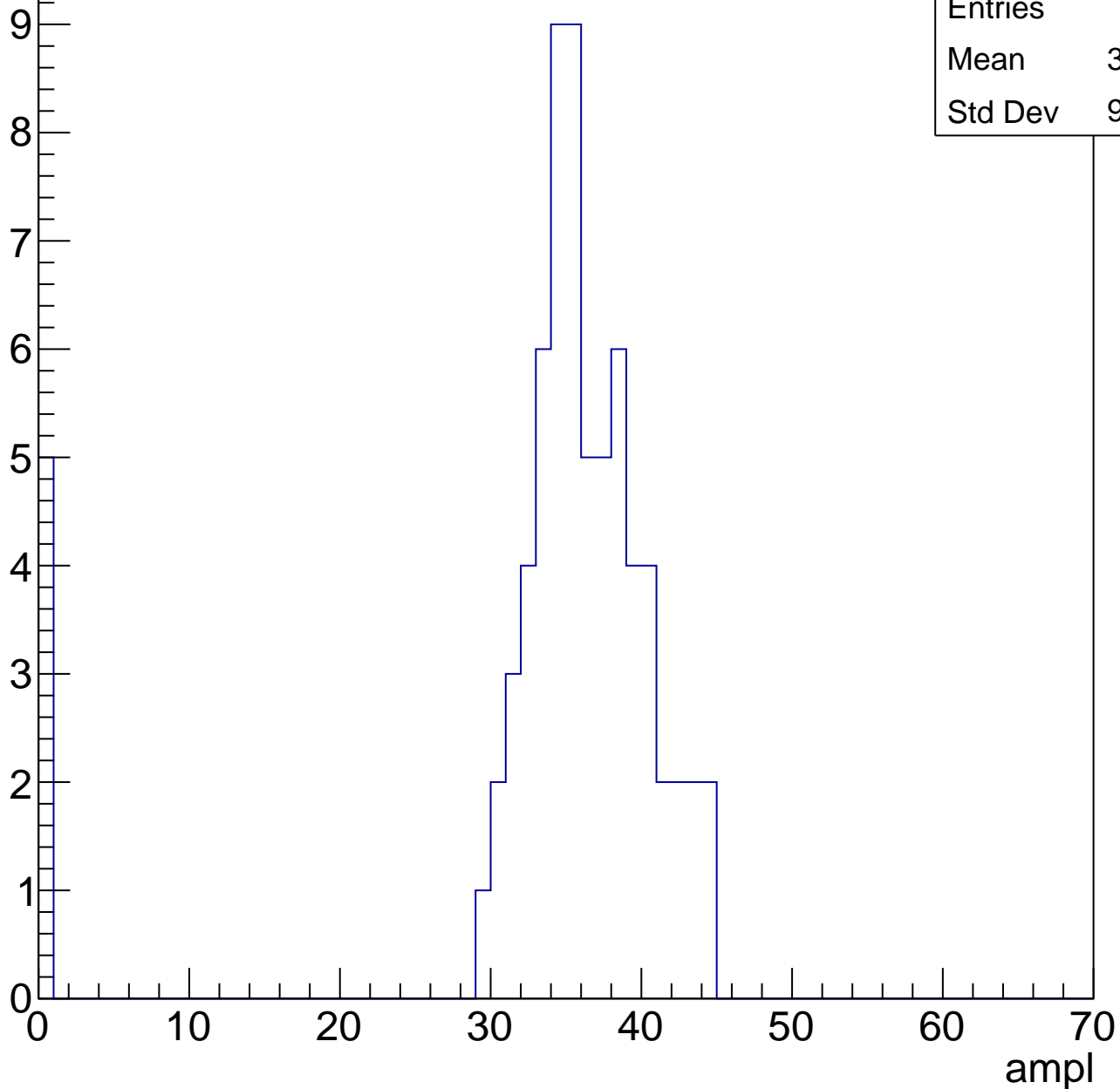
Entries	76
Mean	27.38
Std Dev	7.936



B1L103S, U23-ch5, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry



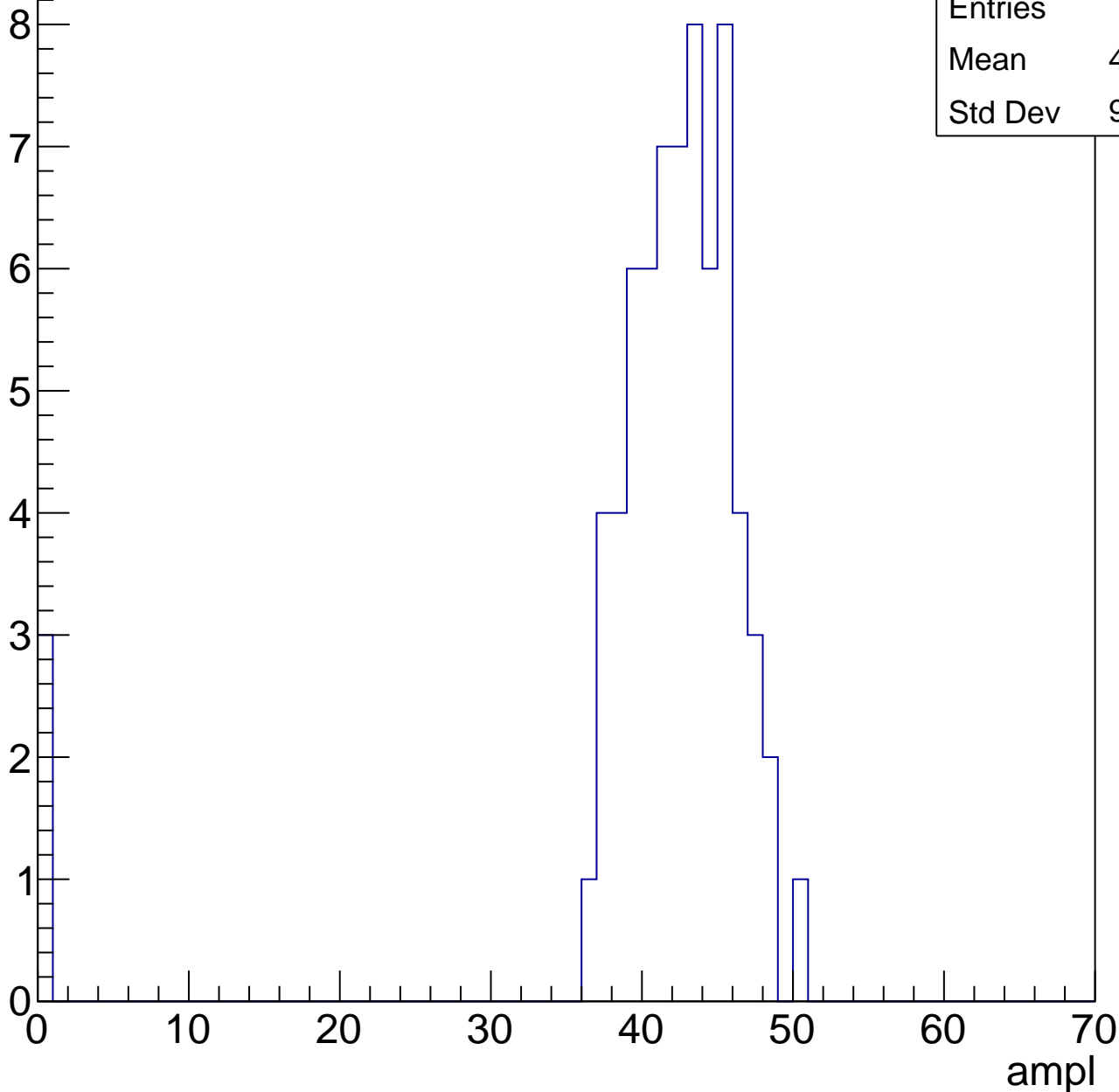
Entries	71
Mean	33.49
Std Dev	9.837

B1L103S, U23-ch5, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	40.43
Std Dev	9.089



B1L103S, U23-ch5, adc3

calib_packv5_041523_1651.root, FC#0, port C2

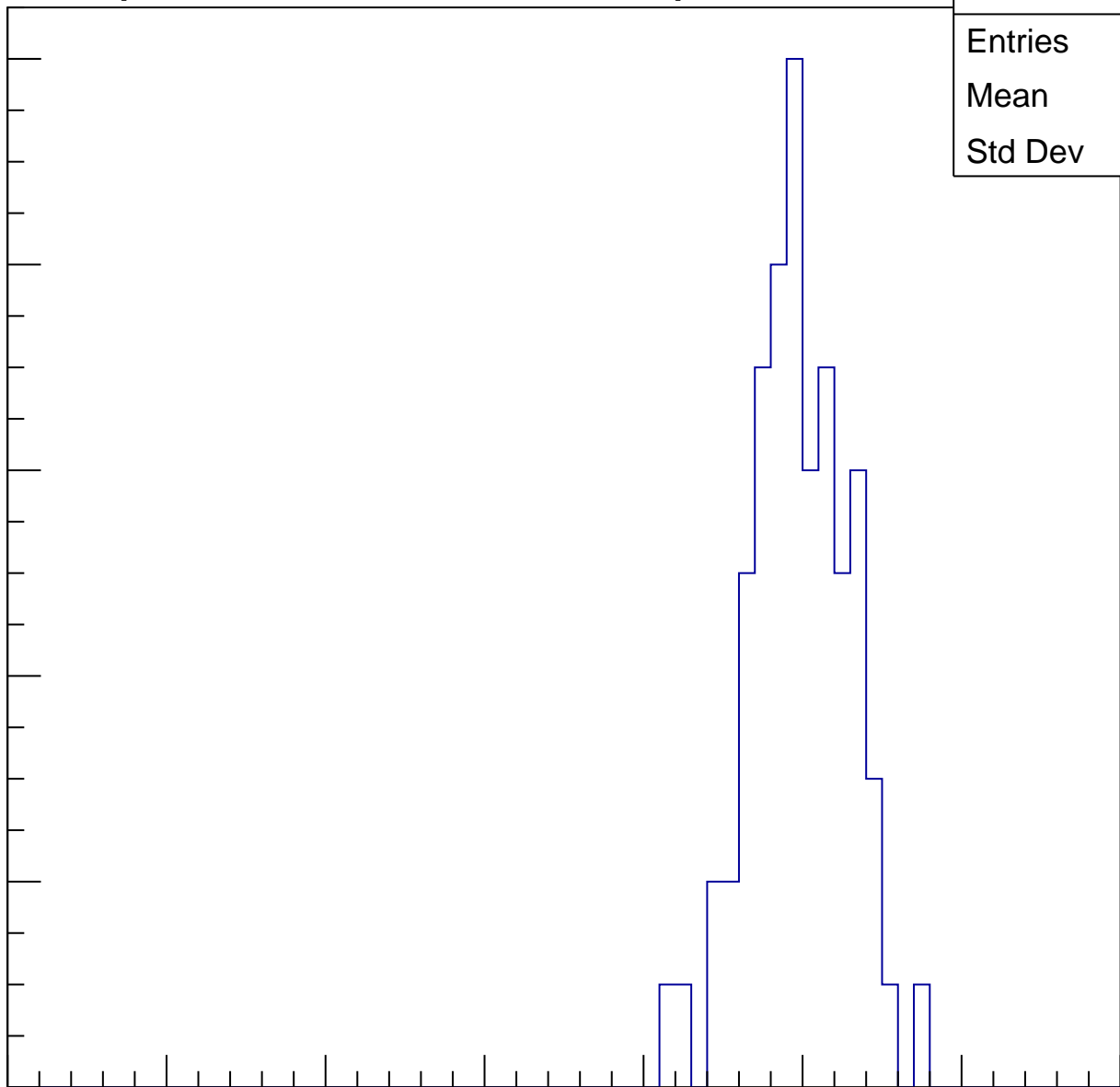
Entries	65
Mean	49.28
Std Dev	3.091

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

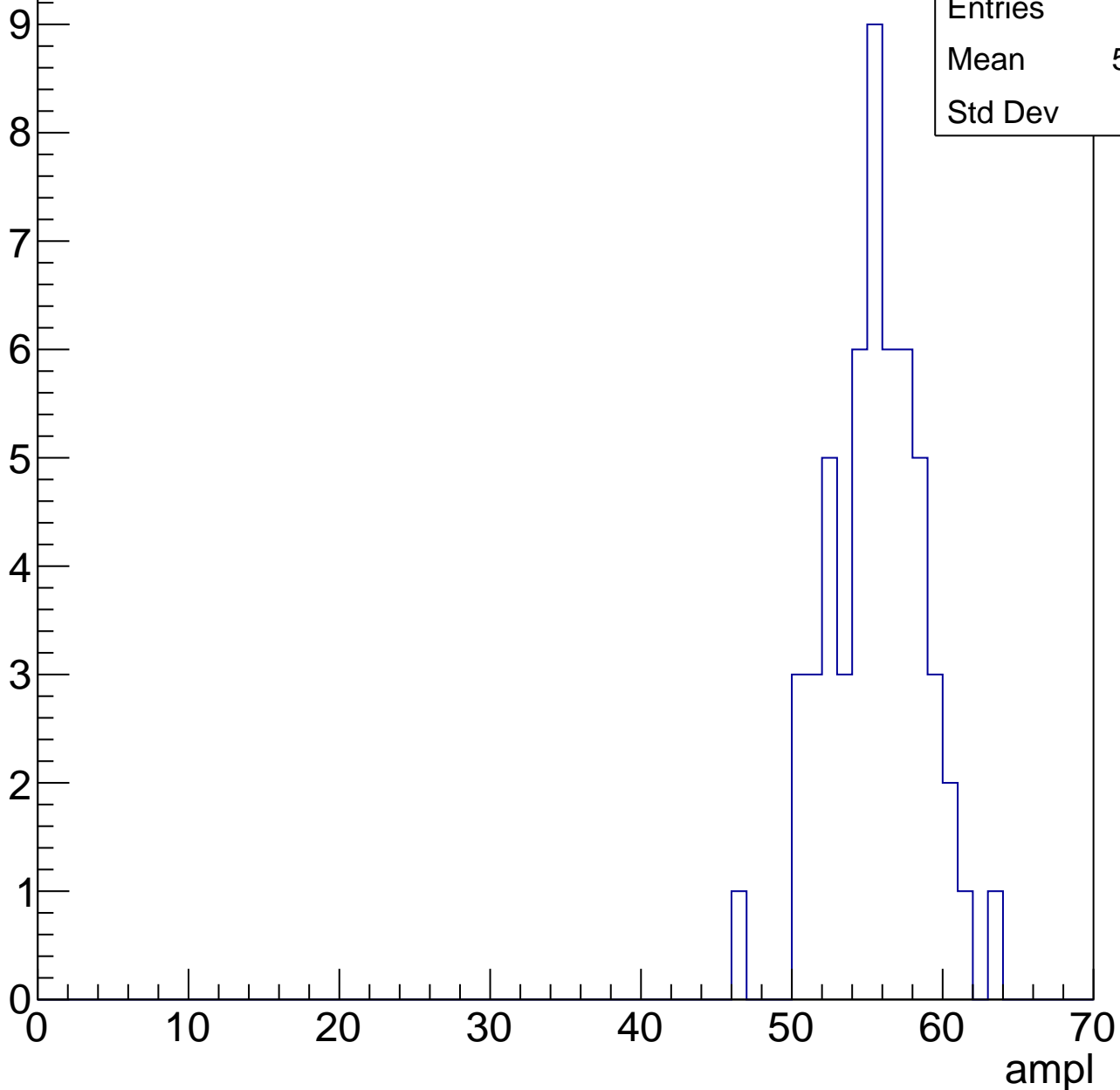
ampl



B1L103S, U23-ch5, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry



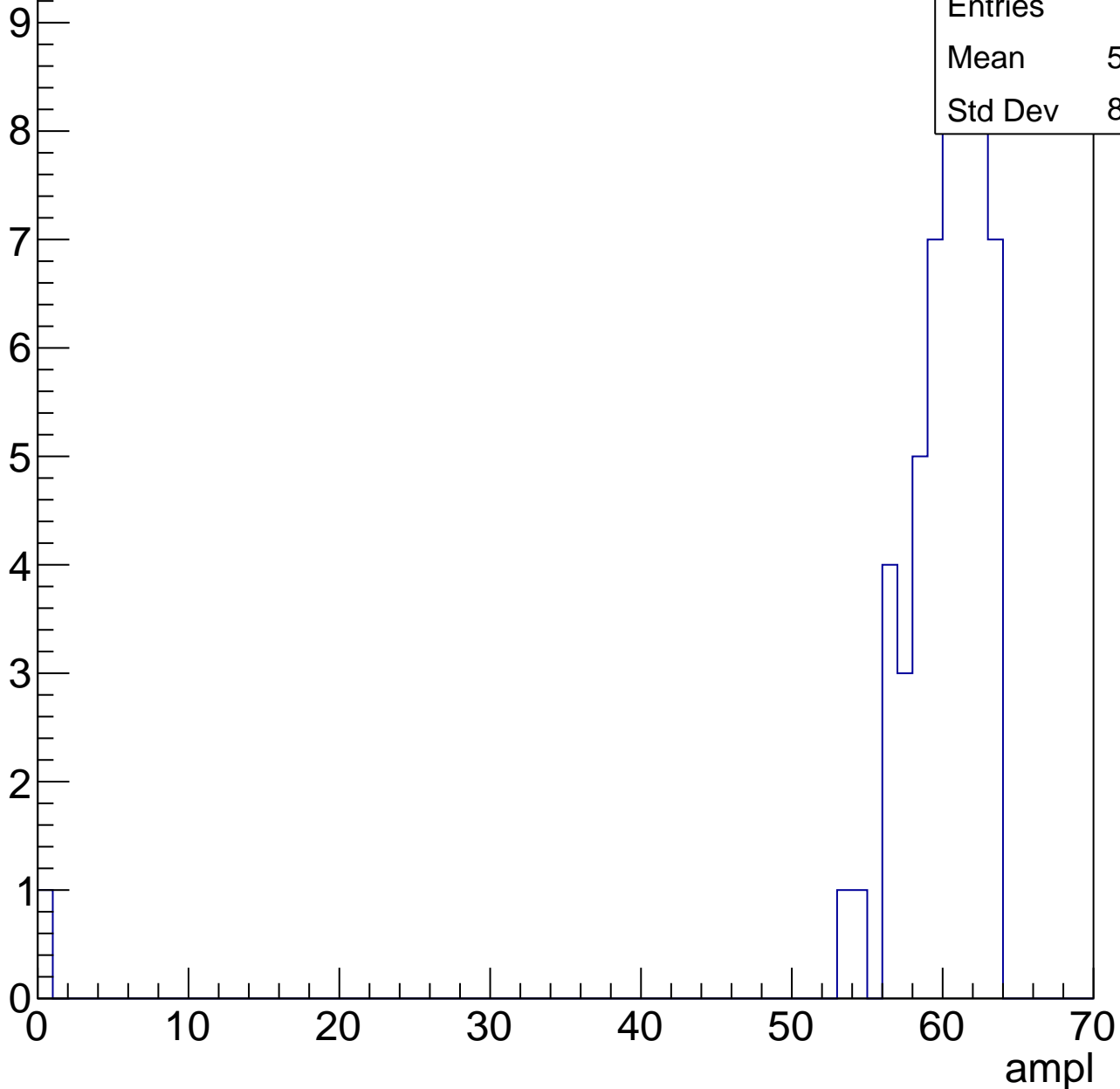
Entries	54
Mean	55.11
Std Dev	3.16

B1L103S, U23-ch5, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	54
Mean	58.74
Std Dev	8.416



B1L103S, U23-ch5, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch5, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

ampl

B1L103S, U23-ch6, adc0

calib_packv5_041523_1651.root, FC#0, port C2

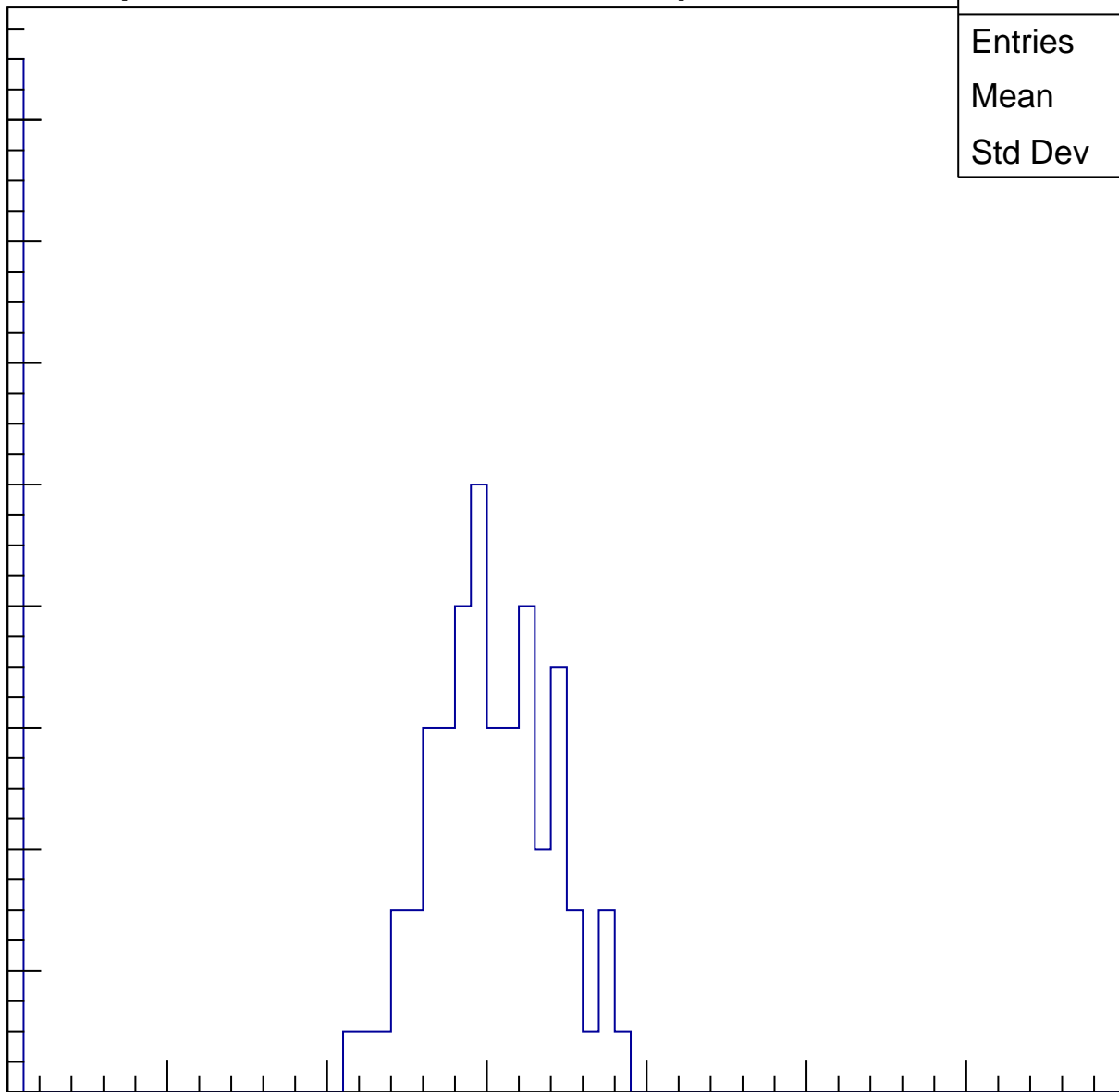
Entries	95
Mean	24.49
Std Dev	11.92

Entry

16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

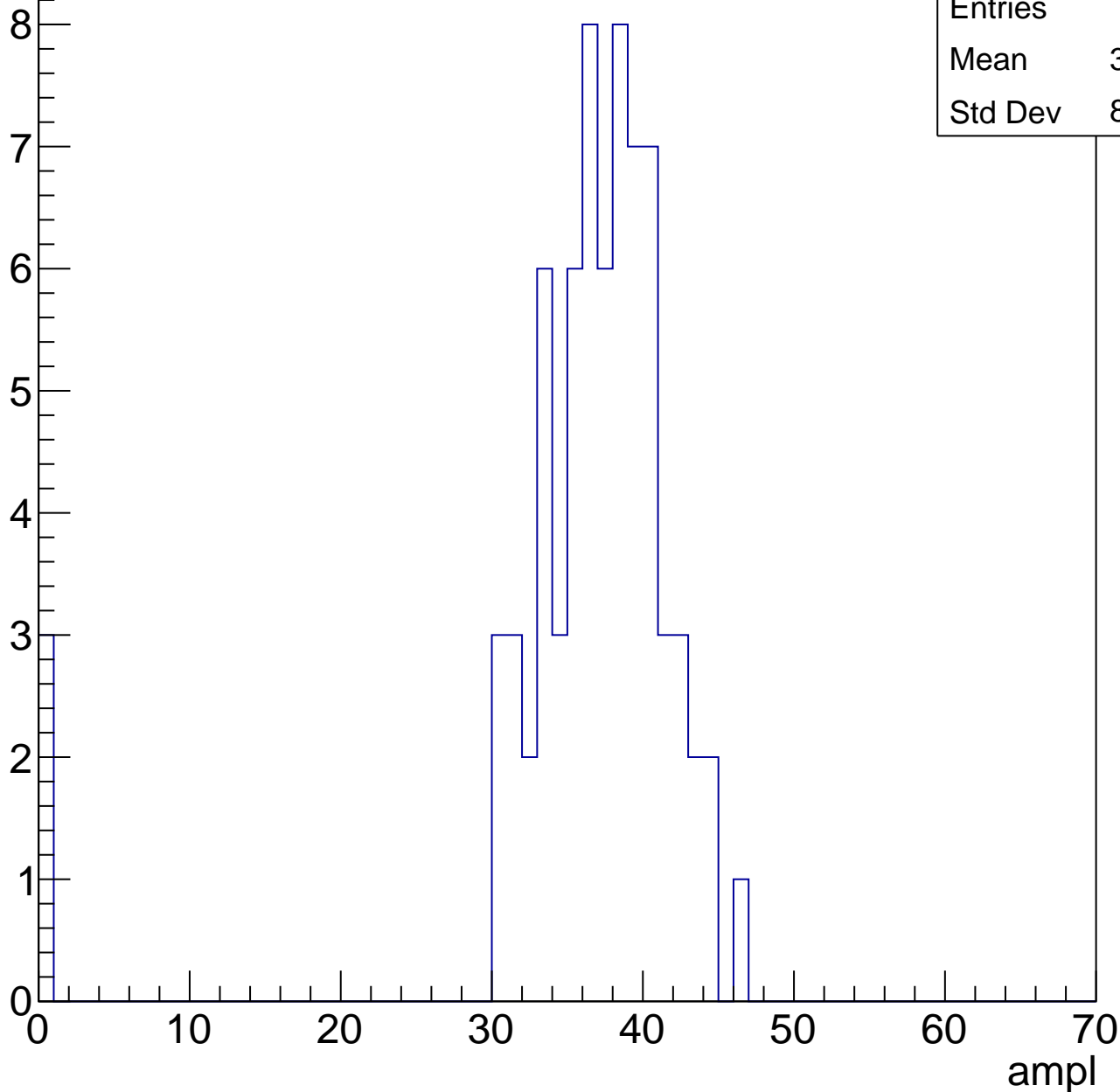


B1L103S, U23-ch6, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

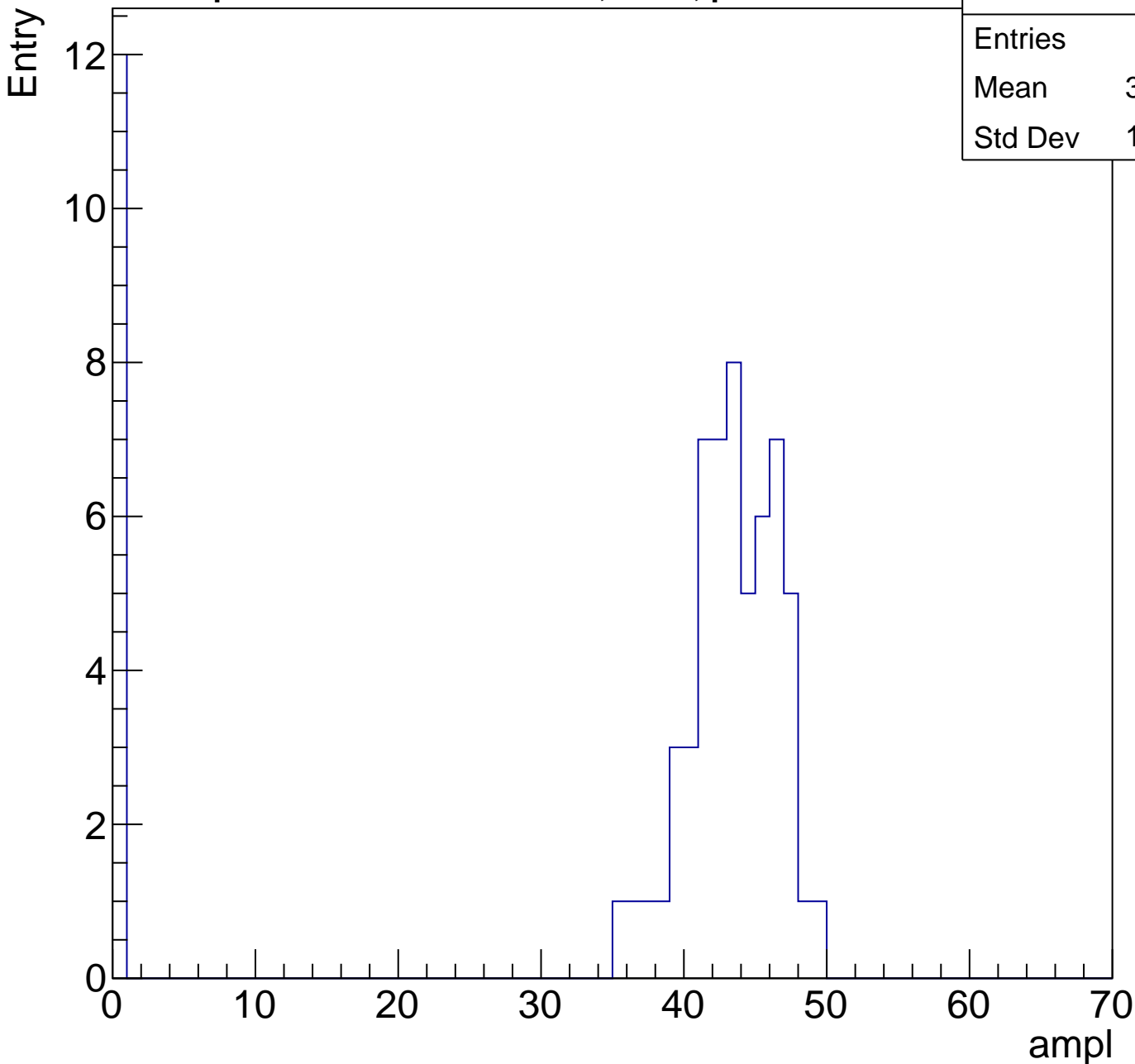
Entries	73
Mean	35.52
Std Dev	8.176



B1L103S, U23-ch6, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	69
Mean	35.54
Std Dev	16.53

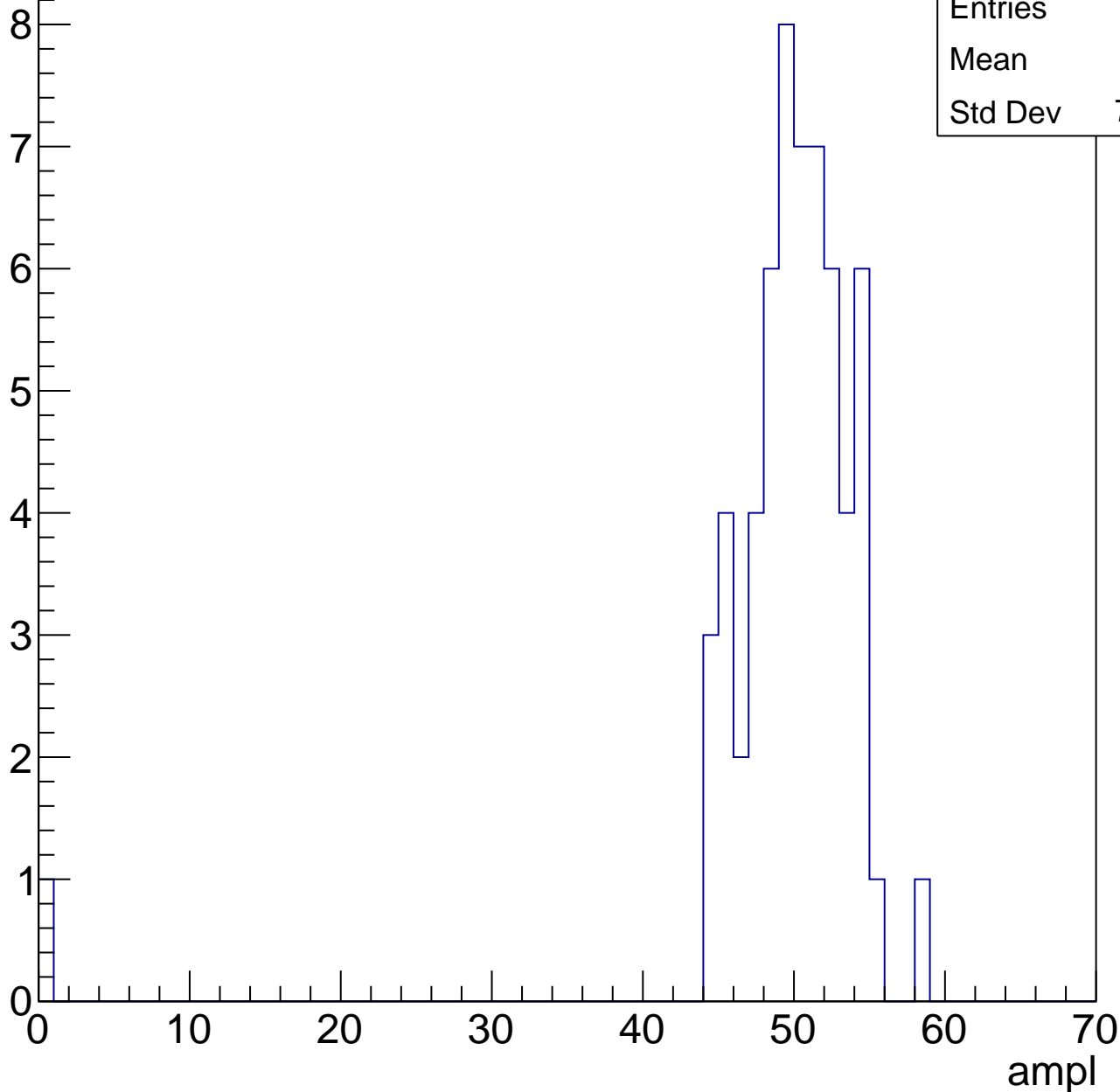


B1L103S, U23-ch6, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	49
Std Dev	7.071

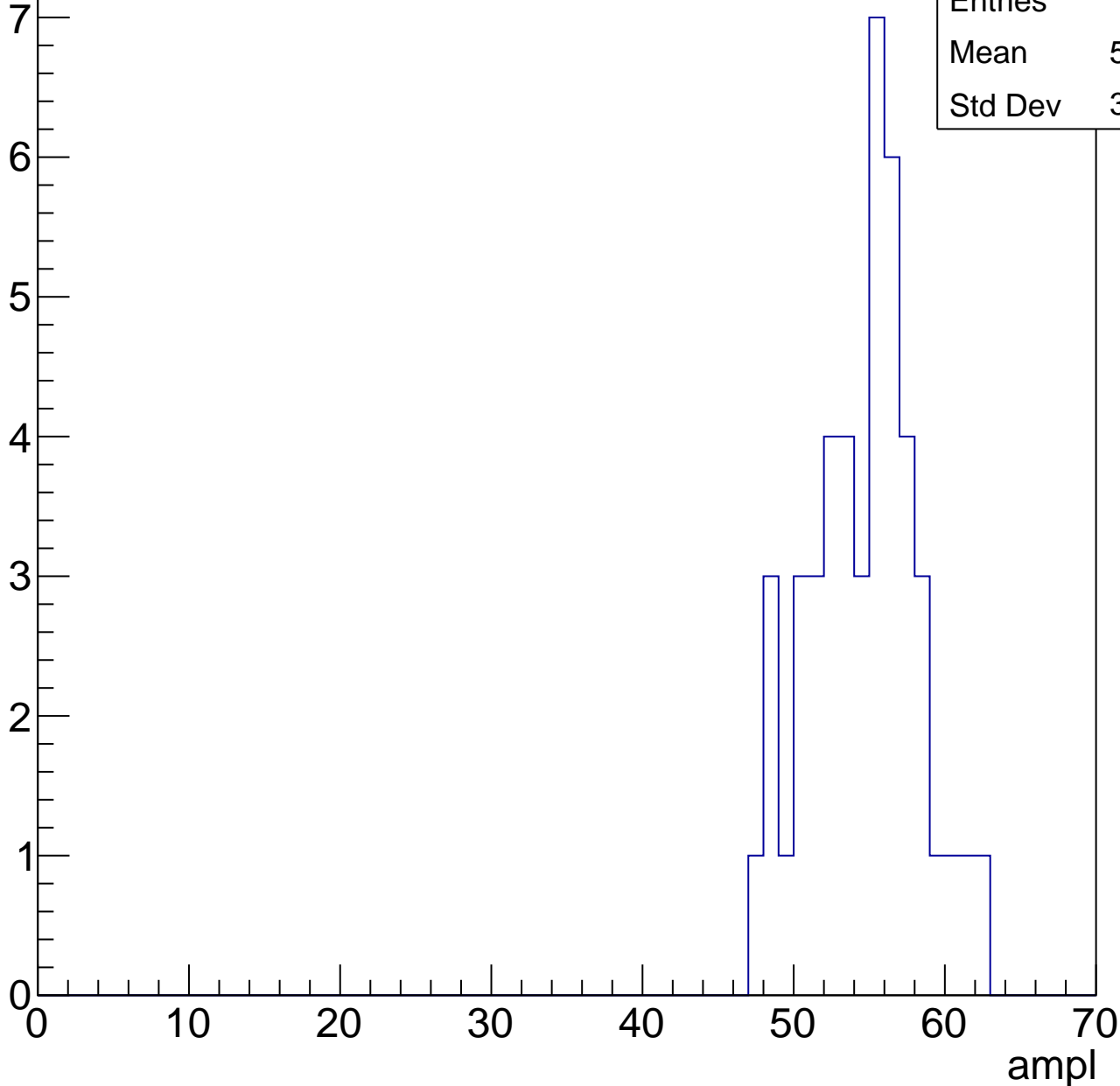


B1L103S, U23-ch6, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	46
Mean	54.13
Std Dev	3.505

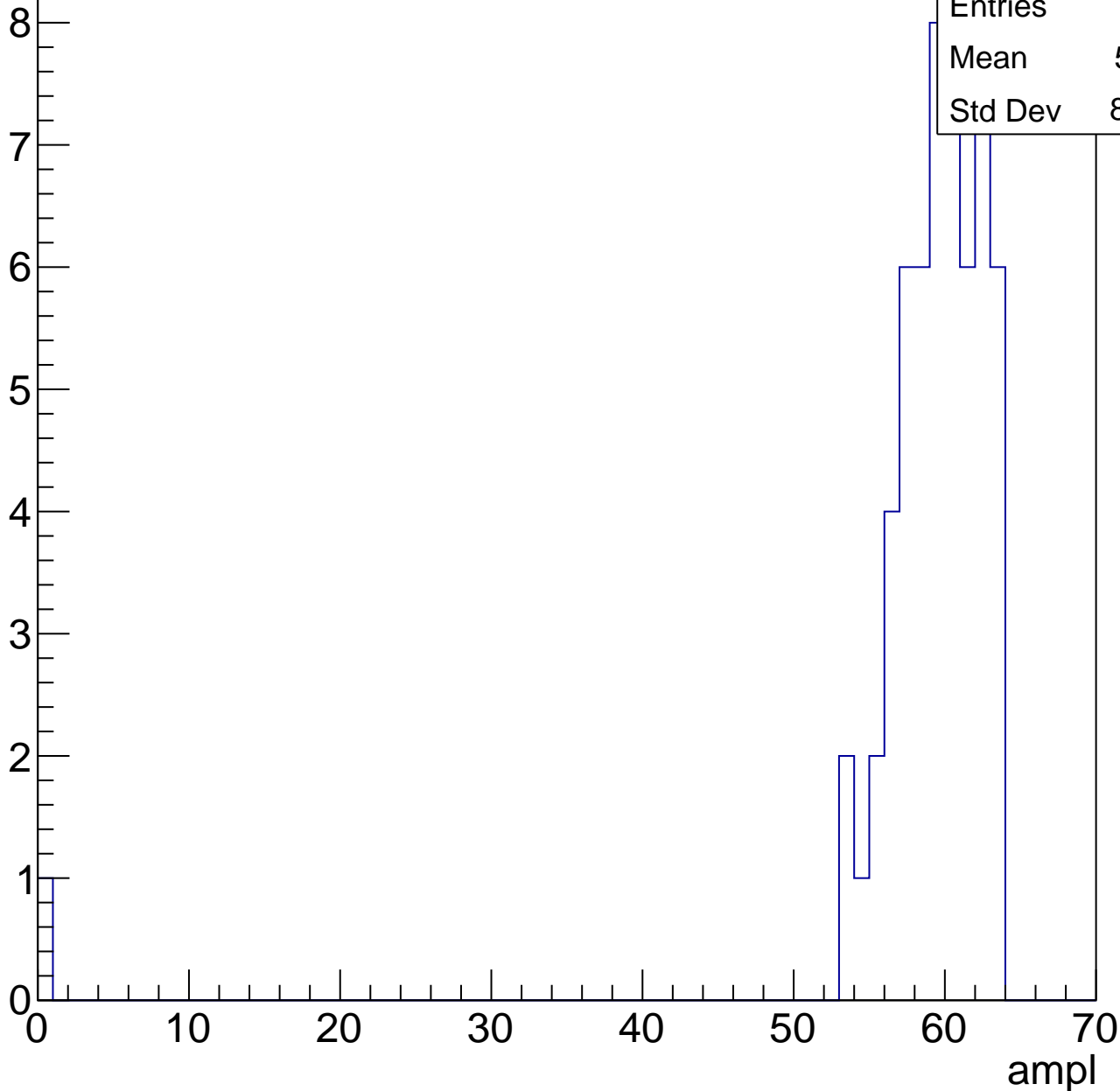


B1L103S, U23-ch6, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

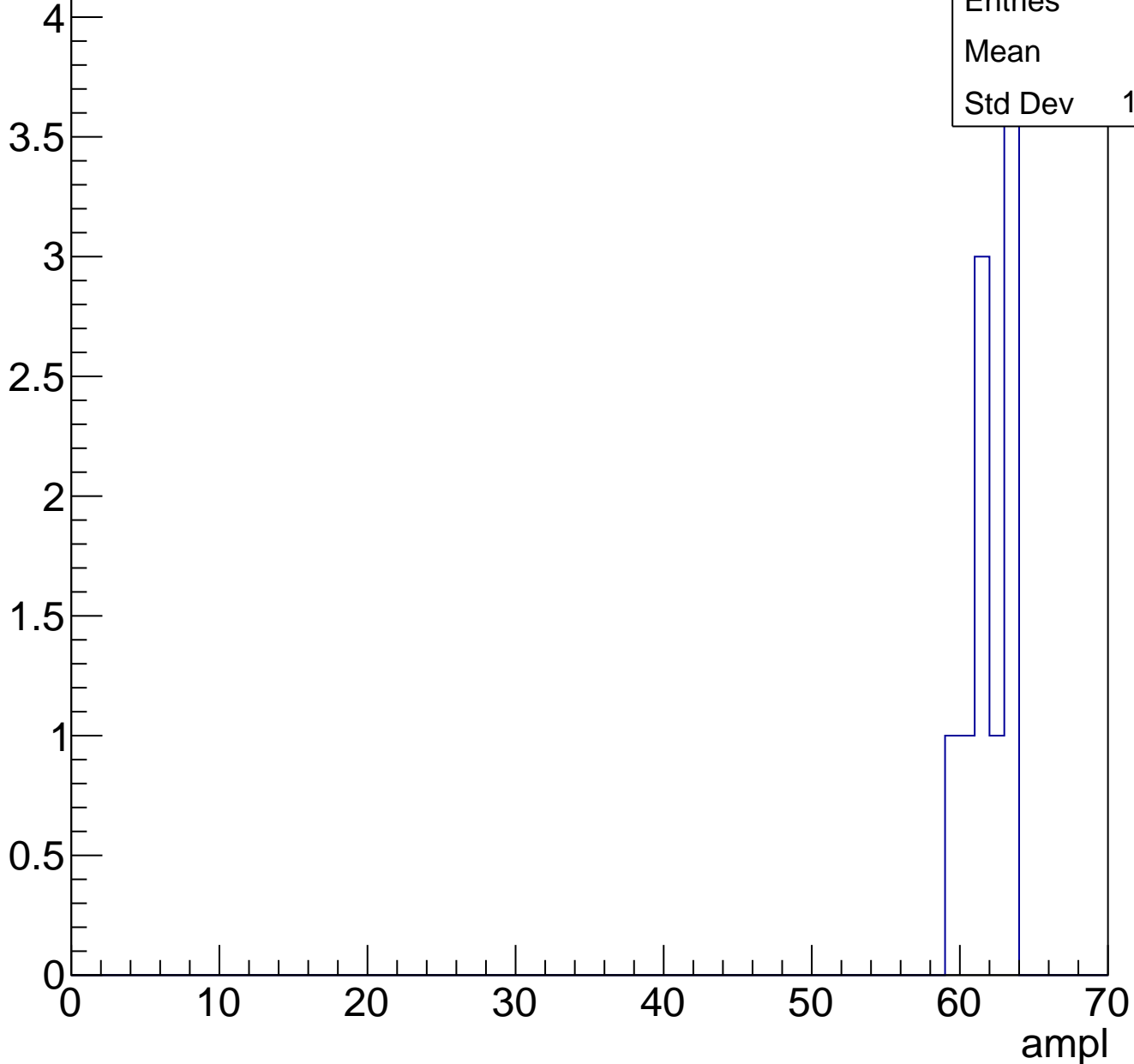
Entries	58
Mean	58.21
Std Dev	8.136



B1L103S, U23-ch6, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch6, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

ampl

B1L103S, U23-ch7, adc0

calib_packv5_041523_1651.root, FC#0, port C2

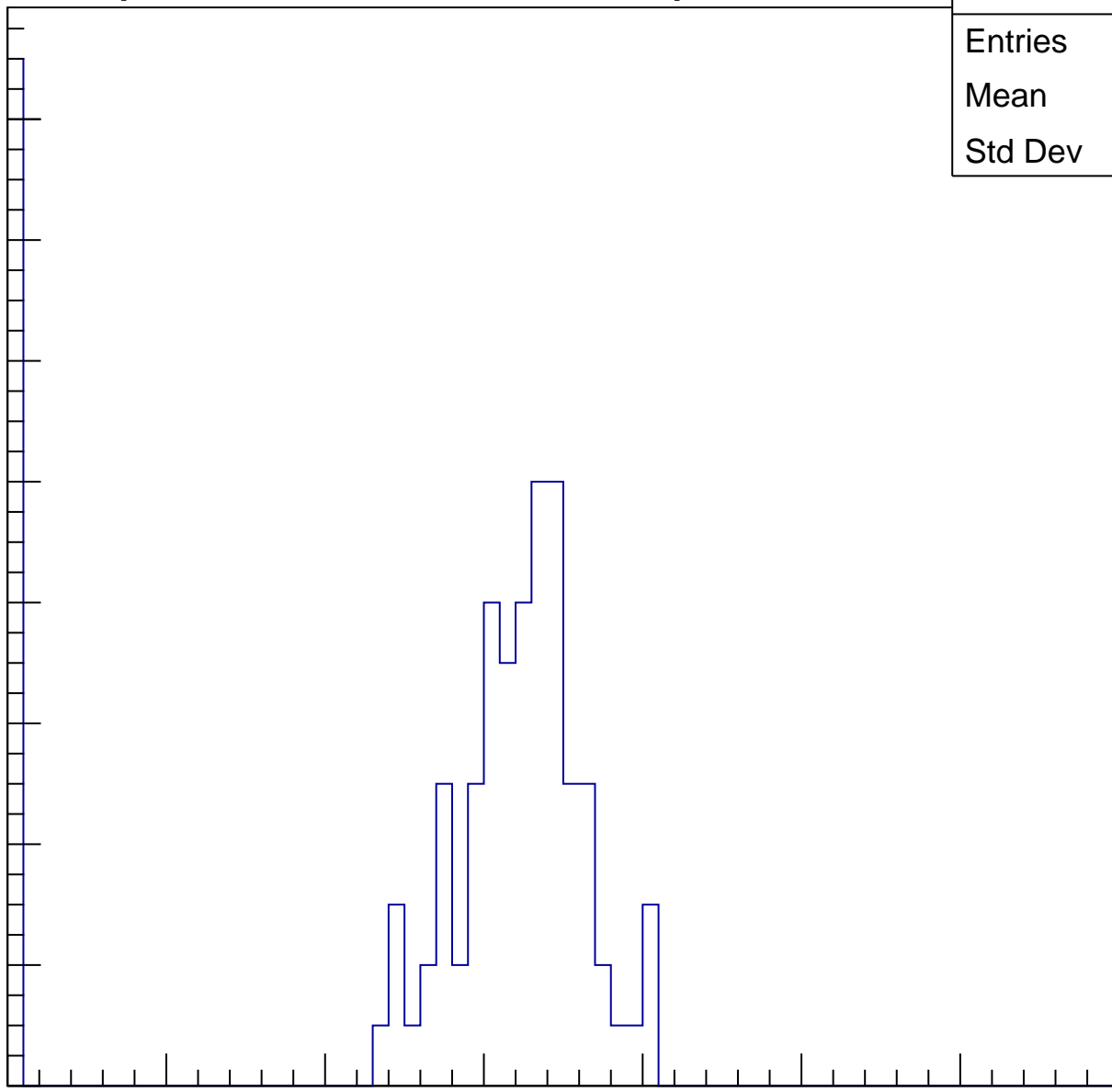
Entries	96
Mean	26.22
Std Dev	12.64

Entry

16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

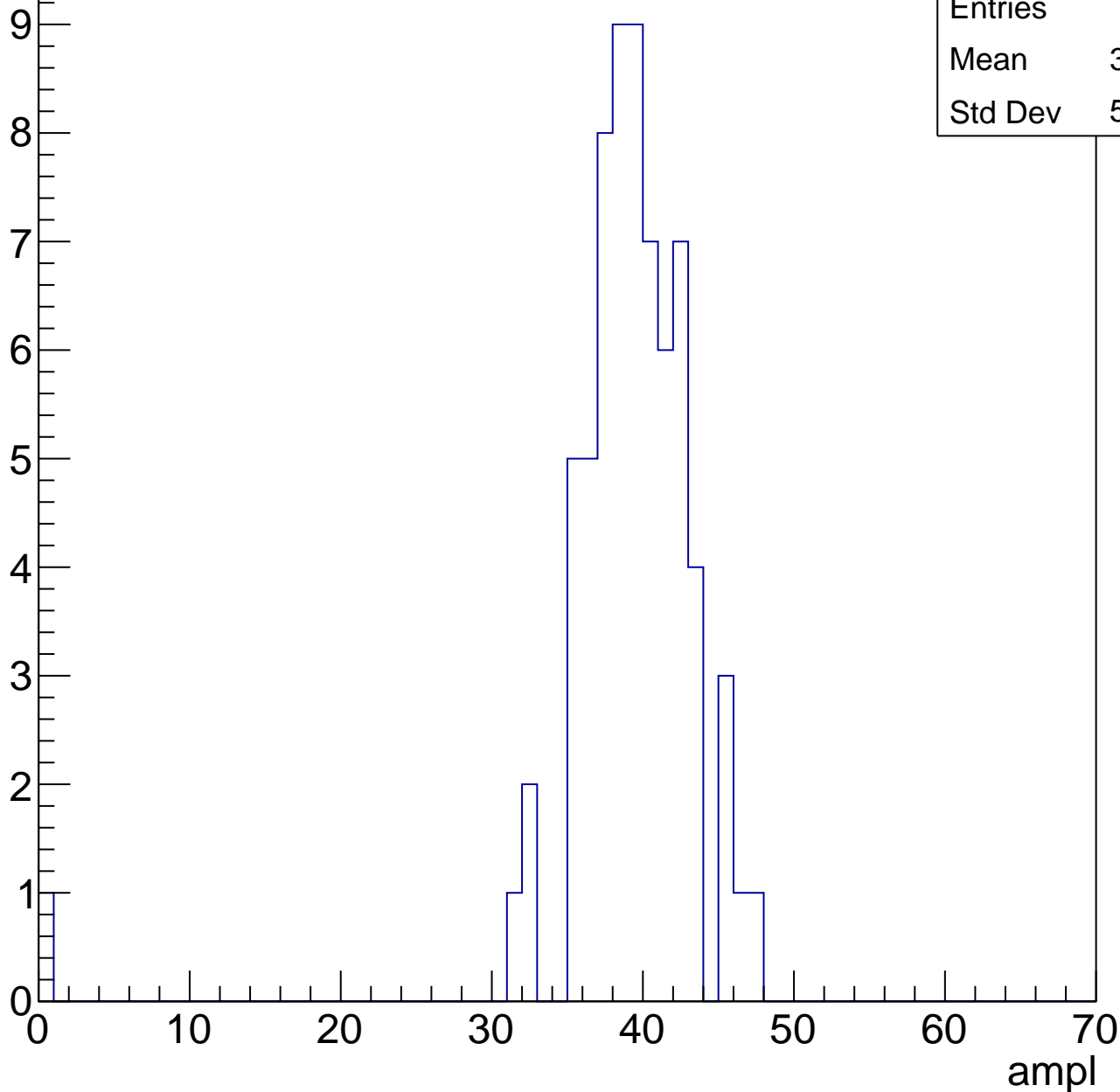


B1L103S, U23-ch7, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	38.54
Std Dev	5.663



B1L103S, U23-ch7, adc2

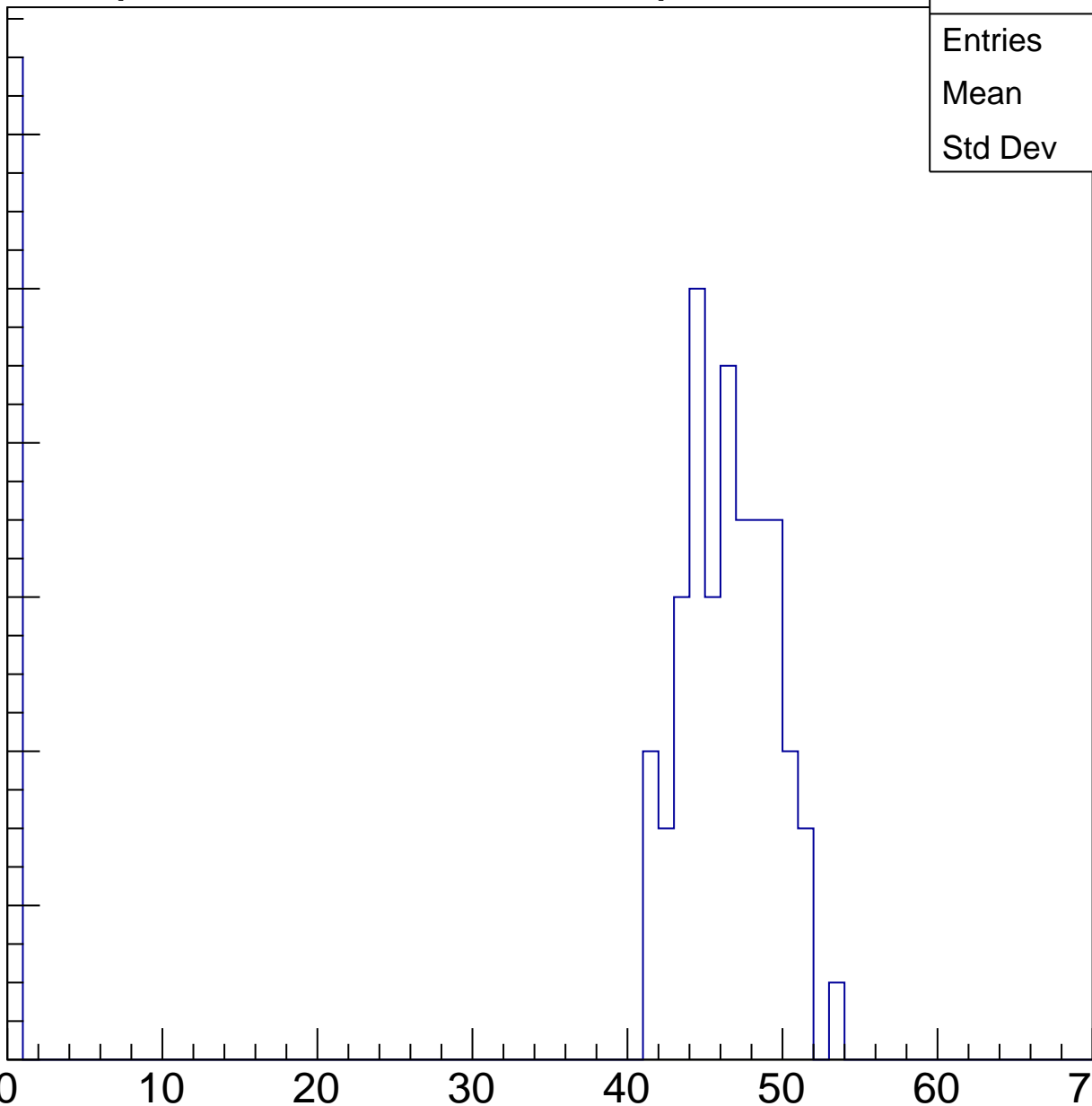
calib_packv5_041523_1651.root, FC#0, port C2

Entry

12
10
8
6
4
2
0

Entries	80
Mean	38.58
Std Dev	17.19

ampl

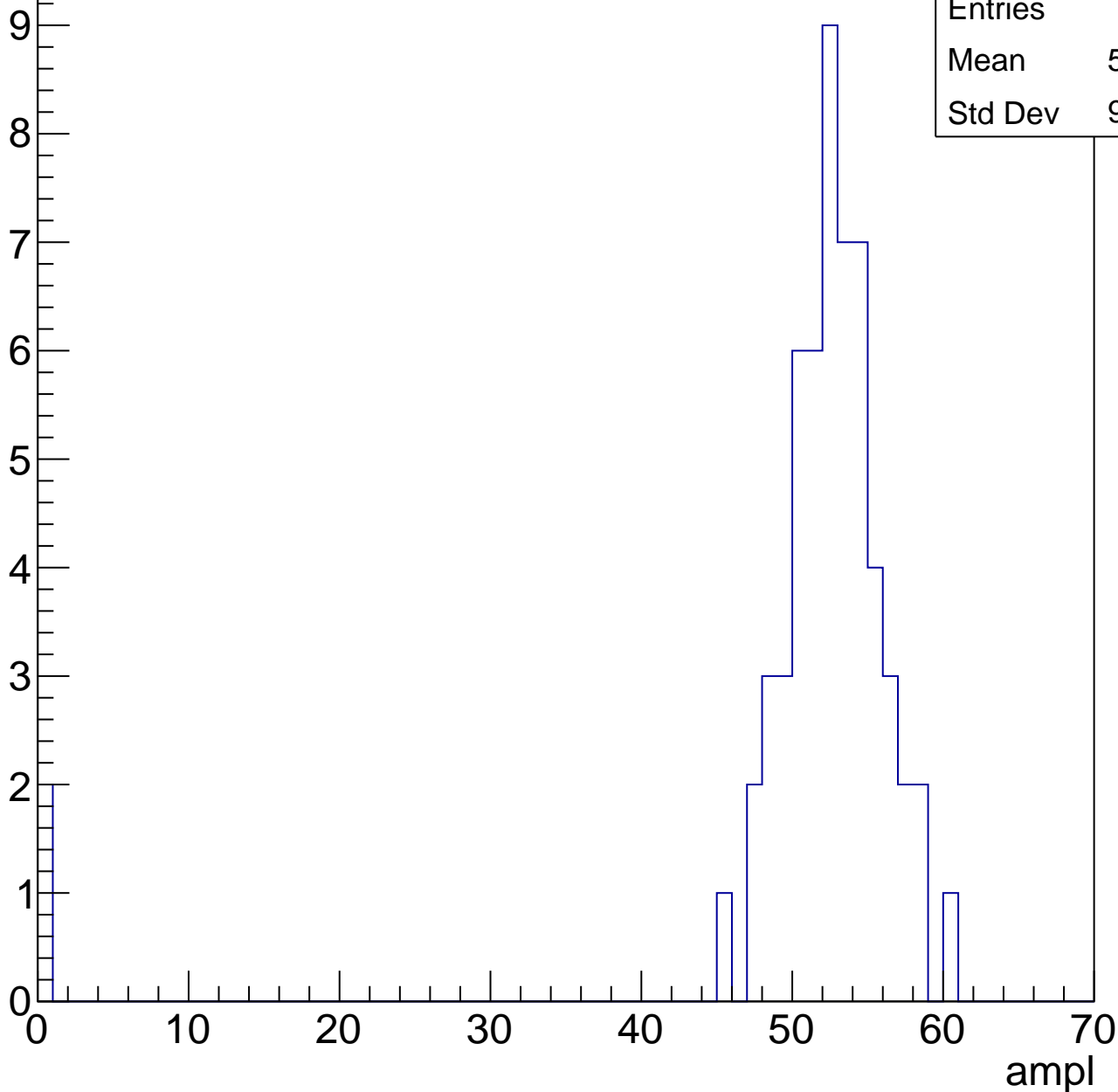


B1L103S, U23-ch7, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

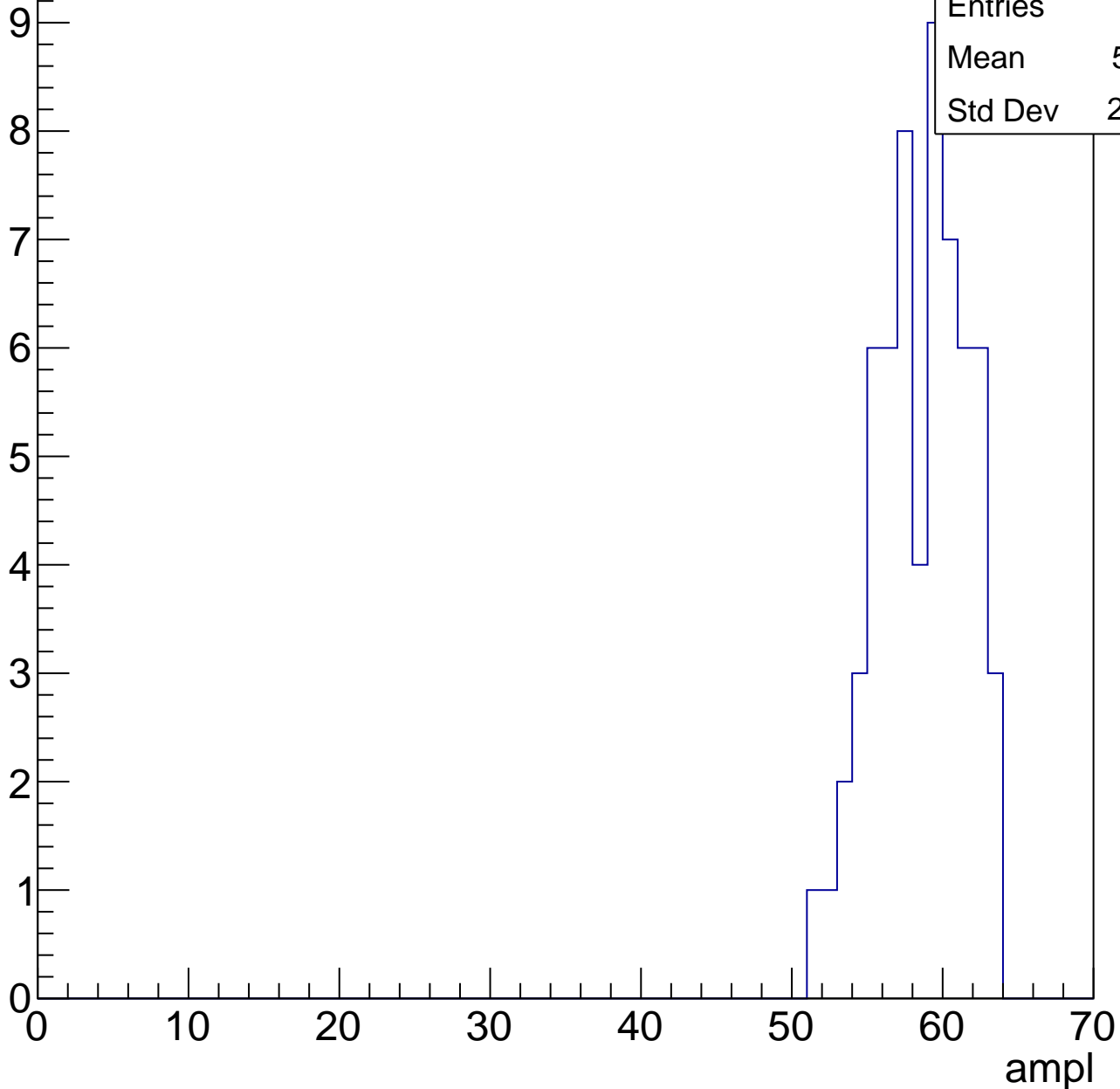
Entries	58
Mean	50.53
Std Dev	9.993



B1L103S, U23-ch7, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

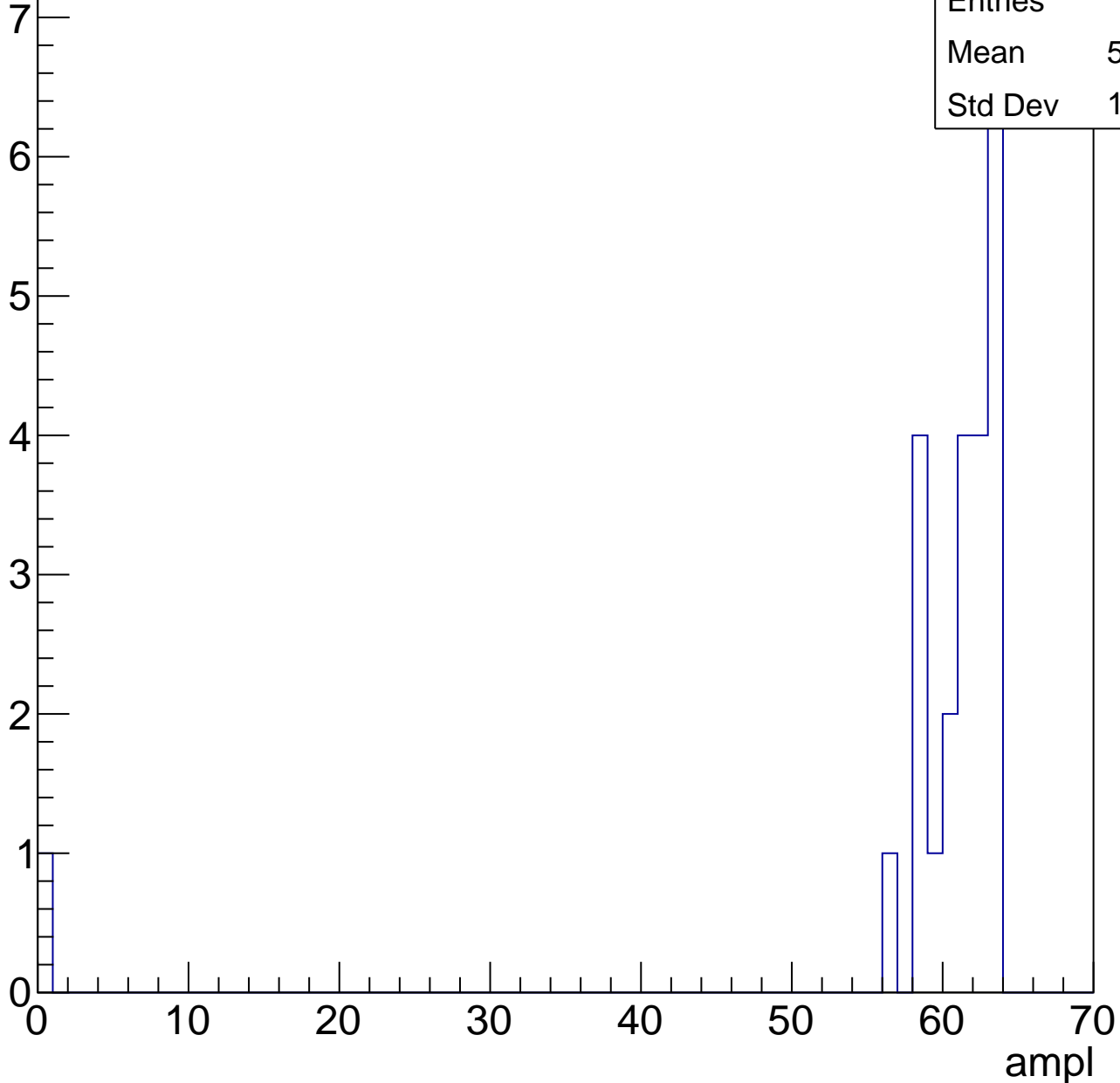


B1L103S, U23-ch7, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	24
Mean	58.33
Std Dev	12.33



B1L103S, U23-ch7, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	0
Mean	0
Std Dev	0

B1L103S, U23-ch7, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



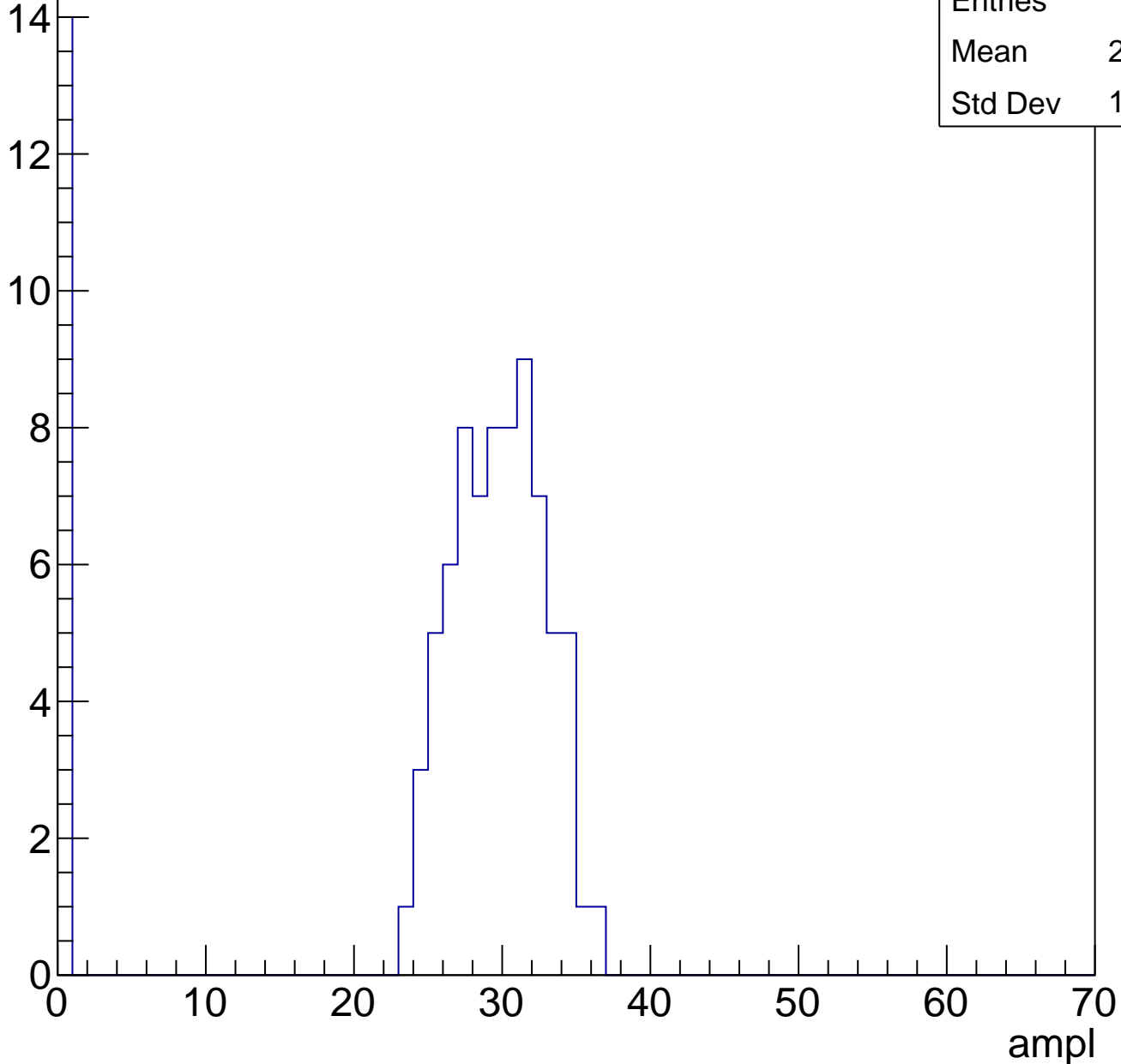
Entries	19
Mean	0
Std Dev	0

B1L103S, U23-ch8, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	88
Mean	24.65
Std Dev	11.07

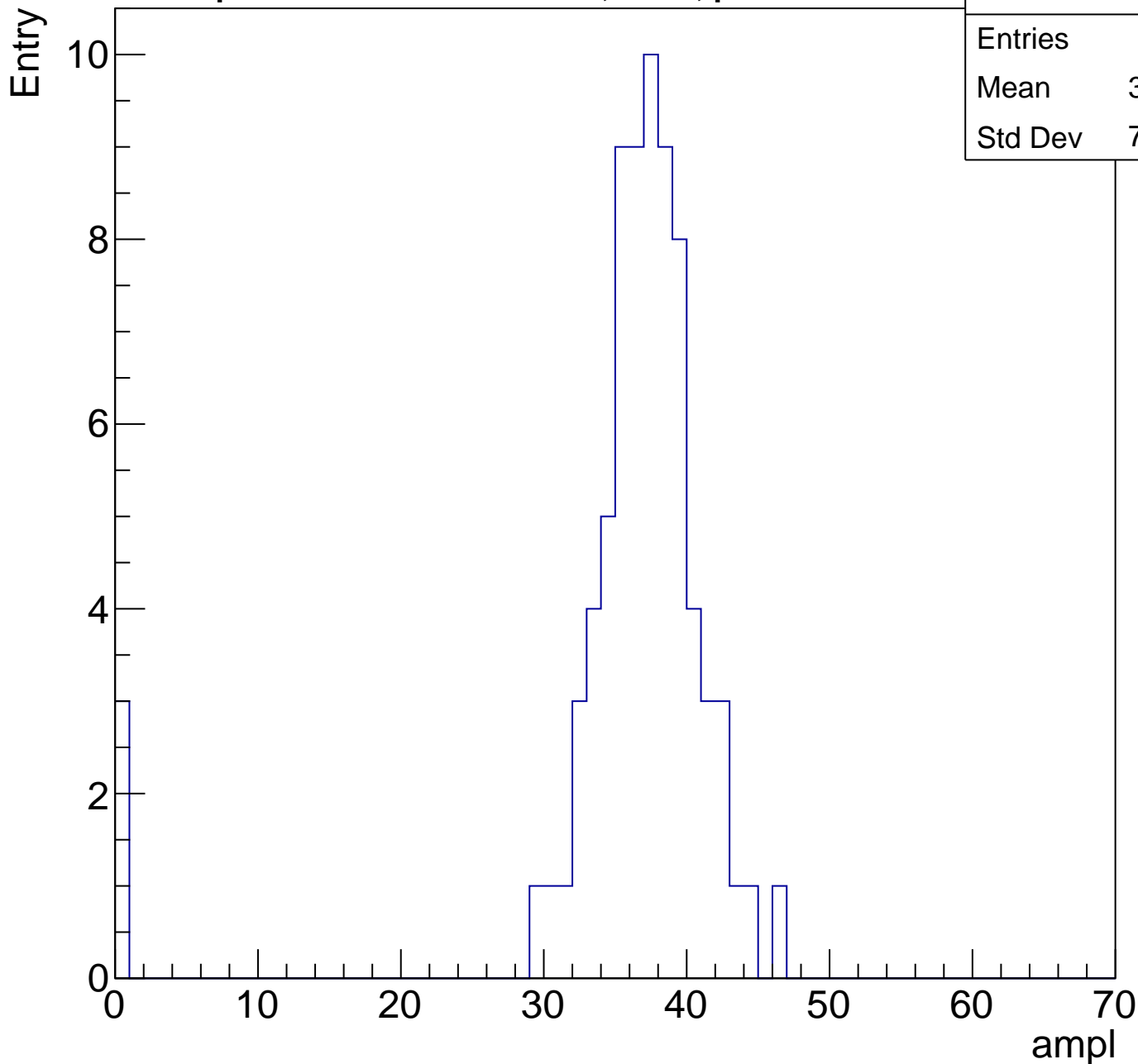
Entry



B1L103S, U23-ch8, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	76
Mean	35.43
Std Dev	7.834



B1L103S, U23-ch8, adc2

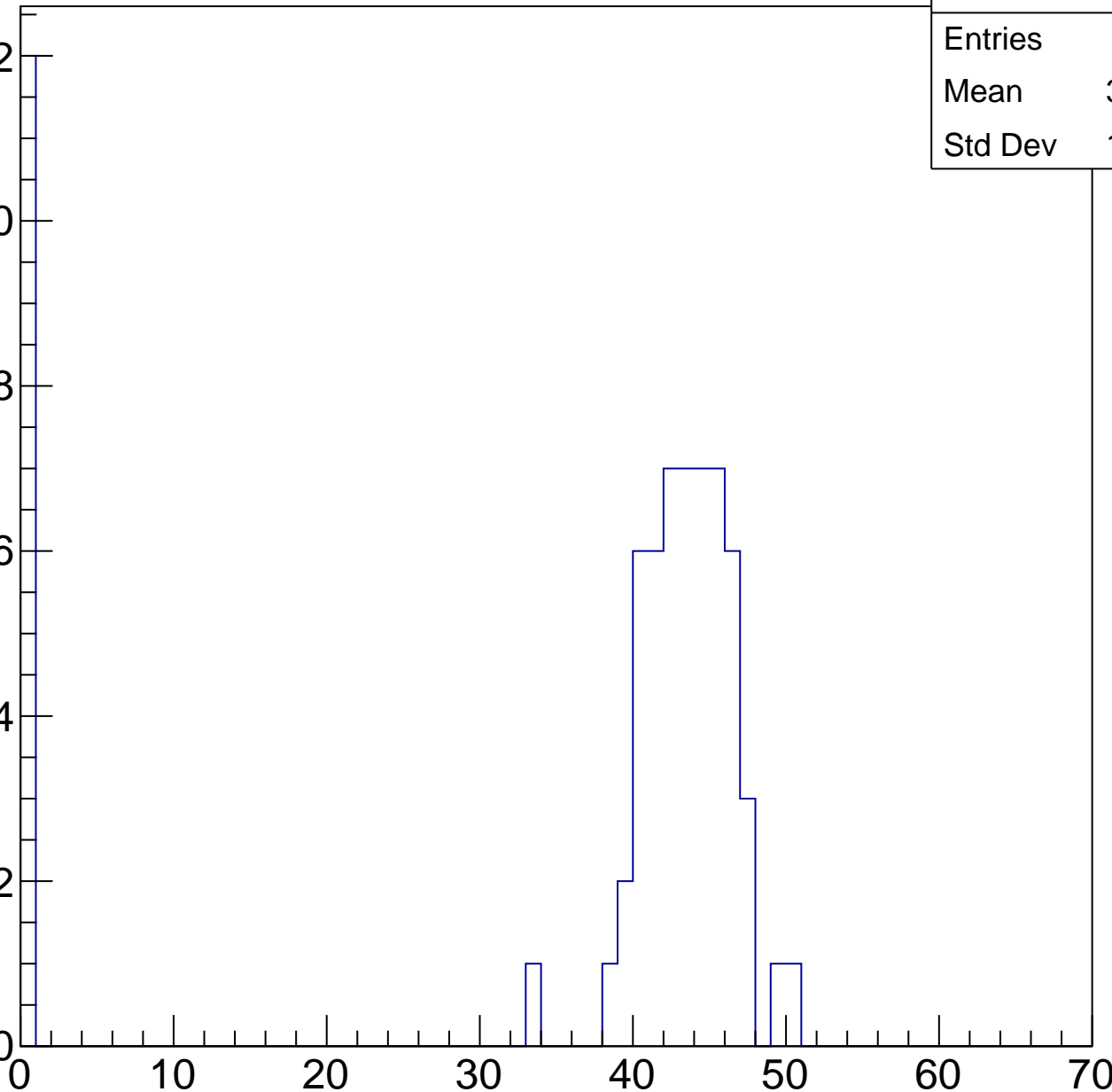
calib_packv5_041523_1651.root, FC#0, port C2

Entry

12
10
8
6
4
2
0

Entries	67
Mean	35.36
Std Dev	16.72

ampl

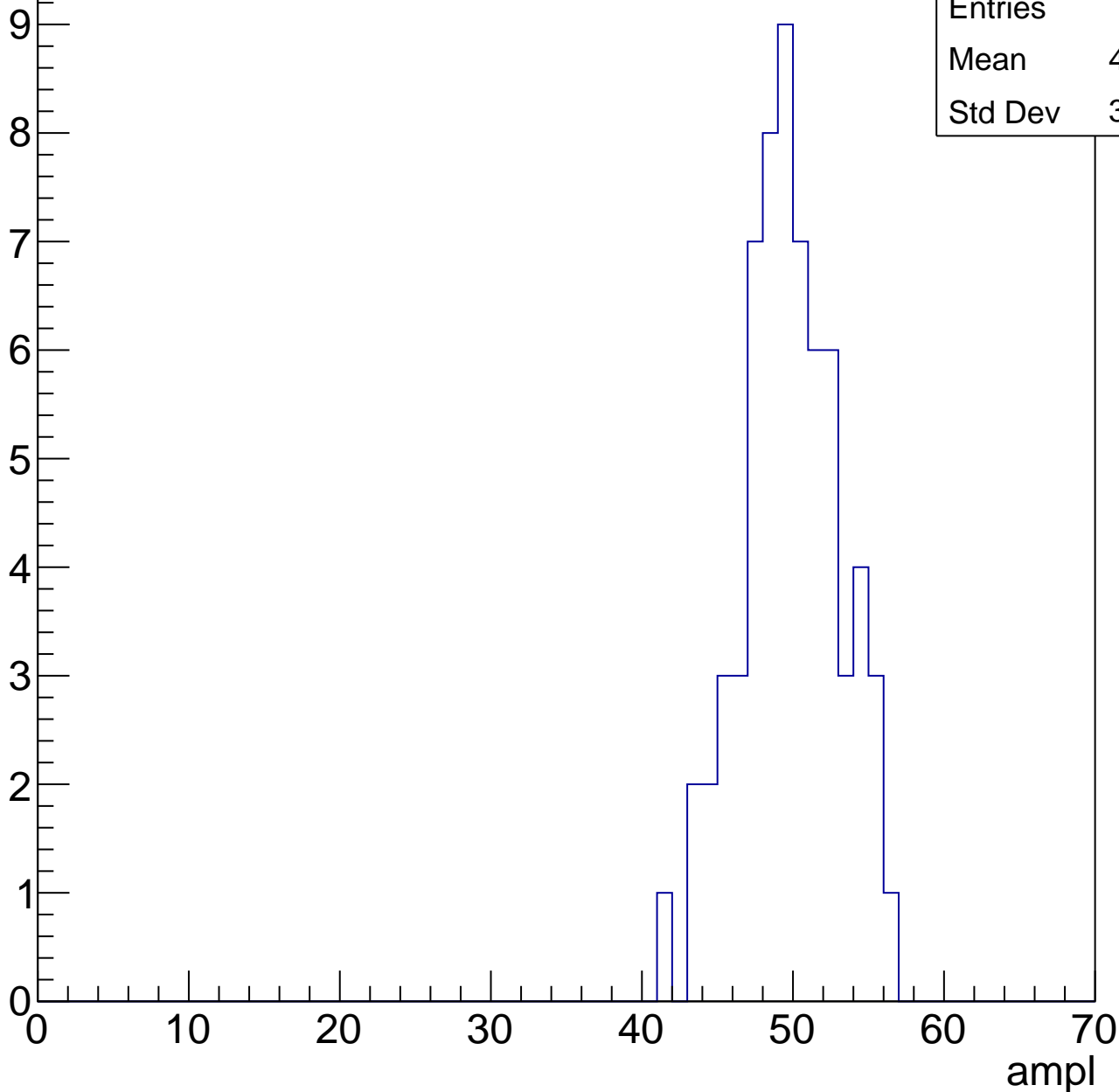


B1L103S, U23-ch8, adc3

calib_packv5_041523_1651.root, FC#0, port C2

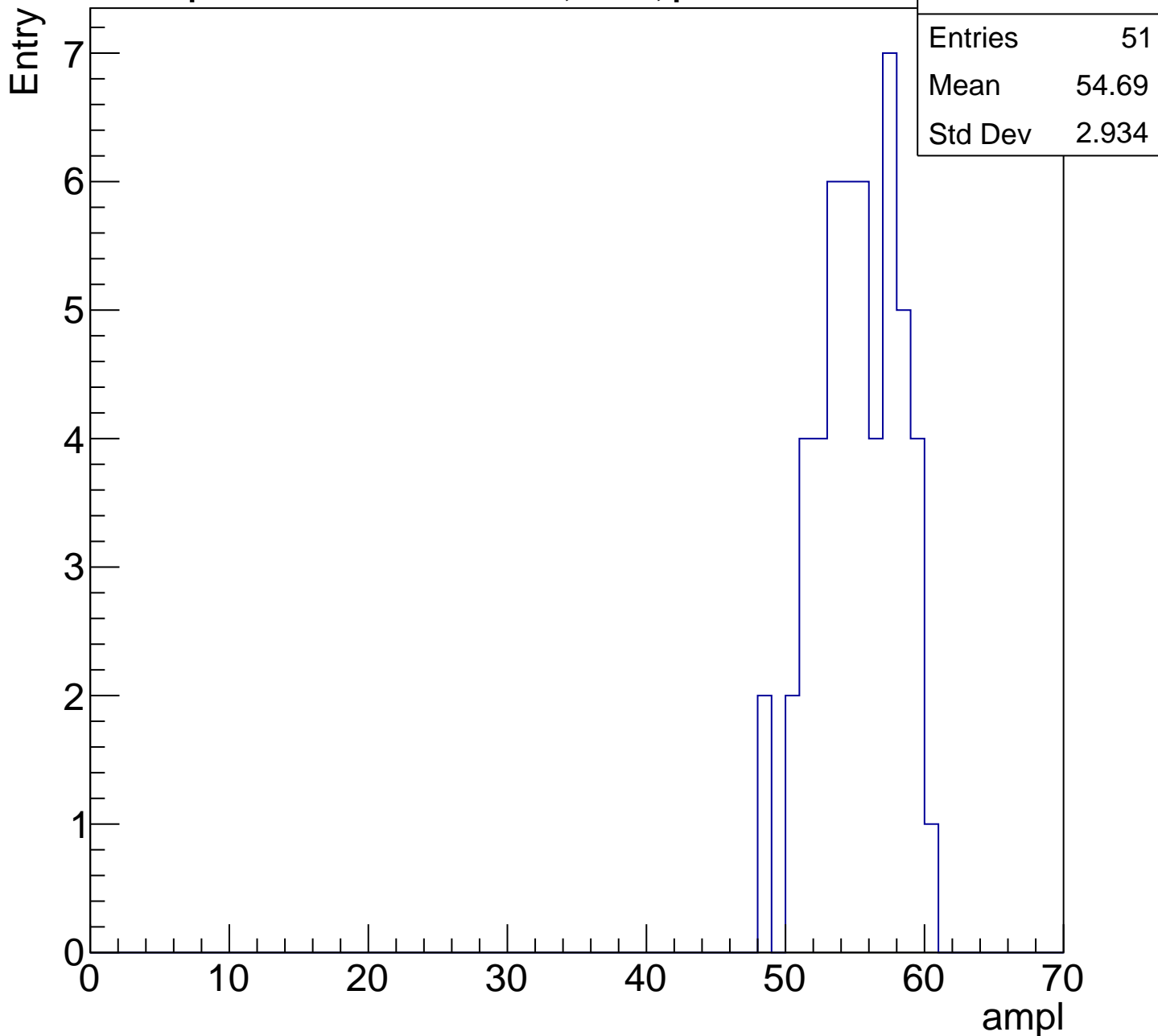
Entry

Entries	65
Mean	49.32
Std Dev	3.235



B1L103S, U23-ch8, adc4

calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U23-ch8, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

10

Entries 58

Mean 58.88

Std Dev 8.15

8

6

4

2

0

0

10

20

30

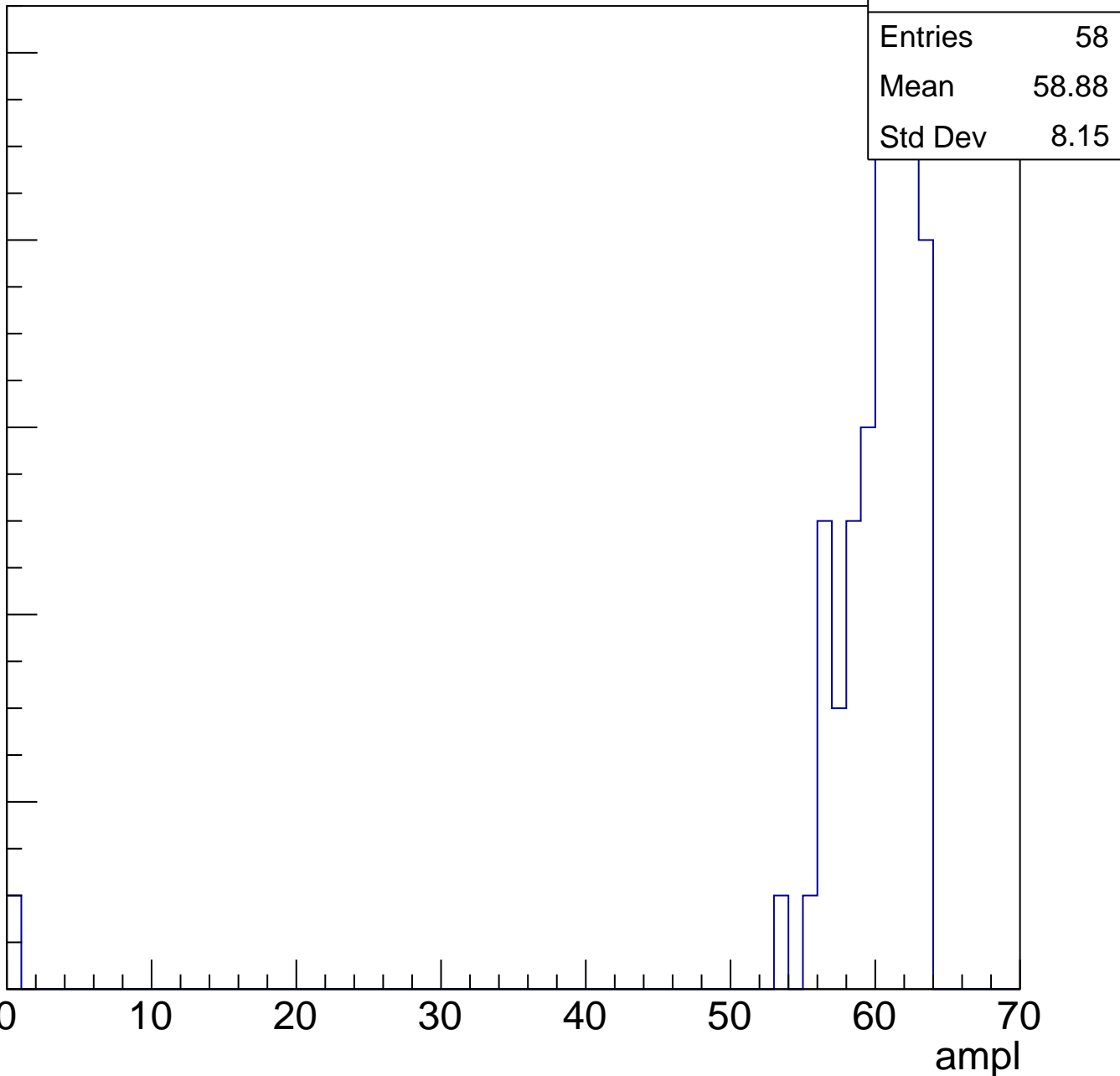
40

50

60

70

ampl



B1L103S, U23-ch8, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	3
Mean	62.67
Std Dev	0.4714

ampl

0 10 20 30 40 50 60 70

B1L103S, U23-ch8, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U23-ch9, adc0

calib_packv5_041523_1651.root, FC#0, port C2

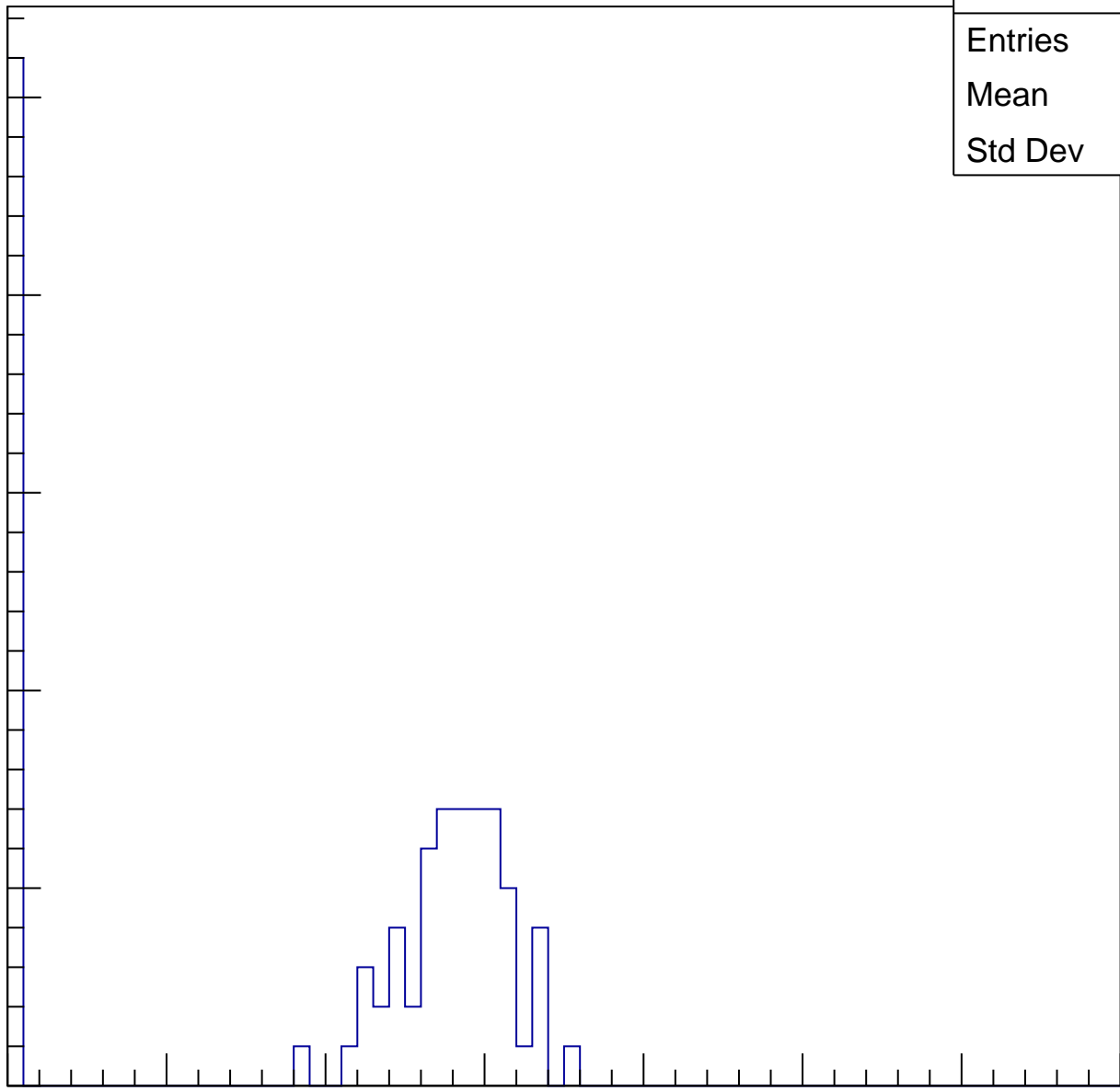
Entries	84
Mean	19.11
Std Dev	13.1

Entry

25
20
15
10
5
0

0 10 20 30 40 50 60 70

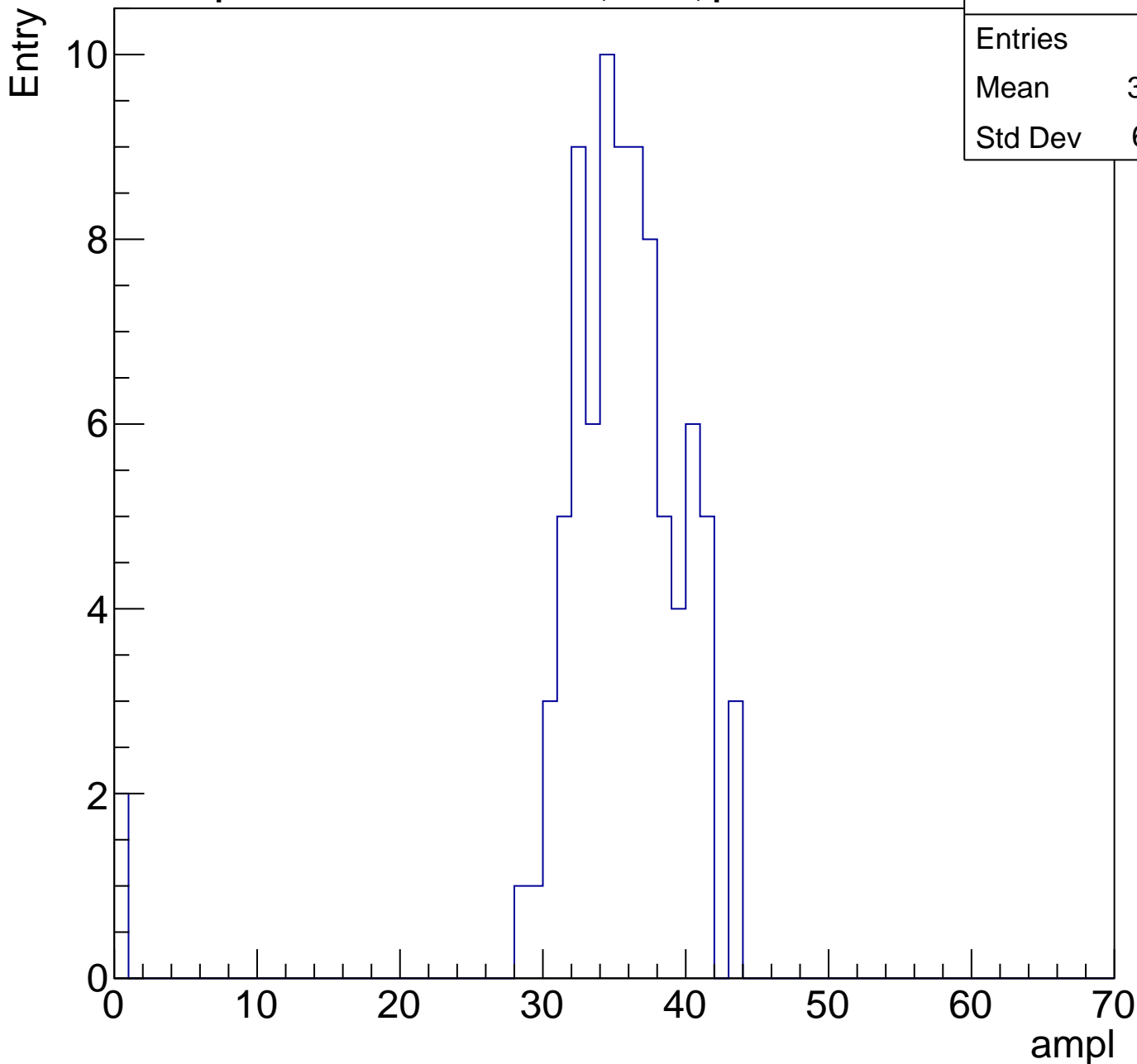
ampl



B1L103S, U23-ch9, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	86
Mean	34.69
Std Dev	6.351

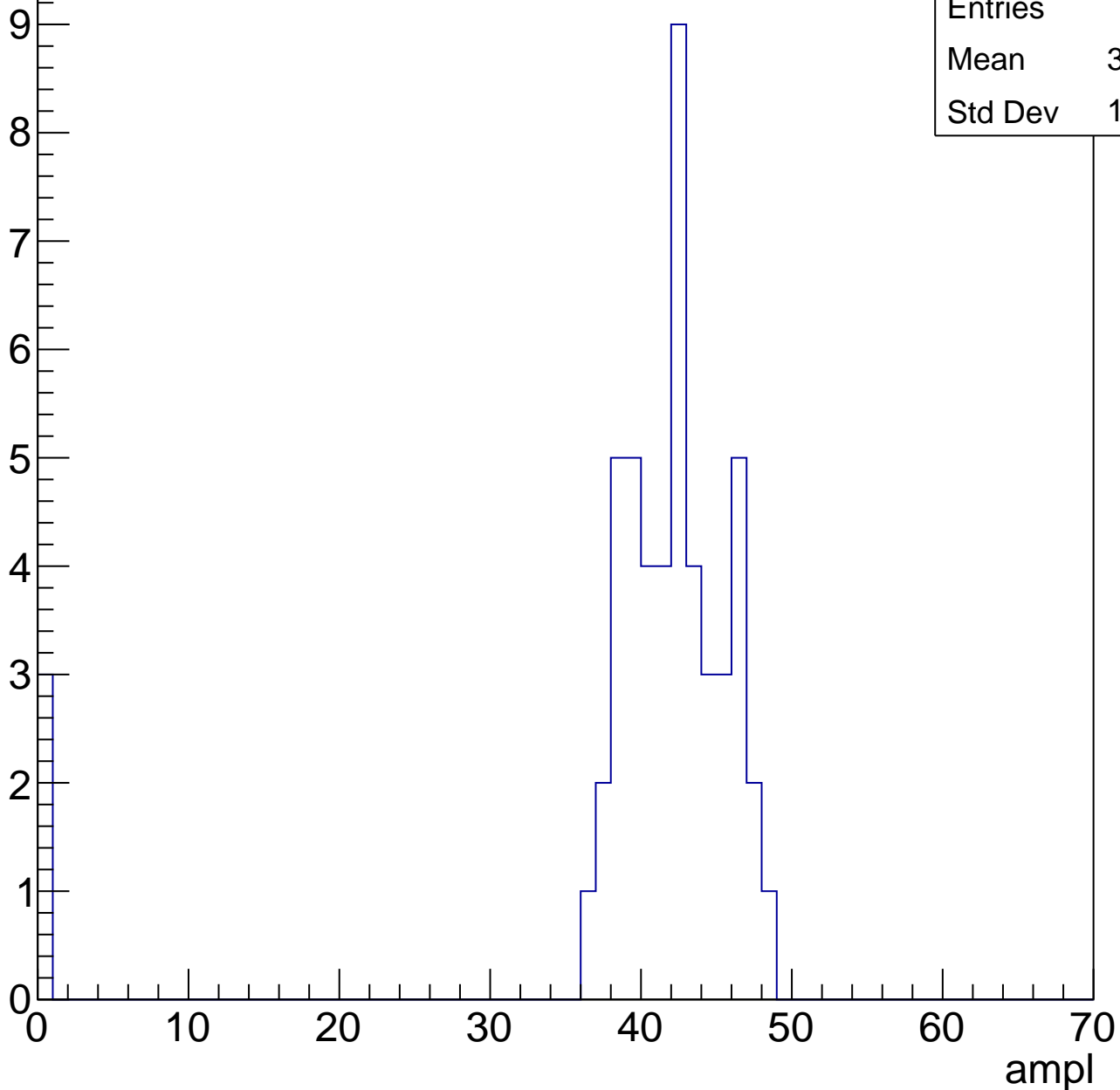


B1L103S, U23-ch9, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	51
Mean	39.37
Std Dev	10.27



B1L103S, U23-ch9, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	93
Mean	41.51
Std Dev	17.05

Entry

12

10

8

6

4

2

0

0

10

20

30

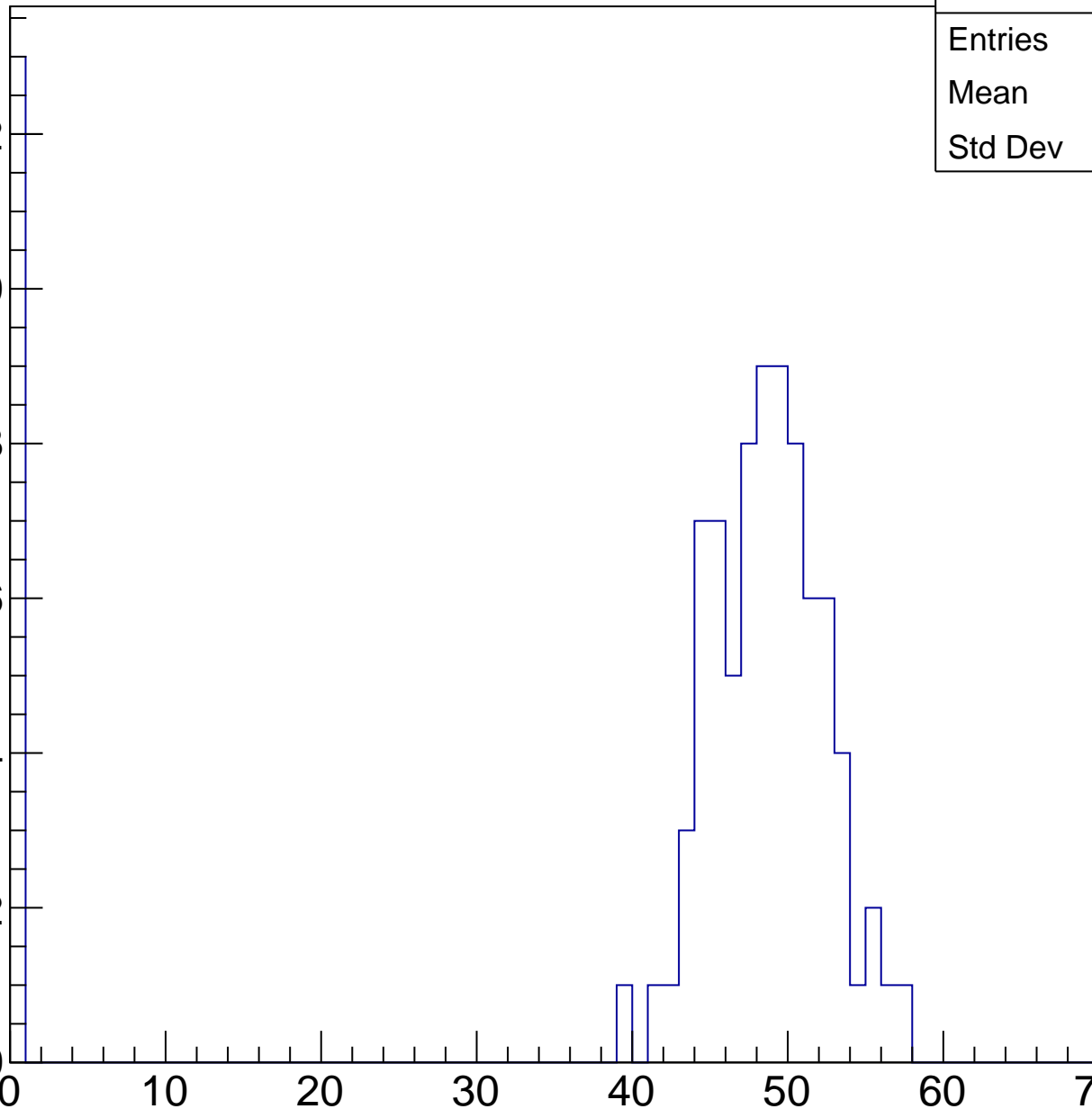
40

50

60

70

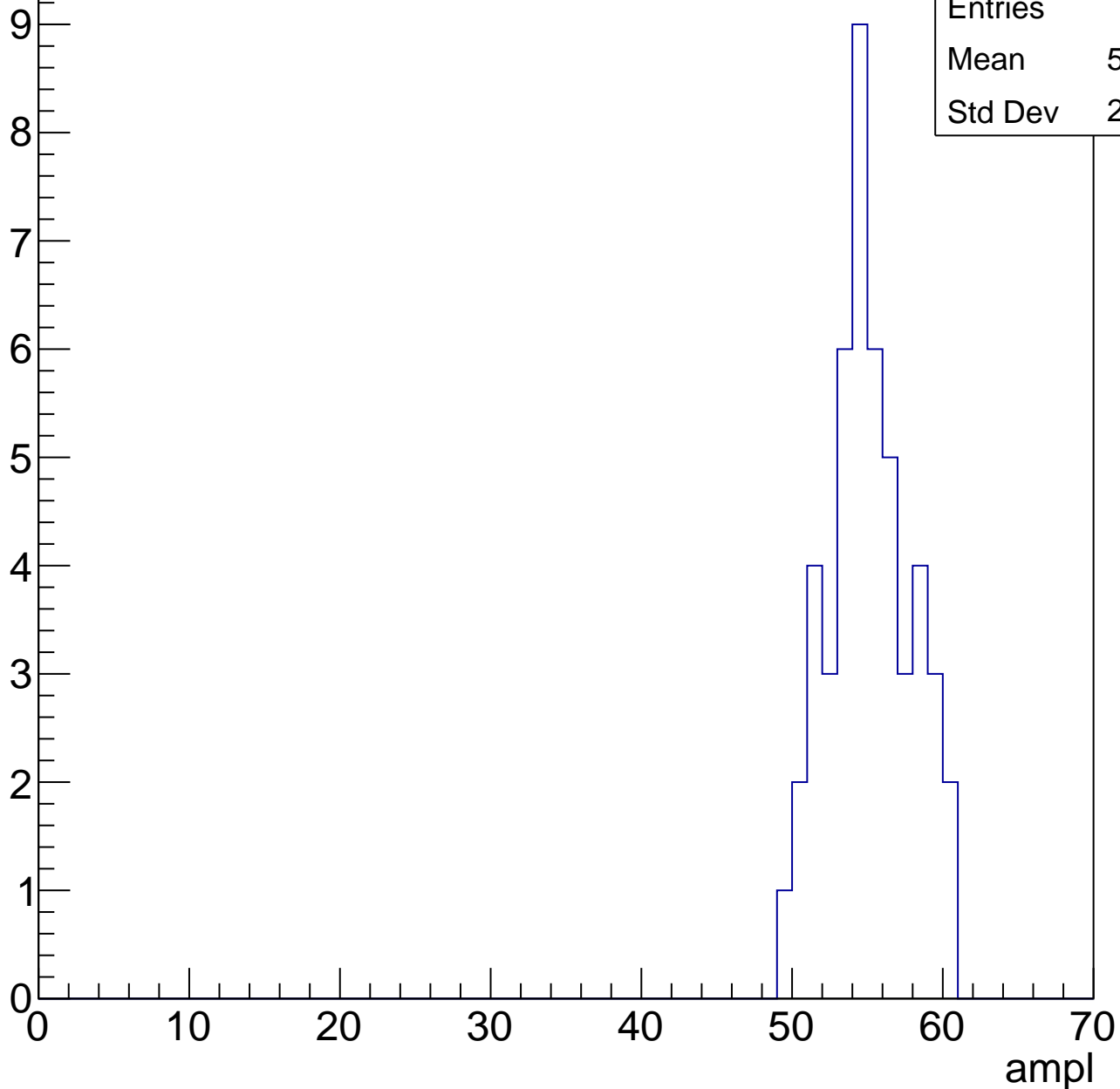
ampl



B1L103S, U23-ch9, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry



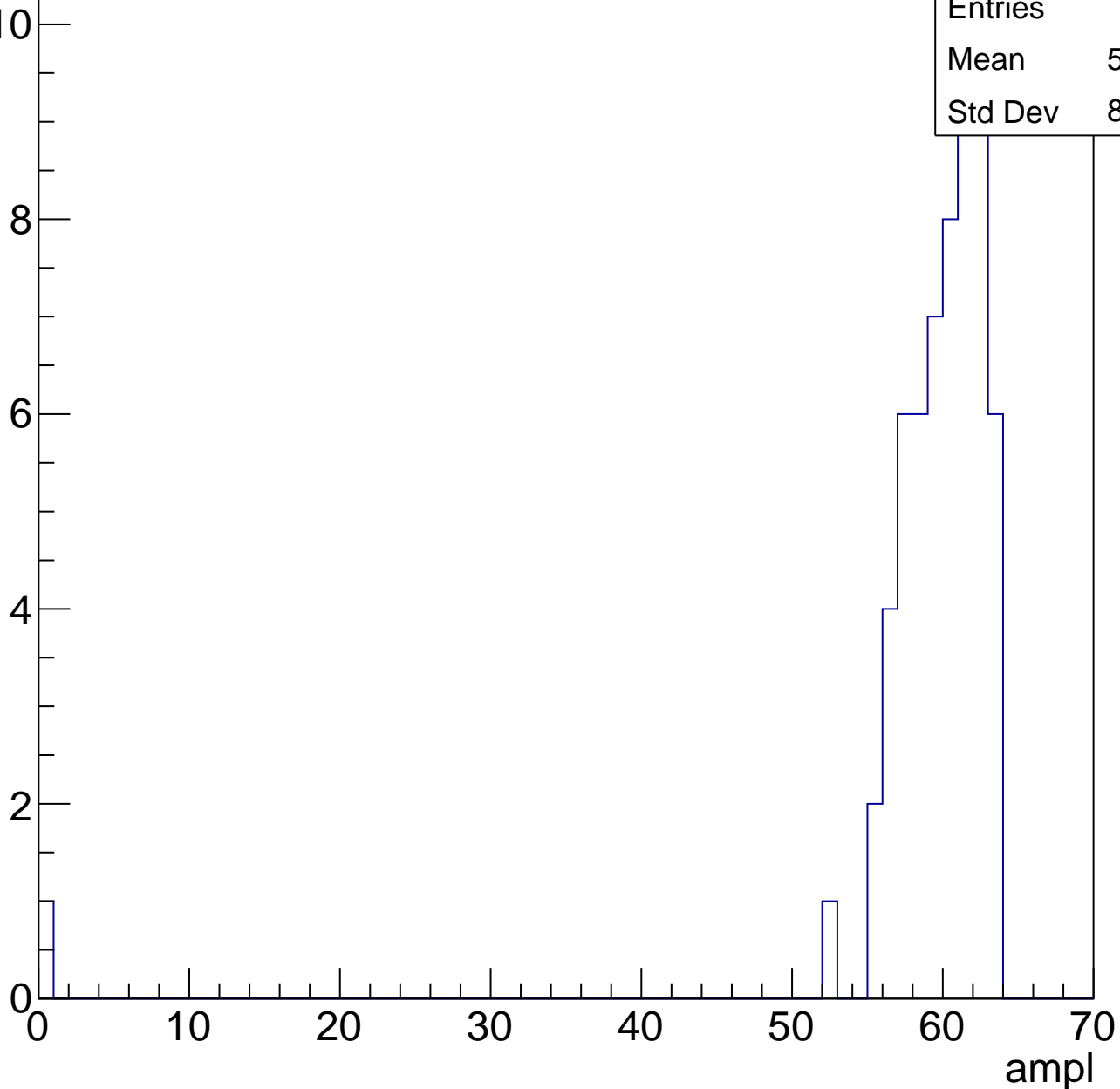
Entries	48
Mean	54.65
Std Dev	2.719

B1L103S, U23-ch9, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

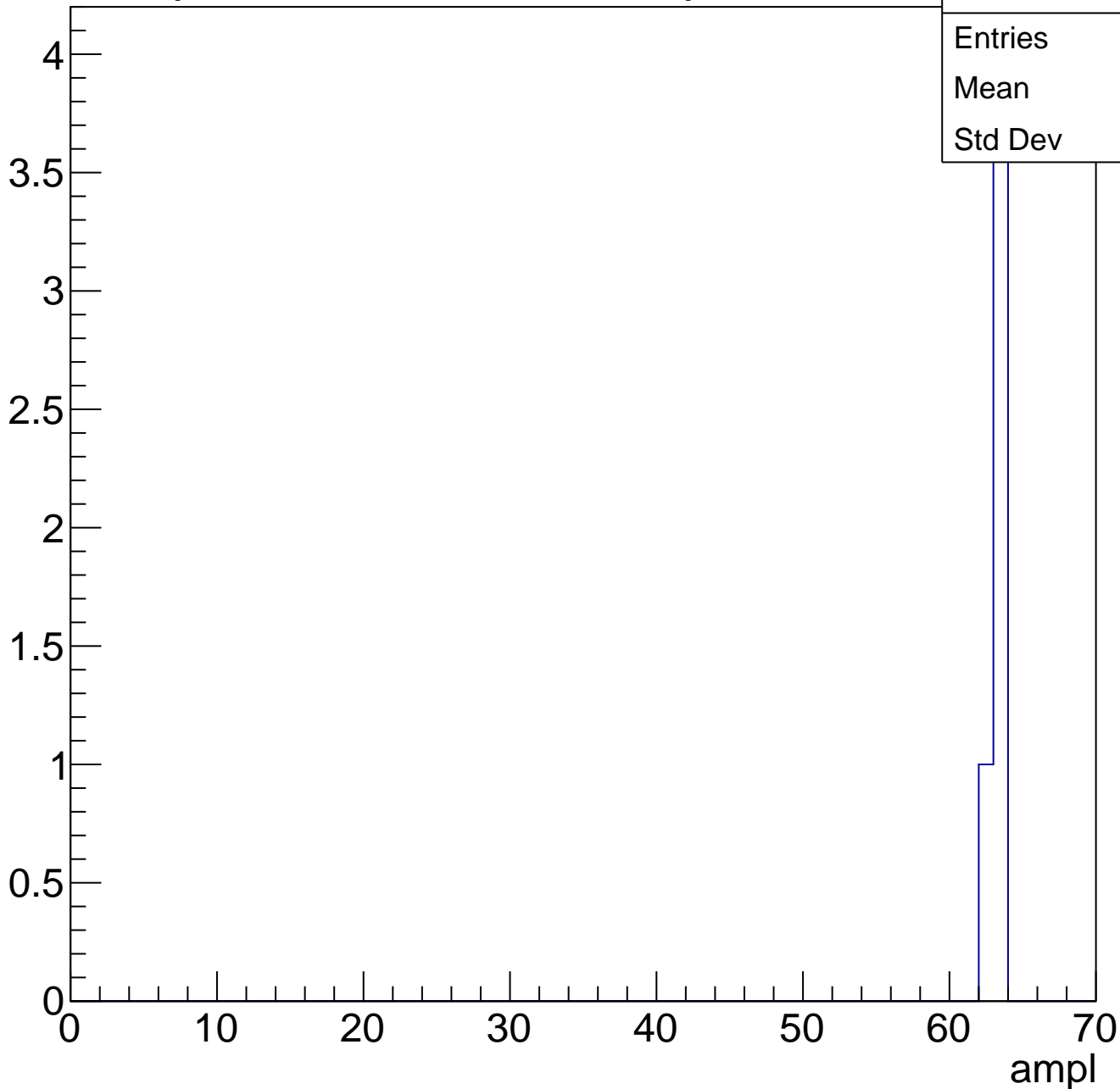
Entries	60
Mean	58.58
Std Dev	8.003



B1L103S, U23-ch9, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch9, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

ampl

B1L103S, U23-ch10, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	95
Mean	23.04
Std Dev	10.88

Entry

16
14
12
10
8
6
4
2
0

0

10

20

30

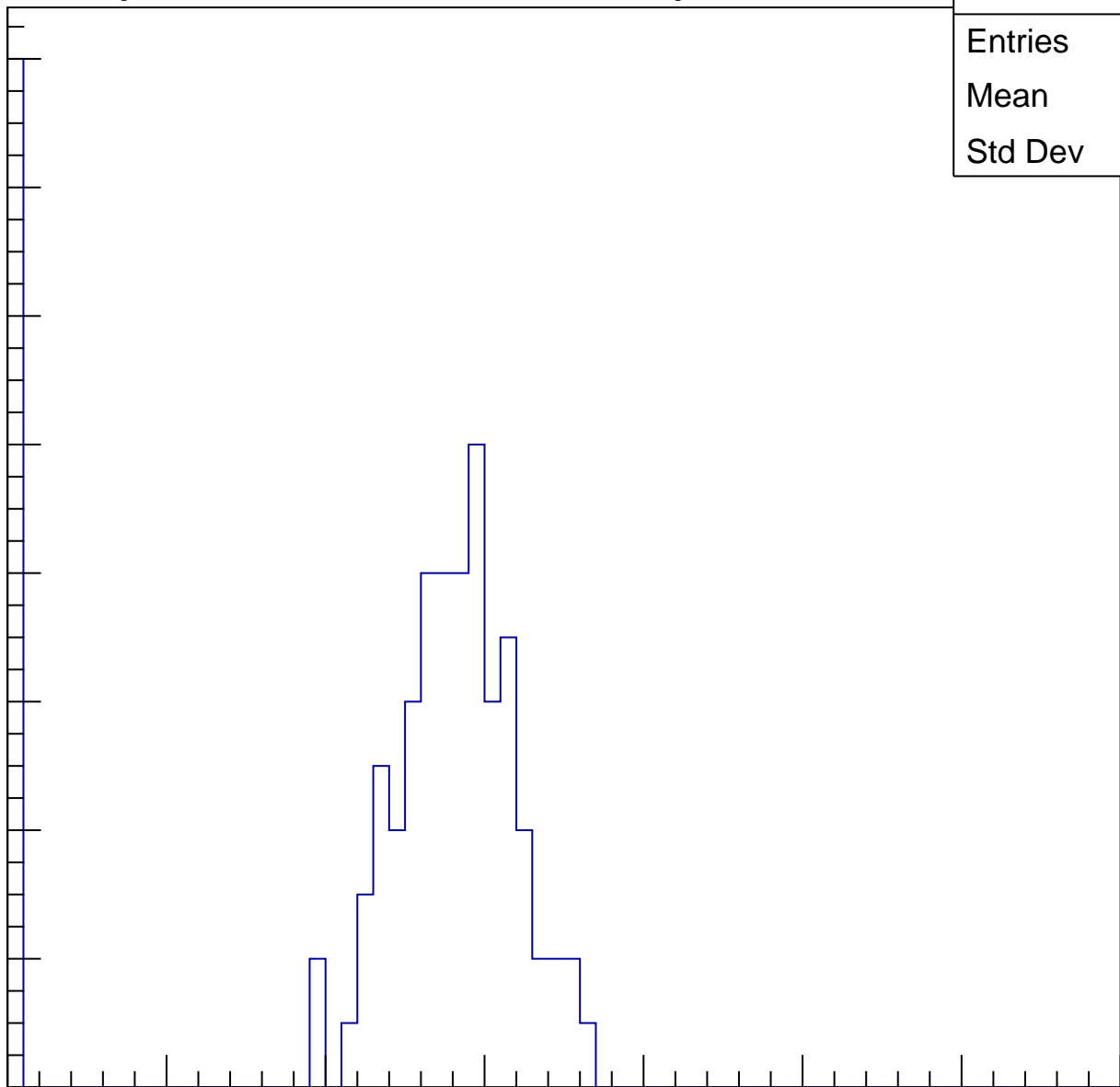
40

50

60

70

ampl

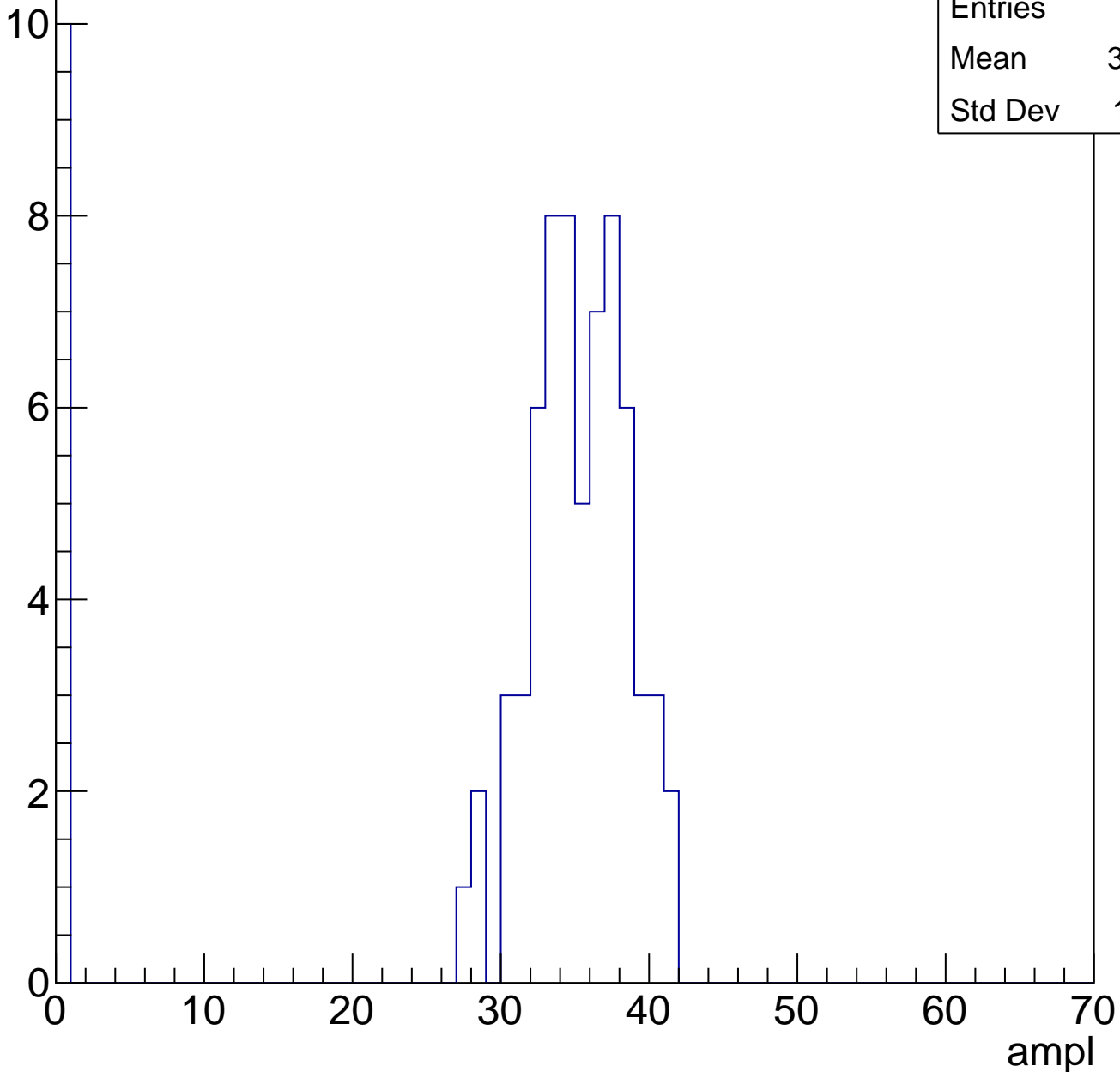


B1L103S, U23-ch10, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	75
Mean	30.19
Std Dev	12.21

Entry

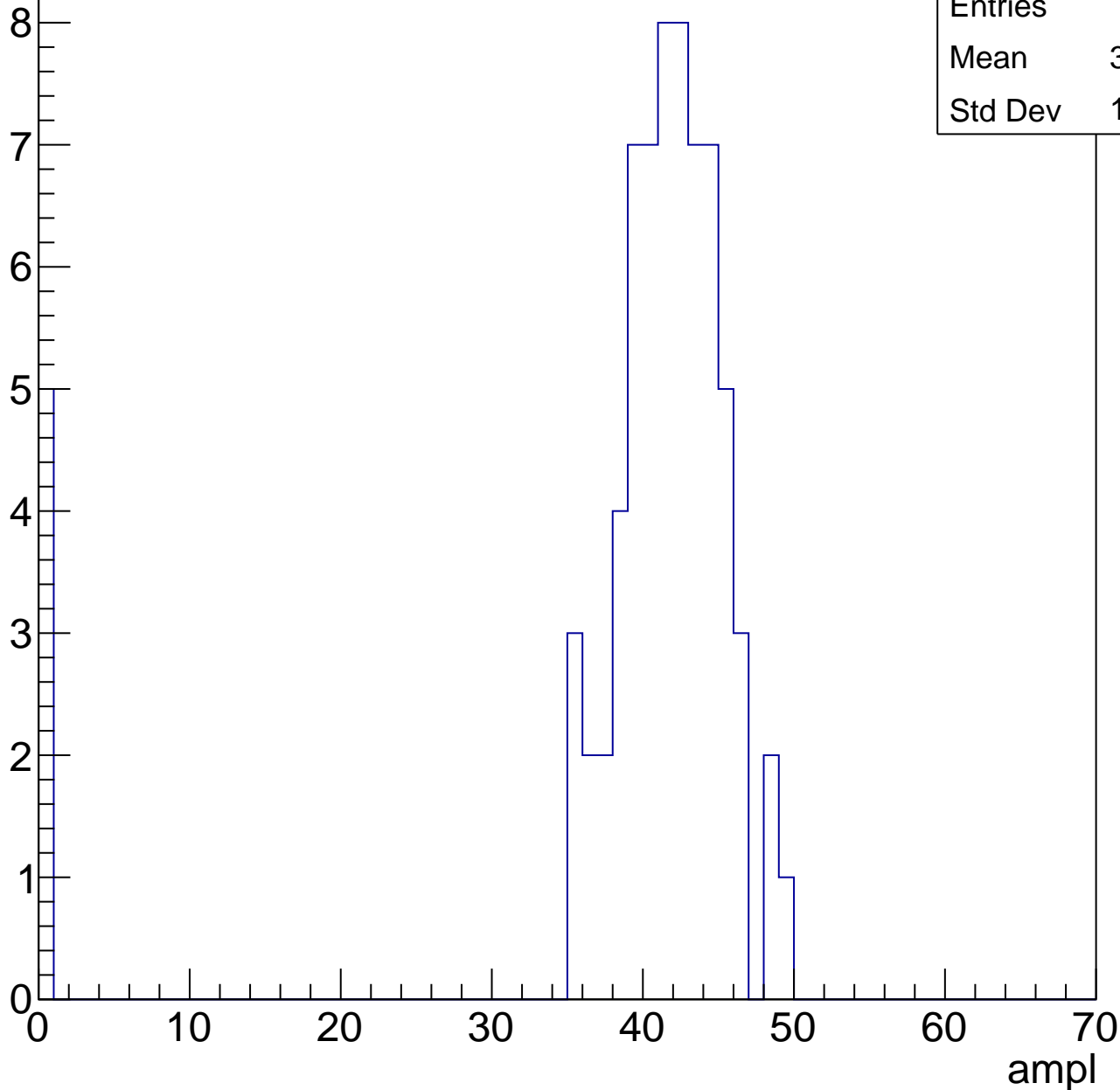


B1L103S, U23-ch10, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	38.55
Std Dev	11.04

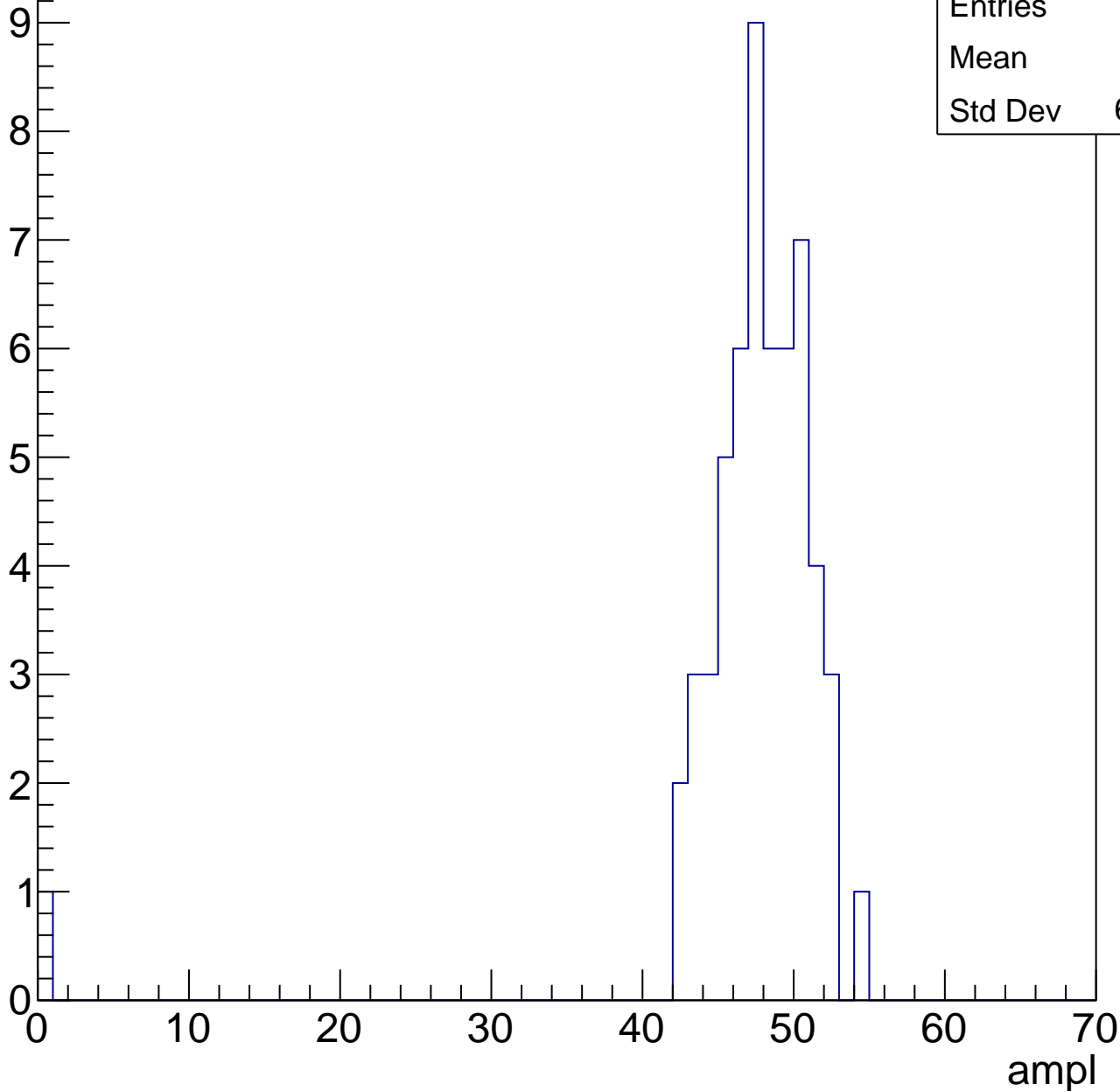


B1L103S, U23-ch10, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	56
Mean	46.7
Std Dev	6.861



B1L103S, U23-ch10, adc4

calib_packv5_041523_1651.root, FC#0, port C2

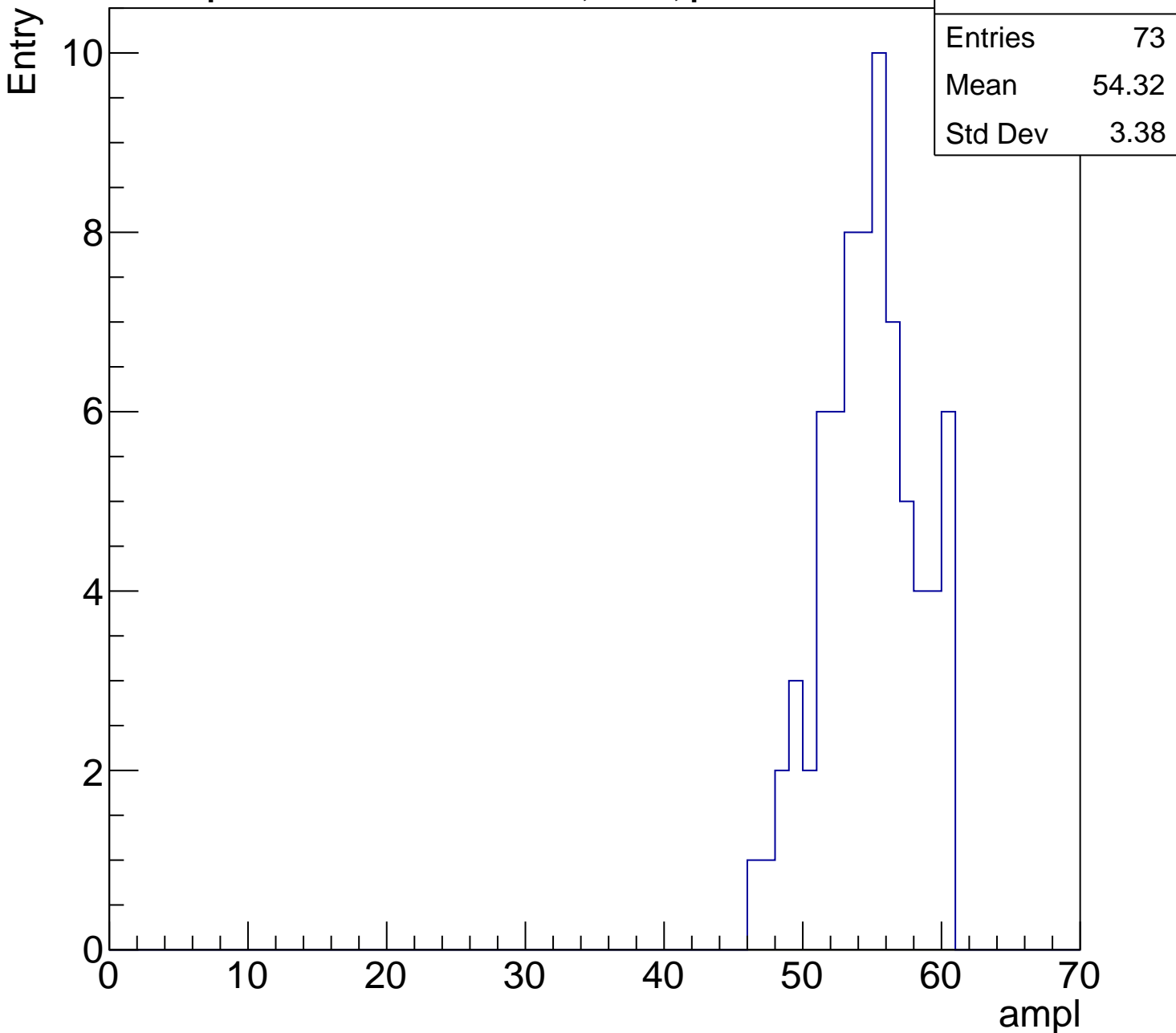
Entries	73
Mean	54.32
Std Dev	3.38

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

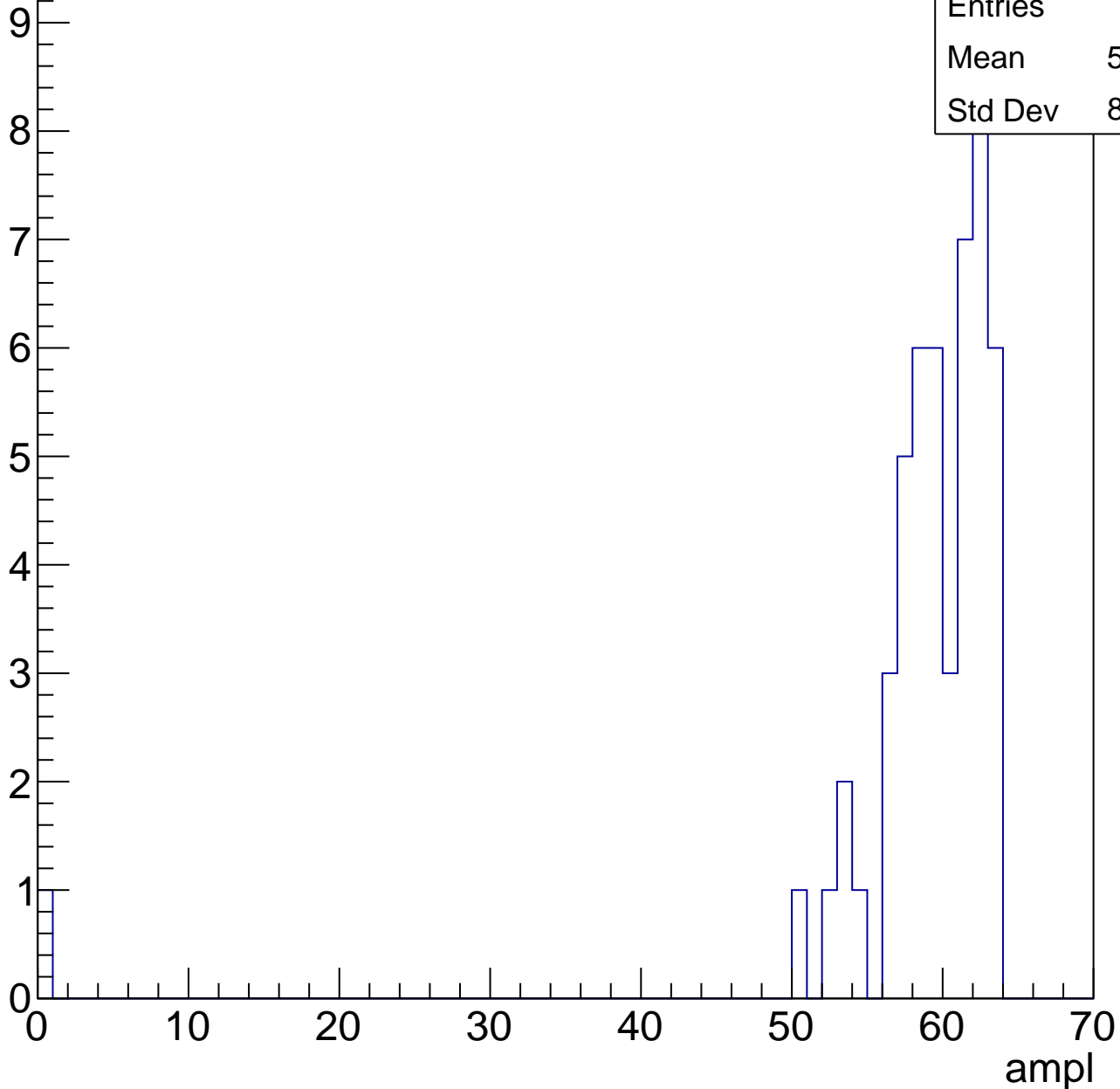


B1L103S, U23-ch10, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

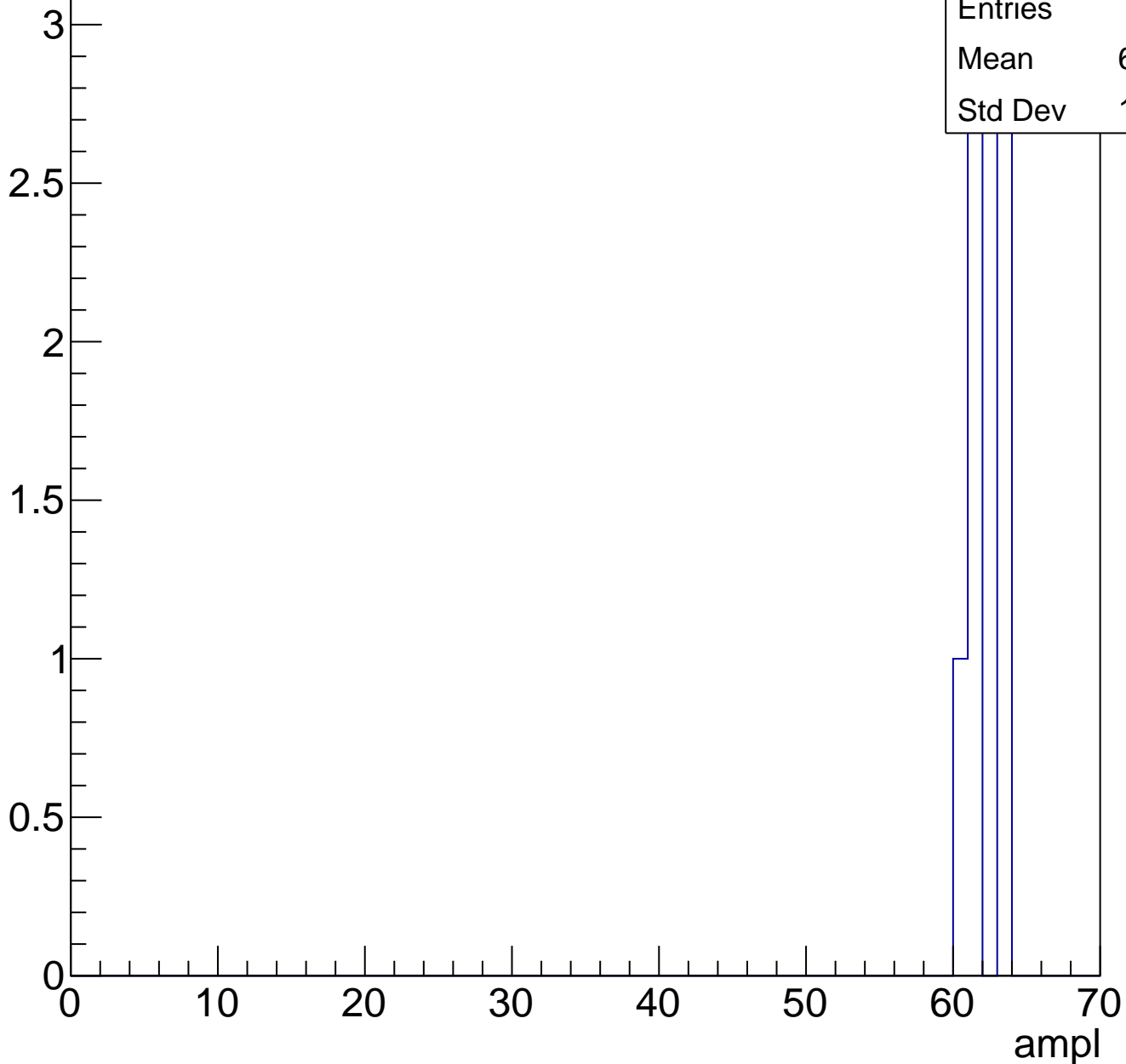
Entries	51
Mean	58.04
Std Dev	8.769



B1L103S, U23-ch10, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

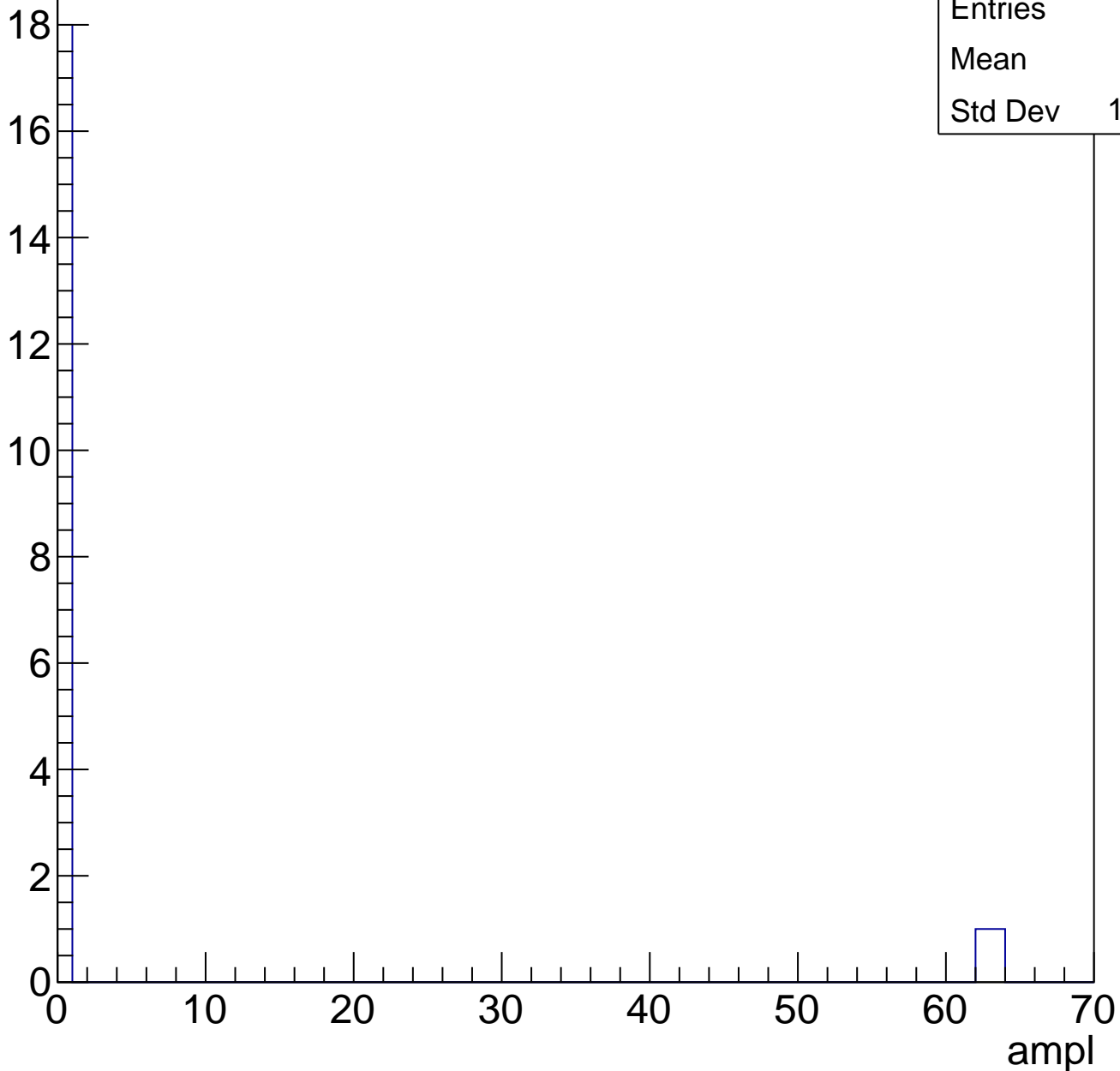


B1L103S, U23-ch10, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	6.25
Std Dev	18.75

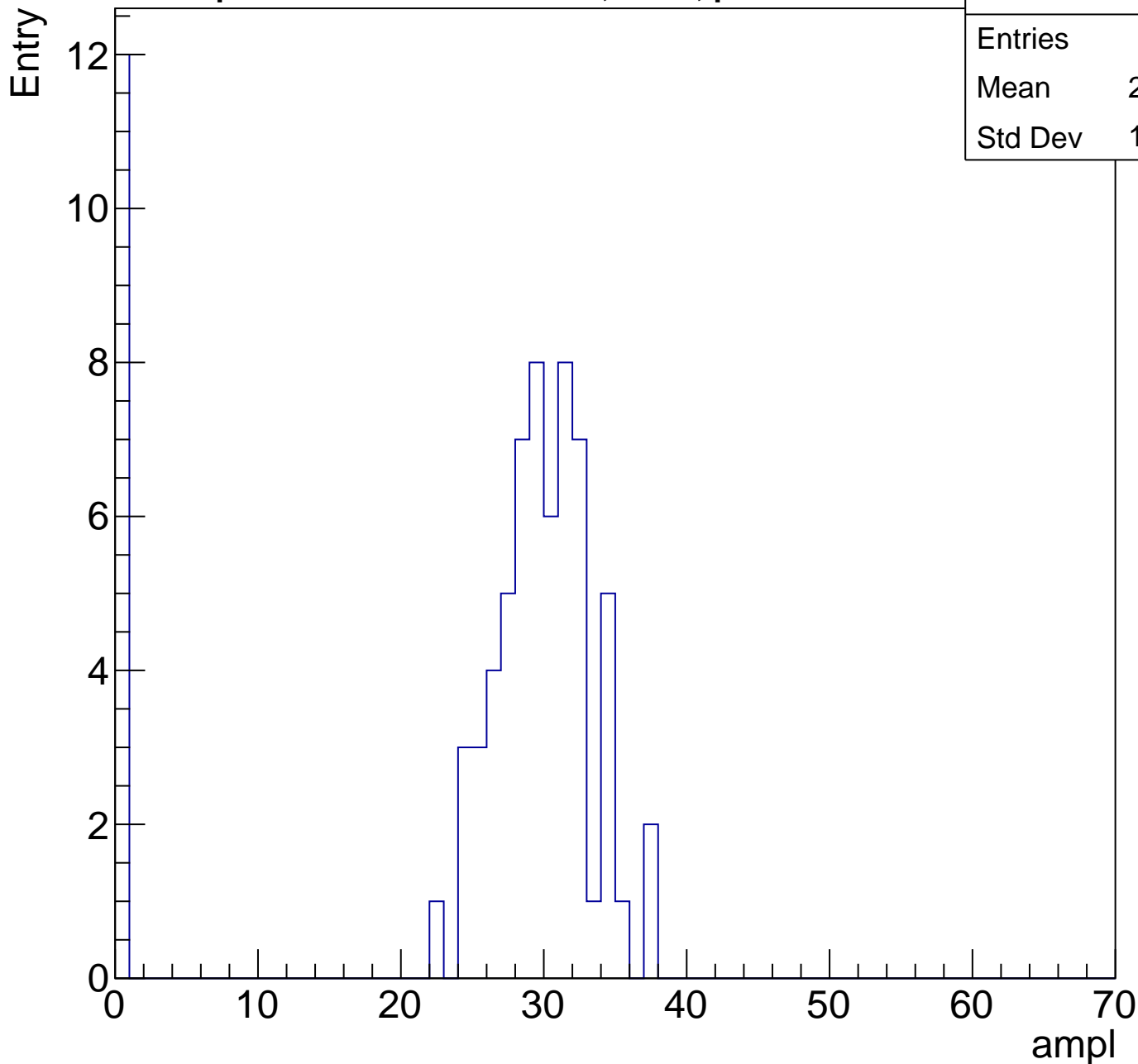
Entry



B1L103S, U23-ch11, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	73
Mean	24.66
Std Dev	11.32



B1L103S, U23-ch11, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	82
Mean	35.79
Std Dev	5.567

Entry

10
8
6
4
2
0

0

10

20

30

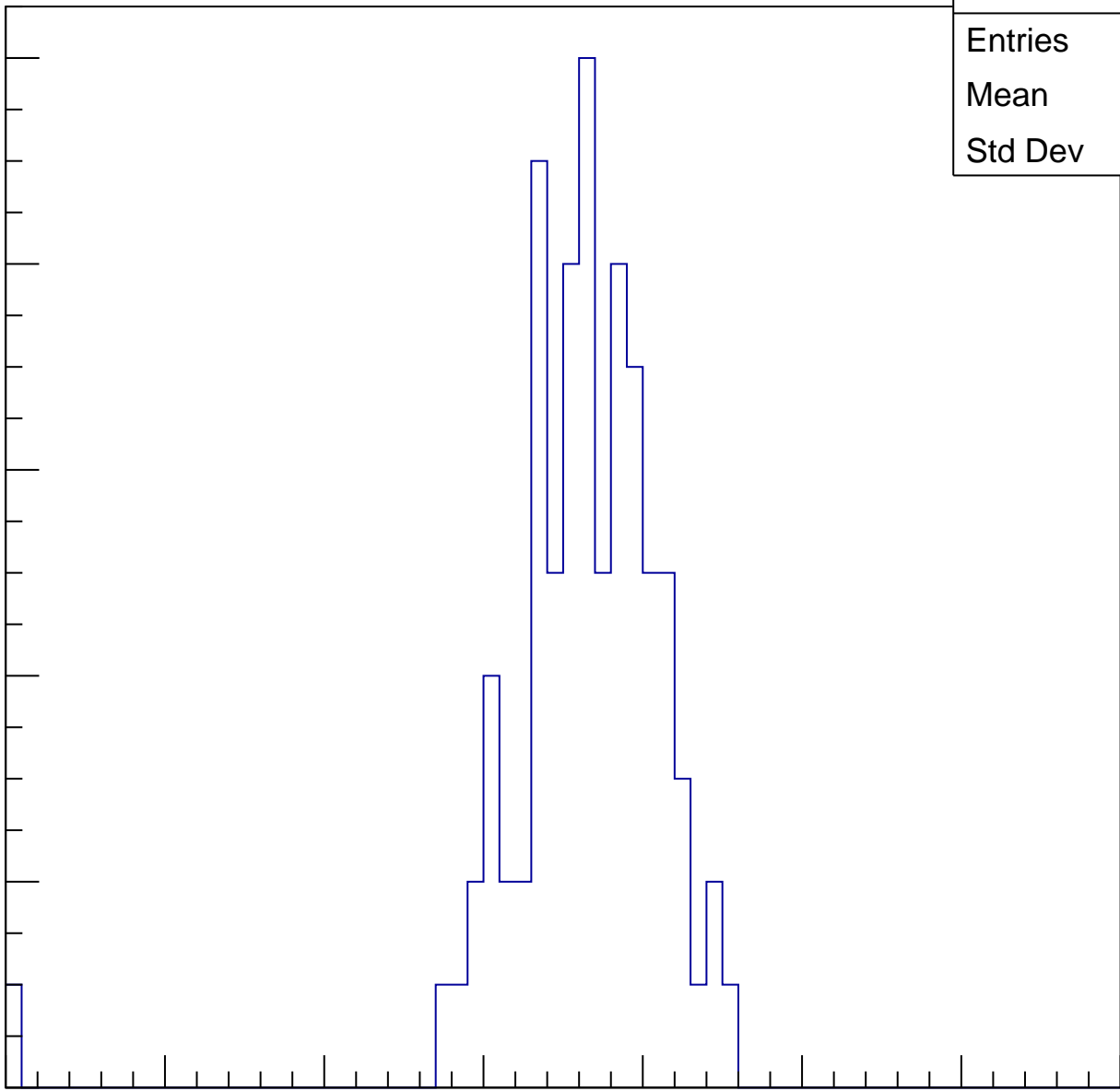
40

50

60

70

ampl



B1L103S, U23-ch11, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	71
Mean	36.61
Std Dev	16

Entry

10

8

6

4

2

0

0

10

20

30

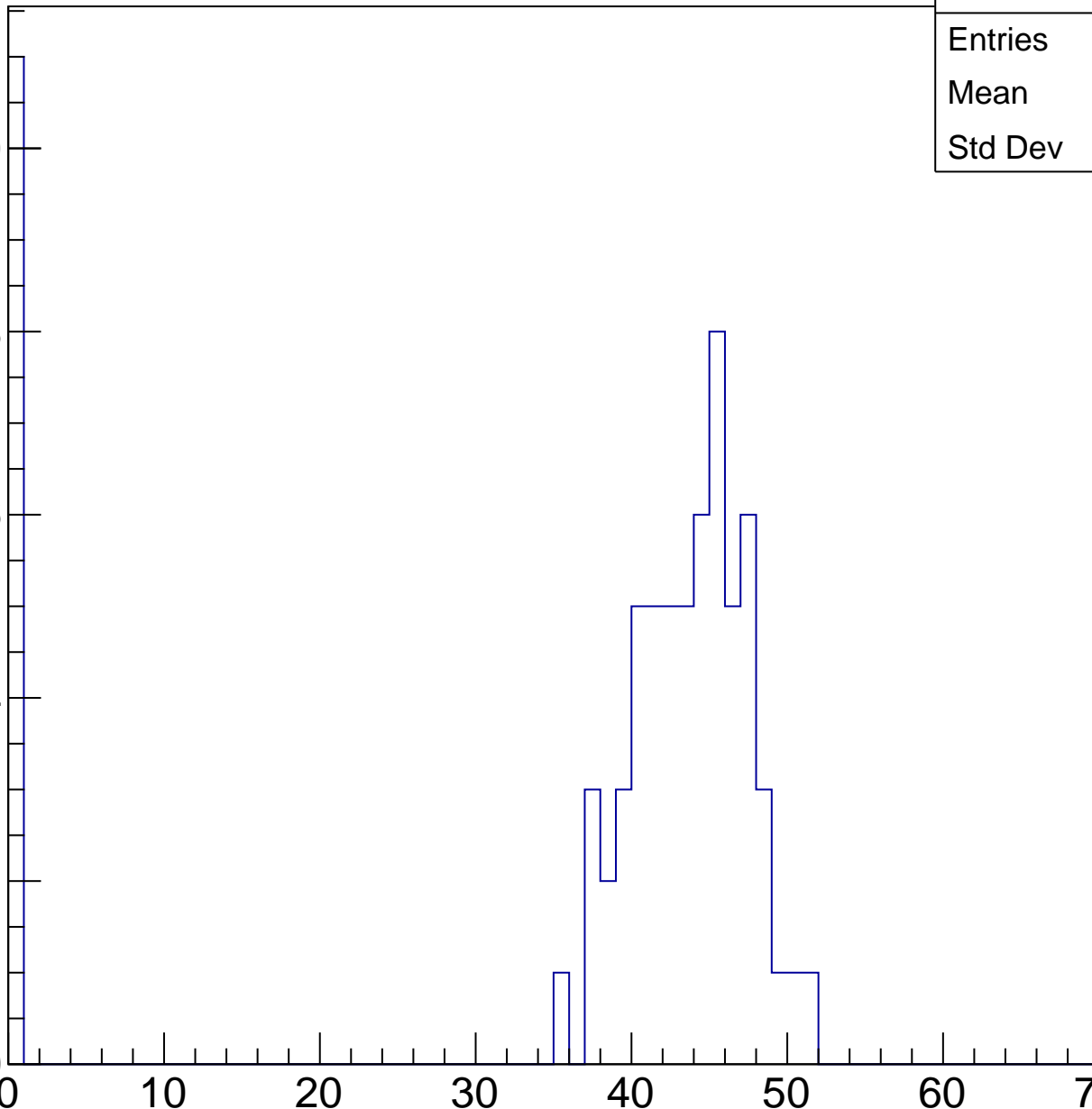
40

50

60

70

ampl

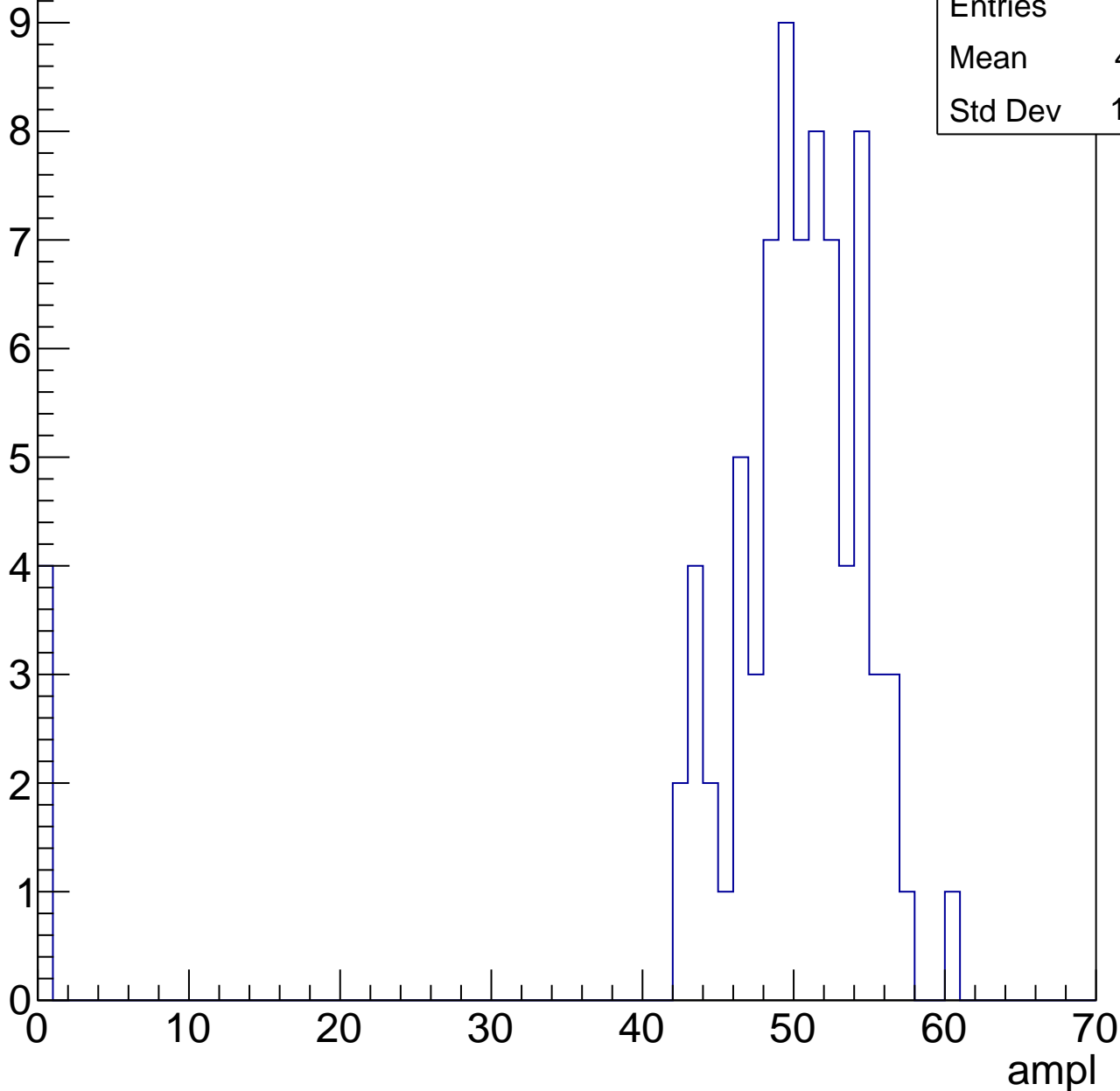


B1L103S, U23-ch11, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

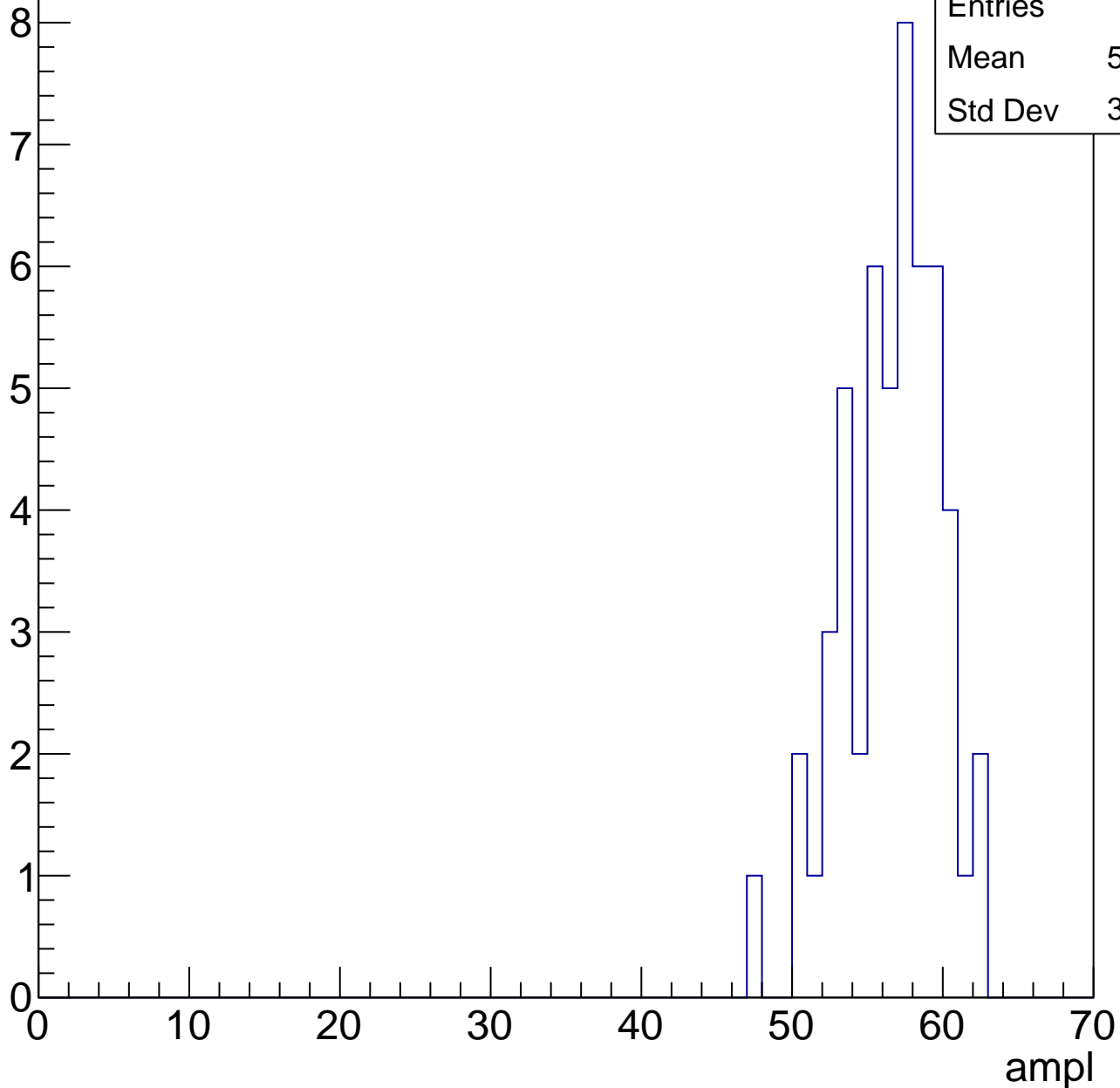
Entries	79
Mean	47.51
Std Dev	11.59



B1L103S, U23-ch11, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

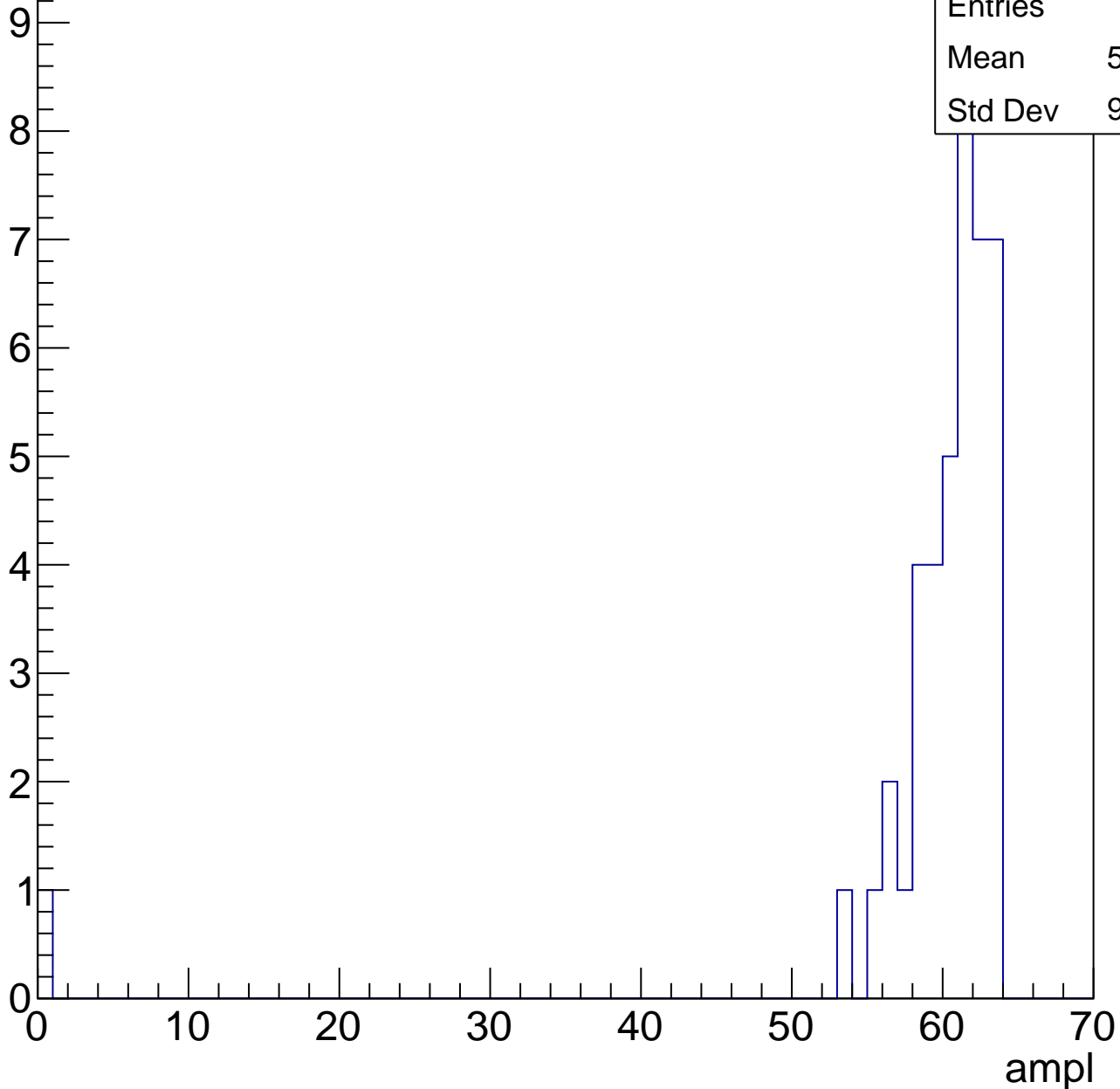


B1L103S, U23-ch11, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	42
Mean	58.79
Std Dev	9.478



B1L103S, U23-ch11, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch11, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.053
Std Dev	4.466

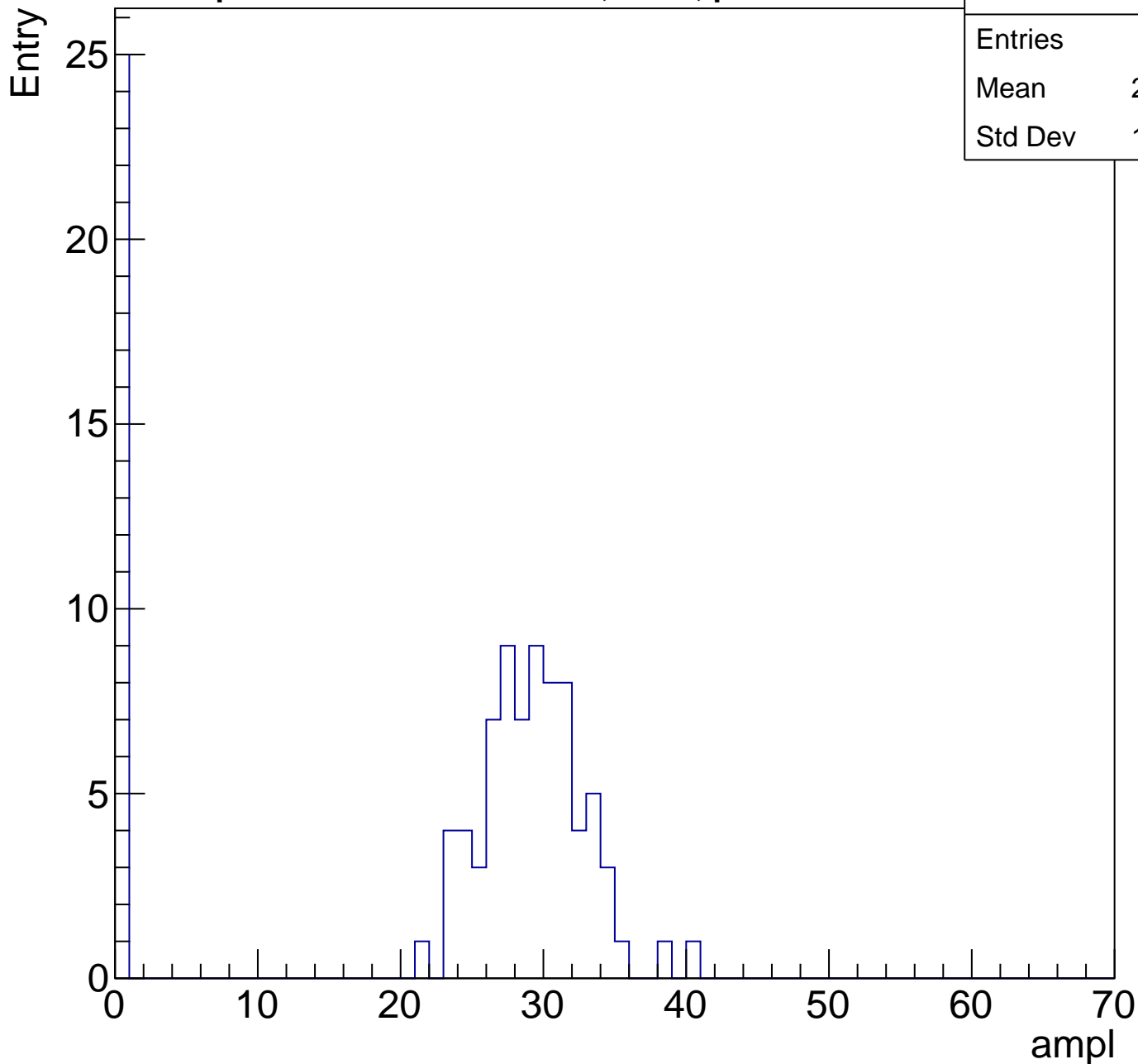
Entry



B1L103S, U23-ch12, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	100
Mean	21.62
Std Dev	12.85

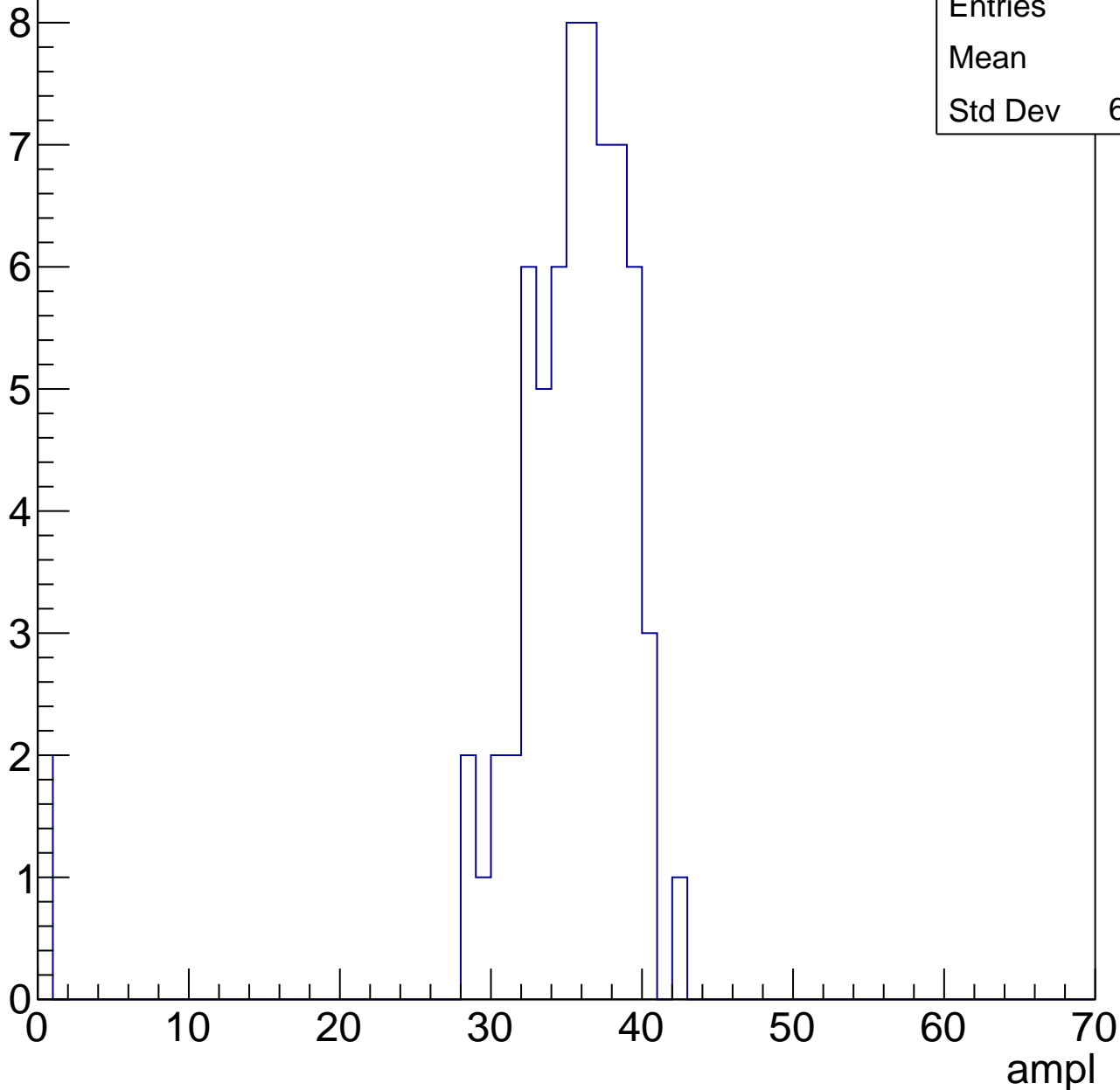


B1L103S, U23-ch12, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	34.2
Std Dev	6.767

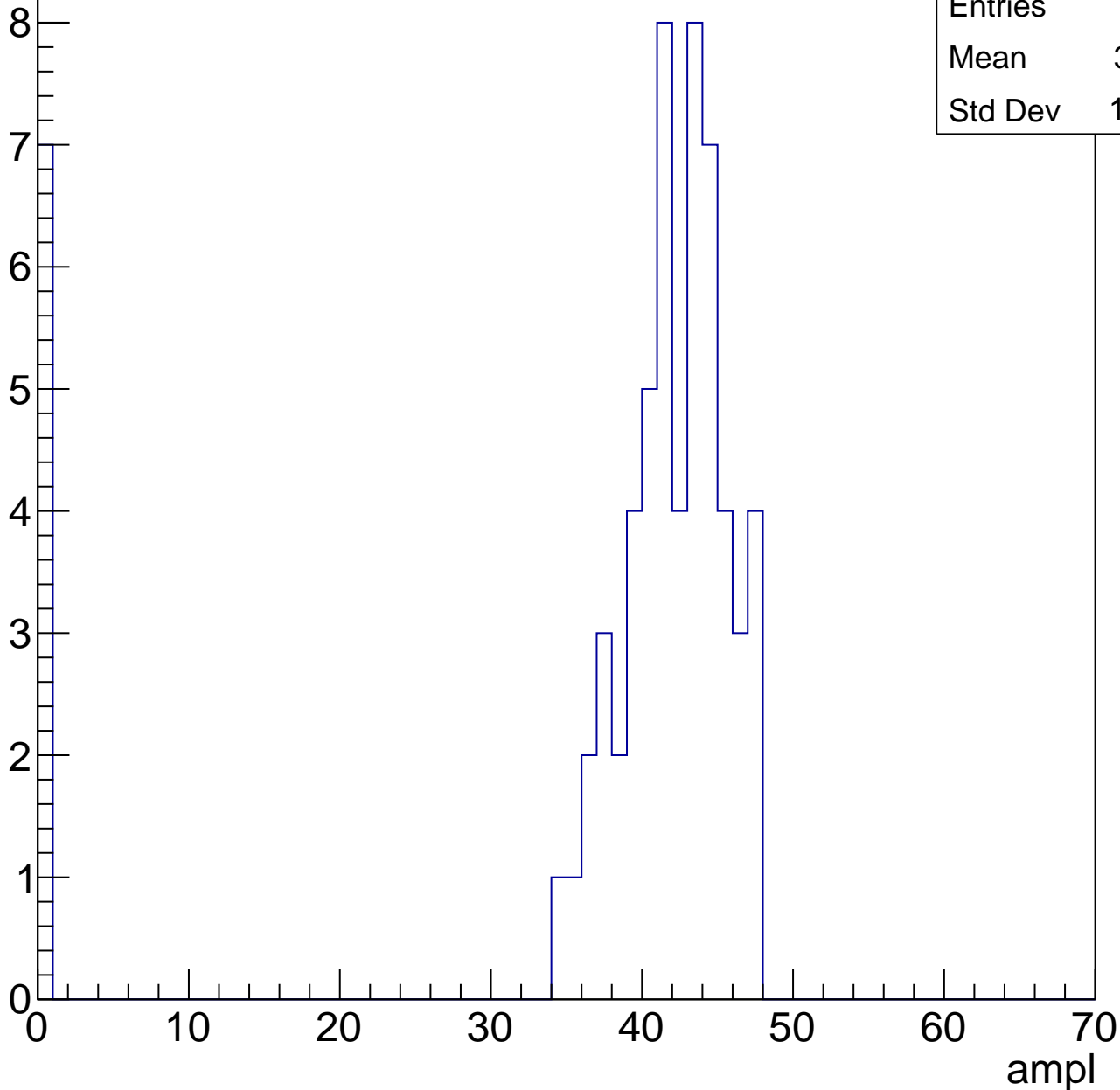


B1L103S, U23-ch12, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	63
Mean	37.11
Std Dev	13.46



B1L103S, U23-ch12, adc3

calib_packv5_041523_1651.root, FC#0, port C2

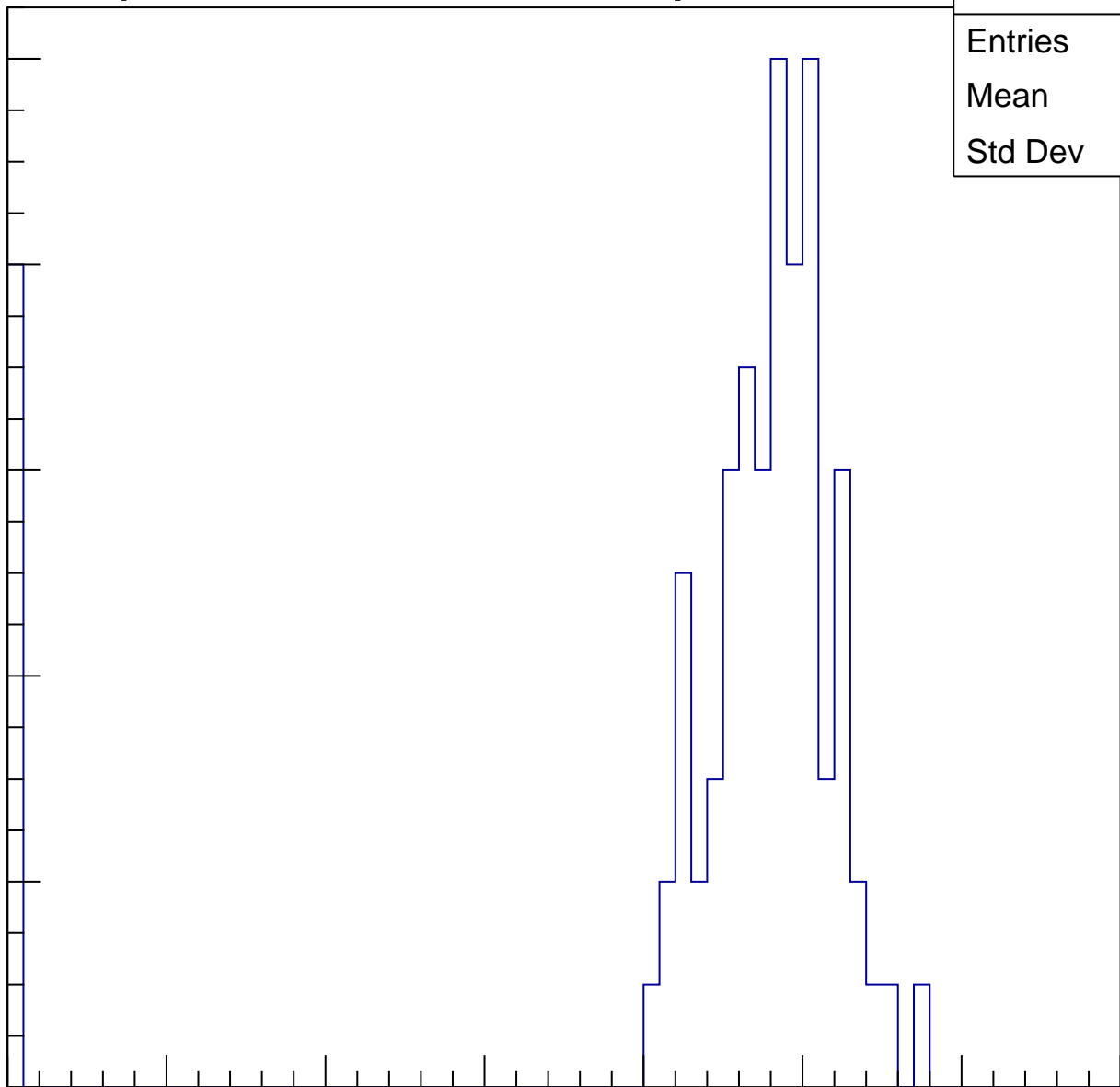
Entries	82
Mean	43.09
Std Dev	14.55

Entry

10
8
6
4
2
0

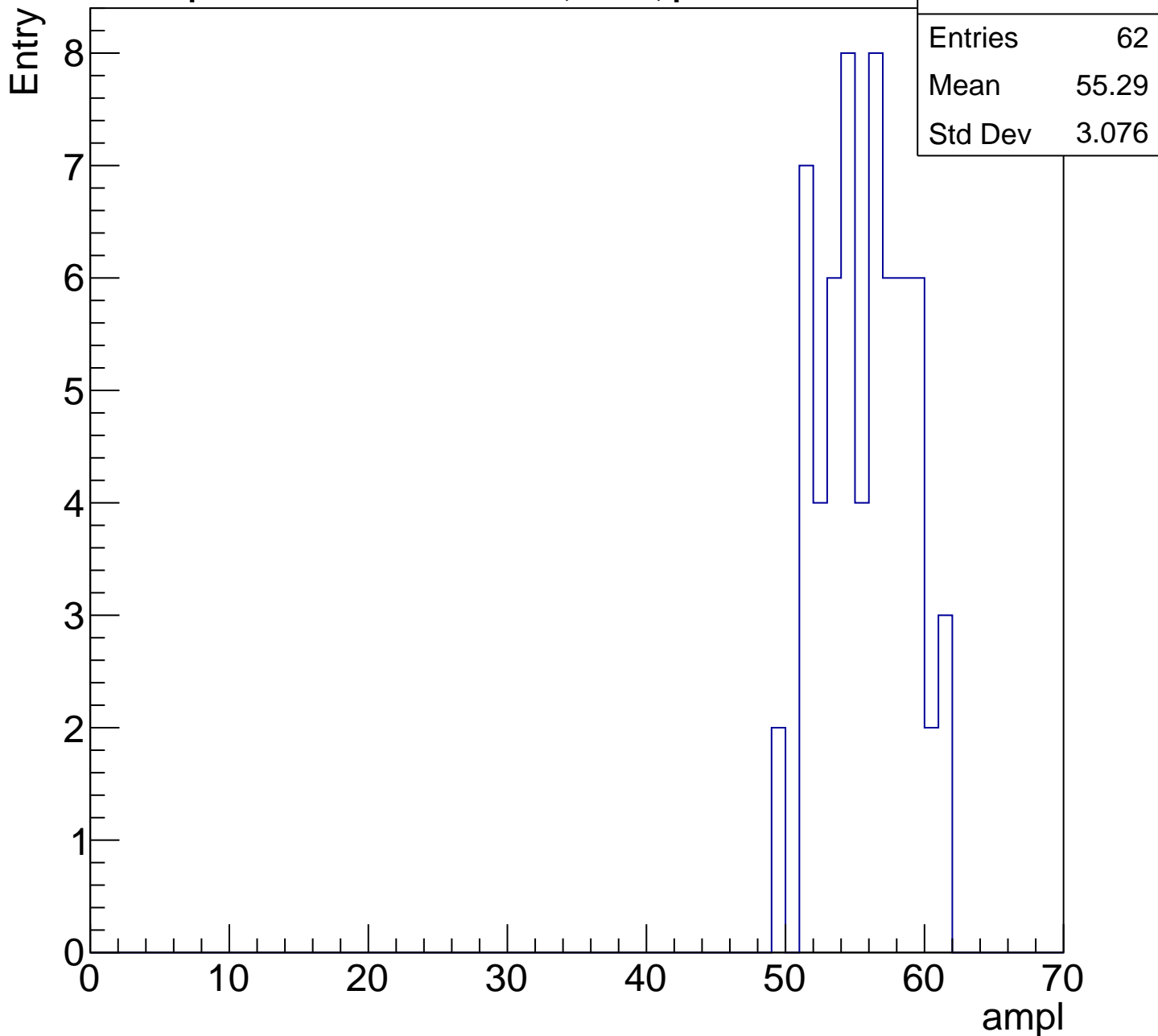
0 10 20 30 40 50 60 70

ampl



B1L103S, U23-ch12, adc4

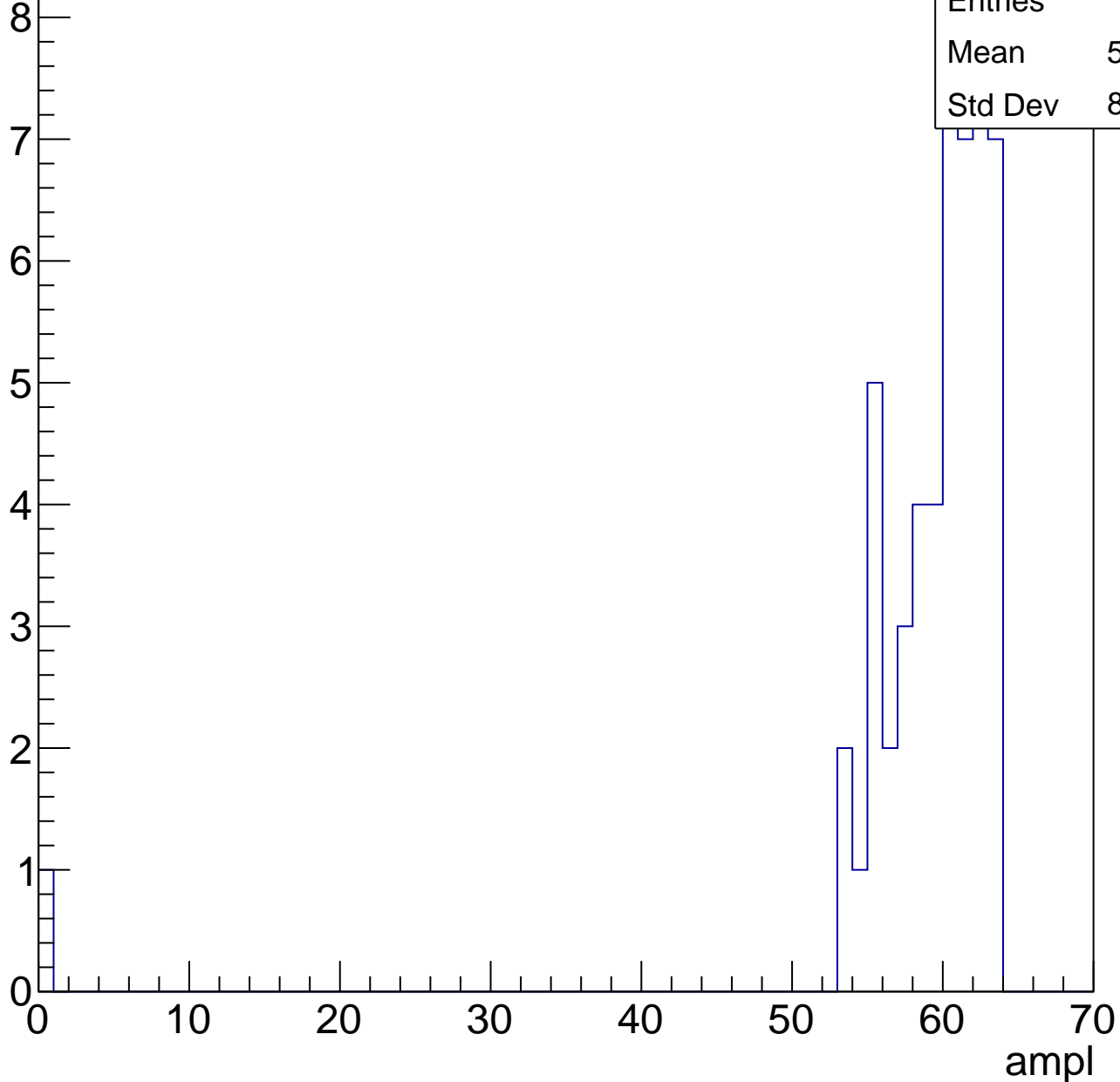
calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U23-ch12, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch12, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch12, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U23-ch13, adc0

calib_packv5_041523_1651.root, FC#0, port C2

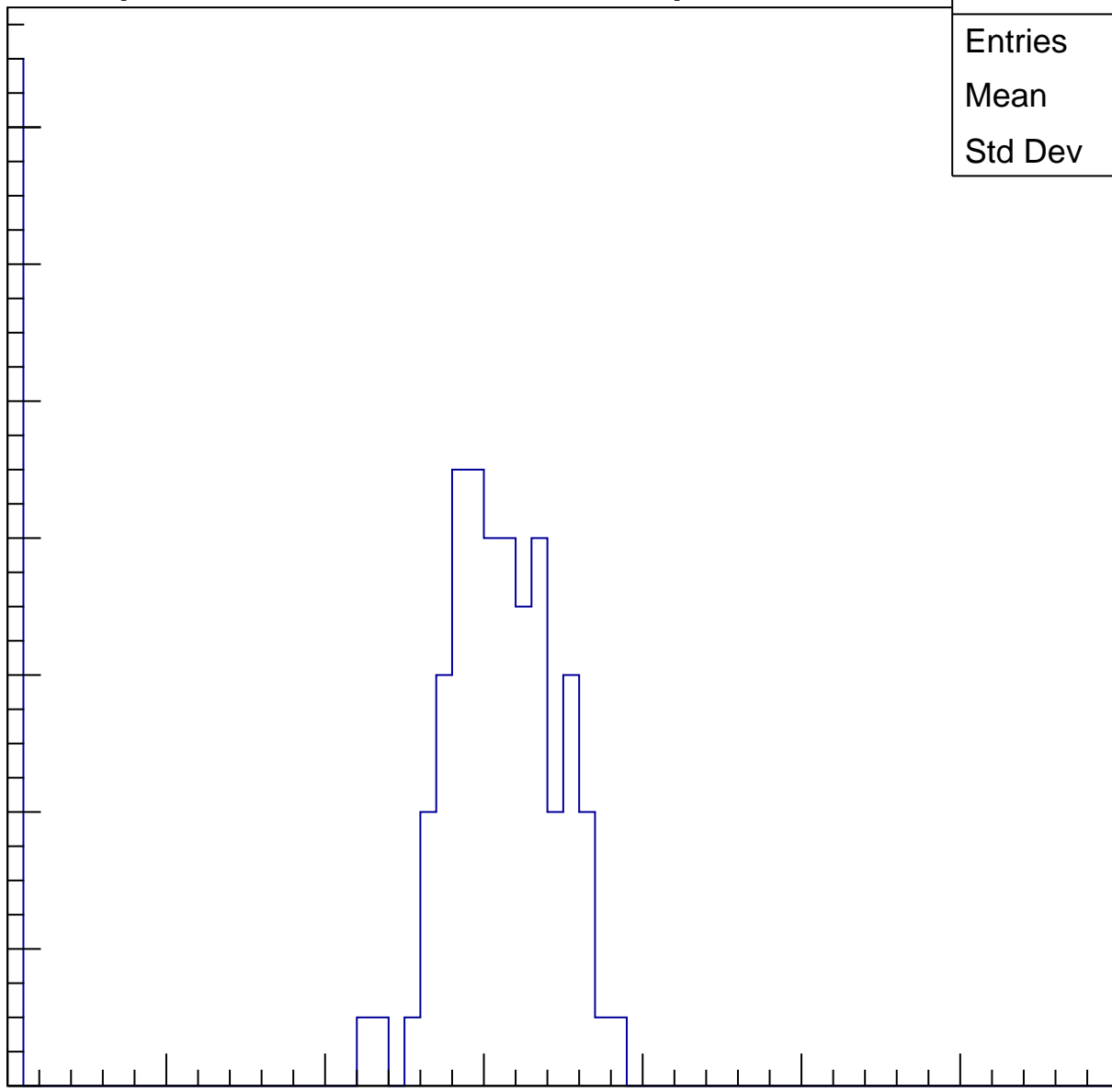
Entries	93
Mean	25.7
Std Dev	11.67

Entry

14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

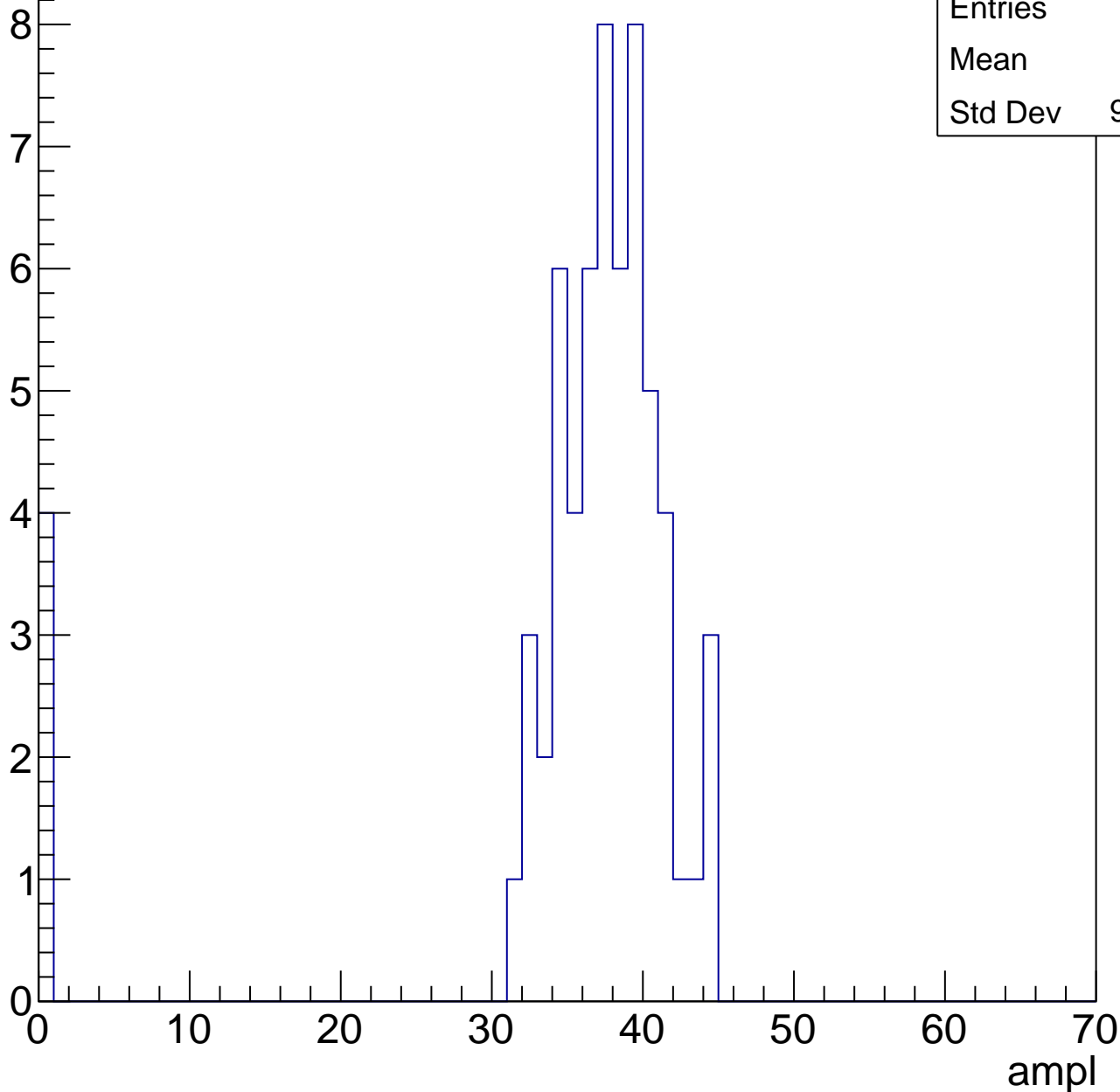


B1L103S, U23-ch13, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	35
Std Dev	9.674

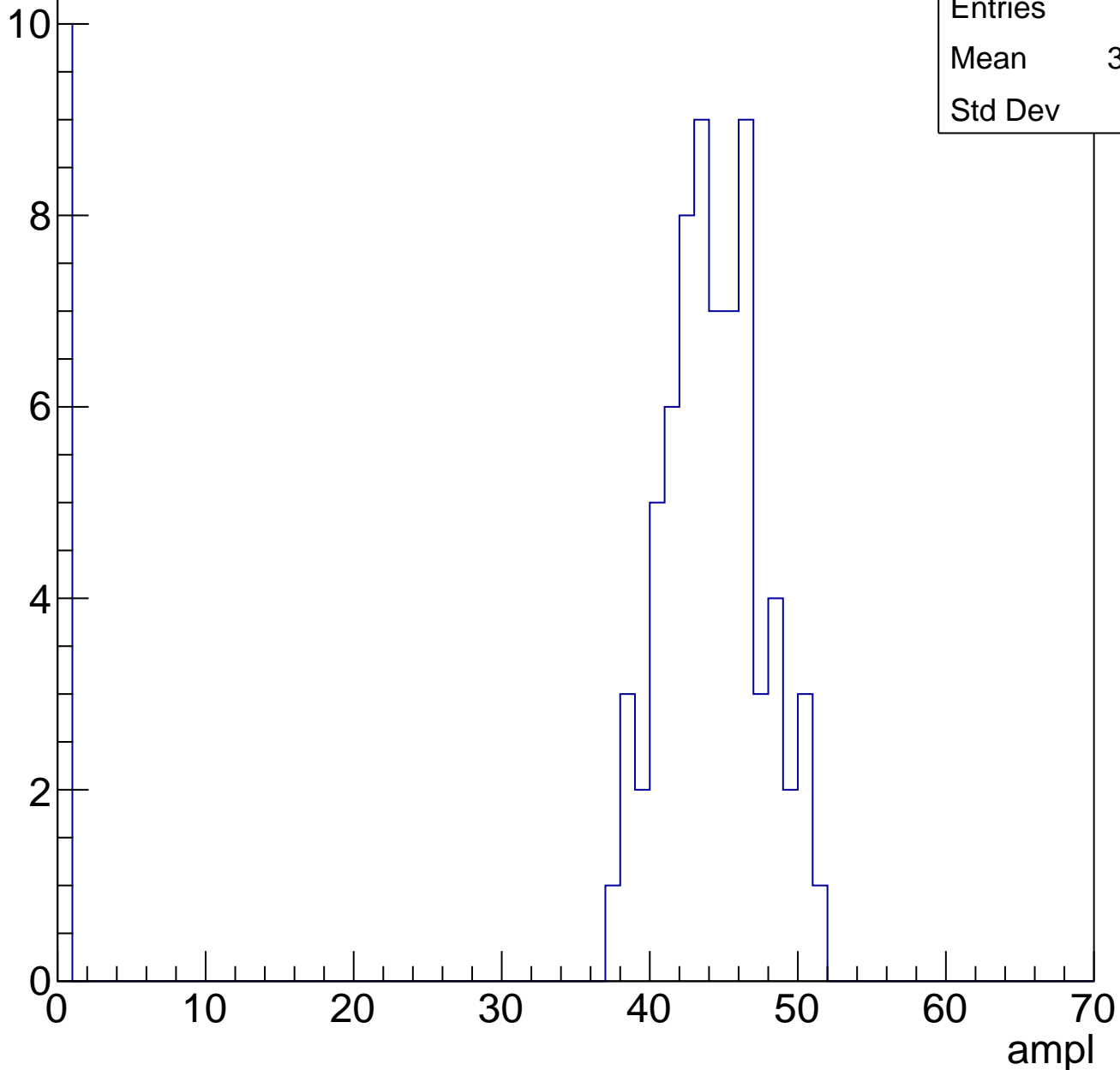


B1L103S, U23-ch13, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	80
Mean	38.34
Std Dev	14.8

Entry

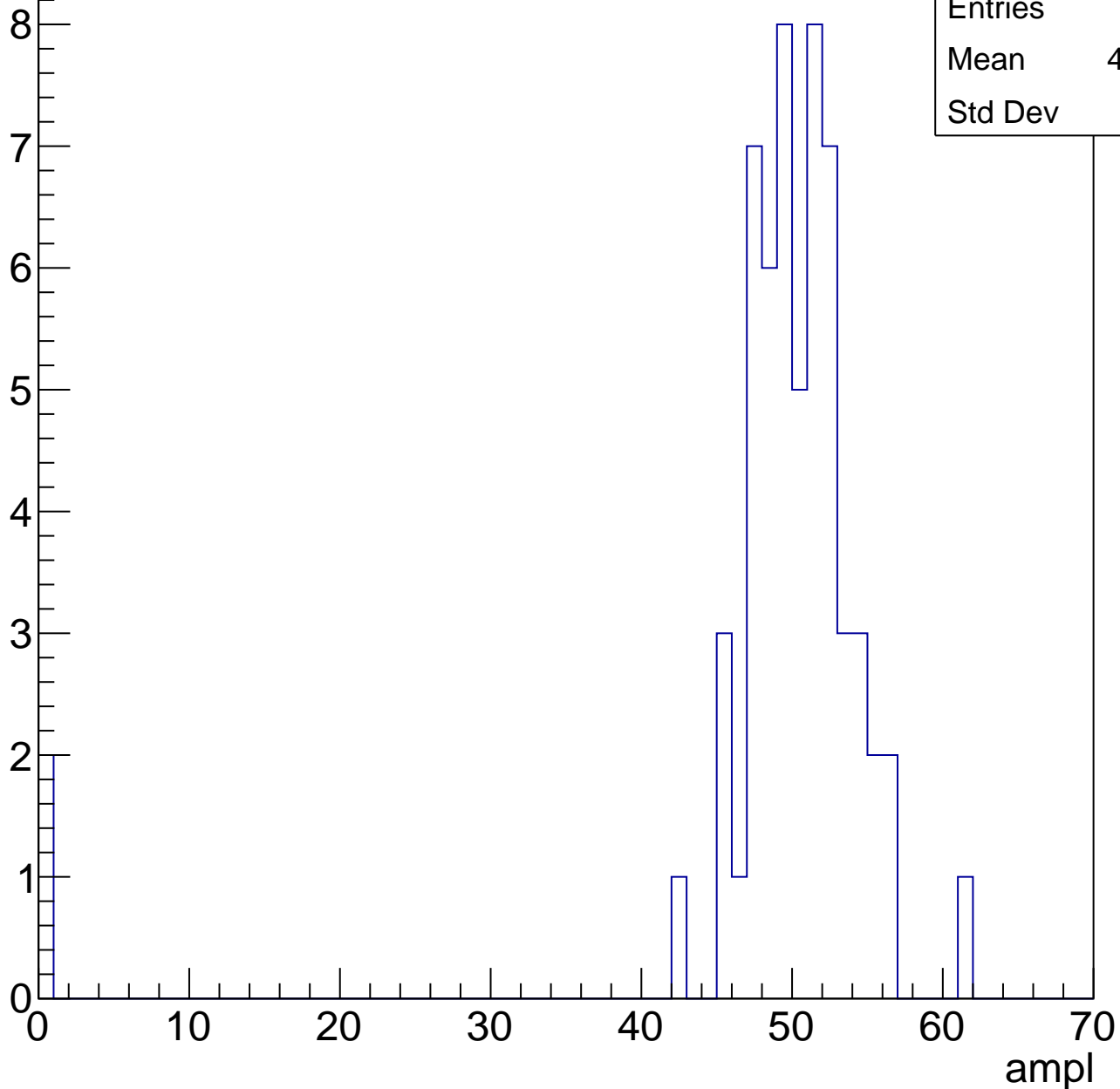


B1L103S, U23-ch13, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	48.44
Std Dev	9.62

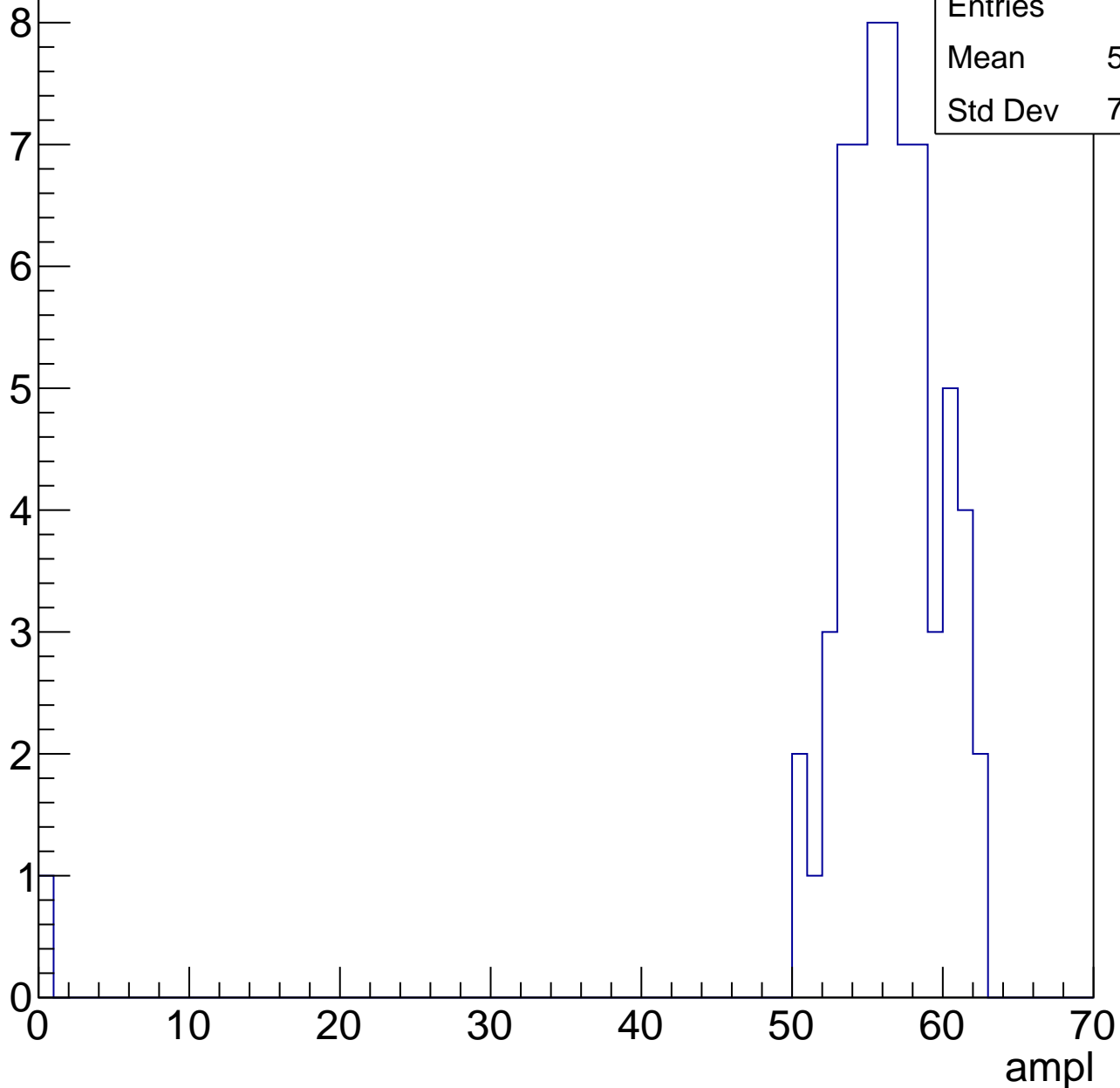


B1L103S, U23-ch13, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

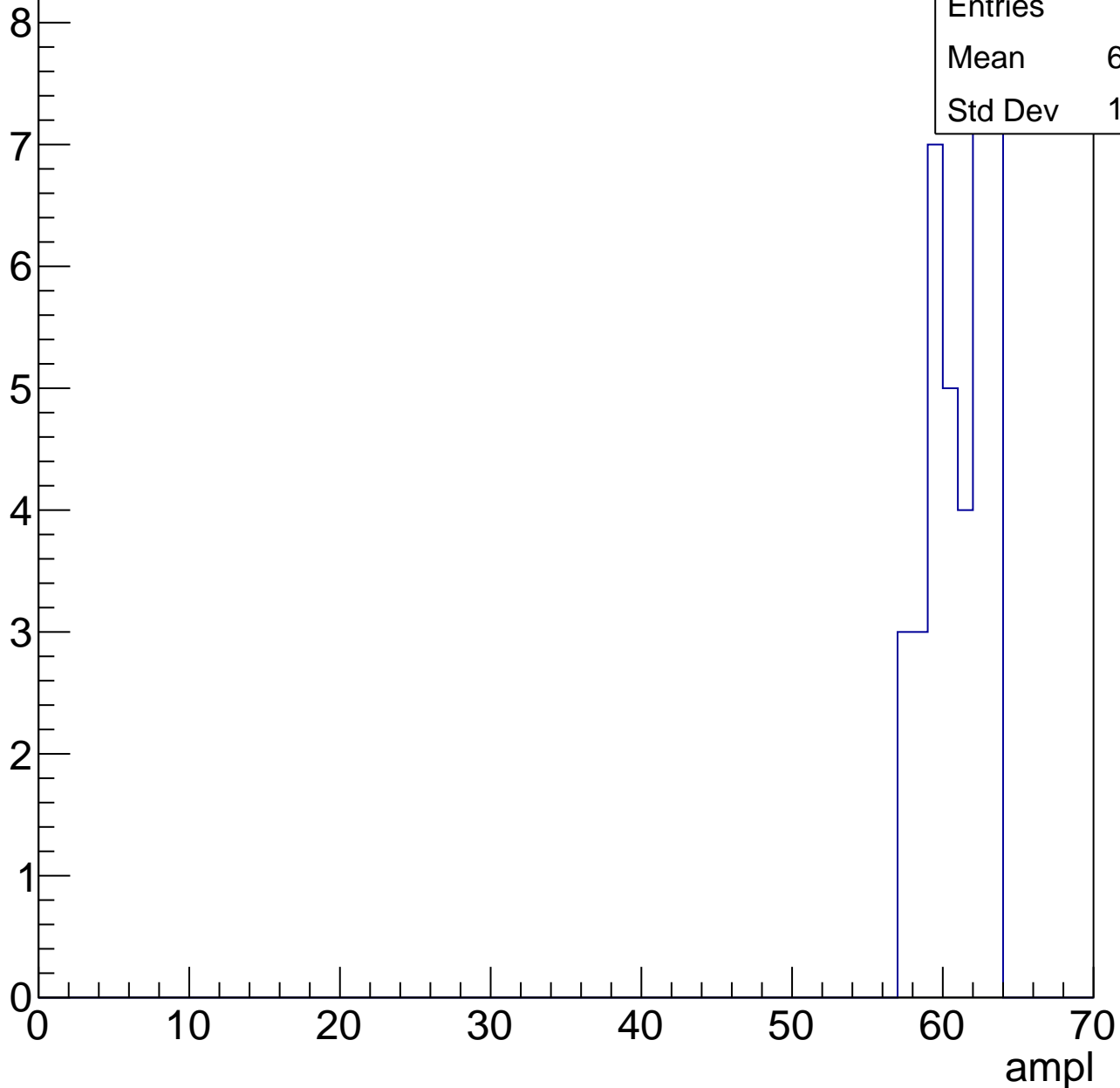
Entries	65
Mean	55.29
Std Dev	7.505



B1L103S, U23-ch13, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	38
Mean	60.58
Std Dev	1.928

B1L103S, U23-ch13, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	3
Mean	62.33
Std Dev	0.9428

0 10 20 30 40 50 60 70

ampl

1

B1L103S, U23-ch13, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

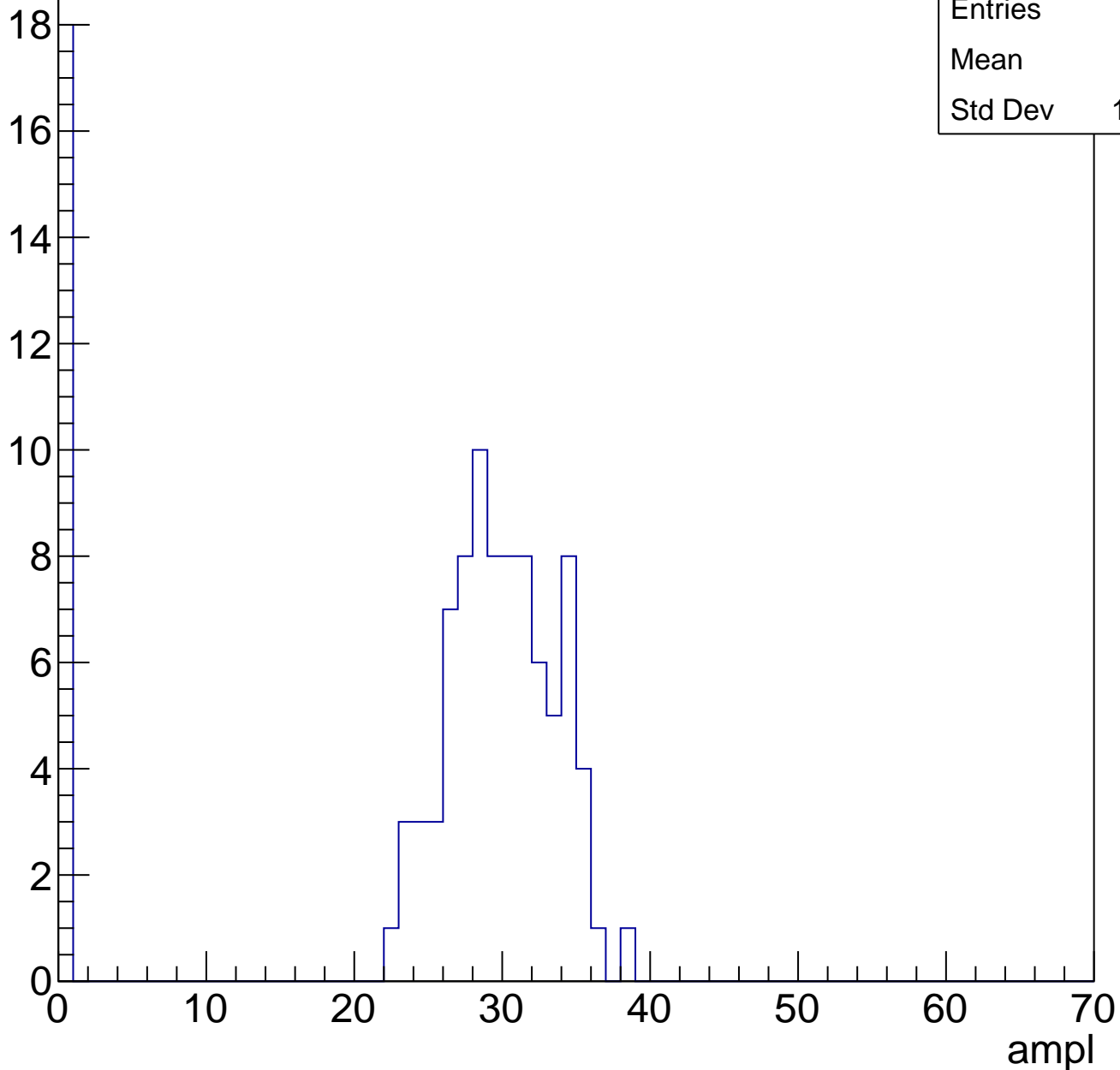
Entries	19
Mean	0
Std Dev	0

B1L103S, U23-ch14, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	102
Mean	24.3
Std Dev	11.68

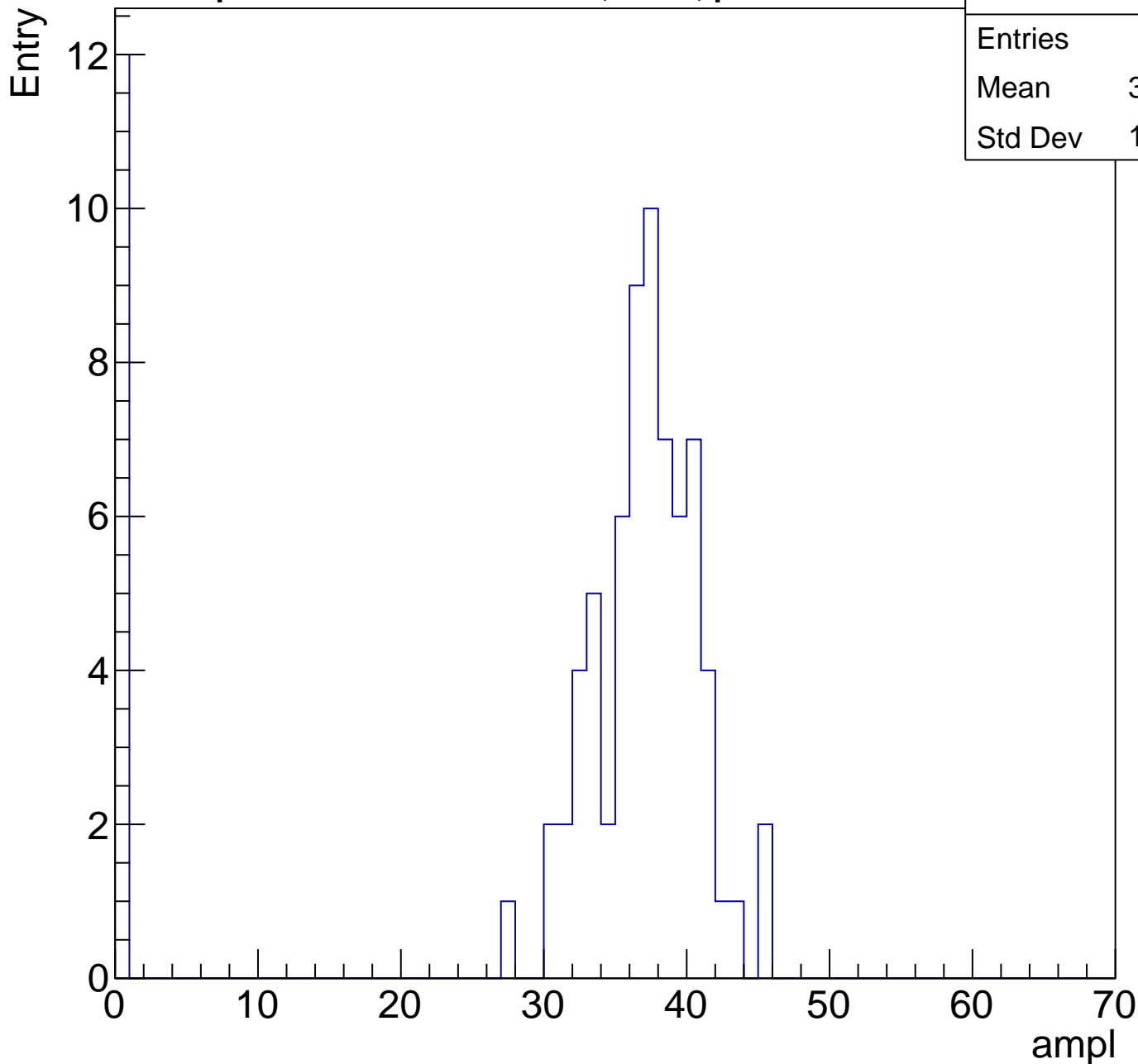
Entry



B1L103S, U23-ch14, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	81
Mean	31.27
Std Dev	13.43

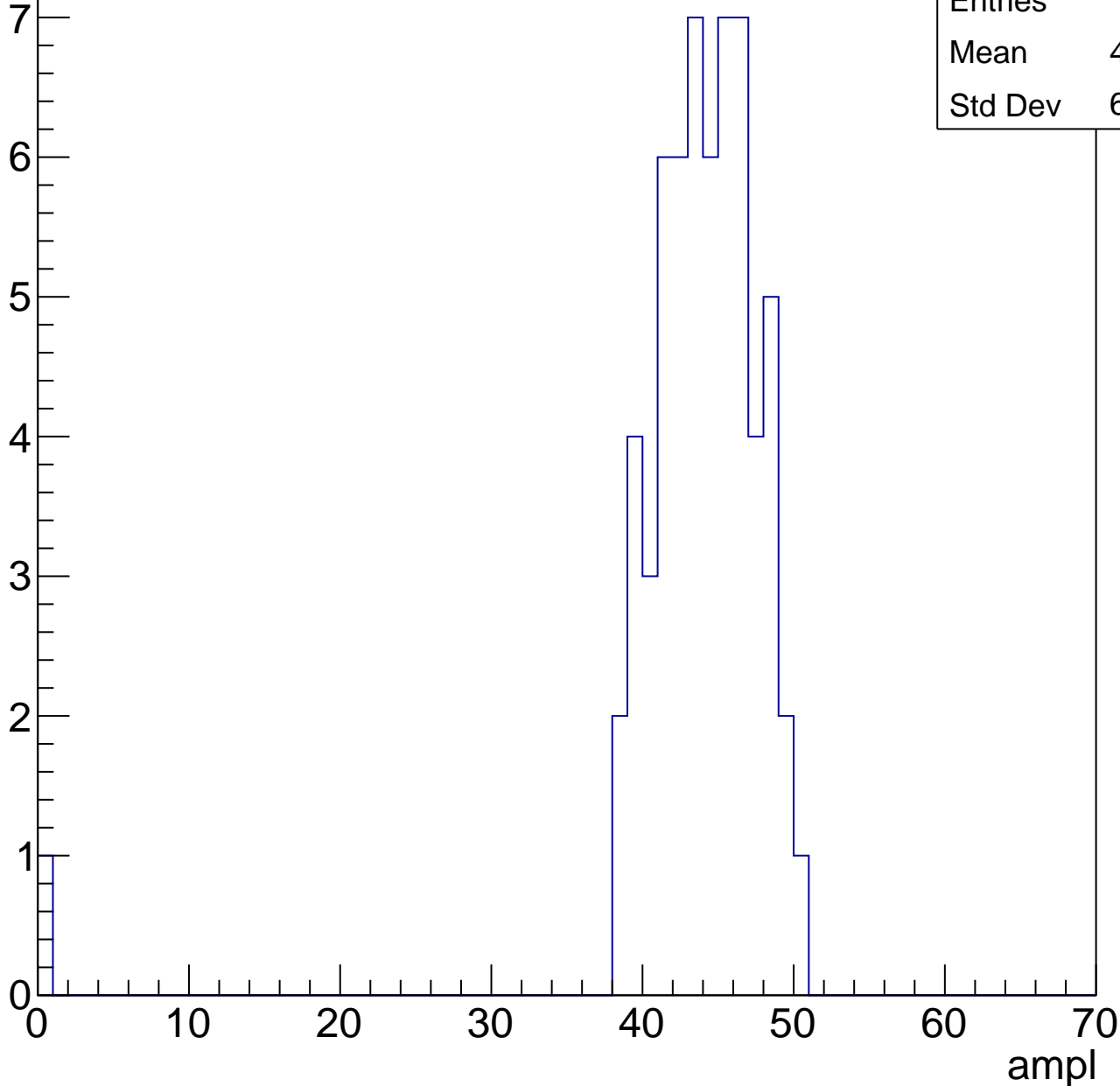


B1L103S, U23-ch14, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	43.08
Std Dev	6.307

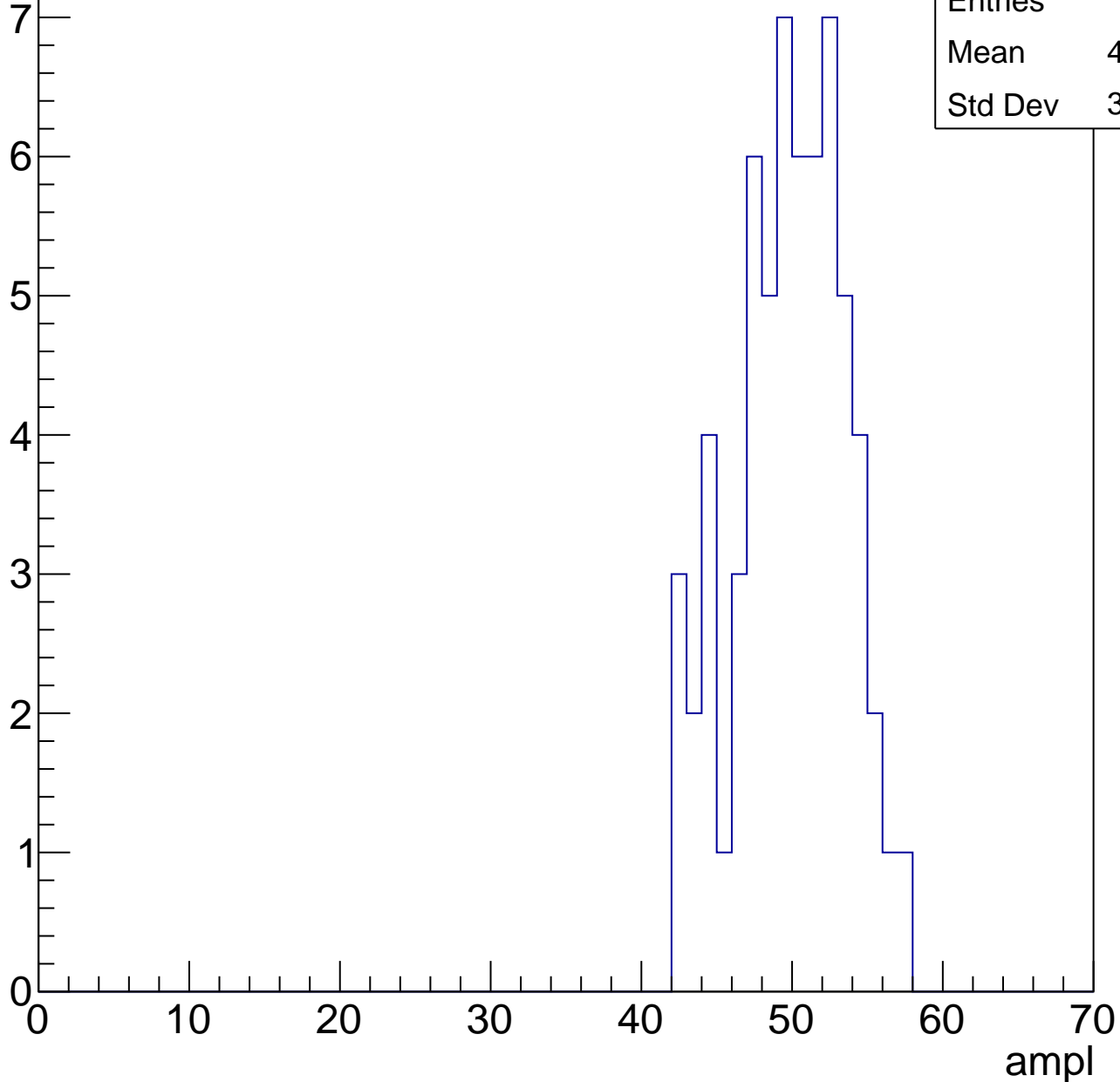


B1L103S, U23-ch14, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	63
Mean	49.37
Std Dev	3.653

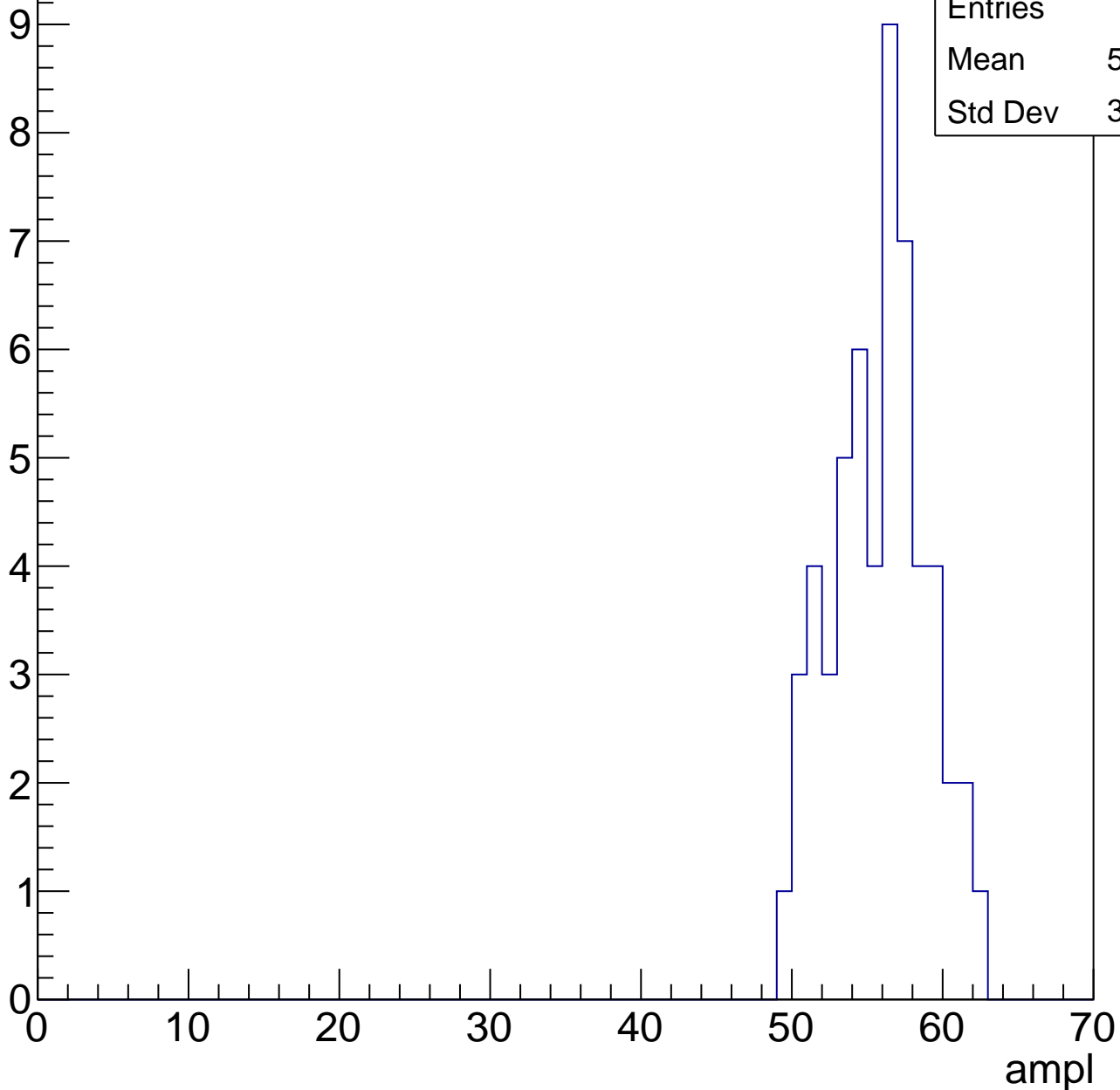


B1L103S, U23-ch14, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	55.33
Std Dev	3.105

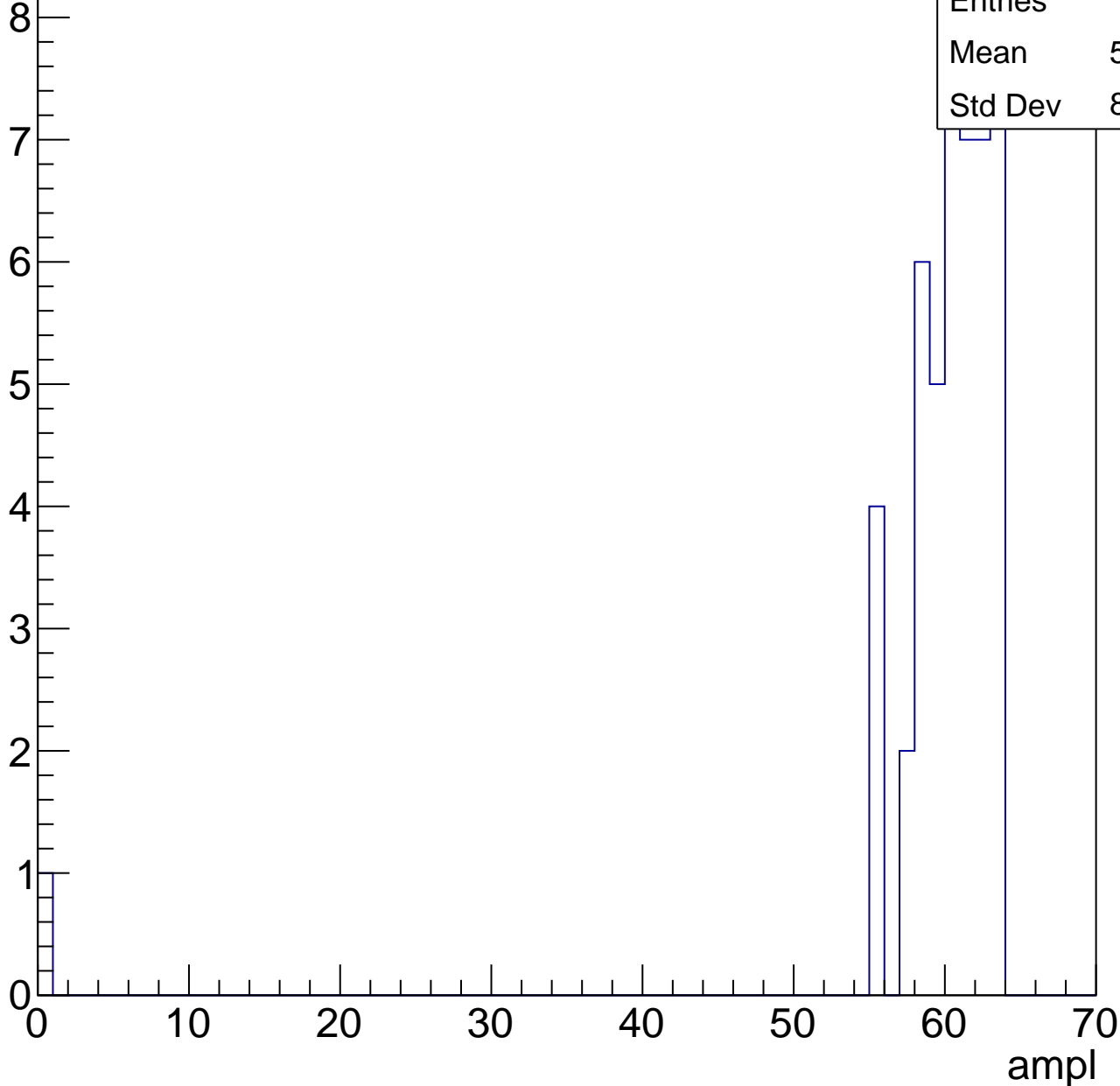


B1L103S, U23-ch14, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	48
Mean	58.79
Std Dev	8.879



B1L103S, U23-ch14, adc6

calib_packv5_041523_1651.root, FC#0, port C2

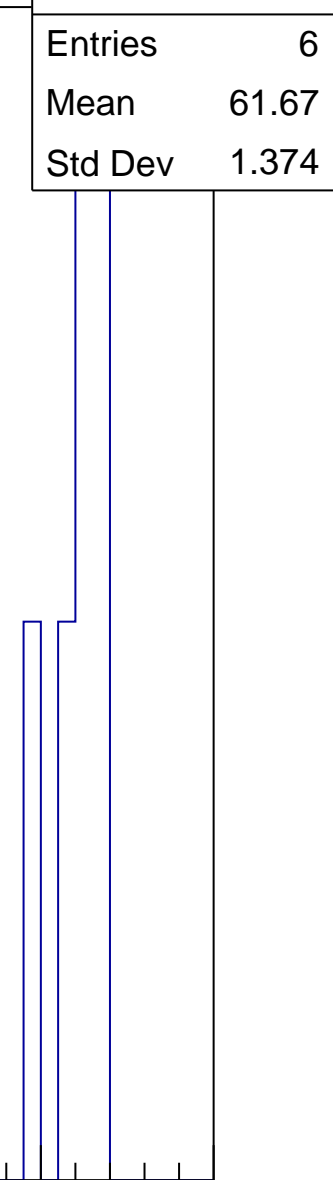
Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	6
Mean	61.67
Std Dev	1.374

0 10 20 30 40 50 60 70

ampl



B1L103S, U23-ch14, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U23-ch15, adc0

calib_packv5_041523_1651.root, FC#0, port C2

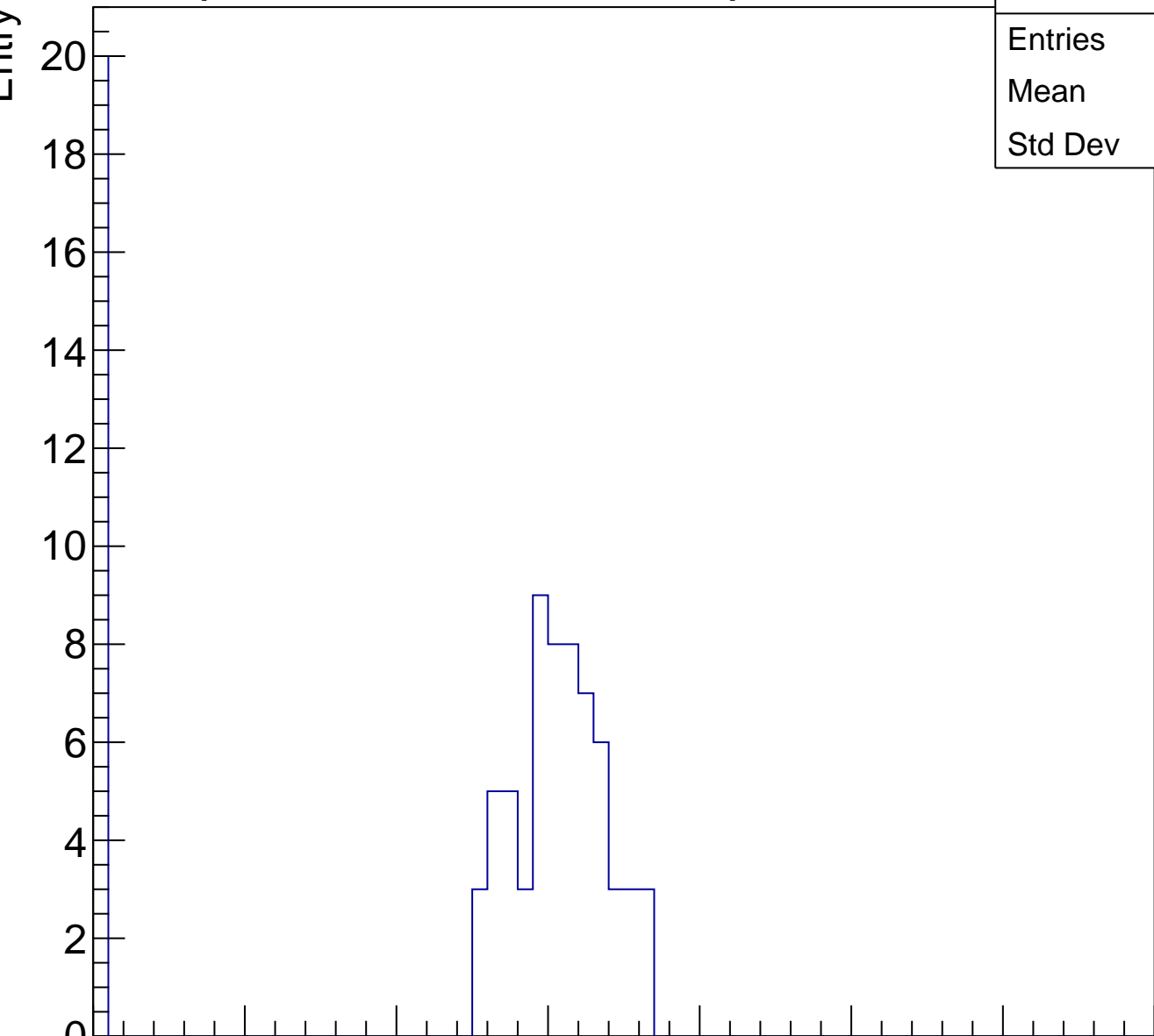
Entries	83
Mean	23.01
Std Dev	13.21

Entry

20
18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

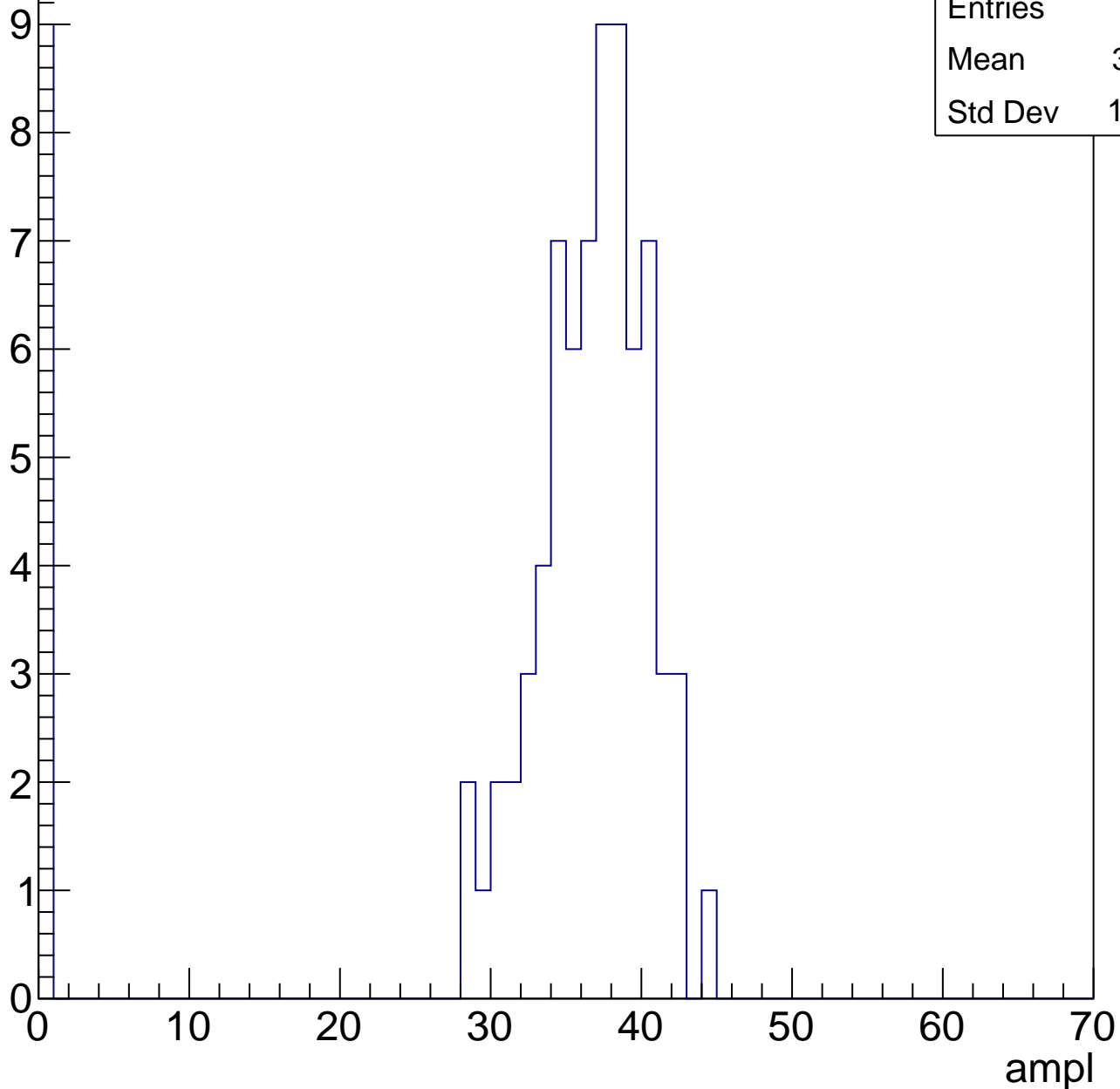


B1L103S, U23-ch15, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	81
Mean	32.31
Std Dev	11.88

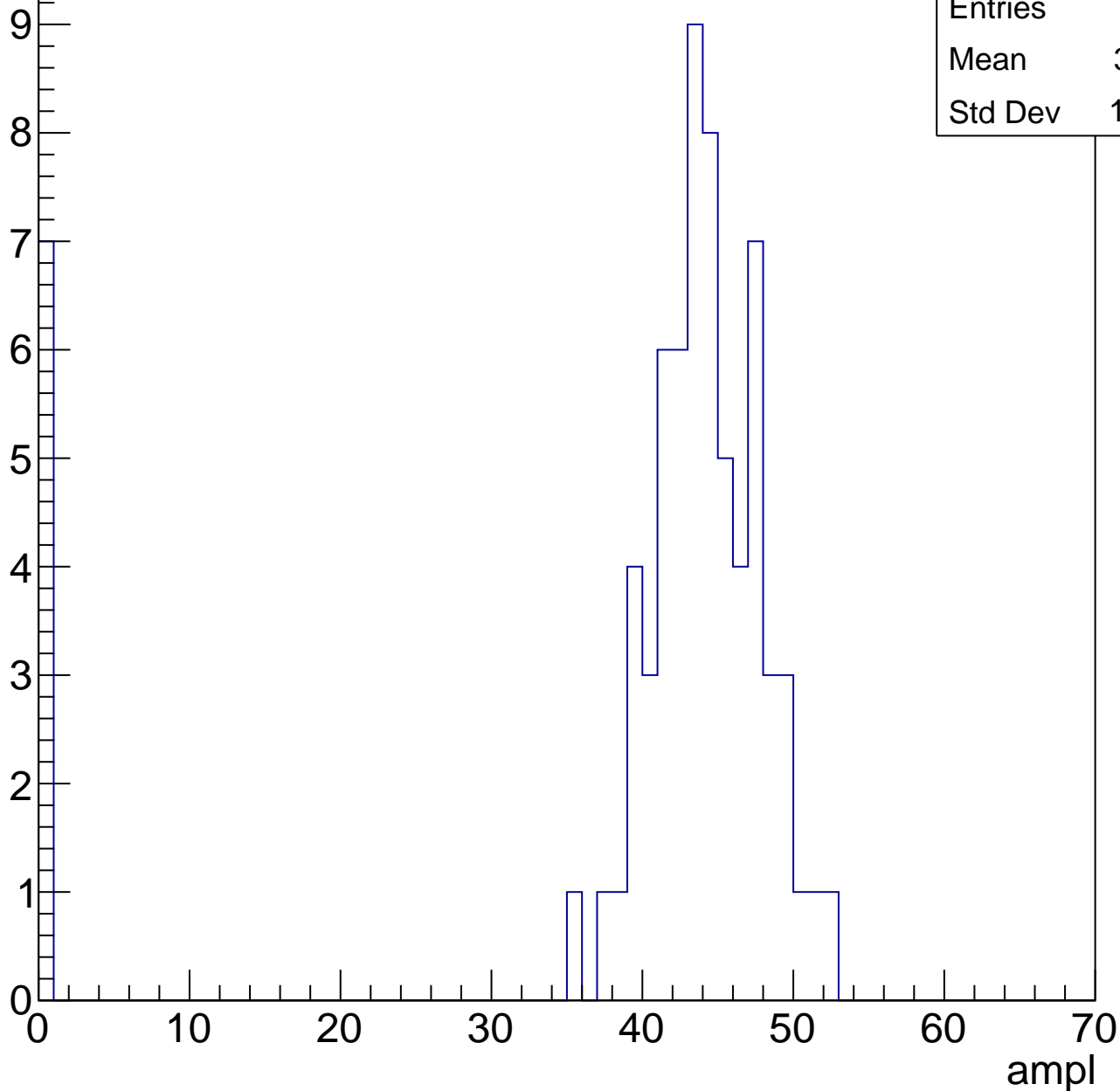


B1L103S, U23-ch15, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	39.51
Std Dev	13.47

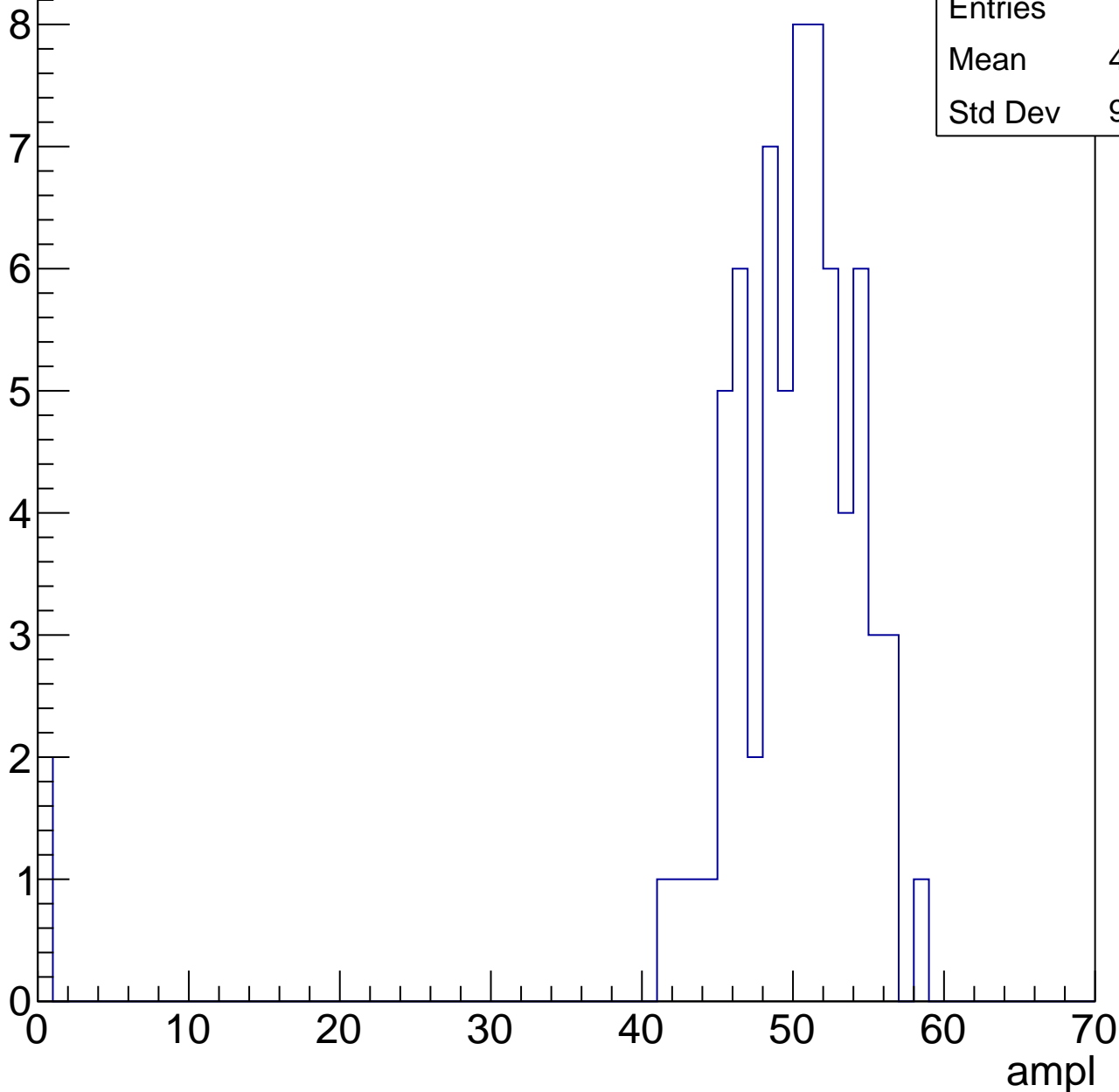


B1L103S, U23-ch15, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	48.47
Std Dev	9.063

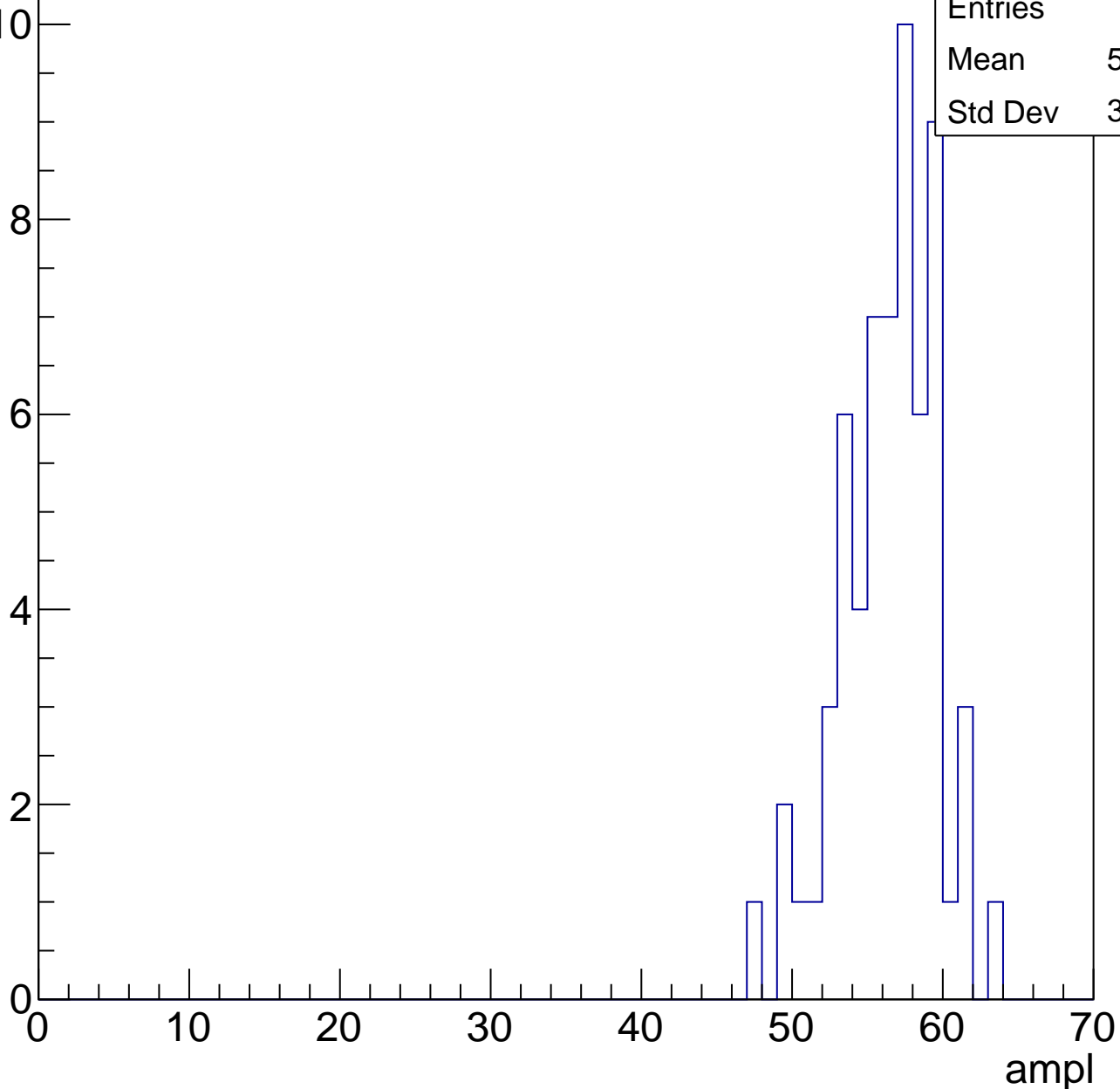


B1L103S, U23-ch15, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

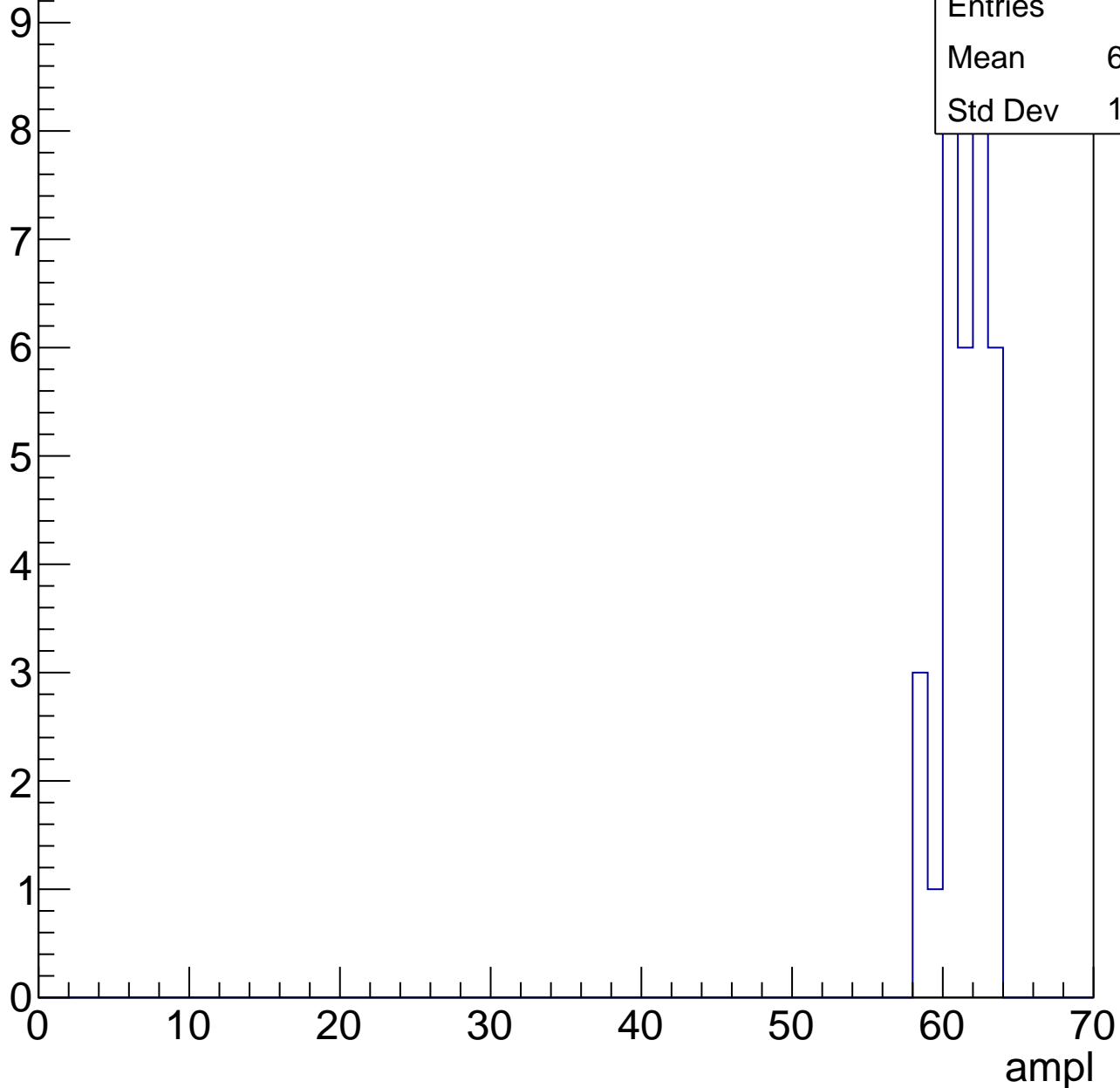
Entries	62
Mean	55.94
Std Dev	3.162



B1L103S, U23-ch15, adc5

calib_packv5_041523_1651.root, FC#0, port C2

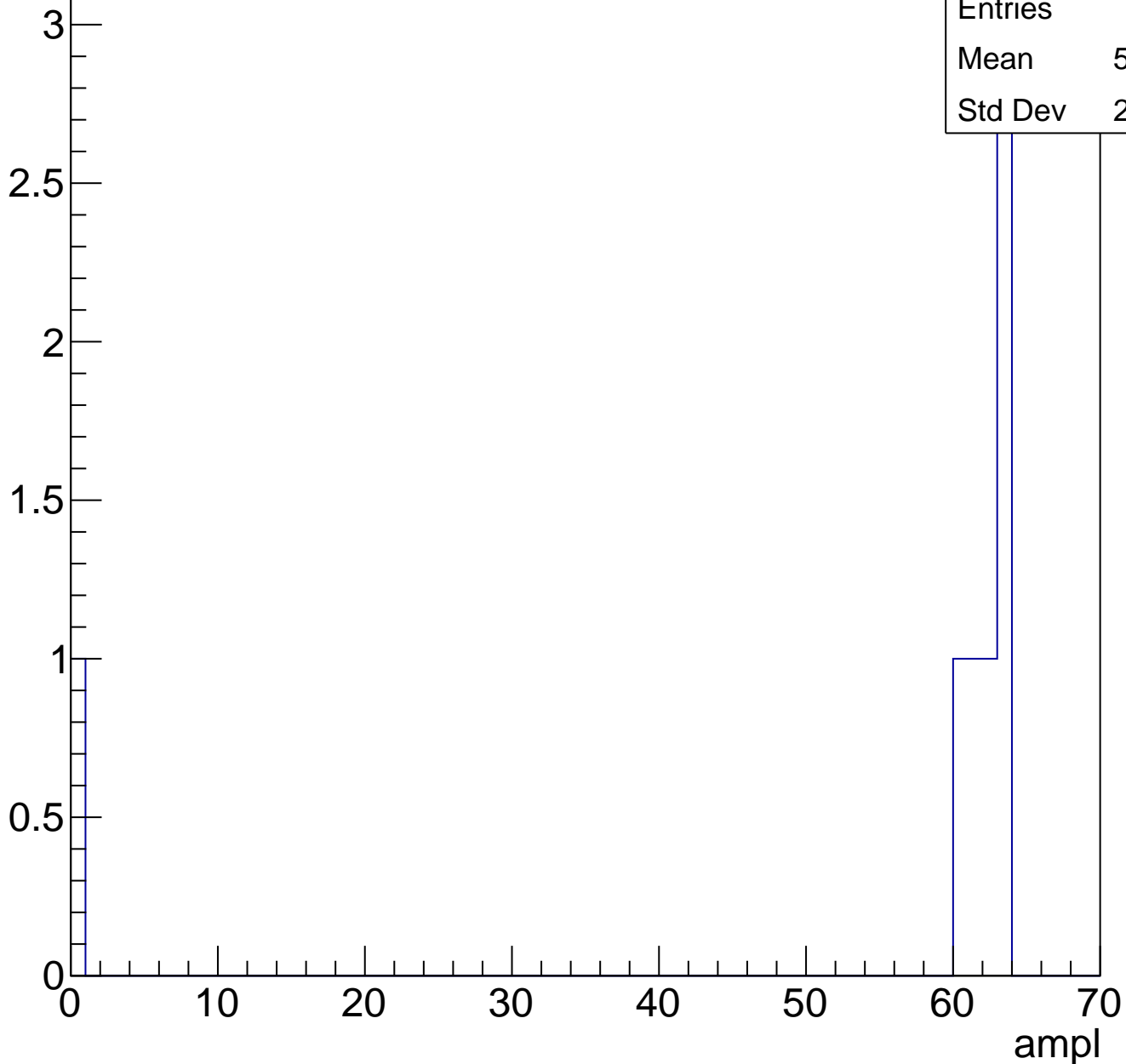
Entry



B1L103S, U23-ch15, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch15, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.105
Std Dev	4.689

Entry



B1L103S, U23-ch16, adc0

calib_packv5_041523_1651.root, FC#0, port C2

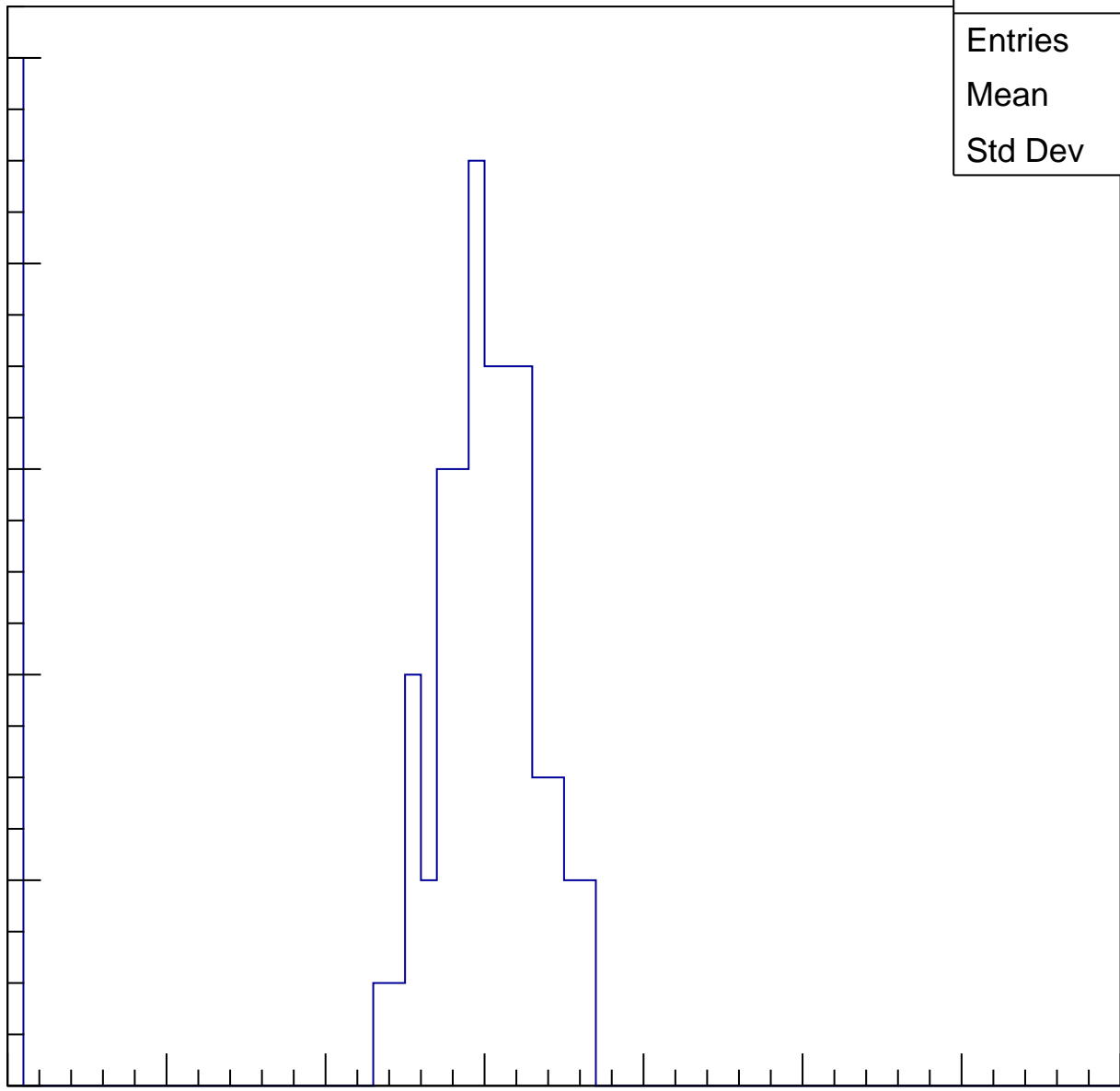
Entries	70
Mean	25.49
Std Dev	10.76

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

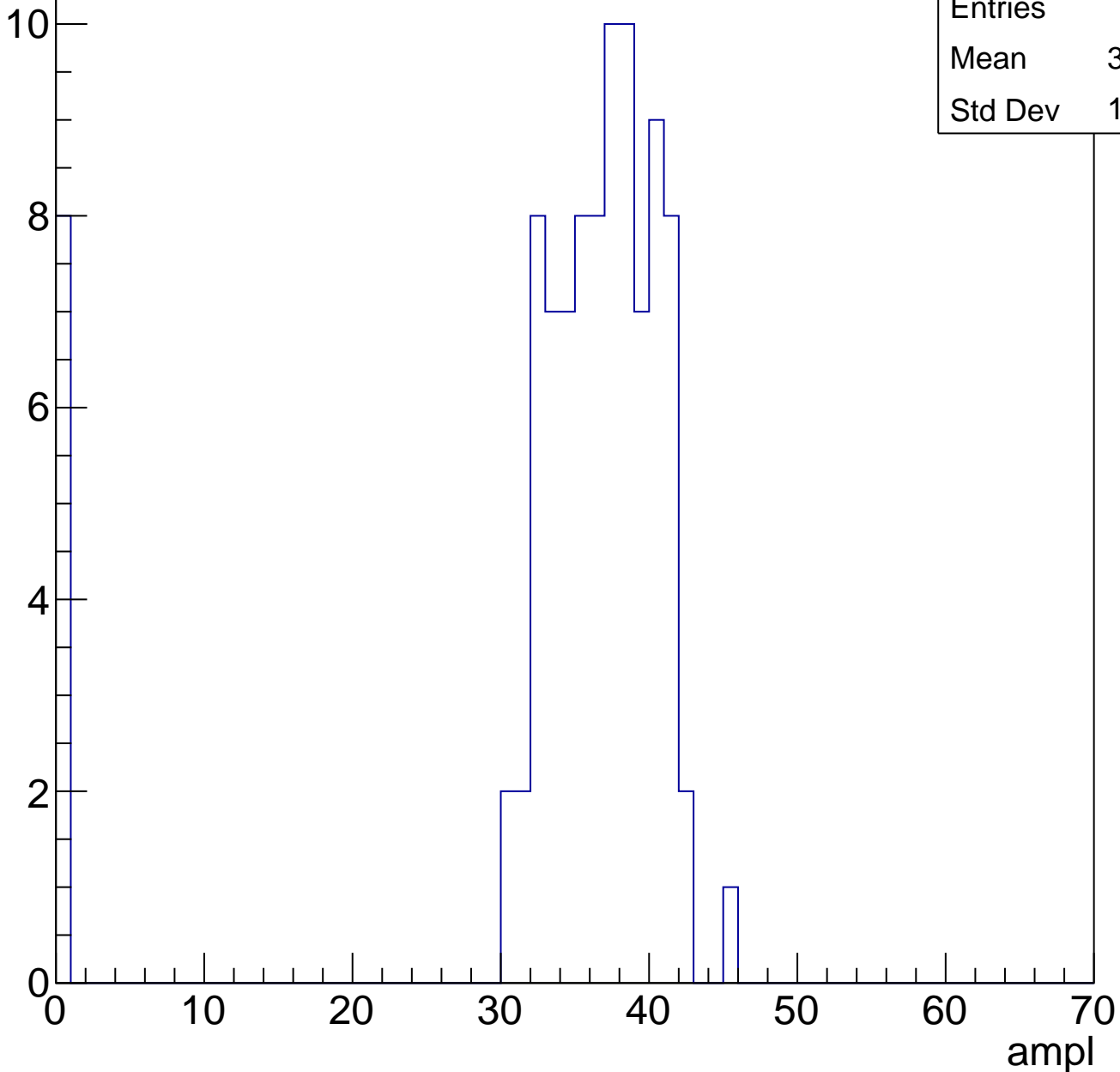


B1L103S, U23-ch16, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	97
Mean	33.56
Std Dev	10.53

Entry



B1L103S, U23-ch16, adc2

calib_packv5_041523_1651.root, FC#0, port C2

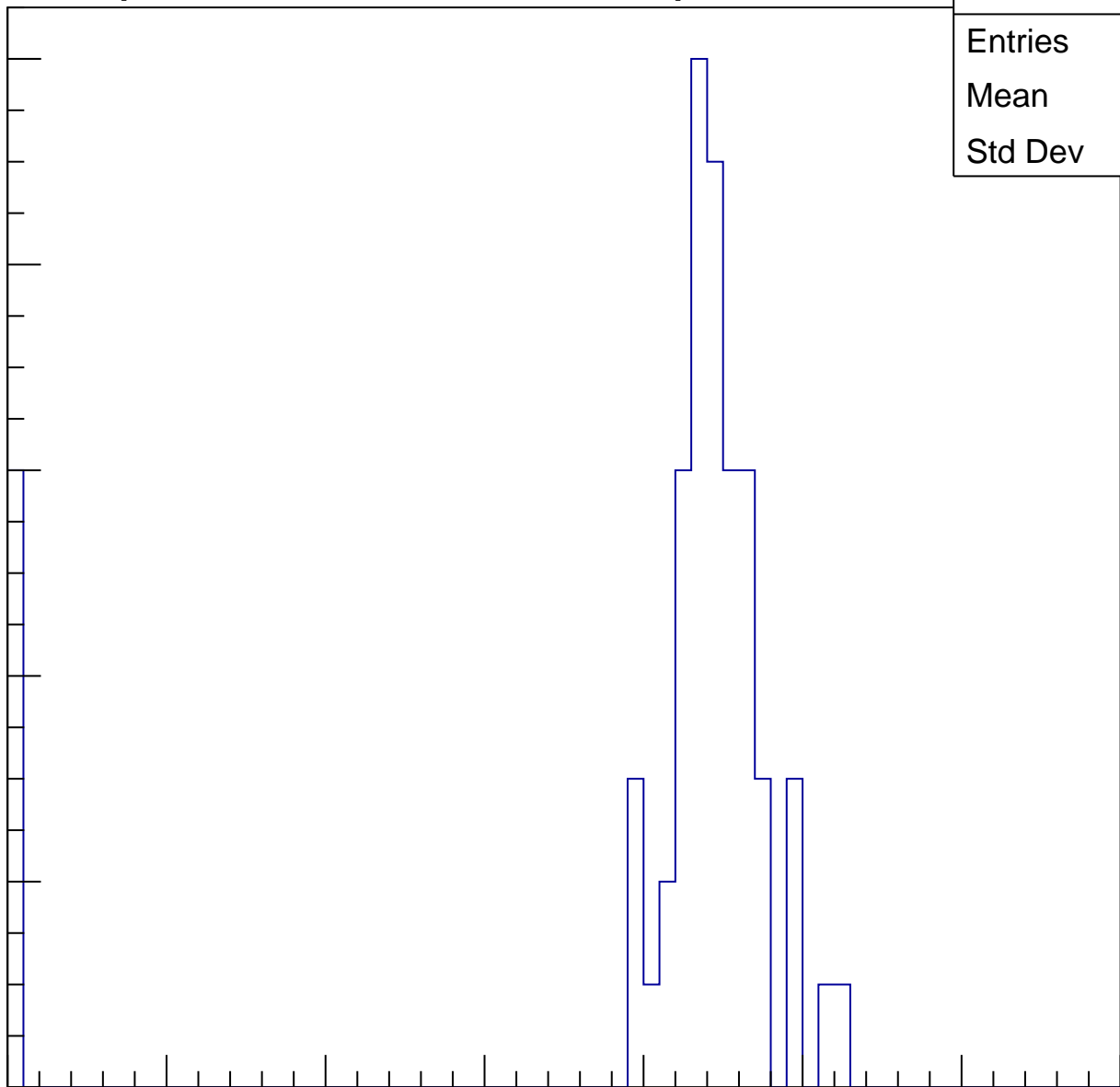
Entries	57
Mean	39.54
Std Dev	13.81

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

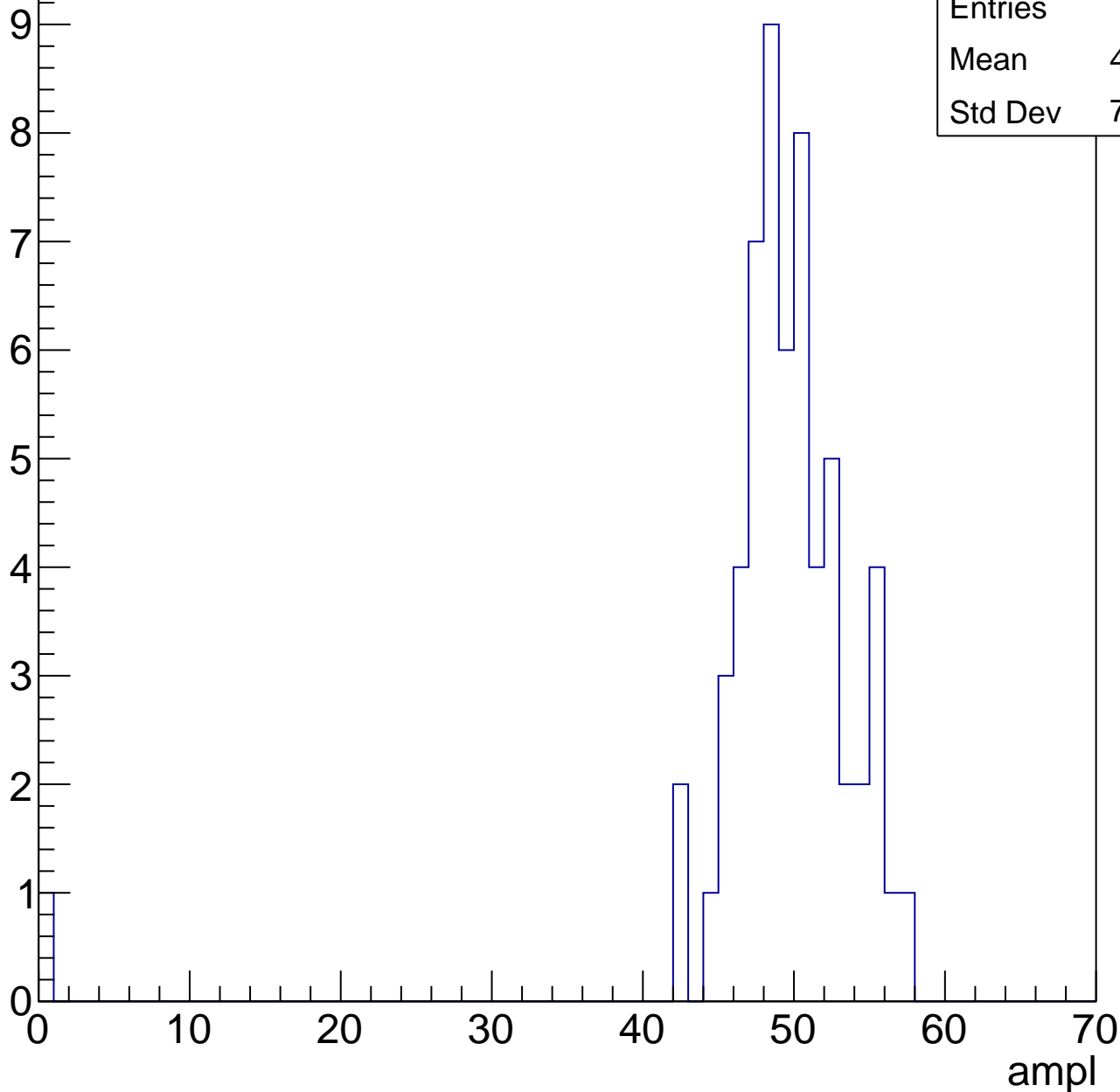


B1L103S, U23-ch16, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	48.55
Std Dev	7.119

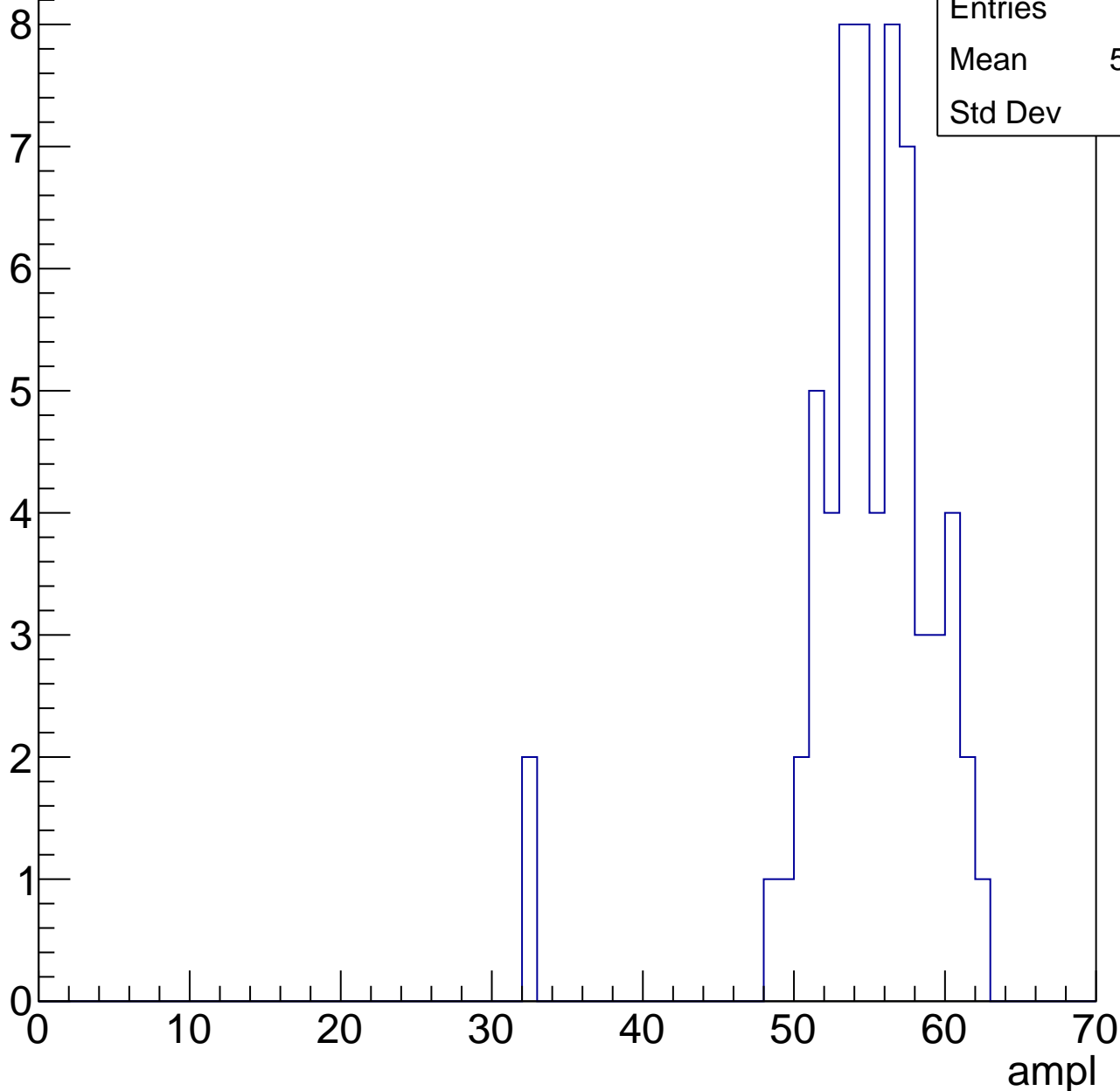


B1L103S, U23-ch16, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	63
Mean	54.32
Std Dev	5.12

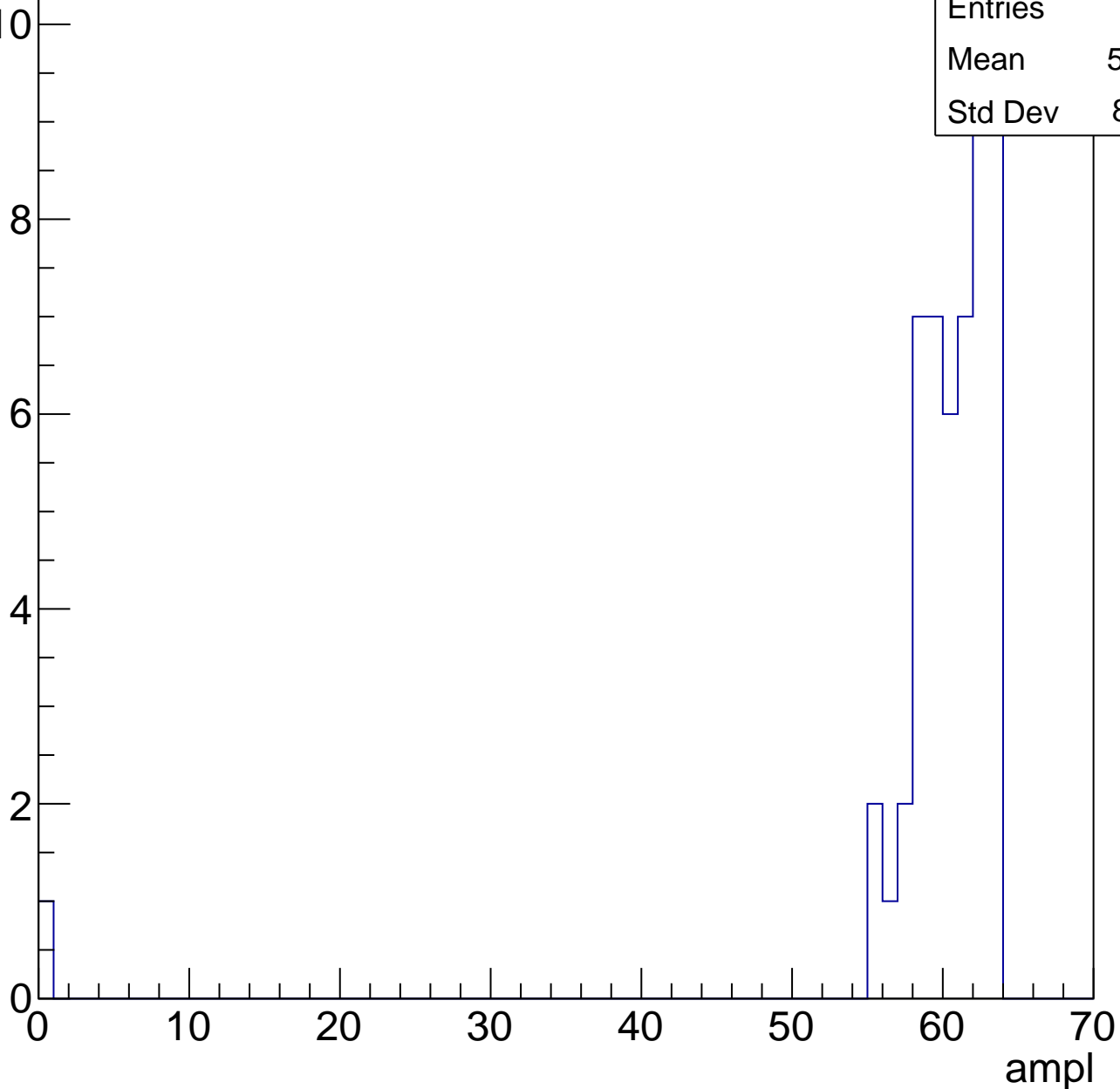


B1L103S, U23-ch16, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	52
Mean	59.12
Std Dev	8.561



B1L103S, U23-ch16, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch16, adc7

calib_packv5_041523_1651.root, FC#0, port C2

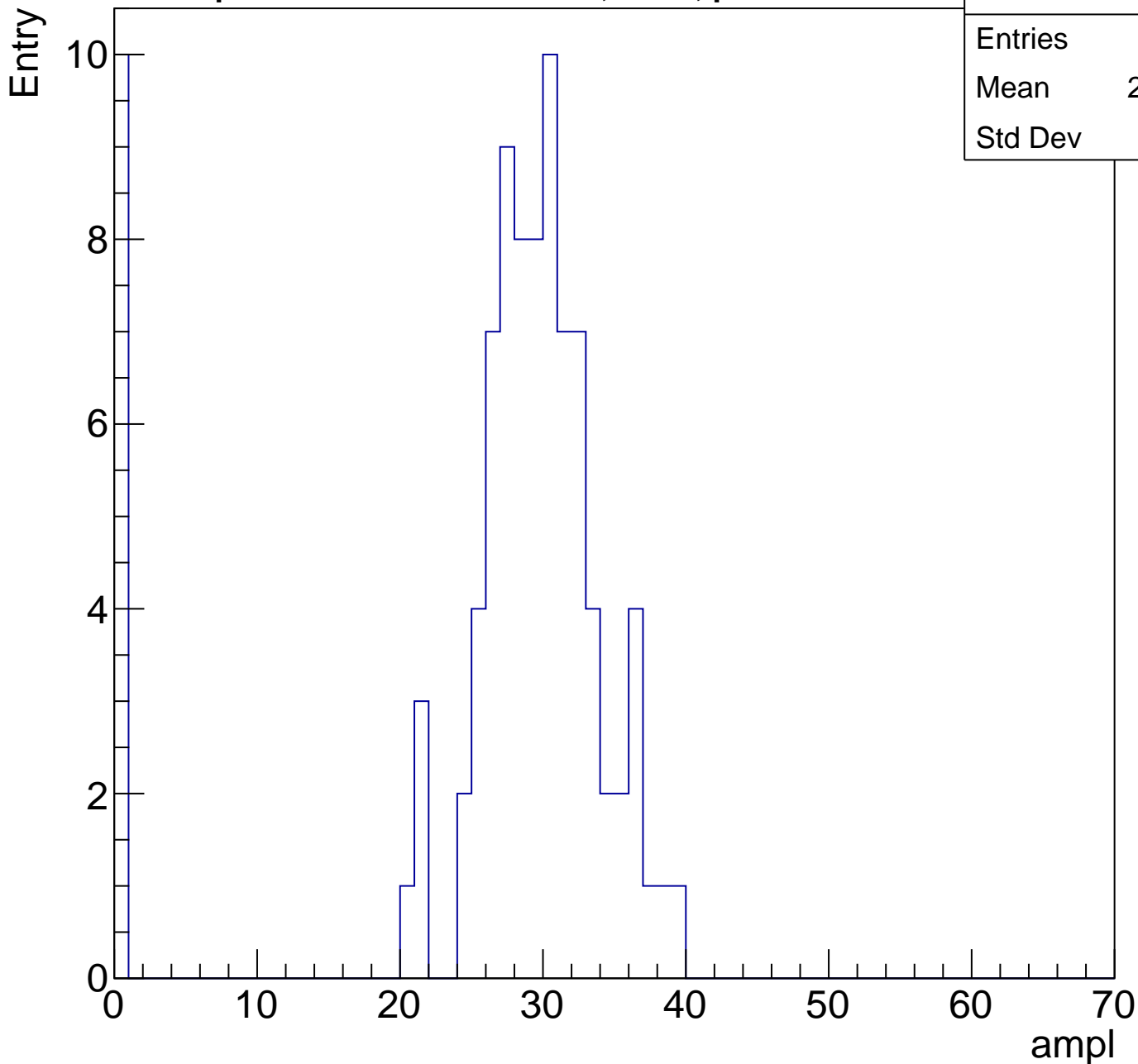
Entry



B1L103S, U23-ch17, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	91
Mean	26.16
Std Dev	9.89

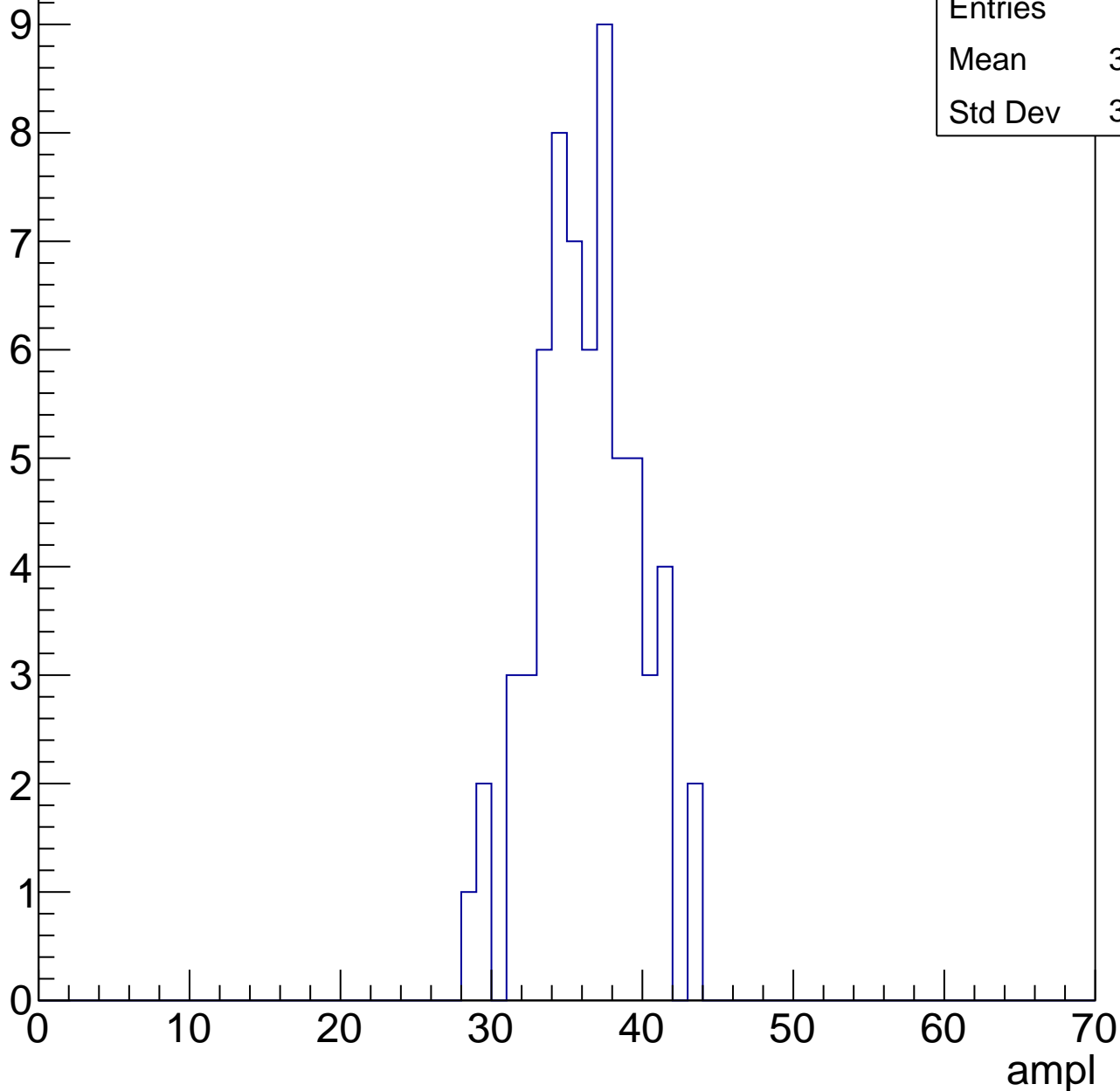


B1L103S, U23-ch17, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	35.84
Std Dev	3.299



B1L103S, U23-ch17, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	71
Mean	41.11
Std Dev	9.148

Entry

10

8

6

4

2

0

0

10

20

30

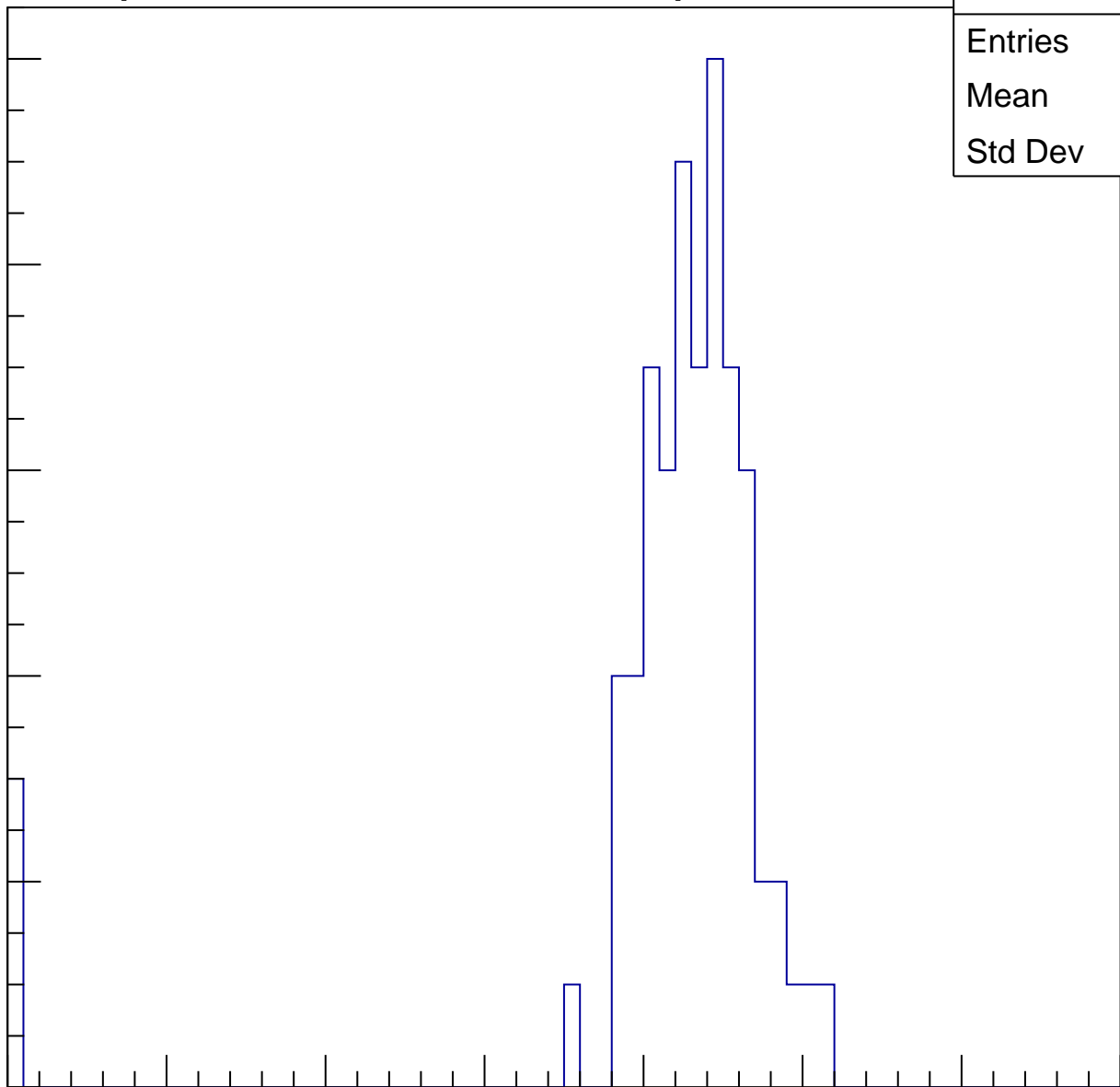
40

50

60

70

ampl



B1L103S, U23-ch17, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	70
Mean	41.76
Std Dev	18.25

Entry

10

8

6

4

2

0

0

10

20

30

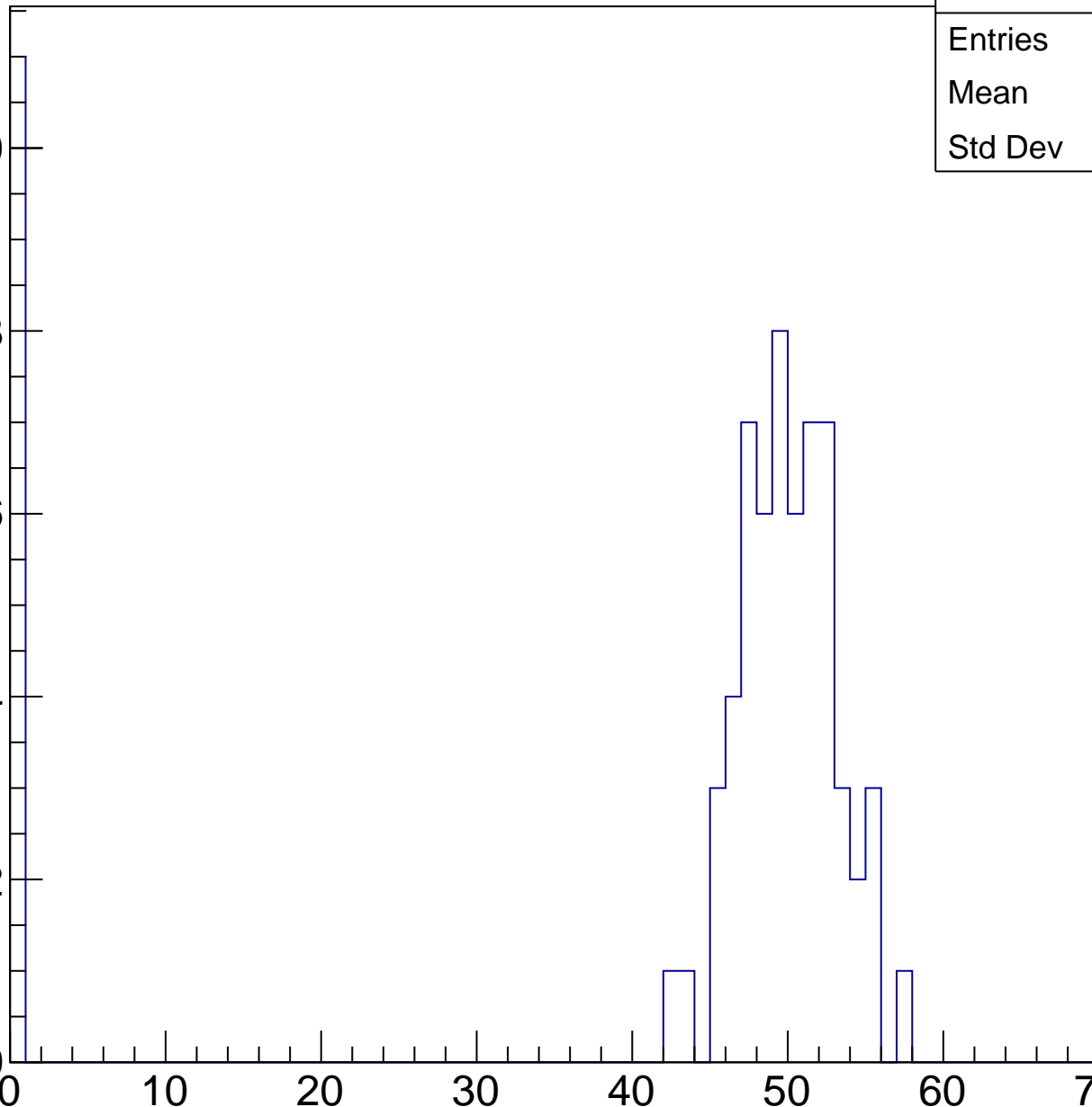
40

50

60

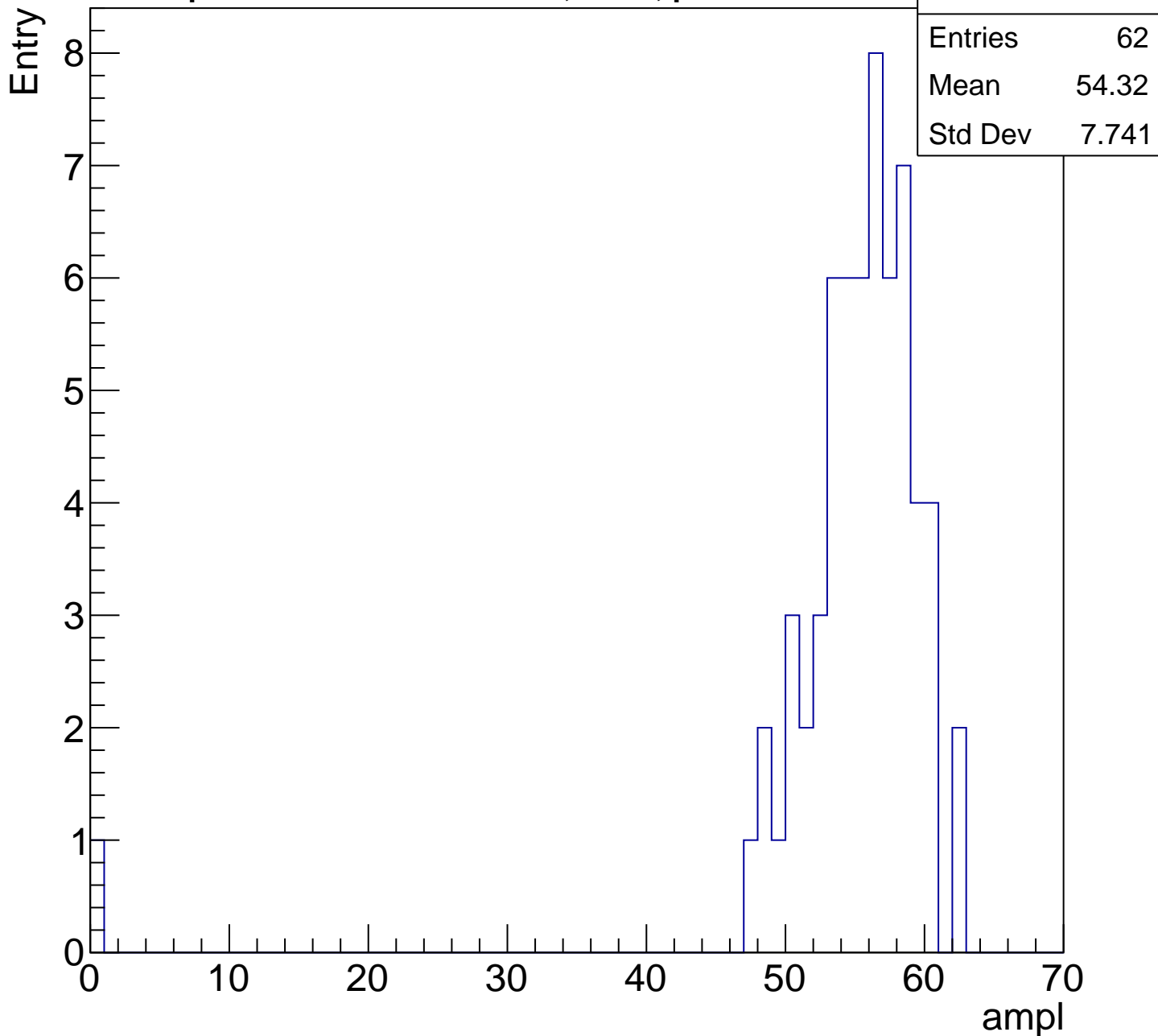
70

ampl



B1L103S, U23-ch17, adc4

calib_packv5_041523_1651.root, FC#0, port C2

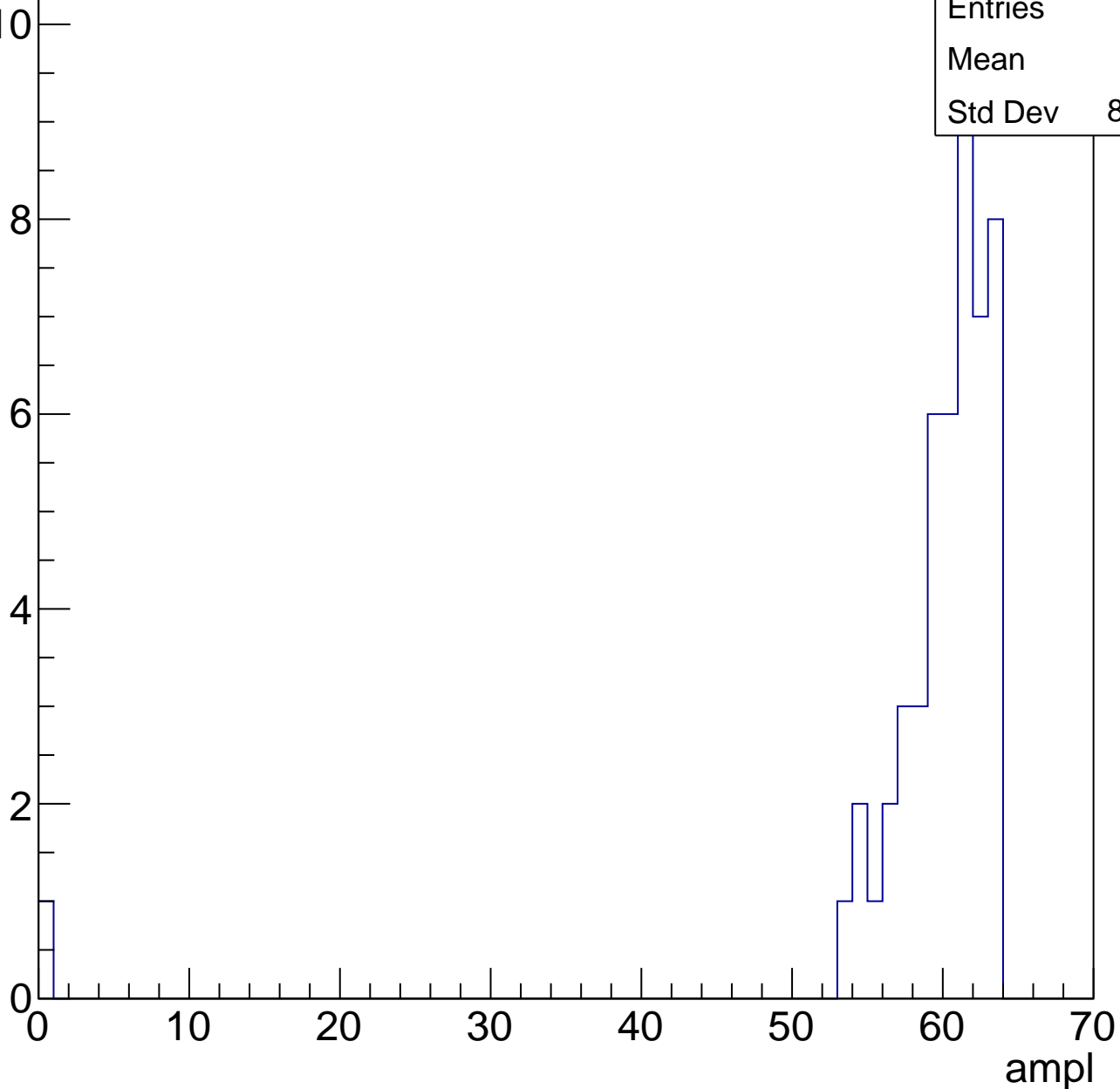


B1L103S, U23-ch17, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	50
Mean	58.7
Std Dev	8.773



B1L103S, U23-ch17, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch17, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.15
Std Dev	13.73

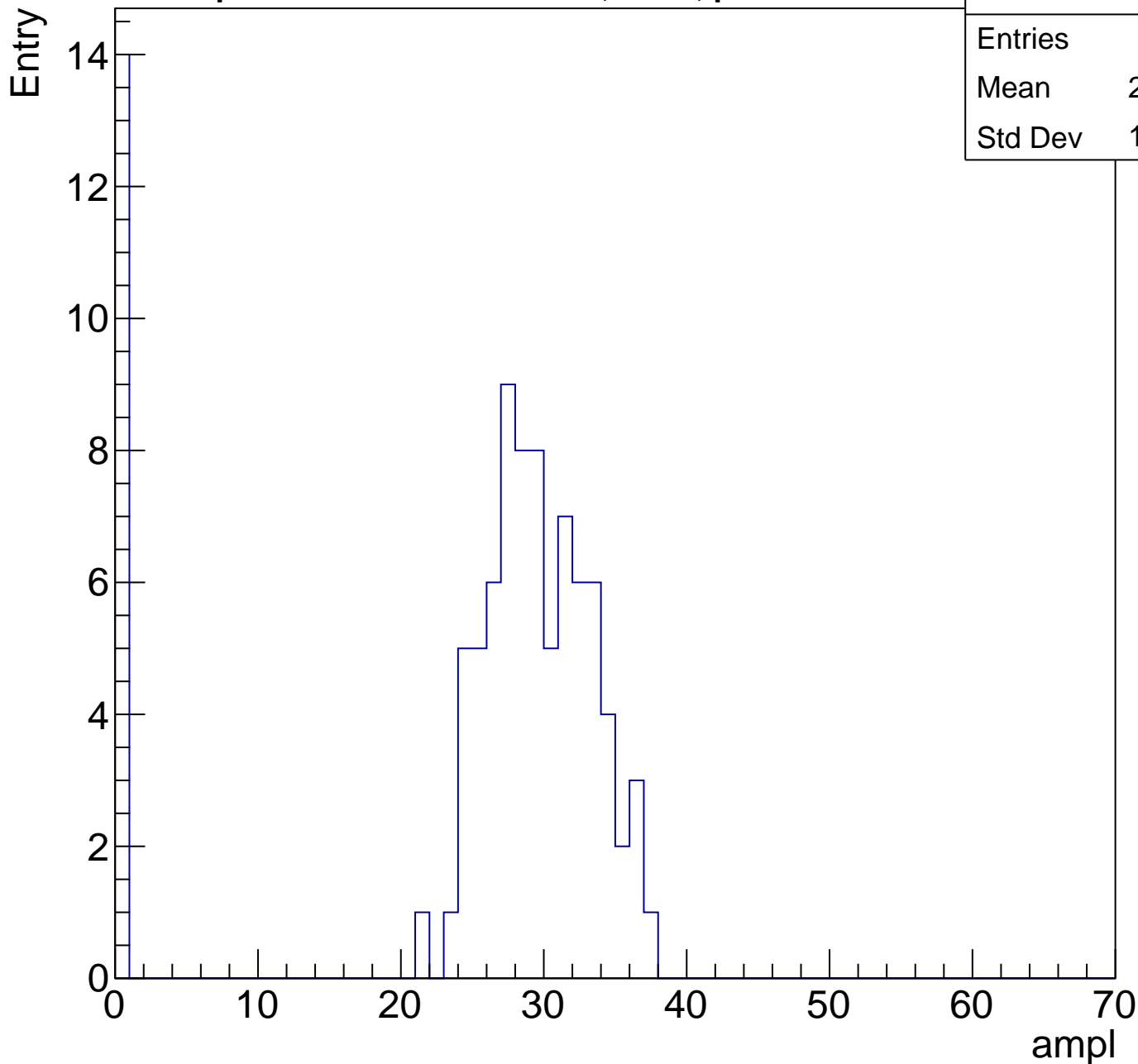
Entry



B1L103S, U23-ch18, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	91
Mean	24.75
Std Dev	11.04

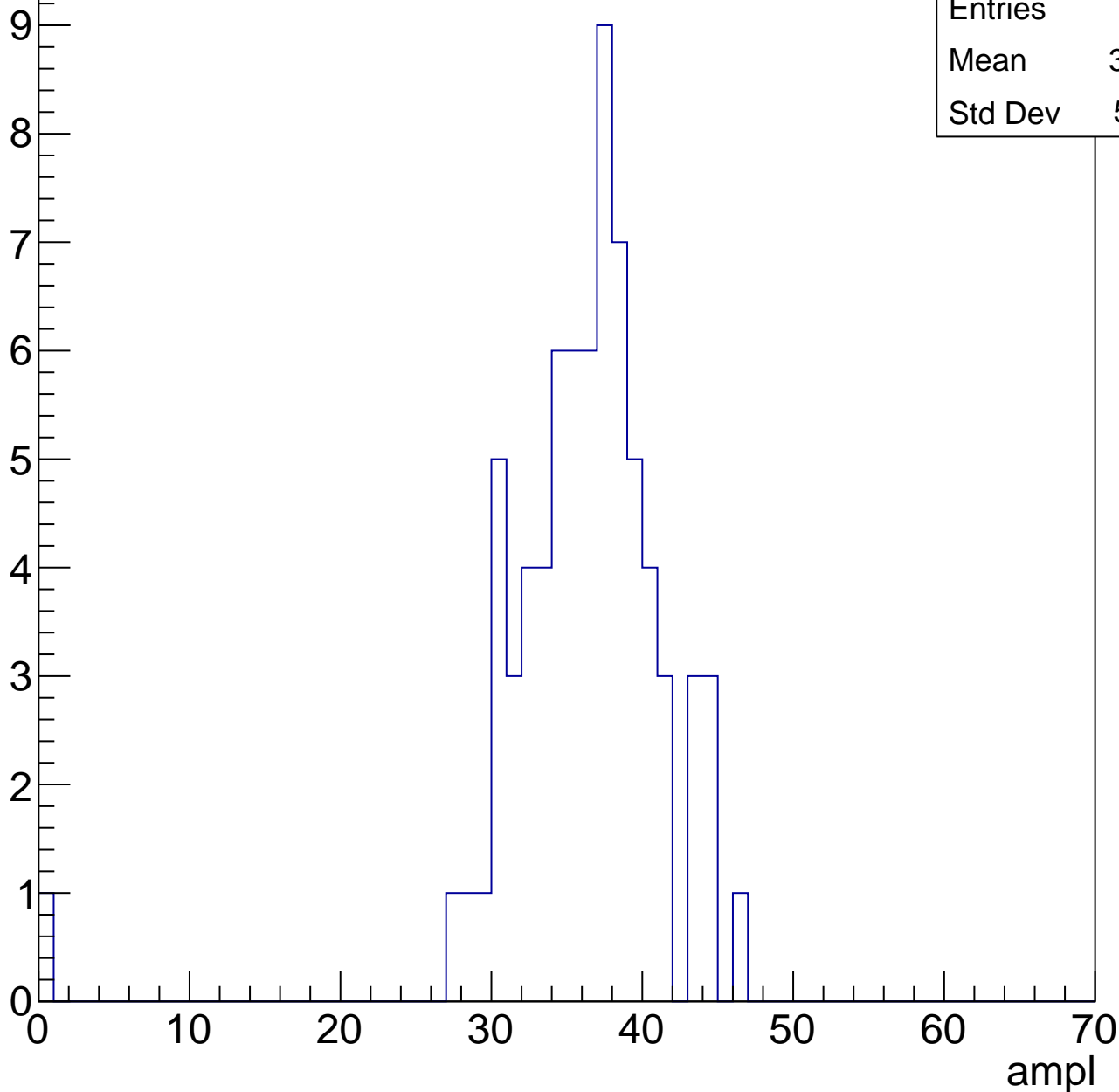


B1L103S, U23-ch18, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	73
Mean	35.63
Std Dev	5.881



B1L103S, U23-ch18, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	77
Mean	35.44
Std Dev	16.29

Entry

12

10

8

6

4

2

0

0

10

20

30

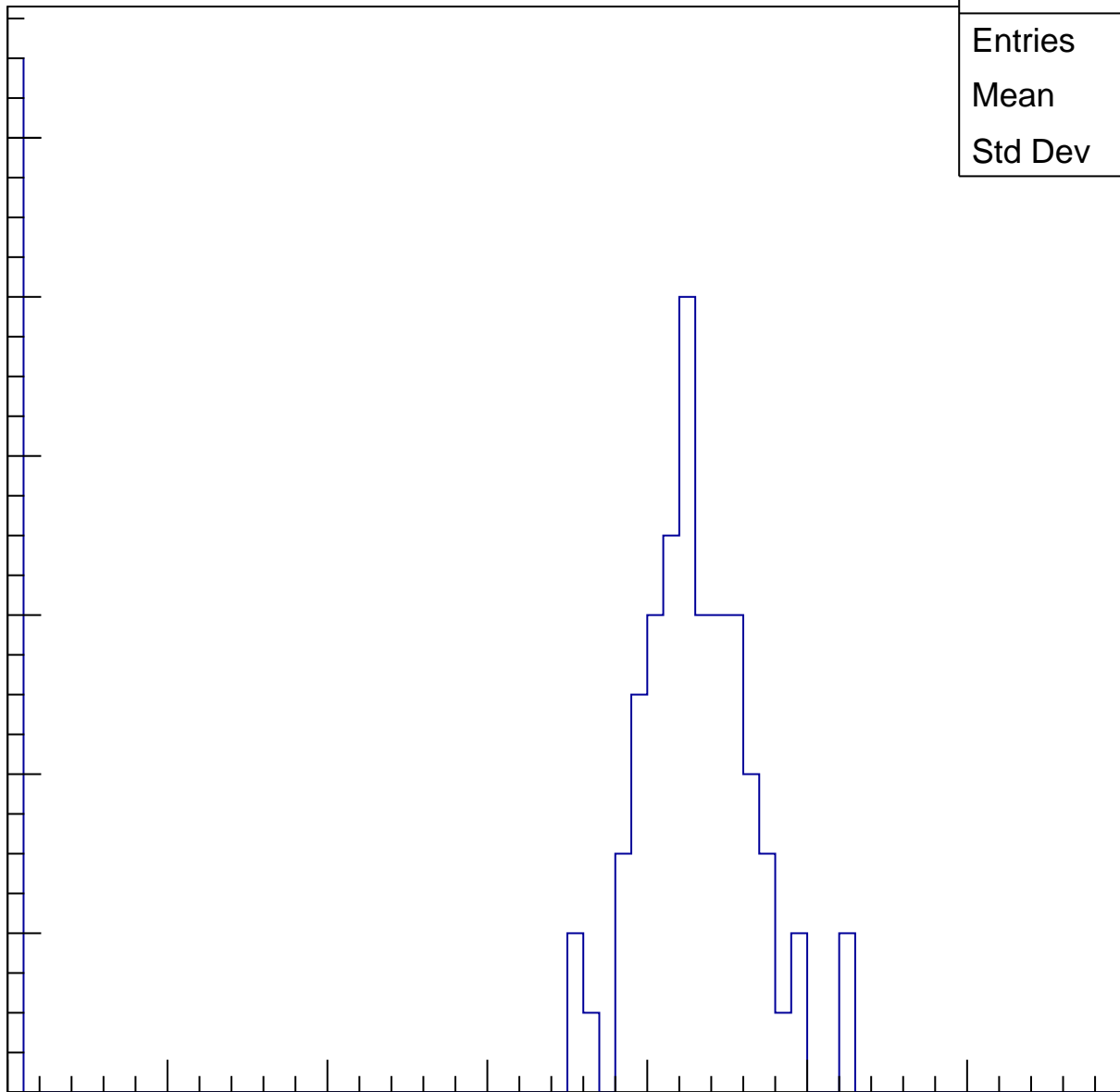
40

50

60

70

ampl

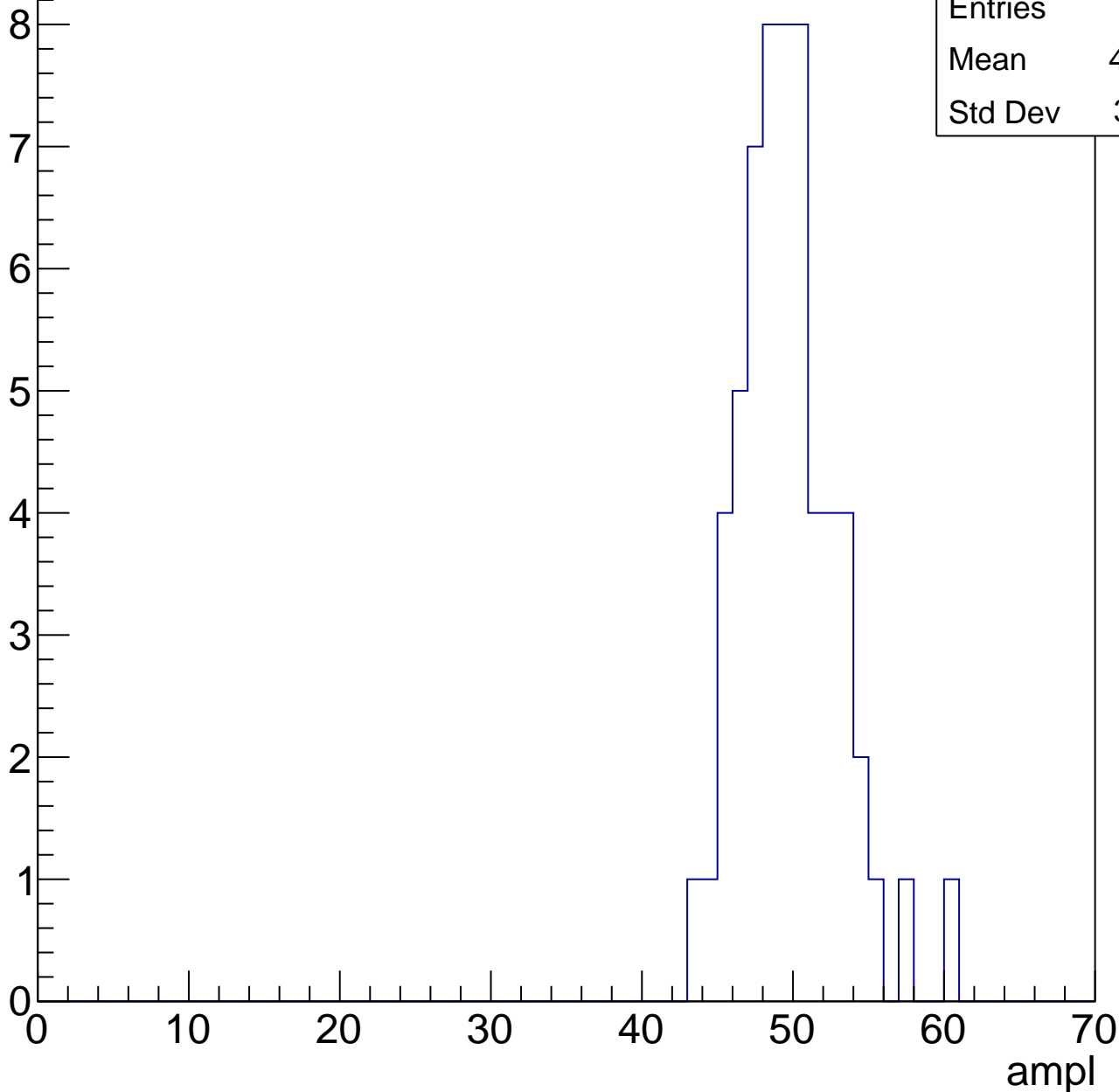


B1L103S, U23-ch18, adc3

calib_packv5_041523_1651.root, FC#0, port C2

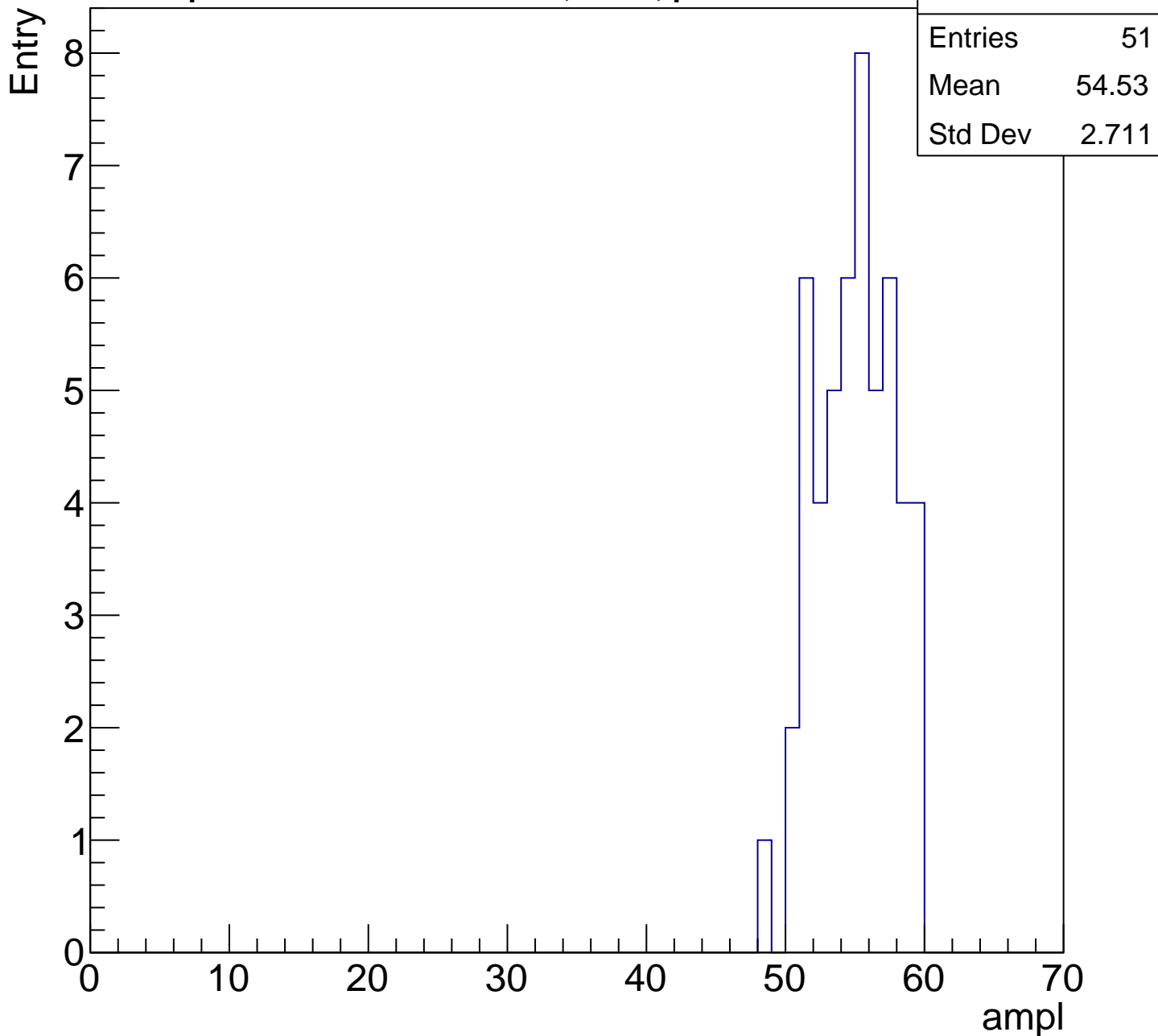
Entry

Entries	59
Mean	49.25
Std Dev	3.181



B1L103S, U23-ch18, adc4

calib_packv5_041523_1651.root, FC#0, port C2

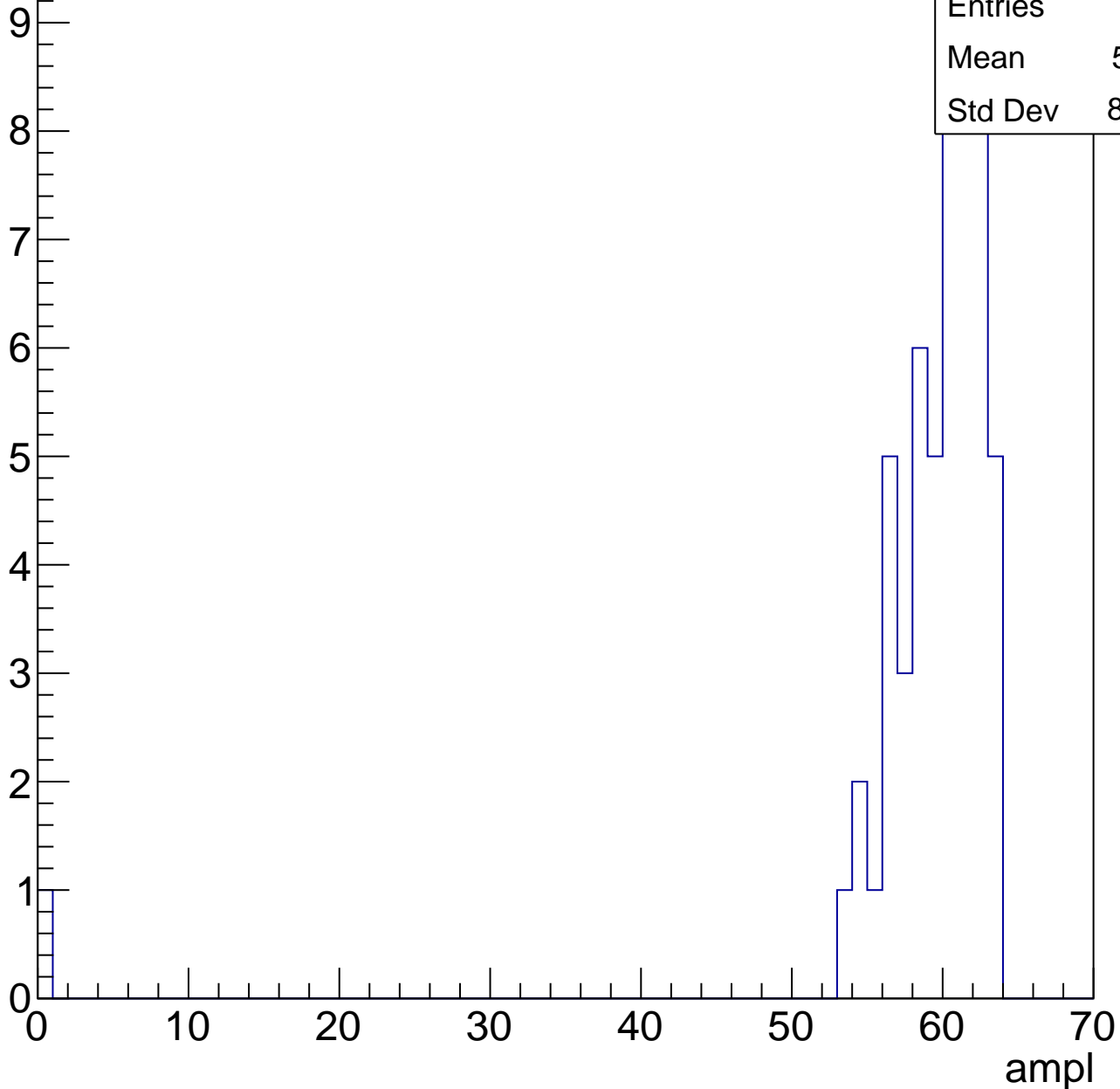


B1L103S, U23-ch18, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

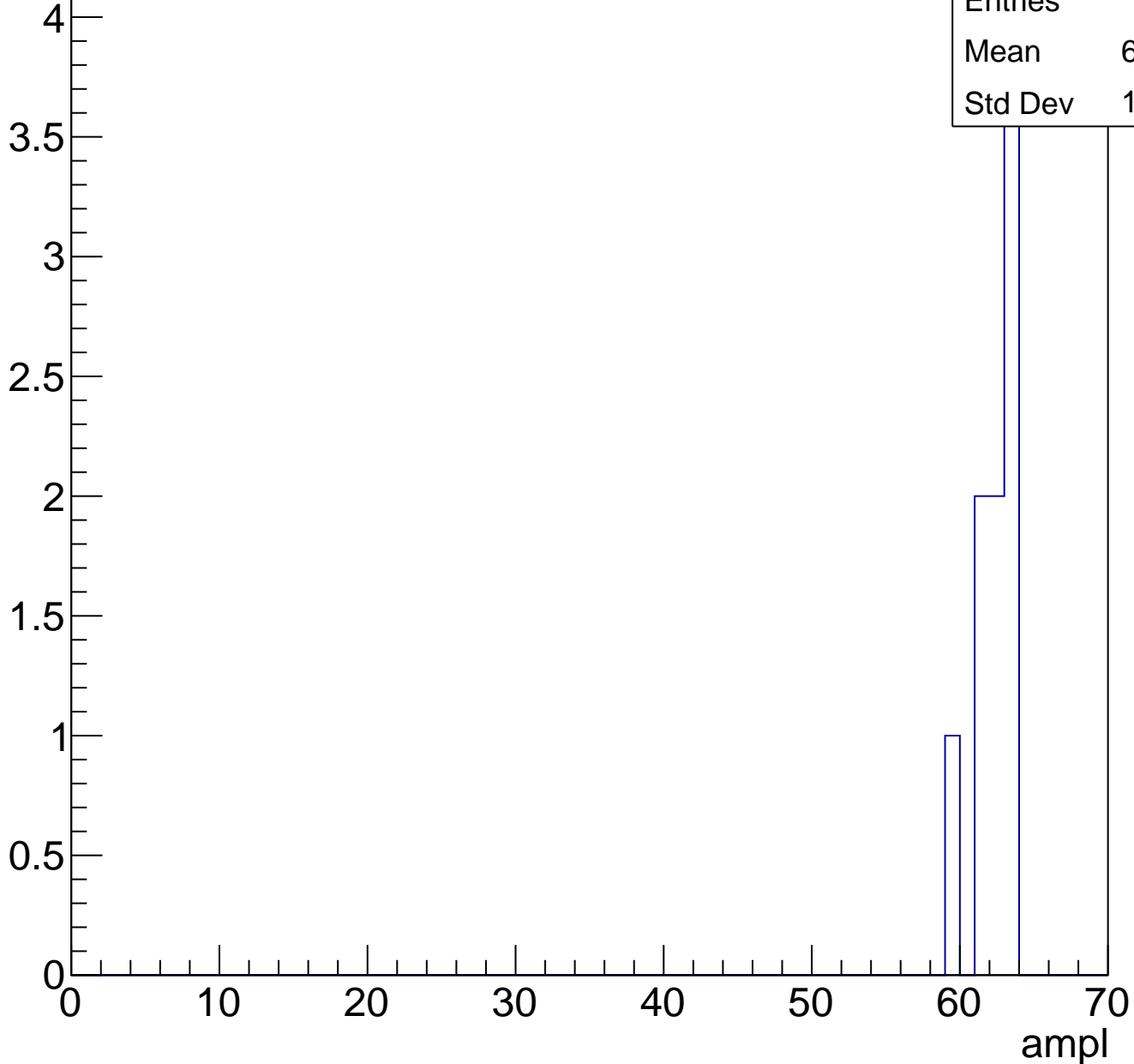
Entries	54
Mean	58.31
Std Dev	8.404



B1L103S, U23-ch18, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch18, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.15
Std Dev	13.73

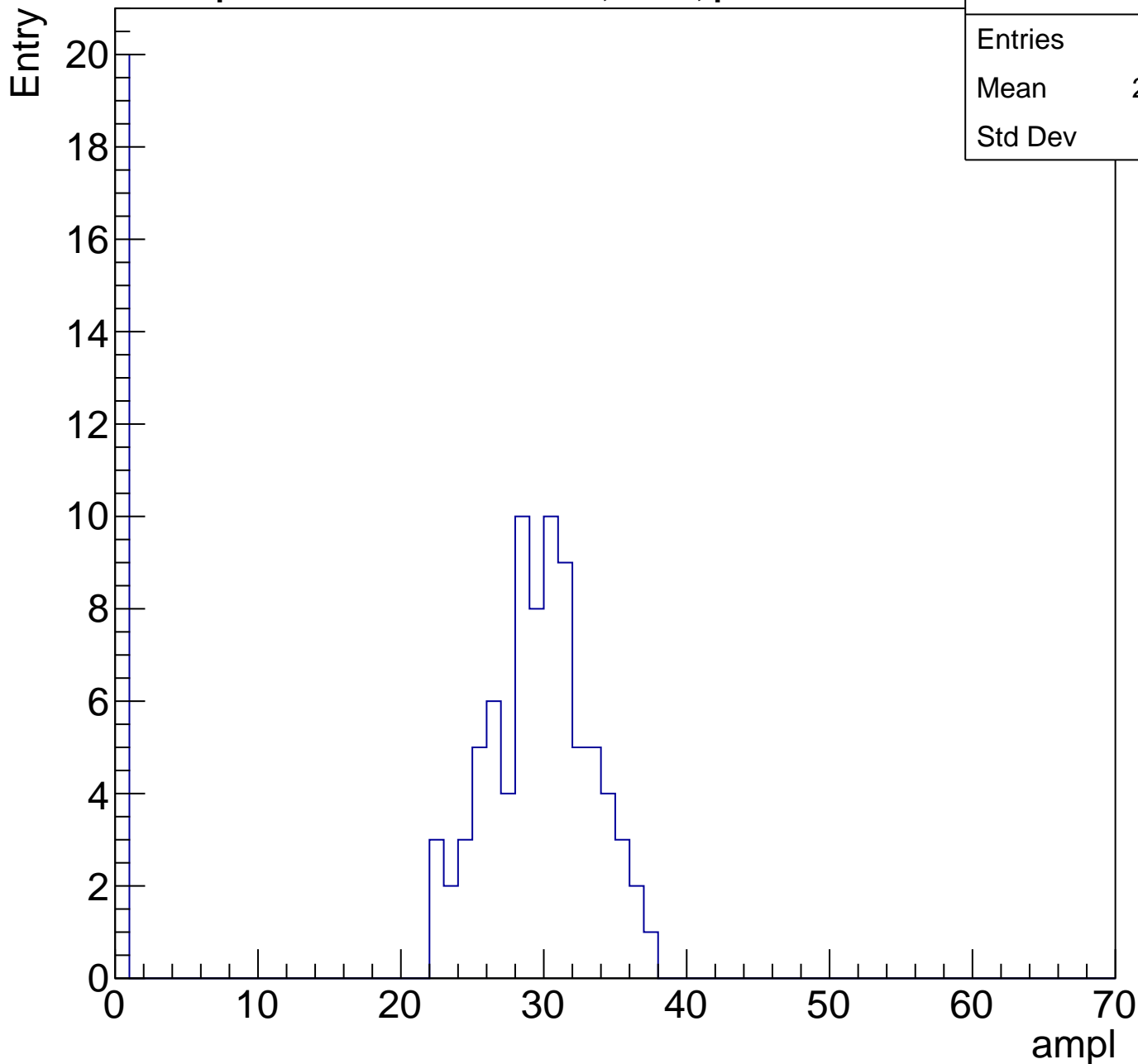
Entry



B1L103S, U23-ch19, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	100
Mean	23.39
Std Dev	12.11

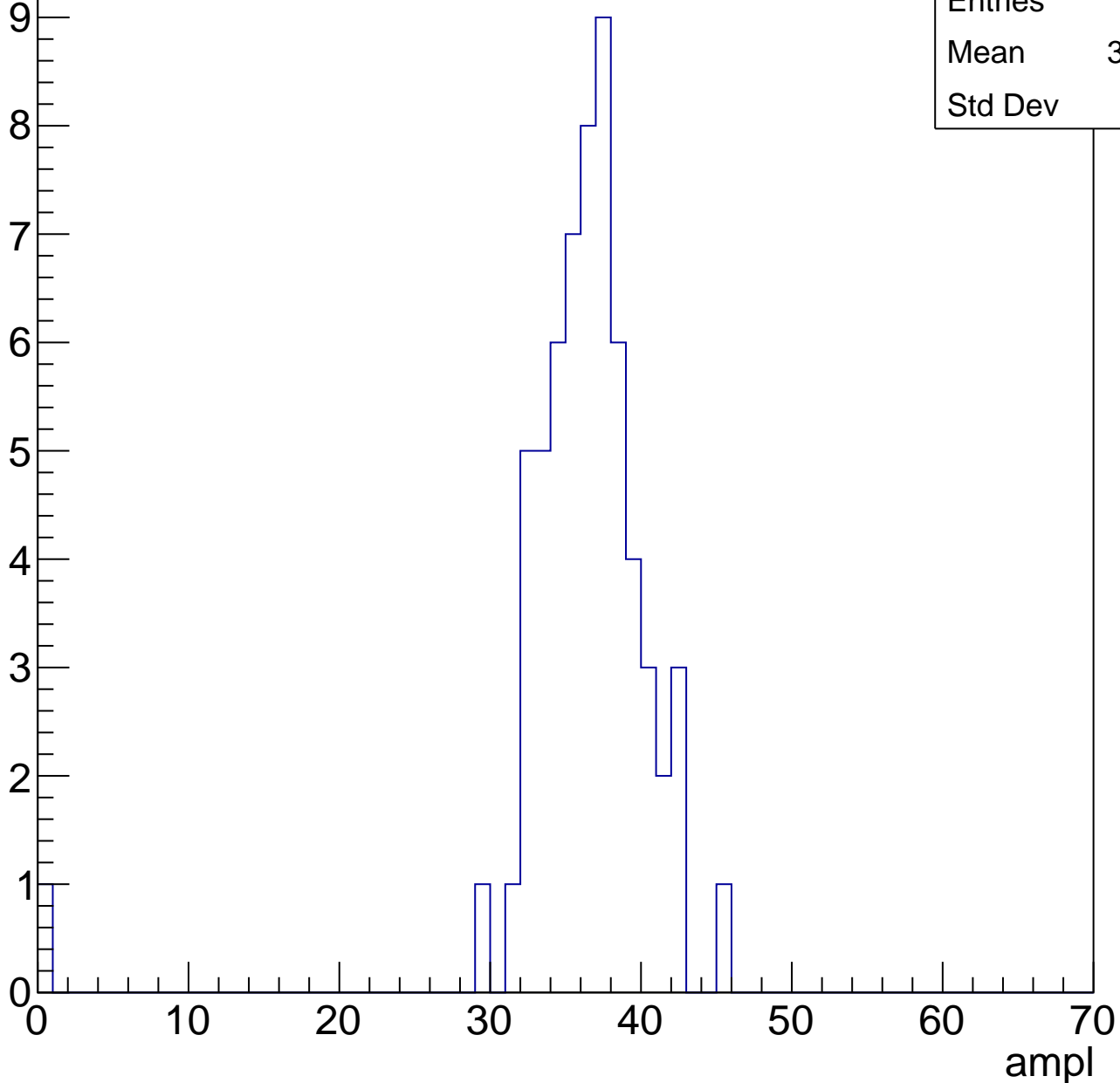


B1L103S, U23-ch19, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	35.68
Std Dev	5.5

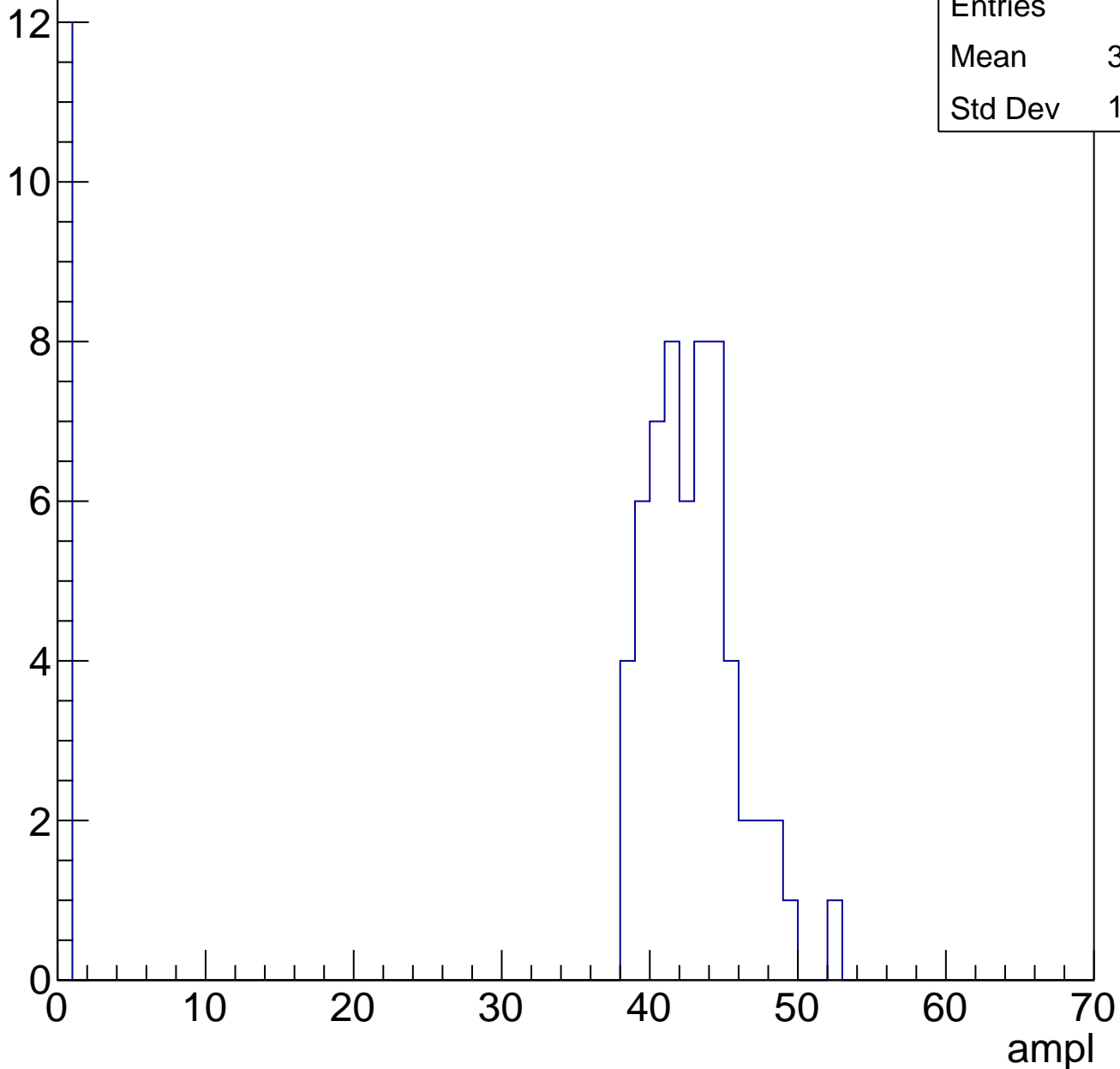


B1L103S, U23-ch19, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	71
Mean	35.28
Std Dev	16.14

Entry

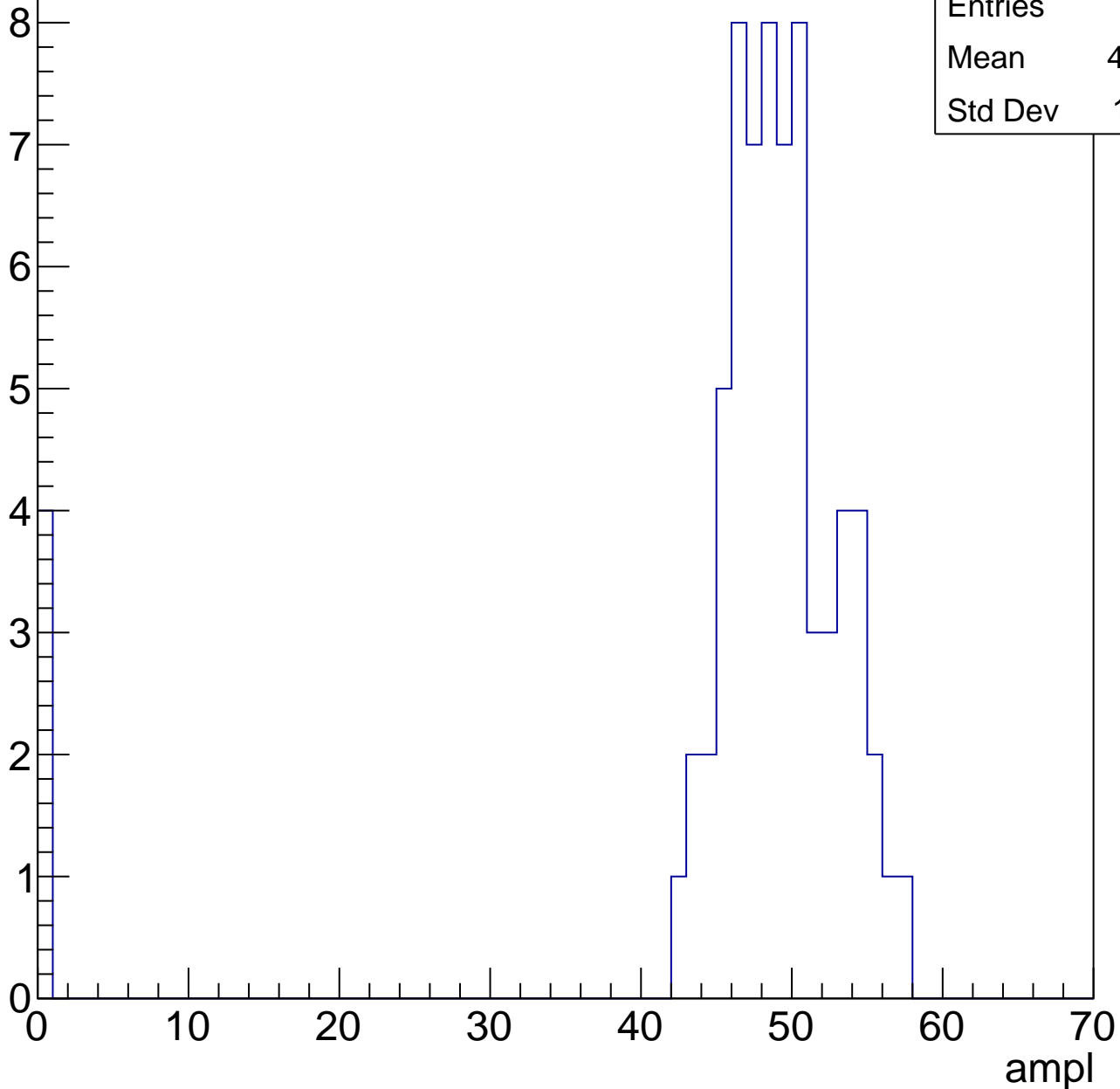


B1L103S, U23-ch19, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	46.07
Std Dev	11.81

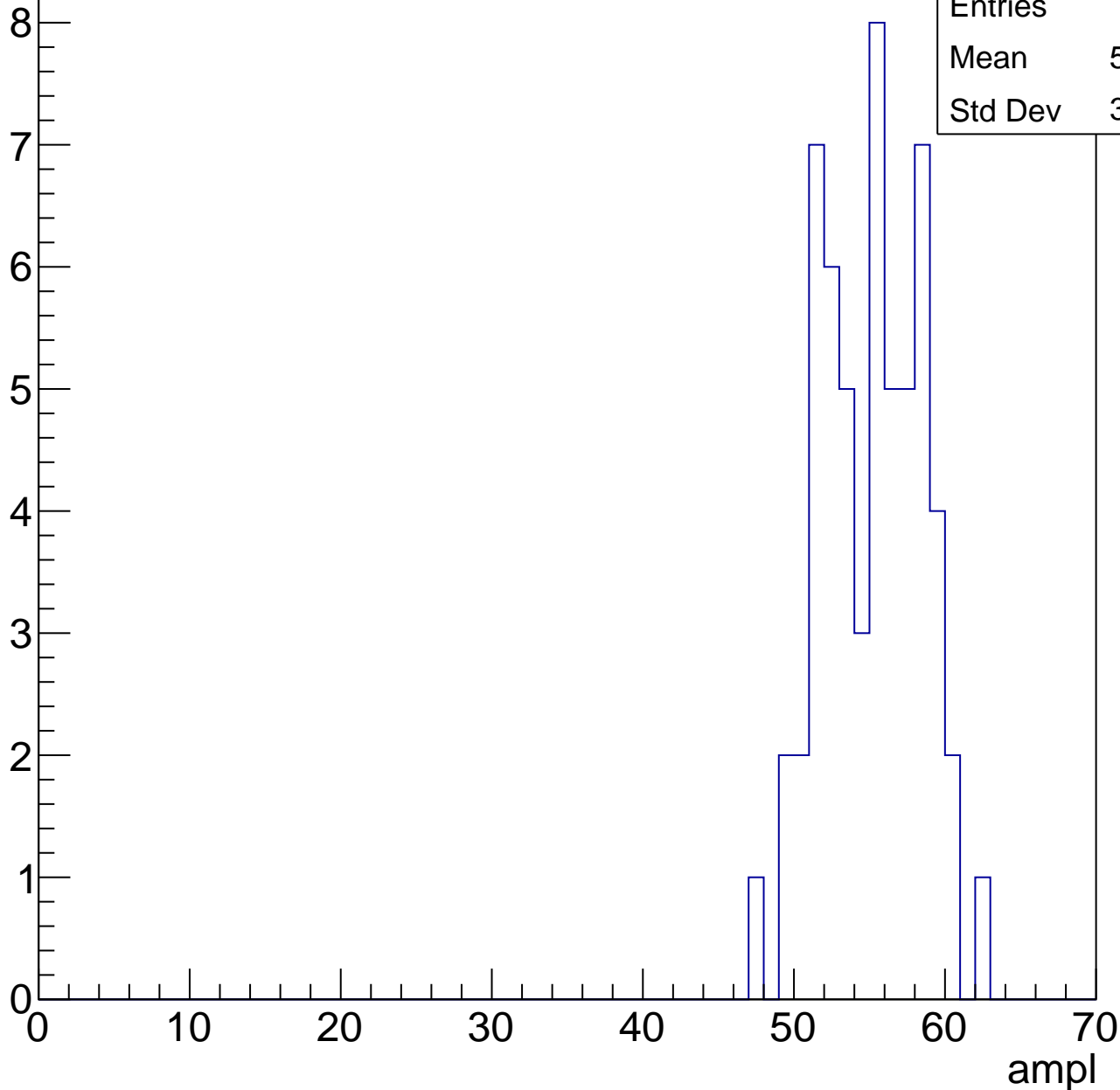


B1L103S, U23-ch19, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	54.66
Std Dev	3.267

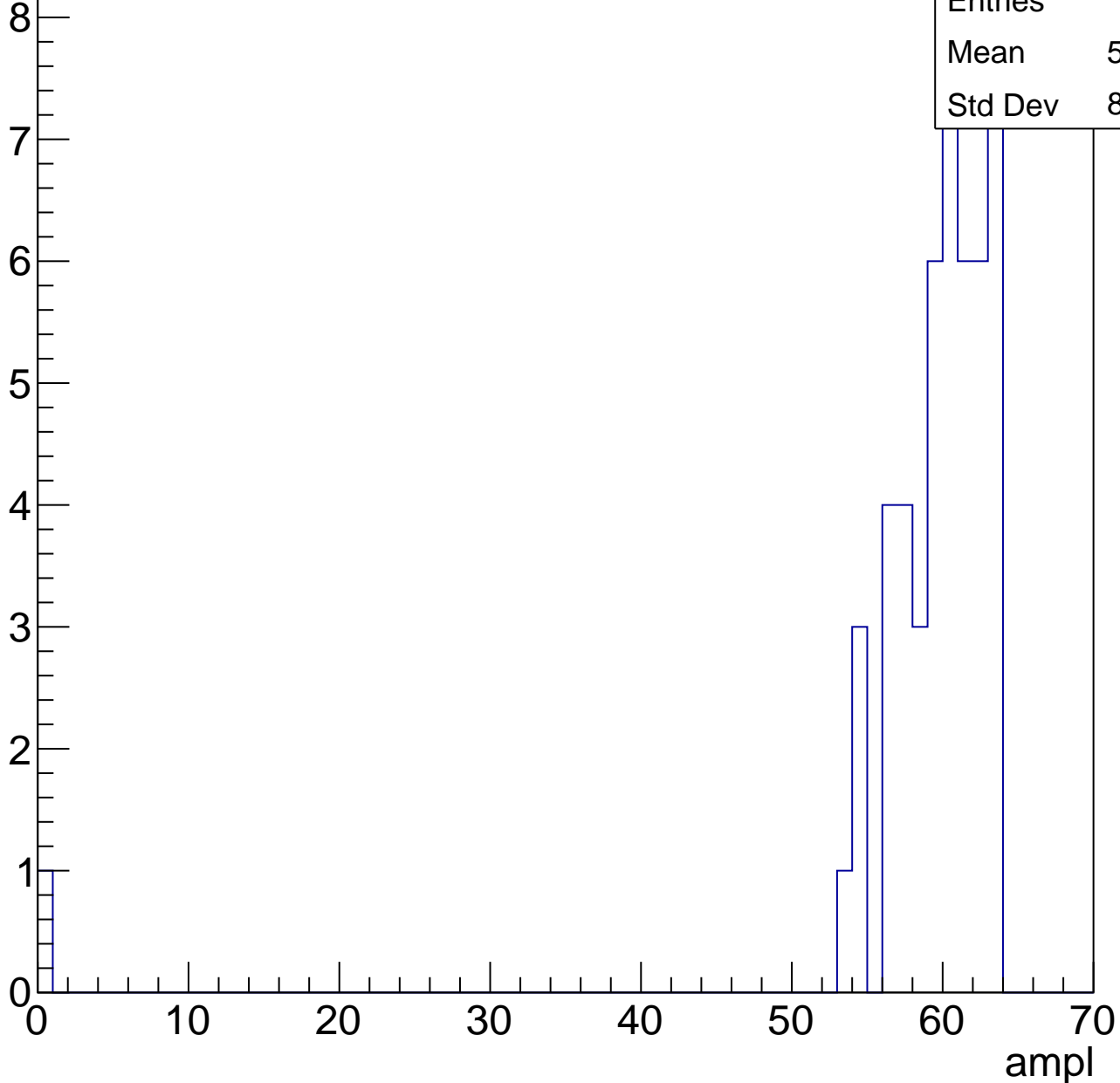


B1L103S, U23-ch19, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

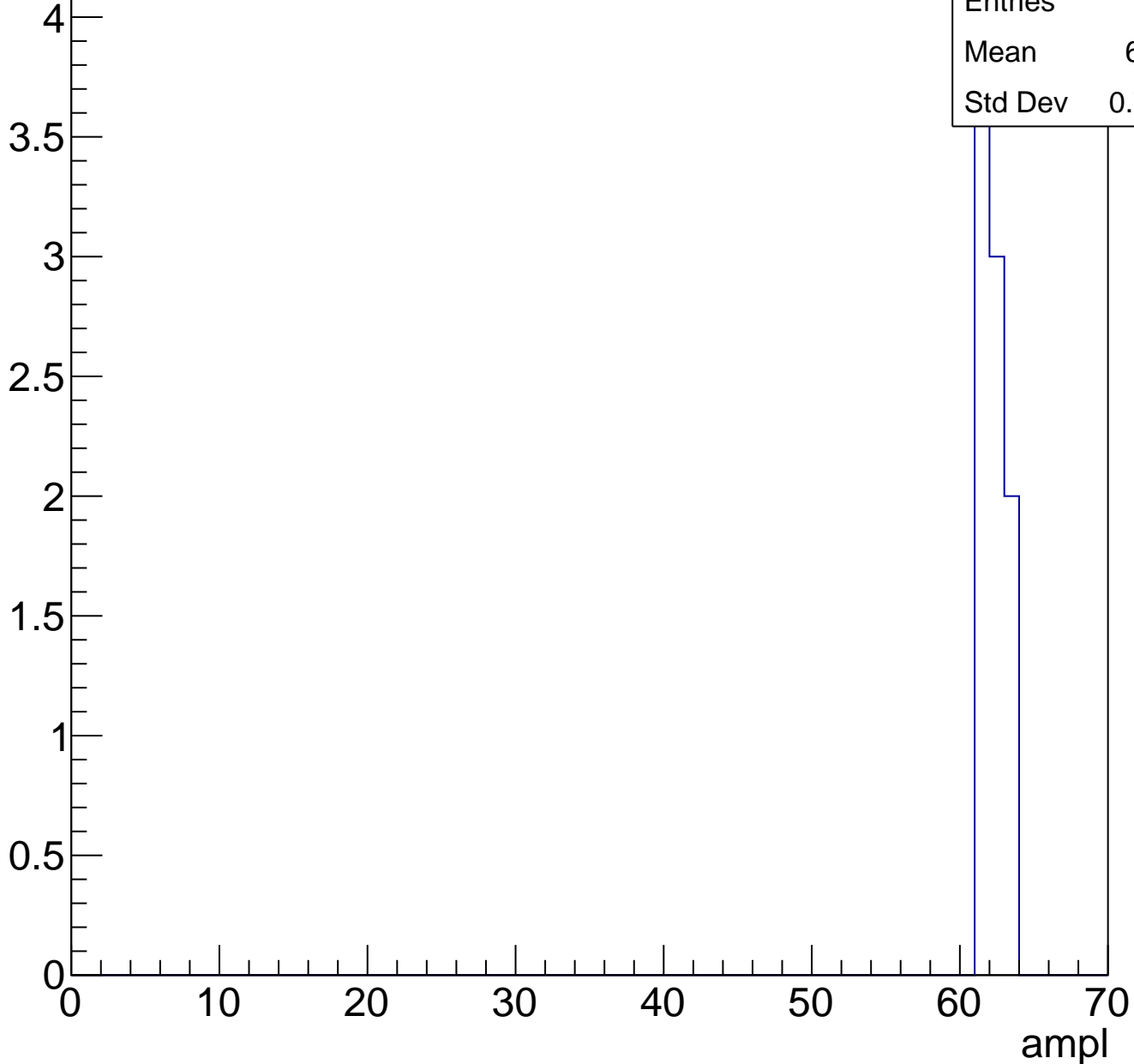
Entries	50
Mean	58.34
Std Dev	8.763



B1L103S, U23-ch19, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

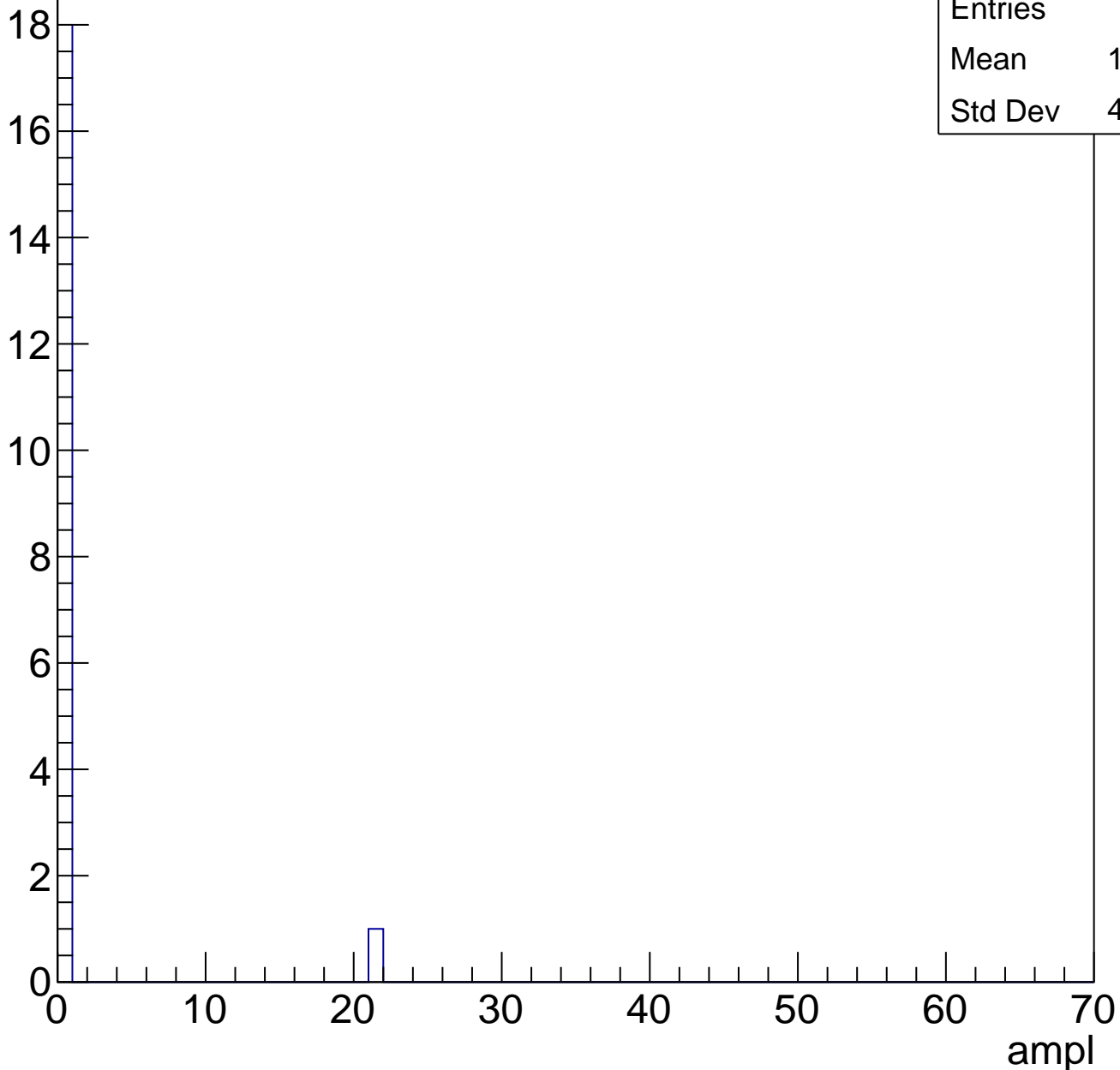


B1L103S, U23-ch19, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.105
Std Dev	4.689

Entry

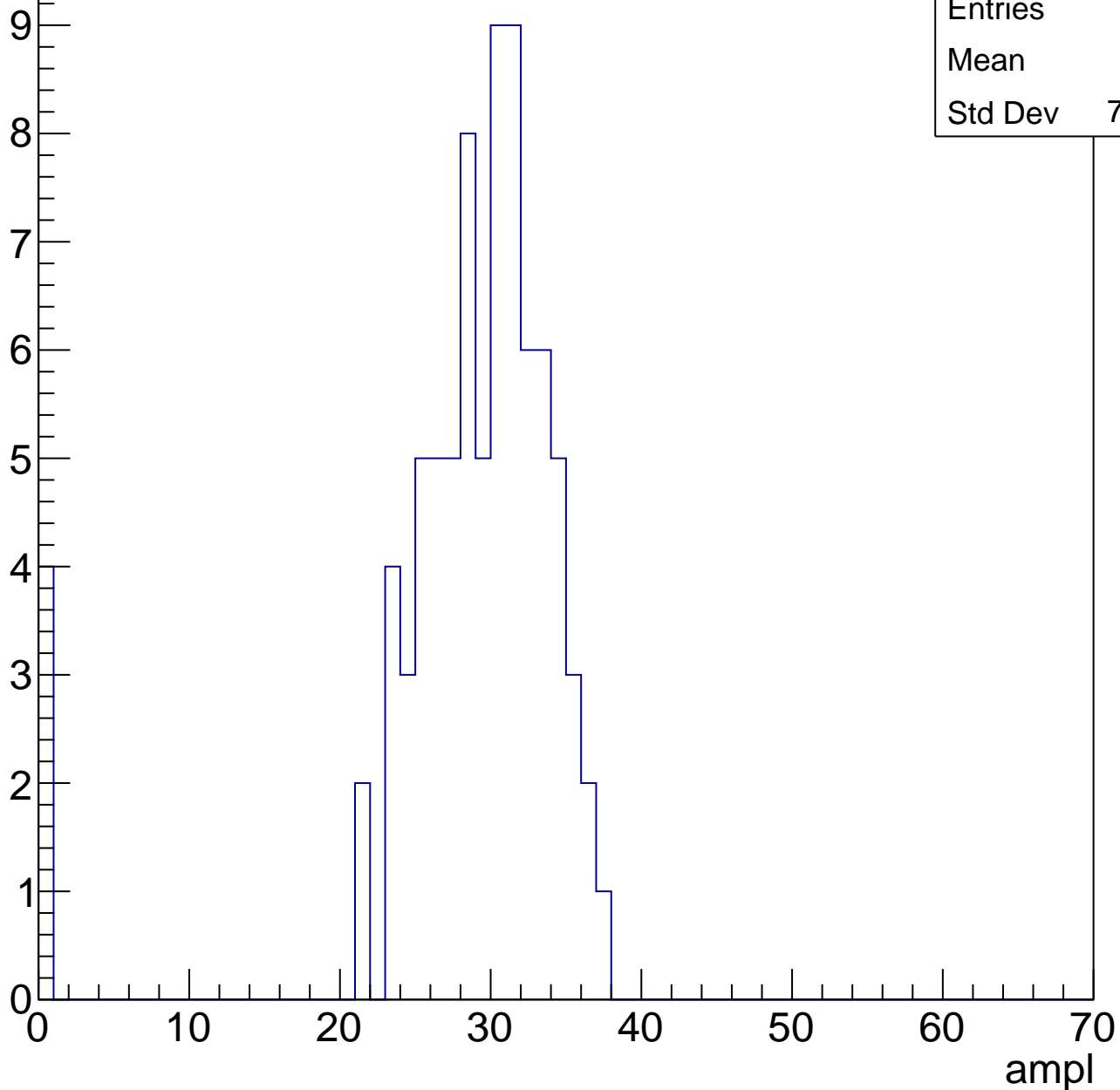


B1L103S, U23-ch20, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	82
Mean	27.9
Std Dev	7.288

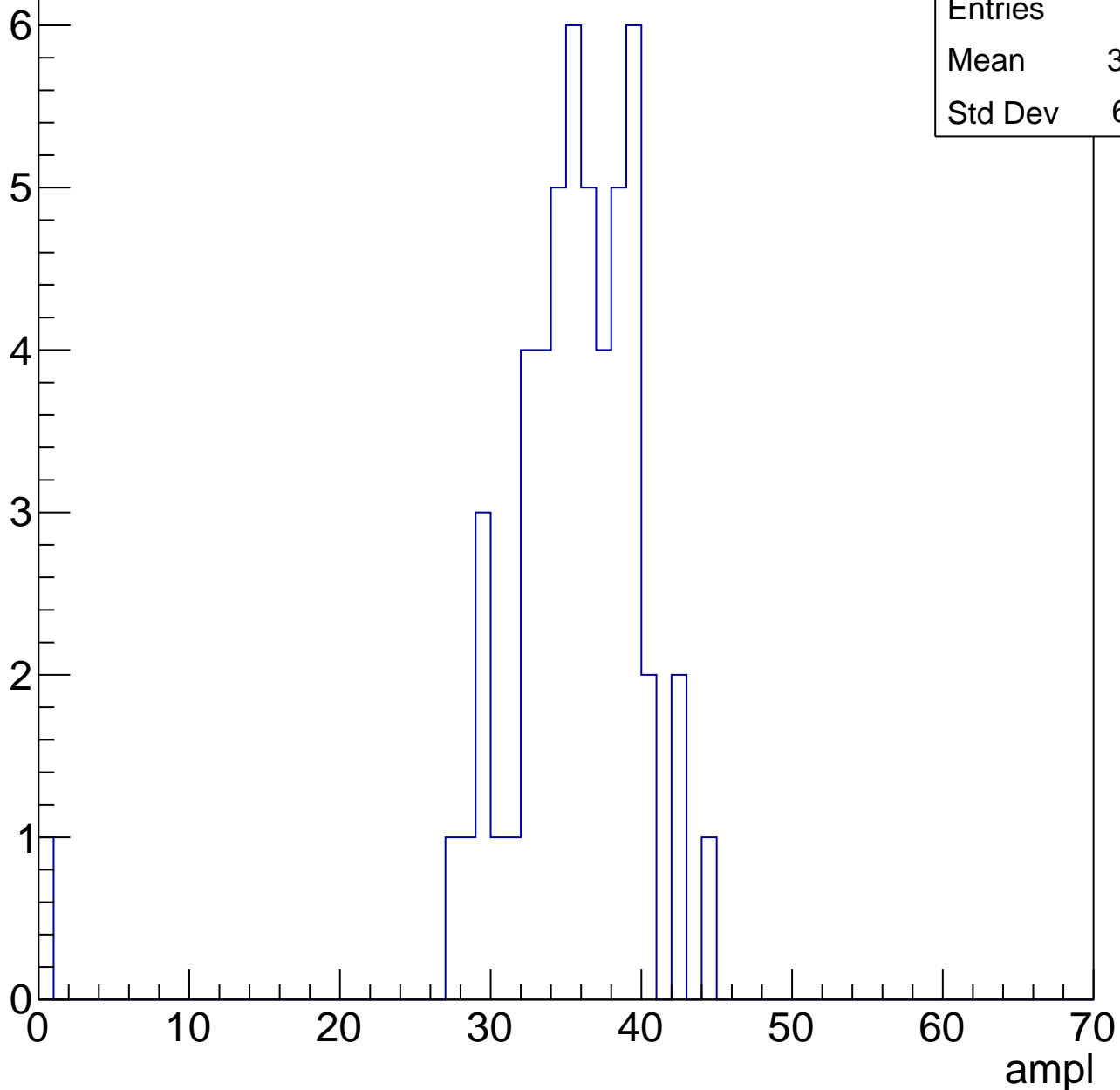


B1L103S, U23-ch20, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	52
Mean	34.67
Std Dev	6.091

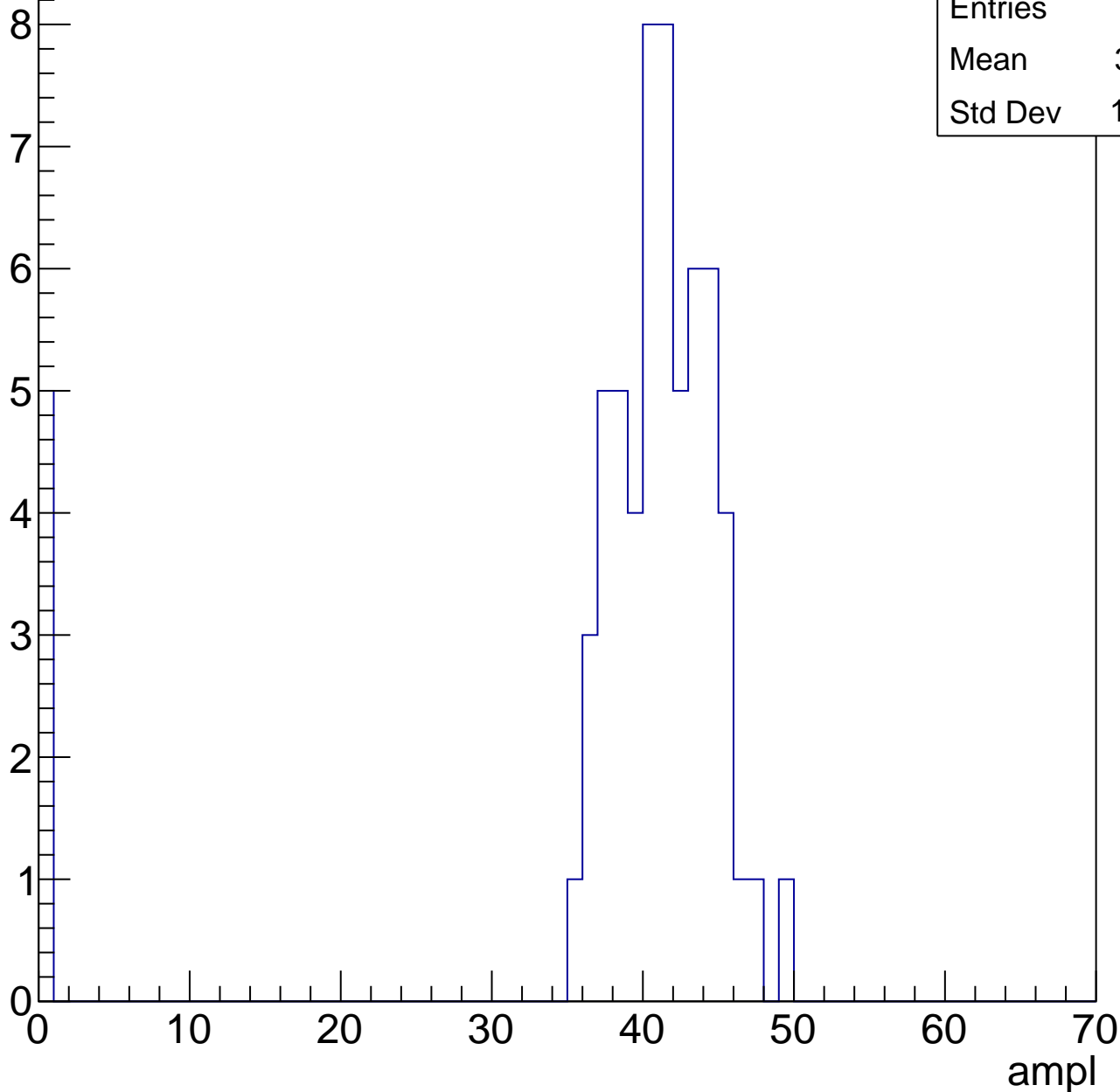


B1L103S, U23-ch20, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	63
Mean	37.71
Std Dev	11.45

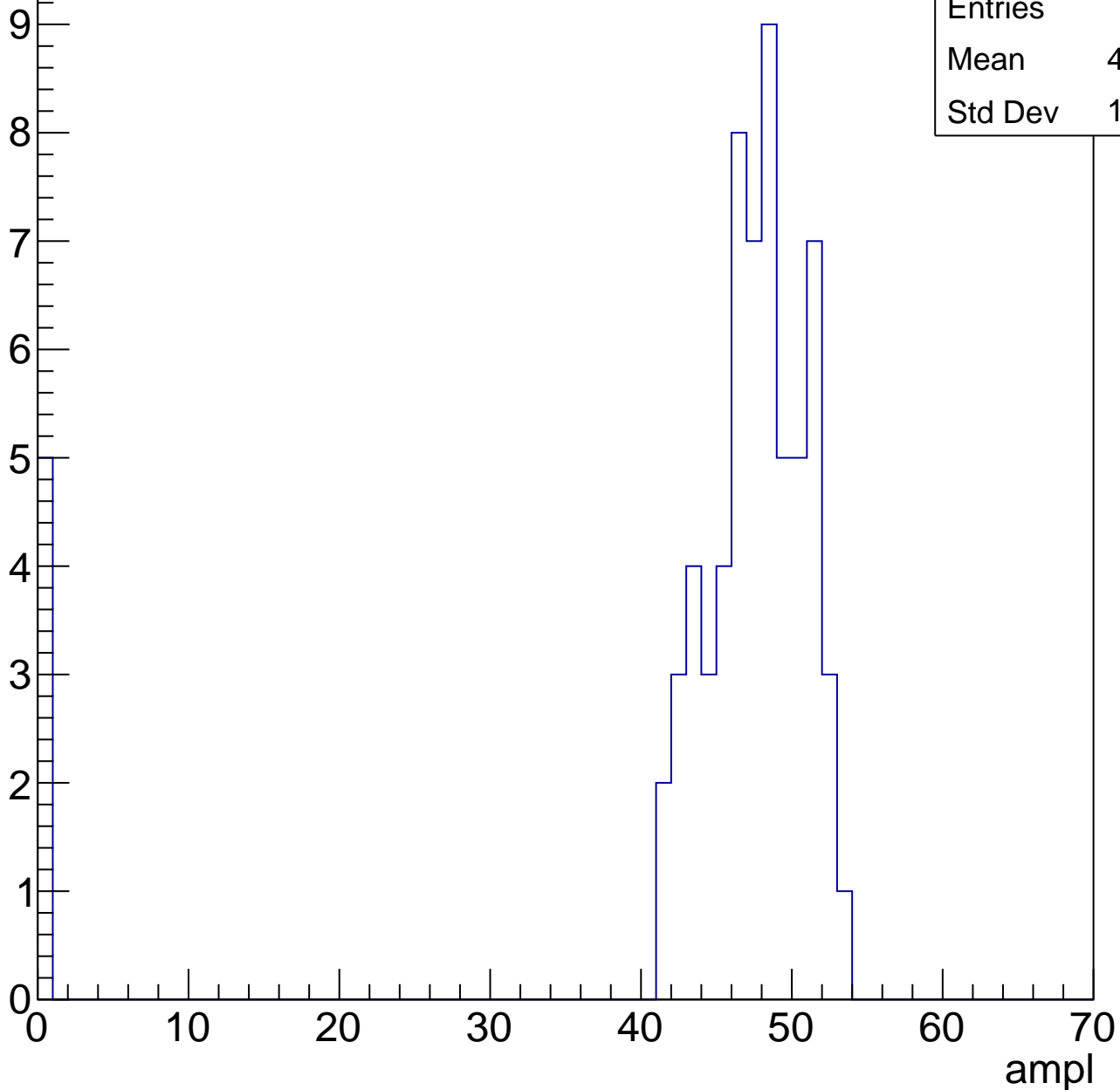


B1L103S, U23-ch20, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	43.67
Std Dev	12.83

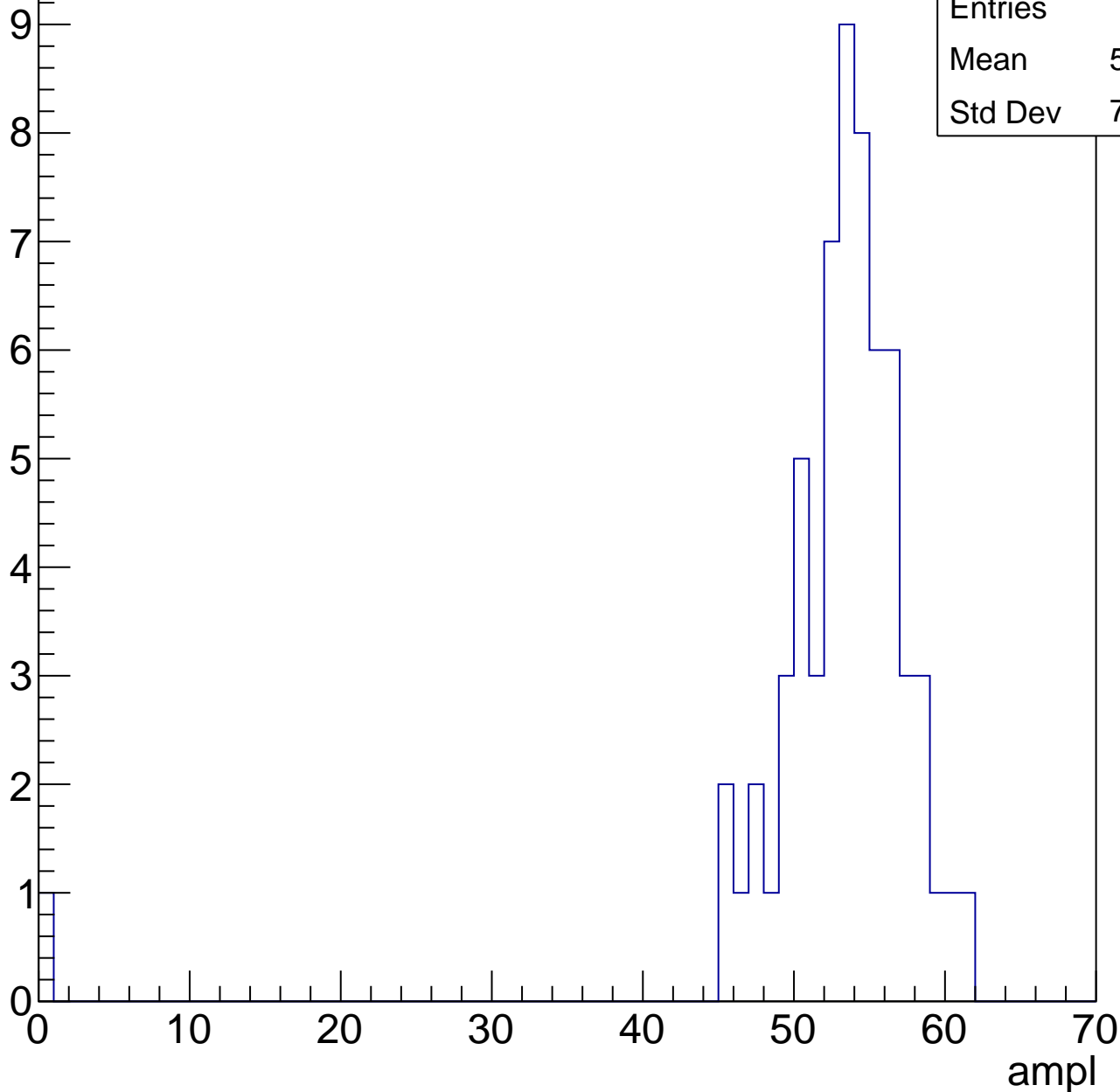


B1L103S, U23-ch20, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

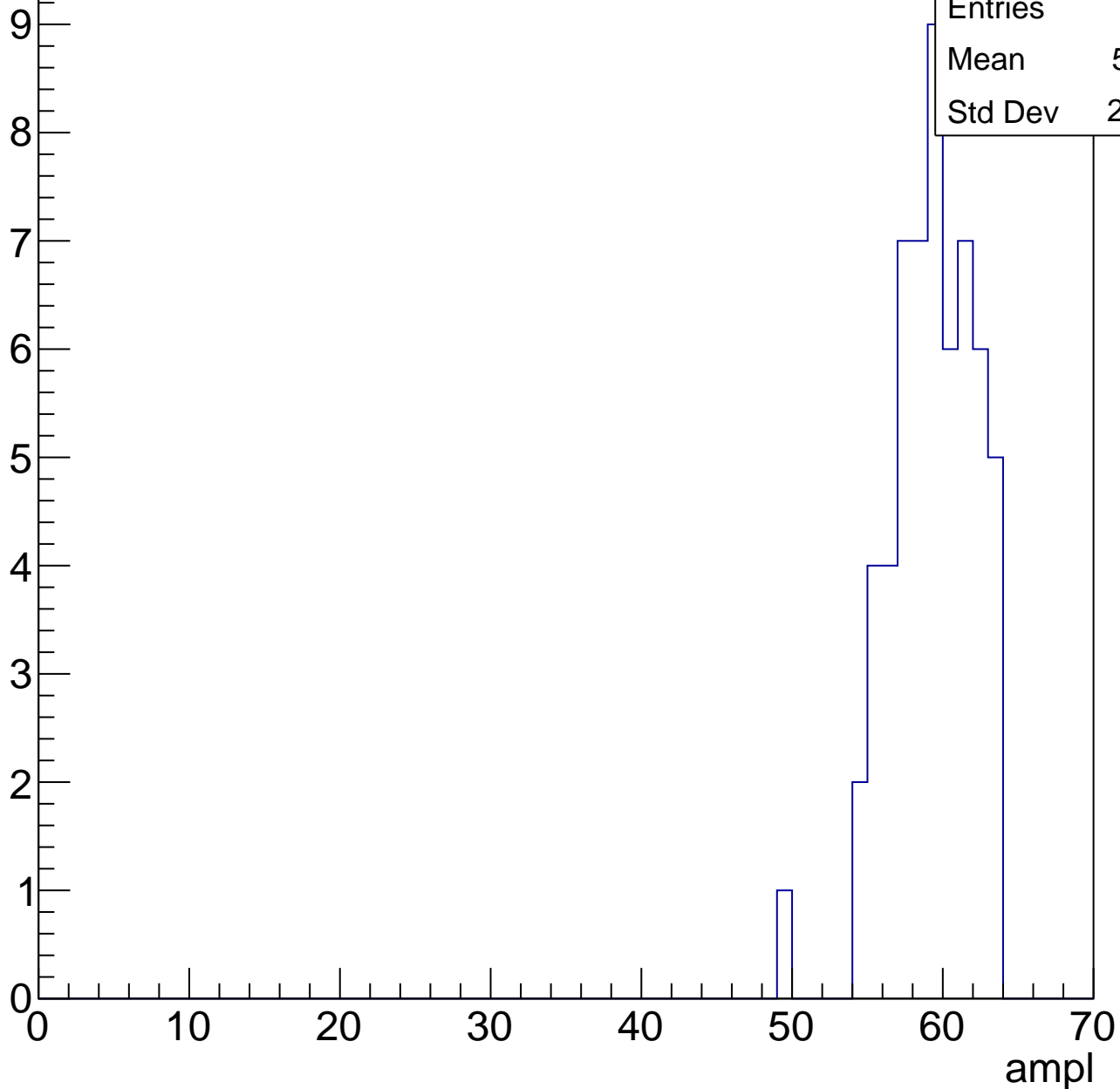
Entries	63
Mean	52.25
Std Dev	7.473



B1L103S, U23-ch20, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

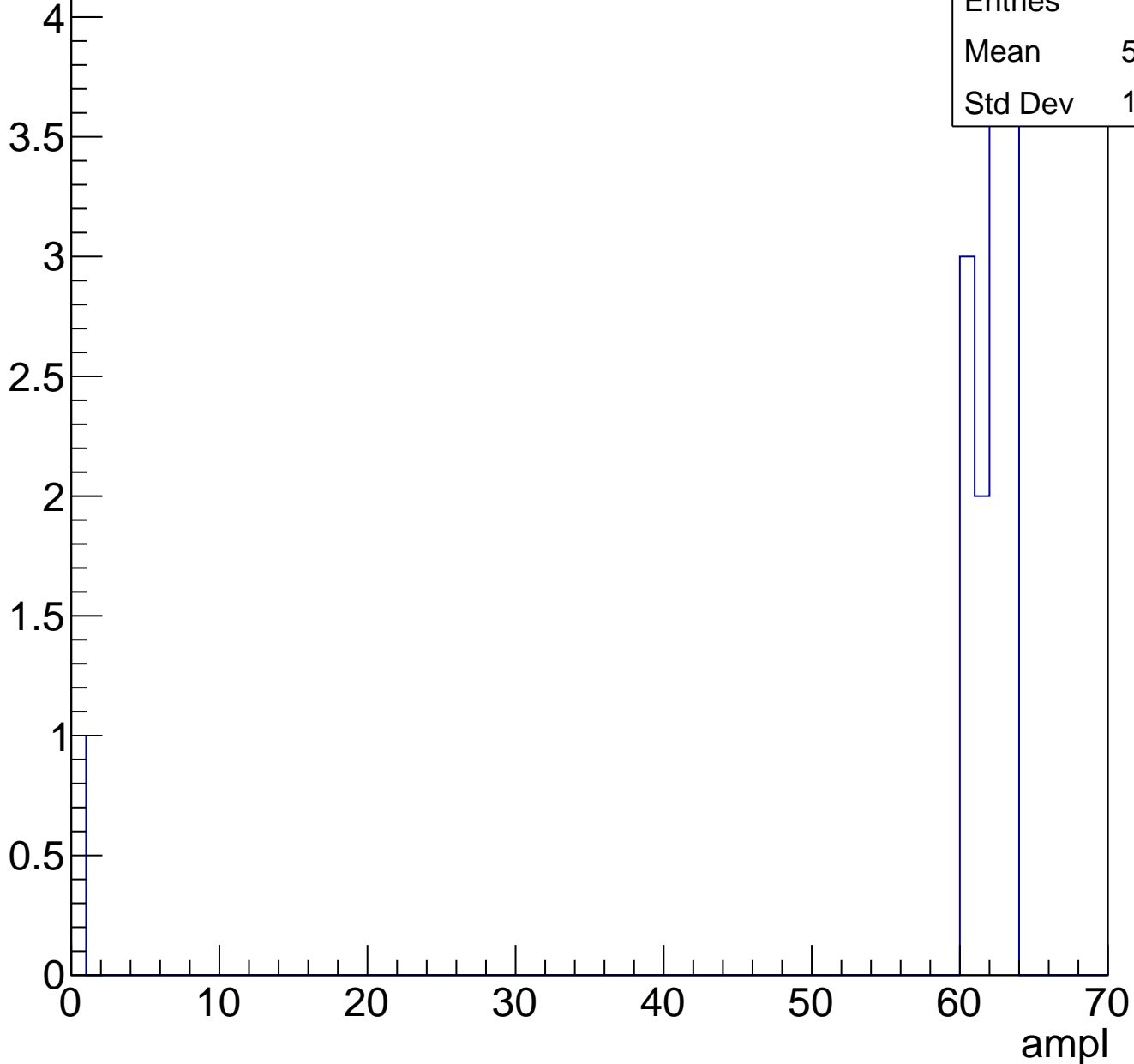


Entries	58
Mean	58.81
Std Dev	2.788

B1L103S, U23-ch20, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

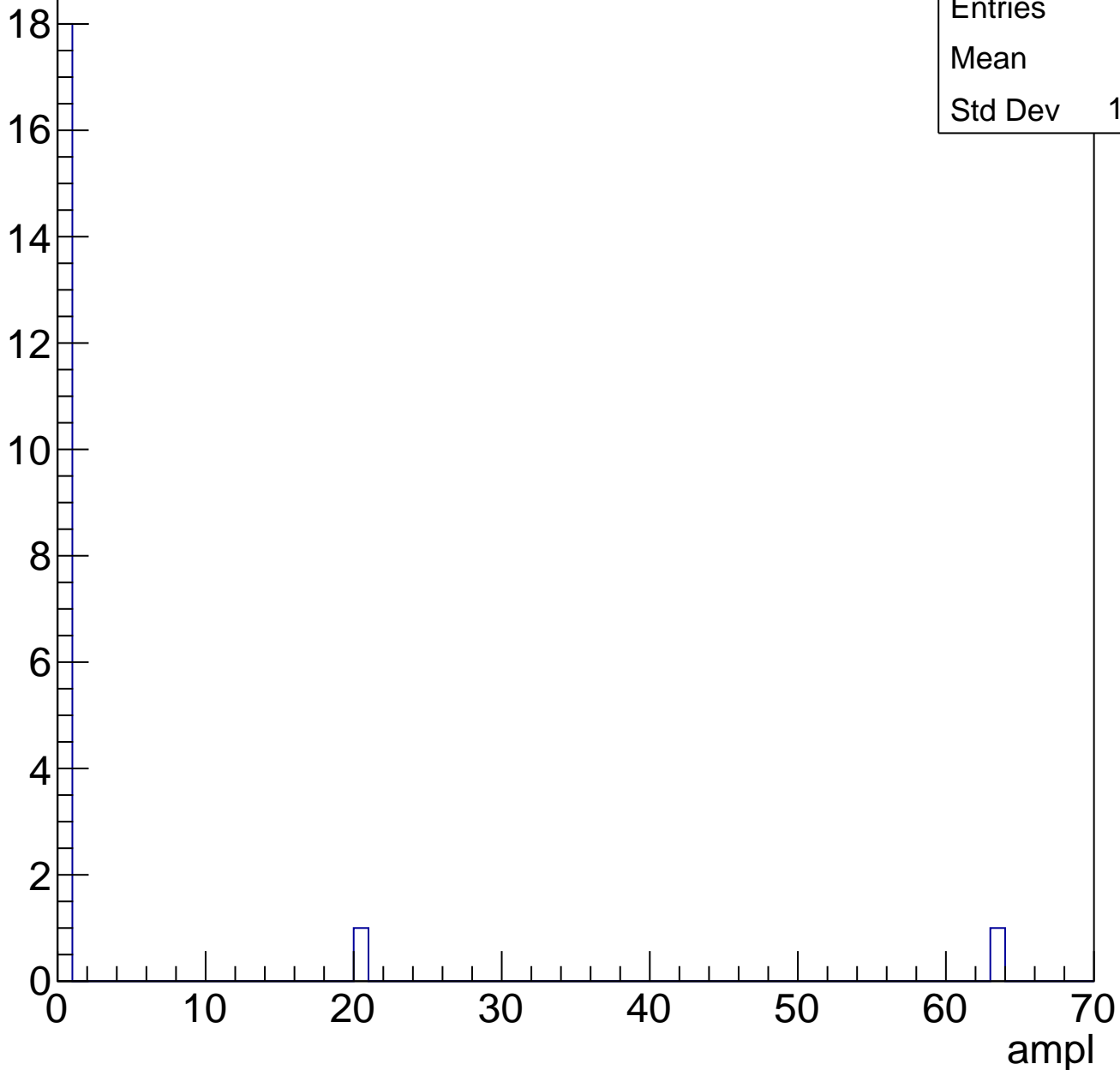


B1L103S, U23-ch20, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	4.15
Std Dev	14.19

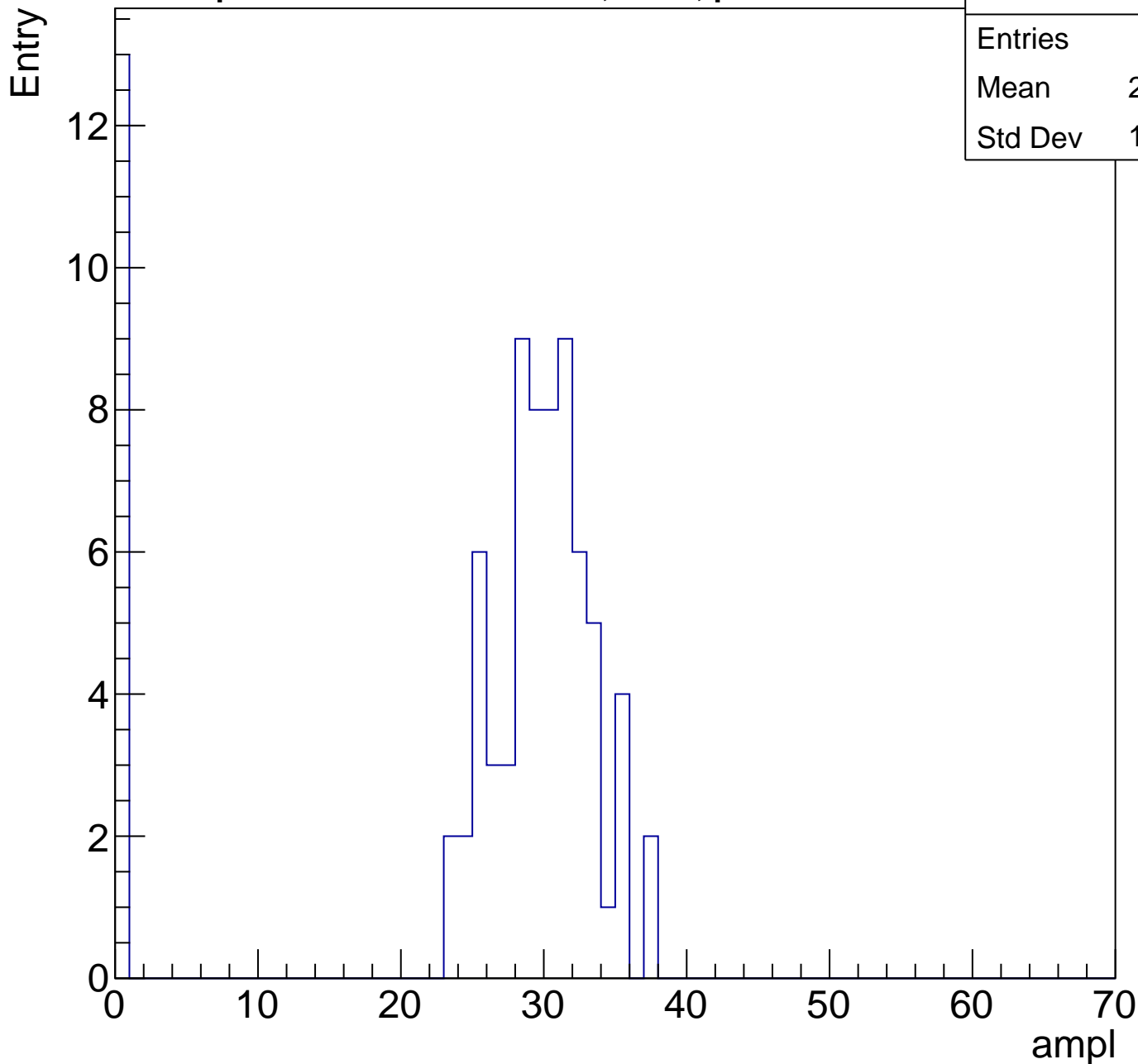
Entry



B1L103S, U23-ch21, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	81
Mean	24.83
Std Dev	11.26



B1L103S, U23-ch21, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	85
Mean	35.75
Std Dev	7.6

Entry

10

8

6

4

2

0

0

10

20

30

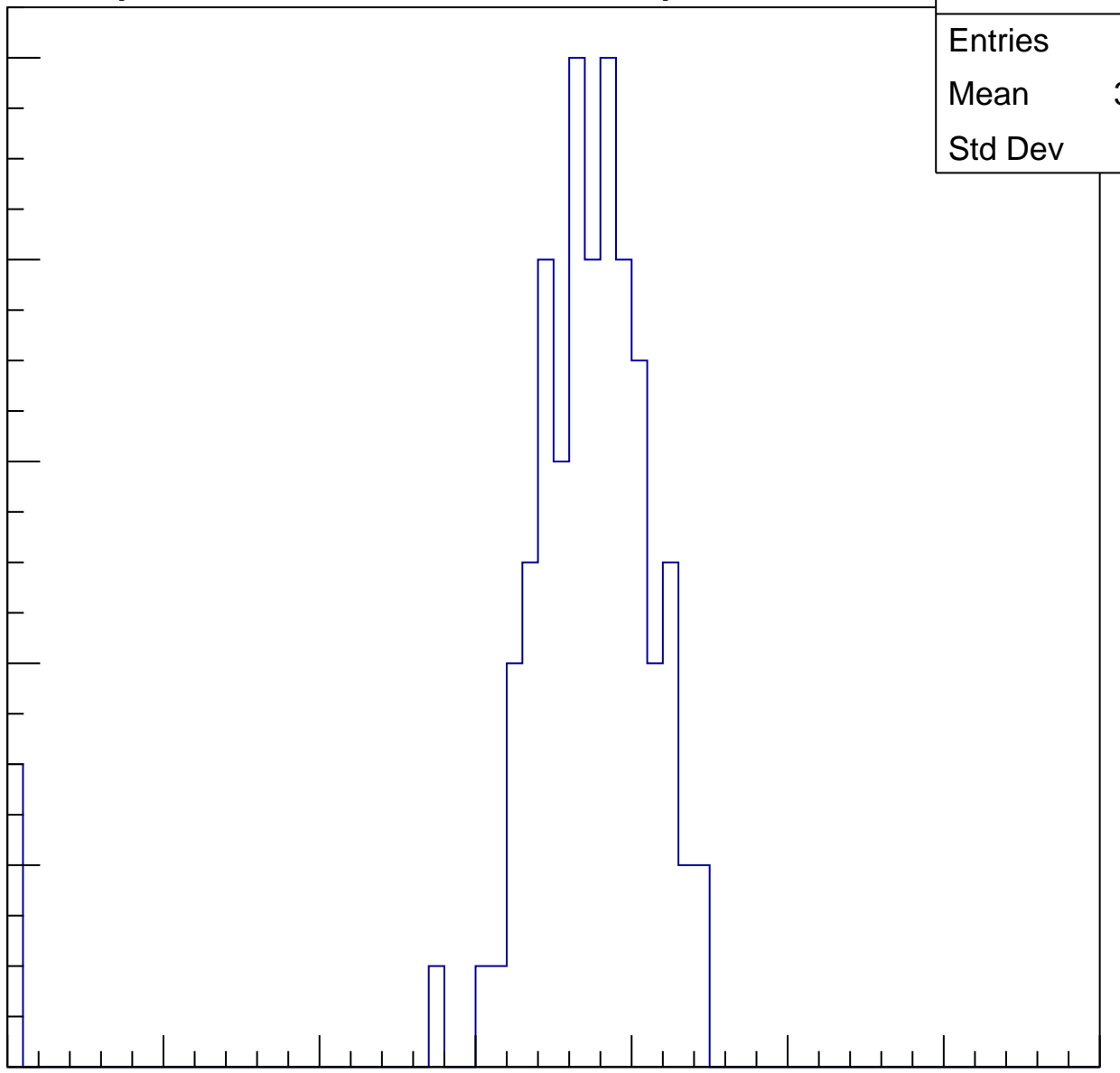
40

50

60

70

ampl



B1L103S, U23-ch21, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	76
Mean	38.07
Std Dev	15.93

Entry

10

8

6

4

2

0

0

10

20

30

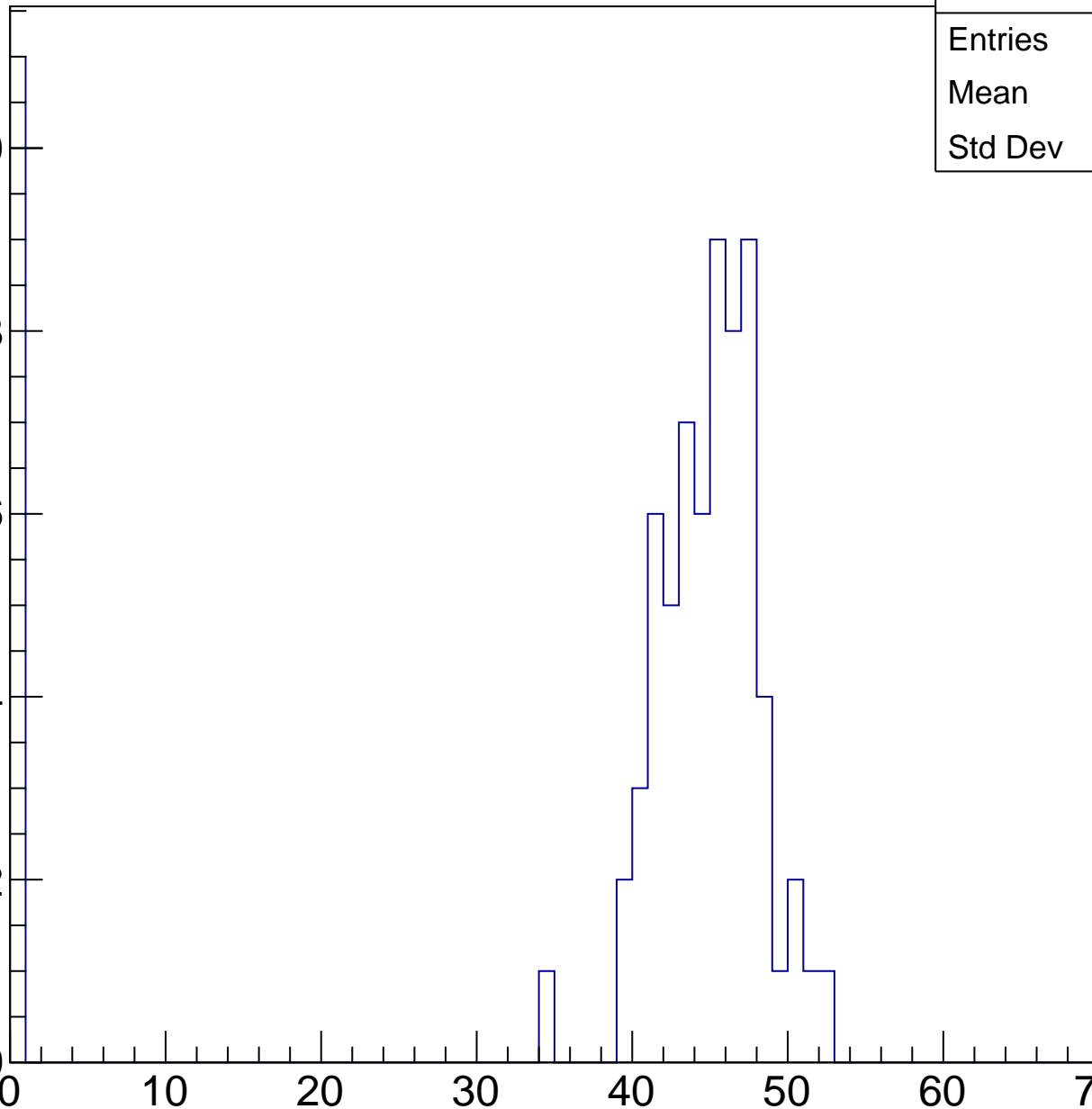
40

50

60

70

ampl

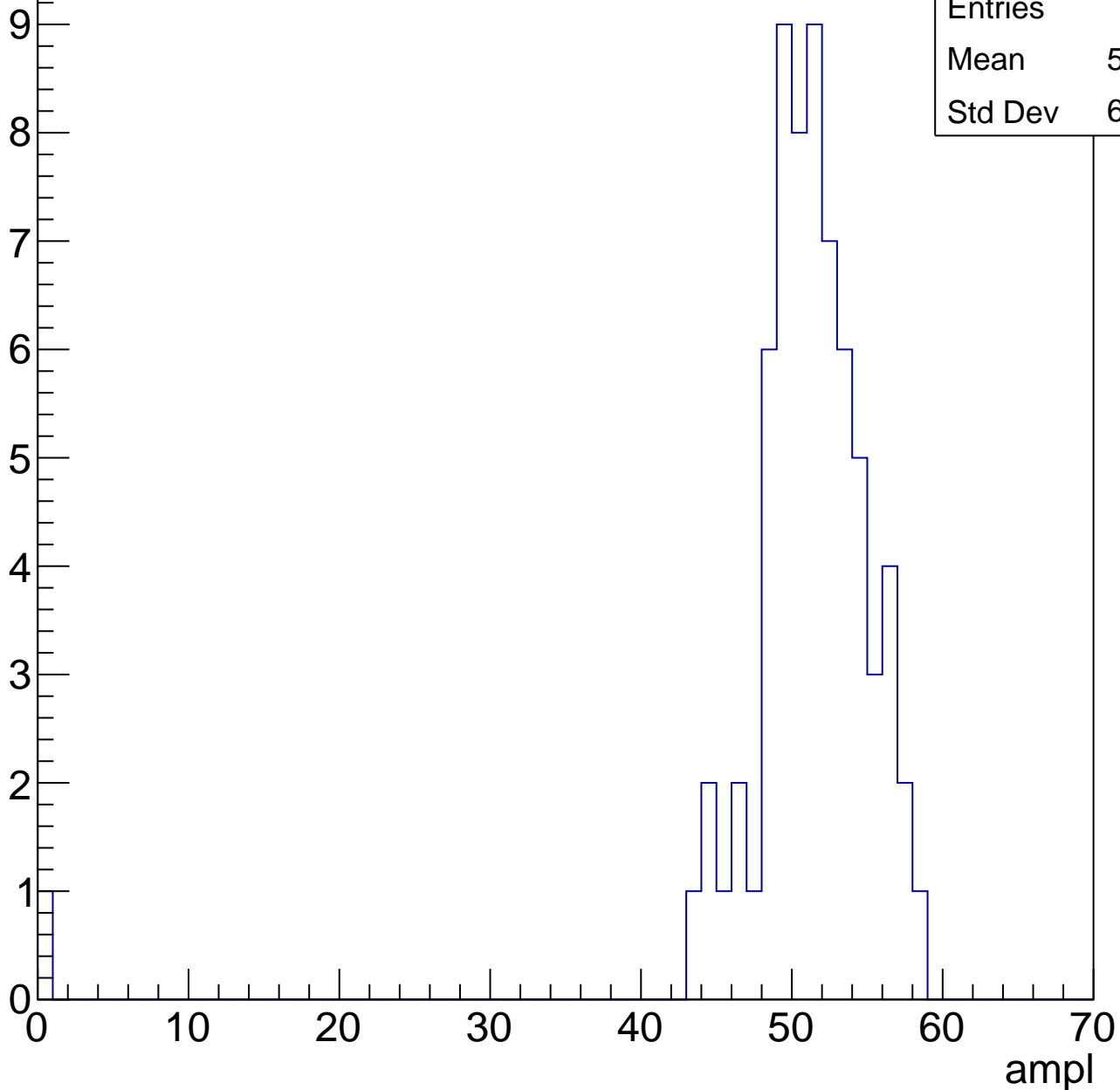


B1L103S, U23-ch21, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	50.24
Std Dev	6.933



B1L103S, U23-ch21, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

6

5

4

3

2

1

0

Entries 40

Mean 56.5

Std Dev 2.748

0

10

20

30

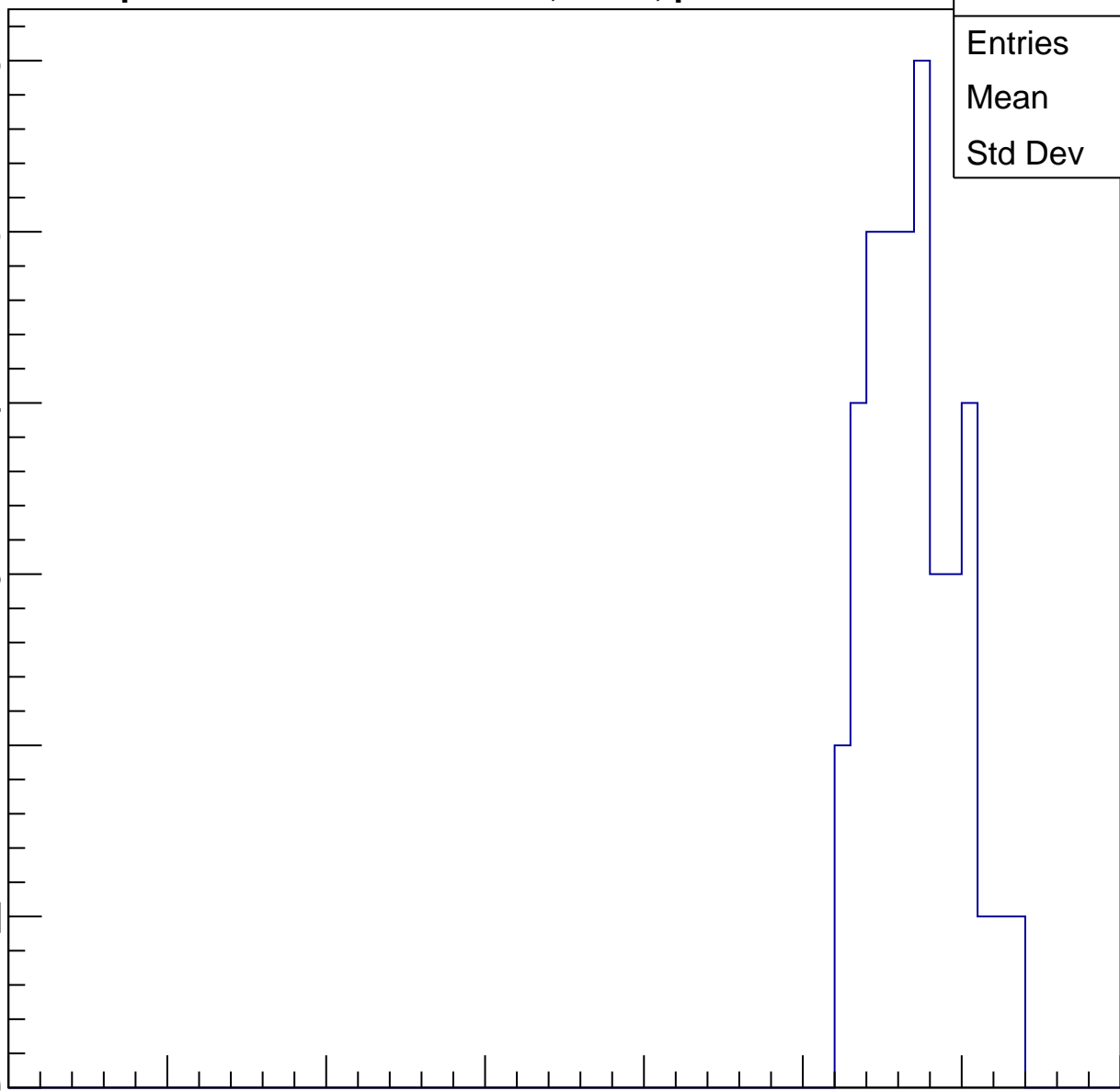
40

50

60

70

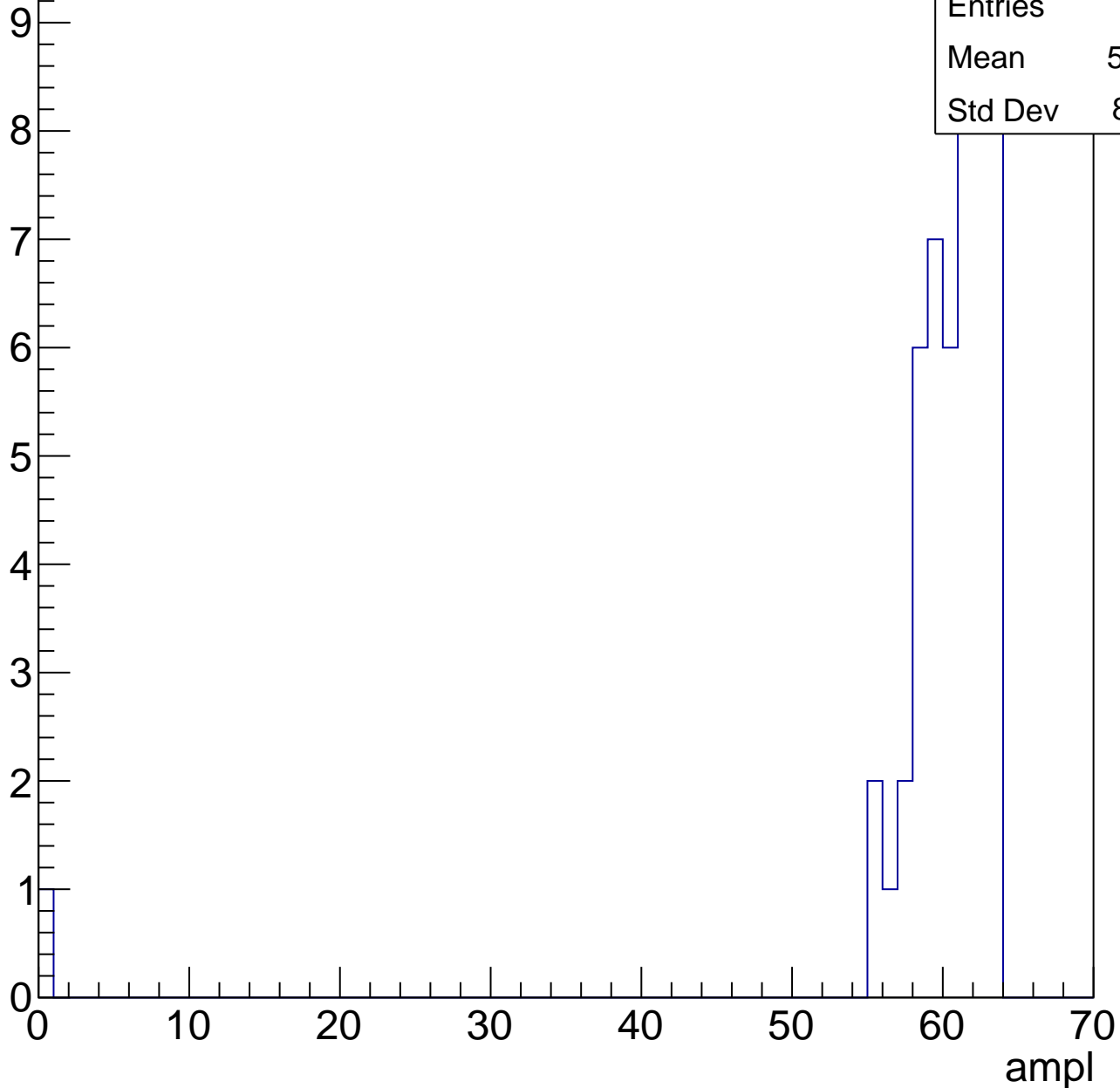
ampl



B1L103S, U23-ch21, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch21, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	0
Mean	0
Std Dev	0

B1L103S, U23-ch21, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.158
Std Dev	4.913

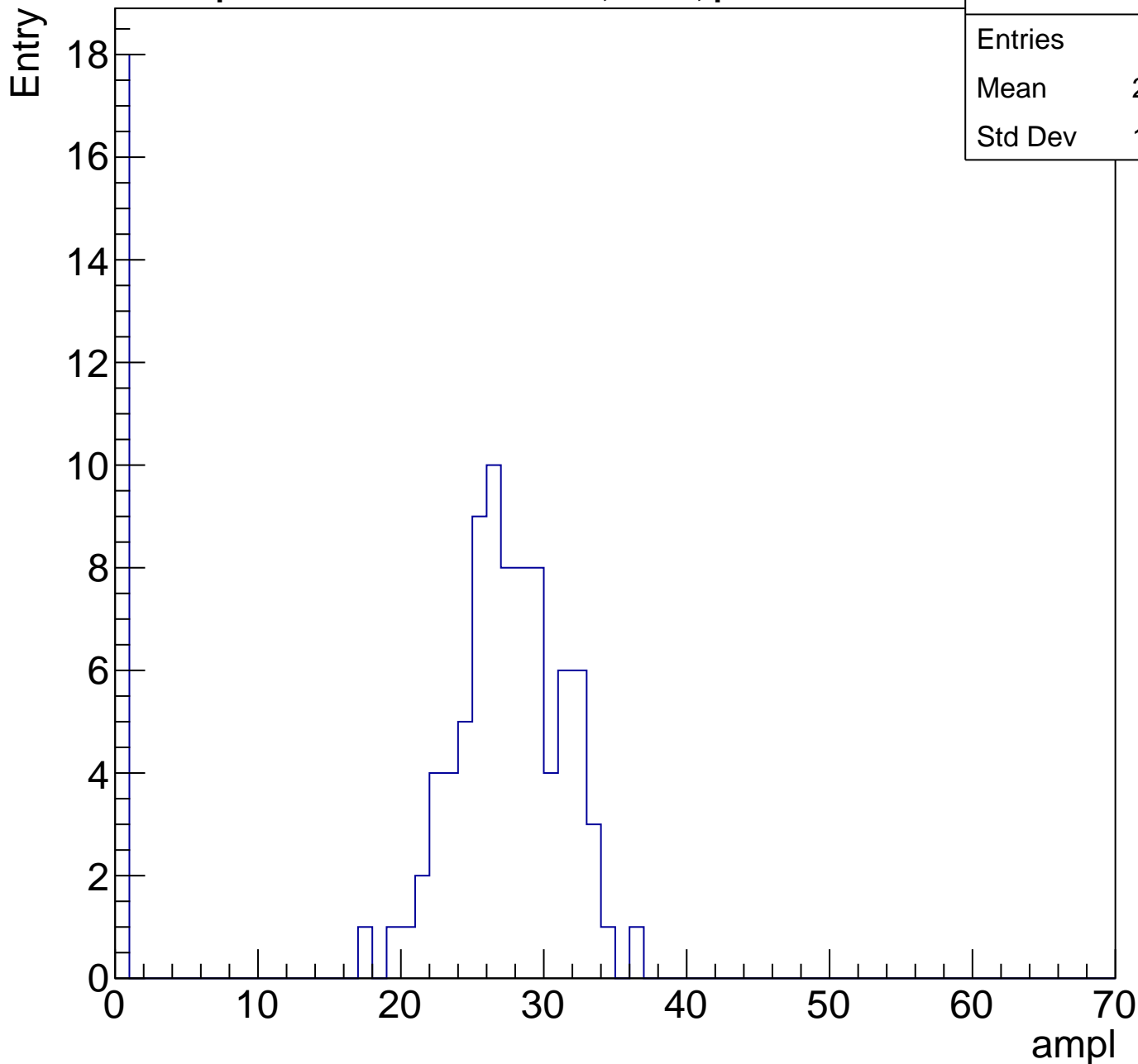
Entry



B1L103S, U23-ch22, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	100
Mean	22.22
Std Dev	10.93

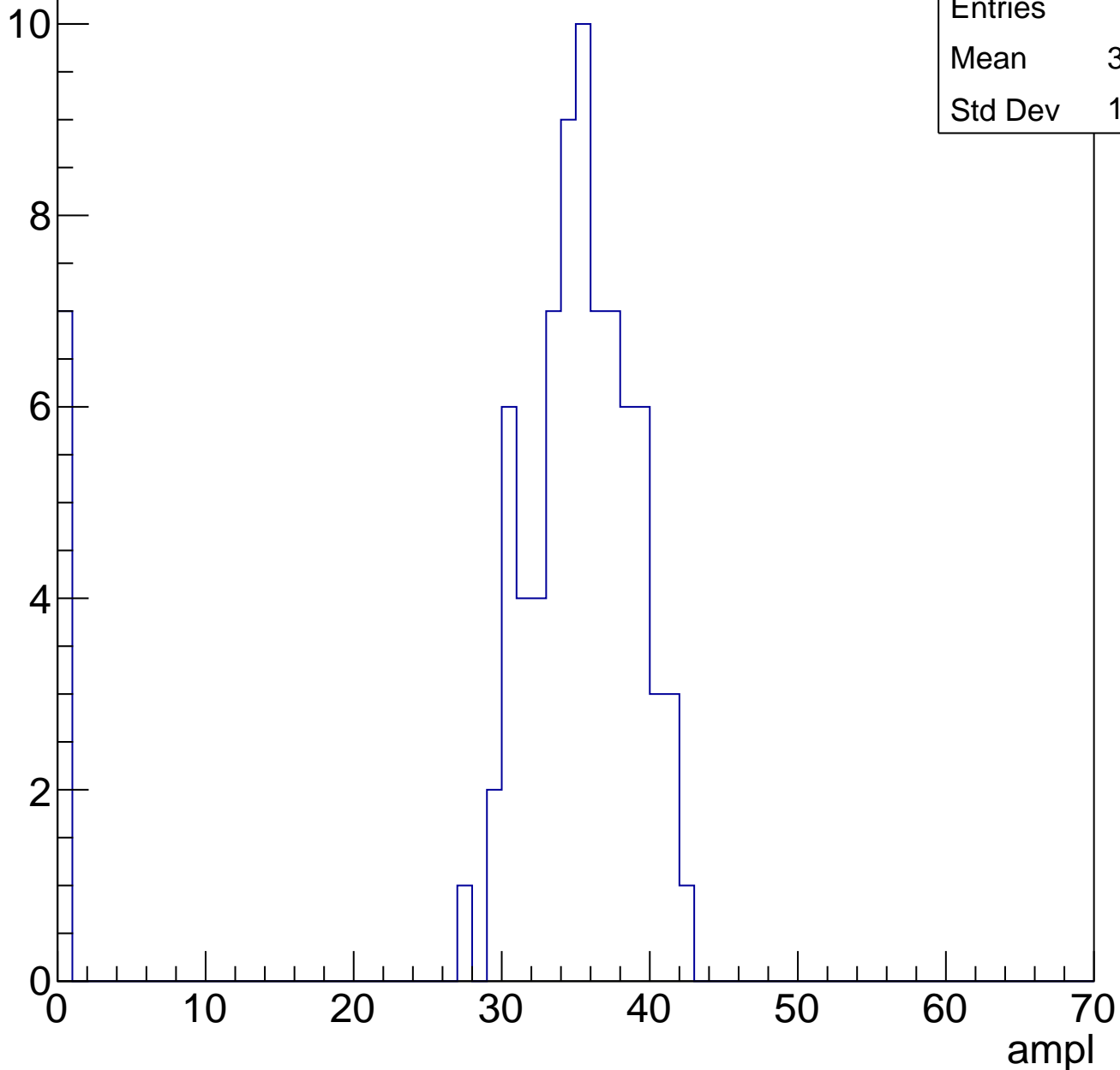


B1L103S, U23-ch22, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	83
Mean	32.07
Std Dev	10.24

Entry

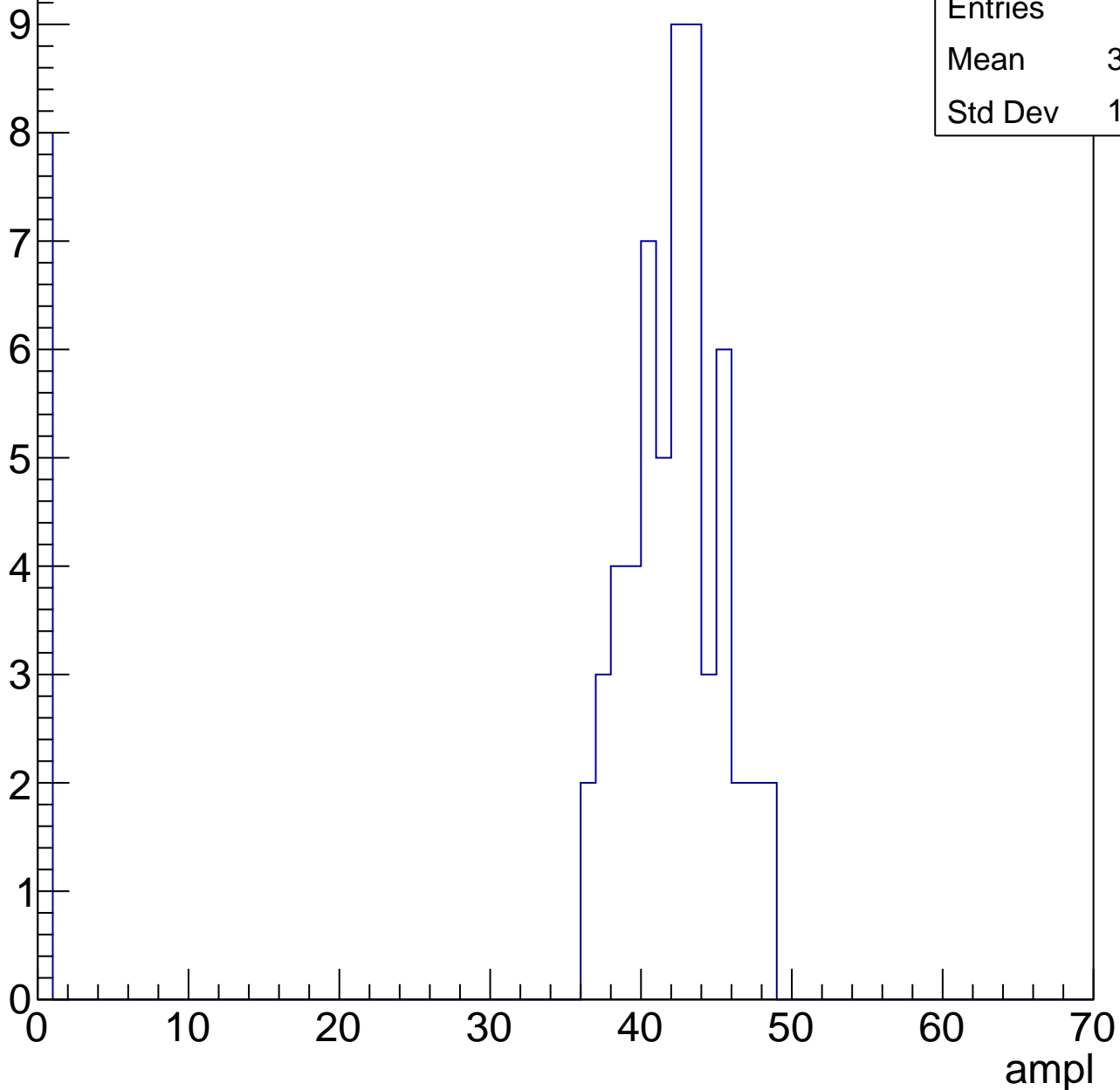


B1L103S, U23-ch22, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	36.74
Std Dev	13.92

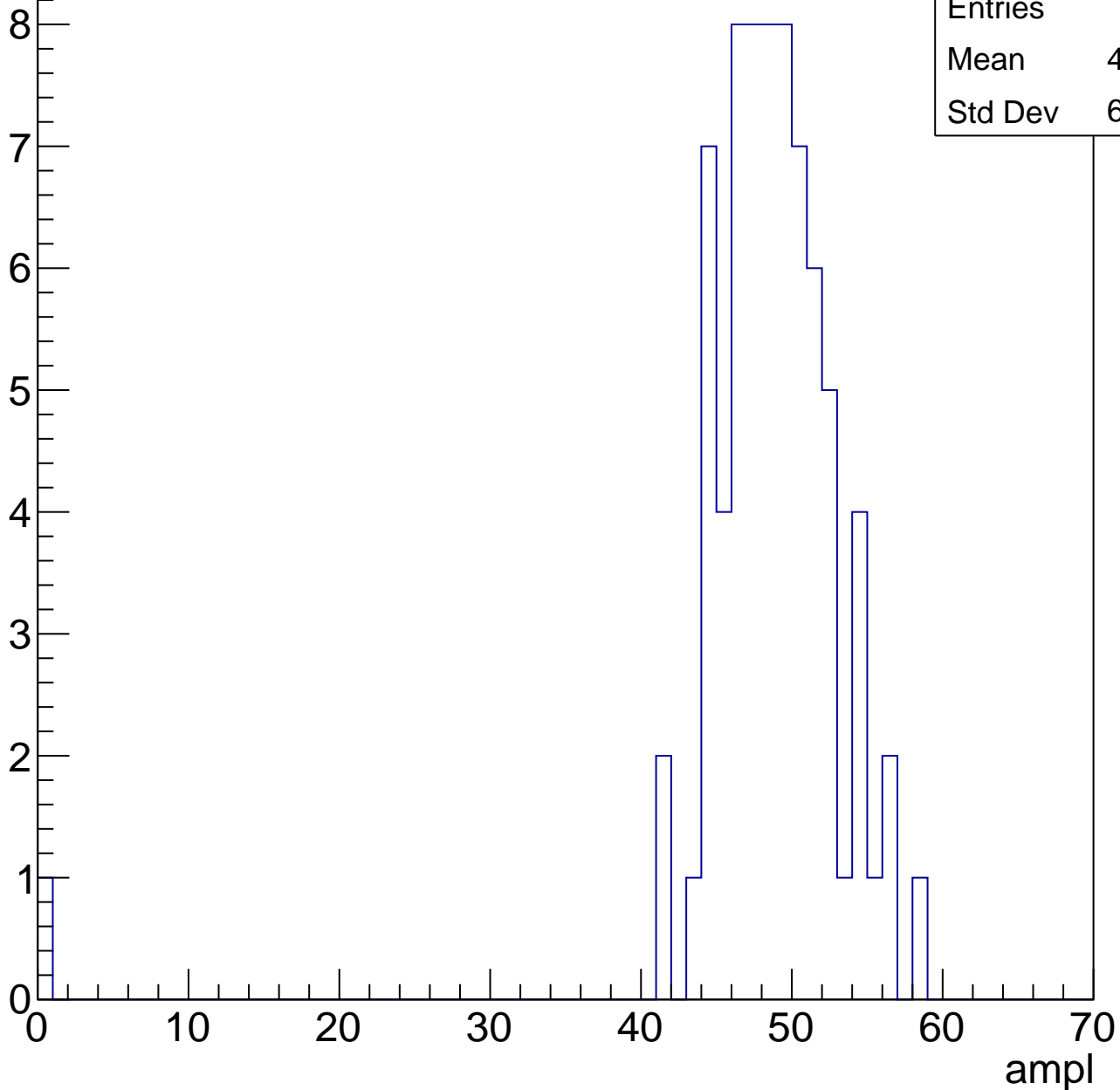


B1L103S, U23-ch22, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	74
Mean	47.88
Std Dev	6.607

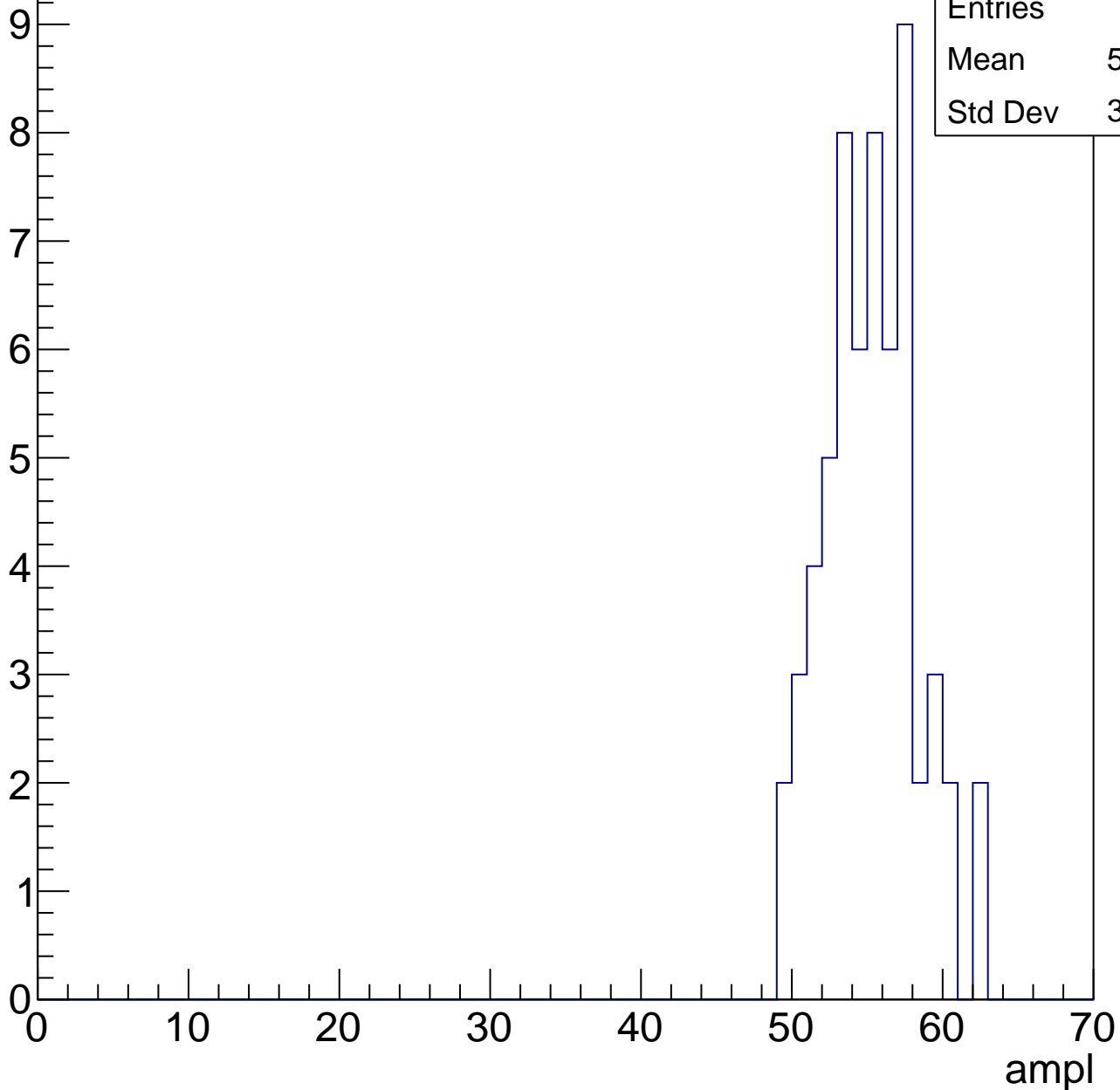


B1L103S, U23-ch22, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	54.77
Std Dev	3.019



B1L103S, U23-ch22, adc5

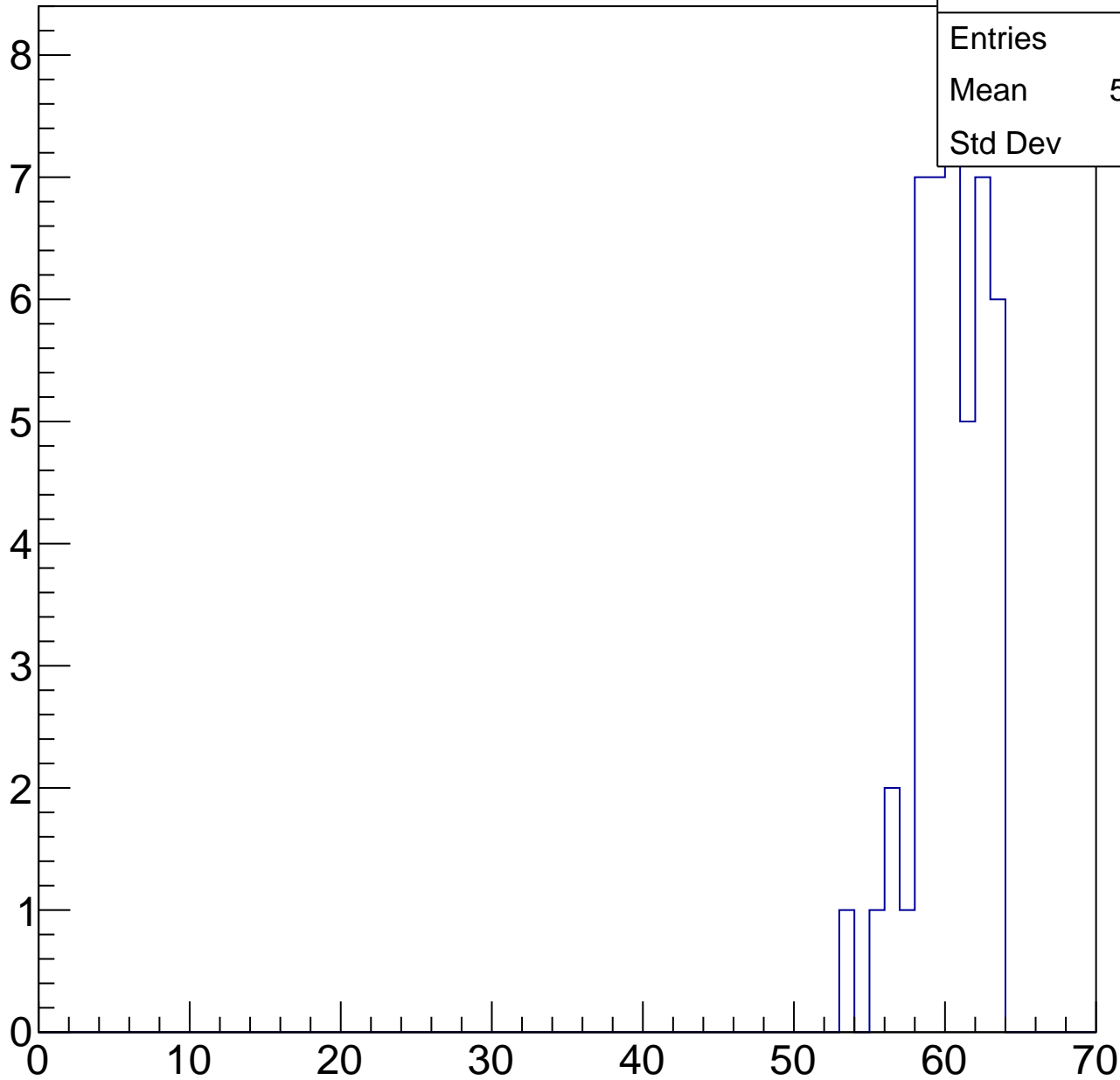
calib_packv5_041523_1651.root, FC#0, port C2

Entry

8
7
6
5
4
3
2
1
0

Entries	45
Mean	59.84
Std Dev	2.29

ampl

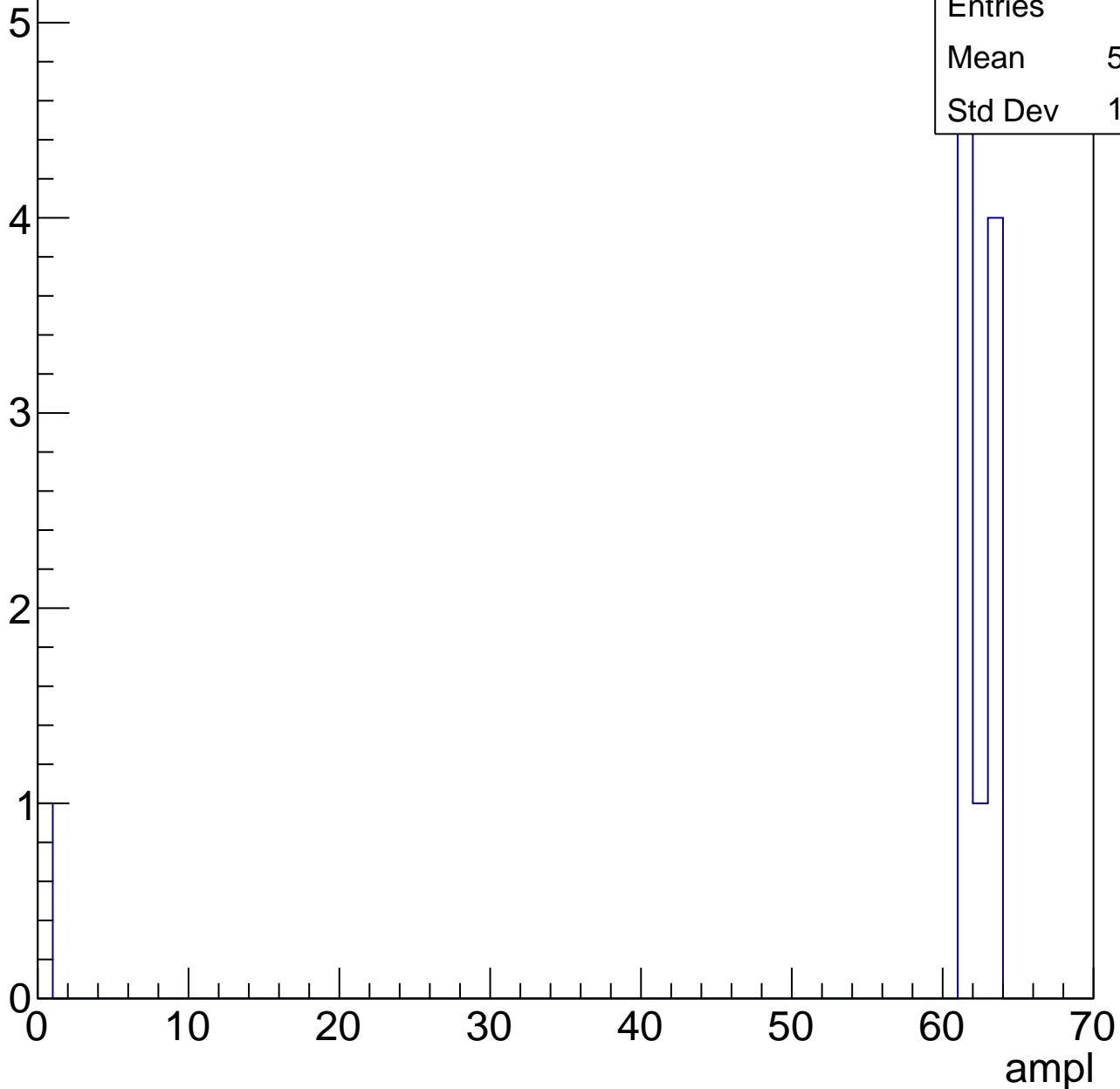


B1L103S, U23-ch22, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	11
Mean	56.27
Std Dev	17.82



B1L103S, U23-ch22, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U23-ch23, adc0

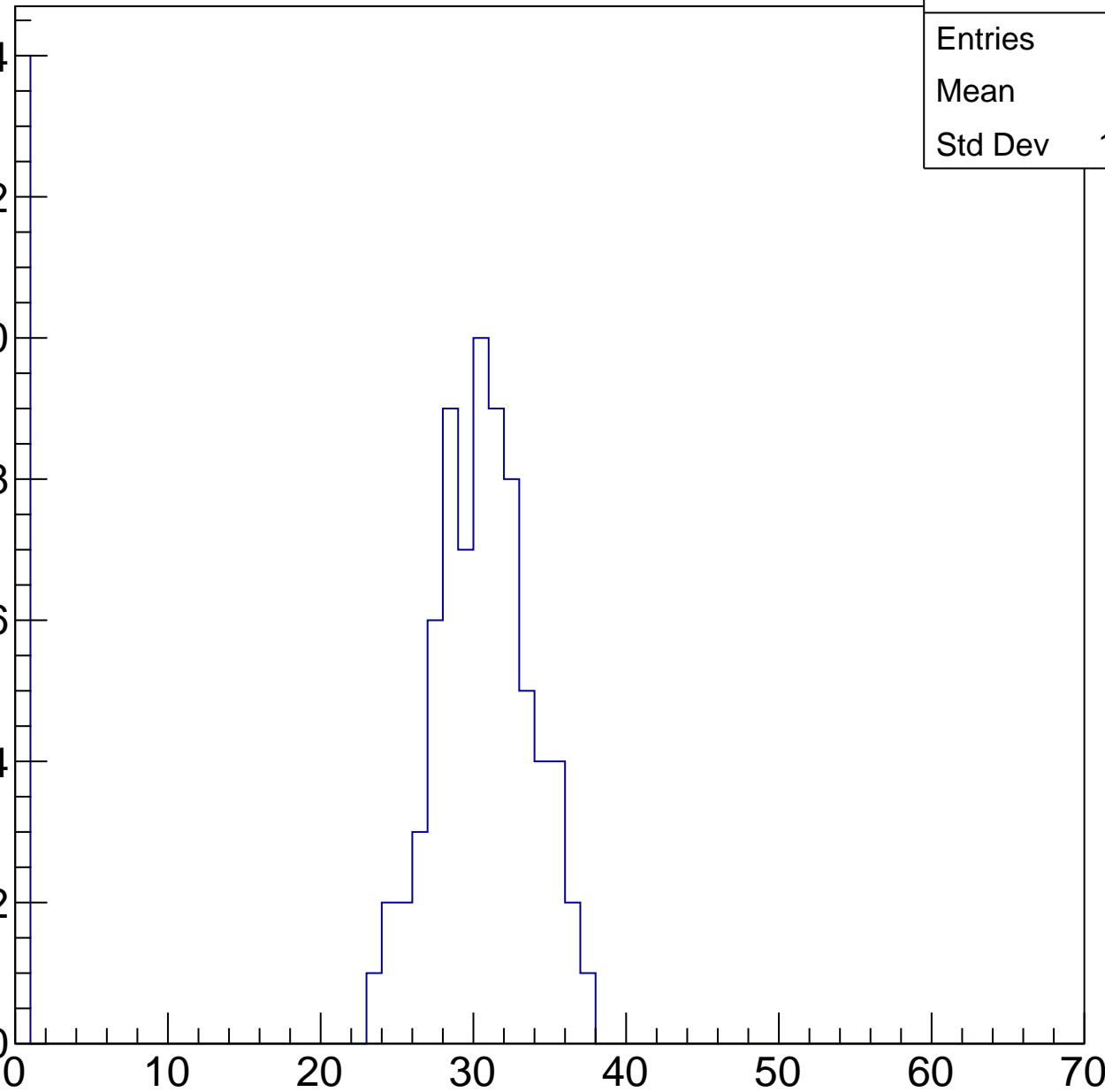
calib_packv5_041523_1651.root, FC#0, port C2

Entries	87
Mean	25.3
Std Dev	11.43

Entry

14
12
10
8
6
4
2
0

ampl

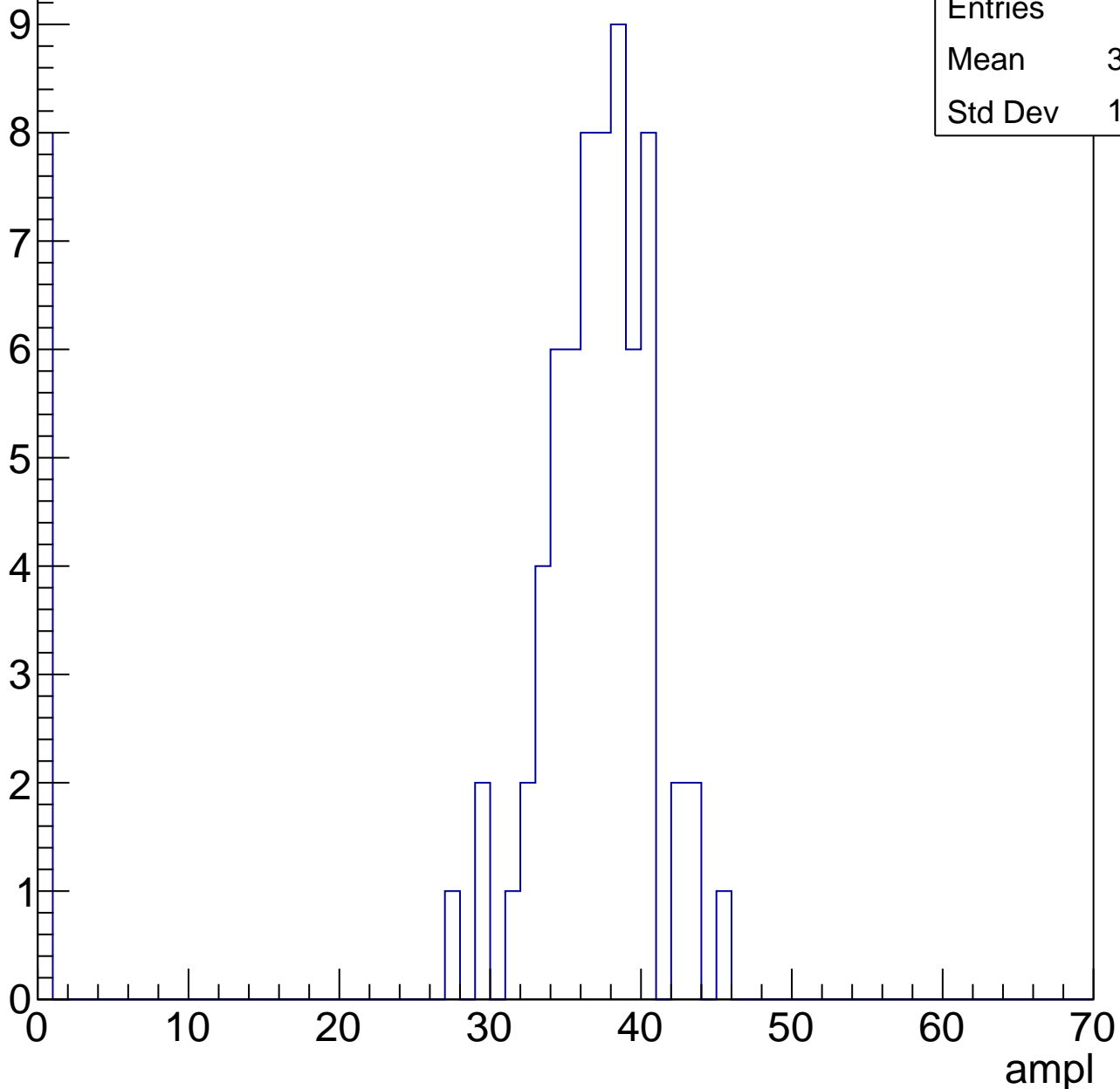


B1L103S, U23-ch23, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	74
Mean	32.72
Std Dev	11.83

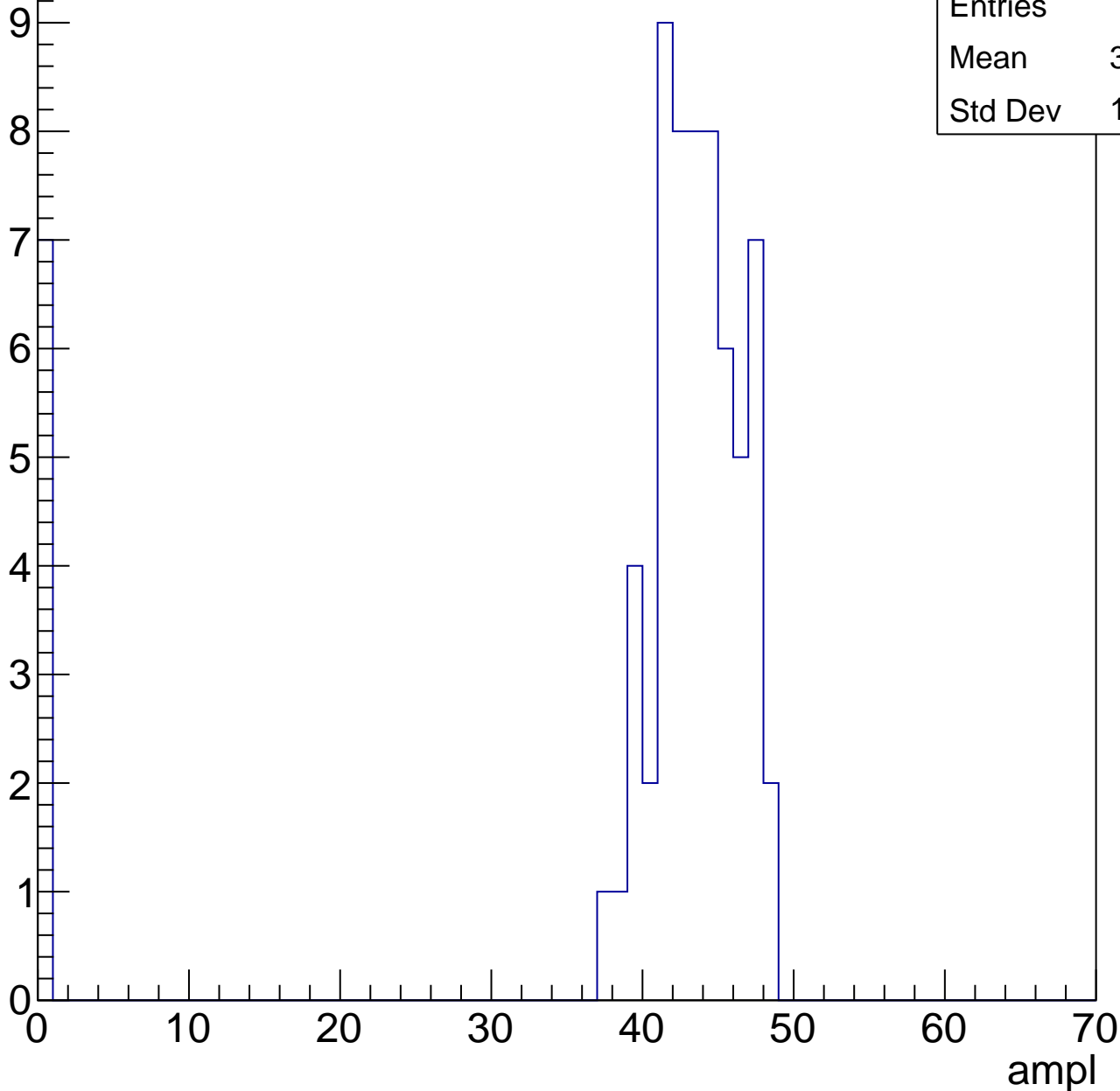


B1L103S, U23-ch23, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	38.78
Std Dev	13.37



B1L103S, U23-ch23, adc3

calib_packv5_041523_1651.root, FC#0, port C2

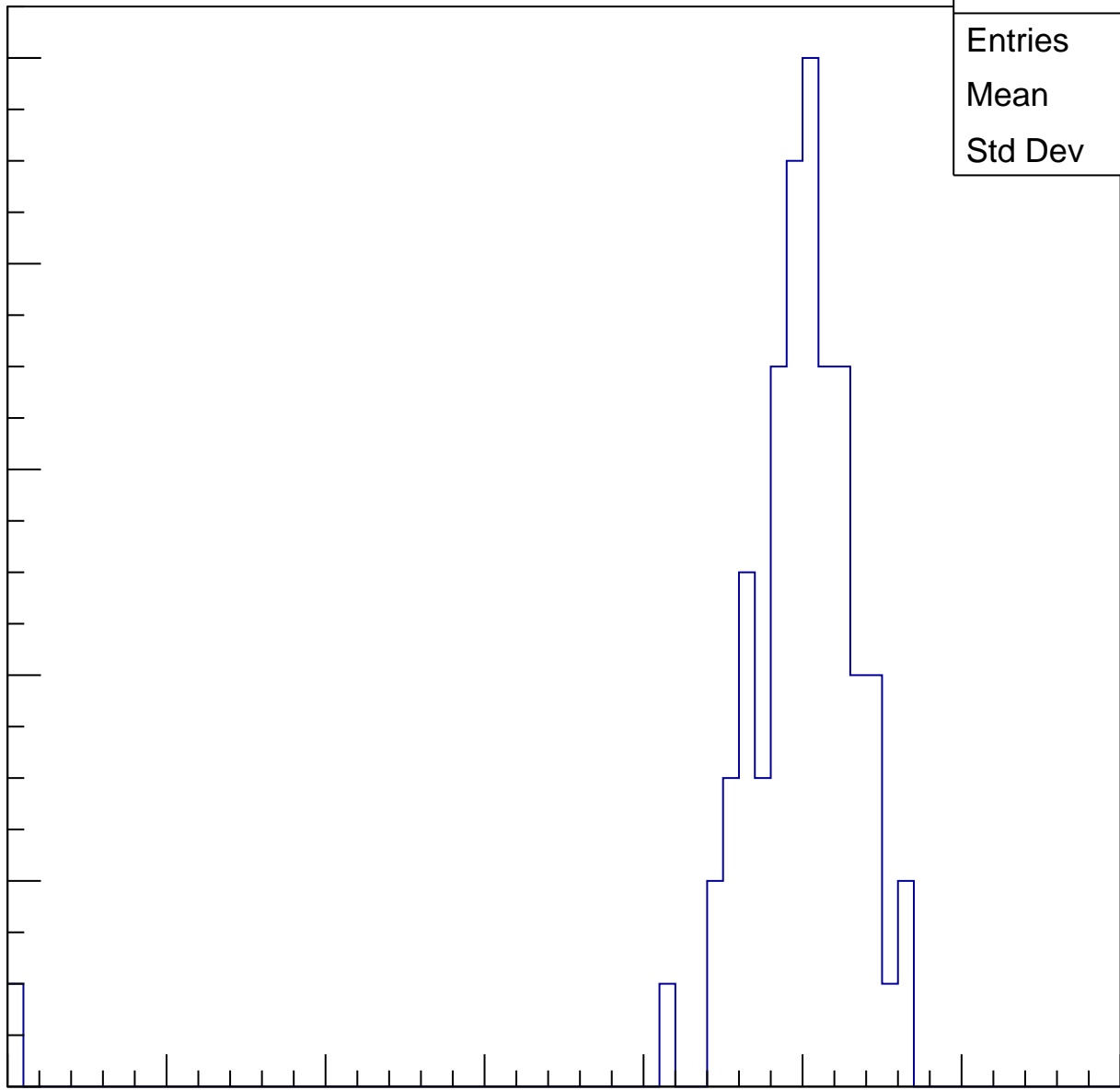
Entries	66
Mean	48.91
Std Dev	6.771

Entry

10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70

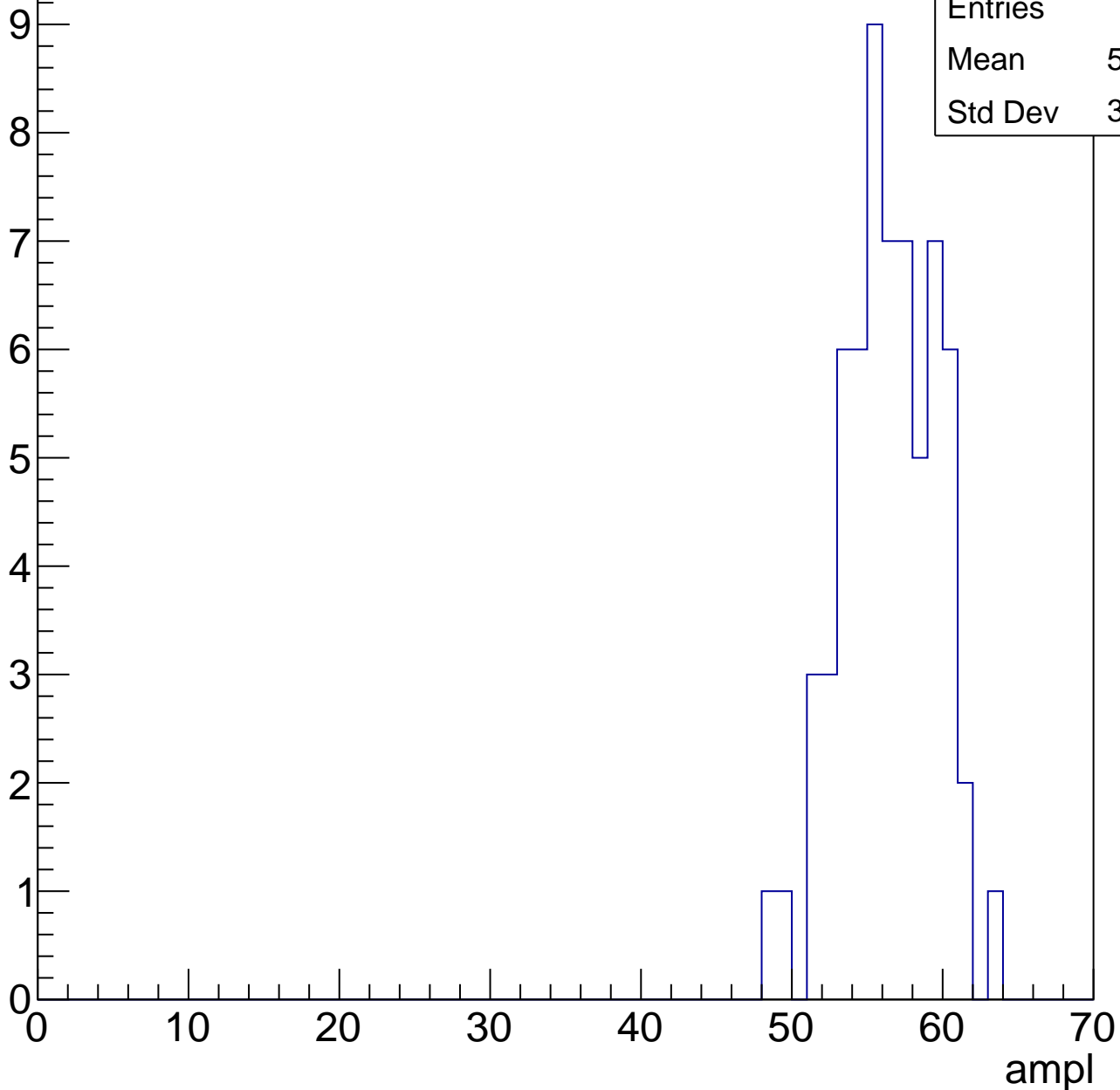


B1L103S, U23-ch23, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	55.97
Std Dev	3.082

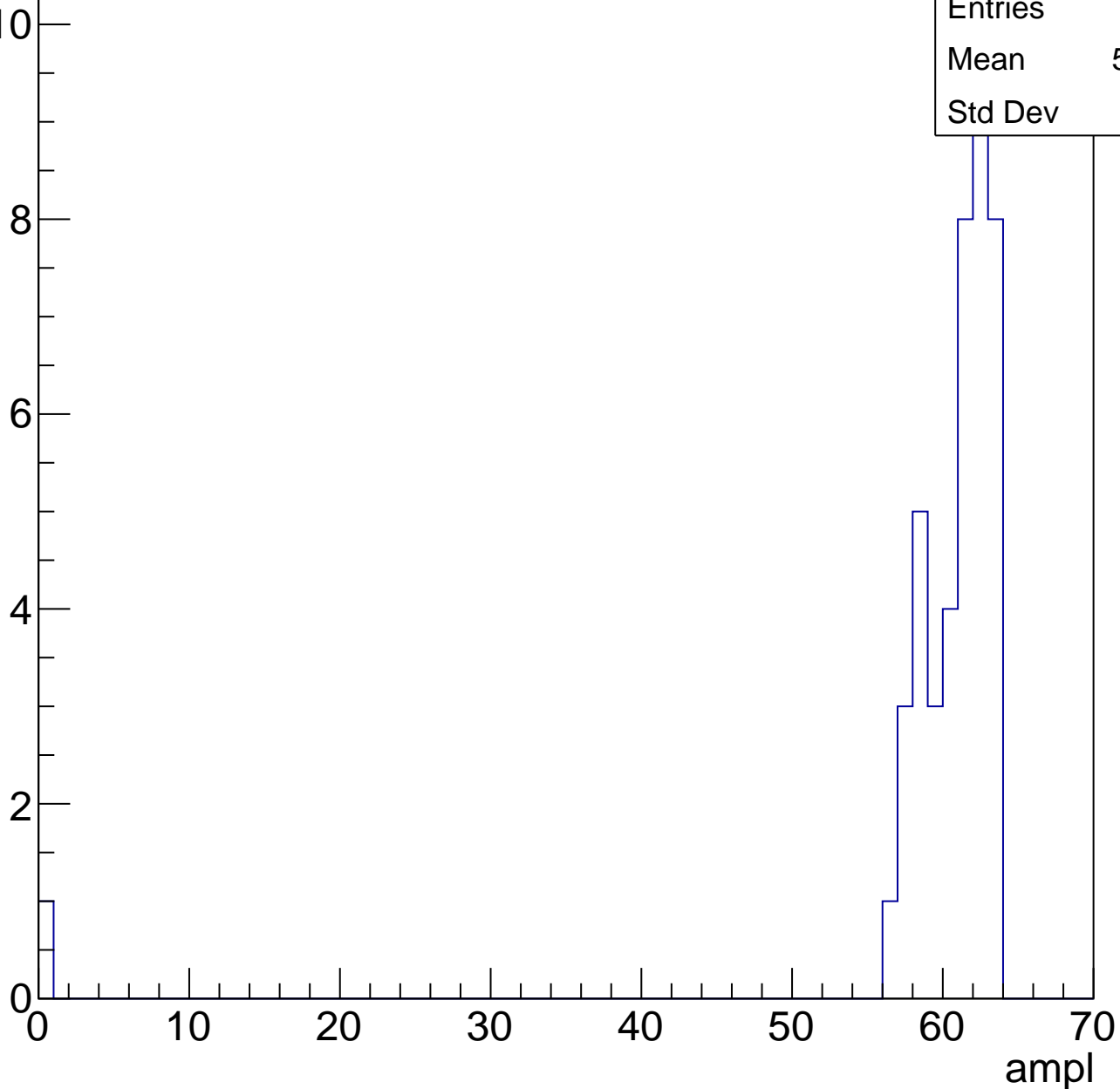


B1L103S, U23-ch23, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	43
Mean	59.21
Std Dev	9.35



B1L103S, U23-ch23, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

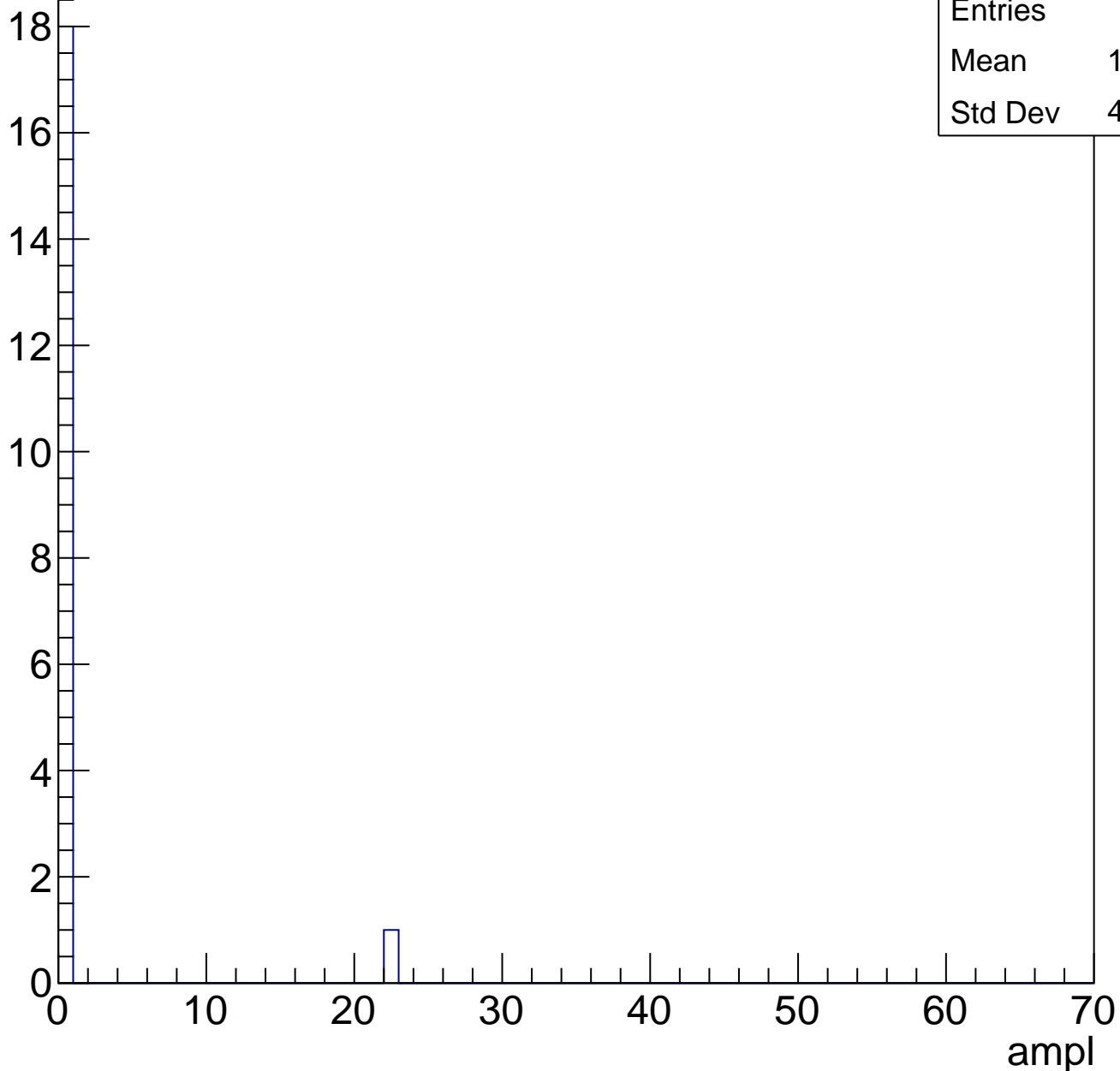


B1L103S, U23-ch23, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.158
Std Dev	4.913

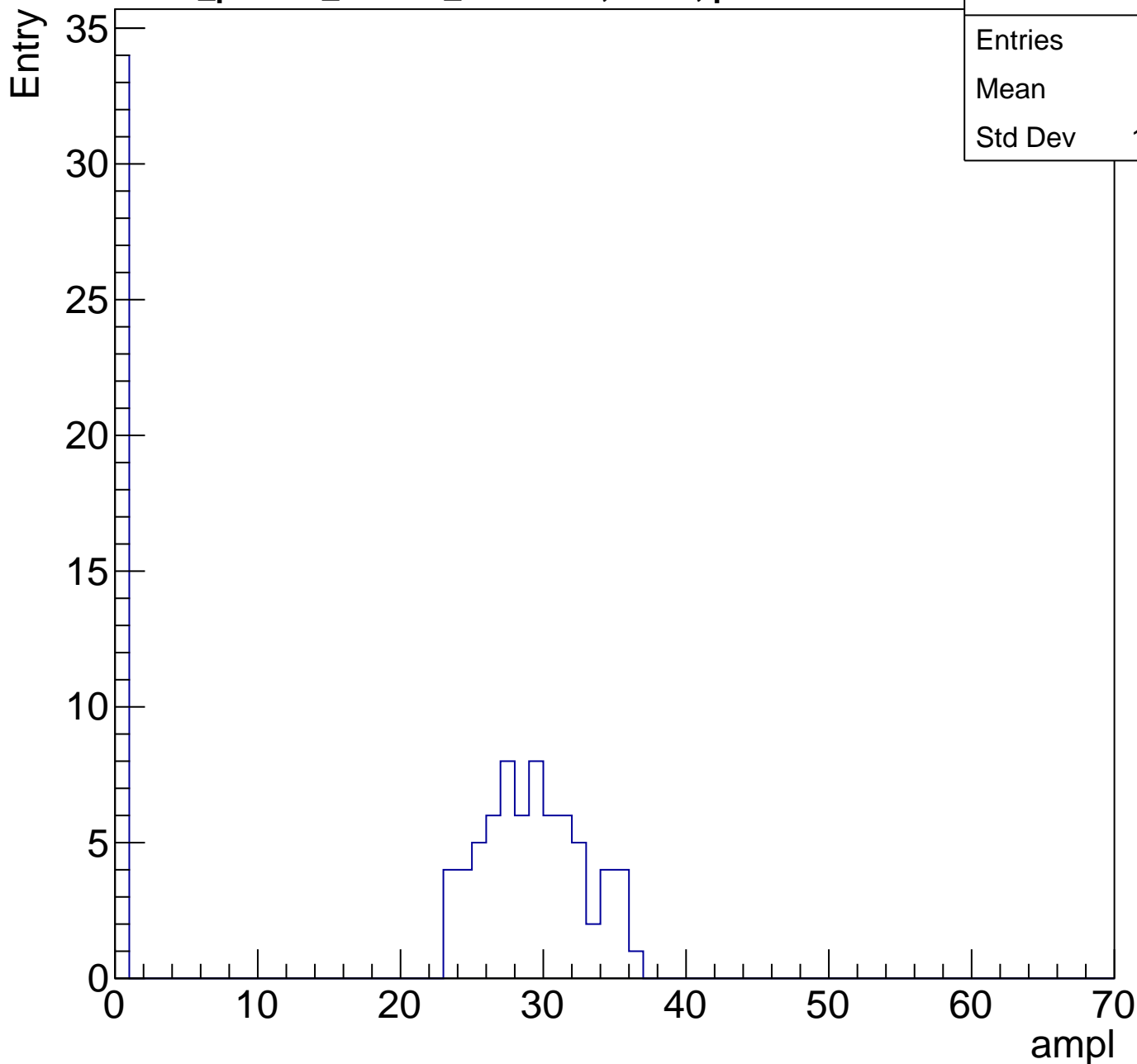
Entry



B1L103S, U23-ch24, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	103
Mean	19.31
Std Dev	13.84

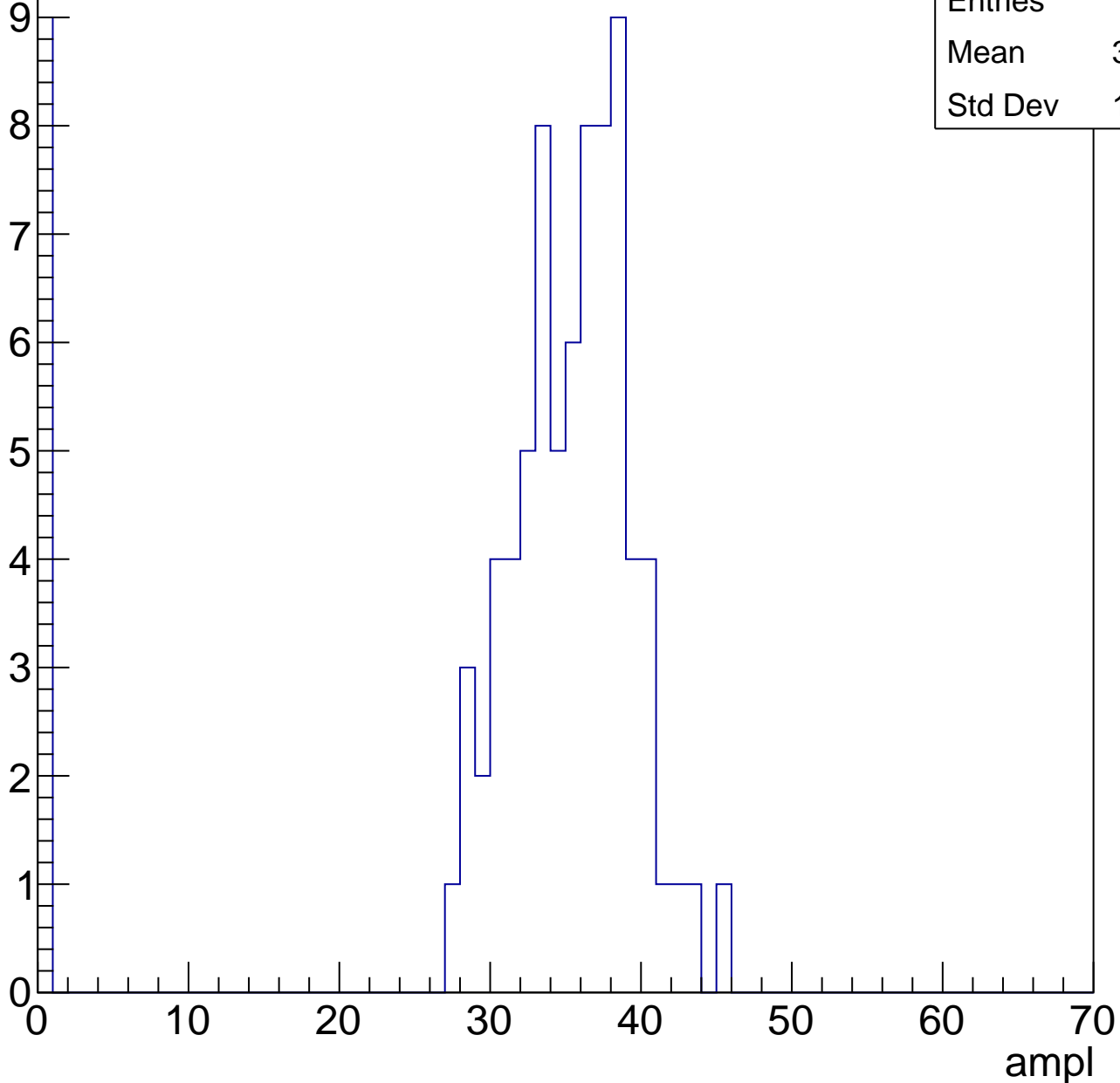


B1L103S, U23-ch24, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	84
Mean	31.31
Std Dev	11.41

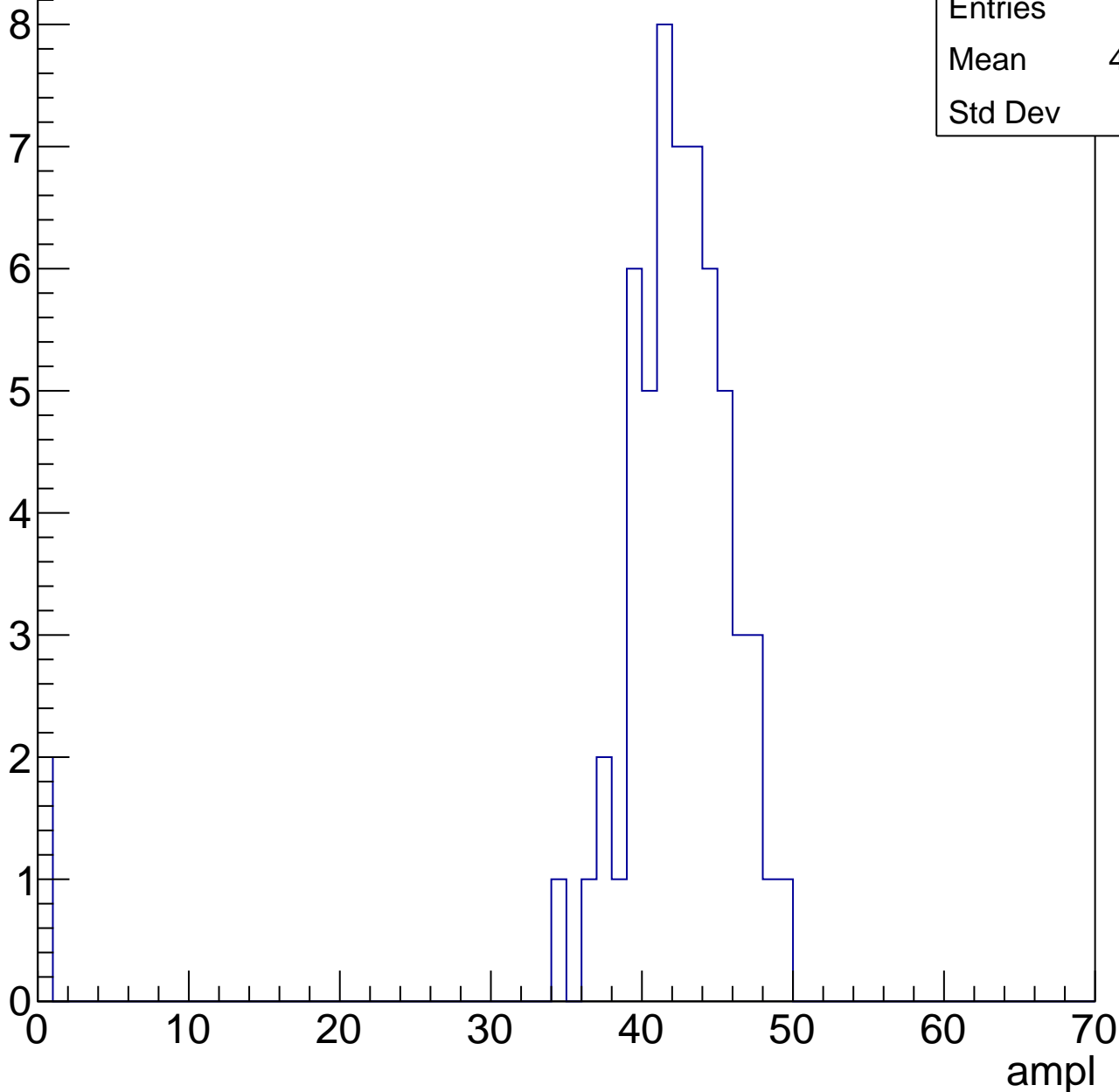


B1L103S, U23-ch24, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	40.75
Std Dev	8.2

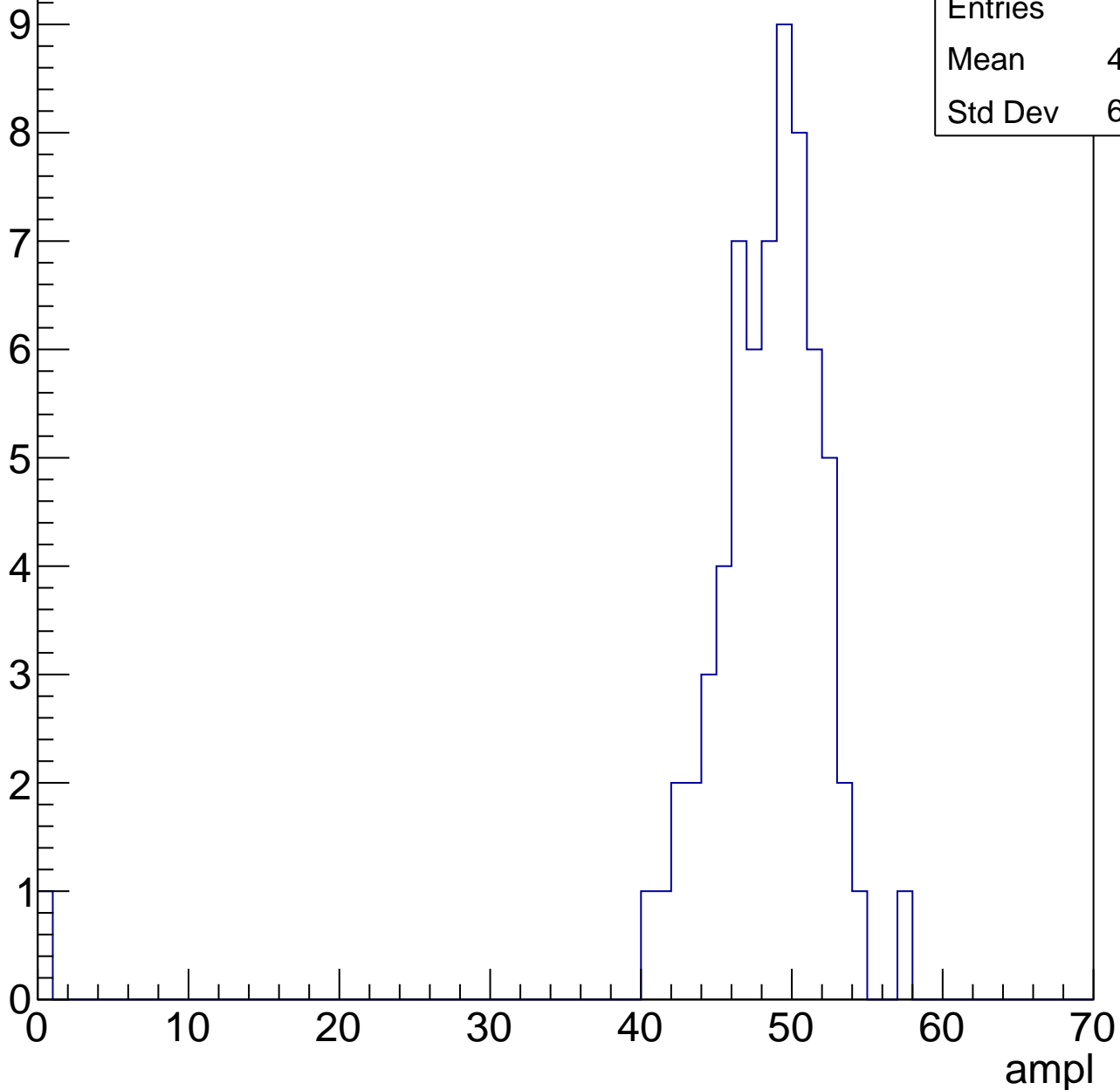


B1L103S, U23-ch24, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	47.38
Std Dev	6.712



B1L103S, U23-ch24, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entries	66
Mean	53.86
Std Dev	7.493

Entry

10

8

6

4

2

0

0

10

20

30

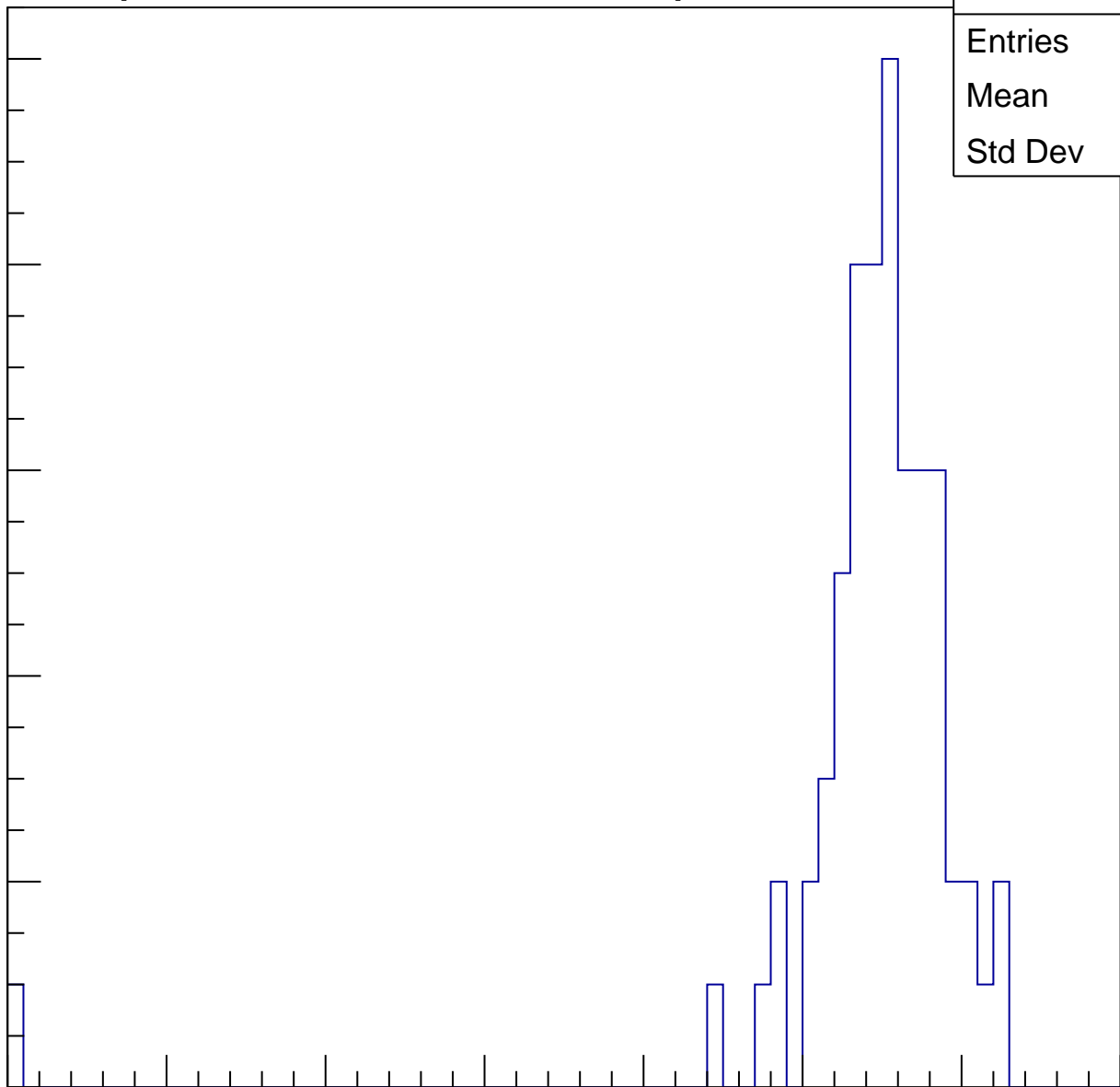
40

50

60

70

ampl

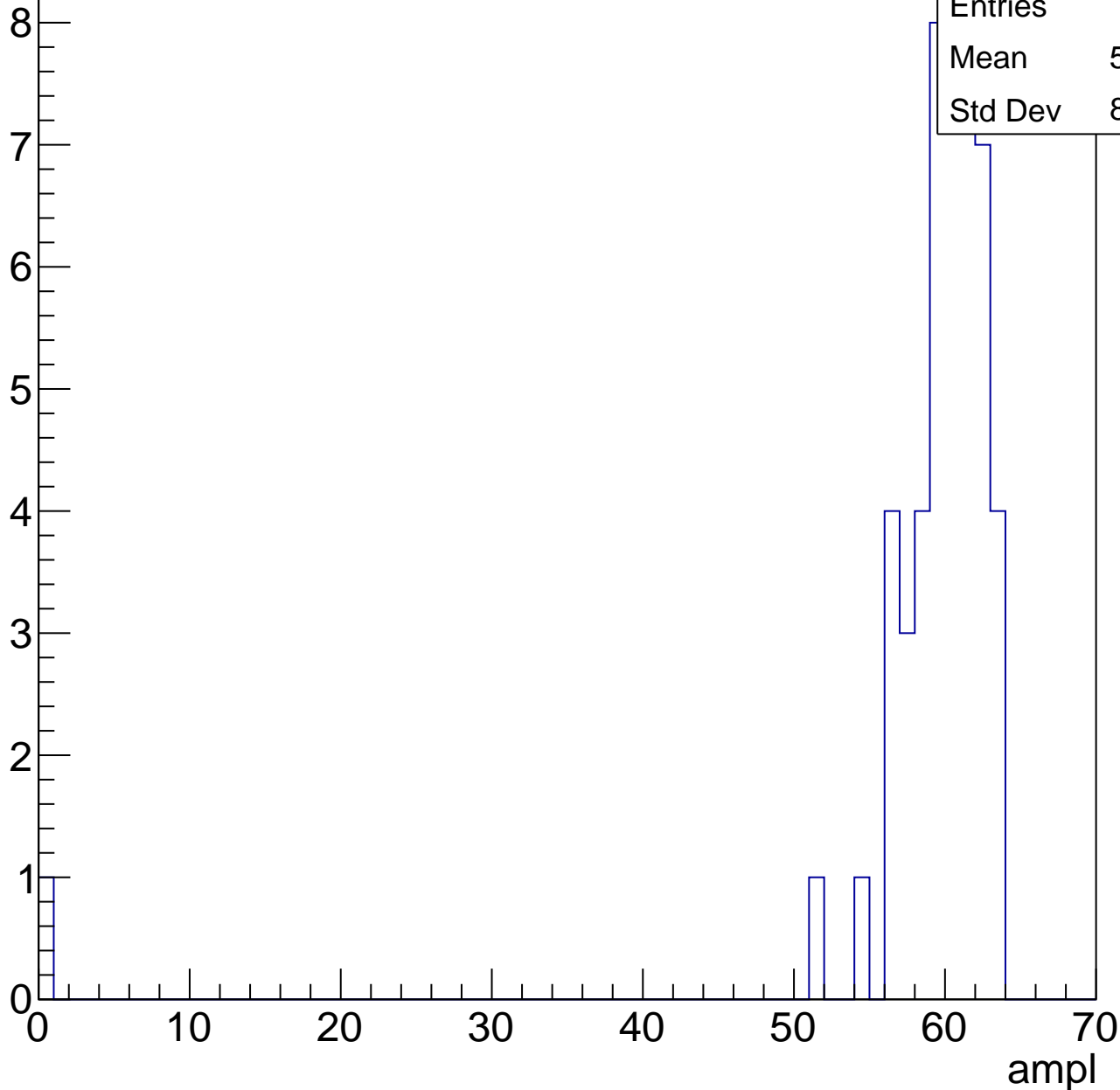


B1L103S, U23-ch24, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	49
Mean	58.33
Std Dev	8.768

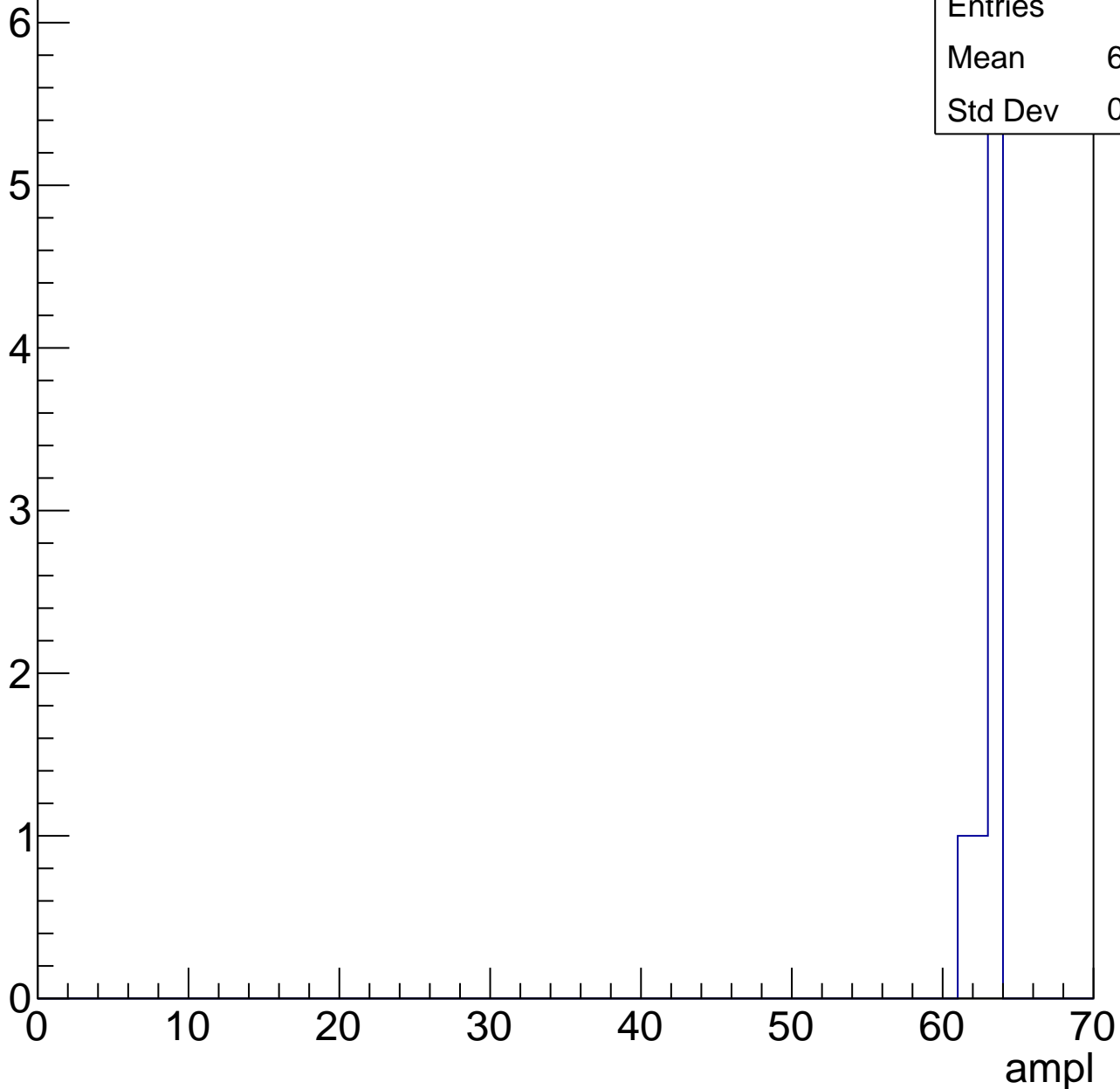


B1L103S, U23-ch24, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	8
Mean	62.62
Std Dev	0.696



B1L103S, U23-ch24, adc7

calib_packv5_041523_1651.root, FC#0, port C2

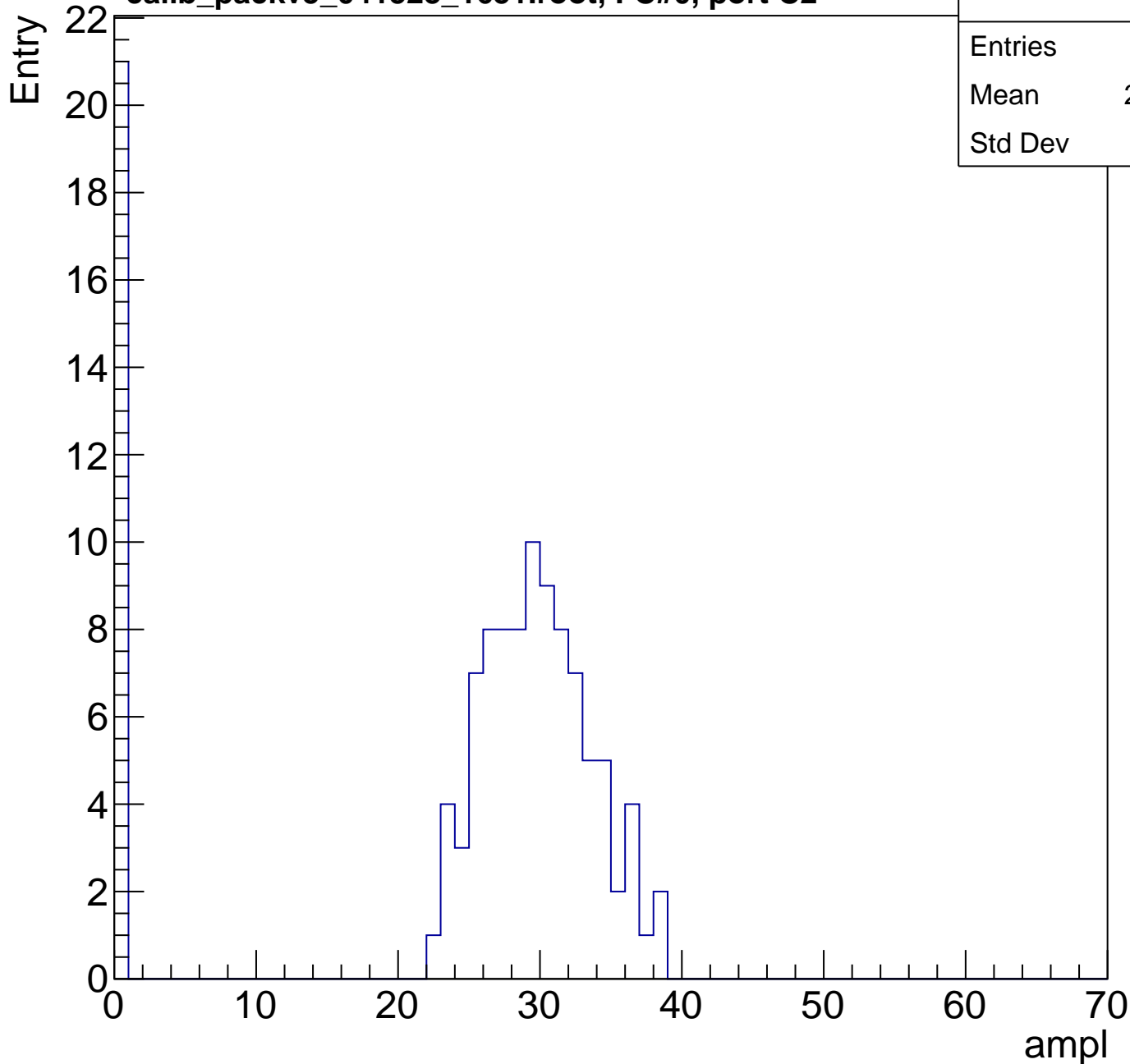
Entry



B1L103S, U23-ch25, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	113
Mean	23.92
Std Dev	11.91

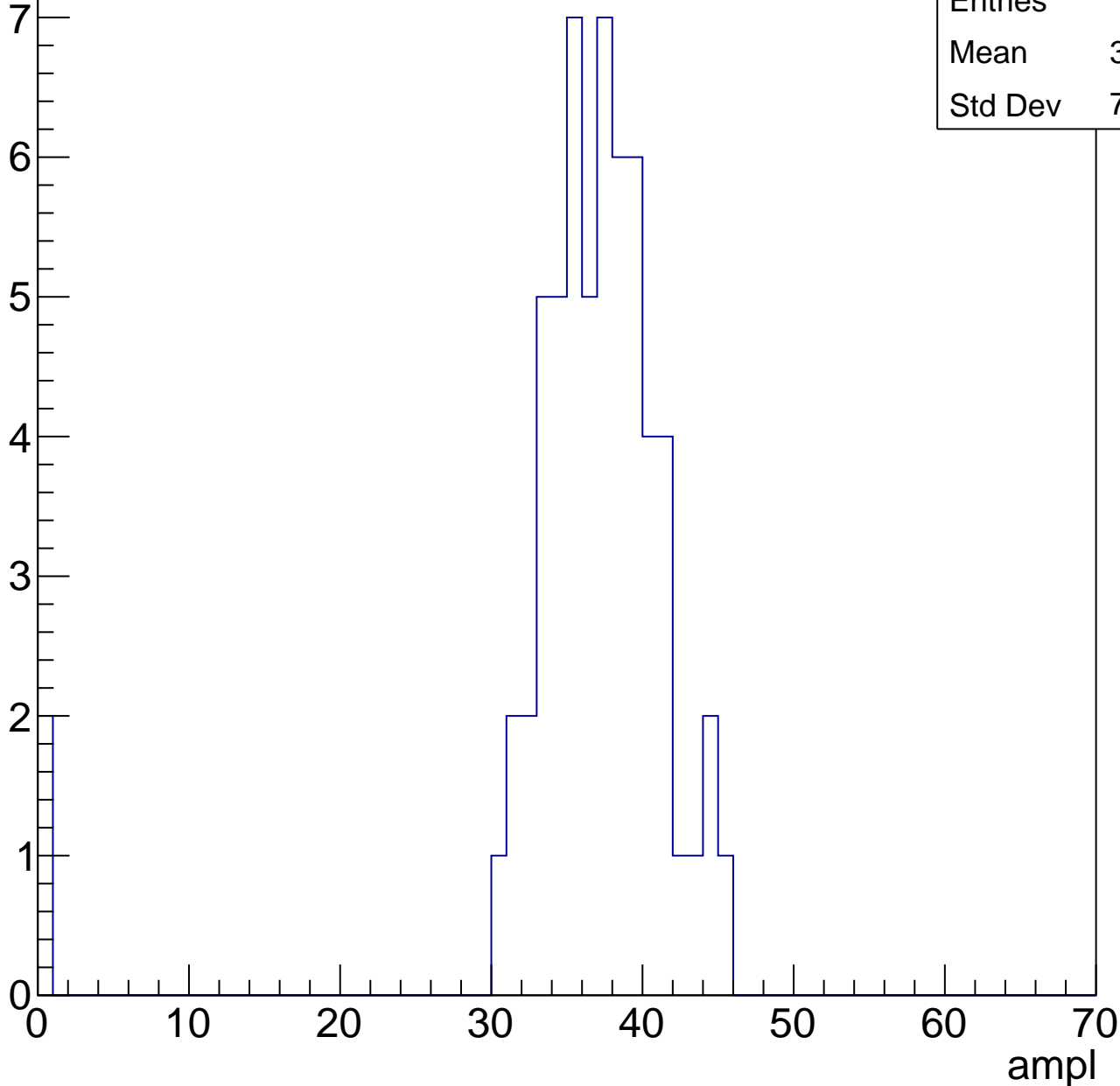


B1L103S, U23-ch25, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	35.72
Std Dev	7.378

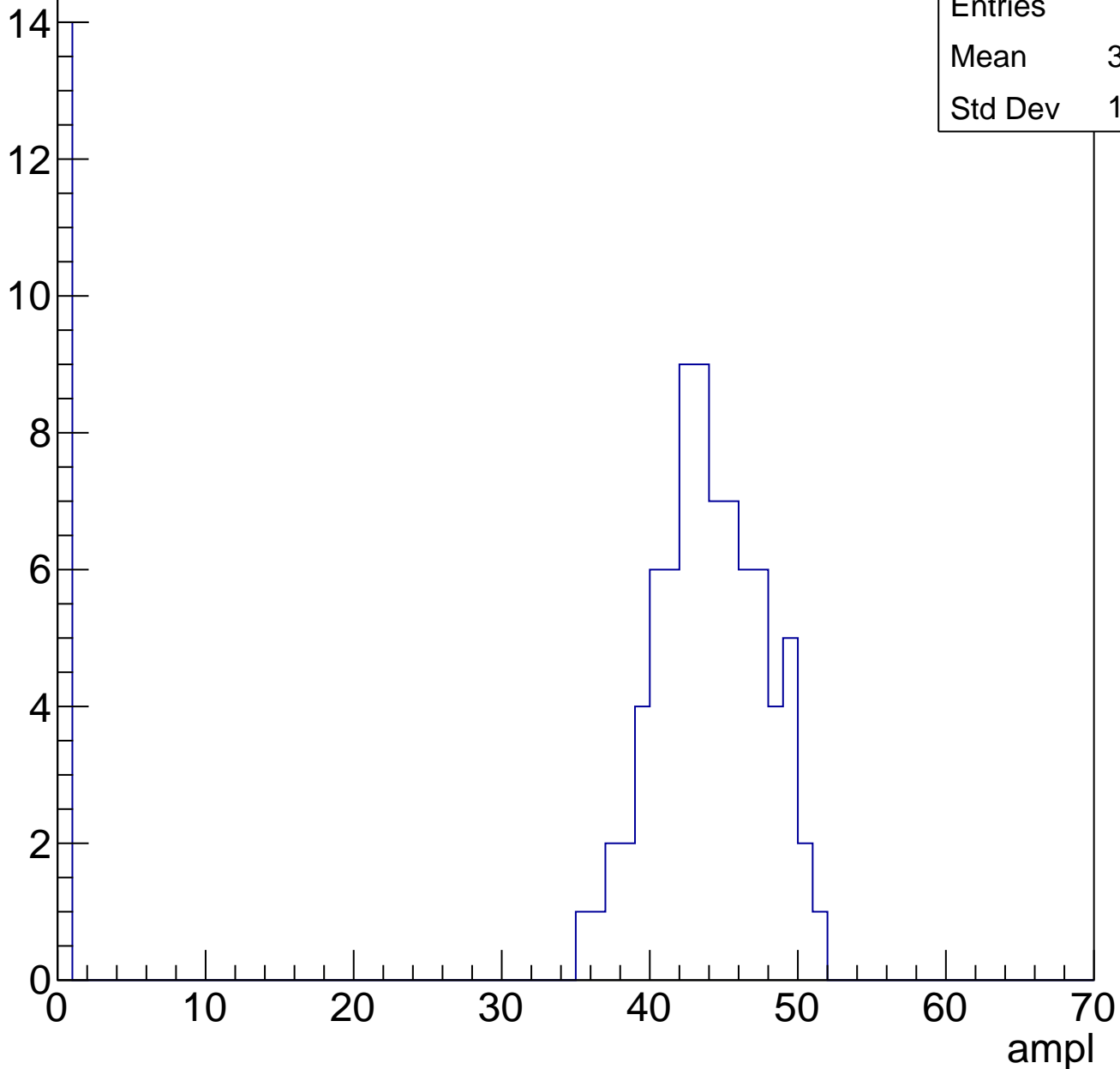


B1L103S, U23-ch25, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	92
Mean	36.92
Std Dev	15.98

Entry

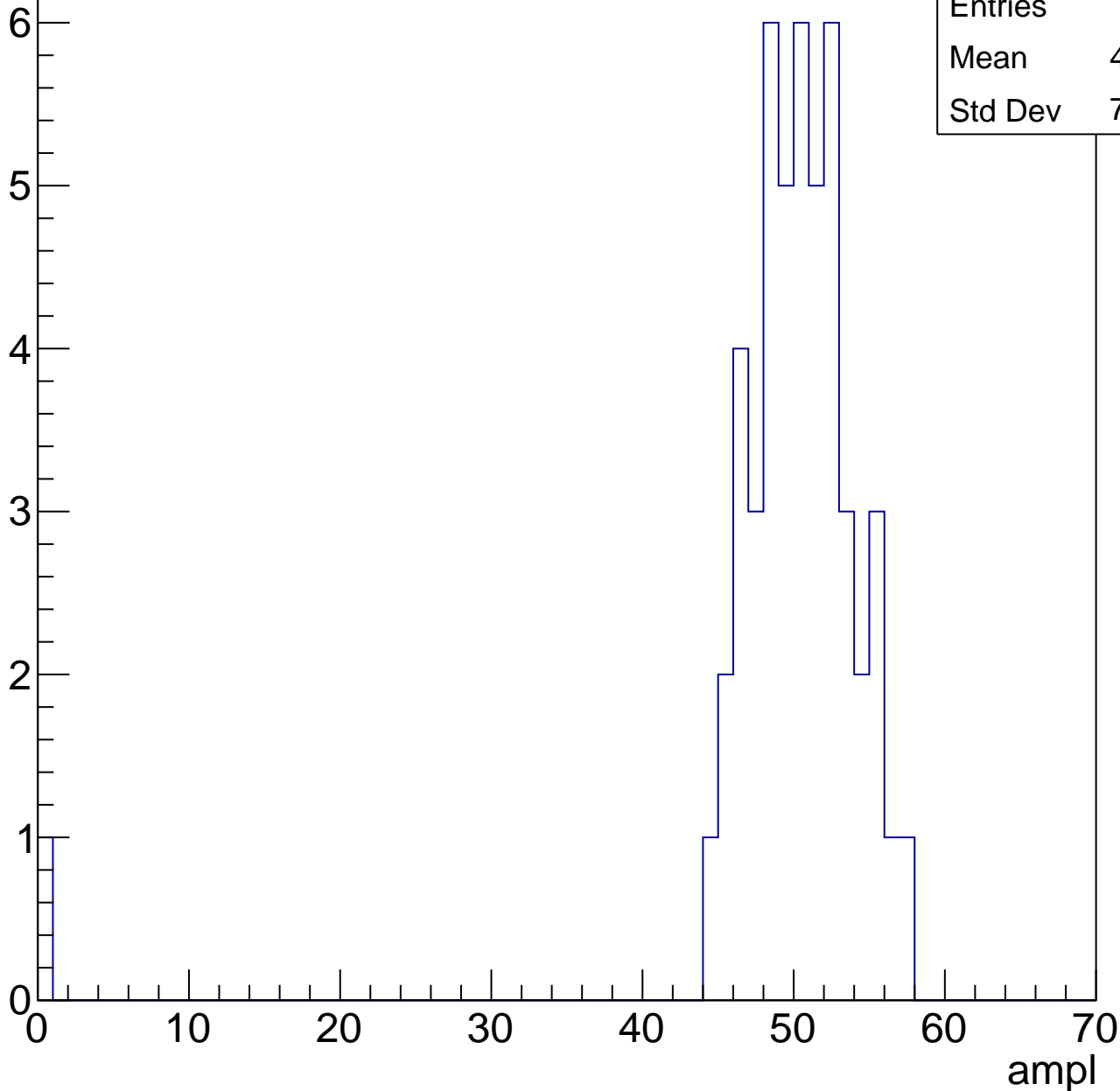


B1L103S, U23-ch25, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	49
Mean	49.06
Std Dev	7.707

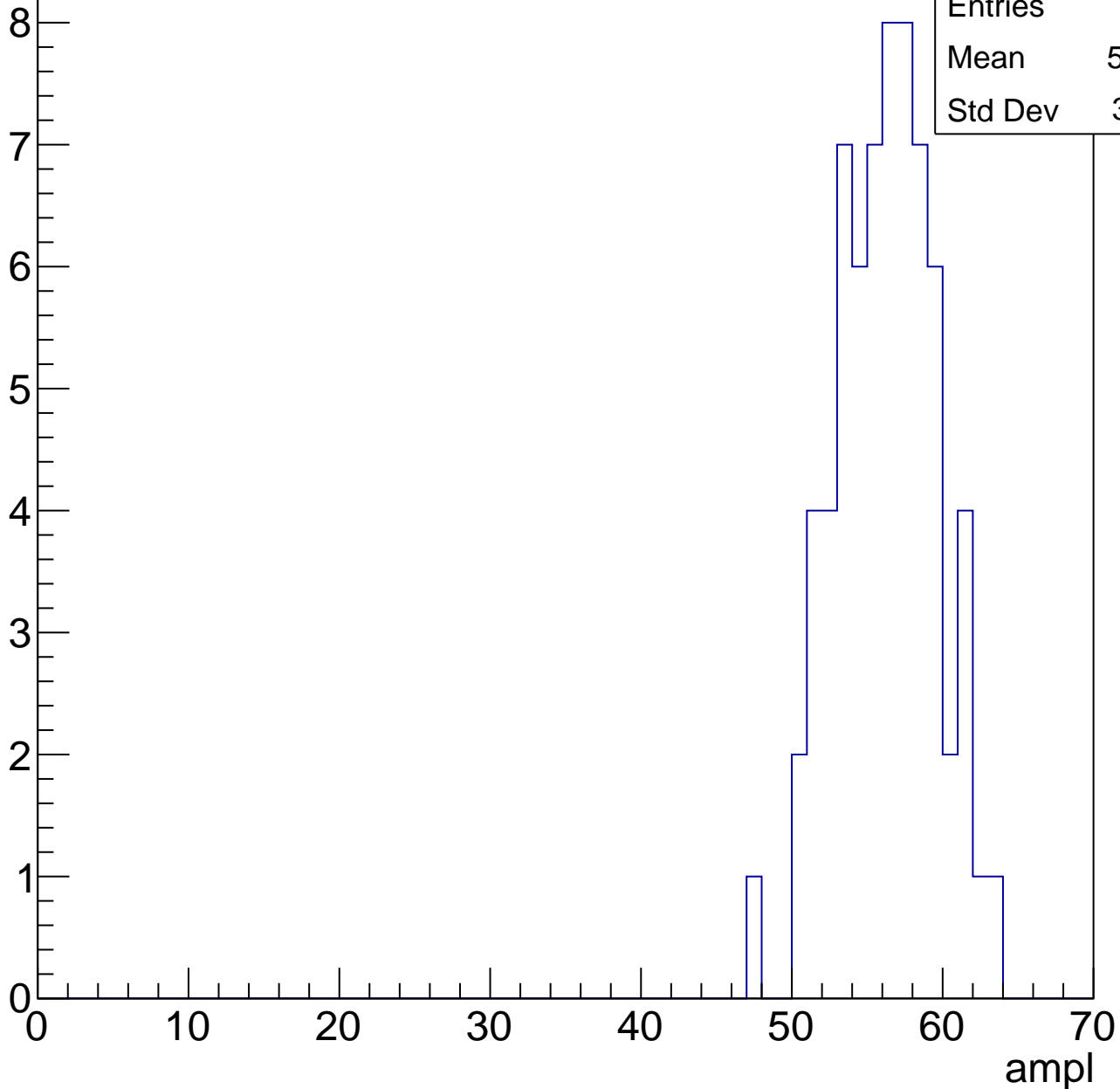


B1L103S, U23-ch25, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	55.76
Std Dev	3.241



B1L103S, U23-ch25, adc5

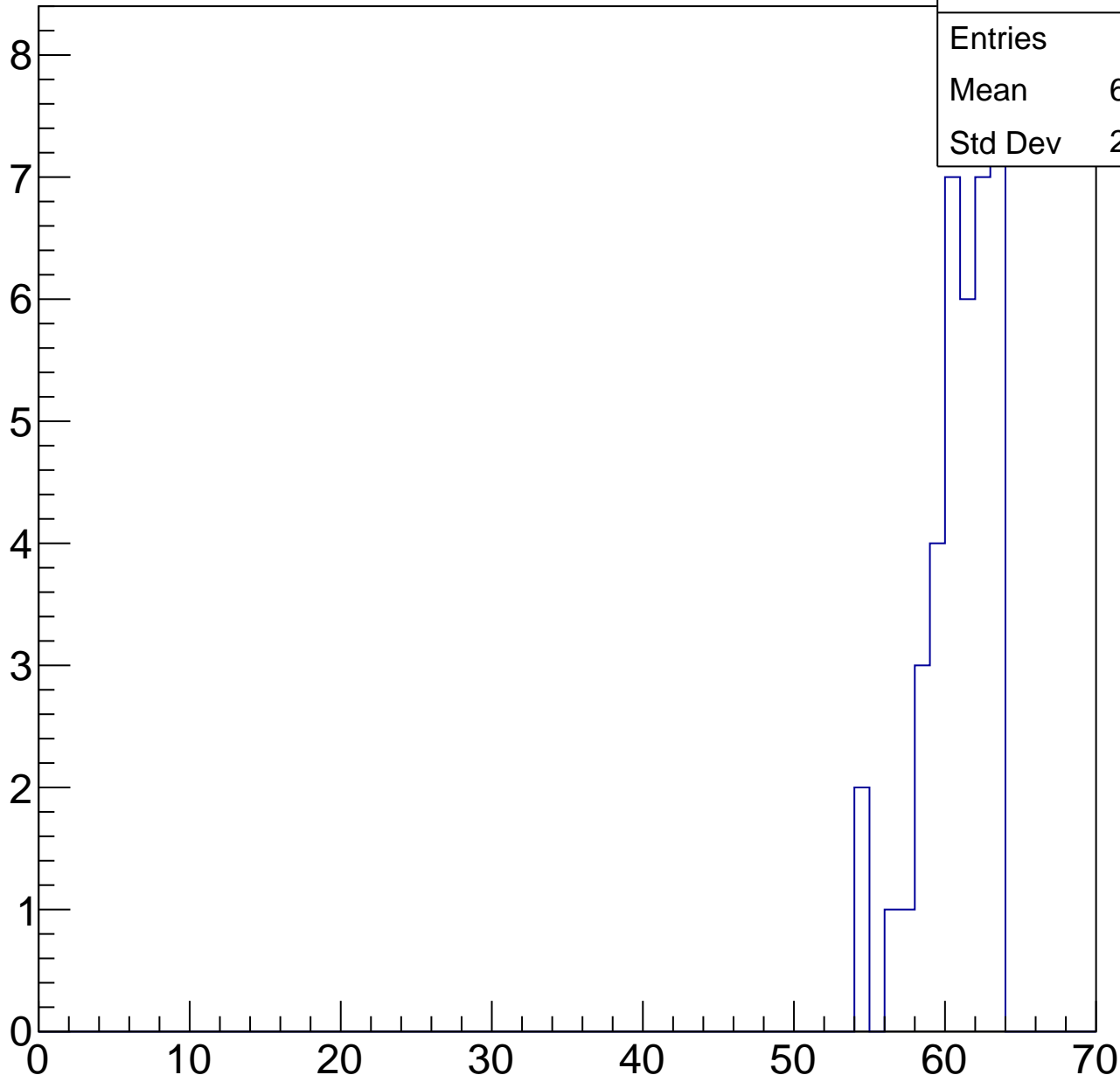
calib_packv5_041523_1651.root, FC#0, port C2

Entry

8
7
6
5
4
3
2
1
0

Entries	39
Mean	60.38
Std Dev	2.338

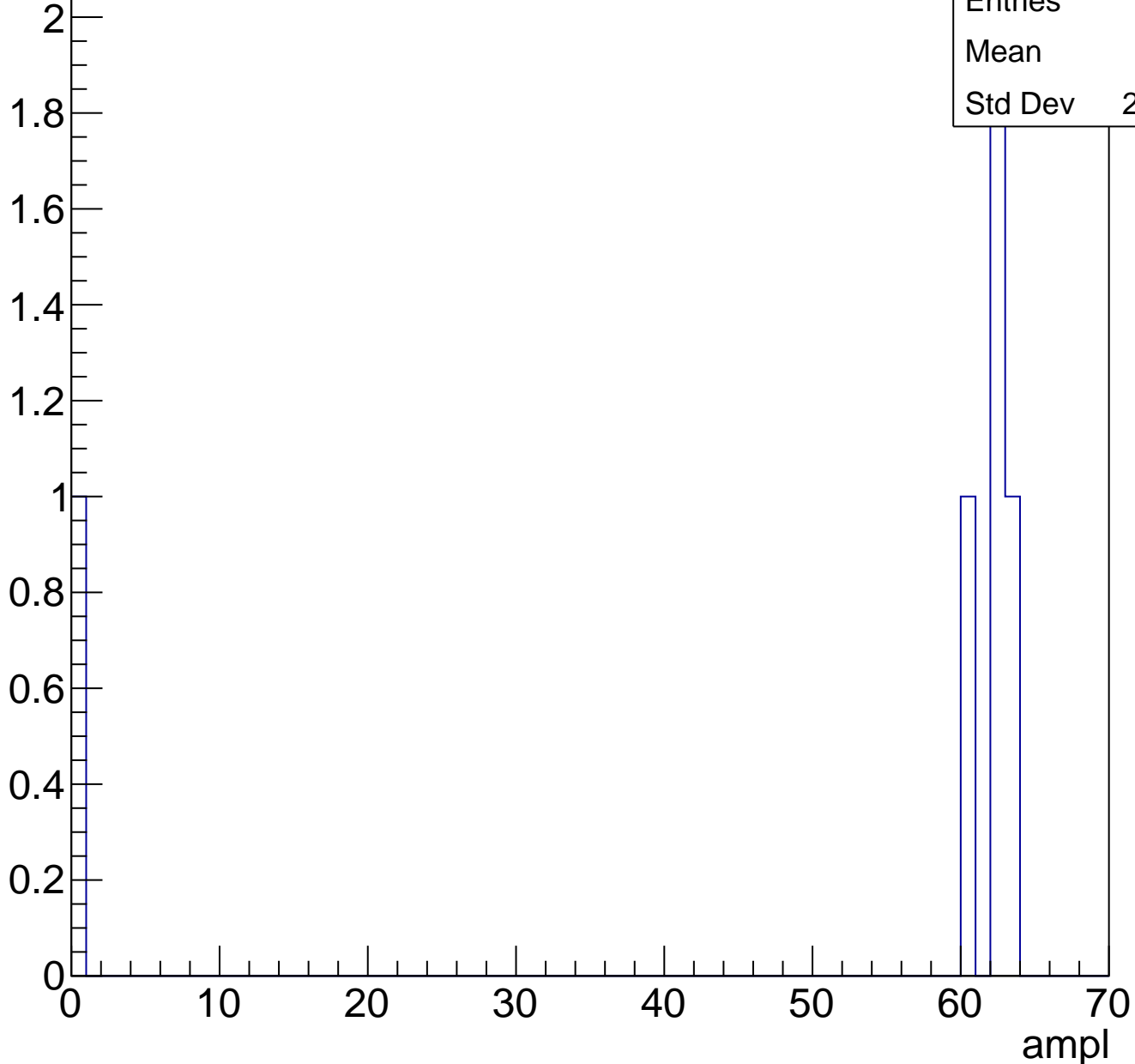
ampl



B1L103S, U23-ch25, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	5
Mean	49.4
Std Dev	24.72

B1L103S, U23-ch25, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

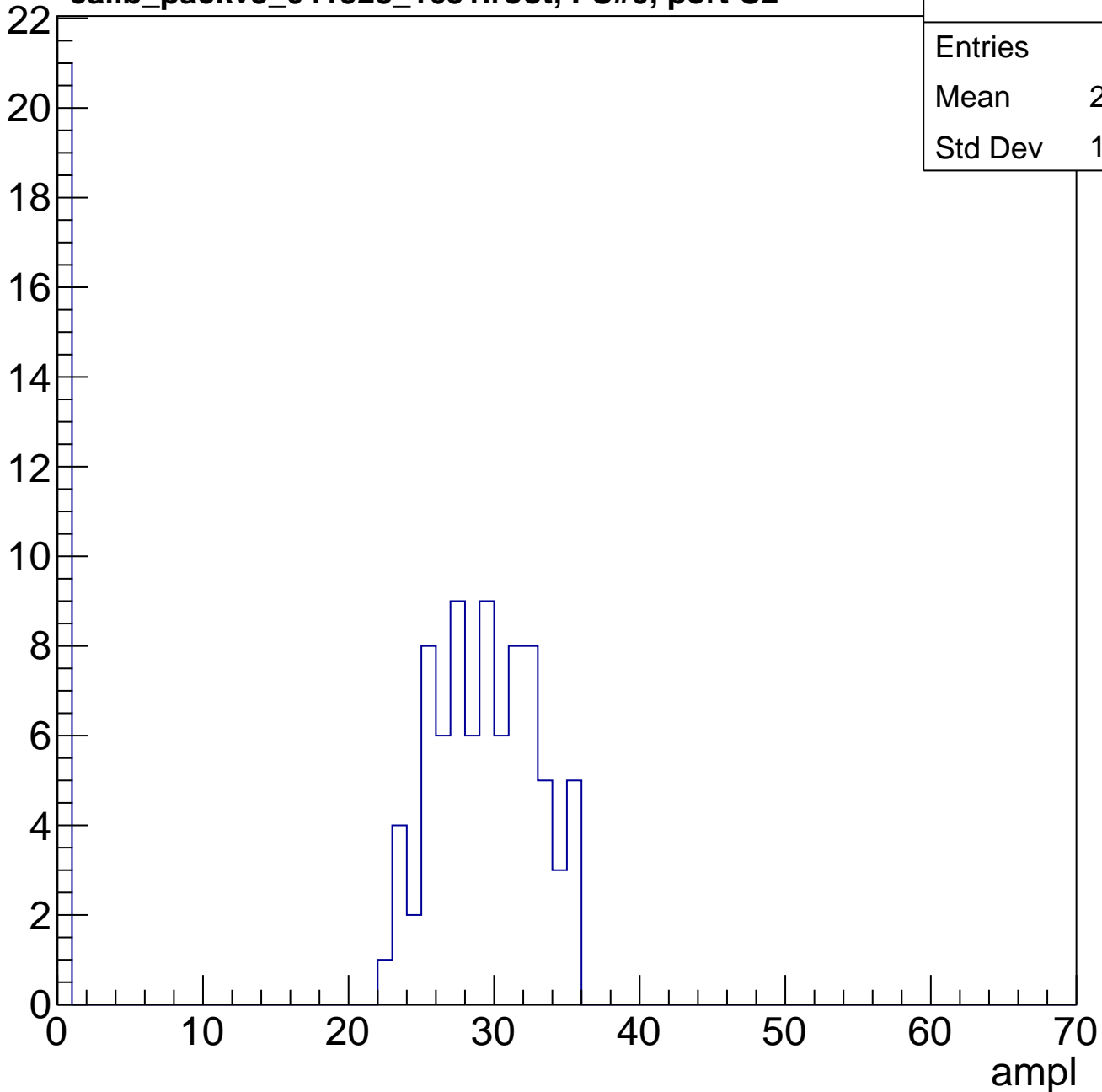
ampl

B1L103S, U23-ch26, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	101
Mean	22.93
Std Dev	12.13

Entry

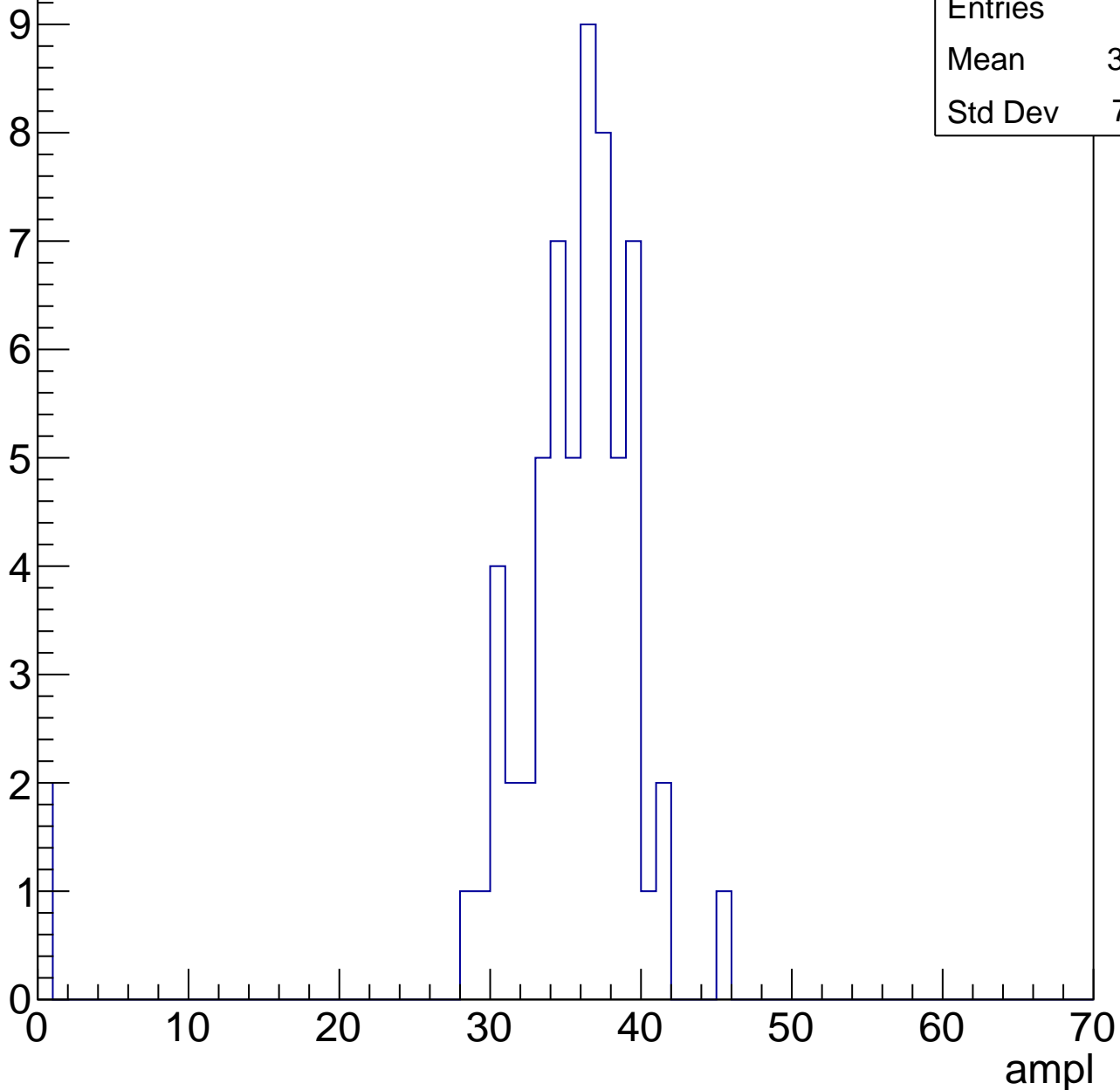


B1L103S, U23-ch26, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	34.37
Std Dev	7.051



B1L103S, U23-ch26, adc2

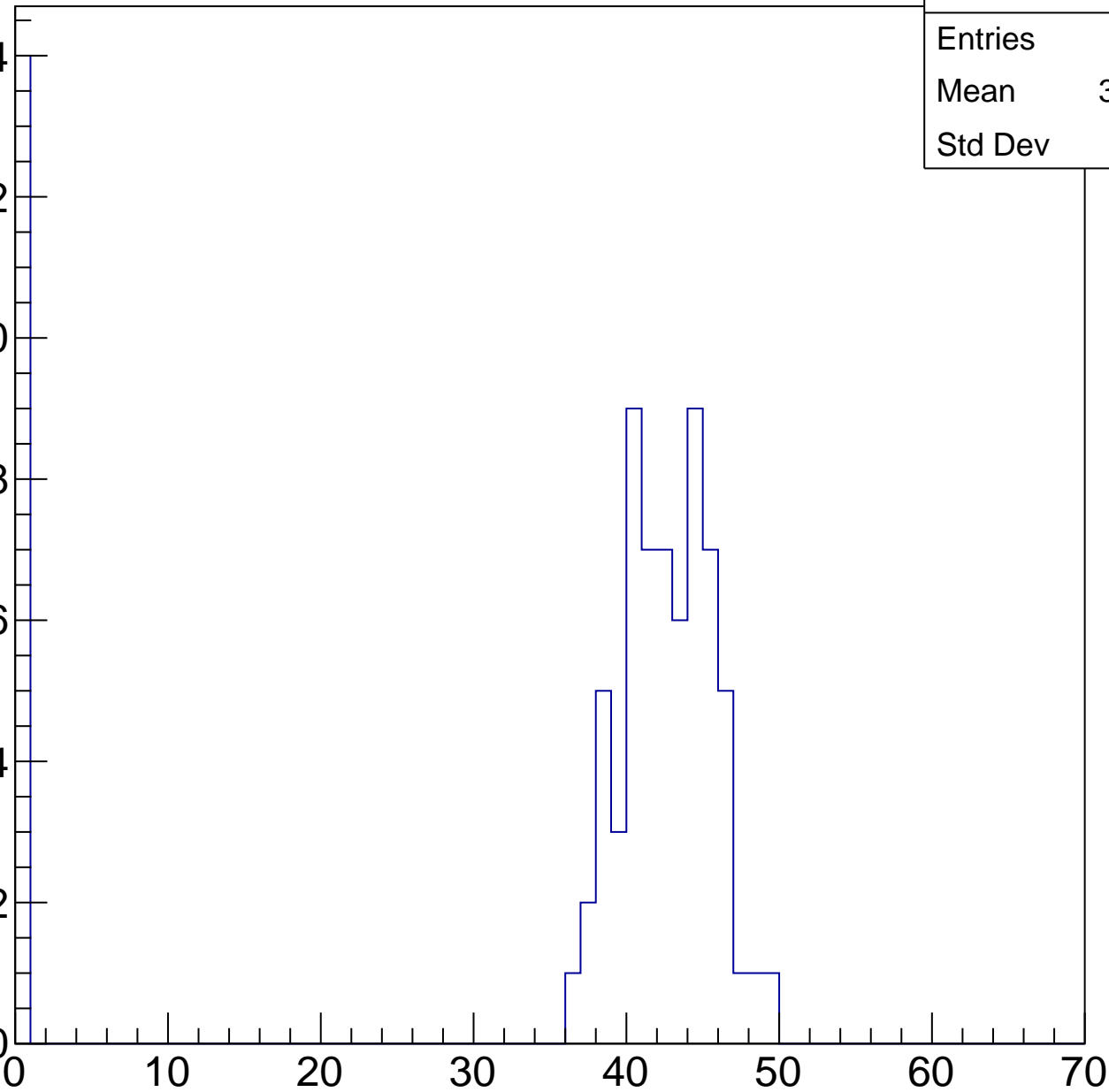
calib_packv5_041523_1651.root, FC#0, port C2

Entries	78
Mean	34.63
Std Dev	16.4

Entry

14
12
10
8
6
4
2
0

ampl

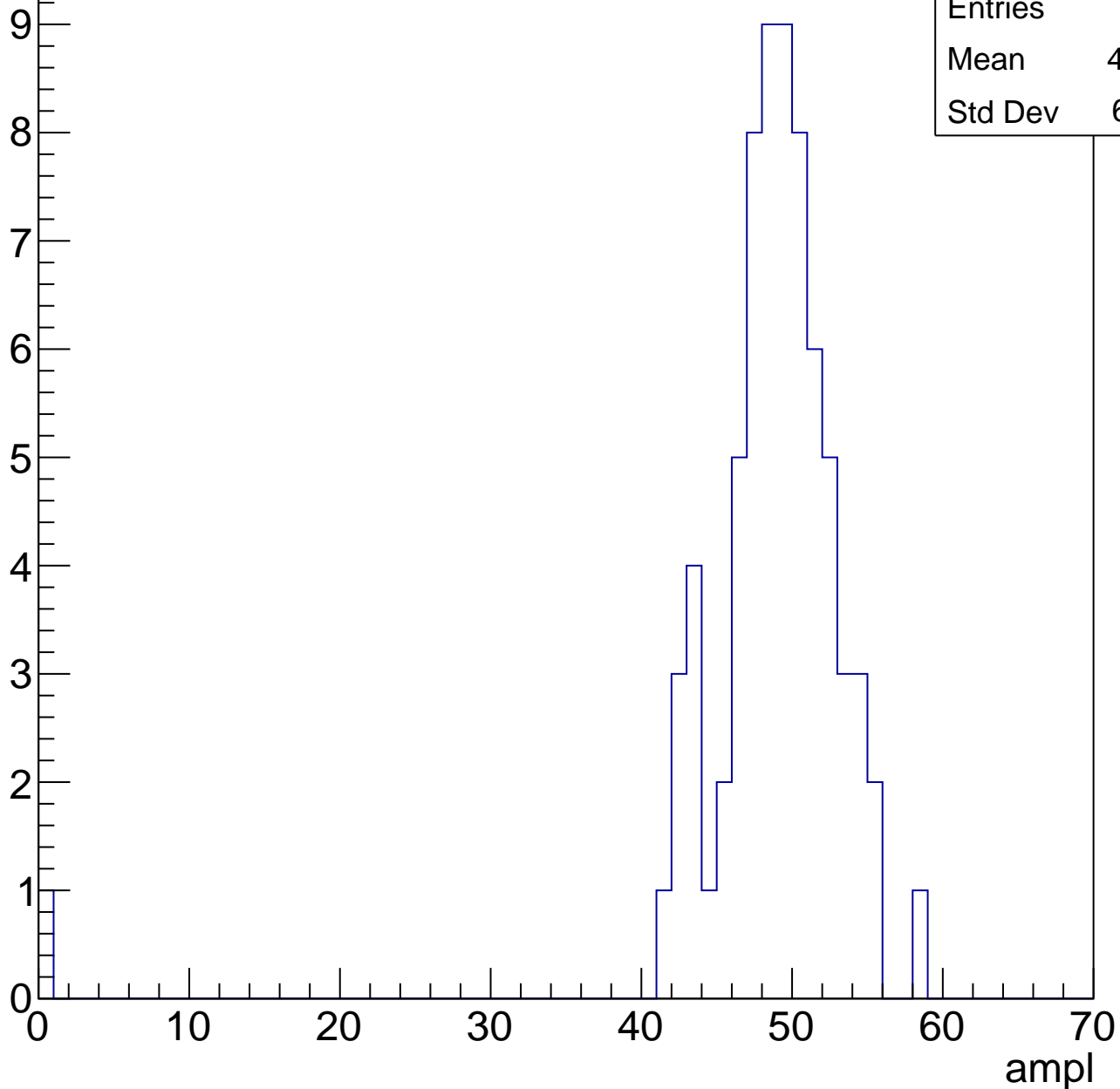


B1L103S, U23-ch26, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	47.99
Std Dev	6.691



B1L103S, U23-ch26, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

7

6

5

4

3

2

1

0

0

10

20

30

40

50

60

70

ampl

Entries 63

Mean 55.38

Std Dev 3.083

0

1

2

3

4

5

6

7

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9

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11

12

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304

305

306

307

308

309

310

311

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321

322

323

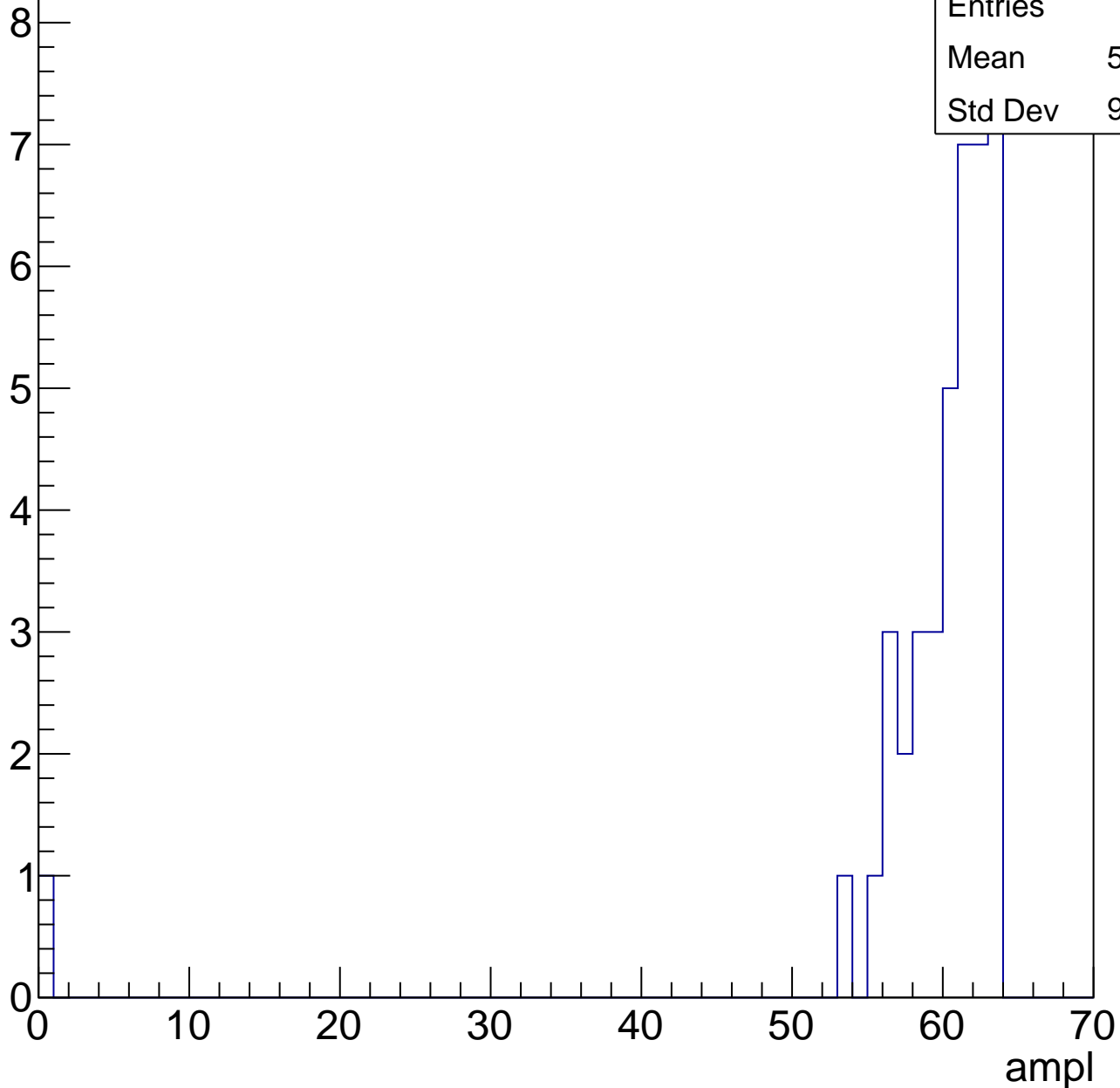
324

B1L103S, U23-ch26, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	41
Mean	58.68
Std Dev	9.616



B1L103S, U23-ch26, adc6

calib_packv5_041523_1651.root, FC#0, port C2

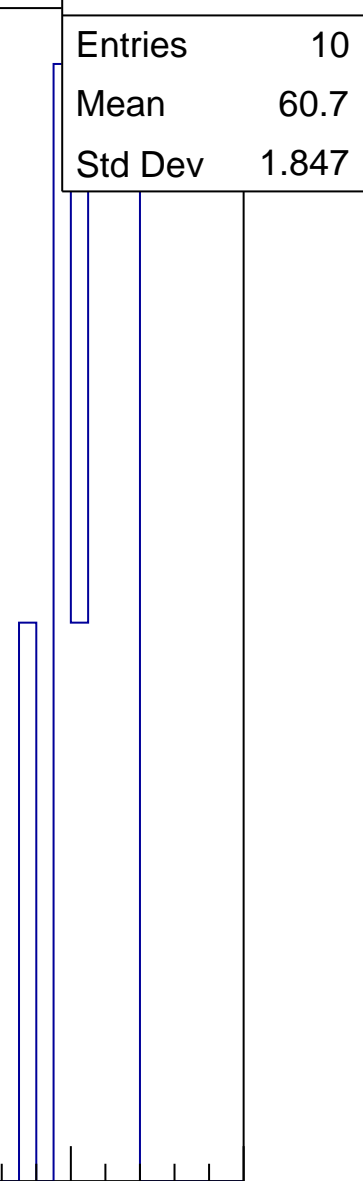
Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	10
Mean	60.7
Std Dev	1.847

0 10 20 30 40 50 60 70

ampl



B1L103S, U23-ch26, adc7

calib_packv5_041523_1651.root, FC#0, port C2

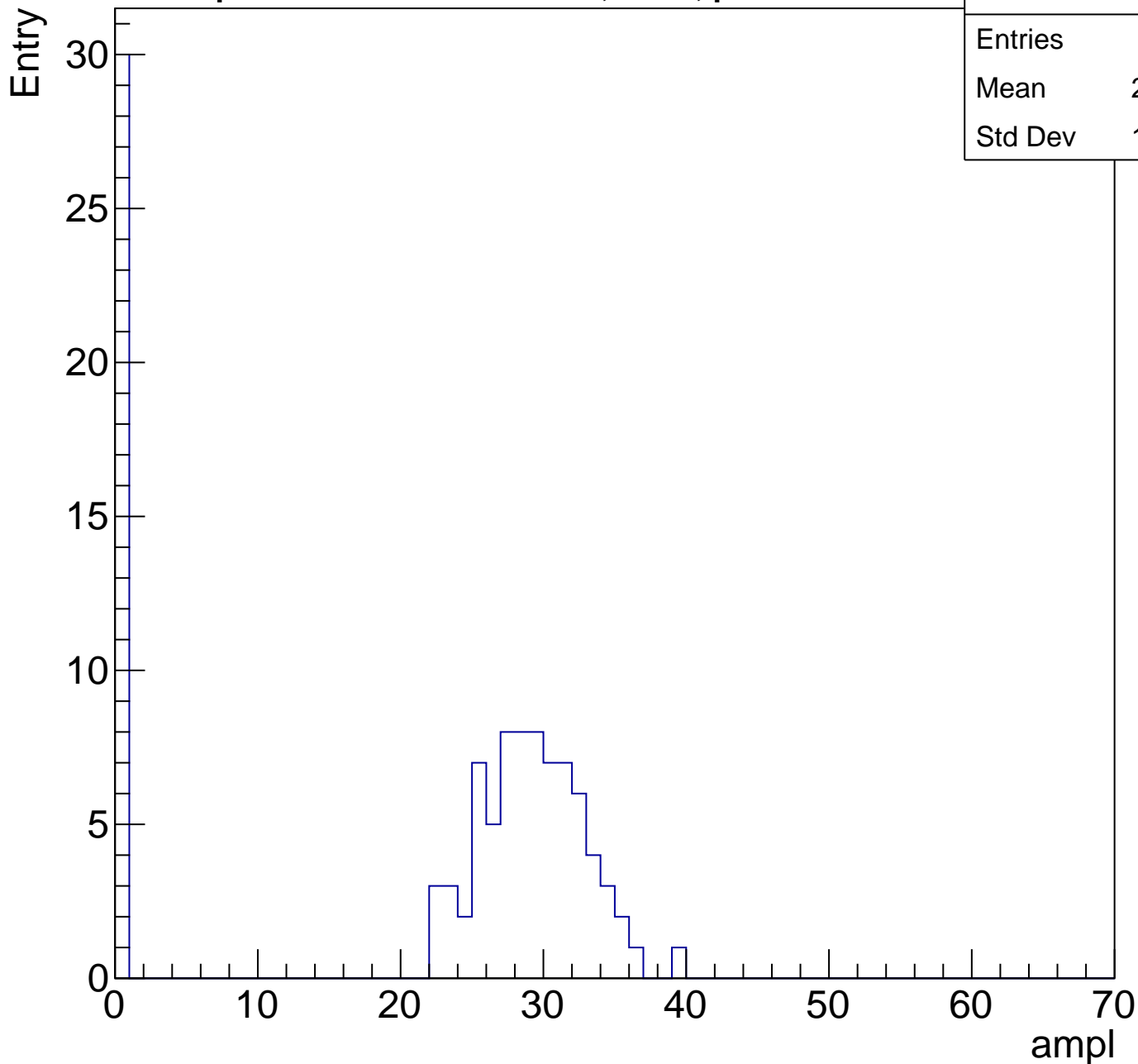
Entry



B1L103S, U23-ch27, adc0

calib_packv5_041523_1651.root, FC#0, port C2

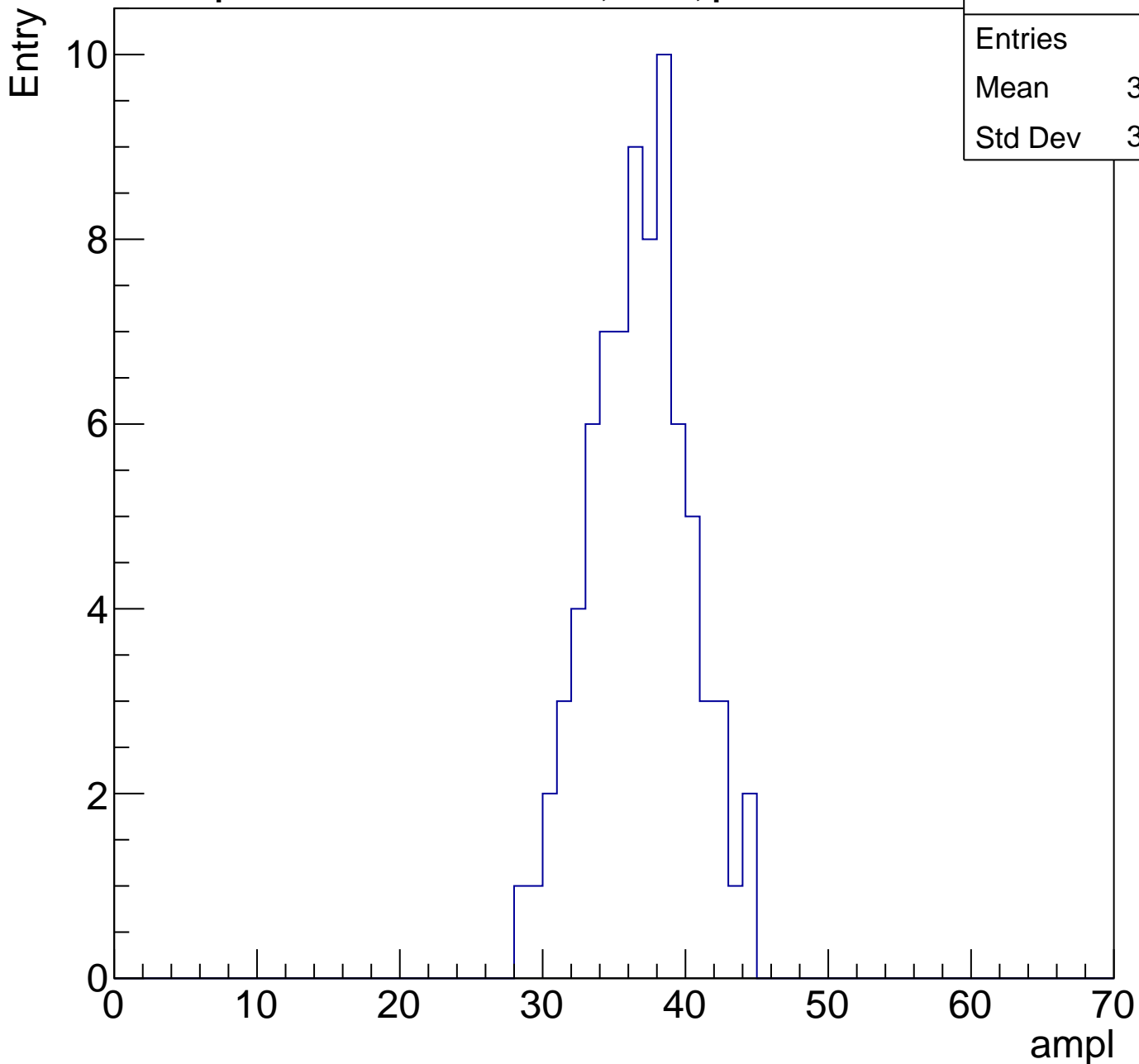
Entries	105
Mean	20.55
Std Dev	13.34



B1L103S, U23-ch27, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	78
Mean	36.32
Std Dev	3.484



B1L103S, U23-ch27, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

12

10

8

6

4

2

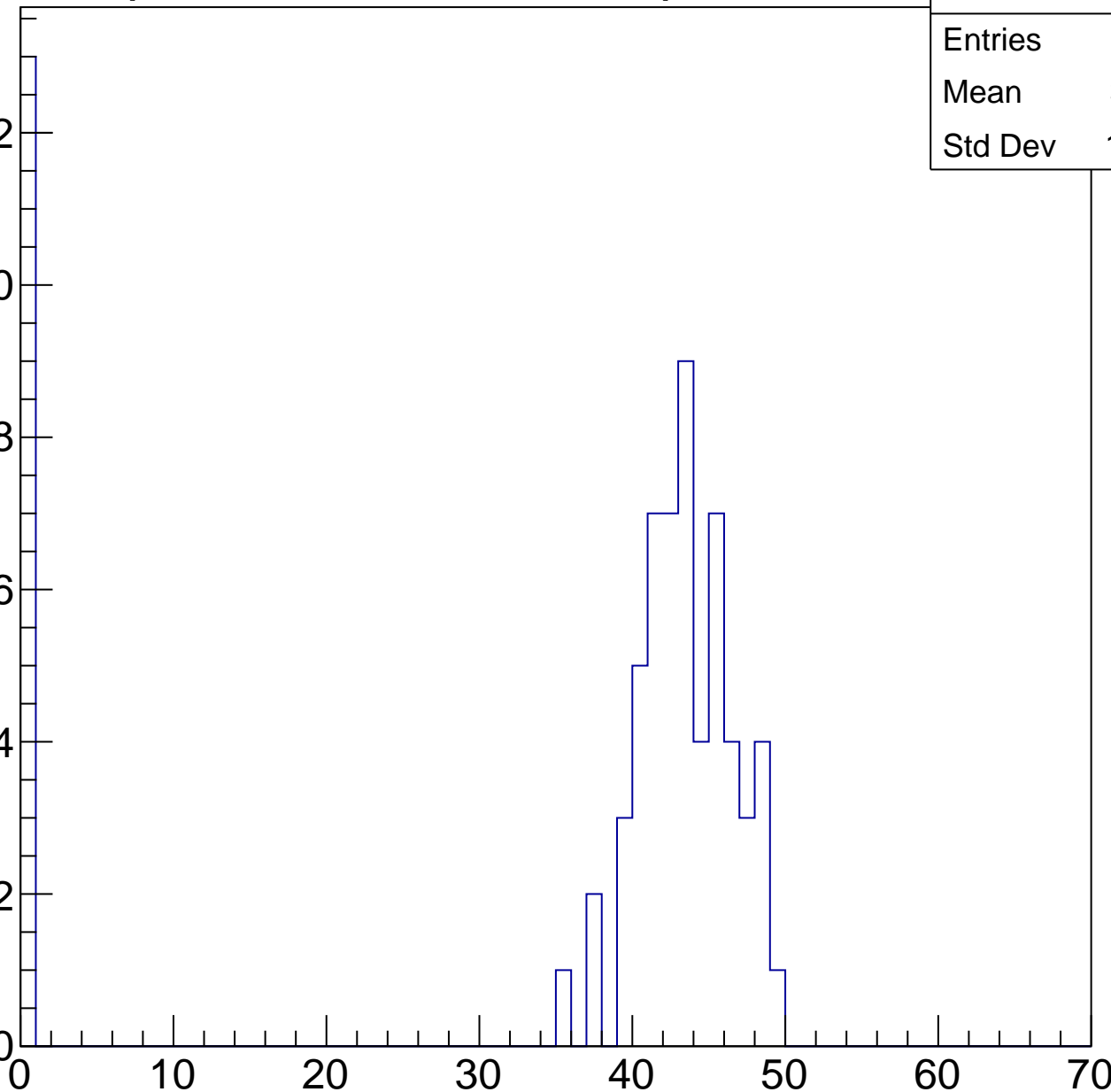
0

Entries 70

Mean 35.01

Std Dev 16.94

ampl

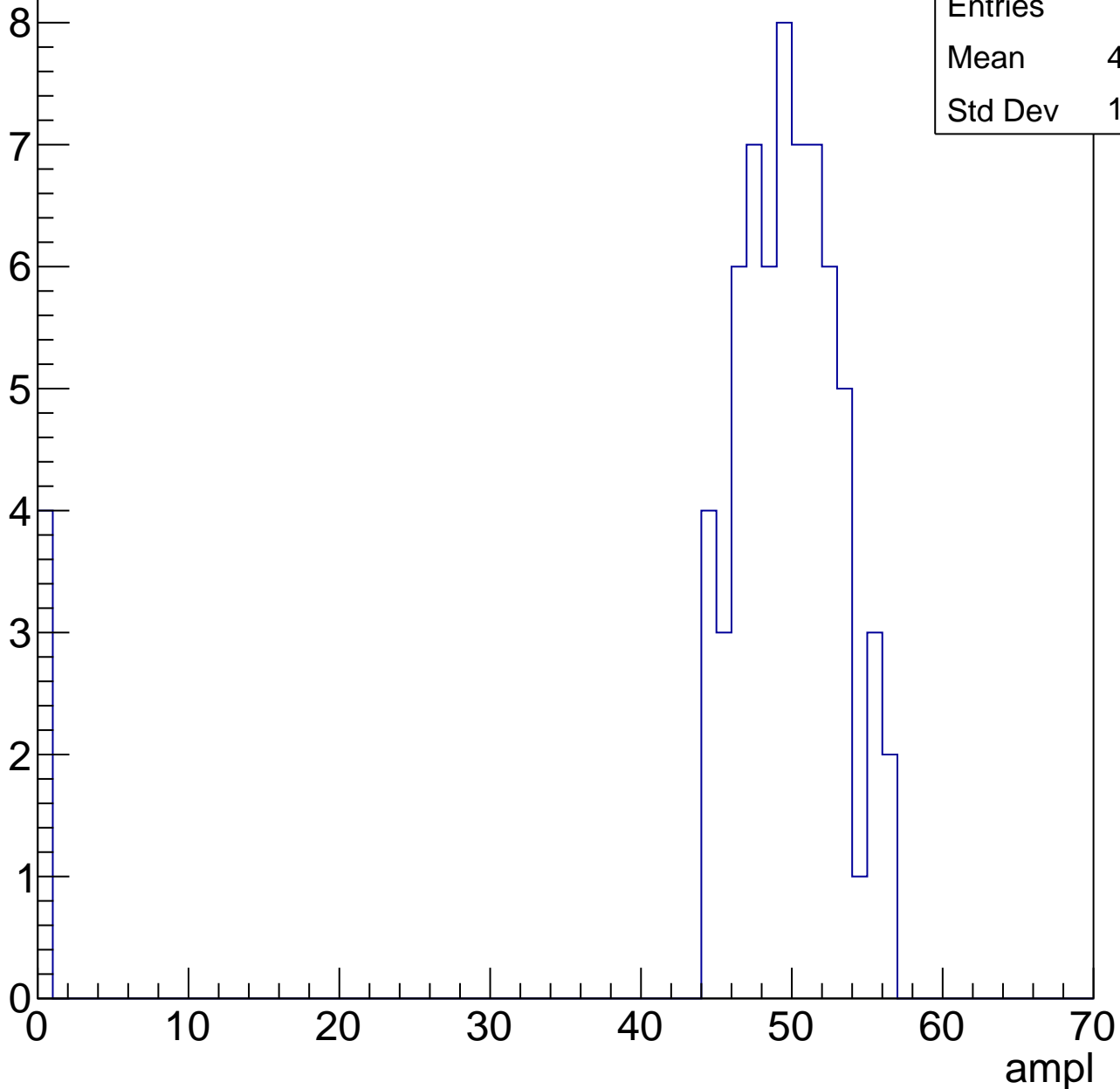


B1L103S, U23-ch27, adc3

calib_packv5_041523_1651.root, FC#0, port C2

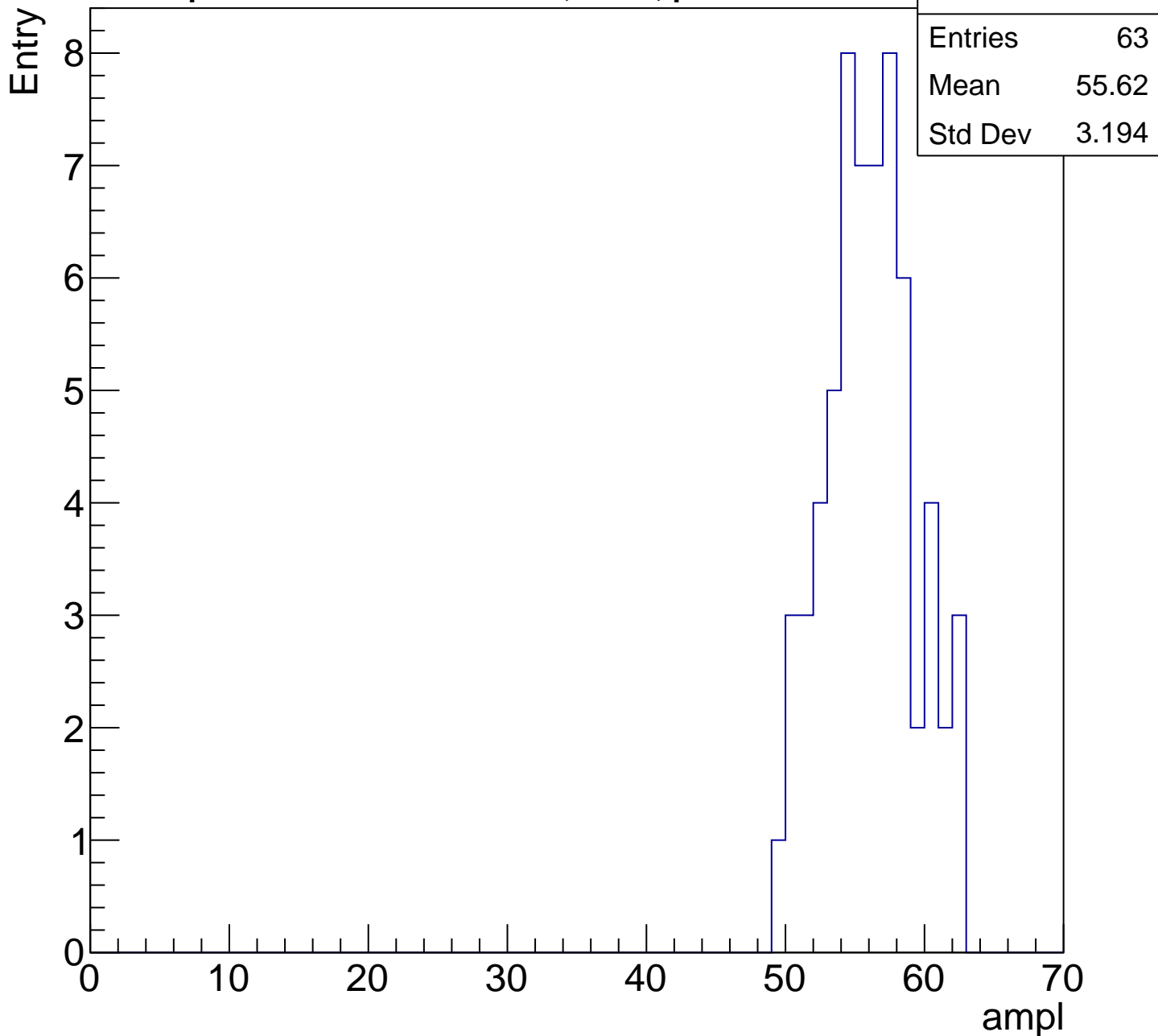
Entry

Entries	69
Mean	46.54
Std Dev	11.93



B1L103S, U23-ch27, adc4

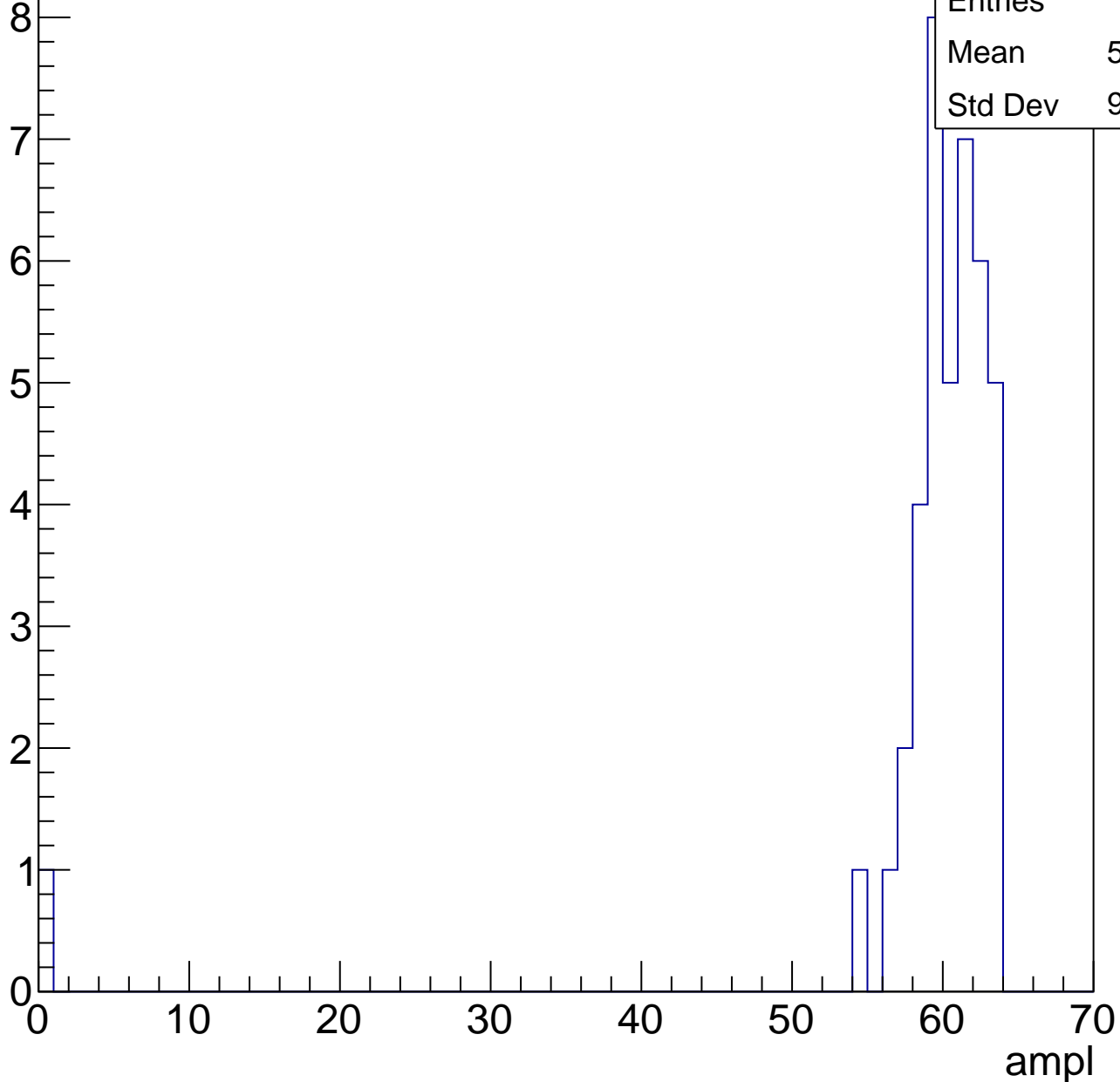
calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U23-ch27, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

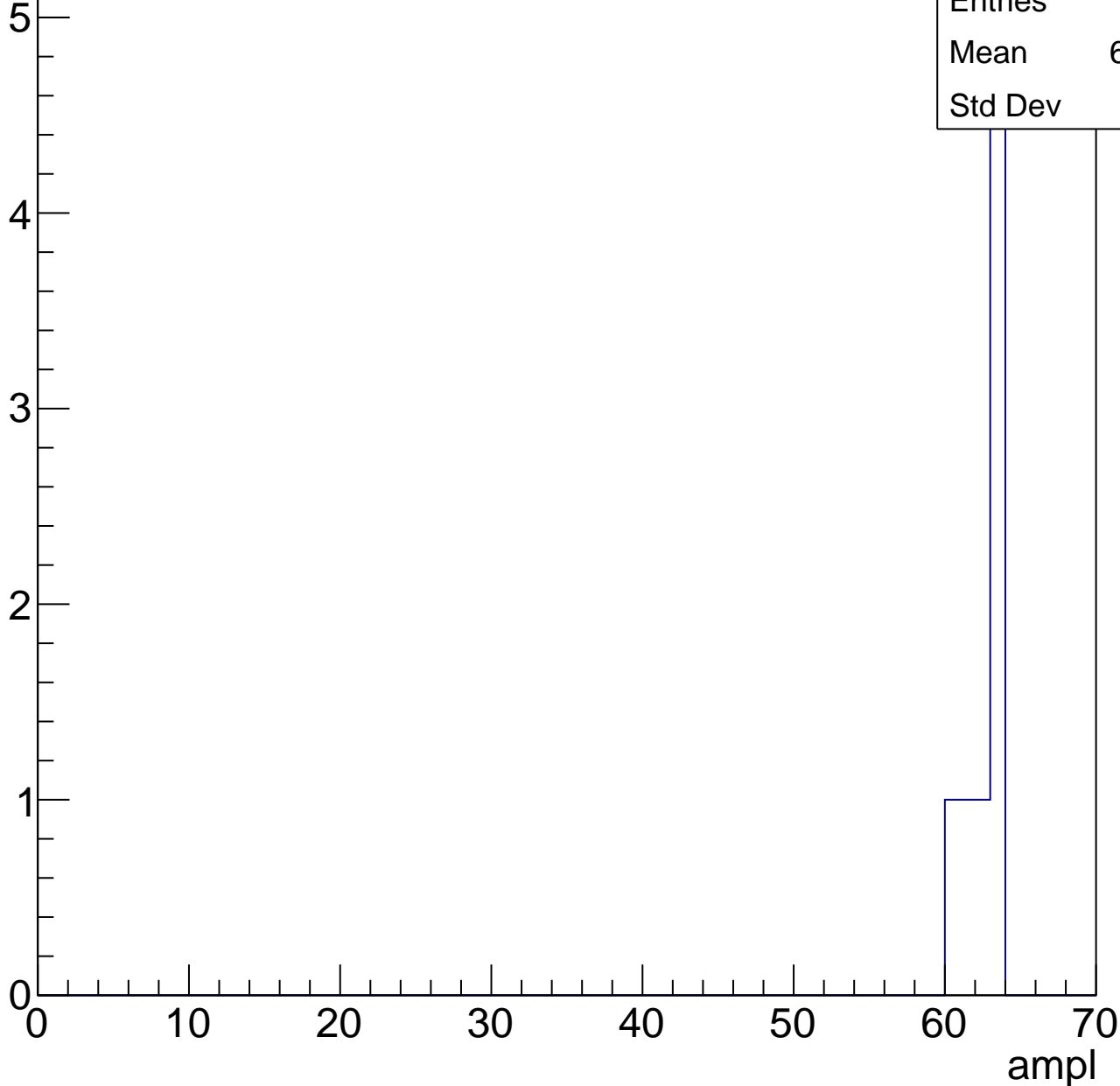


B1L103S, U23-ch27, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	8
Mean	62.25
Std Dev	1.09



B1L103S, U23-ch27, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	19
Mean	0
Std Dev	0

B1L103S, U23-ch28, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	97
Mean	19.21
Std Dev	12.65

Entry

25

20

15

10

5

0

0

10

20

30

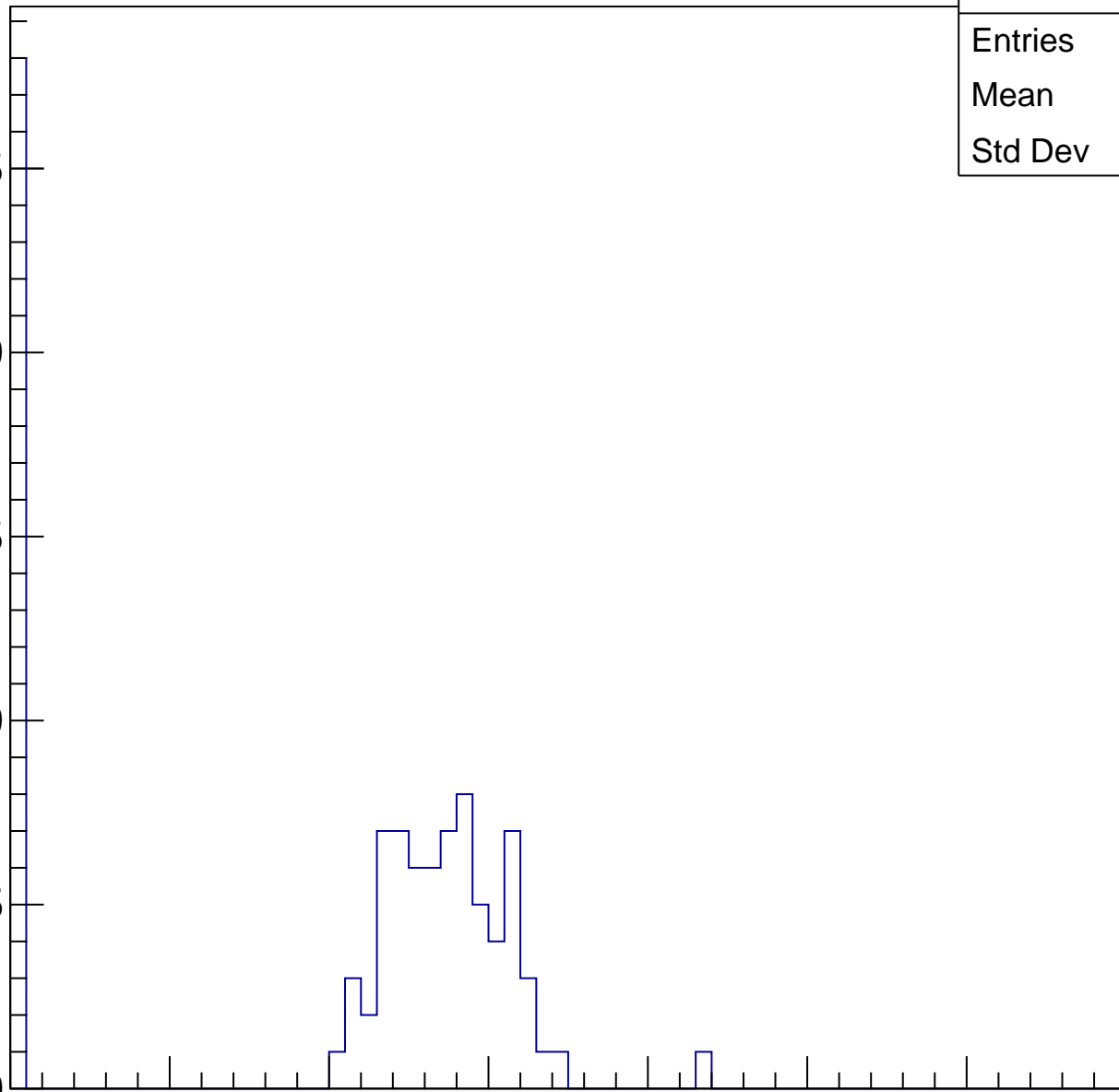
40

50

60

70

ampl

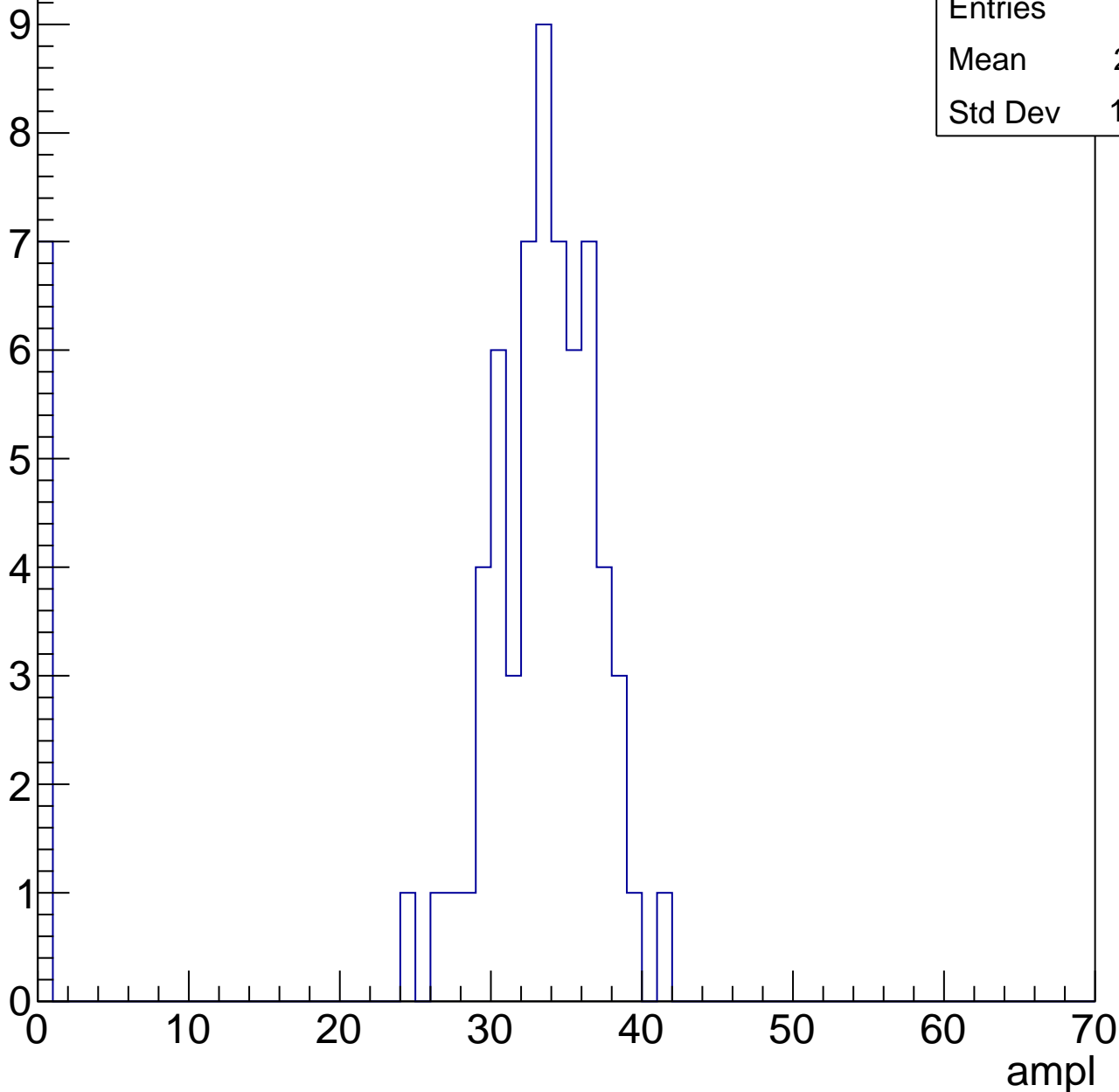


B1L103S, U23-ch28, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

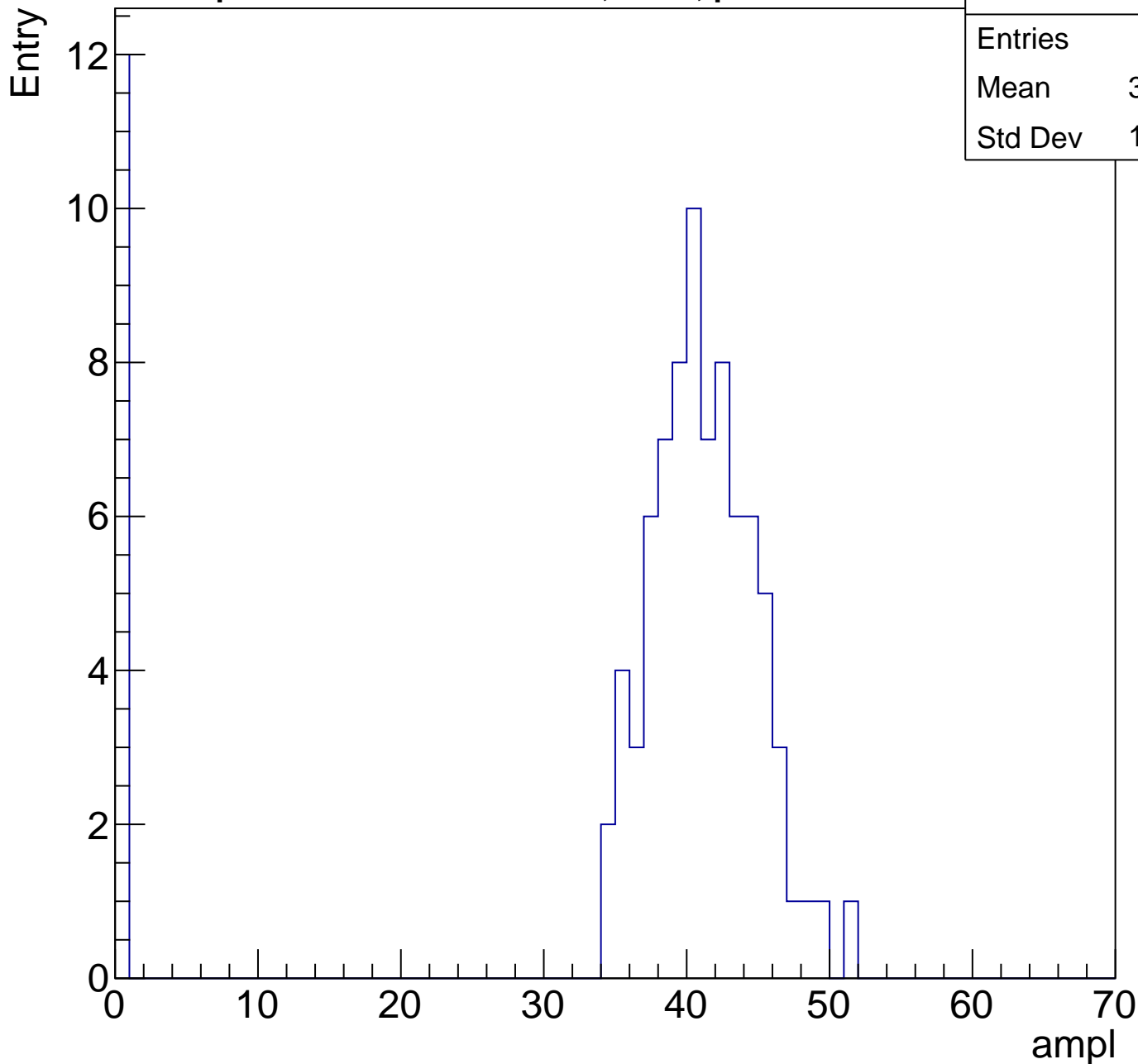
Entries	69
Mean	29.81
Std Dev	10.48



B1L103S, U23-ch28, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	91
Mean	35.37
Std Dev	14.18

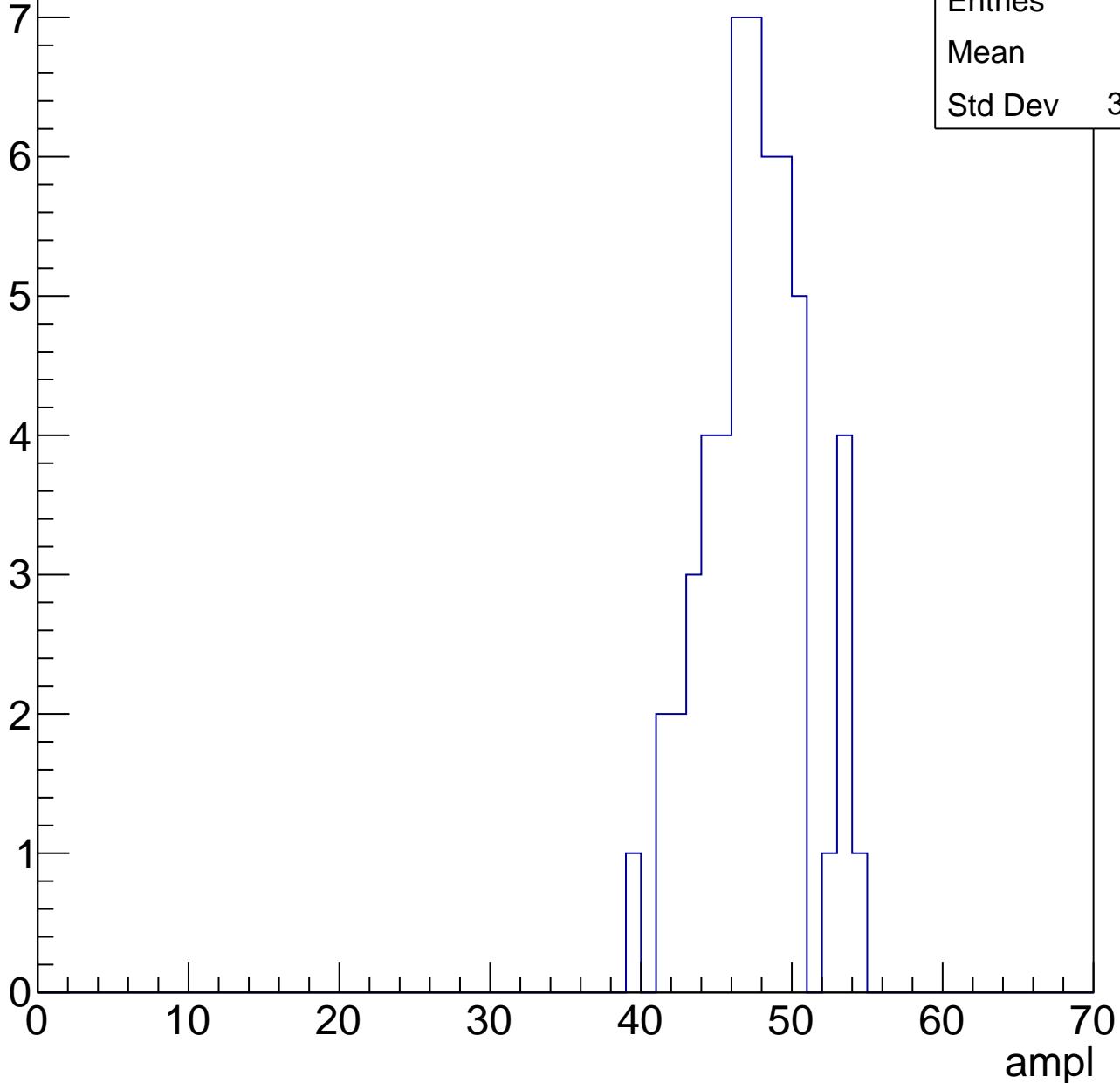


B1L103S, U23-ch28, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	53
Mean	47
Std Dev	3.325

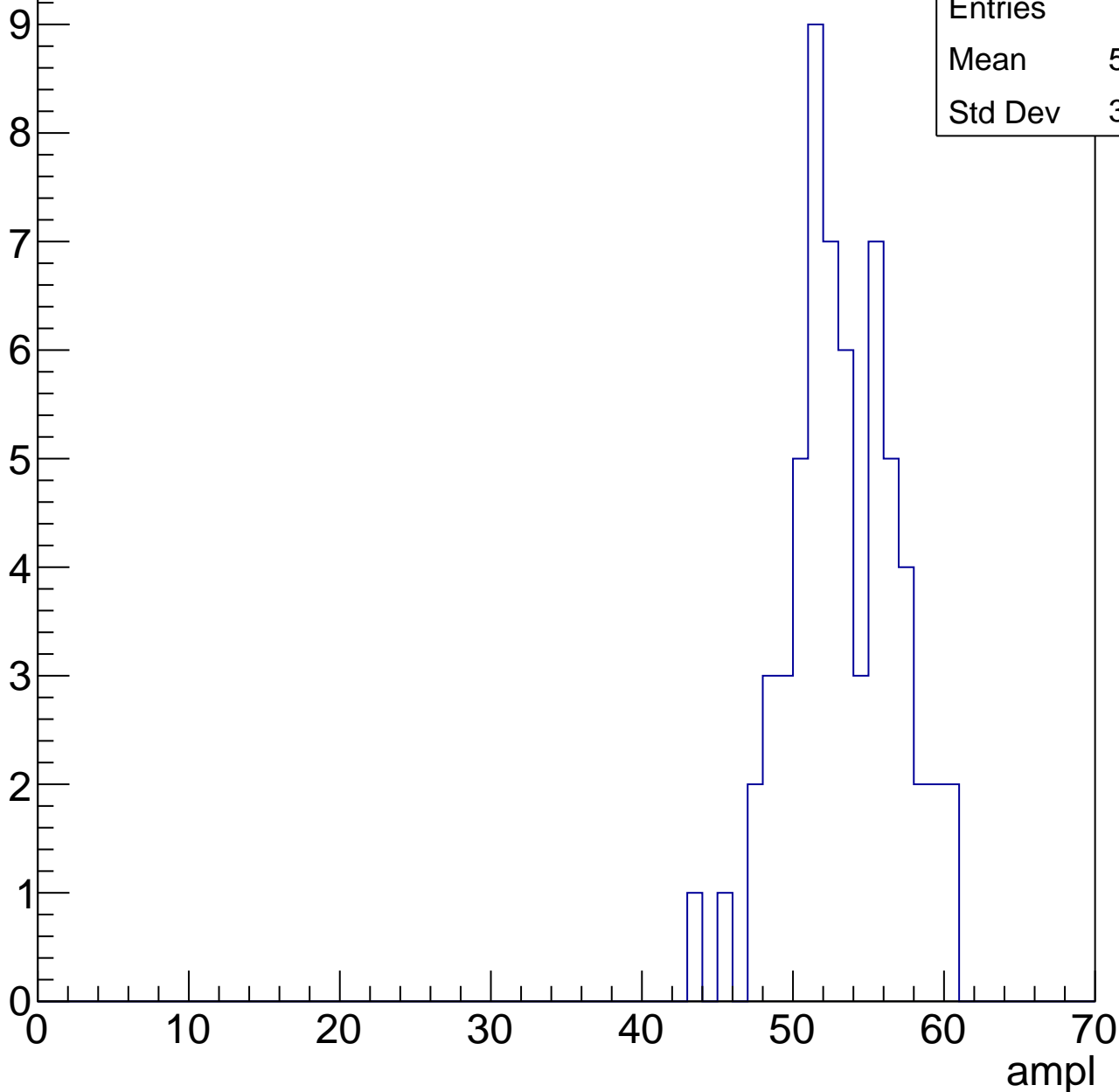


B1L103S, U23-ch28, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

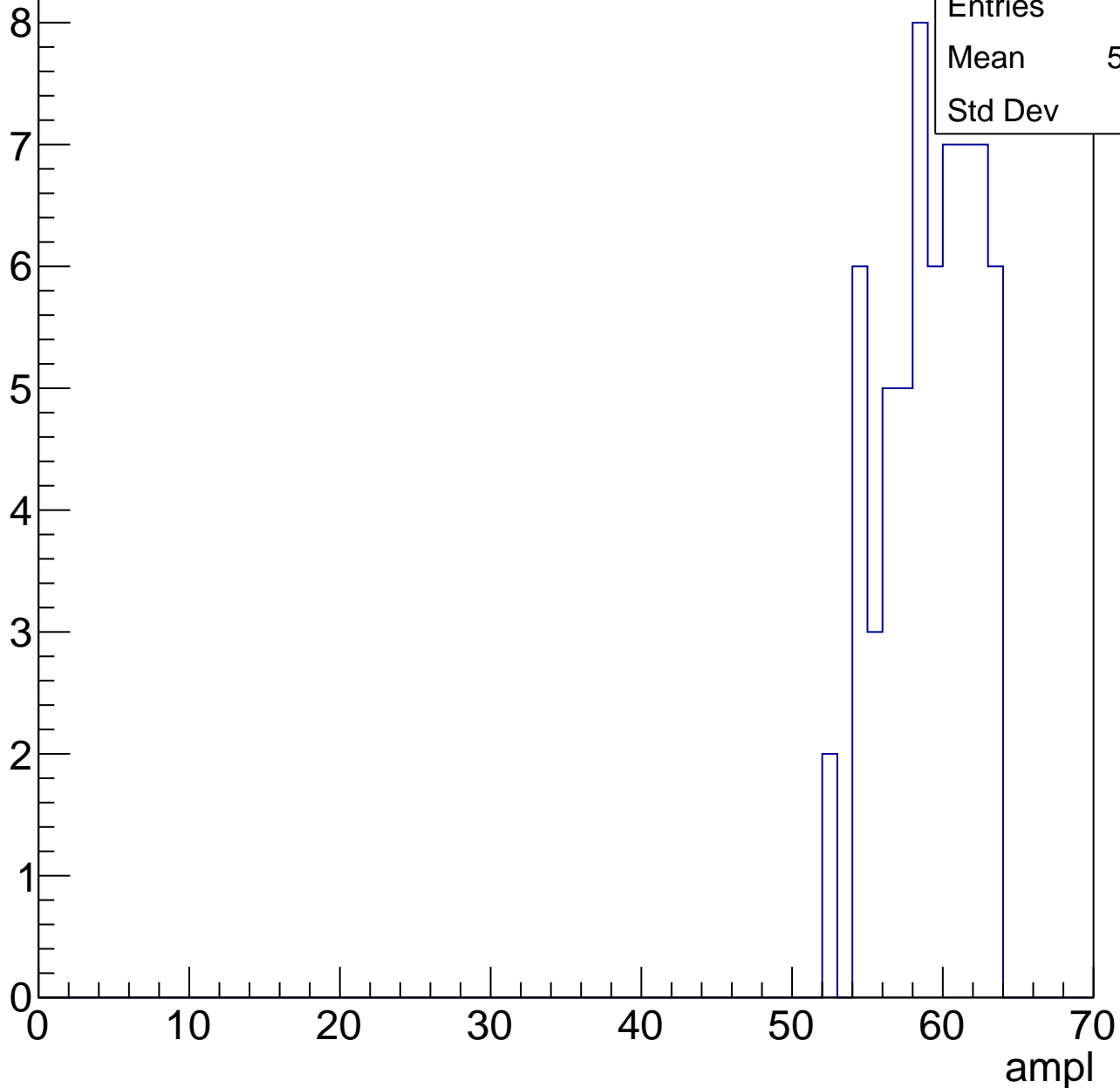
Entries	62
Mean	52.79
Std Dev	3.602



B1L103S, U23-ch28, adc5

calib_packv5_041523_1651.root, FC#0, port C2

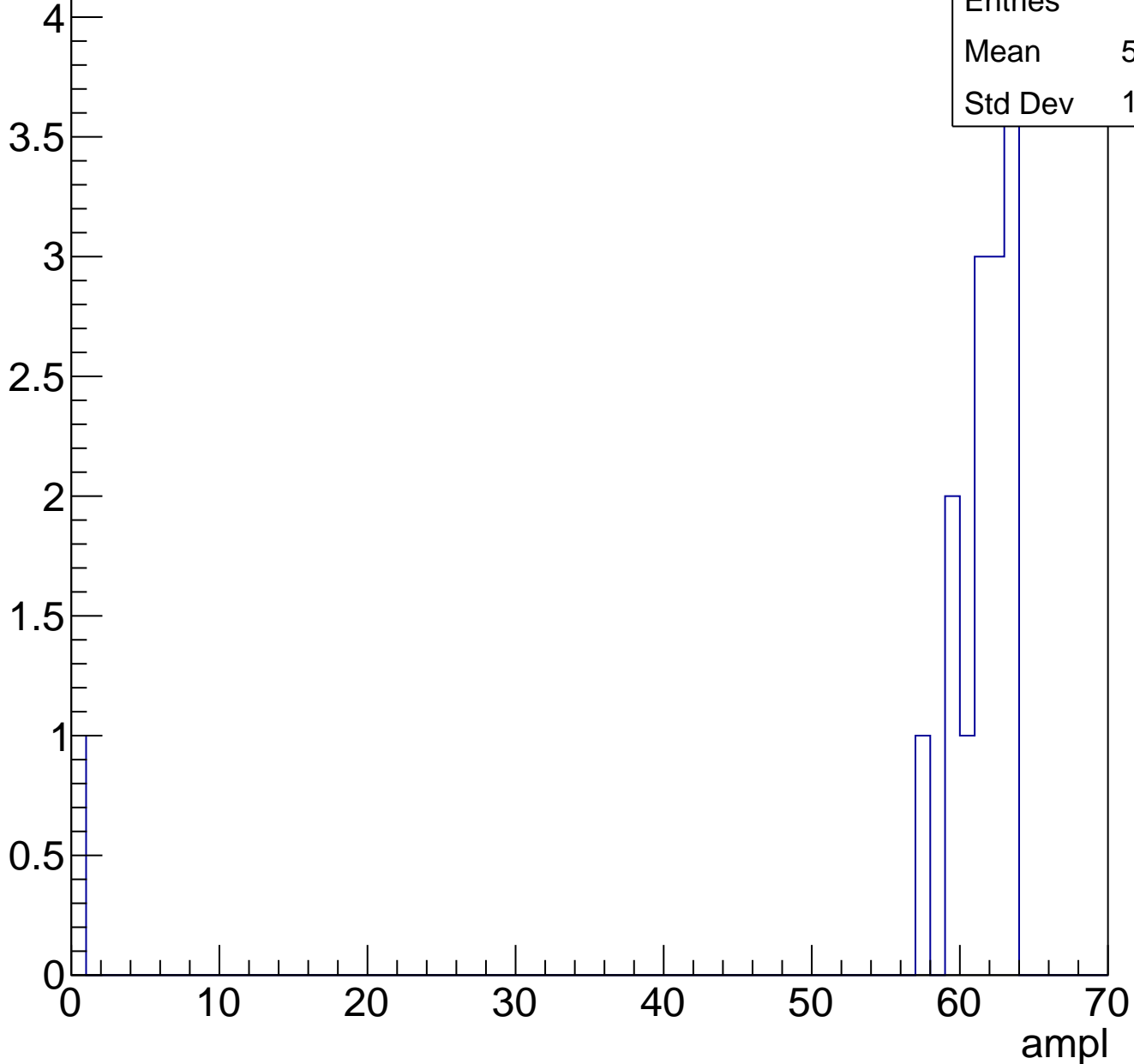
Entry



B1L103S, U23-ch28, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch28, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

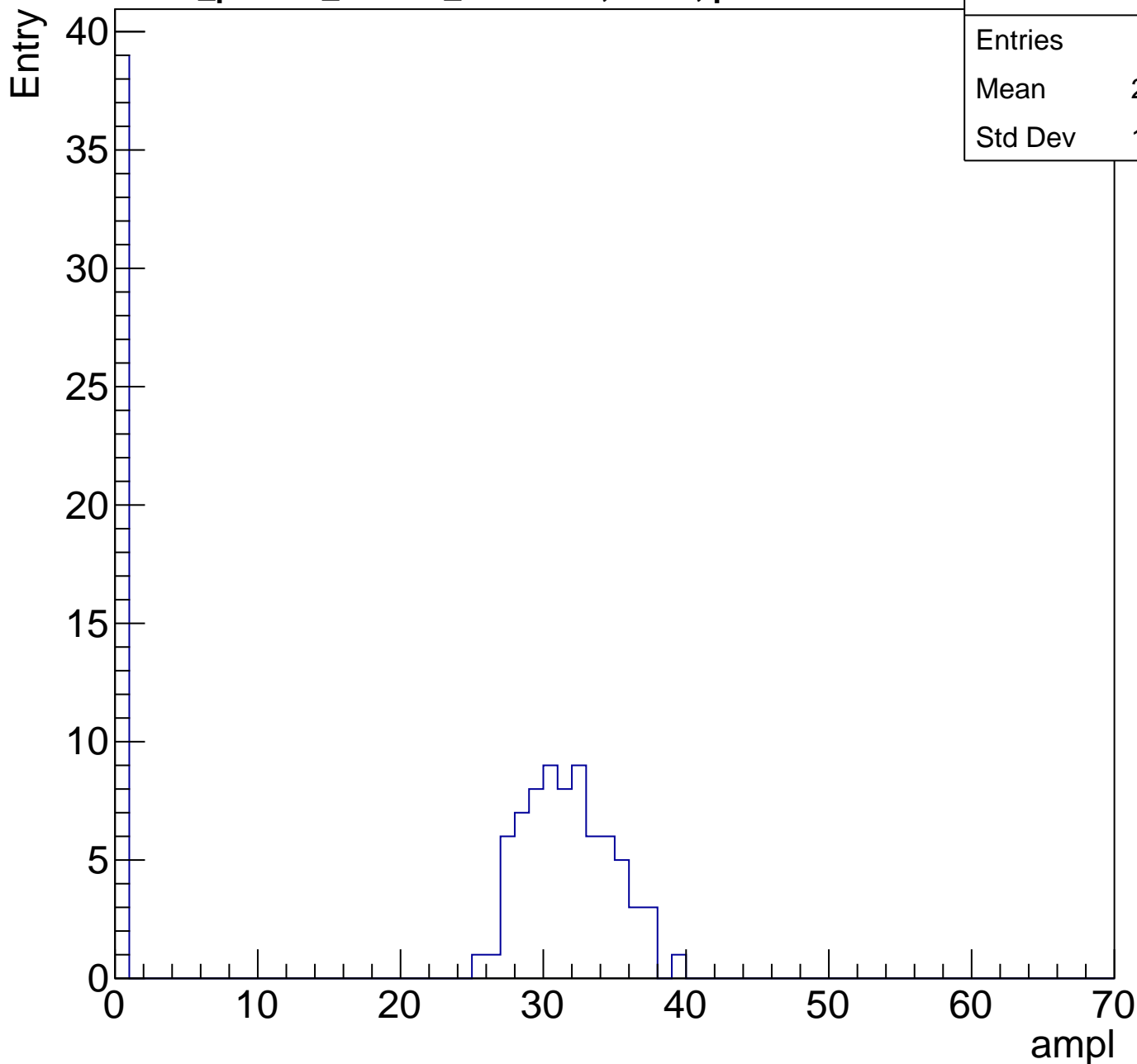
ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U23-ch29, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	112
Mean	20.38
Std Dev	15.09

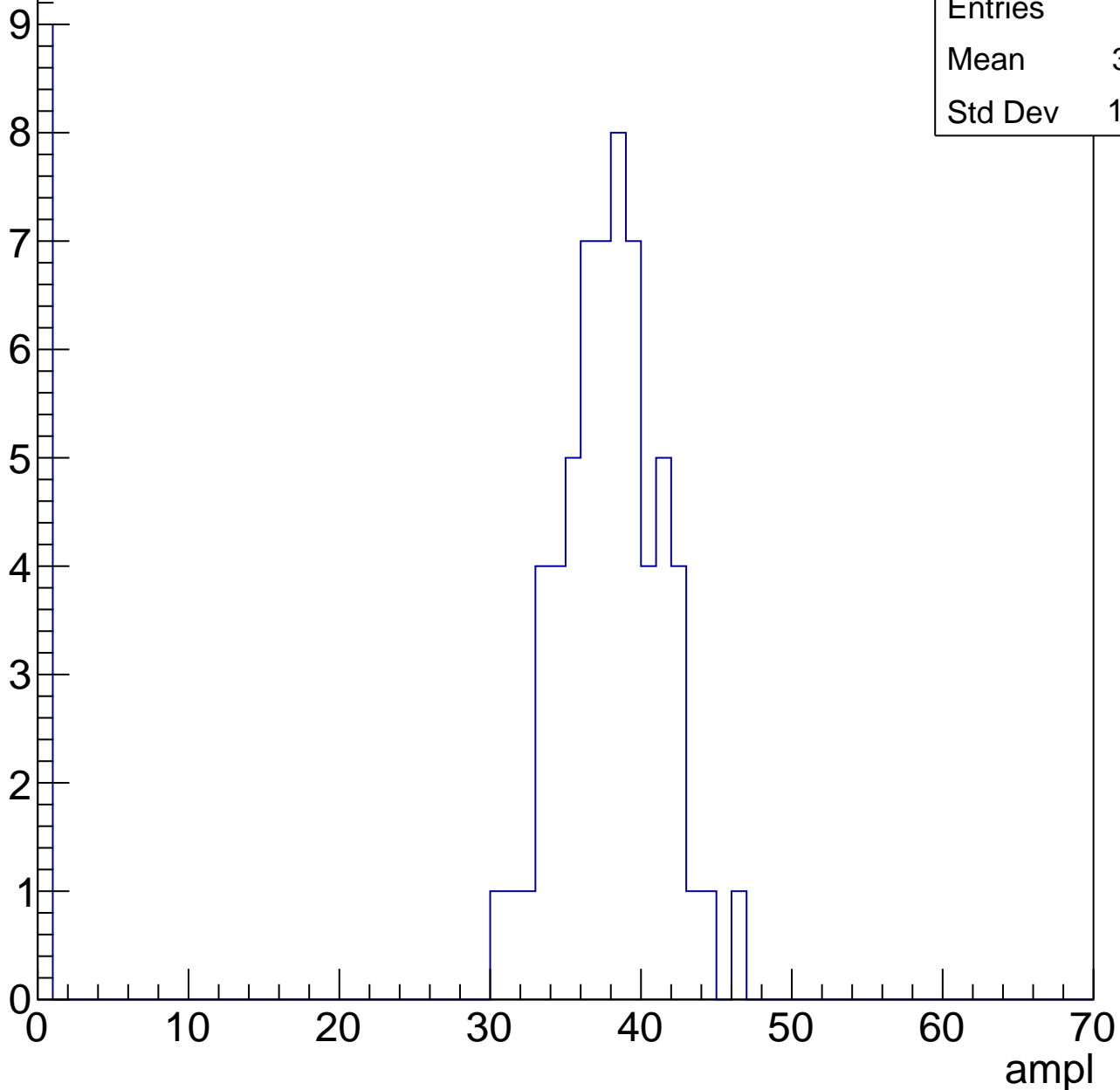


B1L103S, U23-ch29, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

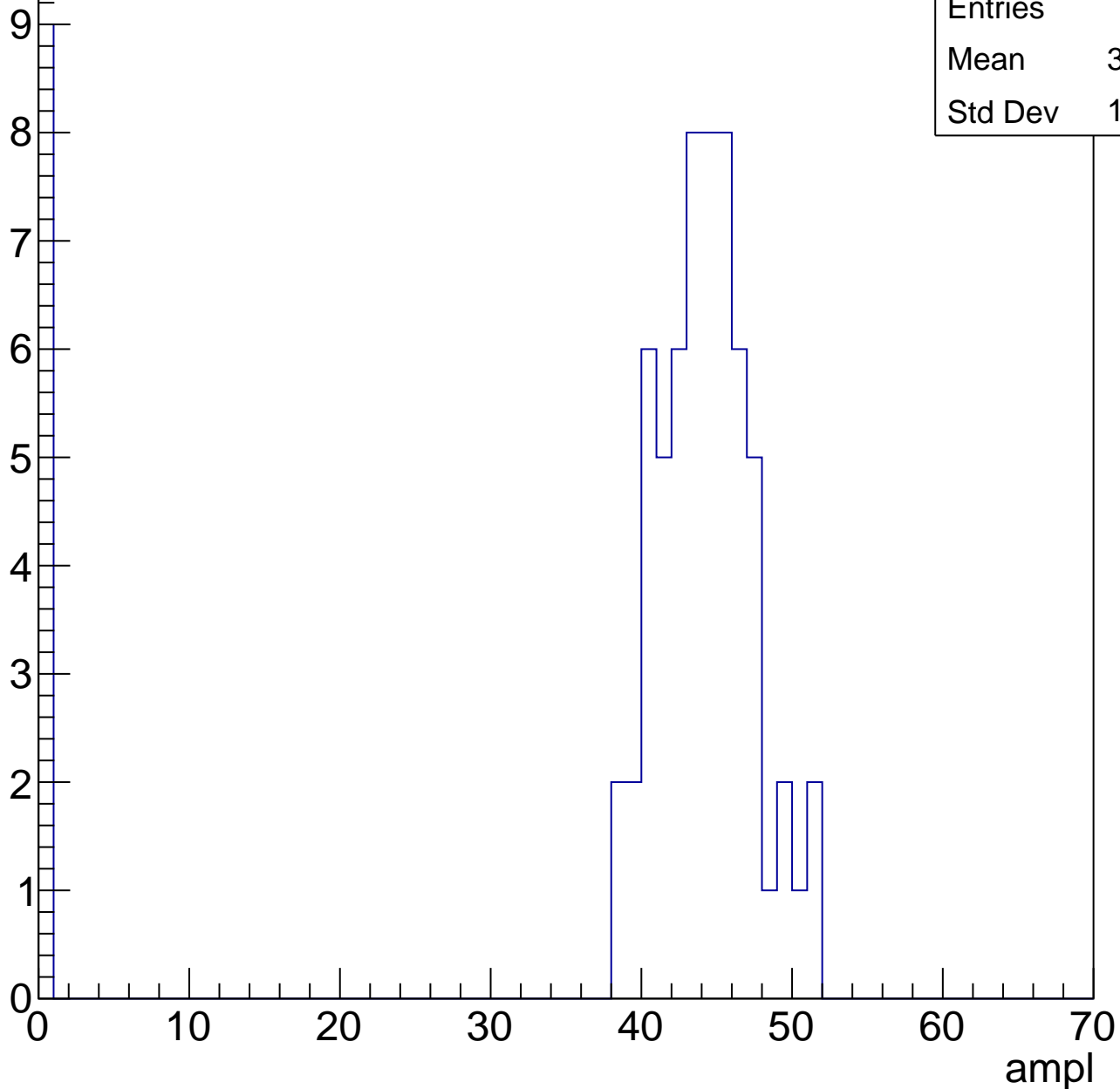
Entries	70
Mean	32.71
Std Dev	12.92



B1L103S, U23-ch29, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry



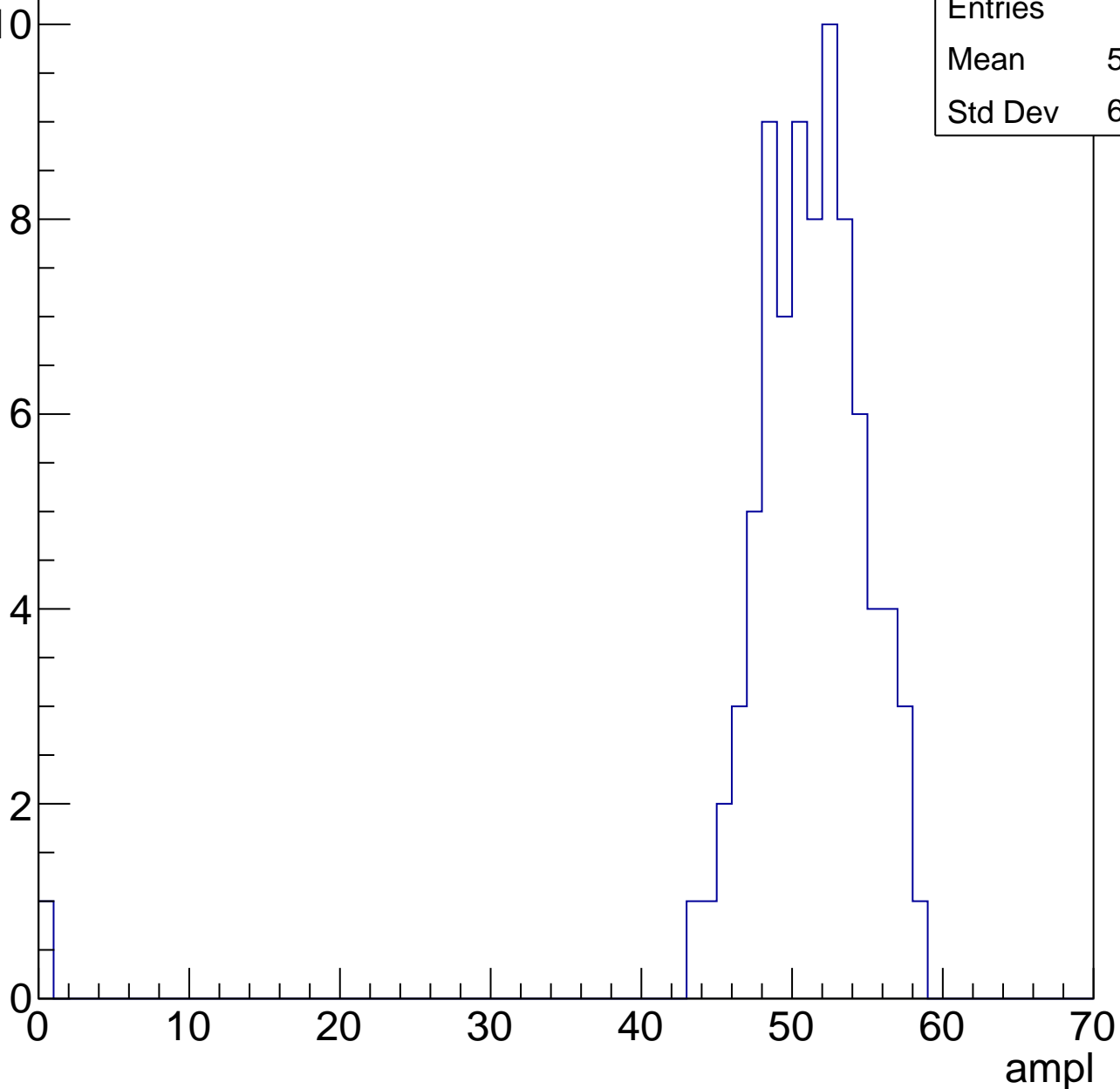
Entries	71
Mean	38.25
Std Dev	14.85

B1L103S, U23-ch29, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	82
Mean	50.29
Std Dev	6.472

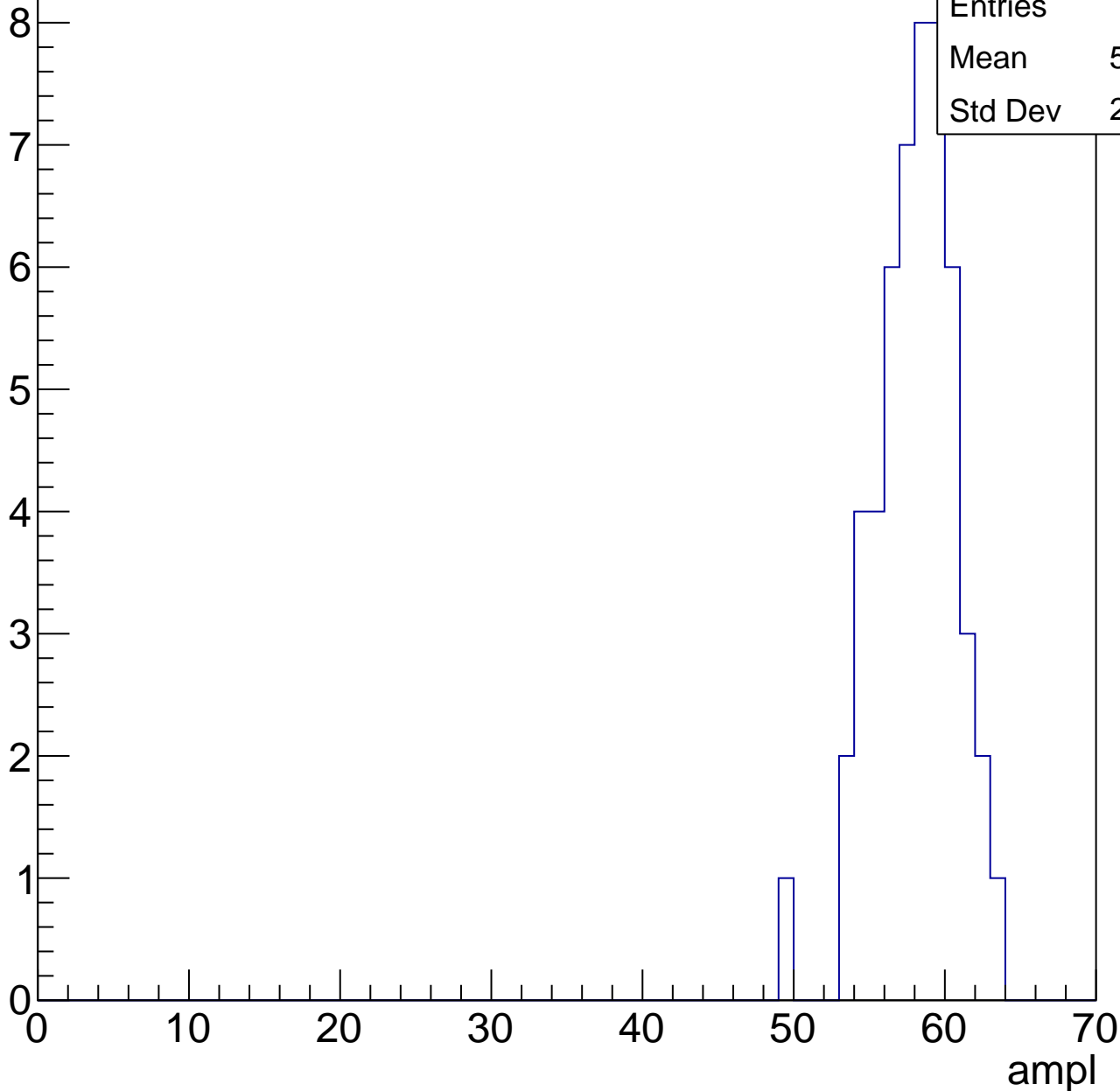


B1L103S, U23-ch29, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	52
Mean	57.54
Std Dev	2.656

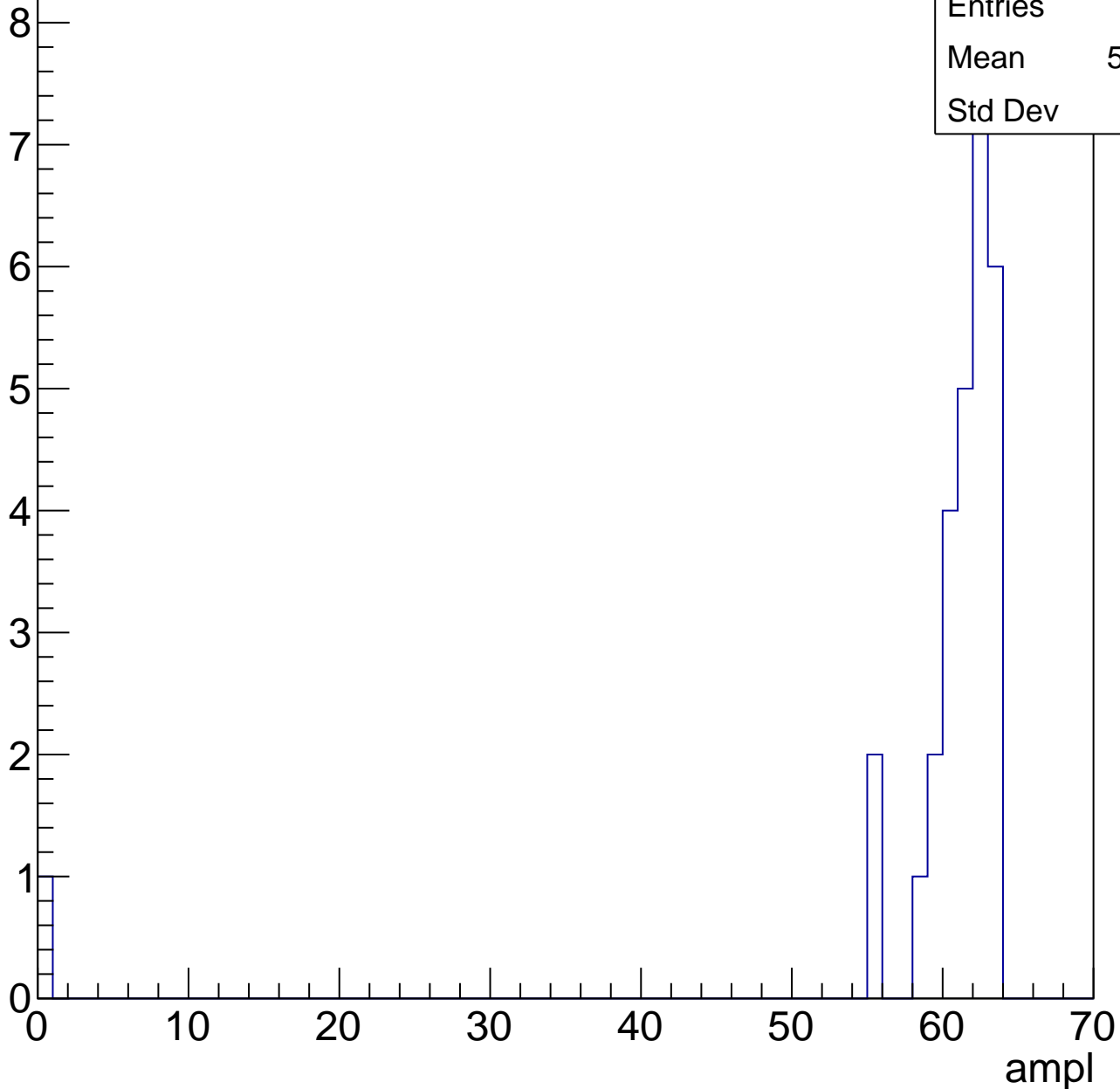


B1L103S, U23-ch29, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	29
Mean	58.79
Std Dev	11.3



B1L103S, U23-ch29, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch29, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

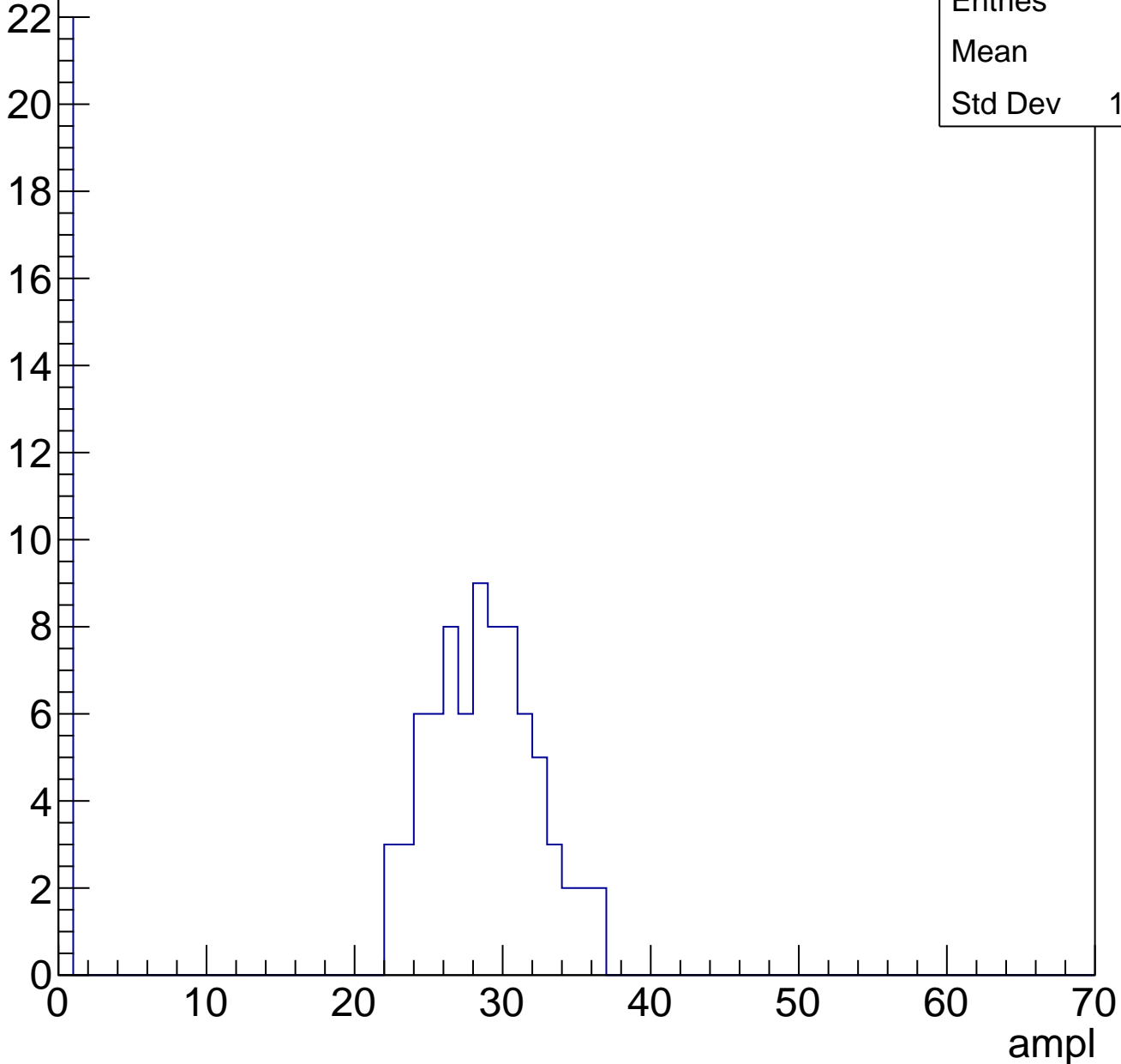
Entries	19
Mean	0
Std Dev	0

B1L103S, U23-ch30, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	99
Mean	22
Std Dev	12.14

Entry

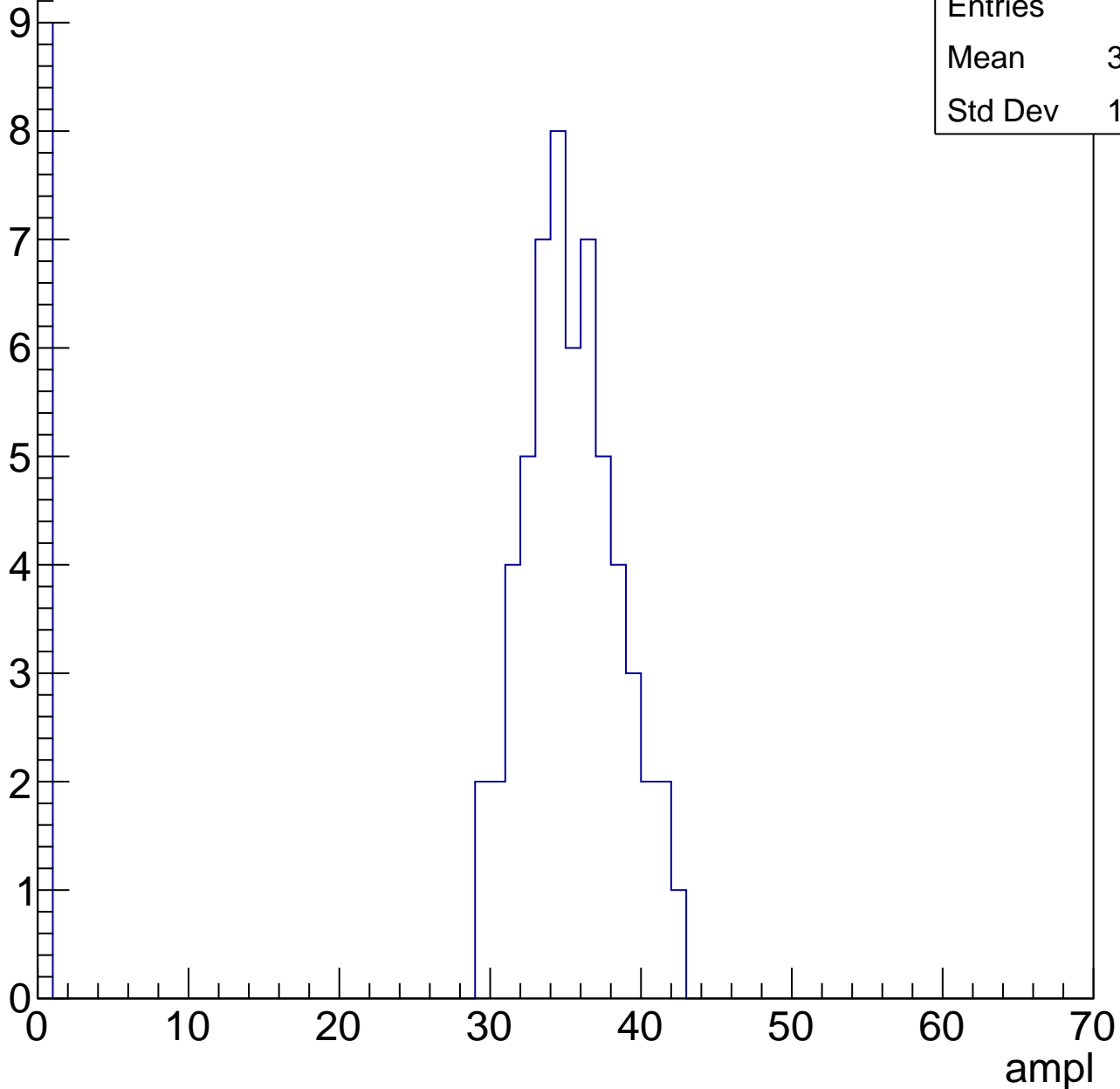


B1L103S, U23-ch30, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	30.22
Std Dev	12.24

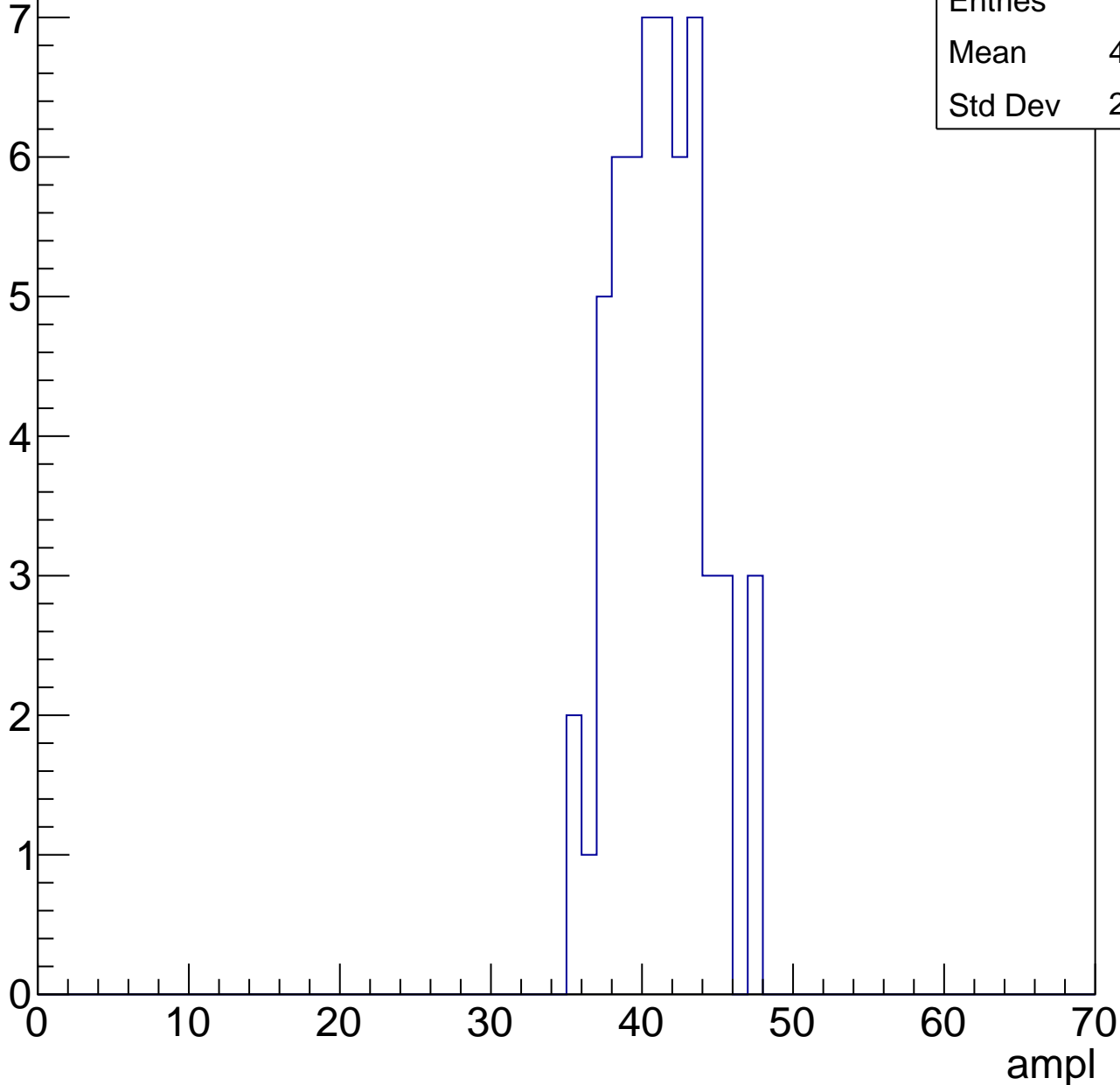


B1L103S, U23-ch30, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	56
Mean	40.73
Std Dev	2.912

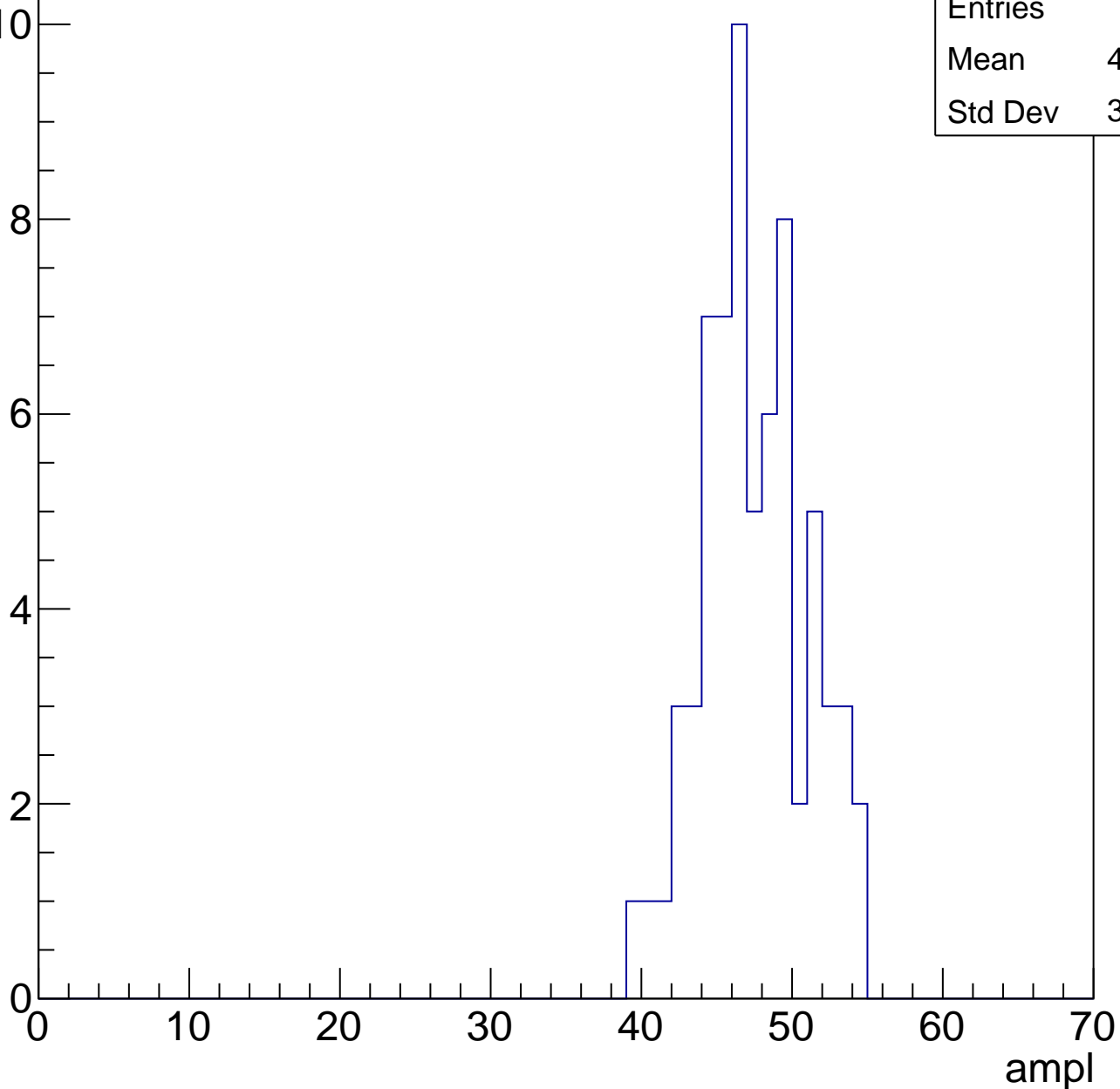


B1L103S, U23-ch30, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

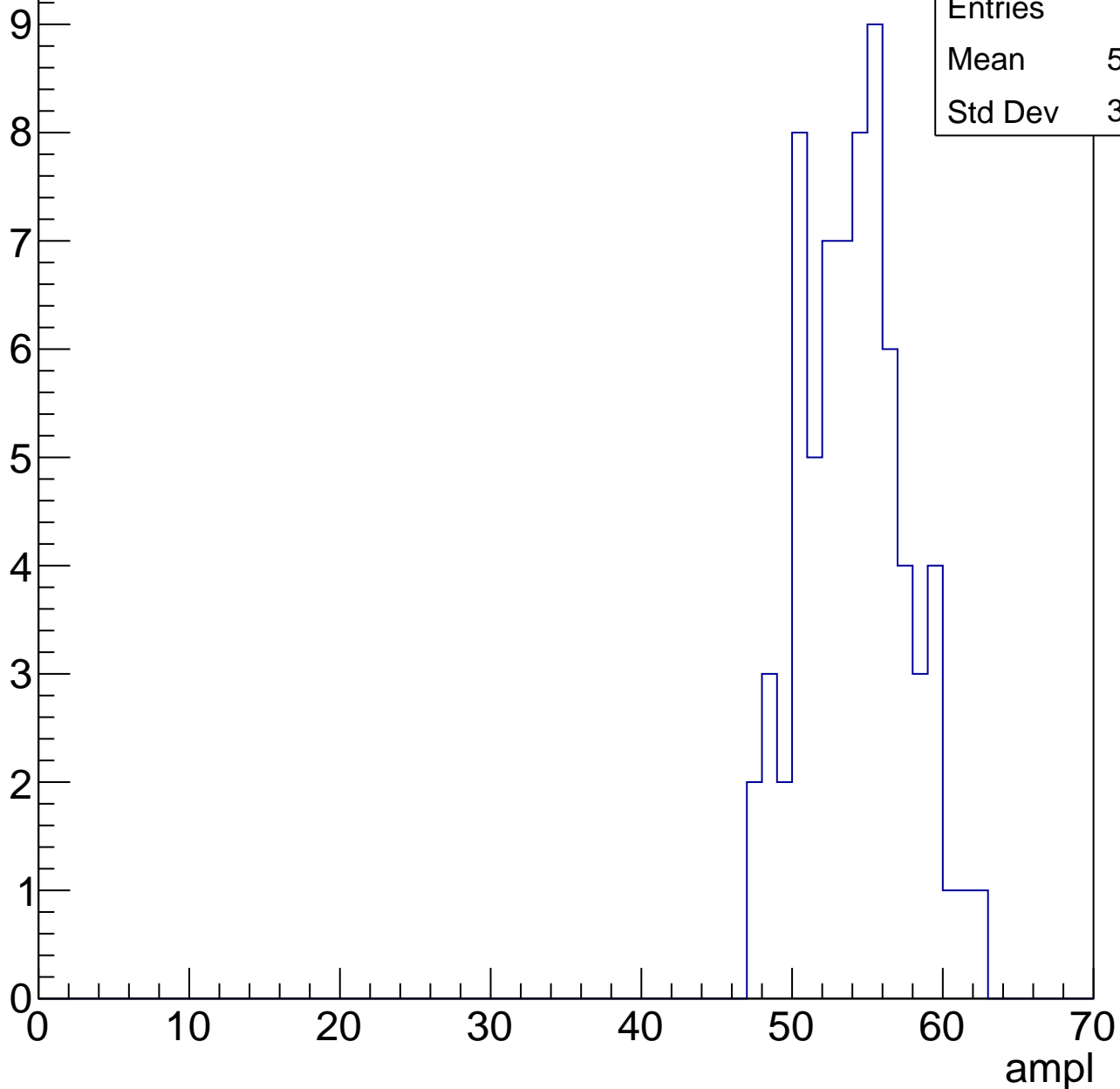
Entries	67
Mean	47.03
Std Dev	3.434



B1L103S, U23-ch30, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

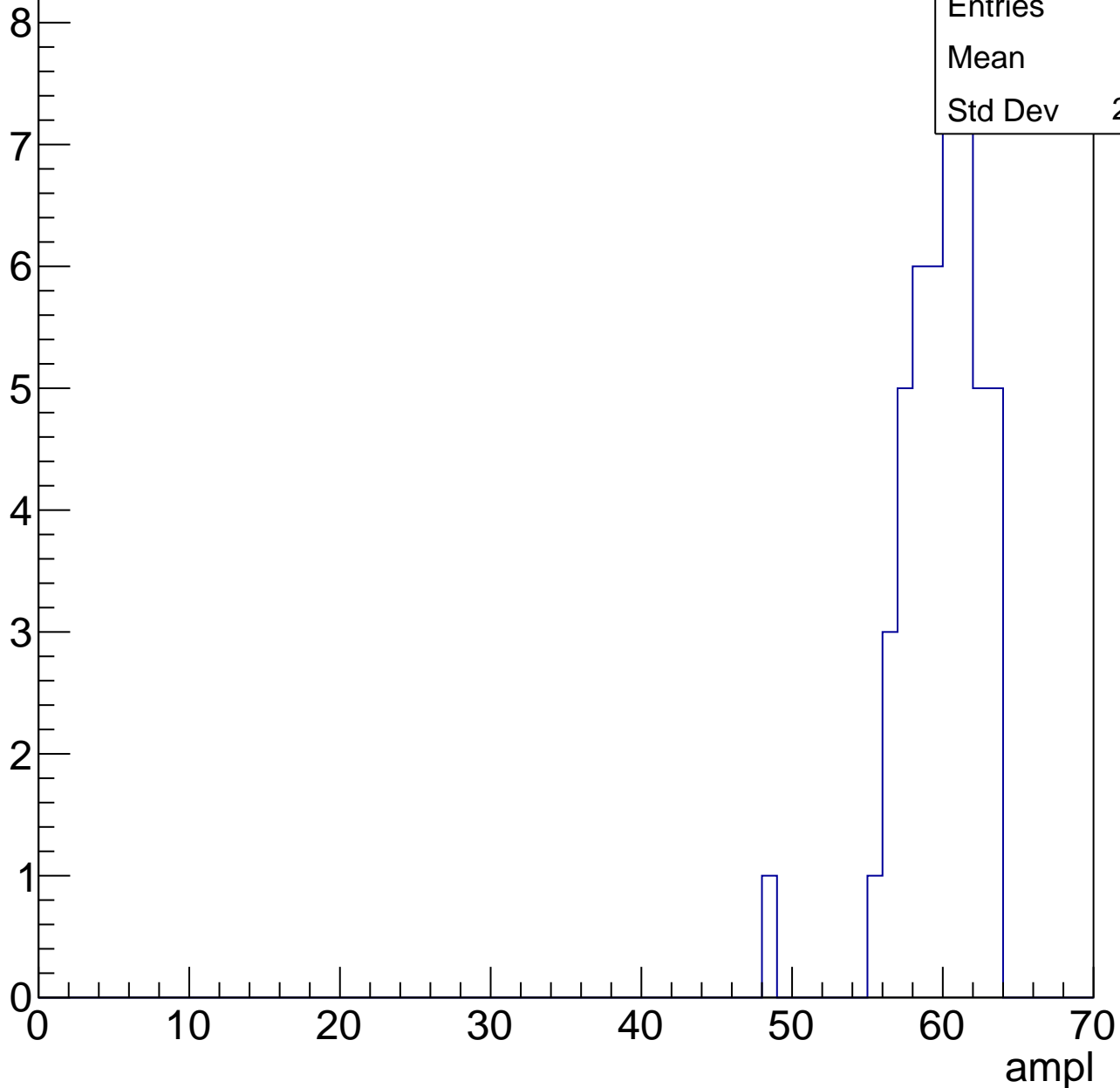


B1L103S, U23-ch30, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	48
Mean	59.4
Std Dev	2.691

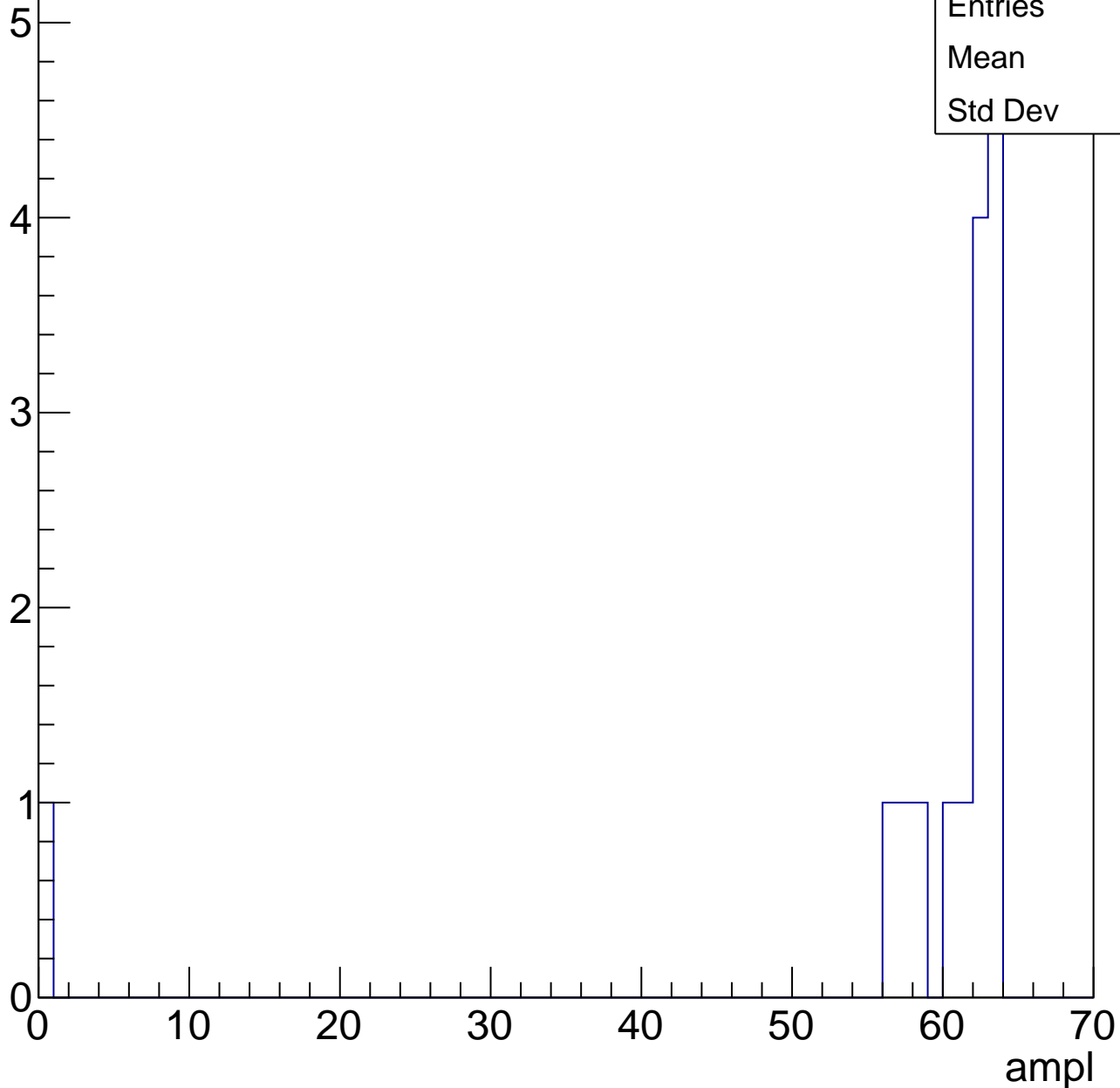


B1L103S, U23-ch30, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	15
Mean	57
Std Dev	15.4



B1L103S, U23-ch30, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

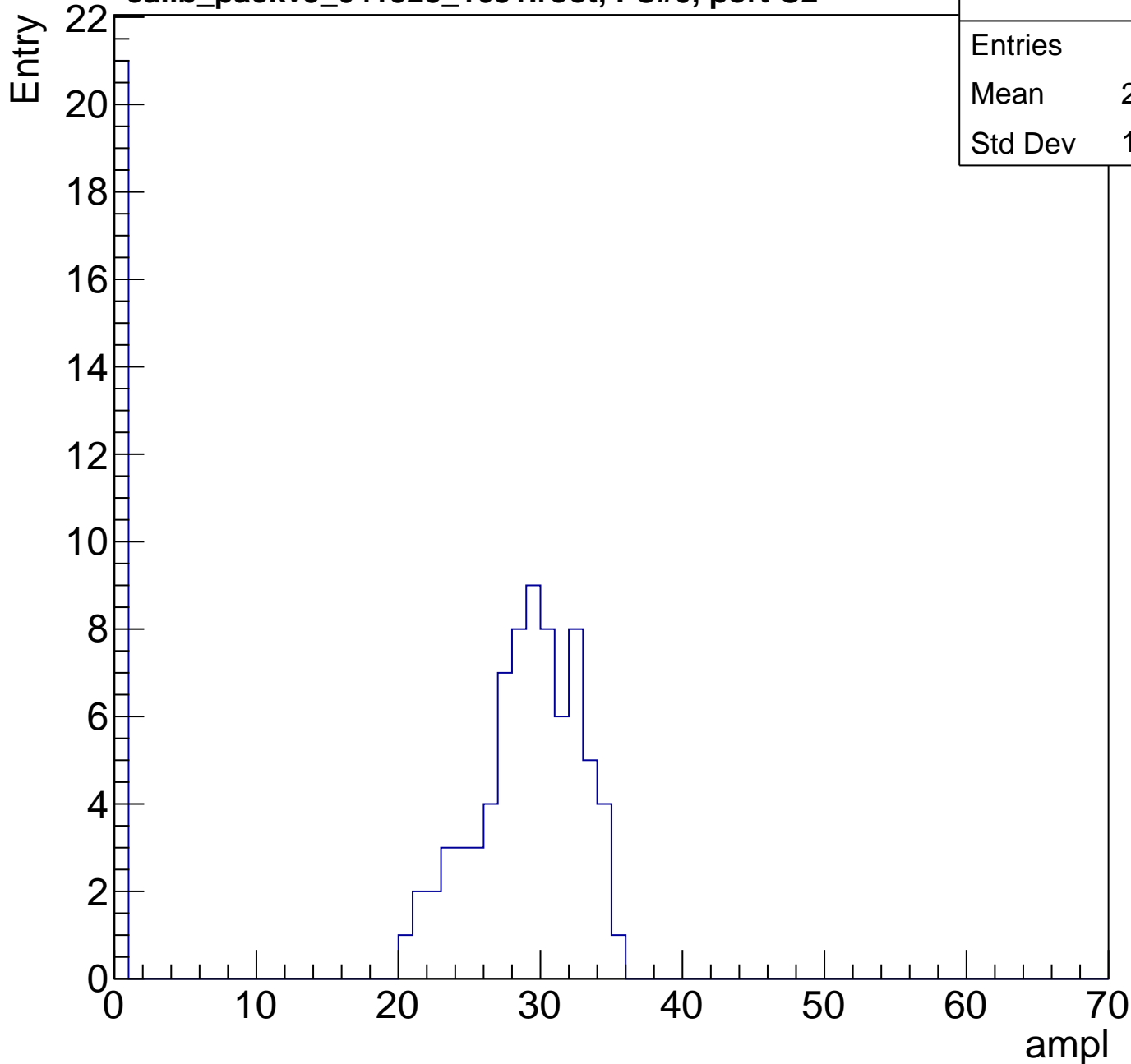
ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U23-ch31, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	95
Mean	22.29
Std Dev	12.28

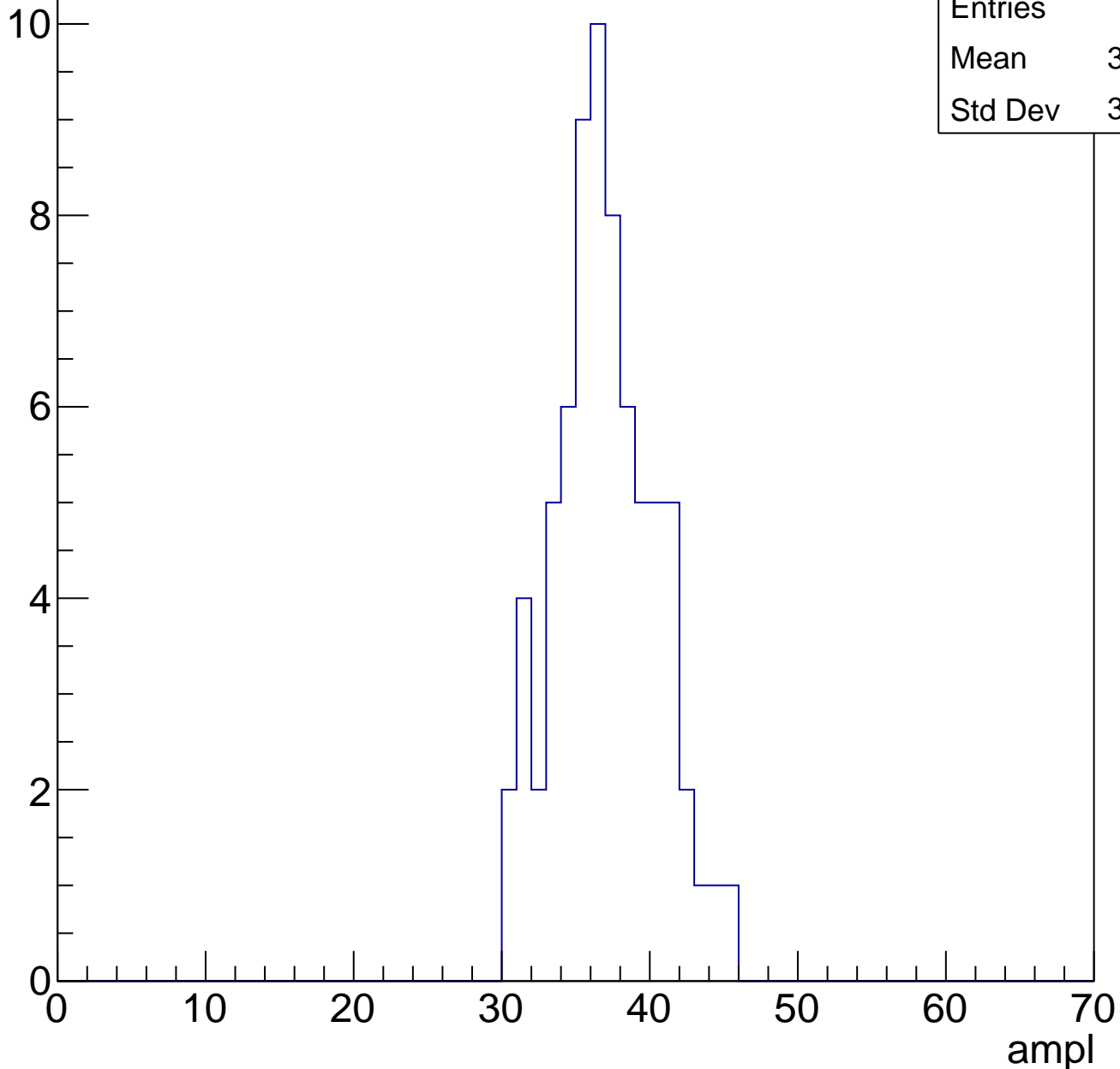


B1L103S, U23-ch31, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	72
Mean	36.56
Std Dev	3.349

Entry

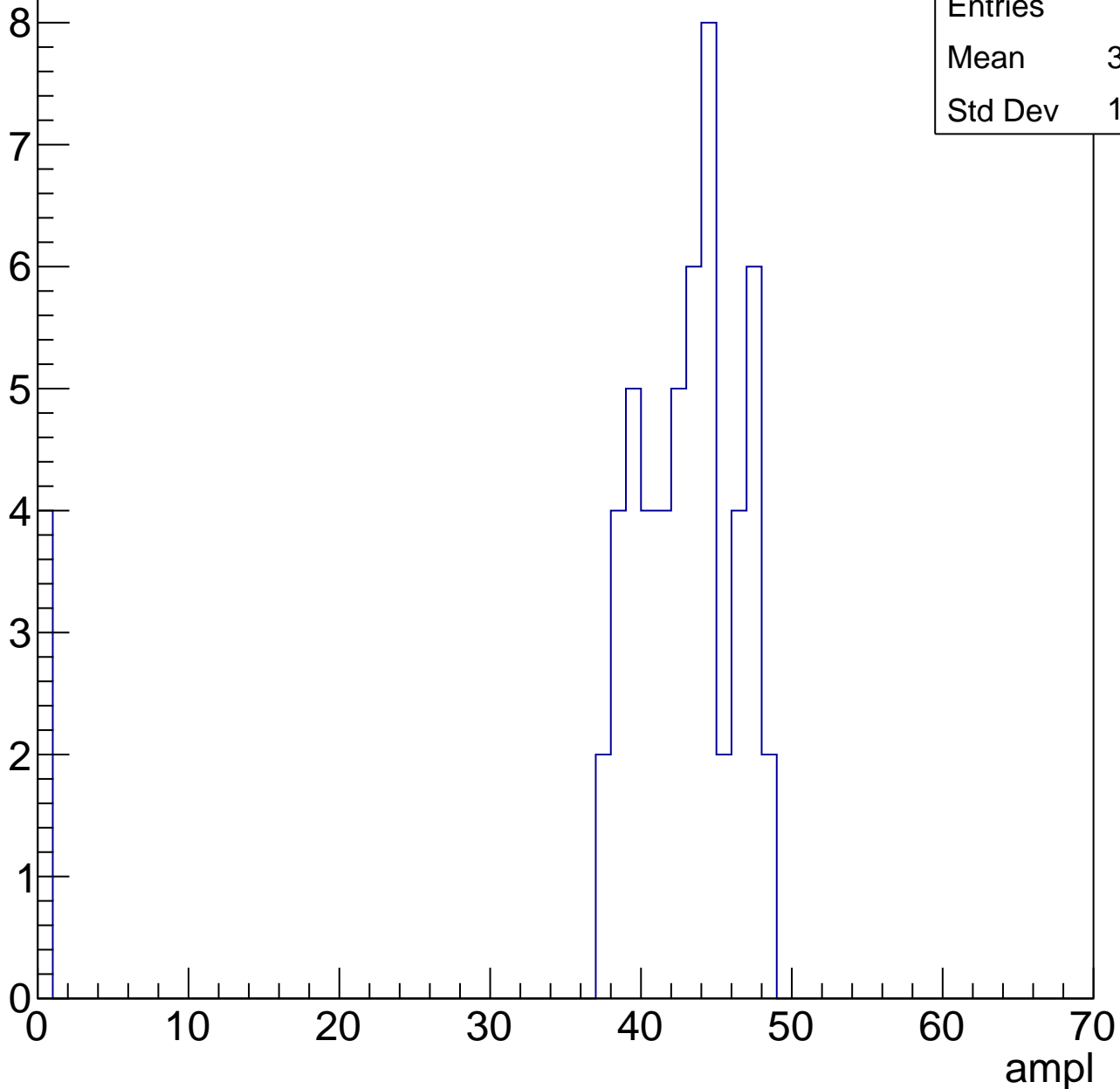


B1L103S, U23-ch31, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

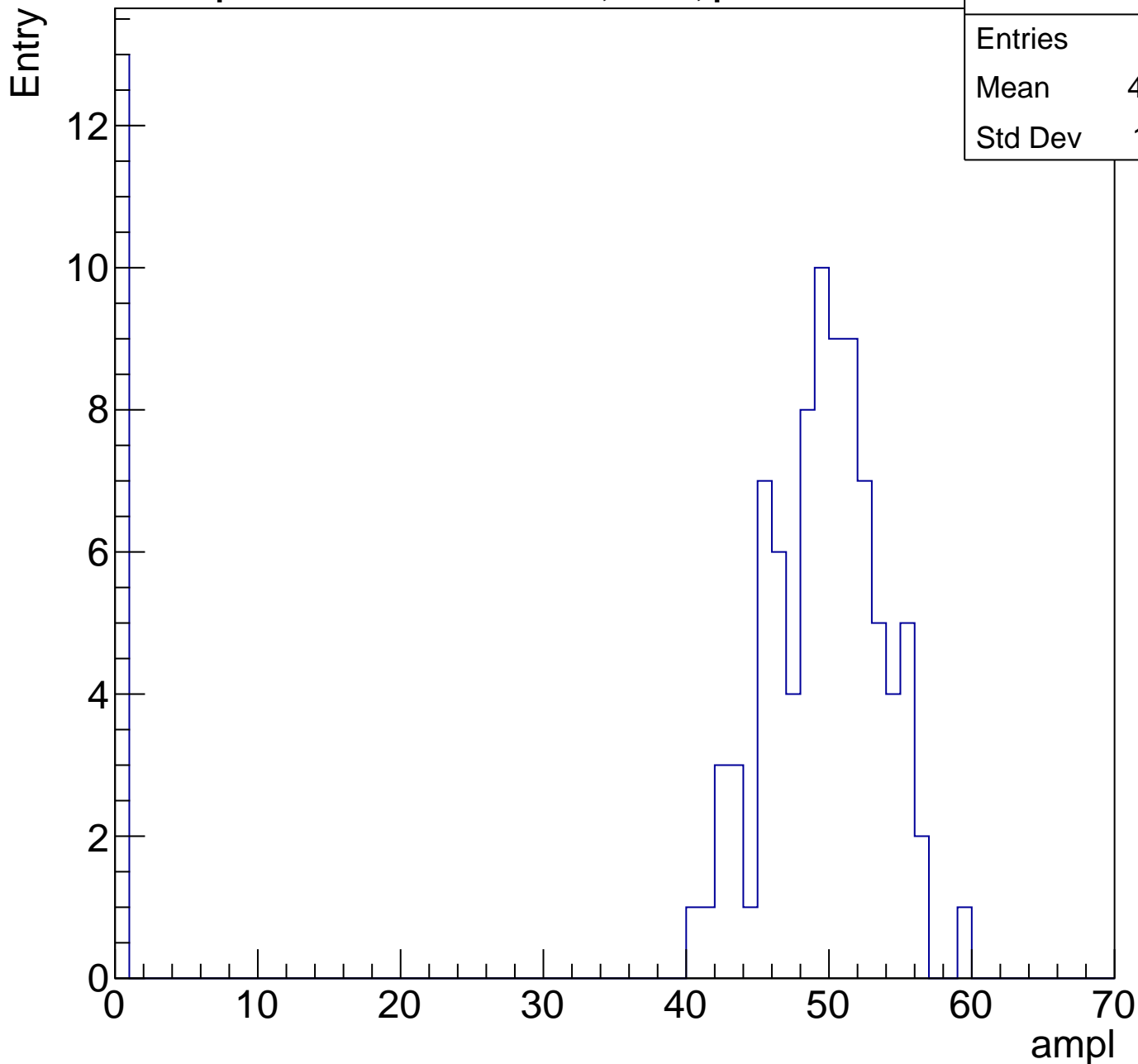
Entries	56
Mean	39.59
Std Dev	11.38



B1L103S, U23-ch31, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	99
Mean	42.76
Std Dev	17.01

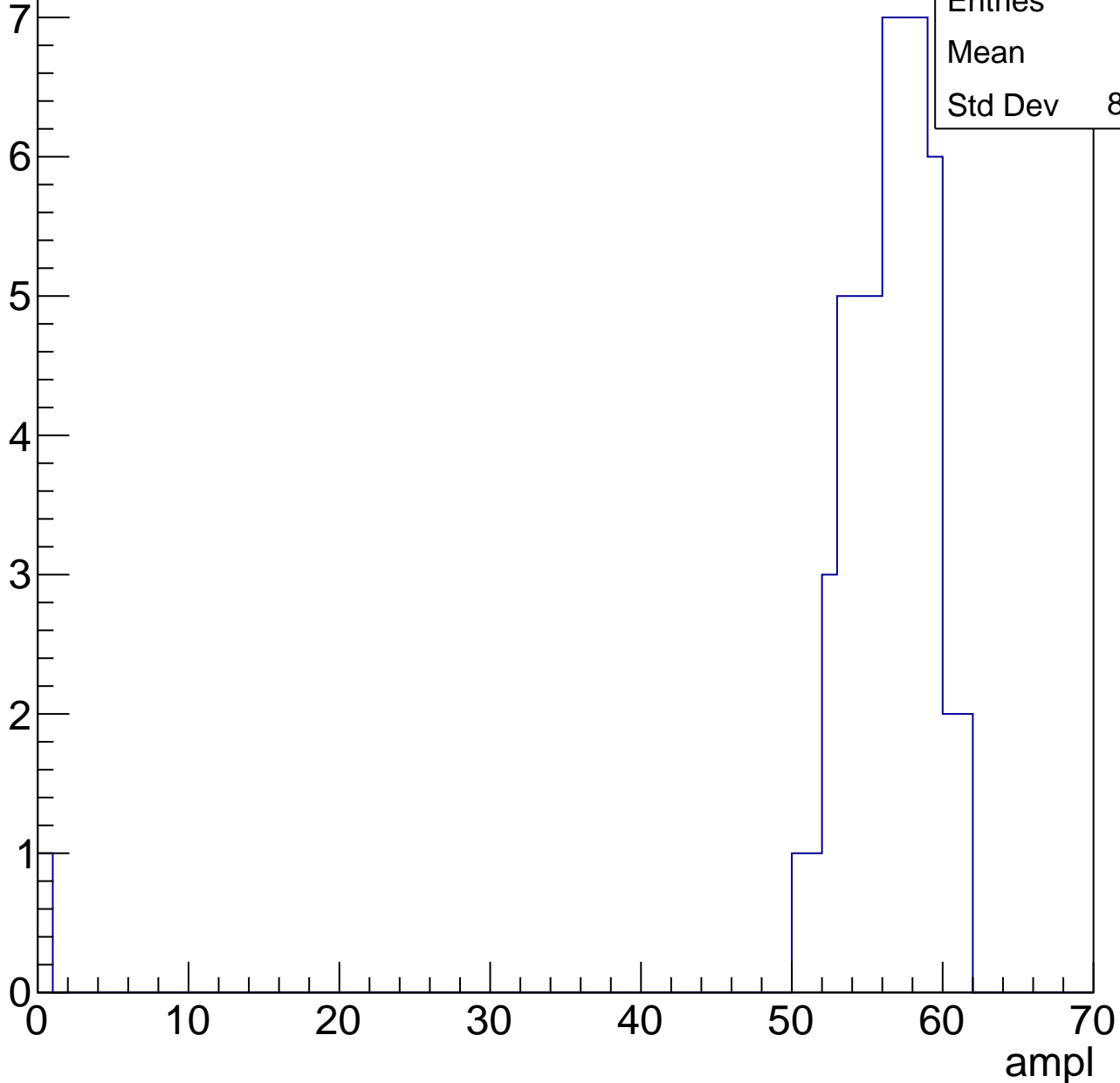


B1L103S, U23-ch31, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

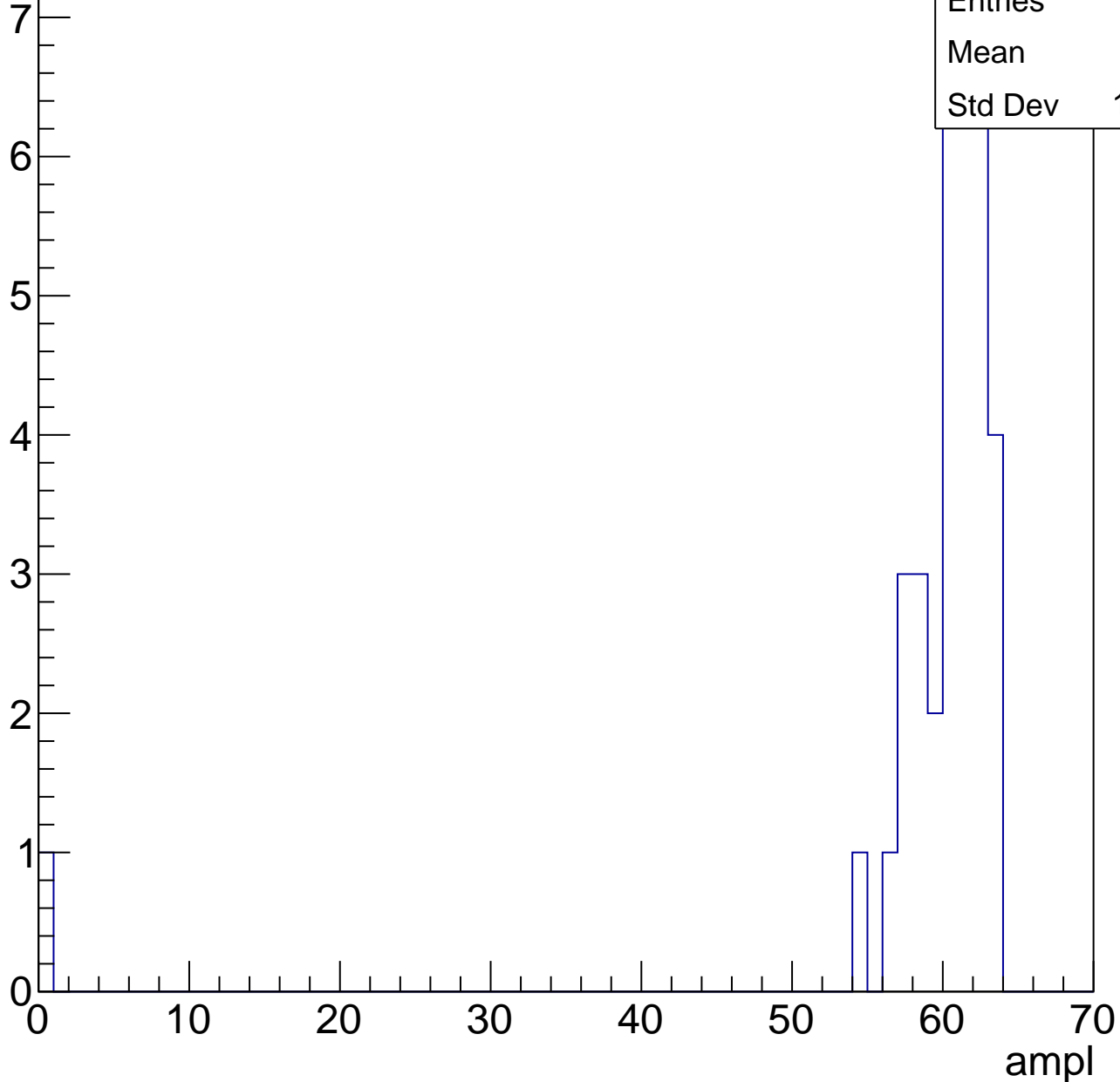
Entries	52
Mean	55
Std Dev	8.126



B1L103S, U23-ch31, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

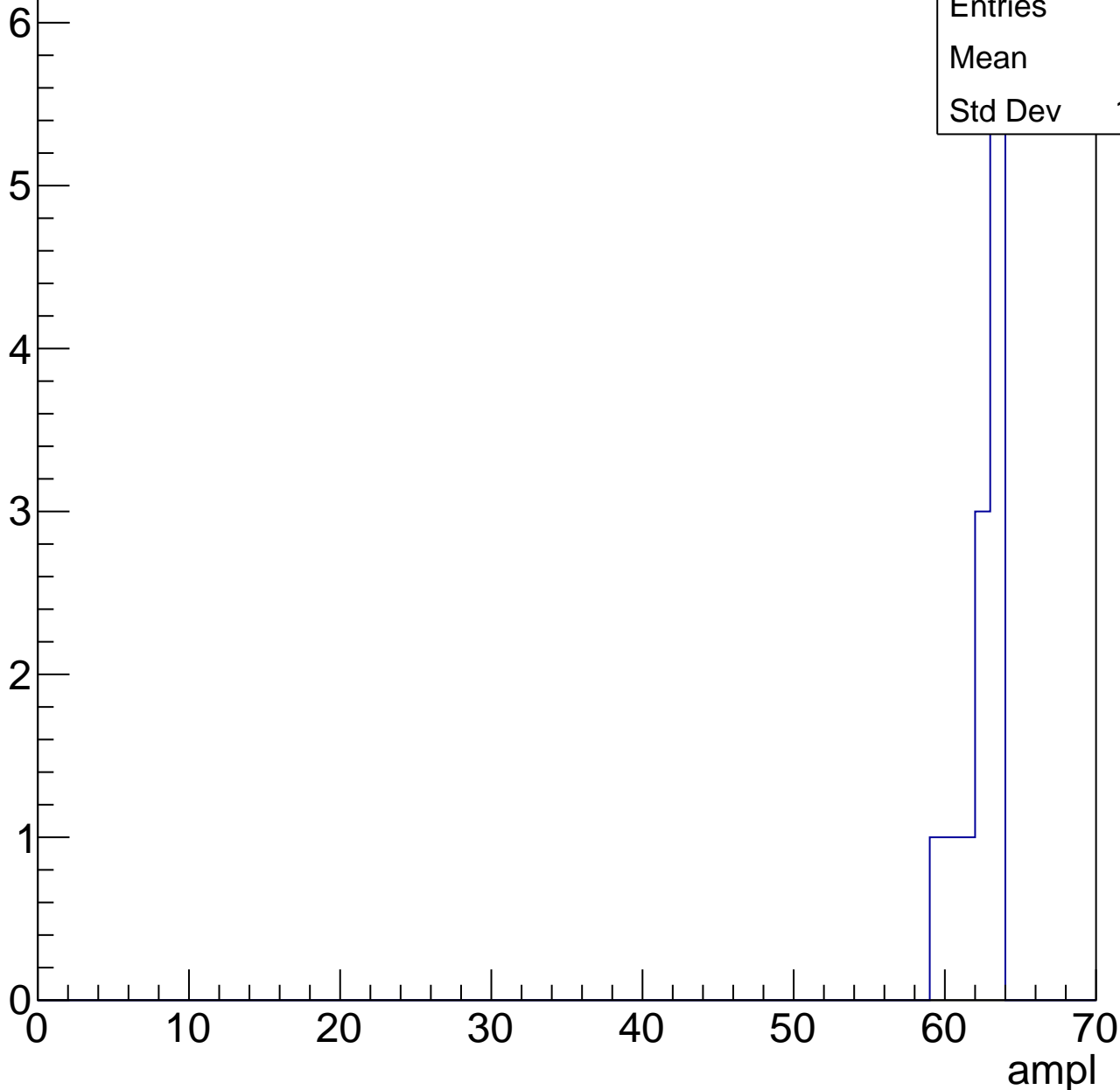


B1L103S, U23-ch31, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	12
Mean	62
Std Dev	1.291



B1L103S, U23-ch31, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U23-ch32, adc0

calib_packv5_041523_1651.root, FC#0, port C2

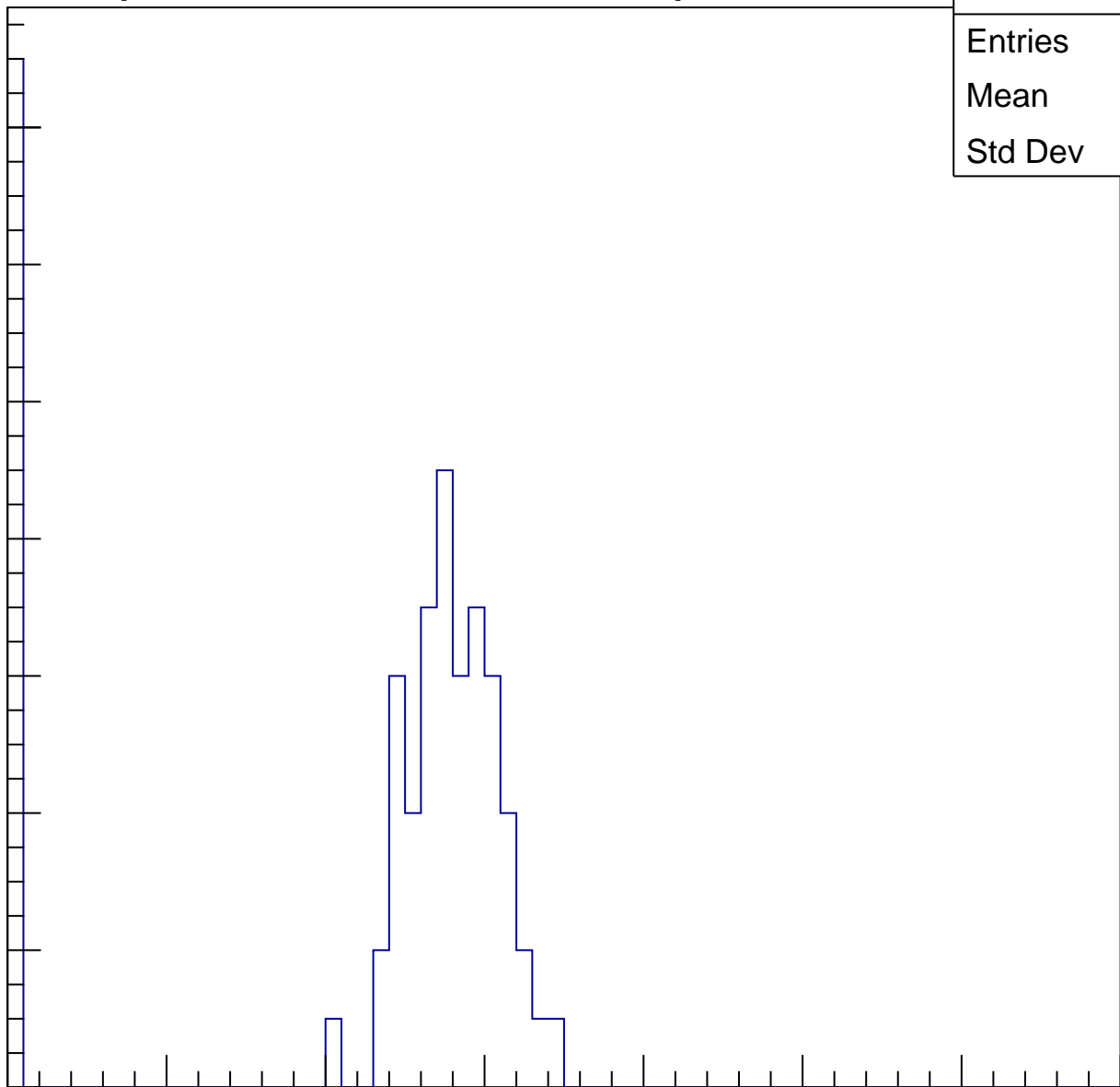
Entries	71
Mean	21.7
Std Dev	11.5

Entry

14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

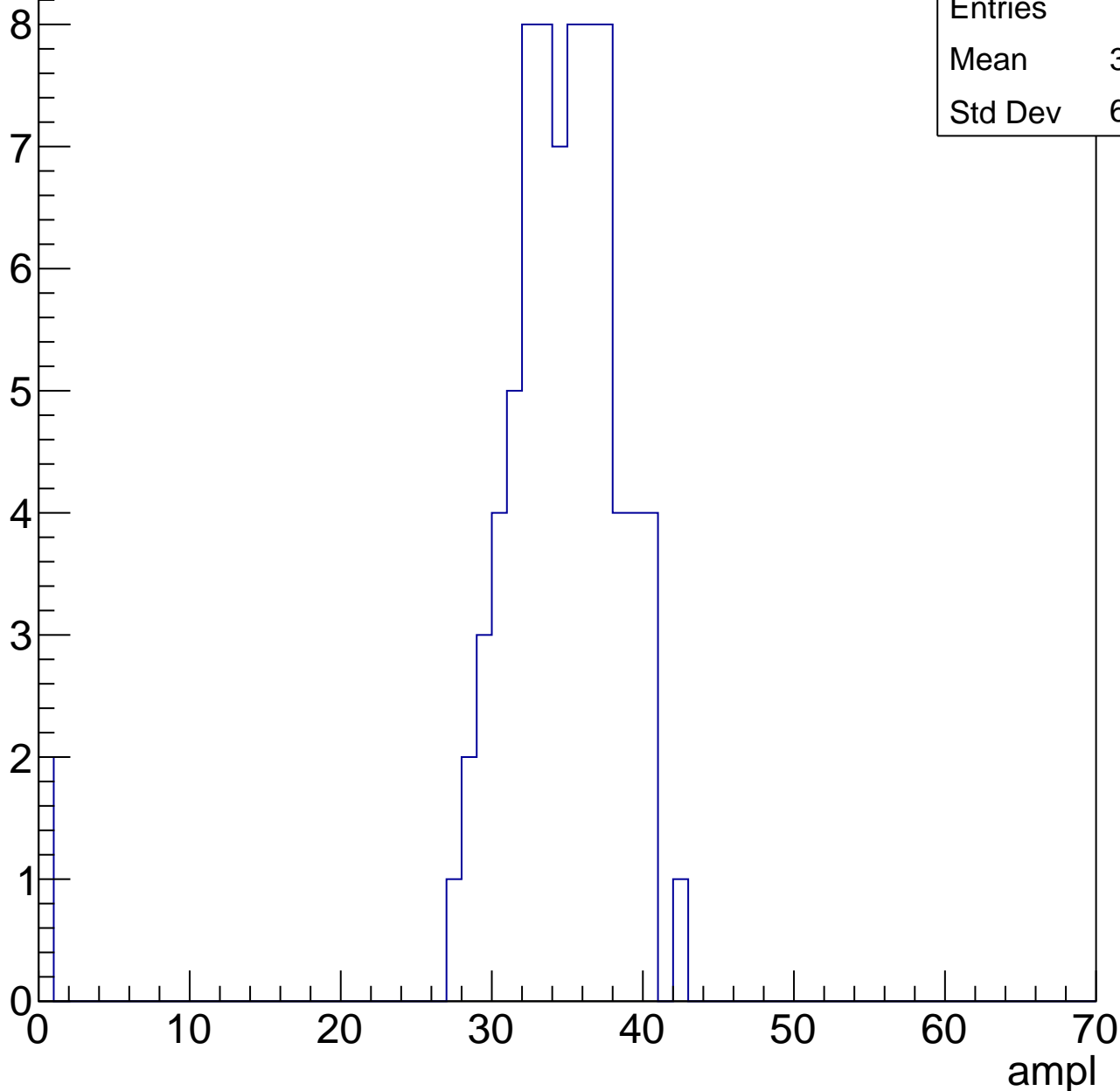


B1L103S, U23-ch32, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	77
Mean	33.47
Std Dev	6.365

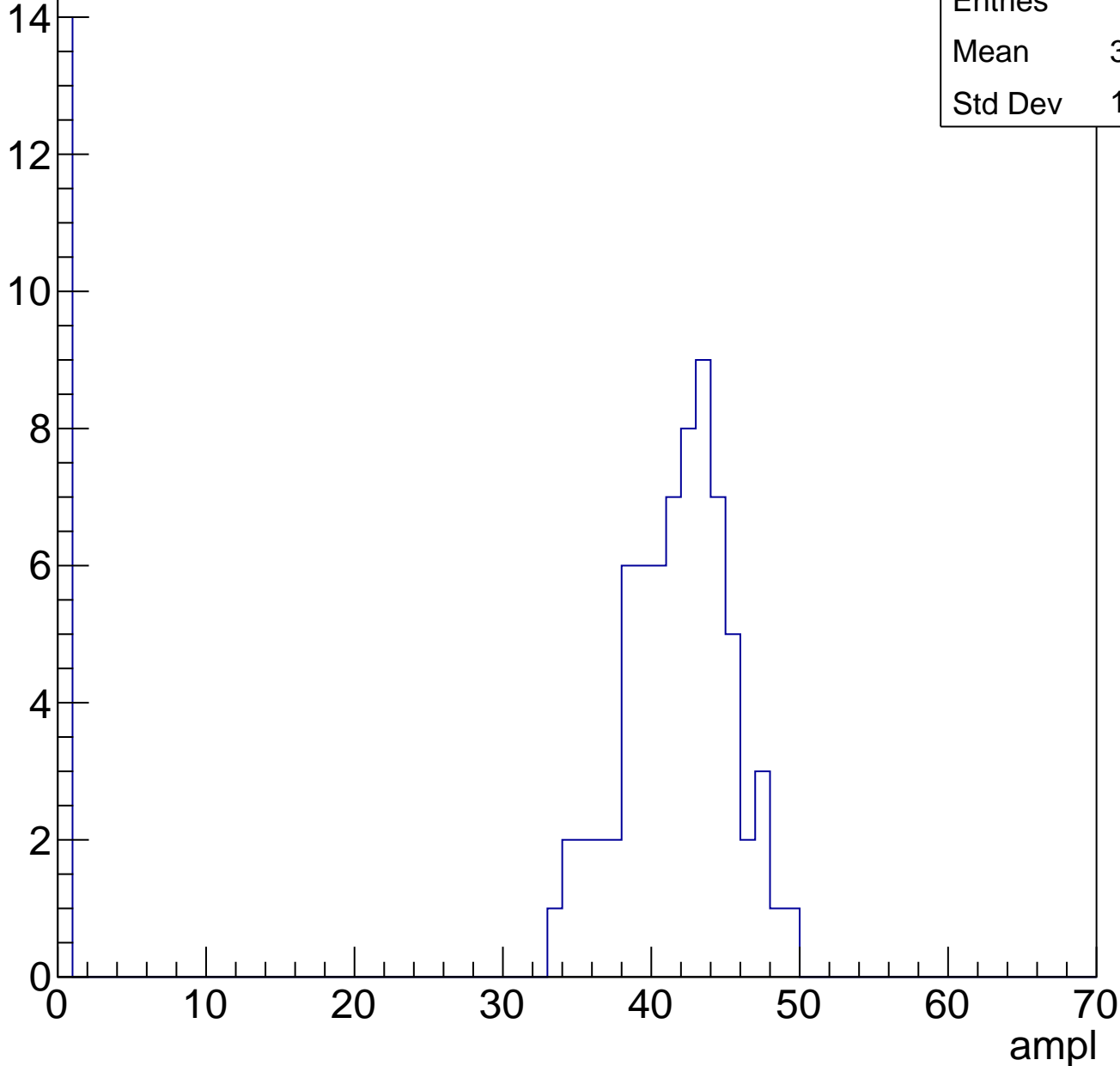


B1L103S, U23-ch32, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	84
Mean	34.43
Std Dev	15.72

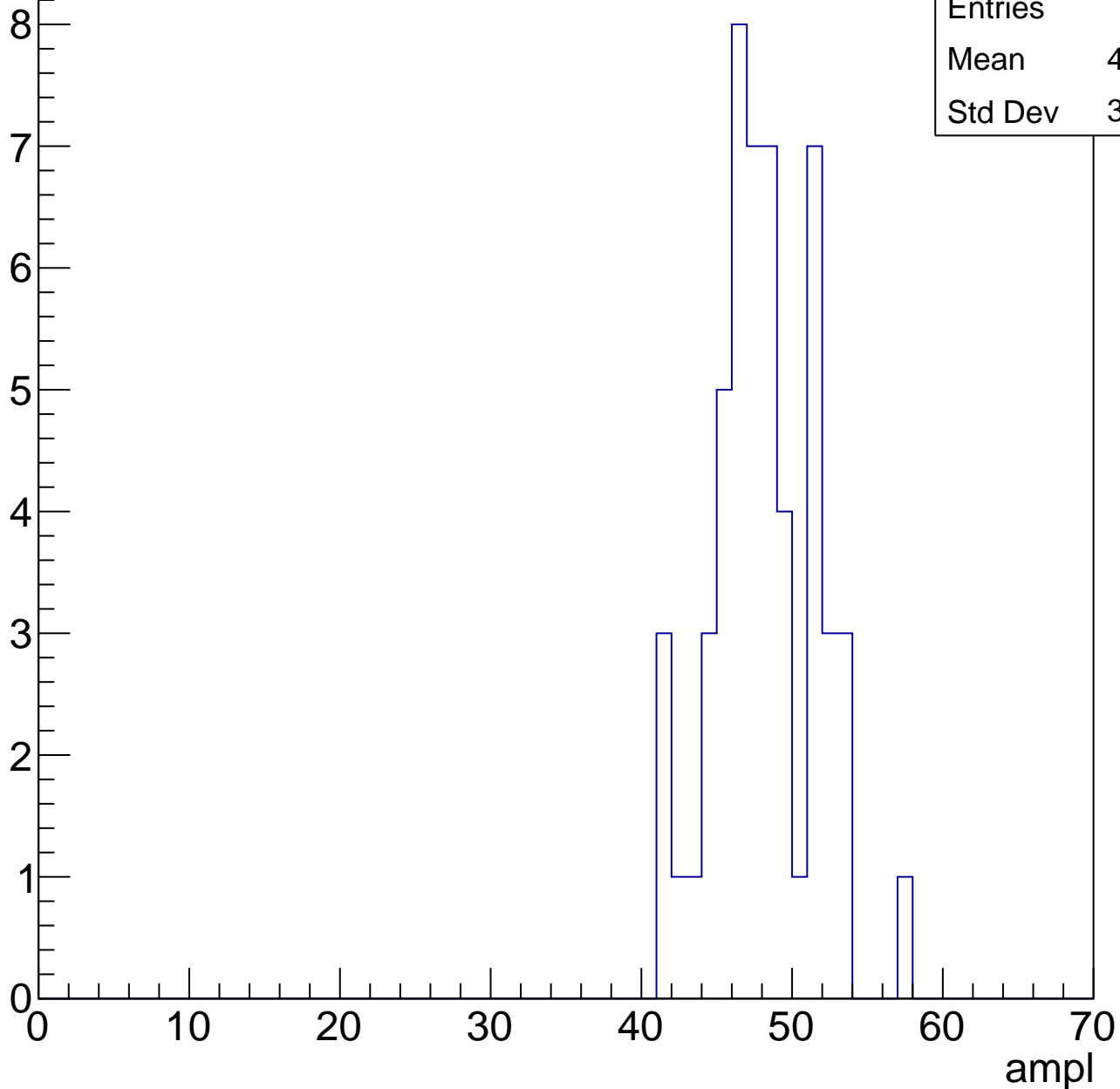
Entry



B1L103S, U23-ch32, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

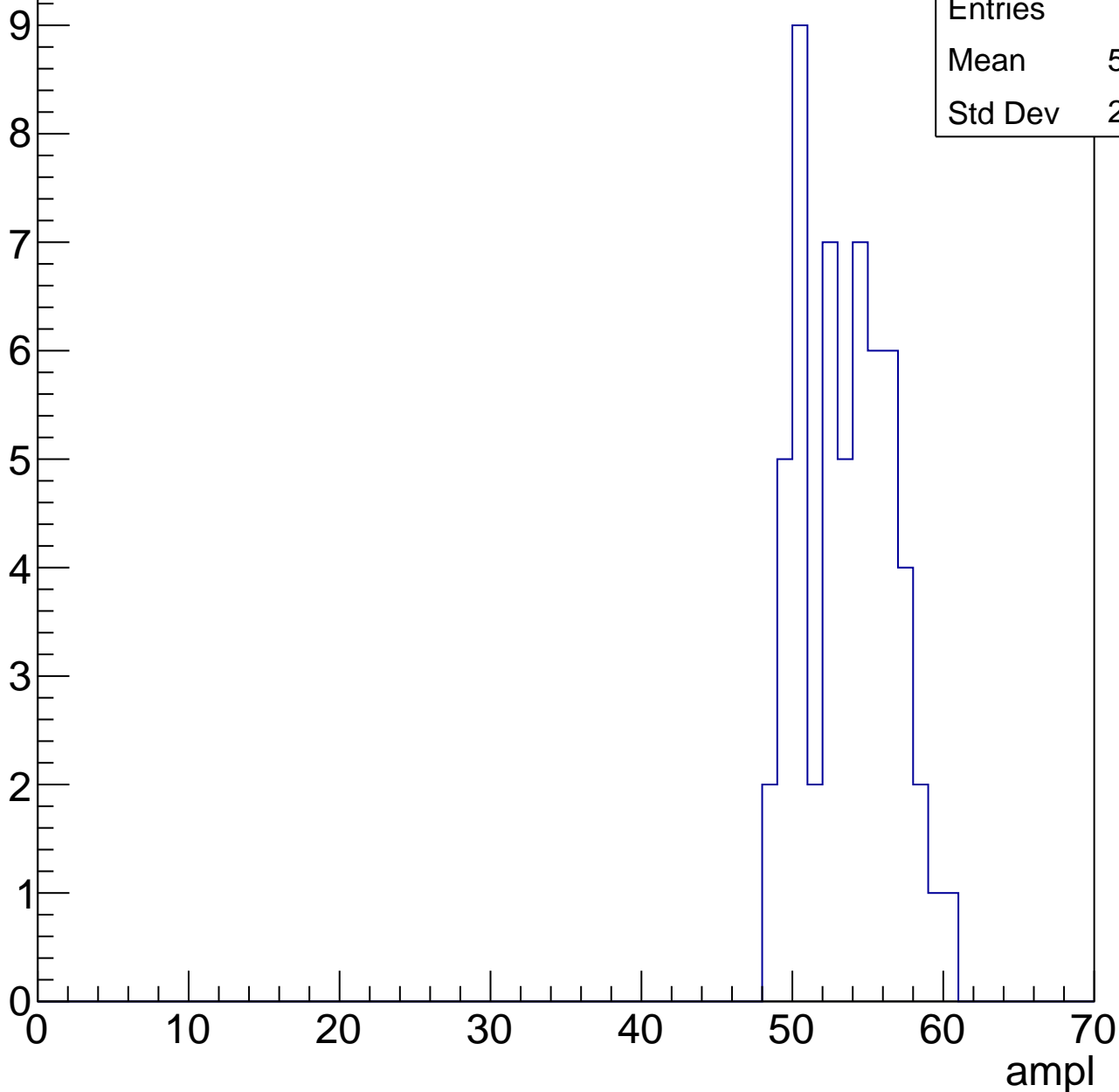


B1L103S, U23-ch32, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

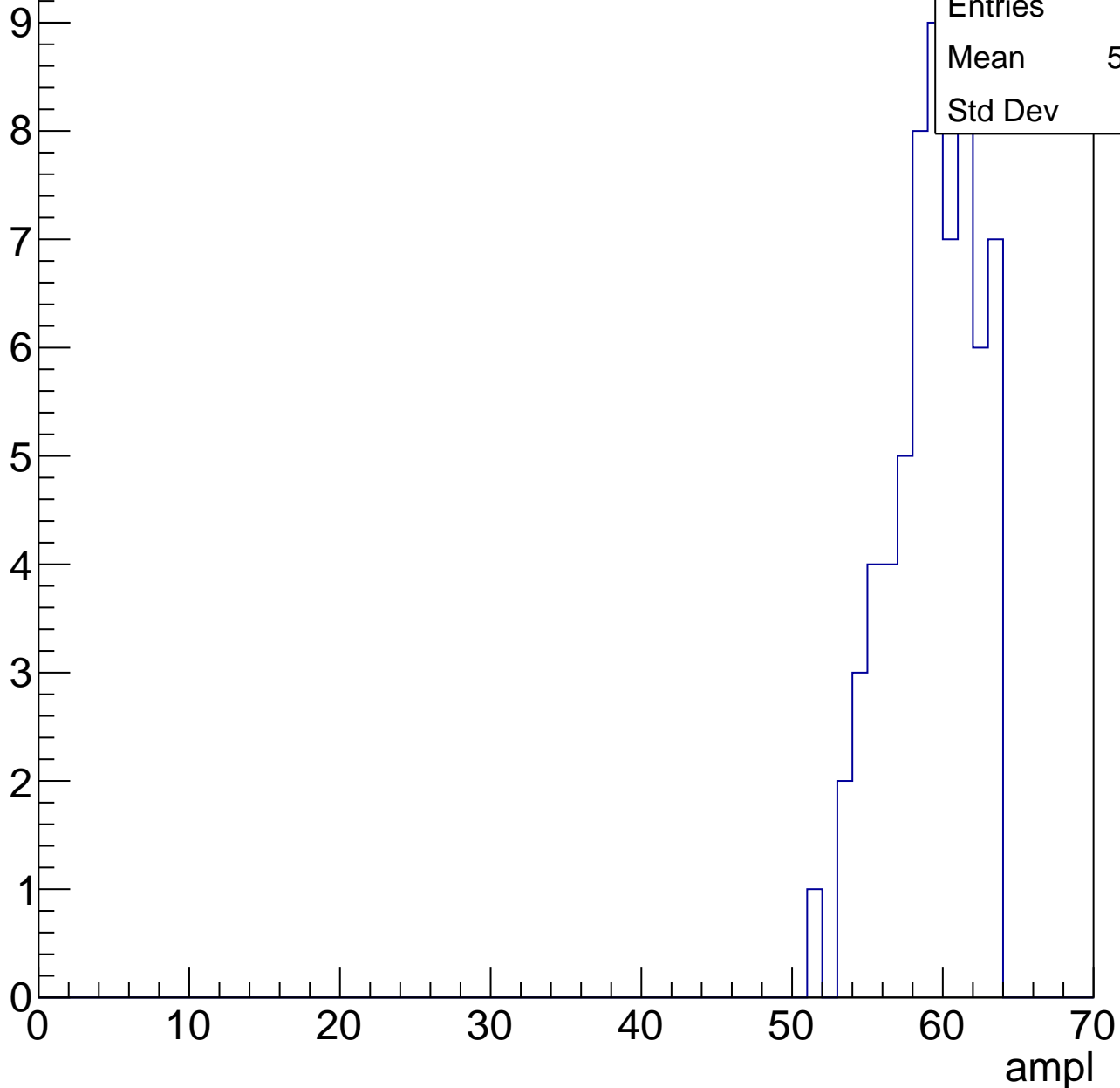
Entries	57
Mean	53.14
Std Dev	2.988



B1L103S, U23-ch32, adc5

calib_packv5_041523_1651.root, FC#0, port C2

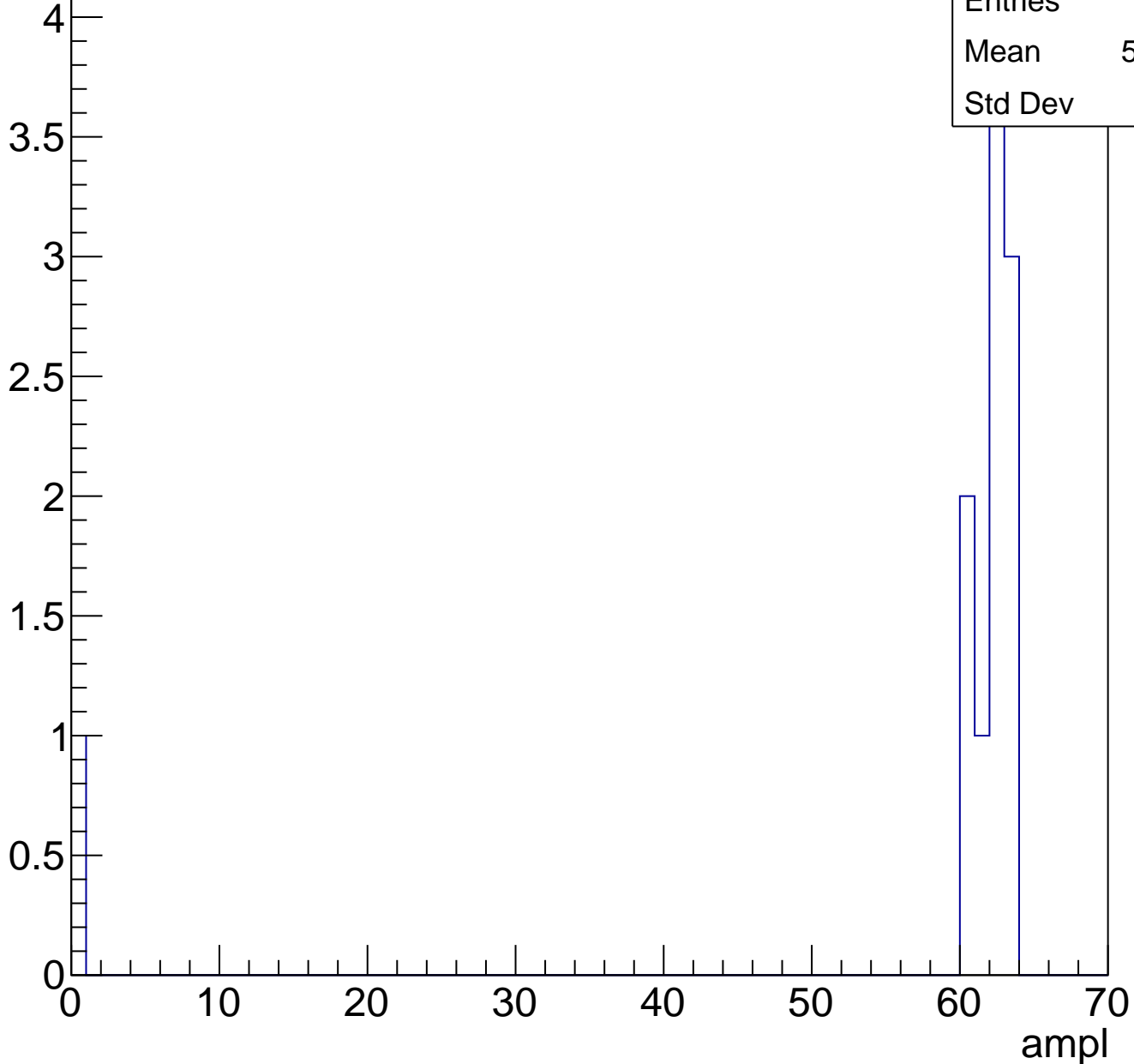
Entry



B1L103S, U23-ch32, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch32, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

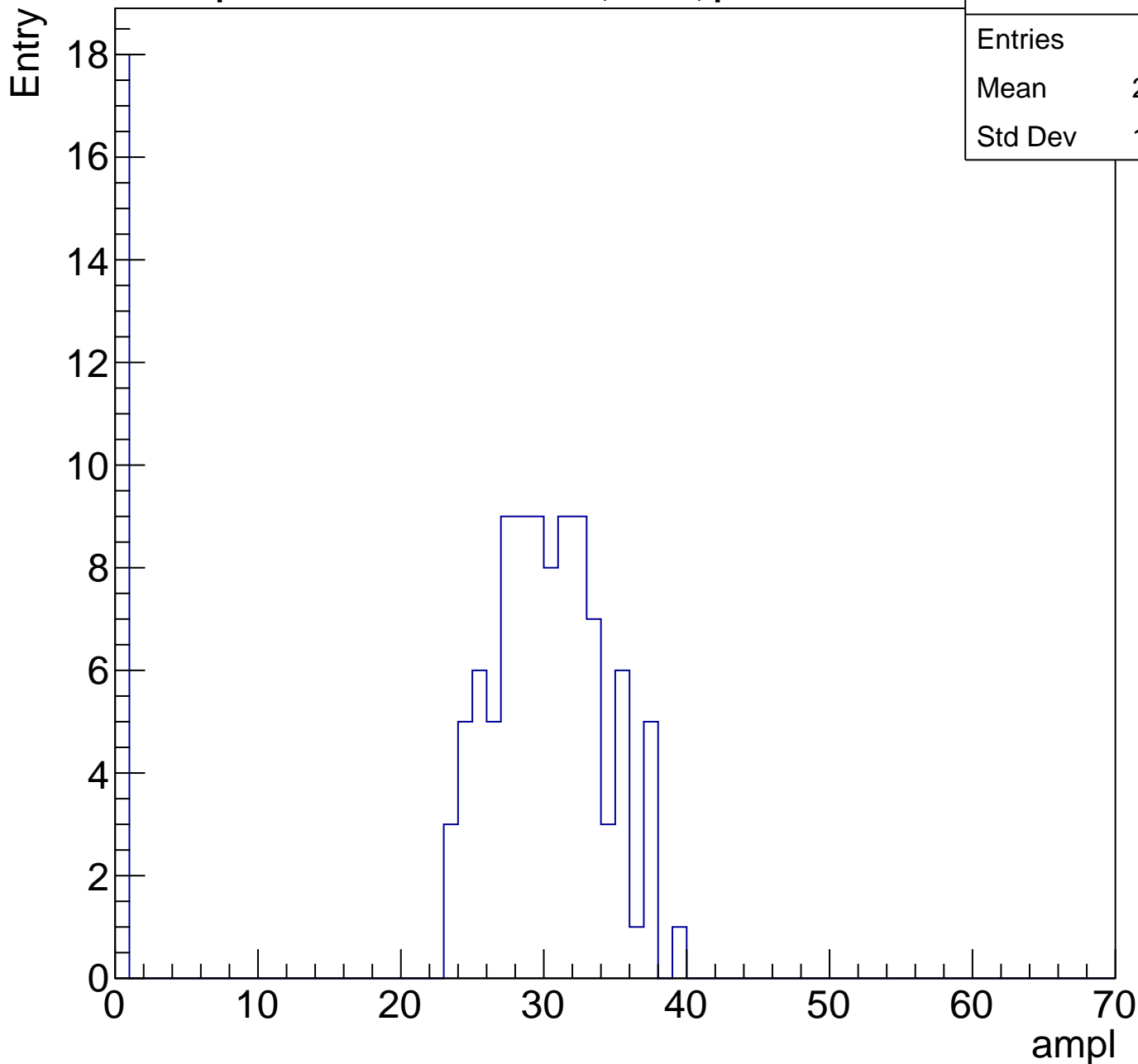
ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U23-ch33, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	113
Mean	25.09
Std Dev	11.45

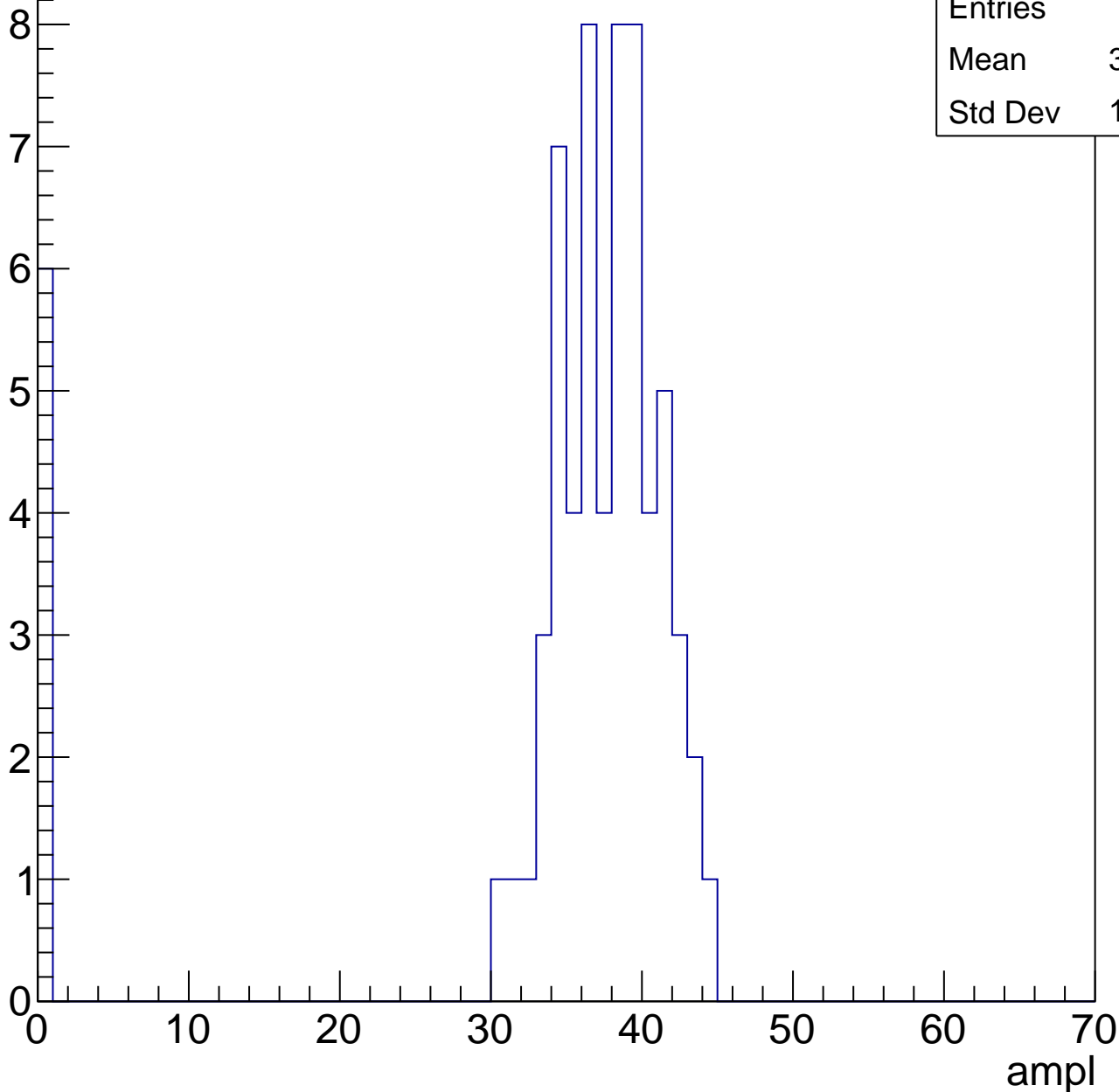


B1L103S, U23-ch33, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	33.98
Std Dev	11.15



B1L103S, U23-ch33, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

70

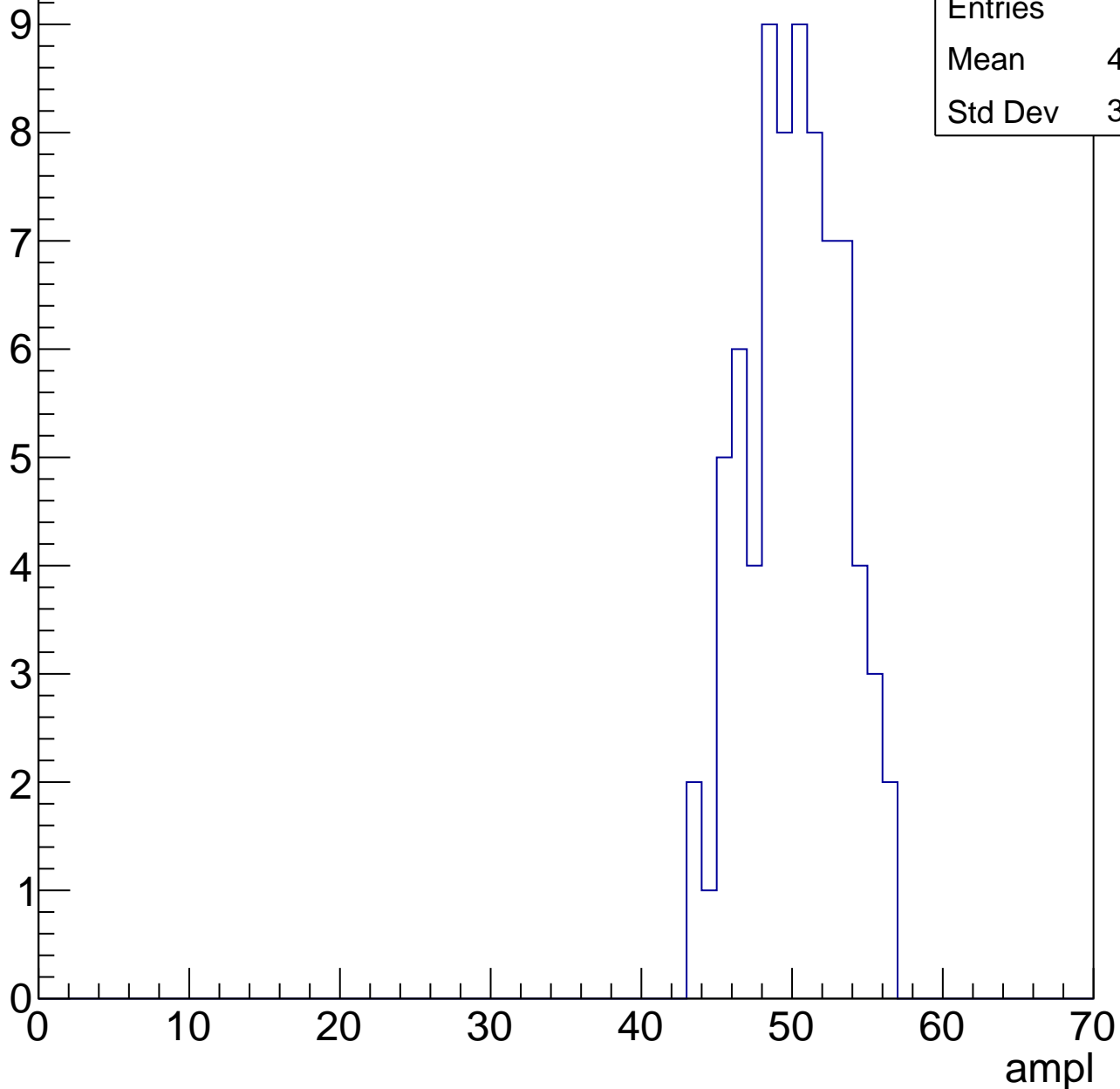
ampl

Entries	66
Mean	36
Std Dev	16.34

B1L103S, U23-ch33, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry



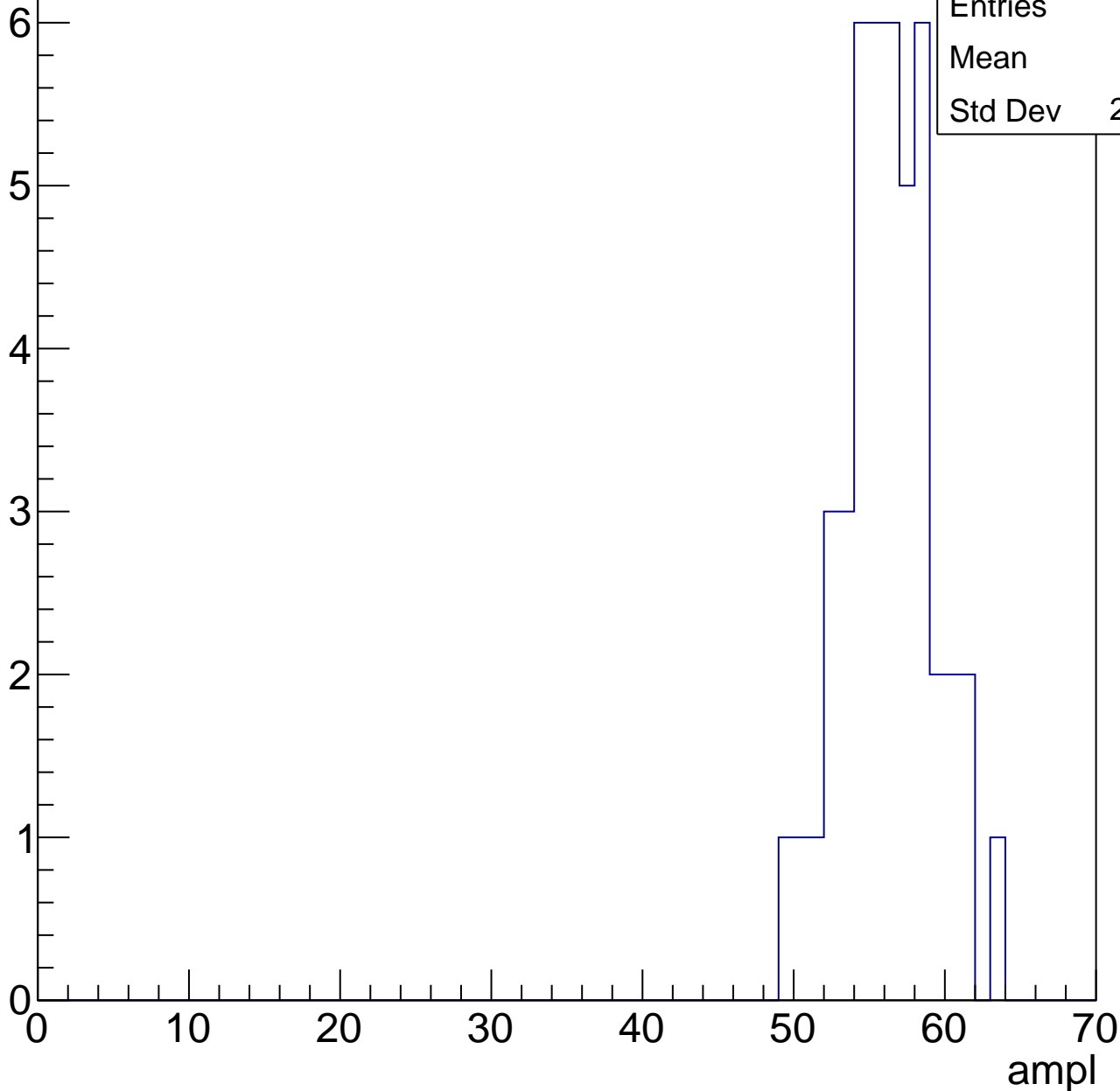
Entries	75
Mean	49.72
Std Dev	3.139

B1L103S, U23-ch33, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	45
Mean	55.8
Std Dev	2.948

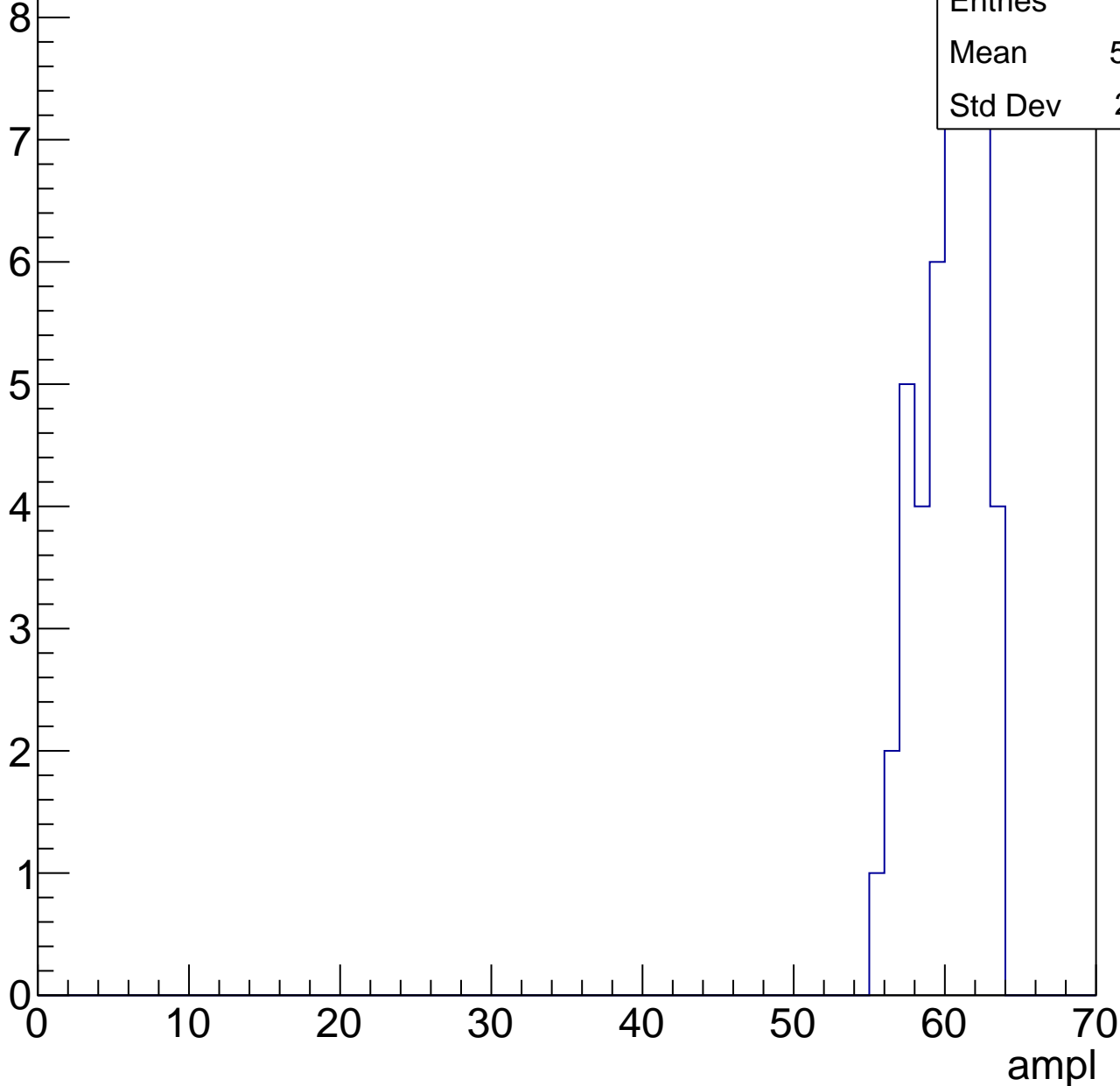


B1L103S, U23-ch33, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	46
Mean	59.87
Std Dev	2.081

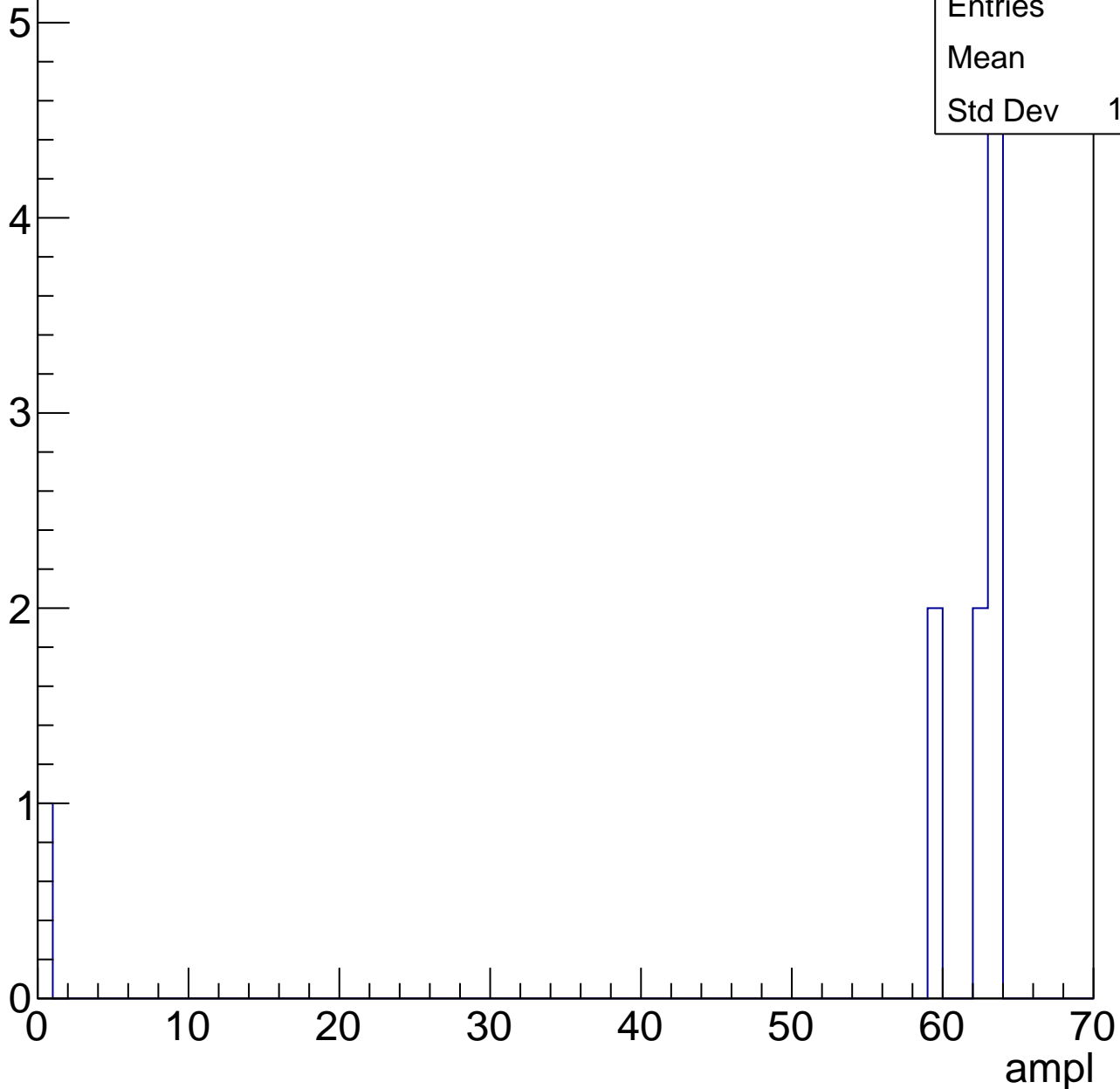


B1L103S, U23-ch33, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	10
Mean	55.7
Std Dev	18.63



B1L103S, U23-ch33, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

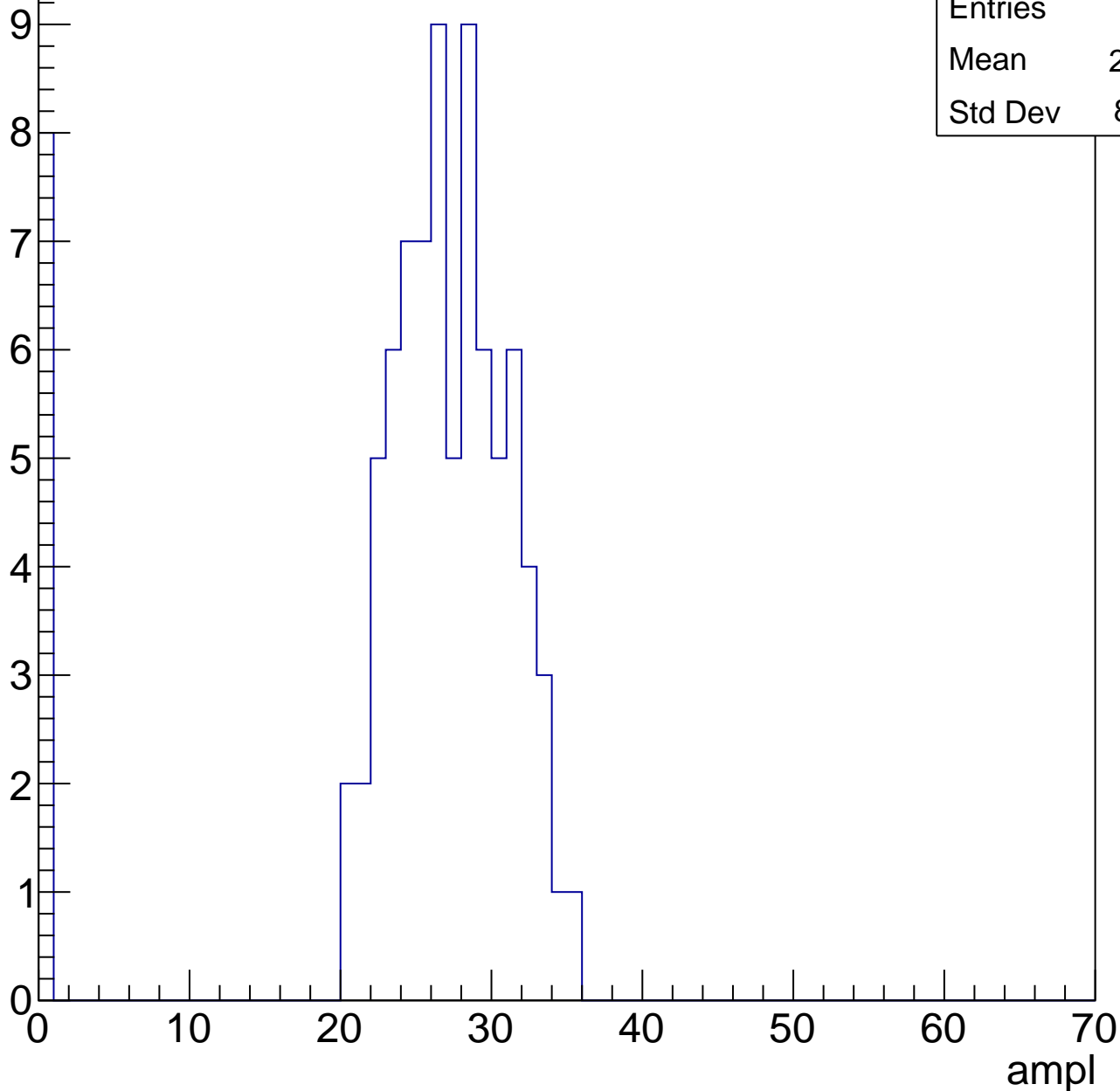
Entries	19
Mean	0
Std Dev	0

B1L103S, U23-ch34, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

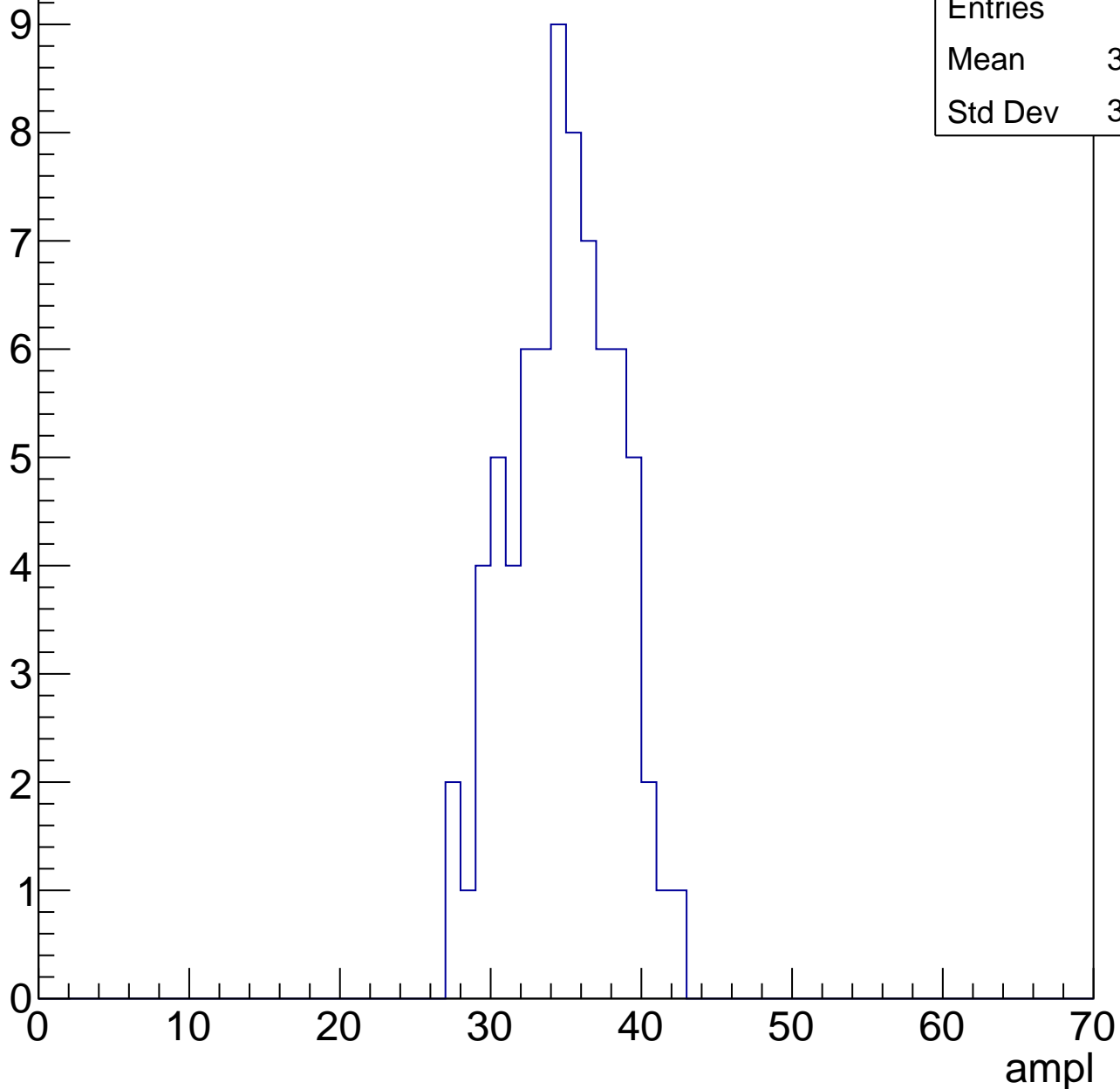
Entries	86
Mean	24.42
Std Dev	8.521



B1L103S, U23-ch34, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry



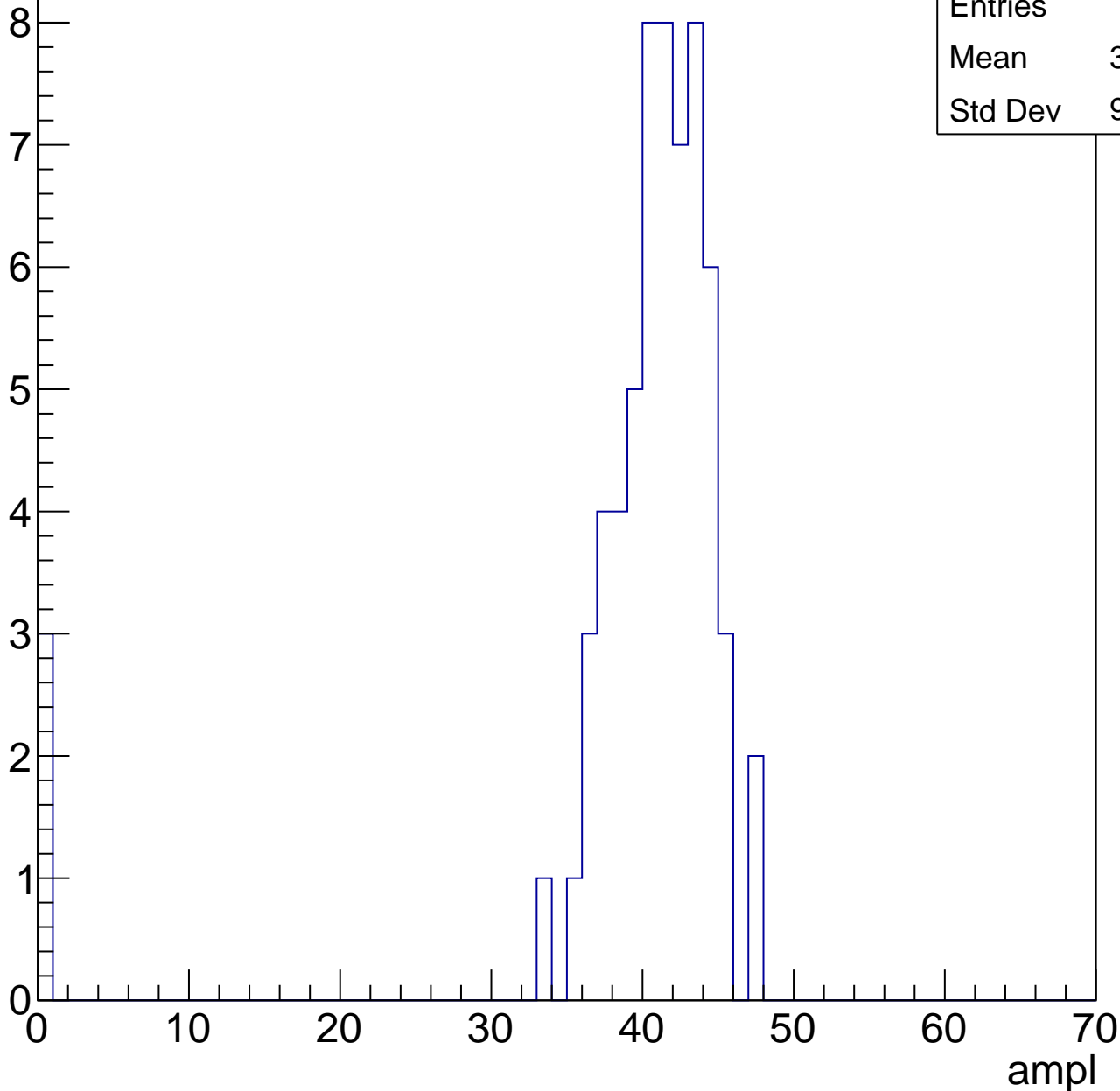
Entries	73
Mean	34.36
Std Dev	3.446

B1L103S, U23-ch34, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	63
Mean	38.89
Std Dev	9.153



B1L103S, U23-ch34, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	74
Mean	40.34
Std Dev	17.06

Entry

10

8

6

4

2

0

0

10

20

30

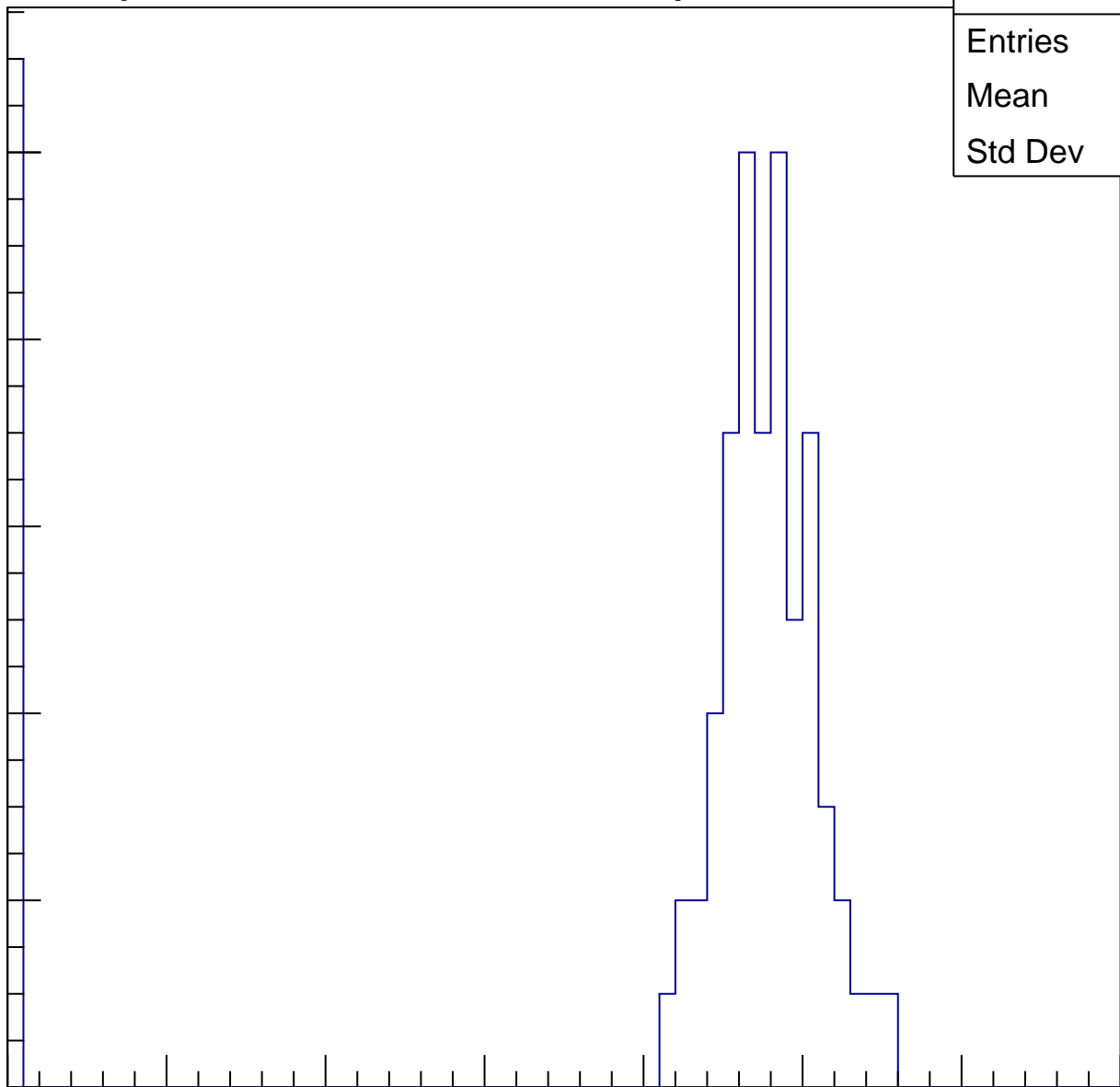
40

50

60

70

ampl

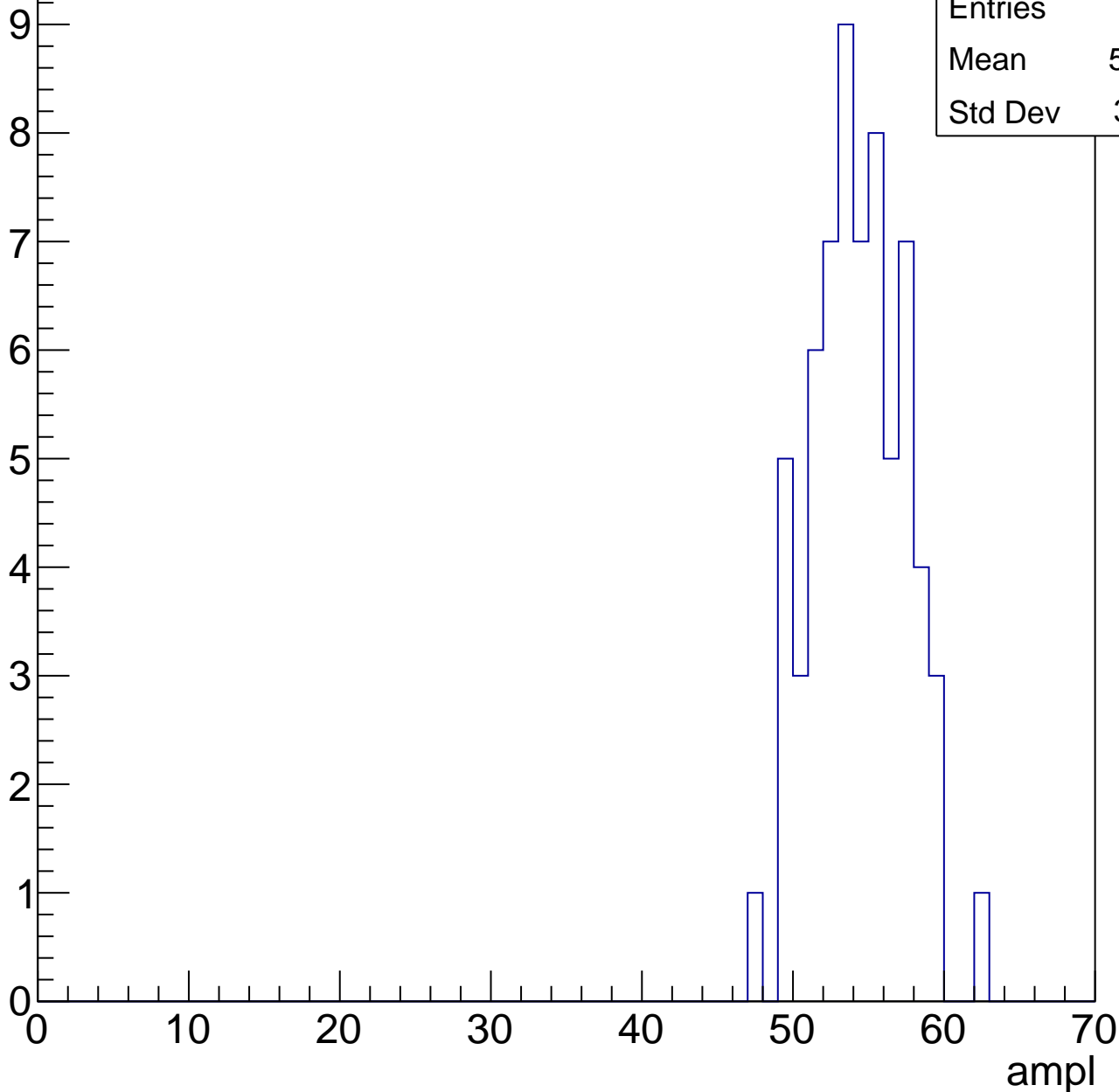


B1L103S, U23-ch34, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	53.89
Std Dev	3.031

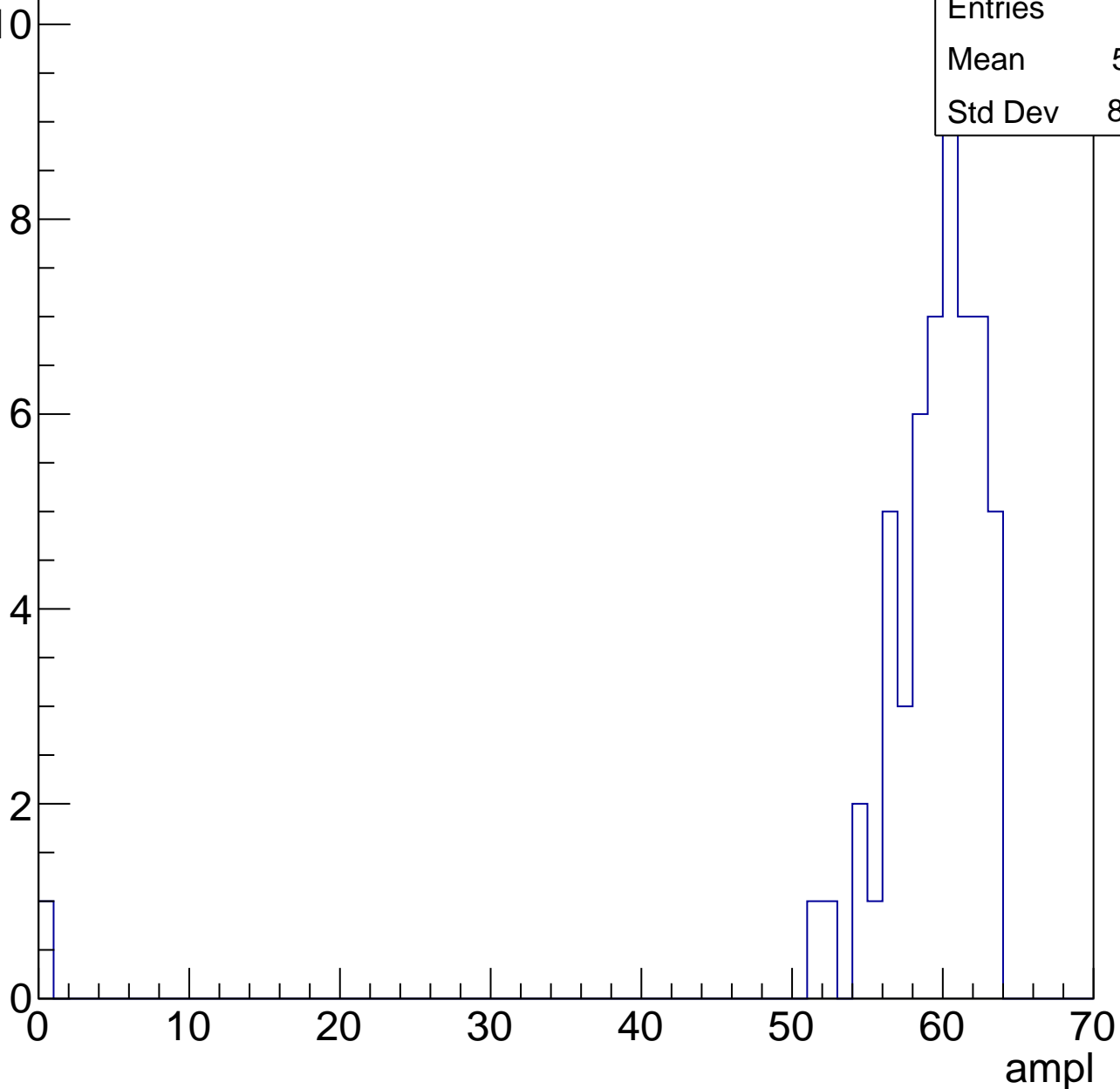


B1L103S, U23-ch34, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	56
Mean	58.11
Std Dev	8.302

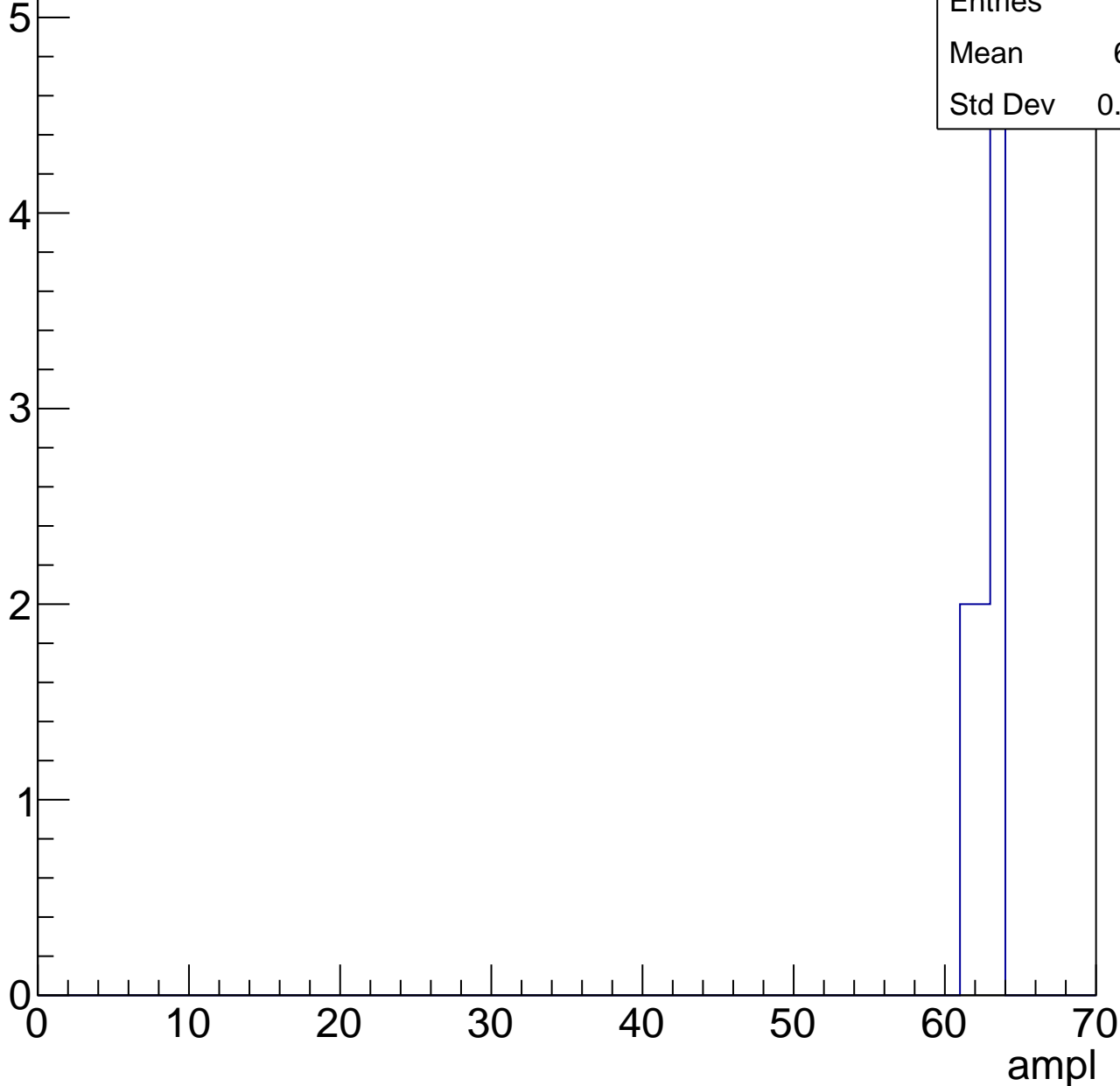


B1L103S, U23-ch34, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	9
Mean	62.33
Std Dev	0.8165



B1L103S, U23-ch34, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.05
Std Dev	13.29

Entry

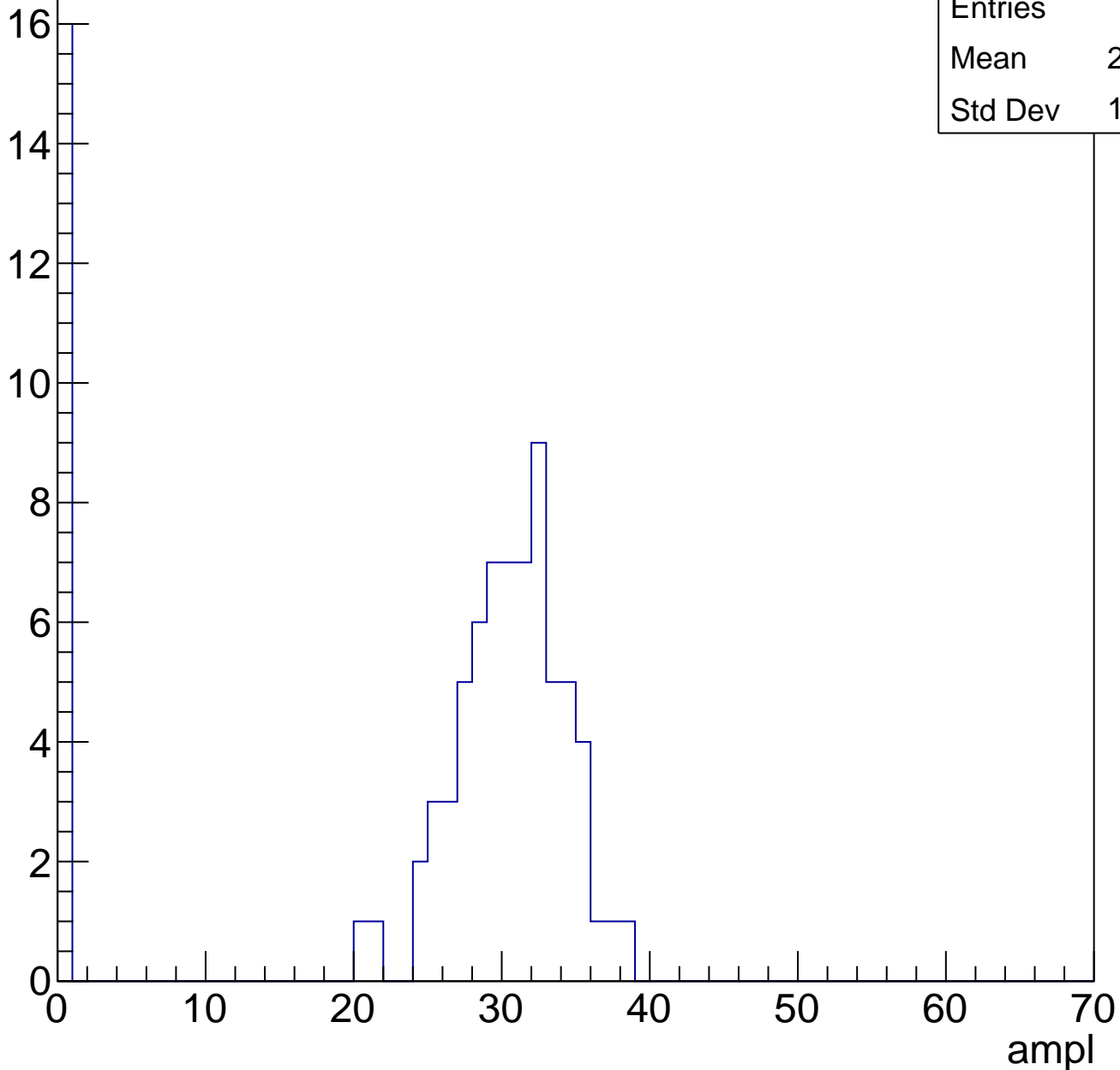


B1L103S, U23-ch35, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	84
Mean	24.39
Std Dev	12.26

Entry

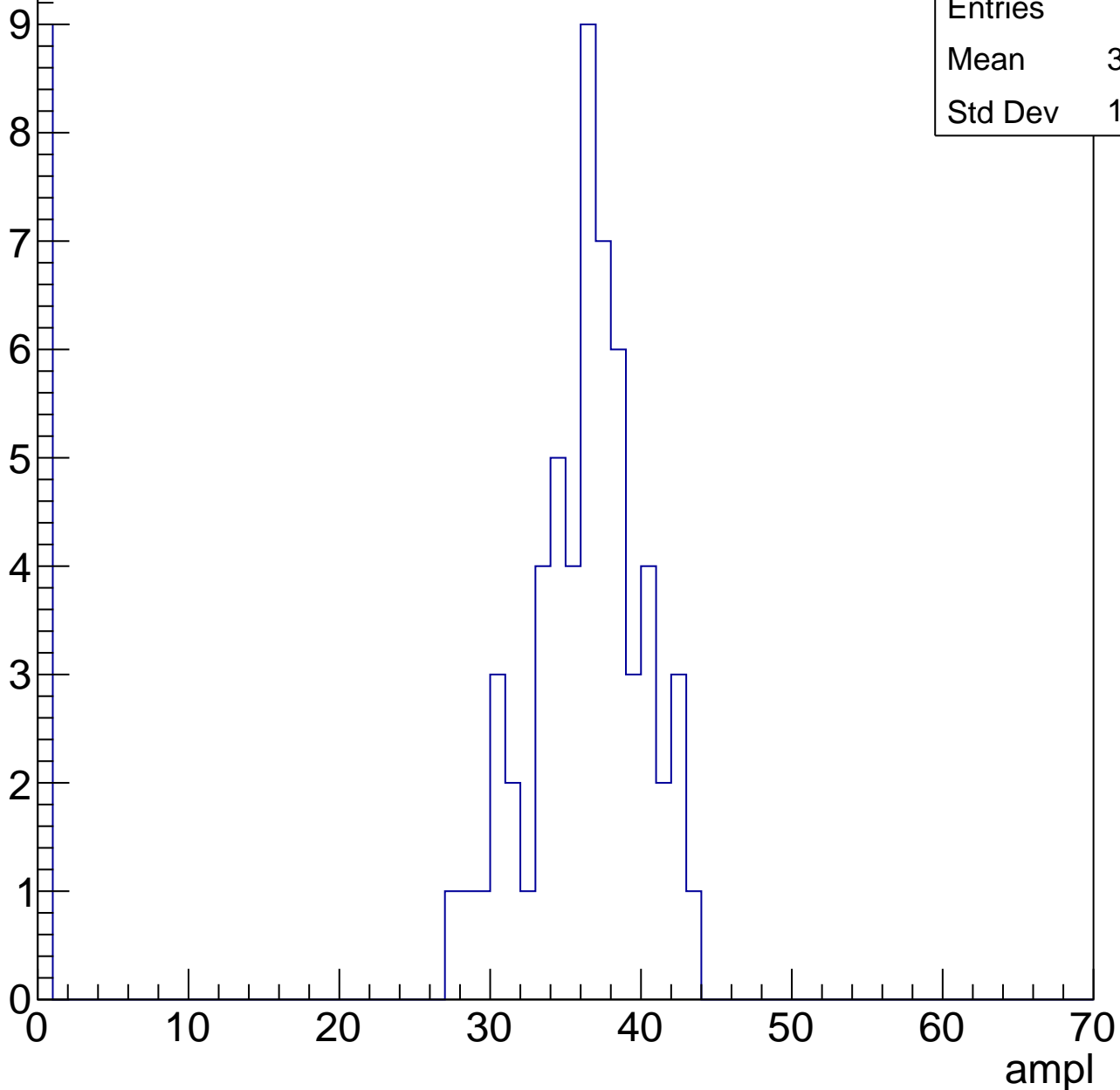


B1L103S, U23-ch35, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	31.05
Std Dev	12.79

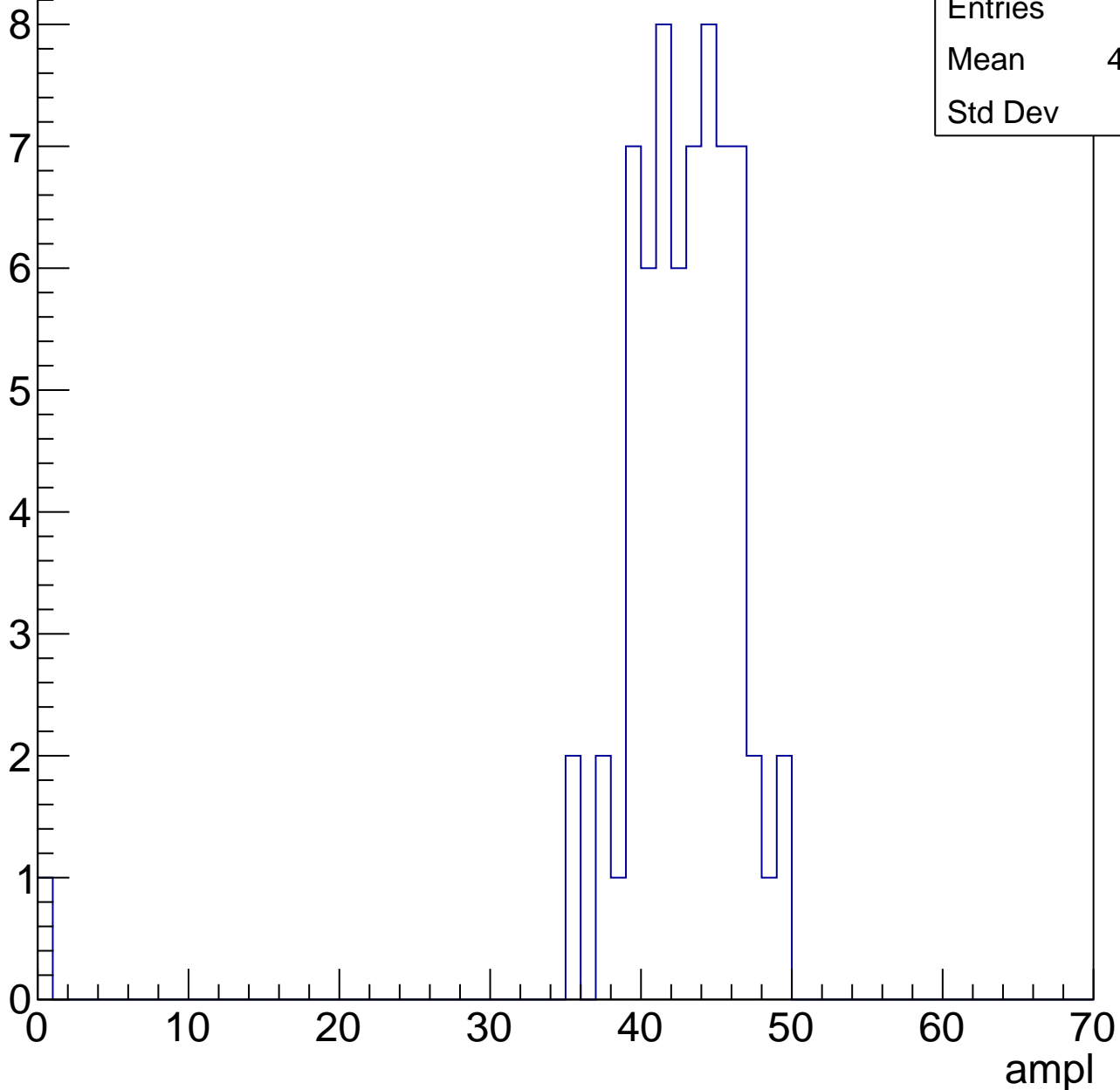


B1L103S, U23-ch35, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	41.87
Std Dev	6.01



B1L103S, U23-ch35, adc3

calib_packv5_041523_1651.root, FC#0, port C2

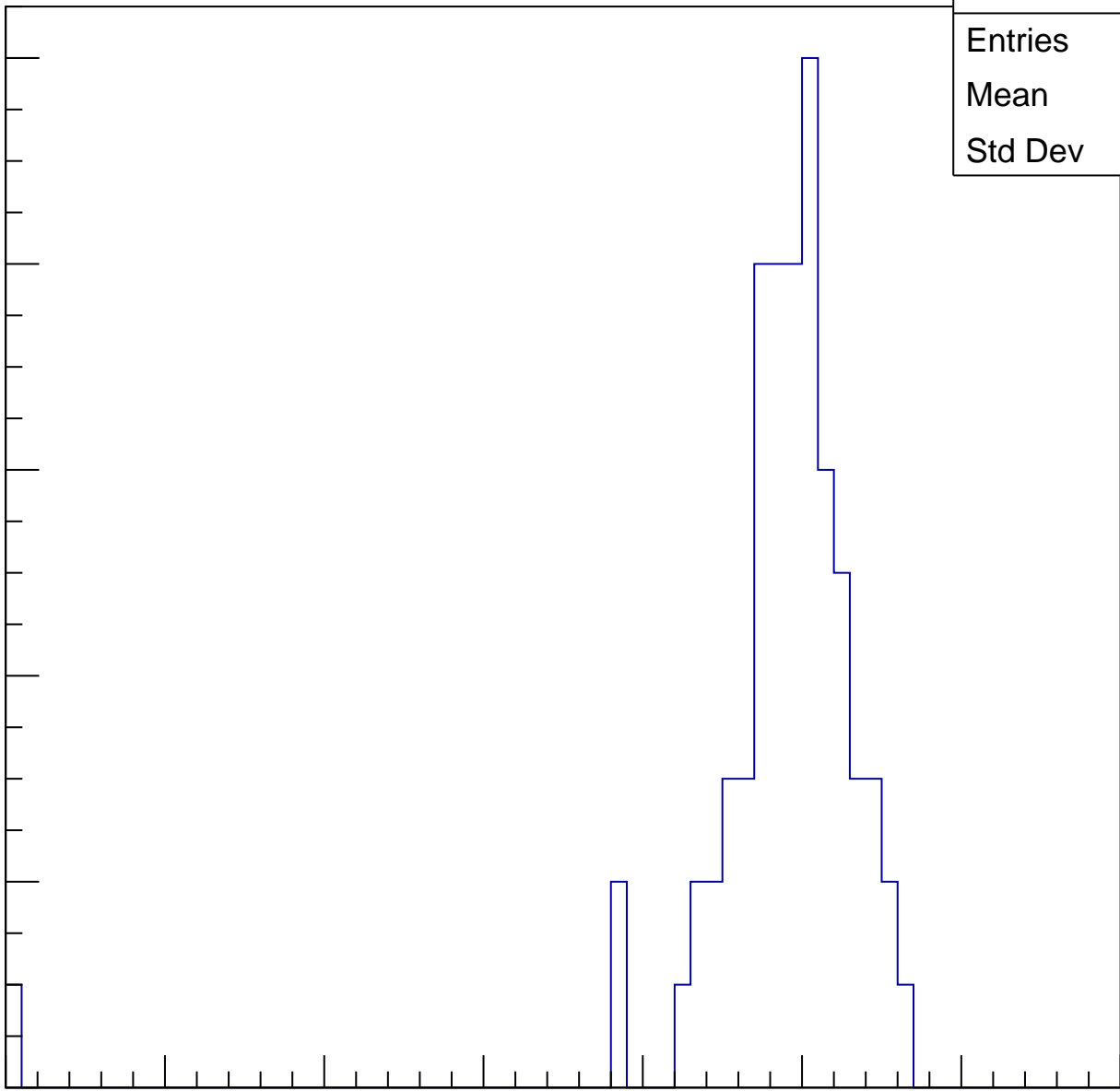
Entries	68
Mean	48.09
Std Dev	6.855

Entry

10
8
6
4
2
0

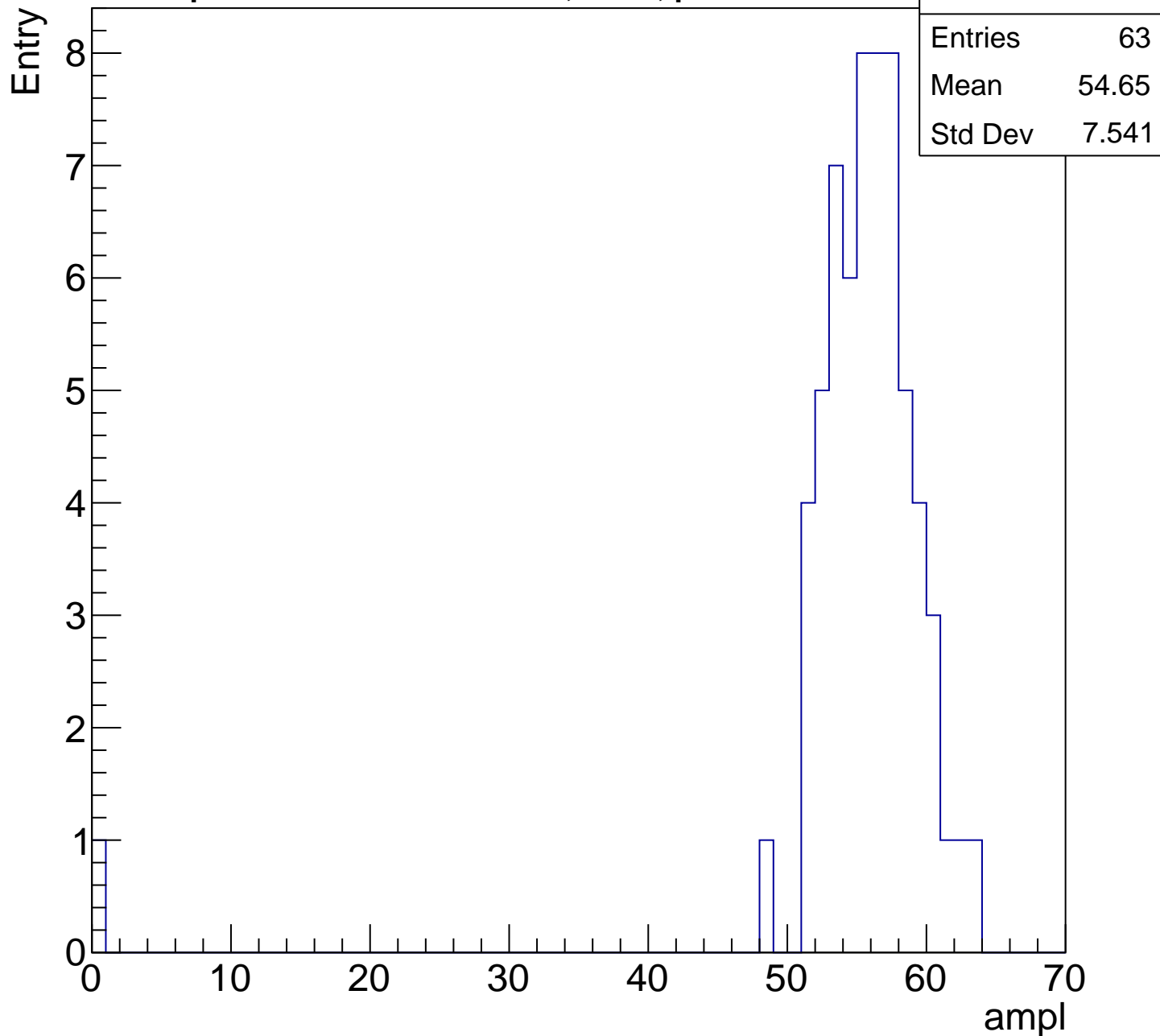
ampl

0 10 20 30 40 50 60 70



B1L103S, U23-ch35, adc4

calib_packv5_041523_1651.root, FC#0, port C2

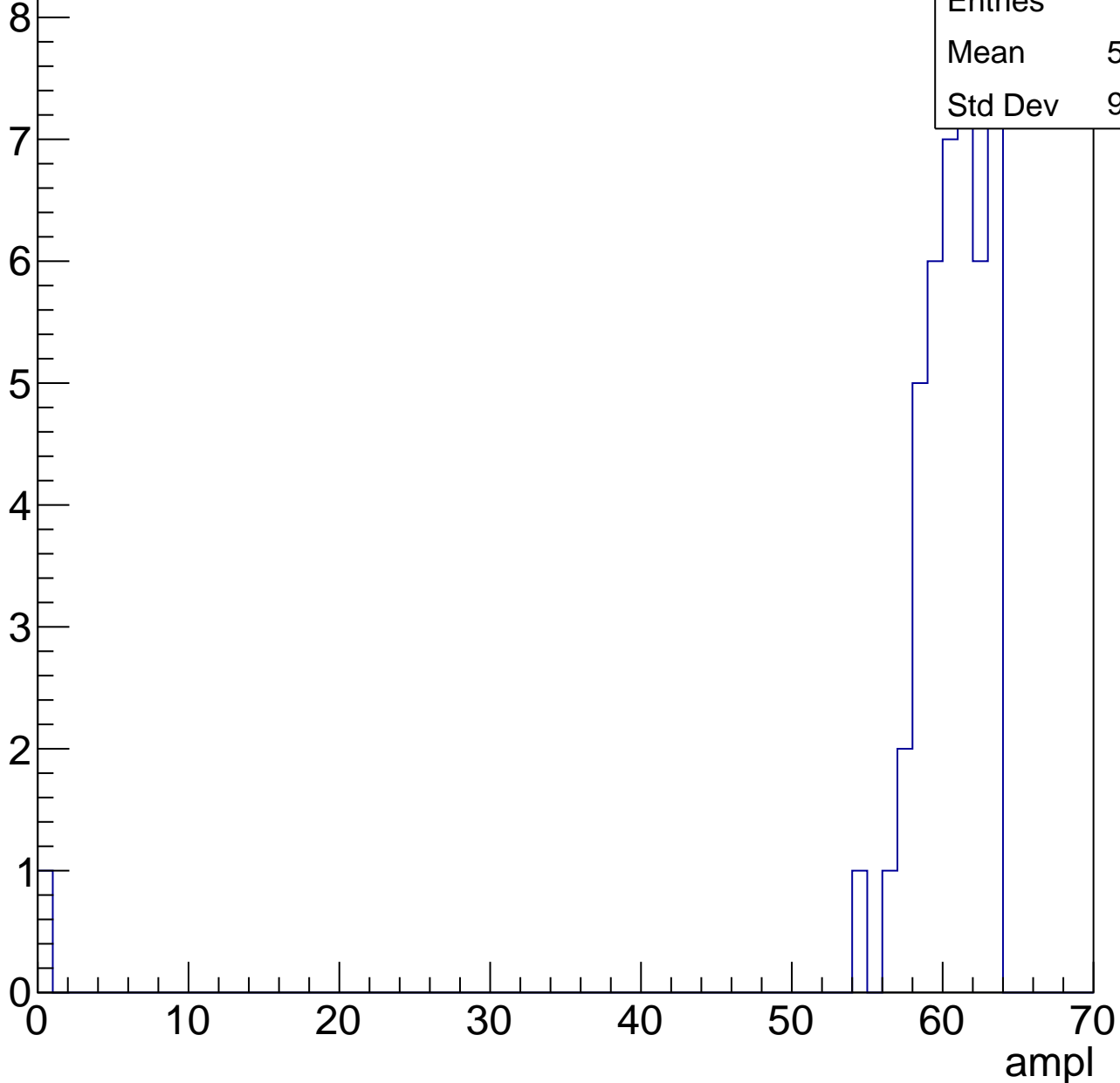


B1L103S, U23-ch35, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	45
Mean	58.93
Std Dev	9.127



B1L103S, U23-ch35, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch35, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	19
Mean	0
Std Dev	0

B1L103S, U23-ch36, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	80
Mean	18.99
Std Dev	13.05

Entry

25
20
15
10
5
0

0

10

20

30

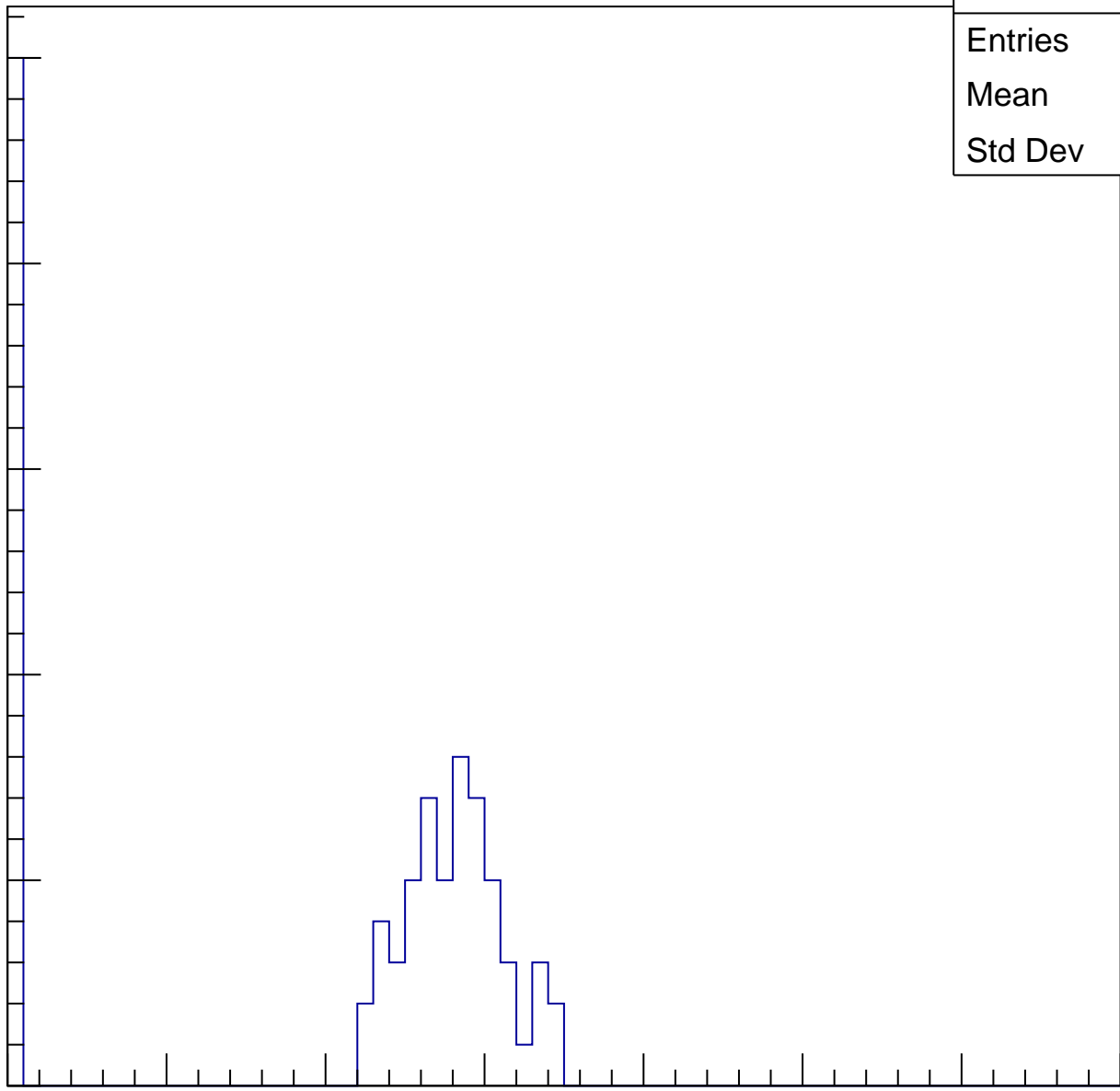
40

50

60

70

ampl

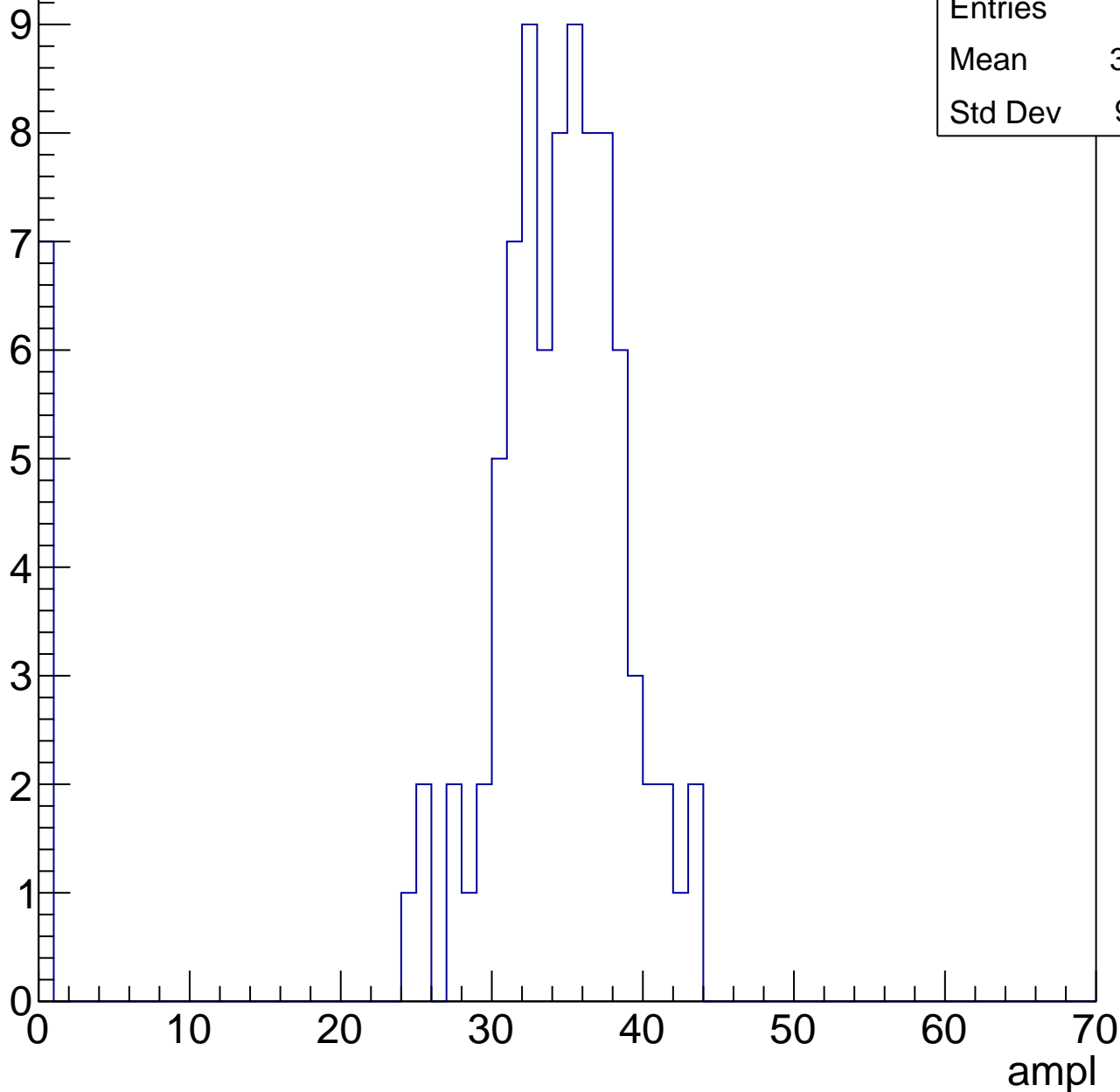


B1L103S, U23-ch36, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	91
Mean	31.57
Std Dev	9.871

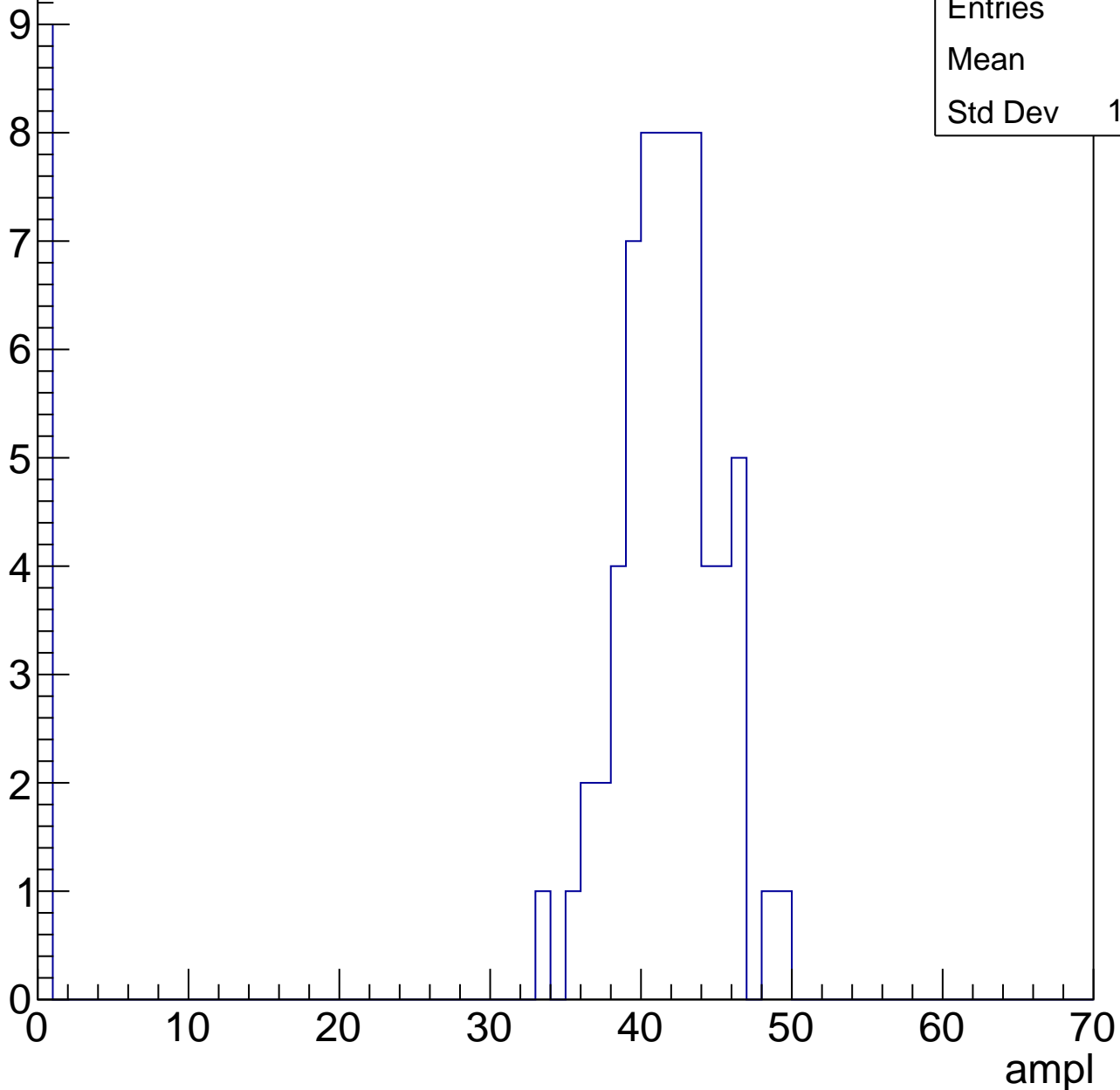


B1L103S, U23-ch36, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	73
Mean	36.3
Std Dev	13.92

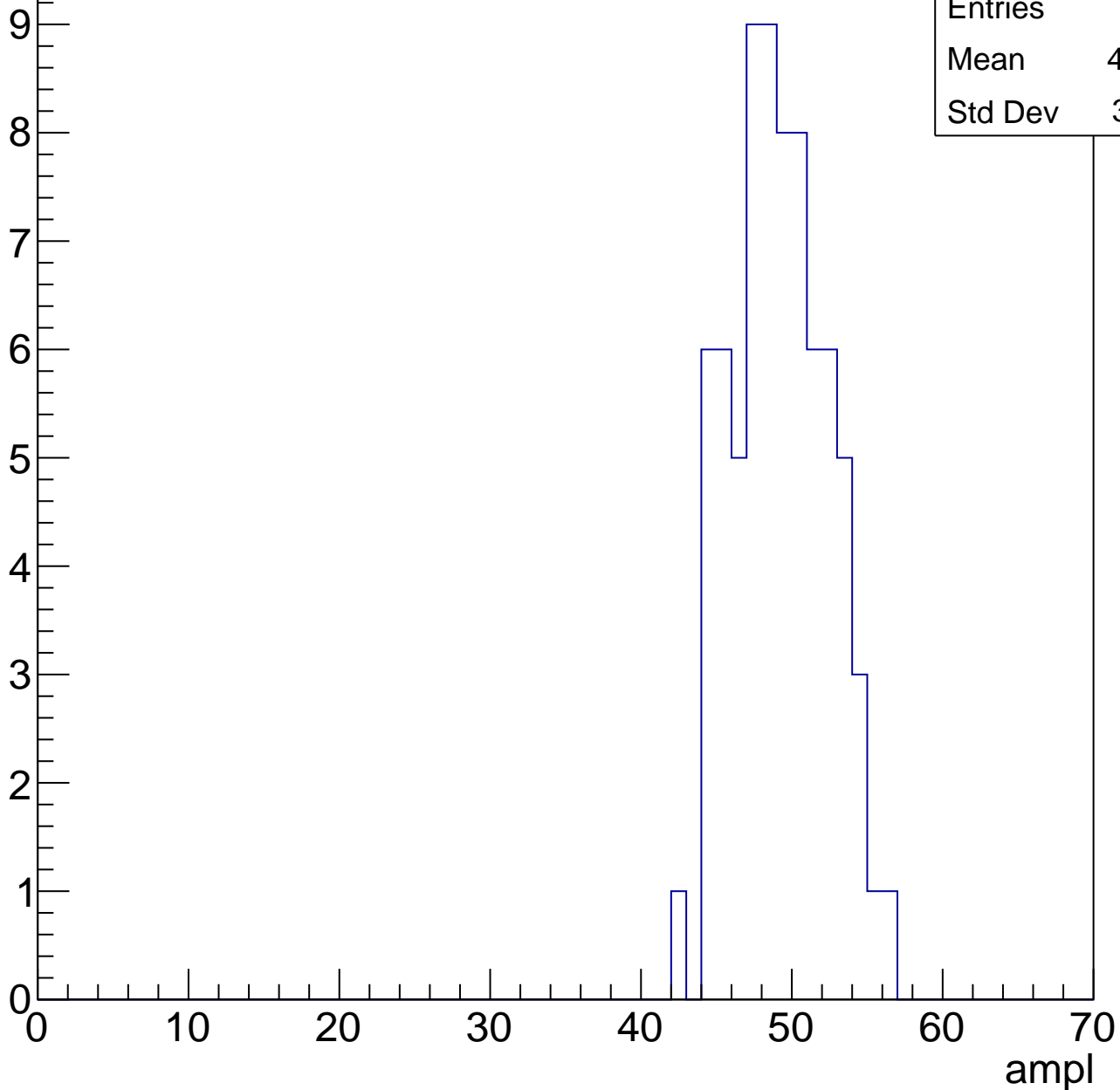


B1L103S, U23-ch36, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	74
Mean	48.77
Std Dev	3.091

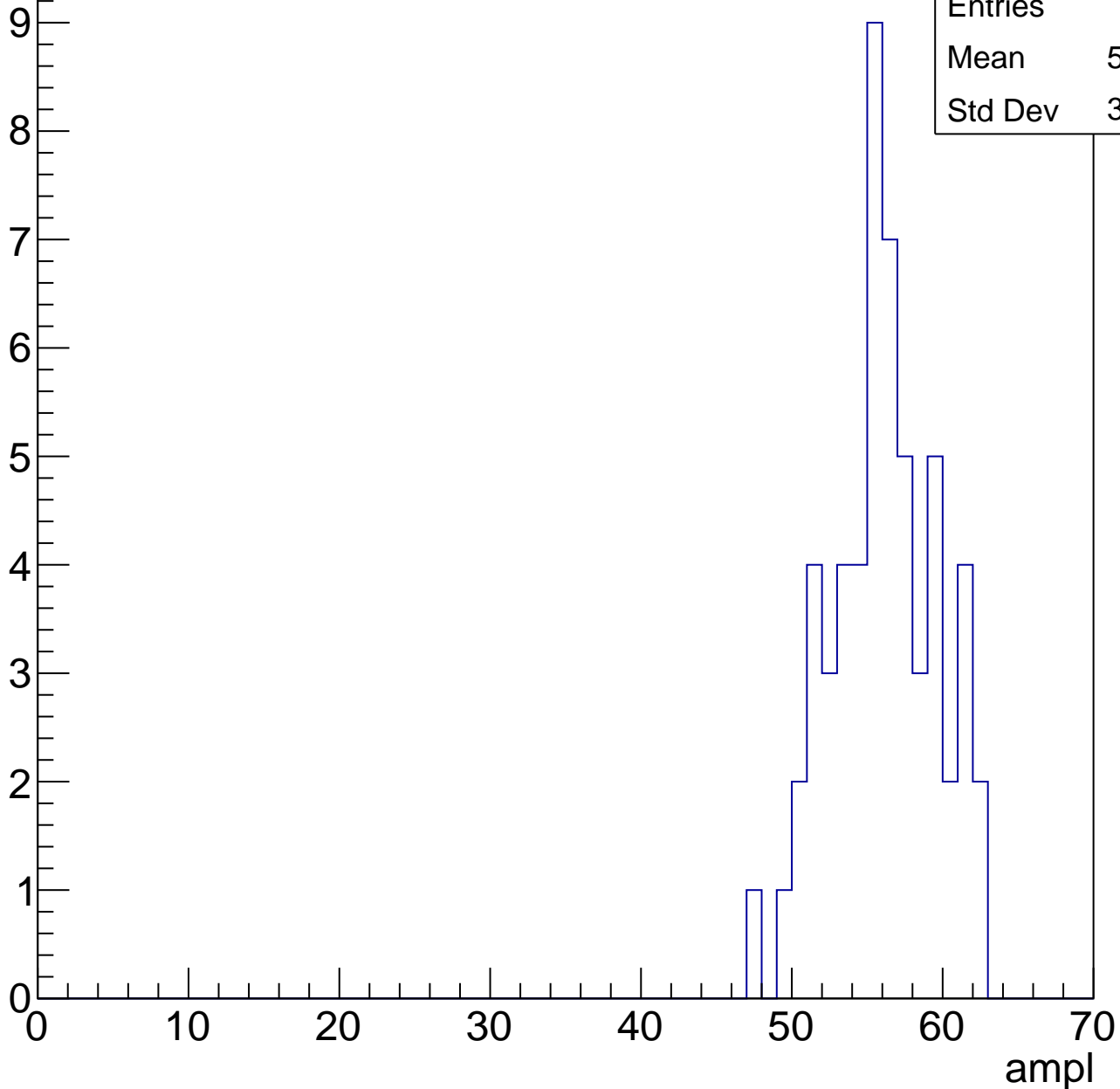


B1L103S, U23-ch36, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

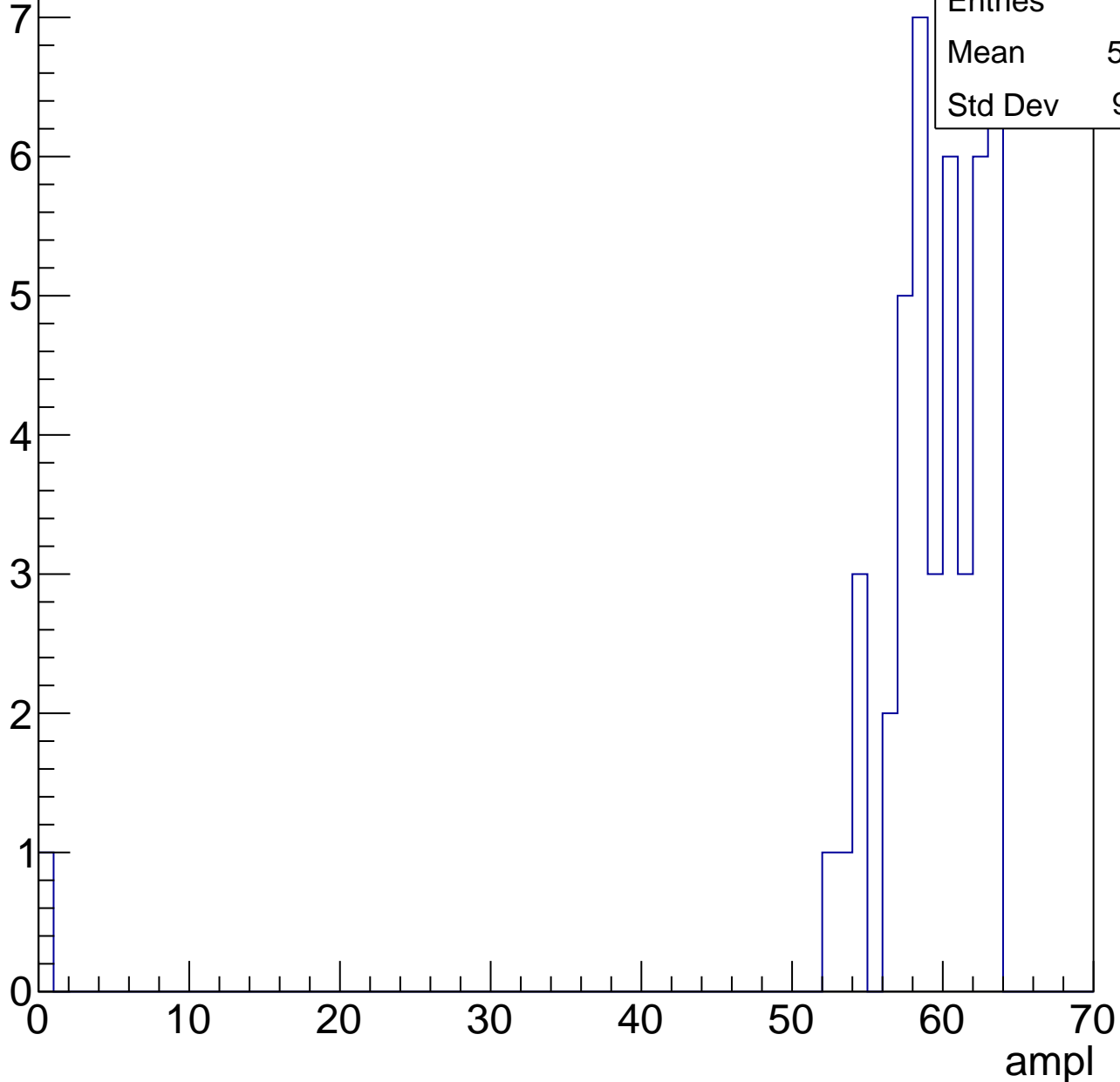
Entries	56
Mean	55.59
Std Dev	3.453



B1L103S, U23-ch36, adc5

calib_packv5_041523_1651.root, FC#0, port C2

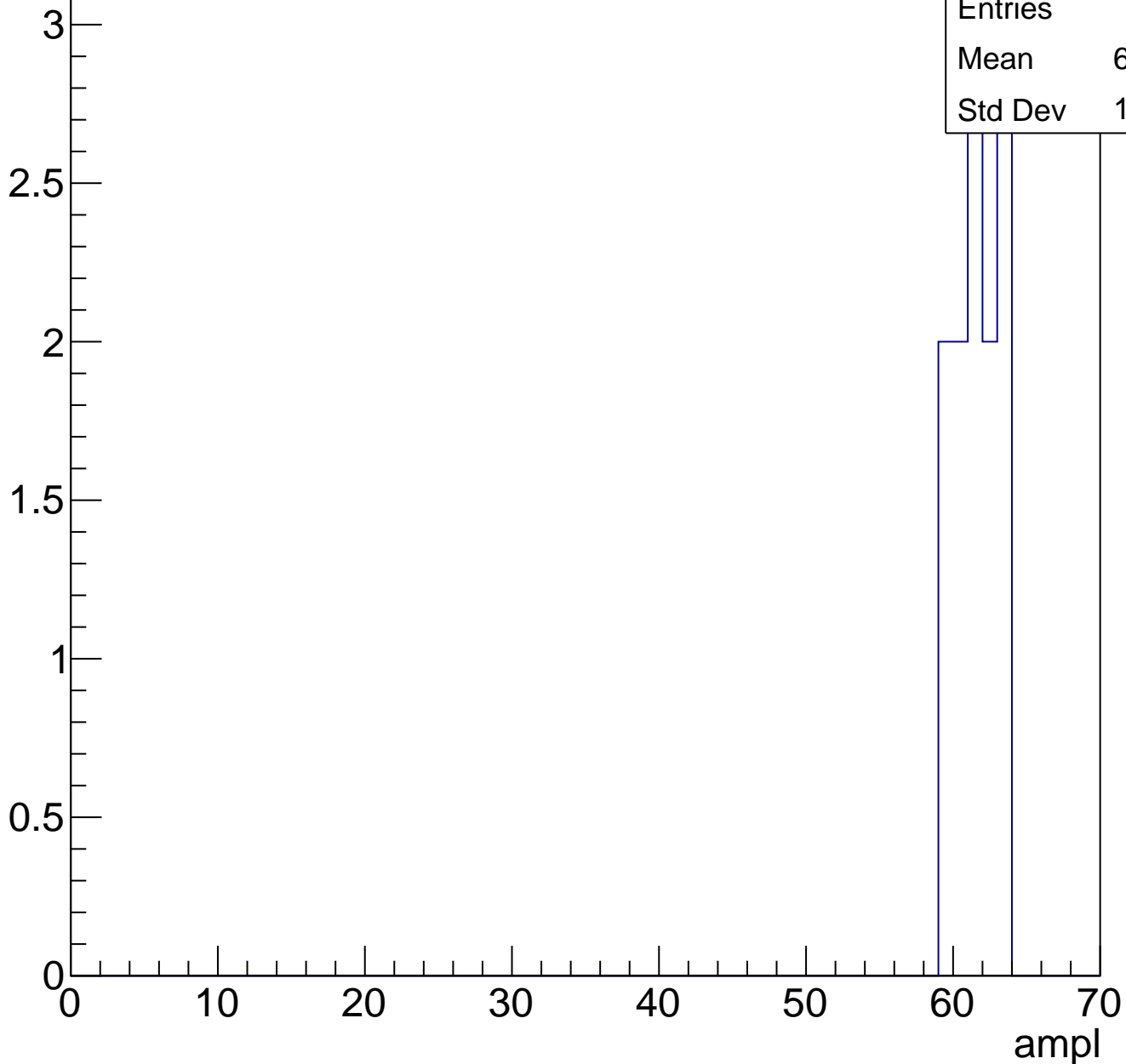
Entry



B1L103S, U23-ch36, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch36, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

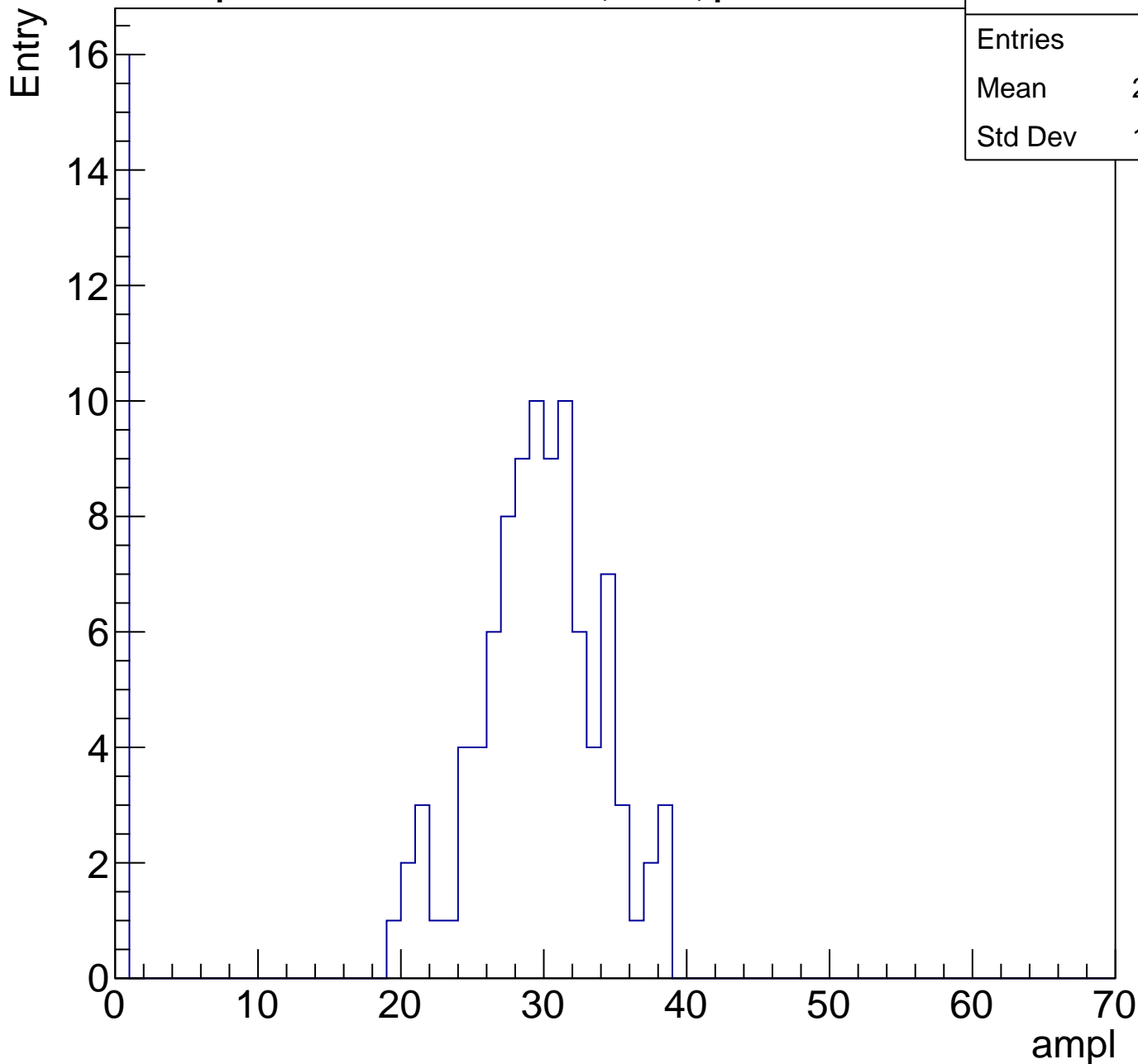
ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U23-ch37, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	110
Mean	24.98
Std Dev	11.02

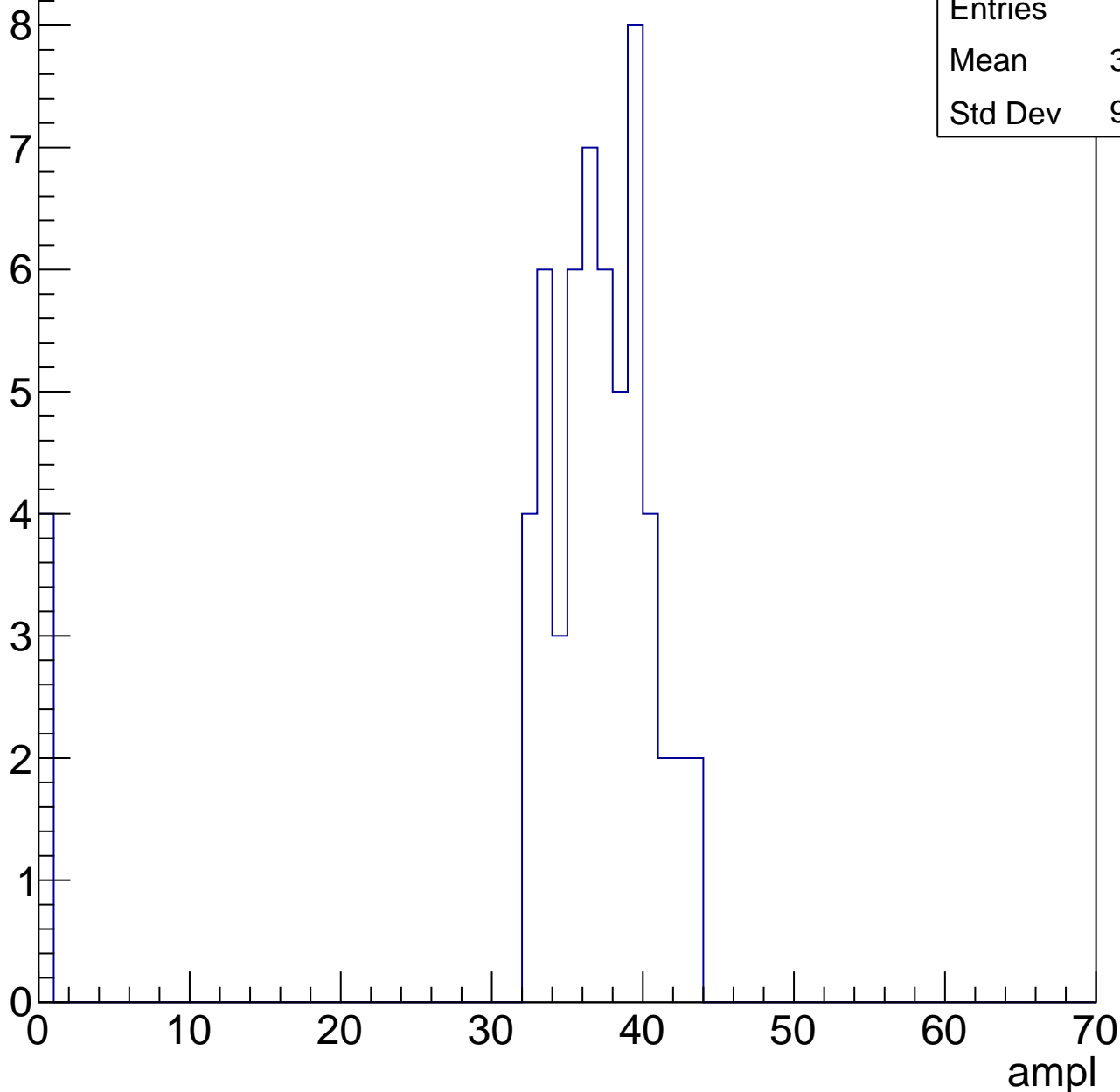


B1L103S, U23-ch37, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	34.34
Std Dev	9.689

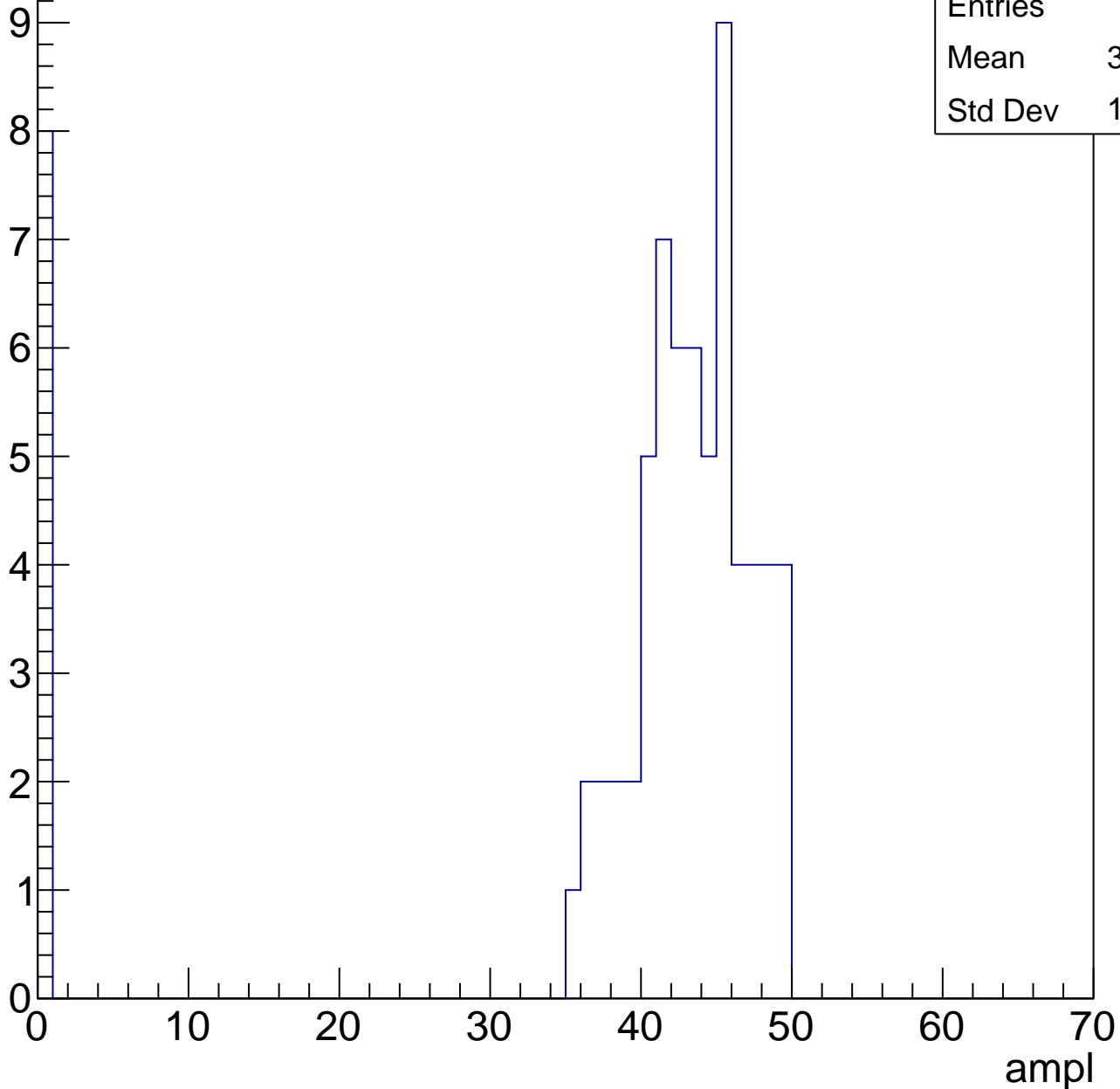


B1L103S, U23-ch37, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

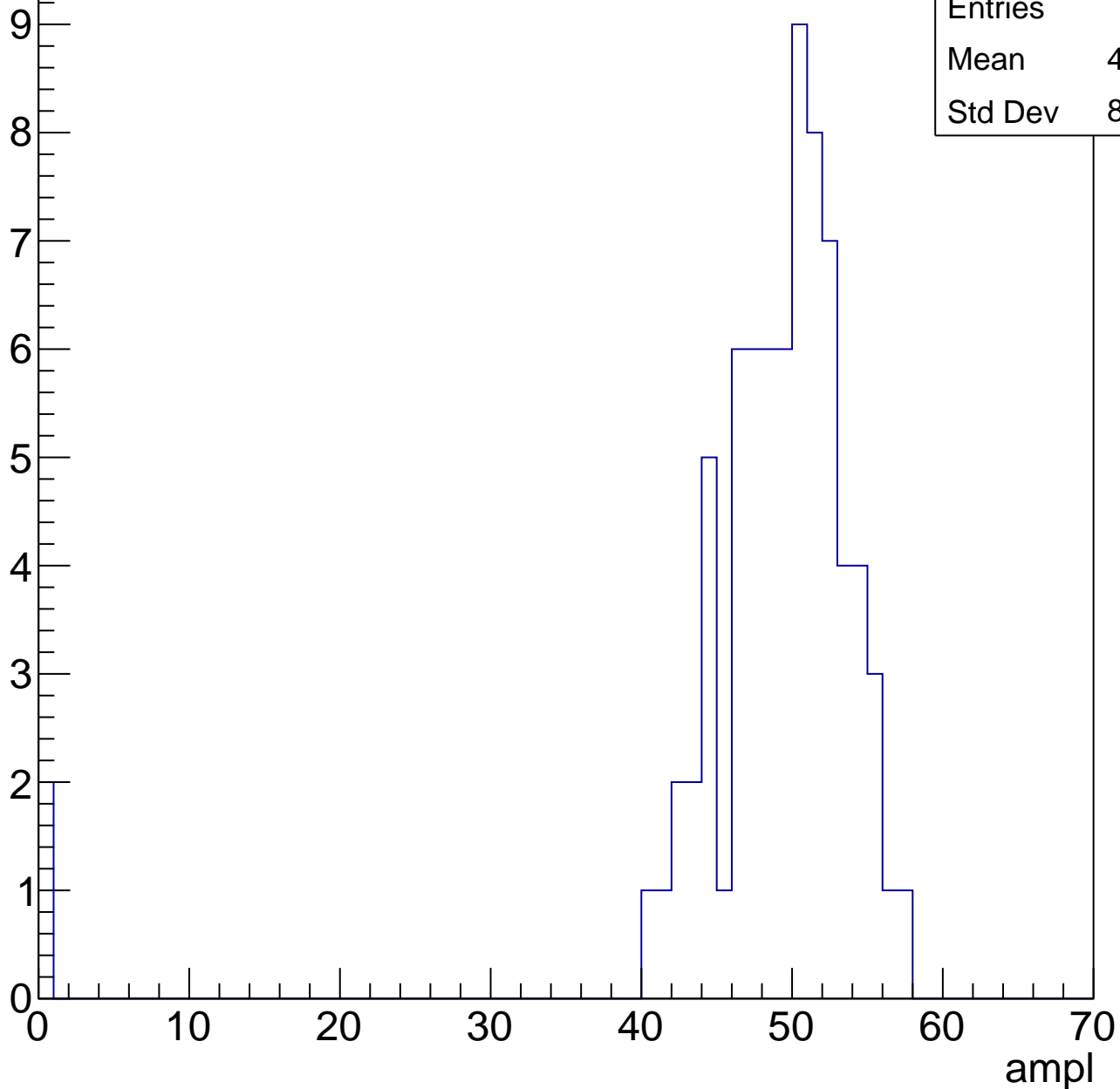
Entries	71
Mean	38.27
Std Dev	14.03



B1L103S, U23-ch37, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

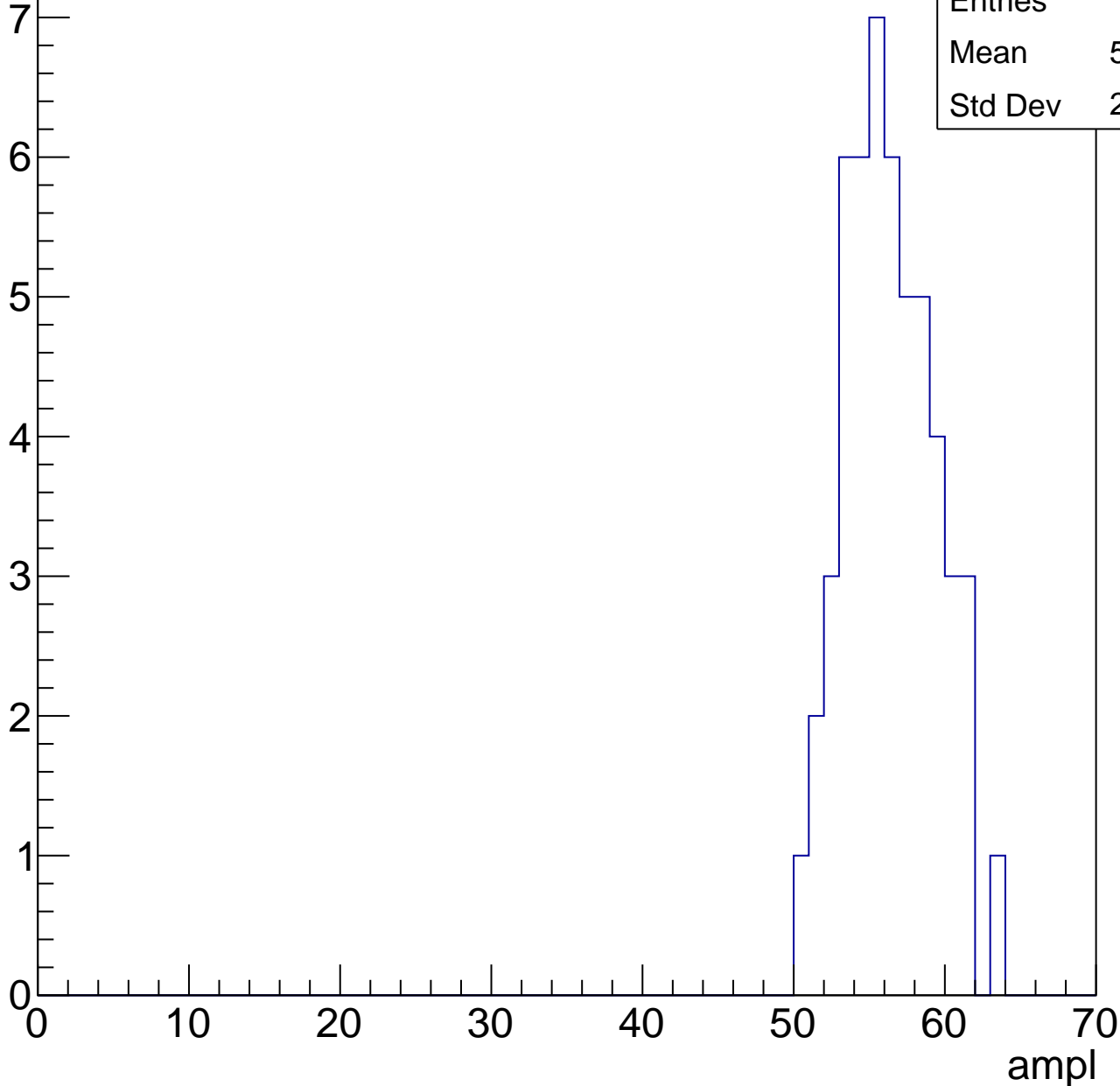


B1L103S, U23-ch37, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	52
Mean	55.92
Std Dev	2.947

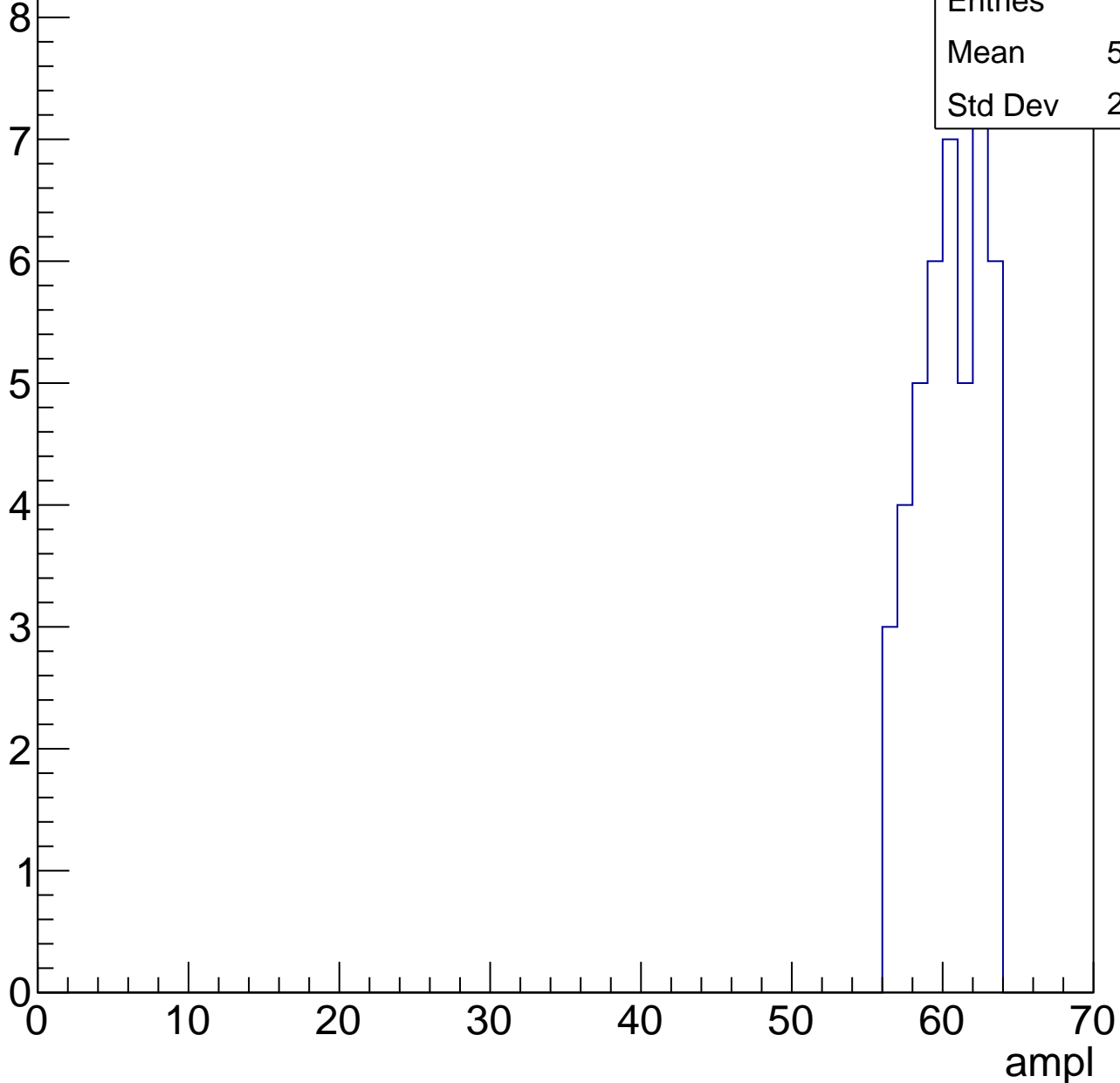


B1L103S, U23-ch37, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

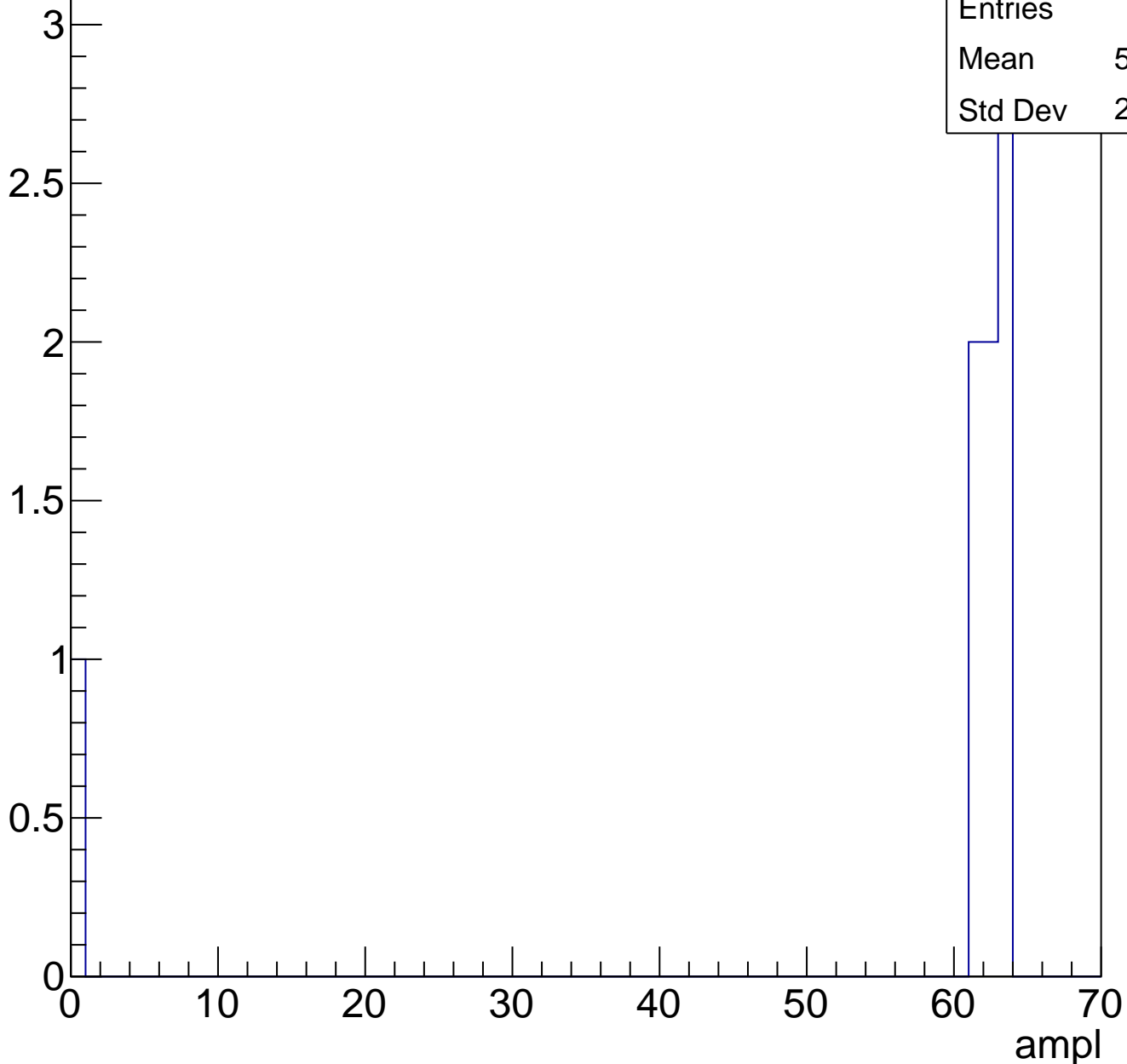
Entries	44
Mean	59.98
Std Dev	2.137



B1L103S, U23-ch37, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch37, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch38, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	72
Mean	25.79
Std Dev	9.011

Entry

10
8
6
4
2
0

ampl

0

10

20

30

40

50

60

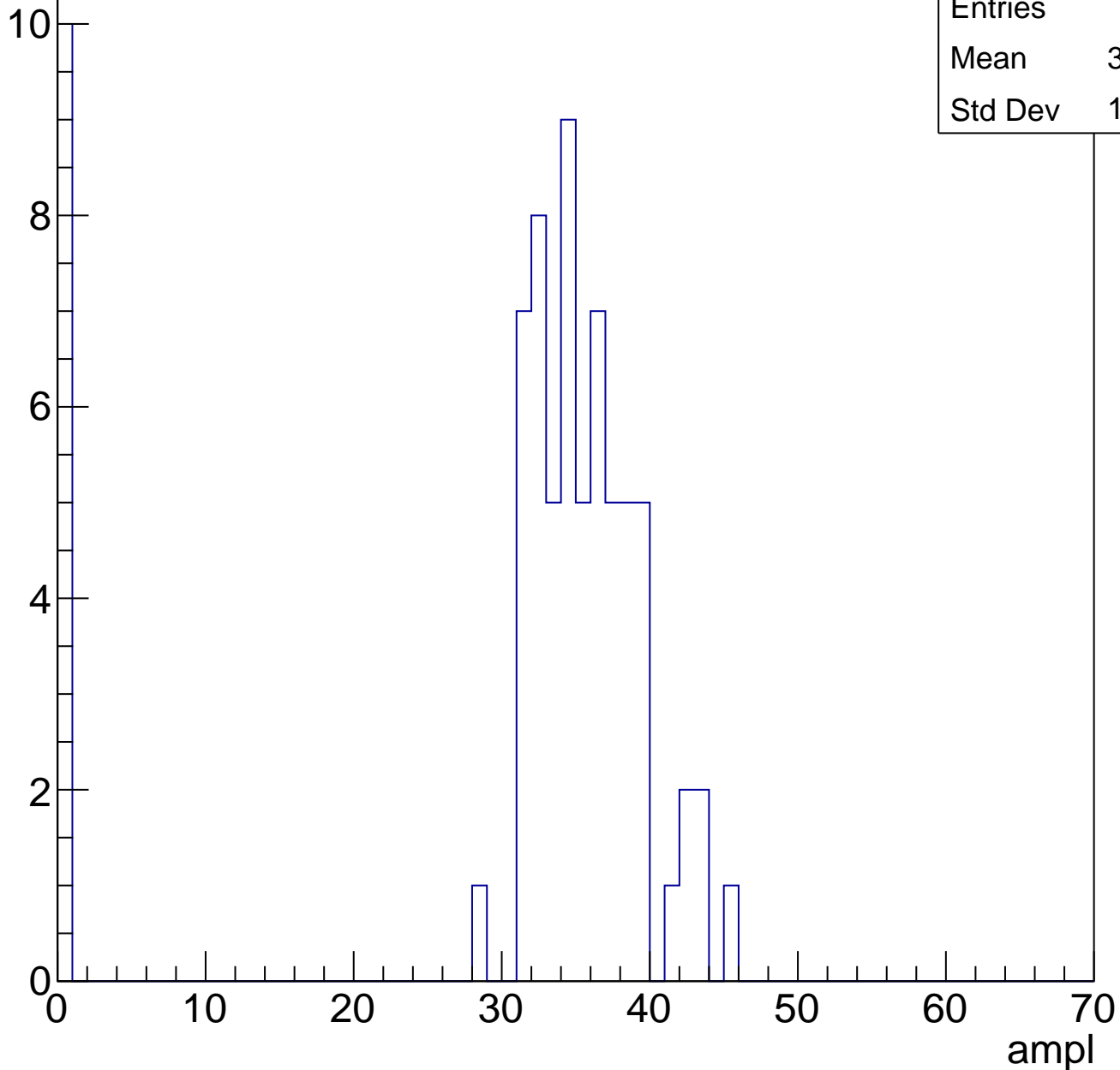
70

B1L103S, U23-ch38, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	73
Mean	30.48
Std Dev	12.57

Entry

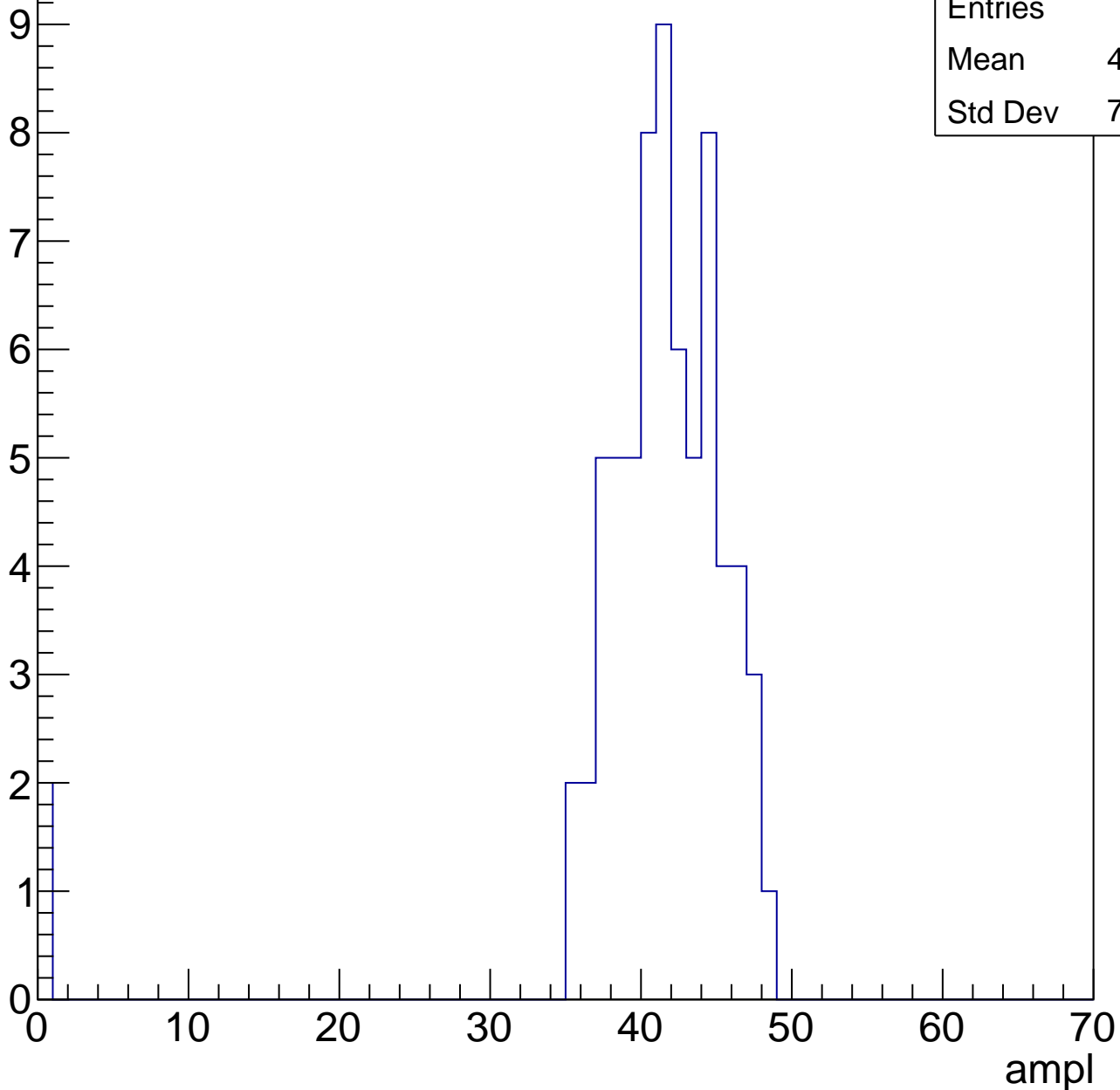


B1L103S, U23-ch38, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	40.19
Std Dev	7.624

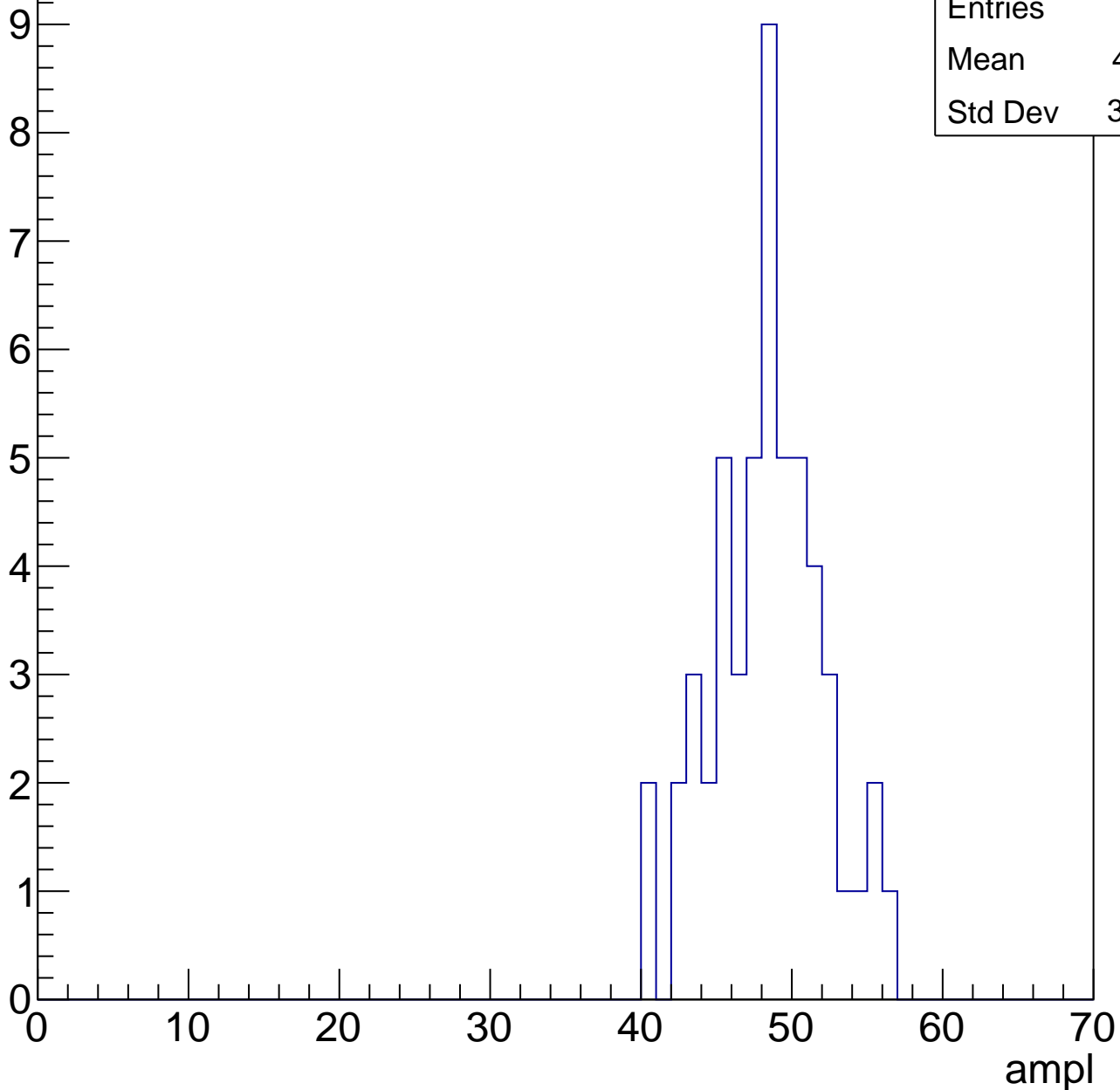


B1L103S, U23-ch38, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	53
Mean	47.91
Std Dev	3.636

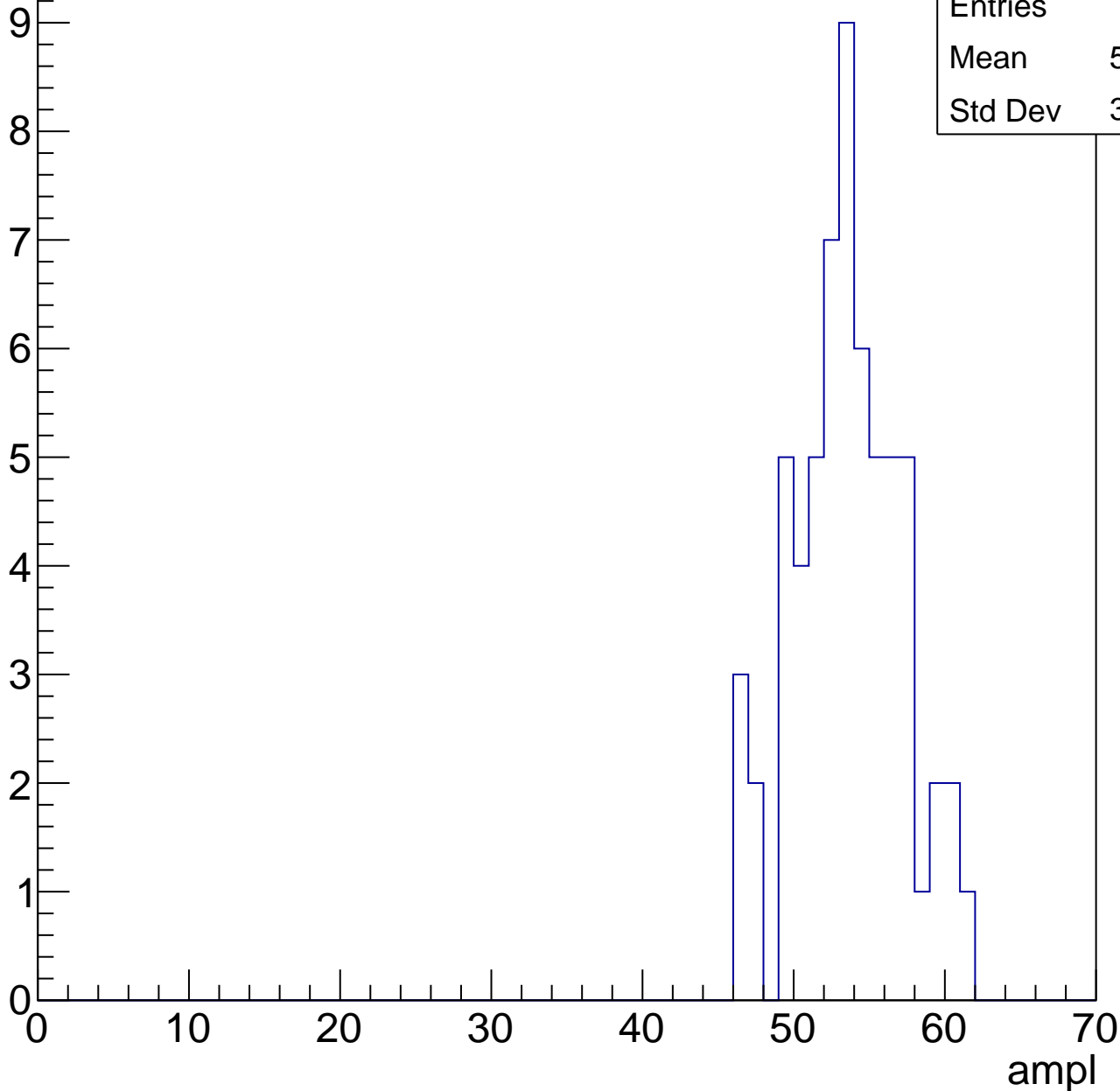


B1L103S, U23-ch38, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

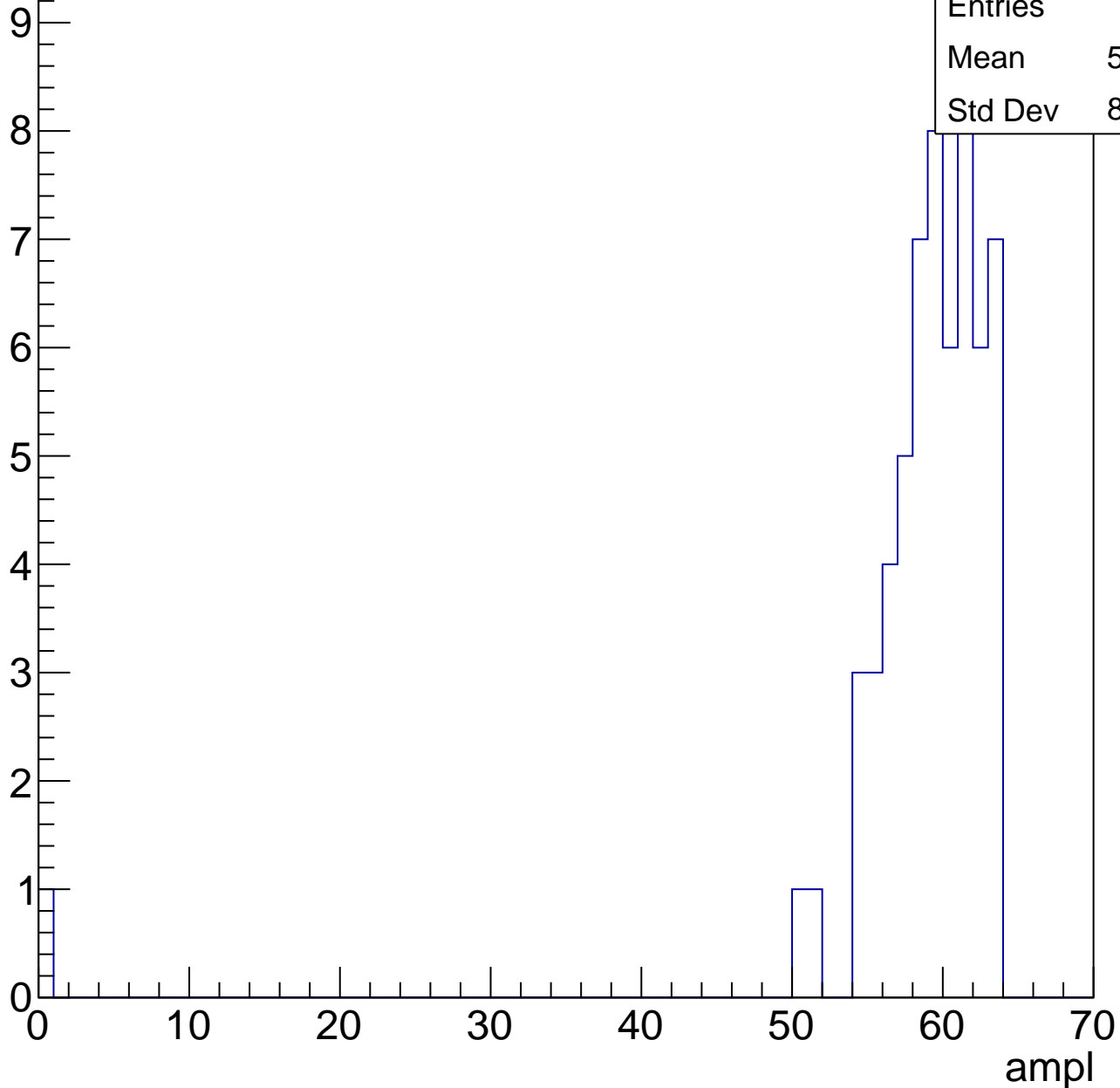
Entries	62
Mean	53.13
Std Dev	3.526



B1L103S, U23-ch38, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

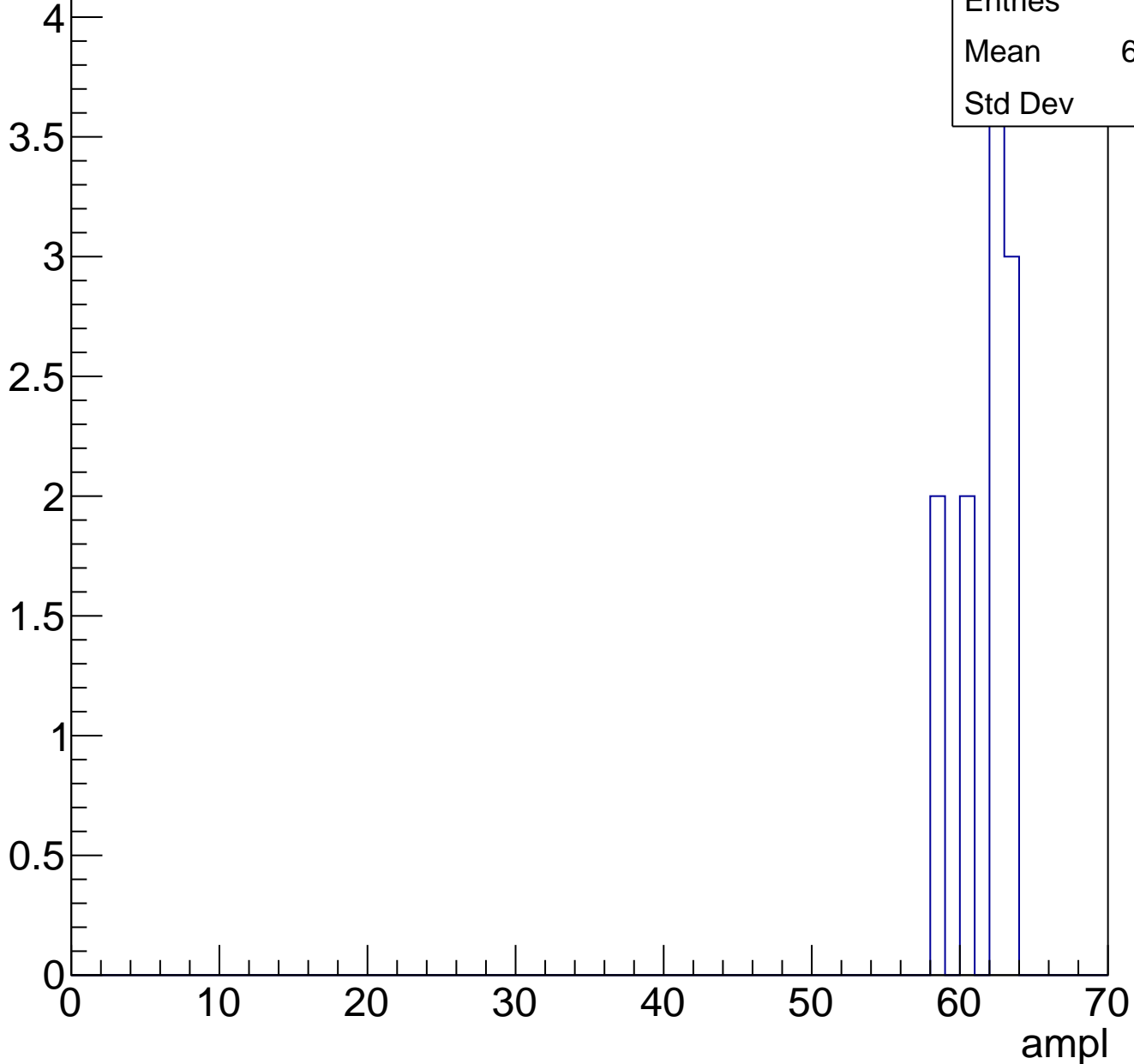


Entries	61
Mean	57.98
Std Dev	8.054

B1L103S, U23-ch38, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch38, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

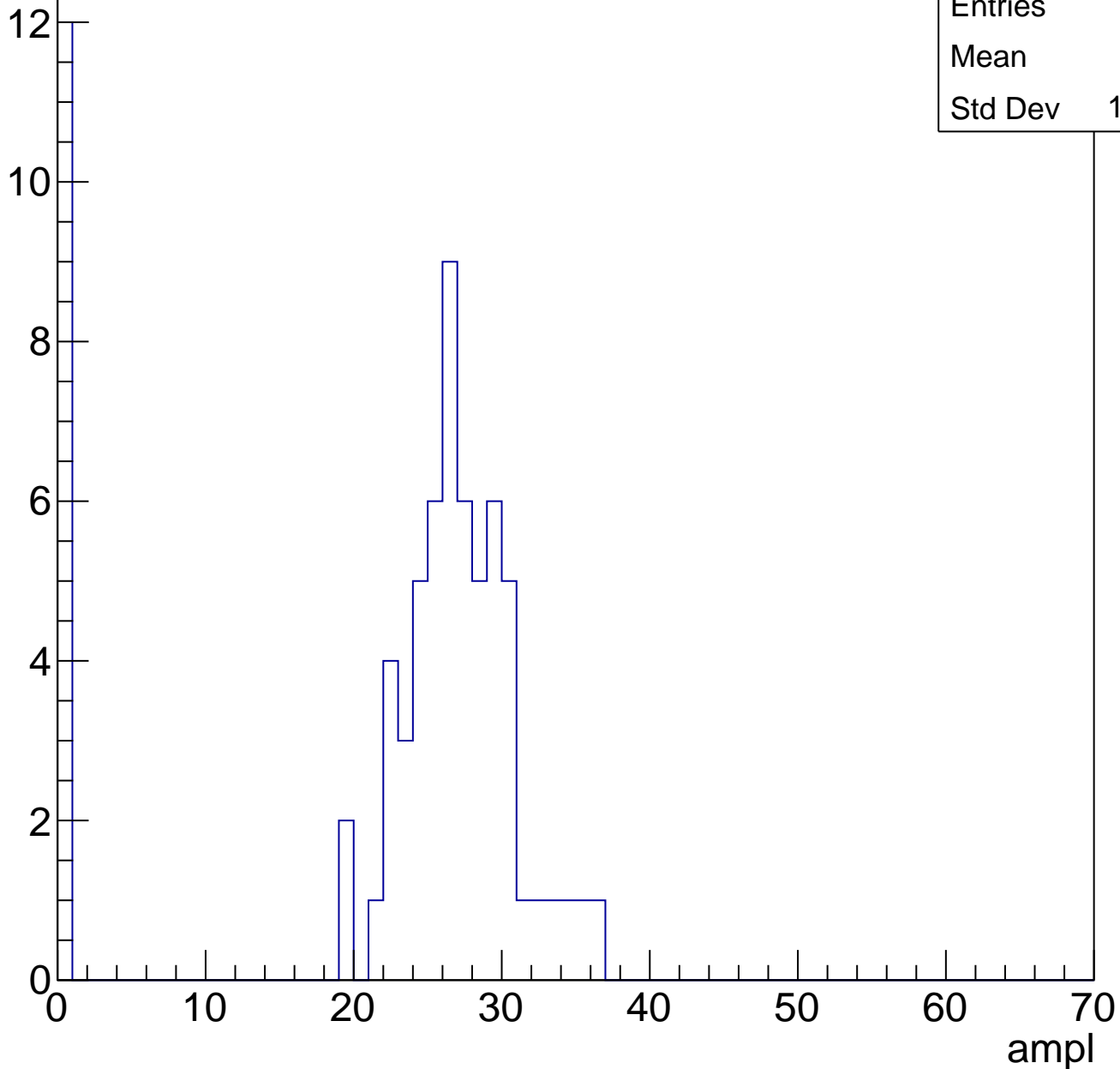
ampl

B1L103S, U23-ch39, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	70
Mean	22.1
Std Dev	10.56

Entry

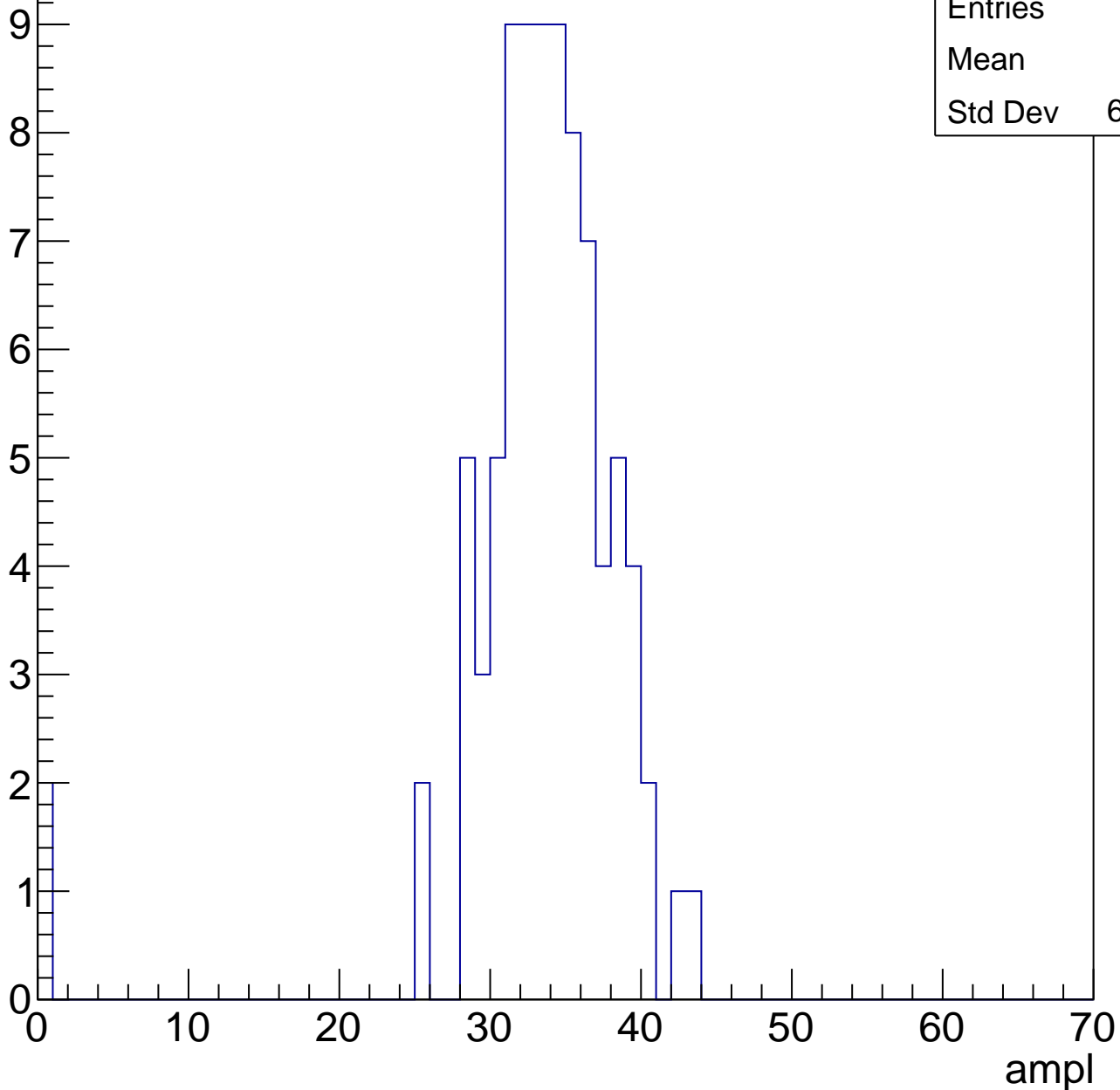


B1L103S, U23-ch39, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	85
Mean	32.8
Std Dev	6.213

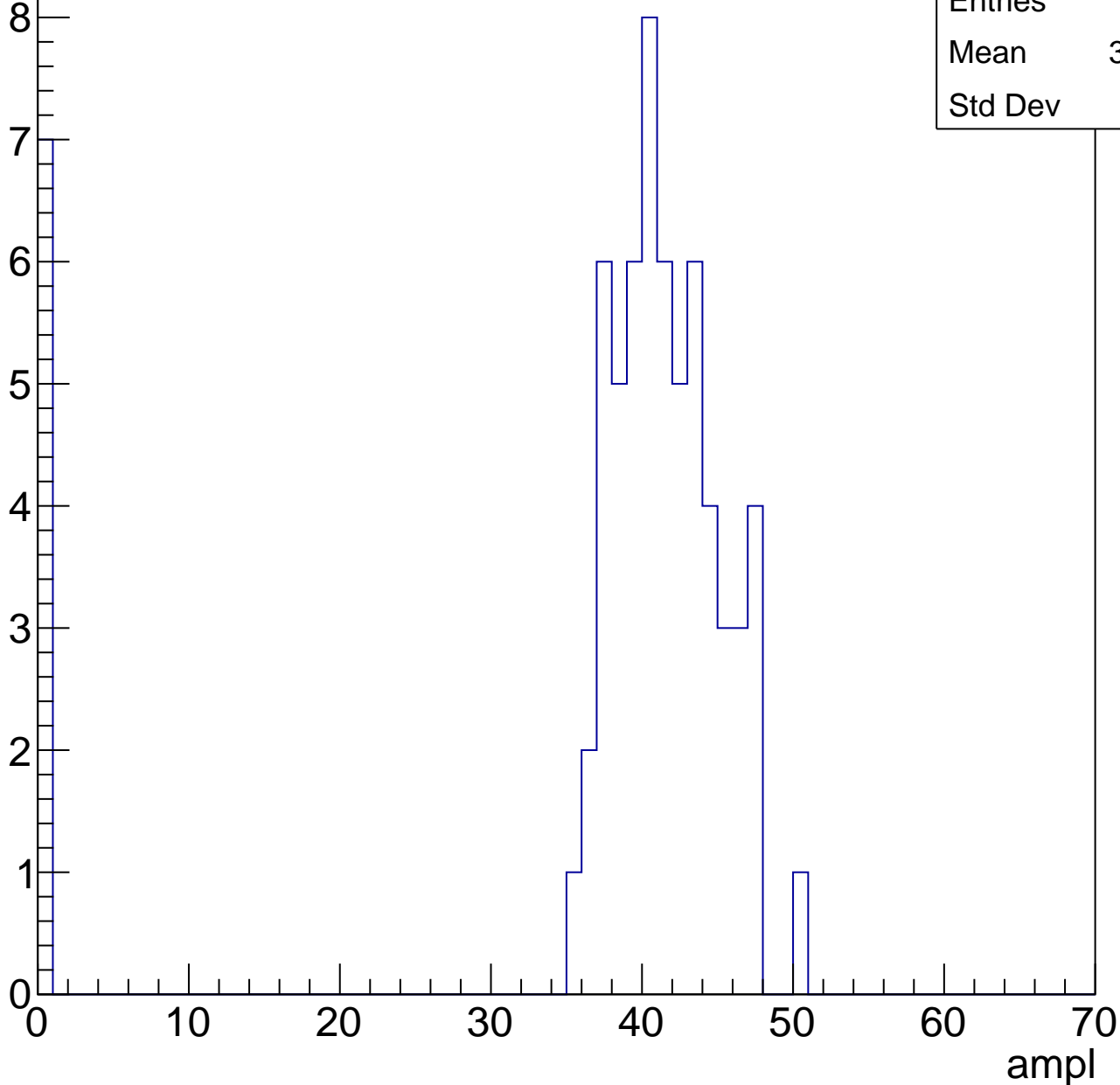


B1L103S, U23-ch39, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	36.93
Std Dev	13

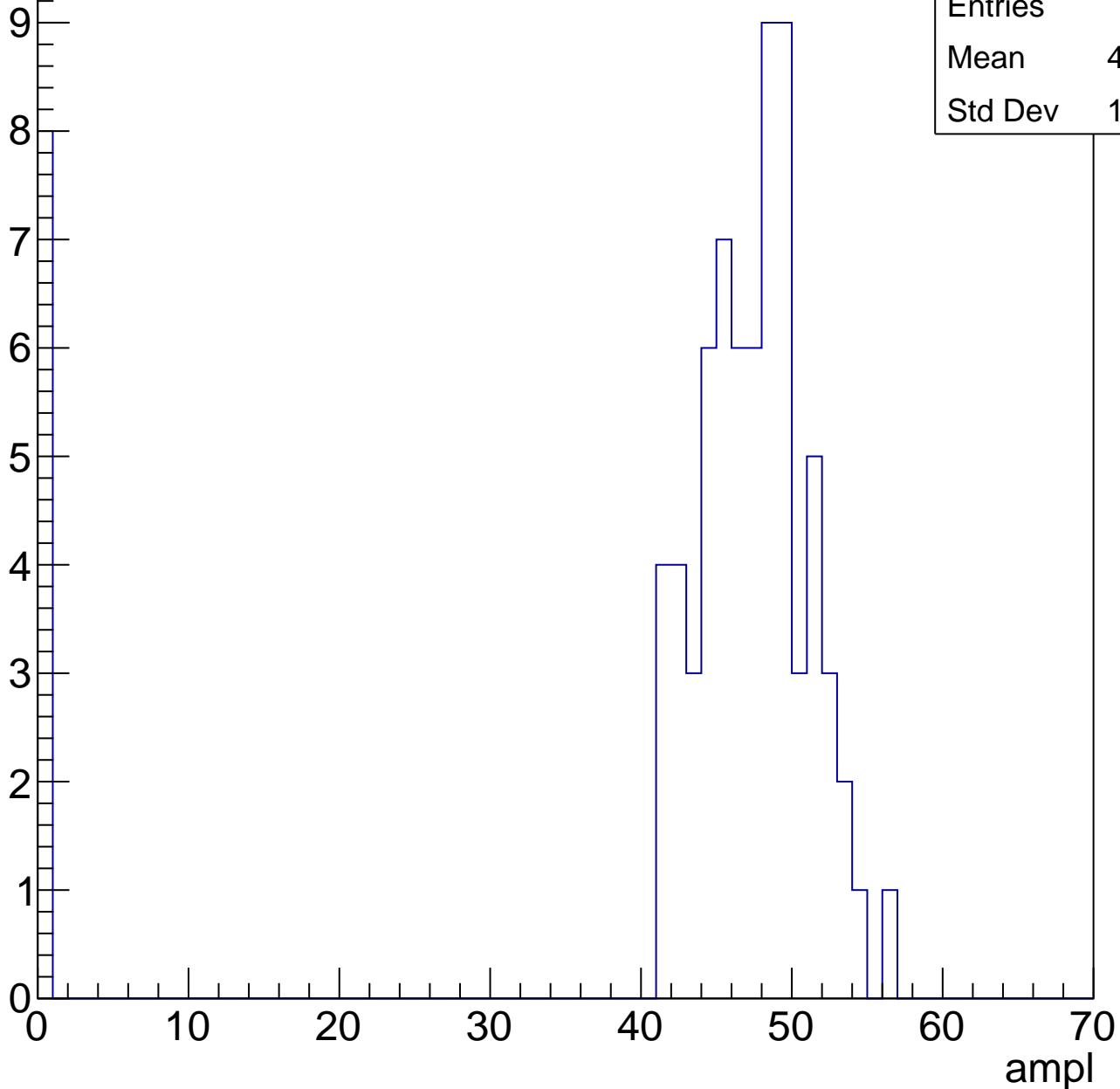


B1L103S, U23-ch39, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	77
Mean	42.18
Std Dev	14.72

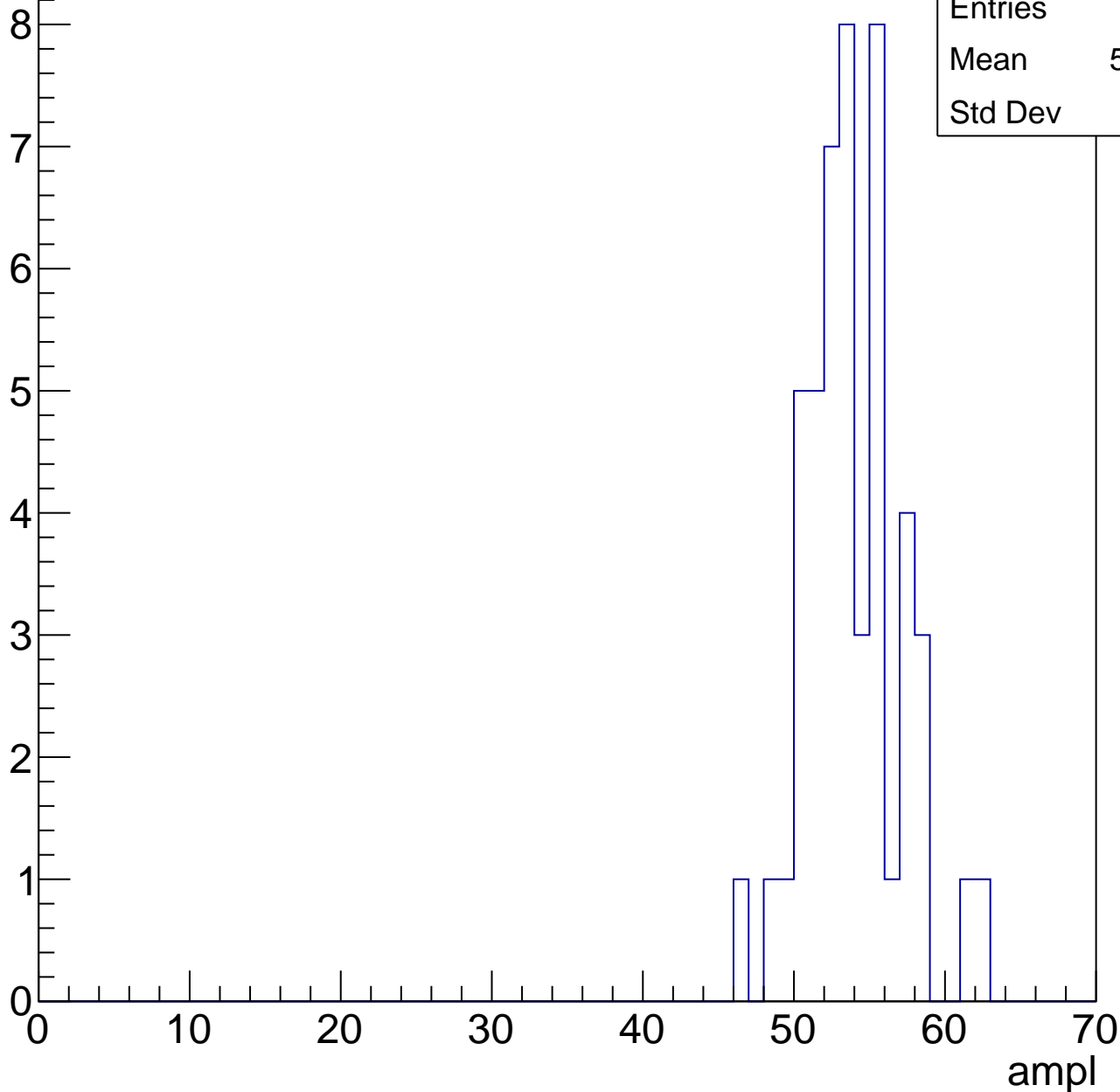


B1L103S, U23-ch39, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	49
Mean	53.45
Std Dev	3.13

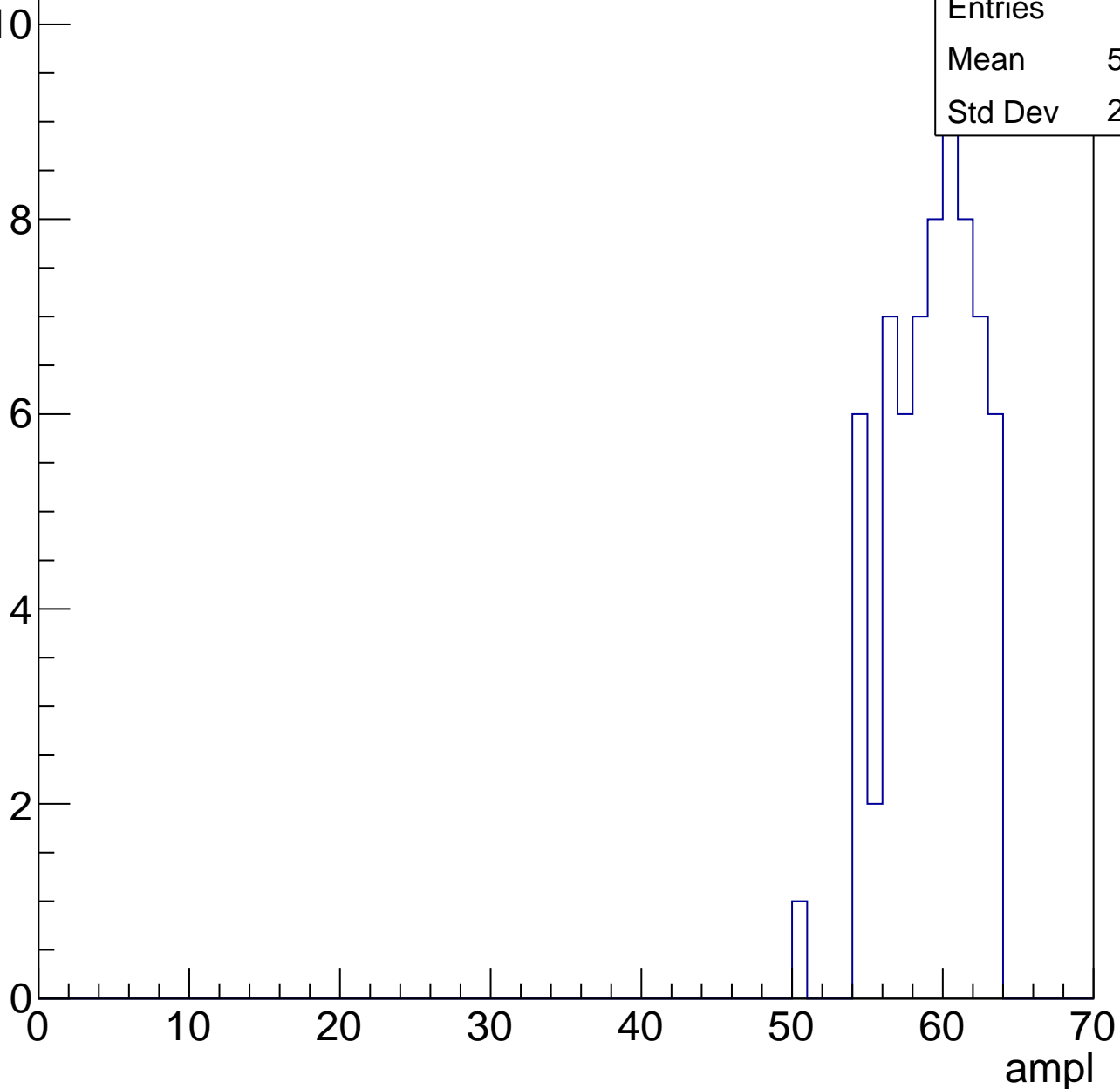


B1L103S, U23-ch39, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

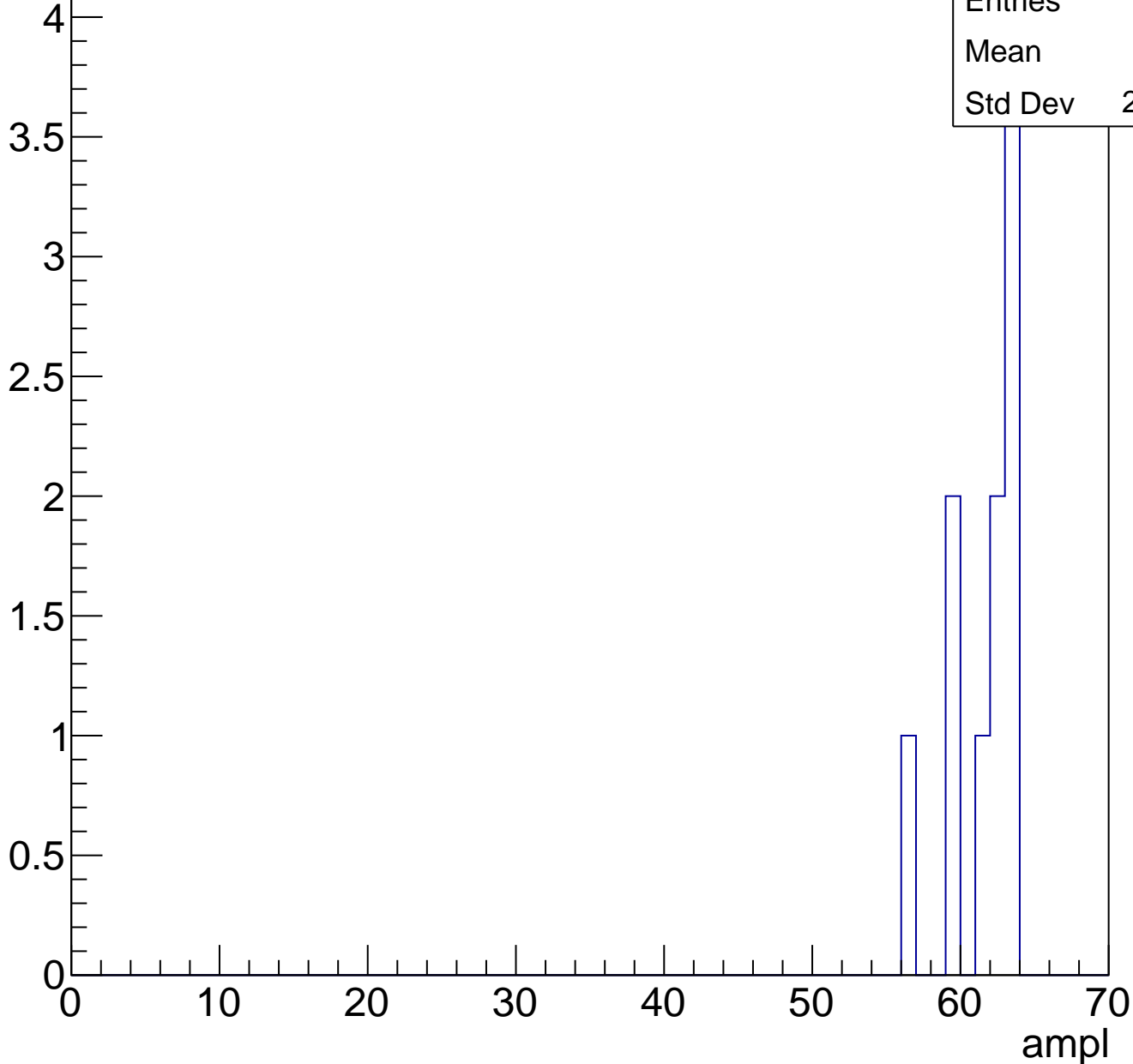
Entries	68
Mean	58.76
Std Dev	2.855



B1L103S, U23-ch39, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch39, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

20
18
16
14
12
10
8
6
4
2
0

Entries	20
Mean	0
Std Dev	0

ampl

B1L103S, U23-ch40, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	85
Mean	24.94
Std Dev	10.46

Entry

10

8

6

4

2

0

0

10

20

30

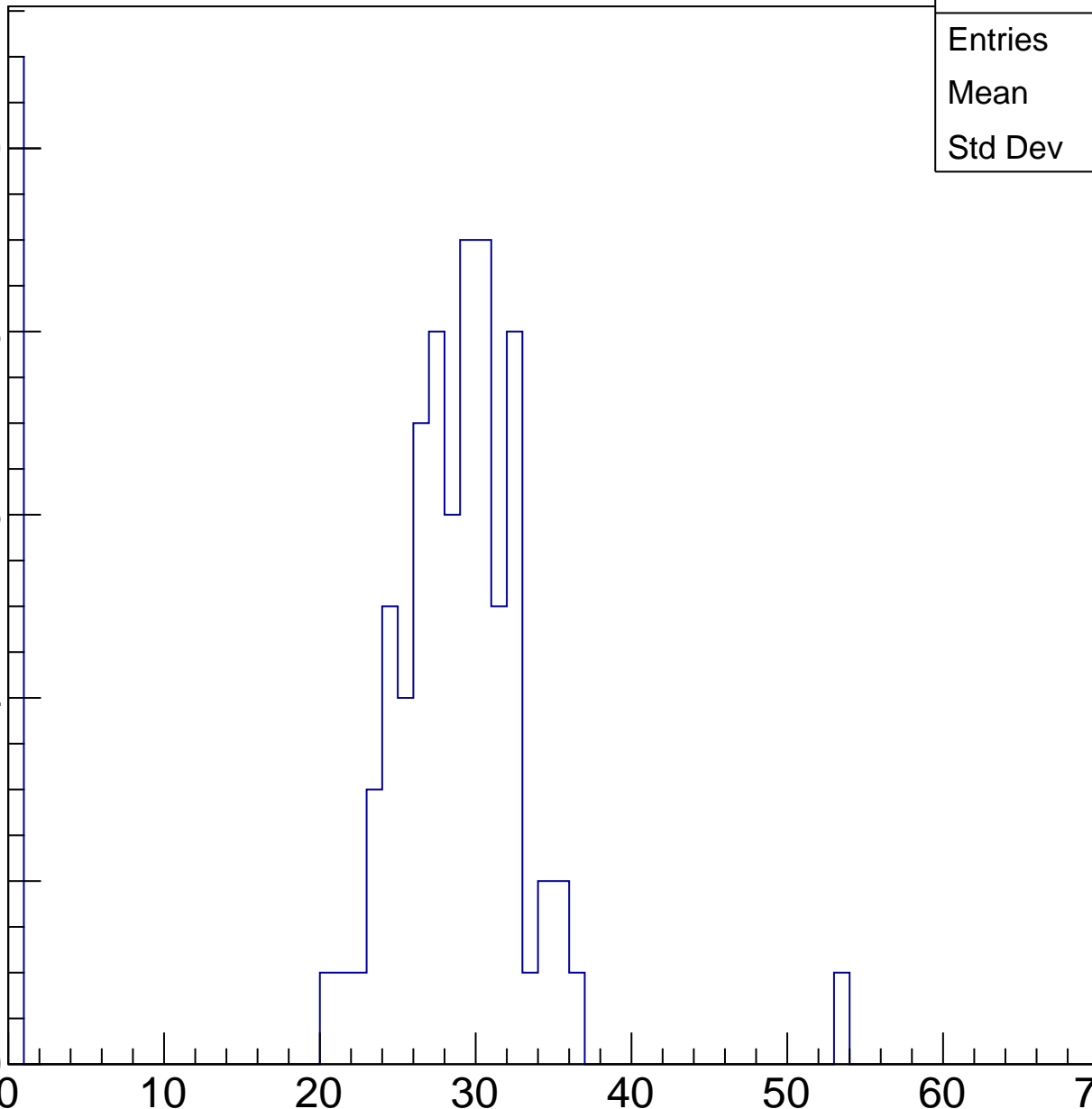
40

50

60

70

ampl

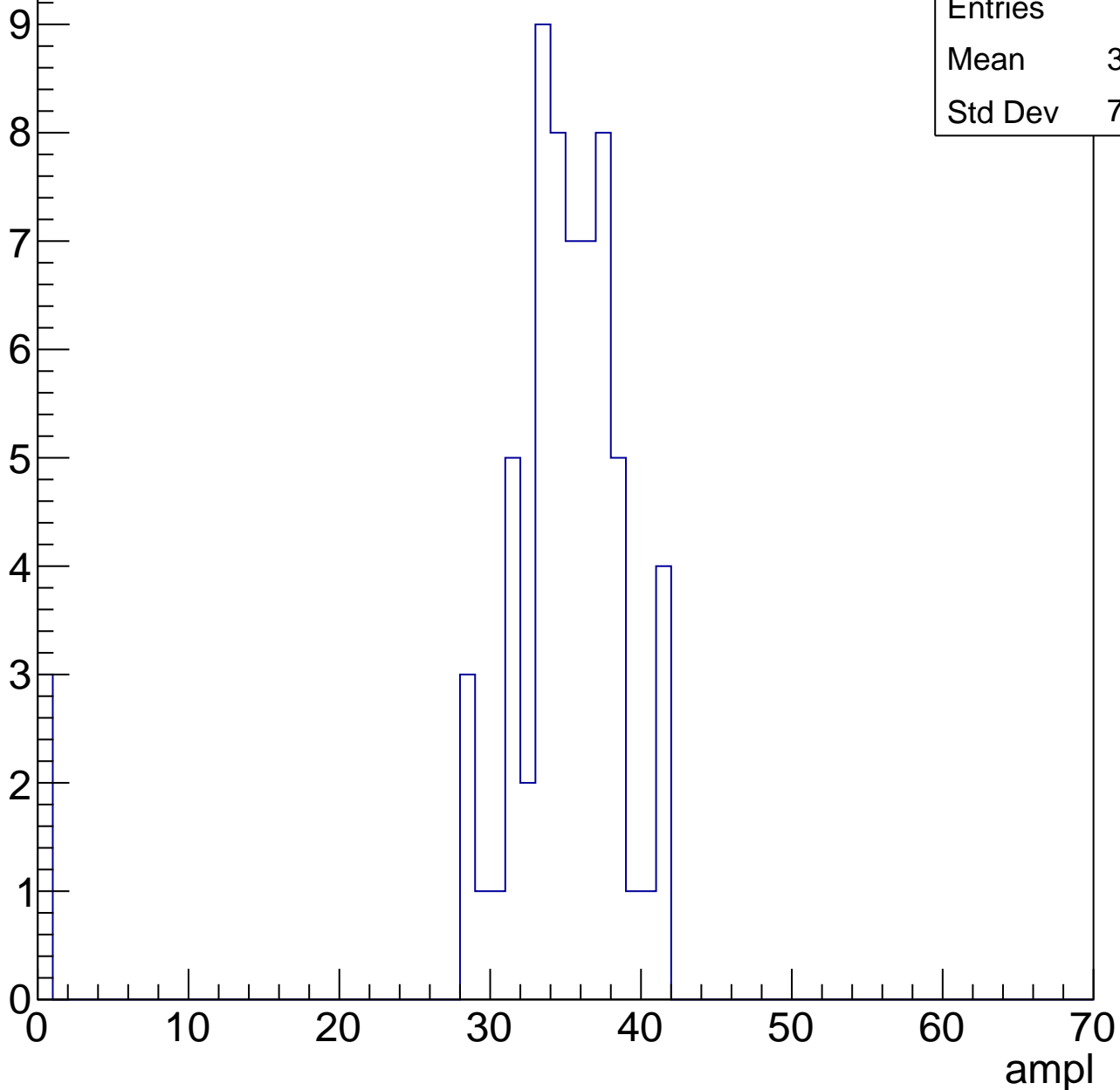


B1L103S, U23-ch40, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

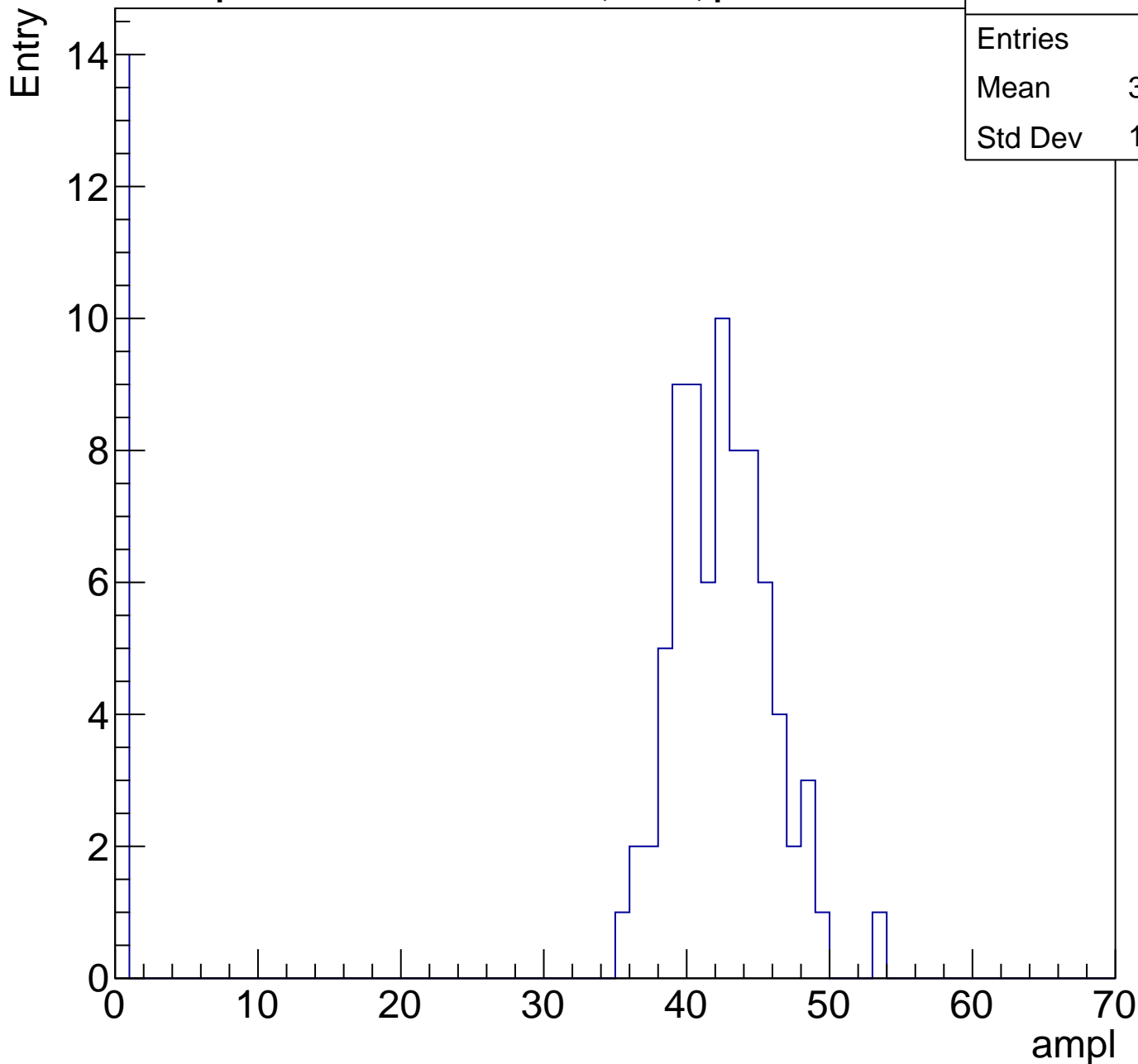
Entries	65
Mean	33.18
Std Dev	7.922



B1L103S, U23-ch40, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	91
Mean	35.58
Std Dev	15.48

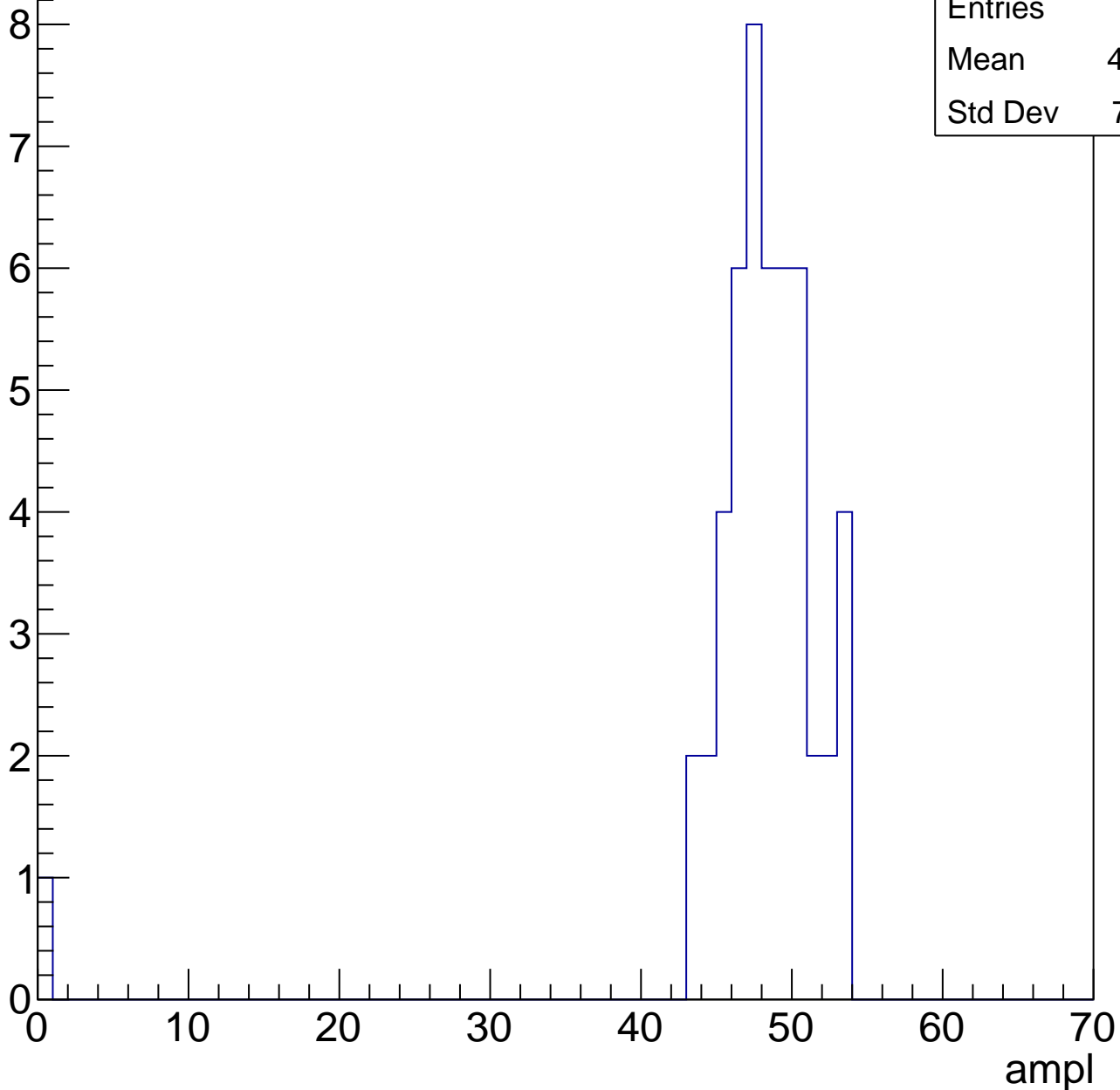


B1L103S, U23-ch40, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	49
Mean	47.06
Std Dev	7.271

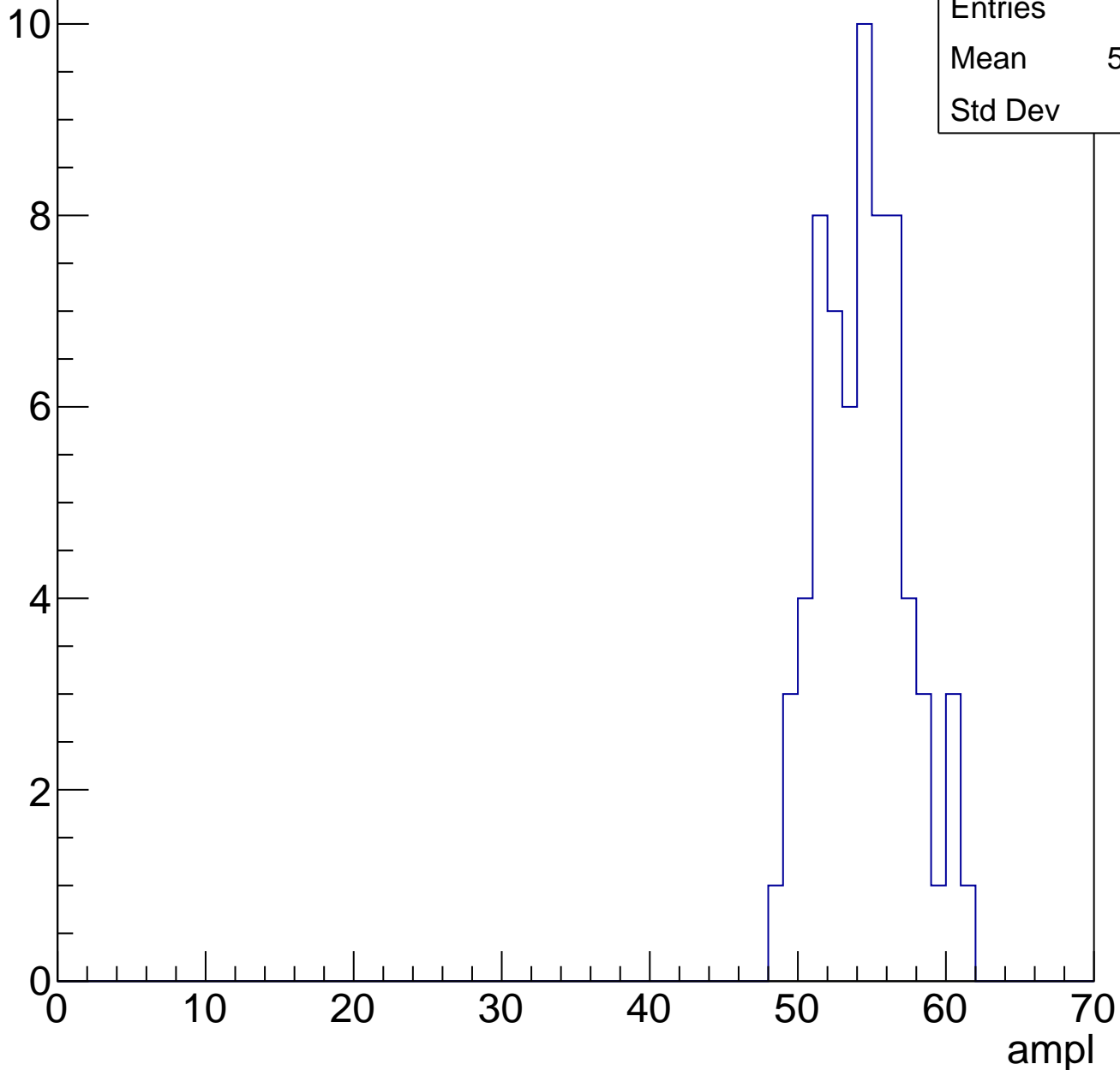


B1L103S, U23-ch40, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entries	67
Mean	53.96
Std Dev	2.96

Entry

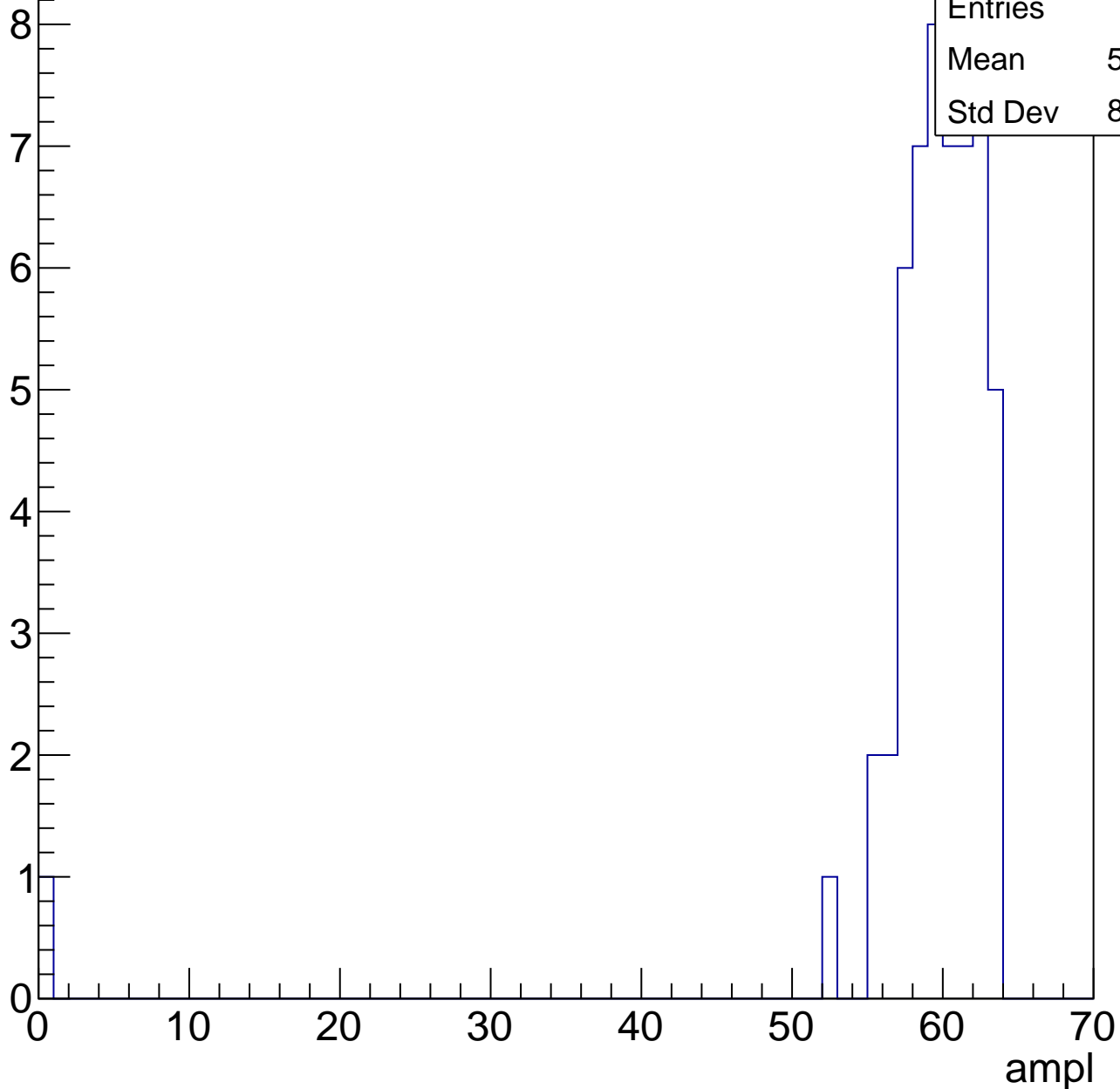


B1L103S, U23-ch40, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

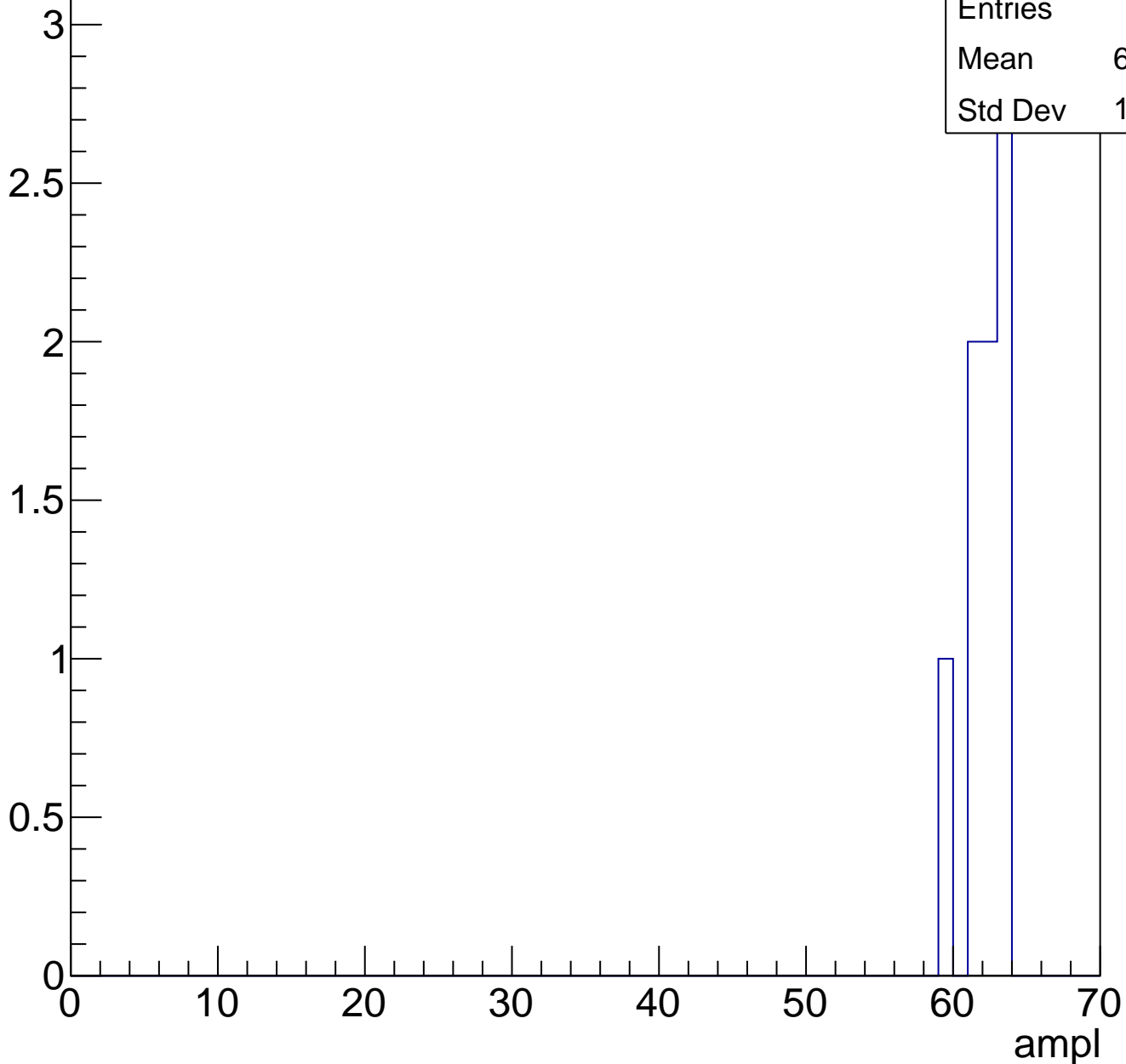
Entries	54
Mean	58.37
Std Dev	8.363



B1L103S, U23-ch40, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

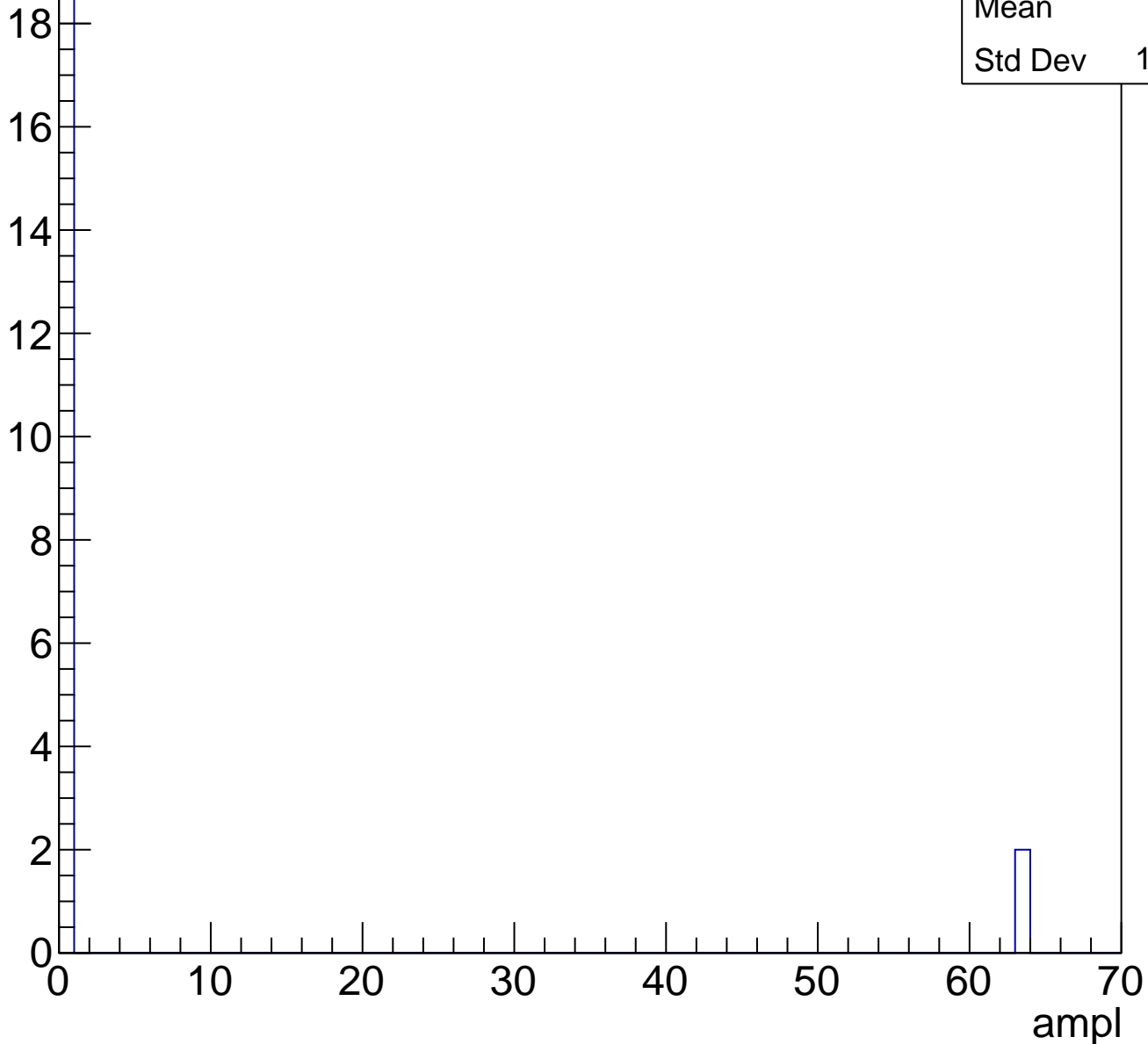


B1L103S, U23-ch40, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	21
Mean	6
Std Dev	18.49

Entry

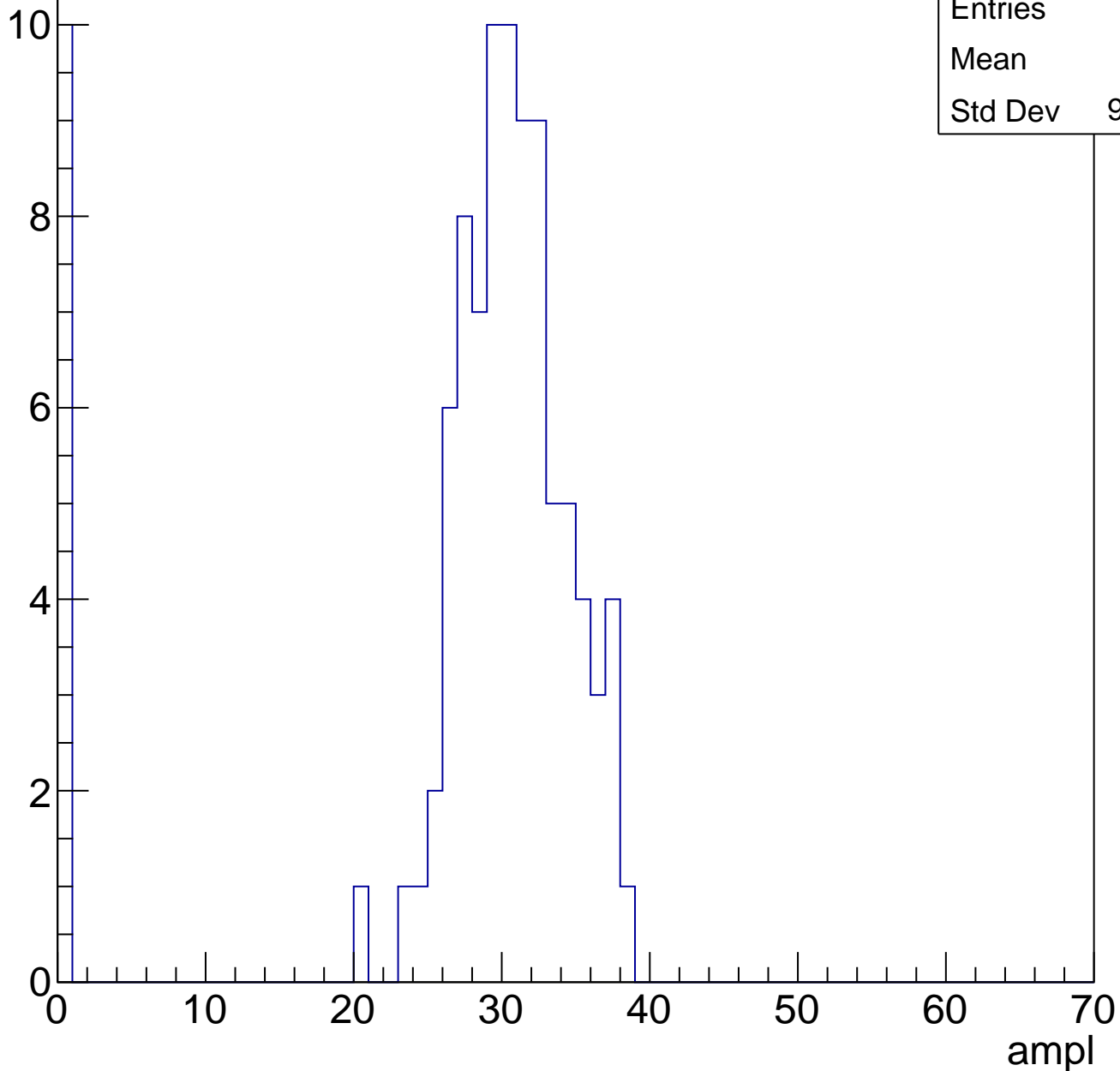


B1L103S, U23-ch41, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	96
Mean	27.2
Std Dev	9.856

Entry

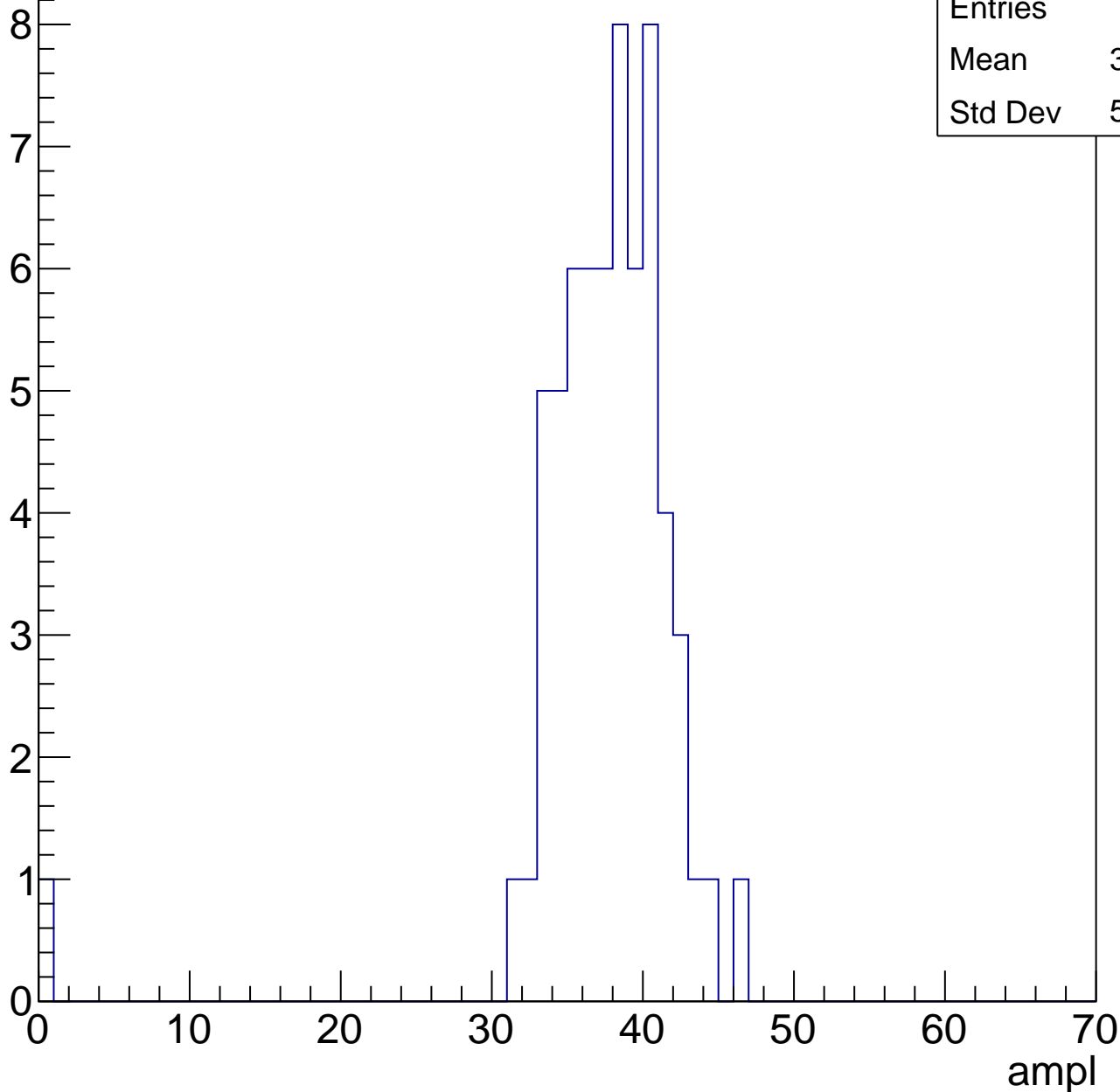


B1L103S, U23-ch41, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	63
Mean	36.94
Std Dev	5.626

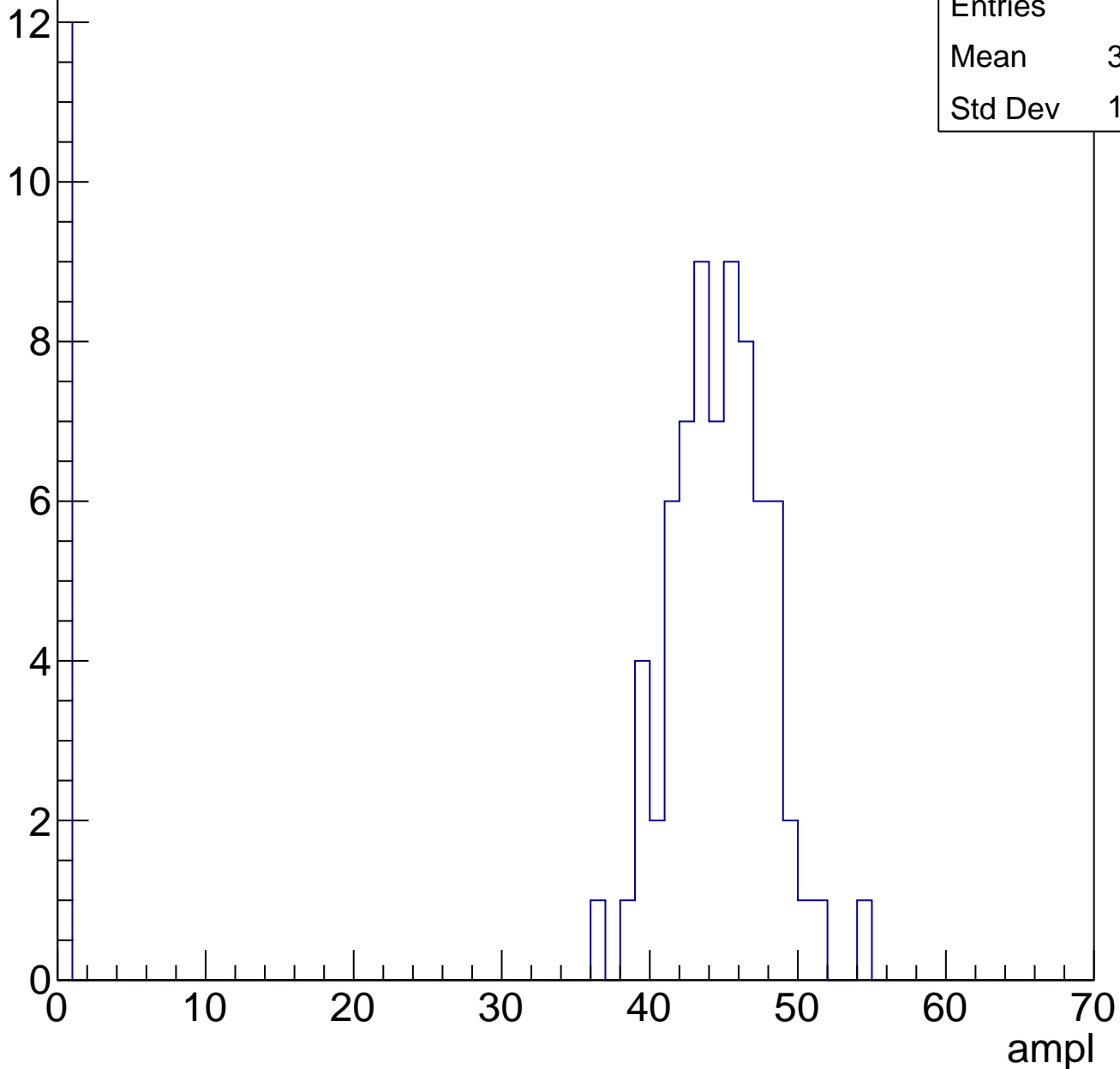


B1L103S, U23-ch41, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	83
Mean	37.84
Std Dev	15.84

Entry

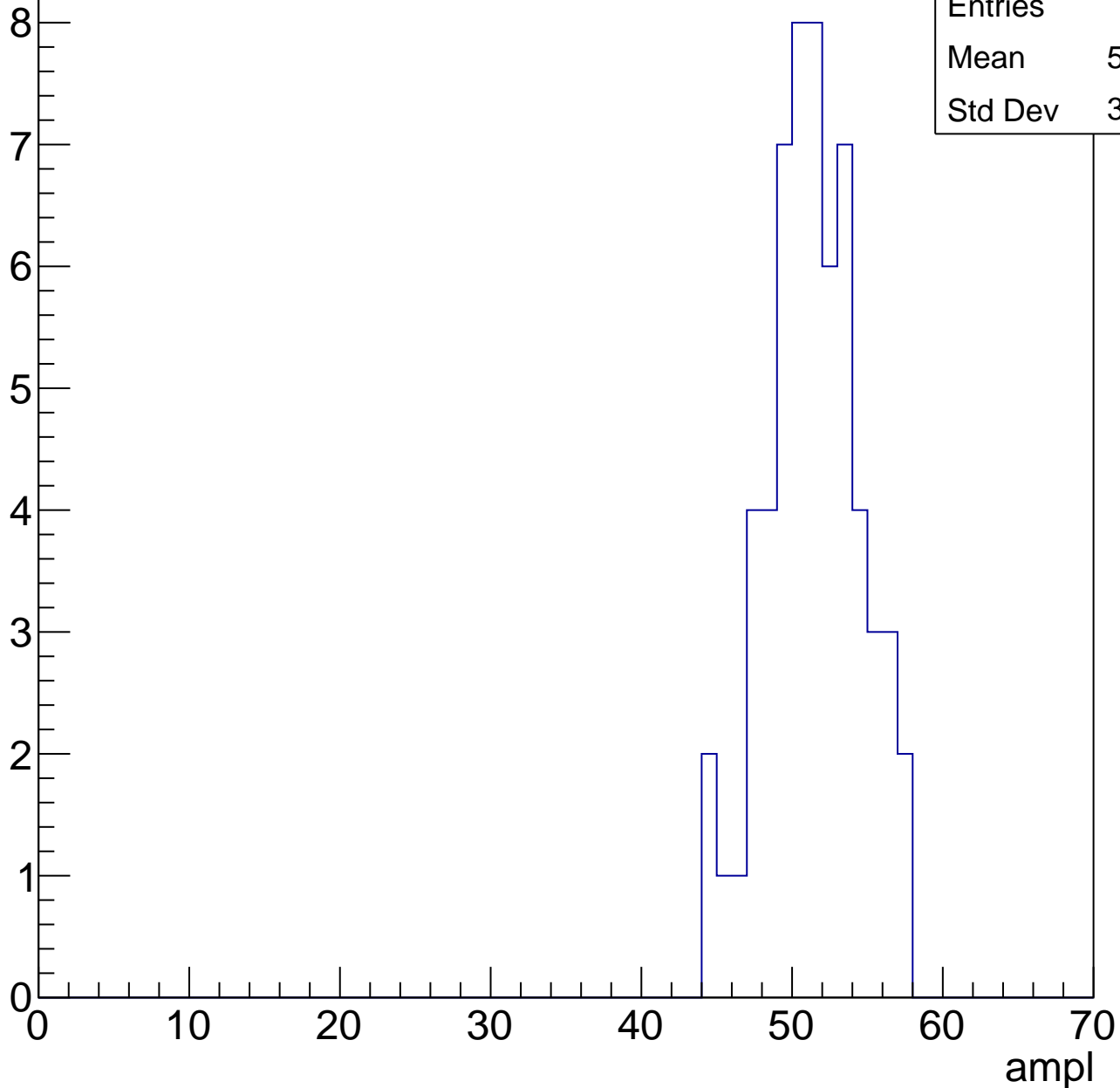


B1L103S, U23-ch41, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

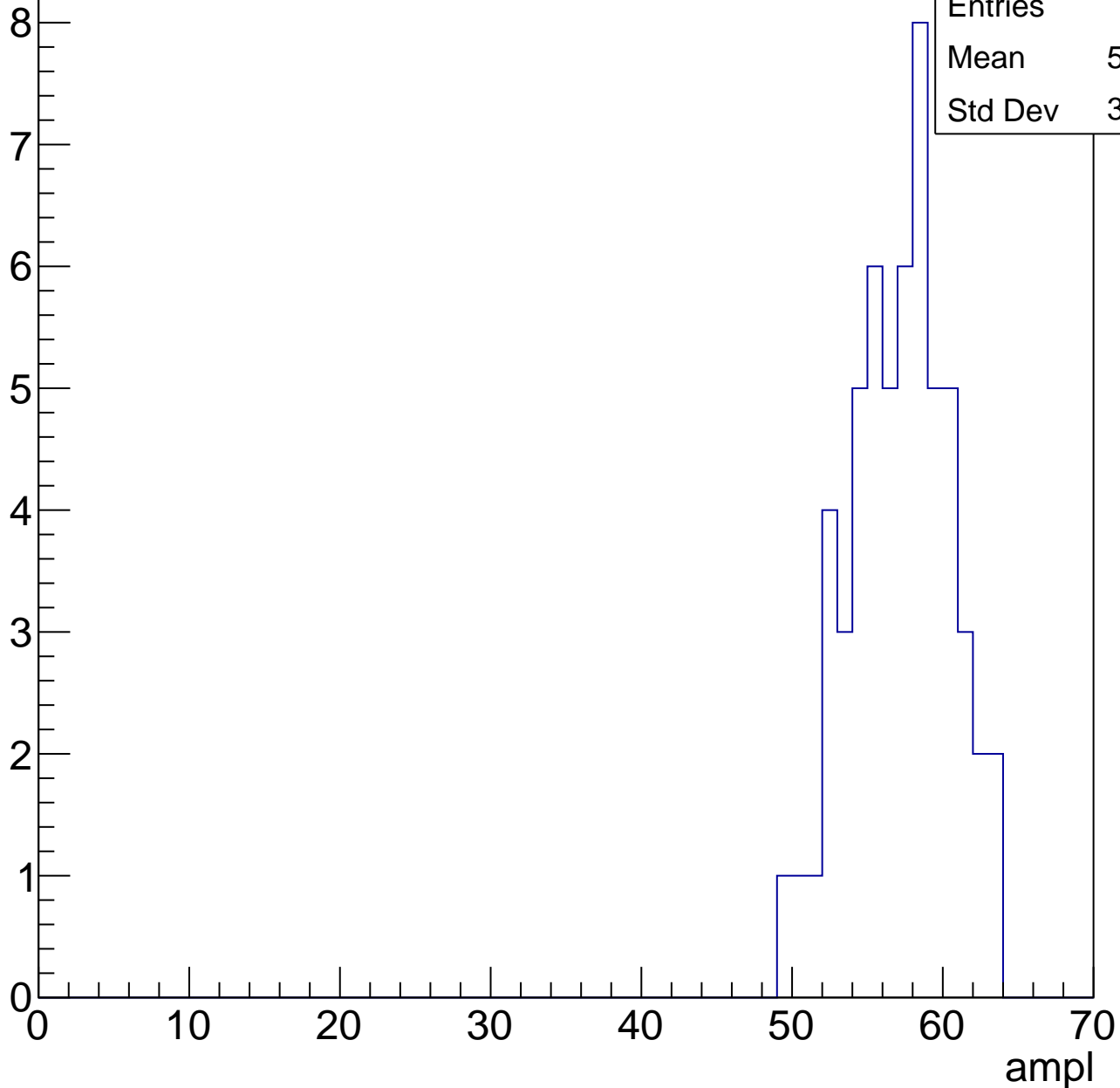
Entries	60
Mean	50.93
Std Dev	3.054



B1L103S, U23-ch41, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

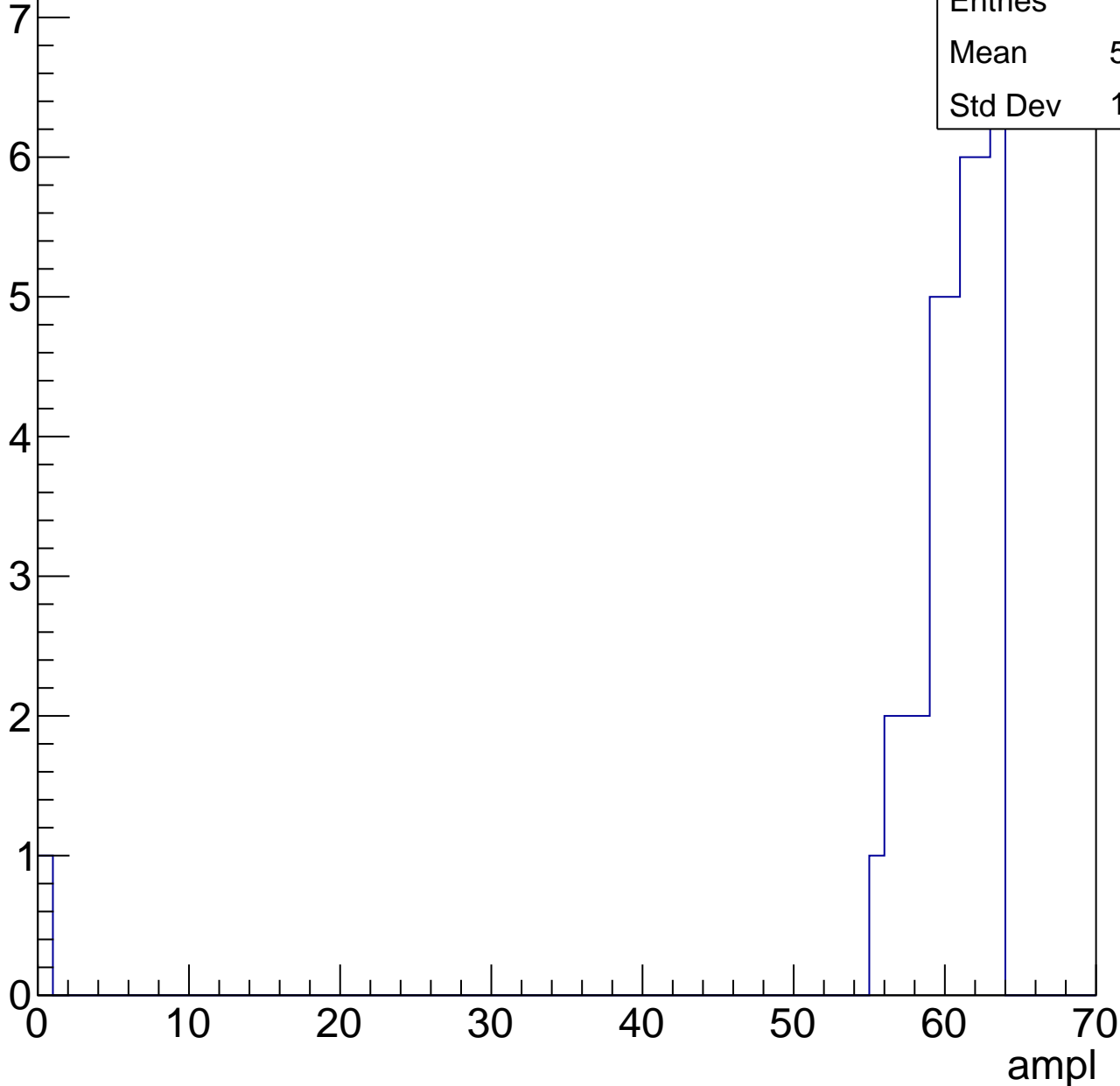


B1L103S, U23-ch41, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	37
Mean	58.68
Std Dev	10.02



B1L103S, U23-ch41, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch41, adc7

calib_packv5_041523_1651.root, FC#0, port C2

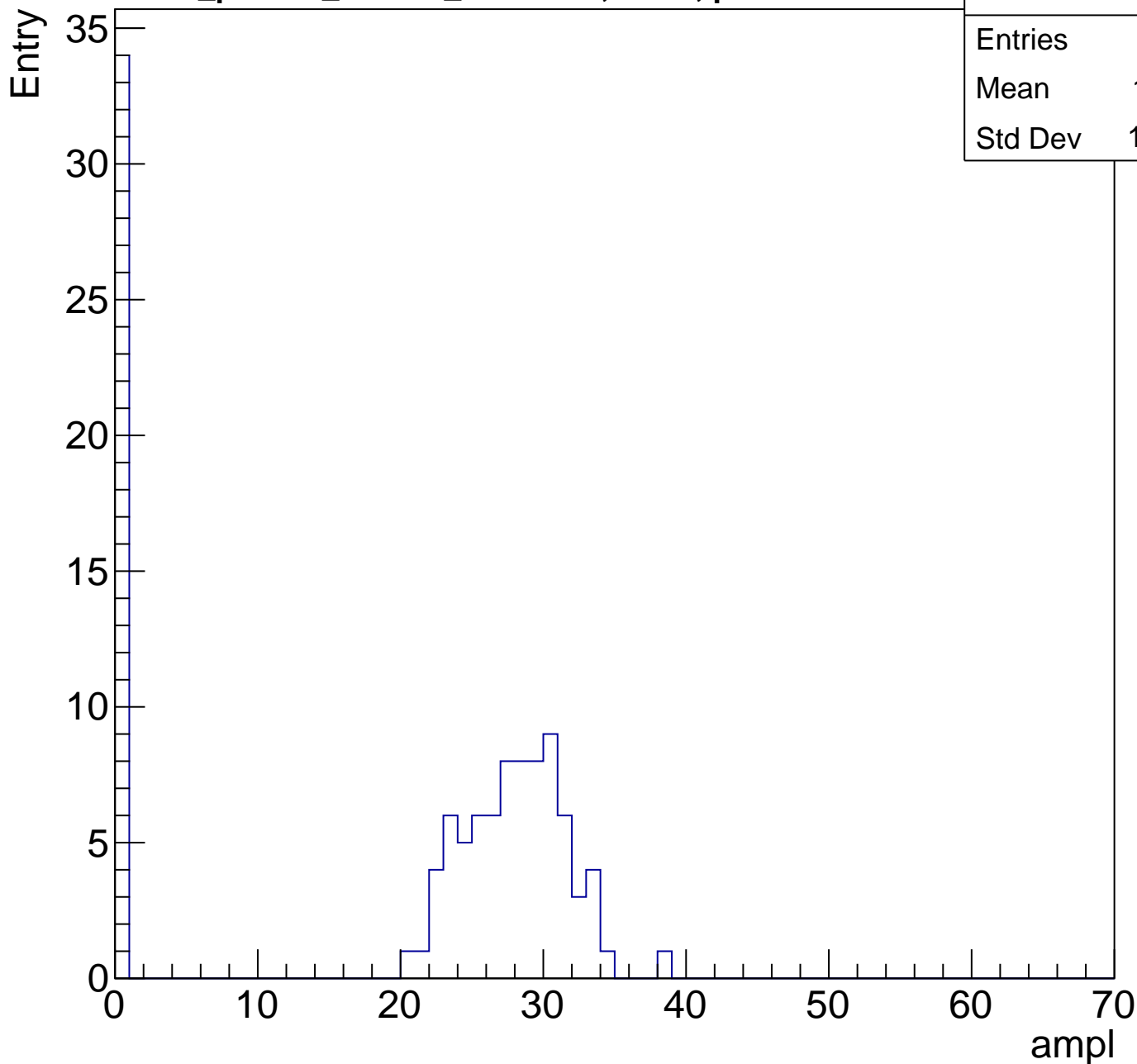
Entry



B1L103S, U23-ch42, adc0

calib_packv5_041523_1651.root, FC#0, port C2

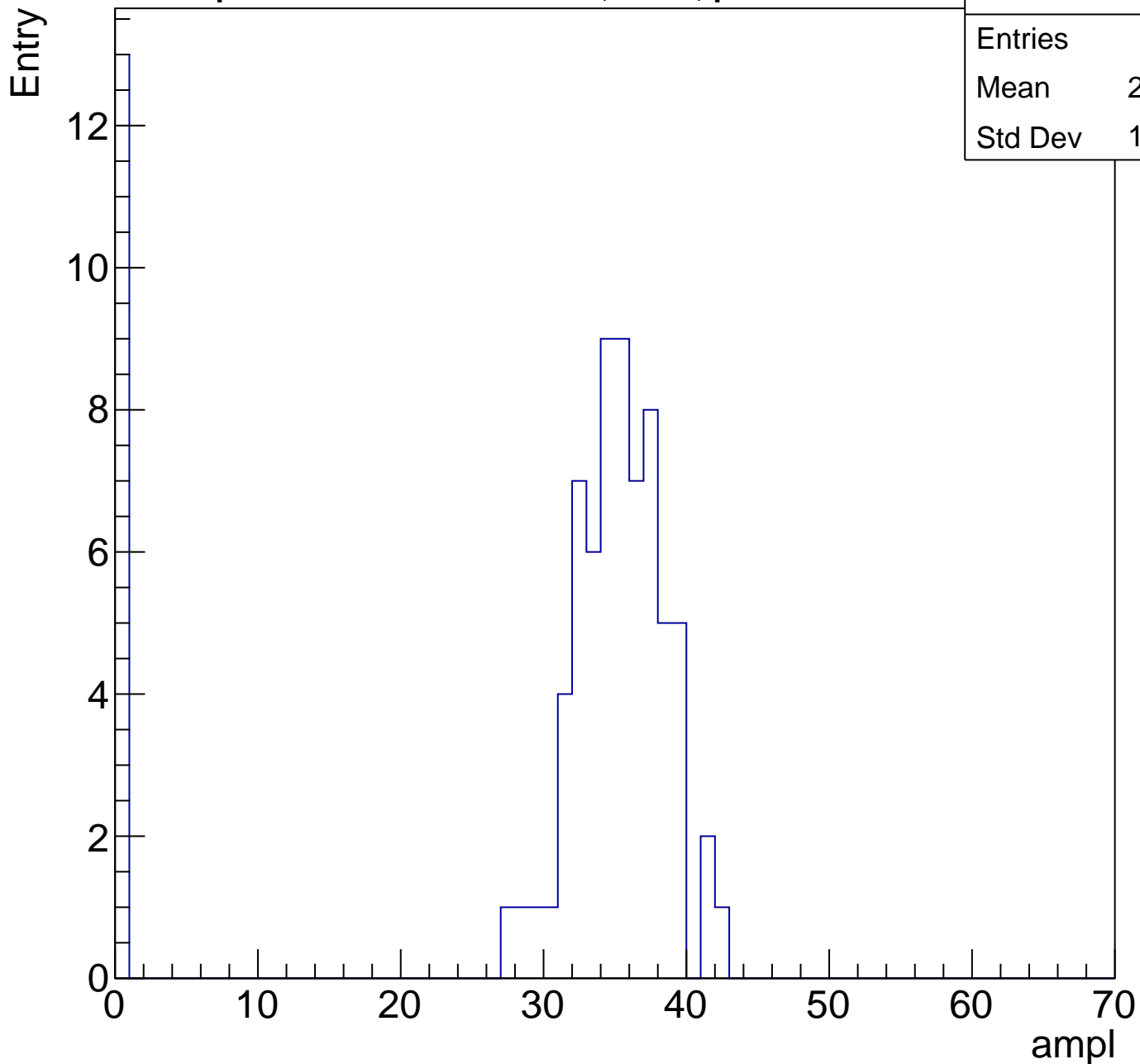
Entries	111
Mean	19.11
Std Dev	13.03



B1L103S, U23-ch42, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	80
Mean	29.23
Std Dev	13.17



B1L103S, U23-ch42, adc2

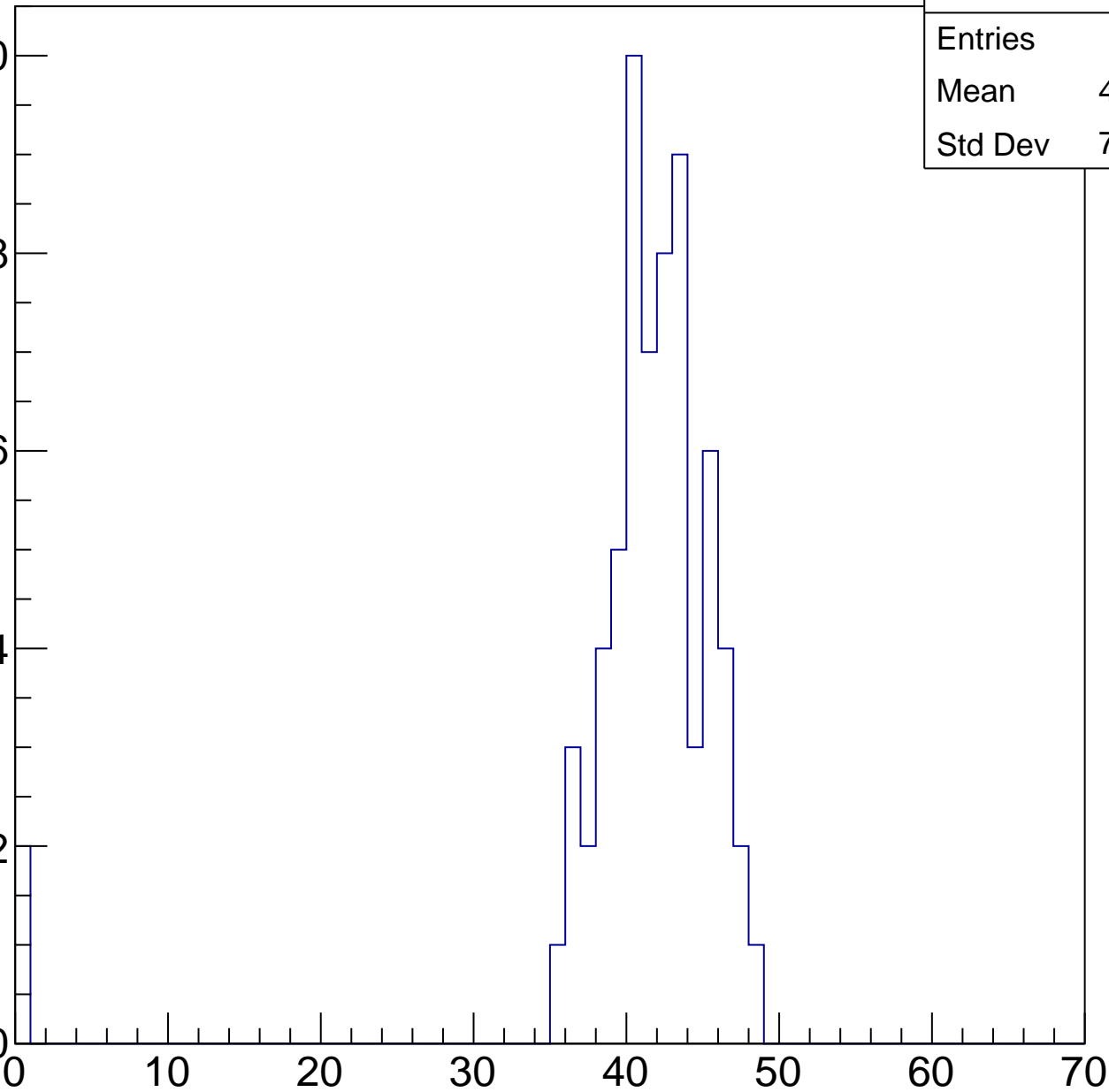
calib_packv5_041523_1651.root, FC#0, port C2

Entries	67
Mean	40.33
Std Dev	7.658

Entry

10
8
6
4
2
0

ampl

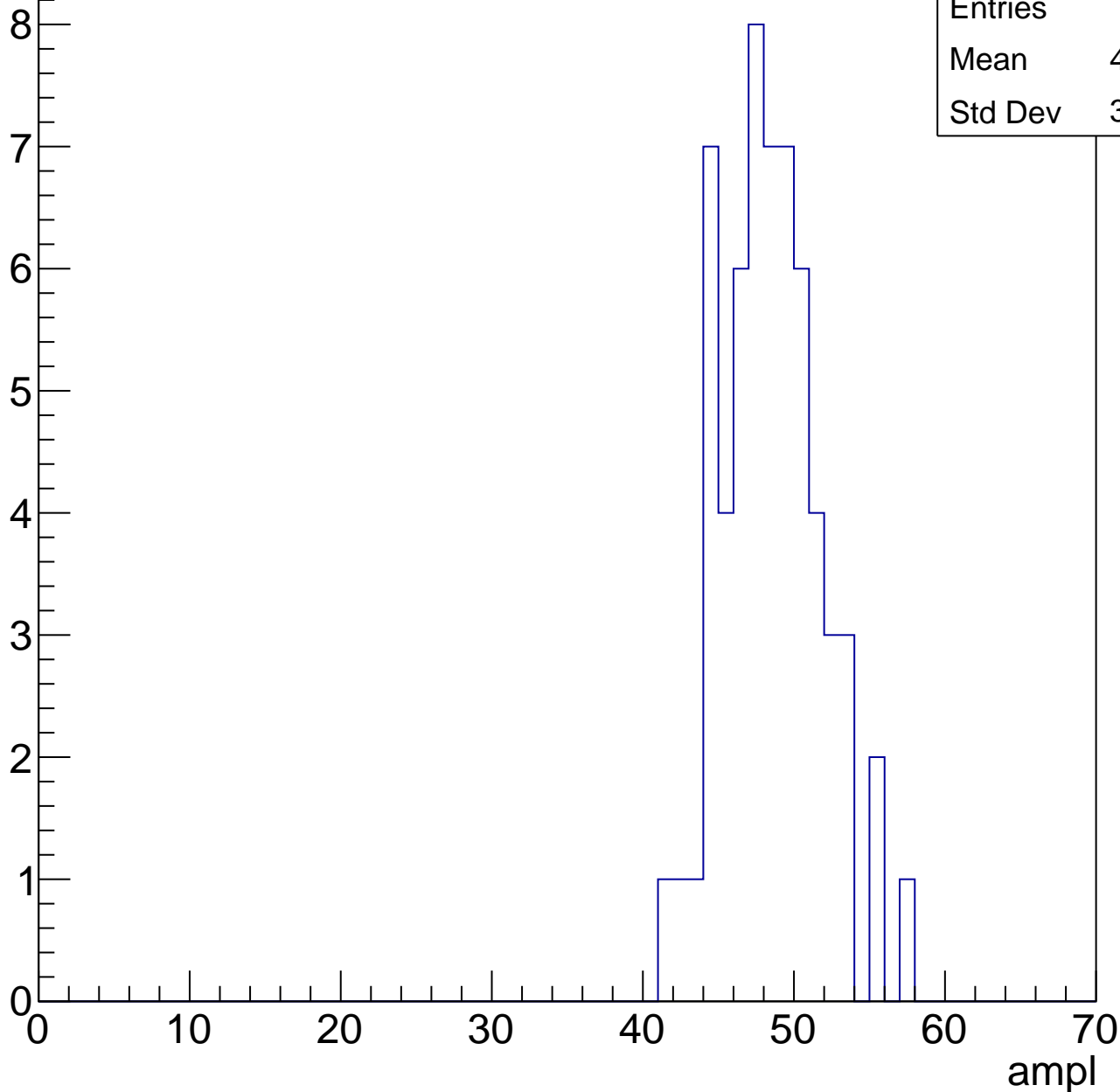


B1L103S, U23-ch42, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	48.05
Std Dev	3.286

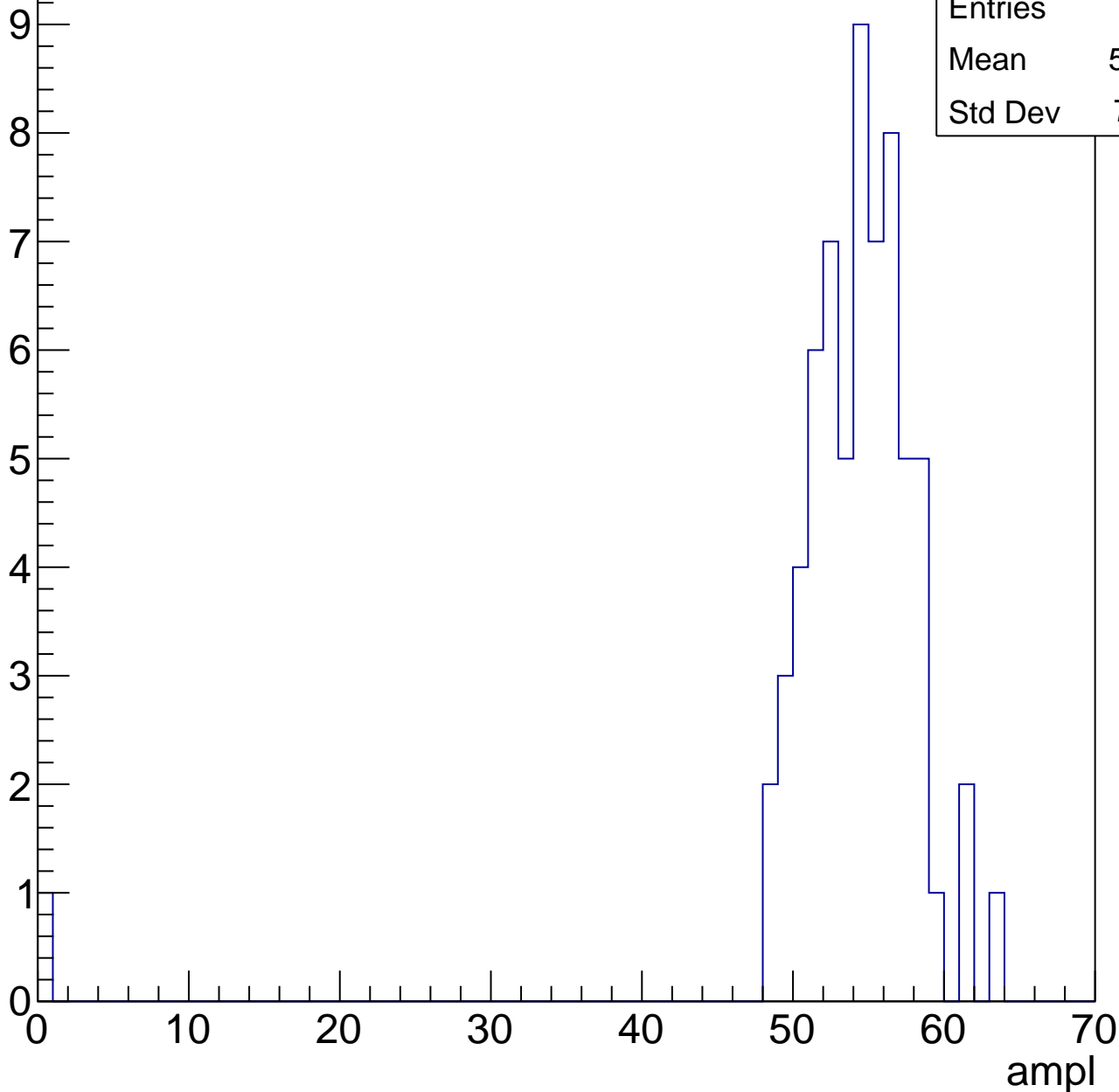


B1L103S, U23-ch42, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

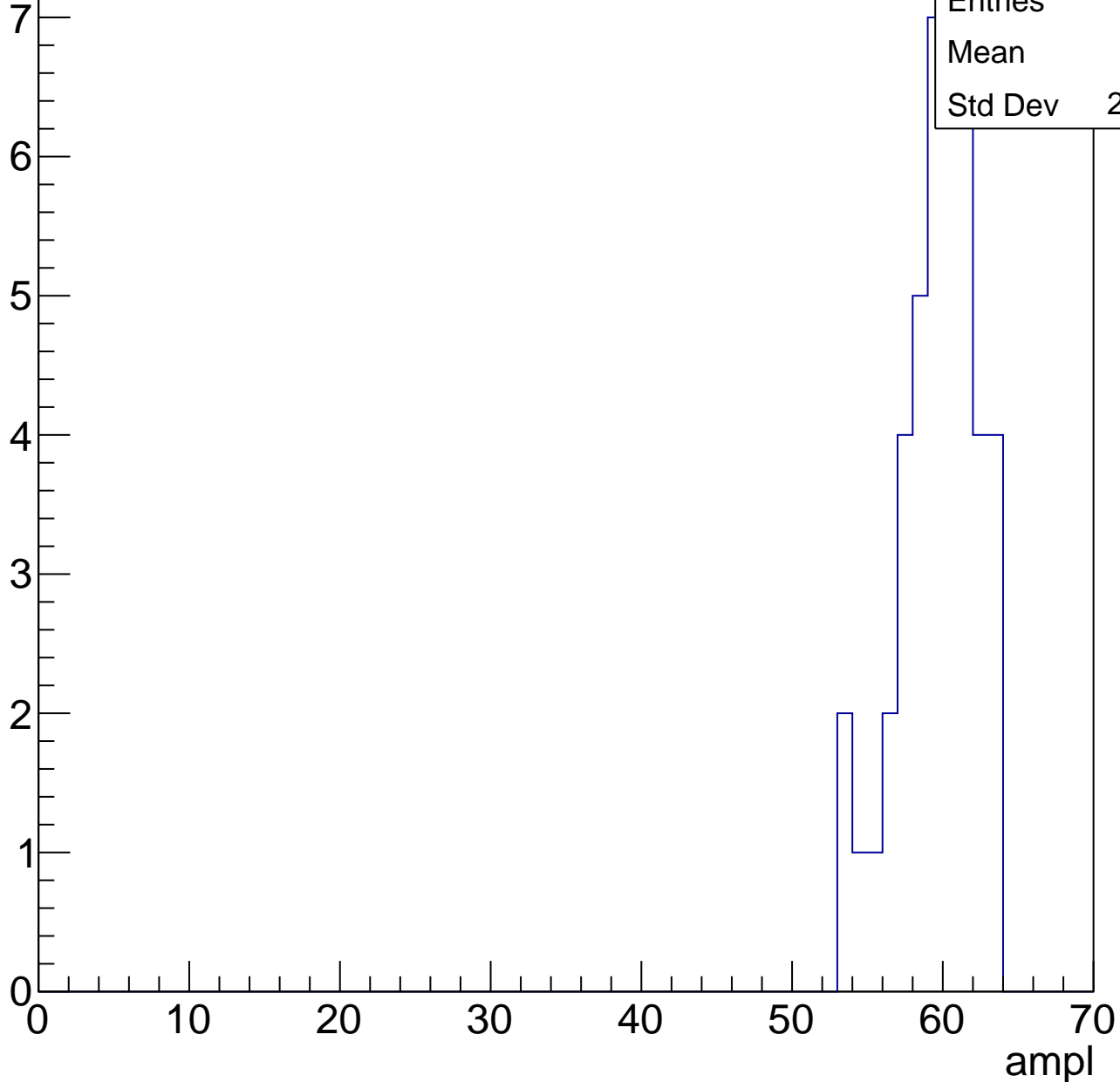
Entries	66
Mean	53.27
Std Dev	7.331



B1L103S, U23-ch42, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

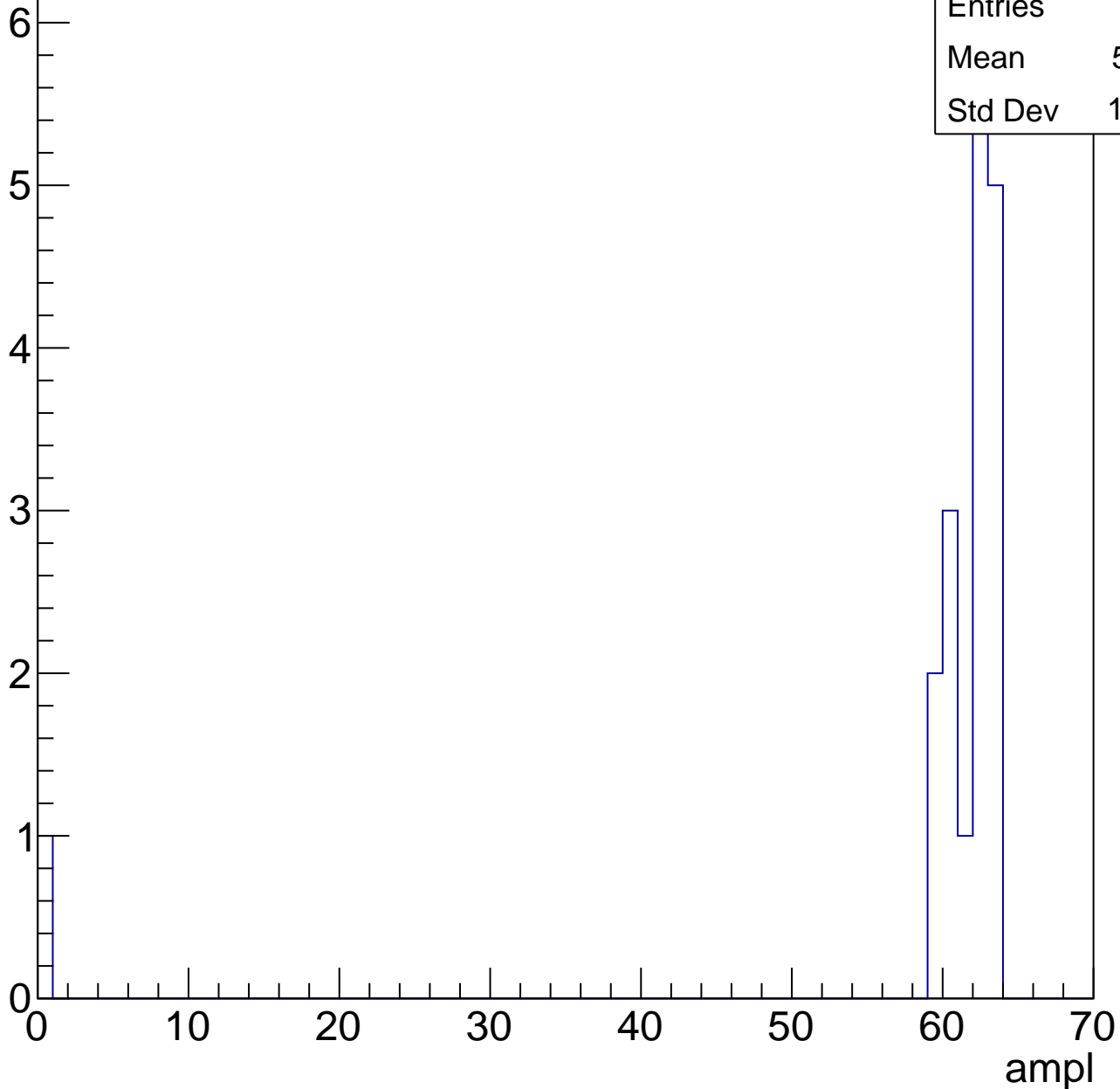


B1L103S, U23-ch42, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	18
Mean	58.11
Std Dev	14.16



B1L103S, U23-ch42, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

ampl

B1L103S, U23-ch43, adc0

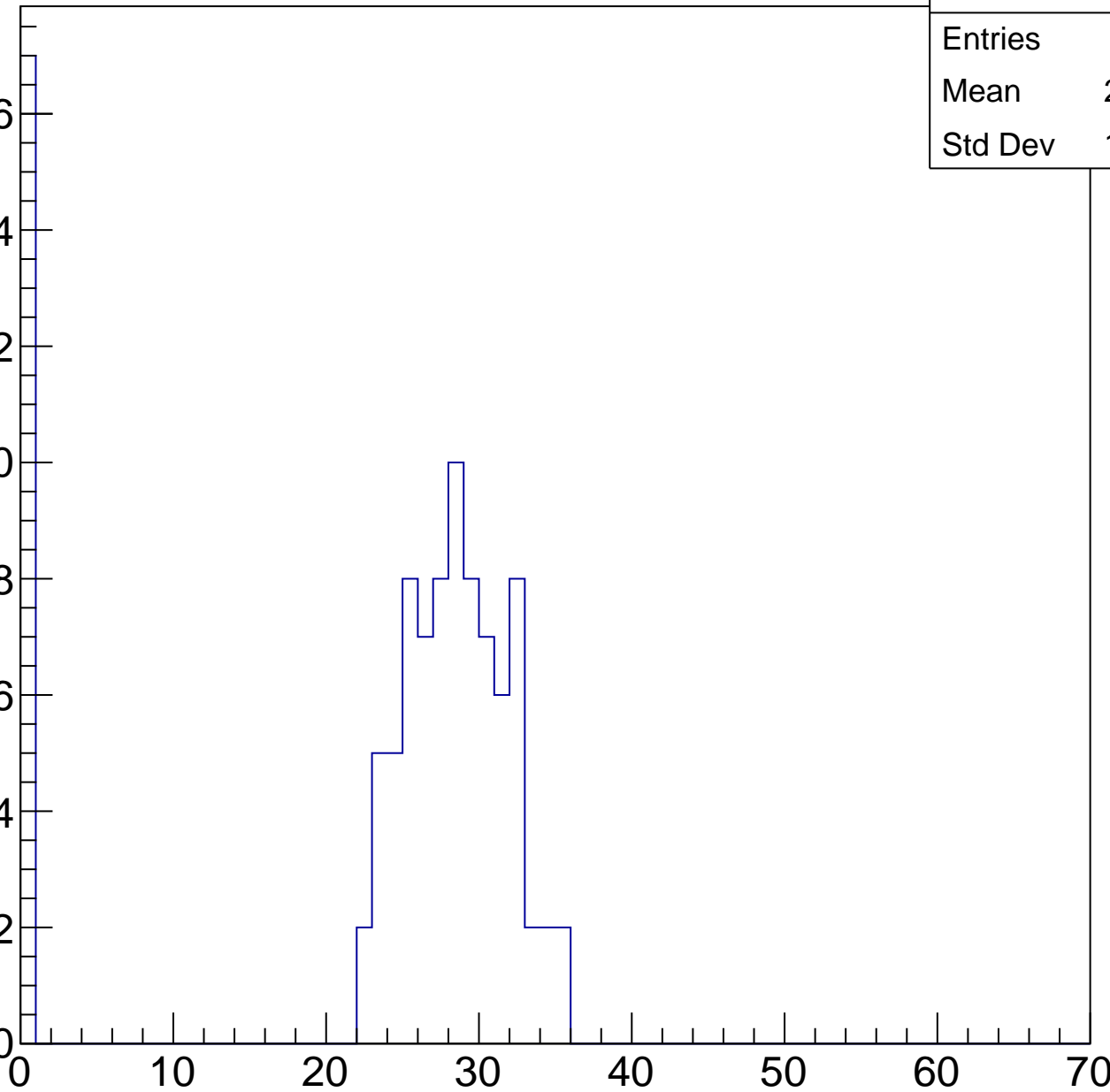
calib_packv5_041523_1651.root, FC#0, port C2

Entries	97
Mean	23.14
Std Dev	11.06

Entry

16
14
12
10
8
6
4
2
0

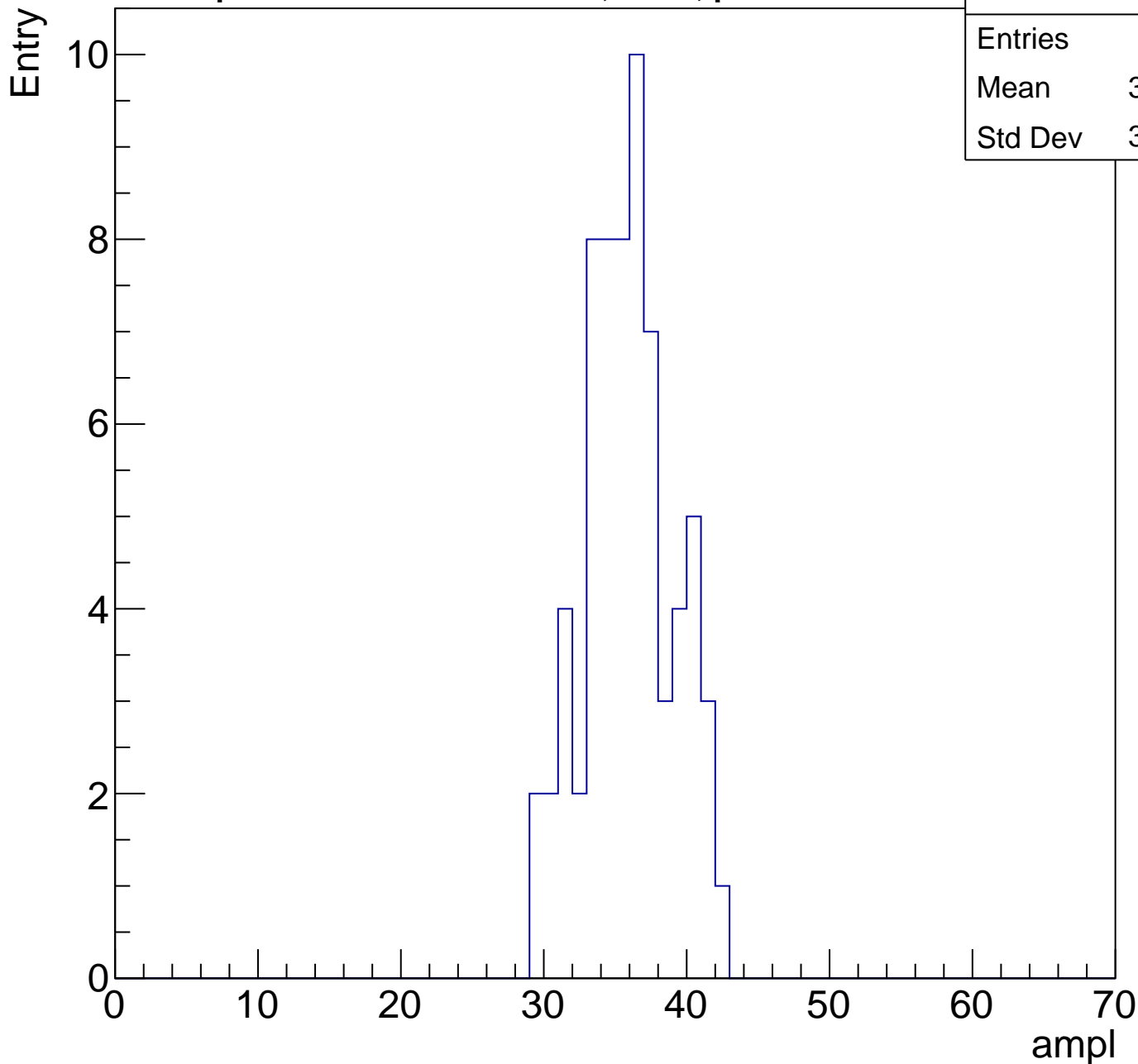
ampl



B1L103S, U23-ch43, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	67
Mean	35.46
Std Dev	3.092

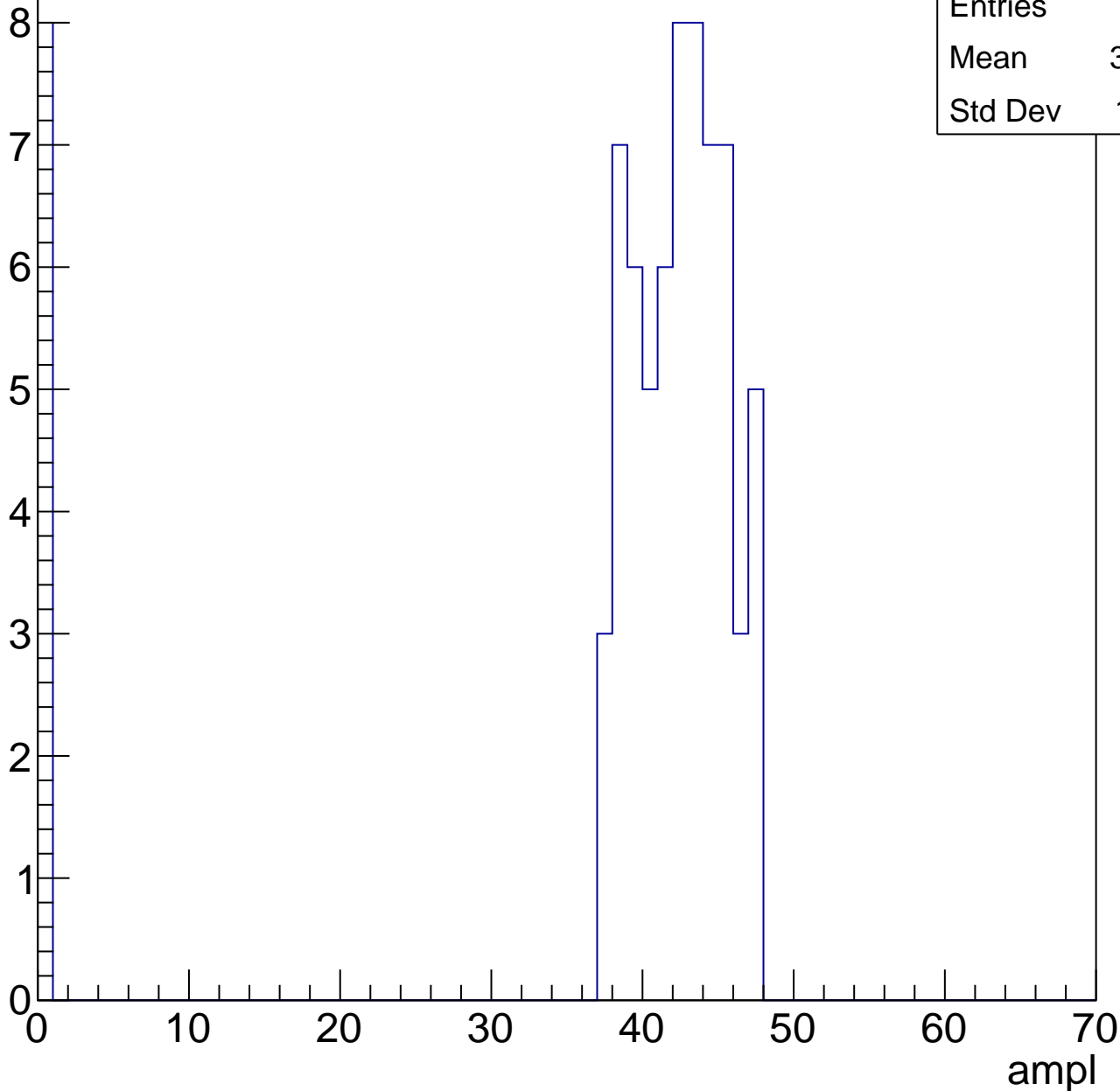


B1L103S, U23-ch43, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	73
Mean	37.44
Std Dev	13.41

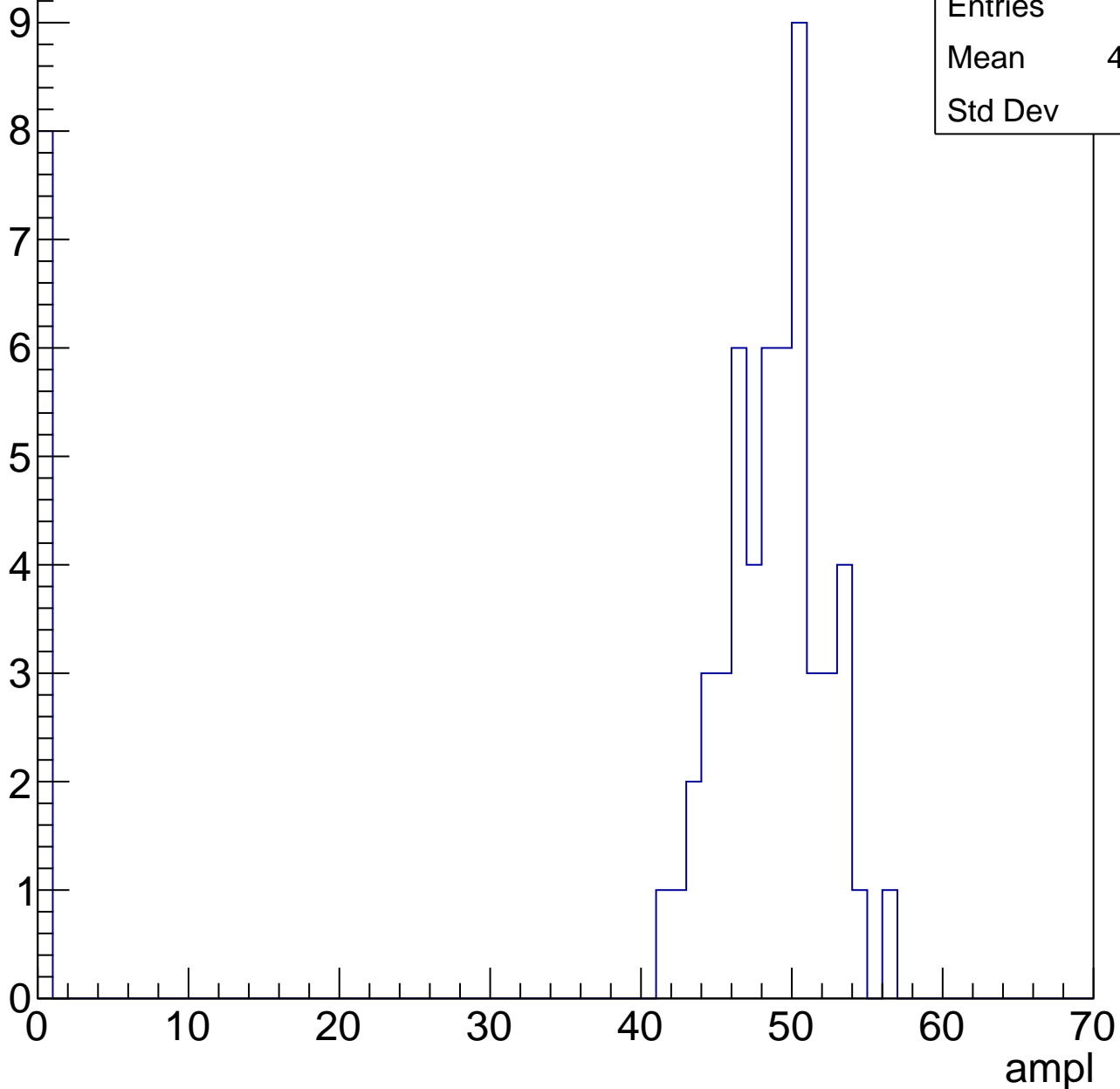


B1L103S, U23-ch43, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

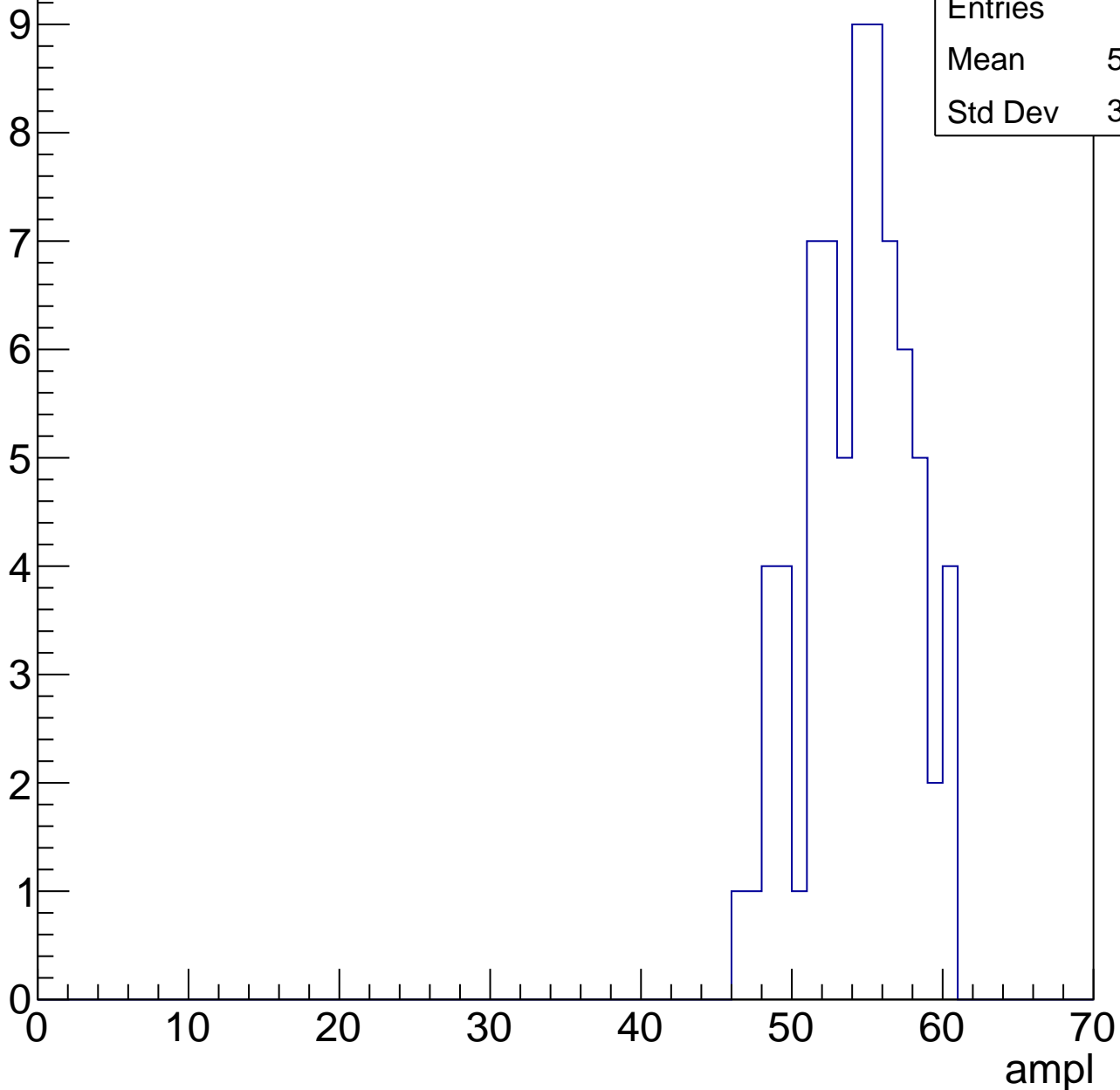
Entries	61
Mean	42.02
Std Dev	16.6



B1L103S, U23-ch43, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

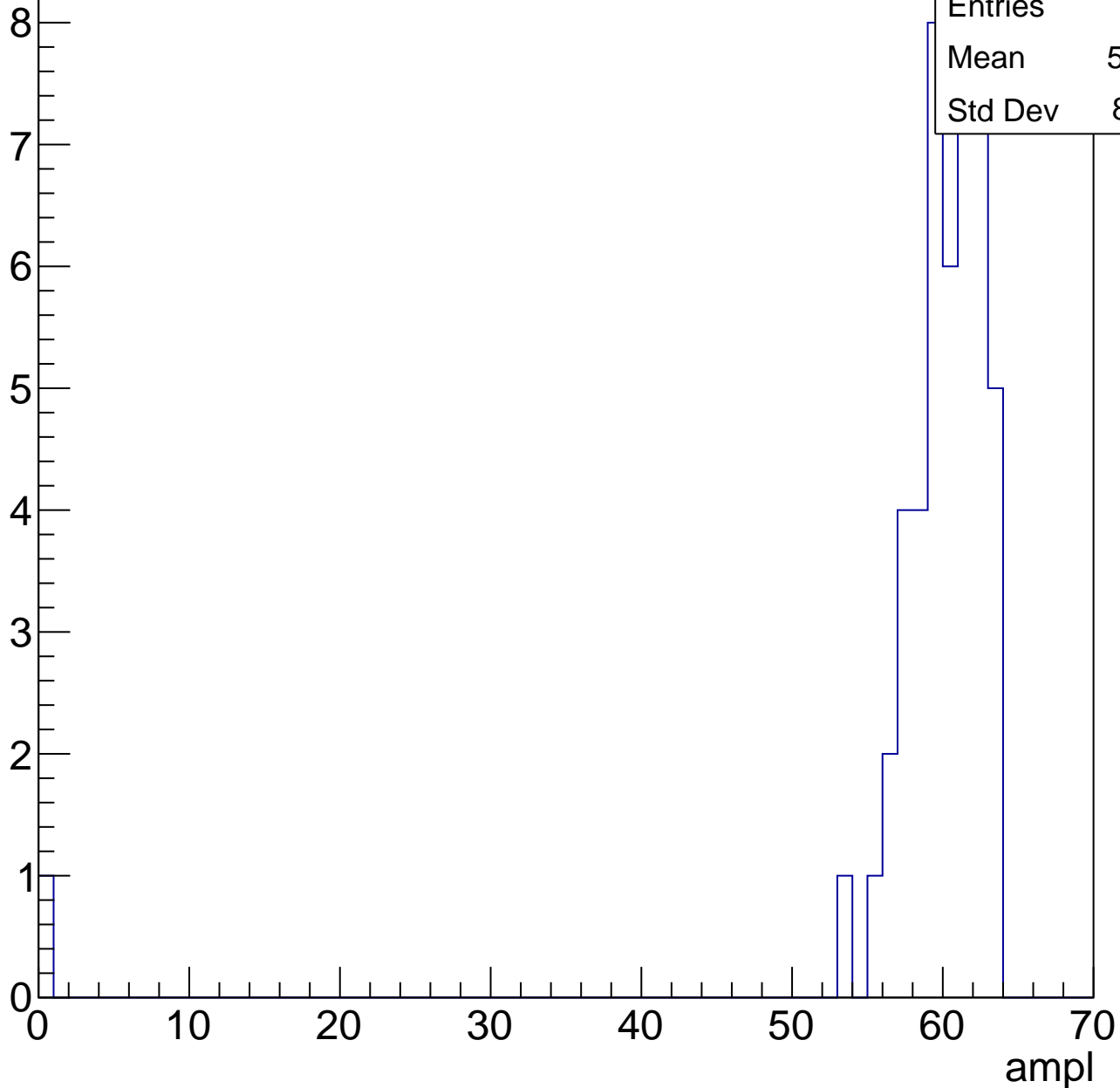


Entries	72
Mean	53.89
Std Dev	3.402

B1L103S, U23-ch43, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

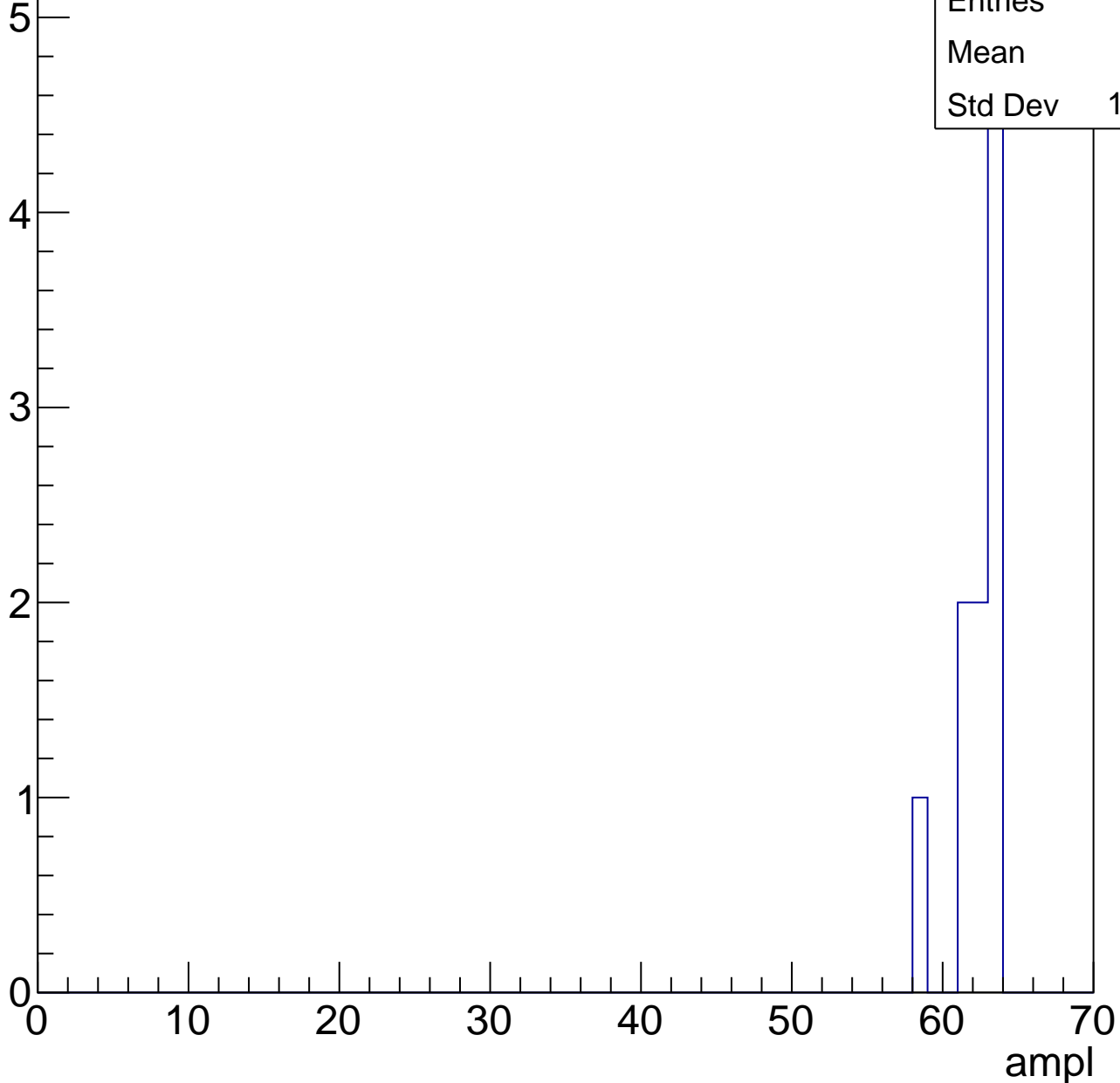


B1L103S, U23-ch43, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	10
Mean	61.9
Std Dev	1.513



B1L103S, U23-ch43, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	18
Mean	0
Std Dev	0

ampl

B1L103S, U23-ch44, adc0

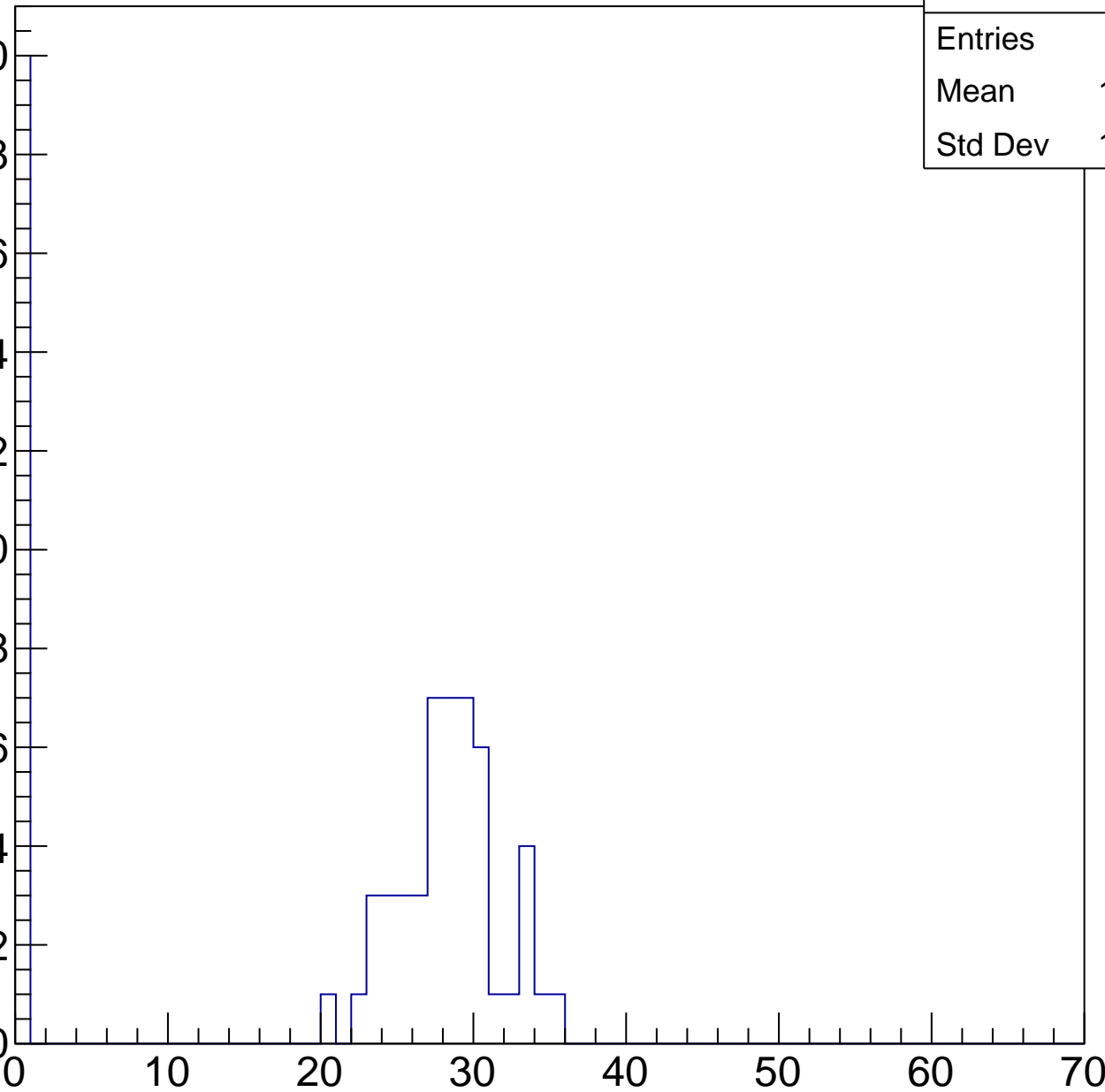
calib_packv5_041523_1651.root, FC#0, port C2

Entries	69
Mean	19.83
Std Dev	12.95

Entry

20
18
16
14
12
10
8
6
4
2
0

ampl

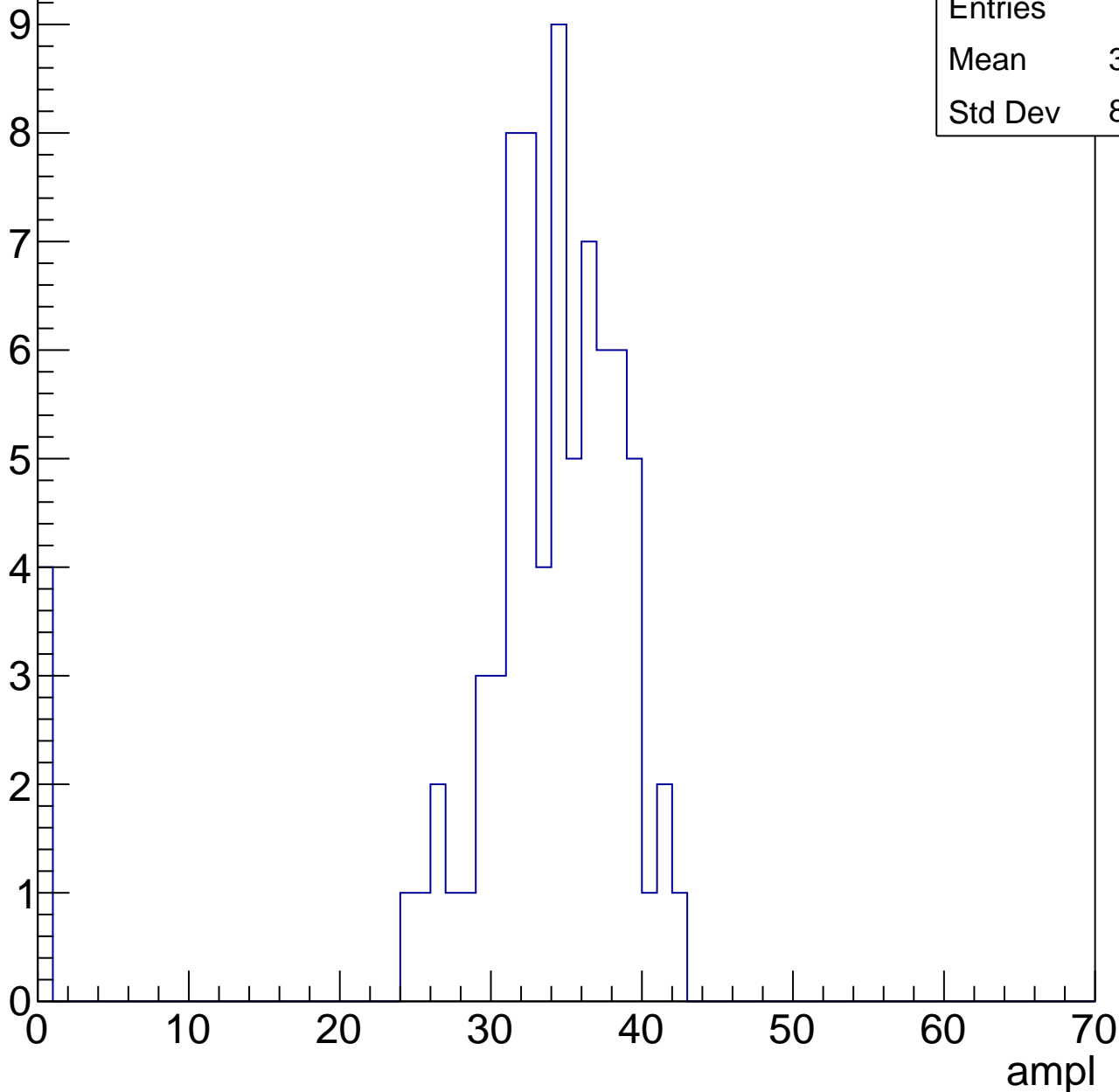


B1L103S, U23-ch44, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	78
Mean	32.19
Std Dev	8.397

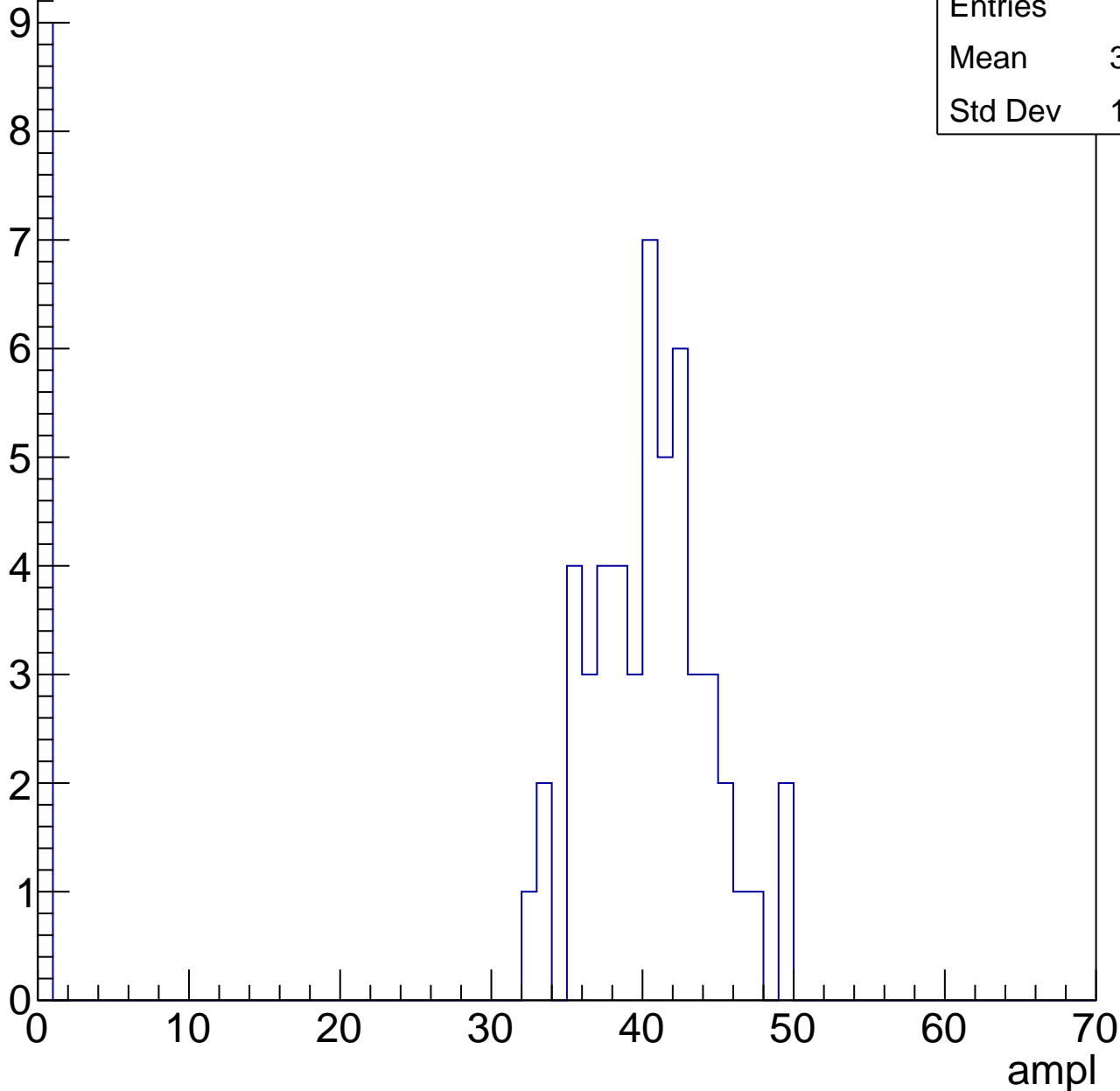


B1L103S, U23-ch44, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	34.03
Std Dev	14.74

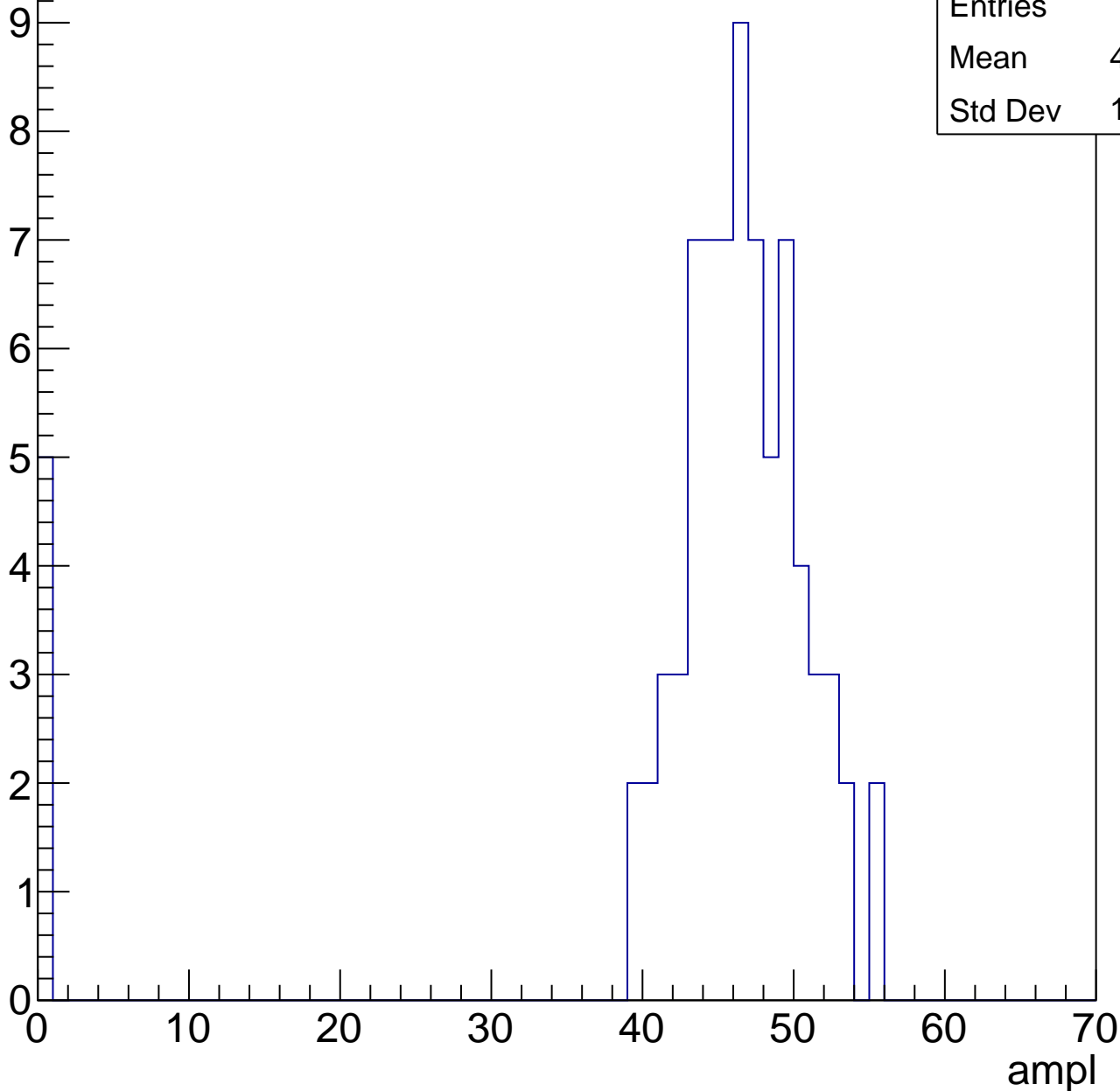


B1L103S, U23-ch44, adc3

calib_packv5_041523_1651.root, FC#0, port C2

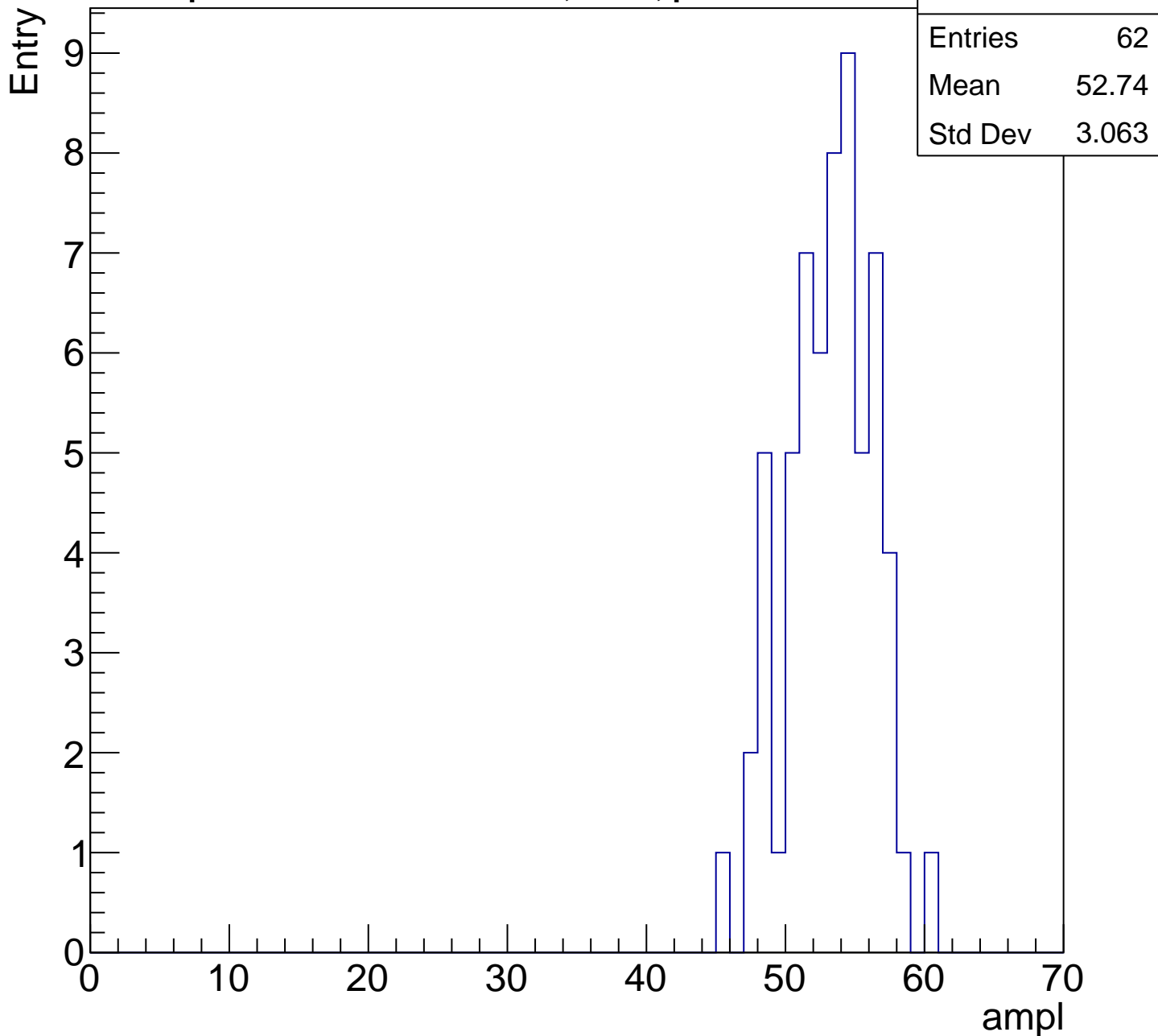
Entry

Entries	78
Mean	43.36
Std Dev	11.89



B1L103S, U23-ch44, adc4

calib_packv5_041523_1651.root, FC#0, port C2

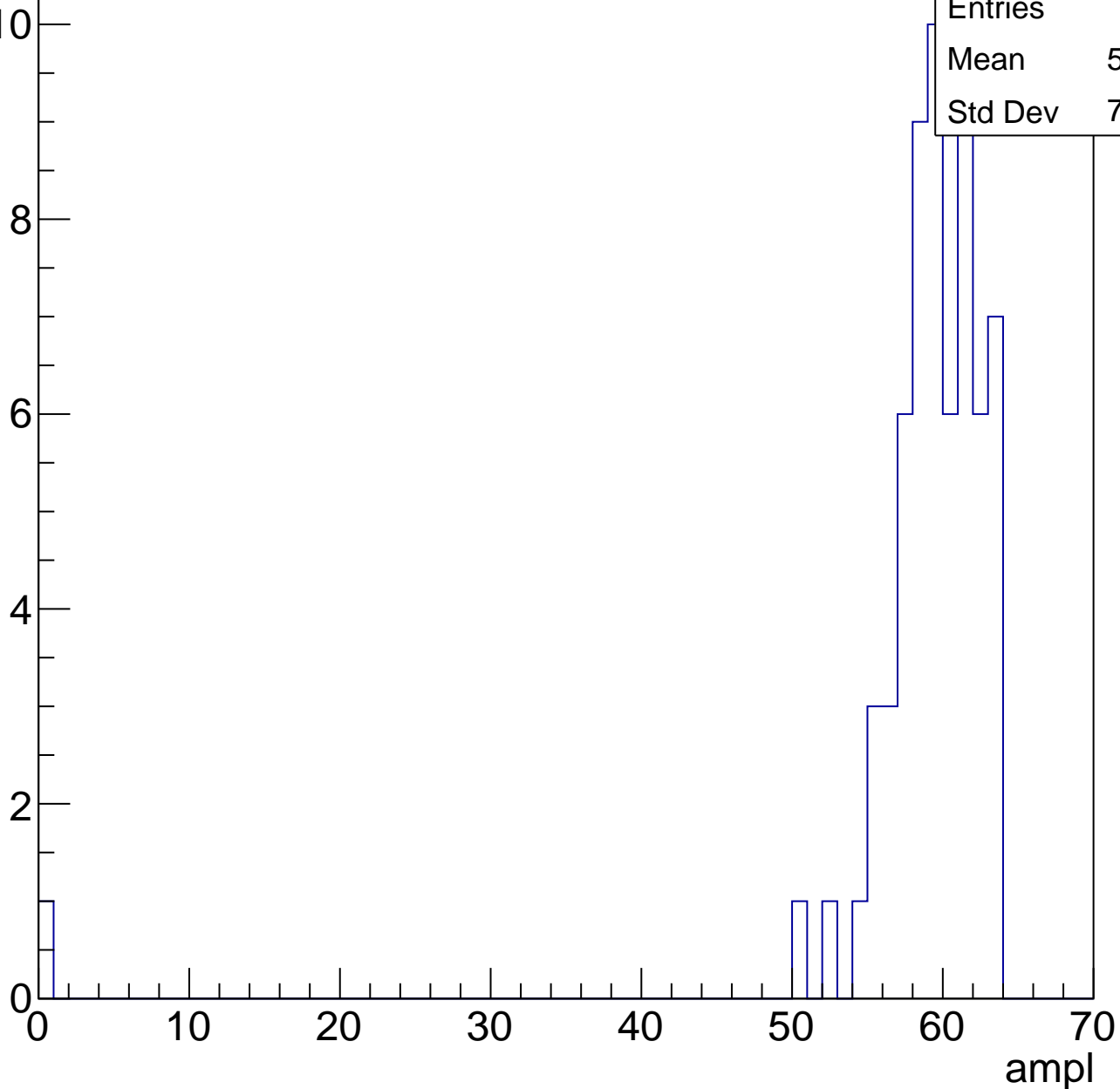


B1L103S, U23-ch44, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	63
Mean	58.17
Std Dev	7.877



B1L103S, U23-ch44, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

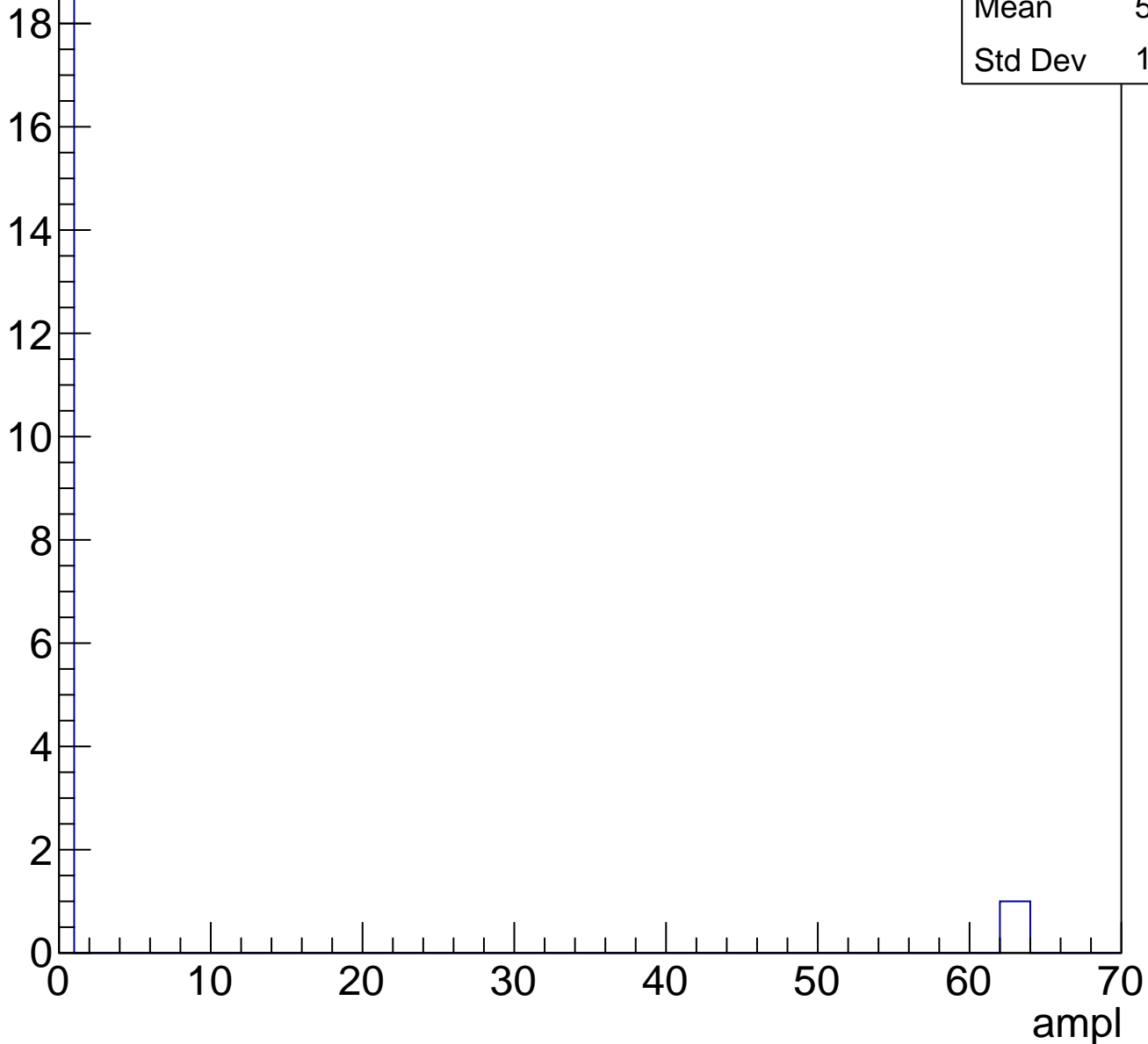
Entries	9
Mean	61.44
Std Dev	1.165

B1L103S, U23-ch44, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	21
Mean	5.952
Std Dev	18.35

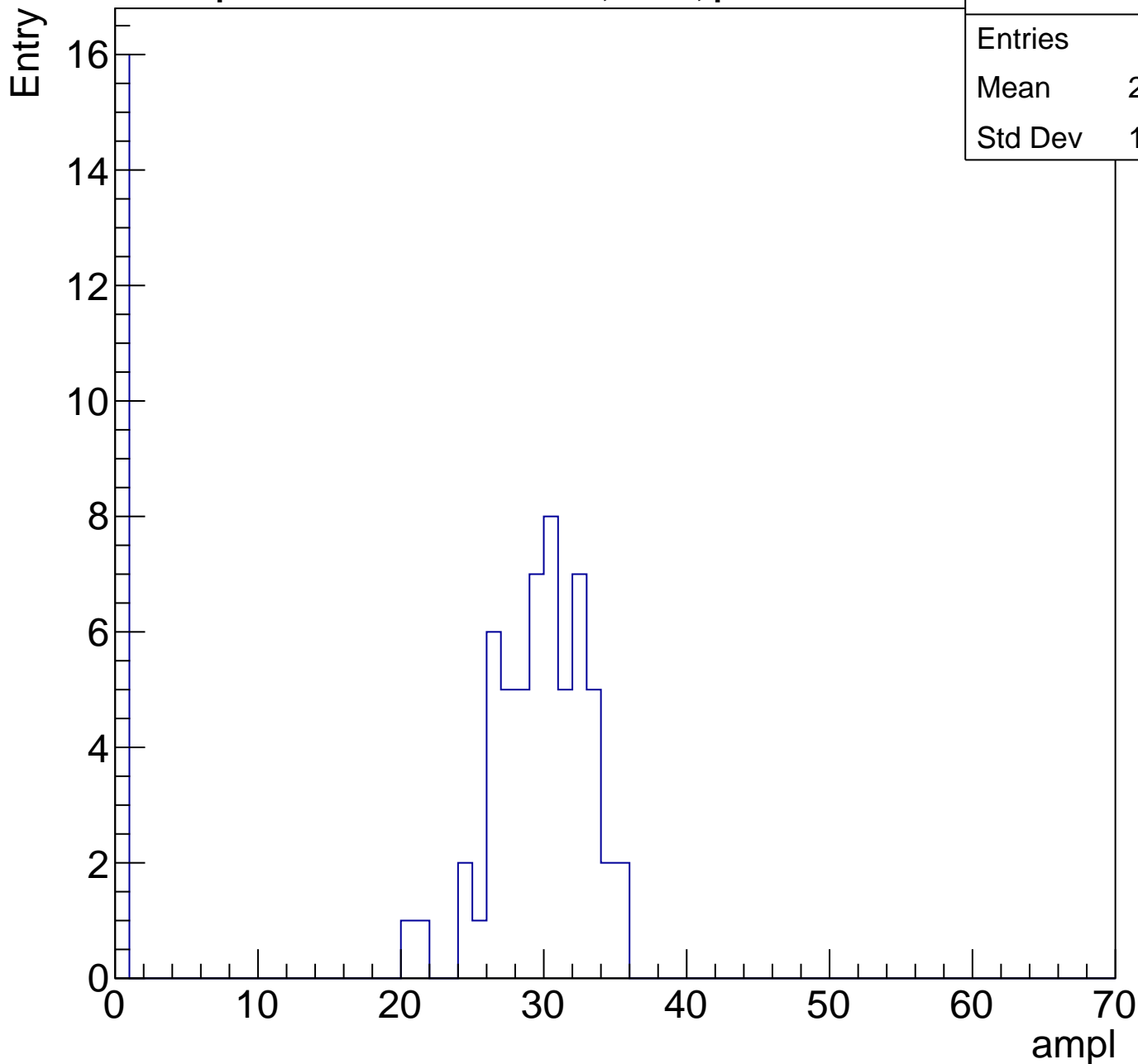
Entry



B1L103S, U23-ch45, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	73
Mean	22.88
Std Dev	12.44

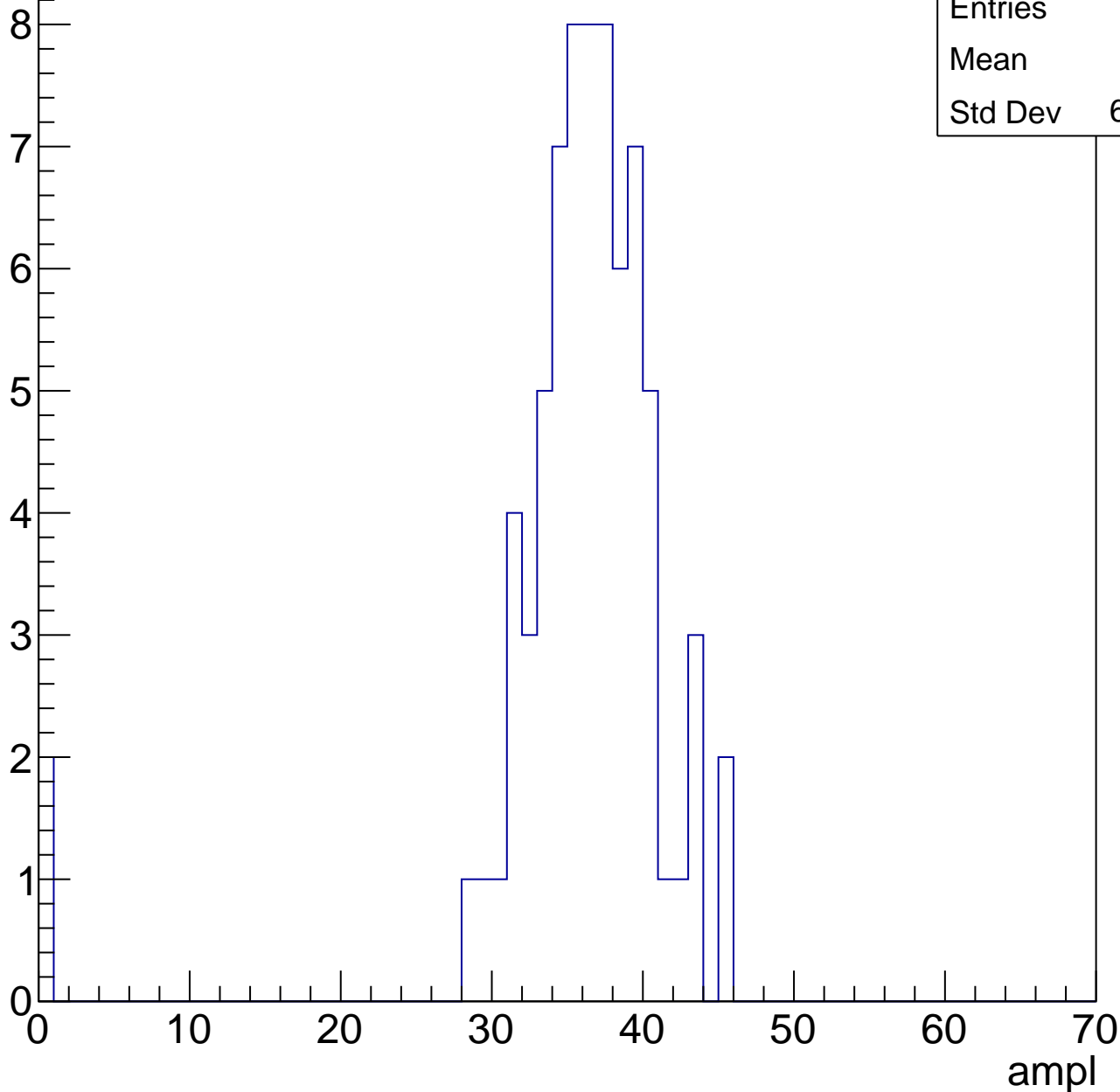


B1L103S, U23-ch45, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

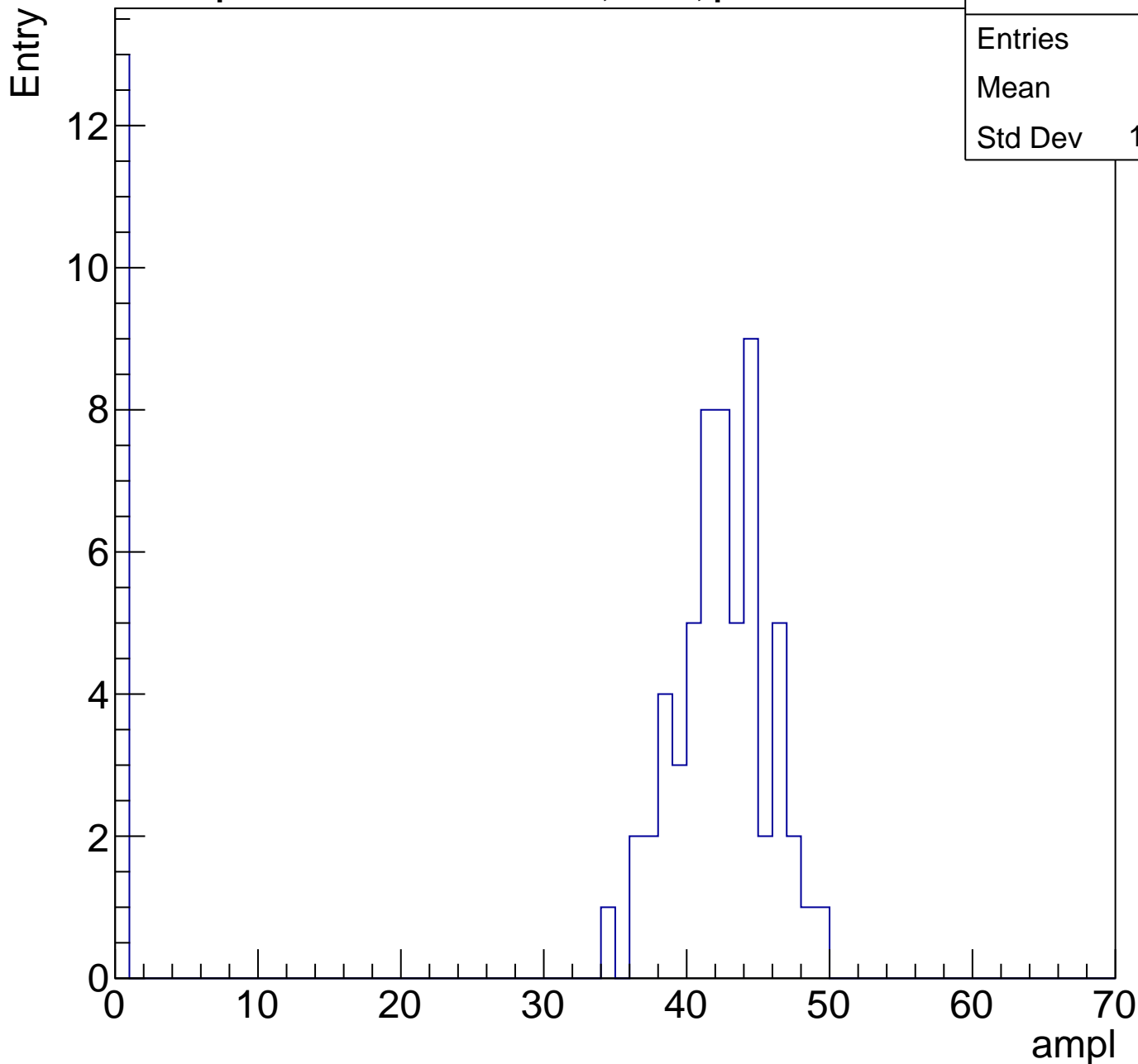
Entries	73
Mean	35.3
Std Dev	6.904



B1L103S, U23-ch45, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	71
Mean	34.3
Std Dev	16.49

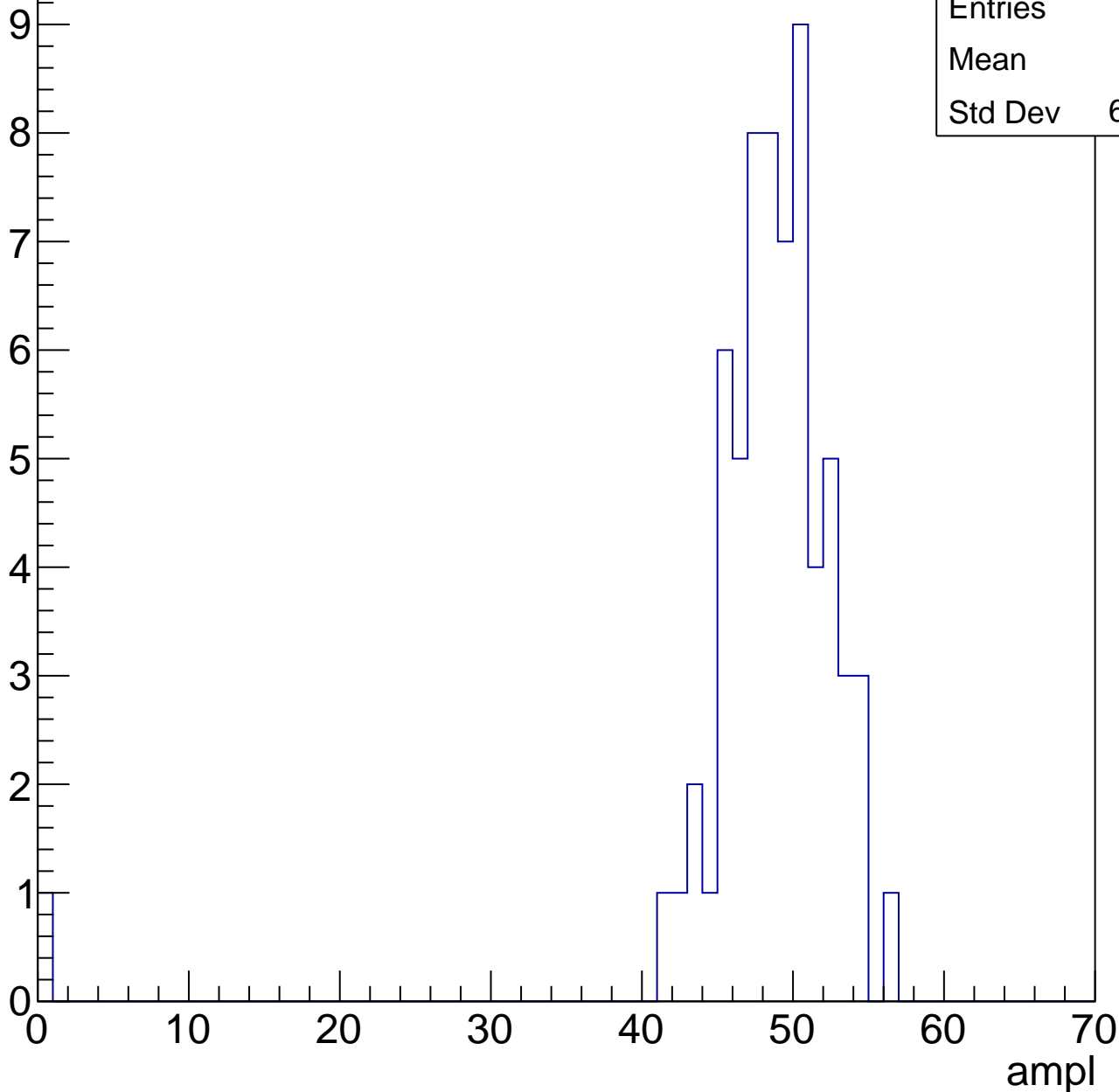


B1L103S, U23-ch45, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	47.8
Std Dev	6.726



B1L103S, U23-ch45, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entries	67
Mean	54.9
Std Dev	2.983

Entry

10

8

6

4

2

0

0

10

20

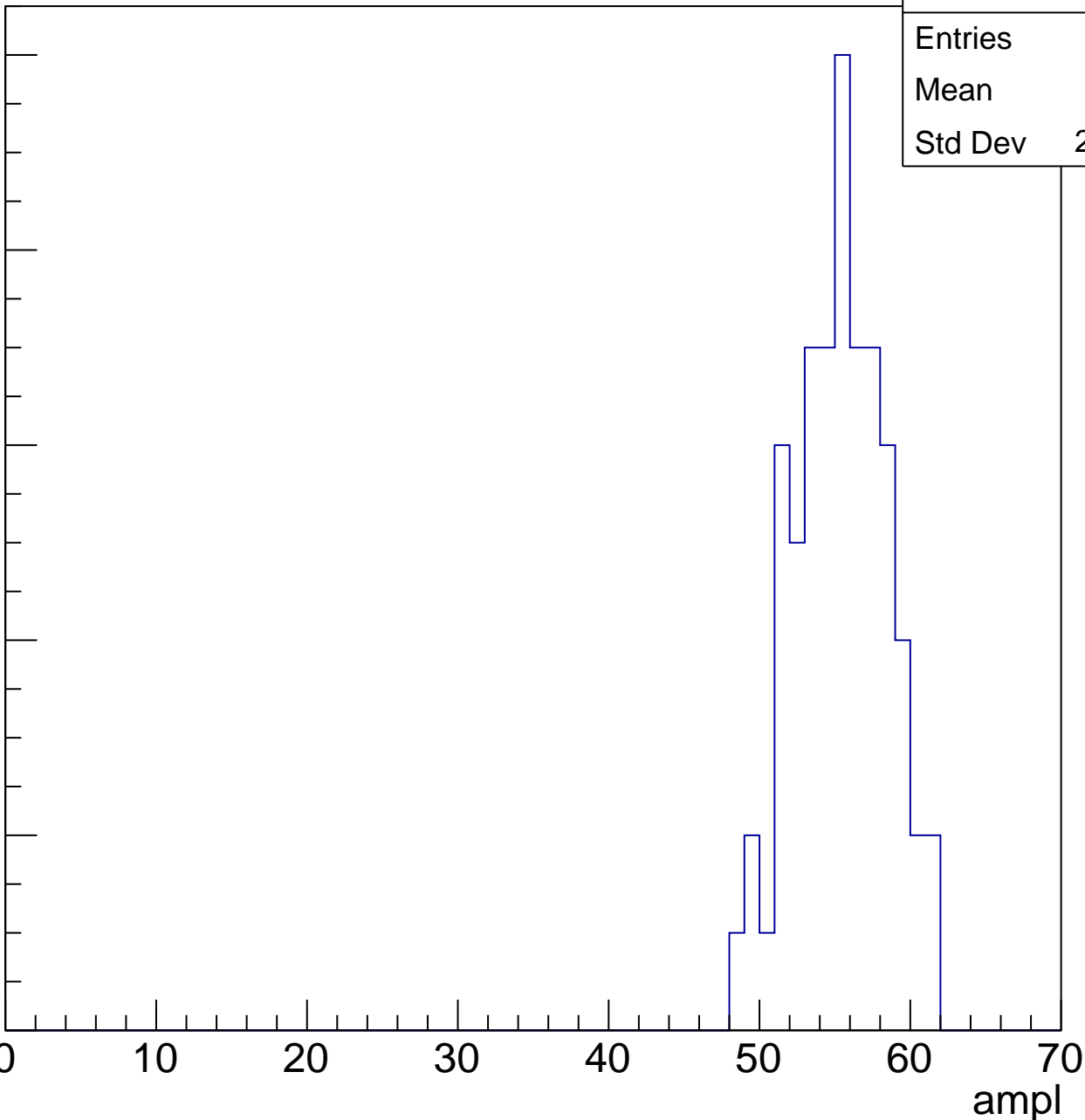
30

40

50

60

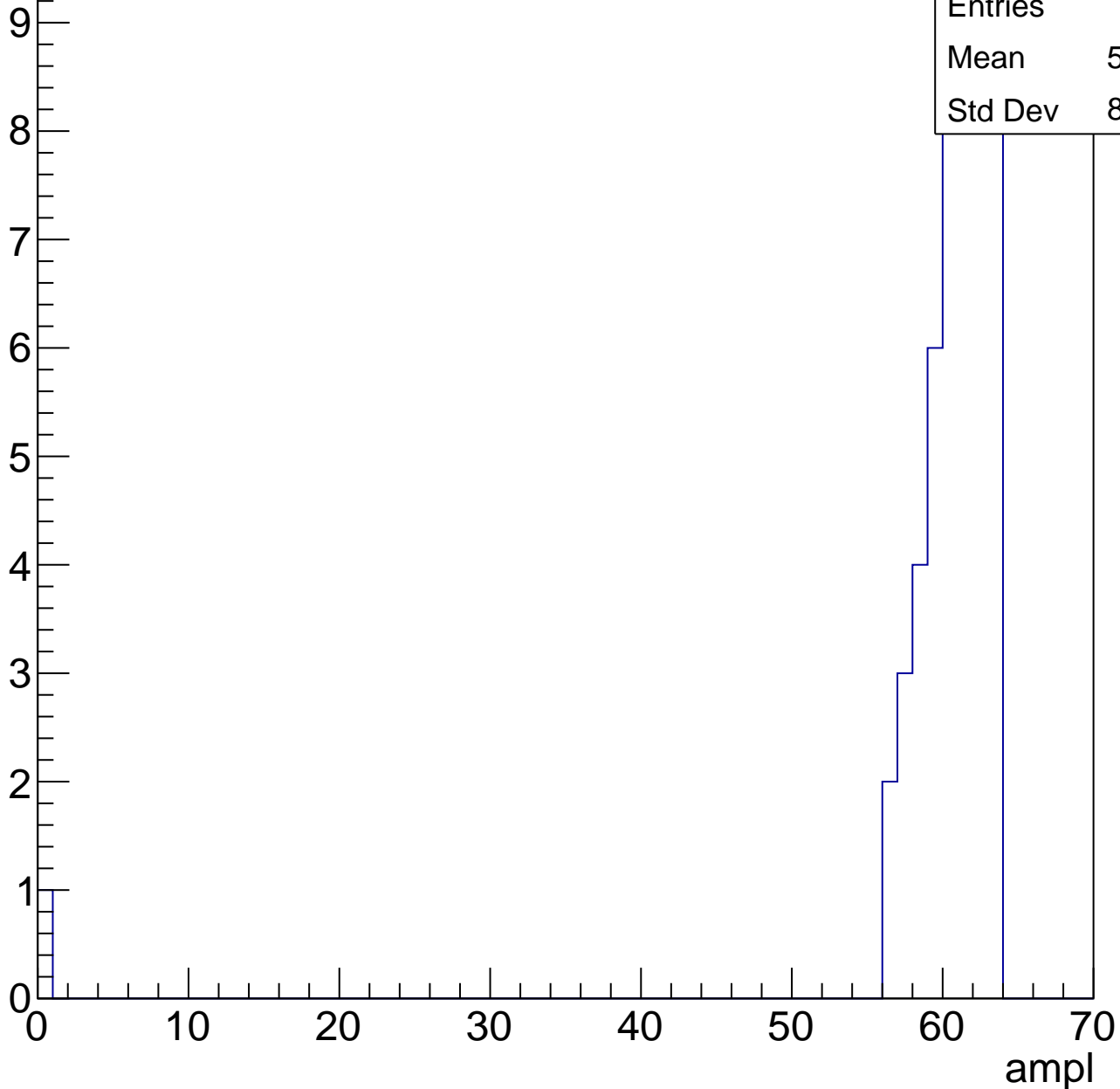
ampl



B1L103S, U23-ch45, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch45, adc6

calib_packv5_041523_1651.root, FC#0, port C2

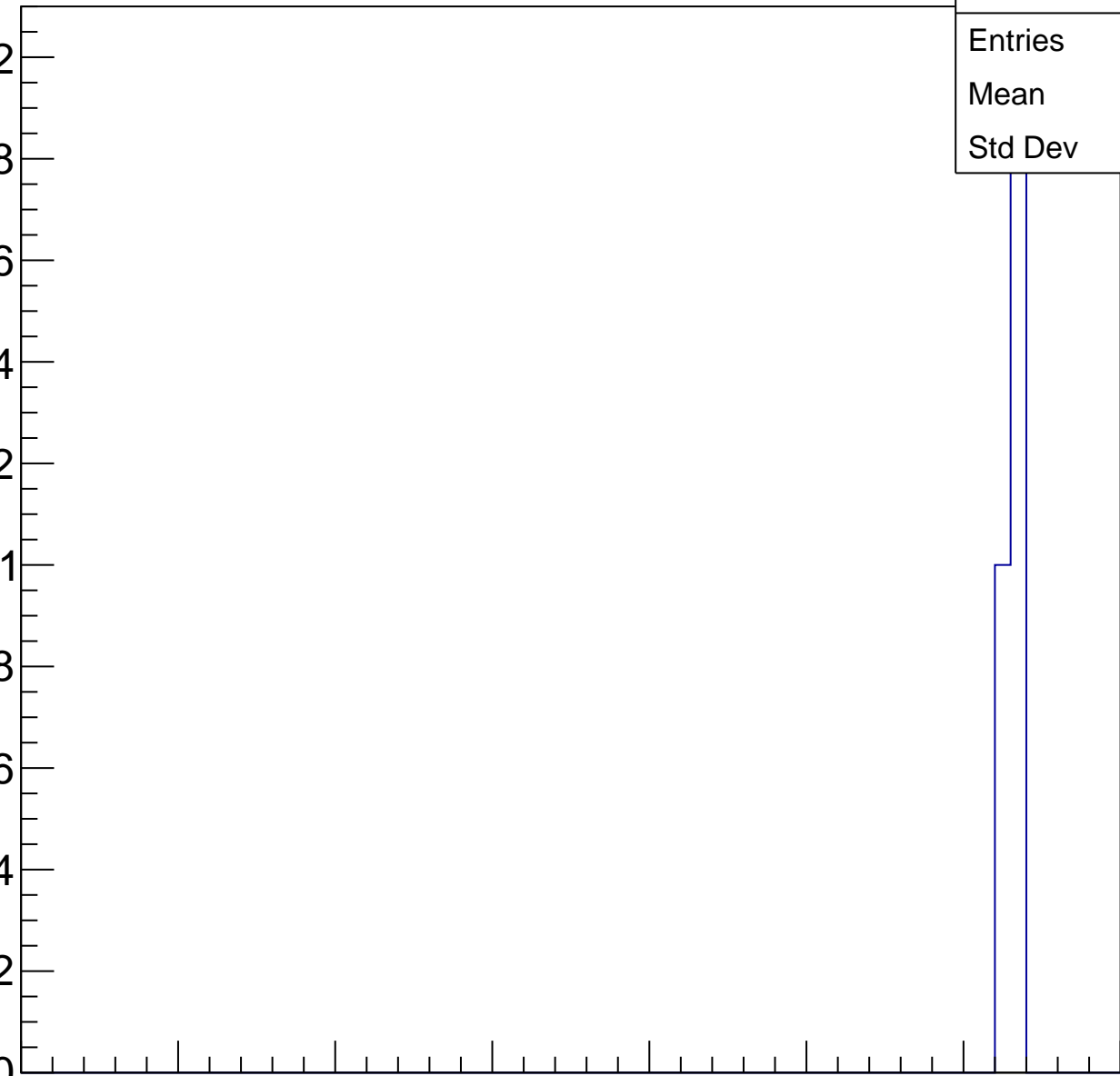
Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	3
Mean	62.67
Std Dev	0.4714

ampl

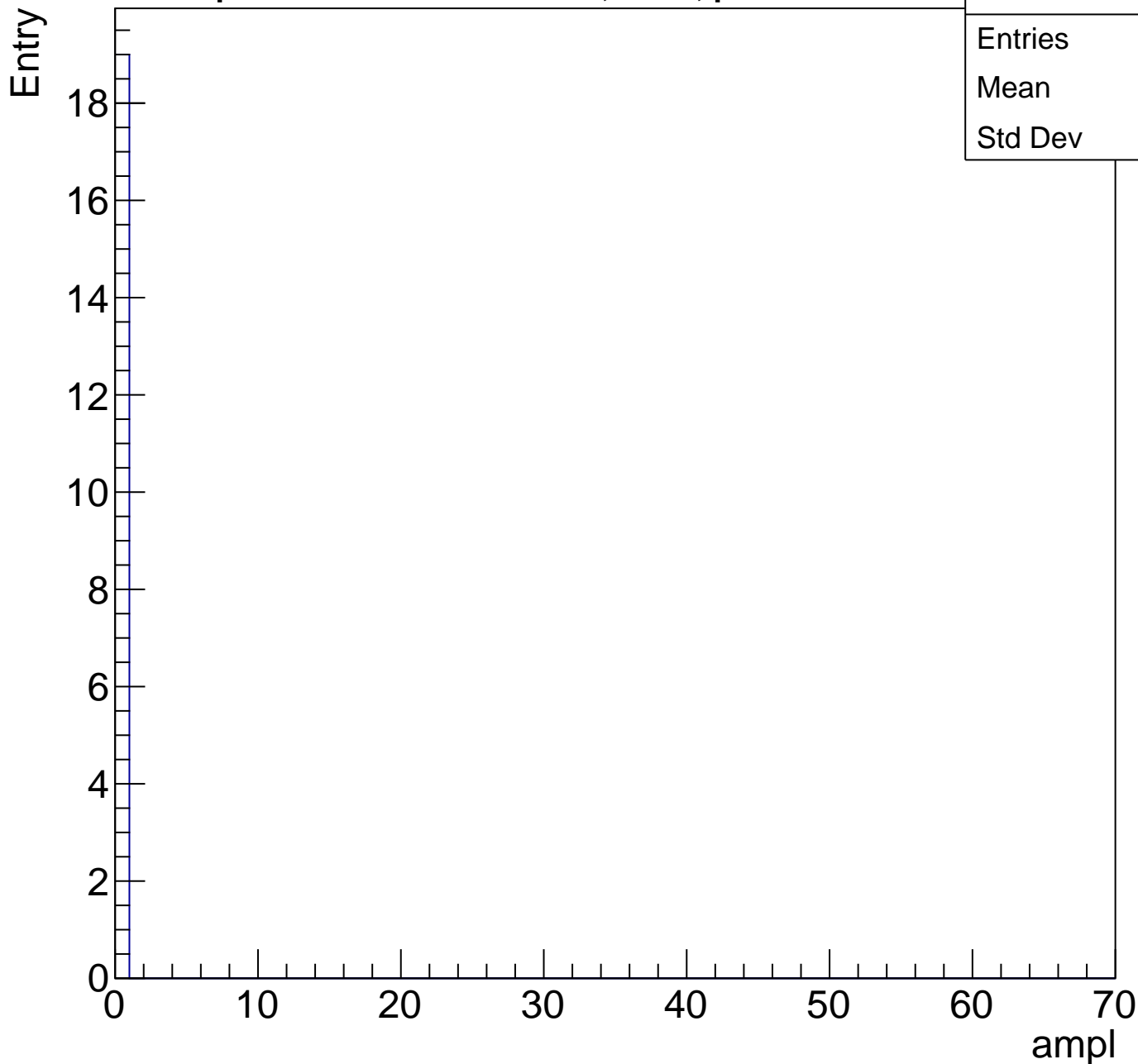
0 10 20 30 40 50 60 70



B1L103S, U23-ch45, adc7

calib_packv5_041523_1651.root, FC#0, port C2

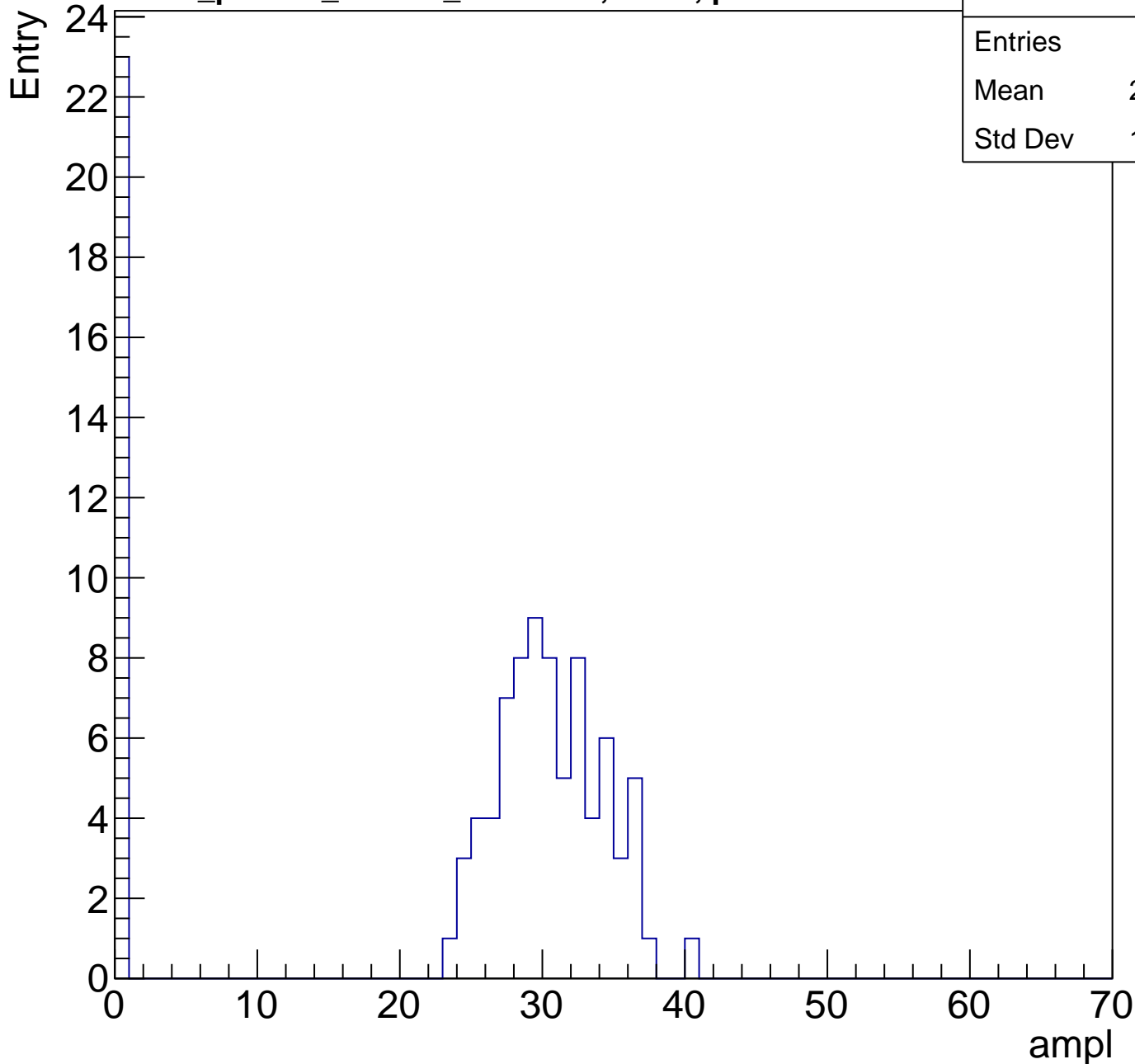
Entries	19
Mean	0
Std Dev	0



B1L103S, U23-ch46, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	100
Mean	23.22
Std Dev	13.08



B1L103S, U23-ch46, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	78
Mean	30.77
Std Dev	14.15

Entry

12

10

8

6

4

2

0

0

10

20

30

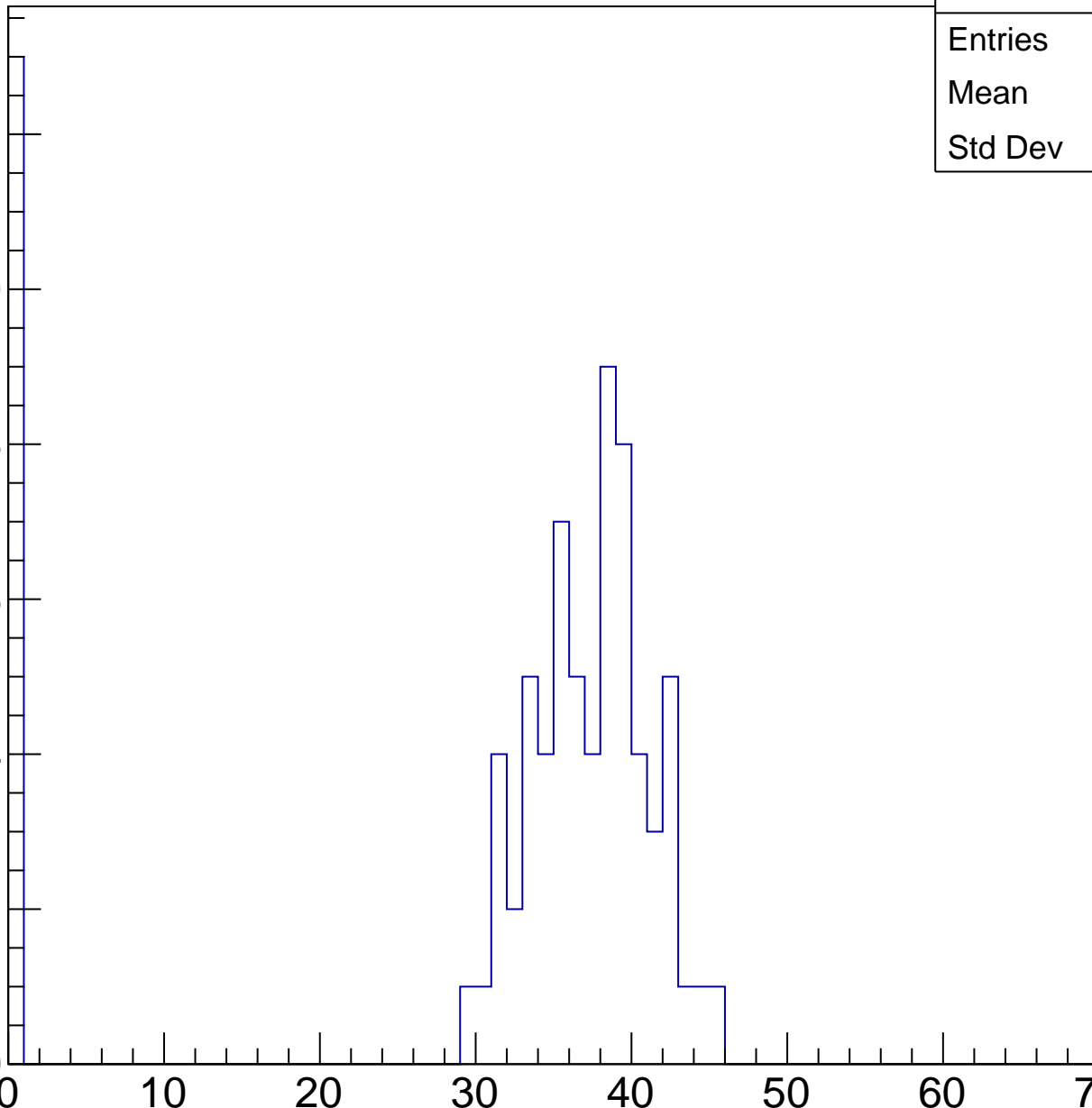
40

50

60

70

ampl

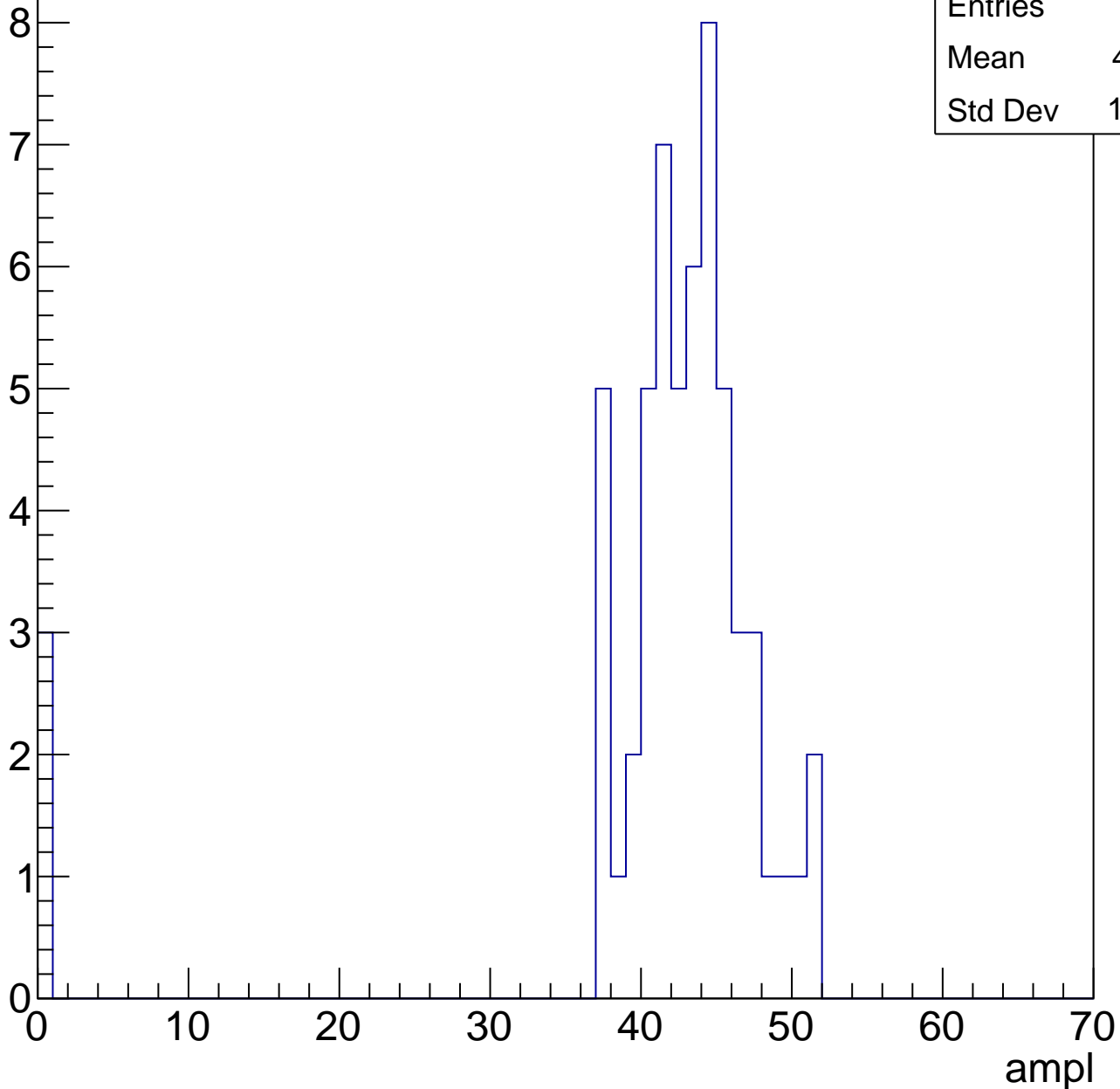


B1L103S, U23-ch46, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	40.71
Std Dev	10.08

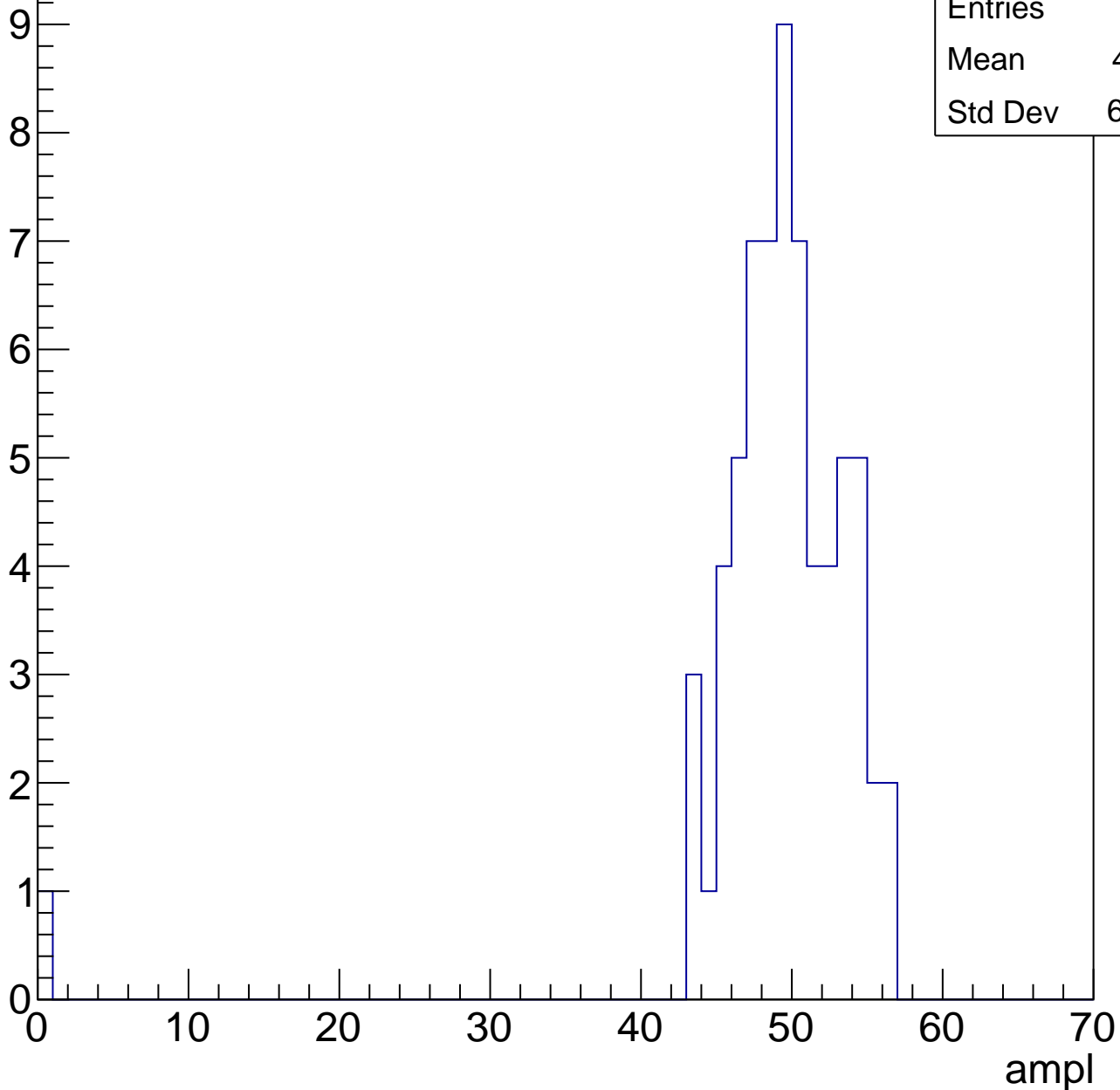


B1L103S, U23-ch46, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	48.61
Std Dev	6.855

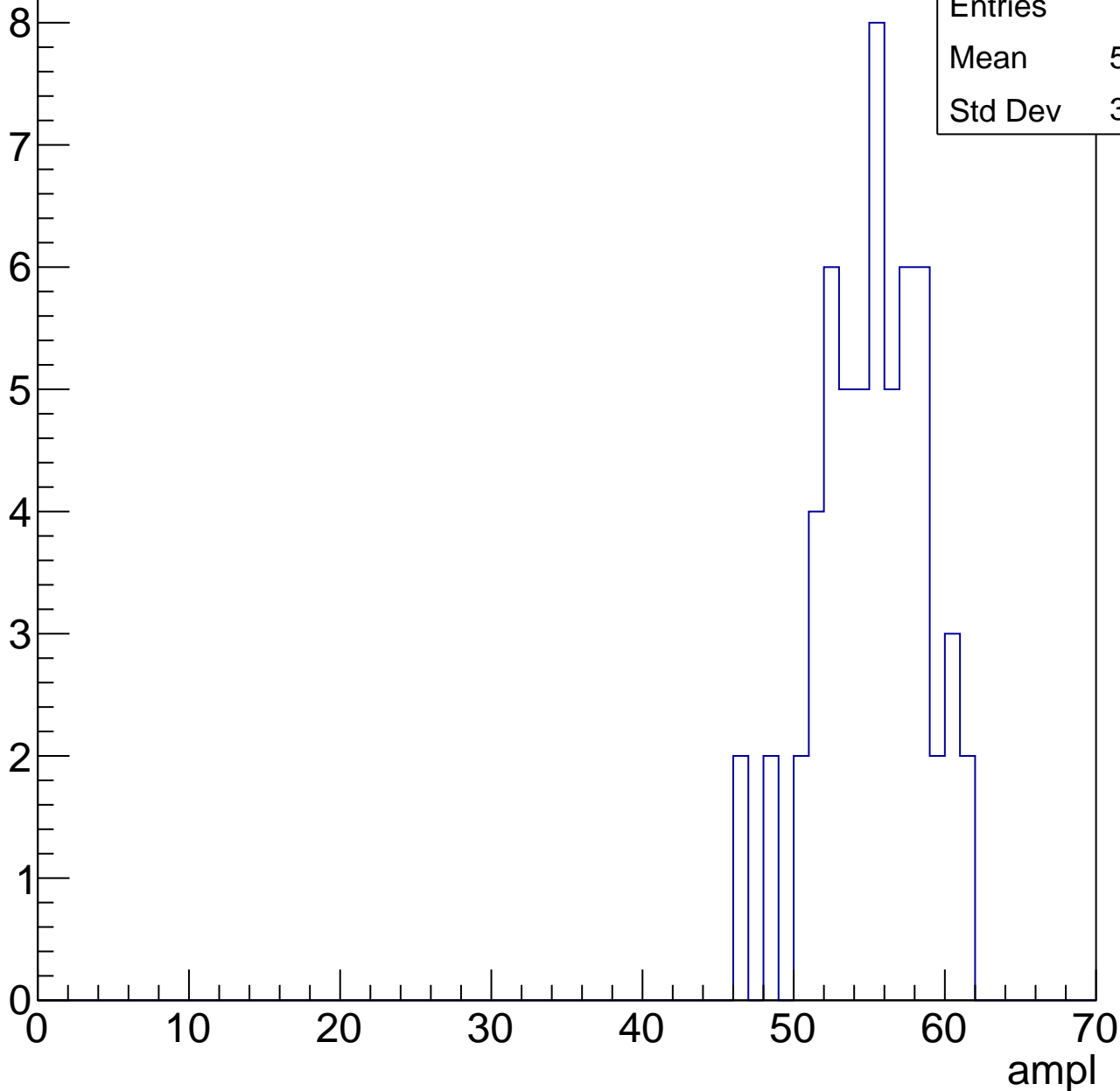


B1L103S, U23-ch46, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

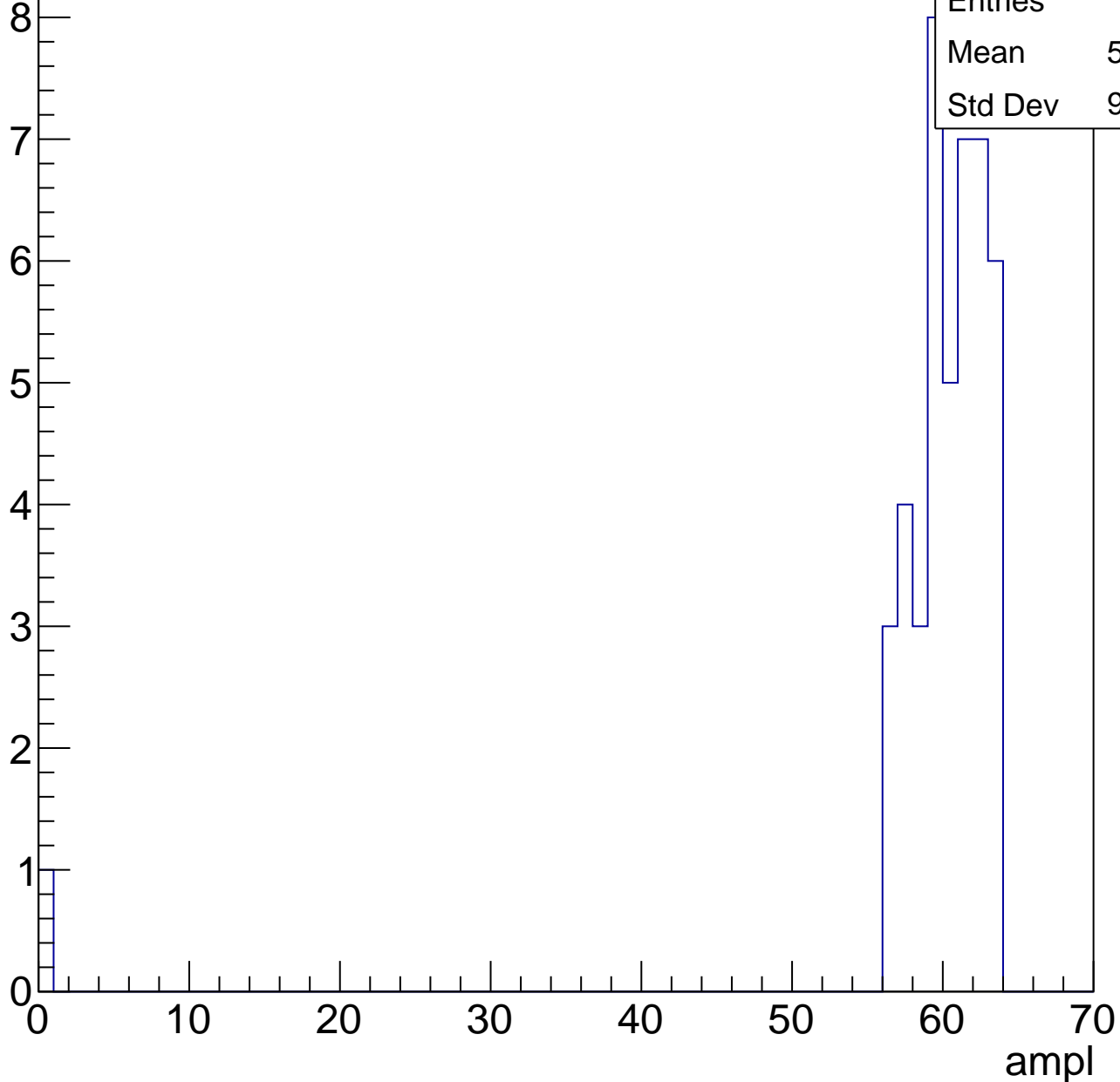
Entries	58
Mean	54.64
Std Dev	3.492



B1L103S, U23-ch46, adc5

calib_packv5_041523_1651.root, FC#0, port C2

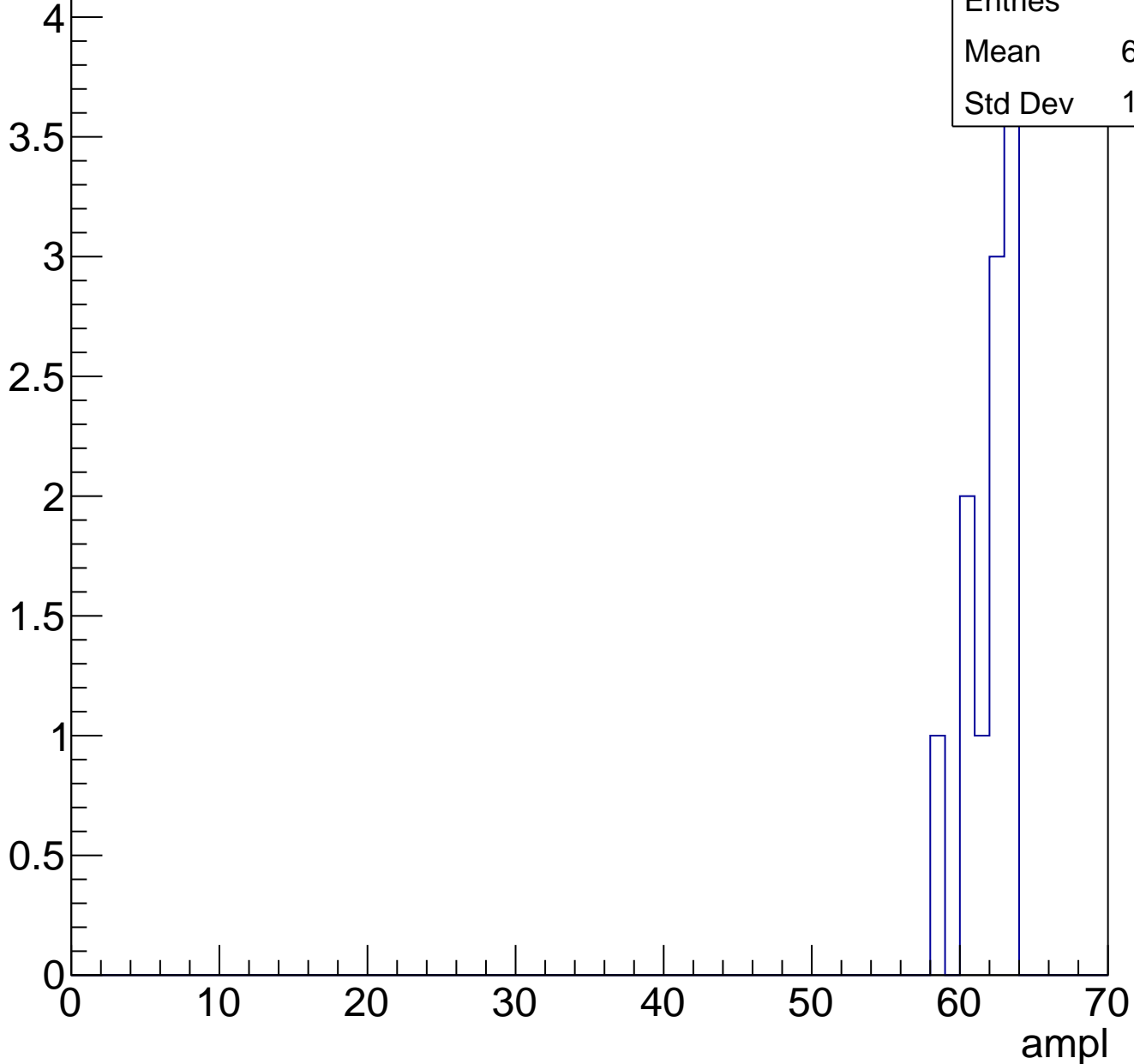
Entry



B1L103S, U23-ch46, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch46, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch47, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	81
Mean	25.44
Std Dev	10.55

Entry

10

8

6

4

2

0

ampl

0

10

20

30

40

50

60

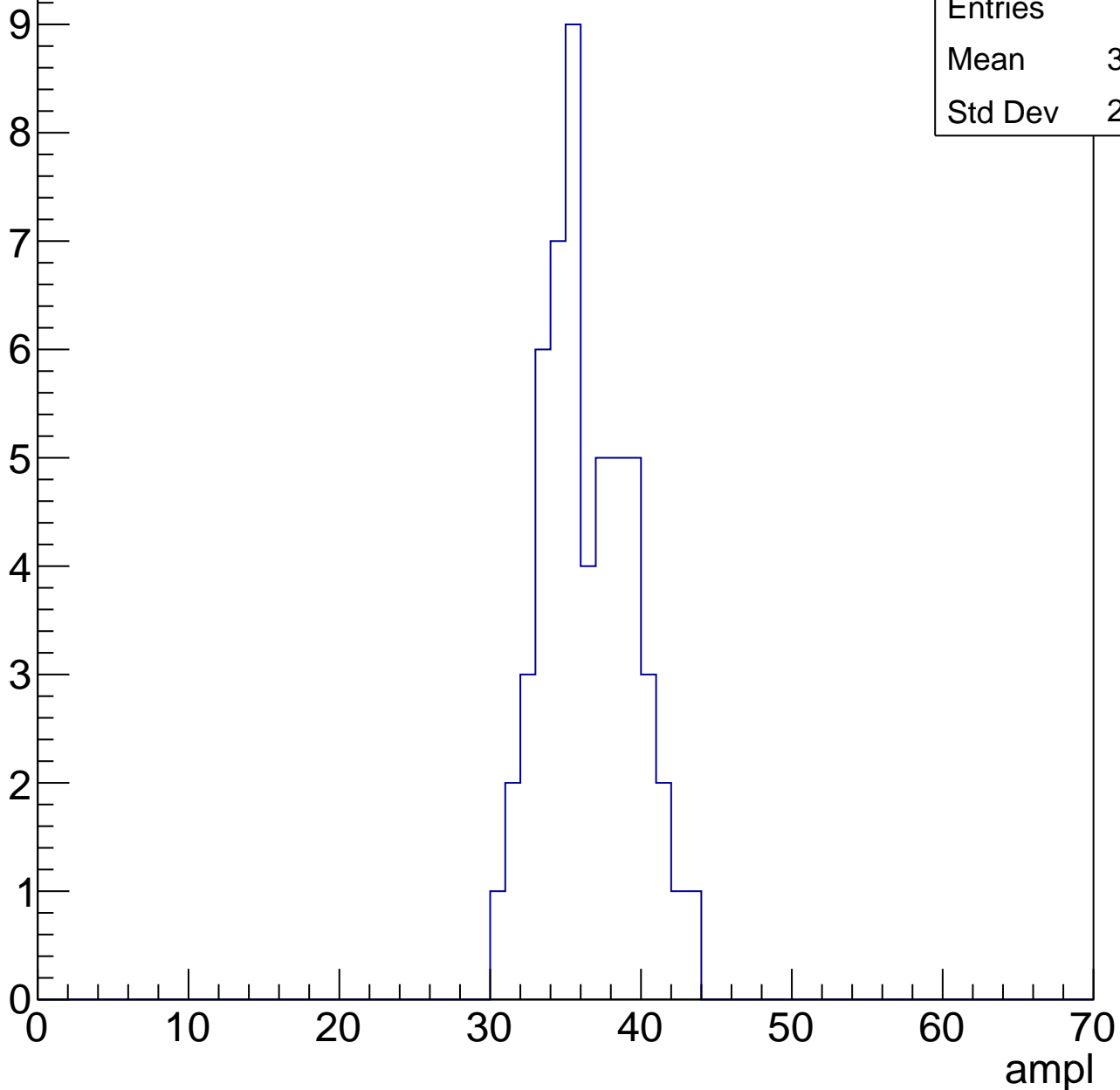
70

B1L103S, U23-ch47, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	54
Mean	35.93
Std Dev	2.974

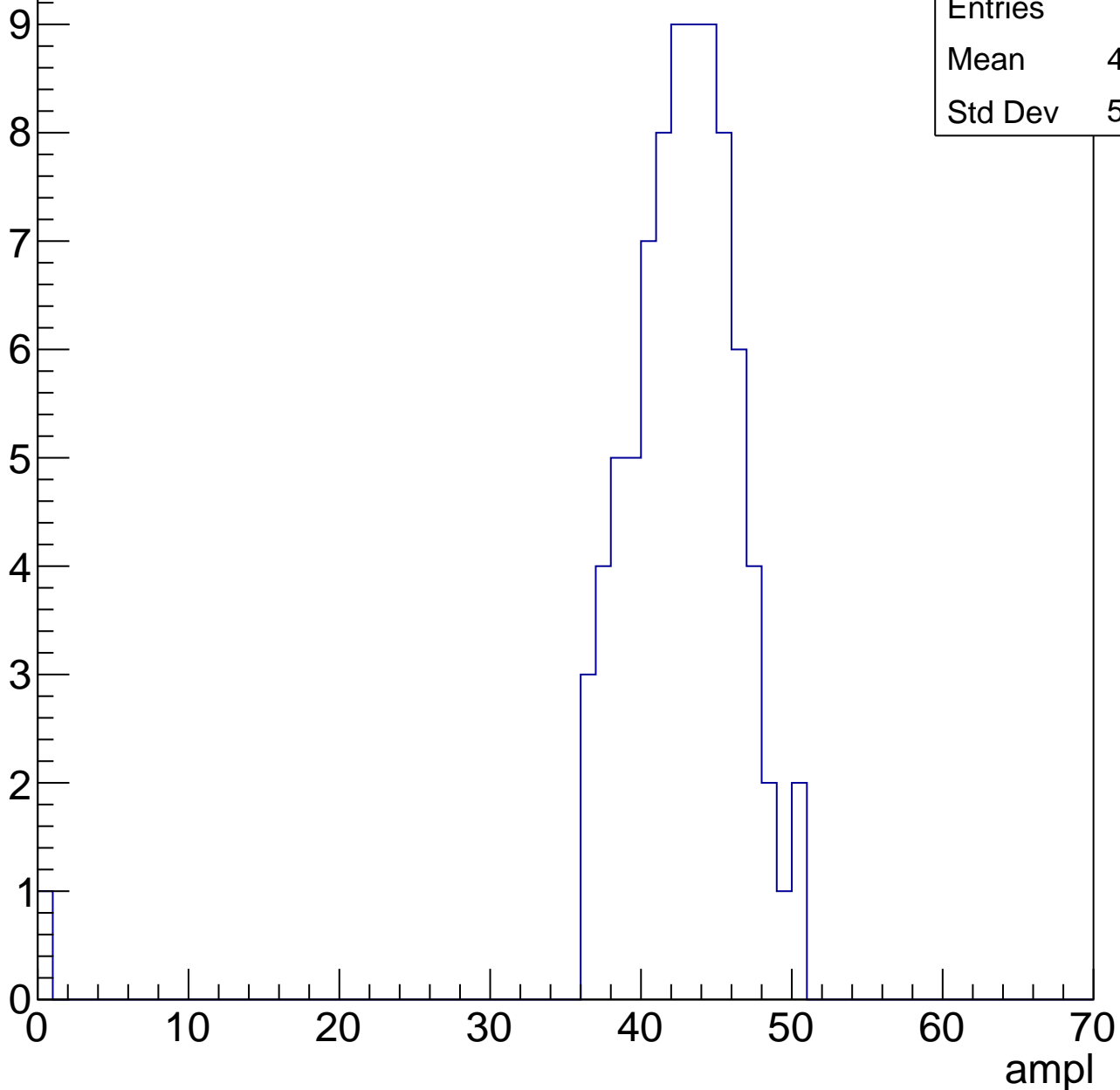


B1L103S, U23-ch47, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	83
Mean	41.92
Std Dev	5.698

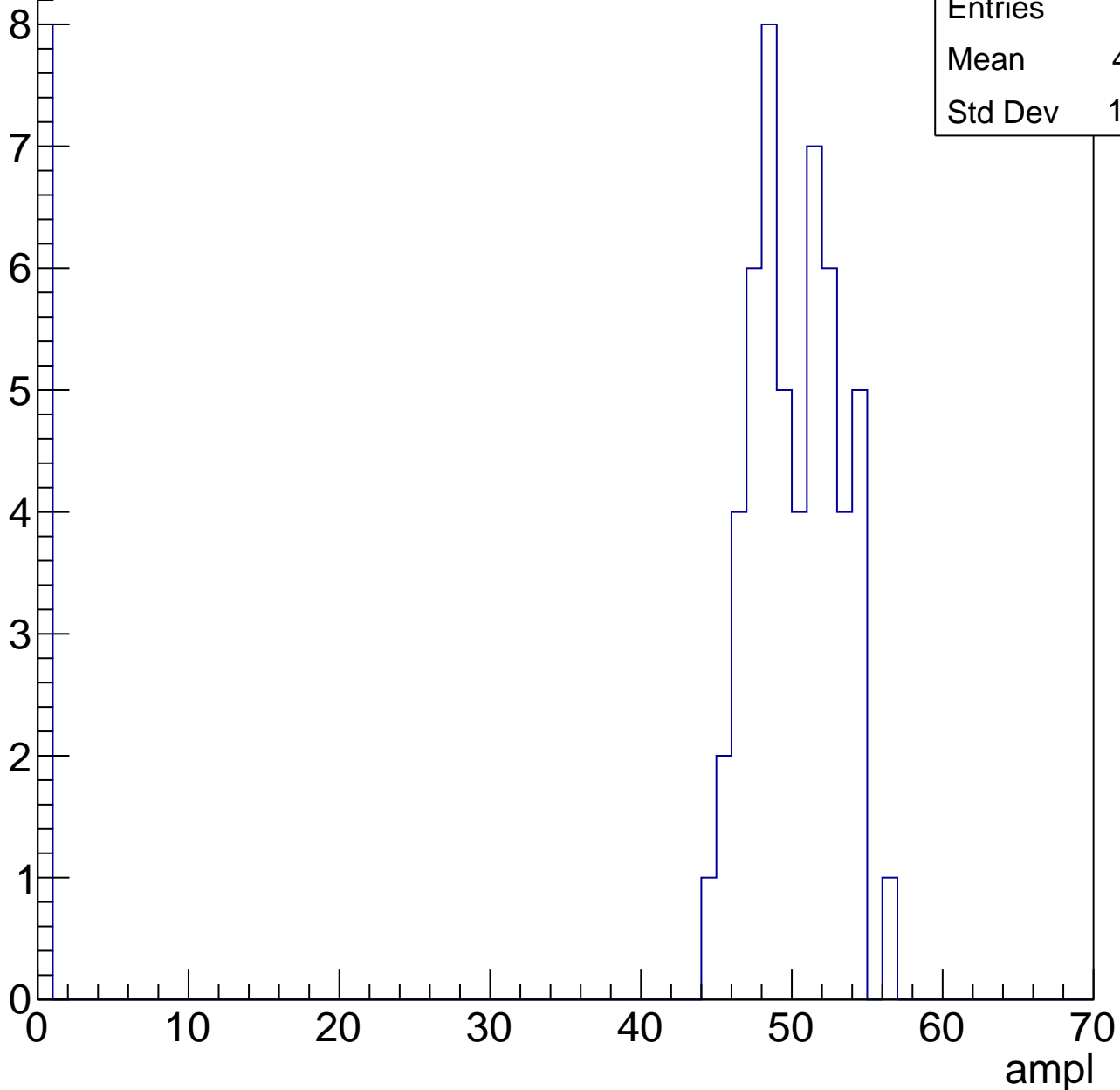


B1L103S, U23-ch47, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	43.21
Std Dev	16.99

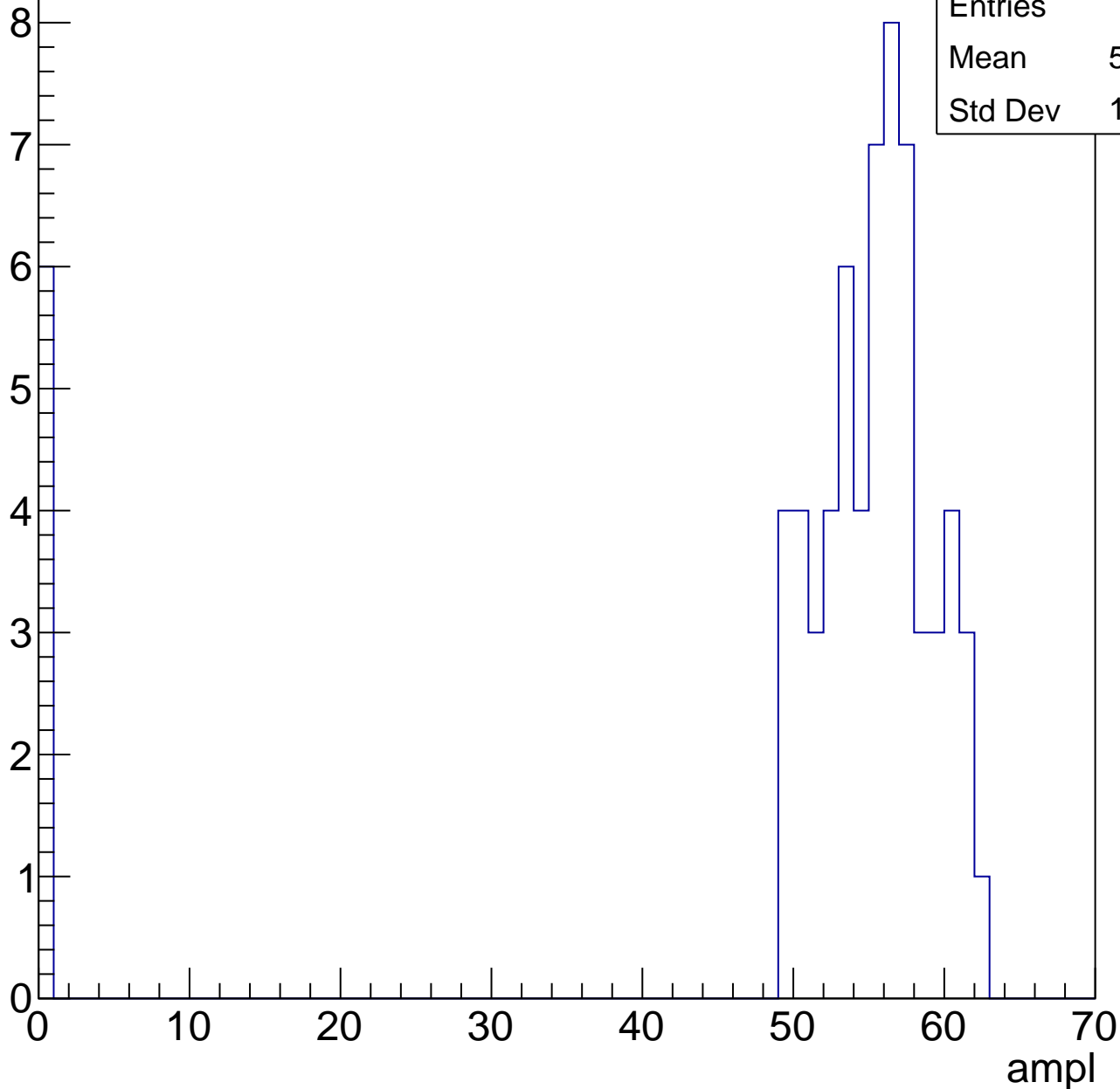


B1L103S, U23-ch47, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	50.13
Std Dev	16.06

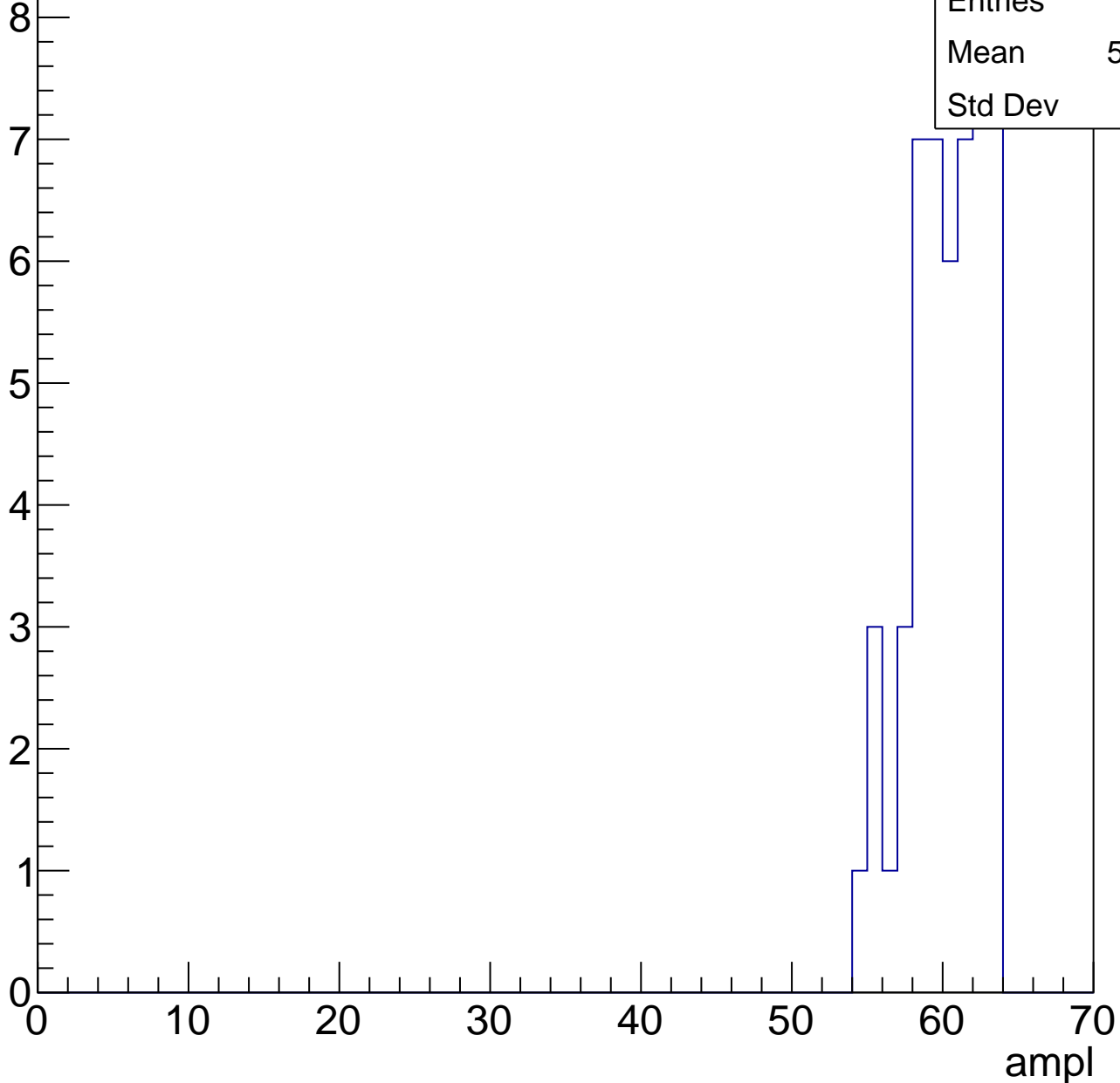


B1L103S, U23-ch47, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	51
Mean	59.84
Std Dev	2.42



B1L103S, U23-ch47, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch47, adc7

calib_packv5_041523_1651.root, FC#0, port C2

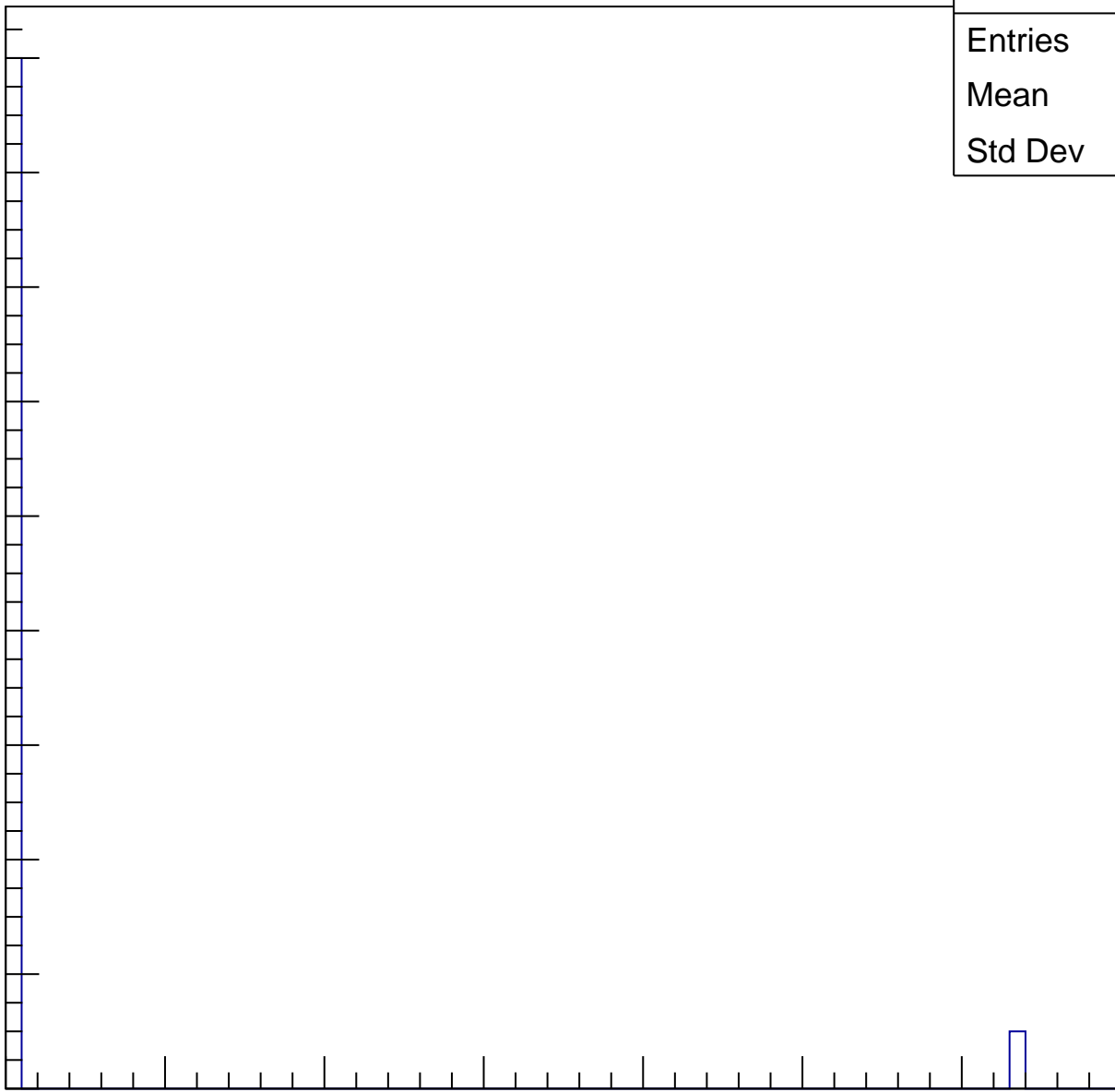
Entries	19
Mean	3.316
Std Dev	14.07

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

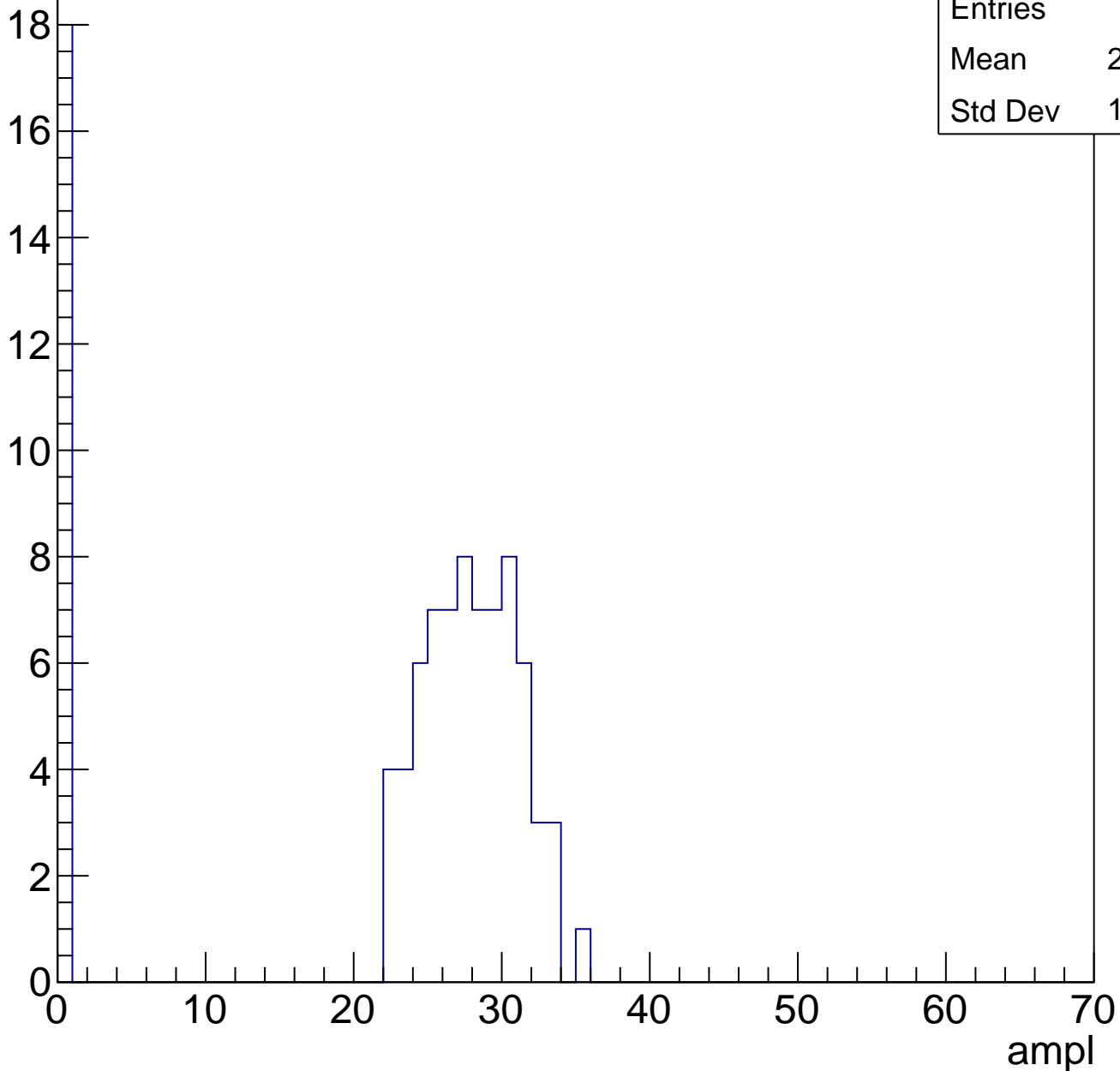


B1L103S, U23-ch48, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	89
Mean	21.93
Std Dev	11.39

Entry

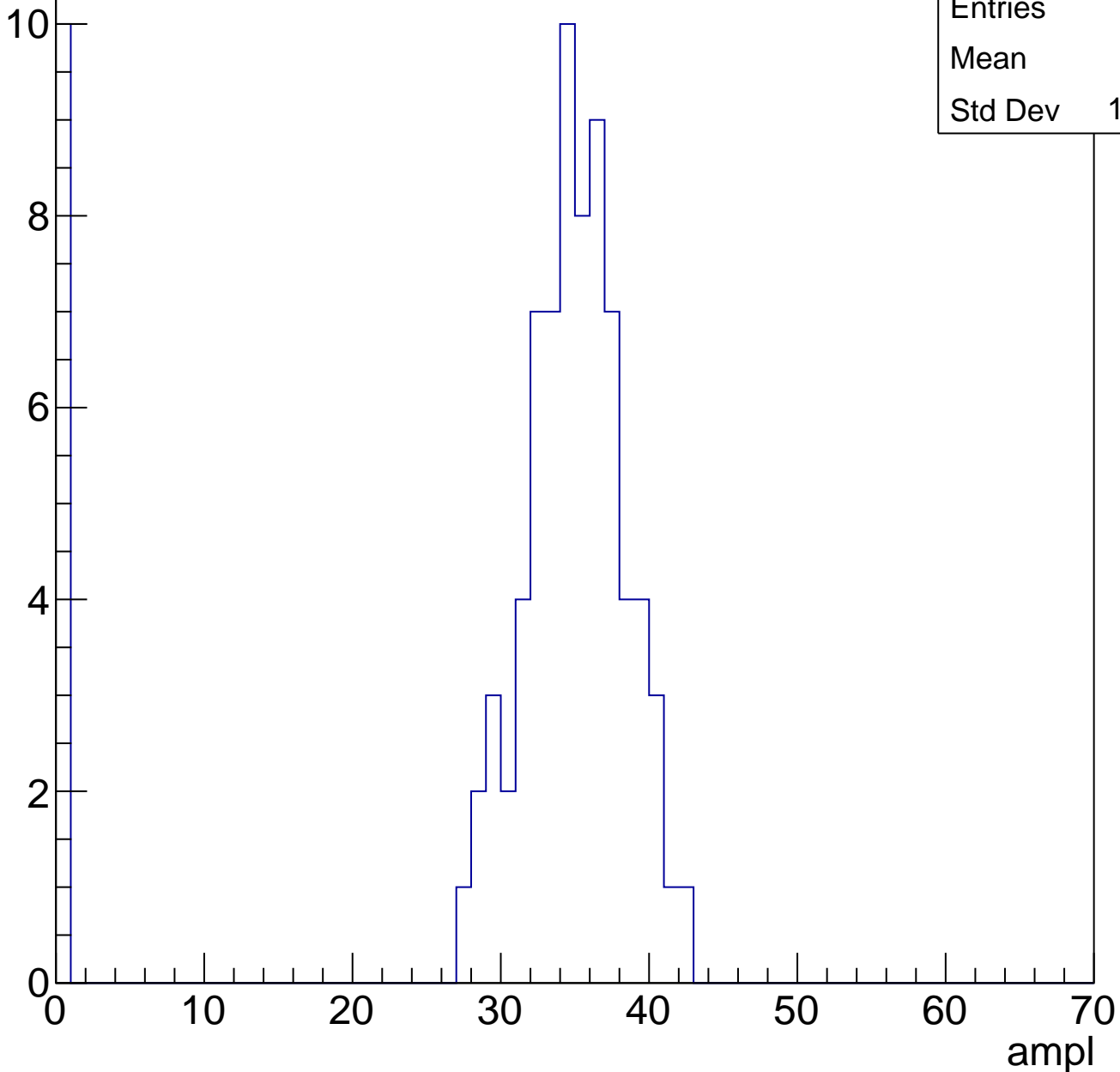


B1L103S, U23-ch48, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	83
Mean	30.4
Std Dev	11.65

Entry

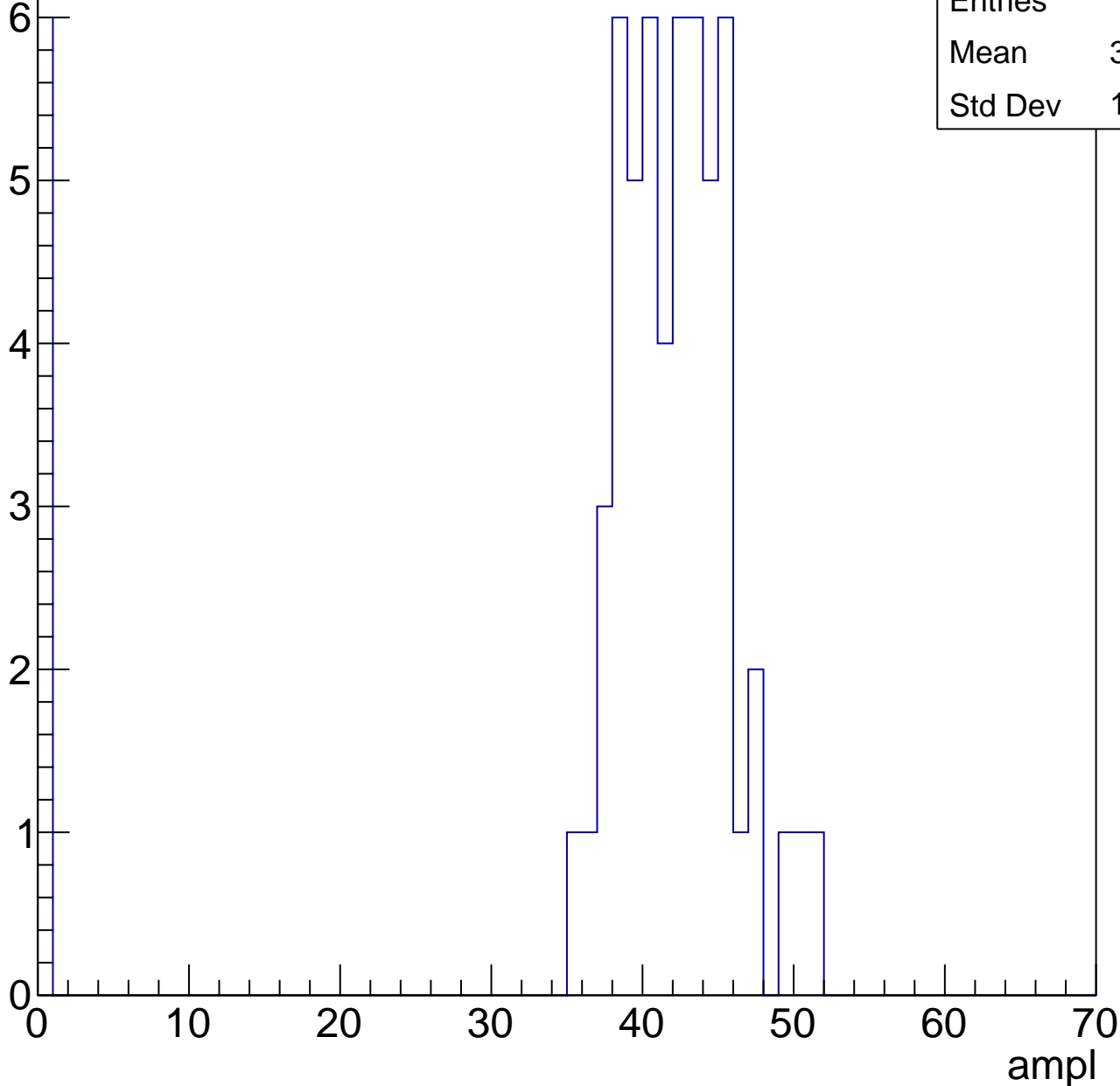


B1L103S, U23-ch48, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	37.69
Std Dev	12.88

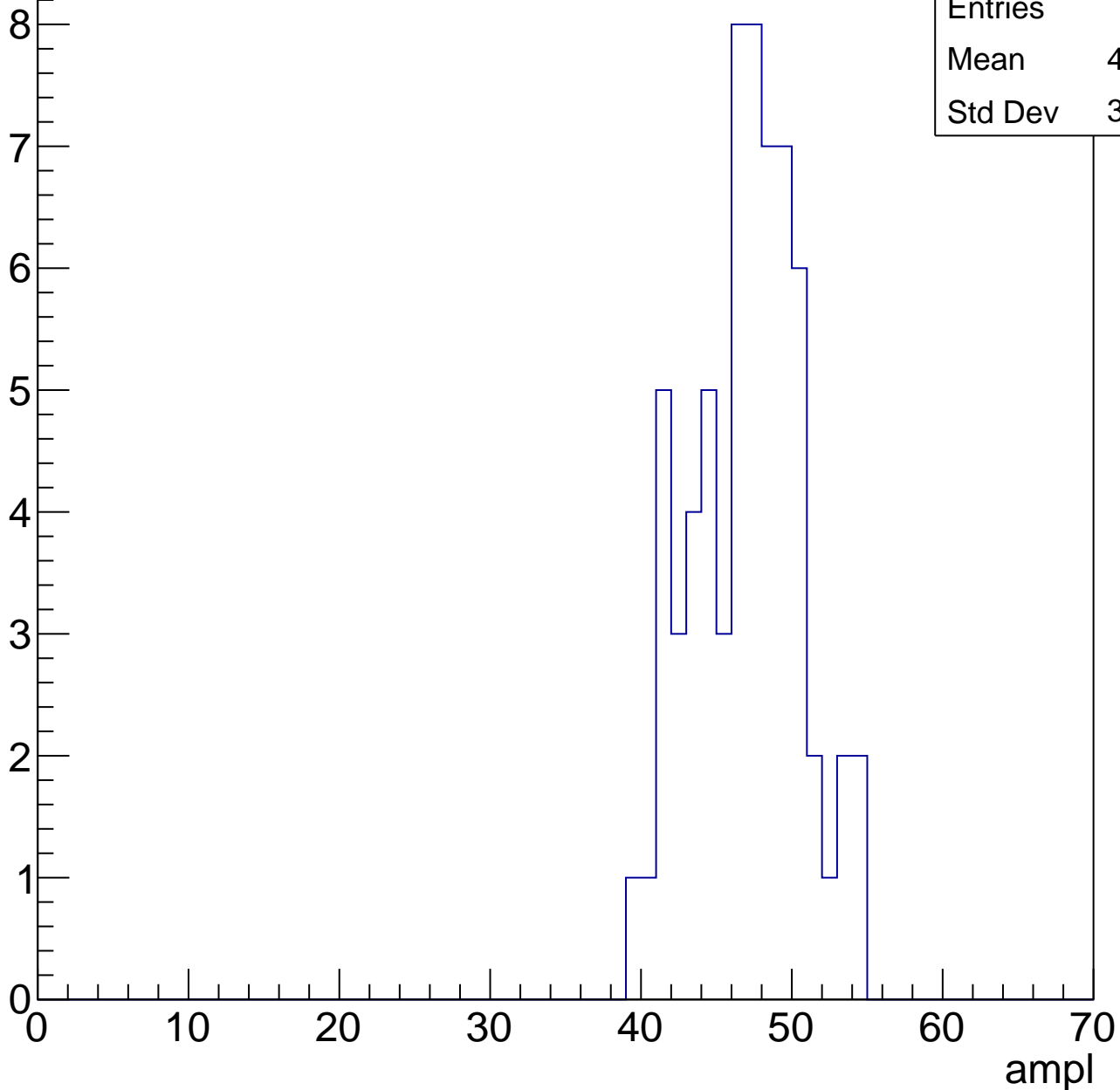


B1L103S, U23-ch48, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	46.58
Std Dev	3.512

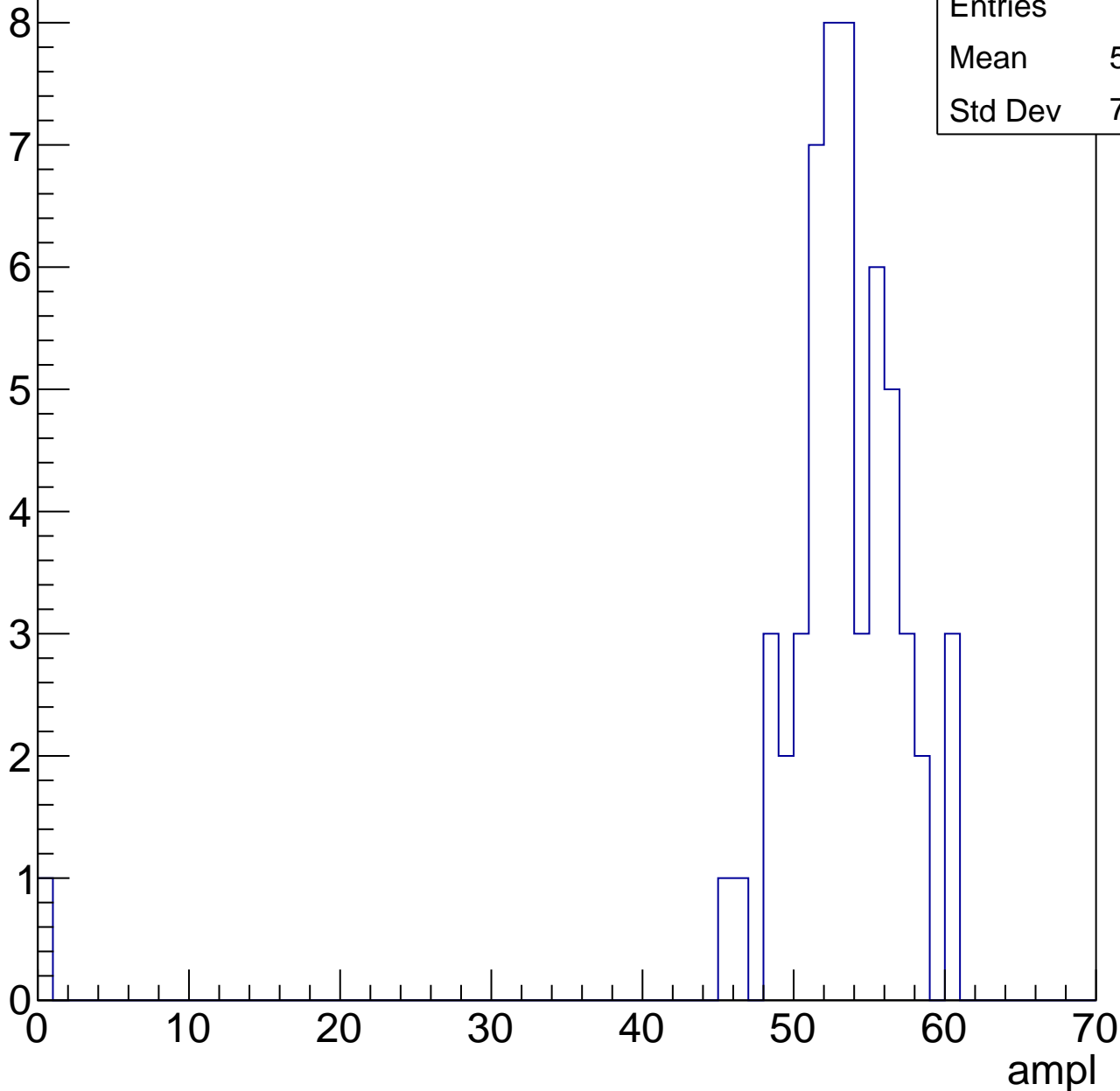


B1L103S, U23-ch48, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	56
Mean	52.12
Std Dev	7.753

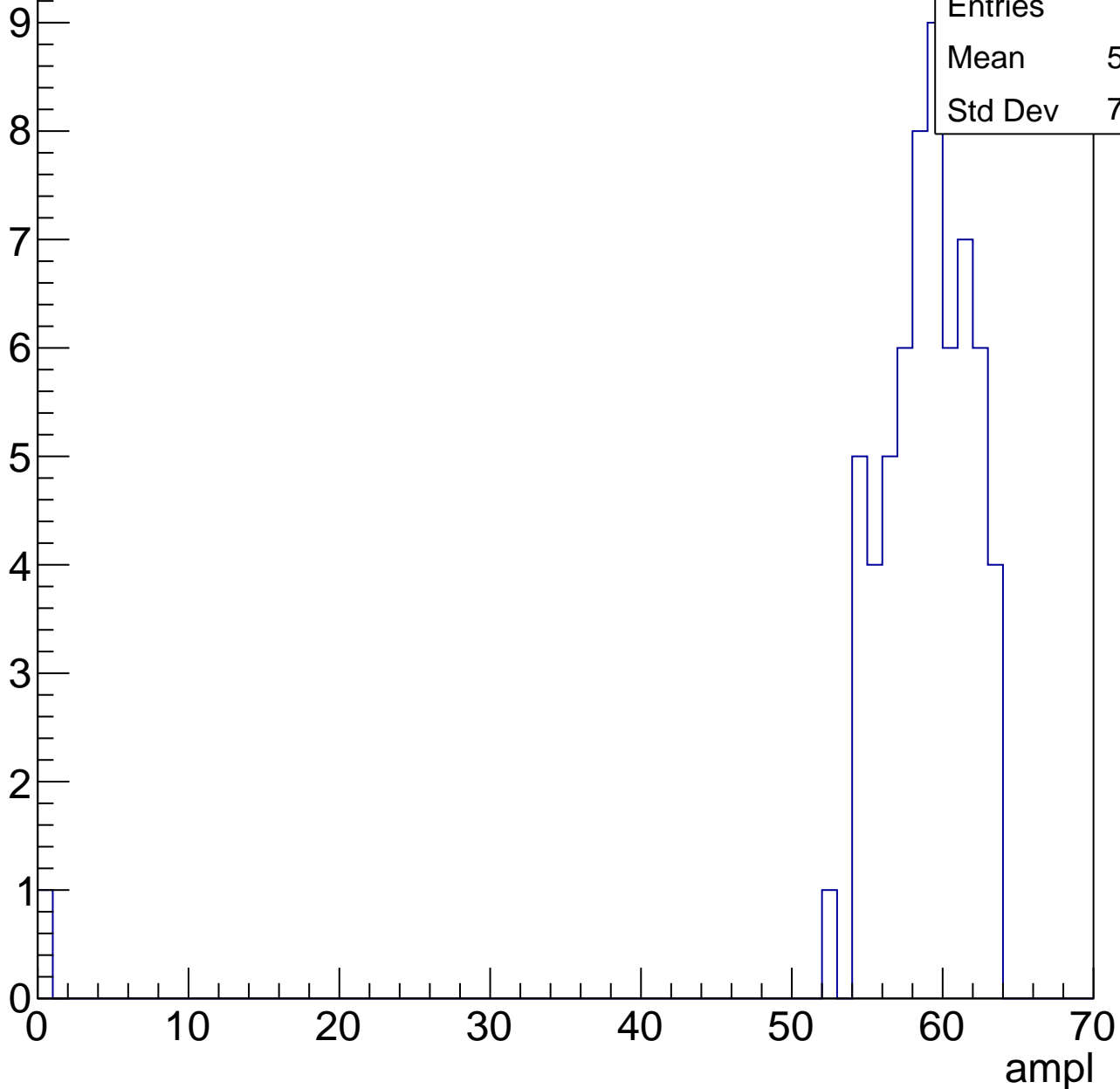


B1L103S, U23-ch48, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	57.58
Std Dev	7.853

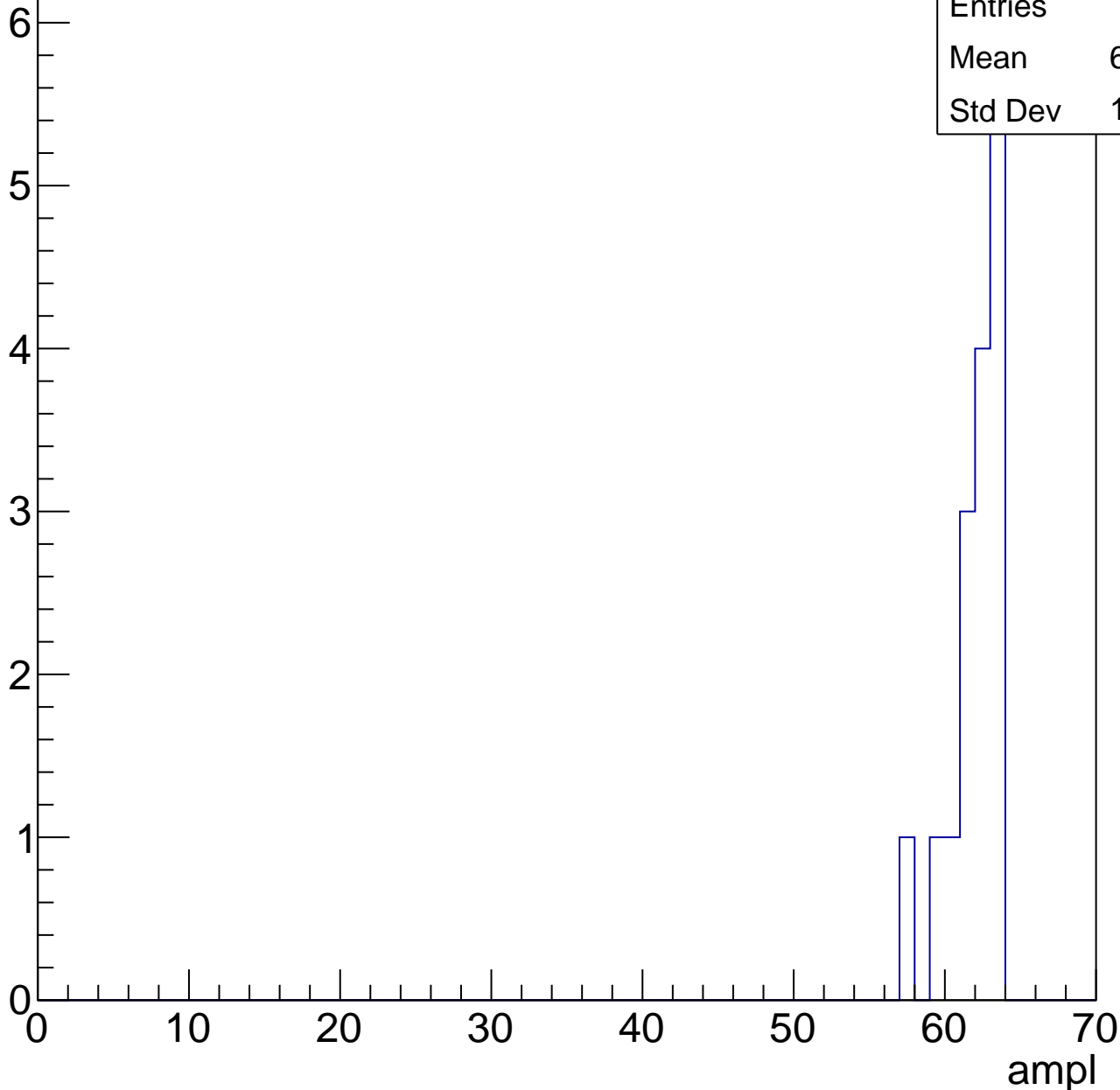


B1L103S, U23-ch48, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	16
Mean	61.56
Std Dev	1.657

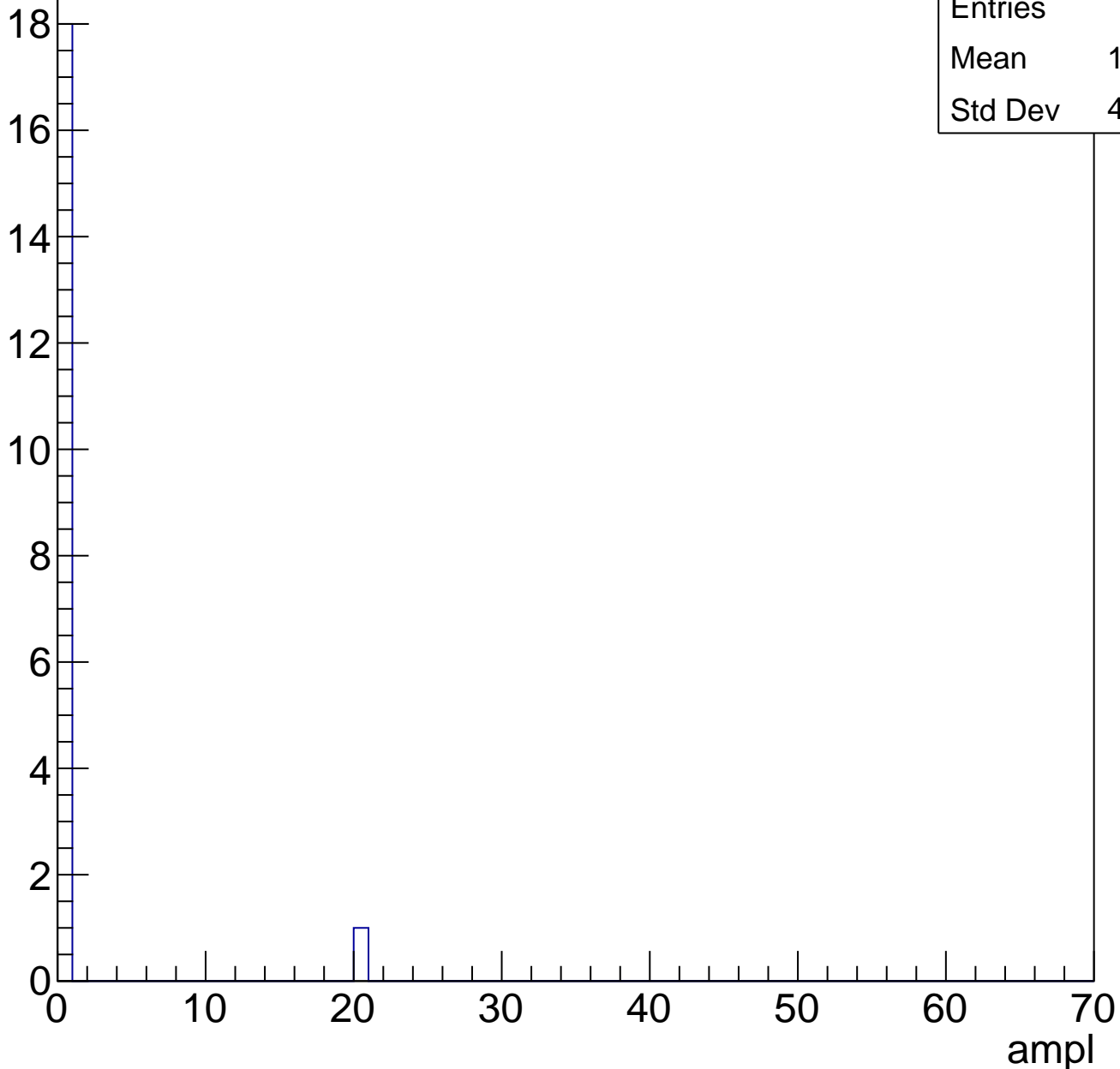


B1L103S, U23-ch48, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.053
Std Dev	4.466

Entry



B1L103S, U23-ch49, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	88
Mean	25.43
Std Dev	10.08

Entry

10

8

6

4

2

0

0

10

20

30

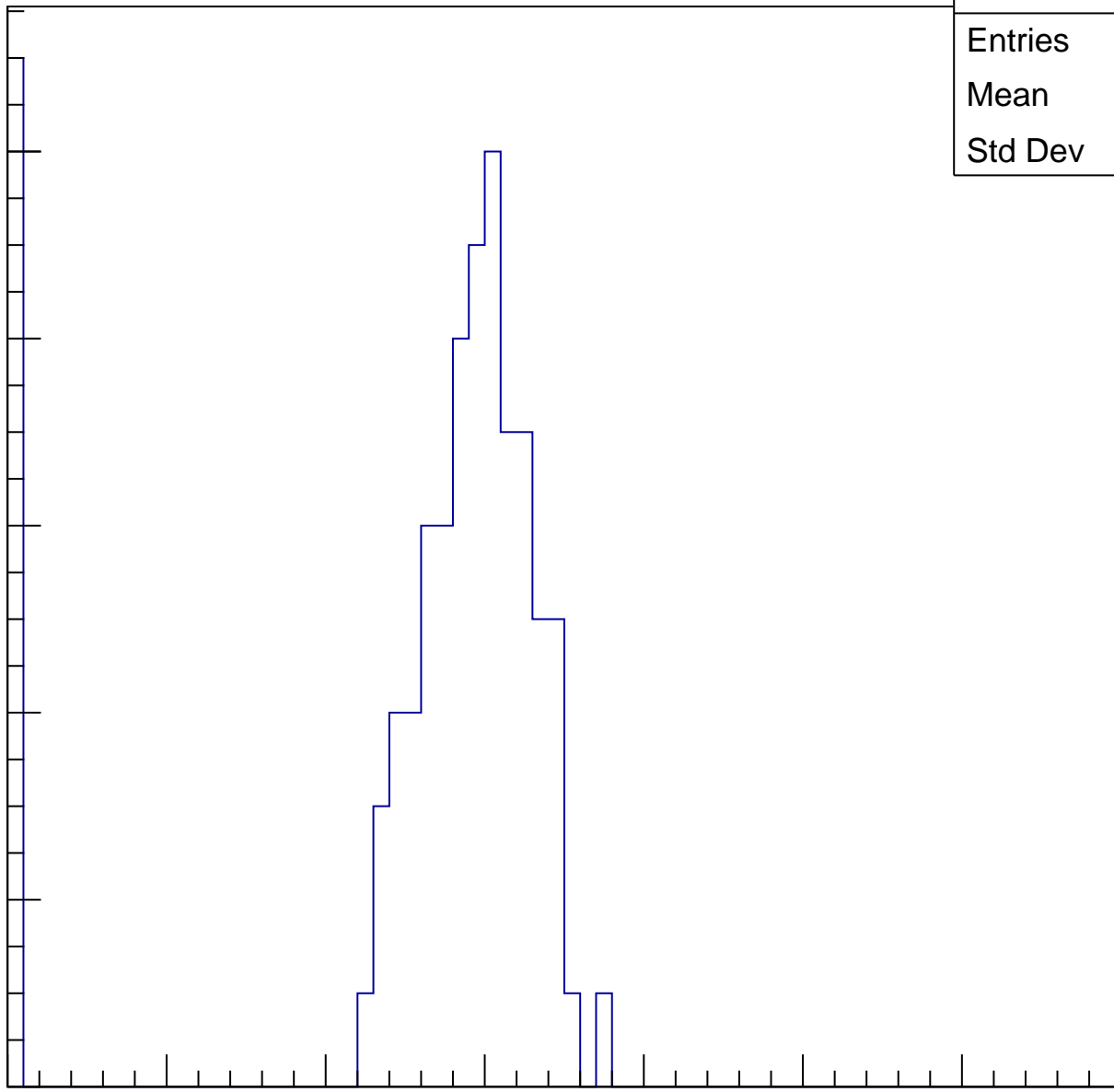
40

50

60

70

ampl

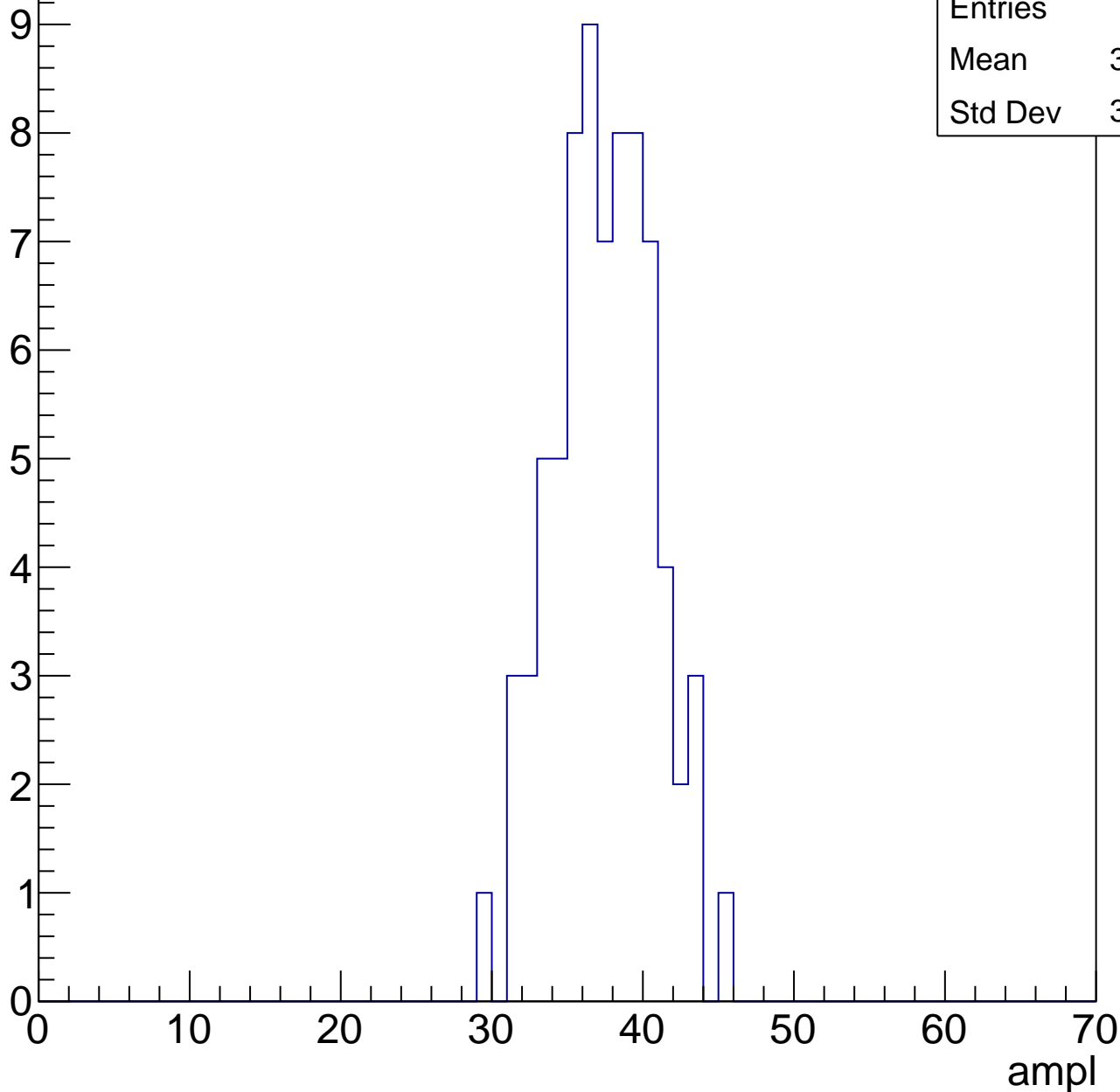


B1L103S, U23-ch49, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	74
Mean	36.95
Std Dev	3.292

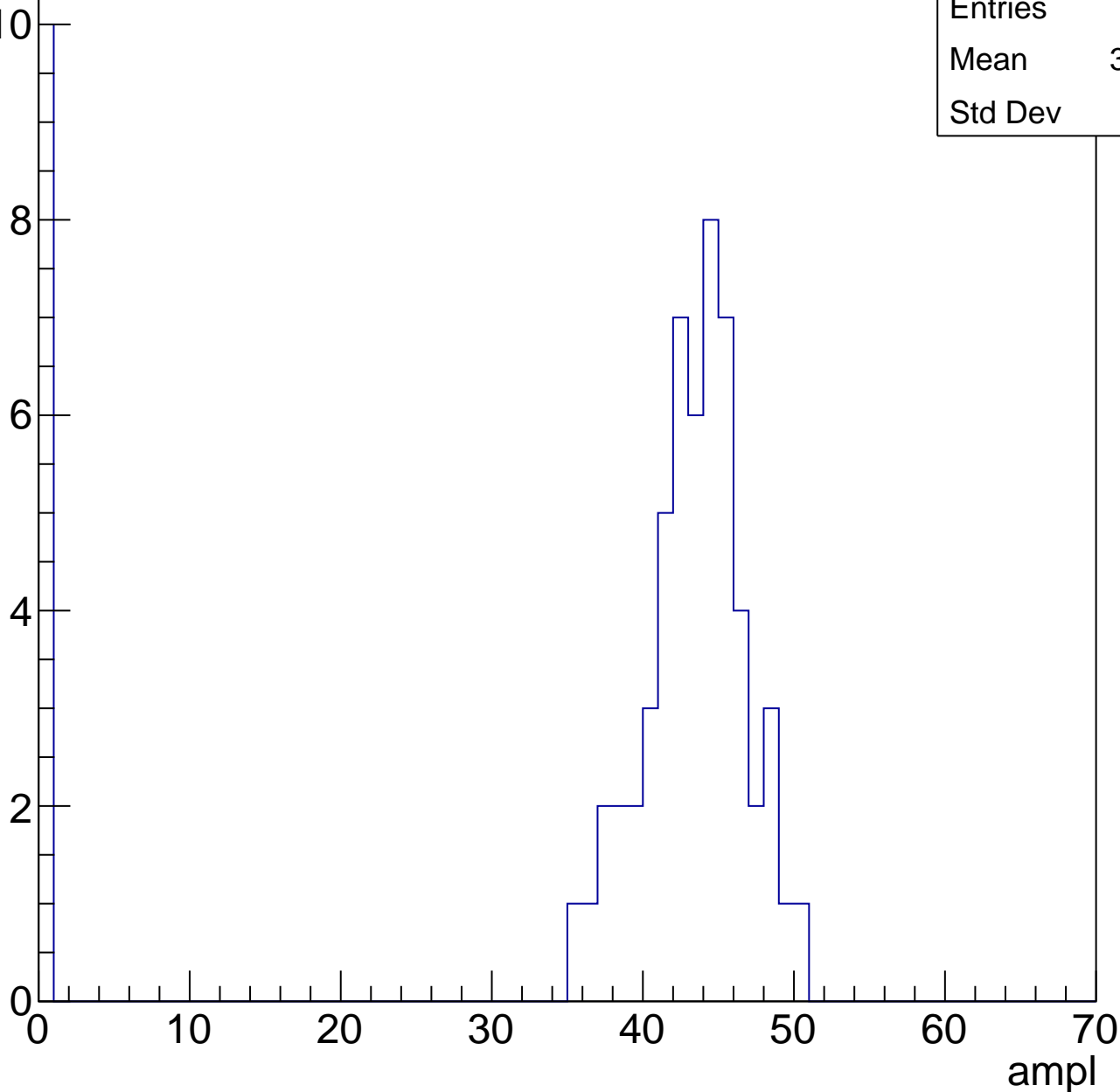


B1L103S, U23-ch49, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	36.37
Std Dev	15.8

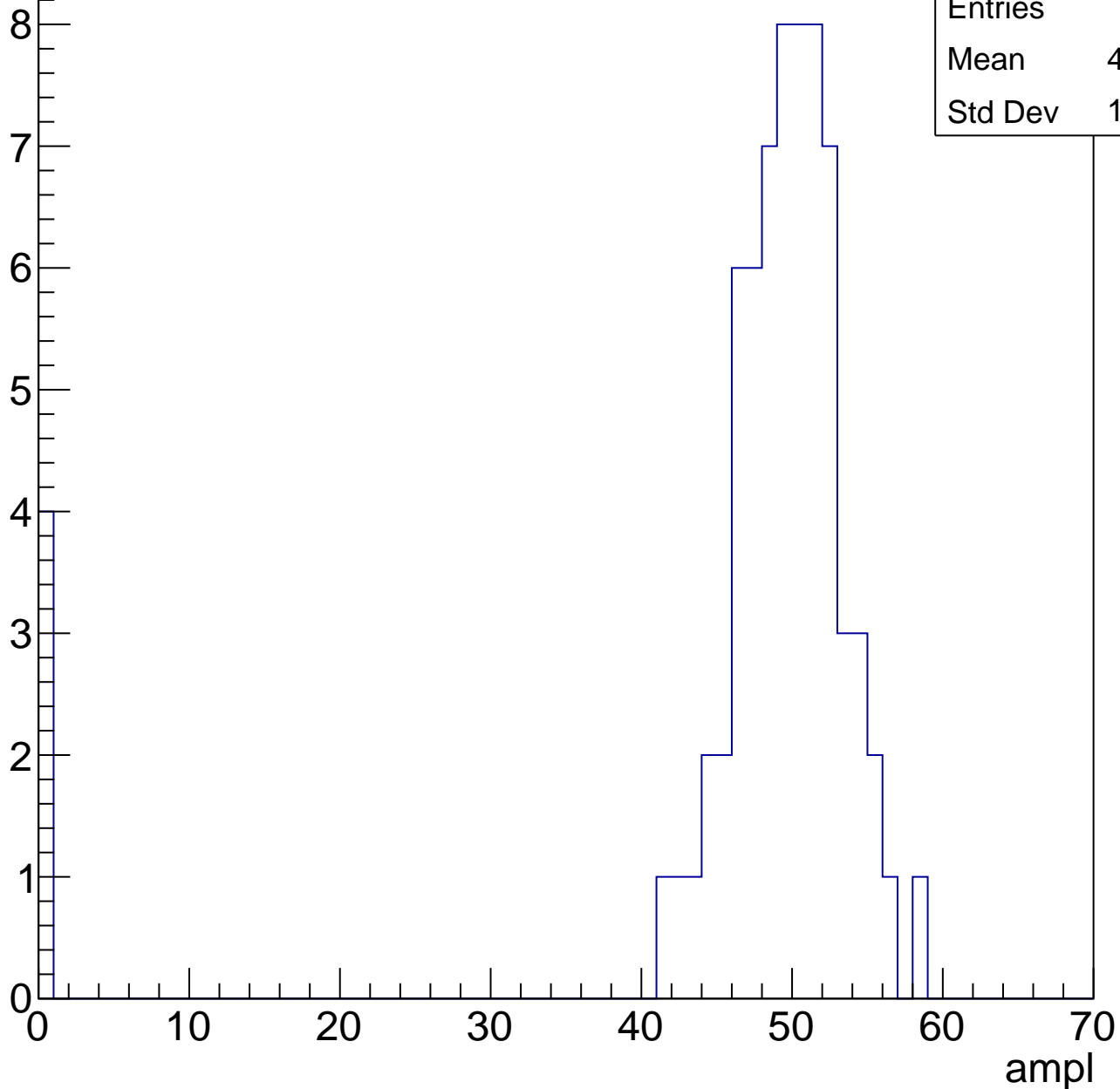


B1L103S, U23-ch49, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	46.58
Std Dev	11.83

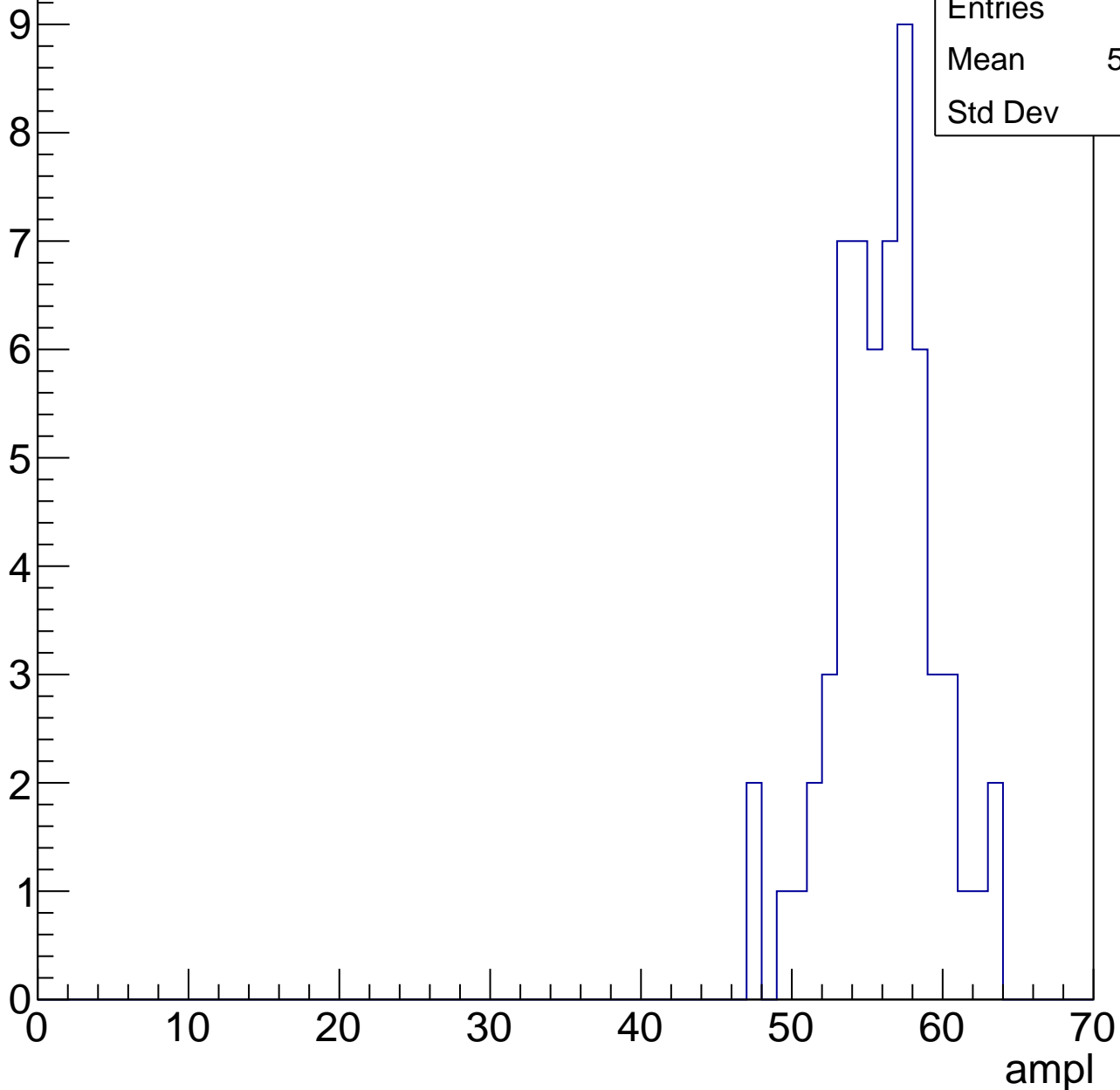


B1L103S, U23-ch49, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	55.56
Std Dev	3.38

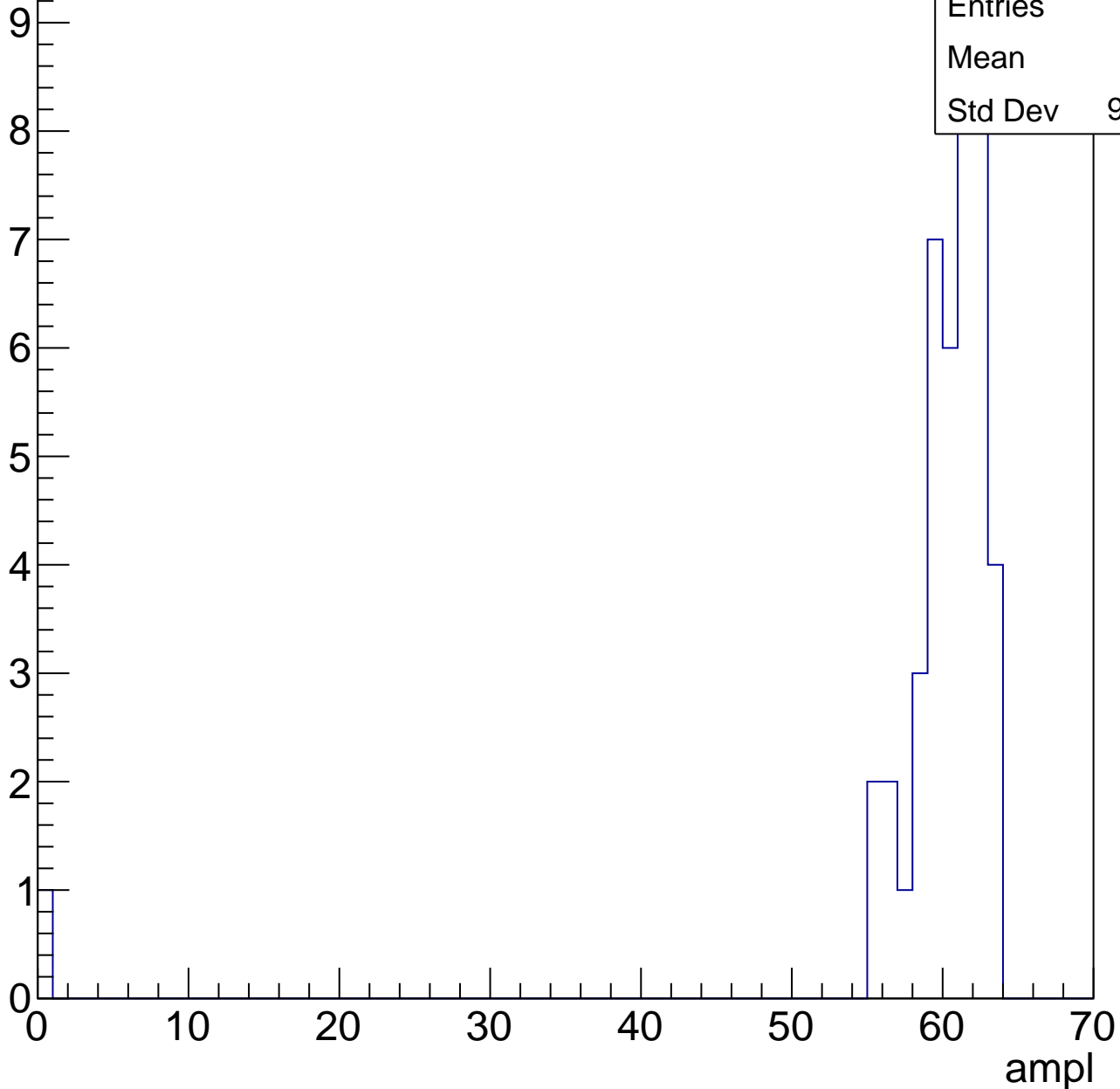


B1L103S, U23-ch49, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

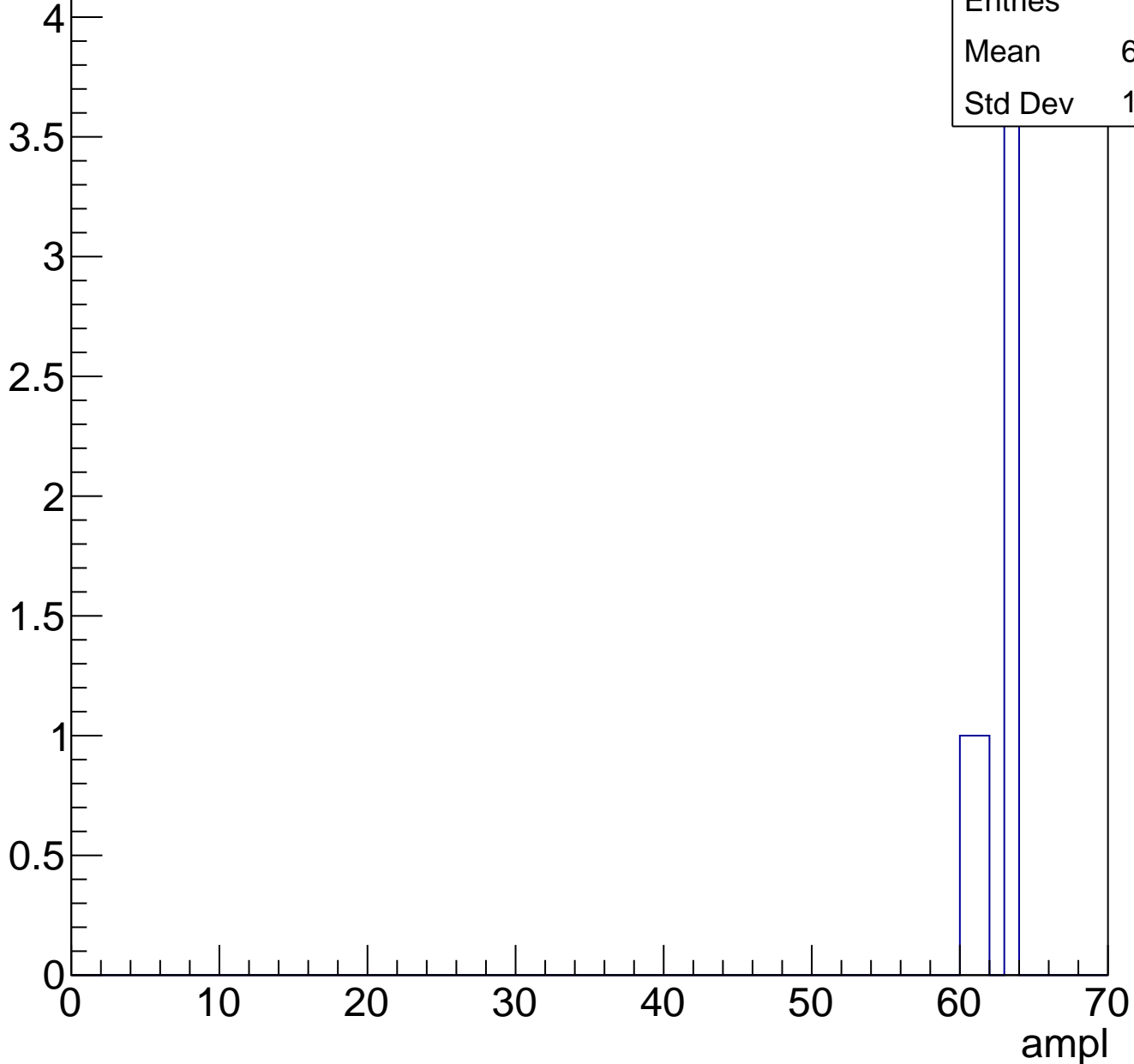
Entries	43
Mean	58.7
Std Dev	9.297



B1L103S, U23-ch49, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch49, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch50, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	87
Mean	23.11
Std Dev	10.22

Entry

12

10

8

6

4

2

0

0

10

20

30

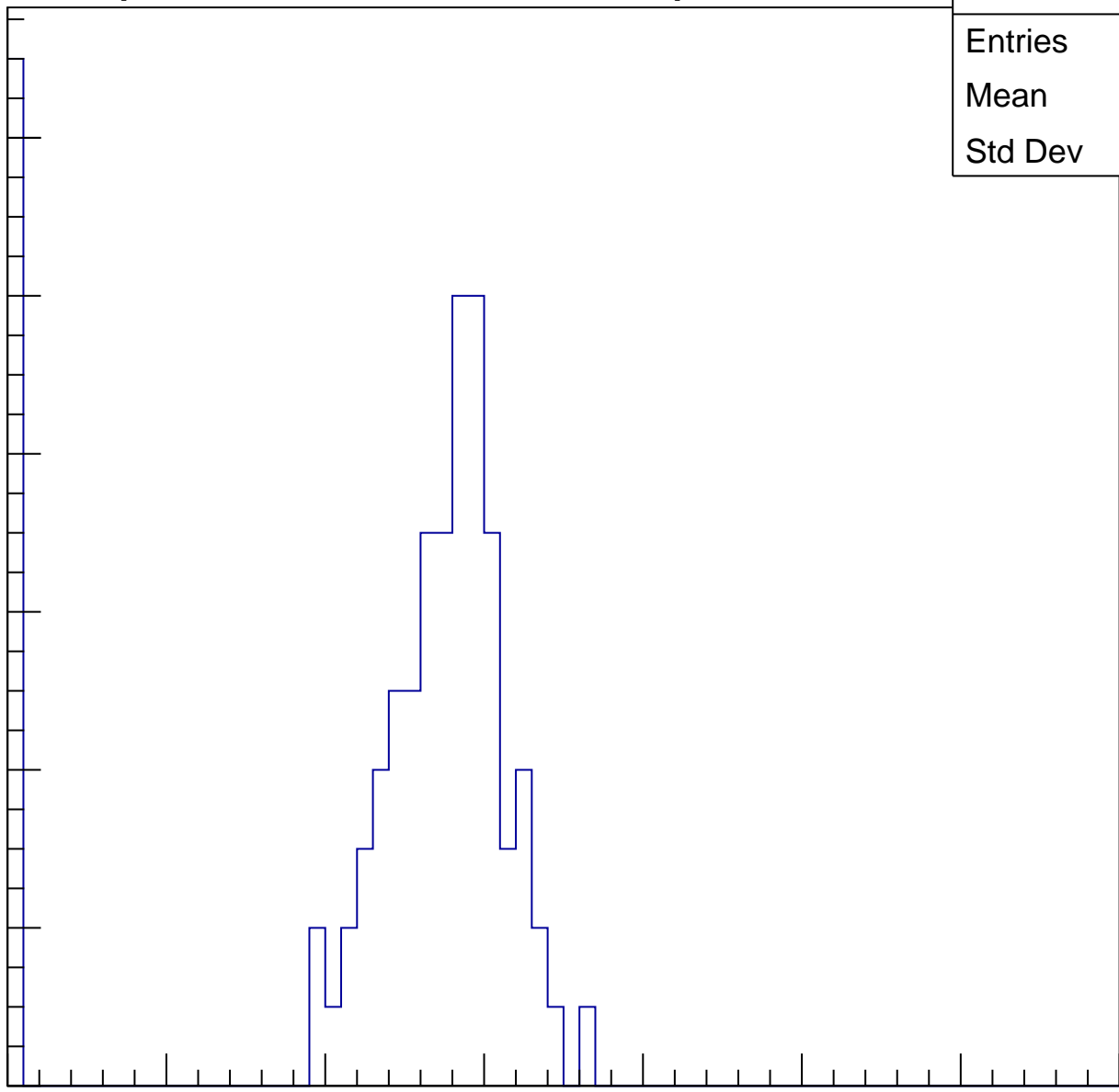
40

50

60

70

ampl



B1L103S, U23-ch50, adc1

calib_packv5_041523_1651.root, FC#0, port C2

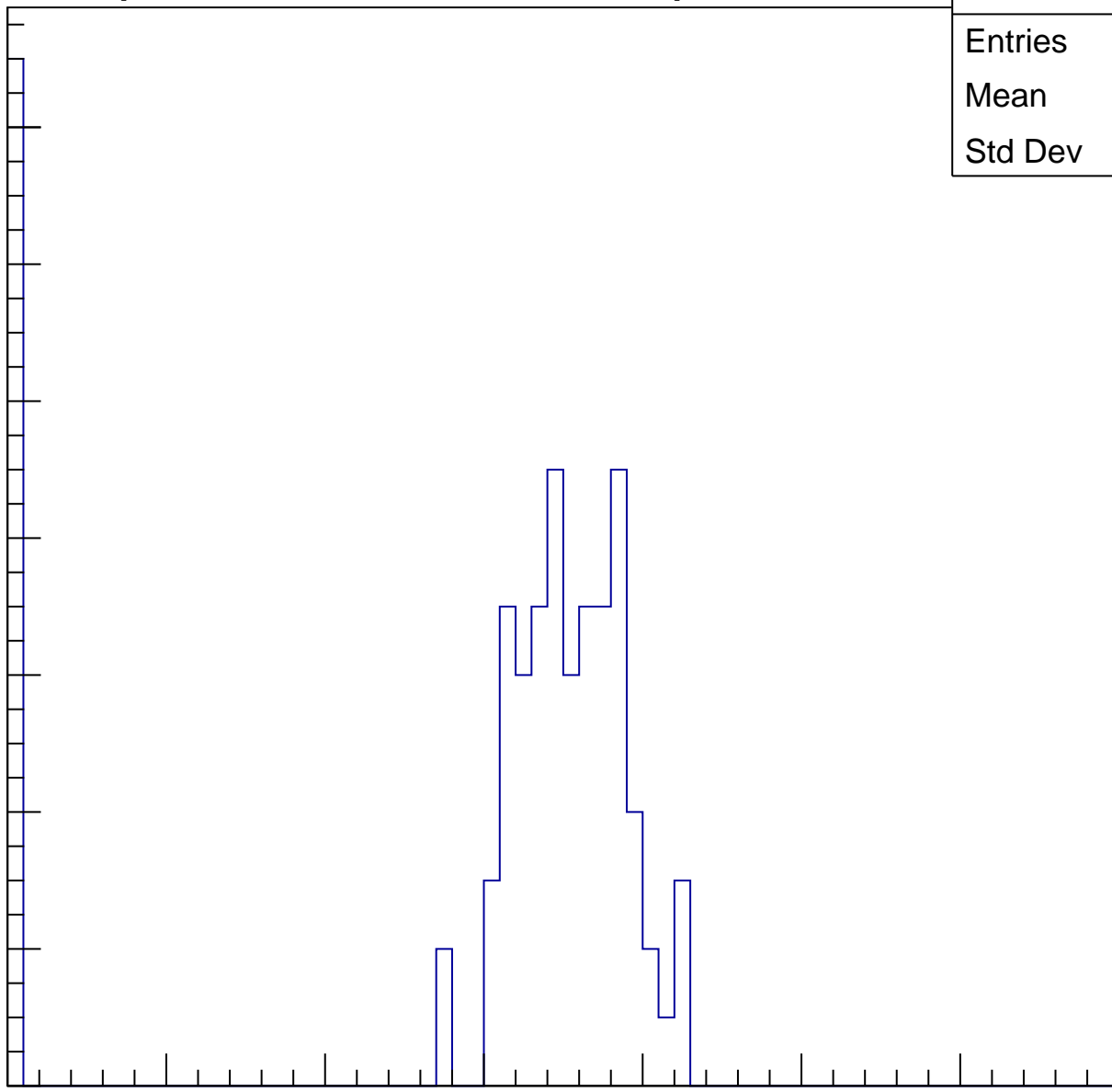
Entries	88
Mean	29.05
Std Dev	13.52

Entry

14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

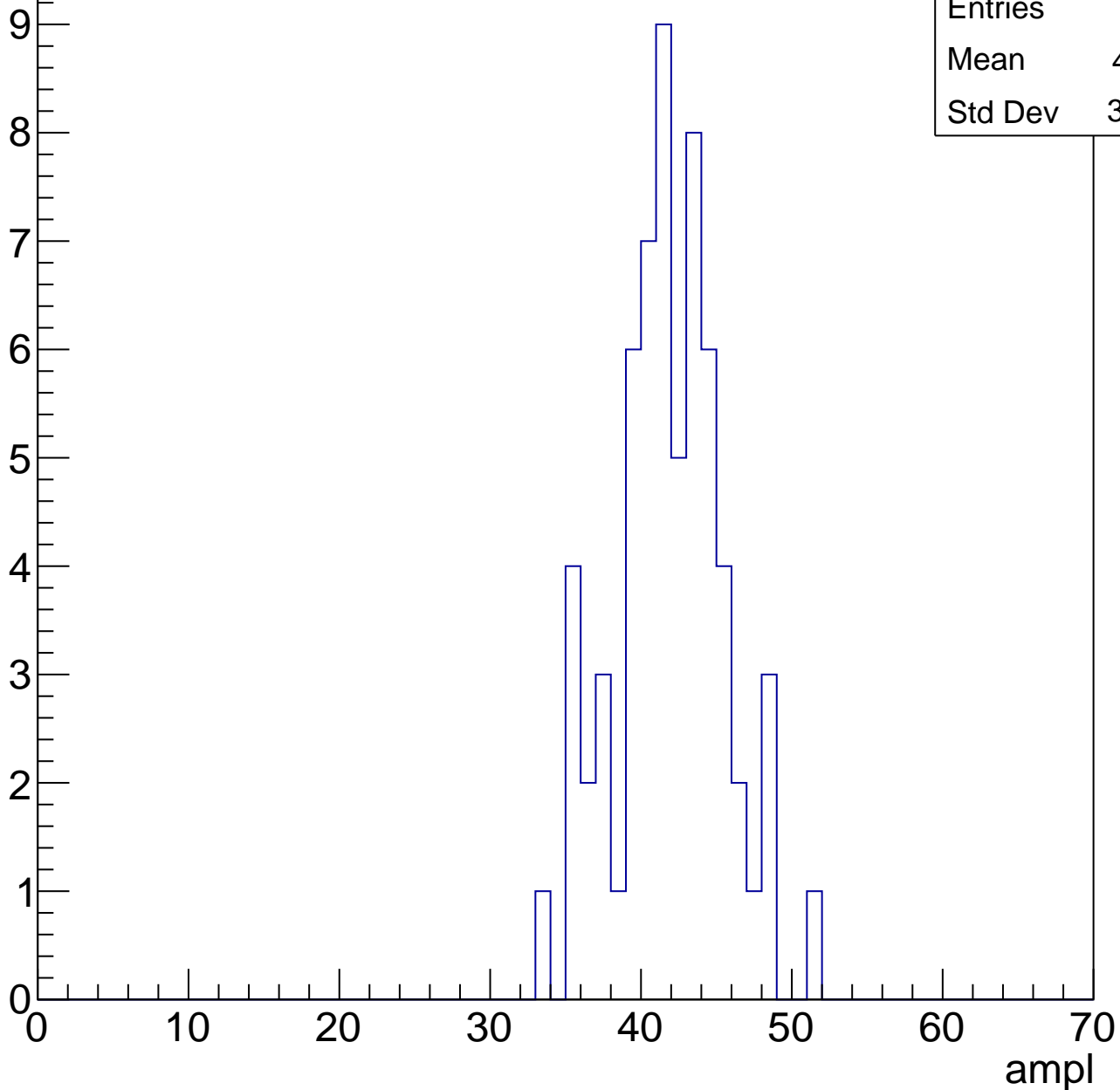


B1L103S, U23-ch50, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	63
Mean	41.41
Std Dev	3.615

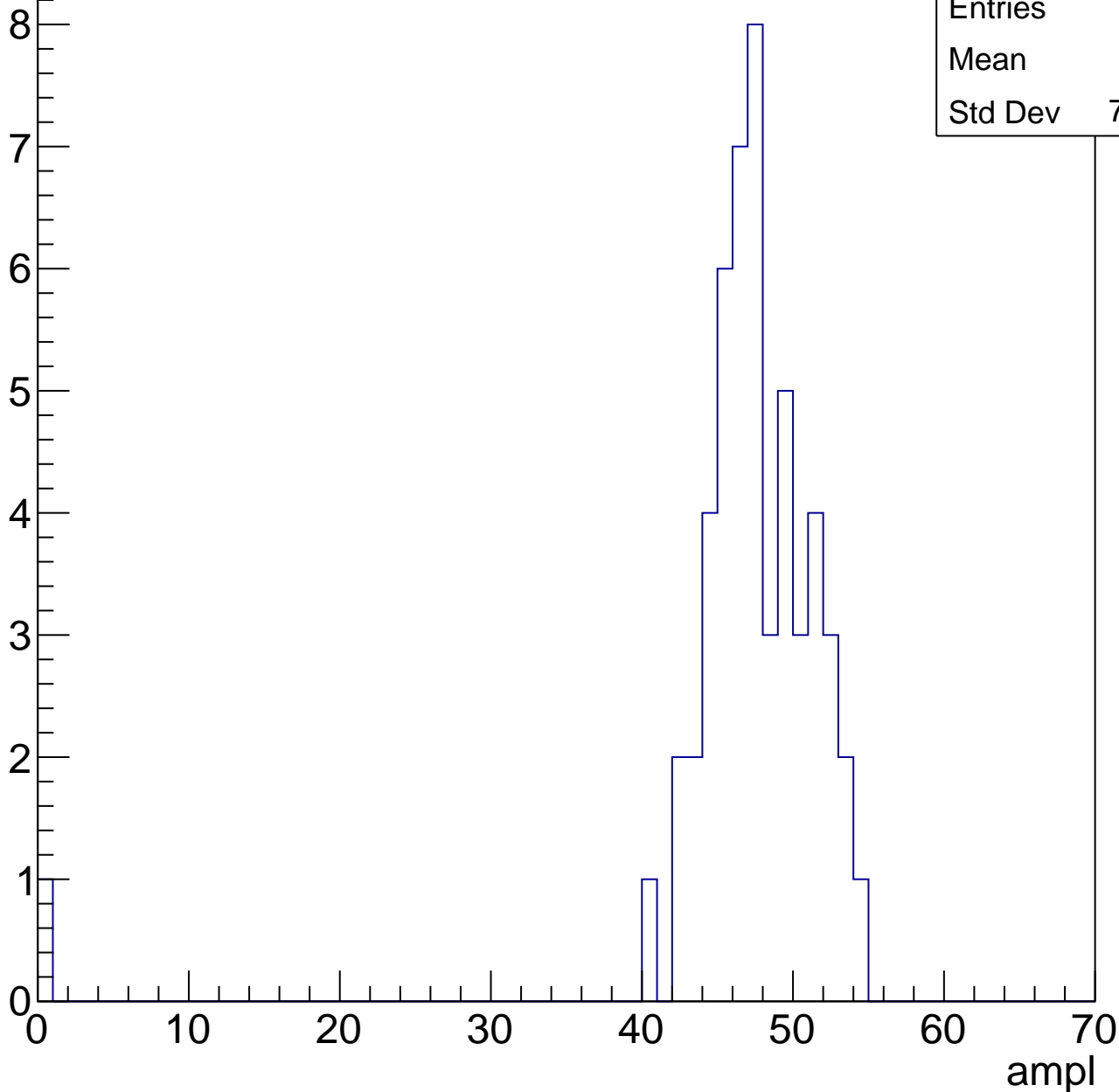


B1L103S, U23-ch50, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	52
Mean	46.4
Std Dev	7.204

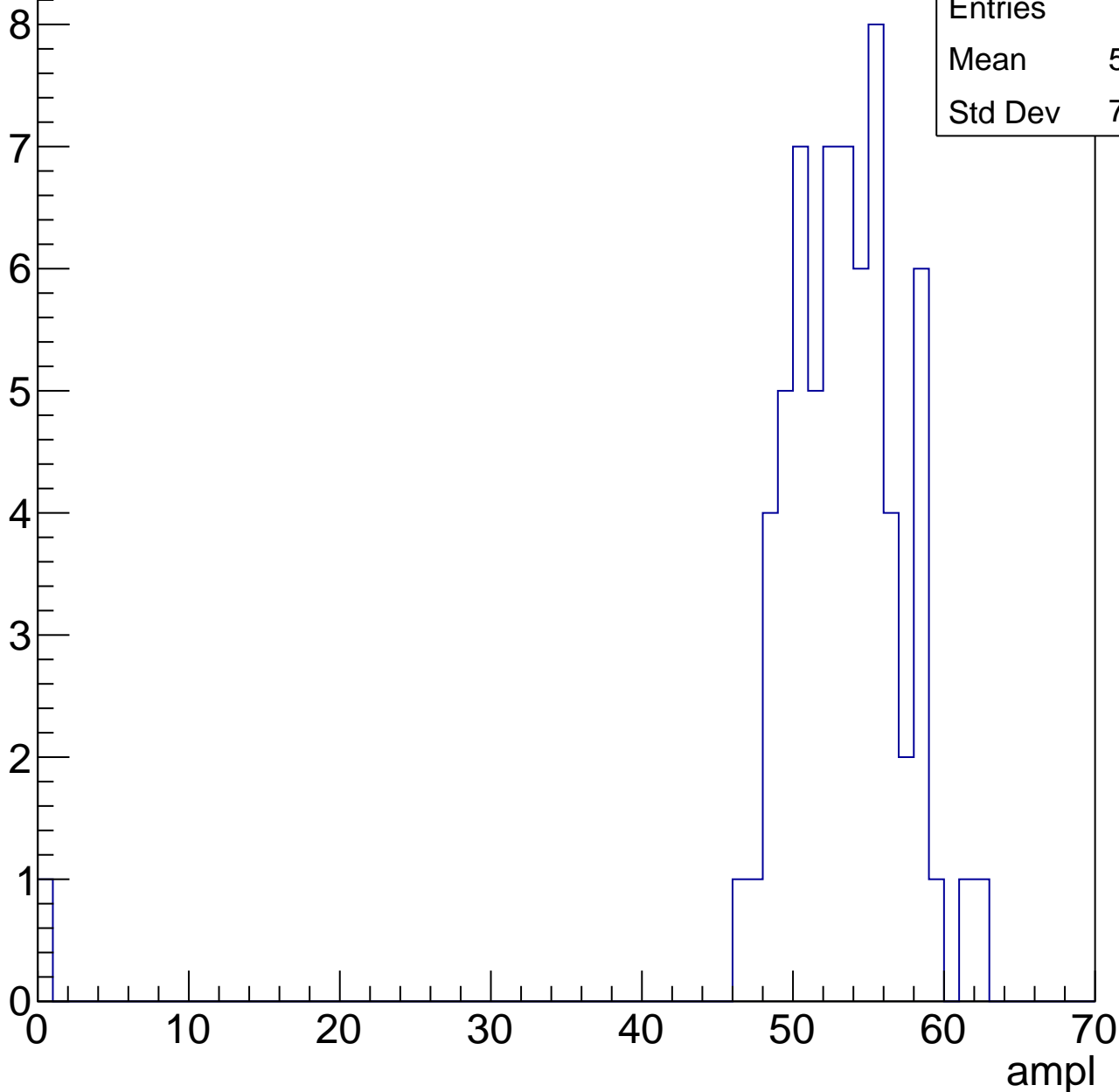


B1L103S, U23-ch50, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	52.27
Std Dev	7.295



B1L103S, U23-ch50, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

10

8

6

4

2

0

0

10

20

30

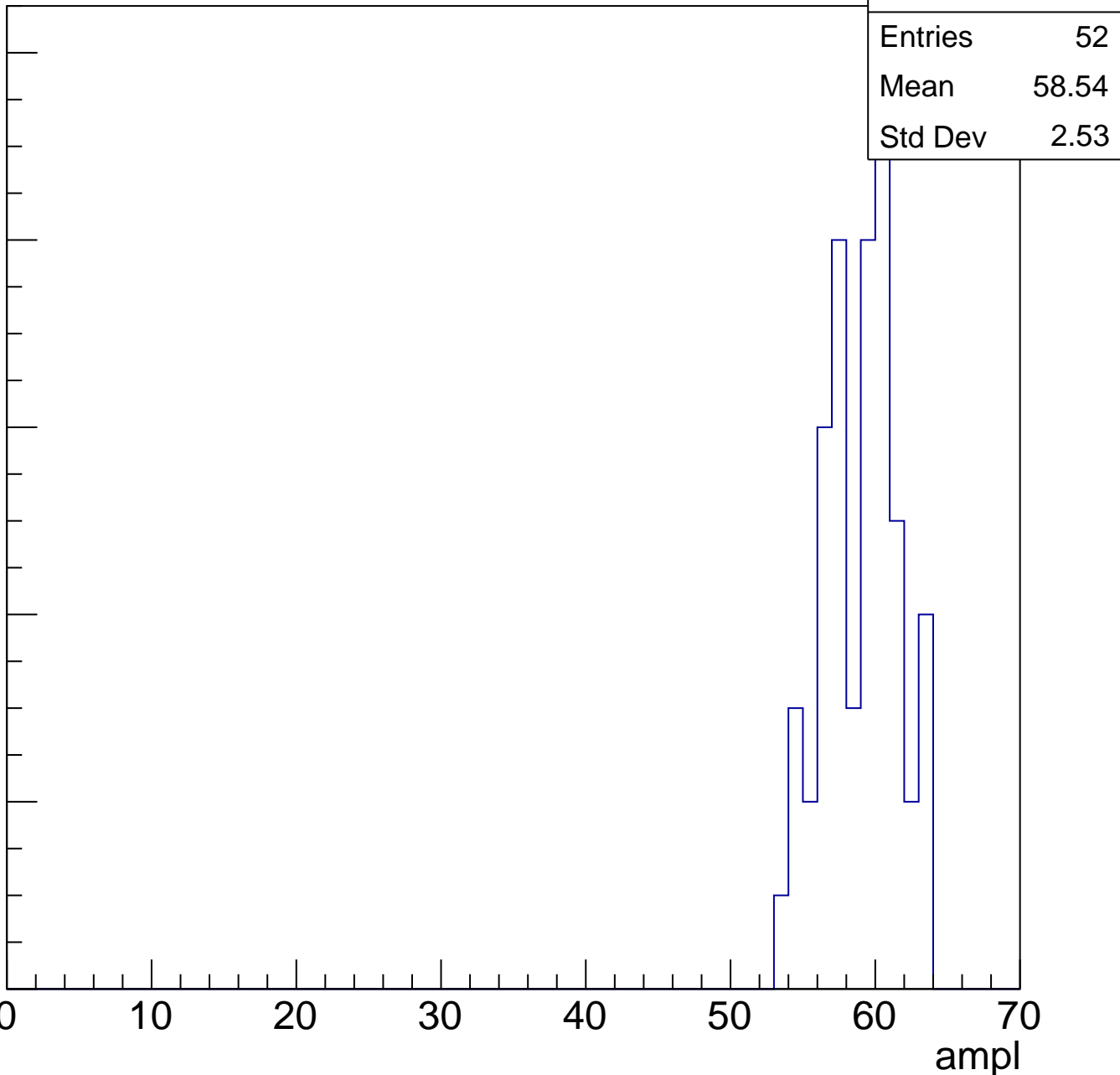
40

50

60

ampl

Entries	52
Mean	58.54
Std Dev	2.53

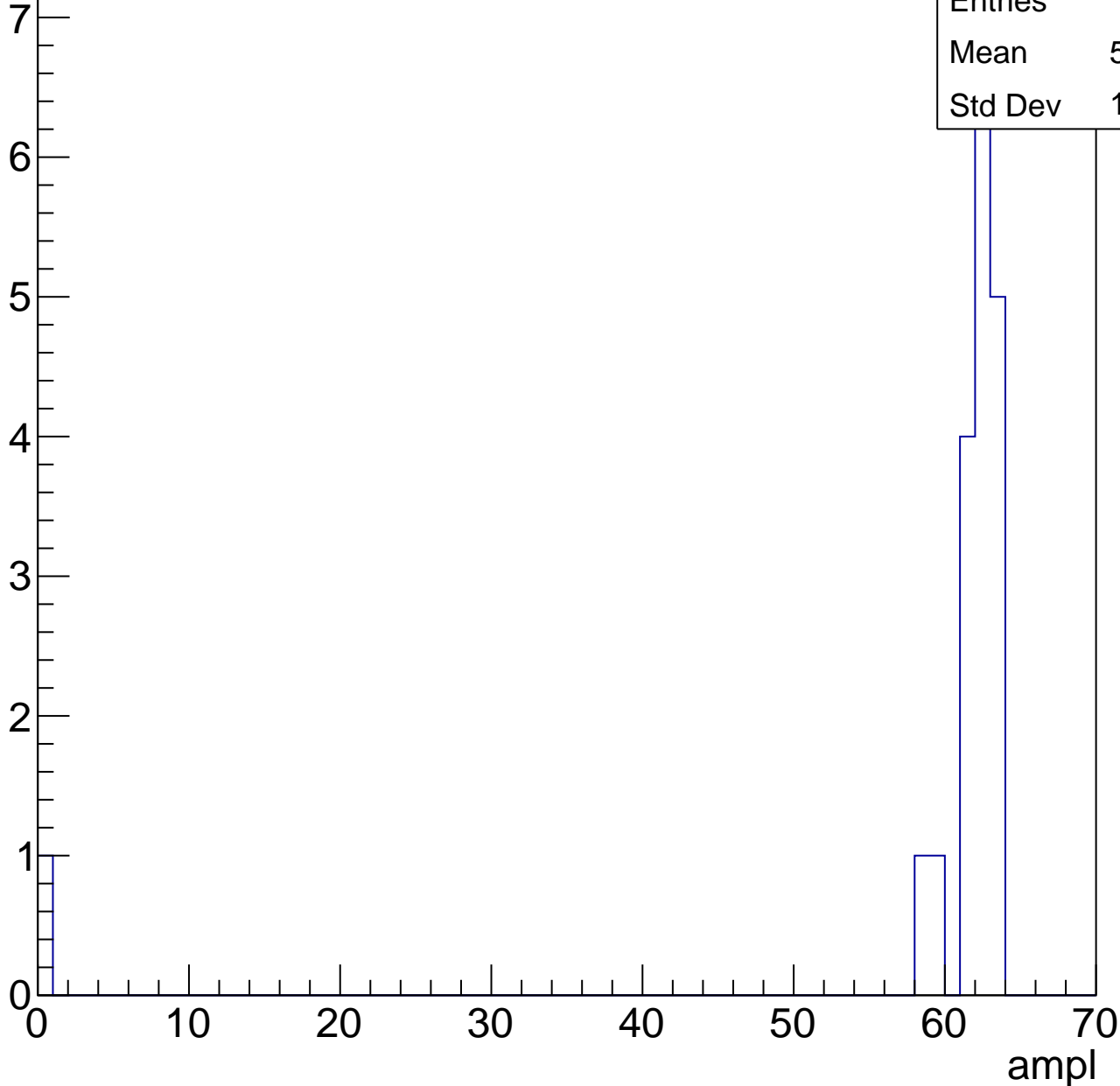


B1L103S, U23-ch50, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	19
Mean	58.42
Std Dev	13.83



B1L103S, U23-ch50, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.15
Std Dev	13.73

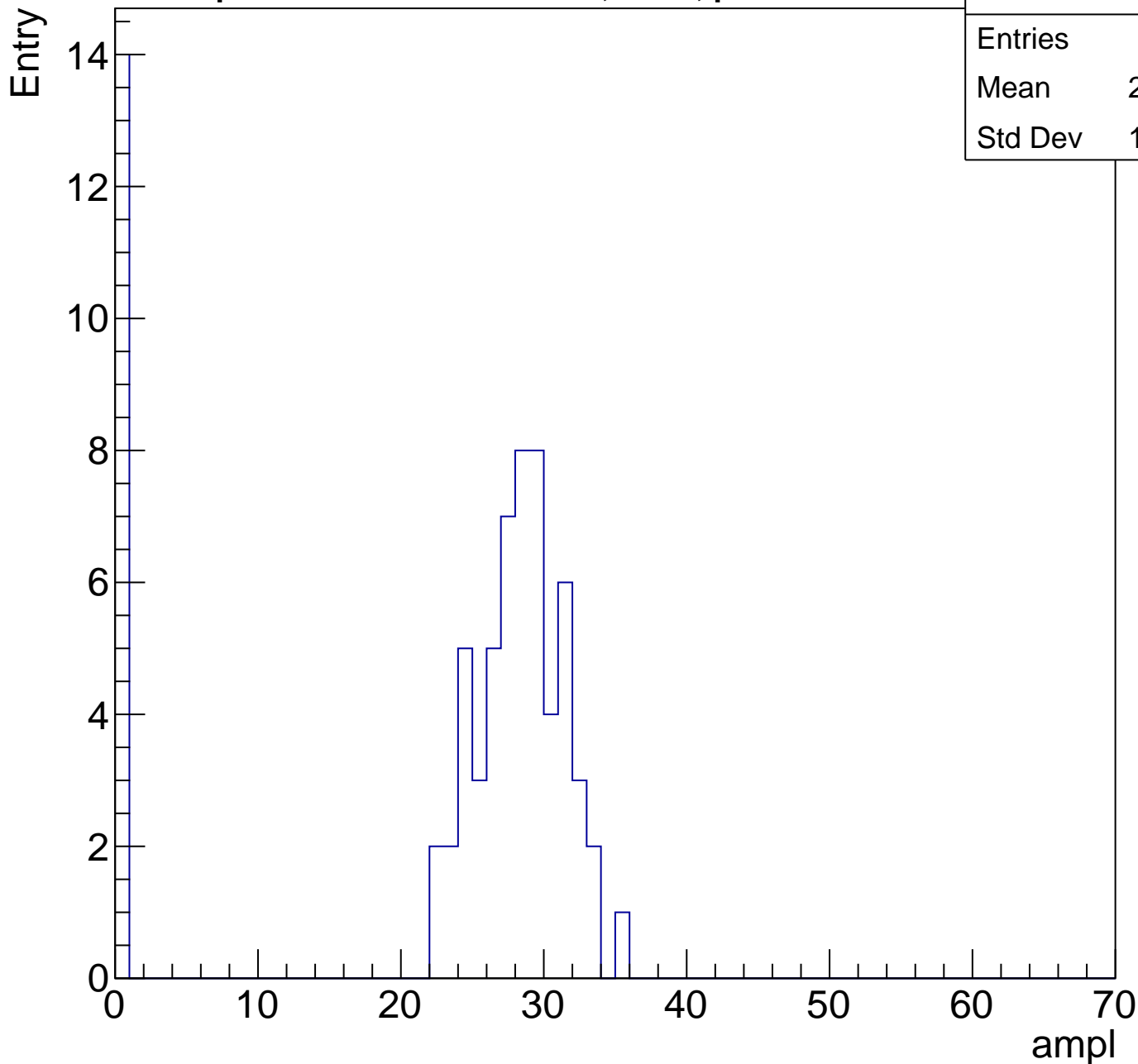
Entry



B1L103S, U23-ch51, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	70
Mean	22.33
Std Dev	11.47



B1L103S, U23-ch51, adc1

calib_packv5_041523_1651.root, FC#0, port C2

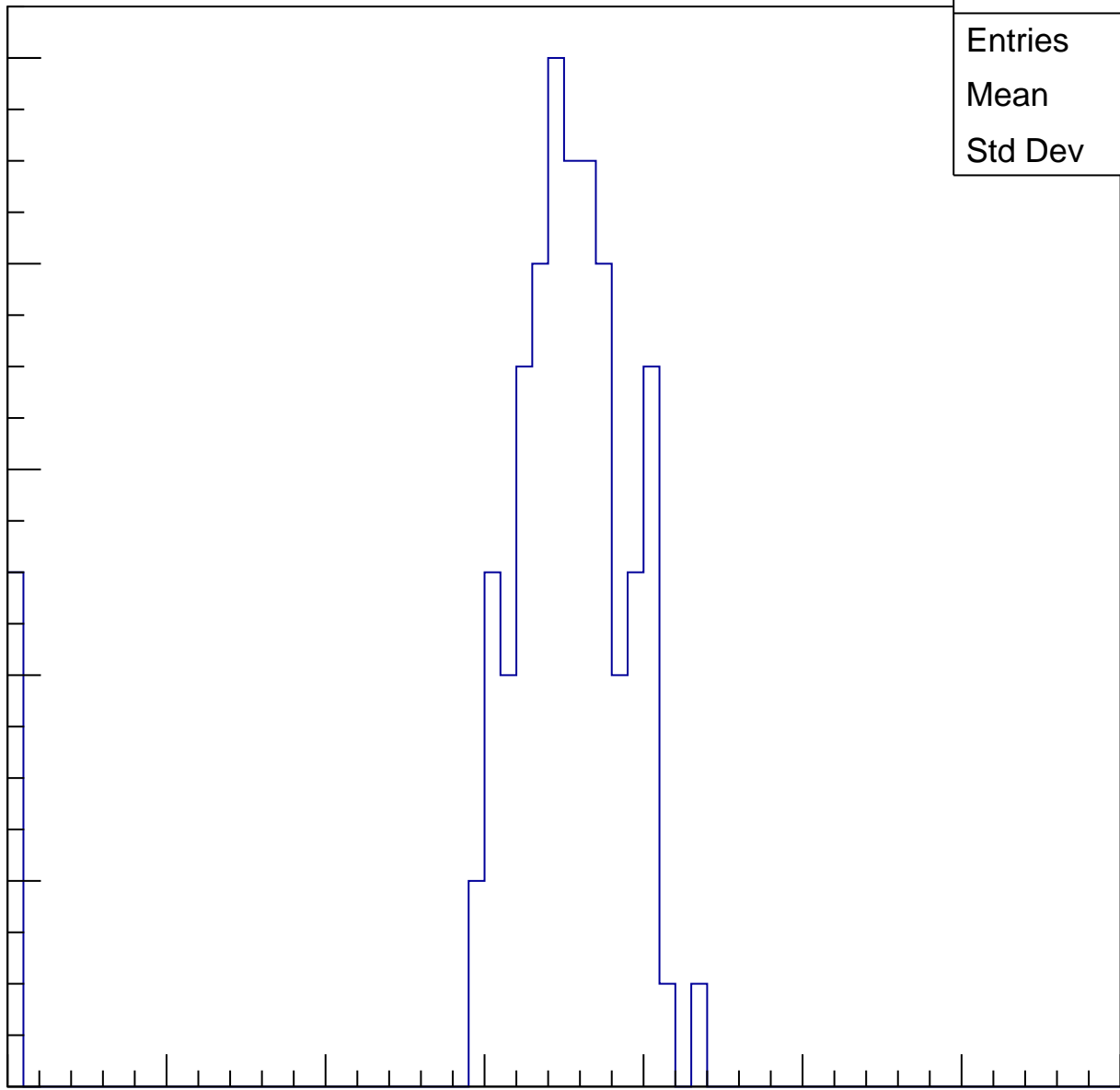
Entries	85
Mean	33.01
Std Dev	8.803

Entry

10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70

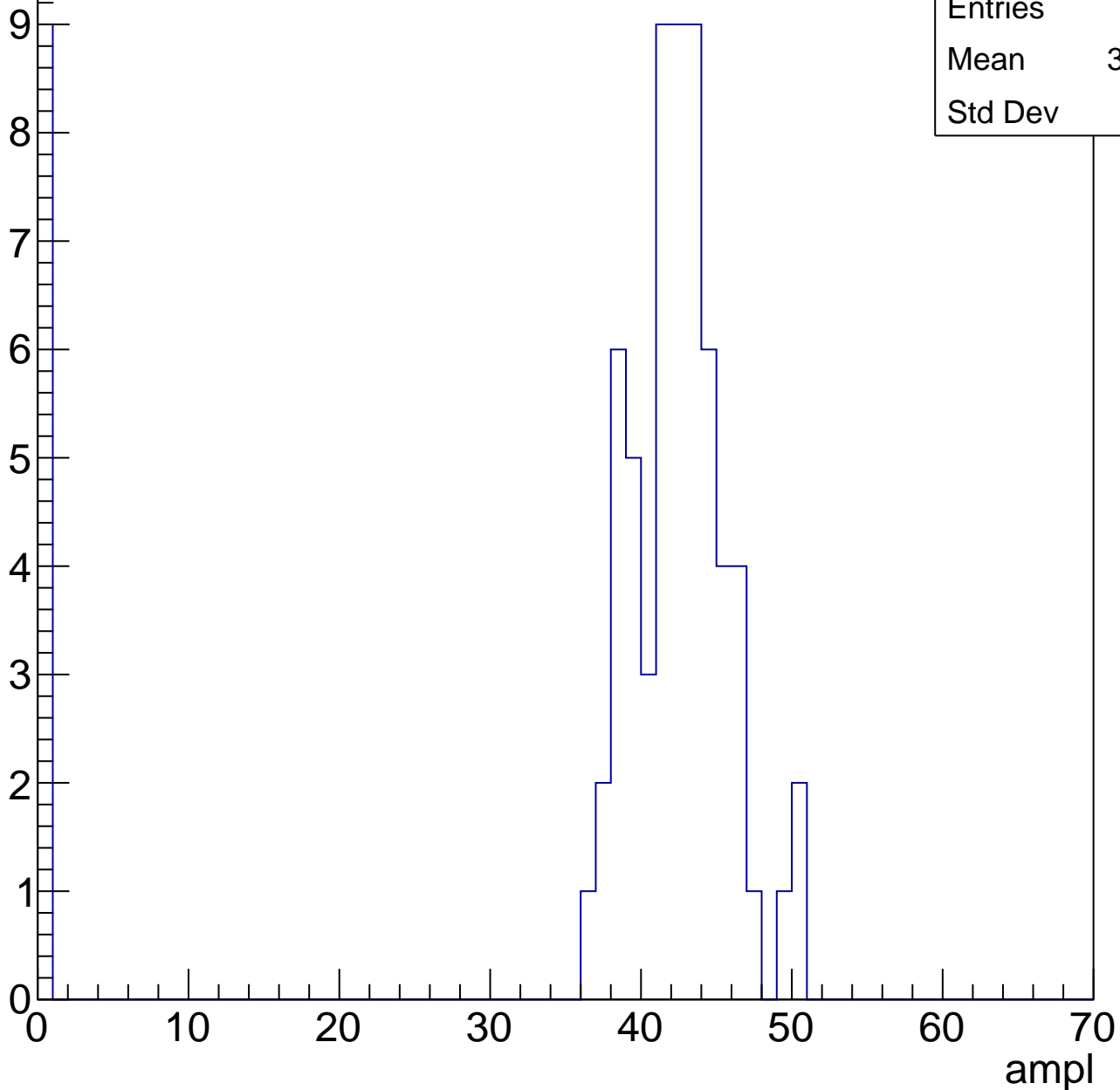


B1L103S, U23-ch51, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	36.77
Std Dev	14.3



B1L103S, U23-ch51, adc3

calib_packv5_041523_1651.root, FC#0, port C2

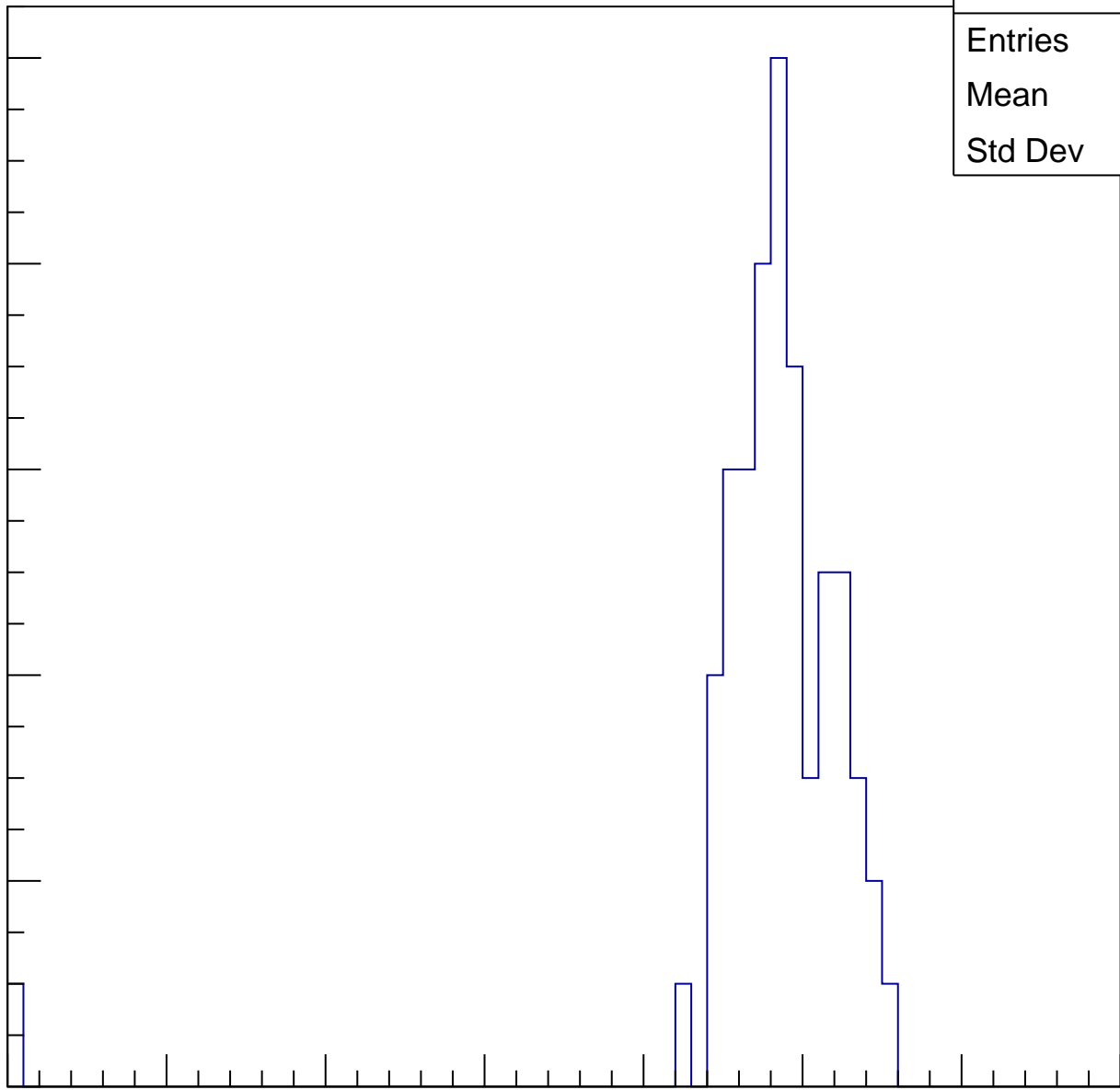
Entries	62
Mean	47.58
Std Dev	6.743

Entry

10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70

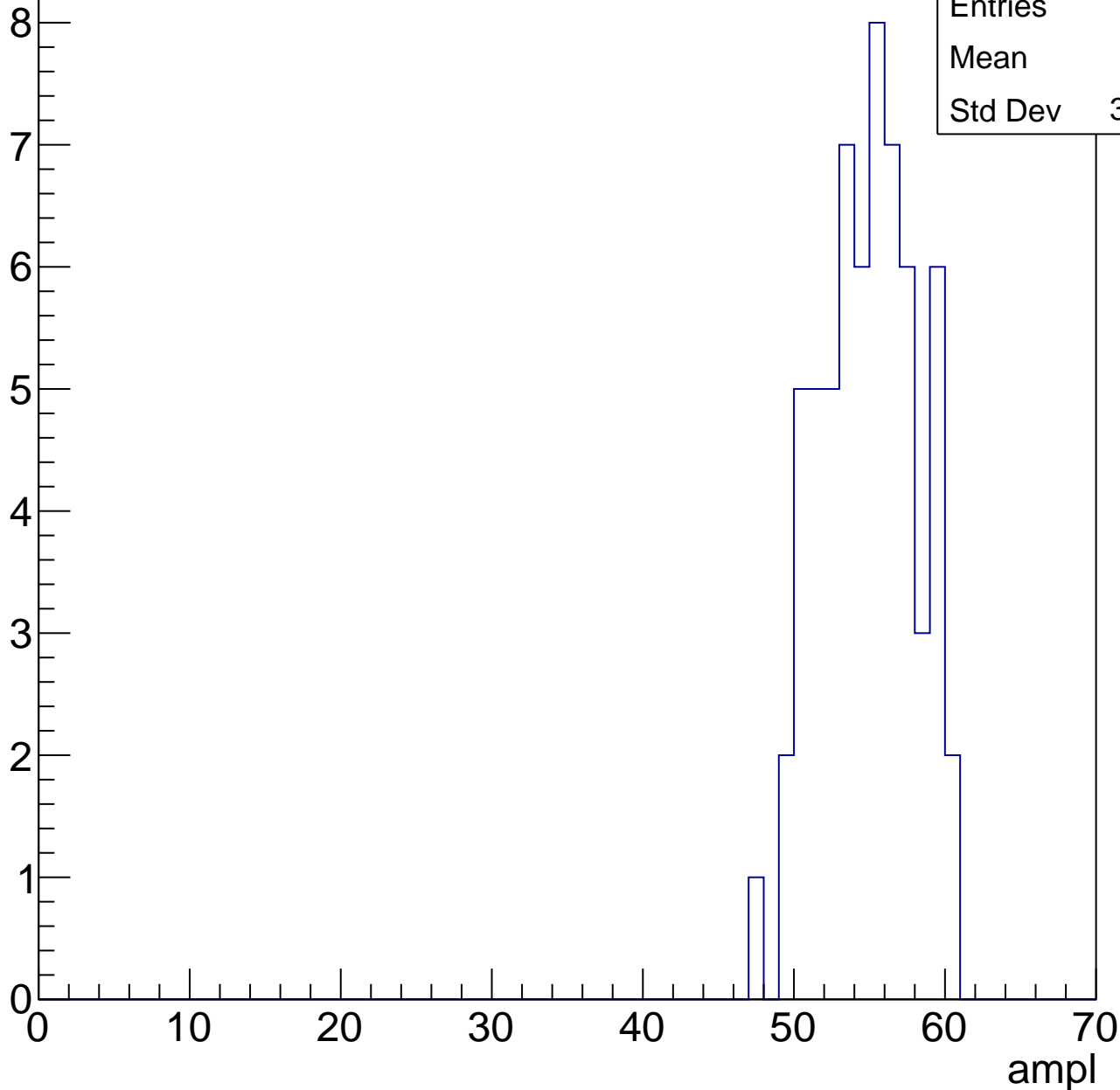


B1L103S, U23-ch51, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	63
Mean	54.4
Std Dev	3.089

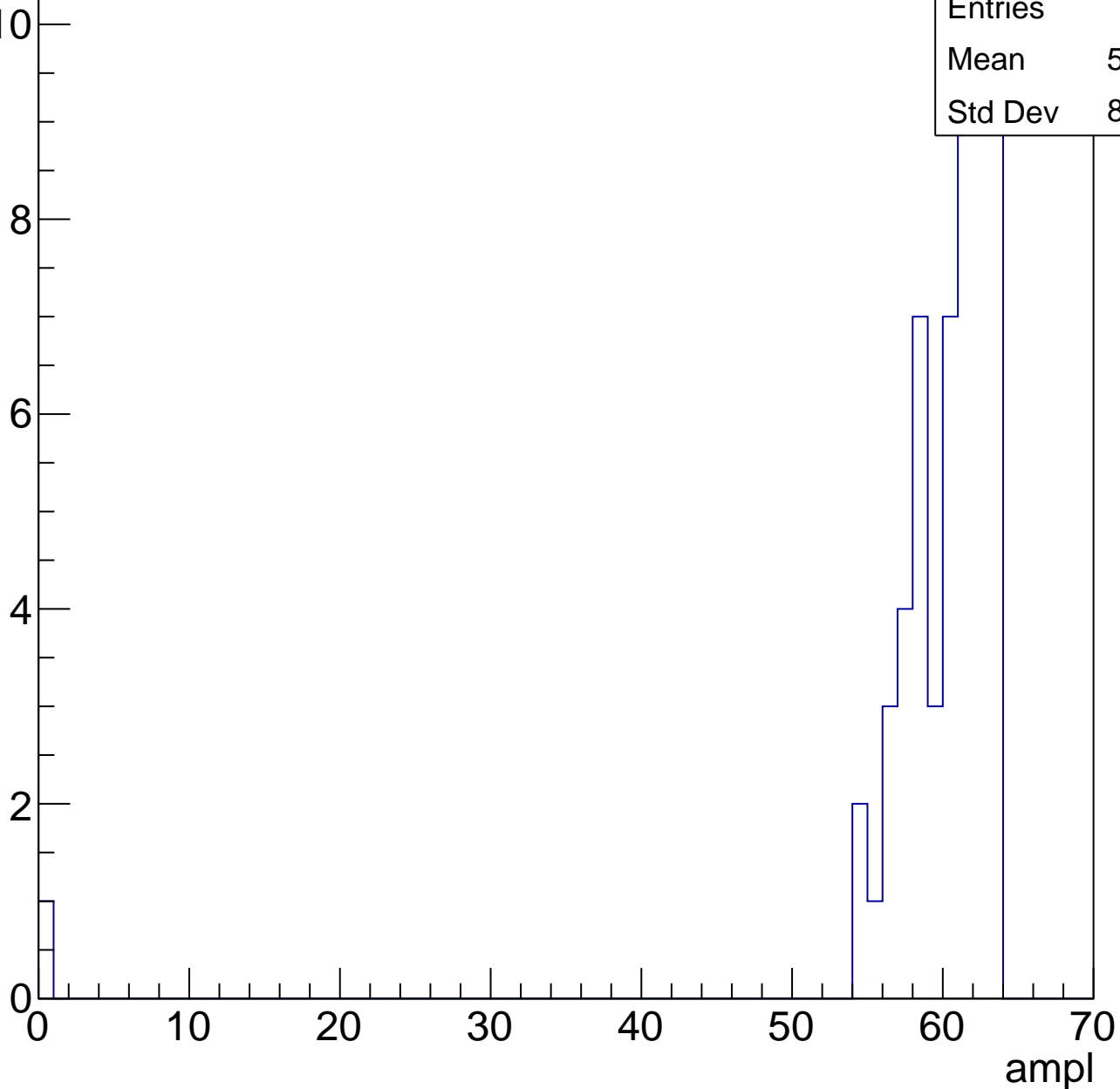


B1L103S, U23-ch51, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

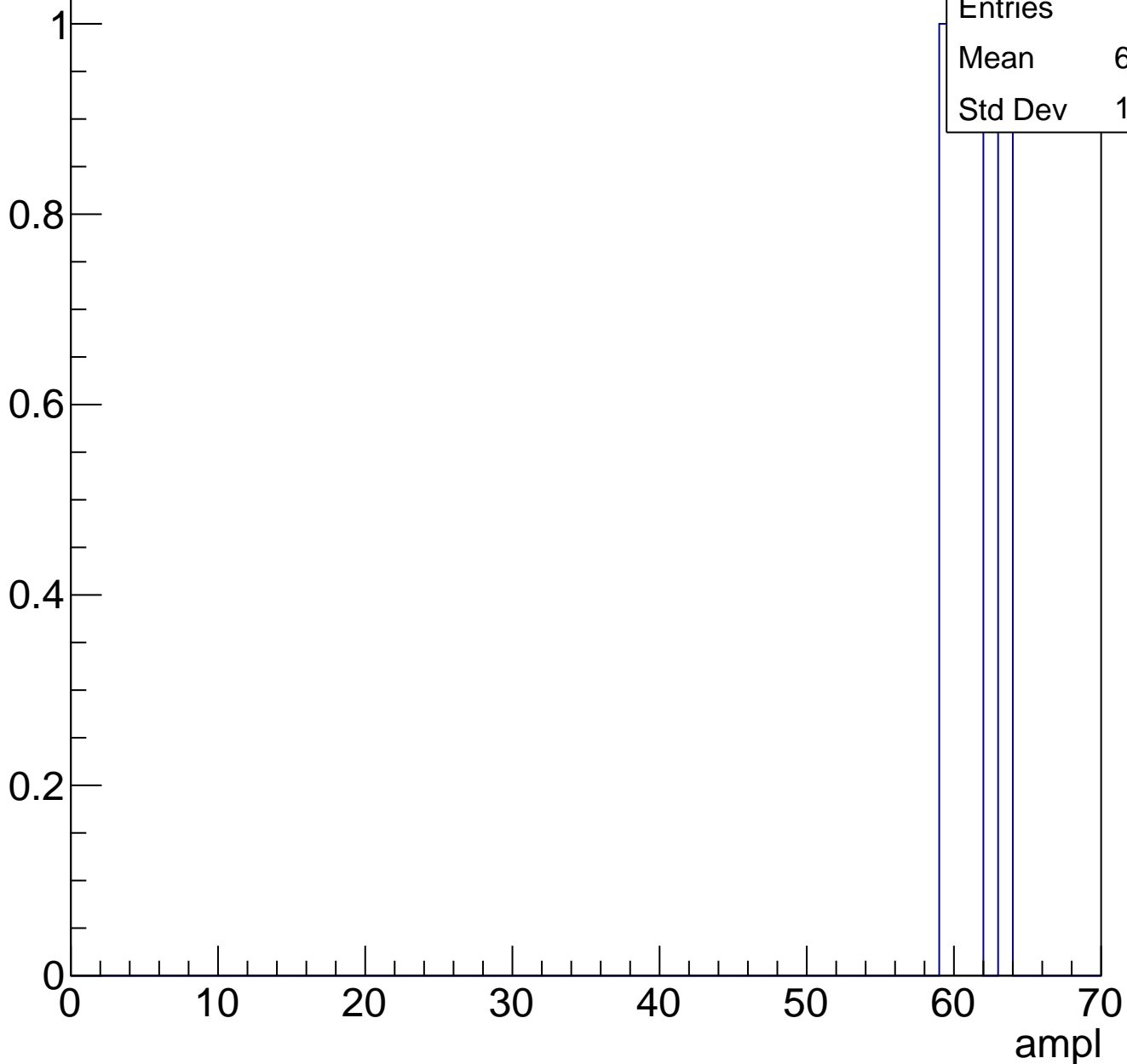
Entries	56
Mean	58.89
Std Dev	8.317



B1L103S, U23-ch51, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch51, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



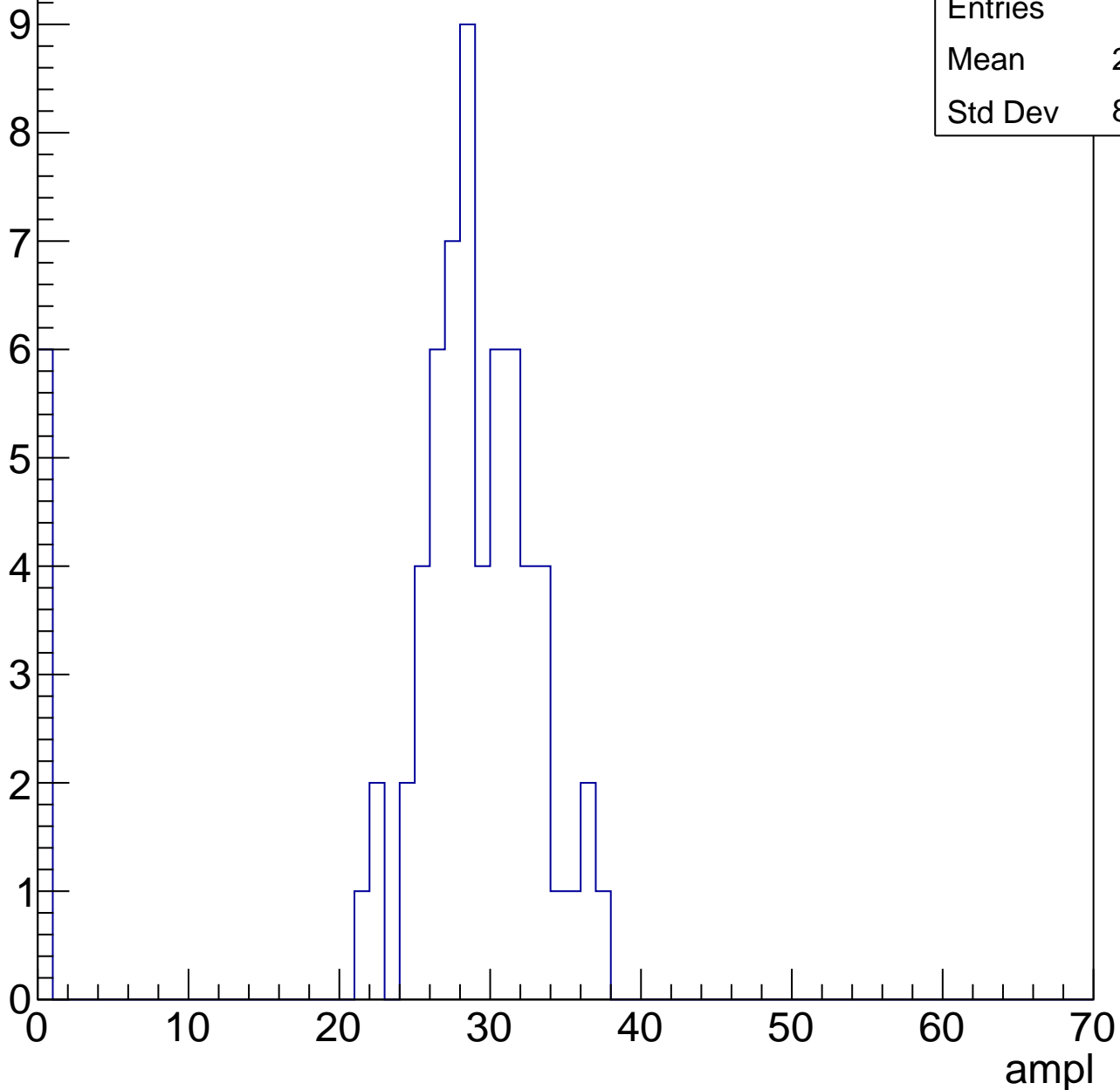
Entries	19
Mean	0
Std Dev	0

B1L103S, U23-ch52, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	26.21
Std Dev	8.921

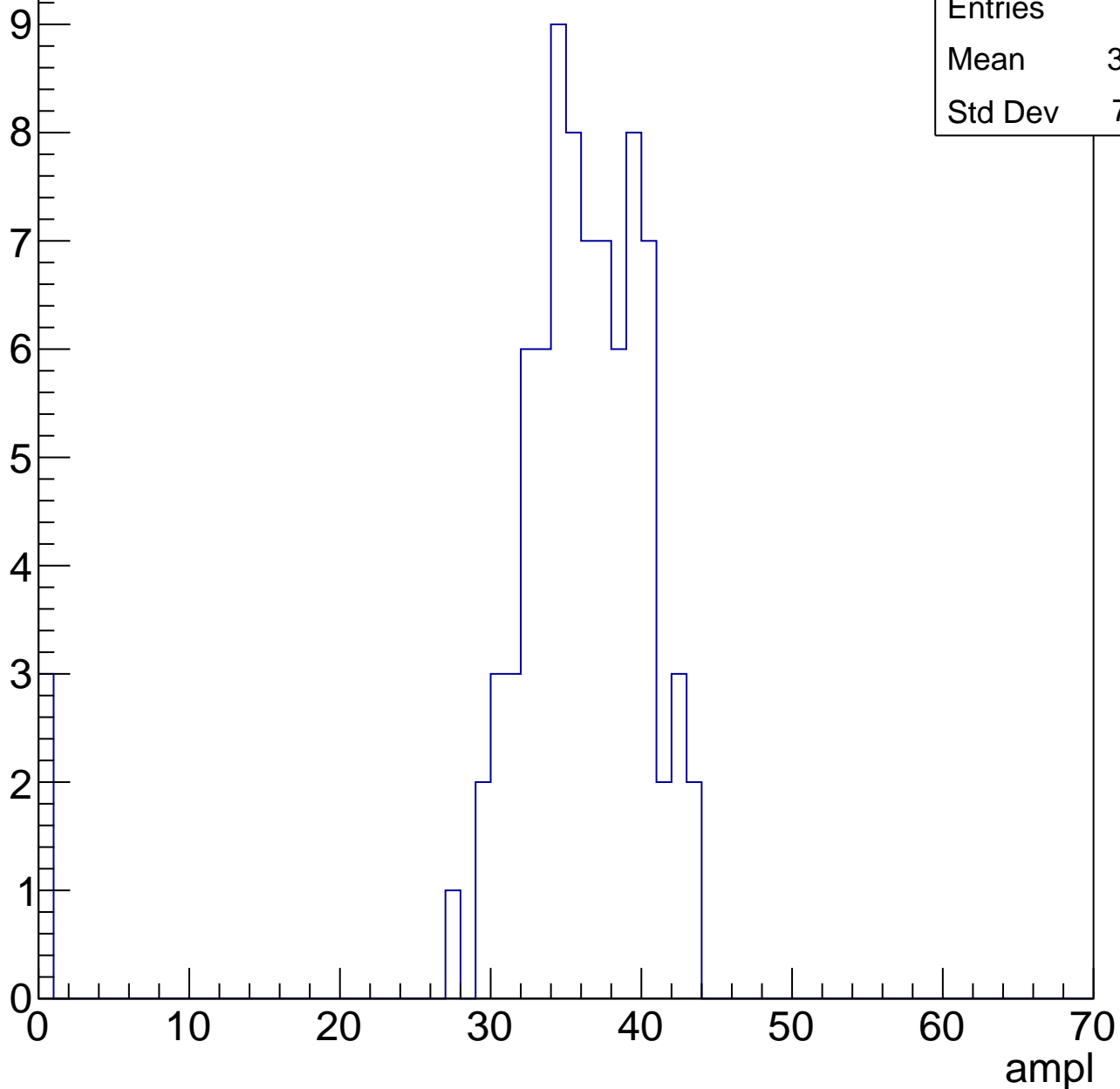


B1L103S, U23-ch52, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	83
Mean	34.57
Std Dev	7.561

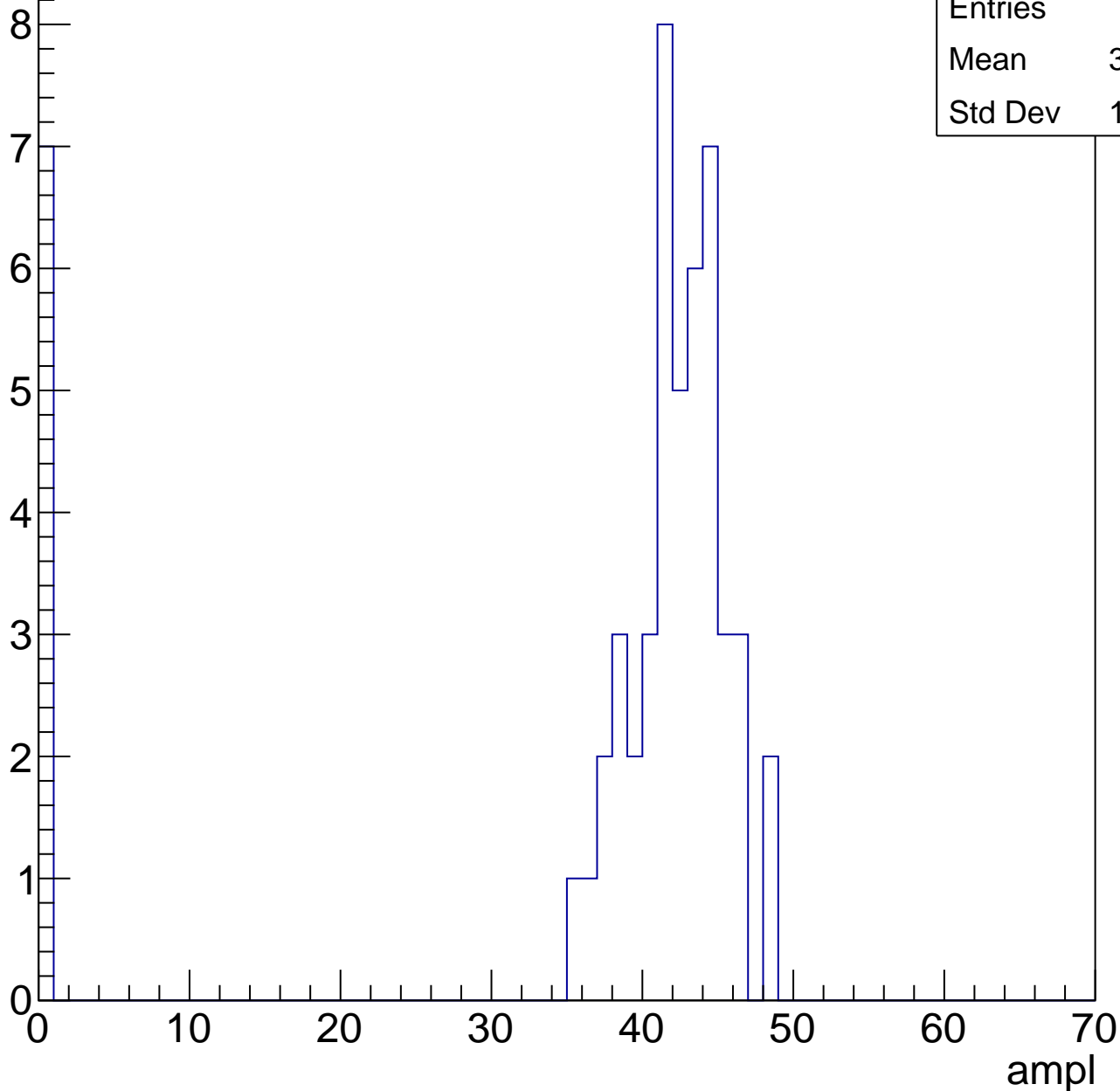


B1L103S, U23-ch52, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	53
Mean	36.42
Std Dev	14.47



B1L103S, U23-ch52, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	82
Mean	48.09
Std Dev	6.344

Entry

10

8

6

4

2

0

0

10

20

30

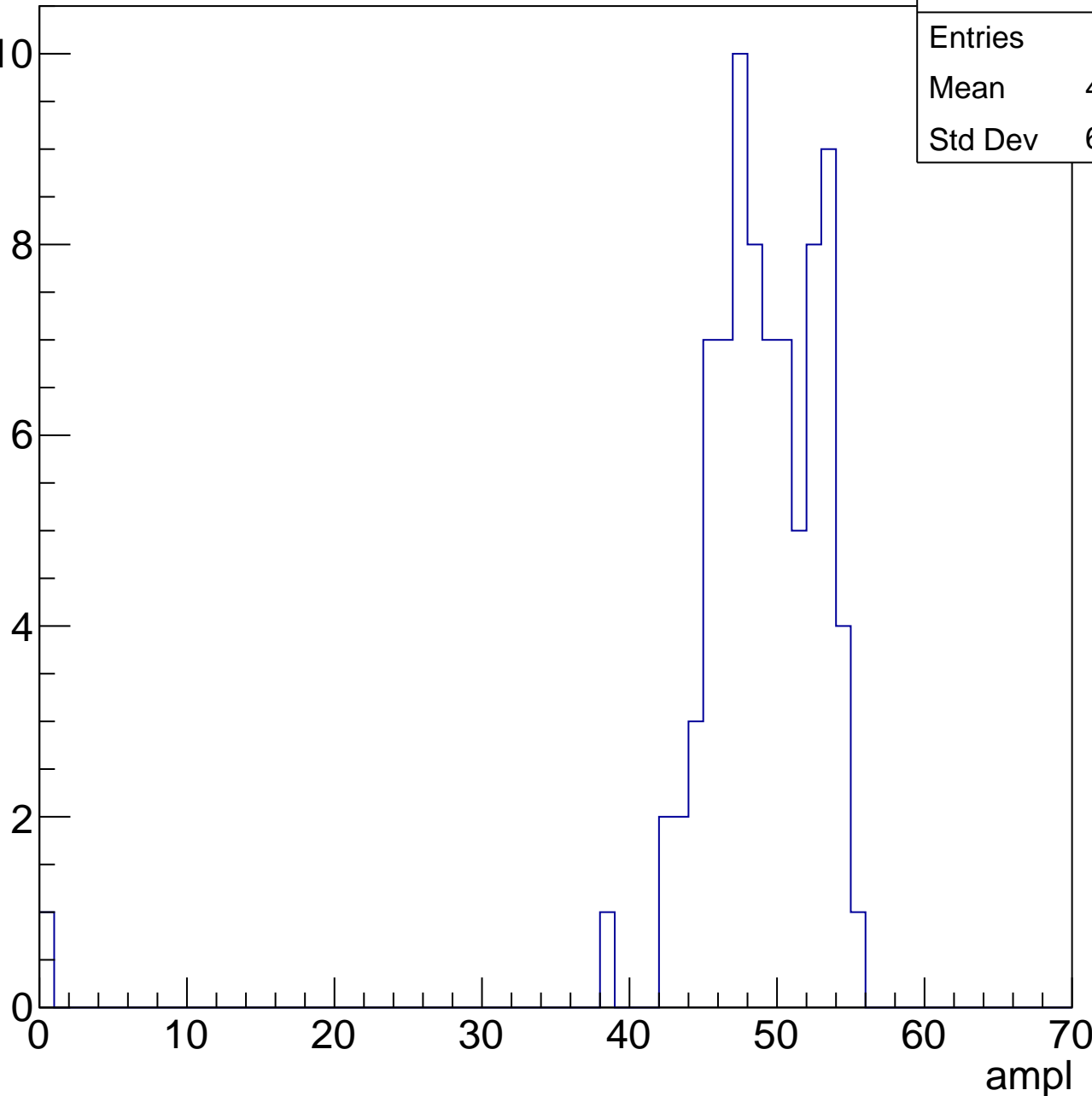
40

50

60

70

ampl

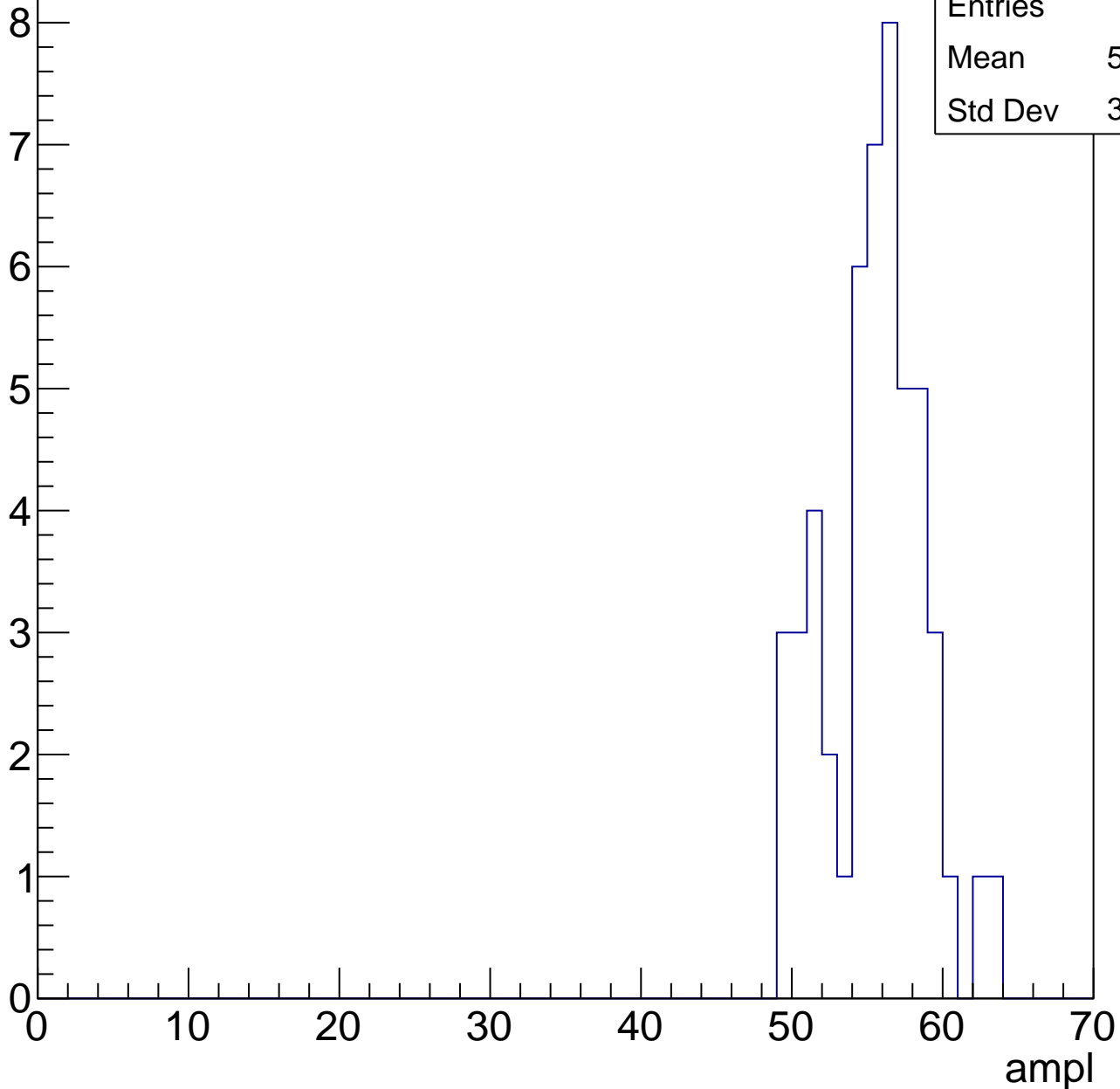


B1L103S, U23-ch52, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	50
Mean	55.04
Std Dev	3.268



B1L103S, U23-ch52, adc5

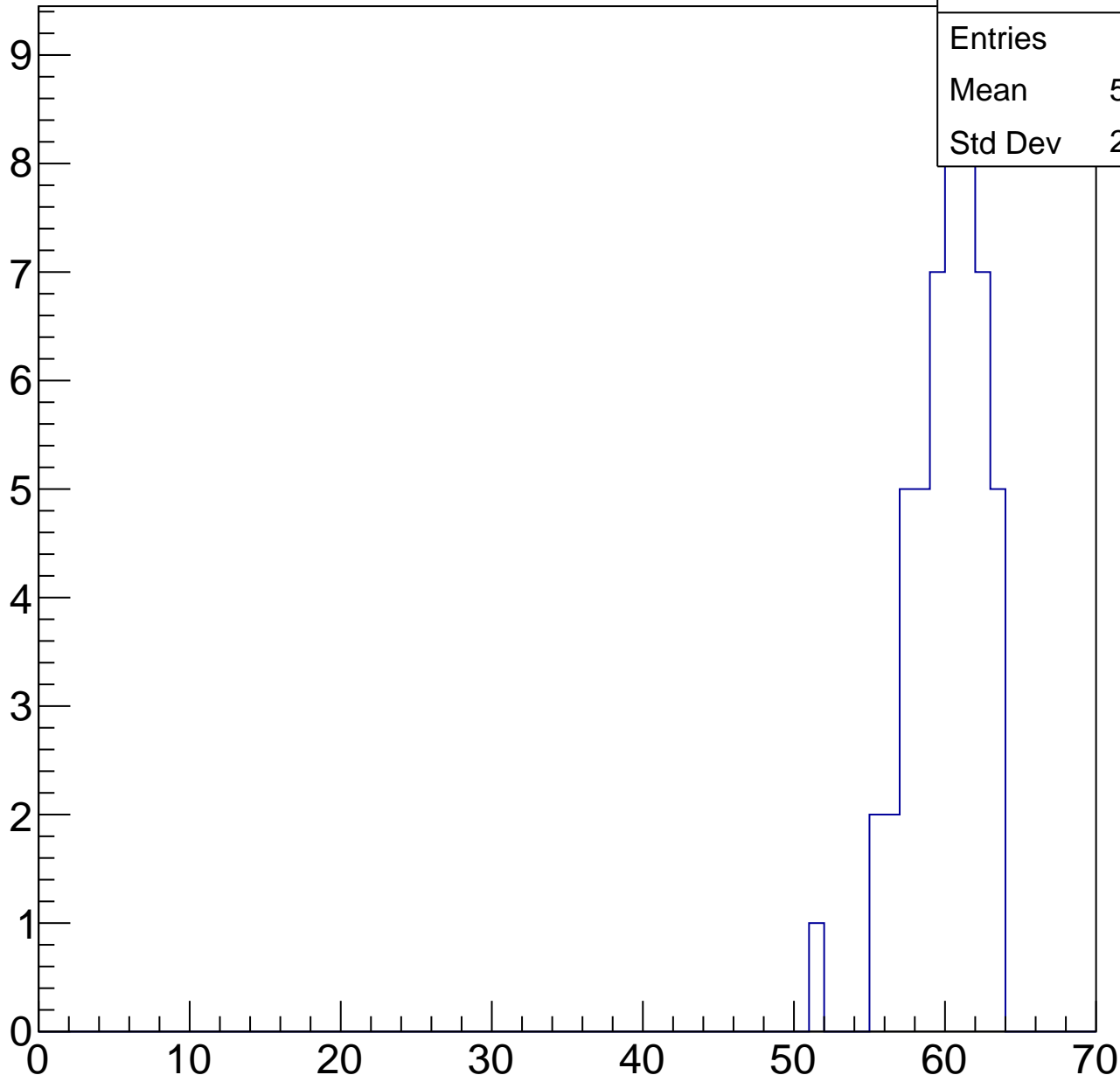
calib_packv5_041523_1651.root, FC#0, port C2

Entry

9
8
7
6
5
4
3
2
1
0

Entries	51
Mean	59.57
Std Dev	2.452

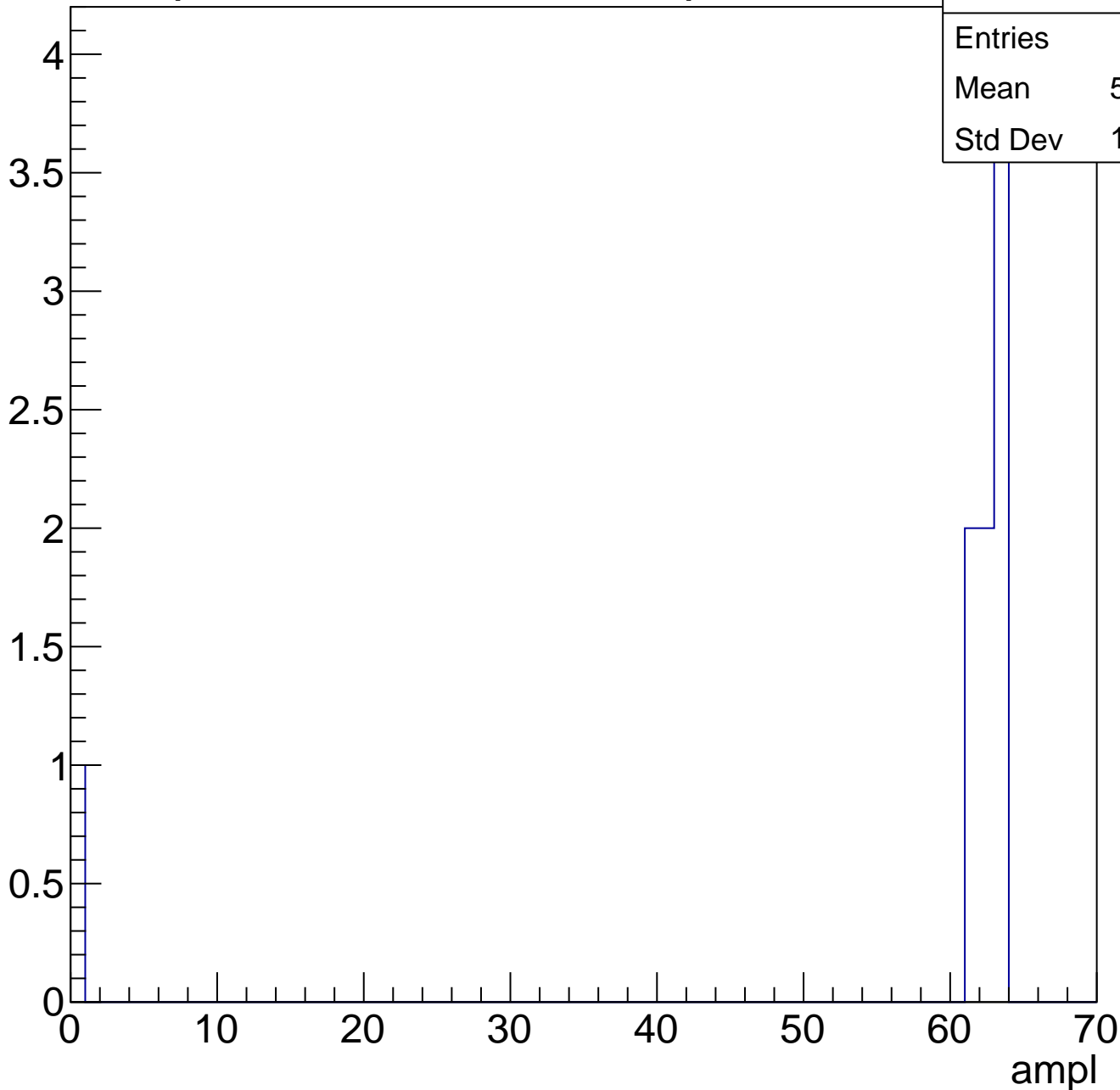
ampl



B1L103S, U23-ch52, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

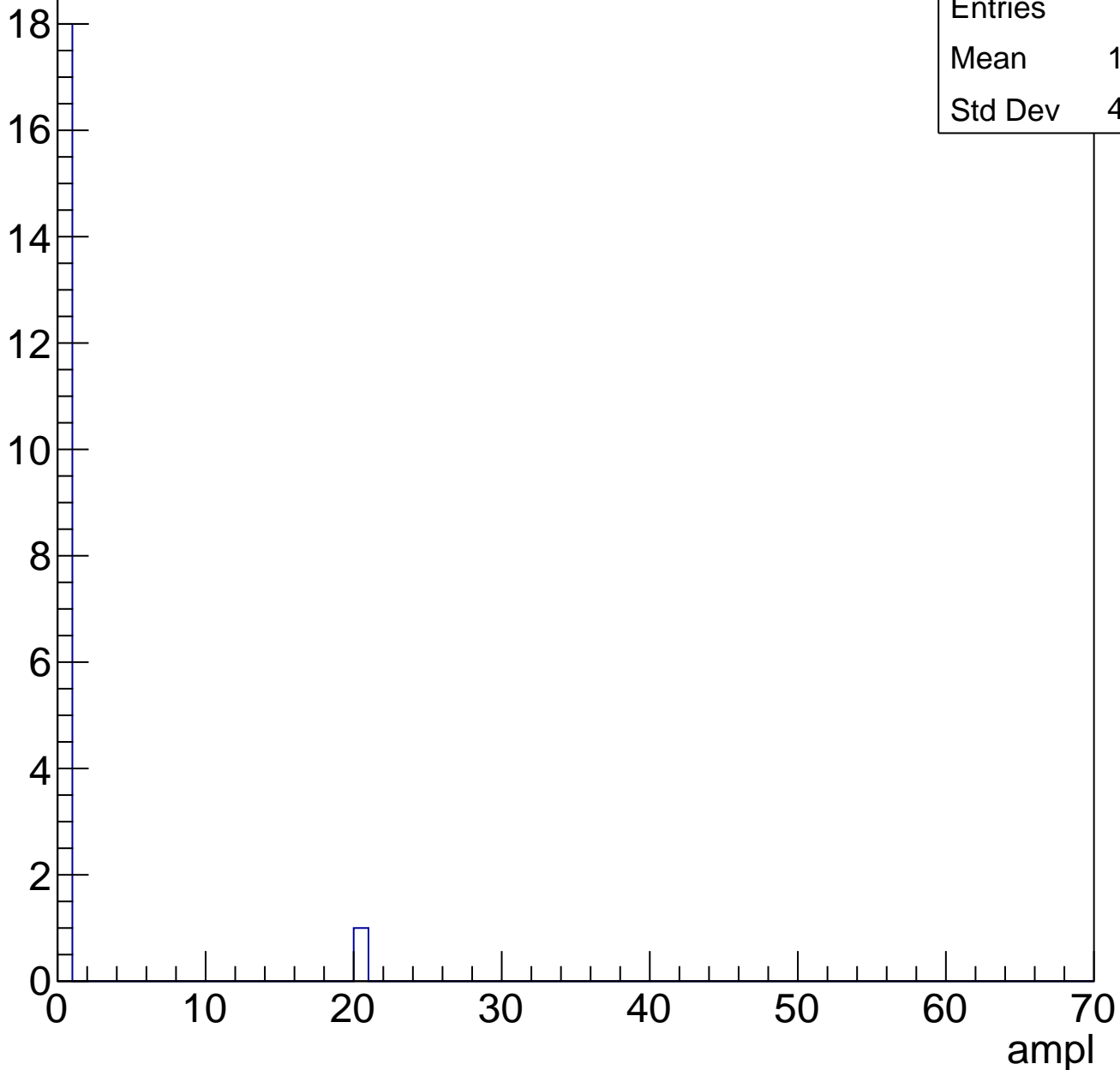


B1L103S, U23-ch52, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.053
Std Dev	4.466

Entry



B1L103S, U23-ch53, adc0

calib_packv5_041523_1651.root, FC#0, port C2

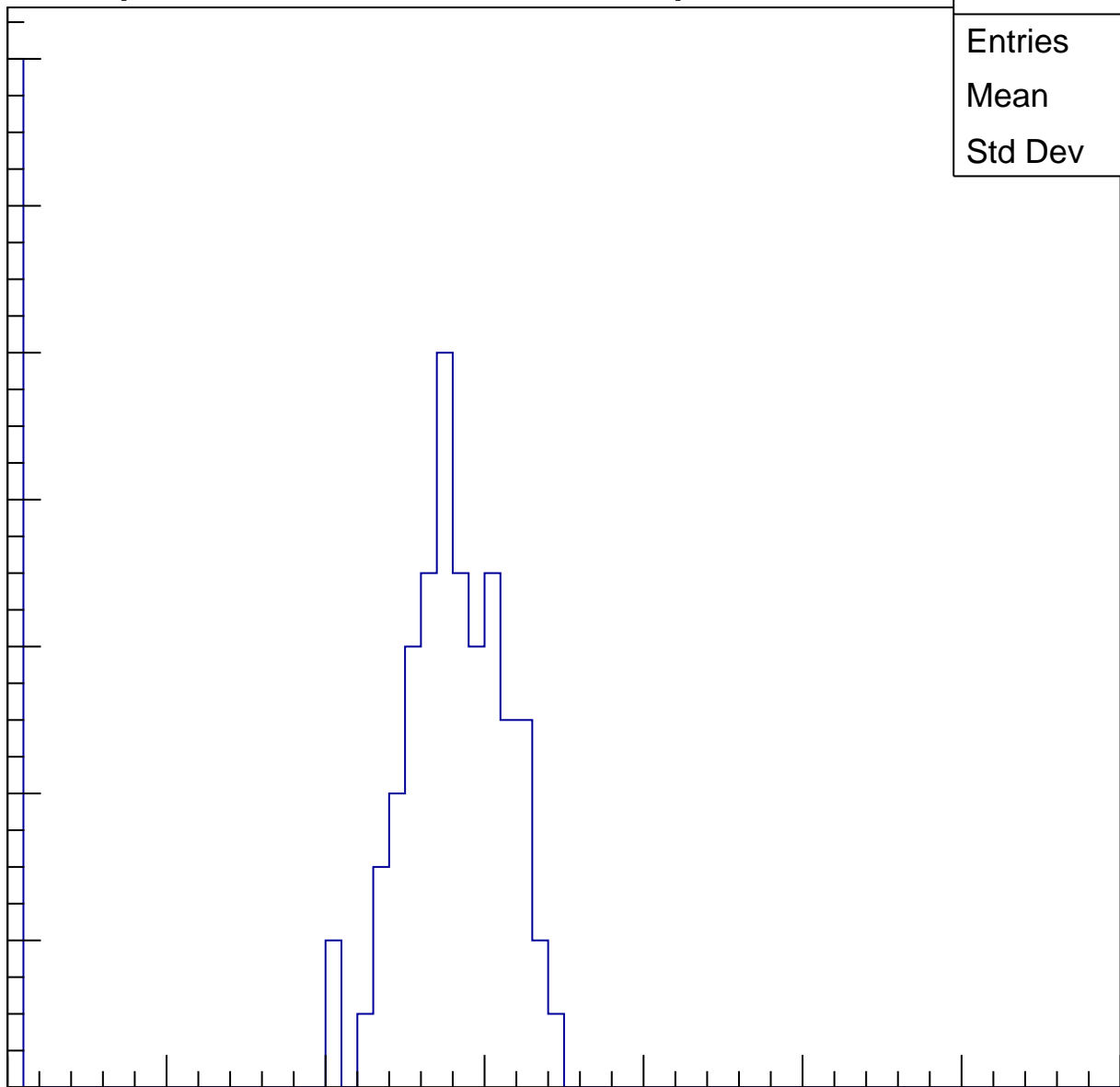
Entries	80
Mean	22.8
Std Dev	10.87

Entry

14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

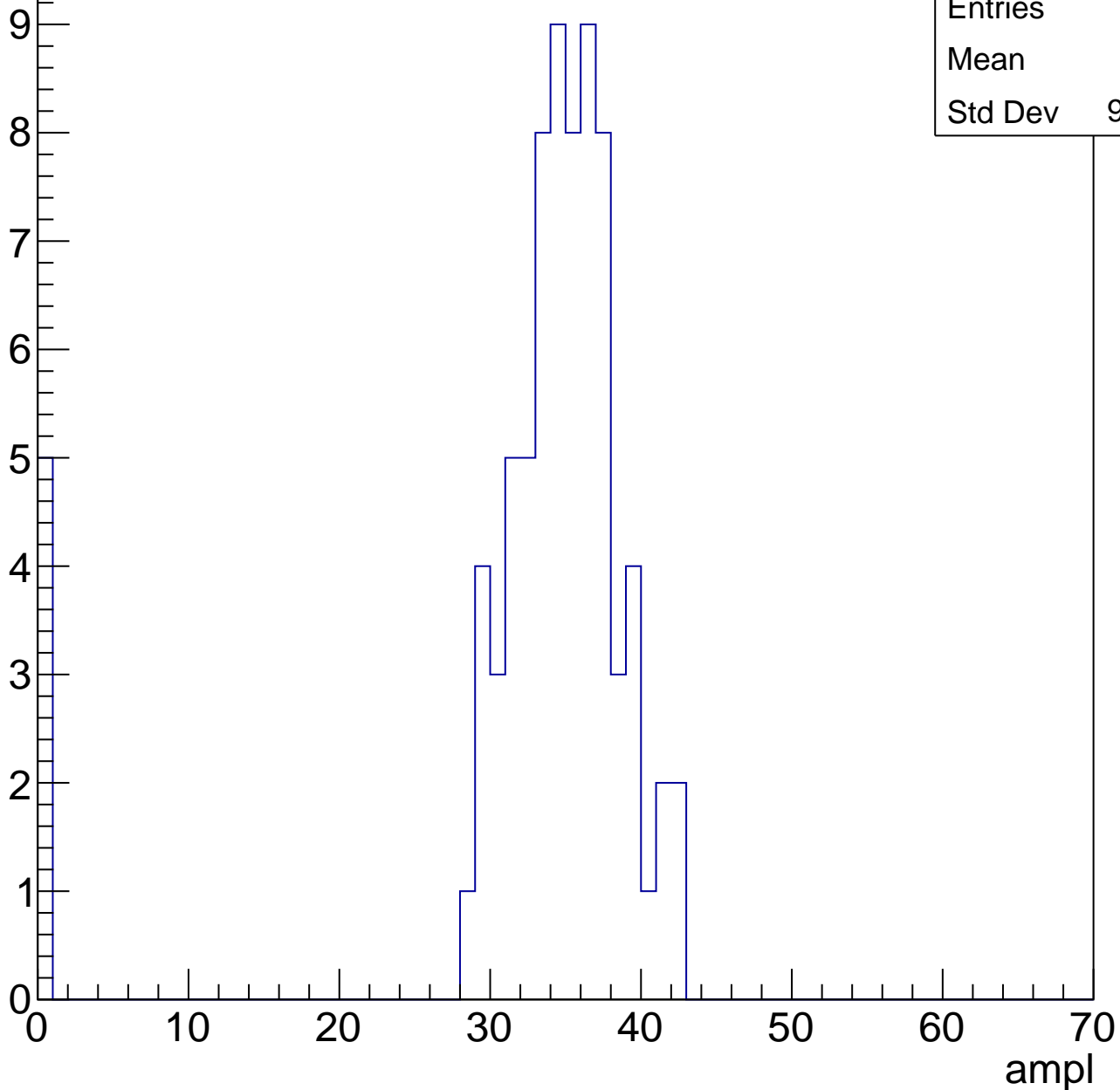


B1L103S, U23-ch53, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	77
Mean	32.4
Std Dev	9.093

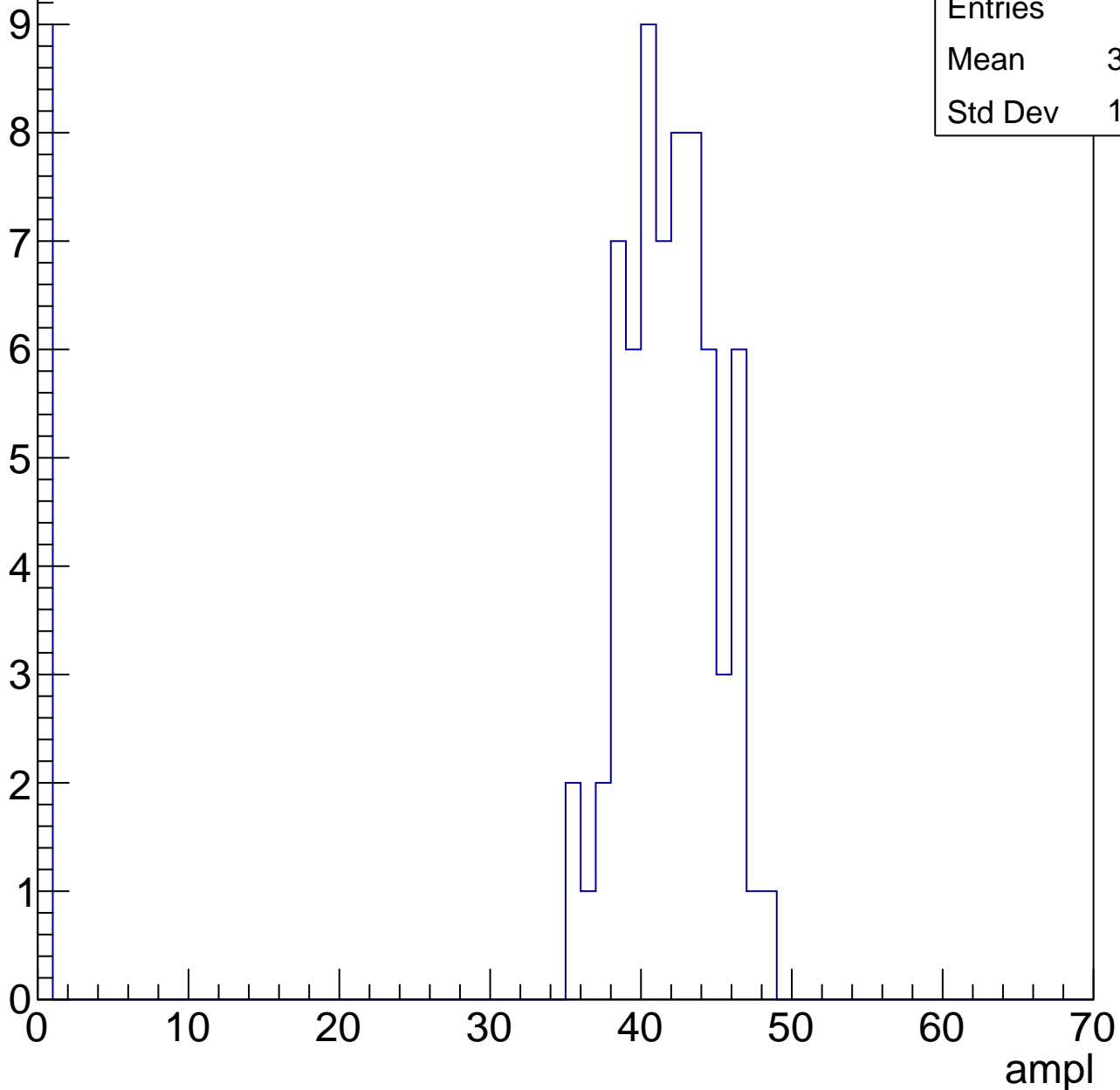


B1L103S, U23-ch53, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	76
Mean	36.54
Std Dev	13.68

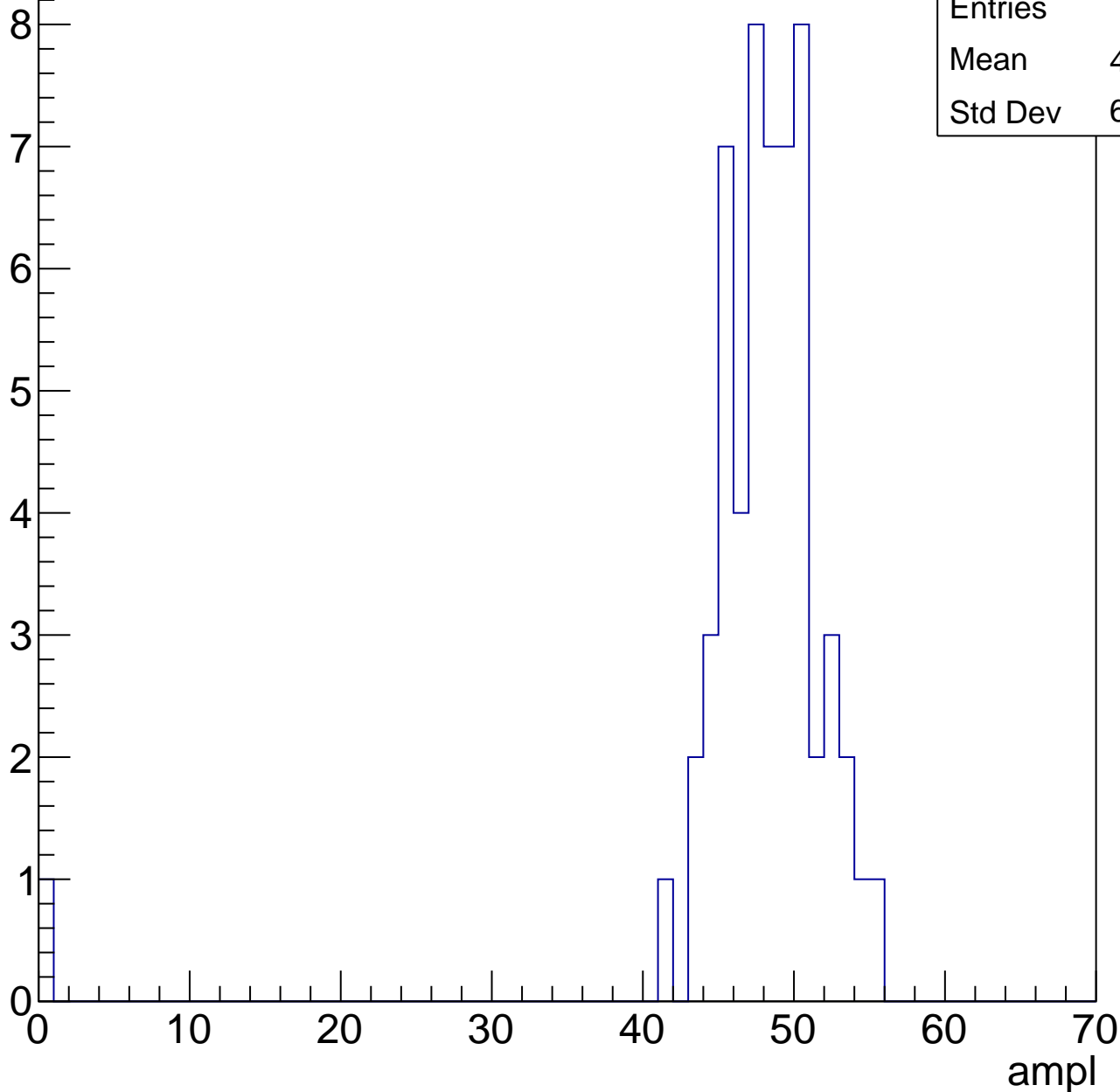


B1L103S, U23-ch53, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	57
Mean	47.12
Std Dev	6.926

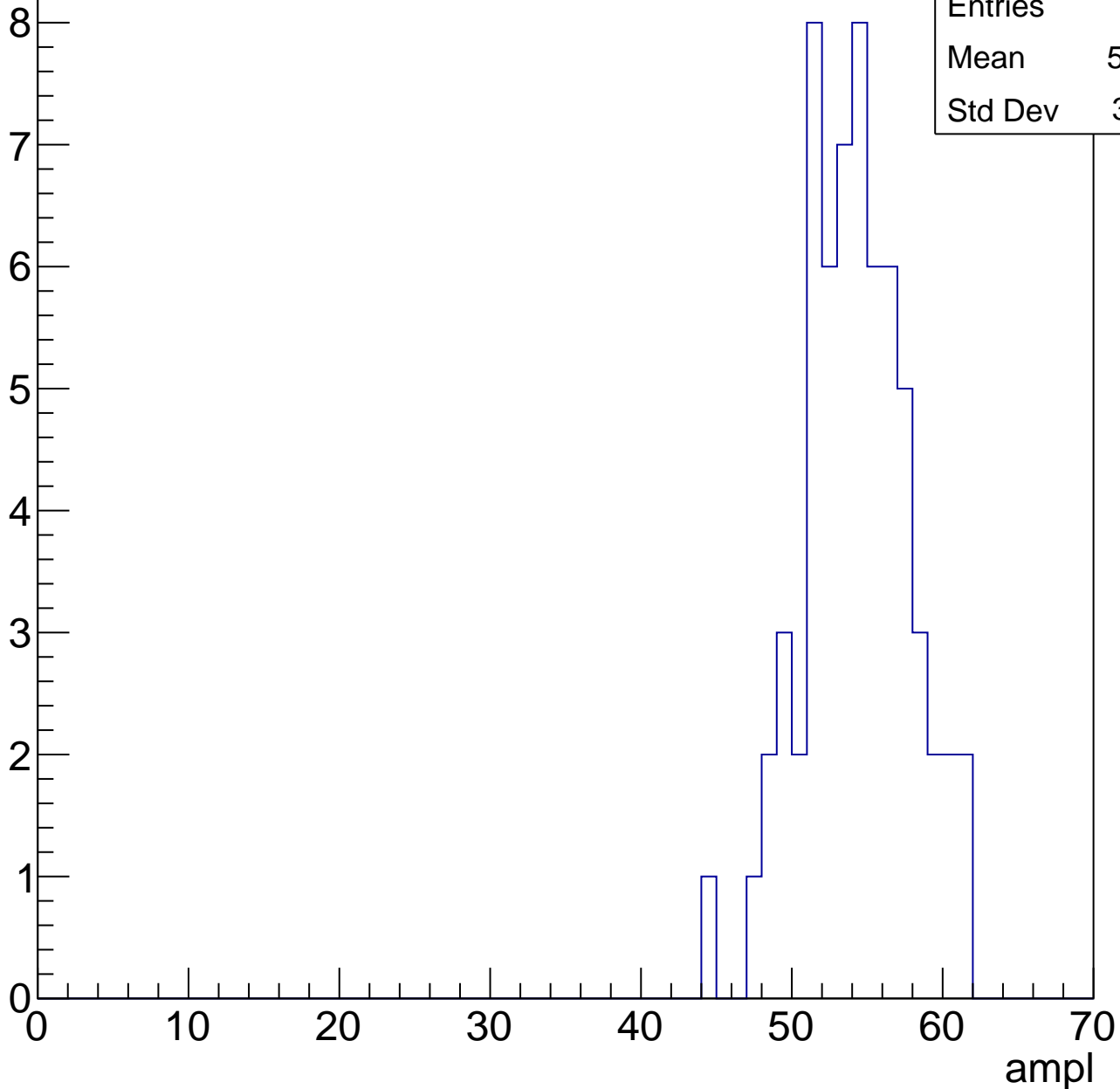


B1L103S, U23-ch53, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	53.78
Std Dev	3.471

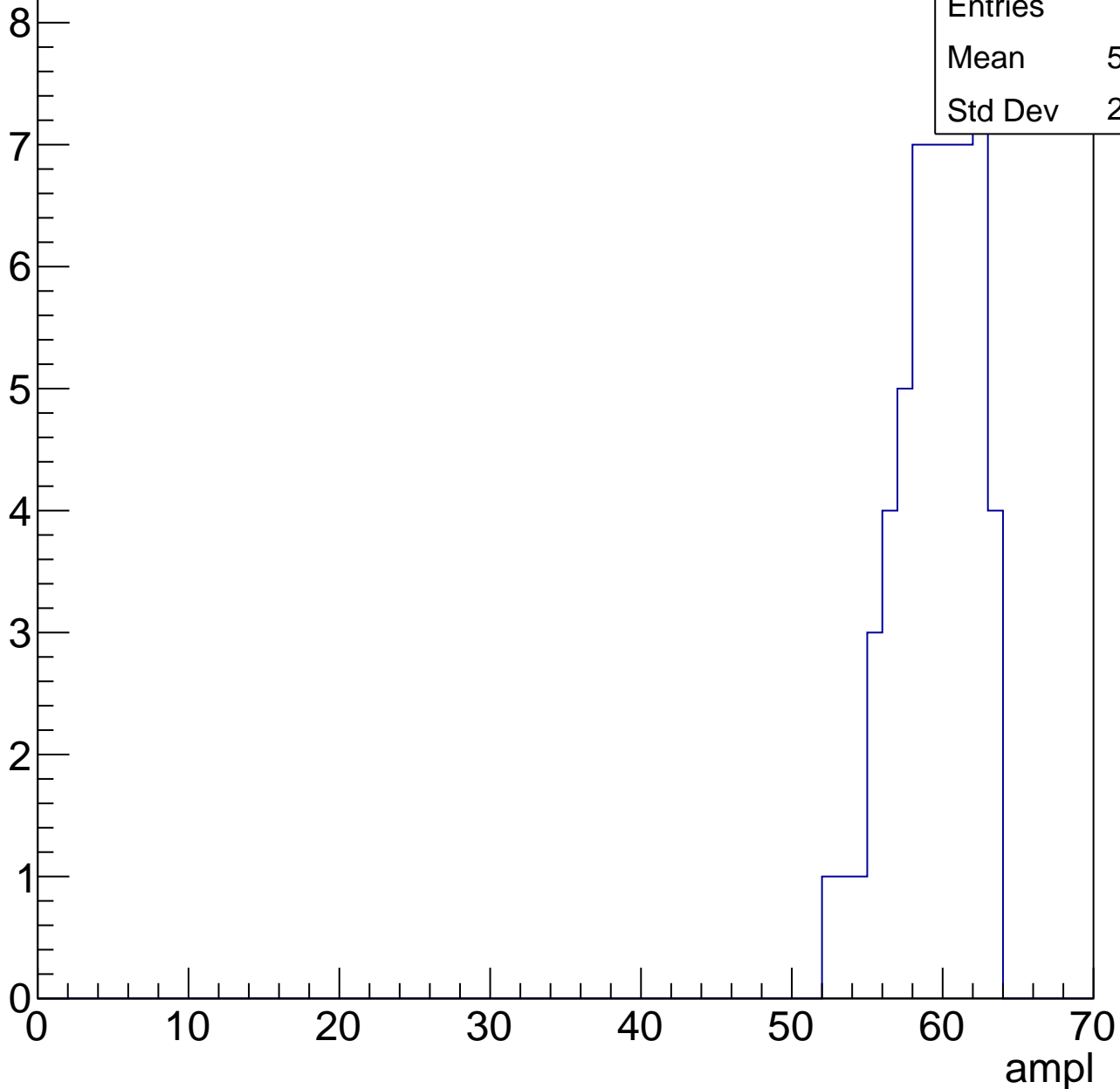


B1L103S, U23-ch53, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	59.04
Std Dev	2.669

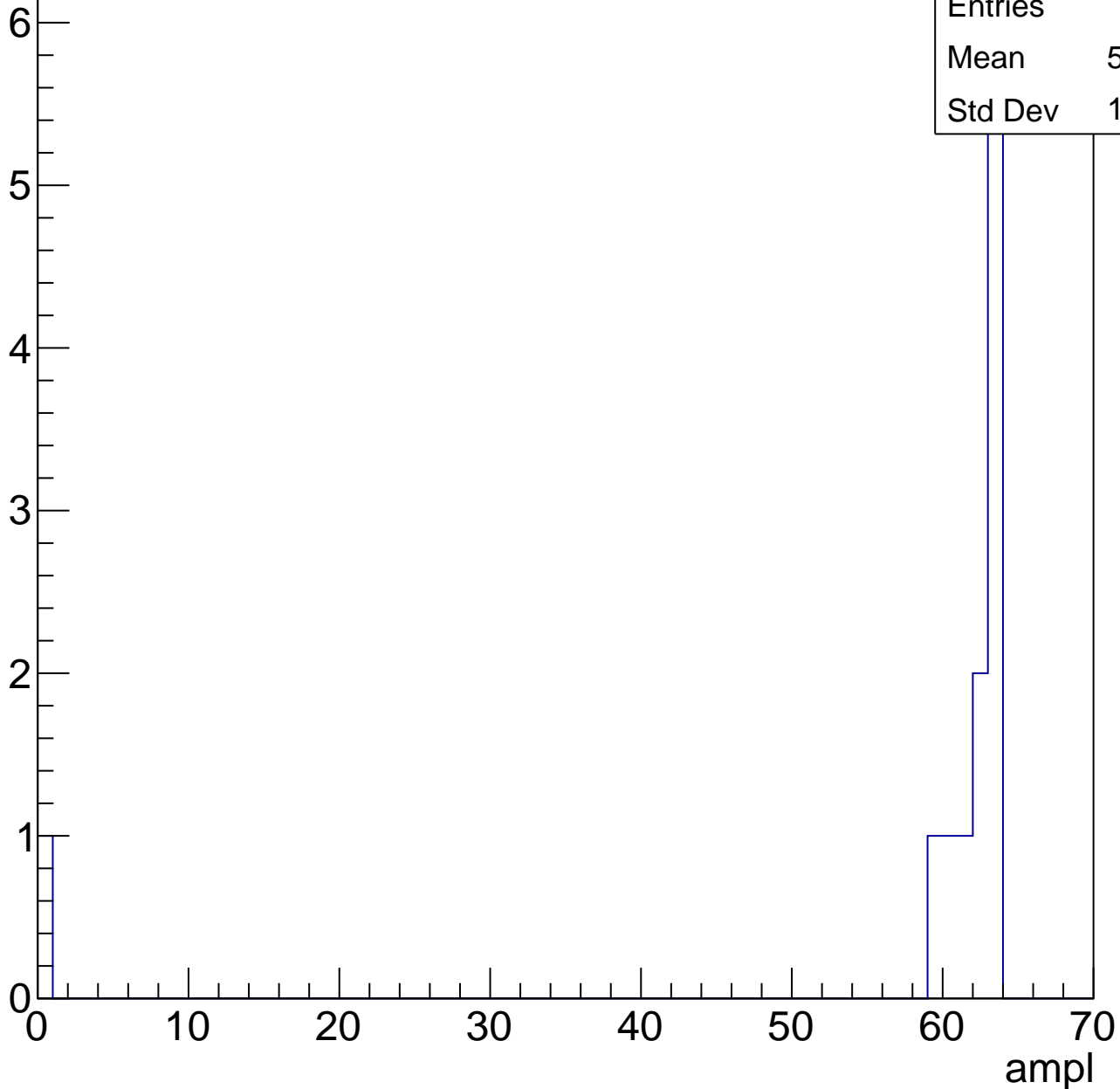


B1L103S, U23-ch53, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	12
Mean	56.83
Std Dev	17.18



B1L103S, U23-ch53, adc7

calib_packv5_041523_1651.root, FC#0, port C2

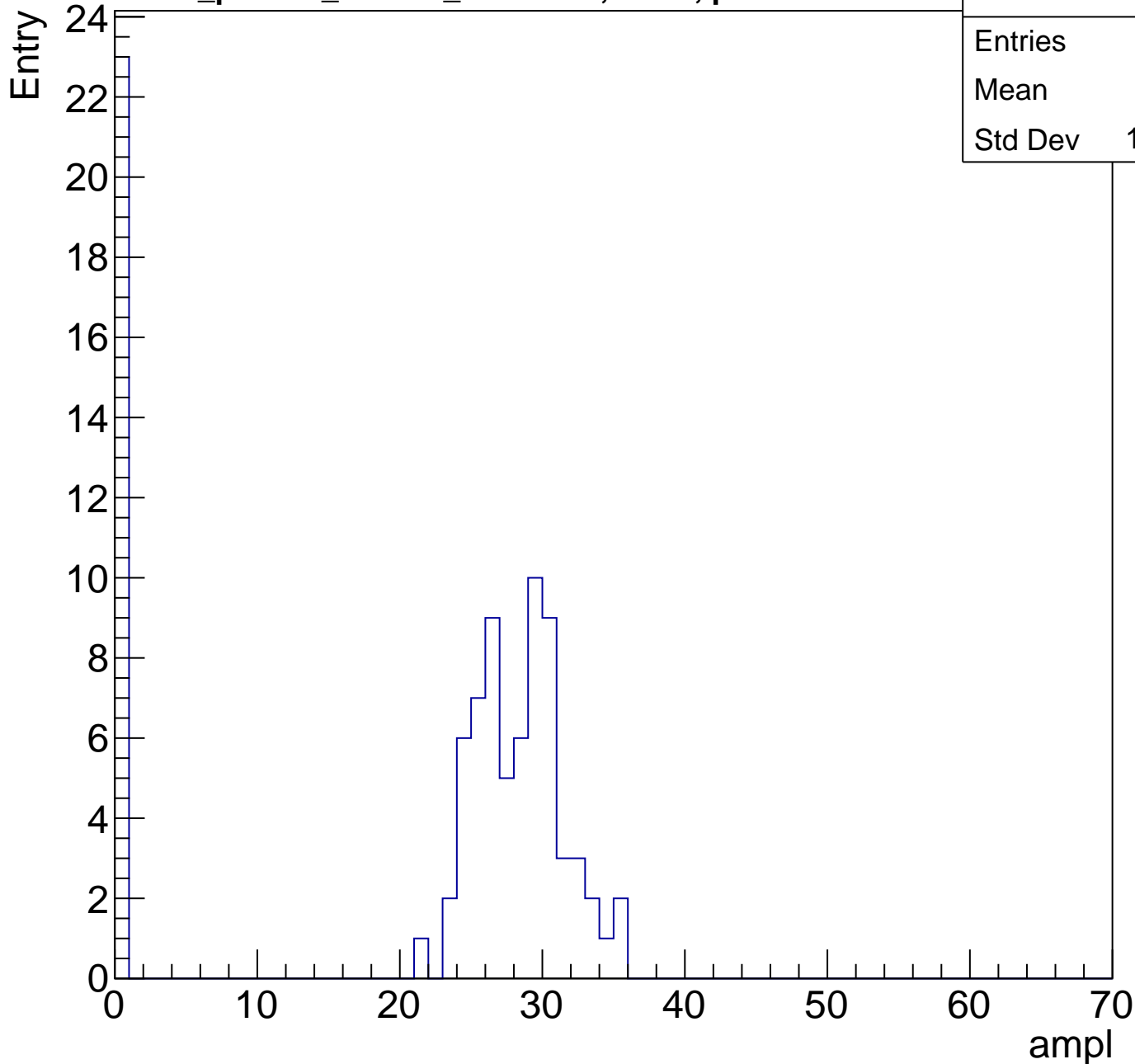
Entry



B1L103S, U23-ch54, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	89
Mean	20.7
Std Dev	12.49

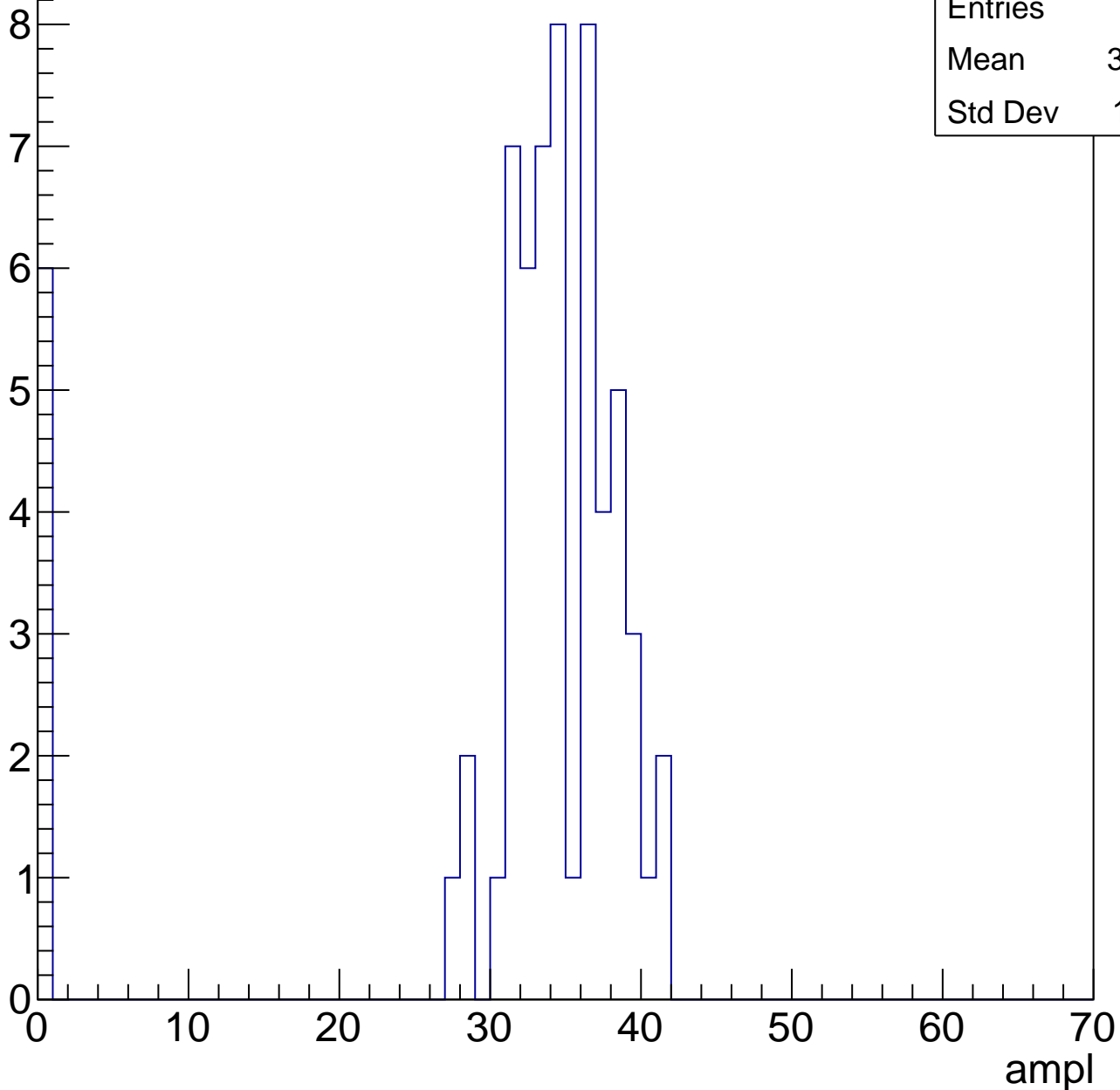


B1L103S, U23-ch54, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	31.05
Std Dev	10.61



B1L103S, U23-ch54, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	74
Mean	33.86
Std Dev	14.51

Entry

10

8

6

4

2

0

0

10

20

30

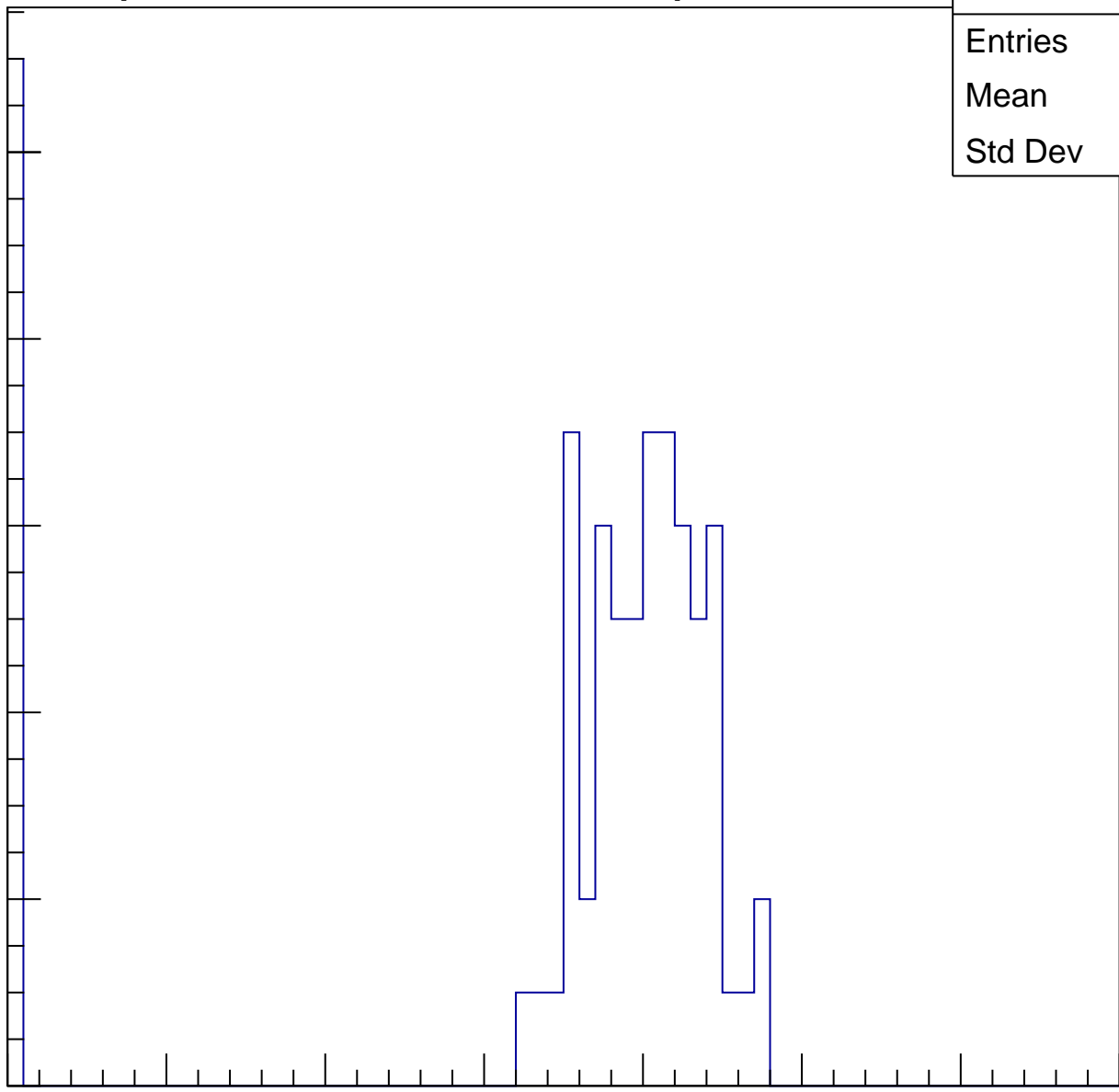
40

50

60

70

ampl

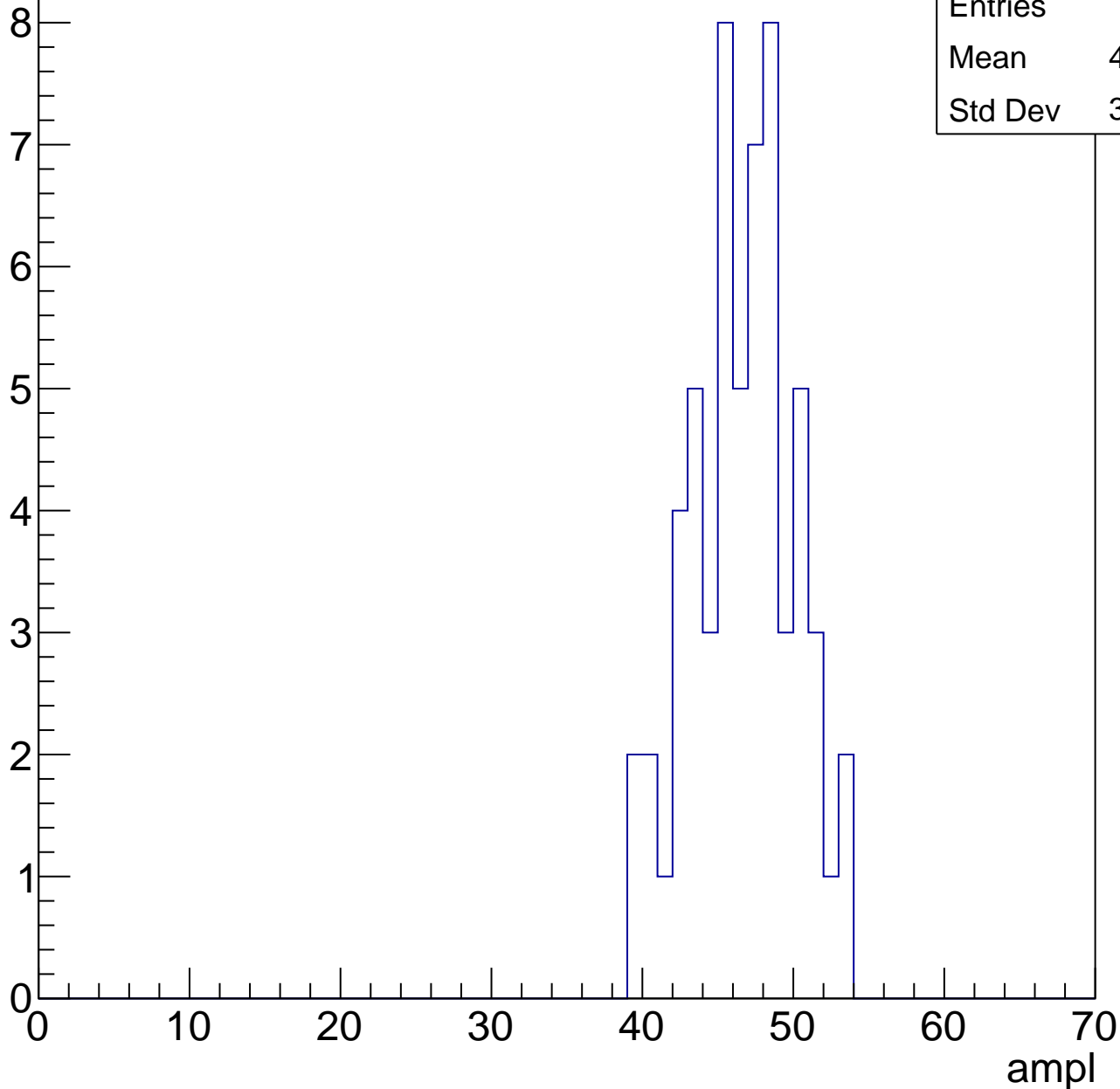


B1L103S, U23-ch54, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	46.19
Std Dev	3.387

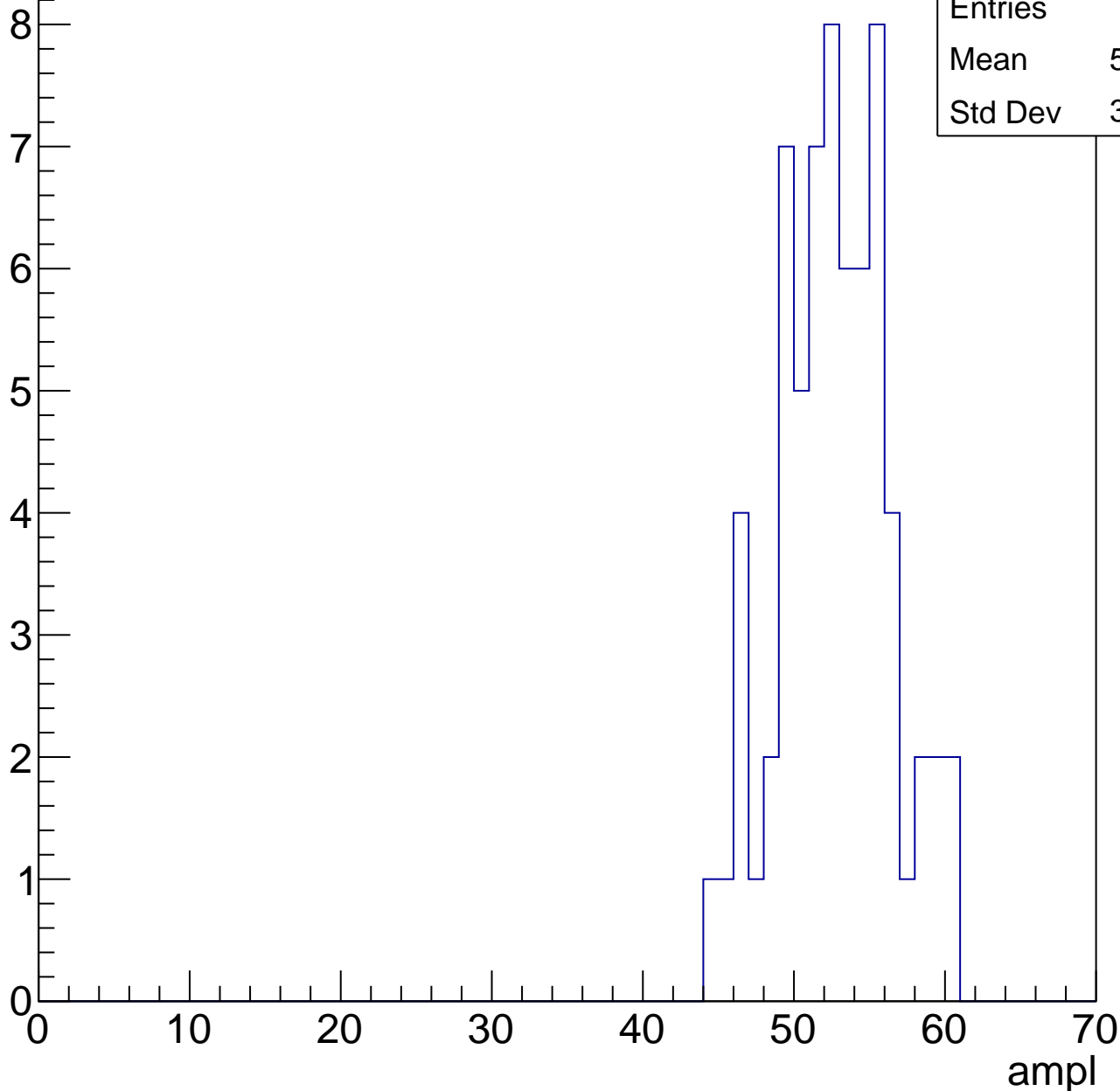


B1L103S, U23-ch54, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

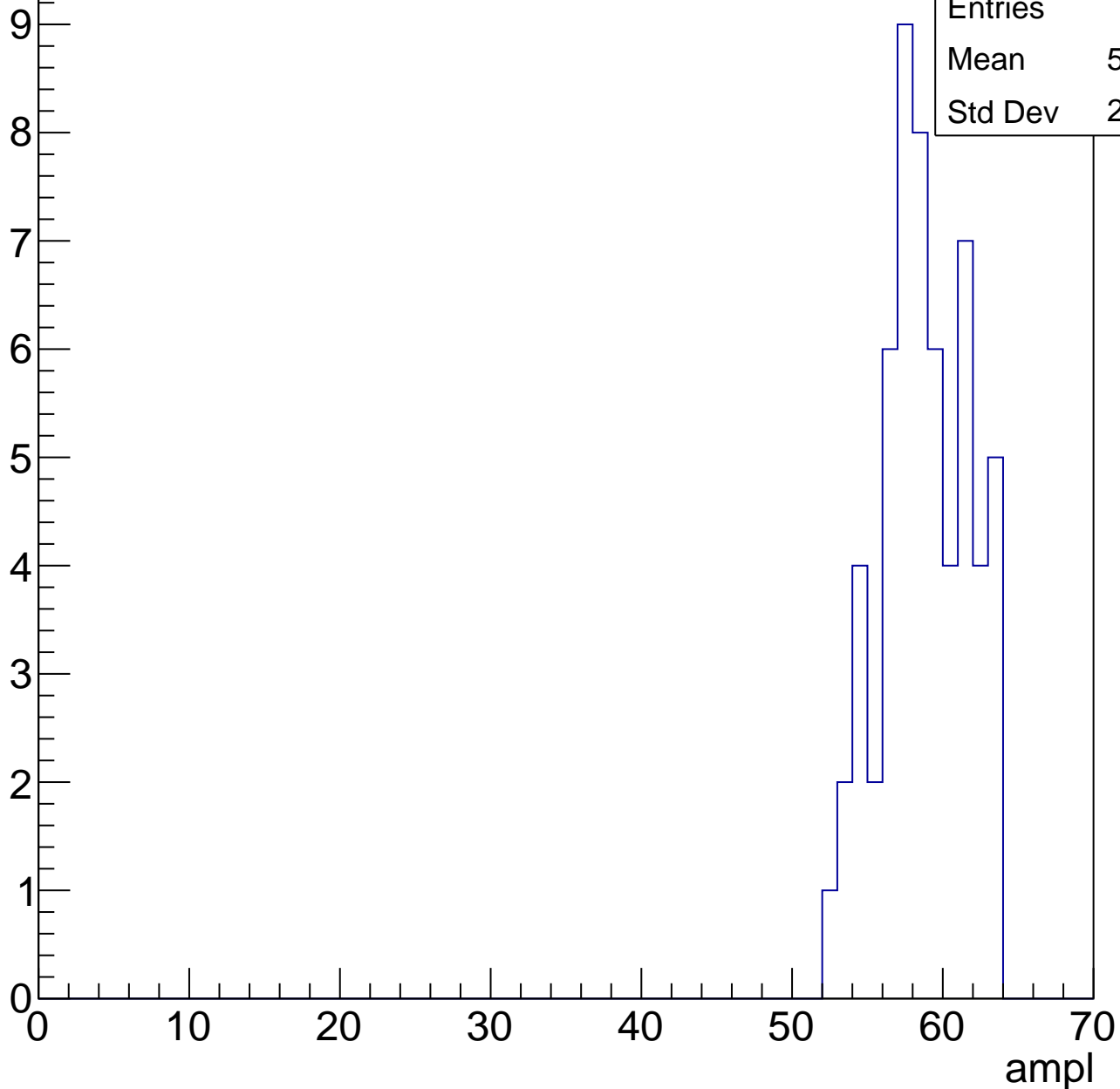
Entries	67
Mean	52.22
Std Dev	3.644



B1L103S, U23-ch54, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



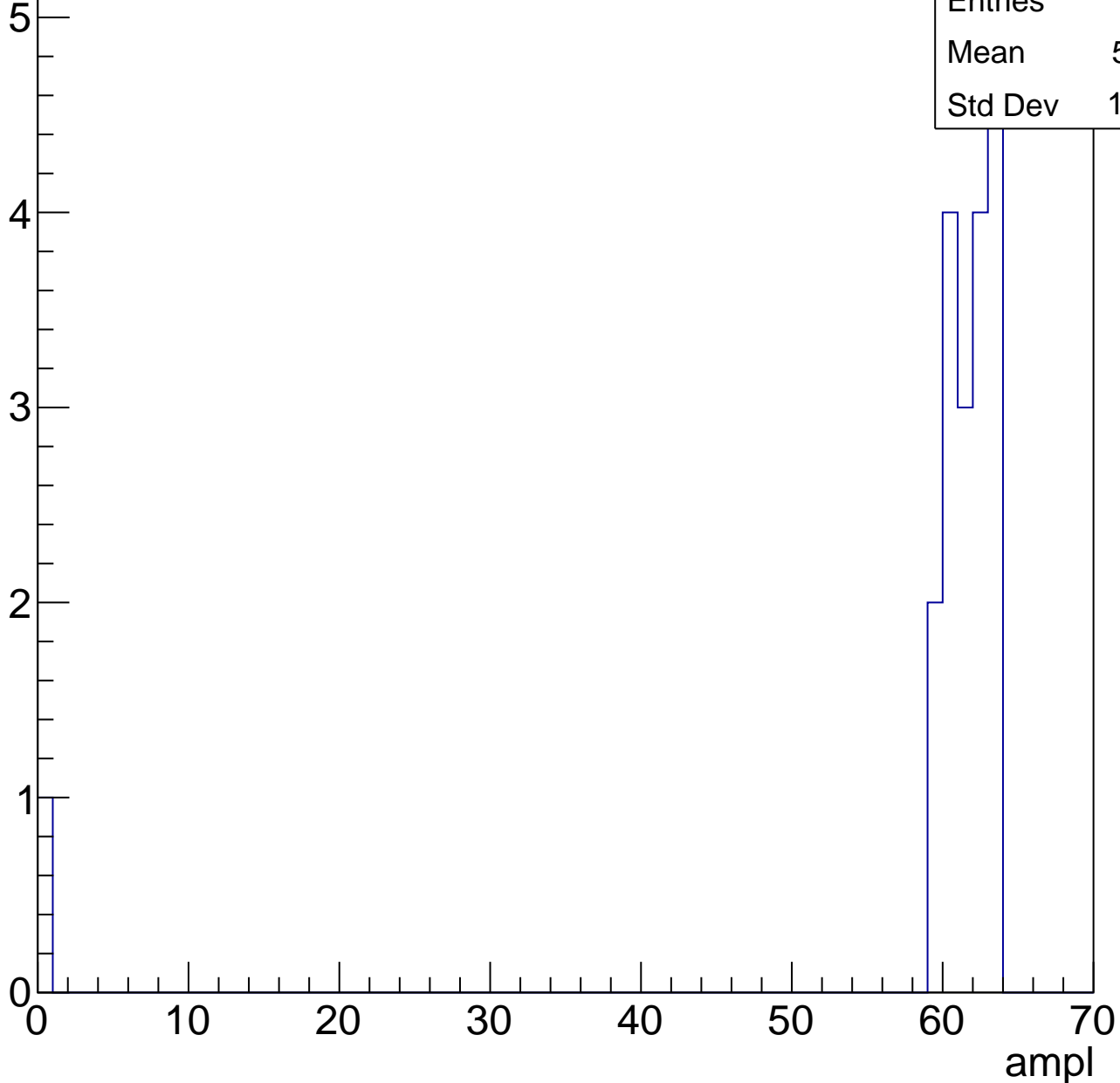
Entries	58
Mean	58.29
Std Dev	2.847

B1L103S, U23-ch54, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	19
Mean	58.11
Std Dev	13.76

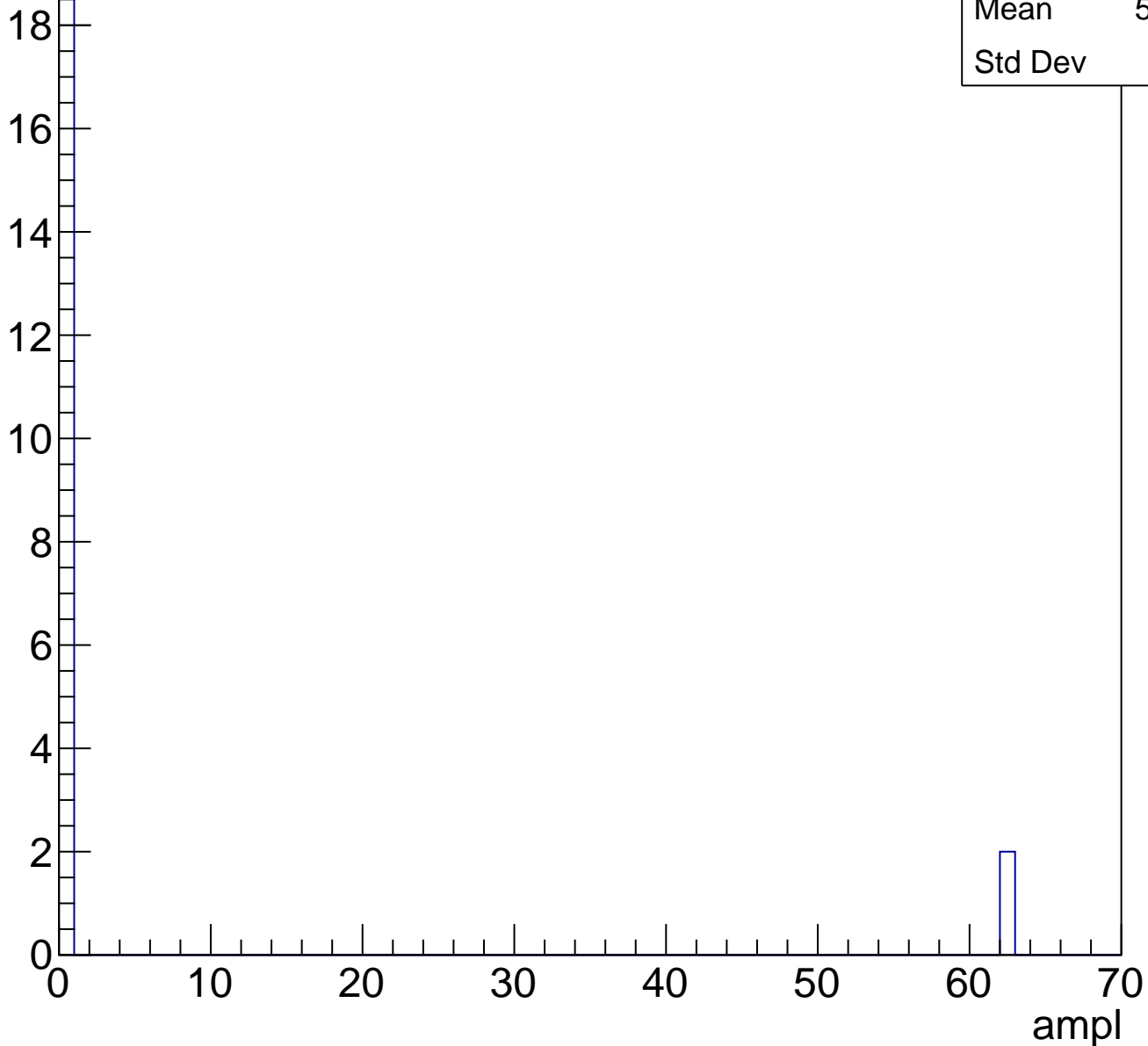


B1L103S, U23-ch54, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	21
Mean	5.905
Std Dev	18.2

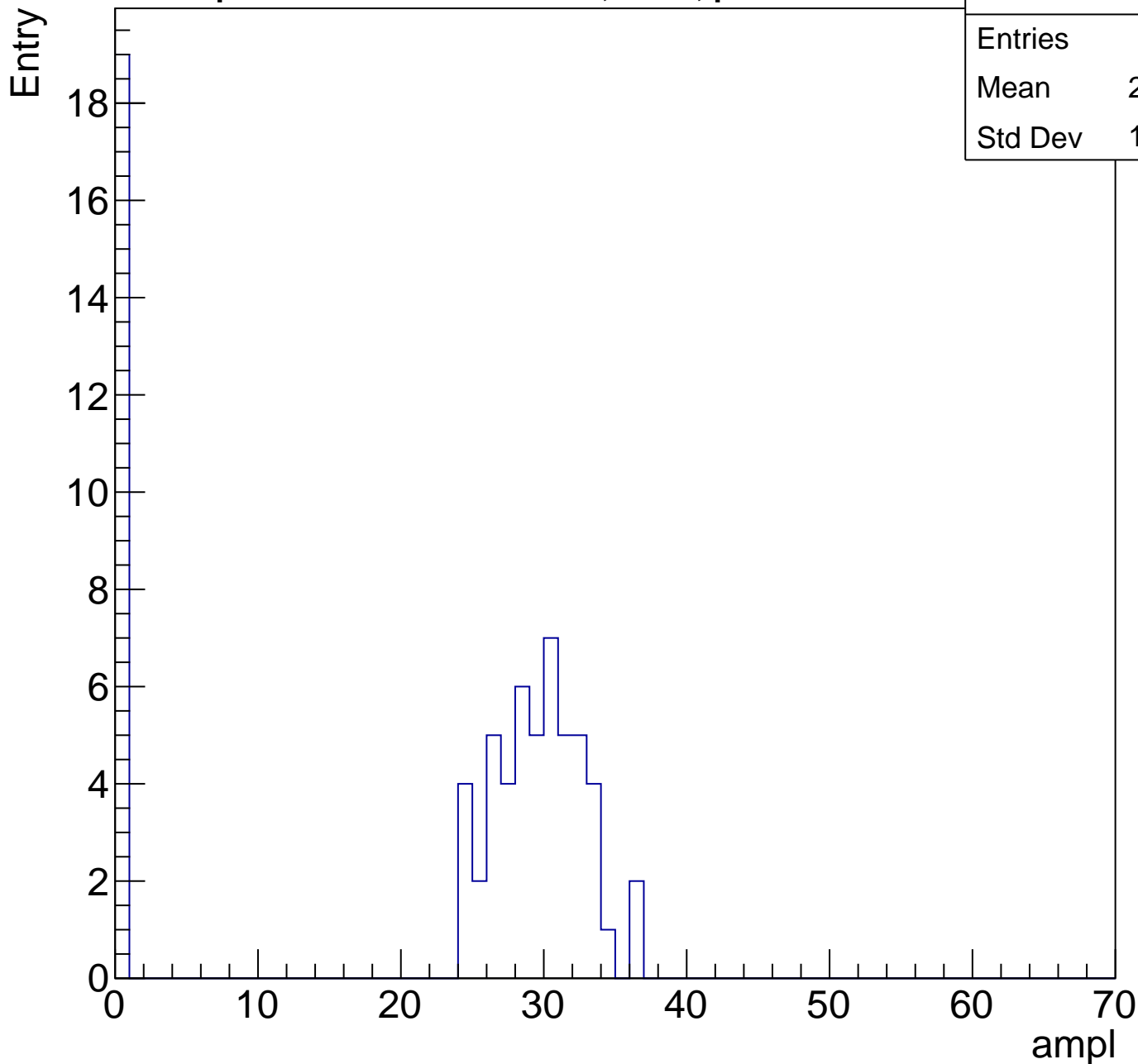
Entry



B1L103S, U23-ch55, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	69
Mean	21.16
Std Dev	13.29

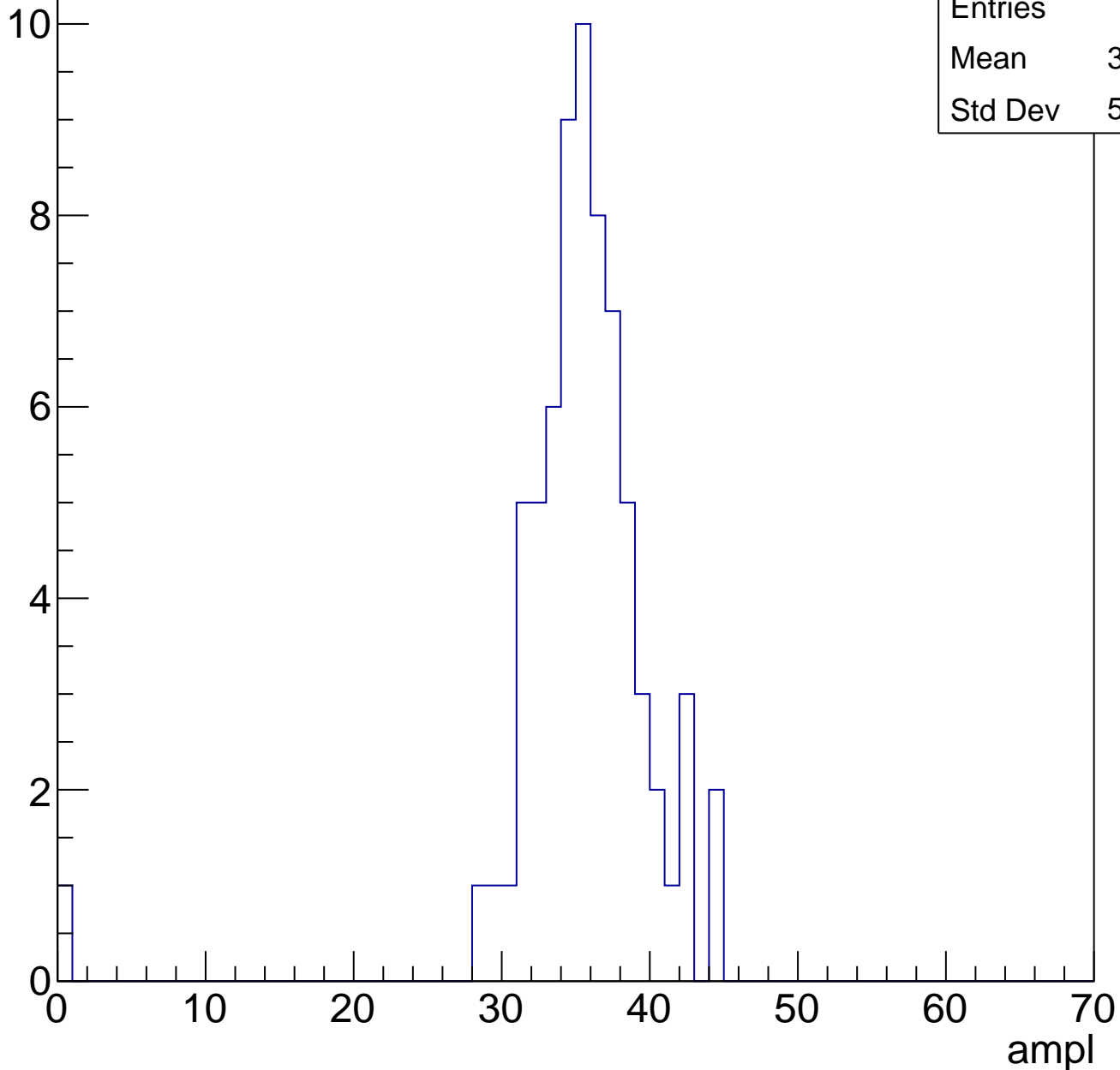


B1L103S, U23-ch55, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	70
Mean	34.93
Std Dev	5.367

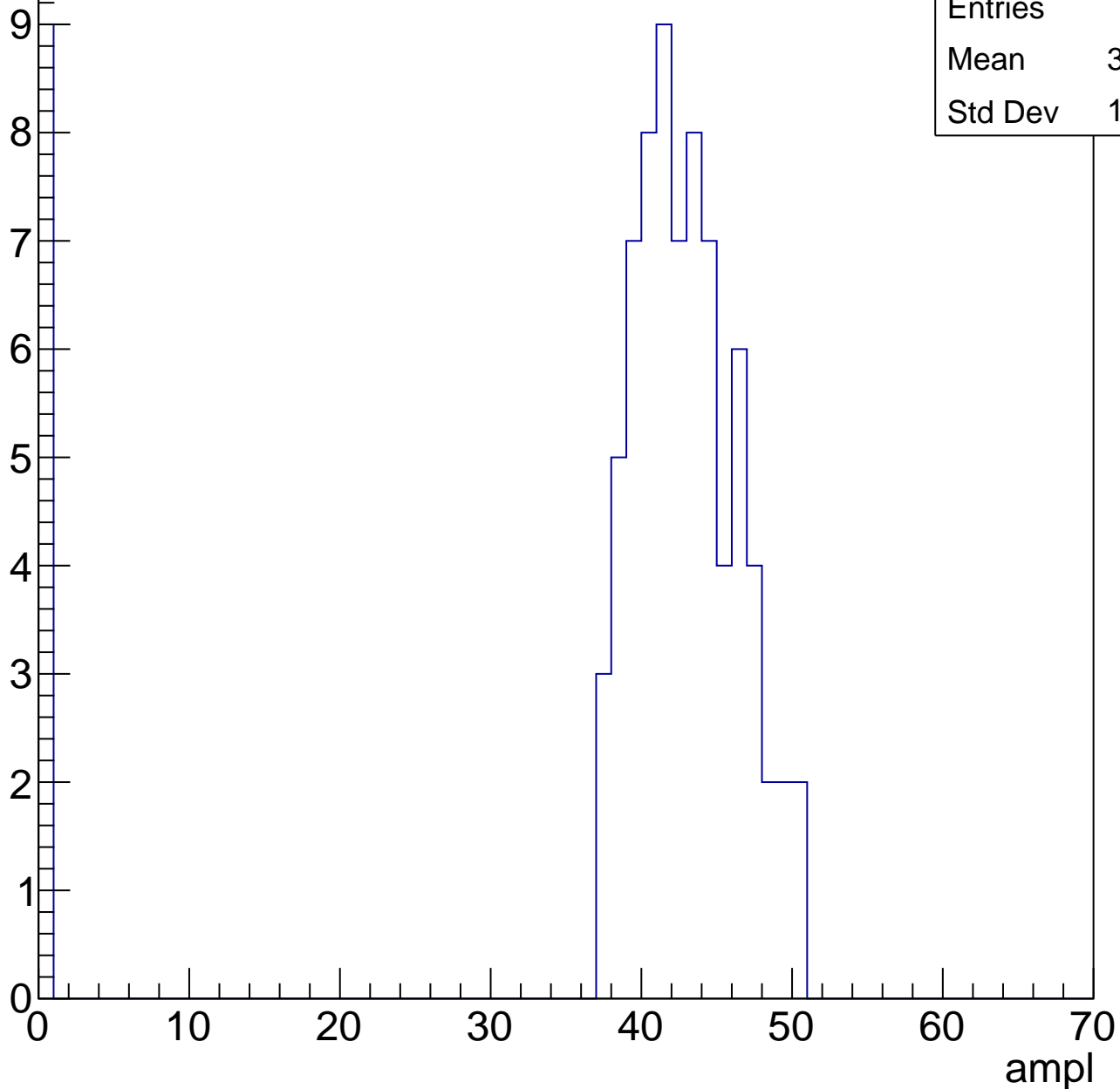
Entry



B1L103S, U23-ch55, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

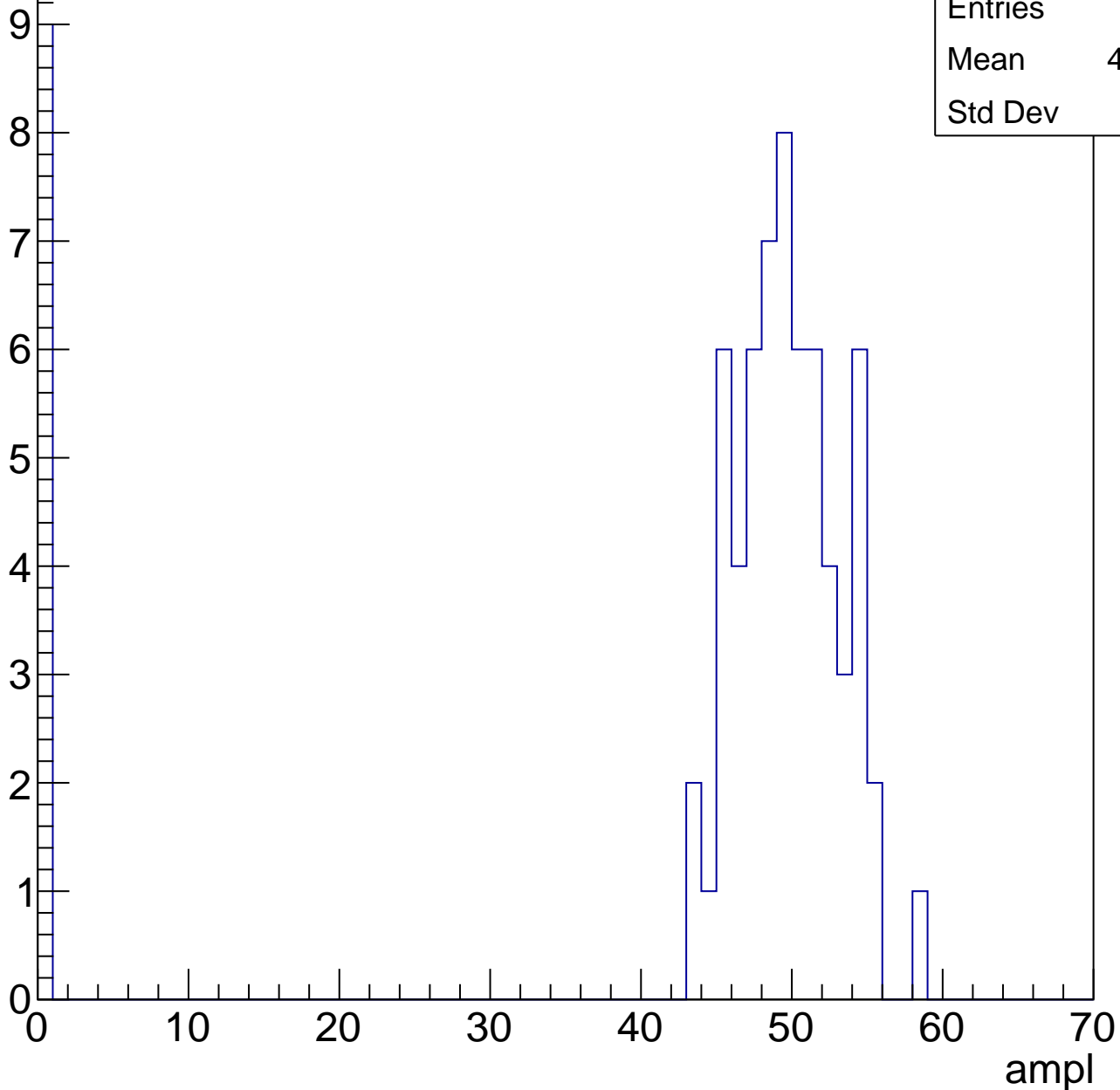


B1L103S, U23-ch55, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	43.08
Std Dev	16.7

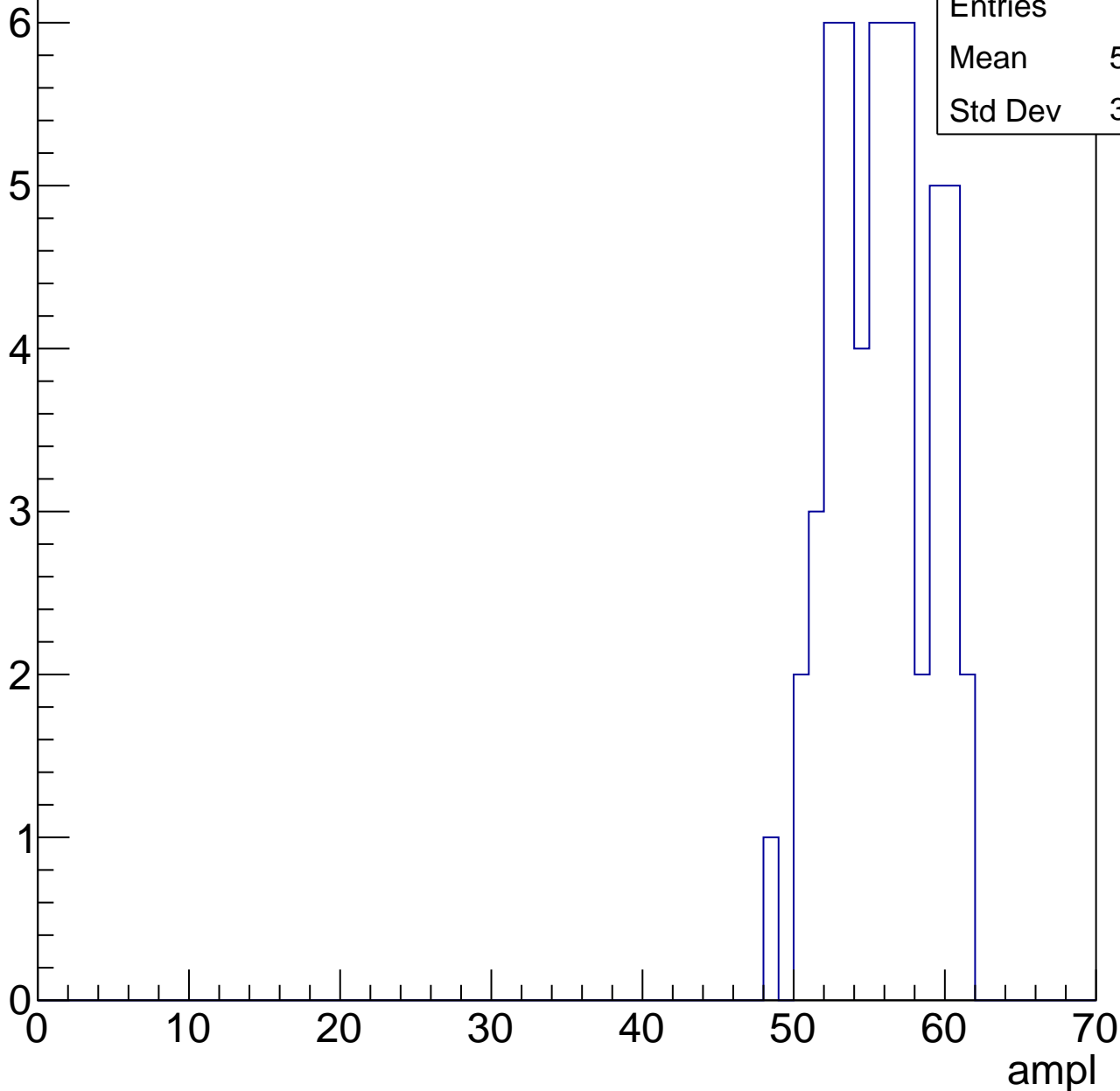


B1L103S, U23-ch55, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	54
Mean	55.33
Std Dev	3.186

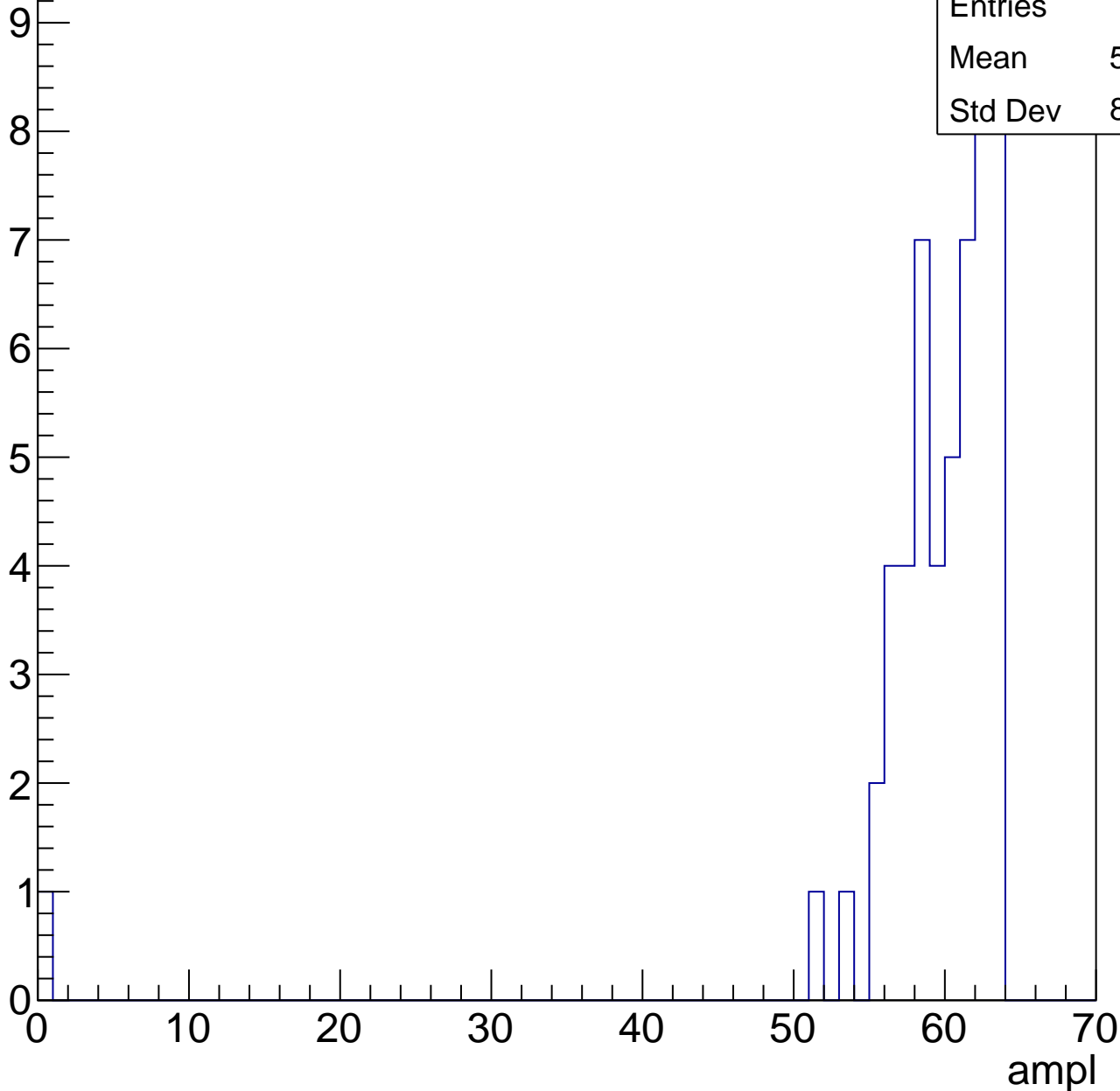


B1L103S, U23-ch55, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

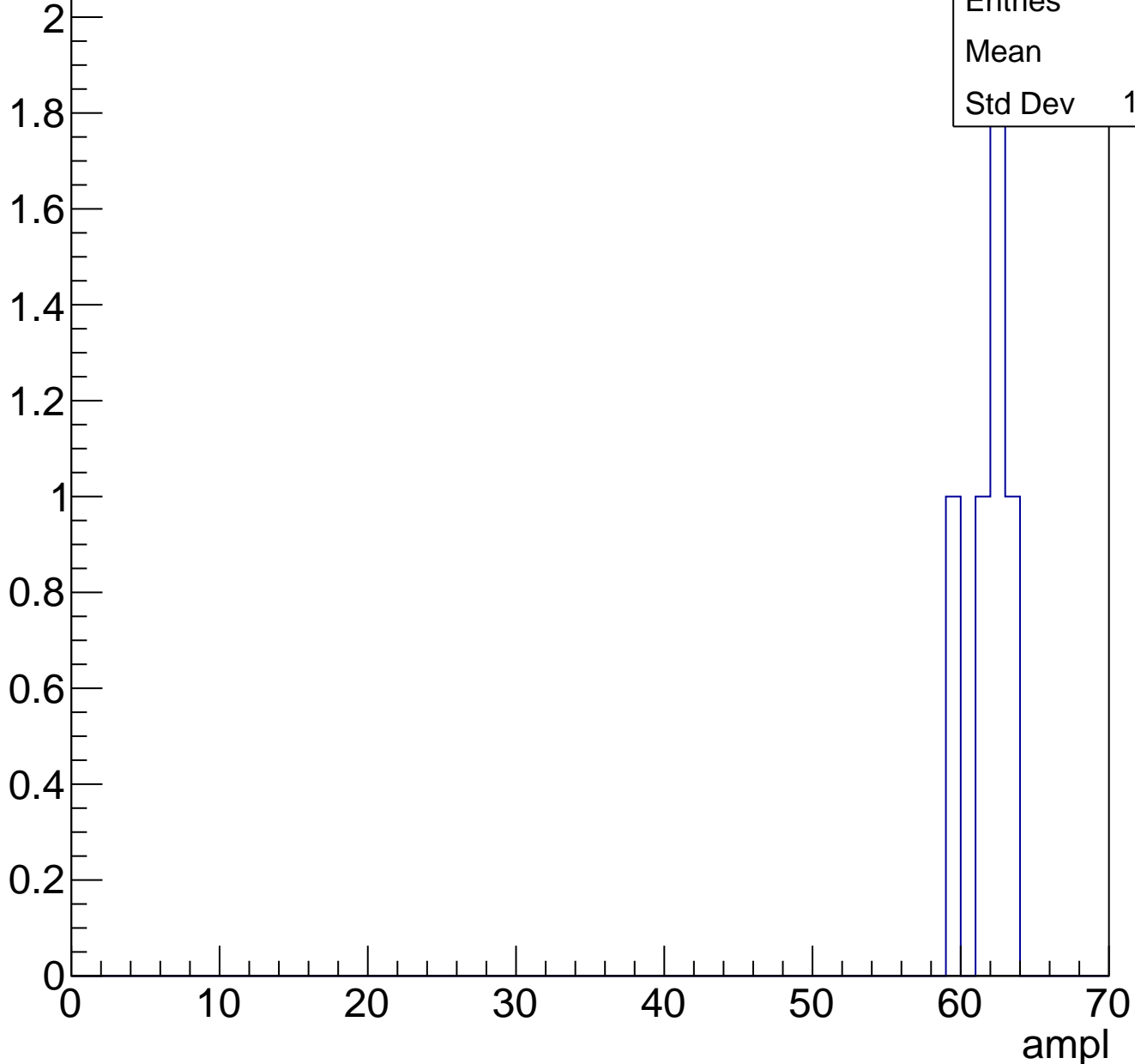
Entries	53
Mean	58.45
Std Dev	8.584



B1L103S, U23-ch55, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch55, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

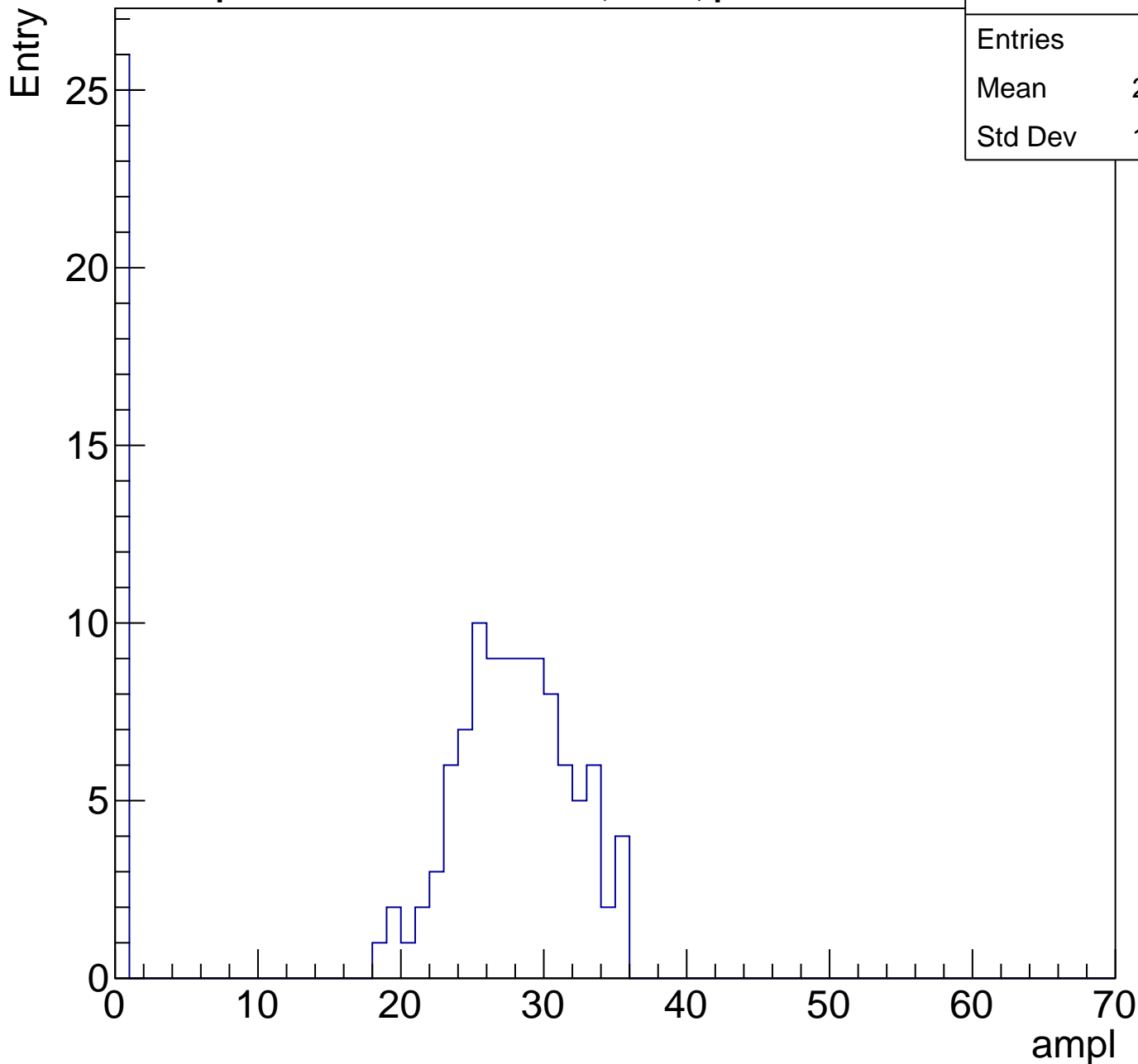
ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U23-ch56, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	125
Mean	21.78
Std Dev	11.68



B1L103S, U23-ch56, adc1

calib_packv5_041523_1651.root, FC#0, port C2

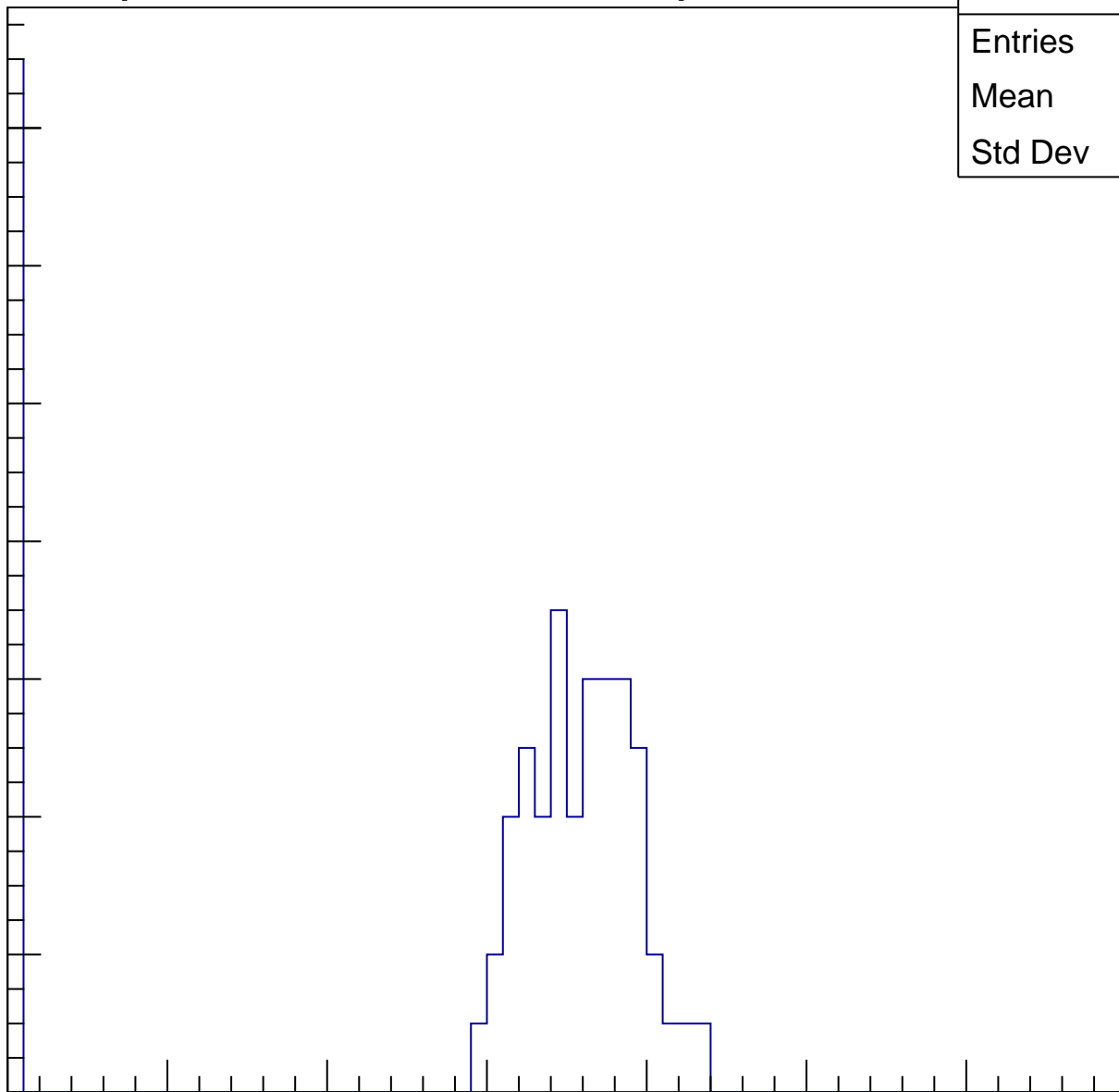
Entries	70
Mean	27.86
Std Dev	14.82

Entry

14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

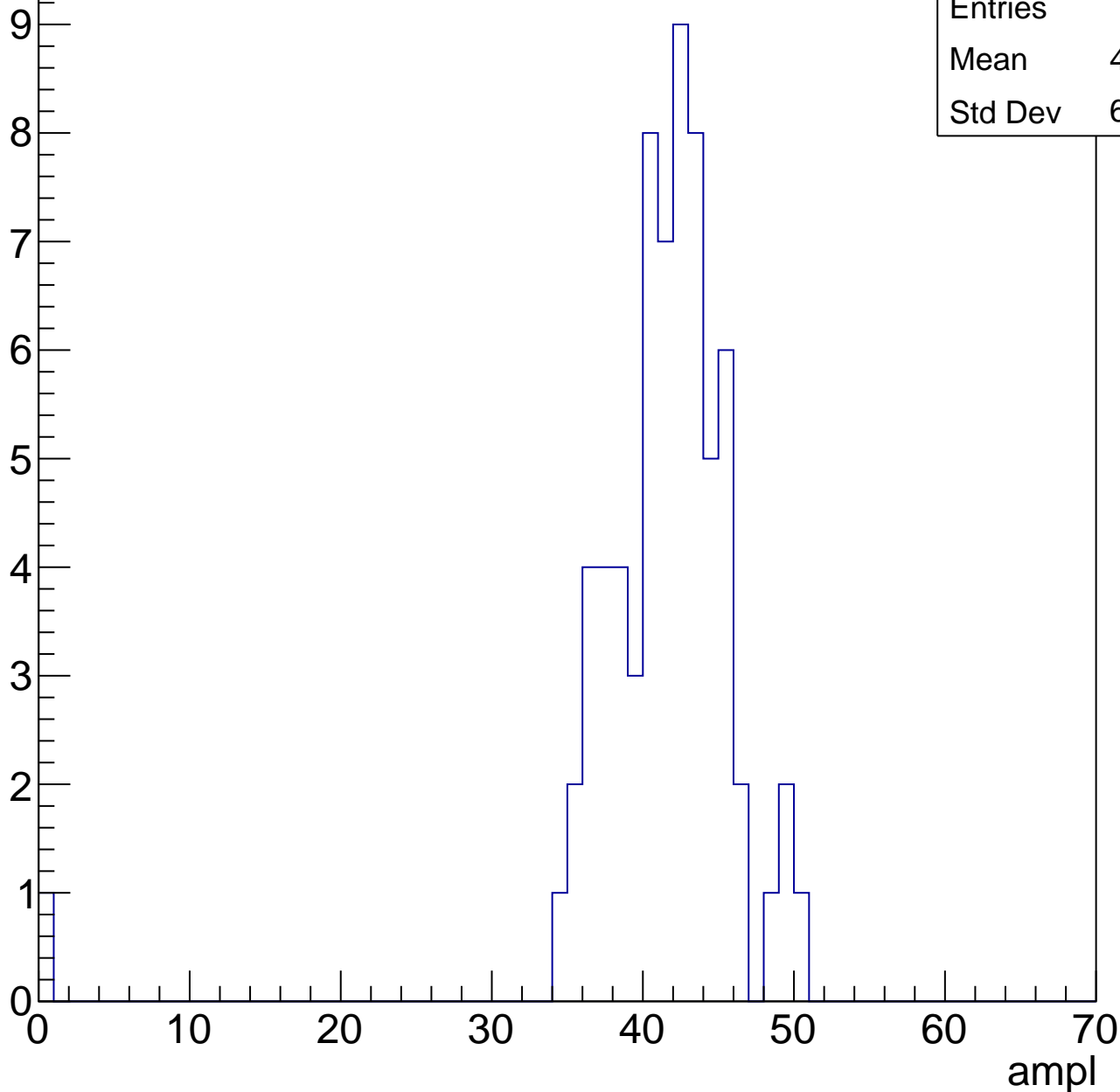


B1L103S, U23-ch56, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	40.76
Std Dev	6.073

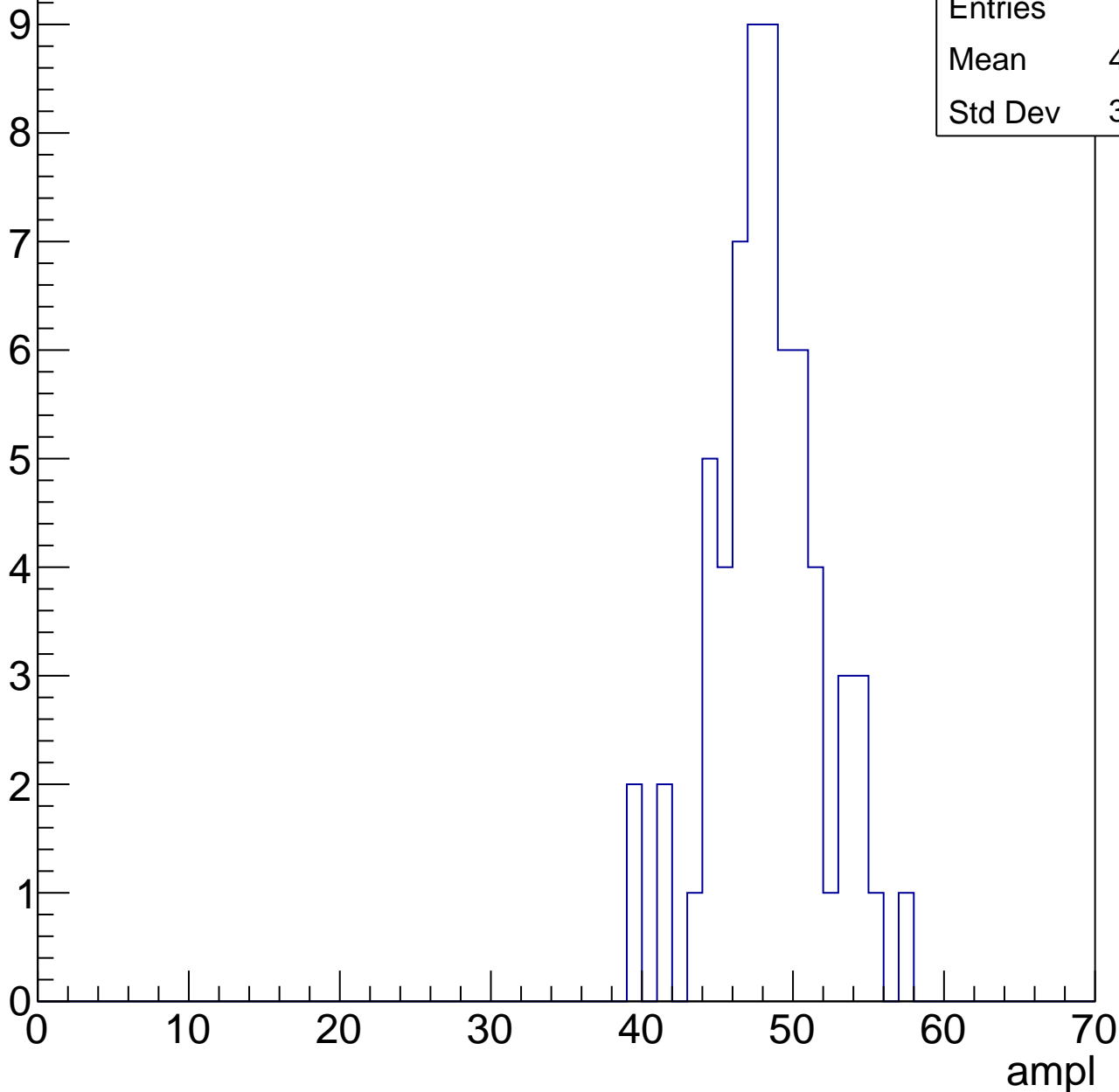


B1L103S, U23-ch56, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	47.86
Std Dev	3.605

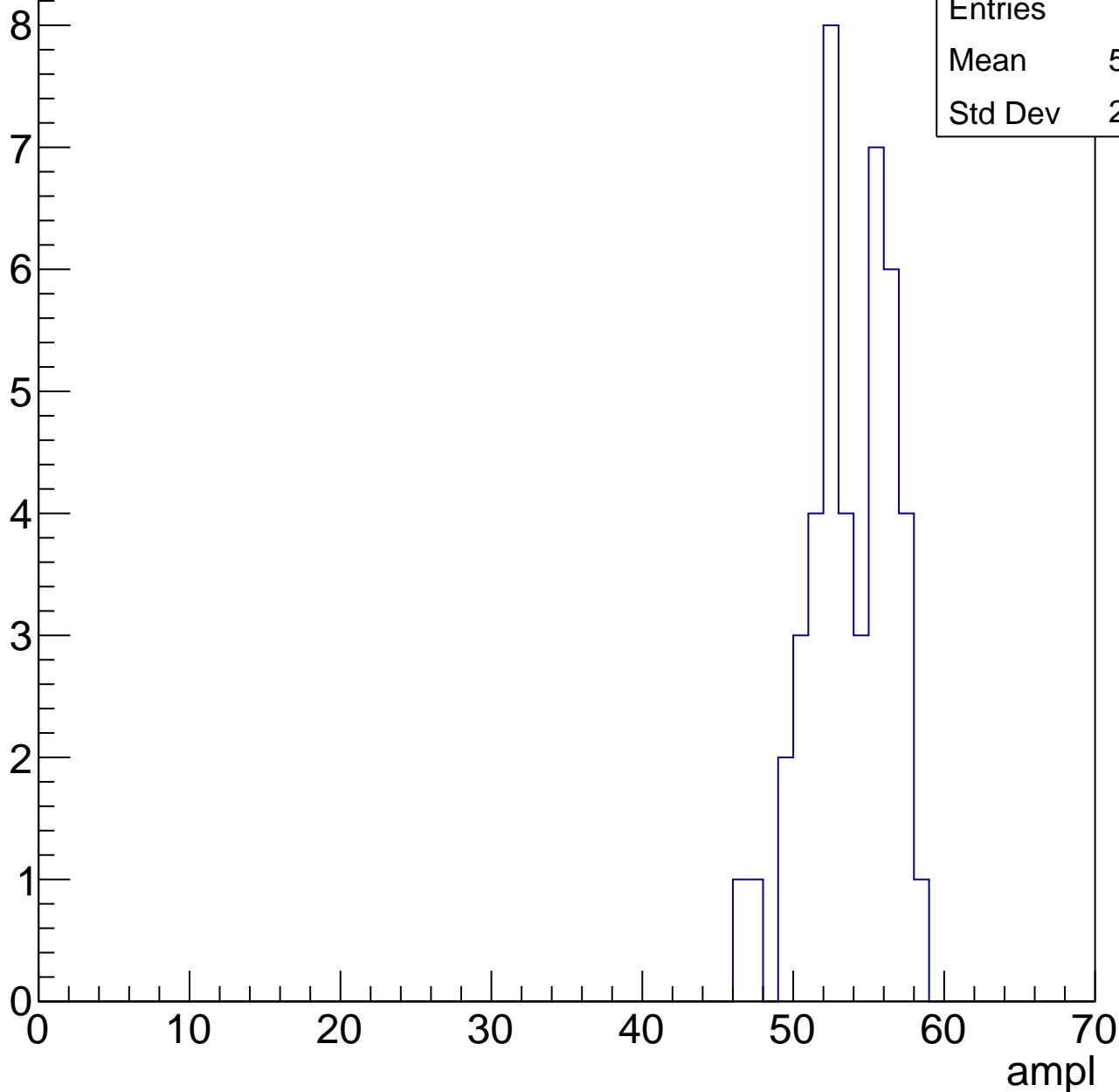


B1L103S, U23-ch56, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	44
Mean	53.23
Std Dev	2.779



B1L103S, U23-ch56, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

10

Entries 67

Mean 57.57

Std Dev 7.716

8

6

4

2

0

0

10

20

30

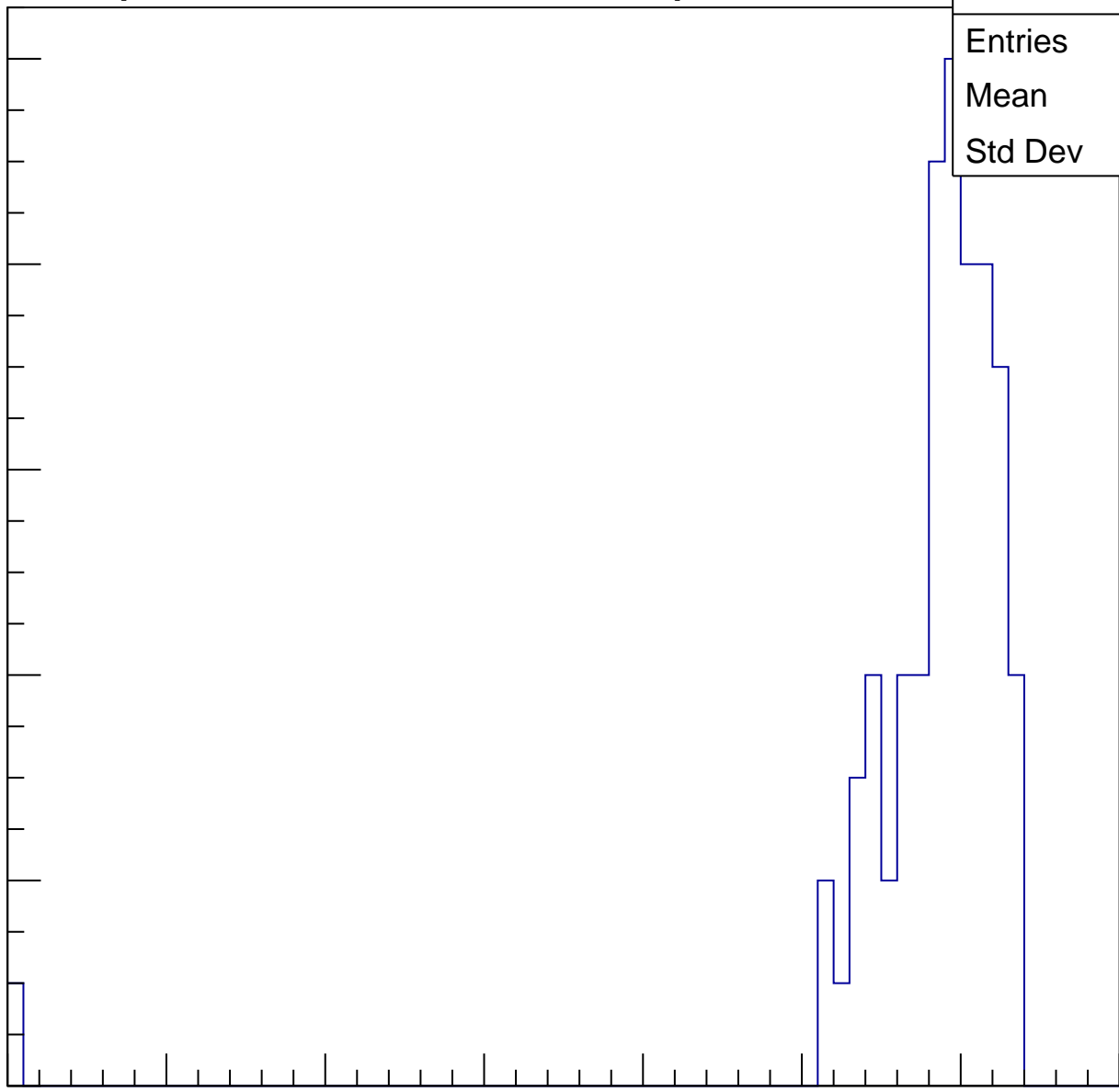
40

50

60

70

ampl

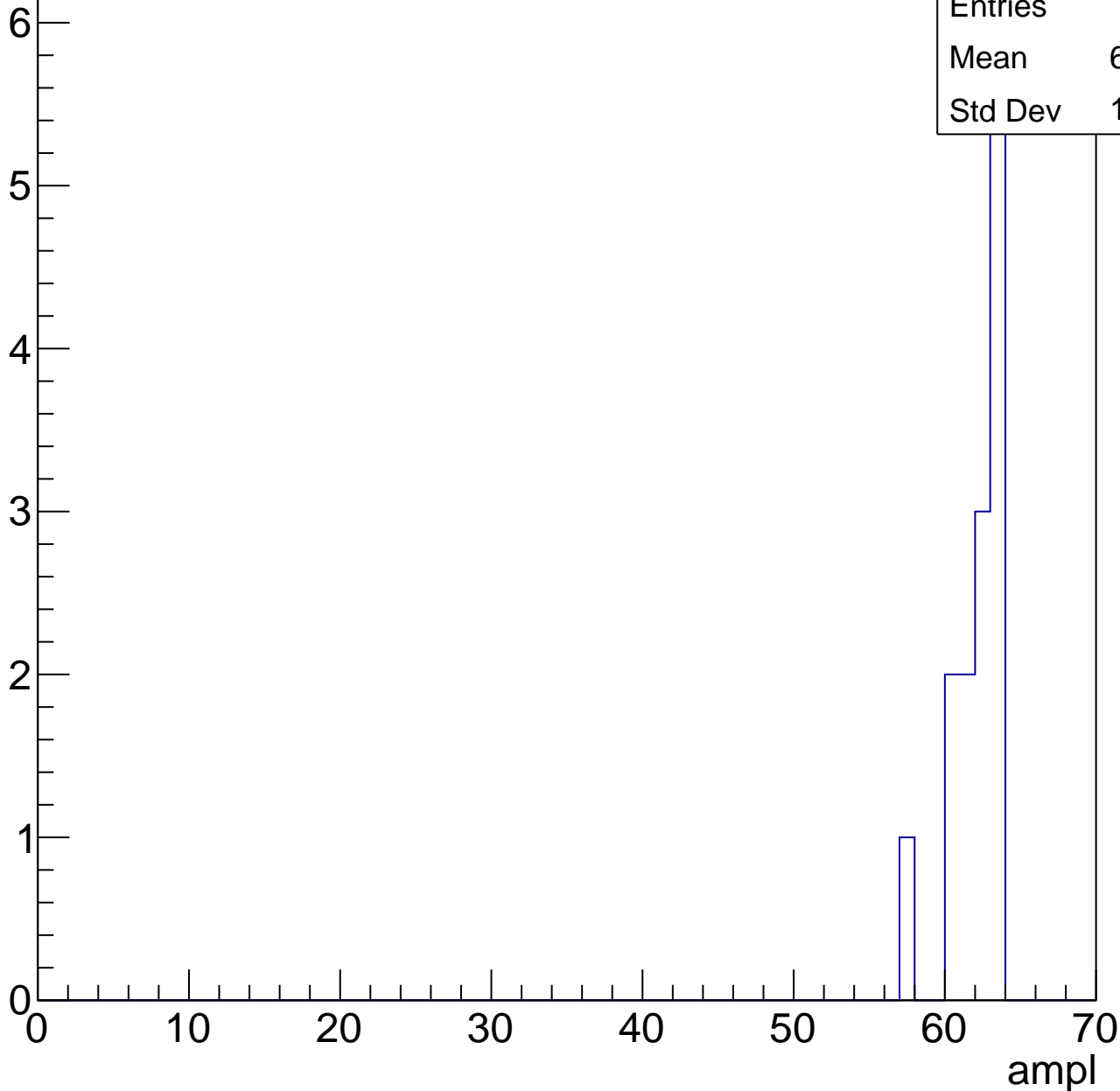


B1L103S, U23-ch56, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	14
Mean	61.64
Std Dev	1.674



B1L103S, U23-ch56, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

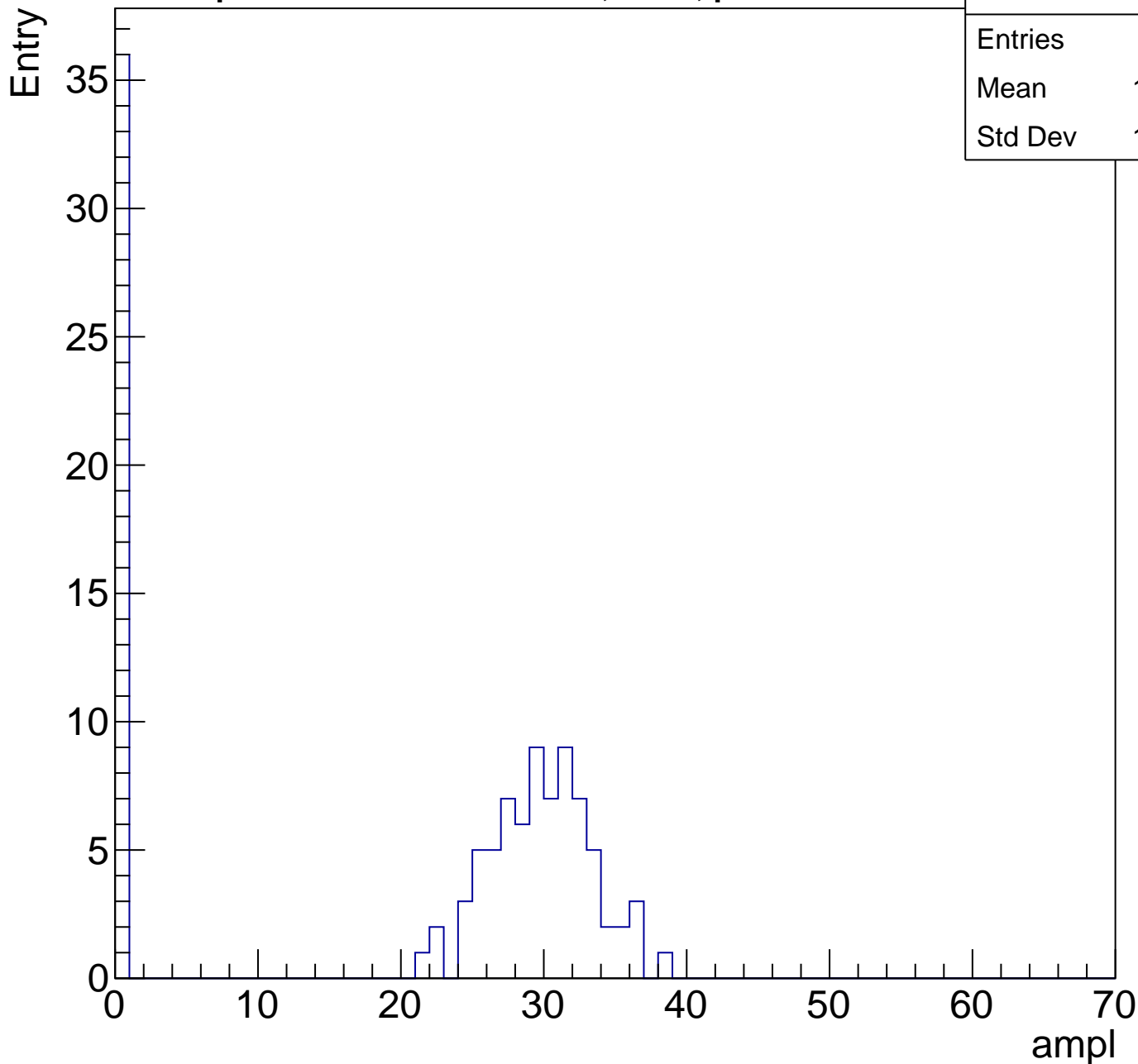
ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U23-ch57, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	110
Mean	19.75
Std Dev	14.07

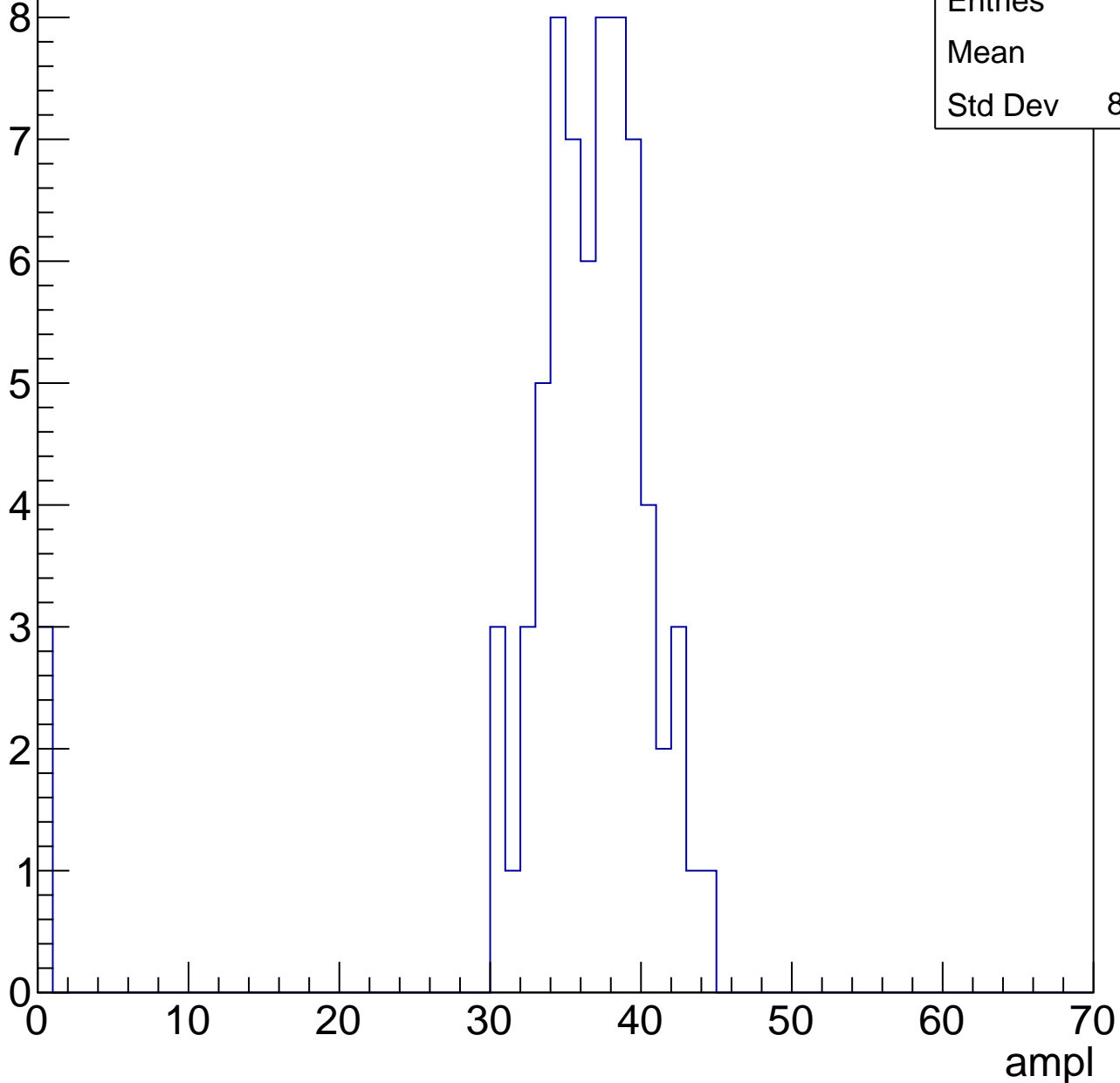


B1L103S, U23-ch57, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	34.9
Std Dev	8.023

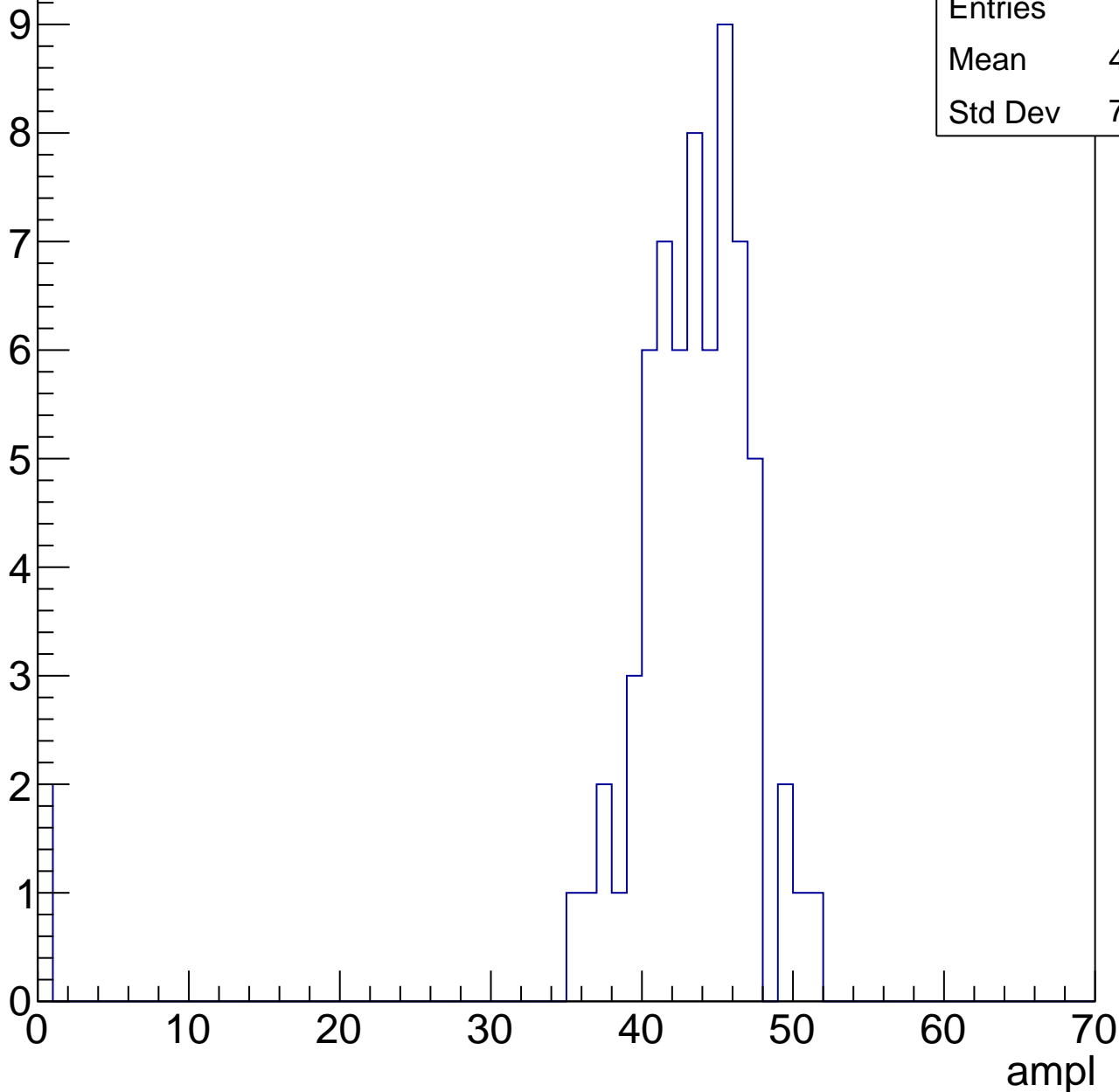


B1L103S, U23-ch57, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	41.88
Std Dev	7.979



B1L103S, U23-ch57, adc3

calib_packv5_041523_1651.root, FC#0, port C2

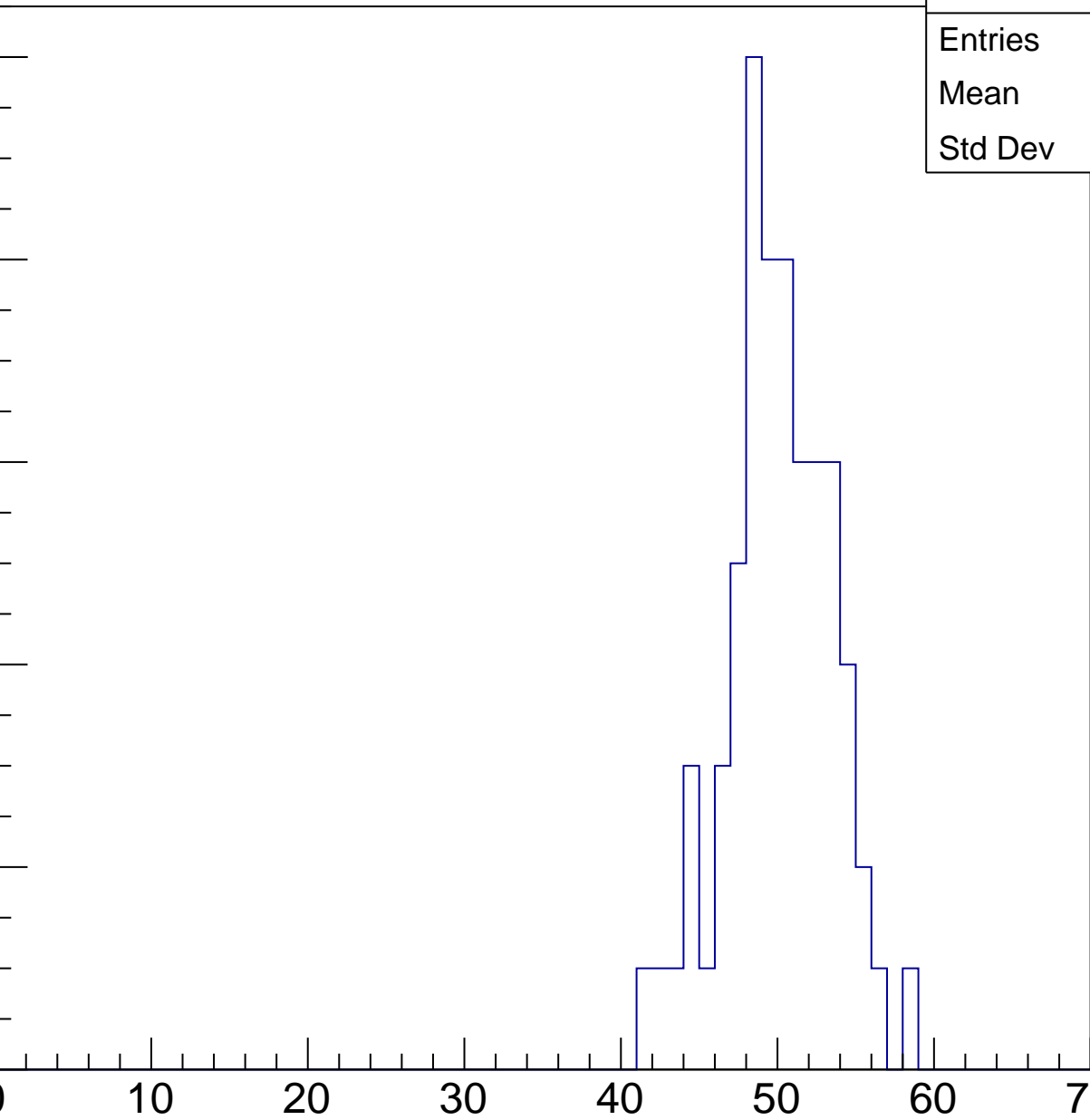
Entries	67
Mean	49.61
Std Dev	3.359

Entry

10
8
6
4
2
0

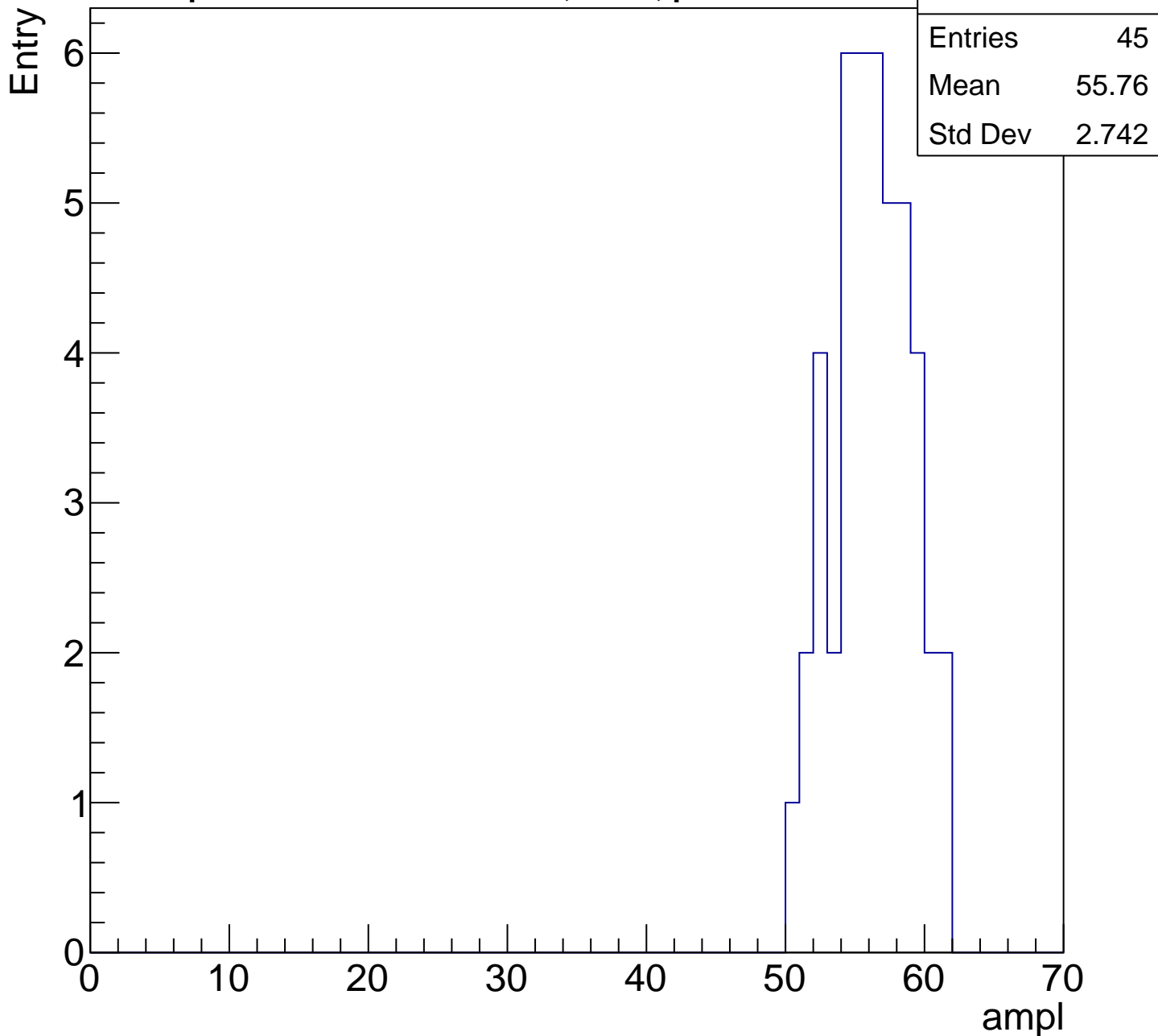
0 10 20 30 40 50 60 70

ampl



B1L103S, U23-ch57, adc4

calib_packv5_041523_1651.root, FC#0, port C2

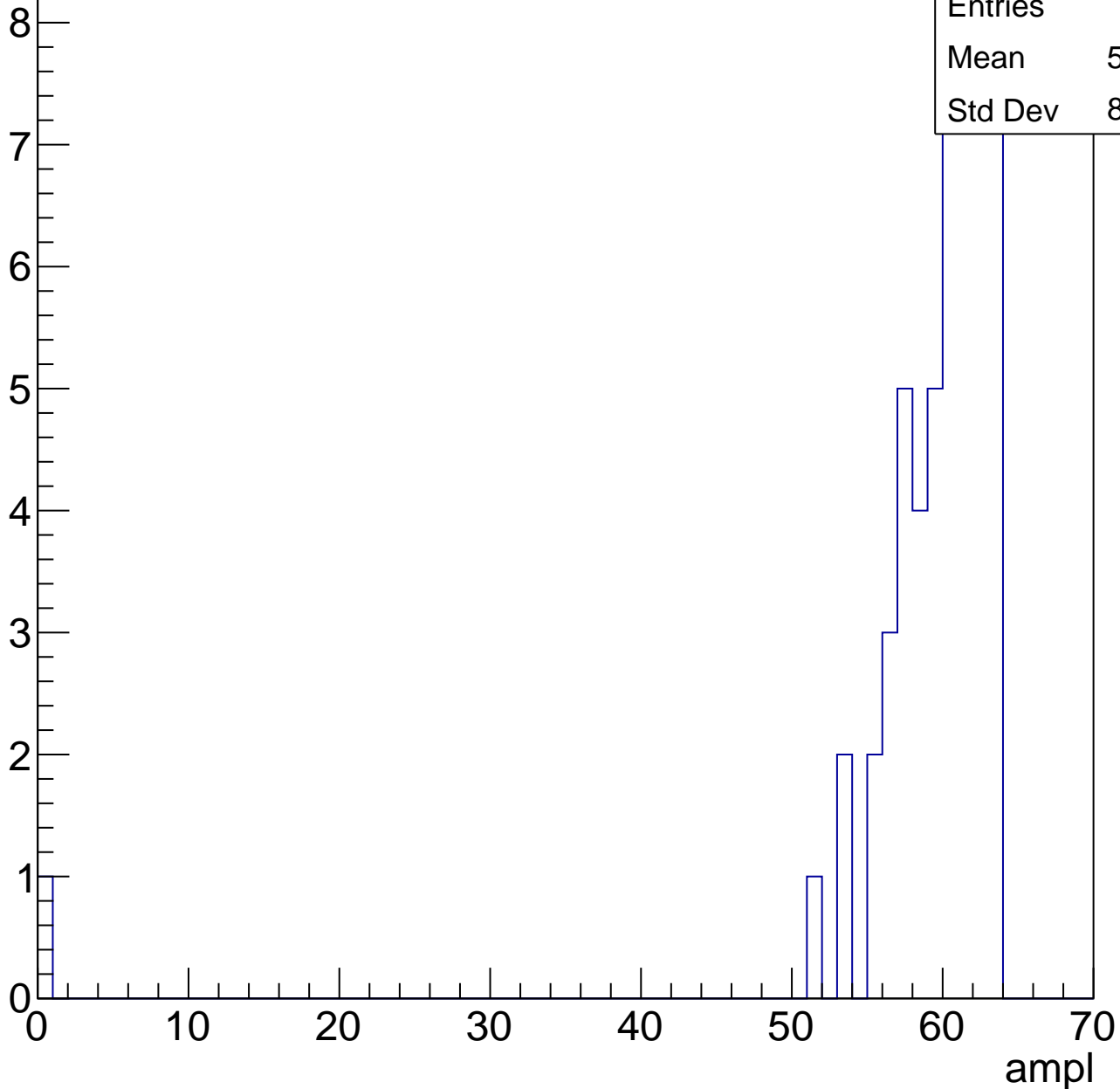


B1L103S, U23-ch57, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	58.45
Std Dev	8.446



B1L103S, U23-ch57, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch57, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U23-ch58, adc0

calib_packv5_041523_1651.root, FC#0, port C2

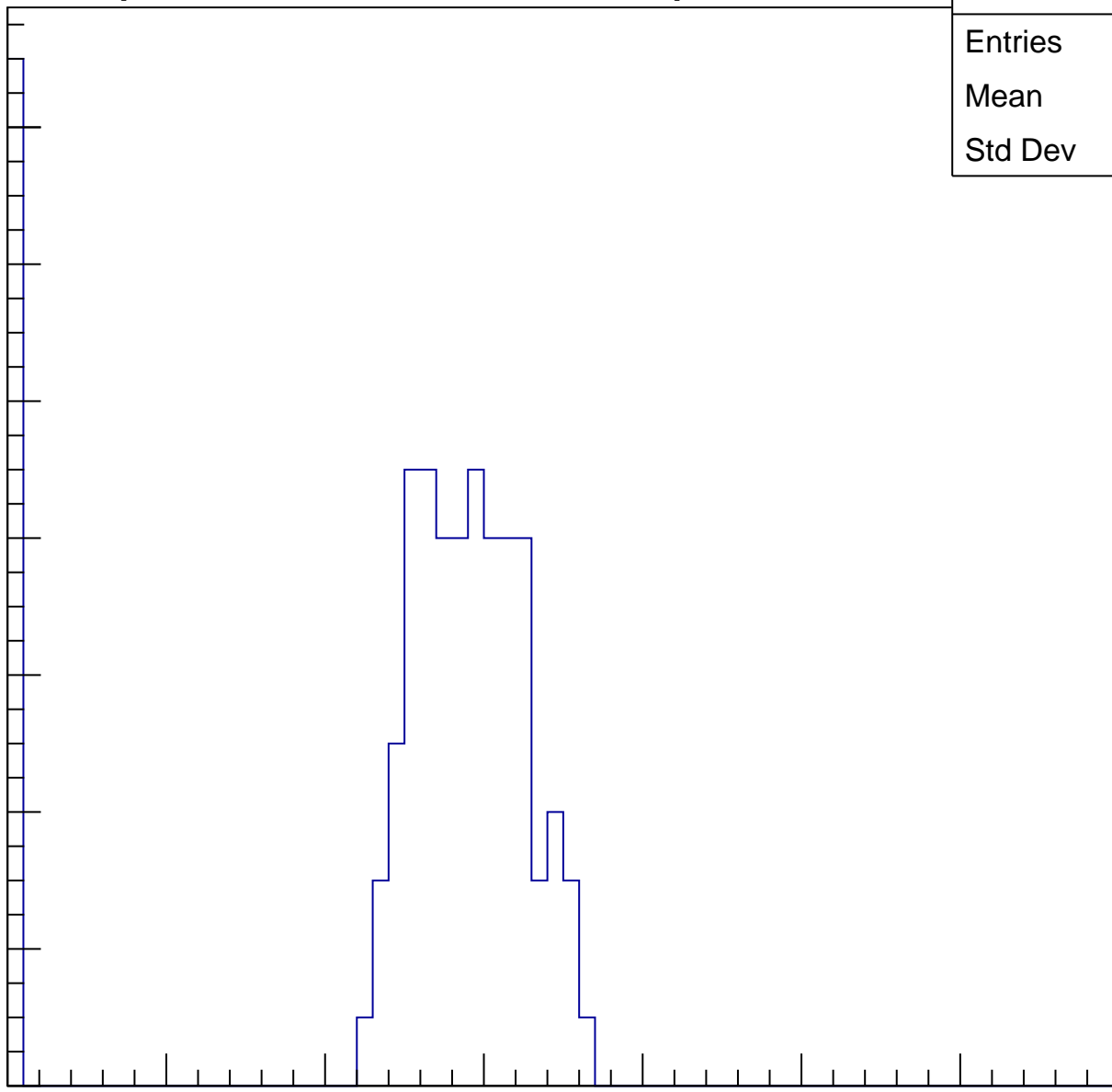
Entries	102
Mean	24.42
Std Dev	10.59

Entry

14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

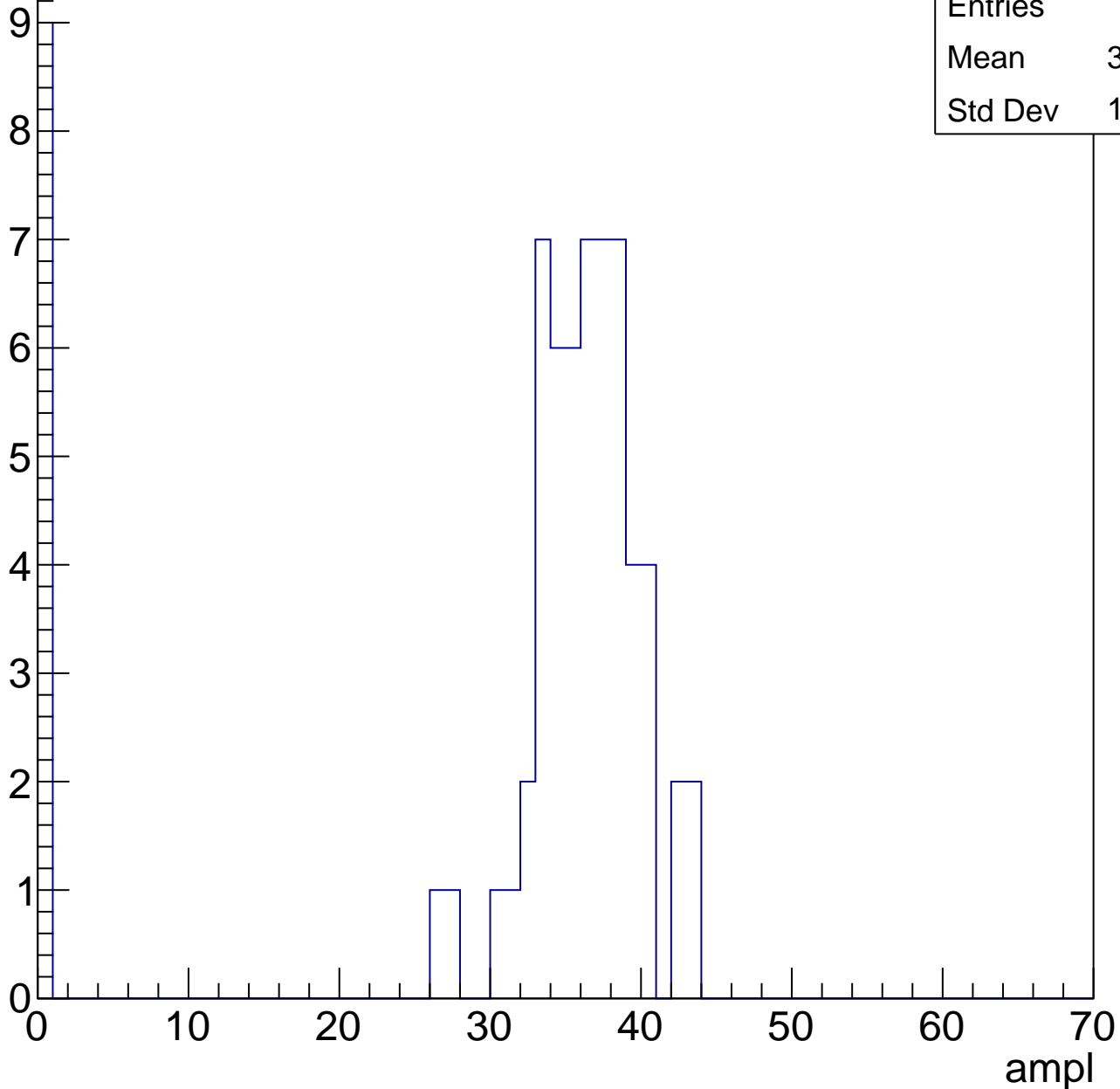


B1L103S, U23-ch58, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	31.13
Std Dev	12.67

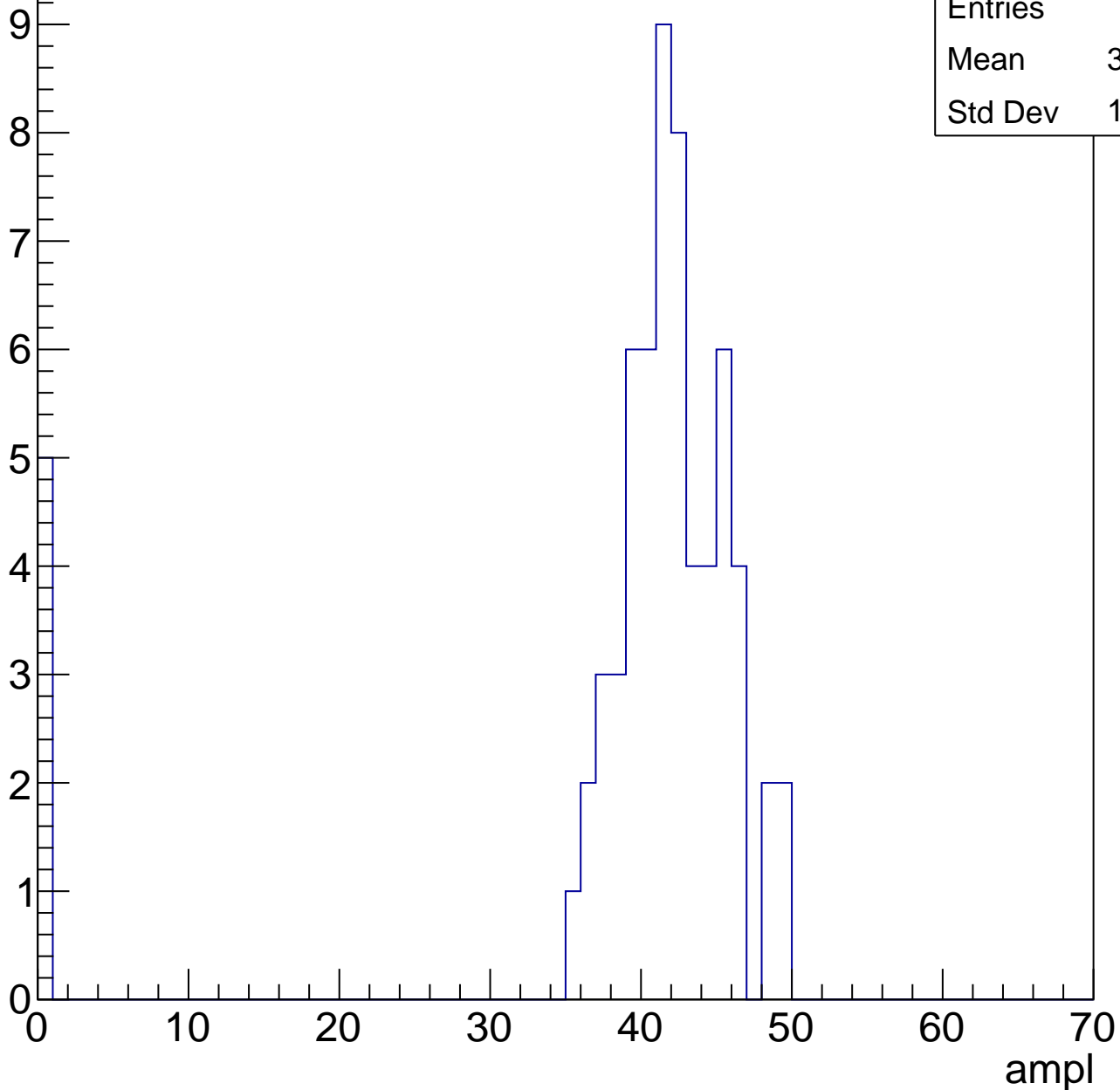


B1L103S, U23-ch58, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	38.57
Std Dev	11.57

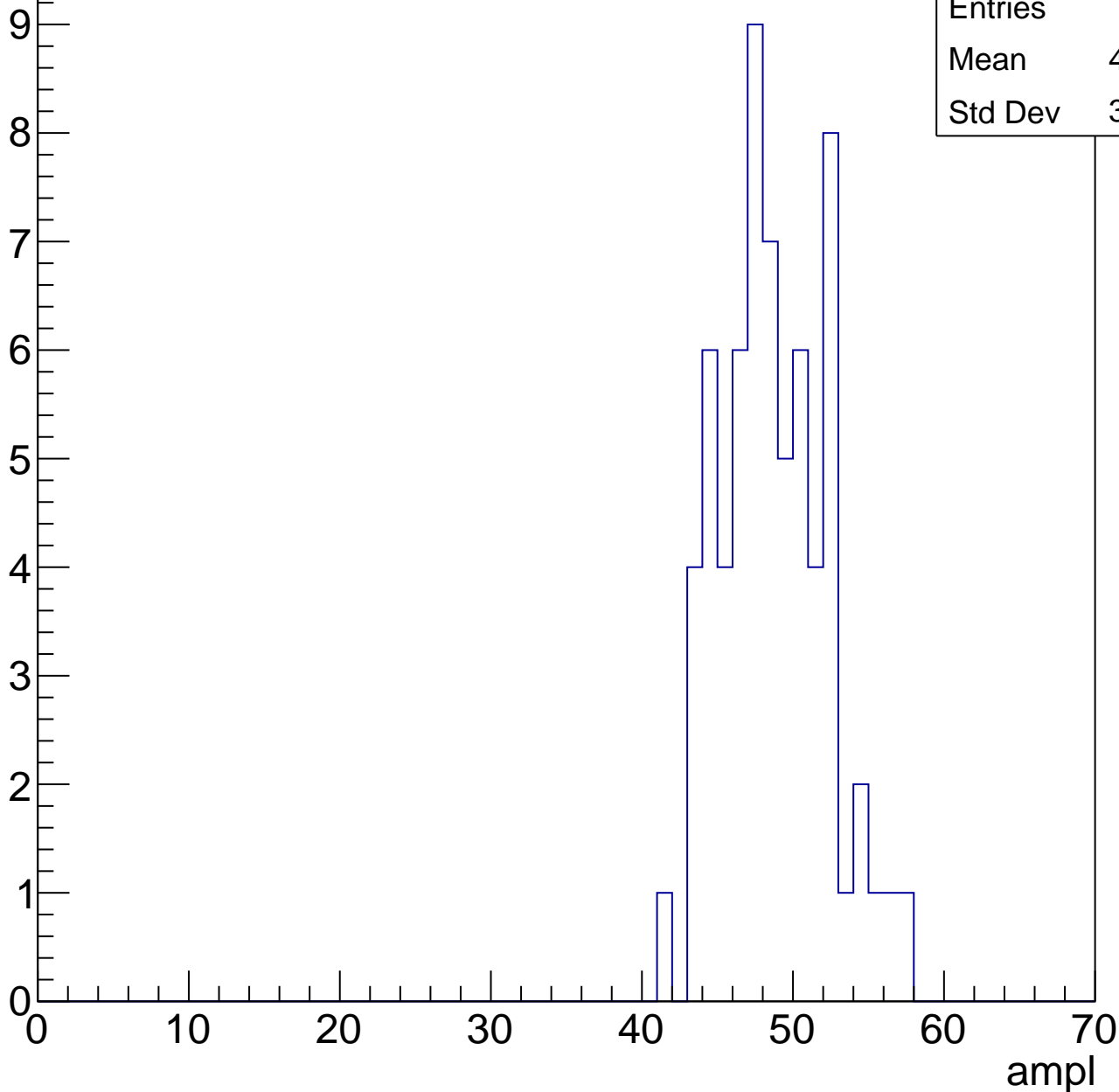


B1L103S, U23-ch58, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

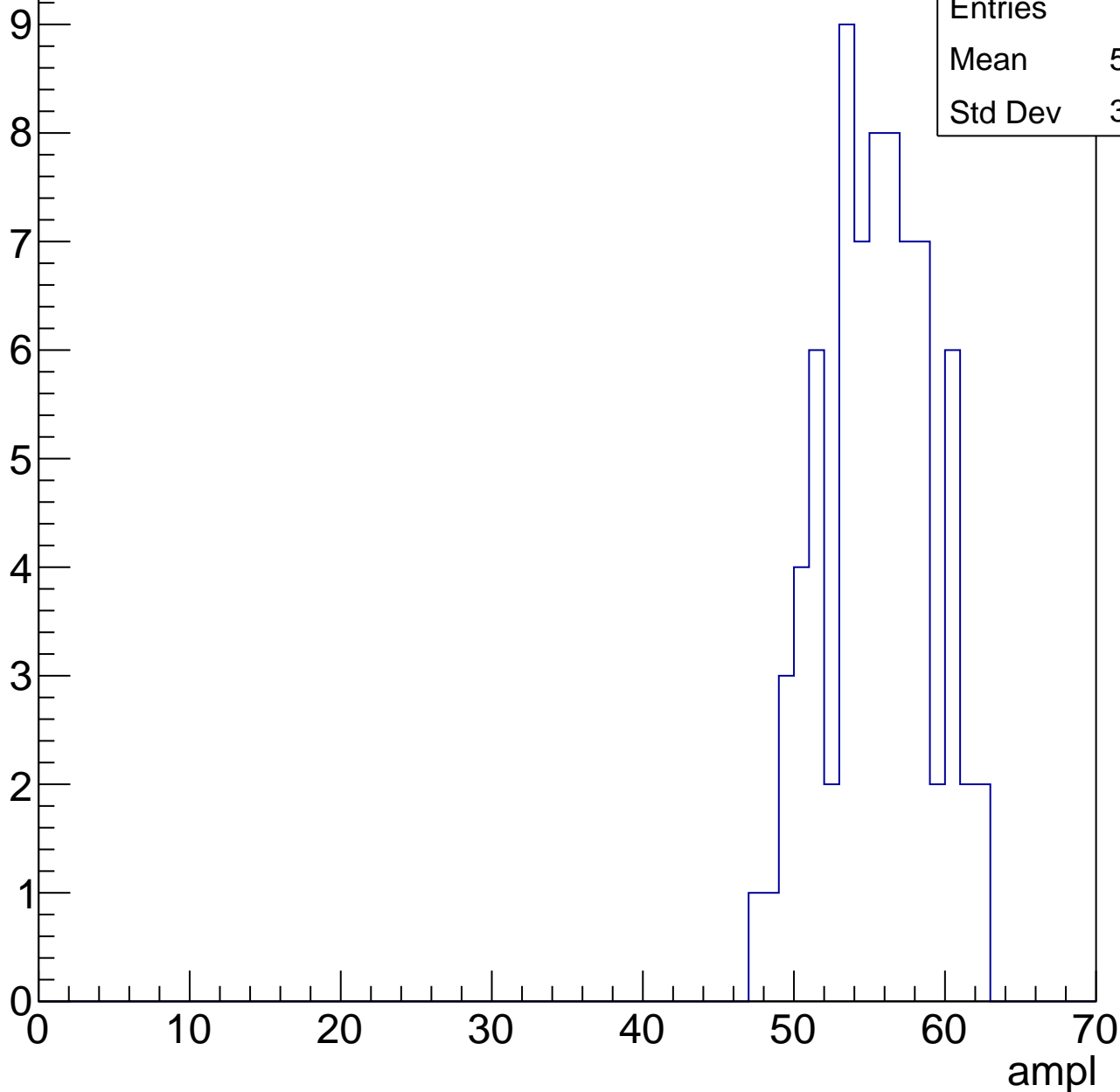
Entries	66
Mean	48.27
Std Dev	3.466



B1L103S, U23-ch58, adc4

calib_packv5_041523_1651.root, FC#0, port C2

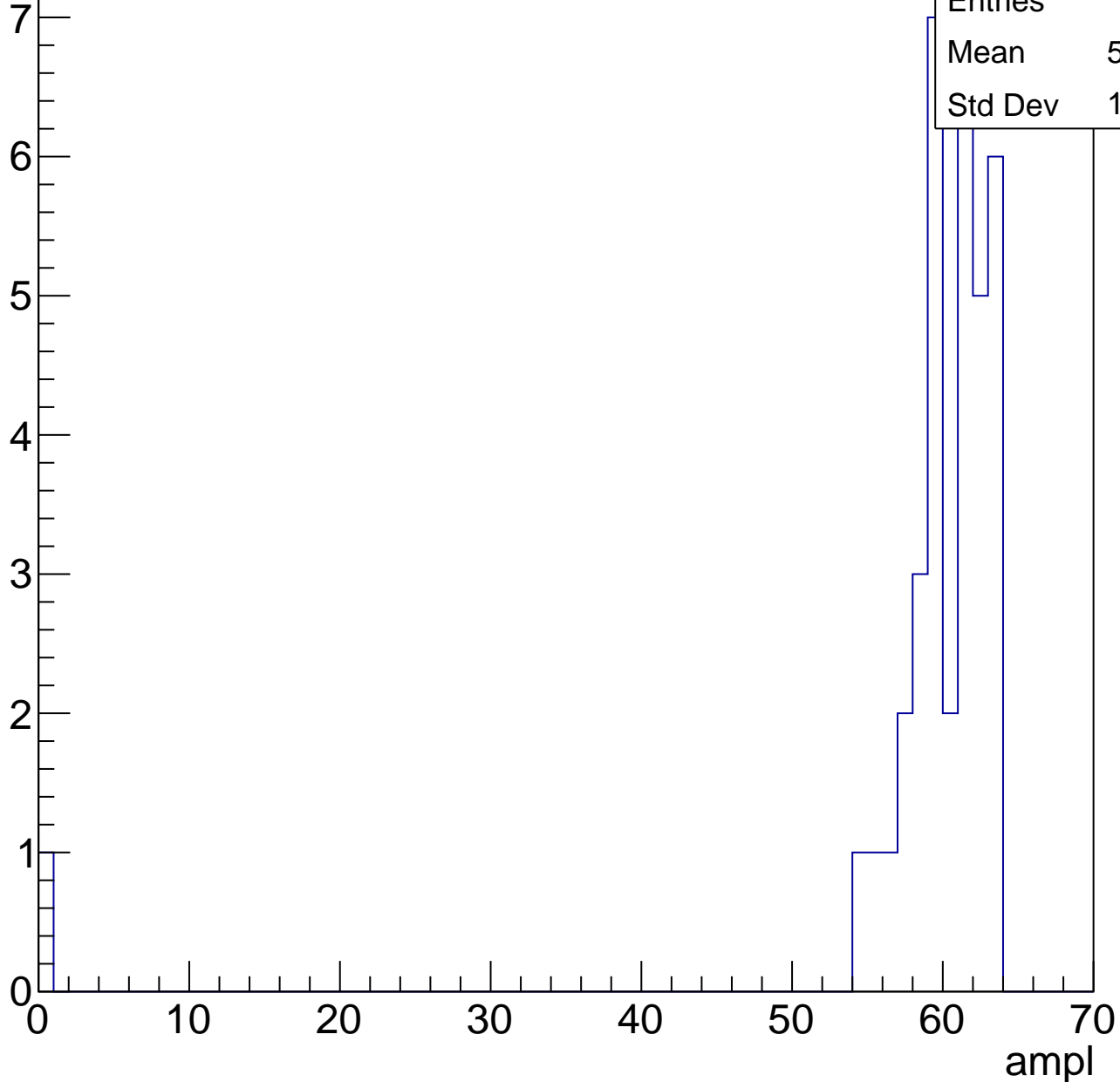
Entry



B1L103S, U23-ch58, adc5

calib_packv5_041523_1651.root, FC#0, port C2

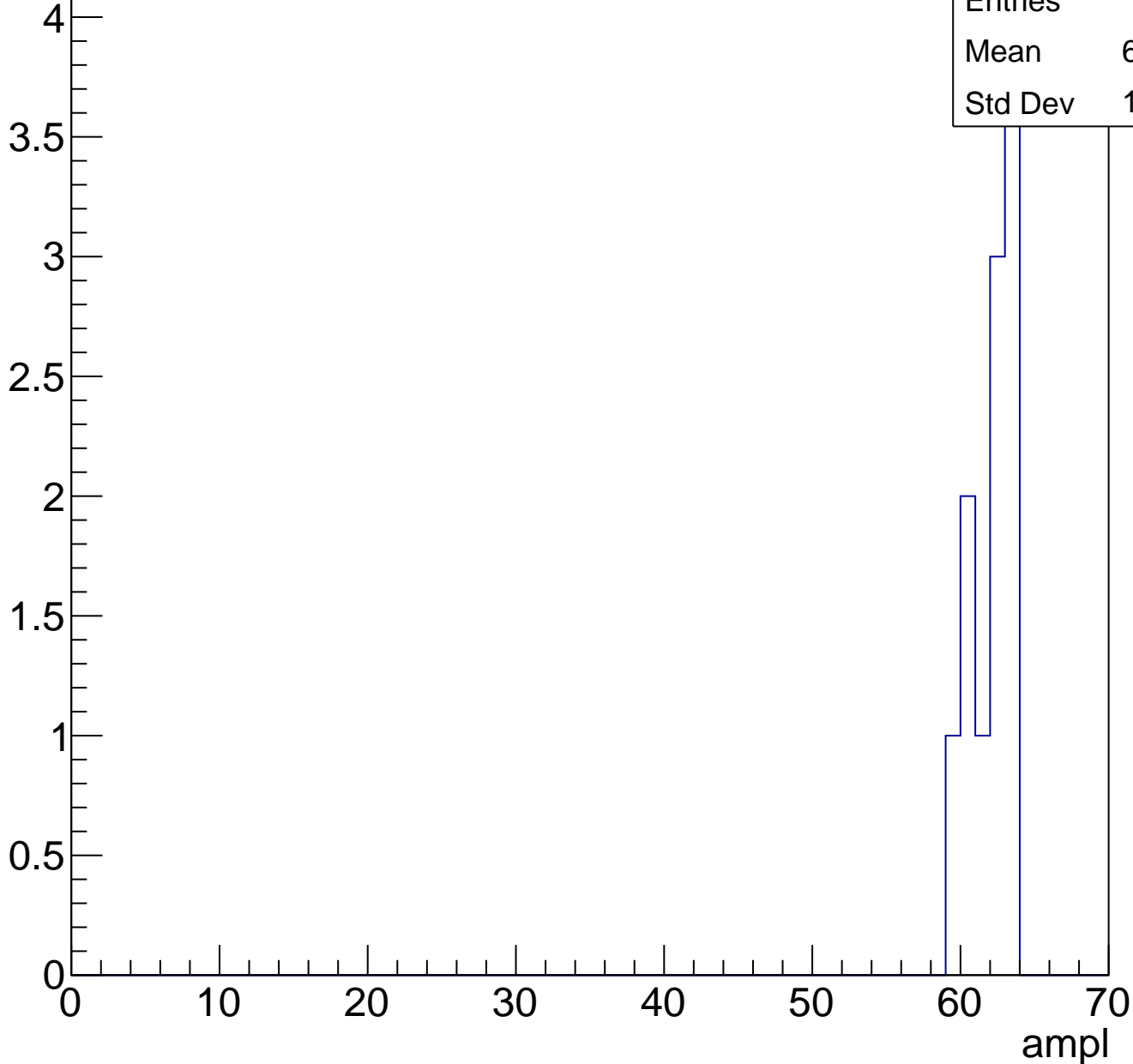
Entry



B1L103S, U23-ch58, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch58, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	19
Mean	0
Std Dev	0

B1L103S, U23-ch59, adc0

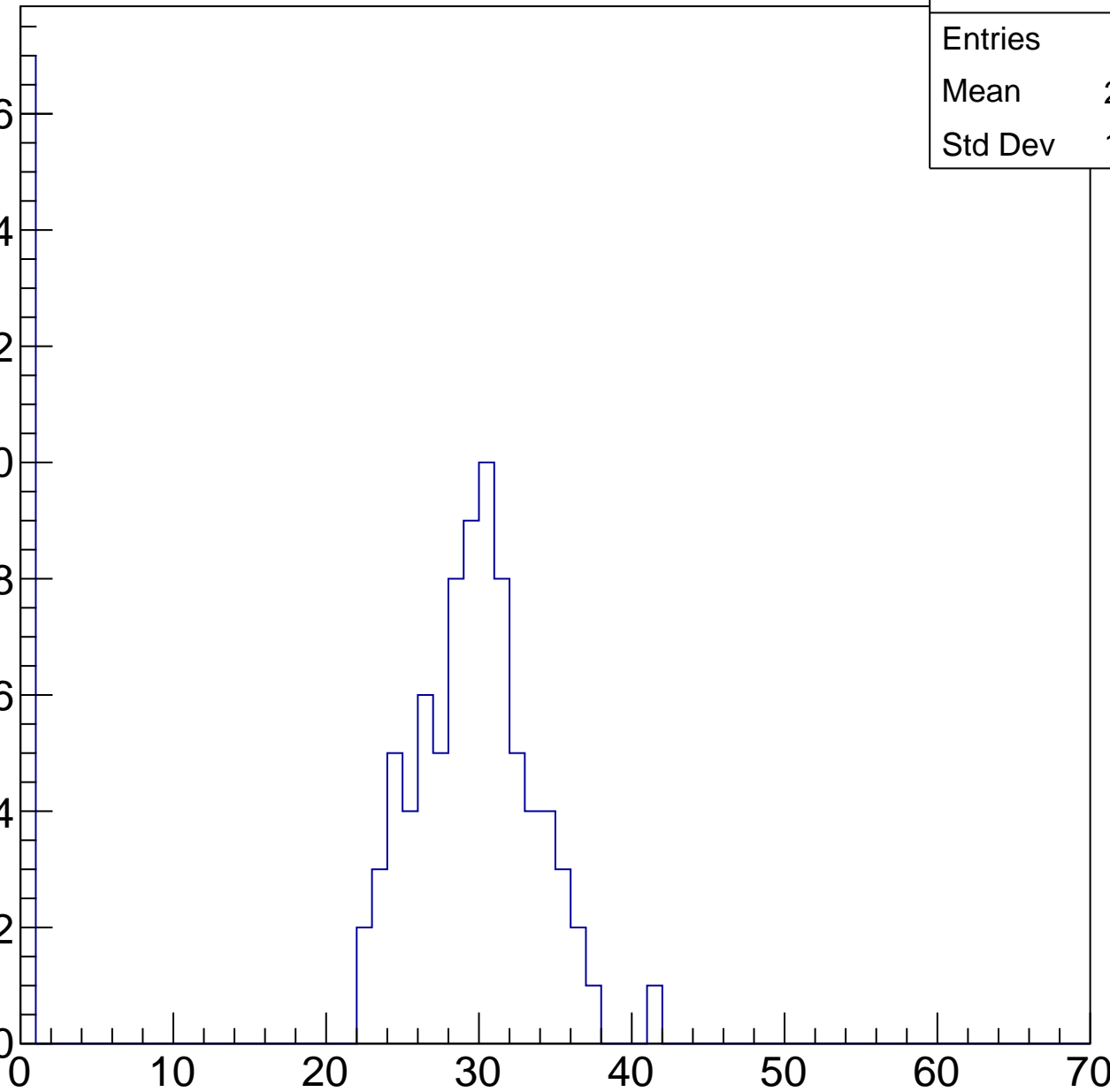
calib_packv5_041523_1651.root, FC#0, port C2

Entries	97
Mean	24.12
Std Dev	11.64

Entry

16
14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch59, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	75
Mean	35.17
Std Dev	7.849

Entry

10

8

6

4

2

0

0

10

20

30

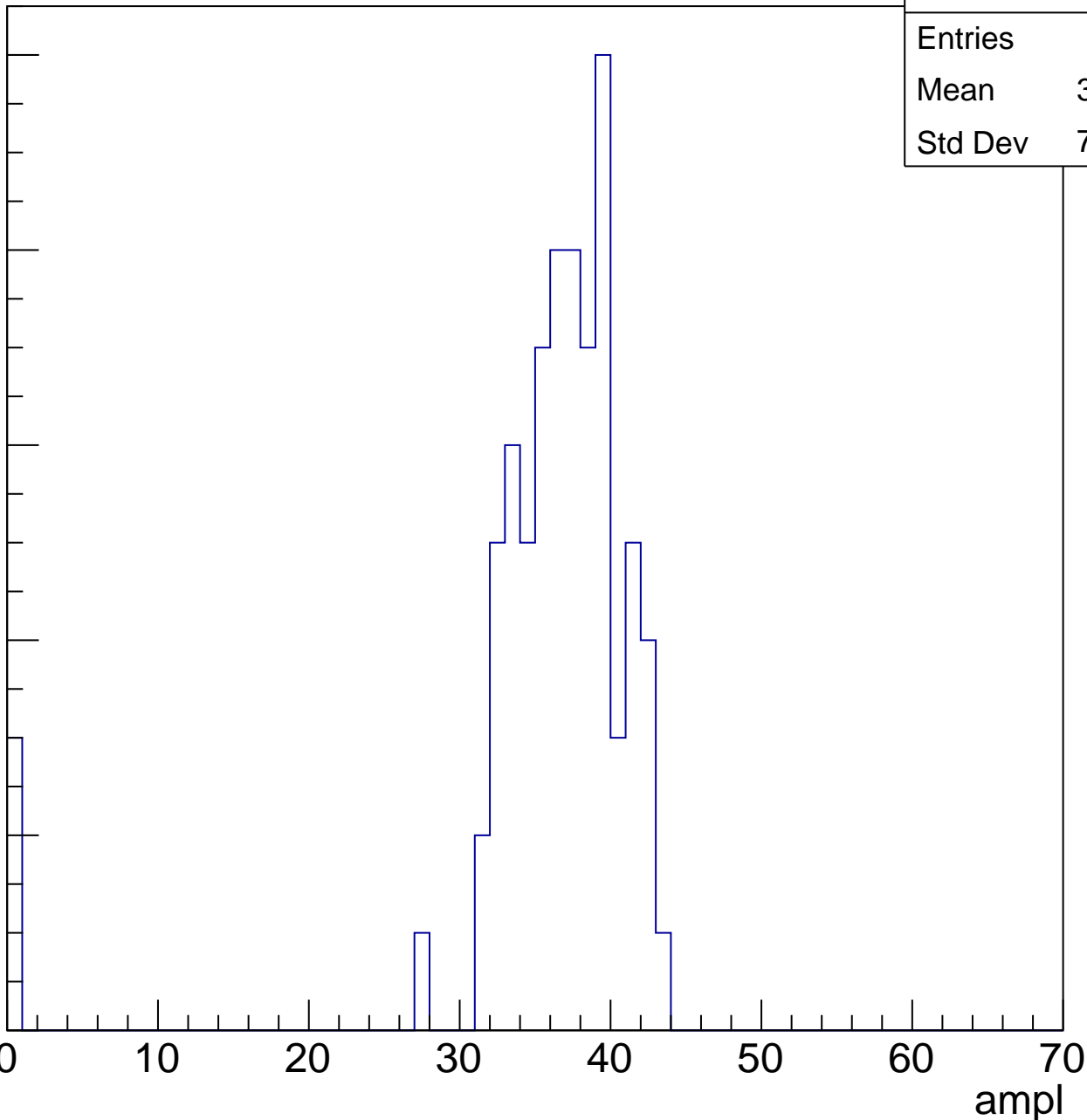
40

50

60

70

ampl

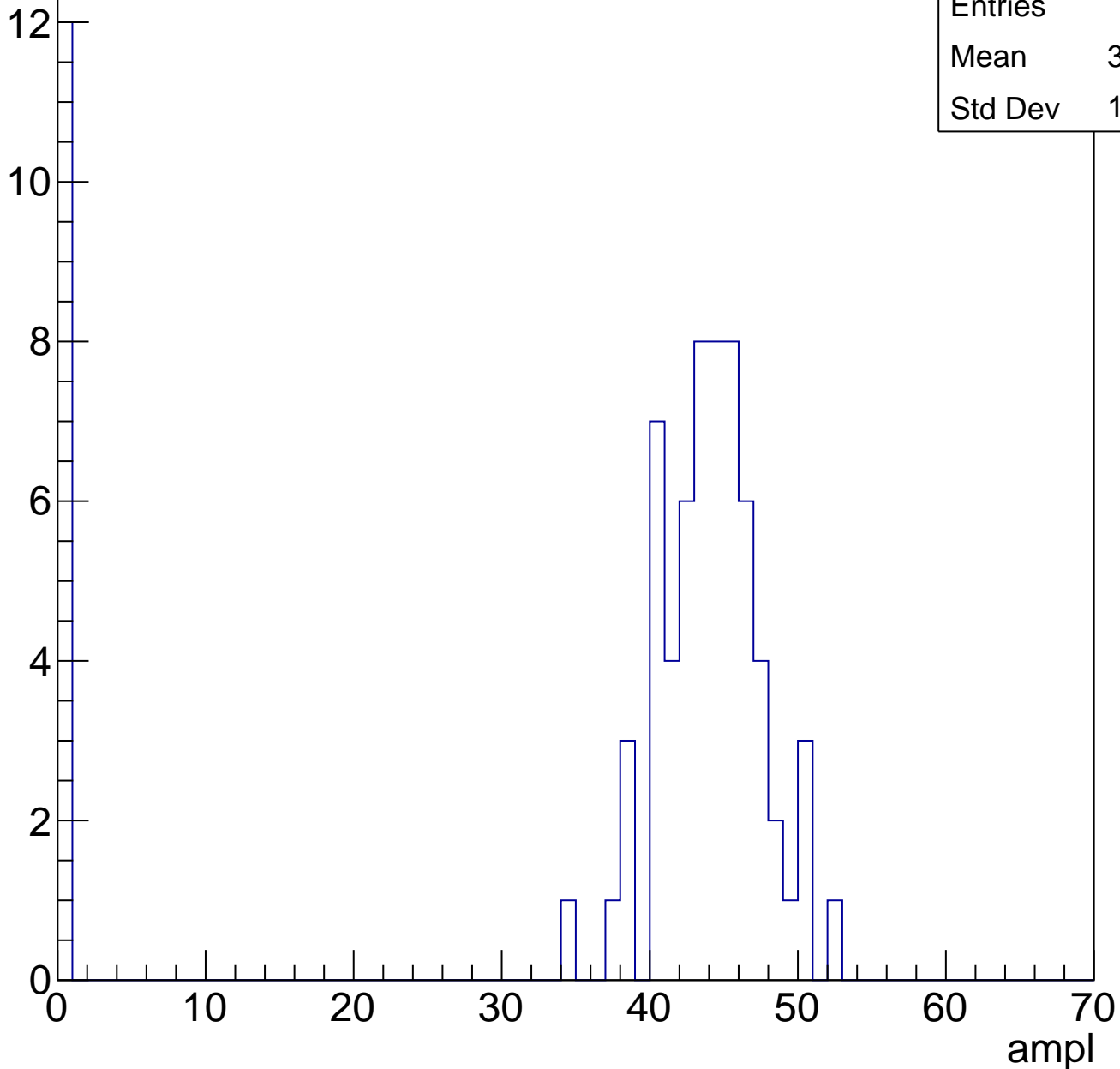


B1L103S, U23-ch59, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	75
Mean	36.64
Std Dev	16.29

Entry

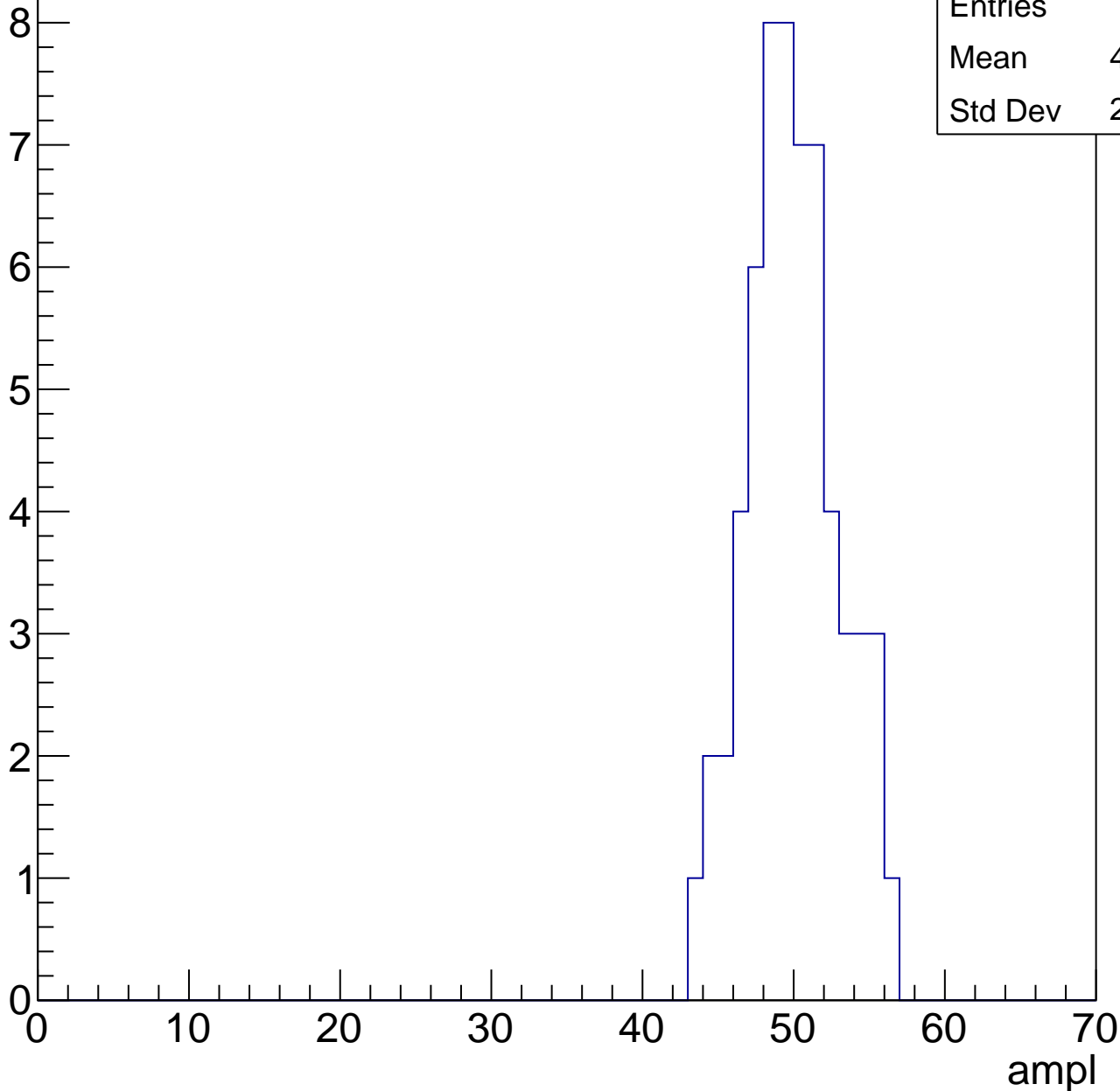


B1L103S, U23-ch59, adc3

calib_packv5_041523_1651.root, FC#0, port C2

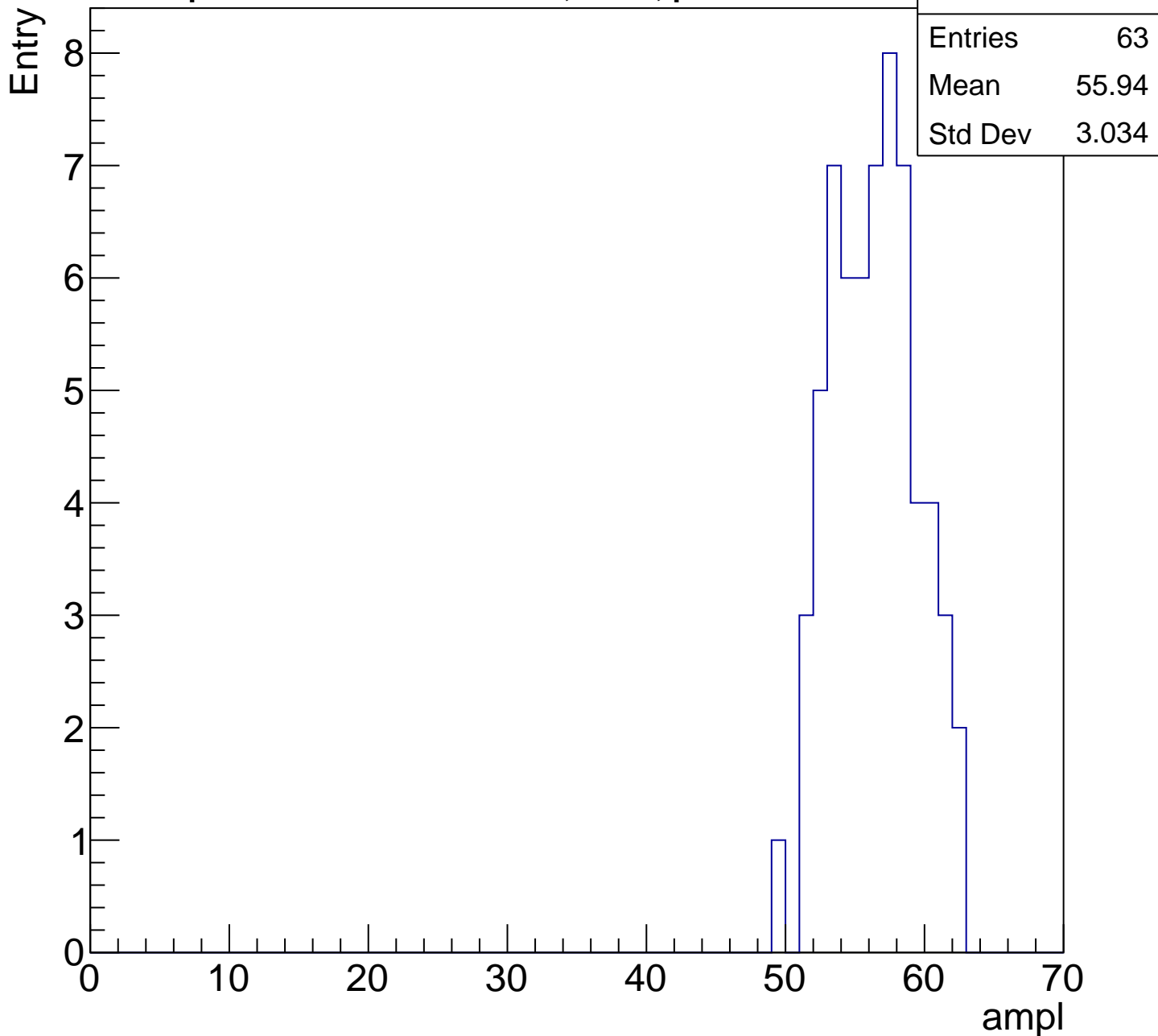
Entry

Entries	59
Mean	49.49
Std Dev	2.977



B1L103S, U23-ch59, adc4

calib_packv5_041523_1651.root, FC#0, port C2

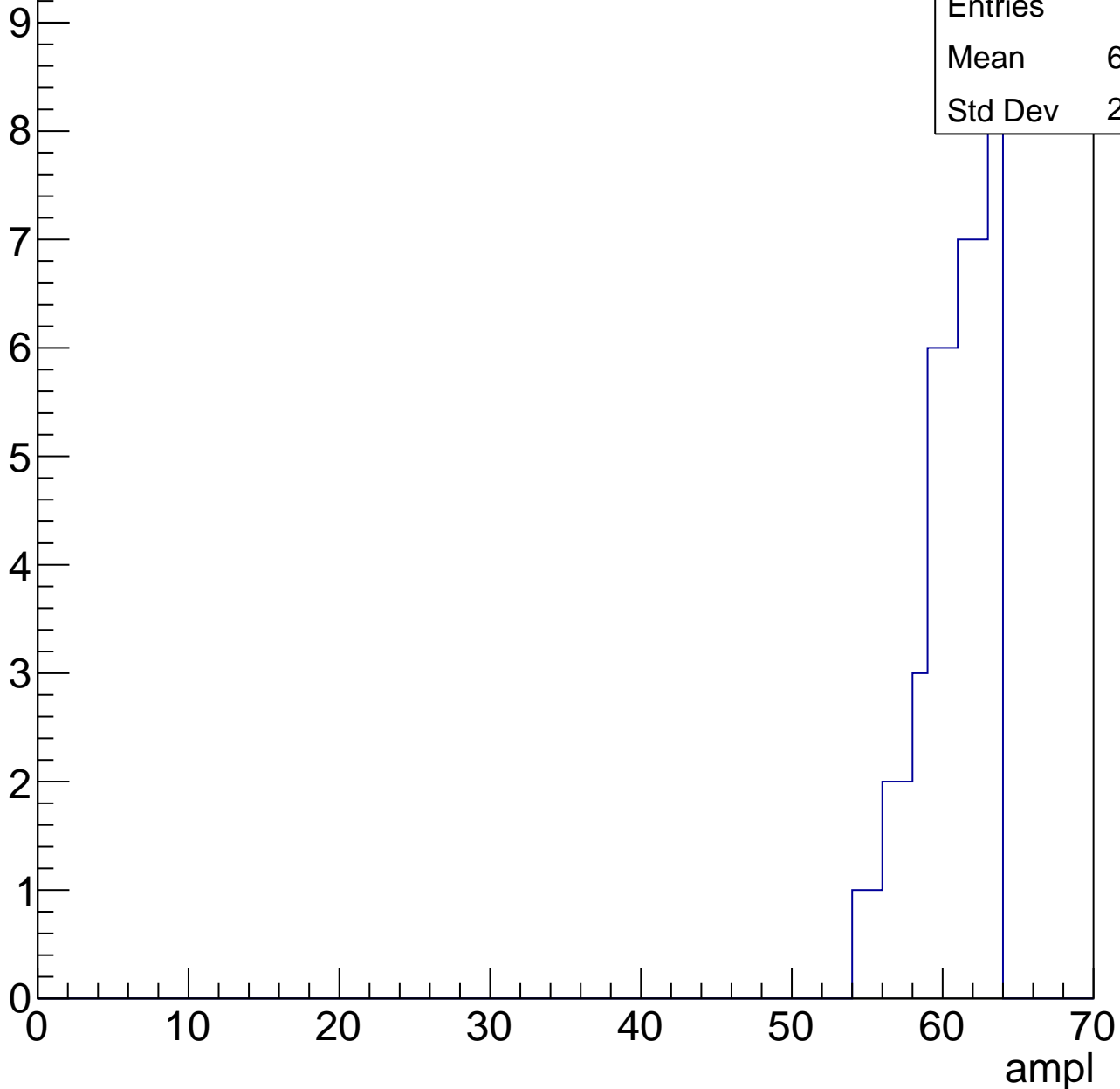


B1L103S, U23-ch59, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	44
Mean	60.25
Std Dev	2.346



B1L103S, U23-ch59, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch59, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U23-ch60, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	89
Mean	20.89
Std Dev	14.11

Entry

25

20

15

10

5

0

0

10

20

30

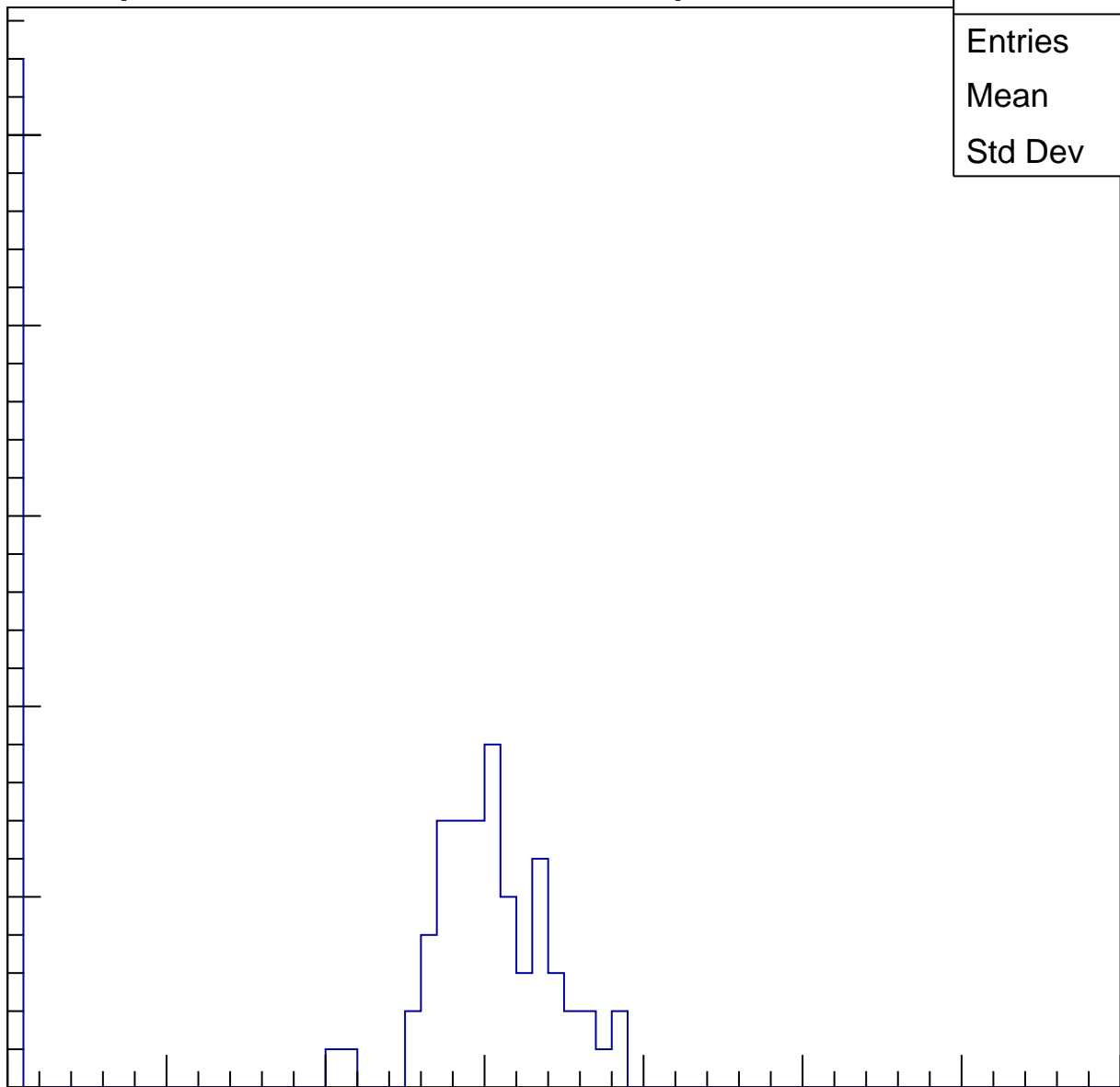
40

50

60

70

ampl

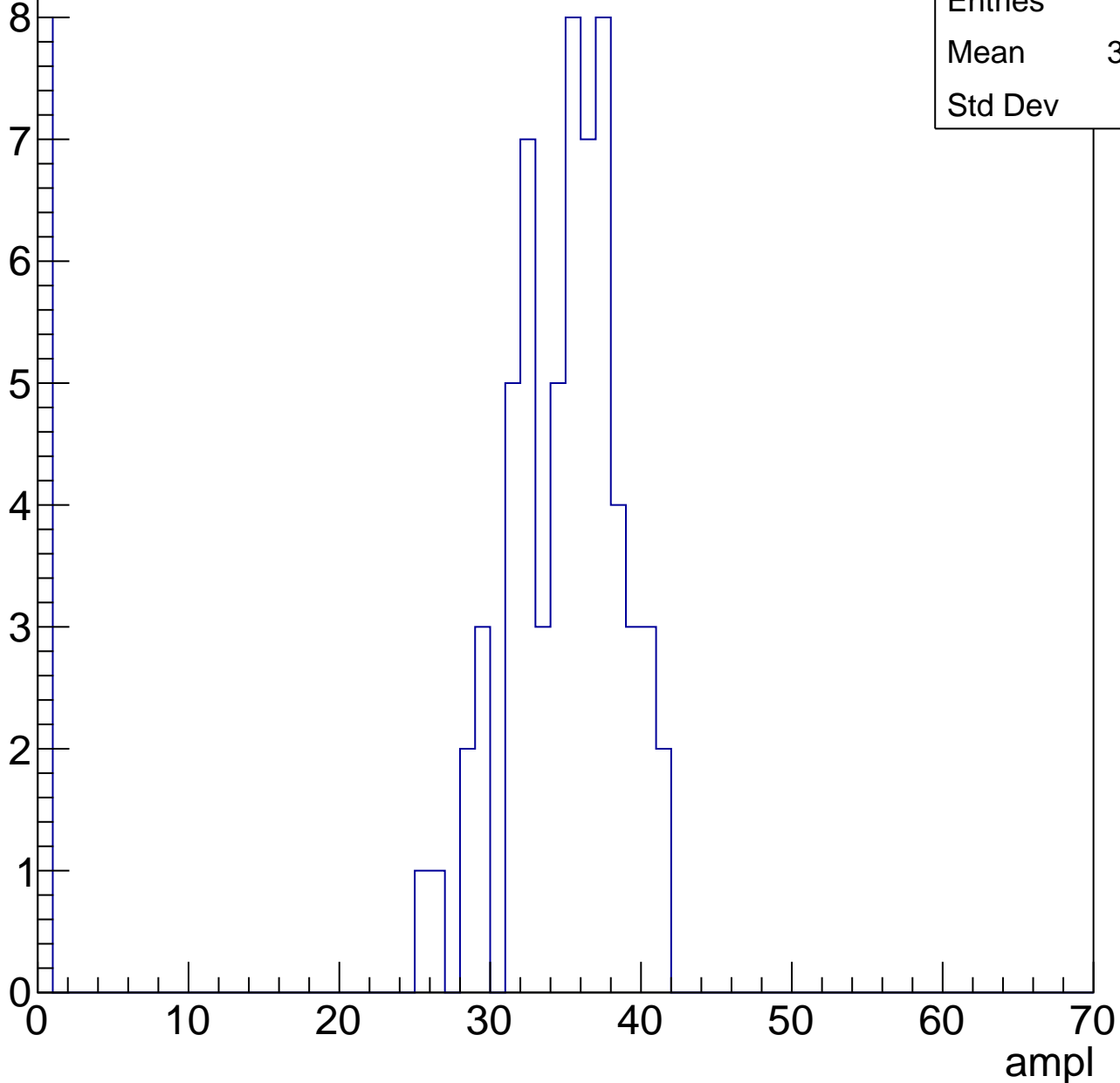


B1L103S, U23-ch60, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	30.59
Std Dev	11.5

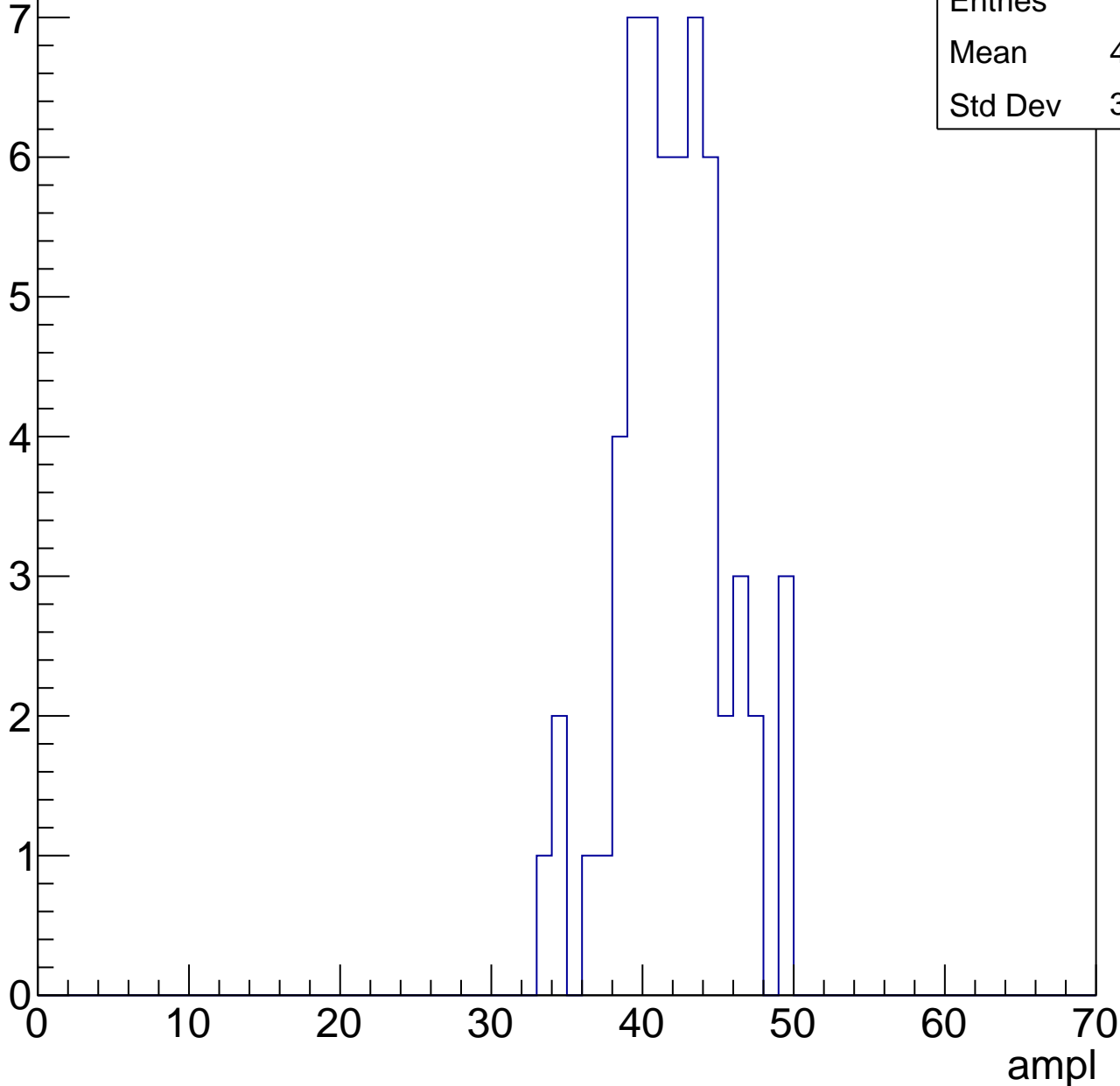


B1L103S, U23-ch60, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	41.57
Std Dev	3.509

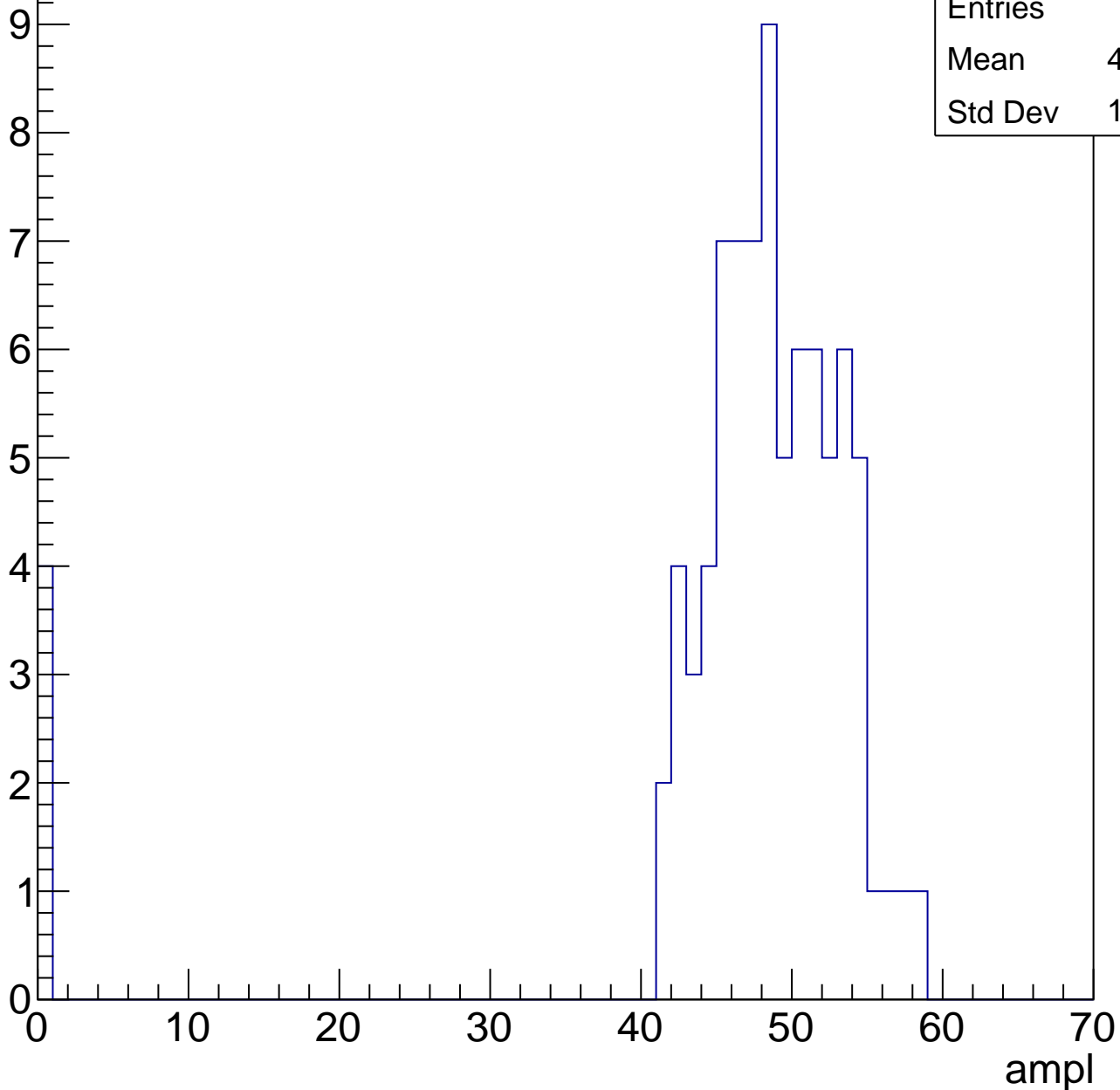


B1L103S, U23-ch60, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	84
Mean	46.17
Std Dev	11.02

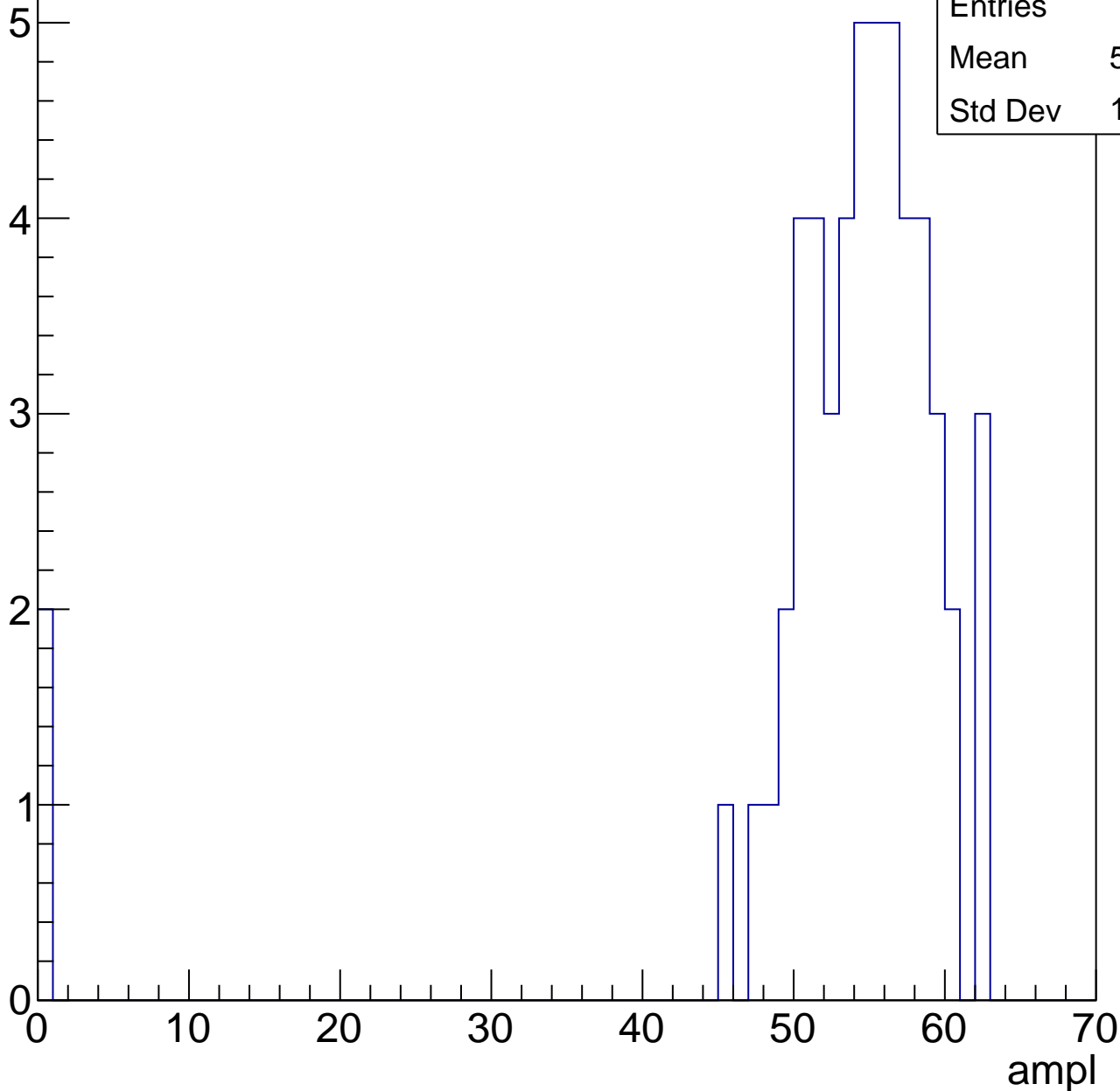


B1L103S, U23-ch60, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	53
Mean	52.42
Std Dev	11.07

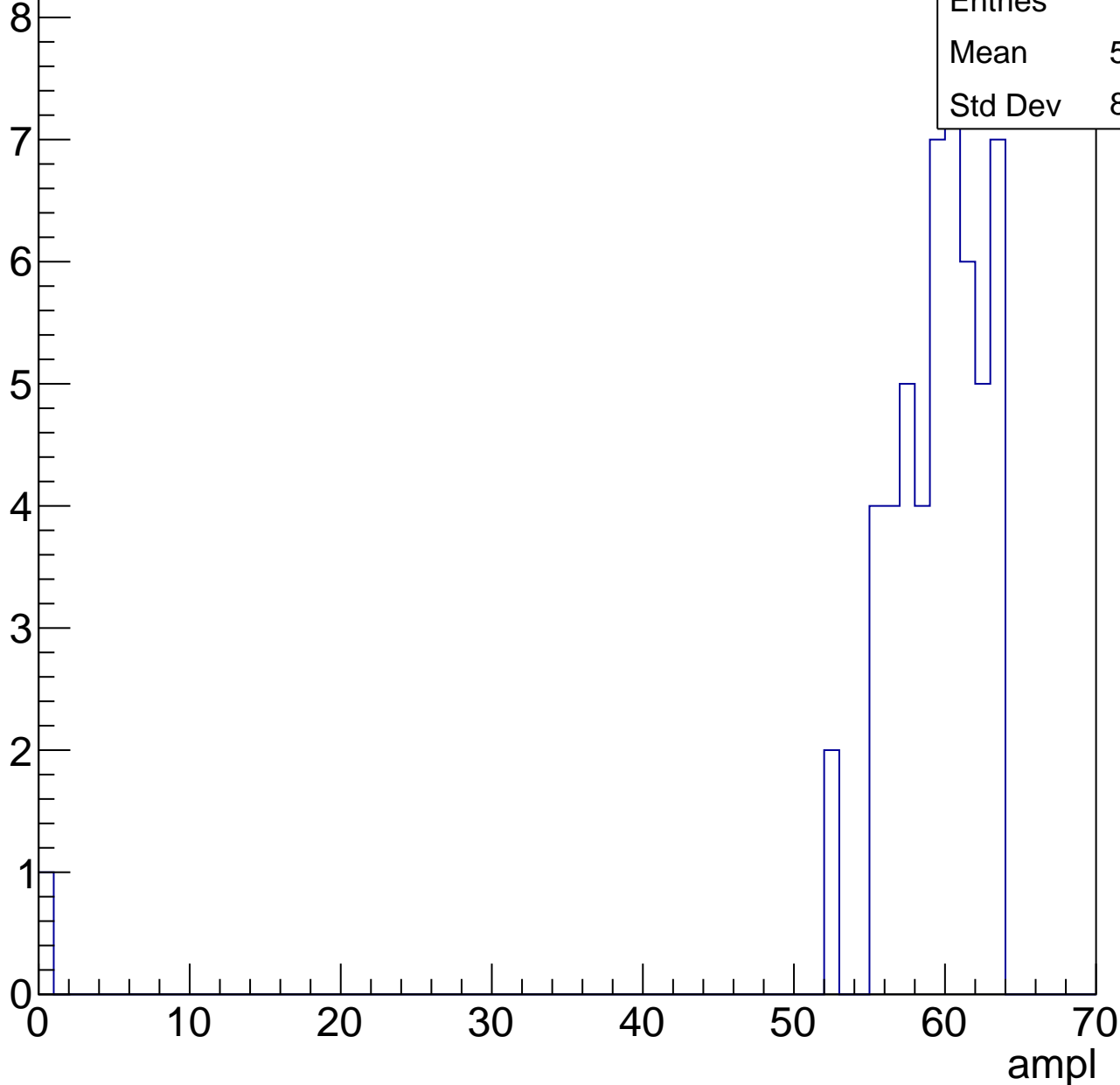


B1L103S, U23-ch60, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

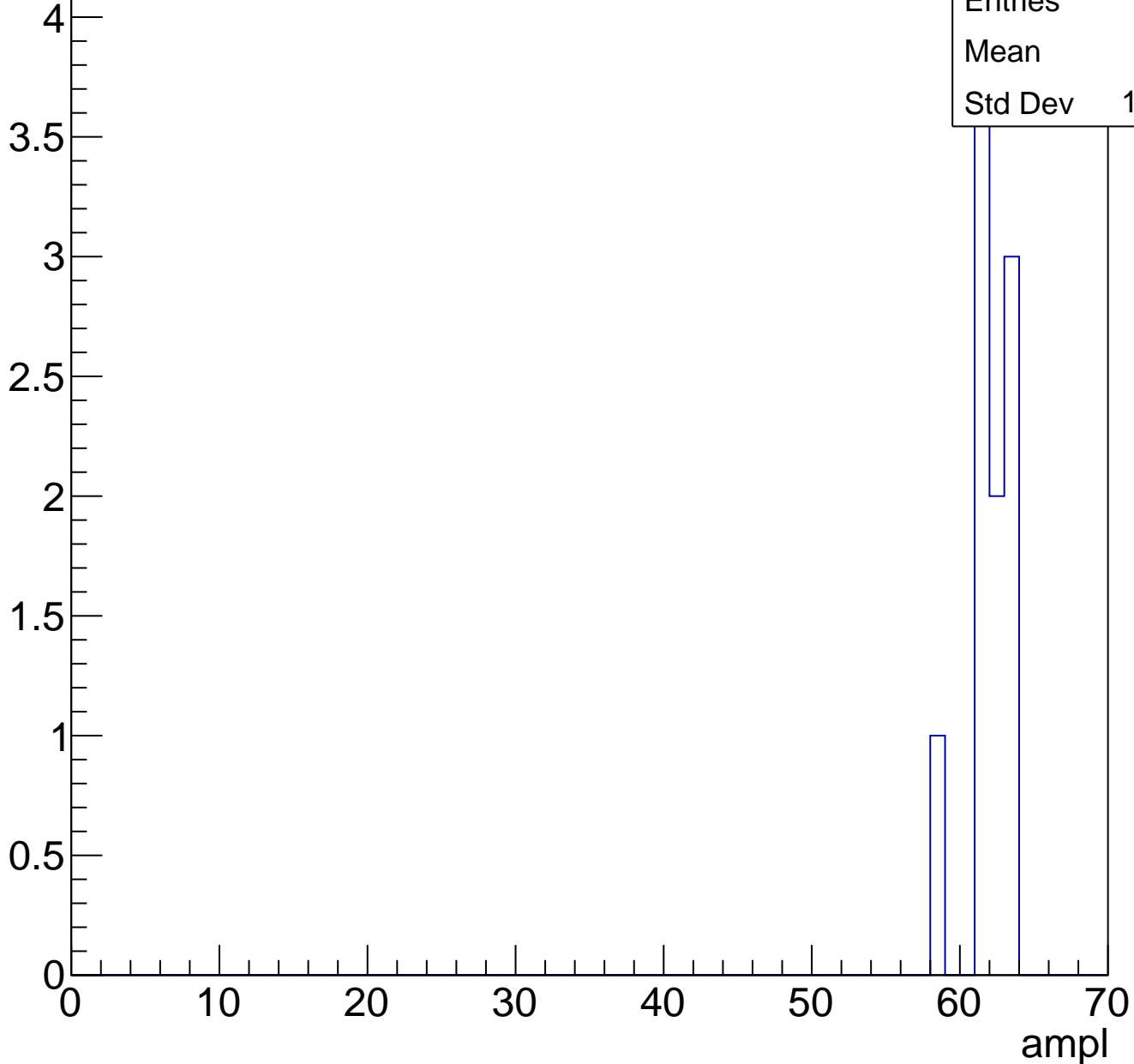
Entries	53
Mean	58.02
Std Dev	8.513



B1L103S, U23-ch60, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch60, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch61, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	91
Mean	19.8
Std Dev	13.45

Entry

25

20

15

10

5

0

0

10

20

30

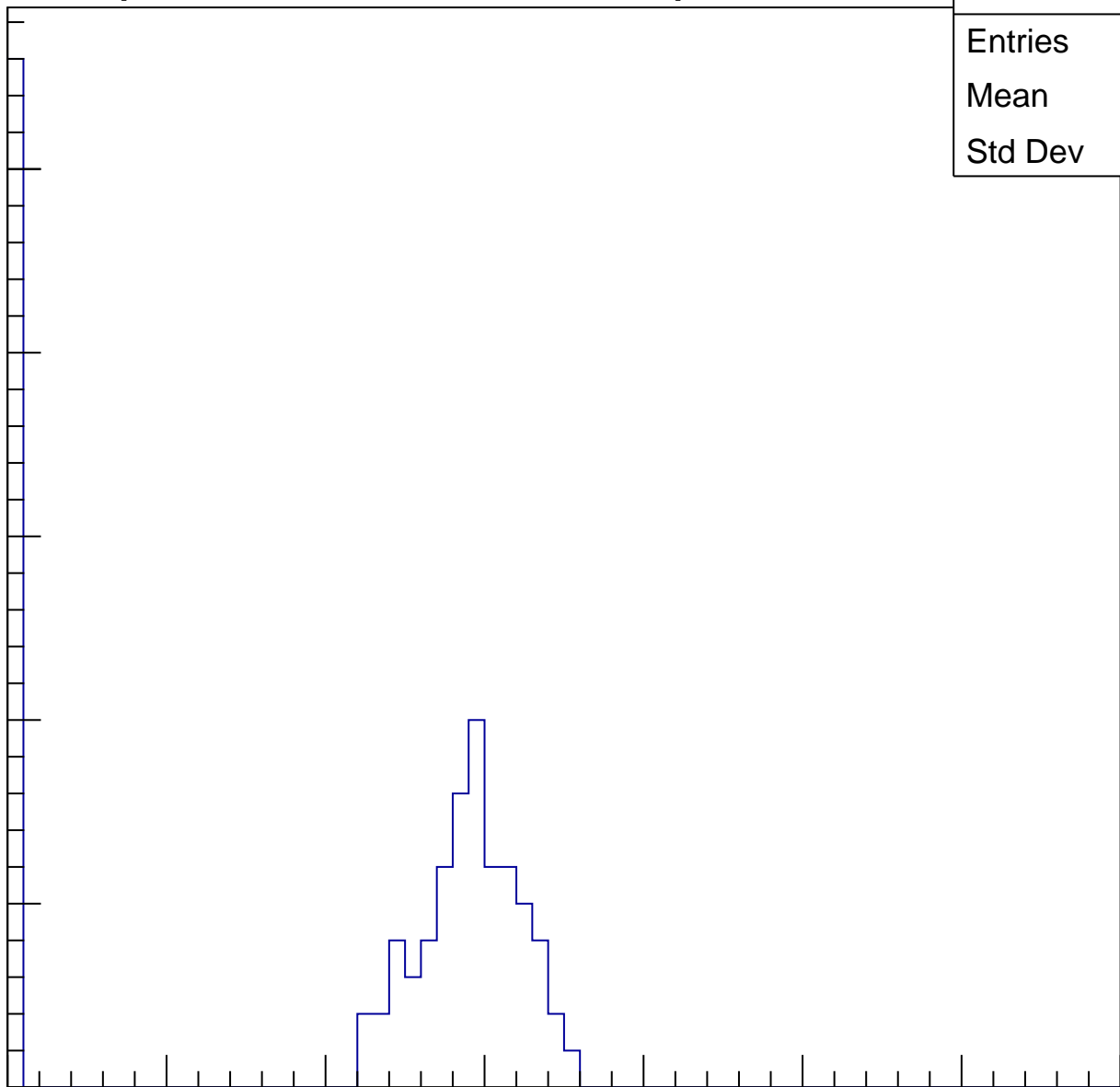
40

50

60

70

ampl



B1L103S, U23-ch61, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	91
Mean	31.7
Std Dev	12.31

Entry

10

8

6

4

2

0

0

10

20

30

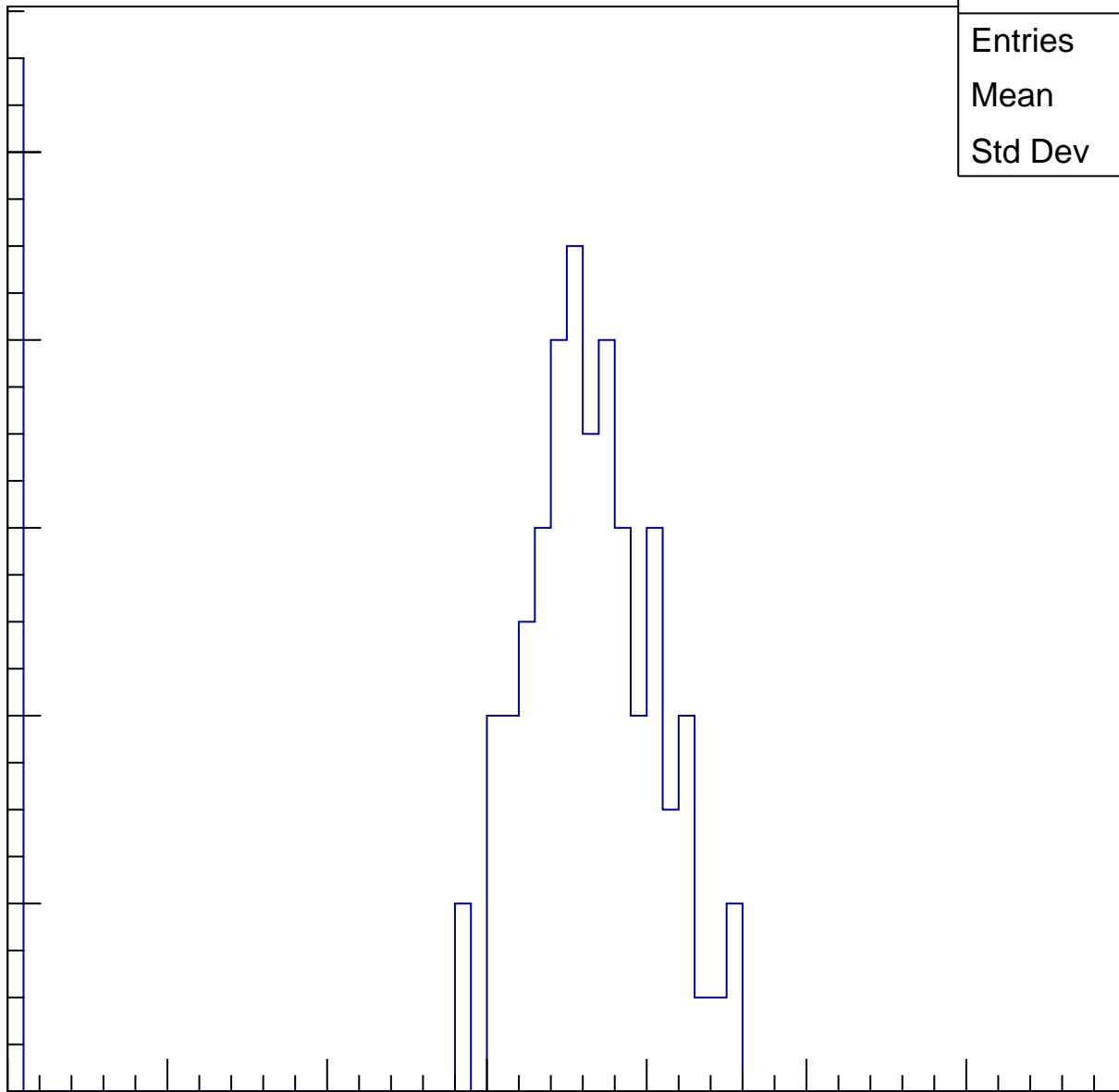
40

50

60

70

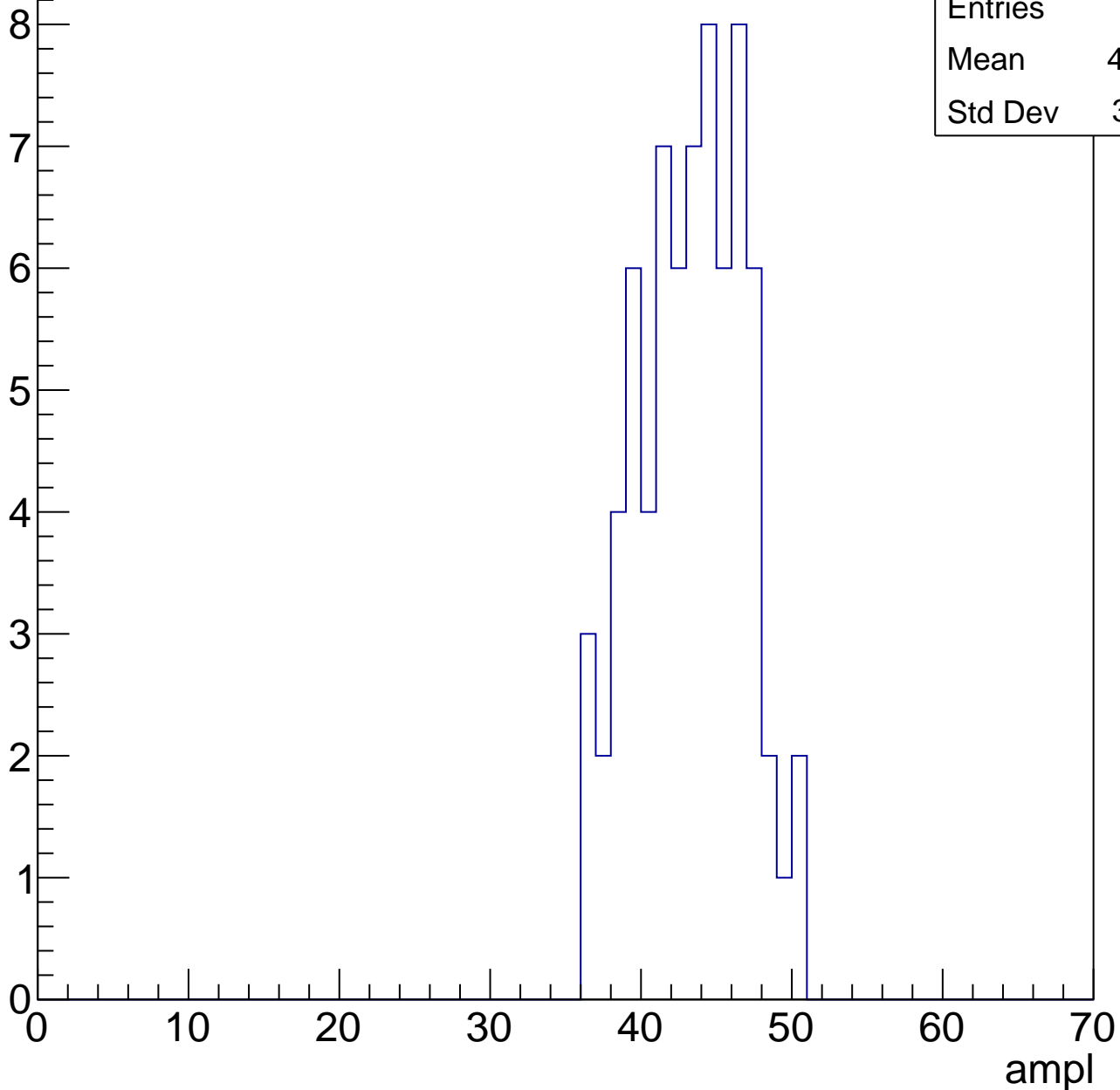
ampl



B1L103S, U23-ch61, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry



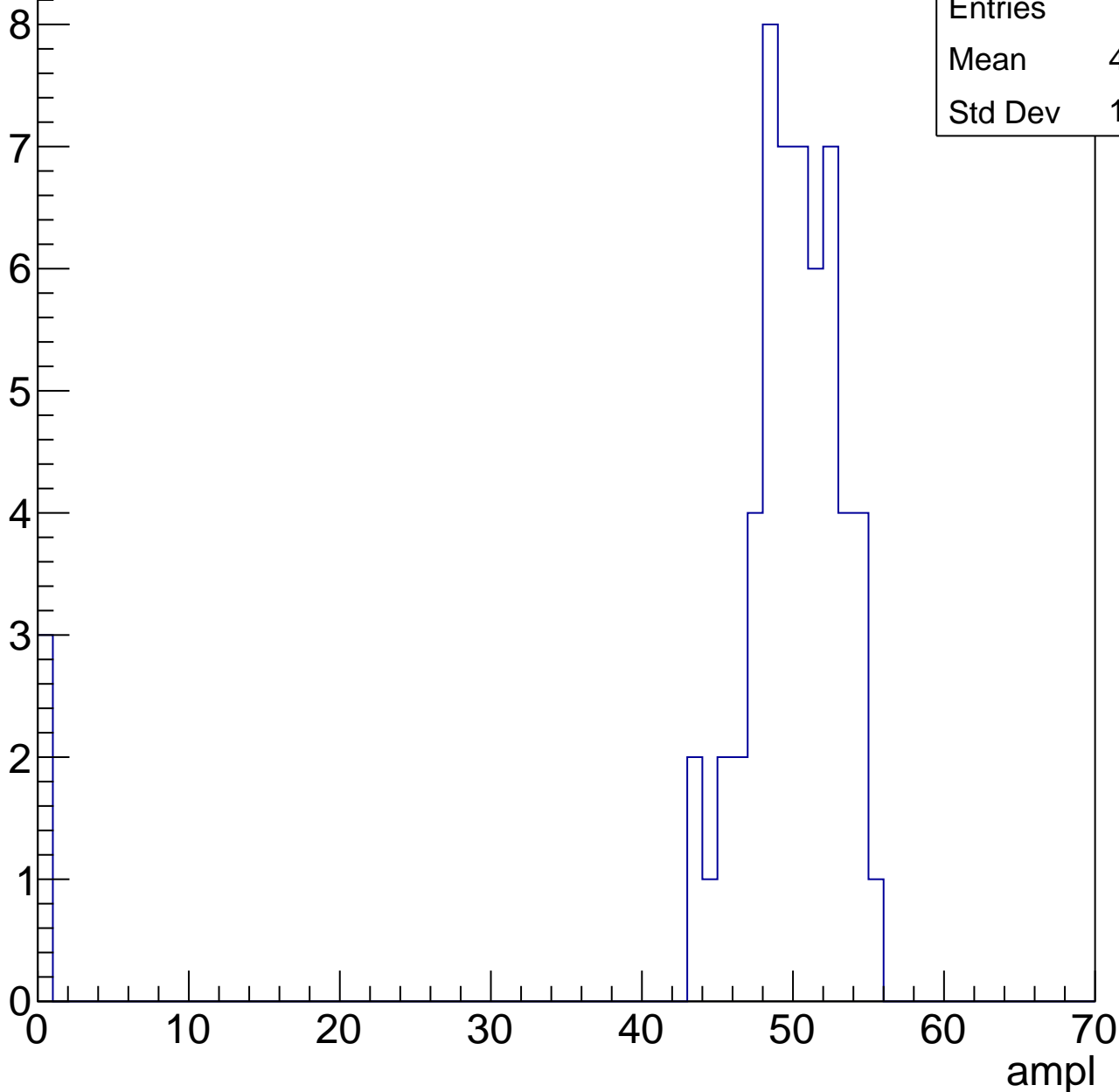
Entries	72
Mean	42.85
Std Dev	3.471

B1L103S, U23-ch61, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	47.07
Std Dev	11.33

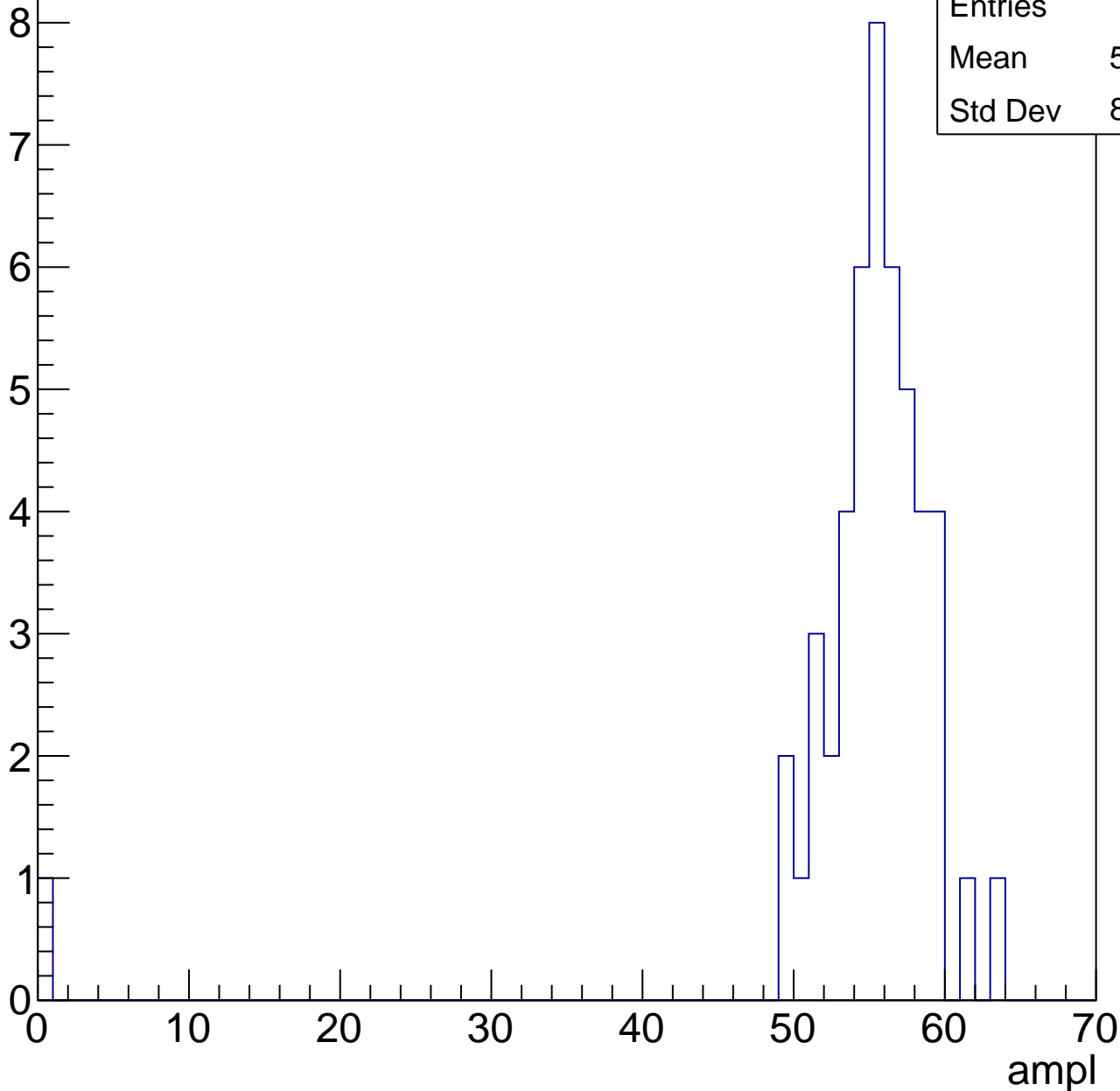


B1L103S, U23-ch61, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	48
Mean	54.04
Std Dev	8.406

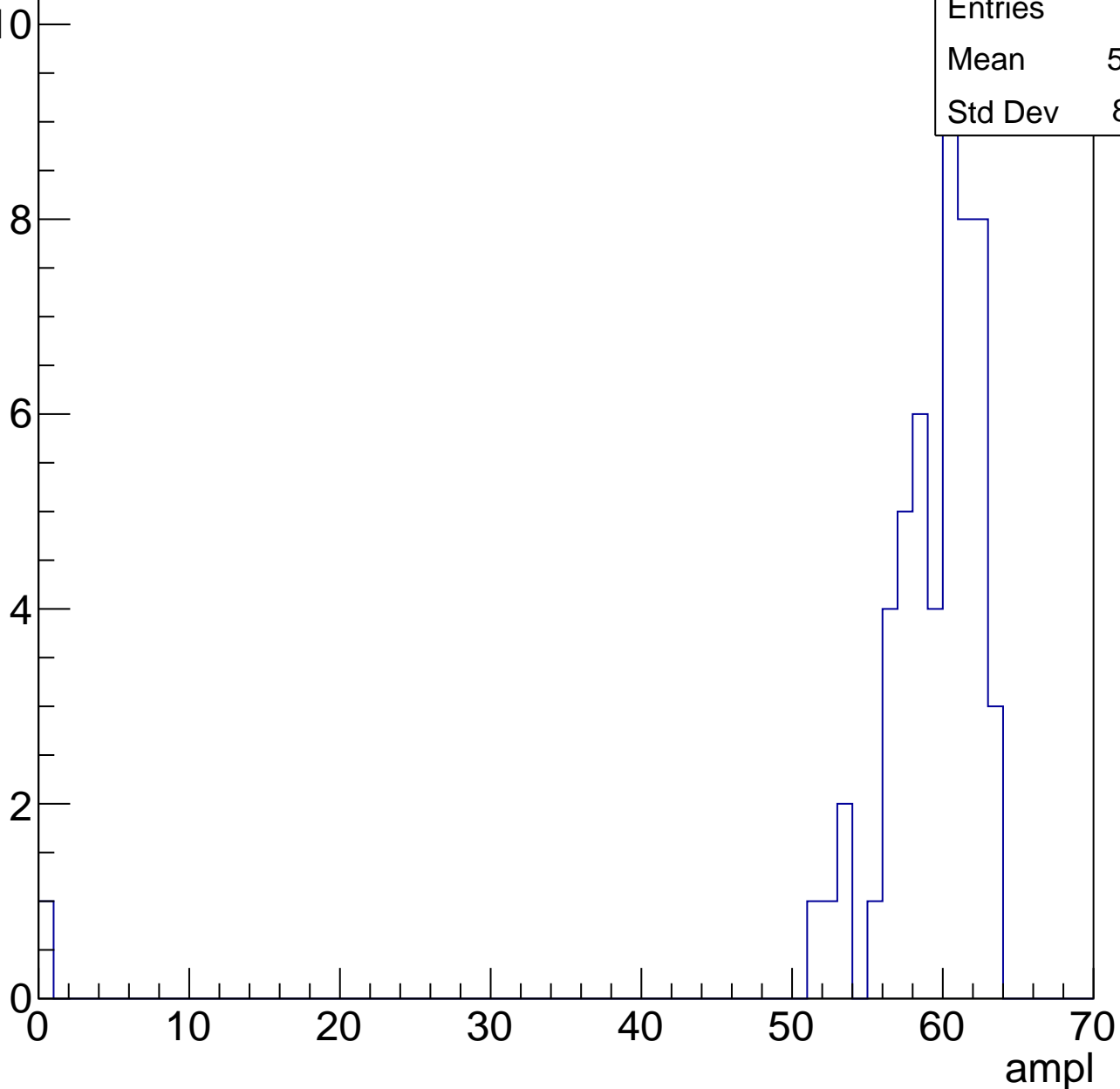


B1L103S, U23-ch61, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	54
Mean	57.96
Std Dev	8.441

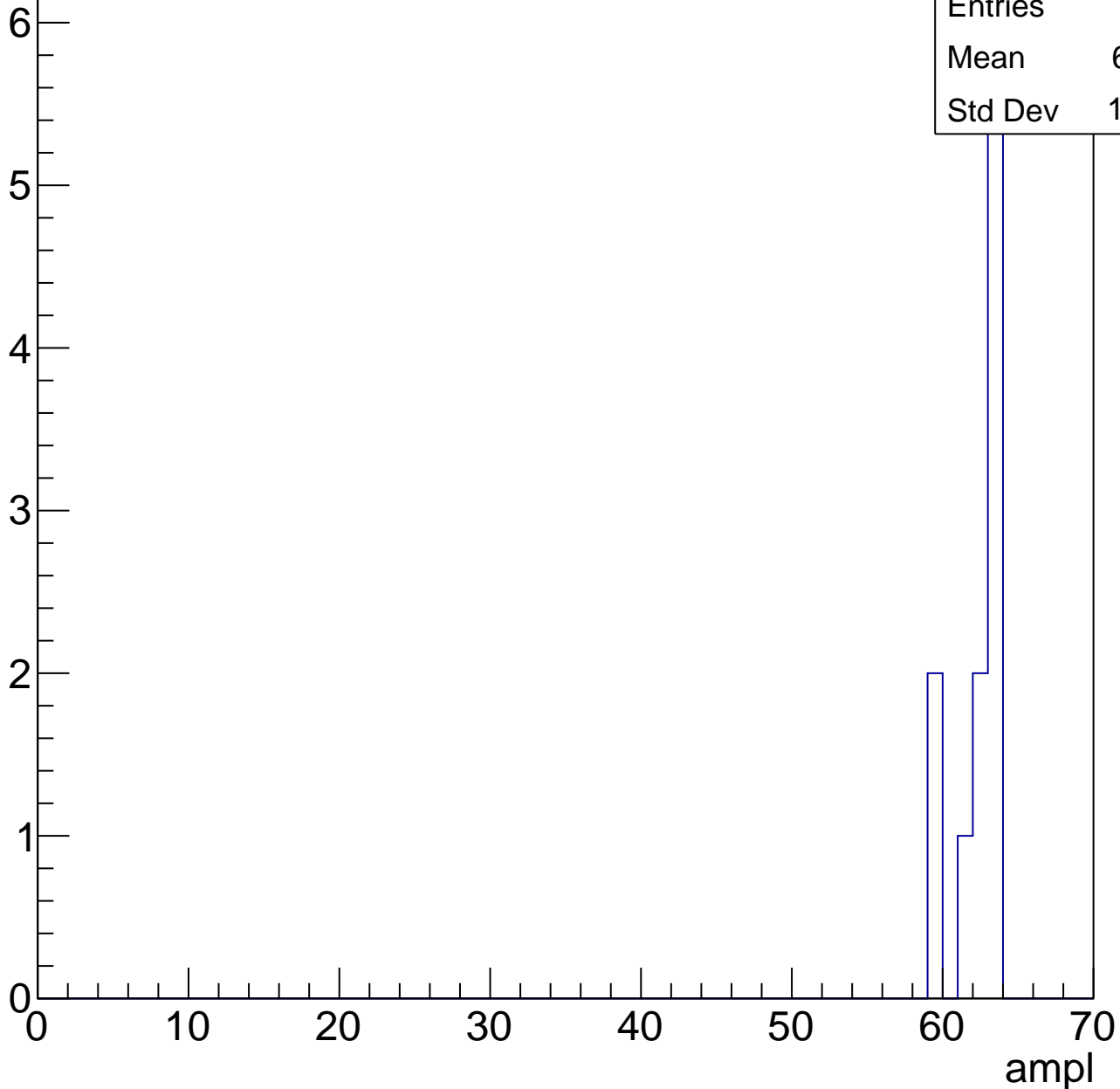


B1L103S, U23-ch61, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	11
Mean	61.91
Std Dev	1.505



B1L103S, U23-ch61, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

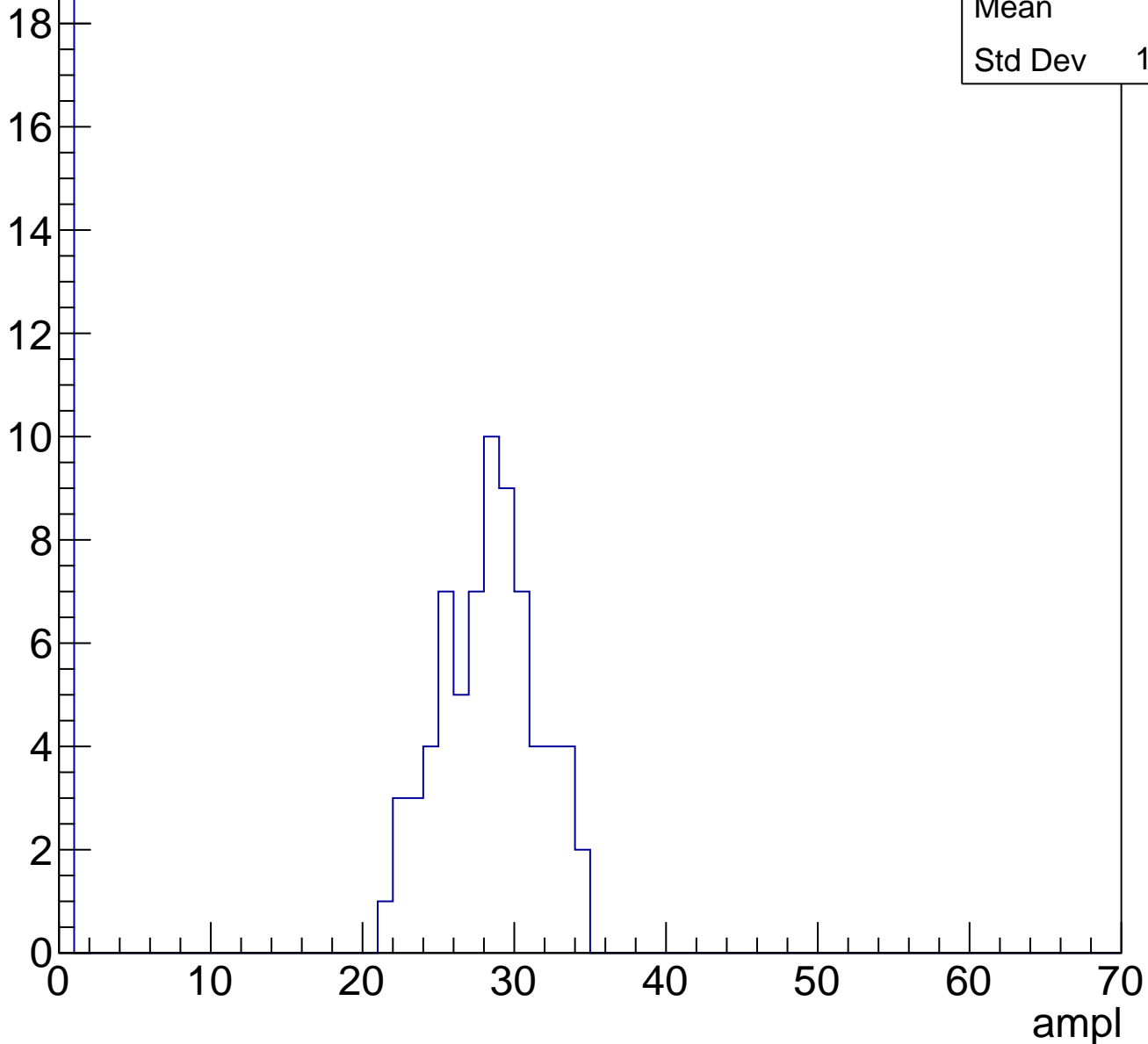


B1L103S, U23-ch62, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	89
Mean	21.9
Std Dev	11.75

Entry

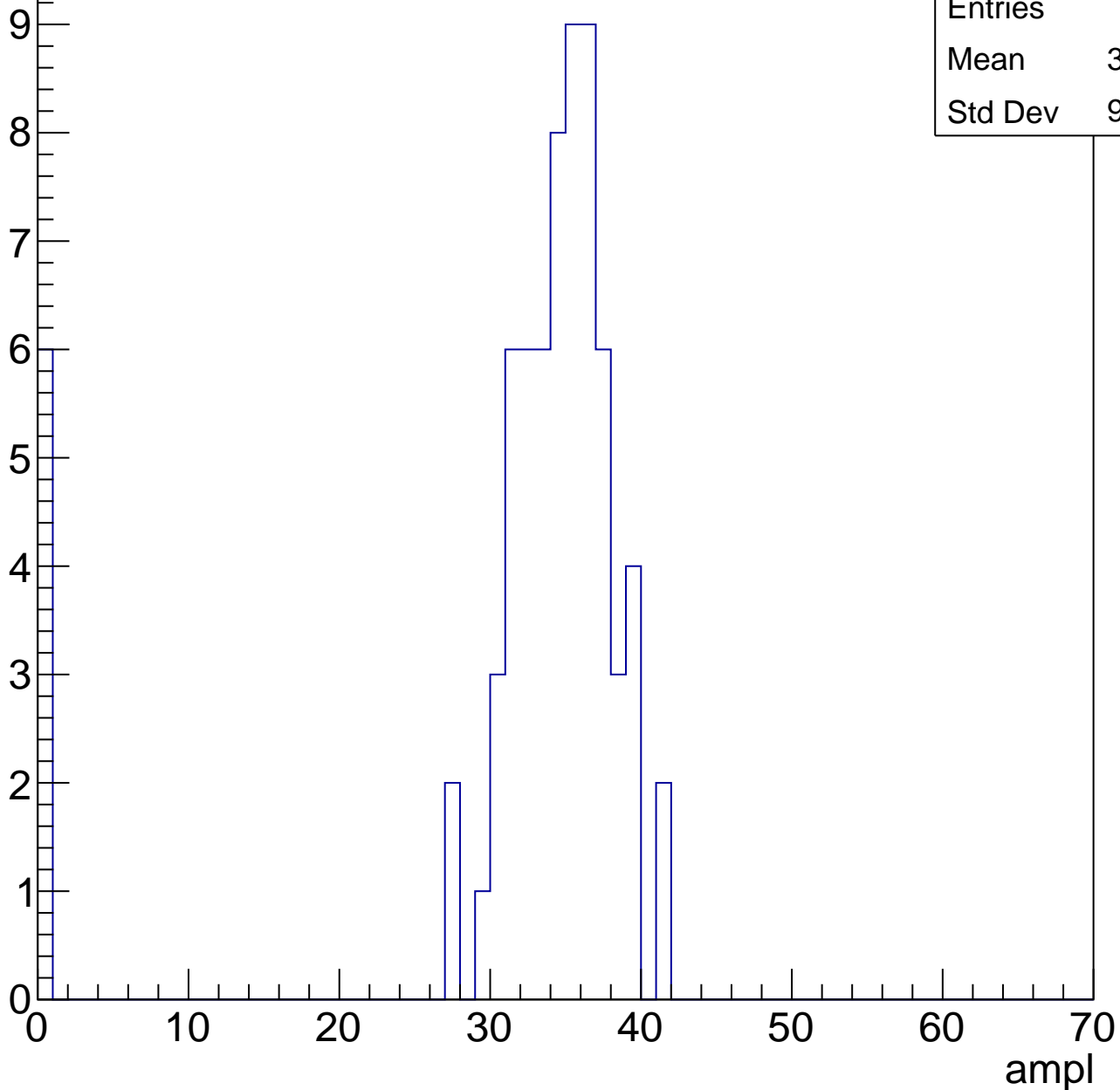


B1L103S, U23-ch62, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	31.46
Std Dev	9.986



B1L103S, U23-ch62, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	61
Mean	33.28
Std Dev	15.82

Entry

10

8

6

4

2

0

0

10

20

30

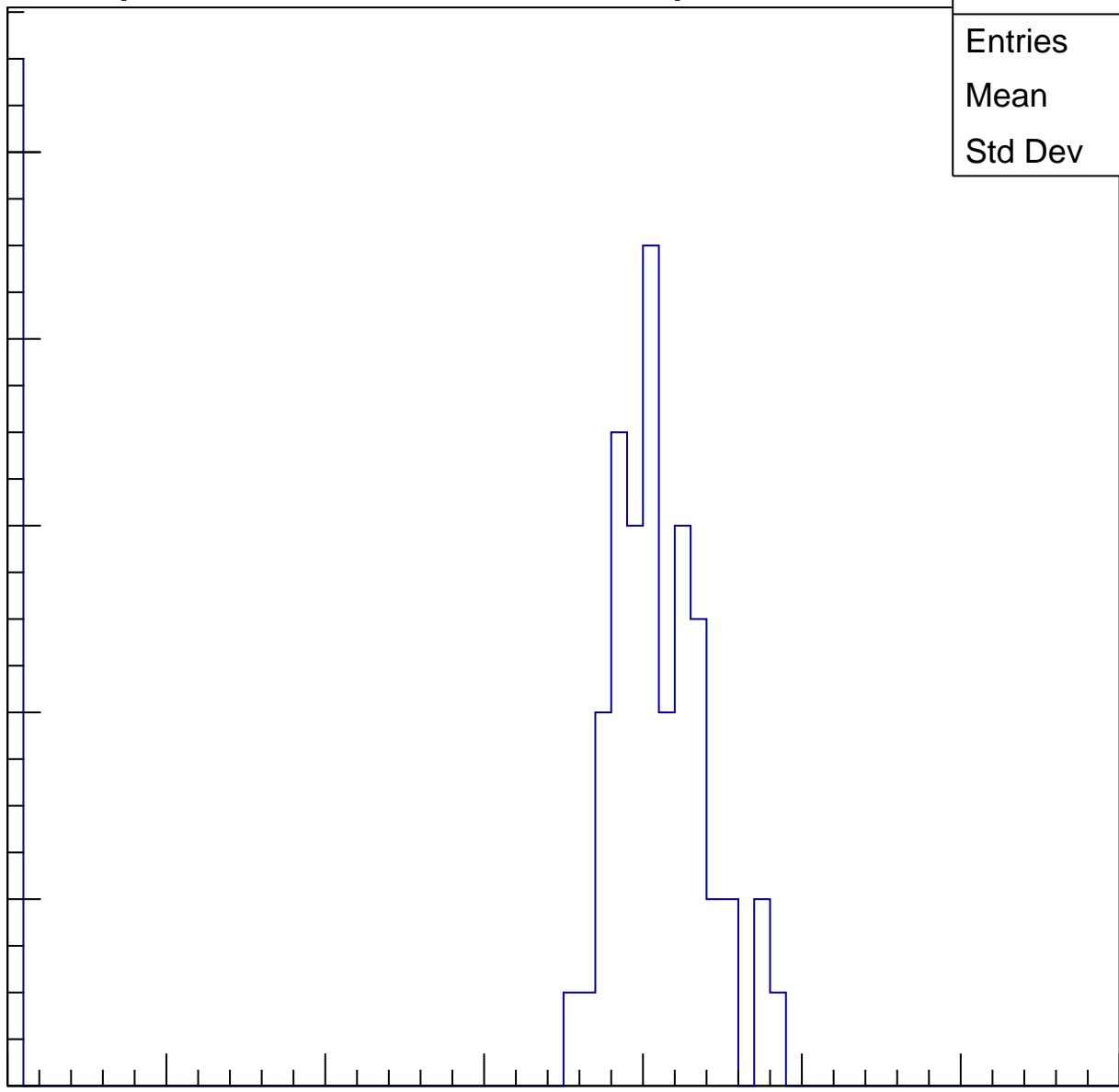
40

50

60

70

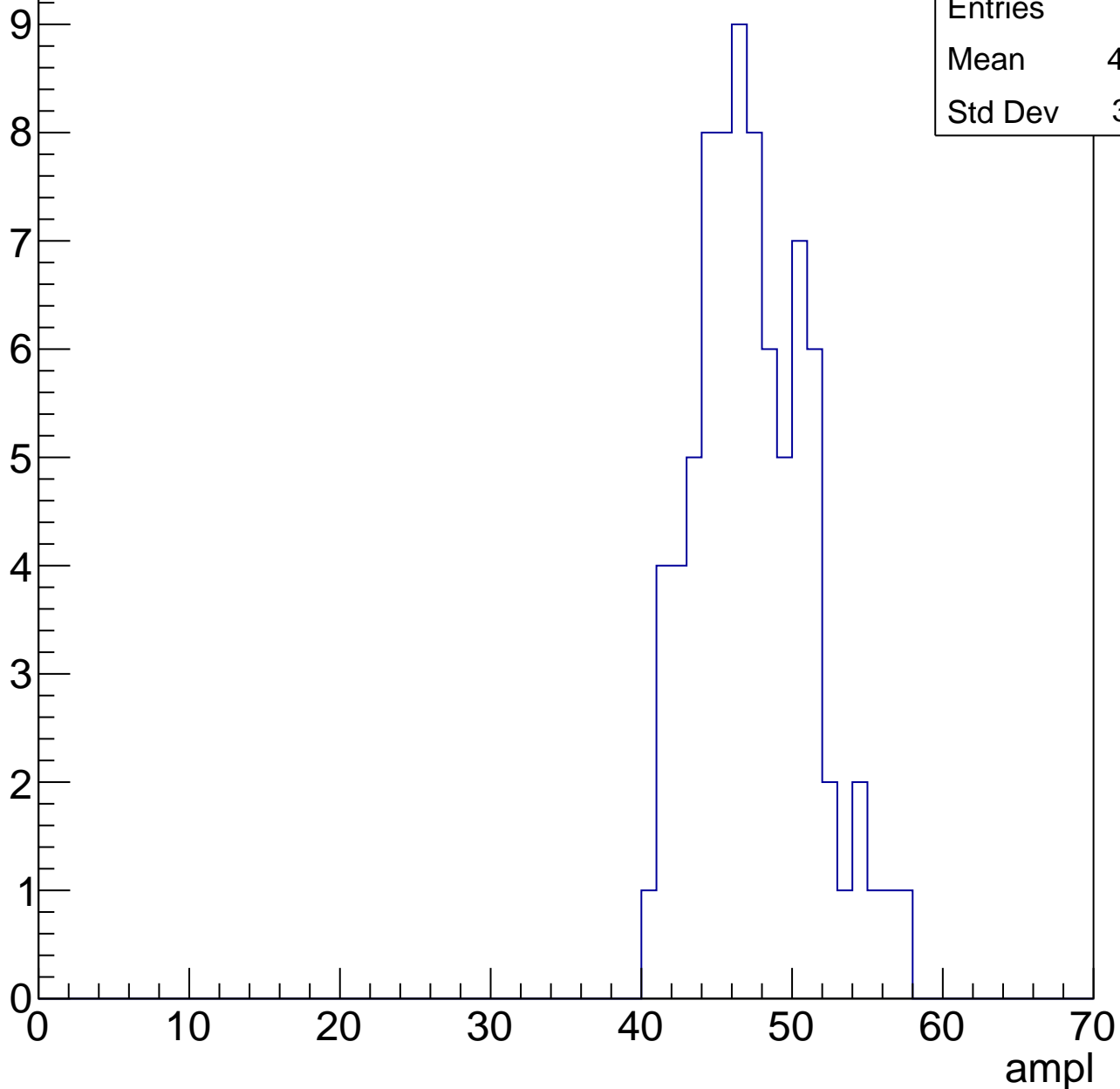
ampl



B1L103S, U23-ch62, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

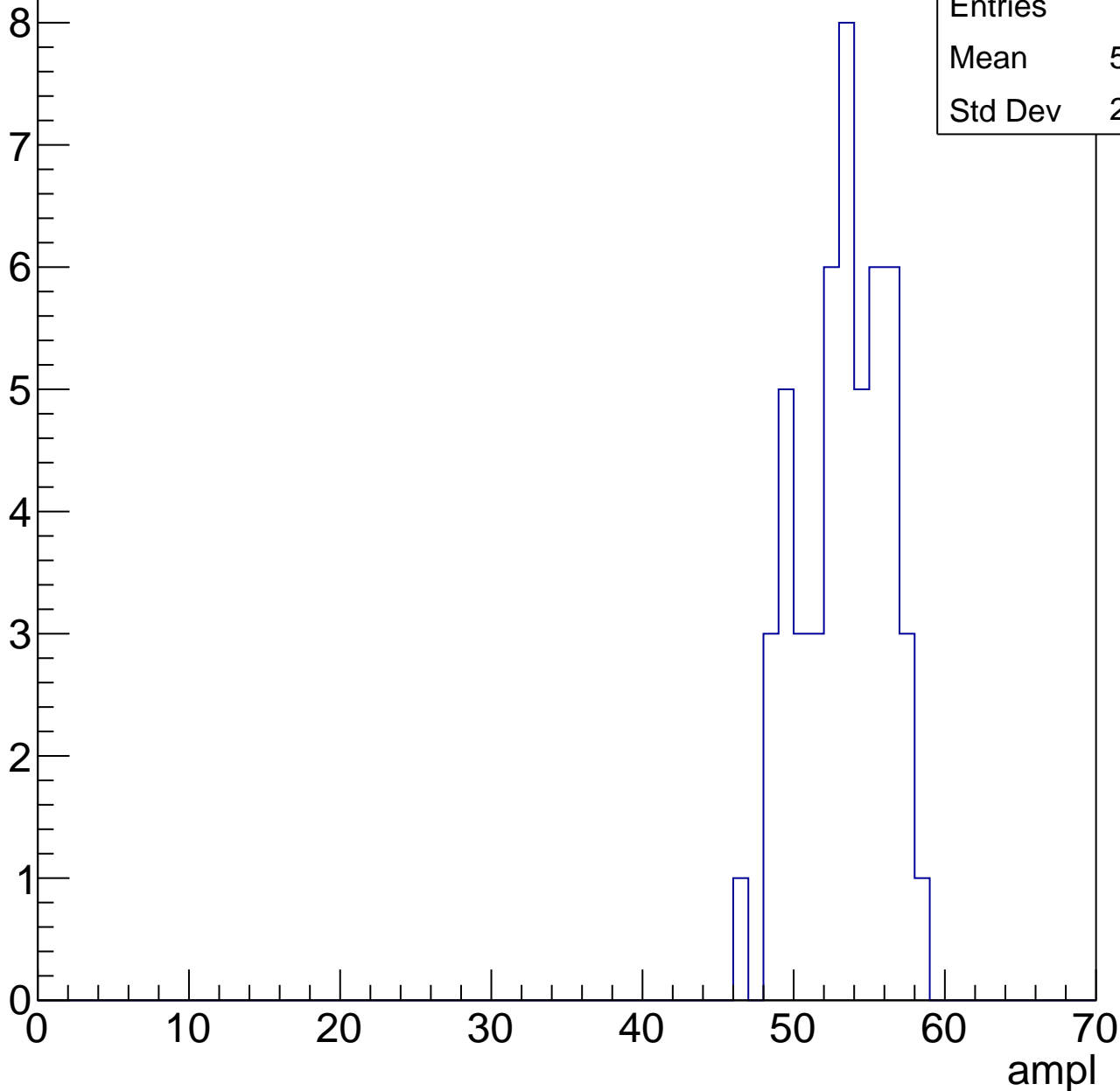


B1L103S, U23-ch62, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	50
Mean	52.78
Std Dev	2.838

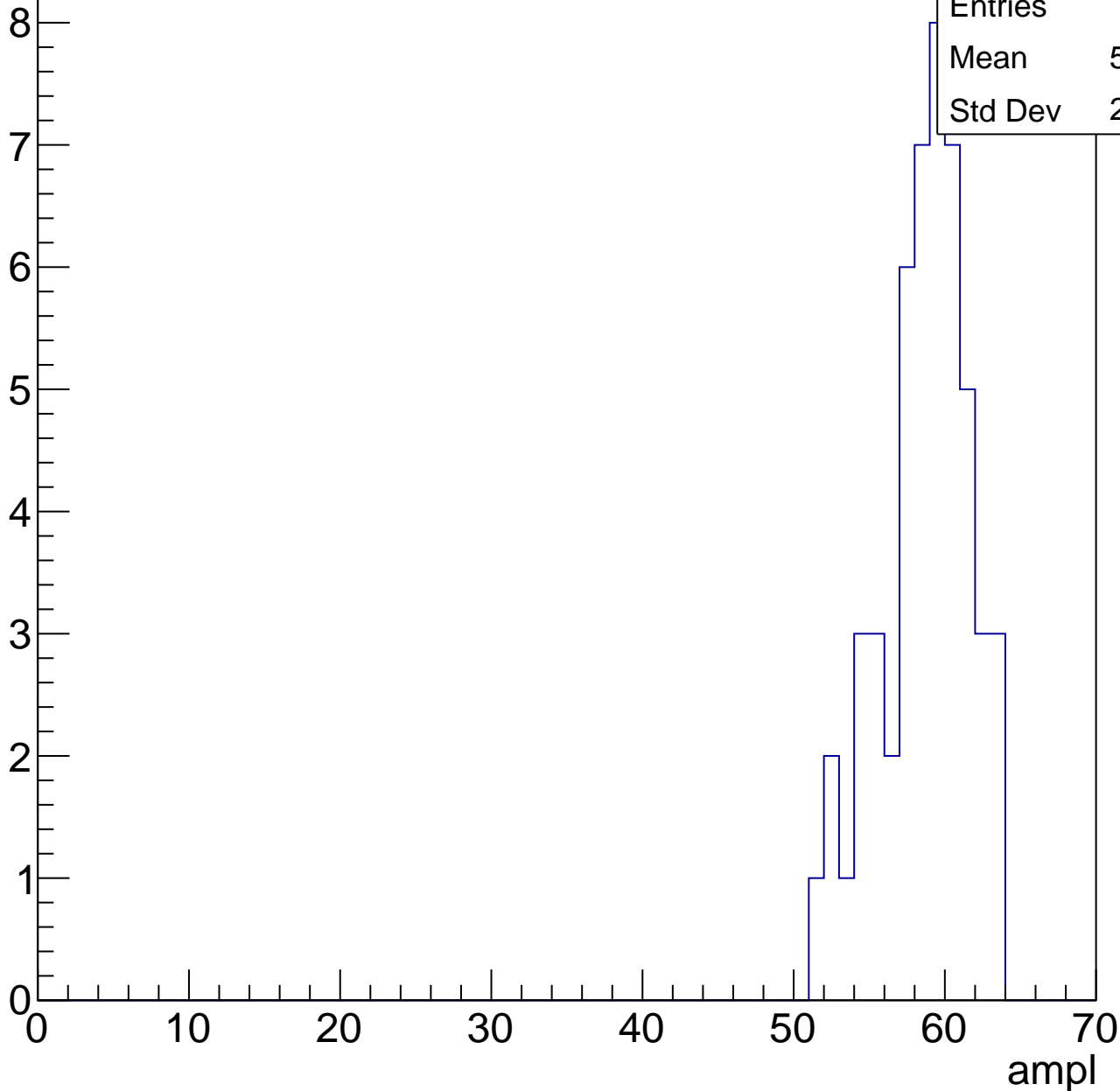


B1L103S, U23-ch62, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	51
Mean	58.18
Std Dev	2.929

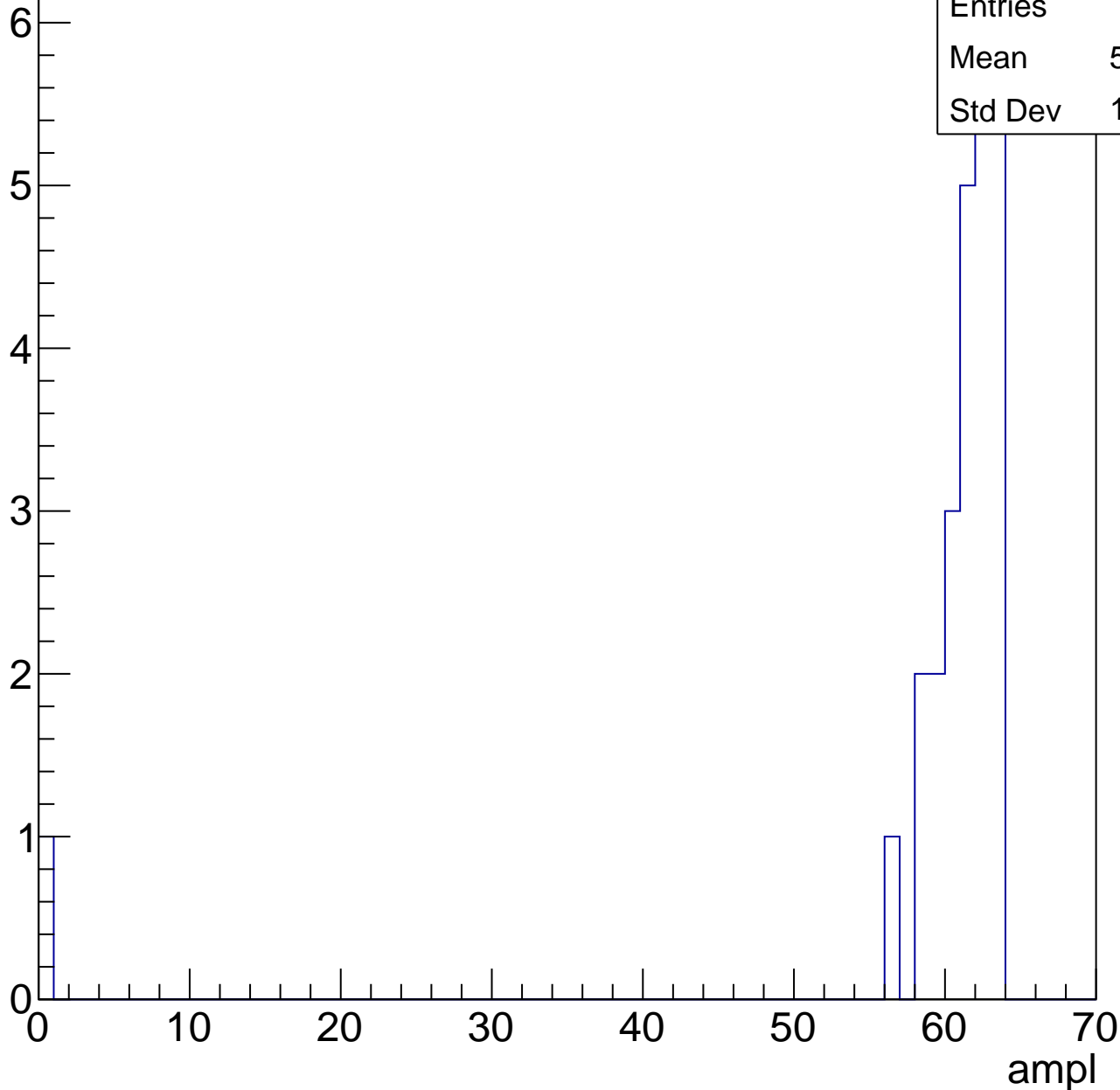


B1L103S, U23-ch62, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	26
Mean	58.65
Std Dev	11.87

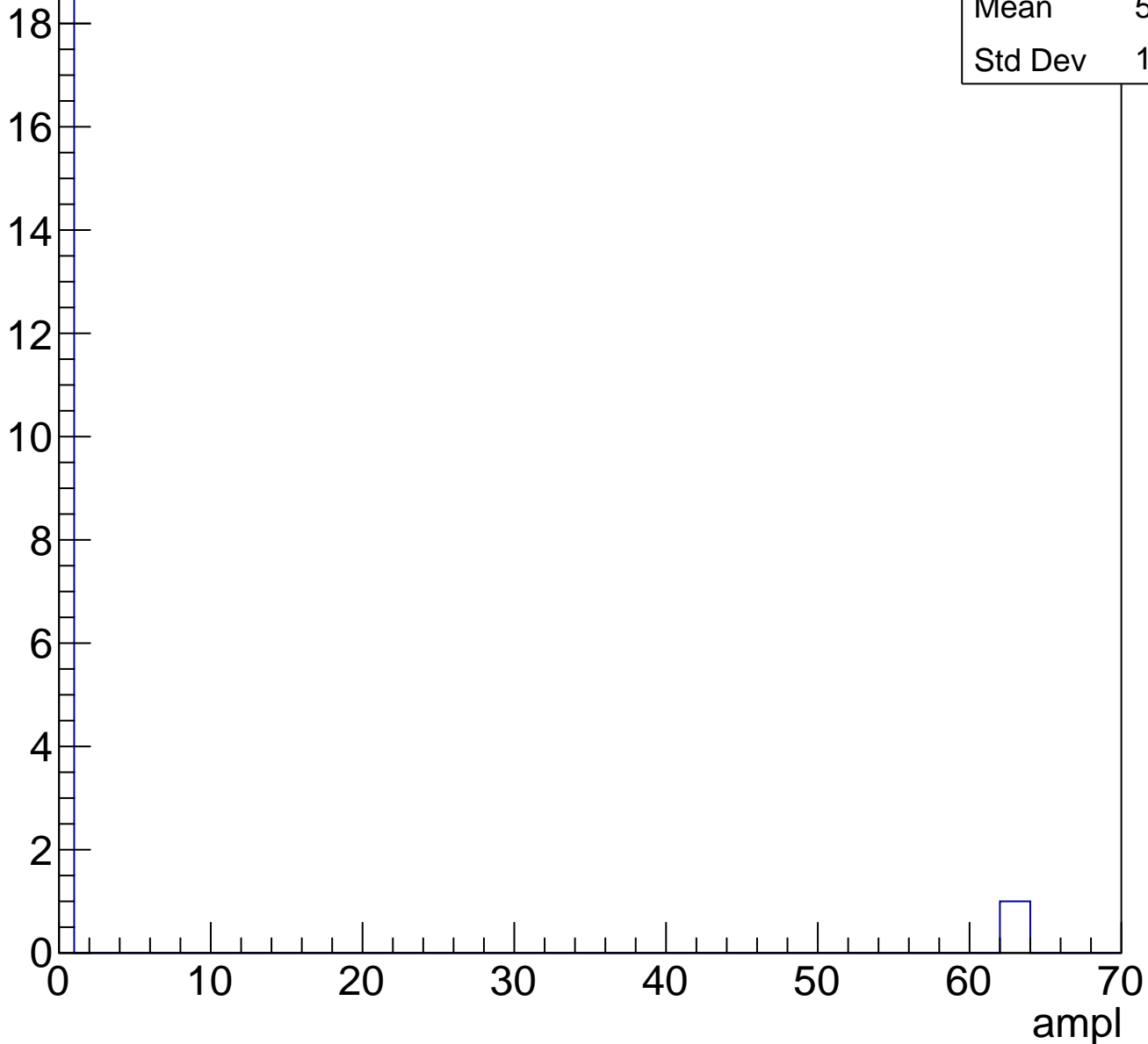


B1L103S, U23-ch62, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	21
Mean	5.952
Std Dev	18.35

Entry

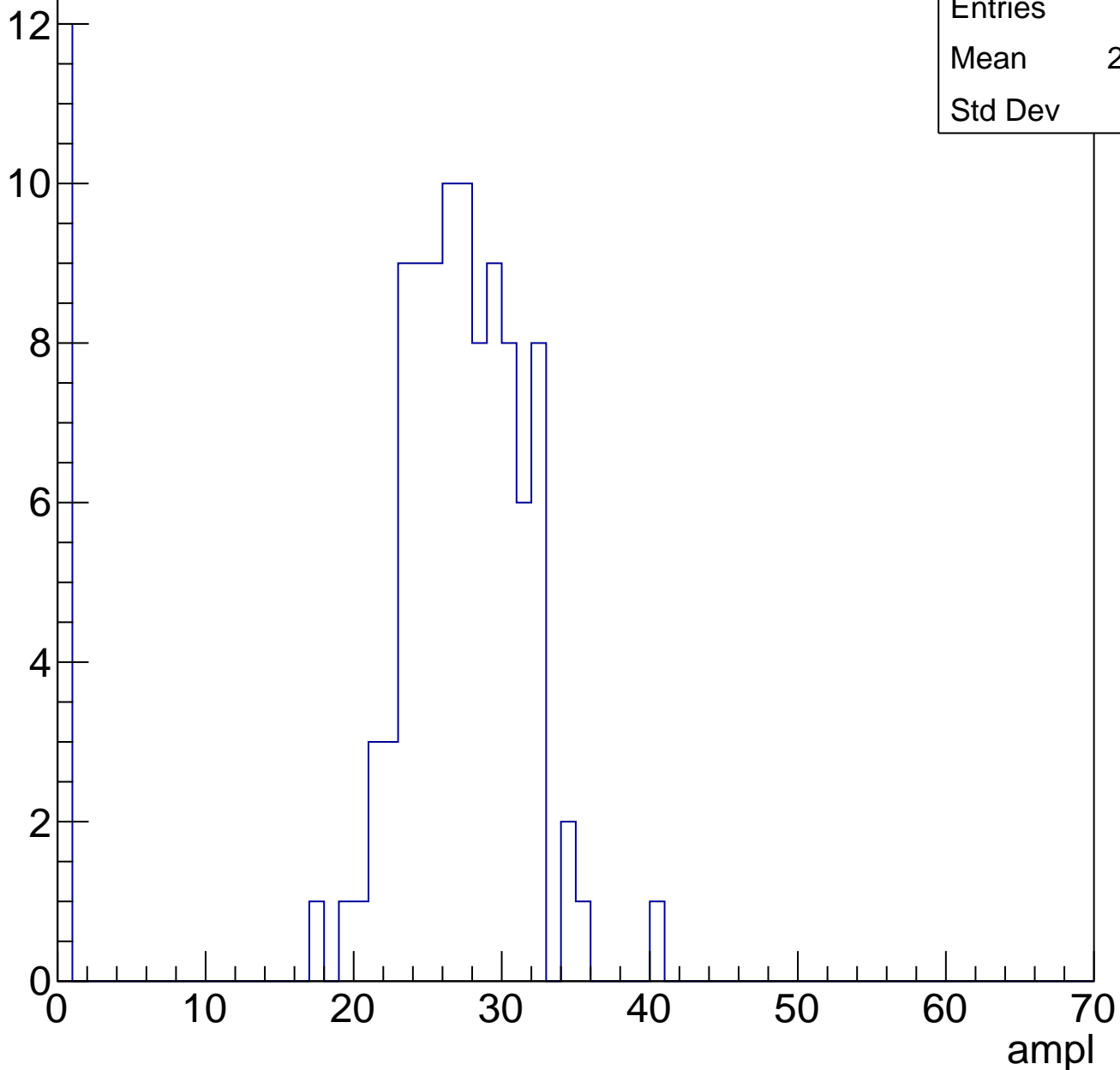


B1L103S, U23-ch63, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	111
Mean	24.08
Std Dev	9.11

Entry

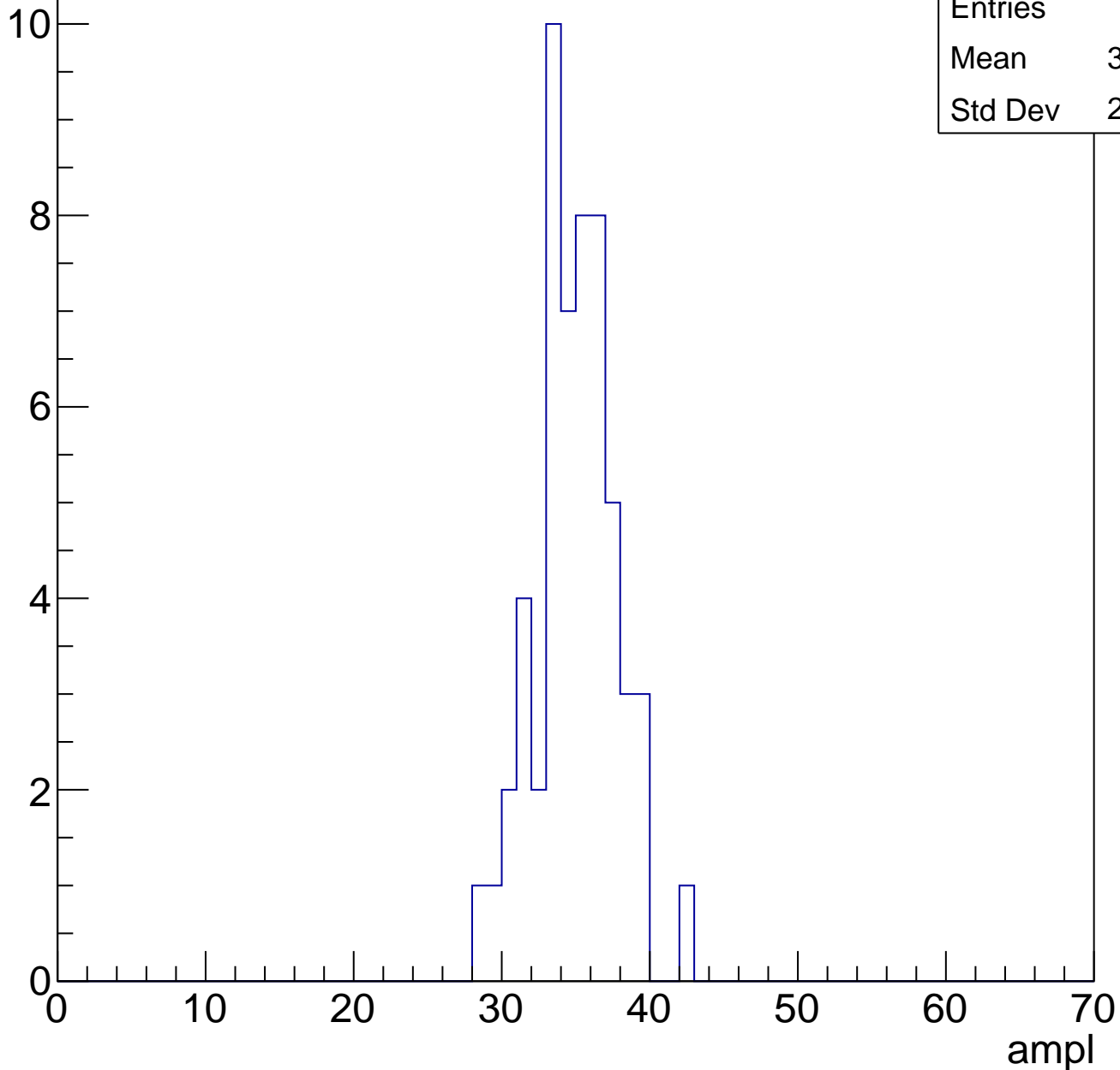


B1L103S, U23-ch63, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	55
Mean	34.53
Std Dev	2.709

Entry

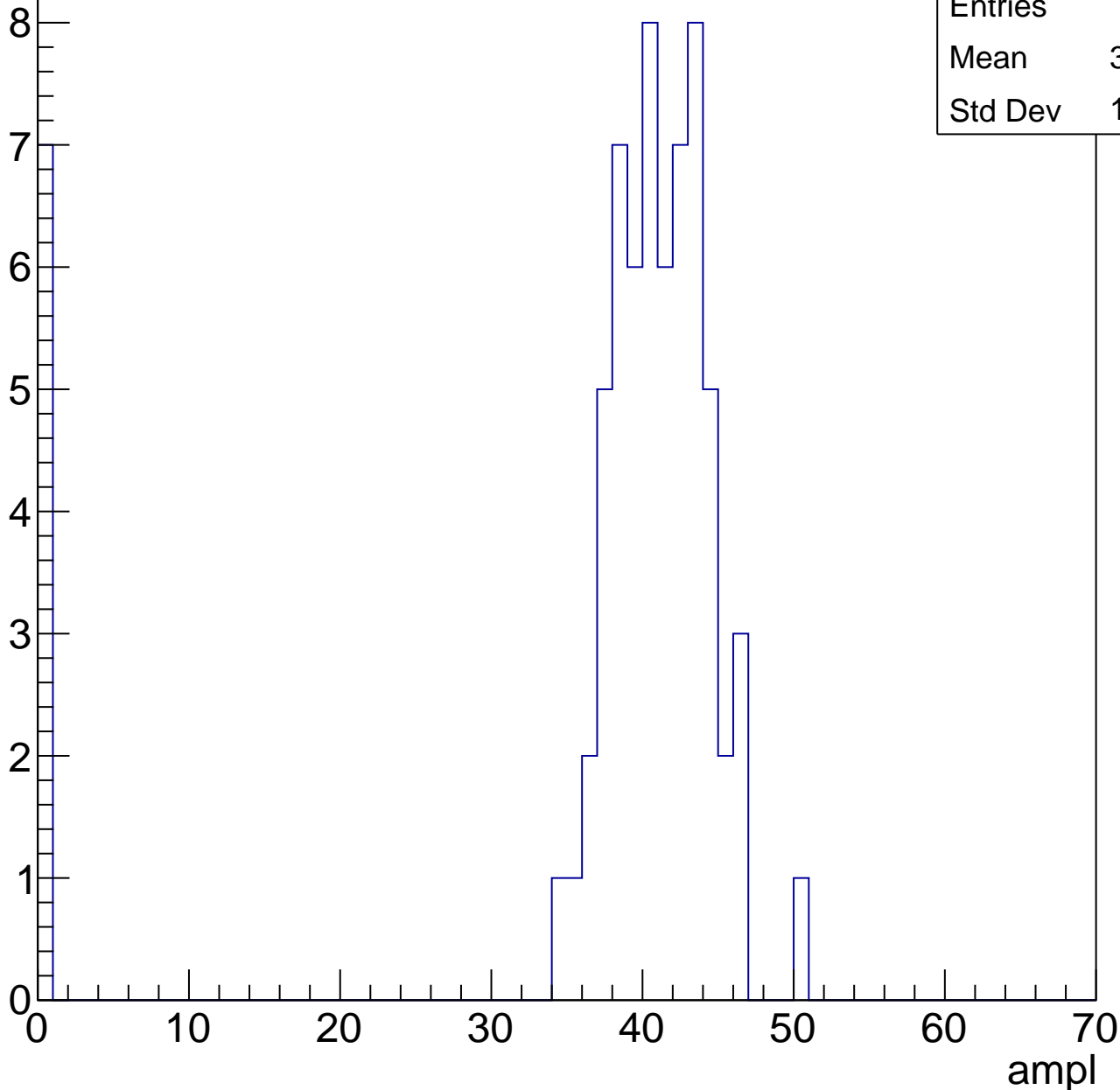


B1L103S, U23-ch63, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	36.64
Std Dev	12.65

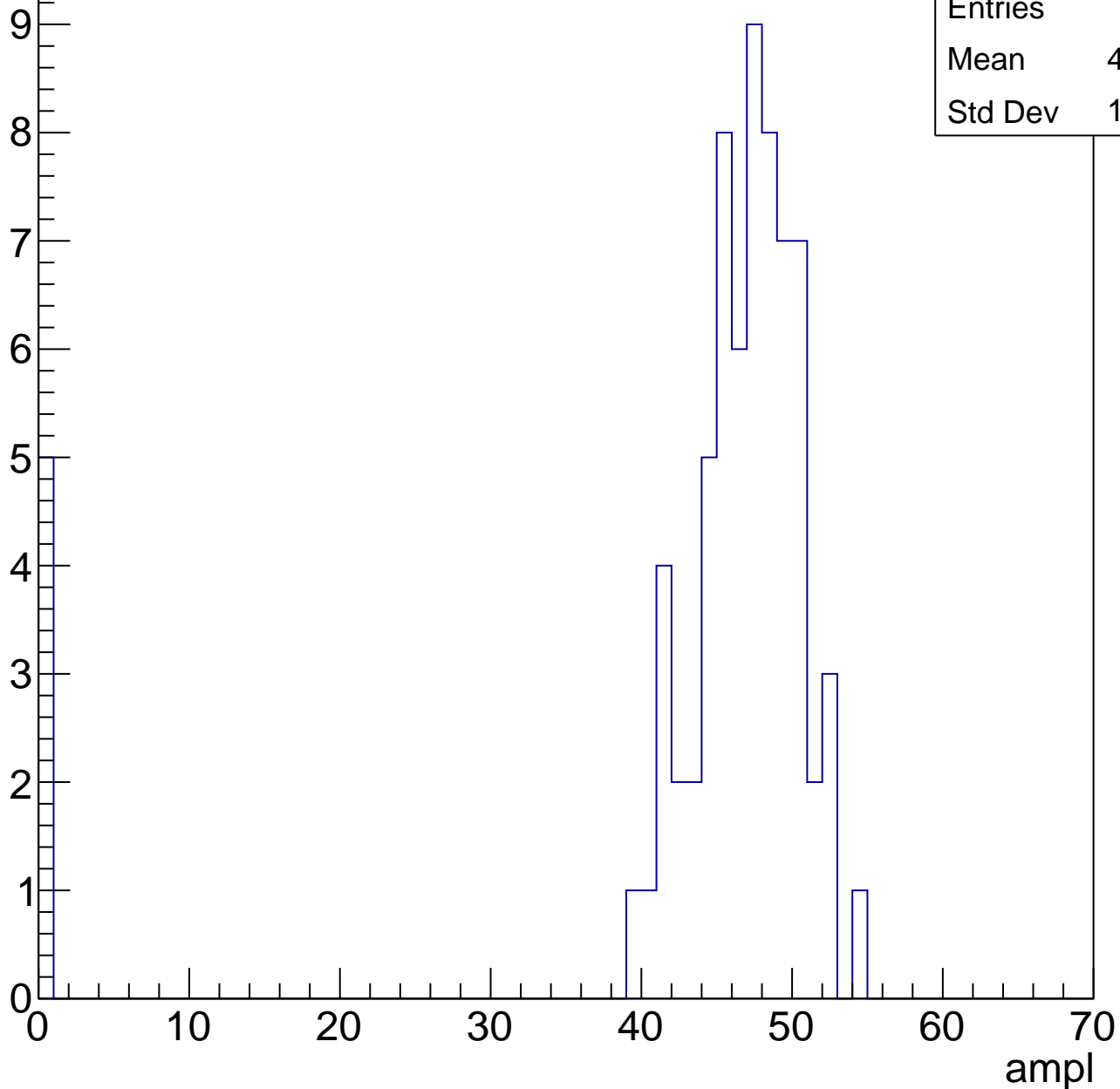


B1L103S, U23-ch63, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	43.39
Std Dev	12.33

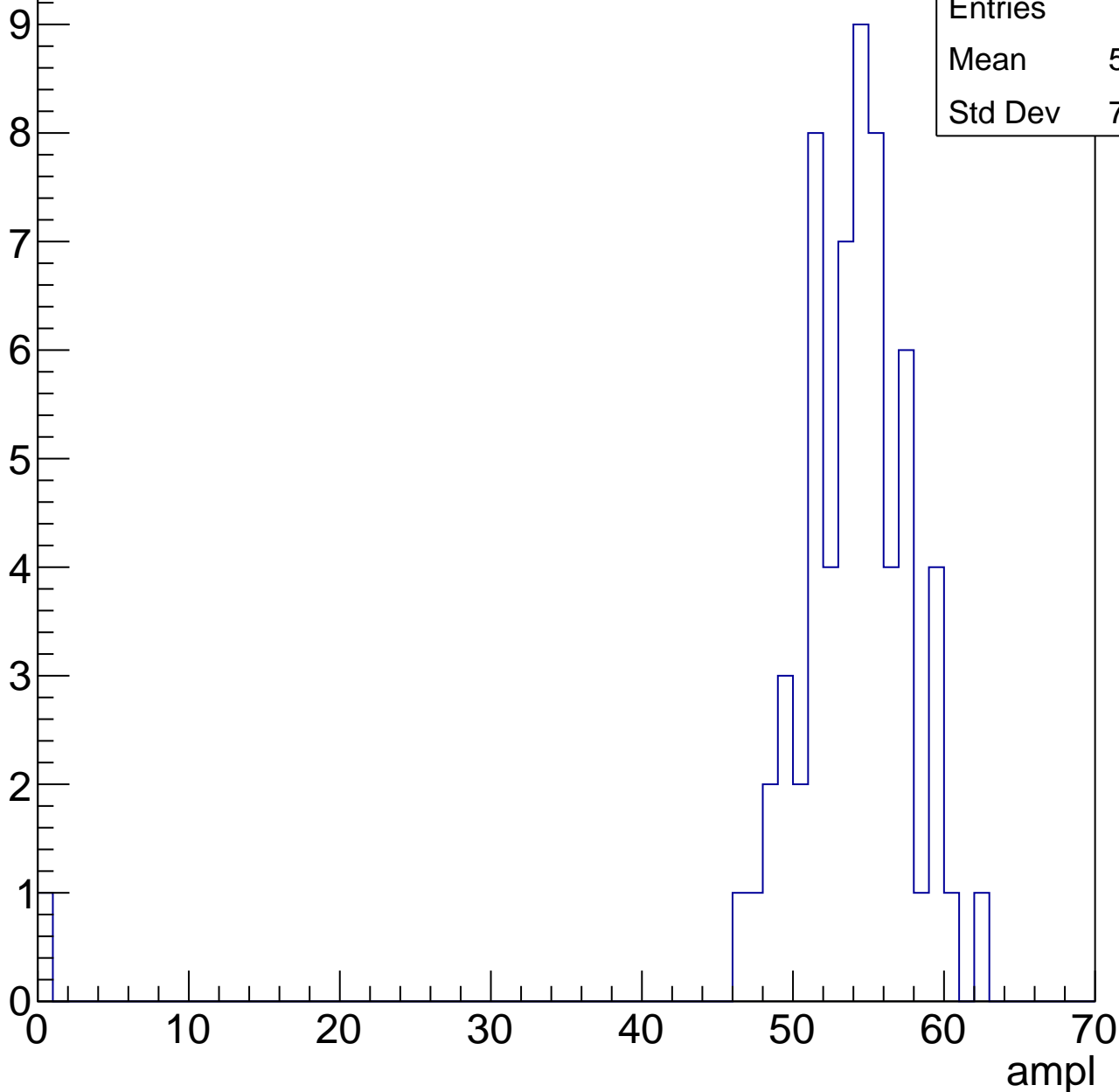


B1L103S, U23-ch63, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	63
Mean	52.87
Std Dev	7.472

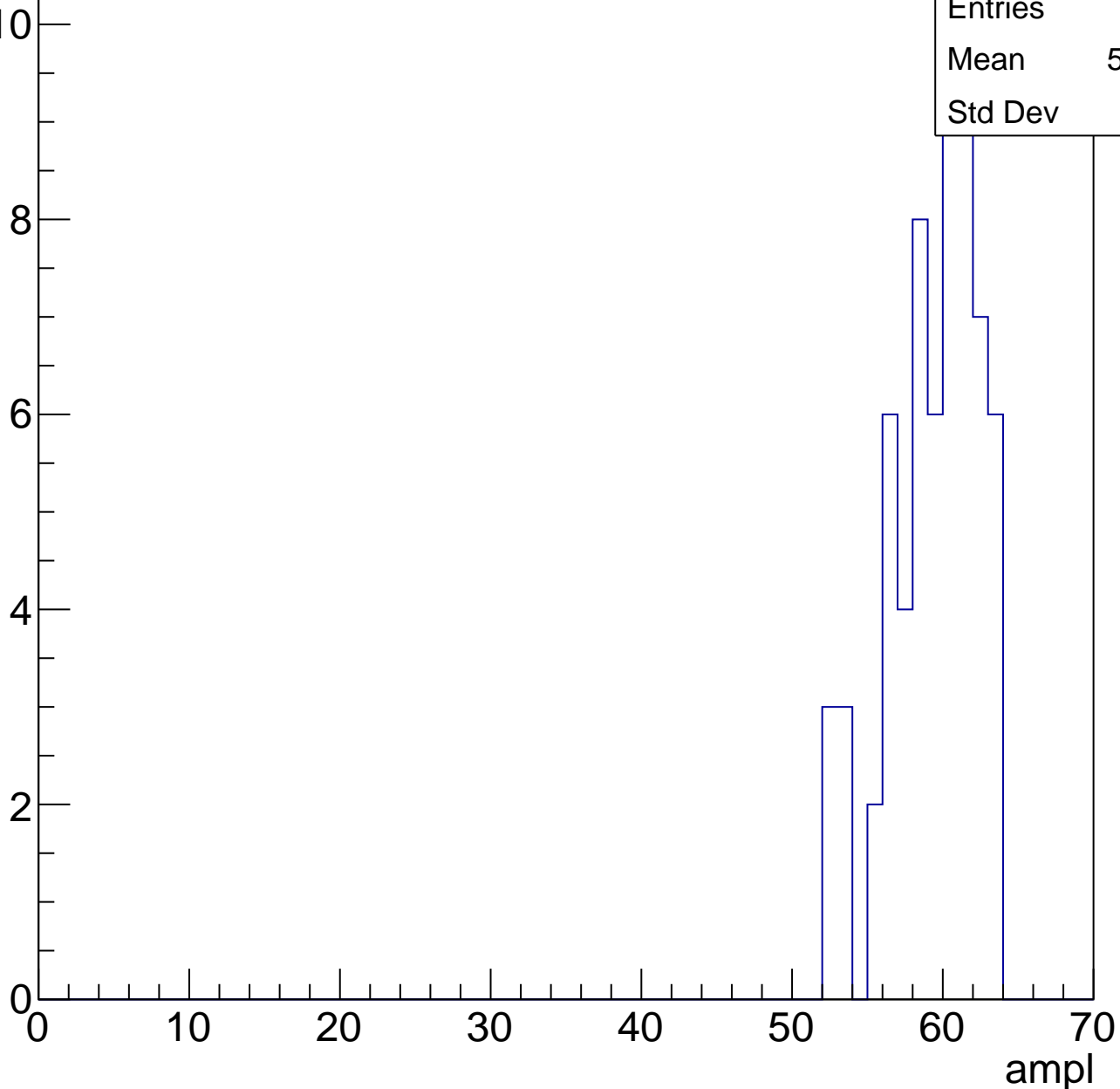


B1L103S, U23-ch63, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

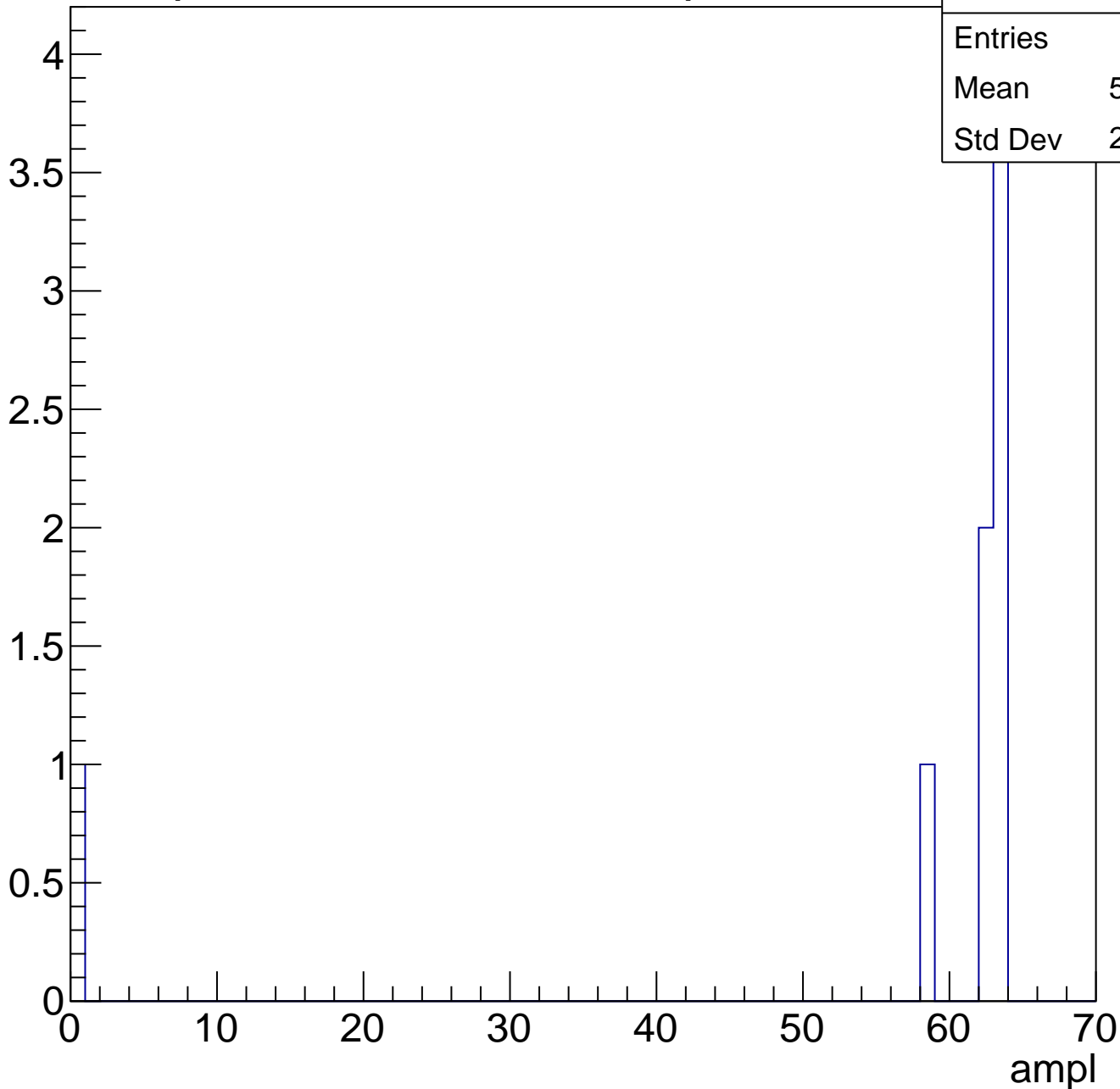
Entries	64
Mean	58.89
Std Dev	2.99



B1L103S, U23-ch63, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch63, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



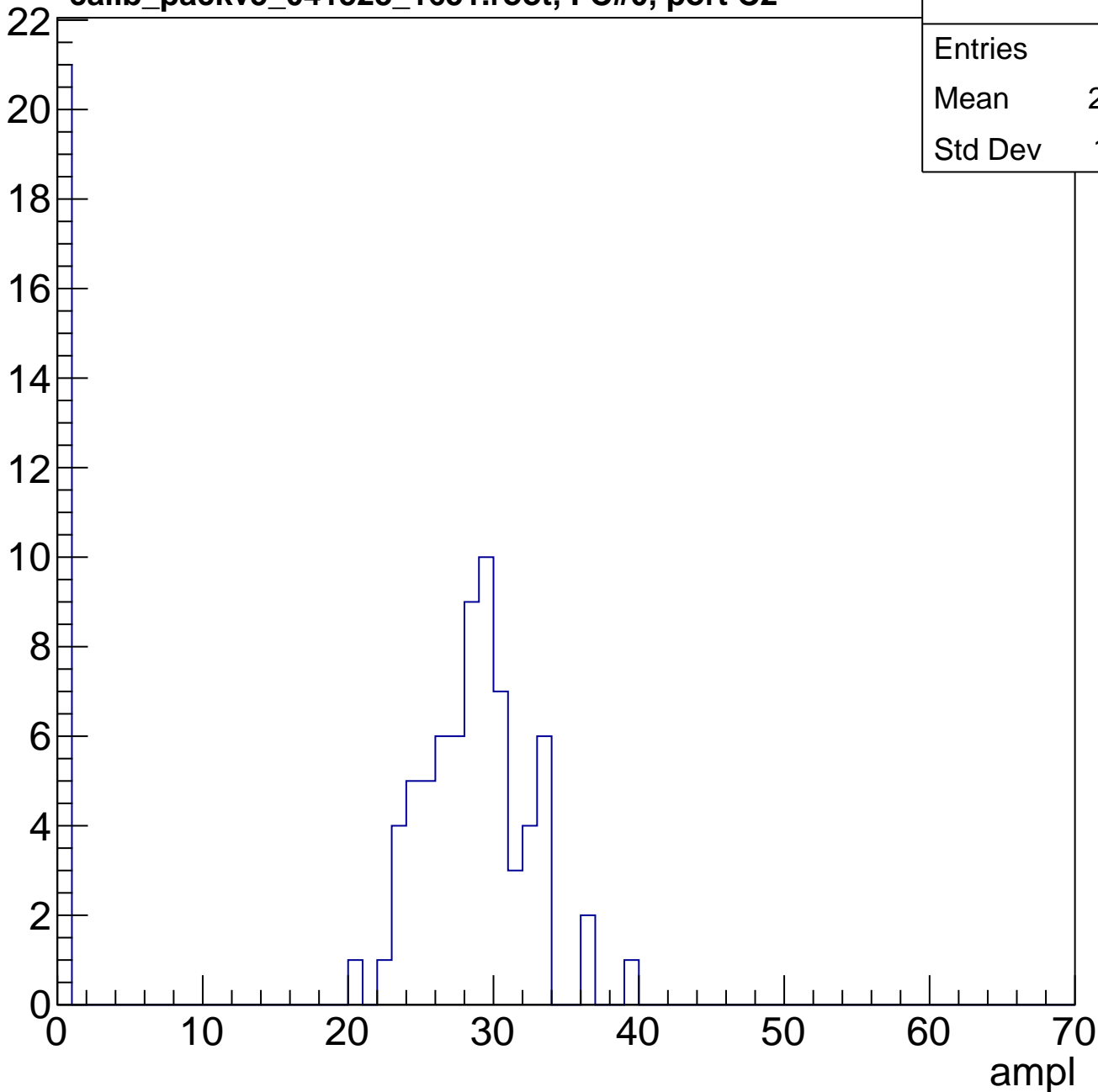
Entries	19
Mean	0
Std Dev	0

B1L103S, U23-ch64, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	91
Mean	21.75
Std Dev	12.31

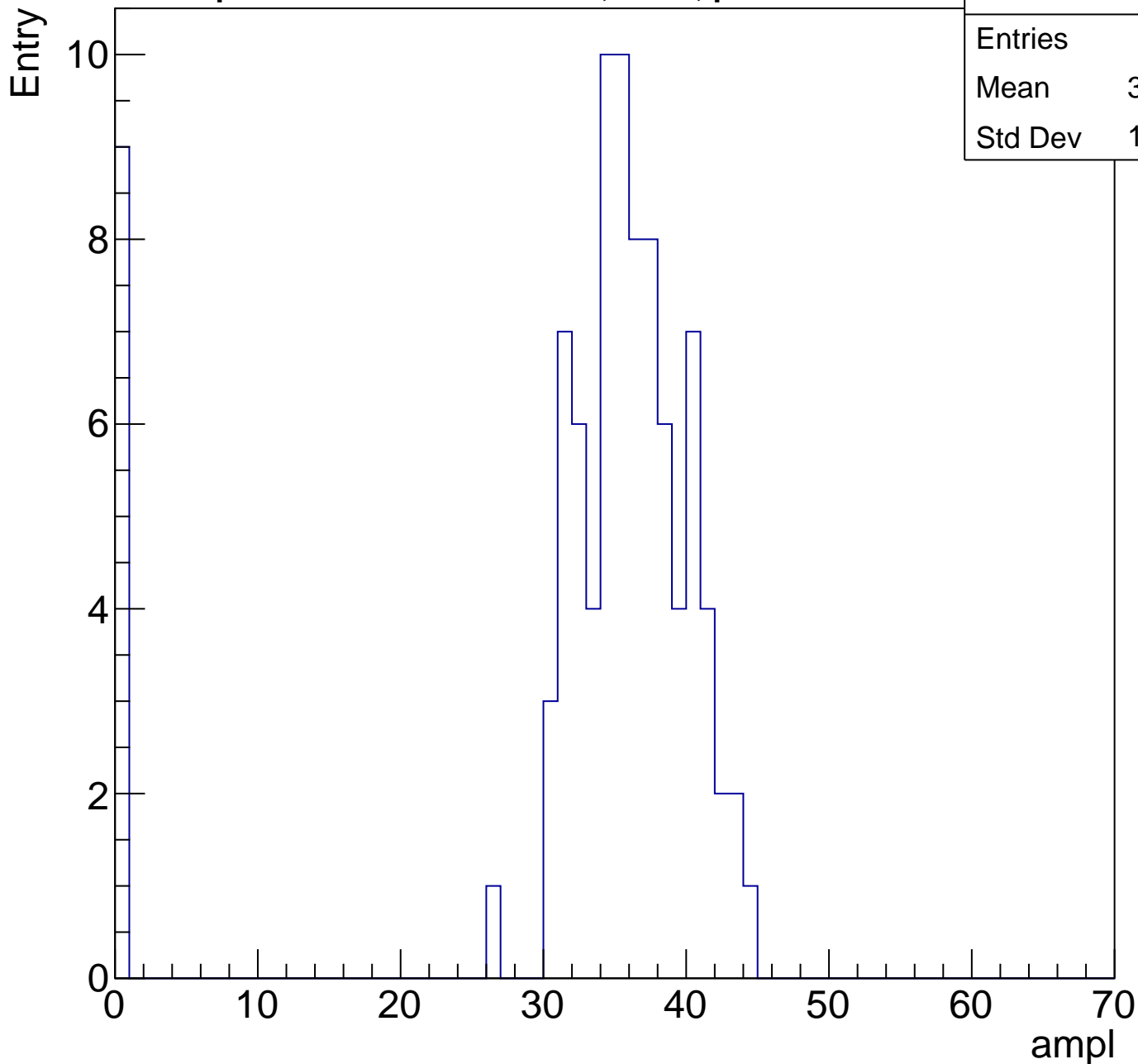
Entry



B1L103S, U23-ch64, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	92
Mean	32.32
Std Dev	11.18

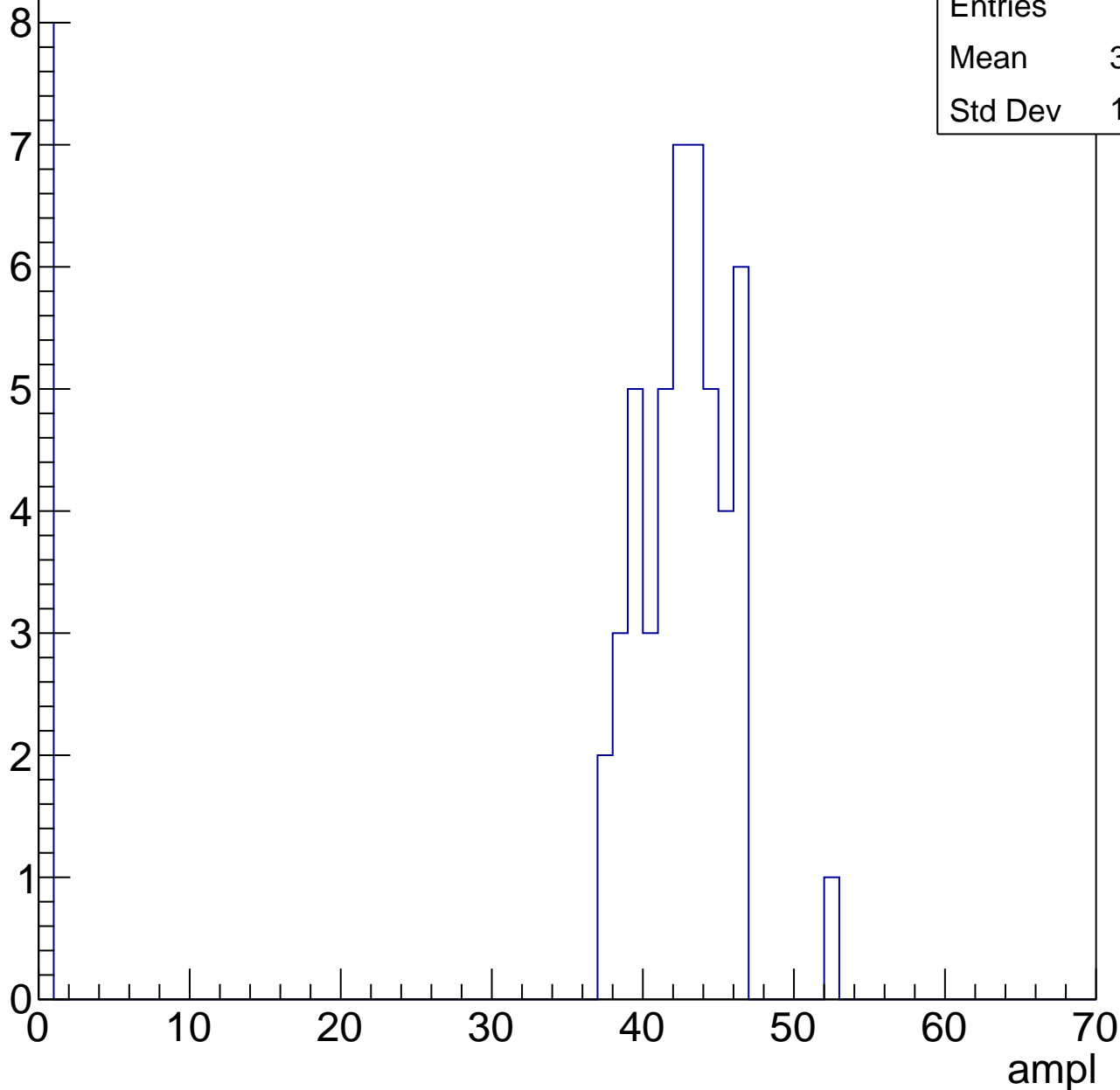


B1L103S, U23-ch64, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	56
Mean	36.27
Std Dev	15.05

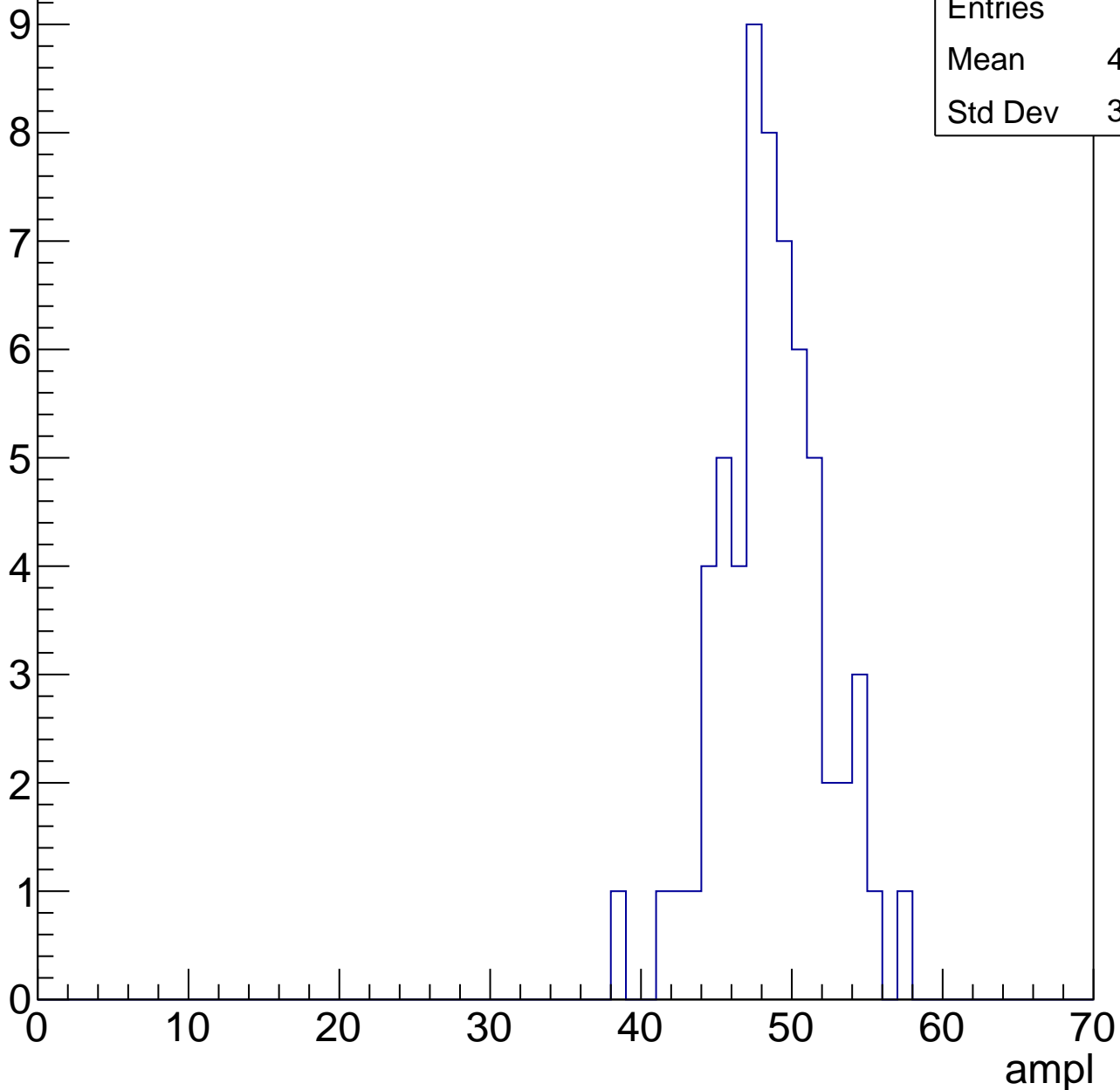


B1L103S, U23-ch64, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	48.16
Std Dev	3.479

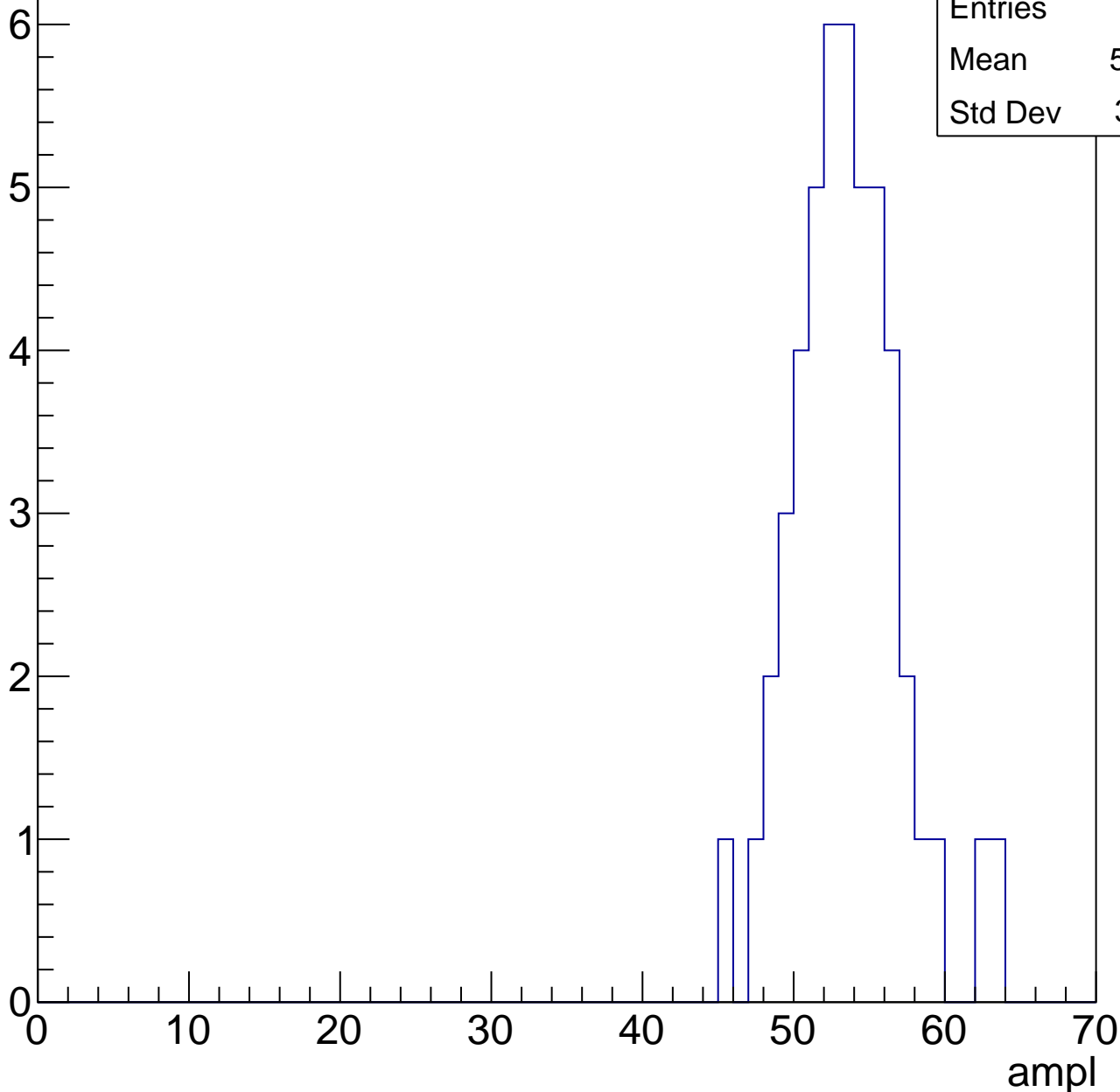


B1L103S, U23-ch64, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	48
Mean	53.02
Std Dev	3.521

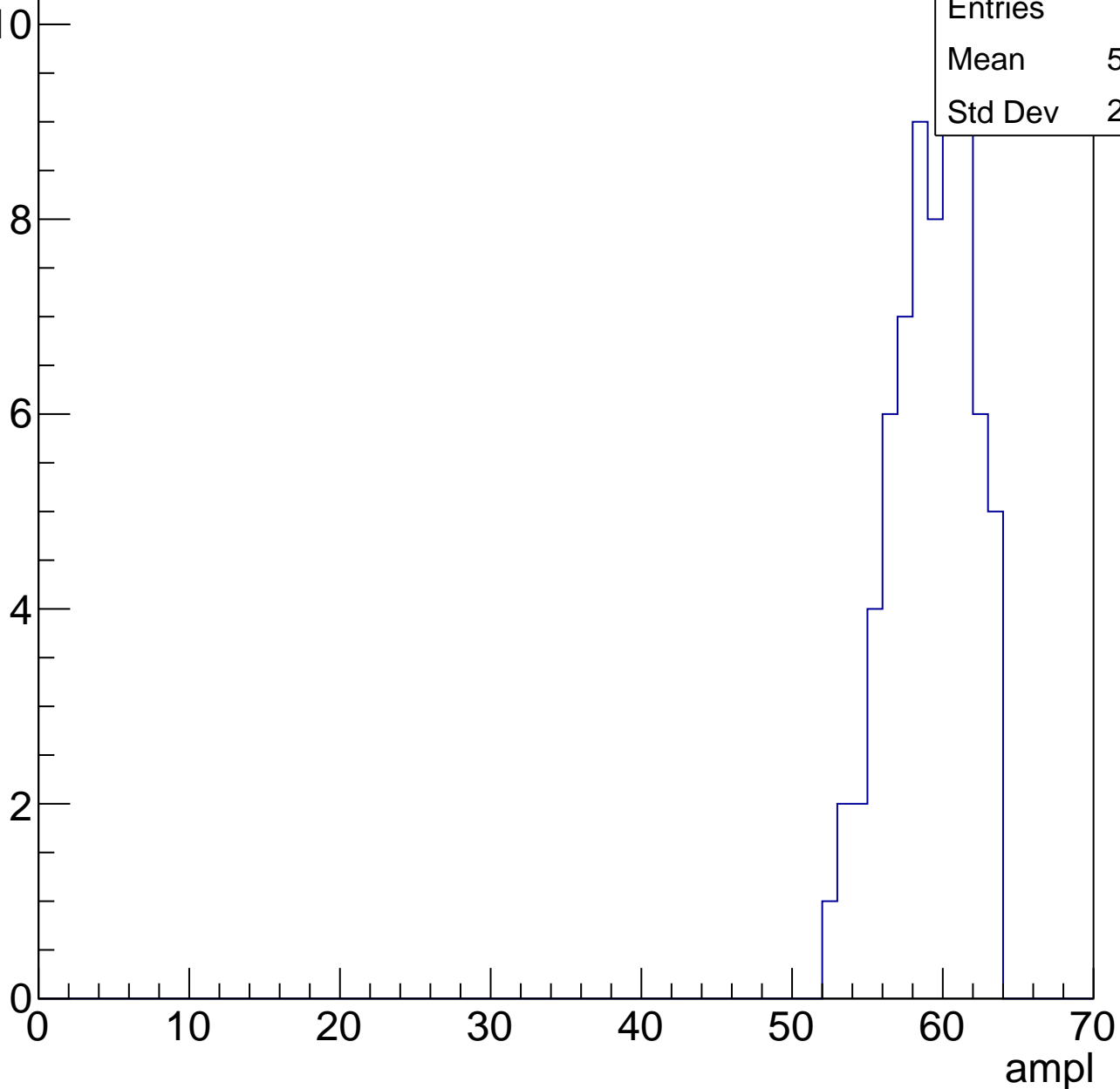


B1L103S, U23-ch64, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

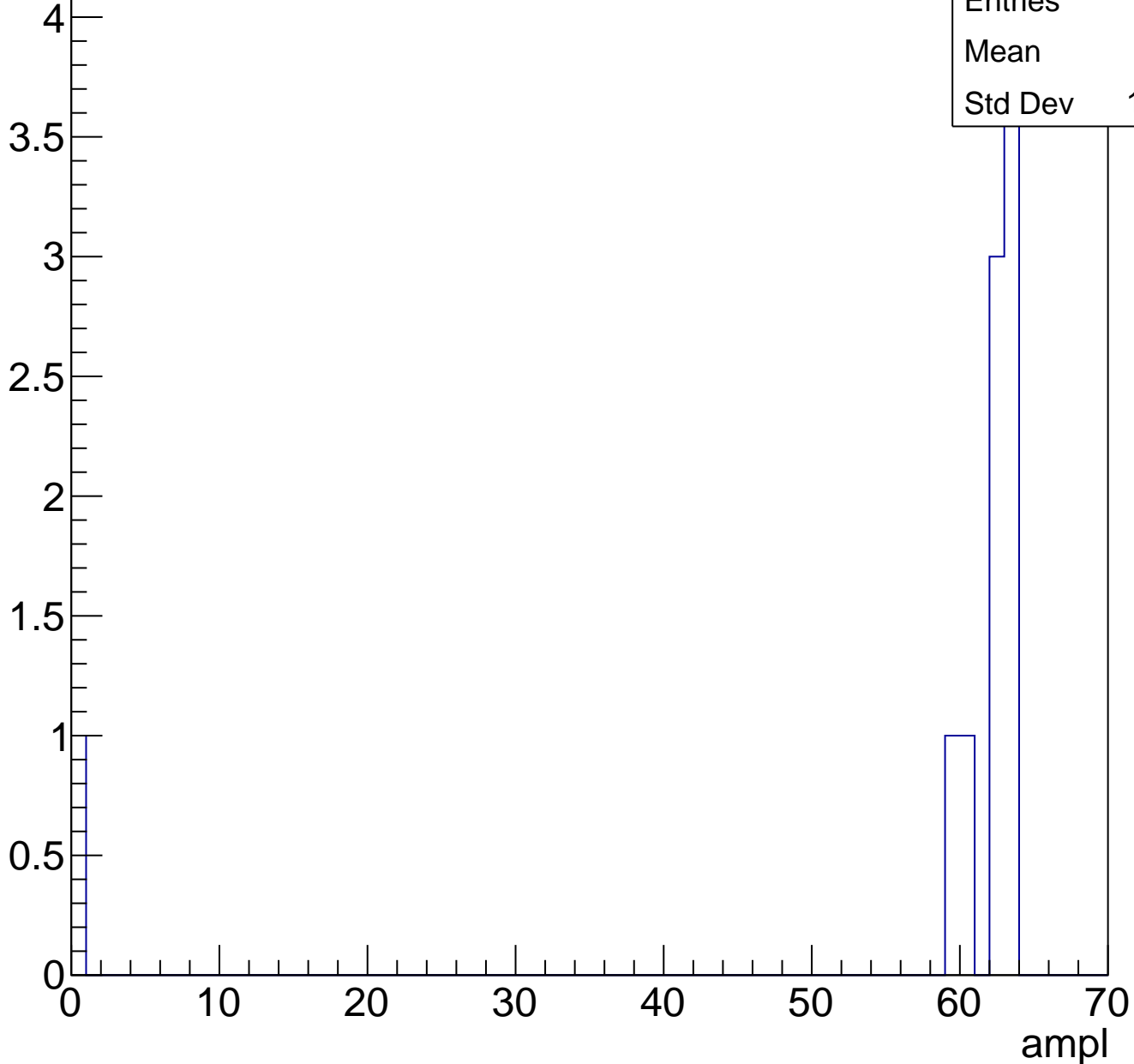
Entries	69
Mean	58.72
Std Dev	2.702



B1L103S, U23-ch64, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch64, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

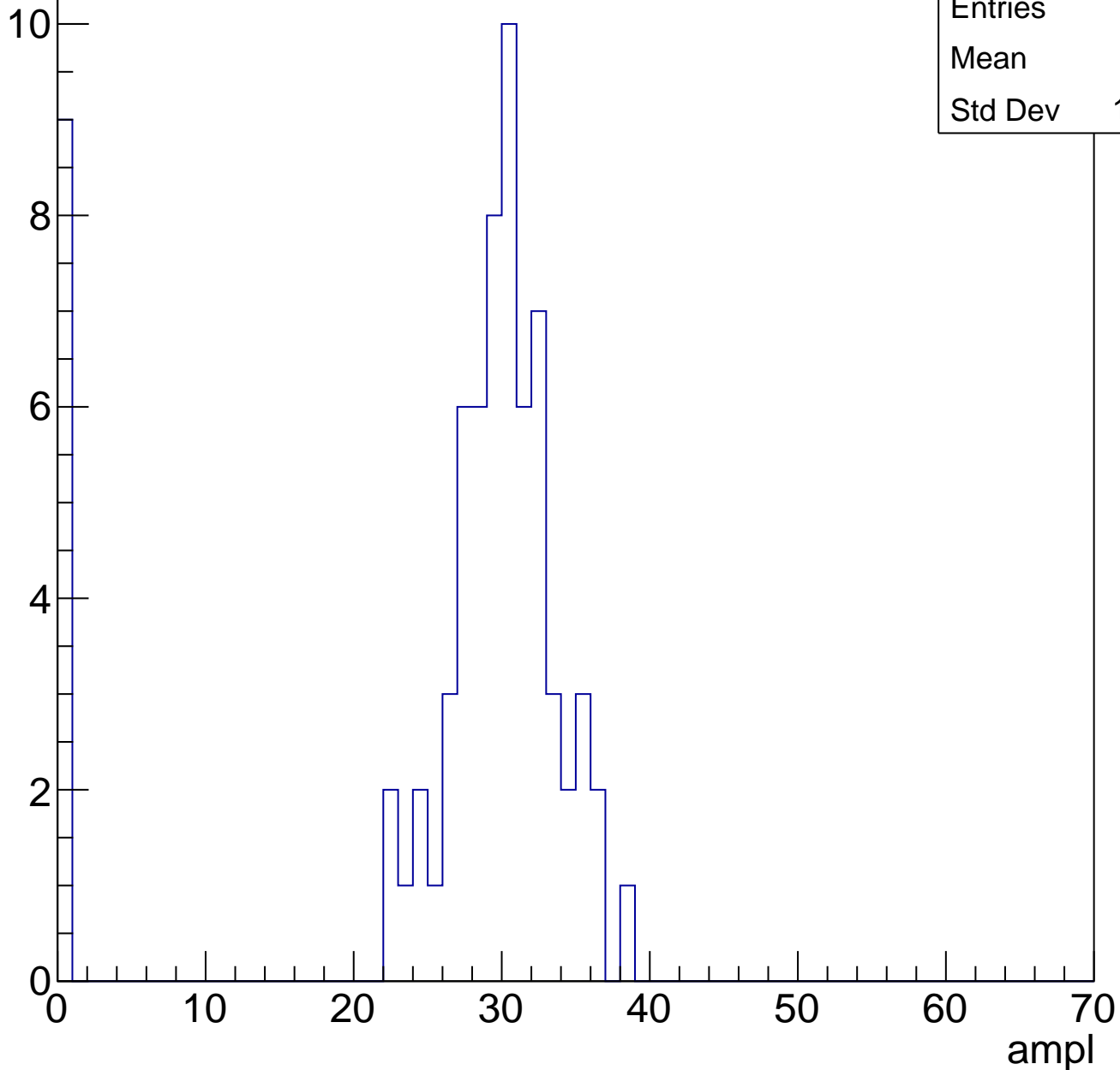
Entries	19
Mean	0
Std Dev	0

B1L103S, U23-ch65, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	72
Mean	26
Std Dev	10.31

Entry



B1L103S, U23-ch65, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	88
Mean	32.1
Std Dev	12.63

Entry

10

8

6

4

2

0

0

10

20

30

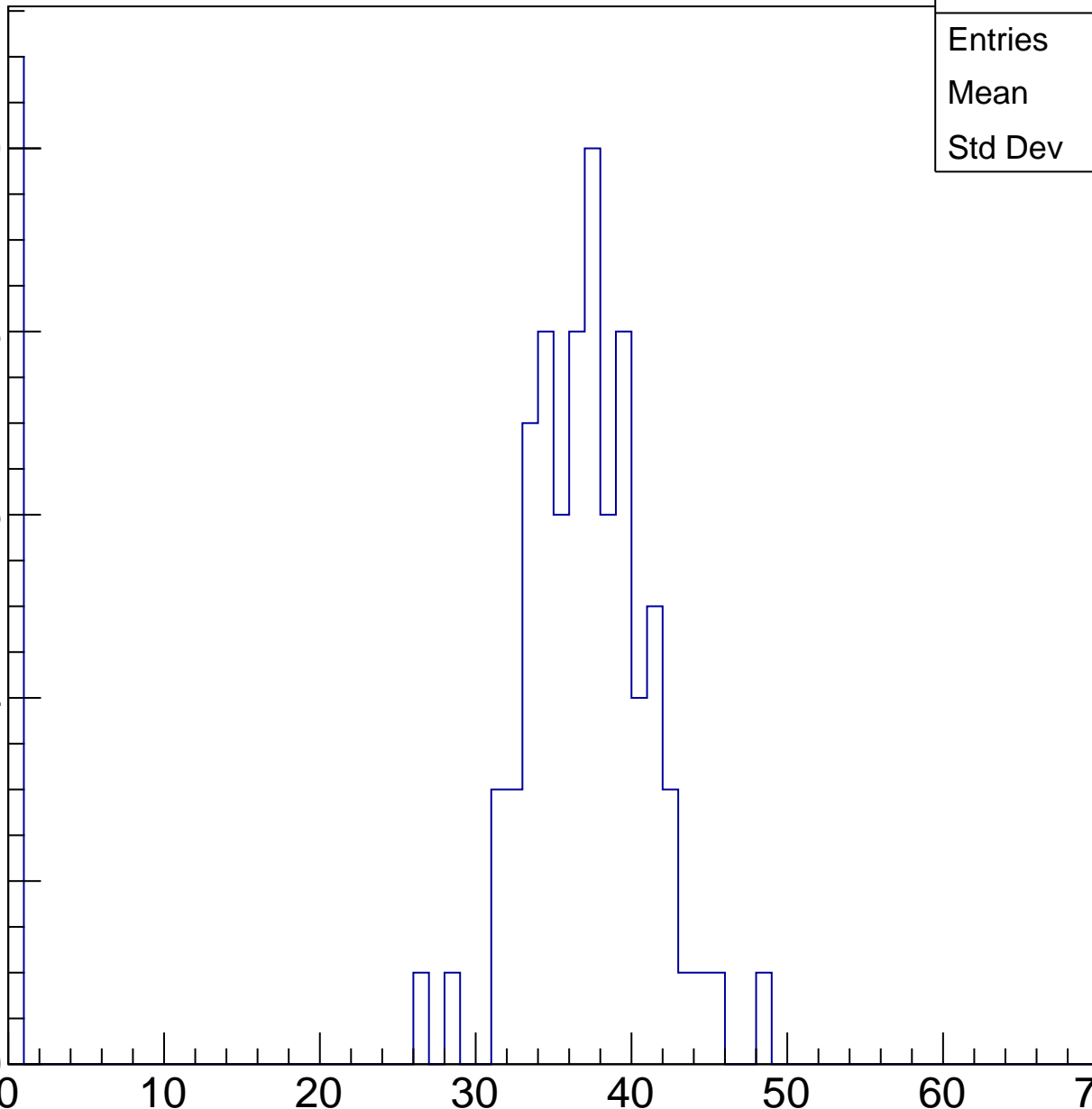
40

50

60

70

ampl

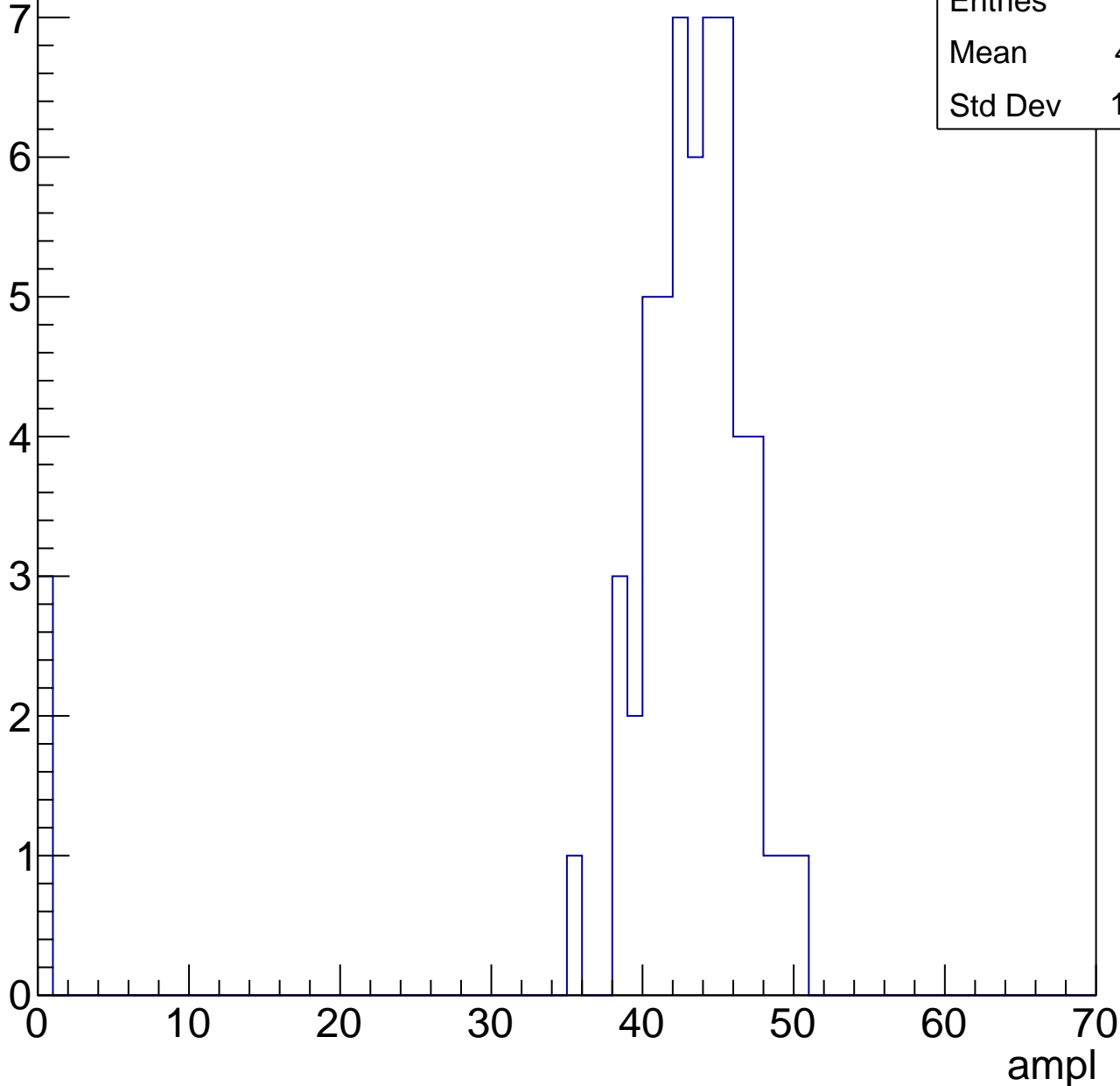


B1L103S, U23-ch65, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	57
Mean	40.81
Std Dev	10.05

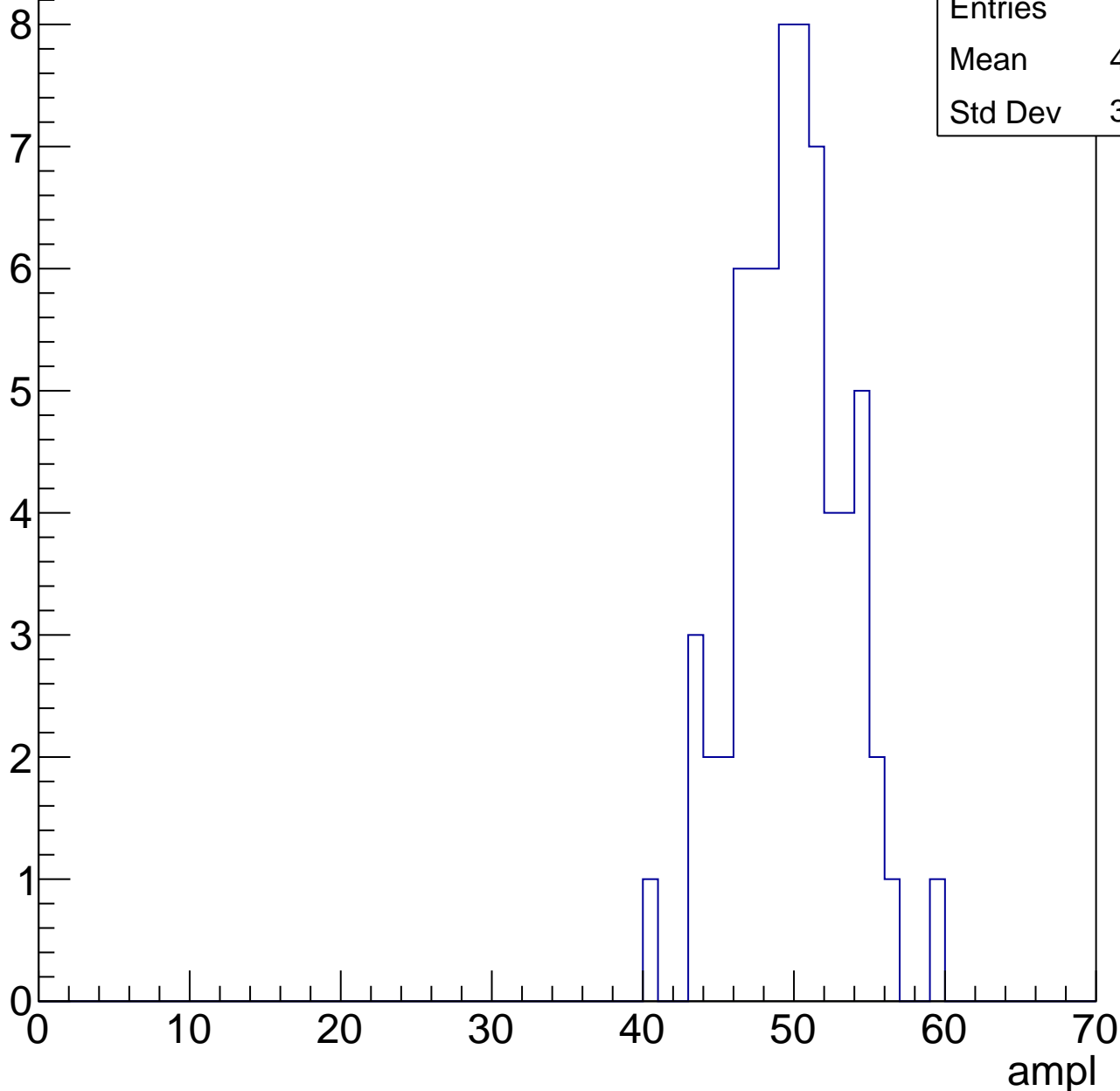


B1L103S, U23-ch65, adc3

calib_packv5_041523_1651.root, FC#0, port C2

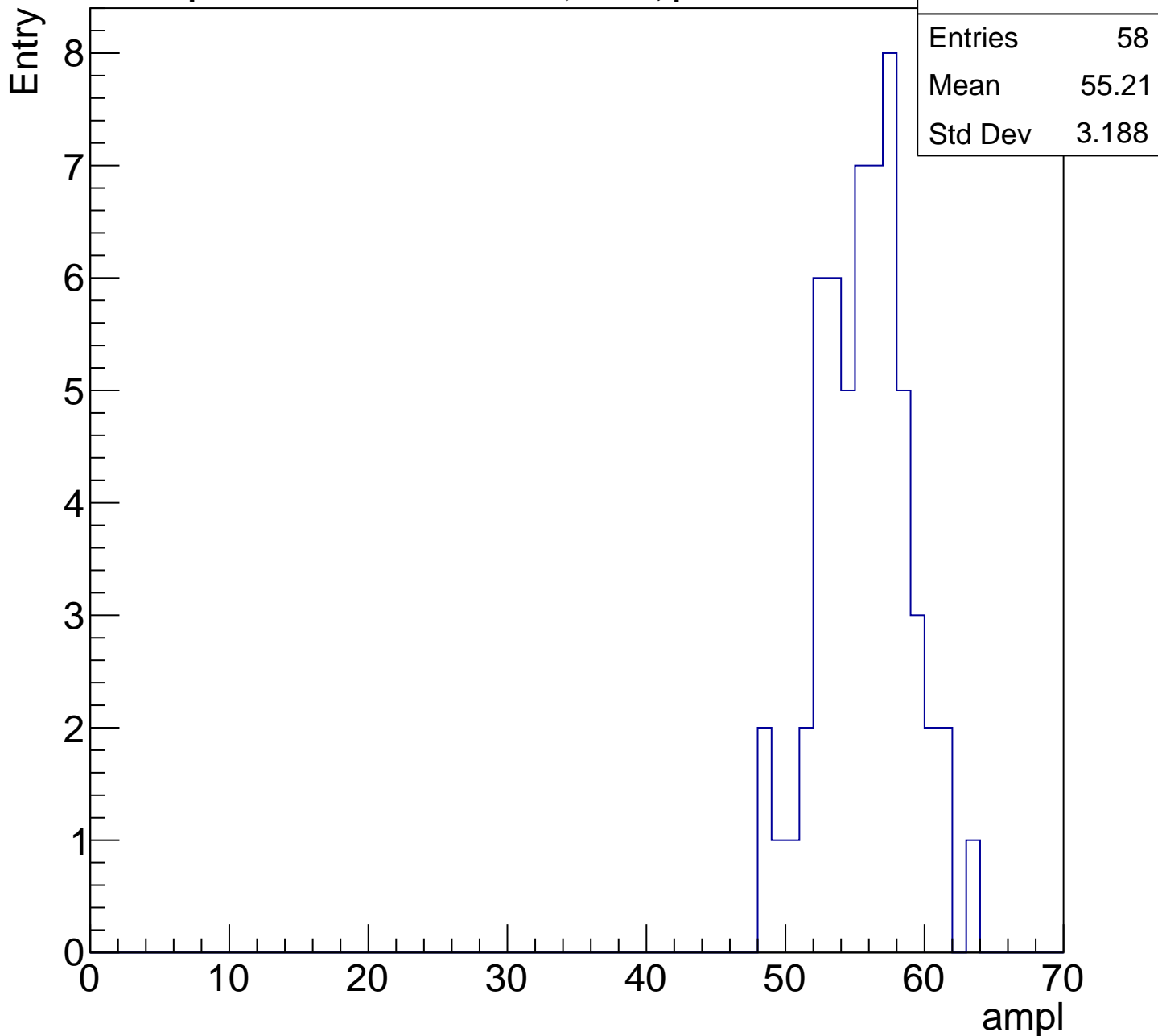
Entry

Entries	66
Mean	49.35
Std Dev	3.544



B1L103S, U23-ch65, adc4

calib_packv5_041523_1651.root, FC#0, port C2

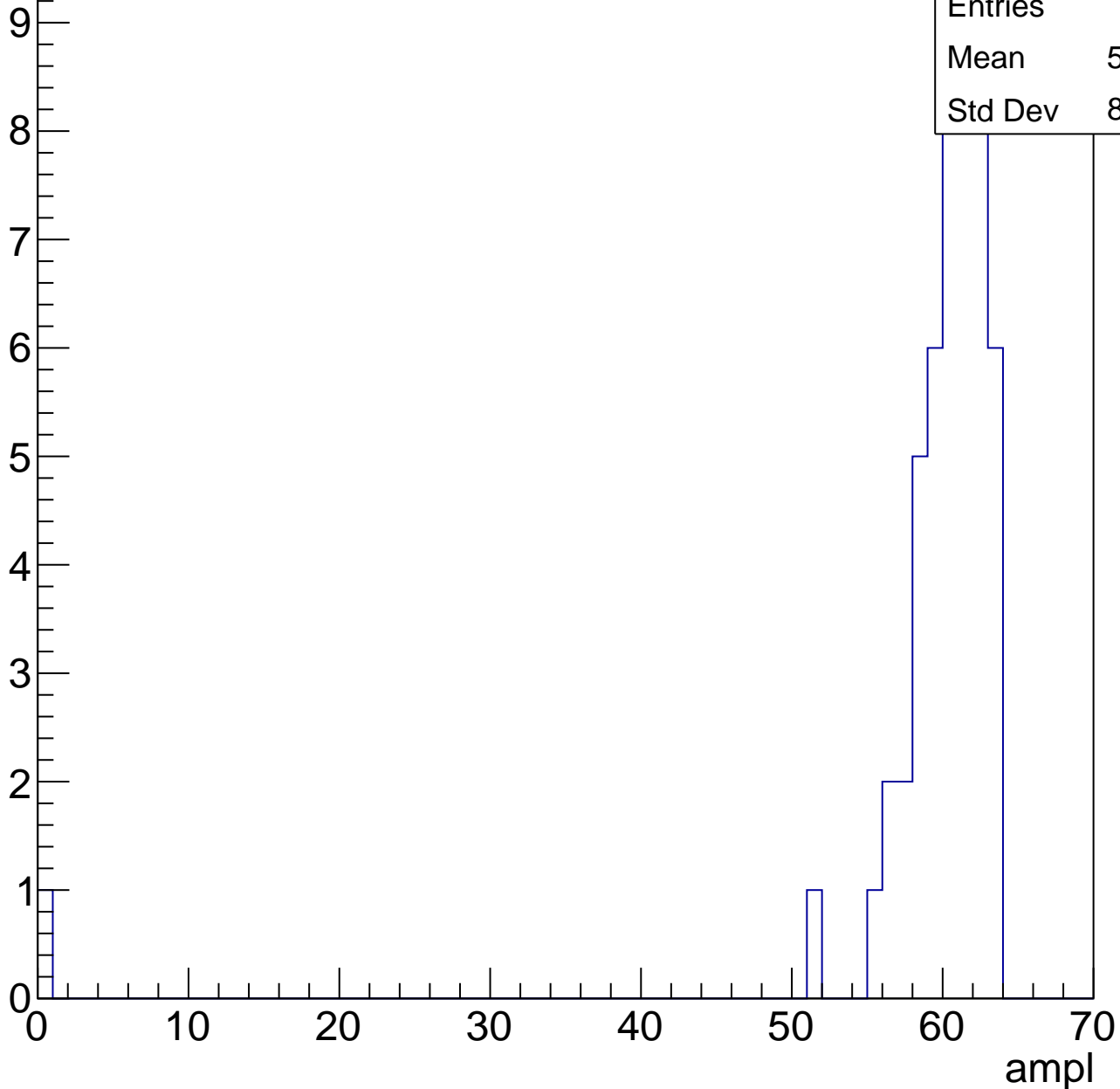


B1L103S, U23-ch65, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	49
Mean	58.78
Std Dev	8.814



B1L103S, U23-ch65, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch65, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	18
Mean	0.9444
Std Dev	3.894

Entry

16
14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70

B1L103S, U23-ch66, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	79
Mean	22.72
Std Dev	10.69

Entry

12

10

8

6

4

2

0

0

10

20

30

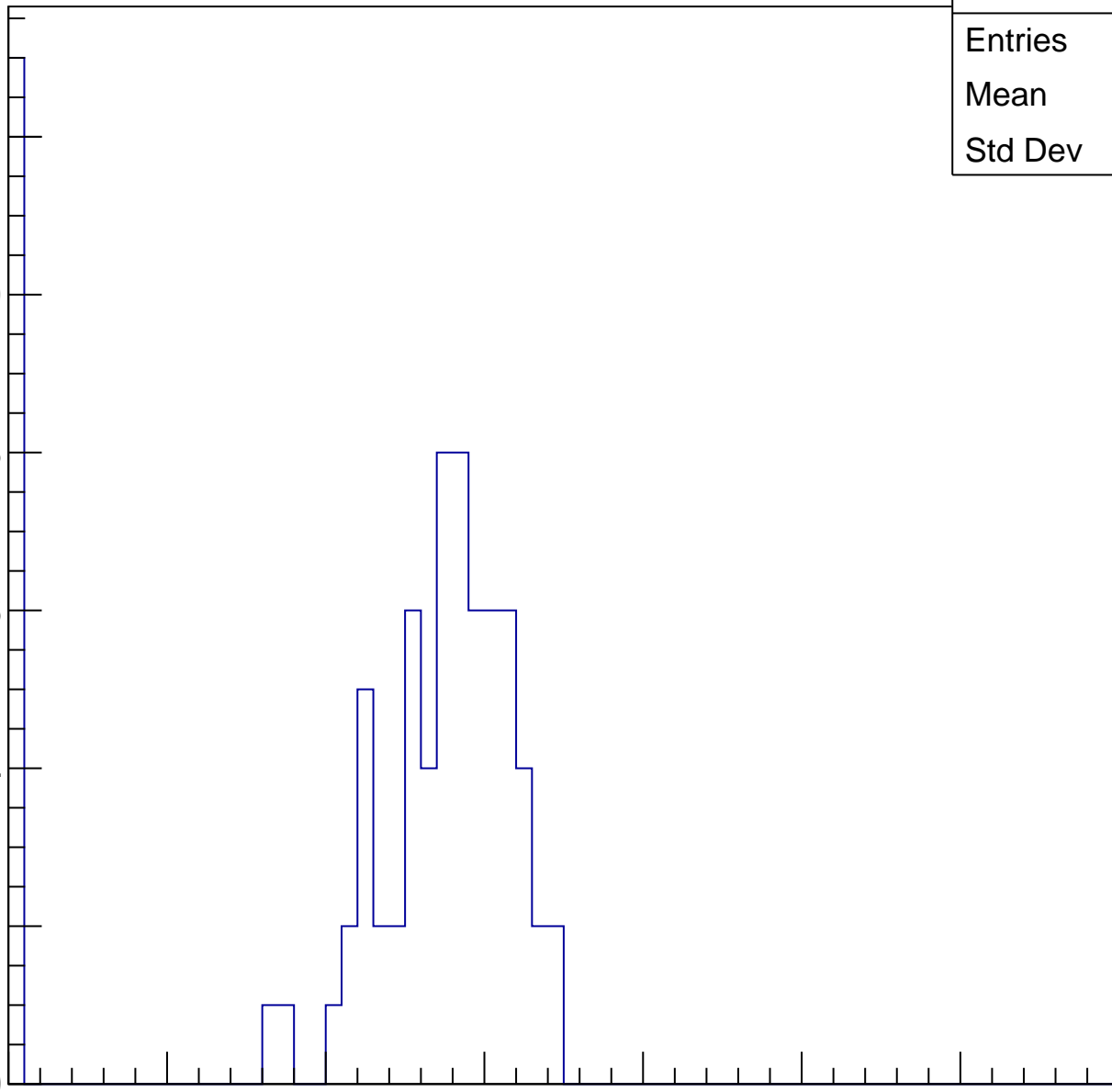
40

50

60

70

ampl

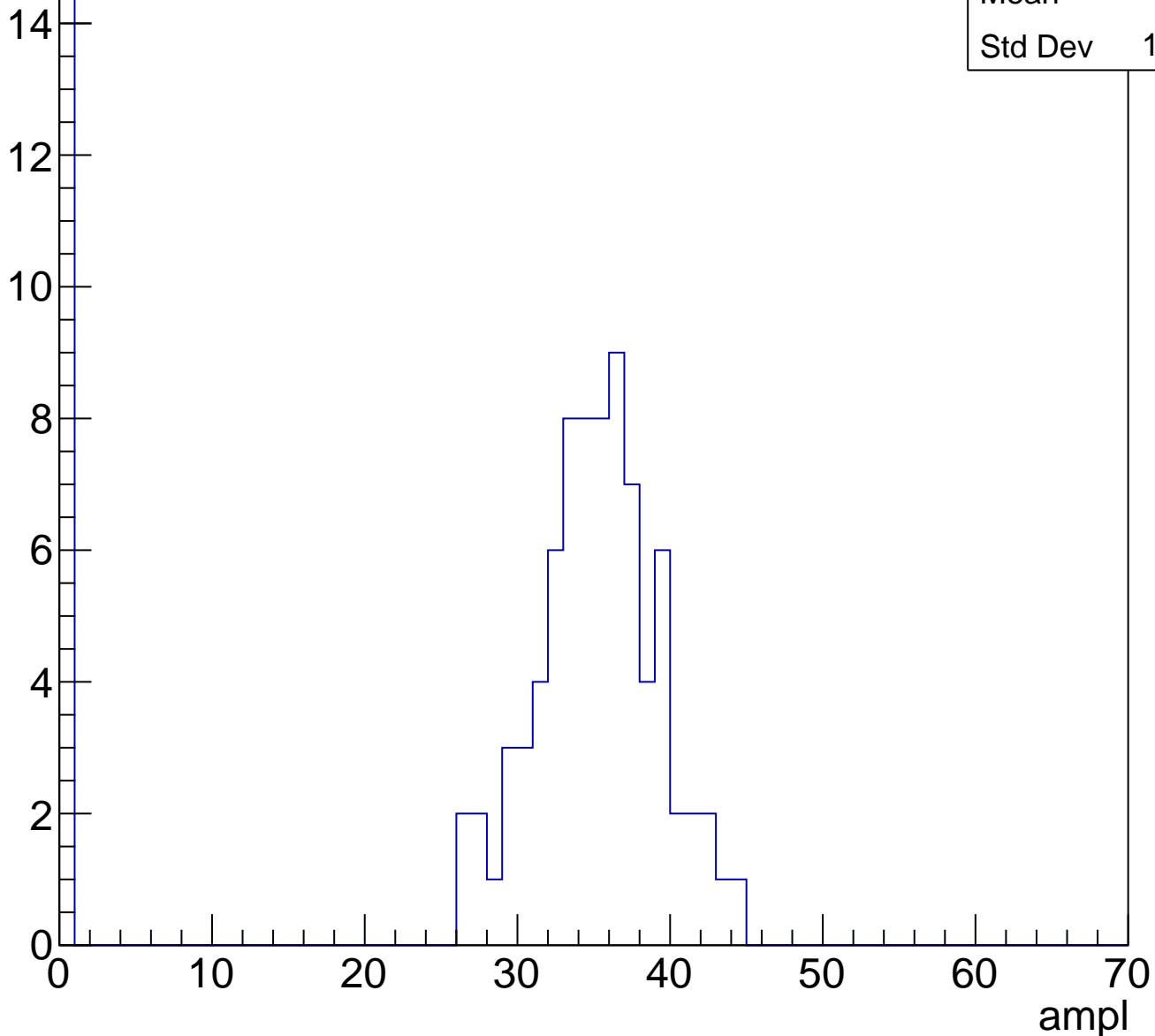


B1L103S, U23-ch66, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	94
Mean	29.2
Std Dev	13.22

Entry

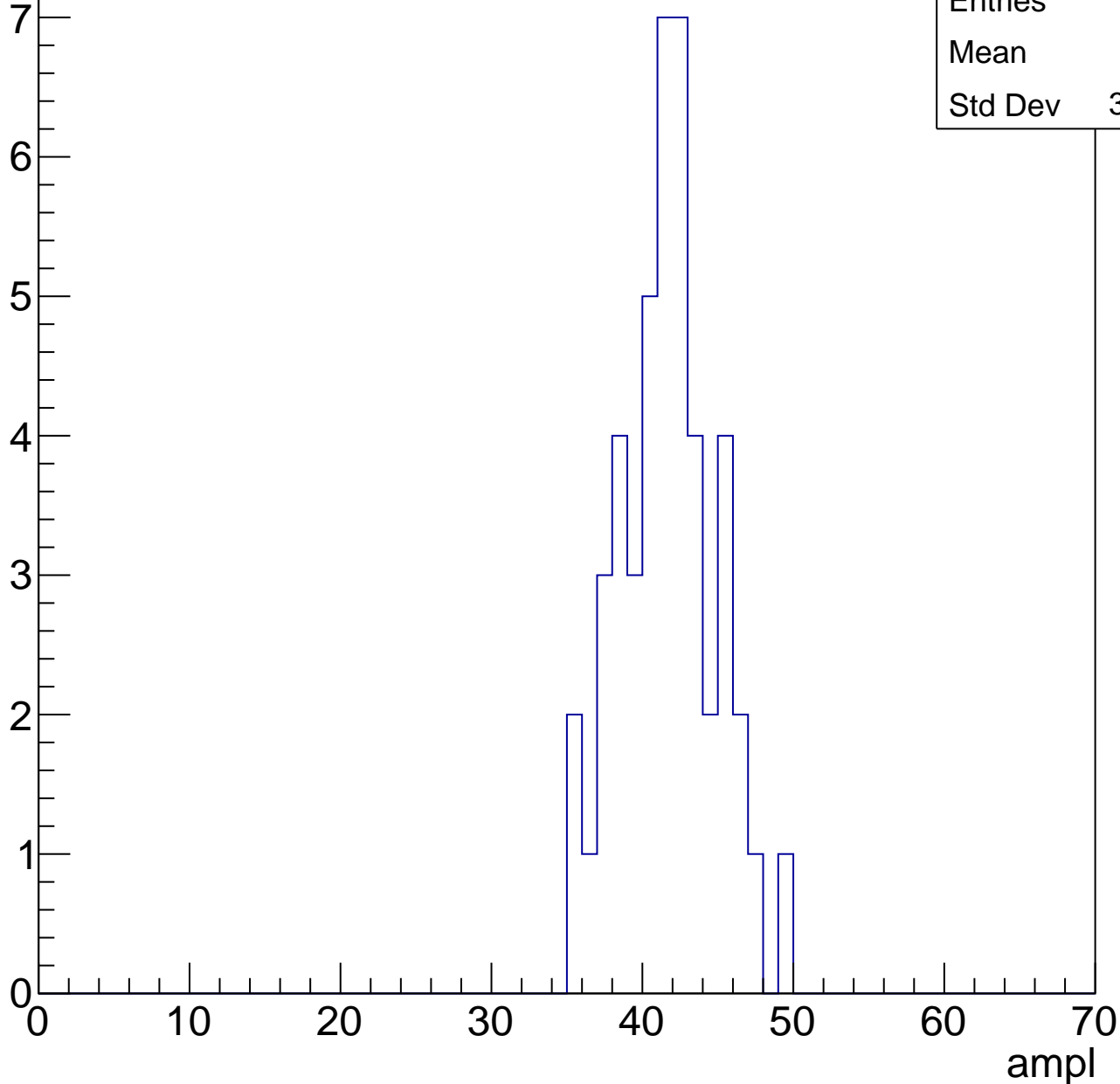


B1L103S, U23-ch66, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	46
Mean	41.2
Std Dev	3.132



B1L103S, U23-ch66, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	72
Mean	46.62
Std Dev	3.747

Entry

10

8

6

4

2

0

0

10

20

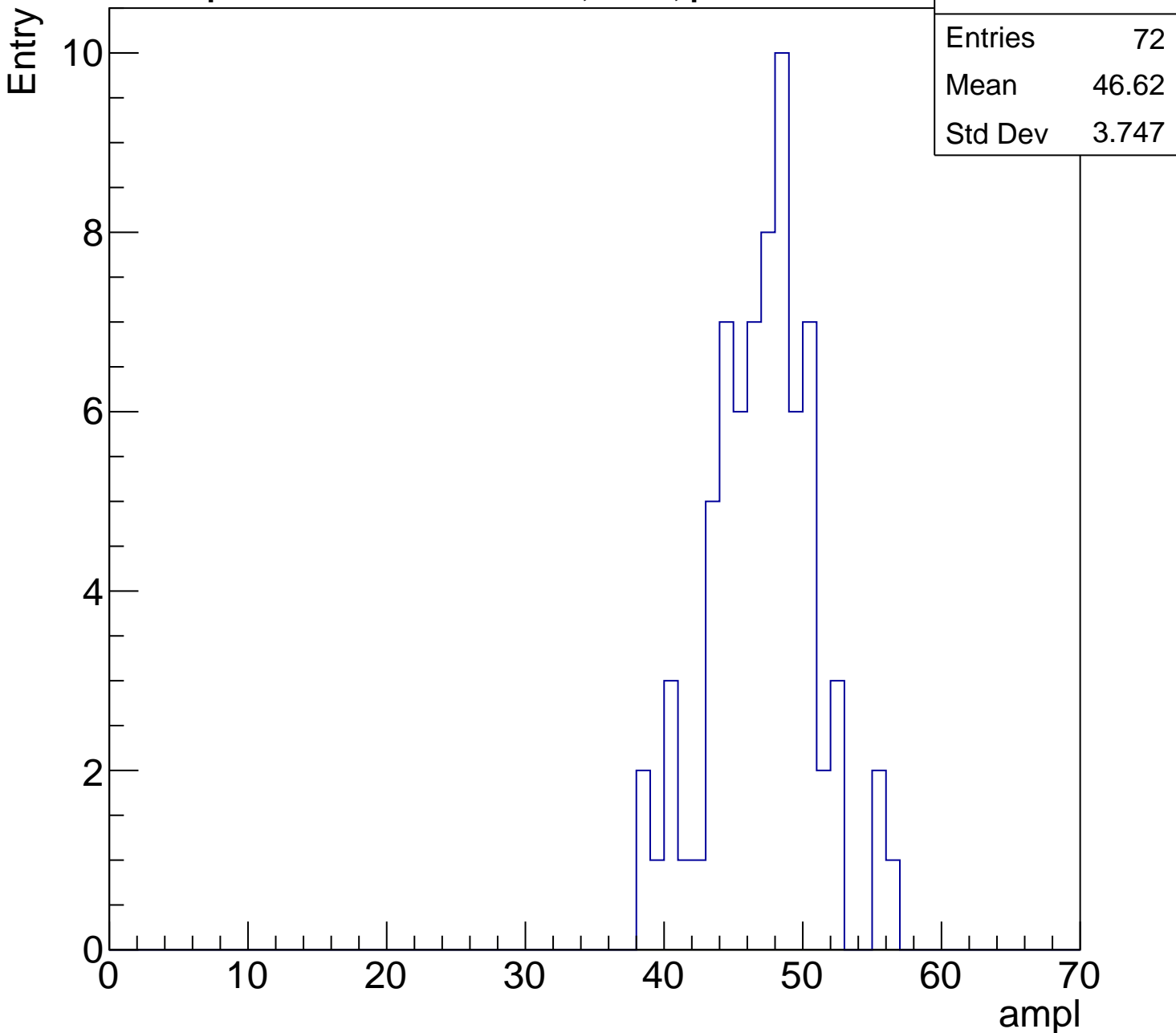
30

40

50

60

ampl

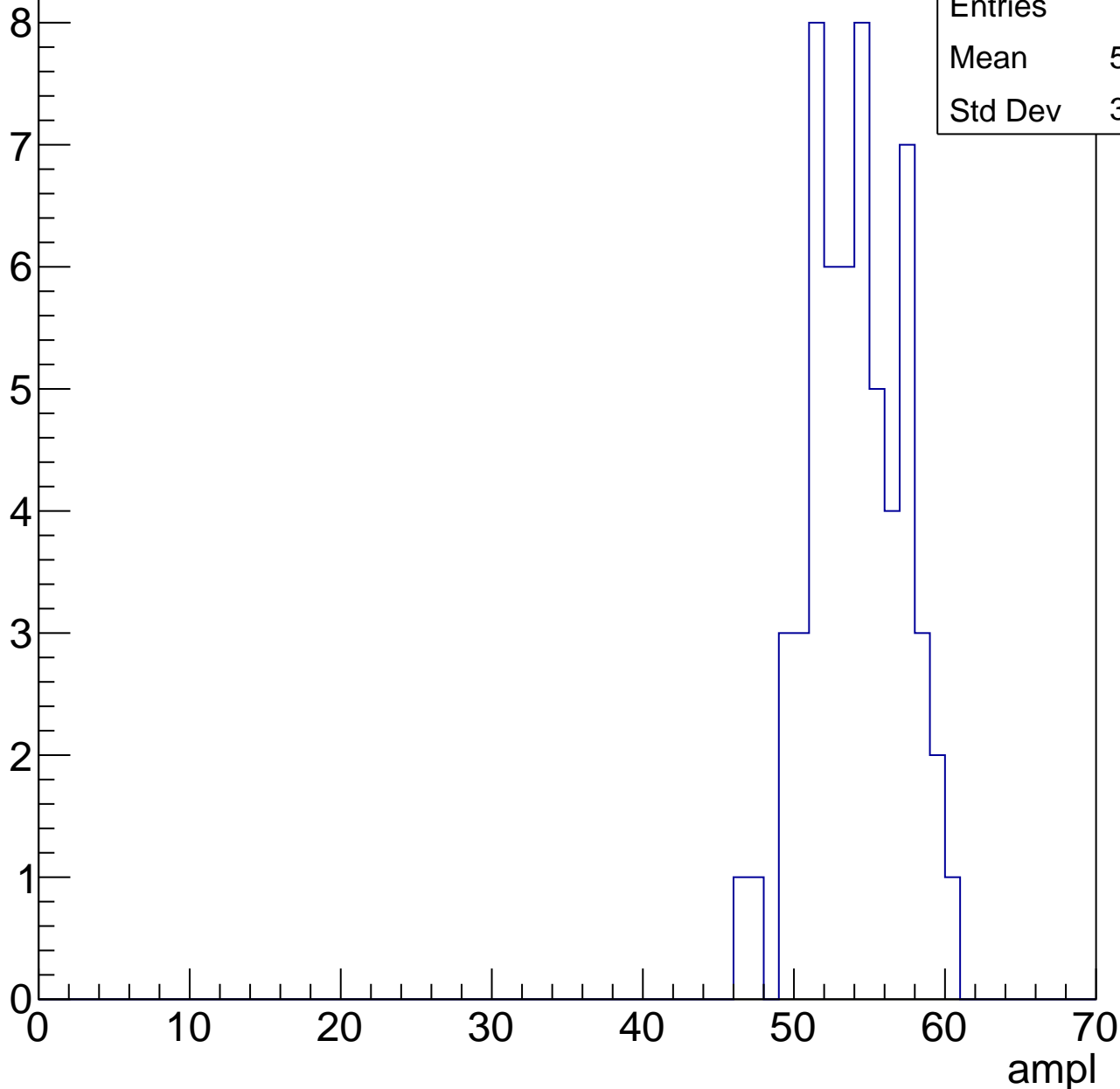


B1L103S, U23-ch66, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	53.62
Std Dev	3.073



B1L103S, U23-ch66, adc5

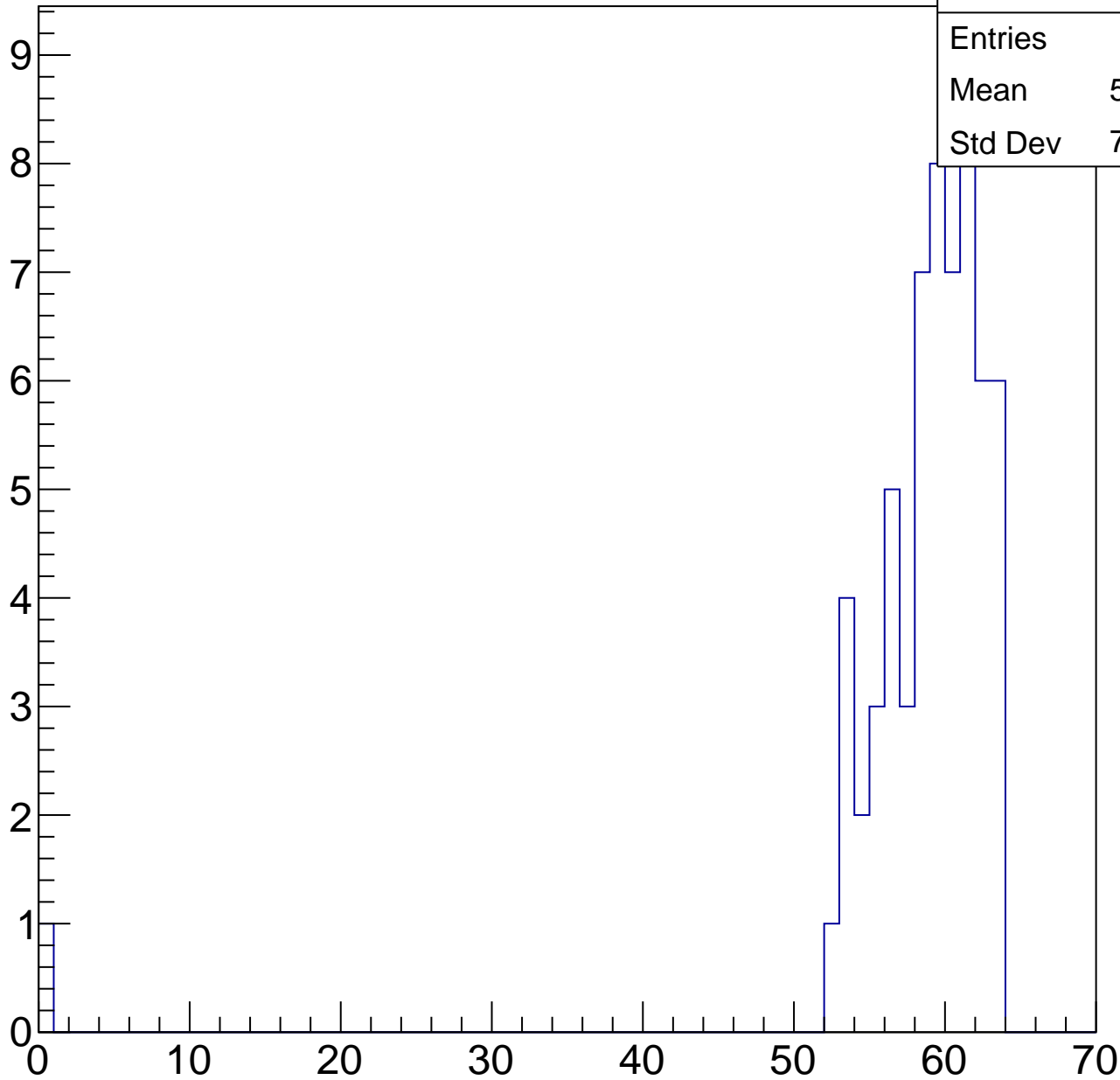
calib_packv5_041523_1651.root, FC#0, port C2

Entry

9
8
7
6
5
4
3
2
1
0

Entries	62
Mean	57.82
Std Dev	7.975

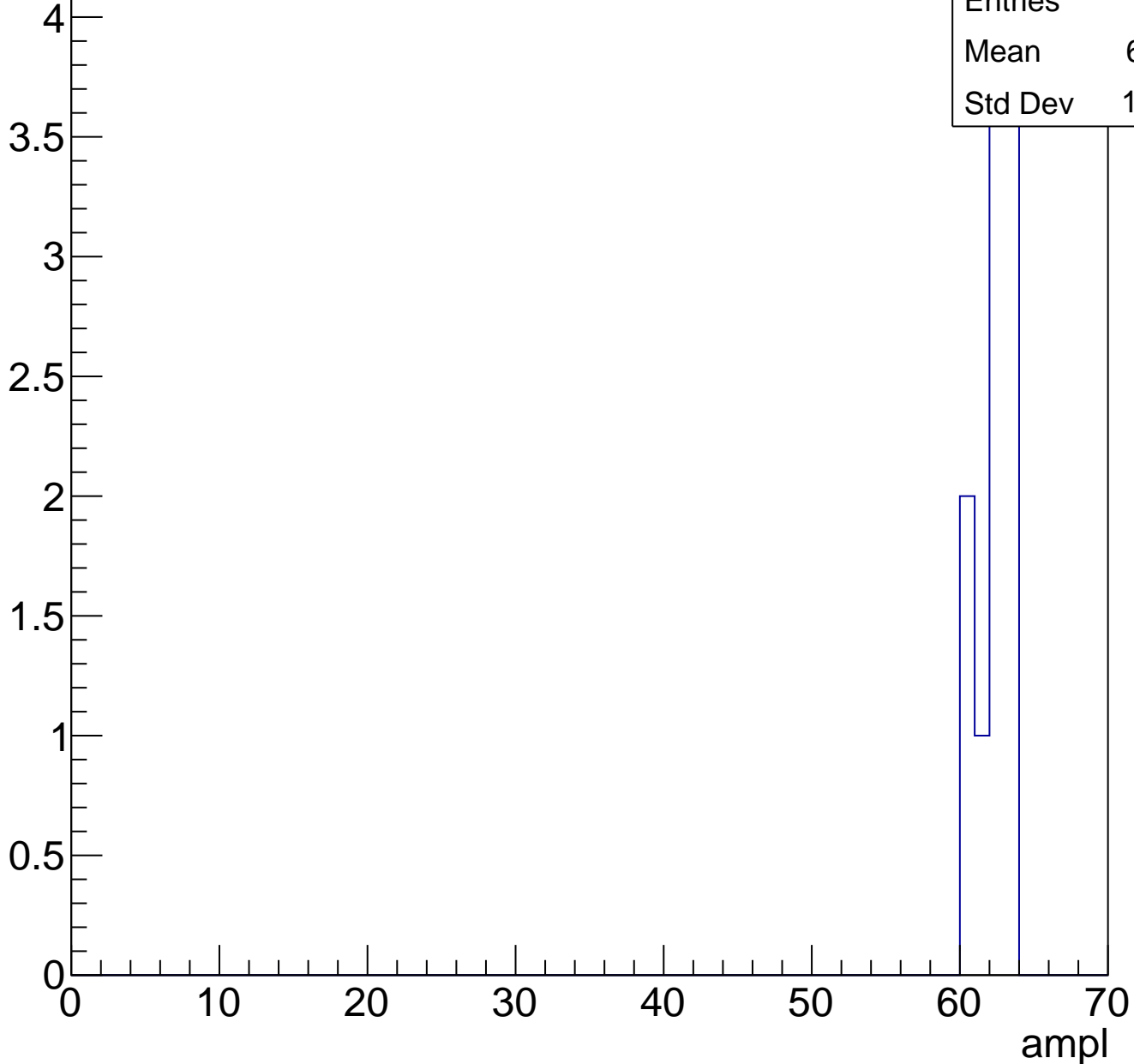
ampl



B1L103S, U23-ch66, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch66, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

ampl

B1L103S, U23-ch67, adc0

calib_packv5_041523_1651.root, FC#0, port C2

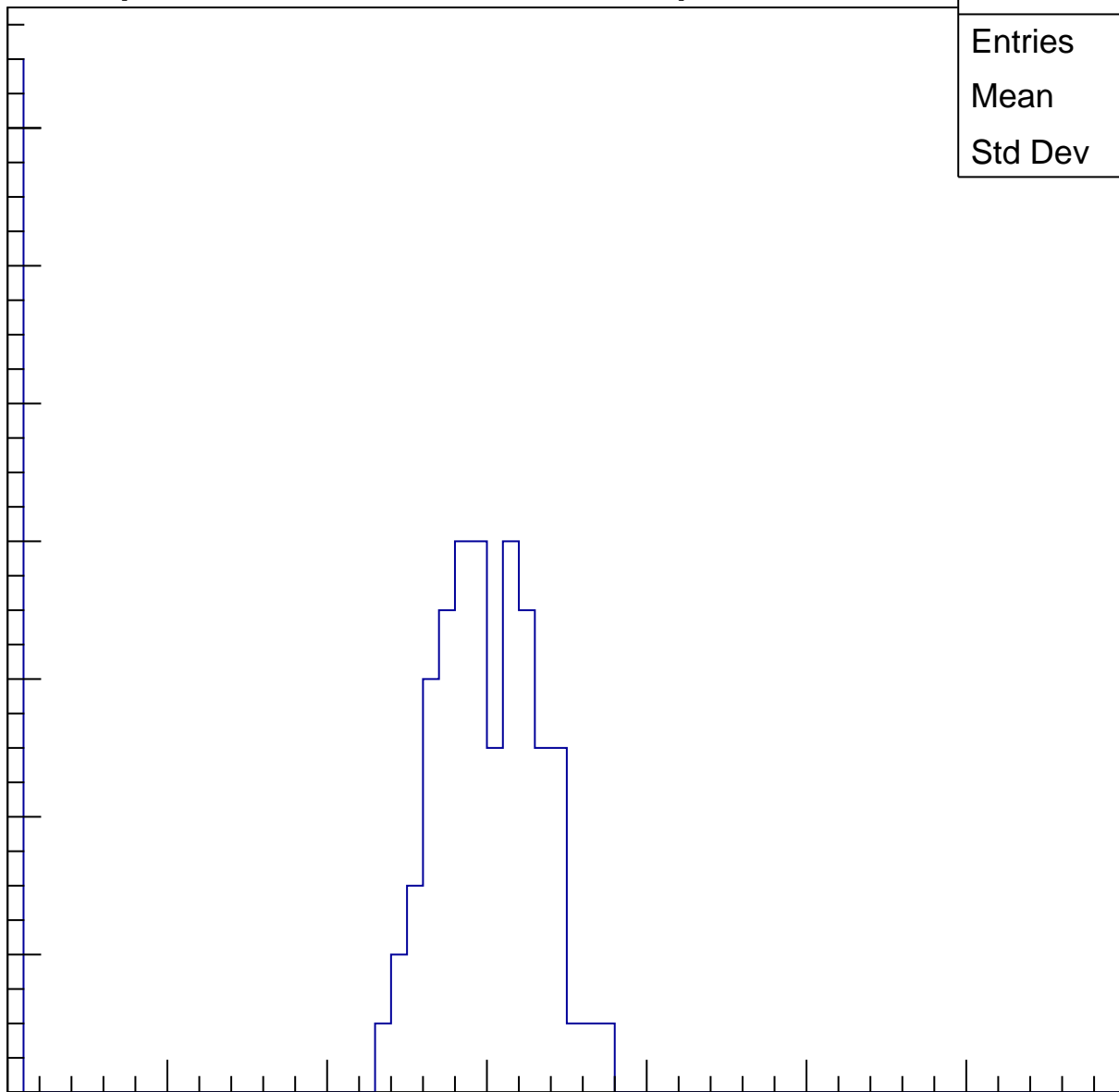
Entries	83
Mean	24.24
Std Dev	11.73

Entry

14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

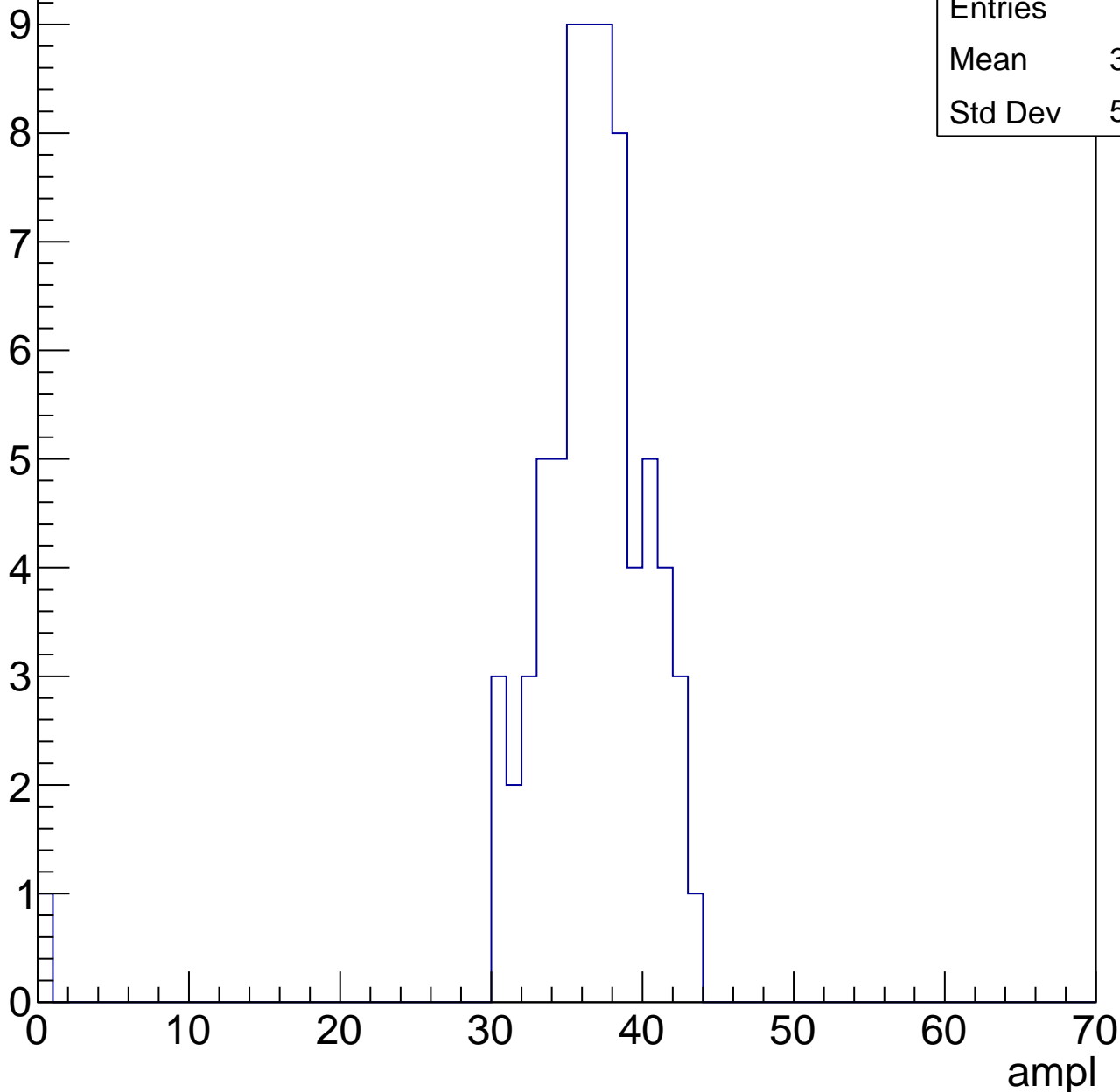


B1L103S, U23-ch67, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	35.89
Std Dev	5.293



B1L103S, U23-ch67, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	74
Mean	35.62
Std Dev	16.66

Entry

12

10

8

6

4

2

0

0

10

20

30

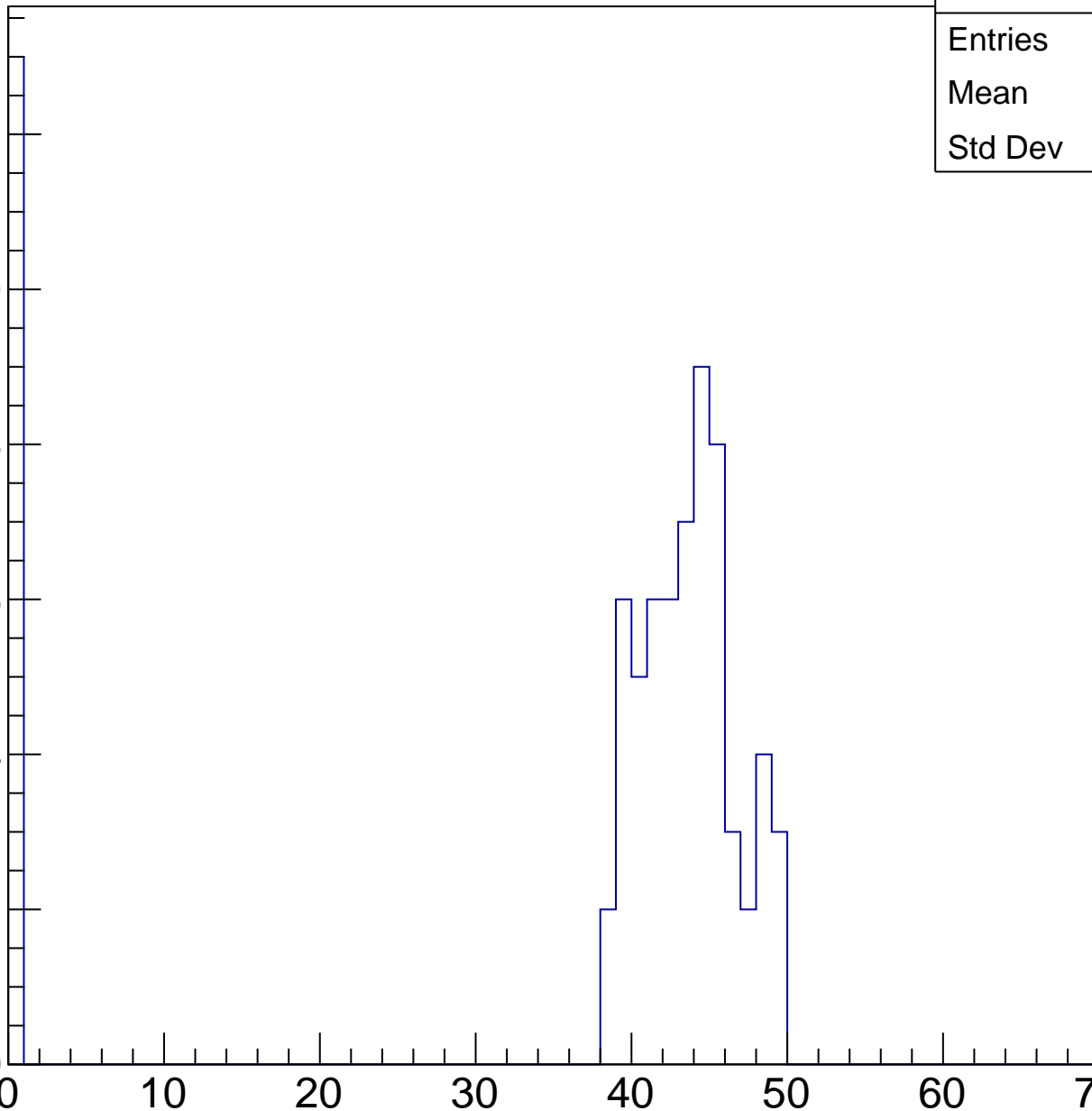
40

50

60

70

ampl

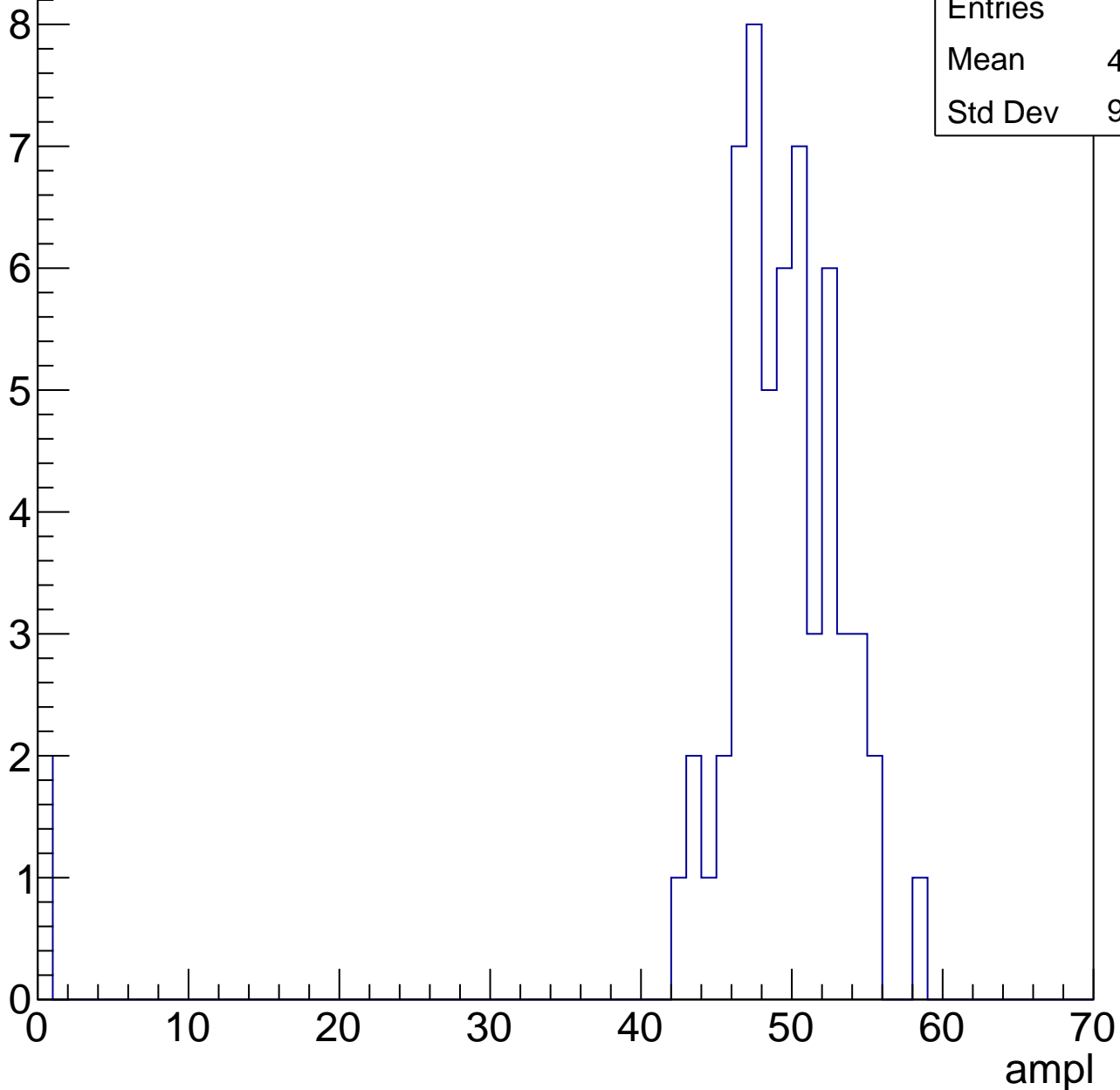


B1L103S, U23-ch67, adc3

calib_packv5_041523_1651.root, FC#0, port C2

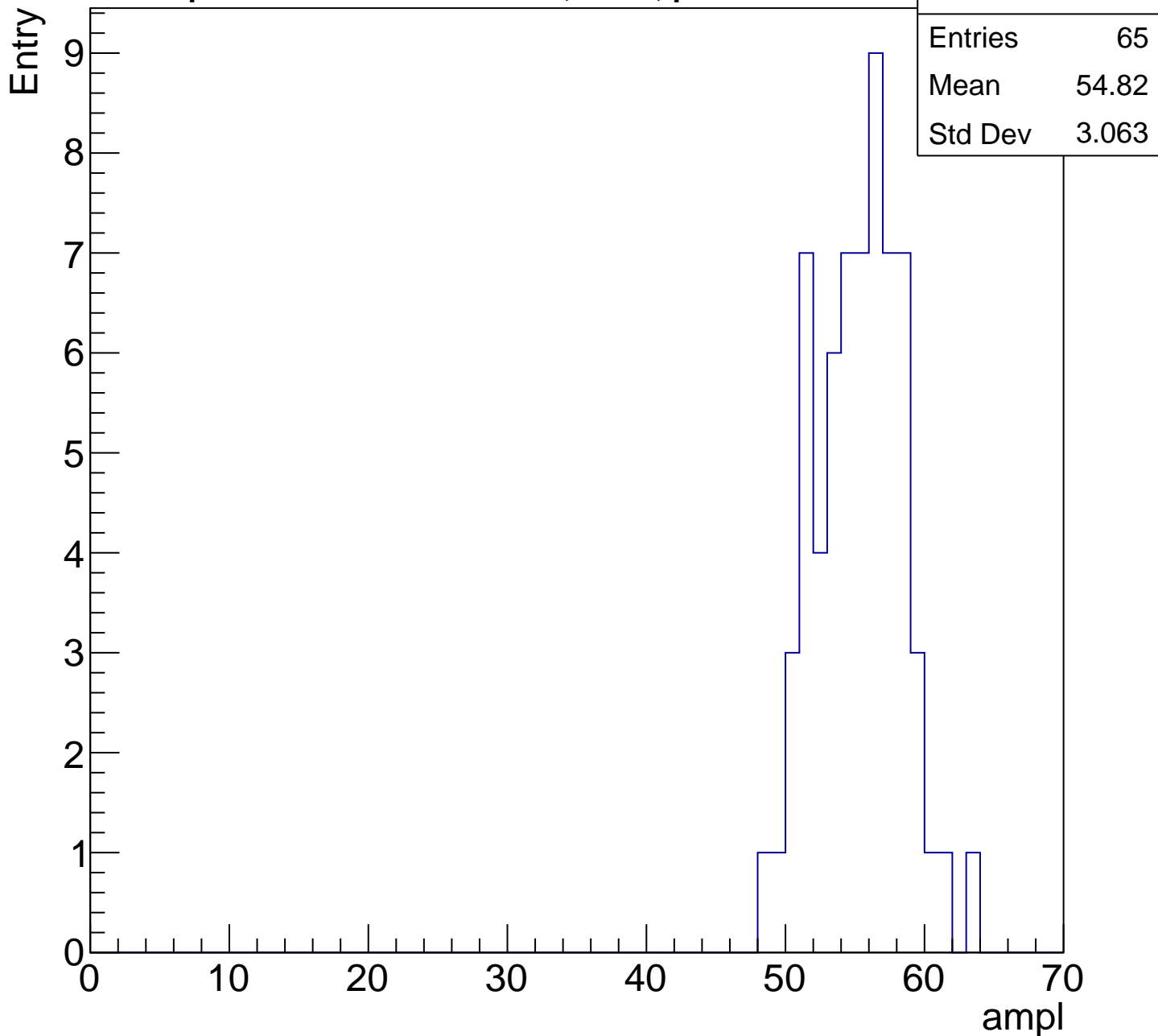
Entry

Entries	59
Mean	47.42
Std Dev	9.462



B1L103S, U23-ch67, adc4

calib_packv5_041523_1651.root, FC#0, port C2

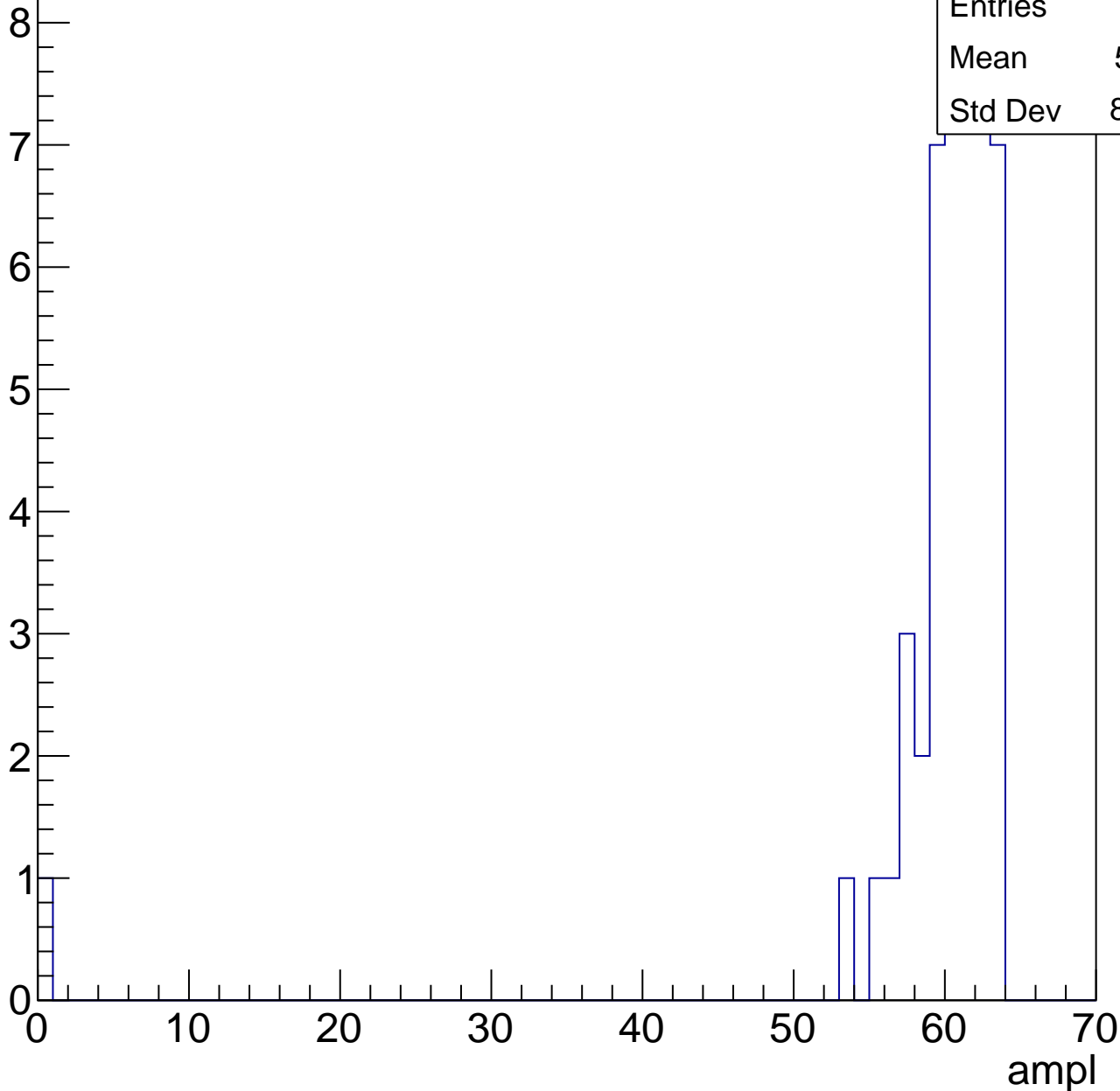


B1L103S, U23-ch67, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

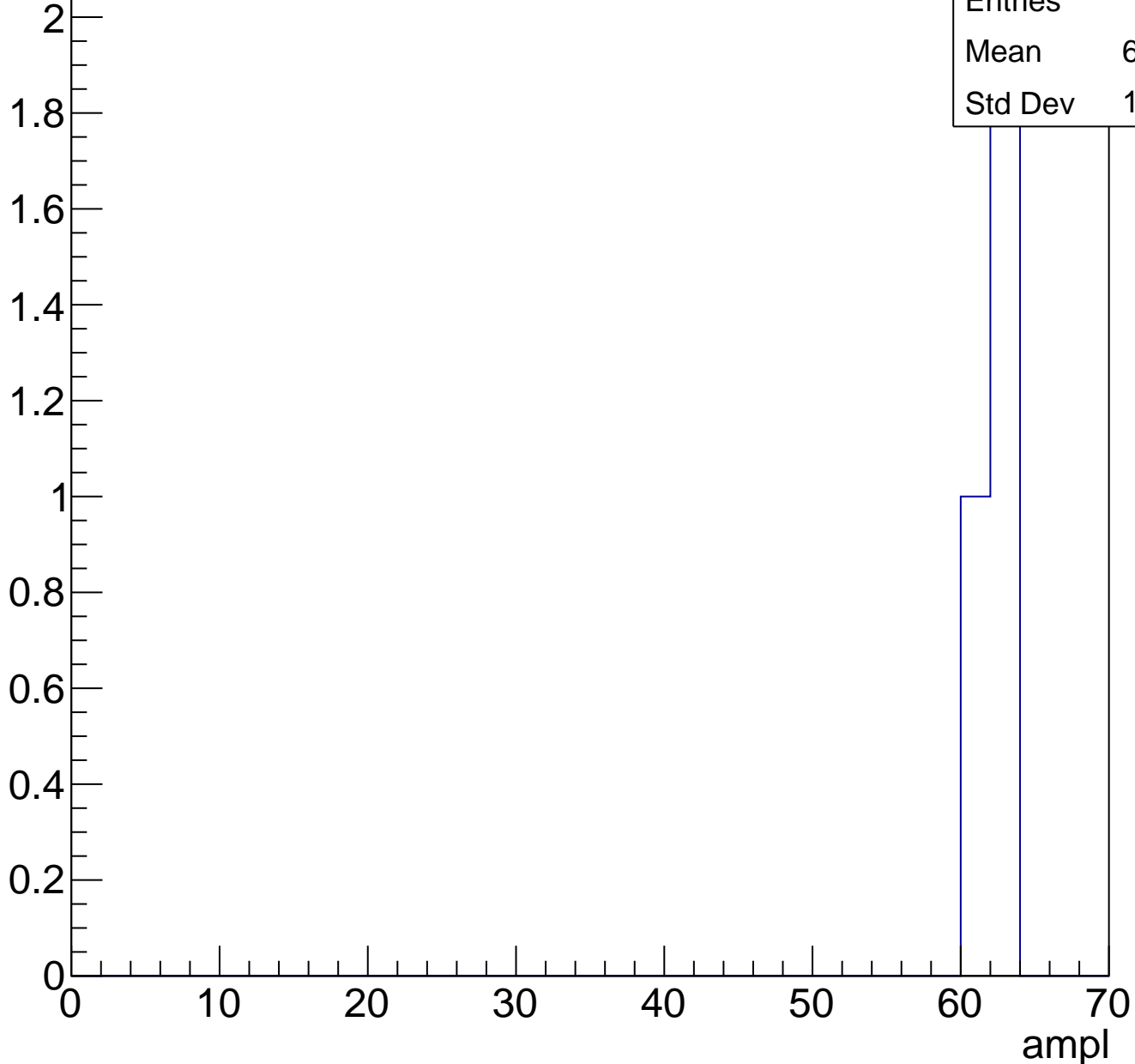
Entries	47
Mean	58.91
Std Dev	8.968



B1L103S, U23-ch67, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch67, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

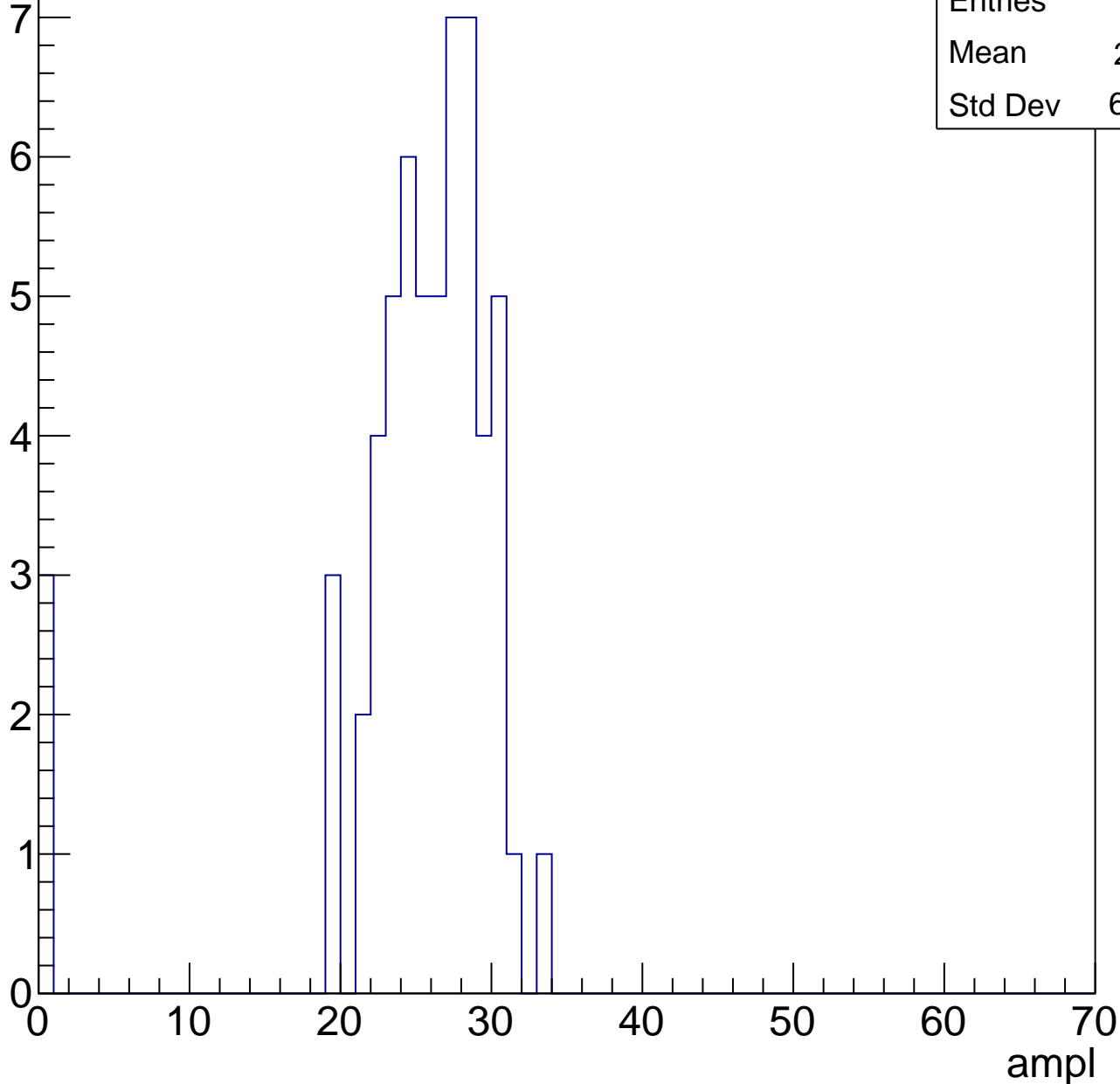


B1L103S, U23-ch68, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

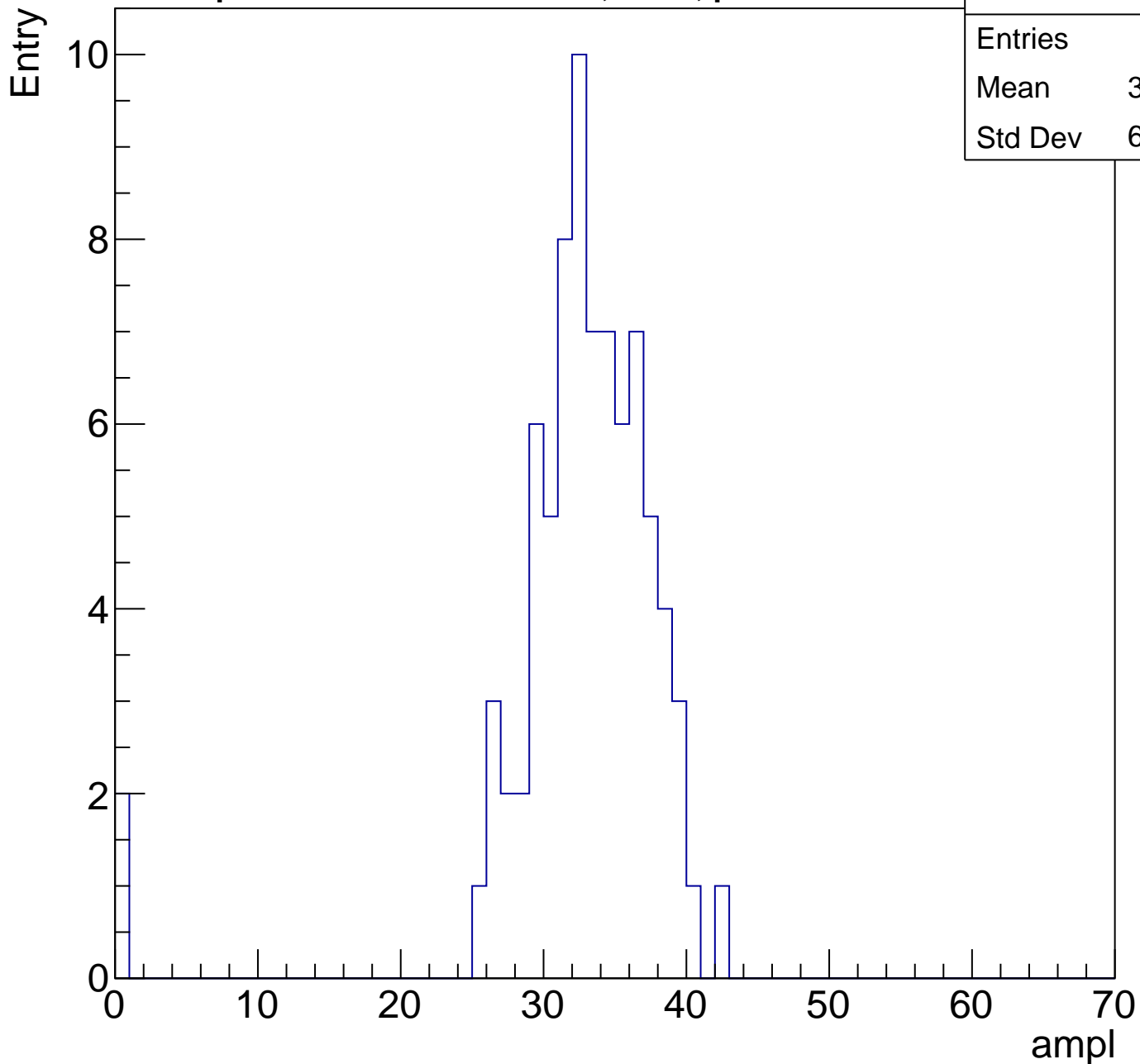
Entries	58
Mean	24.41
Std Dev	6.489



B1L103S, U23-ch68, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	80
Mean	32.15
Std Dev	6.273

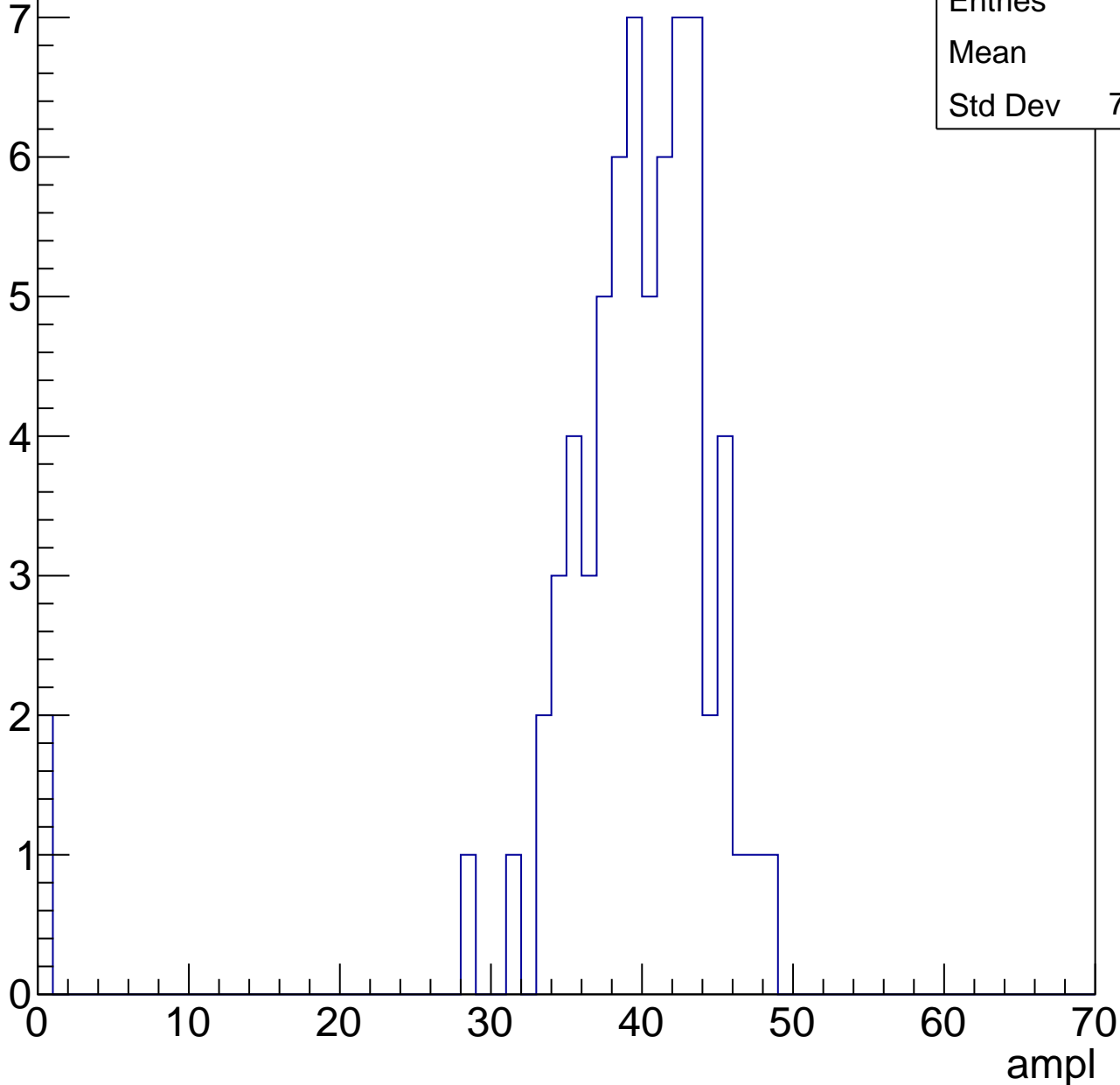


B1L103S, U23-ch68, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	38.4
Std Dev	7.725

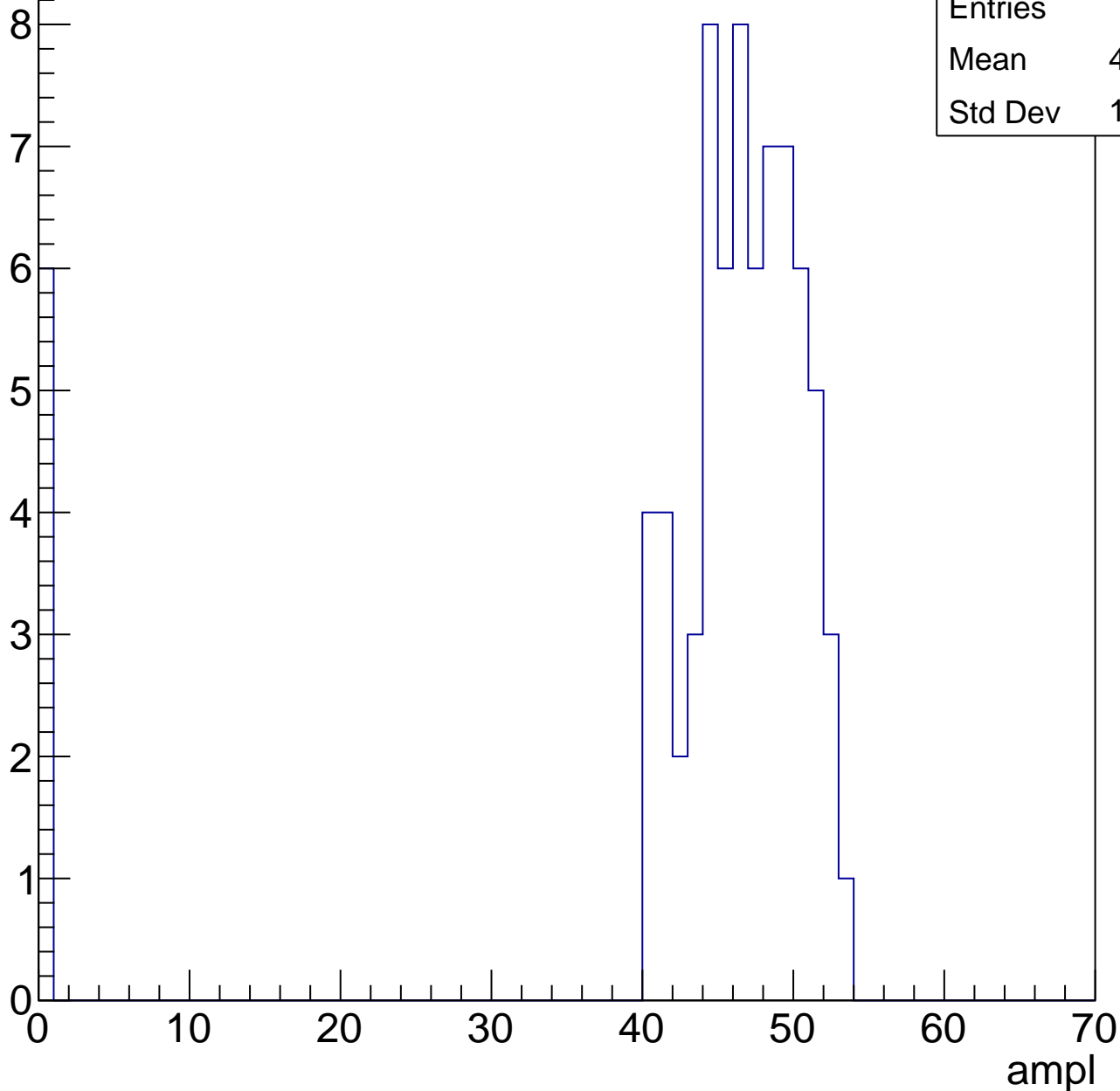


B1L103S, U23-ch68, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	76
Mean	42.79
Std Dev	12.94

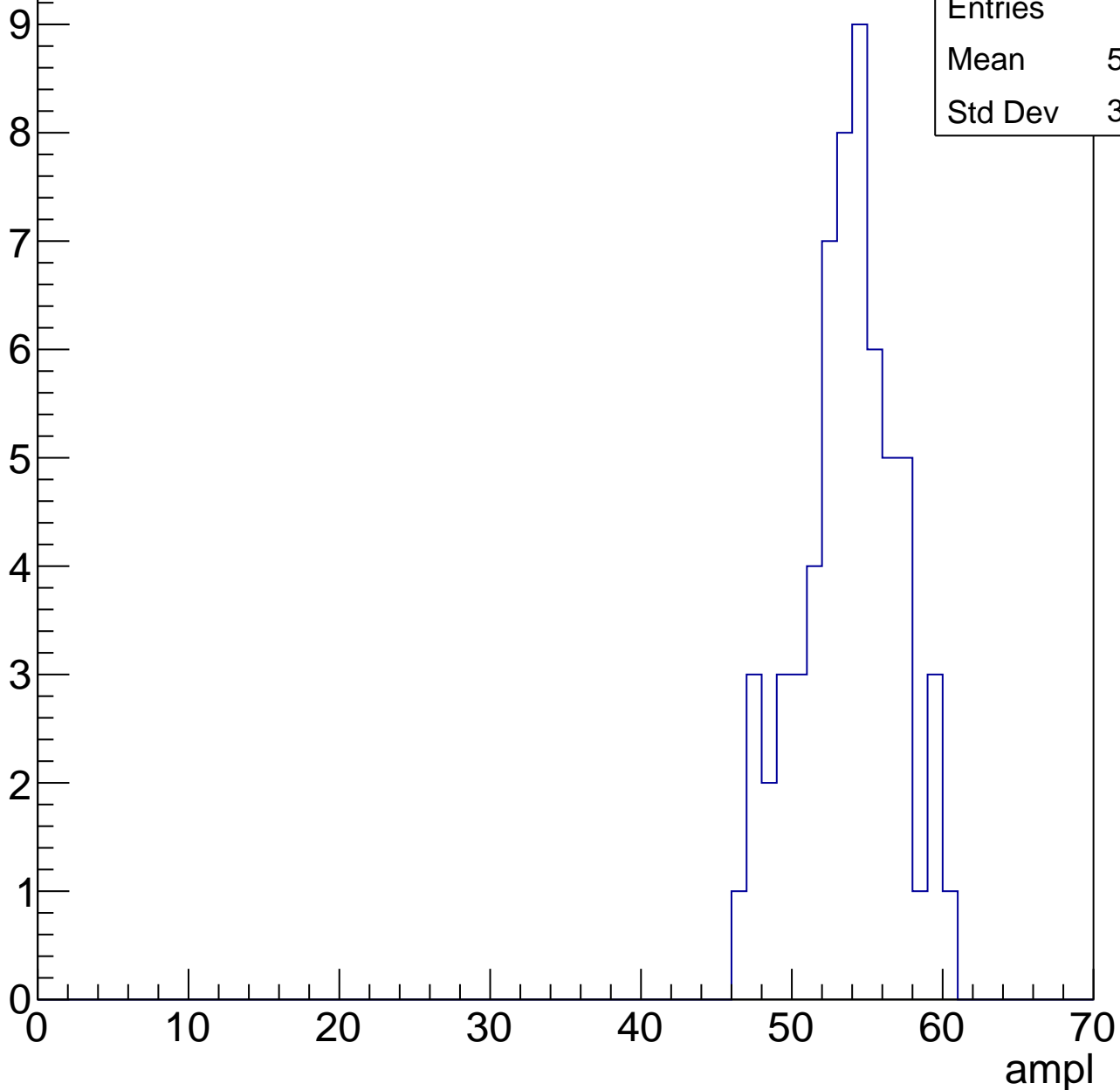


B1L103S, U23-ch68, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	53.25
Std Dev	3.242

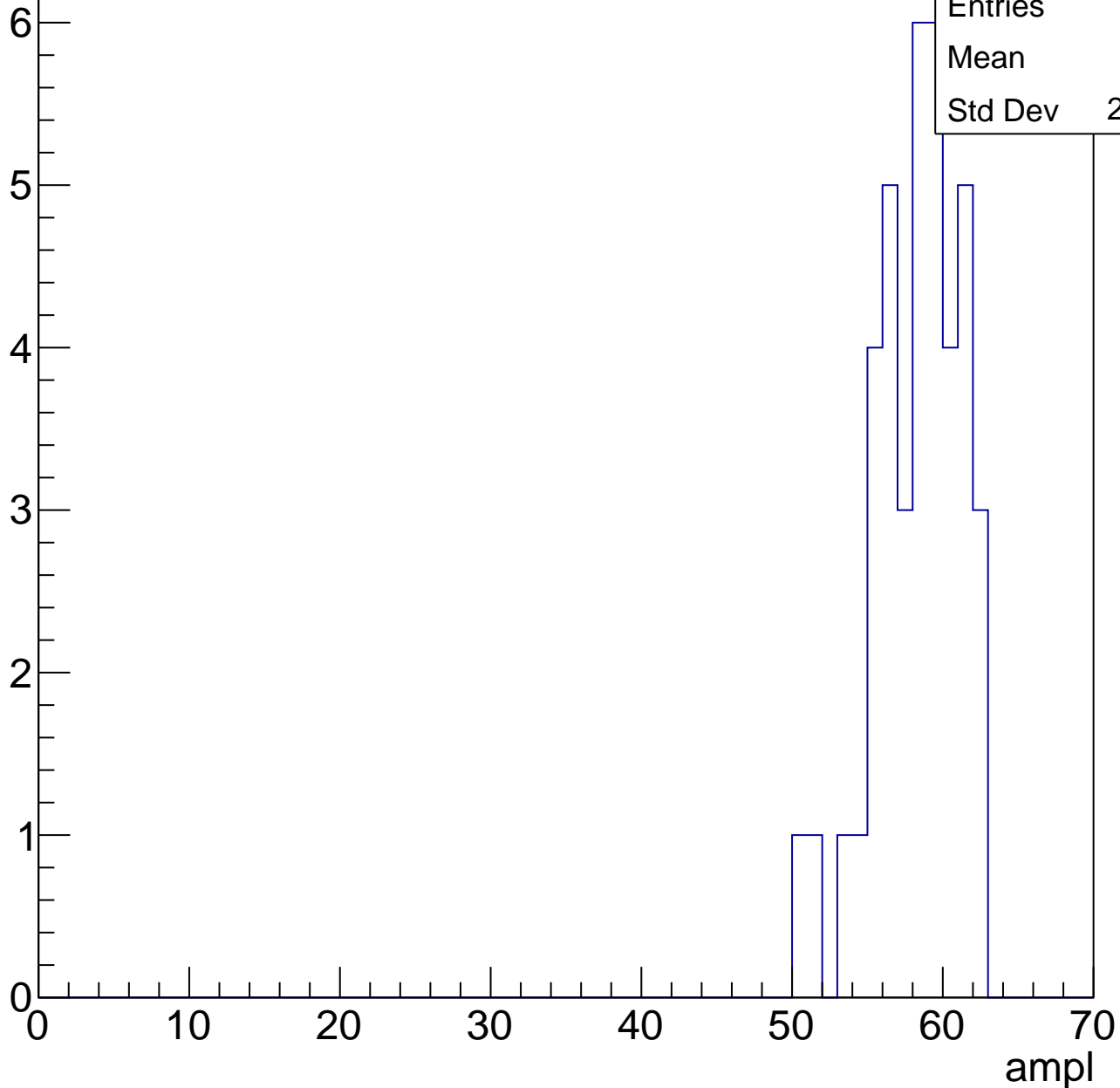


B1L103S, U23-ch68, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	40
Mean	57.8
Std Dev	2.857

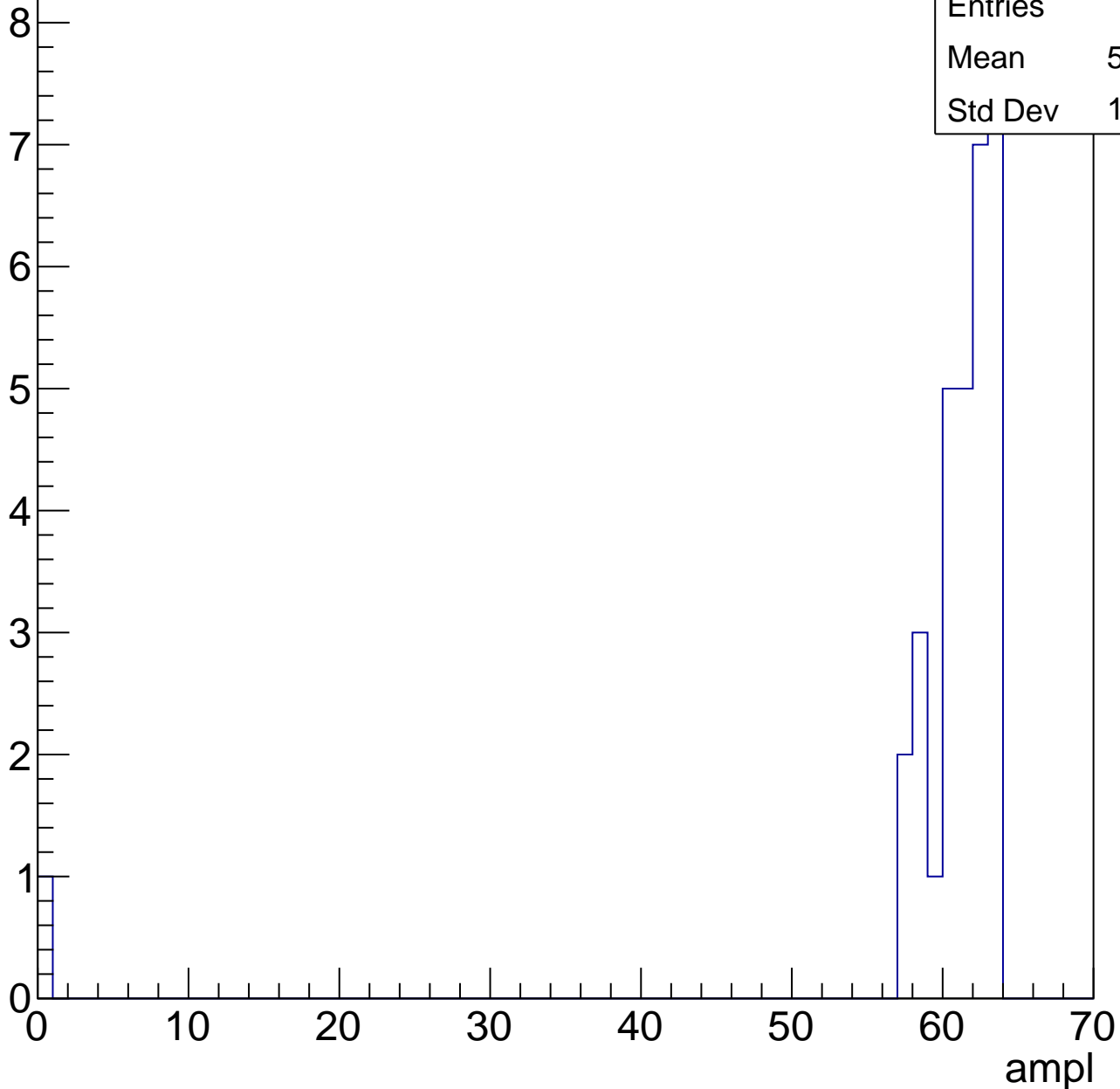


B1L103S, U23-ch68, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

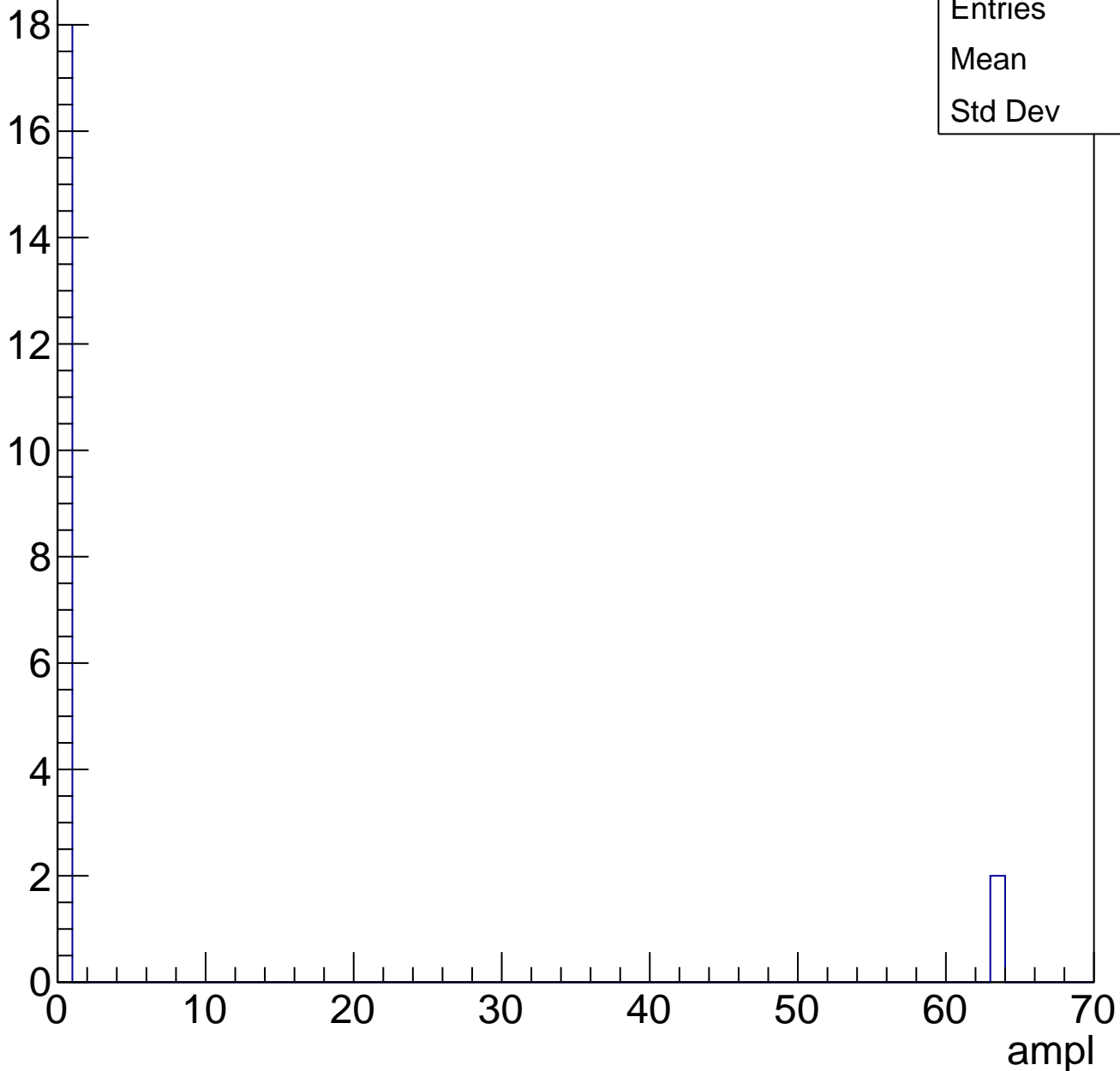
Entries	32
Mean	59.06
Std Dev	10.76



B1L103S, U23-ch68, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

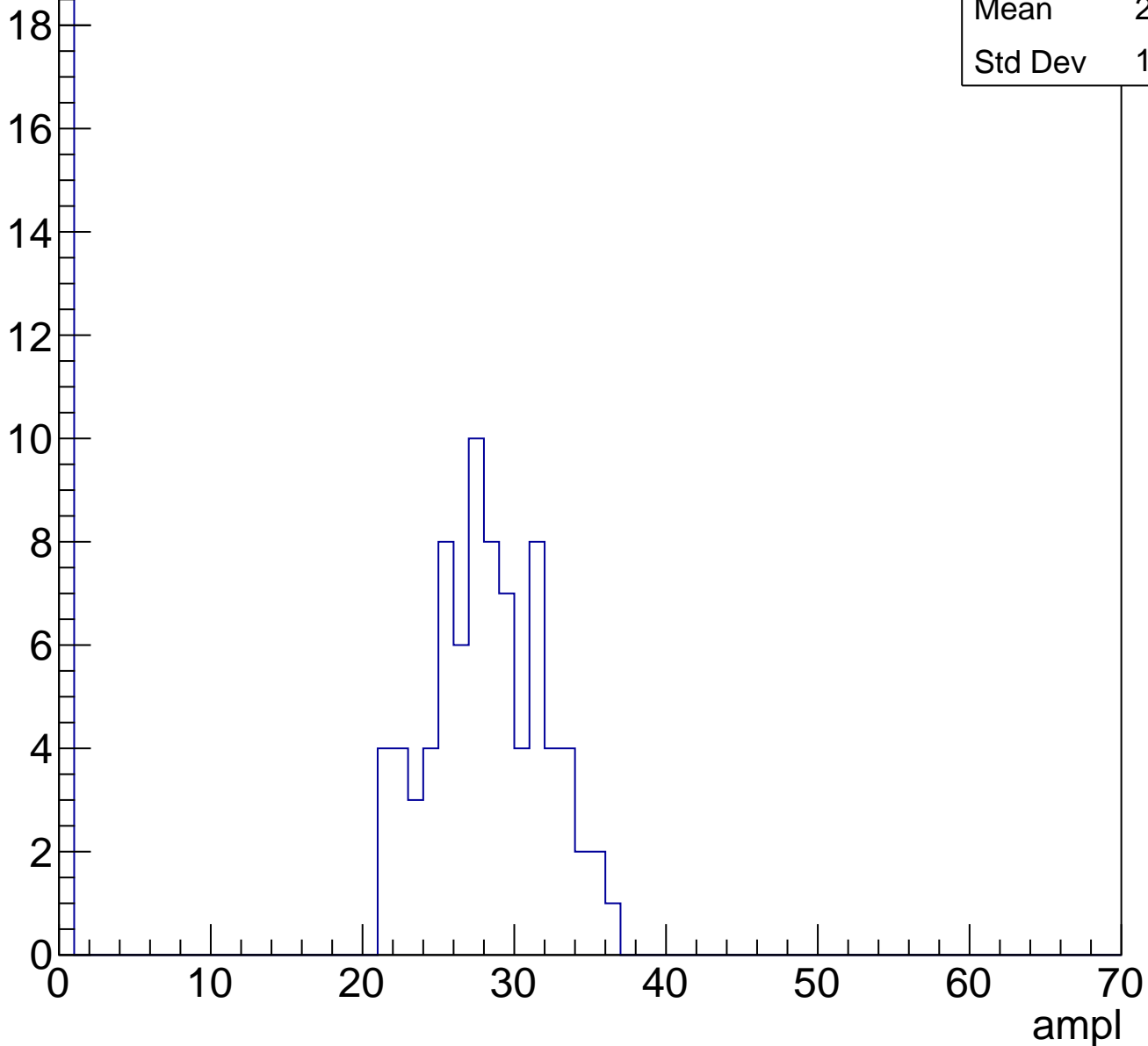


B1L103S, U23-ch69, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	98
Mean	22.37
Std Dev	11.46

Entry

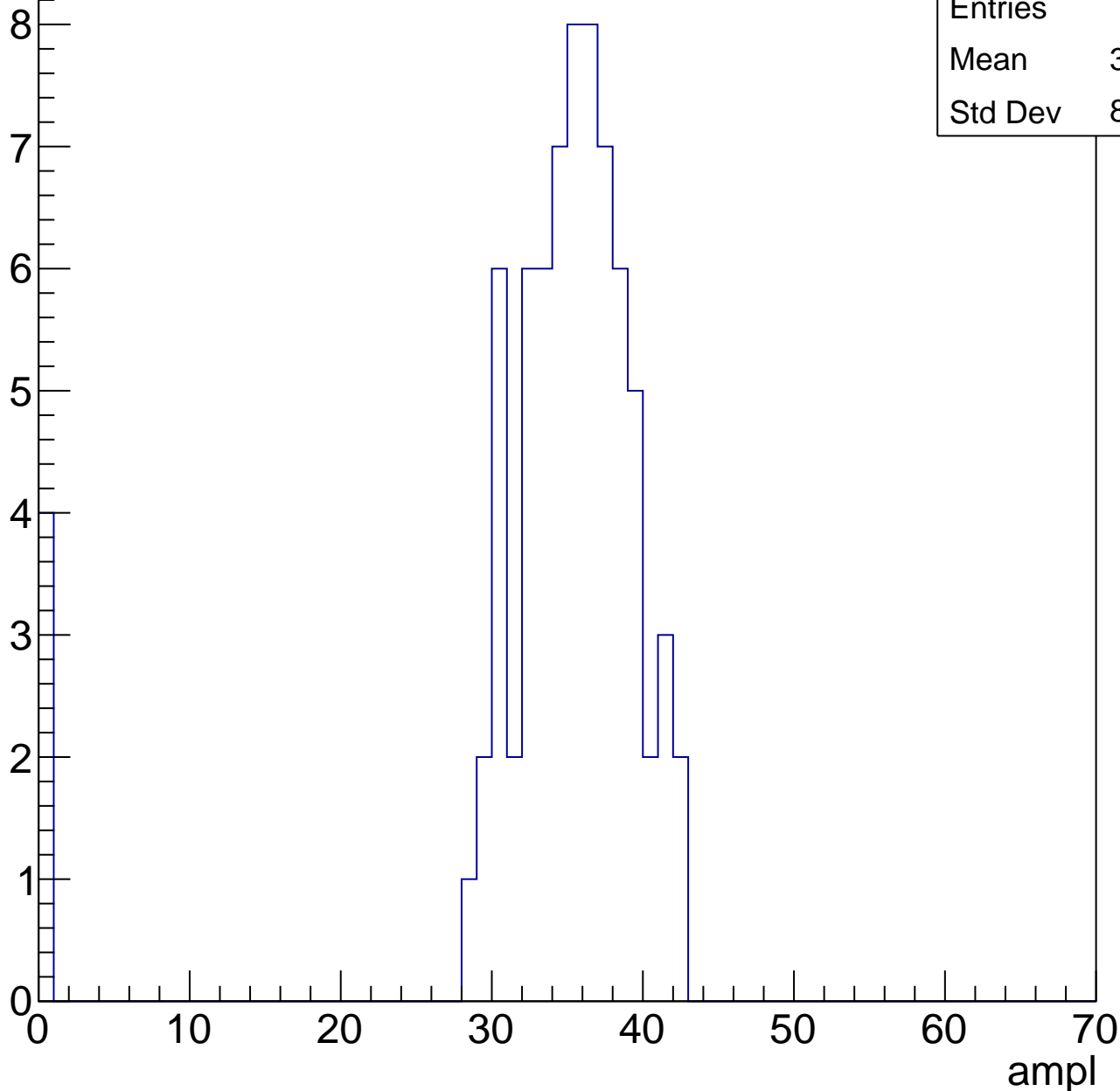


B1L103S, U23-ch69, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	75
Mean	33.24
Std Dev	8.549



B1L103S, U23-ch69, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	64
Mean	32.56
Std Dev	16.7

Entry

12

10

8

6

4

2

0

0

10

20

30

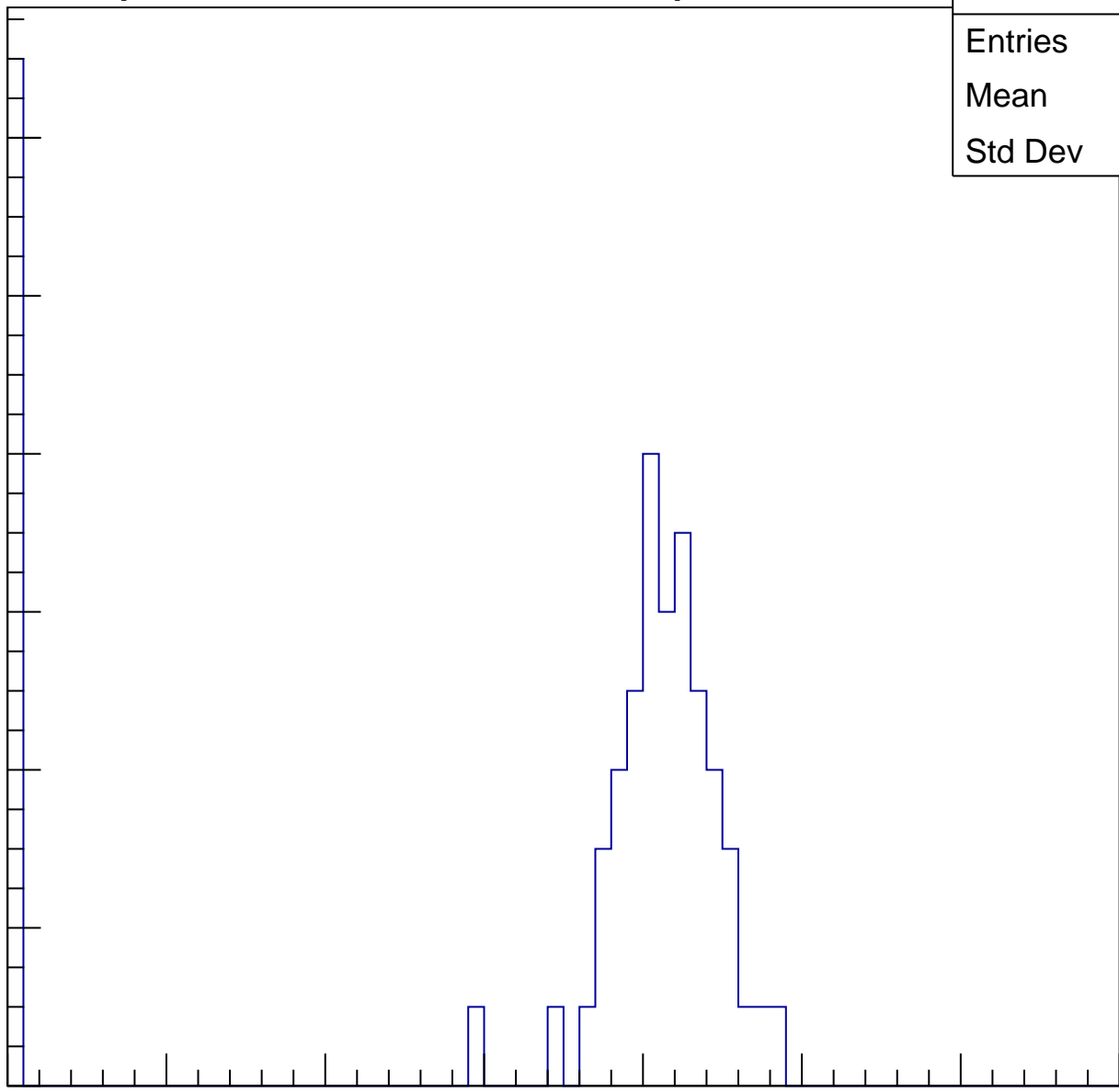
40

50

60

70

ampl

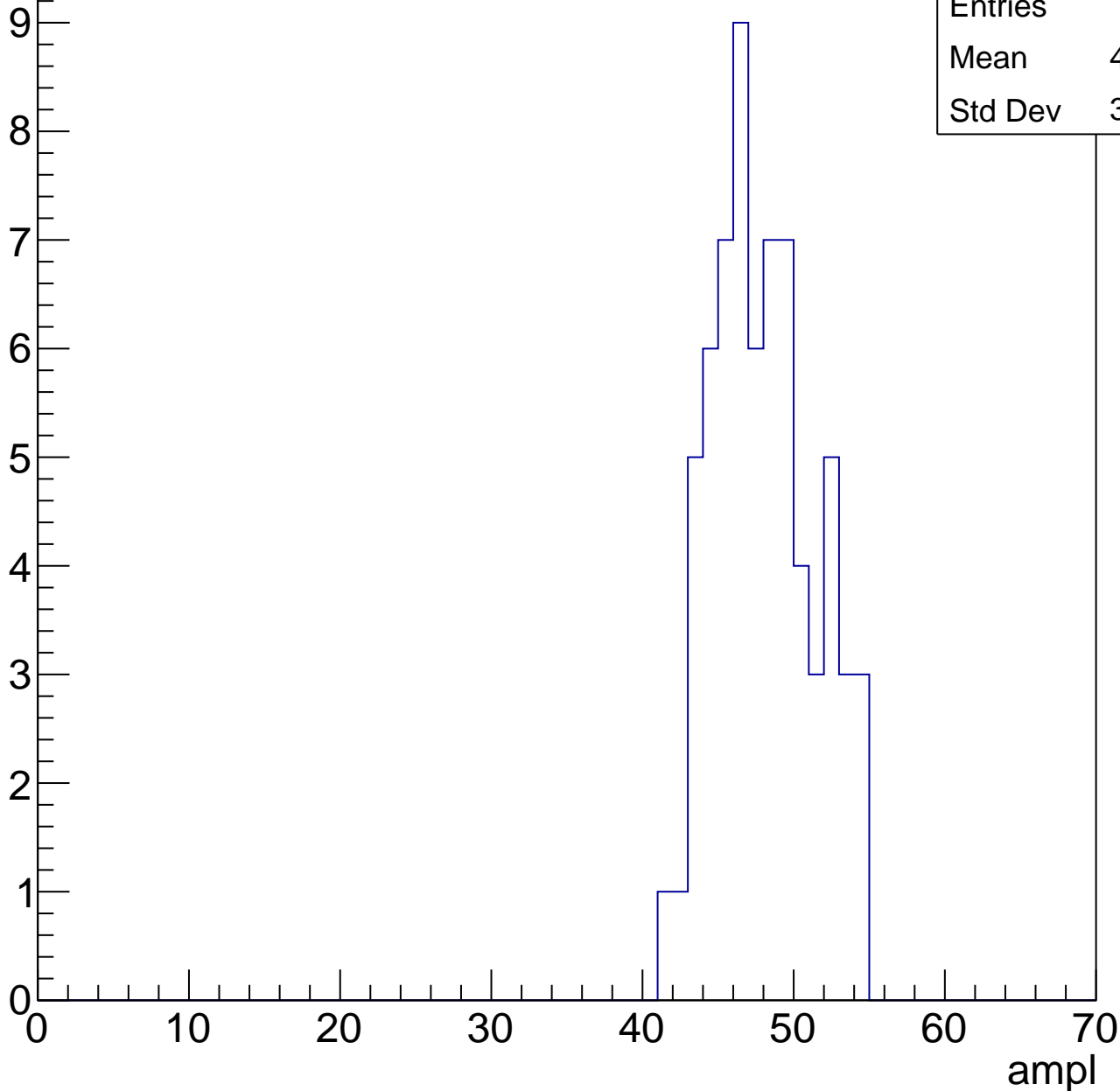


B1L103S, U23-ch69, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	47.55
Std Dev	3.257

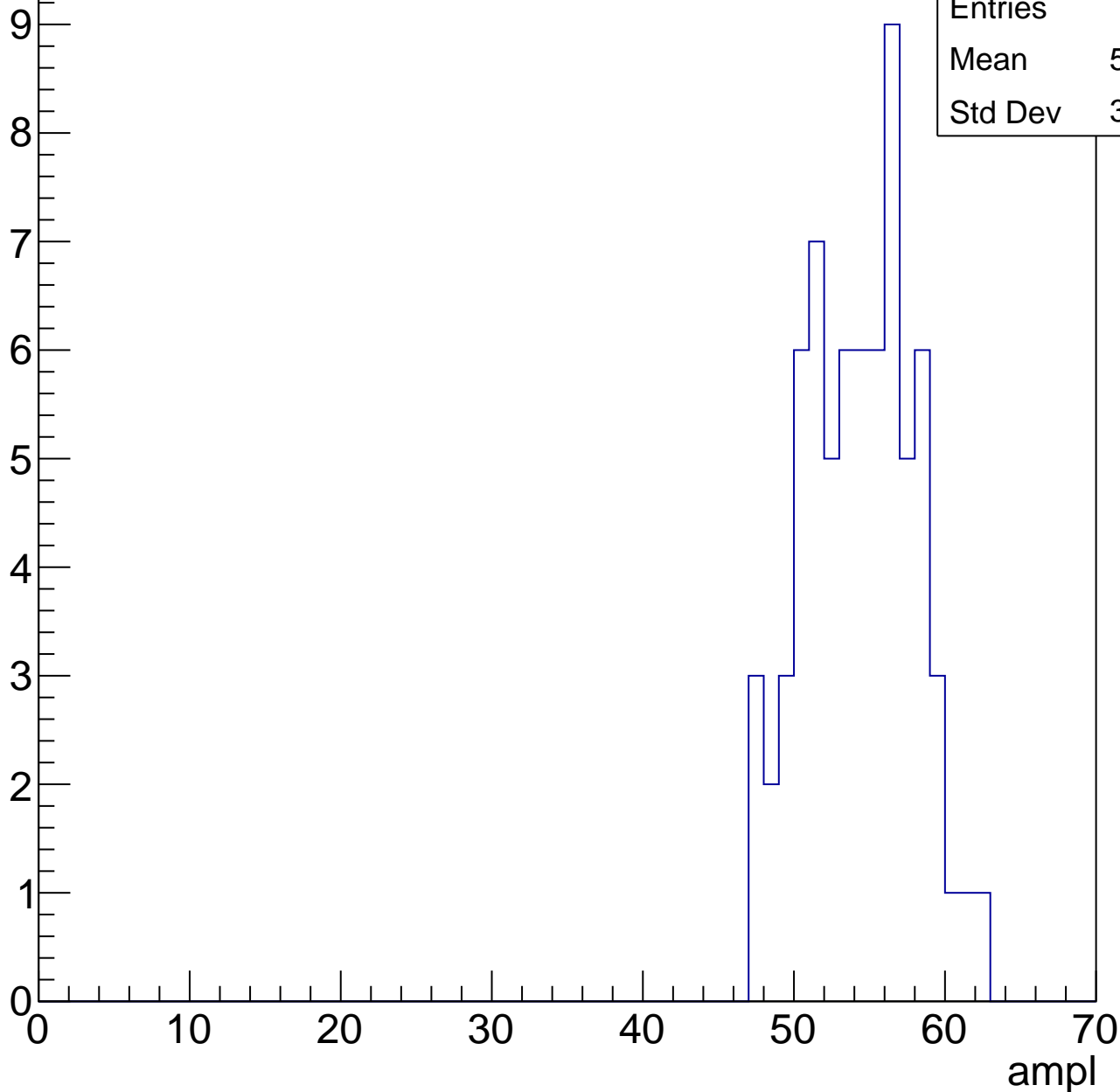


B1L103S, U23-ch69, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	53.86
Std Dev	3.555

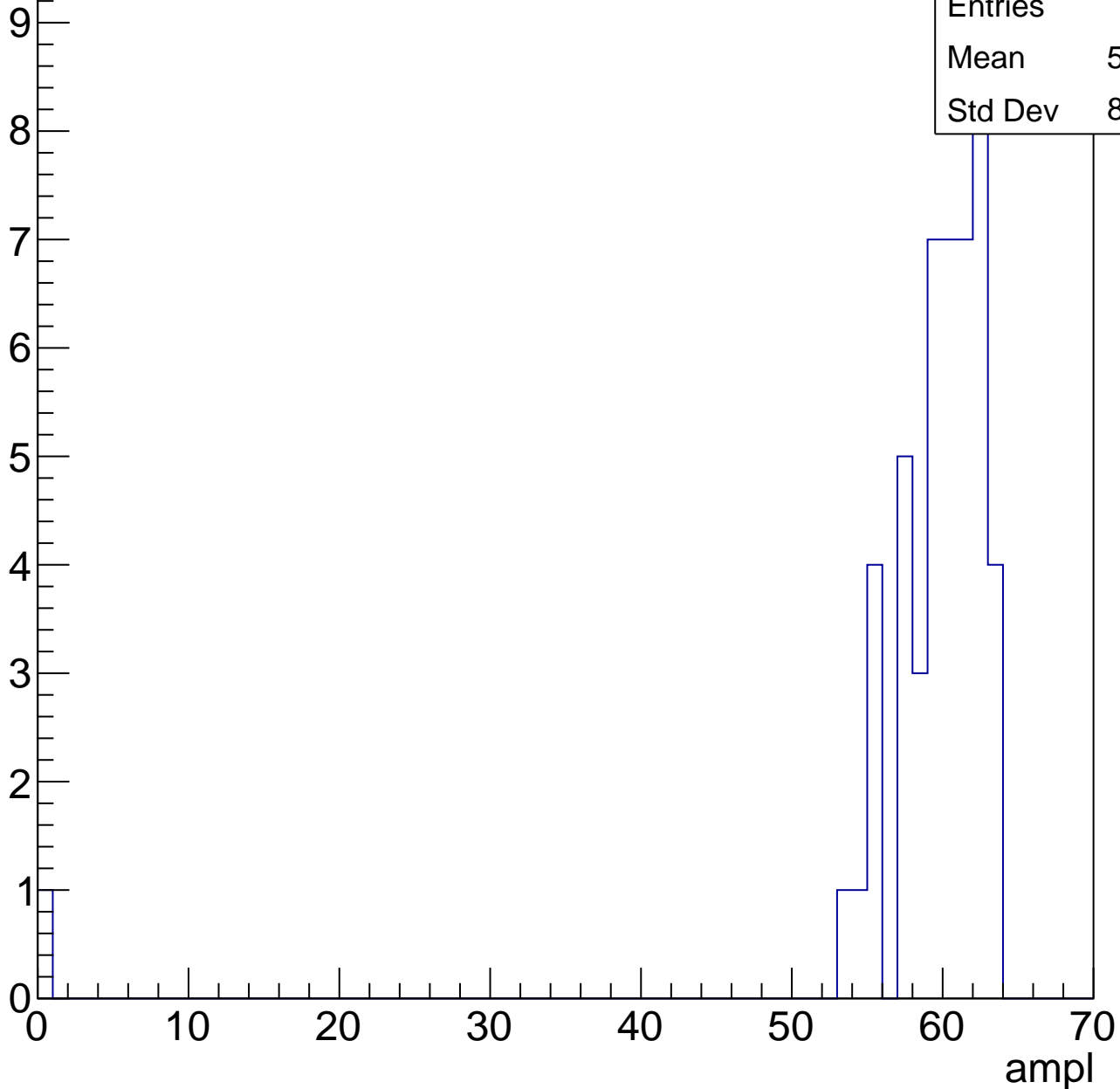


B1L103S, U23-ch69, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	49
Mean	58.29
Std Dev	8.788

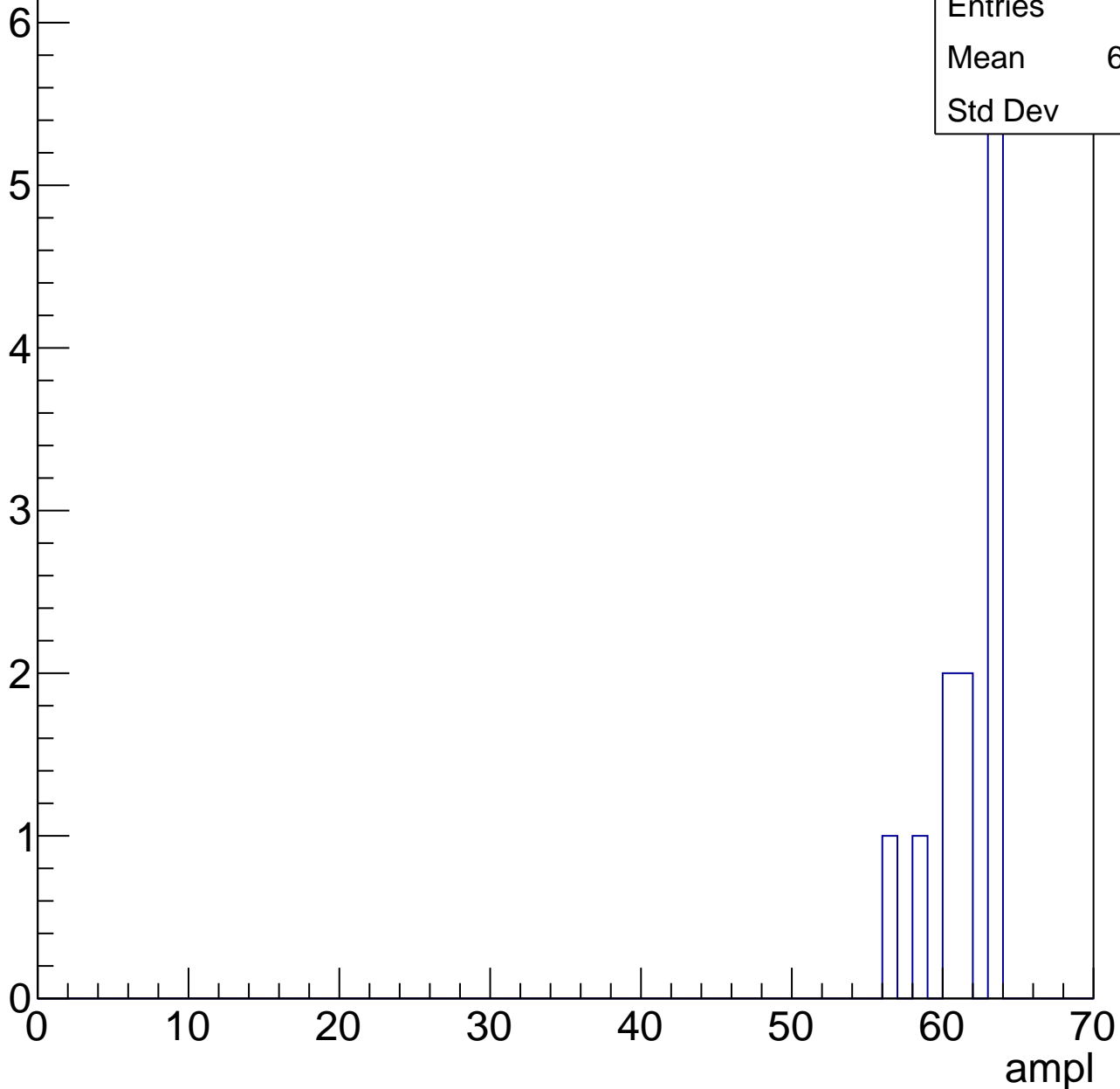


B1L103S, U23-ch69, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	12
Mean	61.17
Std Dev	2.23



B1L103S, U23-ch69, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



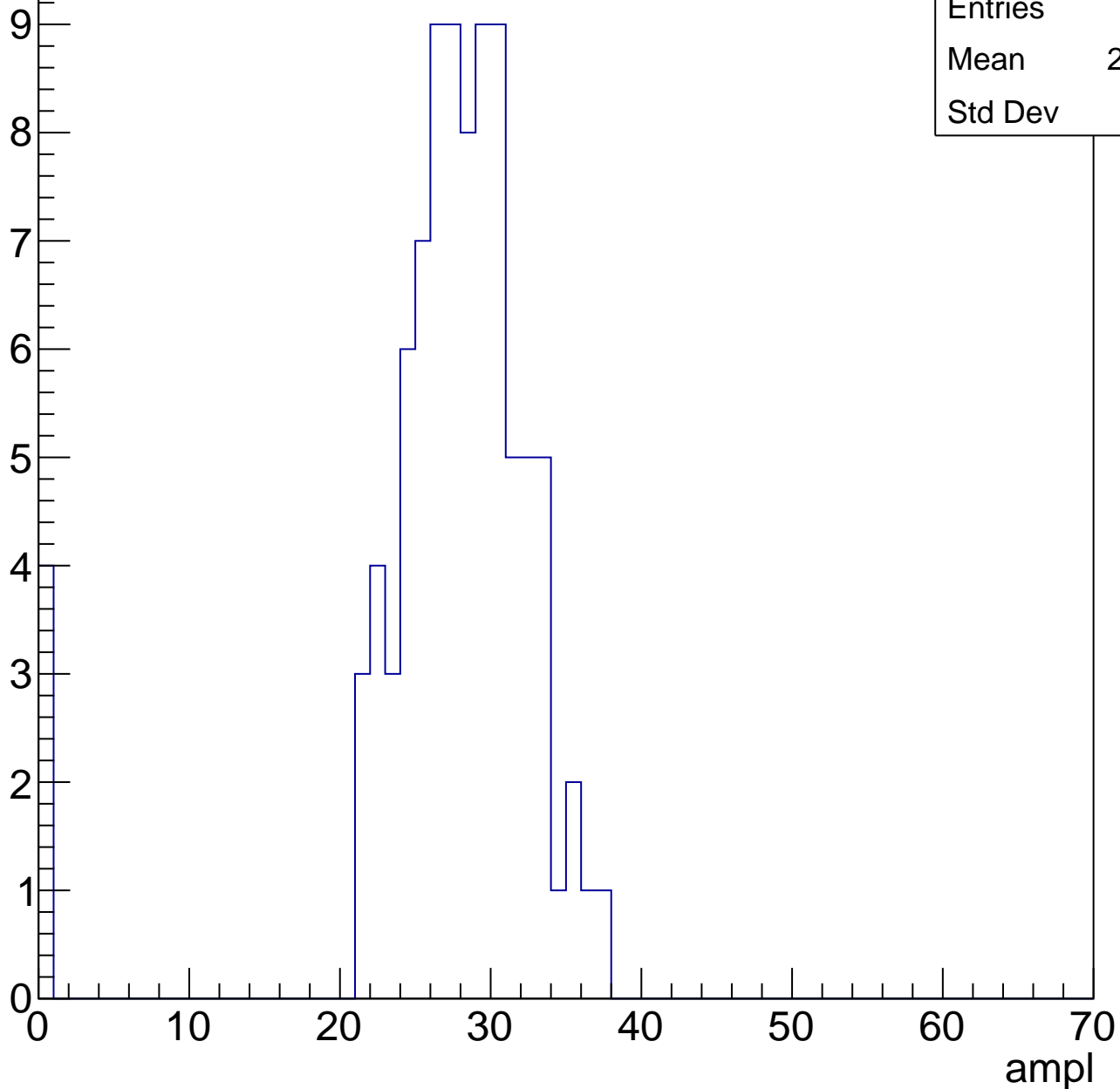
Entries	19
Mean	0
Std Dev	0

B1L103S, U23-ch70, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	91
Mean	26.68
Std Dev	6.73

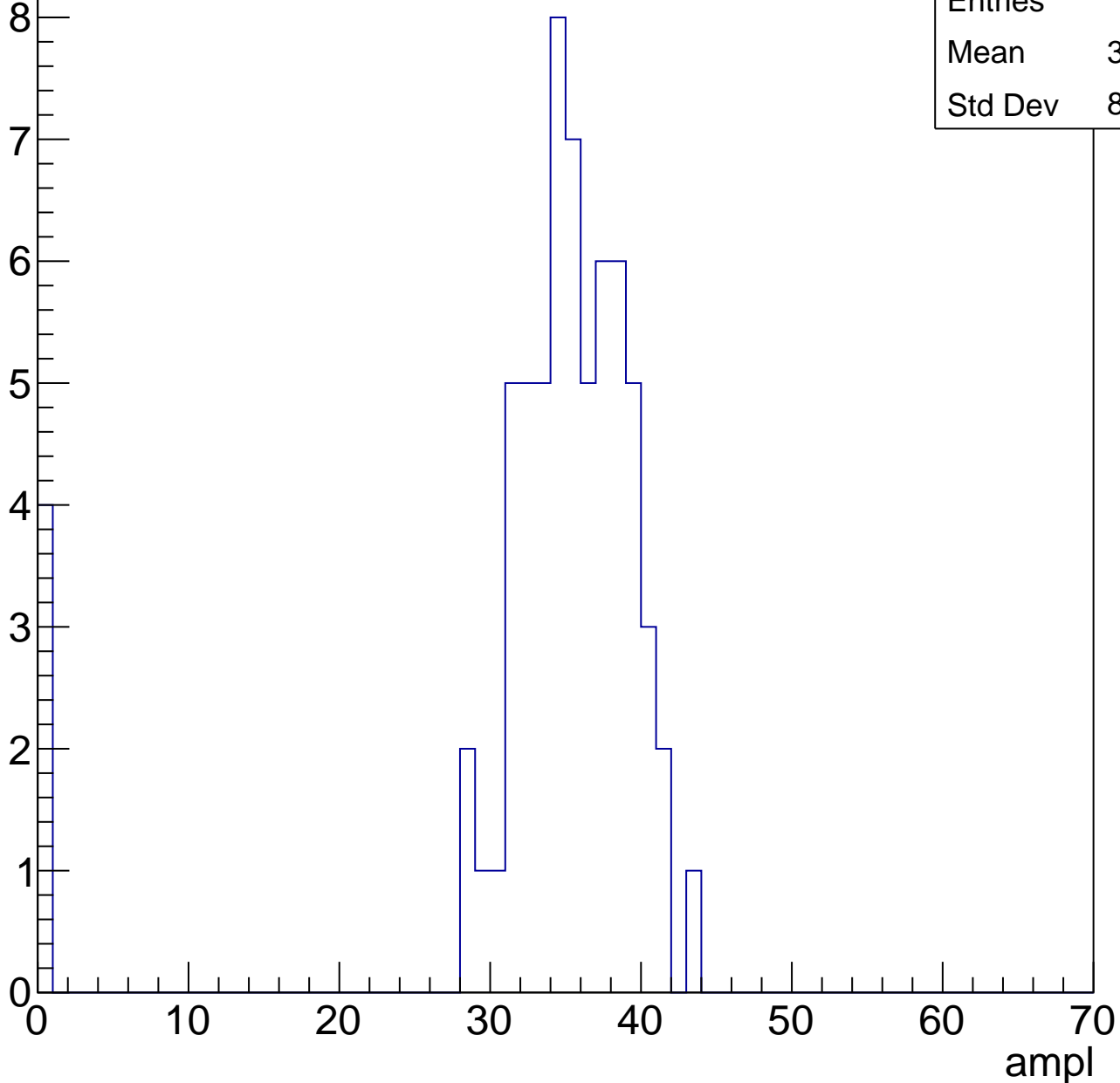


B1L103S, U23-ch70, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	33.06
Std Dev	8.993

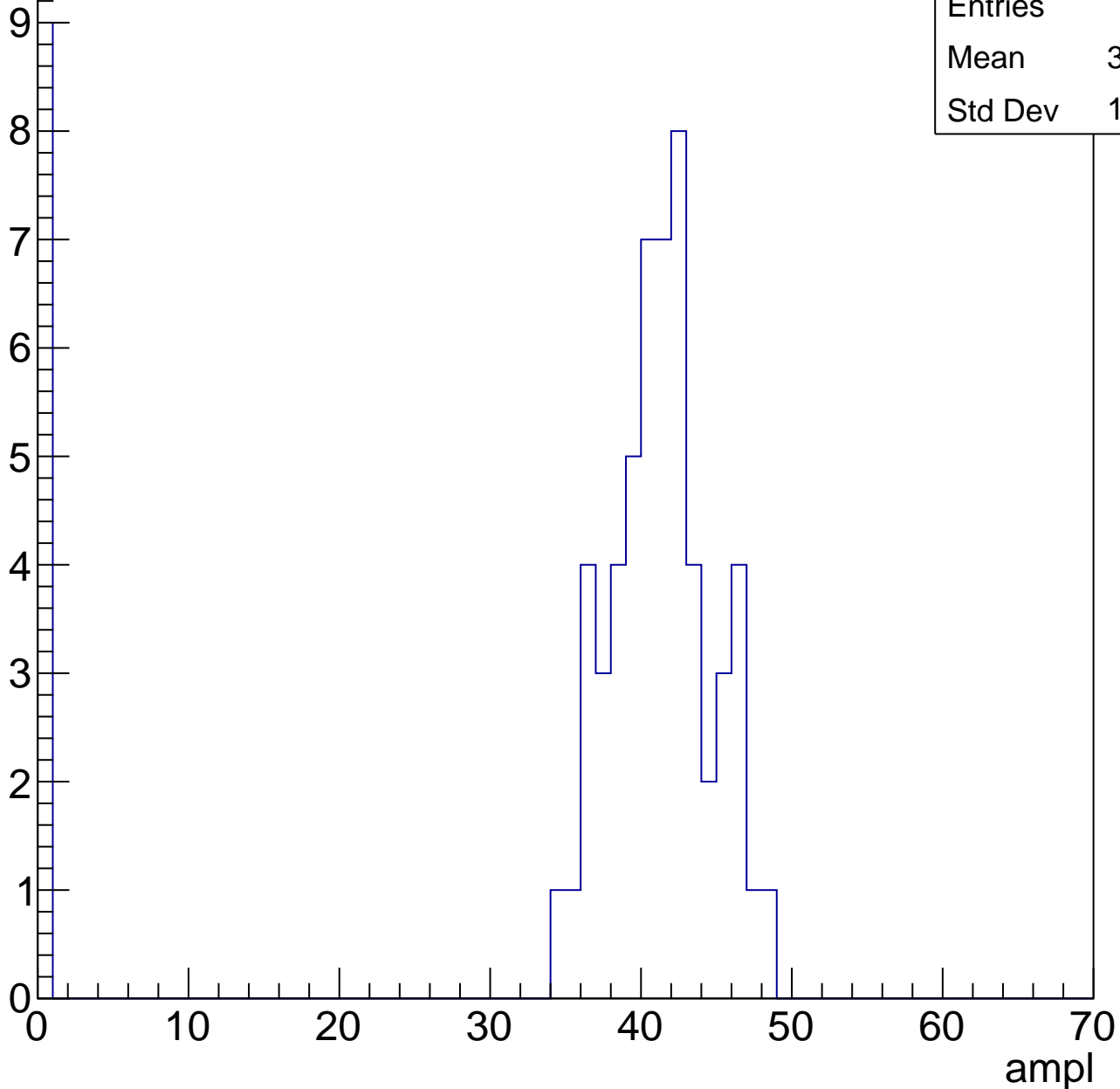


B1L103S, U23-ch70, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	35.12
Std Dev	14.52

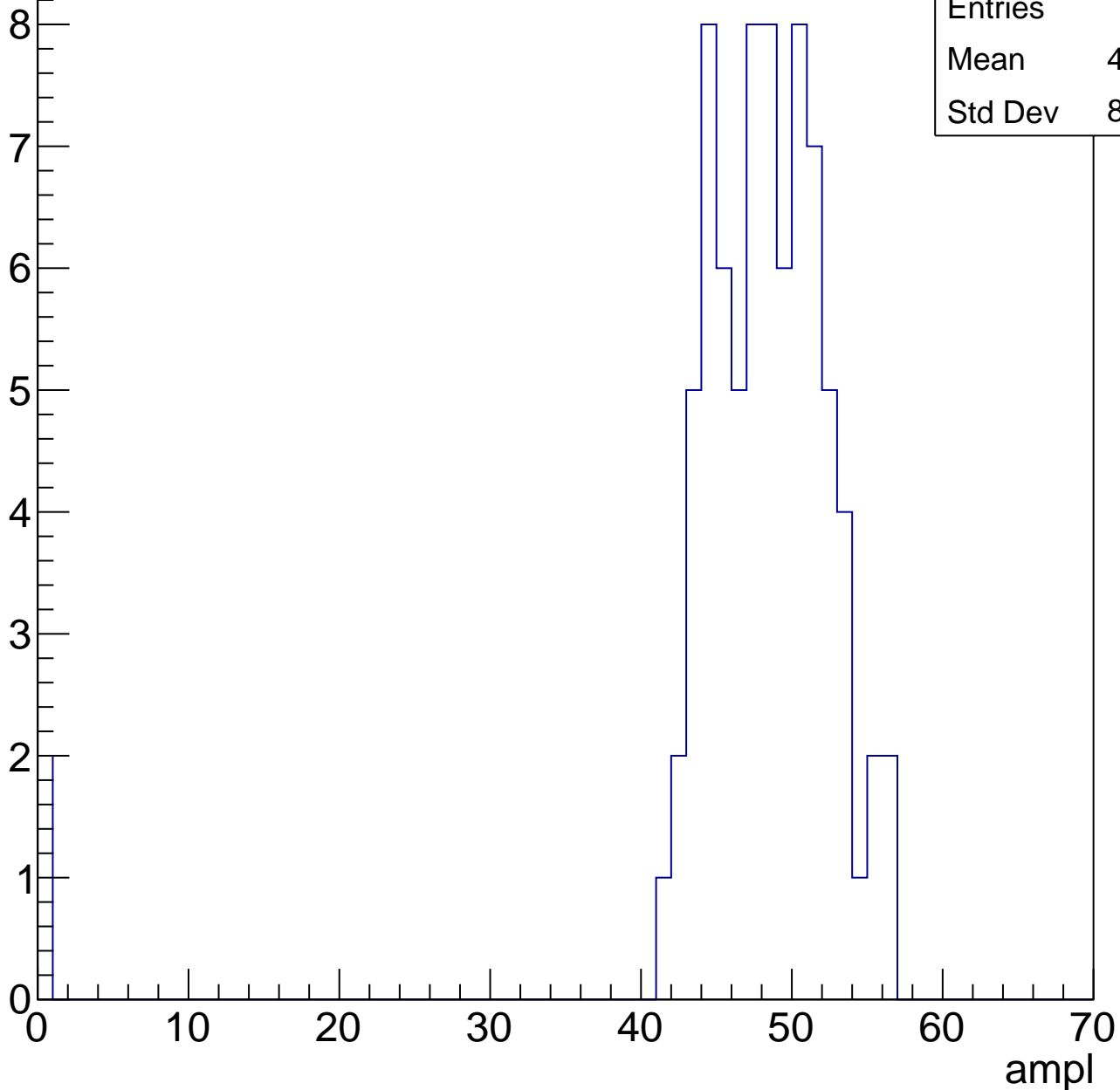


B1L103S, U23-ch70, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	80
Mean	46.89
Std Dev	8.298

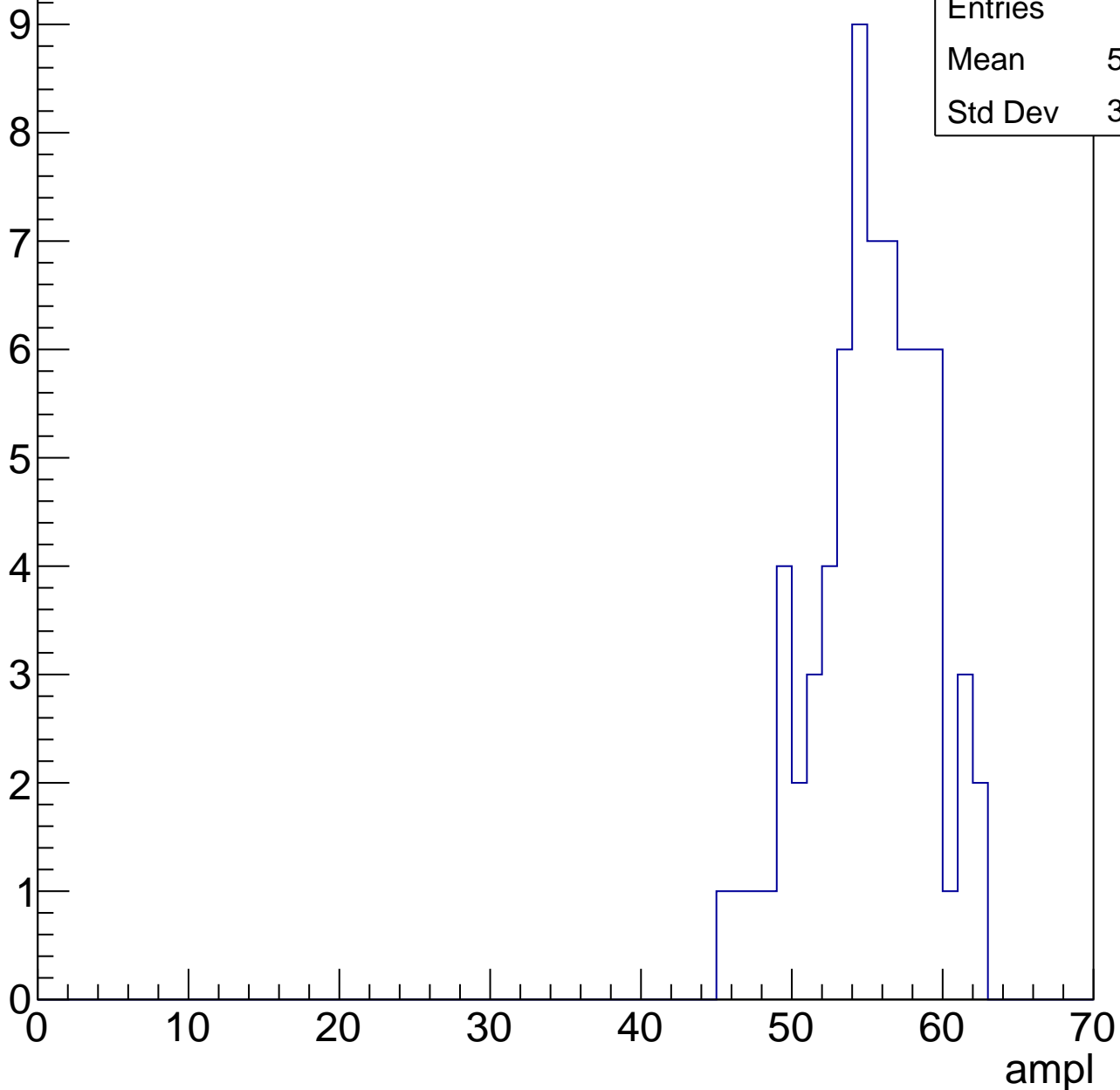


B1L103S, U23-ch70, adc4

calib_packv5_041523_1651.root, FC#0, port C2

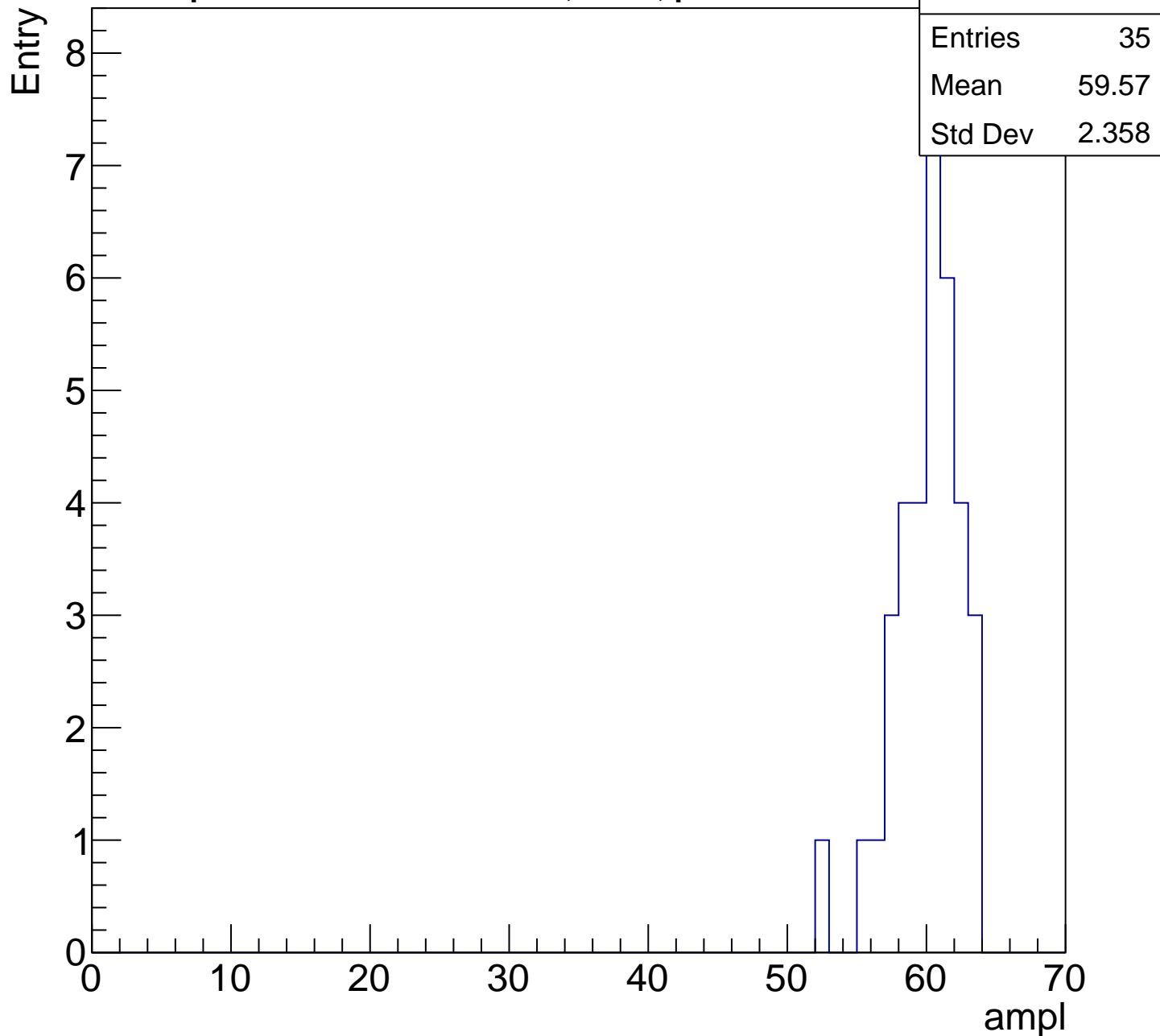
Entry

Entries	70
Mean	54.79
Std Dev	3.806



B1L103S, U23-ch70, adc5

calib_packv5_041523_1651.root, FC#0, port C2

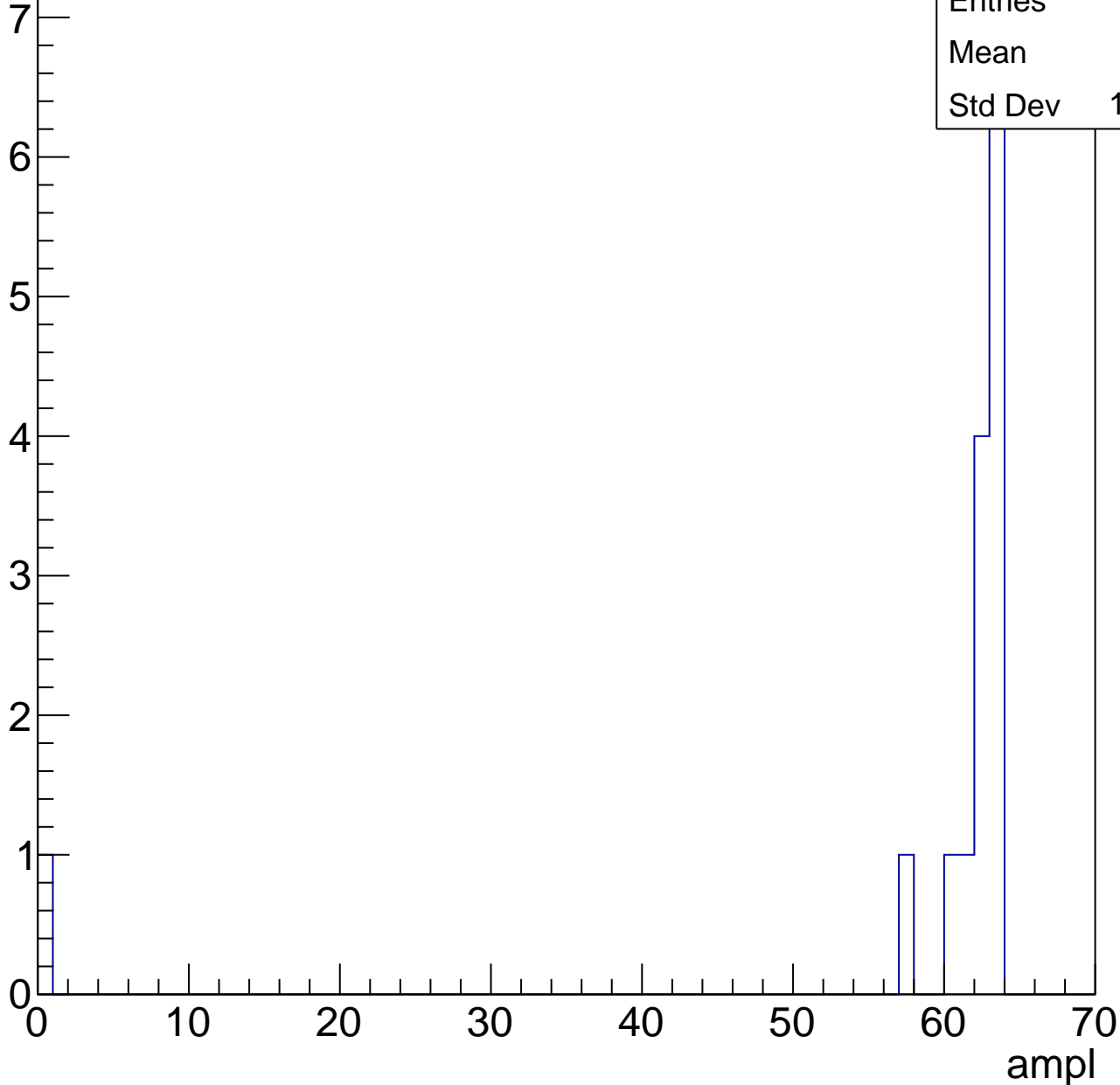


B1L103S, U23-ch70, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	15
Mean	57.8
Std Dev	15.53

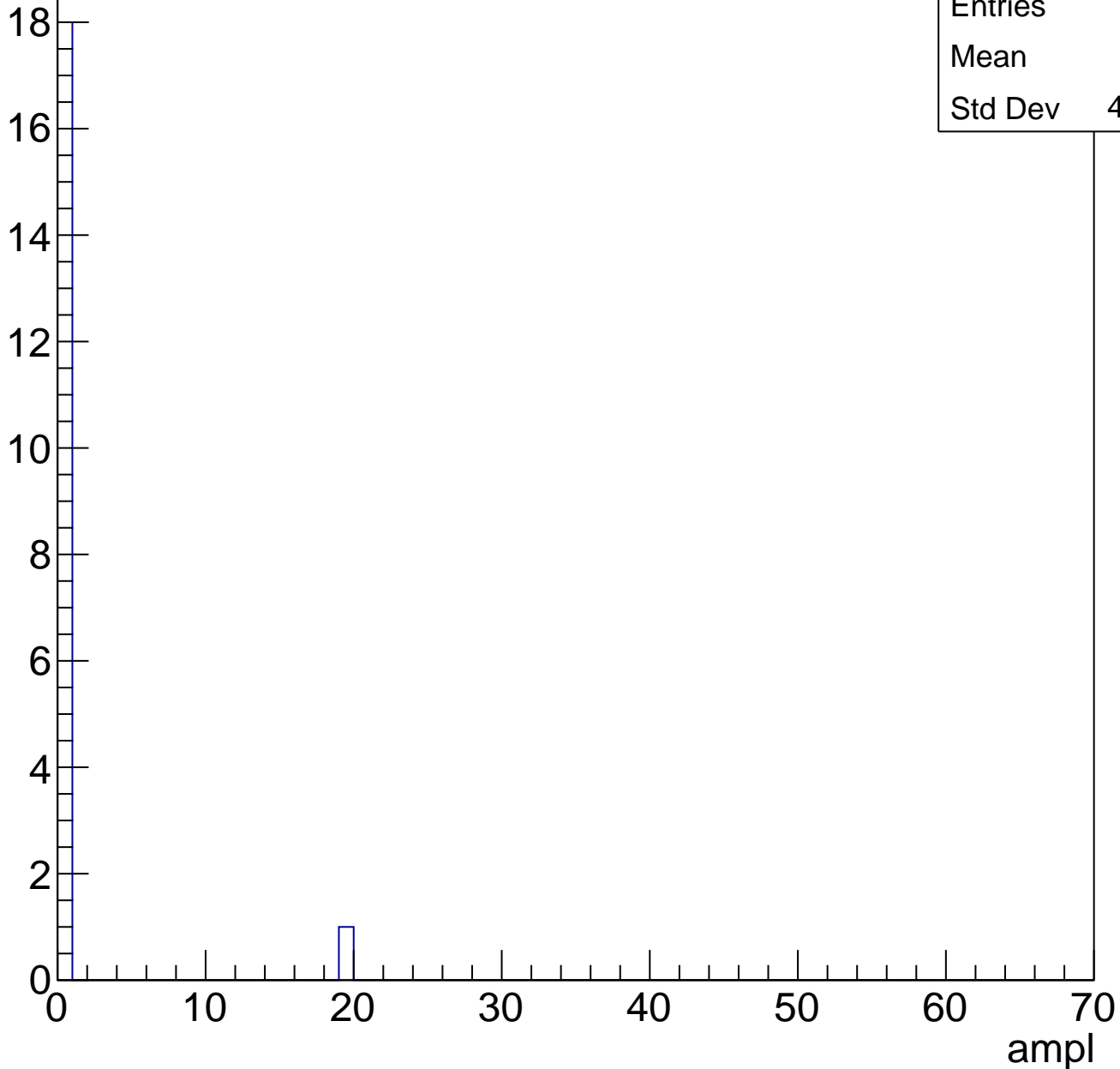


B1L103S, U23-ch70, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1
Std Dev	4.243

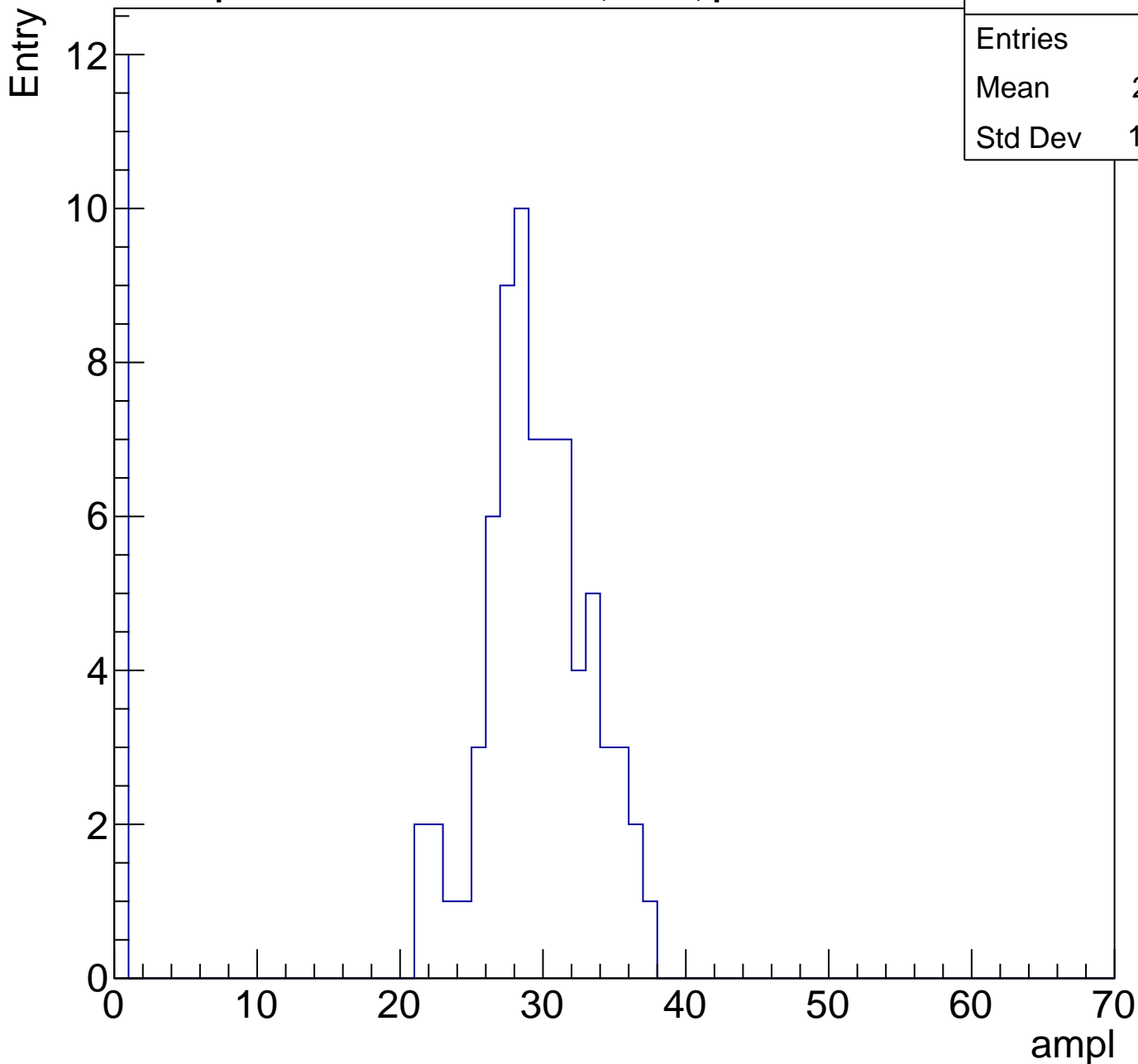
Entry



B1L103S, U23-ch71, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	85
Mean	25.01
Std Dev	10.67

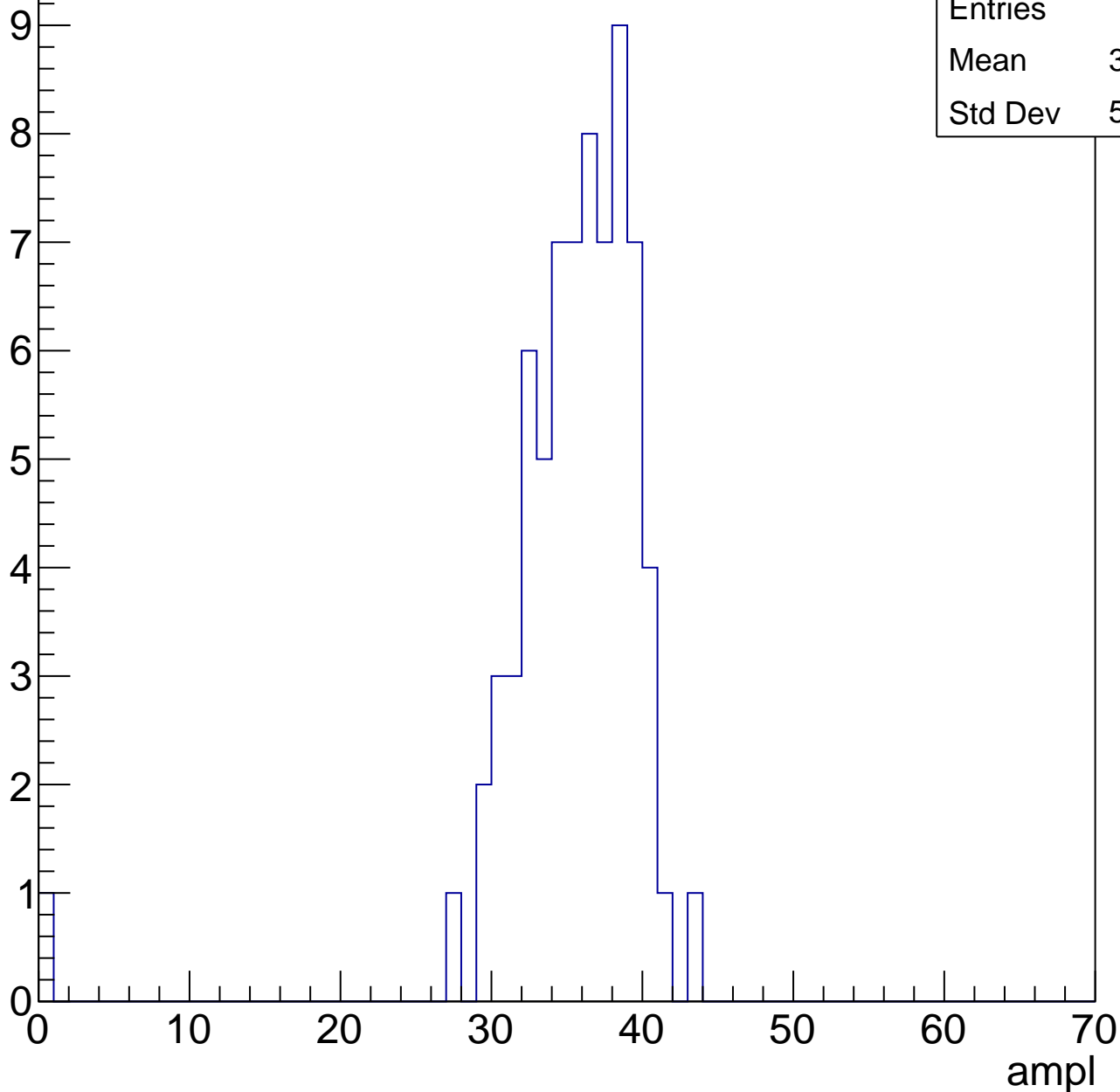


B1L103S, U23-ch71, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	72
Mean	34.92
Std Dev	5.262



B1L103S, U23-ch71, adc2

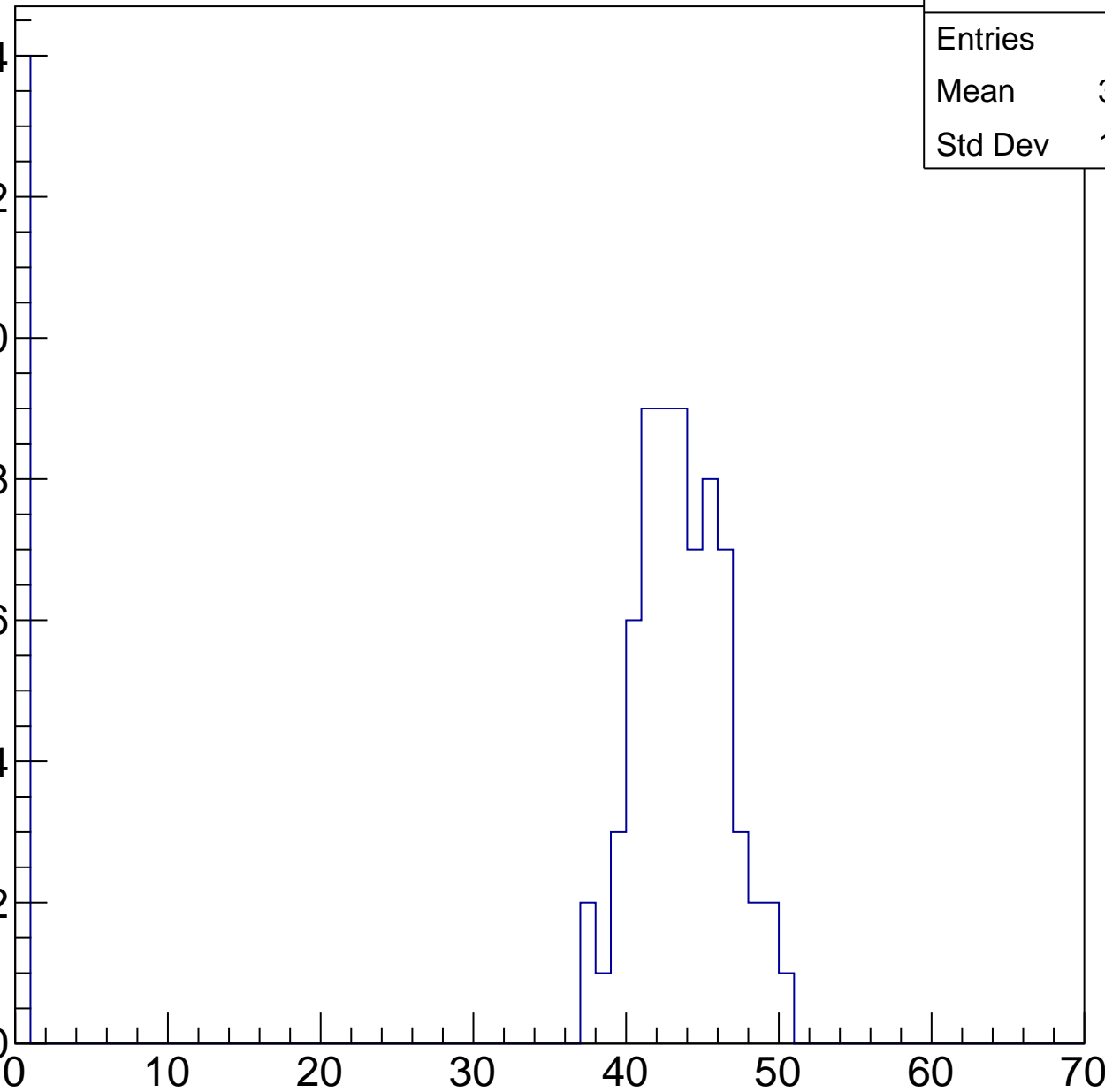
calib_packv5_041523_1651.root, FC#0, port C2

Entries	83
Mean	35.88
Std Dev	16.37

Entry

14
12
10
8
6
4
2
0

ampl

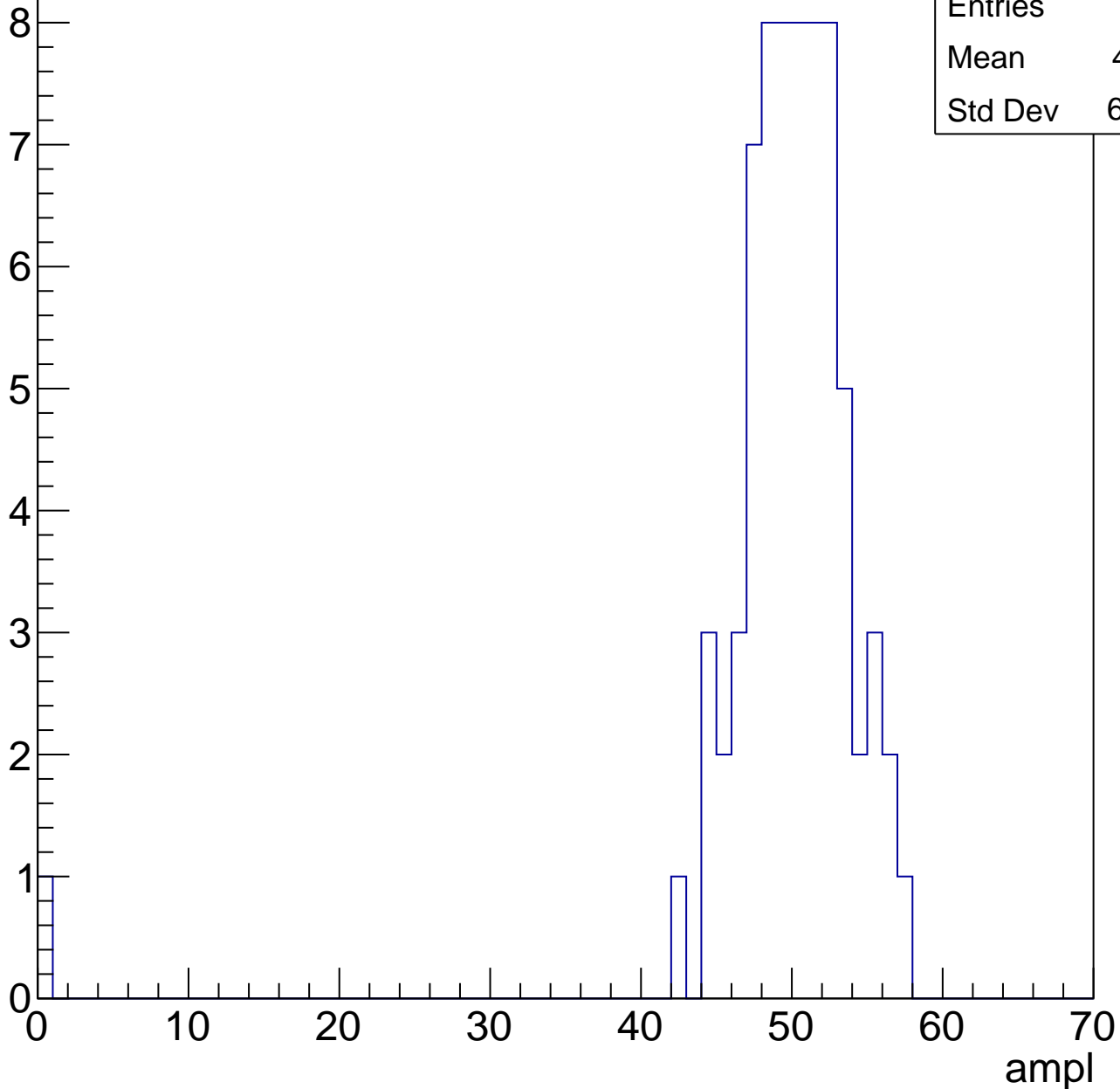


B1L103S, U23-ch71, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	49.11
Std Dev	6.688

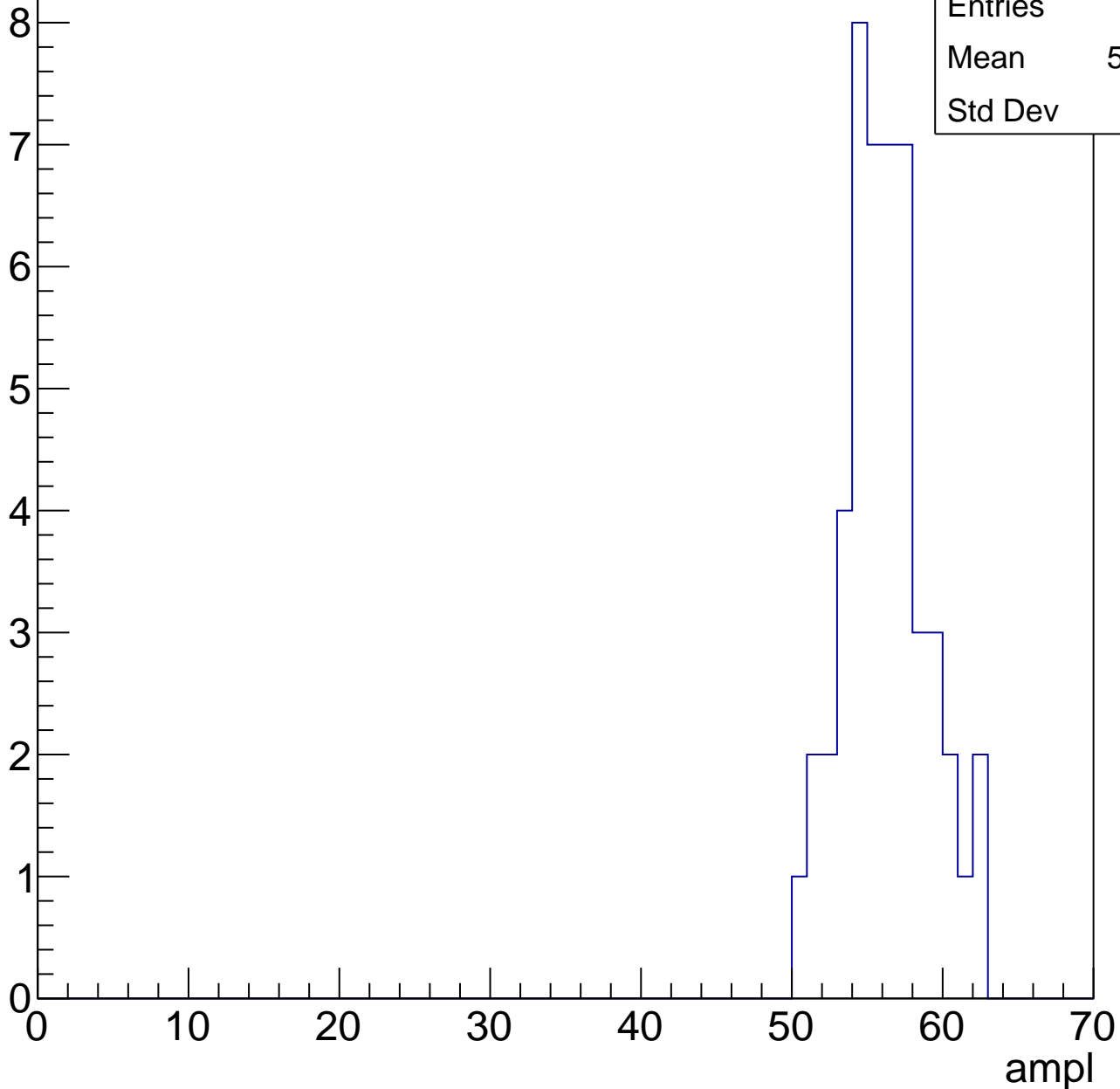


B1L103S, U23-ch71, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	49
Mean	55.76
Std Dev	2.73

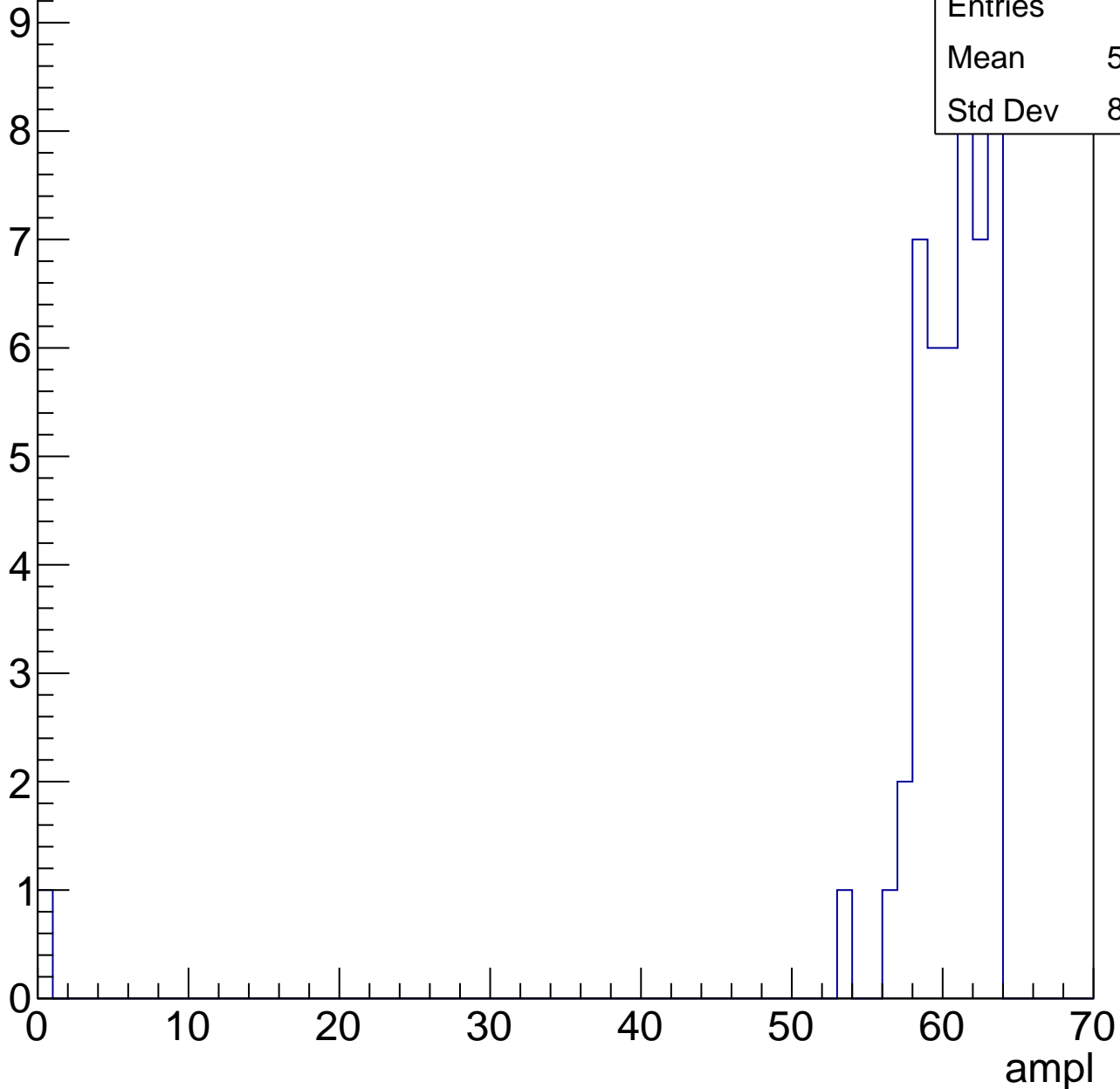


B1L103S, U23-ch71, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

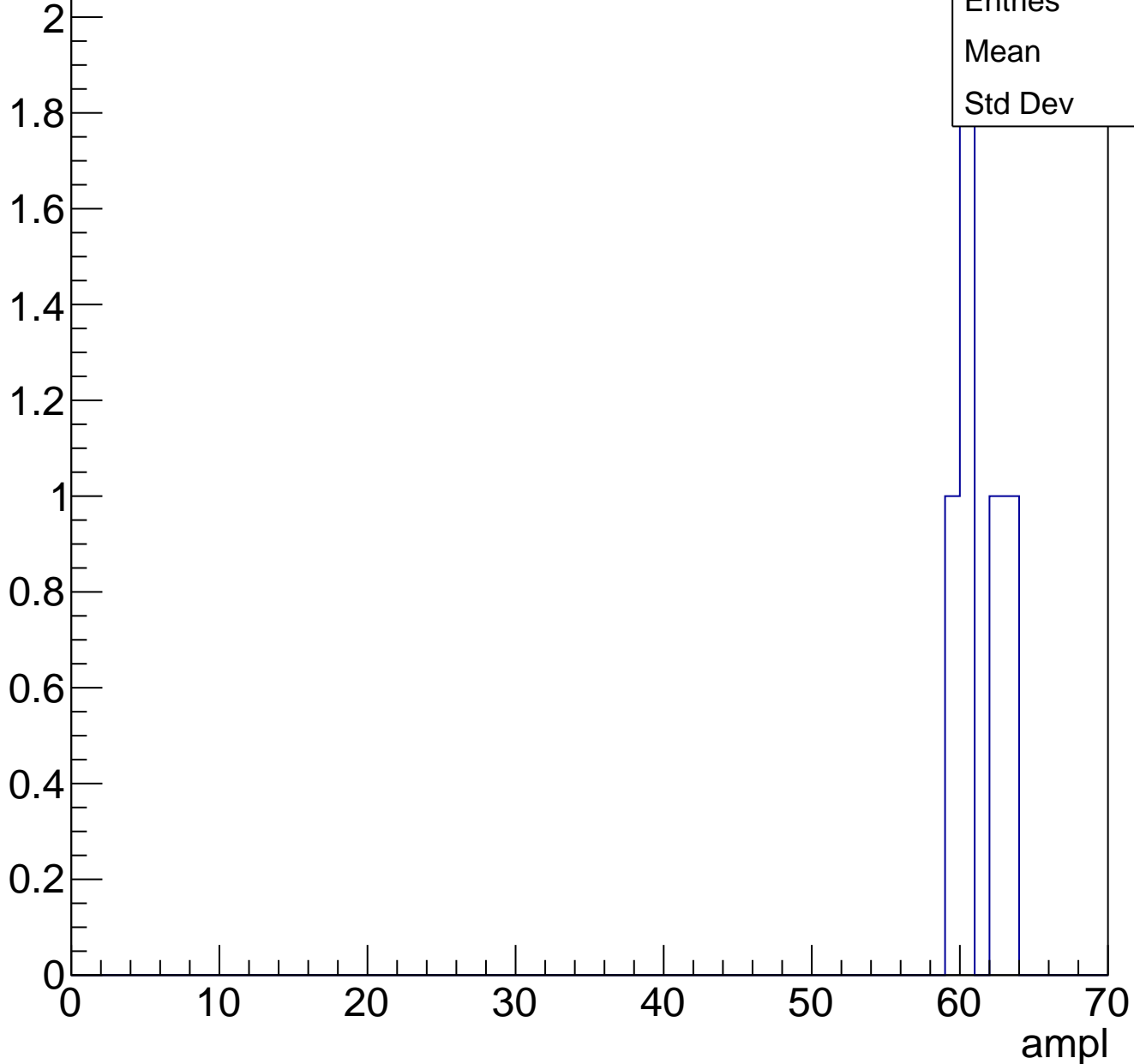
Entries	49
Mean	59.04
Std Dev	8.795



B1L103S, U23-ch71, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch71, adc7

calib_packv5_041523_1651.root, FC#0, port C2

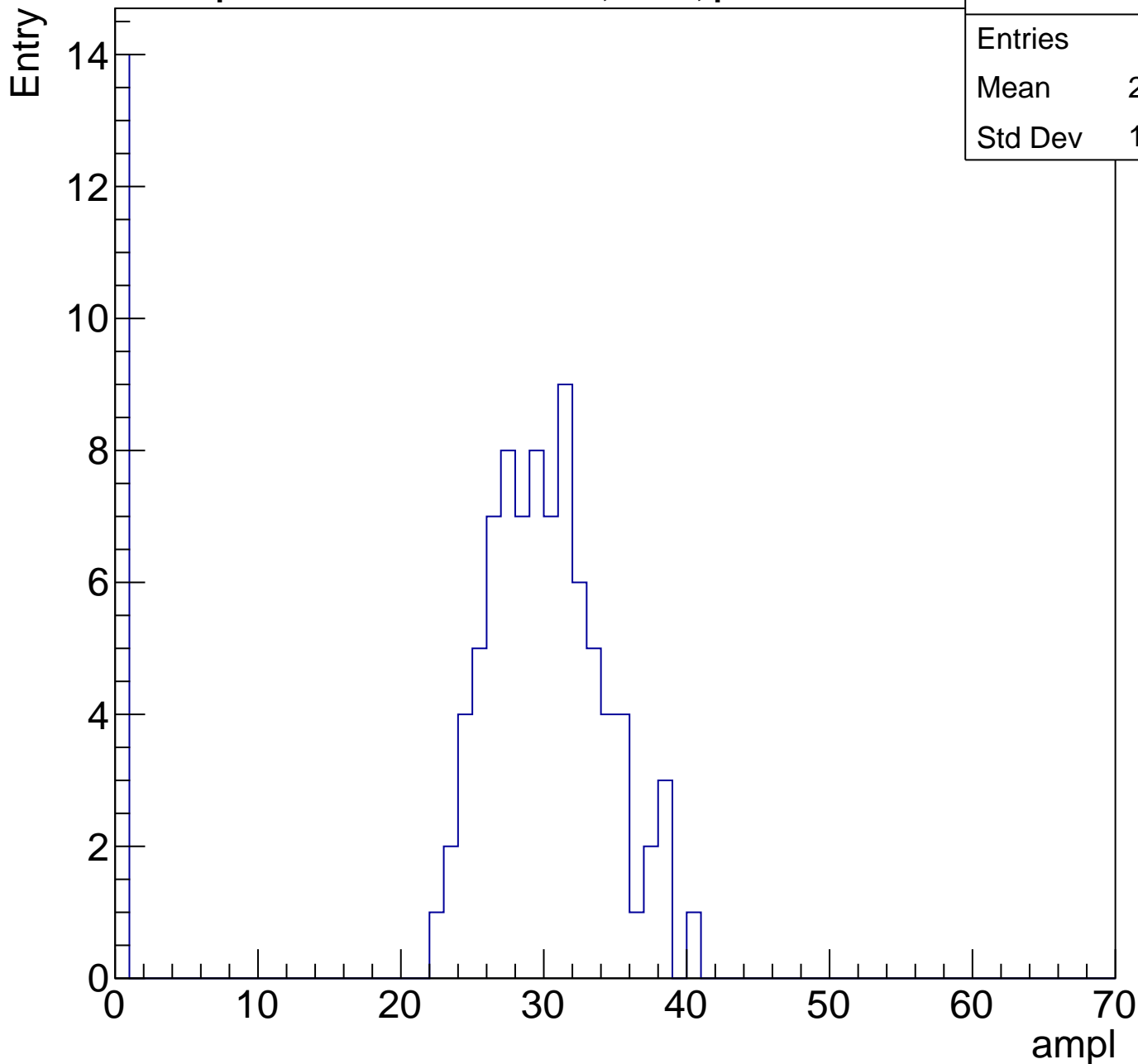
Entry



B1L103S, U23-ch72, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	98
Mean	25.52
Std Dev	11.04

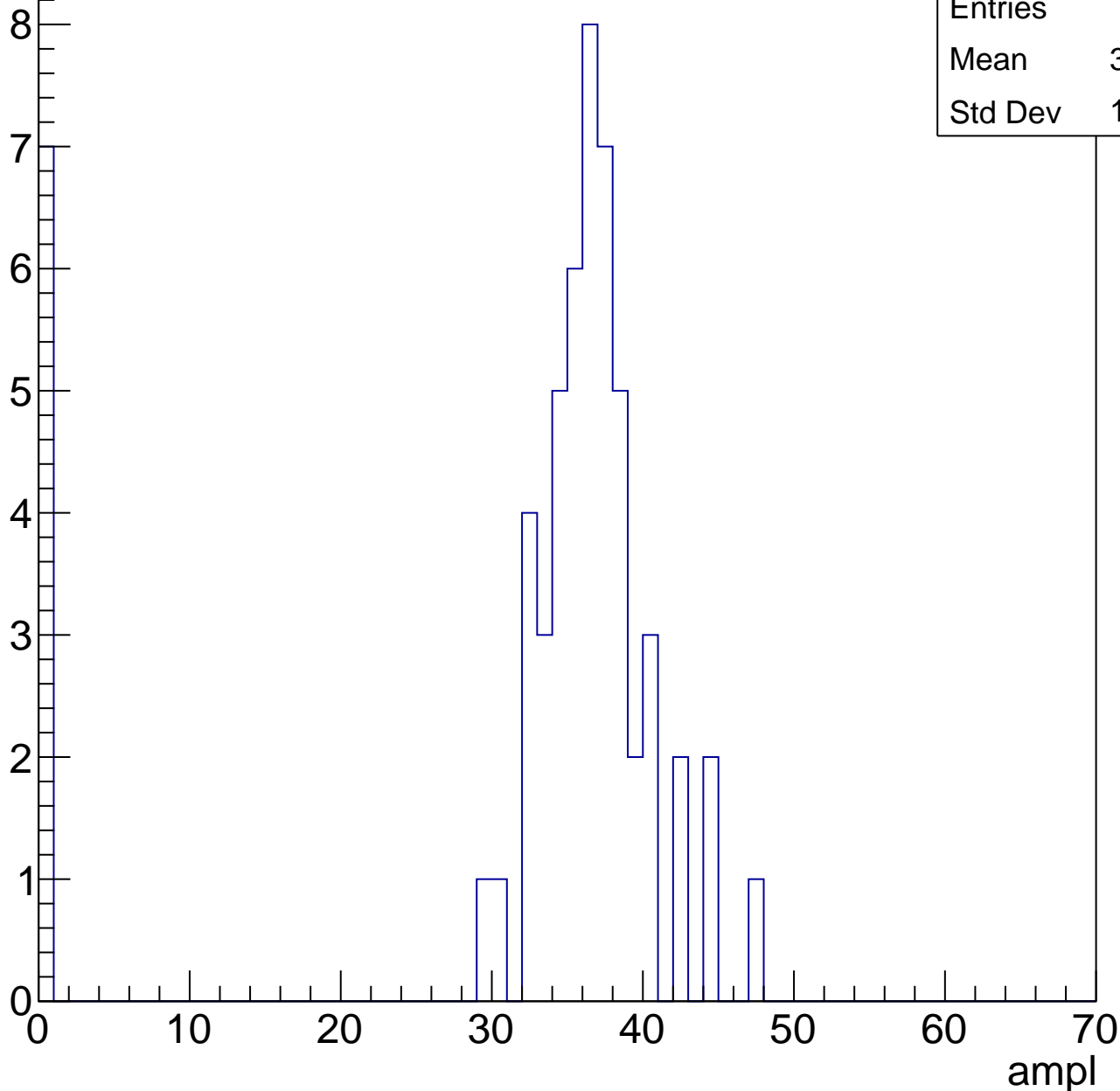


B1L103S, U23-ch72, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	57
Mean	31.93
Std Dev	12.39



B1L103S, U23-ch72, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	80
Mean	41.81
Std Dev	7.647

Entry

10

8

6

4

2

0

0

10

20

30

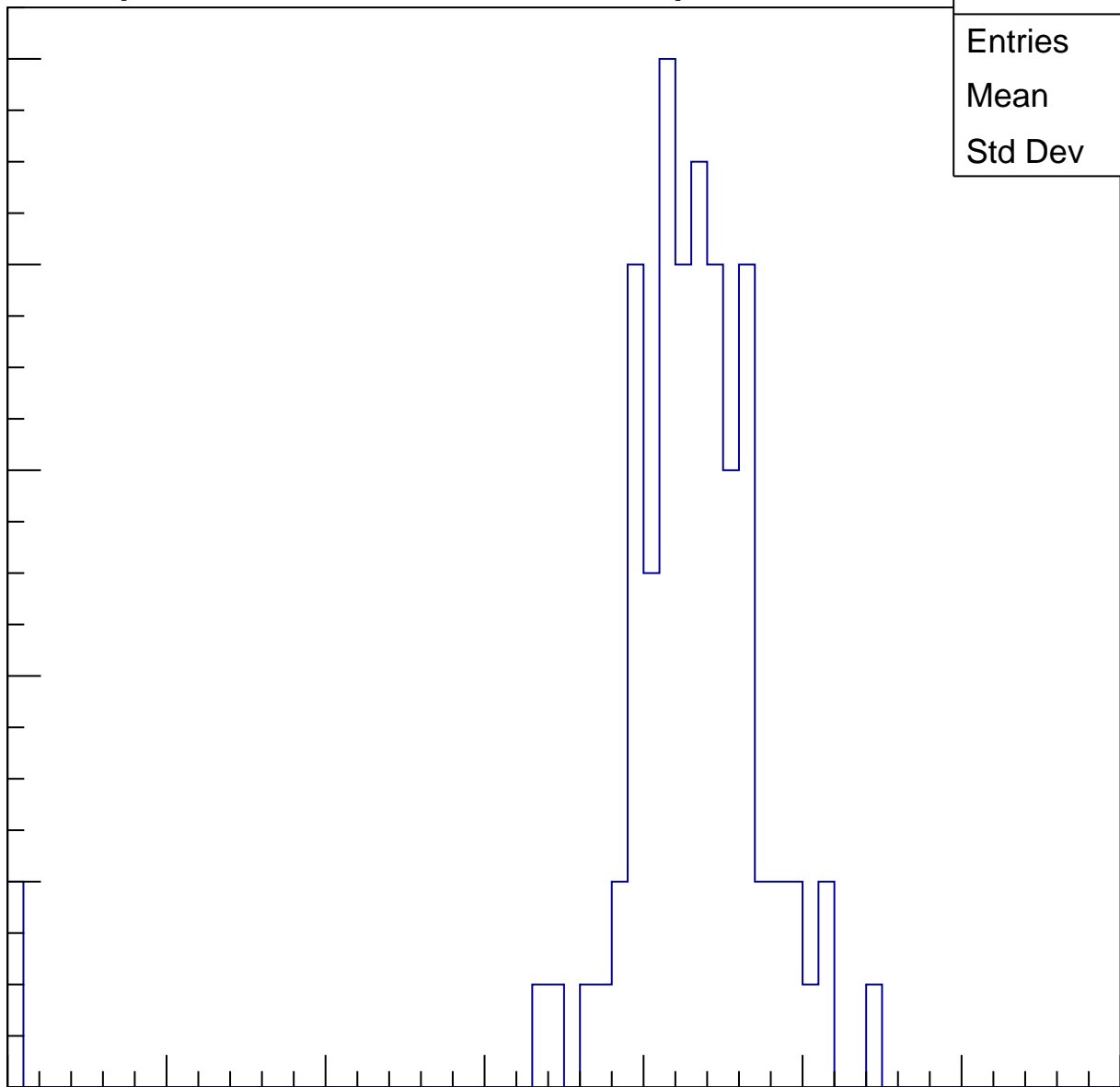
40

50

60

70

ampl

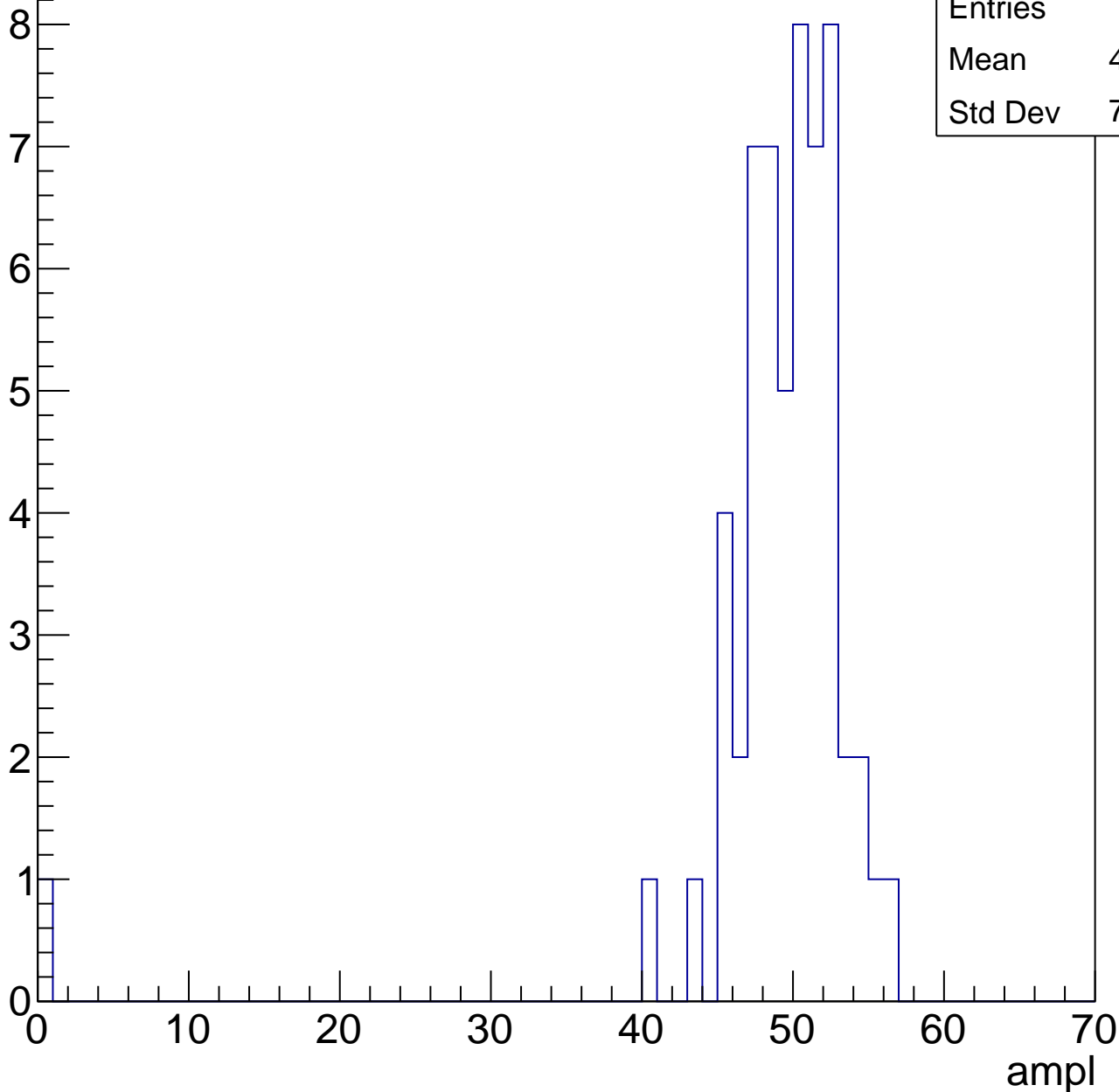


B1L103S, U23-ch72, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	57
Mean	48.47
Std Dev	7.126

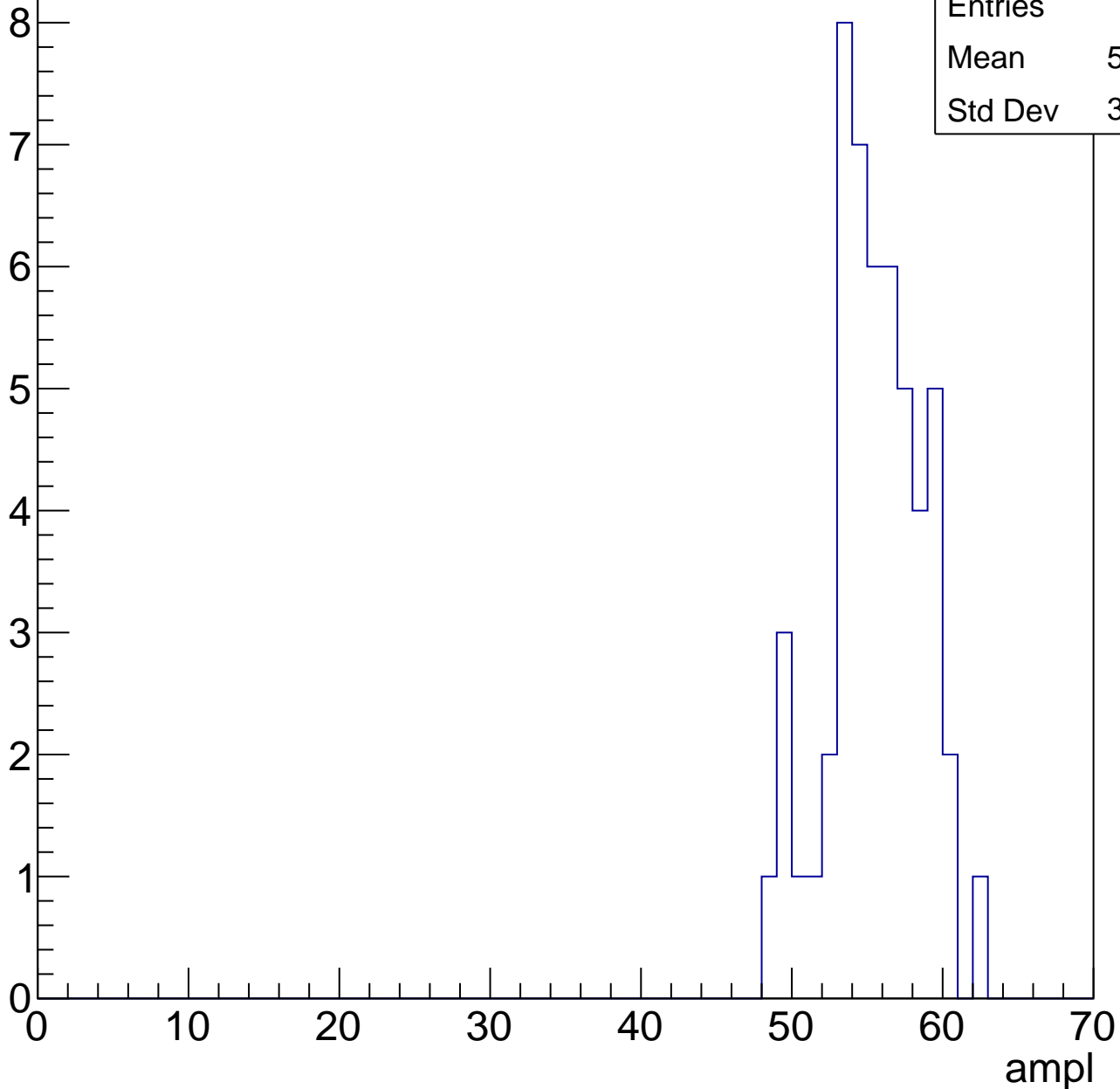


B1L103S, U23-ch72, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

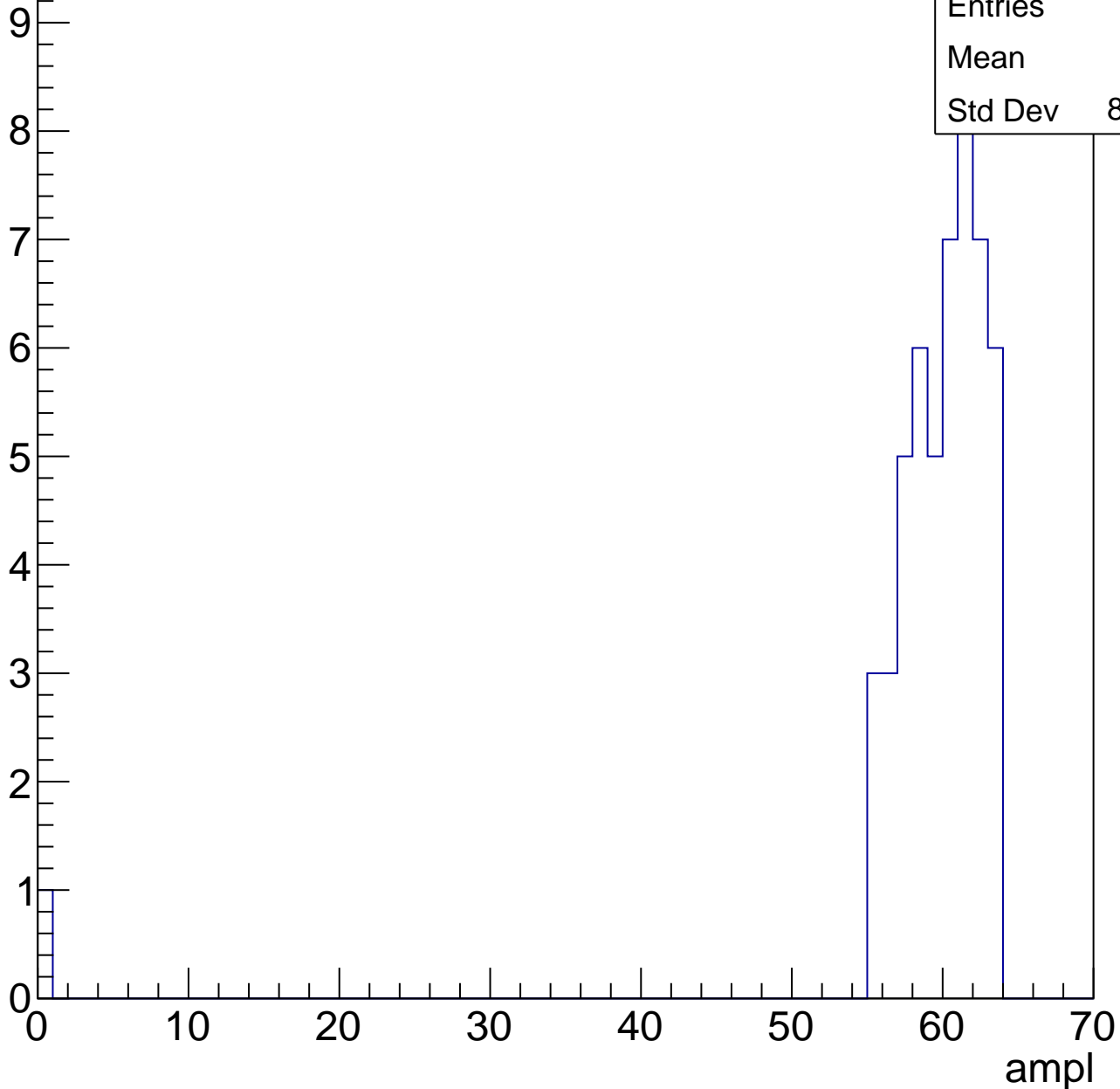
Entries	52
Mean	55.04
Std Dev	3.088



B1L103S, U23-ch72, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch72, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

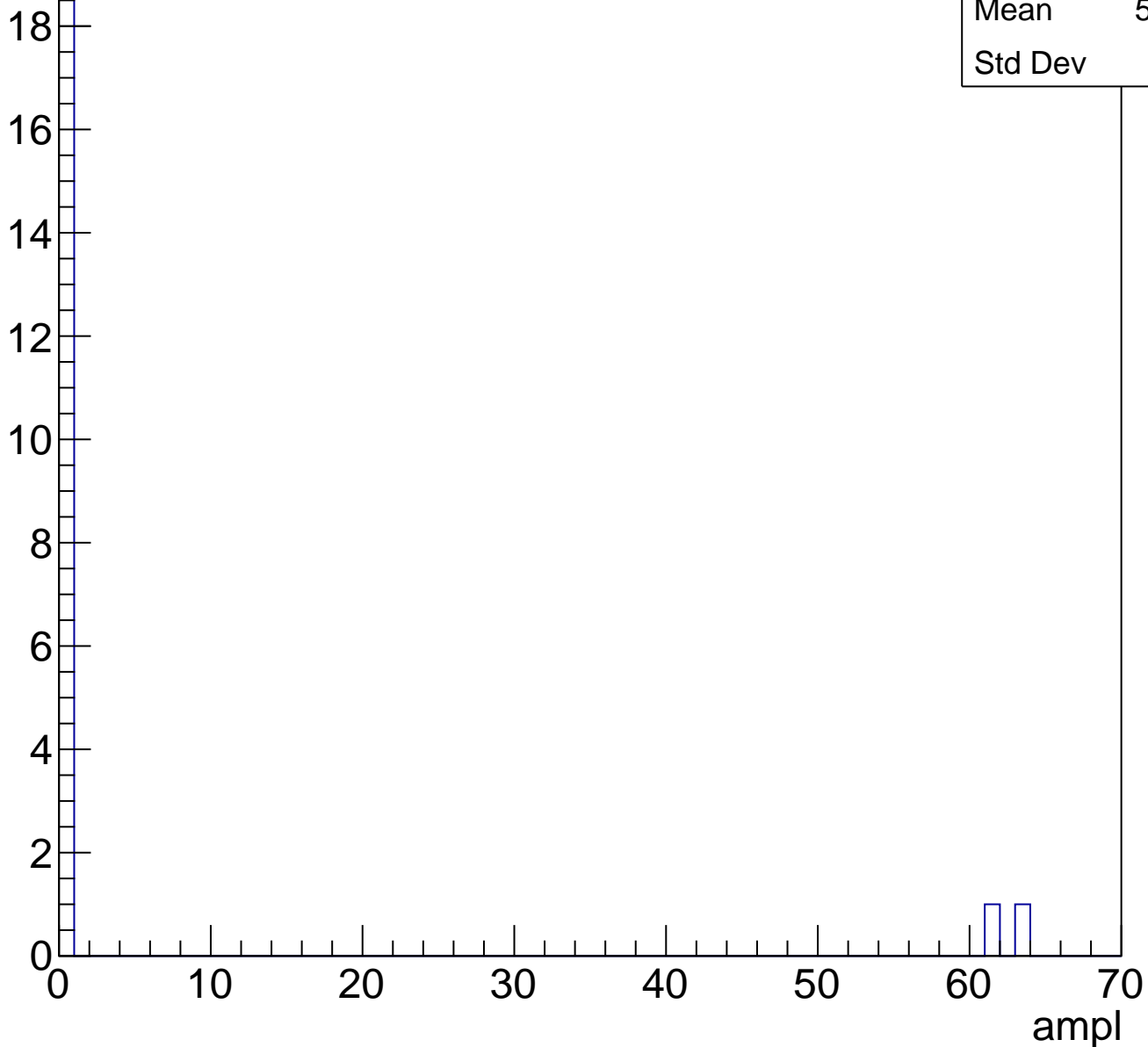


B1L103S, U23-ch72, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	21
Mean	5.905
Std Dev	18.2

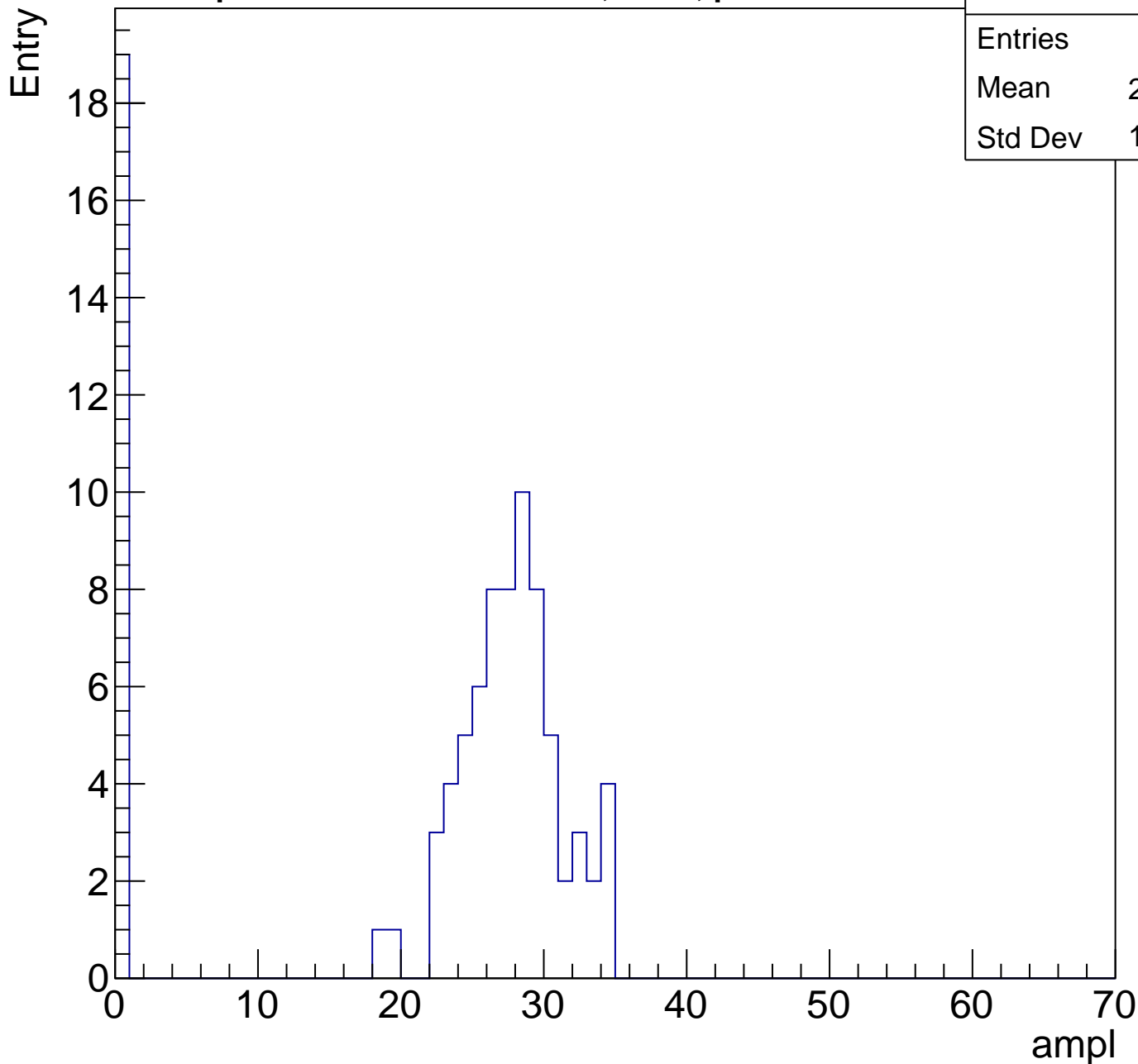
Entry



B1L103S, U23-ch73, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	89
Mean	21.47
Std Dev	11.59

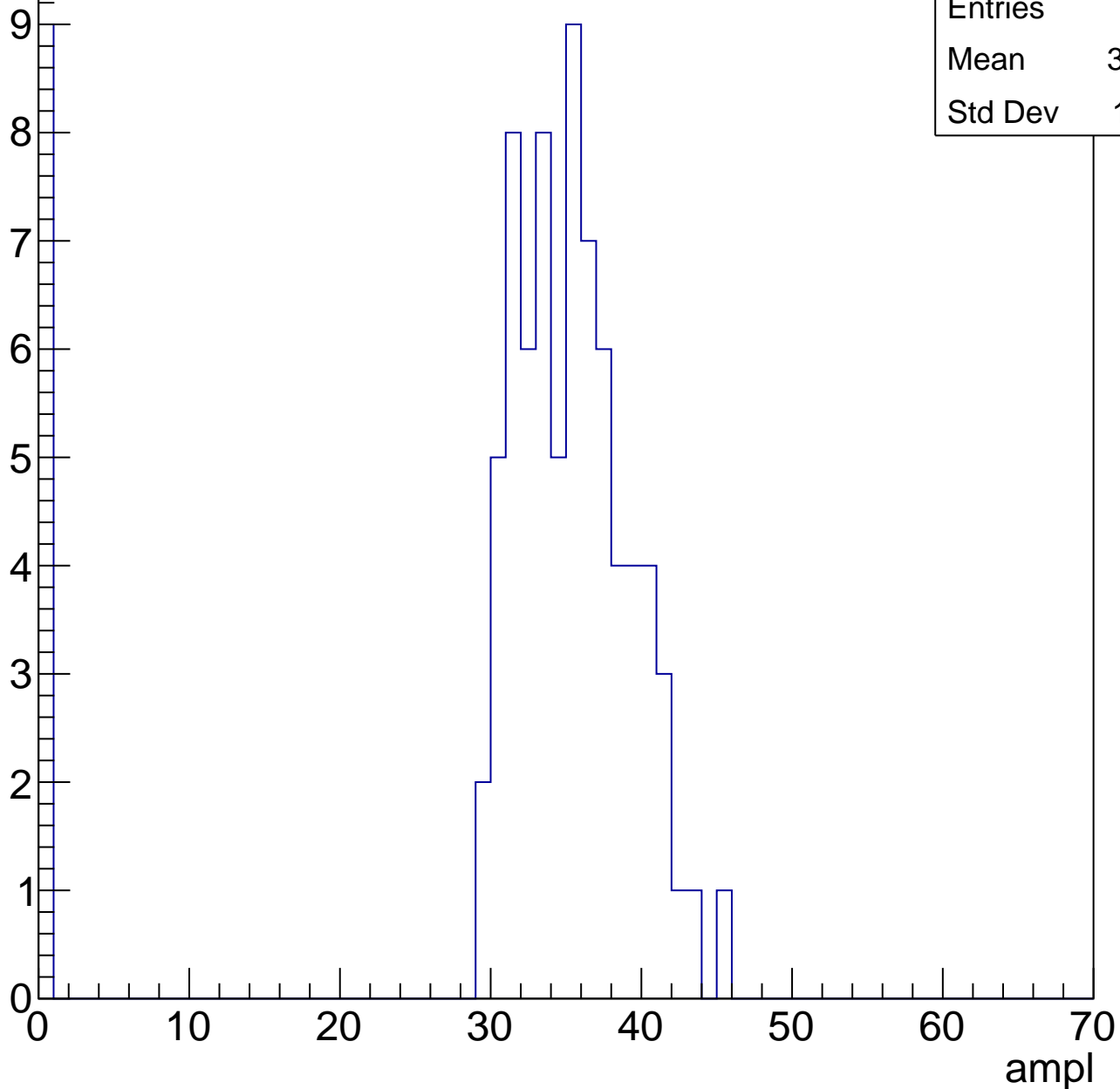


B1L103S, U23-ch73, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	83
Mean	31.23
Std Dev	11.41

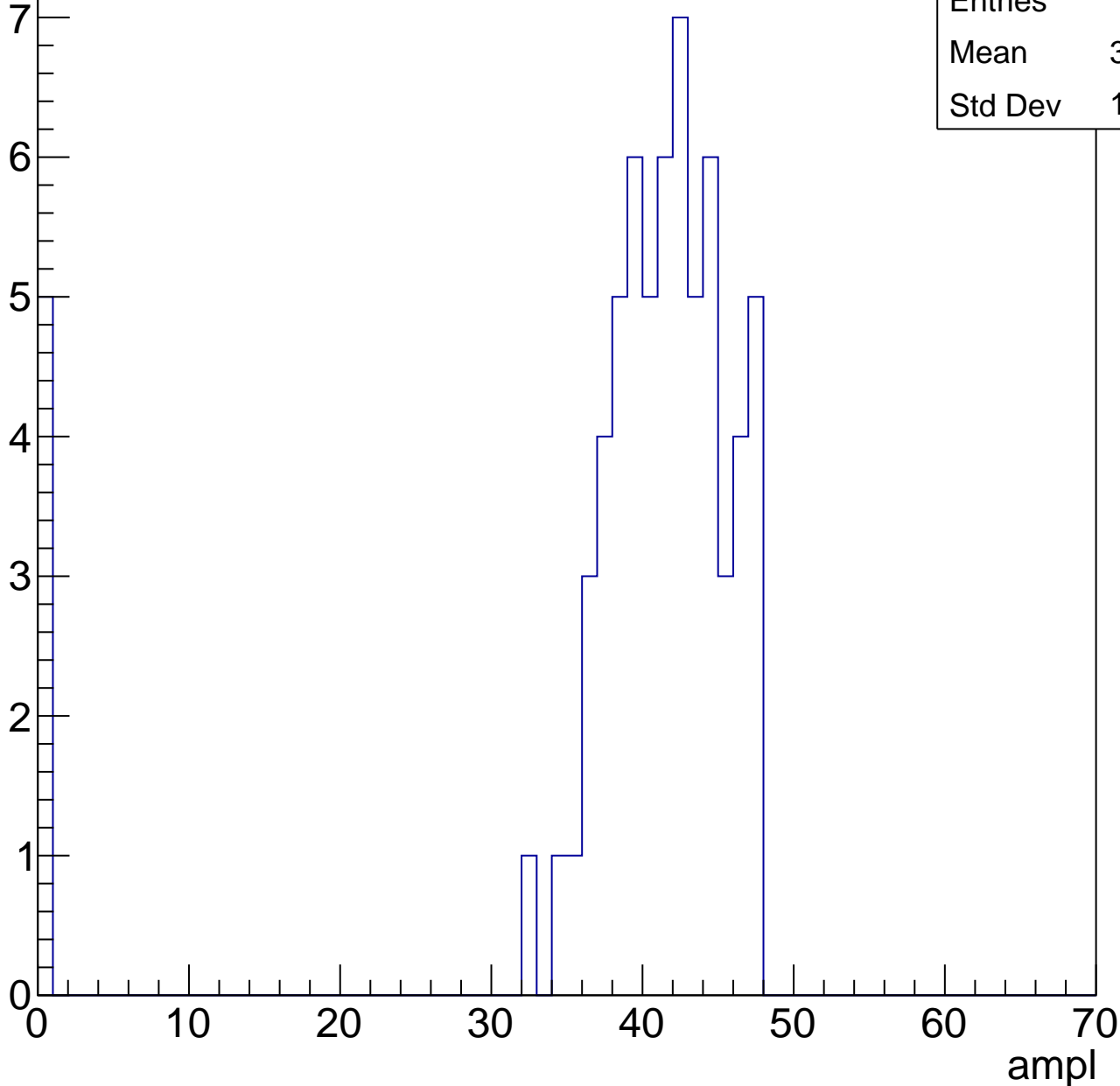


B1L103S, U23-ch73, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	38.12
Std Dev	11.35

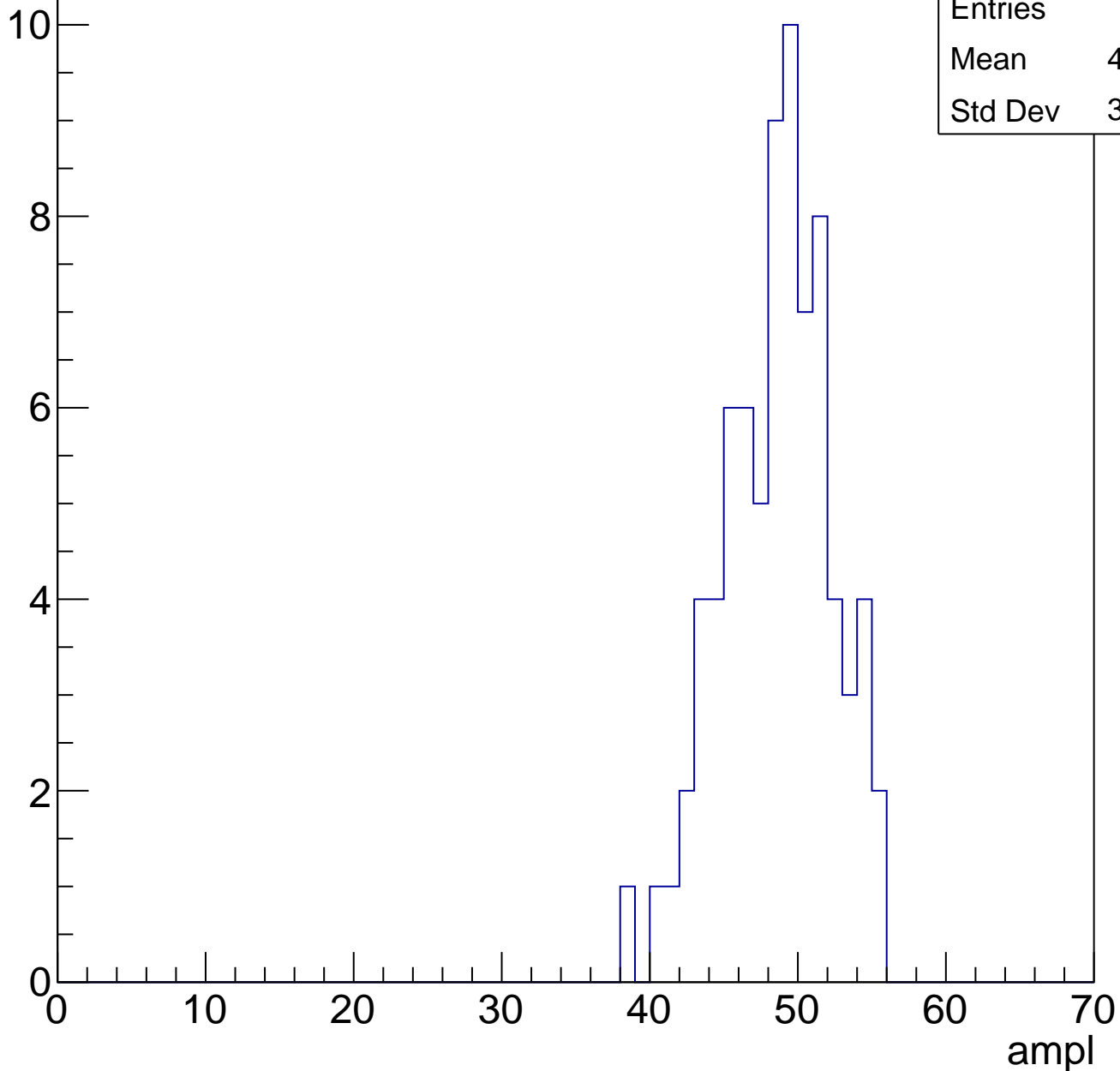


B1L103S, U23-ch73, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	77
Mean	48.12
Std Dev	3.643

Entry

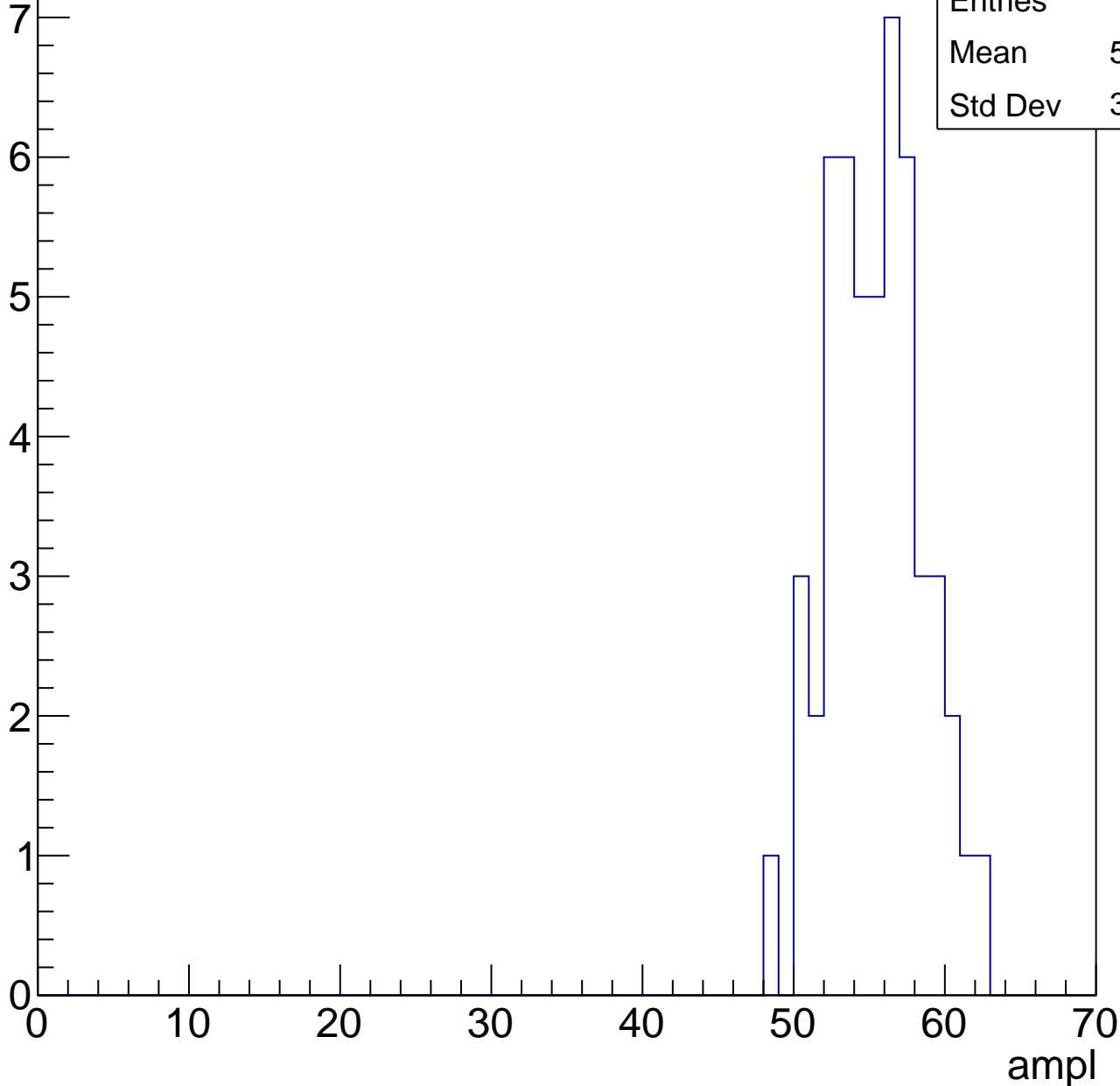


B1L103S, U23-ch73, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	51
Mean	54.96
Std Dev	3.068

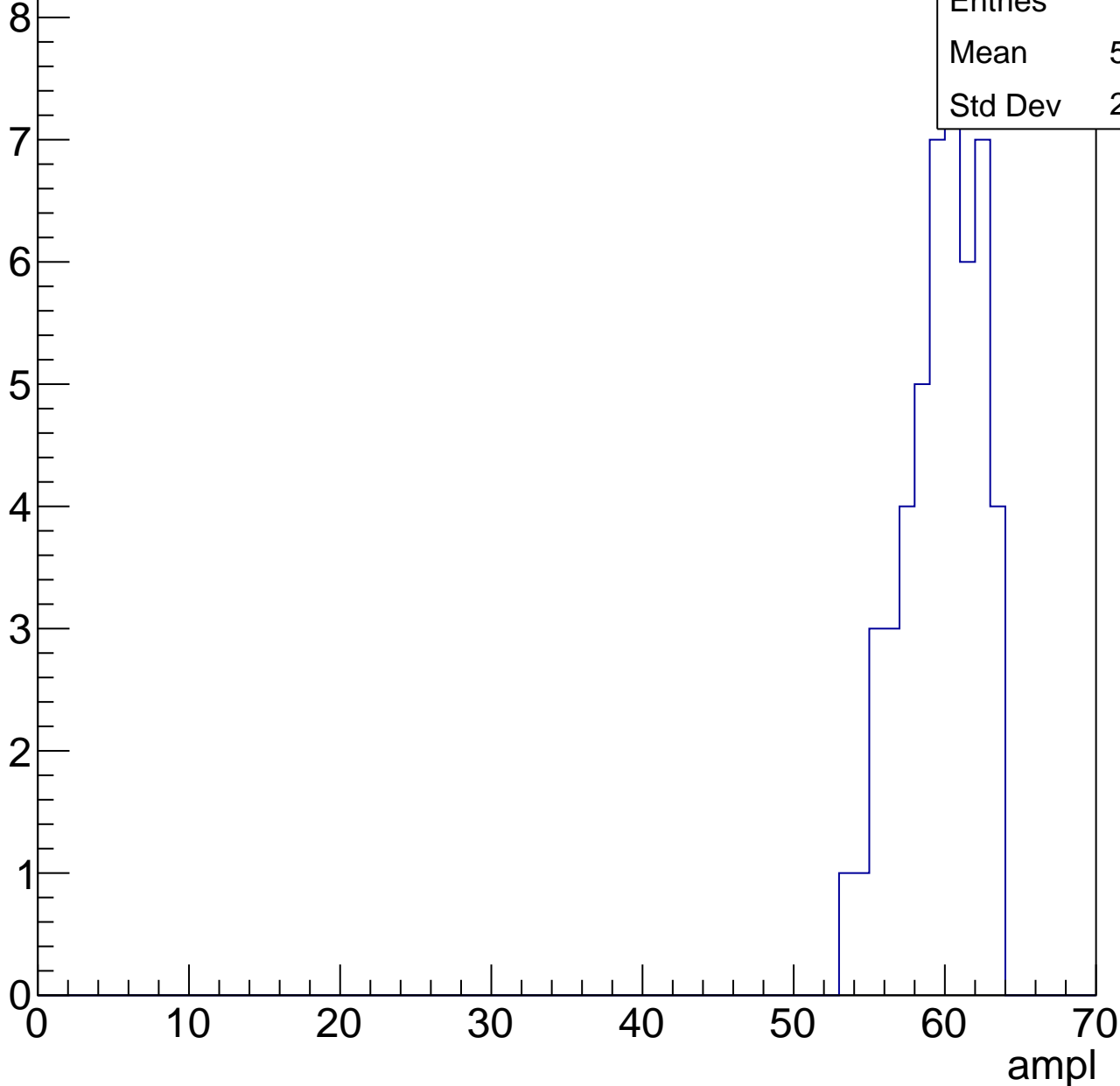


B1L103S, U23-ch73, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	49
Mean	59.24
Std Dev	2.528

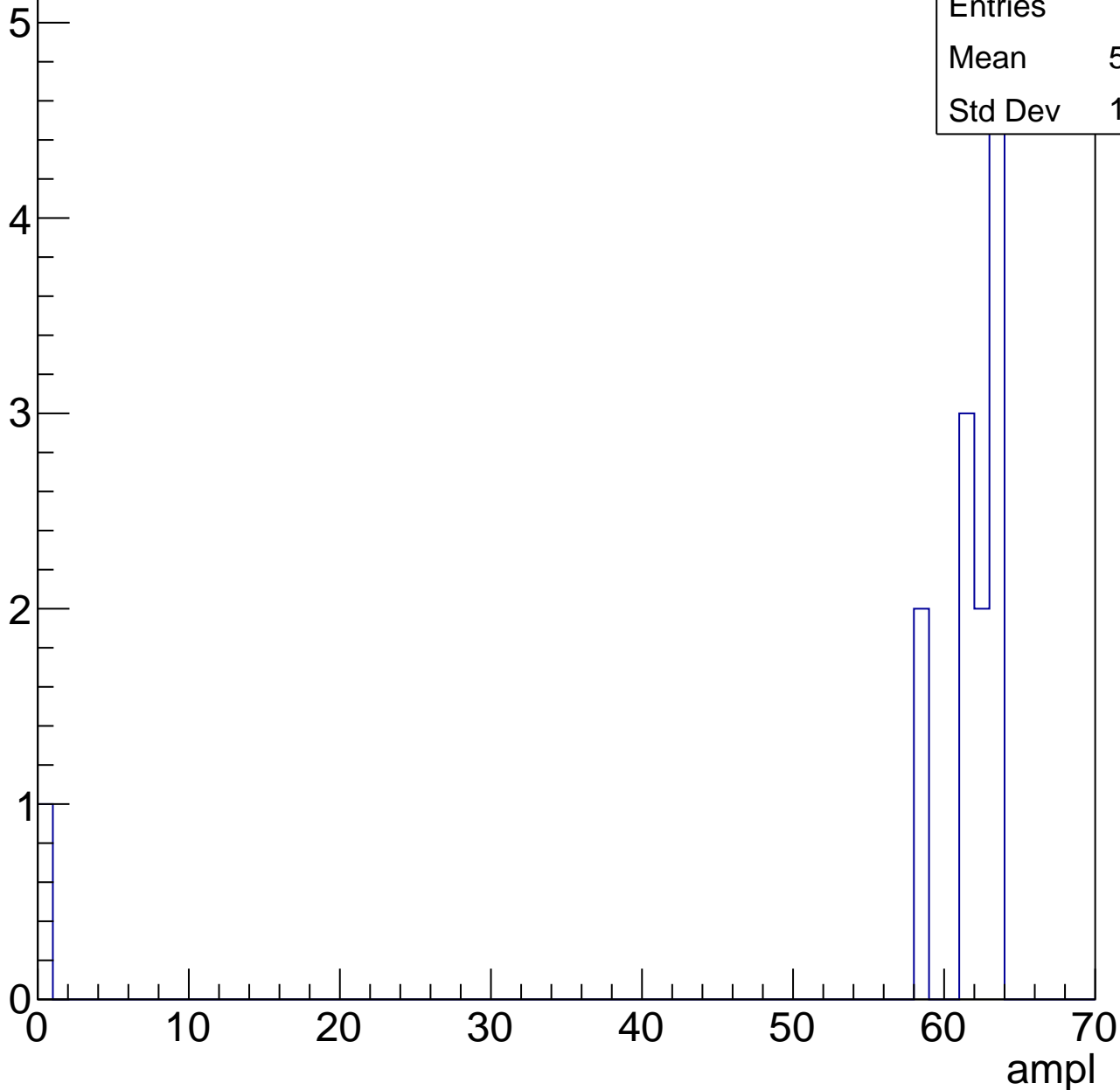


B1L103S, U23-ch73, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	13
Mean	56.77
Std Dev	16.47



B1L103S, U23-ch73, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.15
Std Dev	13.73

Entry

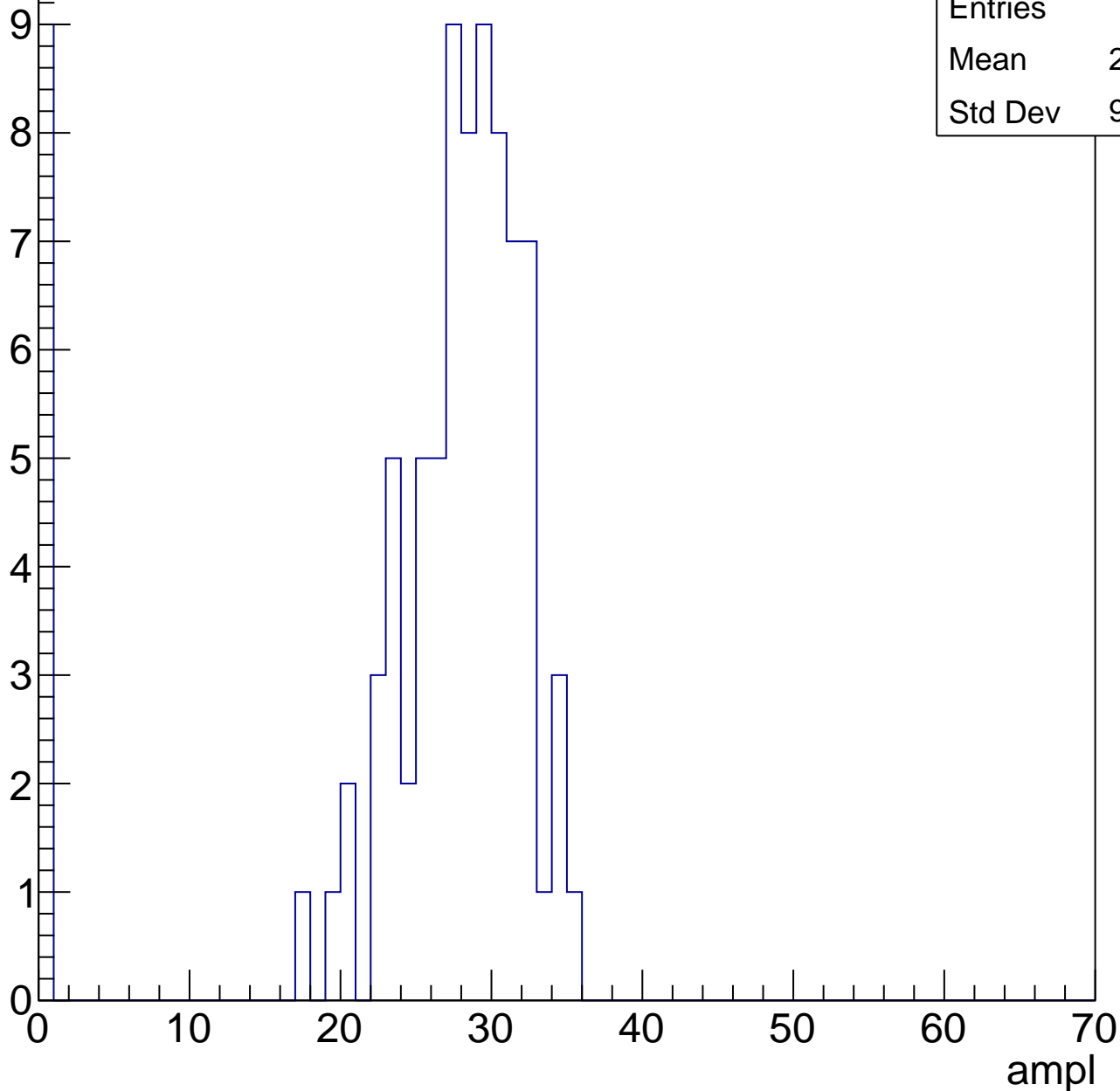


B1L103S, U23-ch74, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	86
Mean	24.87
Std Dev	9.202

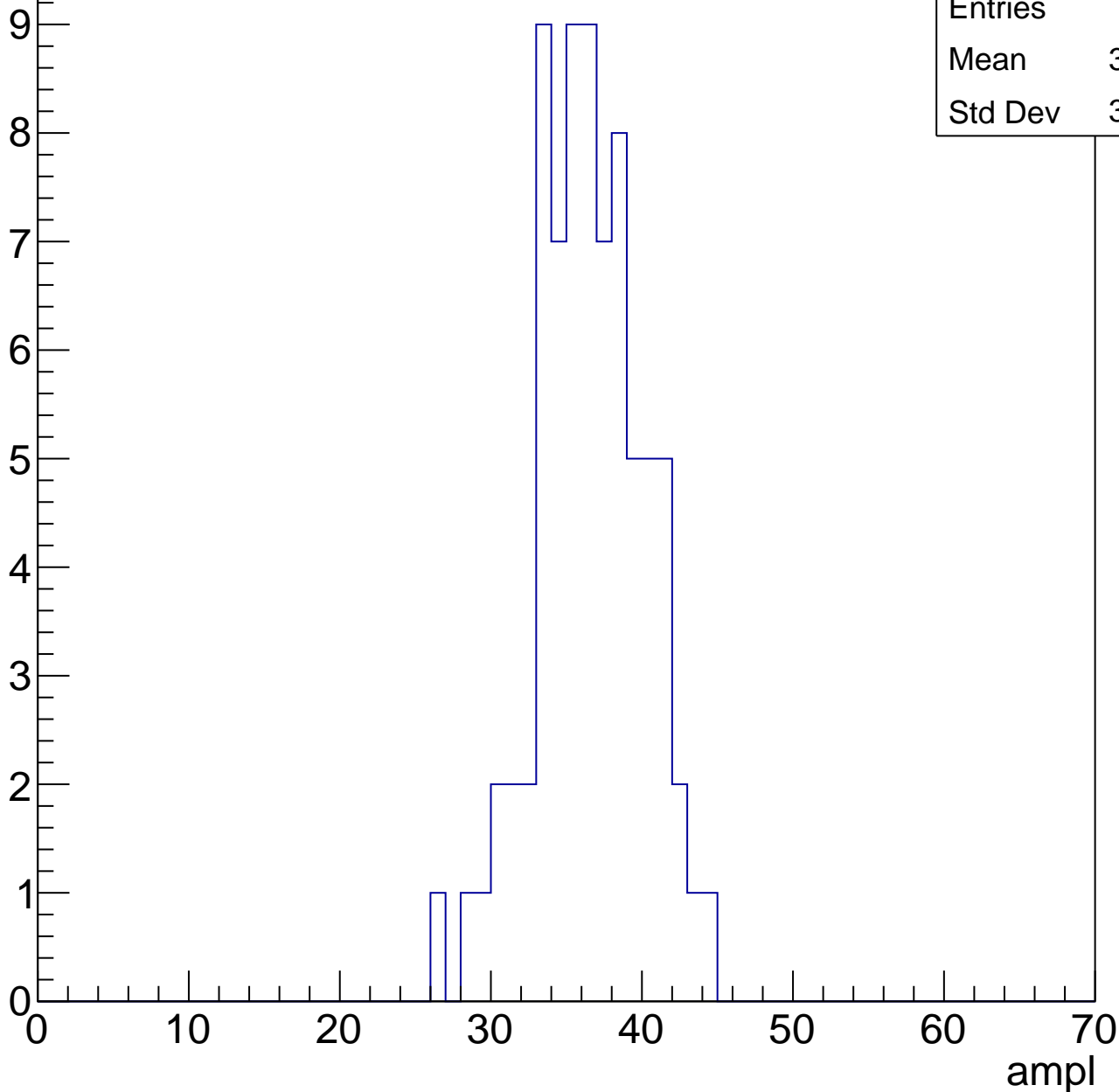


B1L103S, U23-ch74, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	77
Mean	36.06
Std Dev	3.529

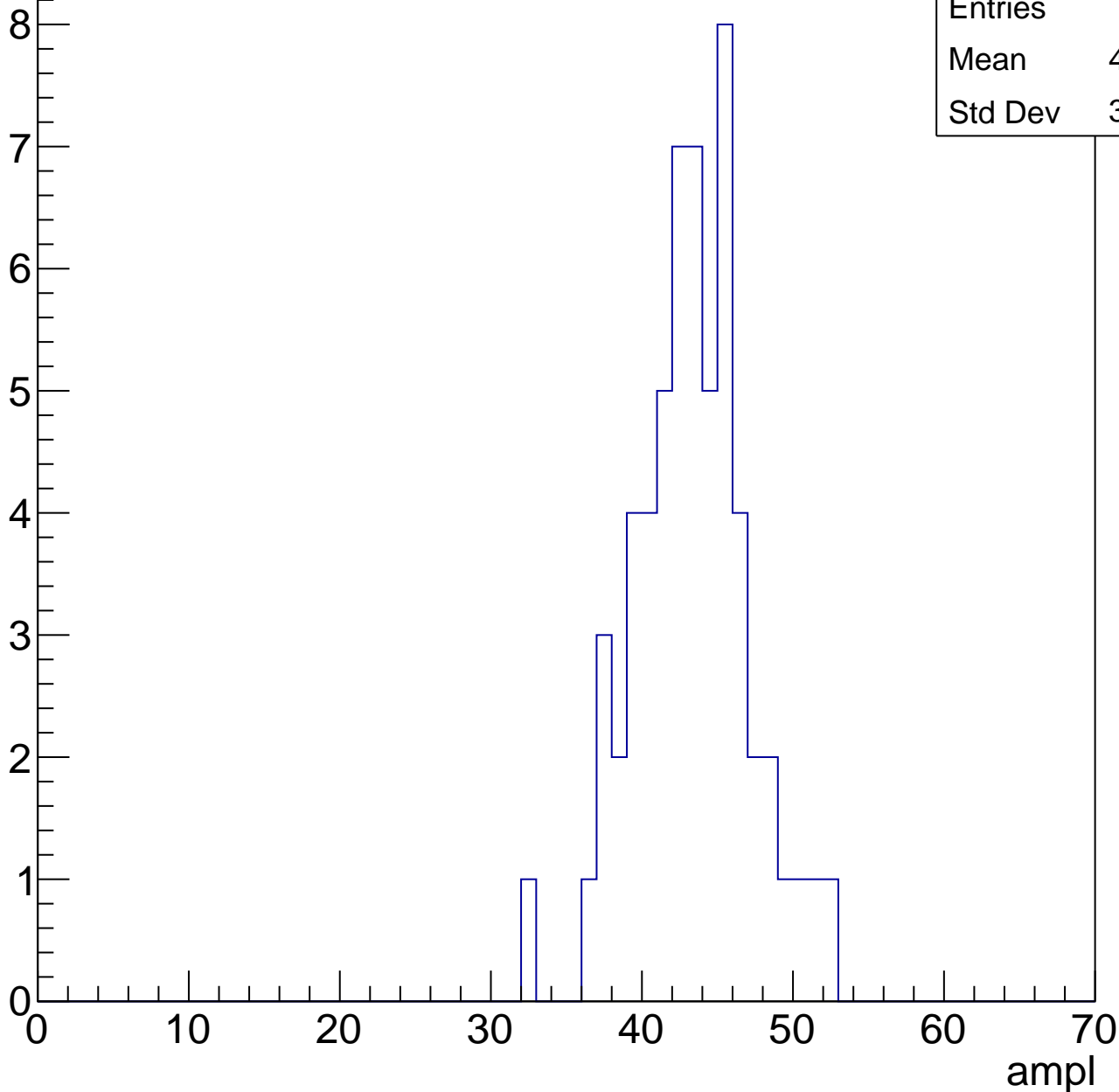


B1L103S, U23-ch74, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	42.83
Std Dev	3.769

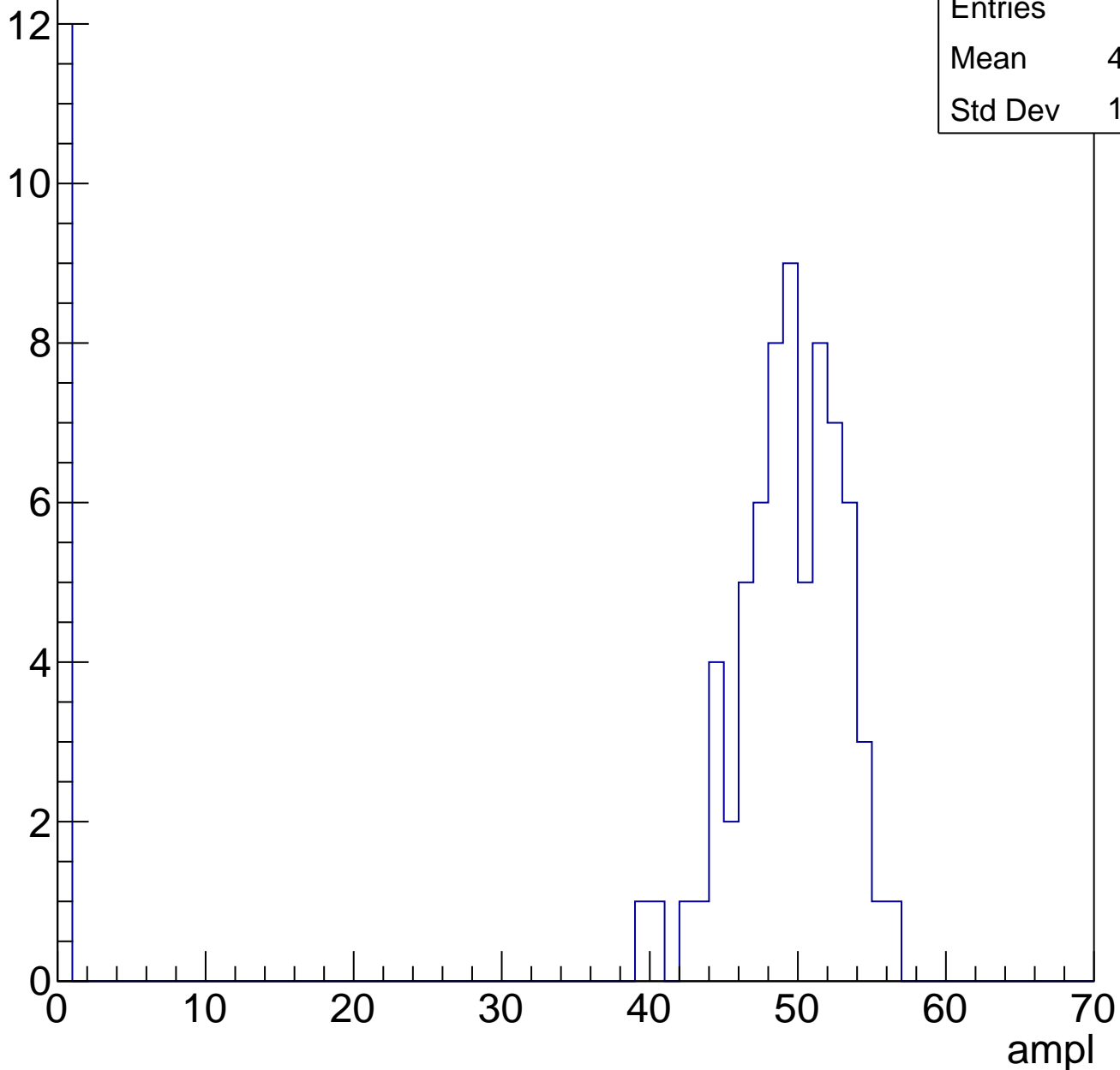


B1L103S, U23-ch74, adc3

calib_packv5_041523_1651.root, FC#0, port C2

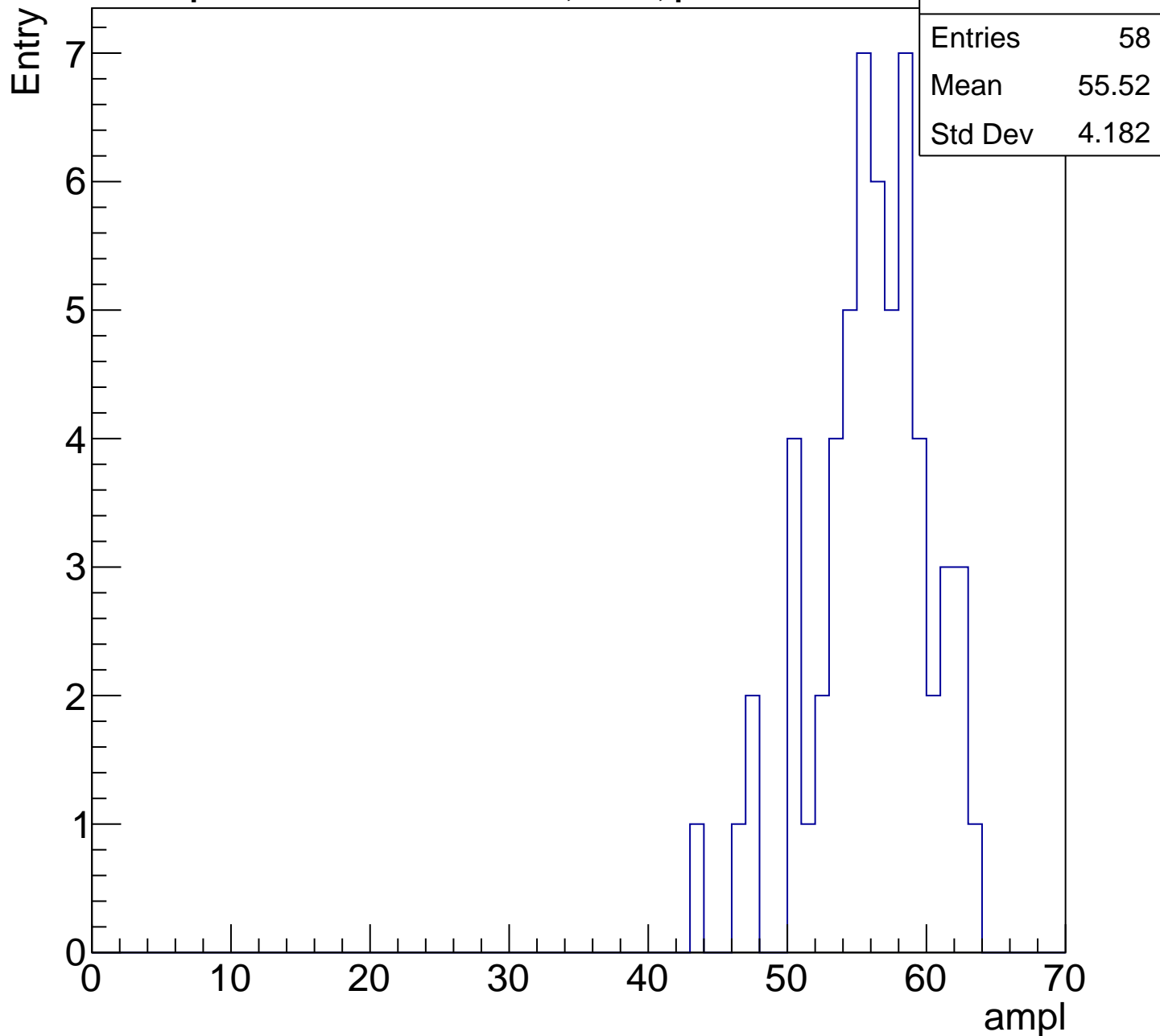
Entries	81
Mean	41.73
Std Dev	17.69

Entry



B1L103S, U23-ch74, adc4

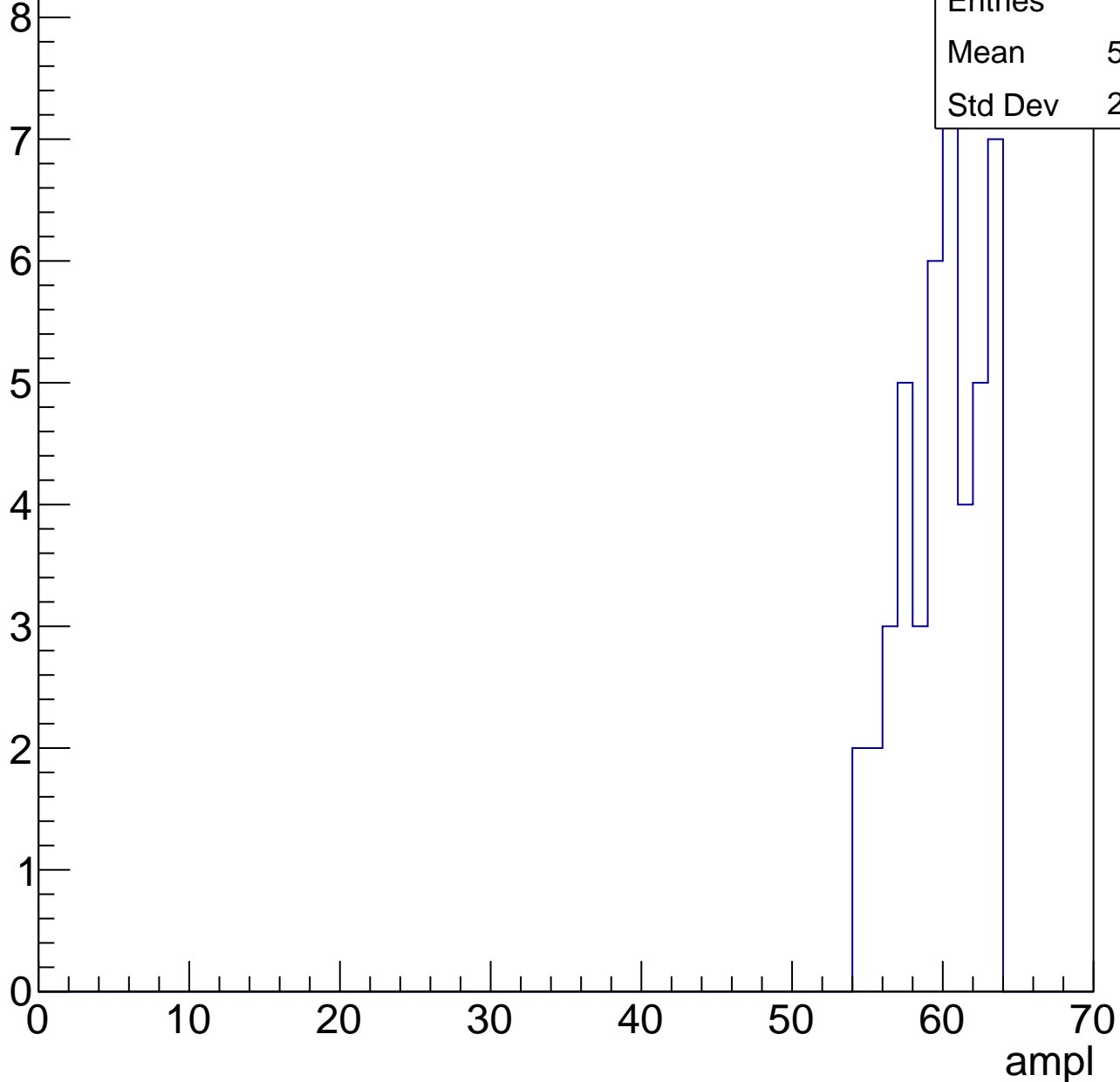
calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U23-ch74, adc5

calib_packv5_041523_1651.root, FC#0, port C2

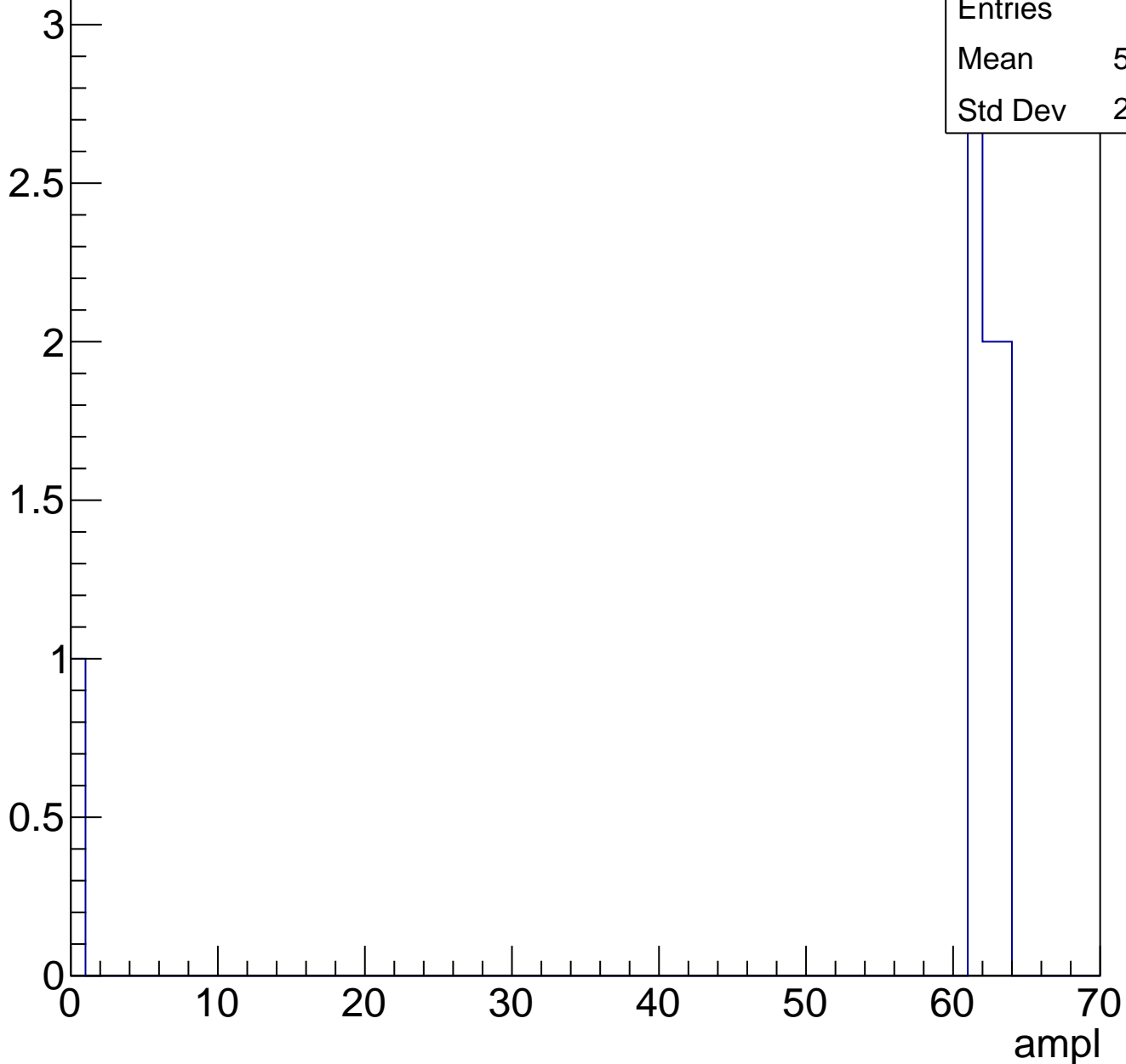
Entry



B1L103S, U23-ch74, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	8
Mean	54.12
Std Dev	20.47

B1L103S, U23-ch74, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch75, adc0

calib_packv5_041523_1651.root, FC#0, port C2

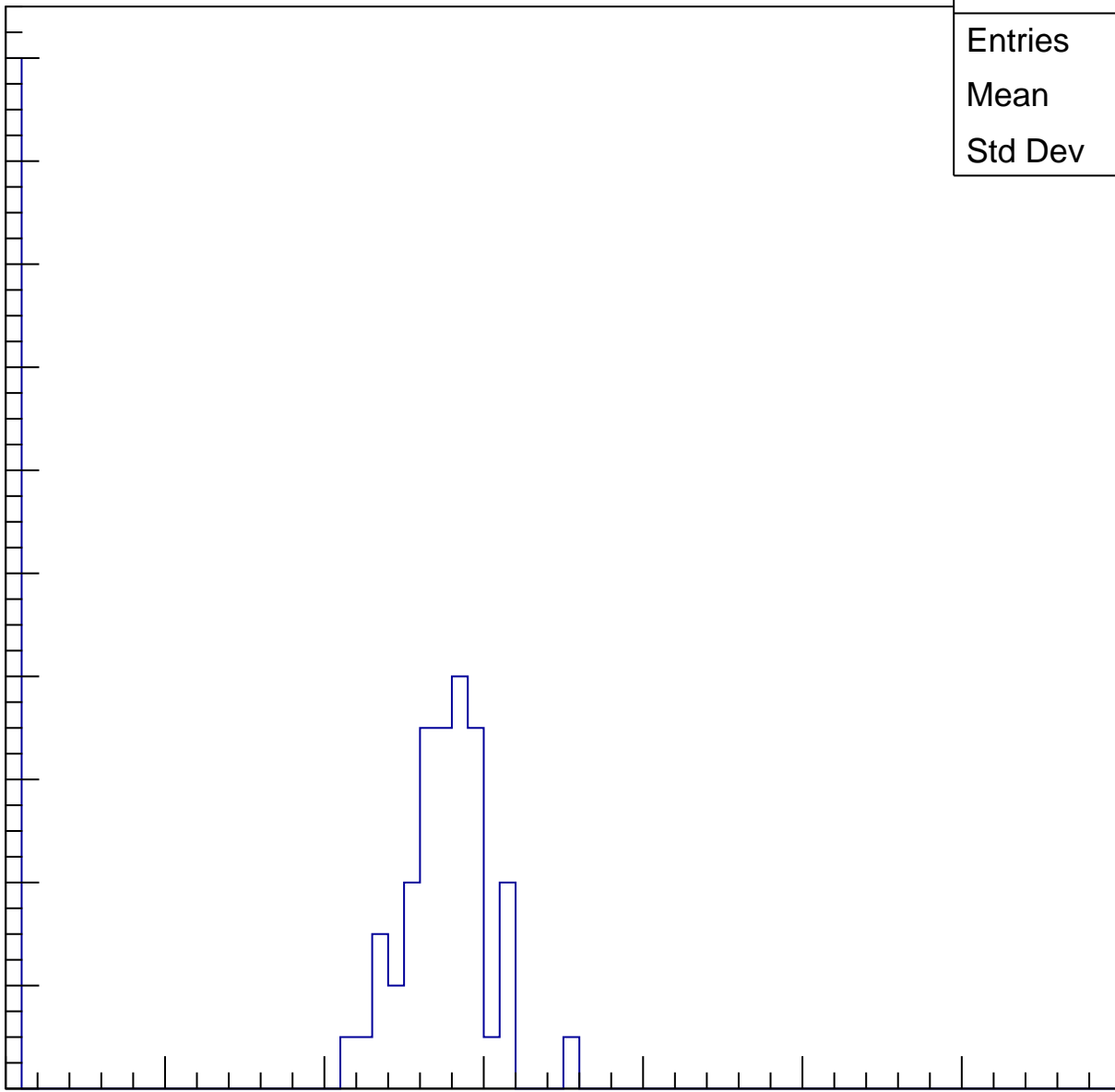
Entries	66
Mean	18.89
Std Dev	12.65

Entry

20
18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

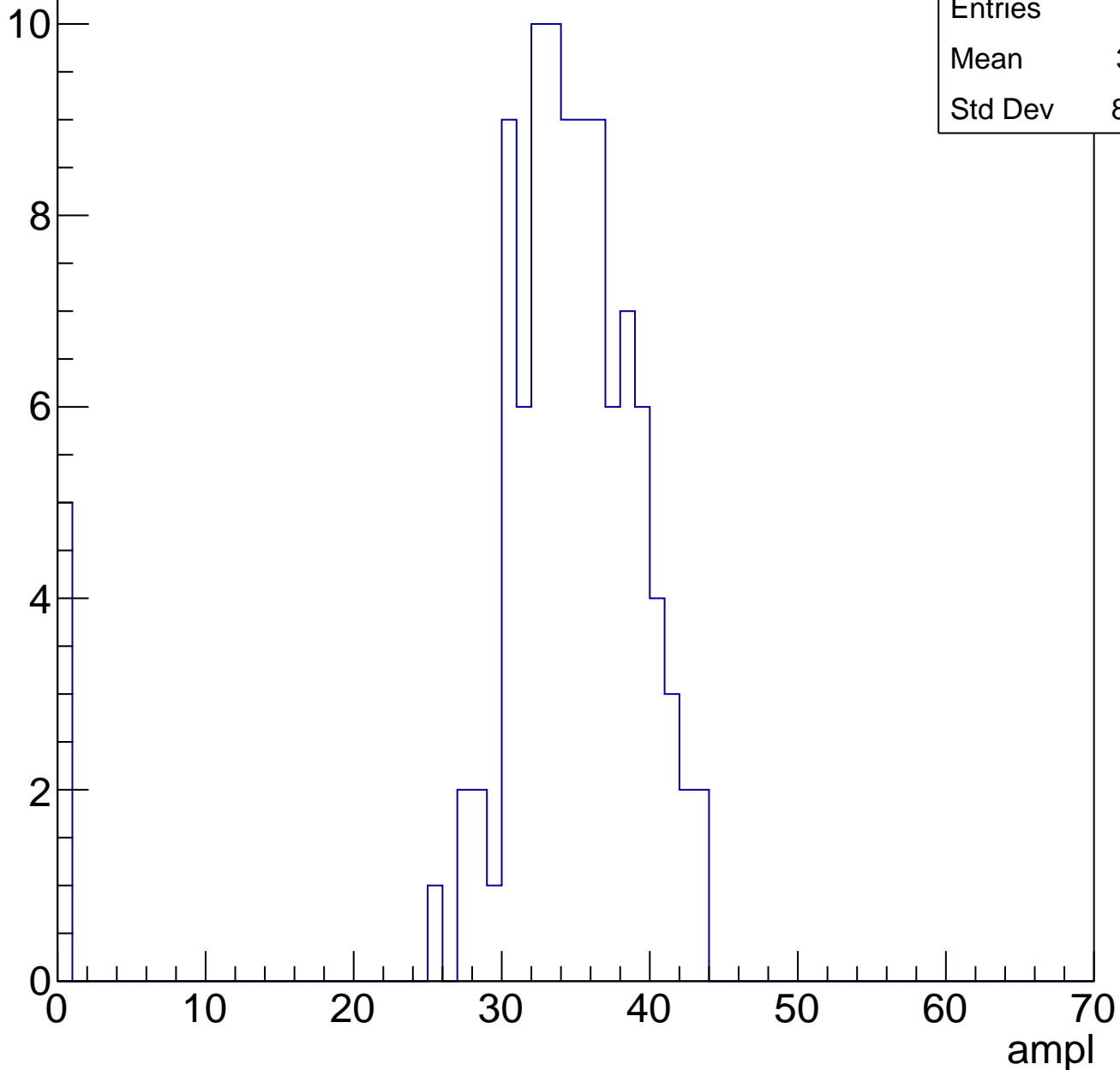


B1L103S, U23-ch75, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	103
Mean	32.91
Std Dev	8.317

Entry



B1L103S, U23-ch75, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	82
Mean	37.09
Std Dev	14.97

Entry

10

8

6

4

2

0

0

10

20

30

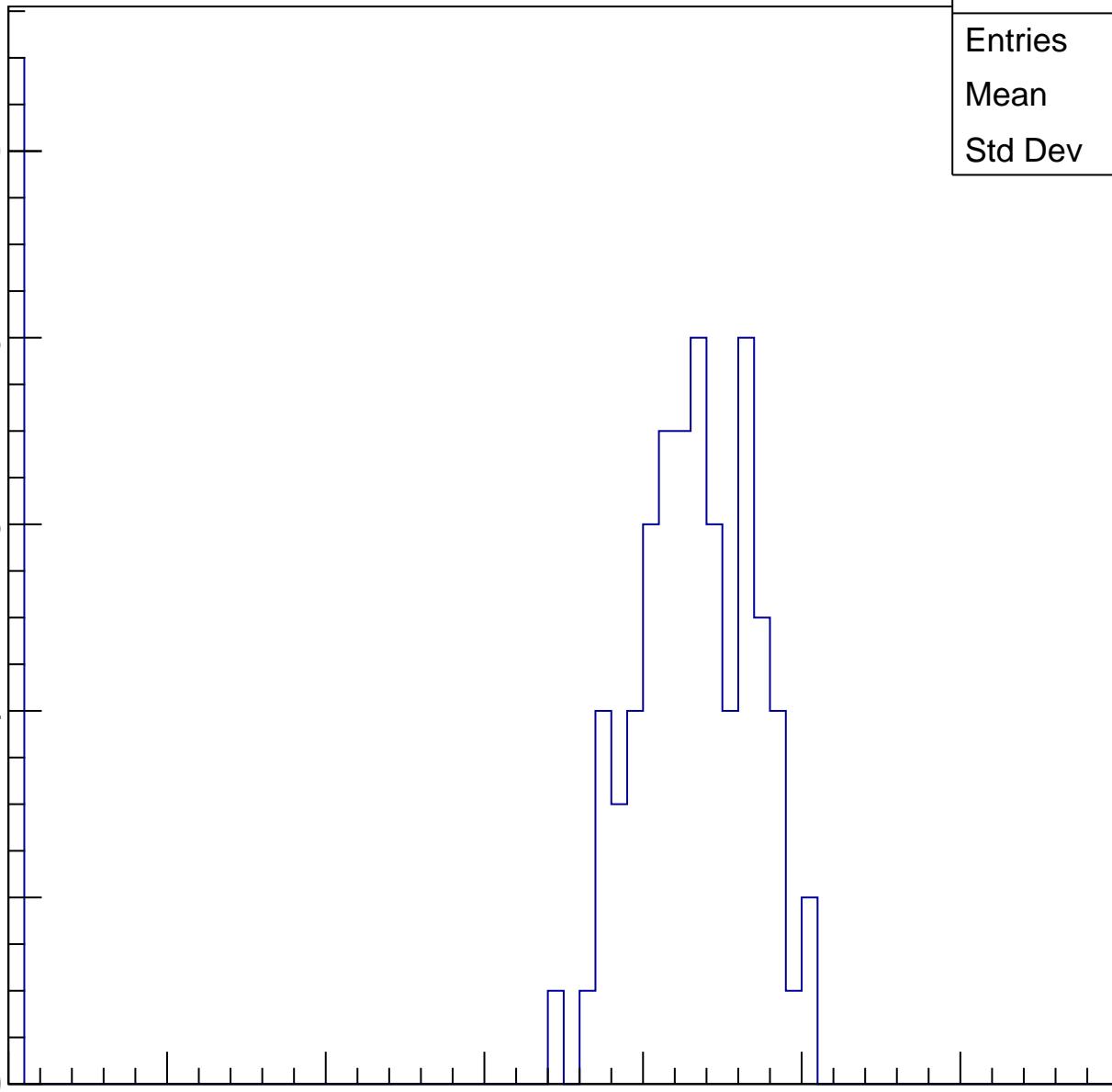
40

50

60

70

ampl

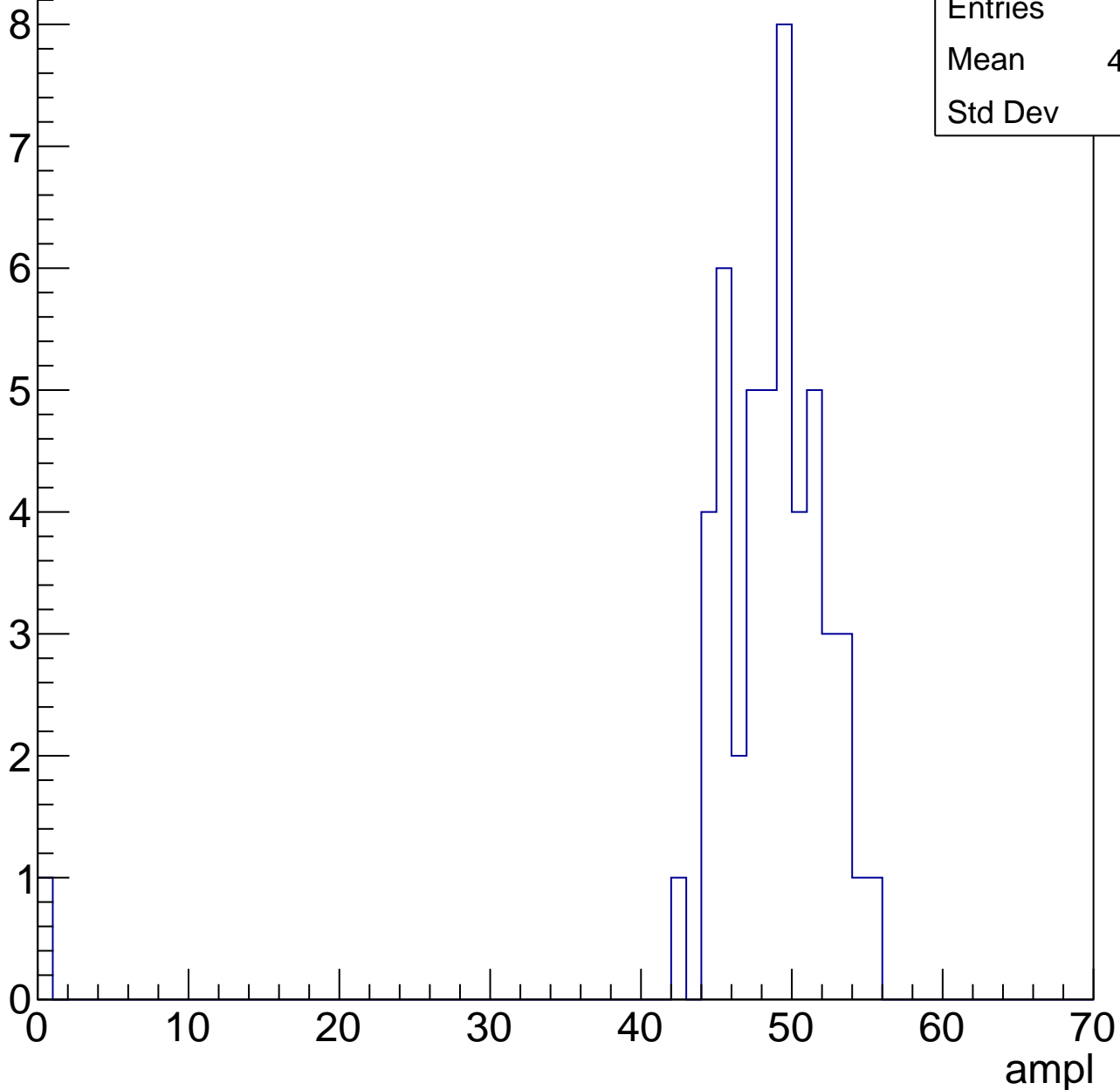


B1L103S, U23-ch75, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	49
Mean	47.47
Std Dev	7.47

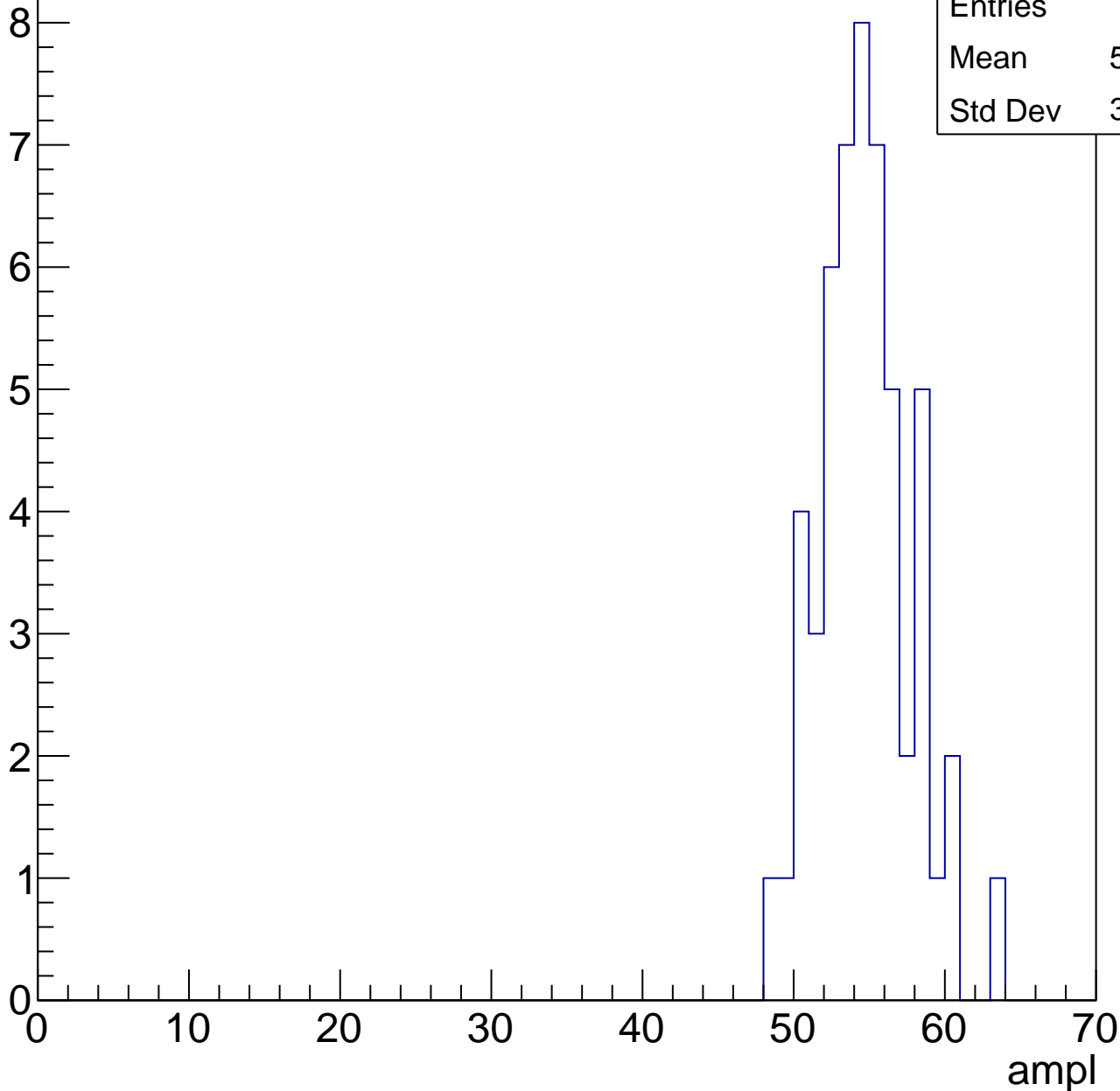


B1L103S, U23-ch75, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

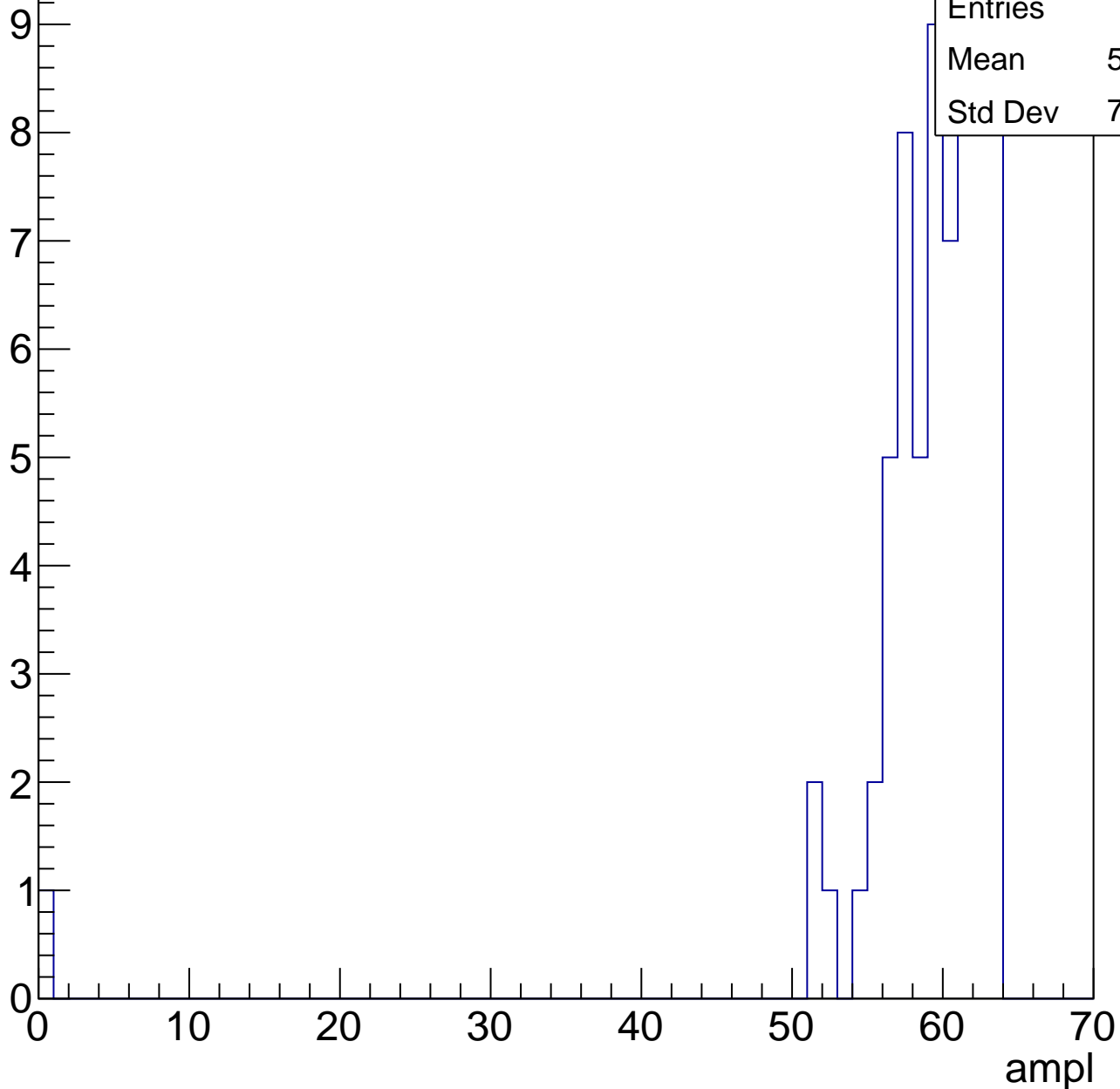
Entries	53
Mean	54.26
Std Dev	3.017



B1L103S, U23-ch75, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch75, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch75, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch76, adc0

calib_packv5_041523_1651.root, FC#0, port C2

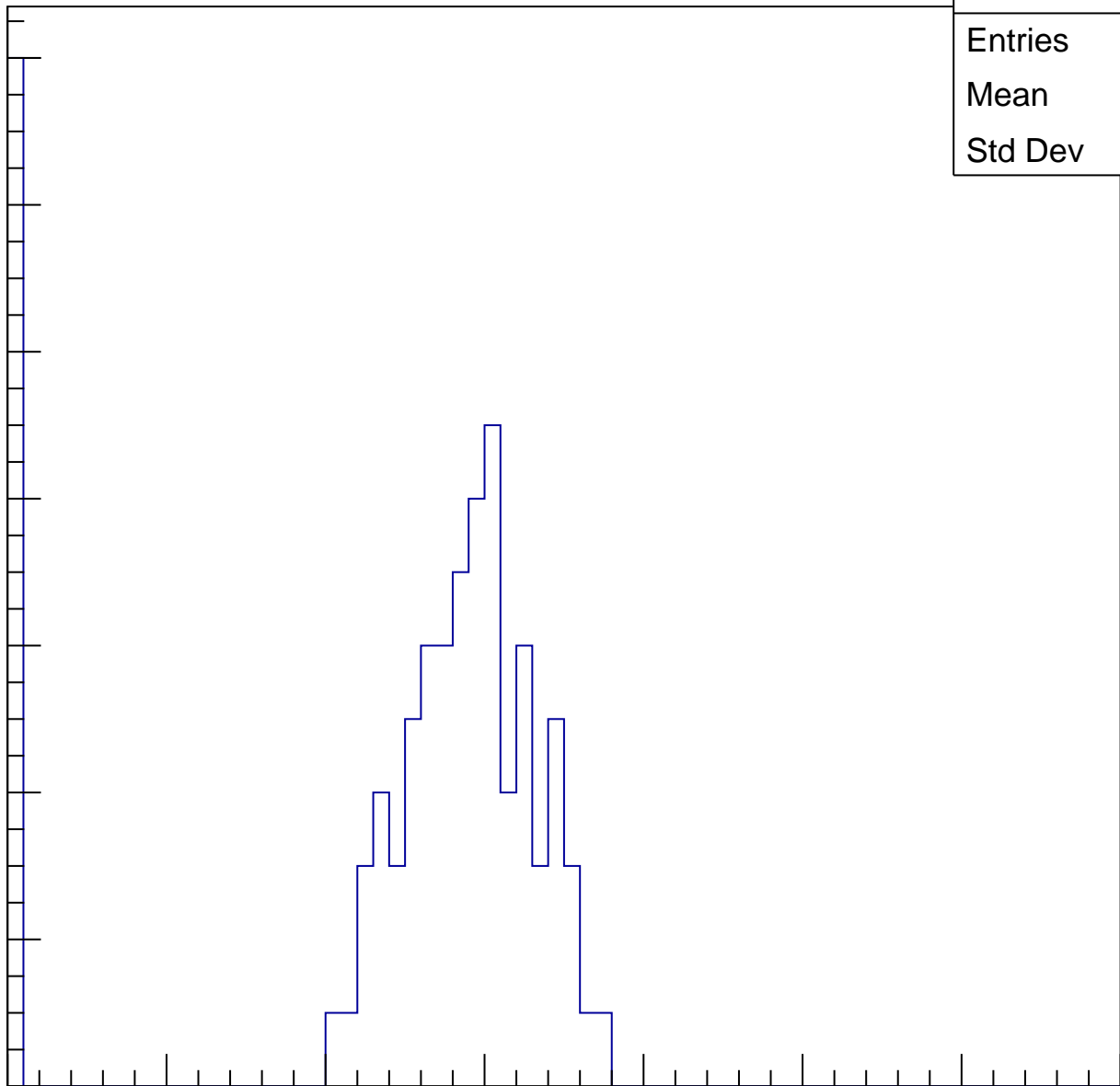
Entries	90
Mean	24.17
Std Dev	10.96

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70

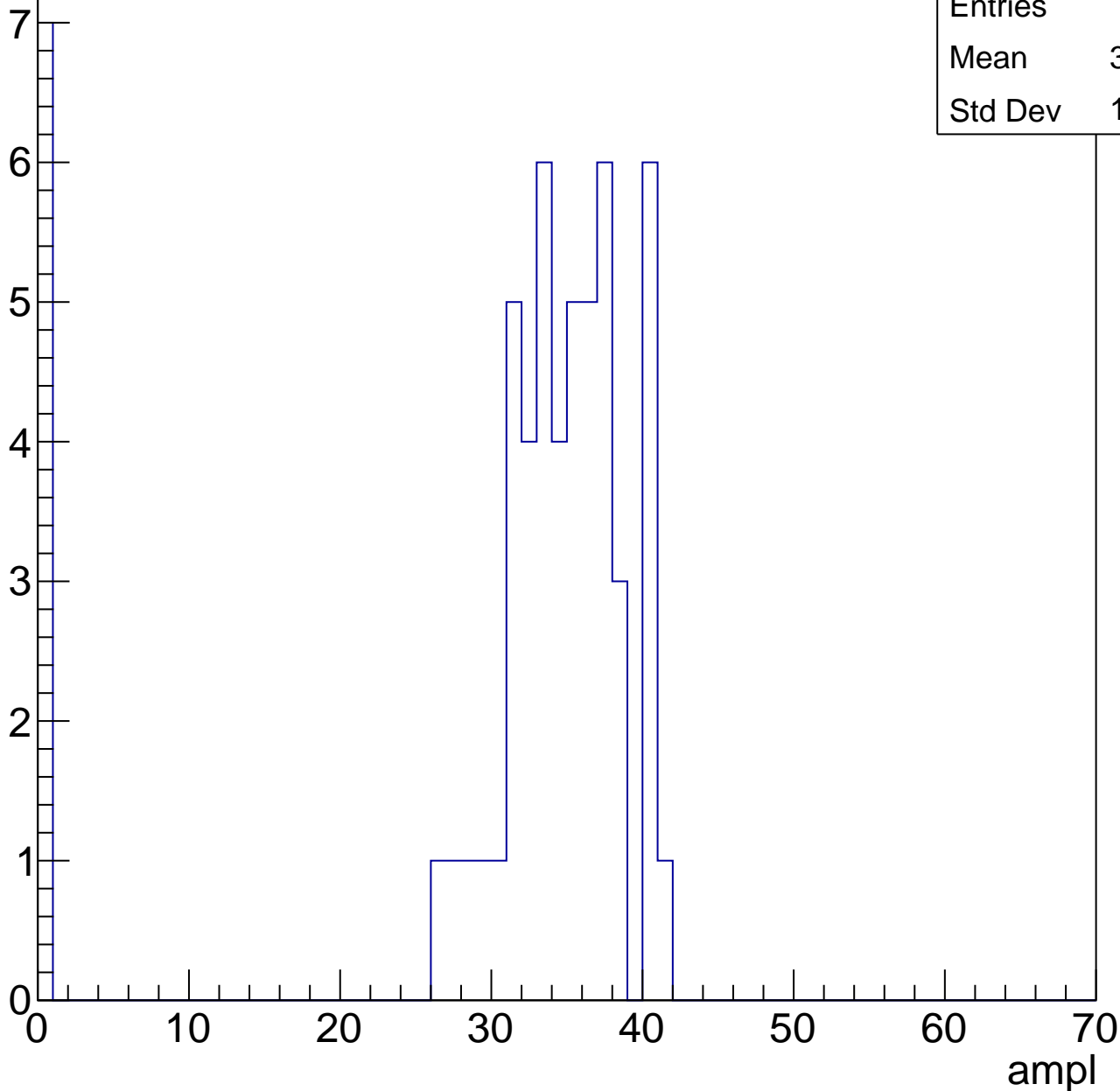


B1L103S, U23-ch76, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	57
Mean	30.33
Std Dev	11.83

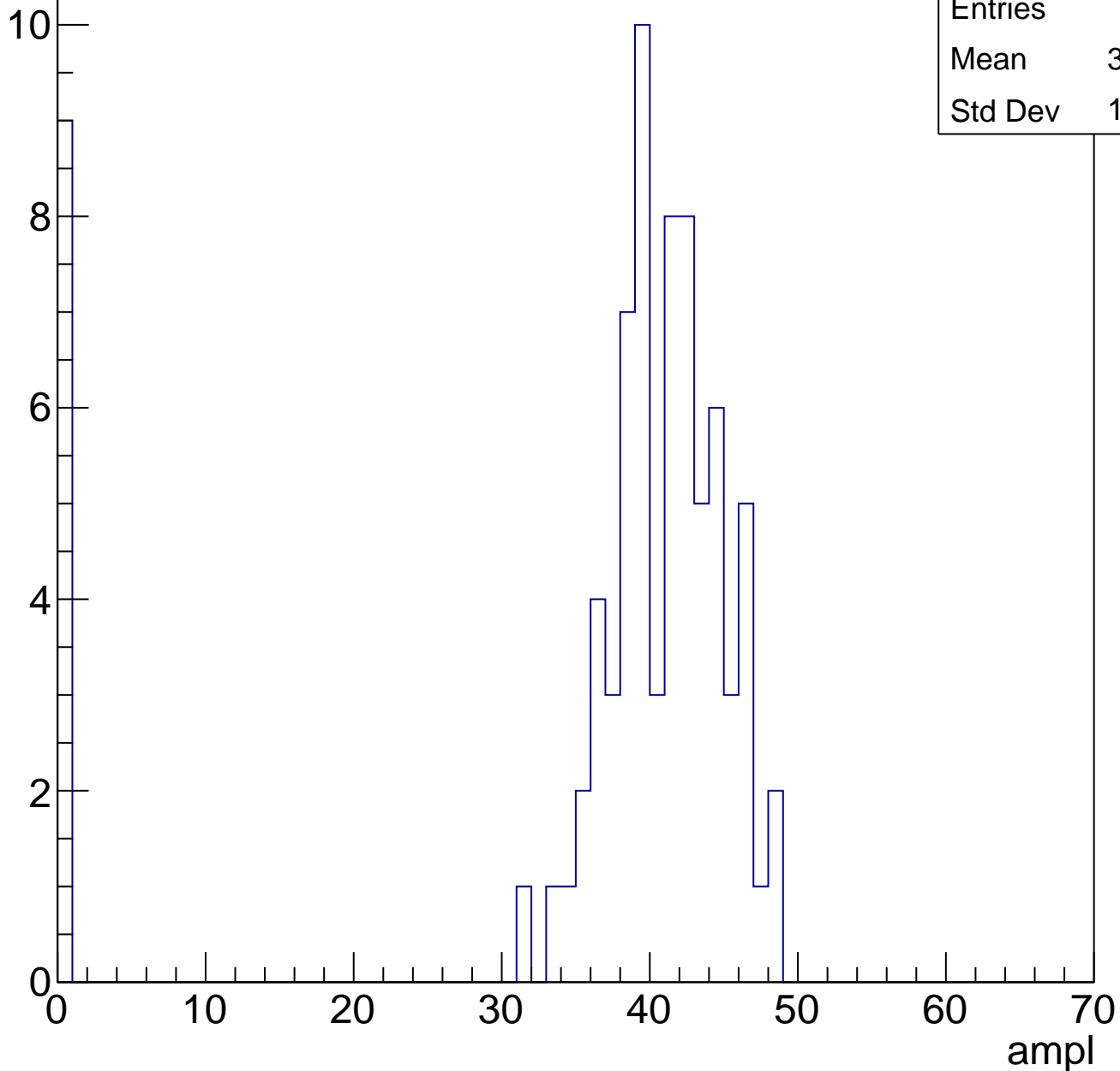


B1L103S, U23-ch76, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	79
Mean	36.08
Std Dev	13.38

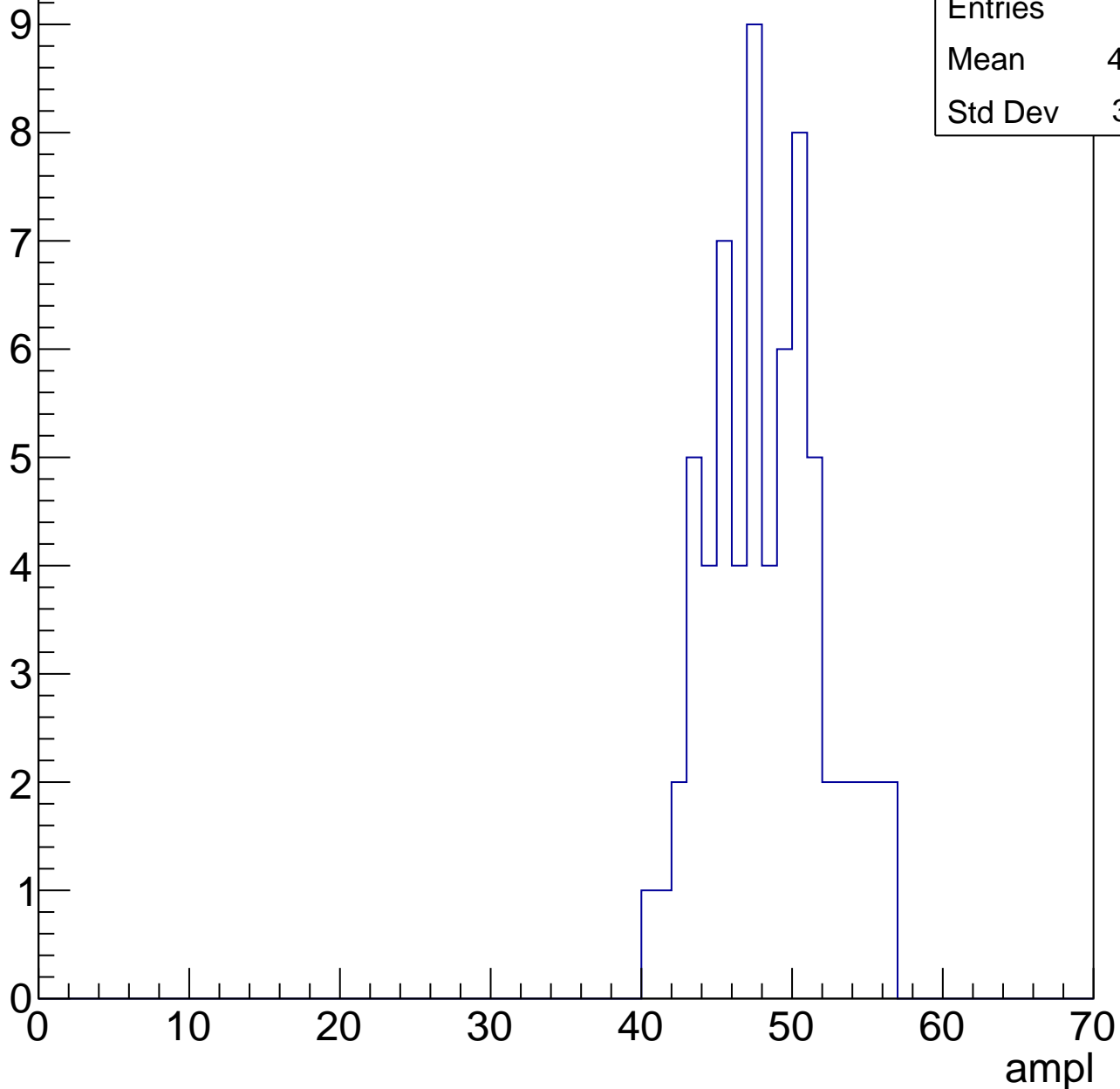
Entry



B1L103S, U23-ch76, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

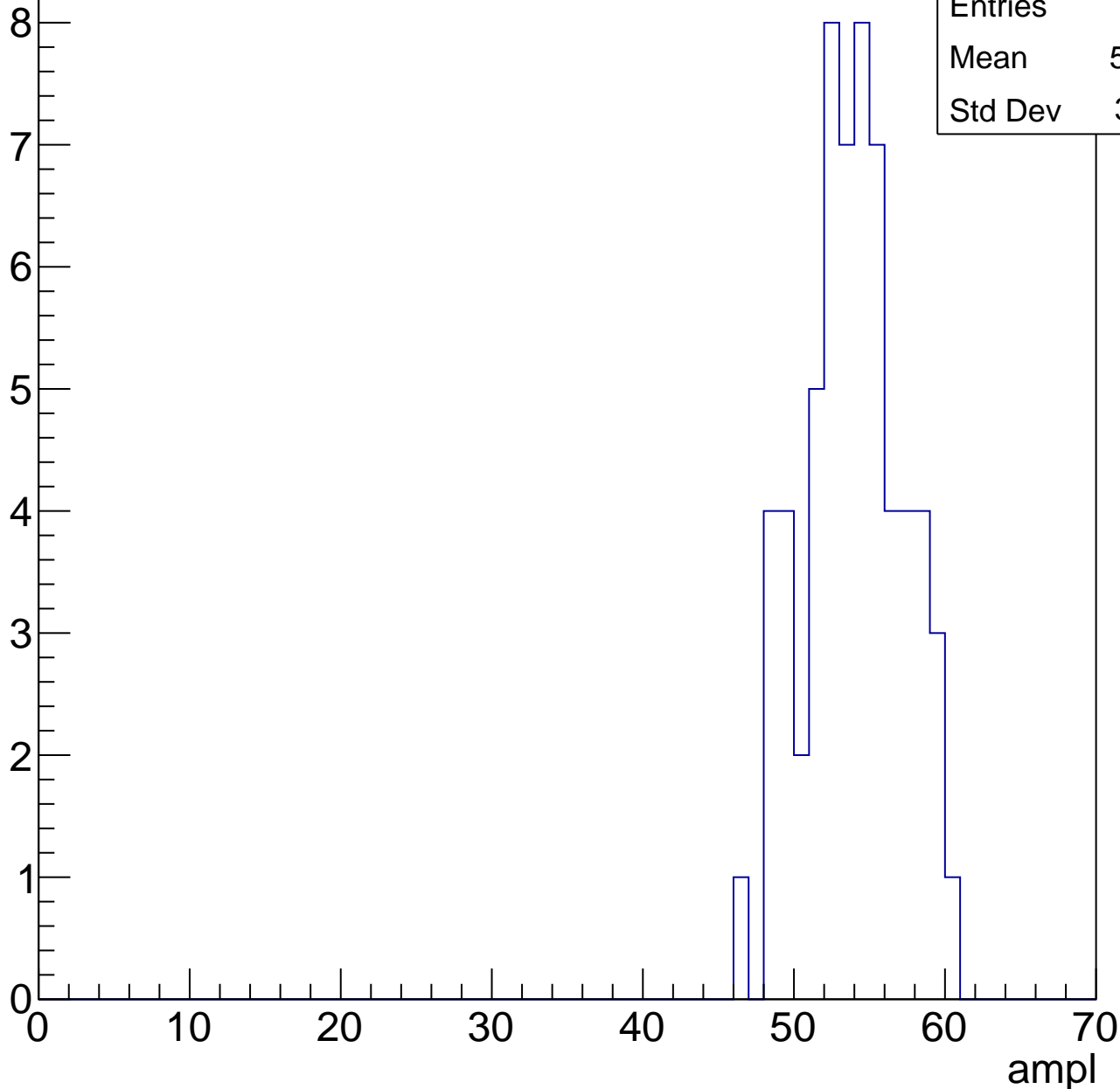


B1L103S, U23-ch76, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	53.45
Std Dev	3.211

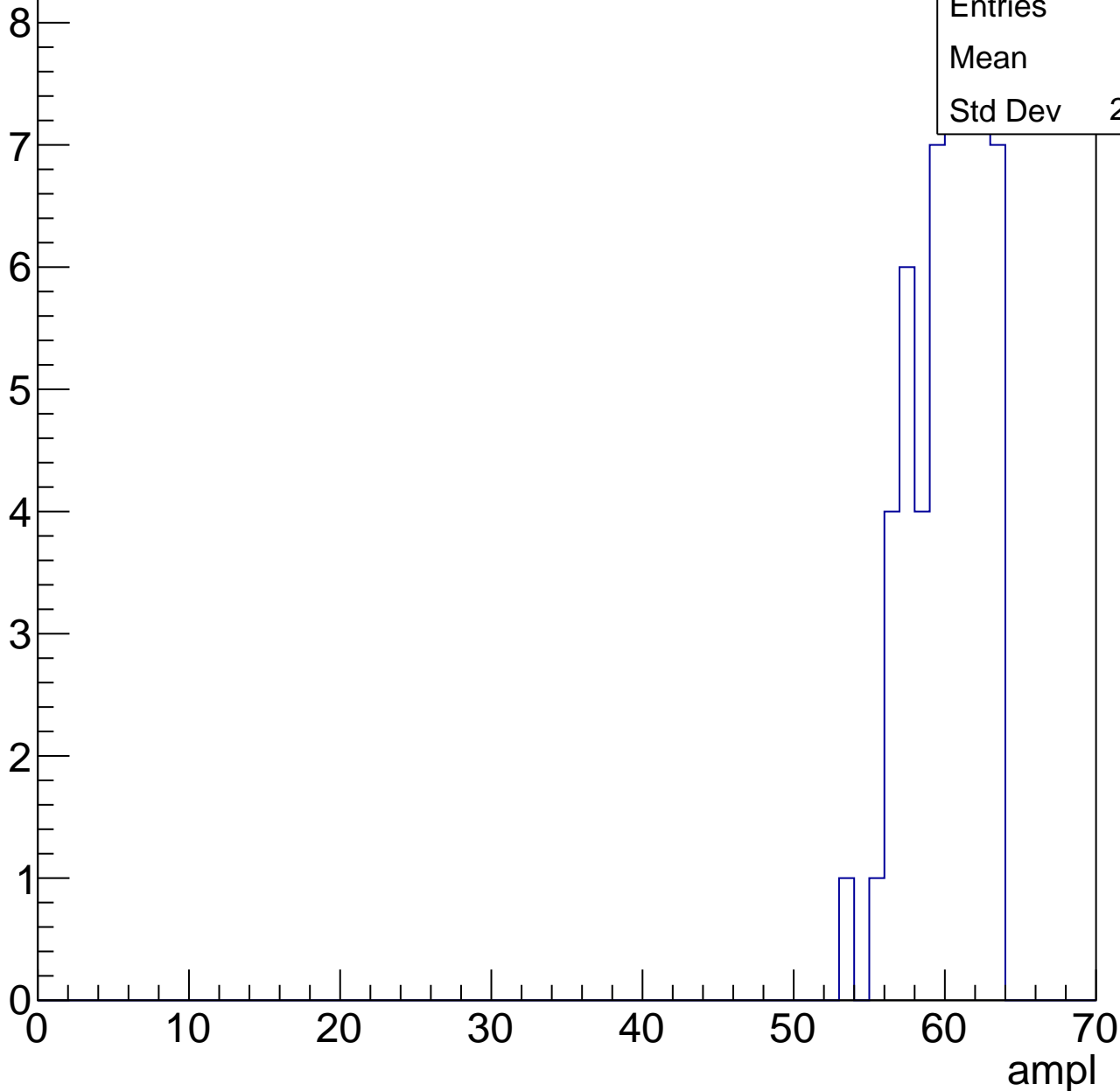


B1L103S, U23-ch76, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

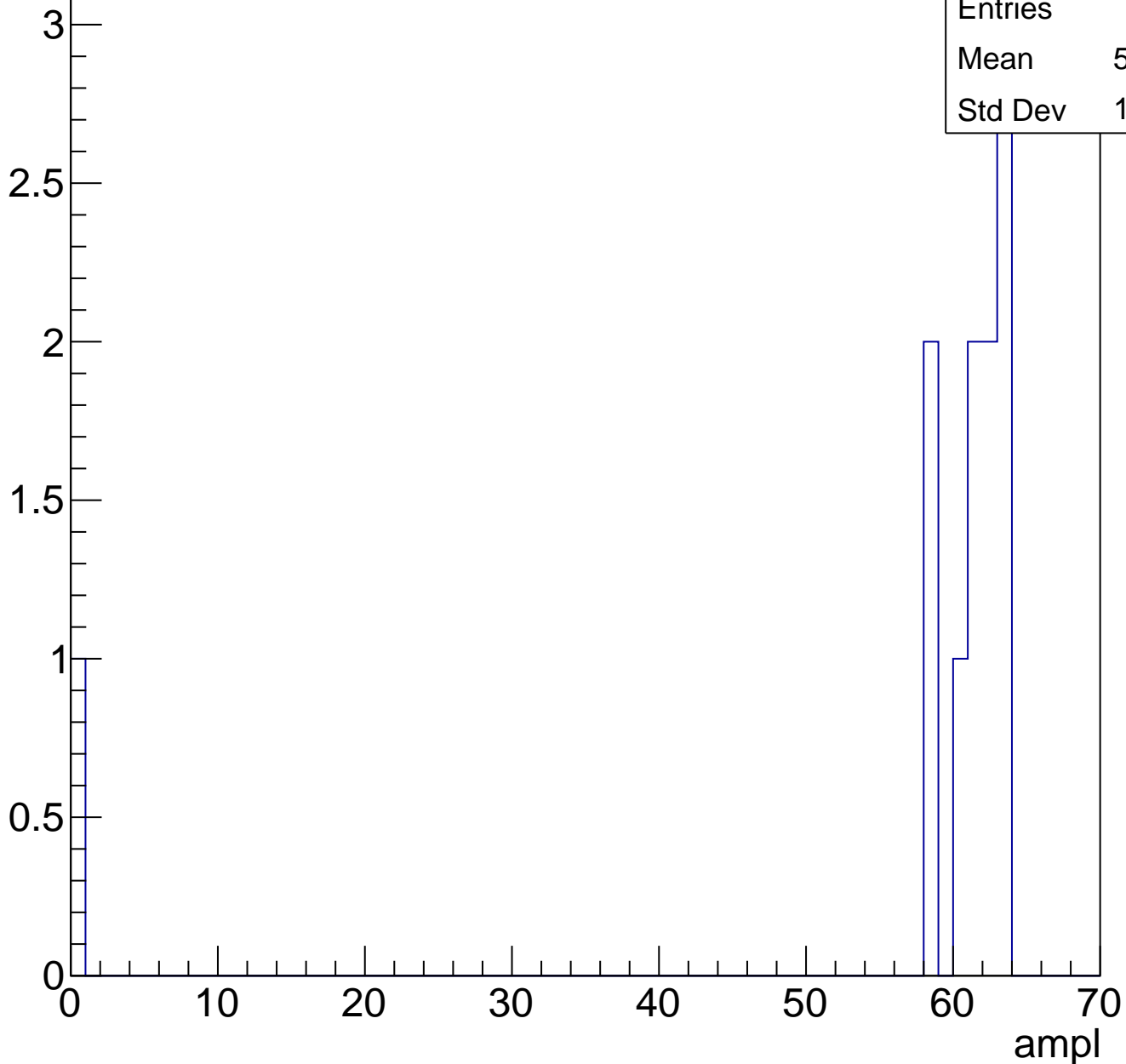
Entries	54
Mean	59.7
Std Dev	2.409



B1L103S, U23-ch76, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch76, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U23-ch77, adc0

calib_packv5_041523_1651.root, FC#0, port C2

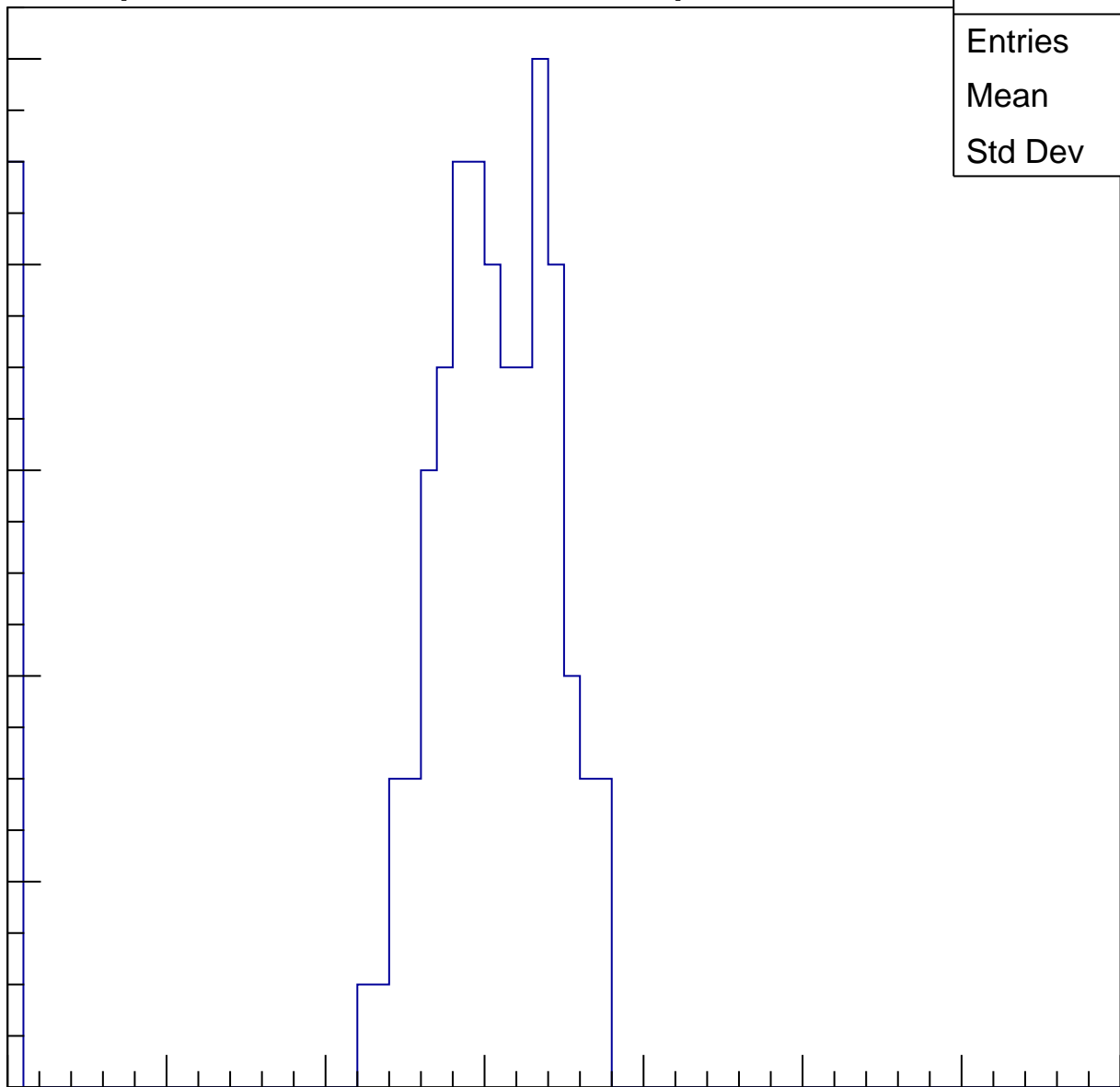
Entries	98
Mean	27.47
Std Dev	9.357

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

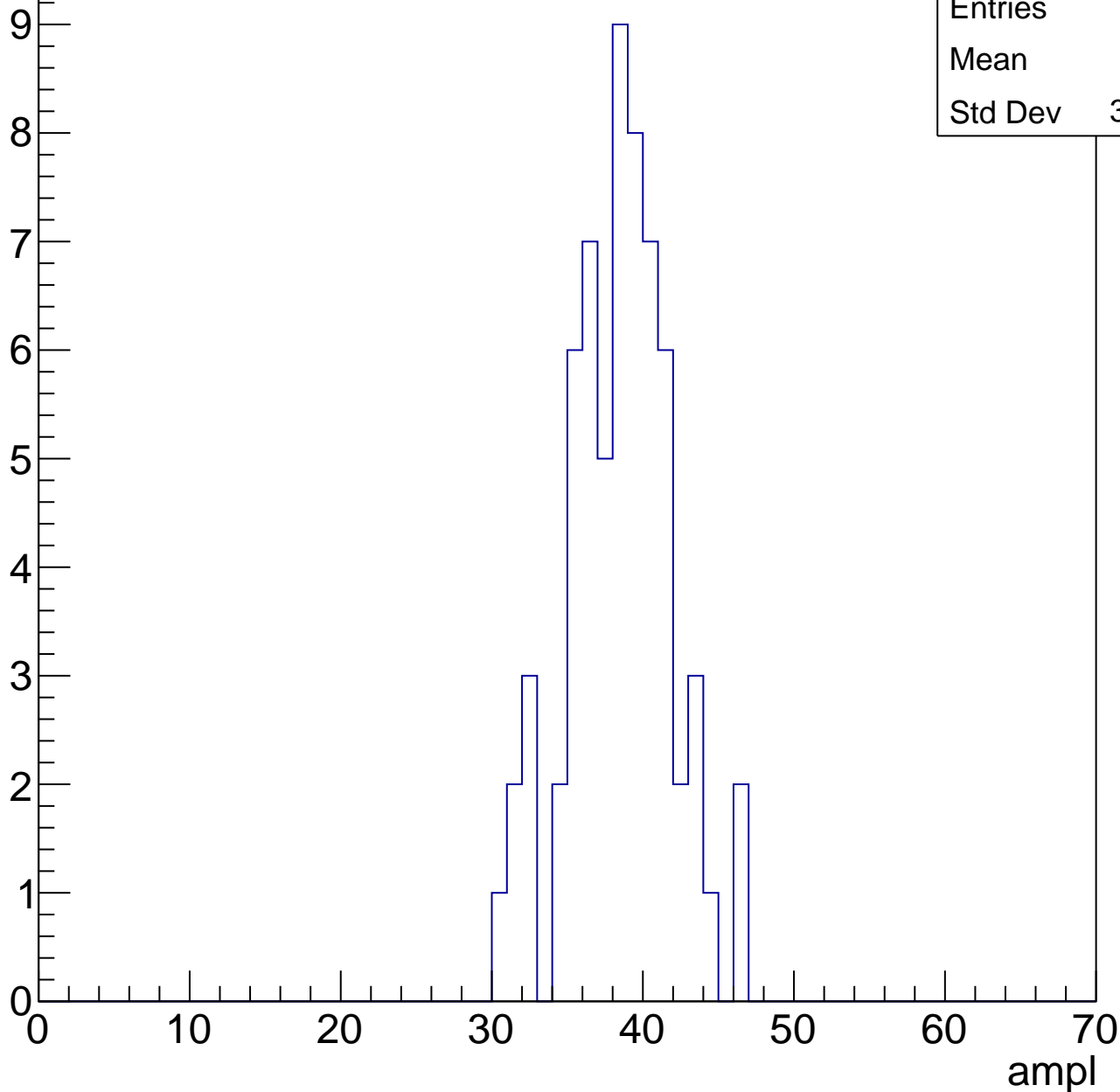


B1L103S, U23-ch77, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	38
Std Dev	3.423

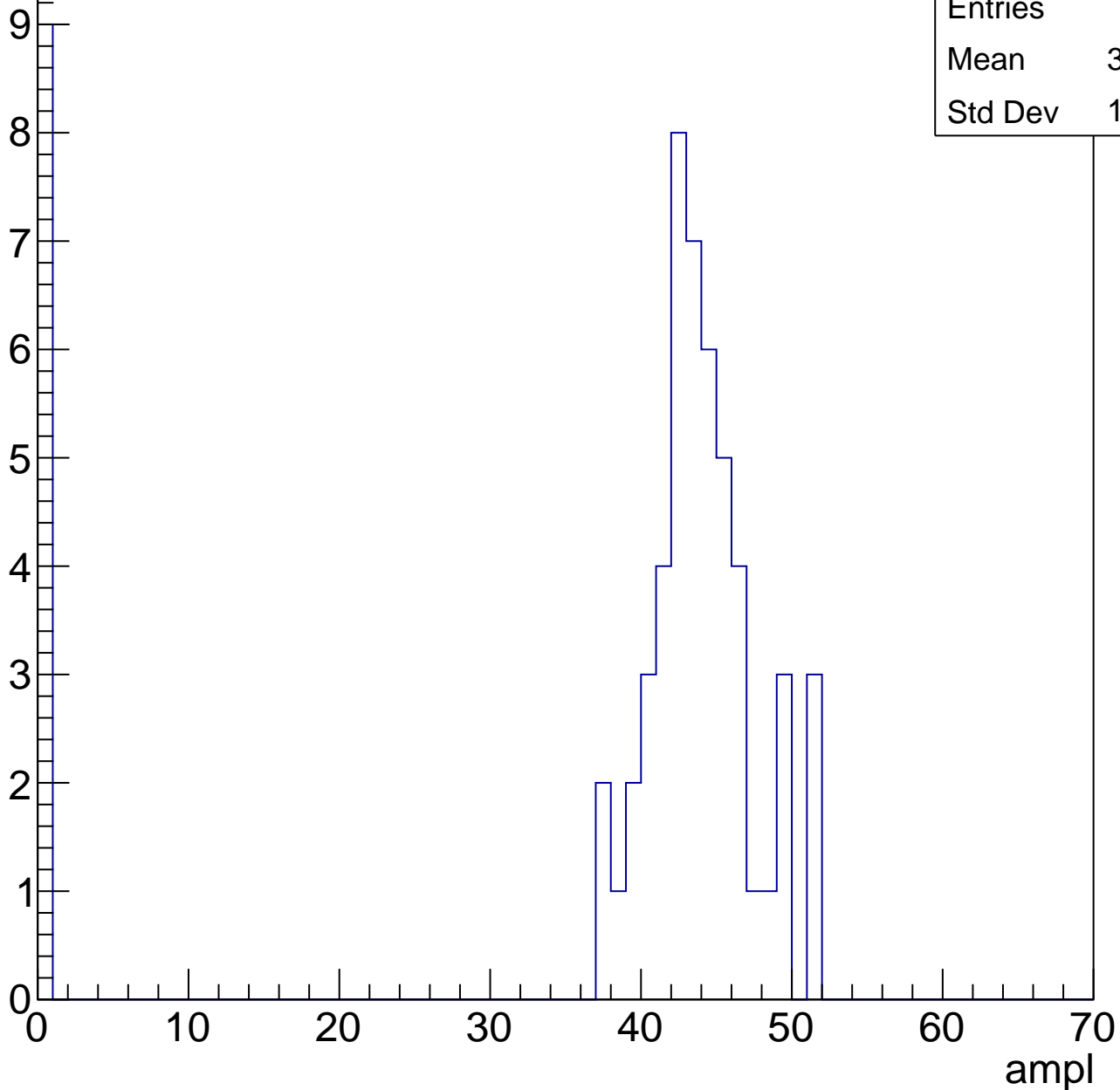


B1L103S, U23-ch77, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	36.93
Std Dev	15.97

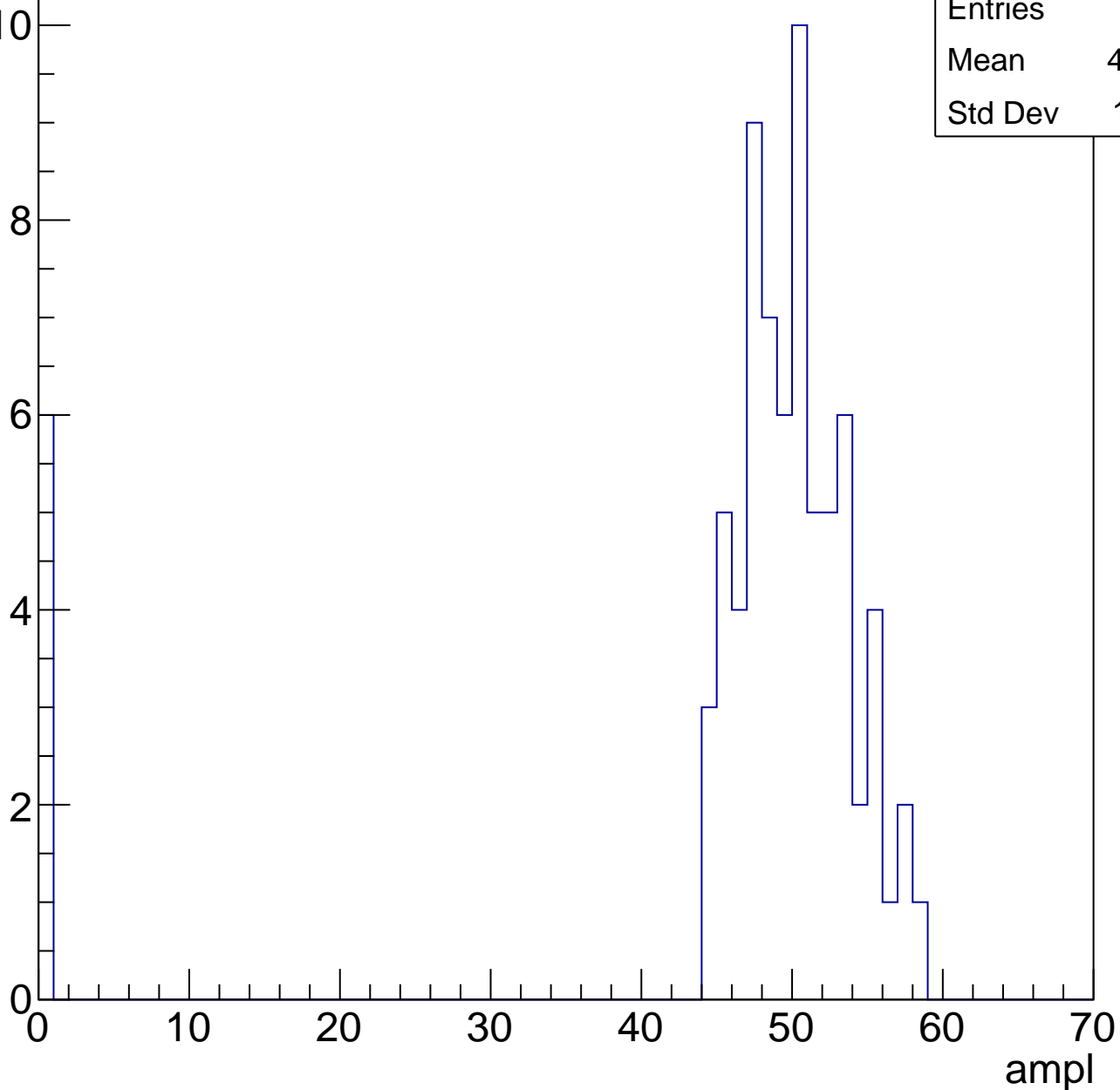


B1L103S, U23-ch77, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	76
Mean	45.83
Std Dev	13.81

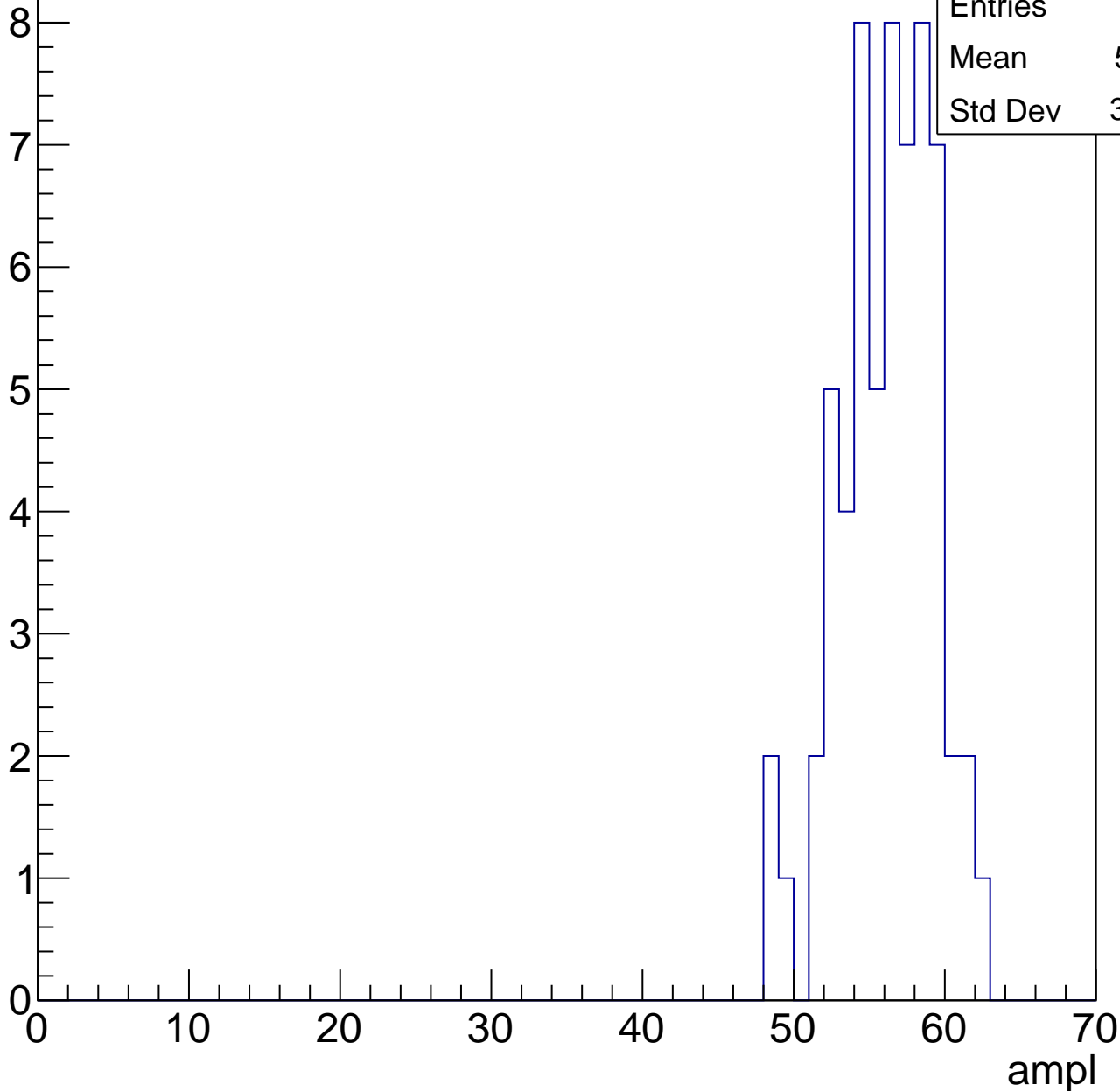


B1L103S, U23-ch77, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

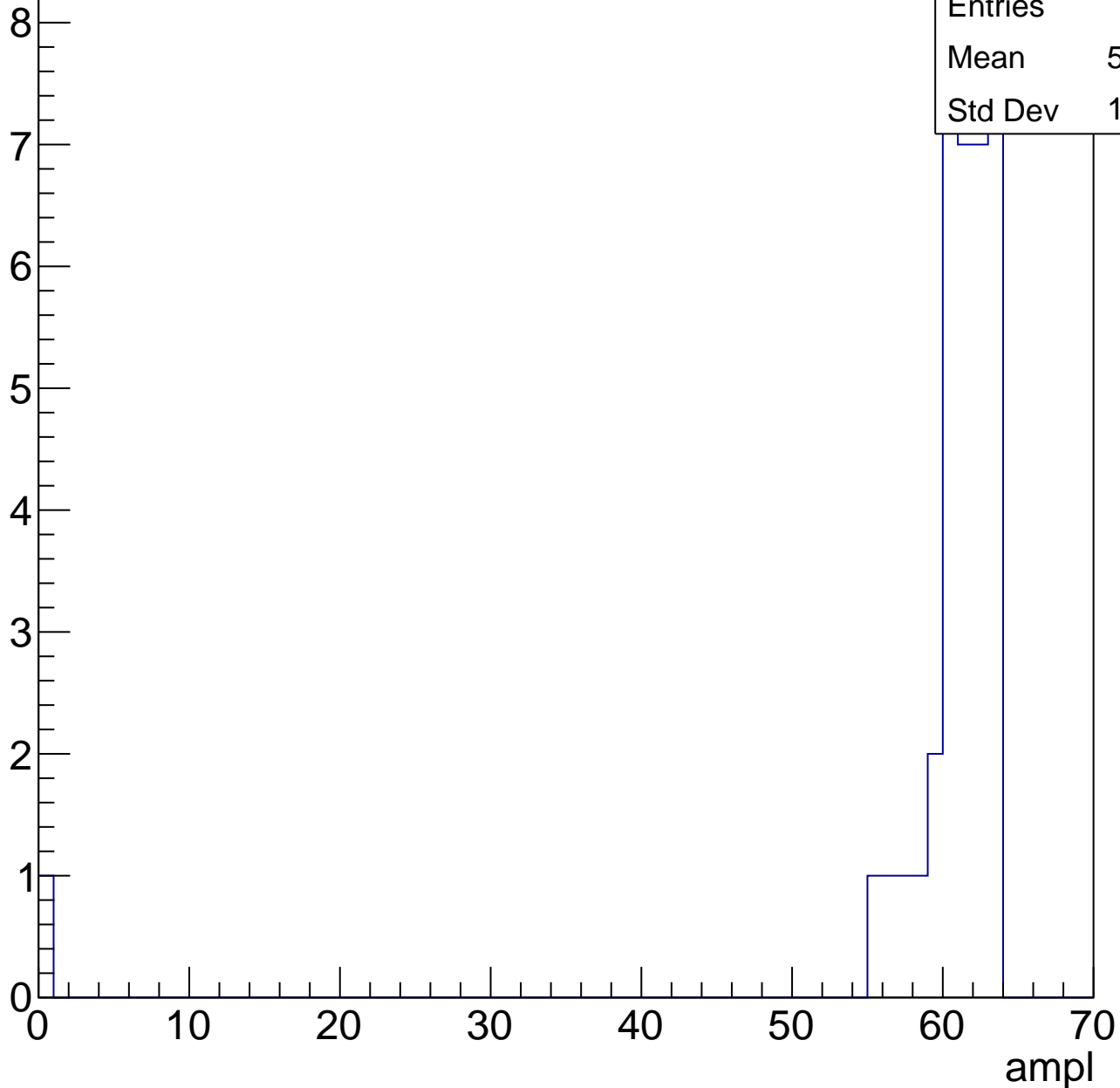
Entries	62
Mean	55.71
Std Dev	3.097



B1L103S, U23-ch77, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	37
Mean	59.16
Std Dev	10.05

B1L103S, U23-ch77, adc6

calib_packv5_041523_1651.root, FC#0, port C2

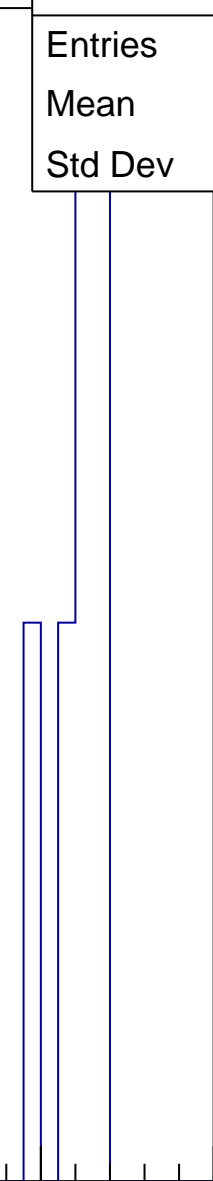
Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	6
Mean	61.67
Std Dev	1.374

0 10 20 30 40 50 60 70

ampl

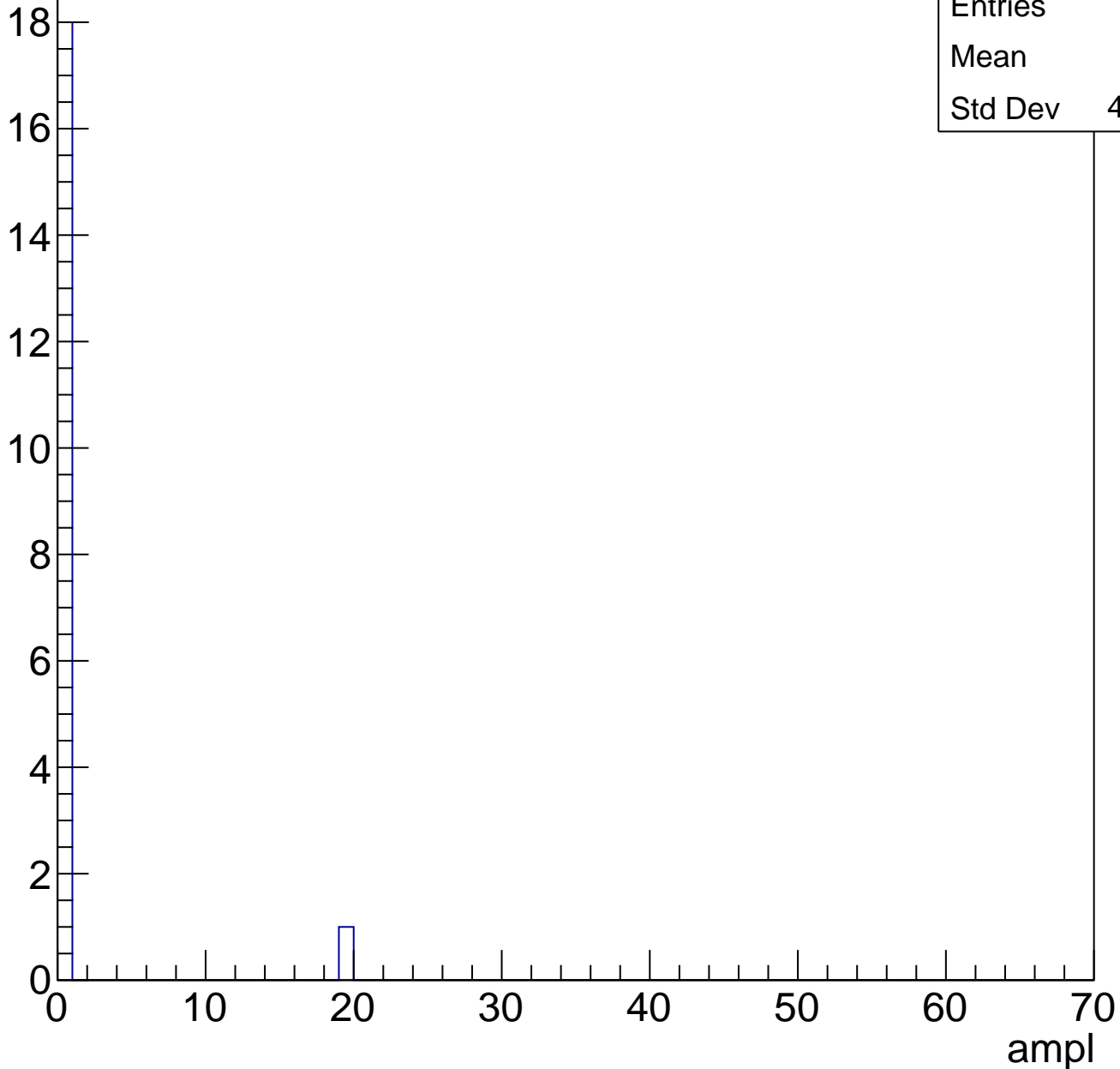


B1L103S, U23-ch77, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1
Std Dev	4.243

Entry

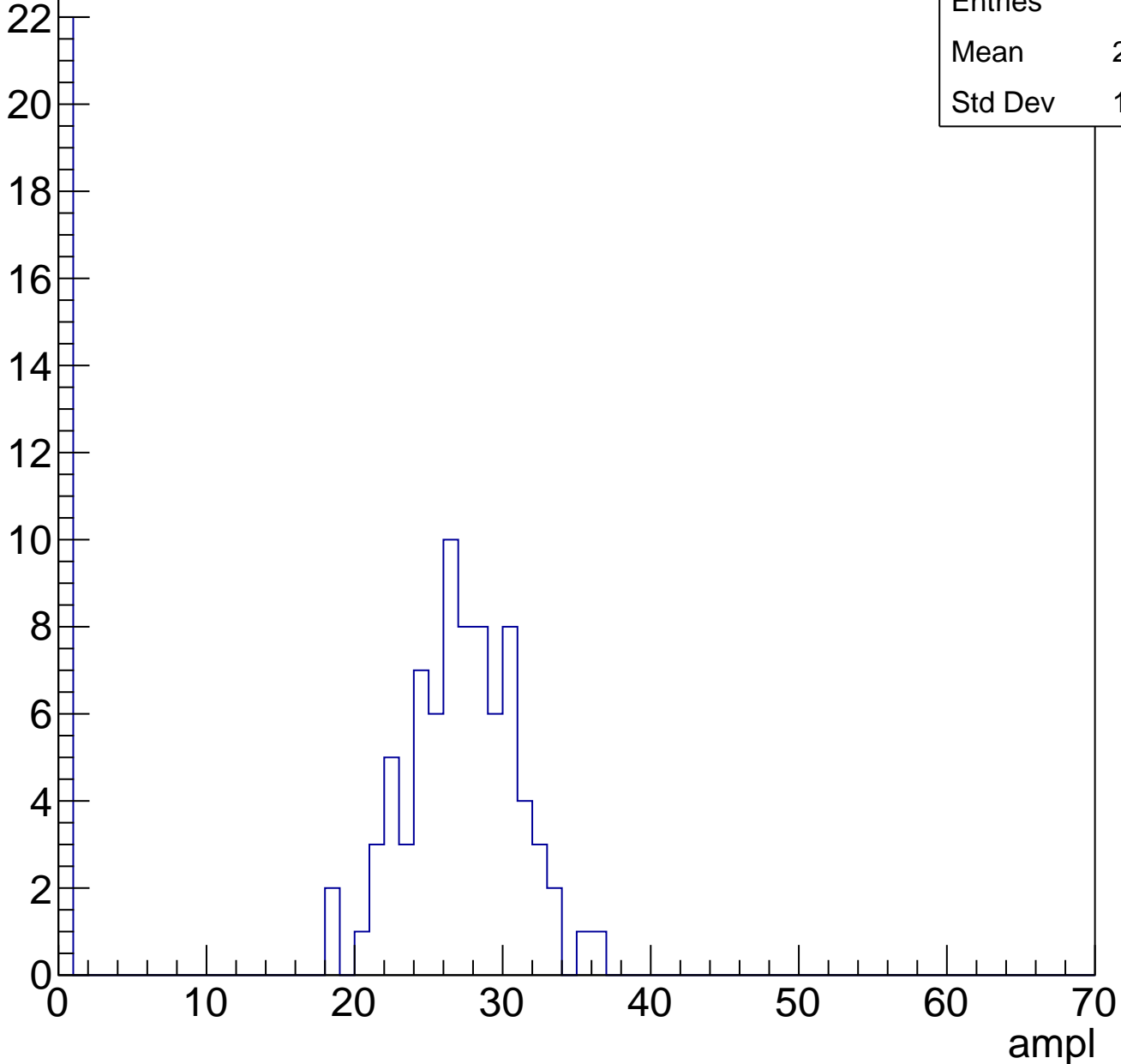


B1L103S, U23-ch78, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	100
Mean	20.87
Std Dev	11.55

Entry

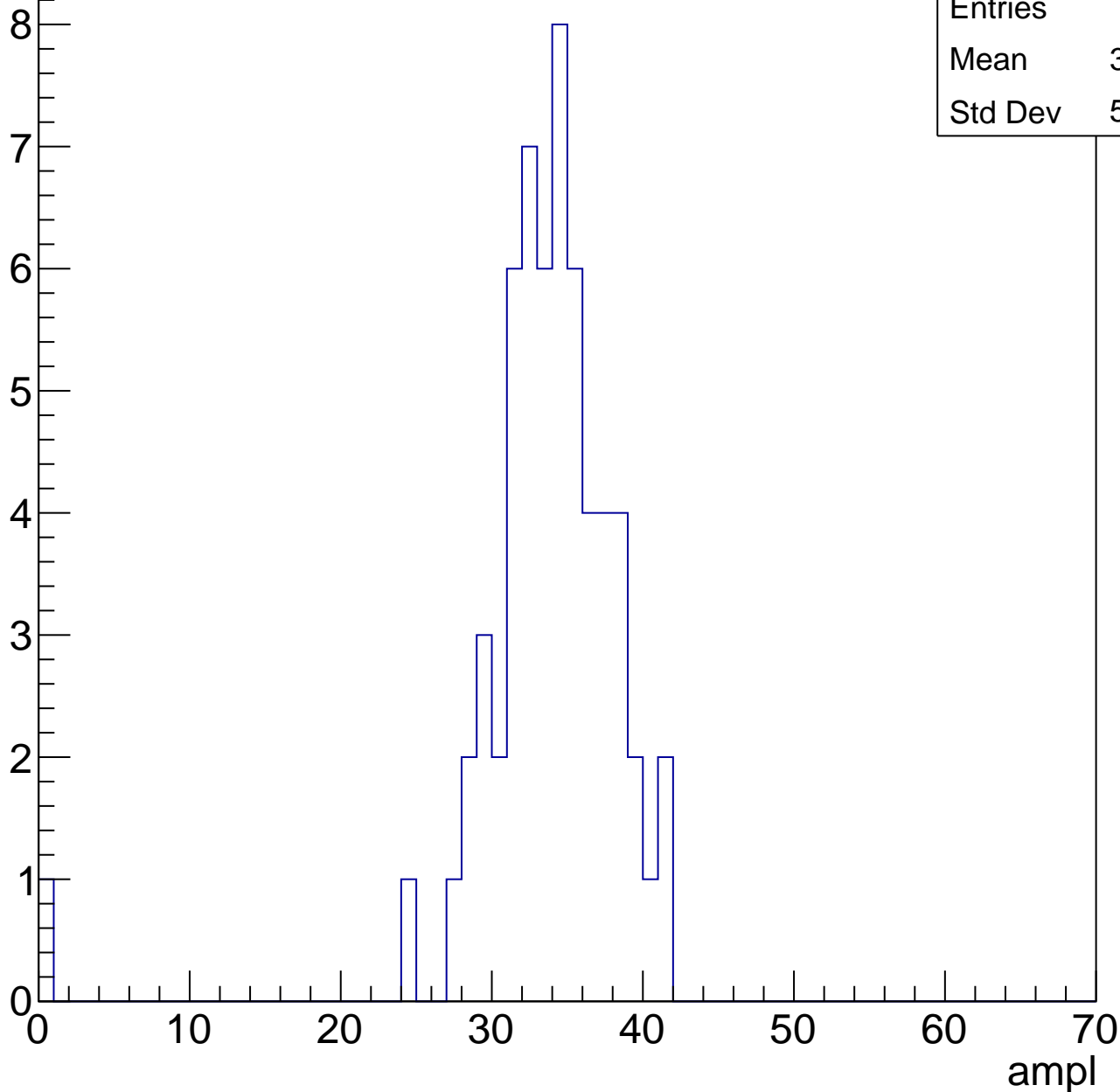


B1L103S, U23-ch78, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	33.13
Std Dev	5.527

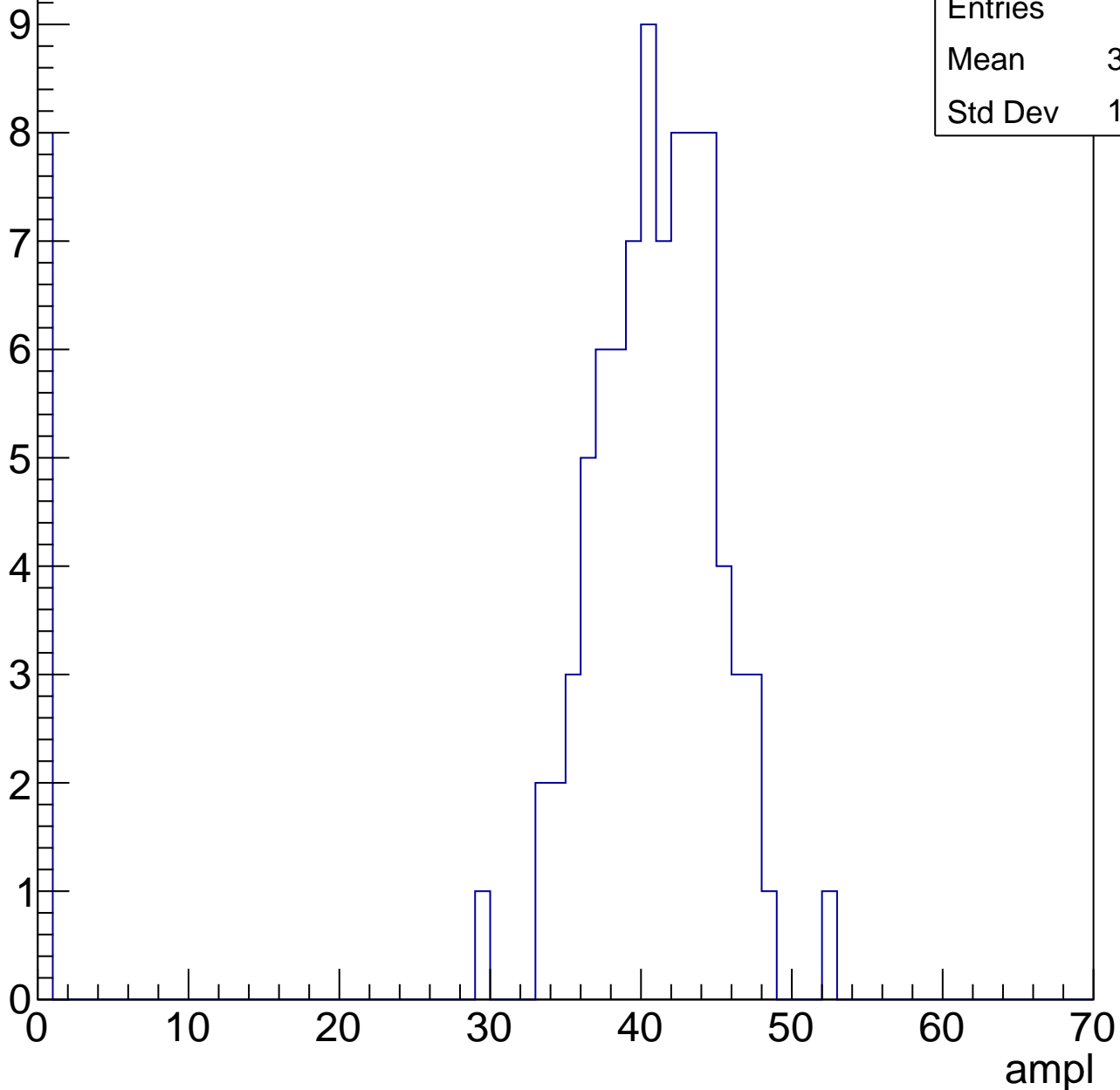


B1L103S, U23-ch78, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	92
Mean	37.05
Std Dev	12.04

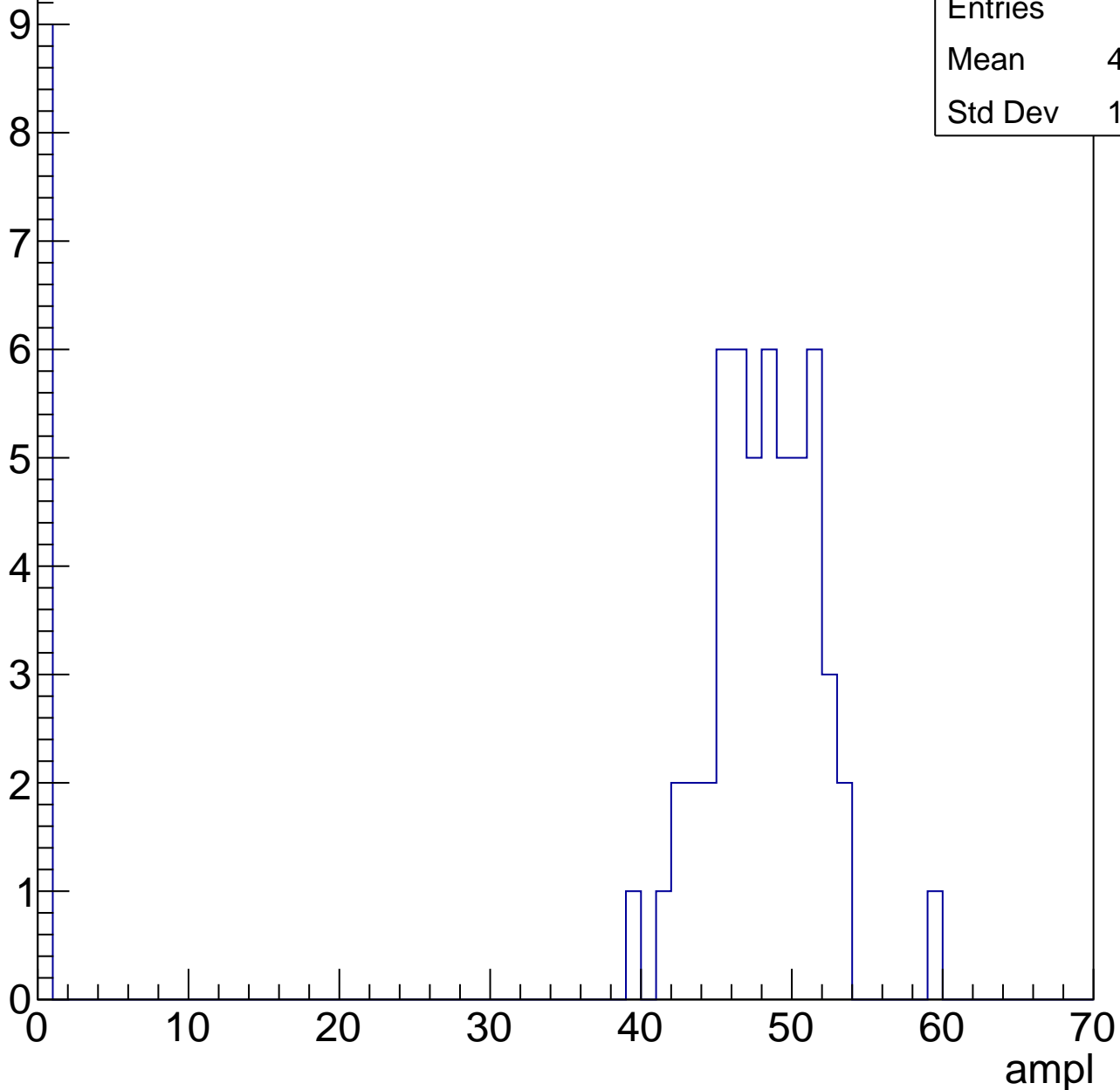


B1L103S, U23-ch78, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

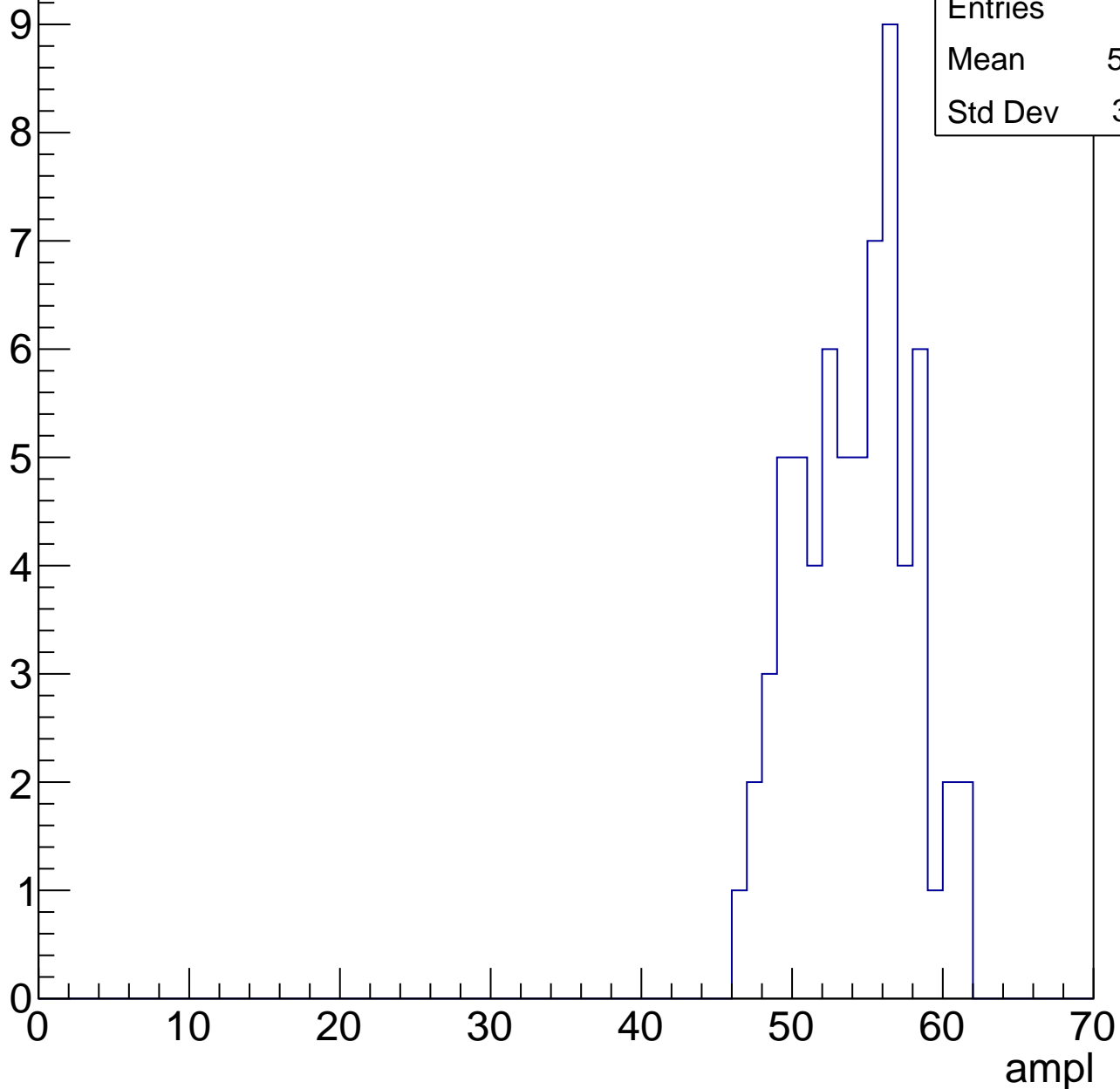
Entries	62
Mean	40.79
Std Dev	17.12



B1L103S, U23-ch78, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

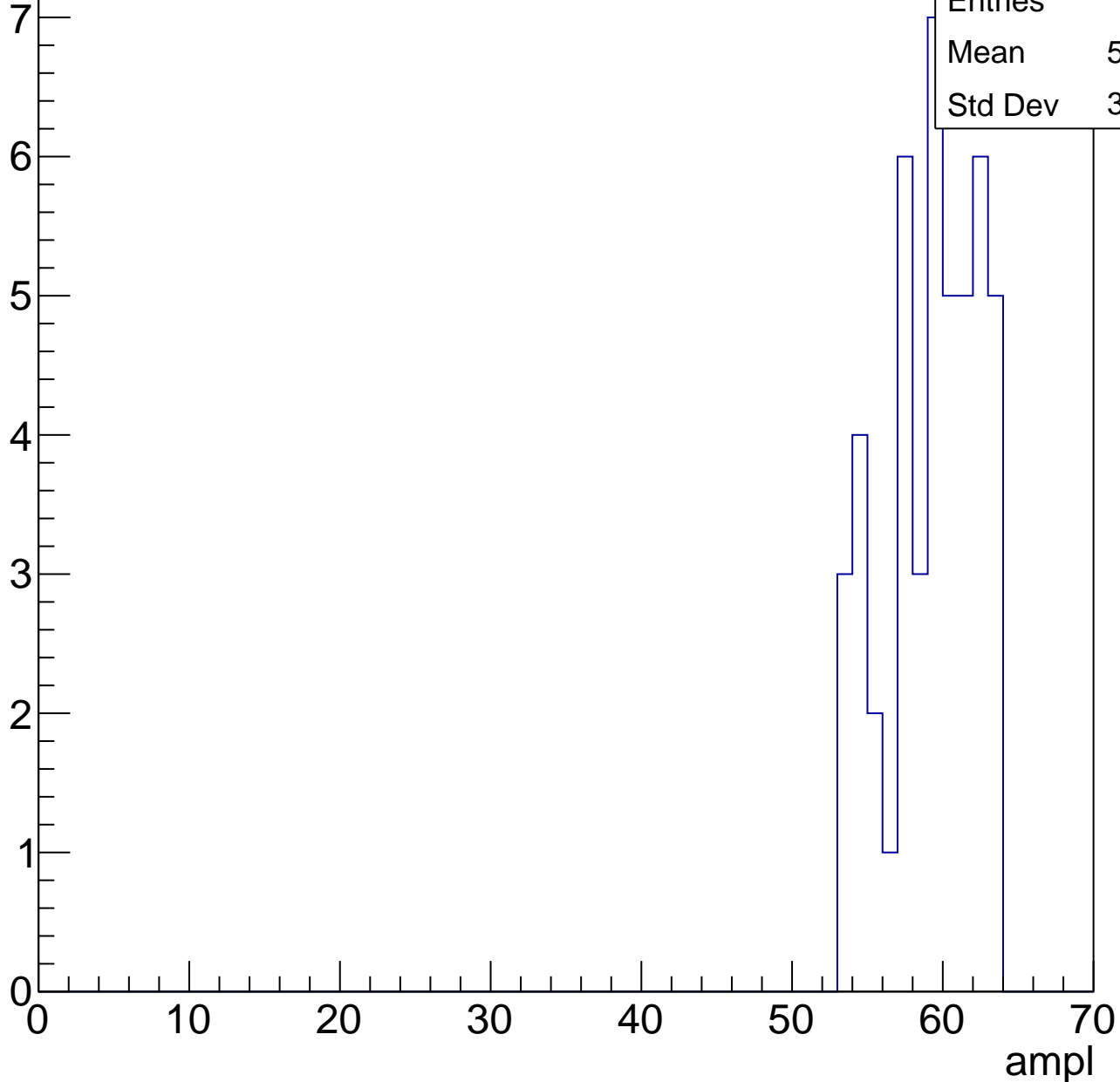


Entries	67
Mean	53.67
Std Dev	3.671

B1L103S, U23-ch78, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

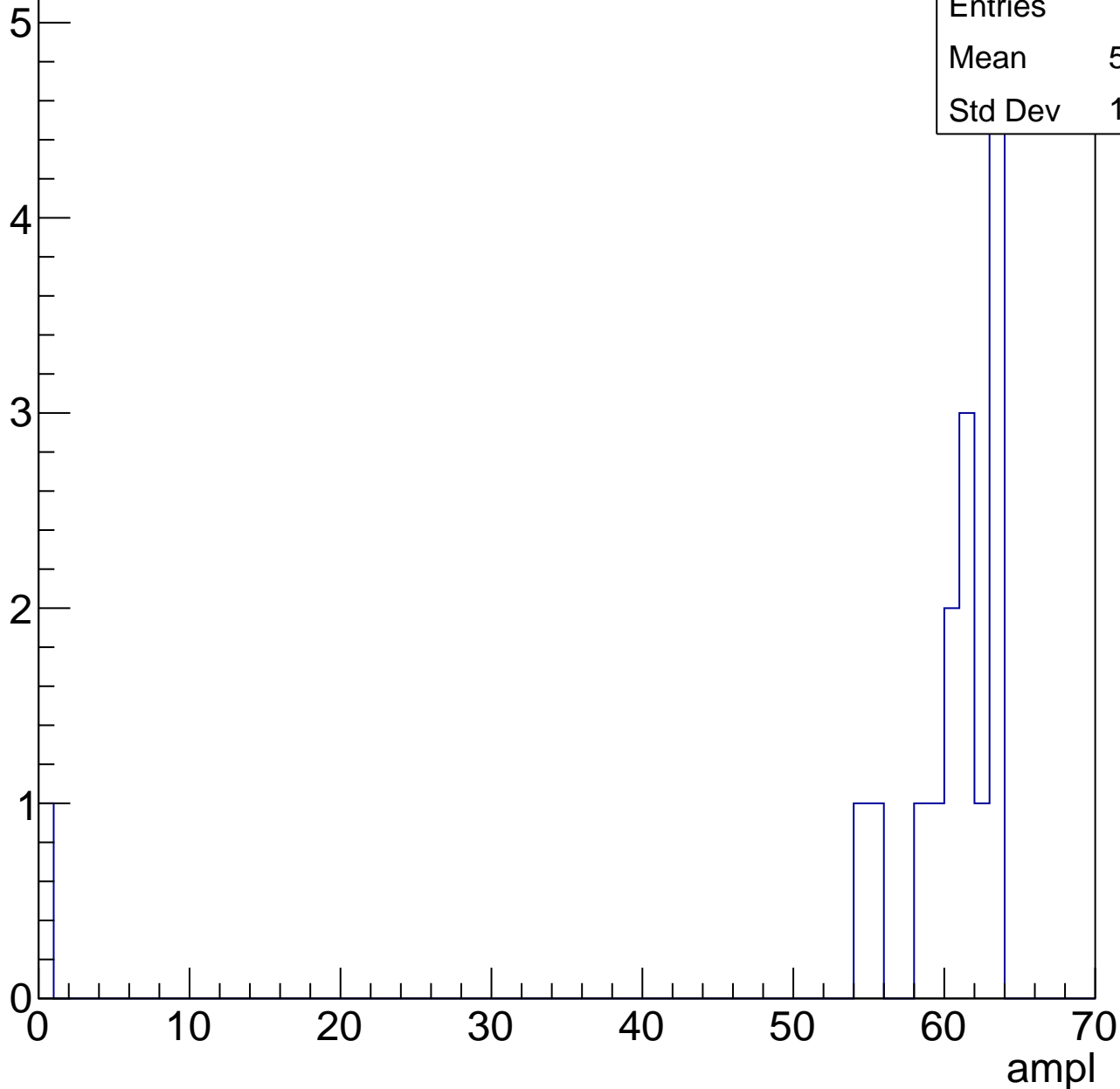


B1L103S, U23-ch78, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	16
Mean	56.62
Std Dev	14.87

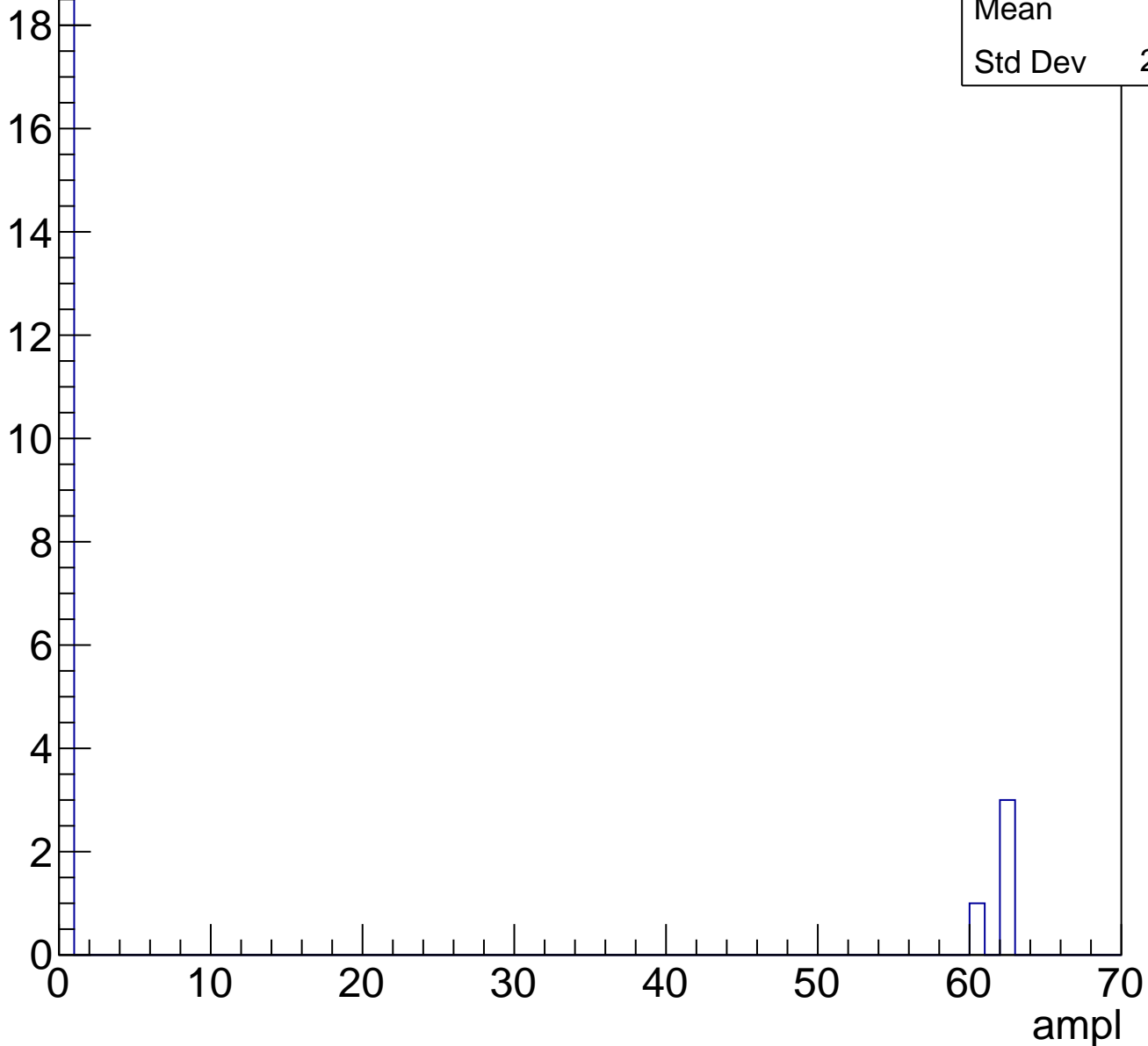


B1L103S, U23-ch78, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	23
Mean	10.7
Std Dev	23.31

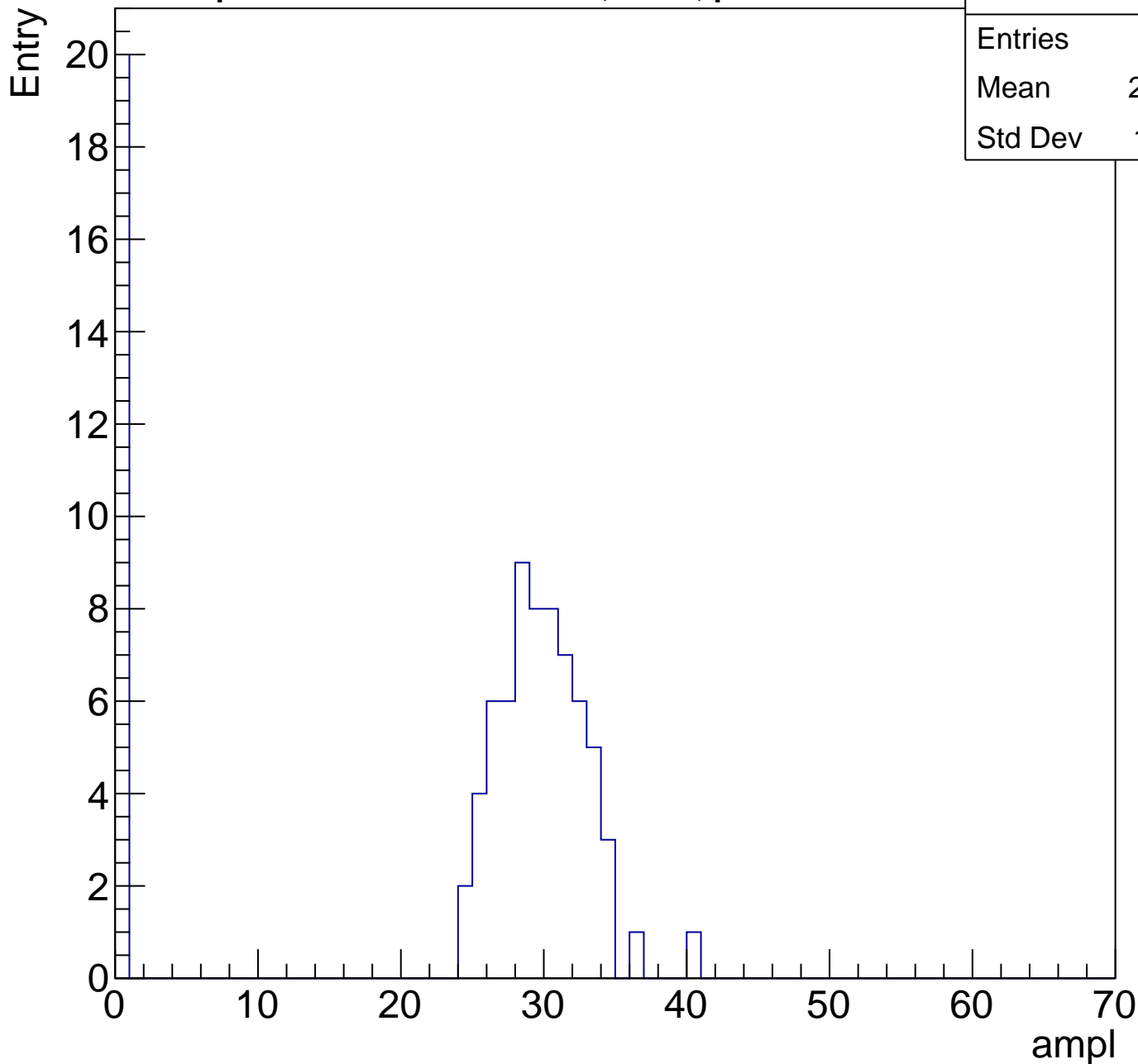
Entry



B1L103S, U23-ch79, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	86
Mean	22.58
Std Dev	12.71

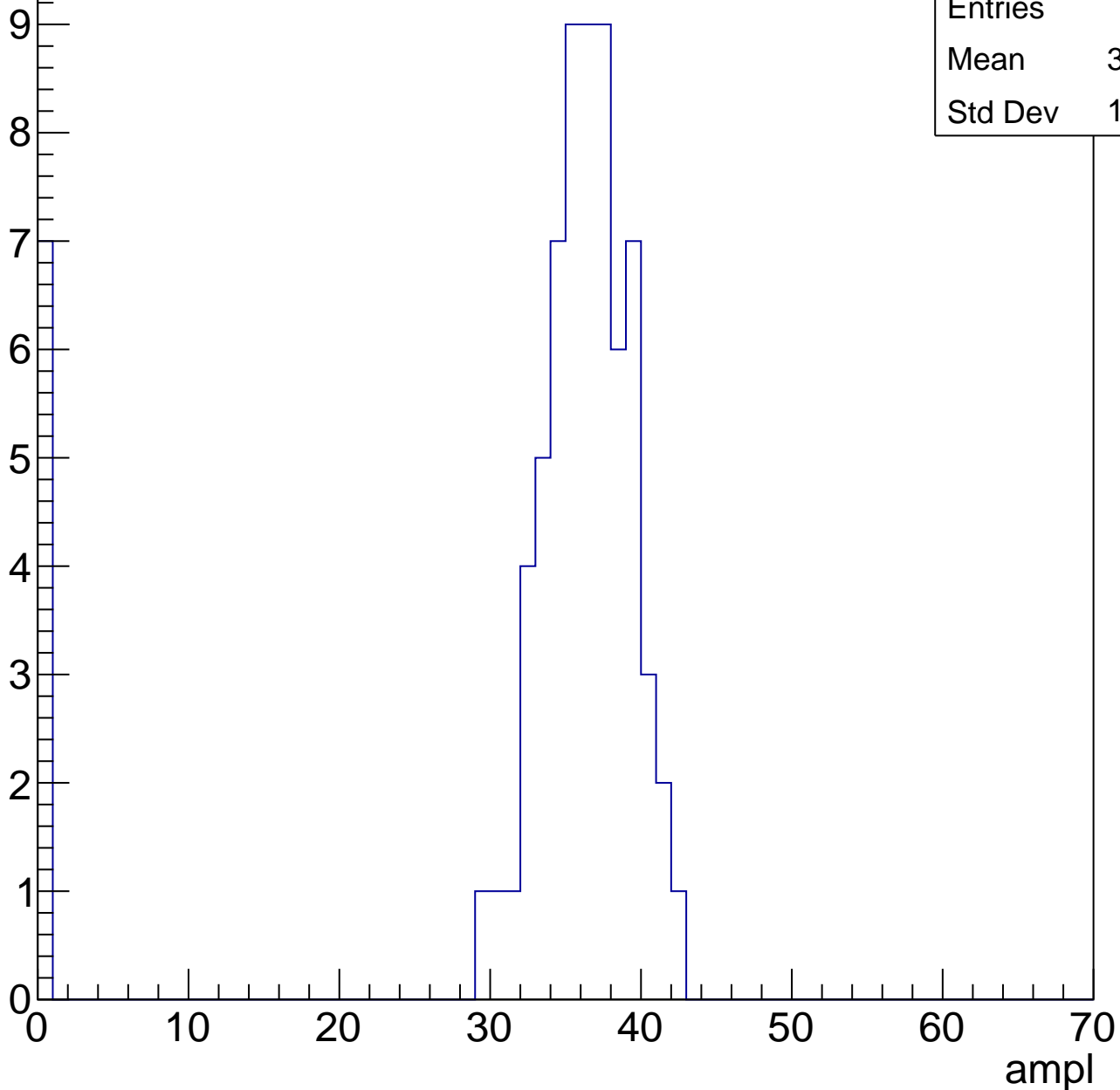


B1L103S, U23-ch79, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	72
Mean	32.47
Std Dev	10.97



B1L103S, U23-ch79, adc2

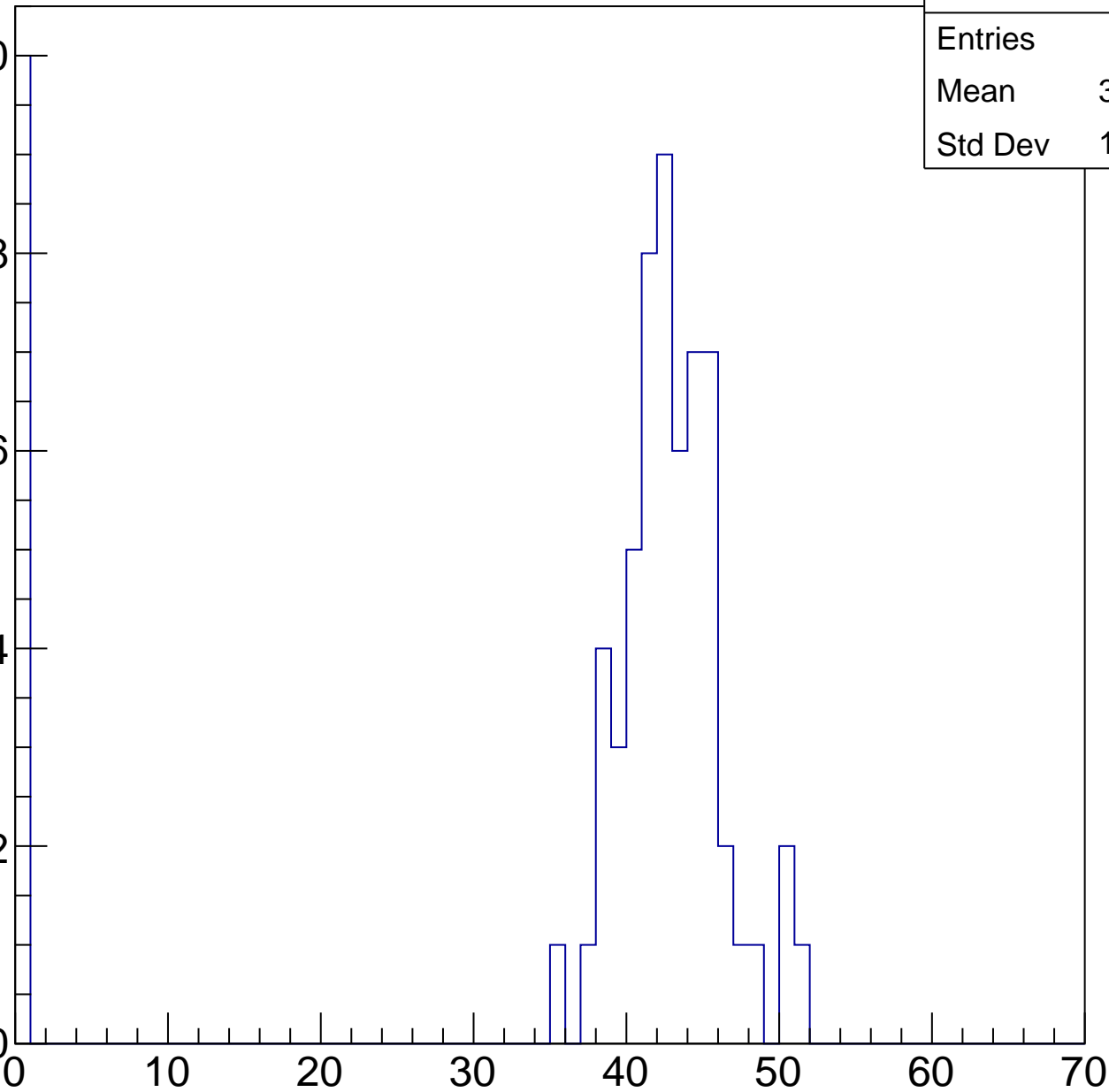
calib_packv5_041523_1651.root, FC#0, port C2

Entries	68
Mean	36.26
Std Dev	15.34

Entry

10
8
6
4
2
0

ampl

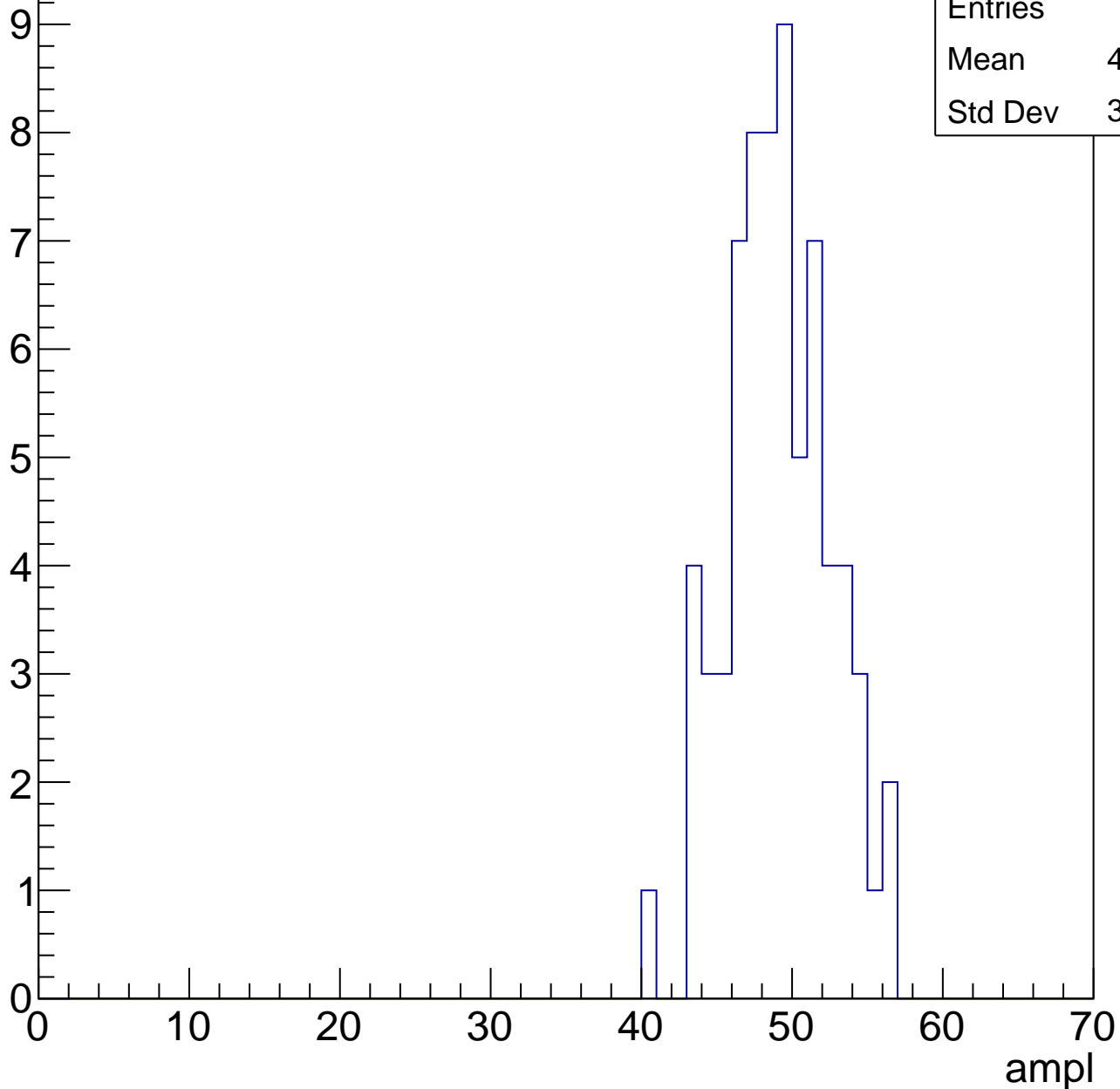


B1L103S, U23-ch79, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	48.67
Std Dev	3.374

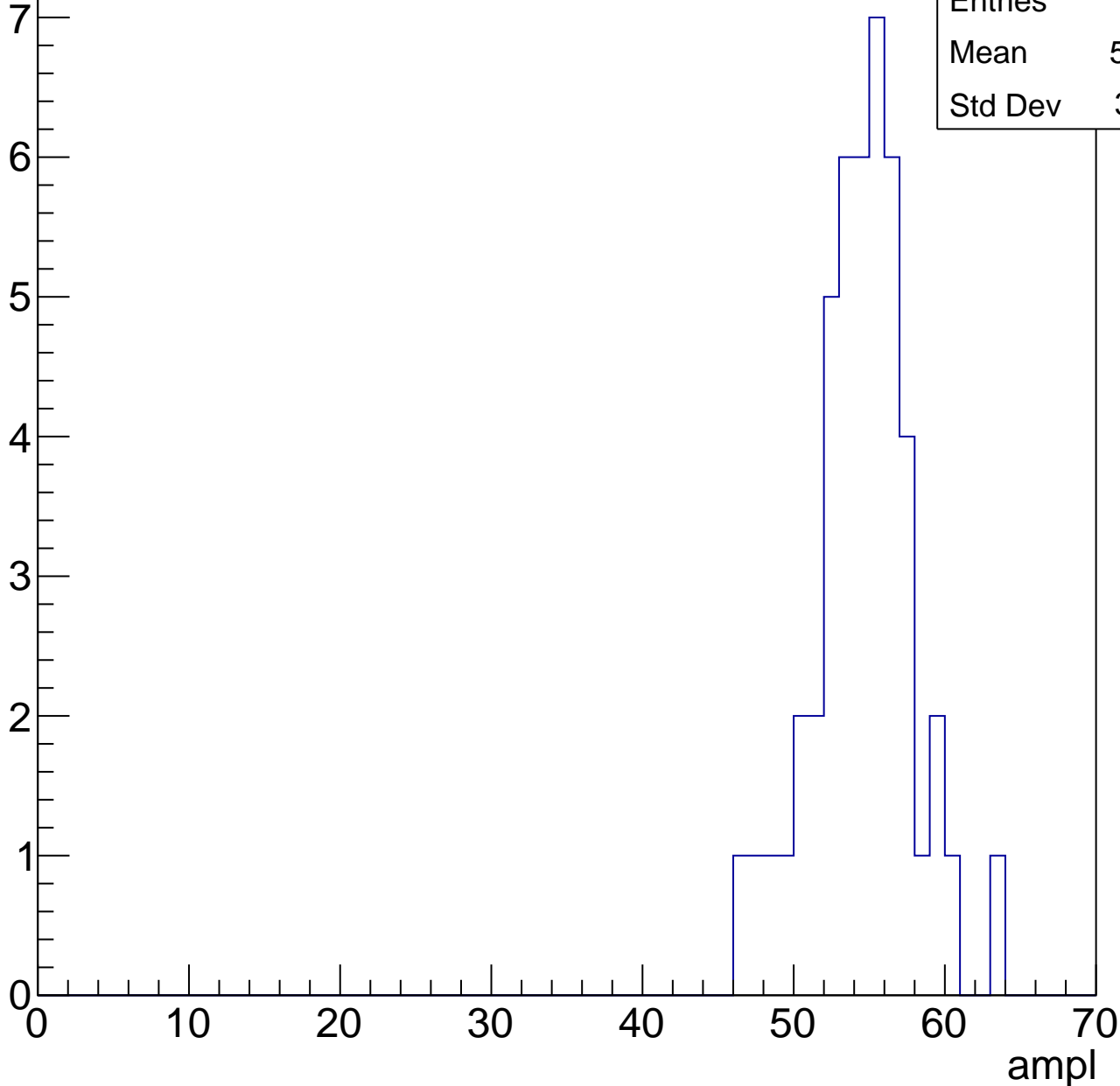


B1L103S, U23-ch79, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	47
Mean	54.09
Std Dev	3.261

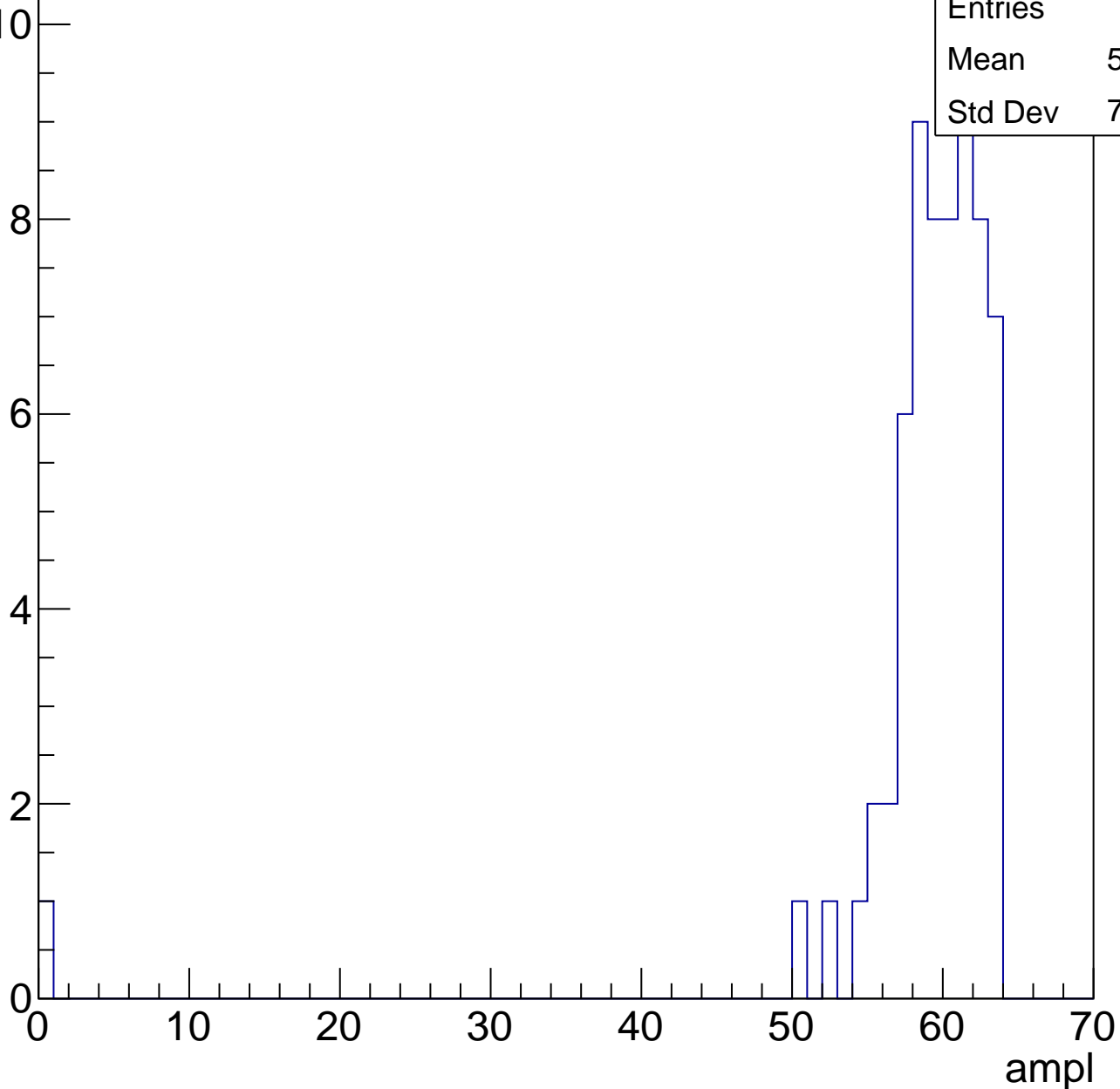


B1L103S, U23-ch79, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	58.45
Std Dev	7.838



B1L103S, U23-ch79, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch79, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.211
Std Dev	5.136

Entry

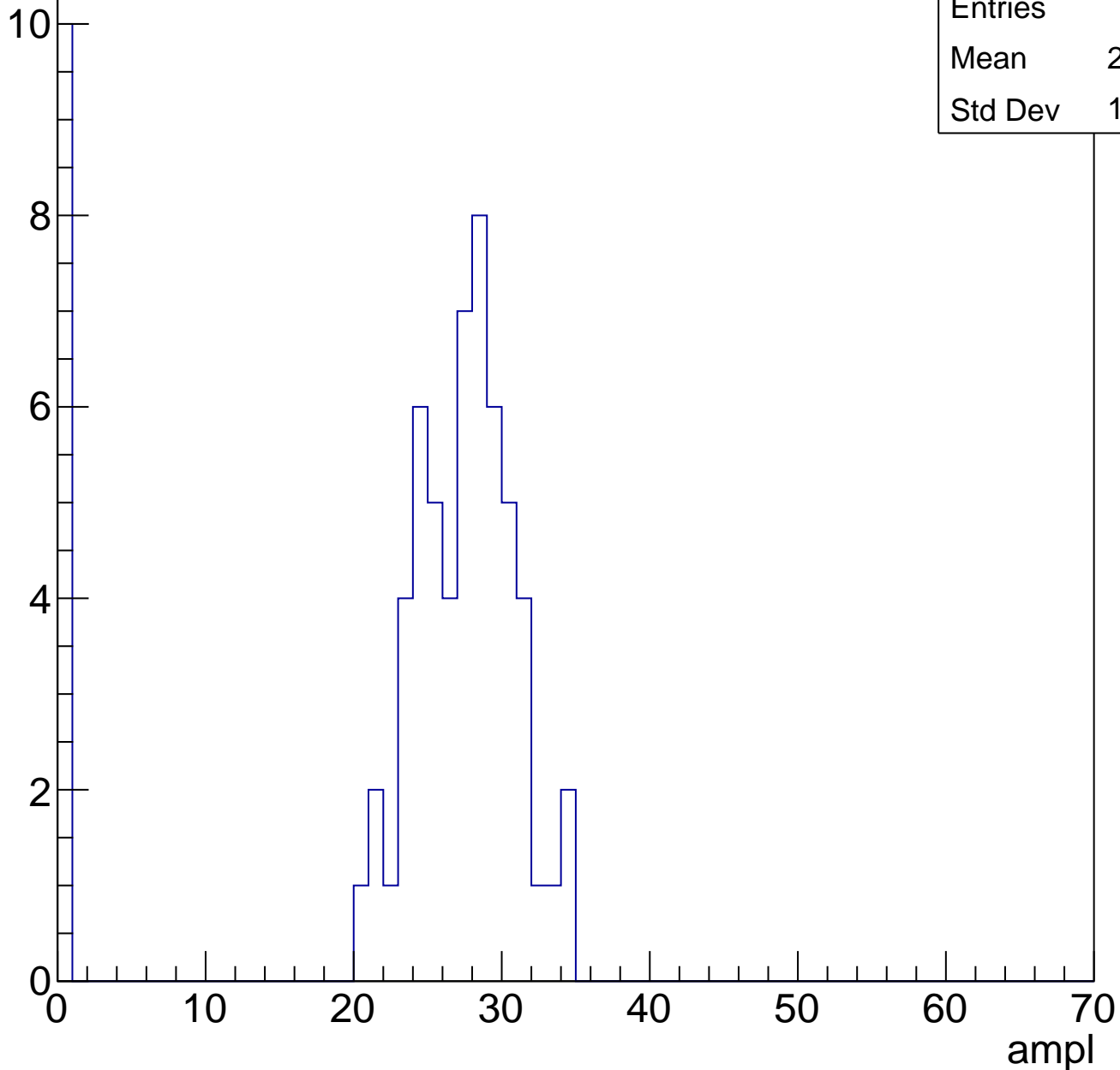


B1L103S, U23-ch80, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	67
Mean	23.03
Std Dev	10.09

Entry

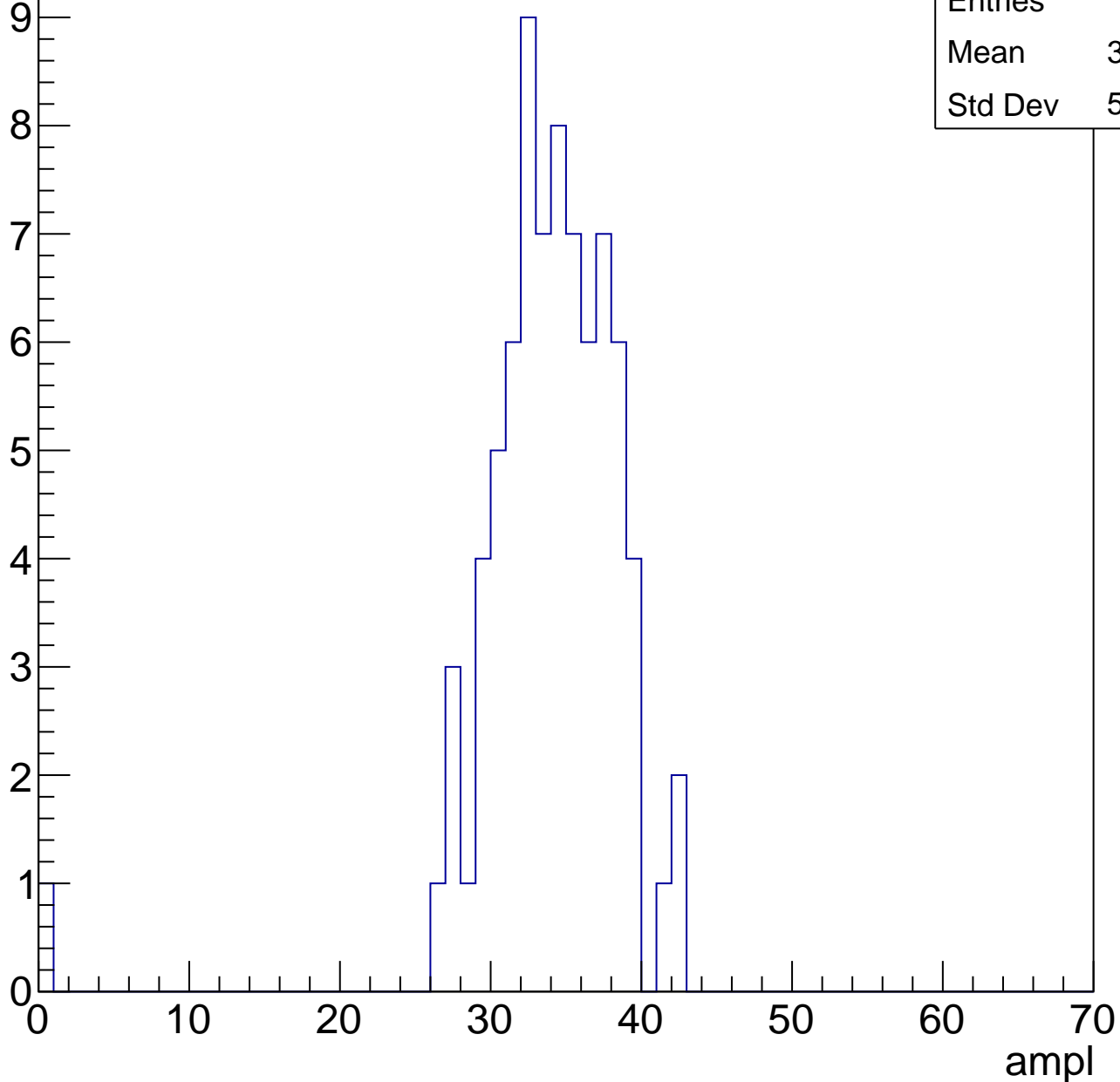


B1L103S, U23-ch80, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	78
Mean	33.42
Std Dev	5.215

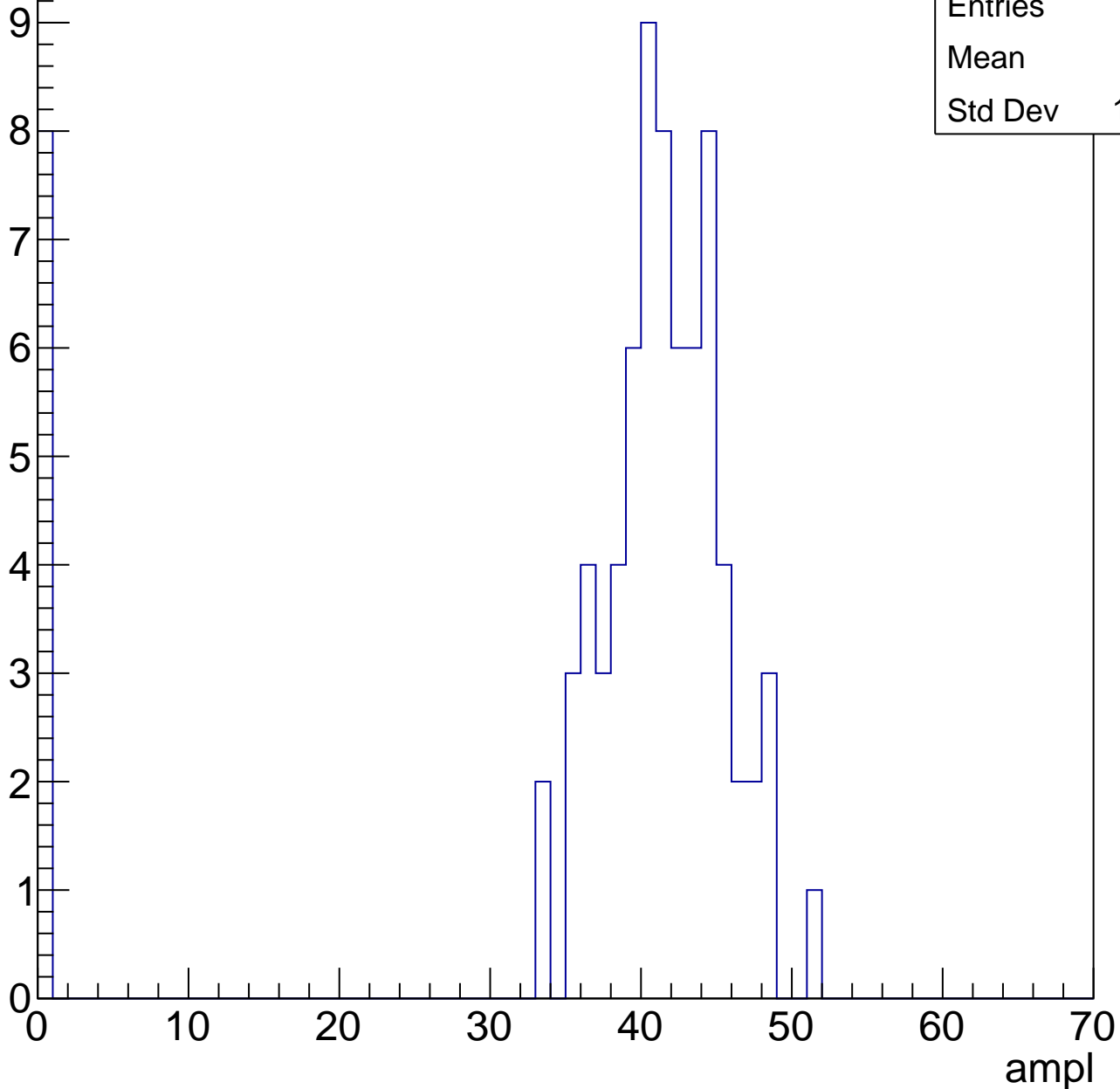


B1L103S, U23-ch80, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	79
Mean	37
Std Dev	12.91

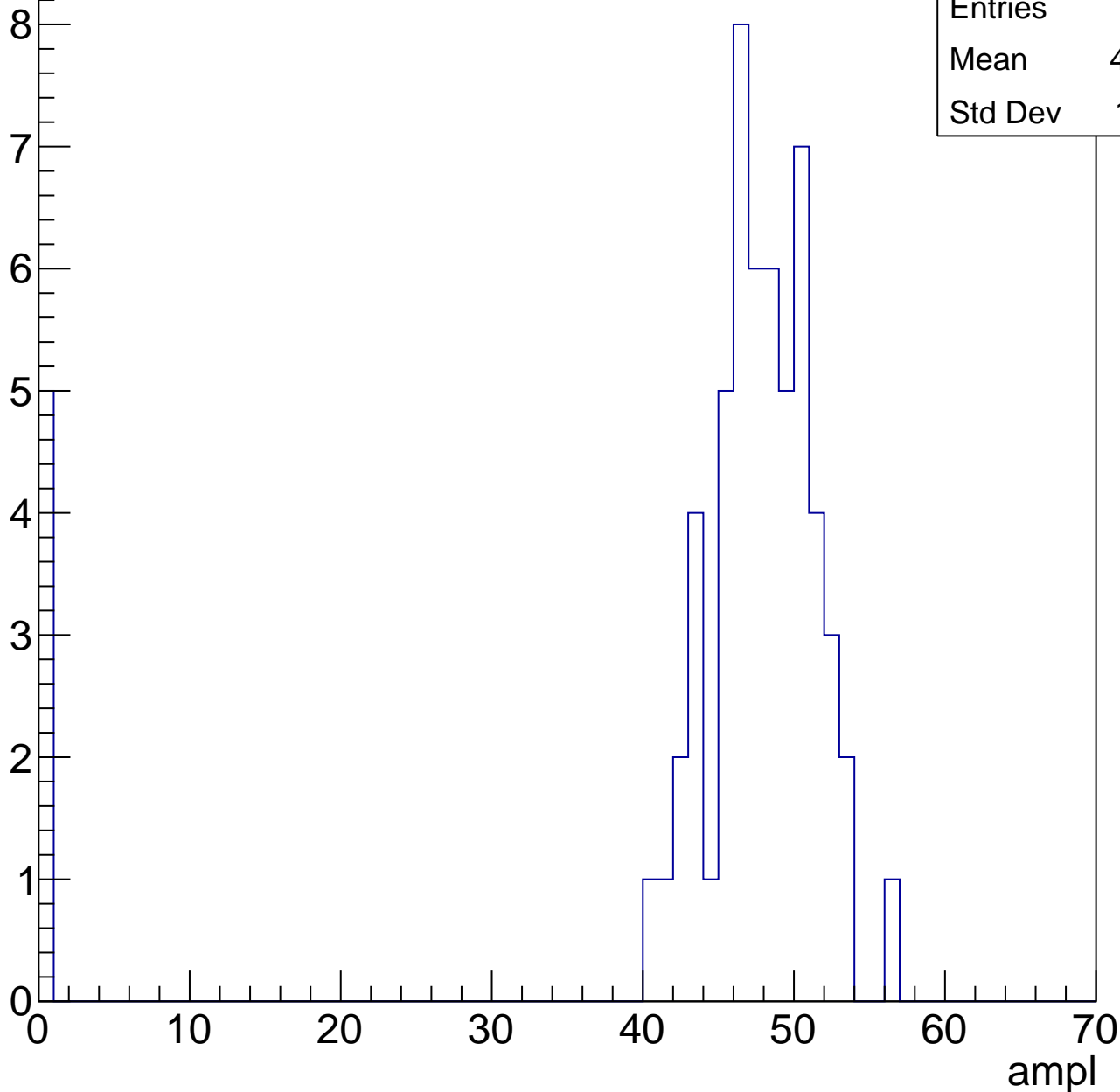


B1L103S, U23-ch80, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	43.62
Std Dev	13.41

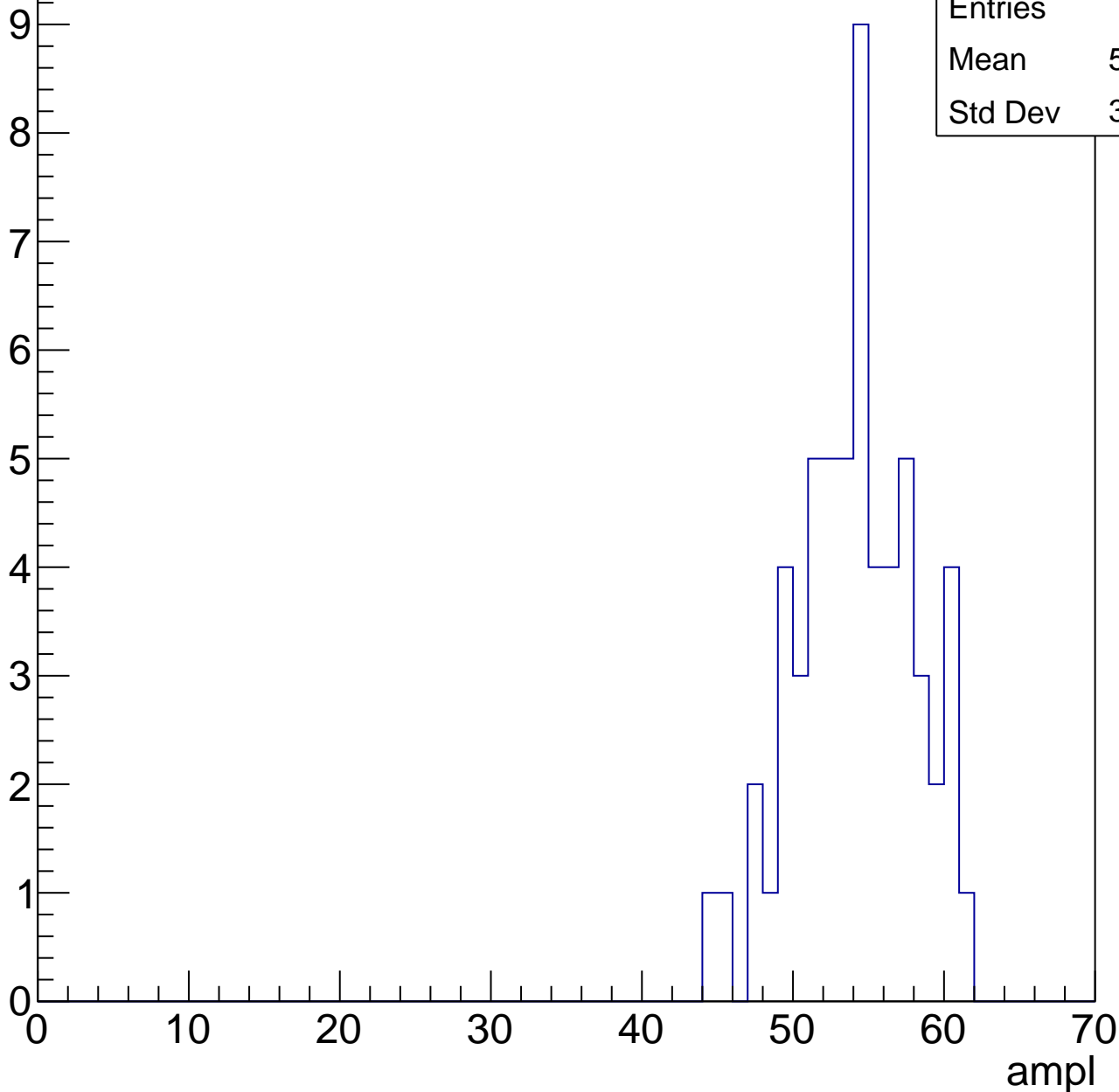


B1L103S, U23-ch80, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

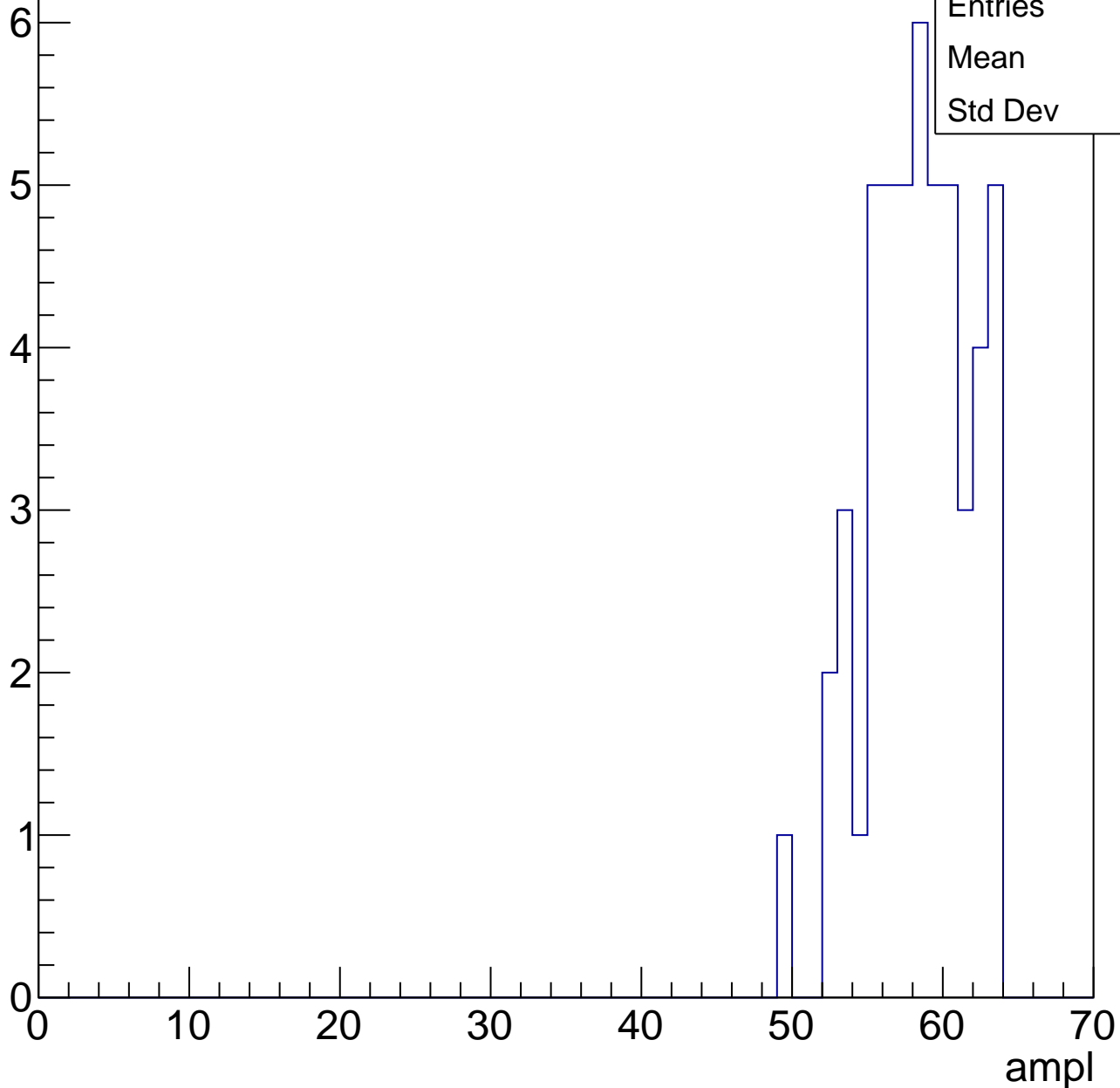
Entries	59
Mean	53.64
Std Dev	3.865



B1L103S, U23-ch80, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

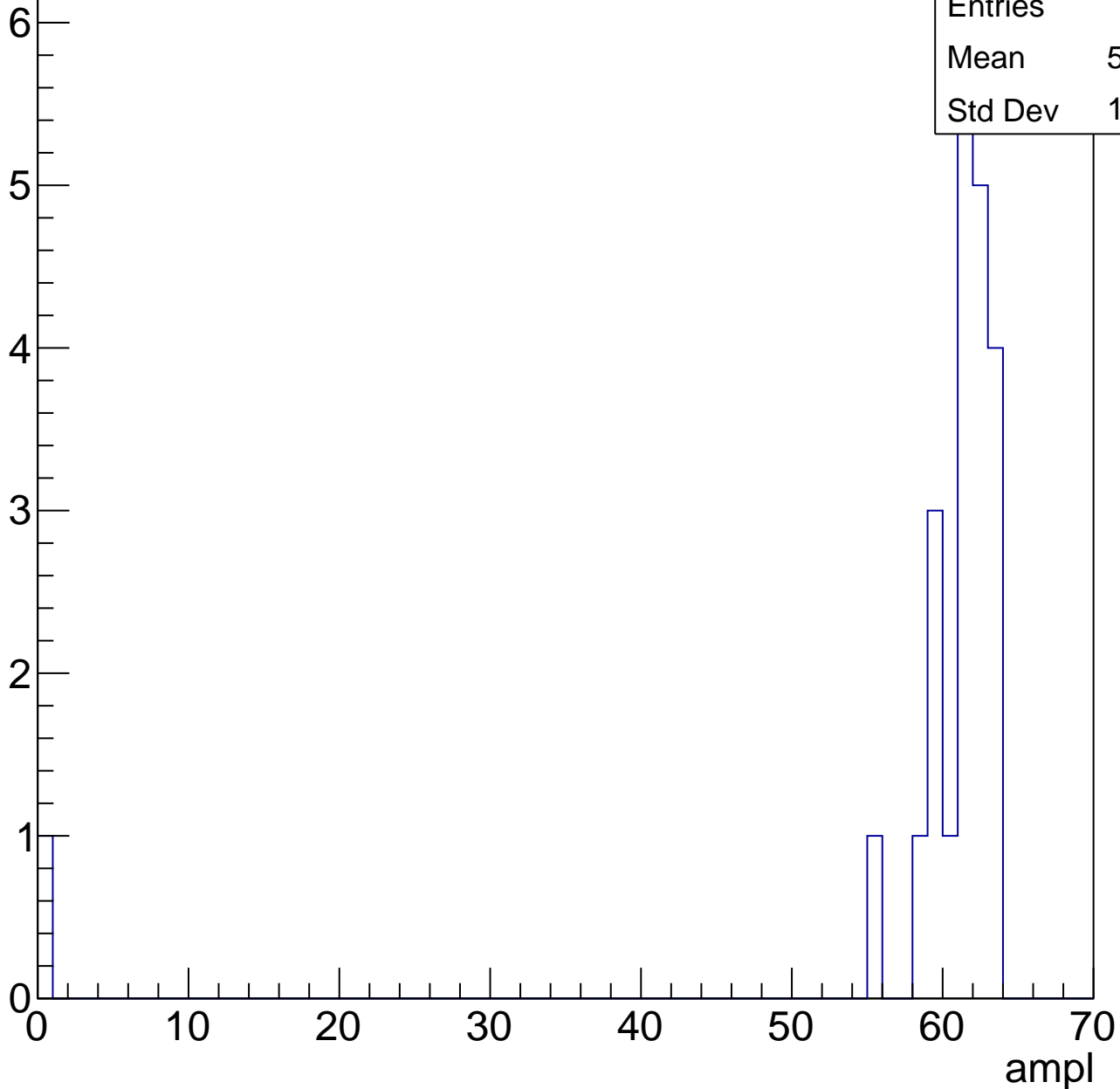


B1L103S, U23-ch80, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	22
Mean	58.09
Std Dev	12.82

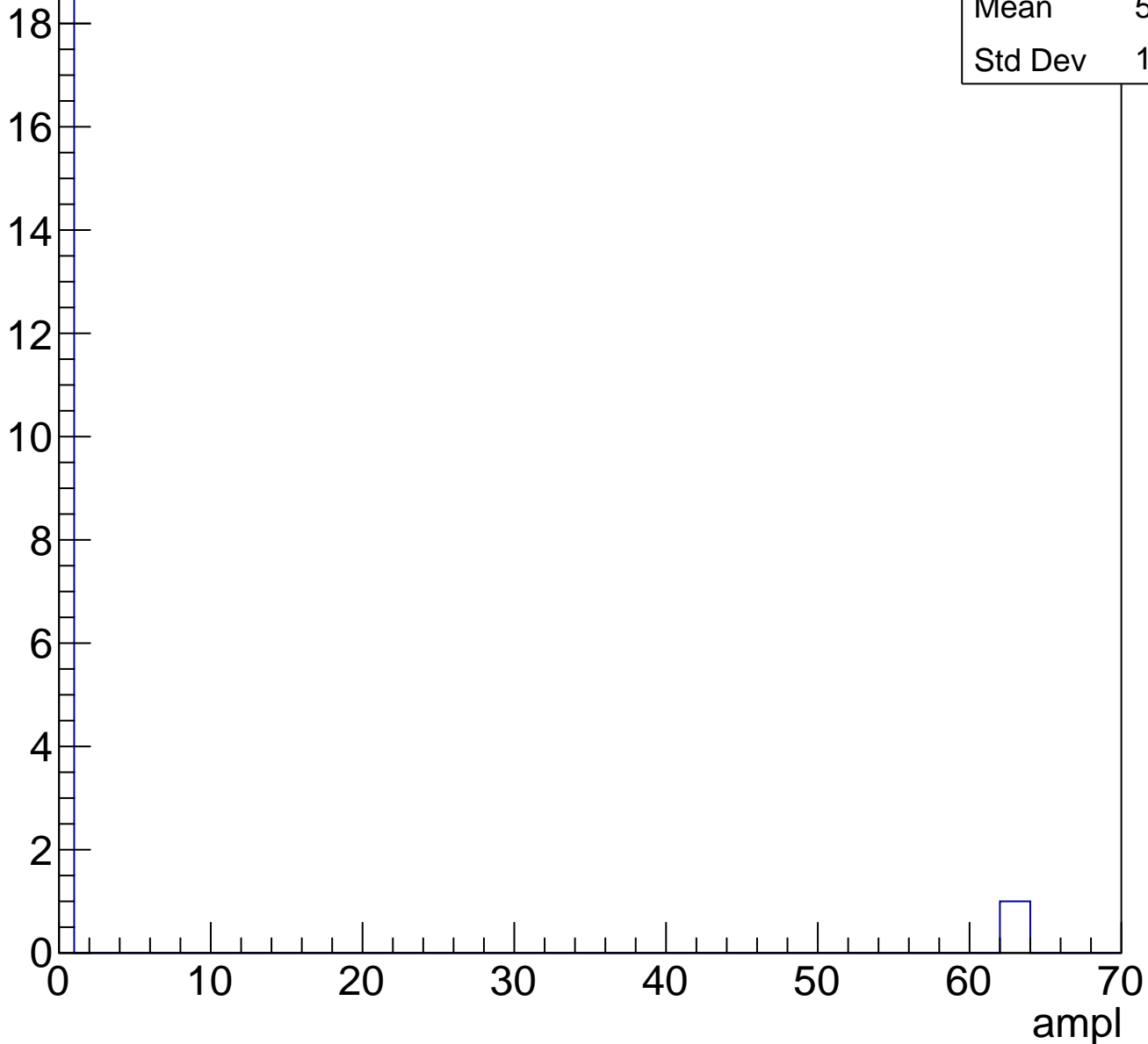


B1L103S, U23-ch80, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	21
Mean	5.952
Std Dev	18.35

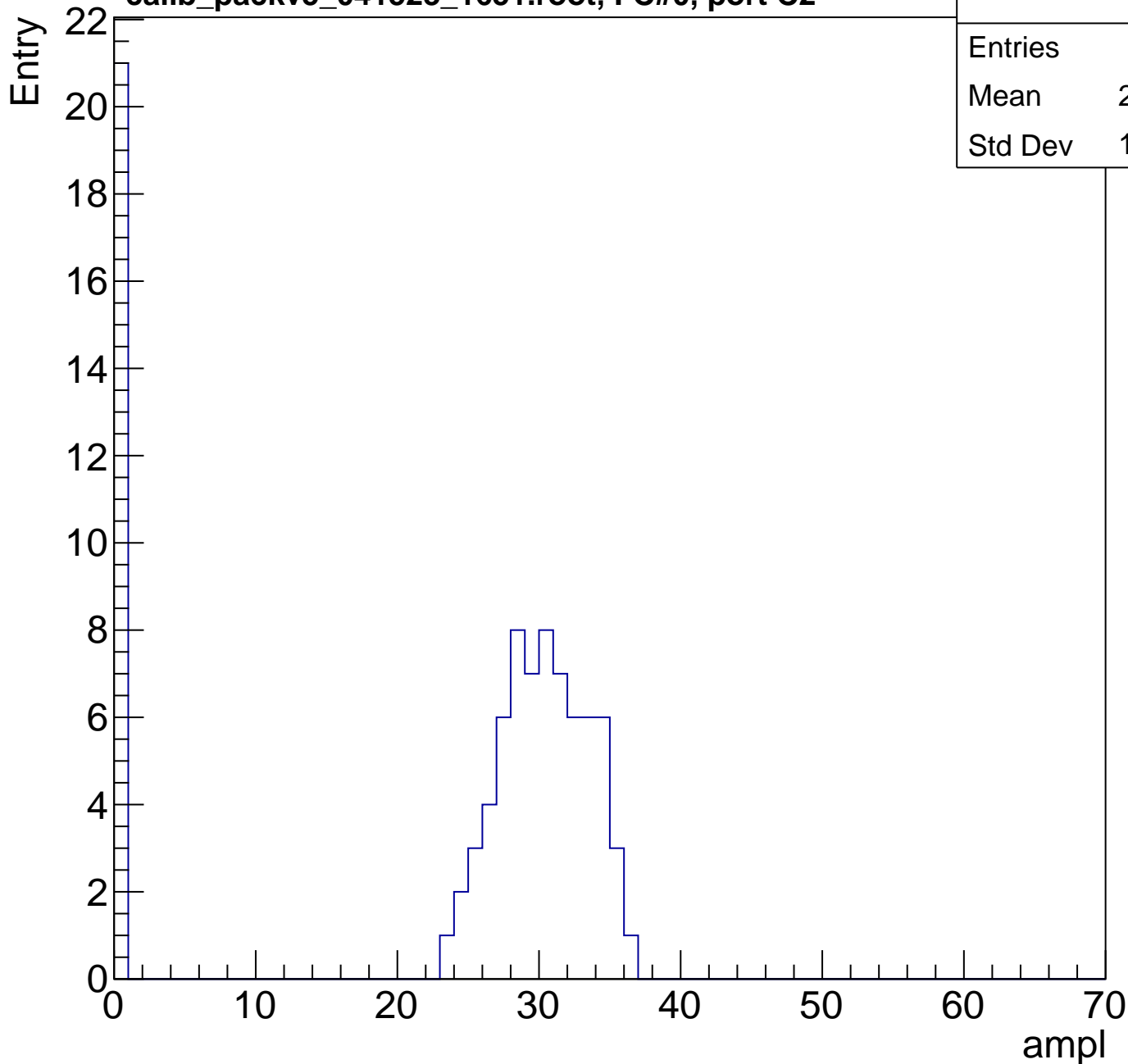
Entry



B1L103S, U23-ch81, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	89
Mean	22.82
Std Dev	12.96



B1L103S, U23-ch81, adc1

calib_packv5_041523_1651.root, FC#0, port C2

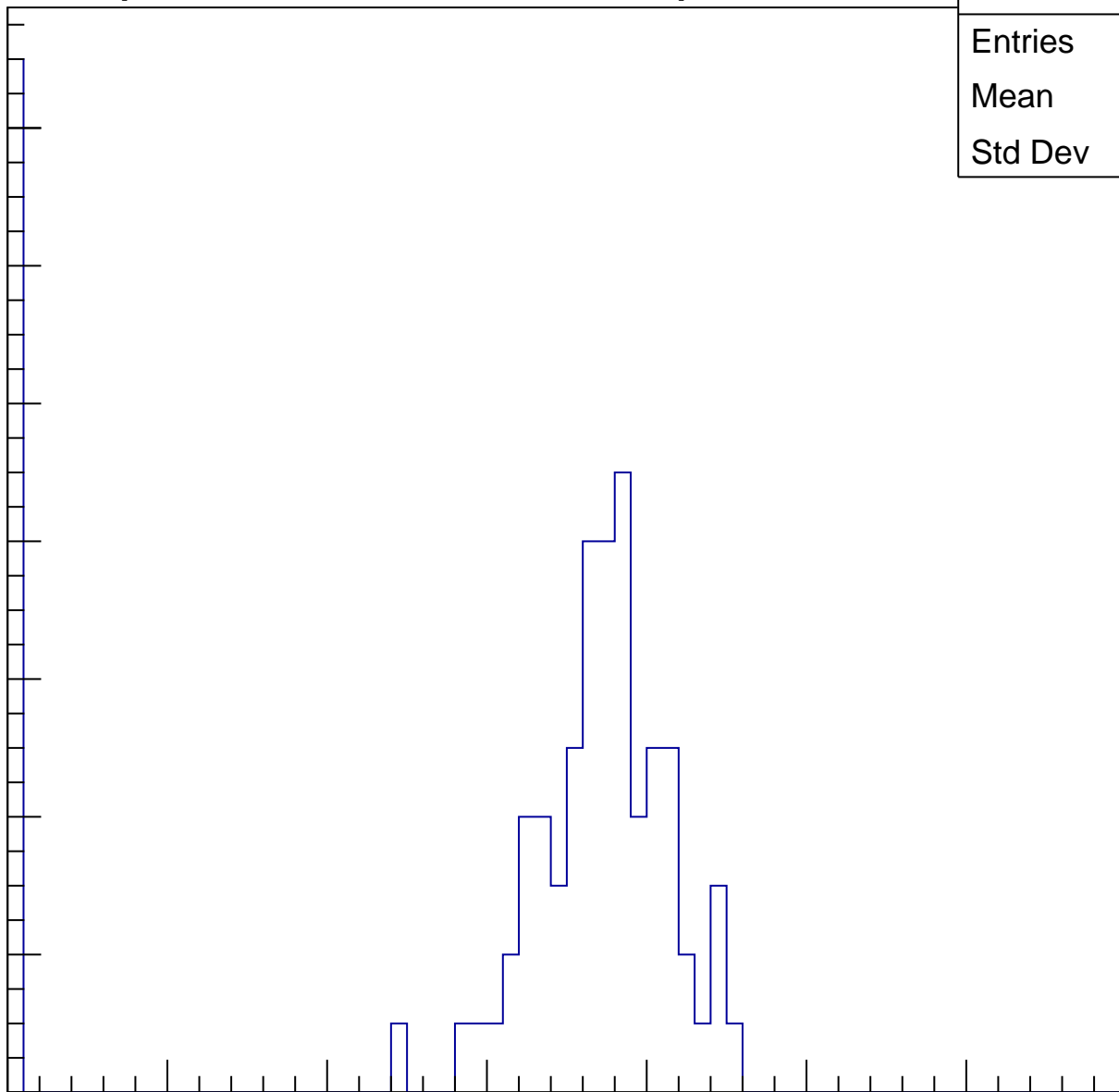
Entries	83
Mean	30.13
Std Dev	14.61

Entry

14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

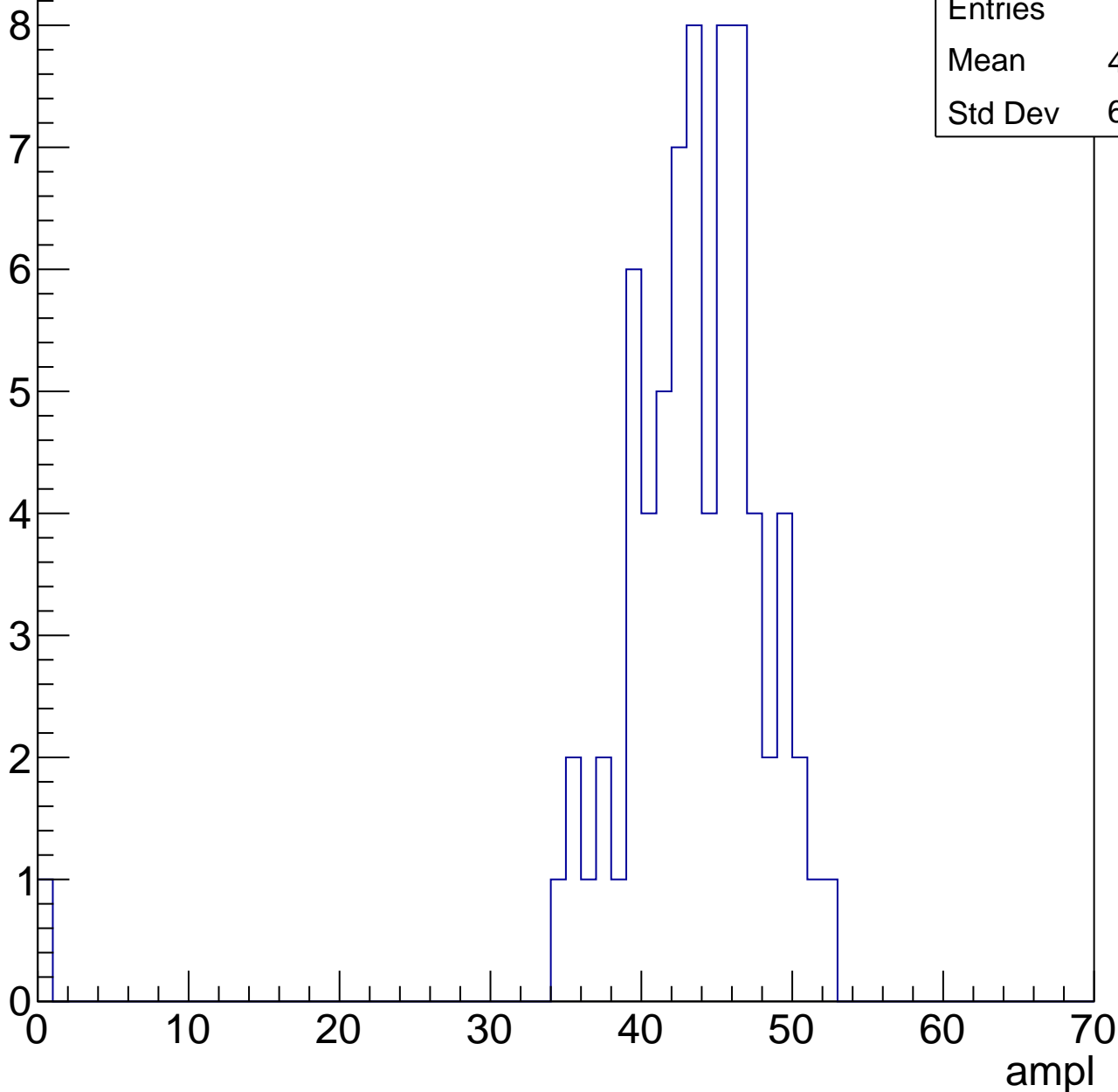


B1L103S, U23-ch81, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	72
Mean	42.72
Std Dev	6.419

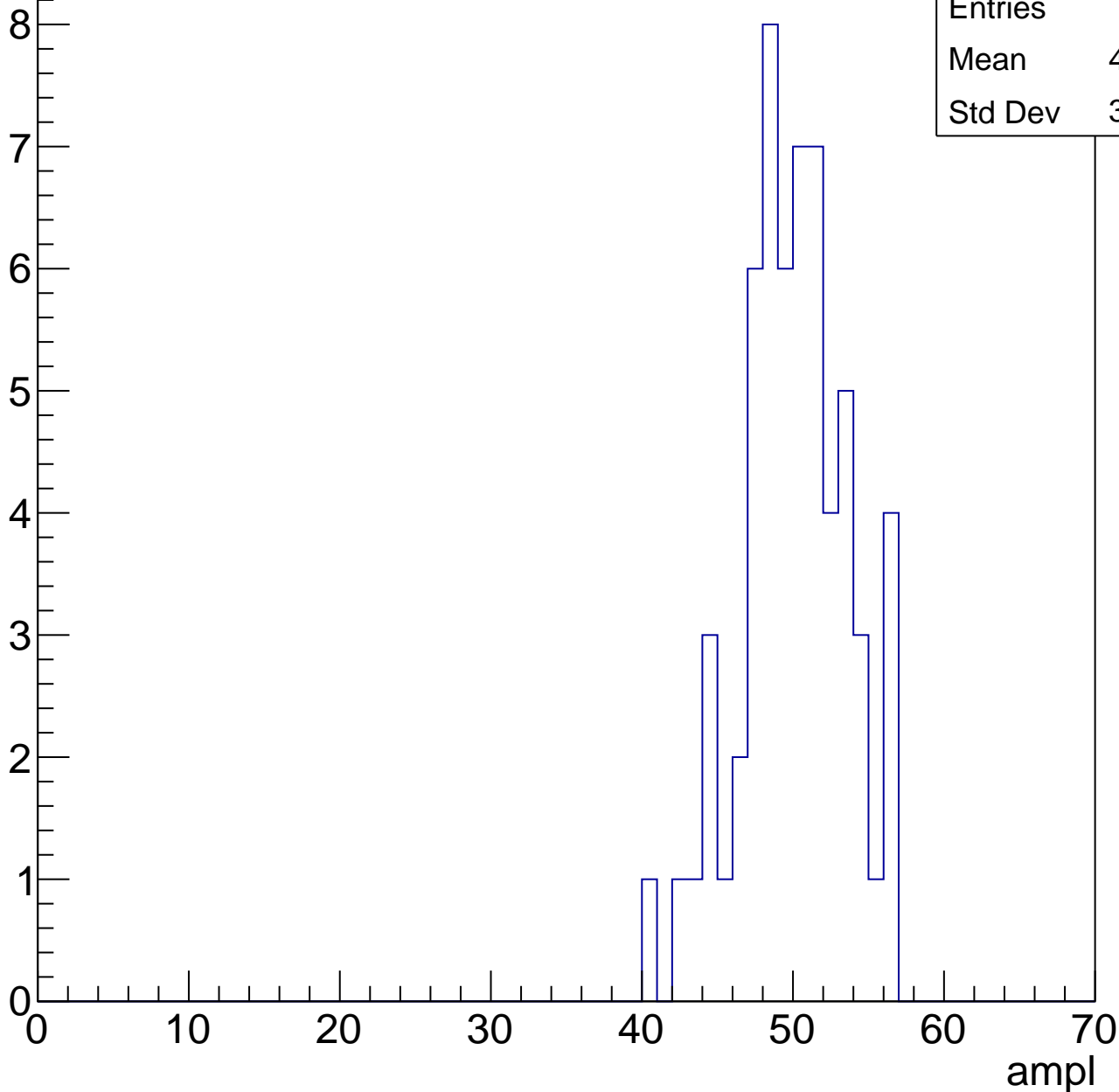


B1L103S, U23-ch81, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	49.58
Std Dev	3.523

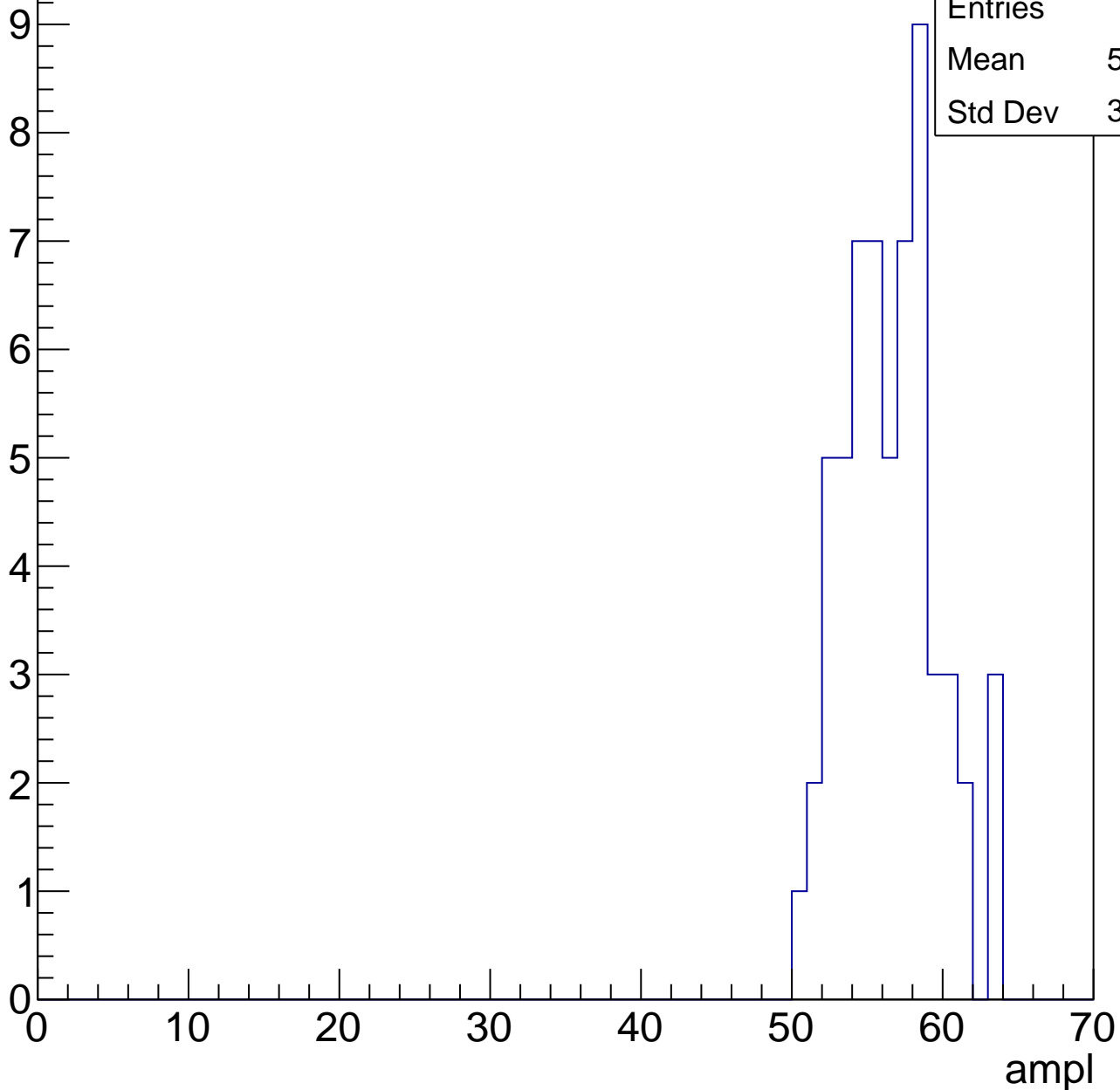


B1L103S, U23-ch81, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

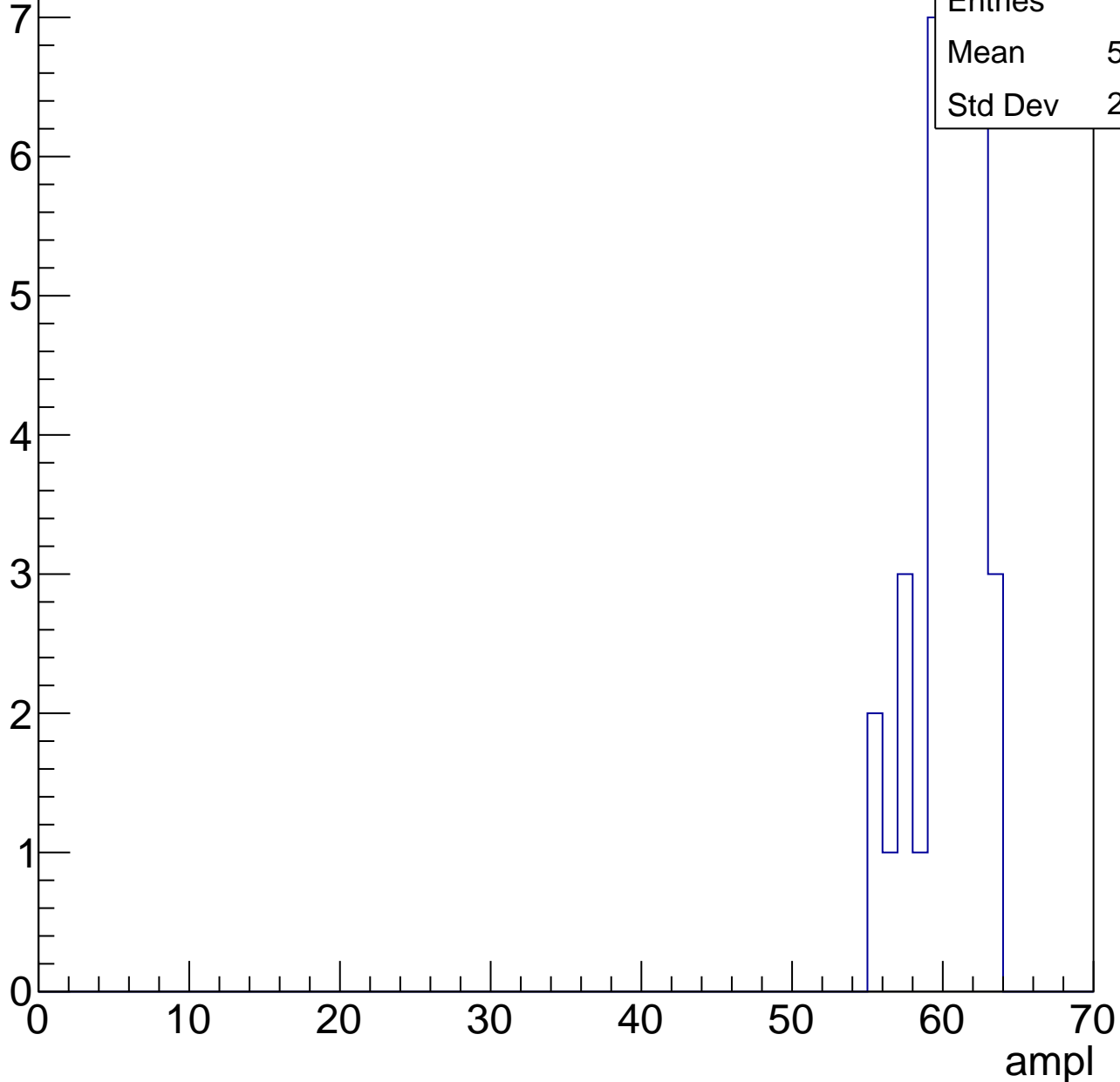
Entries	59
Mean	56.08
Std Dev	3.082



B1L103S, U23-ch81, adc5

calib_packv5_041523_1651.root, FC#0, port C2

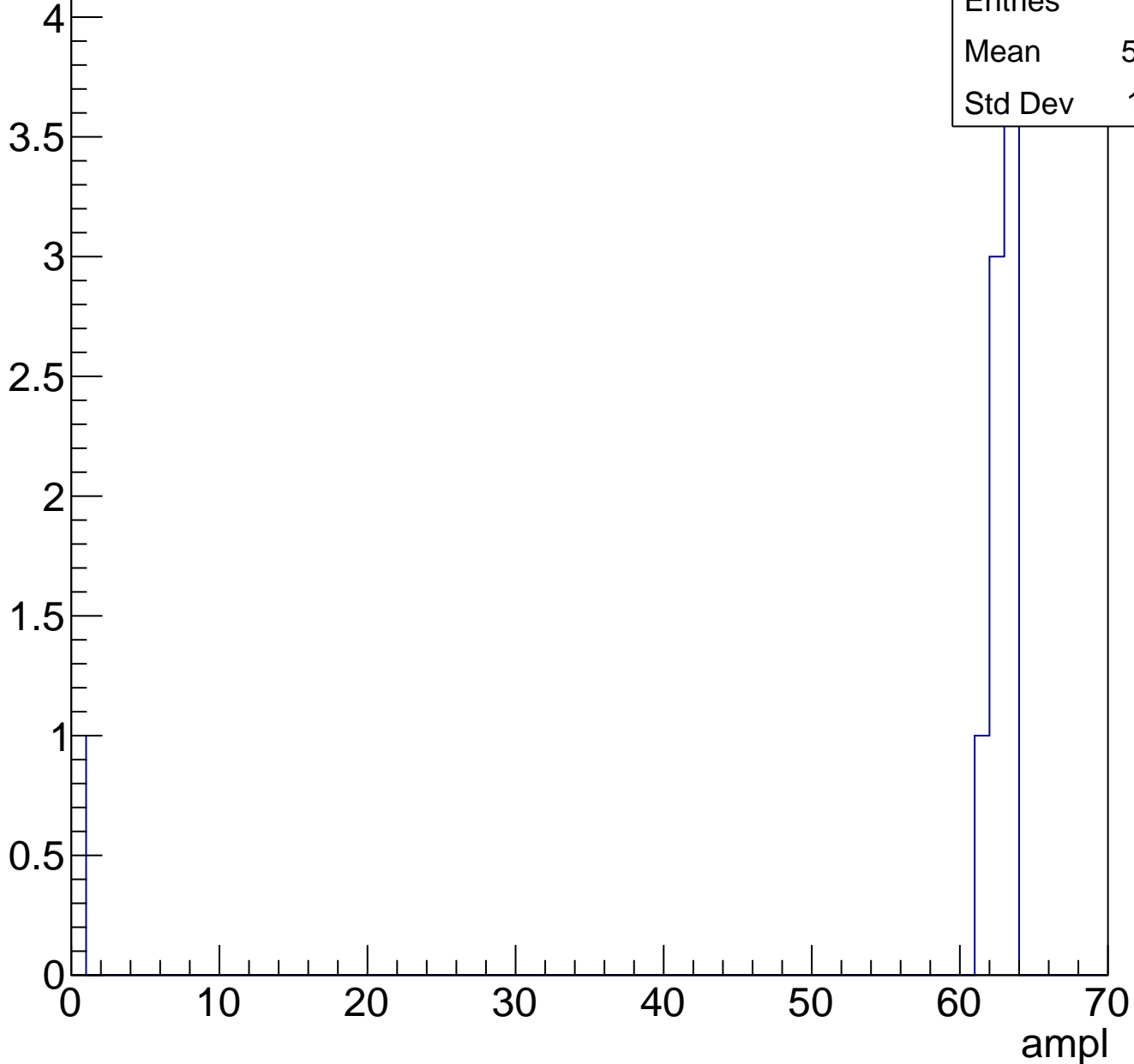
Entry



B1L103S, U23-ch81, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch81, adc7

calib_packv5_041523_1651.root, FC#0, port C2

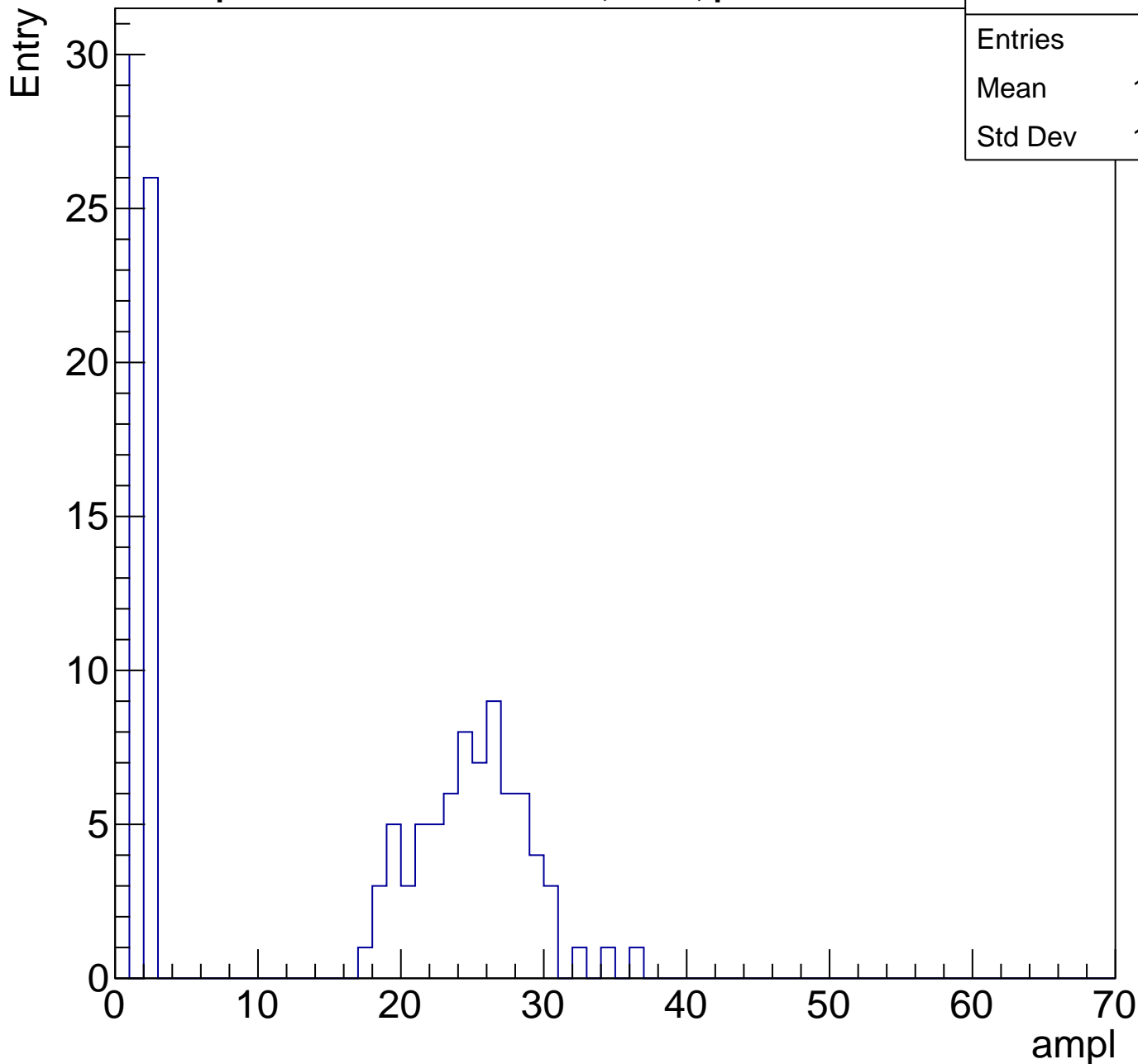
Entry



B1L103S, U23-ch82, adc0

calib_packv5_041523_1651.root, FC#0, port C2

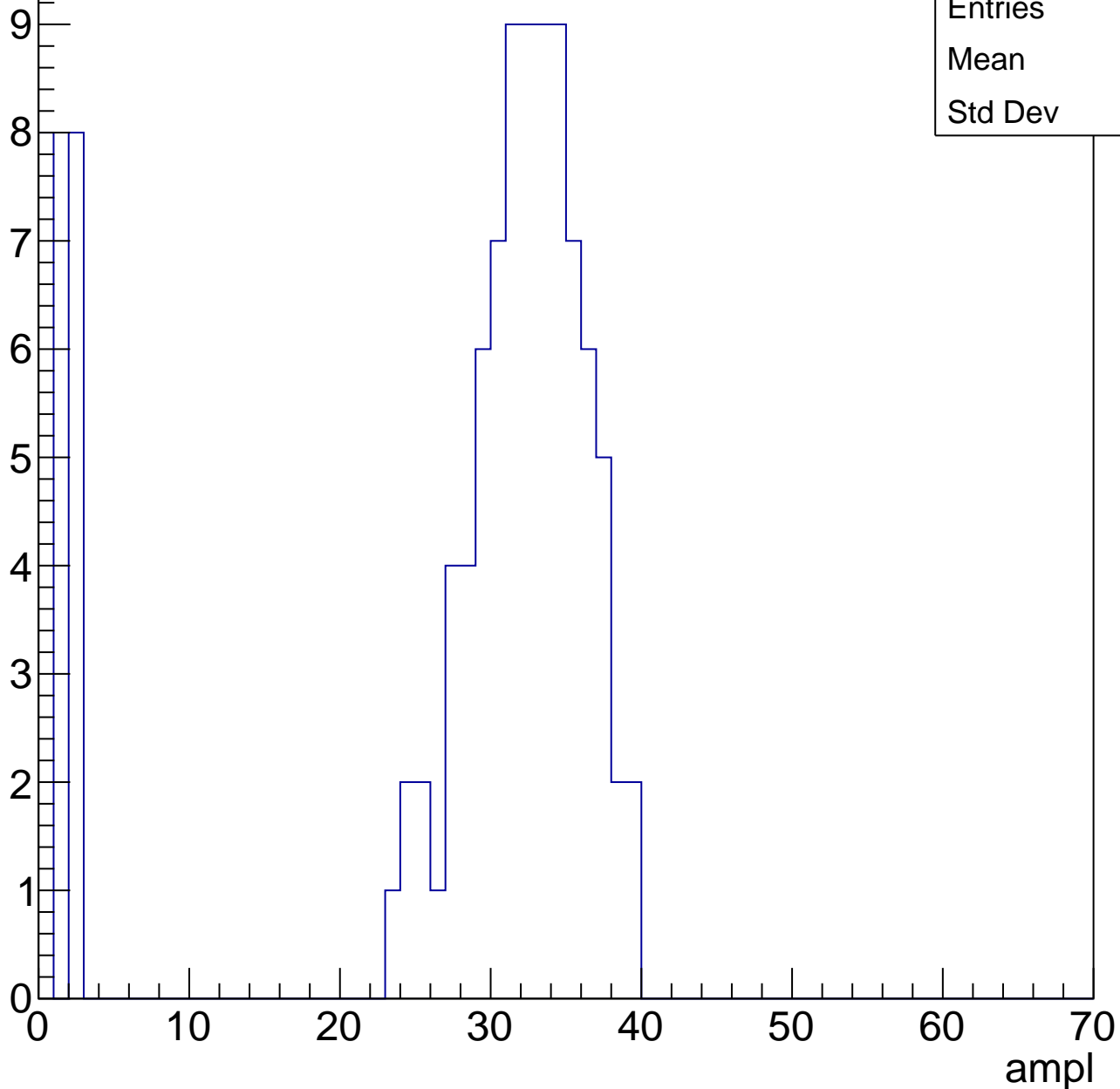
Entries	130
Mean	14.38
Std Dev	12.08



B1L103S, U23-ch82, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry



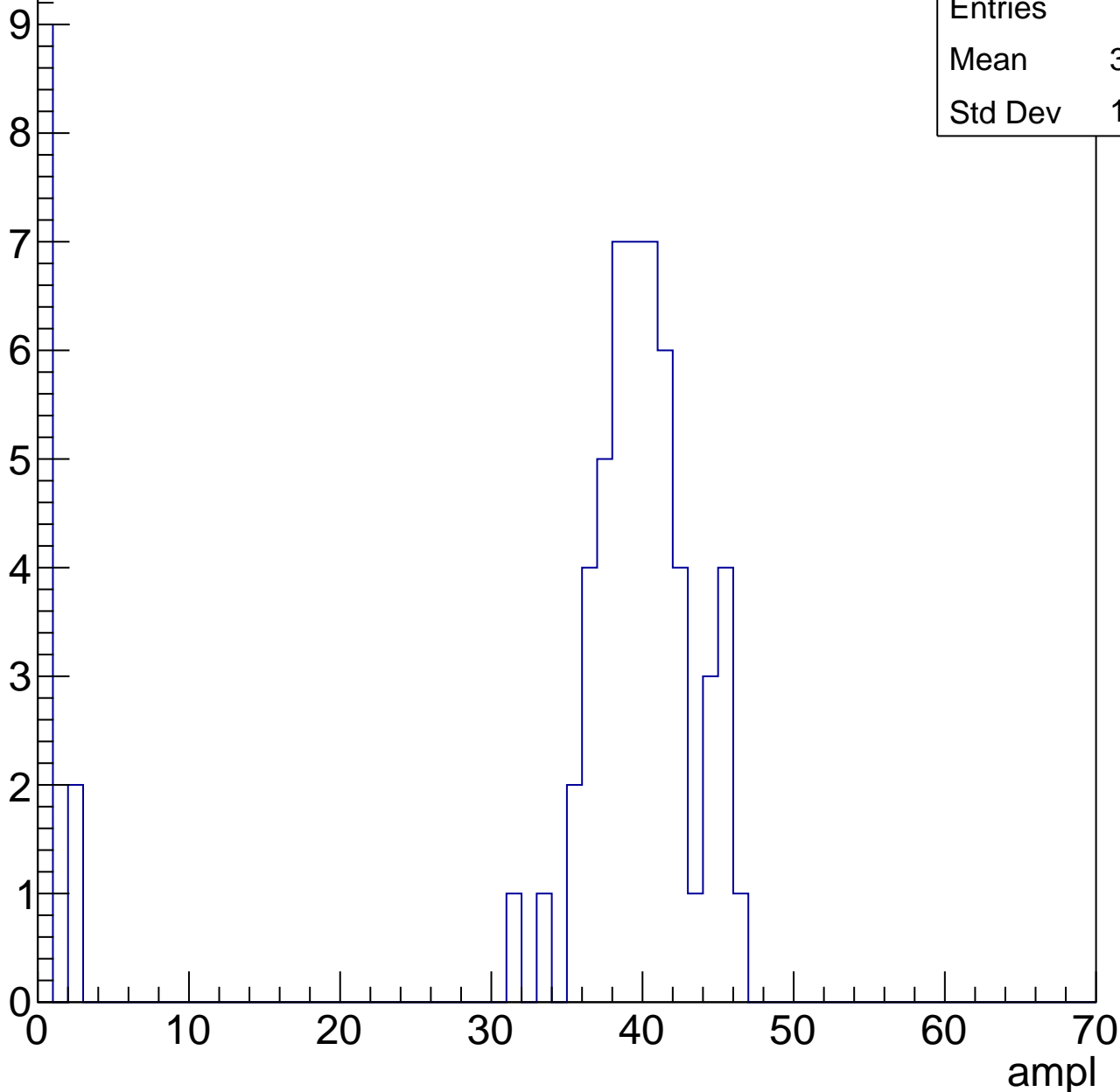
Entries	101
Mean	27.1
Std Dev	11.8

B1L103S, U23-ch82, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	32.83
Std Dev	15.07

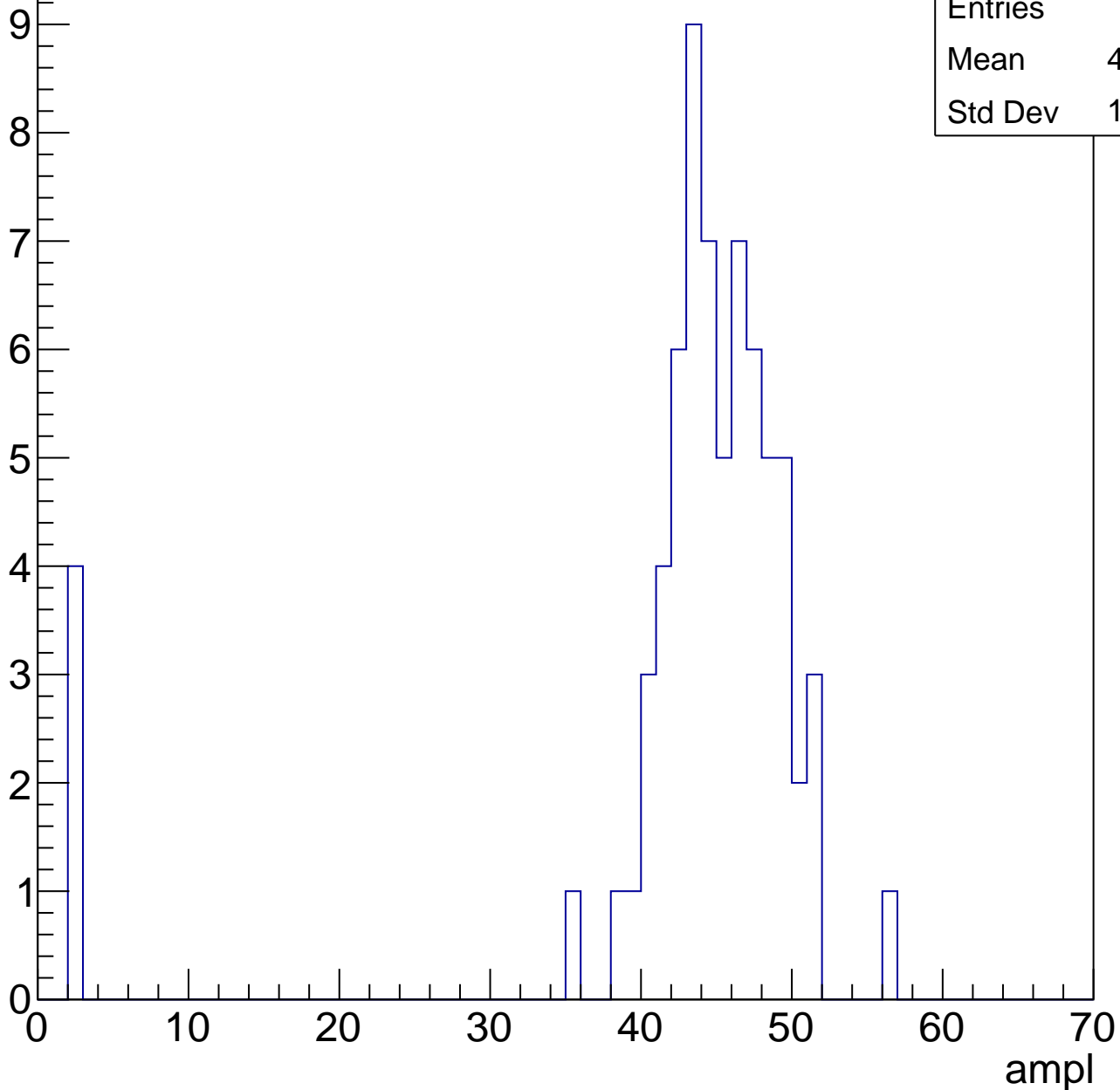


B1L103S, U23-ch82, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	42.49
Std Dev	10.56

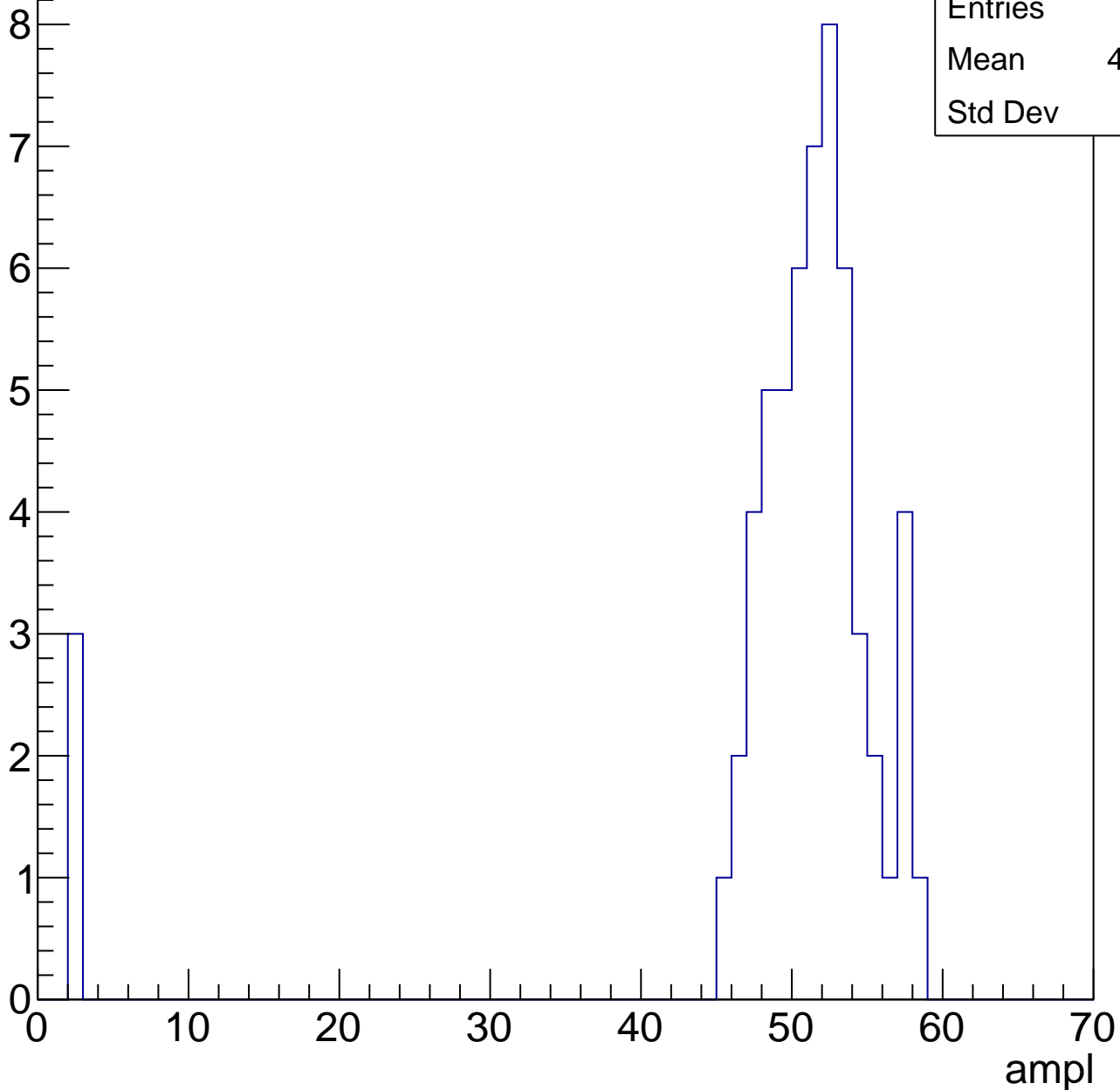


B1L103S, U23-ch82, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

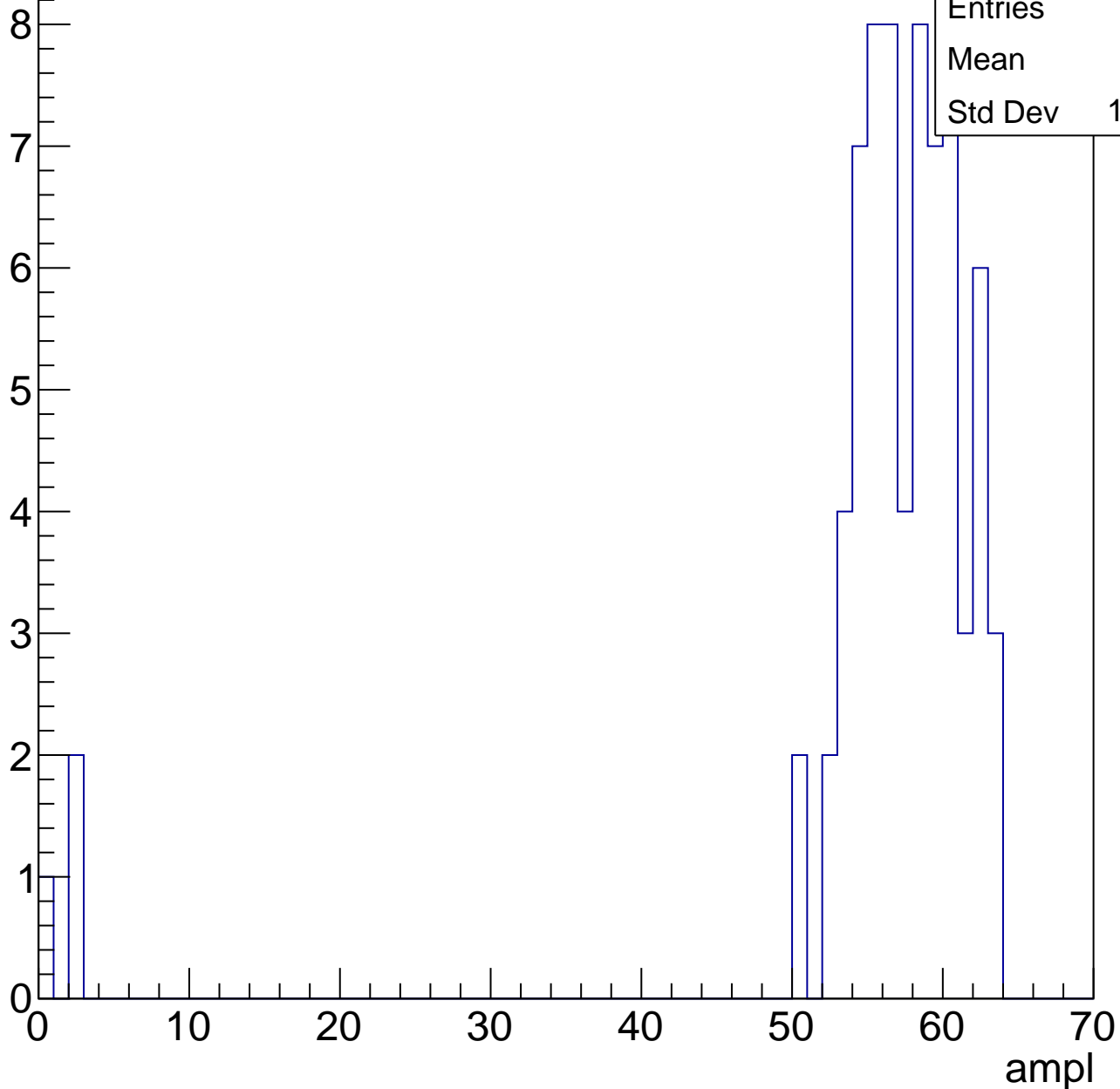
Entries	58
Mean	48.64
Std Dev	11.3



B1L103S, U23-ch82, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

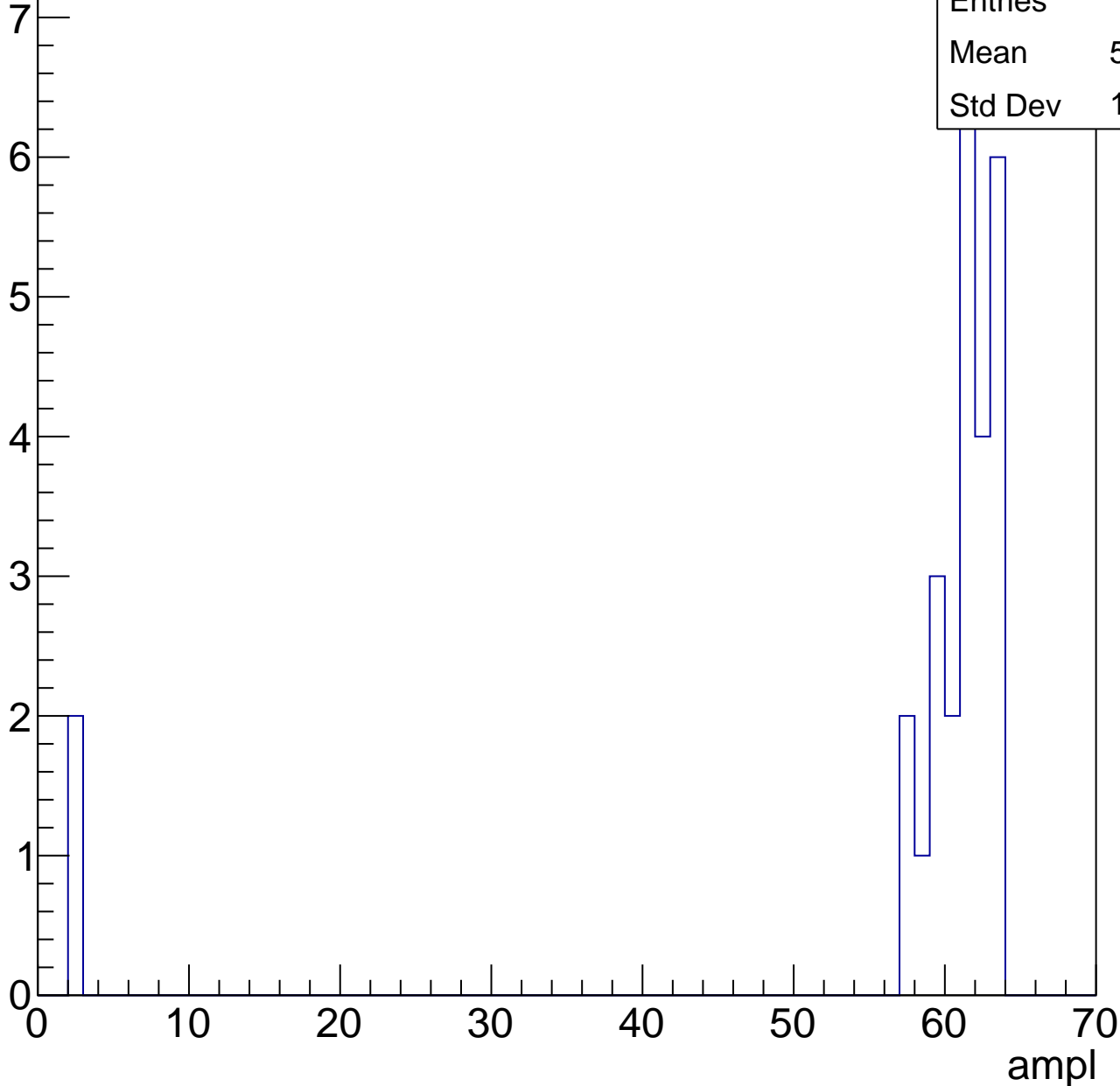


B1L103S, U23-ch82, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

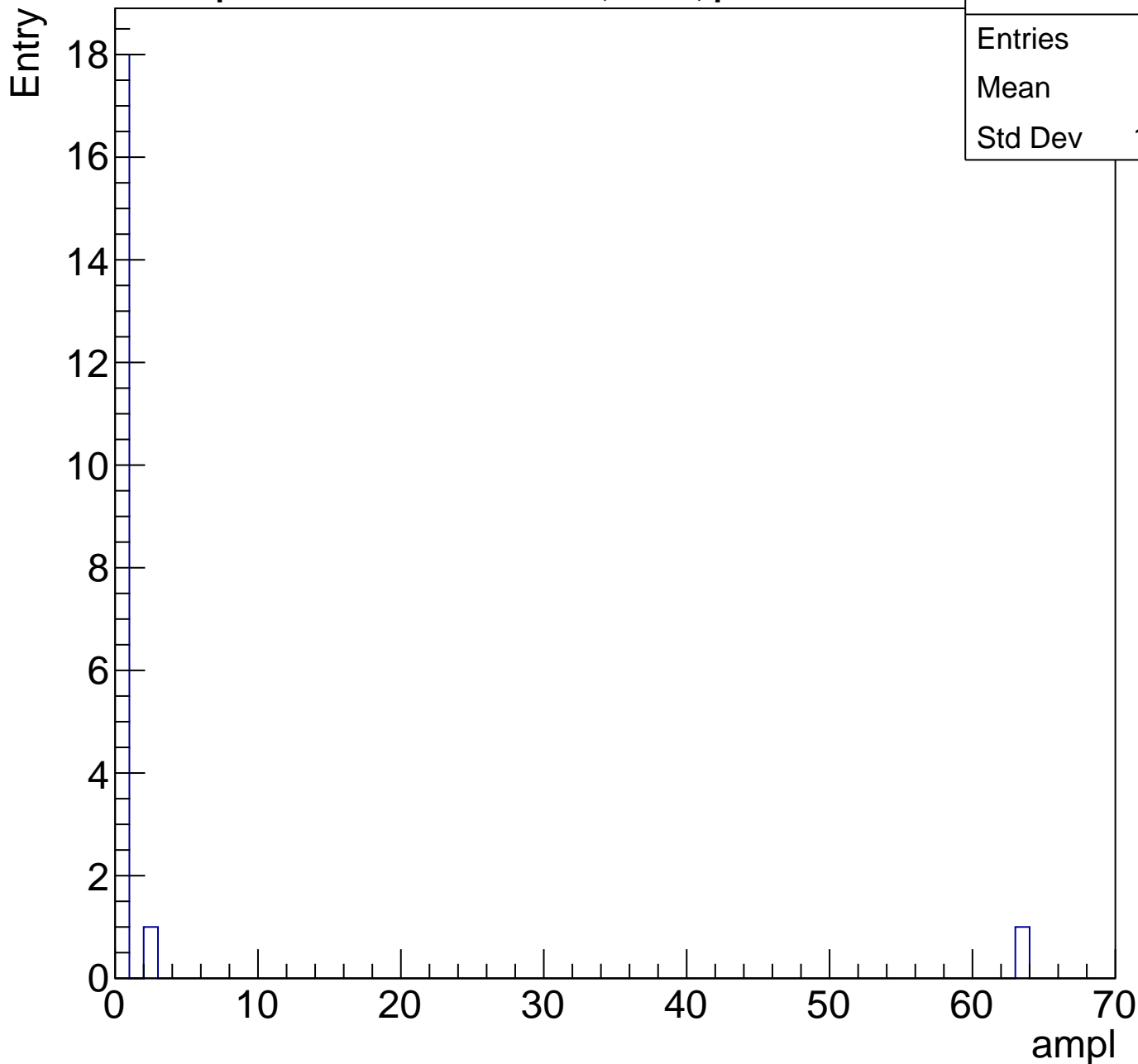
Entries	27
Mean	56.52
Std Dev	15.52



B1L103S, U23-ch82, adc7

calib_packv5_041523_1651.root, FC#0, port C2

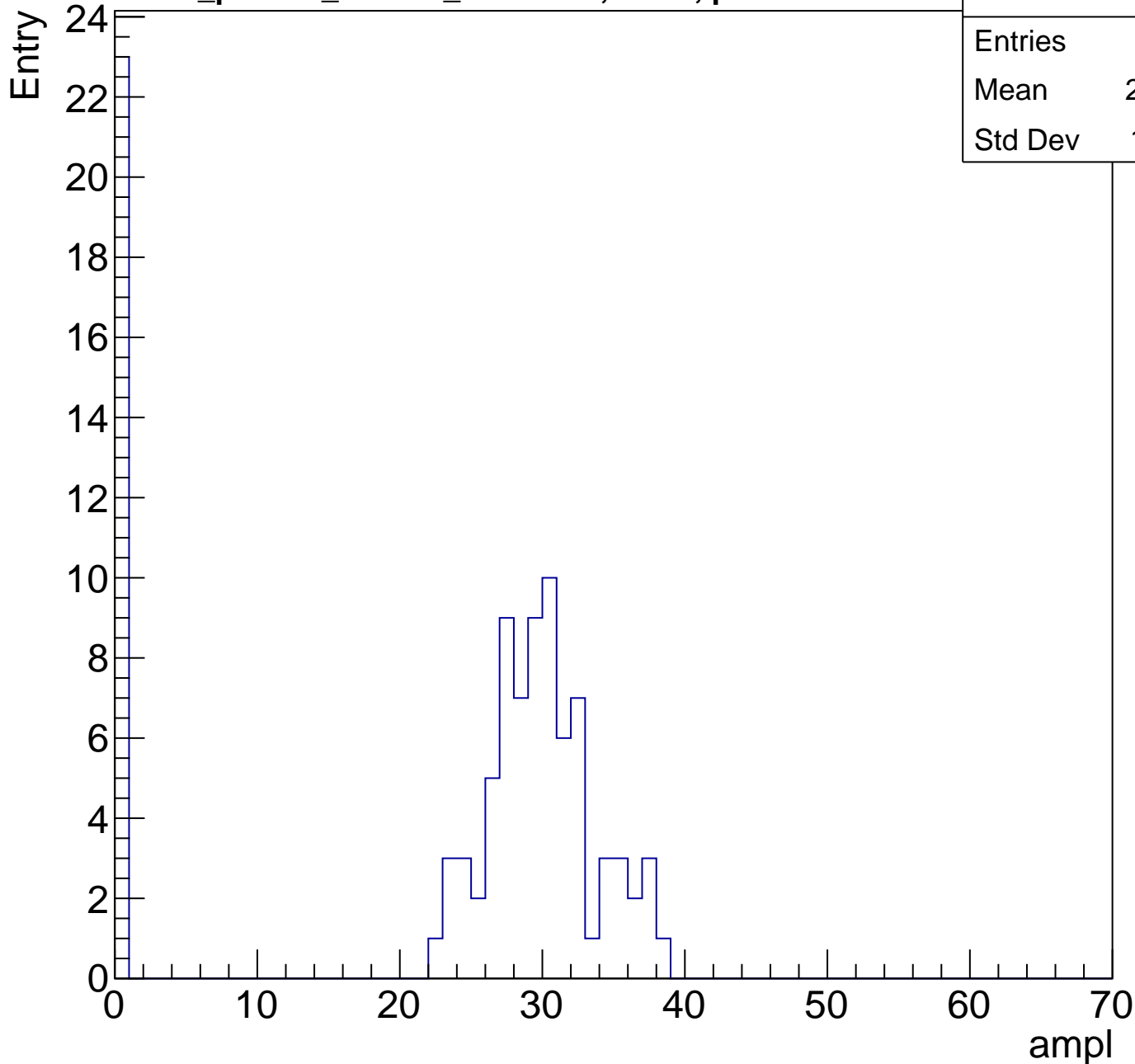
Entries	20
Mean	3.25
Std Dev	13.71



B1L103S, U23-ch83, adc0

calib_packv5_041523_1651.root, FC#0, port C2

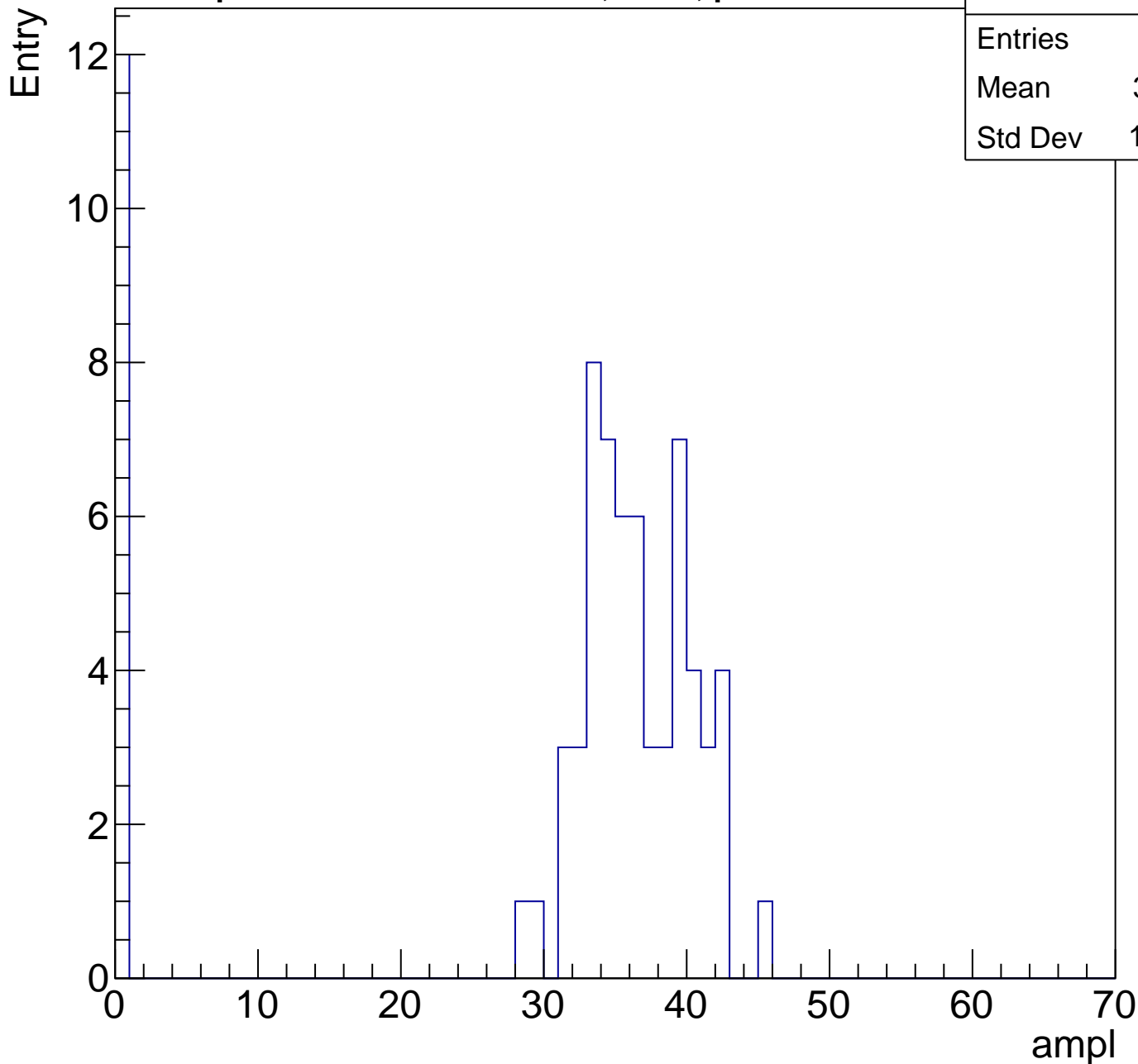
Entries	98
Mean	22.59
Std Dev	12.91



B1L103S, U23-ch83, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	72
Mean	30.11
Std Dev	13.86

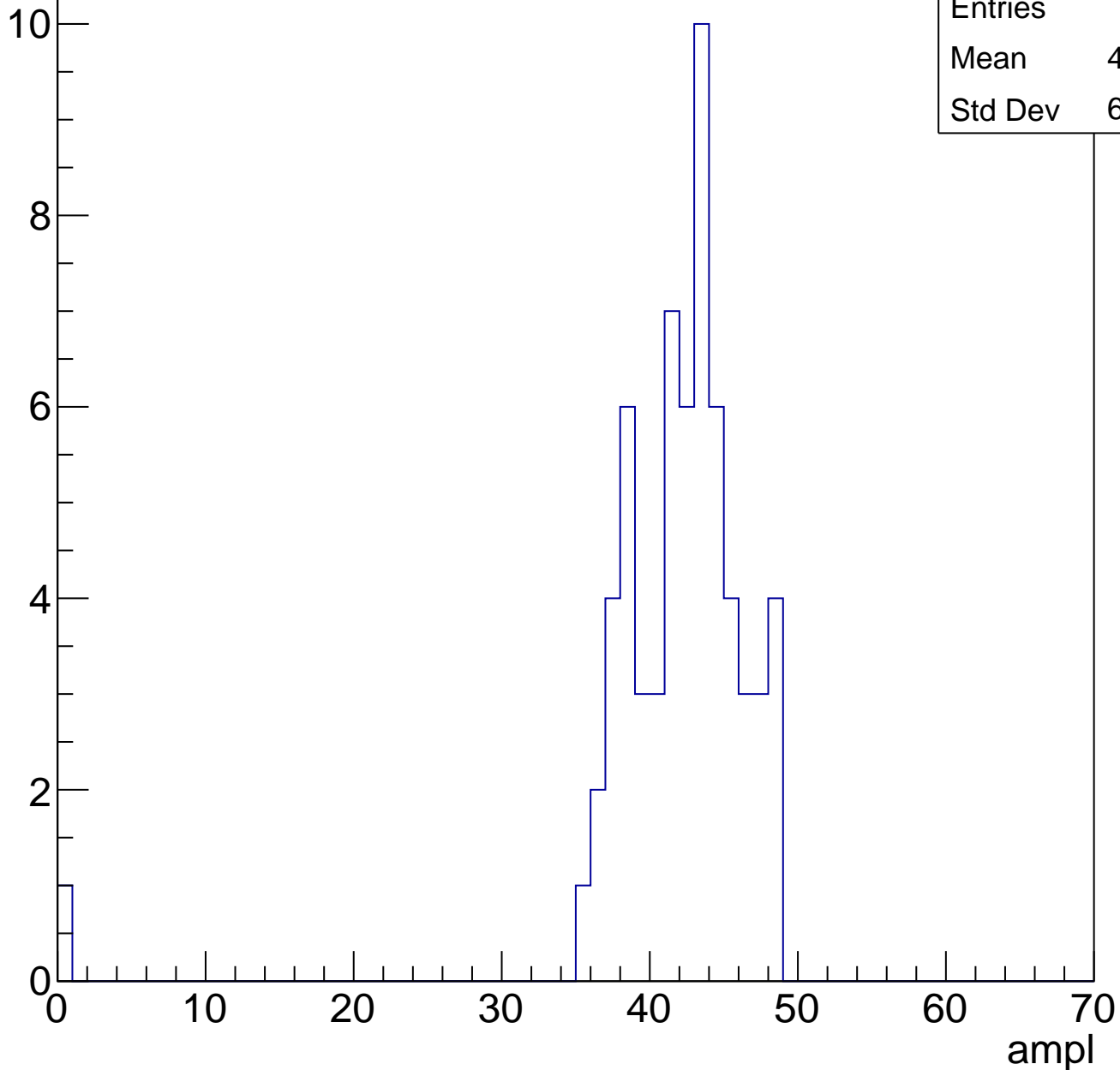


B1L103S, U23-ch83, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	63
Mean	41.33
Std Dev	6.218

Entry

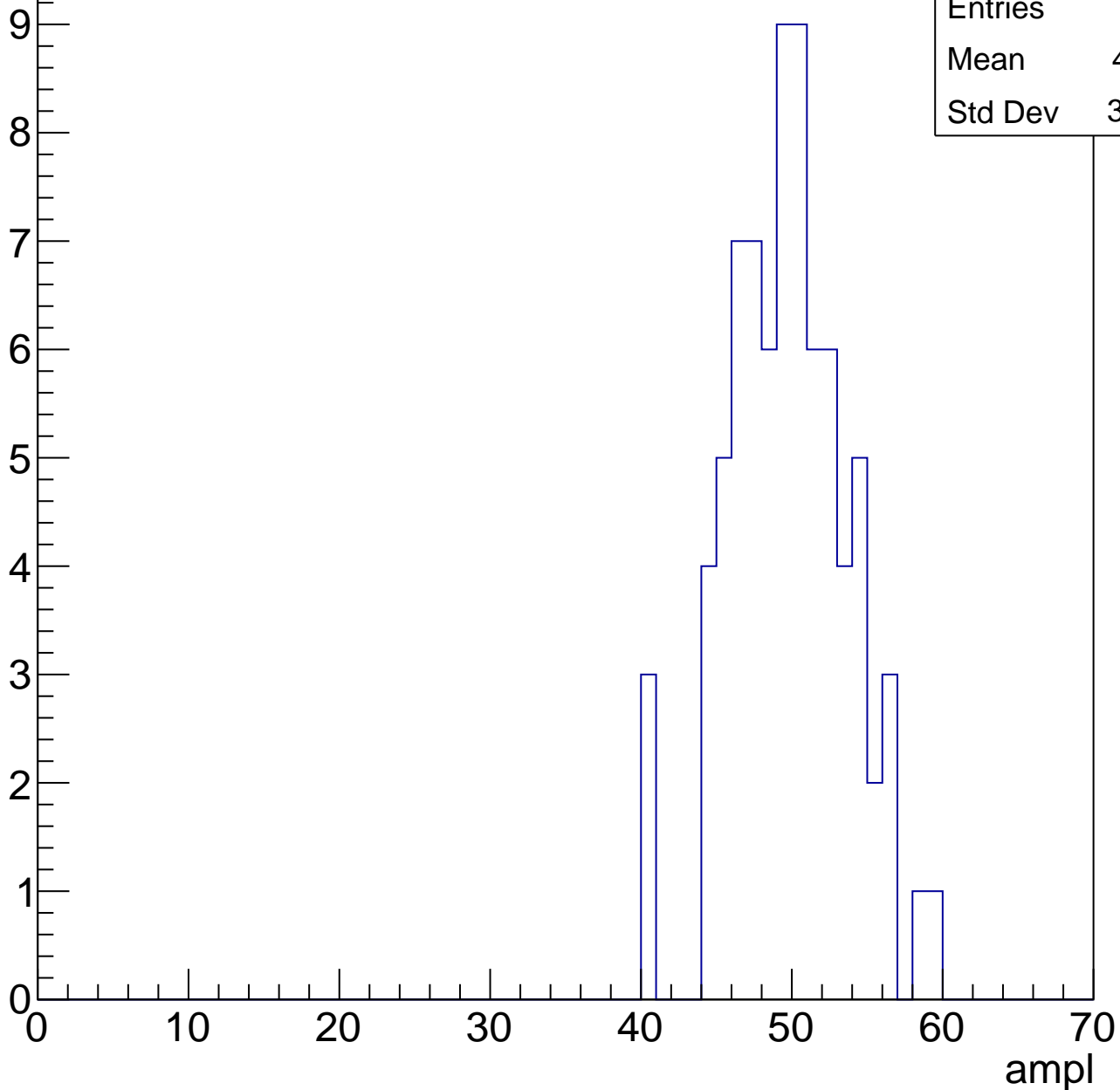


B1L103S, U23-ch83, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	78
Mean	49.31
Std Dev	3.904

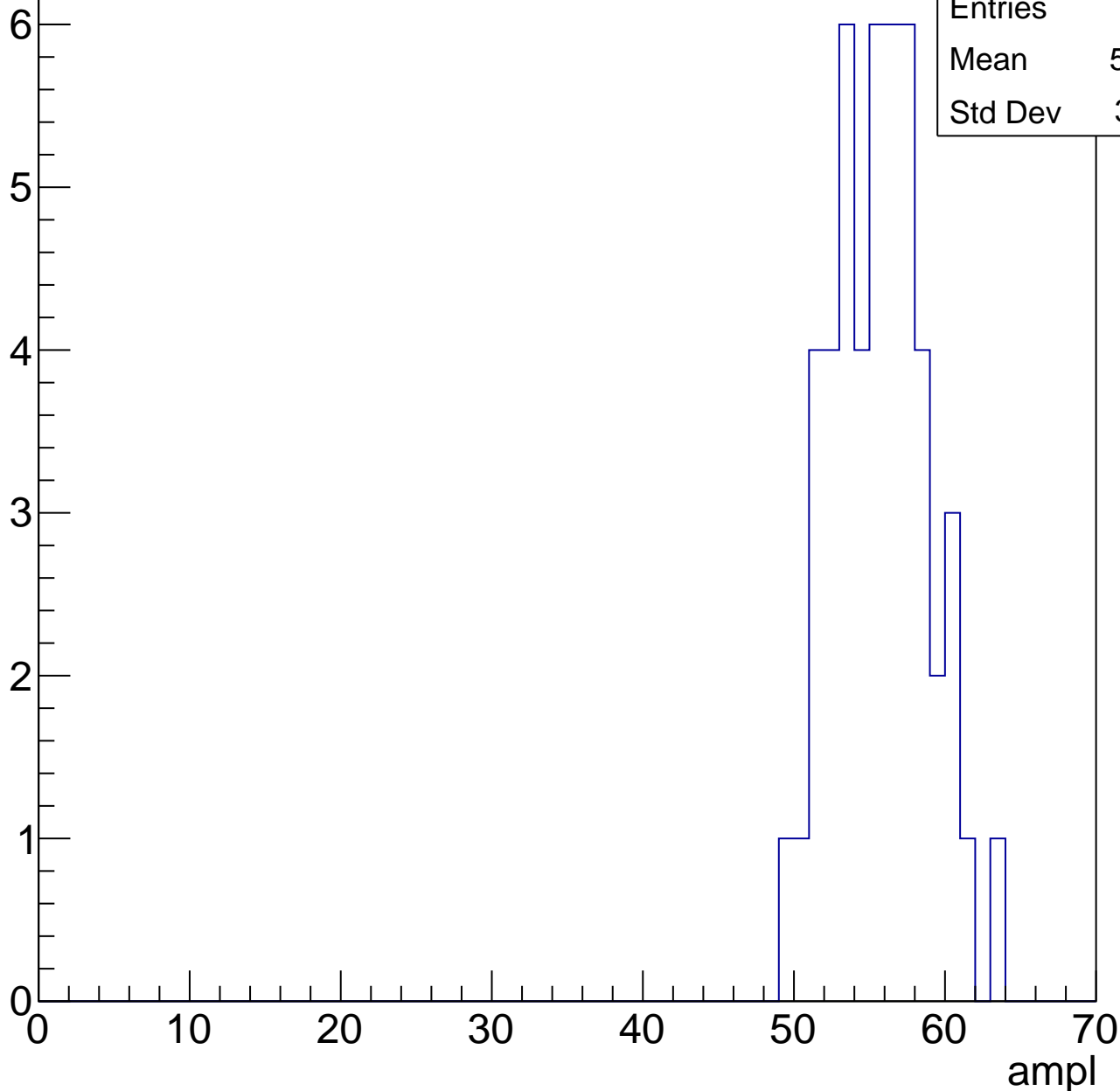


B1L103S, U23-ch83, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	49
Mean	55.24
Std Dev	3.061

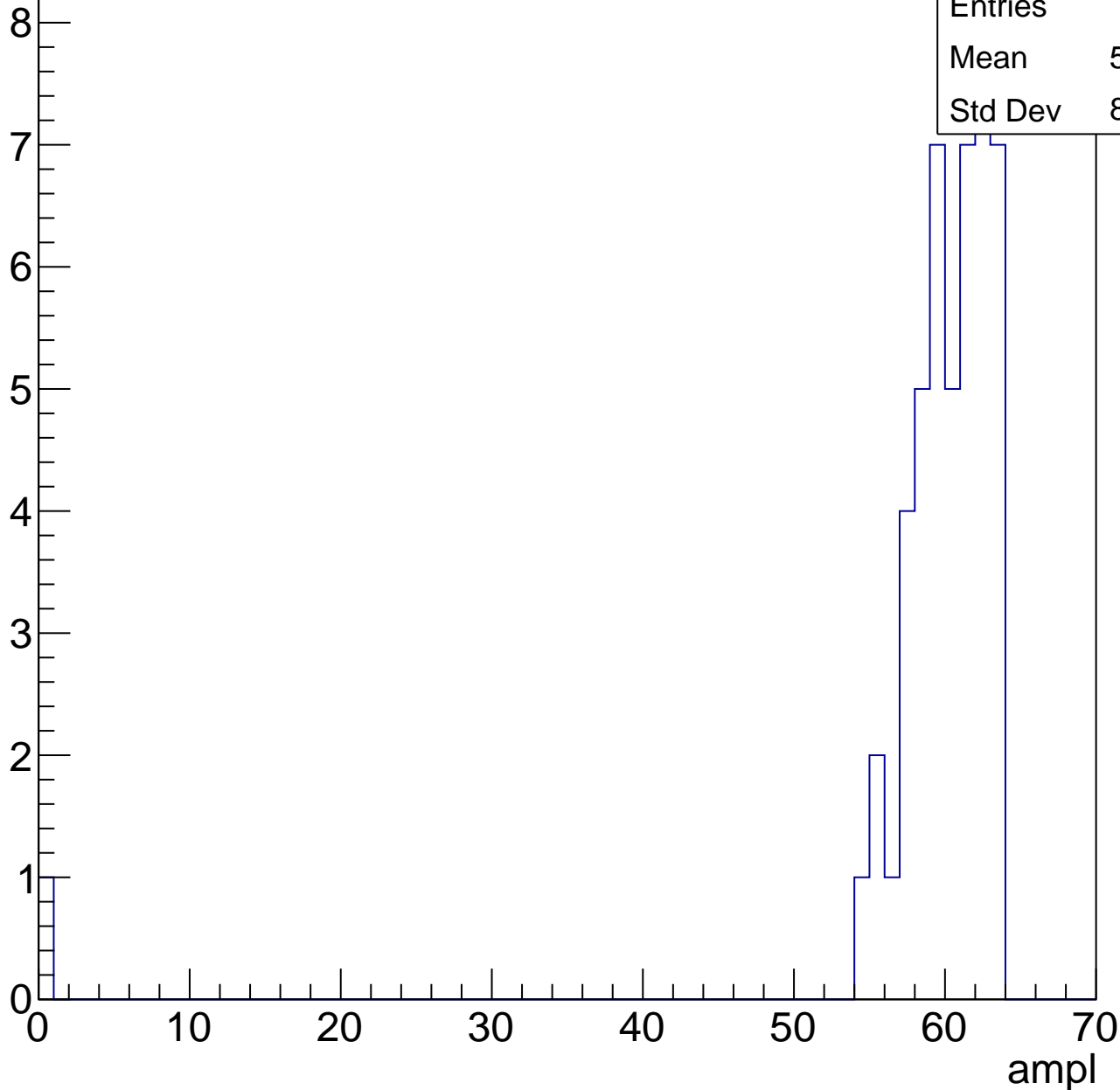


B1L103S, U23-ch83, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	48
Mean	58.65
Std Dev	8.873



B1L103S, U23-ch83, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

0 10 20 30 40 50 60 70

ampl

Entries	8
Mean	61.5
Std Dev	1.118

B1L103S, U23-ch83, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch84, adc0

calib_packv5_041523_1651.root, FC#0, port C2

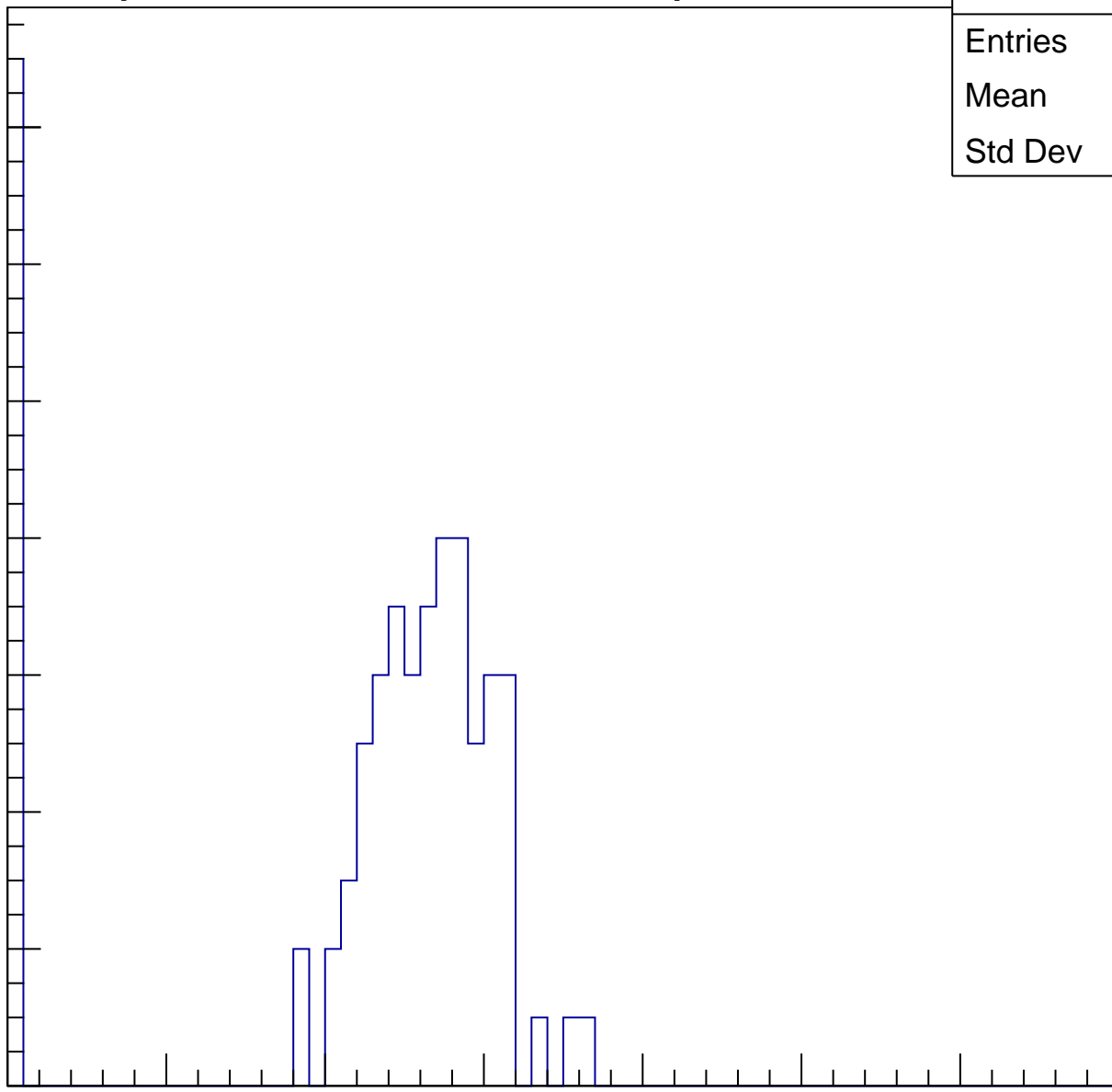
Entries	89
Mean	21.82
Std Dev	10.38

Entry

14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

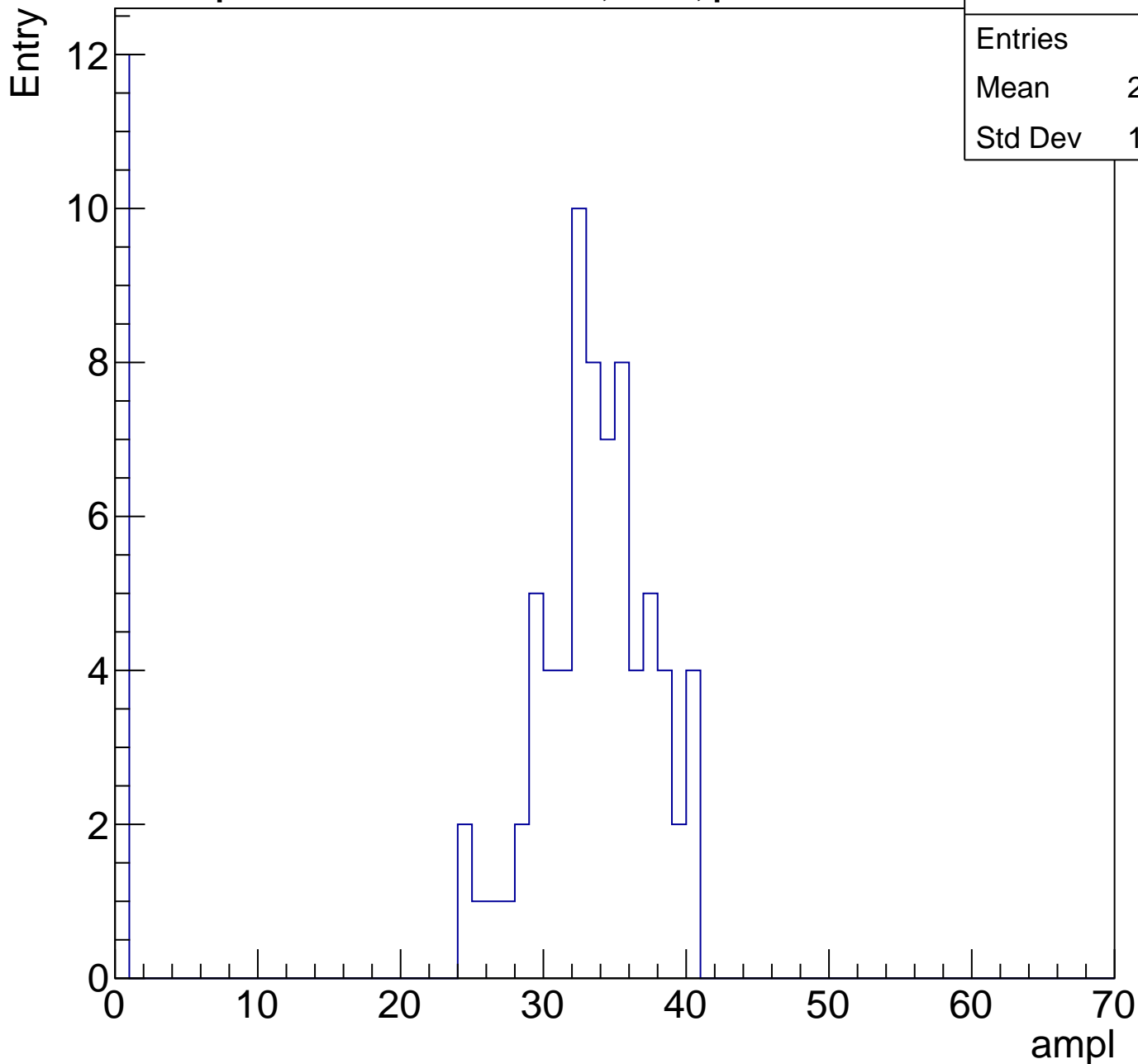
ampl



B1L103S, U23-ch84, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	84
Mean	28.48
Std Dev	12.14

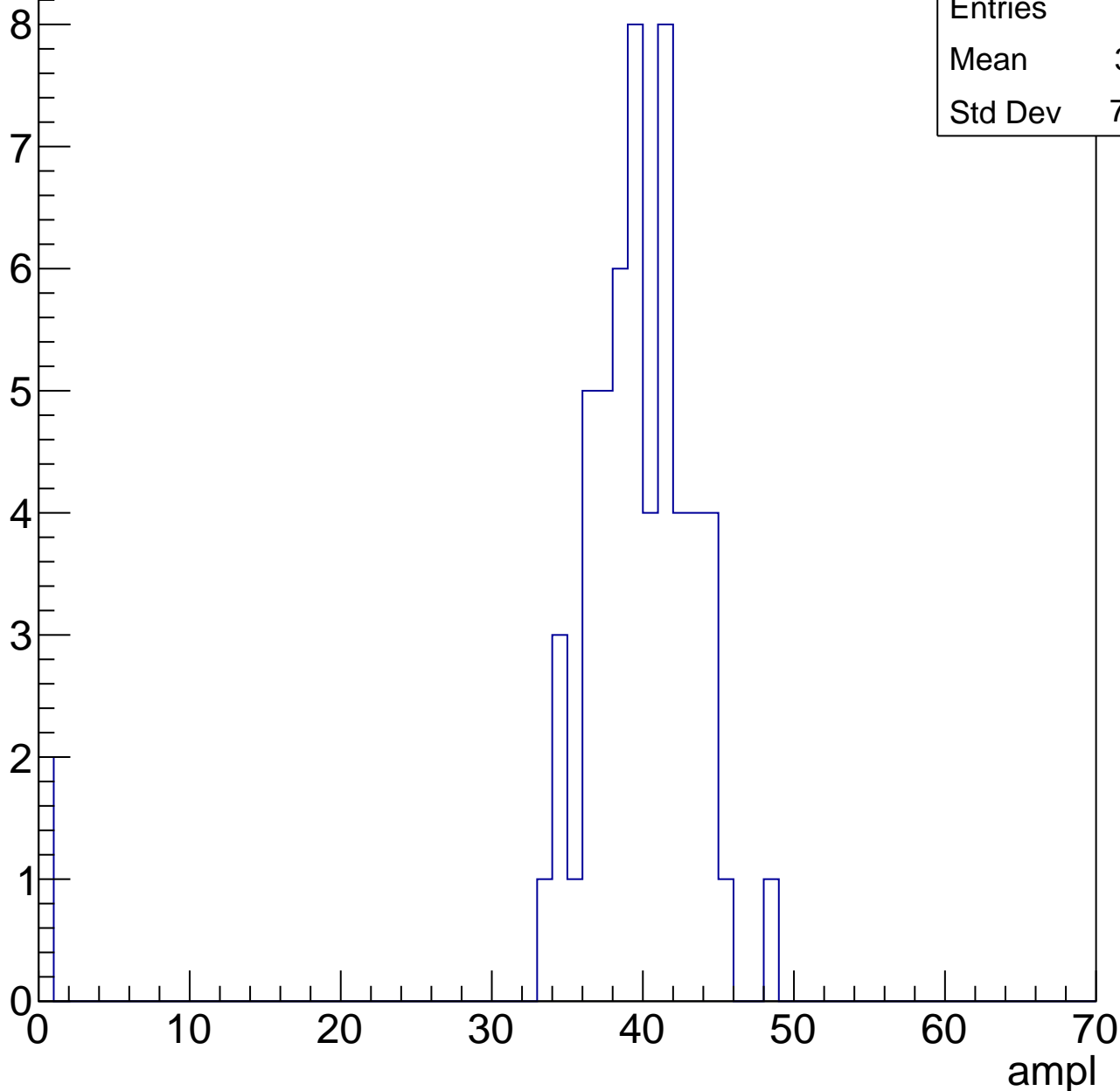


B1L103S, U23-ch84, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	57
Mean	38.11
Std Dev	7.889

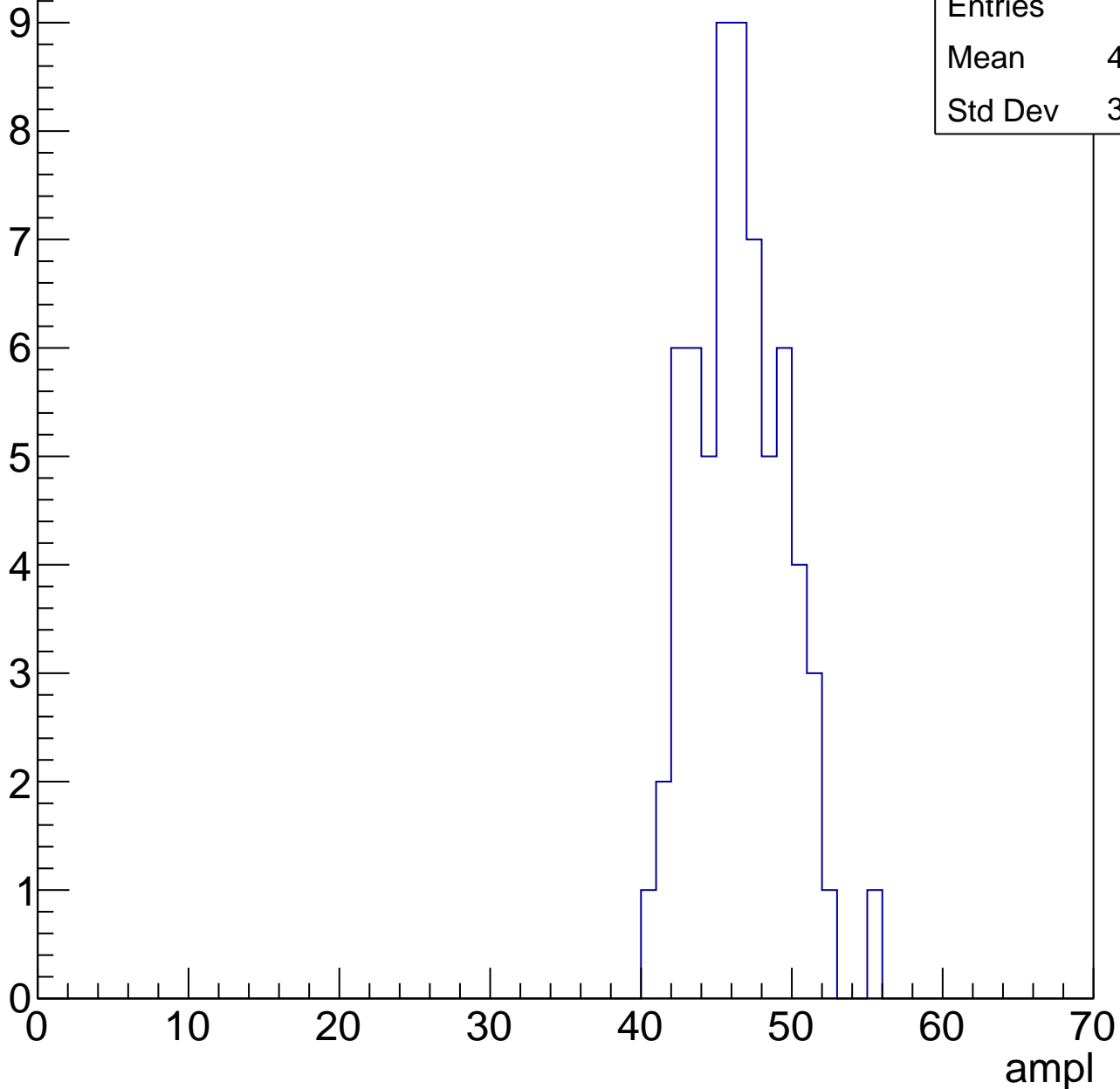


B1L103S, U23-ch84, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	46.06
Std Dev	3.043

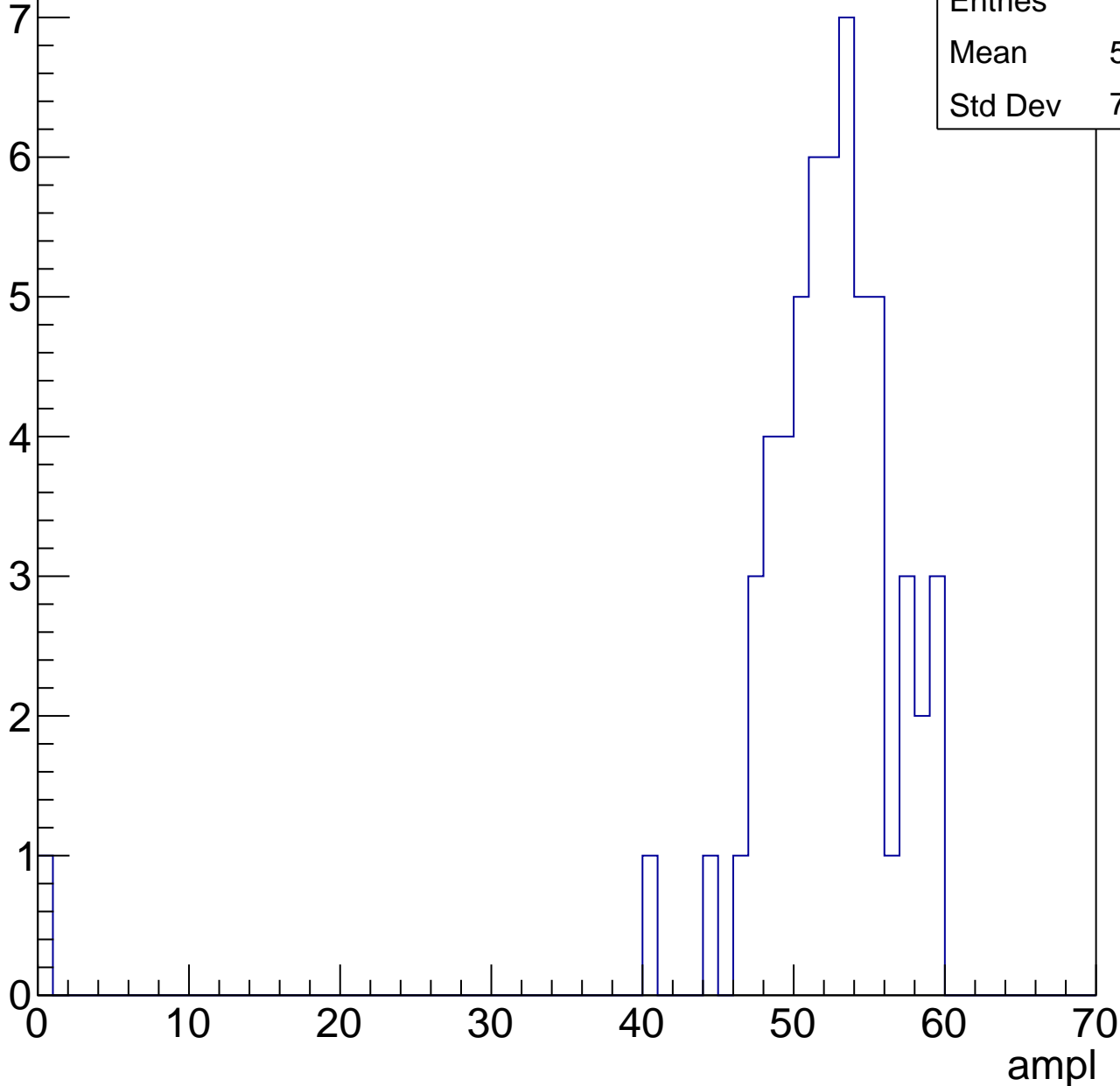


B1L103S, U23-ch84, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

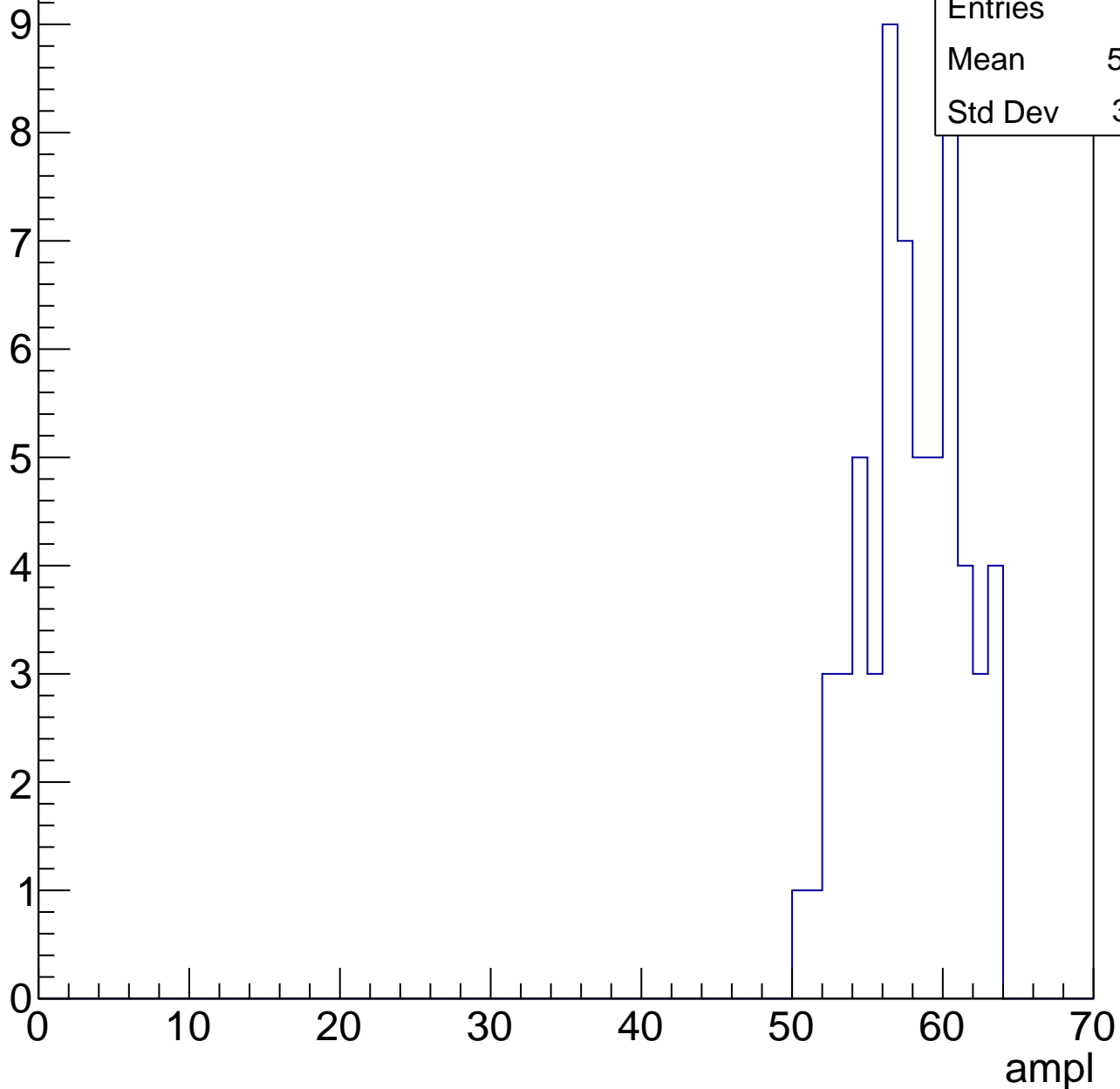
Entries	58
Mean	51.09
Std Dev	7.749



B1L103S, U23-ch84, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



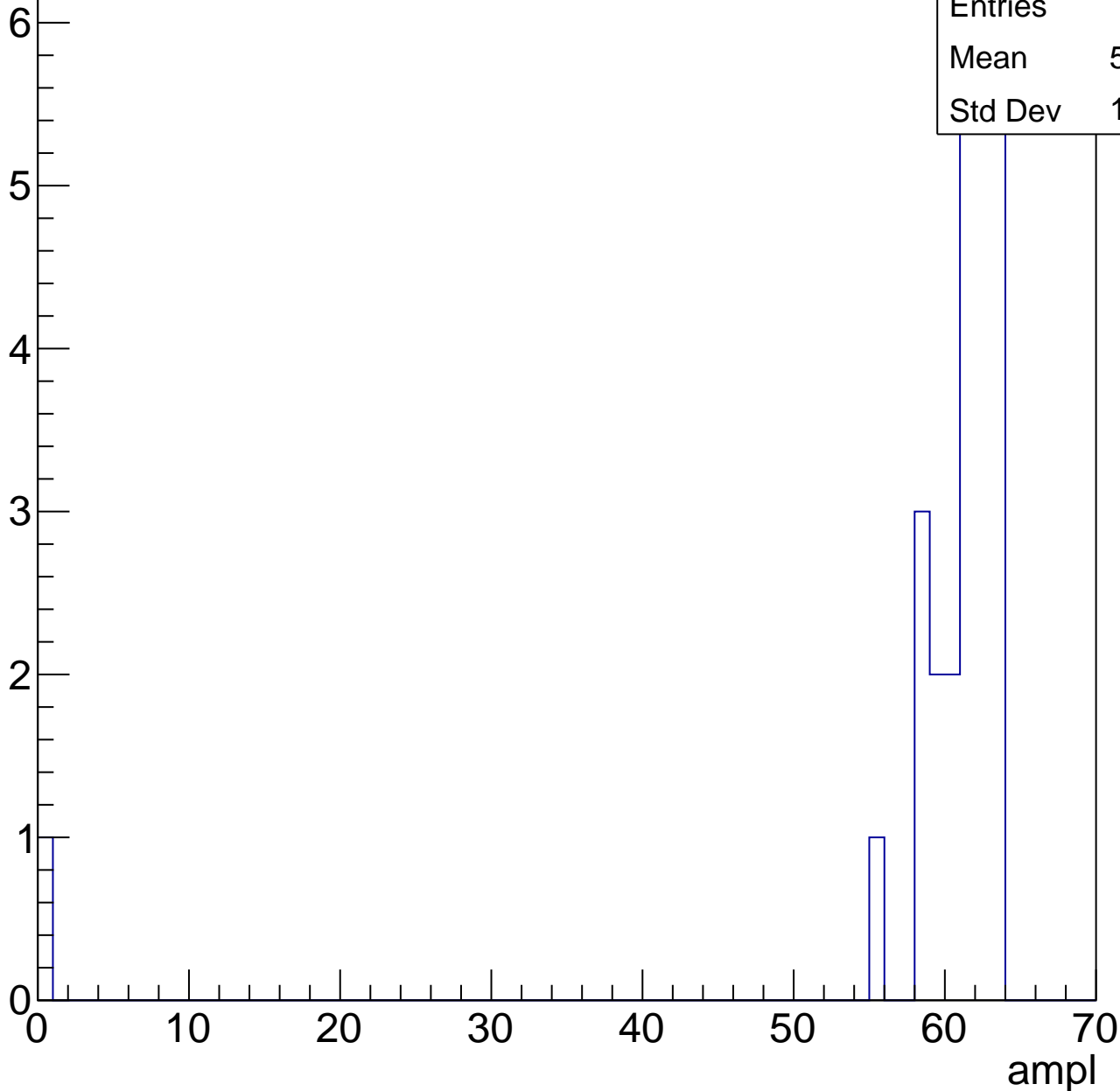
Entries	61
Mean	57.39
Std Dev	3.251

B1L103S, U23-ch84, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	27
Mean	58.63
Std Dev	11.66



B1L103S, U23-ch84, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.1
Std Dev	13.51

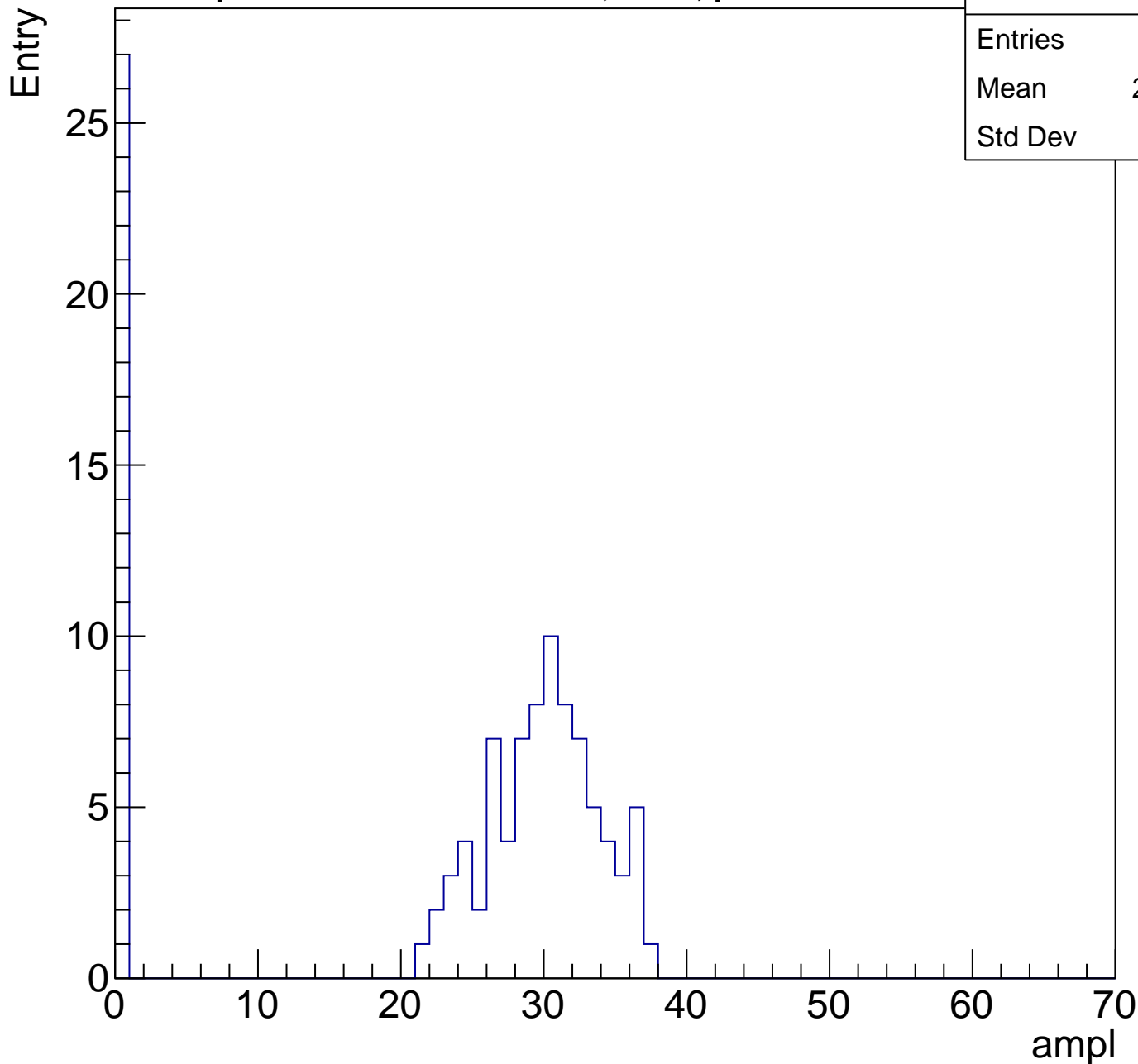
Entry



B1L103S, U23-ch85, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	108
Mean	22.16
Std Dev	13.21

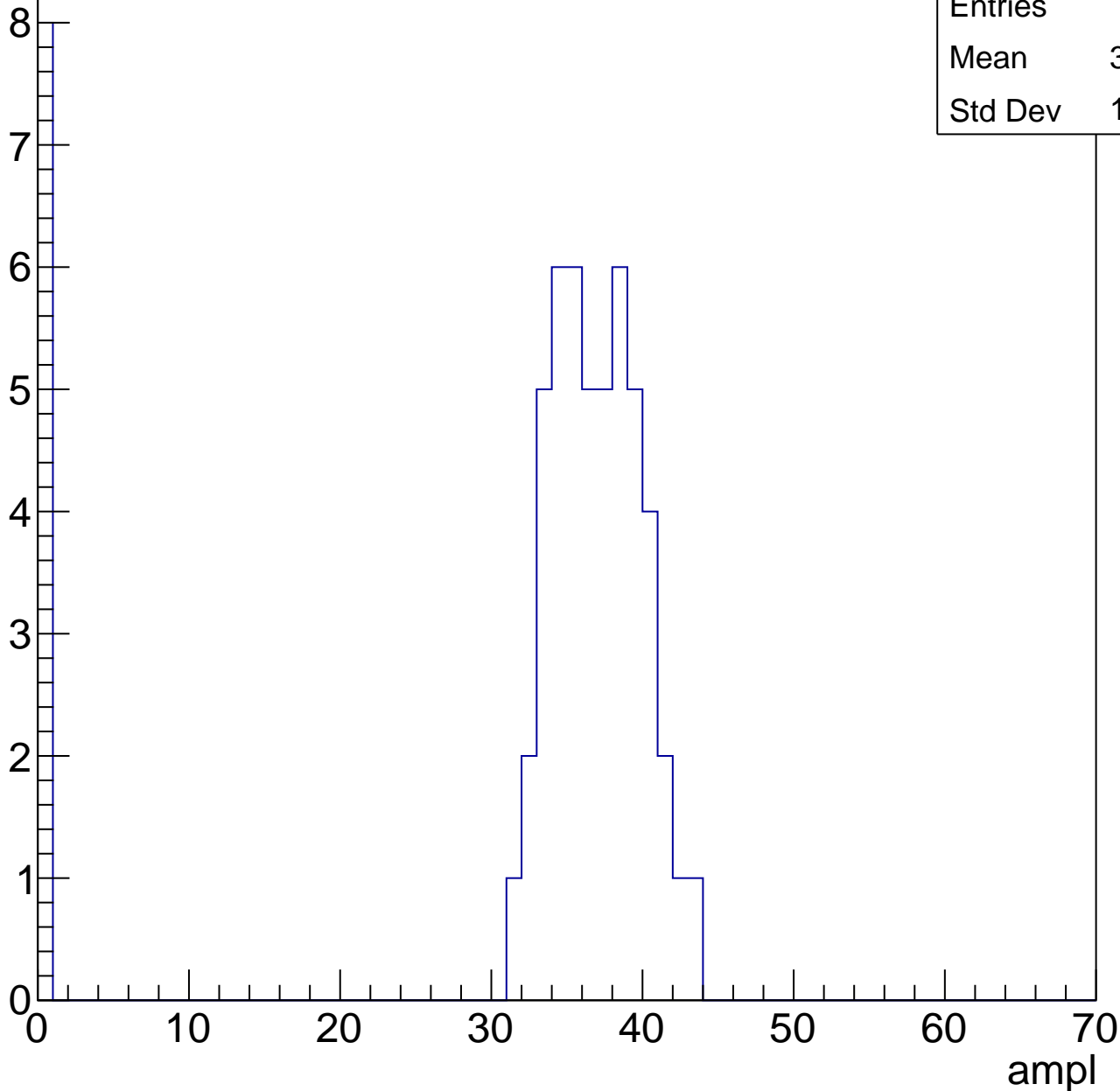


B1L103S, U23-ch85, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	57
Mean	31.39
Std Dev	12.95

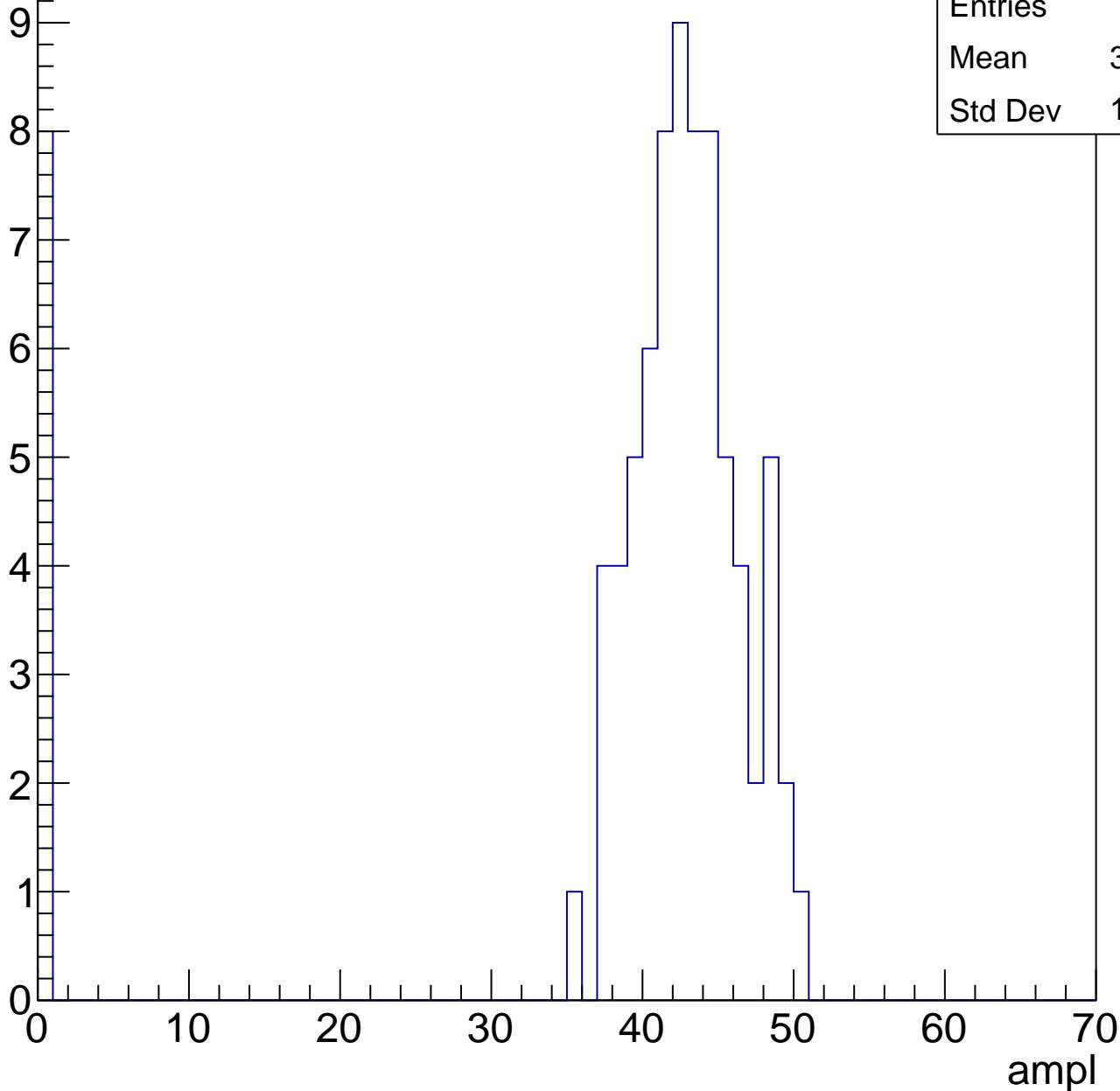


B1L103S, U23-ch85, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	80
Mean	38.29
Std Dev	13.15

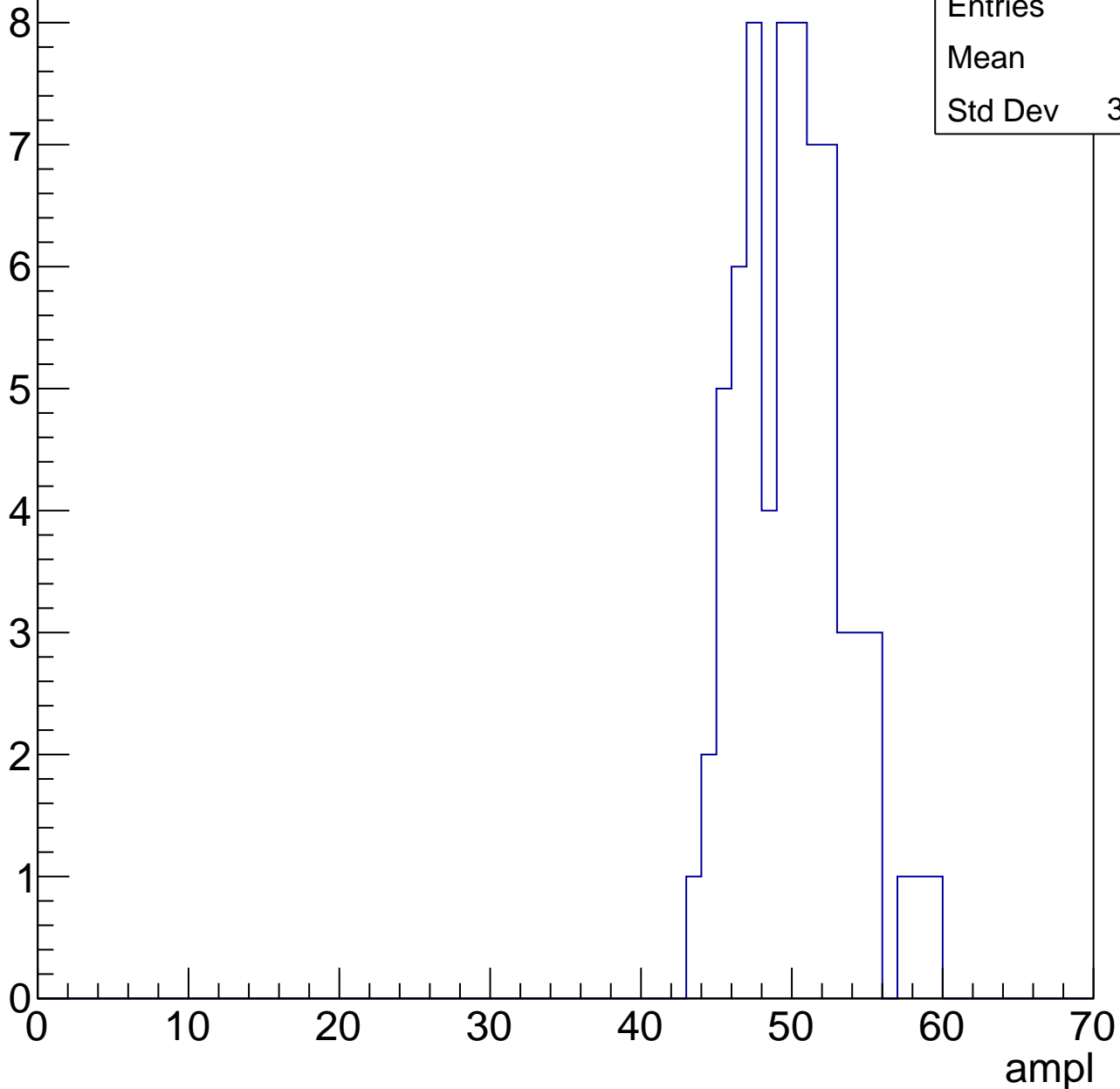


B1L103S, U23-ch85, adc3

calib_packv5_041523_1651.root, FC#0, port C2

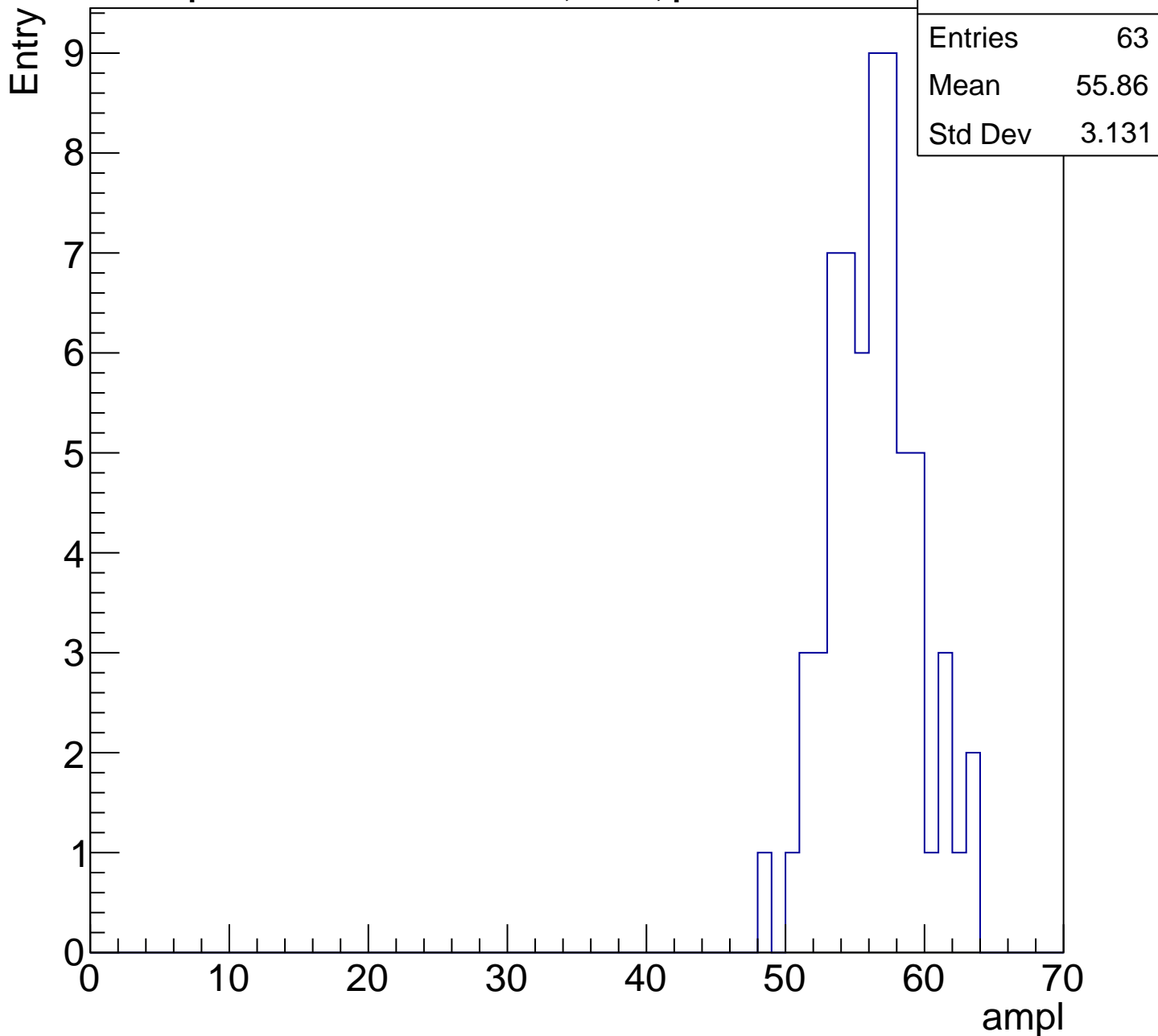
Entry

Entries	68
Mean	49.6
Std Dev	3.443



B1L103S, U23-ch85, adc4

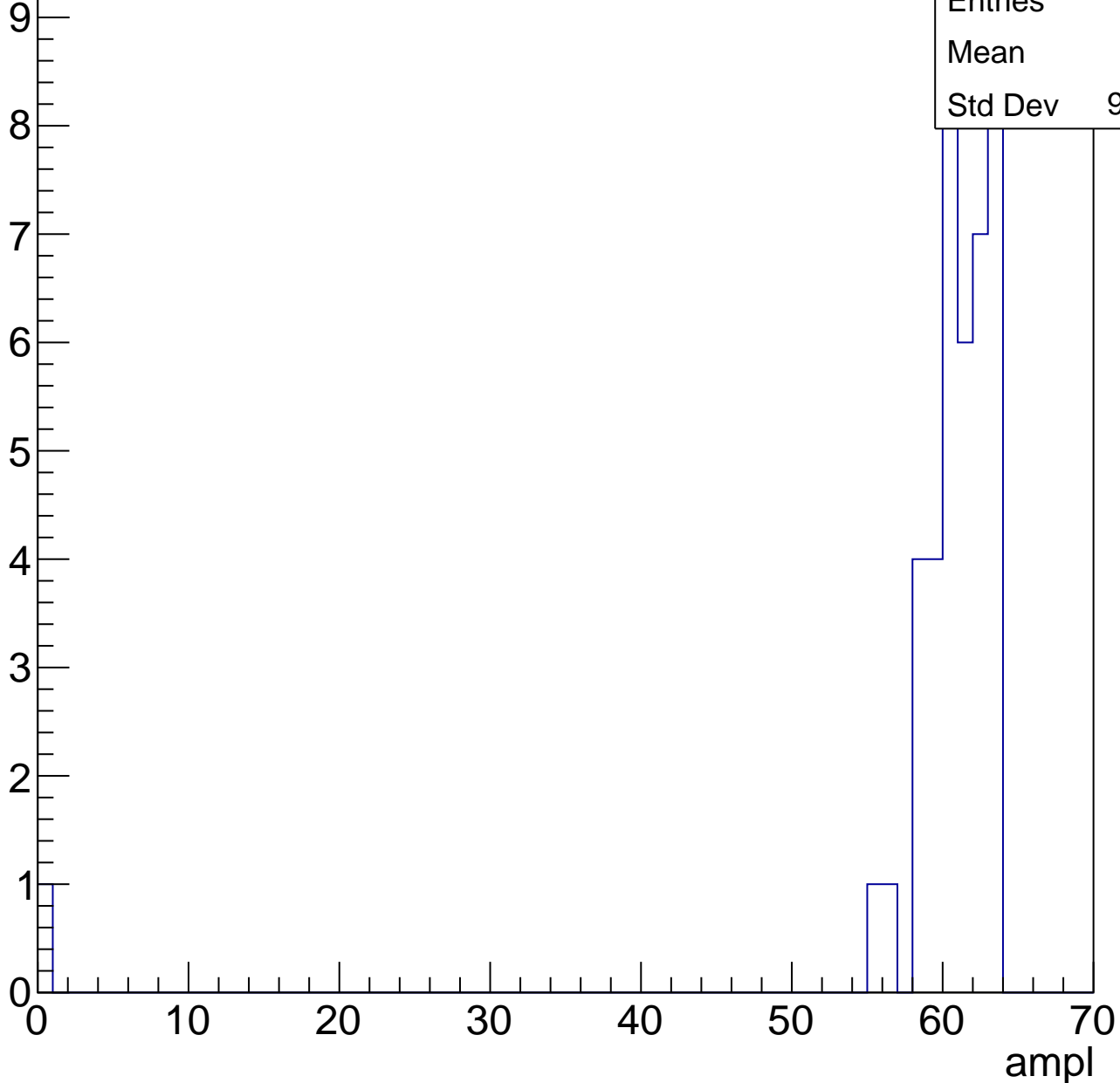
calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U23-ch85, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch85, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	3
Mean	61.67
Std Dev	0.4714

ampl

0 10 20 30 40 50 60 70

B1L103S, U23-ch85, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U23-ch86, adc0

calib_packv5_041523_1651.root, FC#0, port C2

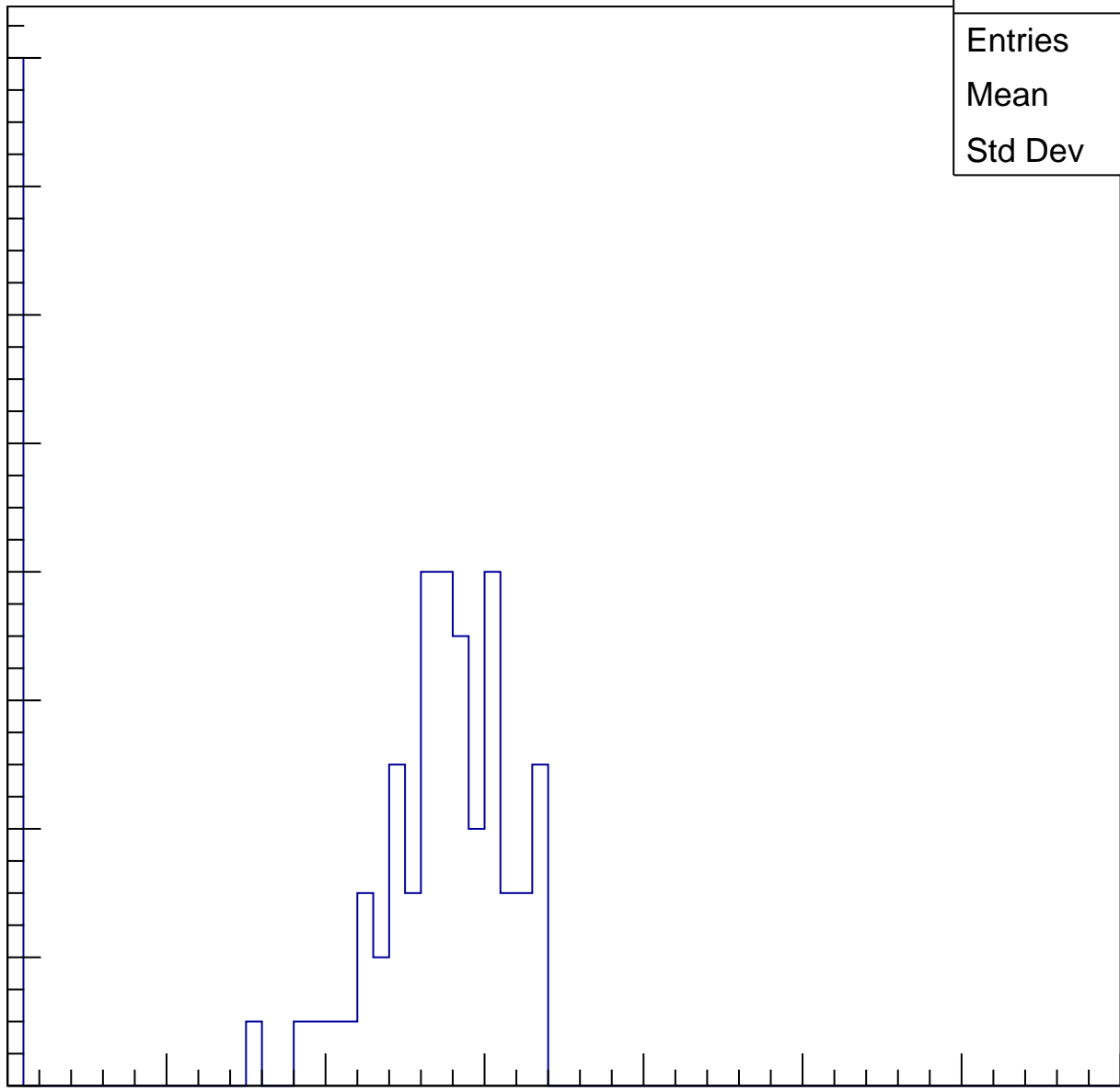
Entries	80
Mean	21.62
Std Dev	11.35

Entry

16
14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70

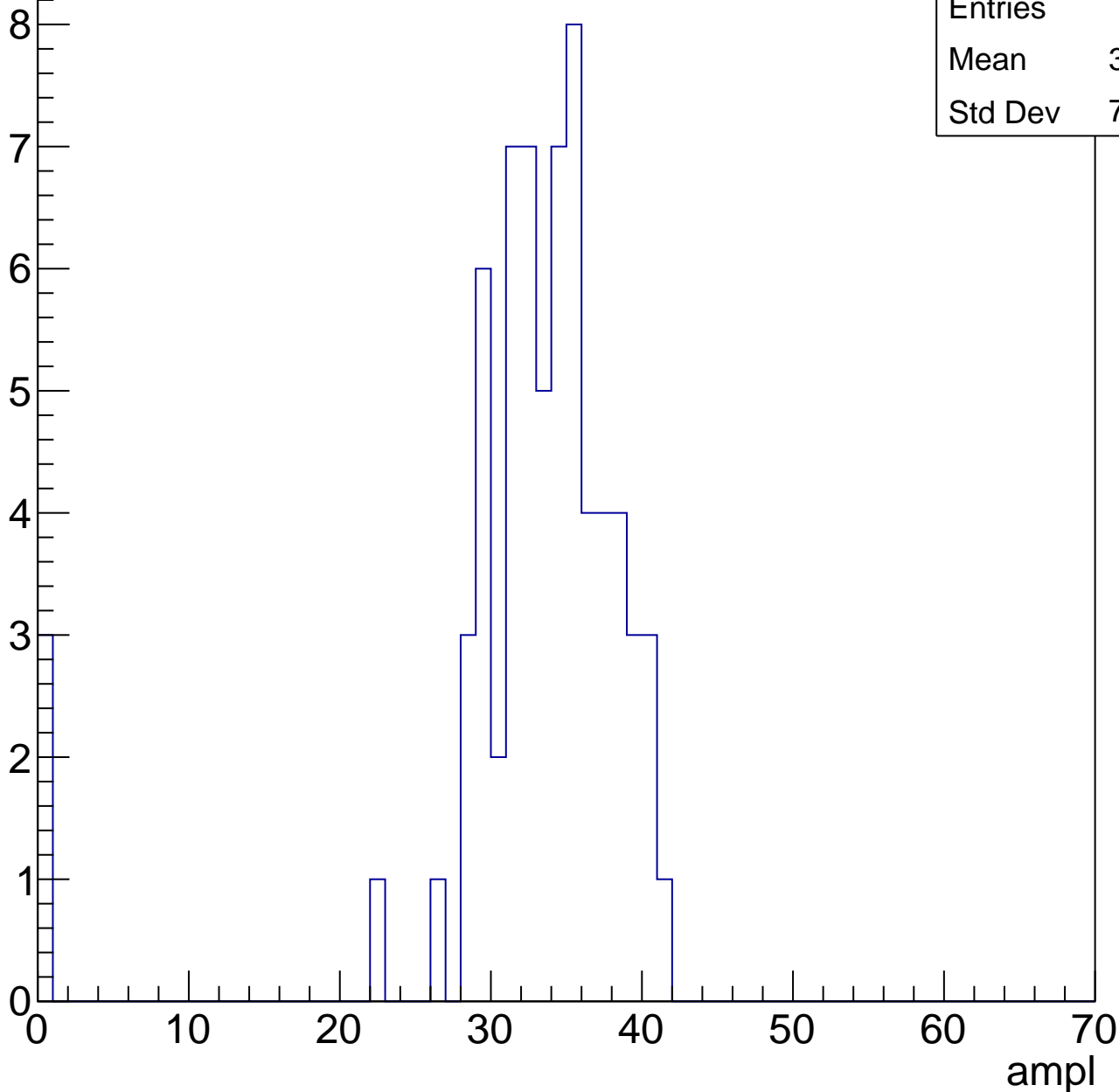


B1L103S, U23-ch86, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	32.06
Std Dev	7.763



B1L103S, U23-ch86, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

10

8

6

4

2

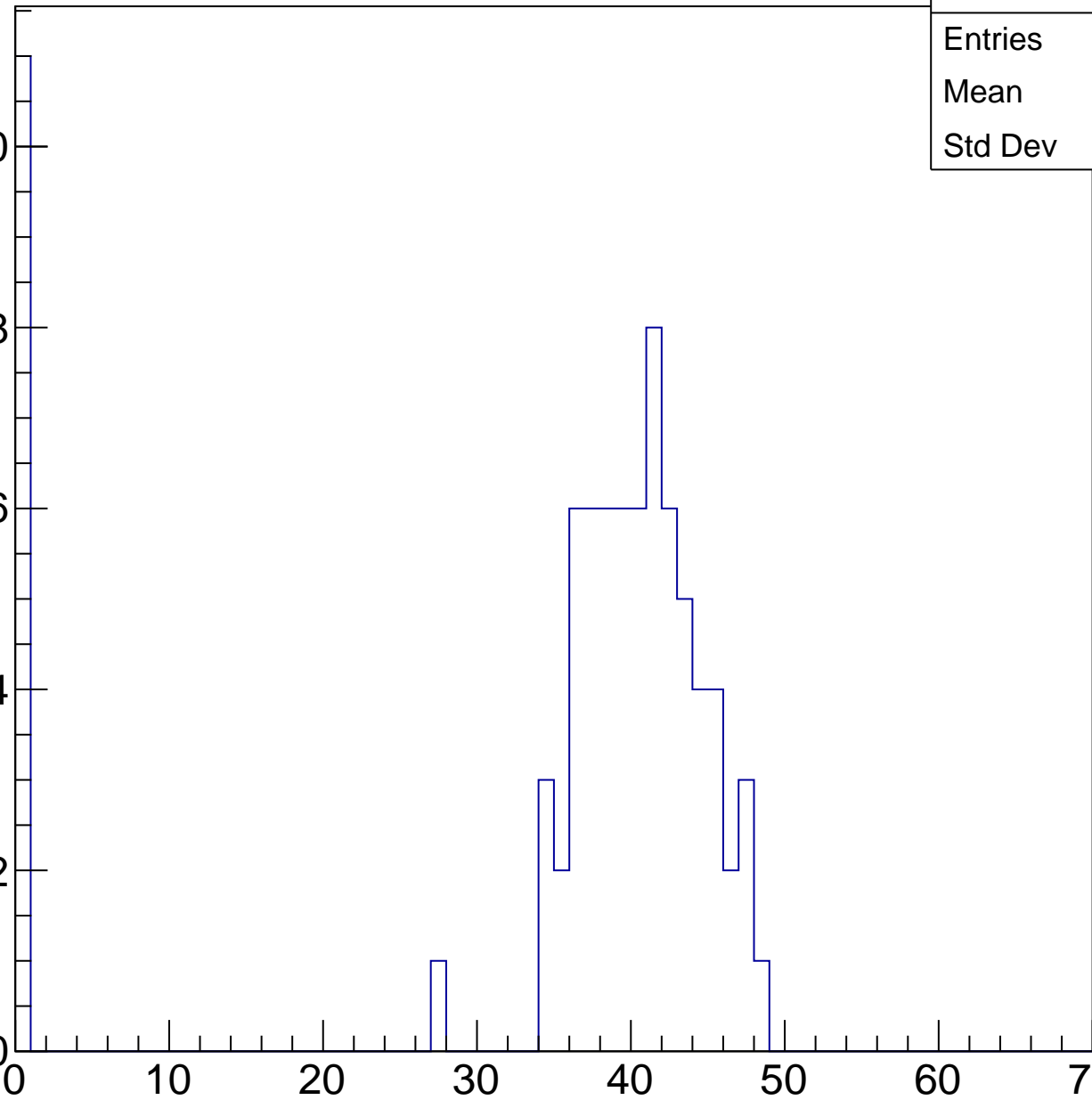
0

Entries 80

Mean 34.64

Std Dev 14.29

ampl

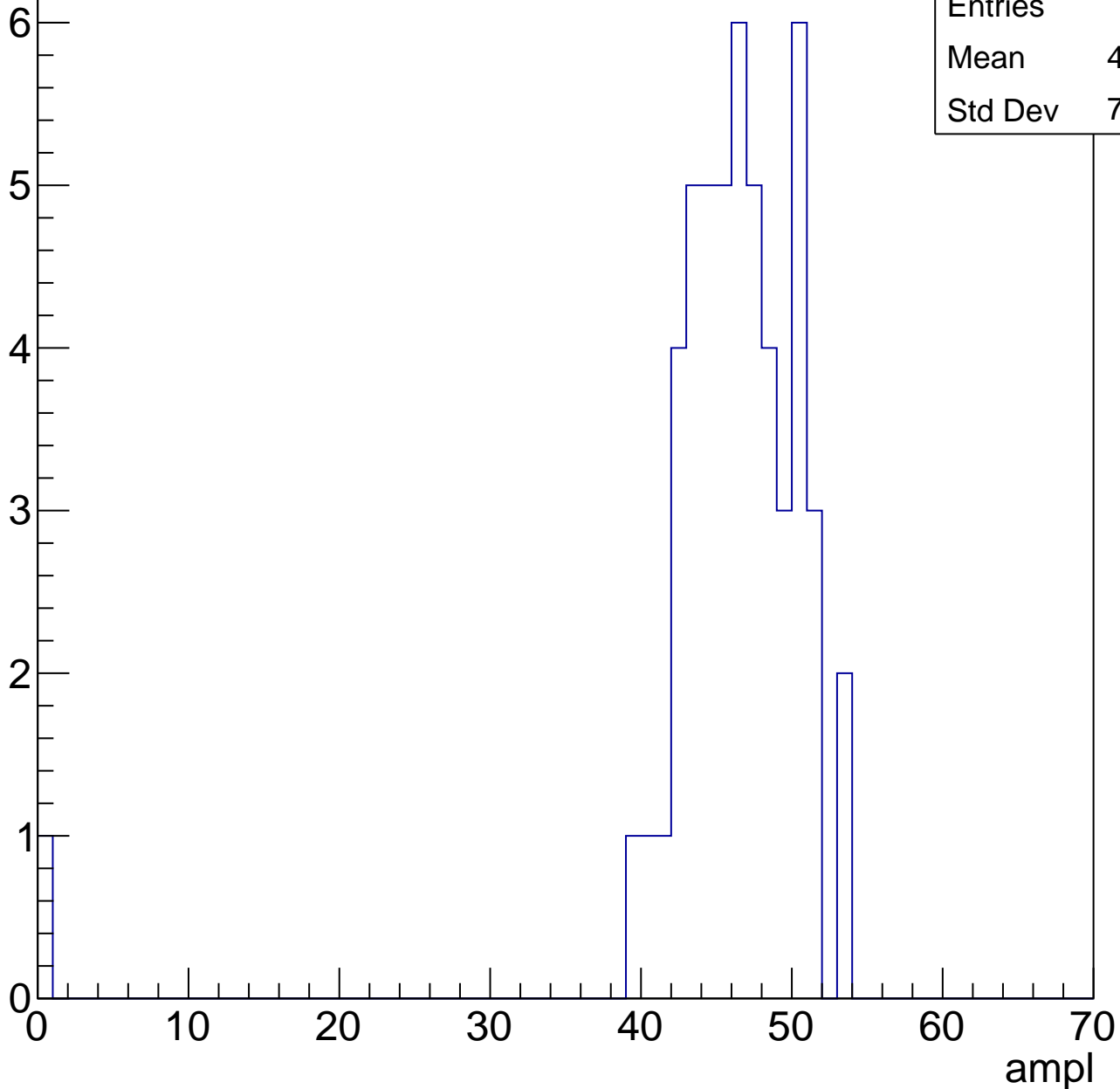


B1L103S, U23-ch86, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

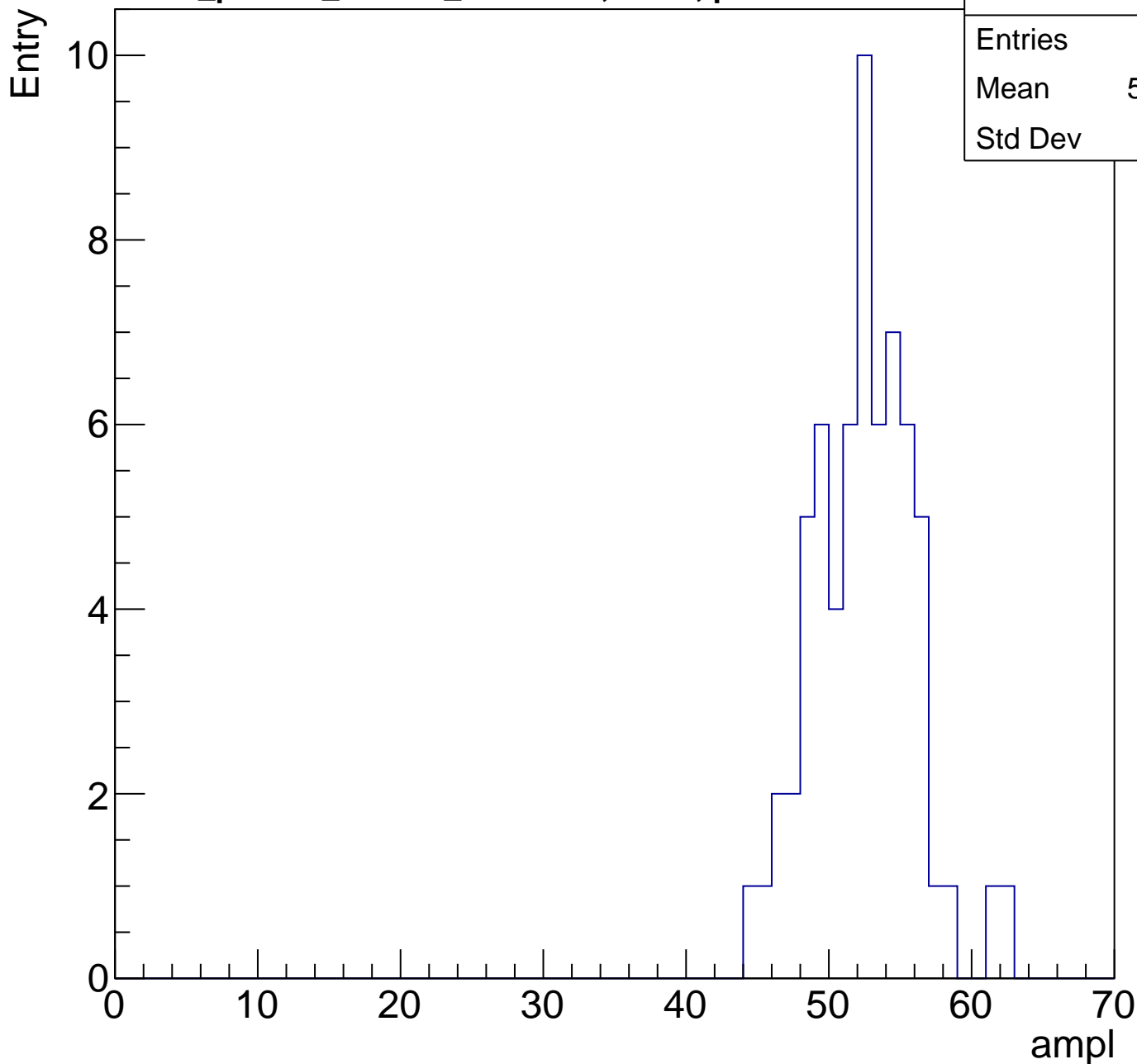
Entries	52
Mean	45.33
Std Dev	7.143



B1L103S, U23-ch86, adc4

calib_packv5_041523_1651.root, FC#0, port C2

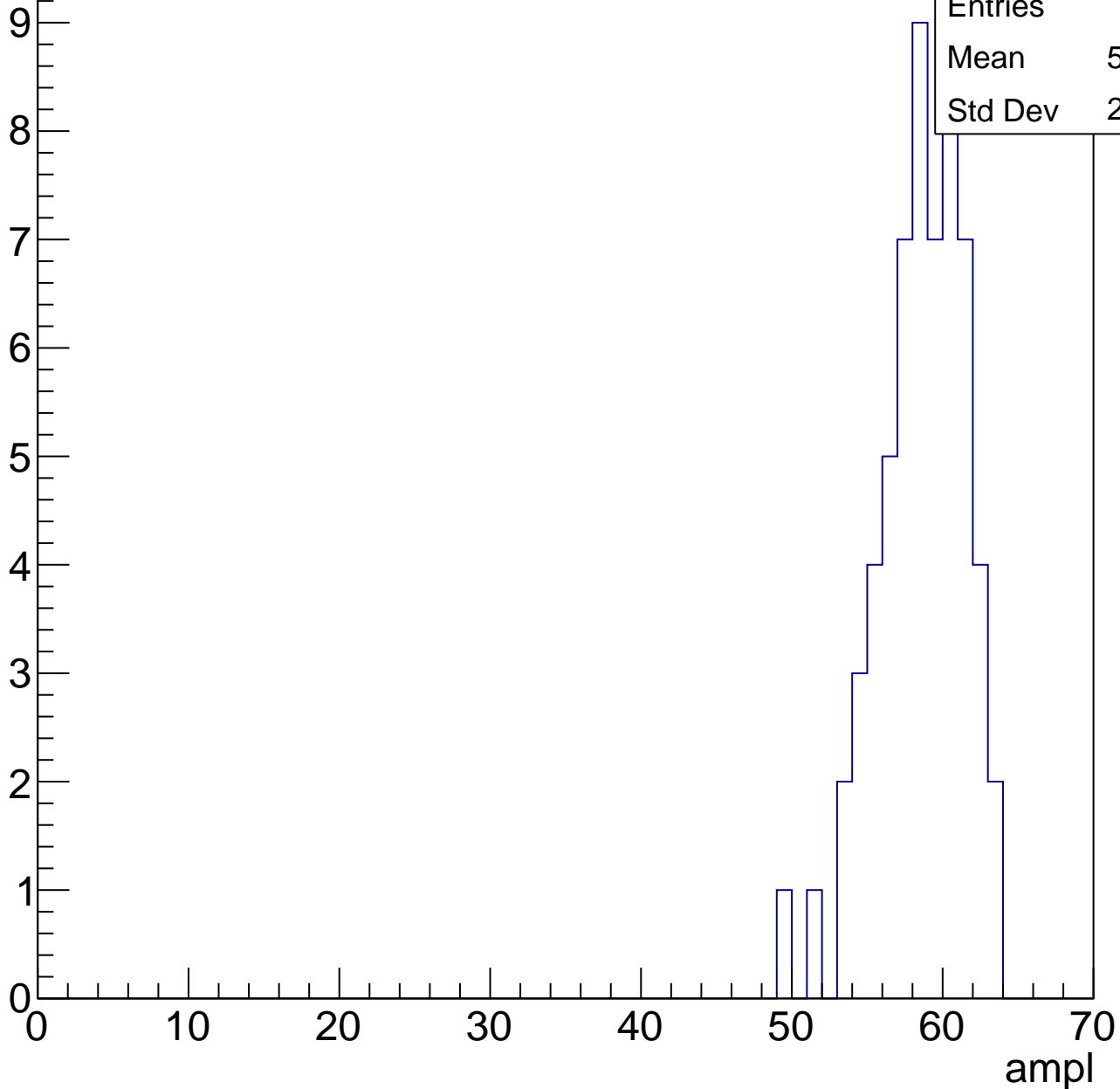
Entries	65
Mean	51.98
Std Dev	3.51



B1L103S, U23-ch86, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

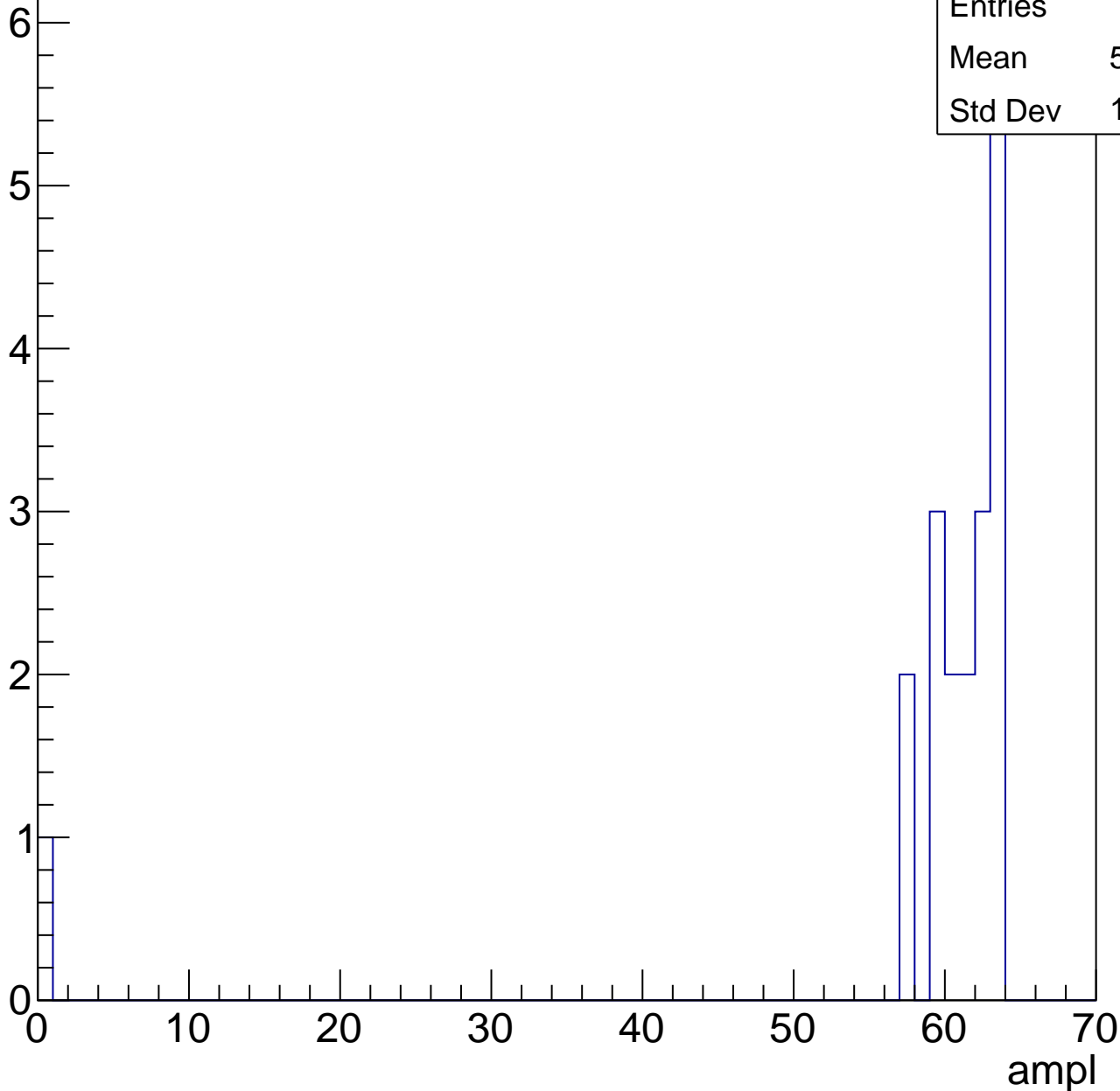


B1L103S, U23-ch86, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	19
Mean	57.74
Std Dev	13.75

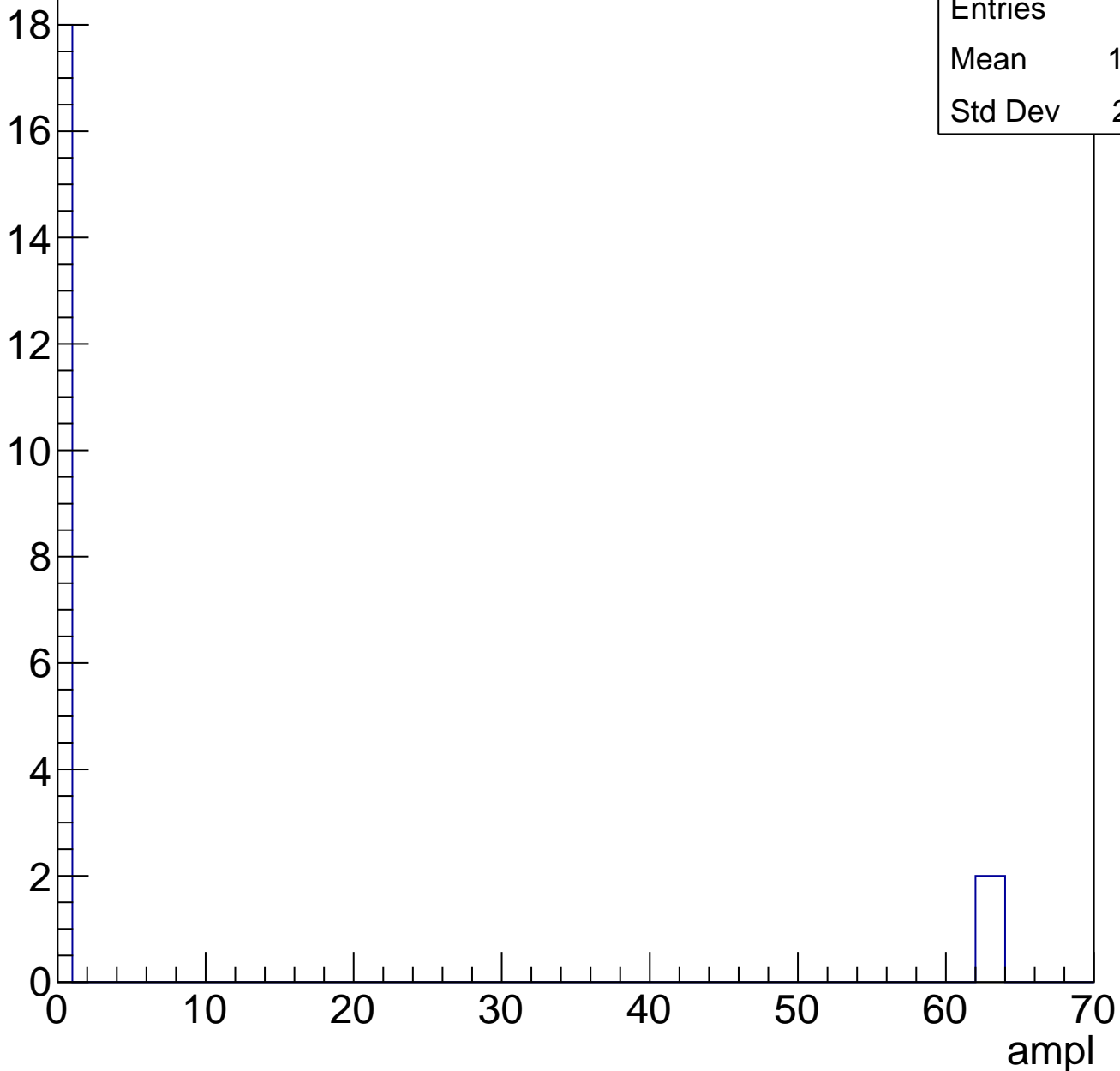


B1L103S, U23-ch86, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	22
Mean	11.36
Std Dev	24.11

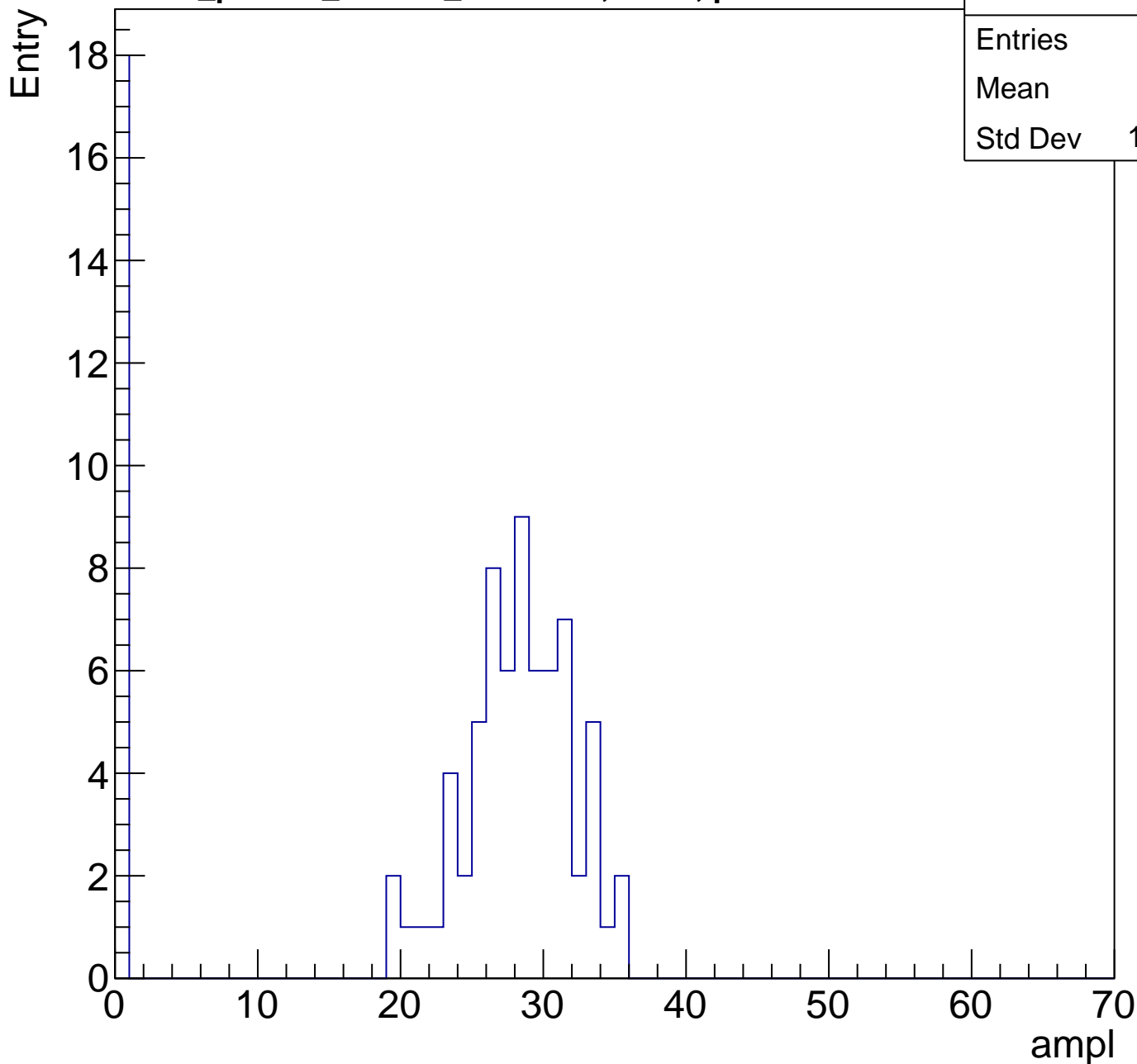
Entry



B1L103S, U23-ch87, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	86
Mean	22
Std Dev	11.78

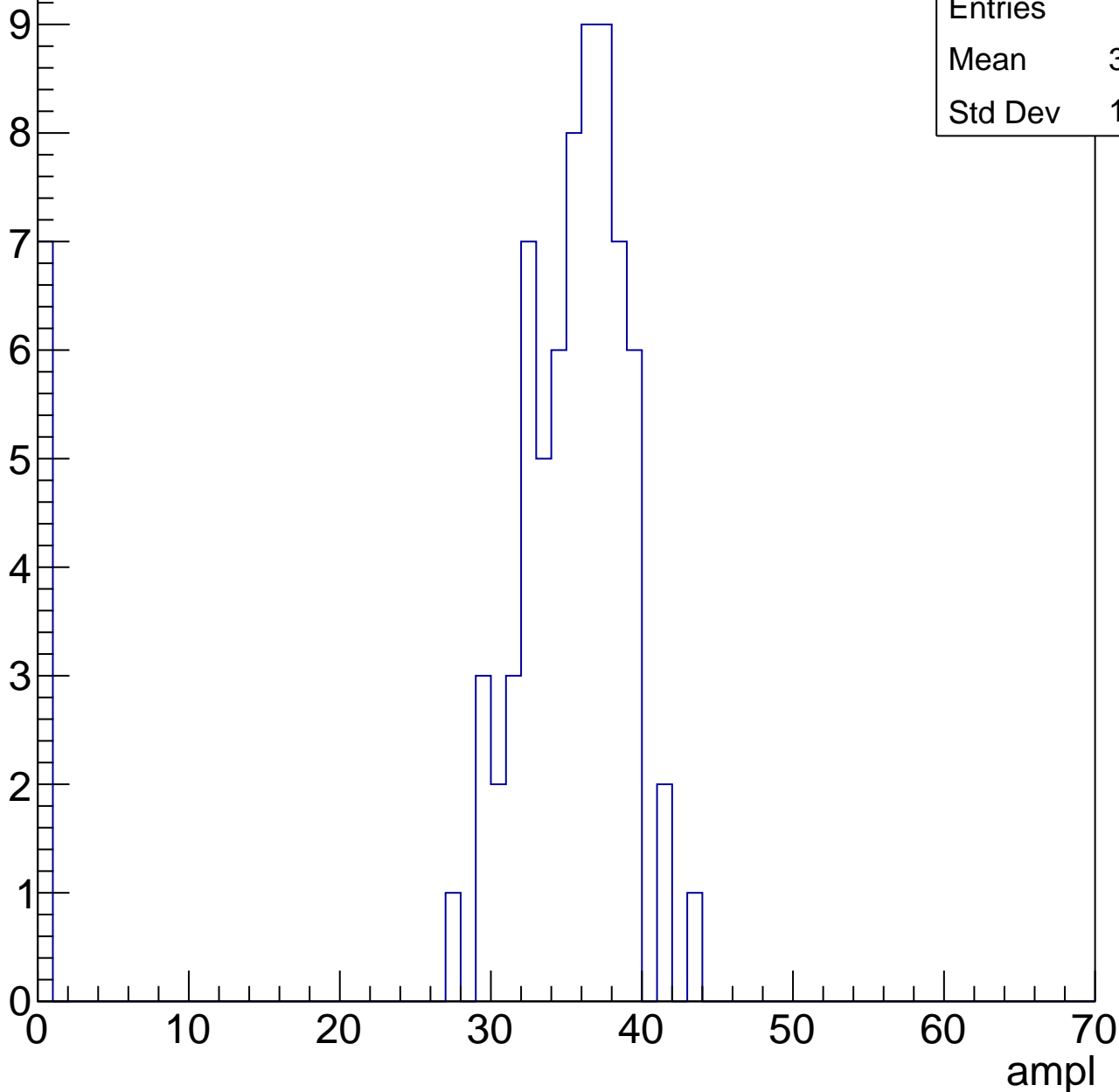


B1L103S, U23-ch87, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	76
Mean	31.87
Std Dev	10.59

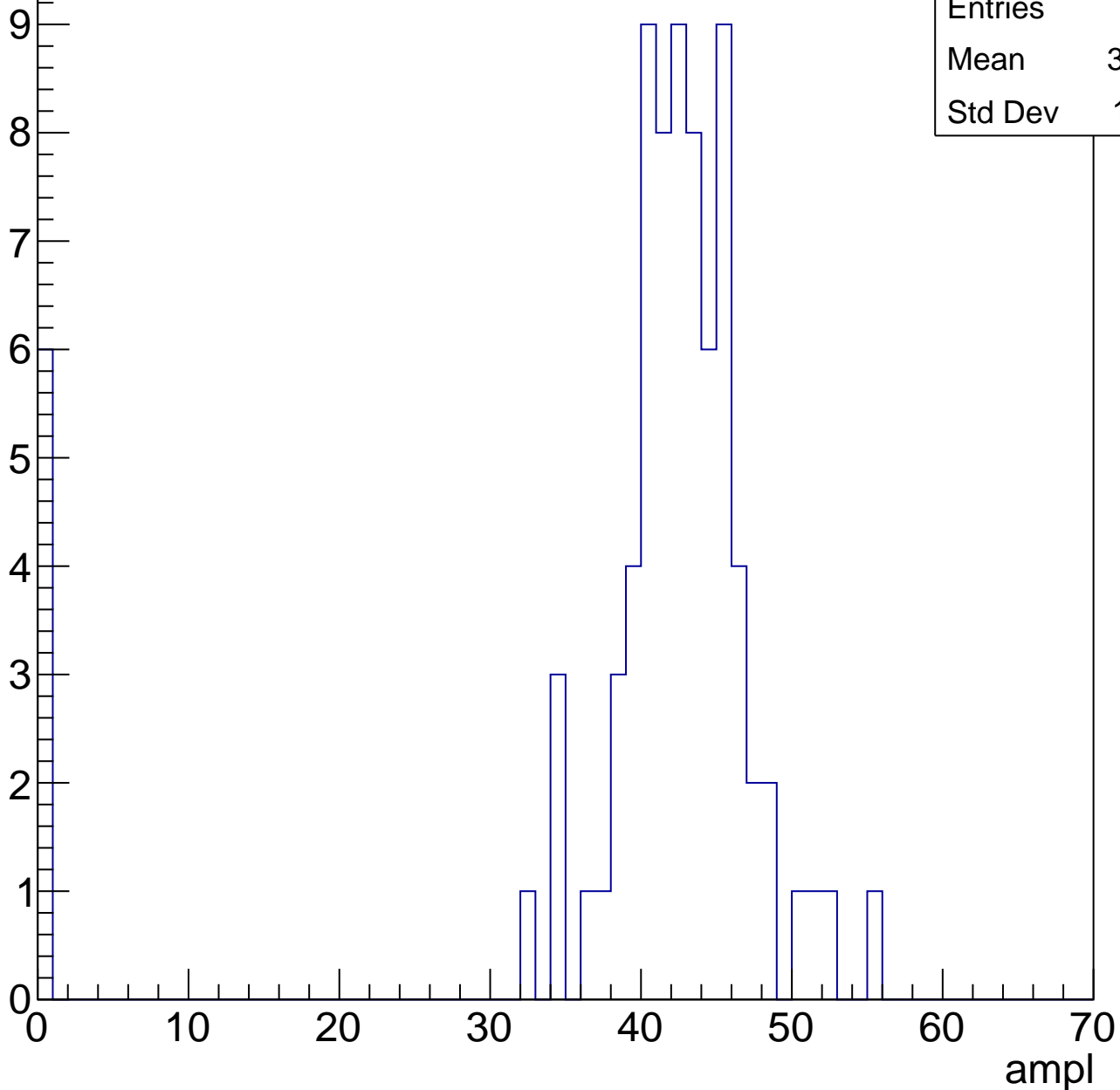


B1L103S, U23-ch87, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	80
Mean	39.23
Std Dev	11.81

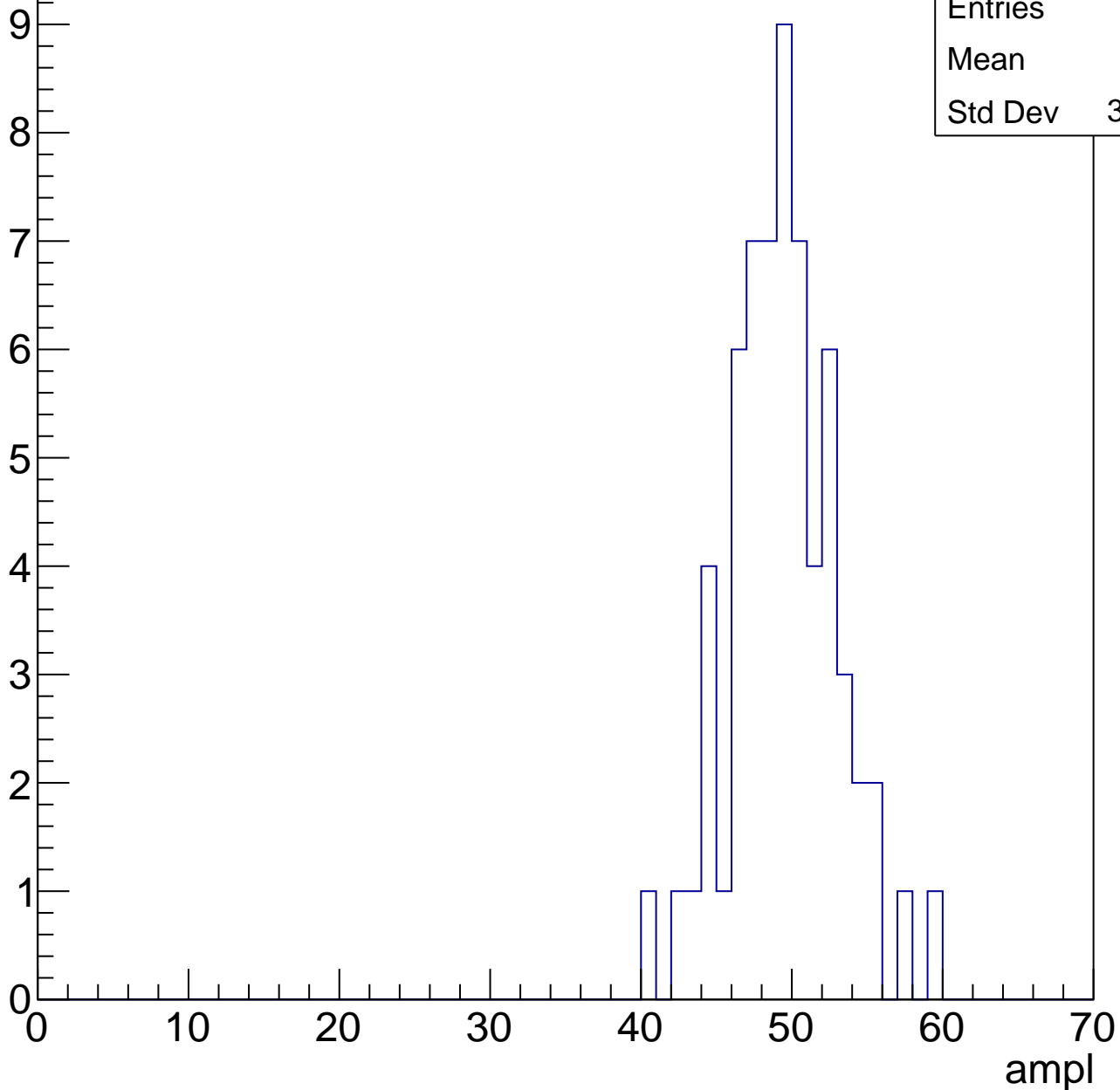


B1L103S, U23-ch87, adc3

calib_packv5_041523_1651.root, FC#0, port C2

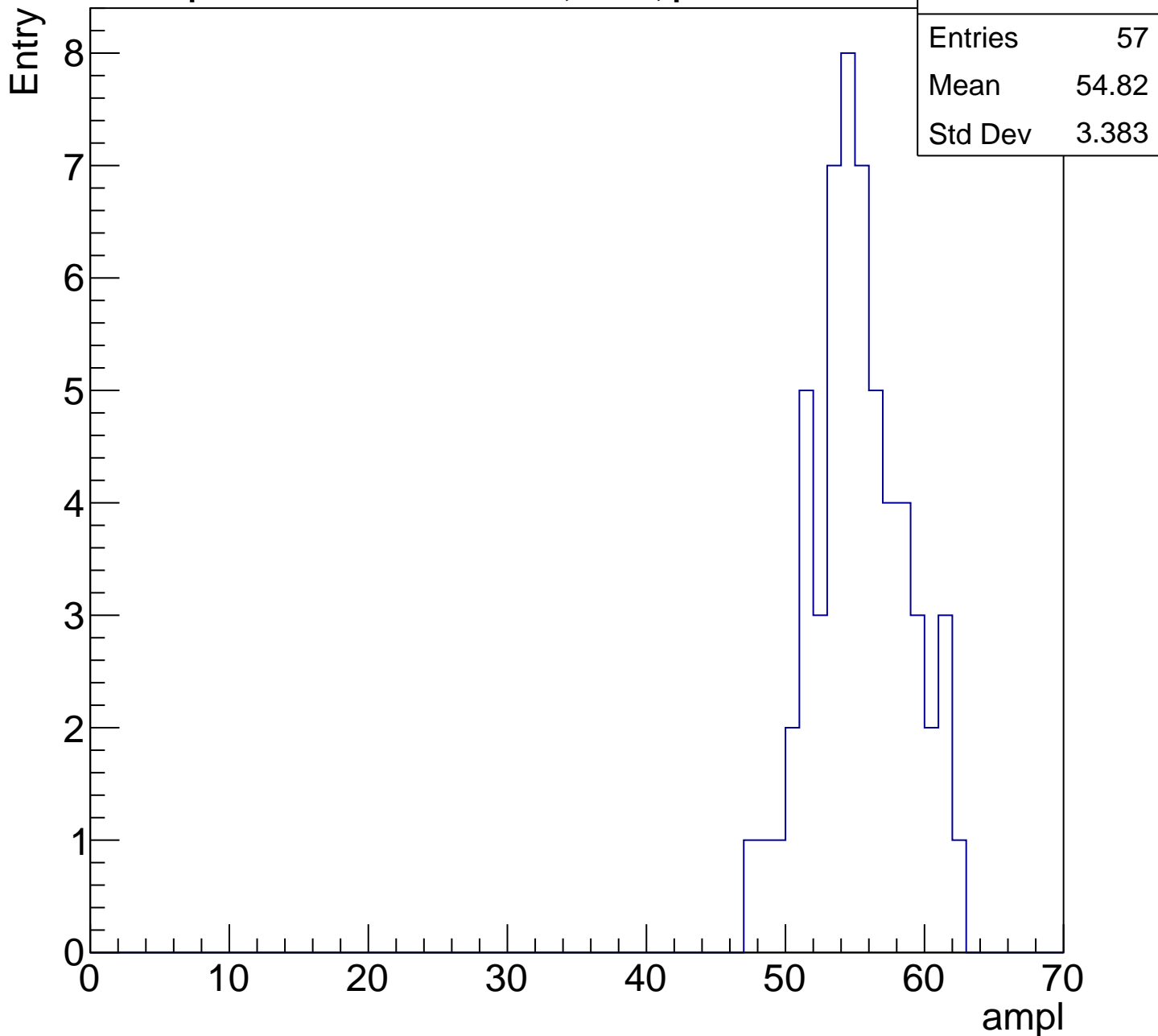
Entry

Entries	63
Mean	49
Std Dev	3.523



B1L103S, U23-ch87, adc4

calib_packv5_041523_1651.root, FC#0, port C2

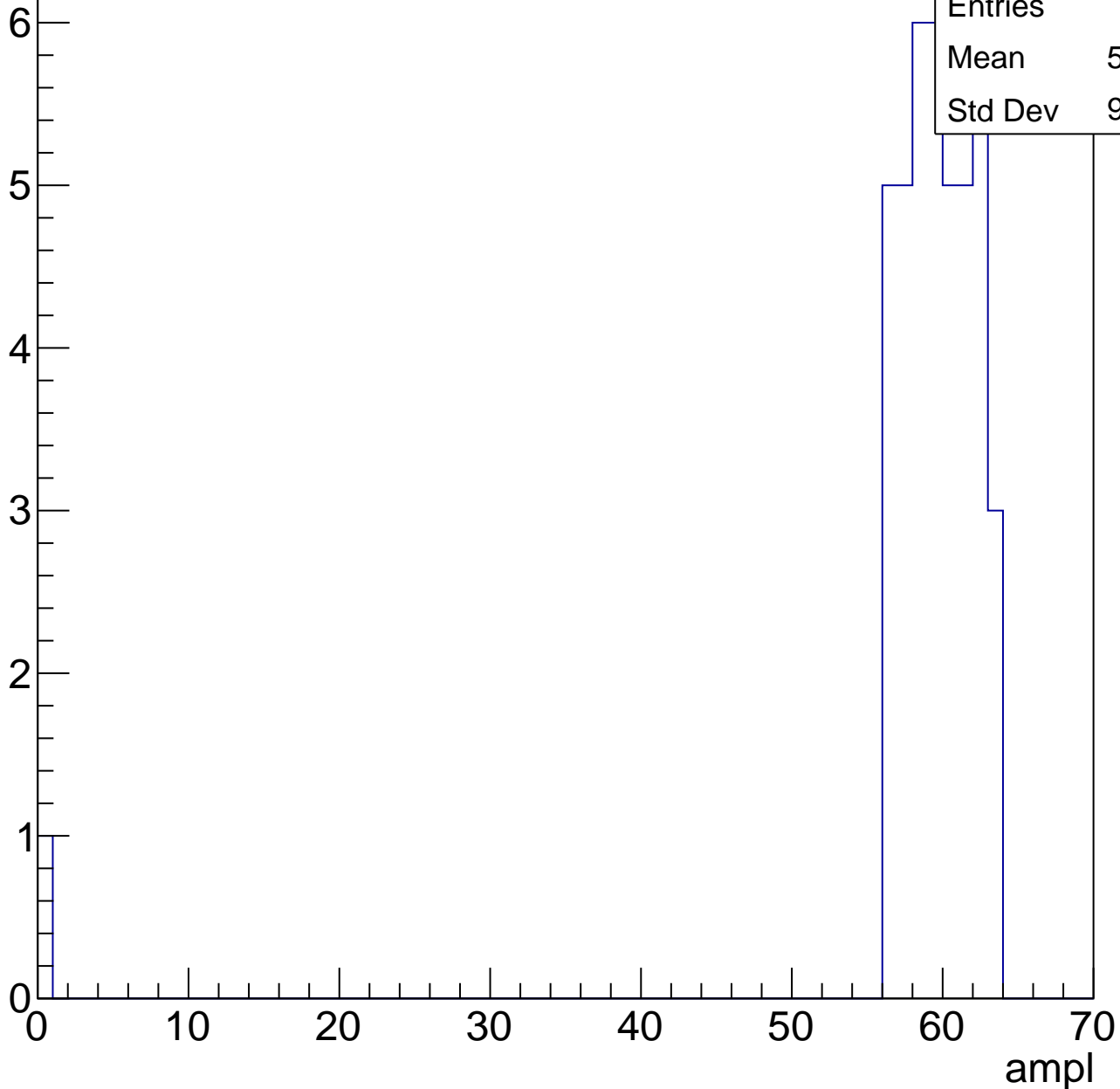


B1L103S, U23-ch87, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	42
Mean	57.93
Std Dev	9.298

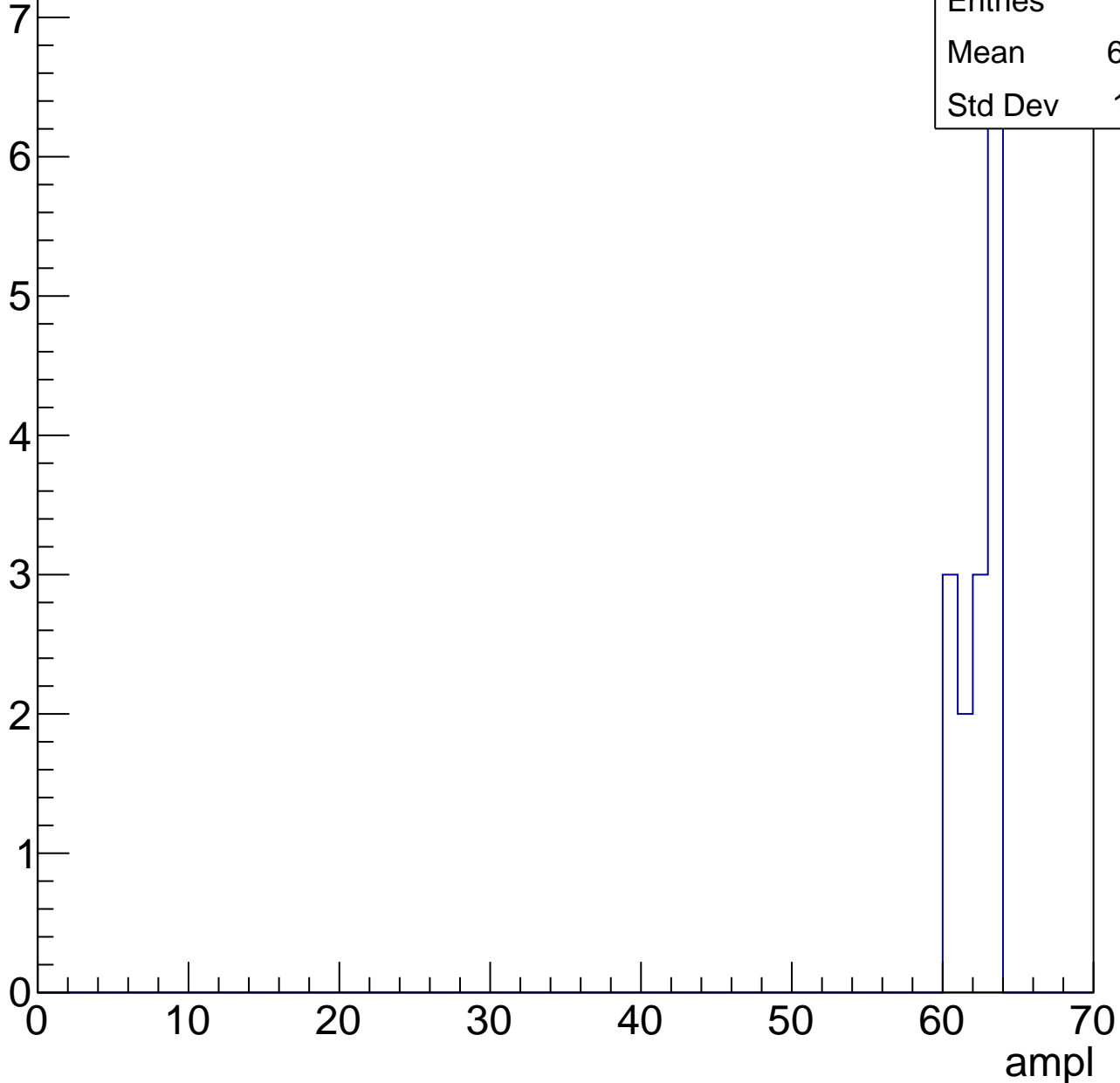


B1L103S, U23-ch87, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	15
Mean	61.93
Std Dev	1.181



B1L103S, U23-ch87, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

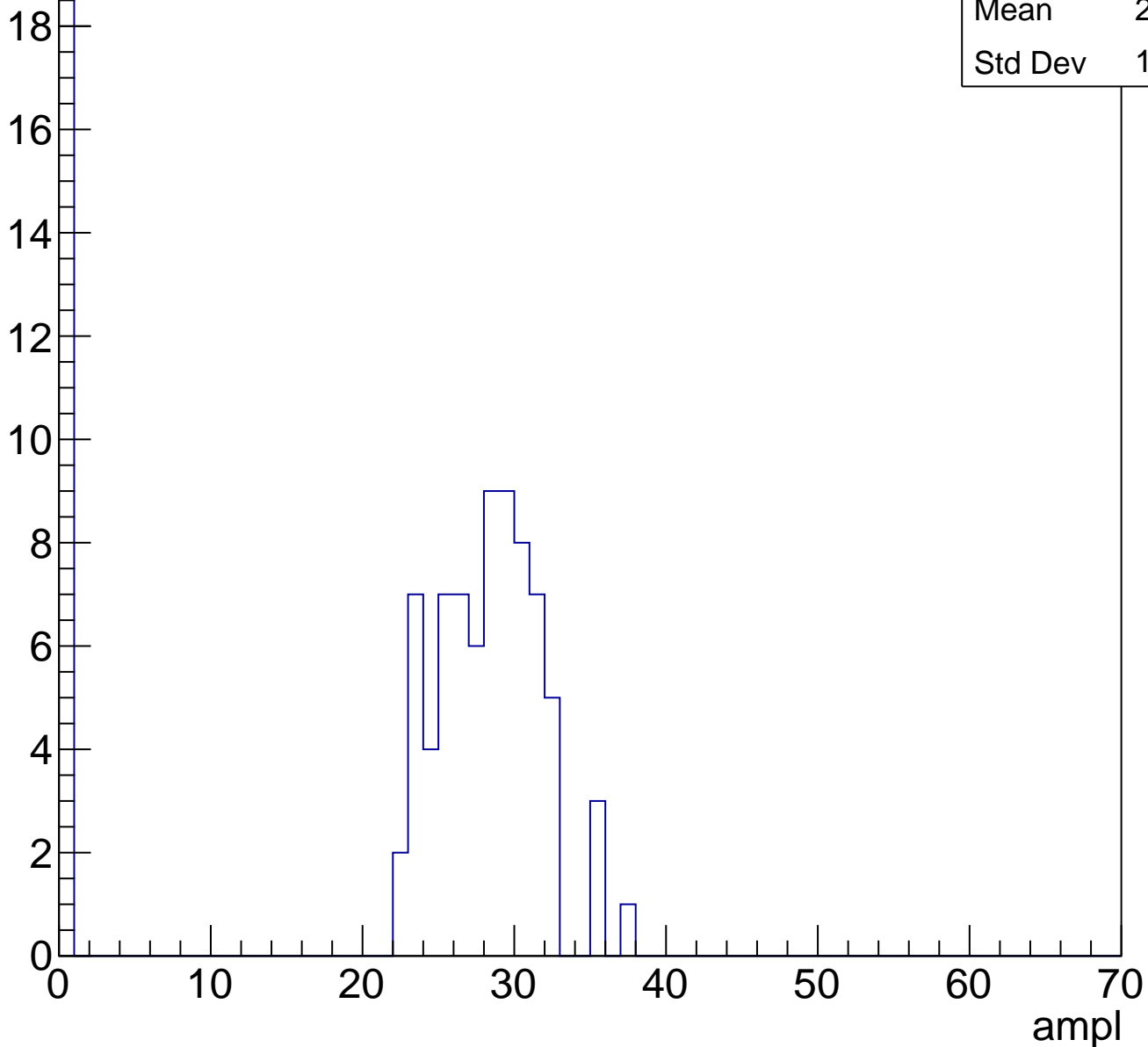
ampl

B1L103S, U23-ch88, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	94
Mean	22.26
Std Dev	11.58

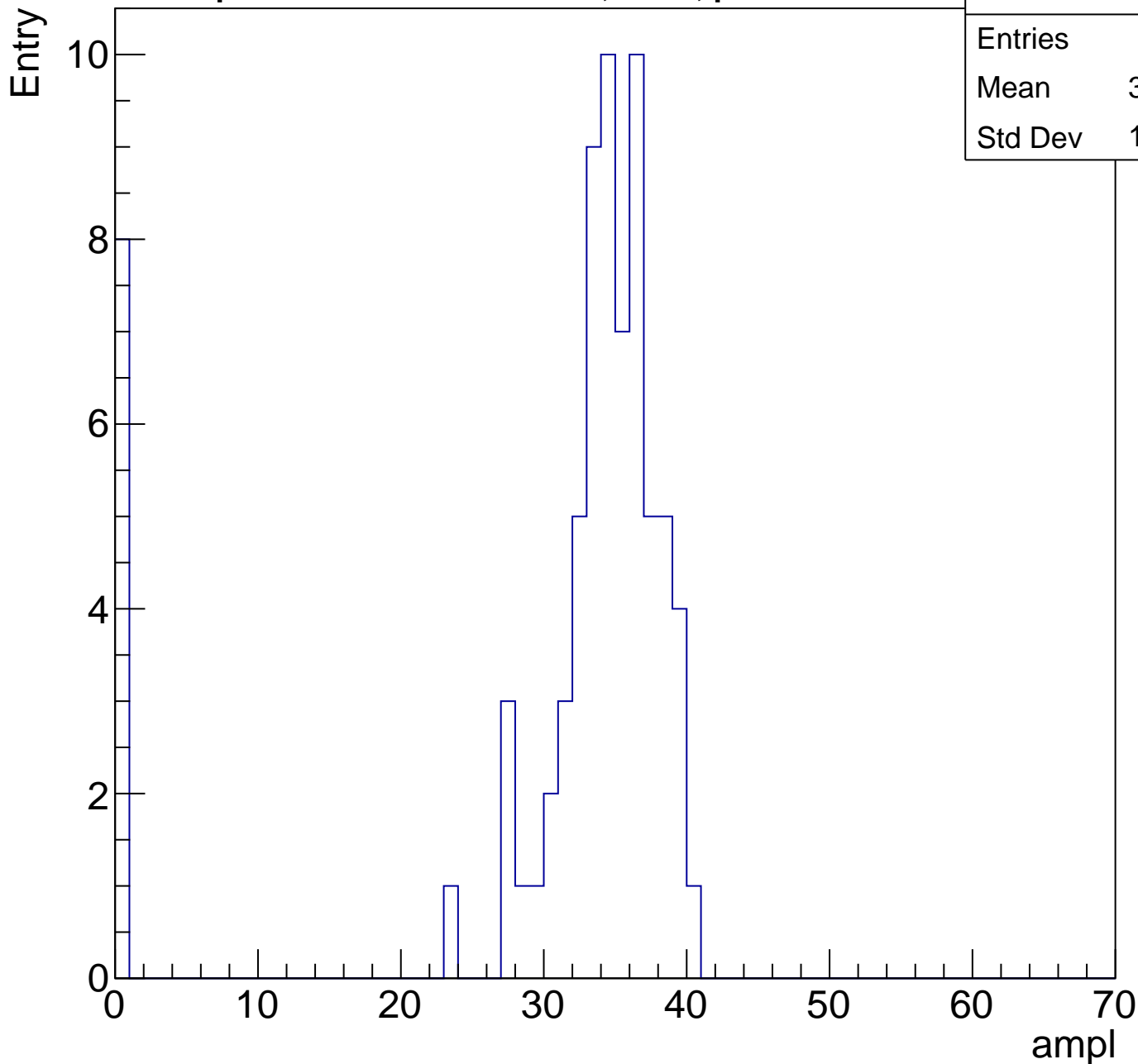
Entry



B1L103S, U23-ch88, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	75
Mean	30.49
Std Dev	10.99



B1L103S, U23-ch88, adc2

calib_packv5_041523_1651.root, FC#0, port C2

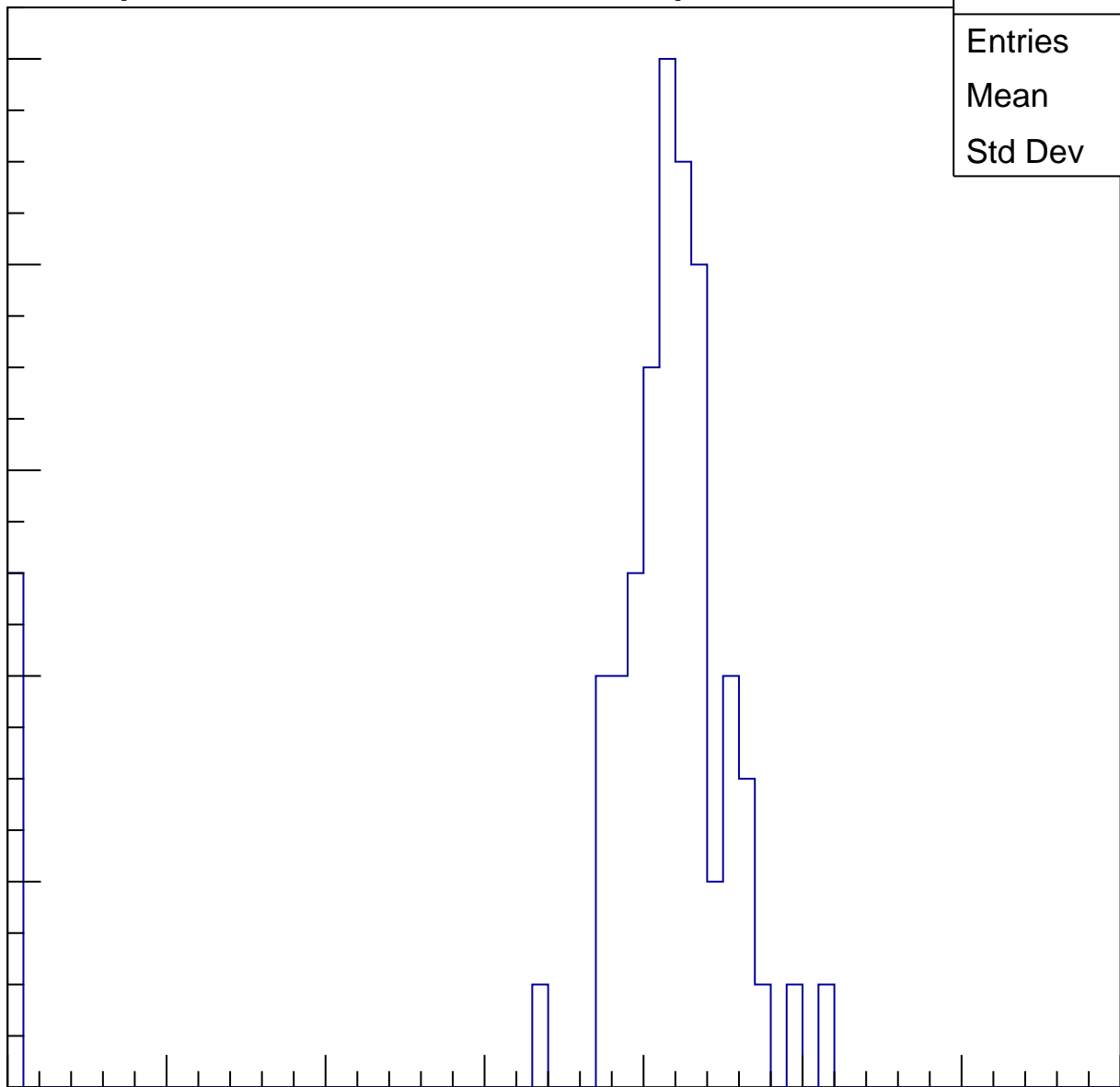
Entries	65
Mean	38.35
Std Dev	11.46

Entry

10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70

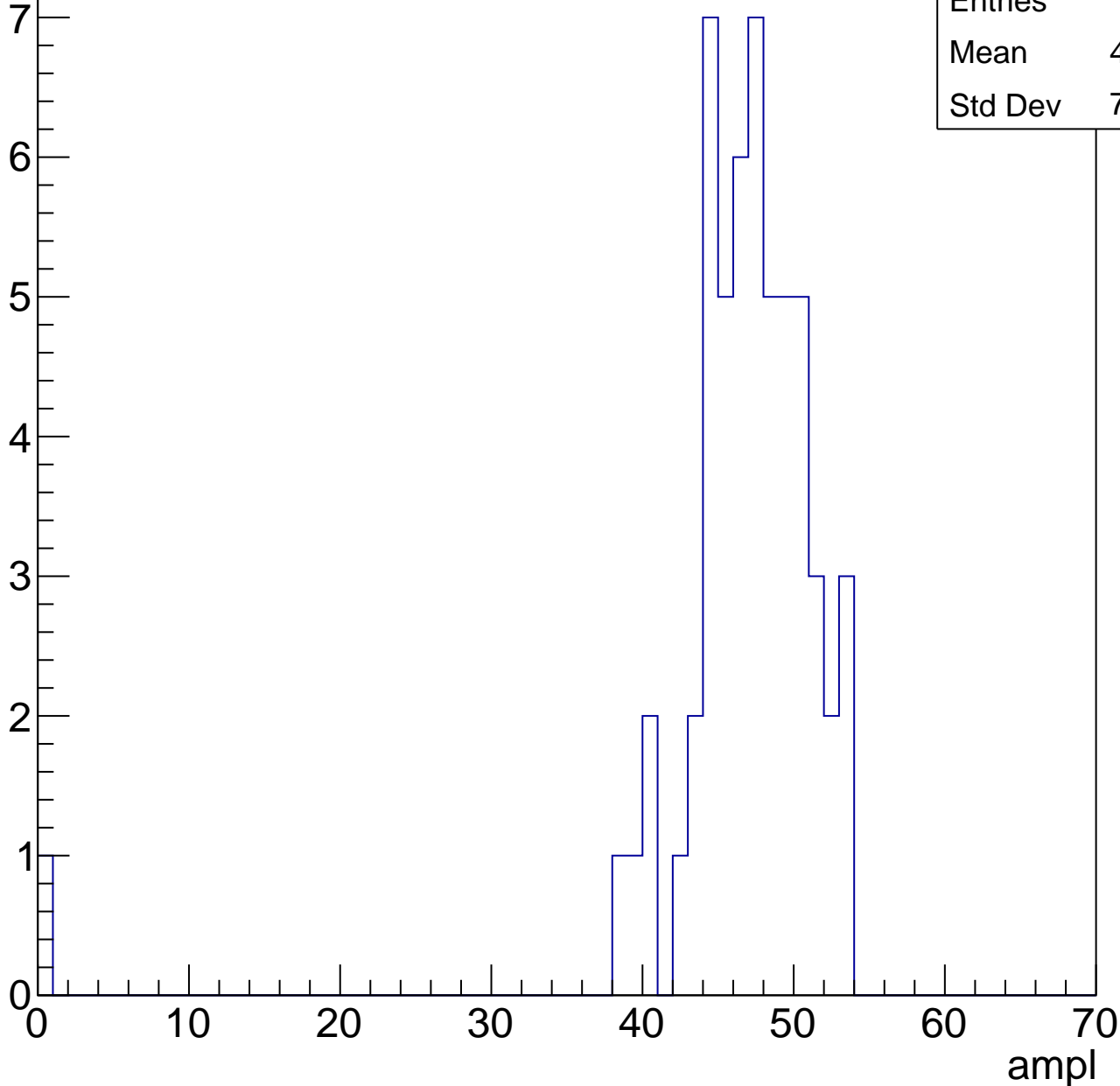


B1L103S, U23-ch88, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	56
Mean	45.96
Std Dev	7.089

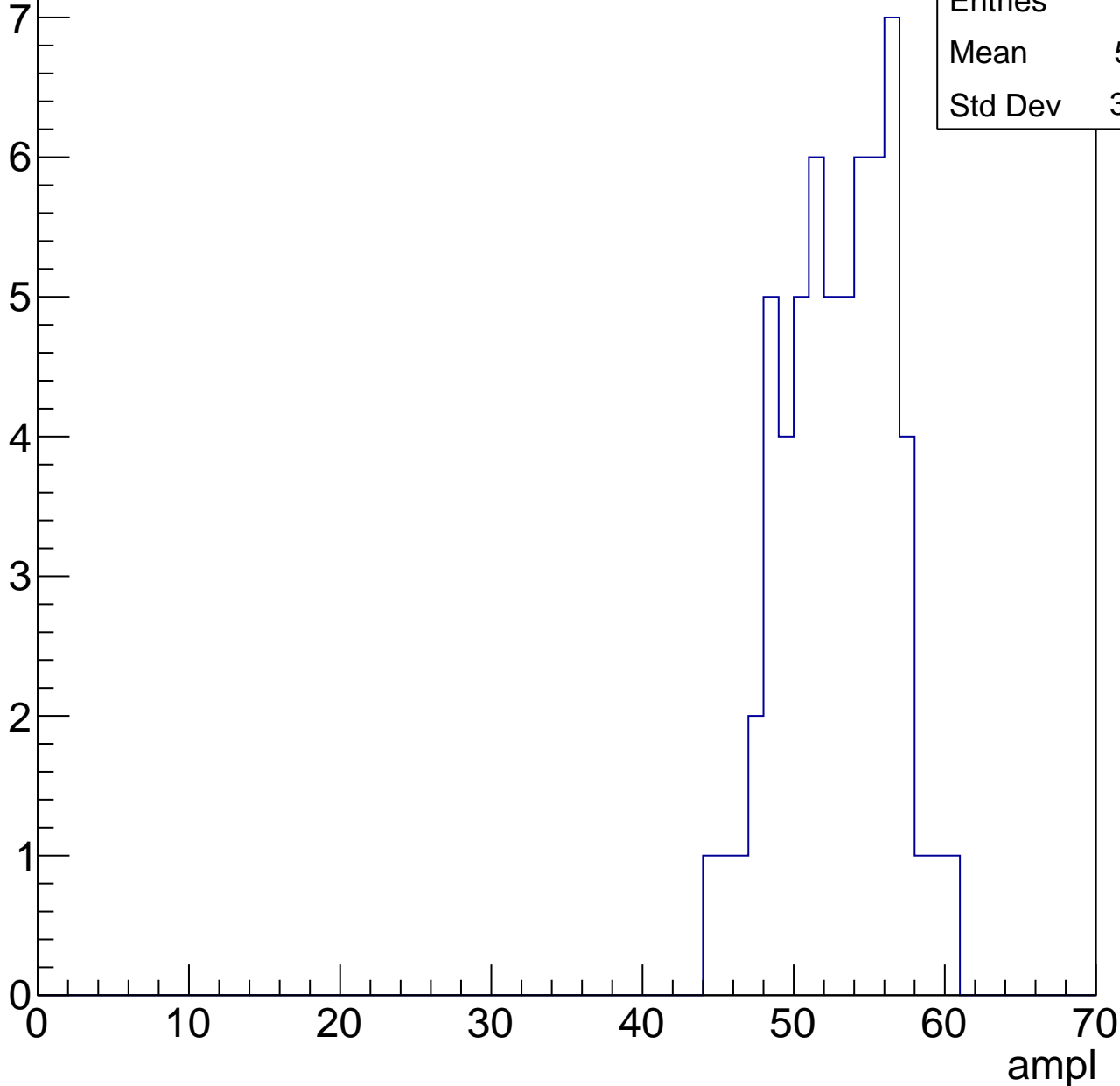


B1L103S, U23-ch88, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

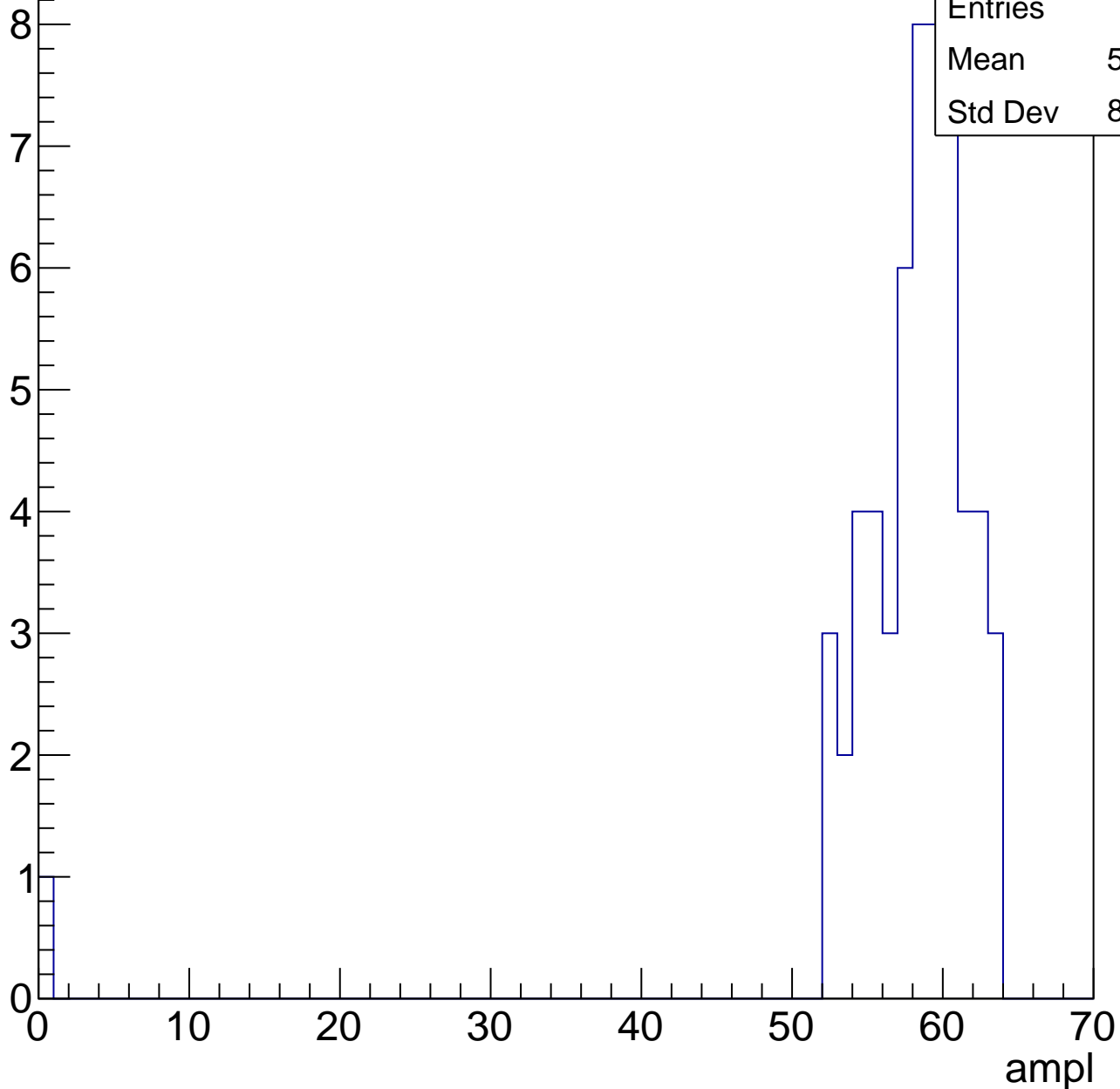
Entries	61
Mean	52.41
Std Dev	3.564



B1L103S, U23-ch88, adc5

calib_packv5_041523_1651.root, FC#0, port C2

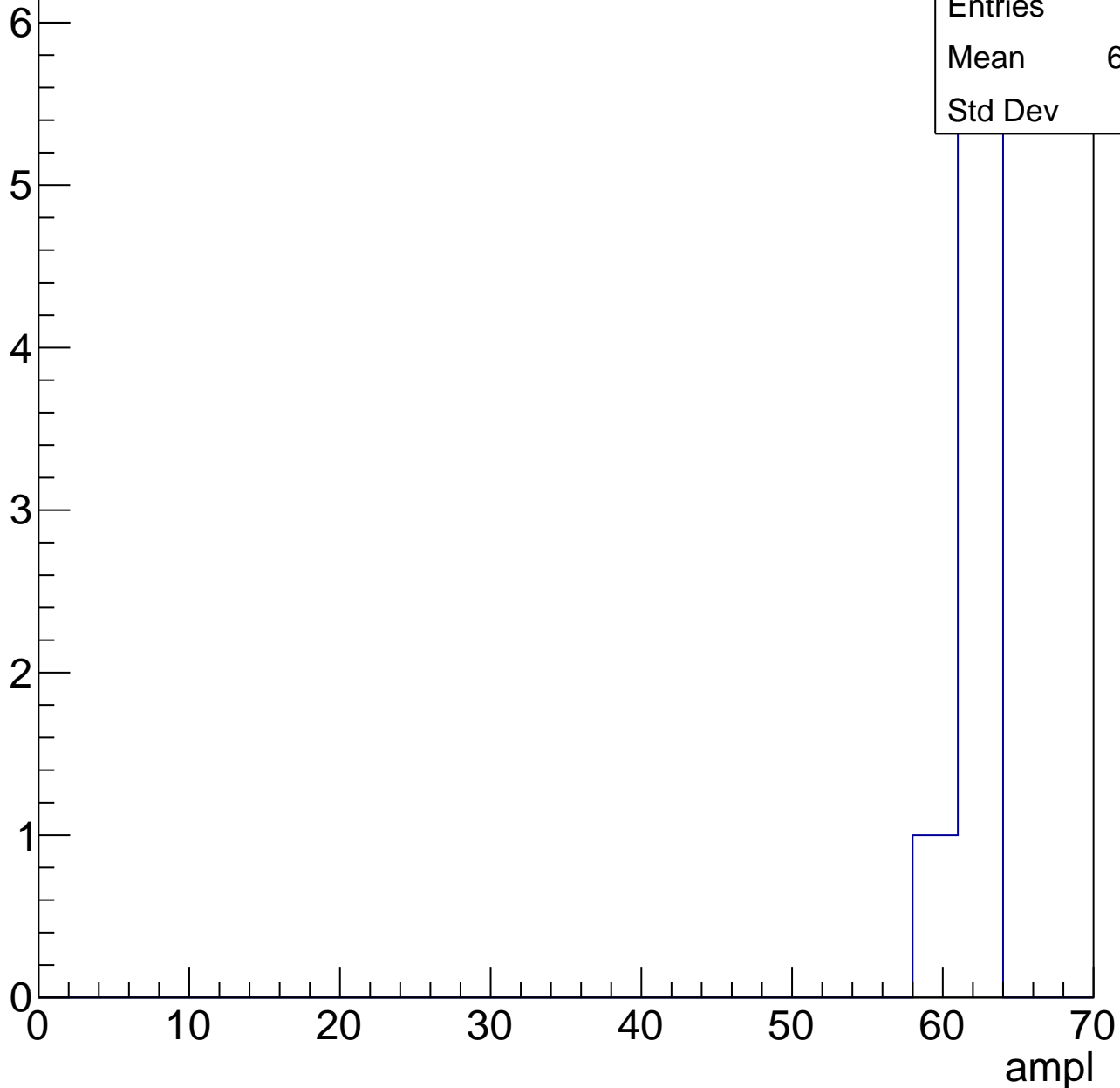
Entry



B1L103S, U23-ch88, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch88, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	3.316
Std Dev	14.07

Entry



B1L103S, U23-ch89, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	97
Mean	23.96
Std Dev	11.64

Entry

16
14
12
10
8
6
4
2
0

0

10

20

30

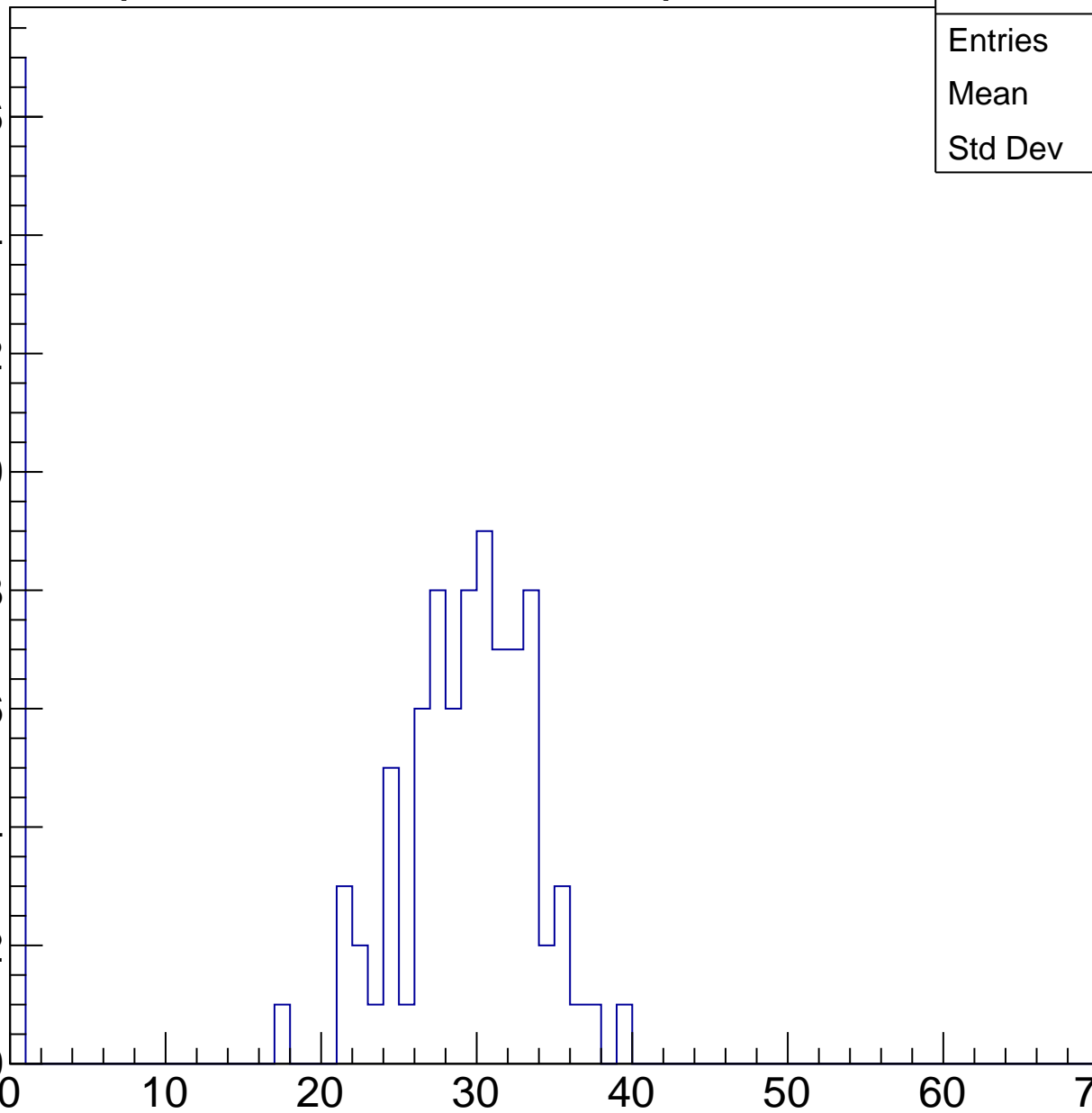
40

50

60

70

ampl



B1L103S, U23-ch89, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	76
Mean	31.28
Std Dev	13.24

Entry

10

8

6

4

2

0

0

10

20

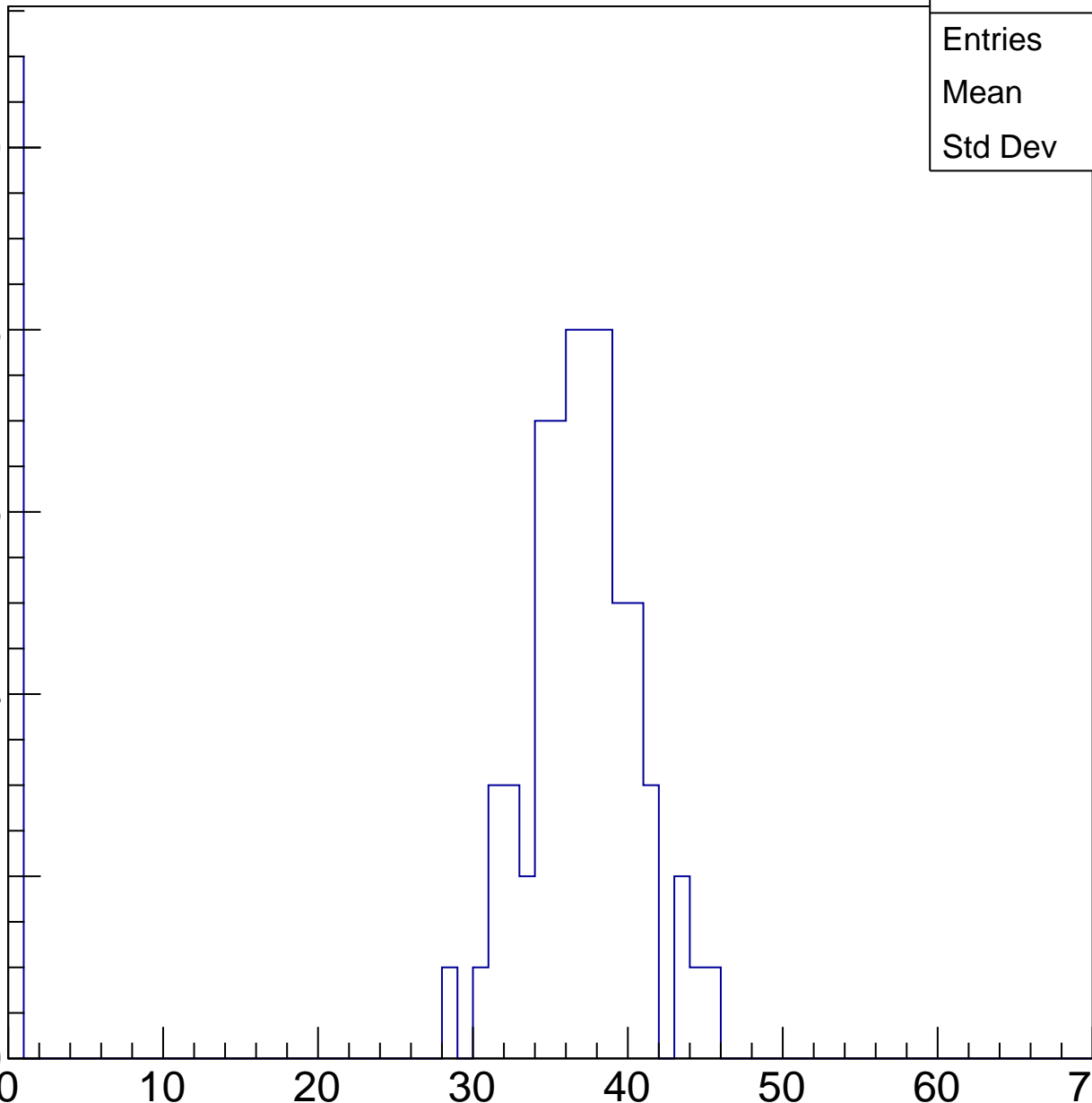
30

40

50

60

ampl



B1L103S, U23-ch89, adc2

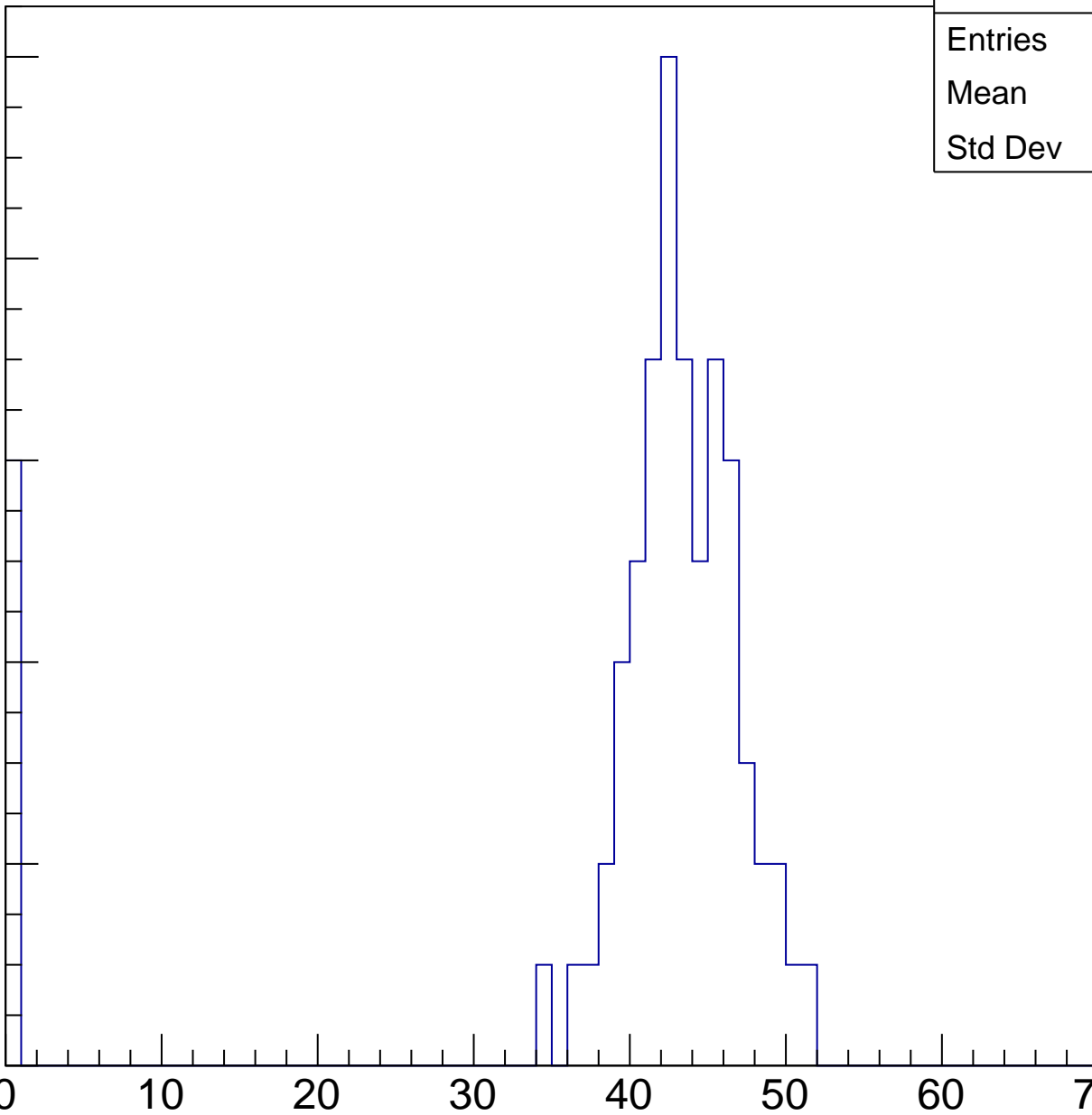
calib_packv5_041523_1651.root, FC#0, port C2

Entries	71
Mean	39.35
Std Dev	12.38

Entry

10
8
6
4
2
0

ampl

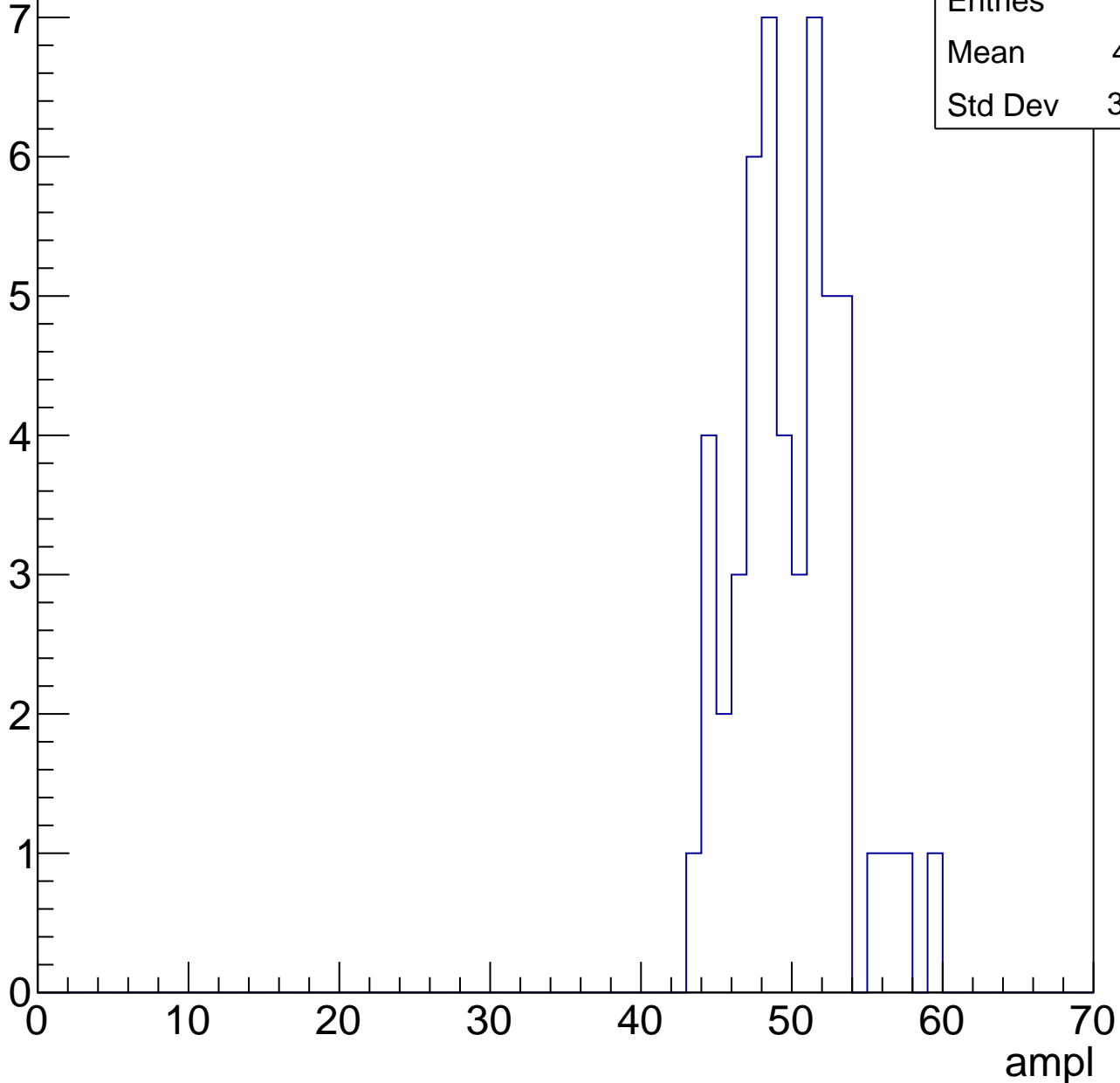


B1L103S, U23-ch89, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	51
Mean	49.41
Std Dev	3.493

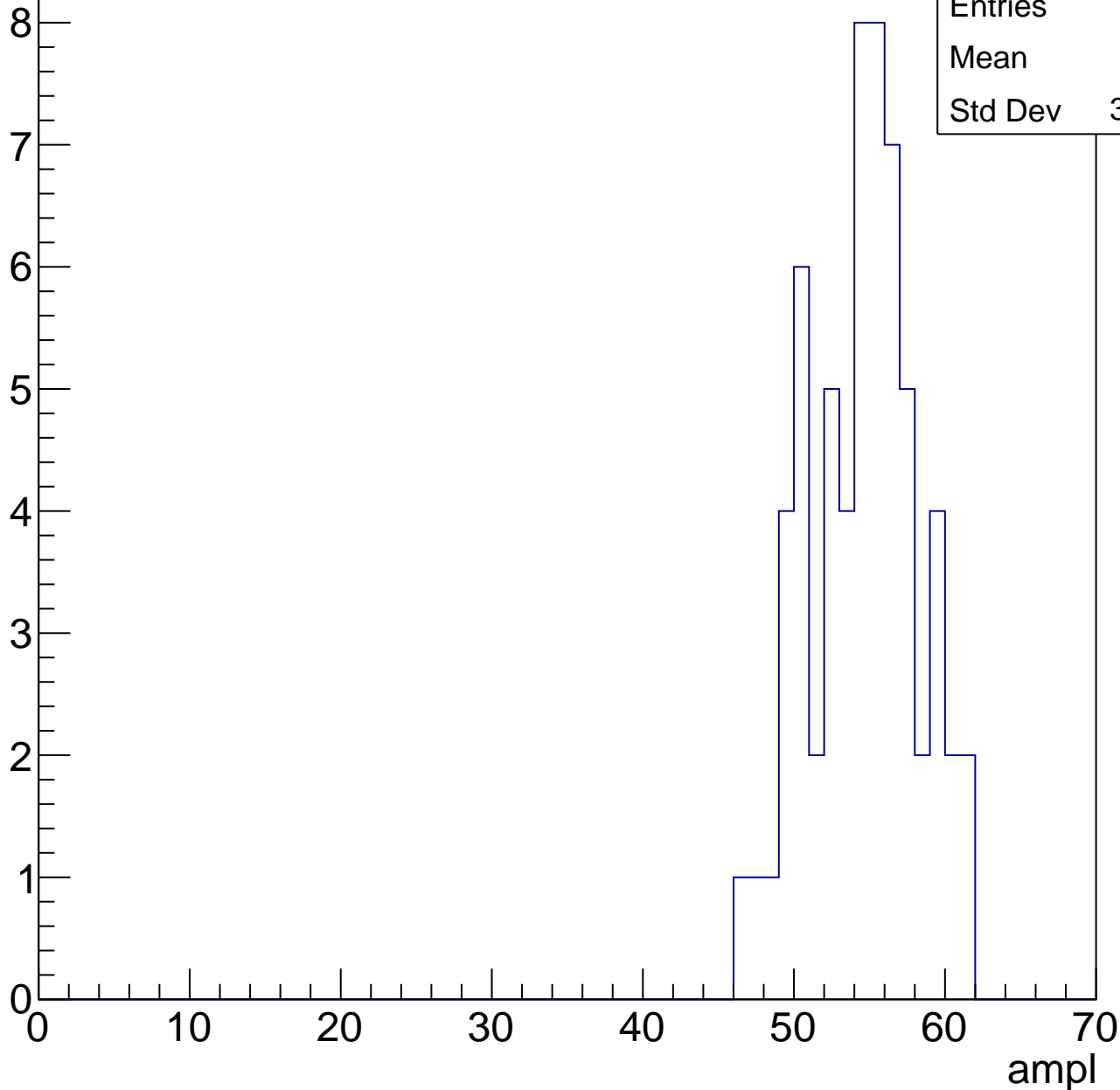


B1L103S, U23-ch89, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	54.1
Std Dev	3.523



B1L103S, U23-ch89, adc5

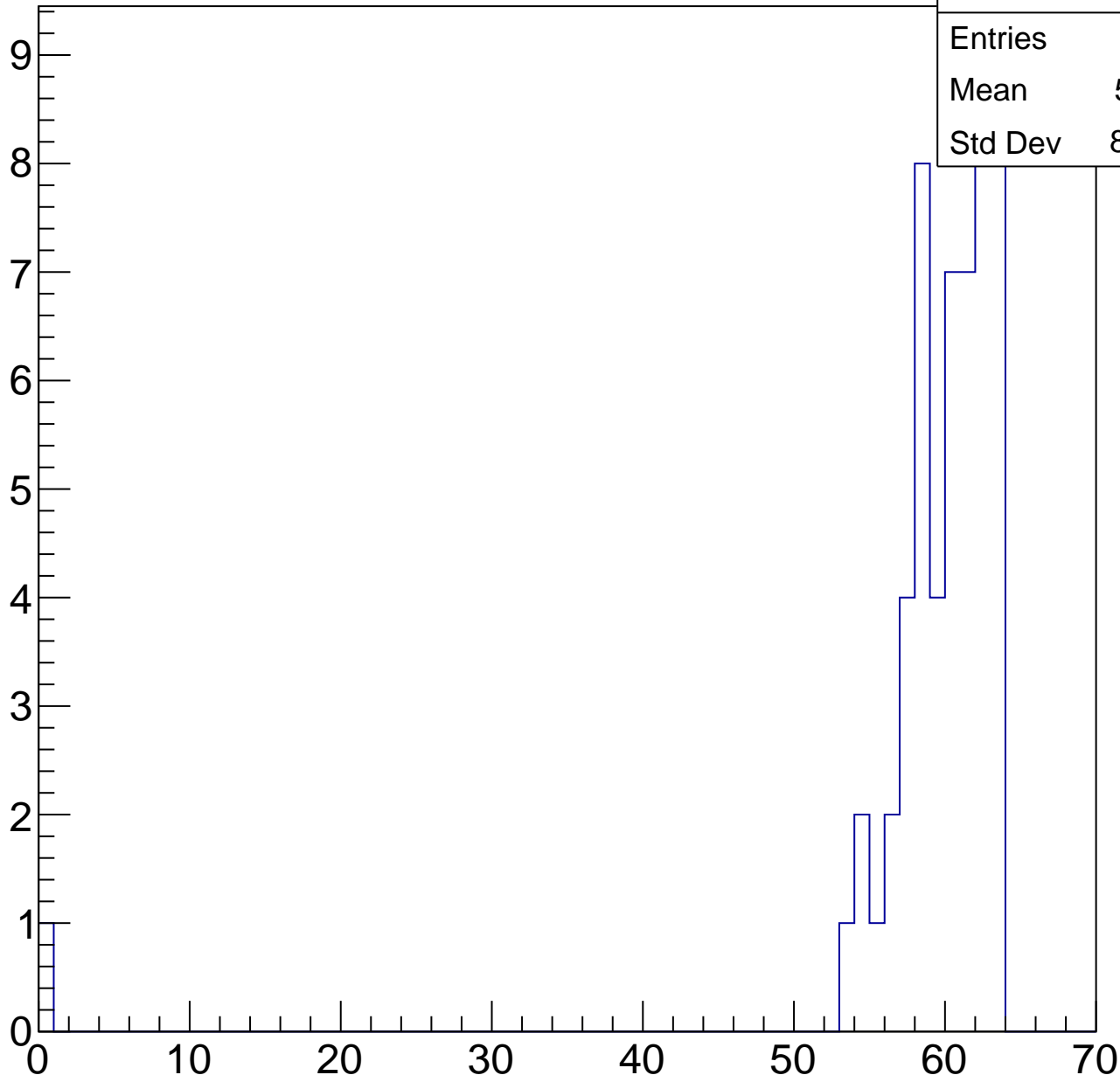
calib_packv5_041523_1651.root, FC#0, port C2

Entry

9
8
7
6
5
4
3
2
1
0

Entries	54
Mean	58.61
Std Dev	8.456

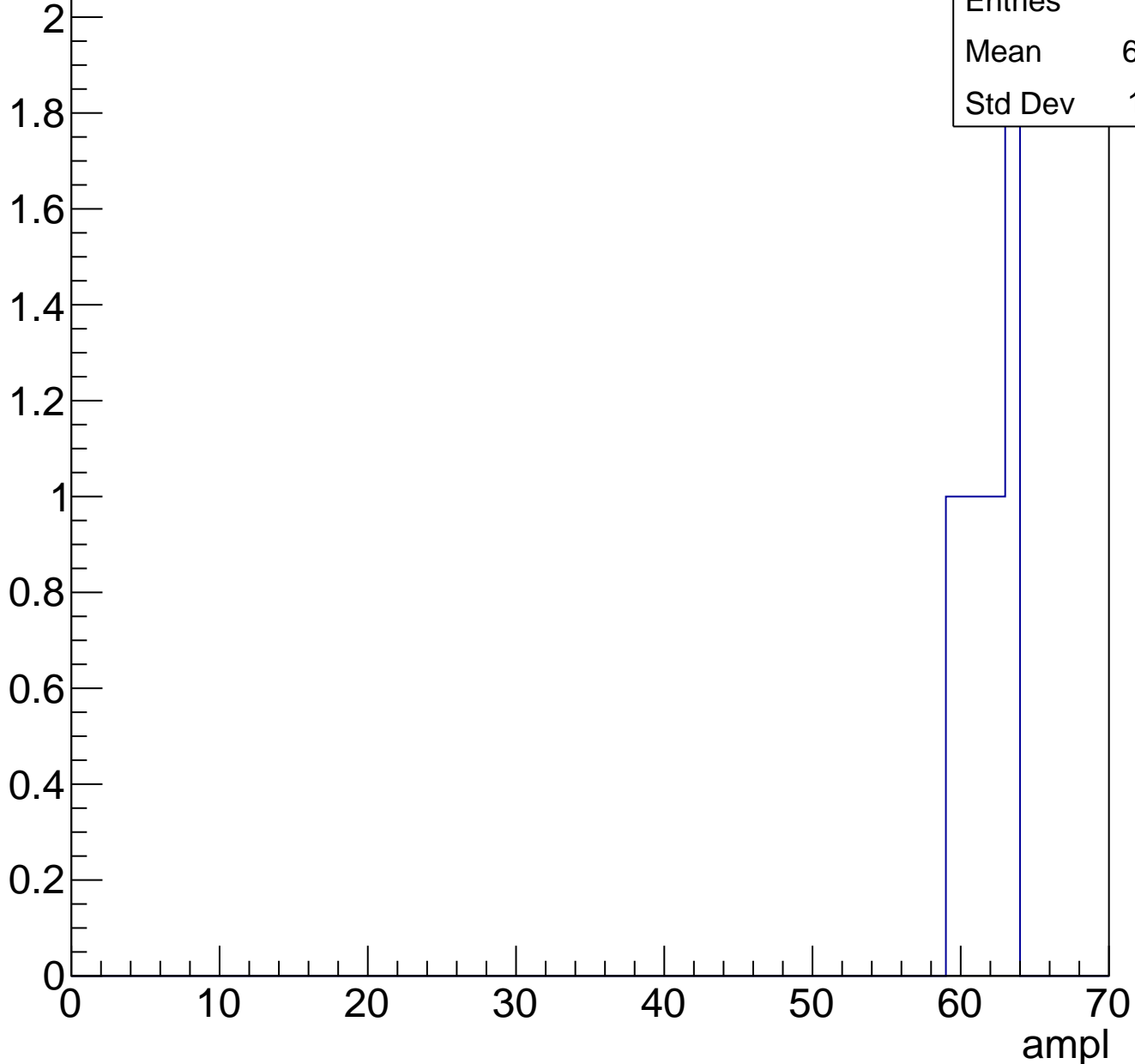
ampl



B1L103S, U23-ch89, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch89, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

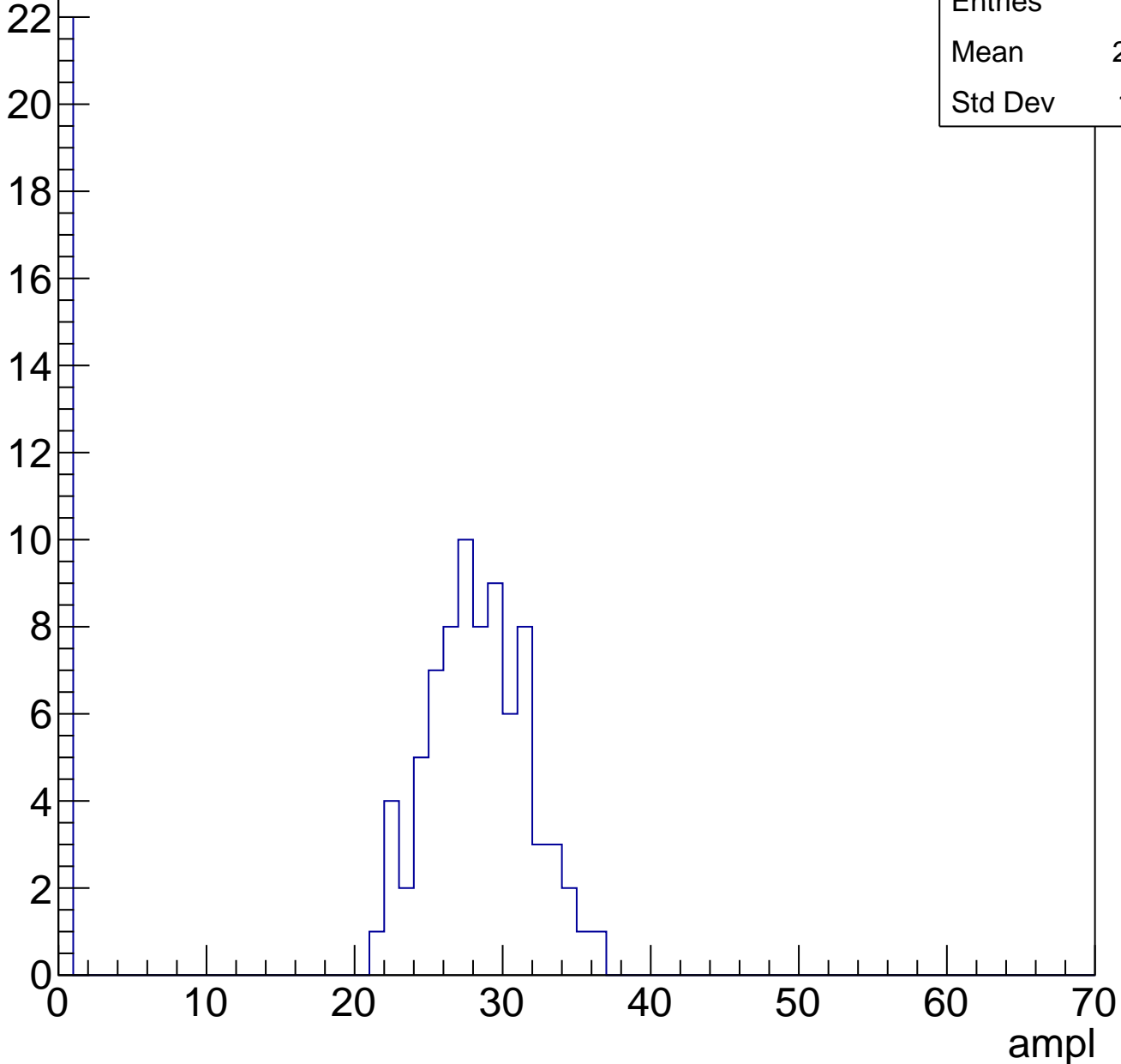
Entries	19
Mean	0
Std Dev	0

B1L103S, U23-ch90, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	100
Mean	21.75
Std Dev	11.91

Entry

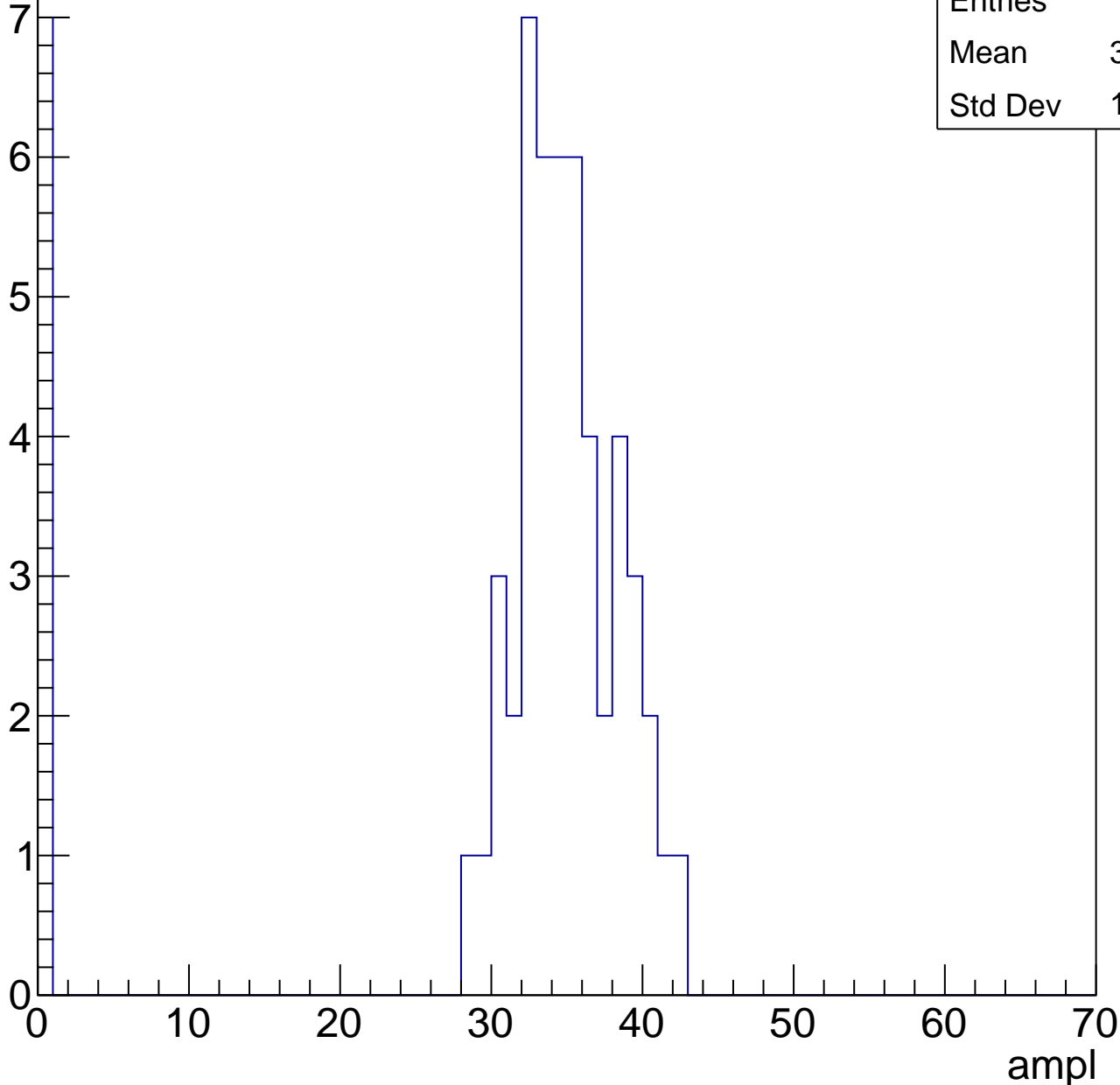


B1L103S, U23-ch90, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	56
Mean	30.27
Std Dev	11.83



B1L103S, U23-ch90, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	90
Mean	35.42
Std Dev	13.69

Entry

10

8

6

4

2

0

0

10

20

30

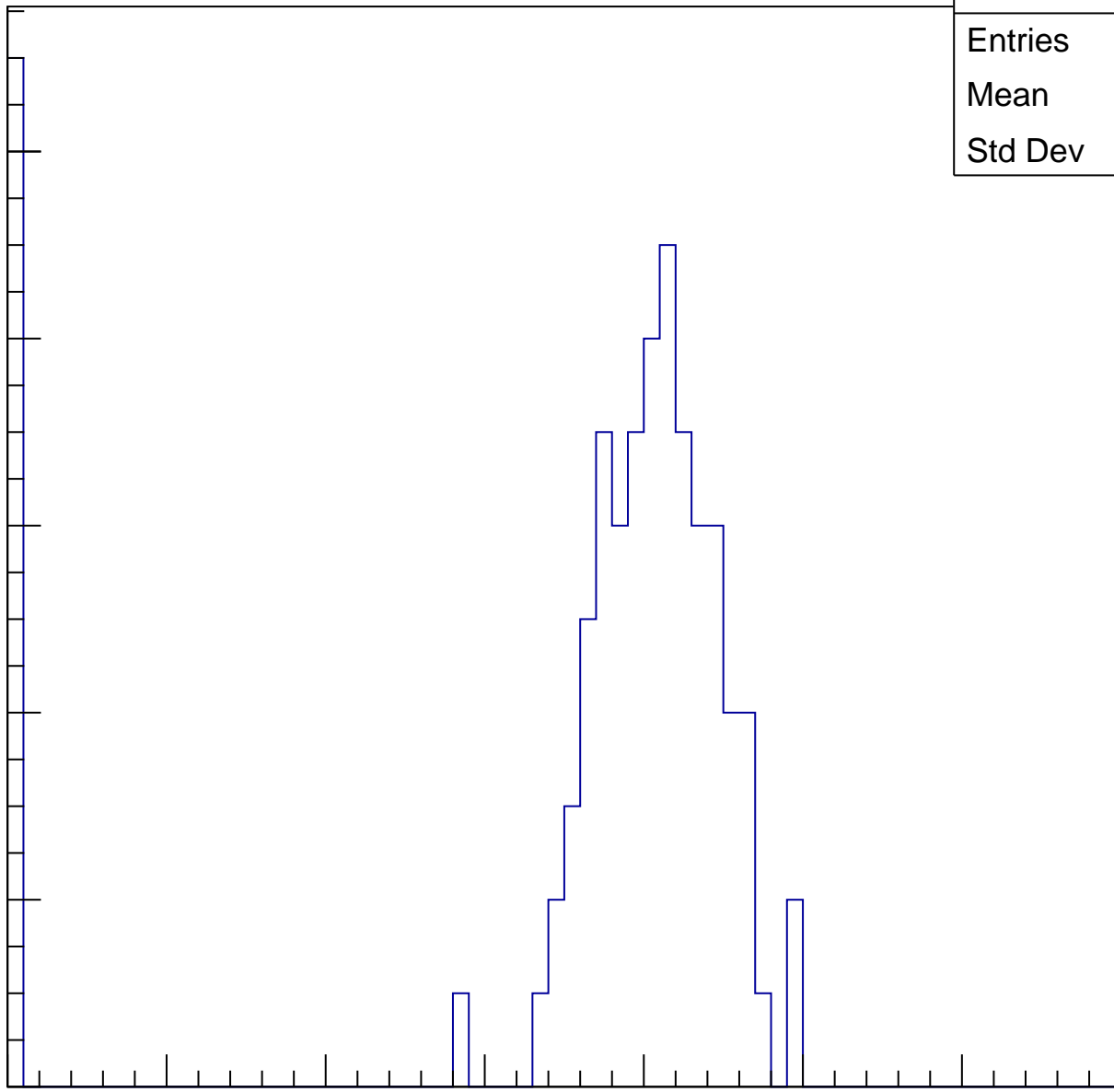
40

50

60

70

ampl

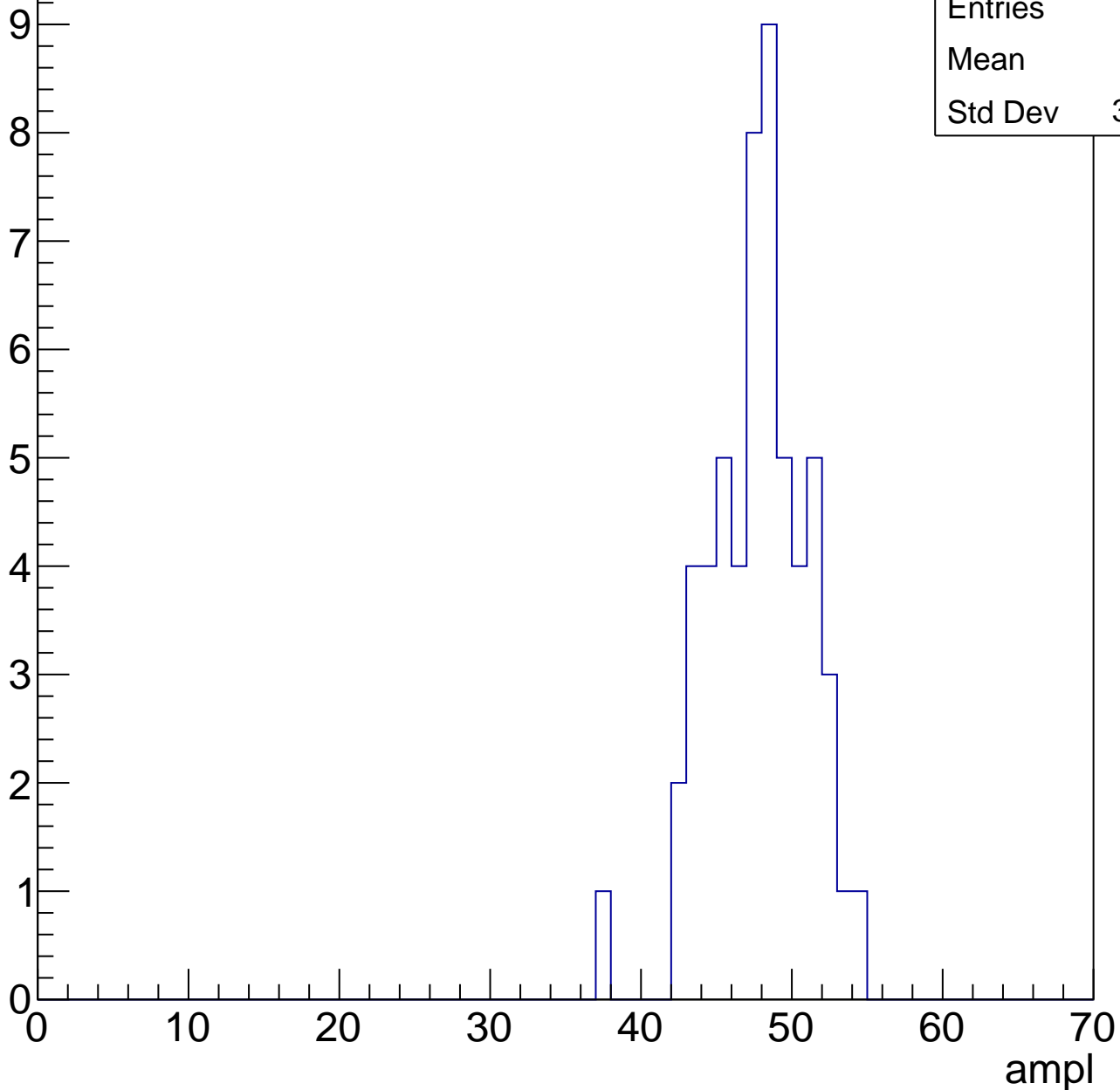


B1L103S, U23-ch90, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	56
Mean	47.3
Std Dev	3.201

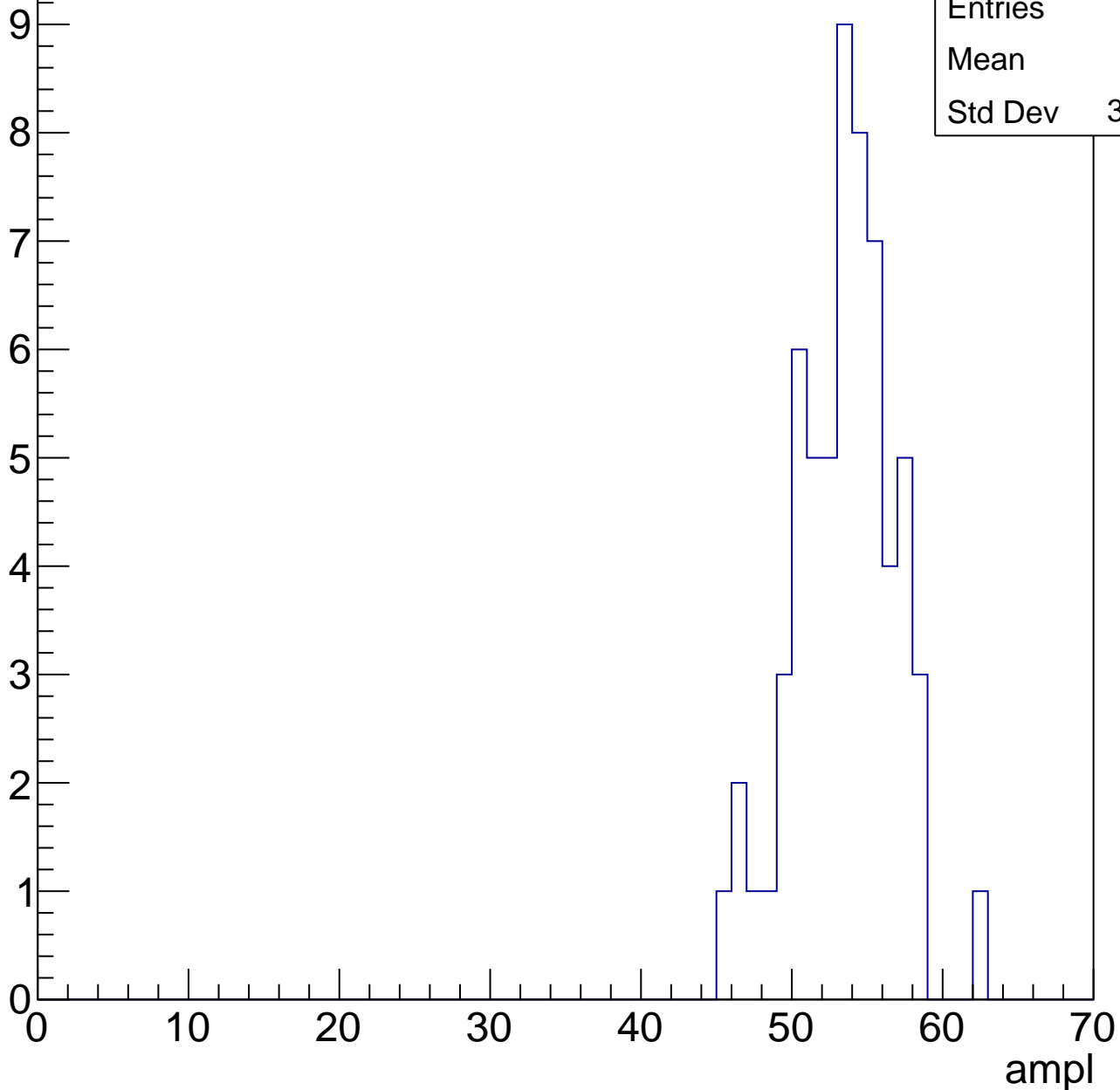


B1L103S, U23-ch90, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

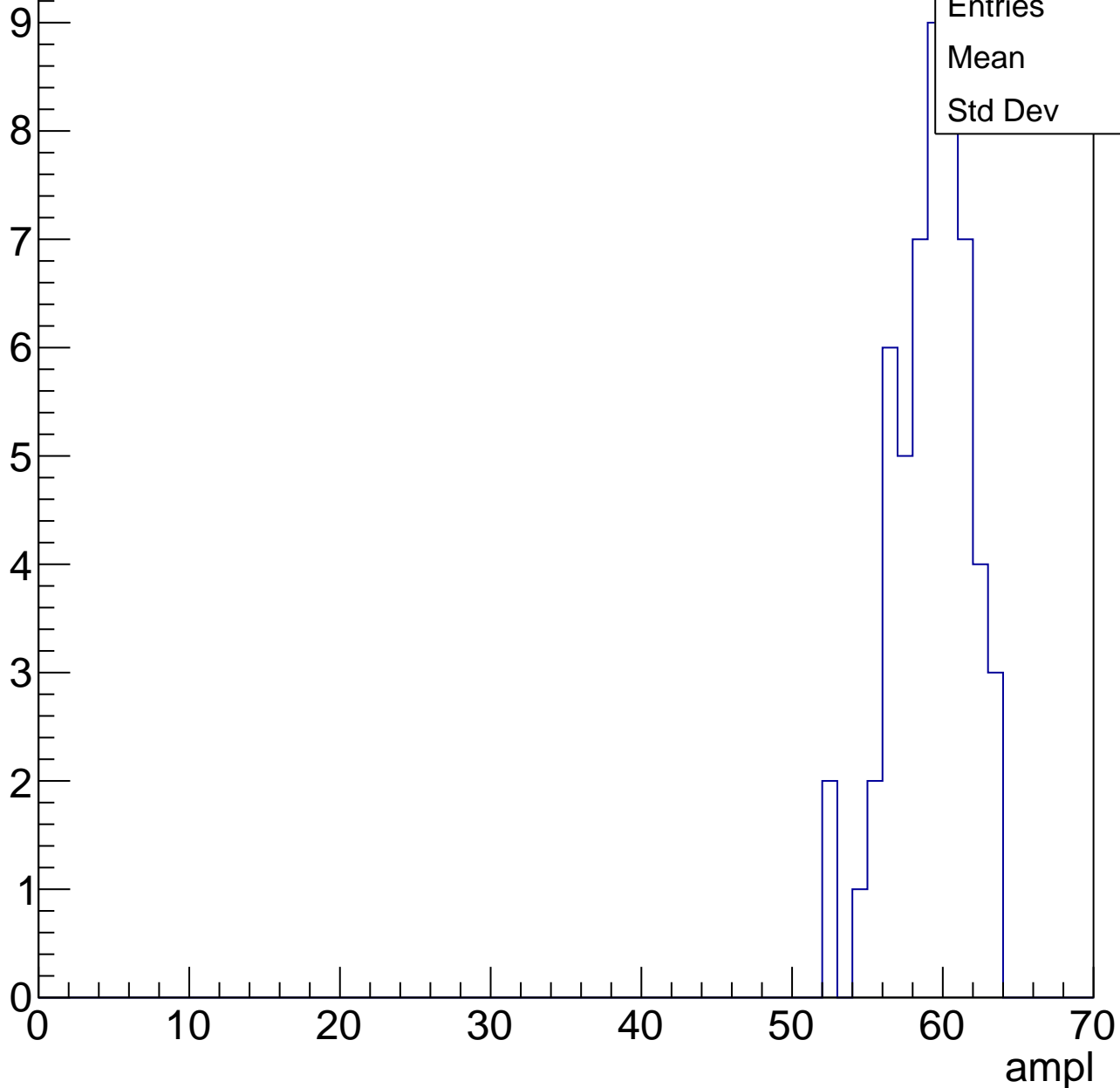
Entries	61
Mean	53
Std Dev	3.284



B1L103S, U23-ch90, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

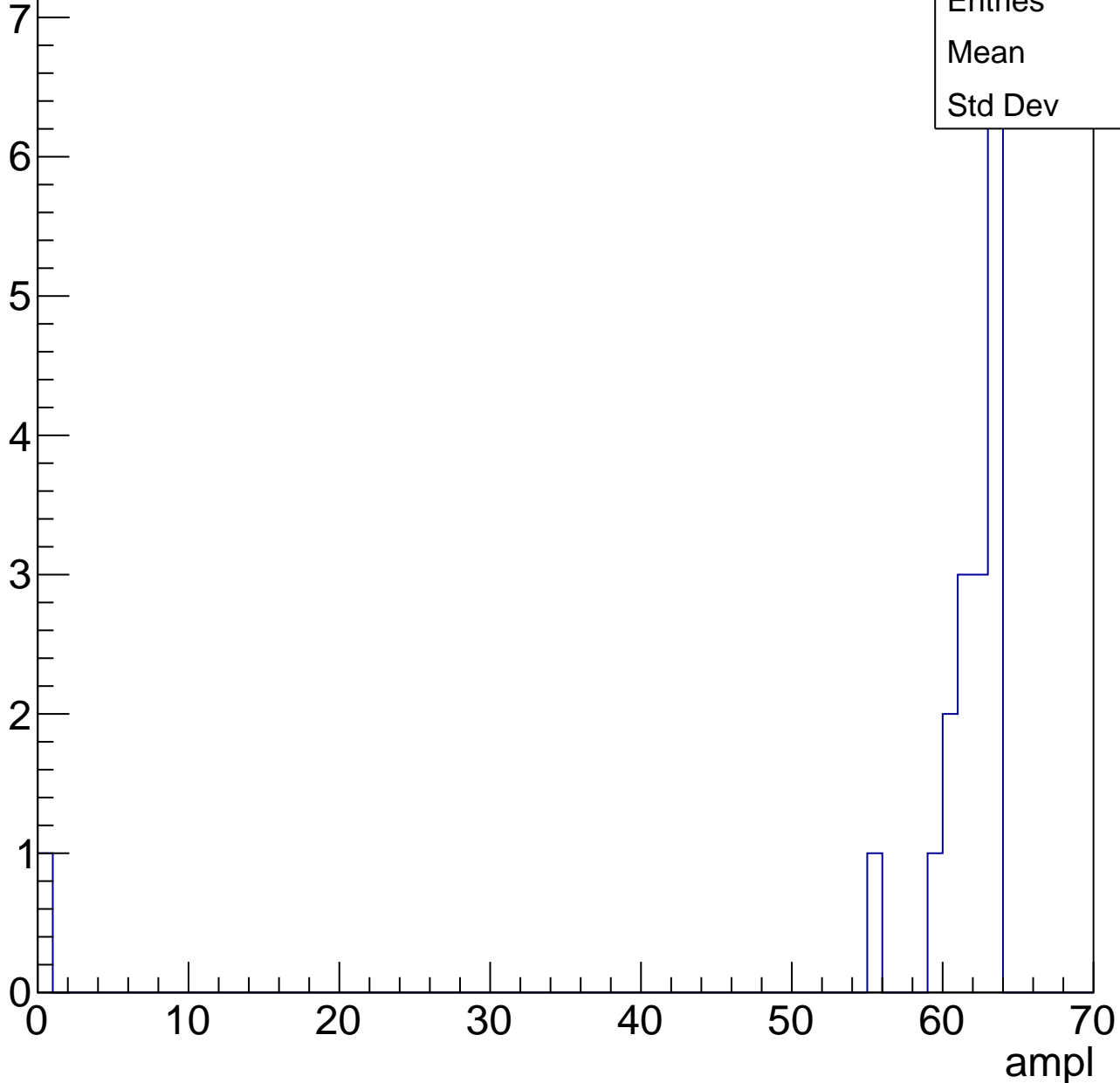


B1L103S, U23-ch90, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	18
Mean	58
Std Dev	14.2

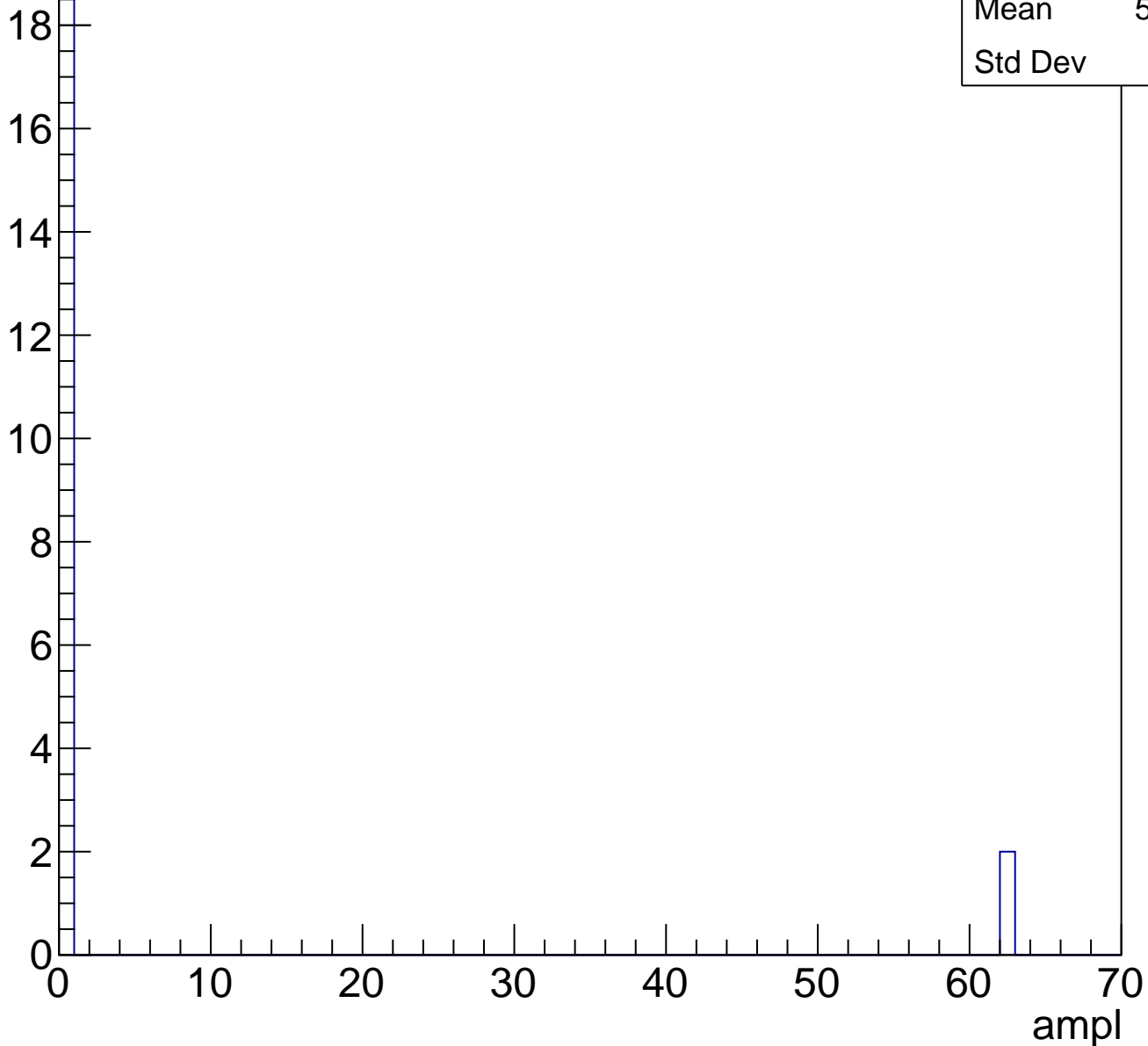


B1L103S, U23-ch90, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	21
Mean	5.905
Std Dev	18.2

Entry



B1L103S, U23-ch91, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	74
Mean	22.97
Std Dev	11.04

Entry

12

10

8

6

4

2

0

0

10

20

30

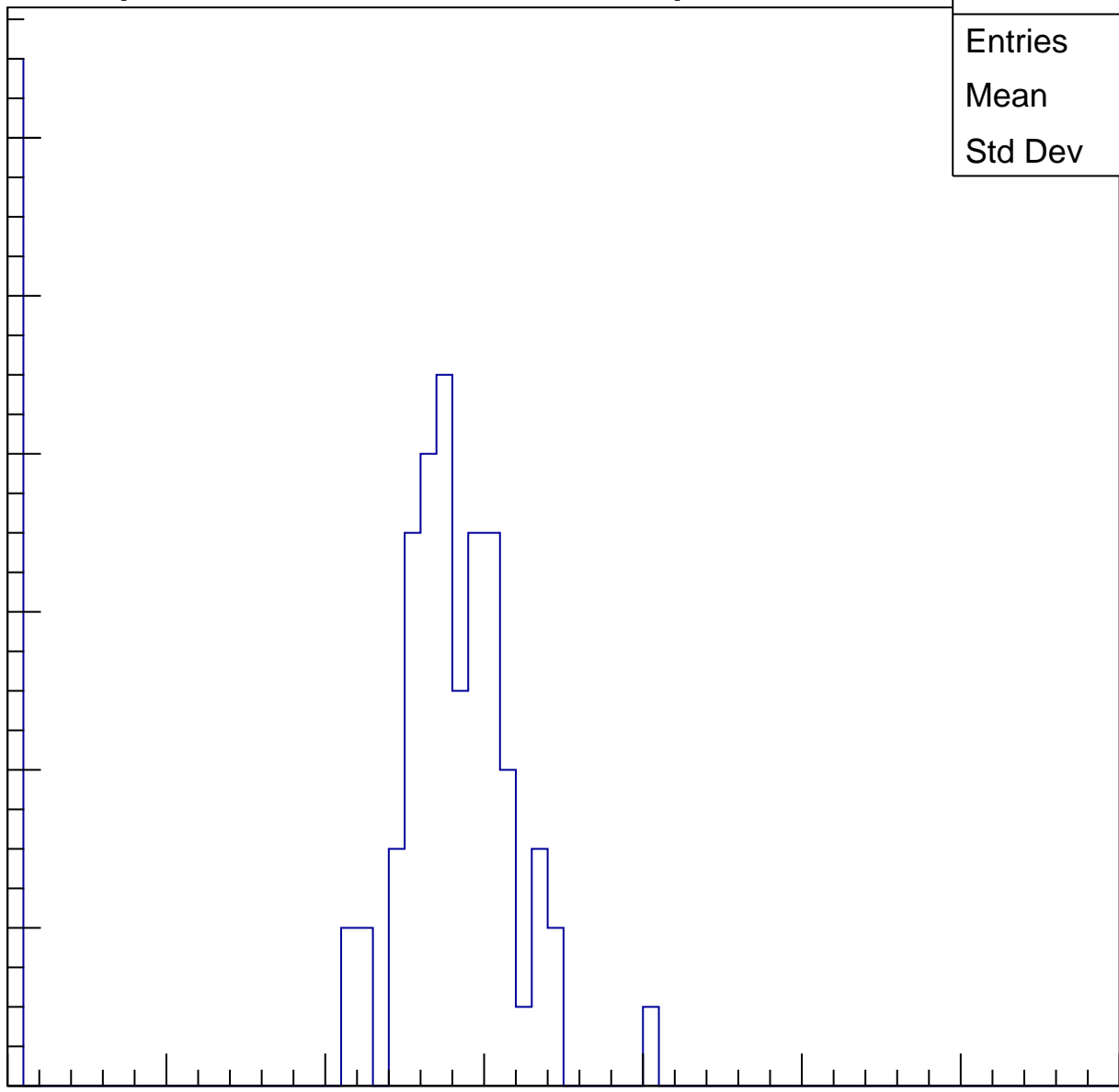
40

50

60

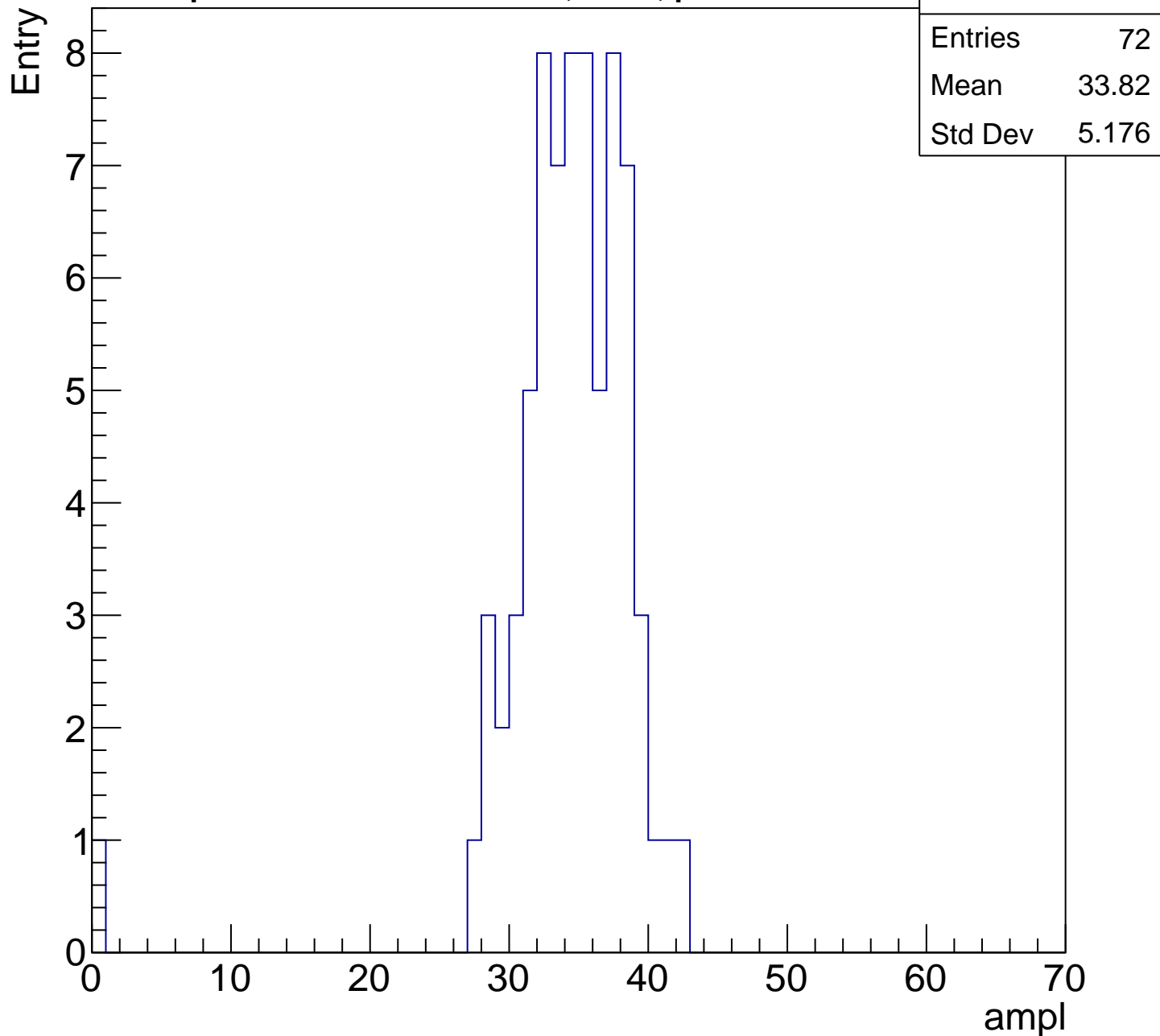
70

ampl



B1L103S, U23-ch91, adc1

calib_packv5_041523_1651.root, FC#0, port C2

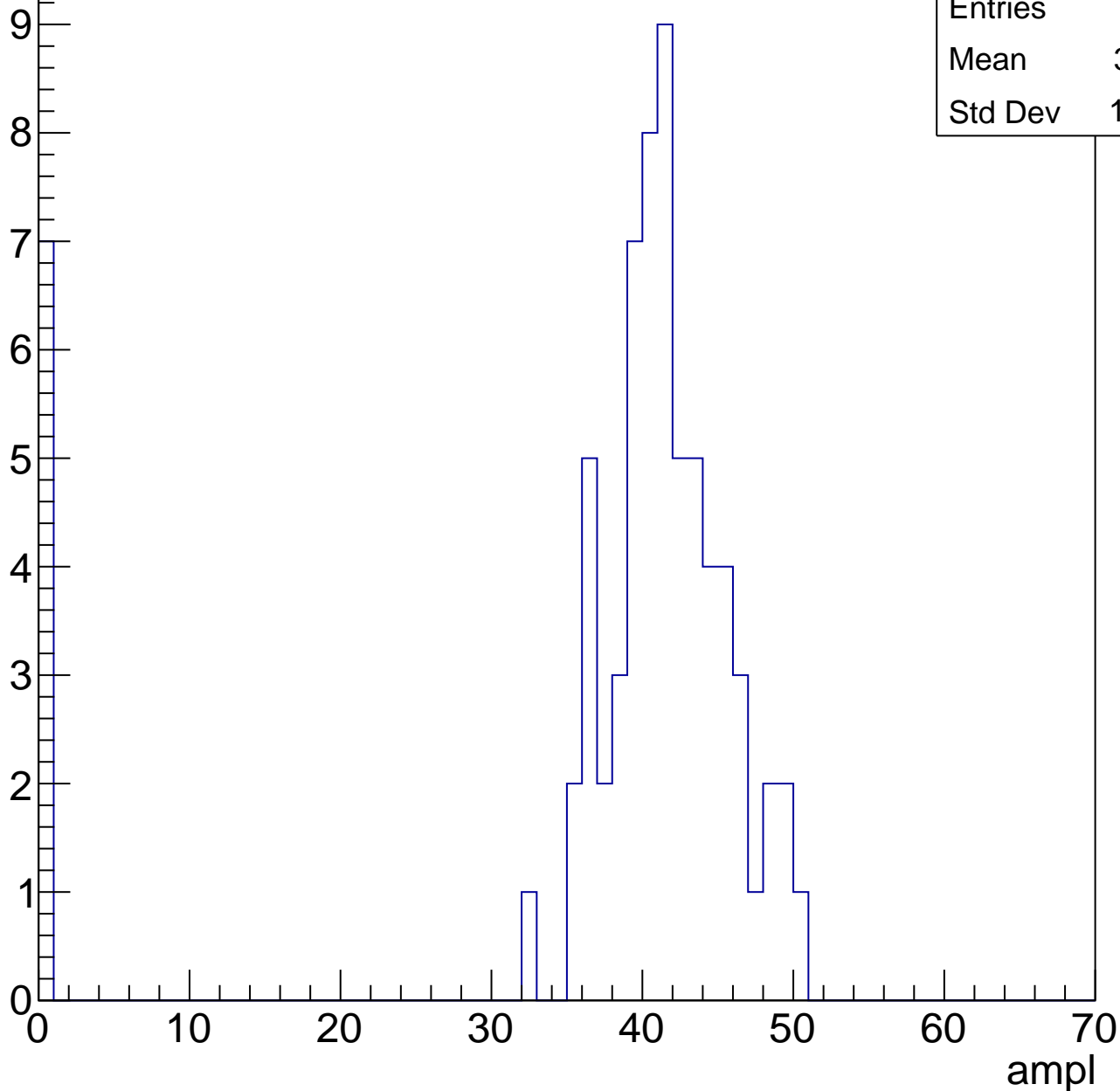


B1L103S, U23-ch91, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

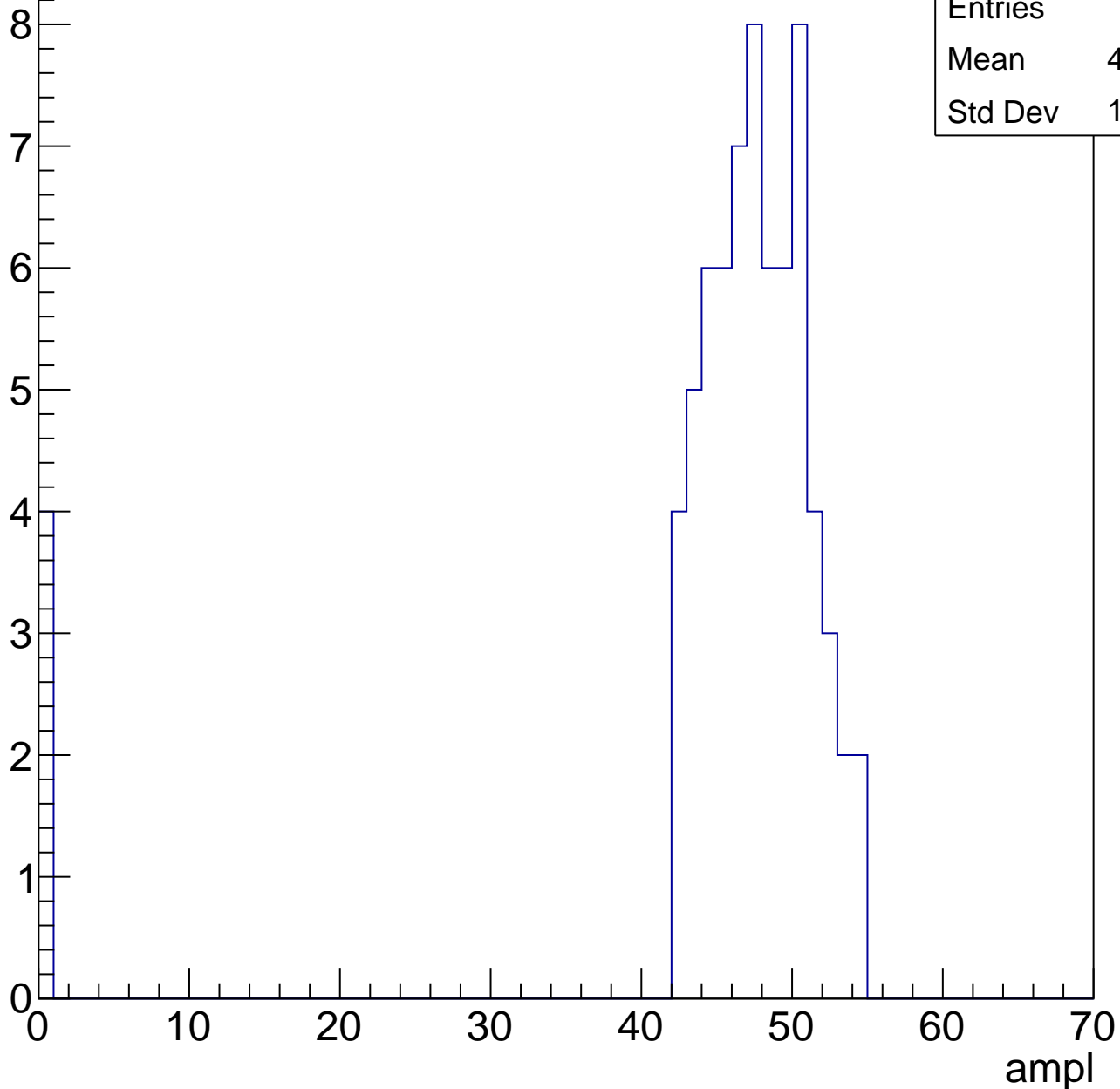
Entries	71
Mean	37.21
Std Dev	12.82



B1L103S, U23-ch91, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

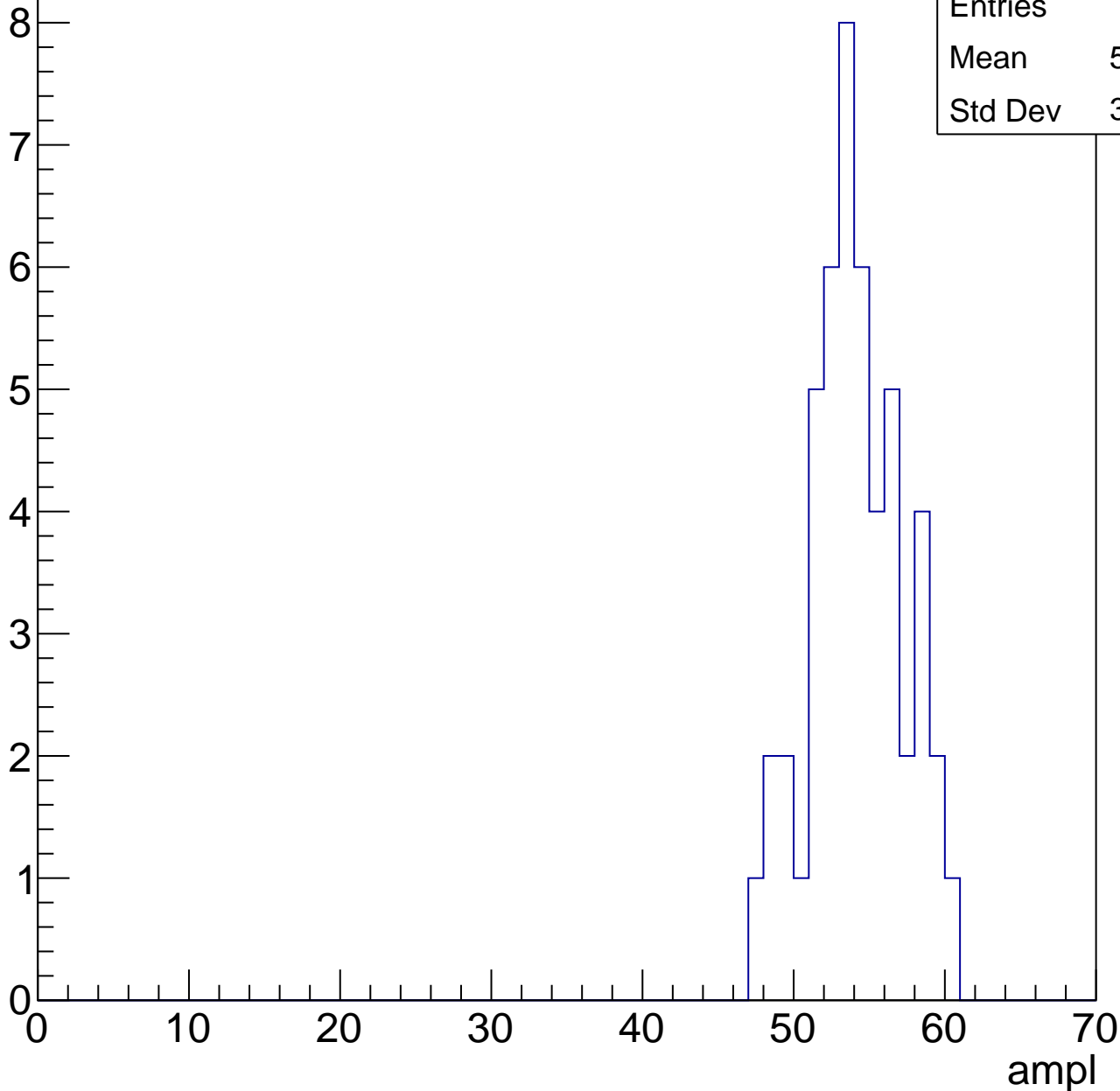


B1L103S, U23-ch91, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	49
Mean	53.67
Std Dev	3.033

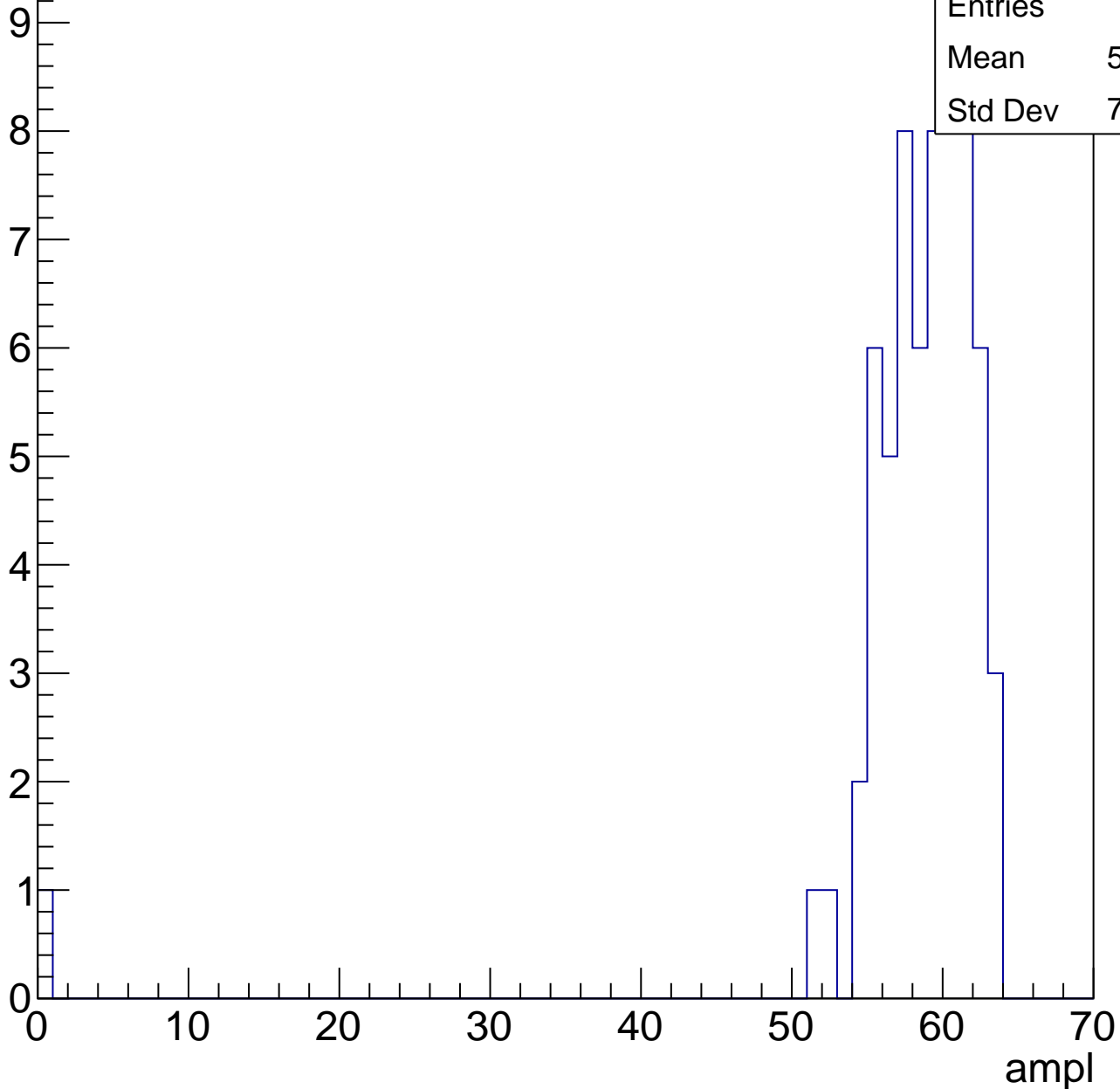


B1L103S, U23-ch91, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	57.59
Std Dev	7.745

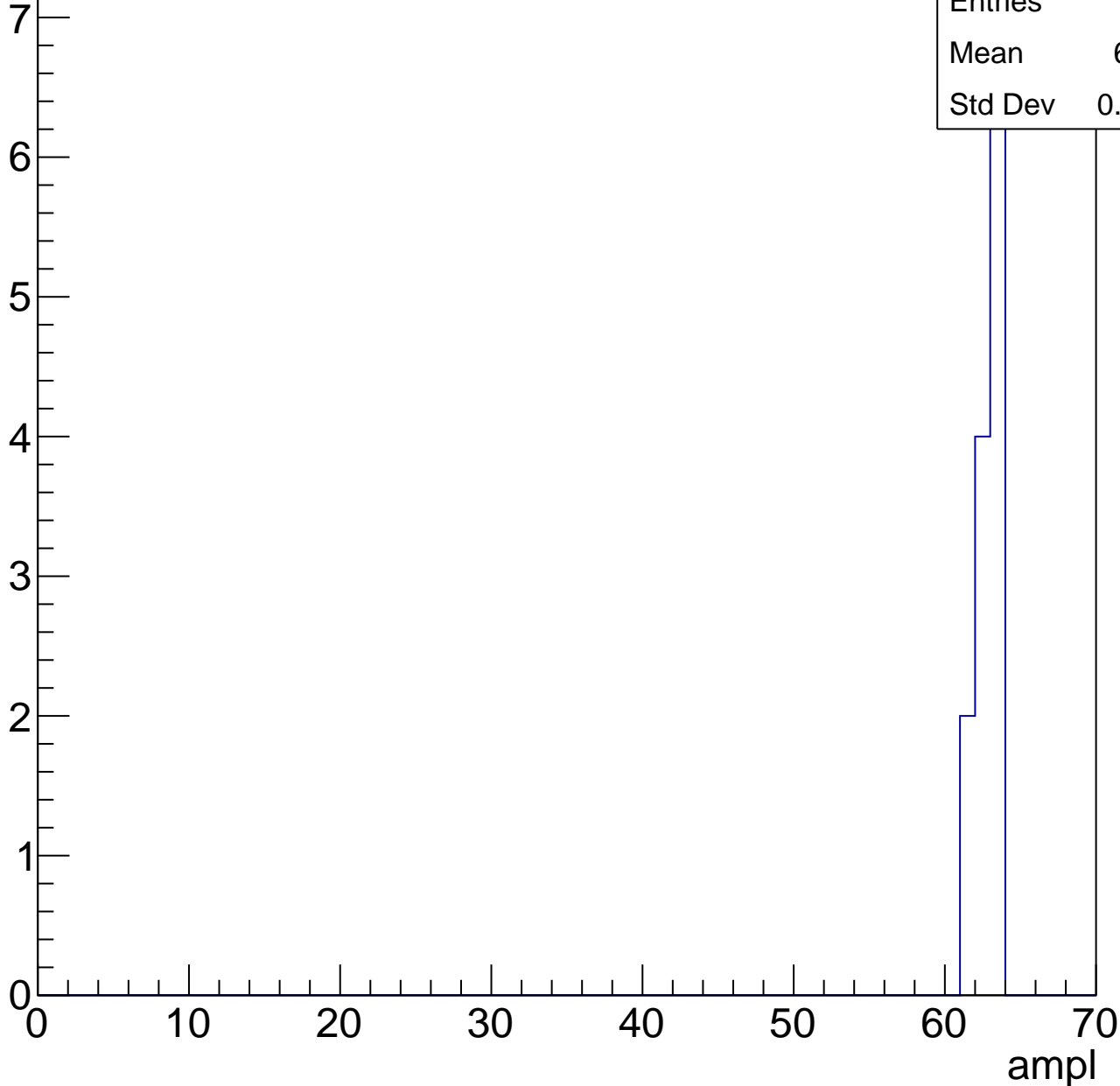


B1L103S, U23-ch91, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	13
Mean	62.38
Std Dev	0.7378

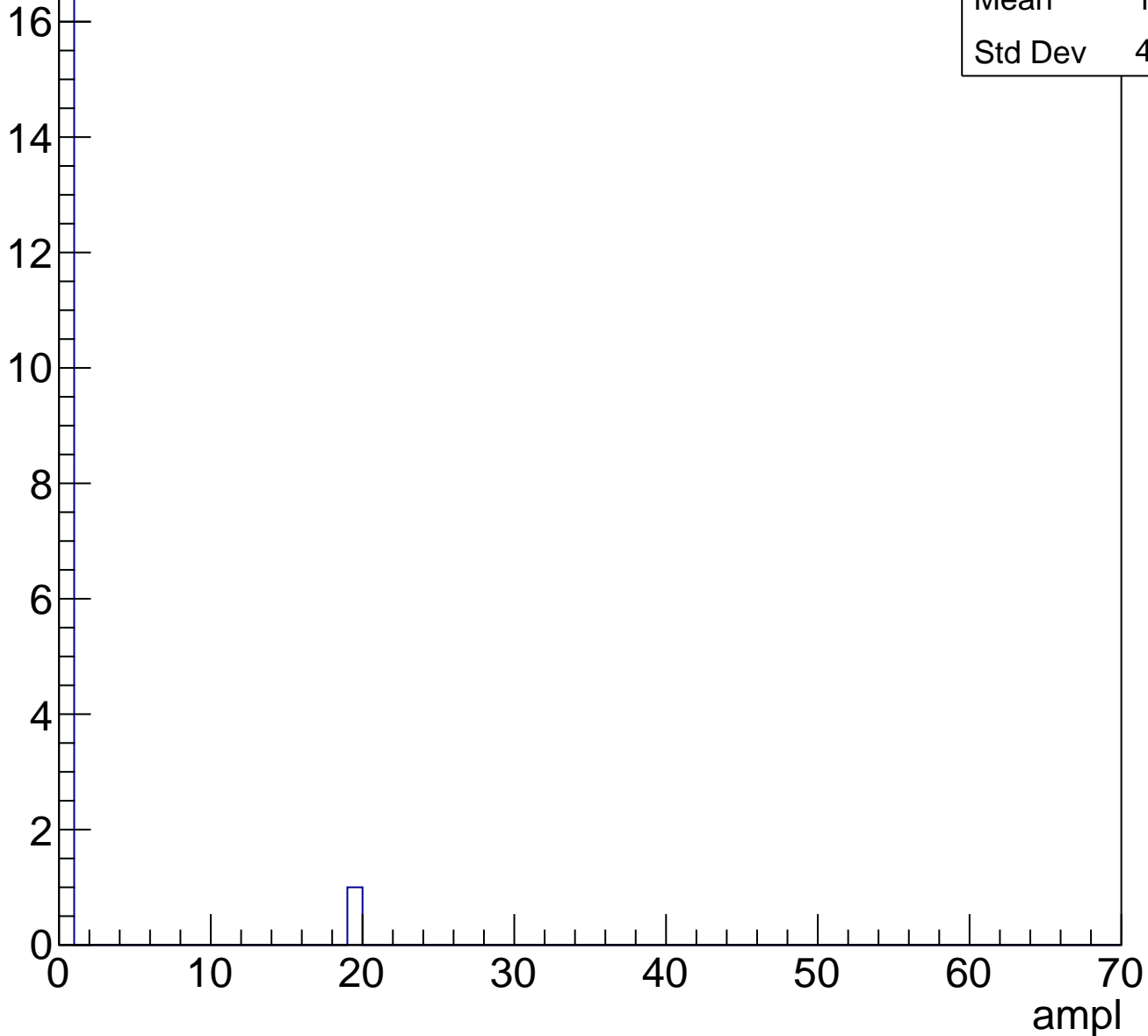


B1L103S, U23-ch91, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	18
Mean	1.056
Std Dev	4.352

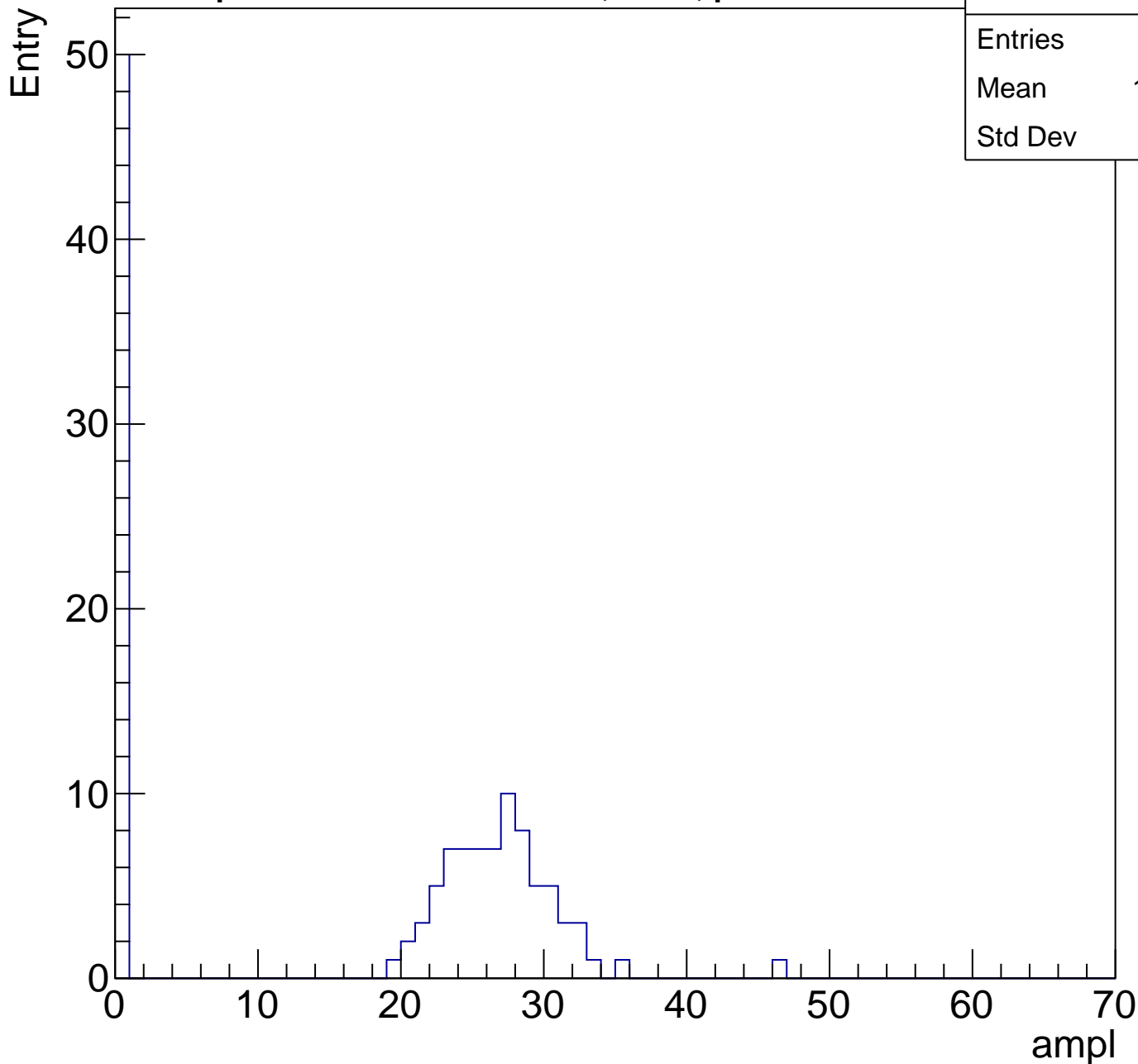
Entry



B1L103S, U23-ch92, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	126
Mean	15.95
Std Dev	13.31

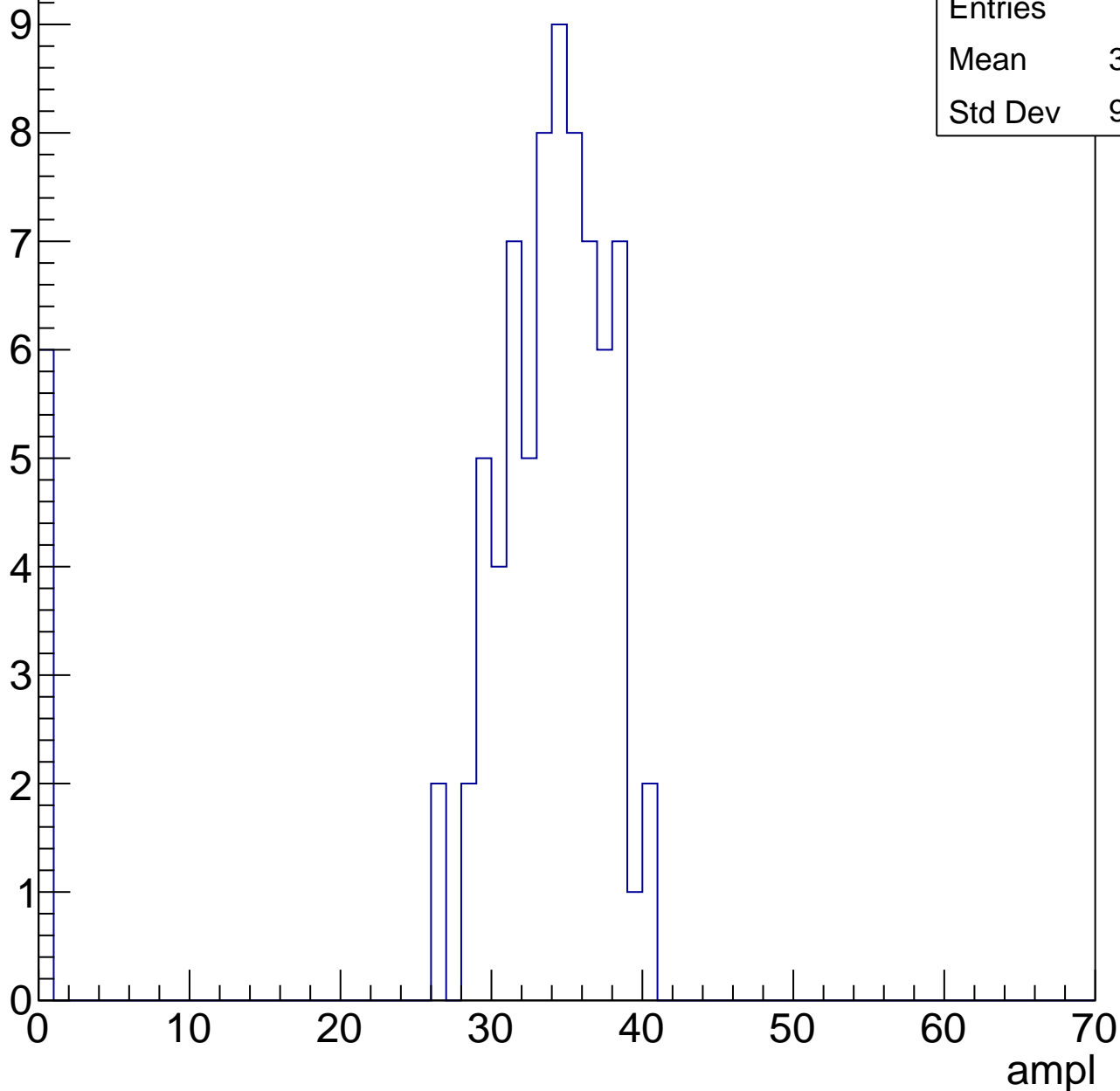


B1L103S, U23-ch92, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

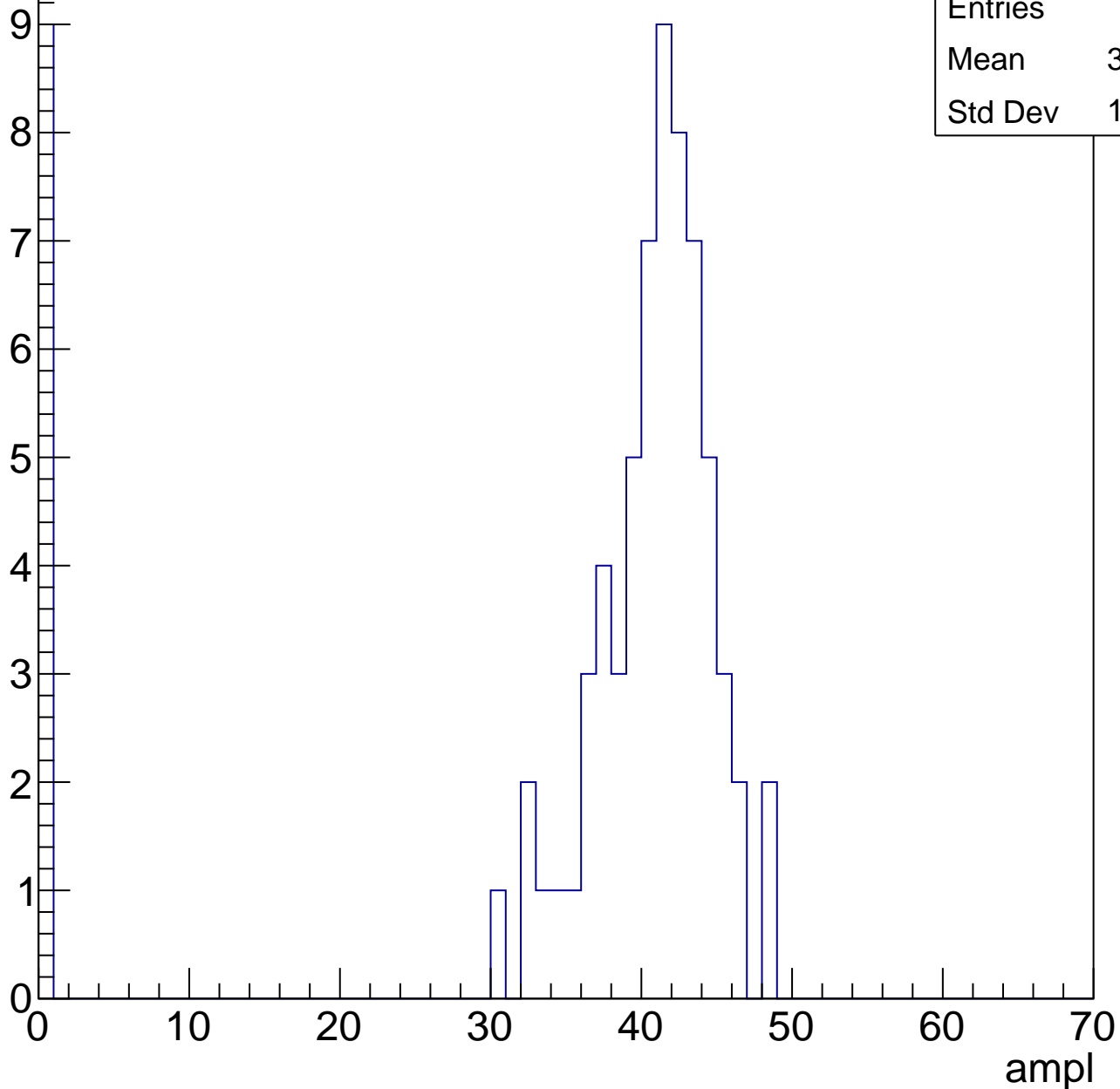
Entries	79
Mean	31.13
Std Dev	9.455



B1L103S, U23-ch92, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry



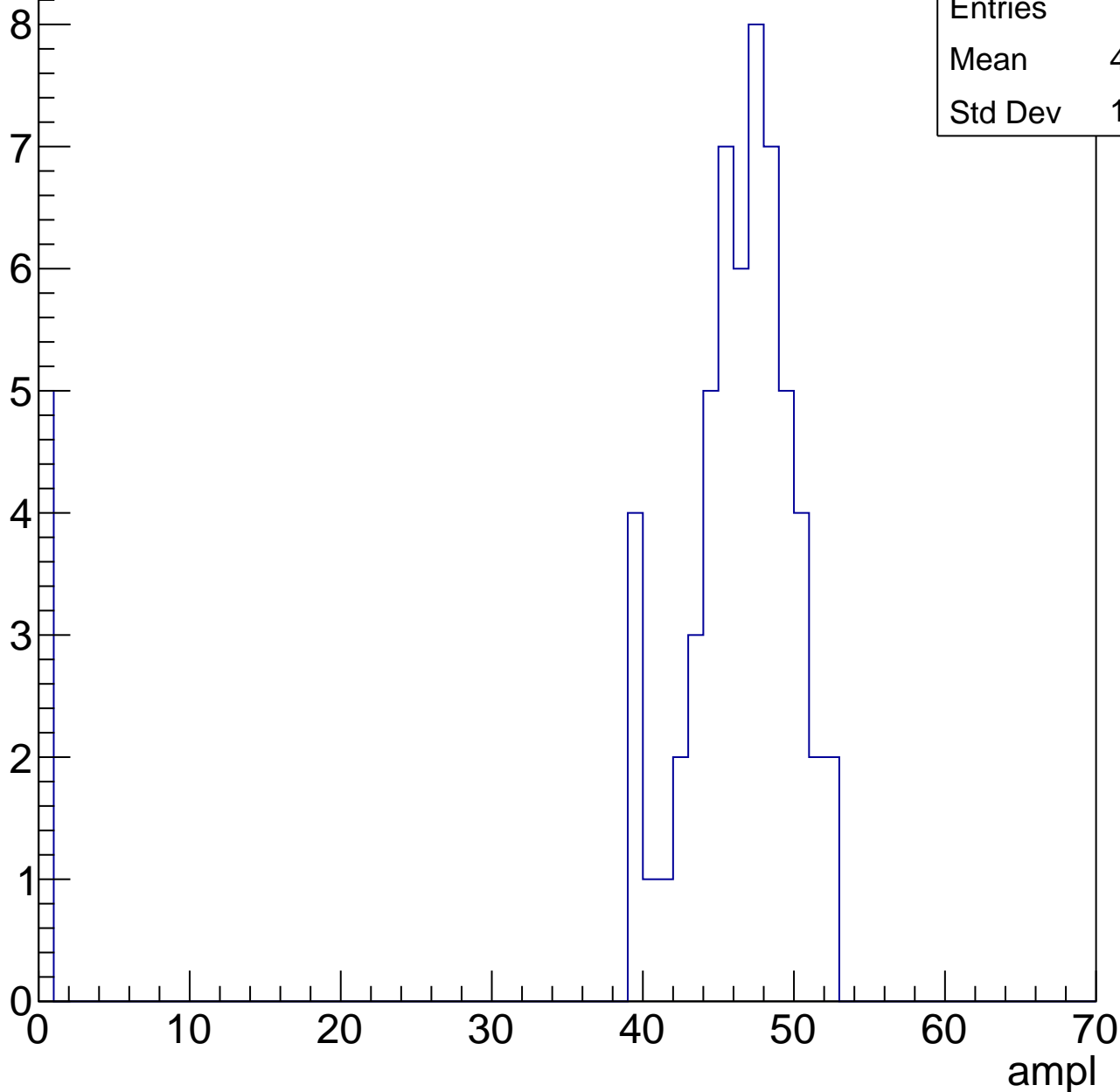
Entries	73
Mean	35.48
Std Dev	13.75

B1L103S, U23-ch92, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	42.32
Std Dev	12.92

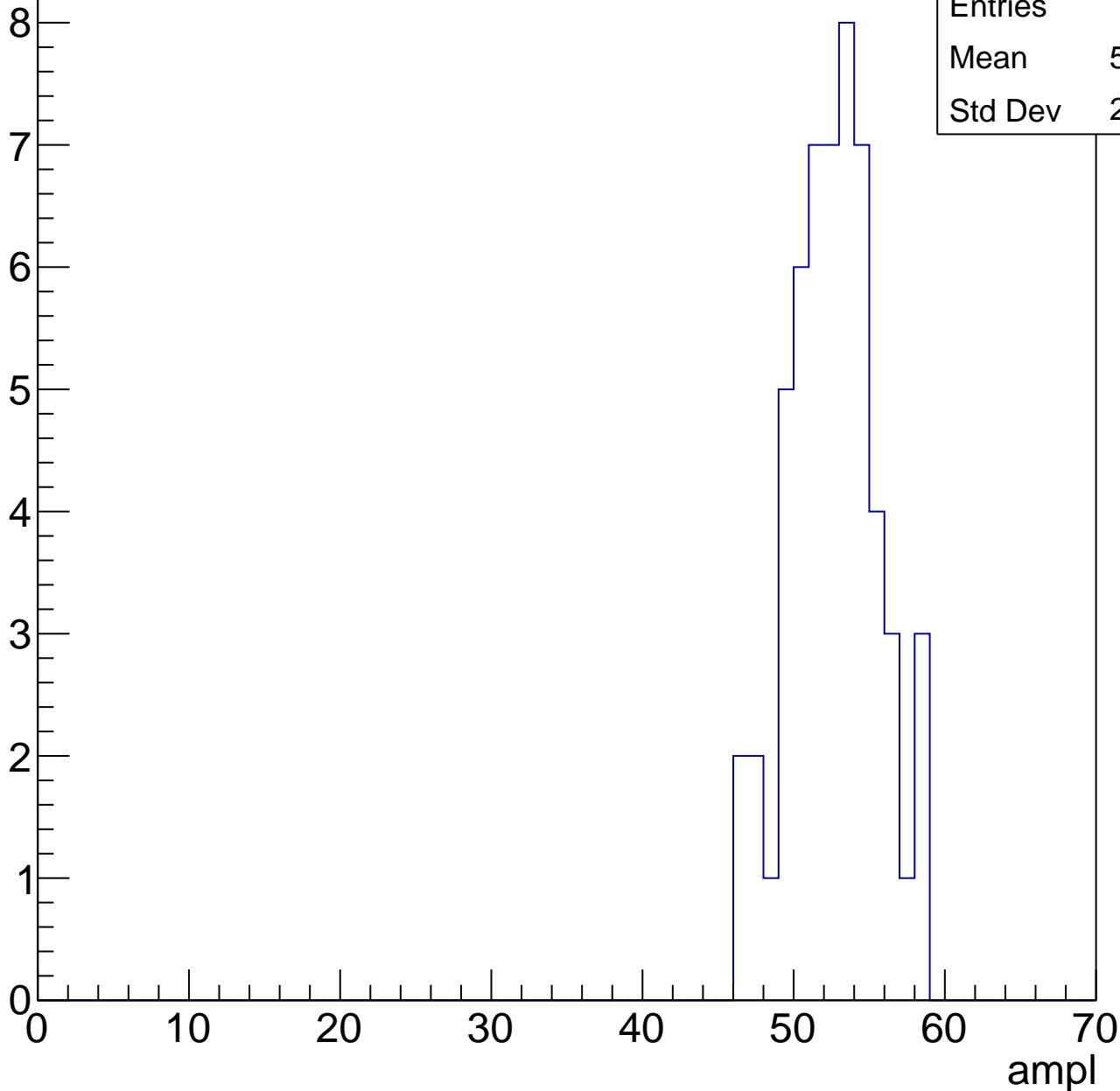


B1L103S, U23-ch92, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	56
Mean	52.16
Std Dev	2.883



B1L103S, U23-ch92, adc5

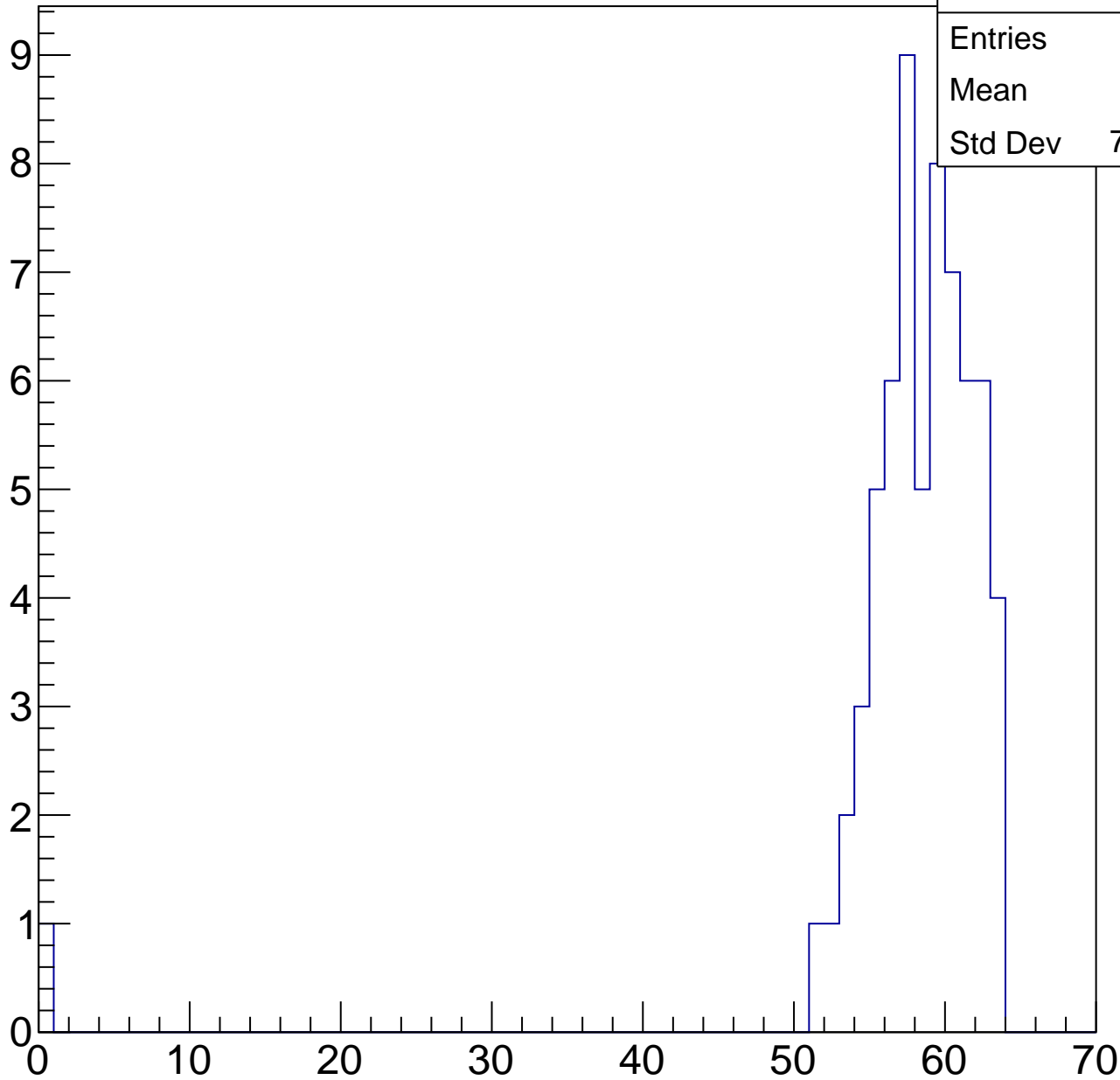
calib_packv5_041523_1651.root, FC#0, port C2

Entry

9
8
7
6
5
4
3
2
1
0

Entries	64
Mean	57.3
Std Dev	7.786

ampl

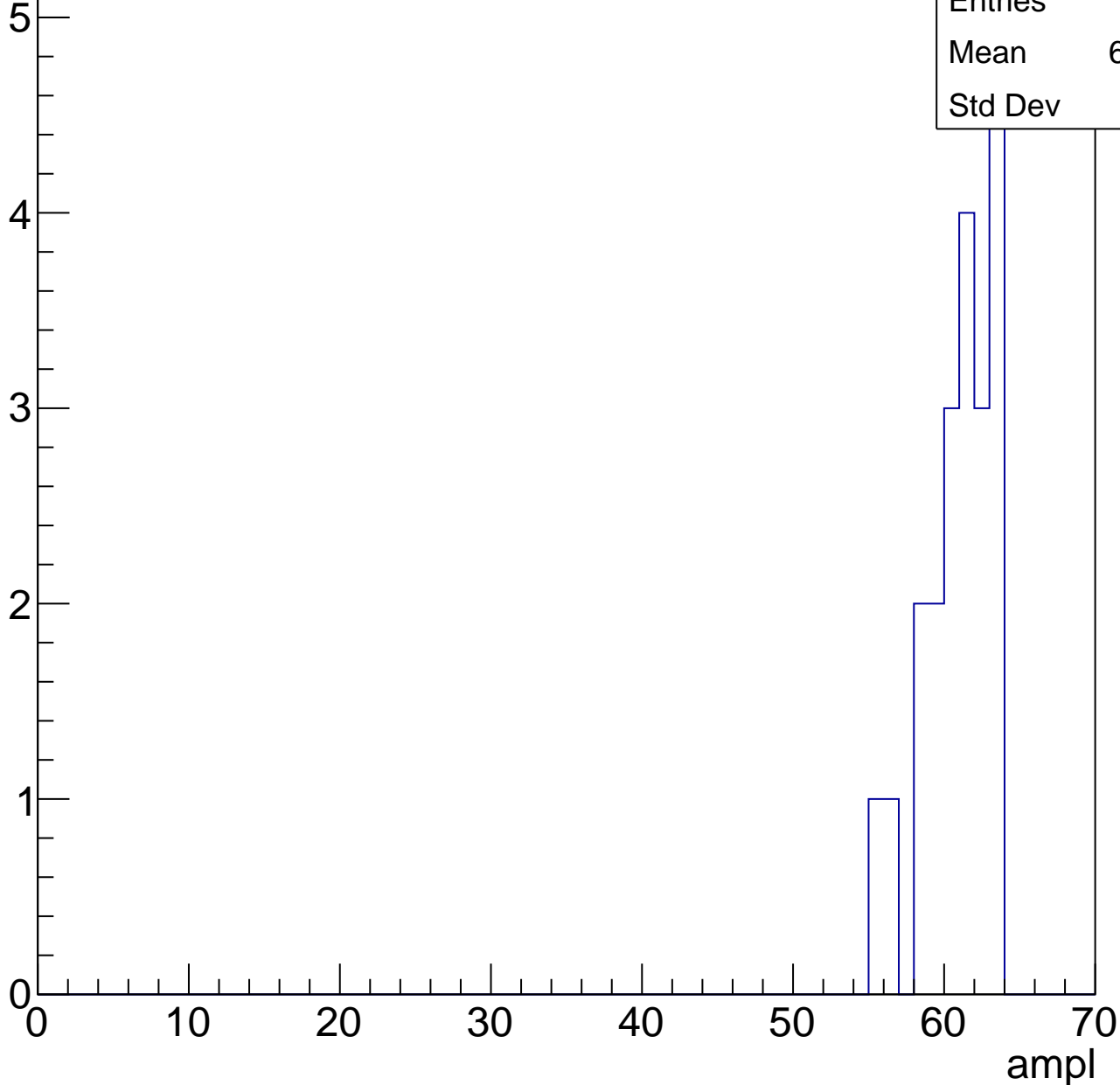


B1L103S, U23-ch92, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	21
Mean	60.48
Std Dev	2.26

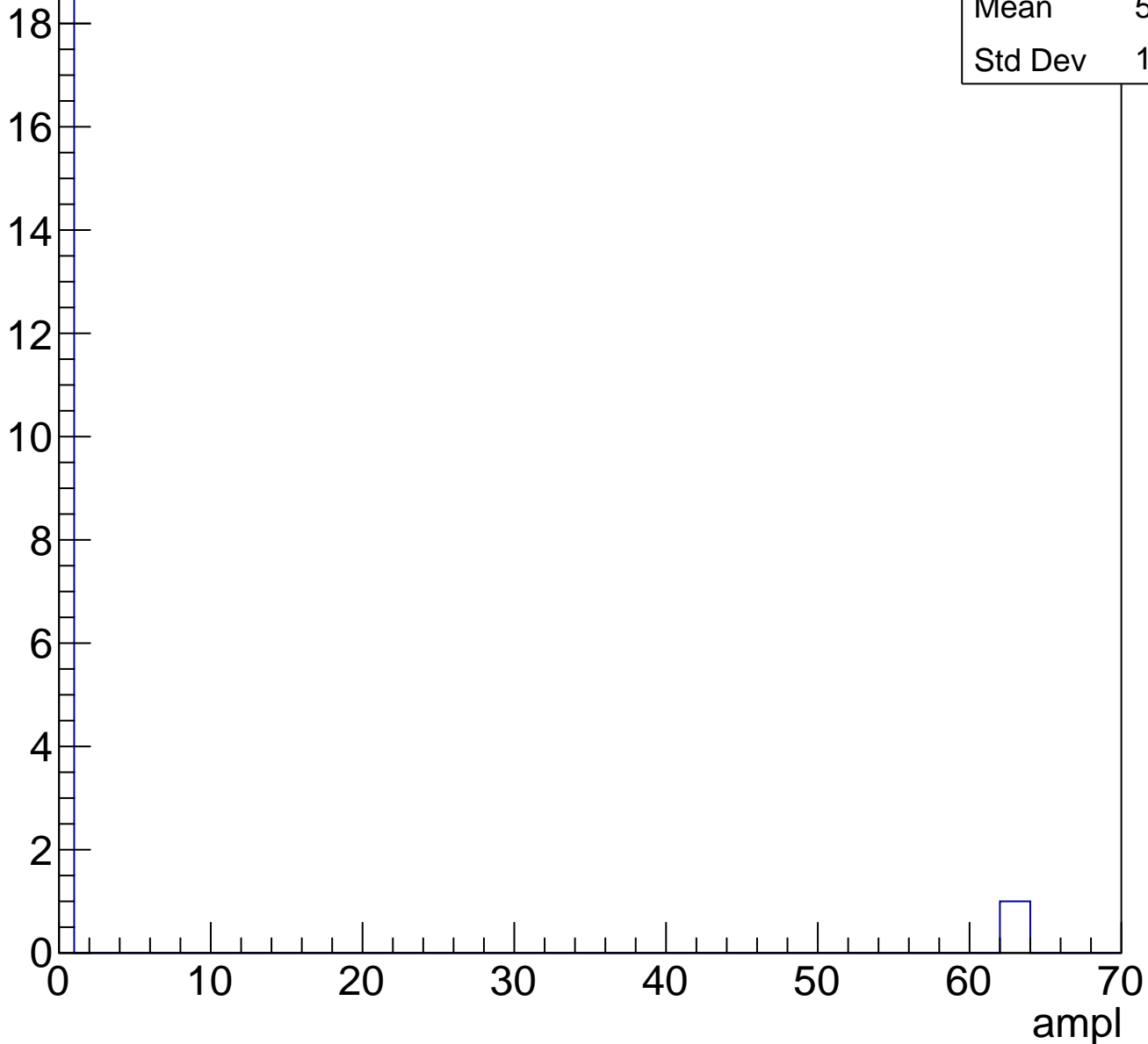


B1L103S, U23-ch92, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	21
Mean	5.952
Std Dev	18.35

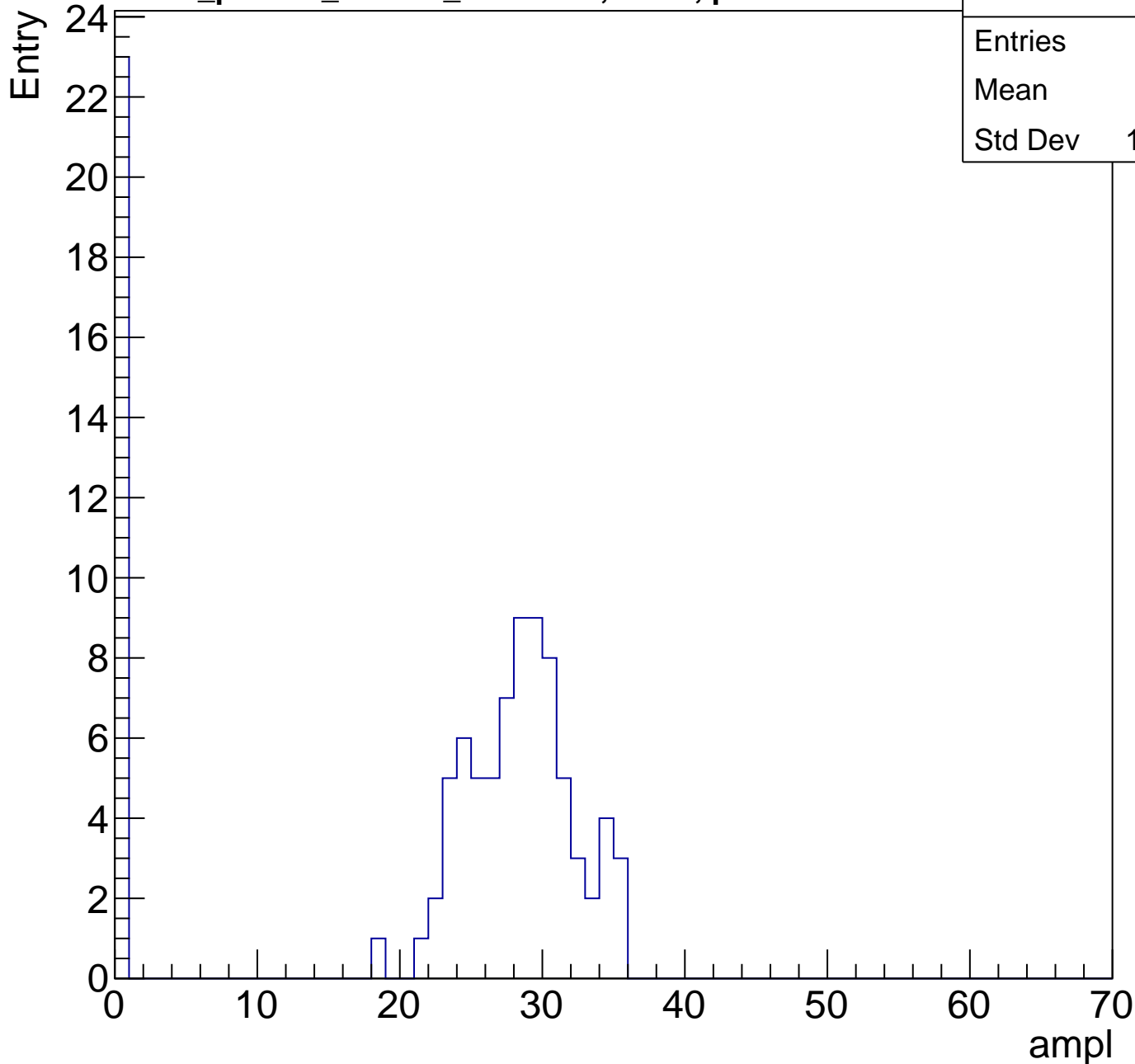
Entry



B1L103S, U23-ch93, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	98
Mean	21.4
Std Dev	12.27



B1L103S, U23-ch93, adc1

calib_packv5_041523_1651.root, FC#0, port C2

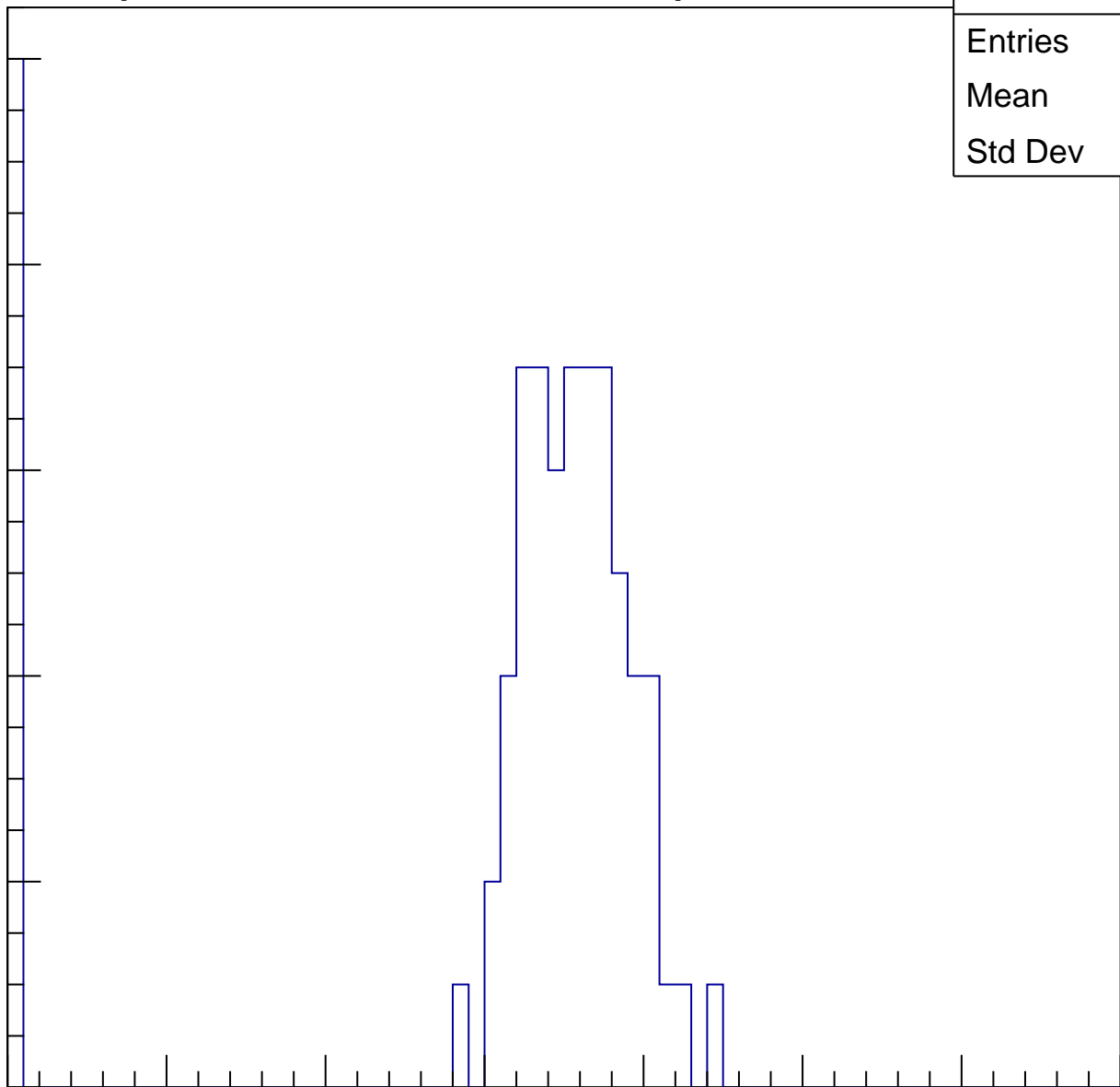
Entries	74
Mean	30.54
Std Dev	12.44

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

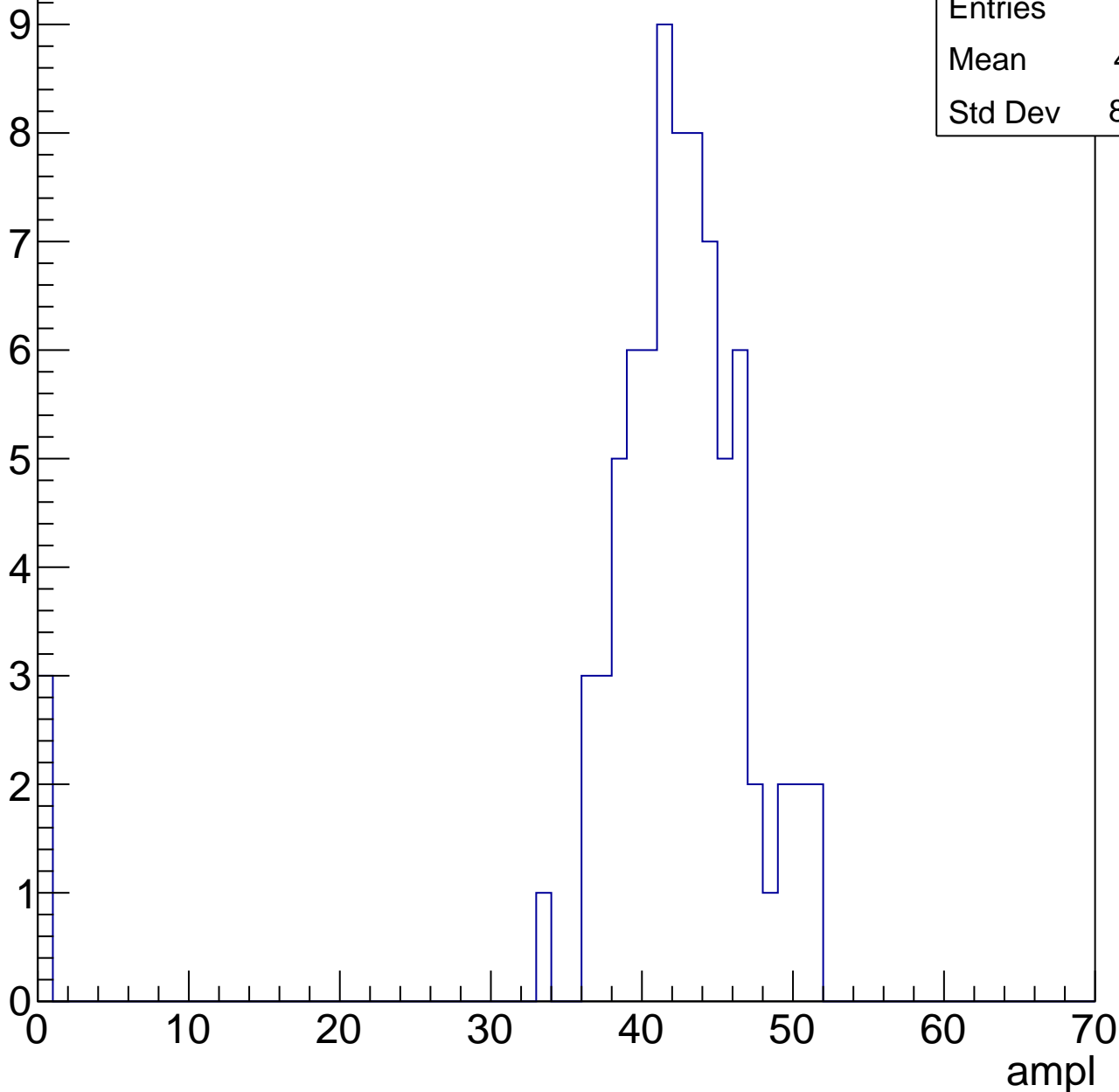


B1L103S, U23-ch93, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	79
Mean	40.71
Std Dev	8.889

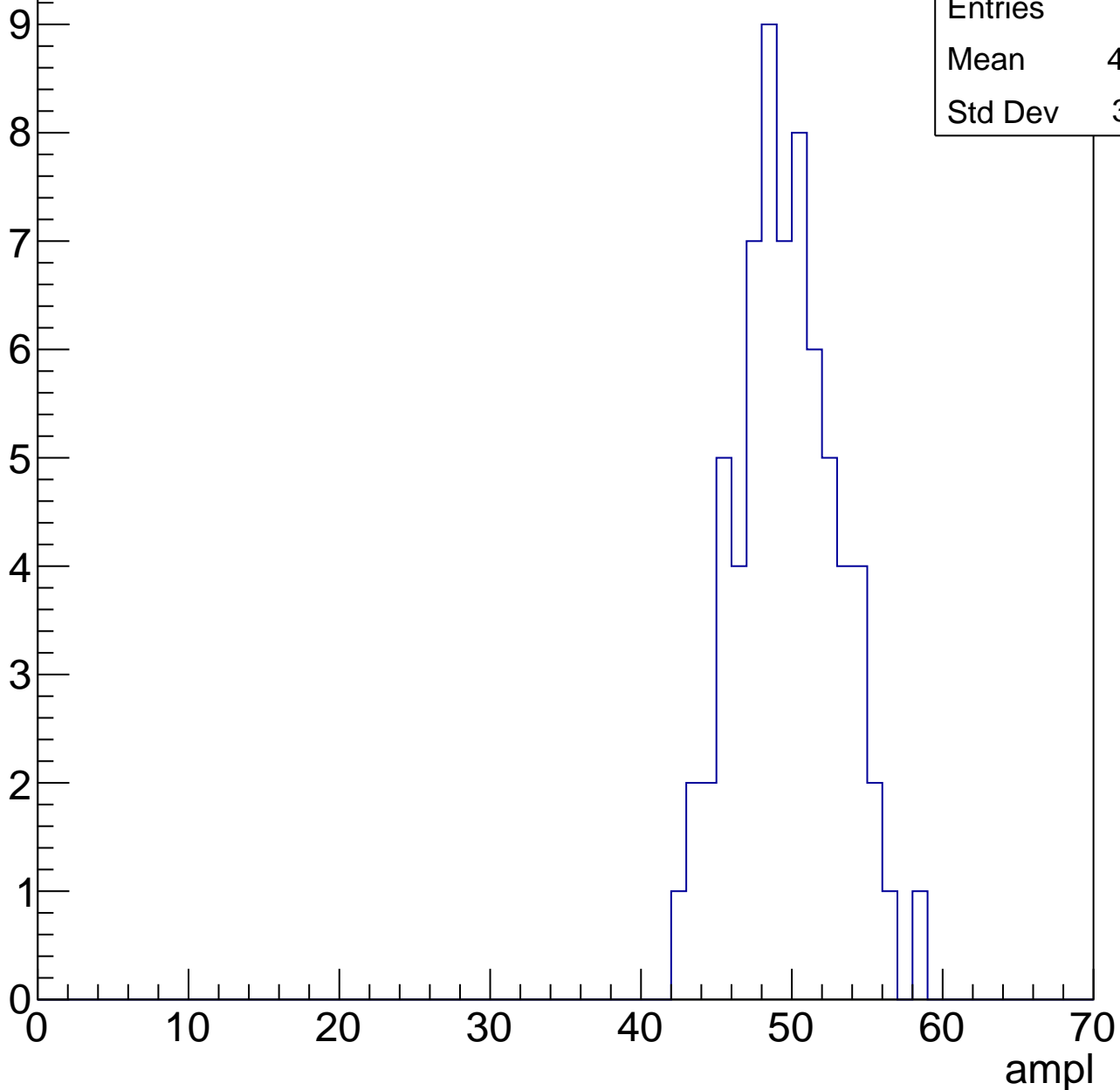


B1L103S, U23-ch93, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	49.22
Std Dev	3.351

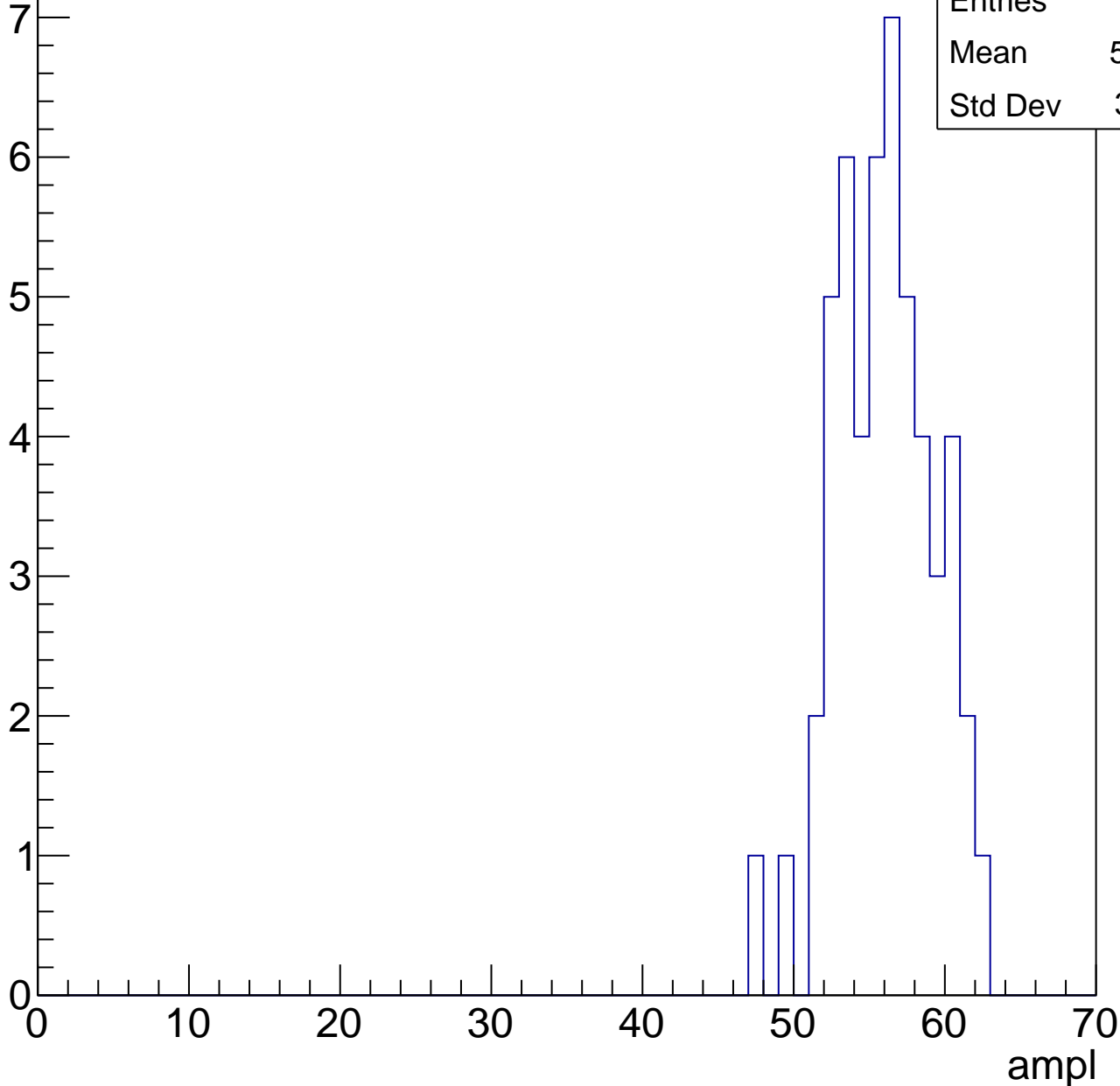


B1L103S, U23-ch93, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

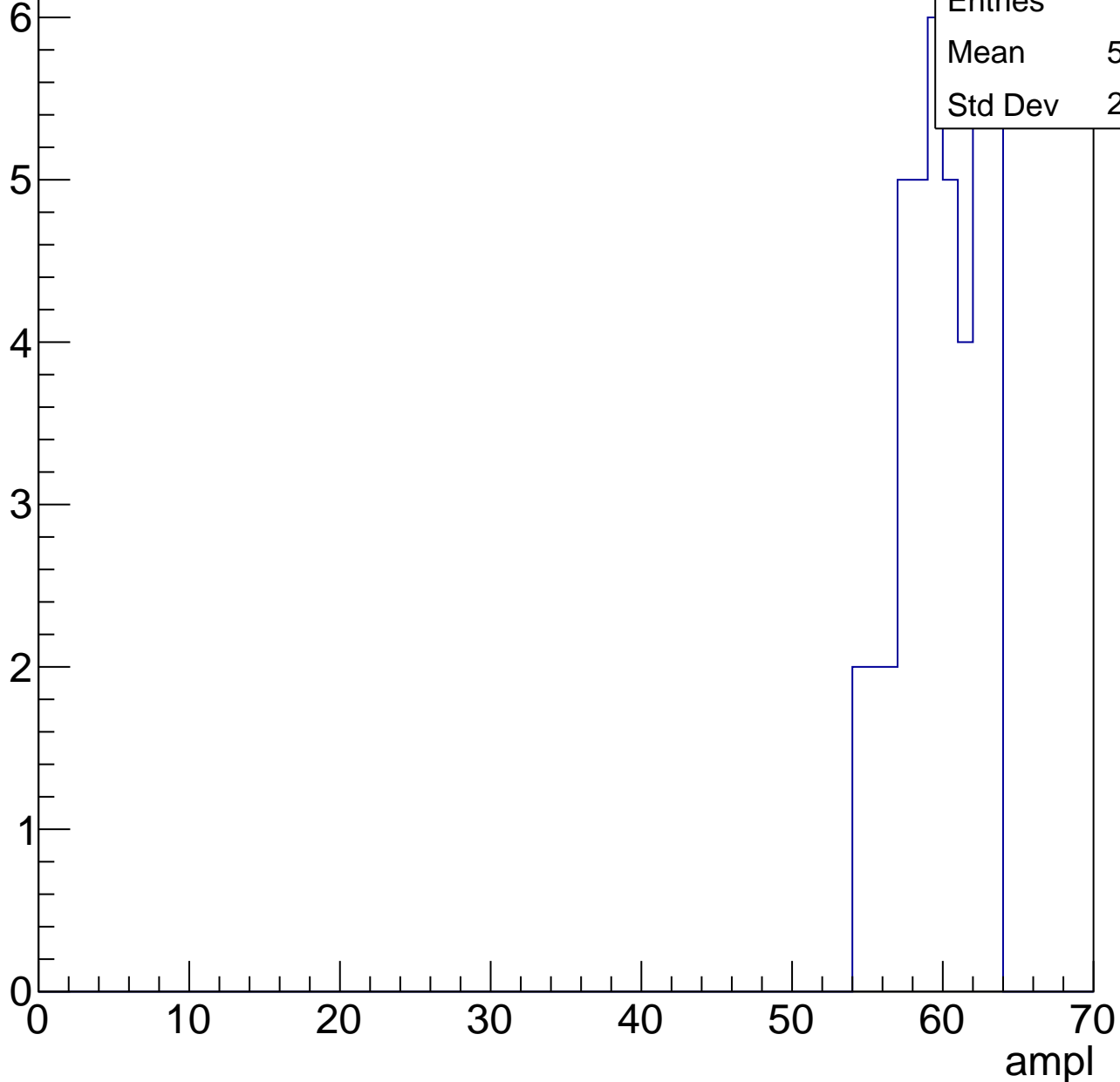
Entries	51
Mean	55.53
Std Dev	3.201



B1L103S, U23-ch93, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

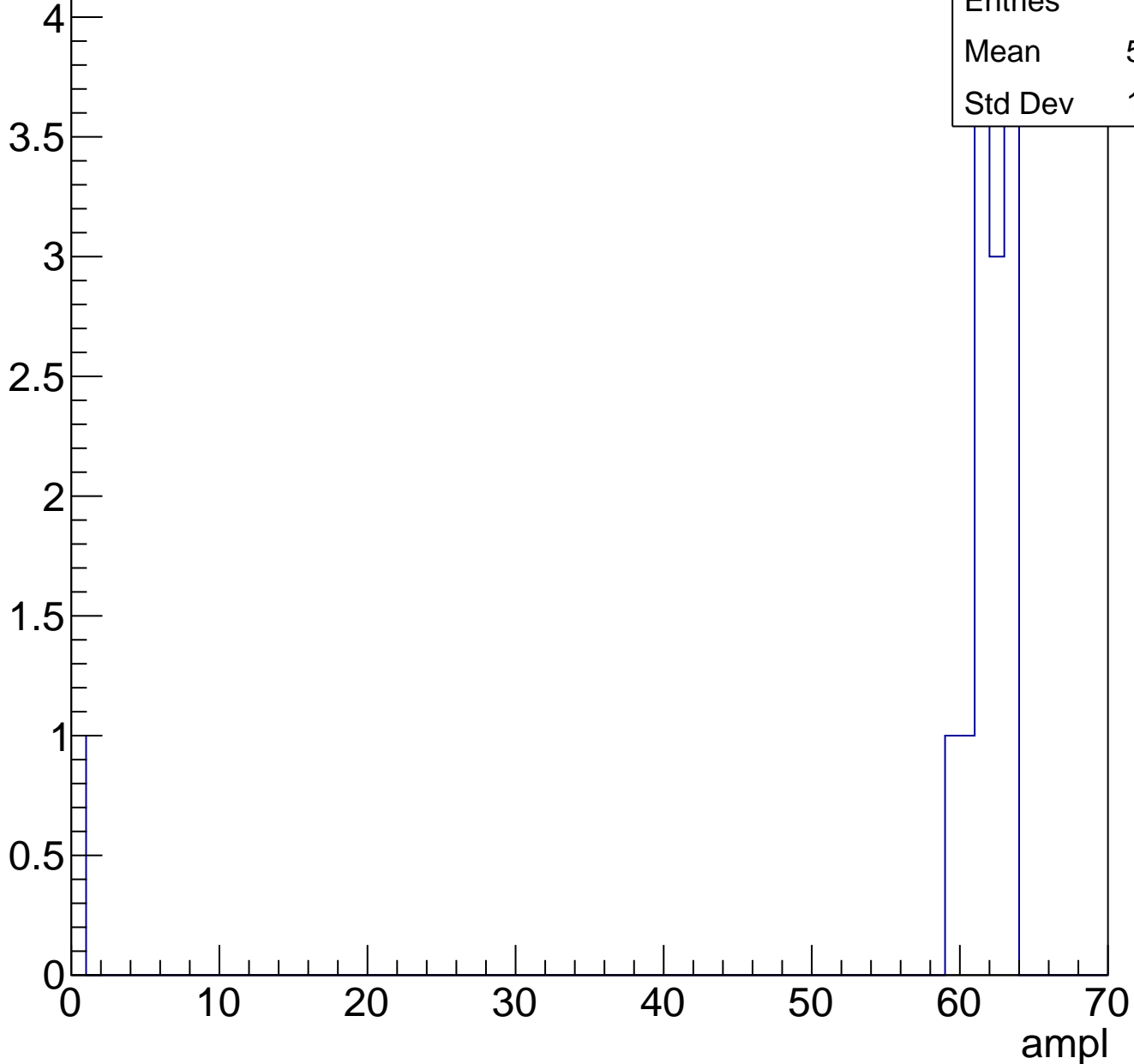


Entries	43
Mean	59.37
Std Dev	2.597

B1L103S, U23-ch93, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch93, adc7

calib_packv5_041523_1651.root, FC#0, port C2

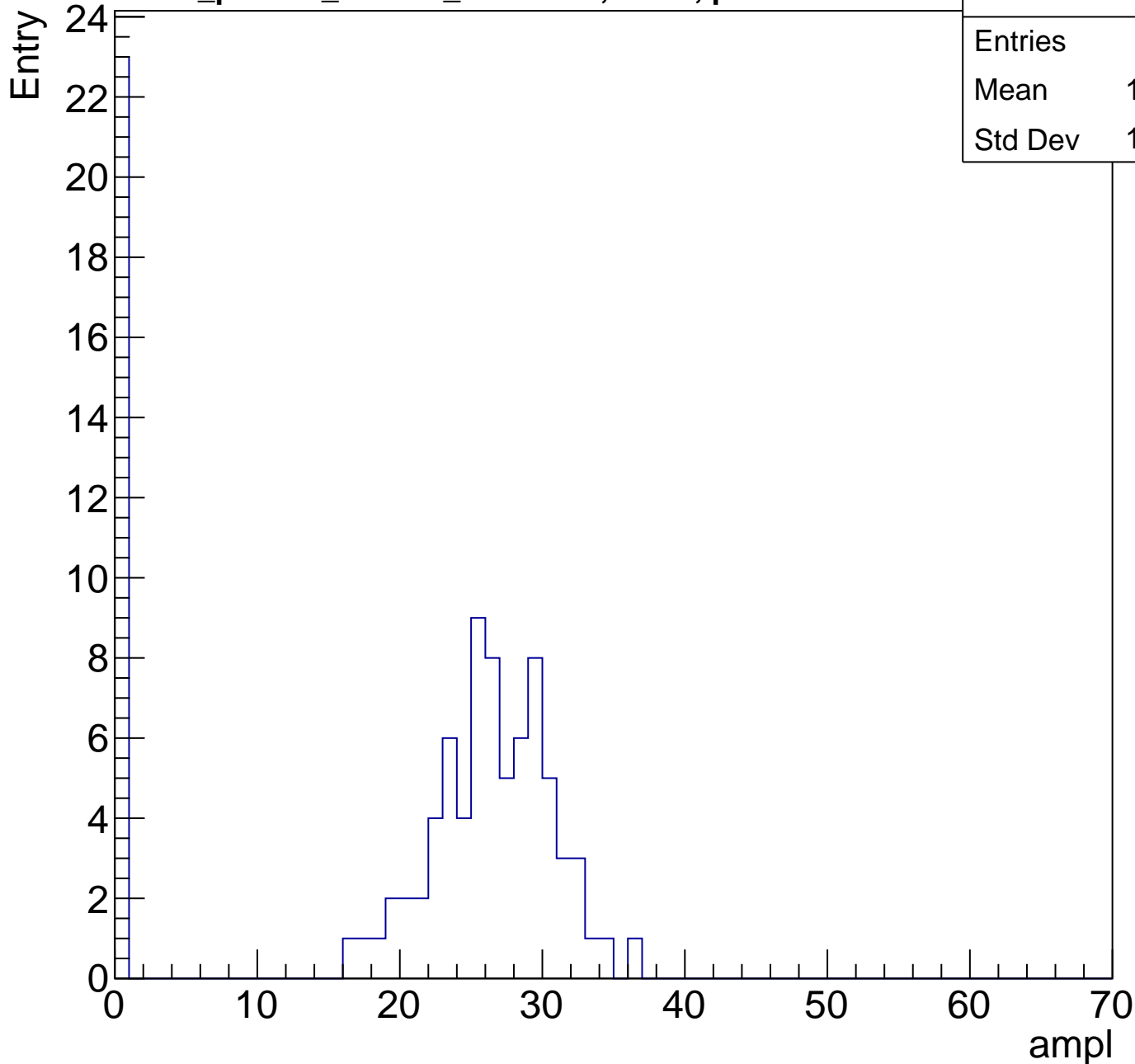
Entry



B1L103S, U23-ch94, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	96
Mean	19.82
Std Dev	11.67

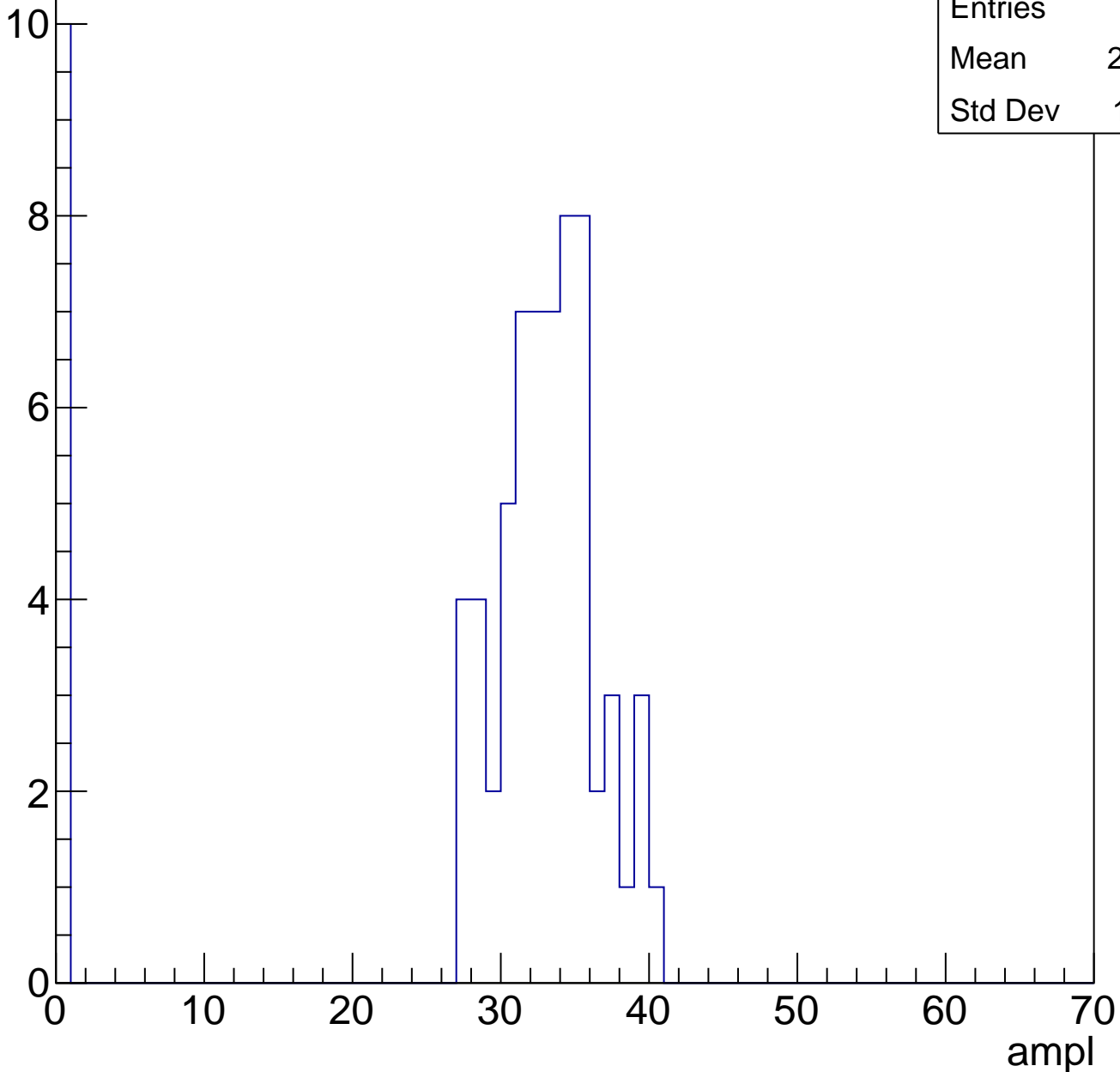


B1L103S, U23-ch94, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	72
Mean	28.19
Std Dev	11.71

Entry

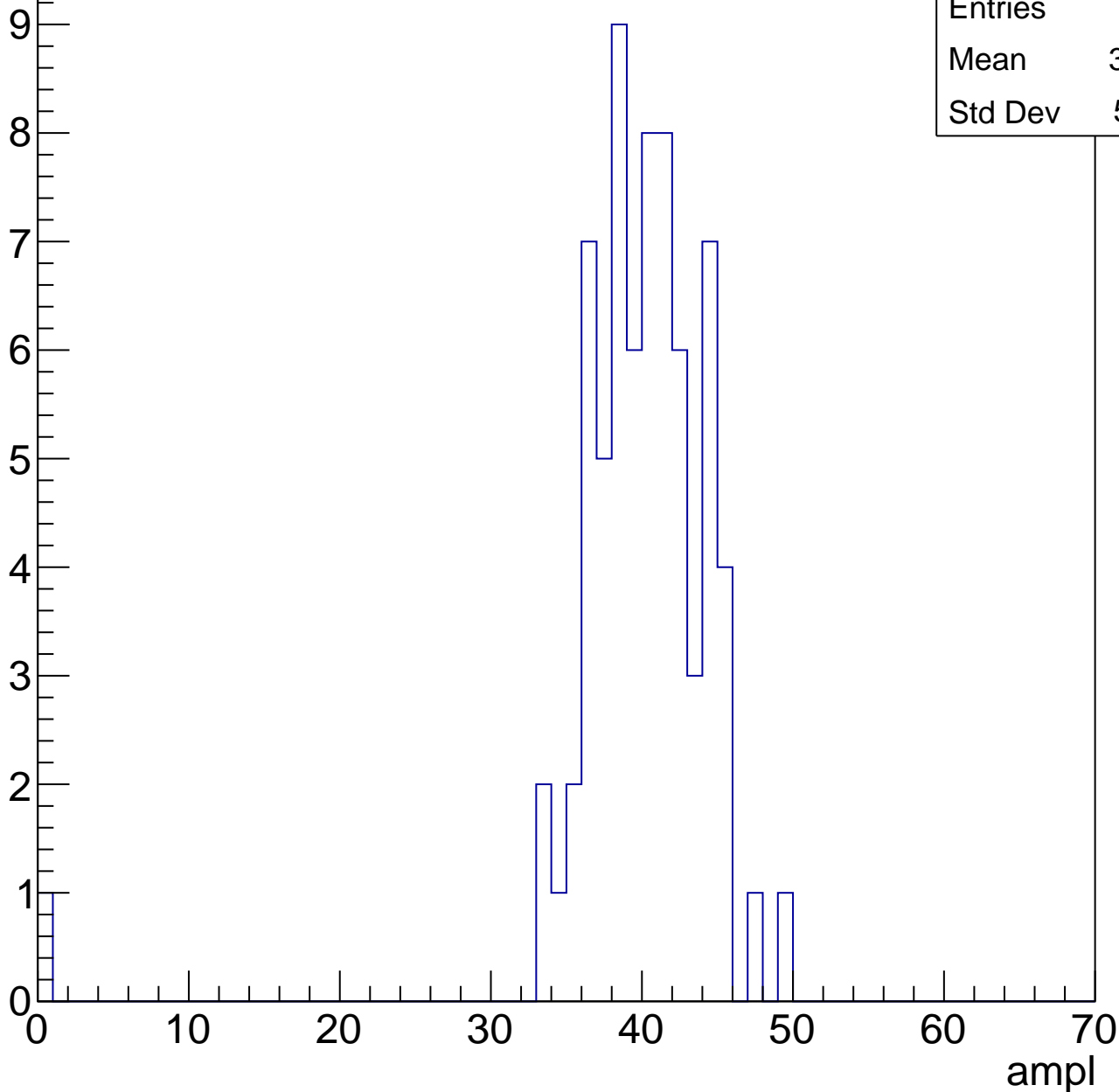


B1L103S, U23-ch94, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	39.38
Std Dev	5.761

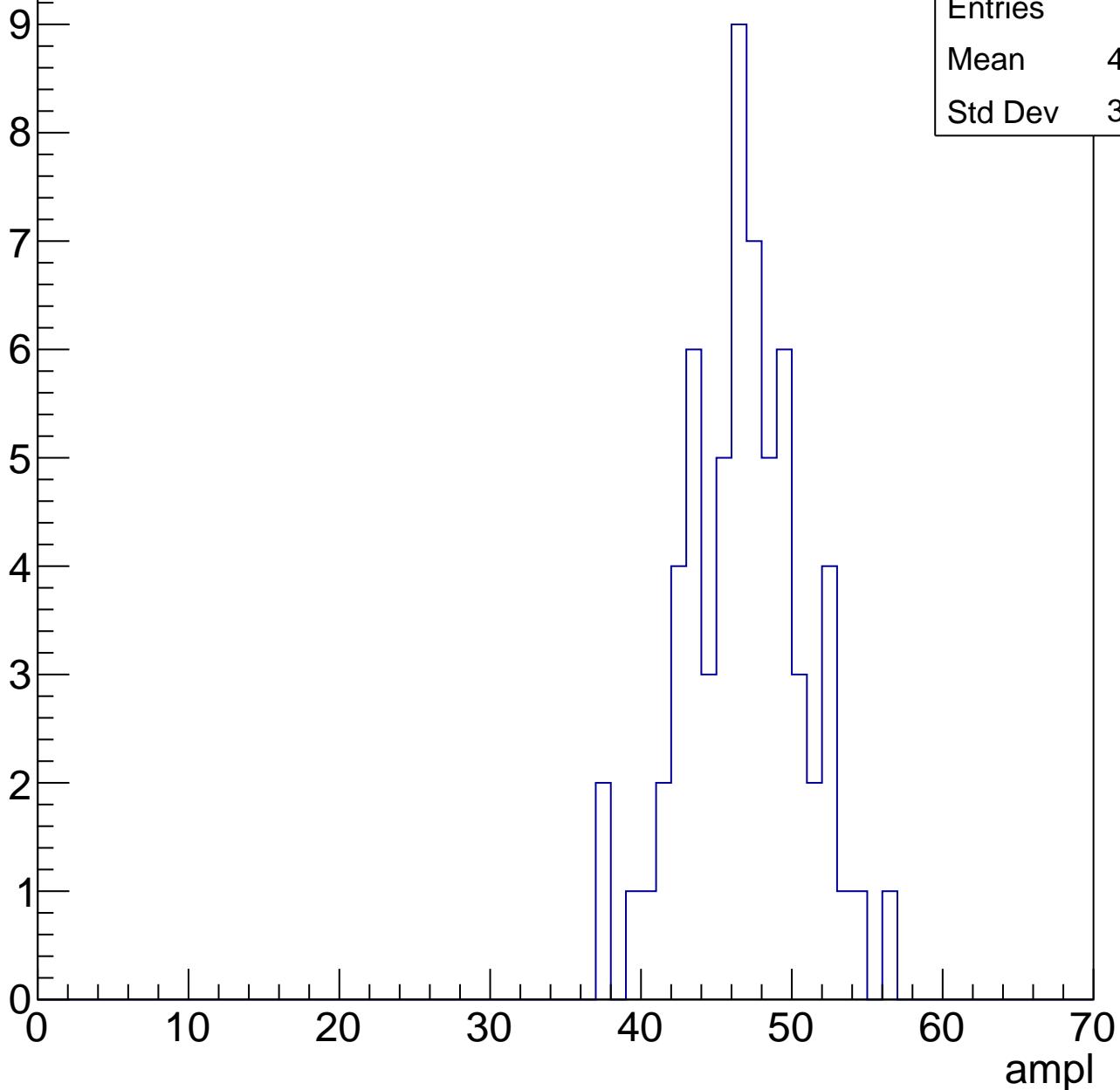


B1L103S, U23-ch94, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	63
Mean	46.32
Std Dev	3.907

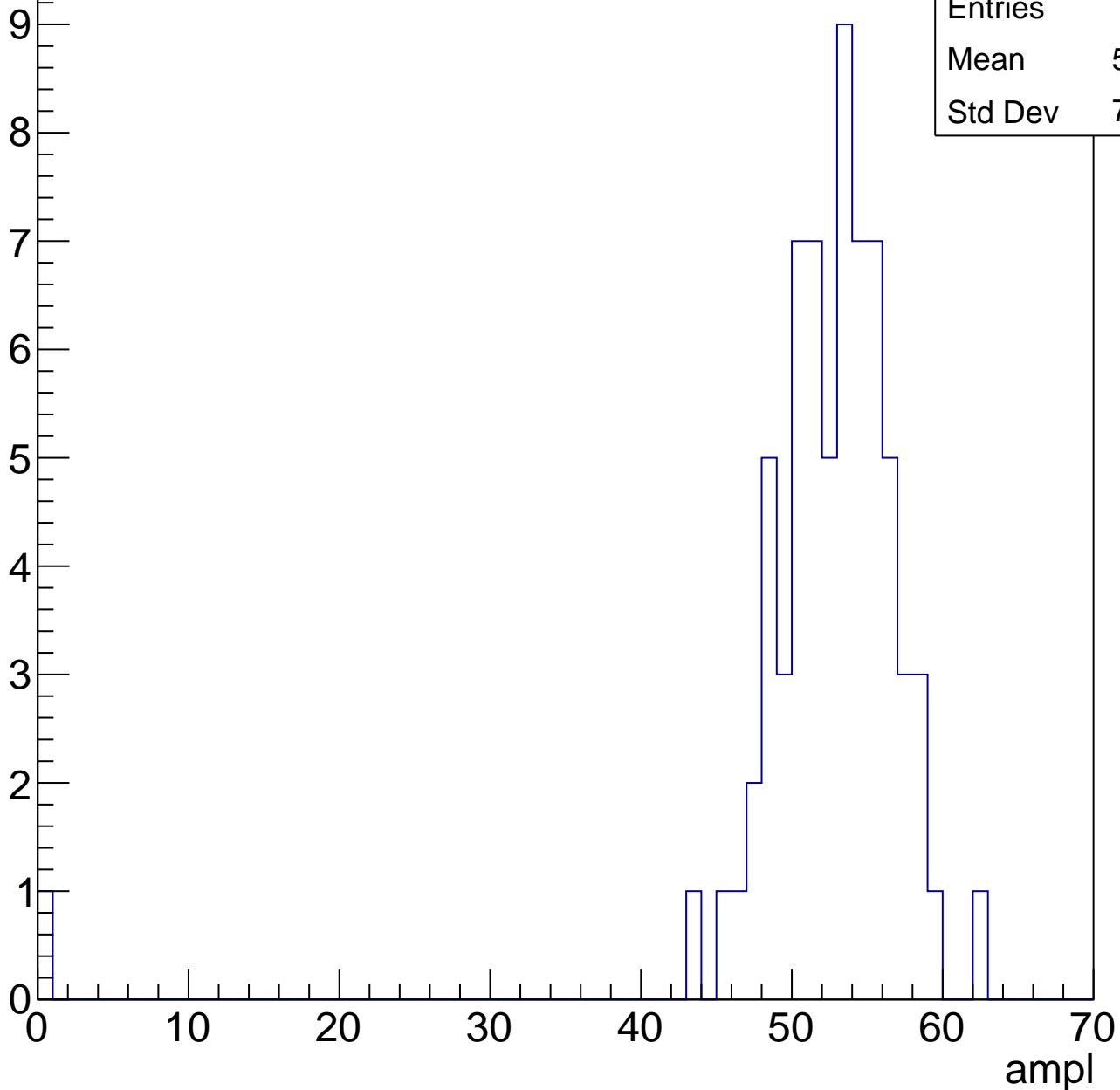


B1L103S, U23-ch94, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	51.71
Std Dev	7.191

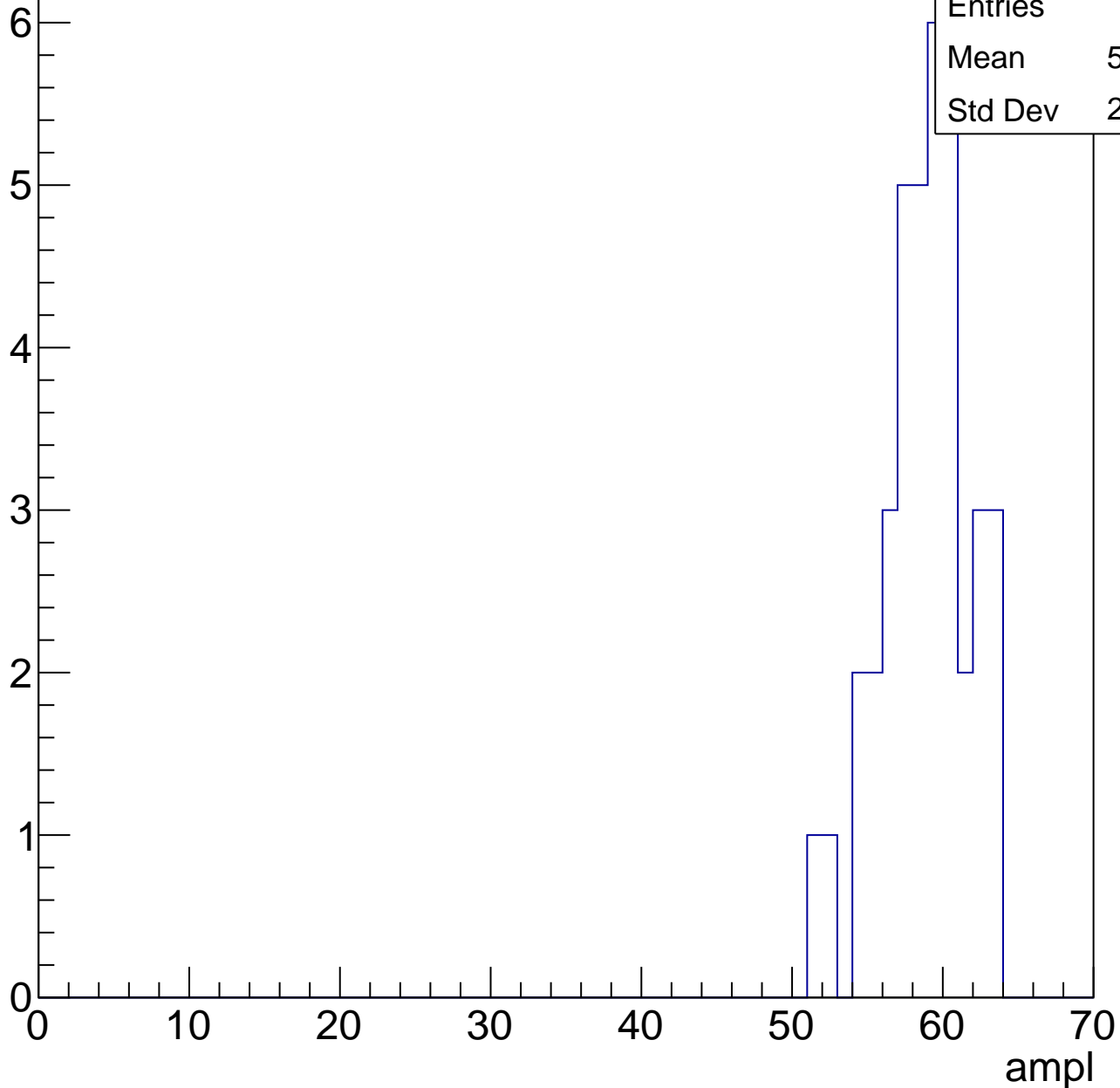


B1L103S, U23-ch94, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	39
Mean	58.33
Std Dev	2.858

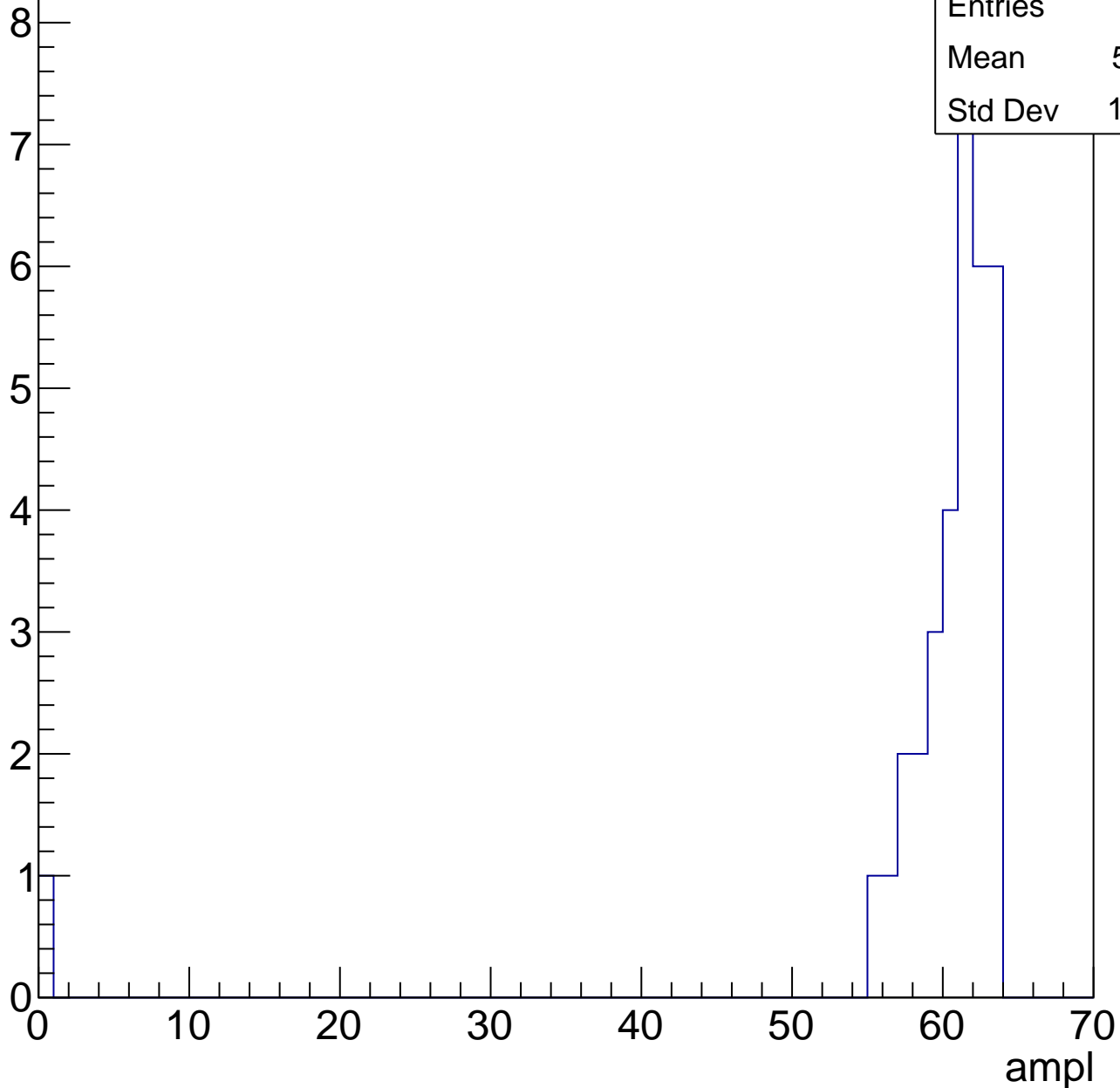


B1L103S, U23-ch94, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	34
Mean	58.71
Std Dev	10.43



B1L103S, U23-ch94, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.15
Std Dev	13.73

Entry



B1L103S, U23-ch95, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	75
Mean	22.61
Std Dev	10.88

Entry

12

10

8

6

4

2

0

0

10

20

30

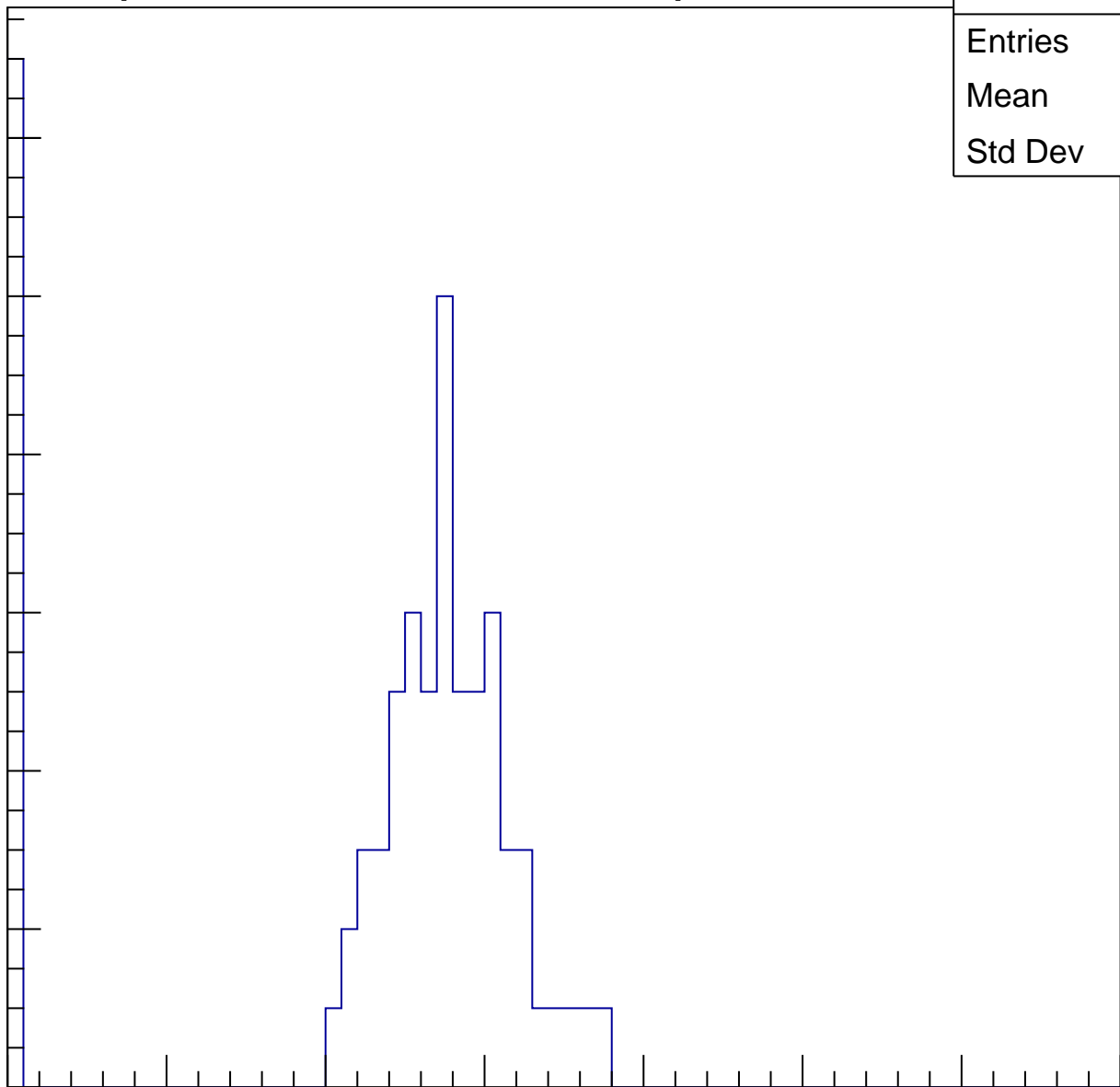
40

50

60

70

ampl

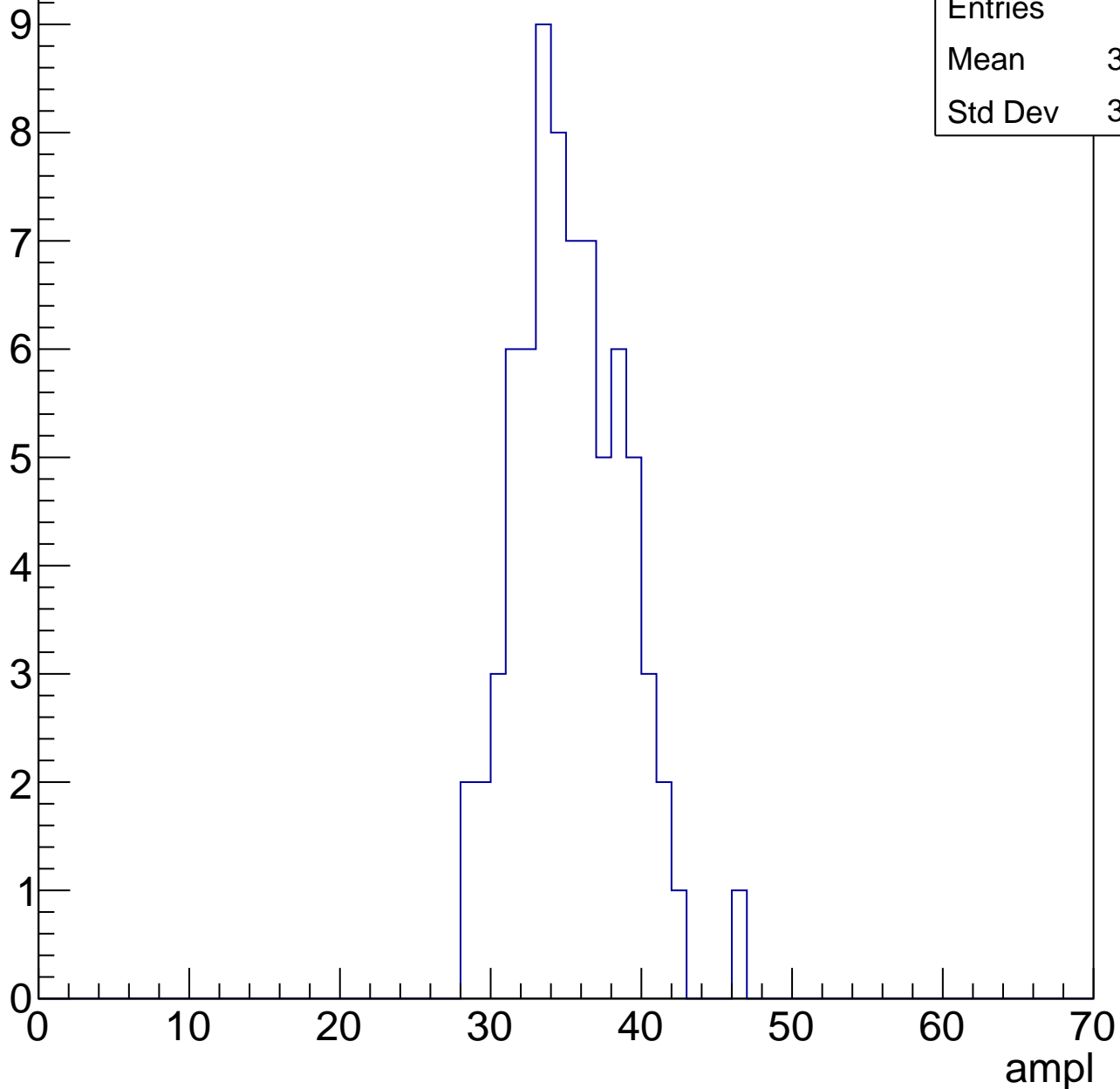


B1L103S, U23-ch95, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	73
Mean	34.88
Std Dev	3.542

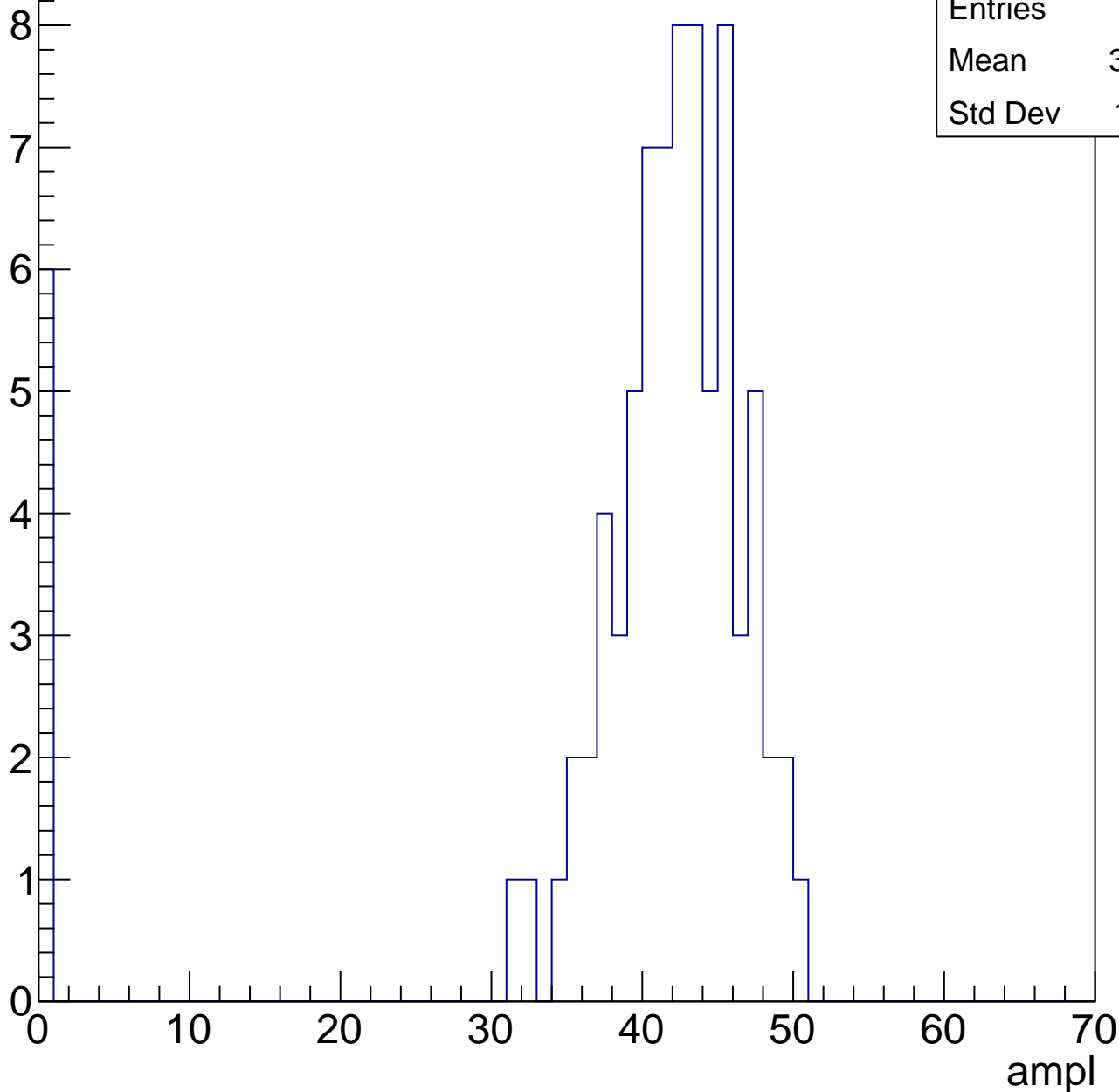


B1L103S, U23-ch95, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	81
Mean	38.77
Std Dev	11.61

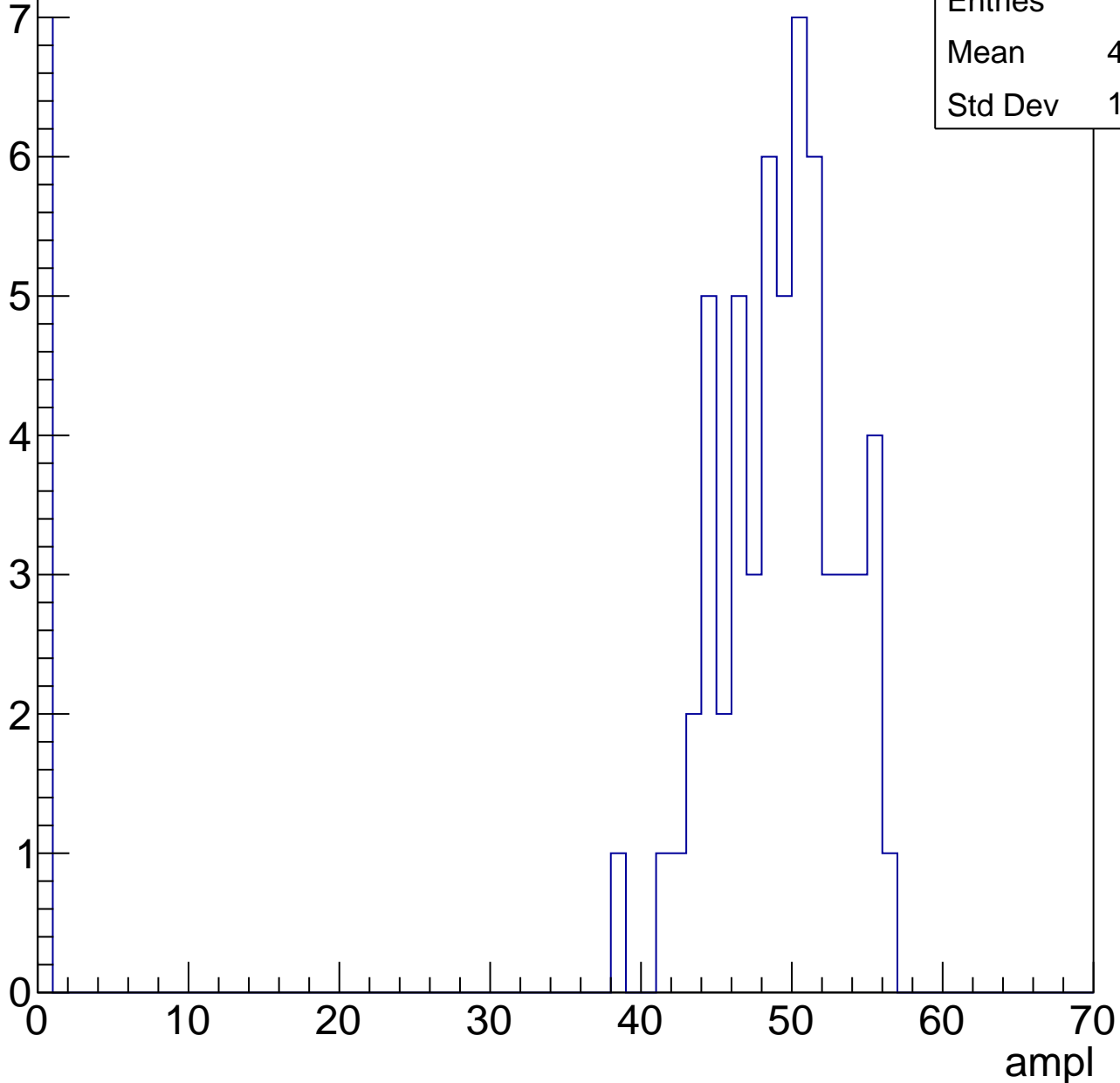


B1L103S, U23-ch95, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	43.54
Std Dev	15.58

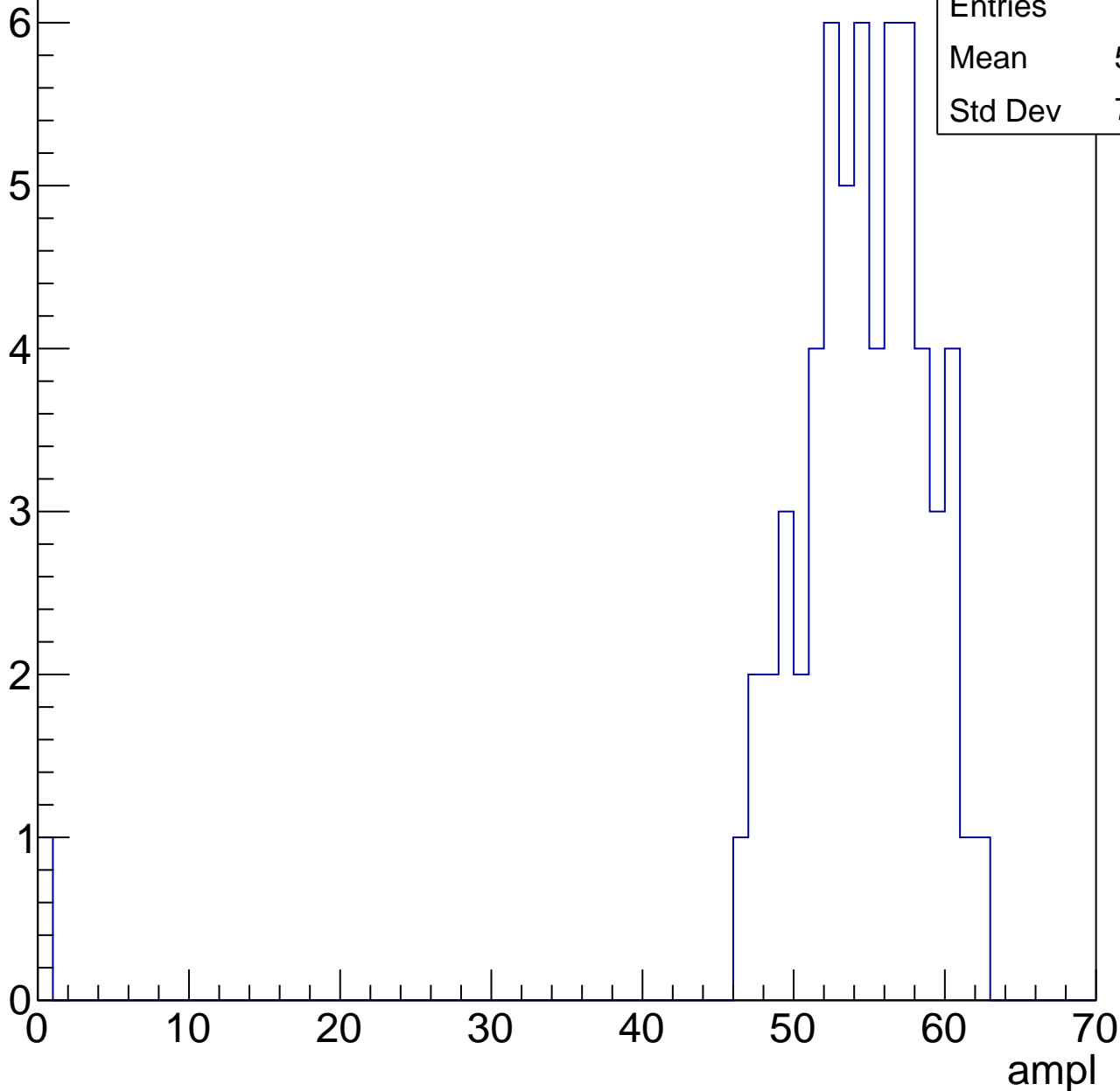


B1L103S, U23-ch95, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

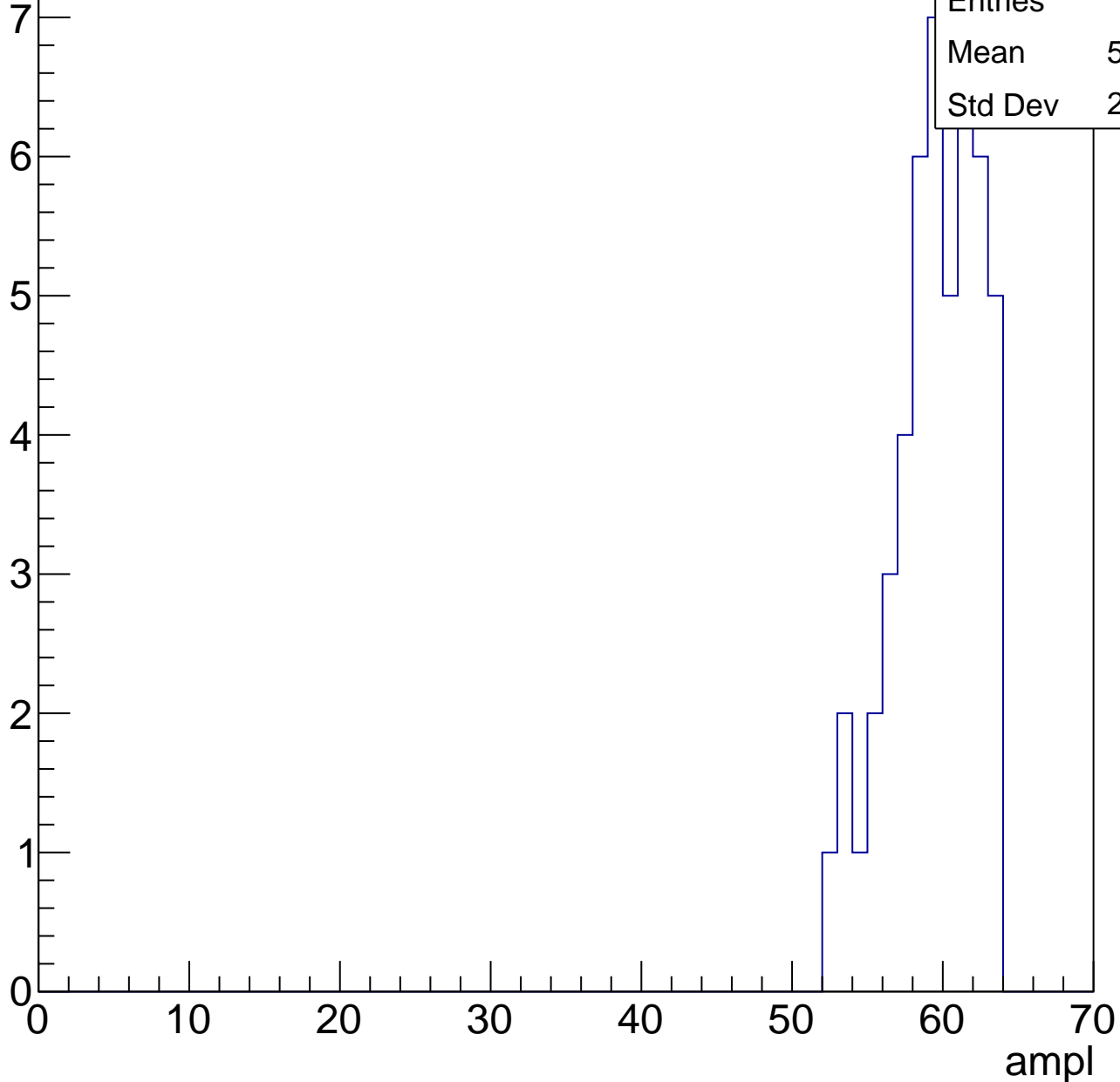
Entries	61
Mean	53.41
Std Dev	7.871



B1L103S, U23-ch95, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

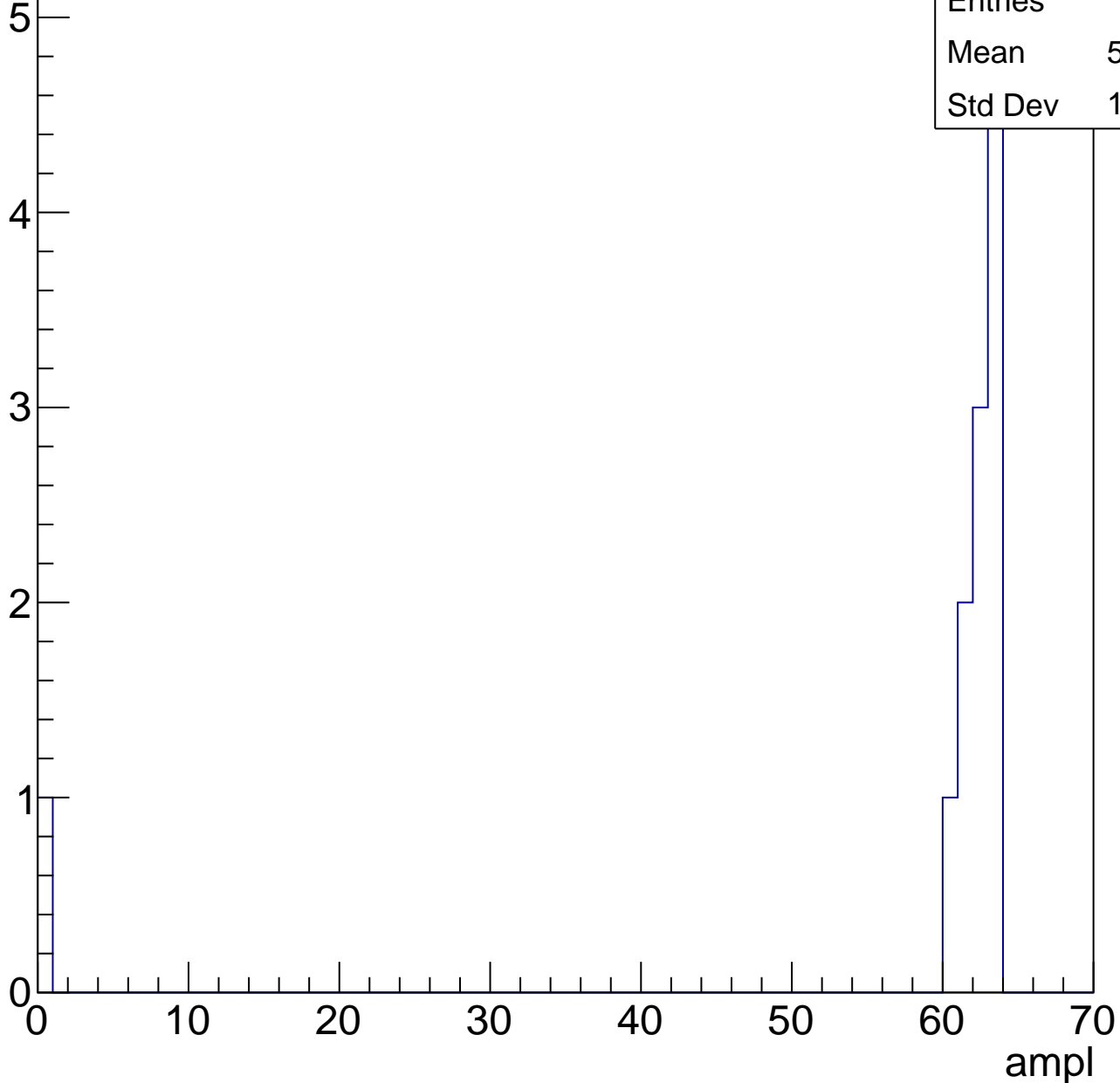


B1L103S, U23-ch95, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	12
Mean	56.92
Std Dev	17.19



B1L103S, U23-ch95, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch96, adc0

calib_packv5_041523_1651.root, FC#0, port C2

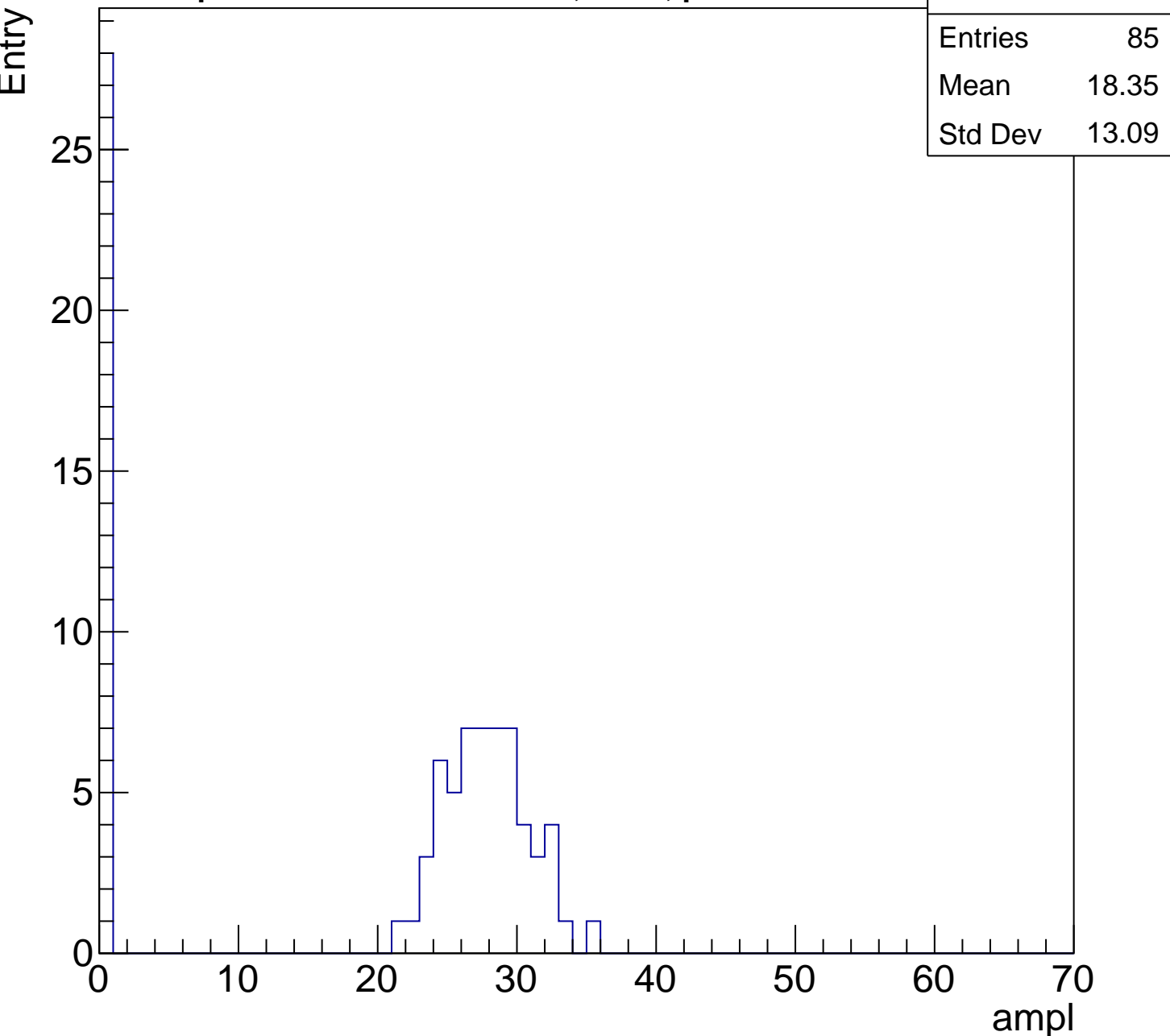
Entries	85
Mean	18.35
Std Dev	13.09

Entry

25
20
15
10
5
0

0 10 20 30 40 50 60 70

ampl



B1L103S, U23-ch96, adc1

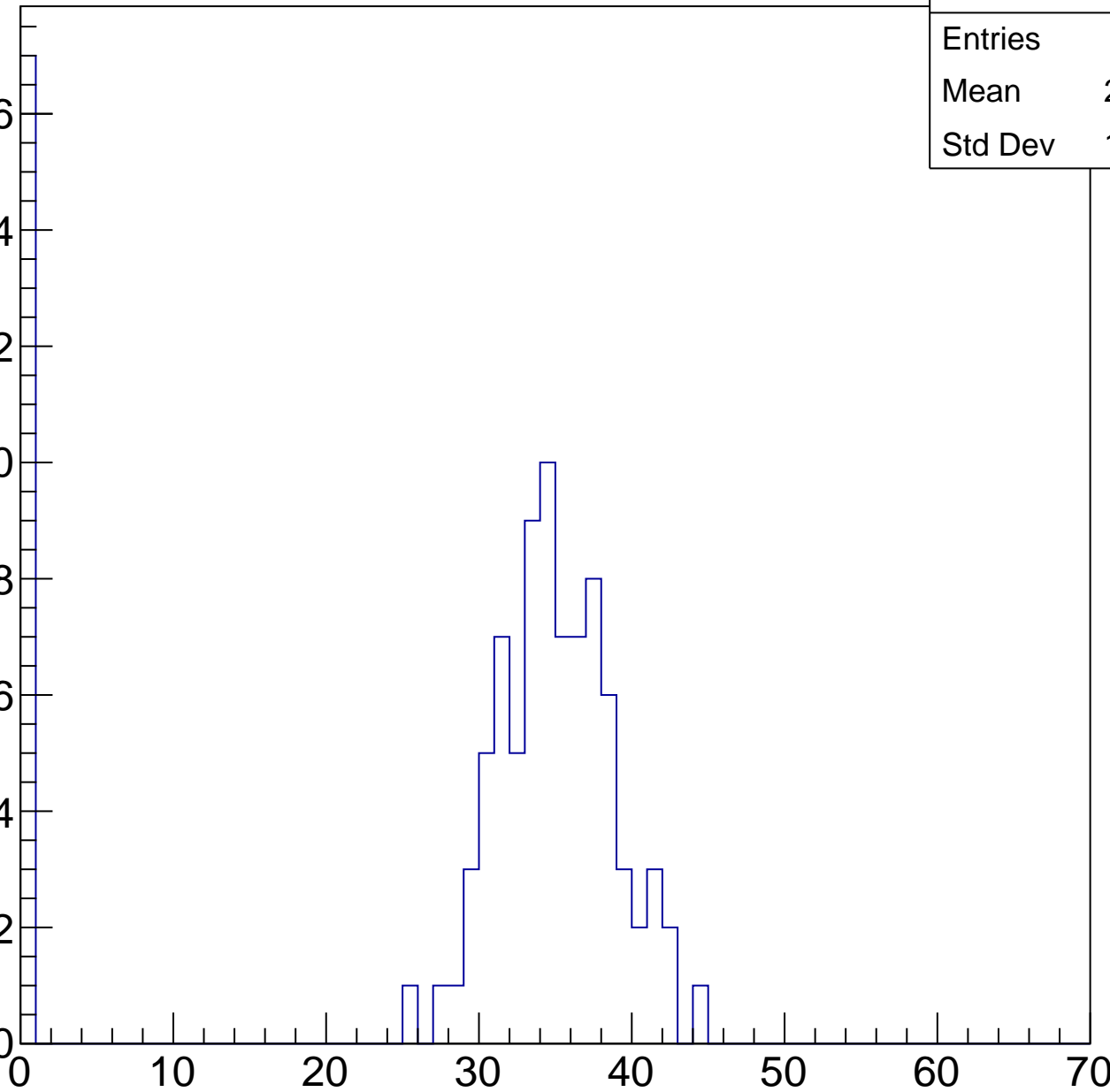
calib_packv5_041523_1651.root, FC#0, port C2

Entries	98
Mean	28.57
Std Dev	13.52

Entry

16
14
12
10
8
6
4
2
0

ampl

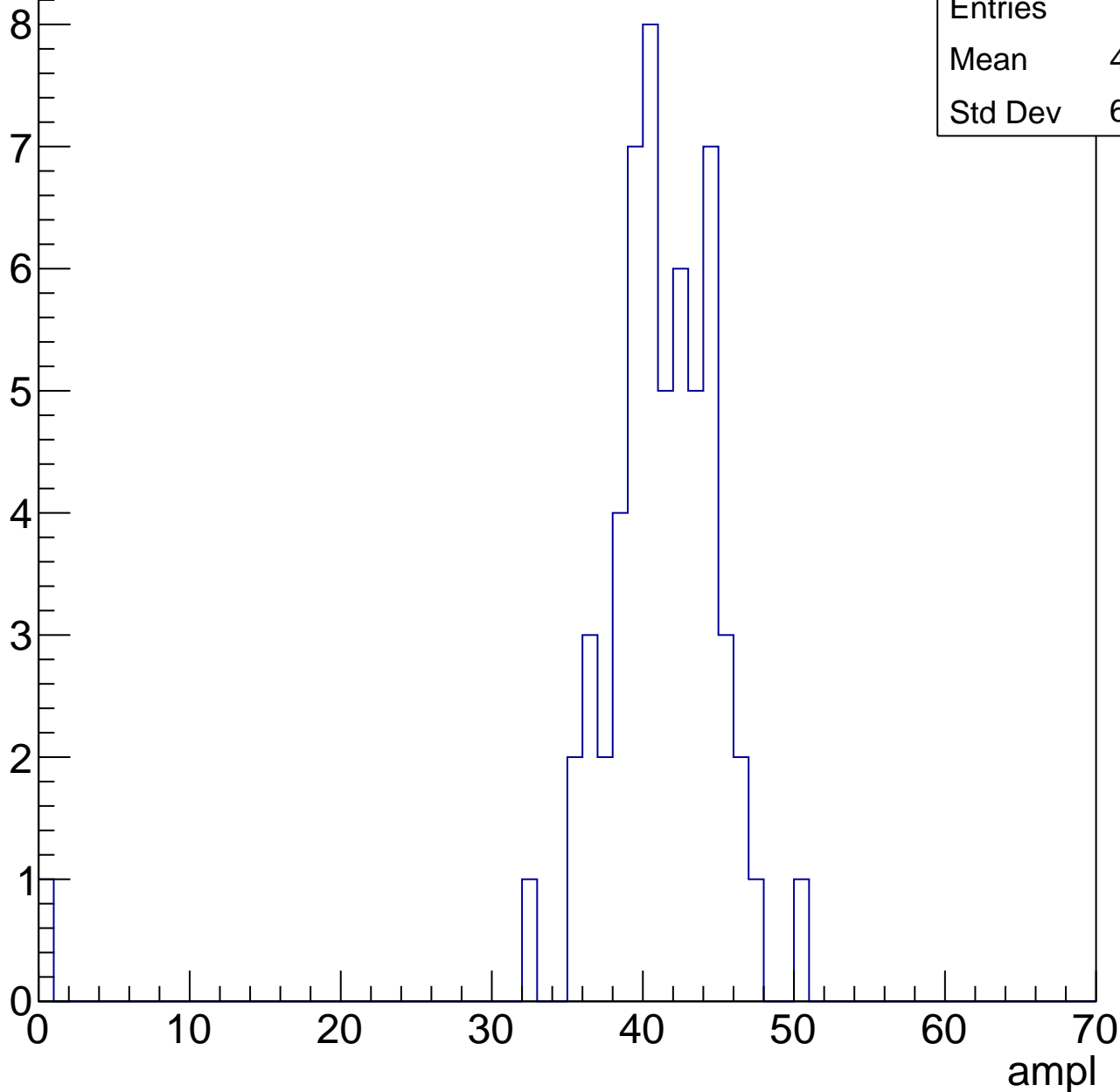


B1L103S, U23-ch96, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	40.22
Std Dev	6.273

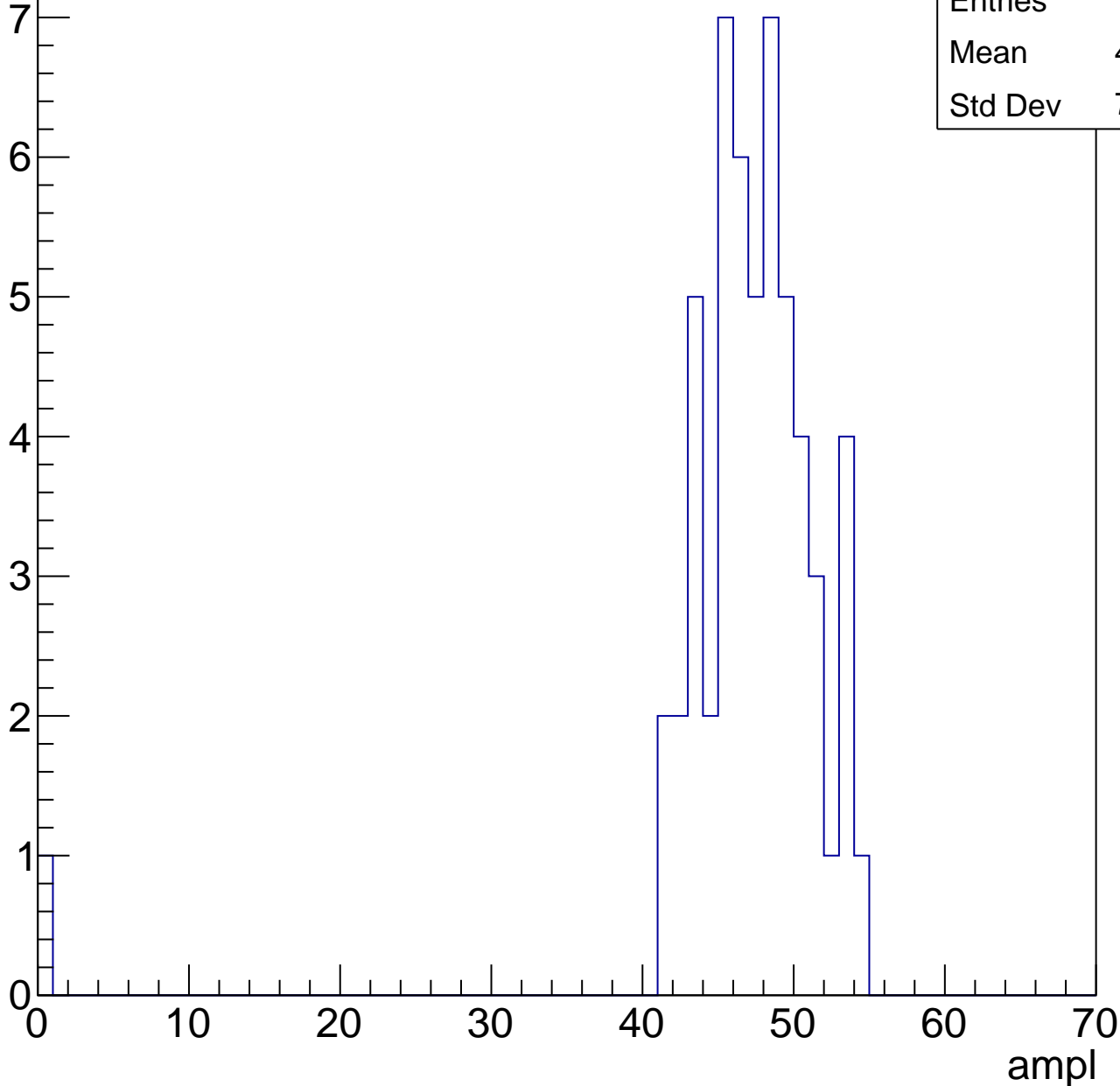


B1L103S, U23-ch96, adc3

calib_packv5_041523_1651.root, FC#0, port C2

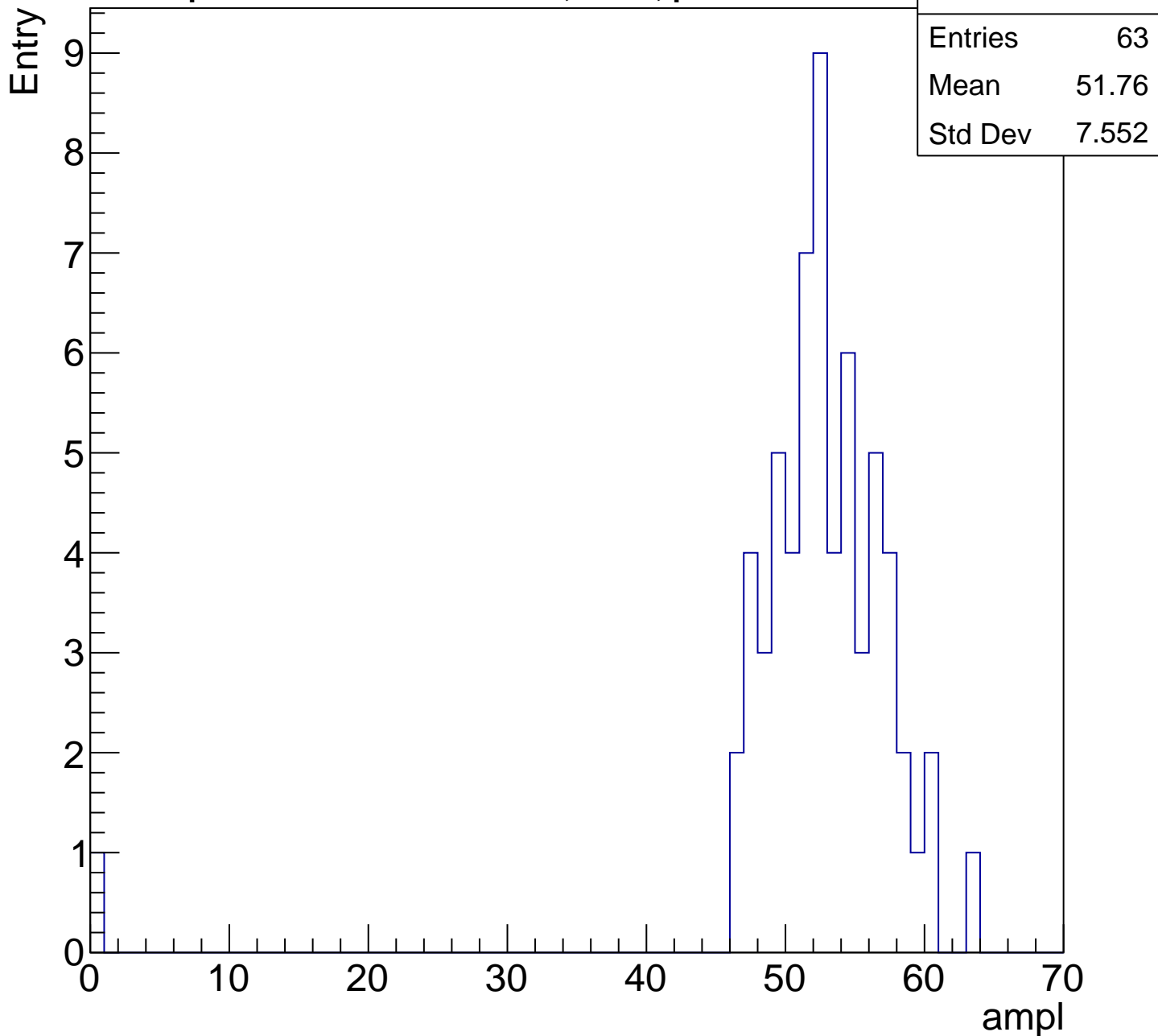
Entry

Entries	55
Mean	46.31
Std Dev	7.091



B1L103S, U23-ch96, adc4

calib_packv5_041523_1651.root, FC#0, port C2

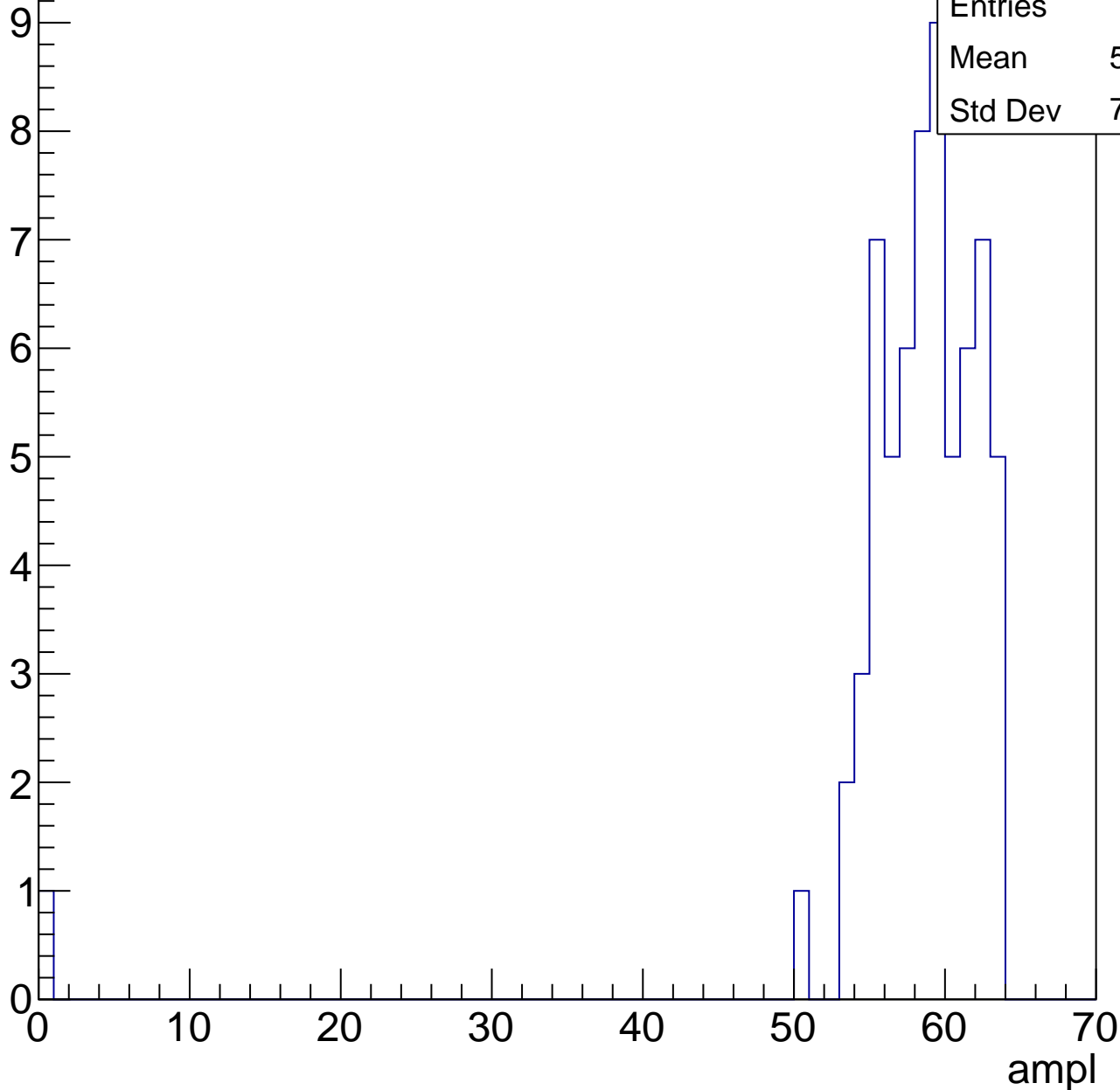


B1L103S, U23-ch96, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

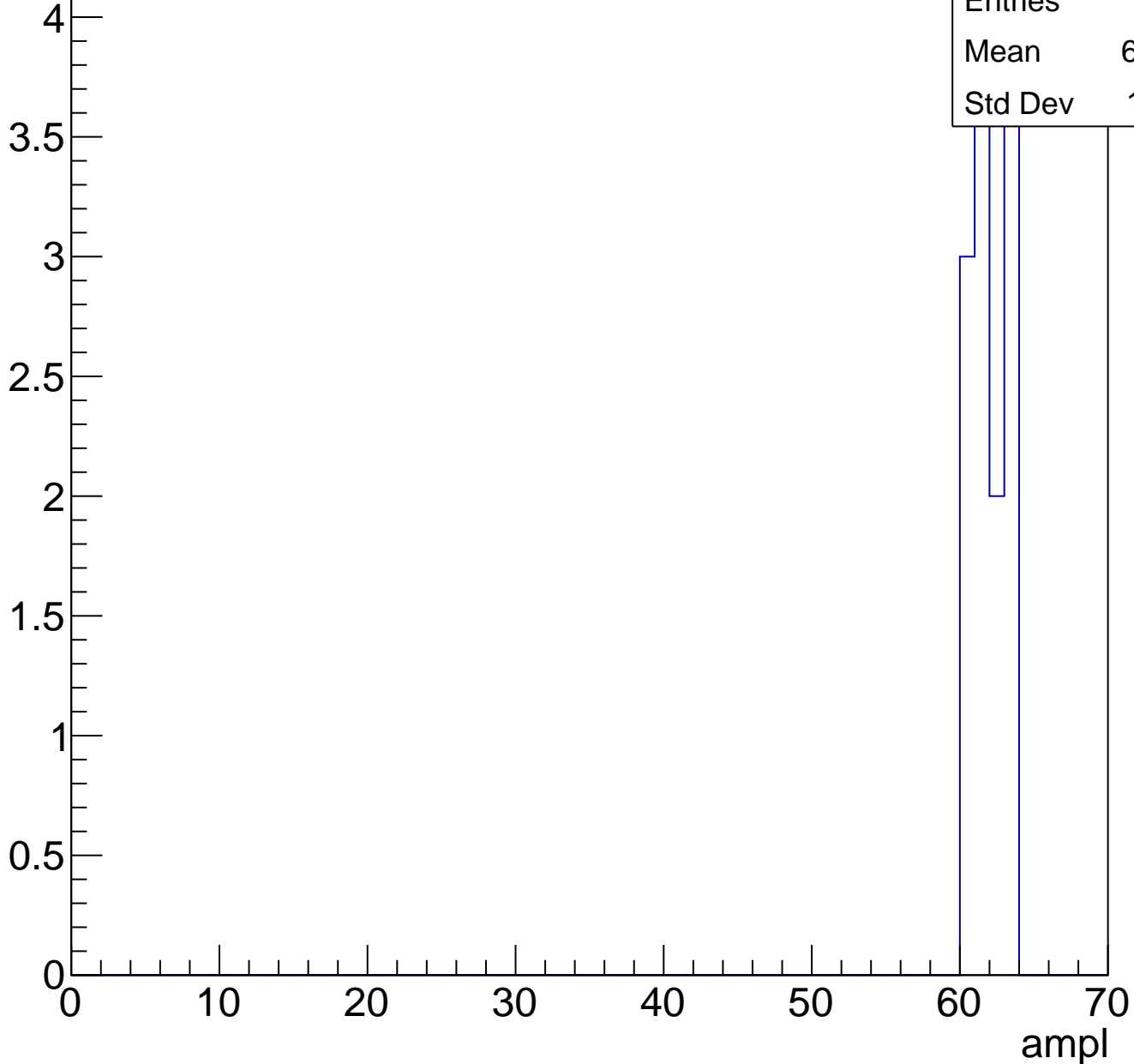
Entries	65
Mean	57.46
Std Dev	7.762



B1L103S, U23-ch96, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch96, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.1
Std Dev	13.51

Entry



B1L103S, U23-ch97, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	89
Mean	22.83
Std Dev	11.26

Entry

16
14
12
10
8
6
4
2
0

0

10

20

30

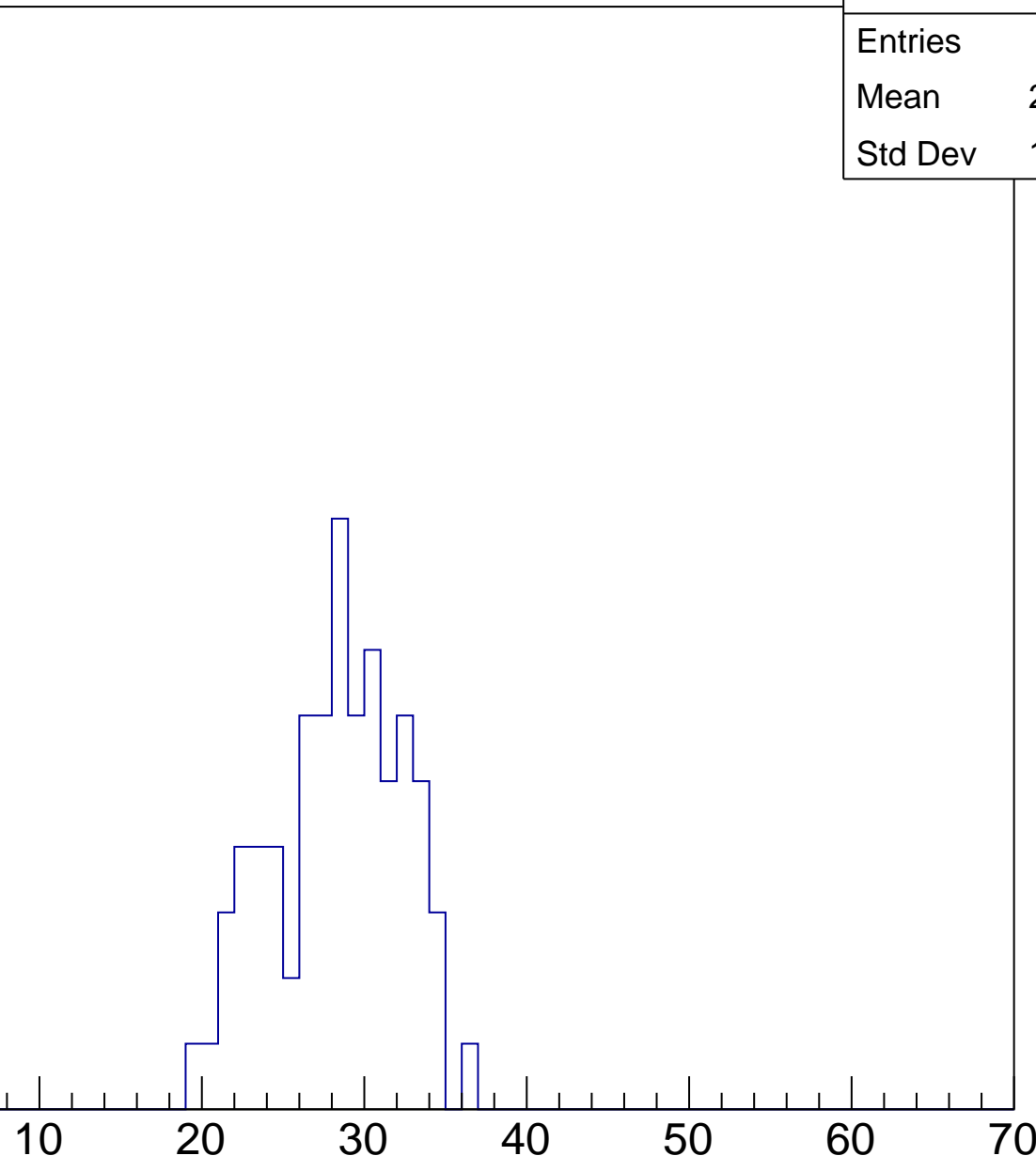
40

50

60

70

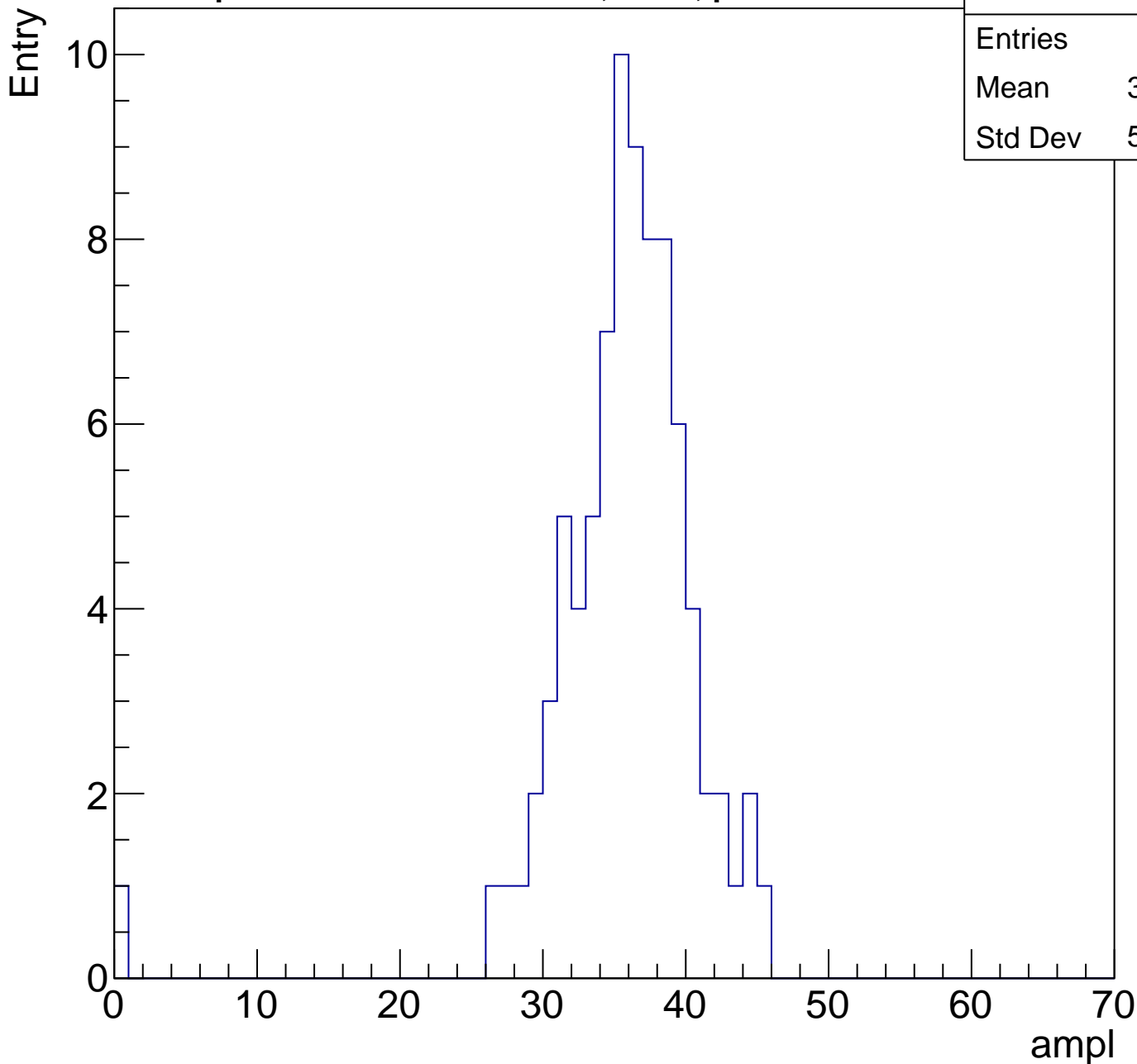
ampl



B1L103S, U23-ch97, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	83
Mean	35.24
Std Dev	5.498



B1L103S, U23-ch97, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	60
Mean	33.13
Std Dev	17.63

Entry

12

10

8

6

4

2

0

0

10

20

30

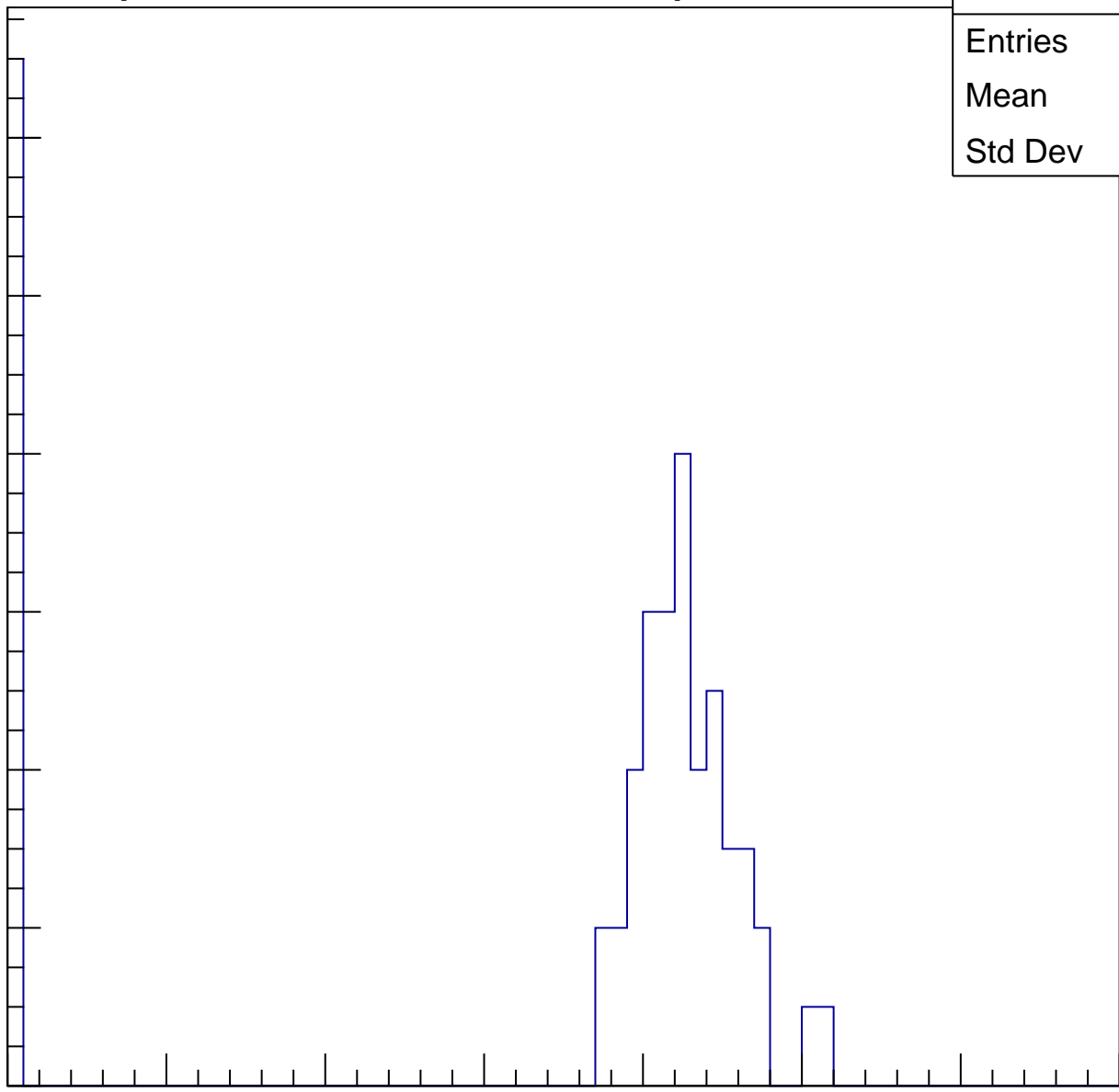
40

50

60

70

ampl



B1L103S, U23-ch97, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	74
Mean	47.7
Std Dev	6.563

Entry

10

8

6

4

2

0

0

10

20

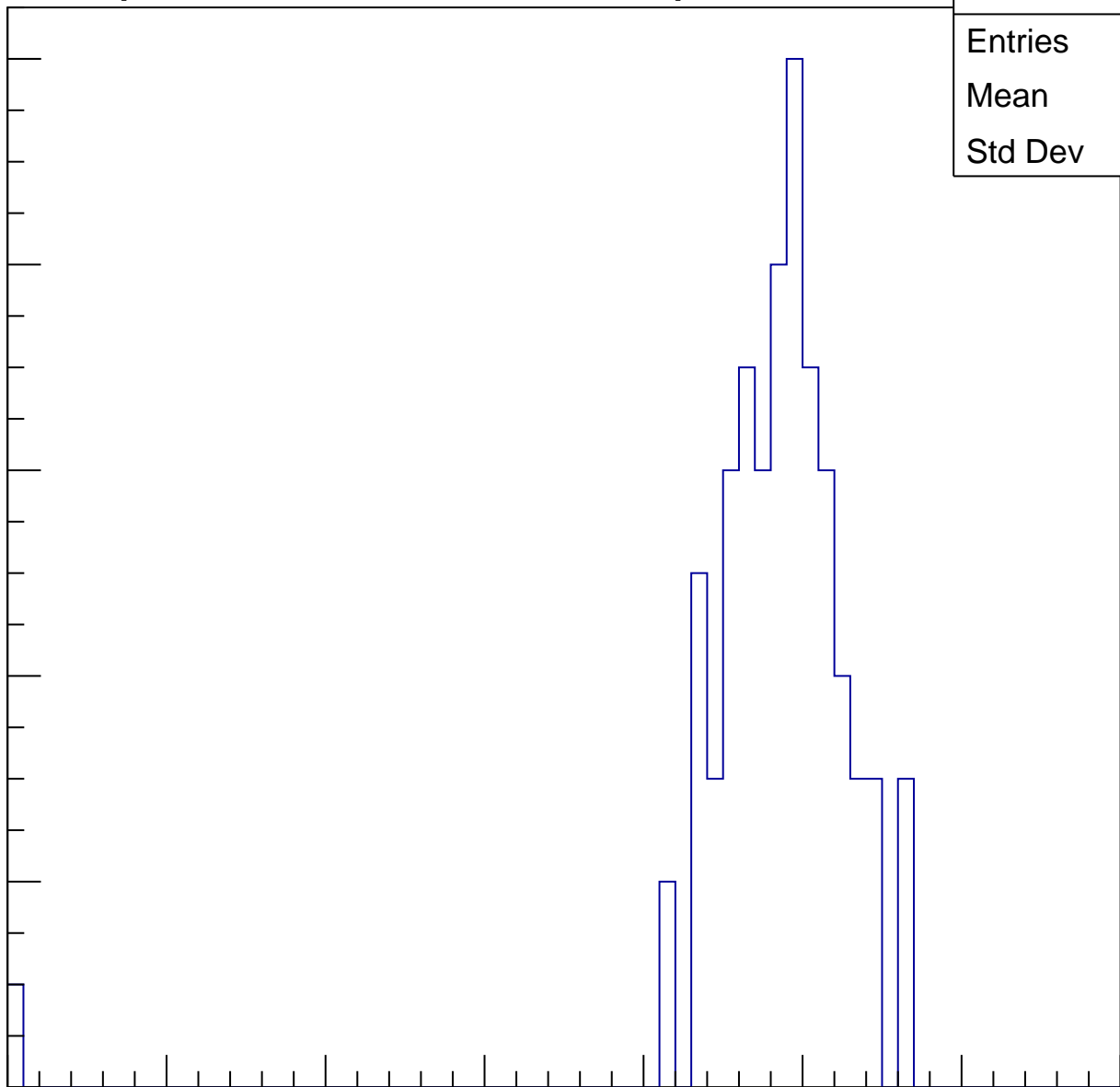
30

40

50

60

ampl

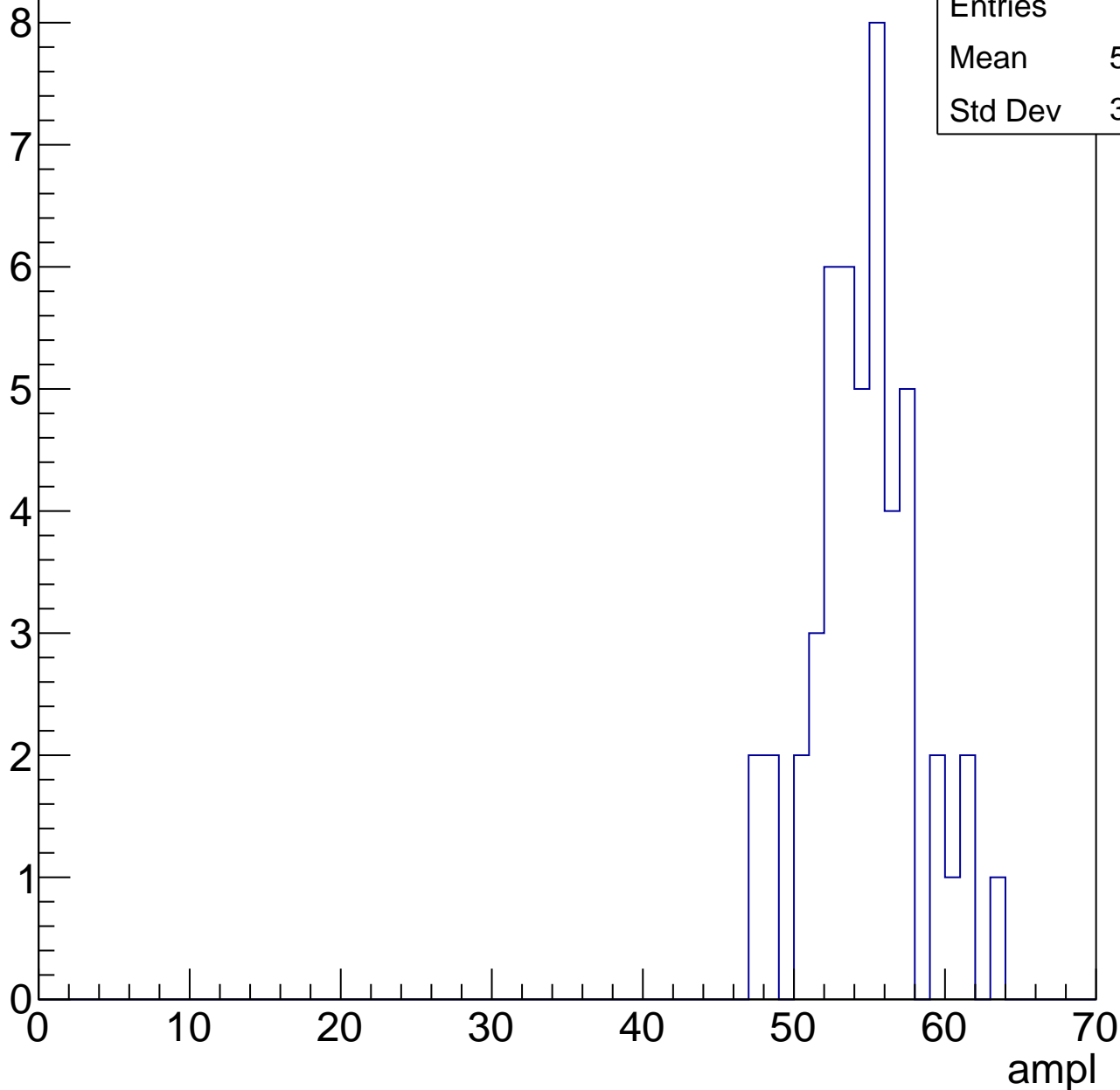


B1L103S, U23-ch97, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	49
Mean	54.18
Std Dev	3.474

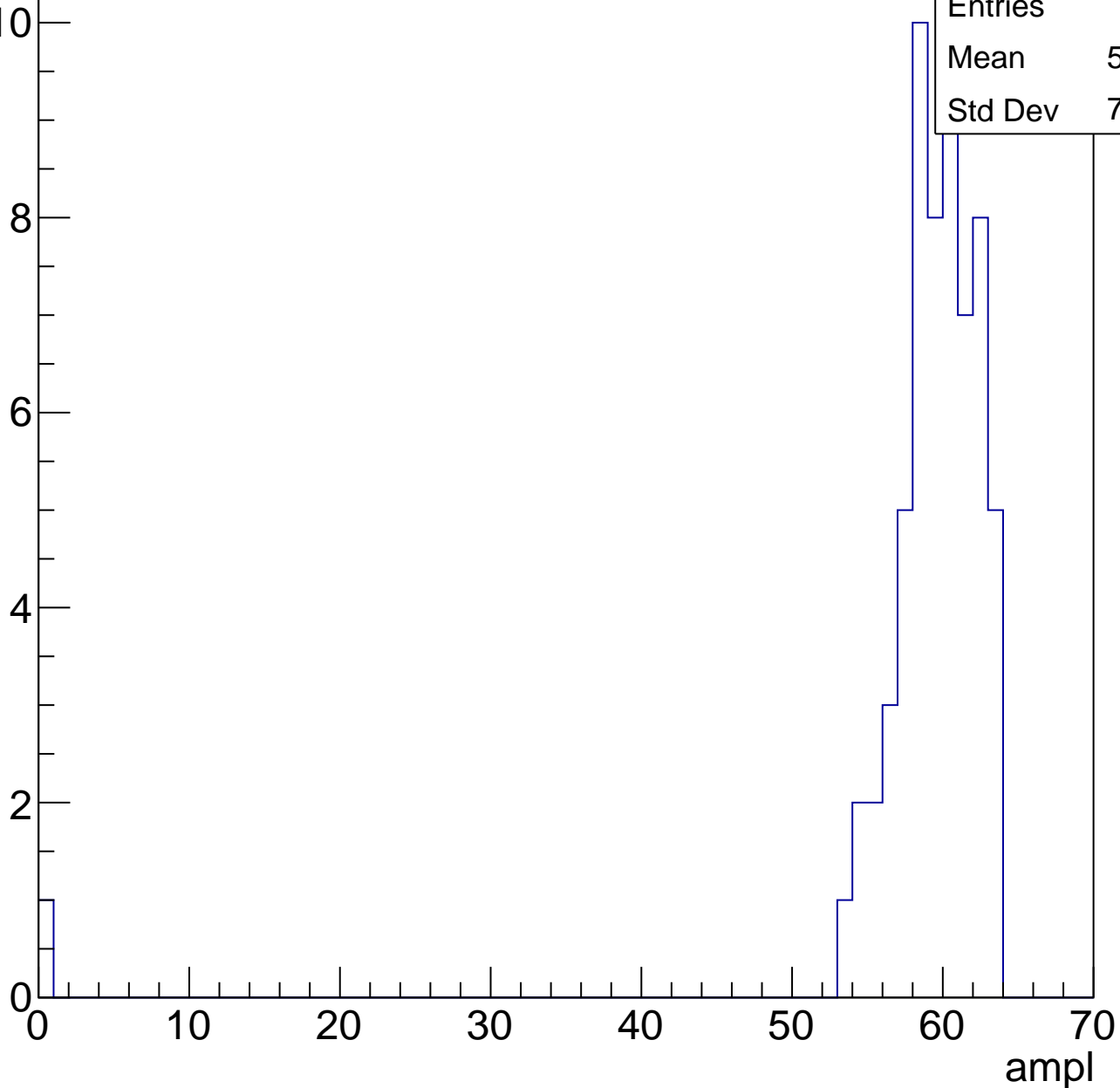


B1L103S, U23-ch97, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	58.26
Std Dev	7.905



B1L103S, U23-ch97, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch97, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.1
Std Dev	13.51

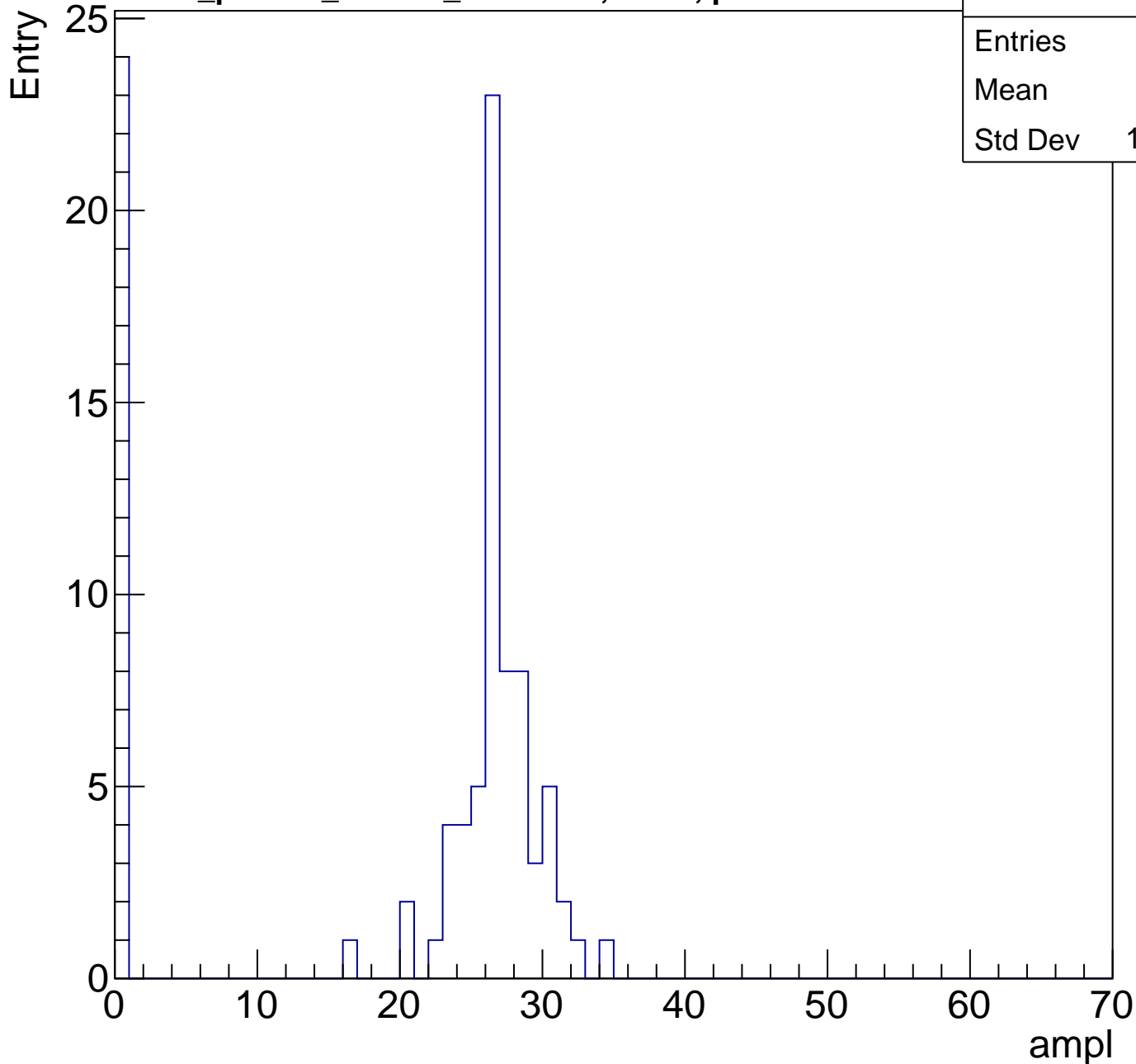
Entry



B1L103S, U23-ch98, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	92
Mean	19.5
Std Dev	11.83



B1L103S, U23-ch98, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	100
Mean	28.22
Std Dev	11.5

Entry

12

10

8

6

4

2

0

0

10

20

30

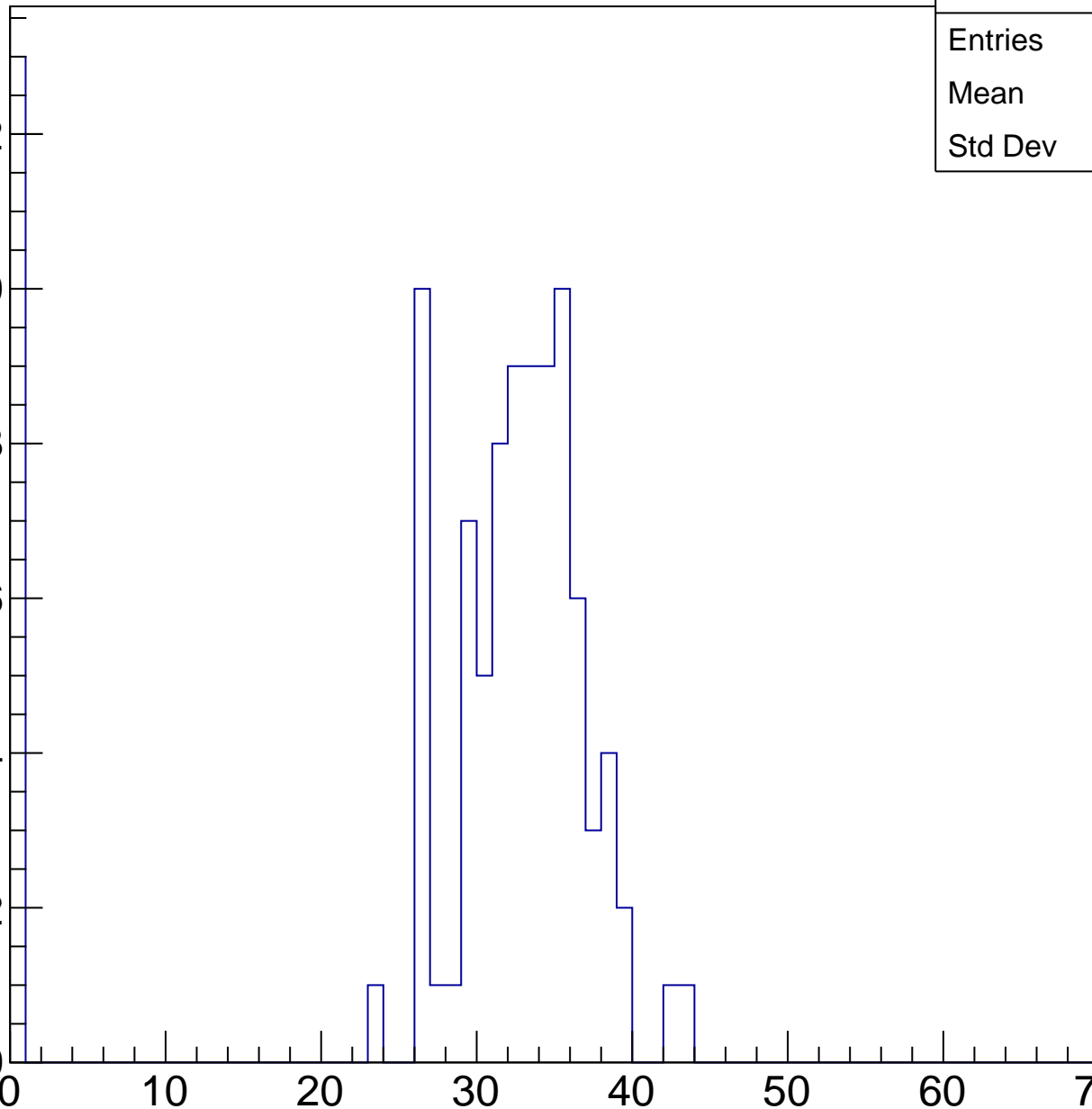
40

50

60

70

ampl

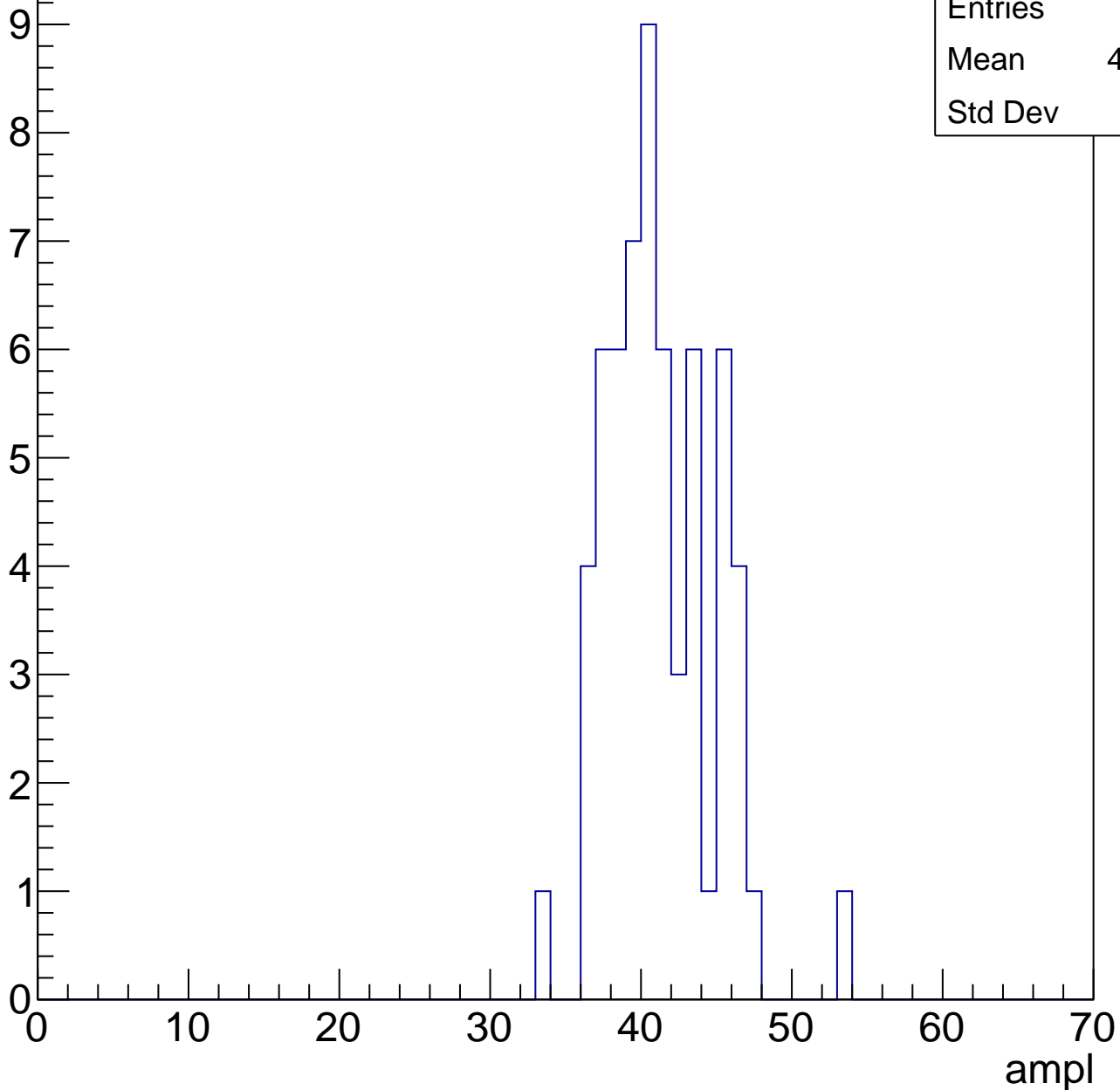


B1L103S, U23-ch98, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	40.79
Std Dev	3.53

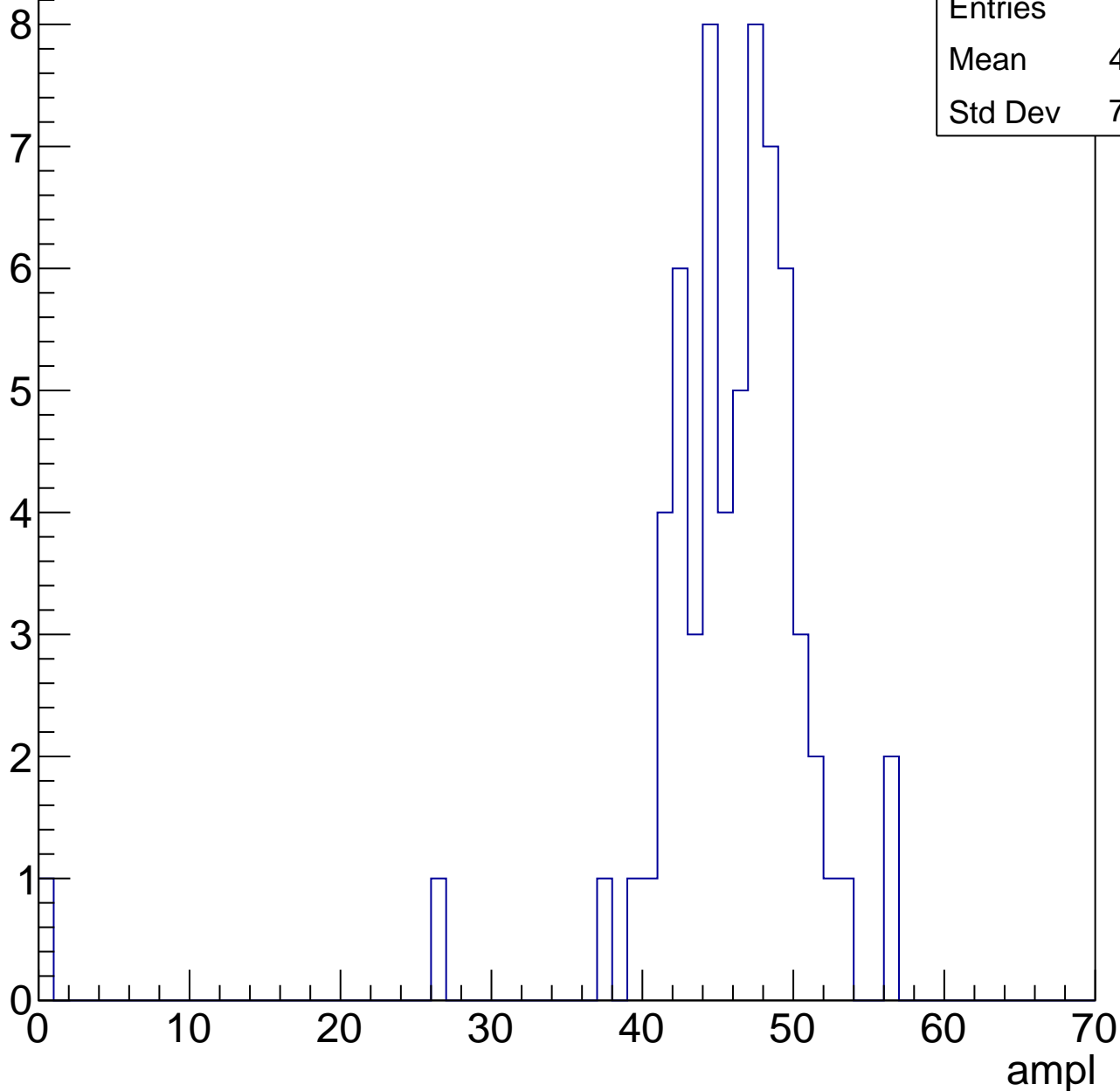


B1L103S, U23-ch98, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	44.98
Std Dev	7.176

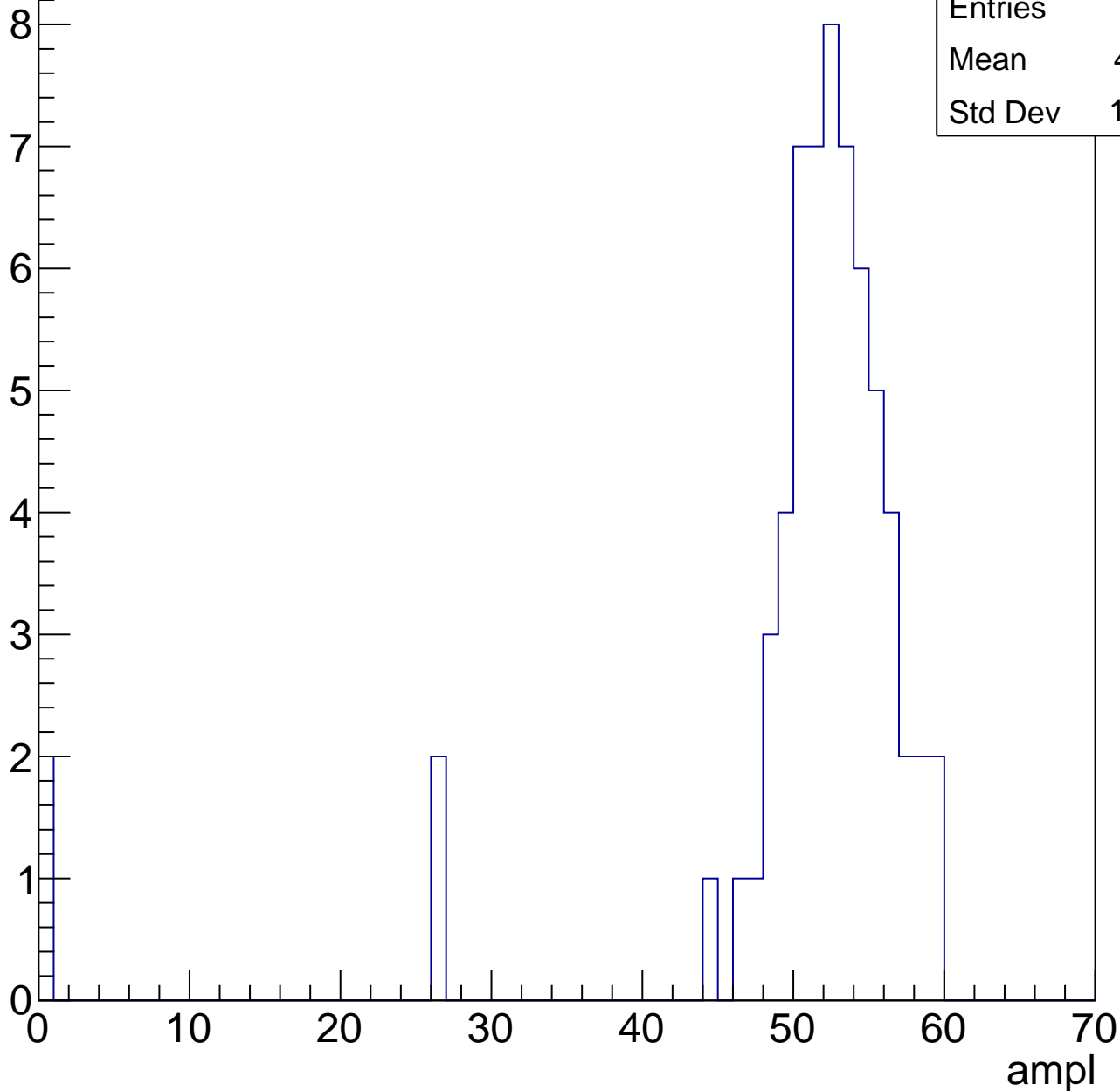


B1L103S, U23-ch98, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	49.91
Std Dev	10.52

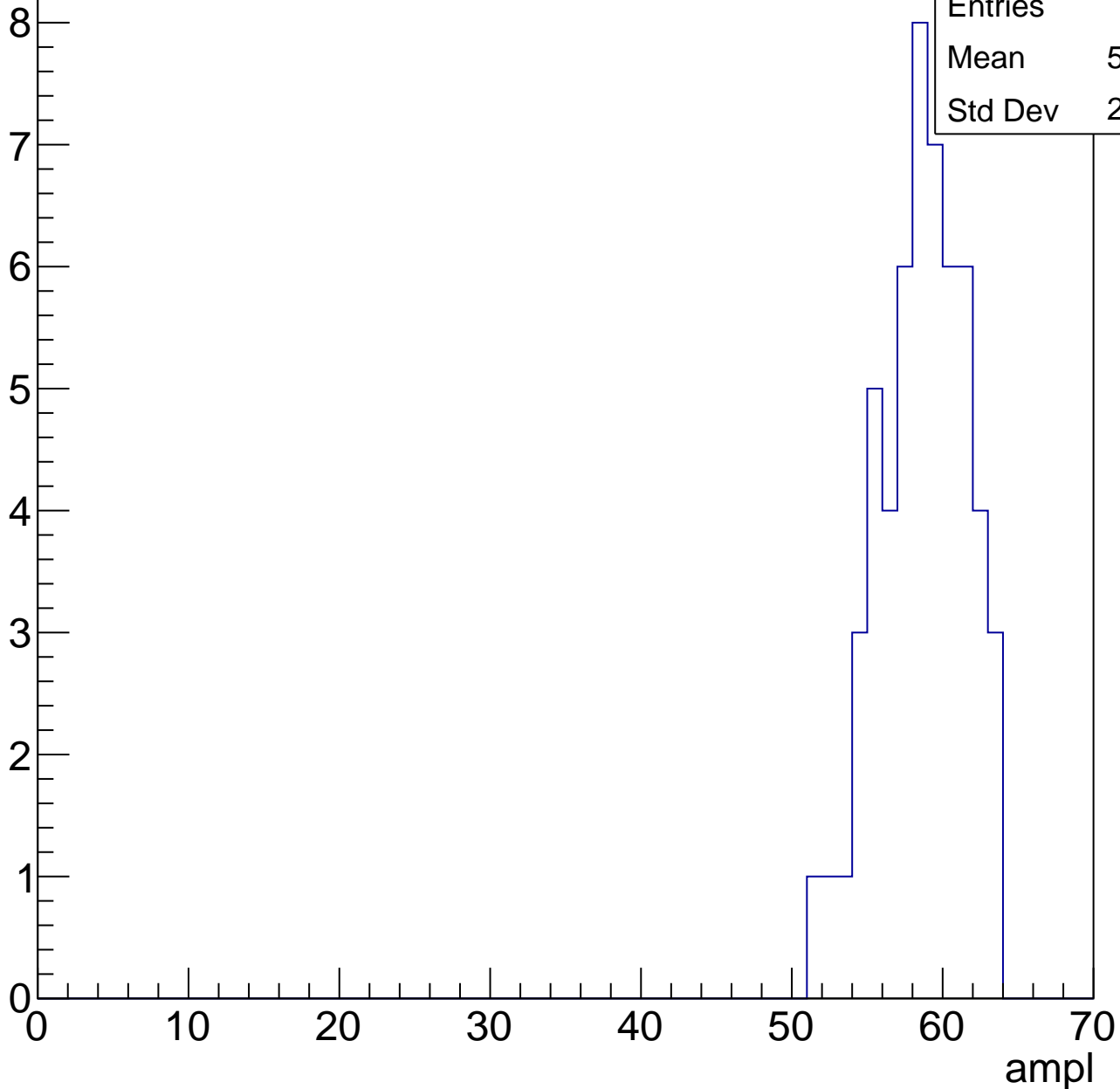


B1L103S, U23-ch98, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	58.16
Std Dev	2.853

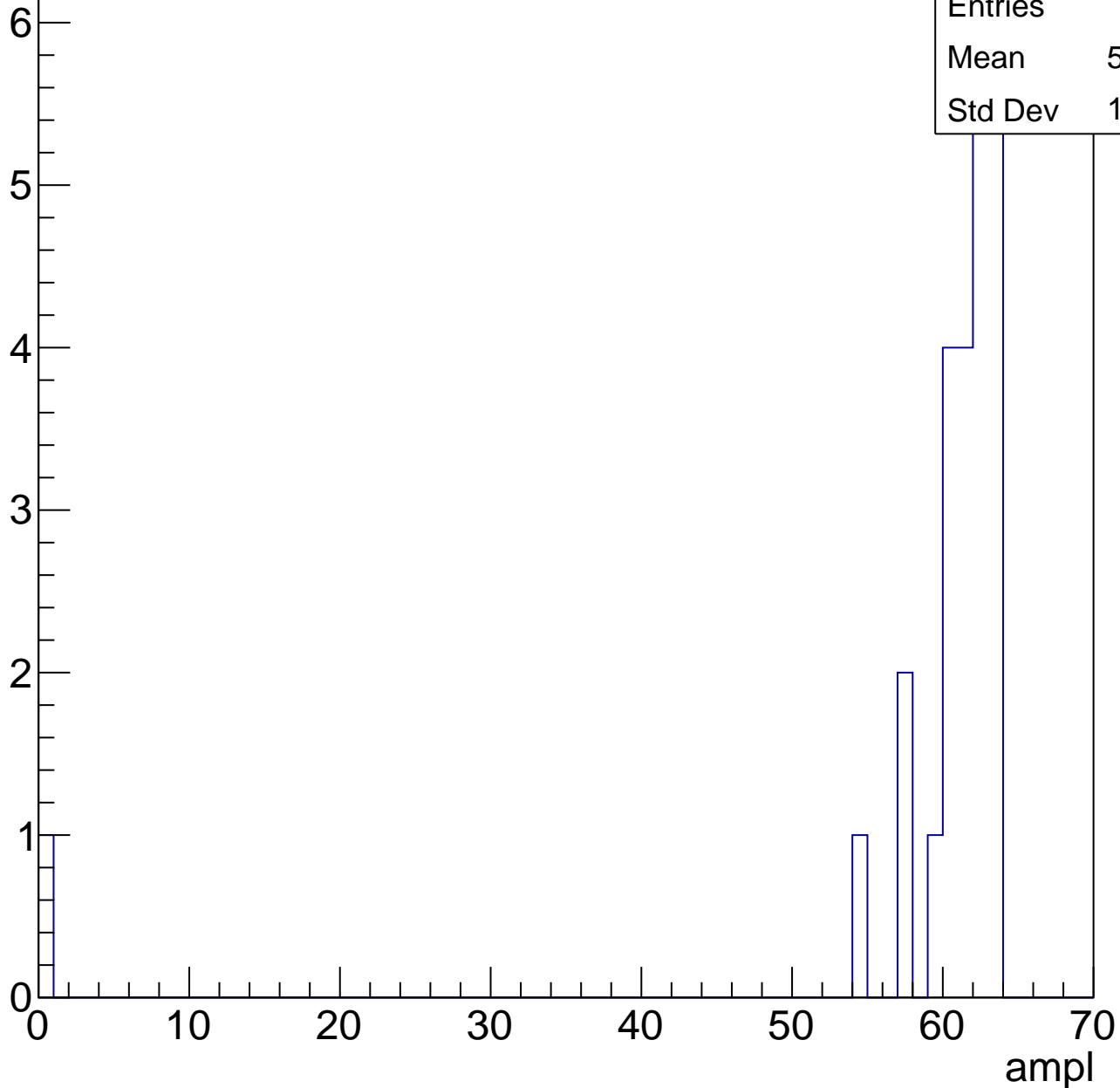


B1L103S, U23-ch98, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	25
Mean	58.44
Std Dev	12.13

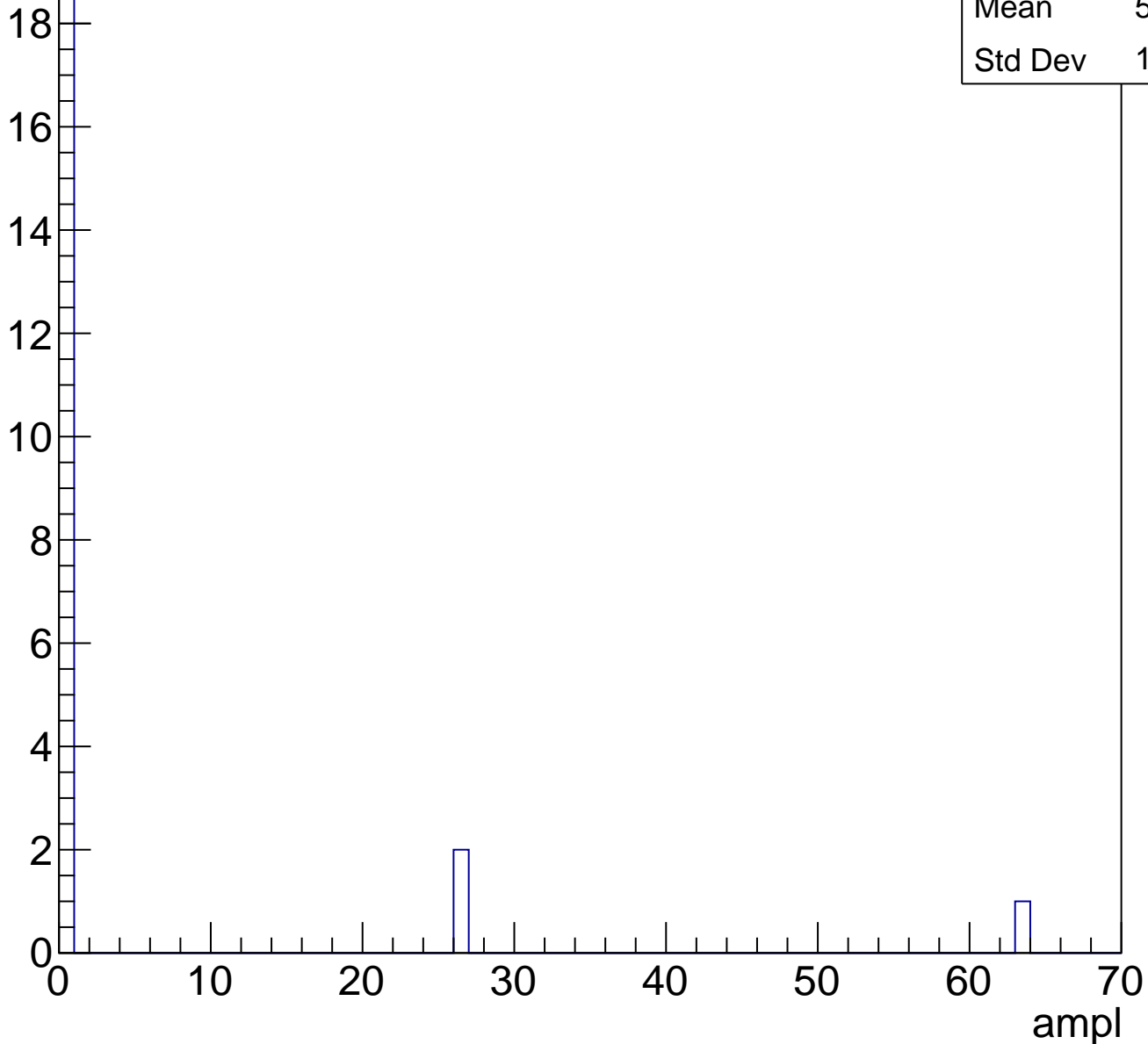


B1L103S, U23-ch98, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	22
Mean	5.227
Std Dev	14.65

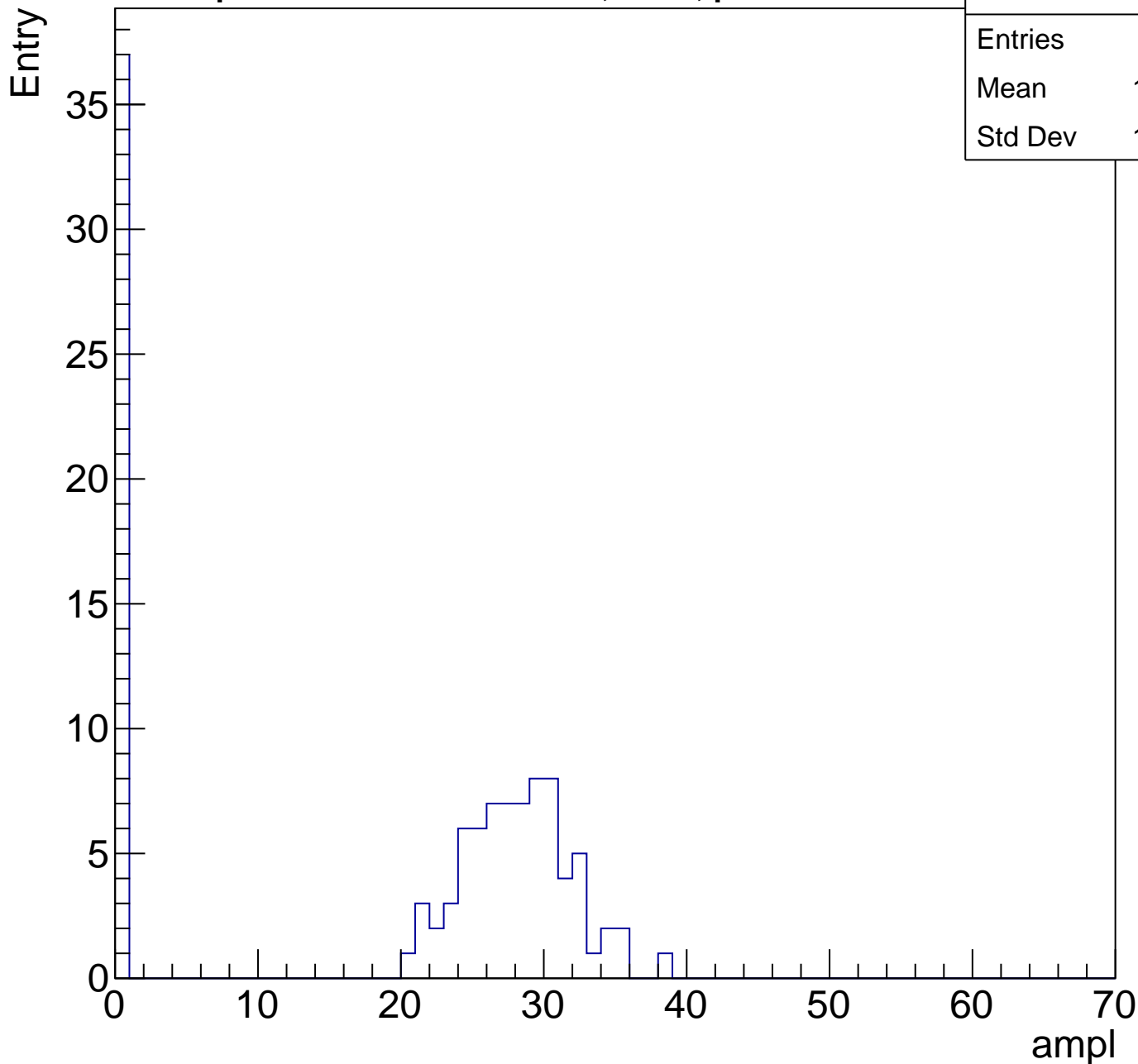
Entry



B1L103S, U23-ch99, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	110
Mean	18.38
Std Dev	13.43

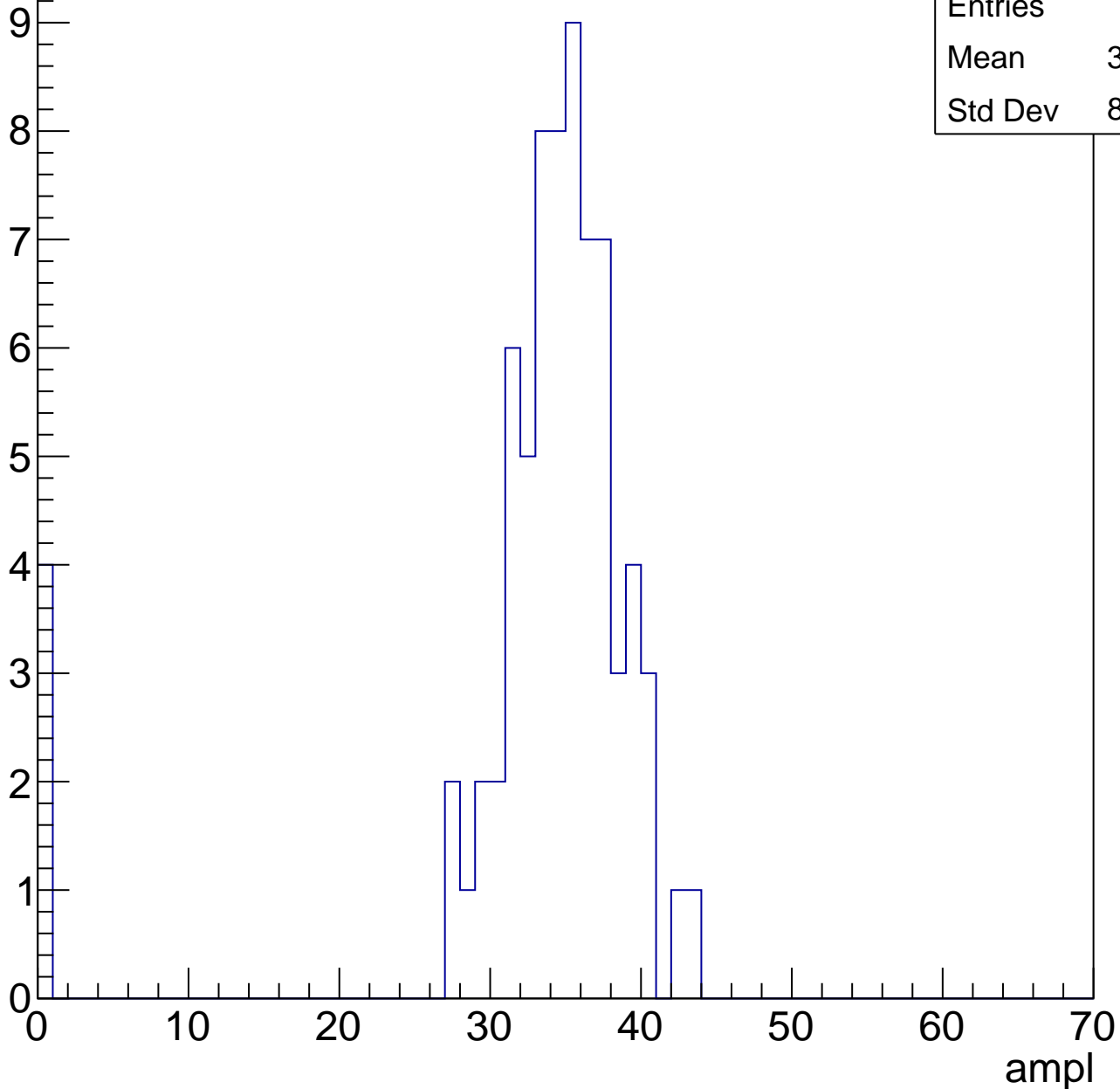


B1L103S, U23-ch99, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	73
Mean	32.64
Std Dev	8.512

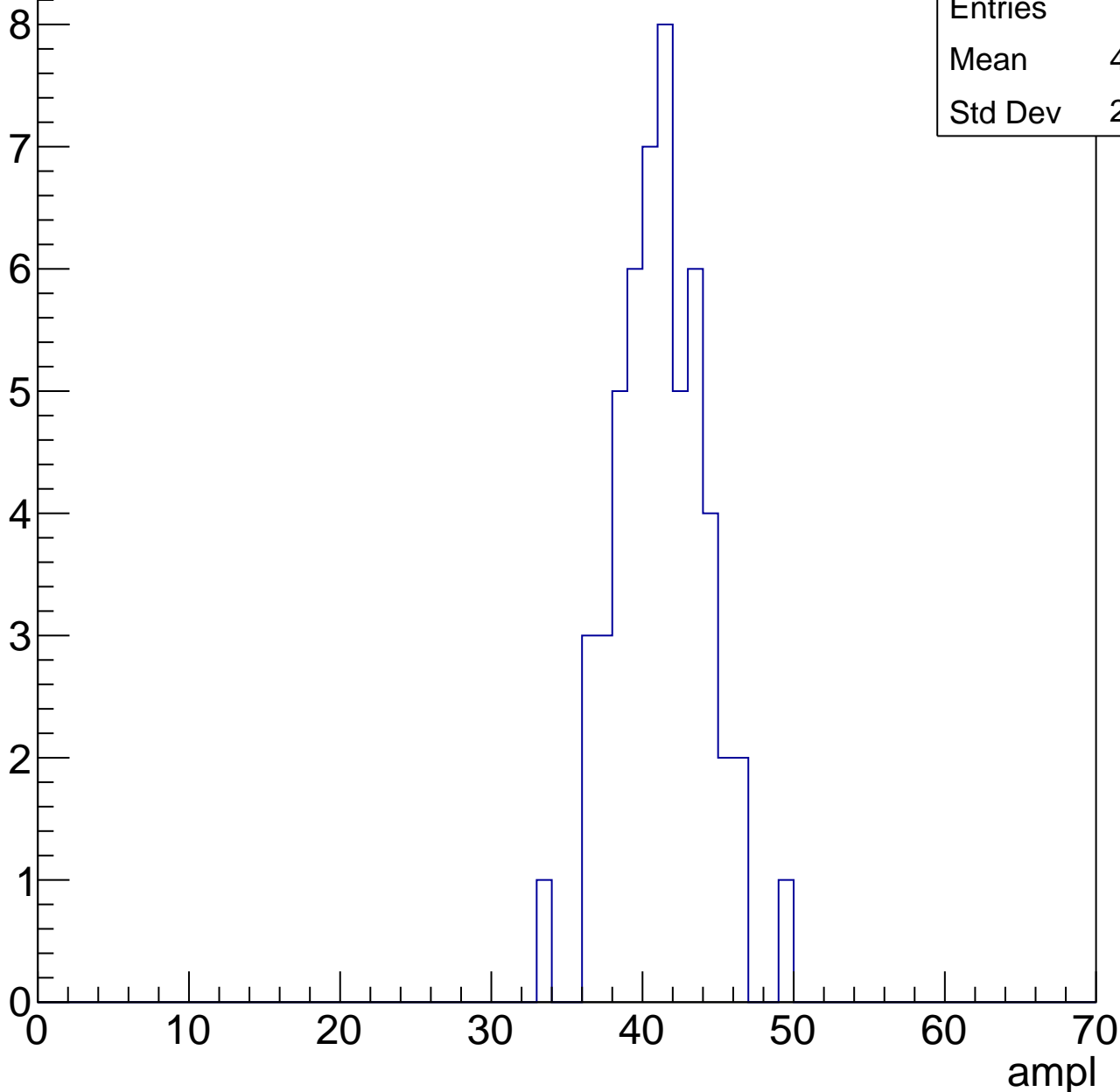


B1L103S, U23-ch99, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	53
Mean	40.74
Std Dev	2.979

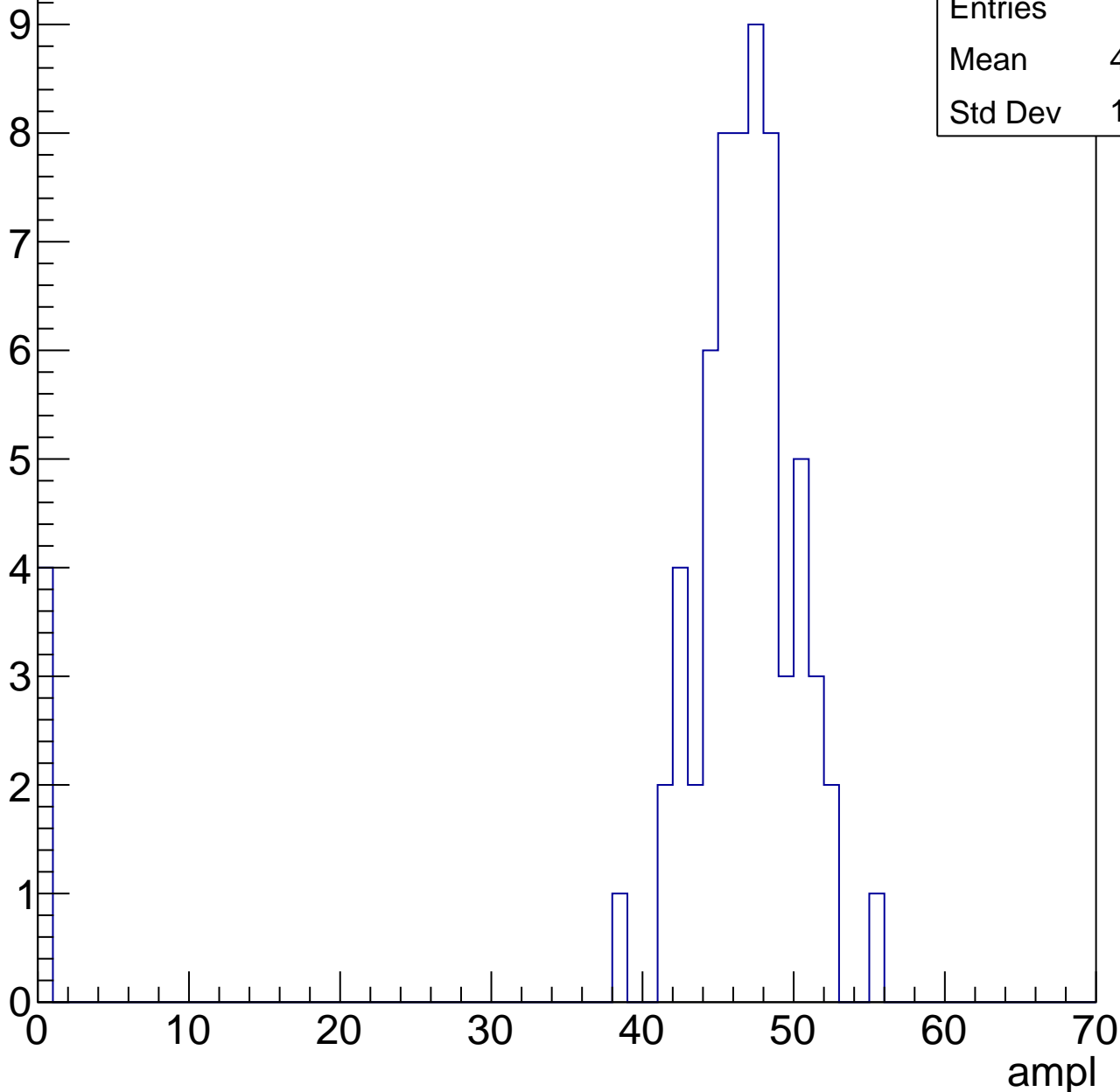


B1L103S, U23-ch99, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	43.67
Std Dev	11.49

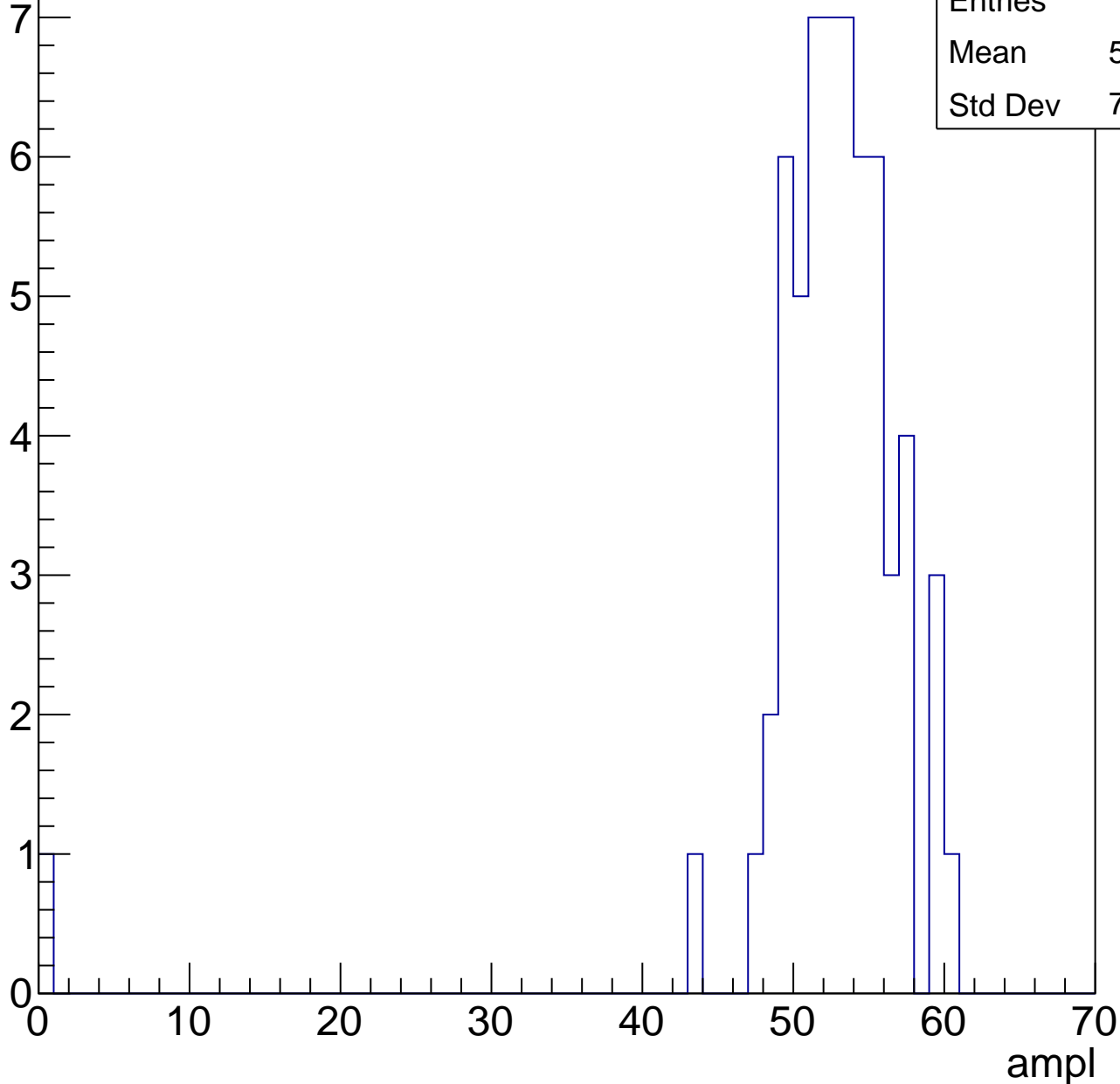


B1L103S, U23-ch99, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	51.82
Std Dev	7.489

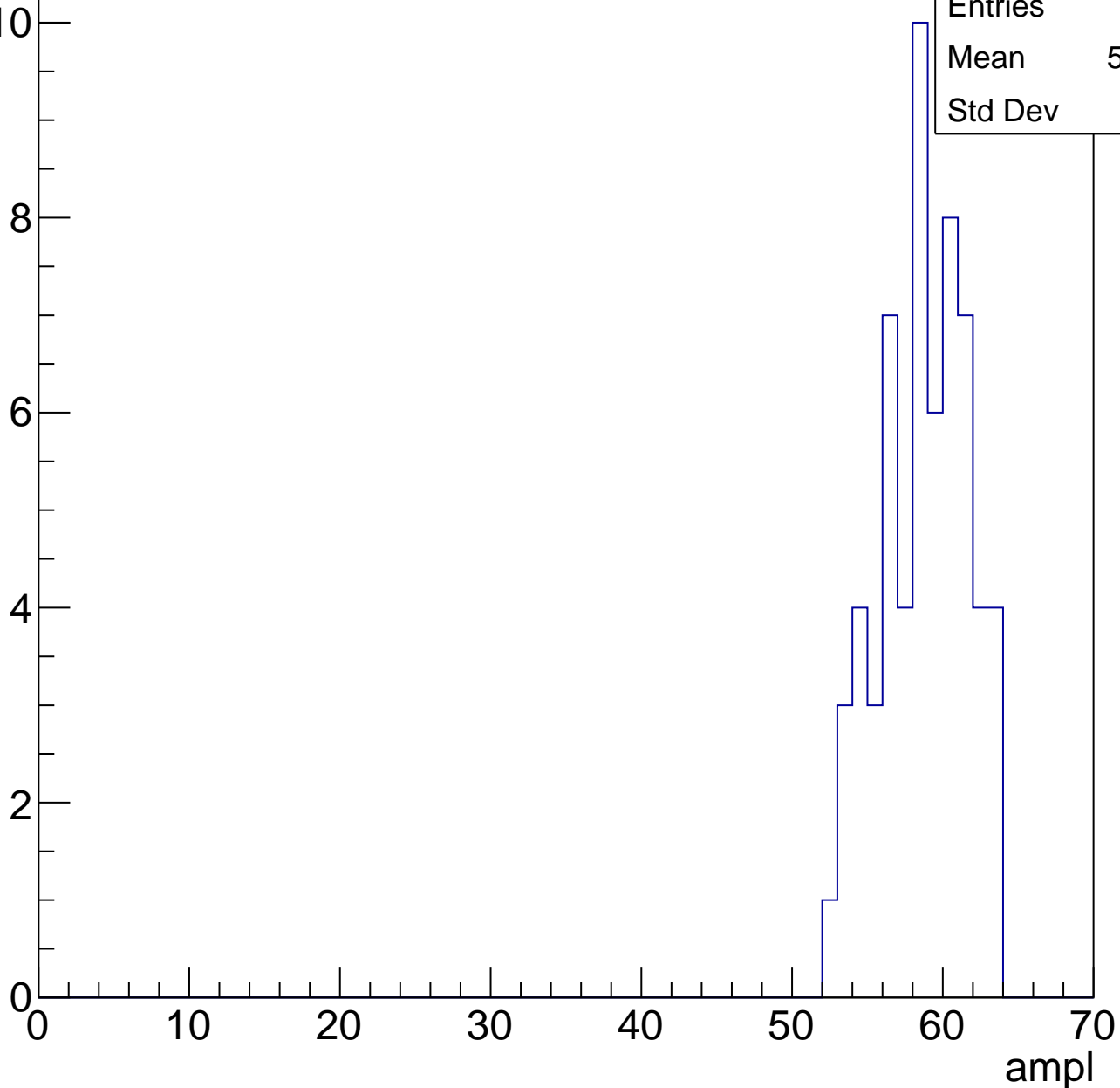


B1L103S, U23-ch99, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	58.25
Std Dev	2.85

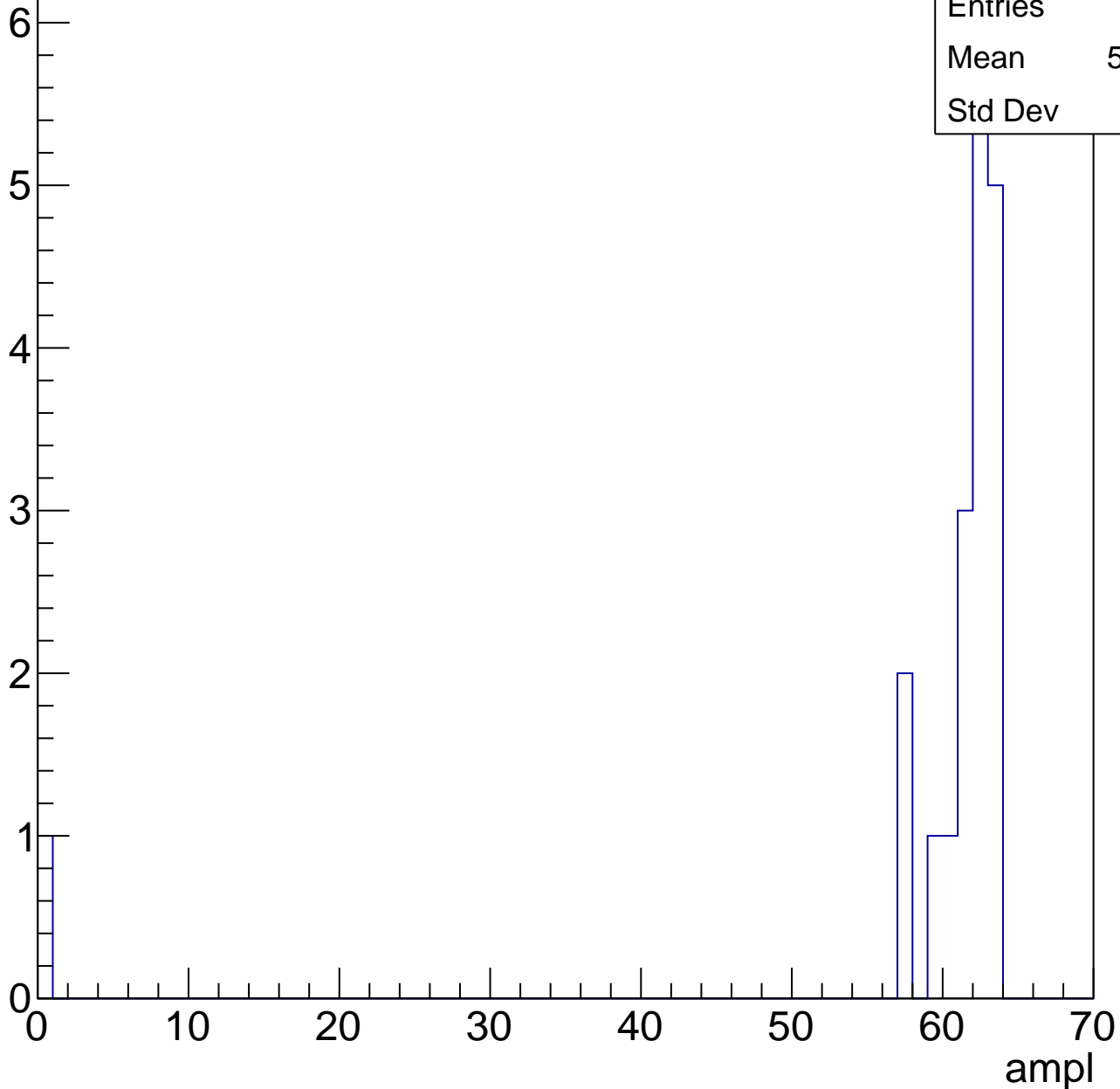


B1L103S, U23-ch99, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	19
Mean	58.05
Std Dev	13.8

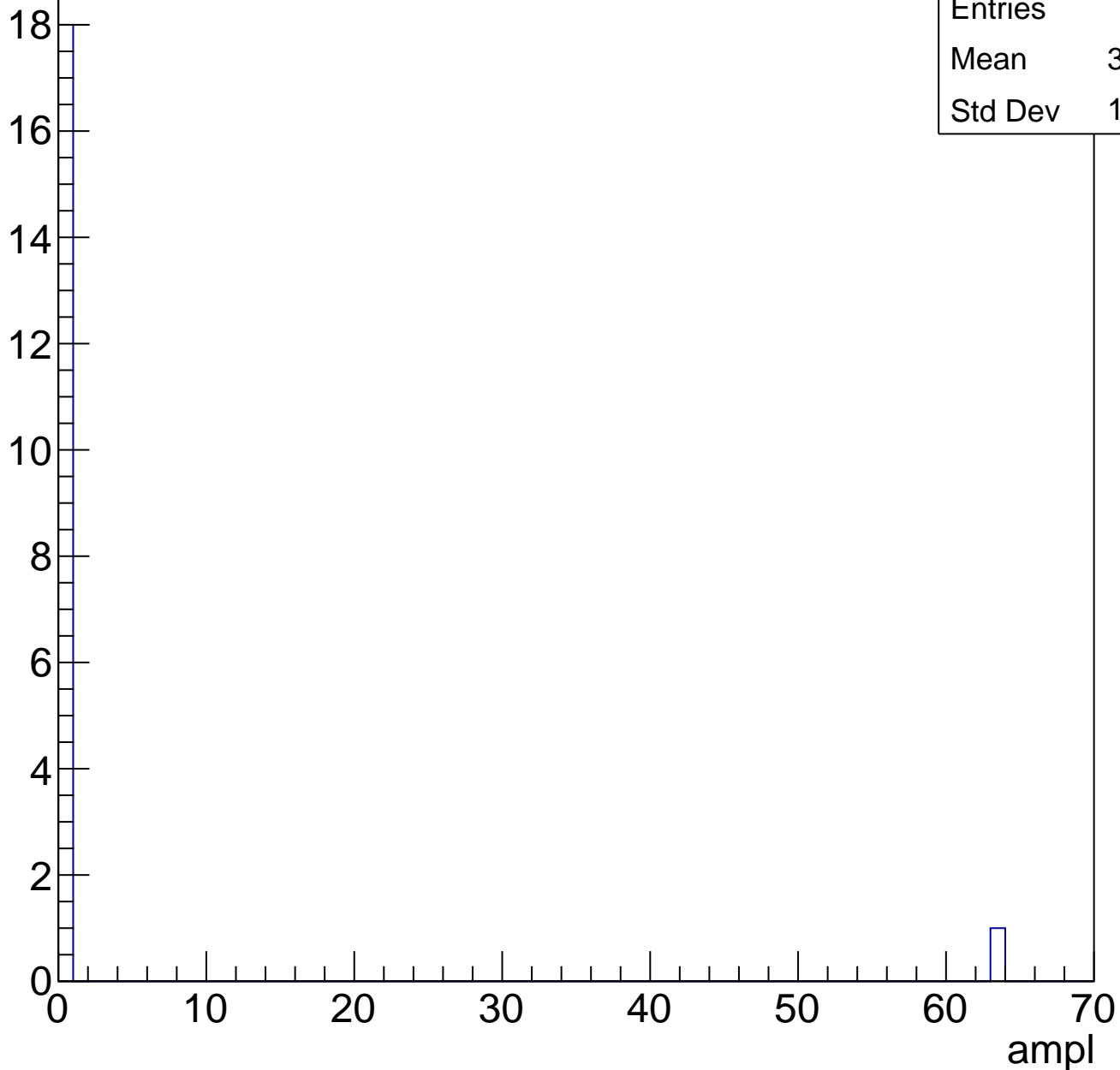


B1L103S, U23-ch99, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	3.316
Std Dev	14.07

Entry

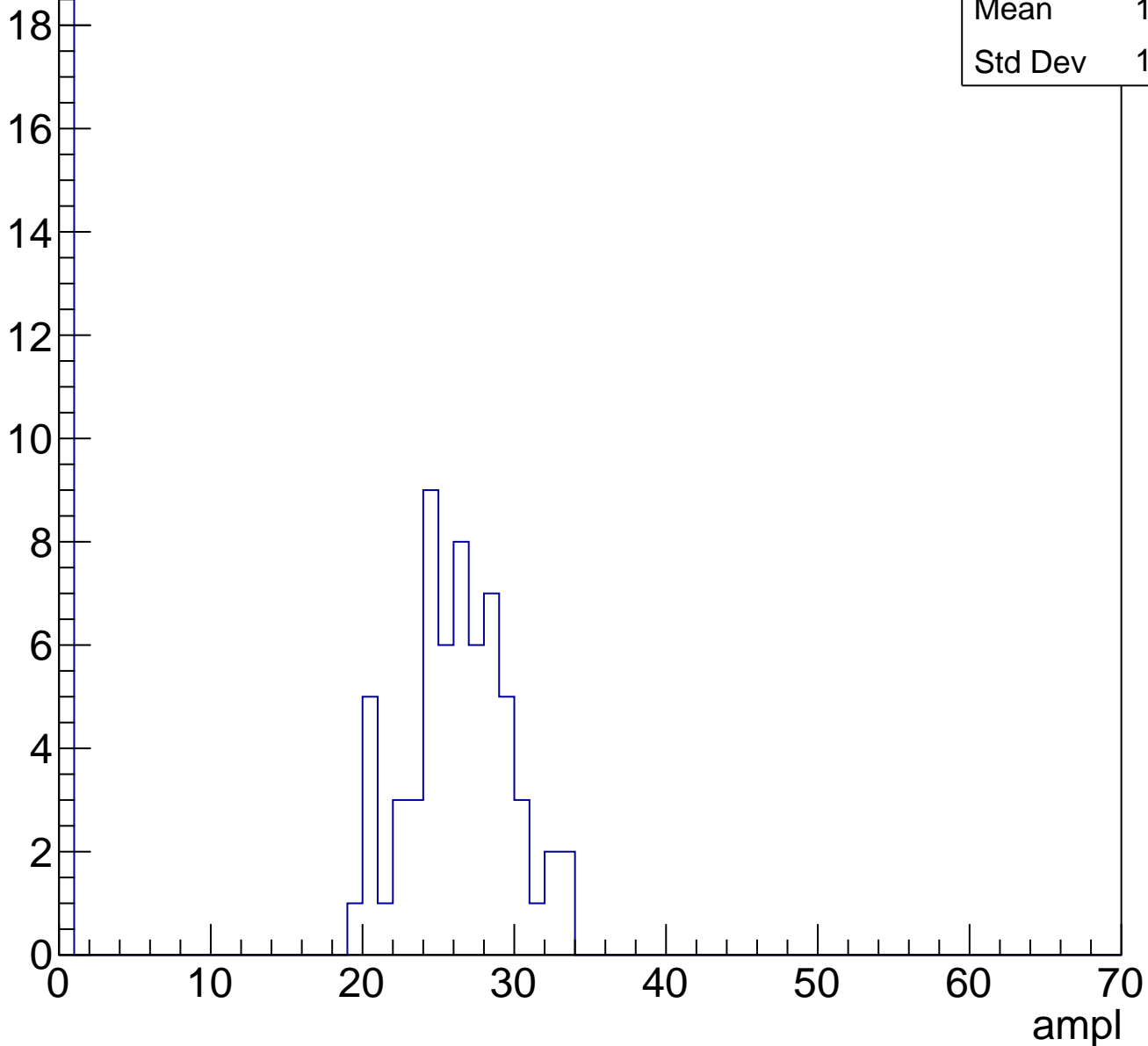


B1L103S, U23-ch100, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	81
Mean	19.79
Std Dev	11.34

Entry

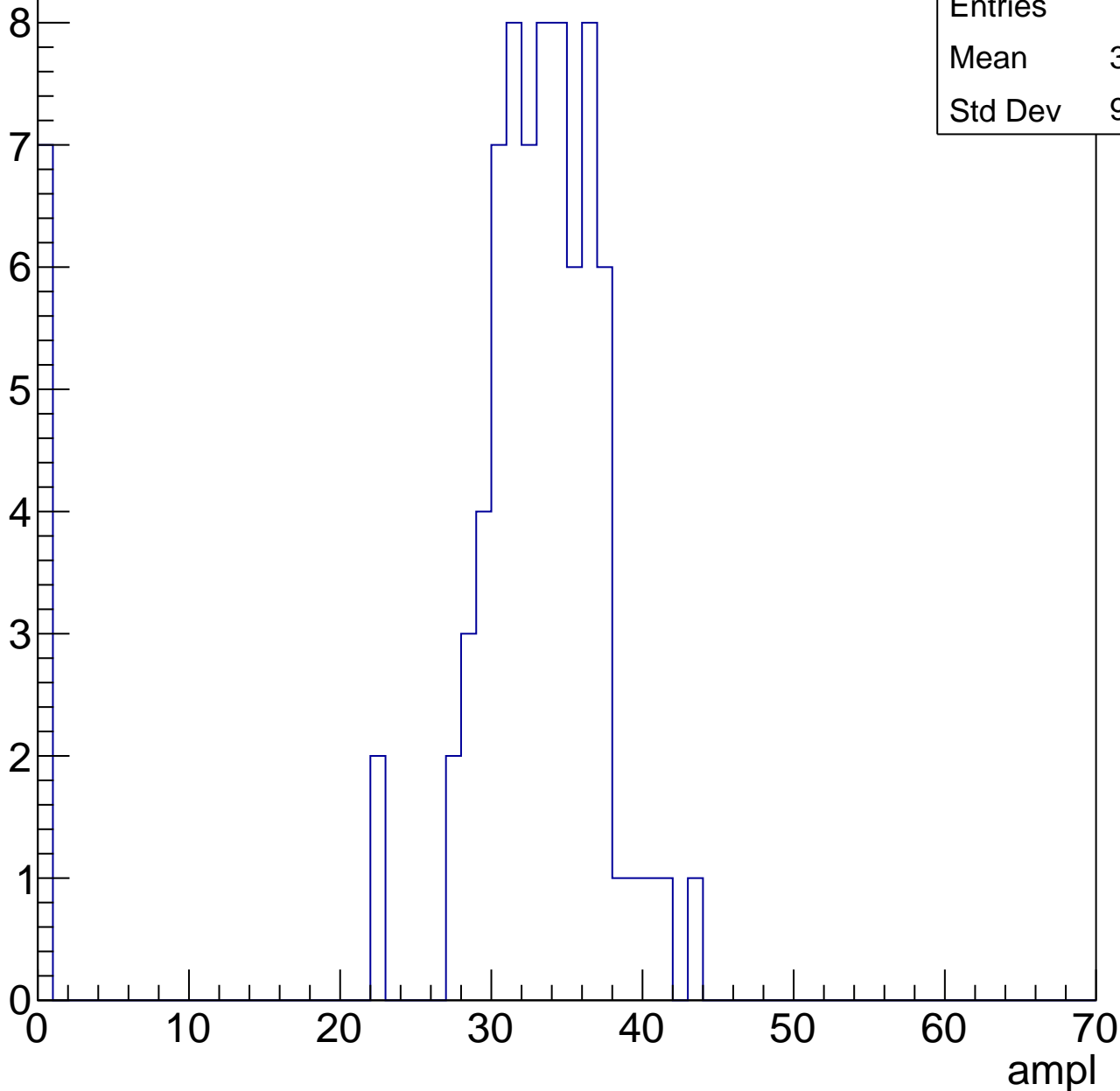


B1L103S, U23-ch100, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	81
Mean	30.09
Std Dev	9.916

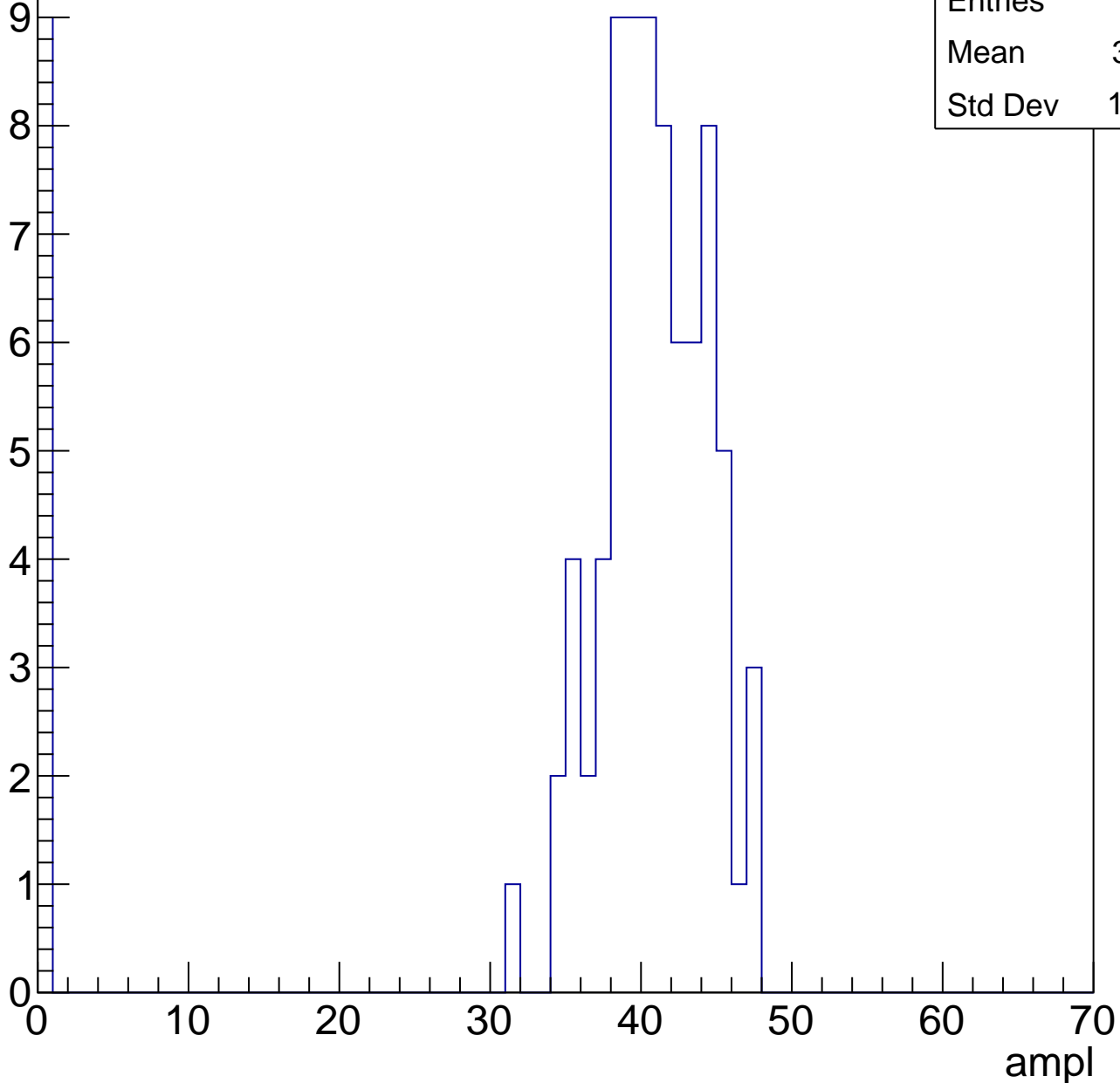


B1L103S, U23-ch100, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	86
Mean	36.21
Std Dev	12.78

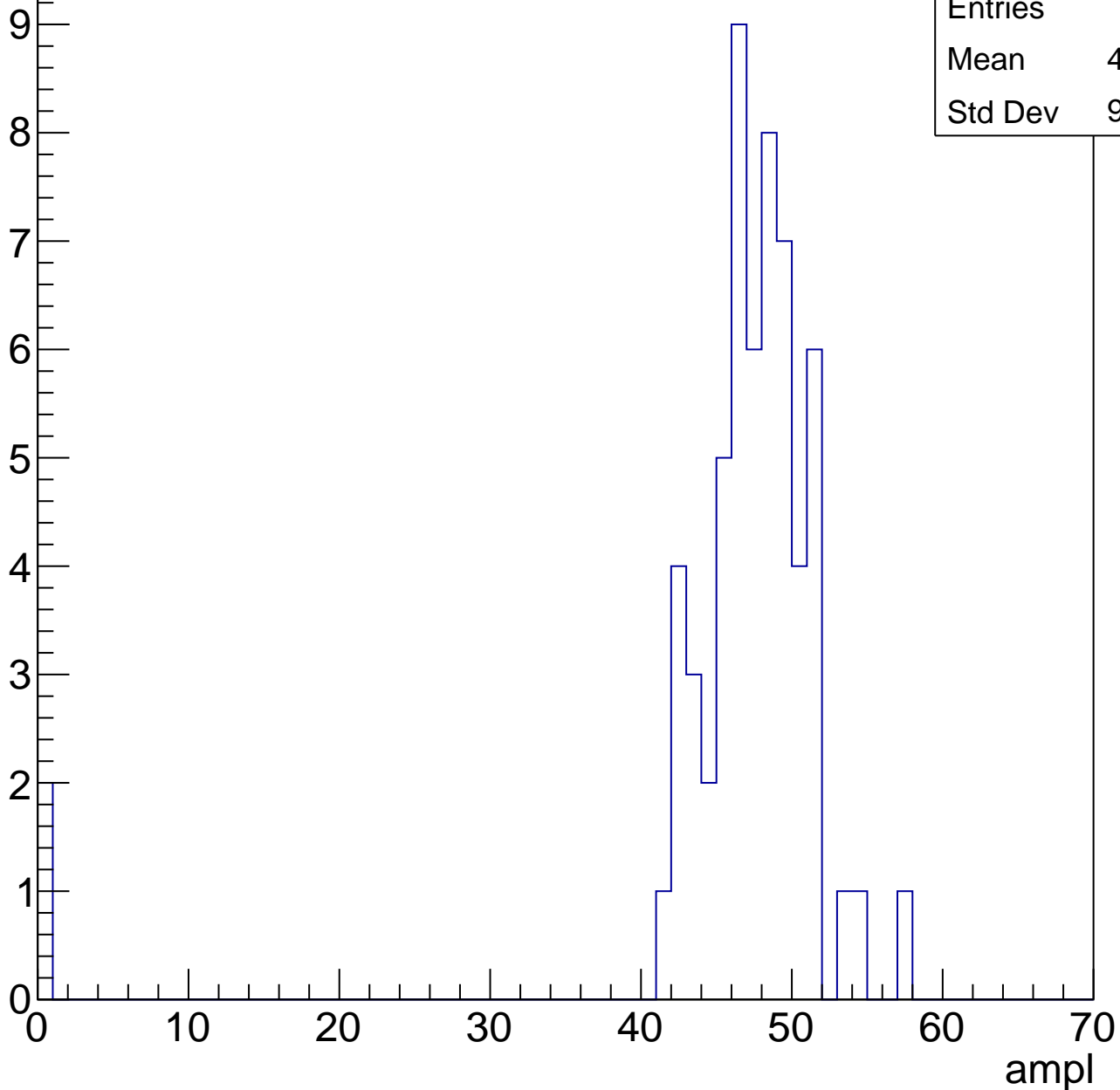


B1L103S, U23-ch100, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	45.73
Std Dev	9.042

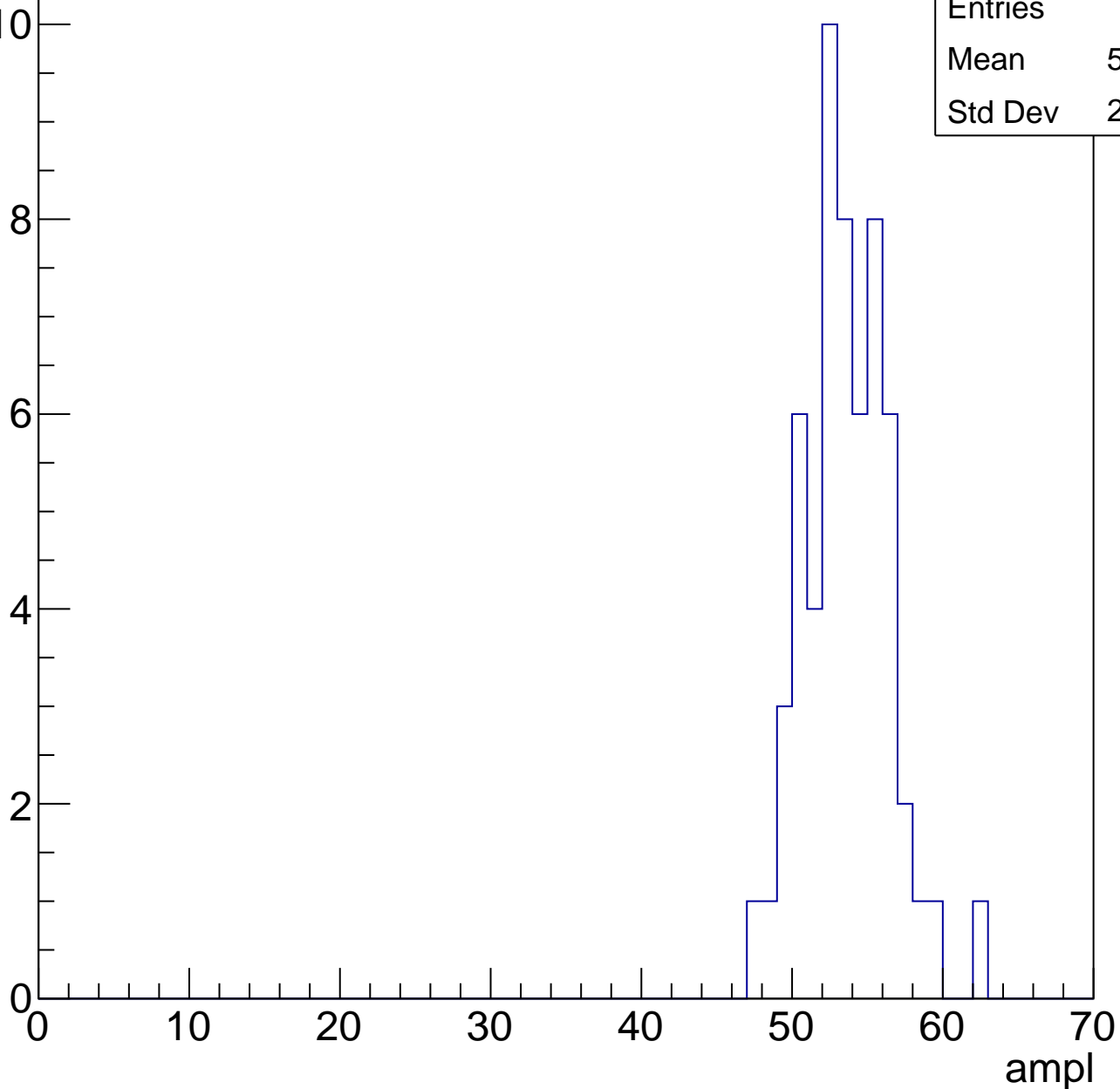


B1L103S, U23-ch100, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	53.16
Std Dev	2.797

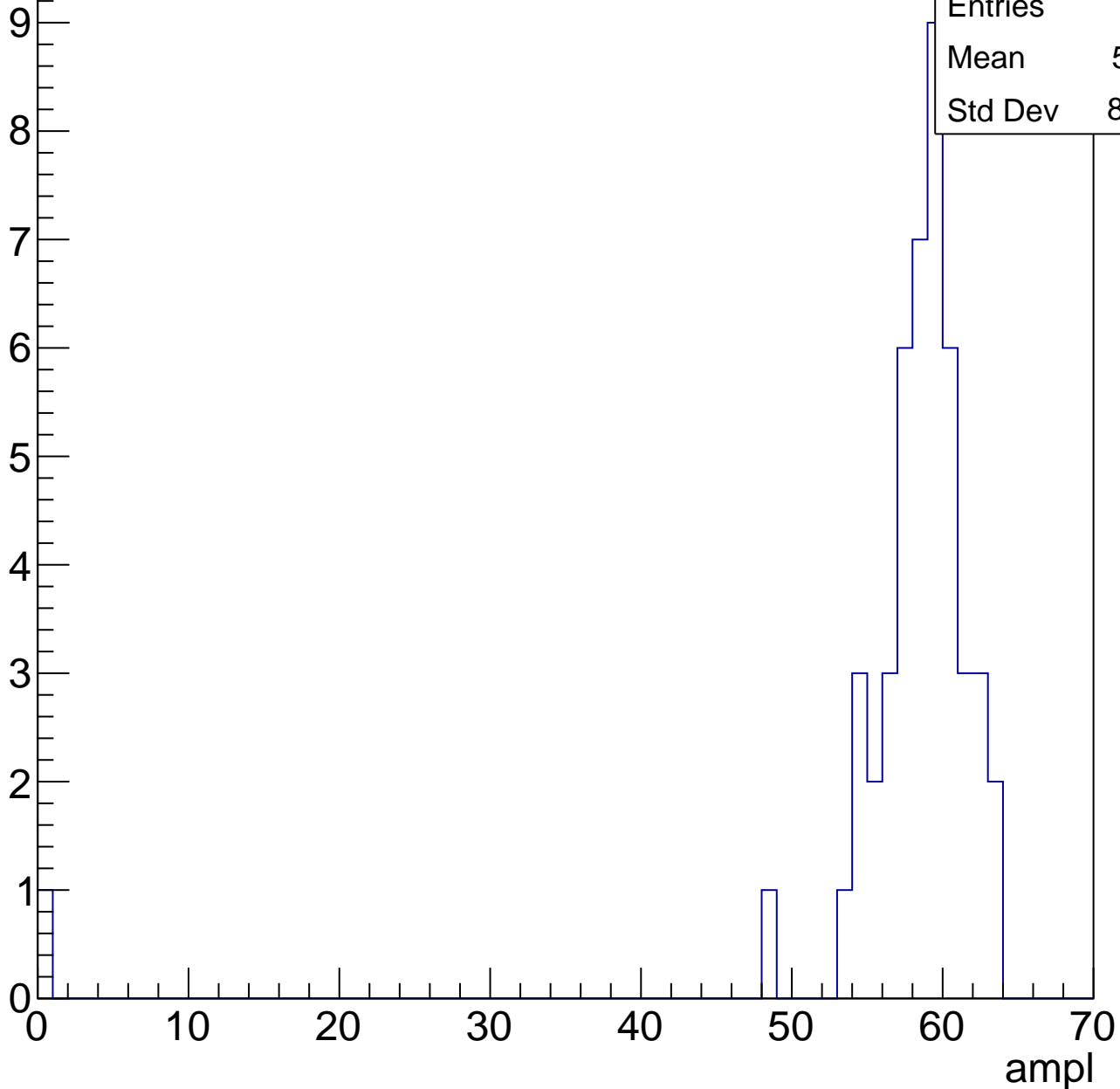


B1L103S, U23-ch100, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	47
Mean	56.91
Std Dev	8.843

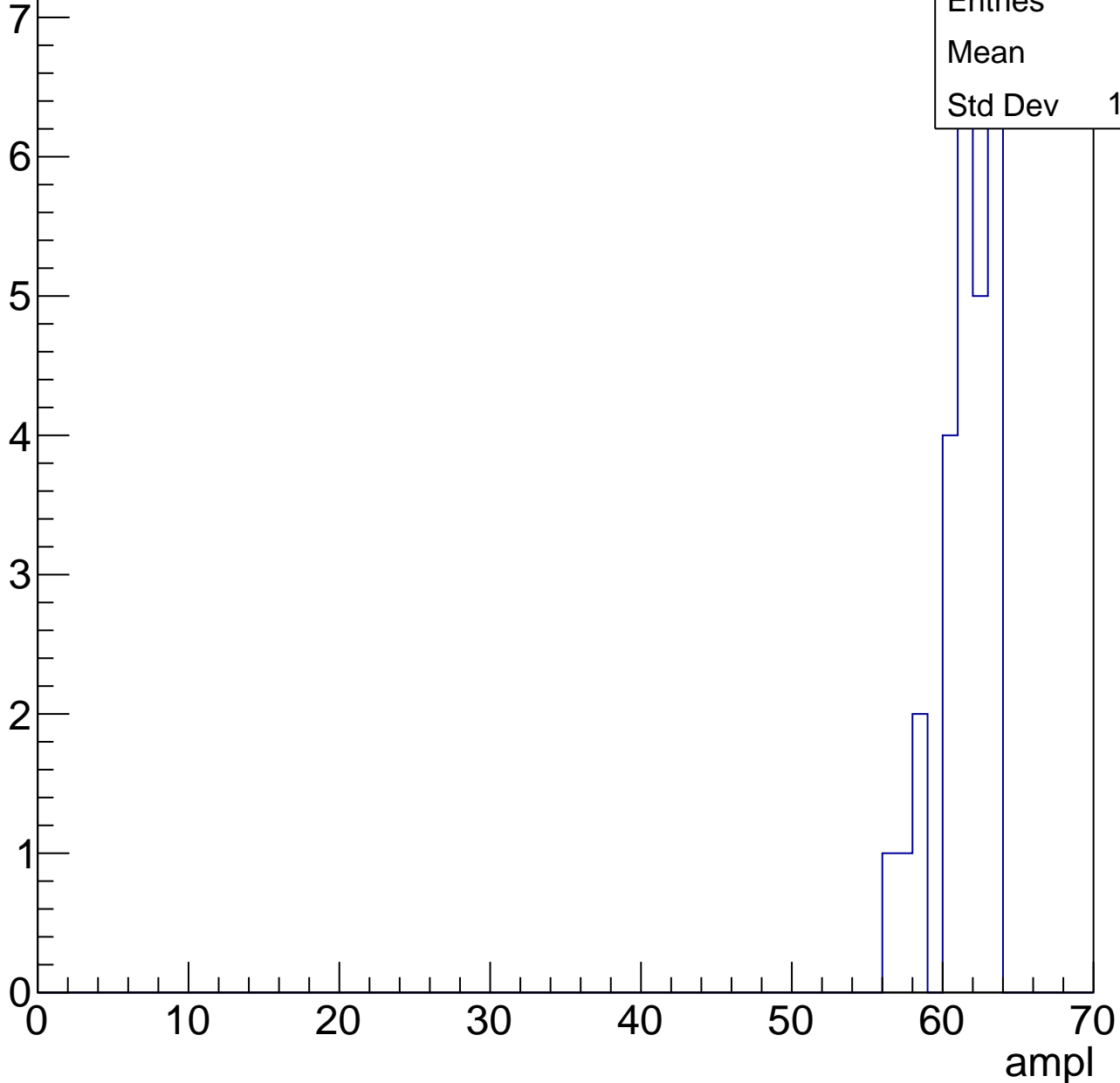


B1L103S, U23-ch100, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

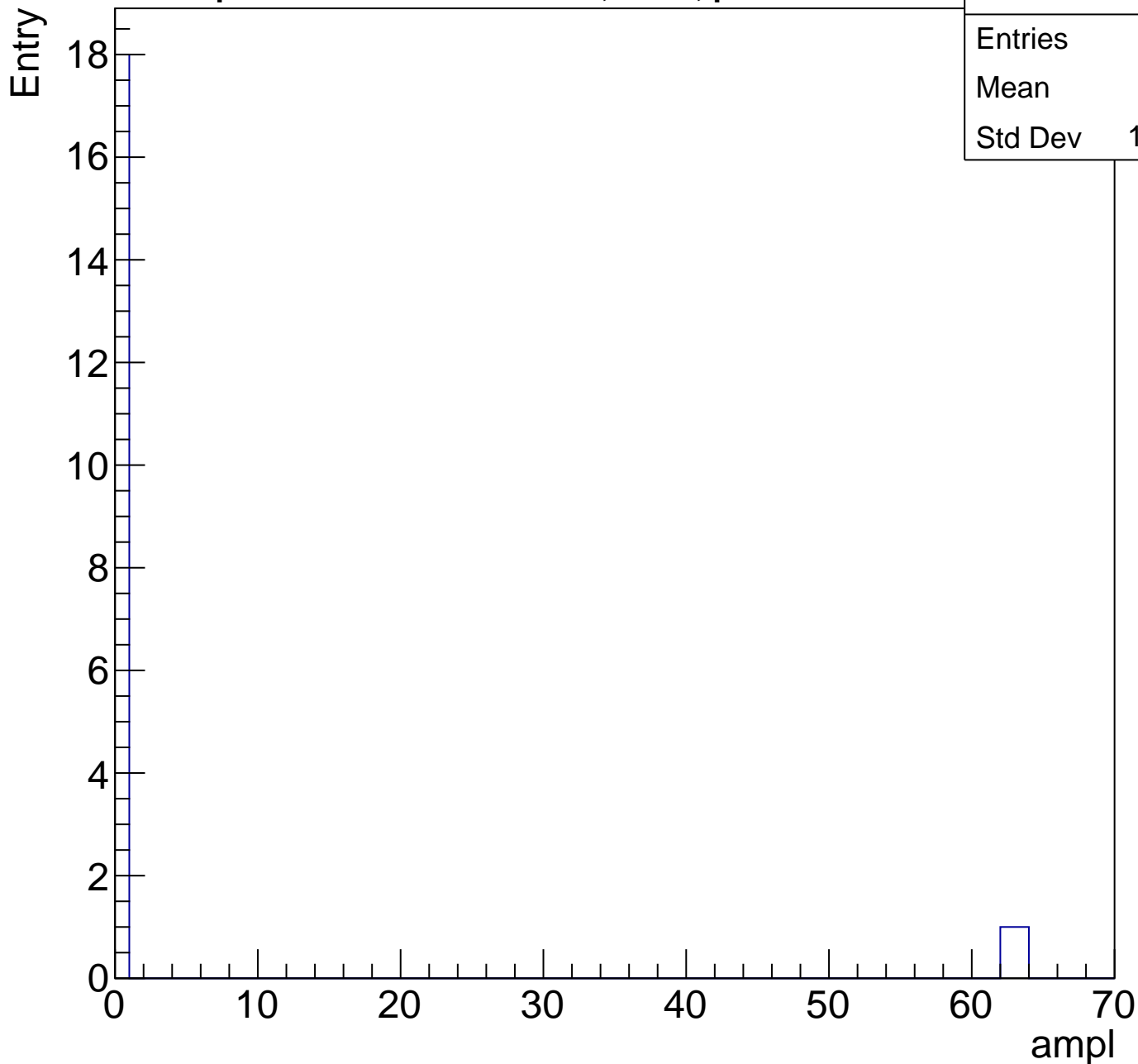
Entries	27
Mean	61
Std Dev	1.886



B1L103S, U23-ch100, adc7

calib_packv5_041523_1651.root, FC#0, port C2

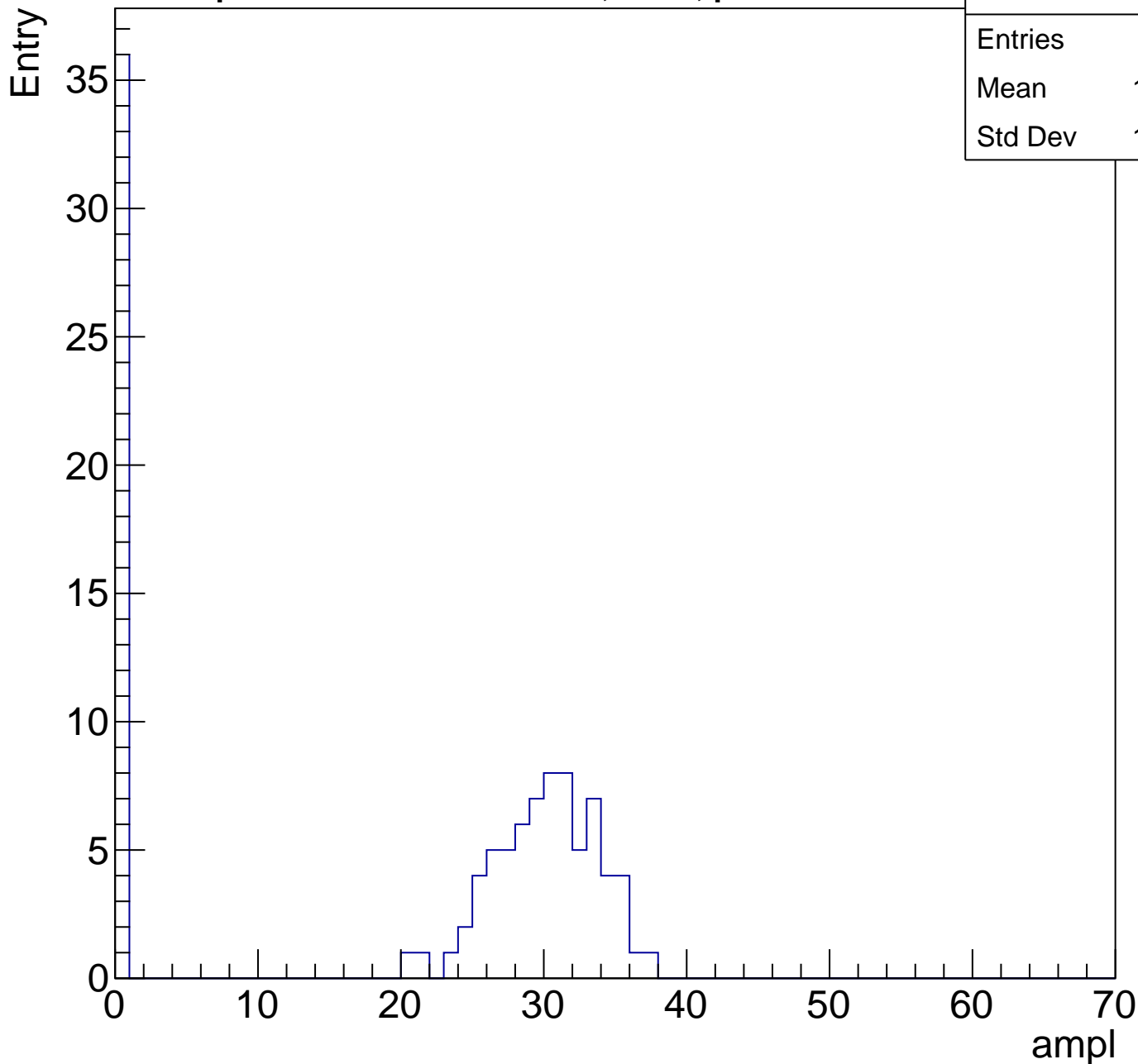
Entries	20
Mean	6.25
Std Dev	18.75



B1L103S, U23-ch101, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	106
Mean	19.58
Std Dev	14.34

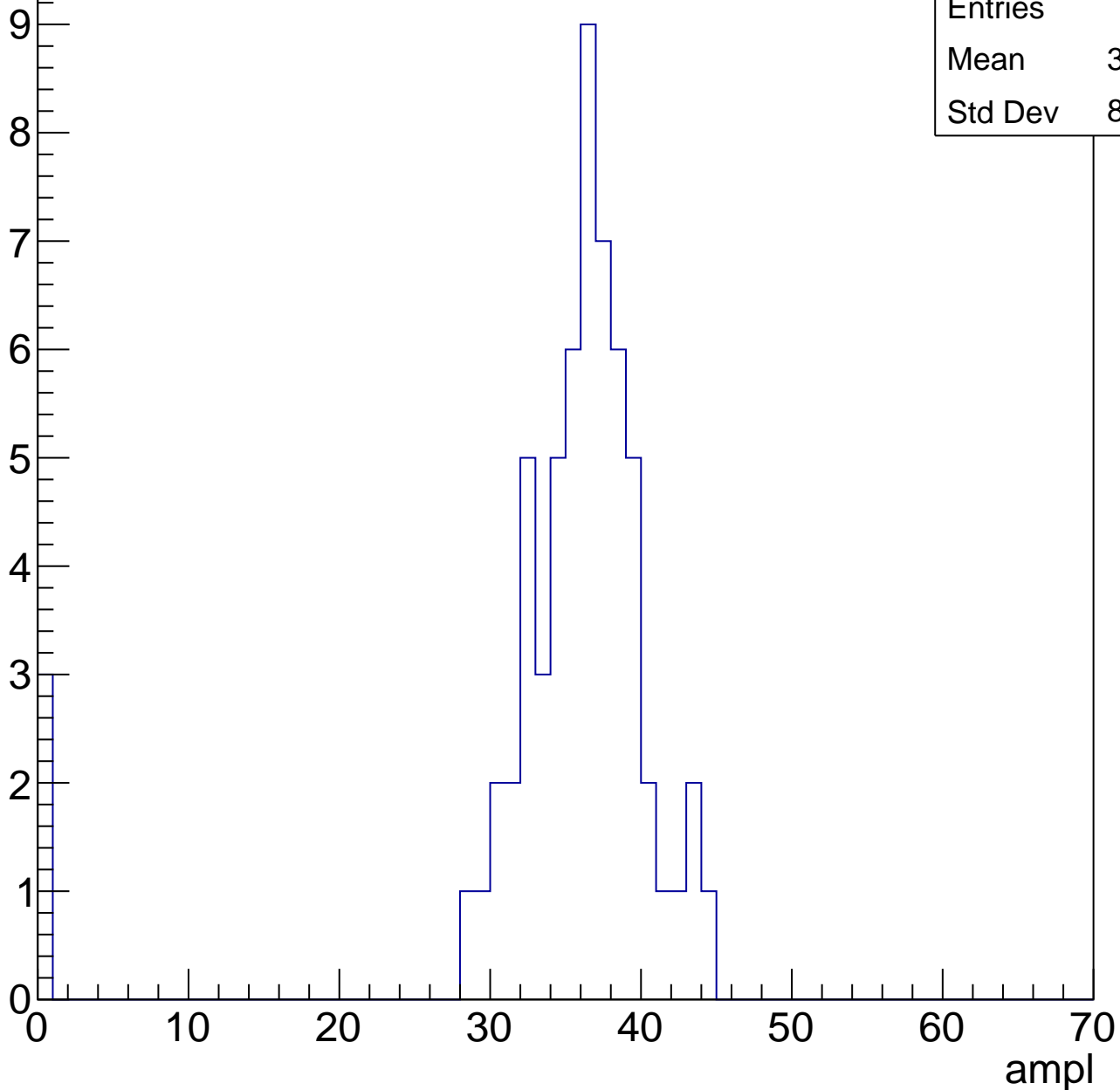


B1L103S, U23-ch101, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	34.15
Std Dev	8.399

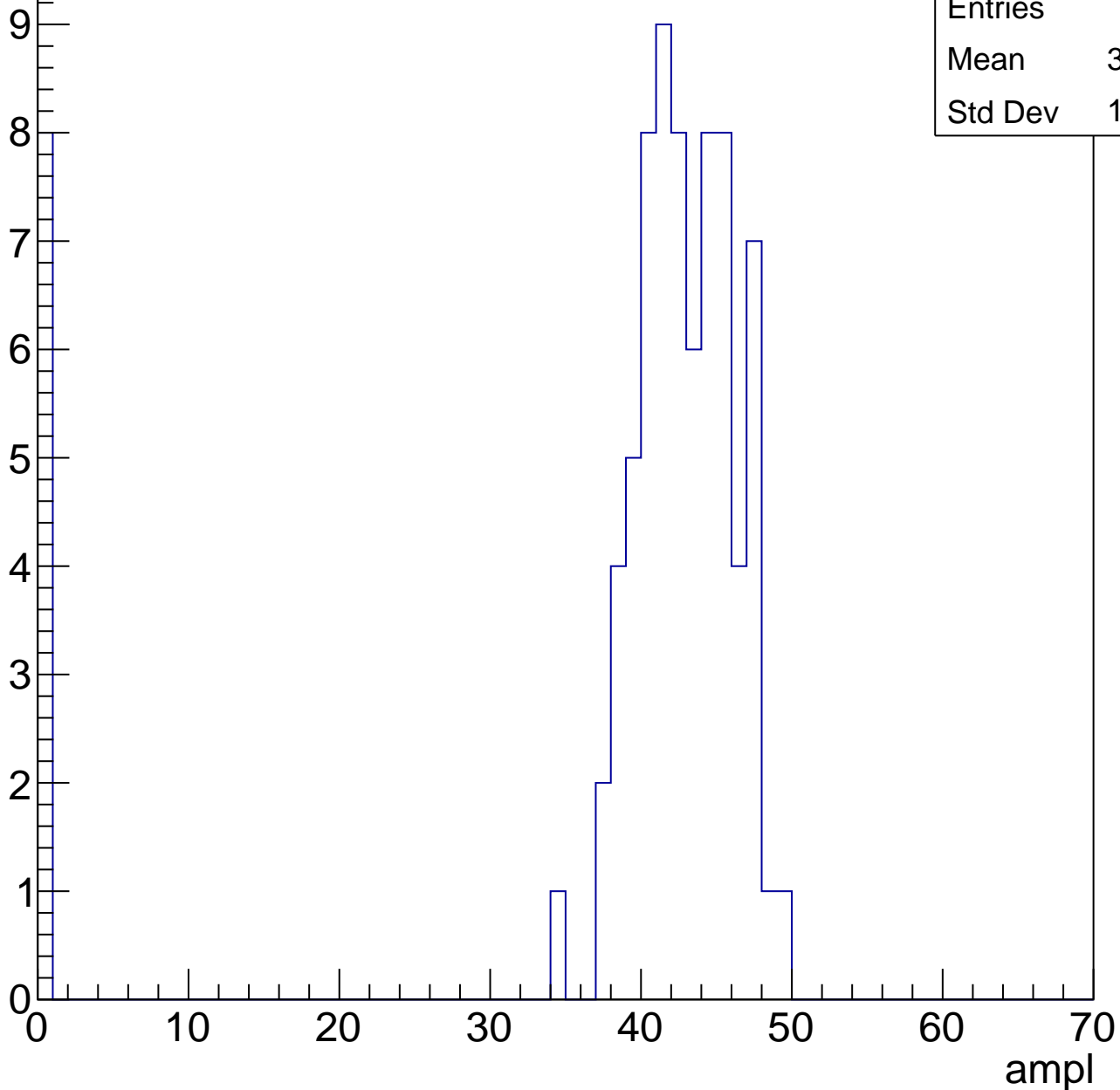


B1L103S, U23-ch101, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

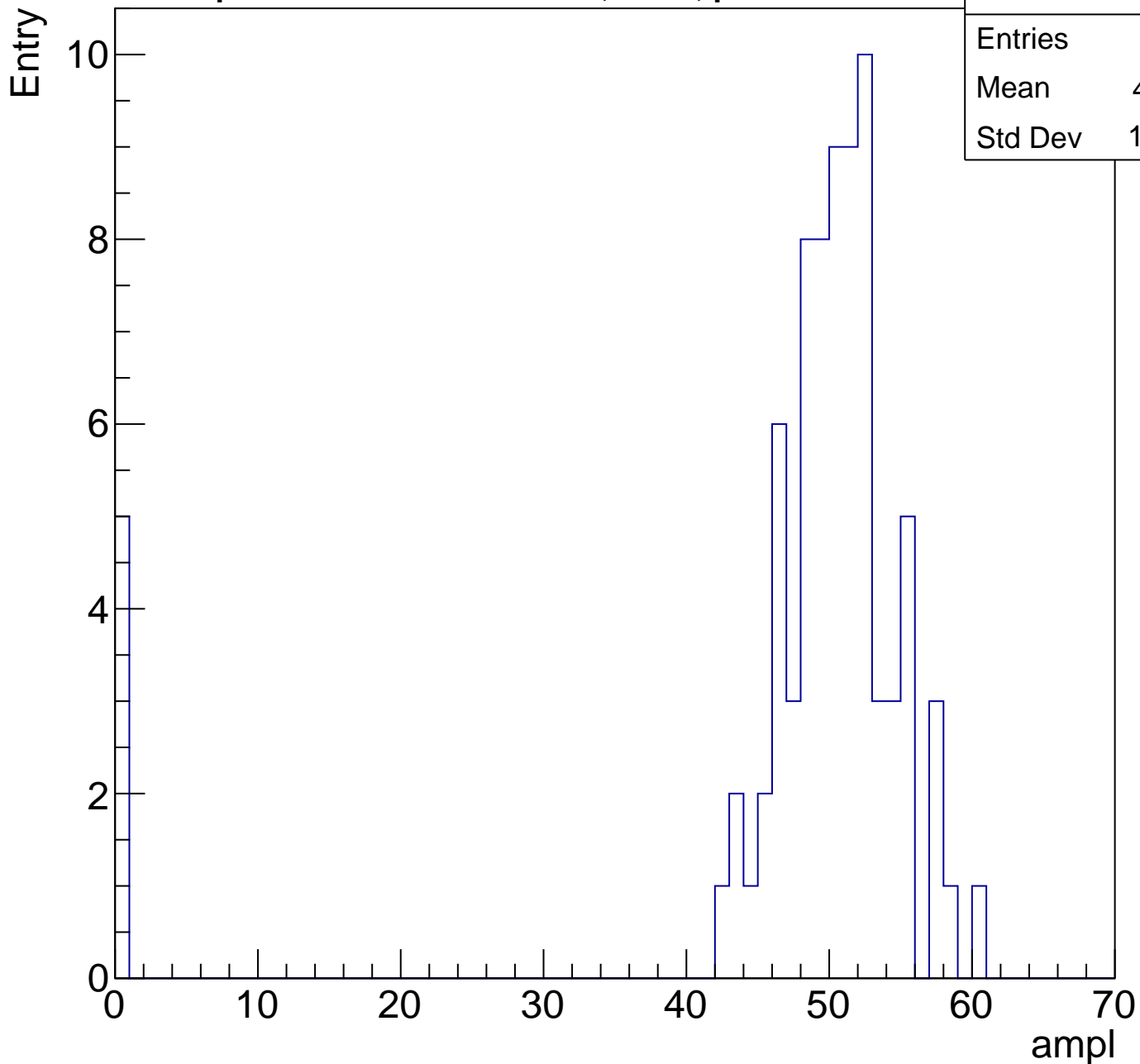
Entries	80
Mean	38.25
Std Dev	13.08



B1L103S, U23-ch101, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	80
Mean	47.11
Std Dev	12.65

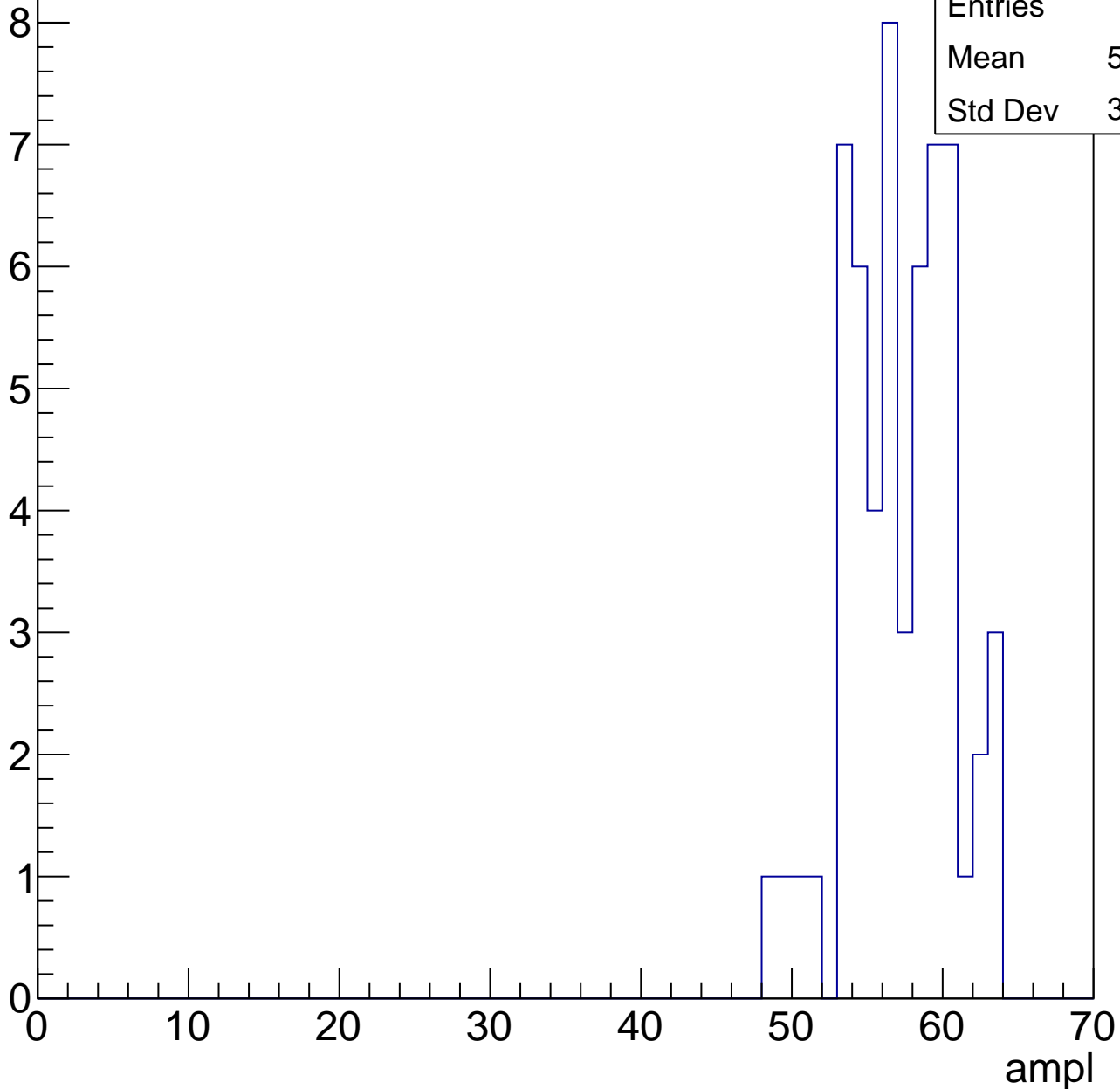


B1L103S, U23-ch101, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	56.67
Std Dev	3.436

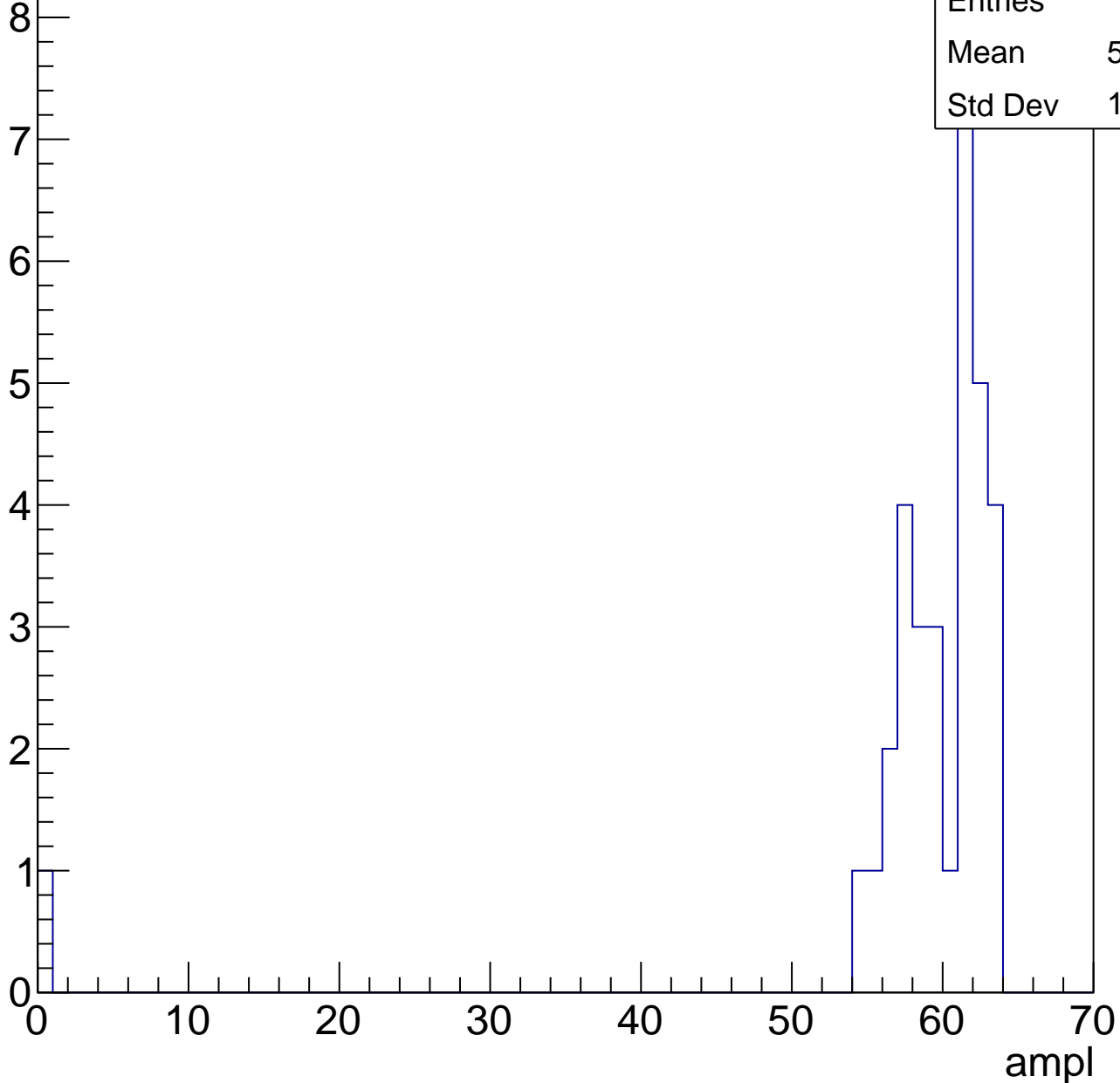


B1L103S, U23-ch101, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	33
Mean	57.88
Std Dev	10.53



B1L103S, U23-ch101, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries

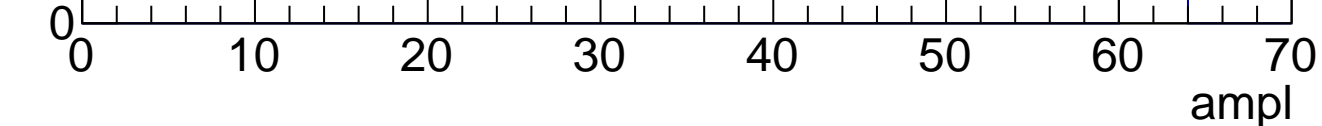
7

Mean

61.86

Std Dev

0.9897



B1L103S, U23-ch101, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.15
Std Dev	13.73

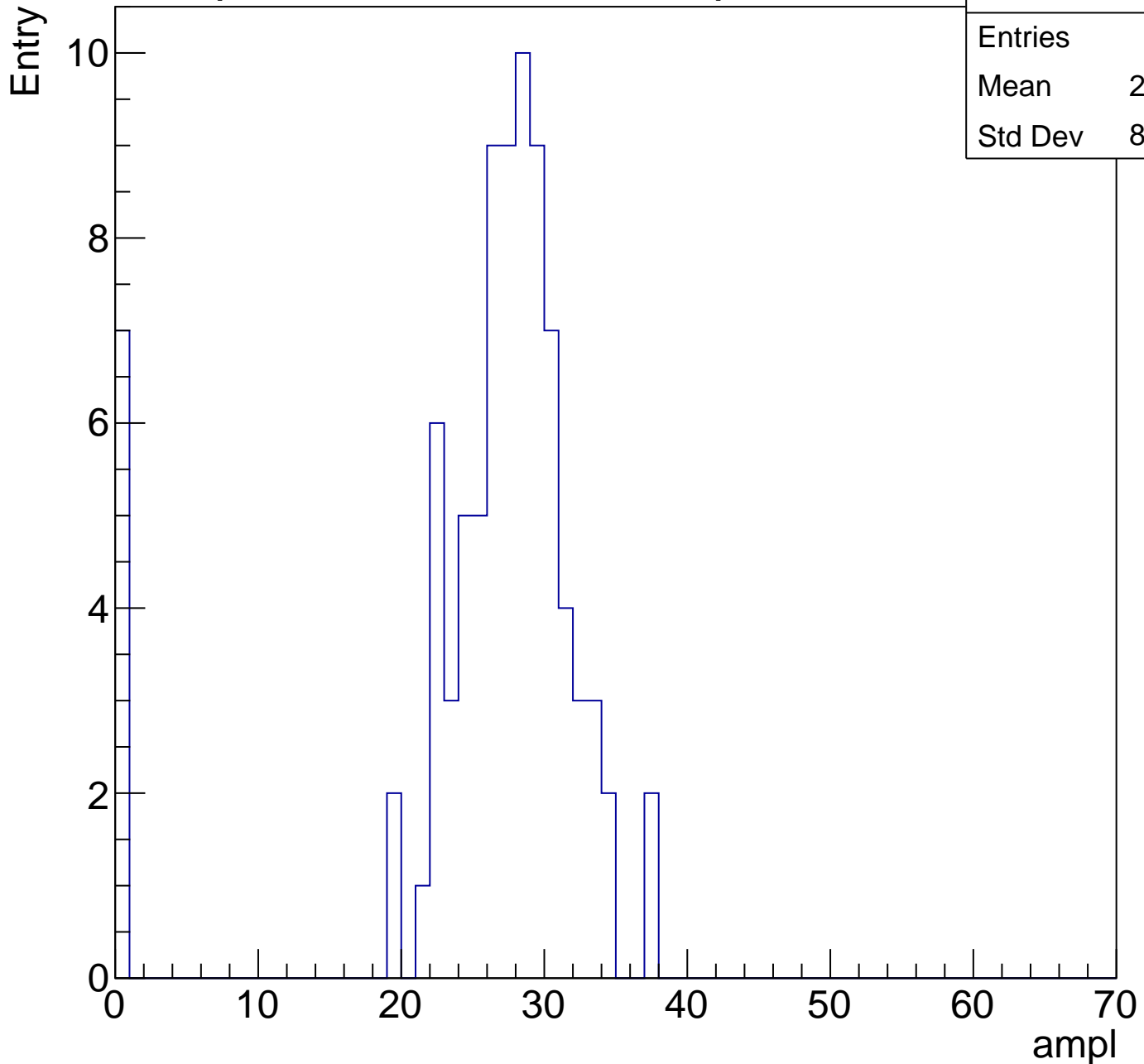
Entry



B1L103S, U23-ch102, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	87
Mean	25.22
Std Dev	8.247

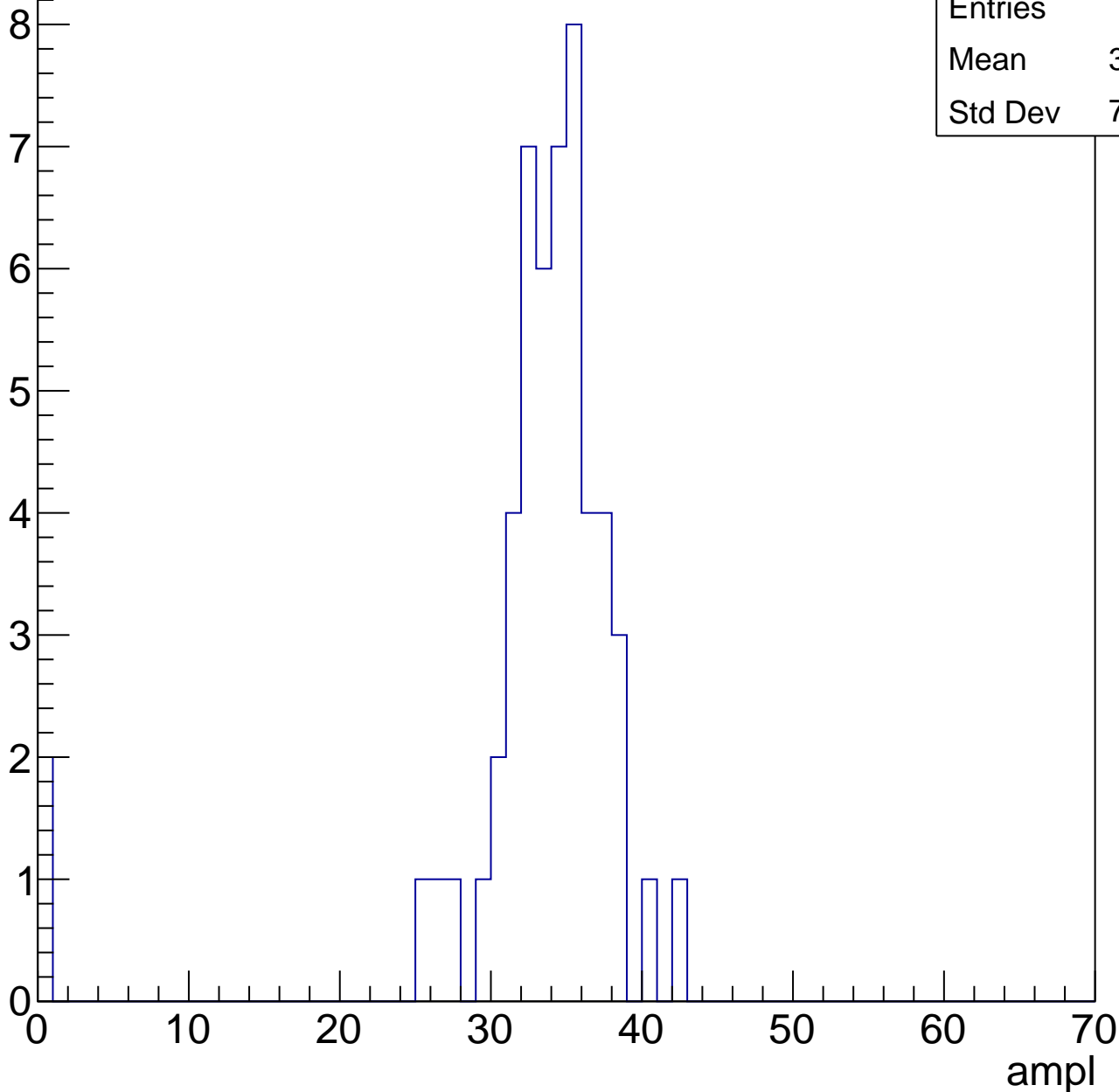


B1L103S, U23-ch102, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	53
Mean	32.43
Std Dev	7.152



B1L103S, U23-ch102, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	78
Mean	34.19
Std Dev	14.31

Entry

10

8

6

4

2

0

0

10

20

30

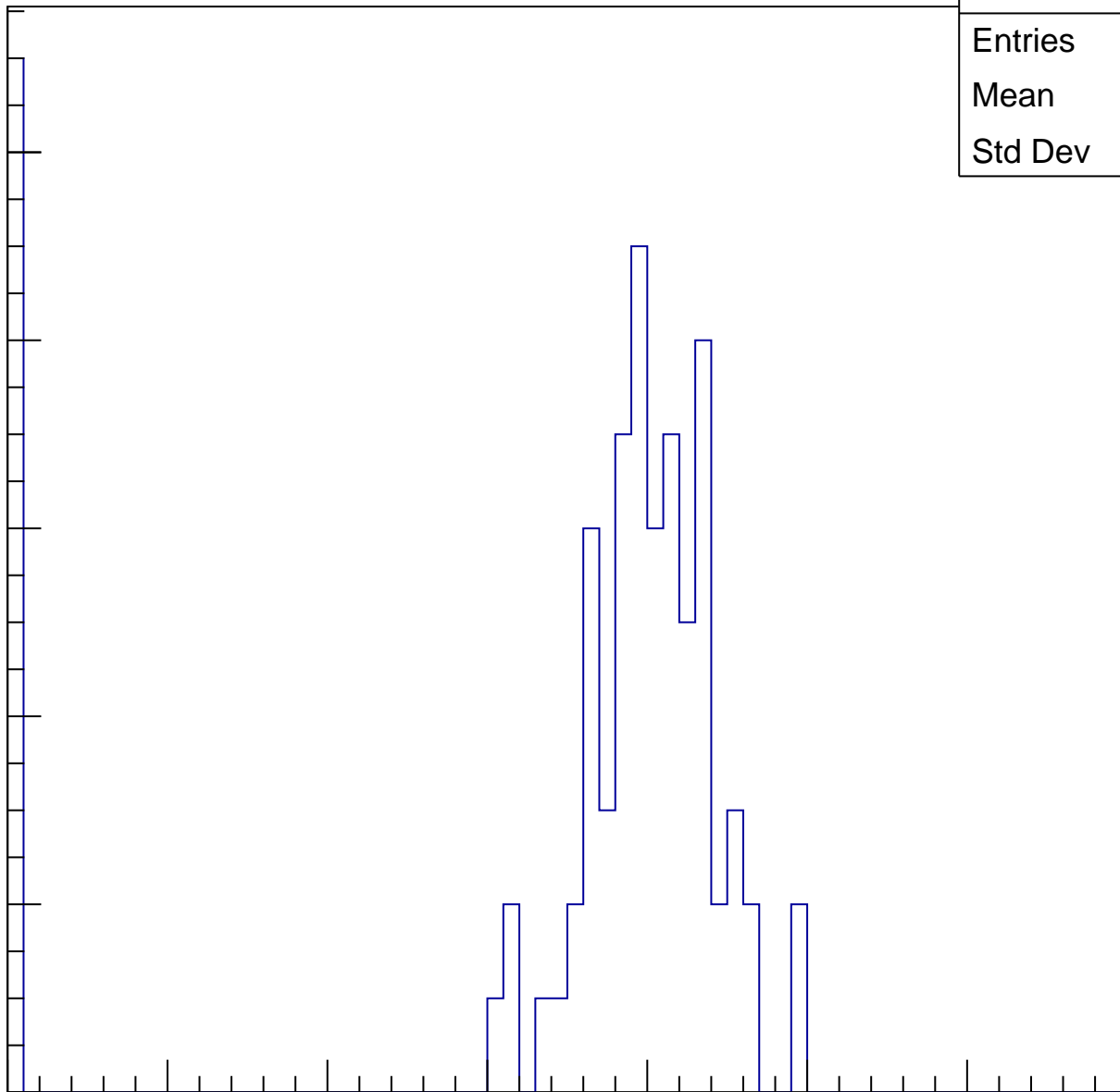
40

50

60

70

ampl

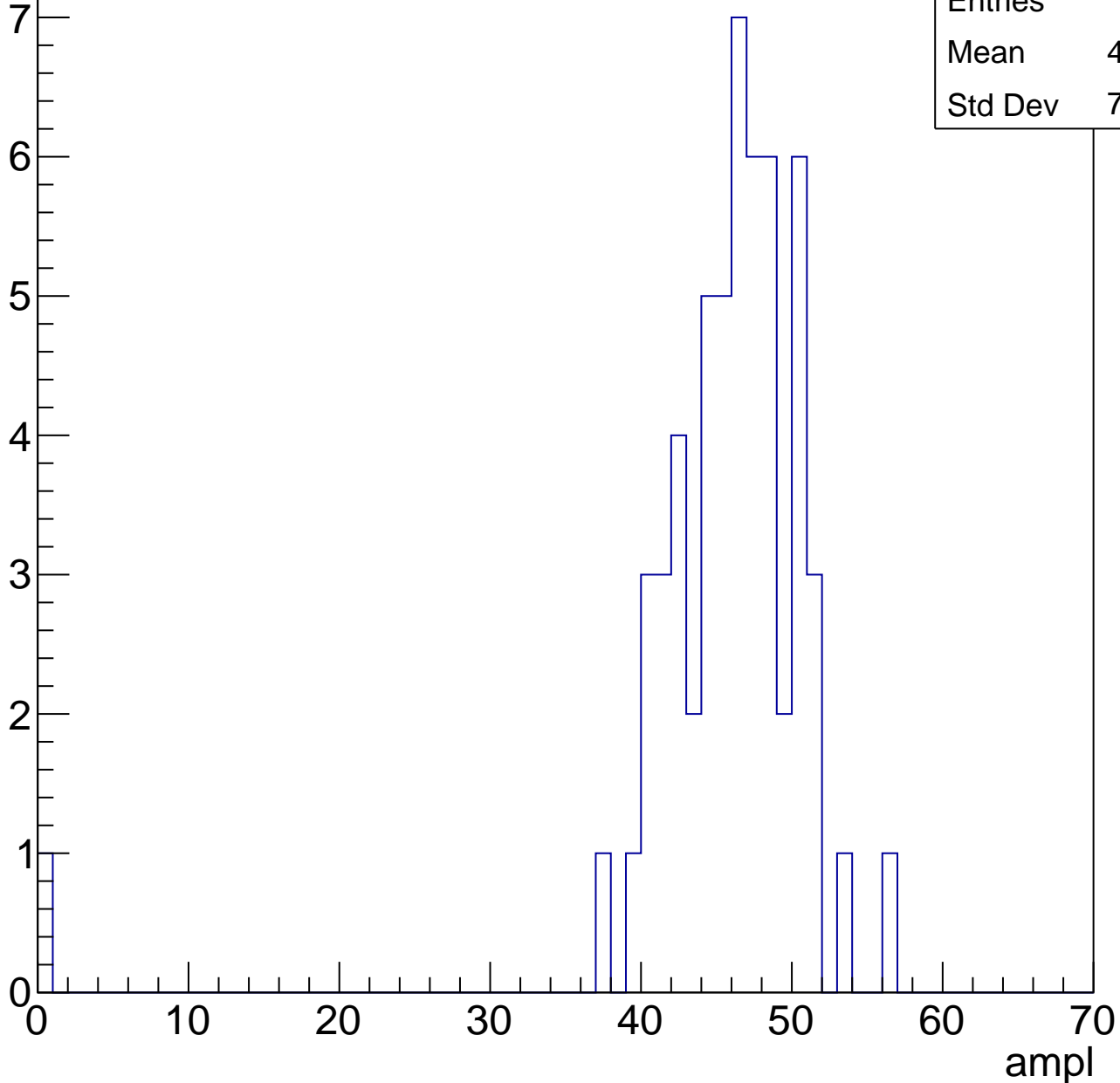


B1L103S, U23-ch102, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	57
Mean	45.09
Std Dev	7.079

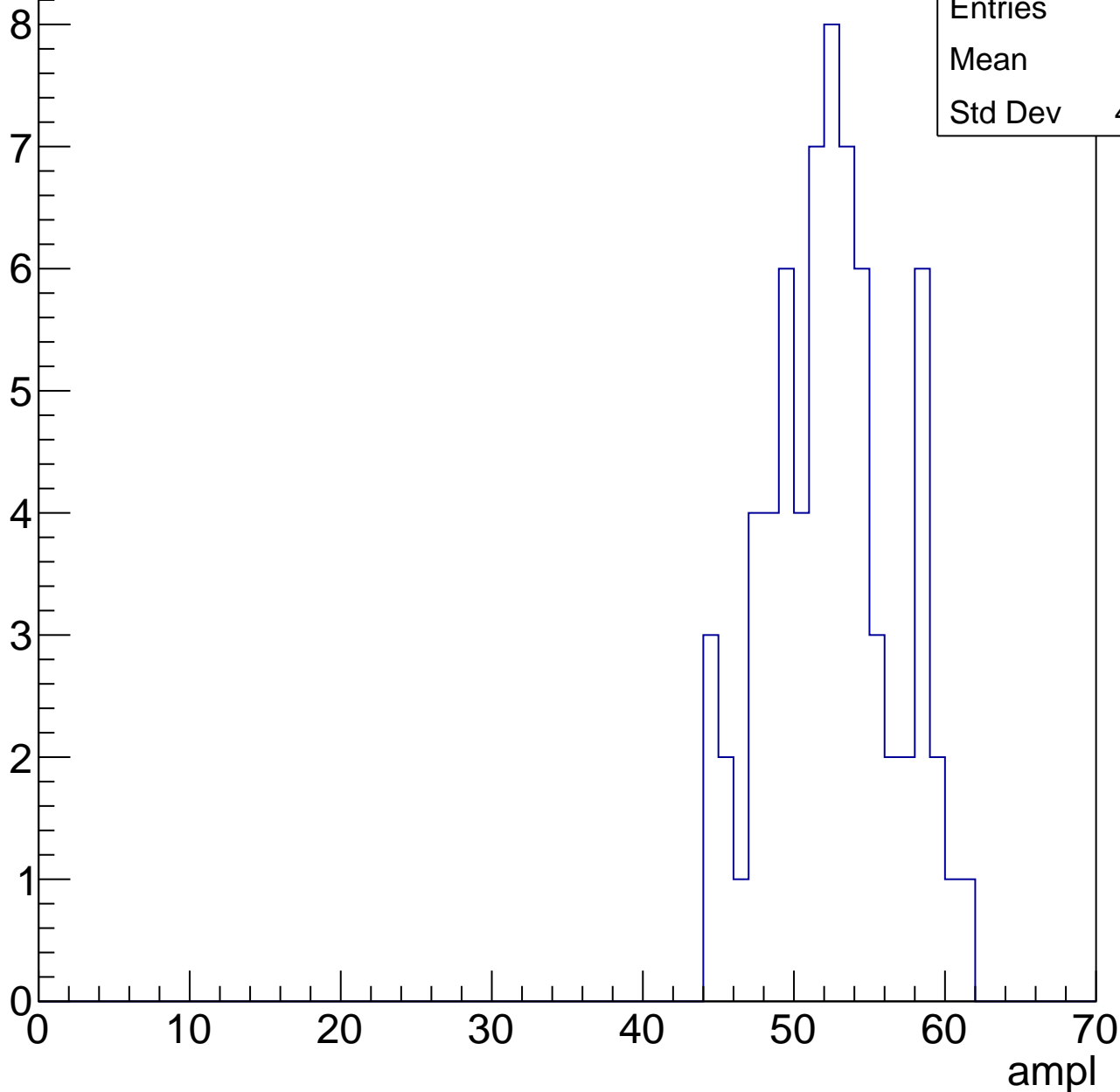


B1L103S, U23-ch102, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

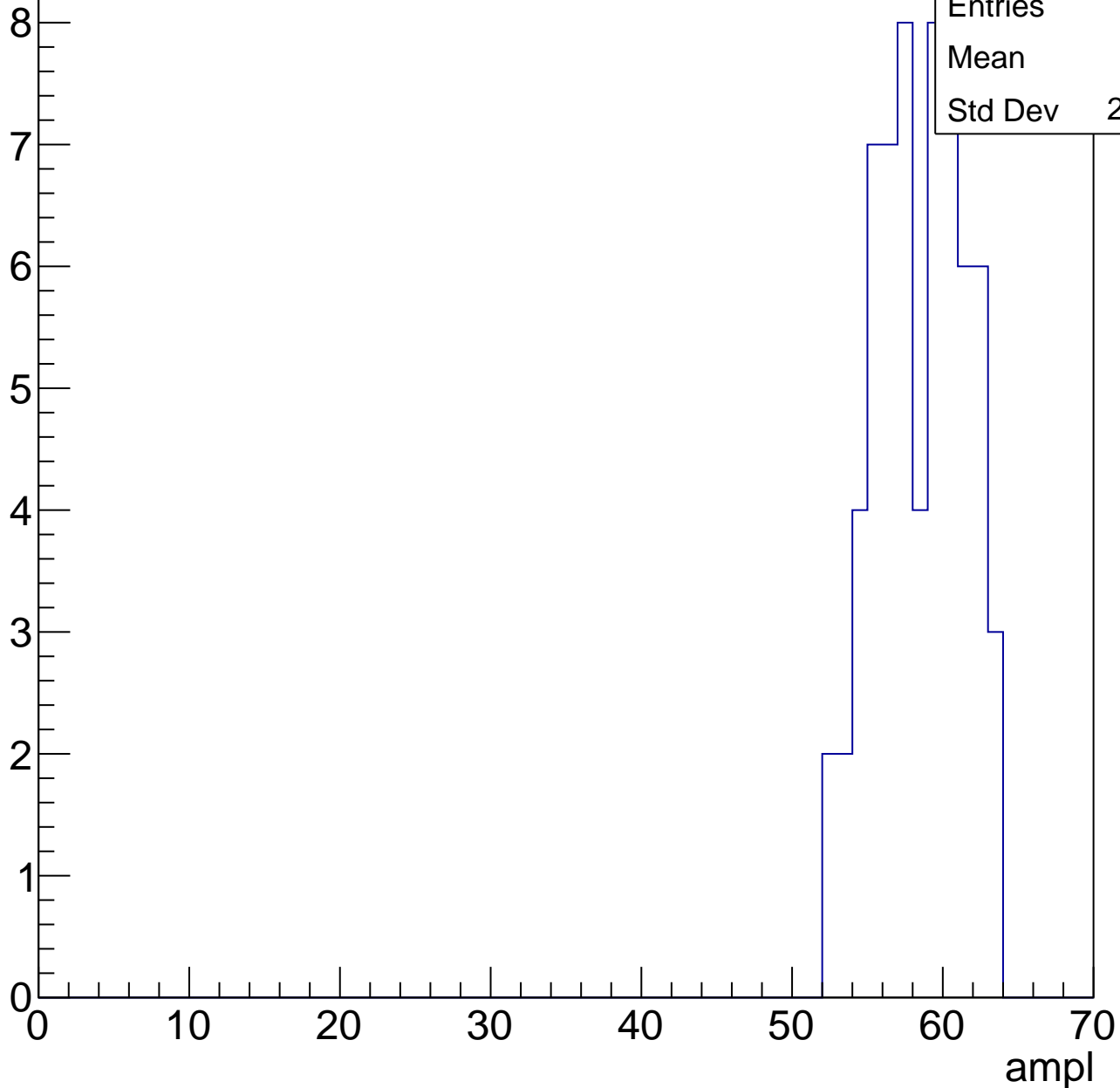
Entries	69
Mean	52
Std Dev	4.111



B1L103S, U23-ch102, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

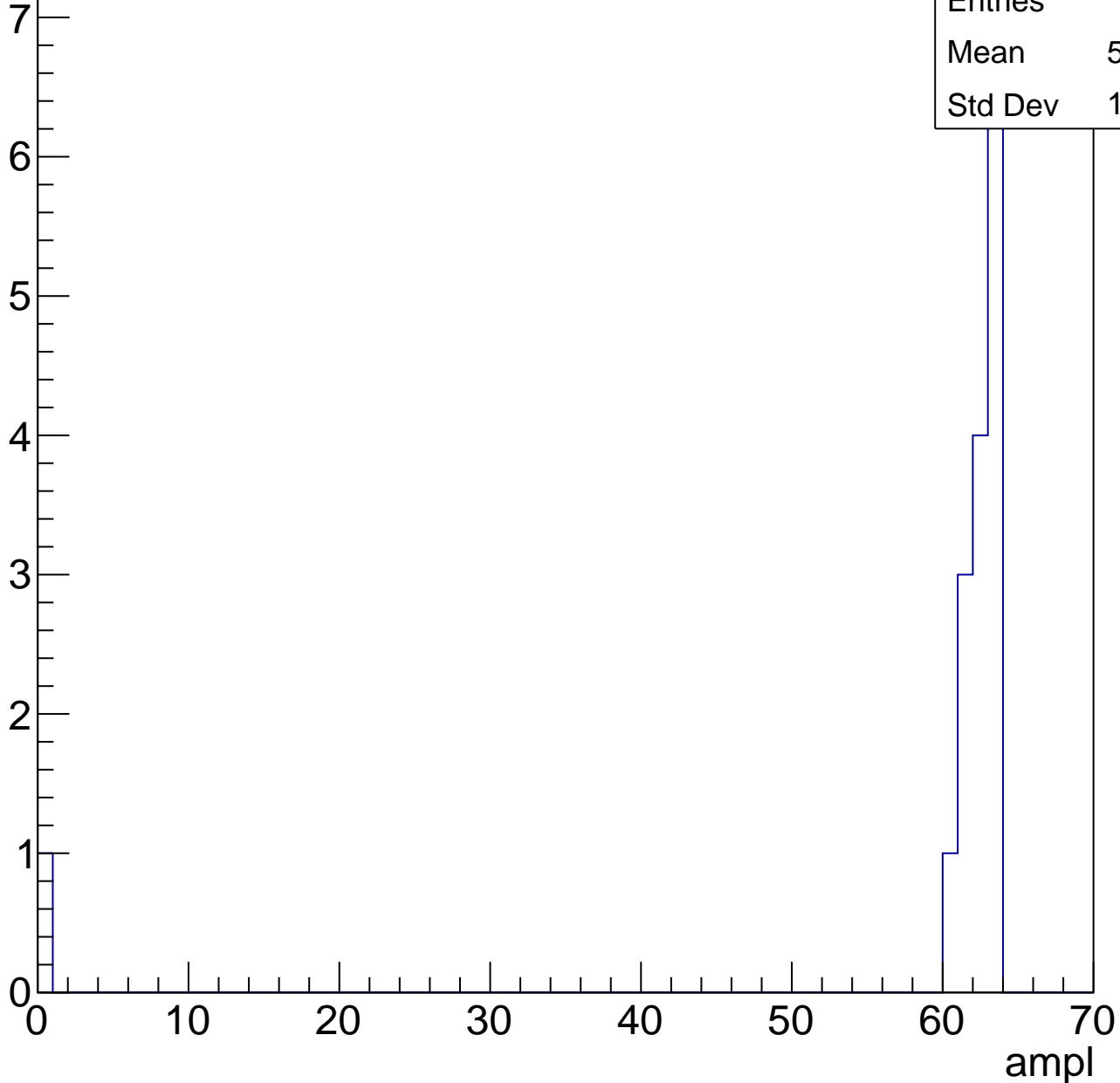


B1L103S, U23-ch102, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	16
Mean	58.25
Std Dev	15.07



B1L103S, U23-ch102, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

ampl

B1L103S, U23-ch103, adc0

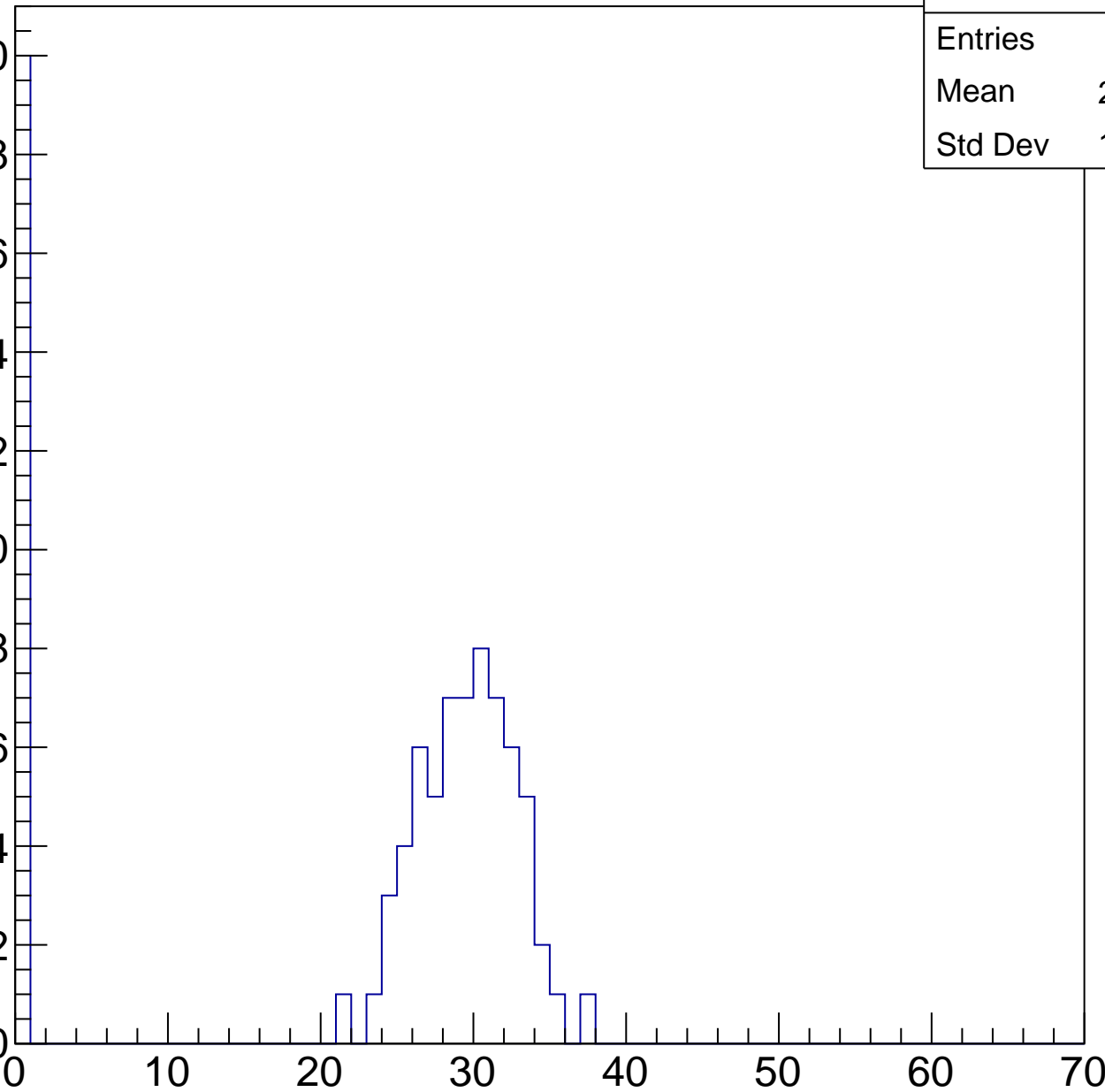
calib_packv5_041523_1651.root, FC#0, port C2

Entry

20
18
16
14
12
10
8
6
4
2
0

Entries	84
Mean	22.14
Std Dev	12.68

ampl

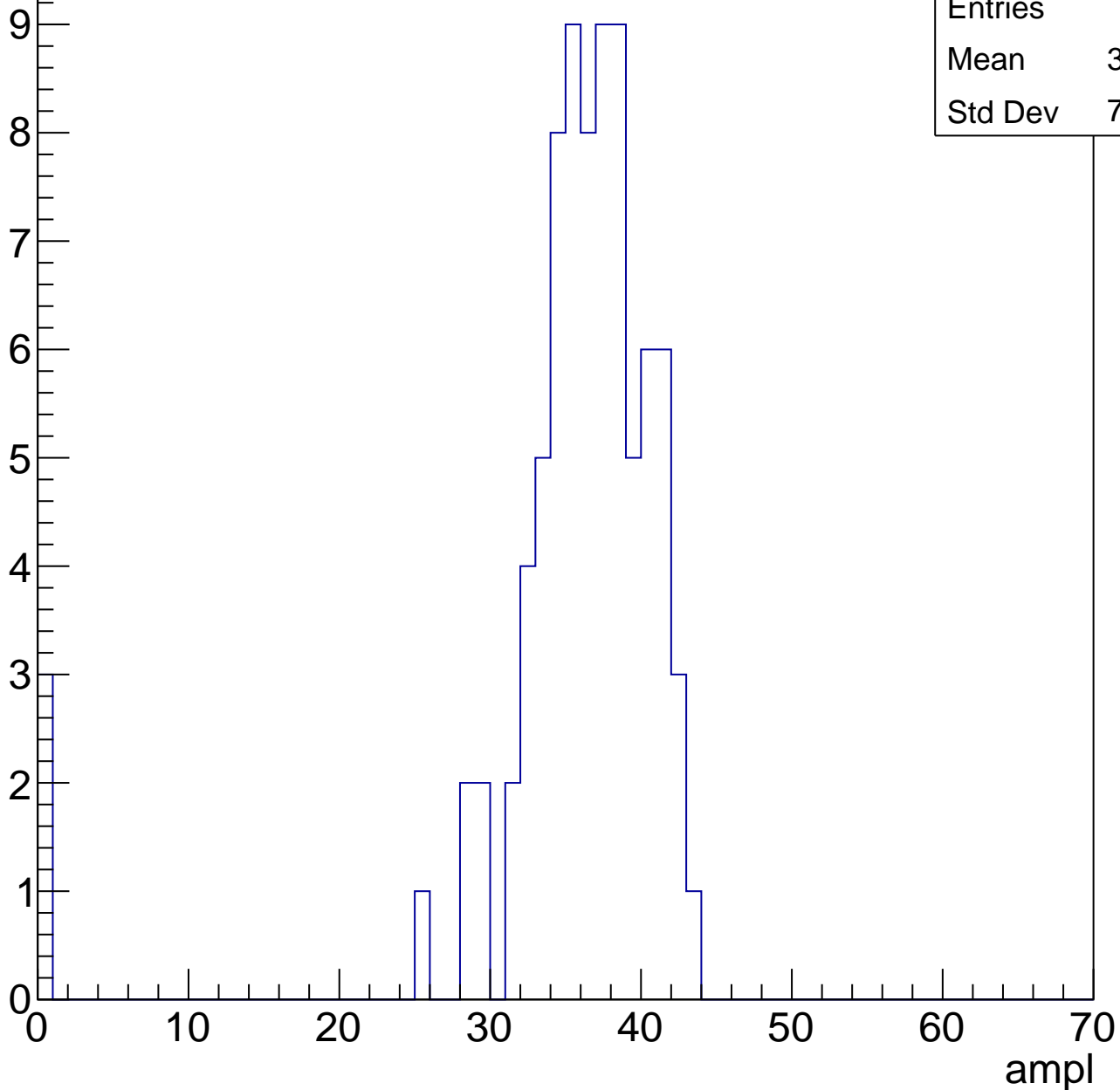


B1L103S, U23-ch103, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

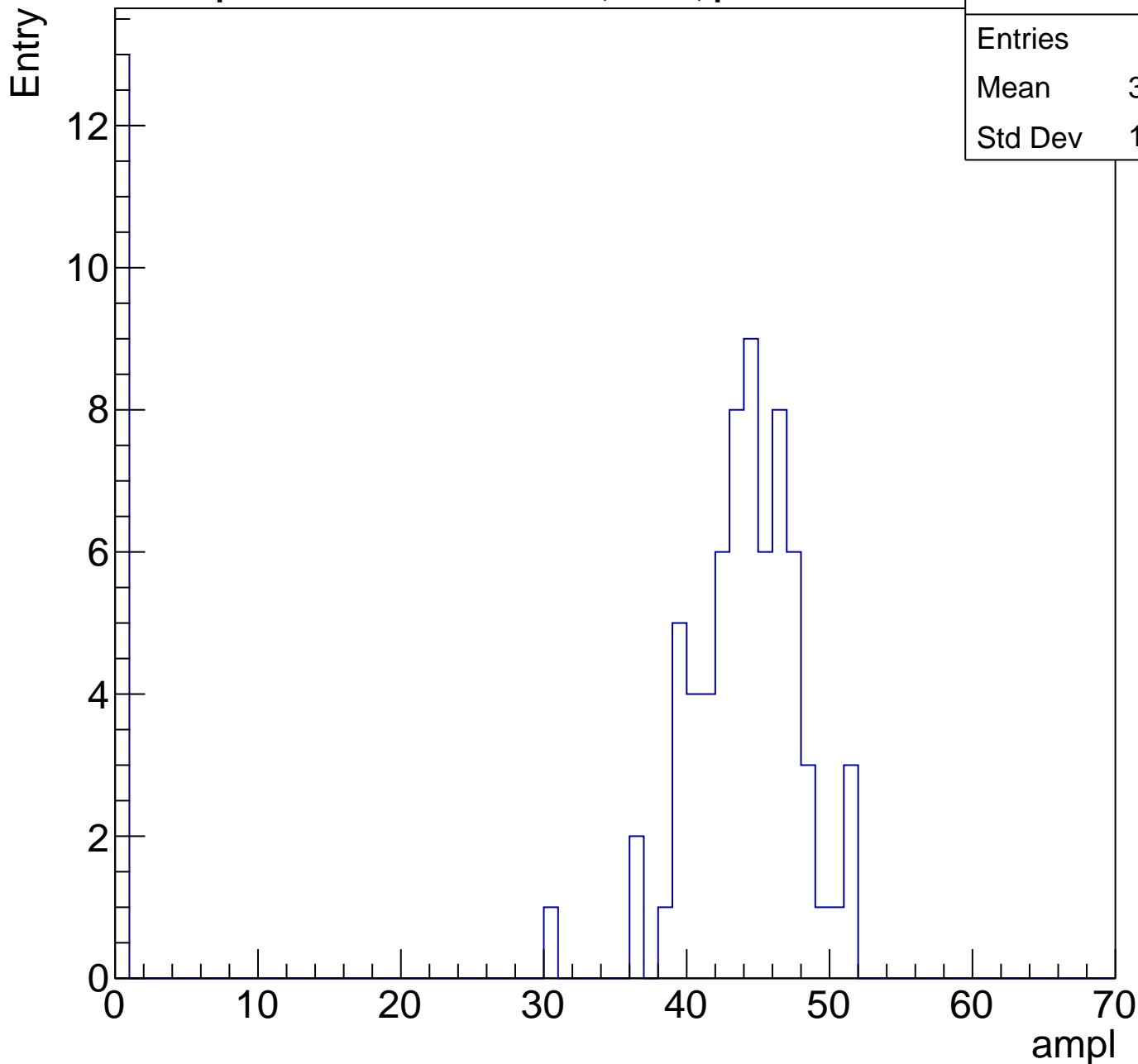
Entries	83
Mean	34.87
Std Dev	7.622



B1L103S, U23-ch103, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	81
Mean	36.63
Std Dev	16.38

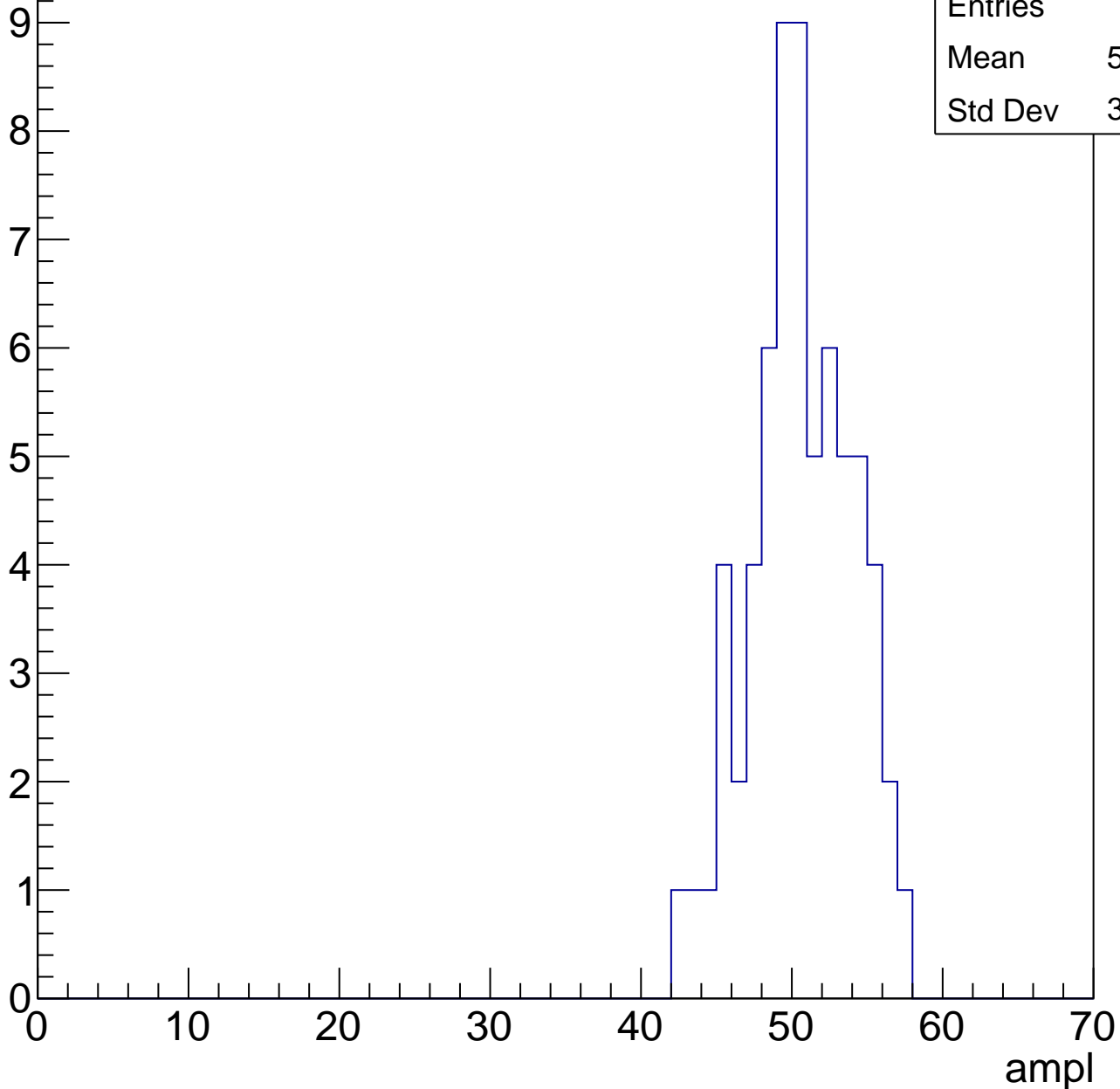


B1L103S, U23-ch103, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	50.14
Std Dev	3.337

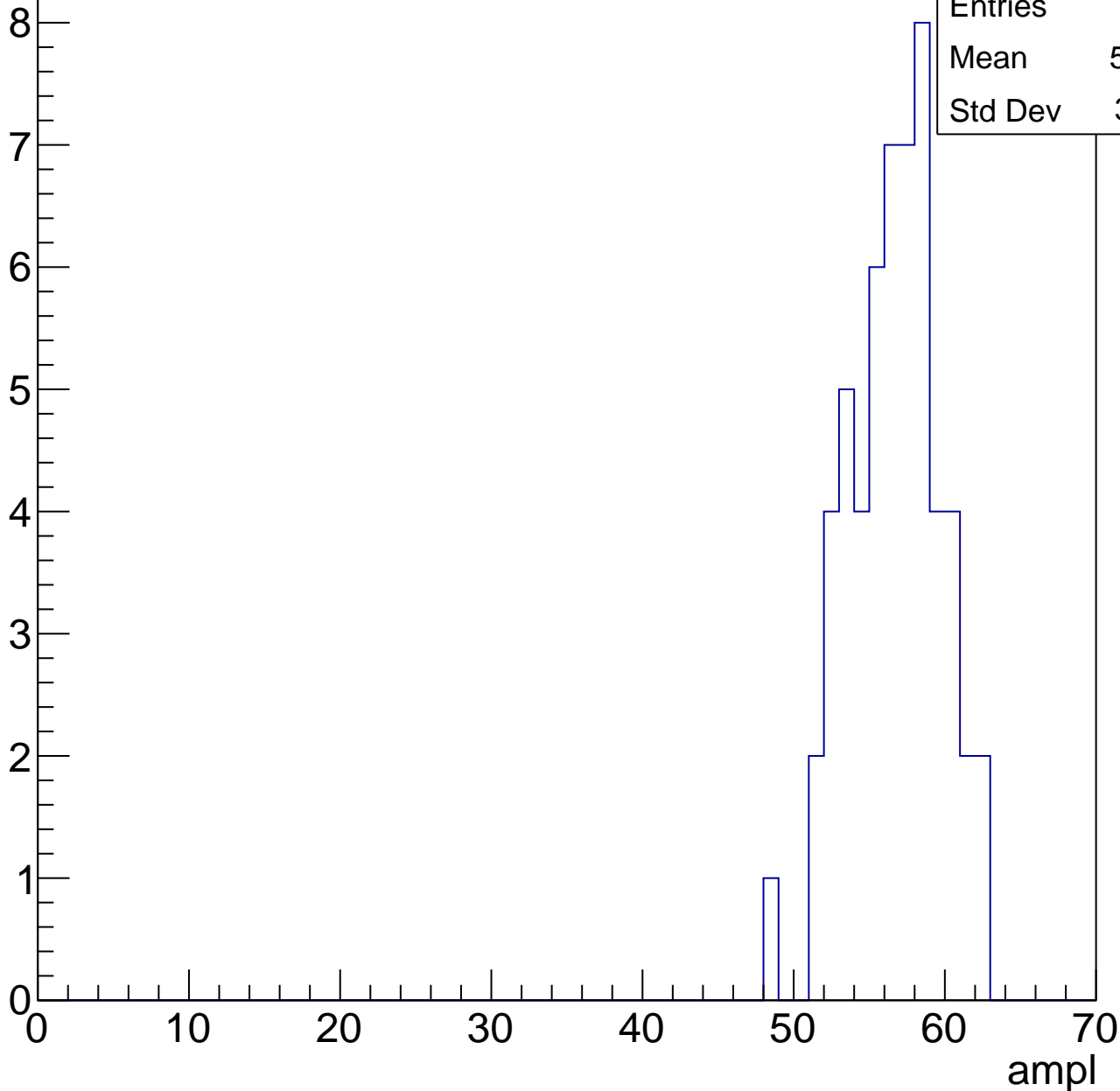


B1L103S, U23-ch103, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	56
Mean	56.18
Std Dev	3.001

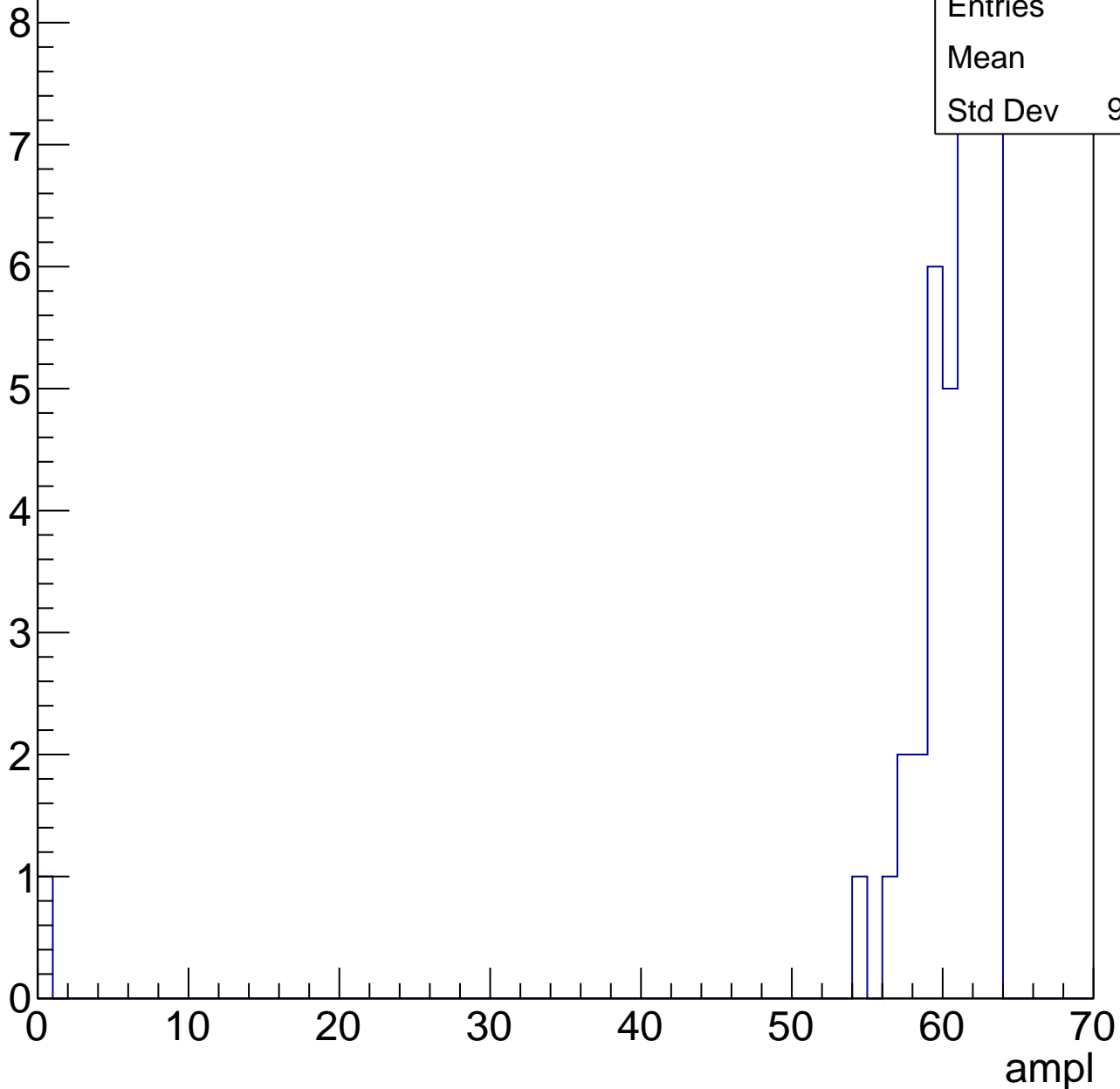


B1L103S, U23-ch103, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	42
Mean	59.1
Std Dev	9.464



B1L103S, U23-ch103, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch103, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

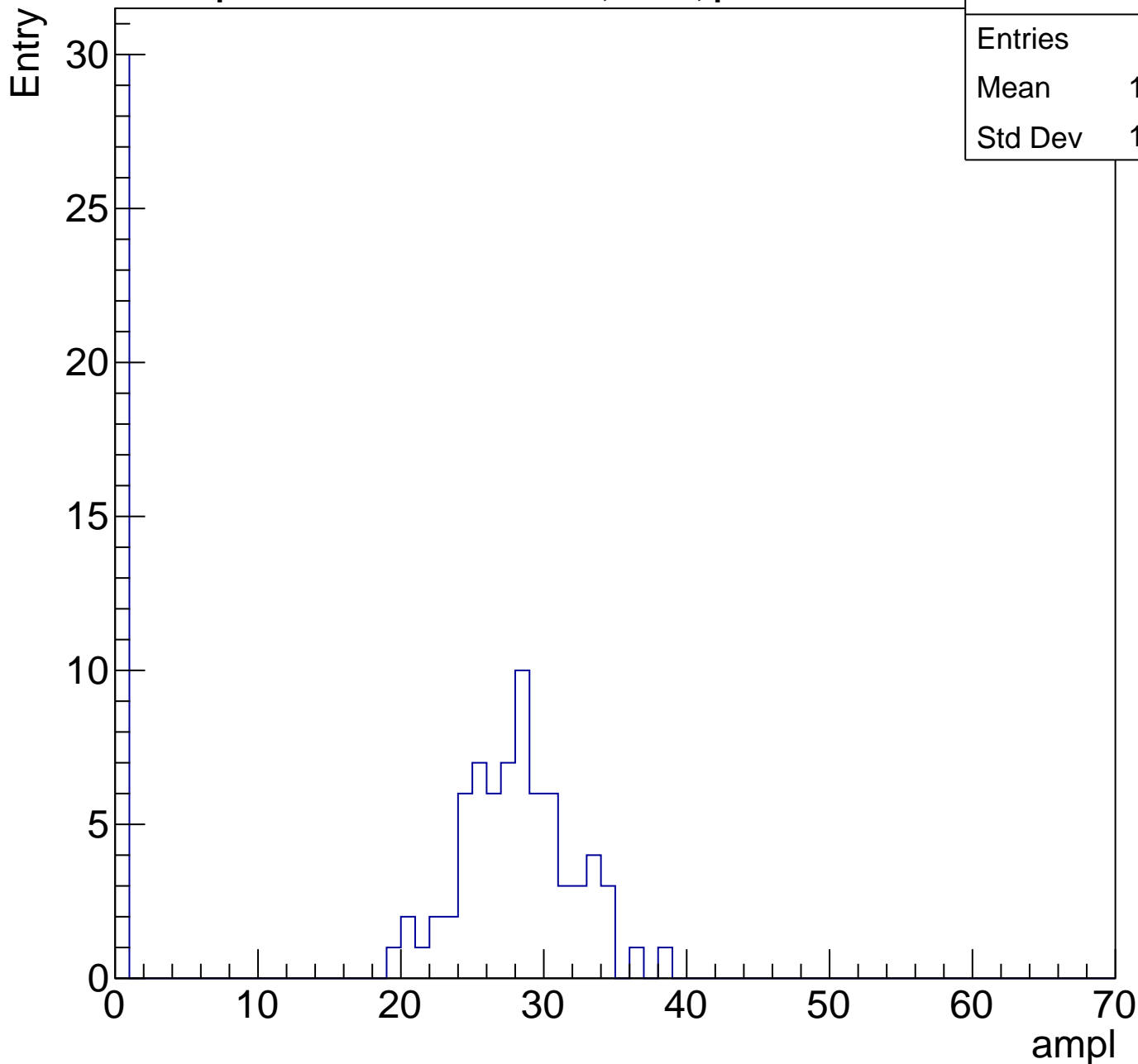
Entries	18
Mean	0
Std Dev	0

ampl

B1L103S, U23-ch104, adc0

calib_packv5_041523_1651.root, FC#0, port C2

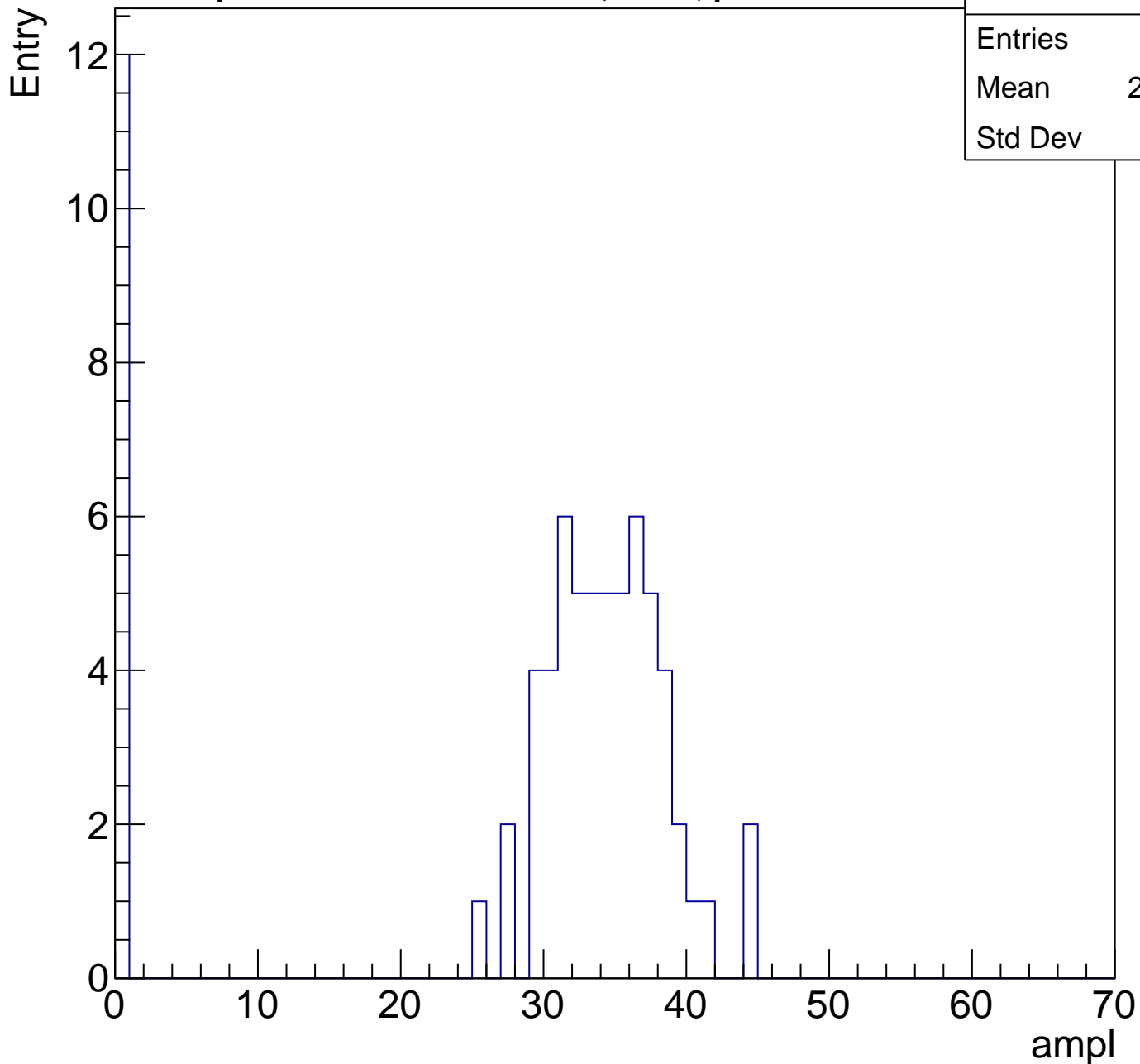
Entries	101
Mean	19.46
Std Dev	13.05



B1L103S, U23-ch104, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	70
Mean	28.16
Std Dev	13.3

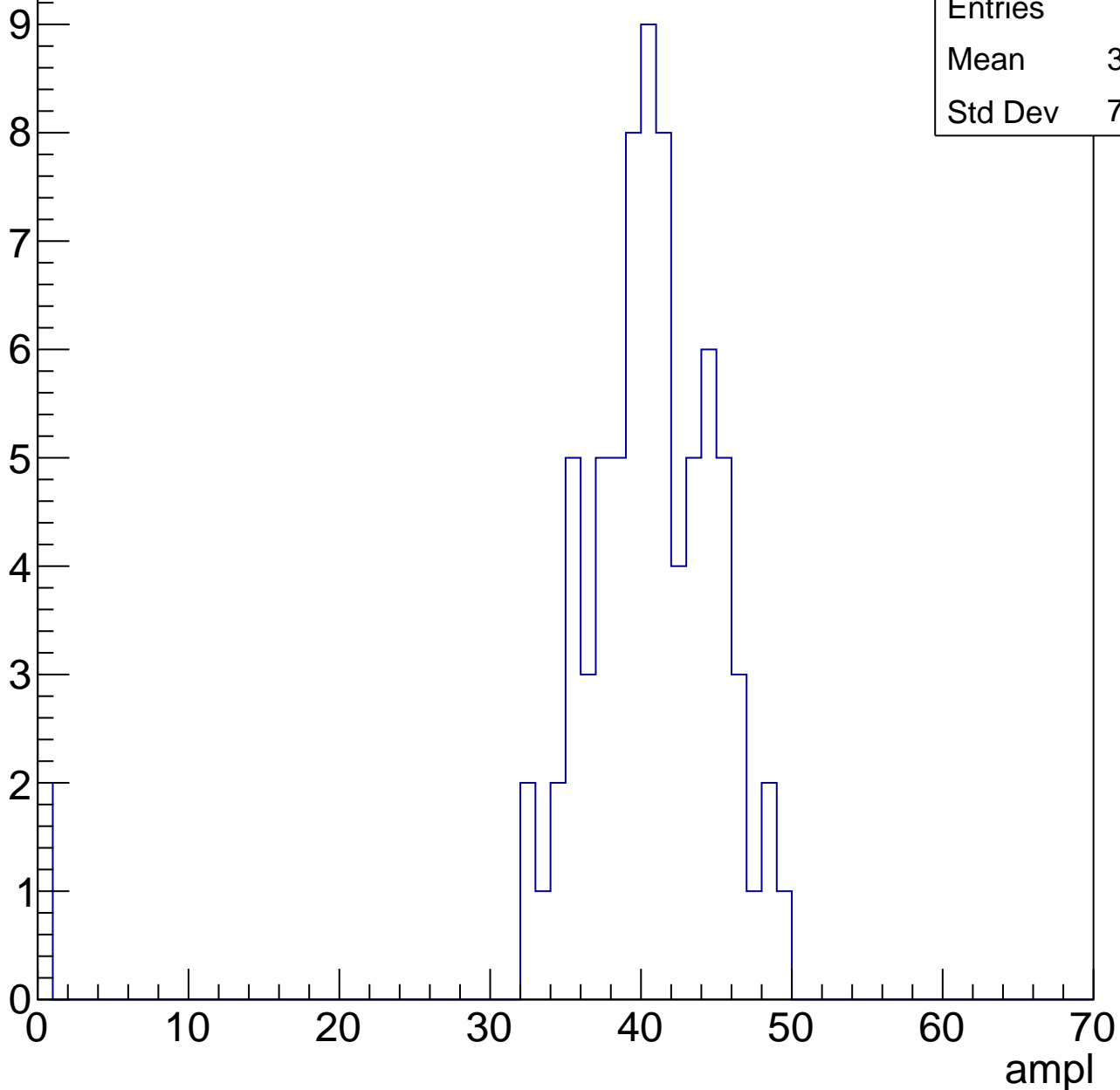


B1L103S, U23-ch104, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	77
Mean	39.29
Std Dev	7.483

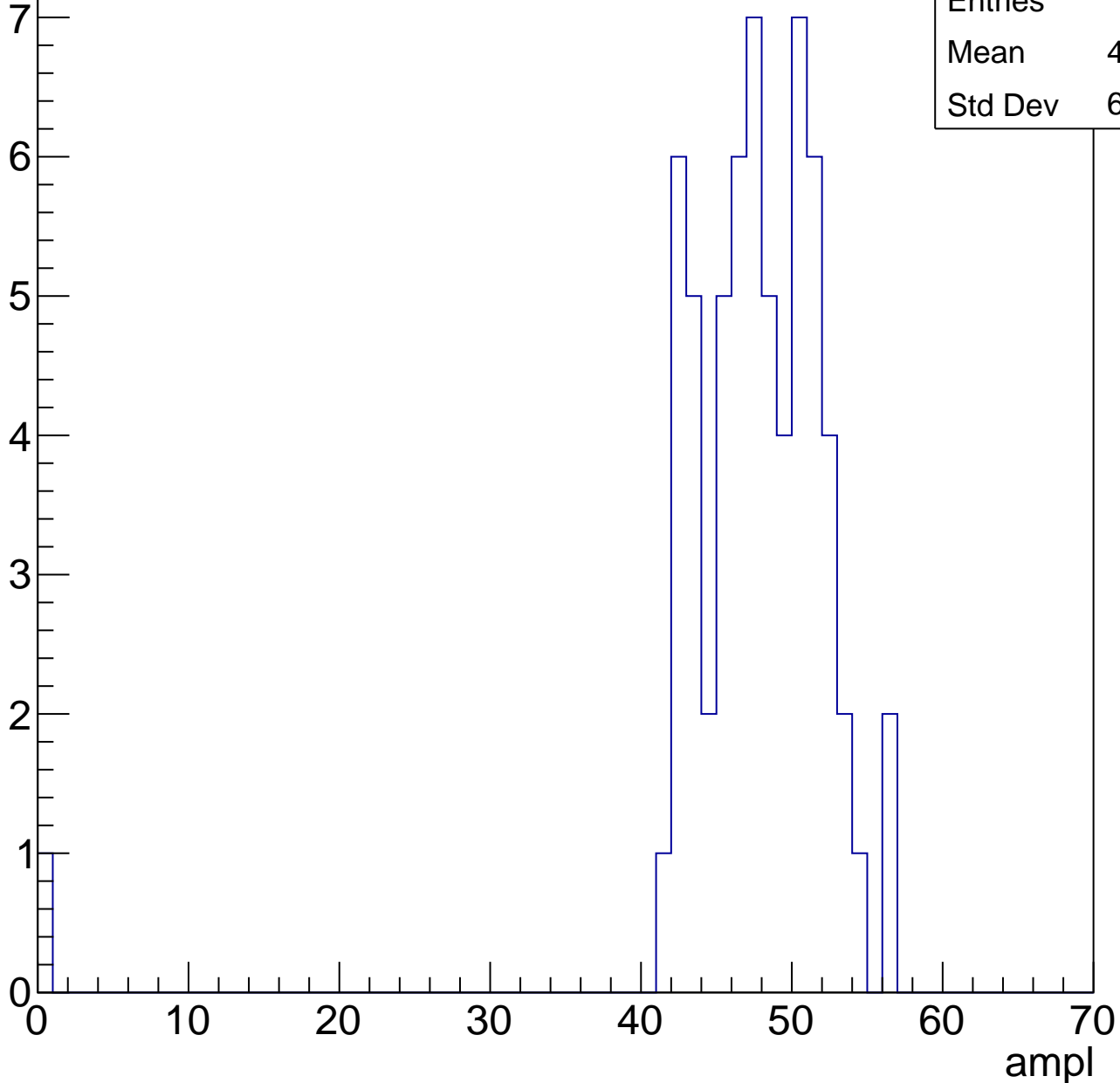


B1L103S, U23-ch104, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	46.84
Std Dev	6.938

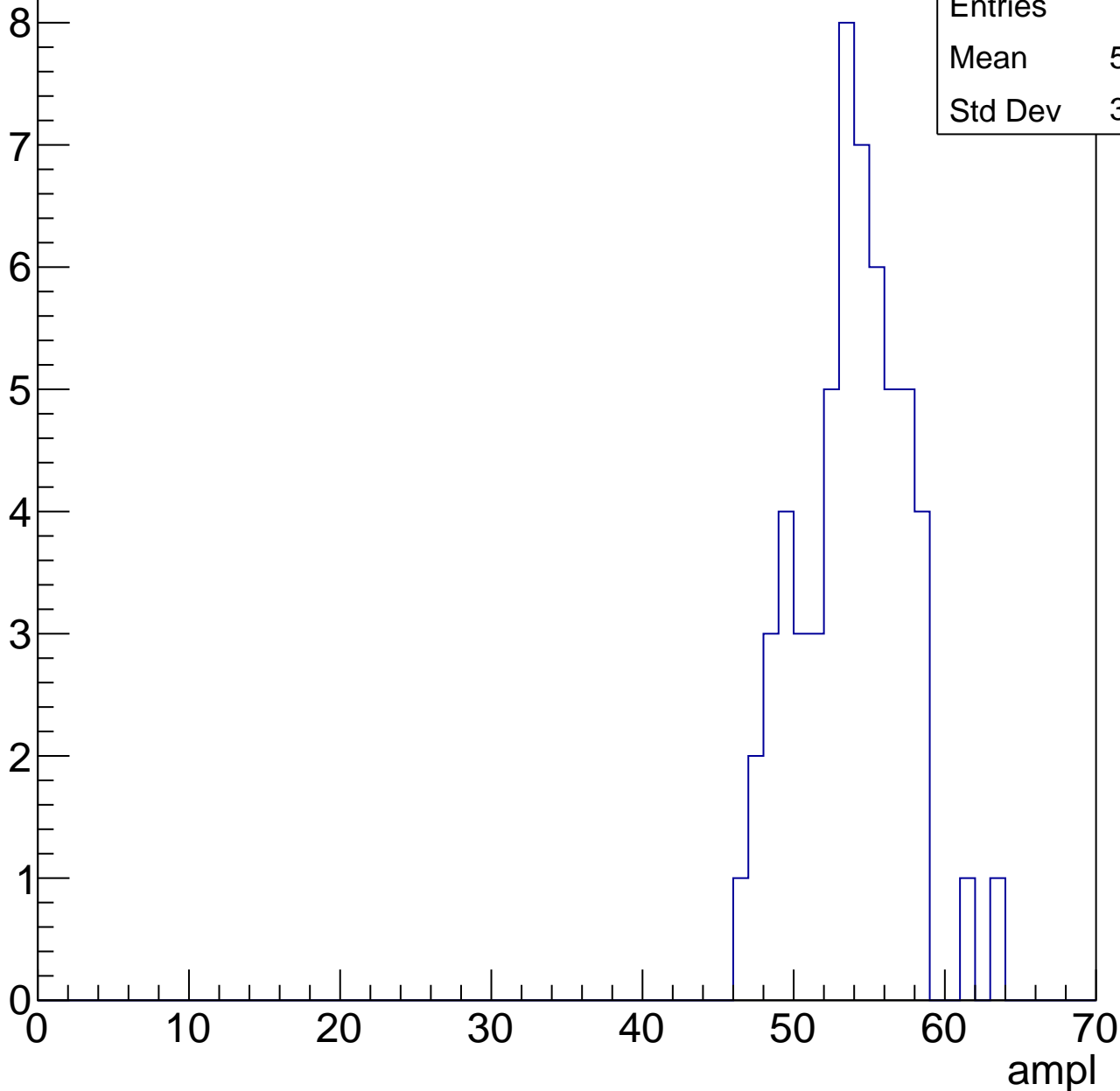


B1L103S, U23-ch104, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	53.38
Std Dev	3.513

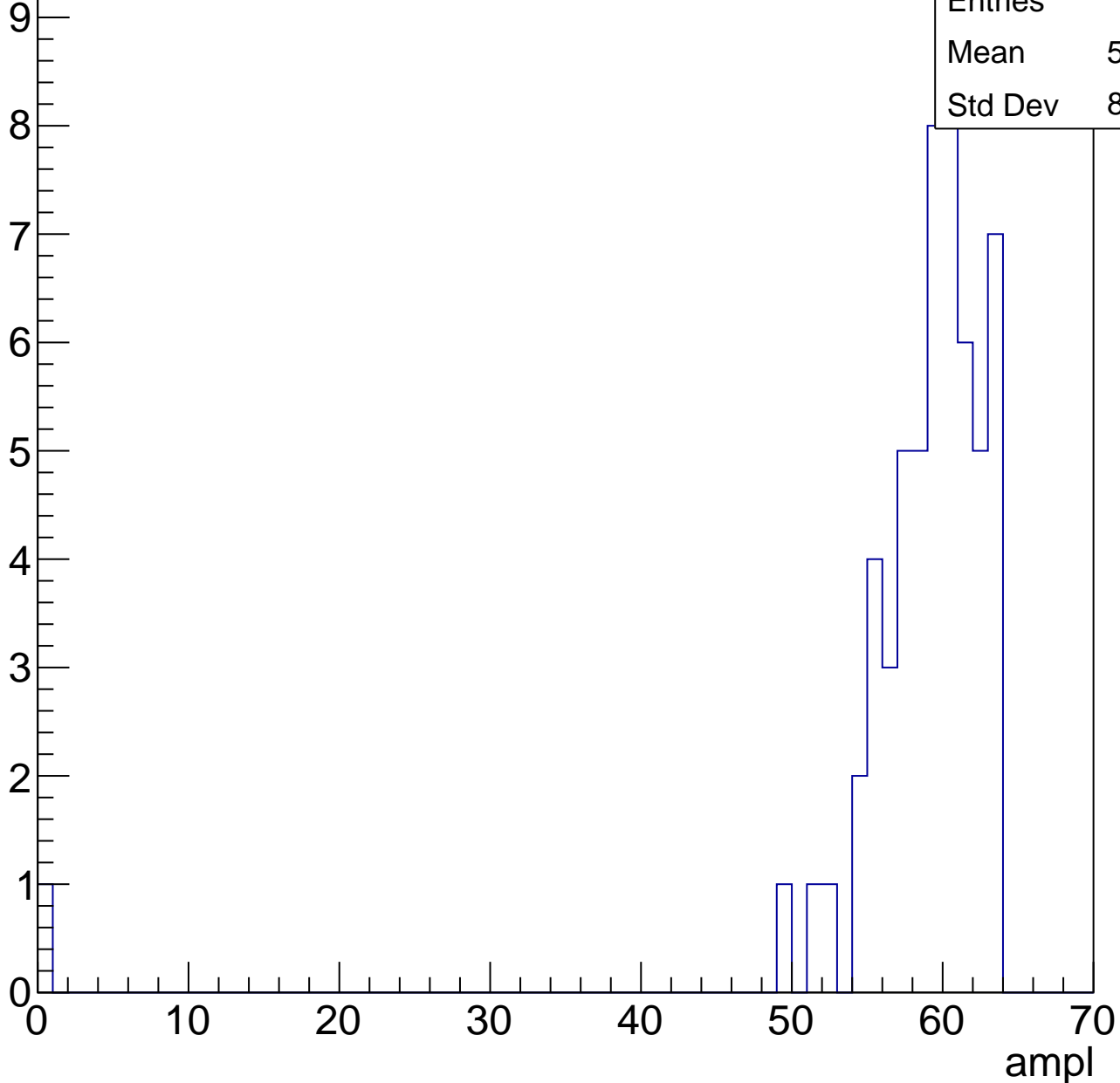


B1L103S, U23-ch104, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	57.79
Std Dev	8.269



B1L103S, U23-ch104, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries

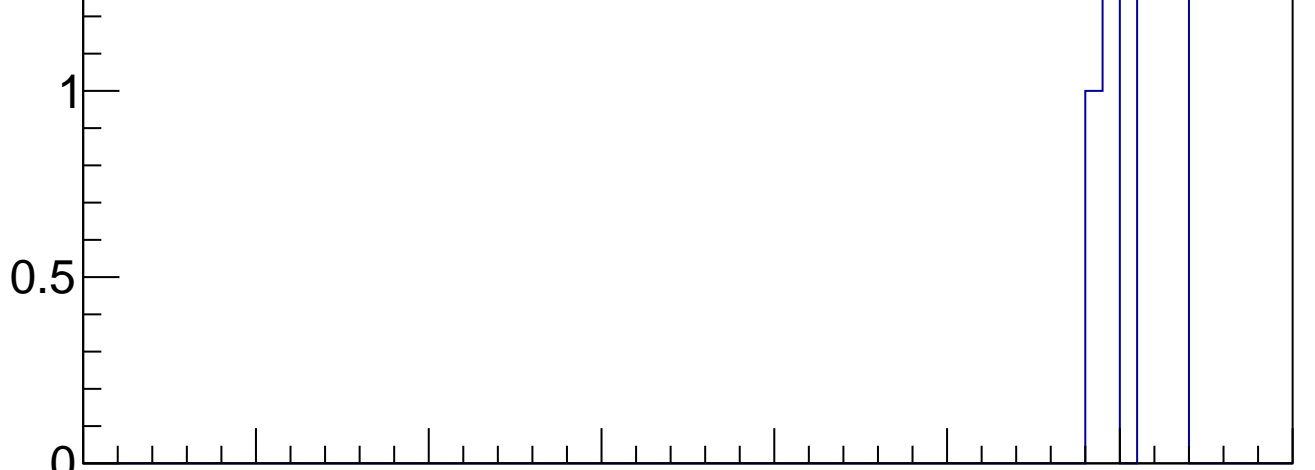
11

Mean

61

Std Dev

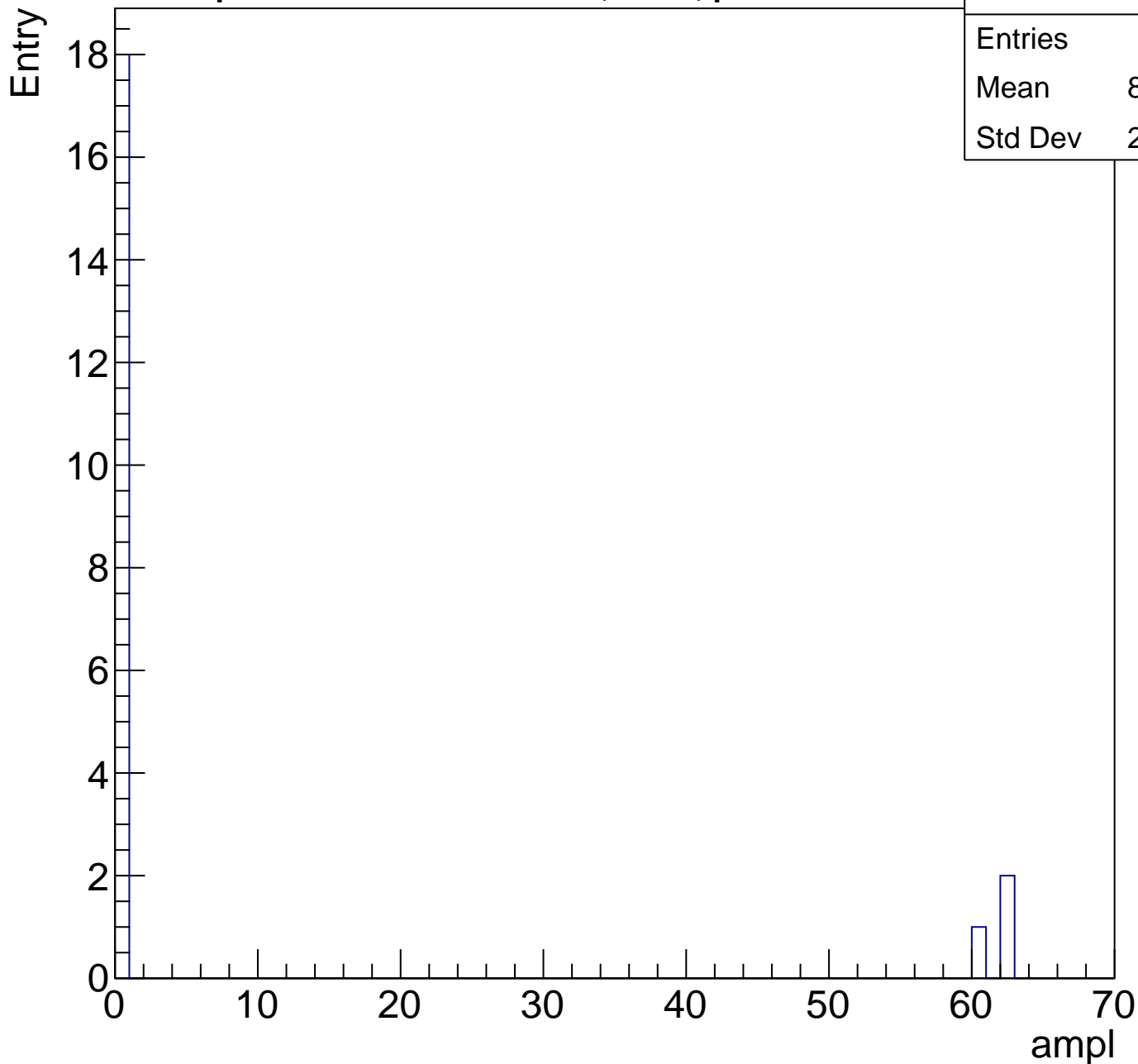
1.595



B1L103S, U23-ch104, adc7

calib_packv5_041523_1651.root, FC#0, port C2

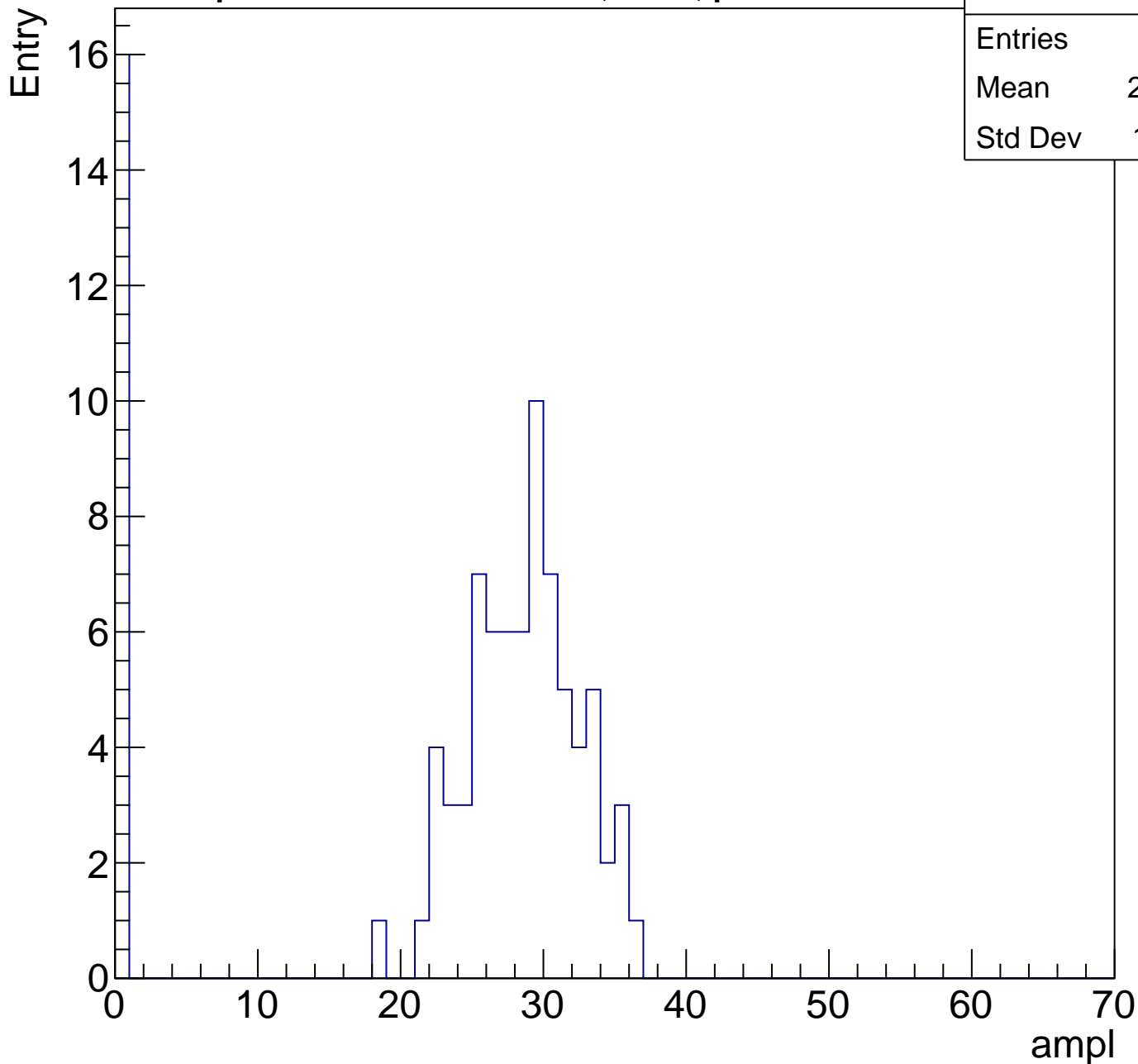
Entries	21
Mean	8.762
Std Dev	21.47



B1L103S, U23-ch105, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	90
Mean	23.18
Std Dev	11.31

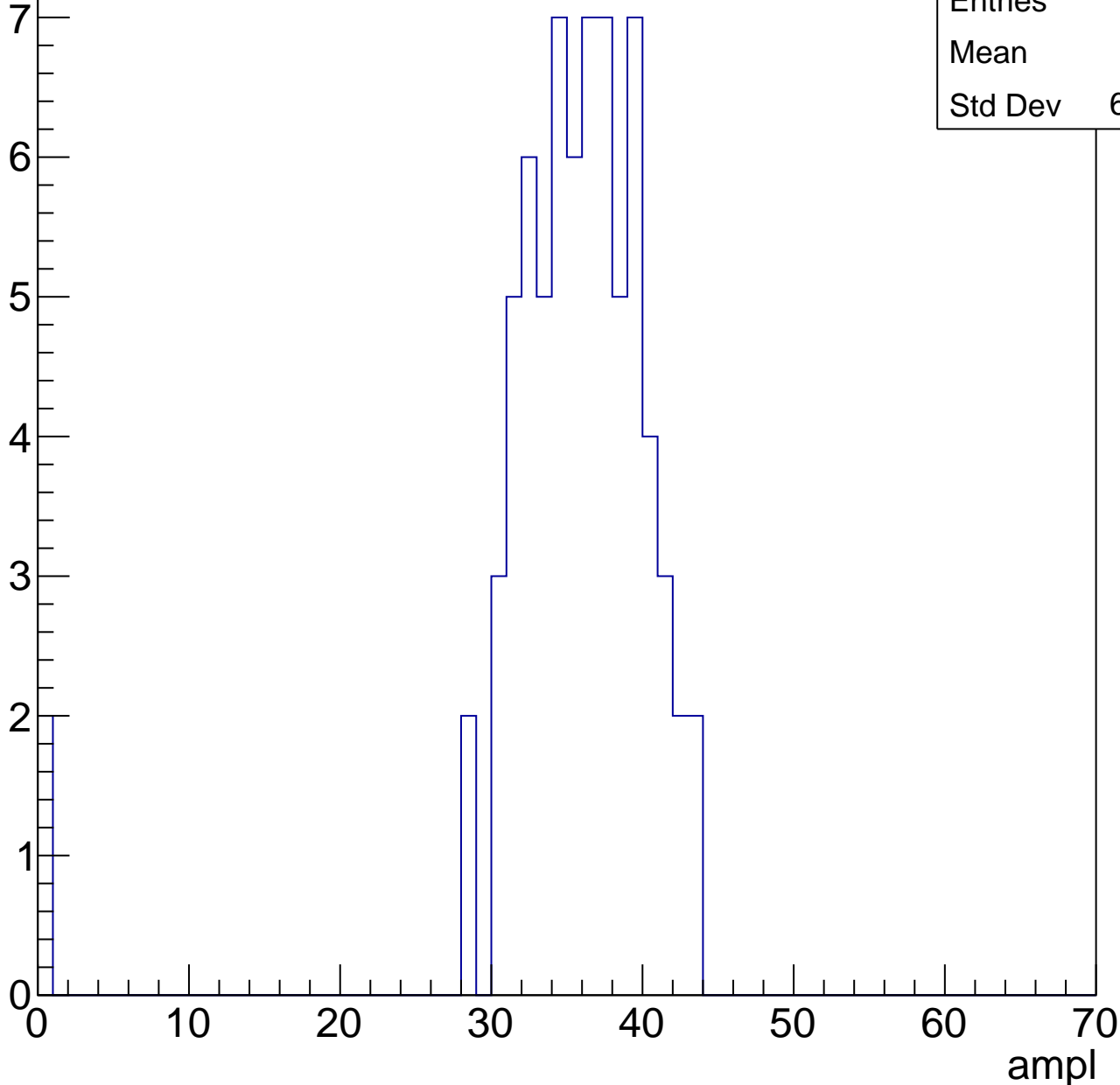


B1L103S, U23-ch105, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	73
Mean	34.7
Std Dev	6.828

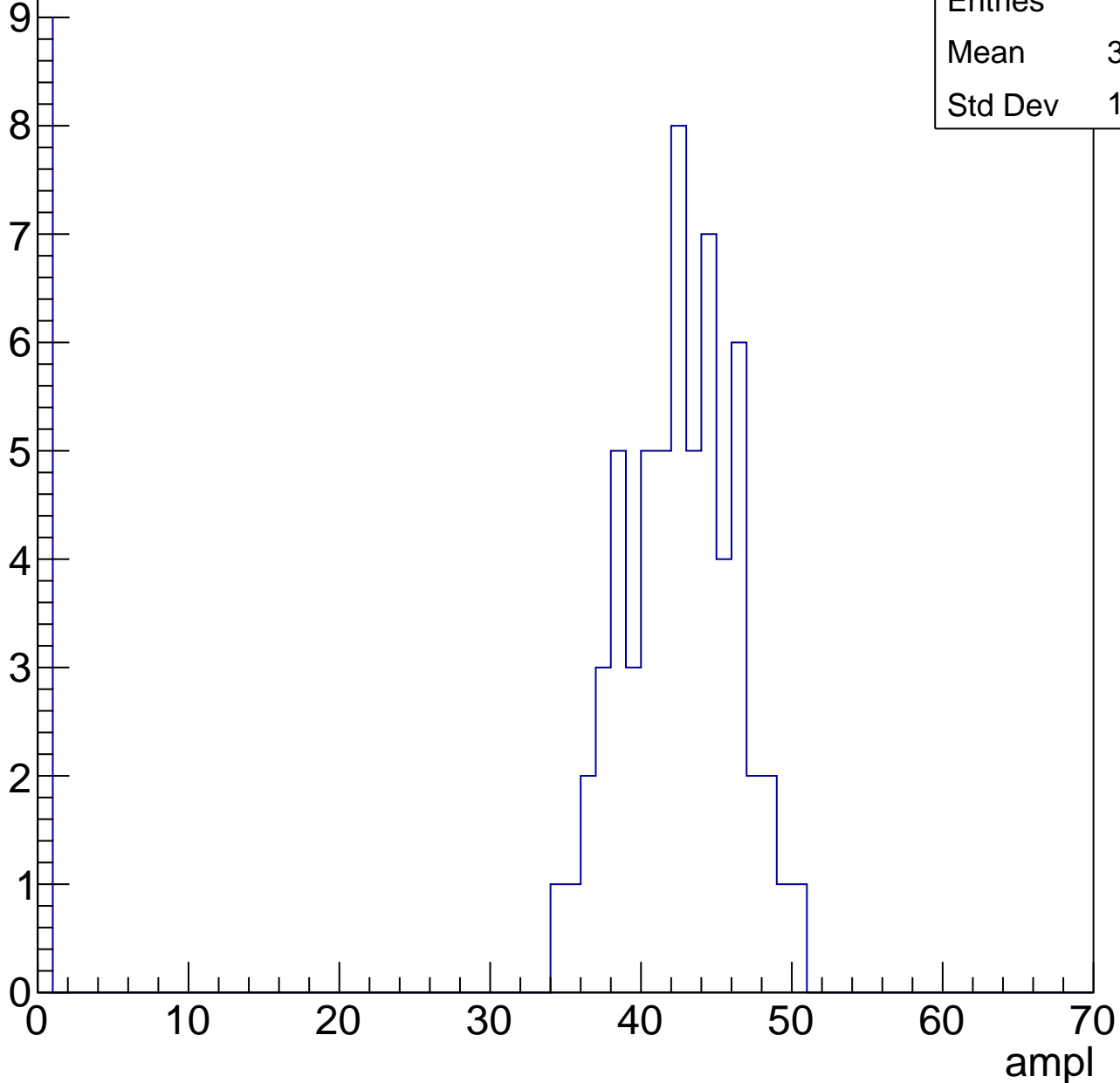


B1L103S, U23-ch105, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	36.69
Std Dev	14.49

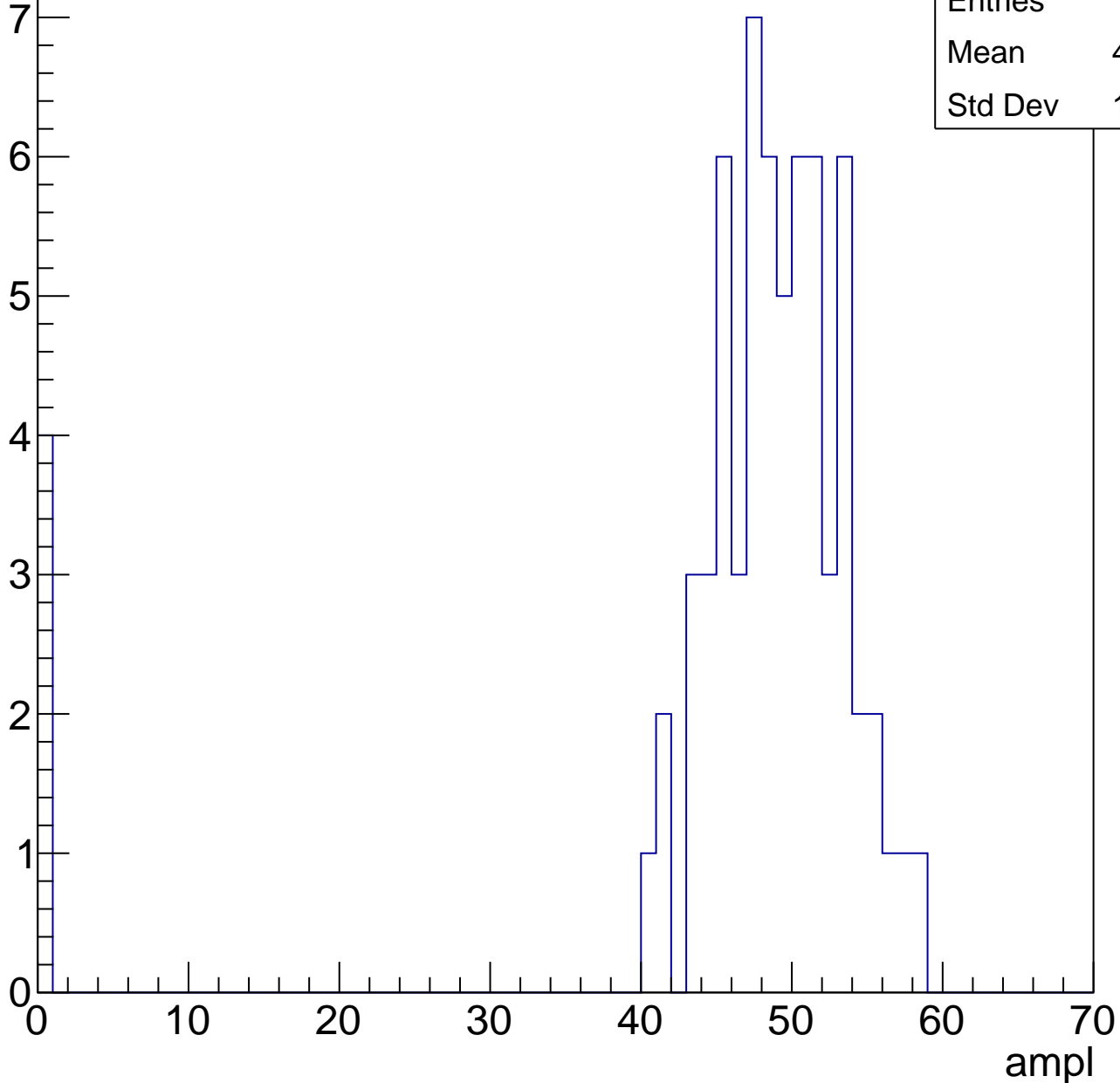


B1L103S, U23-ch105, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	45.91
Std Dev	12.11

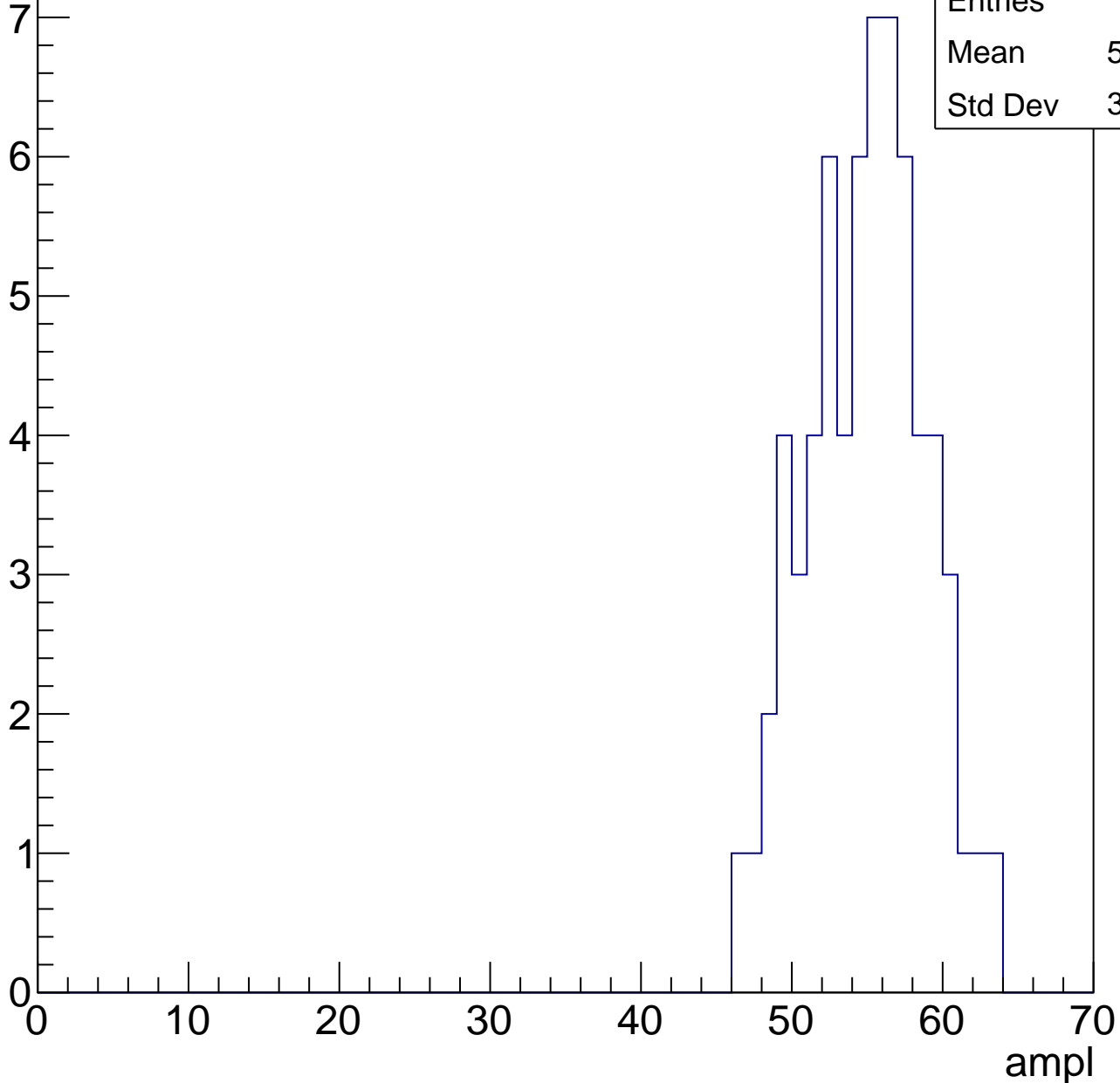


B1L103S, U23-ch105, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	54.46
Std Dev	3.799

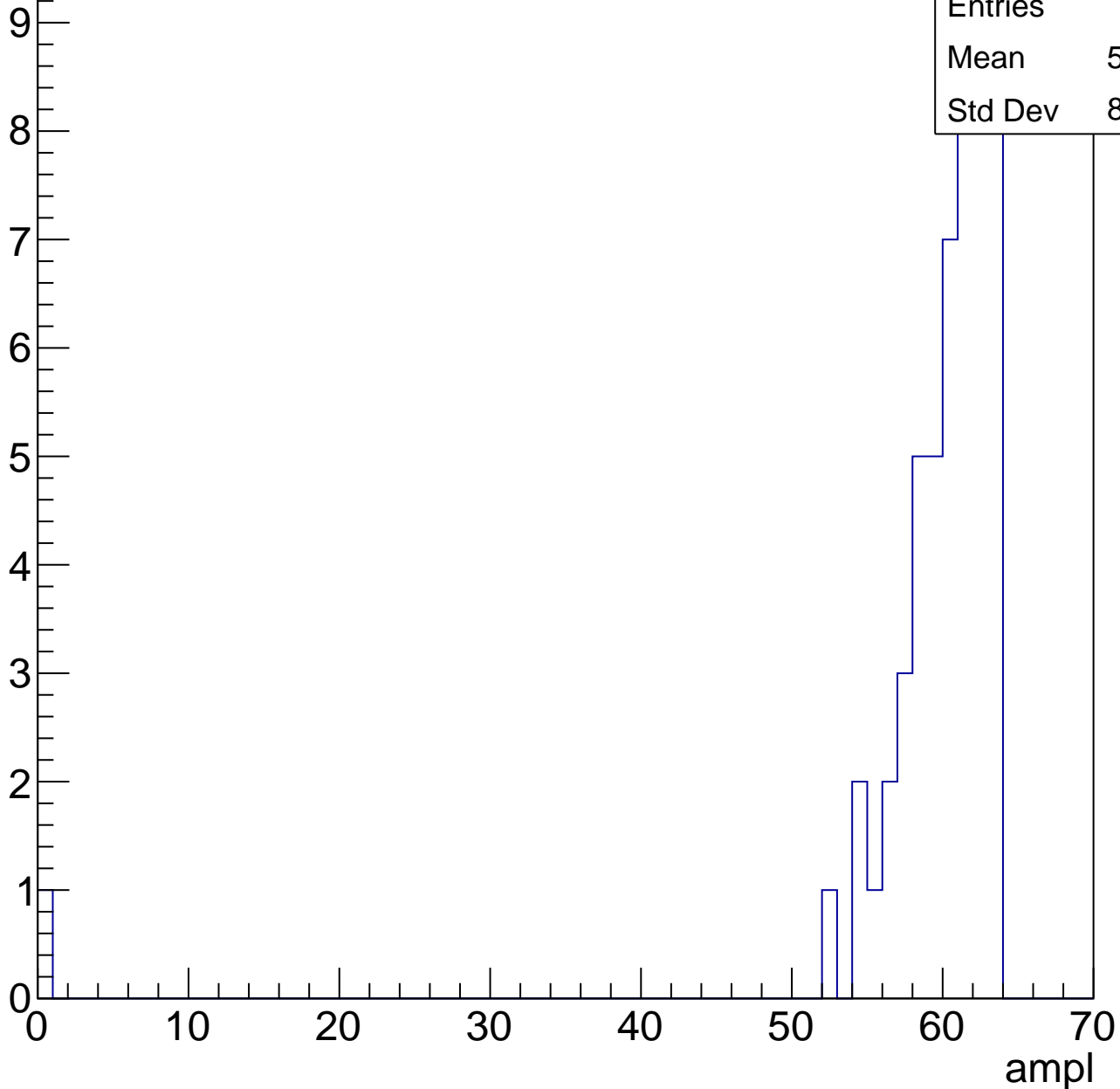


B1L103S, U23-ch105, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	53
Mean	58.75
Std Dev	8.556



B1L103S, U23-ch105, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

2

Mean

61

Std Dev

2

B1L103S, U23-ch105, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

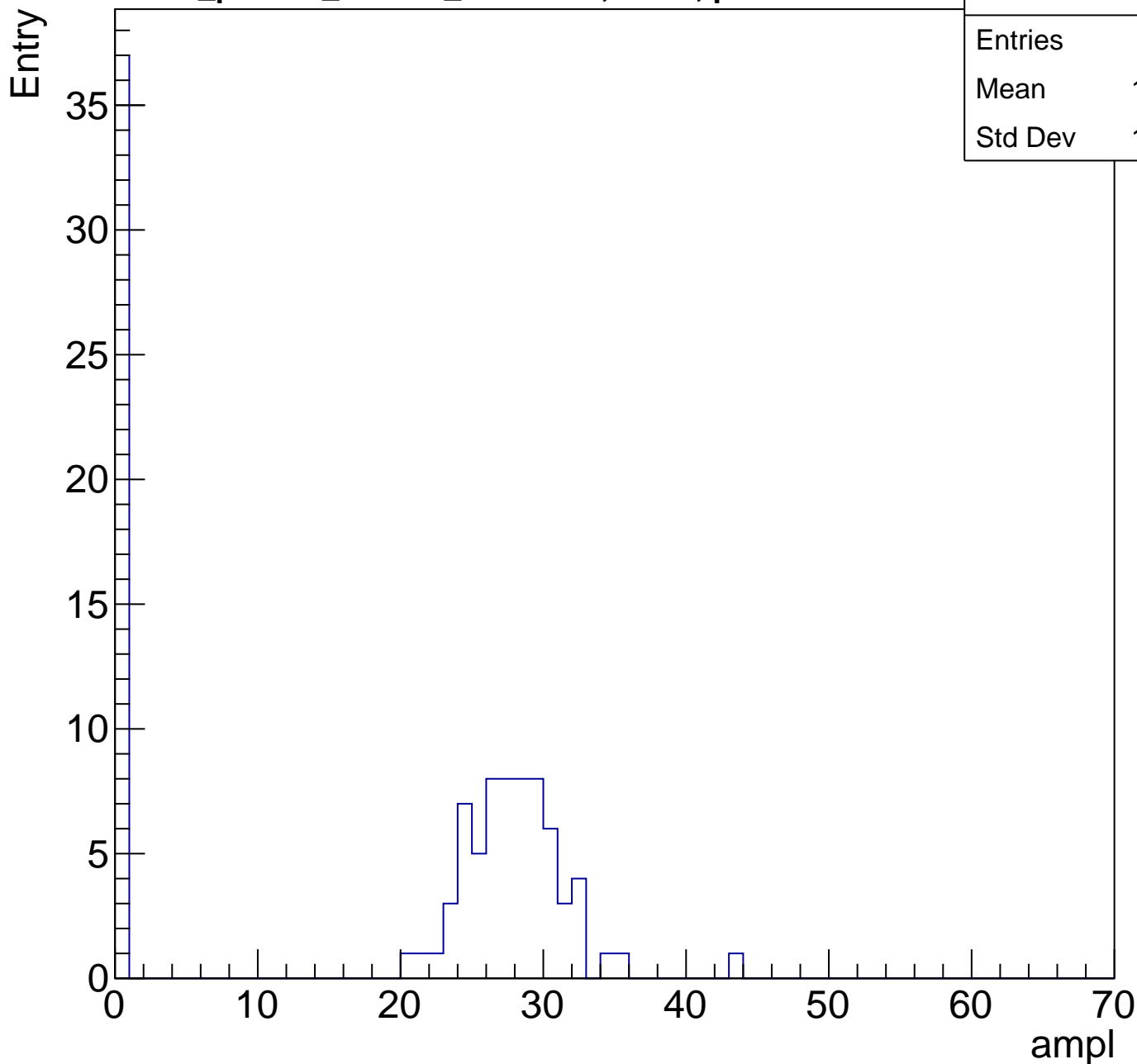
Entries	19
Mean	0
Std Dev	0

ampl

B1L103S, U23-ch106, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	103
Mean	17.65
Std Dev	13.52



B1L103S, U23-ch106, adc1

calib_packv5_041523_1651.root, FC#0, port C2

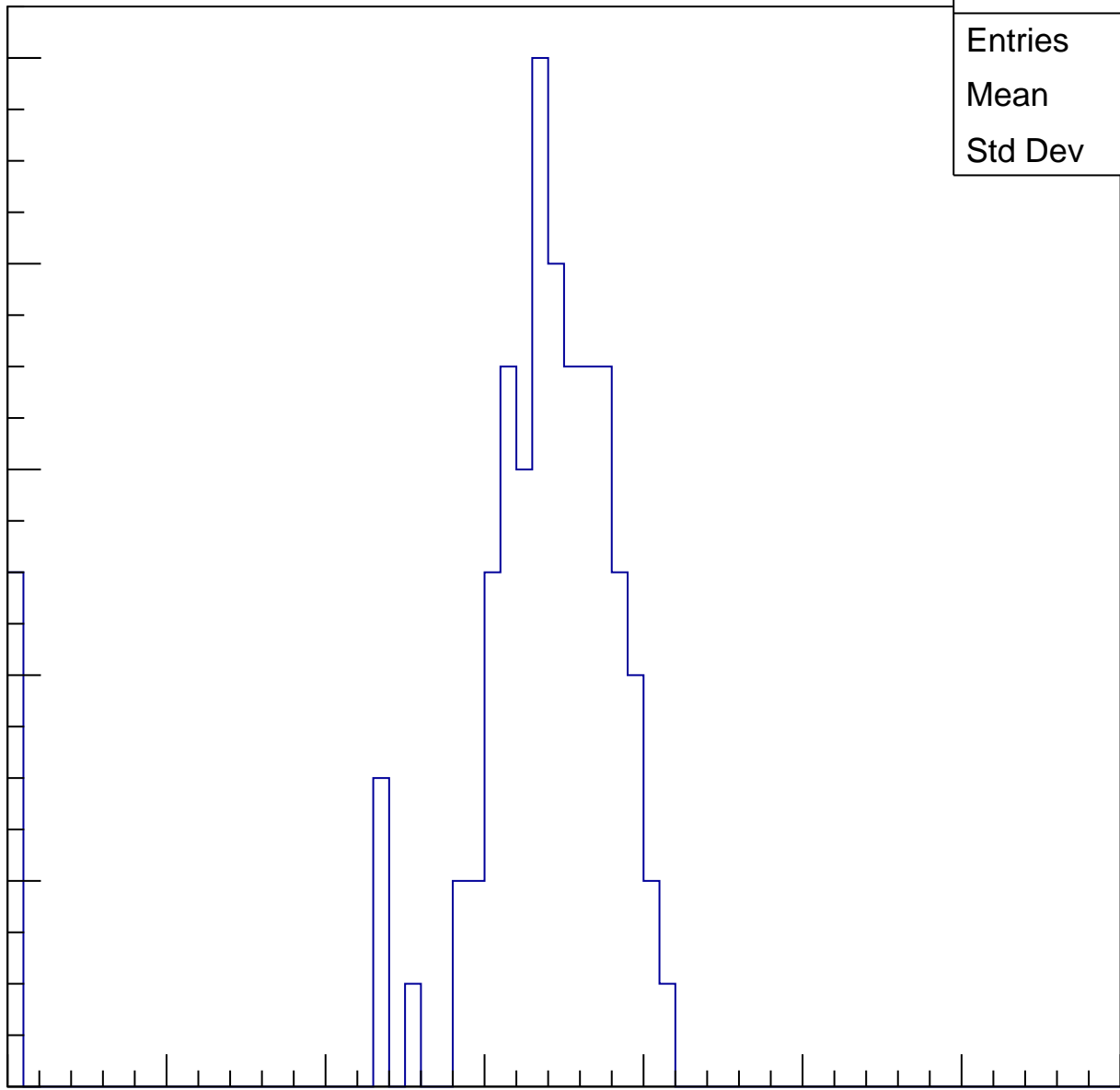
Entries	82
Mean	31.61
Std Dev	8.871

Entry

10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70

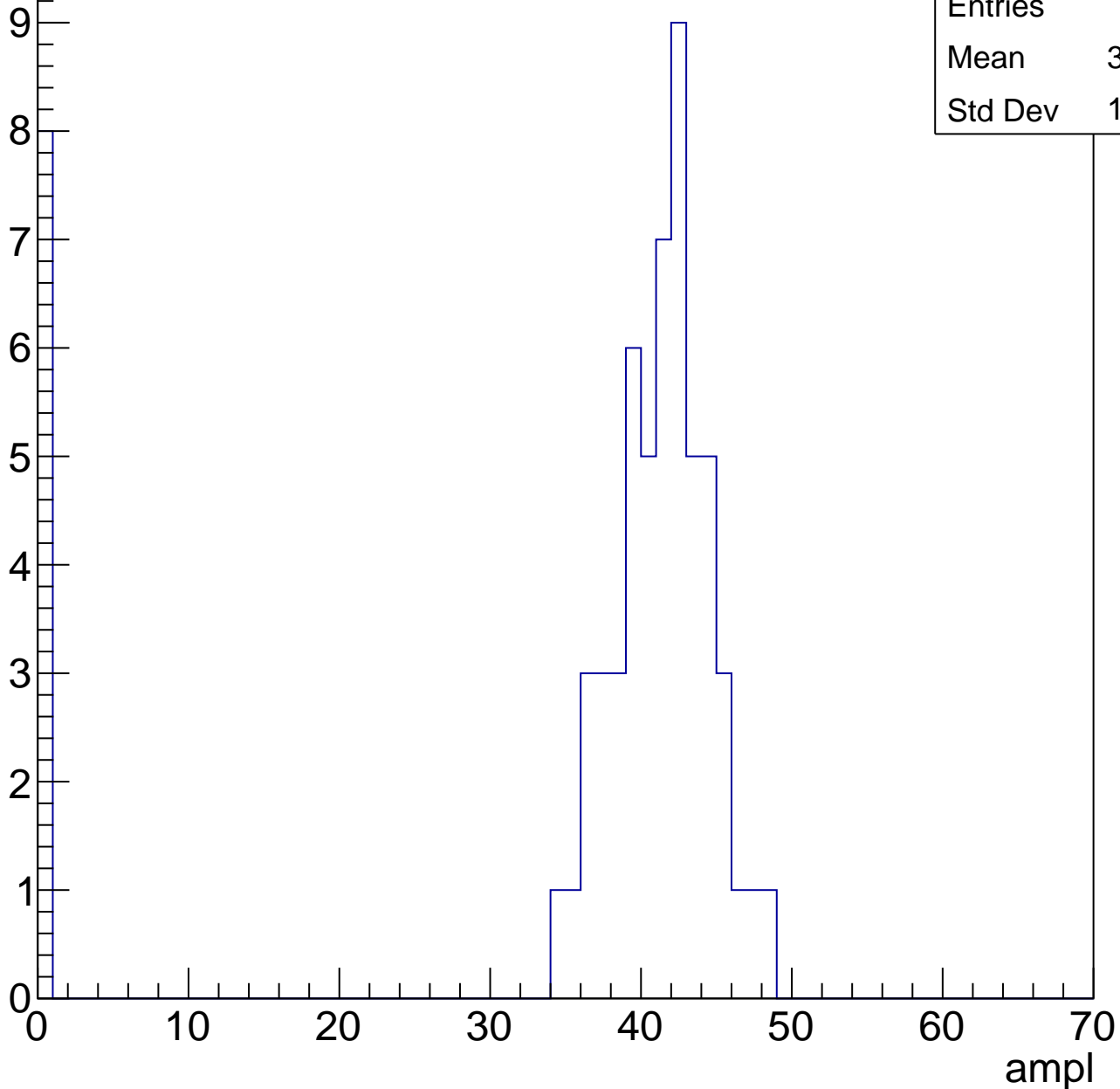


B1L103S, U23-ch106, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	35.68
Std Dev	14.02

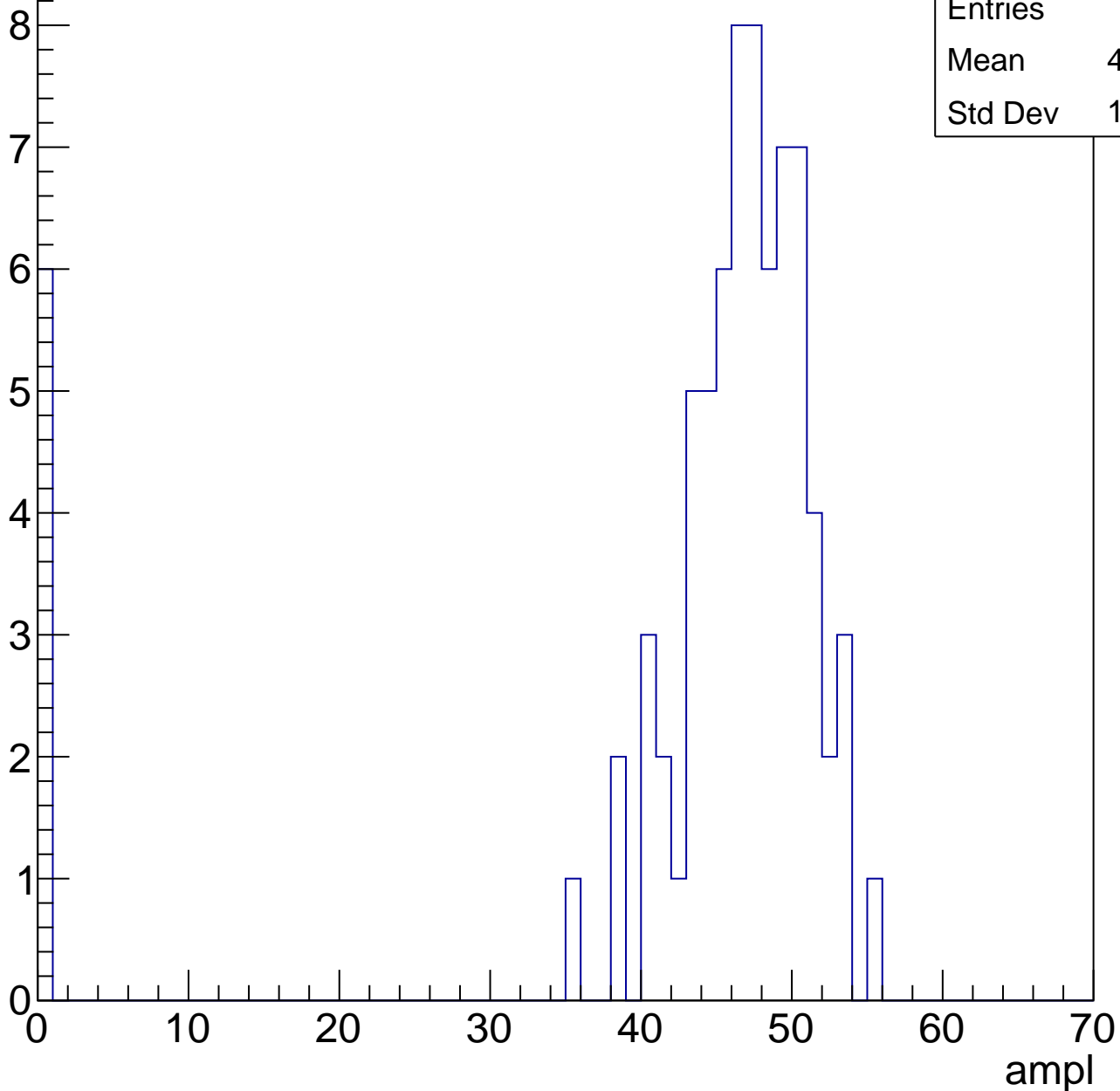


B1L103S, U23-ch106, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	77
Mean	42.95
Std Dev	13.03

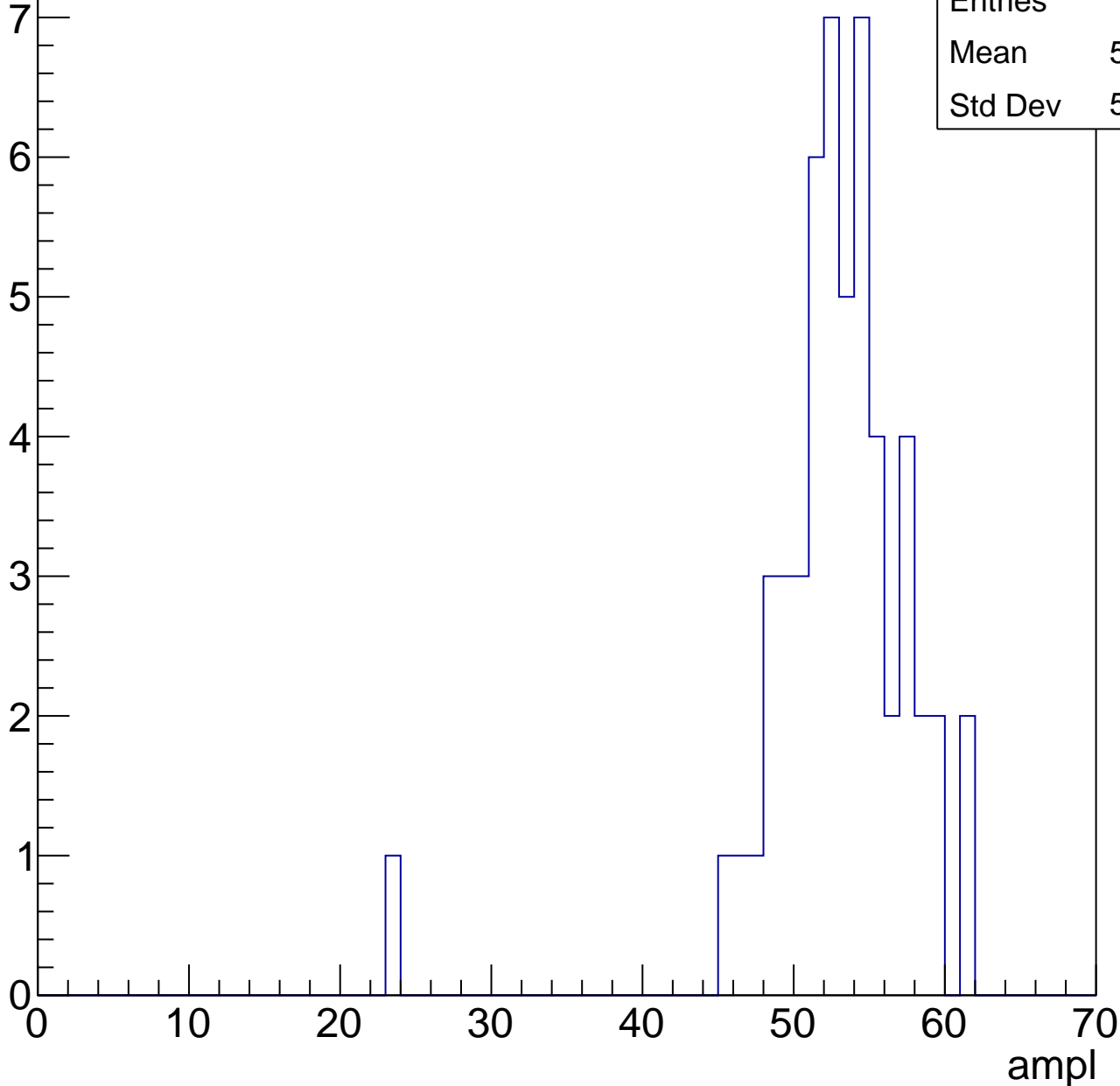


B1L103S, U23-ch106, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	54
Mean	52.43
Std Dev	5.387

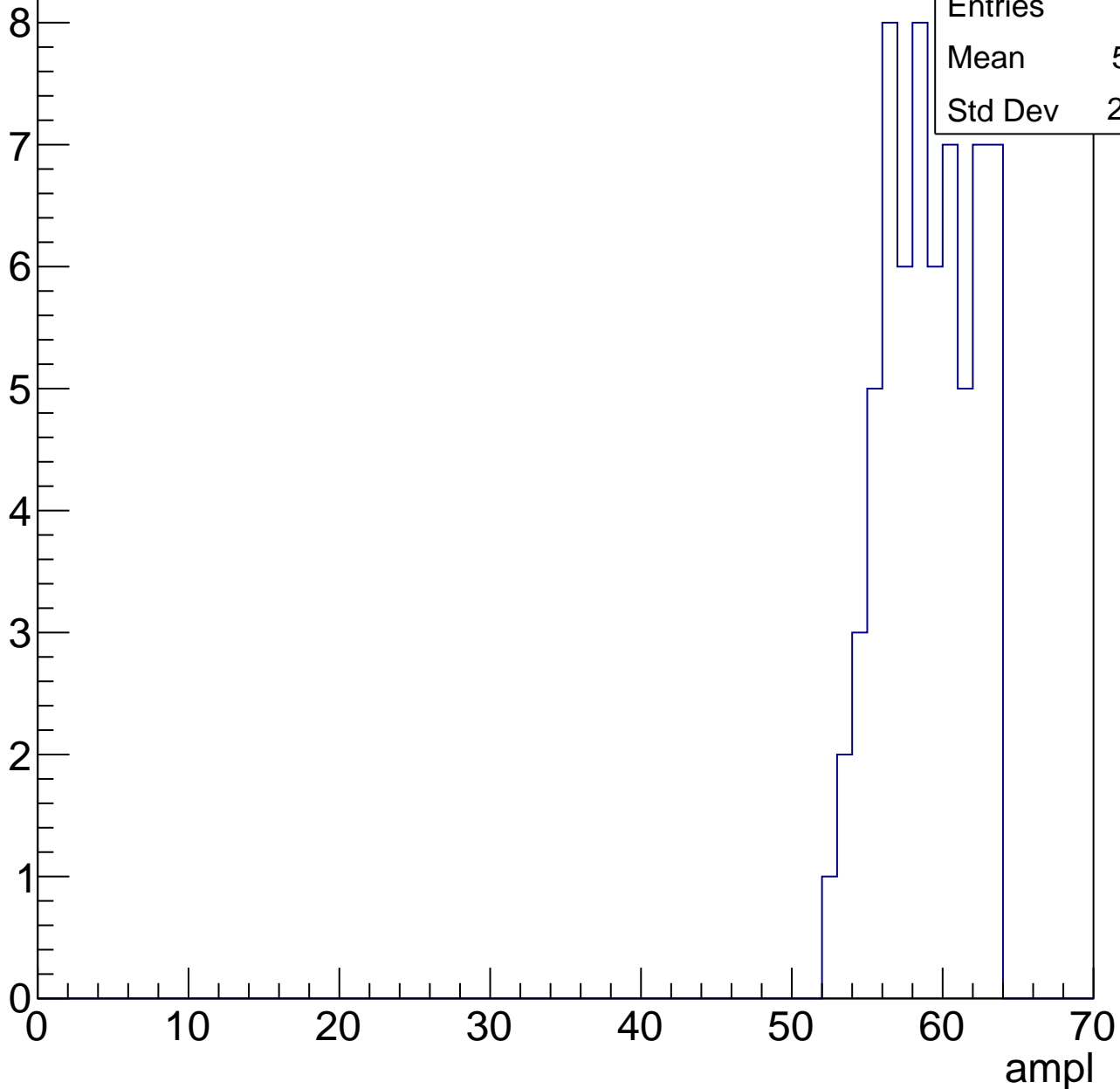


B1L103S, U23-ch106, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	58.51
Std Dev	2.952



B1L103S, U23-ch106, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

3

2.5

2

1.5

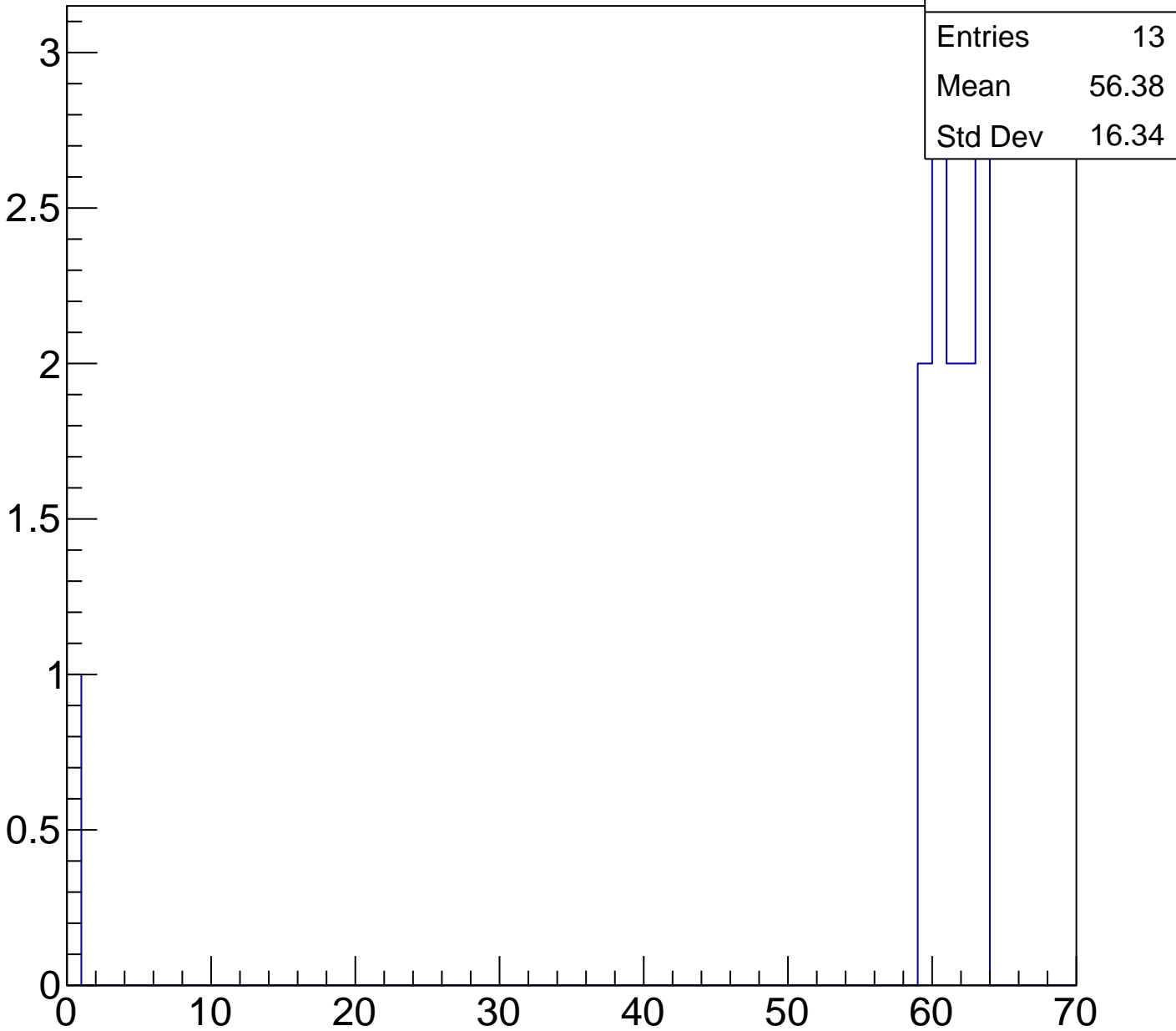
1

0.5

0

ampl

Entries	13
Mean	56.38
Std Dev	16.34

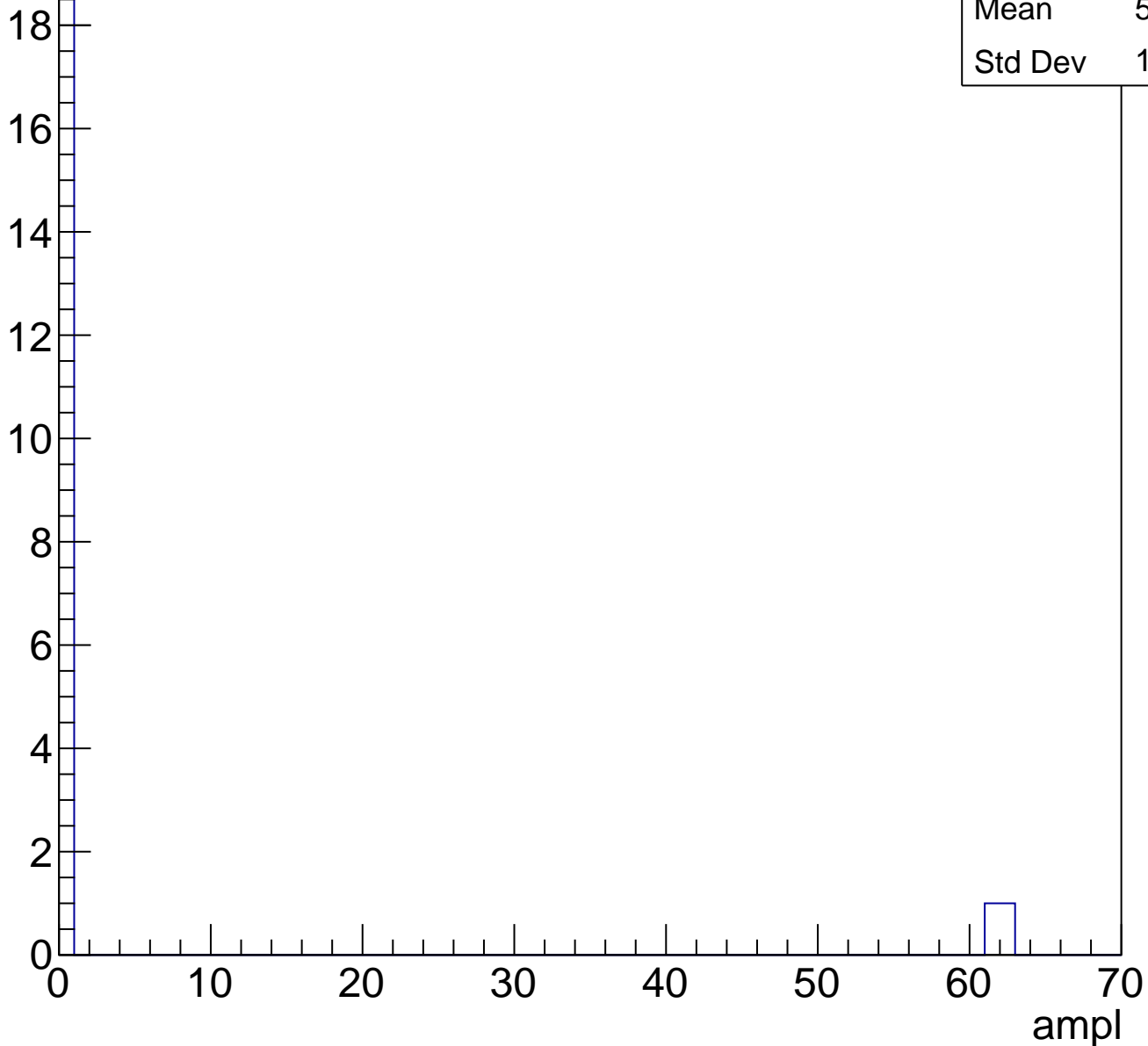


B1L103S, U23-ch106, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	21
Mean	5.857
Std Dev	18.05

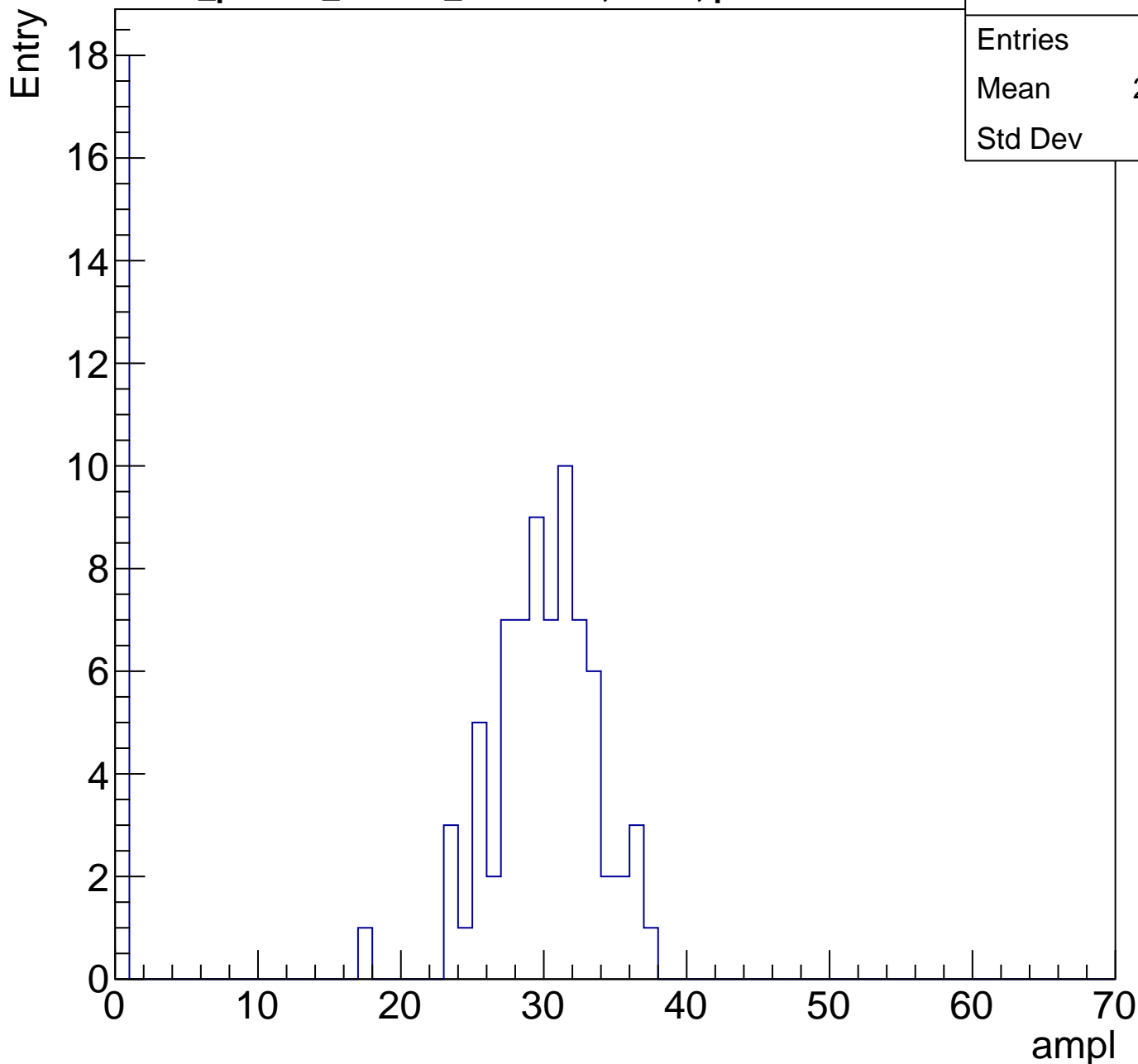
Entry



B1L103S, U23-ch107, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	91
Mean	23.71
Std Dev	12.2



B1L103S, U23-ch107, adc1

calib_packv5_041523_1651.root, FC#0, port C2

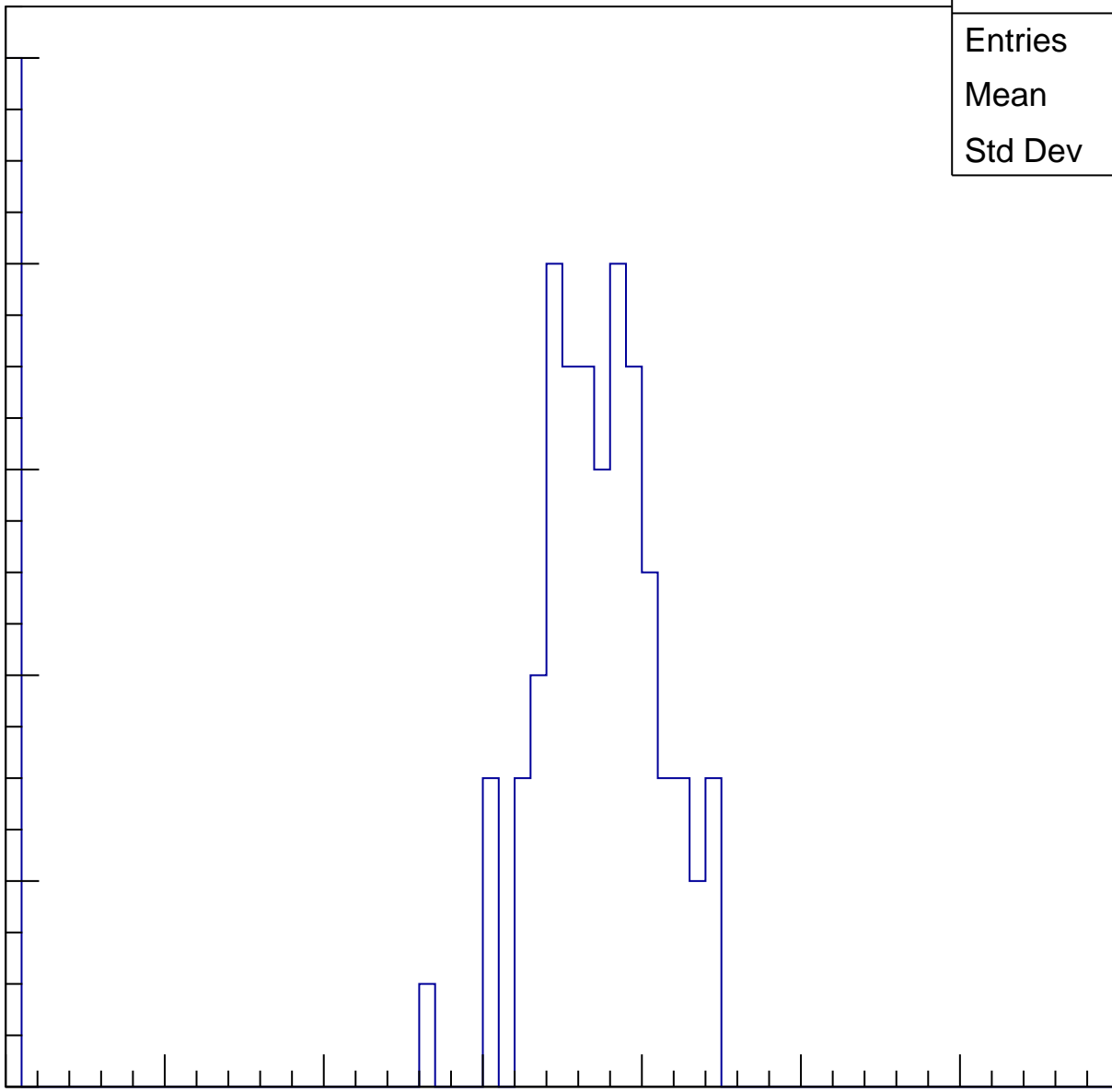
Entries	80
Mean	32.24
Std Dev	12.66

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

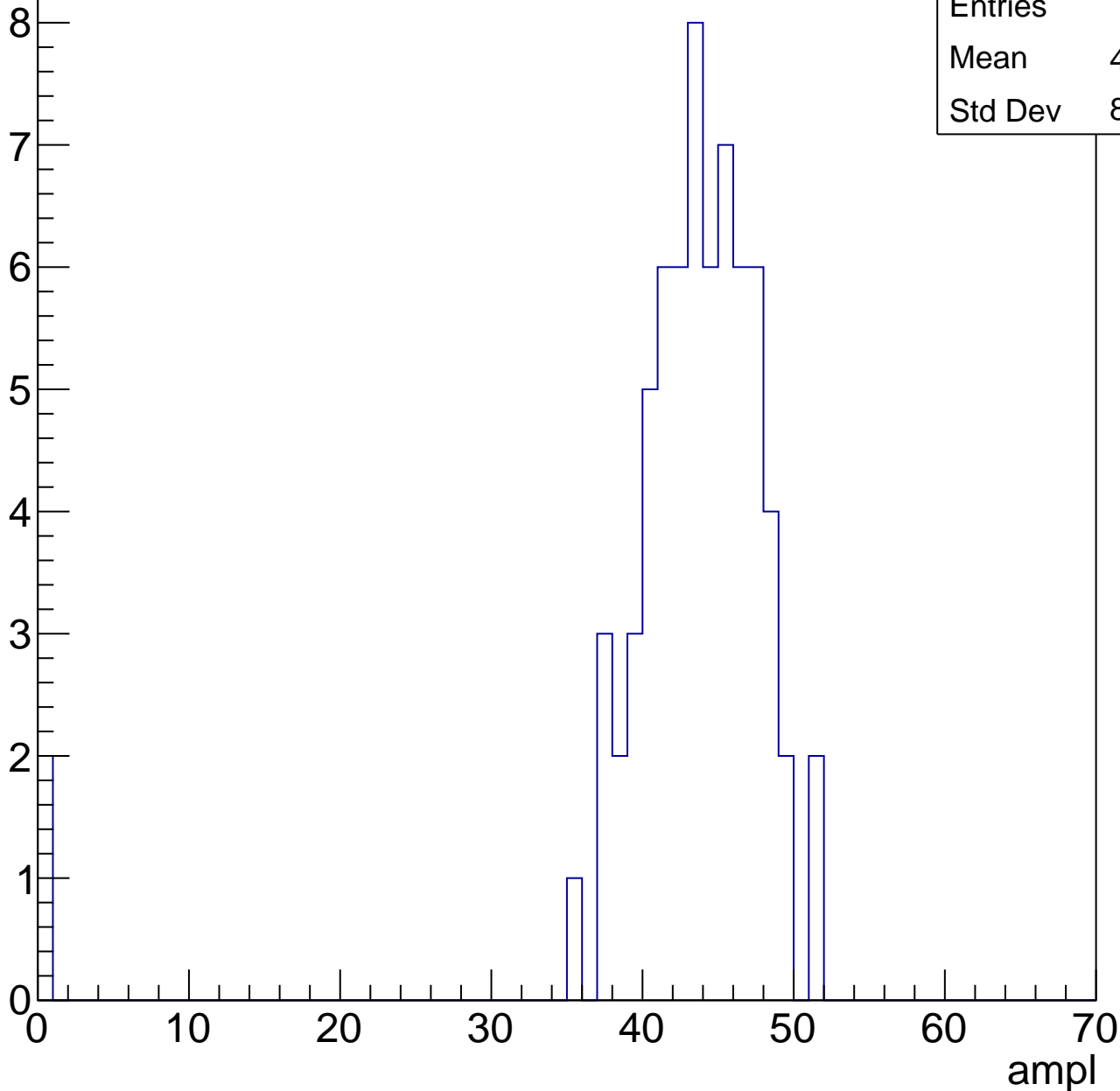


B1L103S, U23-ch107, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	42.17
Std Dev	8.058

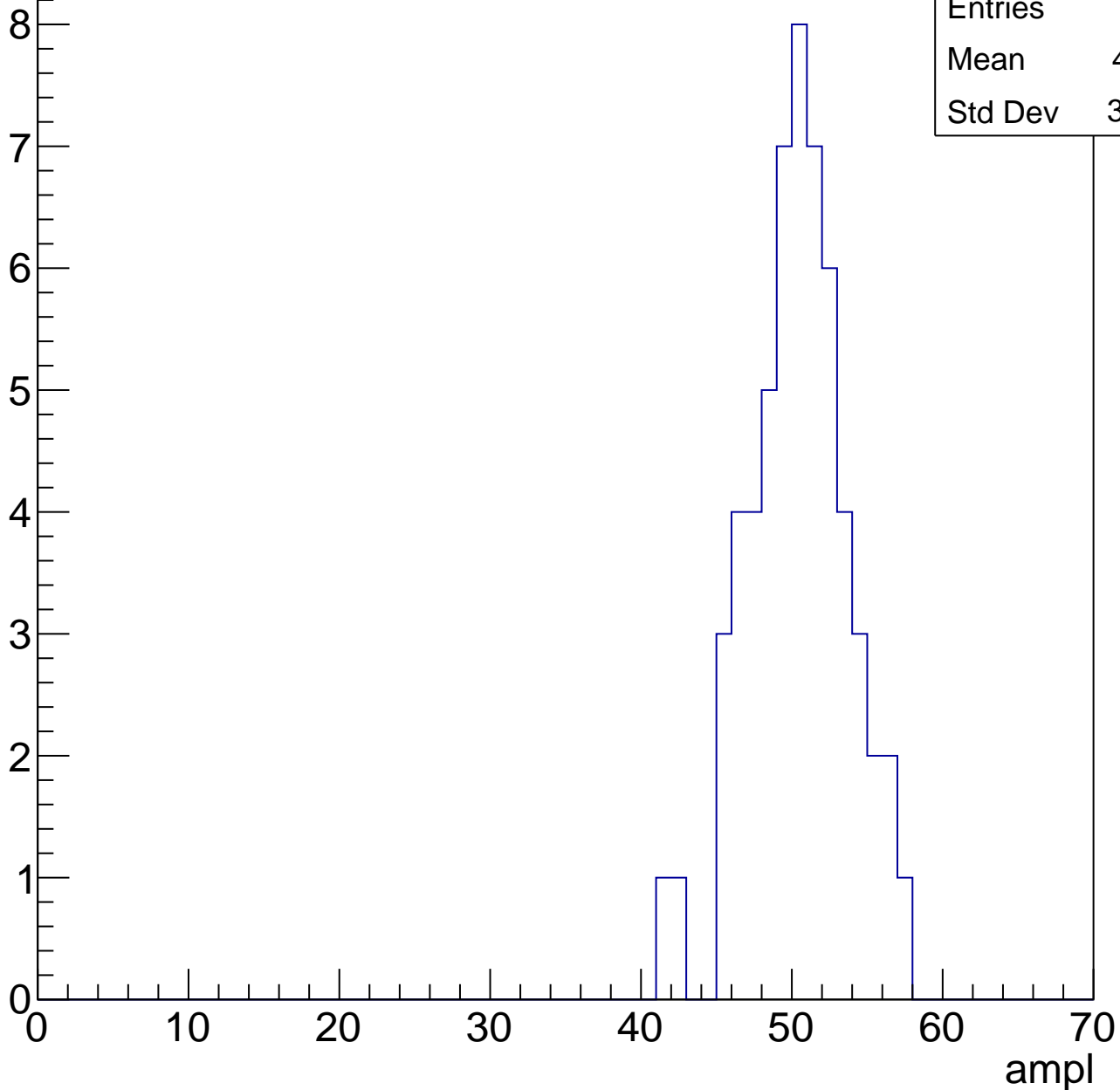


B1L103S, U23-ch107, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	49.91
Std Dev	3.302

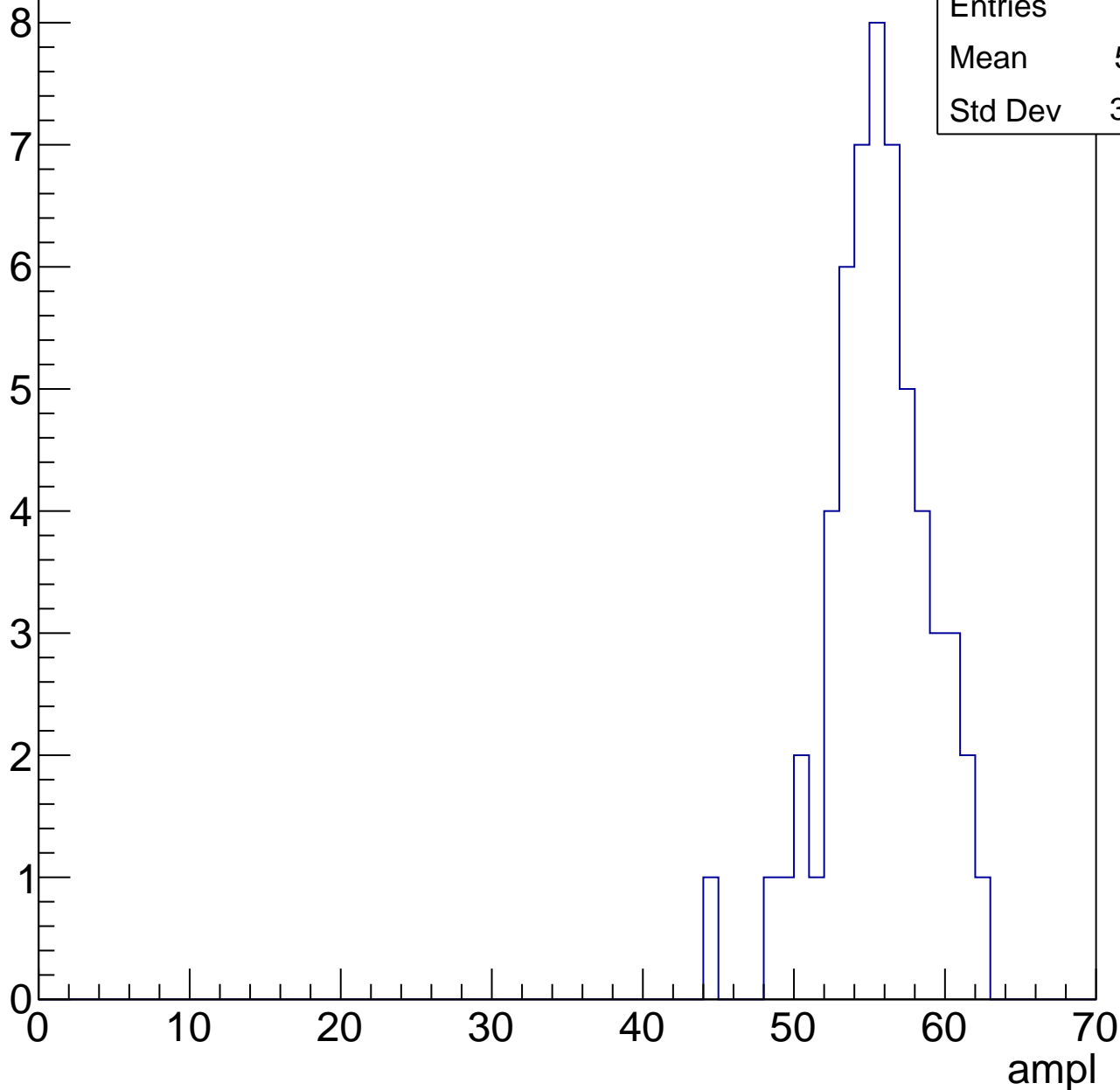


B1L103S, U23-ch107, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

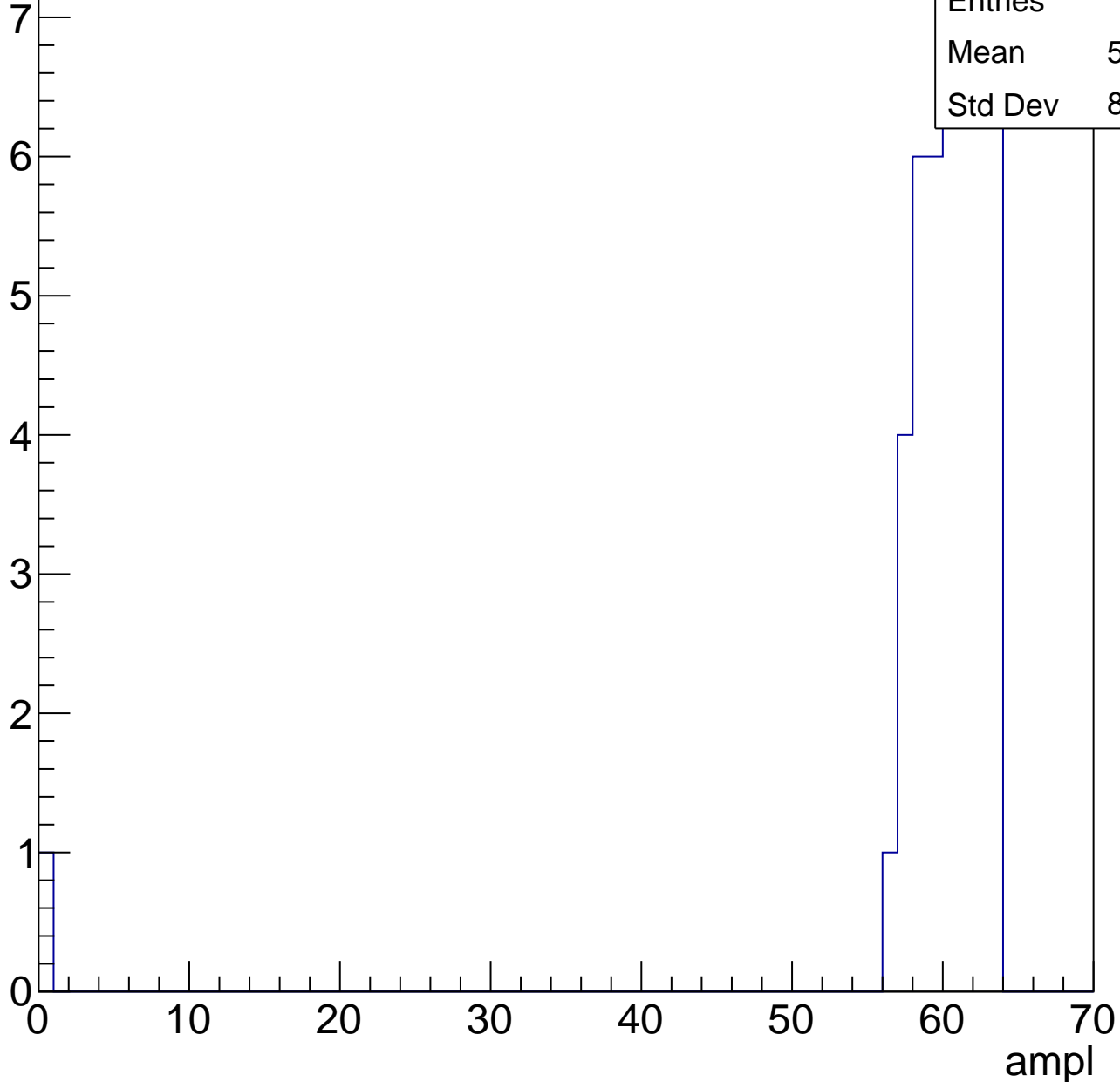
Entries	56
Mean	55.11
Std Dev	3.395



B1L103S, U23-ch107, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch107, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch107, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U23-ch108, adc0

calib_packv5_041523_1651.root, FC#0, port C2

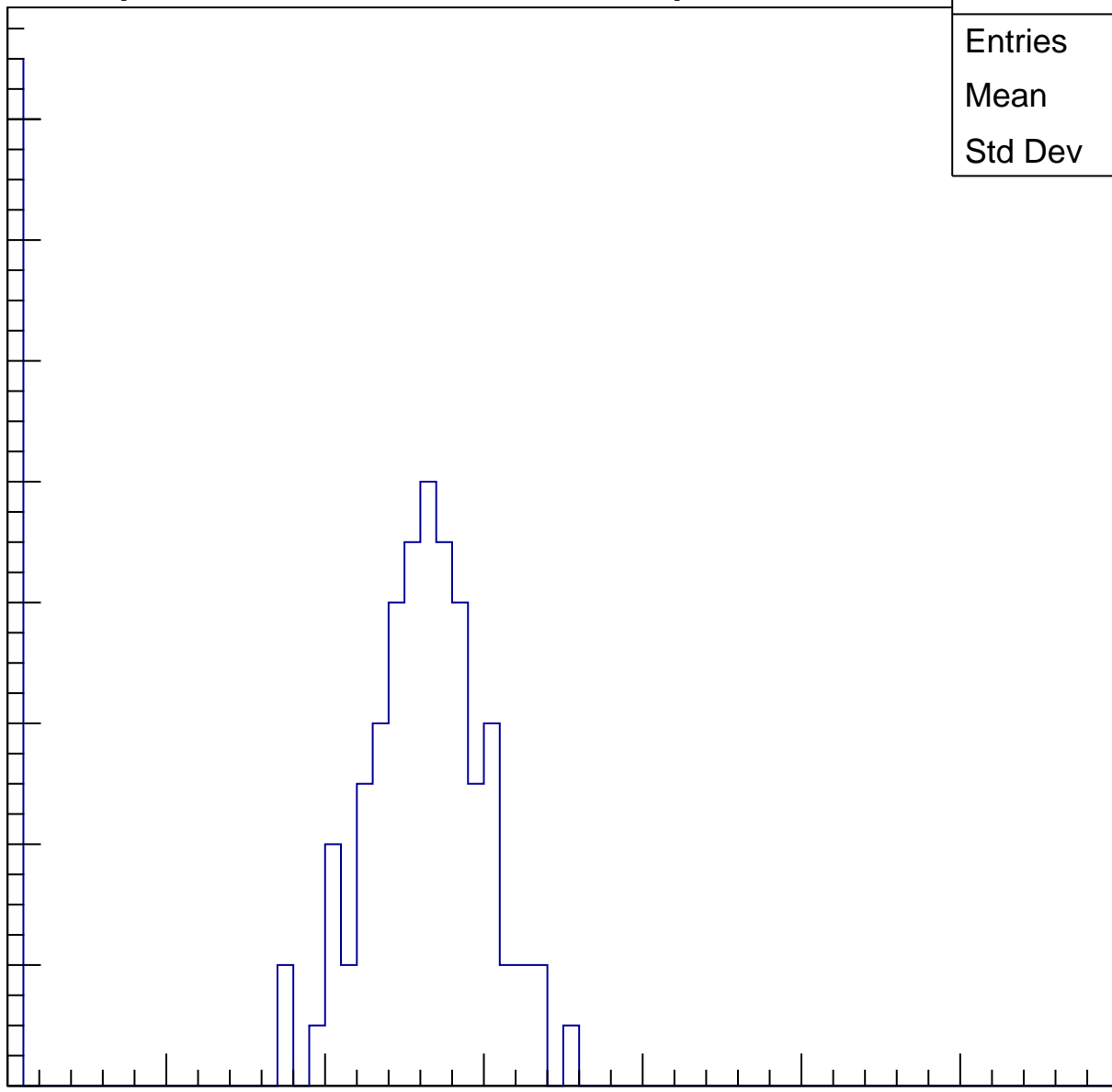
Entries	99
Mean	21.4
Std Dev	10.28

Entry

16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

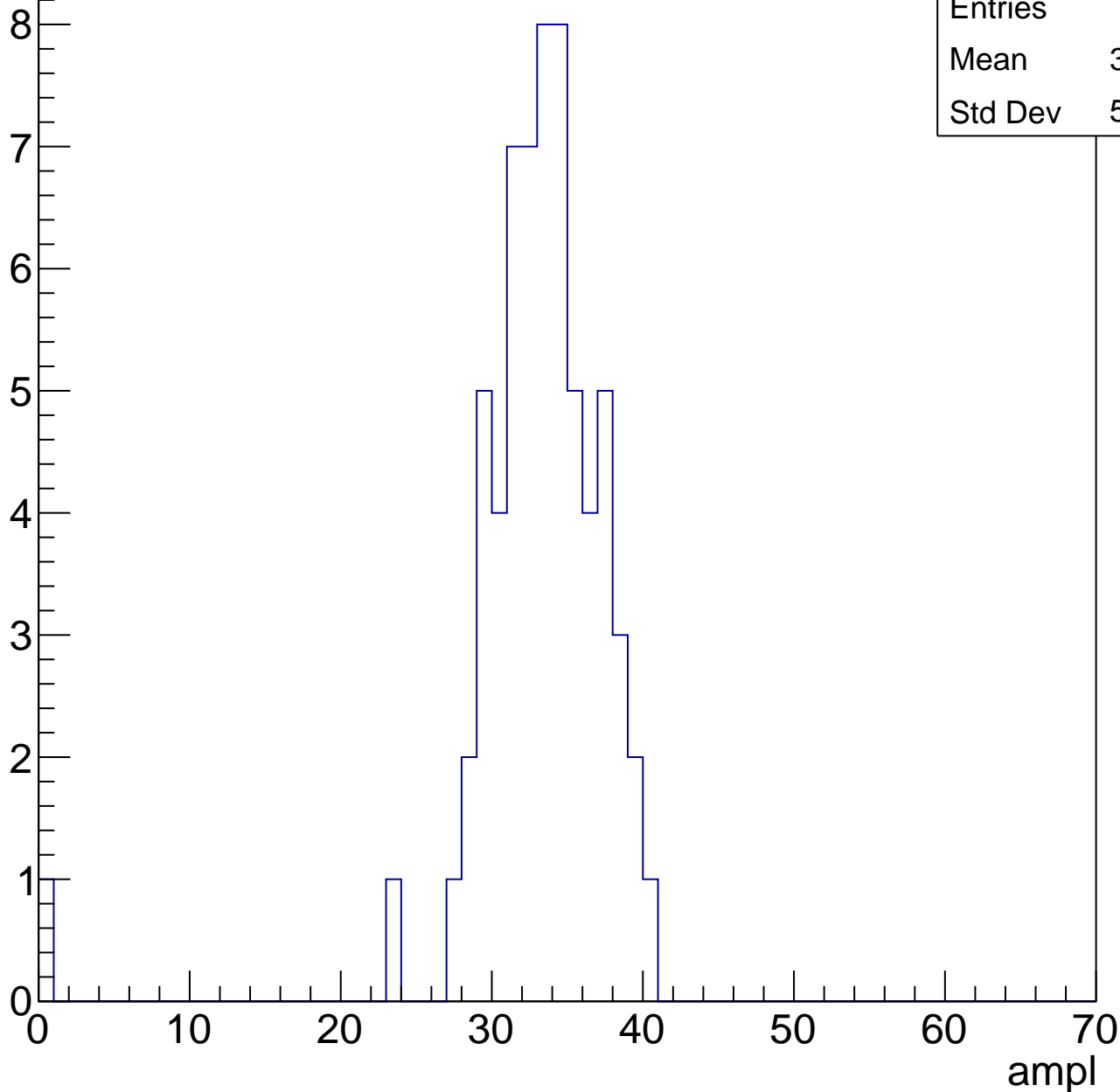


B1L103S, U23-ch108, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	32.56
Std Dev	5.235

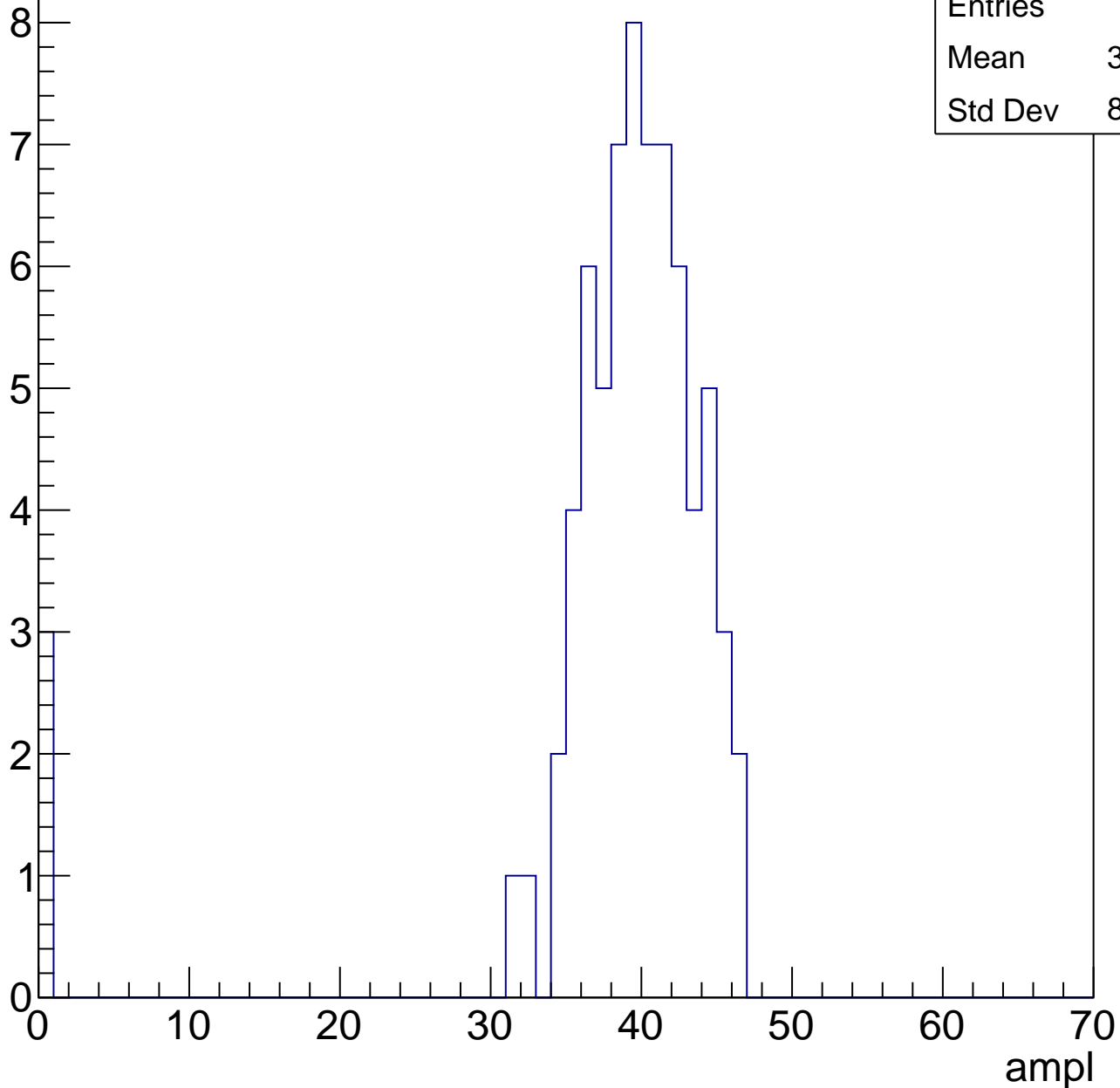


B1L103S, U23-ch108, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	37.86
Std Dev	8.609

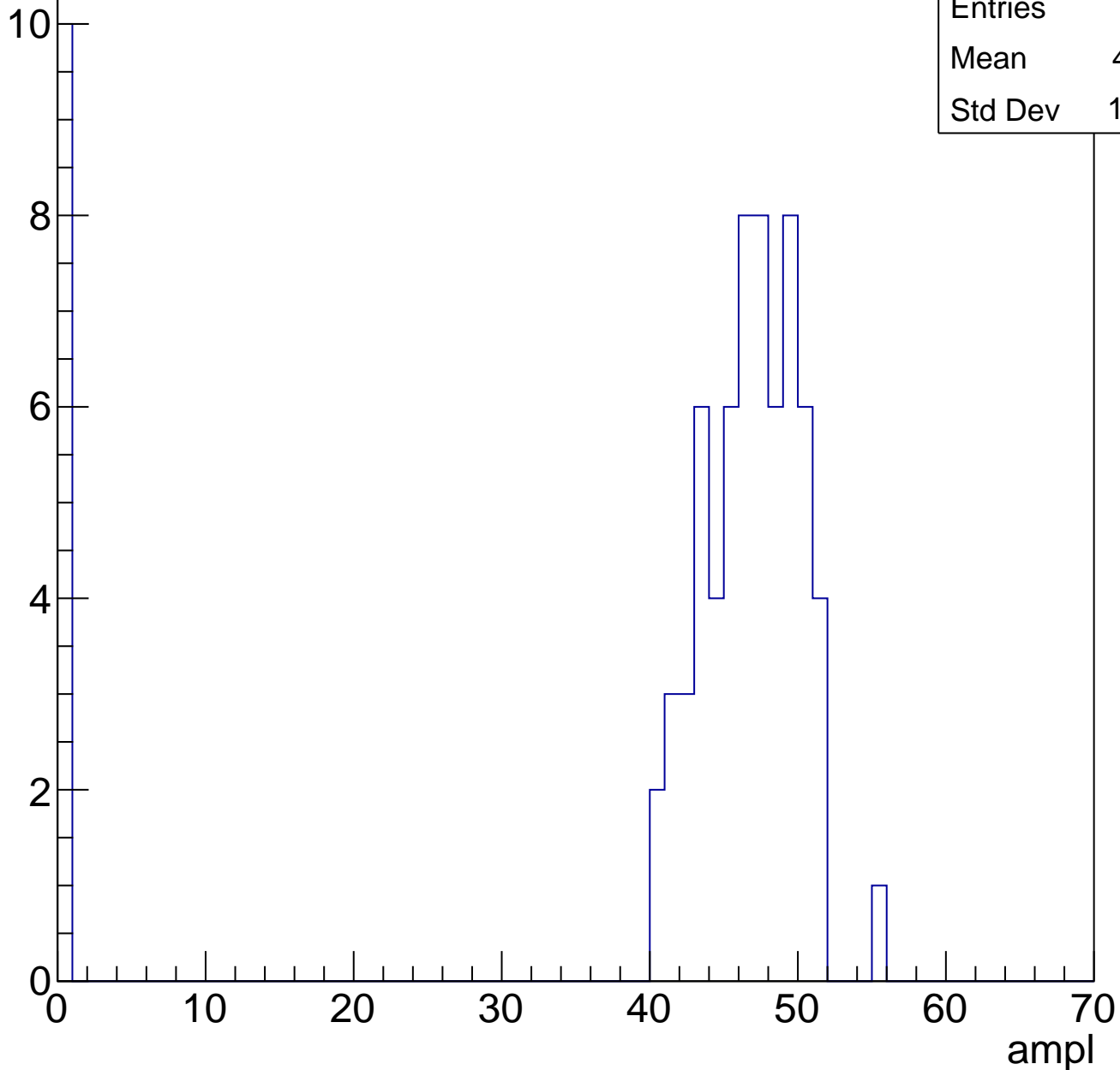


B1L103S, U23-ch108, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	75
Mean	40.21
Std Dev	16.04

Entry

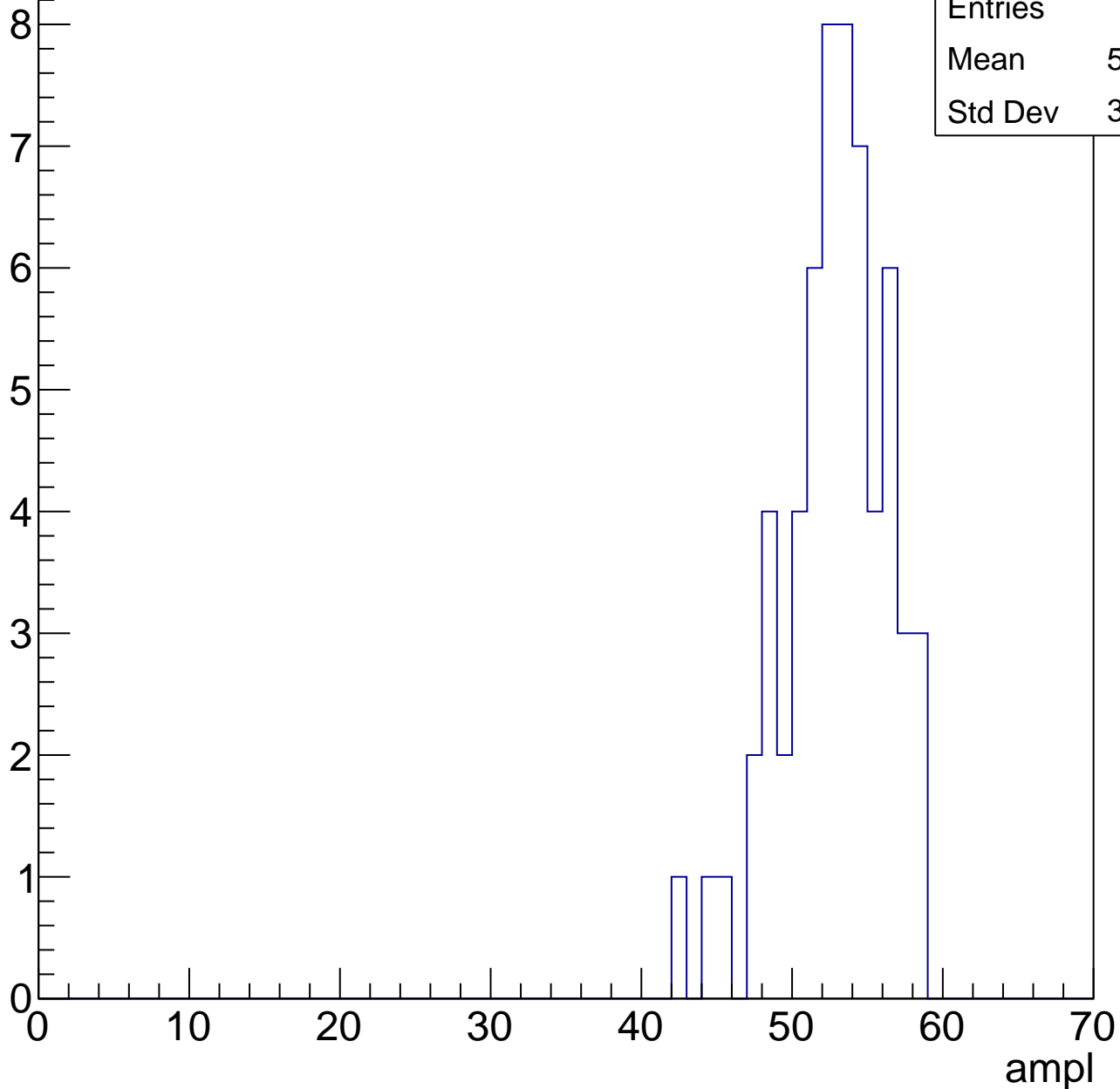


B1L103S, U23-ch108, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	52.33
Std Dev	3.443

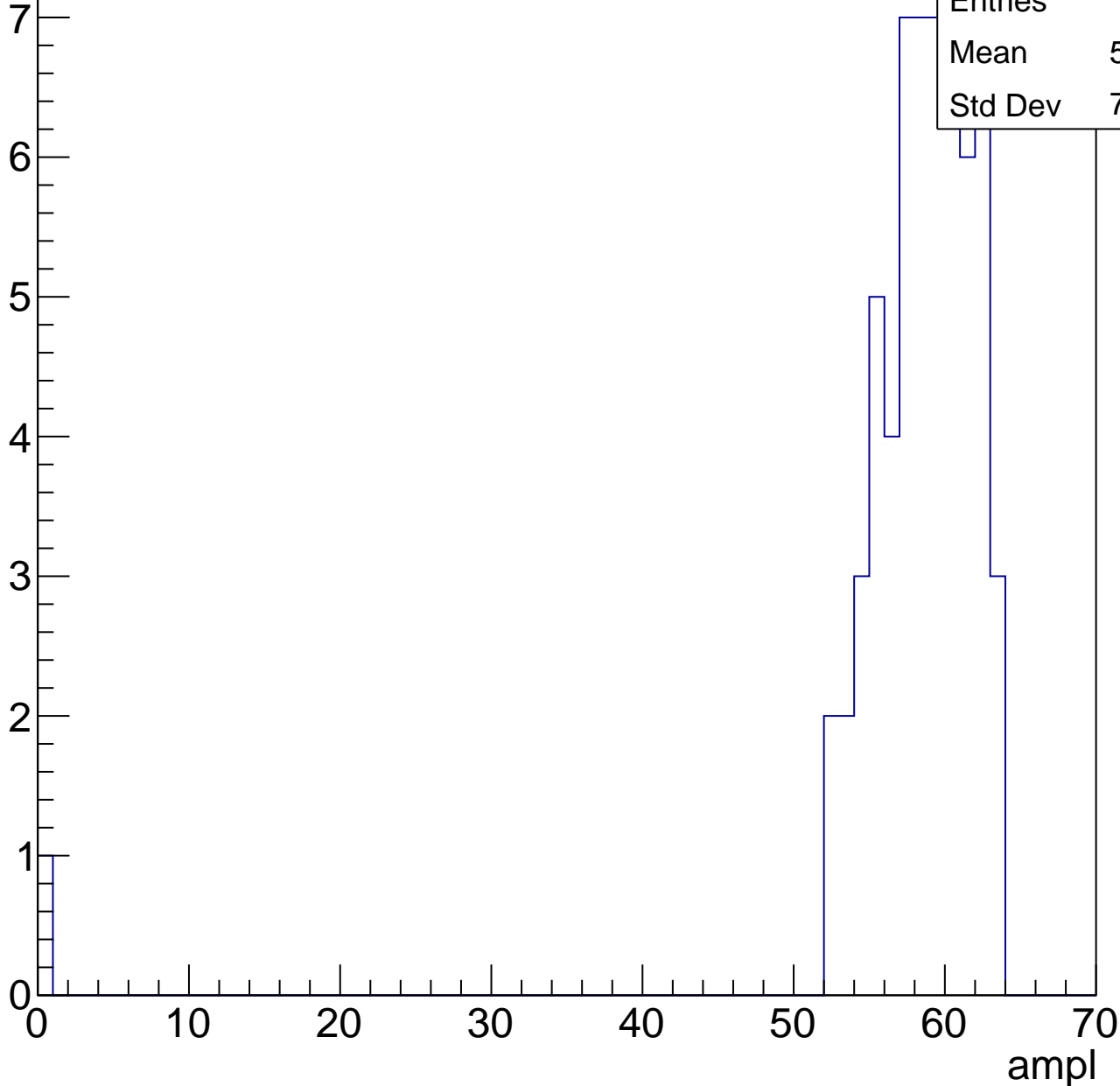


B1L103S, U23-ch108, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	57.34
Std Dev	7.946

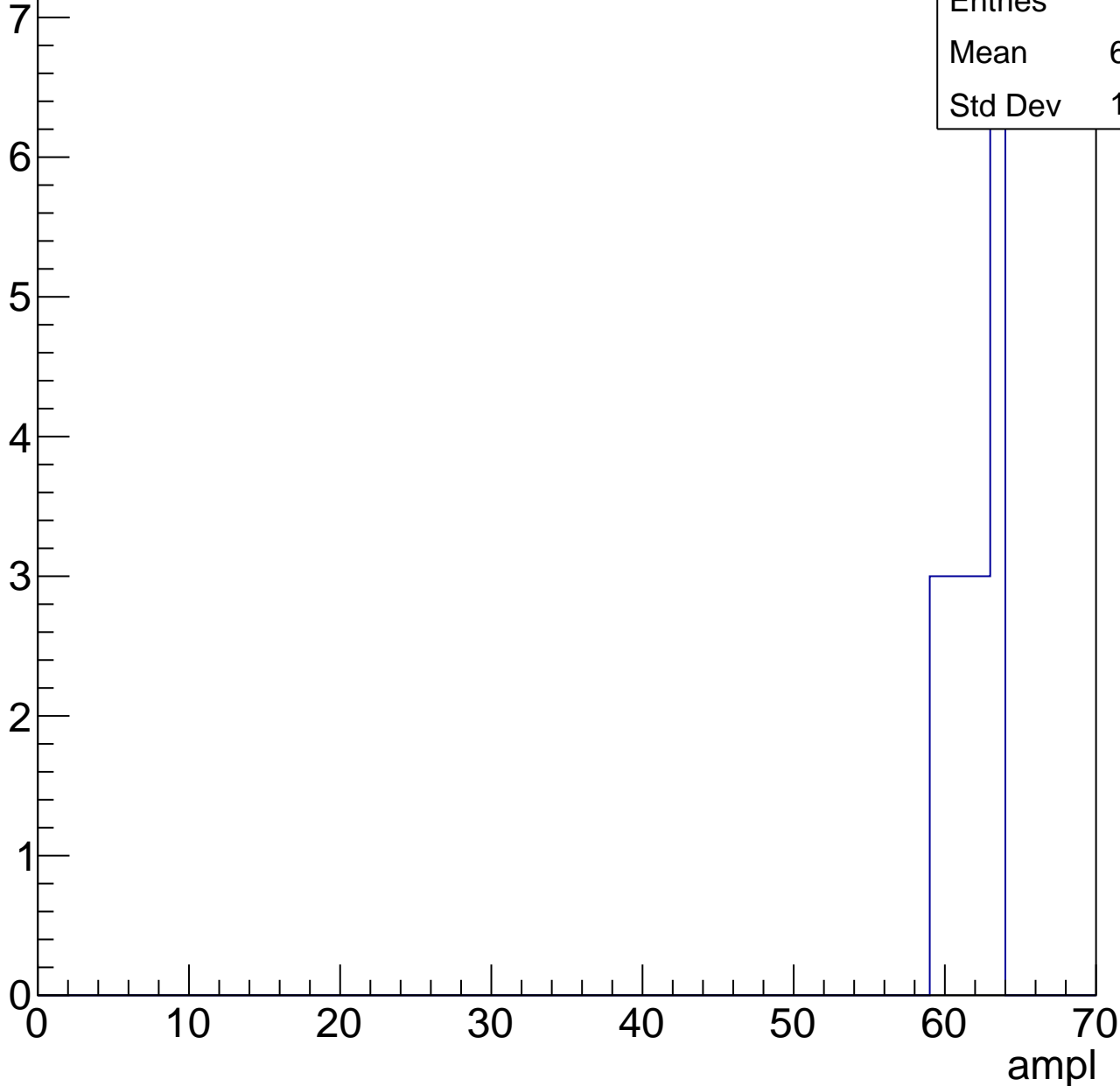


B1L103S, U23-ch108, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

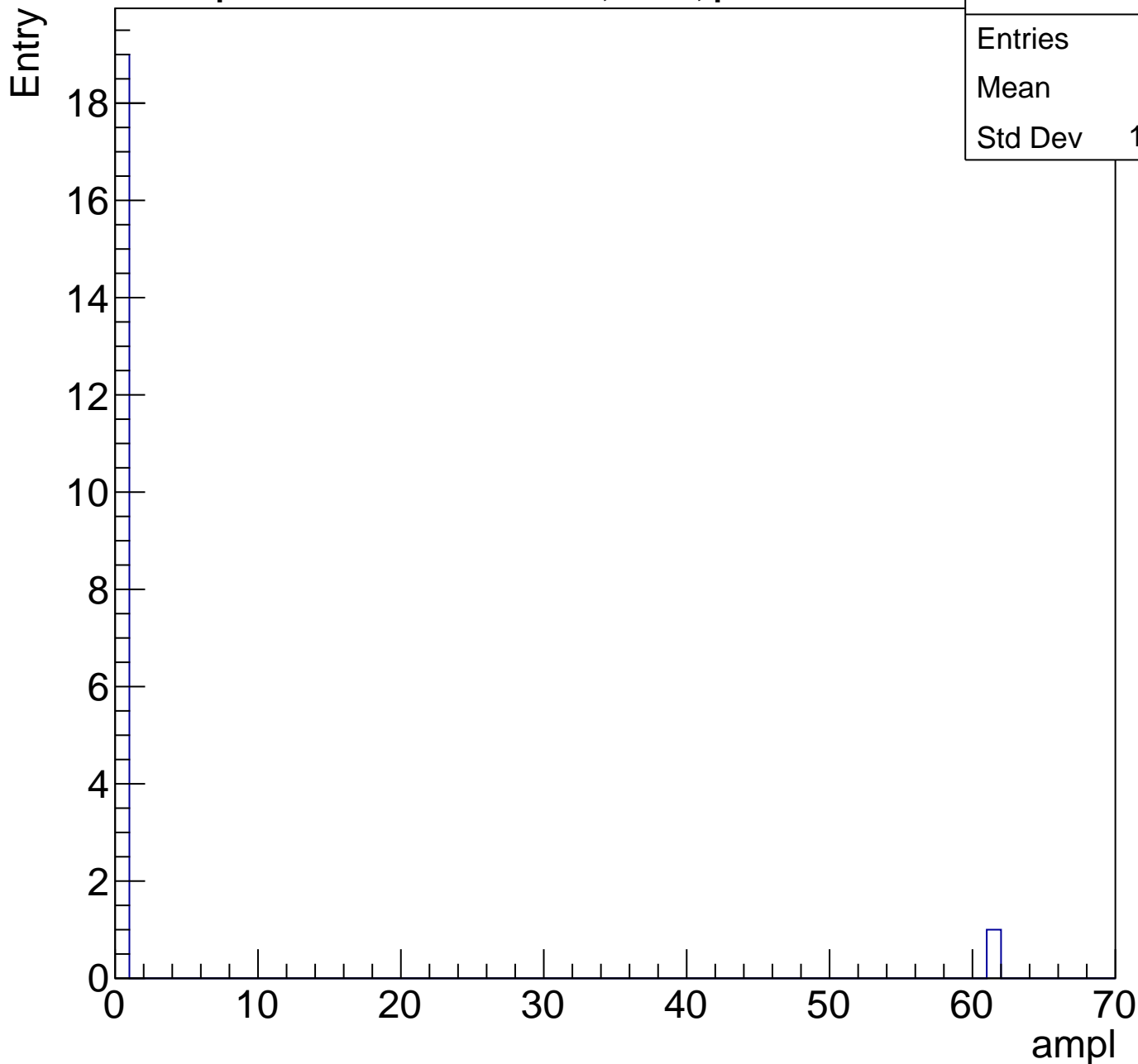
Entries	19
Mean	61.42
Std Dev	1.498



B1L103S, U23-ch108, adc7

calib_packv5_041523_1651.root, FC#0, port C2

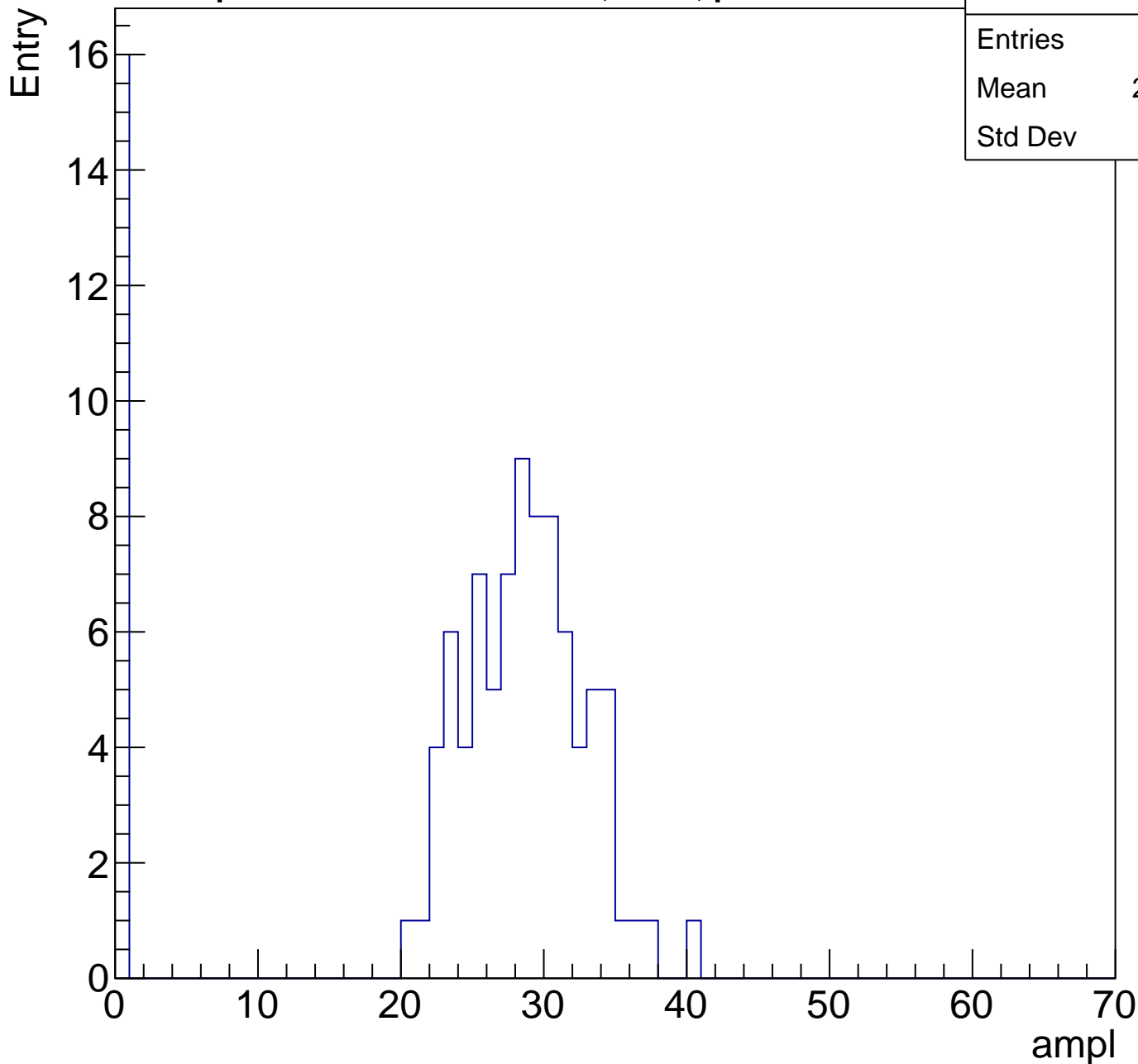
Entries	20
Mean	3.05
Std Dev	13.29



B1L103S, U23-ch109, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	100
Mean	23.78
Std Dev	11.01

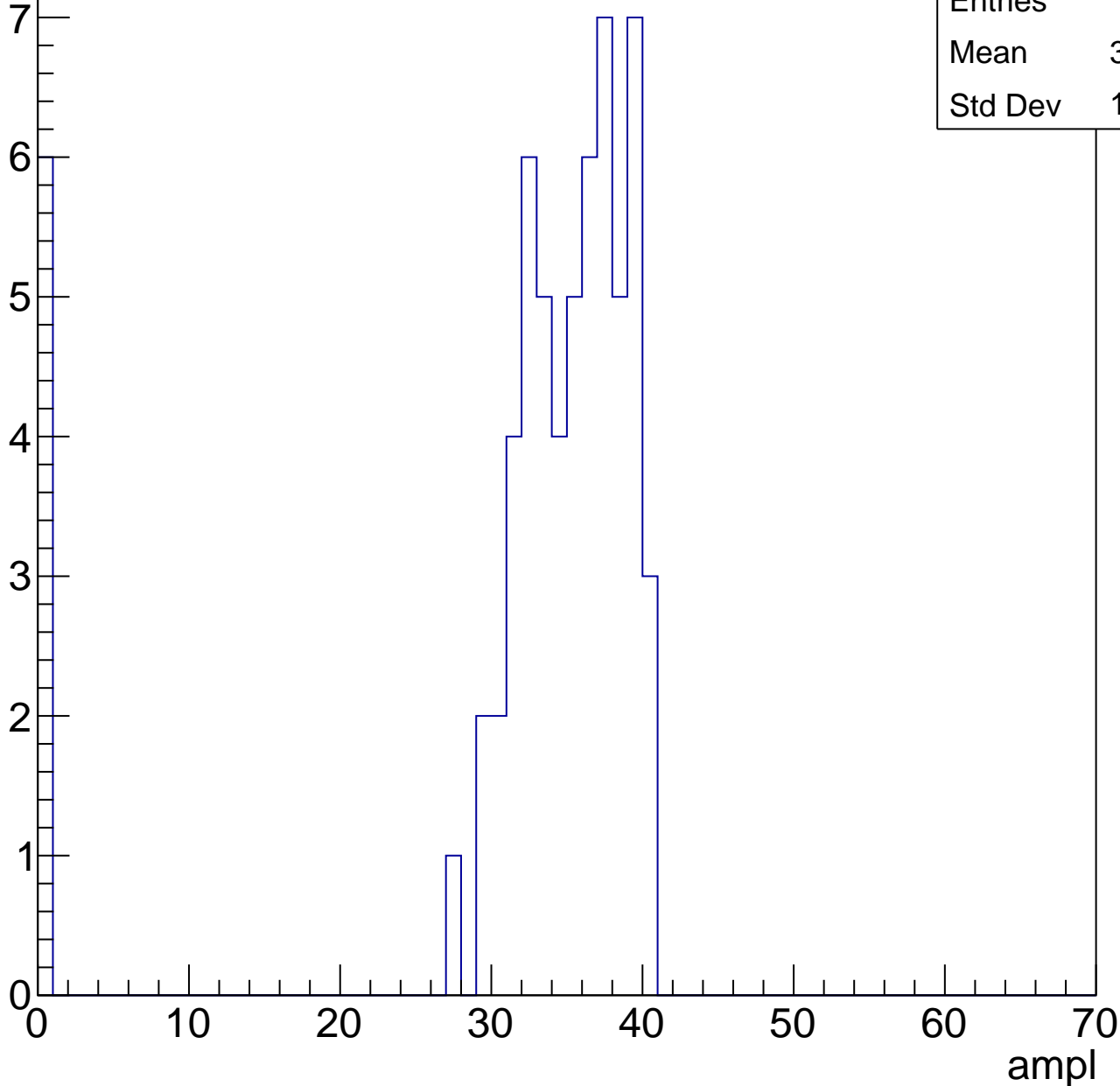


B1L103S, U23-ch109, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	63
Mean	31.67
Std Dev	10.72

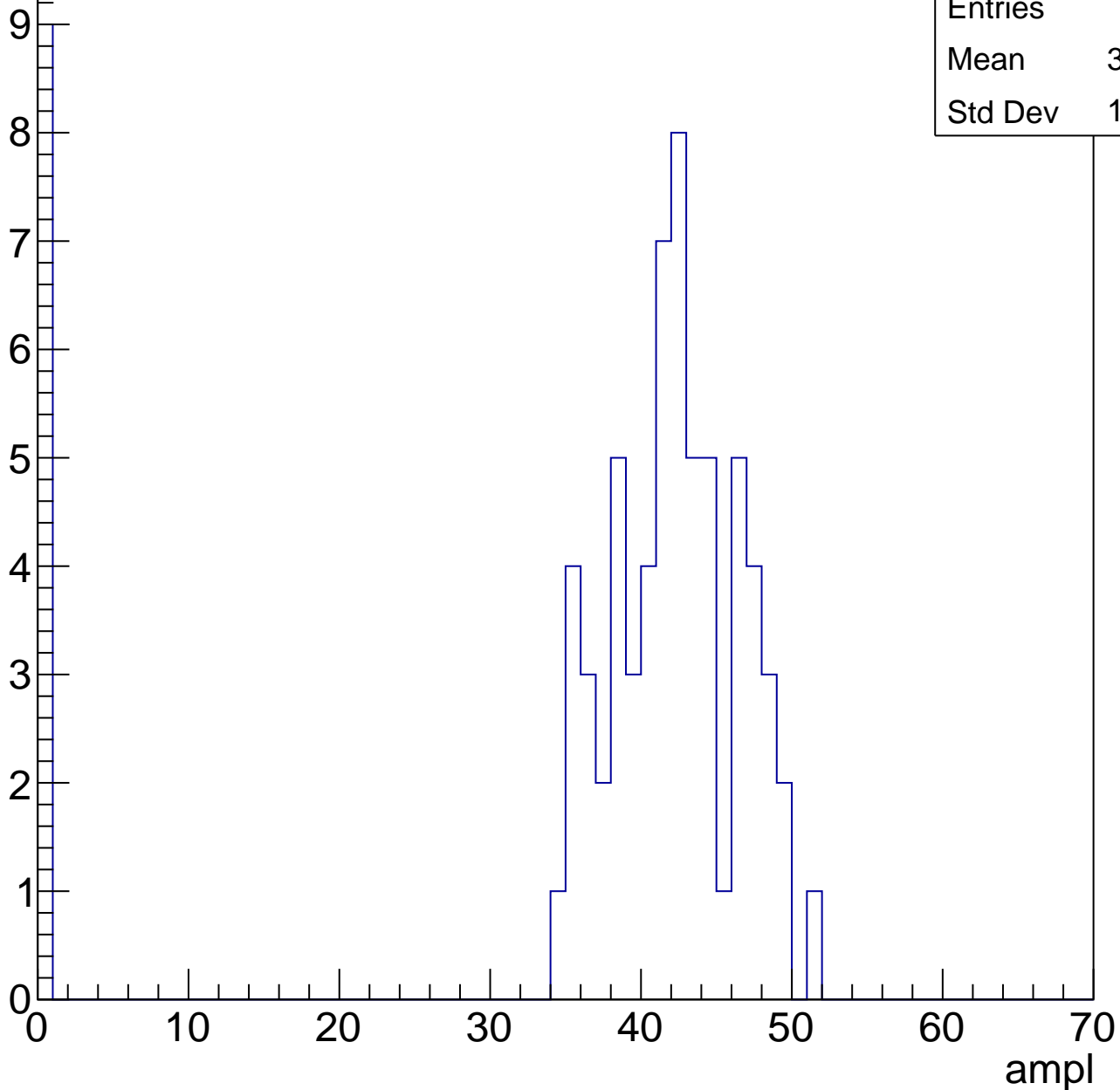


B1L103S, U23-ch109, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

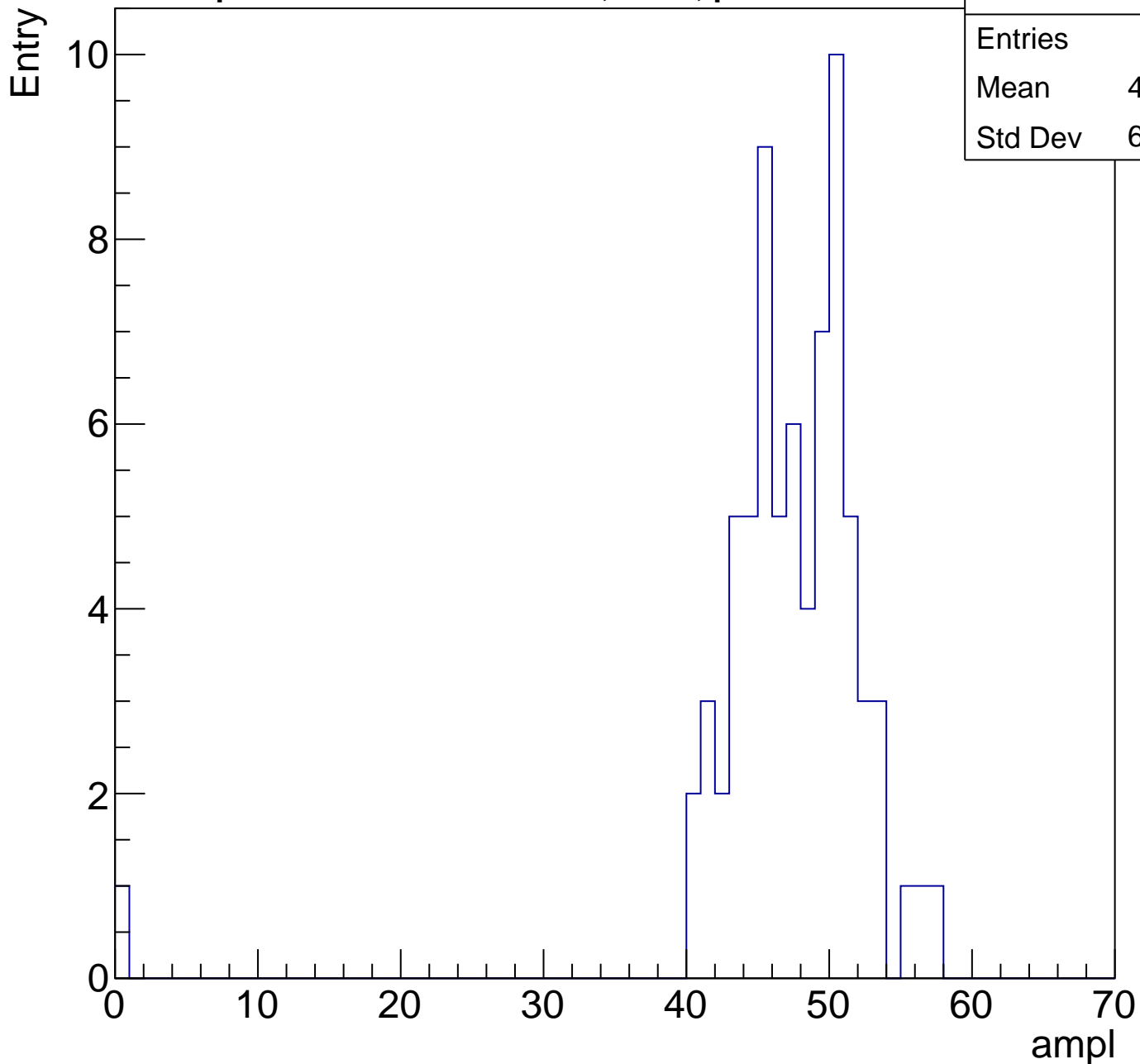
Entries	72
Mean	36.62
Std Dev	14.36



B1L103S, U23-ch109, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	73
Mean	46.74
Std Dev	6.679

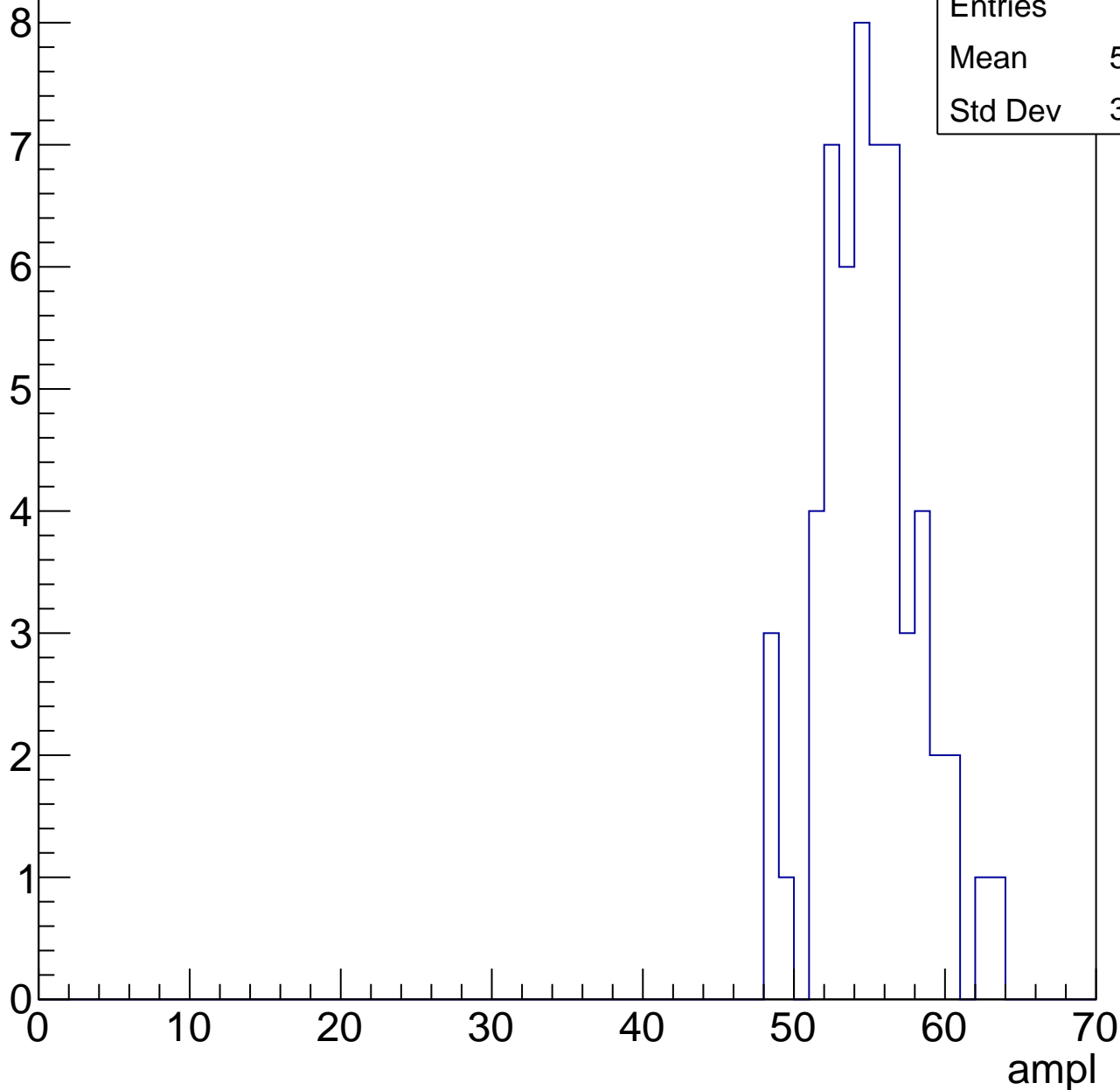


B1L103S, U23-ch109, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	56
Mean	54.54
Std Dev	3.218

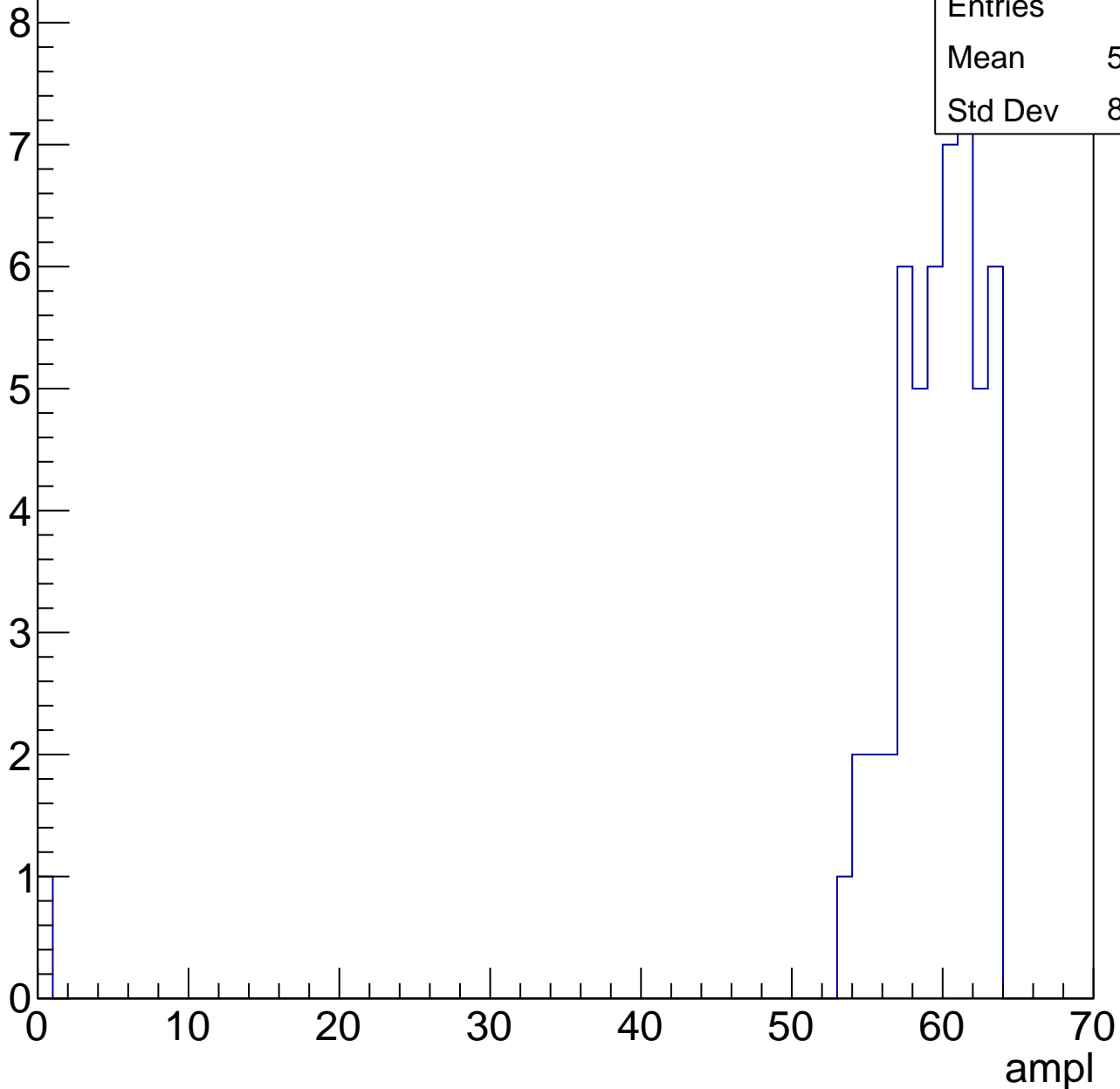


B1L103S, U23-ch109, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

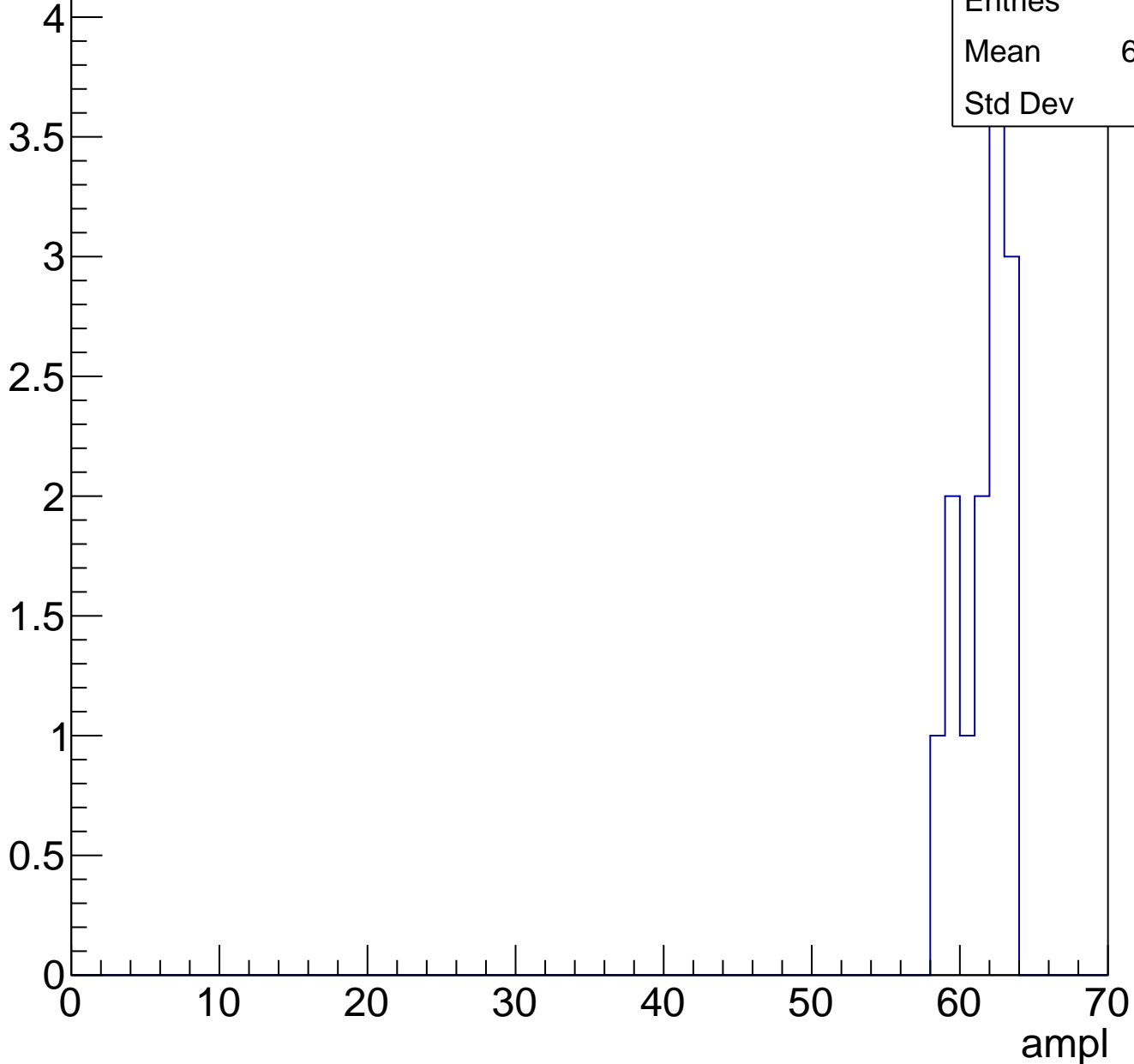
Entries	51
Mean	58.14
Std Dev	8.618



B1L103S, U23-ch109, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

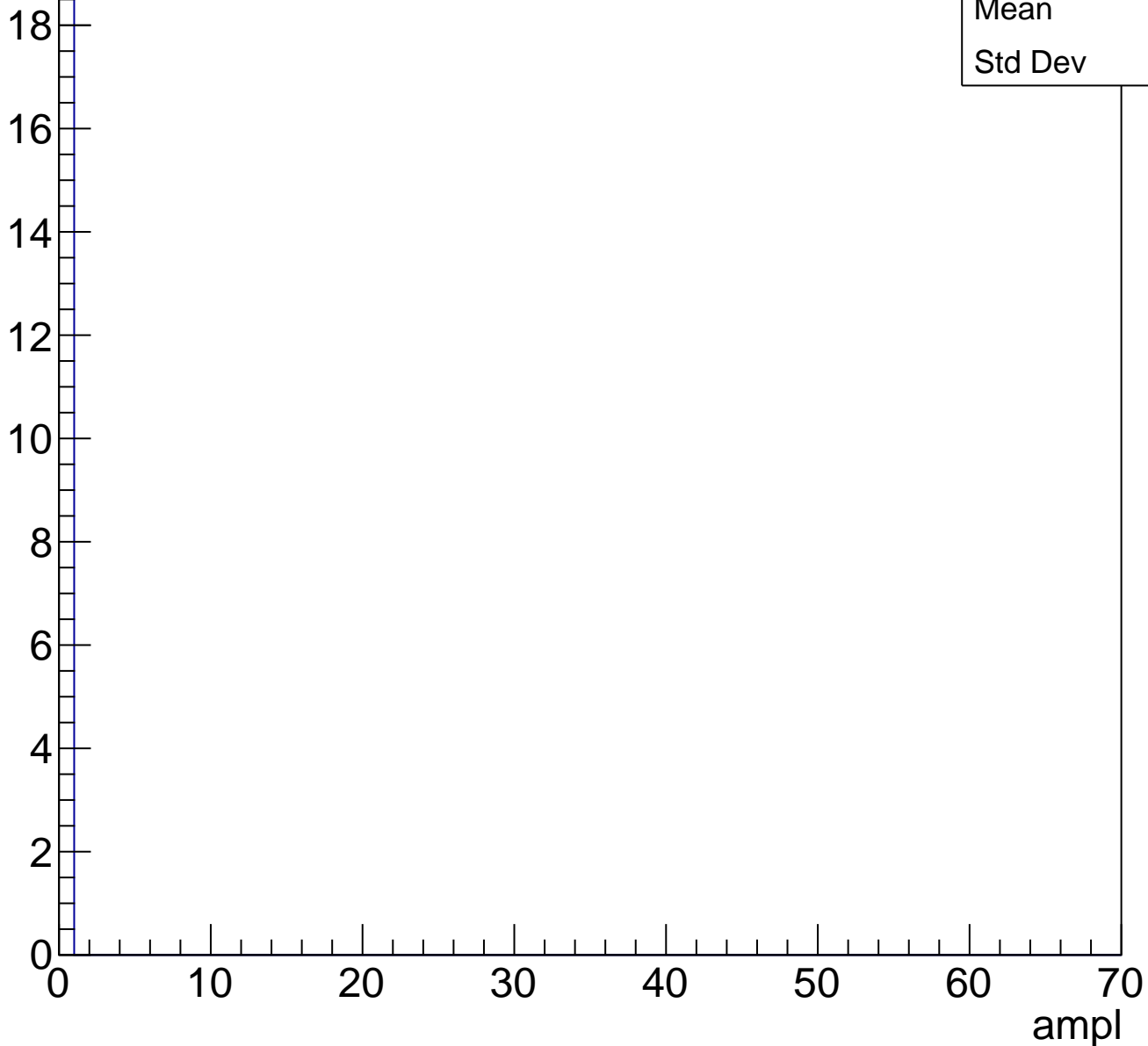


B1L103S, U23-ch109, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	0
Std Dev	0

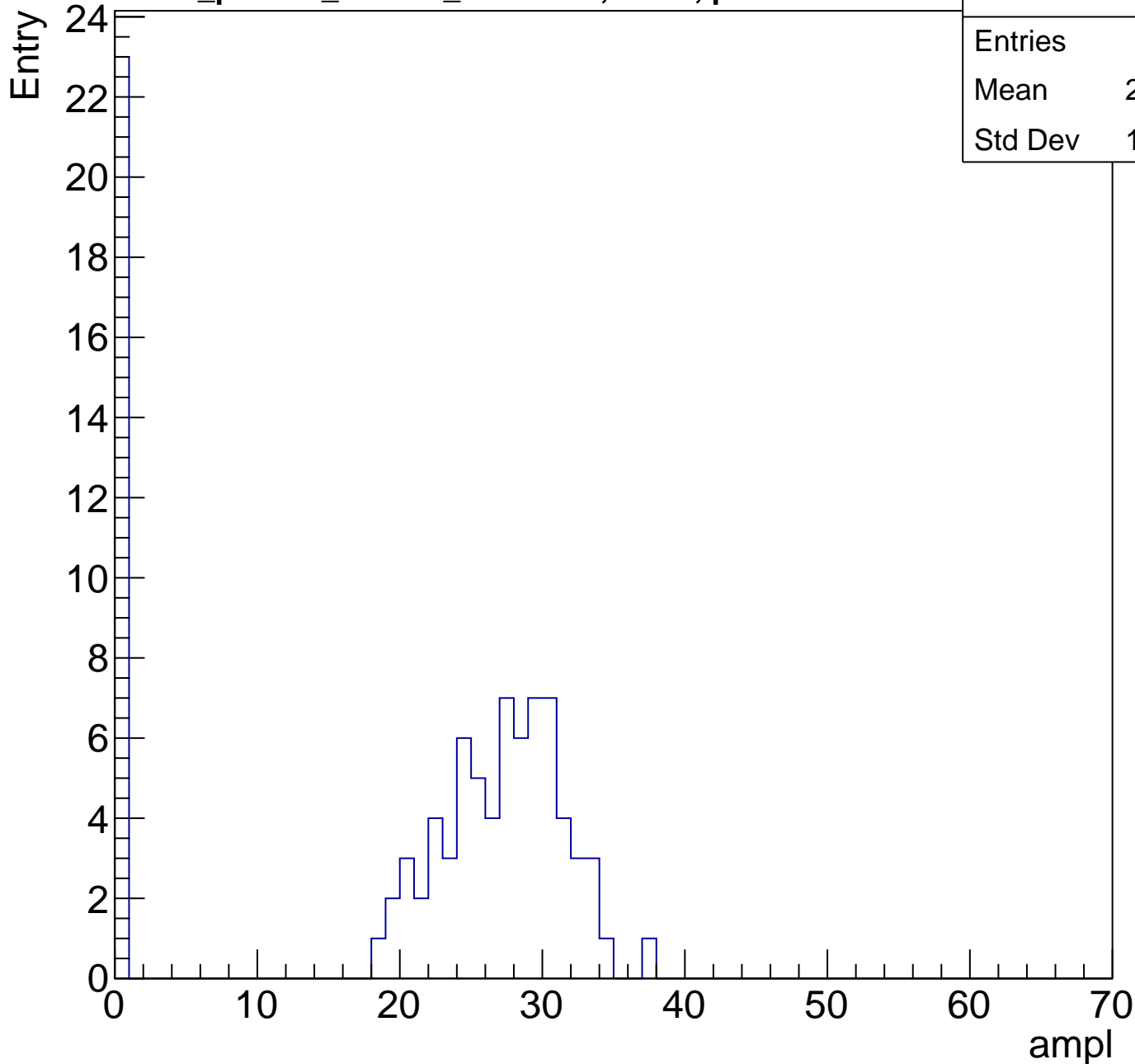
Entry



B1L103S, U23-ch110, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	92
Mean	20.09
Std Dev	12.12



B1L103S, U23-ch110, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	71
Mean	27.18
Std Dev	13.39

Entry

12

10

8

6

4

2

0

0

10

20

30

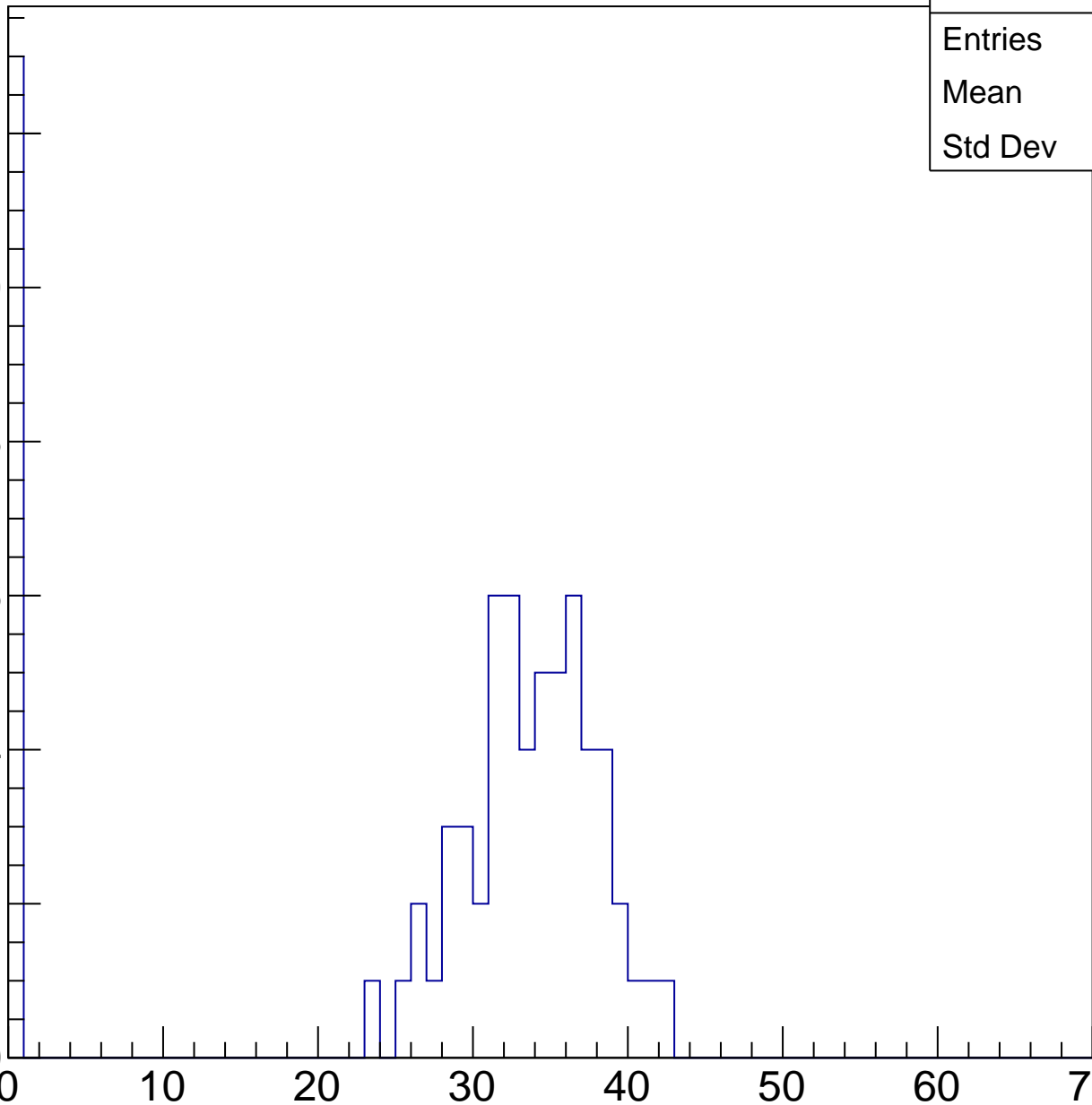
40

50

60

70

ampl

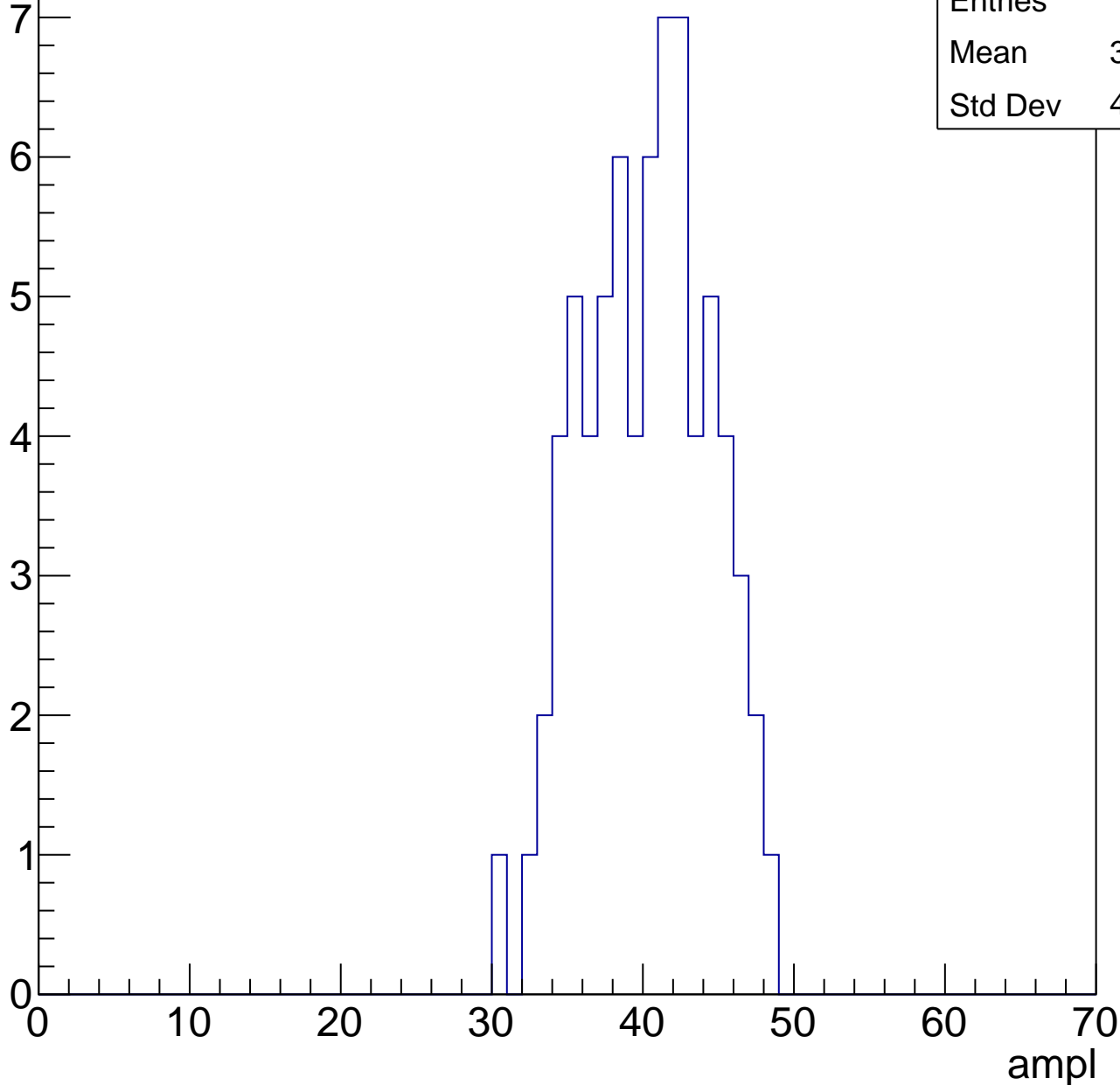


B1L103S, U23-ch110, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	39.79
Std Dev	4.087

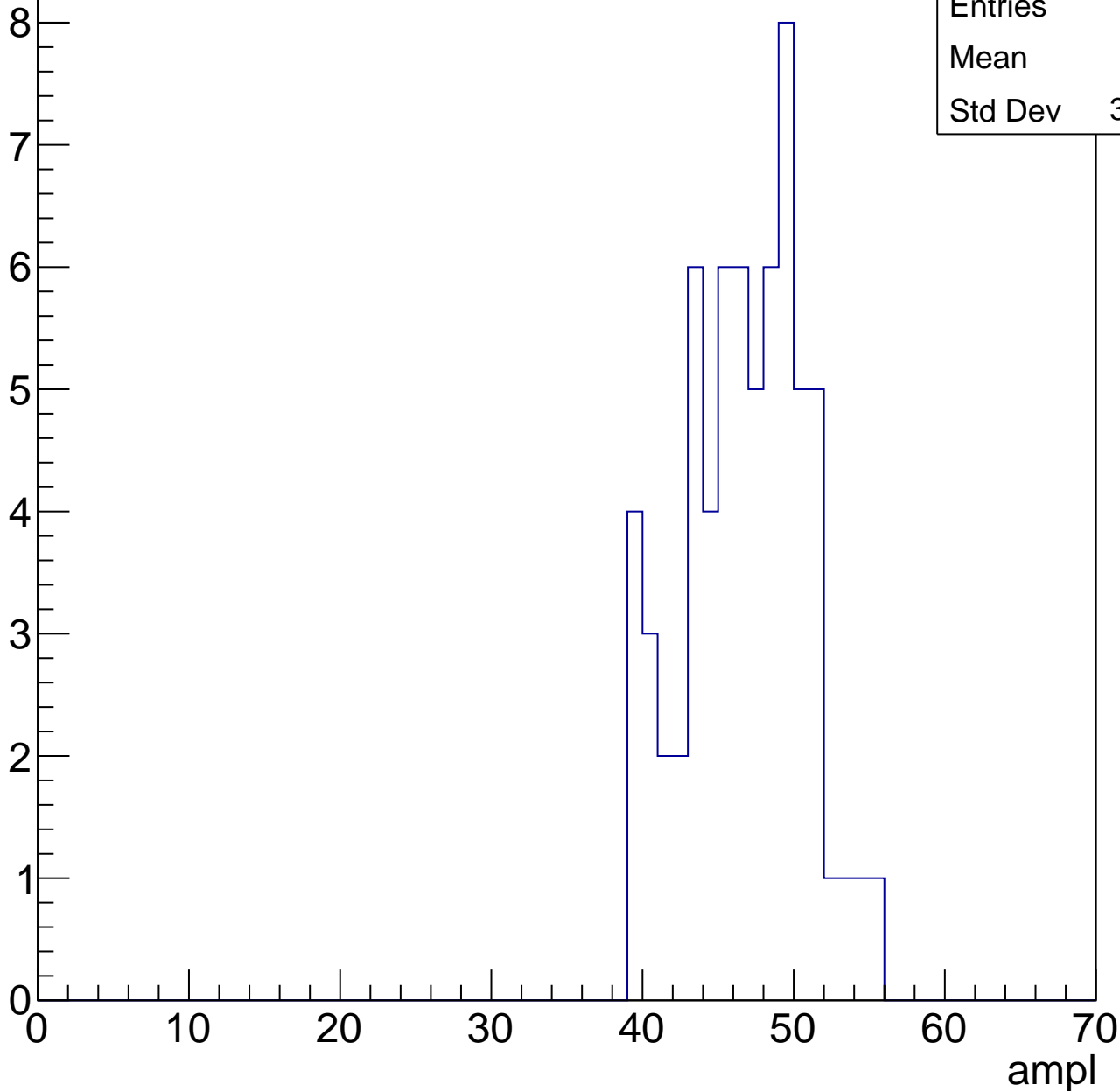


B1L103S, U23-ch110, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	46.3
Std Dev	3.877

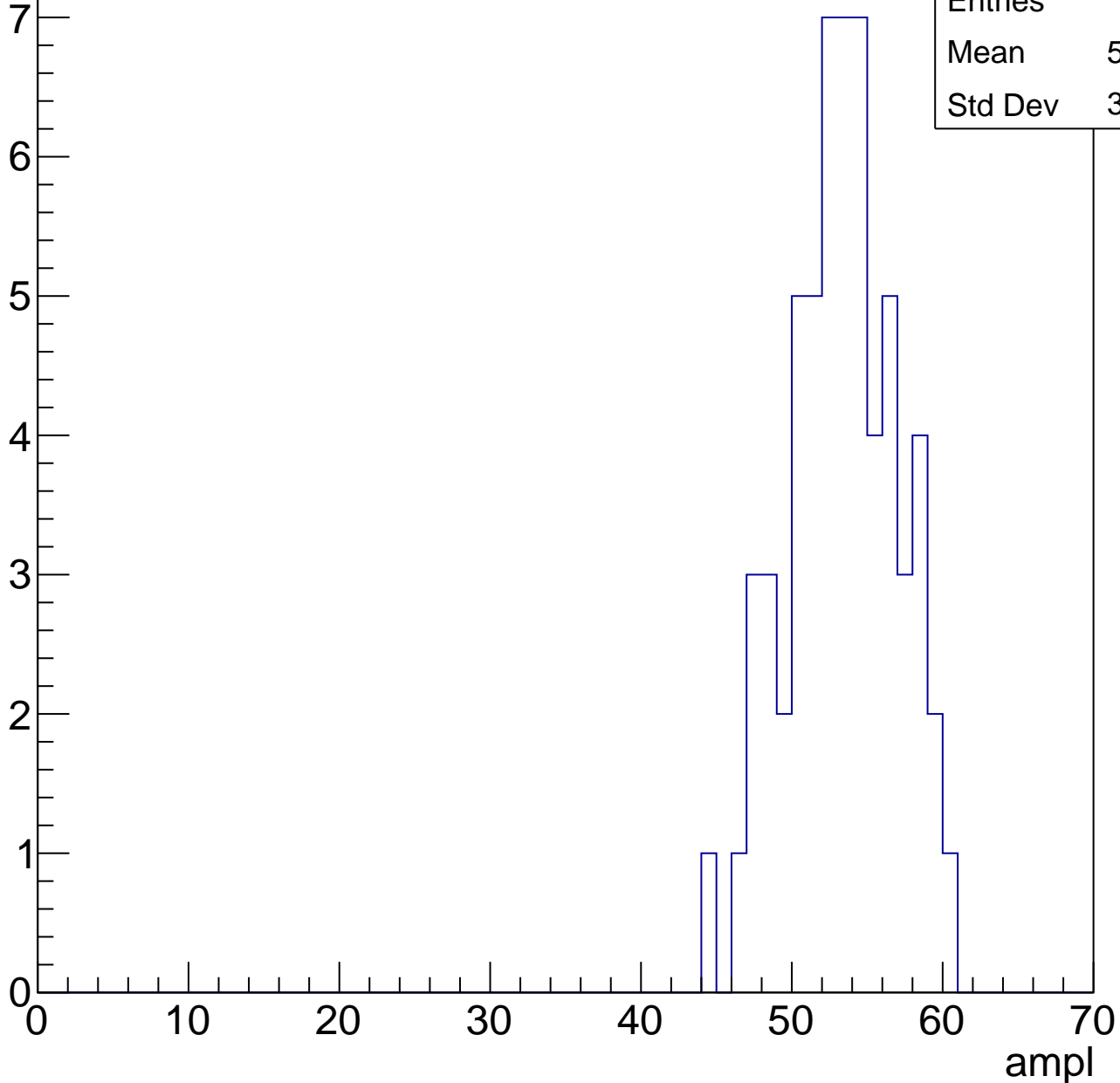


B1L103S, U23-ch110, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	52.87
Std Dev	3.542

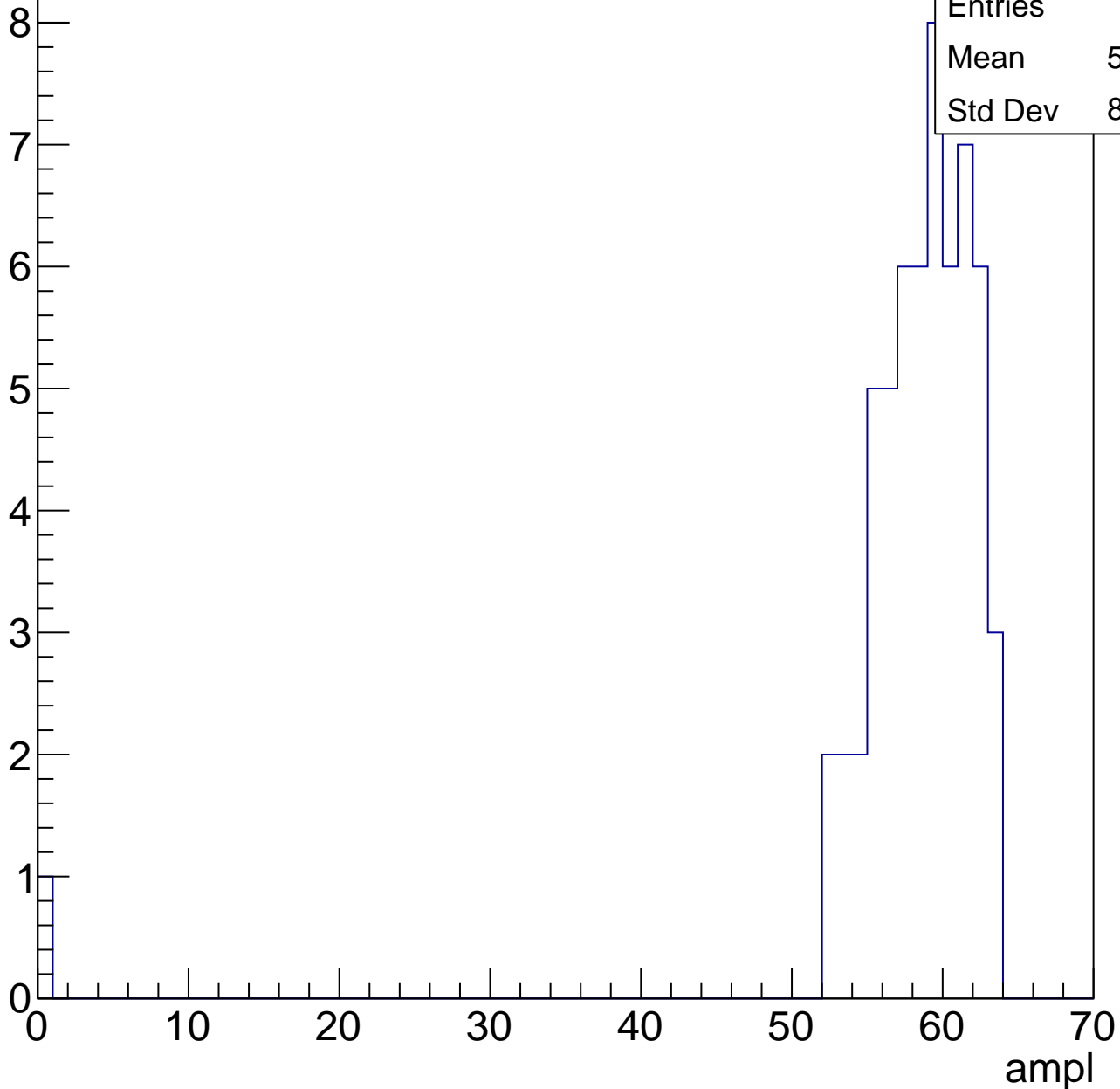


B1L103S, U23-ch110, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	57.34
Std Dev	8.056

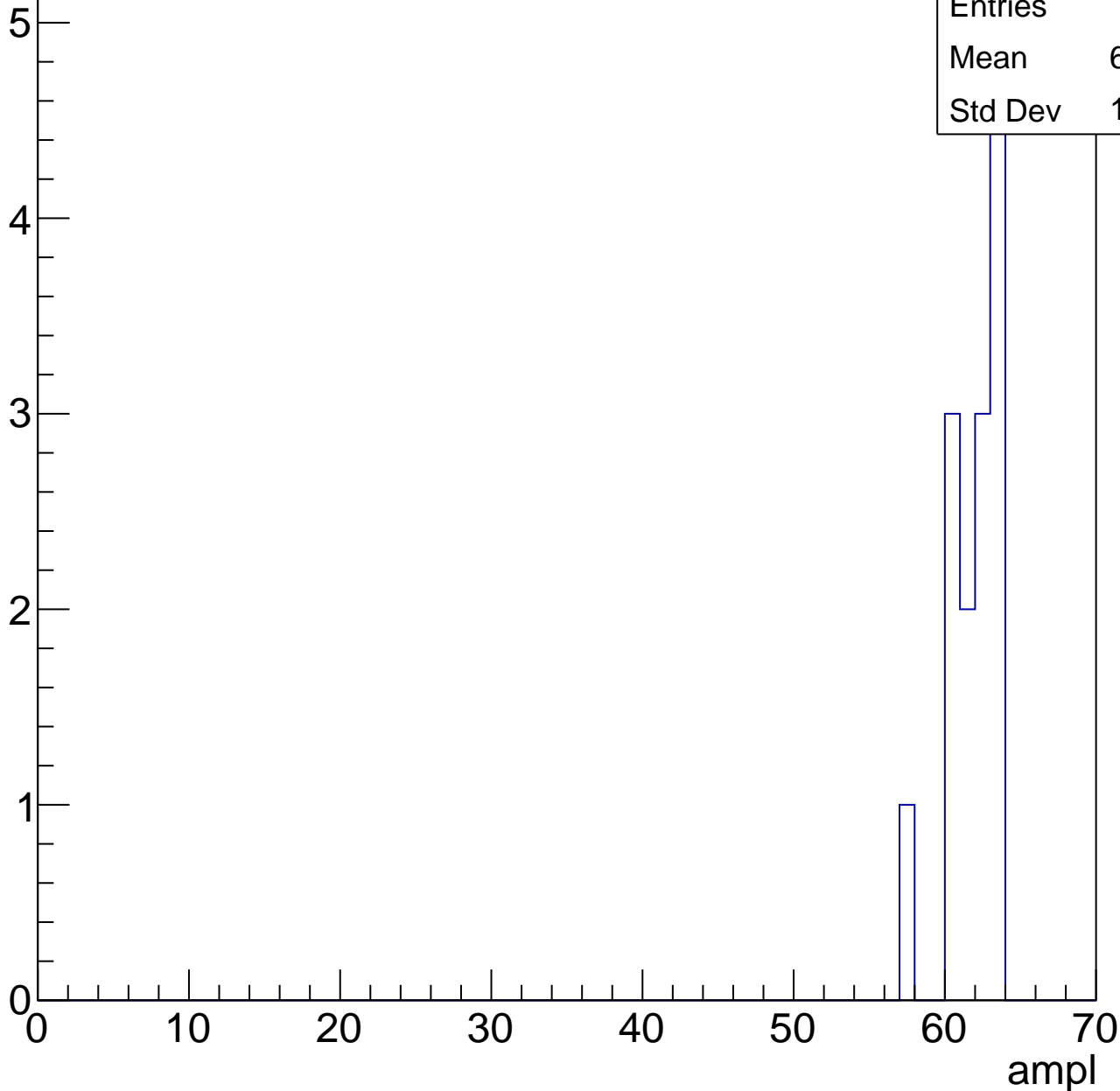


B1L103S, U23-ch110, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	14
Mean	61.43
Std Dev	1.678

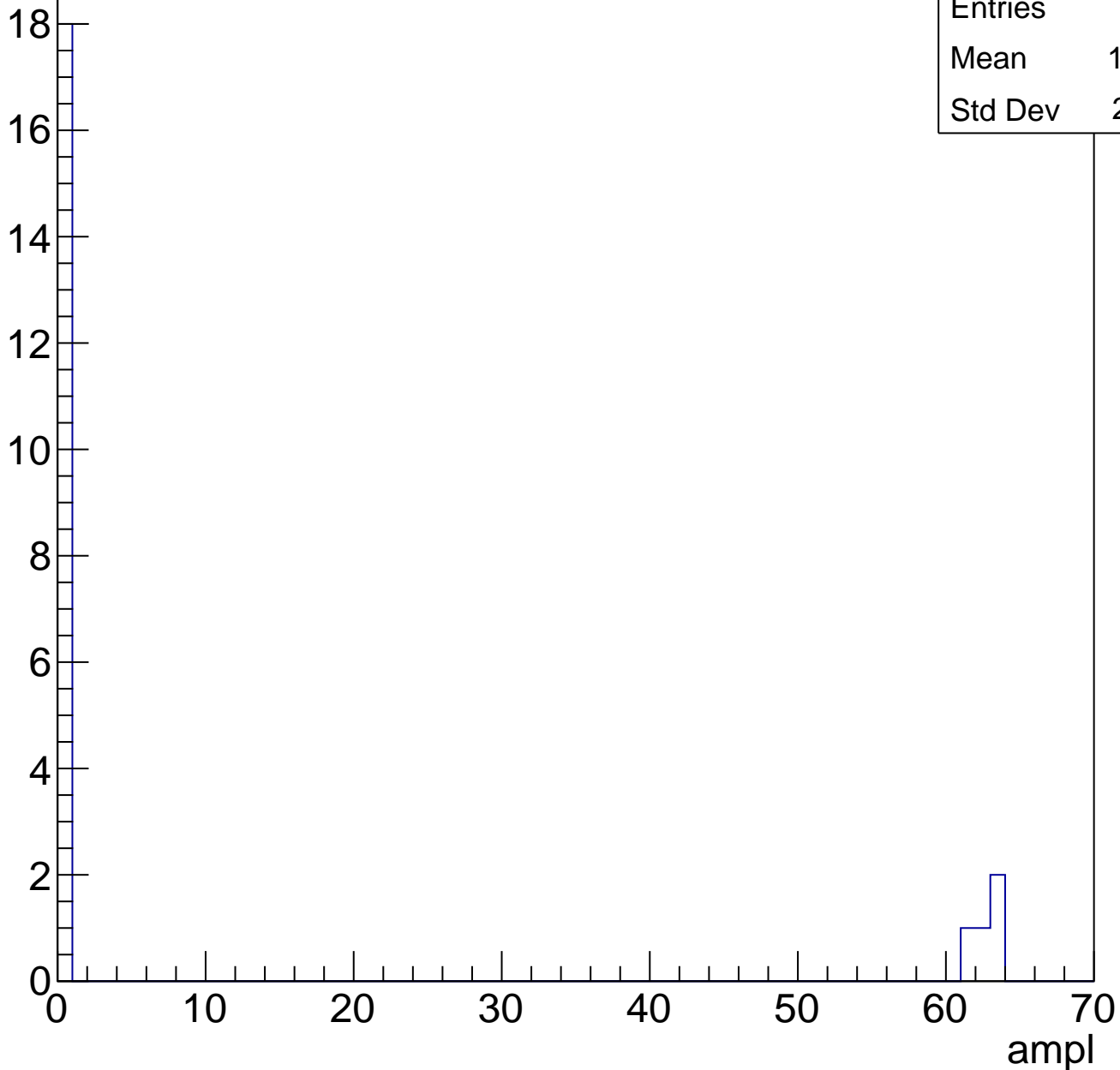


B1L103S, U23-ch110, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	22
Mean	11.32
Std Dev	24.01

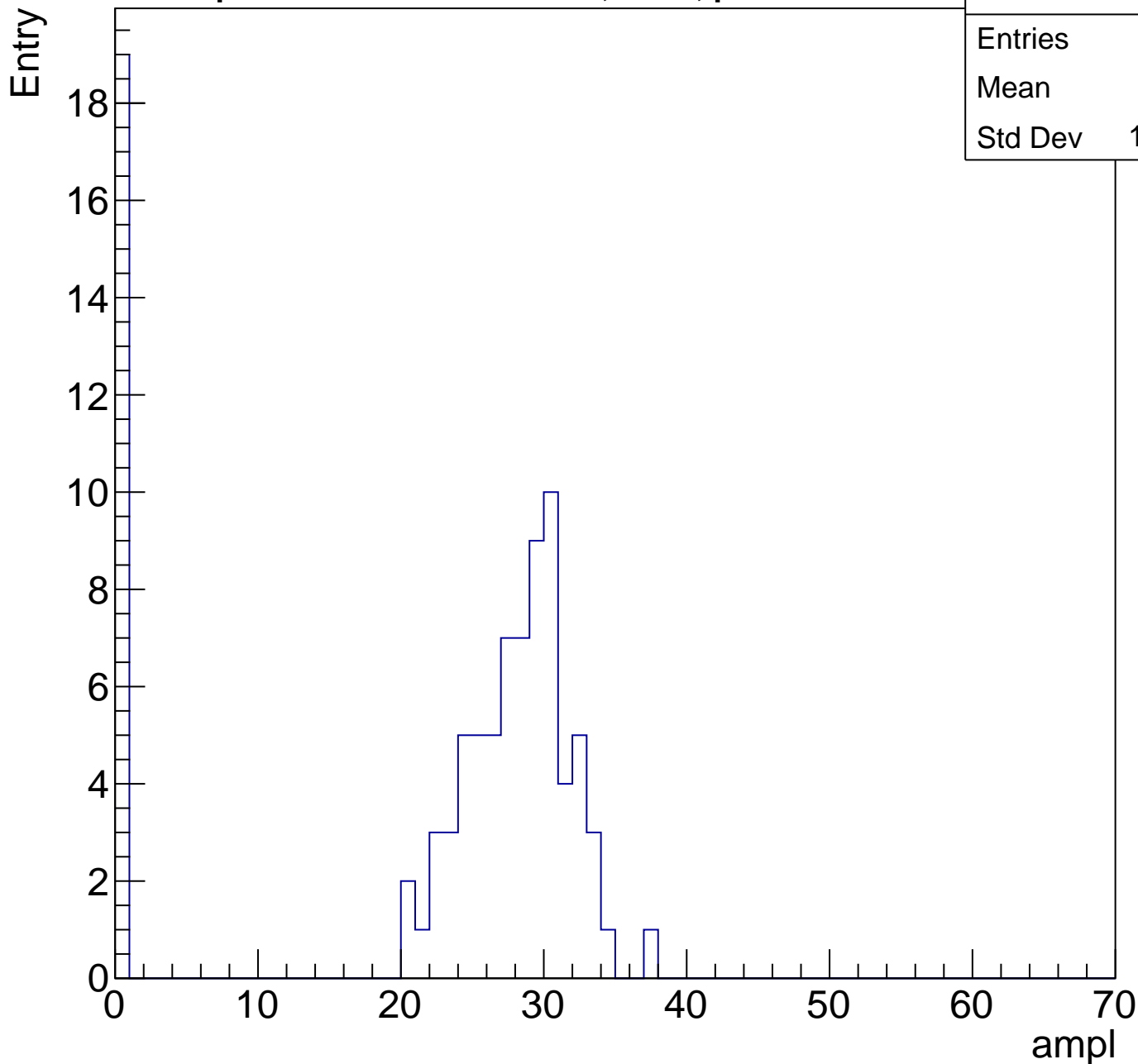
Entry



B1L103S, U23-ch111, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	90
Mean	21.9
Std Dev	11.75



B1L103S, U23-ch111, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	81
Mean	30.86
Std Dev	12.53

Entry

10

8

6

4

2

0

0

10

20

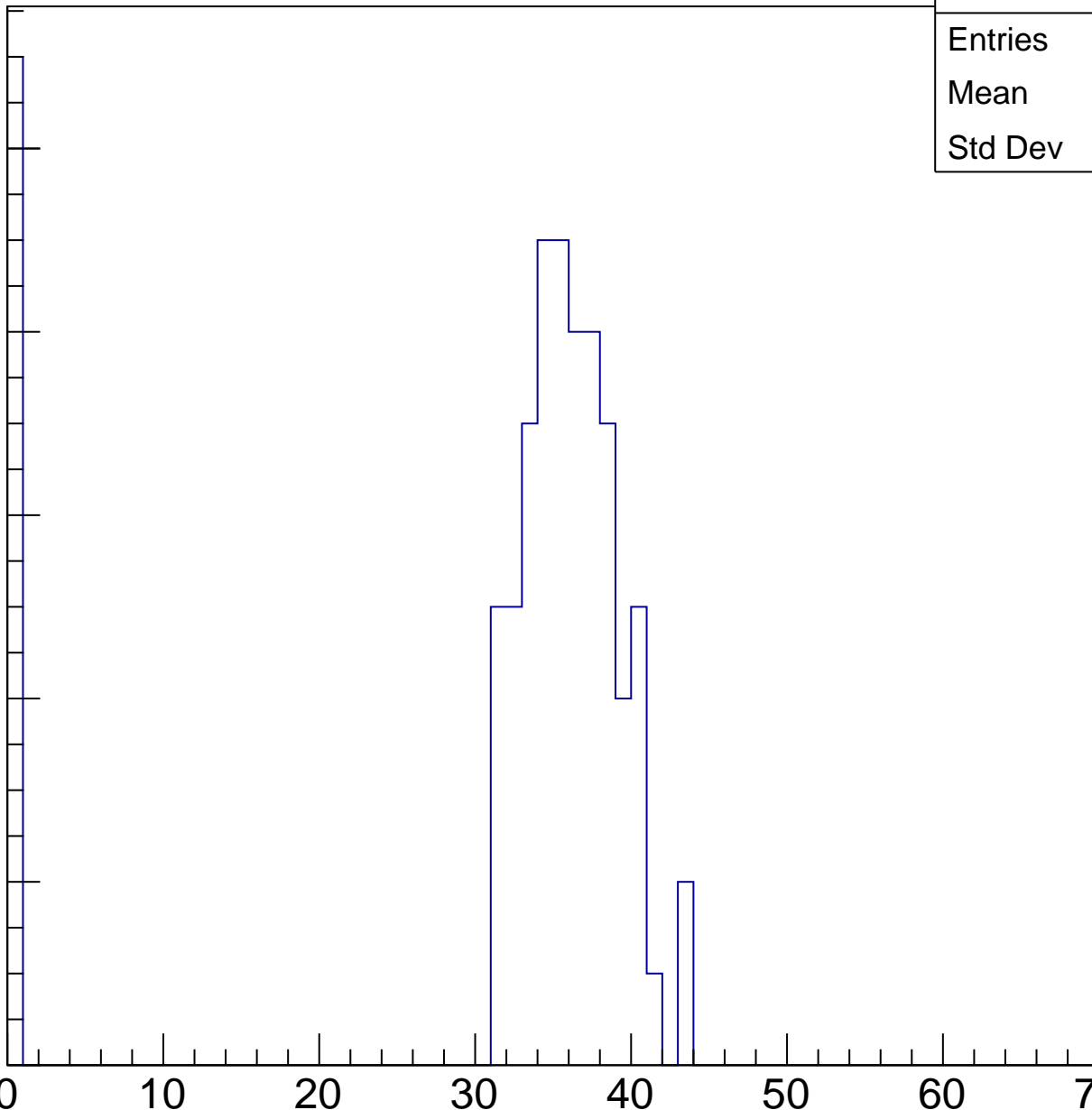
30

40

50

60

ampl

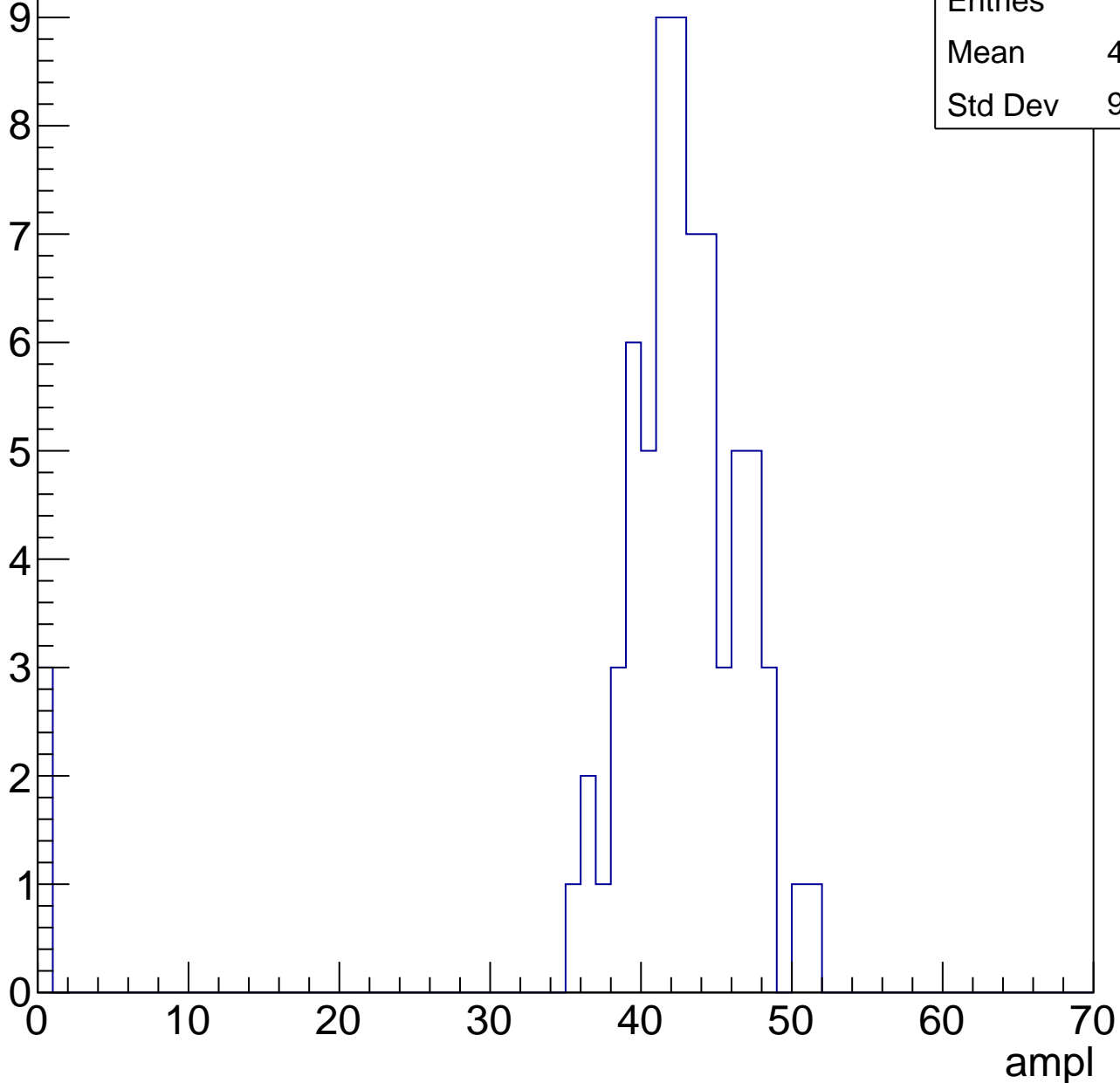


B1L103S, U23-ch111, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	40.75
Std Dev	9.175

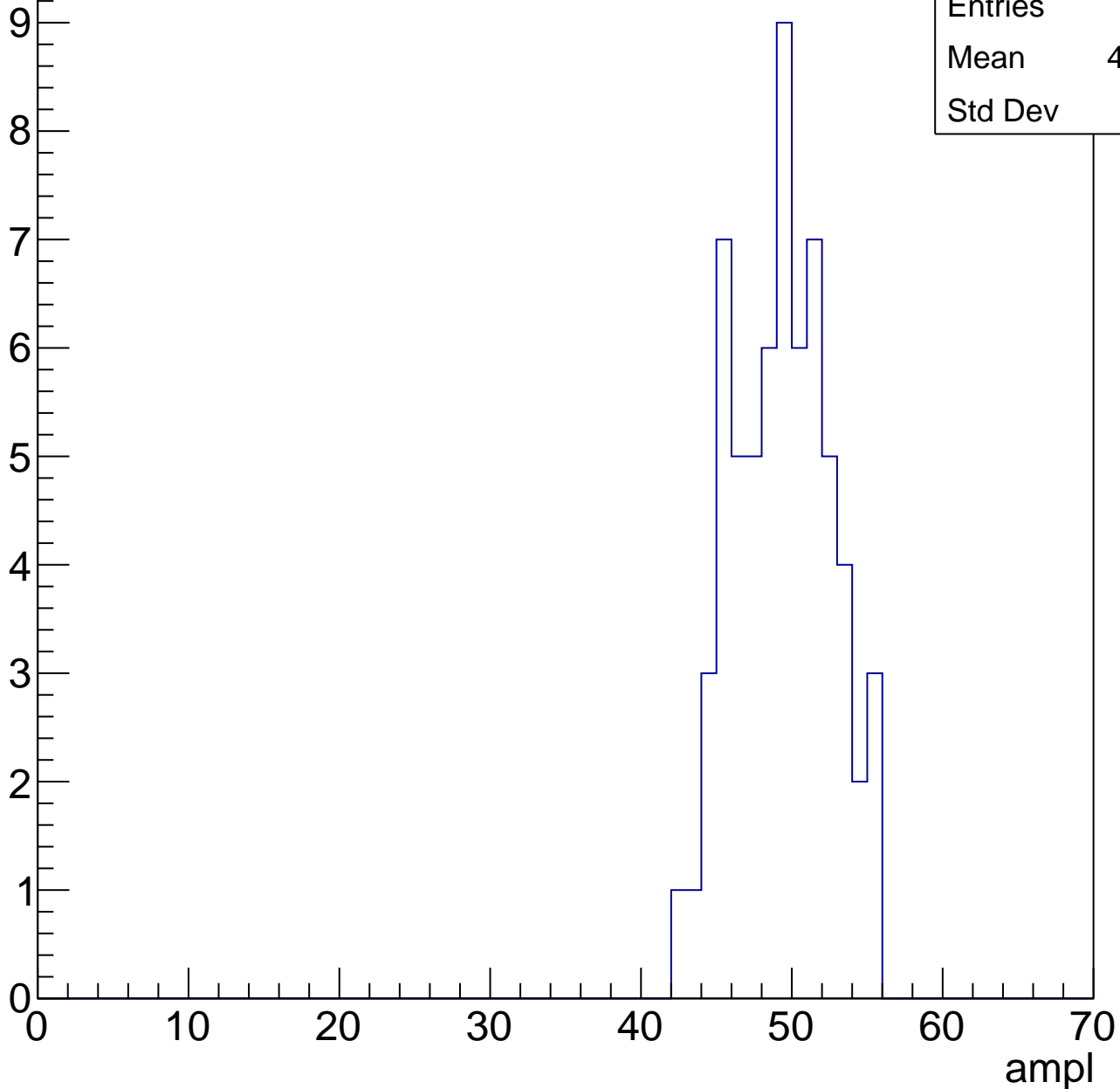


B1L103S, U23-ch111, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	48.88
Std Dev	3.17

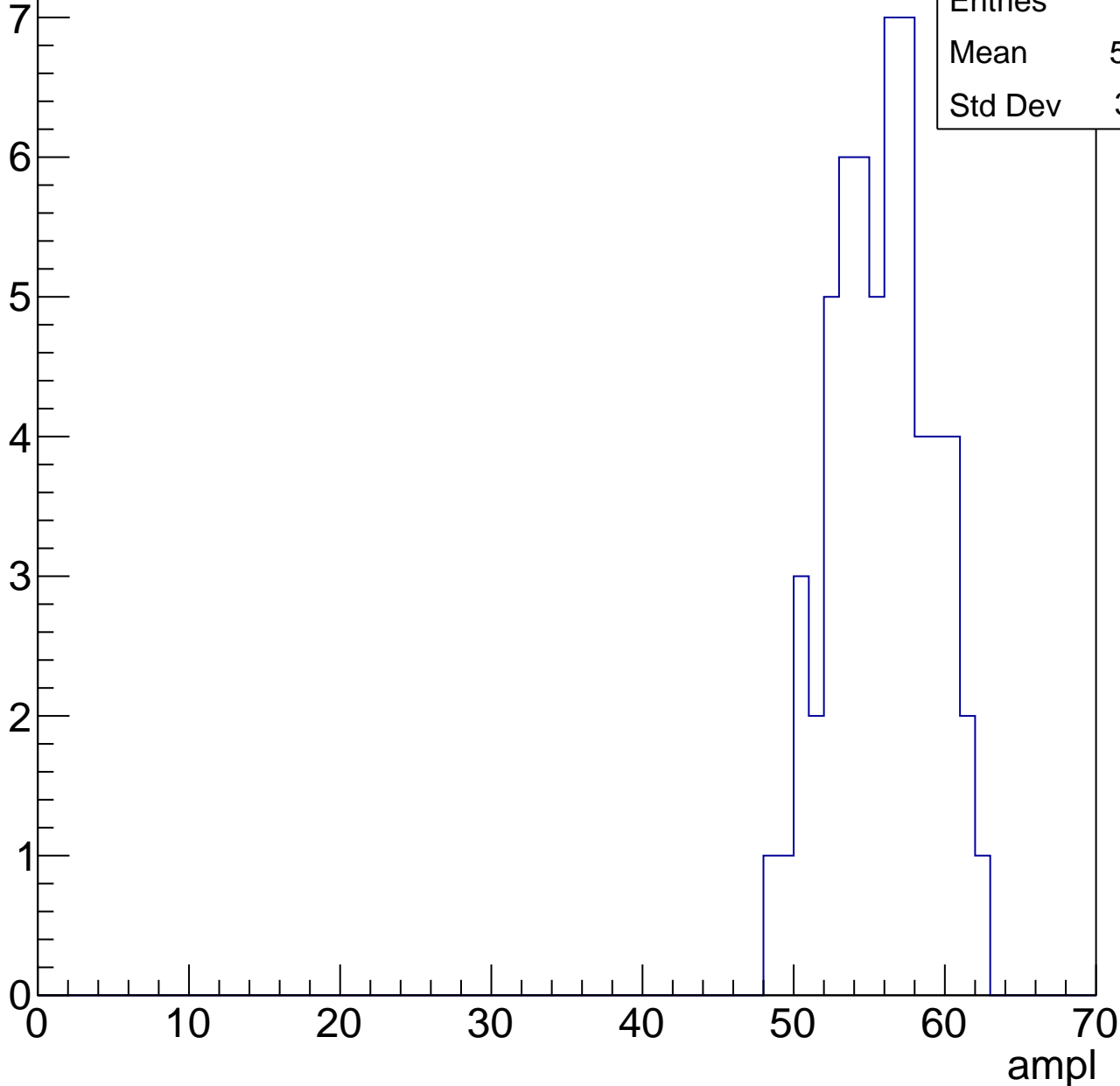


B1L103S, U23-ch111, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

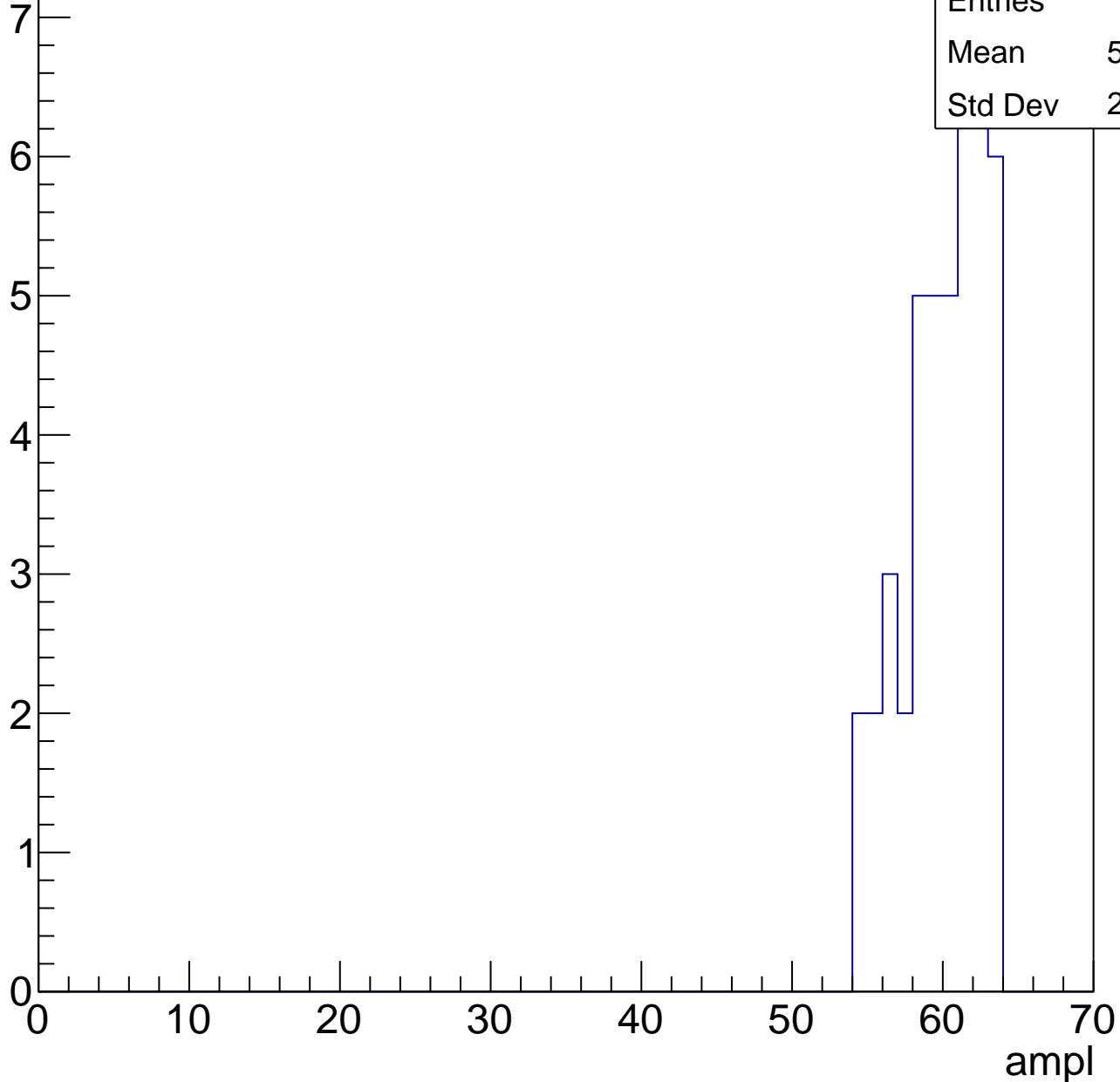
Entries	58
Mean	55.33
Std Dev	3.261



B1L103S, U23-ch111, adc5

calib_packv5_041523_1651.root, FC#0, port C2

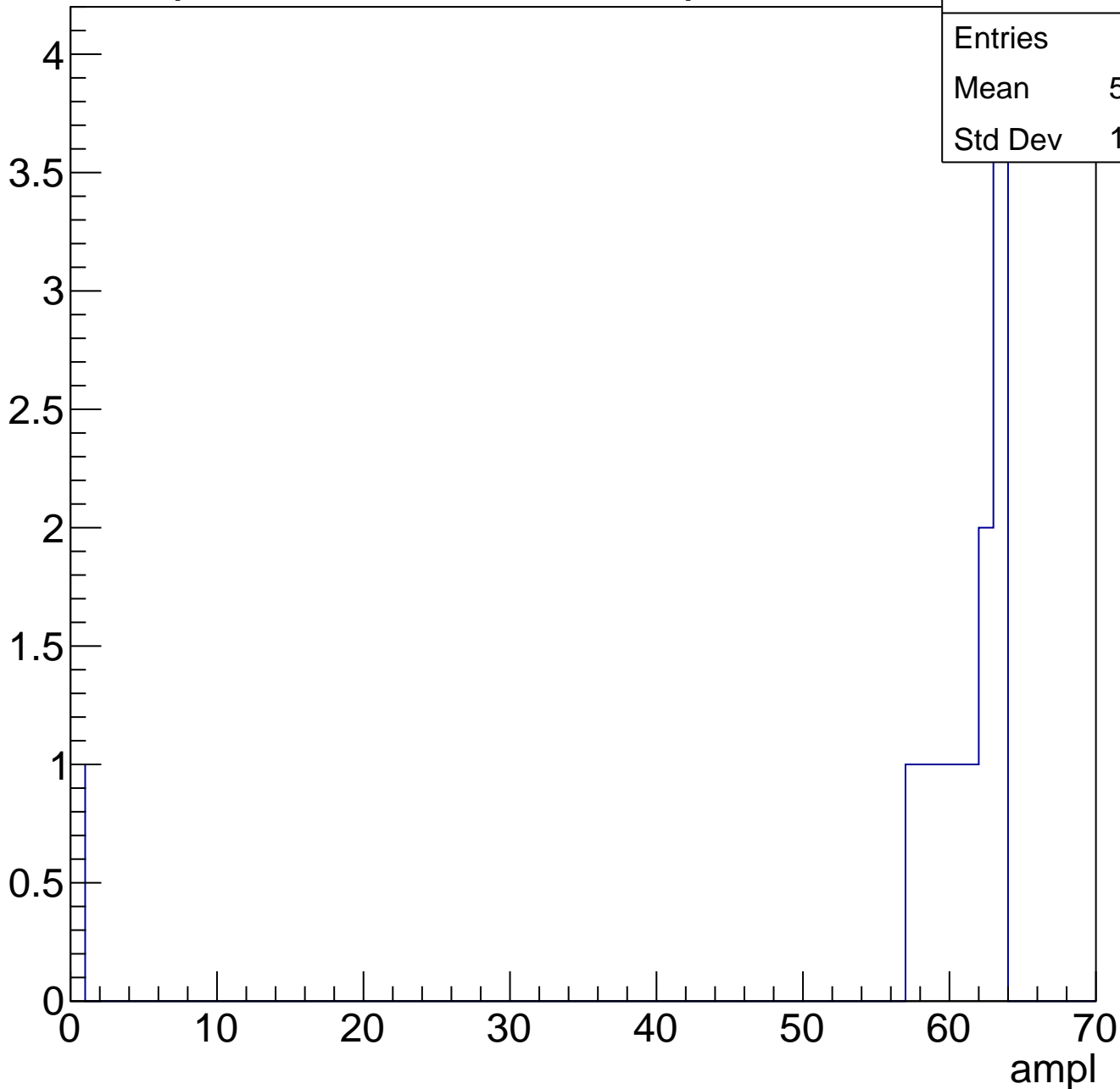
Entry



B1L103S, U23-ch111, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch111, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

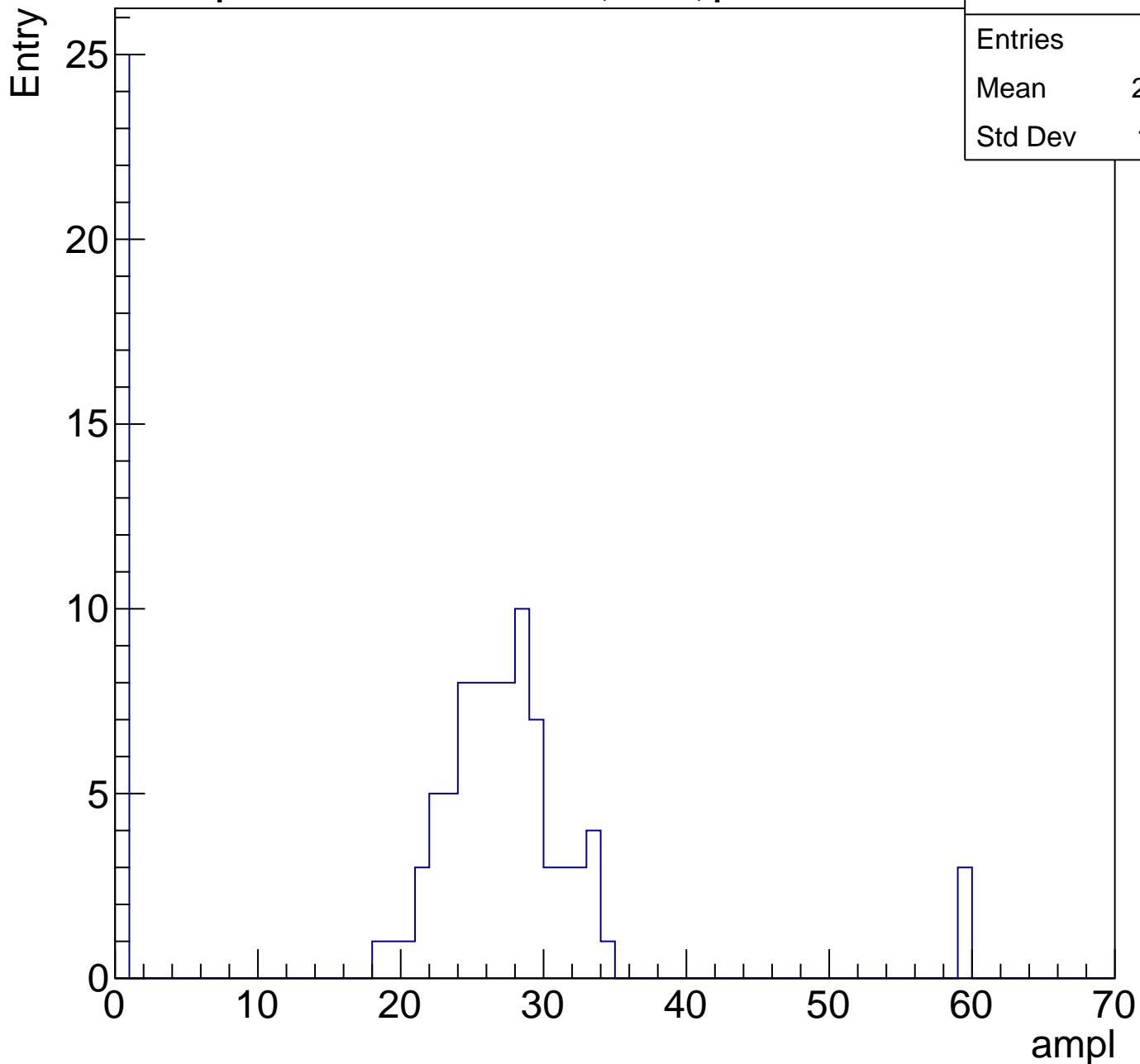
ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U23-ch112, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	107
Mean	21.18
Std Dev	13.21

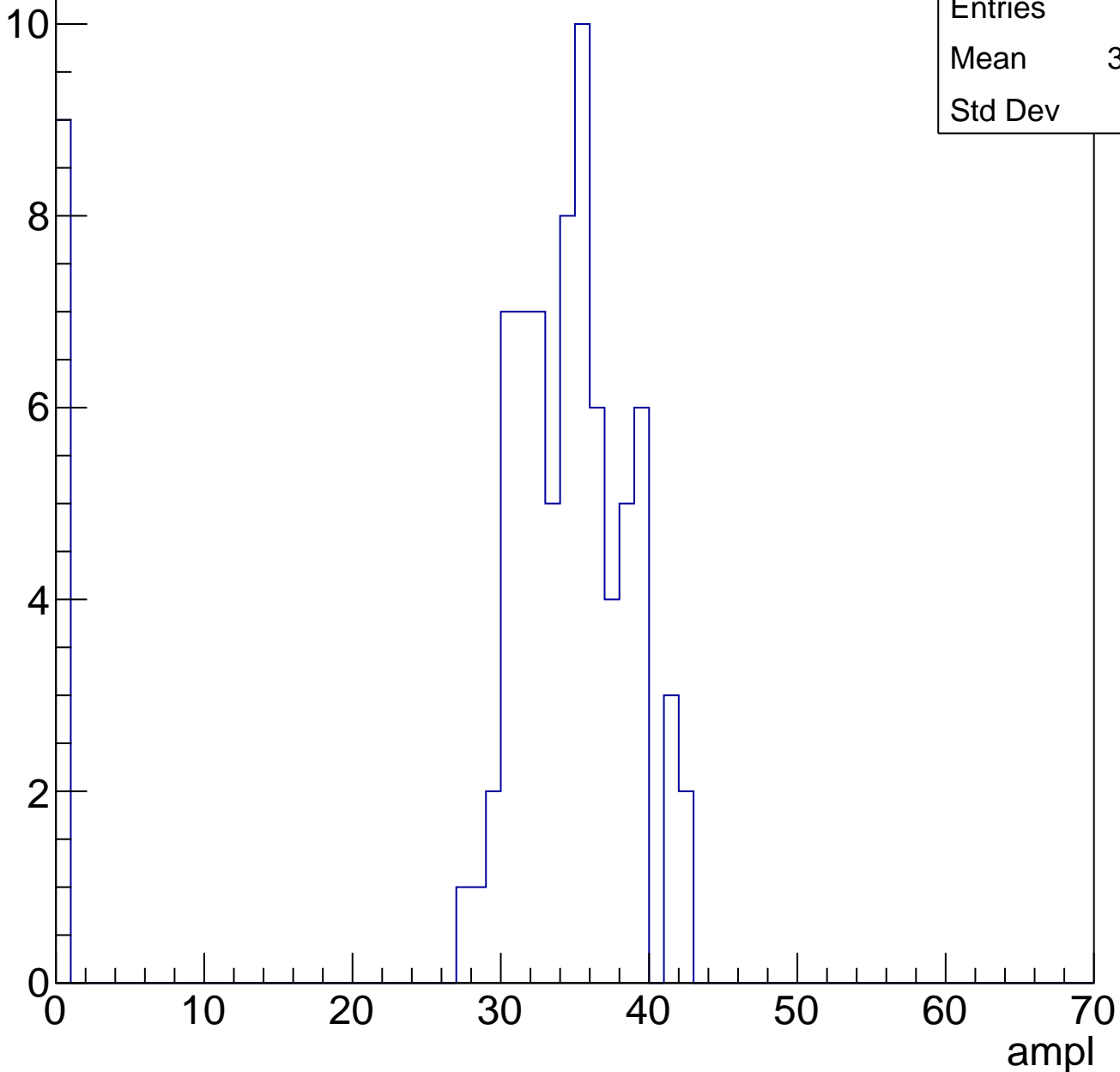


B1L103S, U23-ch112, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	83
Mean	30.67
Std Dev	11.2

Entry

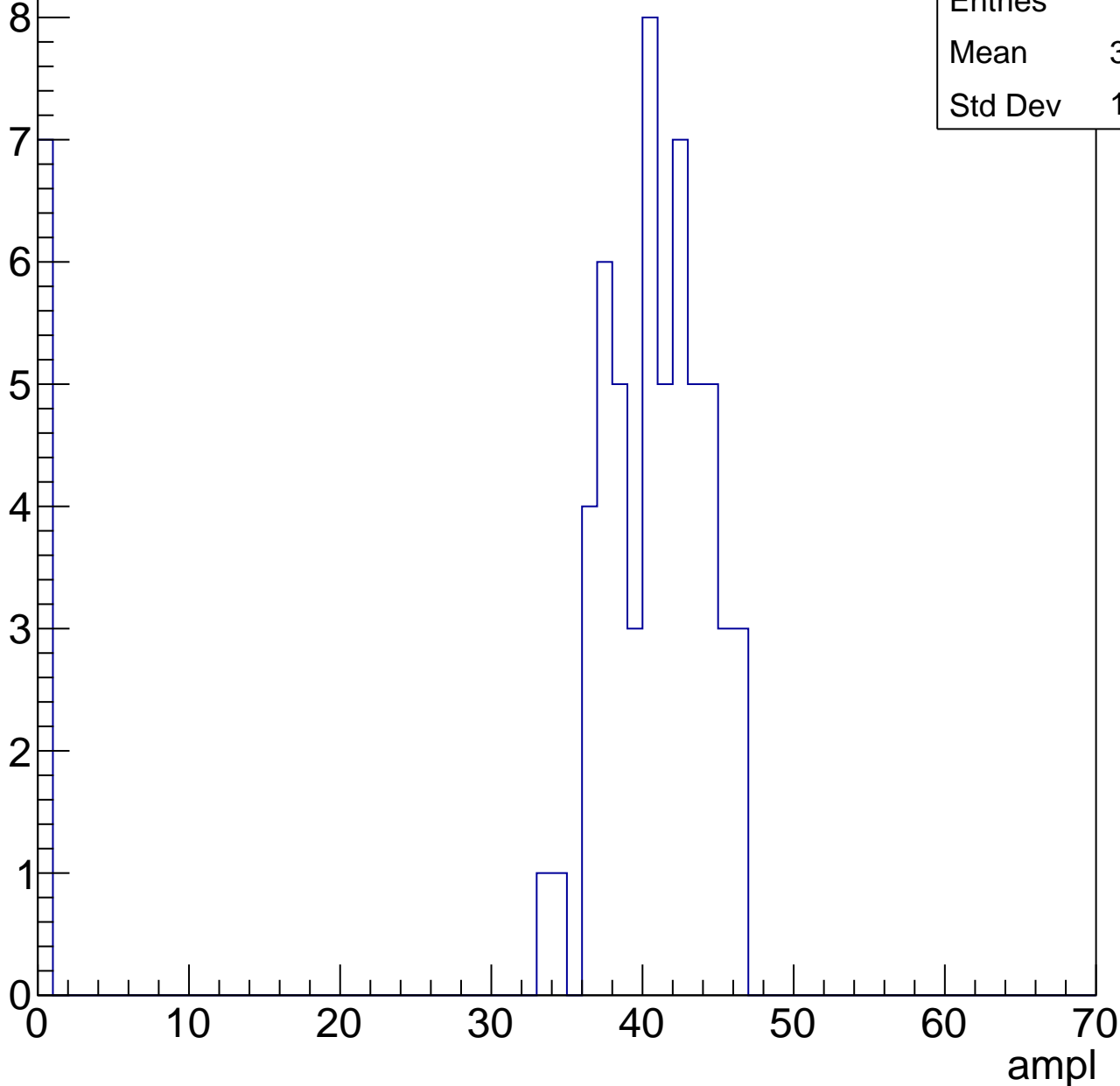


B1L103S, U23-ch112, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

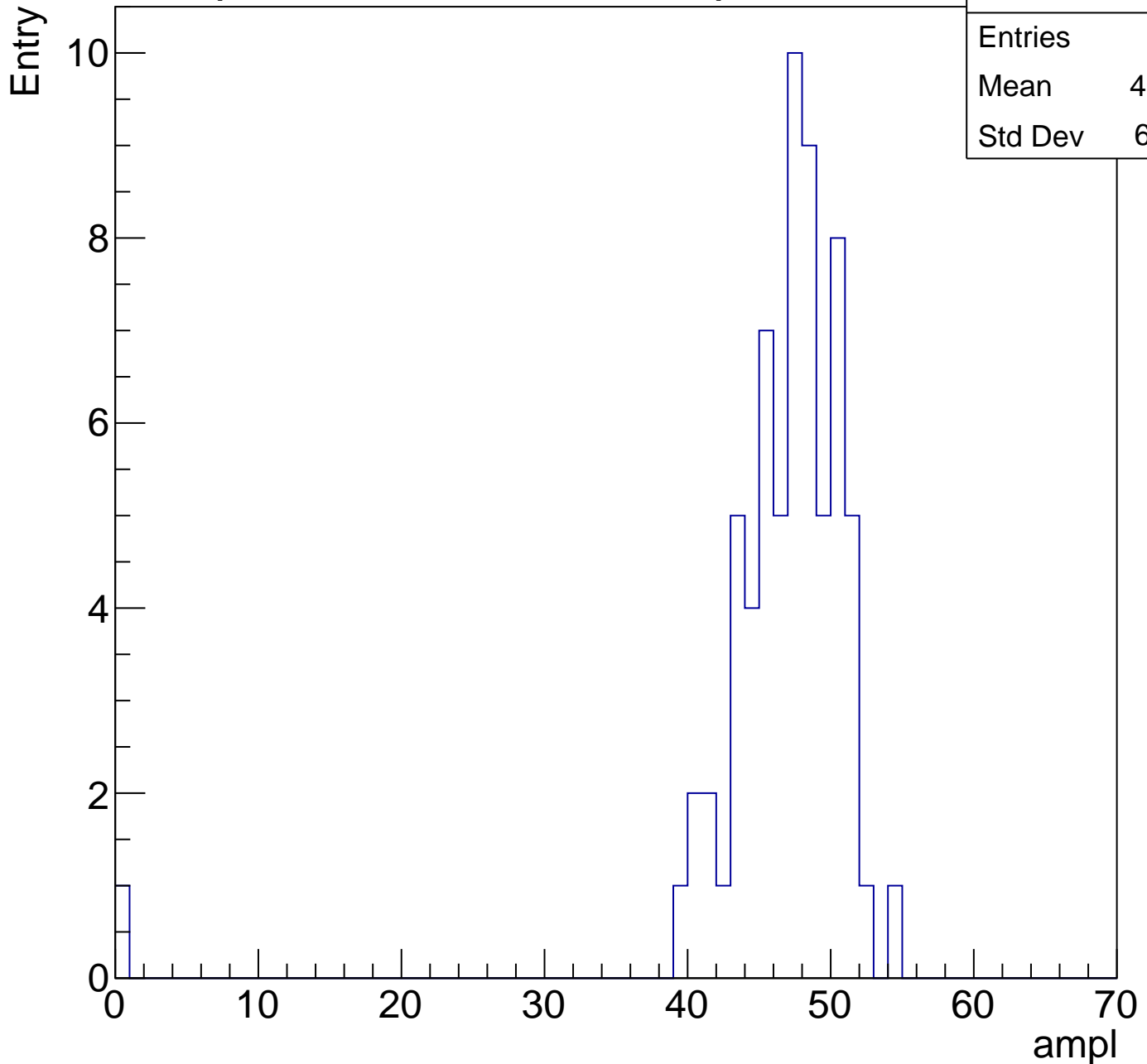
Entries	63
Mean	35.98
Std Dev	13.06



B1L103S, U23-ch112, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	67
Mean	46.07
Std Dev	6.481

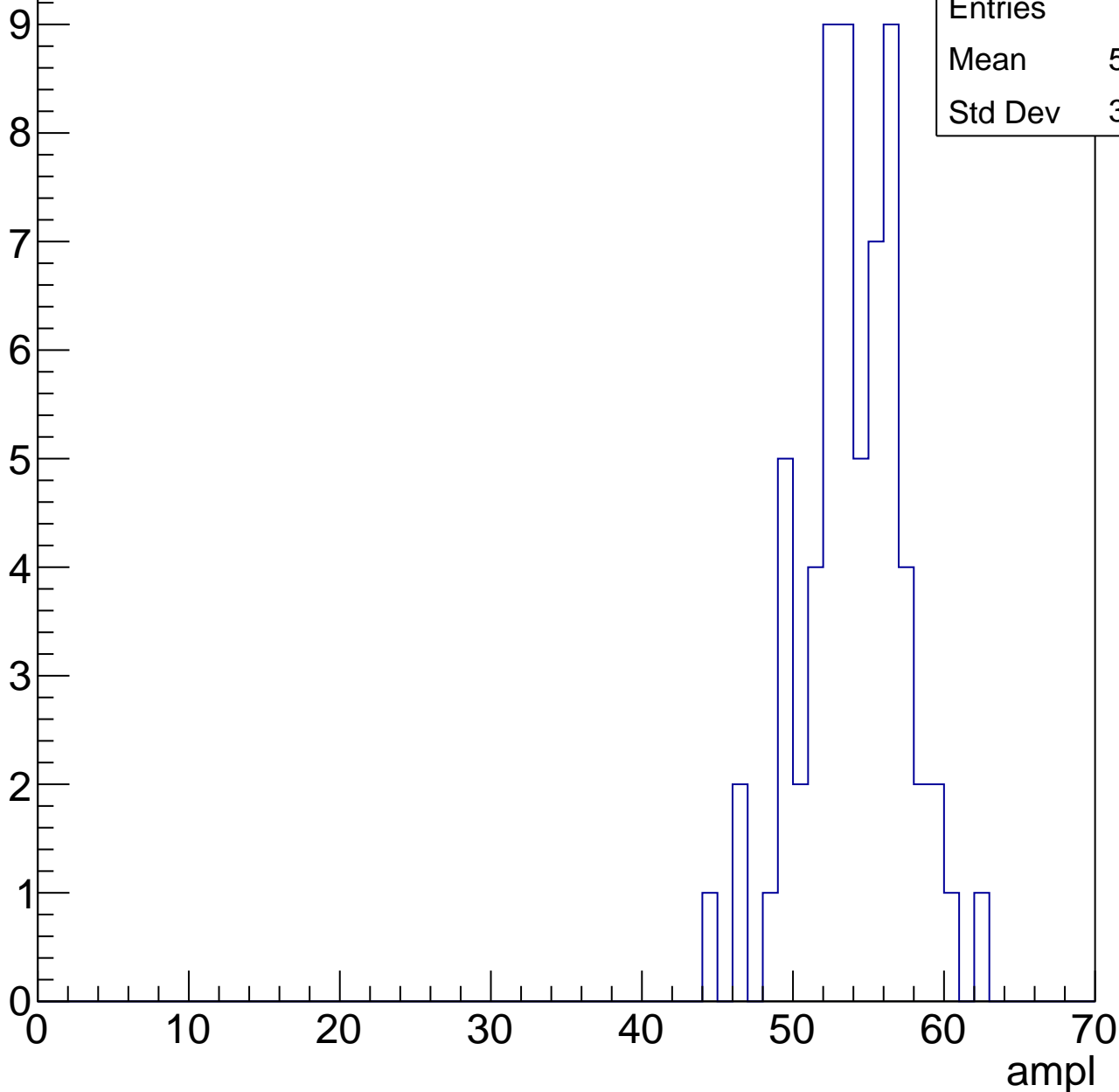


B1L103S, U23-ch112, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	53.45
Std Dev	3.409

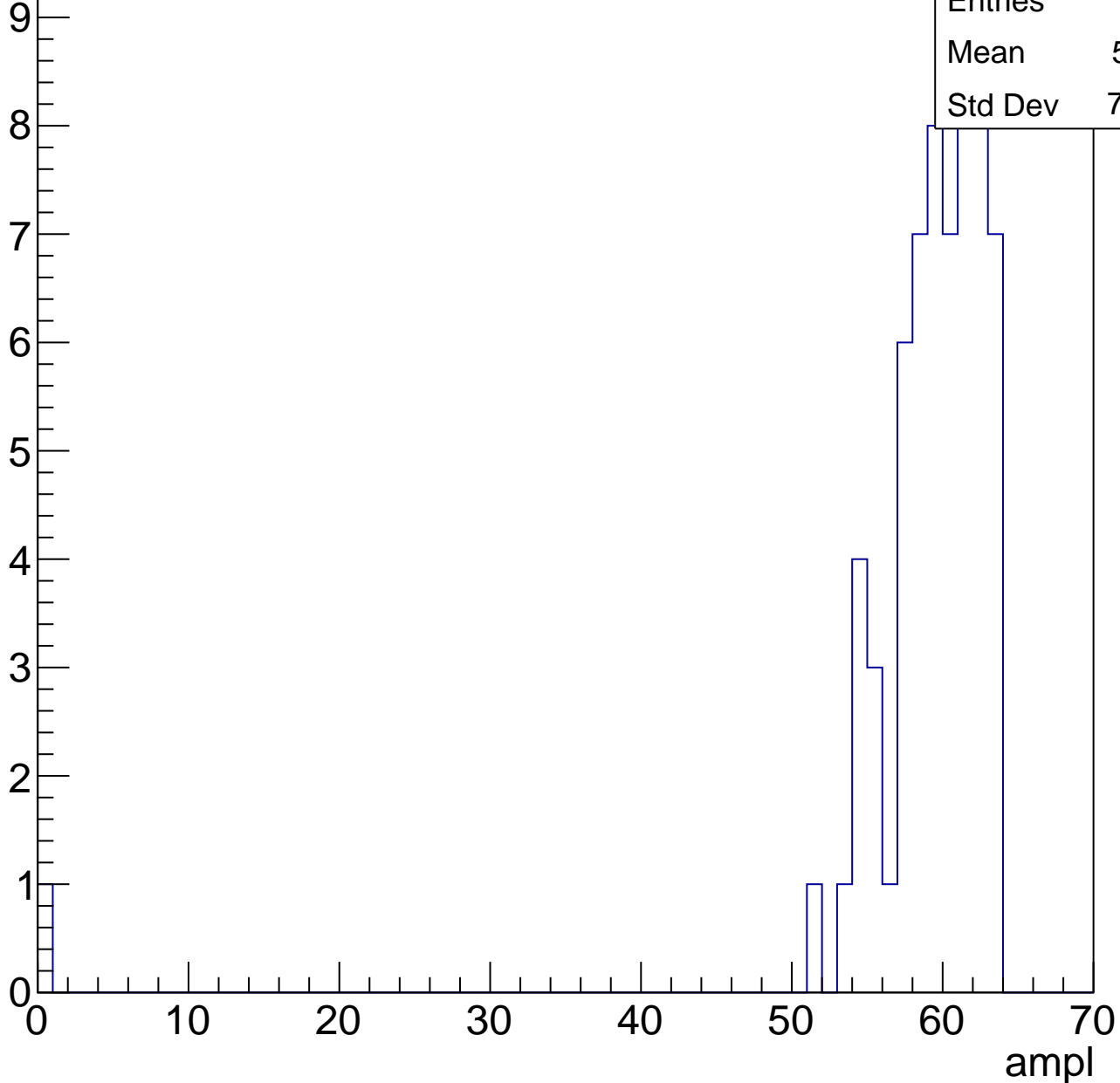


B1L103S, U23-ch112, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

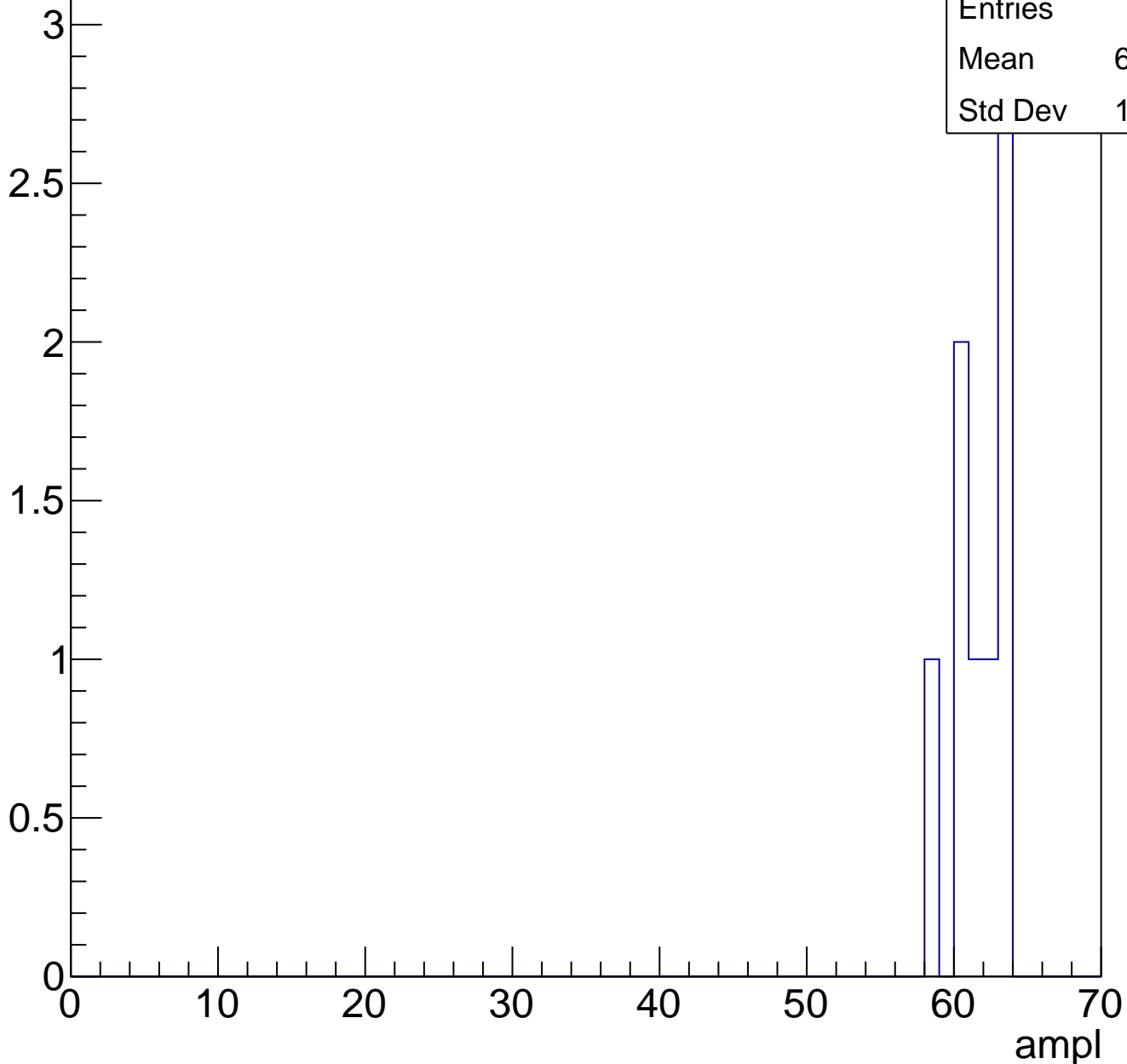
Entries	63
Mean	58.21
Std Dev	7.925



B1L103S, U23-ch112, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch112, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

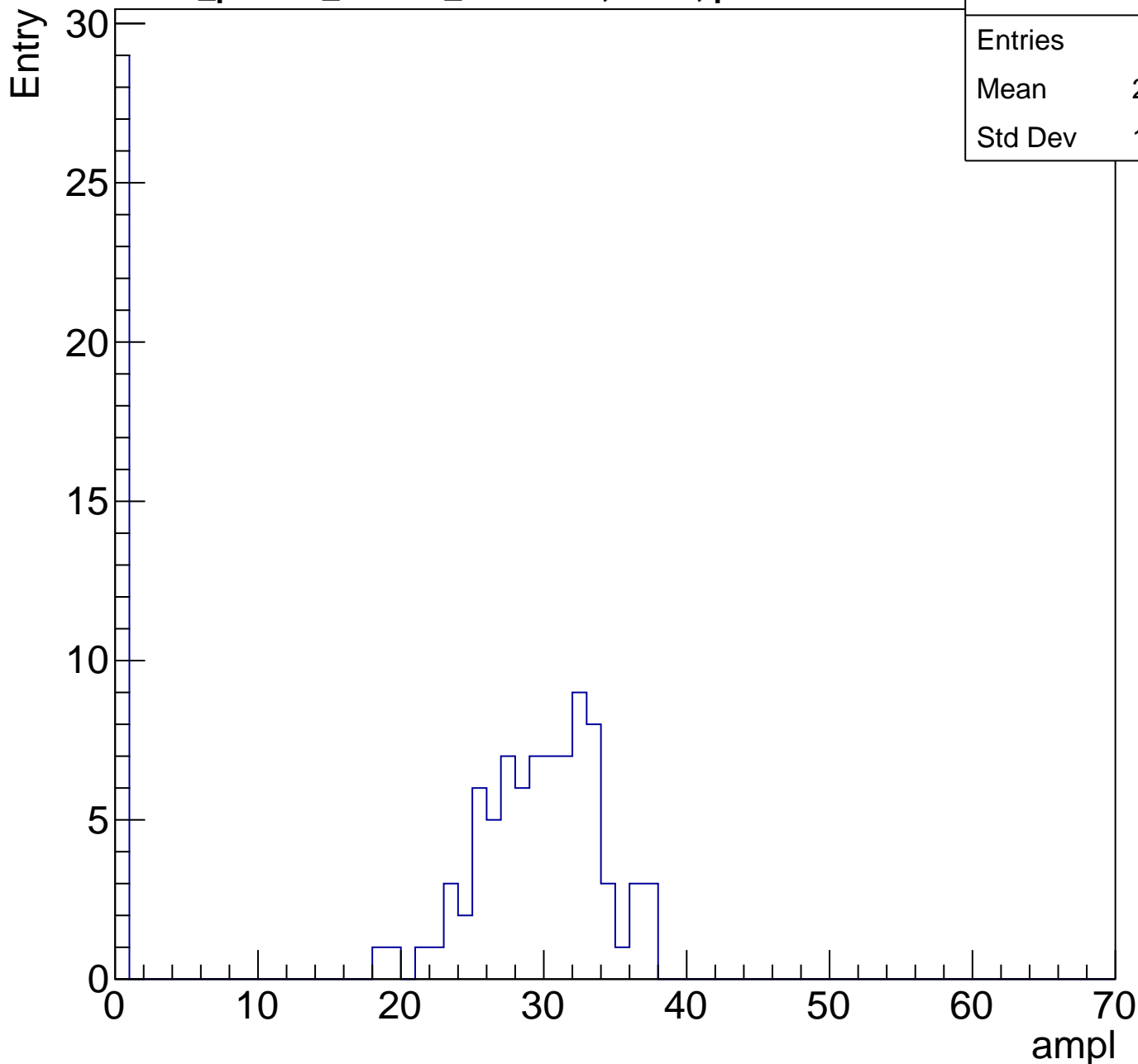
Entries	19
Mean	0
Std Dev	0

ampl

B1L103S, U23-ch113, adc0

calib_packv5_041523_1651.root, FC#0, port C2

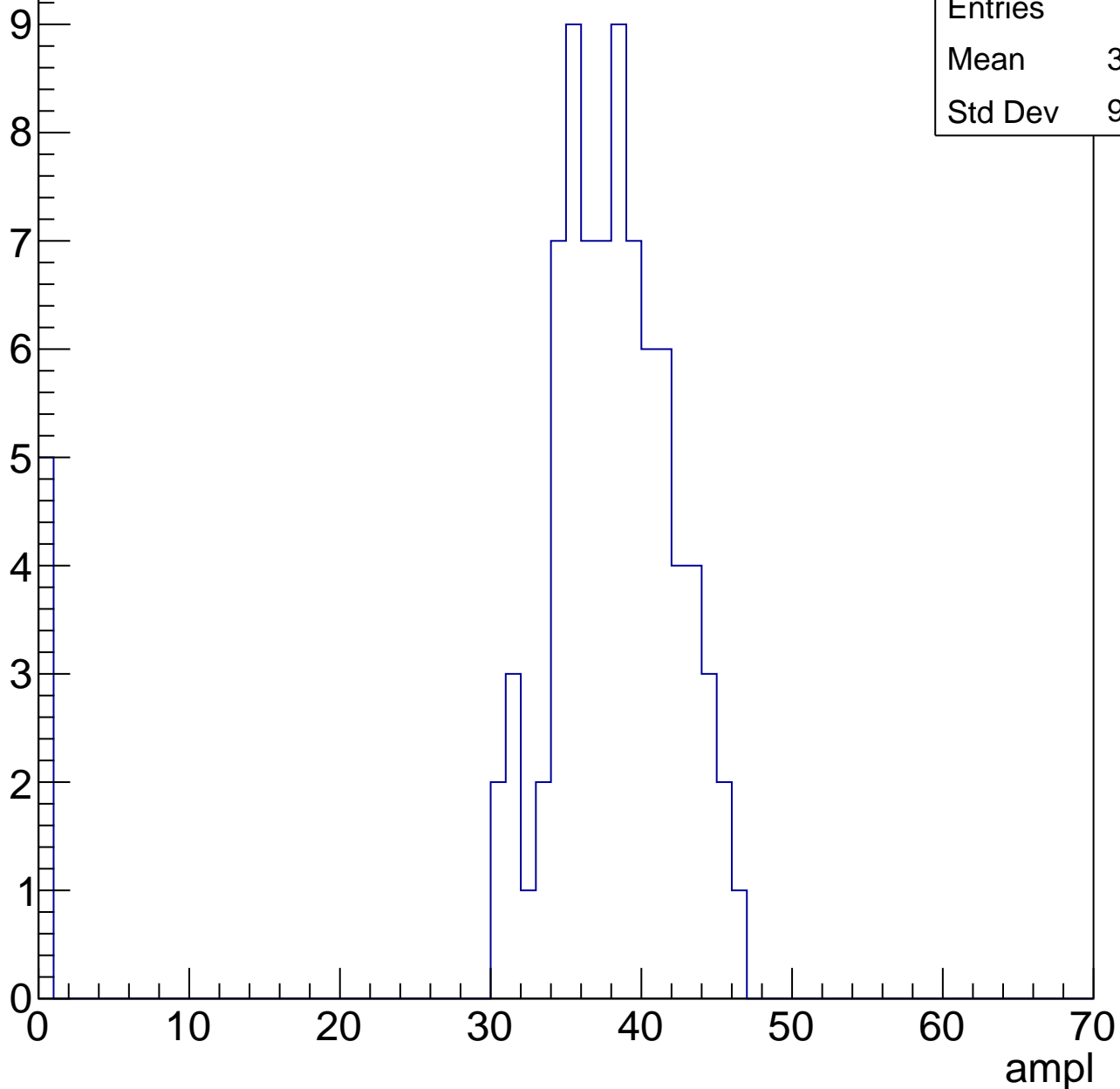
Entries	110
Mean	21.56
Std Dev	13.37



B1L103S, U23-ch113, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry



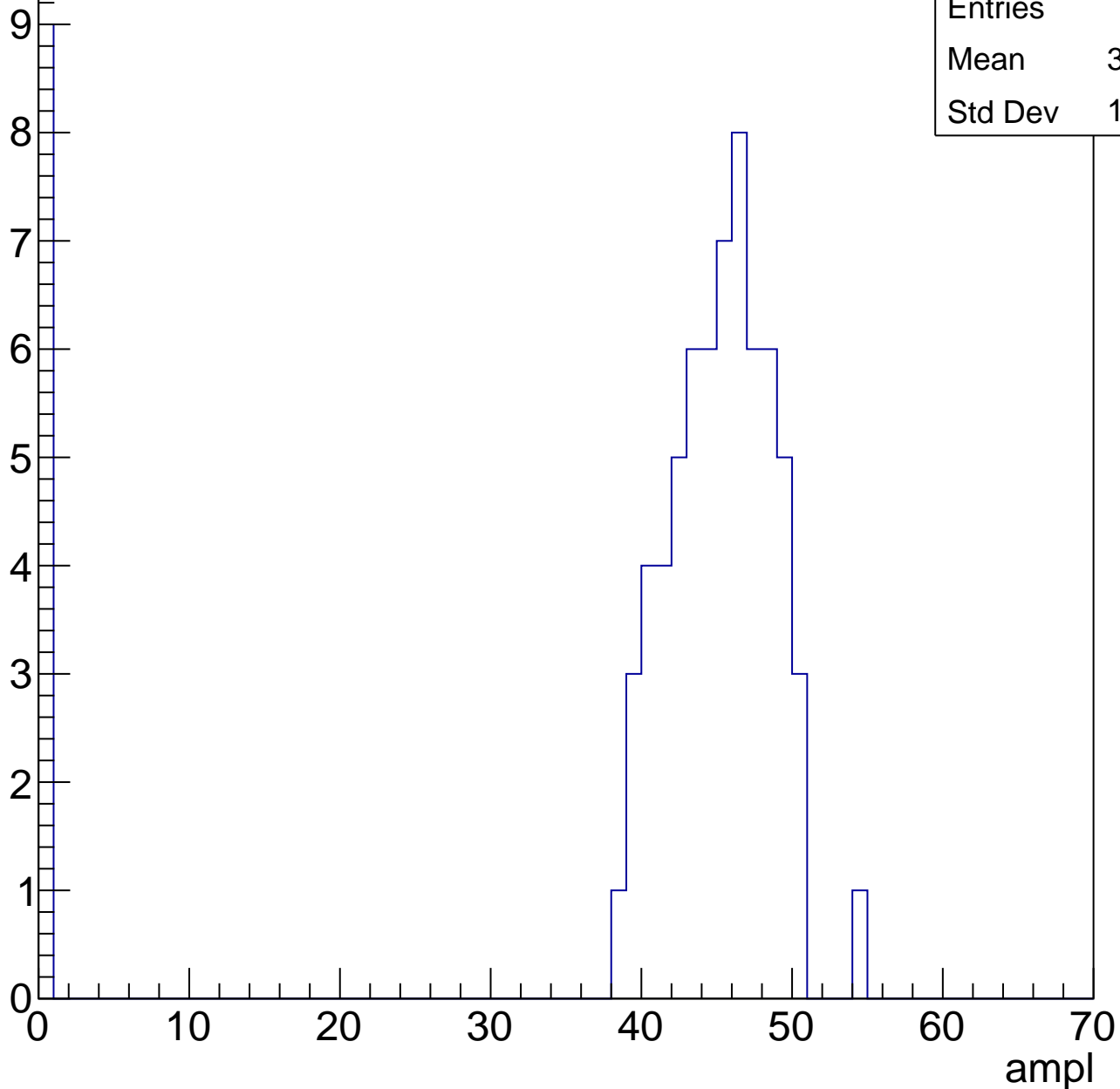
Entries	85
Mean	35.58
Std Dev	9.597

B1L103S, U23-ch113, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	74
Mean	39.36
Std Dev	14.97

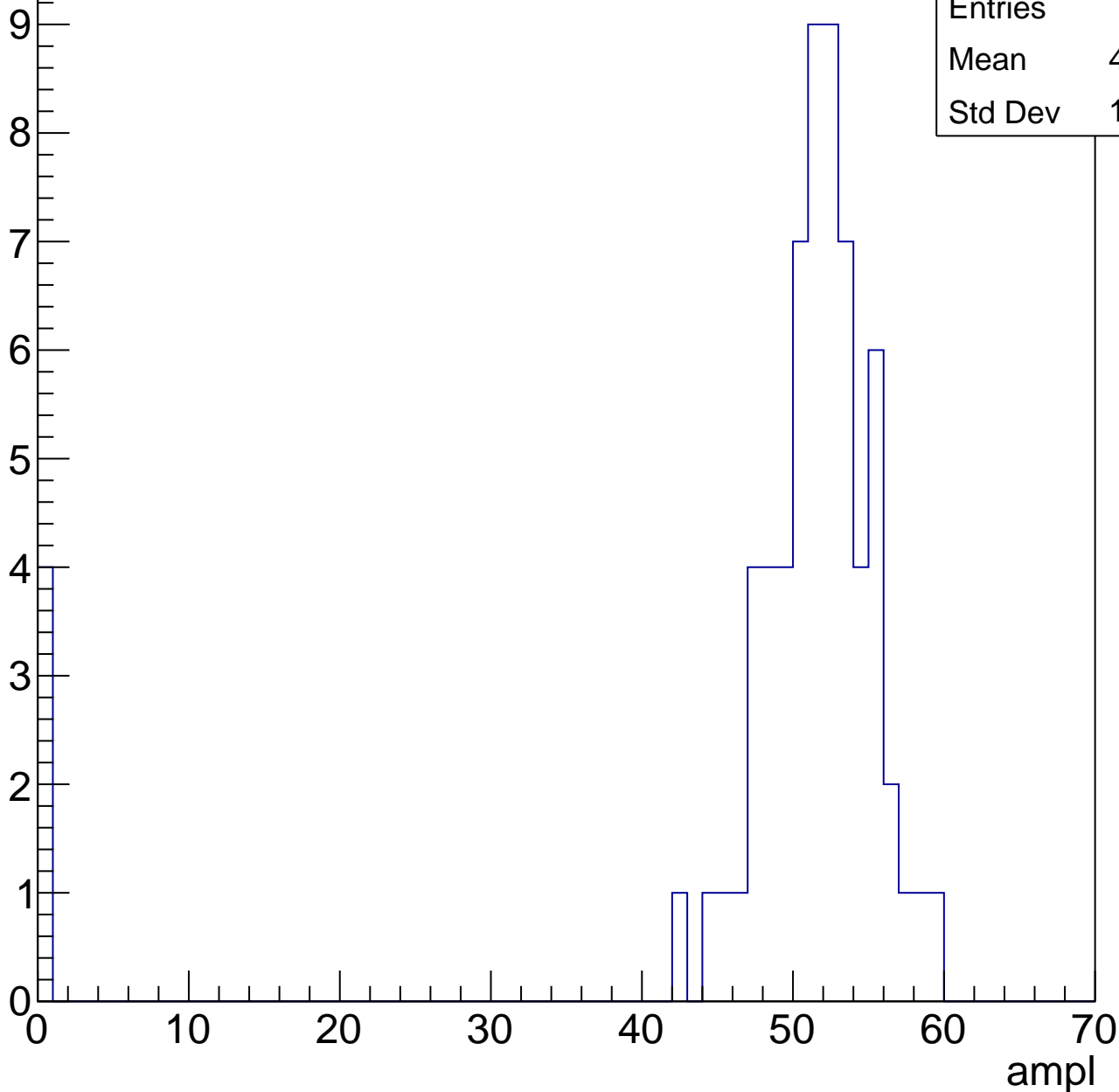


B1L103S, U23-ch113, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	48.25
Std Dev	12.57

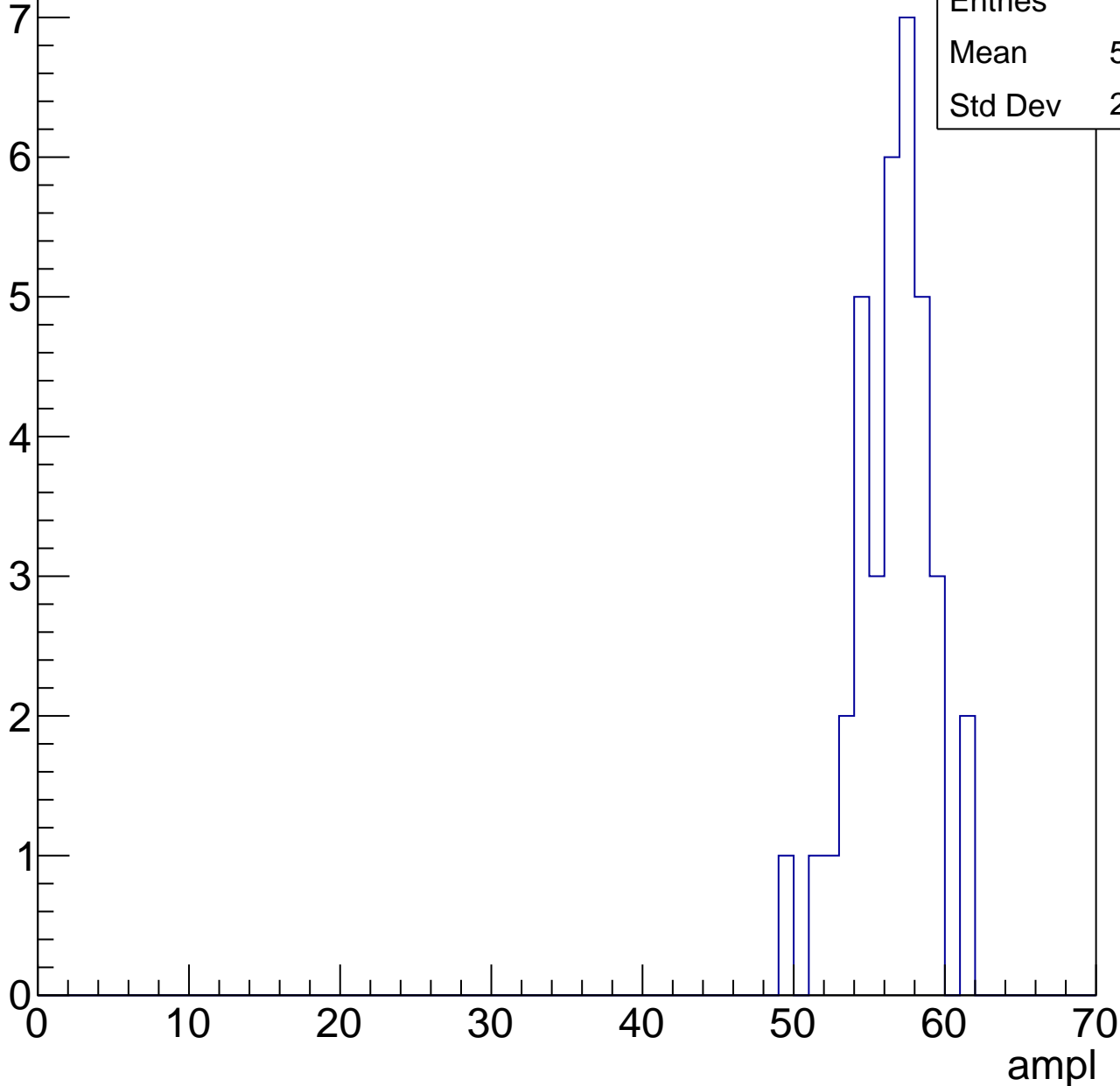


B1L103S, U23-ch113, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	36
Mean	56.03
Std Dev	2.555

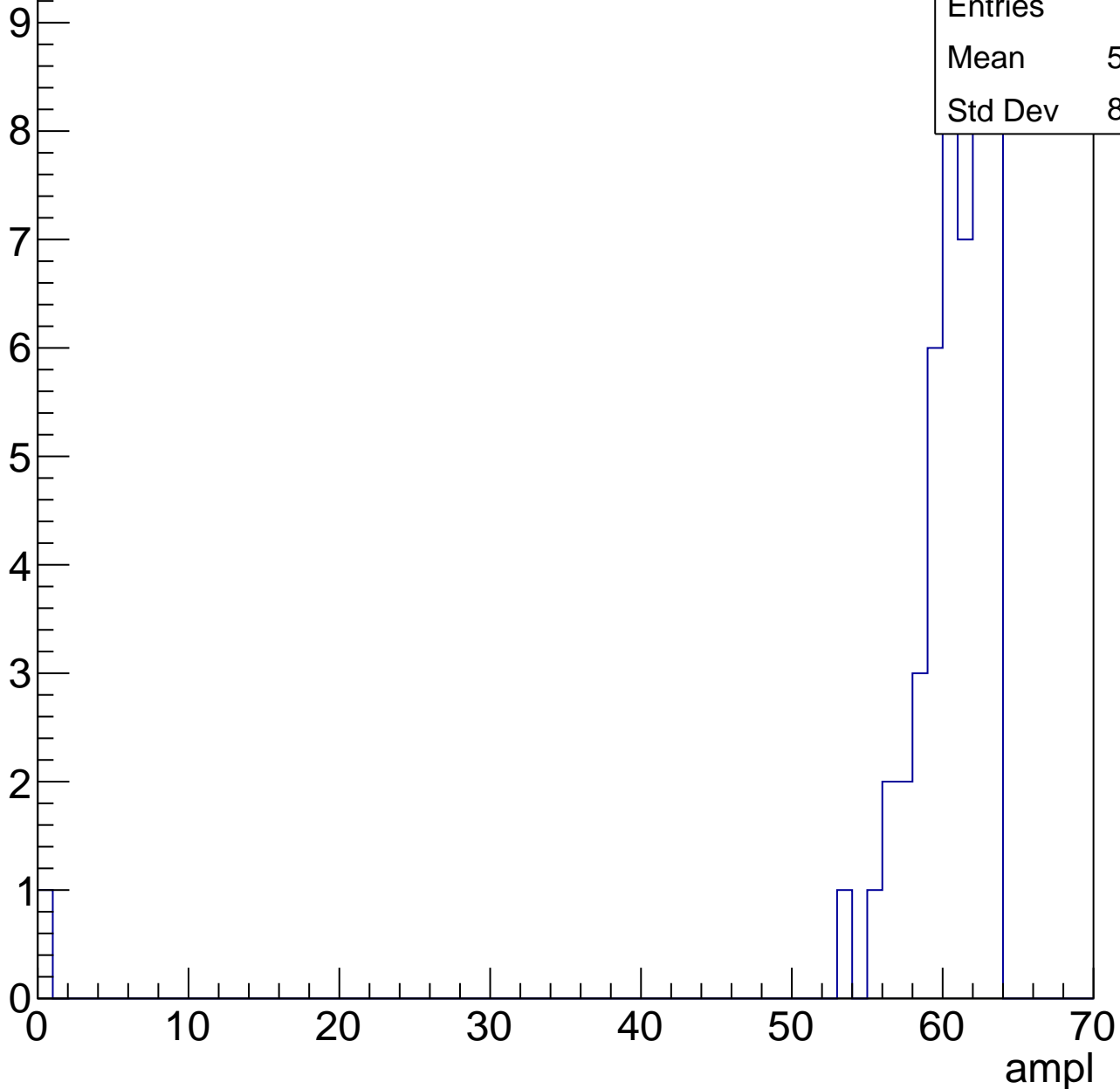


B1L103S, U23-ch113, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

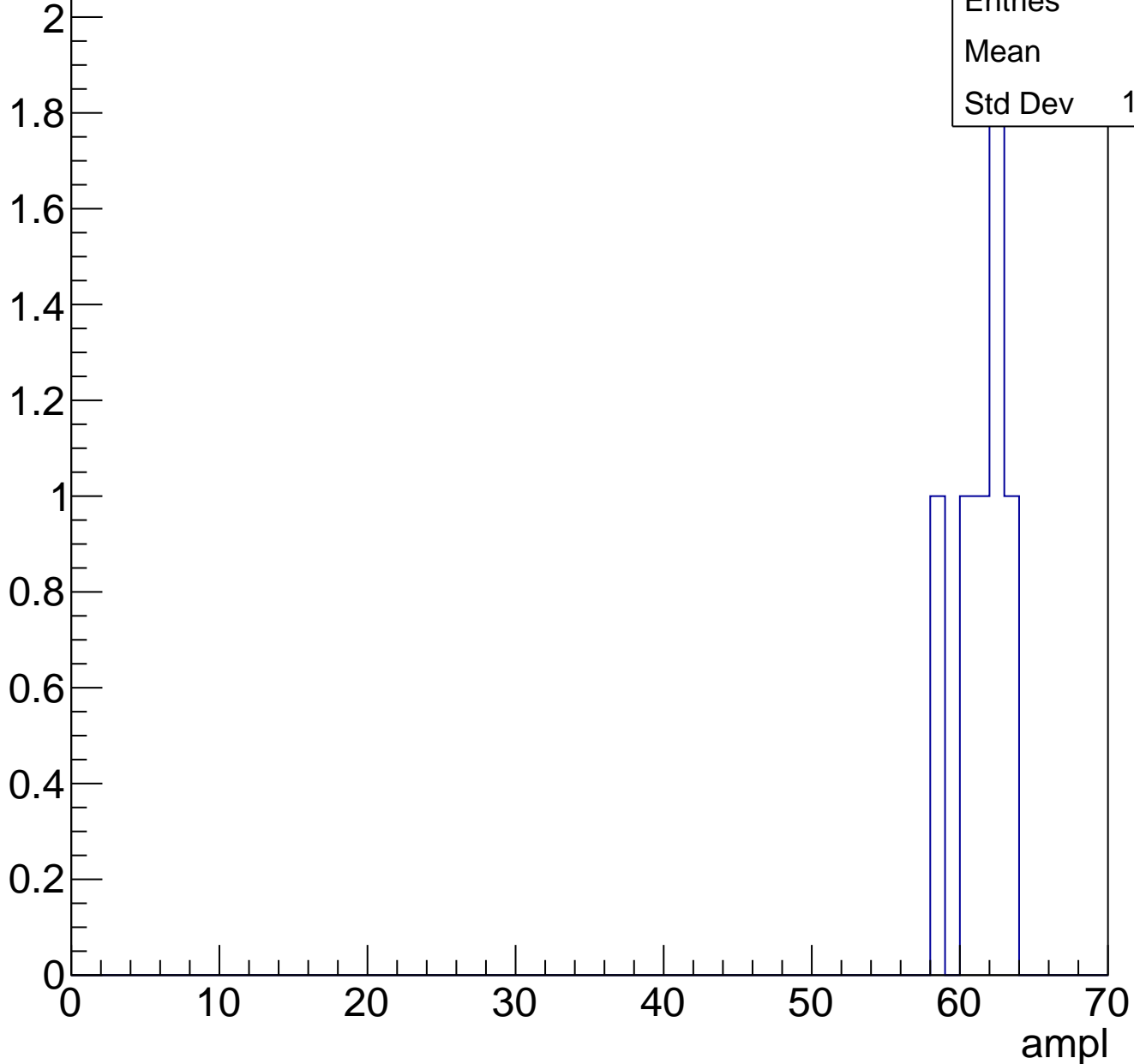
Entries	49
Mean	59.02
Std Dev	8.824



B1L103S, U23-ch113, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch113, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

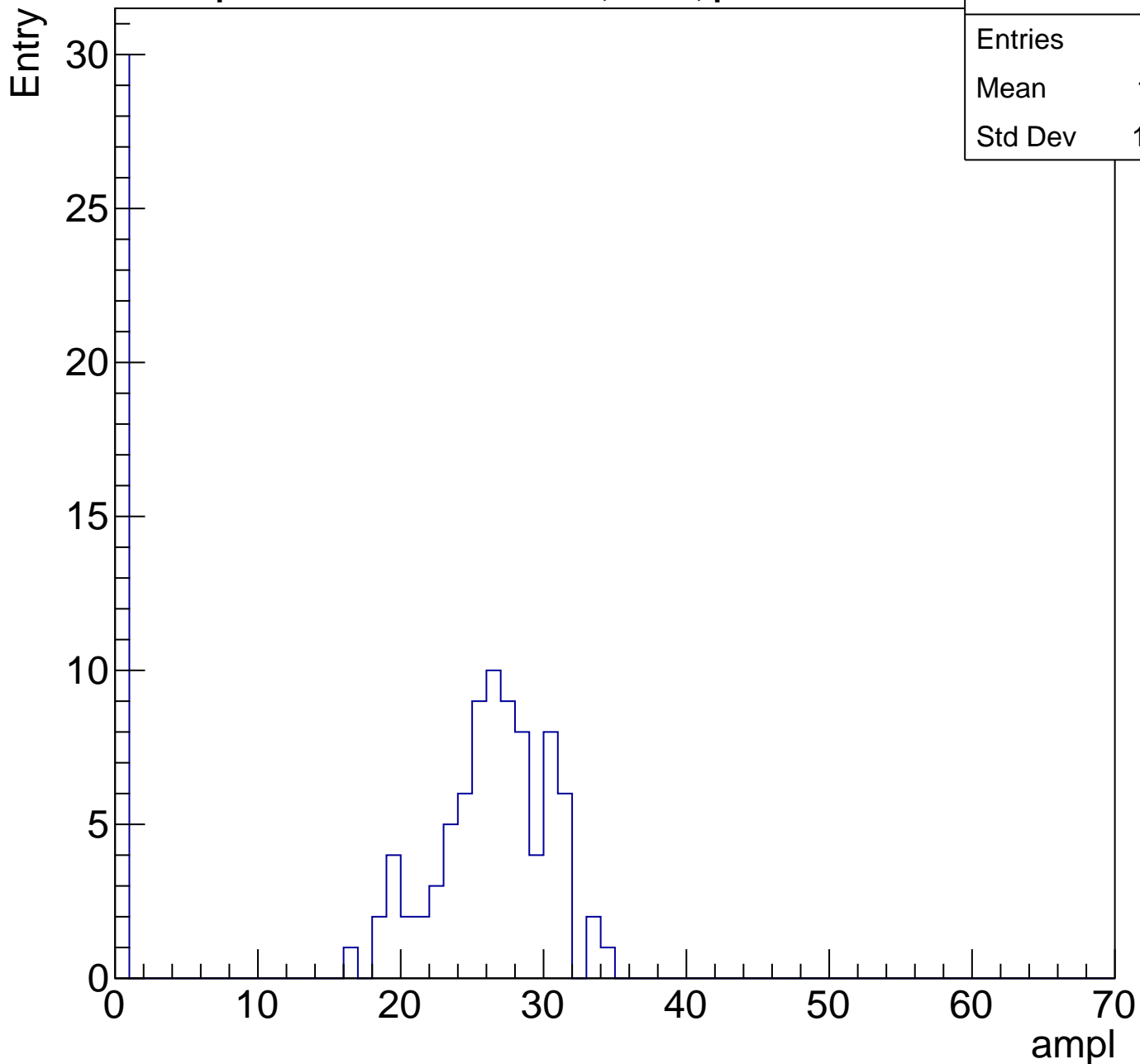
Entries	19
Mean	0
Std Dev	0

ampl

B1L103S, U23-ch114, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	112
Mean	19.01
Std Dev	11.95

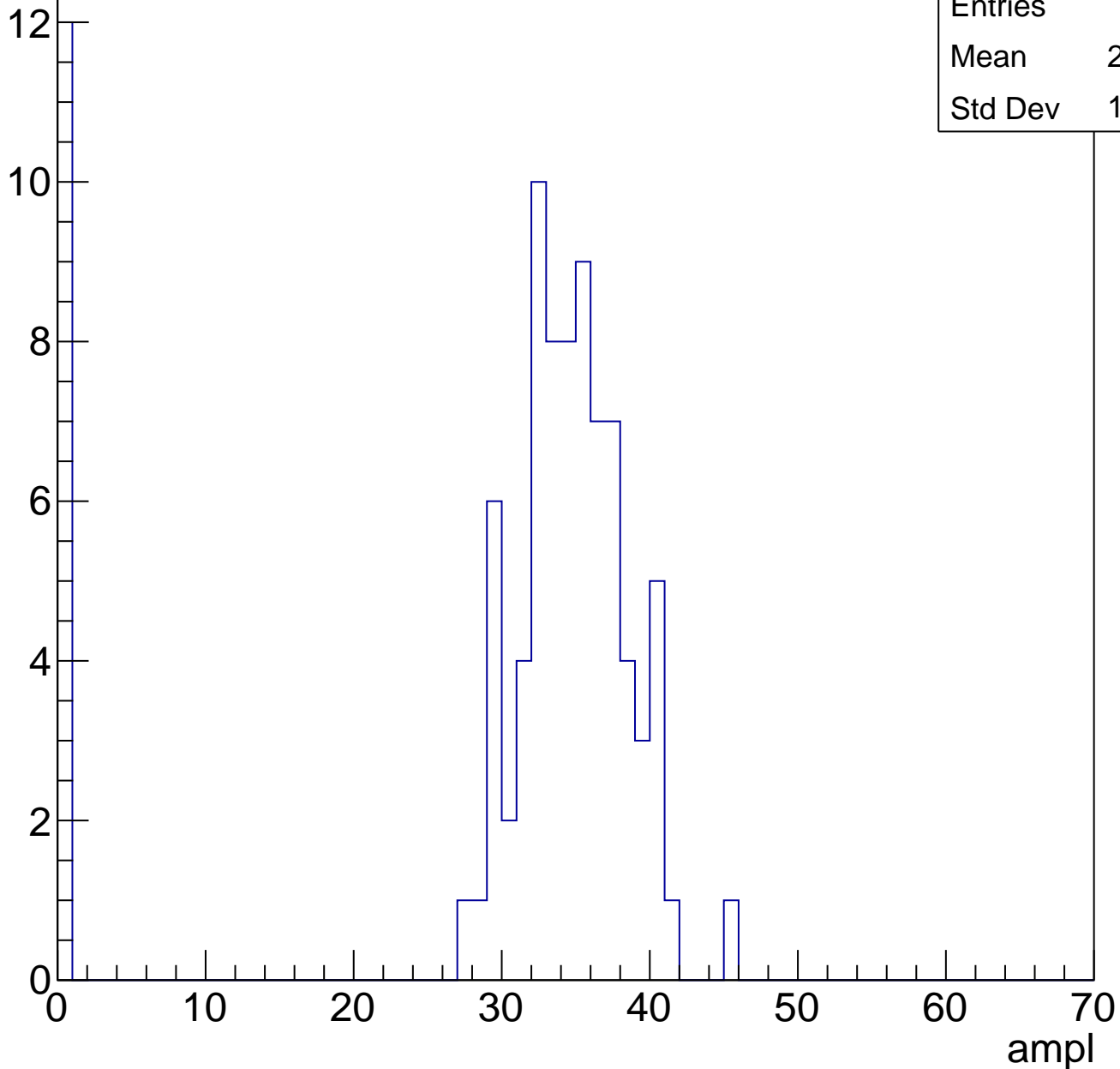


B1L103S, U23-ch114, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	89
Mean	29.78
Std Dev	12.19

Entry

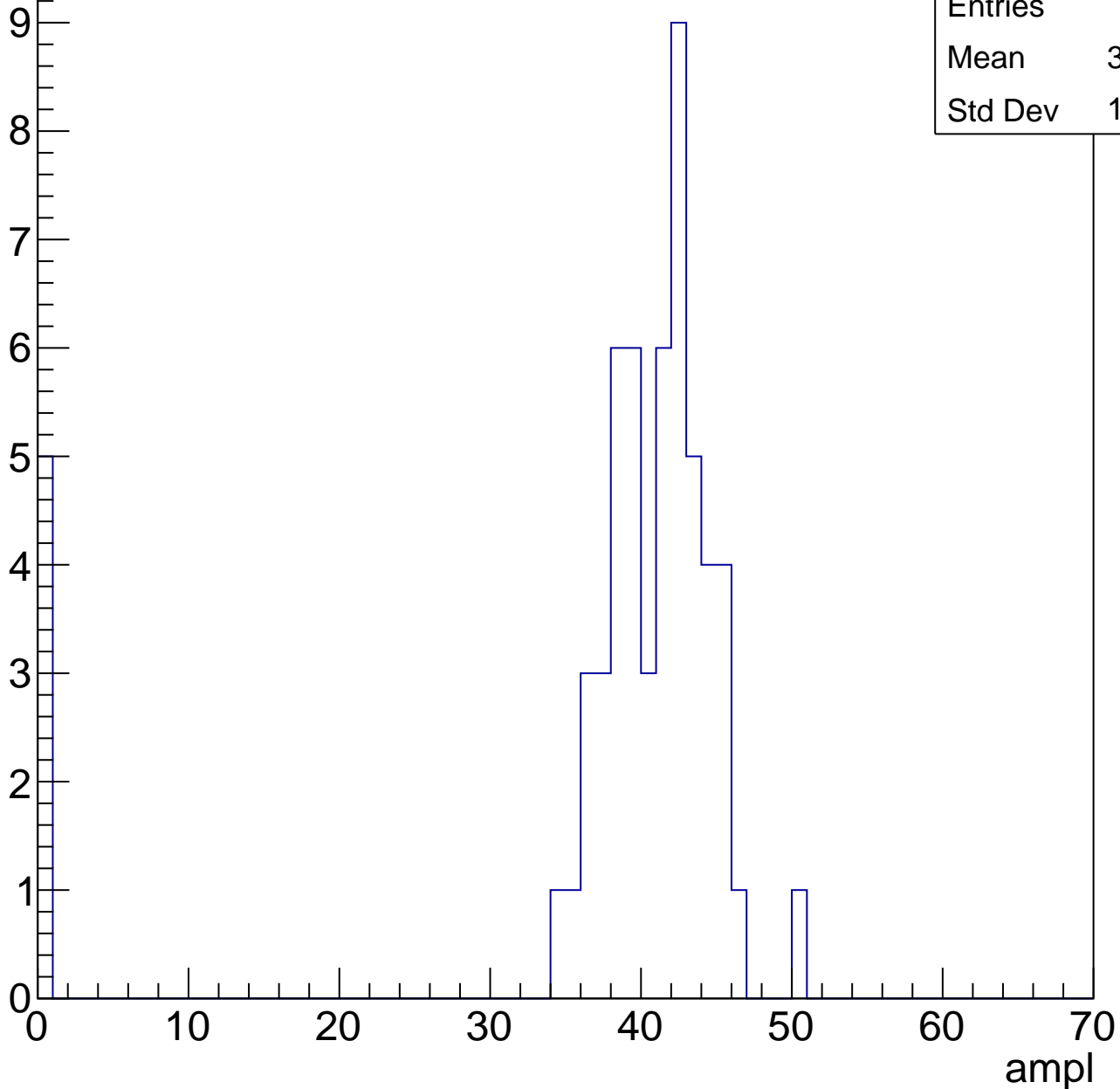


B1L103S, U23-ch114, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	37.26
Std Dev	11.83

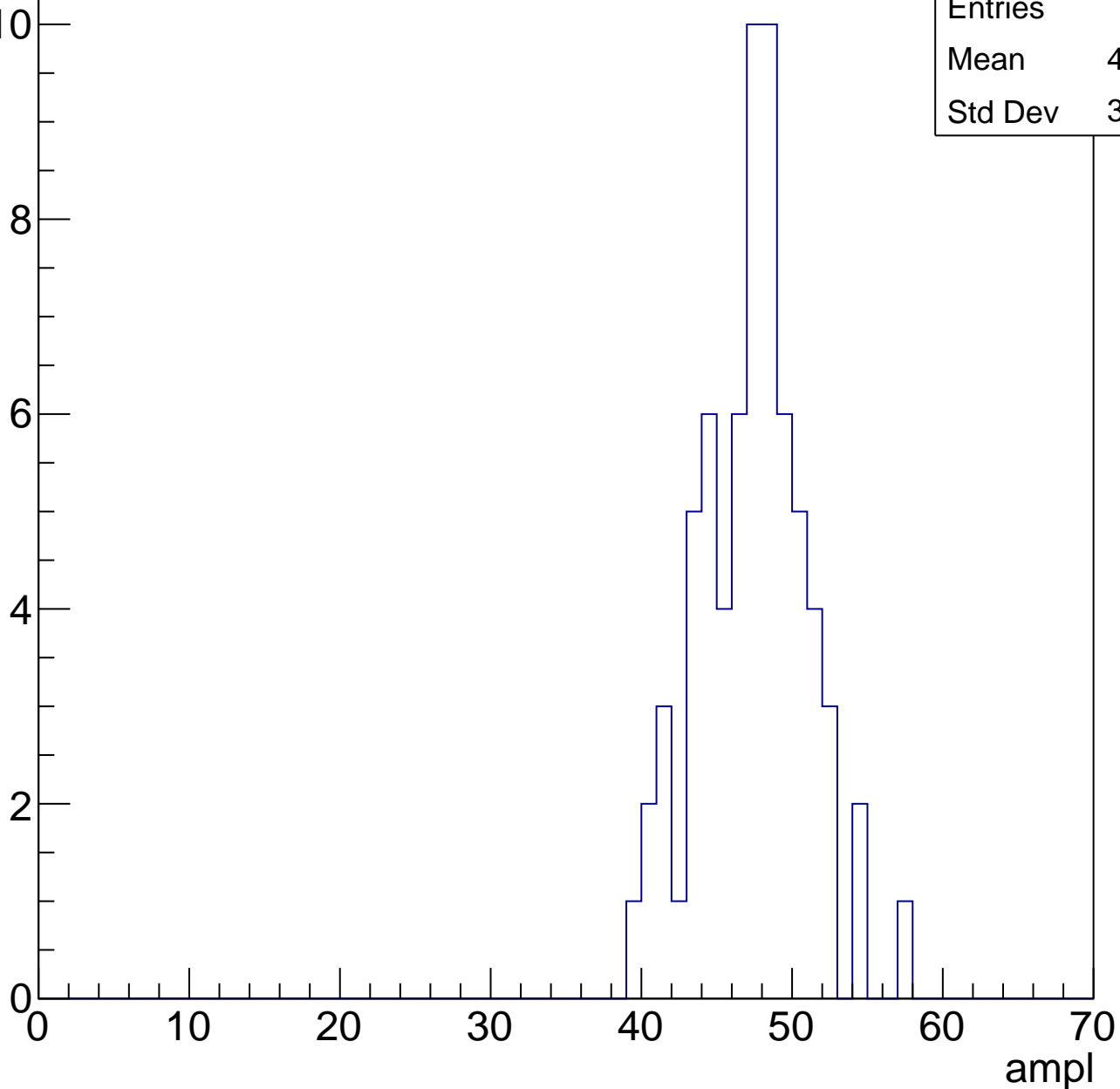


B1L103S, U23-ch114, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	46.93
Std Dev	3.544

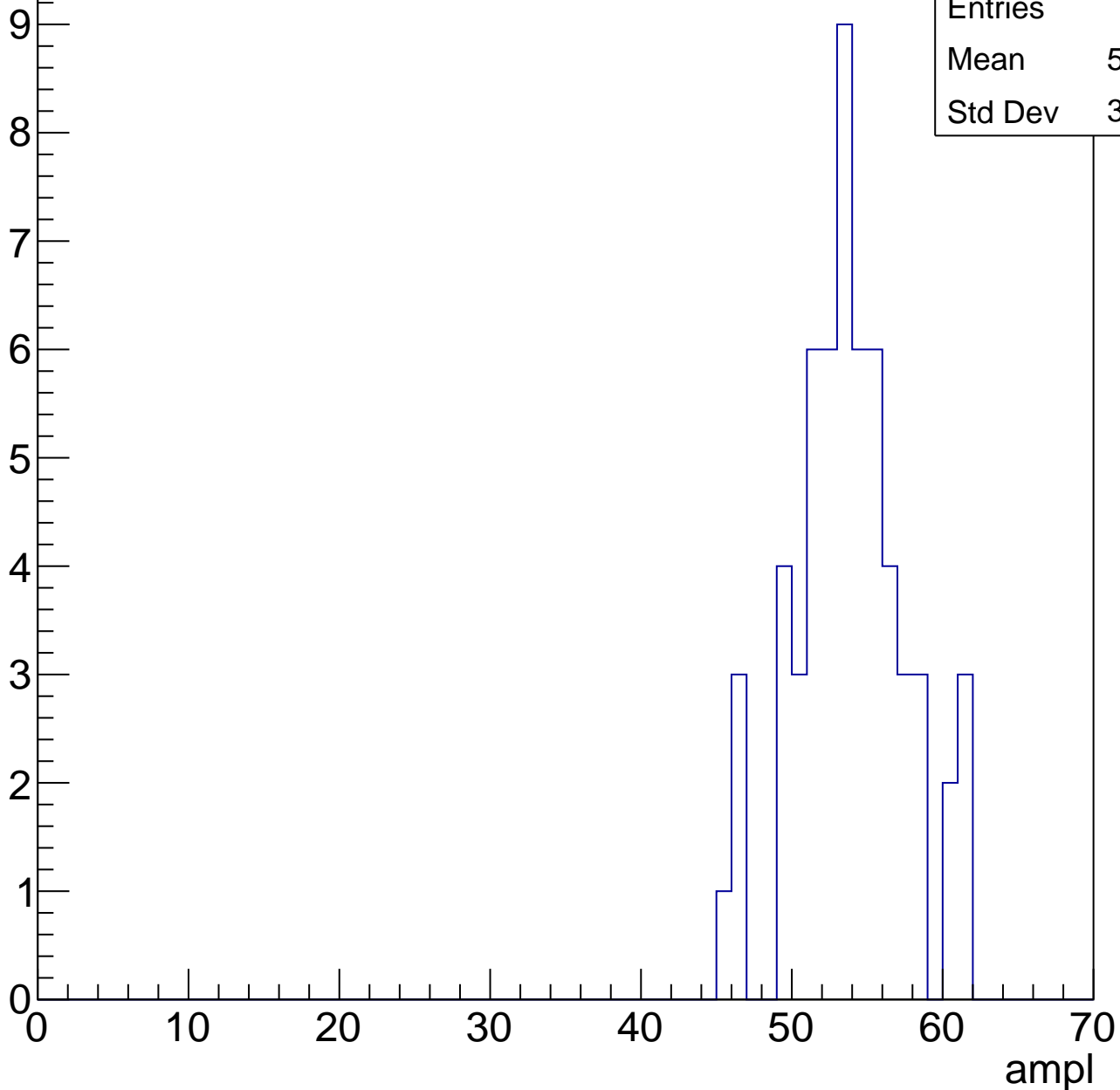


B1L103S, U23-ch114, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	53.39
Std Dev	3.687

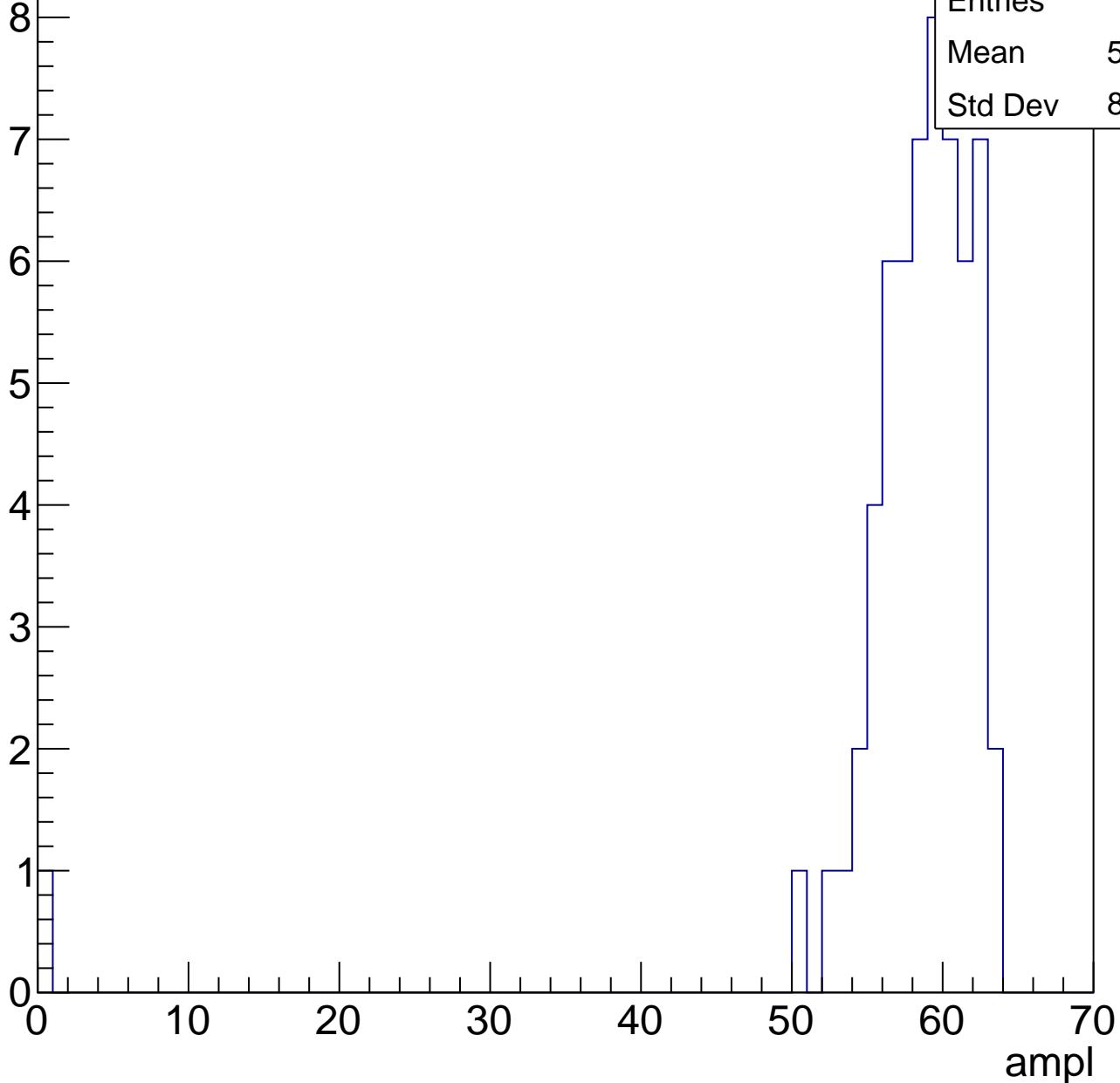


B1L103S, U23-ch114, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	57.37
Std Dev	8.042

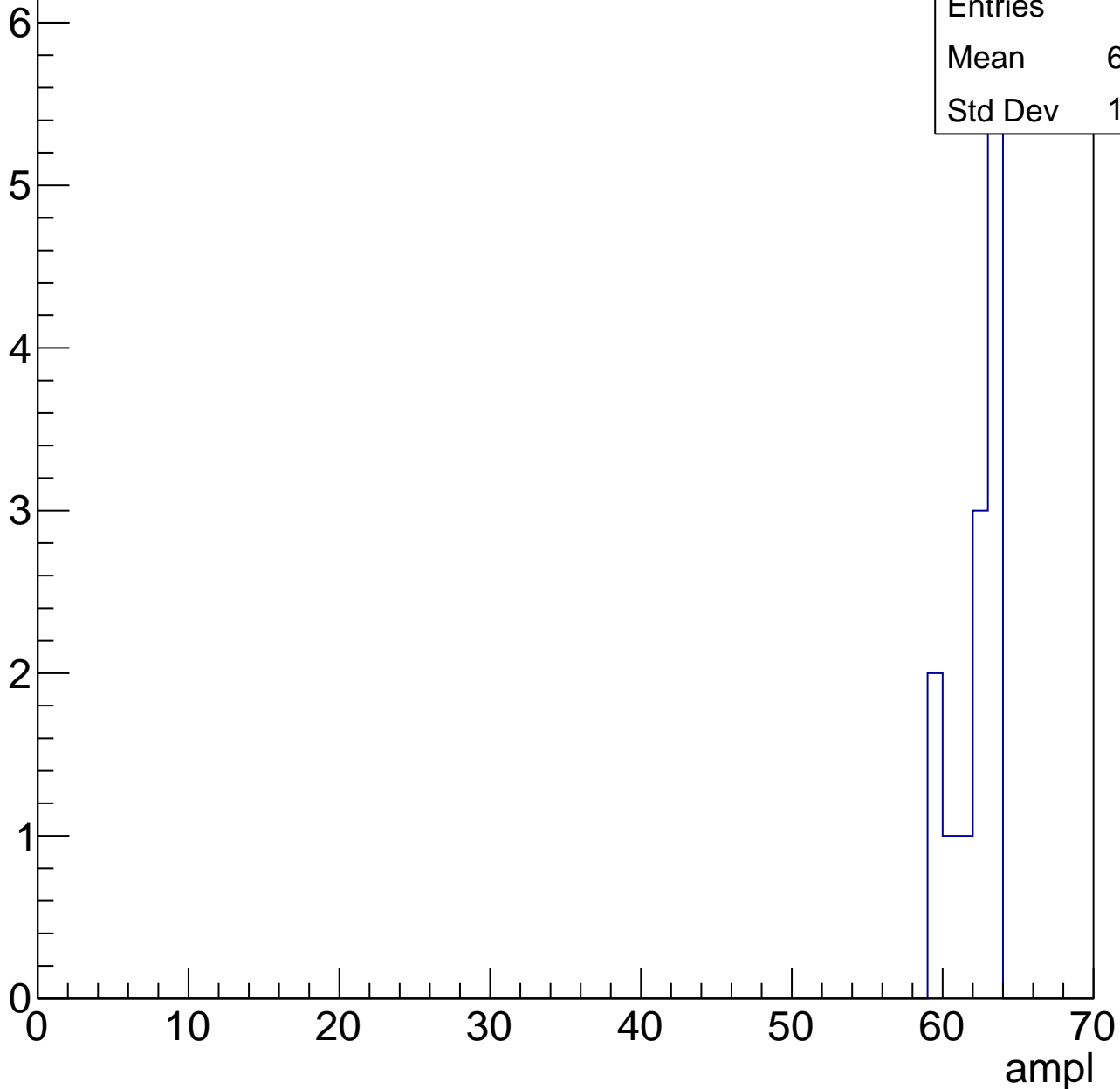


B1L103S, U23-ch114, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

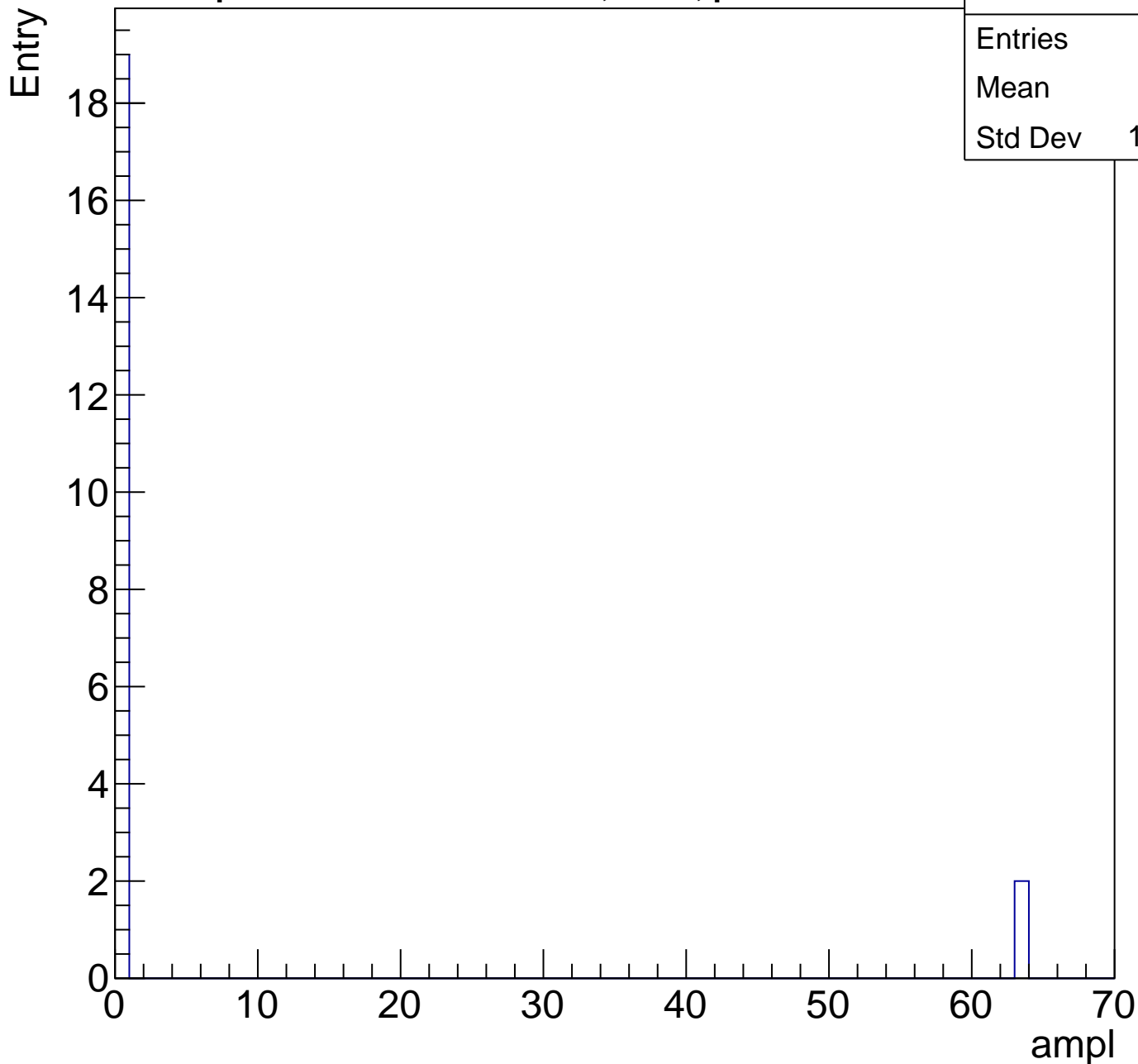
Entries	13
Mean	61.77
Std Dev	1.476



B1L103S, U23-ch114, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	21
Mean	6
Std Dev	18.49

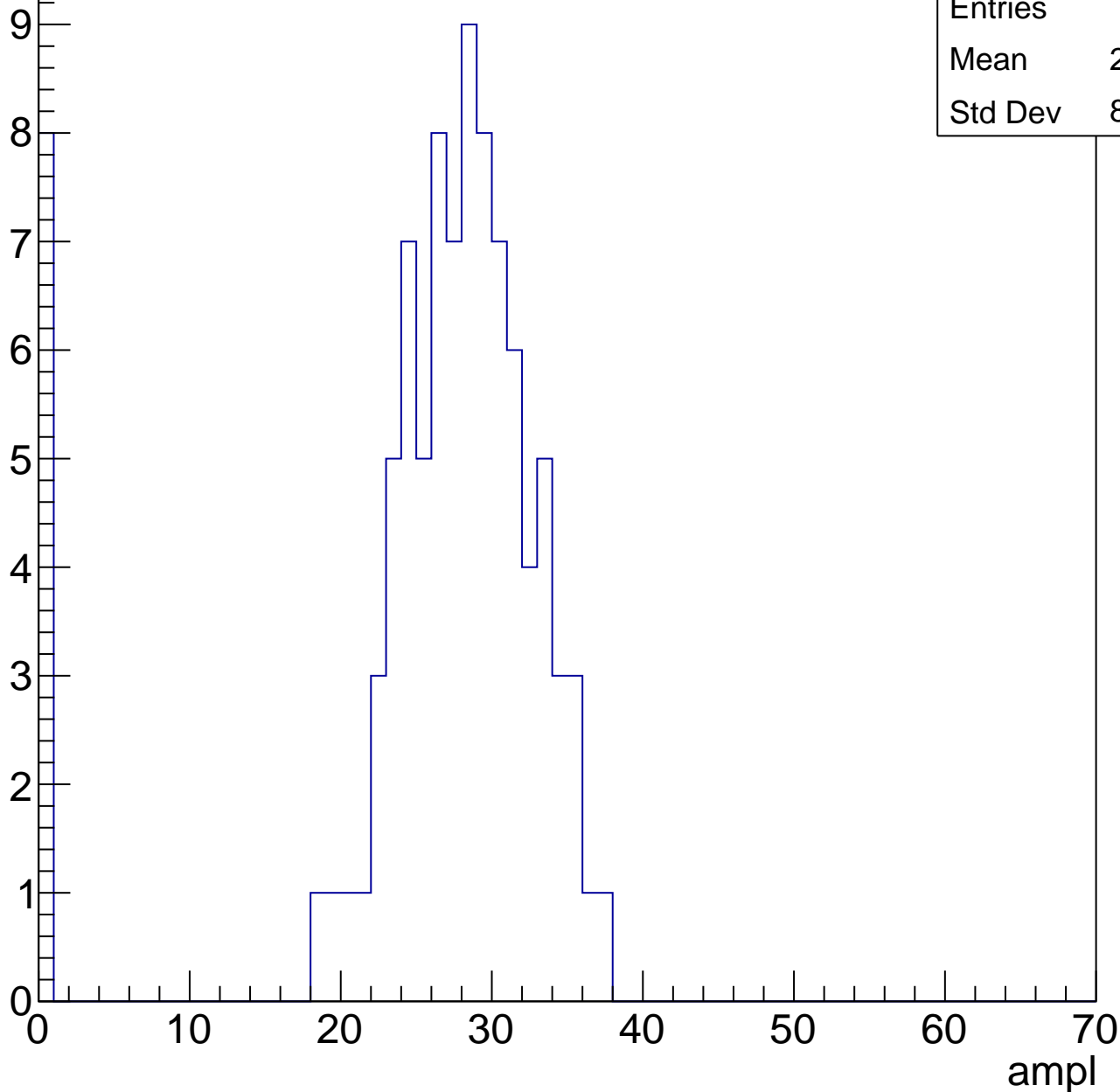


B1L103S, U23-ch115, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	94
Mean	25.55
Std Dev	8.698

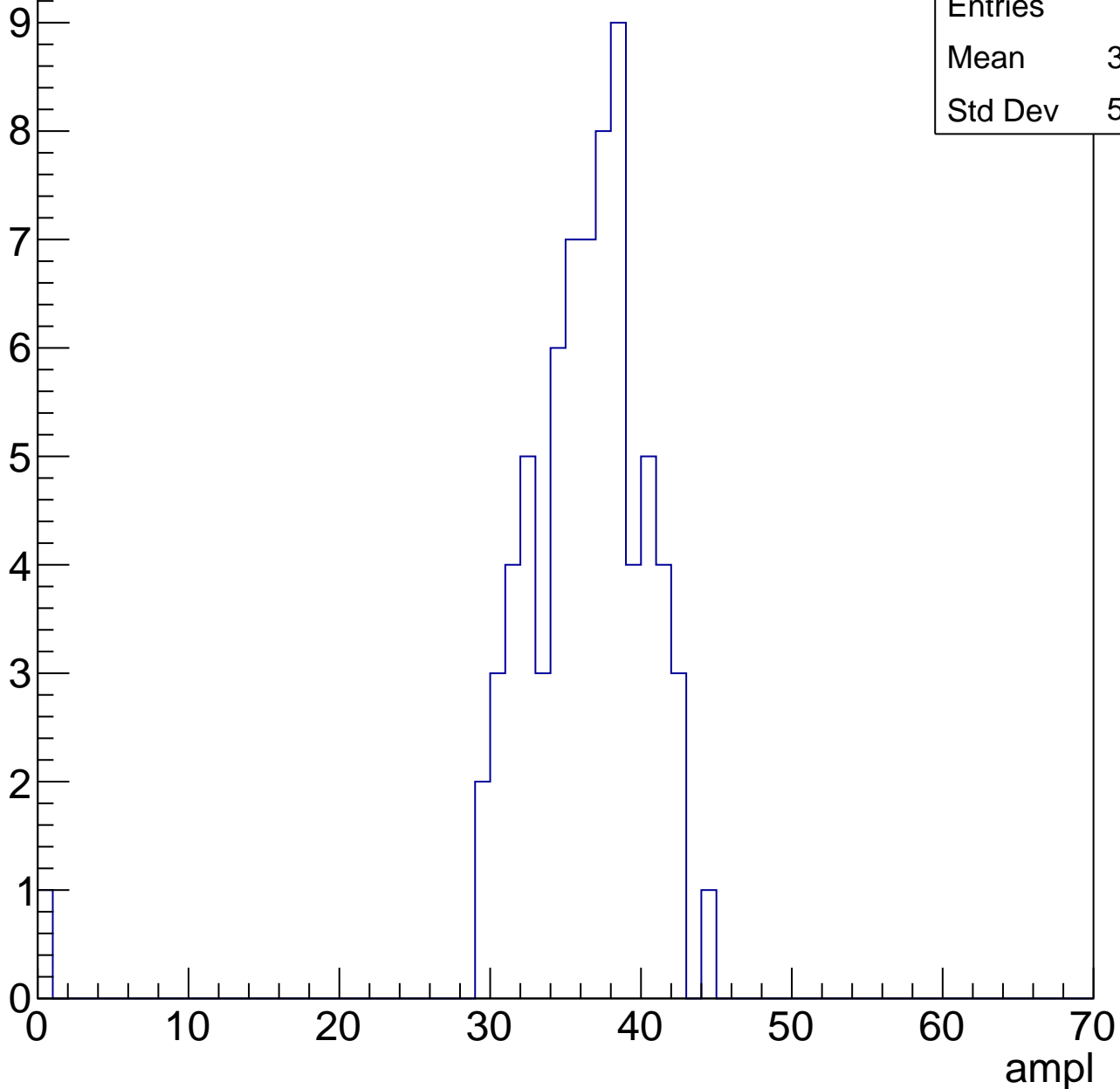


B1L103S, U23-ch115, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	72
Mean	35.56
Std Dev	5.474

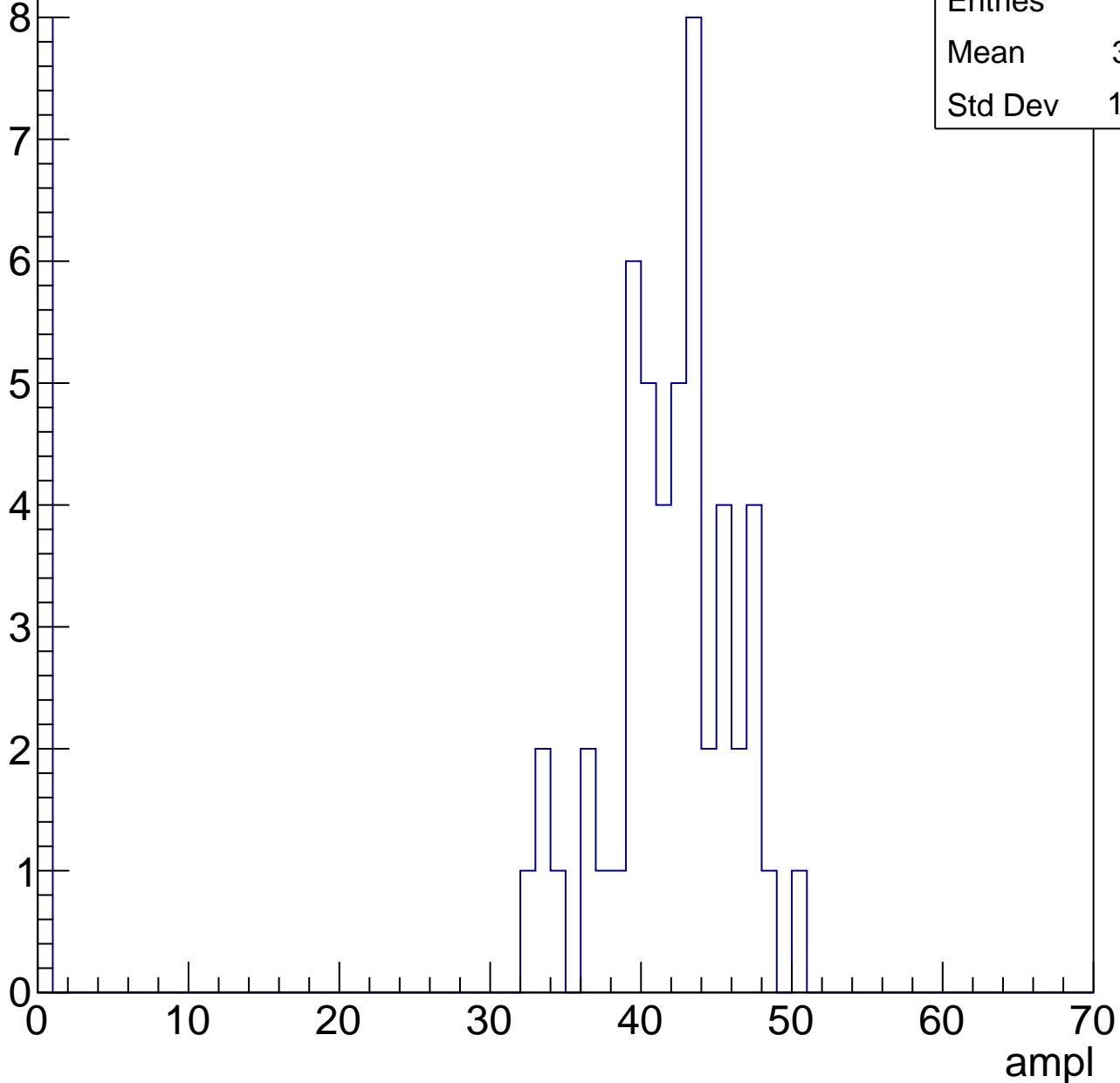


B1L103S, U23-ch115, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	35.81
Std Dev	14.79

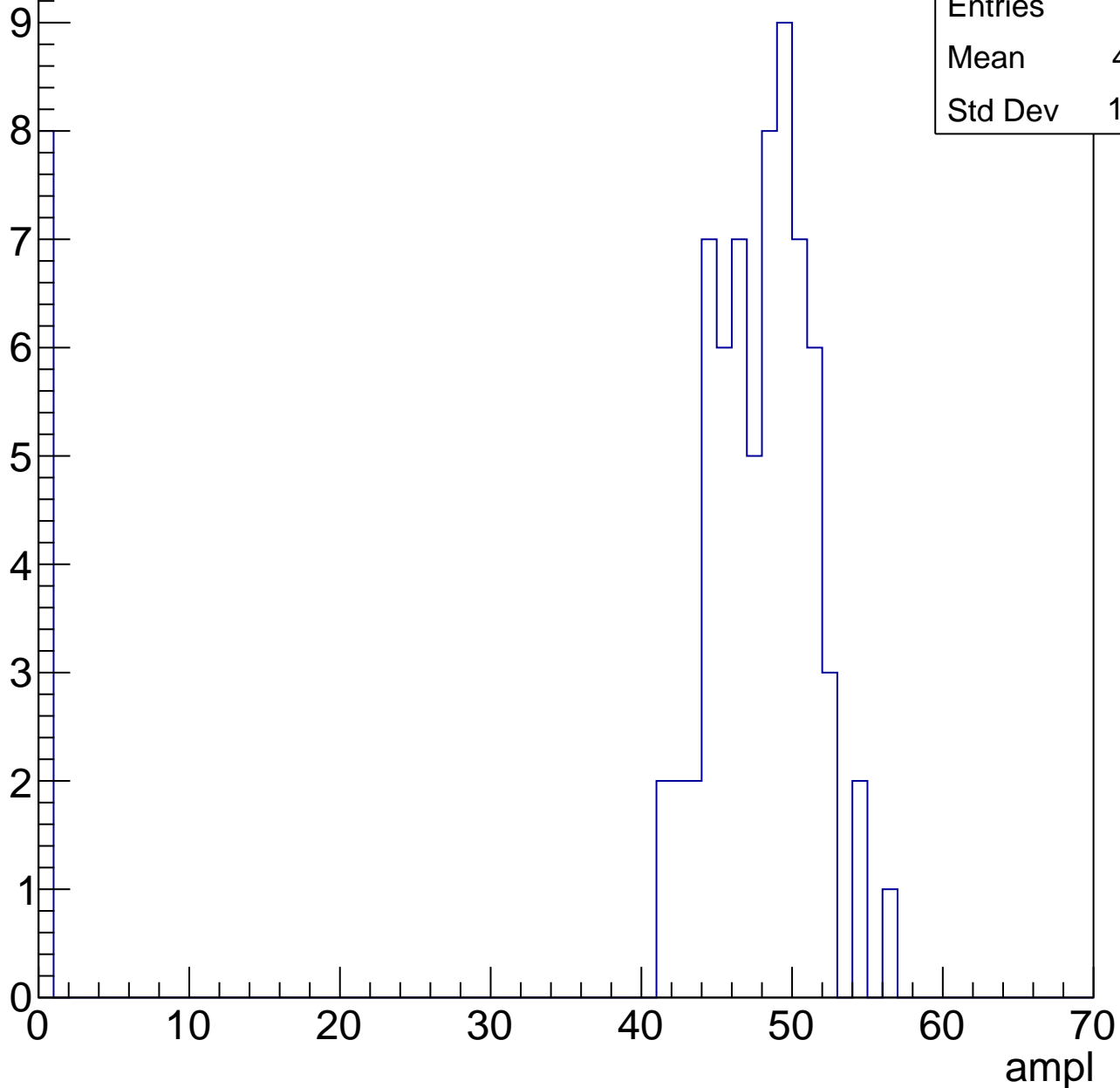


B1L103S, U23-ch115, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	75
Mean	42.51
Std Dev	14.99

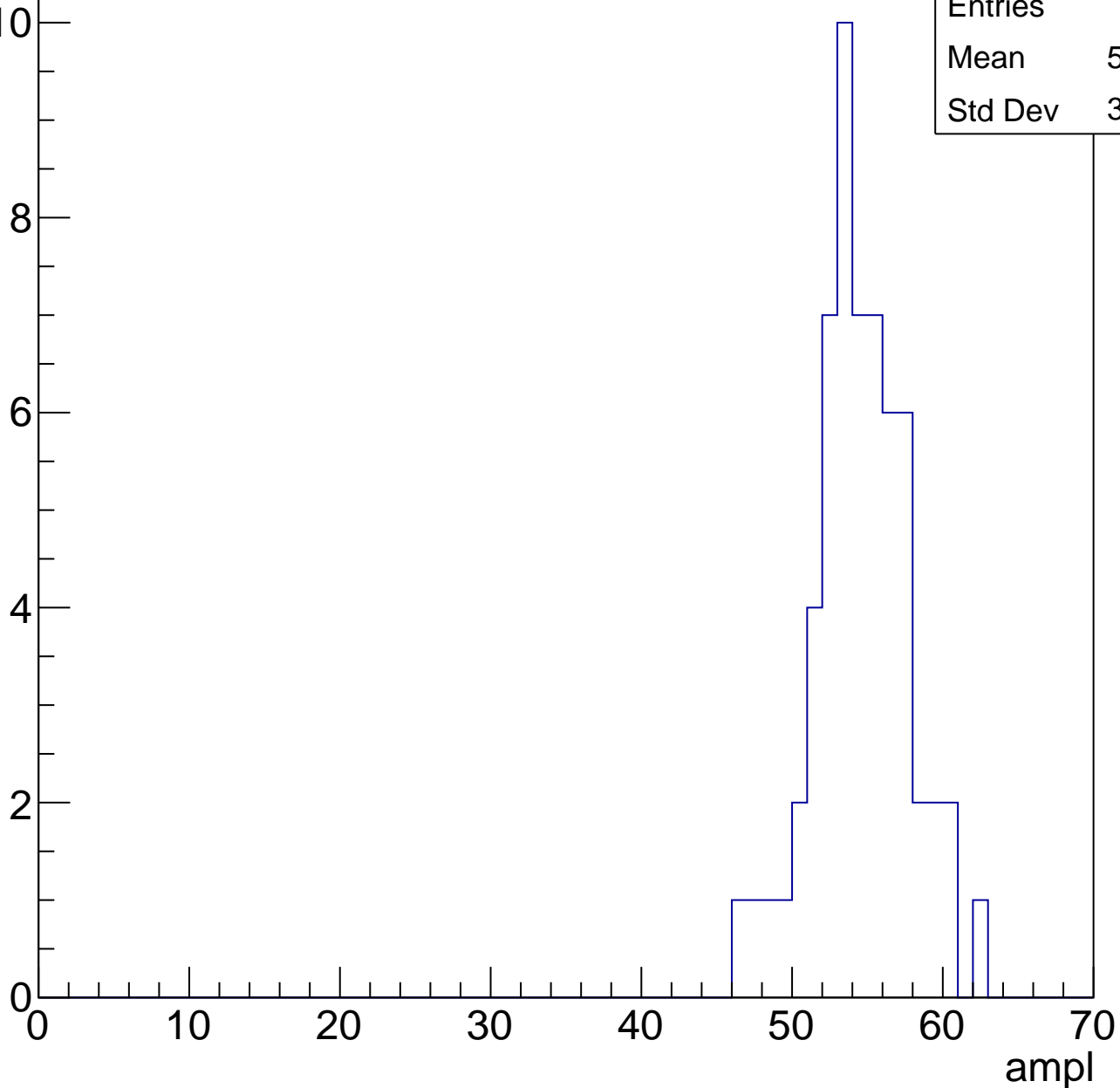


B1L103S, U23-ch115, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	54.08
Std Dev	3.116

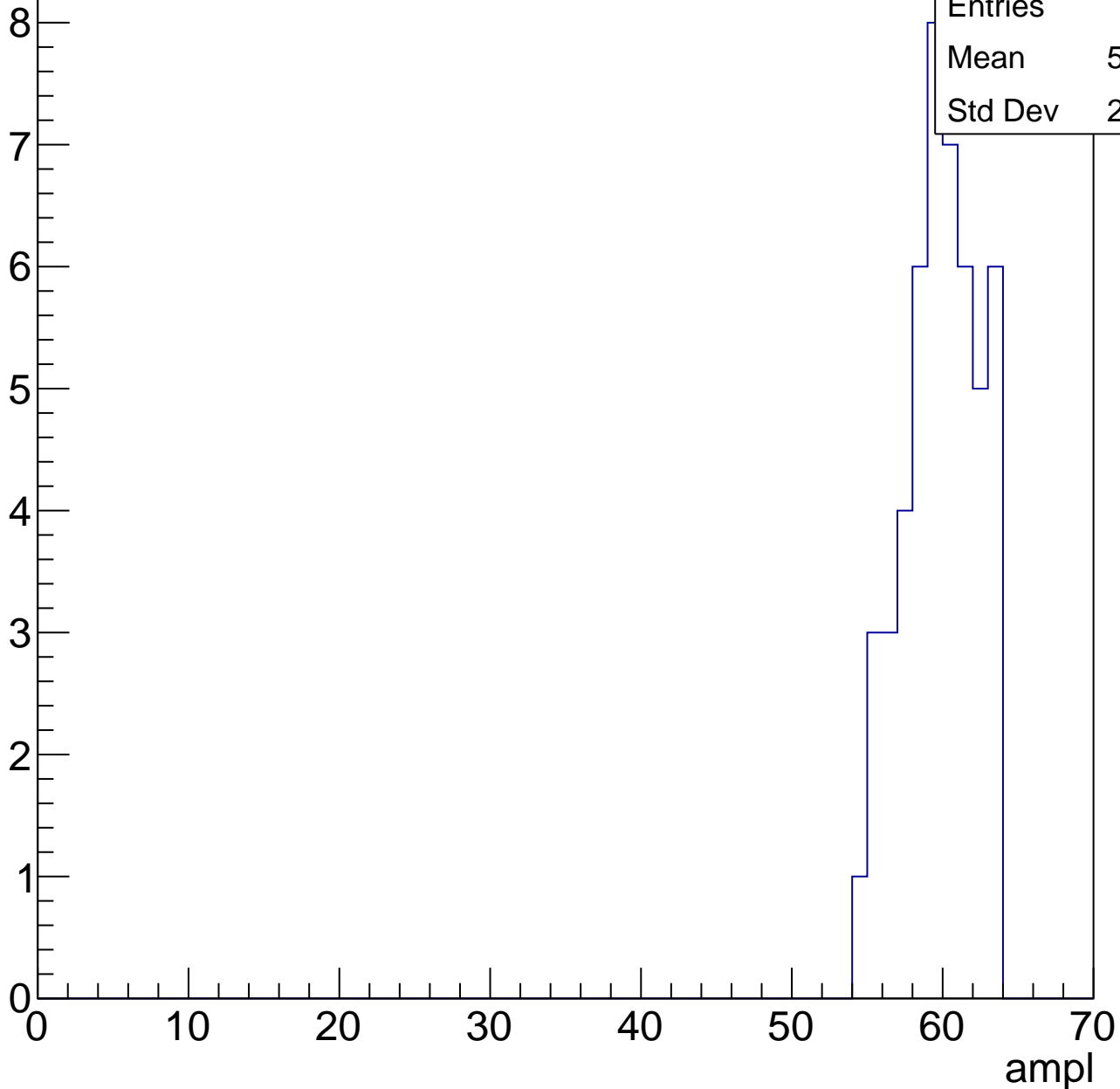


B1L103S, U23-ch115, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

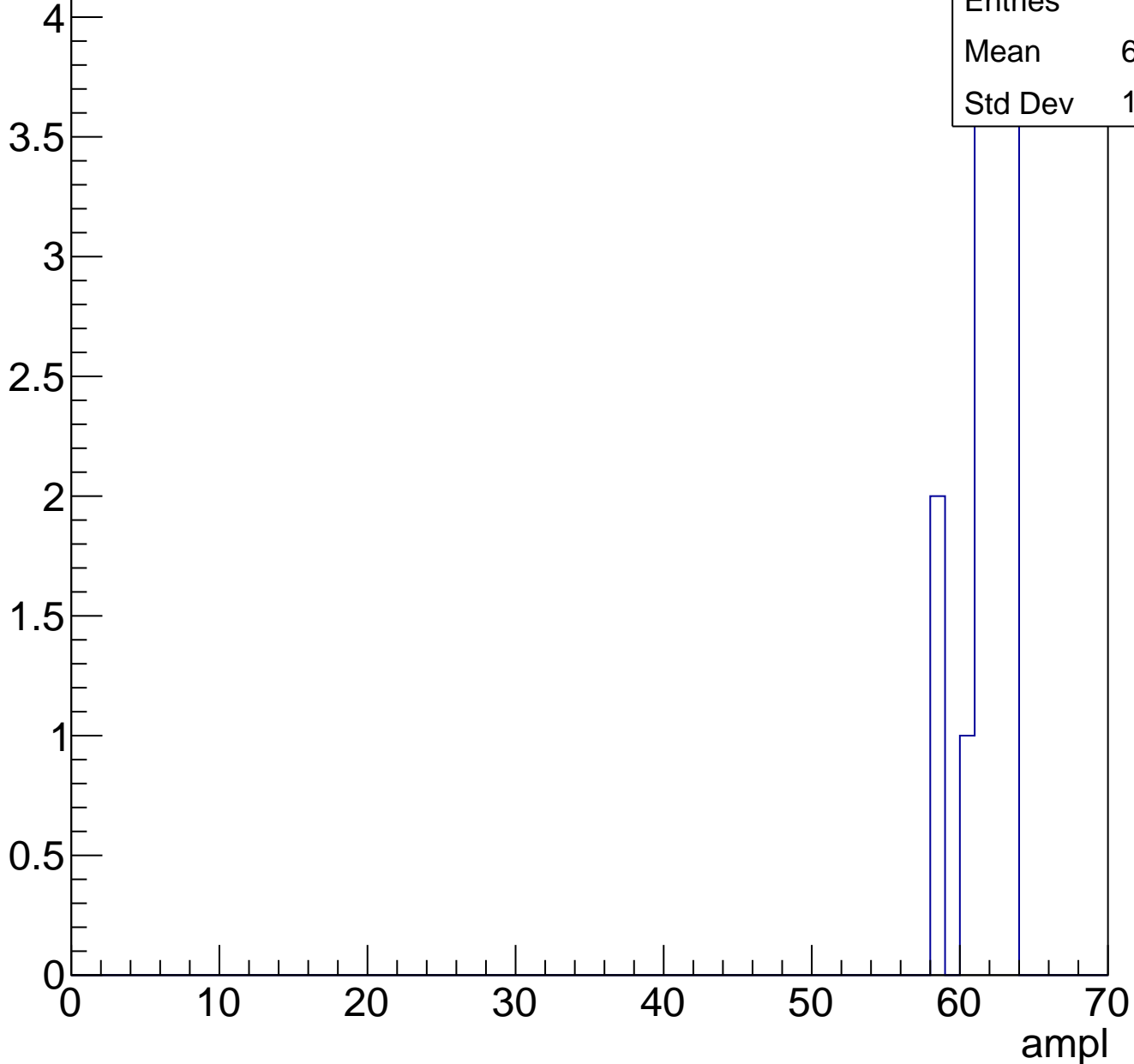
Entries	49
Mean	59.37
Std Dev	2.422



B1L103S, U23-ch115, adc6

calib_packv5_041523_1651.root, FC#0, port C2

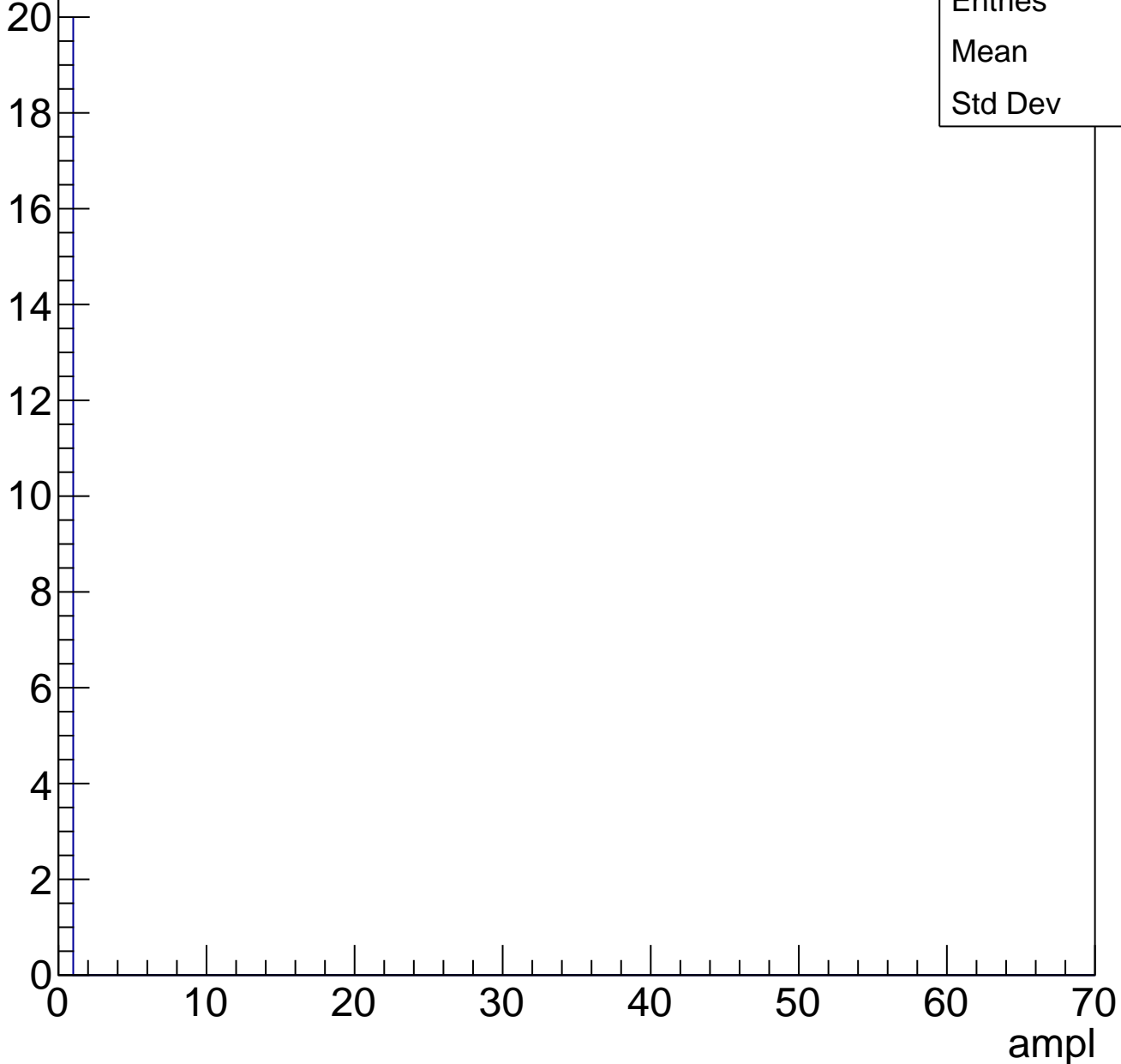
Entry



B1L103S, U23-ch115, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	20
Mean	0
Std Dev	0

B1L103S, U23-ch116, adc0

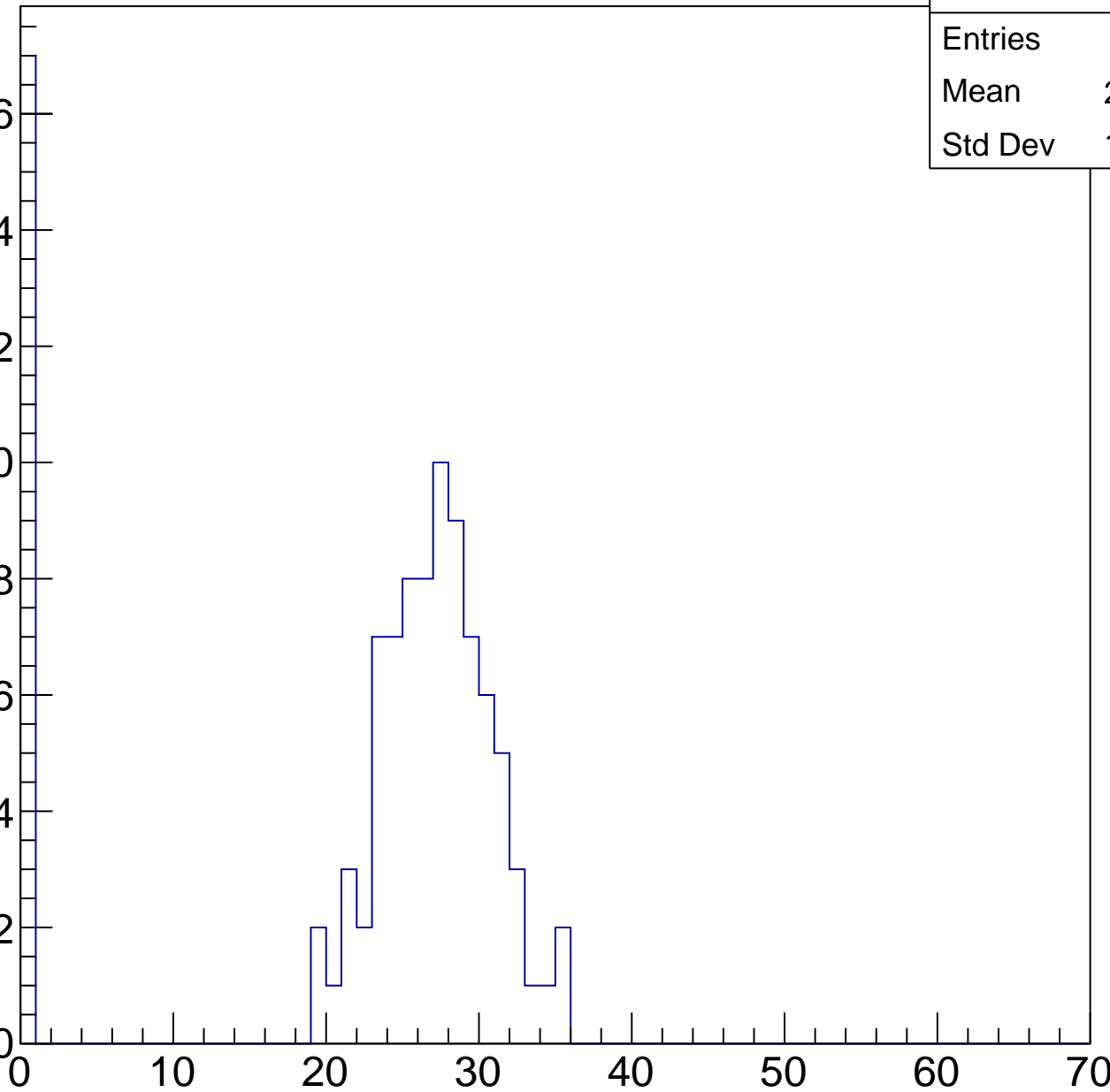
calib_packv5_041523_1651.root, FC#0, port C2

Entries	99
Mean	22.17
Std Dev	10.59

Entry

16
14
12
10
8
6
4
2
0

ampl



B1L103S, U23-ch116, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	77
Mean	29.31
Std Dev	12.45

Entry

10

8

6

4

2

0

0

10

20

30

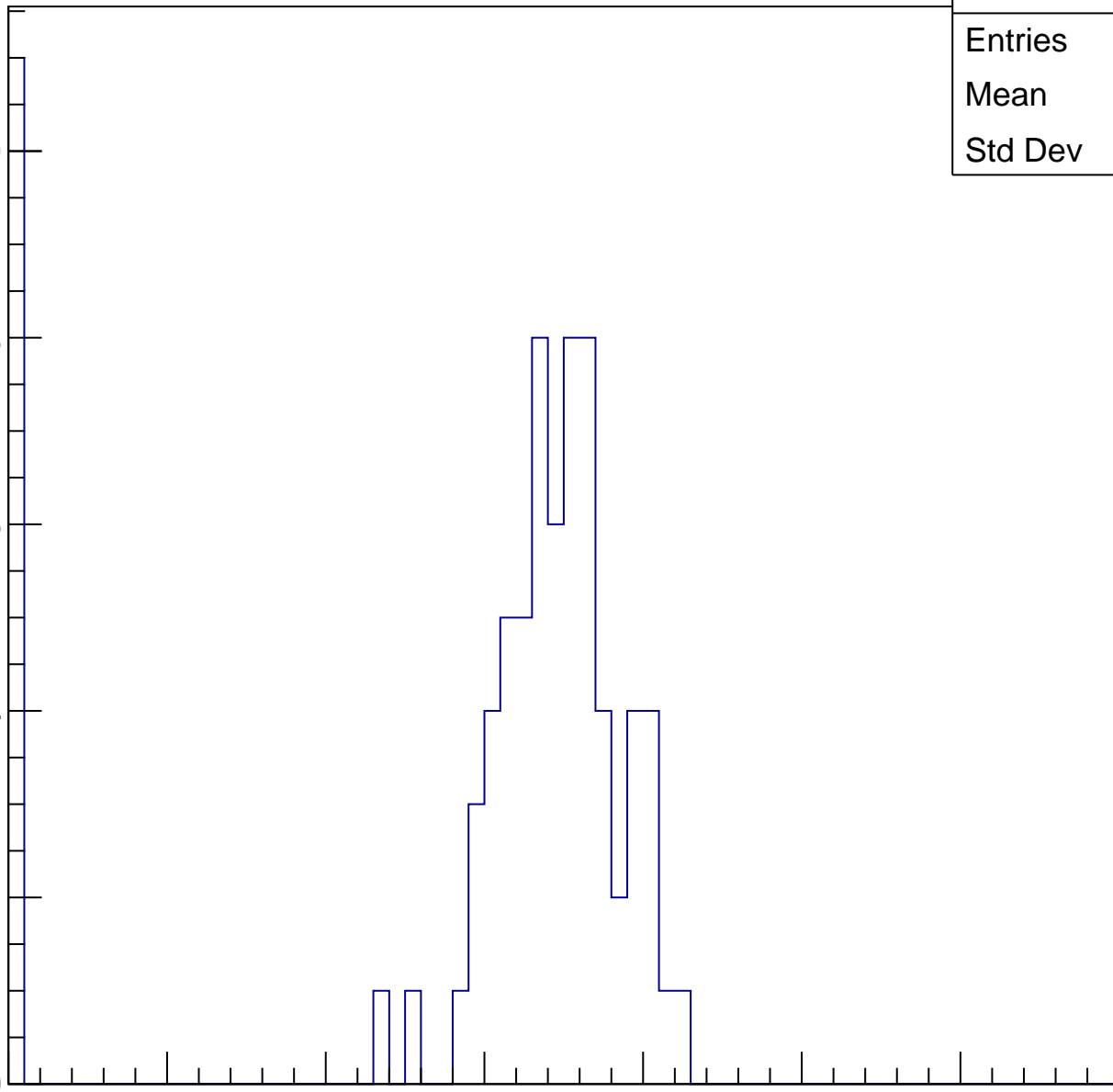
40

50

60

70

ampl

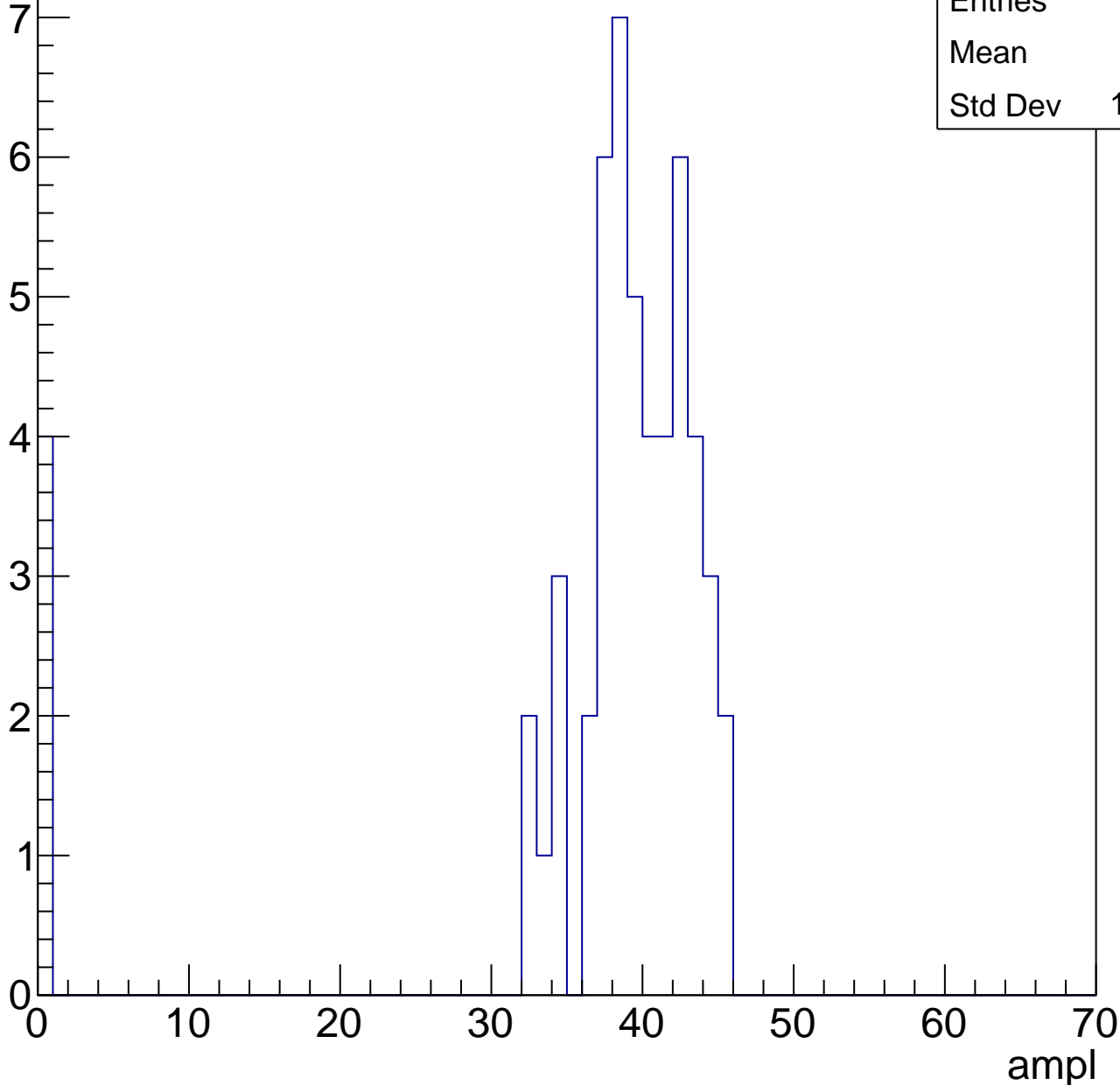


B1L103S, U23-ch116, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	53
Mean	36.3
Std Dev	10.85

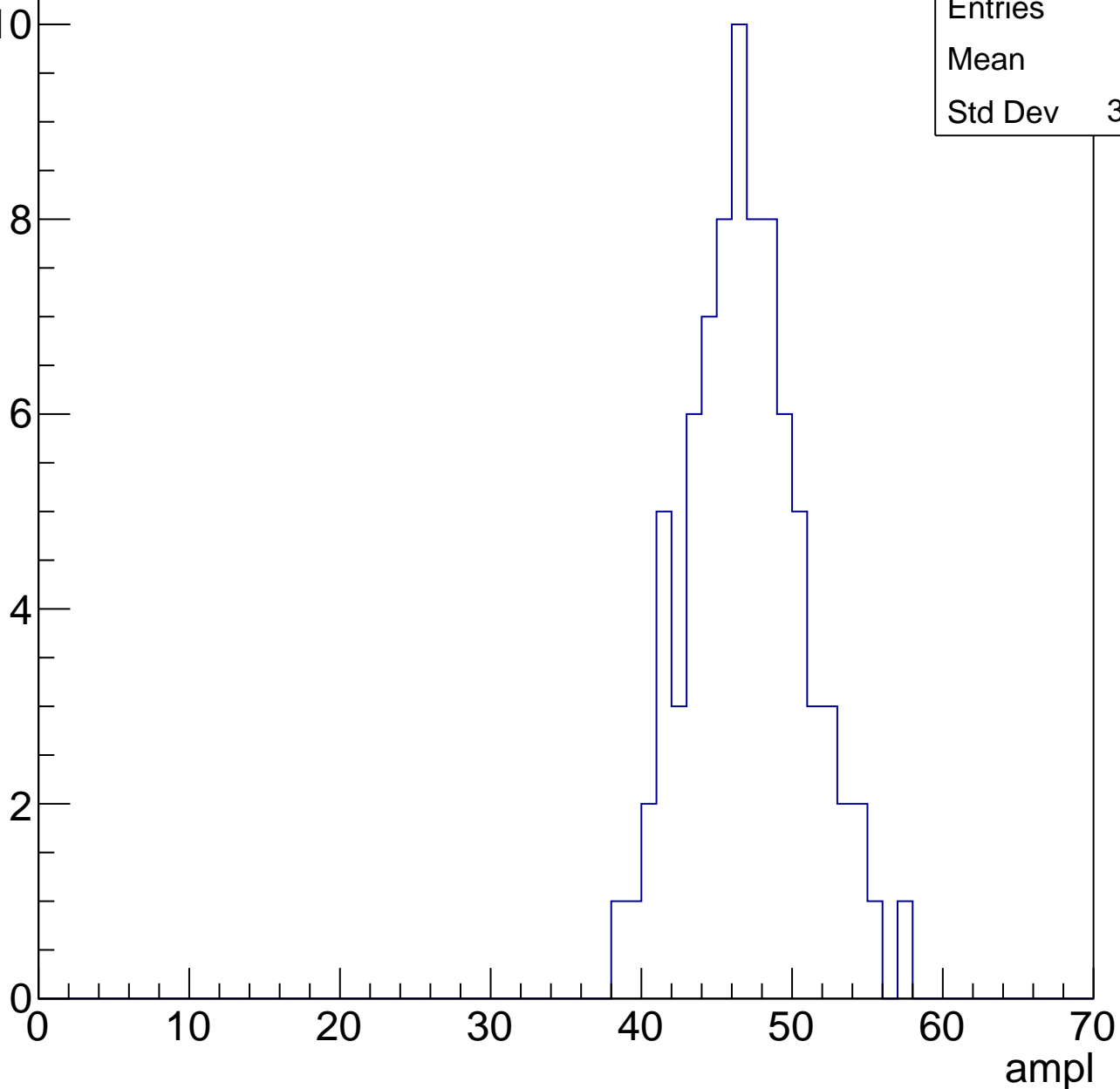


B1L103S, U23-ch116, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	82
Mean	46.5
Std Dev	3.845

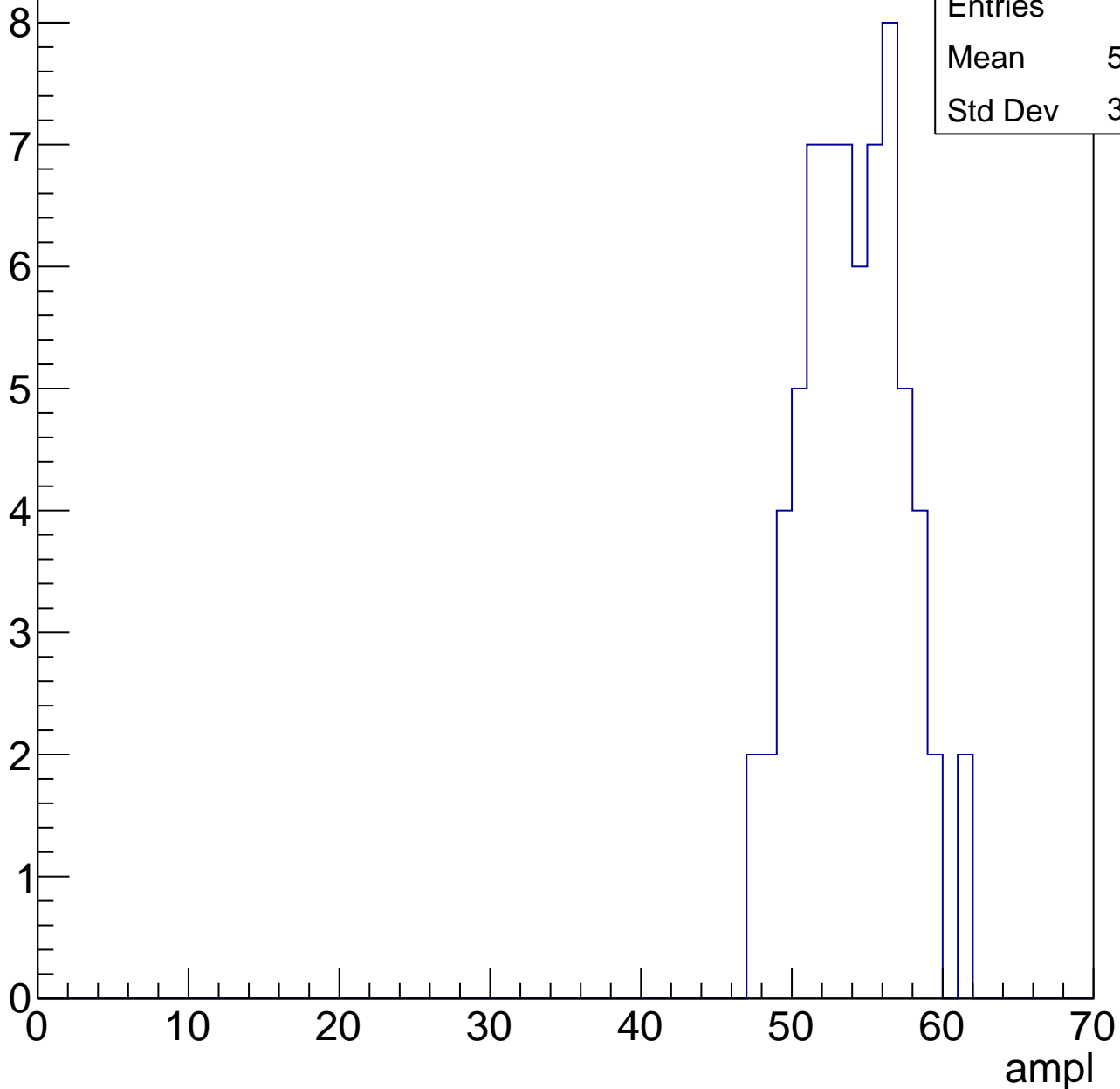


B1L103S, U23-ch116, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	53.56
Std Dev	3.278

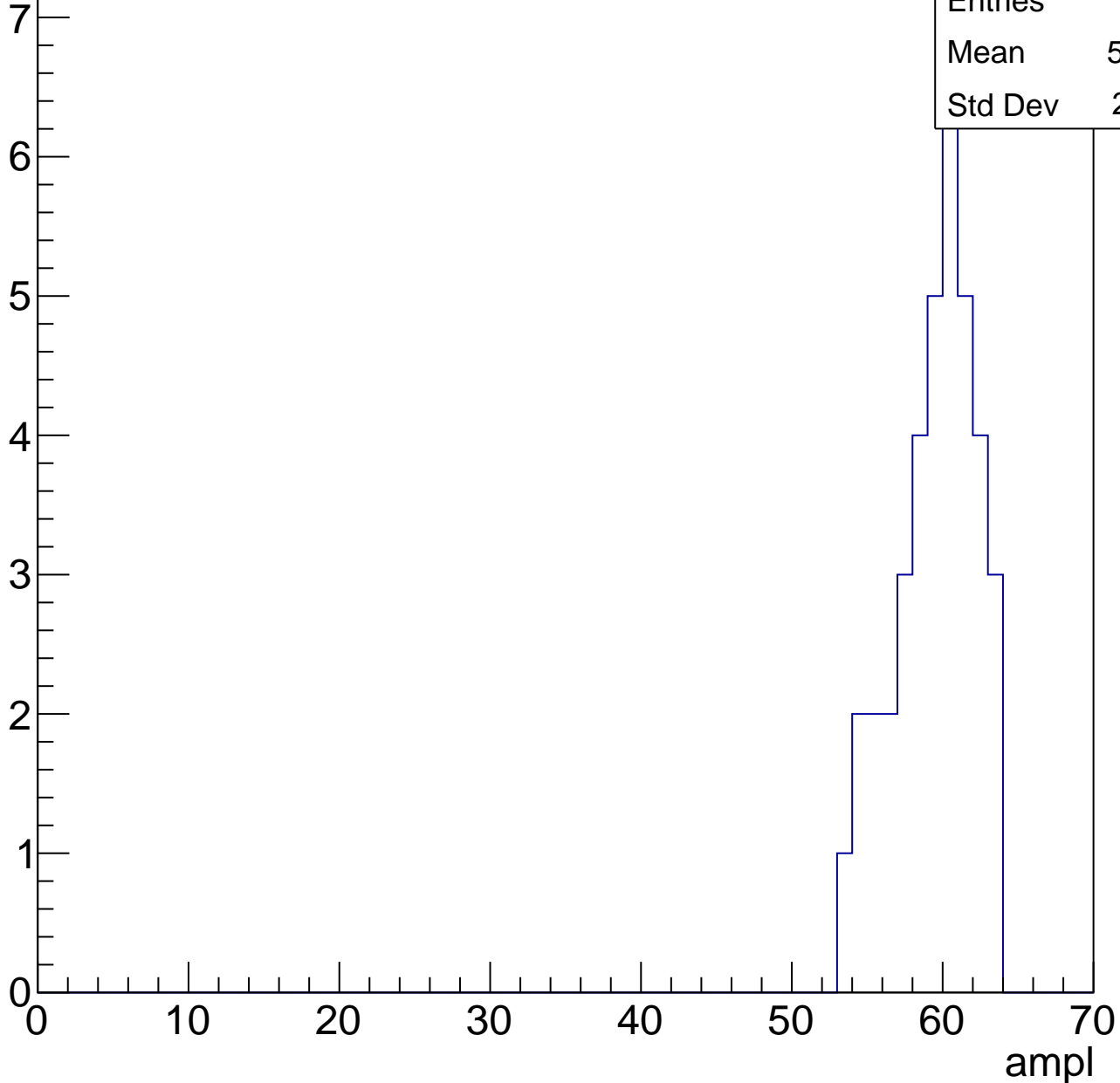


B1L103S, U23-ch116, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	38
Mean	59.03
Std Dev	2.631

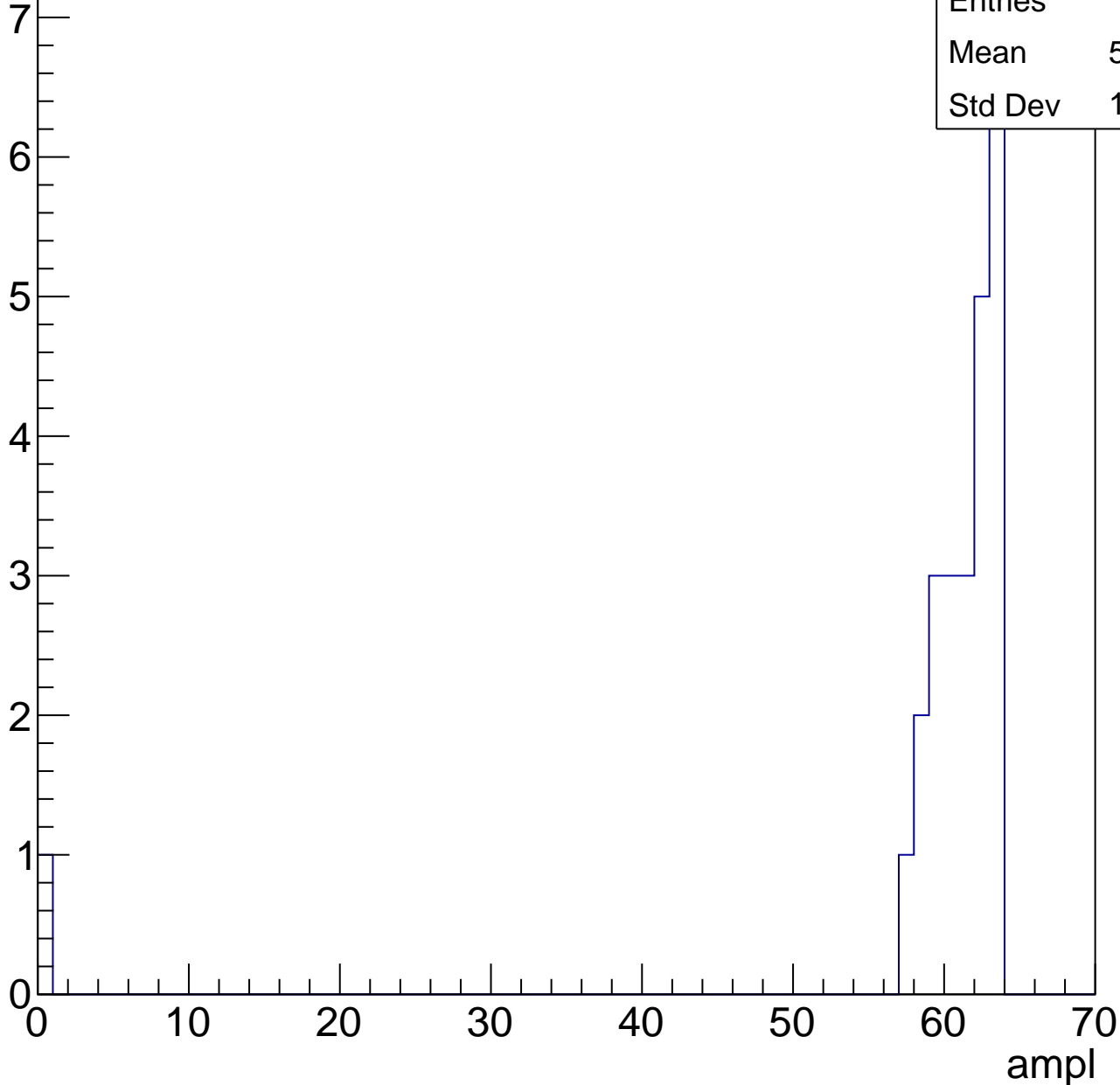


B1L103S, U23-ch116, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	25
Mean	58.56
Std Dev	12.09



B1L103S, U23-ch116, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.1
Std Dev	13.51

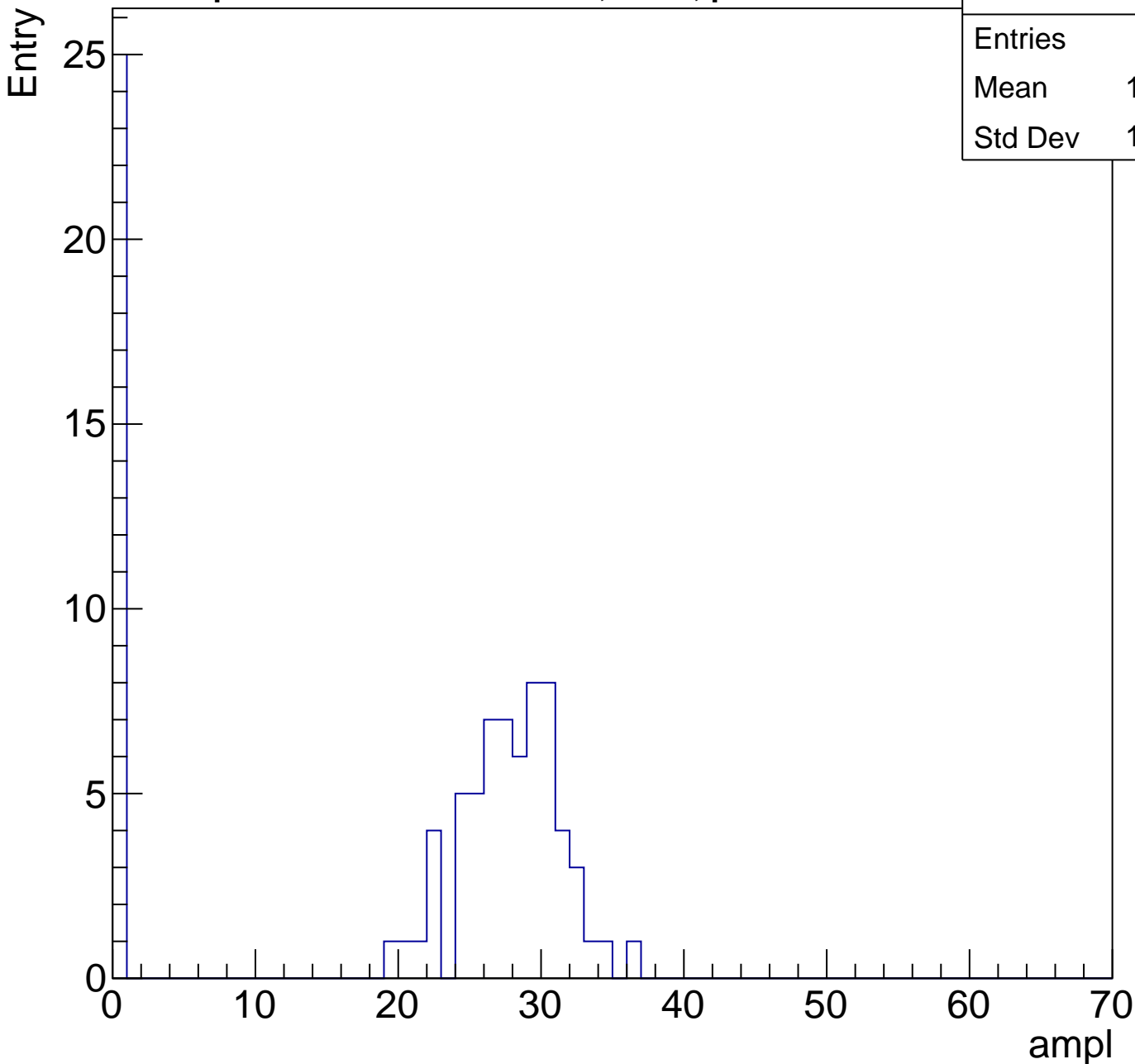
Entry



B1L103S, U23-ch117, adc0

calib_packv5_041523_1651.root, FC#0, port C2

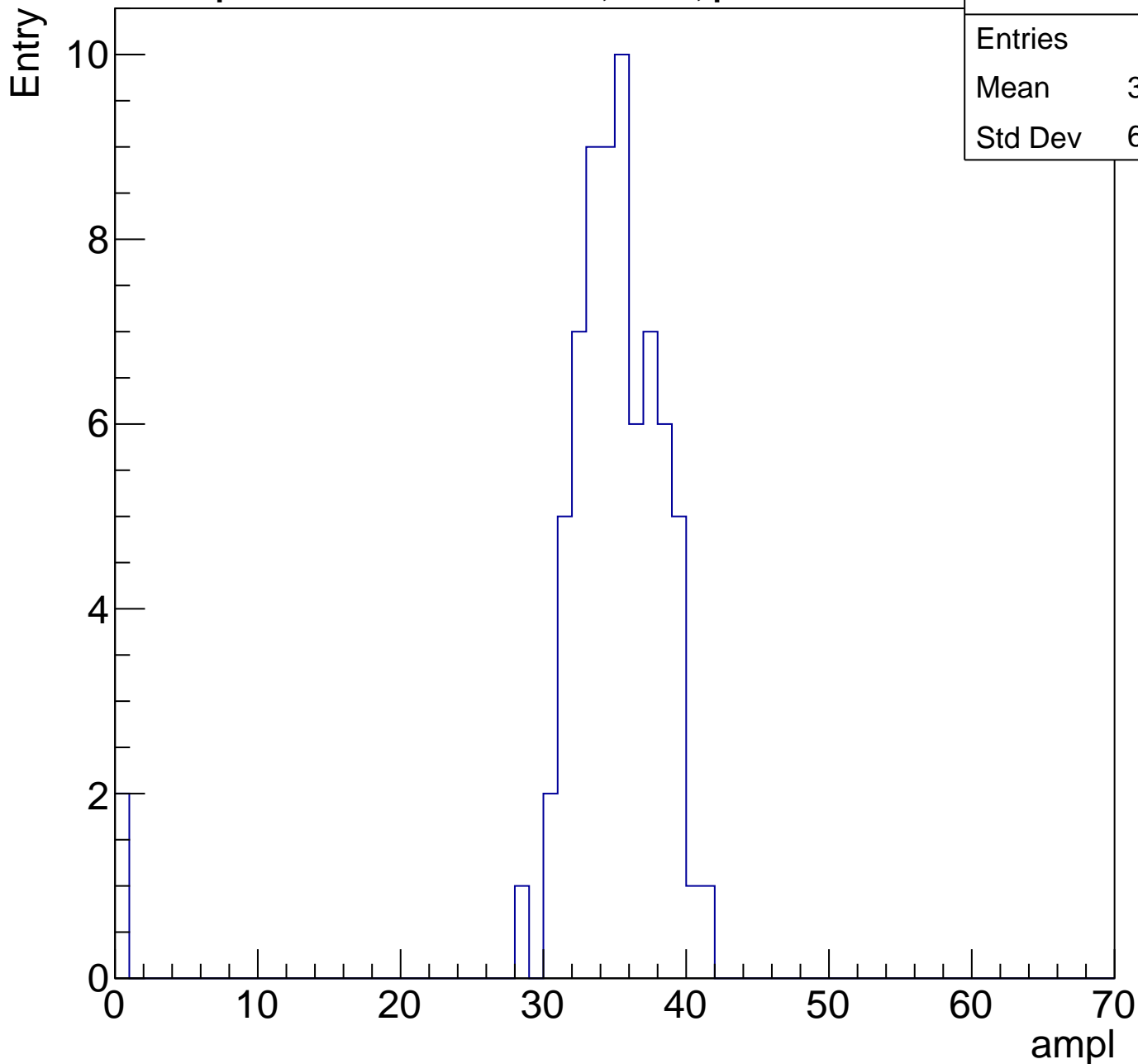
Entries	88
Mean	19.62
Std Dev	12.69



B1L103S, U23-ch117, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	71
Mean	33.79
Std Dev	6.349



B1L103S, U23-ch117, adc2

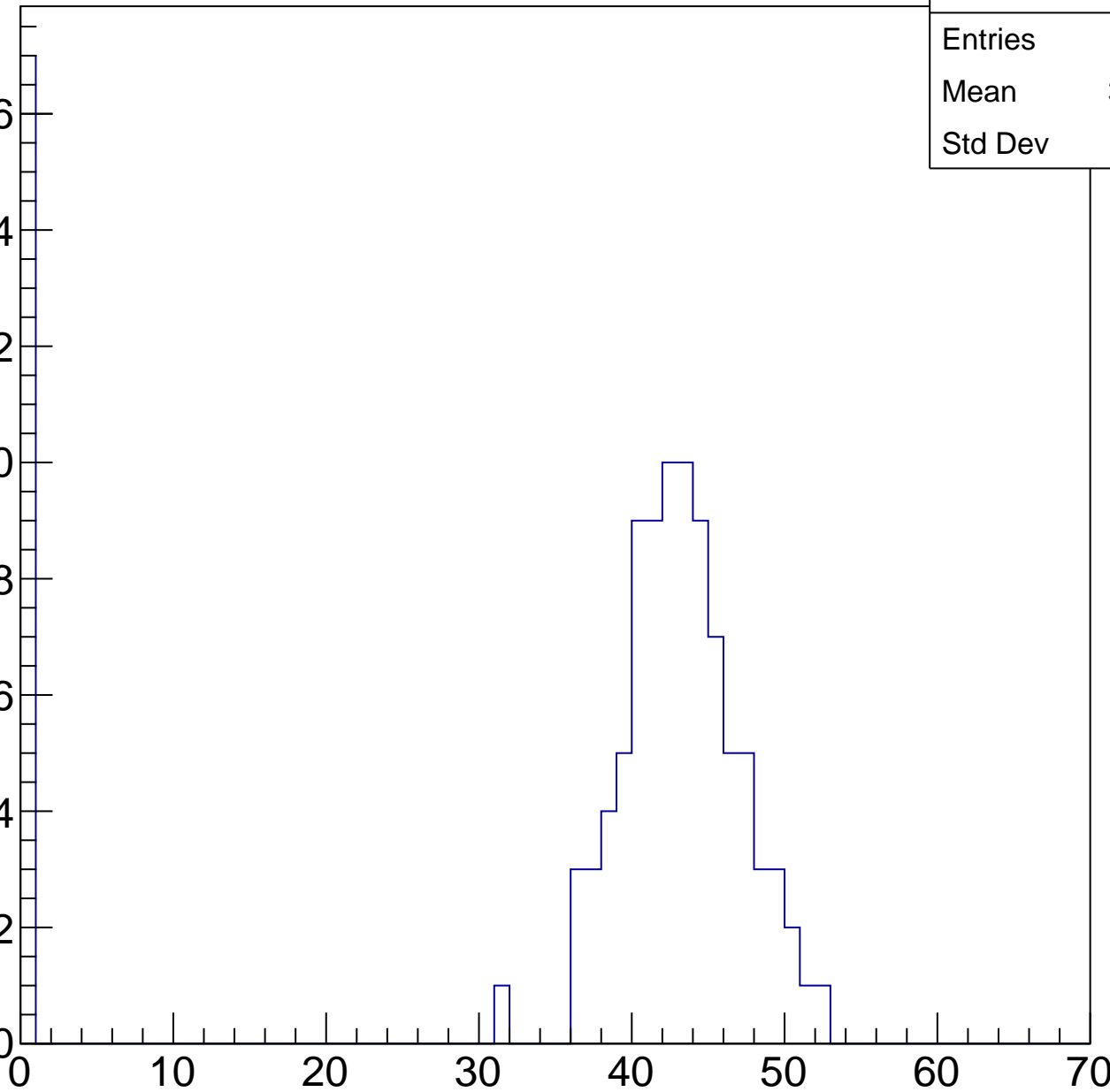
calib_packv5_041523_1651.root, FC#0, port C2

Entries	107
Mean	35.94
Std Dev	16

Entry

16
14
12
10
8
6
4
2
0

ampl

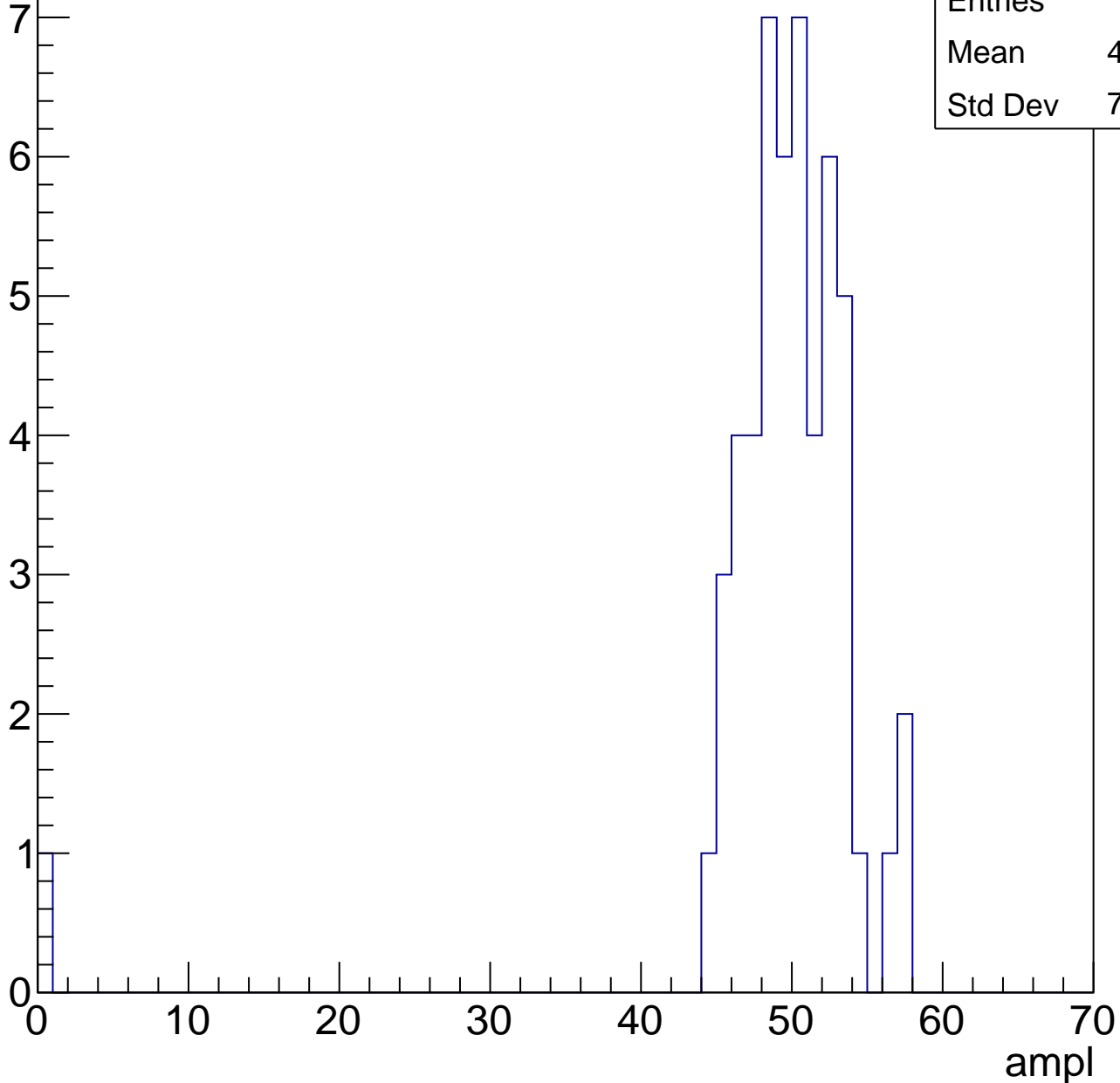


B1L103S, U23-ch117, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	52
Mean	48.77
Std Dev	7.454

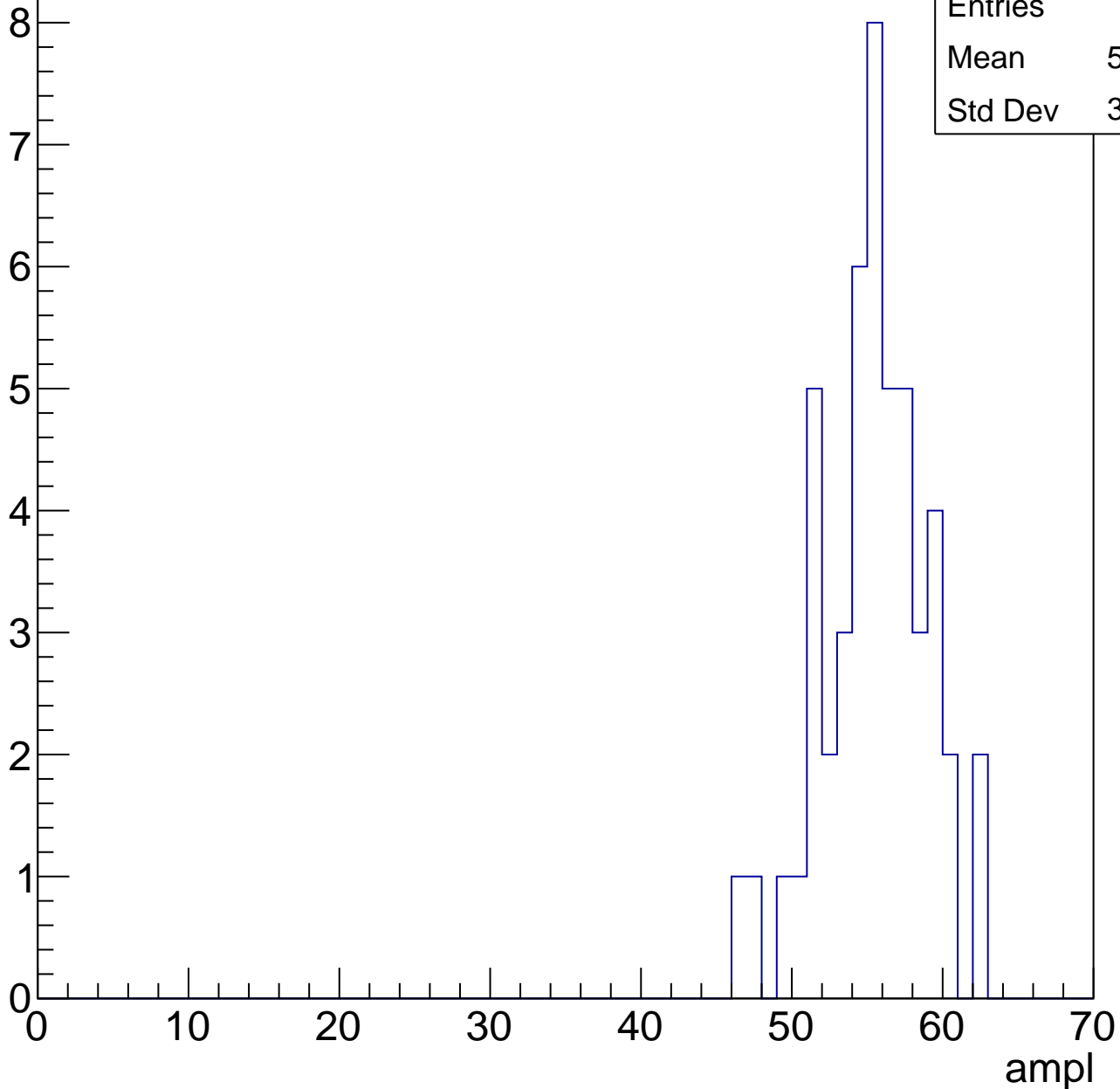


B1L103S, U23-ch117, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	49
Mean	54.96
Std Dev	3.458

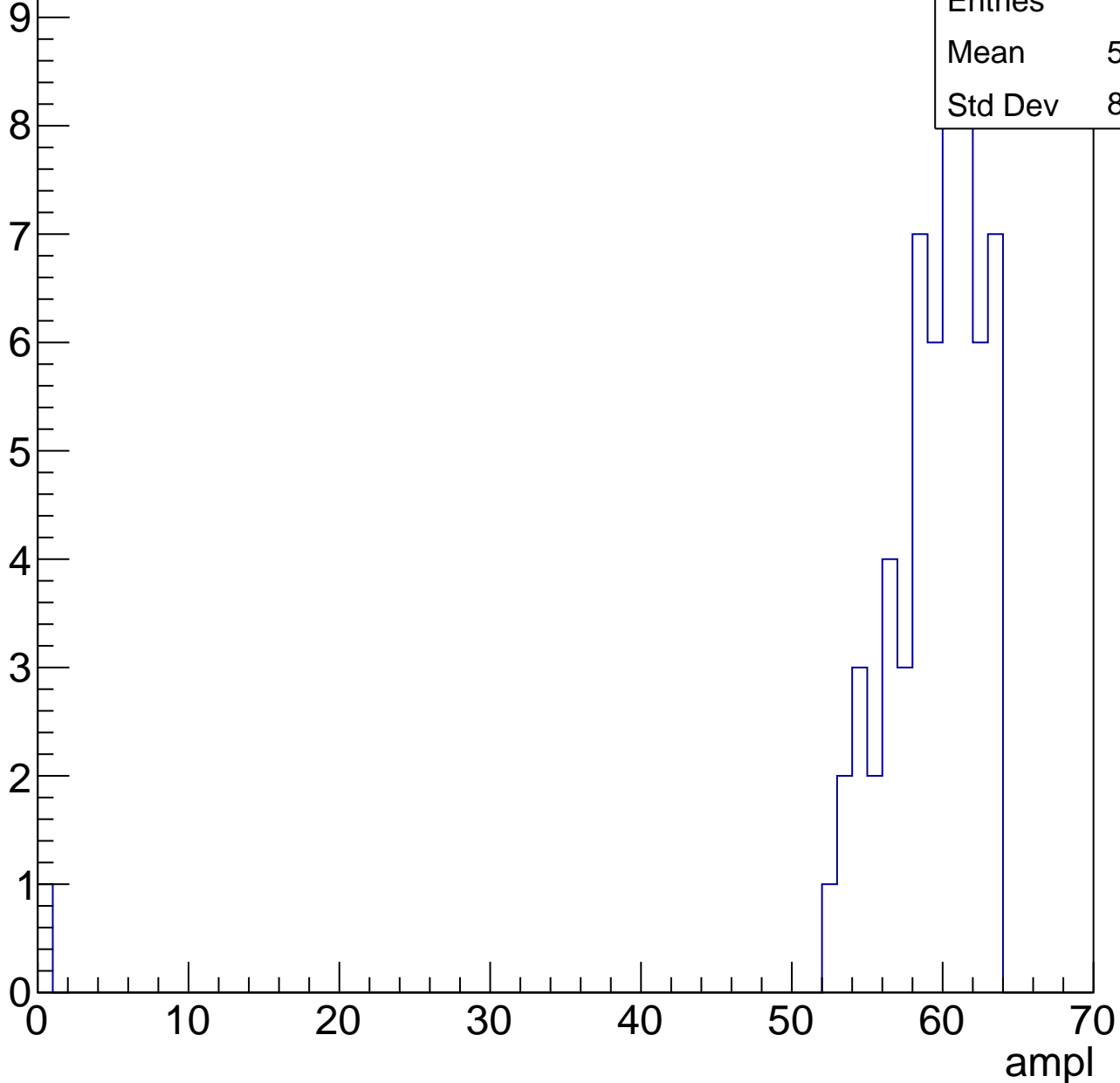


B1L103S, U23-ch117, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	58.08
Std Dev	8.156



B1L103S, U23-ch117, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch117, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

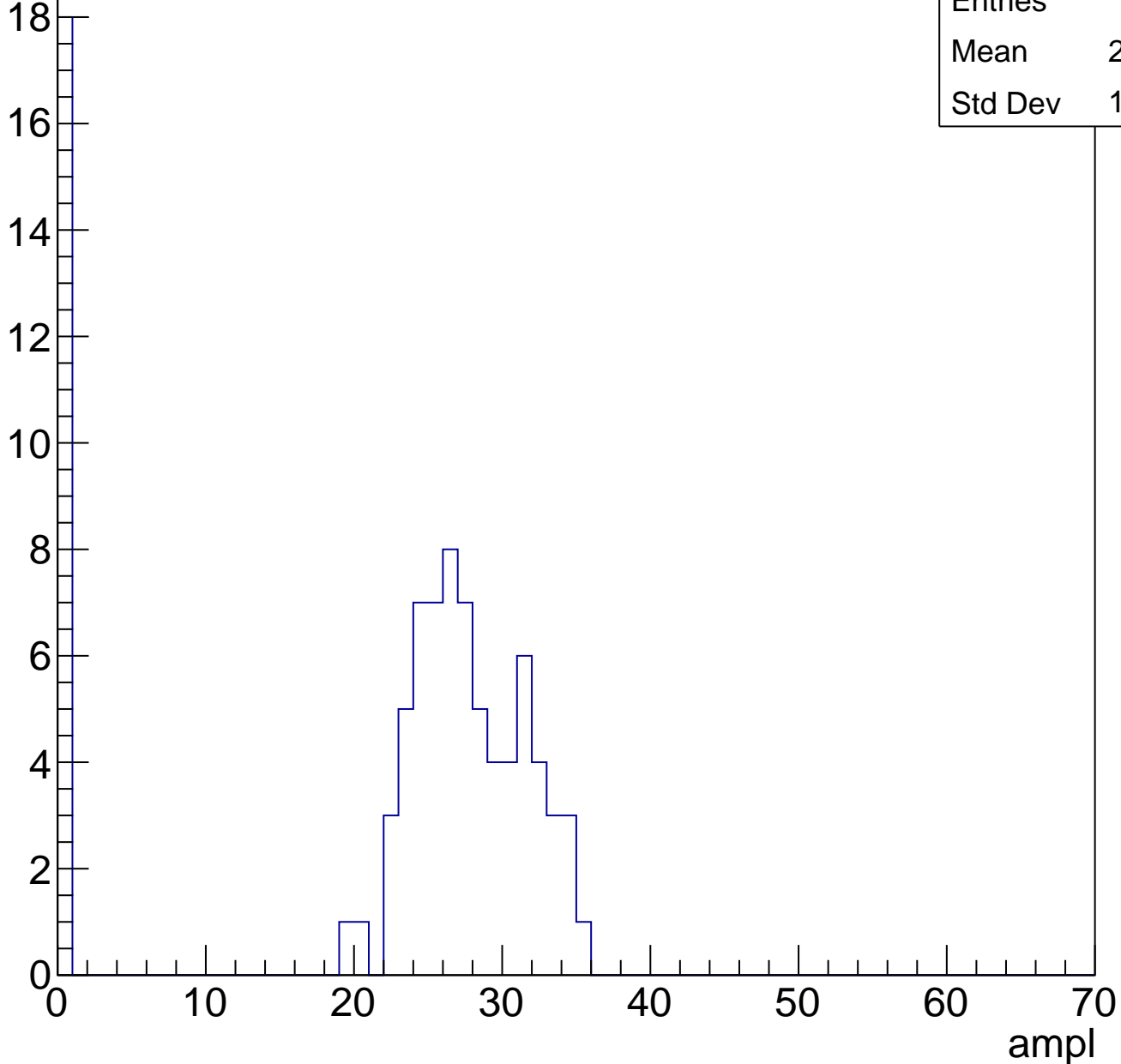
ampl

B1L103S, U23-ch118, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	87
Mean	21.68
Std Dev	11.55

Entry

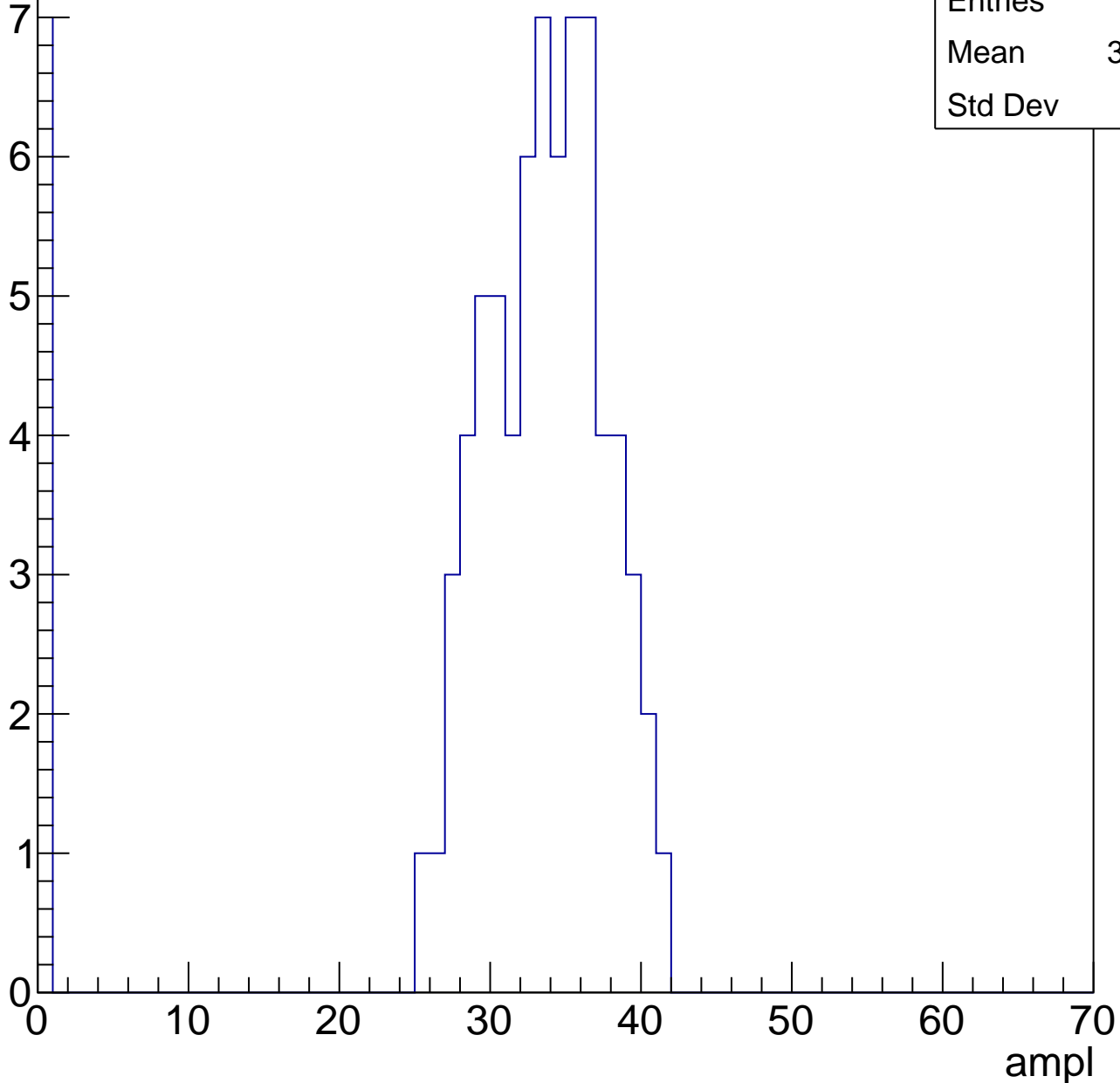


B1L103S, U23-ch118, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	77
Mean	30.19
Std Dev	10.2

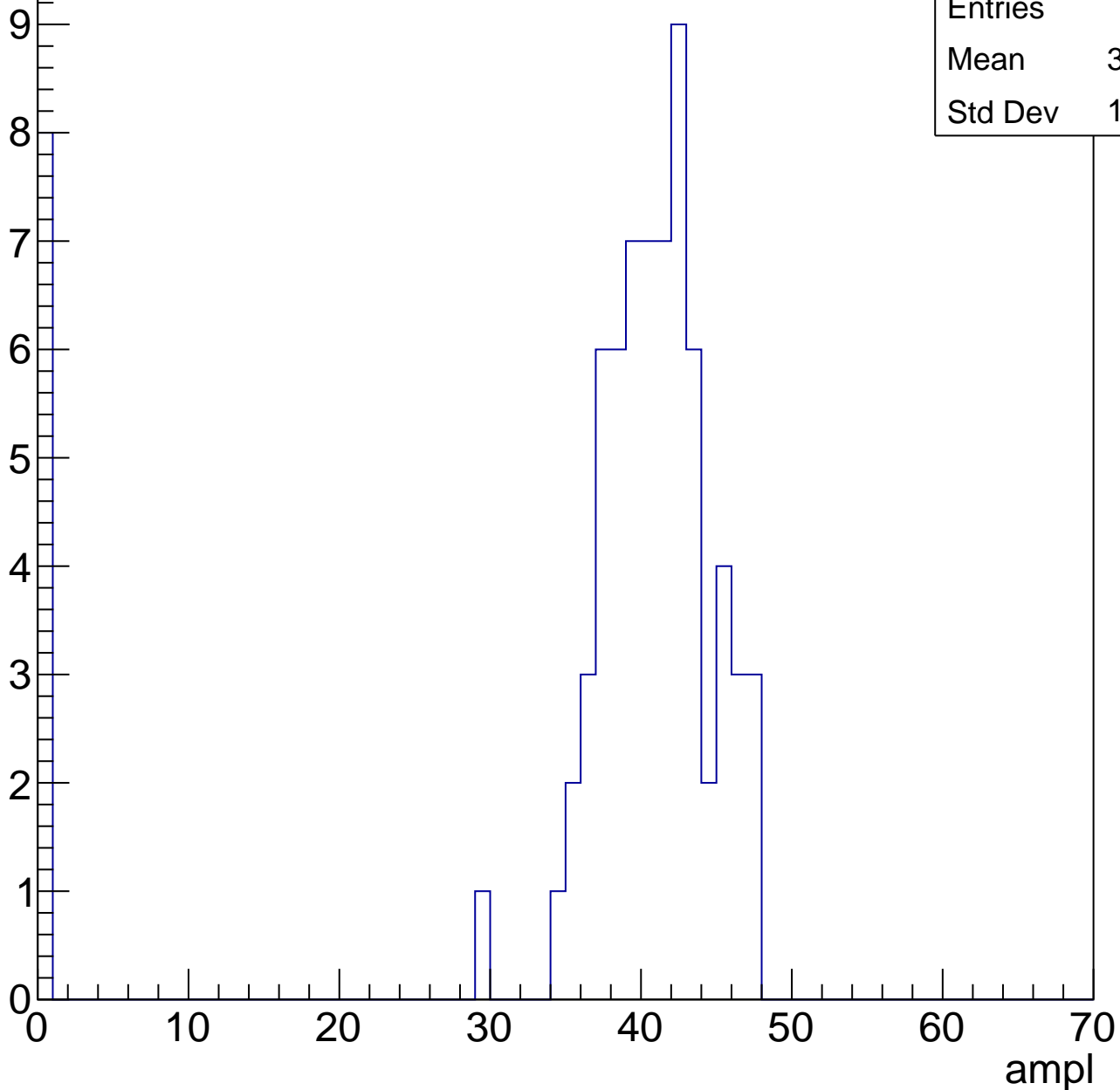


B1L103S, U23-ch118, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	75
Mean	36.19
Std Dev	12.93

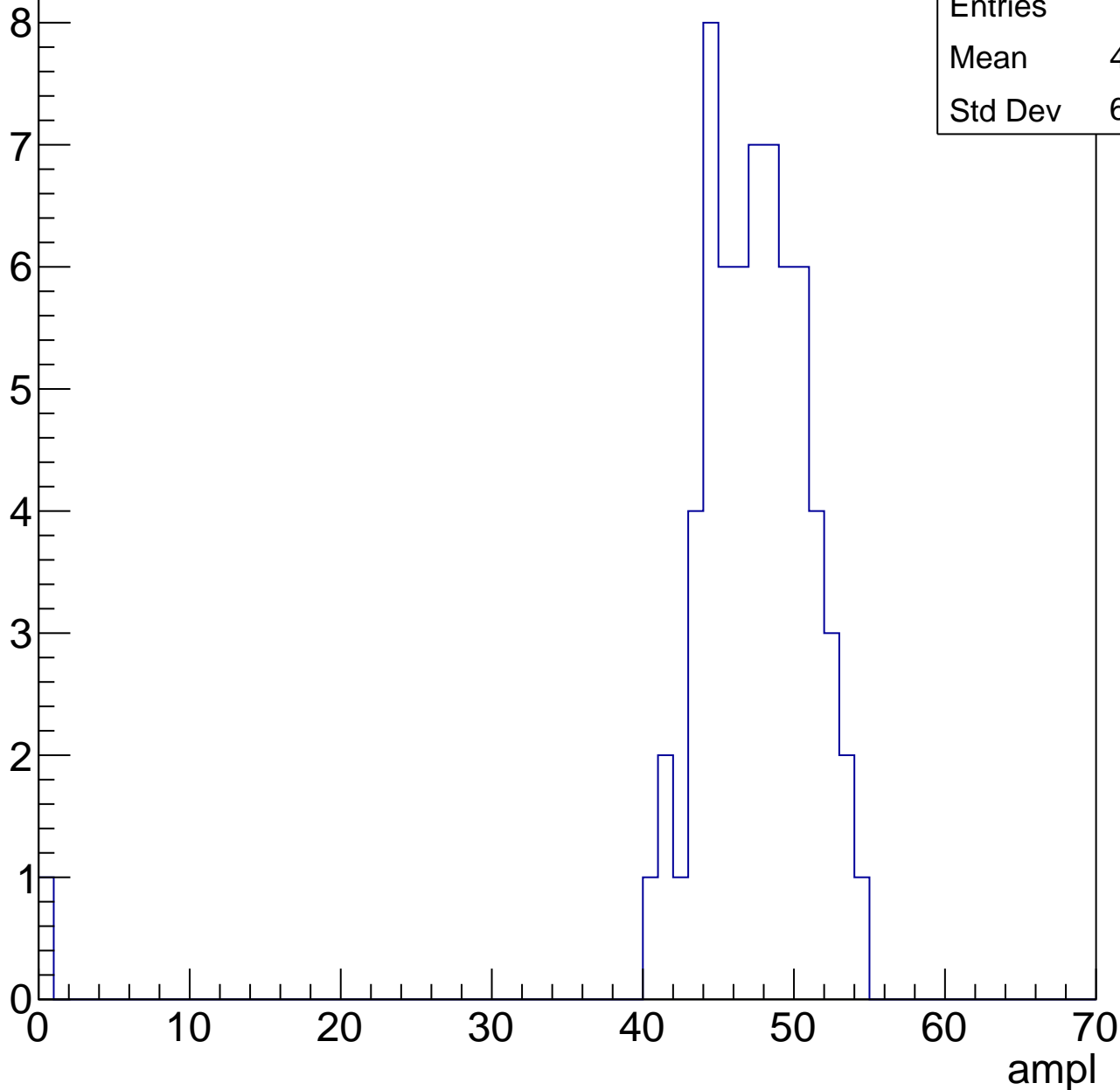


B1L103S, U23-ch118, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	46.35
Std Dev	6.609

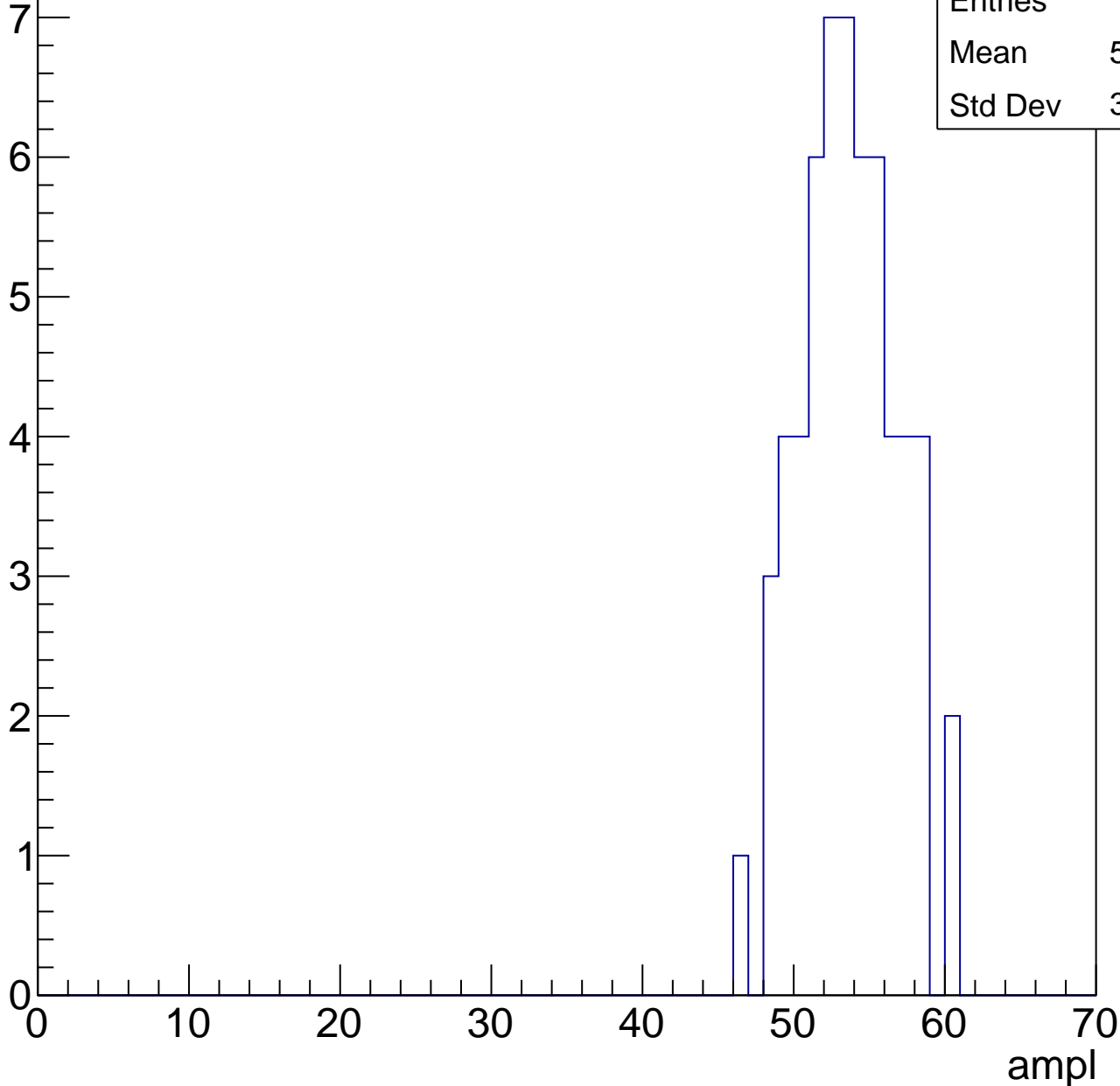


B1L103S, U23-ch118, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	53.19
Std Dev	3.165



B1L103S, U23-ch118, adc5

calib_packv5_041523_1651.root, FC#0, port C2

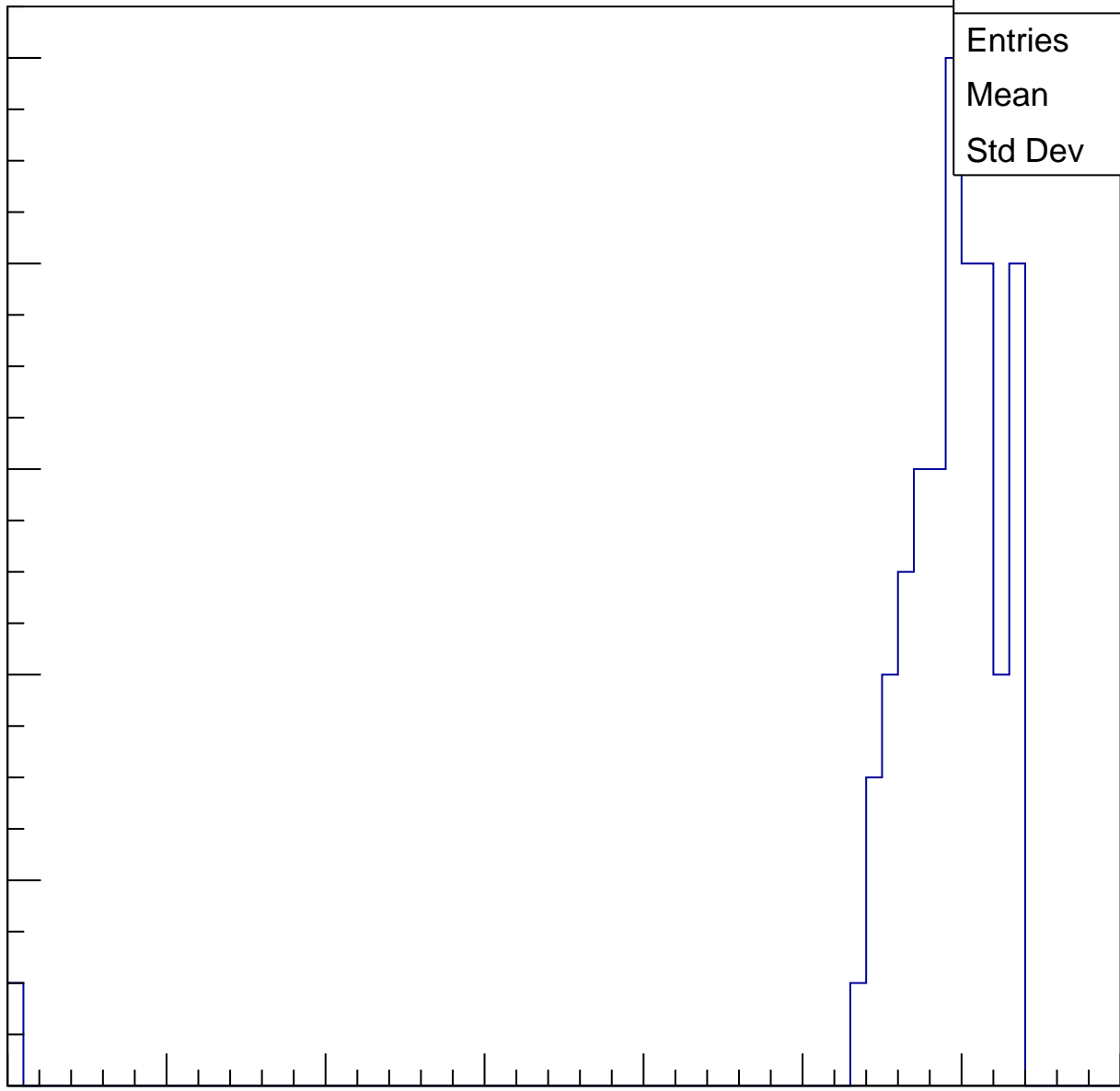
Entries	64
Mean	58.05
Std Dev	7.783

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

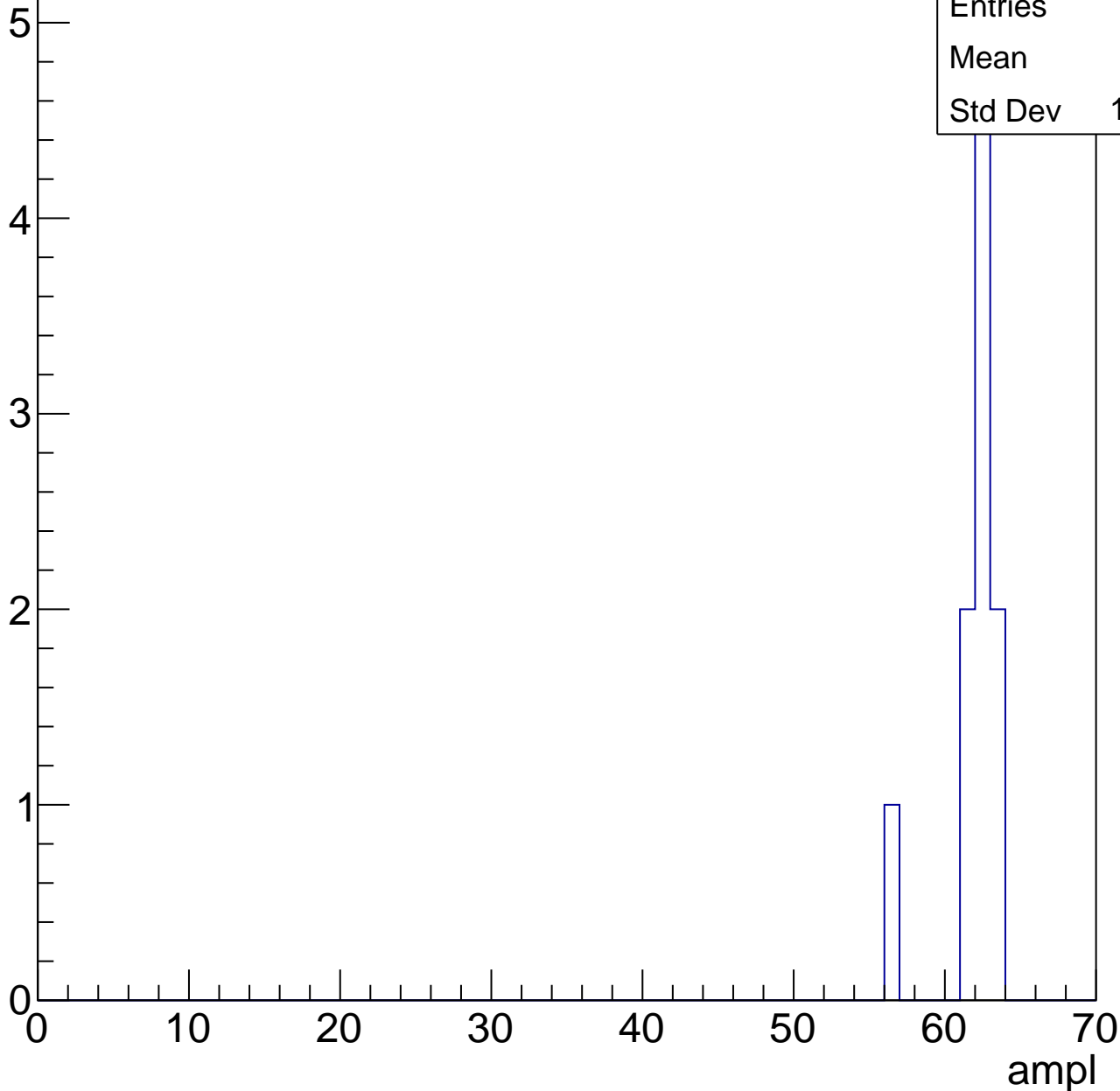


B1L103S, U23-ch118, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

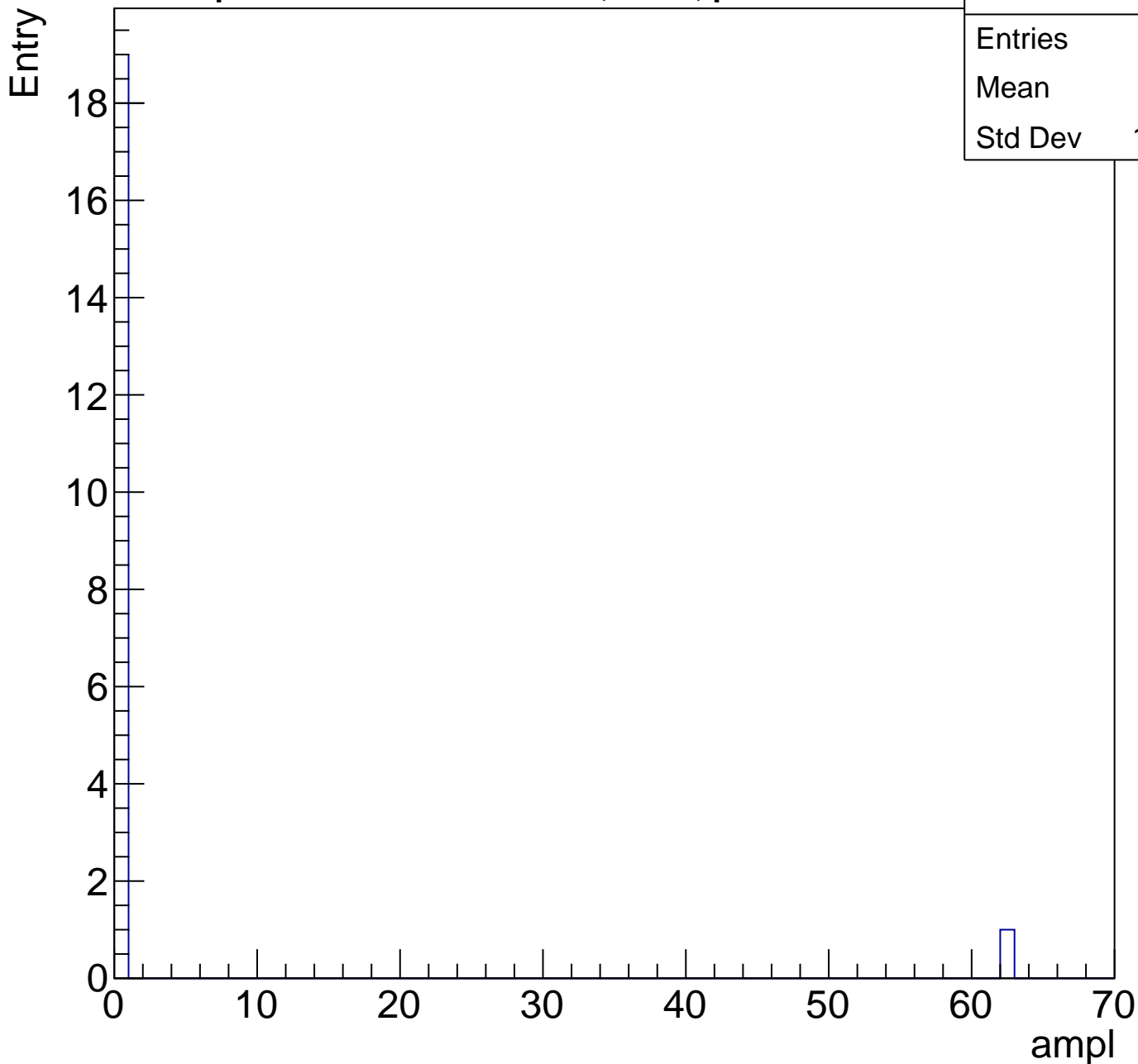
Entries	10
Mean	61.4
Std Dev	1.908



B1L103S, U23-ch118, adc7

calib_packv5_041523_1651.root, FC#0, port C2

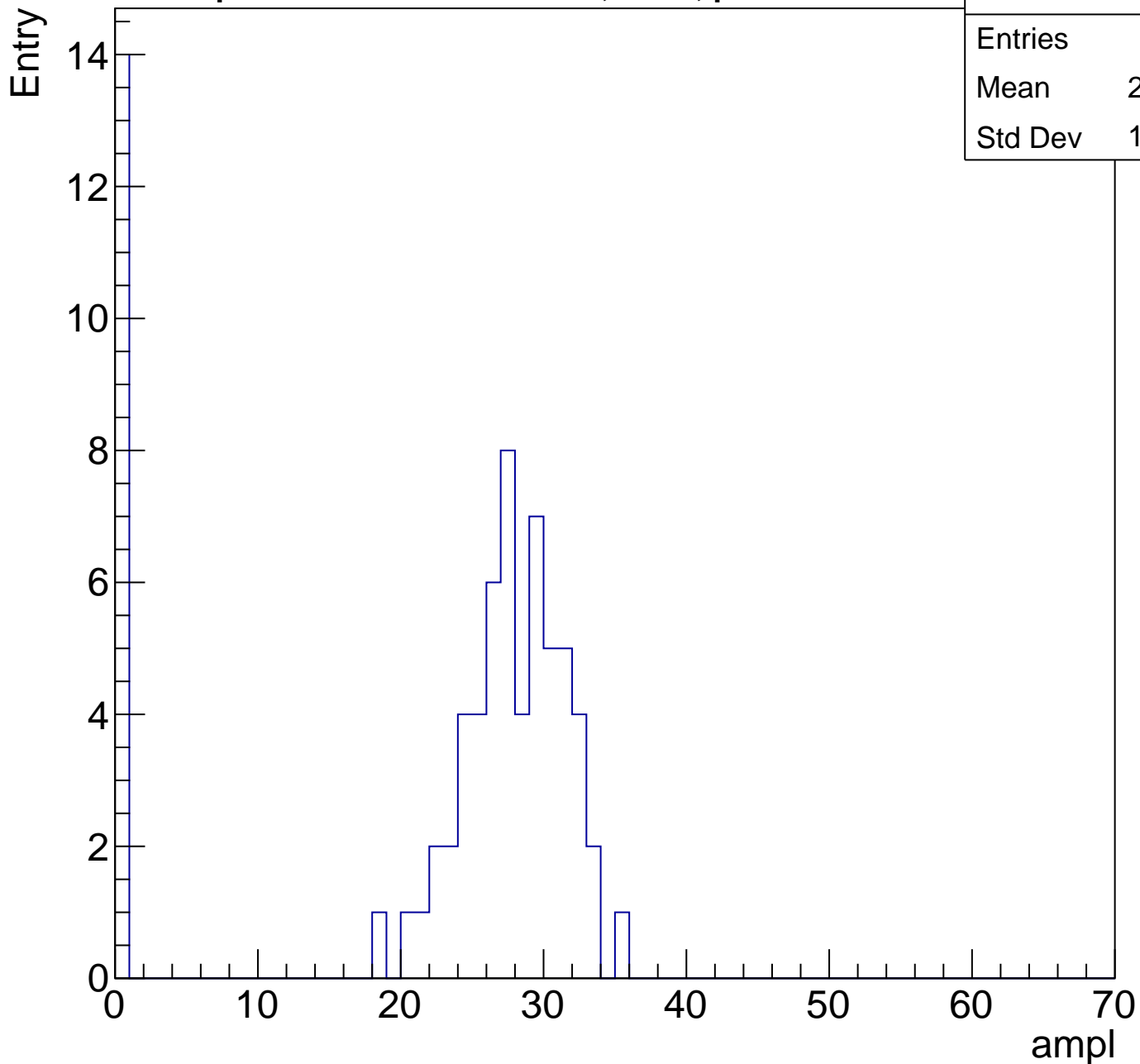
Entries	20
Mean	3.1
Std Dev	13.51



B1L103S, U23-ch119, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	71
Mean	22.06
Std Dev	11.36

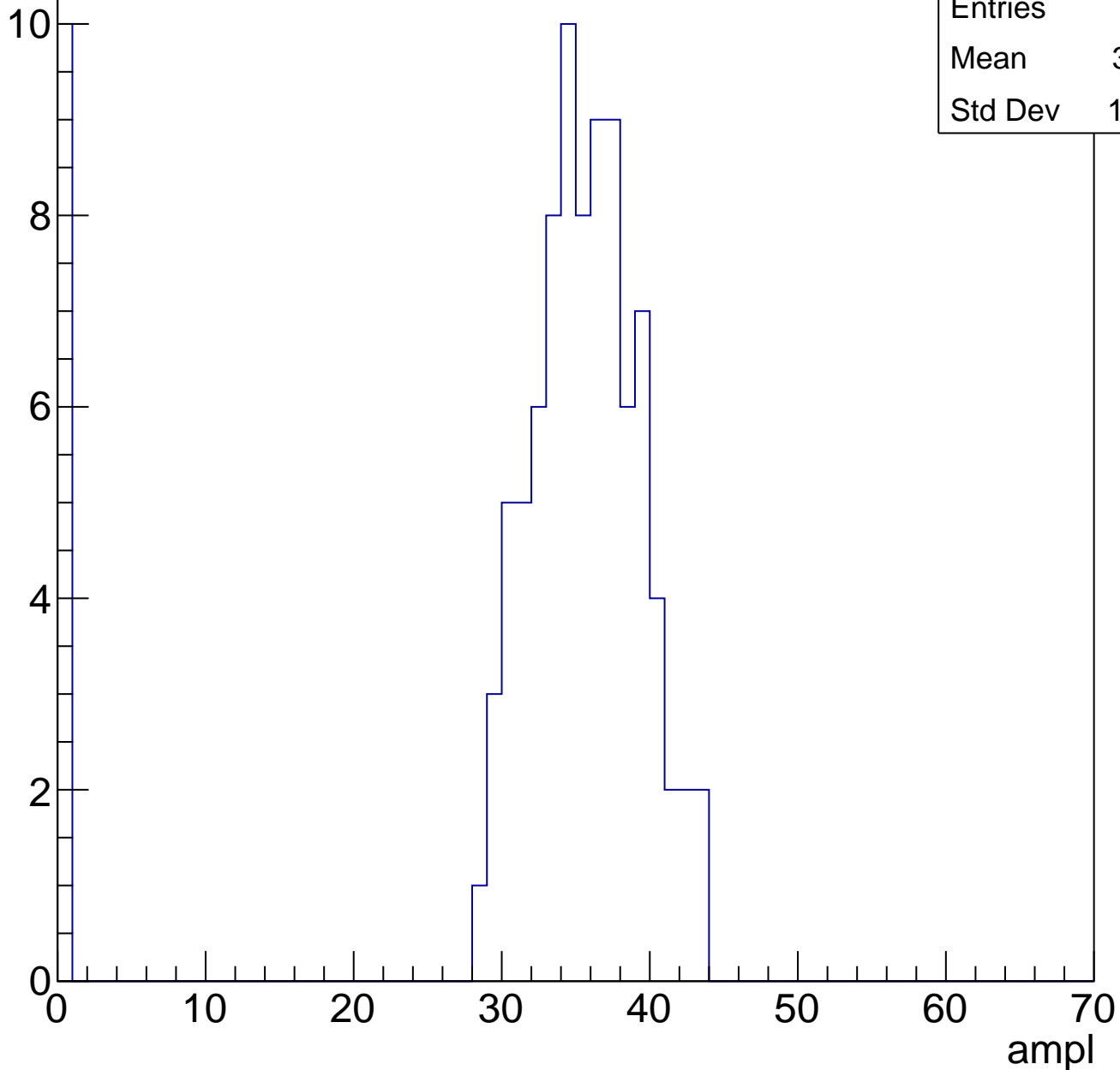


B1L103S, U23-ch119, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	97
Mean	31.61
Std Dev	11.22

Entry

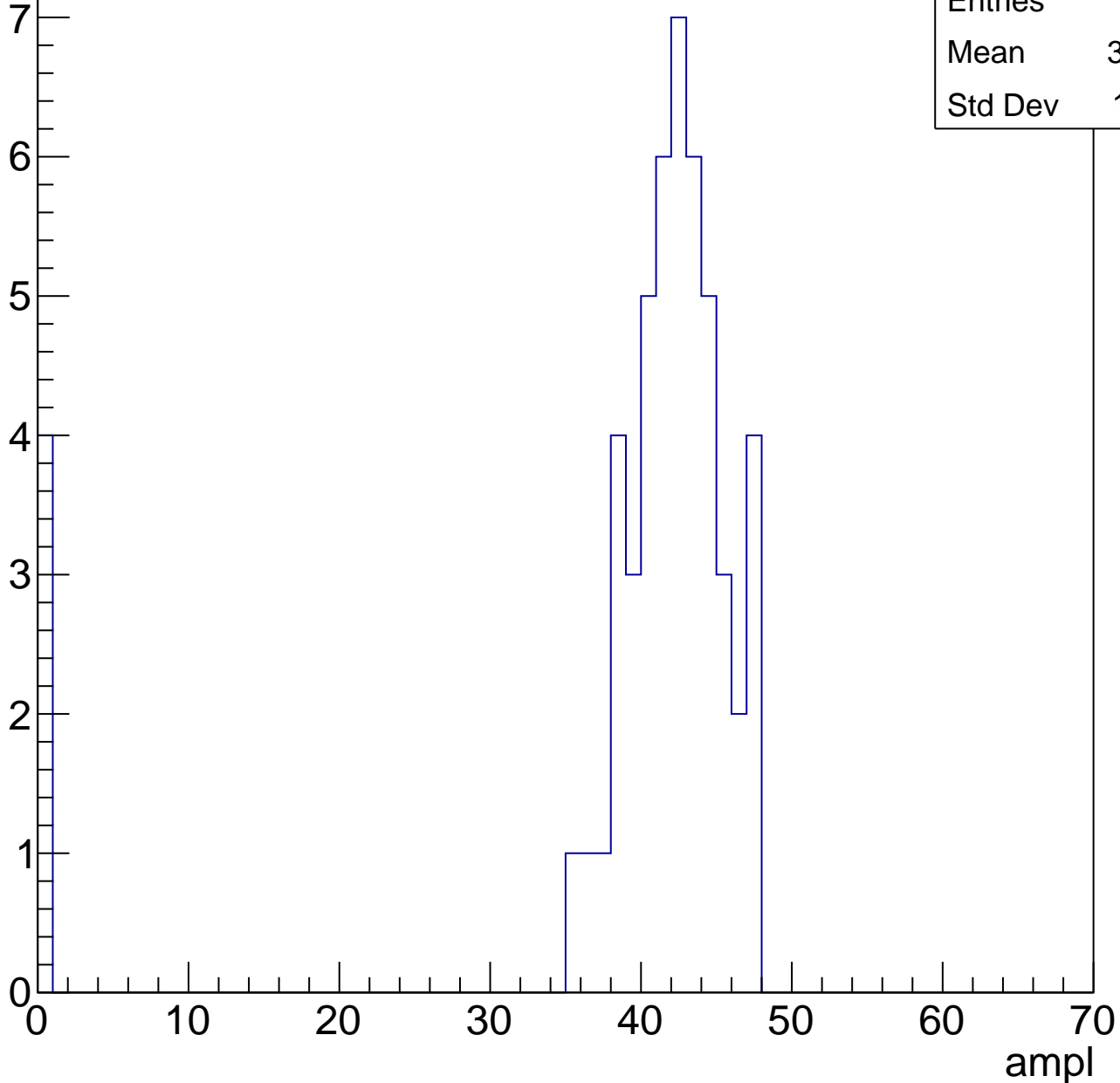


B1L103S, U23-ch119, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

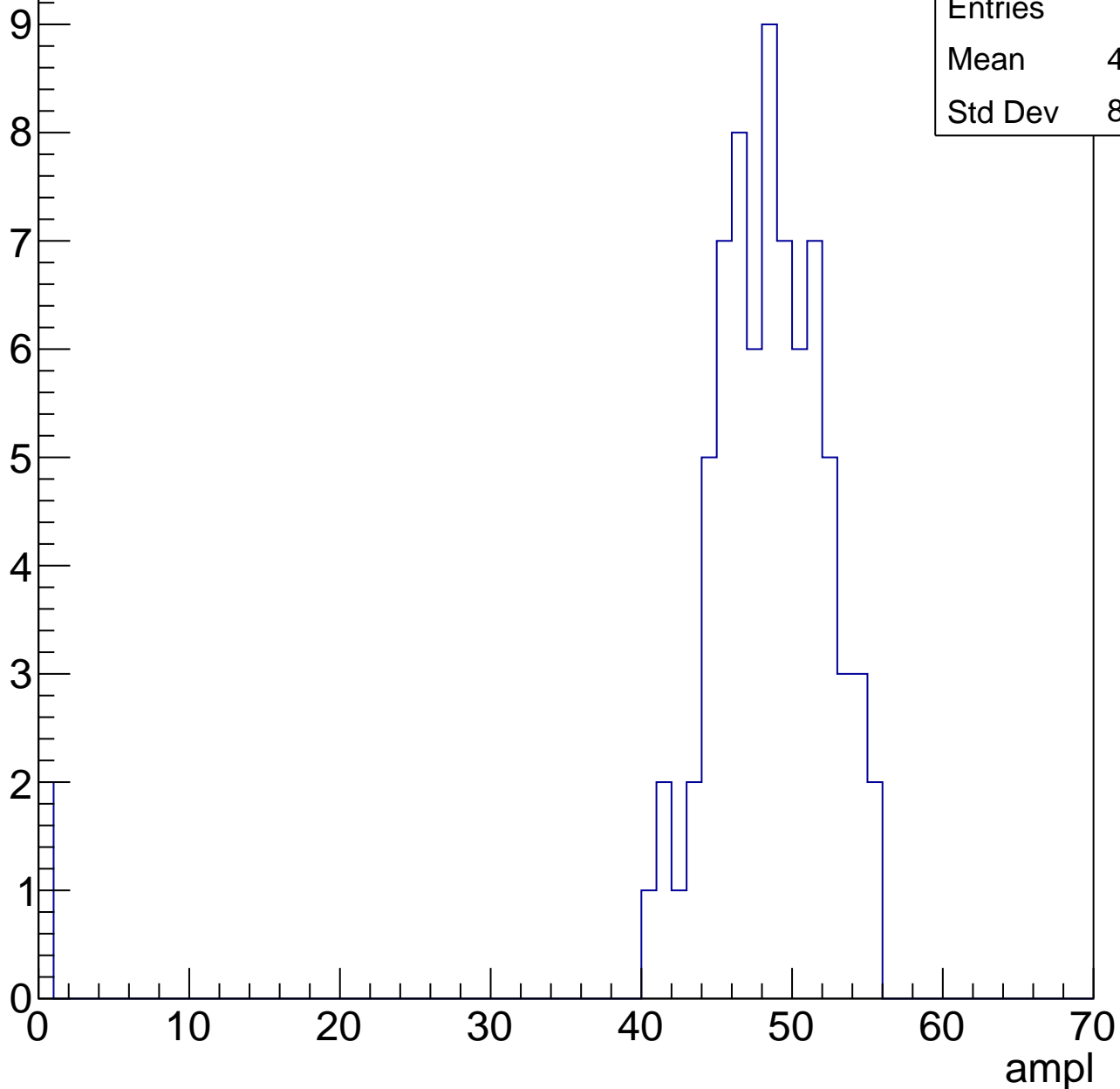
Entries	52
Mean	38.65
Std Dev	11.51



B1L103S, U23-ch119, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

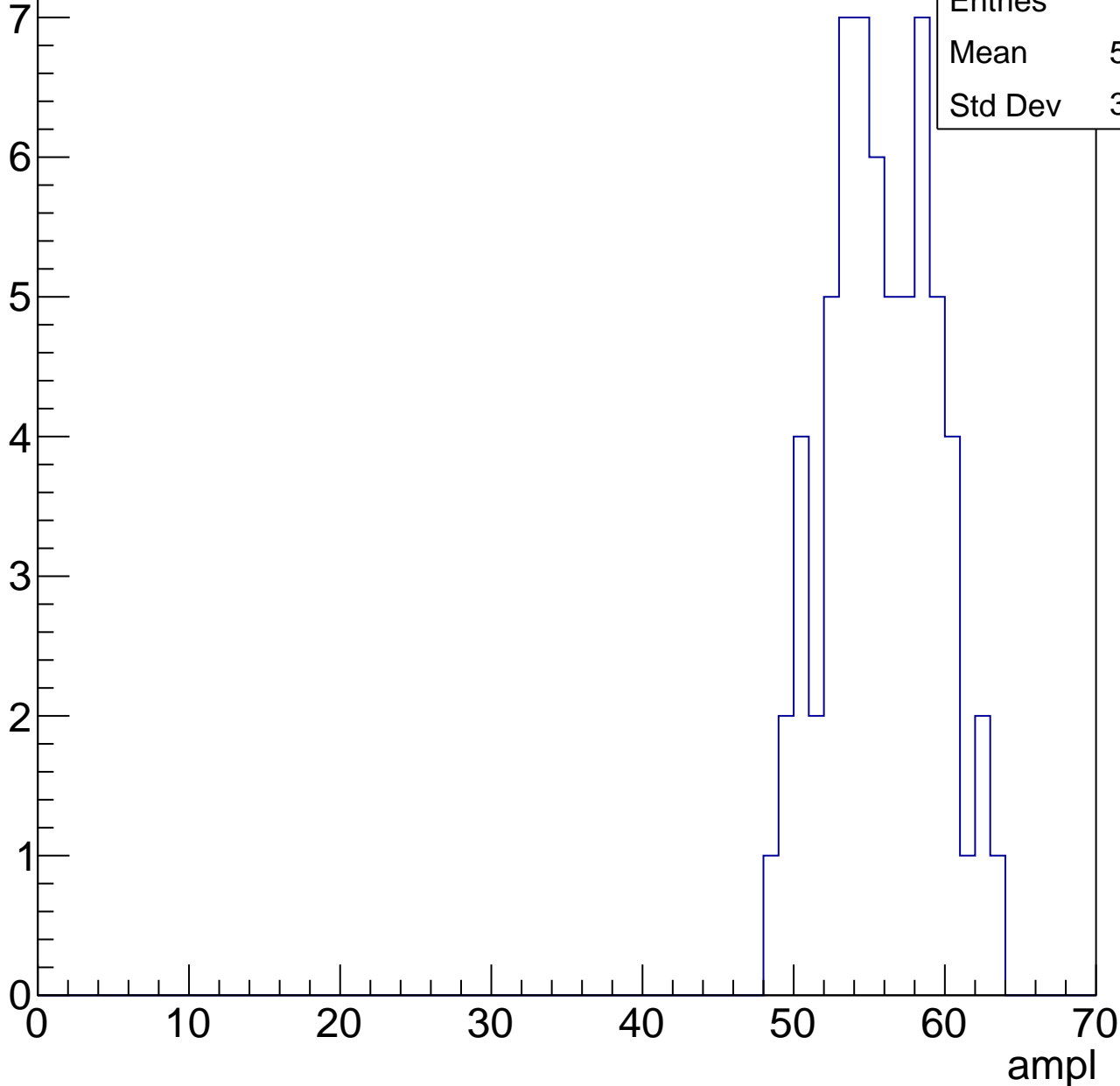


B1L103S, U23-ch119, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	55.33
Std Dev	3.518

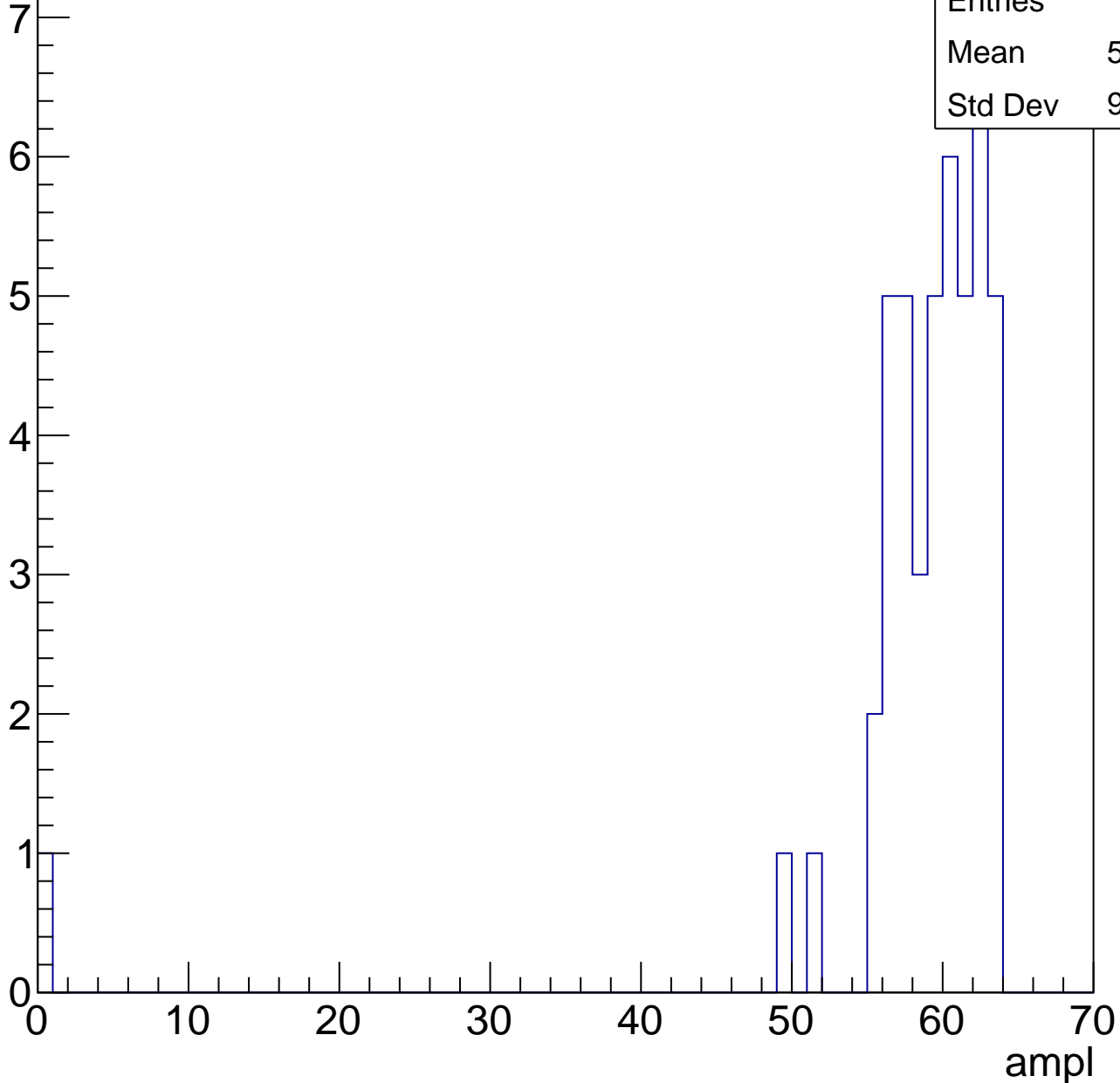


B1L103S, U23-ch119, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

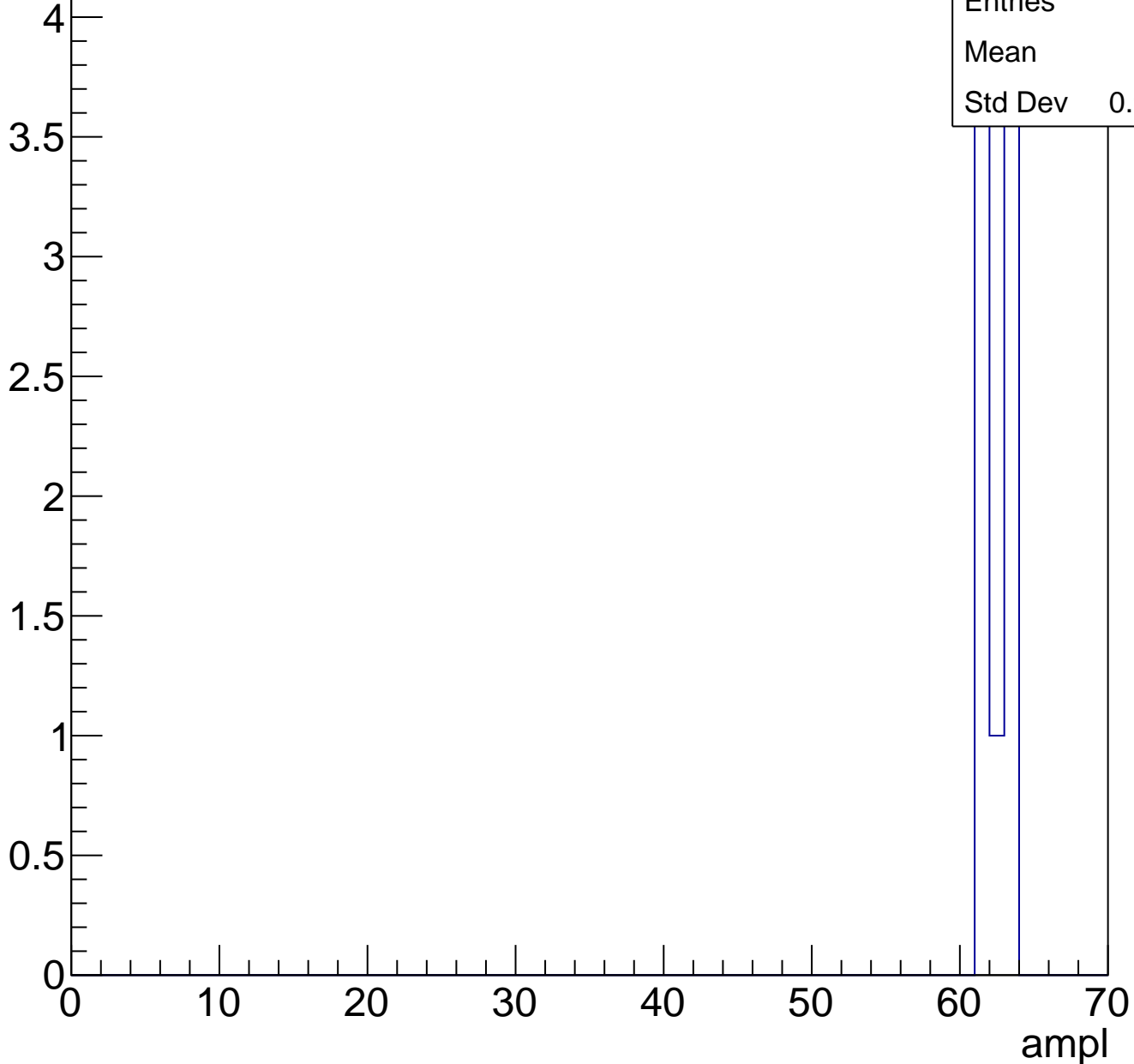
Entries	46
Mean	57.78
Std Dev	9.144



B1L103S, U23-ch119, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch119, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

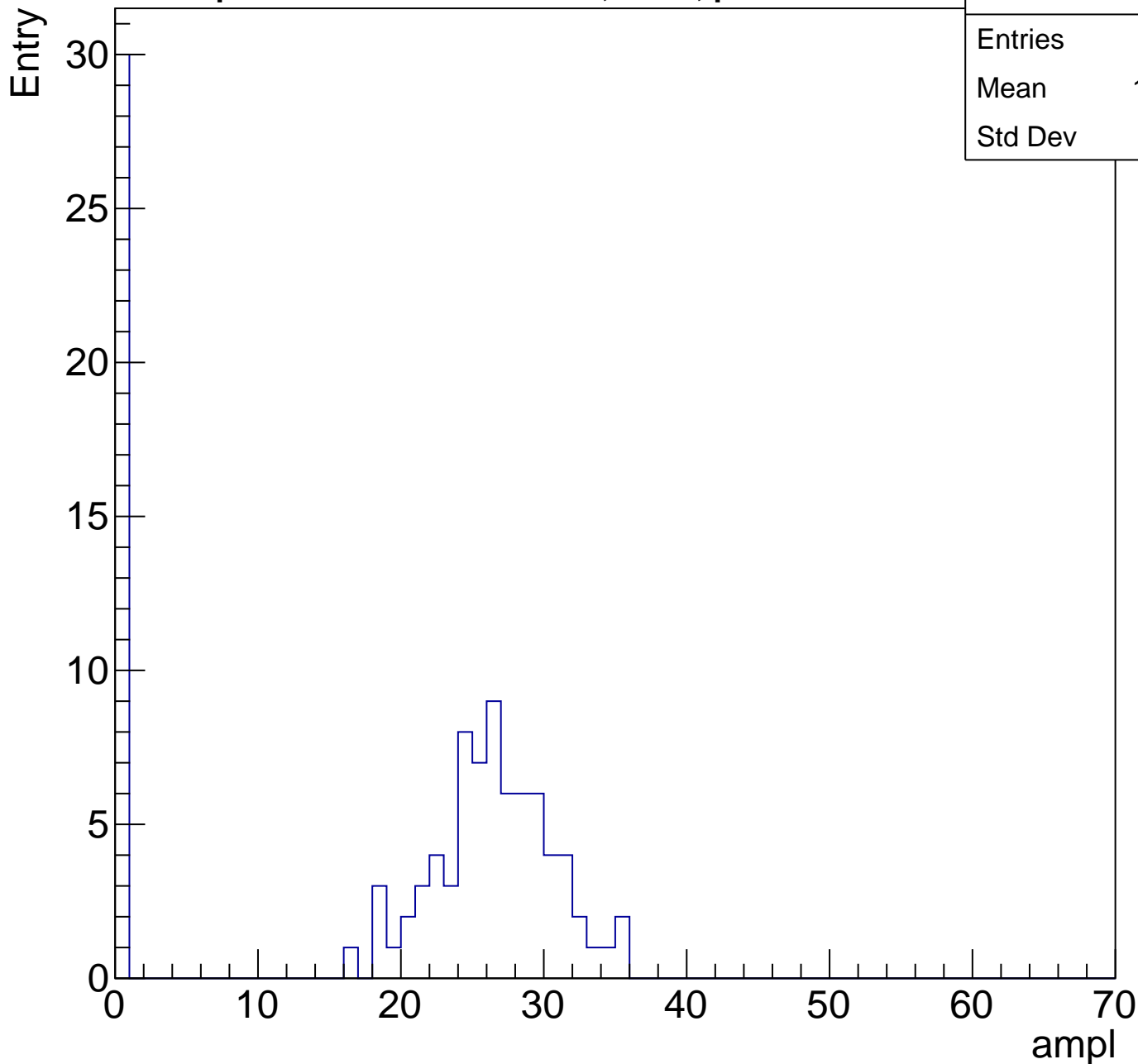
ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U23-ch120, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	103
Mean	18.44
Std Dev	12.31



B1L103S, U23-ch120, adc1

calib_packv5_041523_1651.root, FC#0, port C2

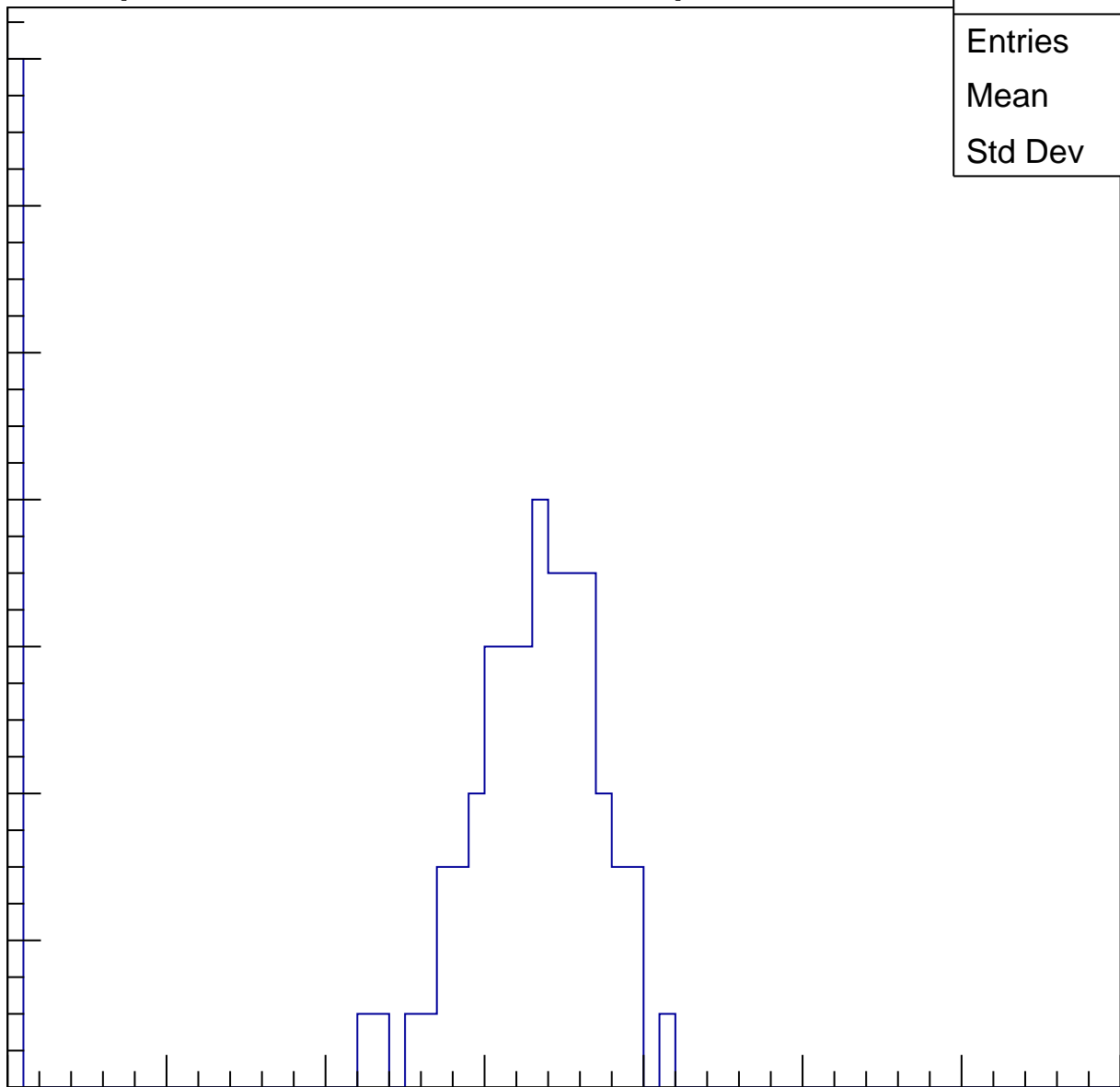
Entries	86
Mean	27.37
Std Dev	12.57

Entry

14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

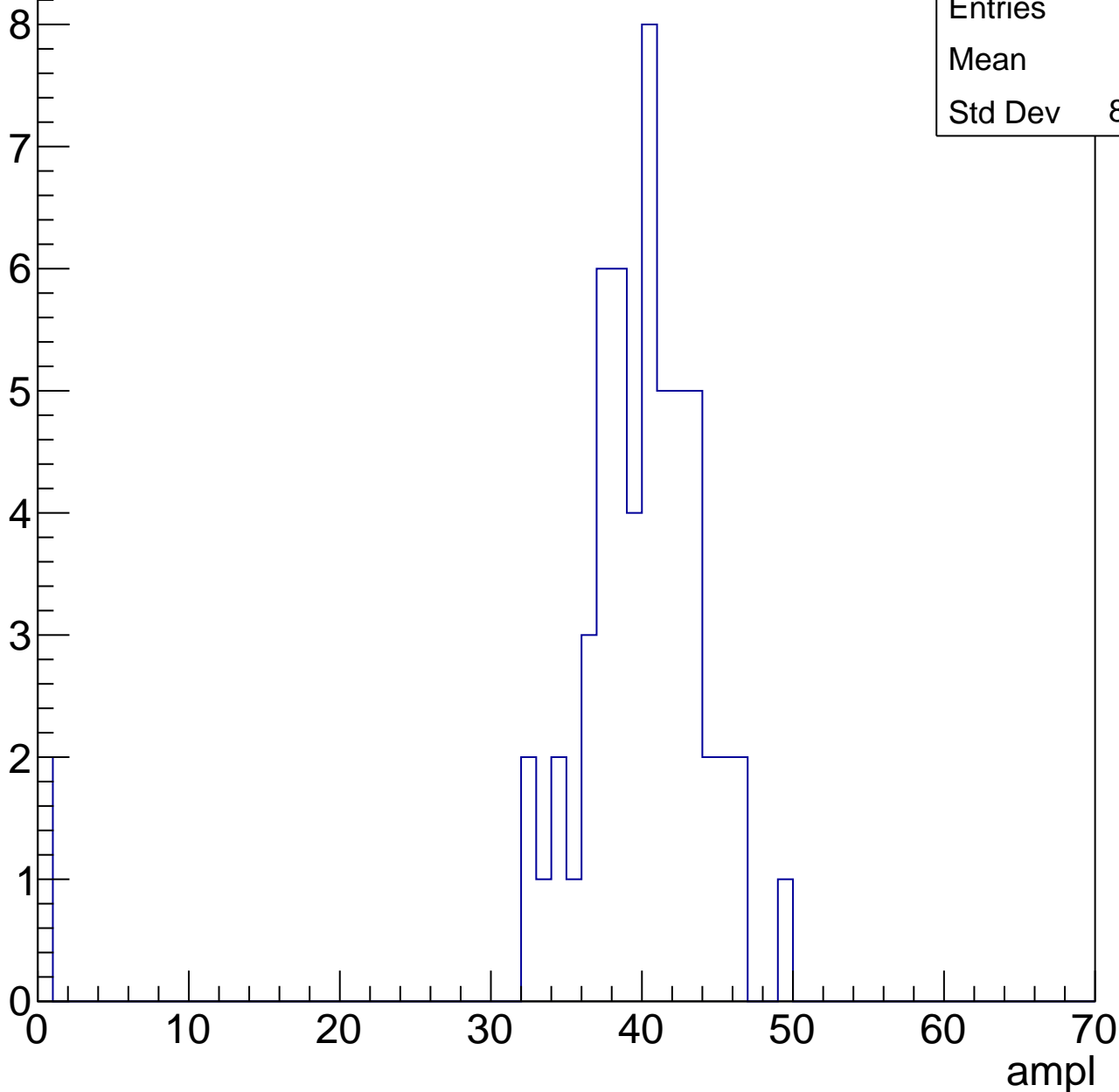


B1L103S, U23-ch120, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	57
Mean	38.3
Std Dev	8.105

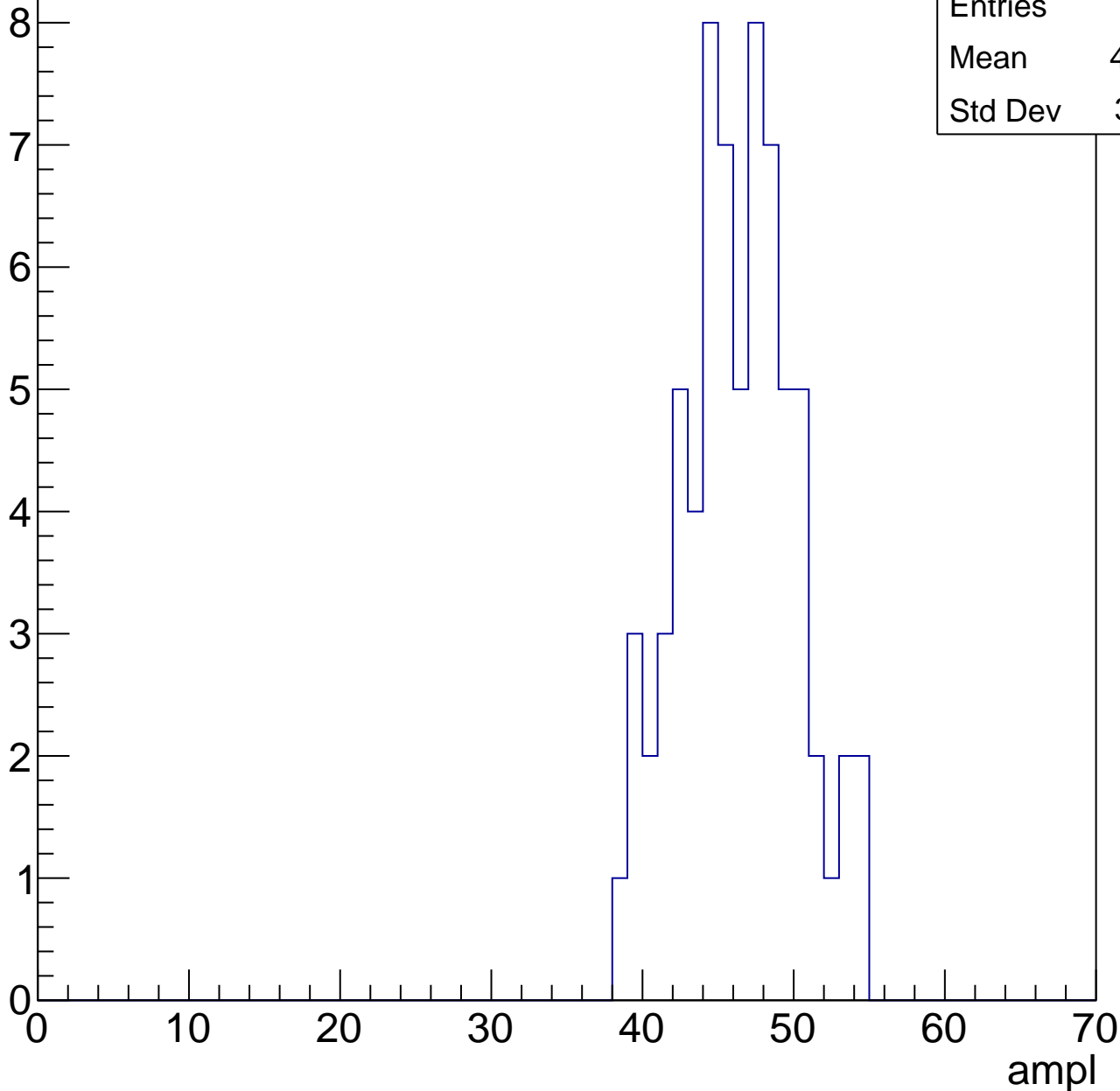


B1L103S, U23-ch120, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	45.89
Std Dev	3.751

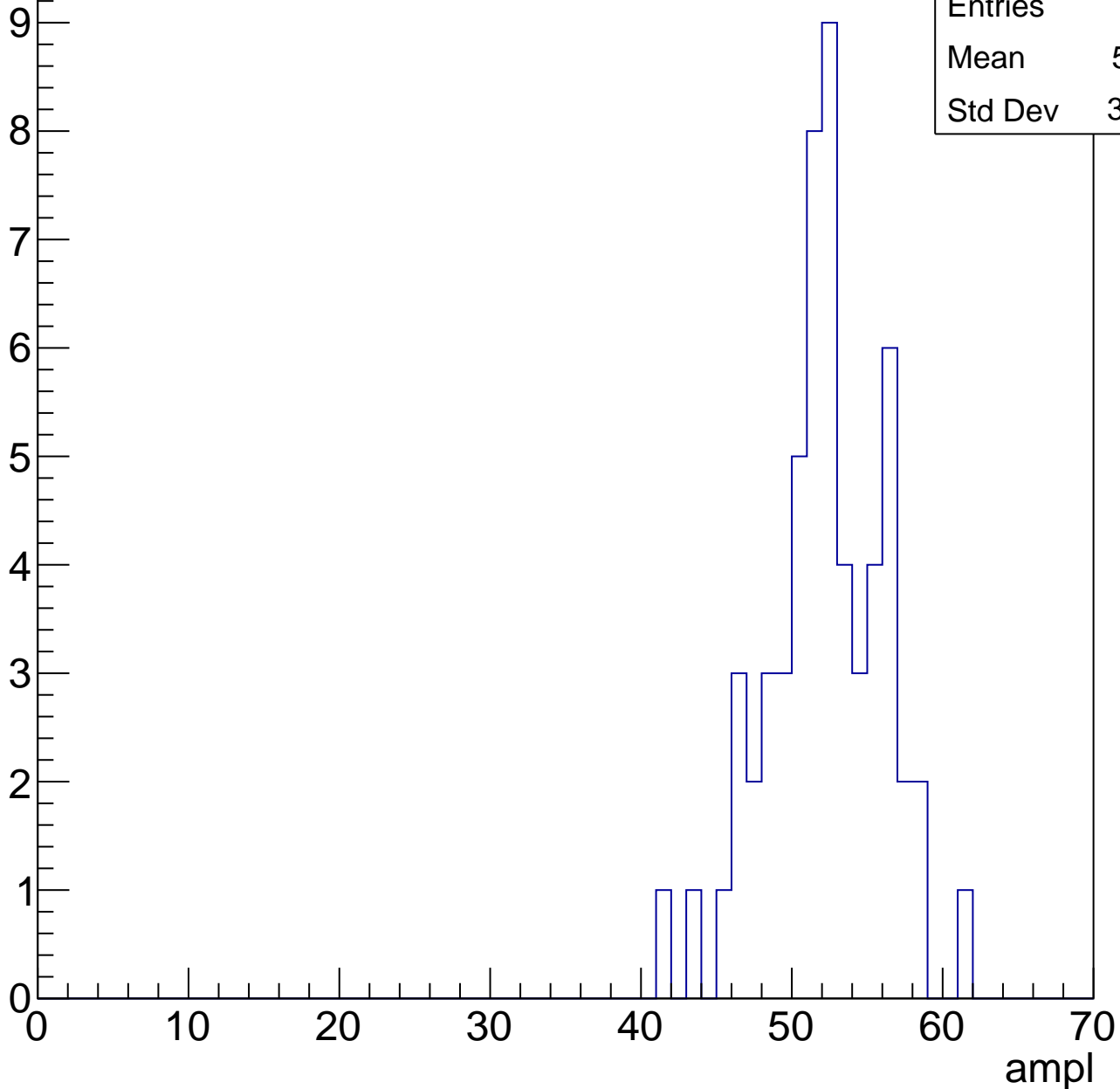


B1L103S, U23-ch120, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	51.71
Std Dev	3.846



B1L103S, U23-ch120, adc5

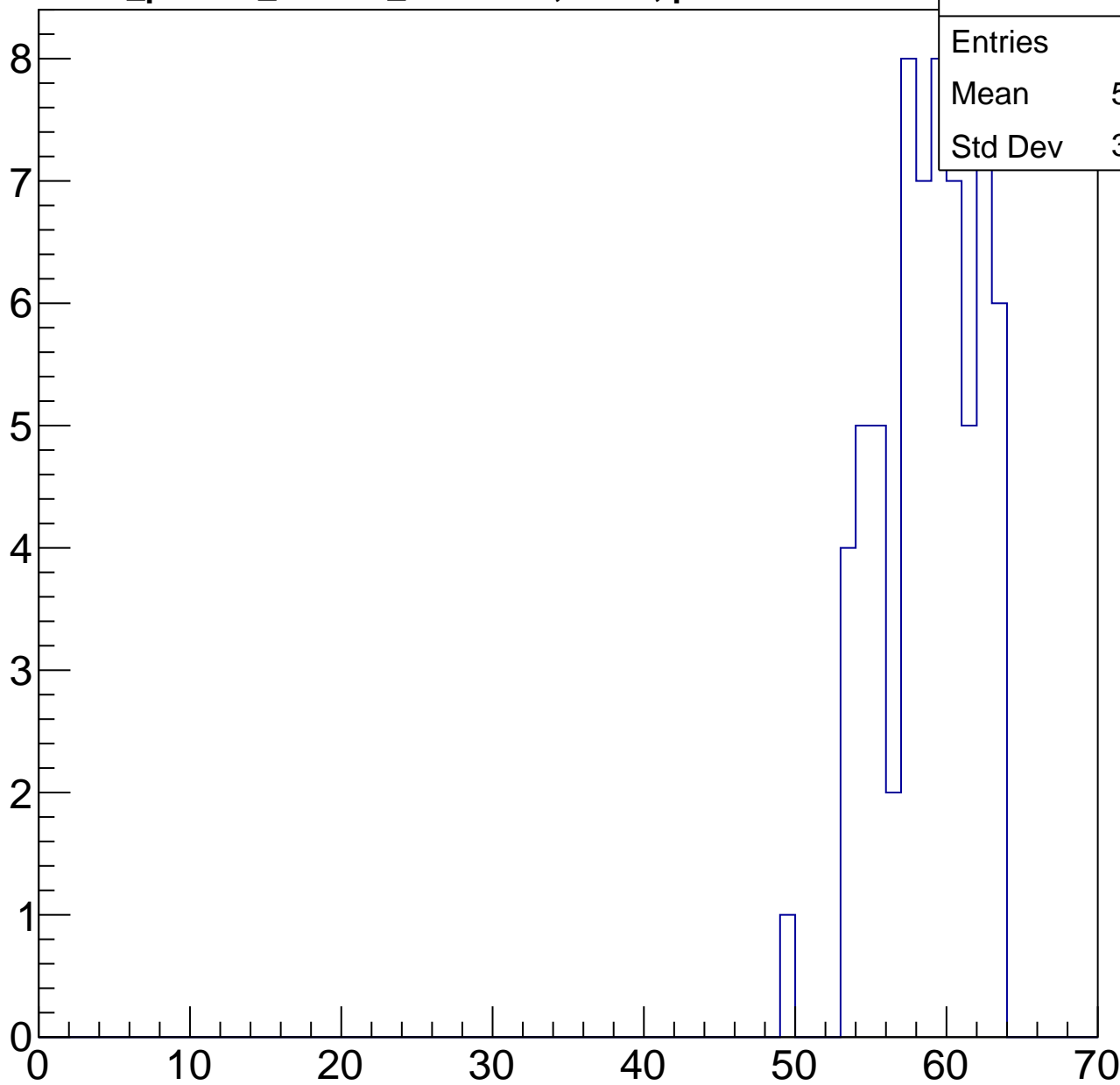
calib_packv5_041523_1651.root, FC#0, port C2

Entry

8
7
6
5
4
3
2
1
0

Entries	66
Mean	58.35
Std Dev	3.193

ampl



B1L103S, U23-ch120, adc6

calib_packv5_041523_1651.root, FC#0, port C2

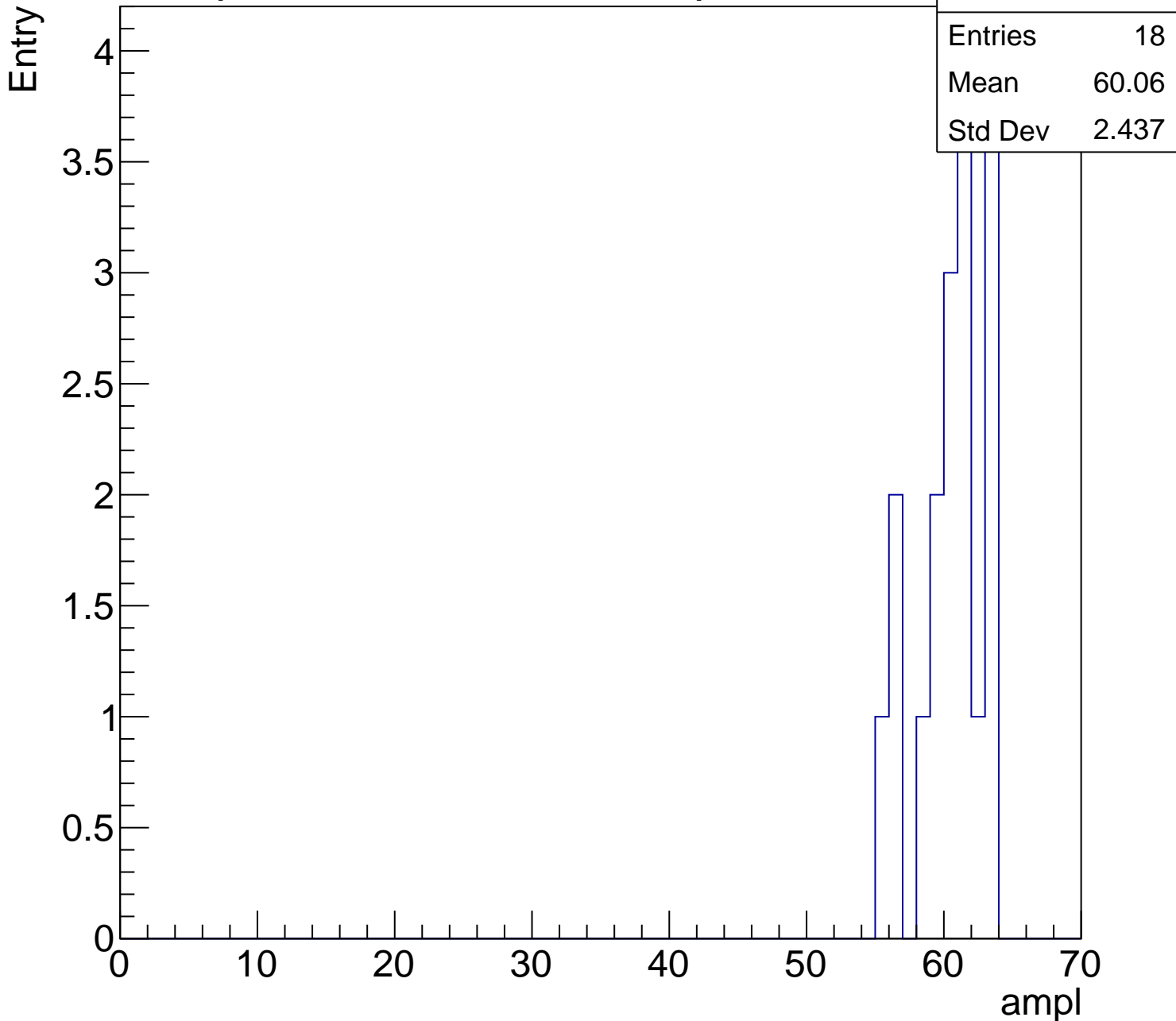
Entry

4
3.5
3
2.5
2
1.5
1
0.5
0

Entries	18
Mean	60.06
Std Dev	2.437

ampl

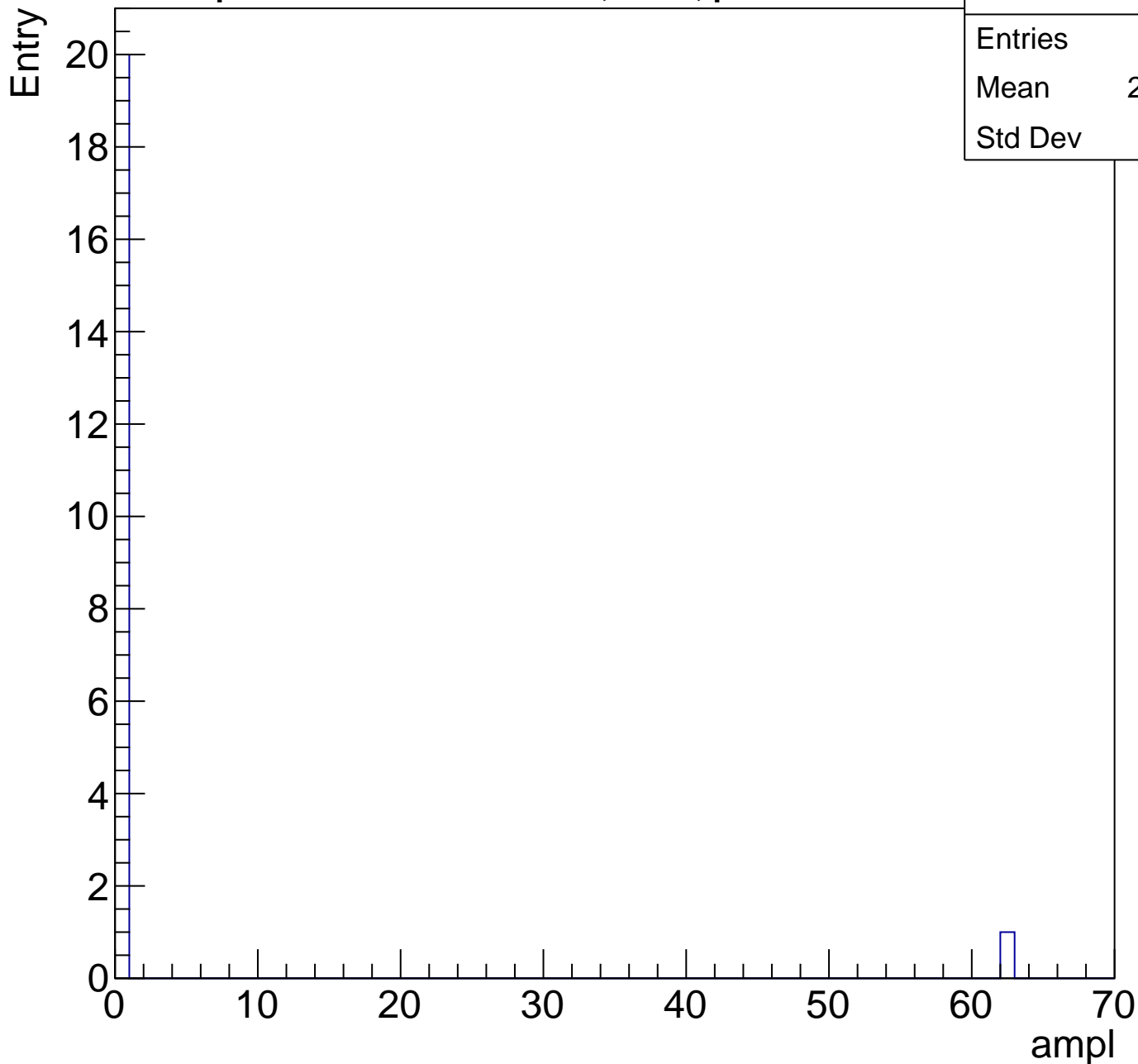
0 10 20 30 40 50 60 70



B1L103S, U23-ch120, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	21
Mean	2.952
Std Dev	13.2

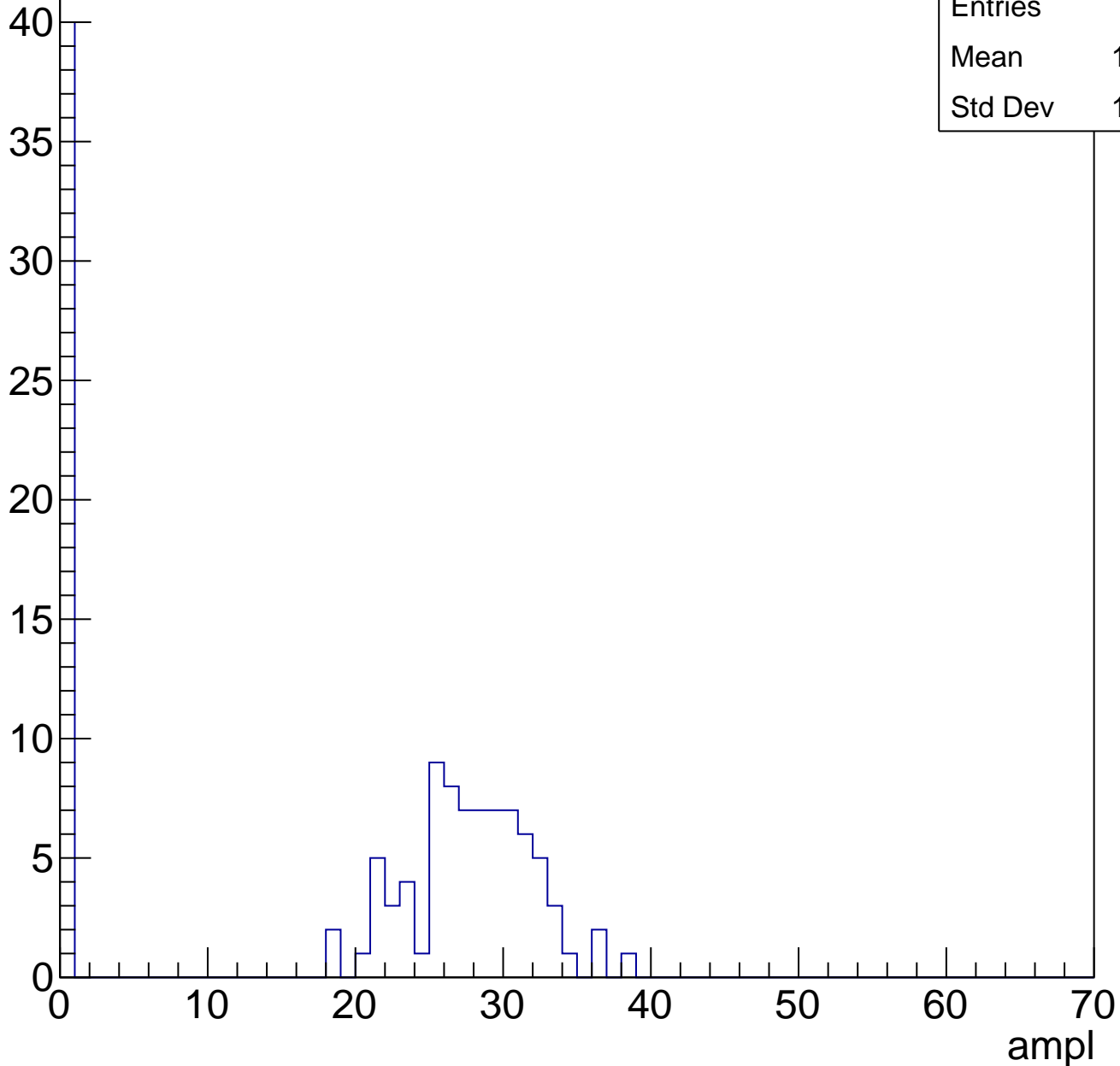


B1L103S, U23-ch121, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	119
Mean	18.18
Std Dev	13.36

Entry

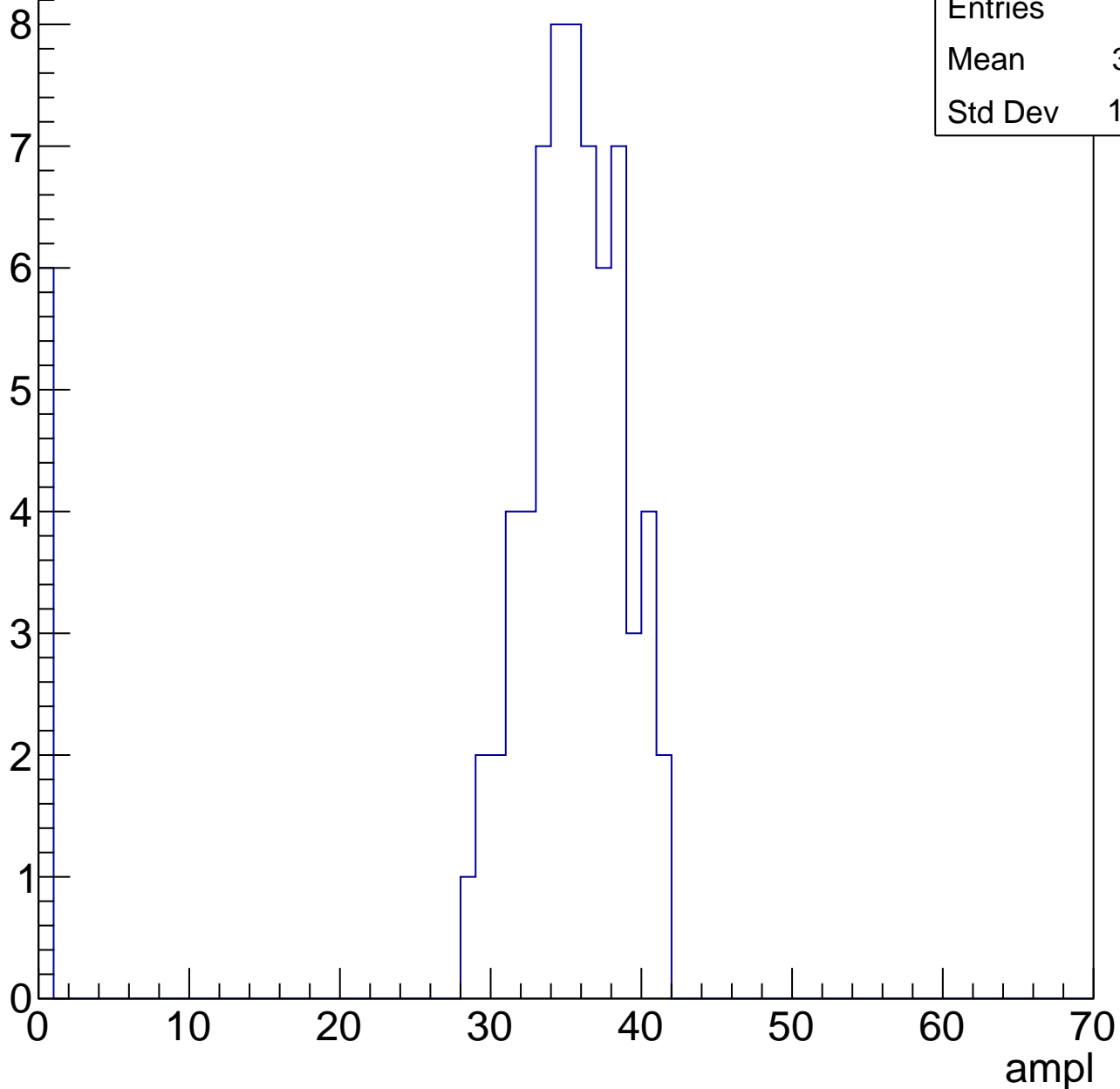


B1L103S, U23-ch121, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	32.11
Std Dev	10.19

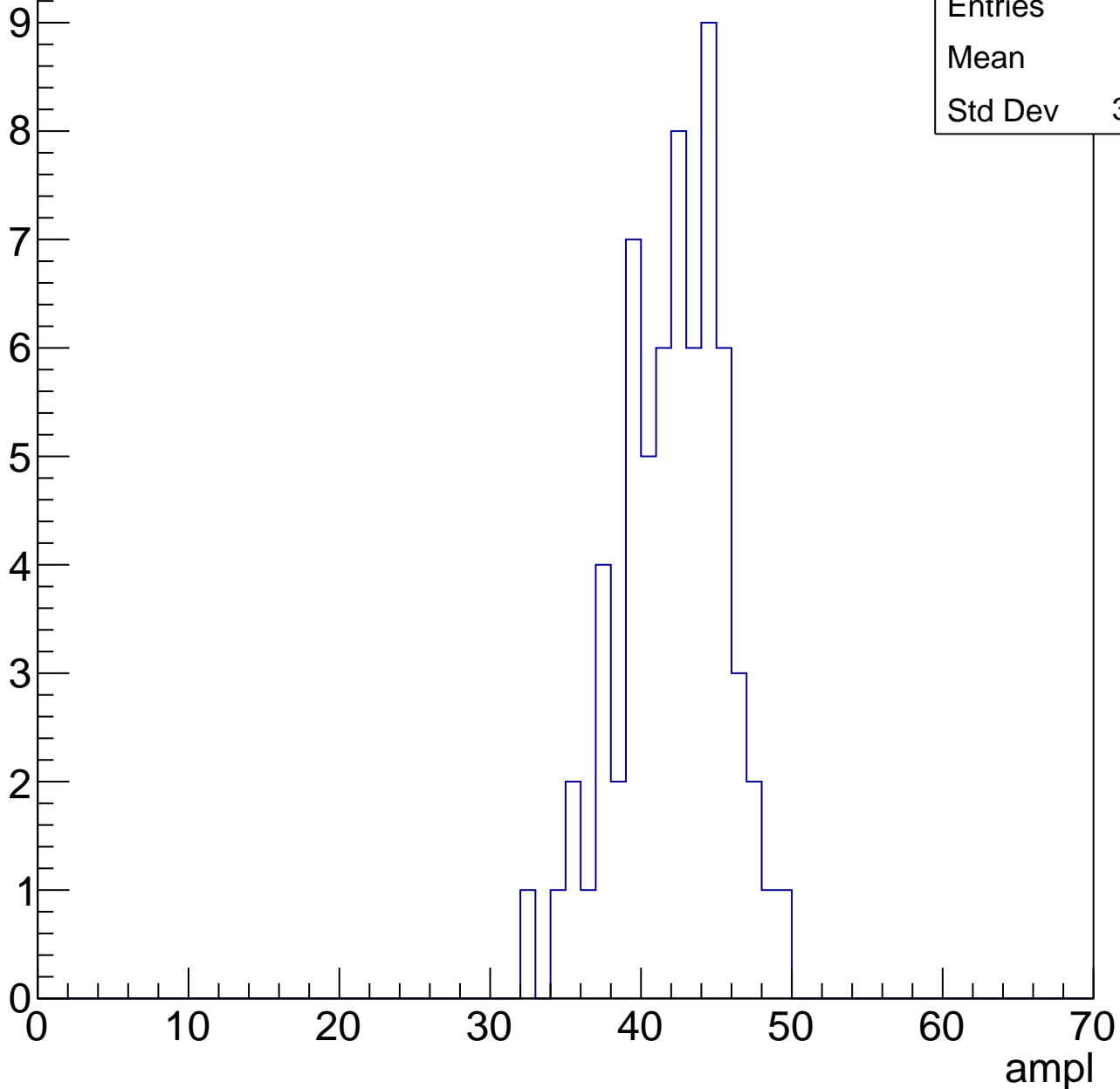


B1L103S, U23-ch121, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	41.6
Std Dev	3.481

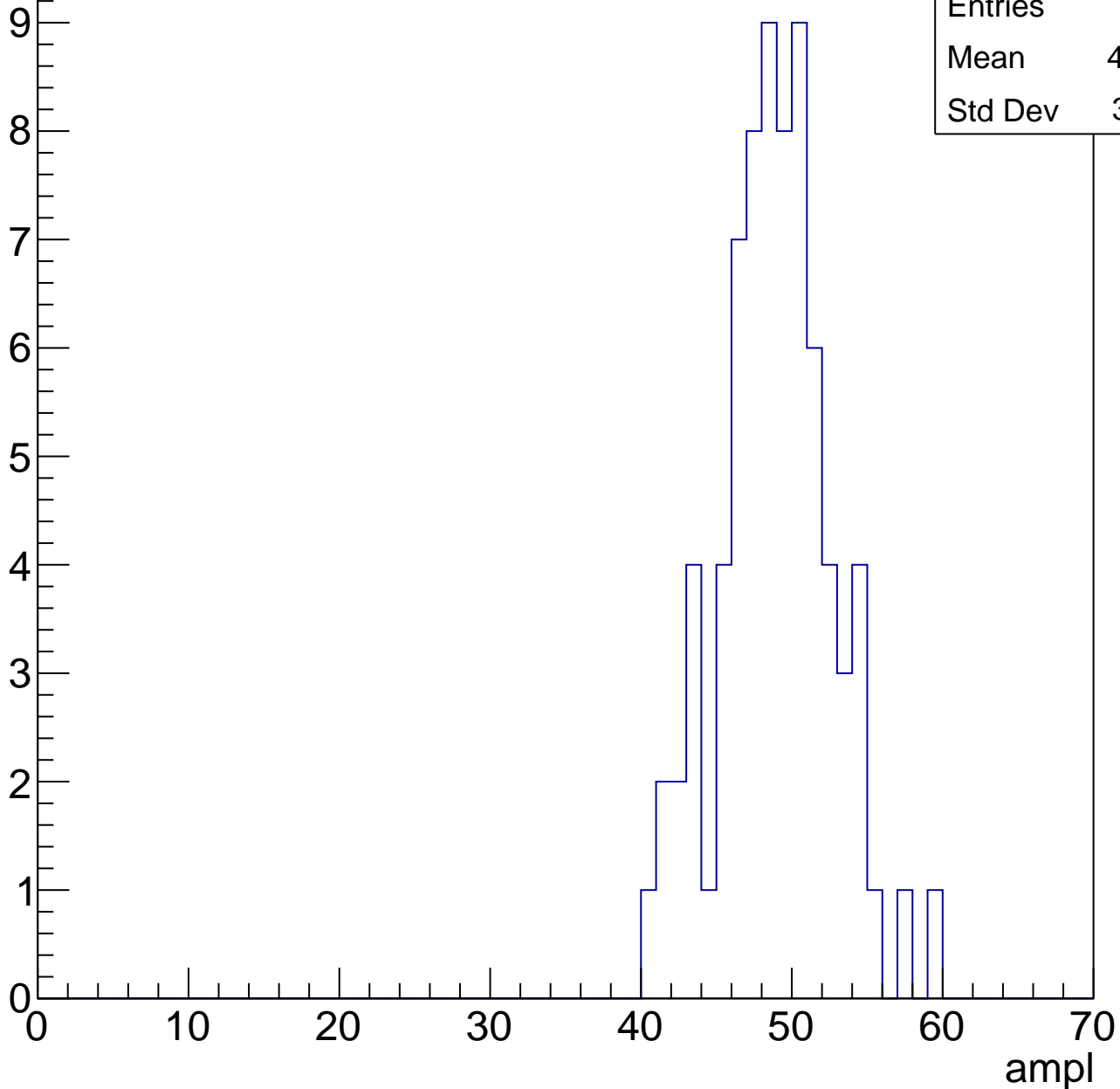


B1L103S, U23-ch121, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	75
Mean	48.45
Std Dev	3.721

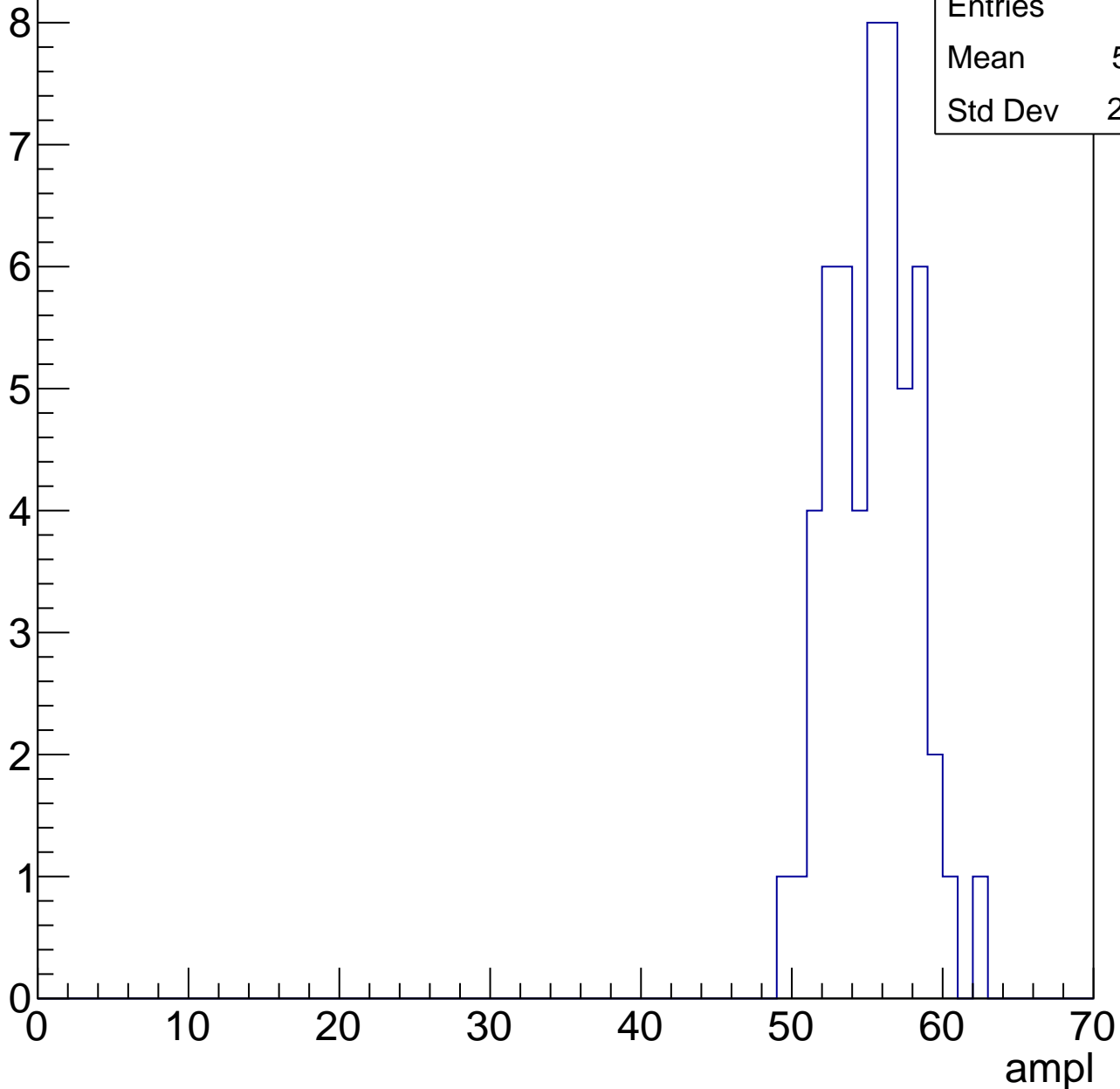


B1L103S, U23-ch121, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	53
Mean	54.91
Std Dev	2.728

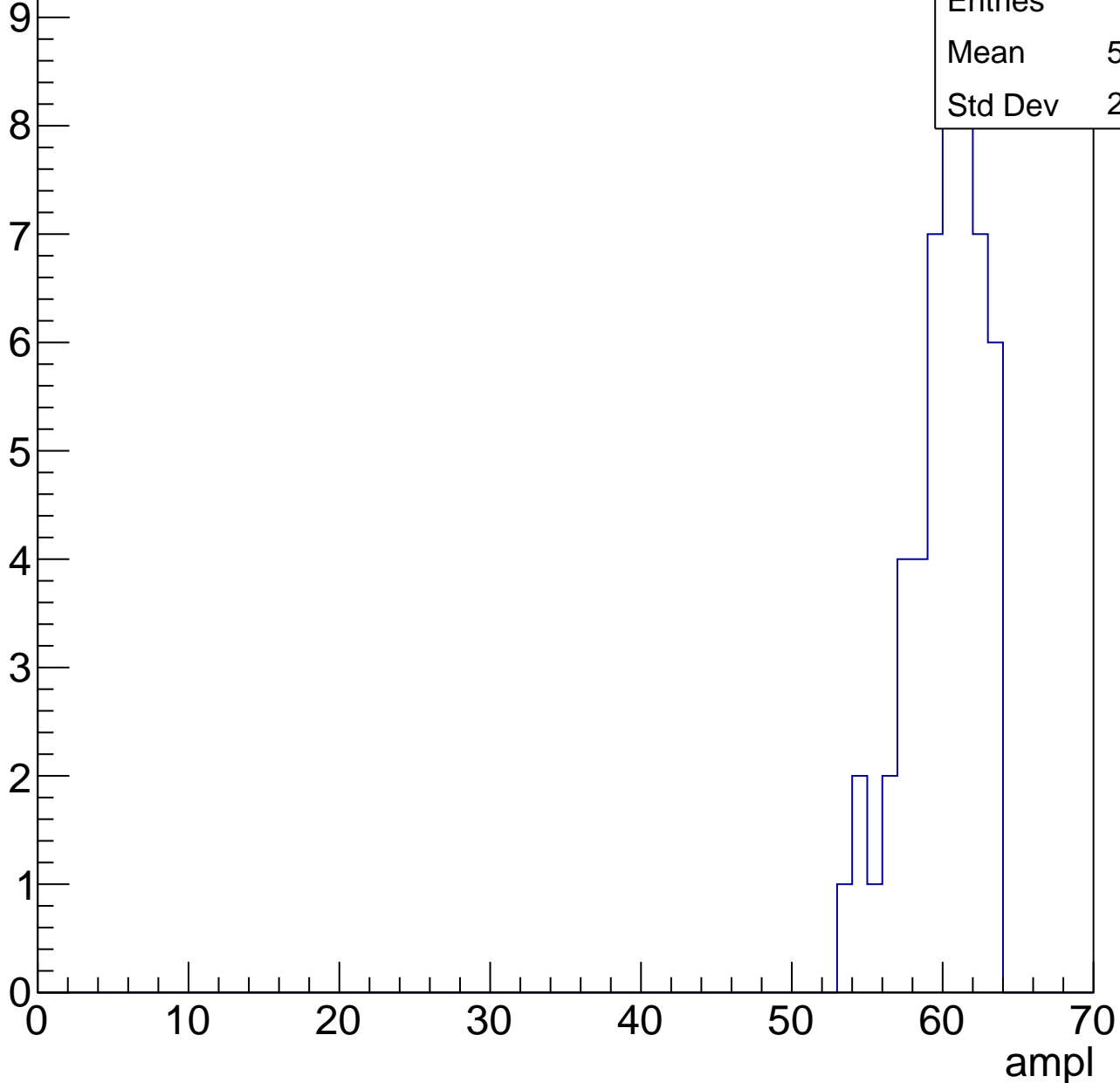


B1L103S, U23-ch121, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

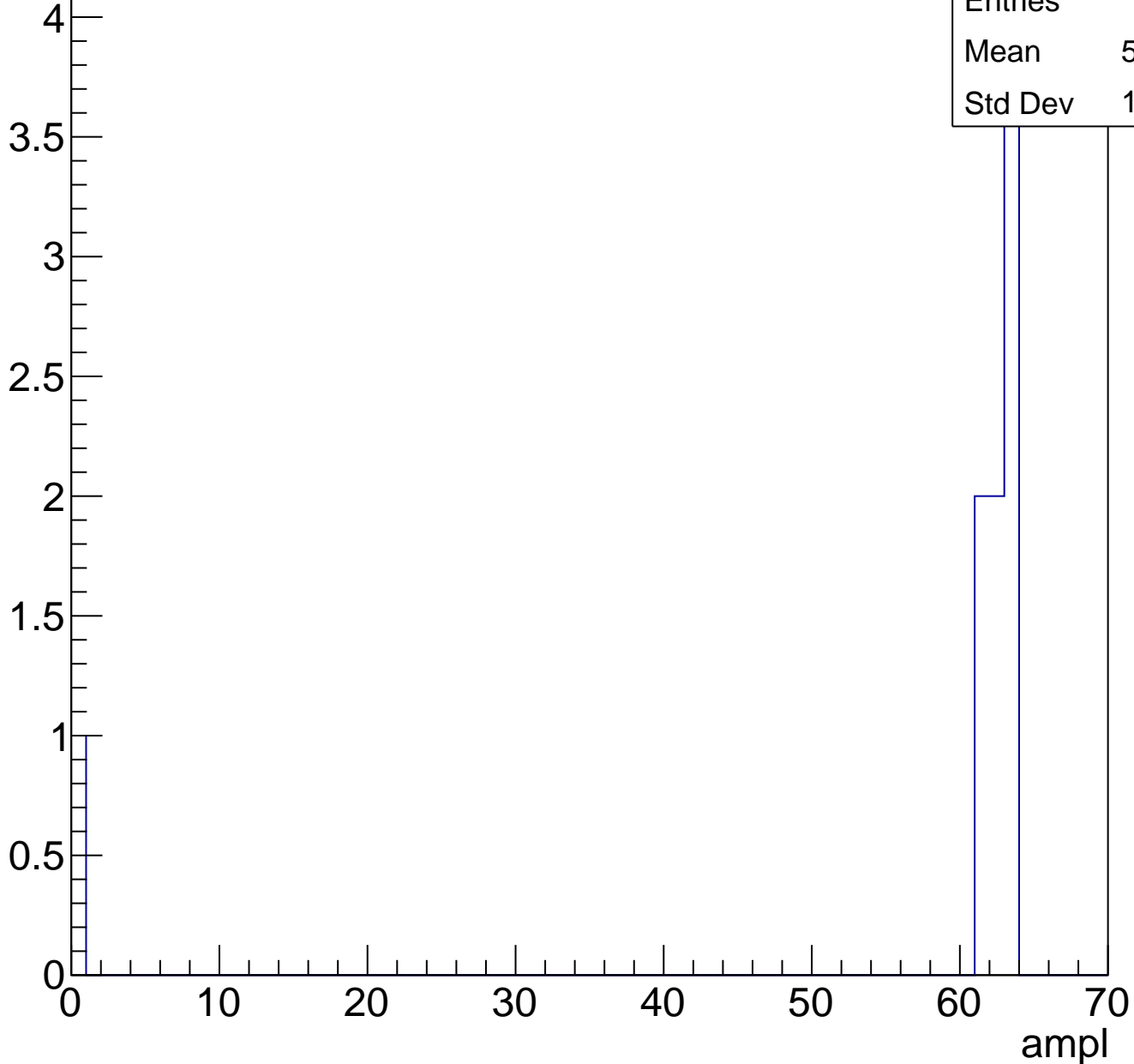
Entries	51
Mean	59.63
Std Dev	2.505



B1L103S, U23-ch121, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch121, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U23-ch122, adc0

calib_packv5_041523_1651.root, FC#0, port C2

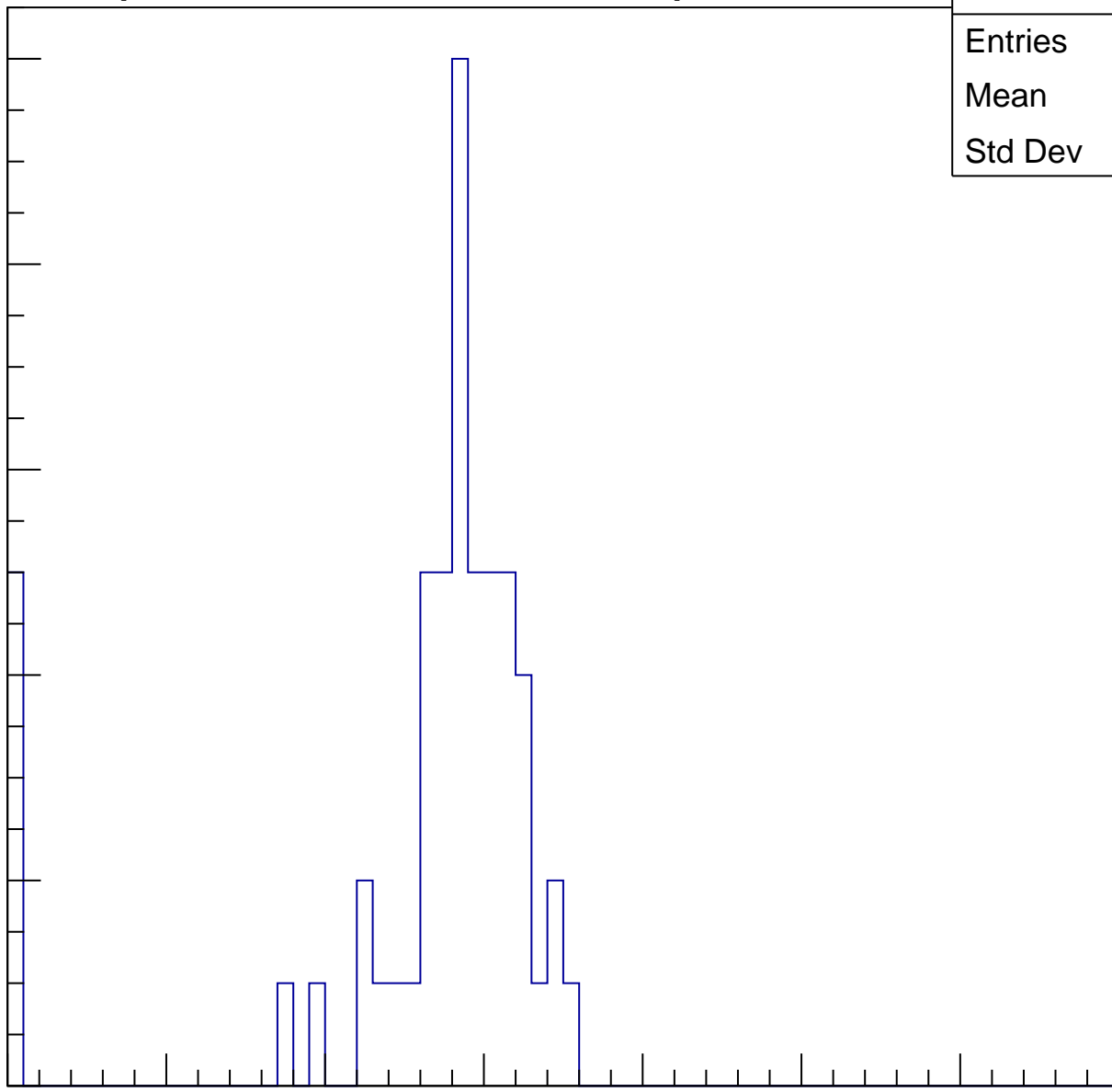
Entries	55
Mean	25.65
Std Dev	8.787

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

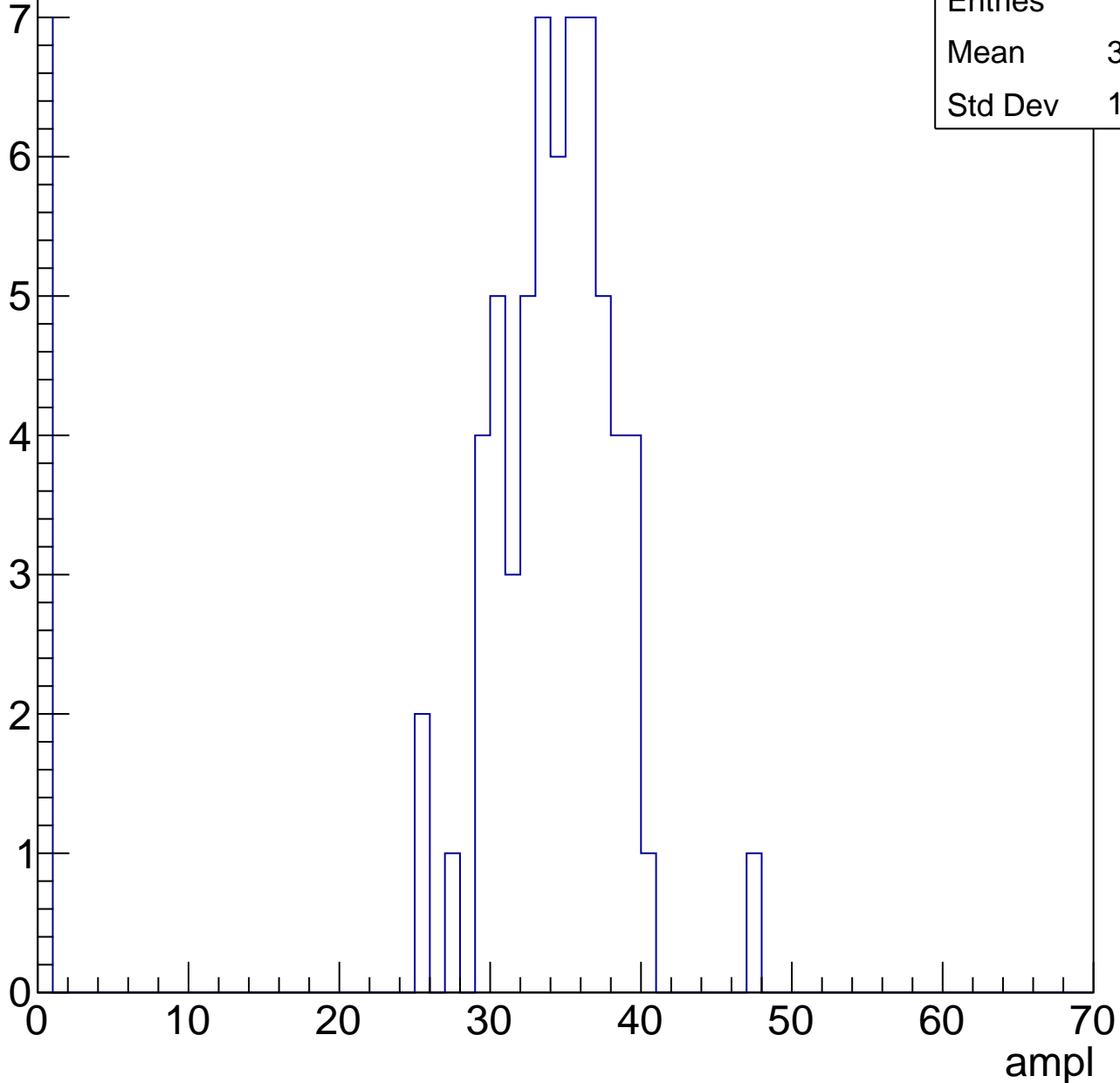


B1L103S, U23-ch122, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	30.55
Std Dev	10.88

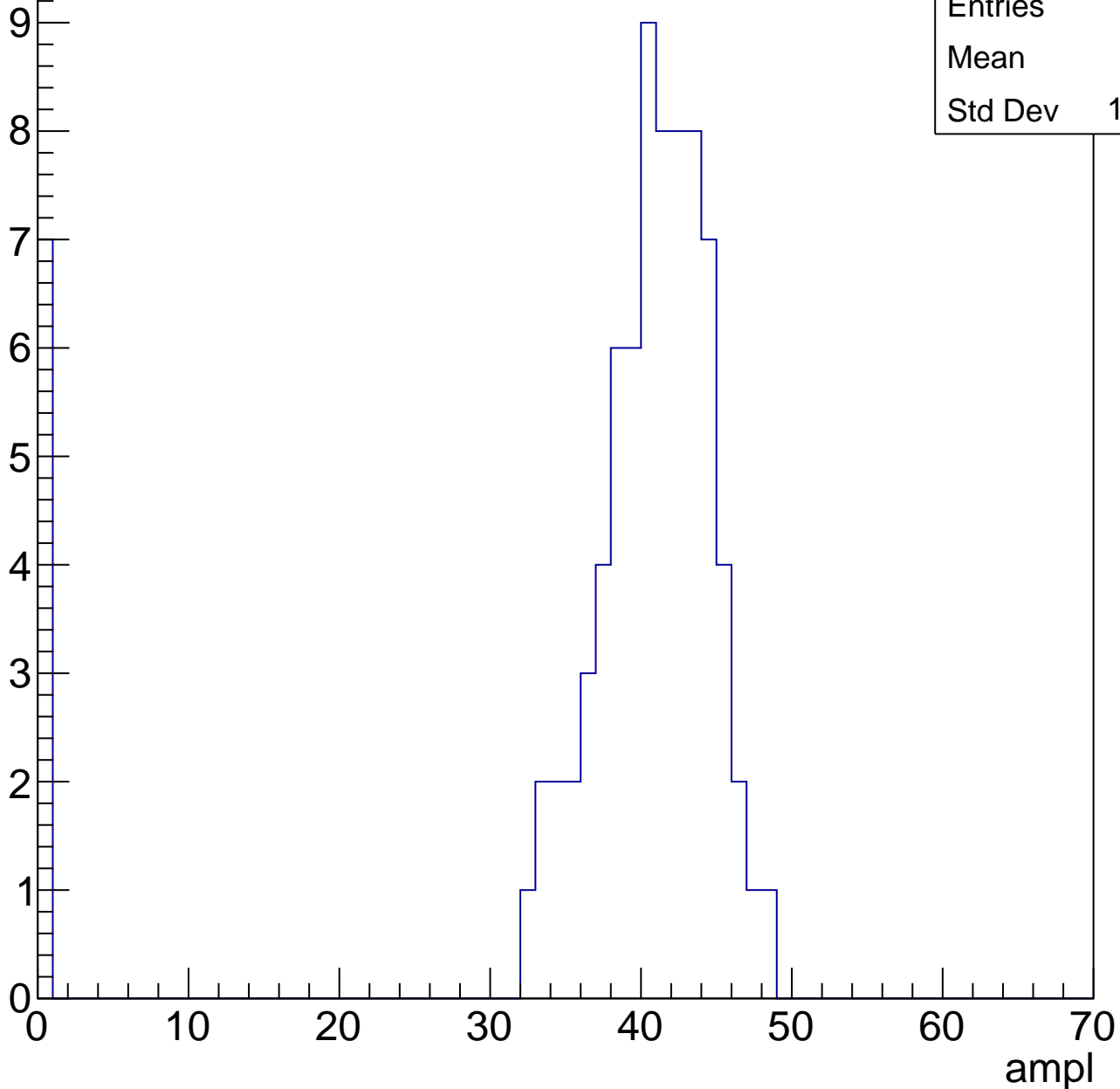


B1L103S, U23-ch122, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	81
Mean	37
Std Dev	11.85

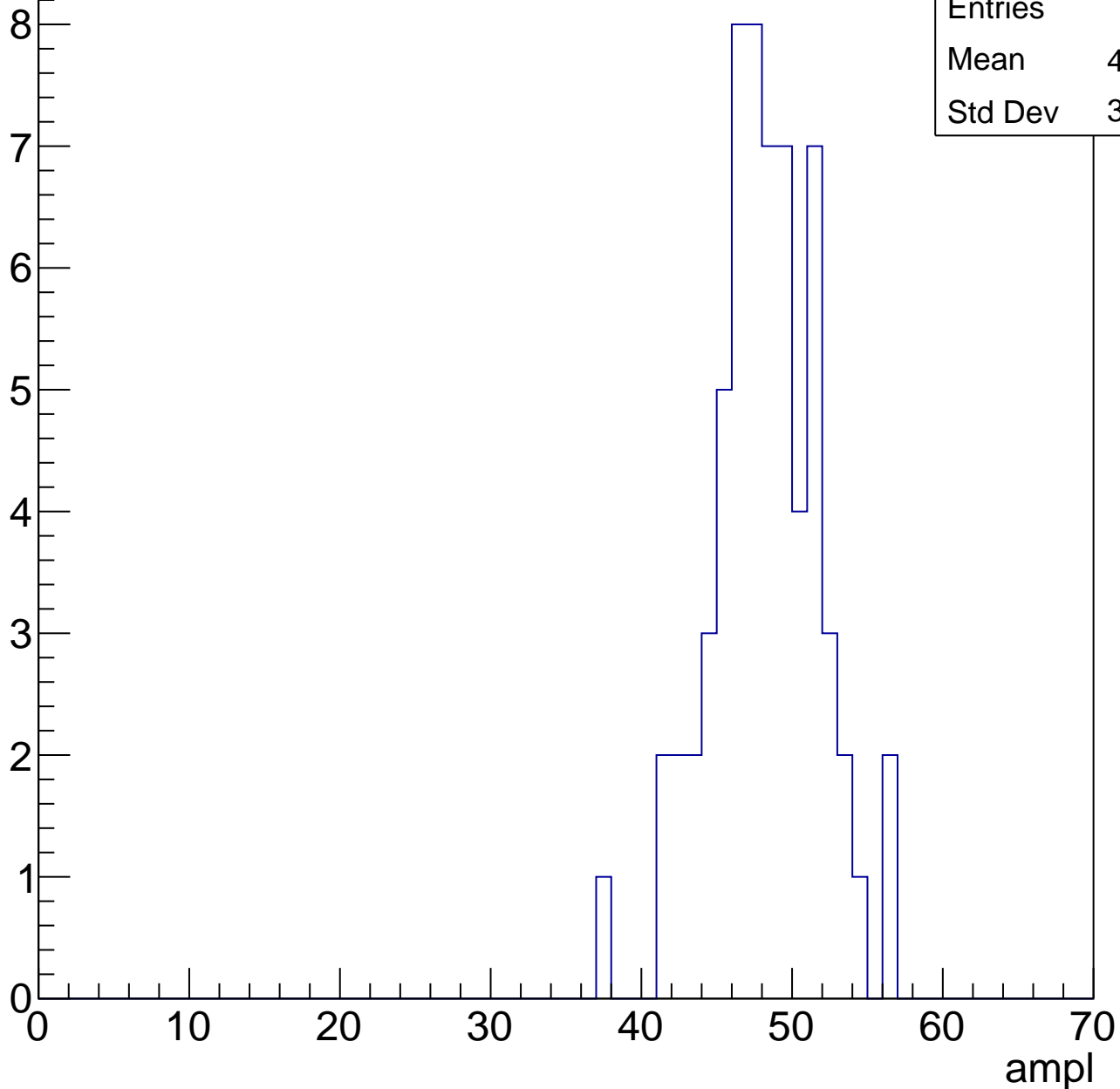


B1L103S, U23-ch122, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	47.72
Std Dev	3.573

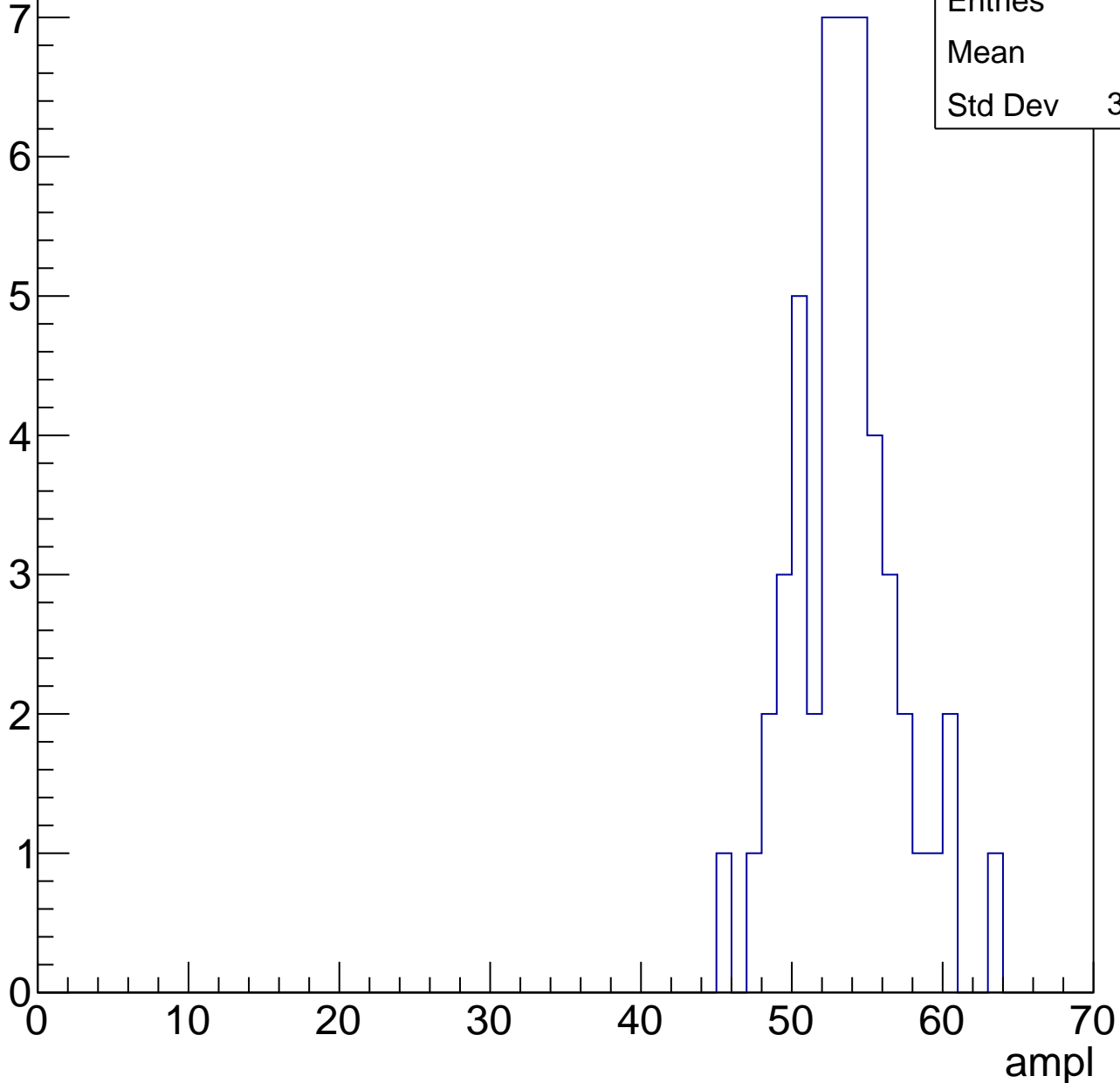


B1L103S, U23-ch122, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	49
Mean	53.1
Std Dev	3.495



B1L103S, U23-ch122, adc5

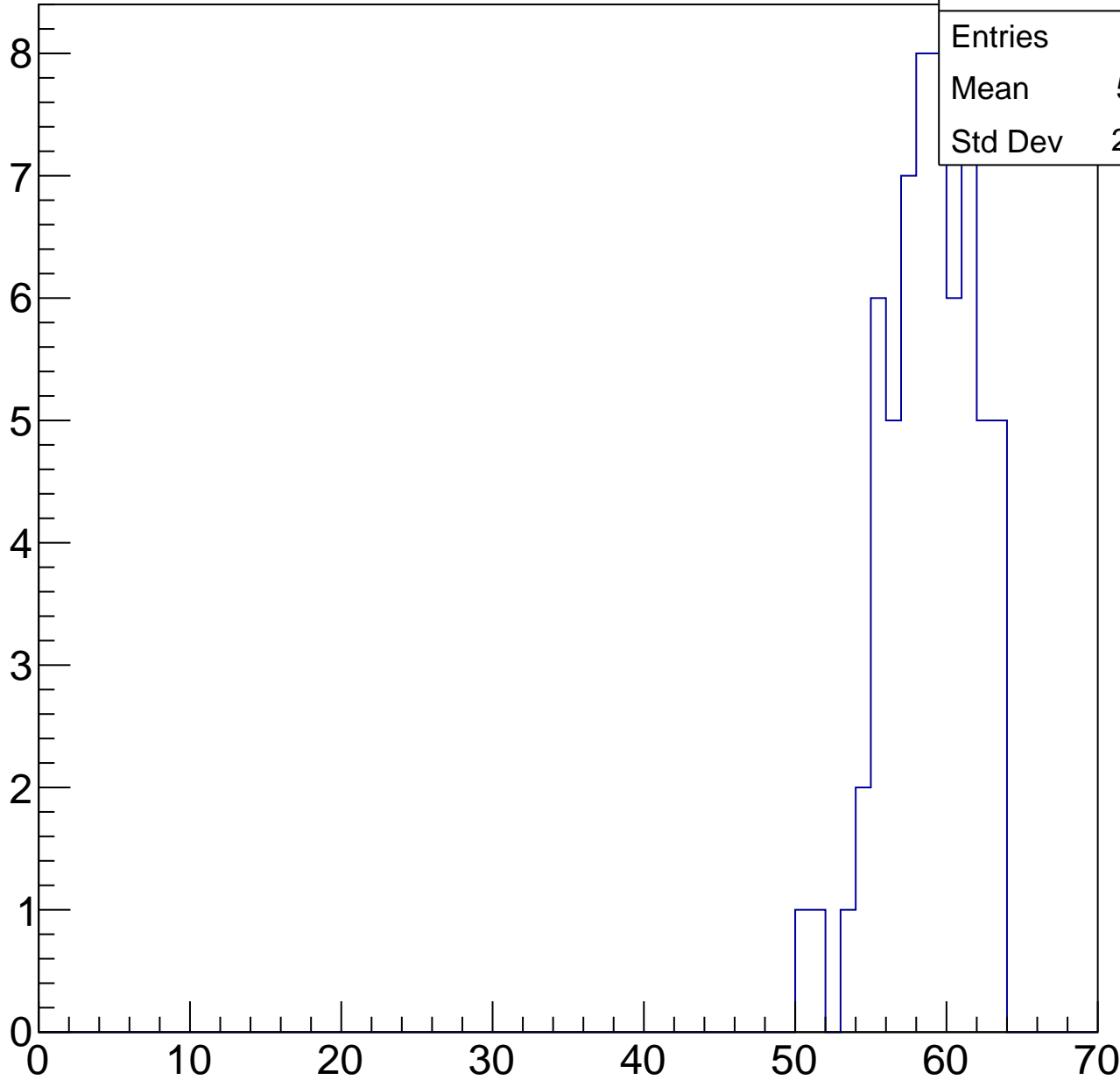
calib_packv5_041523_1651.root, FC#0, port C2

Entry

8
7
6
5
4
3
2
1
0

Entries	63
Mean	58.41
Std Dev	2.953

ampl

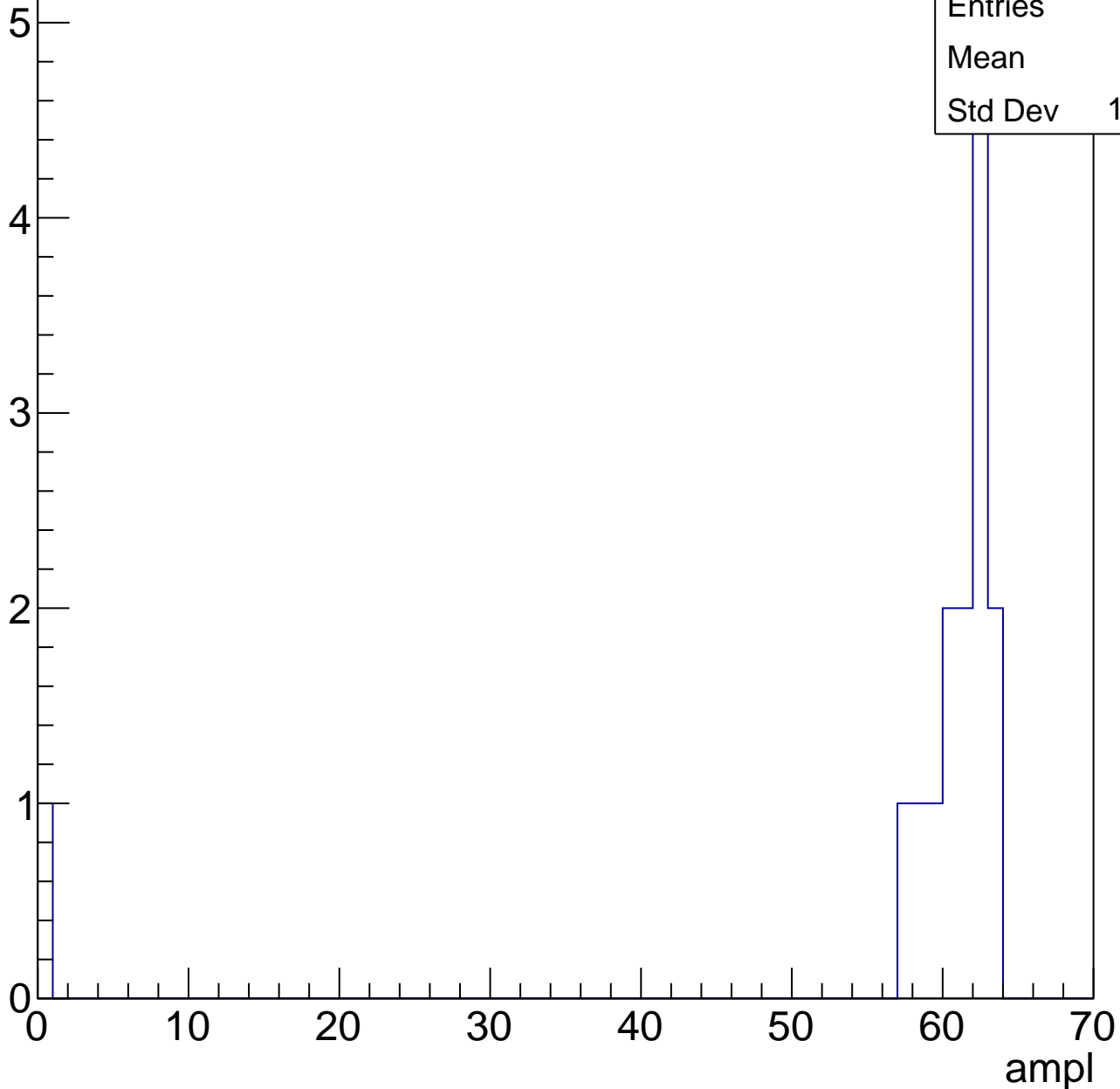


B1L103S, U23-ch122, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	15
Mean	56.8
Std Dev	15.28



B1L103S, U23-ch122, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	21
Mean	6
Std Dev	18.49

Entry

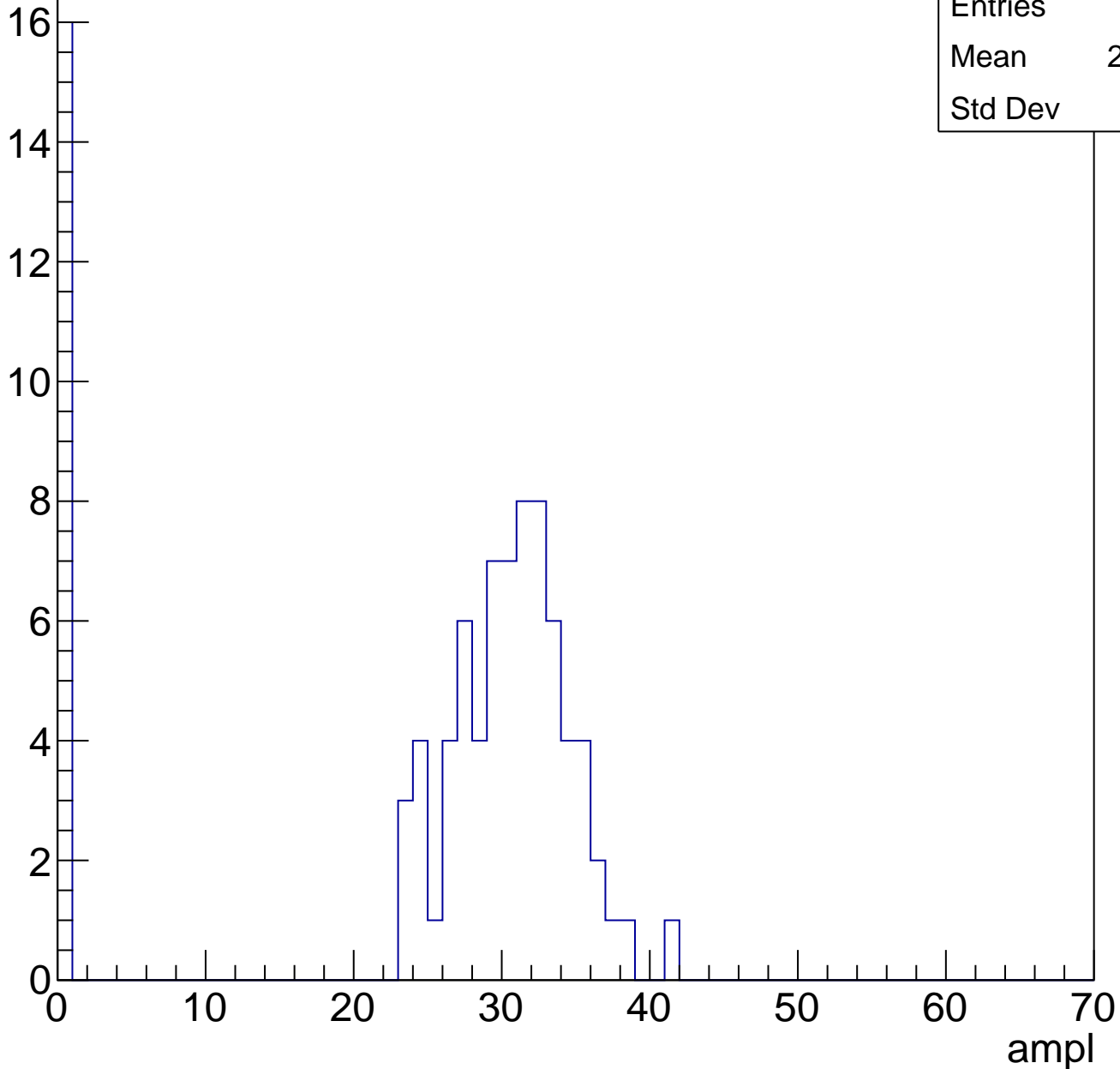


B1L103S, U23-ch123, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	87
Mean	24.68
Std Dev	12.2

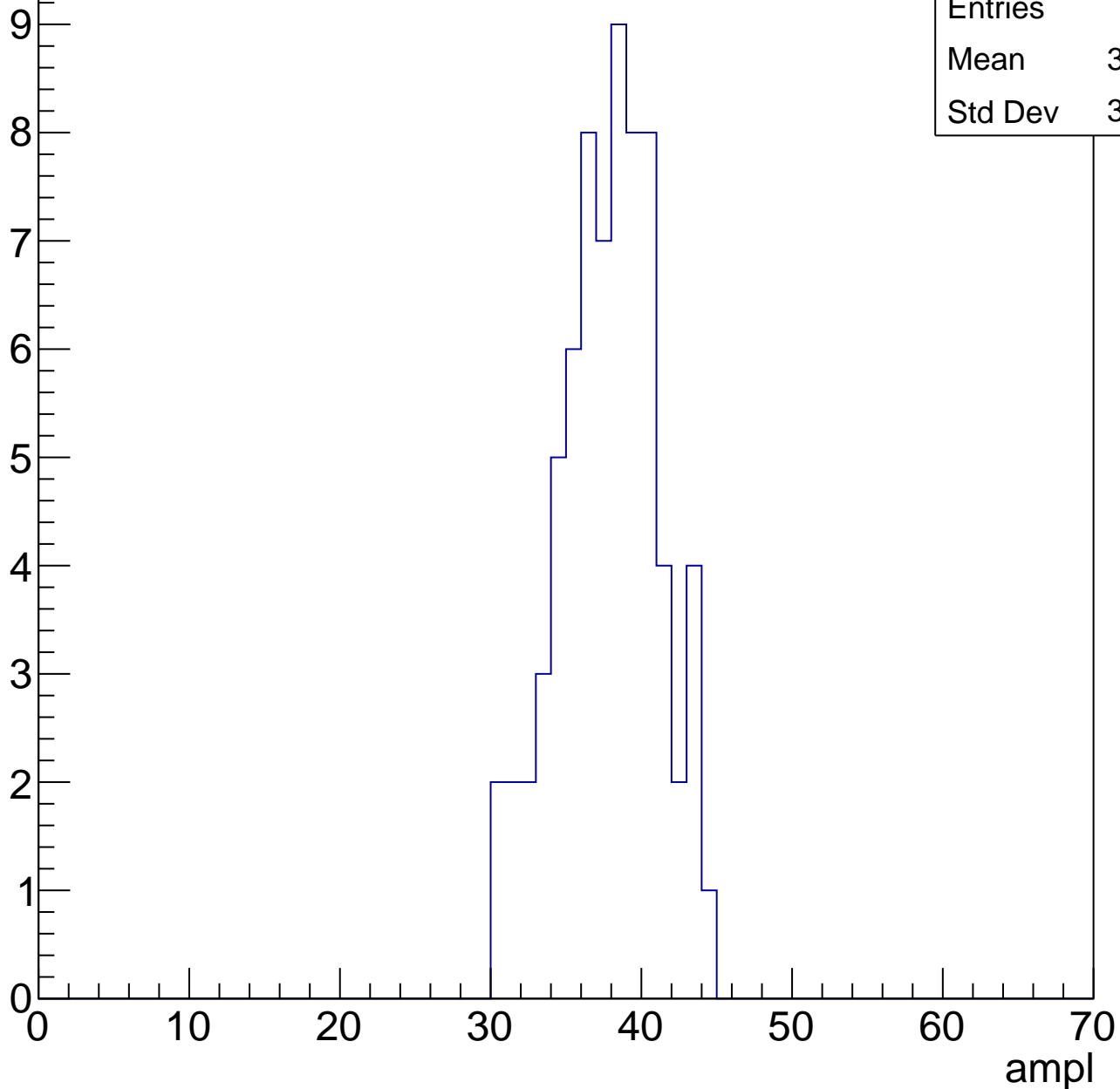
Entry



B1L103S, U23-ch123, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

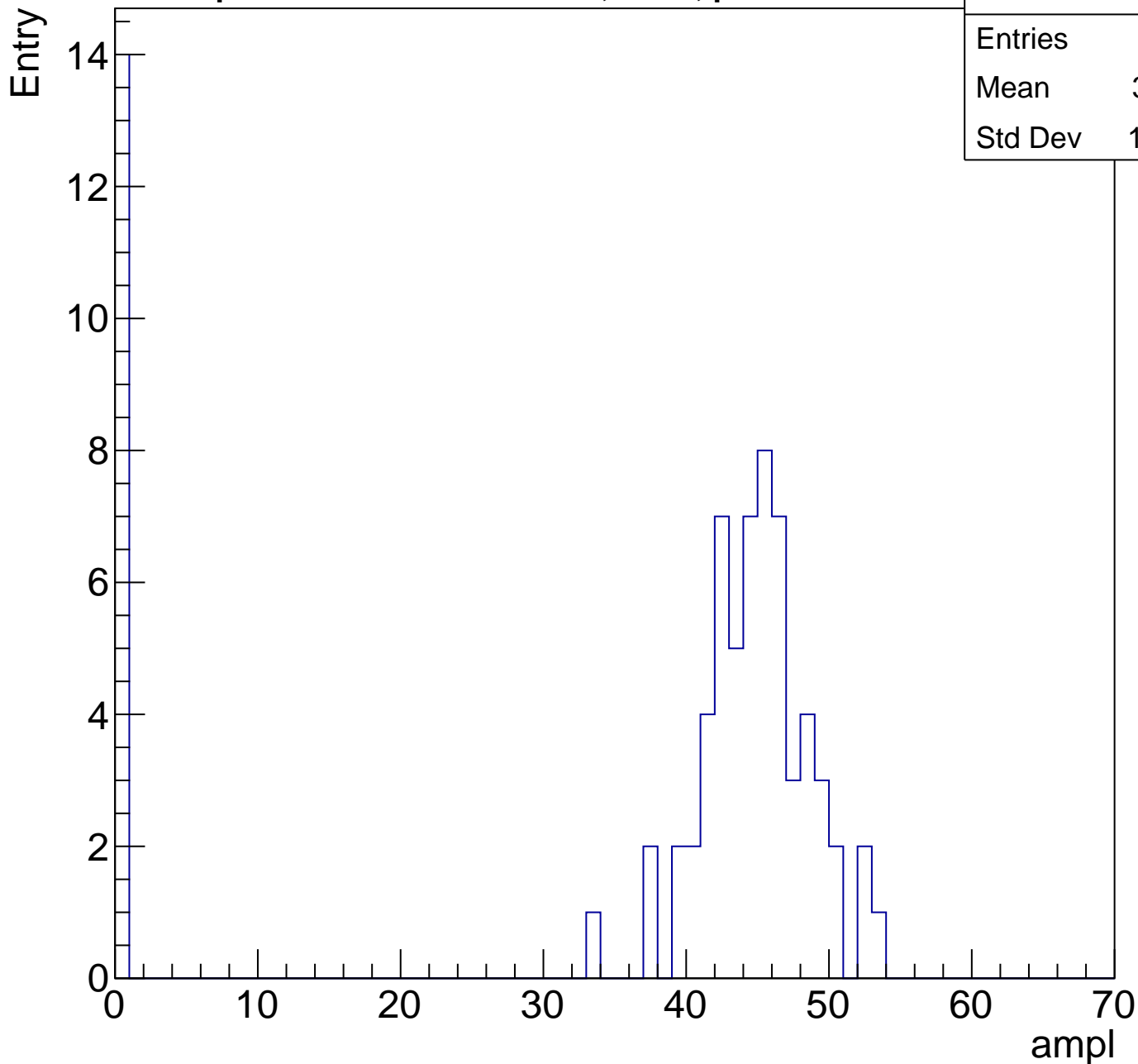


Entries	71
Mean	37.32
Std Dev	3.266

B1L103S, U23-ch123, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	74
Mean	36.01
Std Dev	17.72

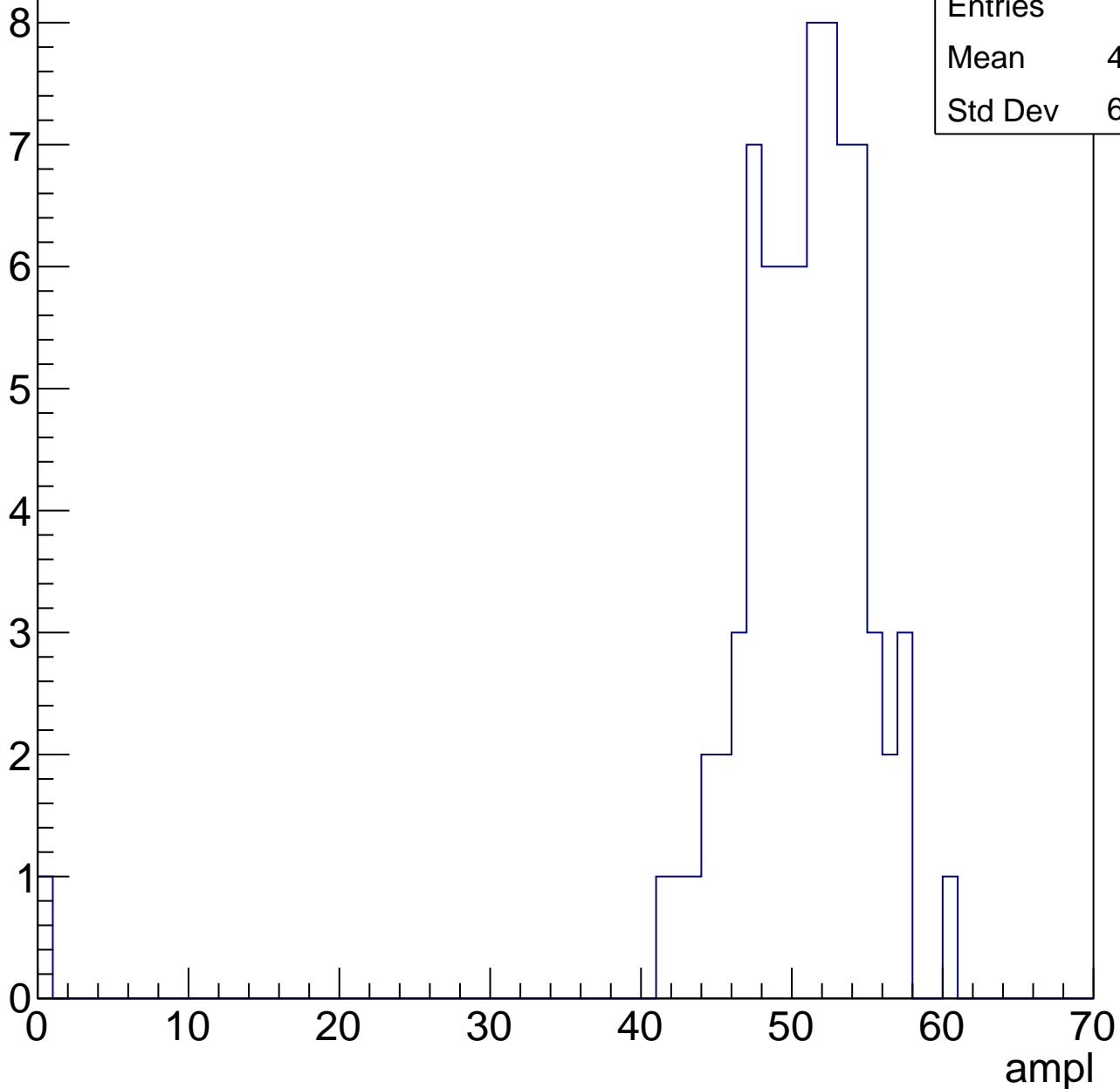


B1L103S, U23-ch123, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	75
Mean	49.79
Std Dev	6.892

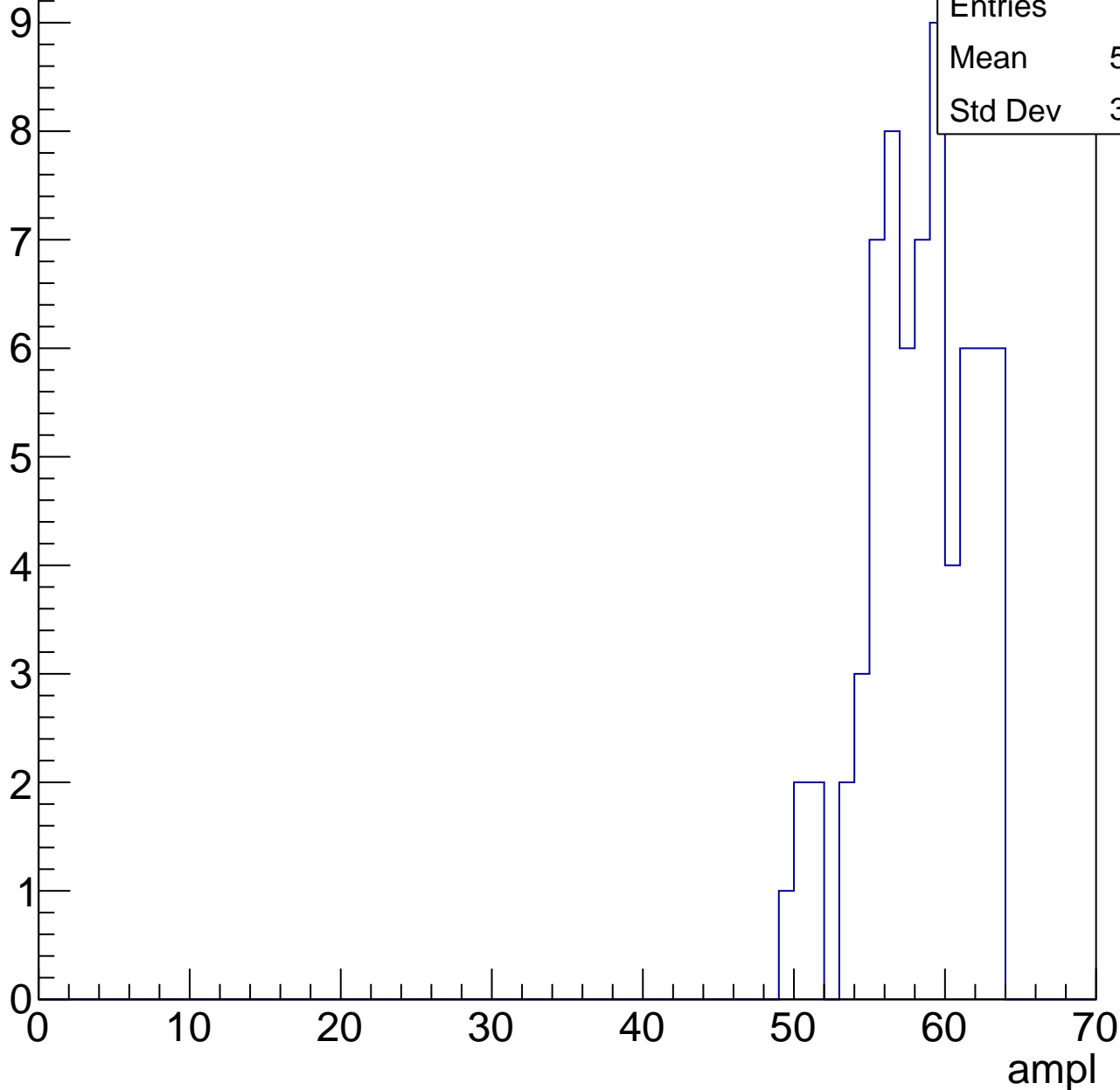


B1L103S, U23-ch123, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	57.78
Std Dev	3.464

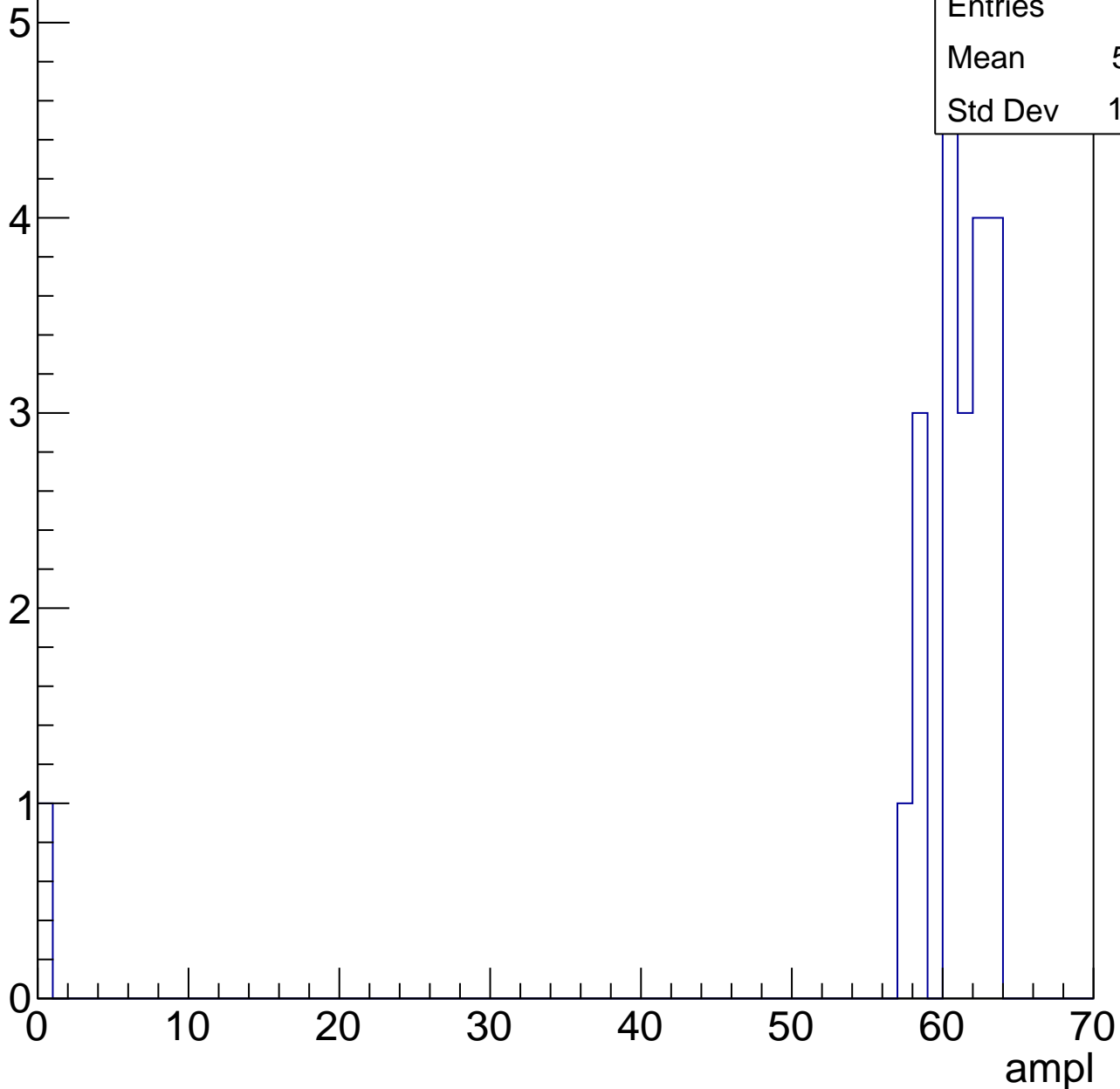


B1L103S, U23-ch123, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

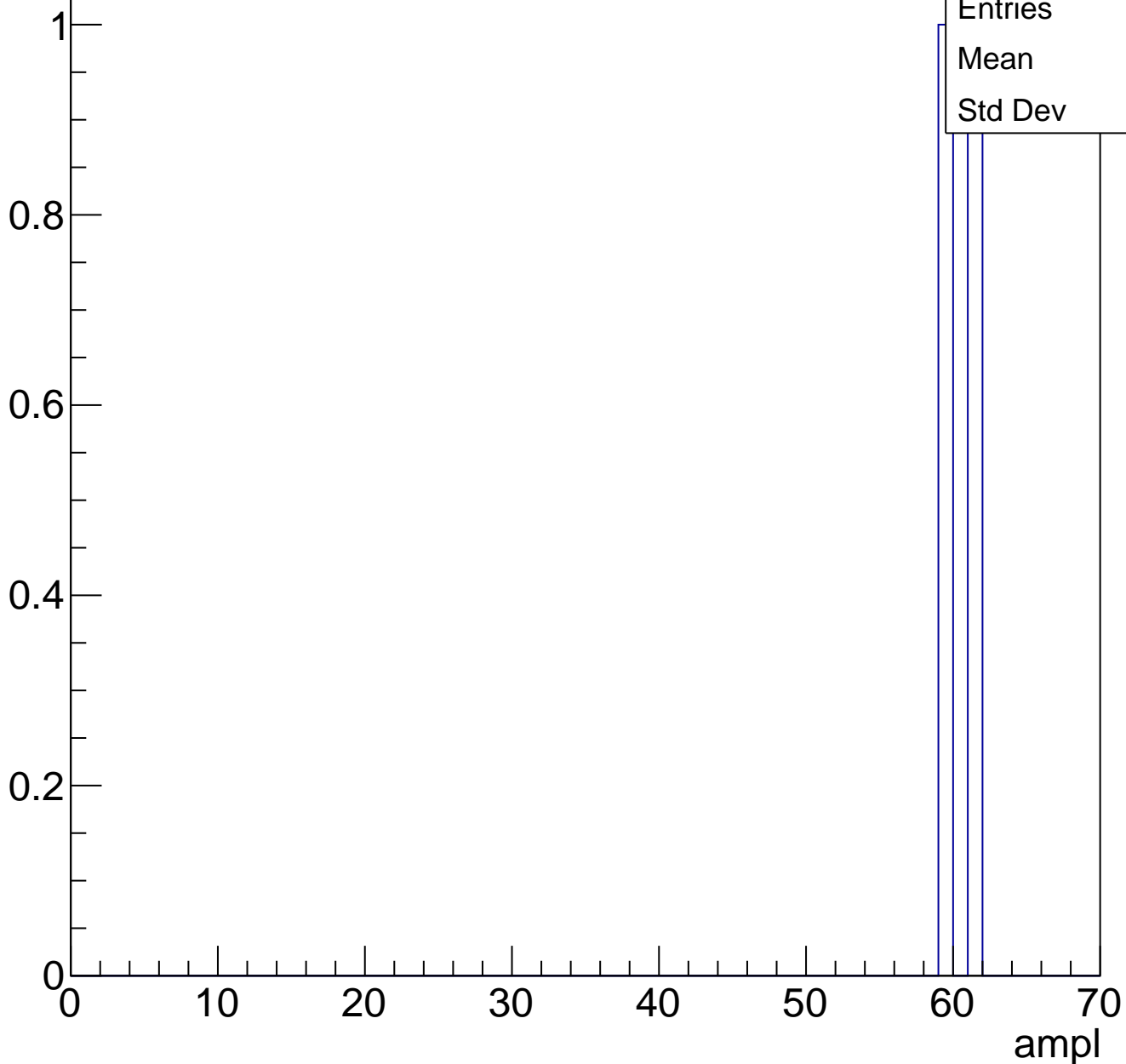
Entries	21
Mean	57.81
Std Dev	13.05



B1L103S, U23-ch123, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch123, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

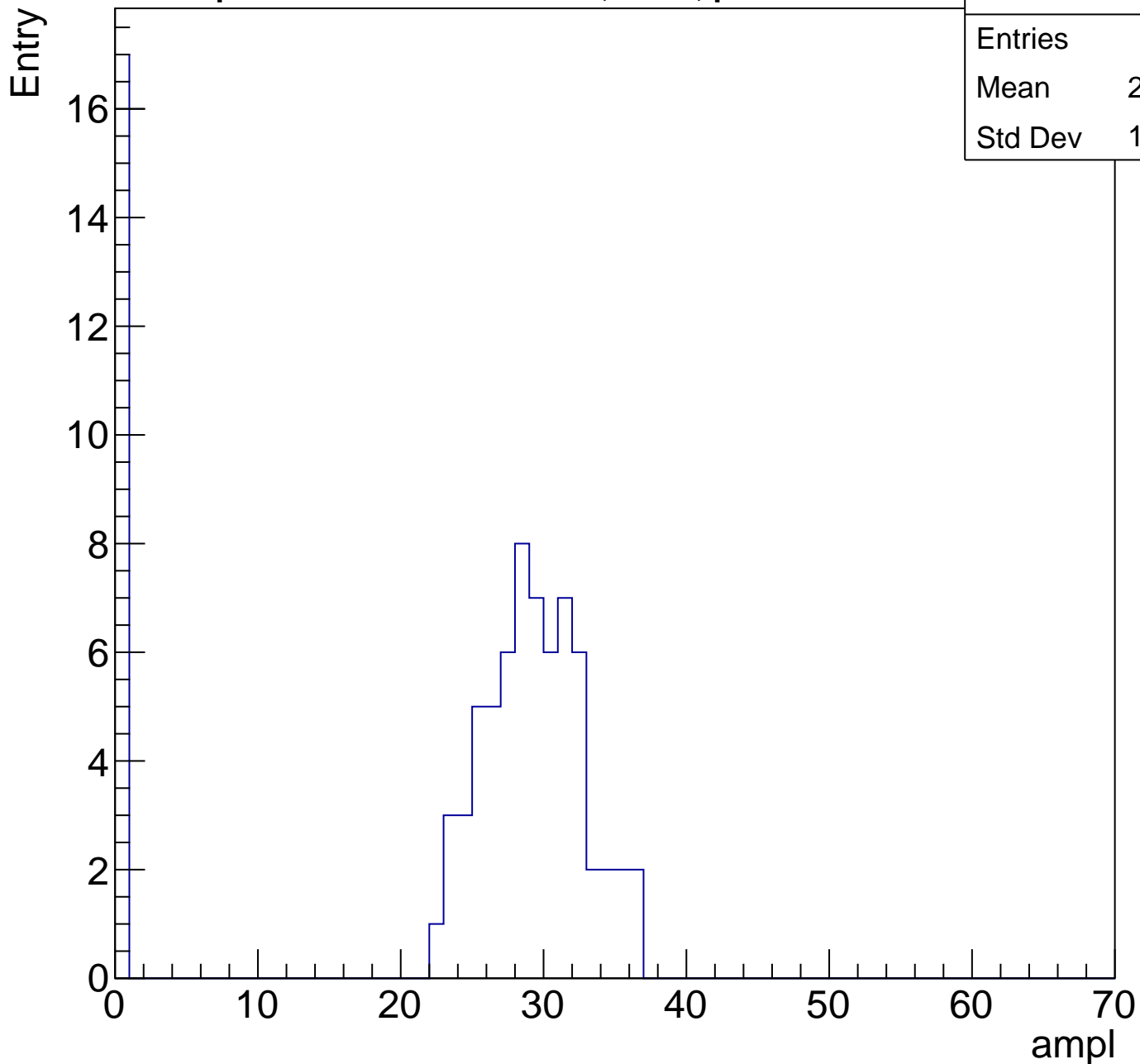
Entries	19
Mean	0
Std Dev	0

ampl

B1L103S, U23-ch124, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	82
Mean	22.83
Std Dev	12.05

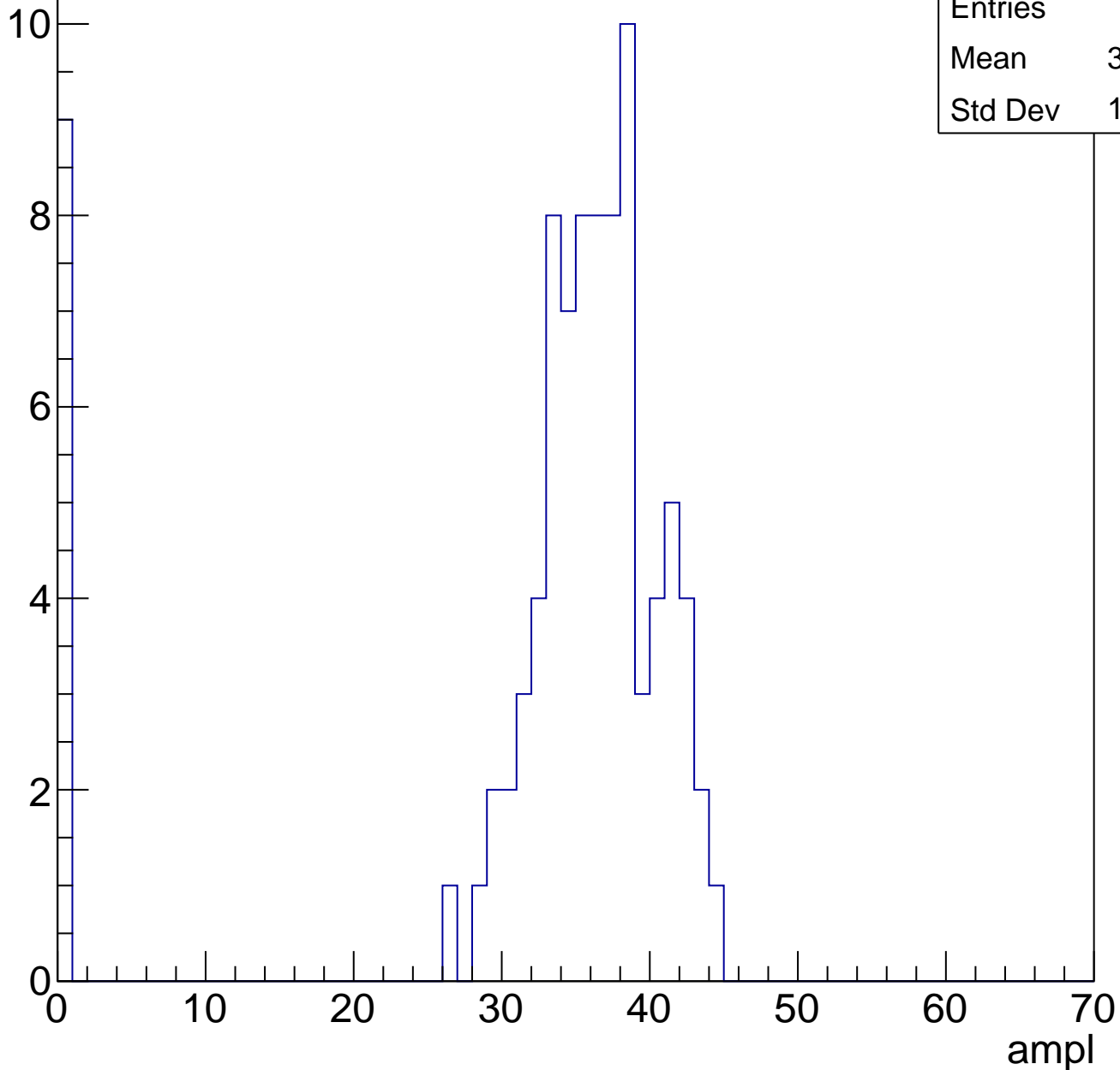


B1L103S, U23-ch124, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	90
Mean	32.43
Std Dev	11.39

Entry

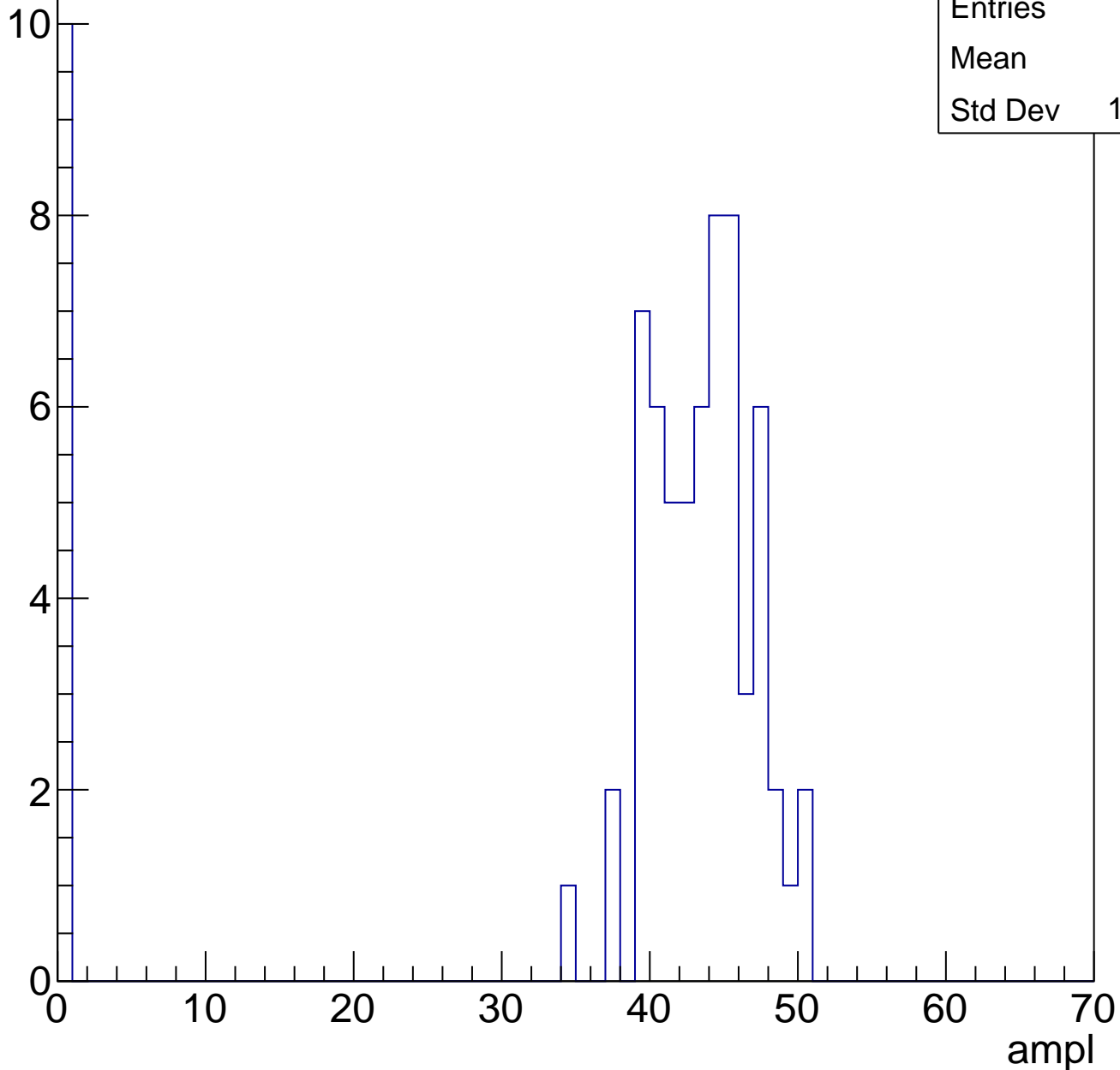


B1L103S, U23-ch124, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	72
Mean	37.1
Std Dev	15.22

Entry

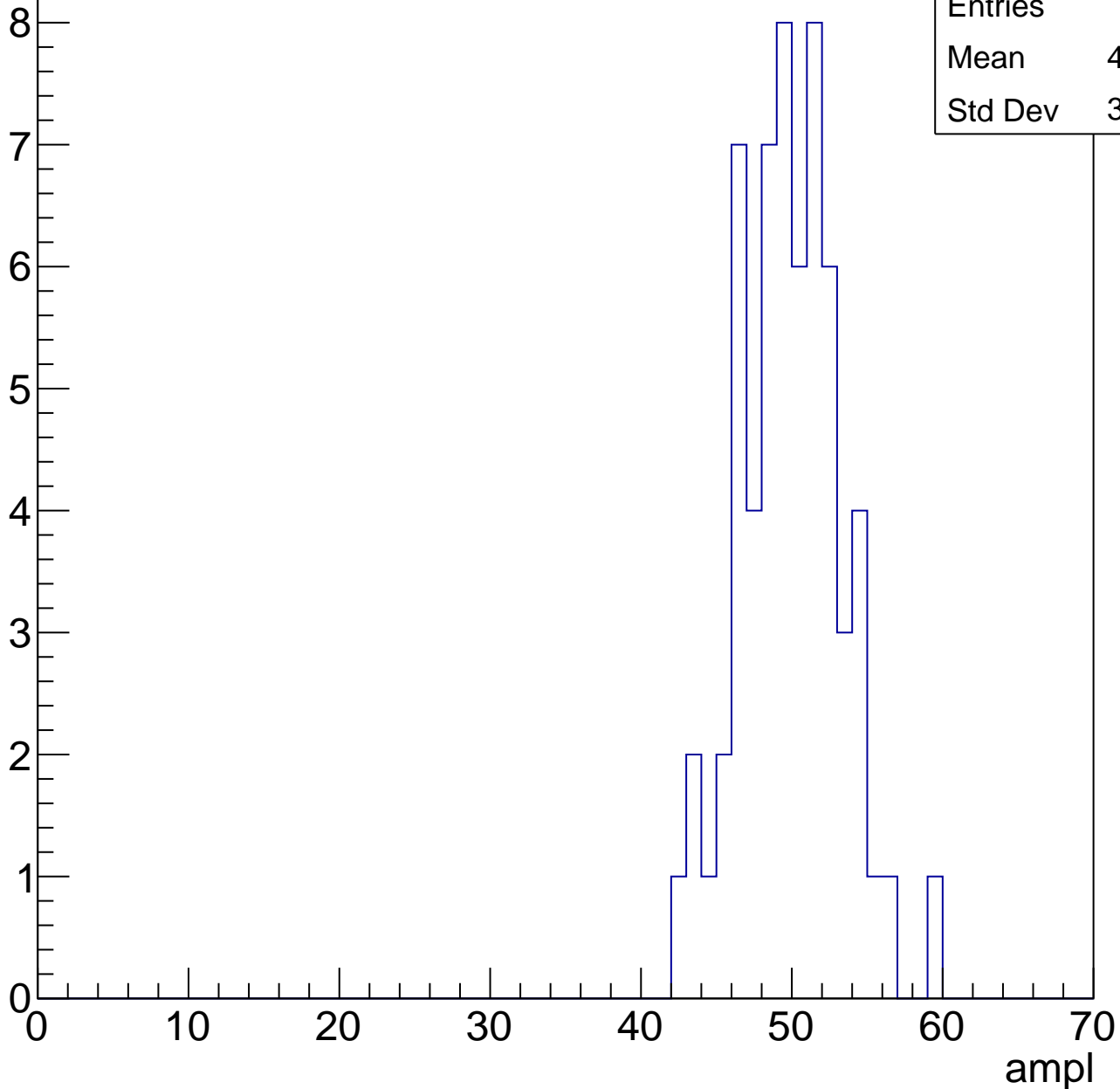


B1L103S, U23-ch124, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	49.44
Std Dev	3.305

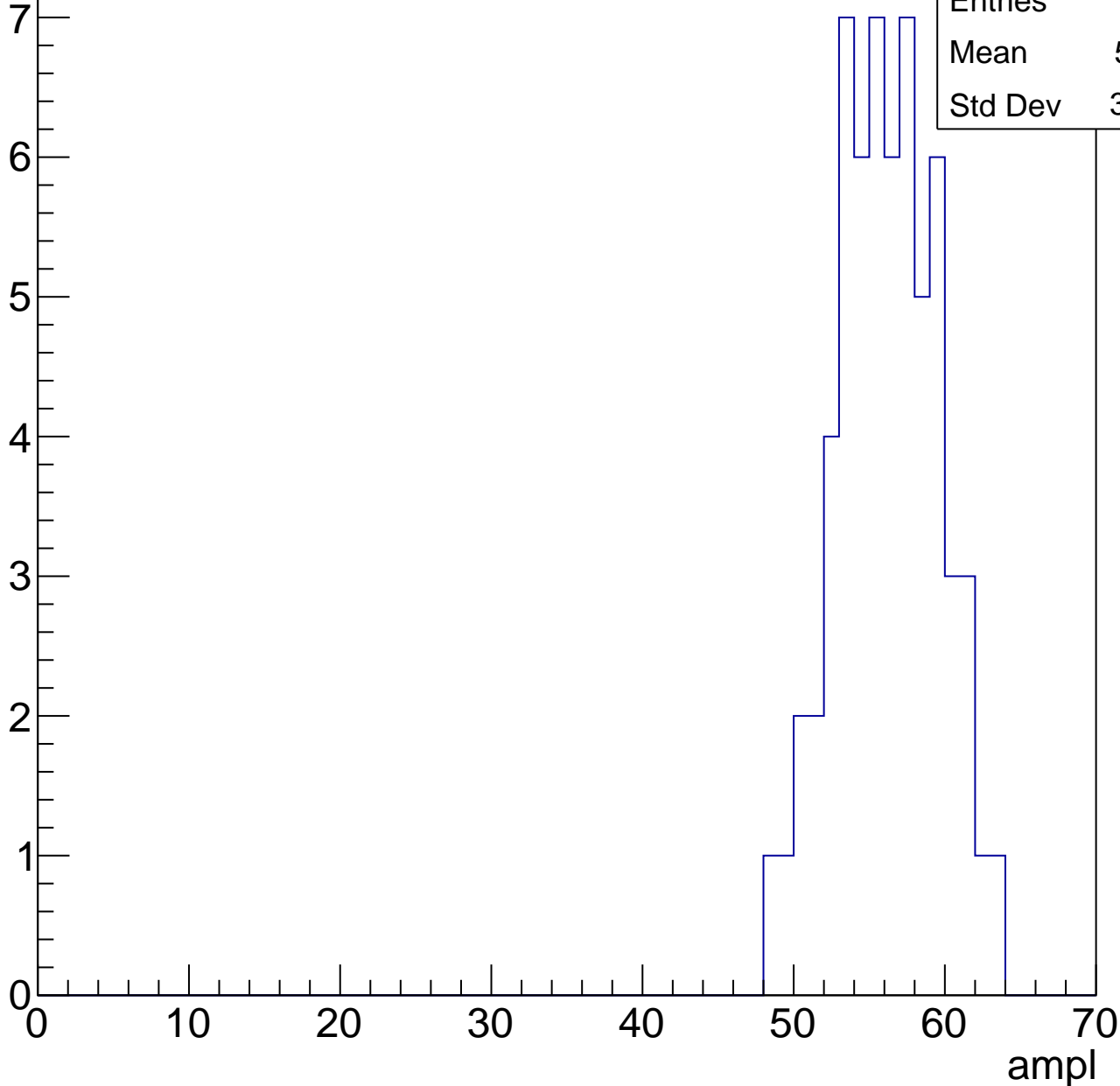


B1L103S, U23-ch124, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	55.71
Std Dev	3.304

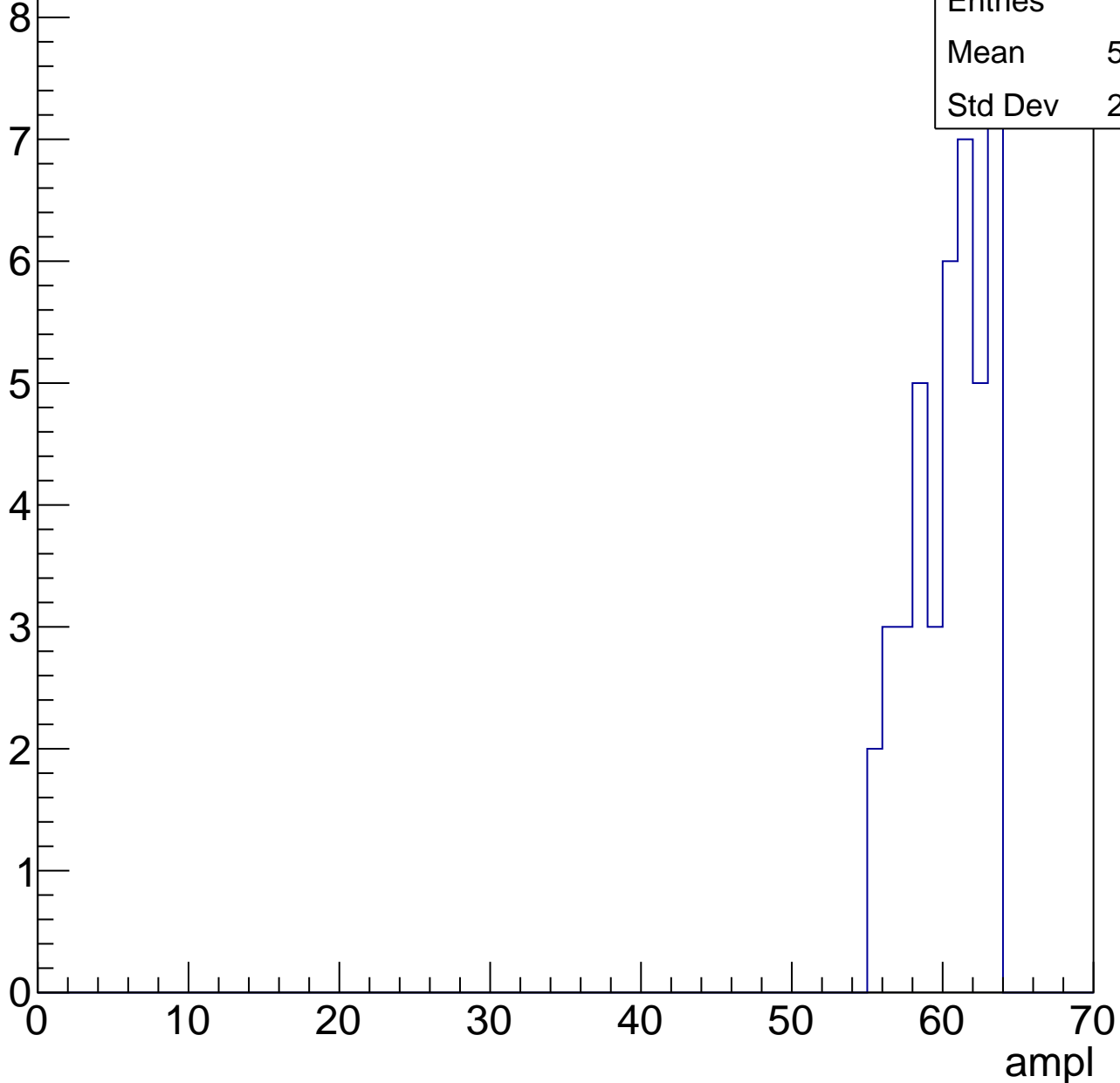


B1L103S, U23-ch124, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

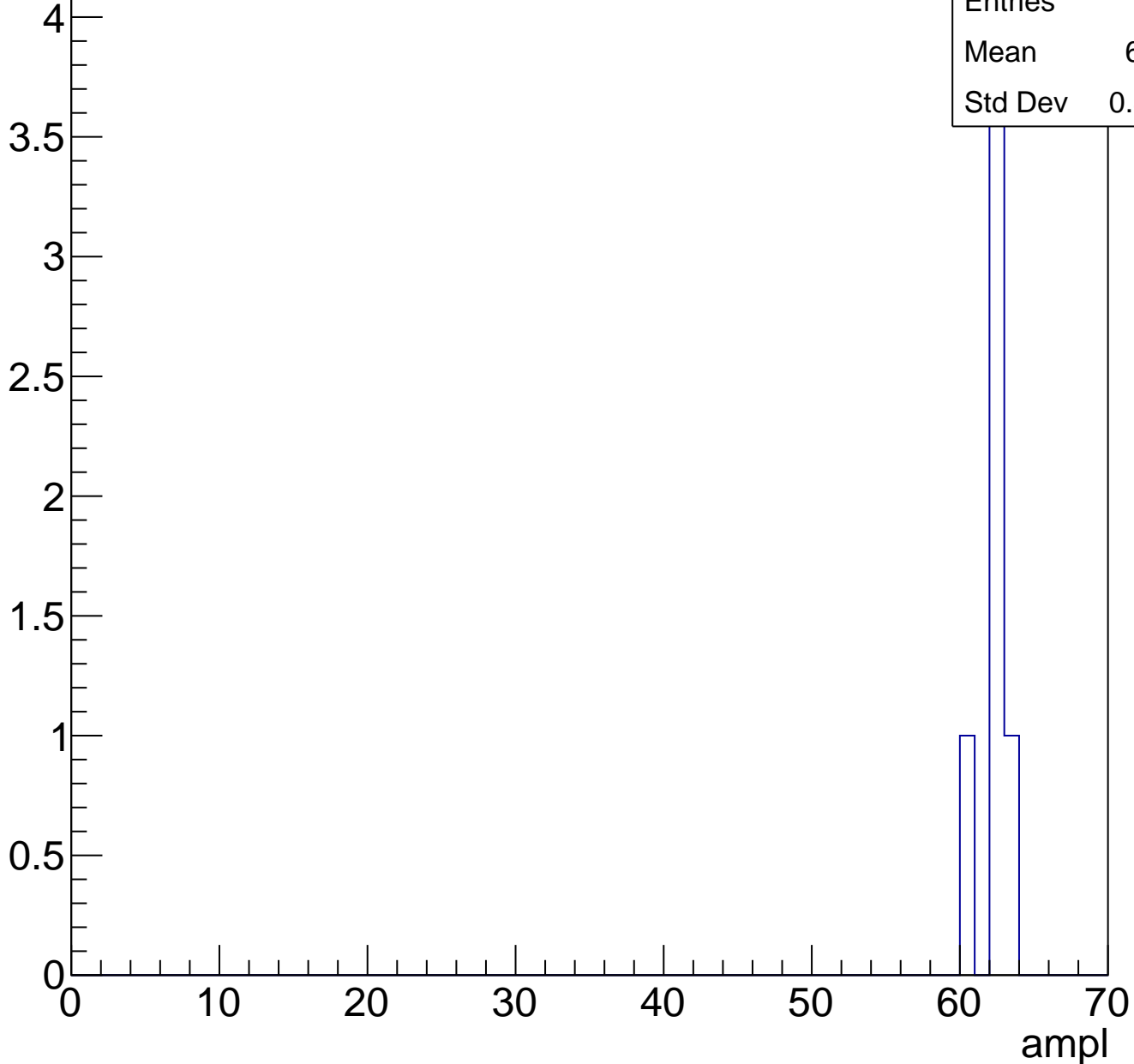
Entries	42
Mean	59.93
Std Dev	2.424



B1L103S, U23-ch124, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U23-ch124, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

20
18
16
14
12
10
8
6
4
2
0

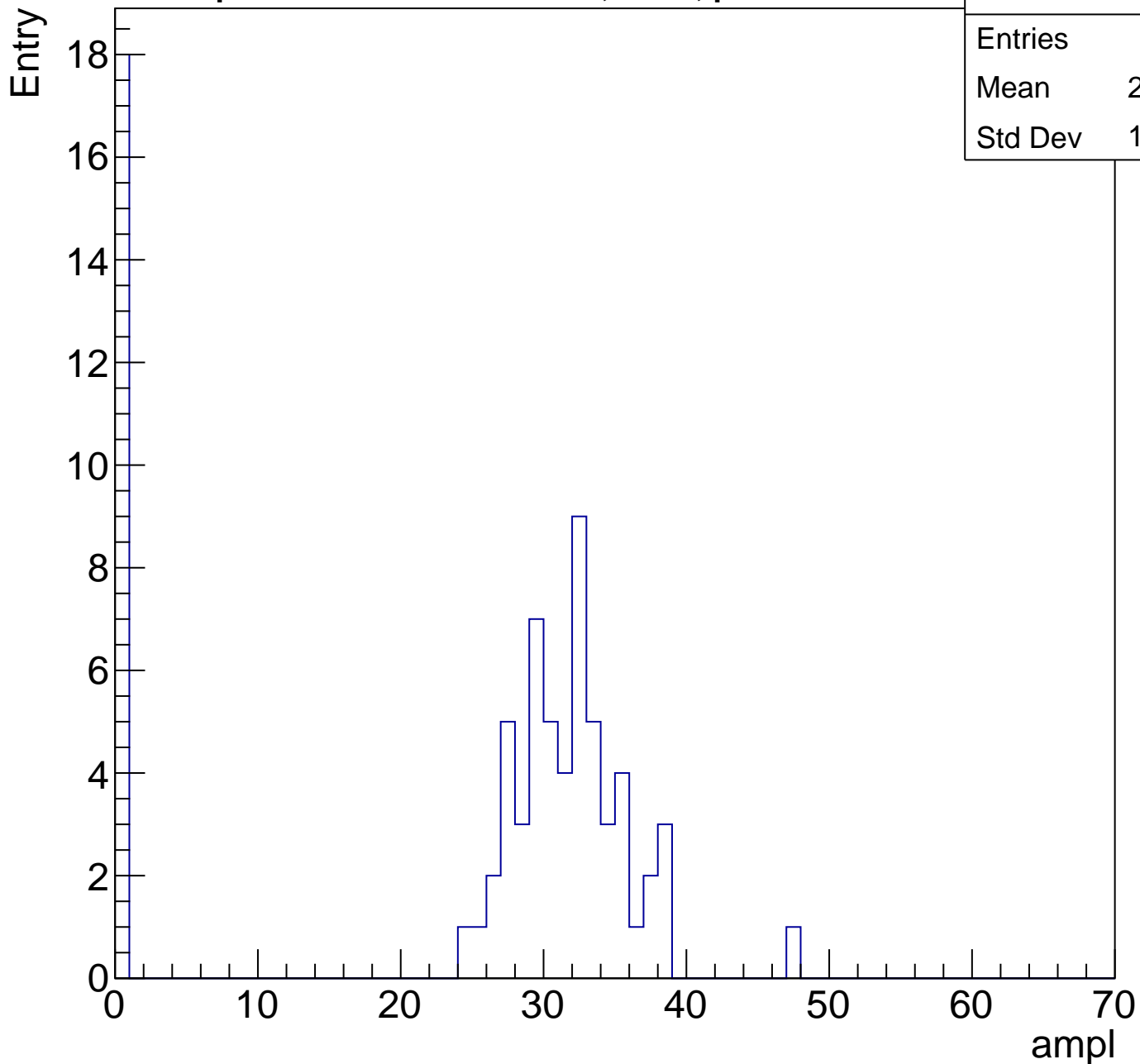
Entries	20
Mean	0
Std Dev	0

ampl

B1L103S, U23-ch125, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	74
Mean	23.82
Std Dev	13.94



B1L103S, U23-ch125, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	65
Mean	28.86
Std Dev	14.69

Entry

12

10

8

6

4

2

0

0

10

20

30

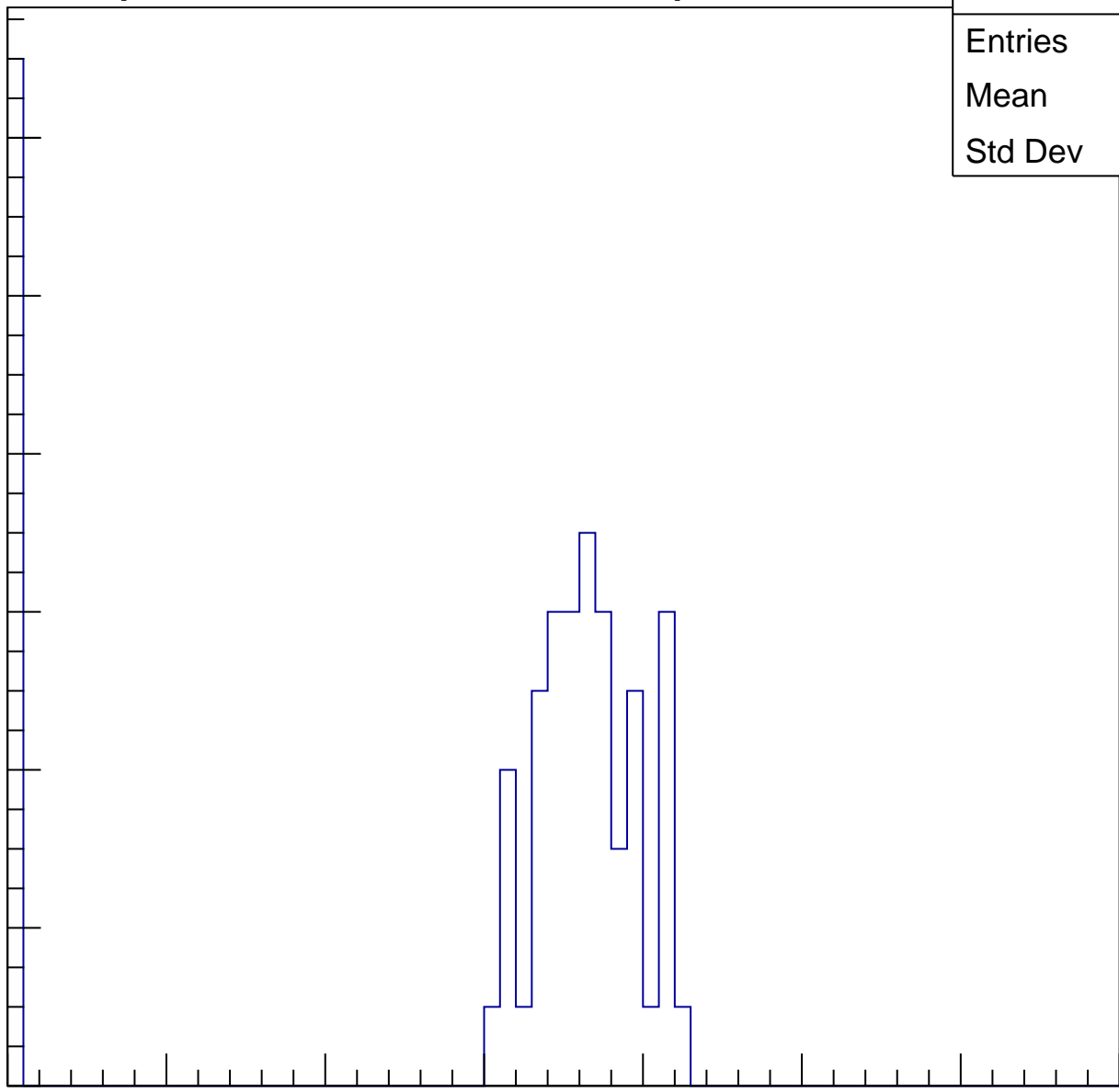
40

50

60

70

ampl

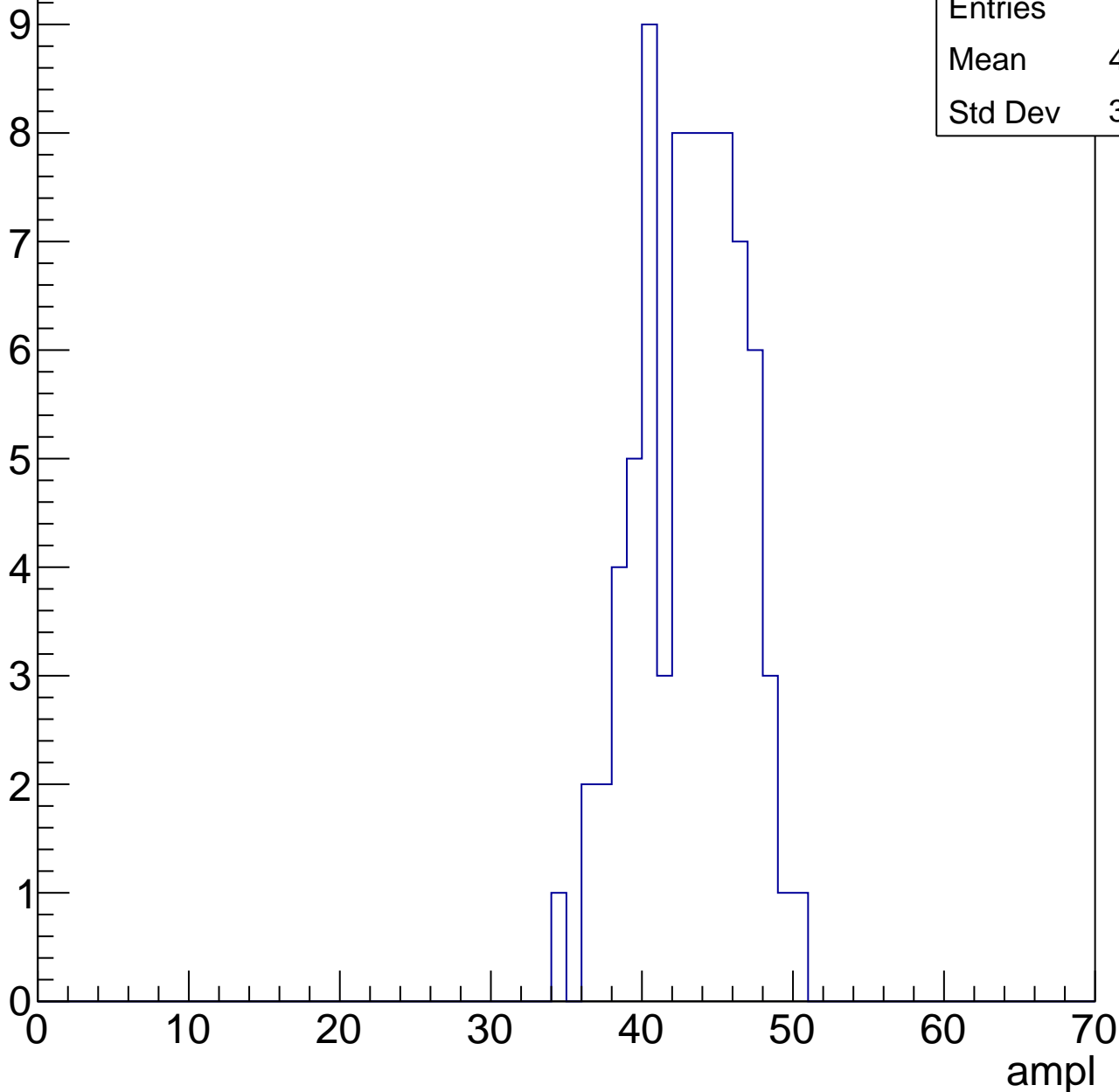


B1L103S, U23-ch125, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	76
Mean	42.75
Std Dev	3.415

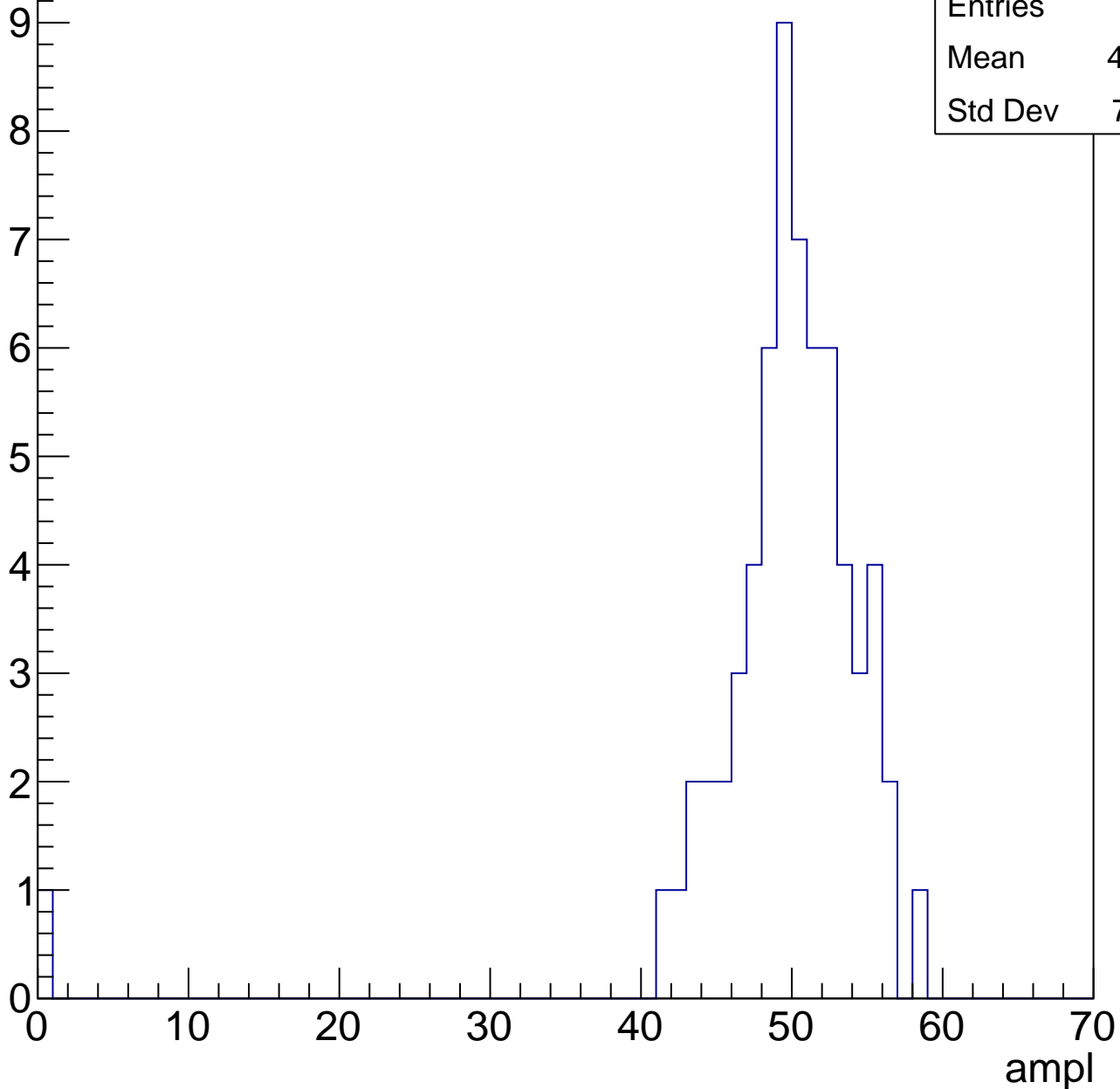


B1L103S, U23-ch125, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	48.97
Std Dev	7.141

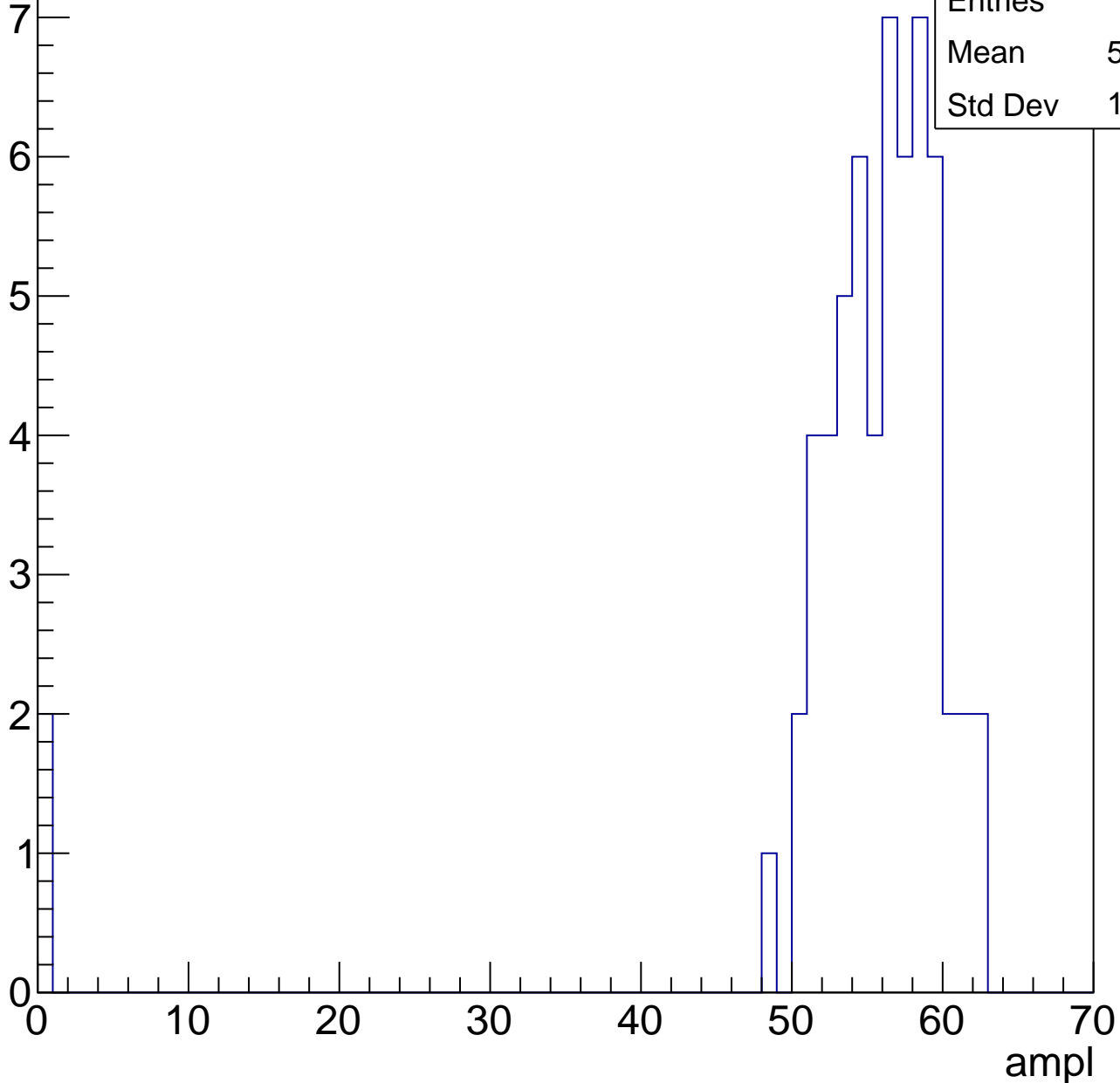


B1L103S, U23-ch125, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	53.82
Std Dev	10.49

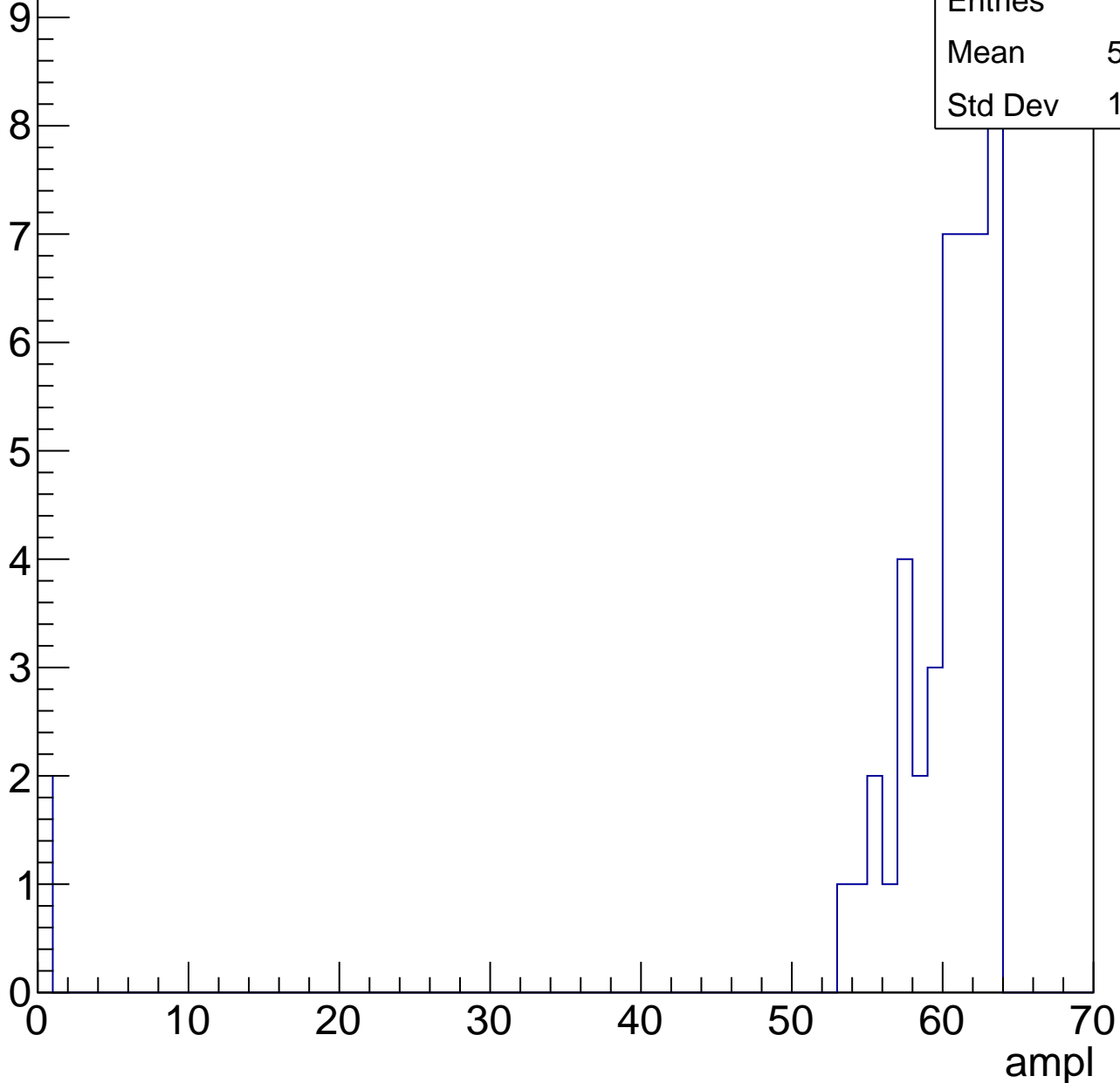


B1L103S, U23-ch125, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	46
Mean	57.43
Std Dev	12.52



B1L103S, U23-ch125, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

5

Mean

61

Std Dev

1.414

B1L103S, U23-ch125, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

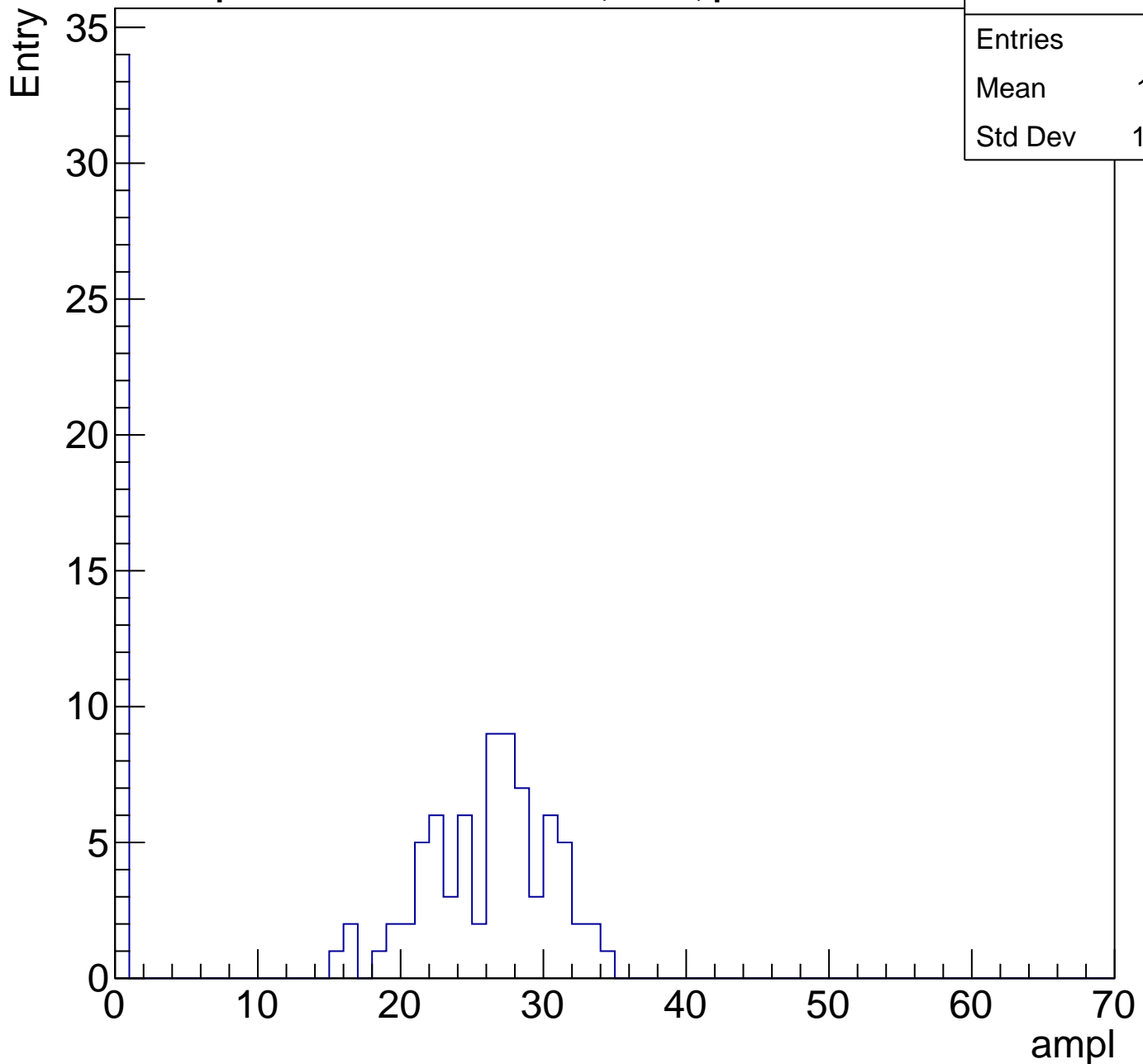
Entries	19
Mean	0
Std Dev	0

ampl

B1L103S, U23-ch126, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	108
Mean	17.61
Std Dev	12.45



B1L103S, U23-ch126, adc1

calib_packv5_041523_1651.root, FC#0, port C2

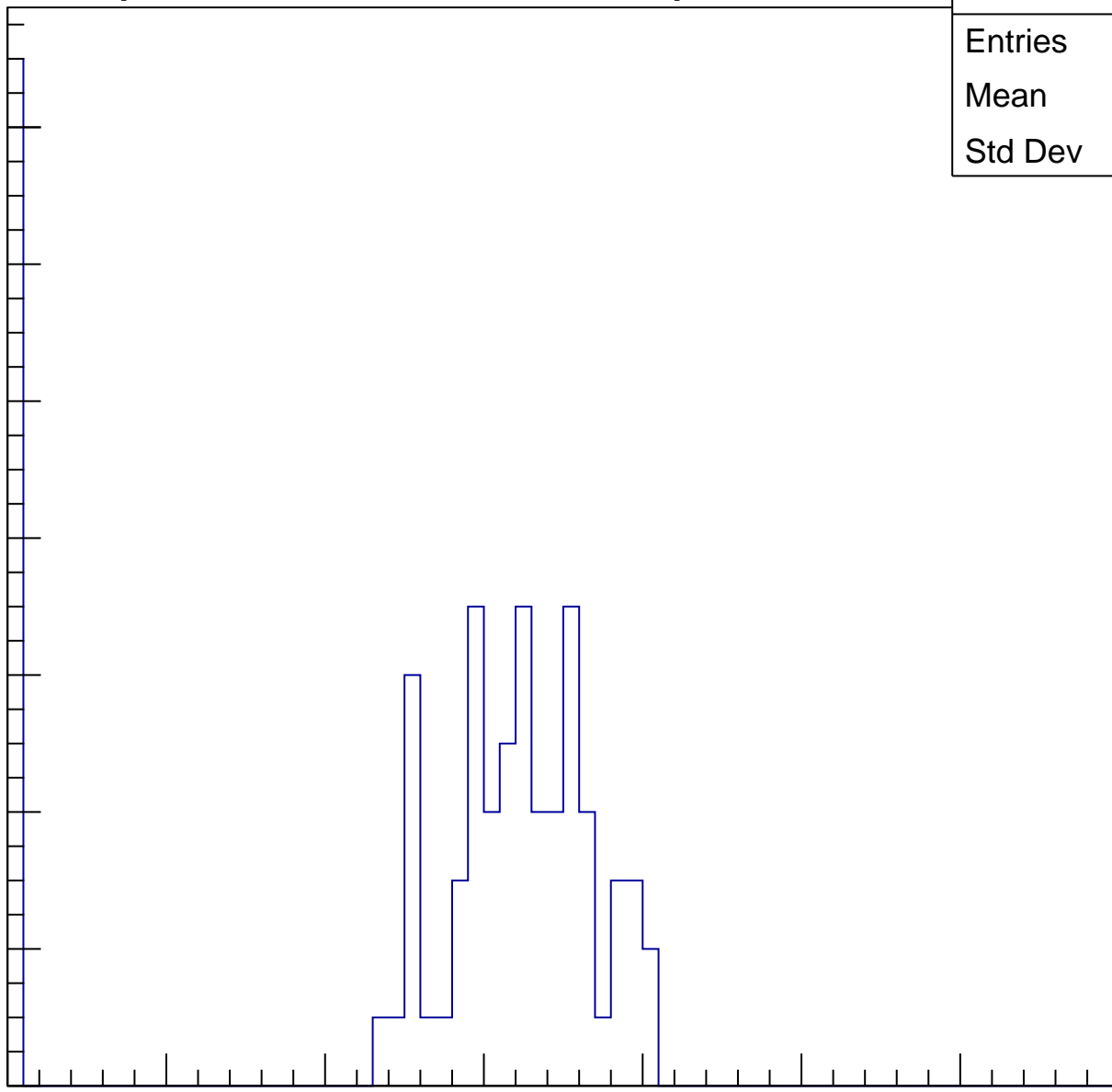
Entries	79
Mean	25.84
Std Dev	13.09

Entry

14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

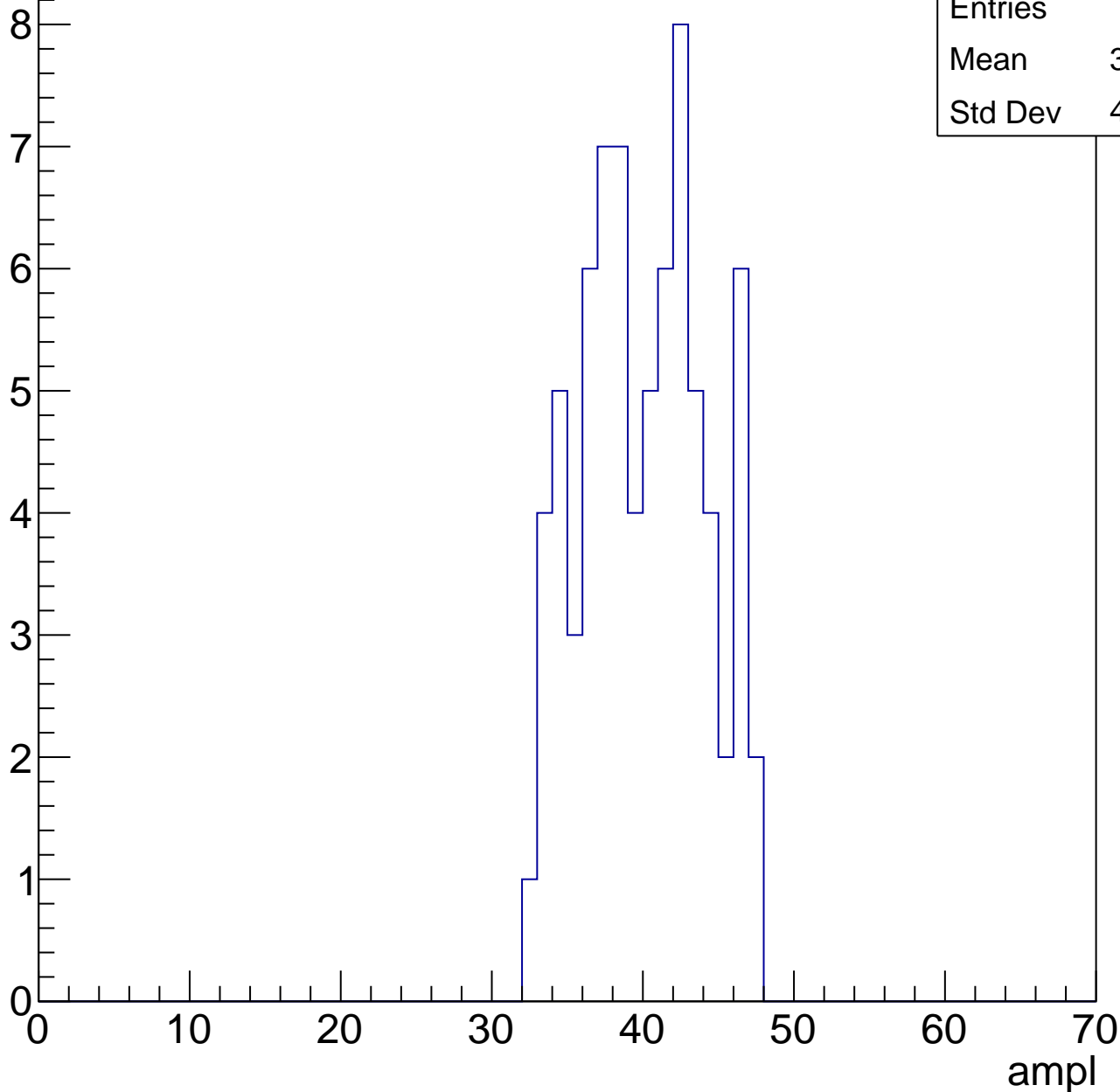


B1L103S, U23-ch126, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	75
Mean	39.59
Std Dev	4.007

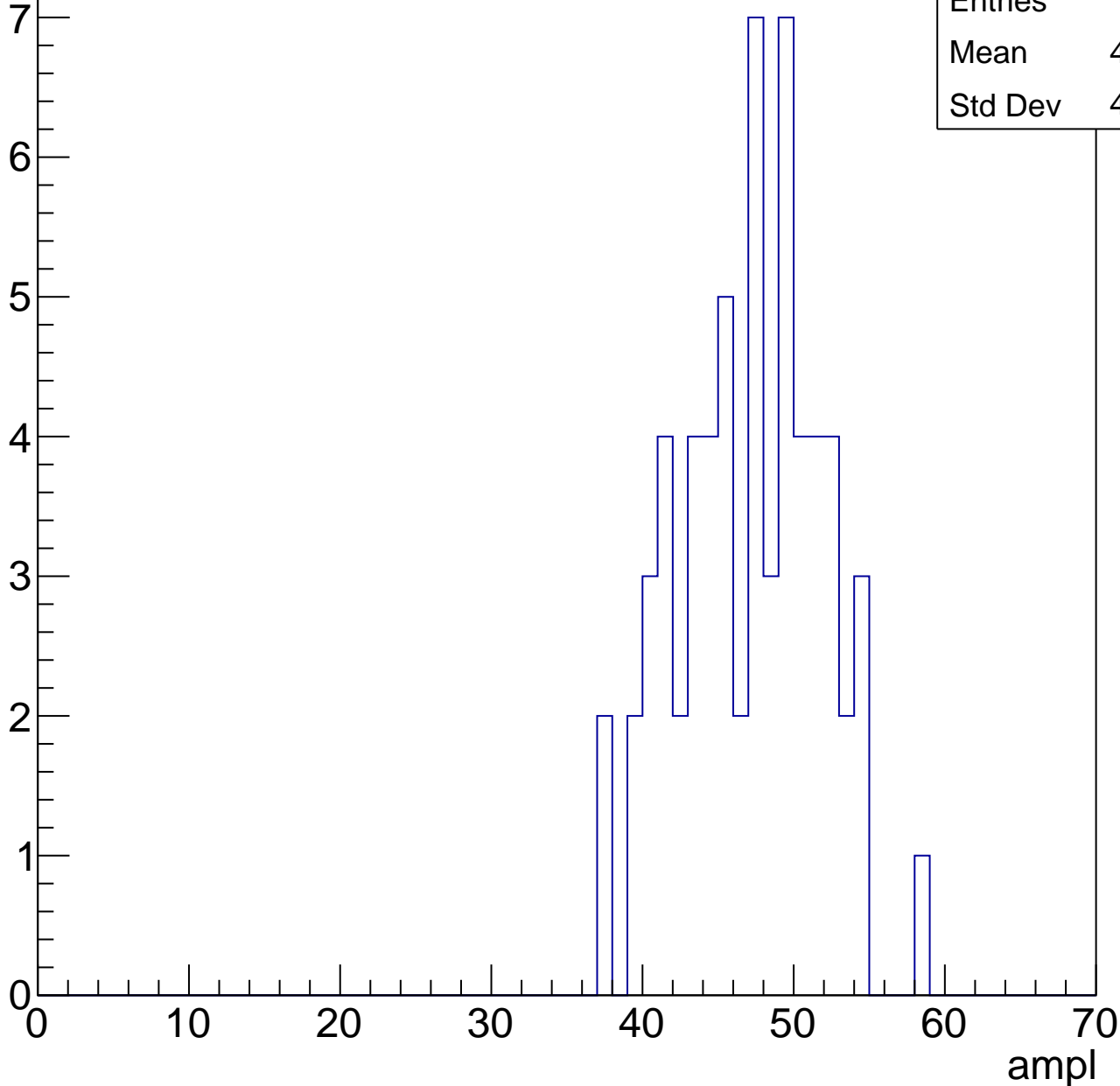


B1L103S, U23-ch126, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	63
Mean	46.65
Std Dev	4.636

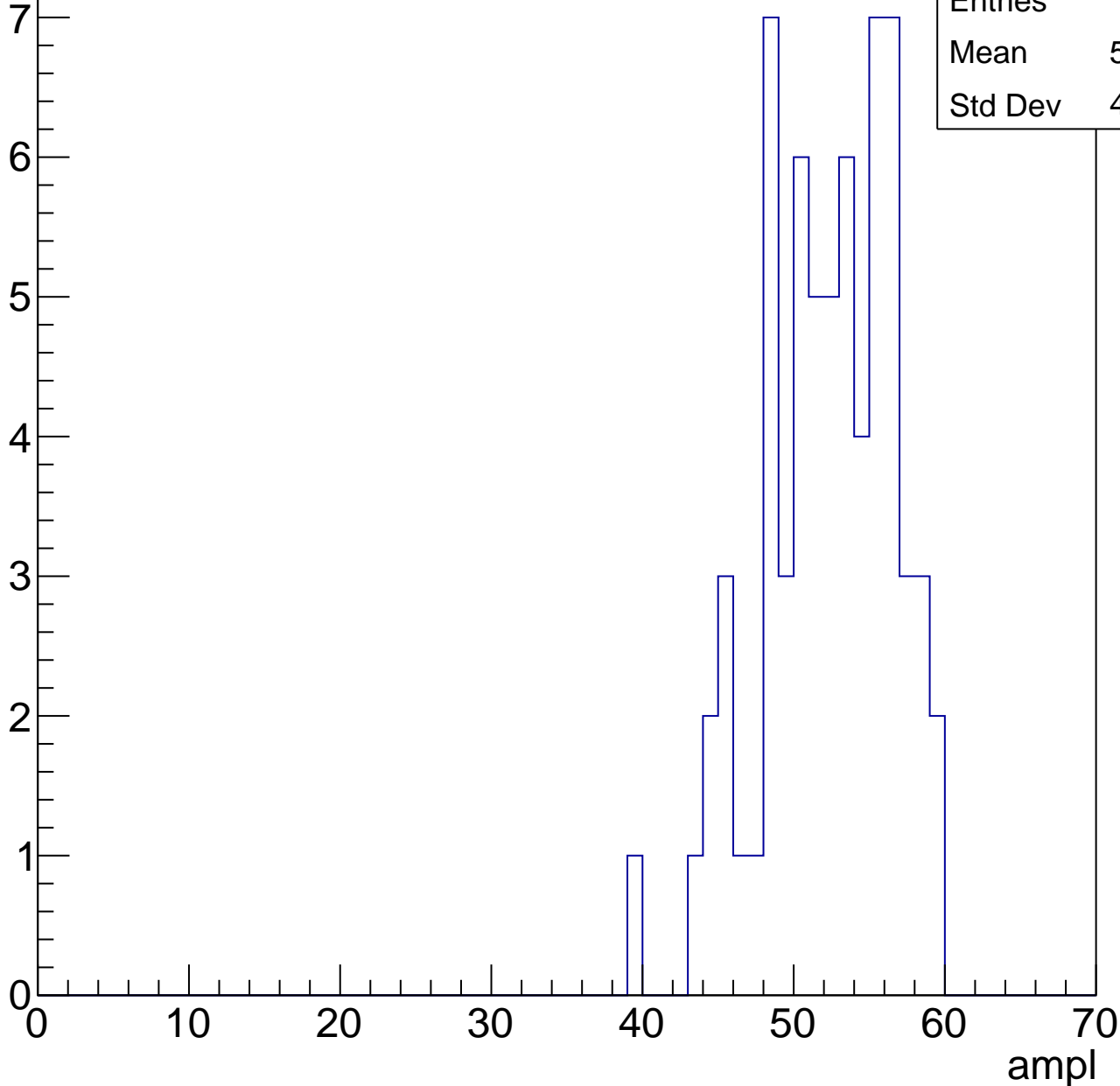


B1L103S, U23-ch126, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	51.79
Std Dev	4.283

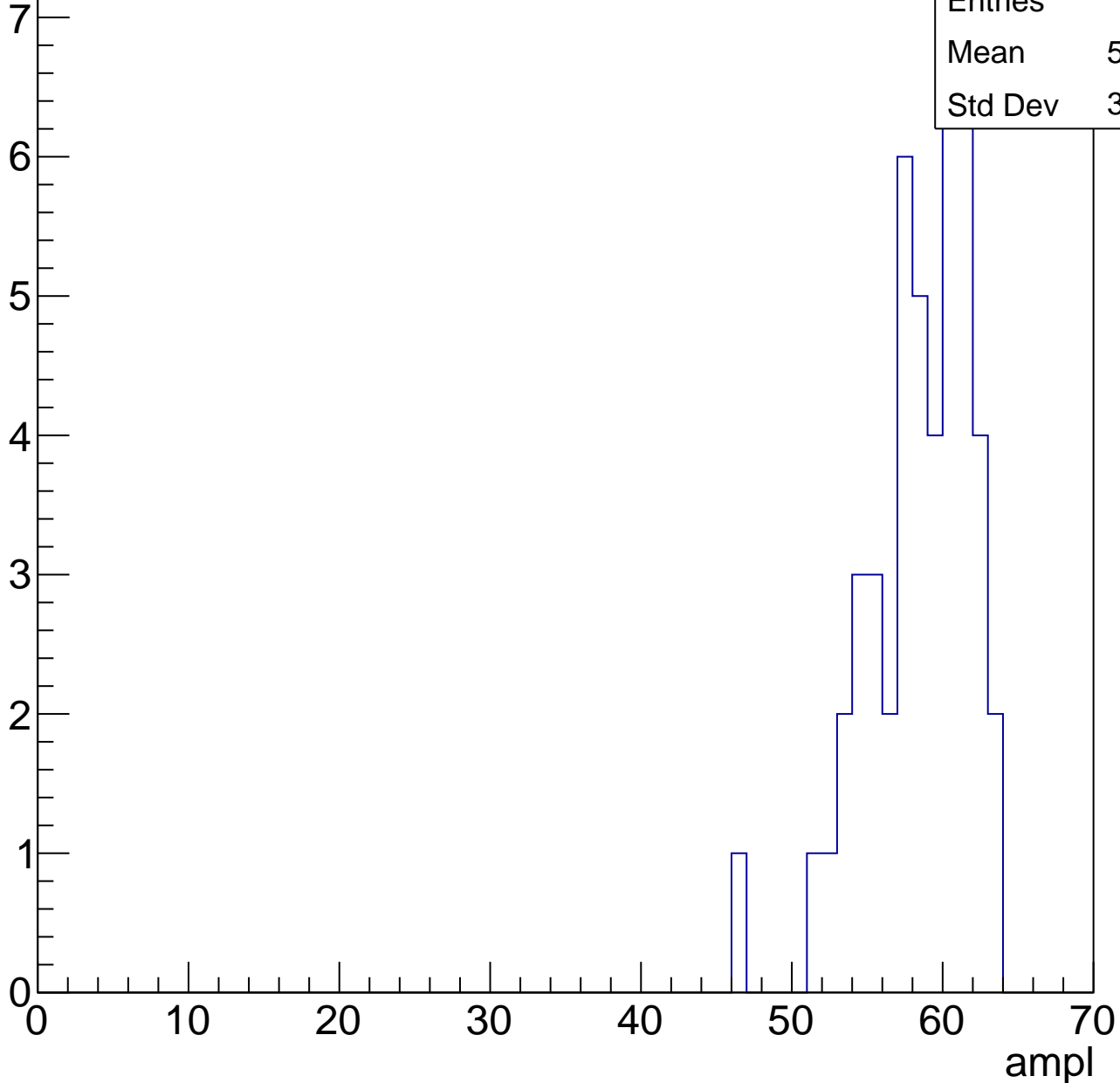


B1L103S, U23-ch126, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	48
Mean	57.98
Std Dev	3.467

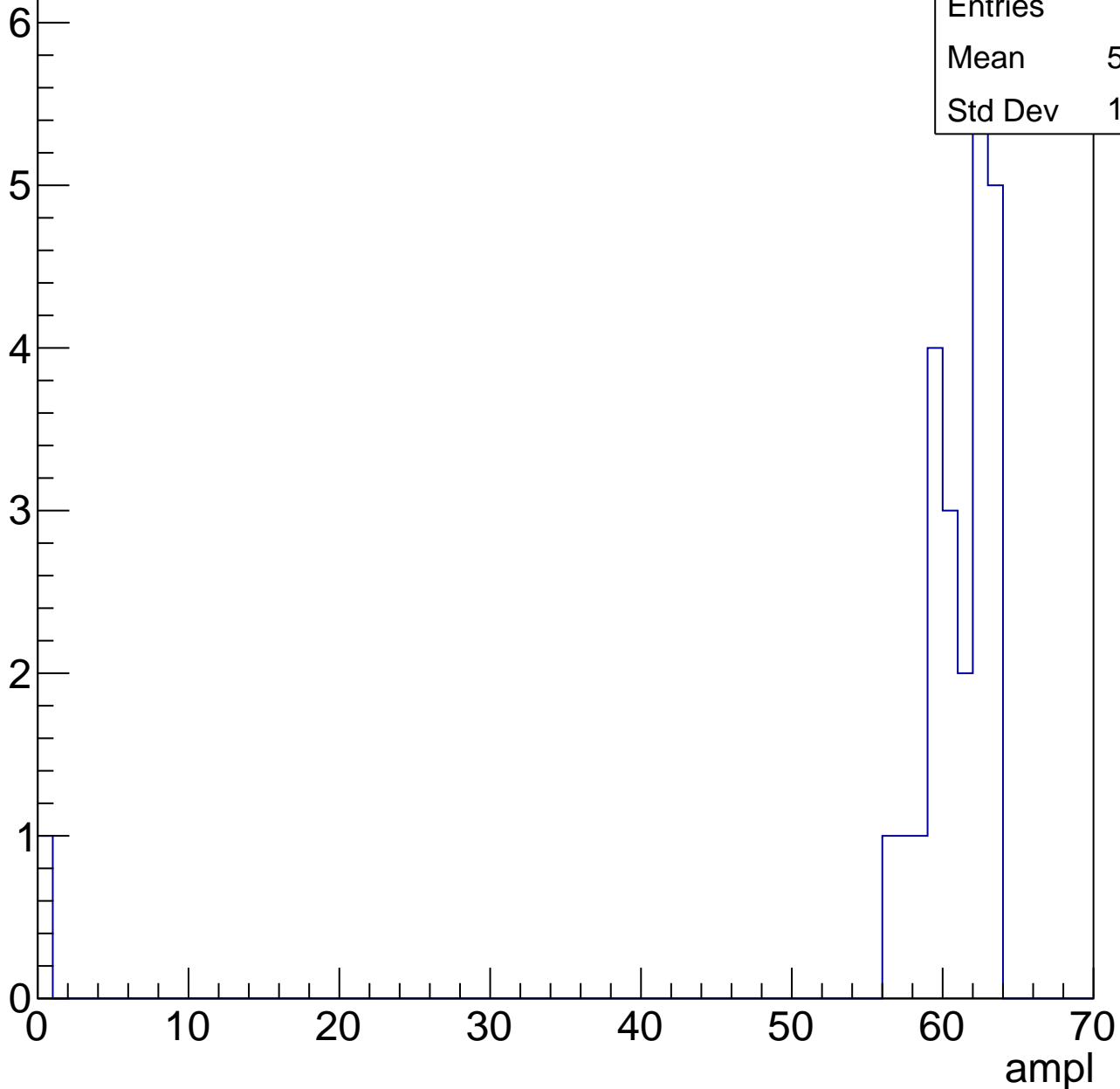


B1L103S, U23-ch126, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	24
Mean	58.17
Std Dev	12.29

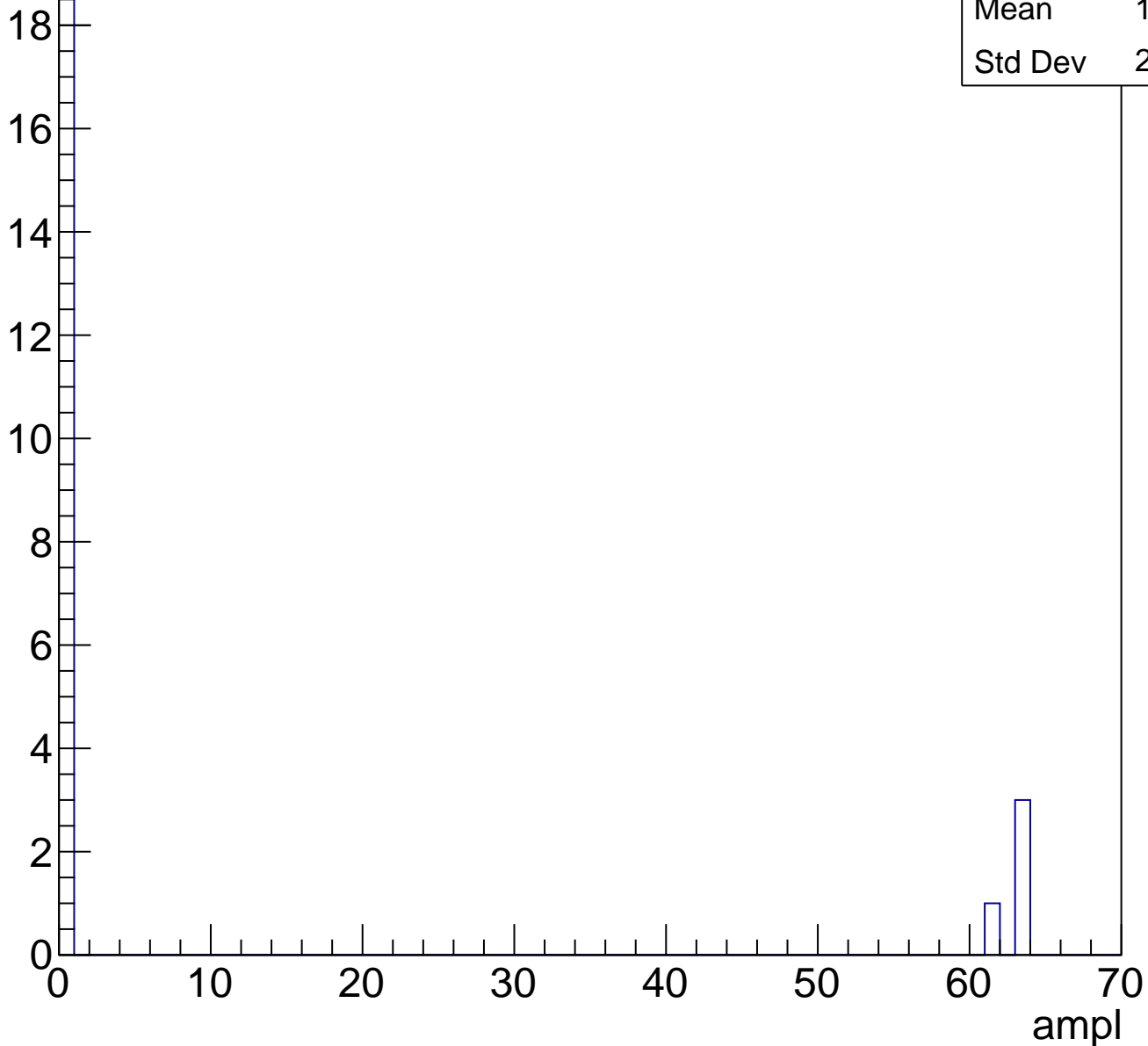


B1L103S, U23-ch126, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	23
Mean	10.87
Std Dev	23.69

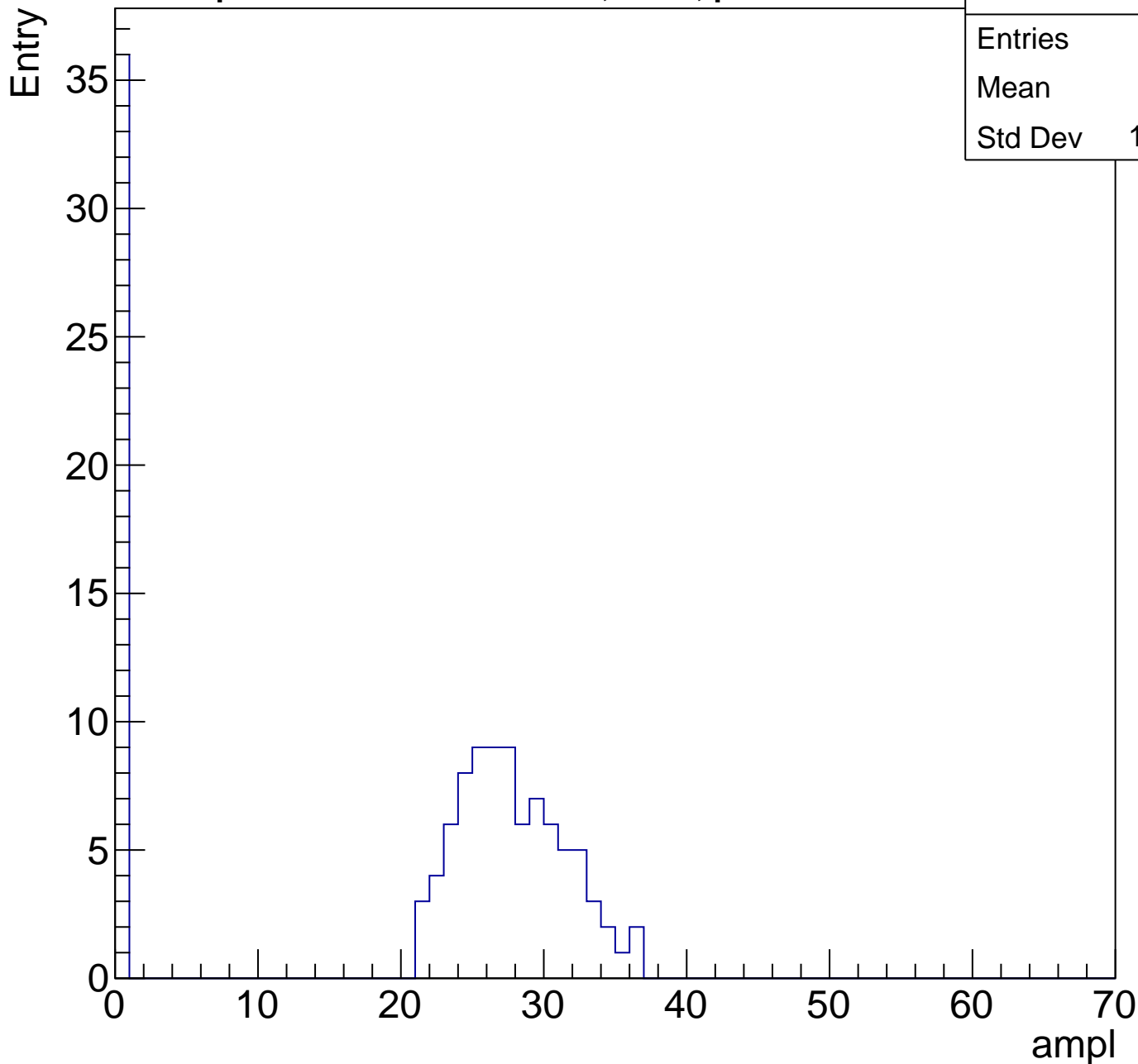
Entry



B1L103S, U23-ch127, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	121
Mean	19.2
Std Dev	12.86



B1L103S, U23-ch127, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	86
Mean	30.43
Std Dev	12.16

Entry

10

8

6

4

2

0

ampl

0

10

20

30

40

50

60

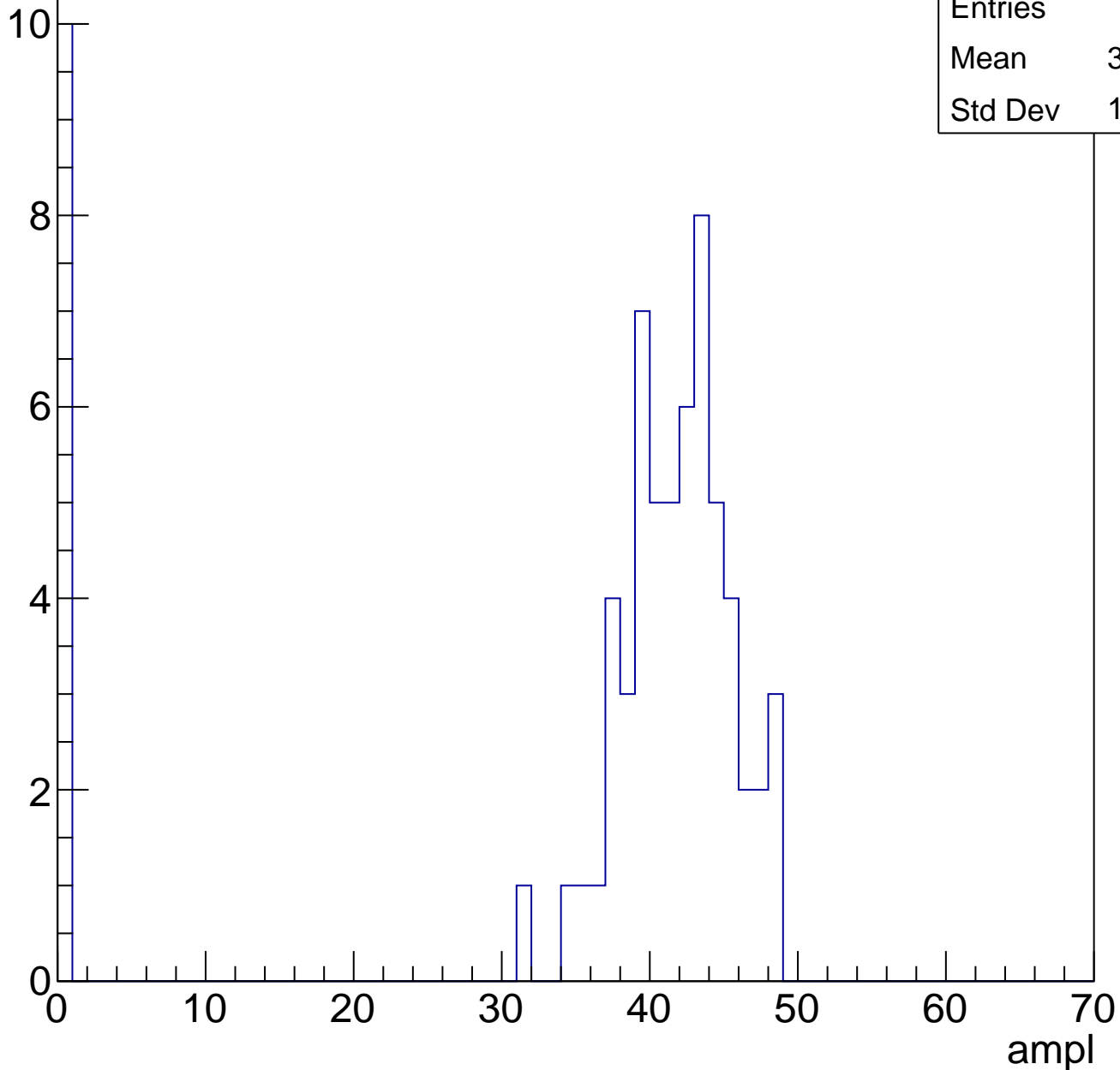
70

B1L103S, U23-ch127, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	68
Mean	35.32
Std Dev	15.03

Entry

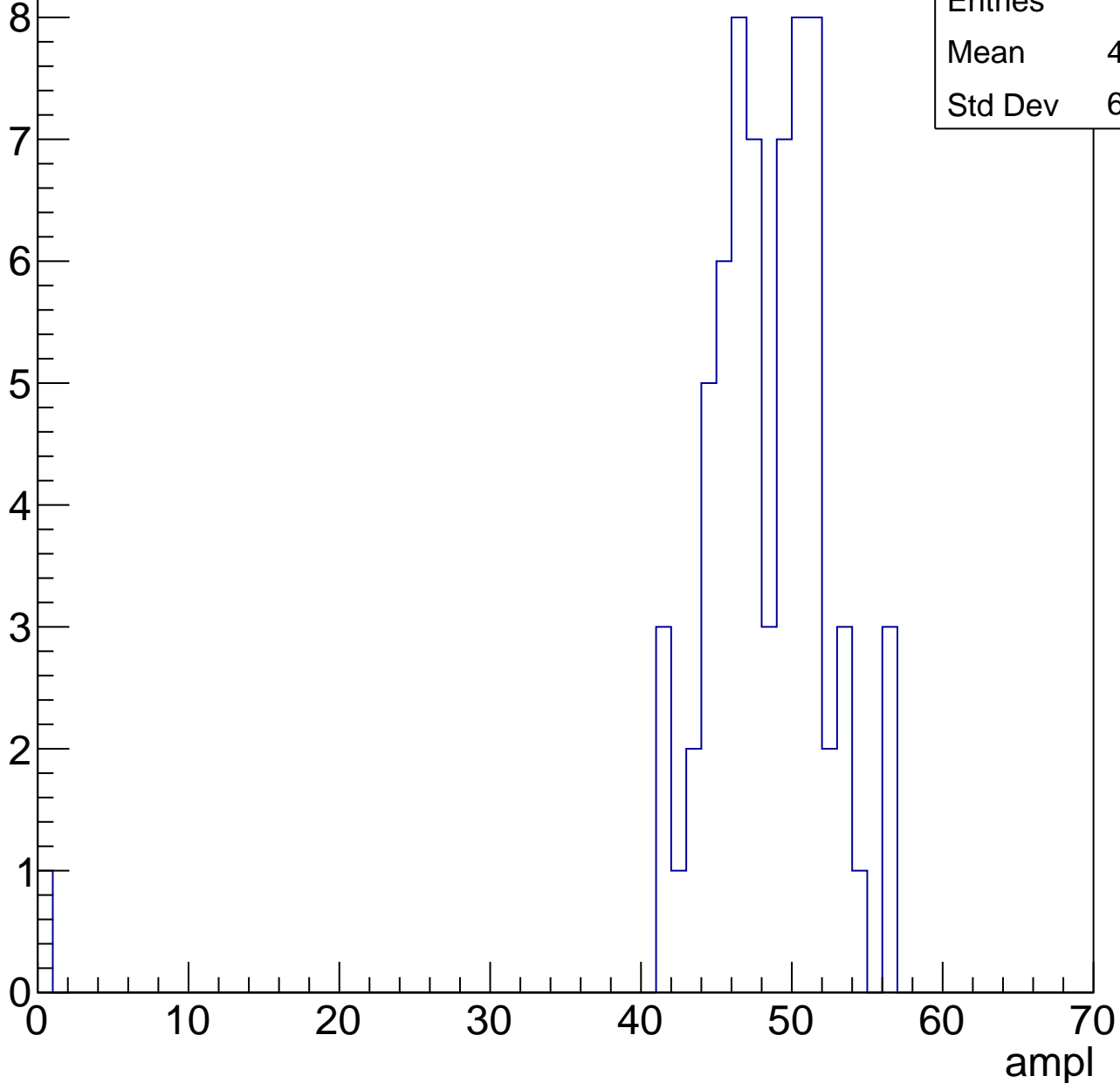


B1L103S, U23-ch127, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

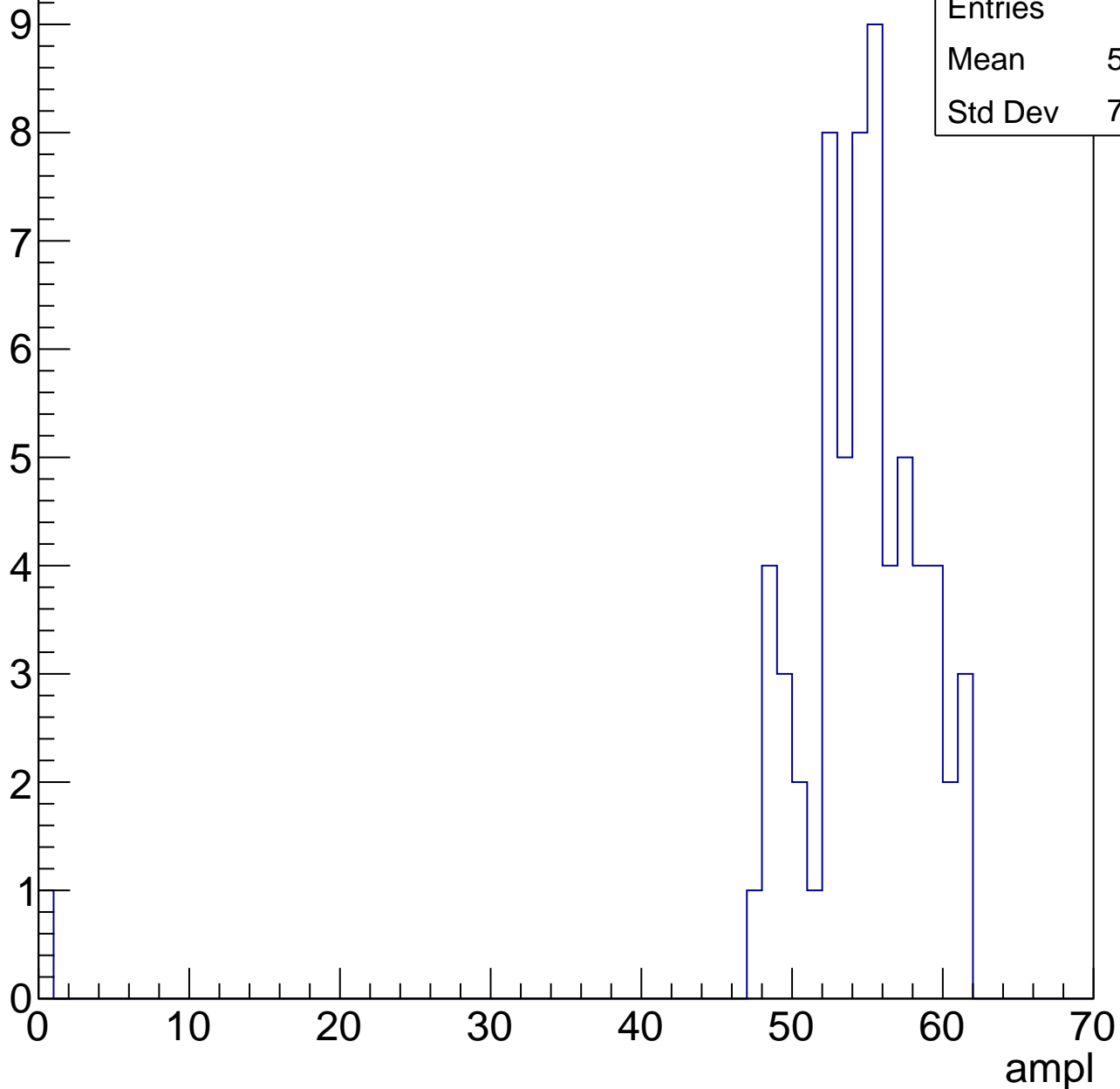
Entries	68
Mean	47.32
Std Dev	6.779



B1L103S, U23-ch127, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

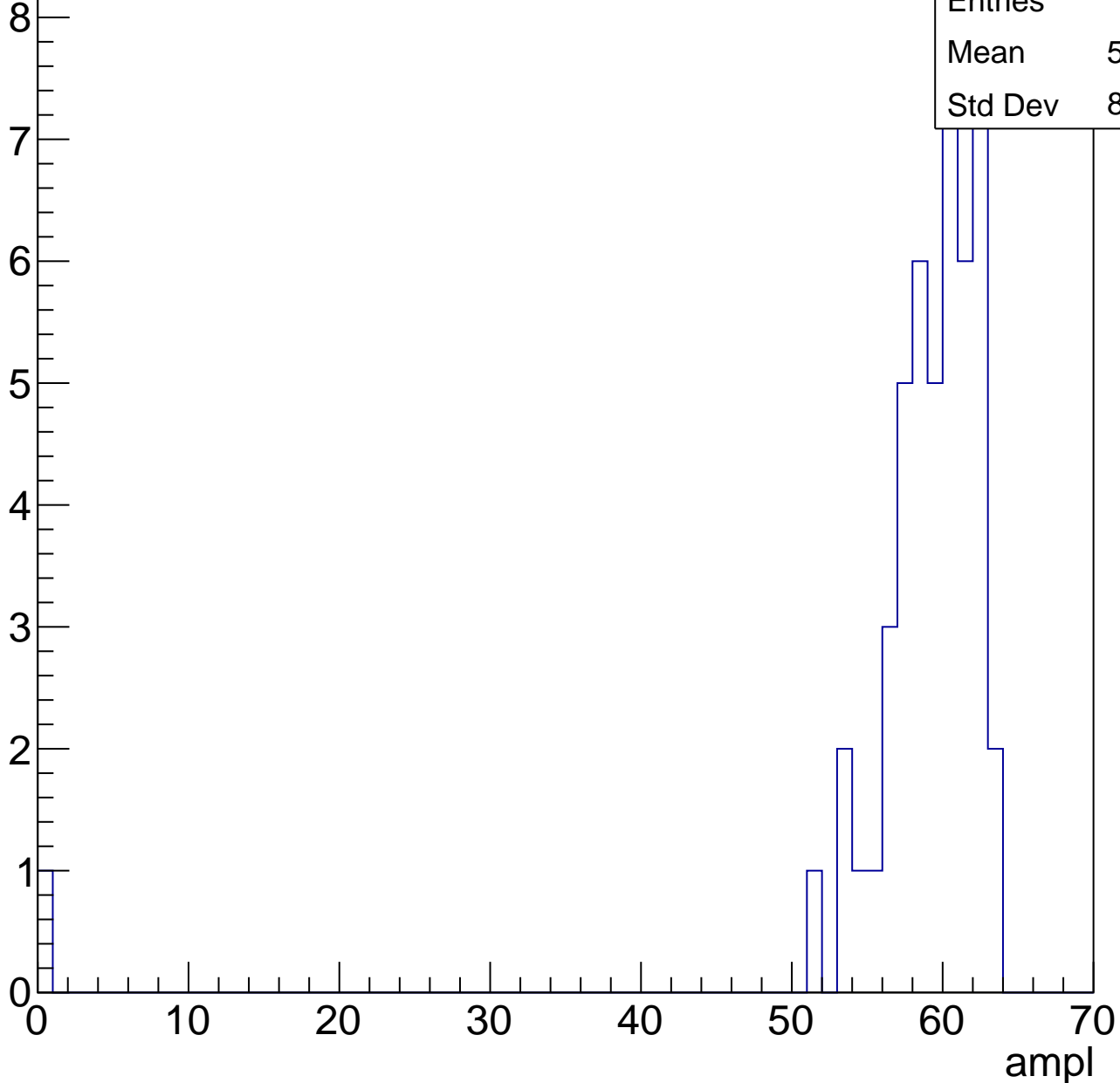


B1L103S, U23-ch127, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	49
Mean	57.76
Std Dev	8.773

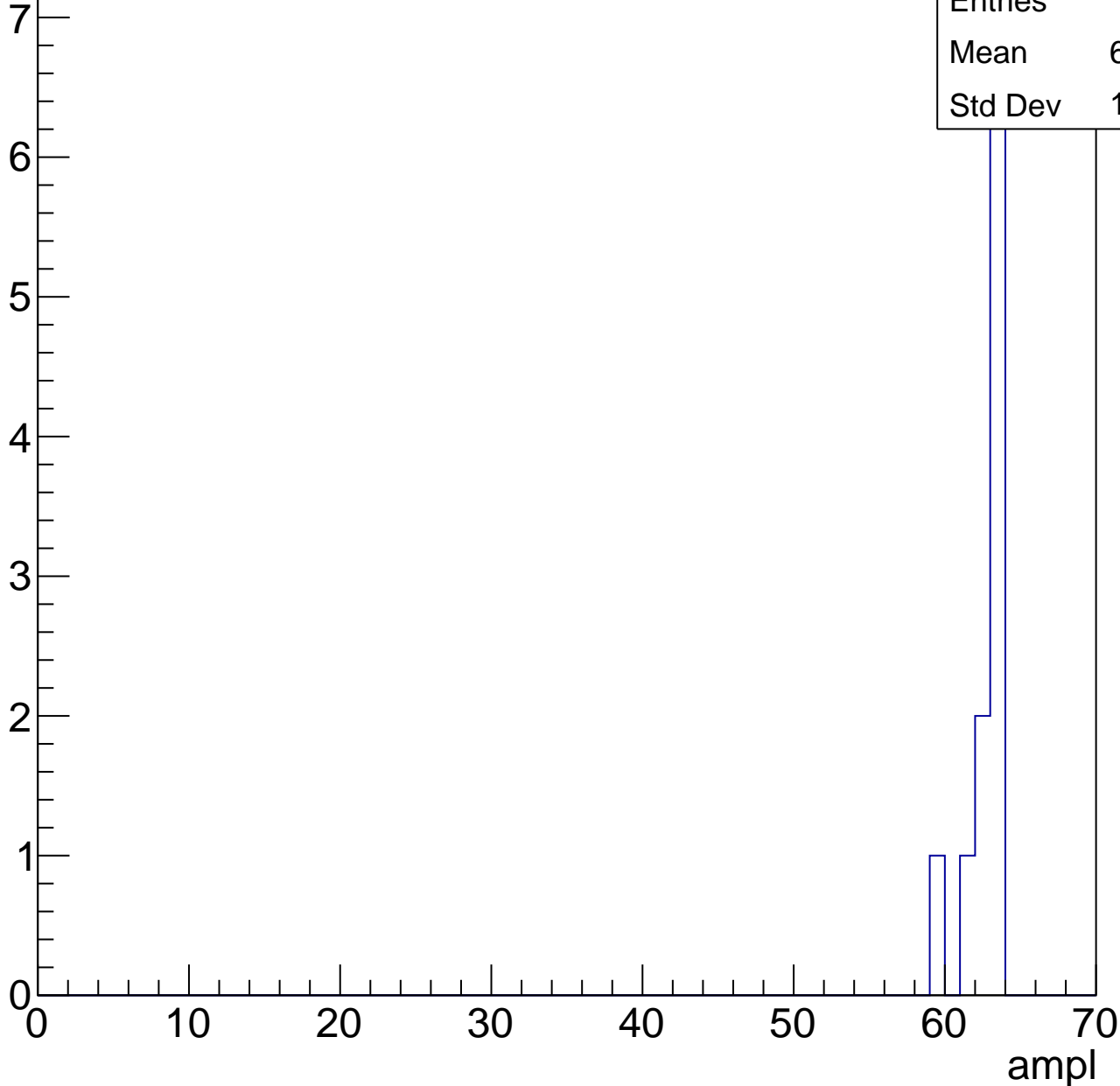


B1L103S, U23-ch127, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

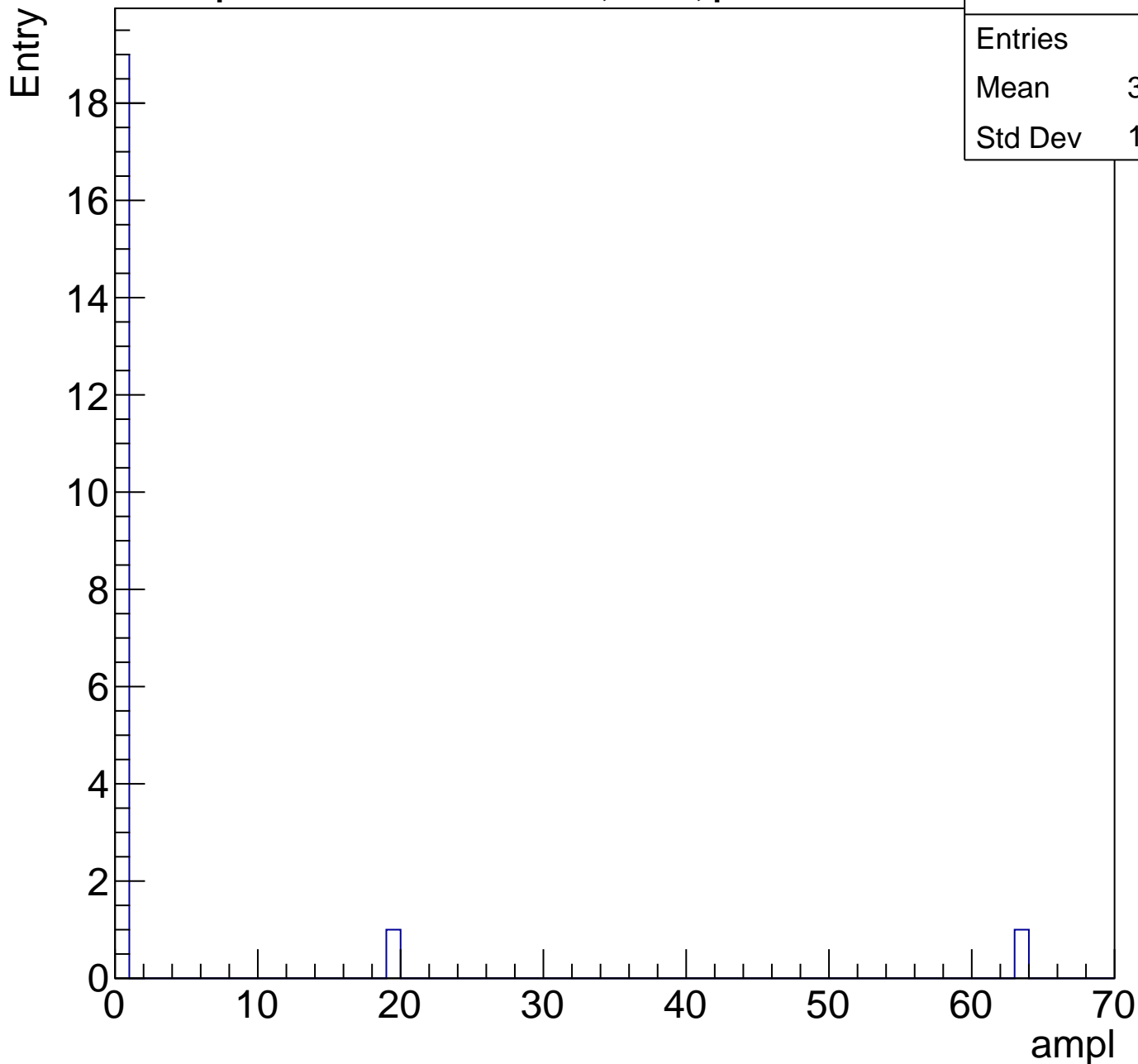
Entries	11
Mean	62.27
Std Dev	1.213



B1L103S, U23-ch127, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	21
Mean	3.905
Std Dev	13.82



B1L103S, U23-ch127, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	21
Mean	3.905
Std Dev	13.82

Entry

