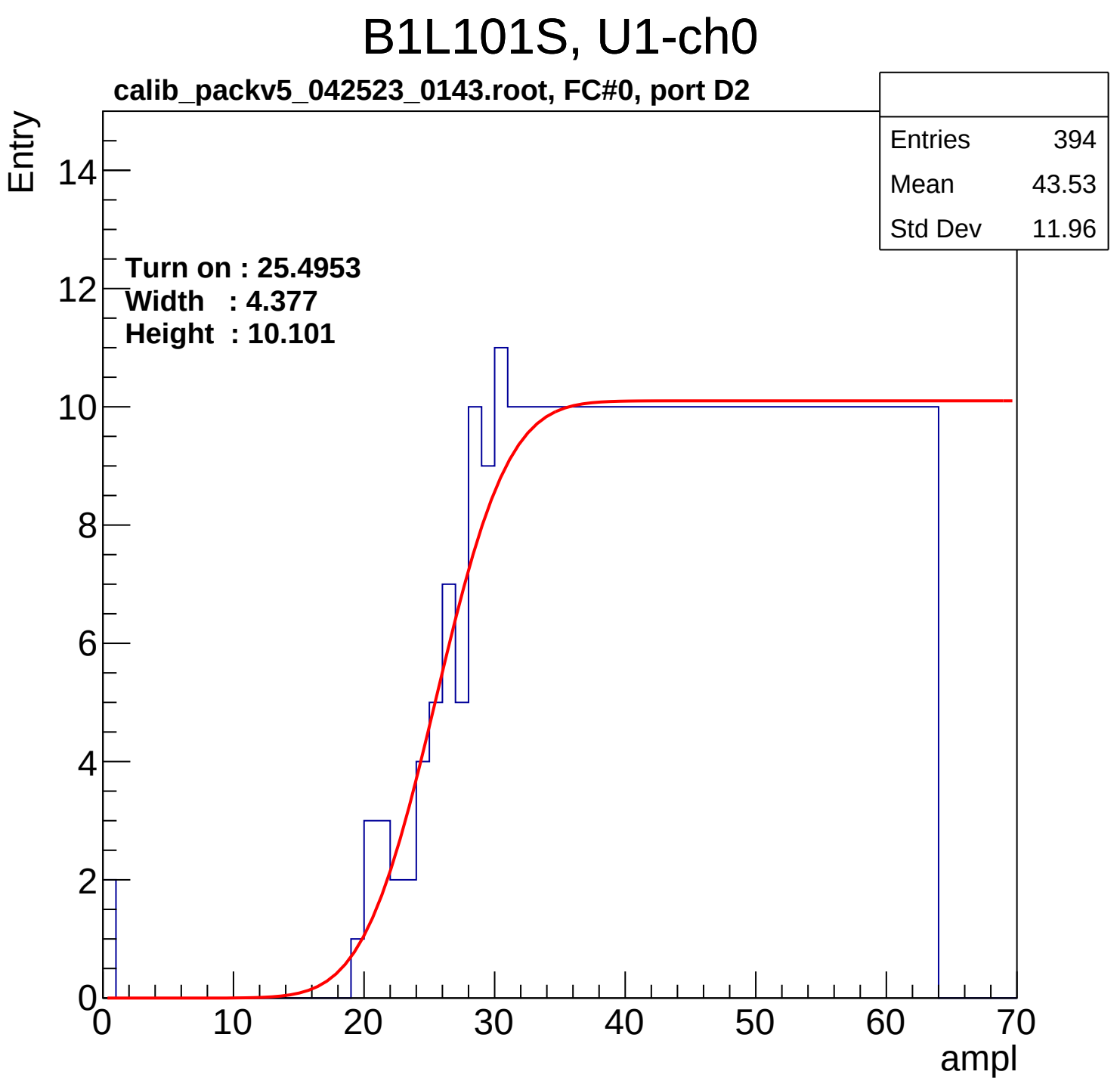
B1L101S, U1-ch0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 394
Mean 43.53
Std Dev 11.96
Turn on : 25.4953
Width : 4.377
Height : 10.101
Entry
ampl
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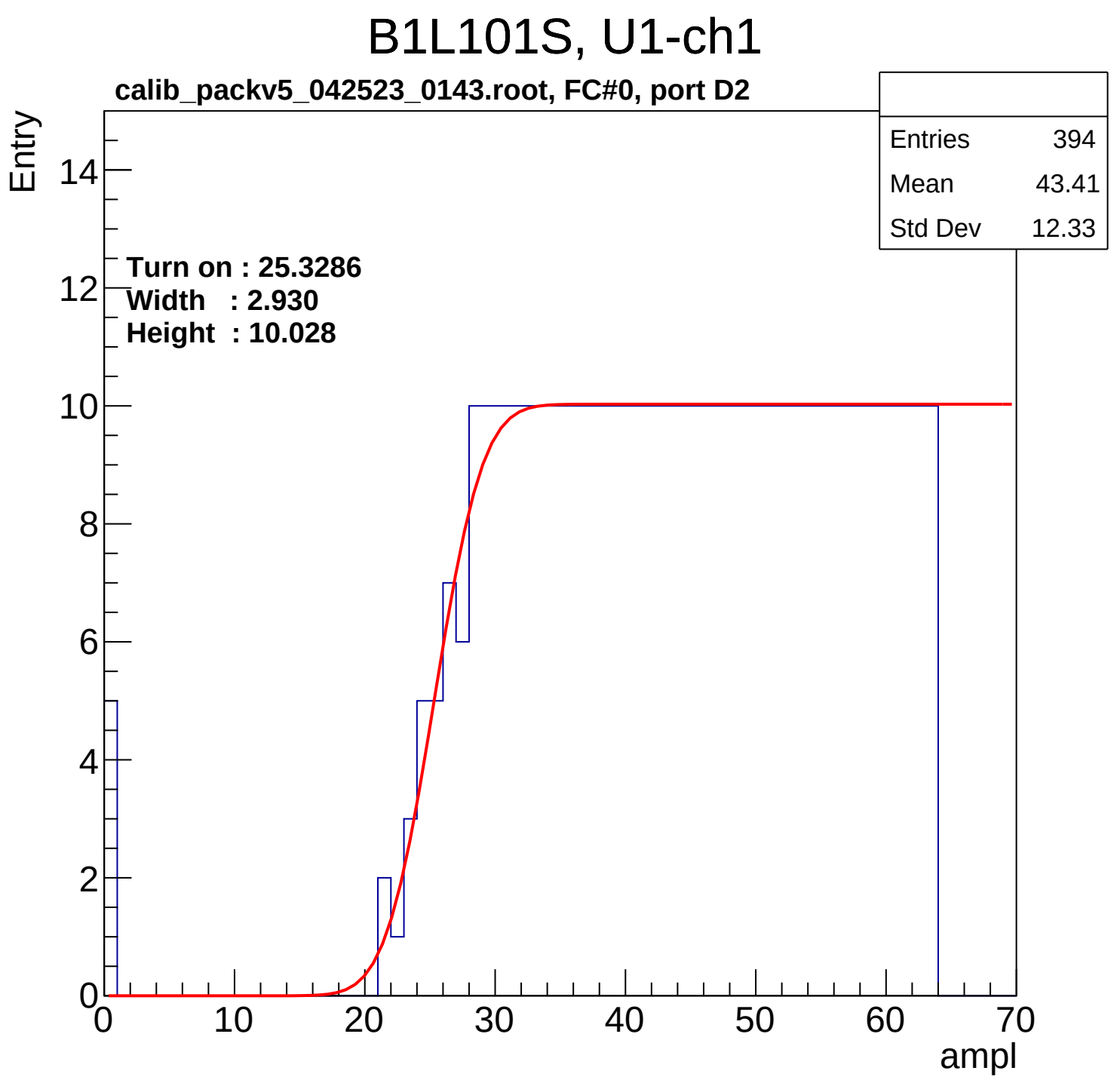
B1L101S, U1-ch1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 394
Mean 43.41
Std Dev 12.33
Turn on : 25.3286
Width : 2.930
Height : 10.028
Entry
ampl
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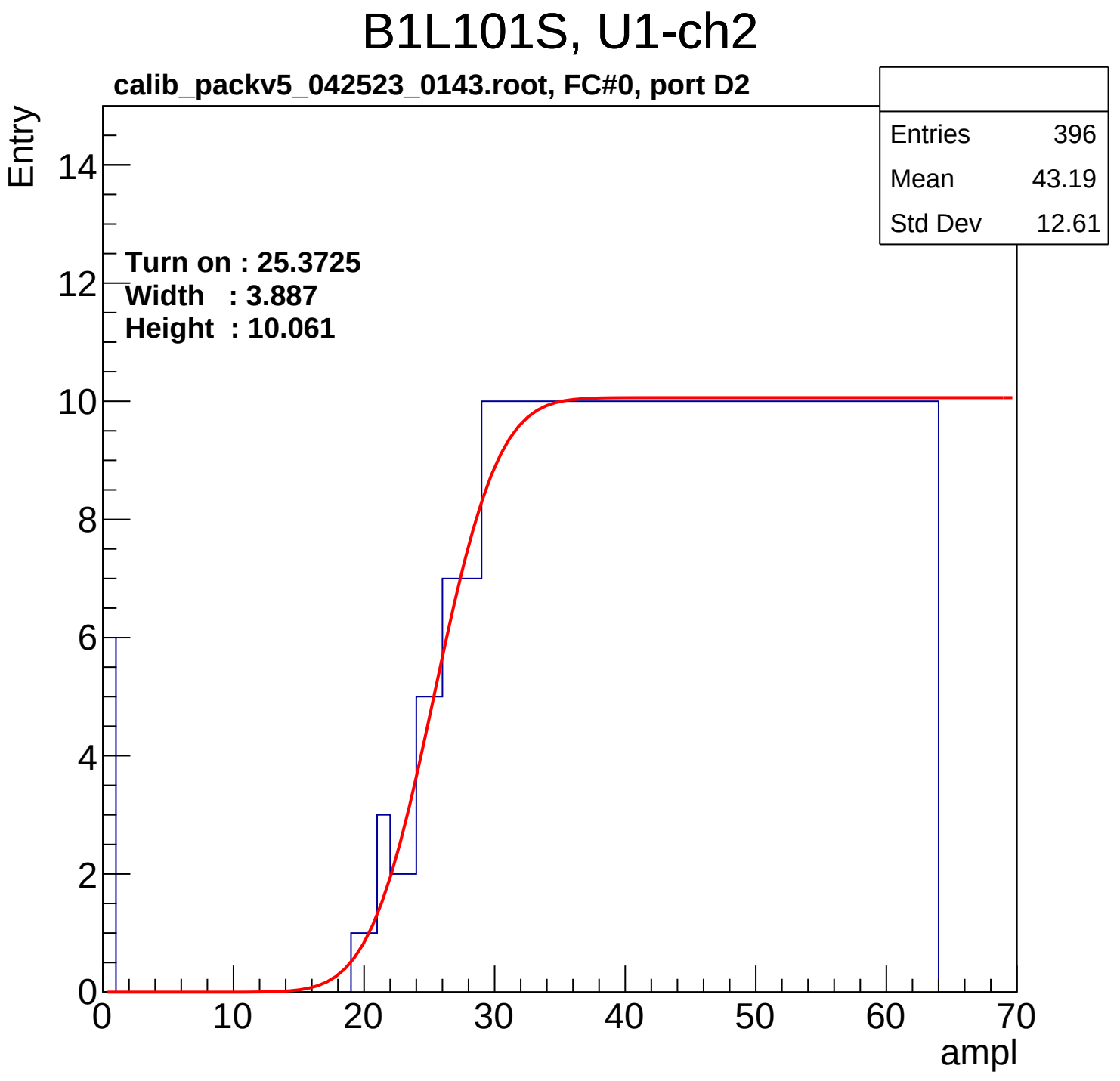
B1L101S, U1-ch2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 396
Mean 43.19
Std Dev 12.61
Turn on : 25.3725
Width : 3.887
Height : 10.061
Entry
ampl
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2
4
6
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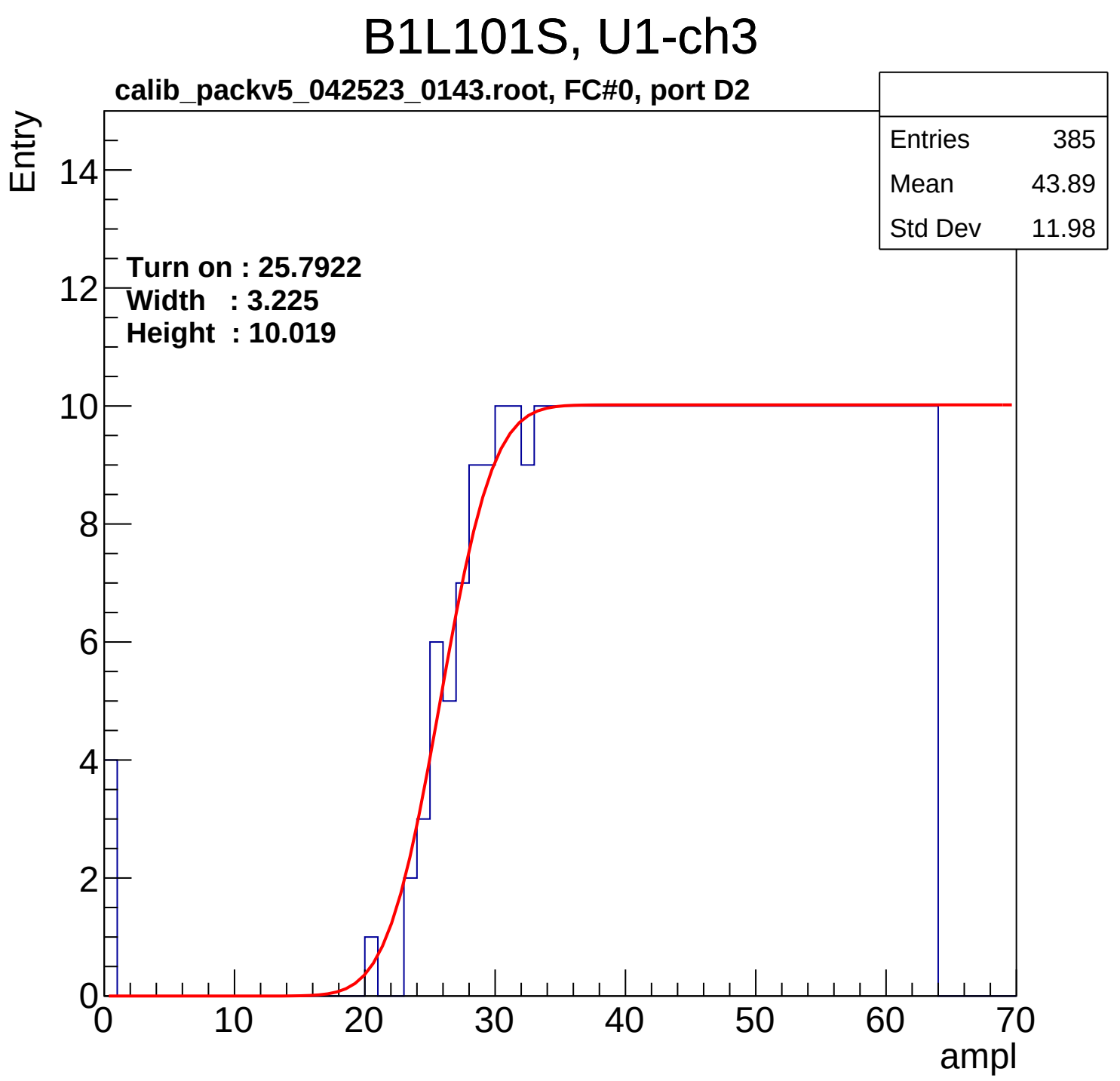
B1L101S, U1-ch3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 385
Mean 43.89
Std Dev 11.98
Turn on : 25.7922
Width : 3.225
Height : 10.019
Entry
ampl
0
2
4
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8
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0
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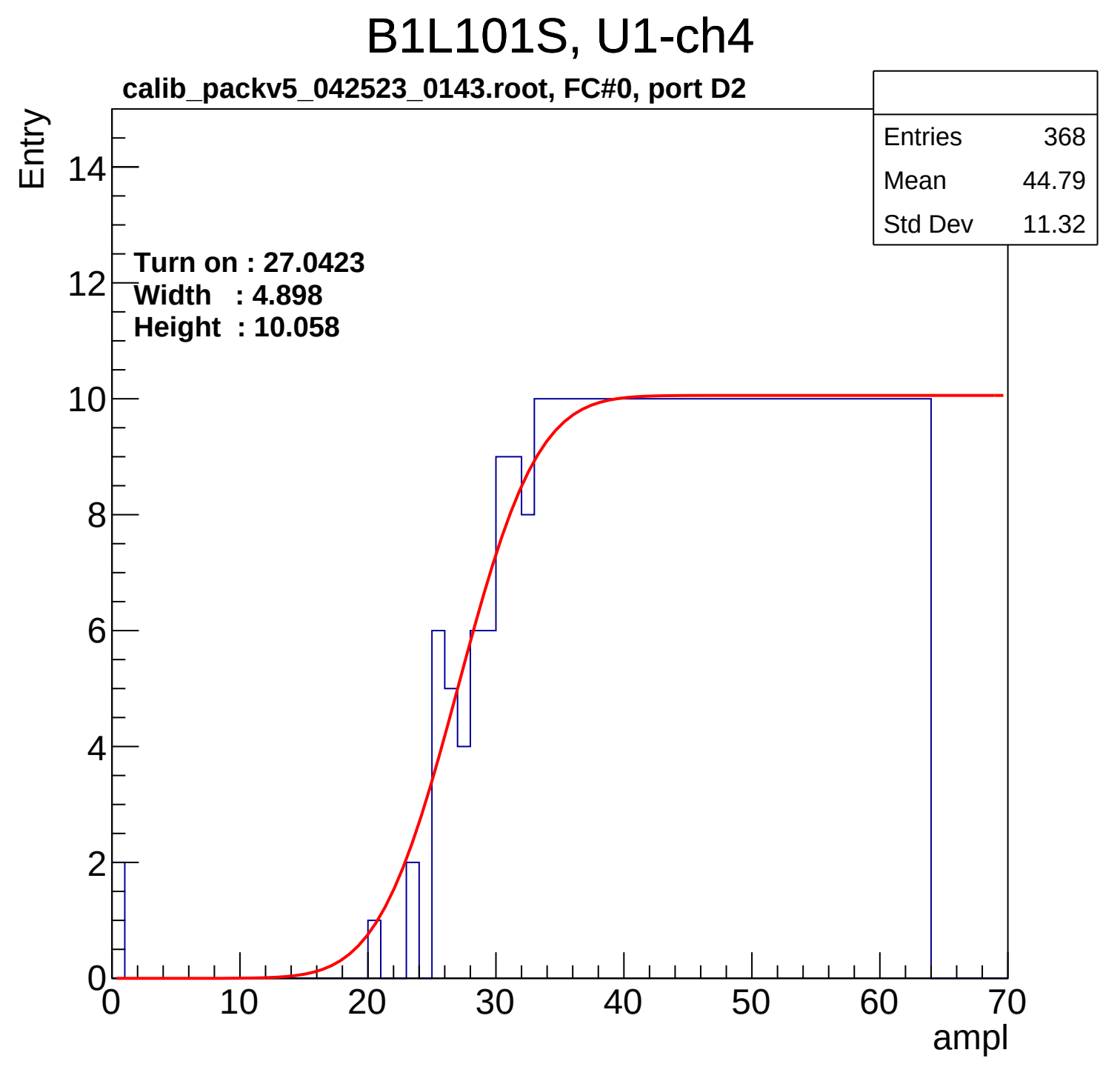
B1L101S, U1-ch4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 368
Mean 44.79
Std Dev 11.32
Turn on : 27.0423
Width : 4.898
Height : 10.058
Entry
ampl
0
2
4
6
8
10
12
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0
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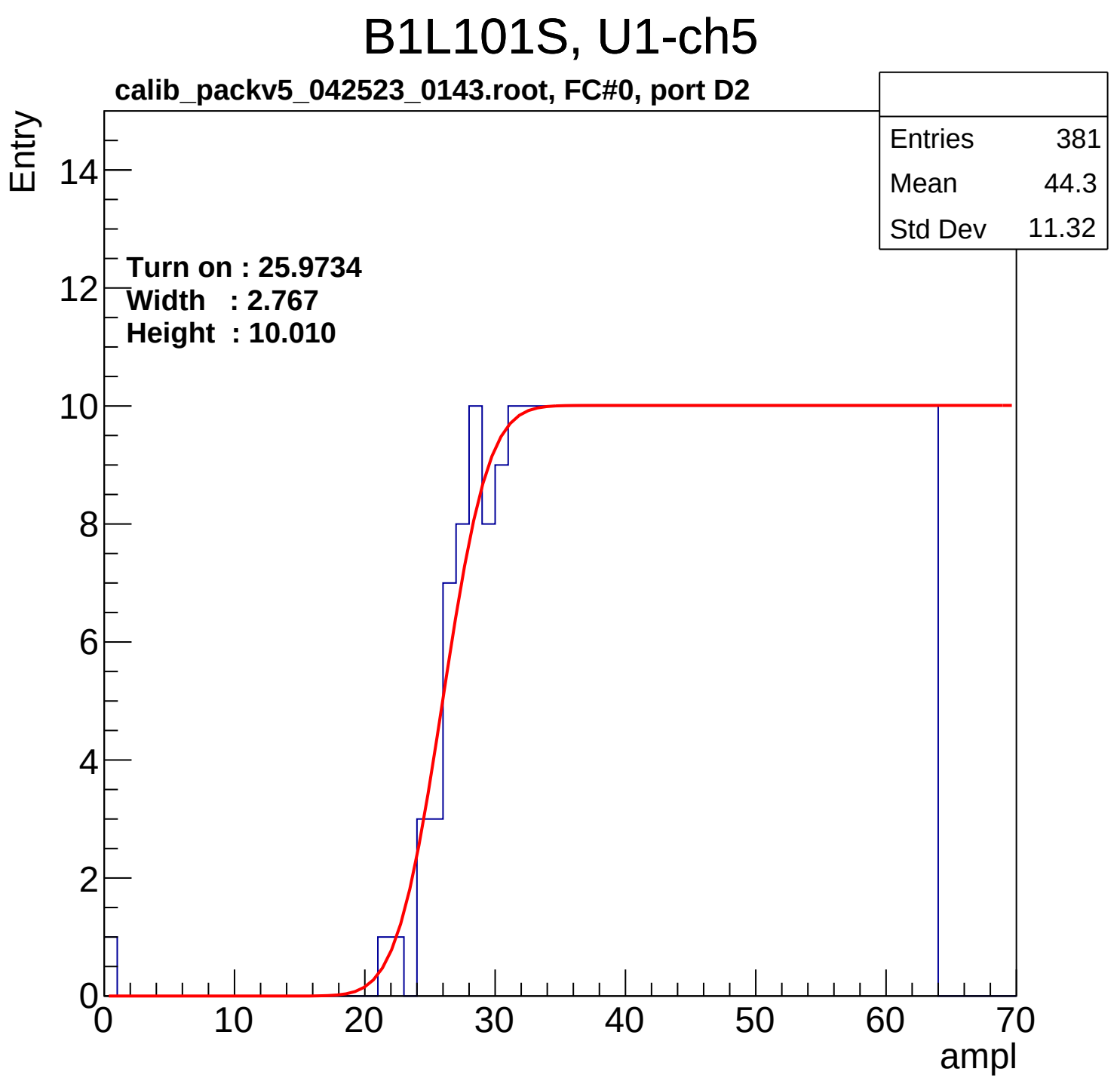
B1L101S, U1-ch5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 381
Mean 44.3
Std Dev 11.32
Turn on : 25.9734
Width : 2.767
Height : 10.010
Entry
ampl
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6
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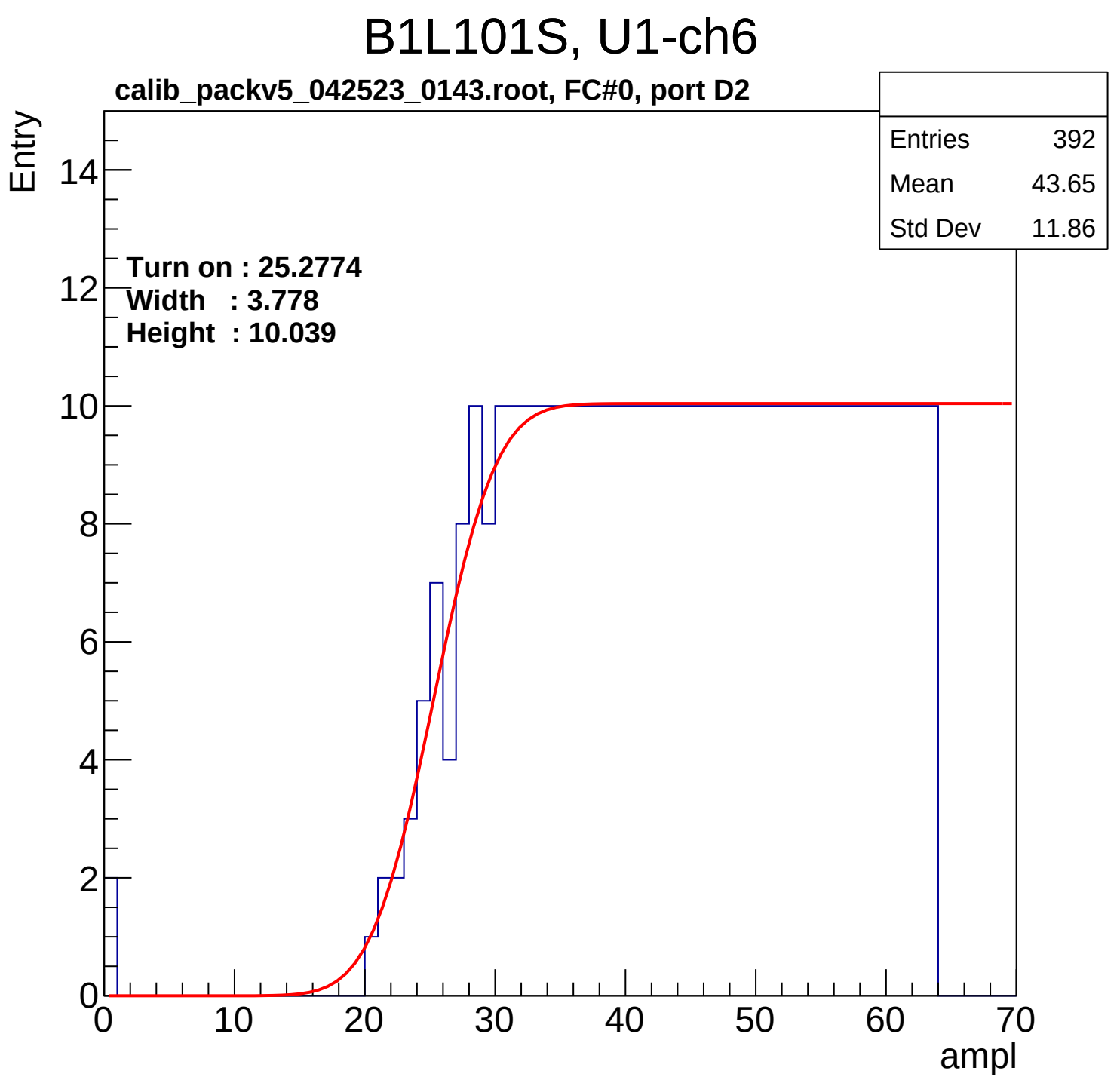
B1L101S, U1-ch6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 392
Mean 43.65
Std Dev 11.86
Turn on : 25.2774
Width : 3.778
Height : 10.039
Entry
ampl
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2
4
6
8
10
12
14
0
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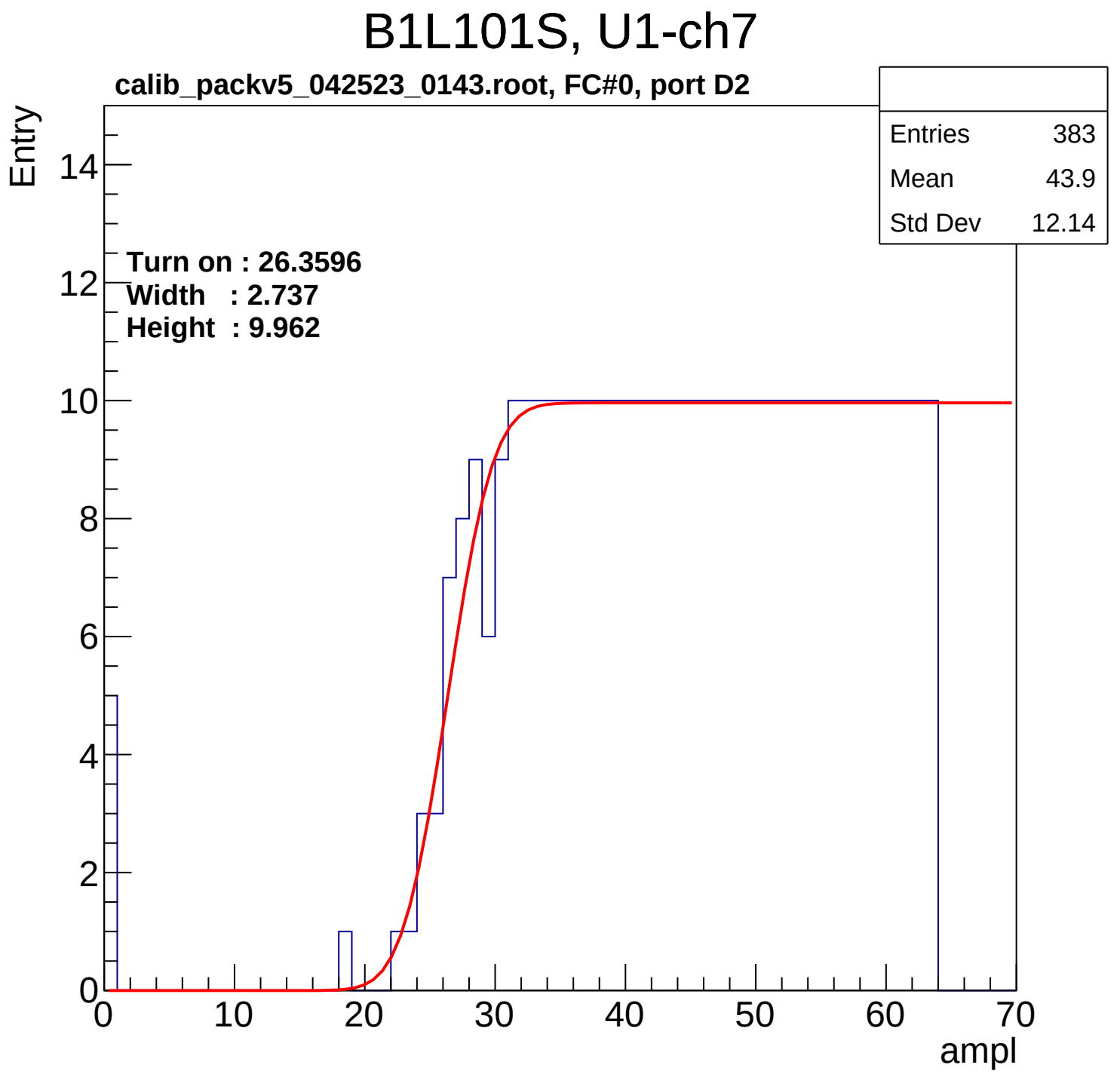
B1L101S, U1-ch7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 383
Mean 43.9
Std Dev 12.14
Turn on : 26.3596
Width : 2.737
Height : 9.962
Entry
ampl
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2
4
6
8
10
12
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0
10
20
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60
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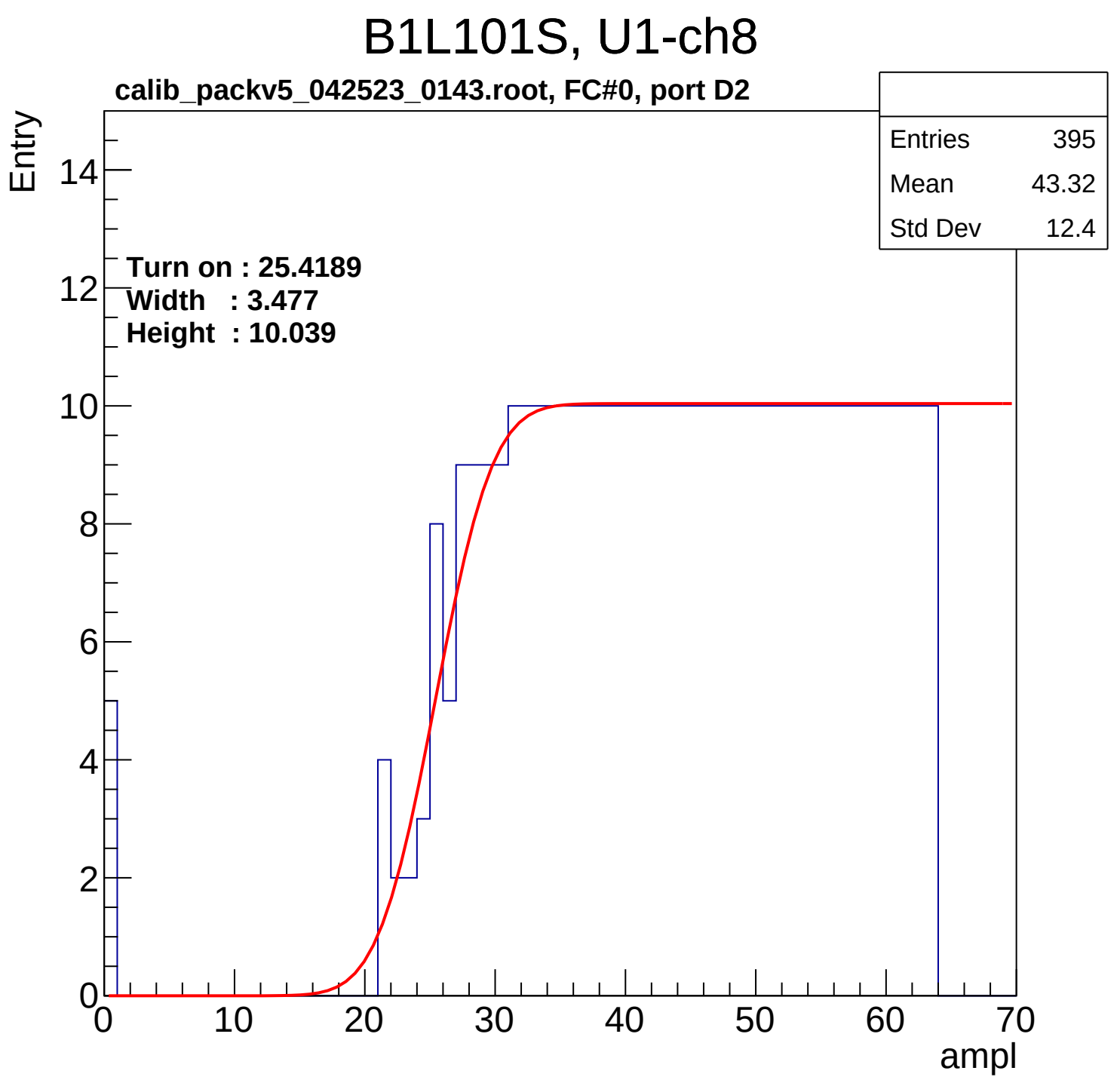
B1L101S, U1-ch8
calib_packv5_042523_0143.root, FC#0, port D2
Entries 395
Mean 43.32
Std Dev 12.4
Turn on : 25.4189
Width : 3.477
Height : 10.039
Entry
ampl
0
2
4
6
8
10
12
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0
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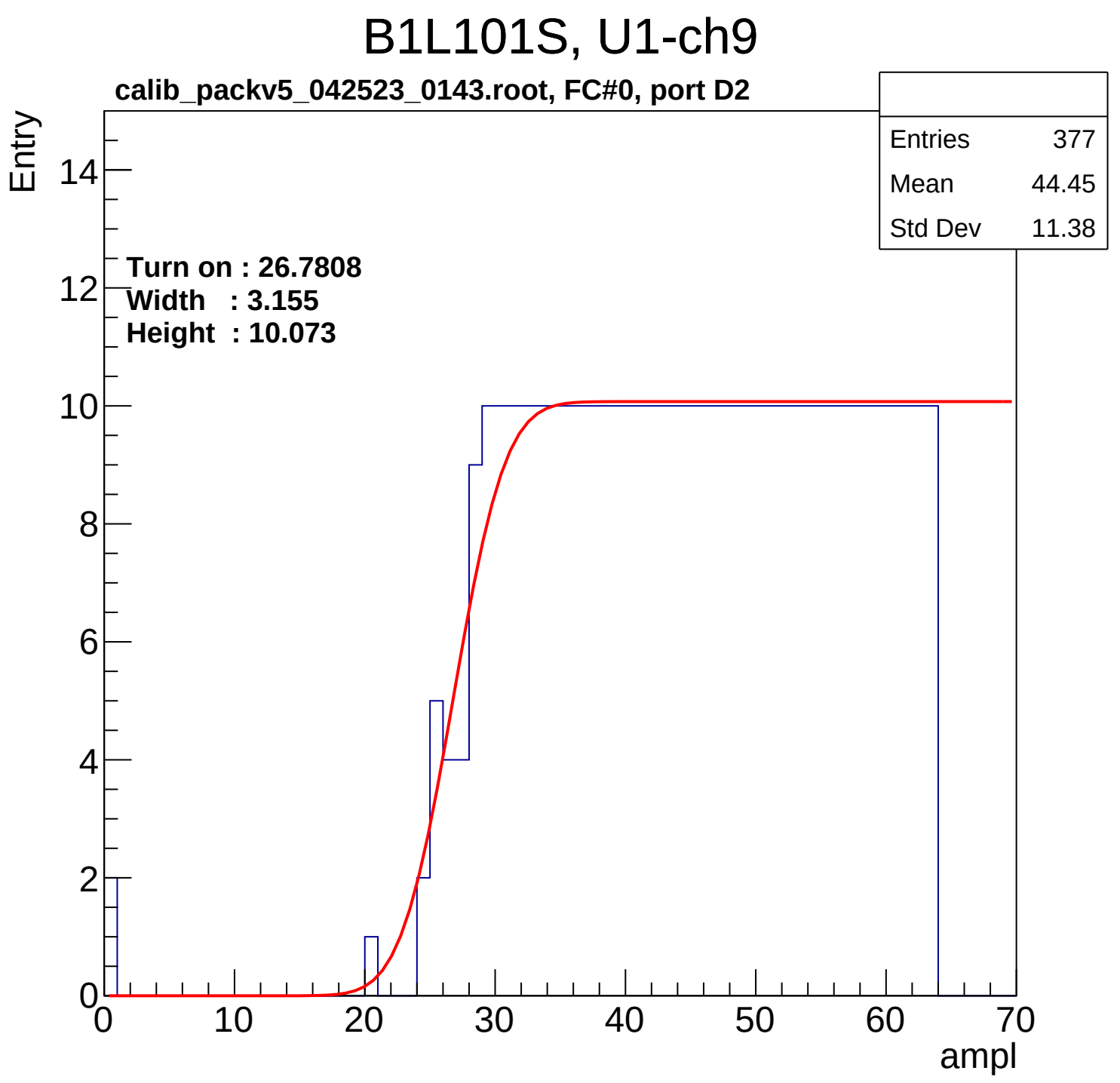
B1L101S, U1-ch9
calib_packv5_042523_0143.root, FC#0, port D2
Entries 377
Mean 44.45
Std Dev 11.38
Turn on : 26.7808
Width : 3.155
Height : 10.073
Entry
ampl
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60
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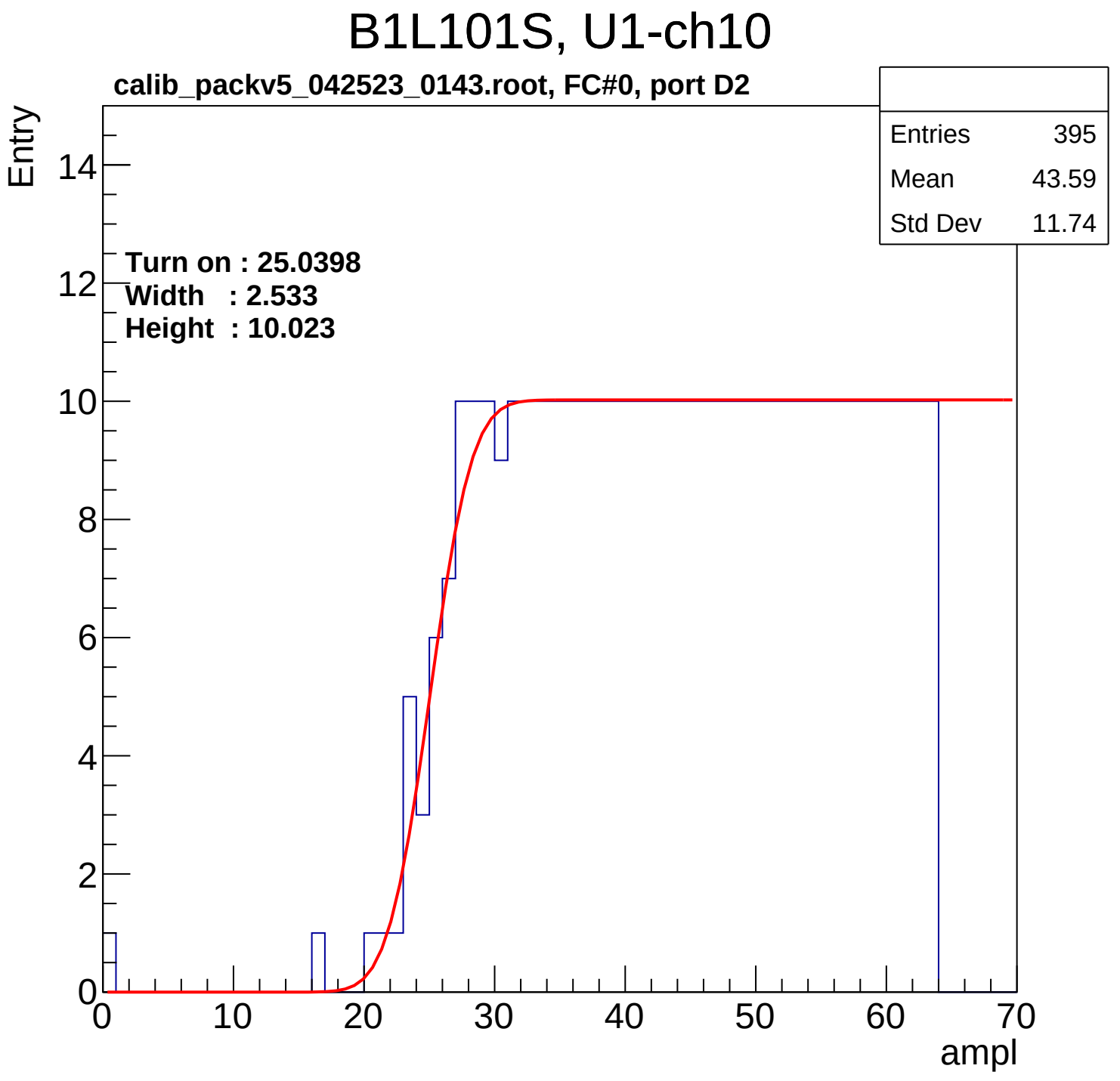
B1L101S, U1-ch10
calib_packv5_042523_0143.root, FC#0, port D2
Entries 395
Mean 43.59
Std Dev 11.74
Turn on : 25.0398
Width : 2.533
Height : 10.023
Entry
ampl
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6
8
10
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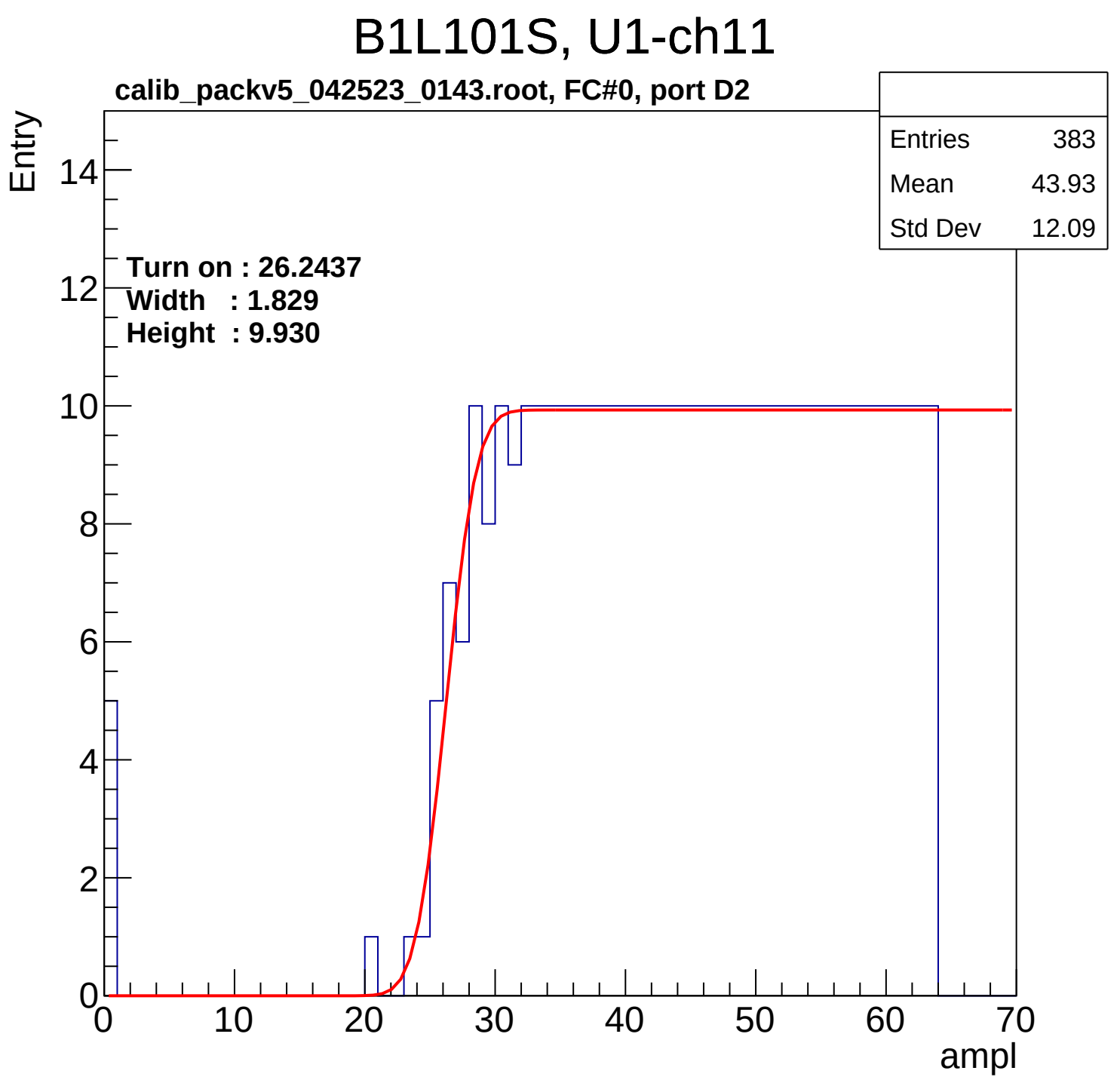
B1L101S, U1-ch11
calib_packv5_042523_0143.root, FC#0, port D2
Entries 383
Mean 43.93
Std Dev 12.09
Turn on : 26.2437
Width : 1.829
Height : 9.930
Entry
ampl
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2
4
6
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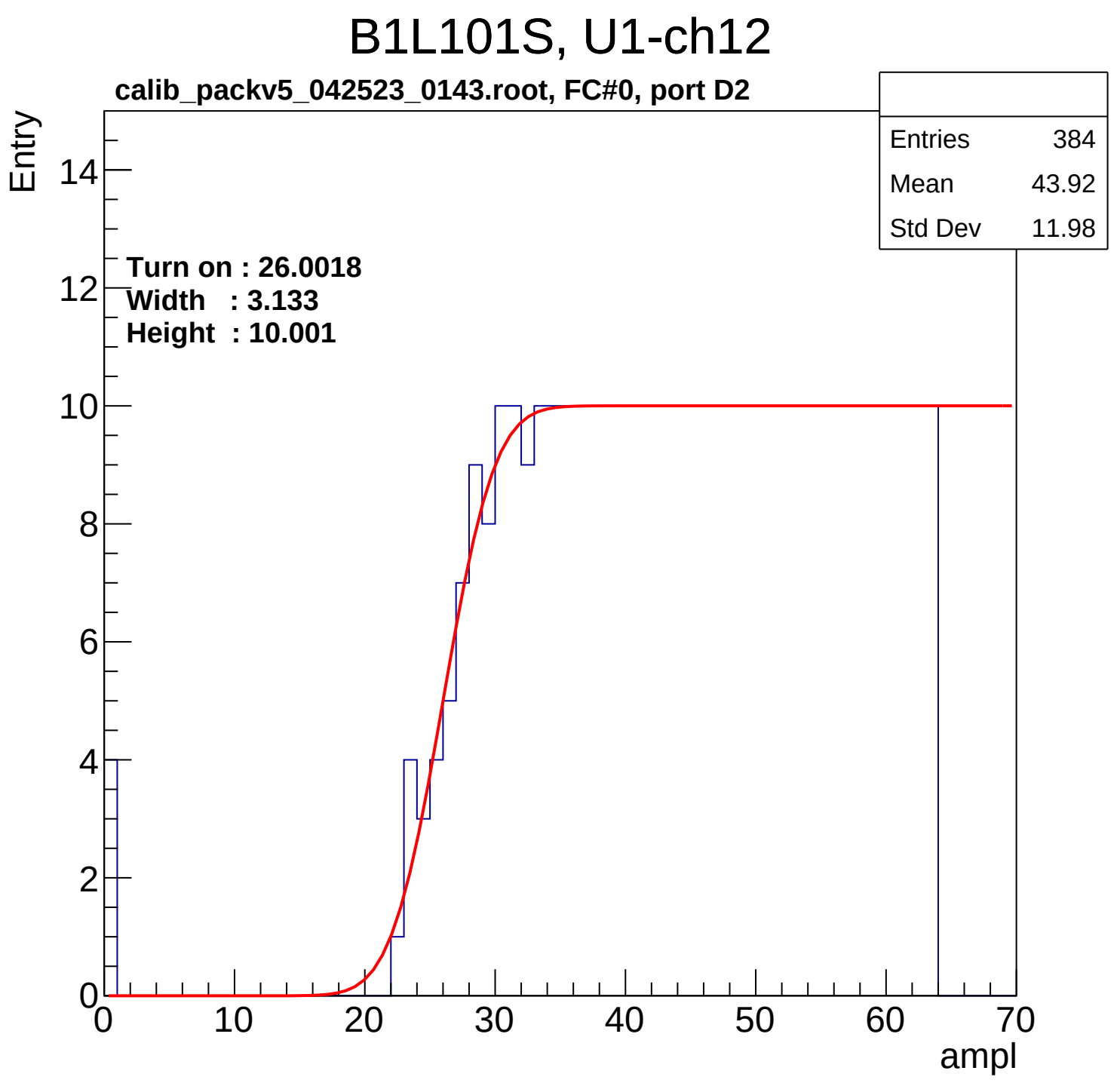
B1L101S, U1-ch12
calib_packv5_042523_0143.root, FC#0, port D2
Entries 384
Mean 43.92
Std Dev 11.98
Turn on : 26.0018
Width : 3.133
Height : 10.001
Entry
ampl
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2
4
6
8
10
12
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0
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20
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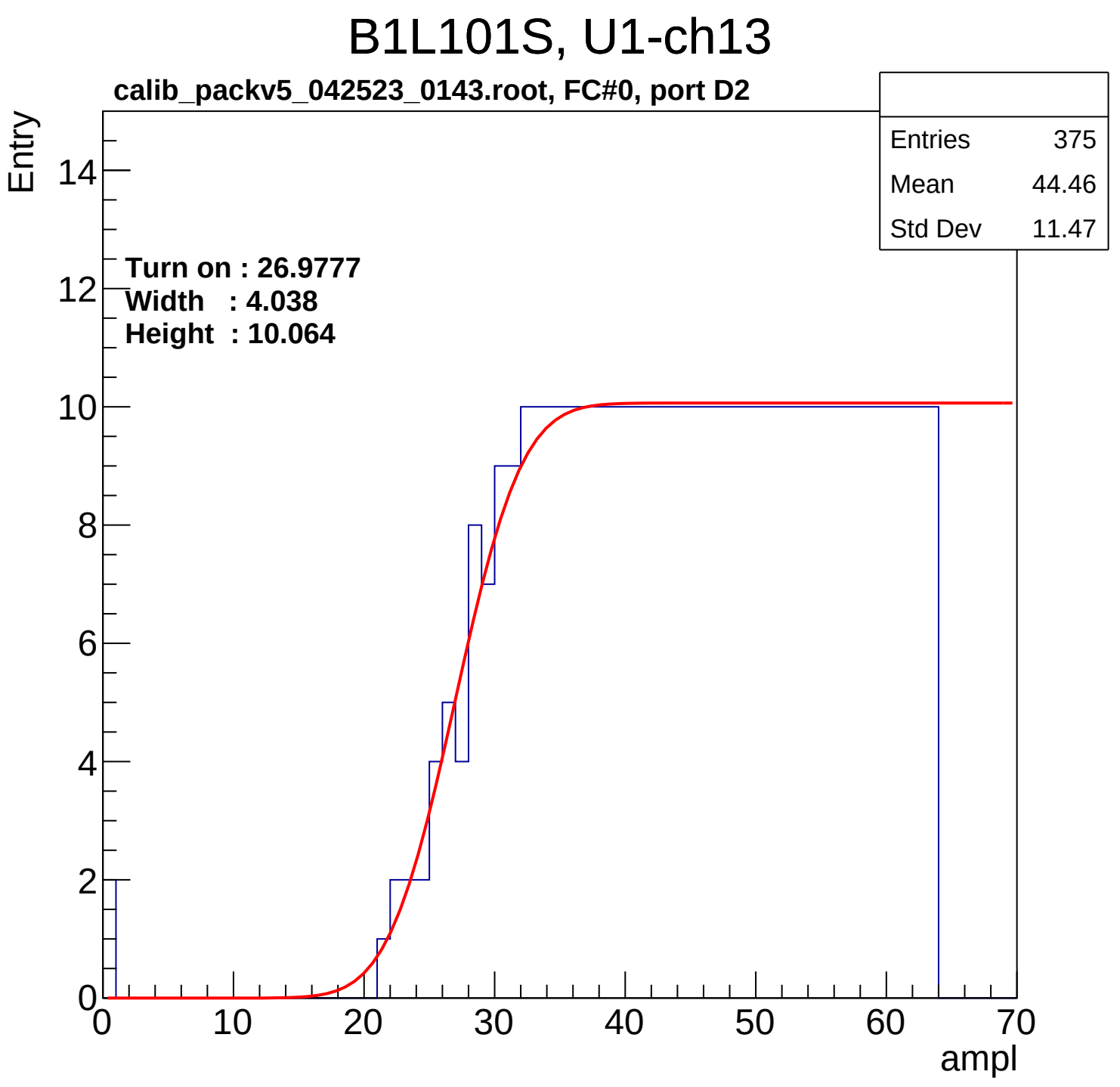
B1L101S, U1-ch13
calib_packv5_042523_0143.root, FC#0, port D2
Entries 375
Mean 44.46
Std Dev 11.47
Turn on : 26.9777
Width : 4.038
Height : 10.064
Entry
ampl
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2
4
6
8
10
12
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0
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20
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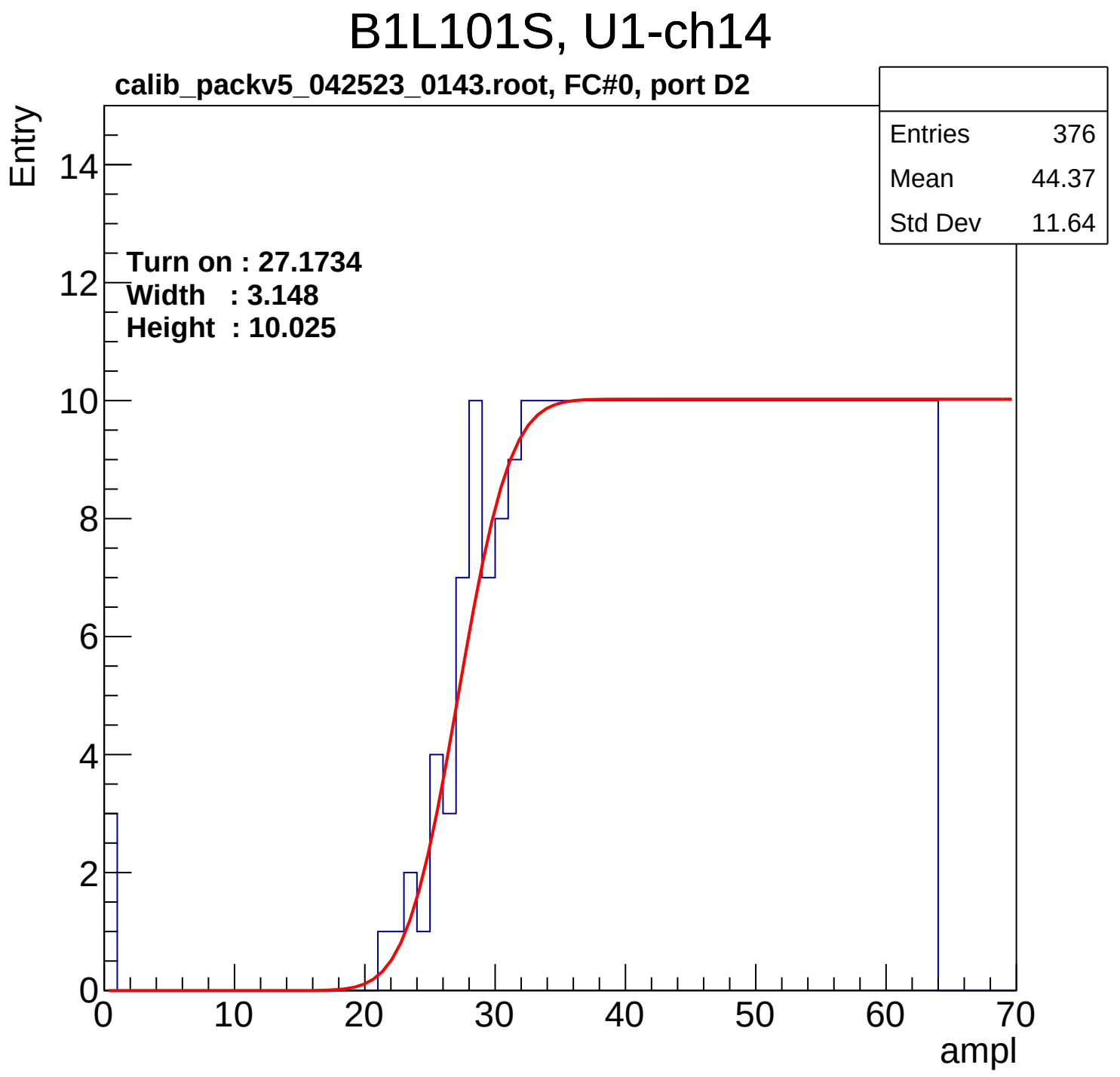
B1L101S, U1-ch14
calib_packv5_042523_0143.root, FC#0, port D2
Entries 376
Mean 44.37
Std Dev 11.64
Turn on : 27.1734
Width : 3.148
Height : 10.025
Entry
ampl
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6
8
10
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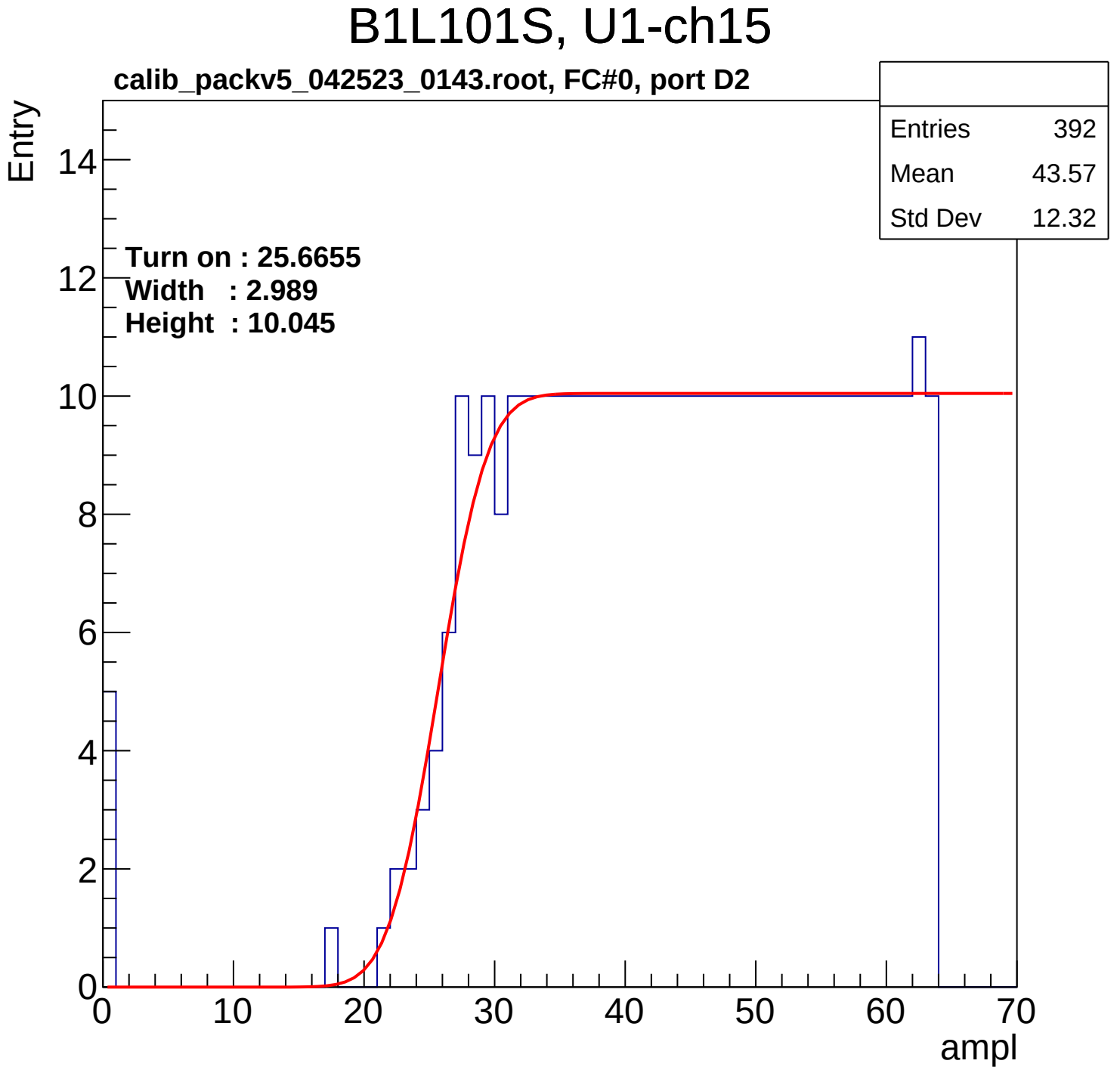
B1L101S, U1-ch15
calib_packv5_042523_0143.root, FC#0, port D2
Entries 392
Mean 43.57
Std Dev 12.32
Turn on : 25.6655
Width : 2.989
Height : 10.045
Entry
ampl
0
2
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8
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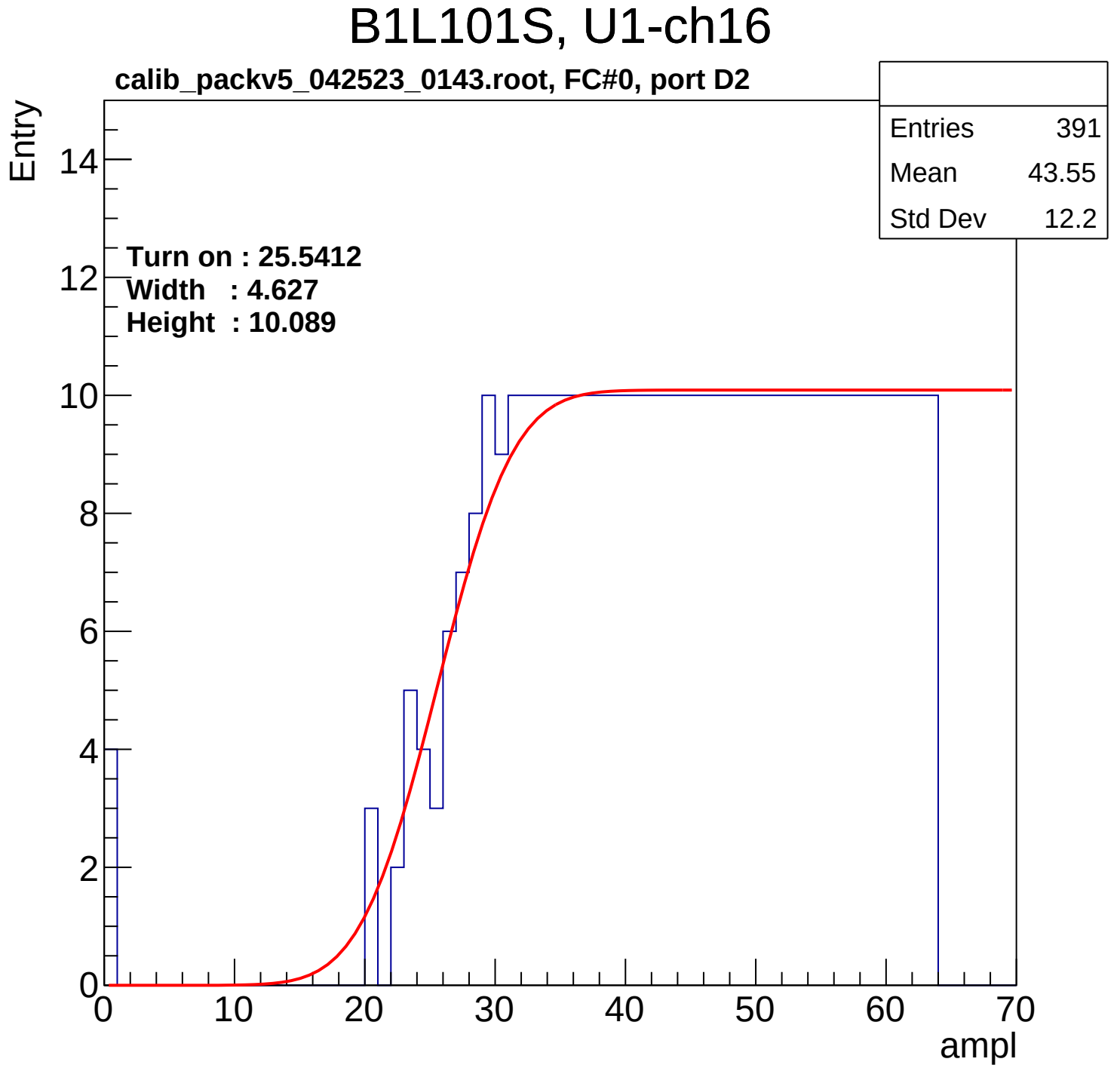
B1L101S, U1-ch16
calib_packv5_042523_0143.root, FC#0, port D2
Entries 391
Mean 43.55
Std Dev 12.2
Turn on : 25.5412
Width : 4.627
Height : 10.089
Entry
ampl
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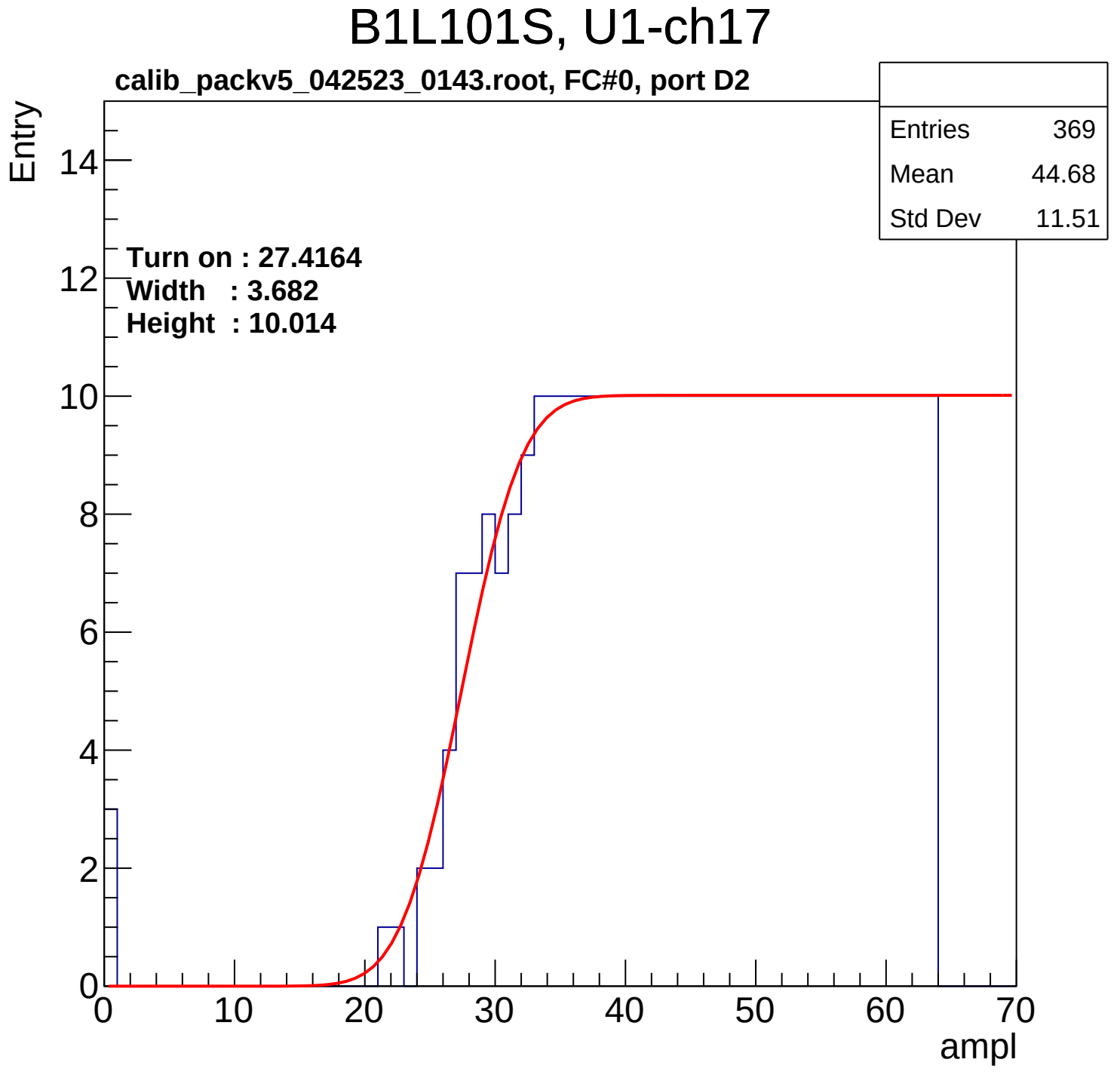
B1L101S, U1-ch17
calib_packv5_042523_0143.root, FC#0, port D2
Entries 369
Mean 44.68
Std Dev 11.51
Turn on : 27.4164
Width : 3.682
Height : 10.014
Entry
ampl
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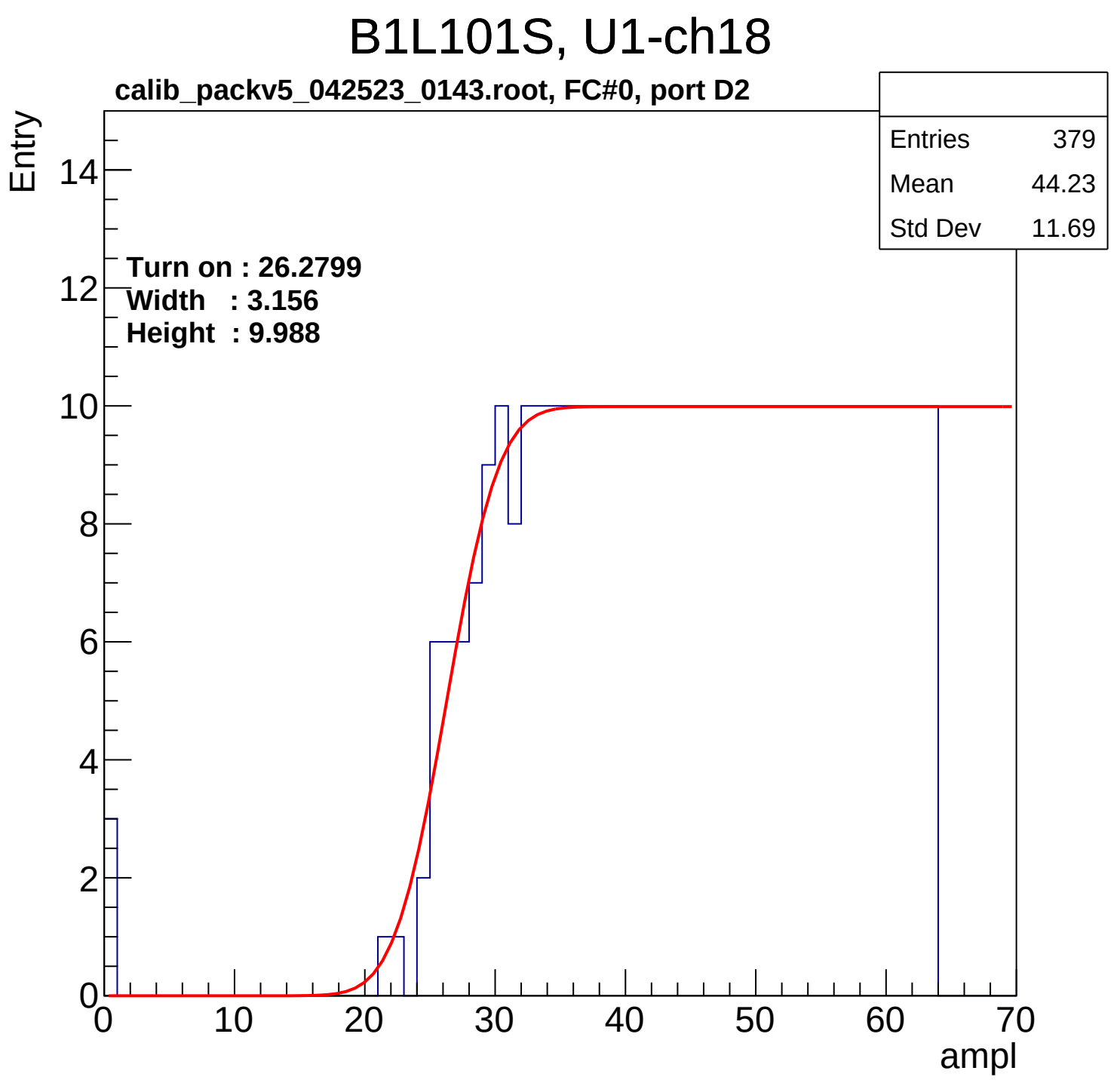
B1L101S, U1-ch18
calib_packv5_042523_0143.root, FC#0, port D2
Entries 379
Mean 44.23
Std Dev 11.69
Turn on : 26.2799
Width : 3.156
Height : 9.988
Entry
ampl
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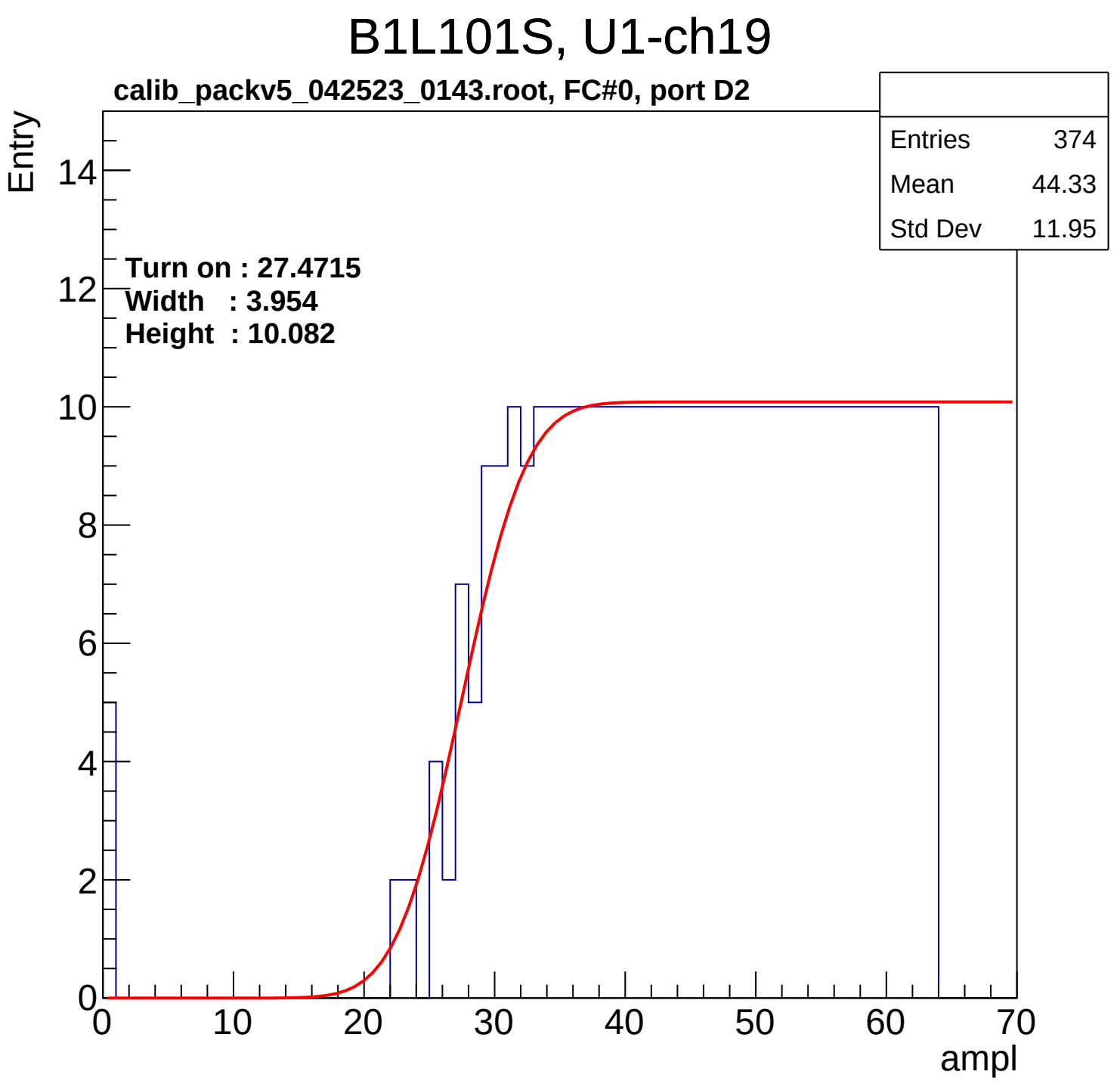
B1L101S, U1-ch19
calib_packv5_042523_0143.root, FC#0, port D2
Entries 374
Mean 44.33
Std Dev 11.95
Turn on : 27.4715
Width : 3.954
Height : 10.082
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ampl
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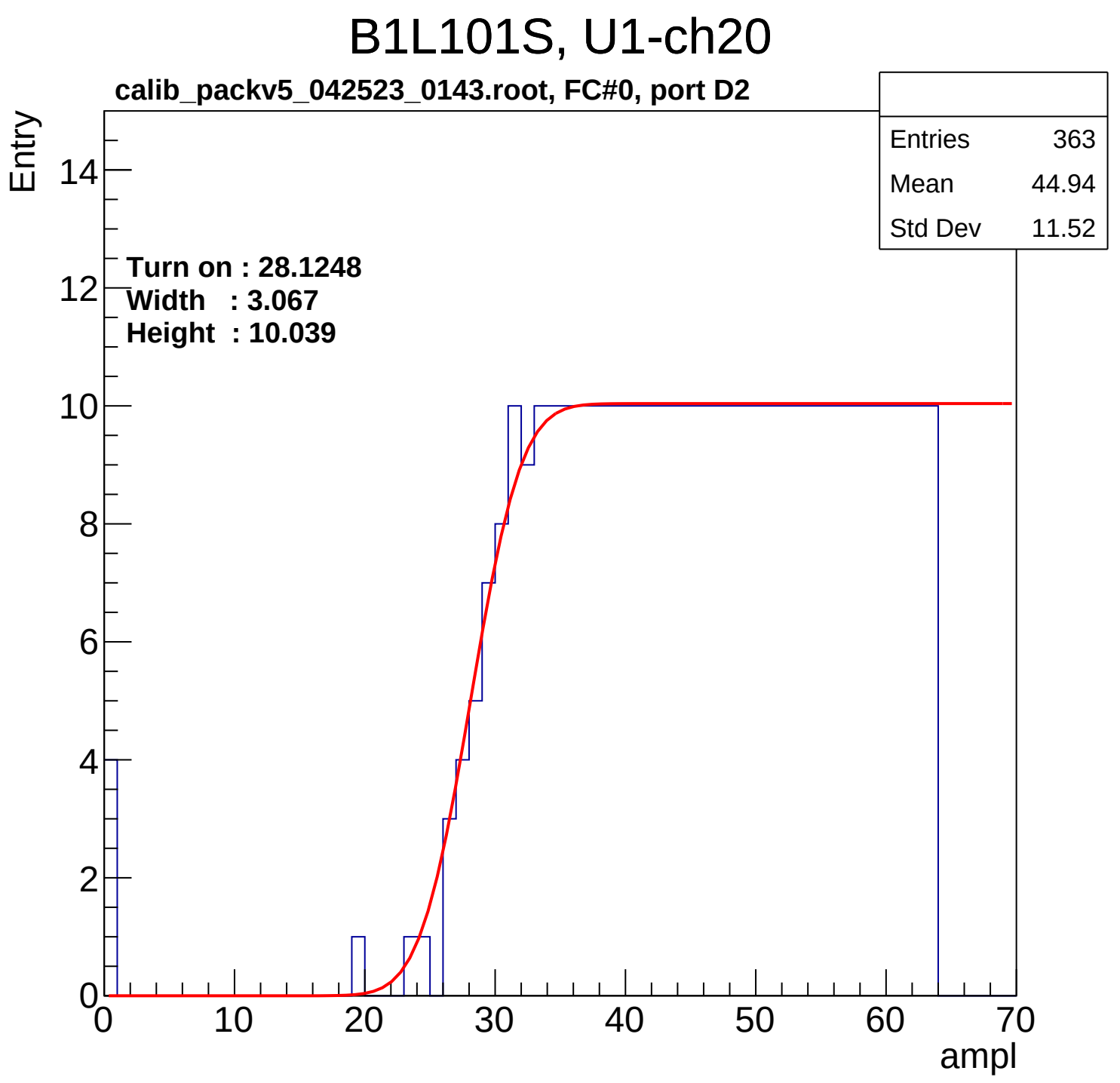
B1L101S, U1-ch20
calib_packv5_042523_0143.root, FC#0, port D2
Entries 363
Mean 44.94
Std Dev 11.52
Turn on : 28.1248
Width : 3.067
Height : 10.039
Entry
ampl
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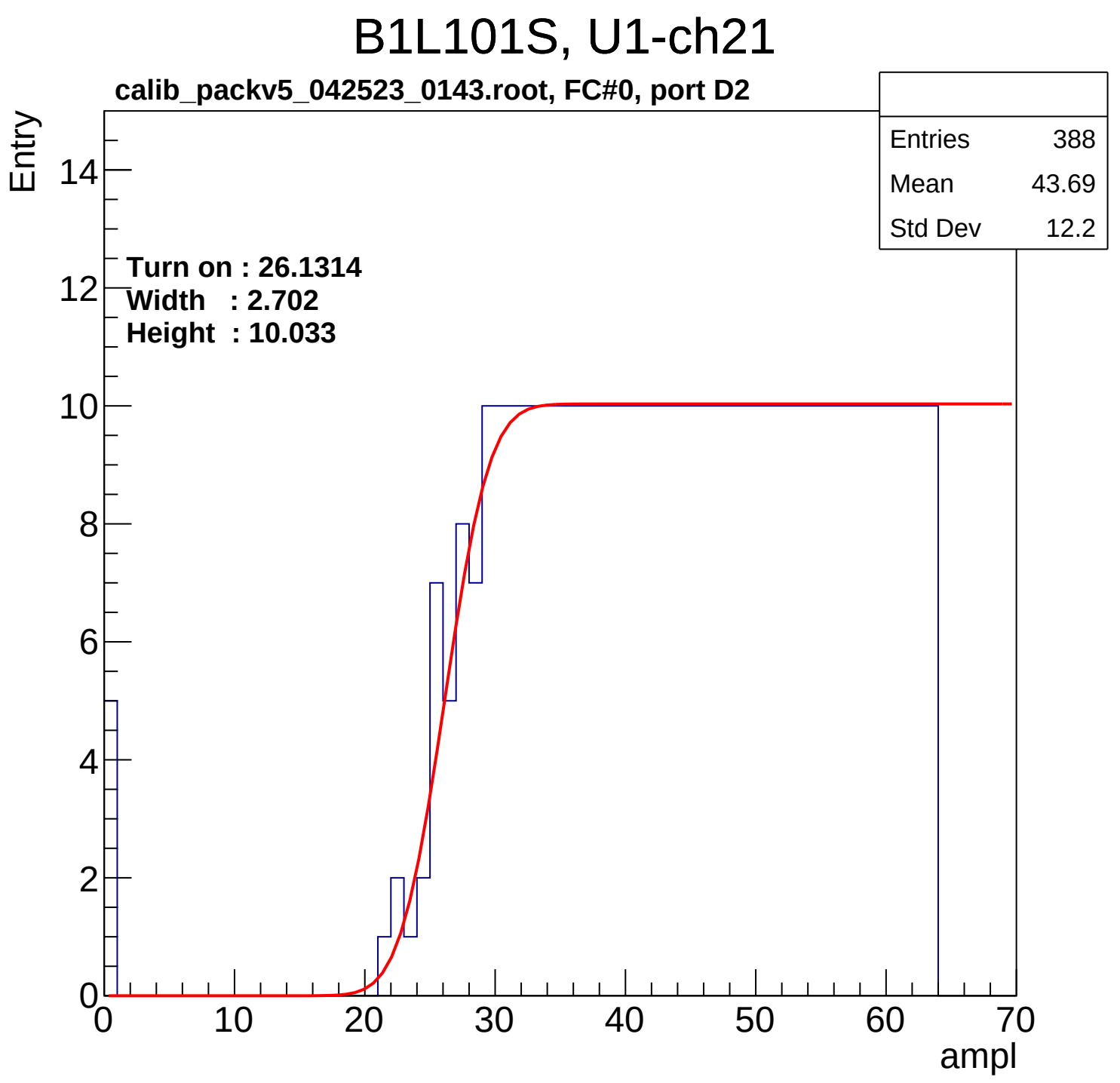
B1L101S, U1-ch21
calib_packv5_042523_0143.root, FC#0, port D2
Entries 388
Mean 43.69
Std Dev 12.2
Turn on : 26.1314
Width : 2.702
Height : 10.033
Entry
ampl
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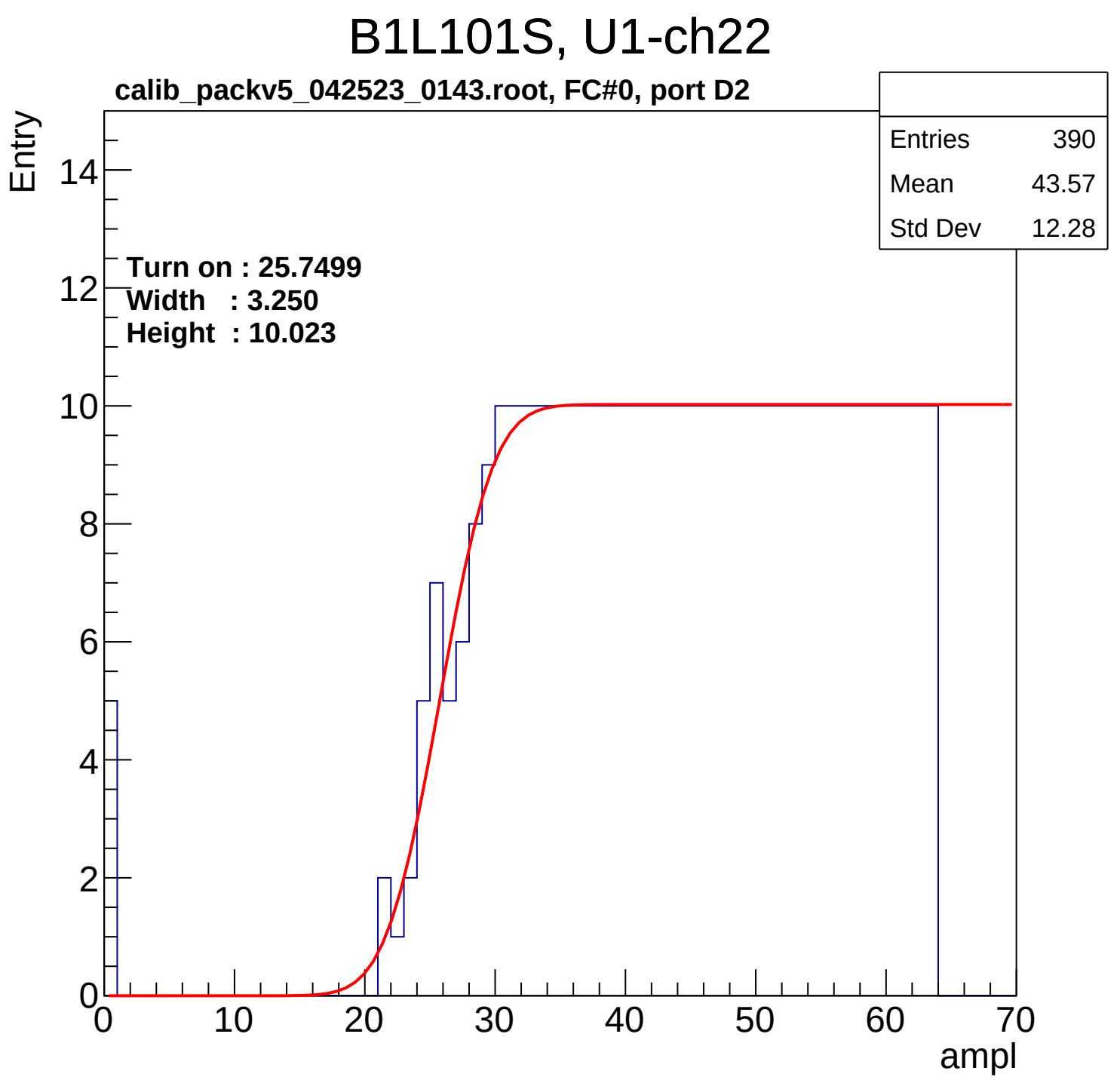
B1L101S, U1-ch22
calib_packv5_042523_0143.root, FC#0, port D2
Entries 390
Mean 43.57
Std Dev 12.28
Turn on : 25.7499
Width : 3.250
Height : 10.023
Entry
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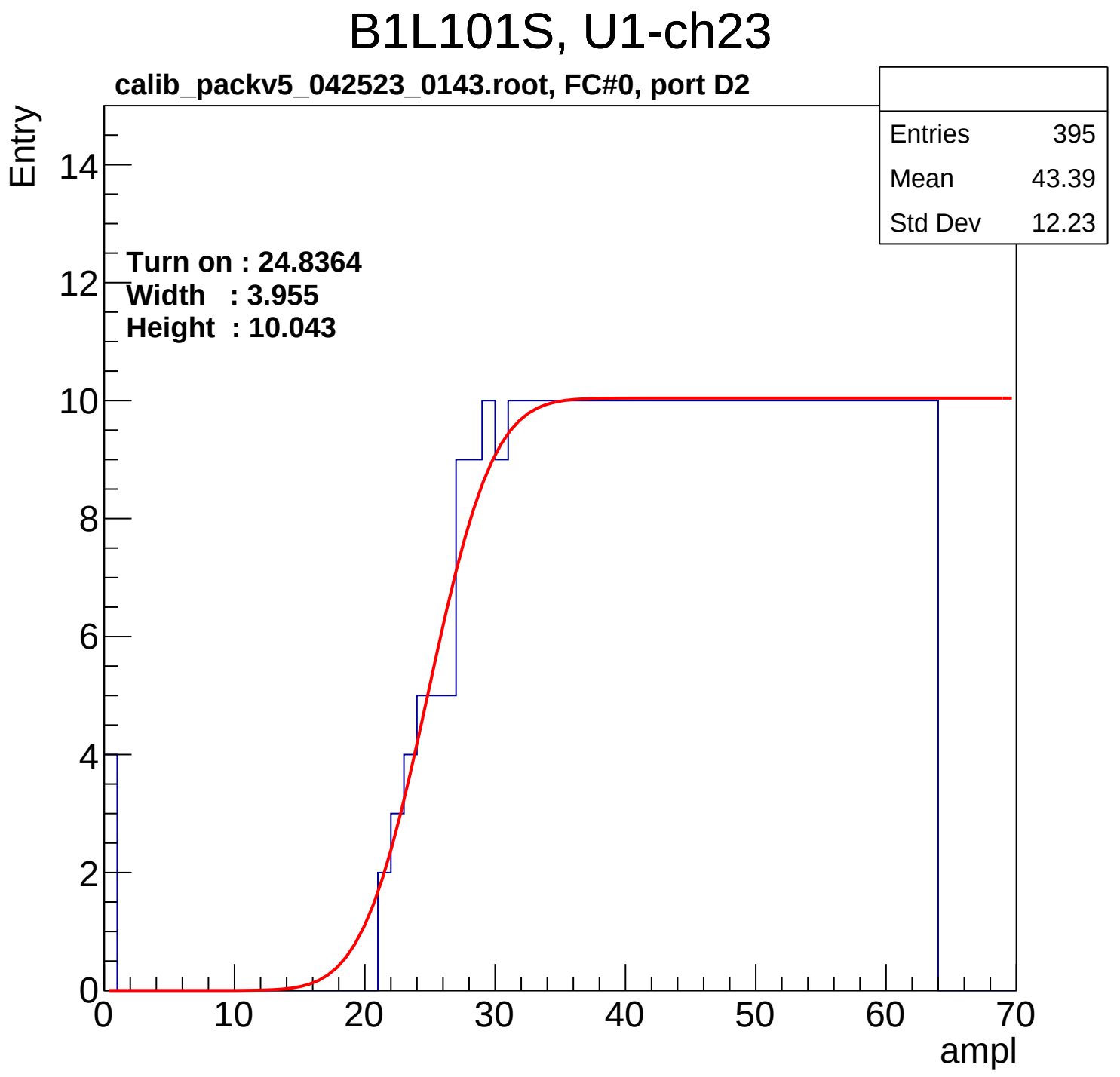
B1L101S, U1-ch23
calib_packv5_042523_0143.root, FC#0, port D2
Entries 395
Mean 43.39
Std Dev 12.23
Turn on : 24.8364
Width : 3.955
Height : 10.043
Entry
ampl
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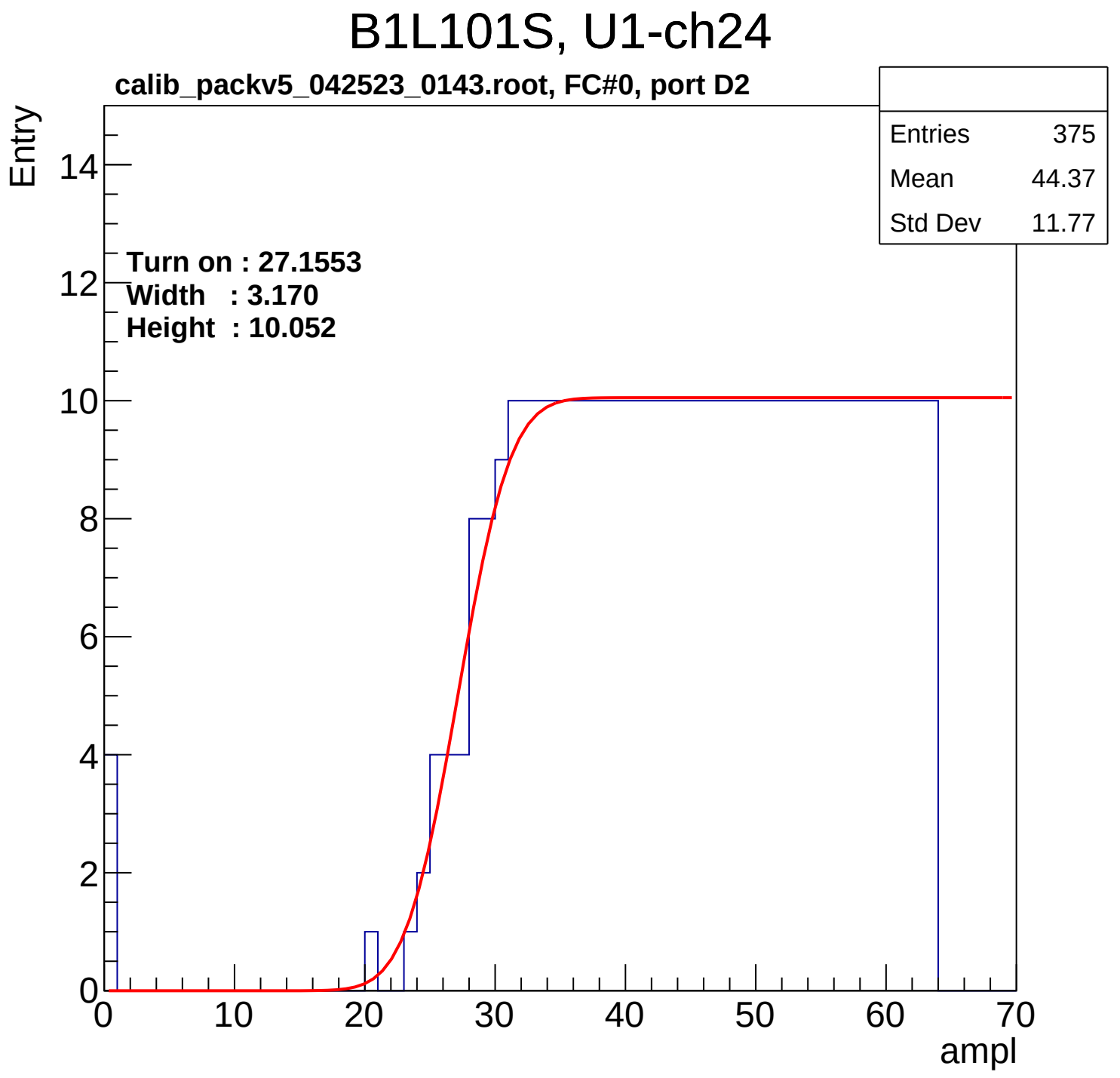
B1L101S, U1-ch24
calib_packv5_042523_0143.root, FC#0, port D2
Entries 375
Mean 44.37
Std Dev 11.77
Turn on : 27.1553
Width : 3.170
Height : 10.052
Entry
ampl
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6
8
10
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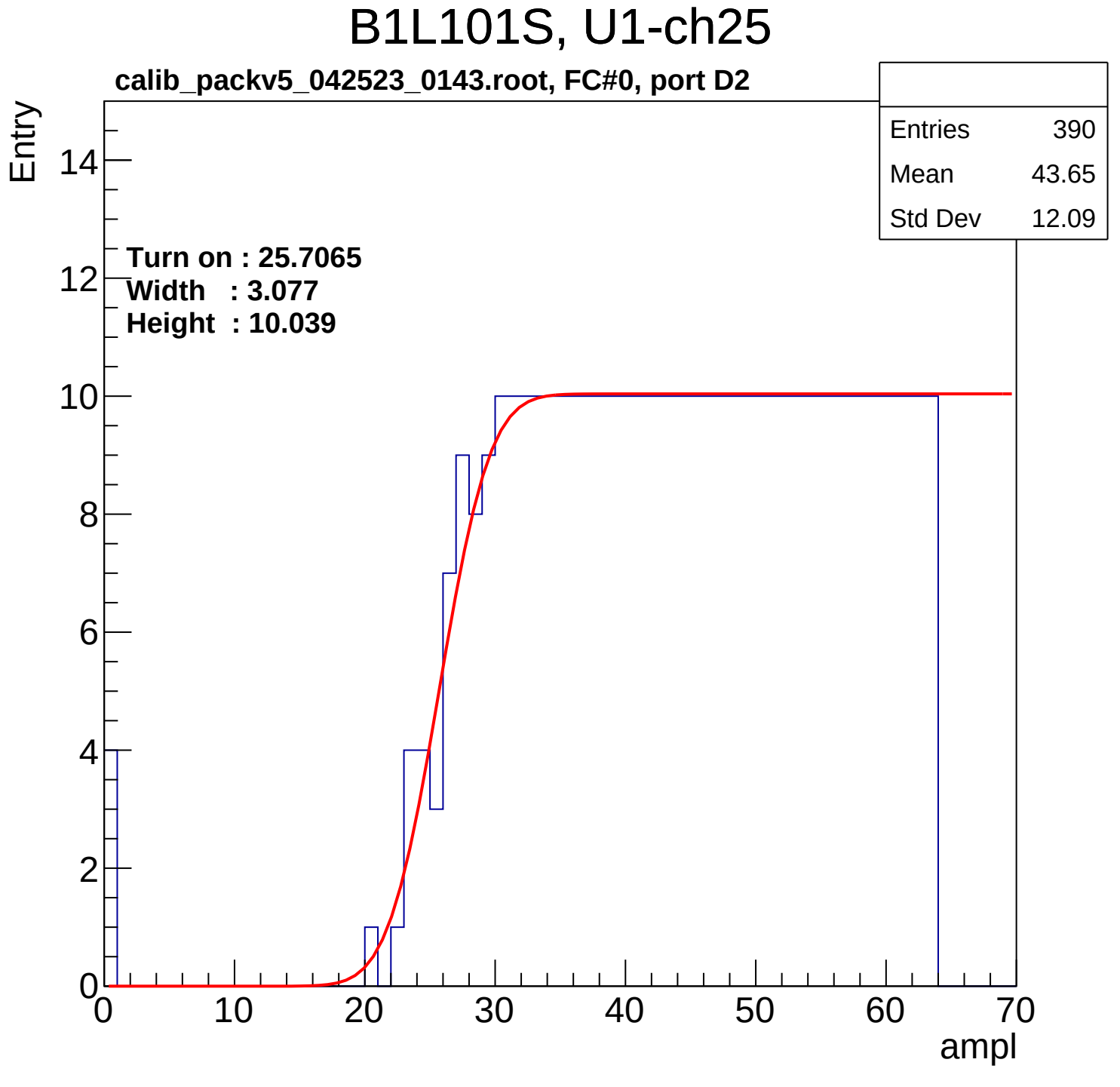
B1L101S, U1-ch25
calib_packv5_042523_0143.root, FC#0, port D2
Entries 390
Mean 43.65
Std Dev 12.09
Turn on : 25.7065
Width : 3.077
Height : 10.039
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ampl
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6
8
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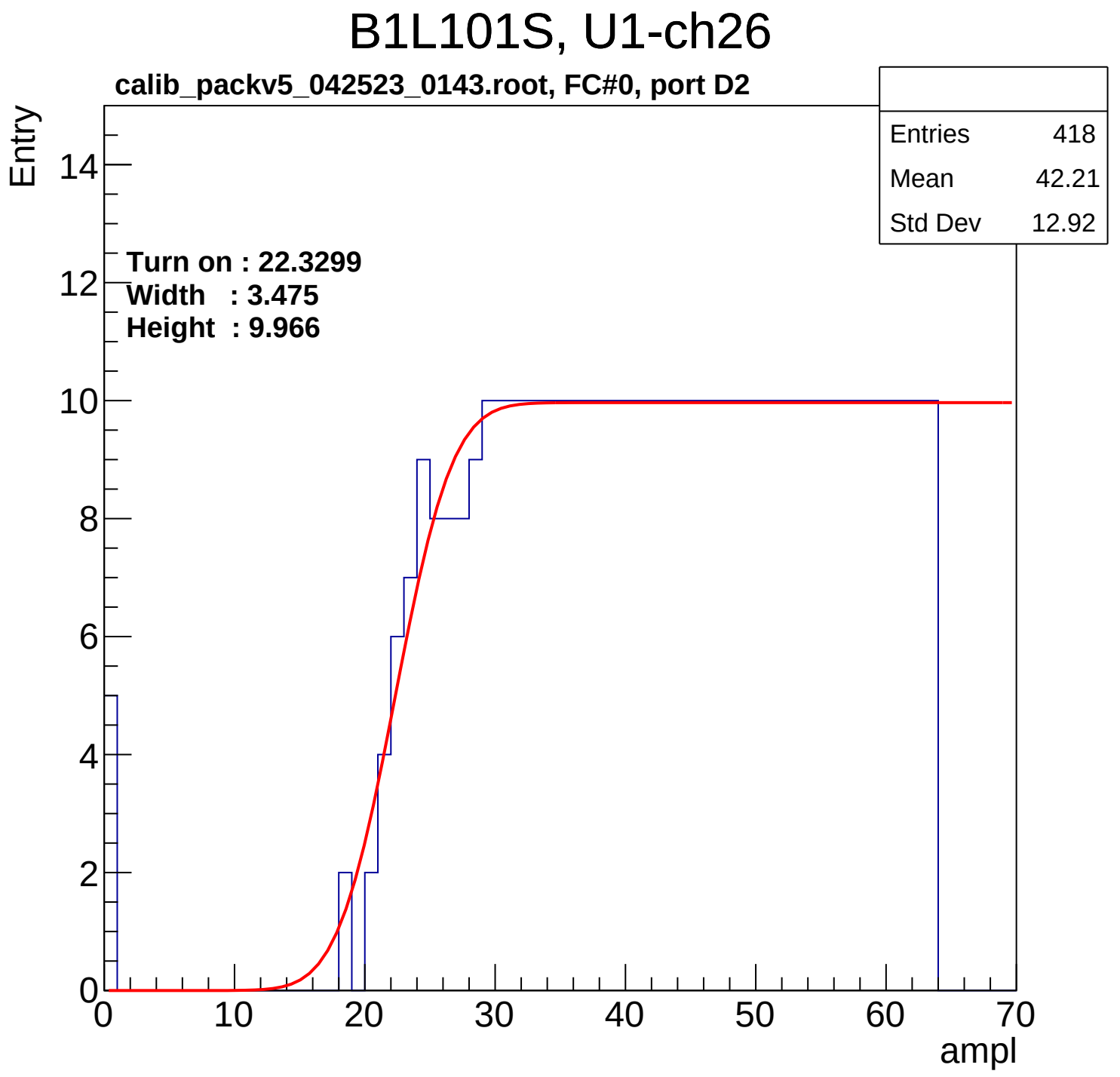
B1L101S, U1-ch26
calib_packv5_042523_0143.root, FC#0, port D2
Entries 418
Mean 42.21
Std Dev 12.92
Turn on : 22.3299
Width : 3.475
Height : 9.966
Entry
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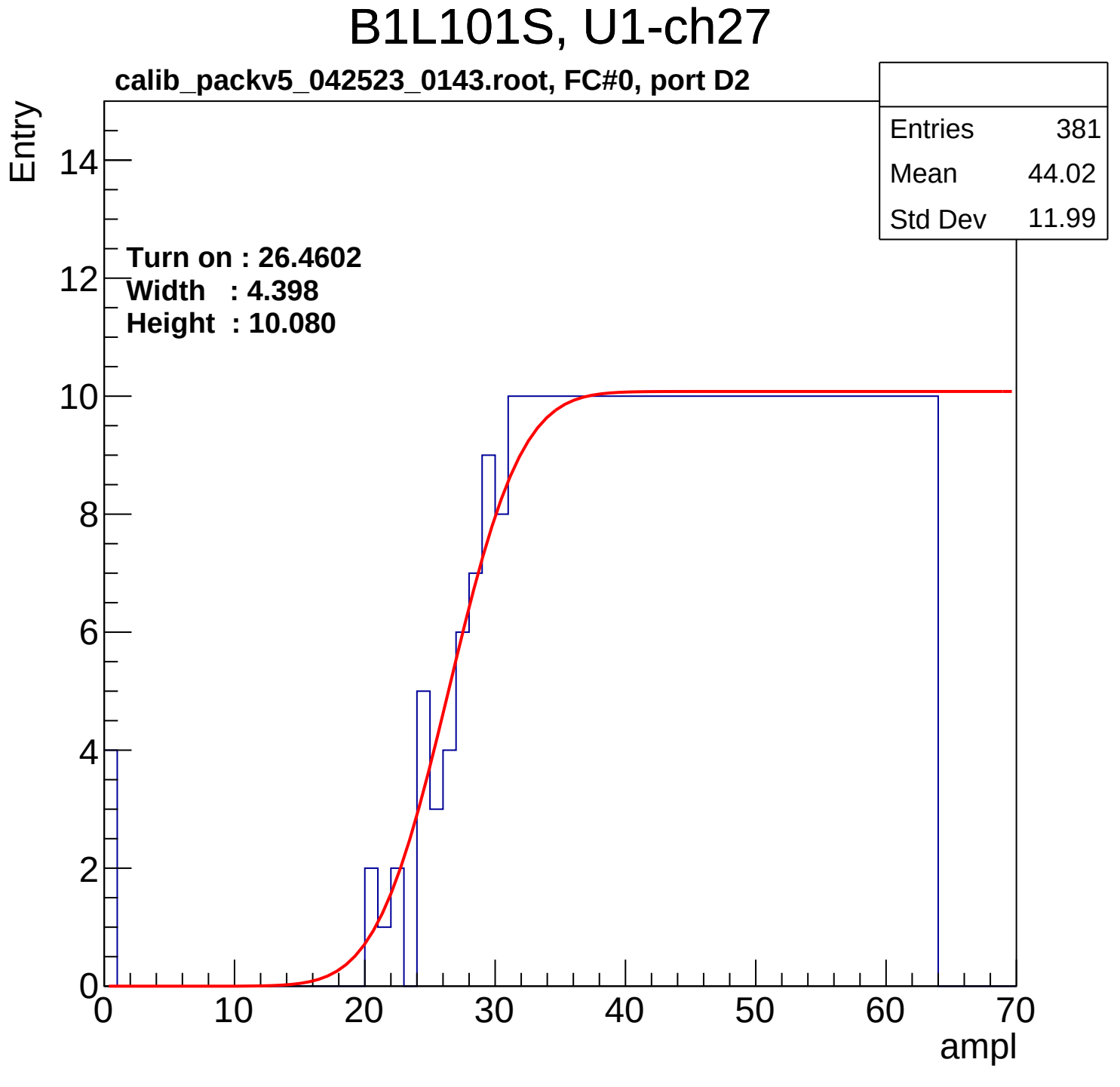
B1L101S, U1-ch27
calib_packv5_042523_0143.root, FC#0, port D2
Entries 381
Mean 44.02
Std Dev 11.99
Turn on : 26.4602
Width : 4.398
Height : 10.080
Entry
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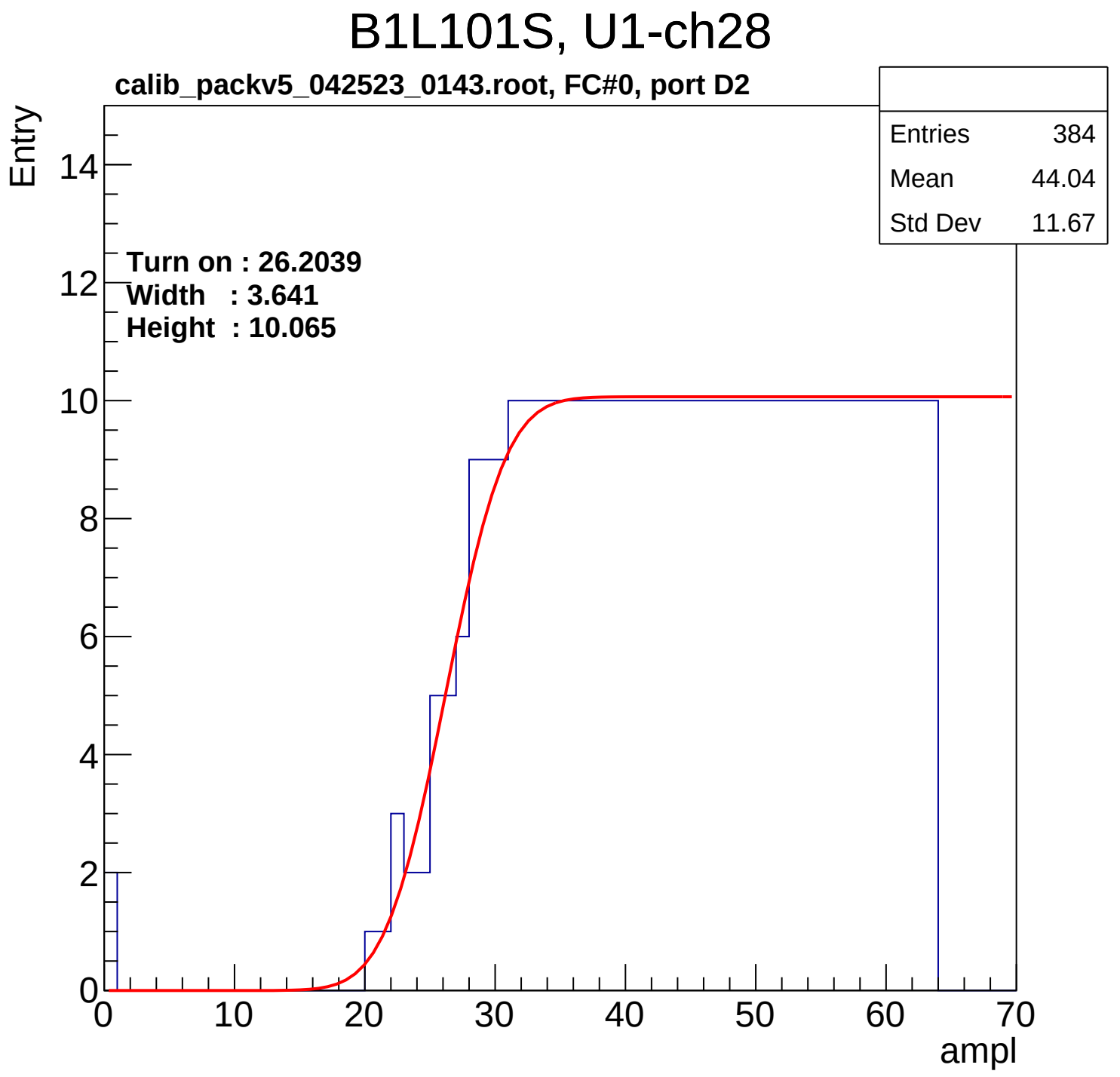
B1L101S, U1-ch28
calib_packv5_042523_0143.root, FC#0, port D2
Entries 384
Mean 44.04
Std Dev 11.67
Turn on : 26.2039
Width : 3.641
Height : 10.065
Entry
ampl
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4
6
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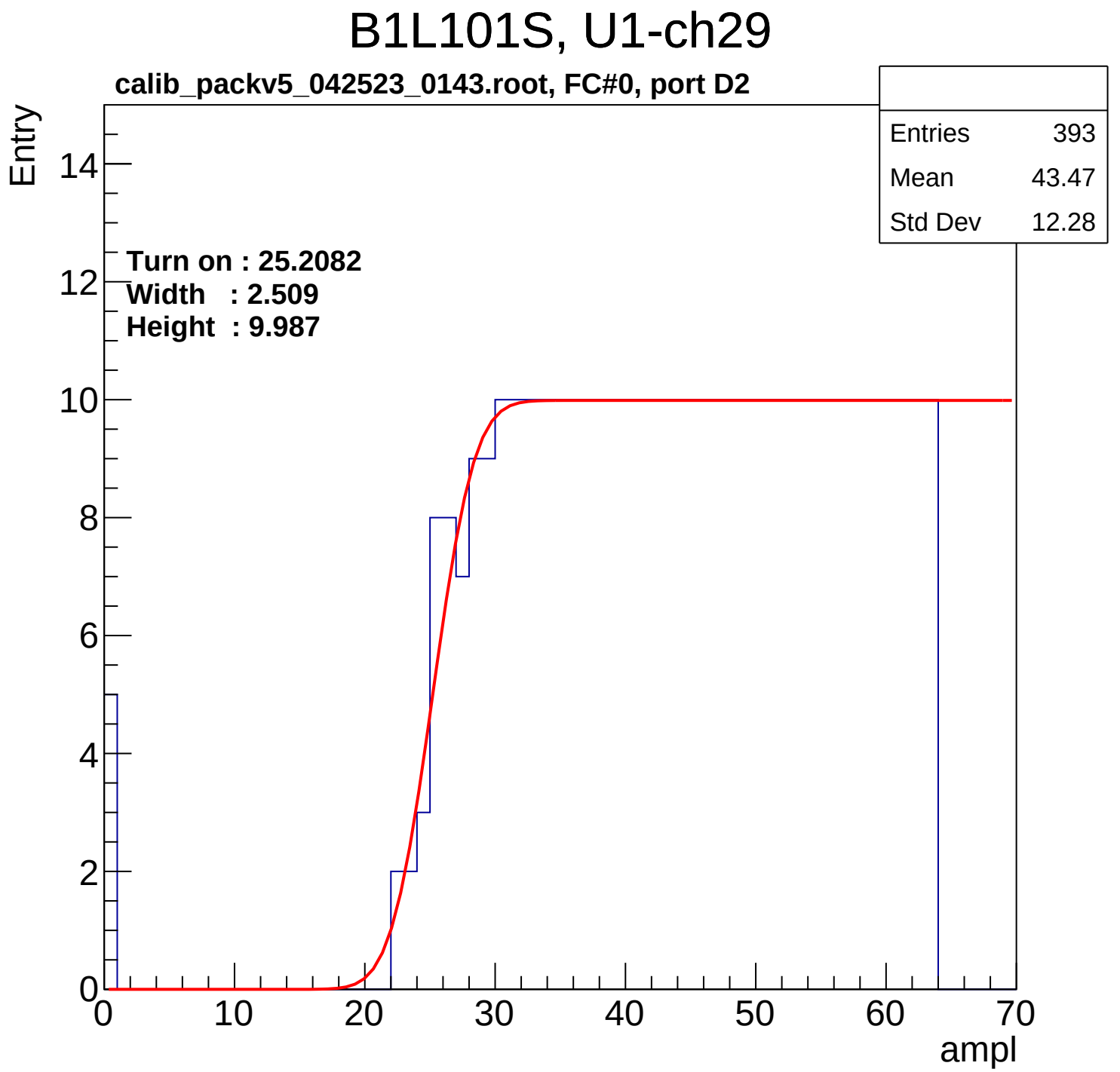
B1L101S, U1-ch29
calib_packv5_042523_0143.root, FC#0, port D2
Entries 393
Mean 43.47
Std Dev 12.28
Turn on : 25.2082
Width : 2.509
Height : 9.987
Entry
ampl
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8
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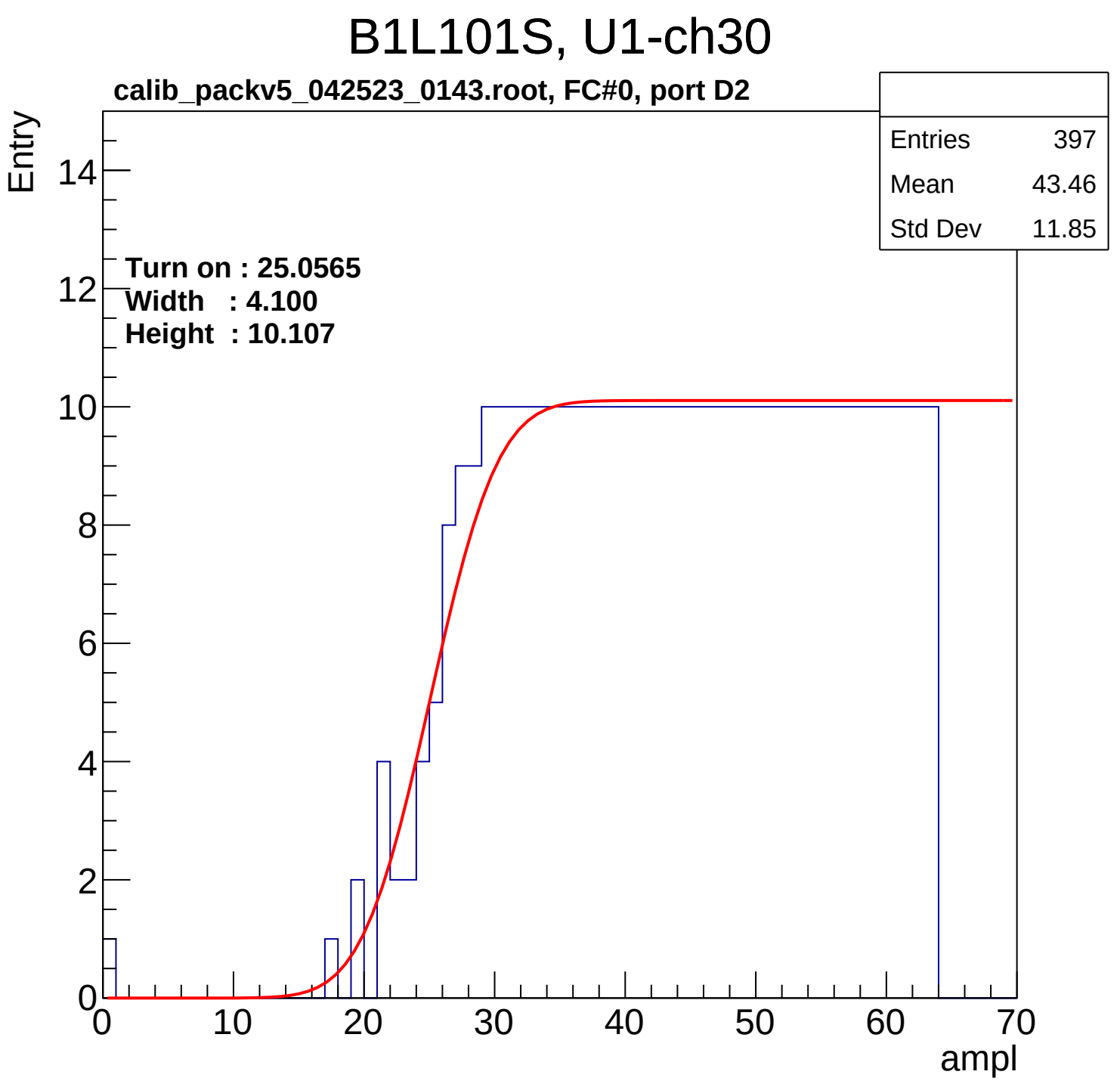
B1L101S, U1-ch30
calib_packv5_042523_0143.root, FC#0, port D2
Entries 397
Mean 43.46
Std Dev 11.85
Turn on : 25.0565
Width : 4.100
Height : 10.107
Entry
ampl
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4
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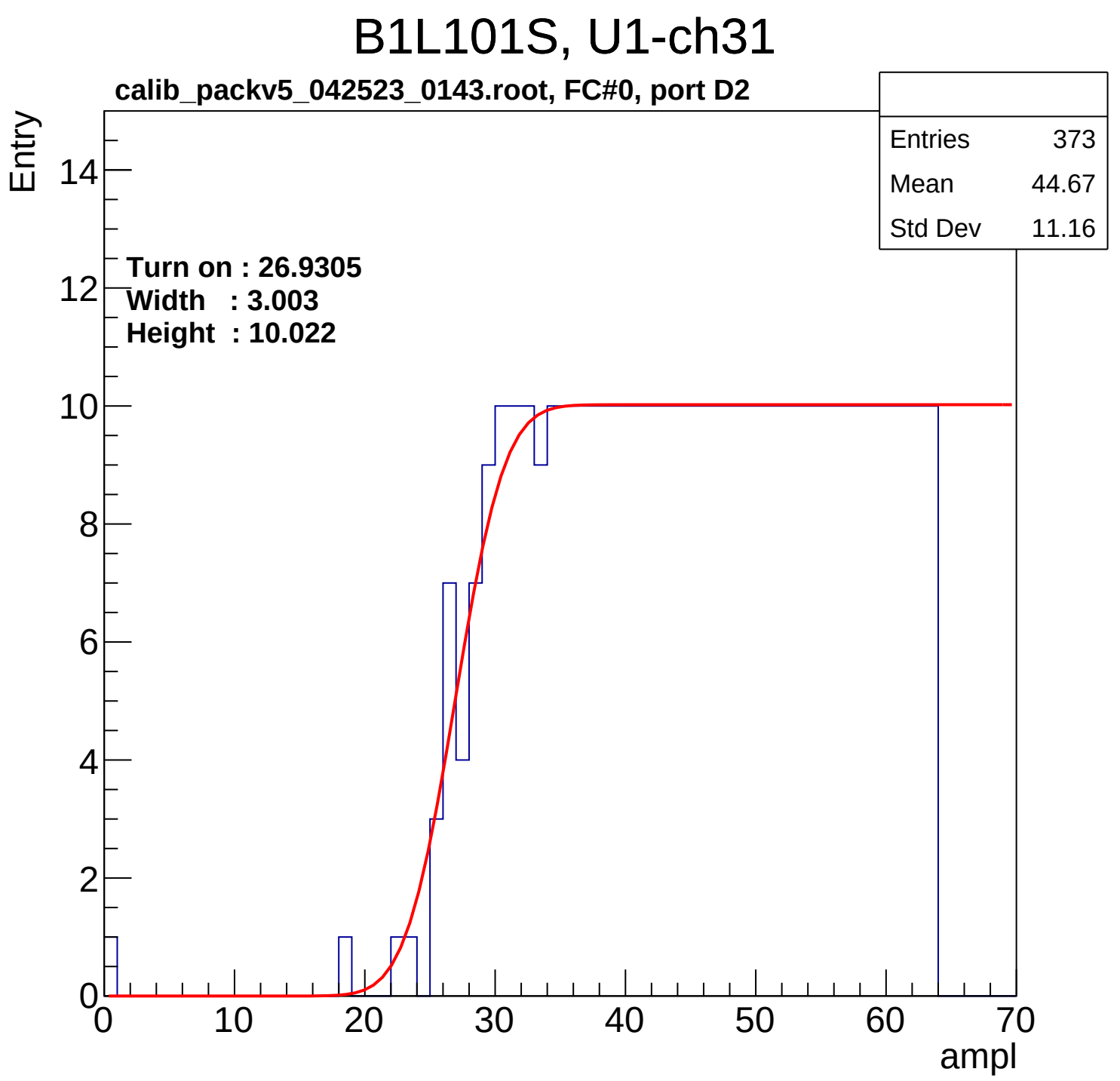
B1L101S, U1-ch31
calib_packv5_042523_0143.root, FC#0, port D2
Entries 373
Mean 44.67
Std Dev 11.16
Turn on : 26.9305
Width : 3.003
Height : 10.022
Entry
ampl
0
2
4
6
8
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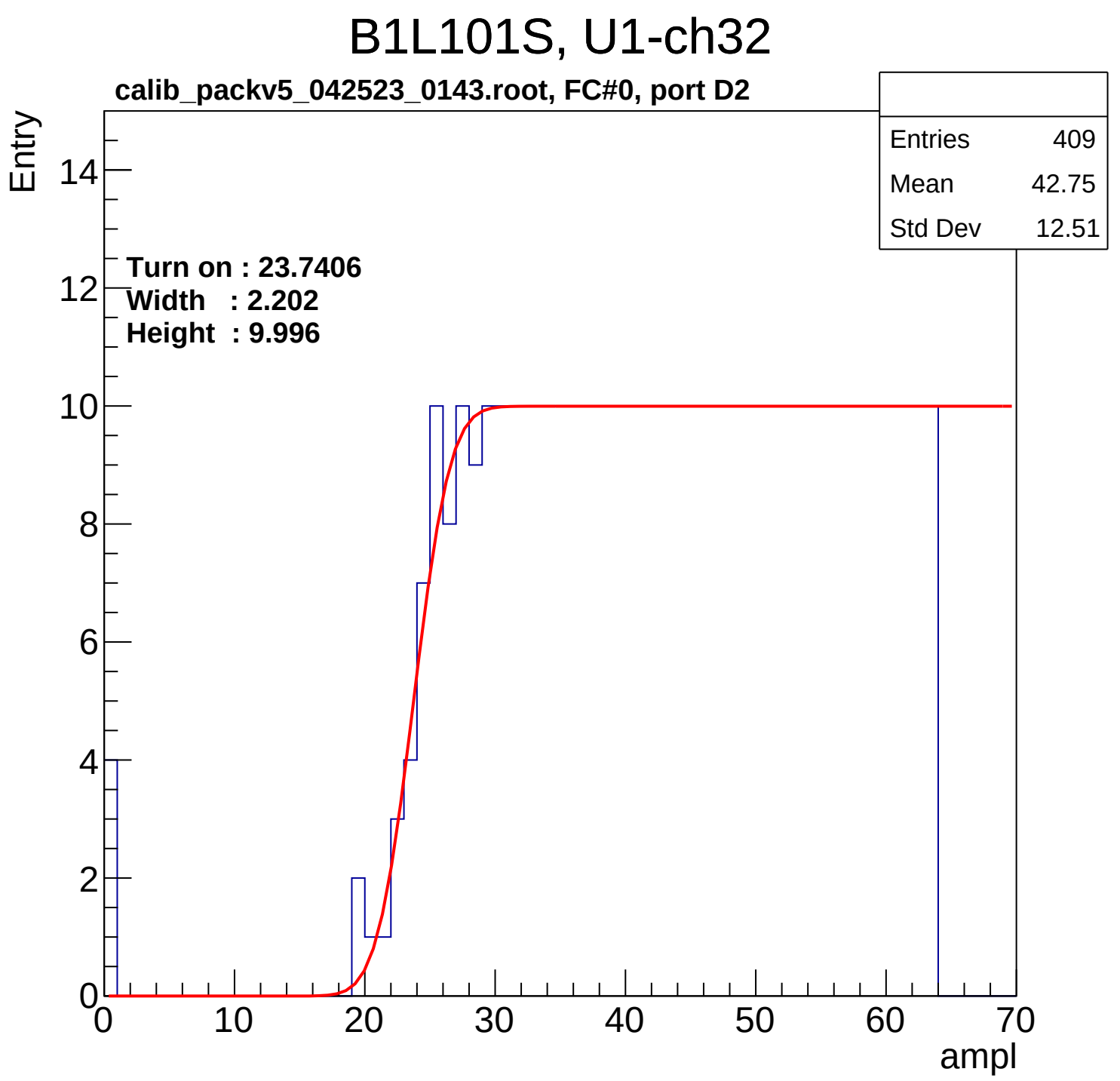
B1L101S, U1-ch32
calib_packv5_042523_0143.root, FC#0, port D2
Entries 409
Mean 42.75
Std Dev 12.51
Turn on : 23.7406
Width : 2.202
Height : 9.996
Entry
ampl
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2
4
6
8
10
12
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0
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60
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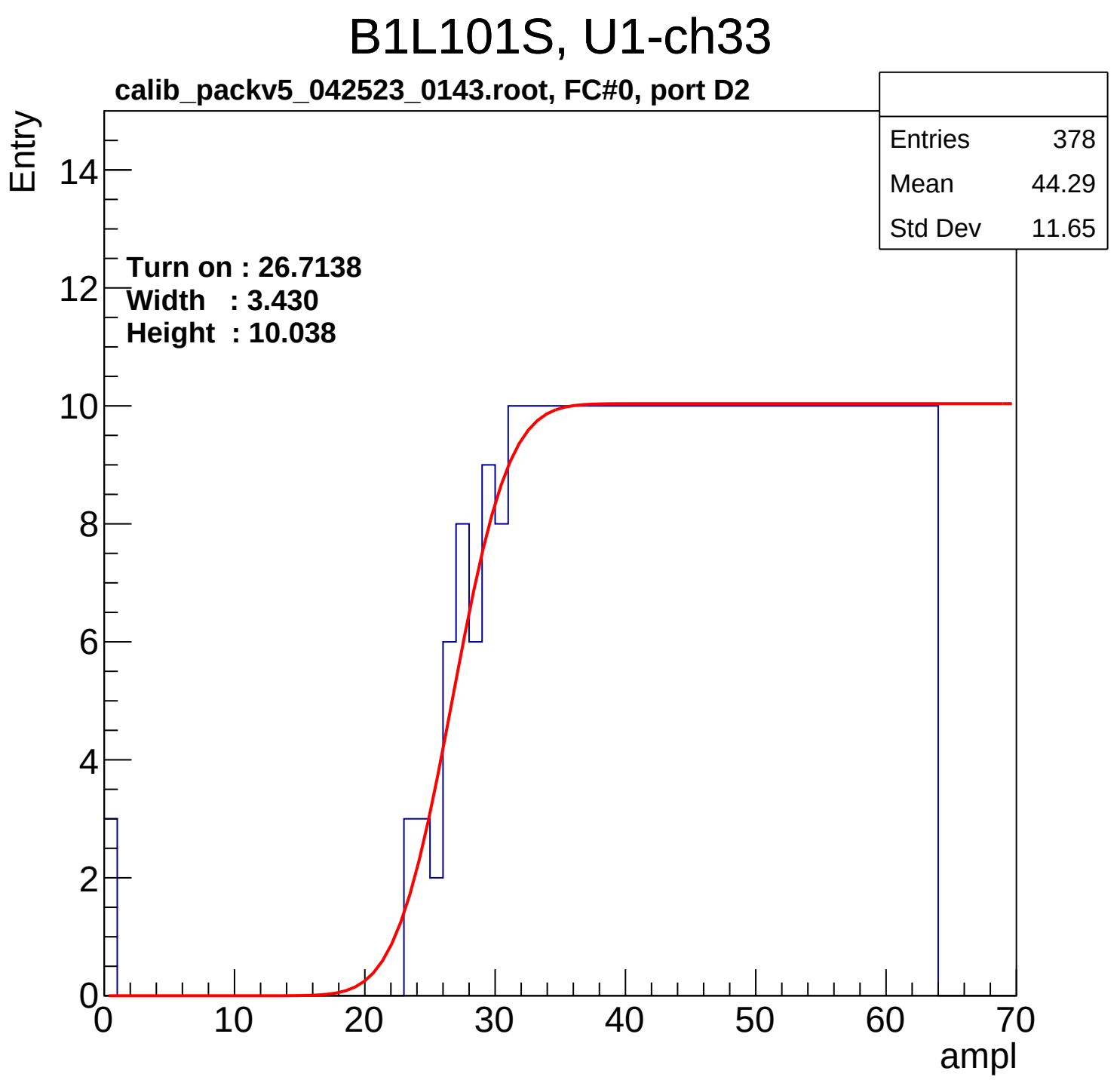
B1L101S, U1-ch33
calib_packv5_042523_0143.root, FC#0, port D2
Entries 378
Mean 44.29
Std Dev 11.65
Turn on : 26.7138
Width : 3.430
Height : 10.038
Entry
ampl
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2
4
6
8
10
12
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0
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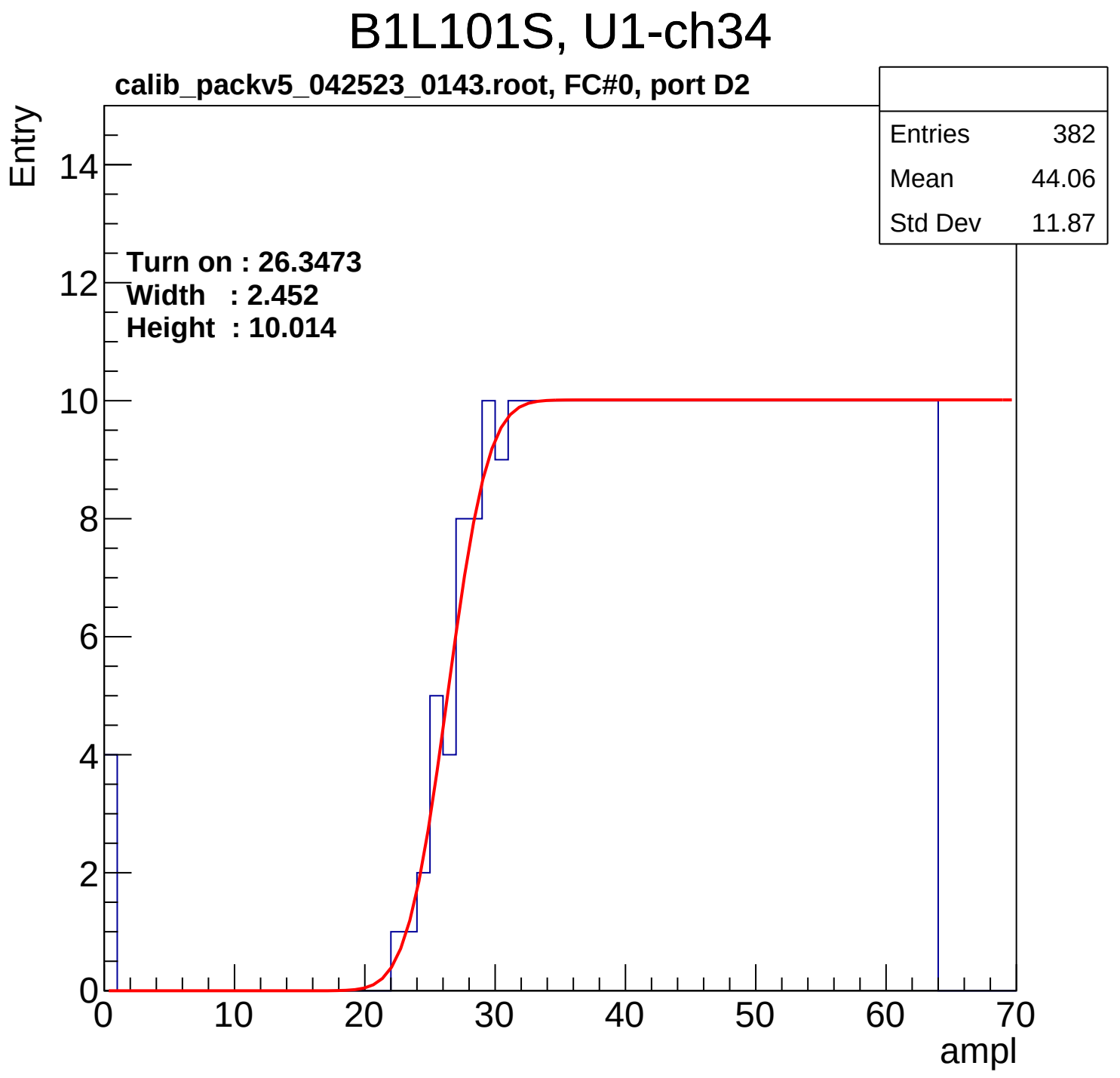
B1L101S, U1-ch34
calib_packv5_042523_0143.root, FC#0, port D2
Entries 382
Mean 44.06
Std Dev 11.87
Turn on : 26.3473
Width : 2.452
Height : 10.014
Entry
ampl
0
2
4
6
8
10
12
14
0
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40
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60
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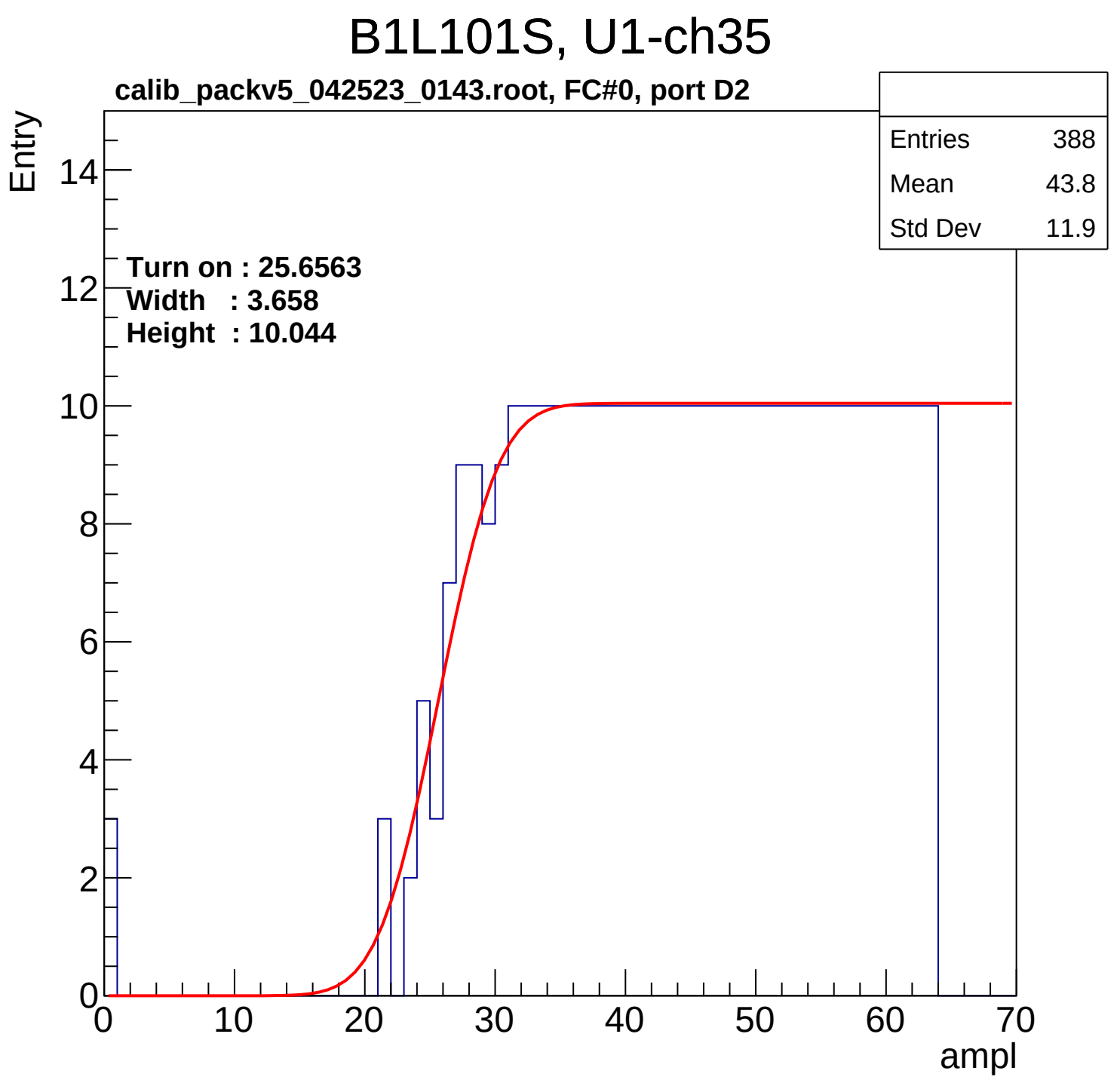
B1L101S, U1-ch35
calib_packv5_042523_0143.root, FC#0, port D2
Entries 388
Mean 43.8
Std Dev 11.9
Turn on : 25.6563
Width : 3.658
Height : 10.044
Entry
ampl
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2
4
6
8
10
12
14
0
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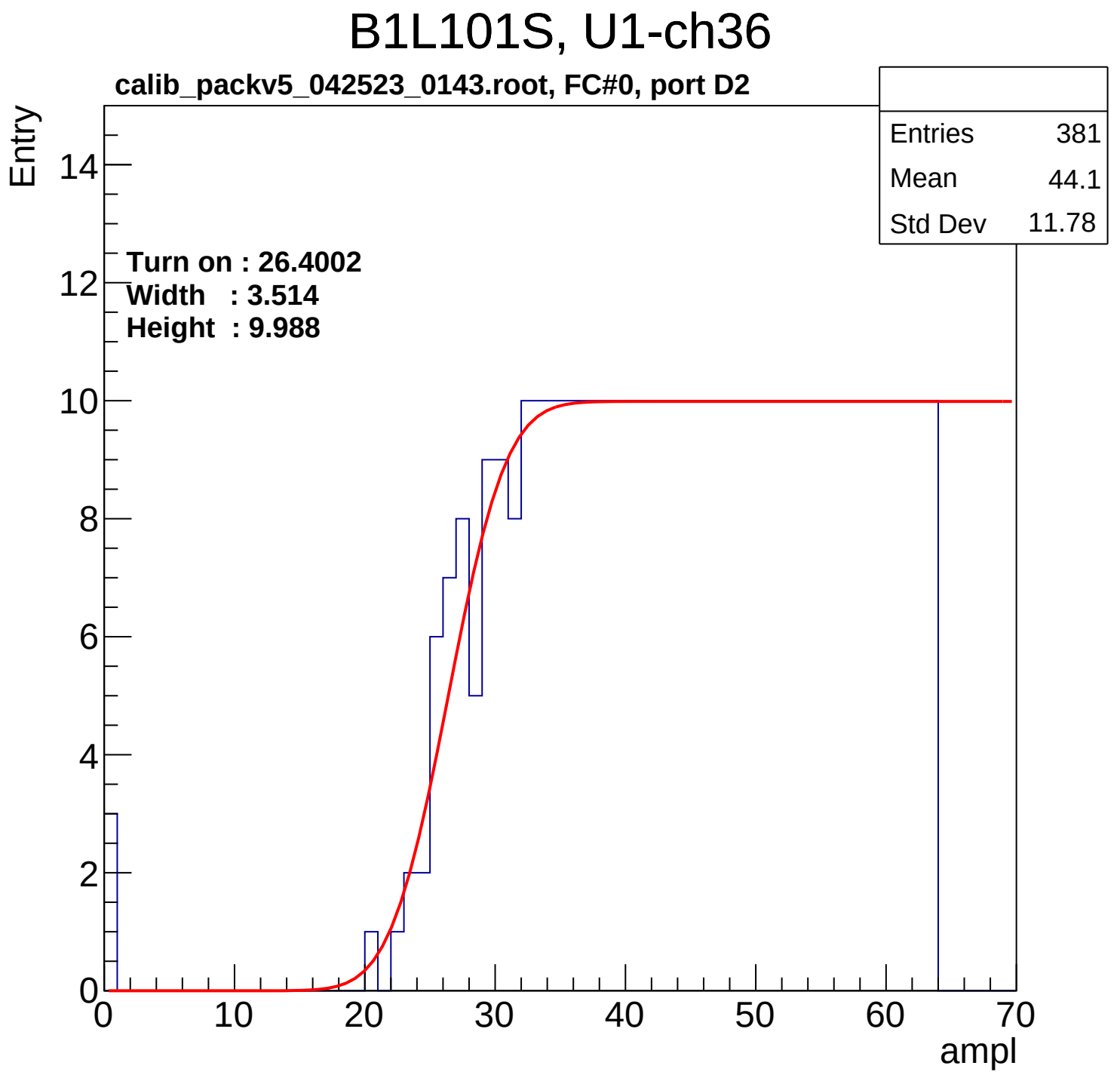
B1L101S, U1-ch36
calib_packv5_042523_0143.root, FC#0, port D2
Entries 381
Mean 44.1
Std Dev 11.78
Turn on : 26.4002
Width : 3.514
Height : 9.988
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
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60
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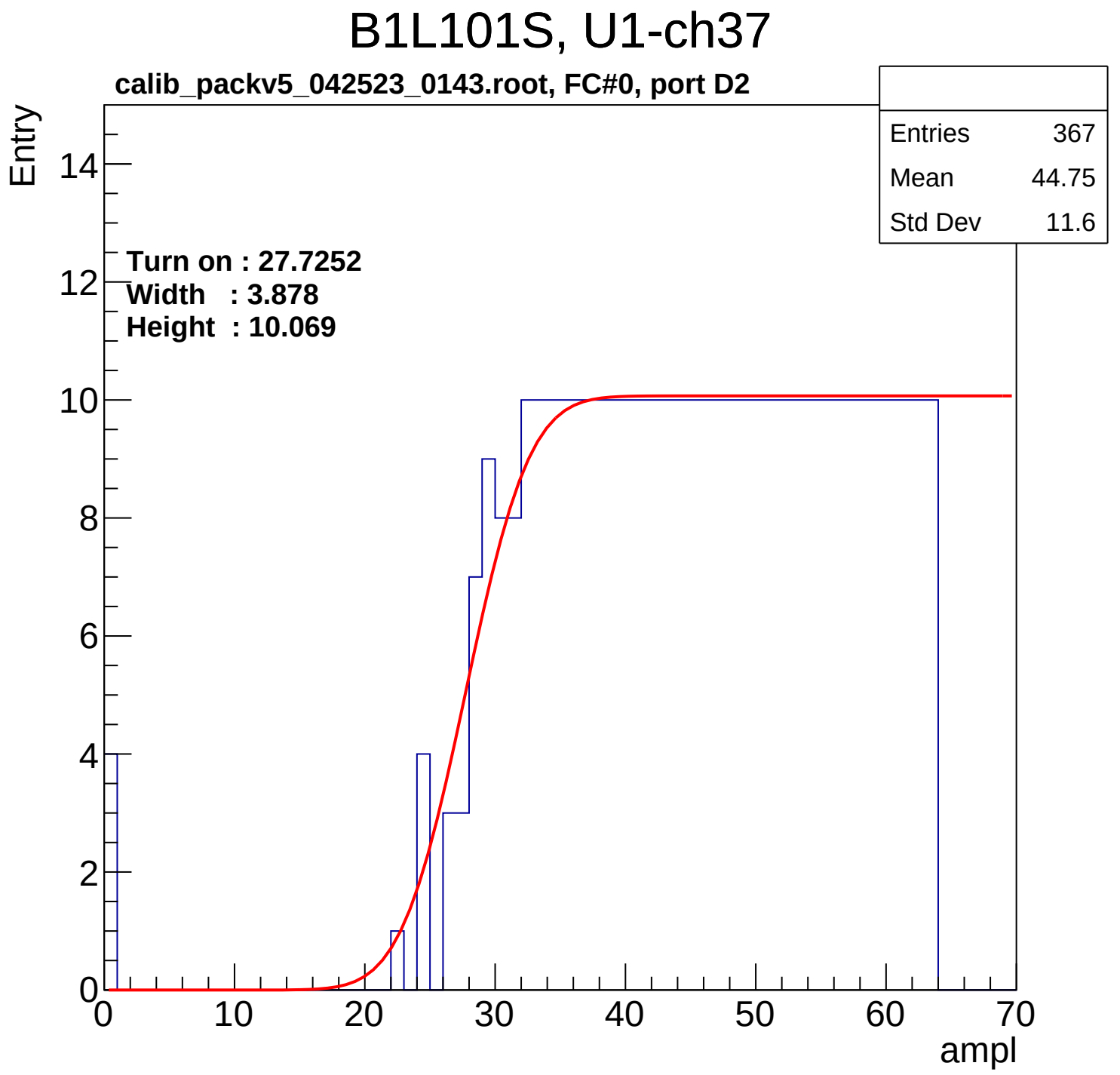
B1L101S, U1-ch37
calib_packv5_042523_0143.root, FC#0, port D2
Entries 367
Mean 44.75
Std Dev 11.6
Turn on : 27.7252
Width : 3.878
Height : 10.069
Entry
ampl
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2
4
6
8
10
12
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0
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60
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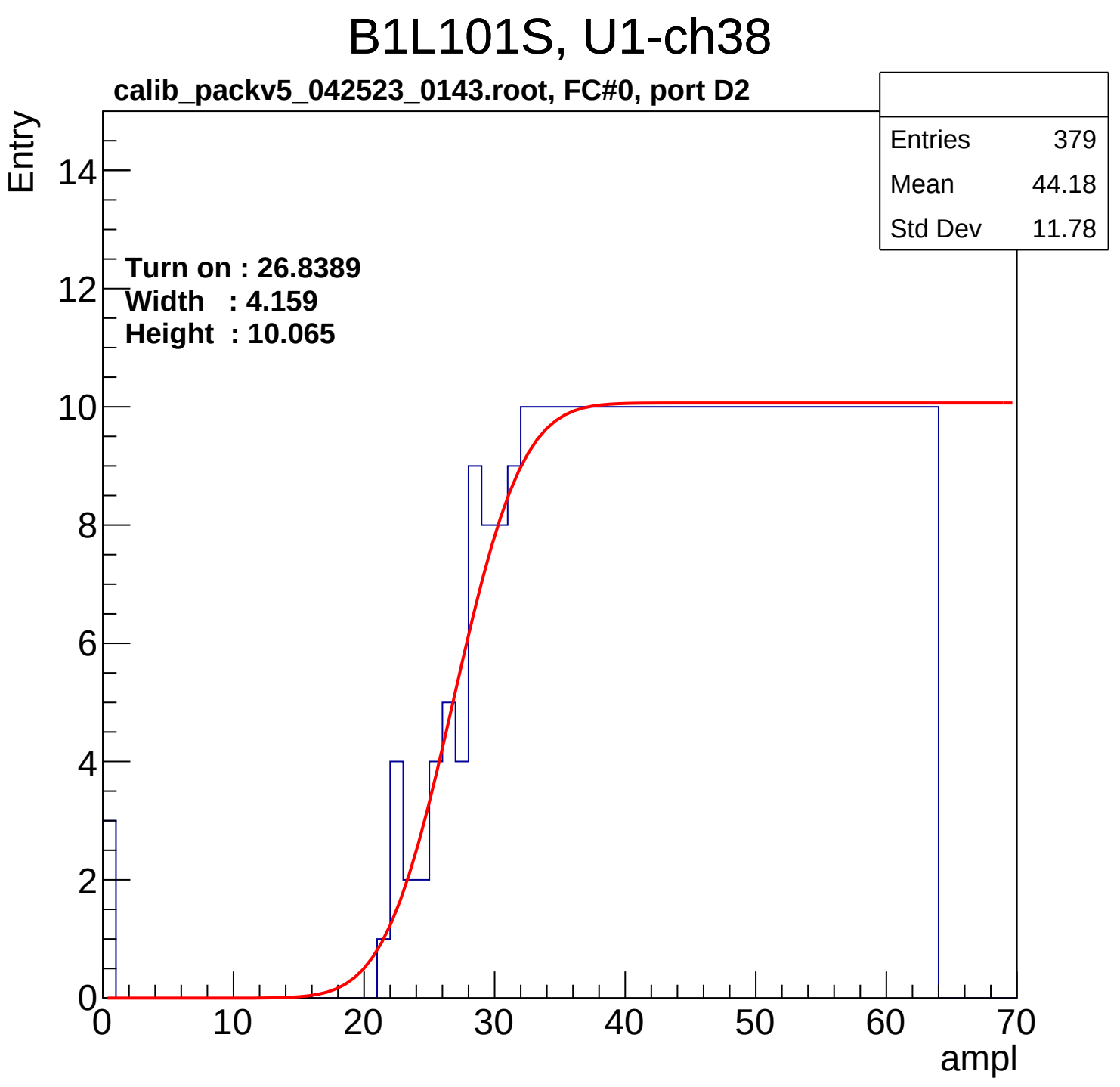
B1L101S, U1-ch38
calib_packv5_042523_0143.root, FC#0, port D2
Entries 379
Mean 44.18
Std Dev 11.78
Turn on : 26.8389
Width : 4.159
Height : 10.065
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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40
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60
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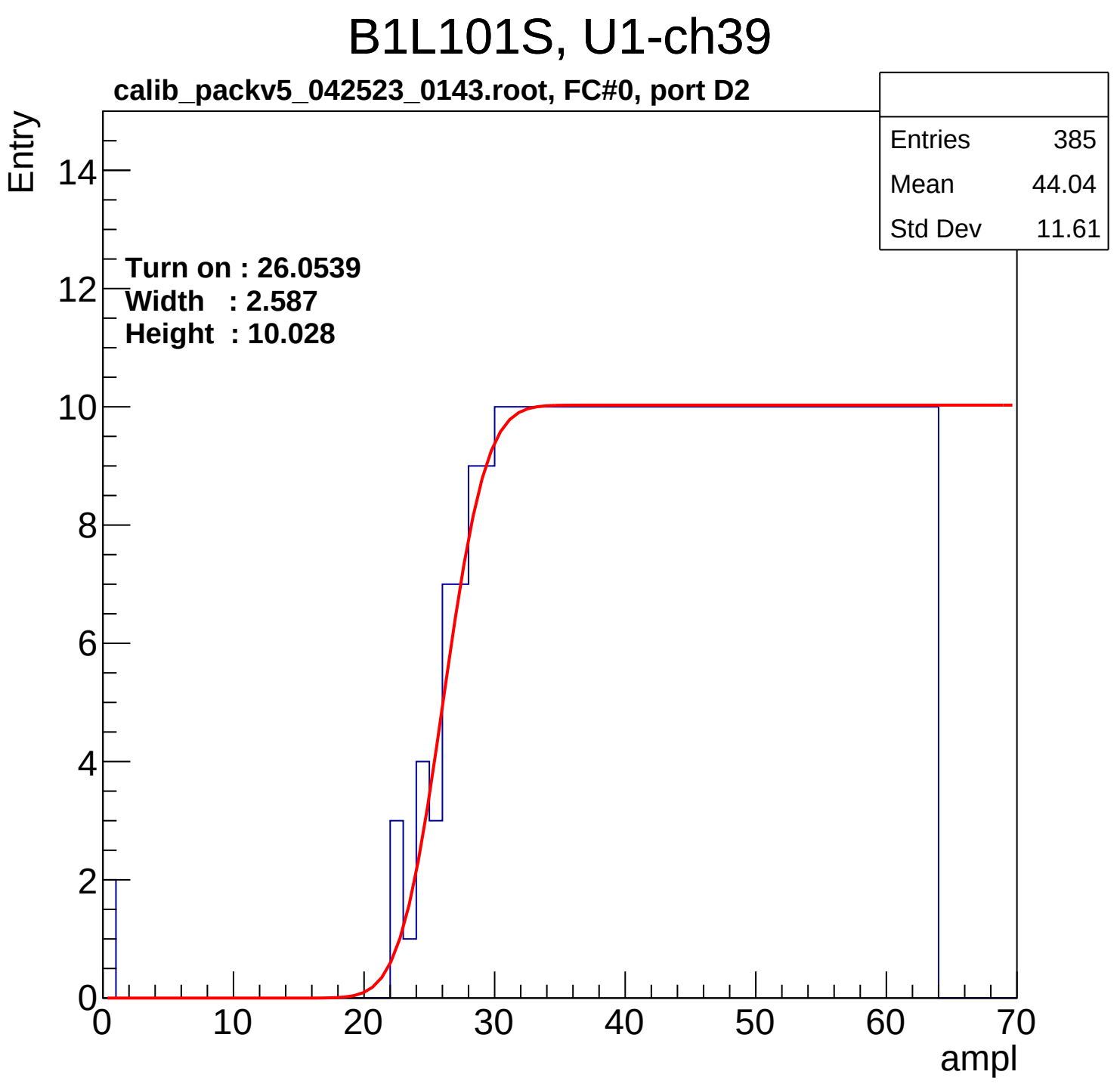
B1L101S, U1-ch39
calib_packv5_042523_0143.root, FC#0, port D2
Entries 385
Mean 44.04
Std Dev 11.61
Turn on : 26.0539
Width : 2.587
Height : 10.028
Entry
ampl
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4
6
8
10
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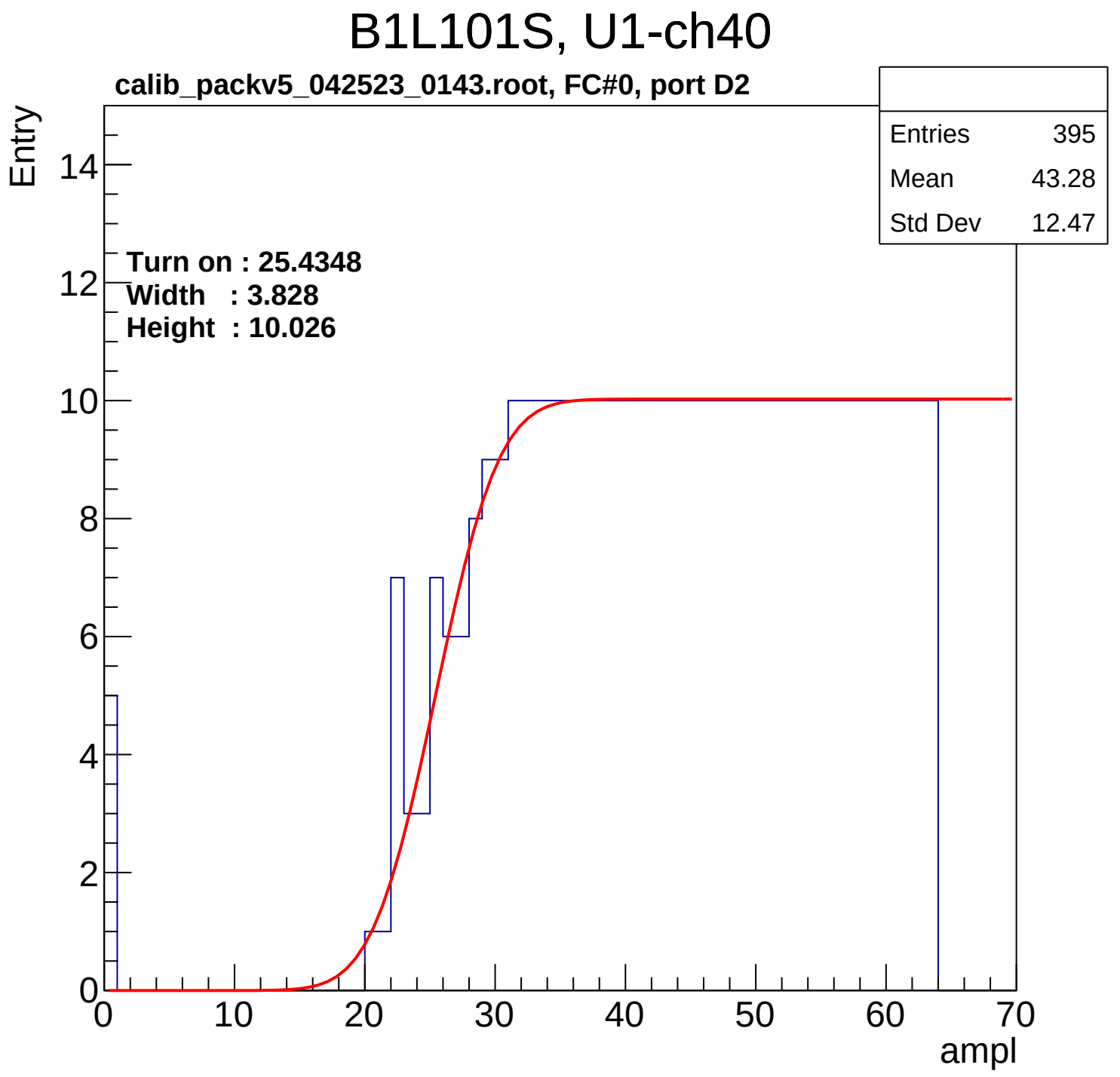
B1L101S, U1-ch40
calib_packv5_042523_0143.root, FC#0, port D2
Entries 395
Mean 43.28
Std Dev 12.47
Turn on : 25.4348
Width : 3.828
Height : 10.026
Entry
ampl
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6
8
10
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0
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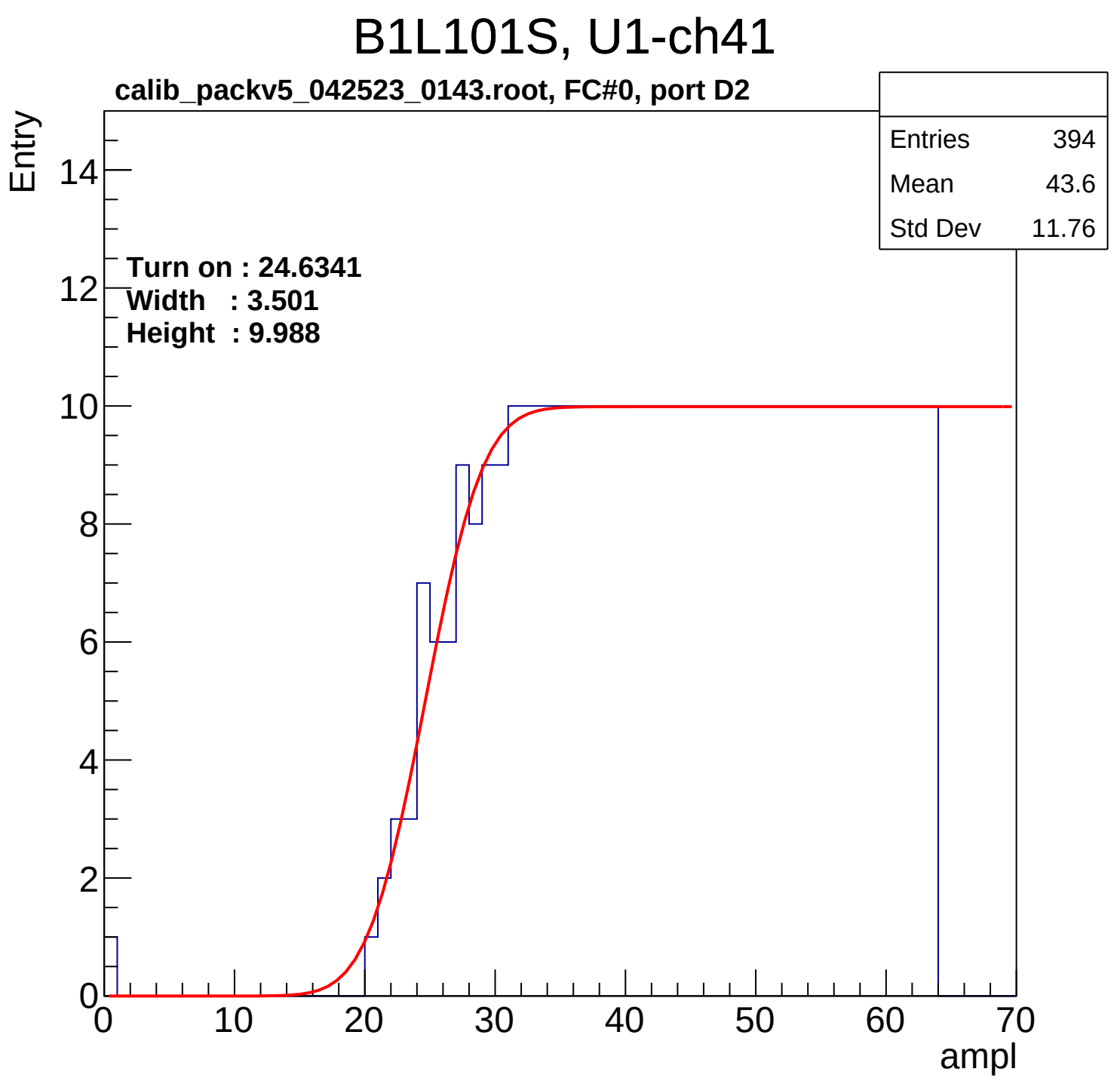
B1L101S, U1-ch41
calib_packv5_042523_0143.root, FC#0, port D2
Entries 394
Mean 43.6
Std Dev 11.76
Turn on : 24.6341
Width : 3.501
Height : 9.988
Entry
ampl
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2
4
6
8
10
12
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0
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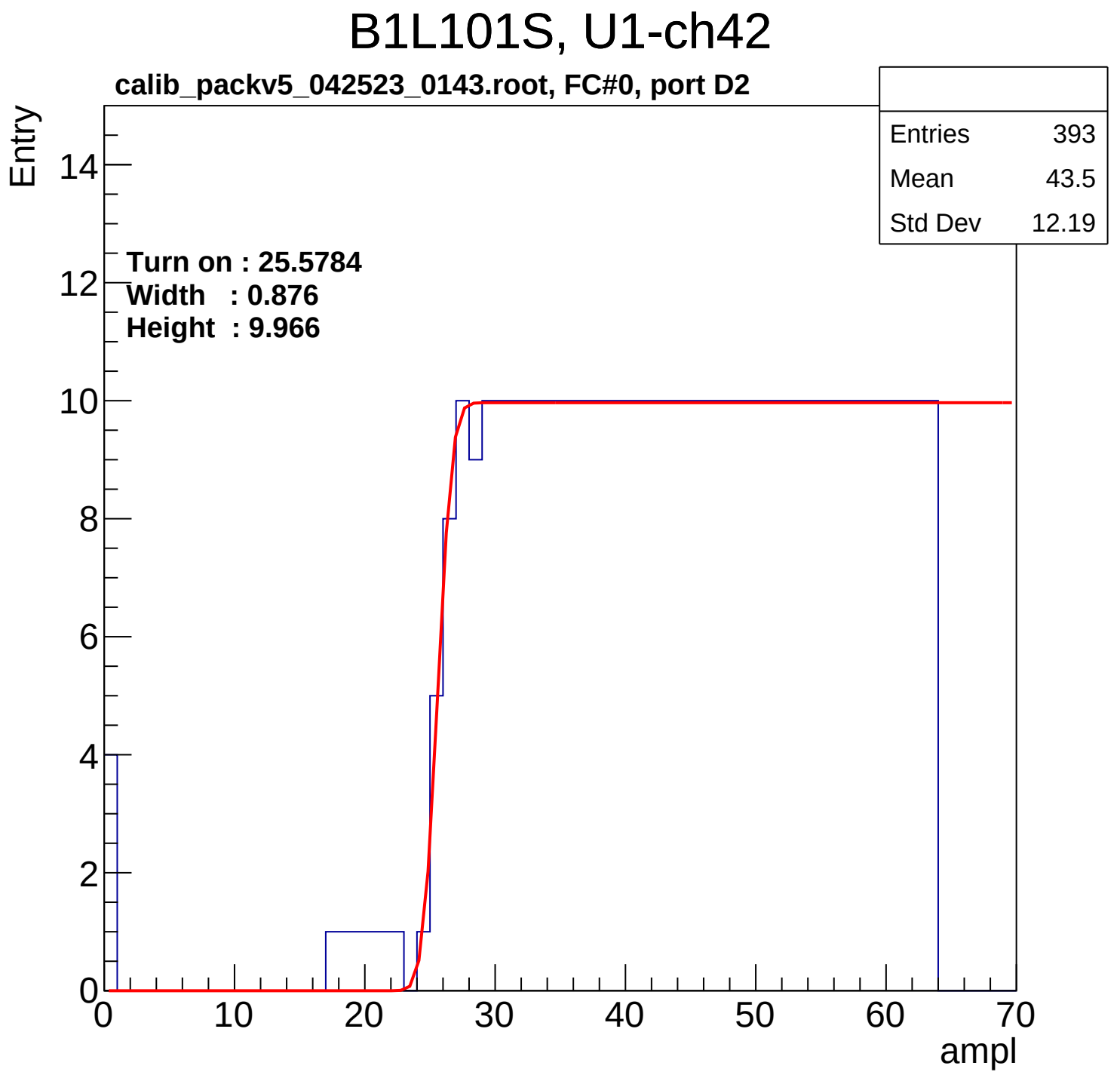
B1L101S, U1-ch42
calib_packv5_042523_0143.root, FC#0, port D2
Entries 393
Mean 43.5
Std Dev 12.19
Turn on : 25.5784
Width : 0.876
Height : 9.966
Entry
ampl
0
2
4
6
8
10
12
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20
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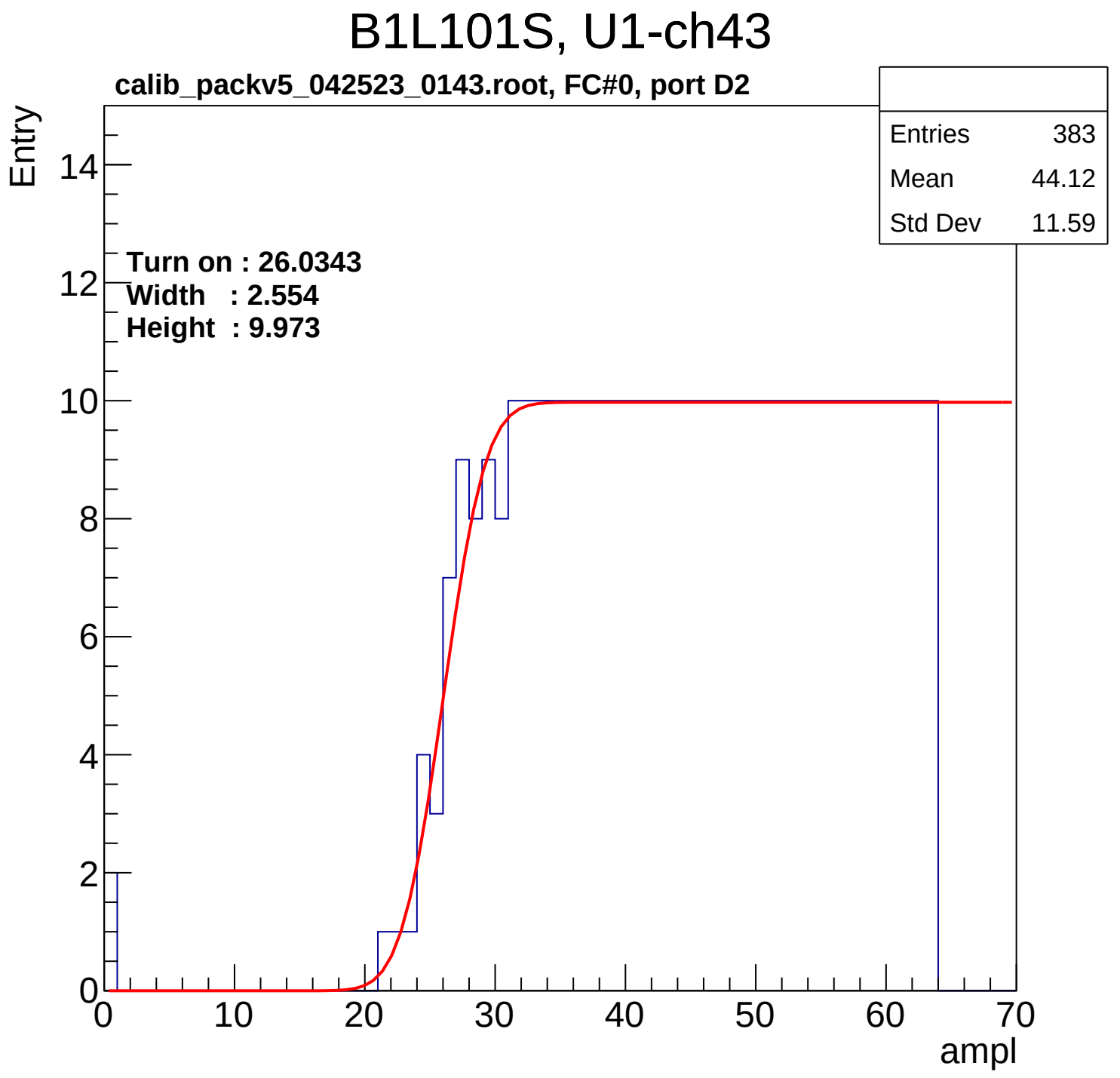
B1L101S, U1-ch43
calib_packv5_042523_0143.root, FC#0, port D2
Entries 383
Mean 44.12
Std Dev 11.59
Turn on : 26.0343
Width : 2.554
Height : 9.973
Entry
ampl
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2
4
6
8
10
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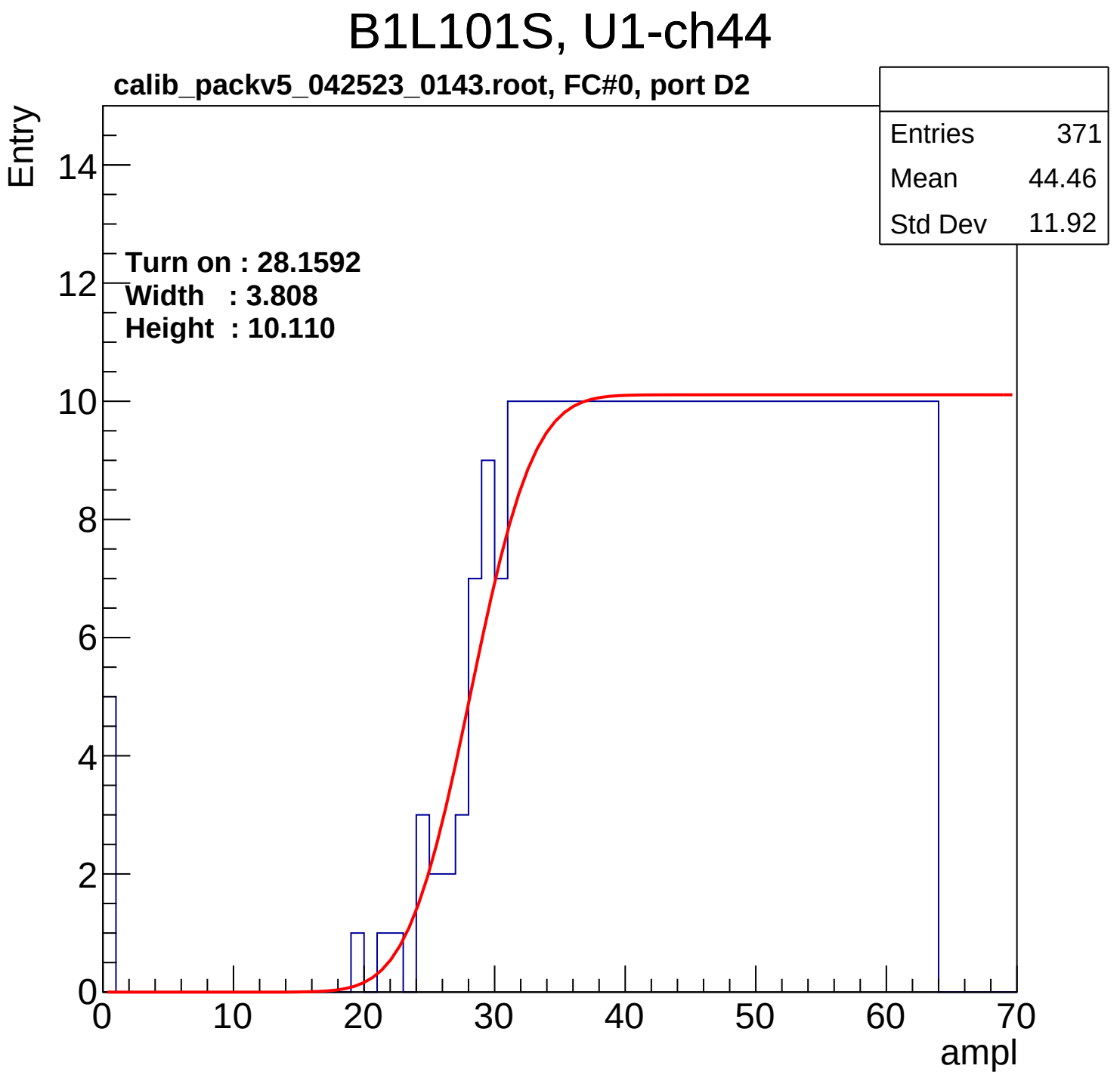
B1L101S, U1-ch44
calib_packv5_042523_0143.root, FC#0, port D2
Entries 371
Mean 44.46
Std Dev 11.92
Turn on : 28.1592
Width : 3.808
Height : 10.110
Entry
ampl
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10
12
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0
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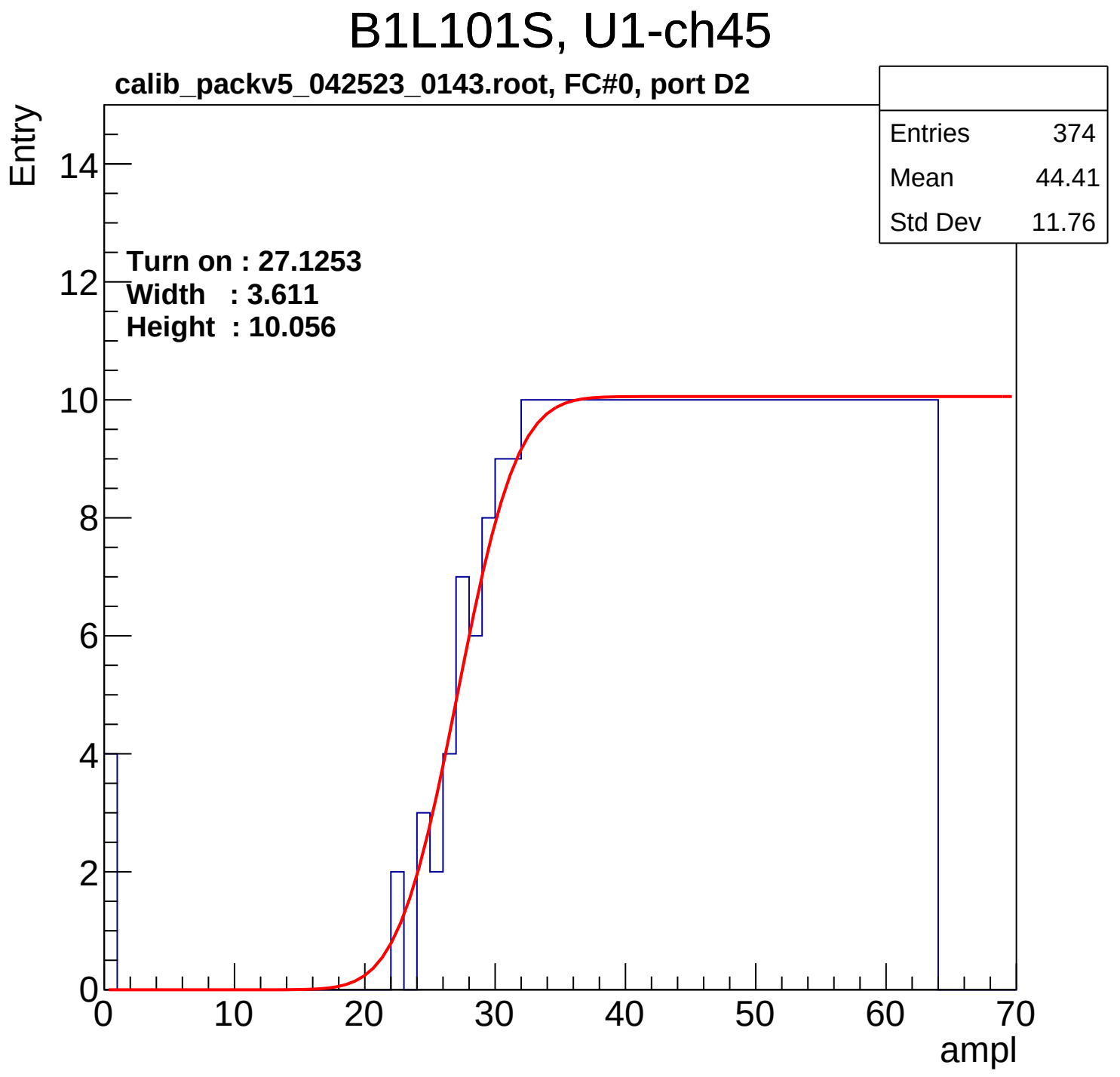
B1L101S, U1-ch45
calib_packv5_042523_0143.root, FC#0, port D2
Entries 374
Mean 44.41
Std Dev 11.76
Turn on : 27.1253
Width : 3.611
Height : 10.056
Entry
ampl
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8
10
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0
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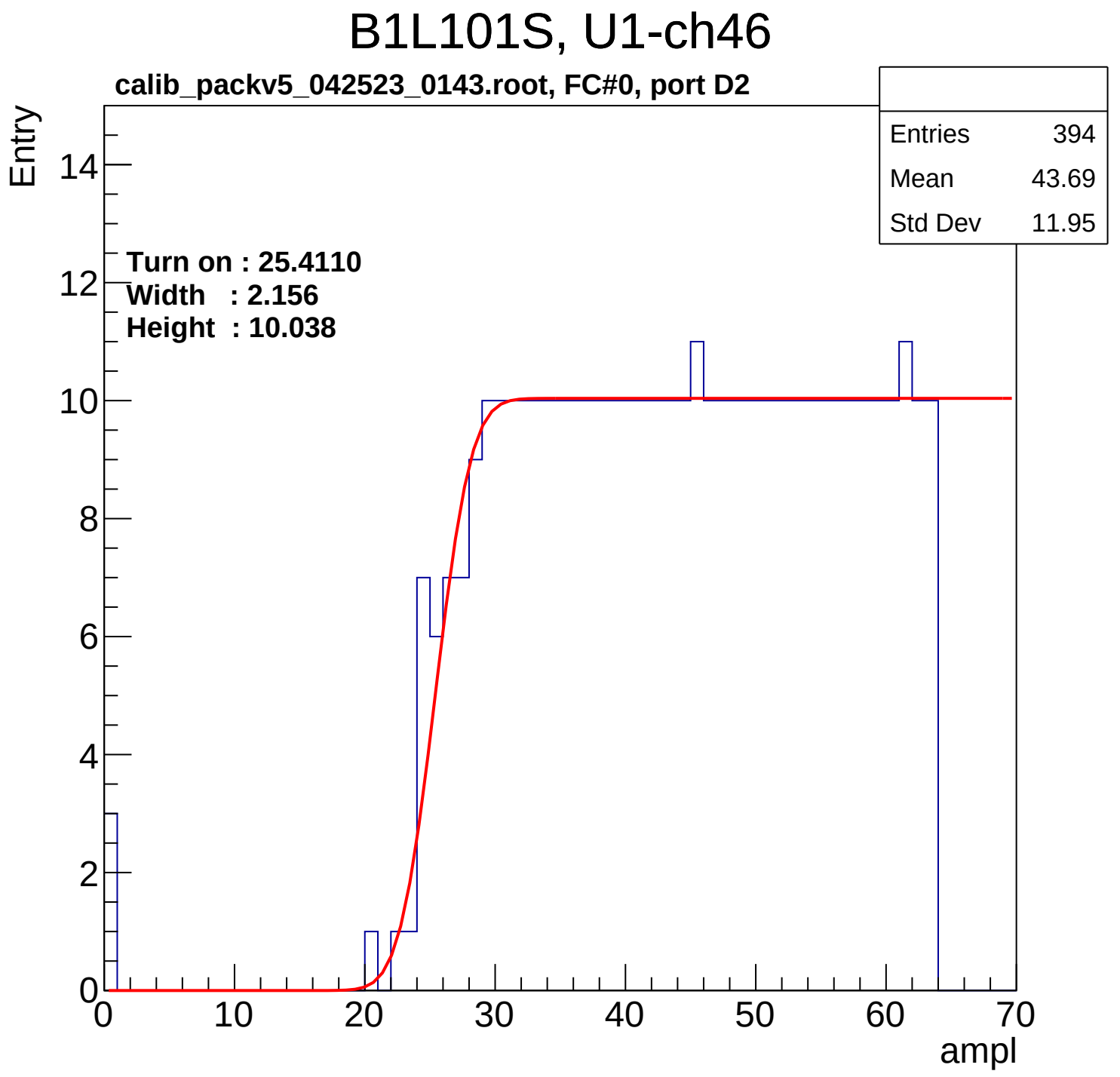
B1L101S, U1-ch46
calib_packv5_042523_0143.root, FC#0, port D2
Entries 394
Mean 43.69
Std Dev 11.95
Turn on : 25.4110
Width : 2.156
Height : 10.038
Entry
ampl
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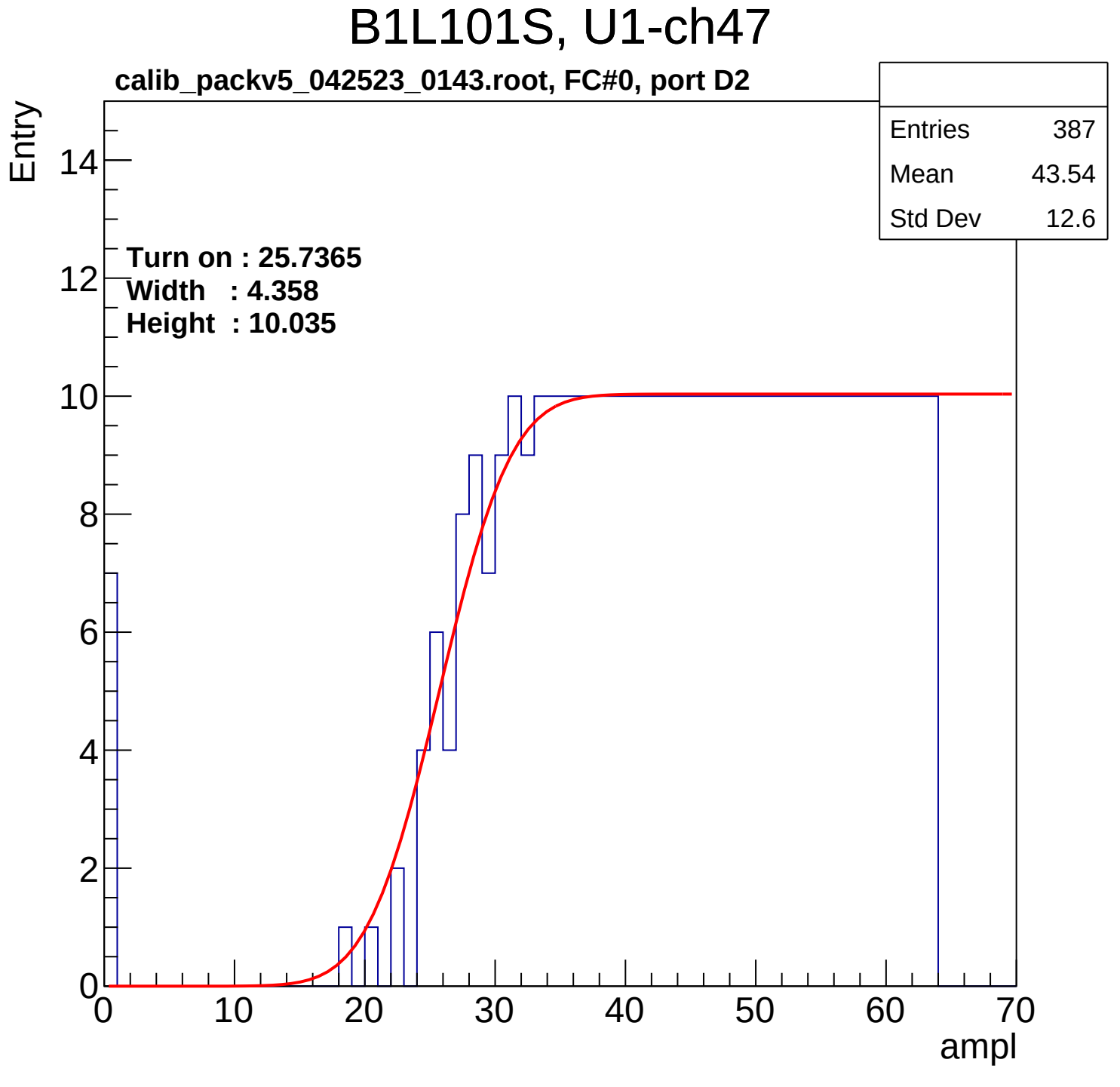
B1L101S, U1-ch47
calib_packv5_042523_0143.root, FC#0, port D2
Entries 387
Mean 43.54
Std Dev 12.6
Turn on : 25.7365
Width : 4.358
Height : 10.035
Entry
ampl
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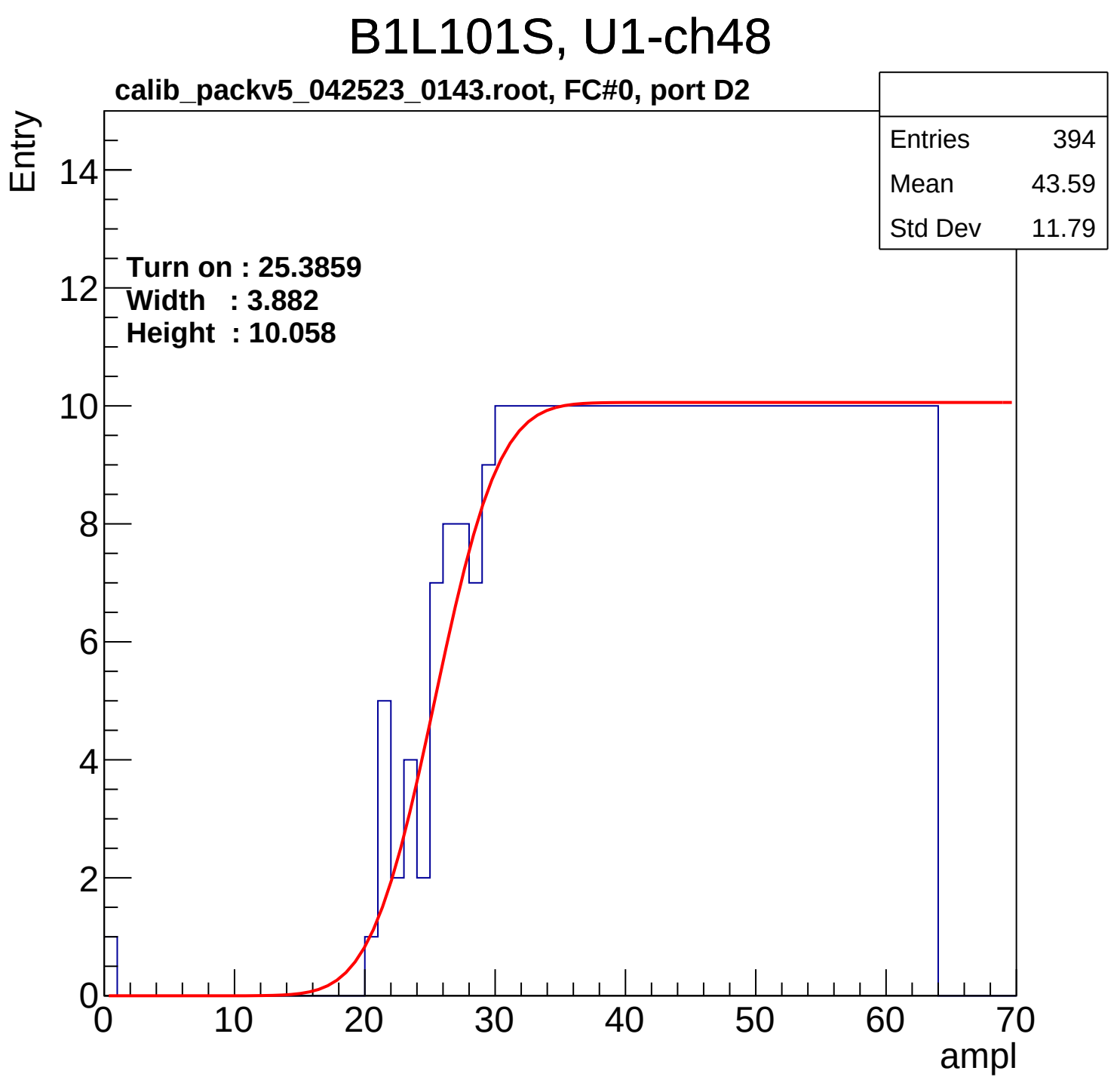
B1L101S, U1-ch48
calib_packv5_042523_0143.root, FC#0, port D2
Entries 394
Mean 43.59
Std Dev 11.79
Turn on : 25.3859
Width : 3.882
Height : 10.058
Entry
ampl
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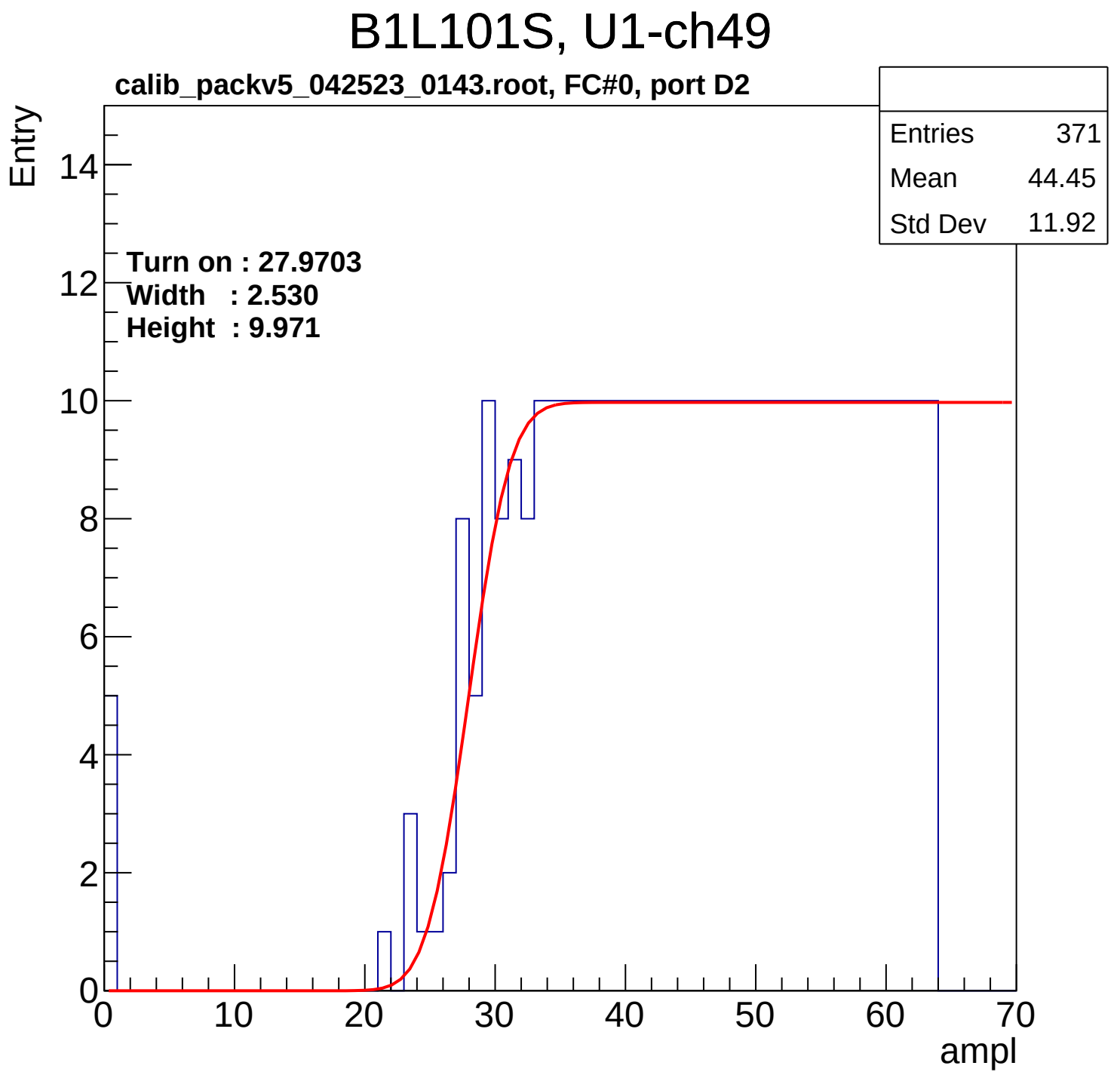
B1L101S, U1-ch49
calib_packv5_042523_0143.root, FC#0, port D2
Entries 371
Mean 44.45
Std Dev 11.92
Turn on : 27.9703
Width : 2.530
Height : 9.971
Entry
ampl
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6
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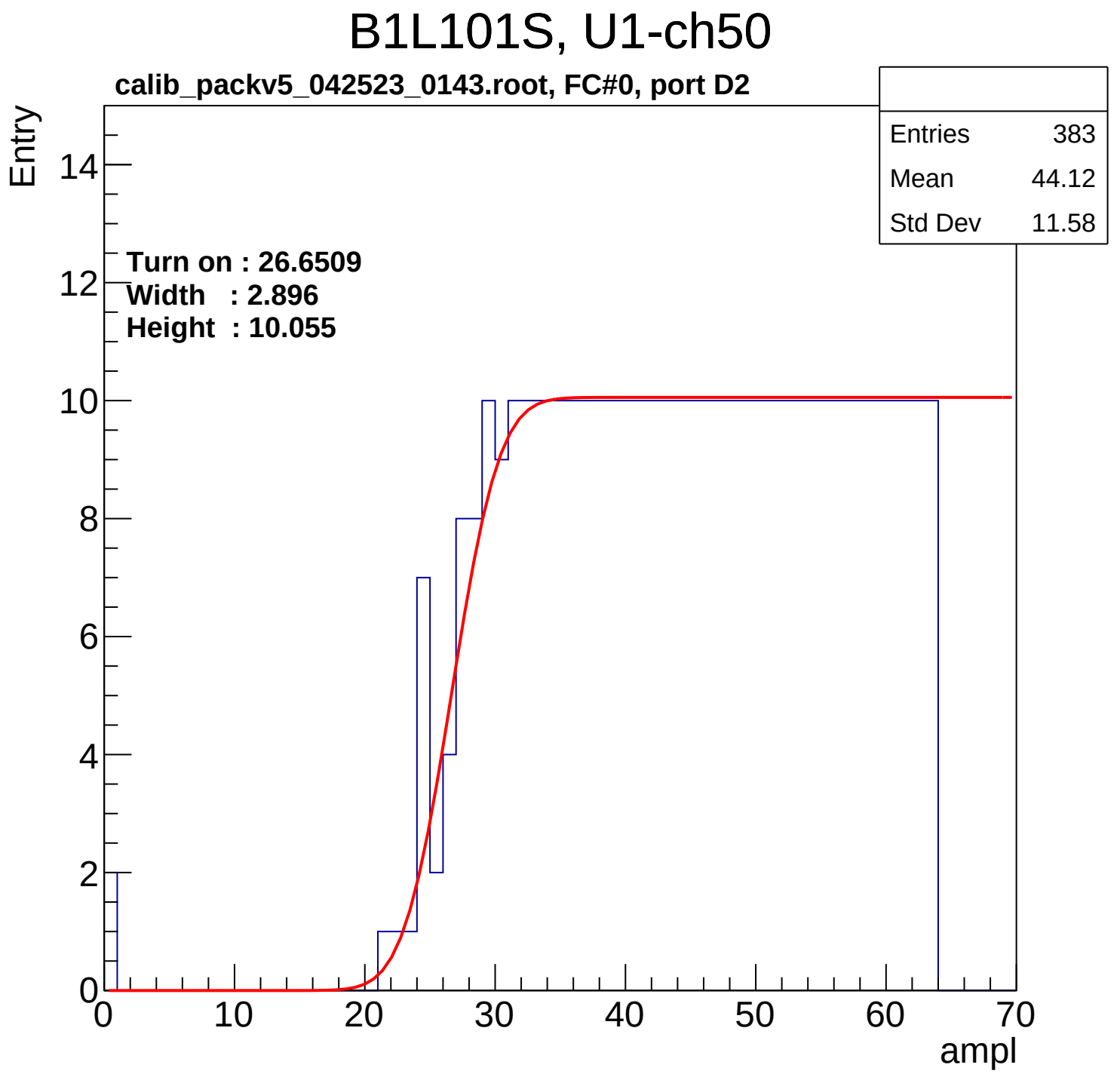
B1L101S, U1-ch50
calib_packv5_042523_0143.root, FC#0, port D2
Entries 383
Mean 44.12
Std Dev 11.58
Turn on : 26.6509
Width : 2.896
Height : 10.055
Entry
ampl
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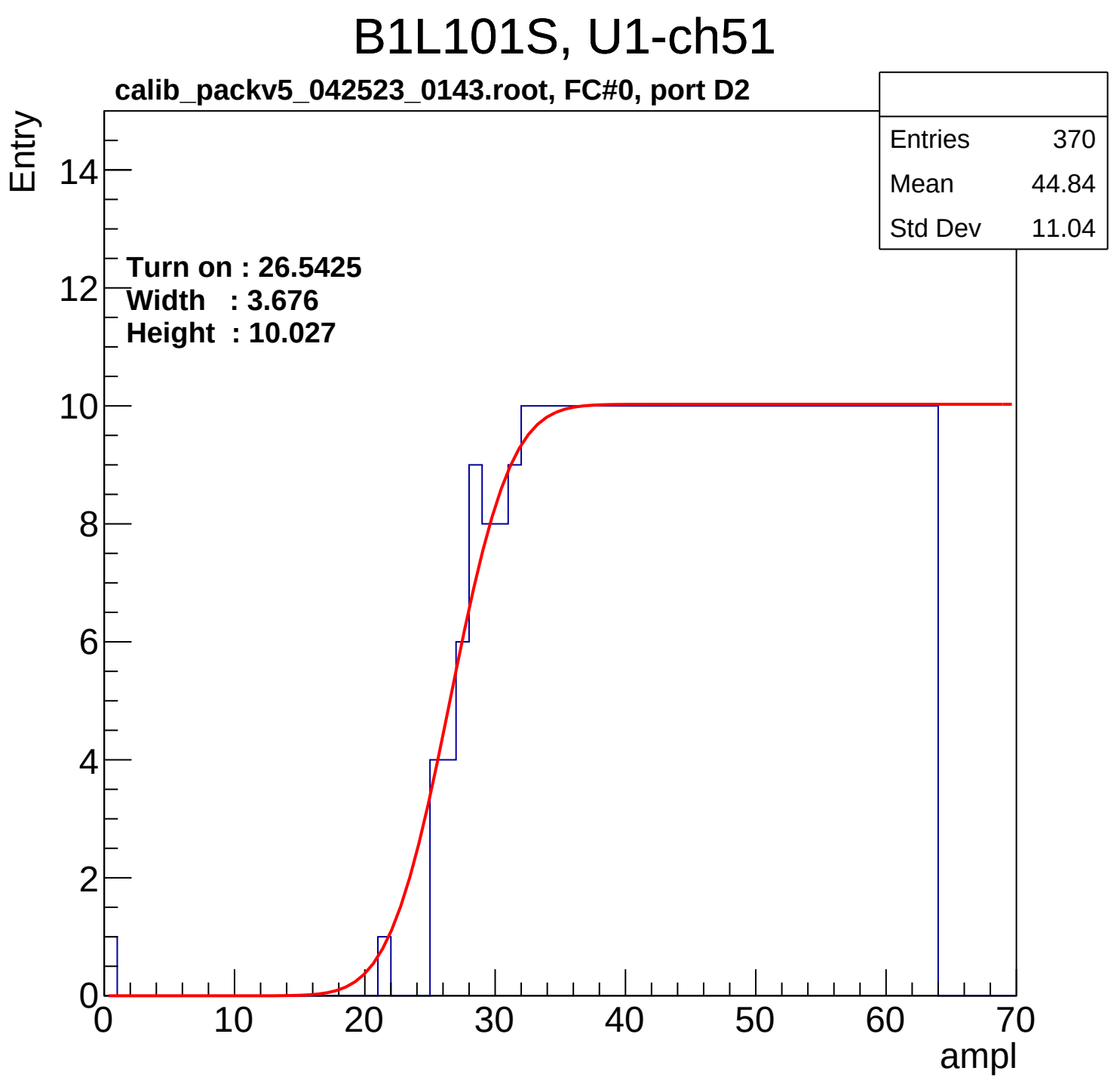
B1L101S, U1-ch51
calib_packv5_042523_0143.root, FC#0, port D2
Entries 370
Mean 44.84
Std Dev 11.04
Turn on : 26.5425
Width : 3.676
Height : 10.027
Entry
ampl
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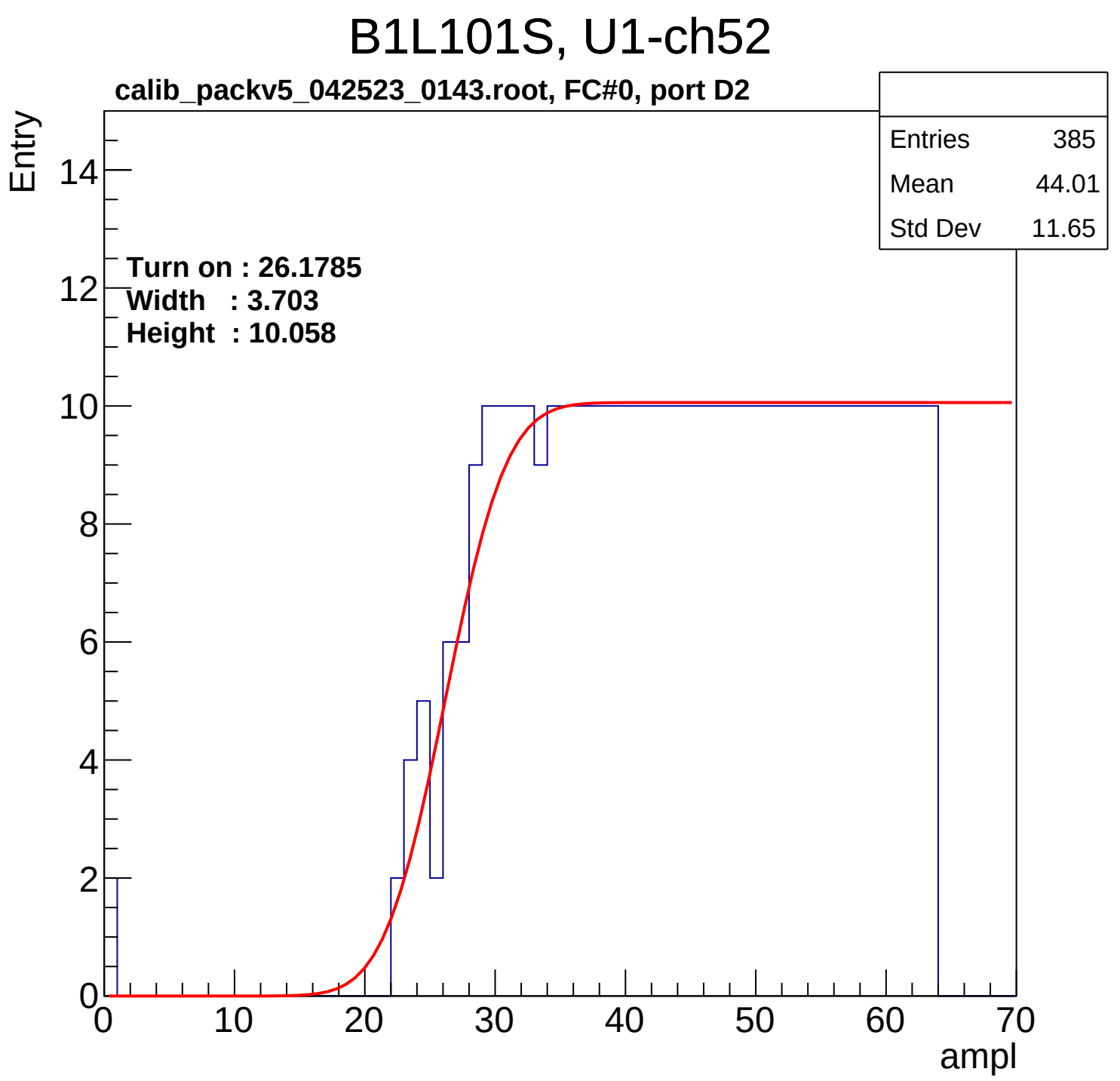
B1L101S, U1-ch52
calib_packv5_042523_0143.root, FC#0, port D2
Entries 385
Mean 44.01
Std Dev 11.65
Turn on : 26.1785
Width : 3.703
Height : 10.058
Entry
ampl
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8
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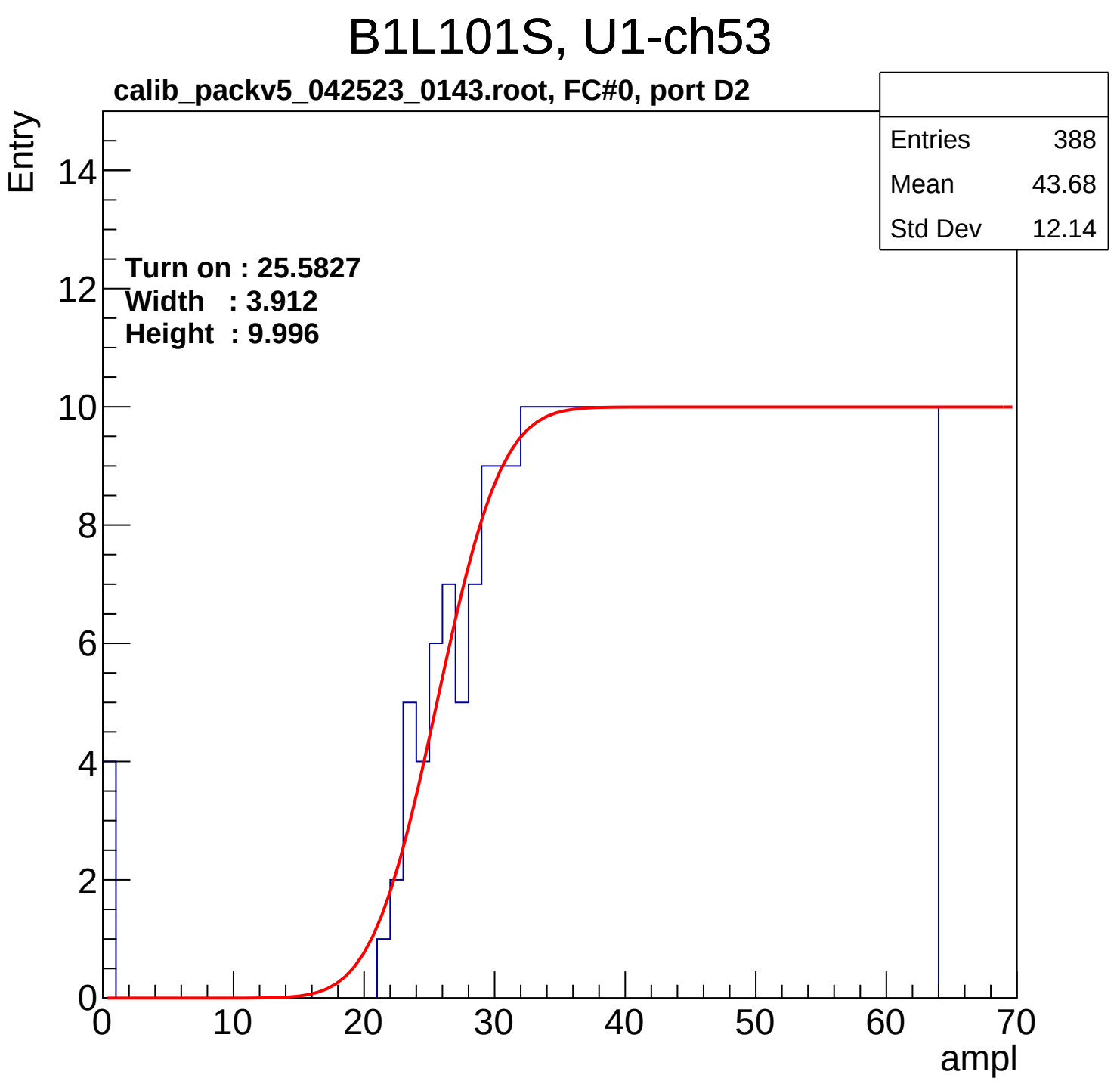
B1L101S, U1-ch53
calib_packv5_042523_0143.root, FC#0, port D2
Entries 388
Mean 43.68
Std Dev 12.14
Turn on : 25.5827
Width : 3.912
Height : 9.996
Entry
ampl
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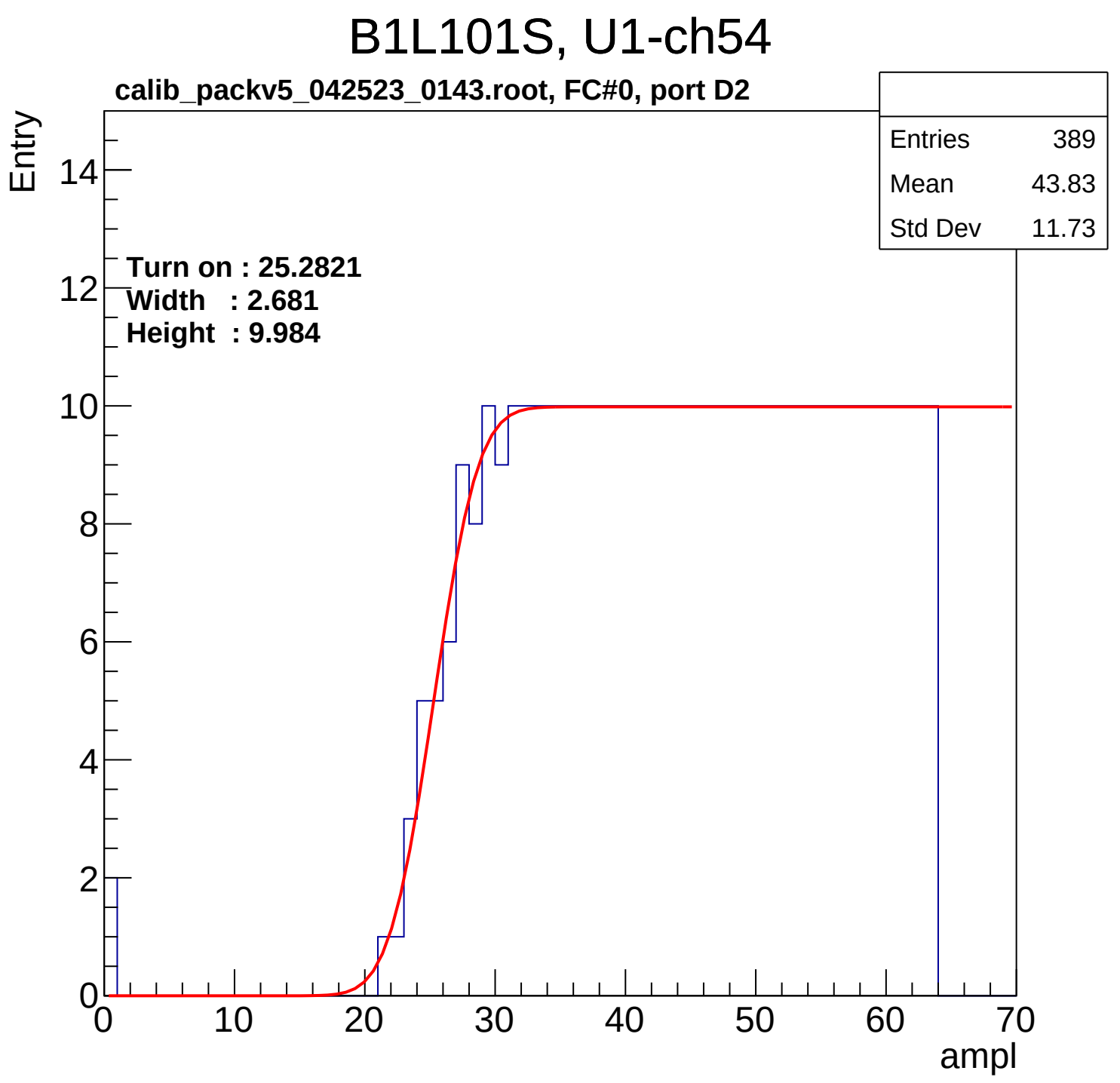
B1L101S, U1-ch54
calib_packv5_042523_0143.root, FC#0, port D2
Entries 389
Mean 43.83
Std Dev 11.73
Turn on : 25.2821
Width : 2.681
Height : 9.984
Entry
ampl
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2
4
6
8
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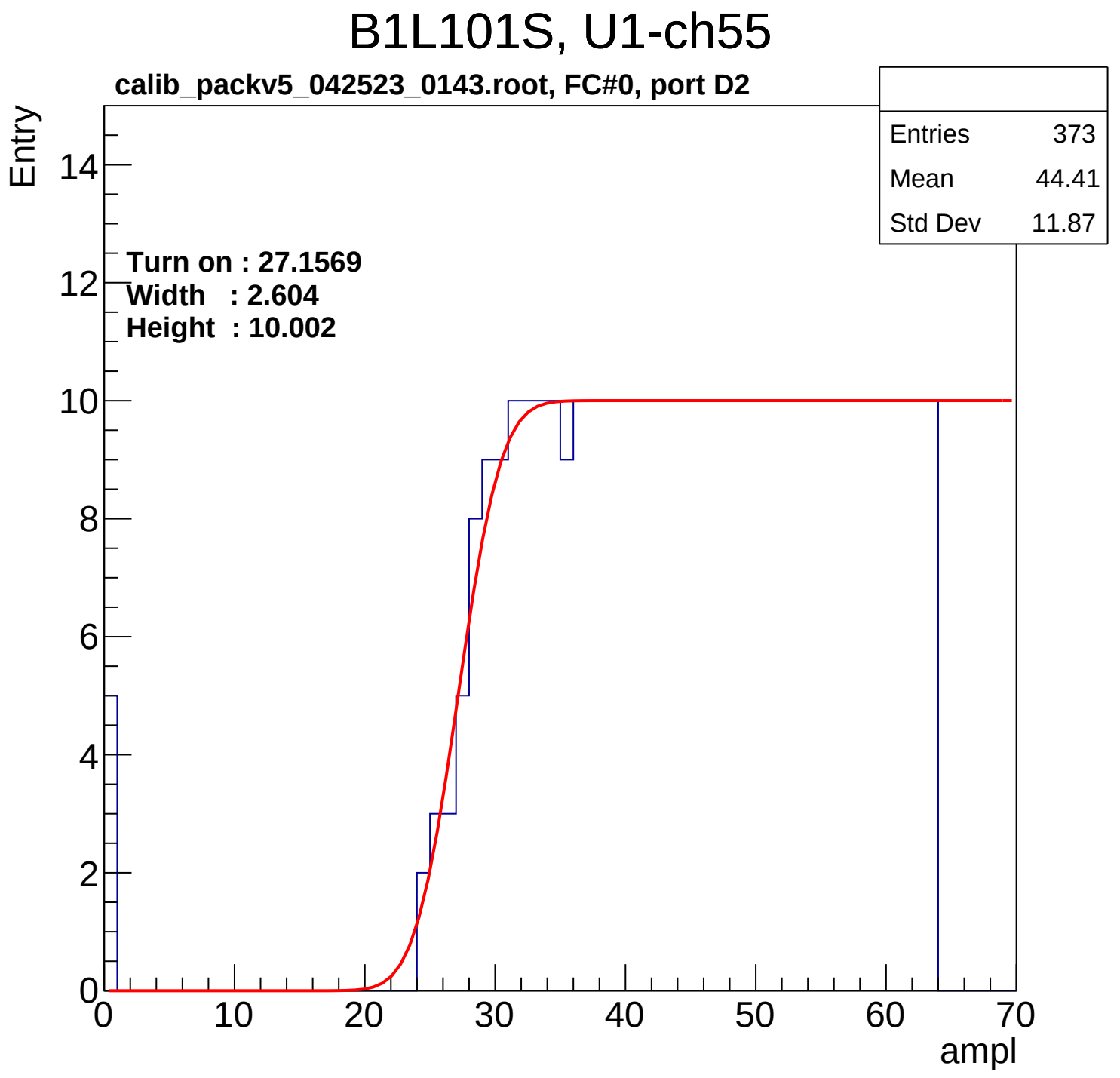
B1L101S, U1-ch55
calib_packv5_042523_0143.root, FC#0, port D2
Entries 373
Mean 44.41
Std Dev 11.87
Turn on : 27.1569
Width : 2.604
Height : 10.002
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ampl
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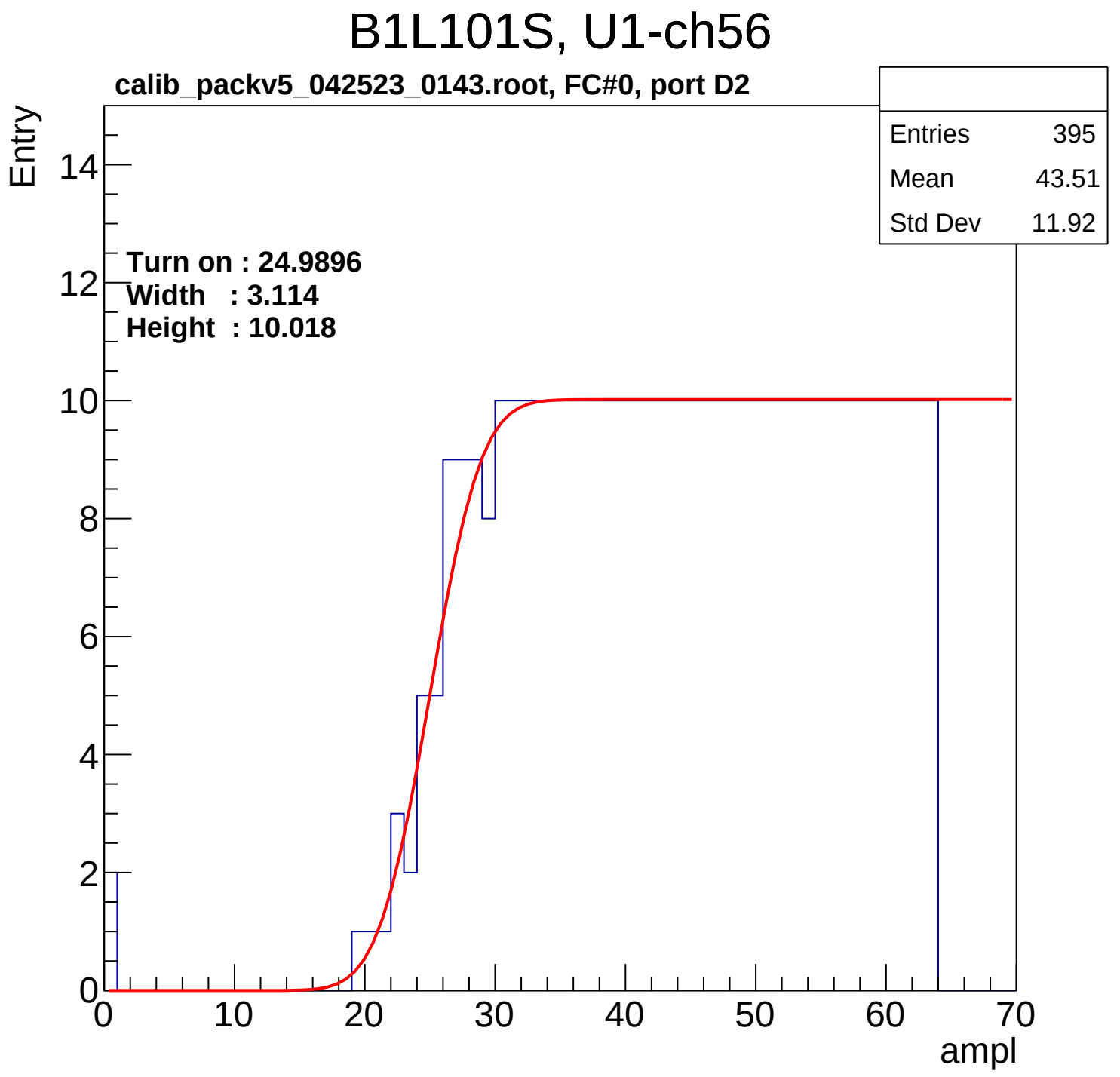
B1L101S, U1-ch56
calib_packv5_042523_0143.root, FC#0, port D2
Entries 395
Mean 43.51
Std Dev 11.92
Turn on : 24.9896
Width : 3.114
Height : 10.018
Entry
ampl
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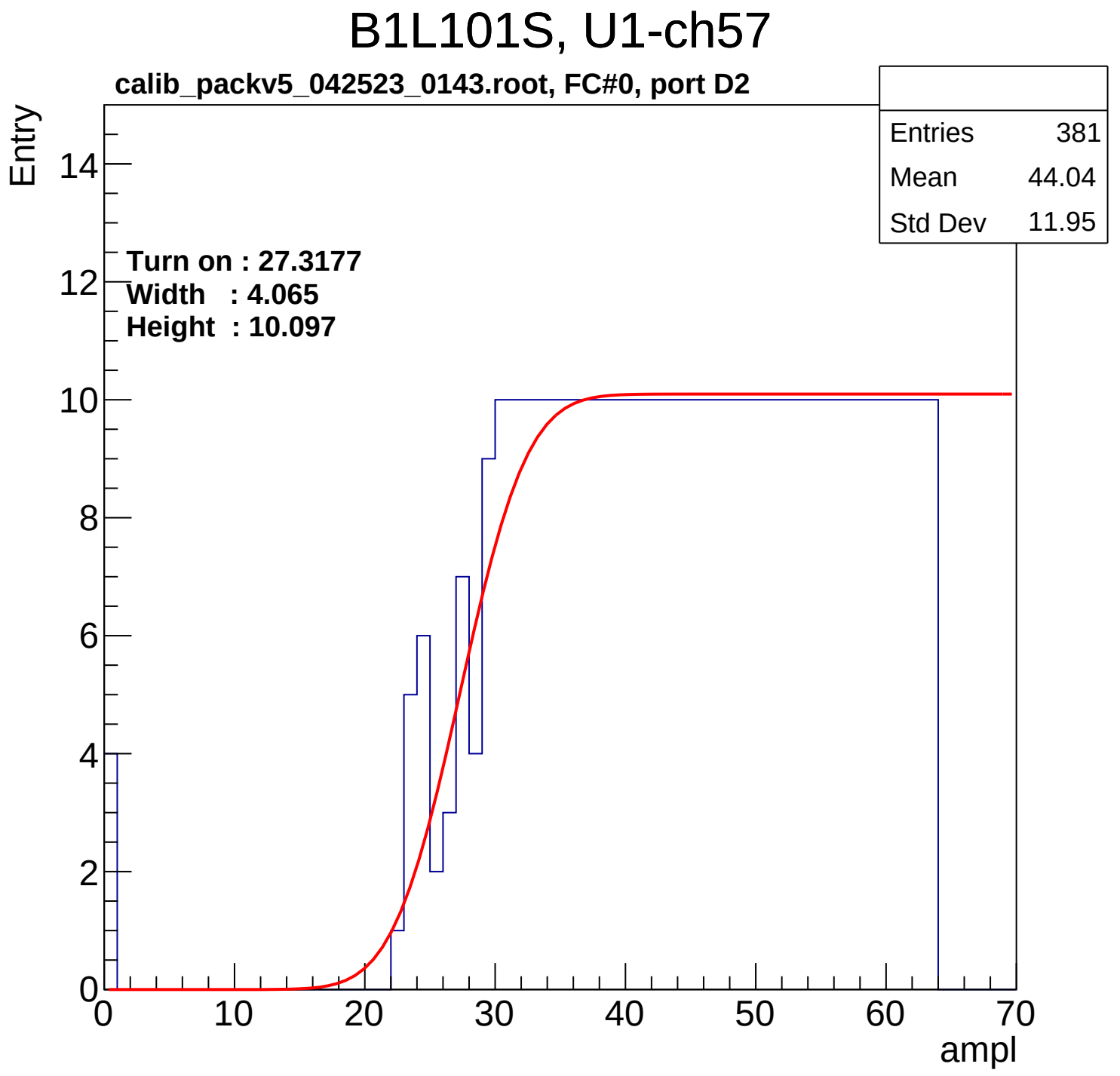
B1L101S, U1-ch57
calib_packv5_042523_0143.root, FC#0, port D2
Entries 381
Mean 44.04
Std Dev 11.95
Turn on : 27.3177
Width : 4.065
Height : 10.097
Entry
ampl
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4
6
8
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12
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10
20
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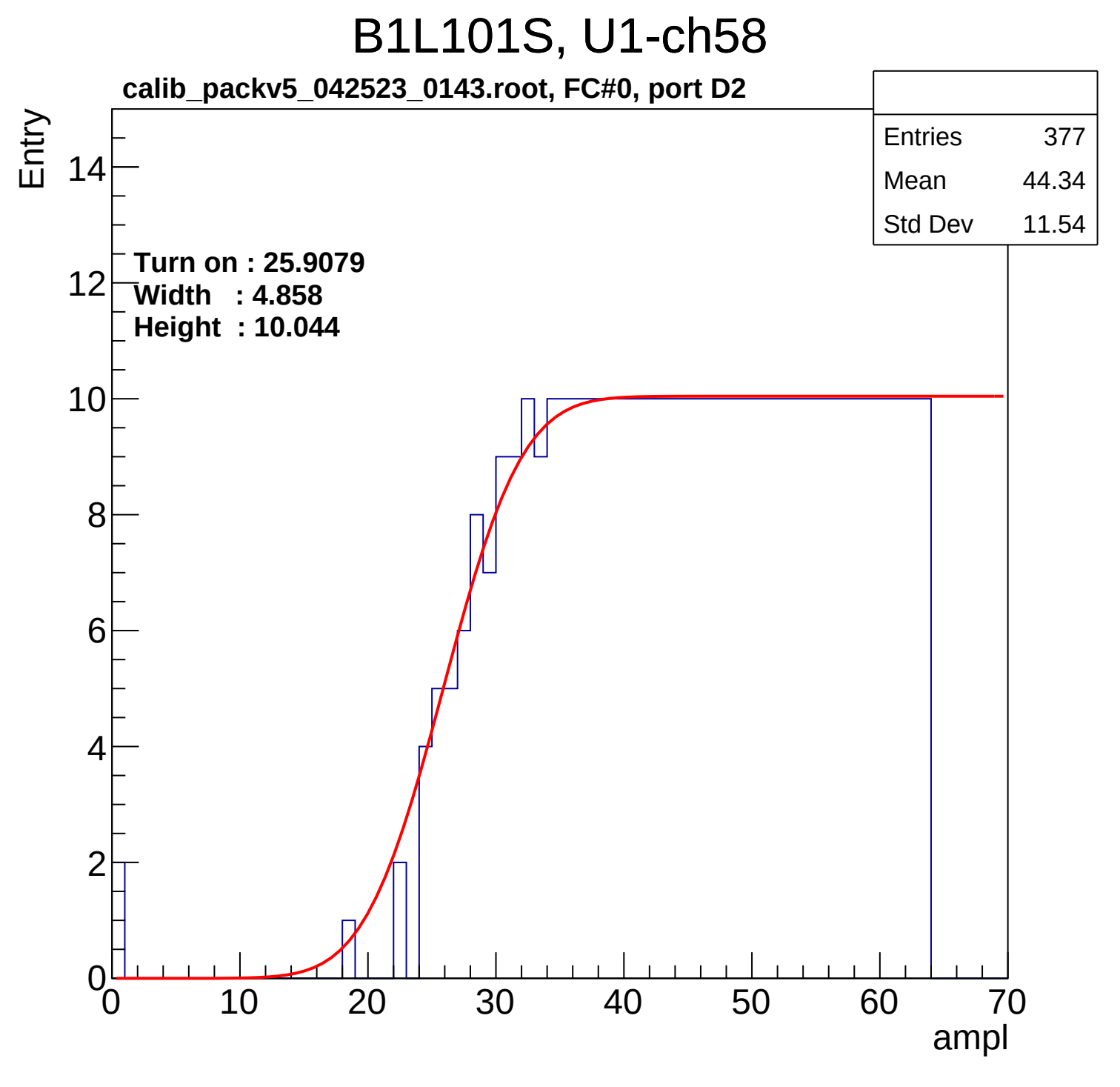
B1L101S, U1-ch58
calib_packv5_042523_0143.root, FC#0, port D2
Entries 377
Mean 44.34
Std Dev 11.54
Turn on : 25.9079
Width : 4.858
Height : 10.044
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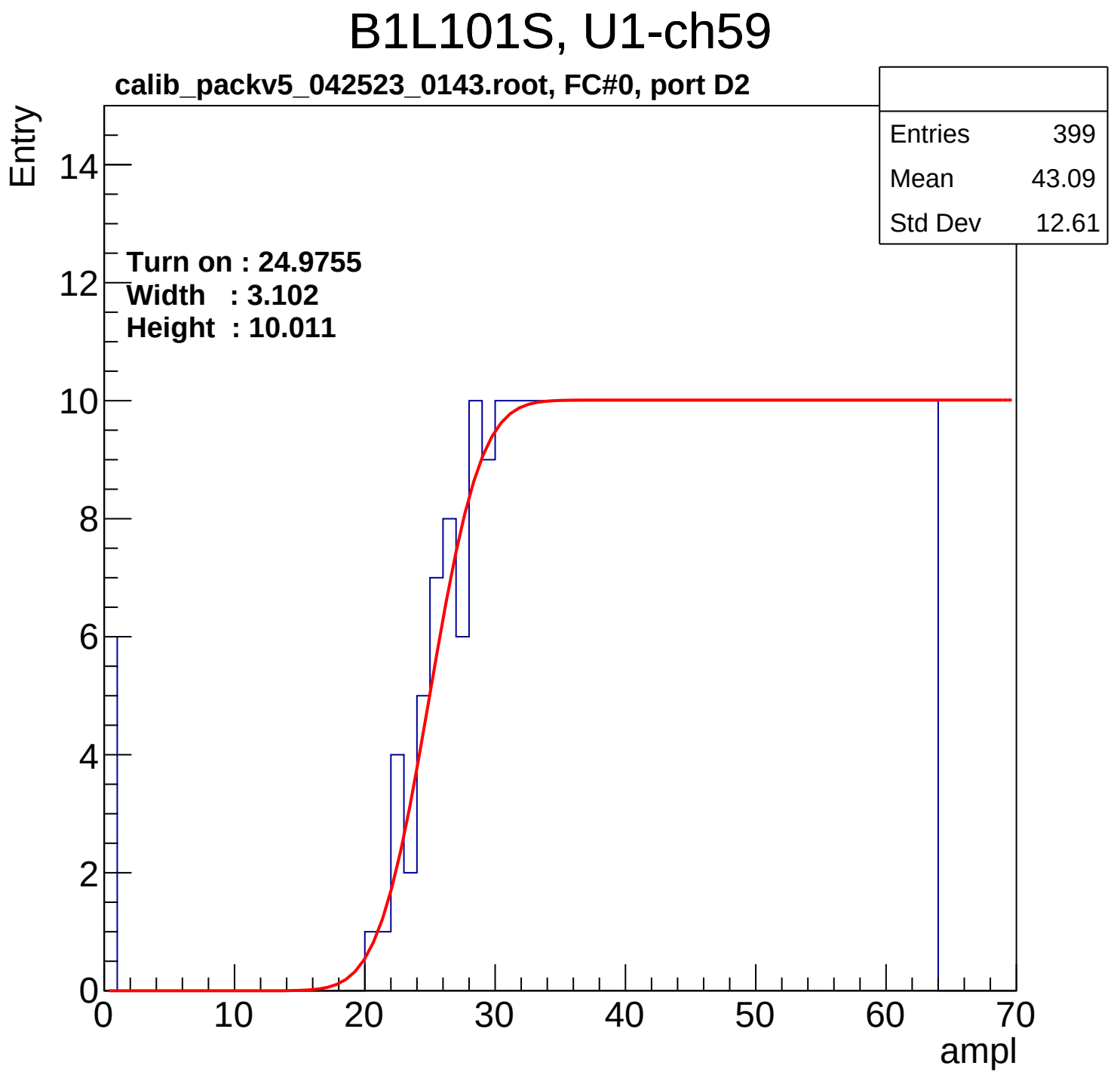
B1L101S, U1-ch59
calib_packv5_042523_0143.root, FC#0, port D2
Entries 399
Mean 43.09
Std Dev 12.61
Turn on : 24.9755
Width : 3.102
Height : 10.011
Entry
ampl
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4
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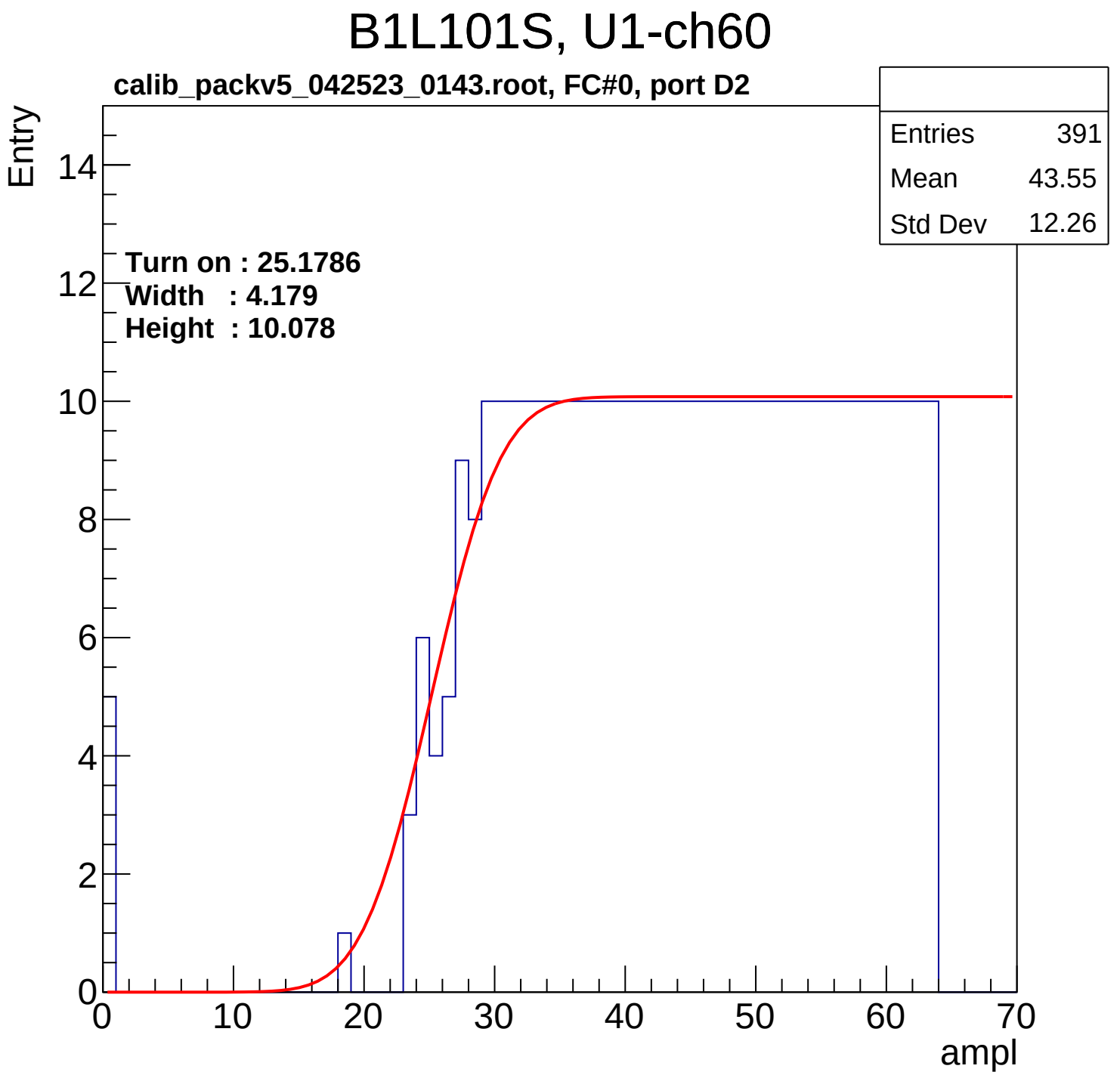
B1L101S, U1-ch60
calib_packv5_042523_0143.root, FC#0, port D2
Entries 391
Mean 43.55
Std Dev 12.26
Turn on : 25.1786
Width : 4.179
Height : 10.078
Entry
ampl
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2
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6
8
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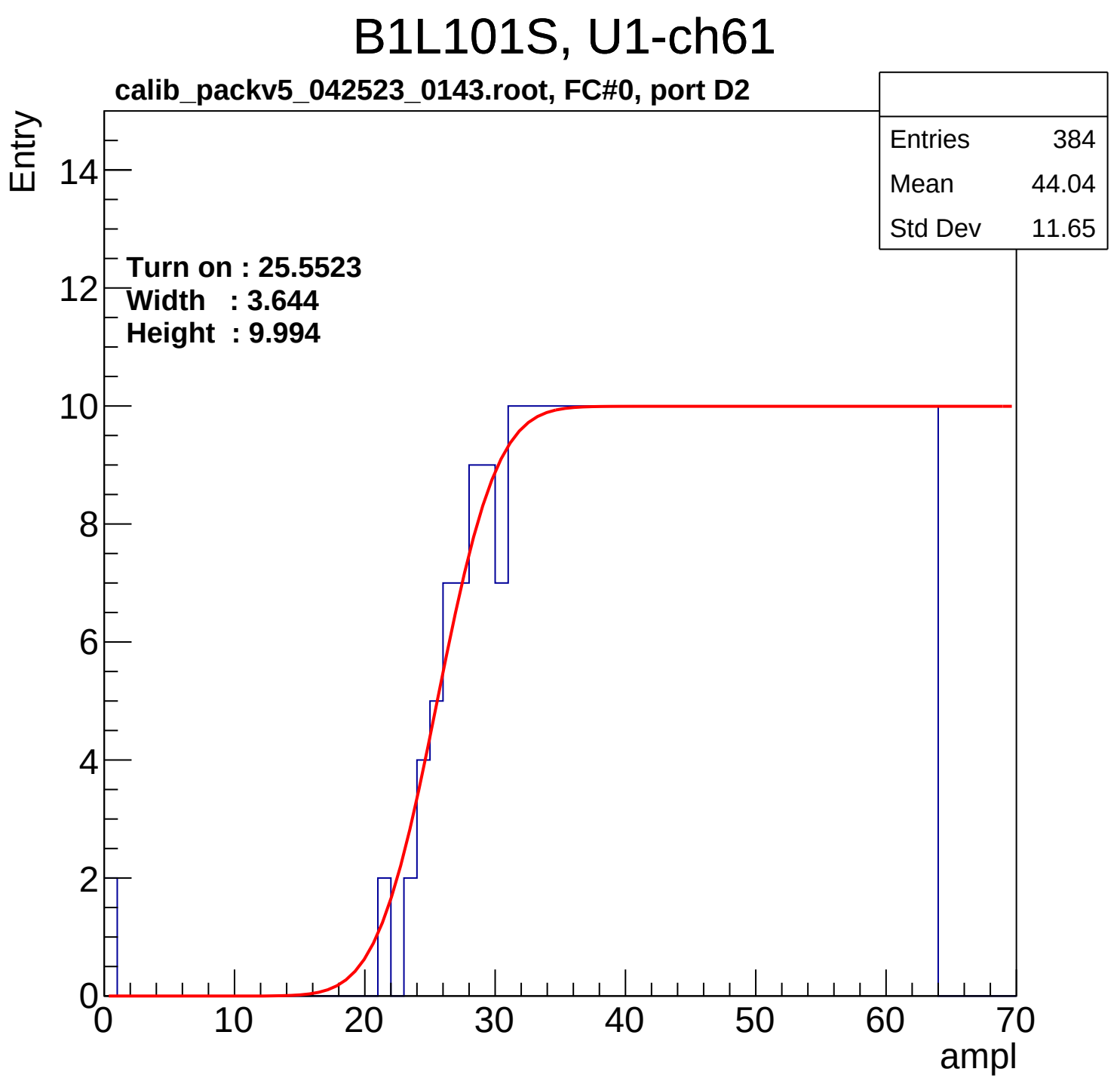
B1L101S, U1-ch61
calib_packv5_042523_0143.root, FC#0, port D2
Entries 384
Mean 44.04
Std Dev 11.65
Turn on : 25.5523
Width : 3.644
Height : 9.994
Entry
ampl
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8
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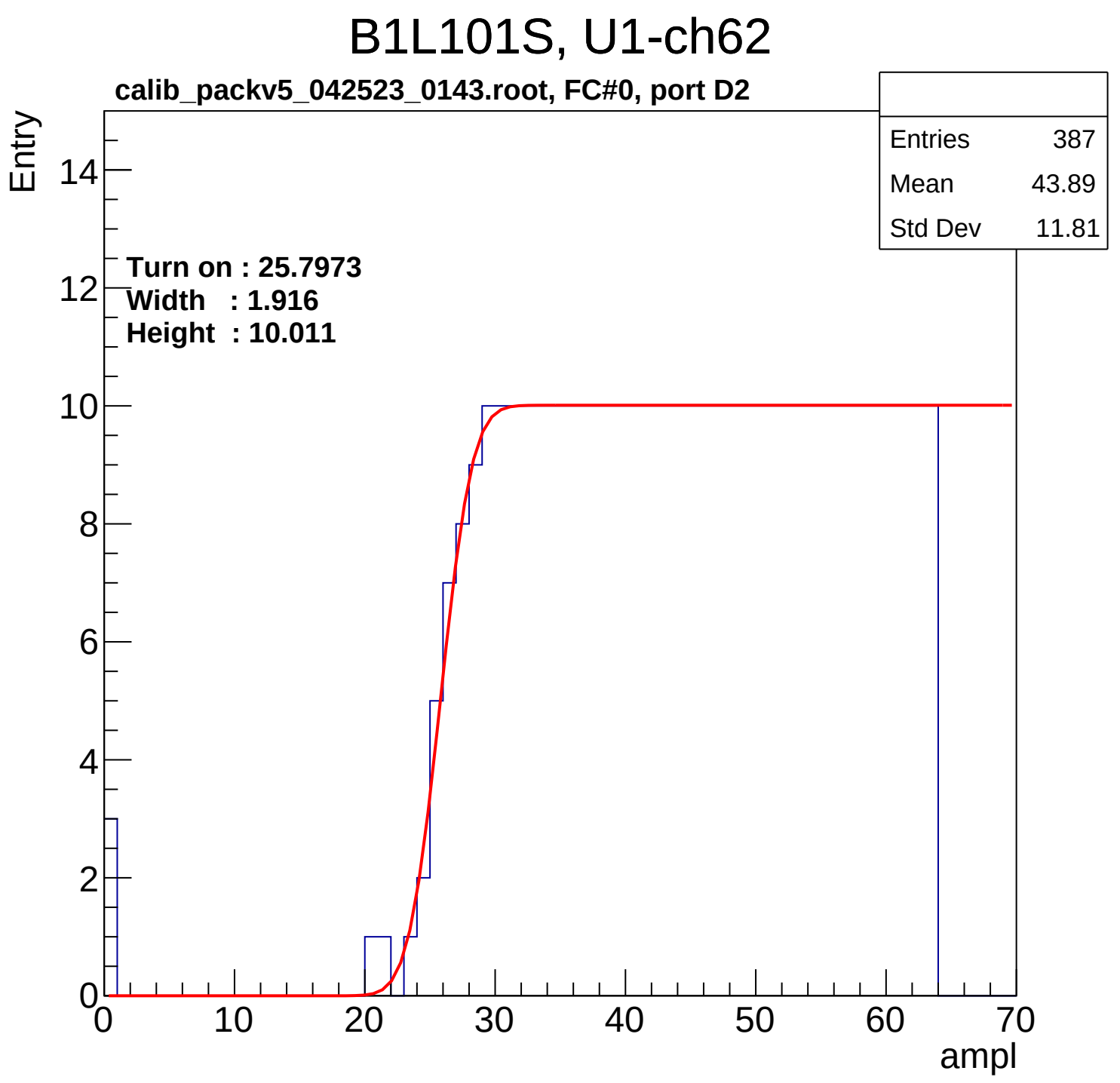
B1L101S, U1-ch62
calib_packv5_042523_0143.root, FC#0, port D2
Entries 387
Mean 43.89
Std Dev 11.81
Turn on : 25.7973
Width : 1.916
Height : 10.011
Entry
ampl
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2
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6
8
10
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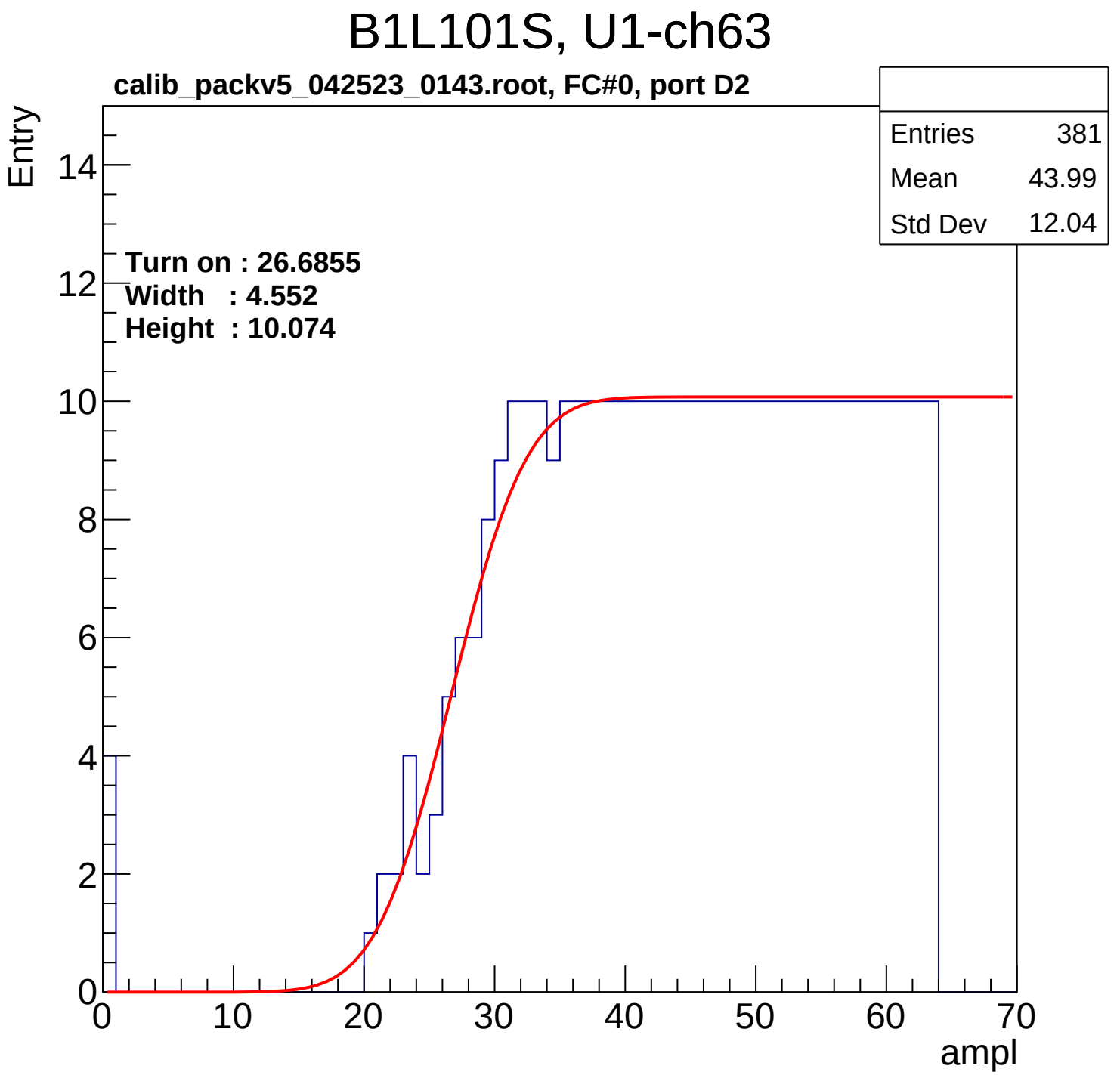
B1L101S, U1-ch63
calib_packv5_042523_0143.root, FC#0, port D2
Entries 381
Mean 43.99
Std Dev 12.04
Turn on : 26.6855
Width : 4.552
Height : 10.074
Entry
ampl
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4
6
8
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0
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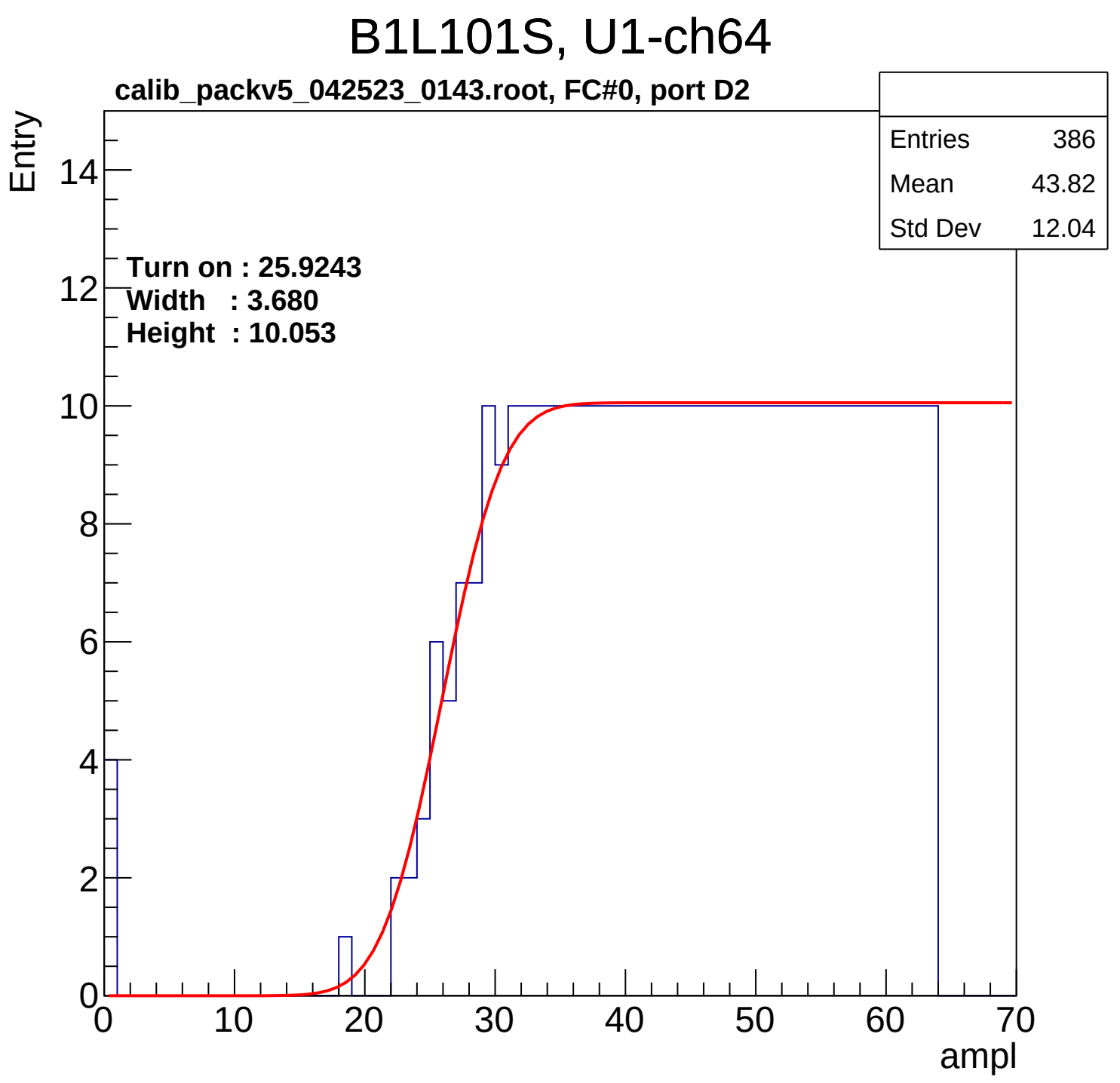
B1L101S, U1-ch64
calib_packv5_042523_0143.root, FC#0, port D2
Entries 386
Mean 43.82
Std Dev 12.04
Turn on : 25.9243
Width : 3.680
Height : 10.053
Entry
ampl
0
2
4
6
8
10
12
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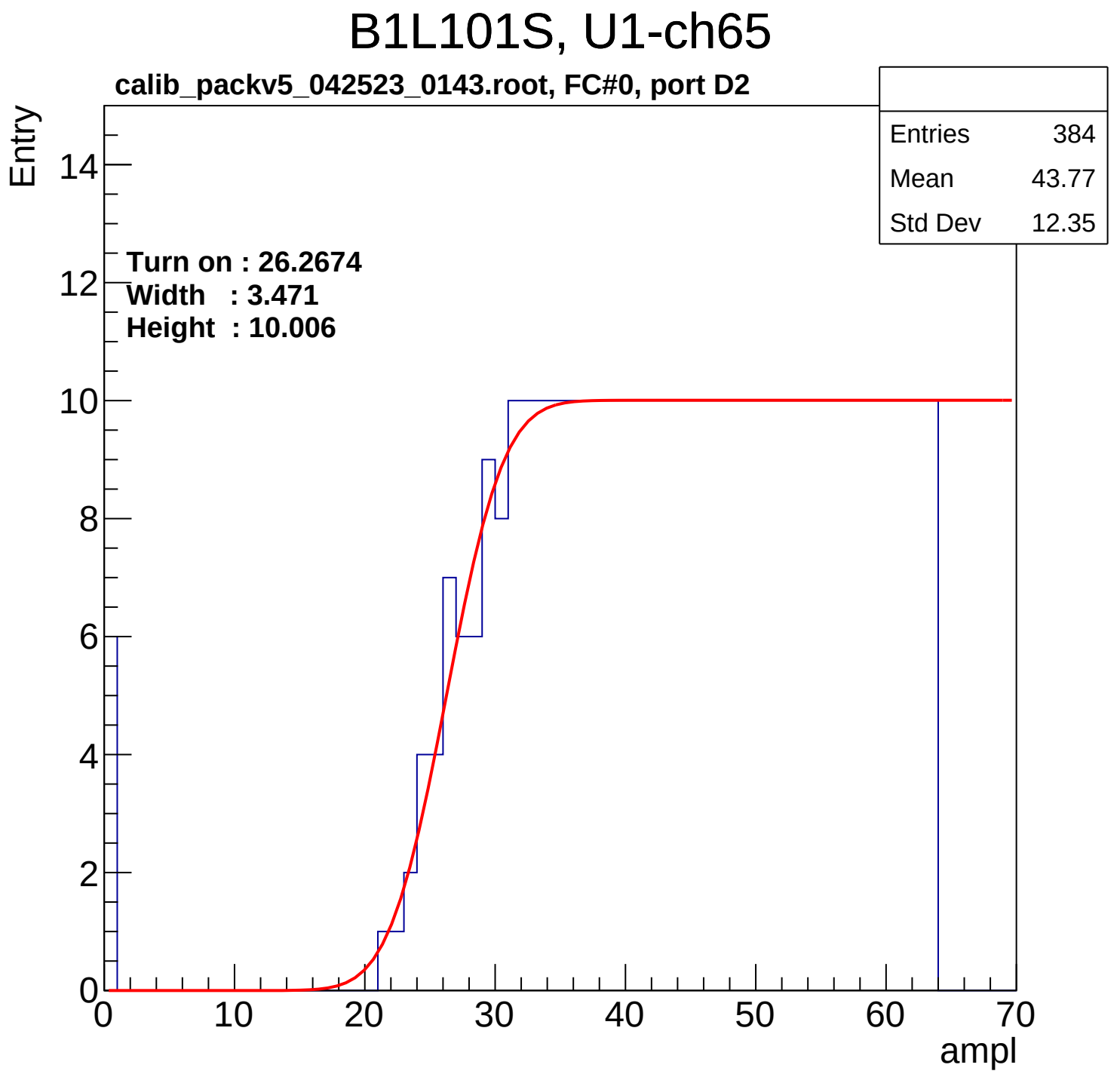
B1L101S, U1-ch65
calib_packv5_042523_0143.root, FC#0, port D2
Entries 384
Mean 43.77
Std Dev 12.35
Turn on : 26.2674
Width : 3.471
Height : 10.006
Entry
ampl
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4
6
8
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60
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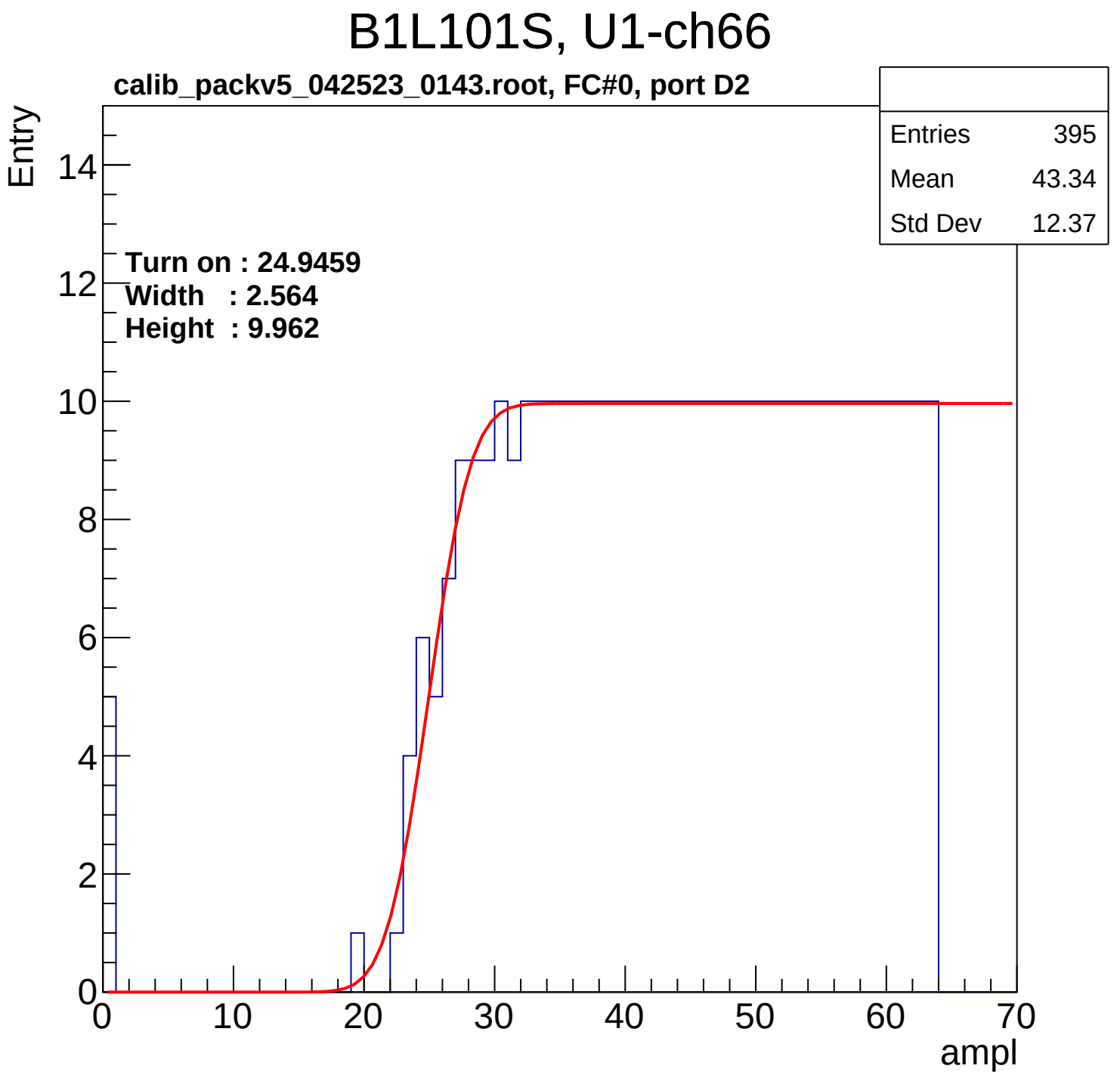
B1L101S, U1-ch66
calib_packv5_042523_0143.root, FC#0, port D2
Entries 395
Mean 43.34
Std Dev 12.37
Turn on : 24.9459
Width : 2.564
Height : 9.962
Entry
ampl
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6
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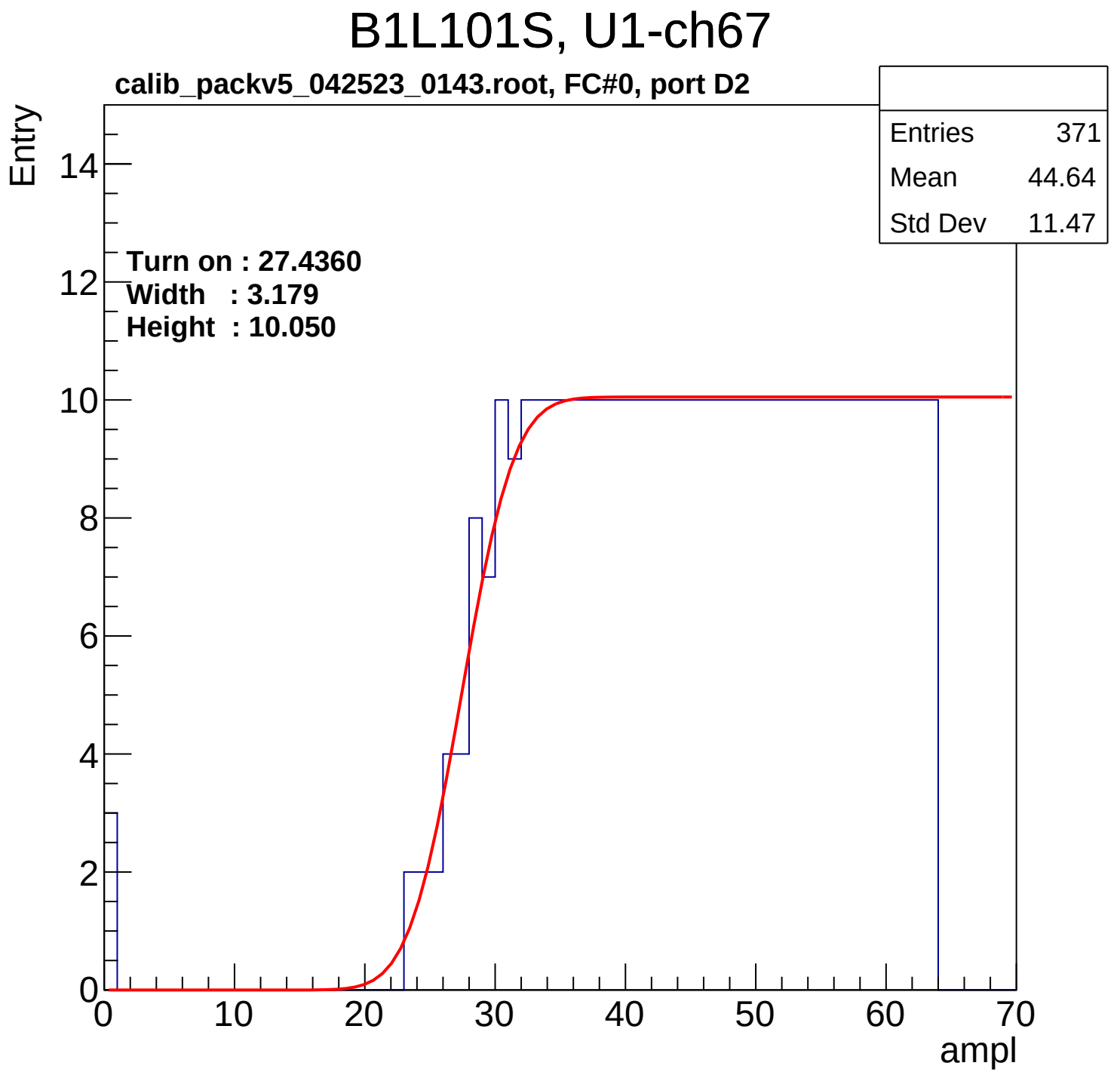
B1L101S, U1-ch67
calib_packv5_042523_0143.root, FC#0, port D2
Entries 371
Mean 44.64
Std Dev 11.47
Turn on : 27.4360
Width : 3.179
Height : 10.050
Entry
ampl
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8
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60
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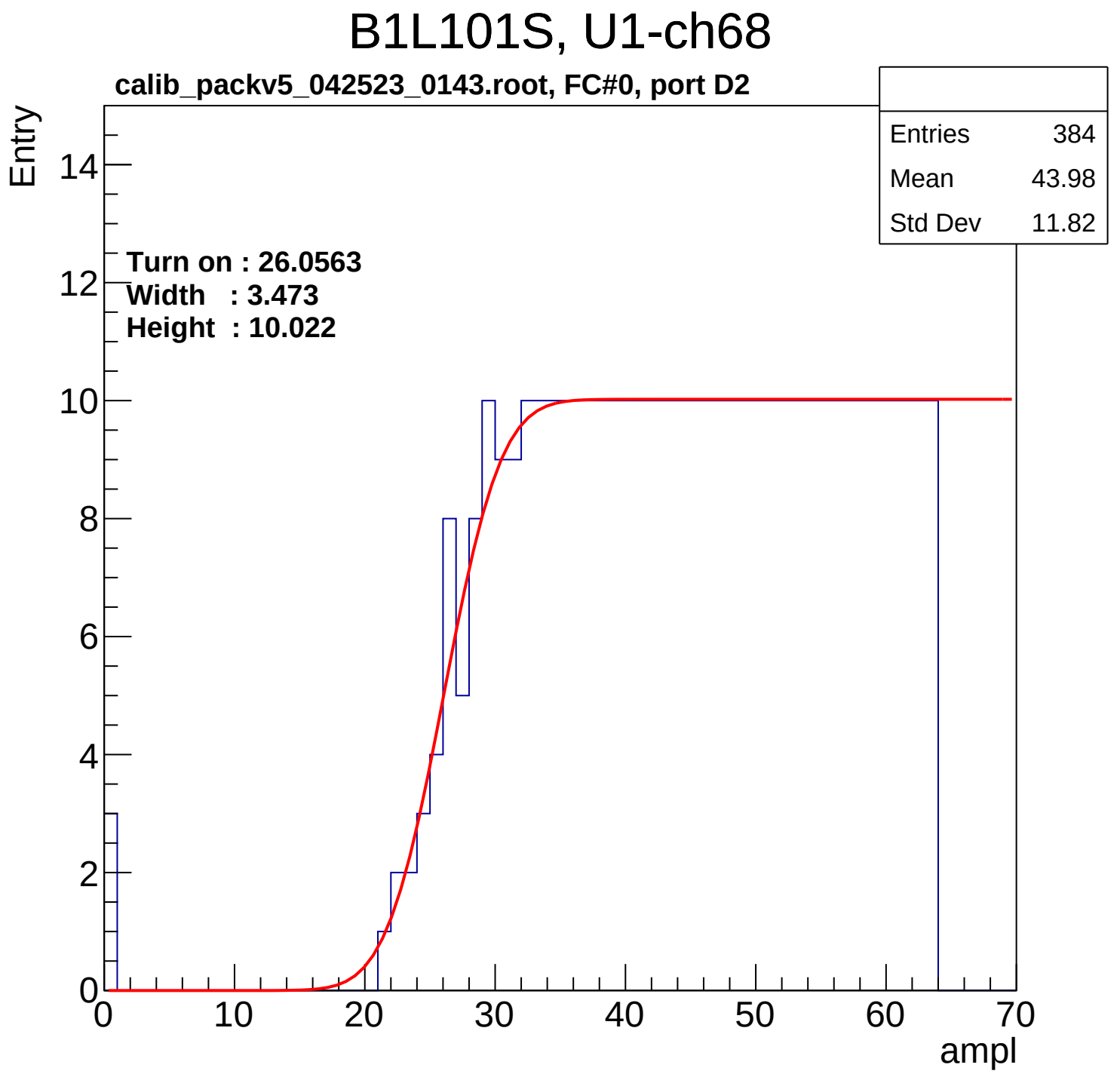
B1L101S, U1-ch68
calib_packv5_042523_0143.root, FC#0, port D2
Entries 384
Mean 43.98
Std Dev 11.82
Turn on : 26.0563
Width : 3.473
Height : 10.022
Entry
ampl
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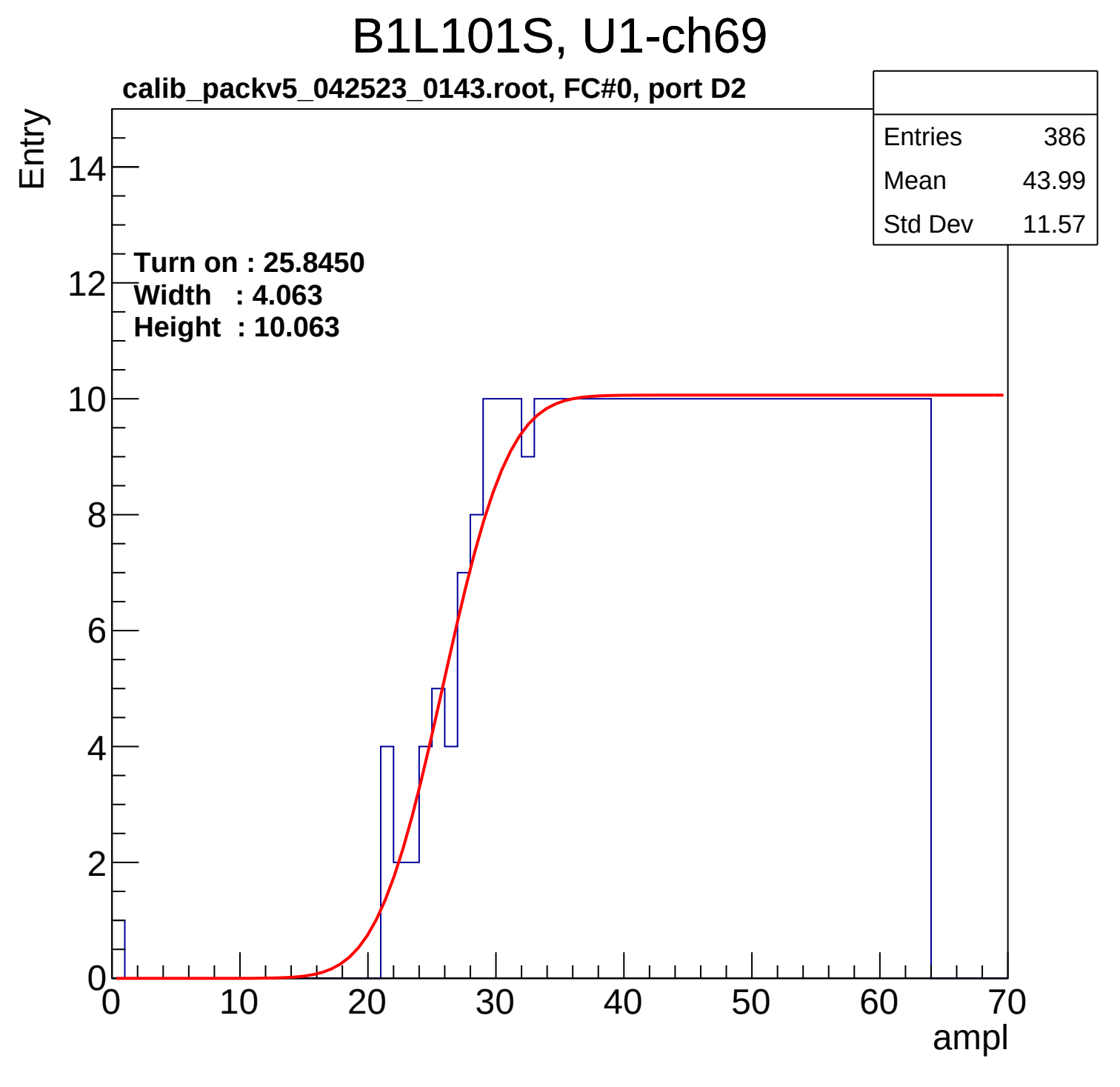
B1L101S, U1-ch69
calib_packv5_042523_0143.root, FC#0, port D2
Entries 386
Mean 43.99
Std Dev 11.57
Turn on : 25.8450
Width : 4.063
Height : 10.063
Entry
ampl
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2
4
6
8
10
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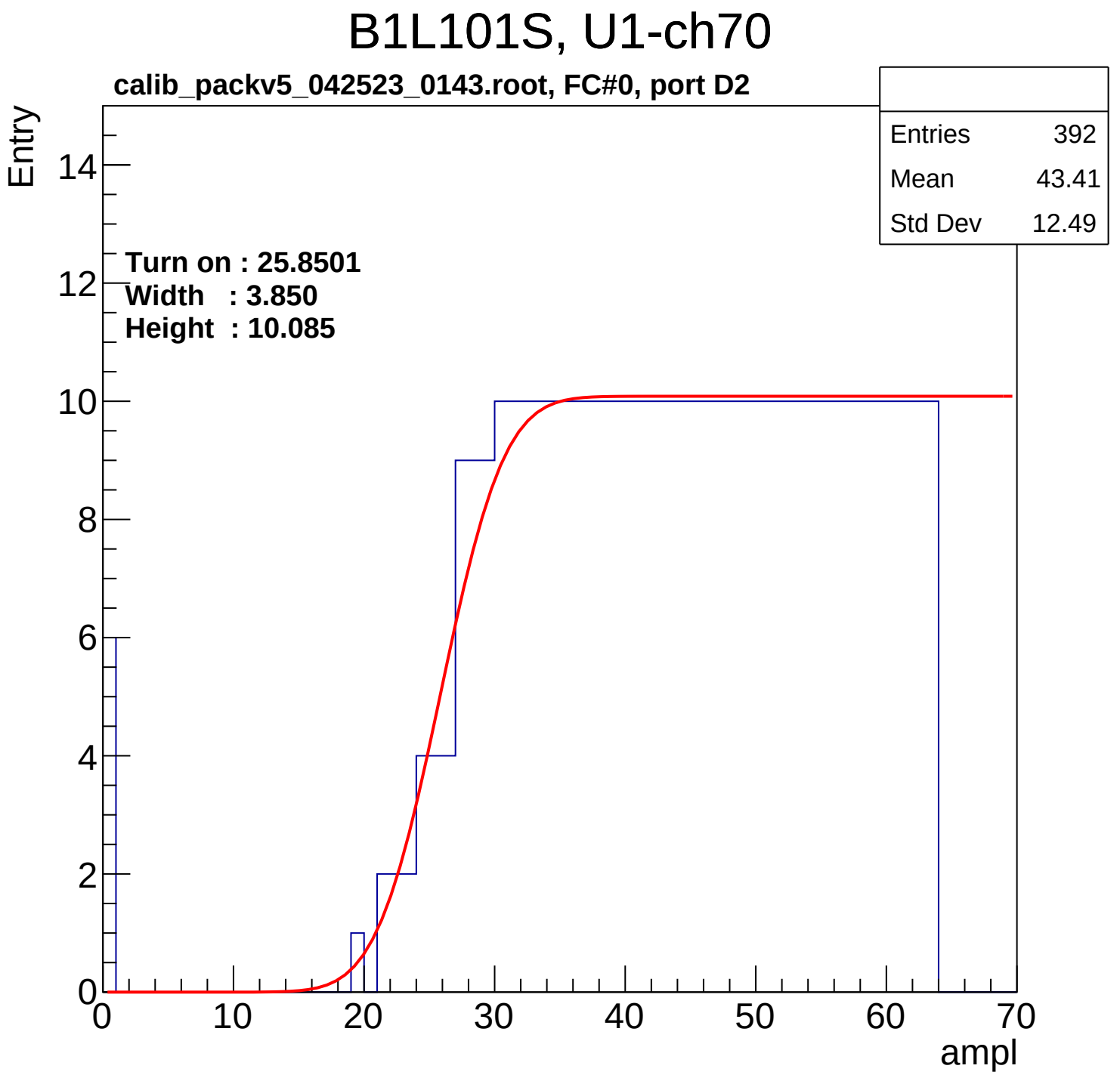
B1L101S, U1-ch70
calib_packv5_042523_0143.root, FC#0, port D2
Entries 392
Mean 43.41
Std Dev 12.49
Turn on : 25.8501
Width : 3.850
Height : 10.085
Entry
ampl
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8
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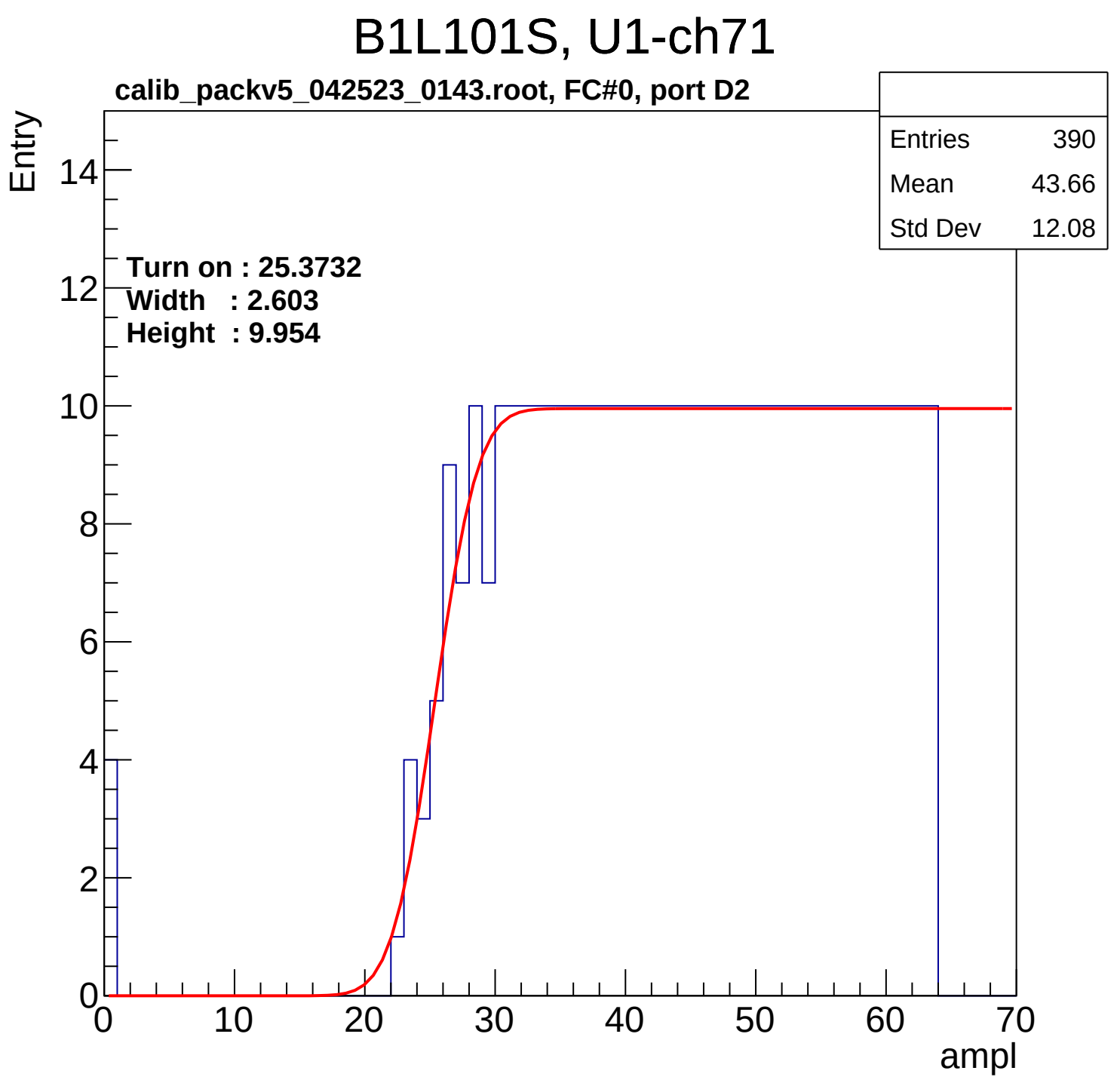
B1L101S, U1-ch71
calib_packv5_042523_0143.root, FC#0, port D2
Entries 390
Mean 43.66
Std Dev 12.08
Turn on : 25.3732
Width : 2.603
Height : 9.954
Entry
ampl
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2
4
6
8
10
12
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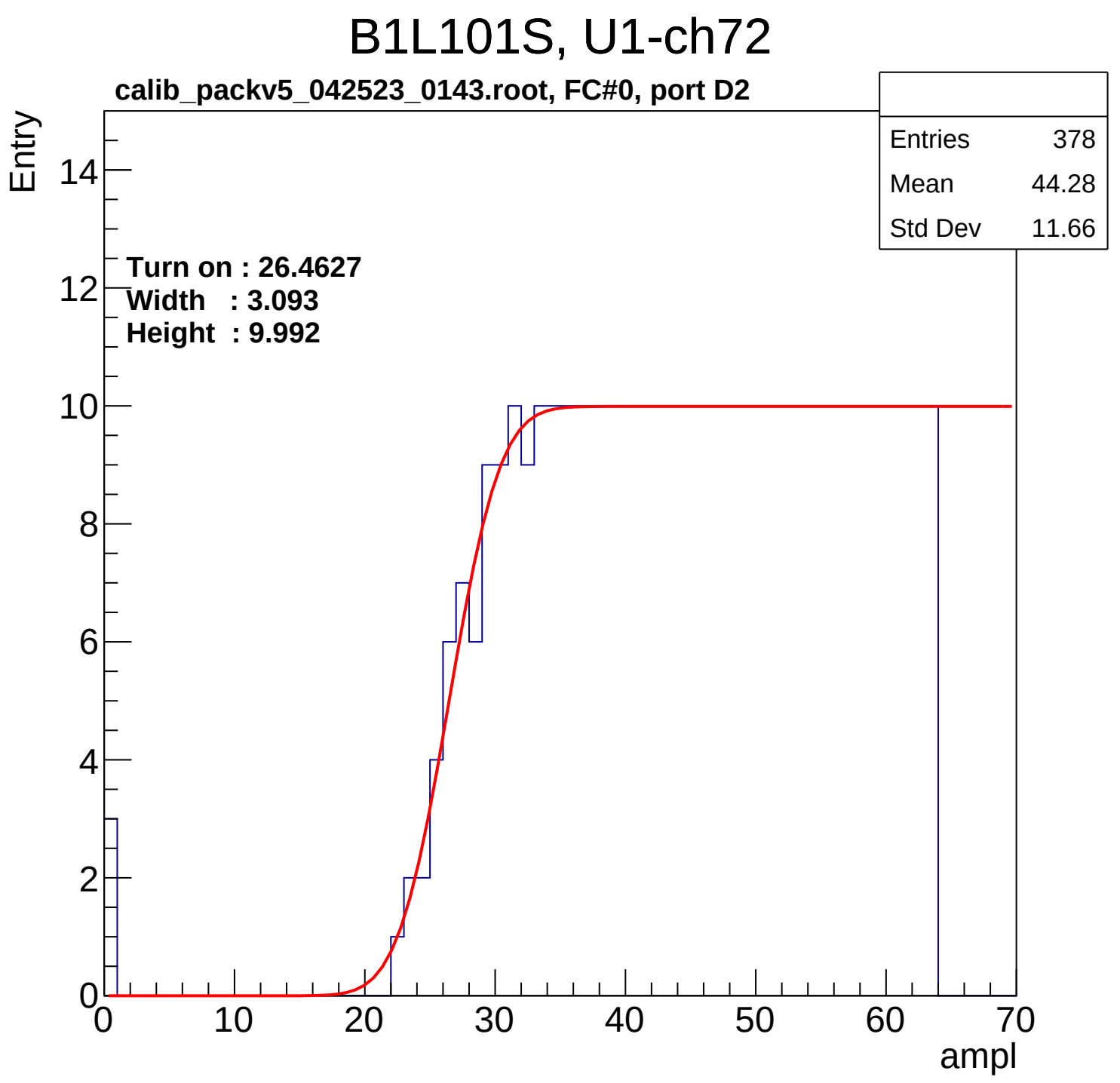
B1L101S, U1-ch72
calib_packv5_042523_0143.root, FC#0, port D2
Entries 378
Mean 44.28
Std Dev 11.66
Turn on : 26.4627
Width : 3.093
Height : 9.992
Entry
ampl
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8
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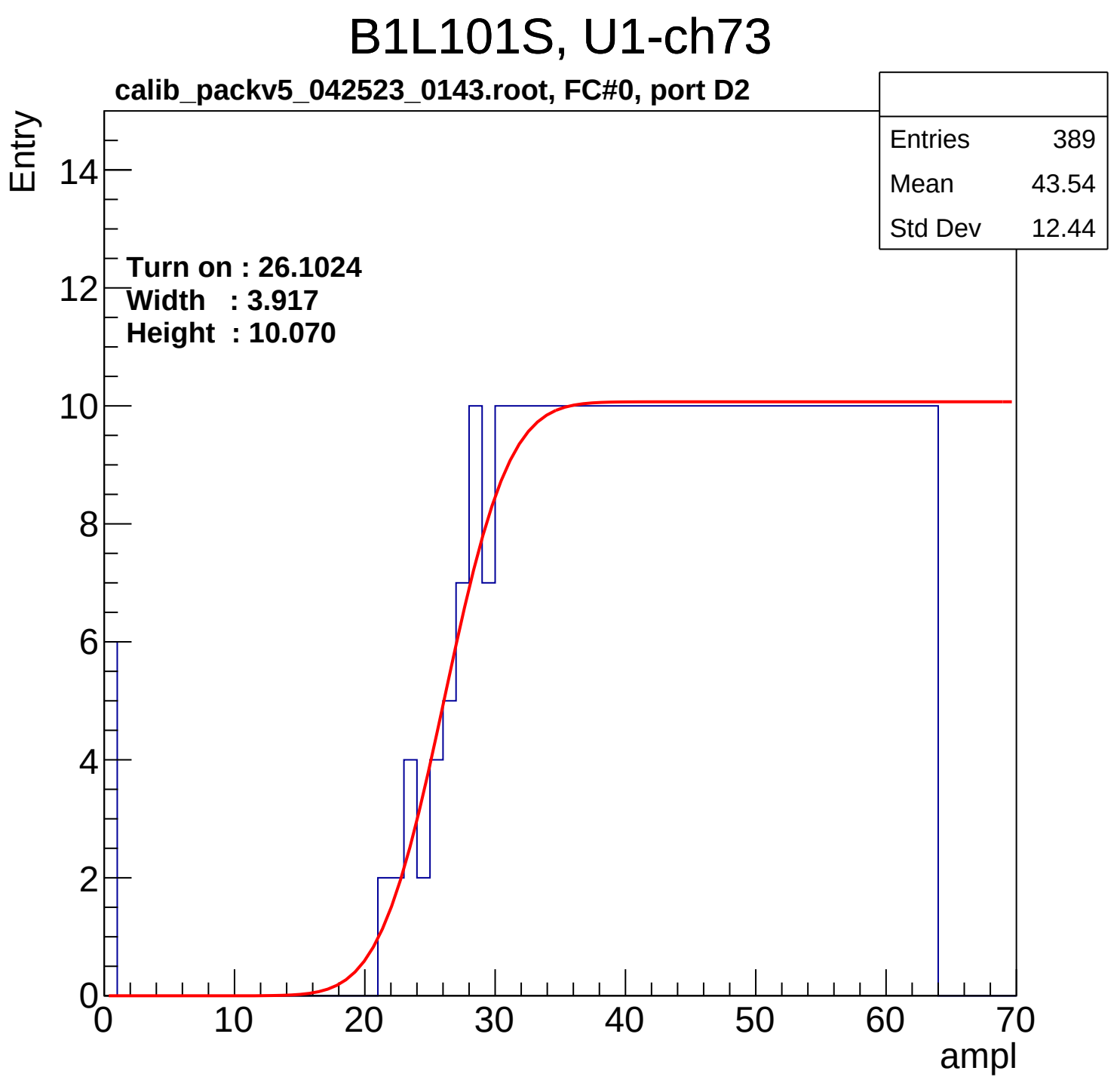
B1L101S, U1-ch73
calib_packv5_042523_0143.root, FC#0, port D2
Entries 389
Mean 43.54
Std Dev 12.44
Turn on : 26.1024
Width : 3.917
Height : 10.070
Entry
ampl
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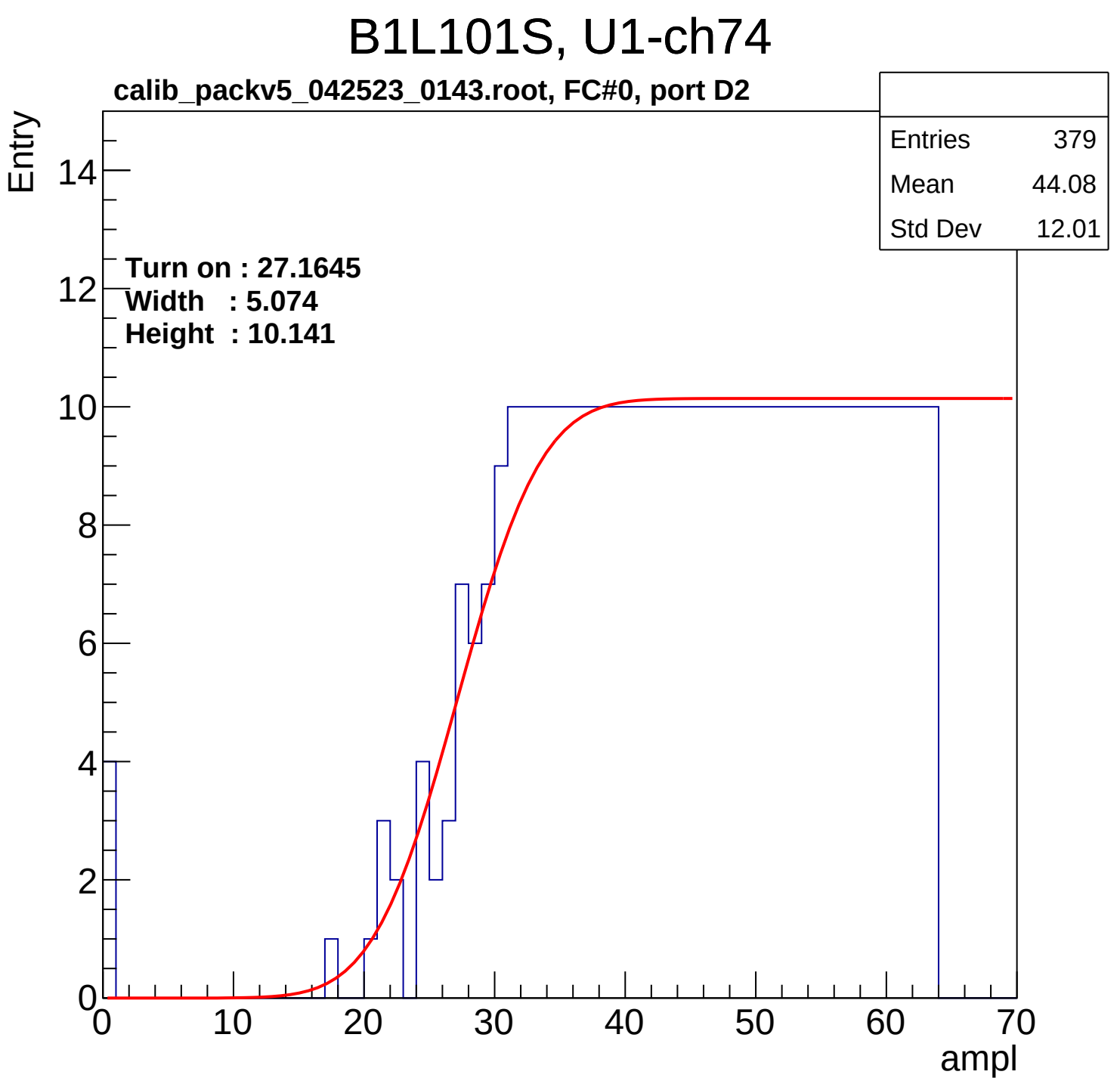
B1L101S, U1-ch74
calib_packv5_042523_0143.root, FC#0, port D2
Entries 379
Mean 44.08
Std Dev 12.01
Turn on : 27.1645
Width : 5.074
Height : 10.141
Entry
ampl
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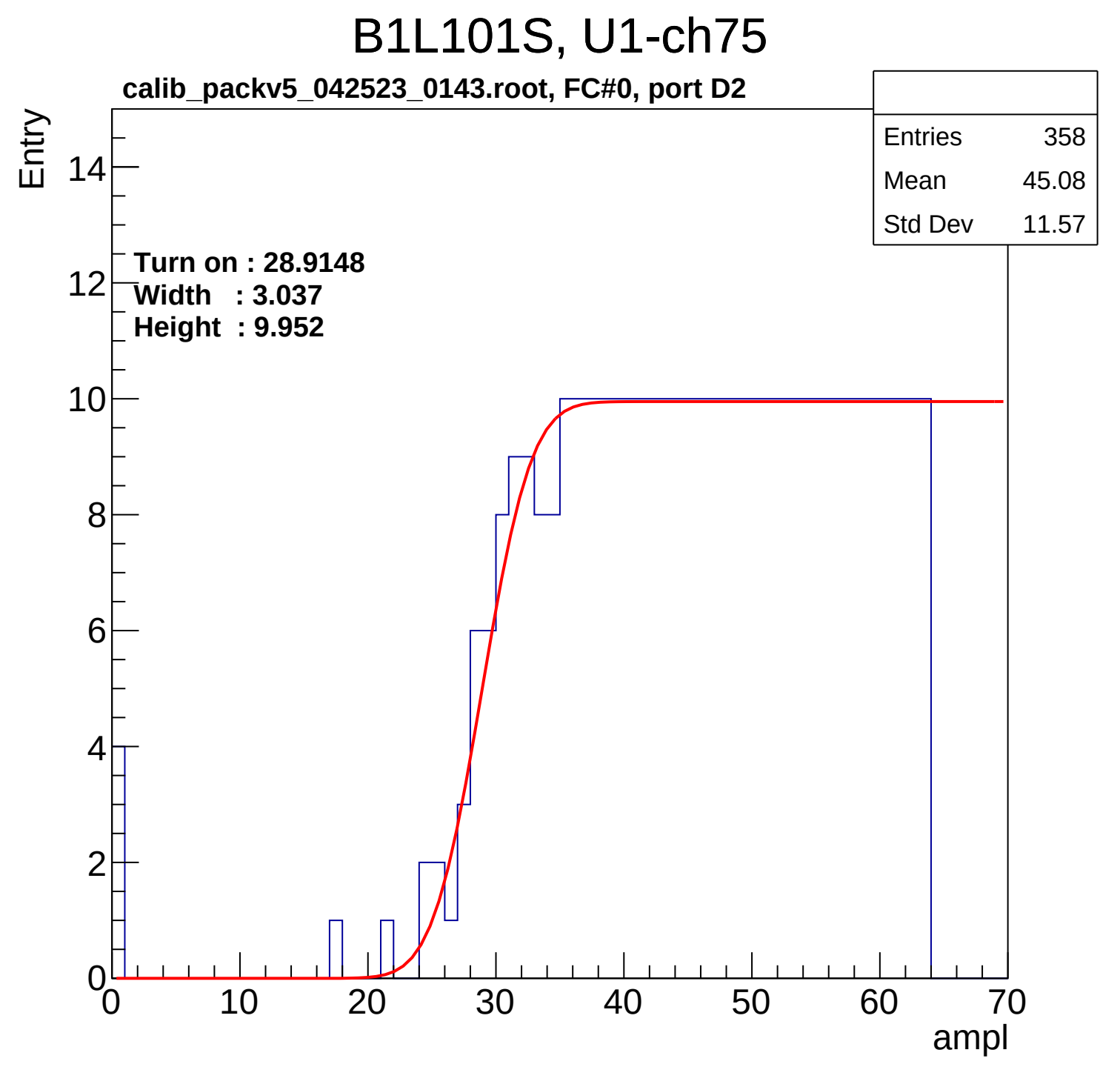
B1L101S, U1-ch75
calib_packv5_042523_0143.root, FC#0, port D2
Entries 358
Mean 45.08
Std Dev 11.57
Turn on : 28.9148
Width : 3.037
Height : 9.952
Entry
ampl
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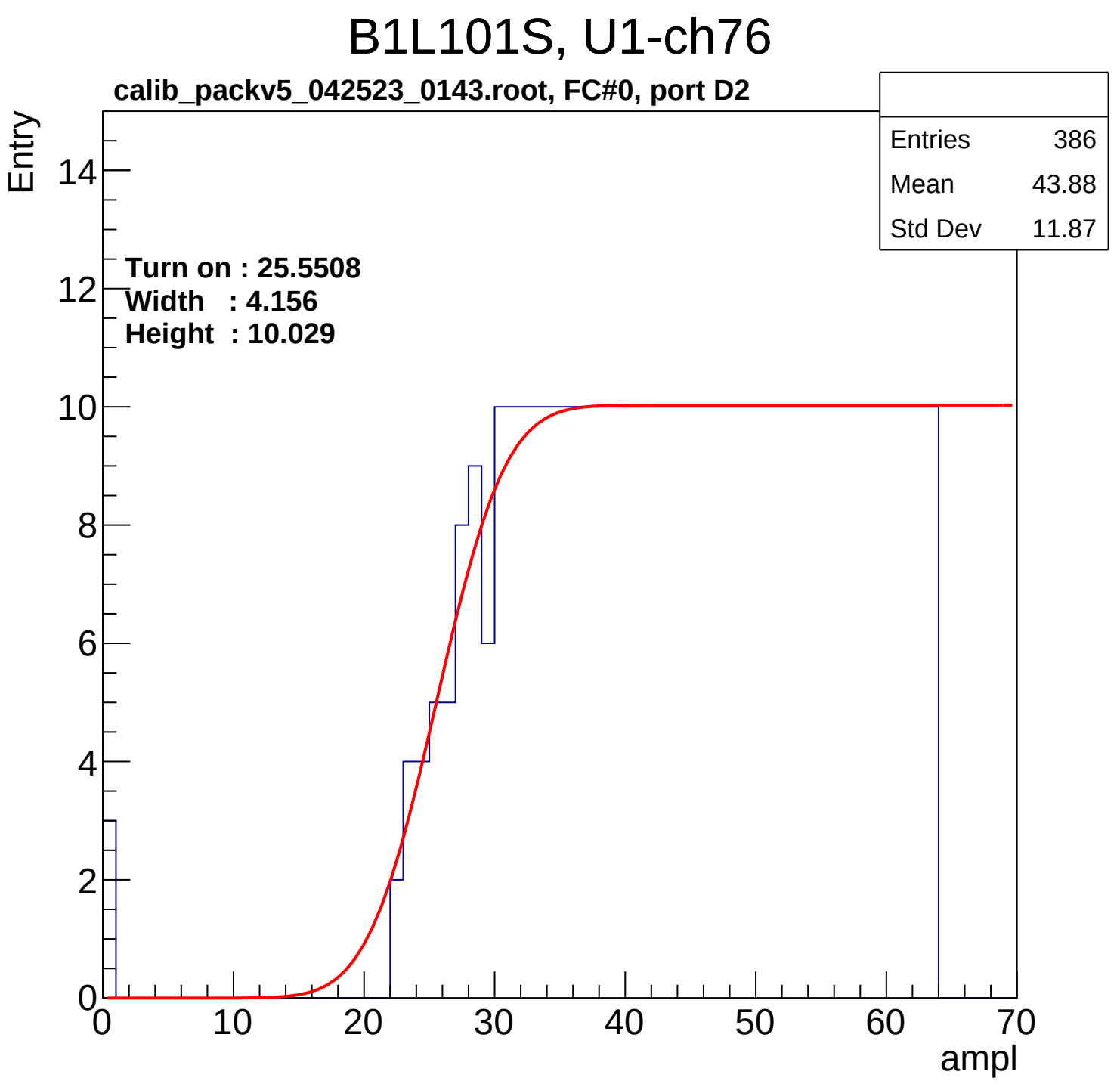
B1L101S, U1-ch76
calib_packv5_042523_0143.root, FC#0, port D2
Entries 386
Mean 43.88
Std Dev 11.87
Turn on : 25.5508
Width : 4.156
Height : 10.029
Entry
ampl
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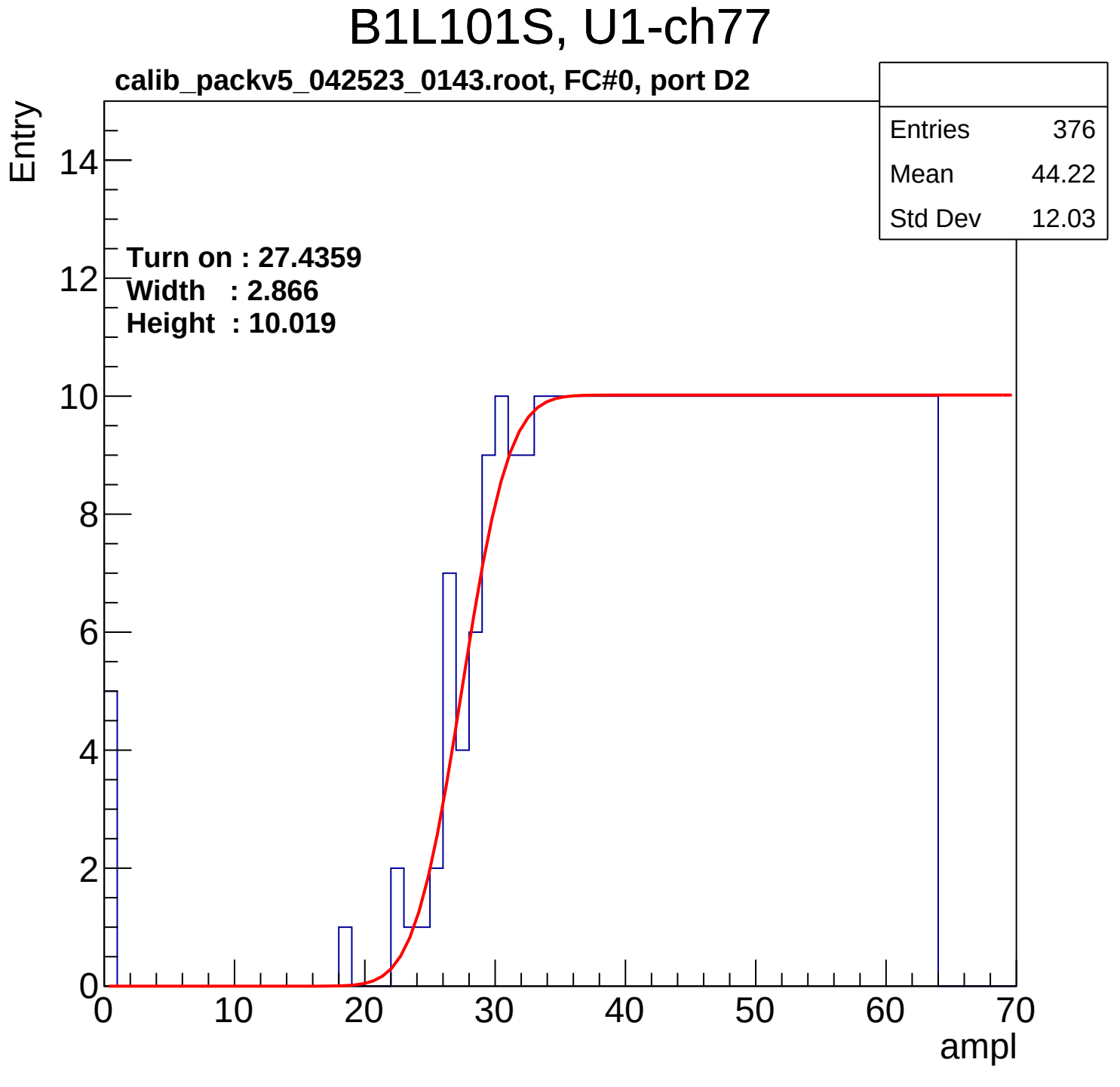
B1L101S, U1-ch77
calib_packv5_042523_0143.root, FC#0, port D2
Entries 376
Mean 44.22
Std Dev 12.03
Turn on : 27.4359
Width : 2.866
Height : 10.019
Entry
ampl
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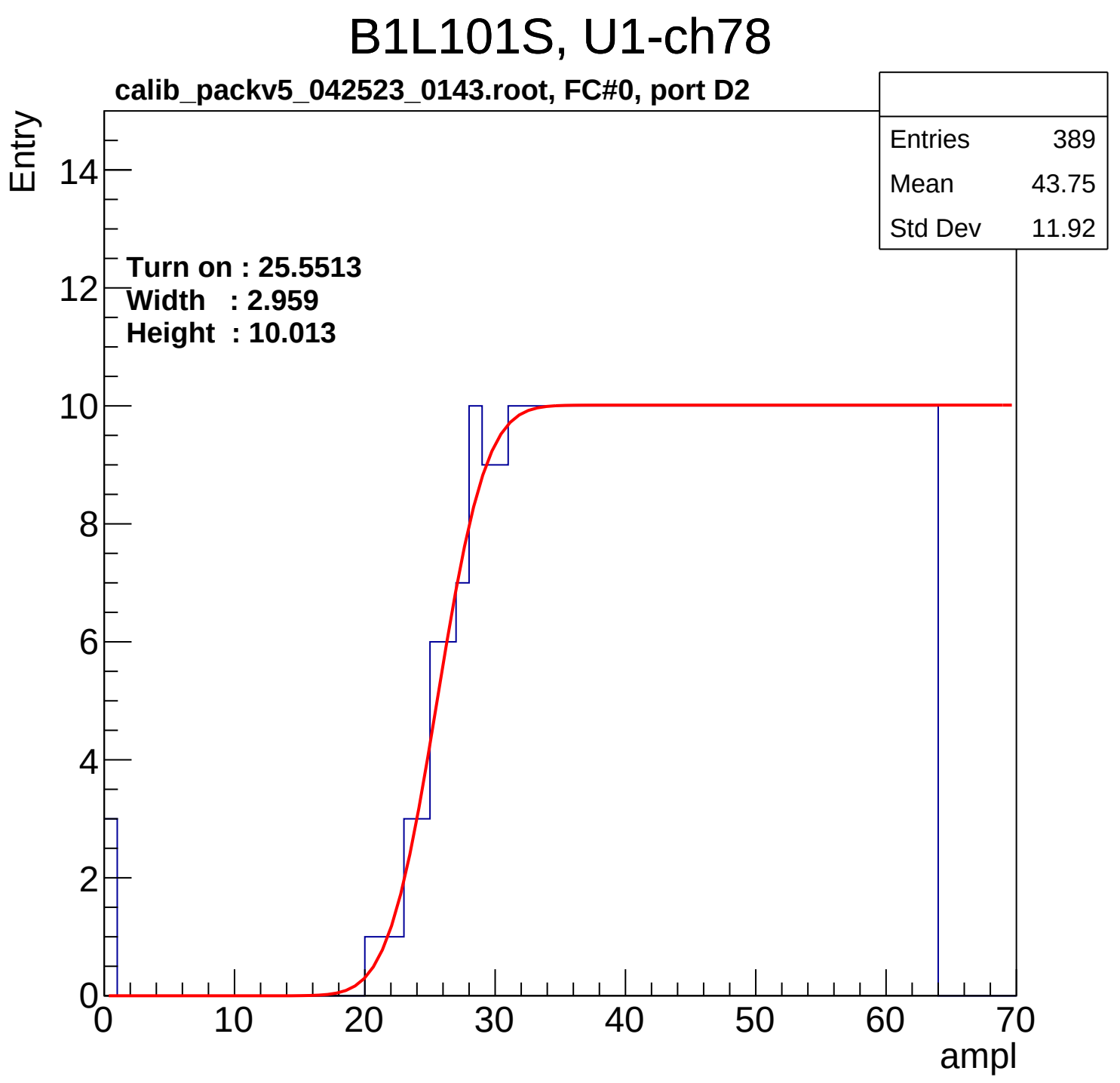
B1L101S, U1-ch78
calib_packv5_042523_0143.root, FC#0, port D2
Entries 389
Mean 43.75
Std Dev 11.92
Turn on : 25.5513
Width : 2.959
Height : 10.013
Entry
ampl
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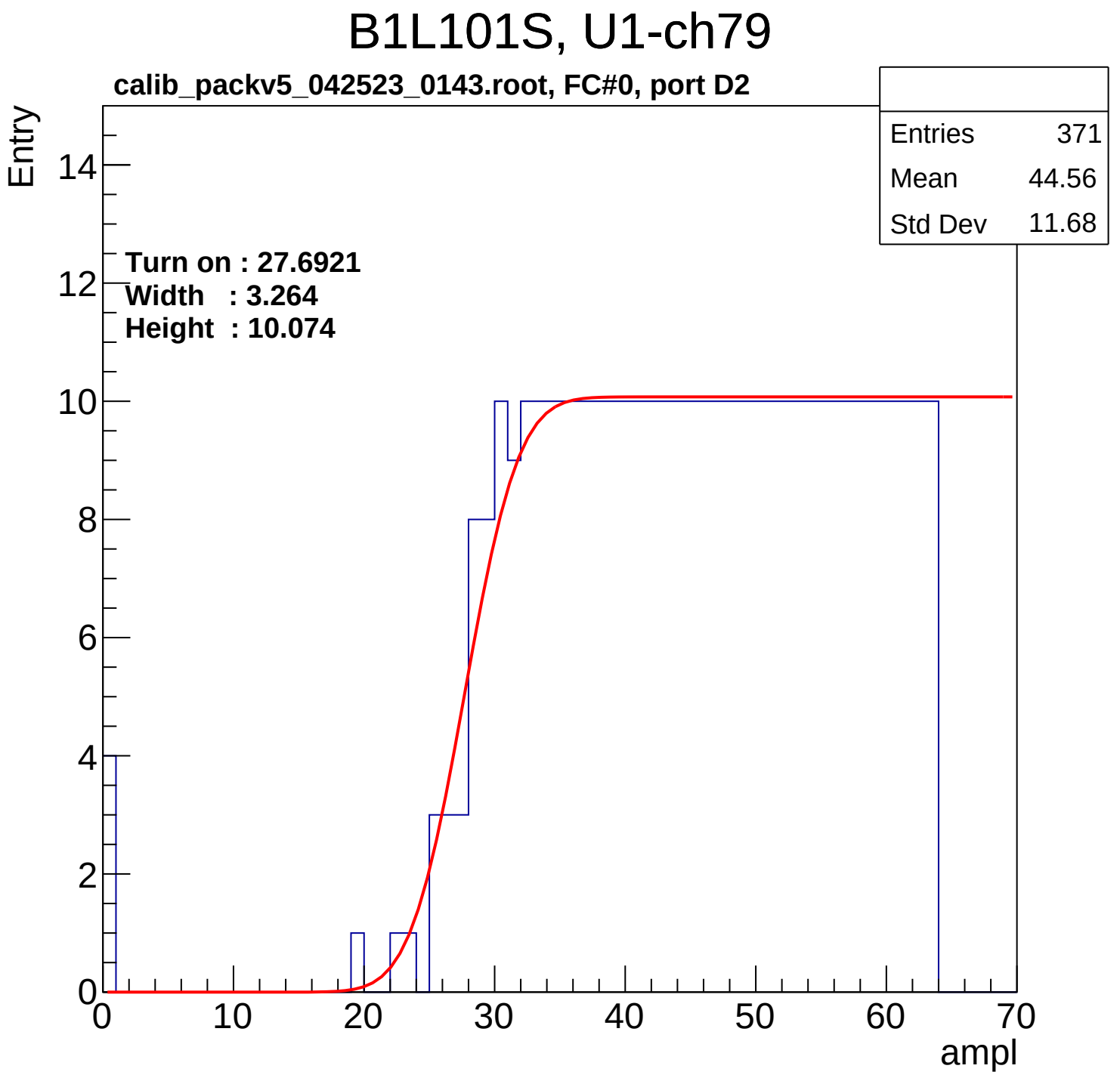
B1L101S, U1-ch79
calib_packv5_042523_0143.root, FC#0, port D2
Entries 371
Mean 44.56
Std Dev 11.68
Turn on : 27.6921
Width : 3.264
Height : 10.074
Entry
ampl
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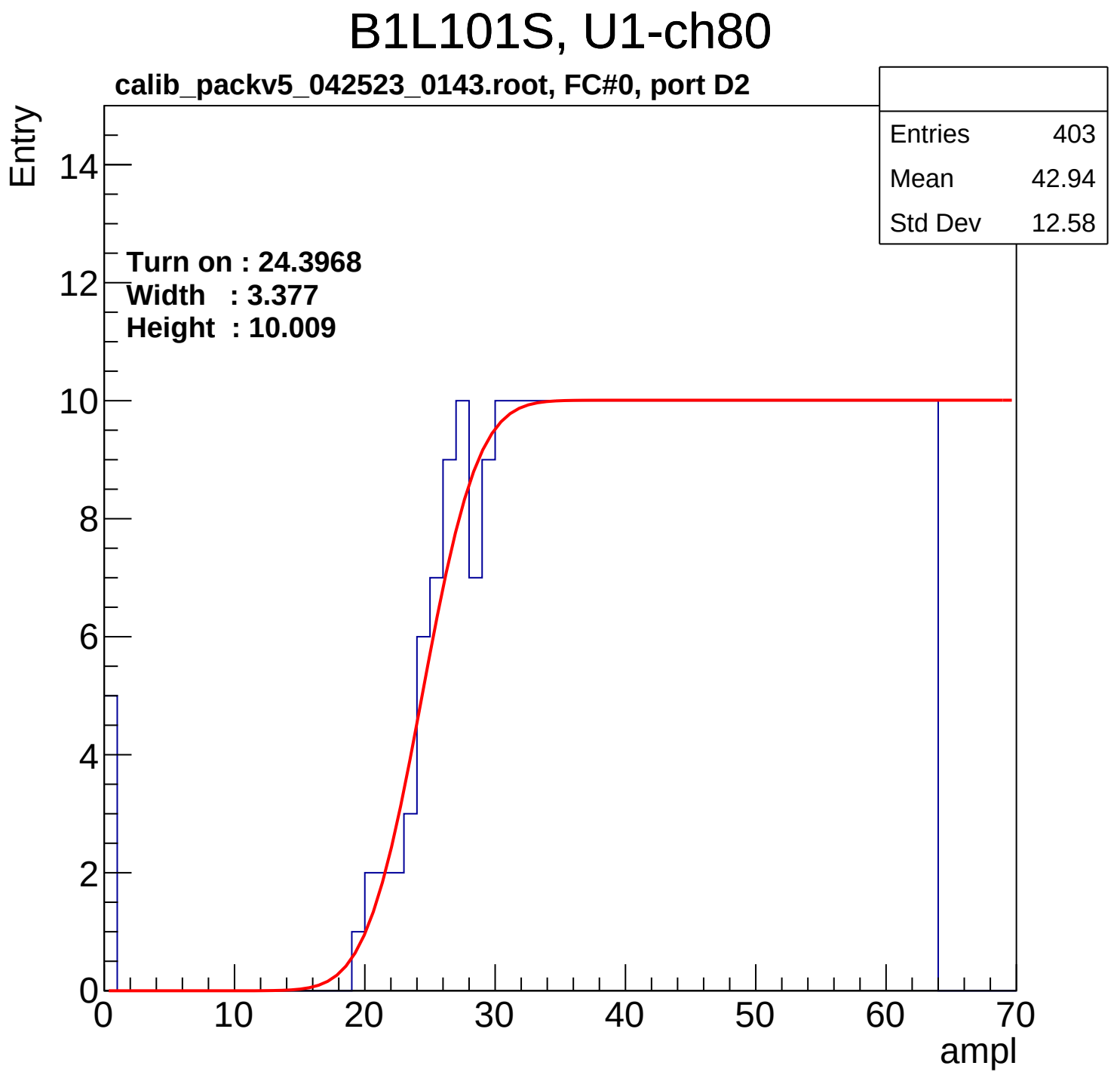
B1L101S, U1-ch80
calib_packv5_042523_0143.root, FC#0, port D2
Entries 403
Mean 42.94
Std Dev 12.58
Turn on : 24.3968
Width : 3.377
Height : 10.009
Entry
ampl
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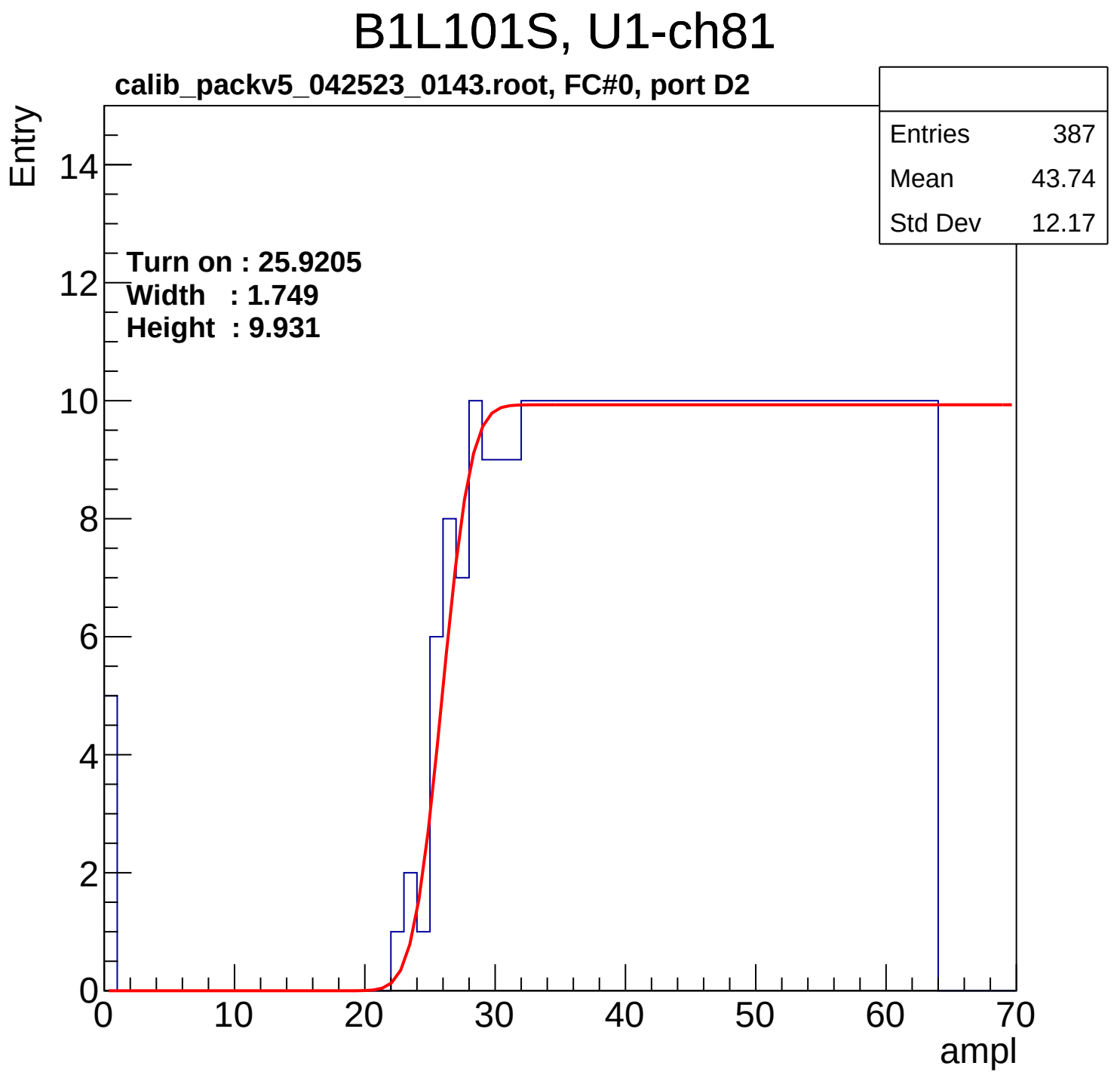
B1L101S, U1-ch81
calib_packv5_042523_0143.root, FC#0, port D2
Entries 387
Mean 43.74
Std Dev 12.17
Turn on : 25.9205
Width : 1.749
Height : 9.931
Entry
ampl
0
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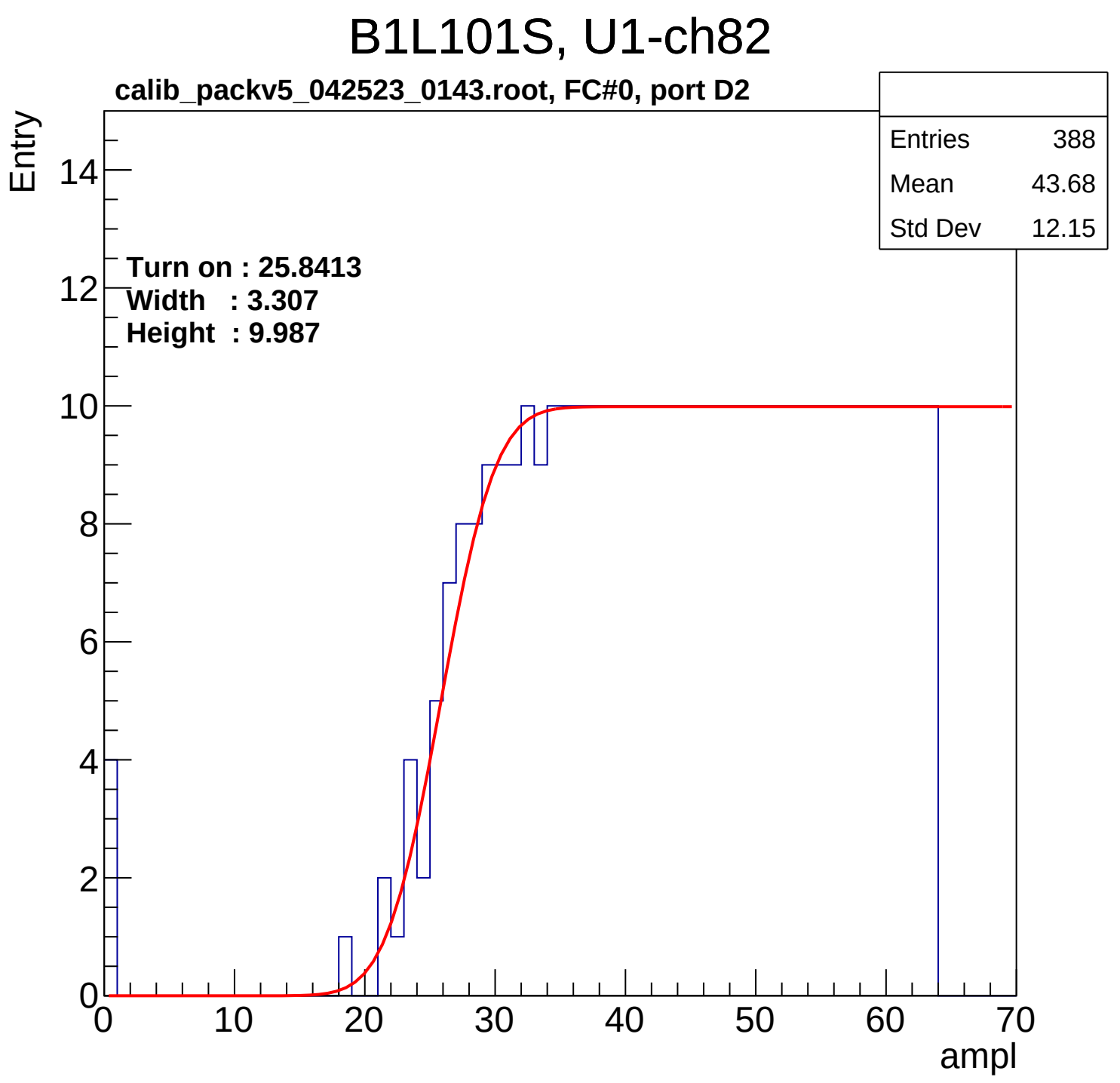
B1L101S, U1-ch82
calib_packv5_042523_0143.root, FC#0, port D2
Entries 388
Mean 43.68
Std Dev 12.15
Turn on : 25.8413
Width : 3.307
Height : 9.987
Entry
ampl
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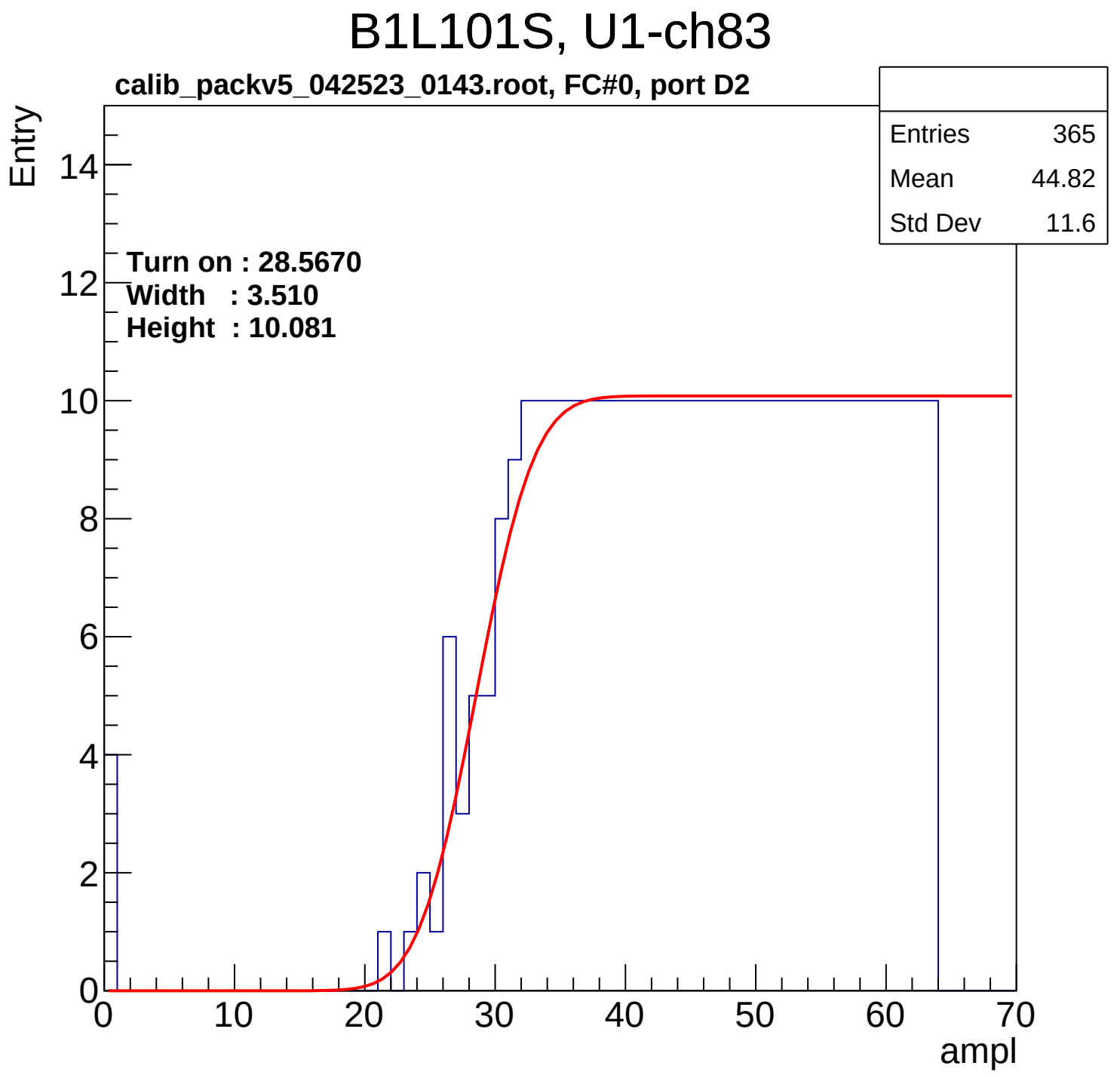
B1L101S, U1-ch83
calib_packv5_042523_0143.root, FC#0, port D2
Entries 365
Mean 44.82
Std Dev 11.6
Turn on : 28.5670
Width : 3.510
Height : 10.081
Entry
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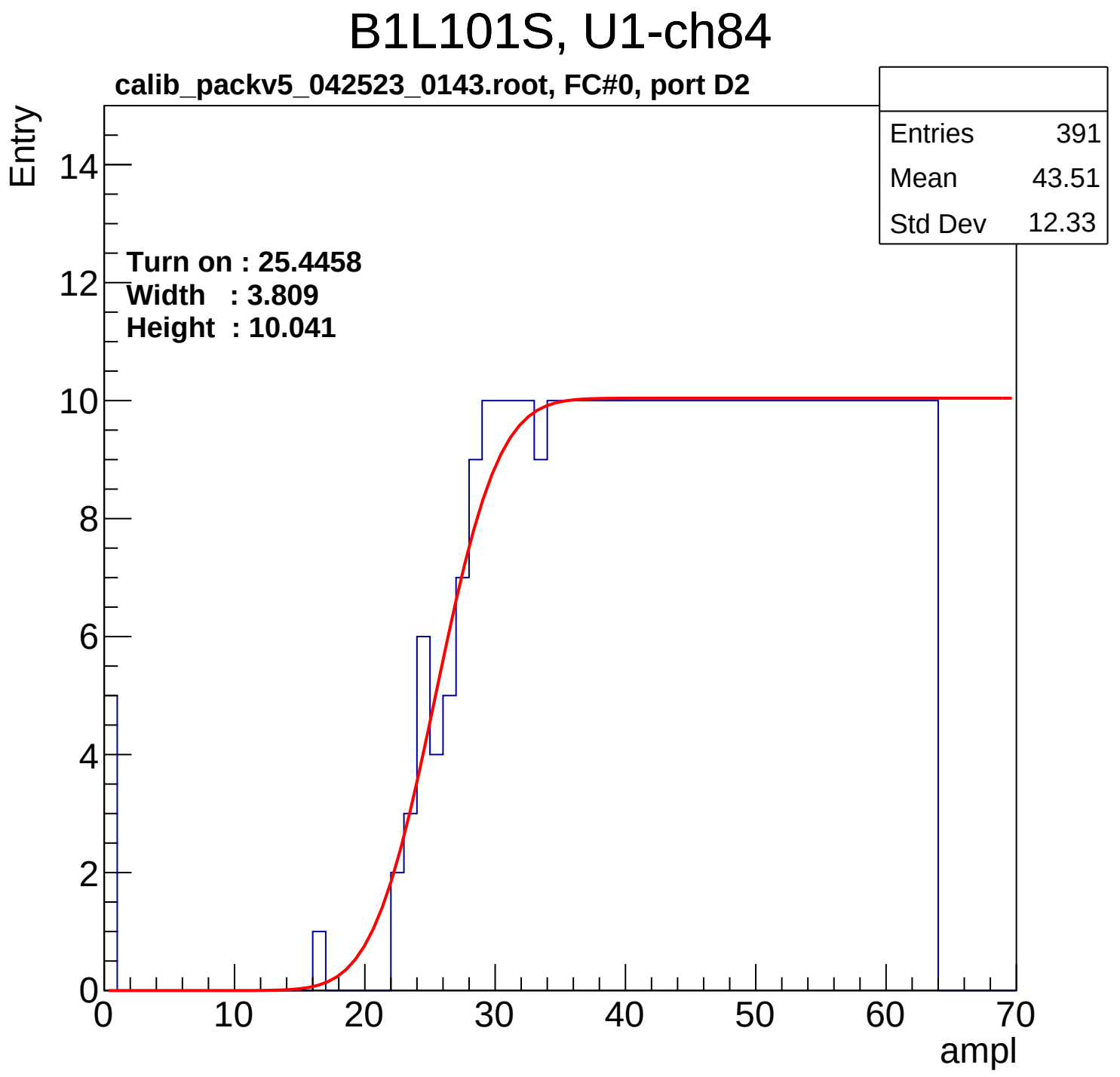
B1L101S, U1-ch84
calib_packv5_042523_0143.root, FC#0, port D2
Entries 391
Mean 43.51
Std Dev 12.33
Turn on : 25.4458
Width : 3.809
Height : 10.041
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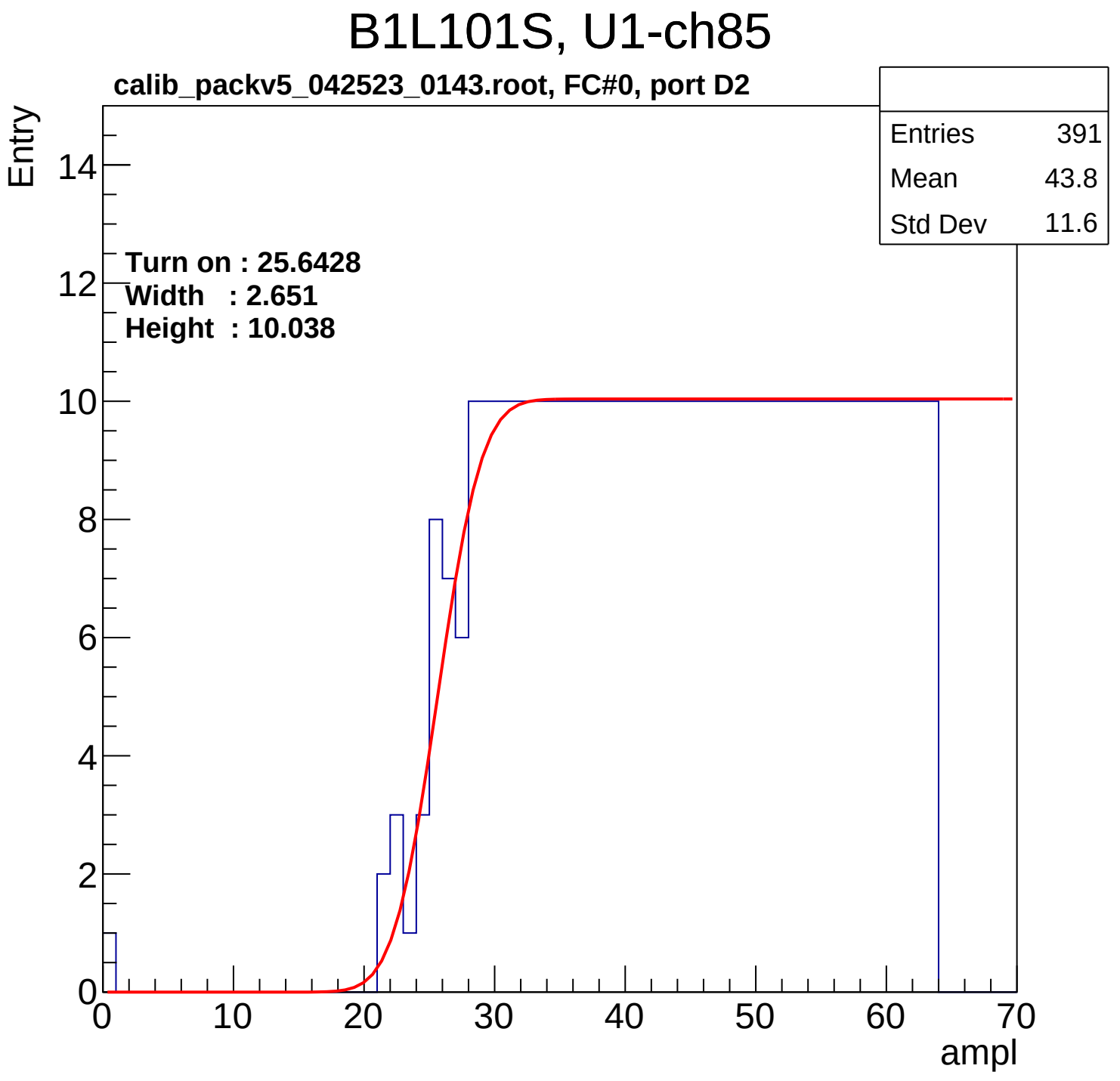
B1L101S, U1-ch85
calib_packv5_042523_0143.root, FC#0, port D2
Entries 391
Mean 43.8
Std Dev 11.6
Turn on : 25.6428
Width : 2.651
Height : 10.038
Entry
ampl
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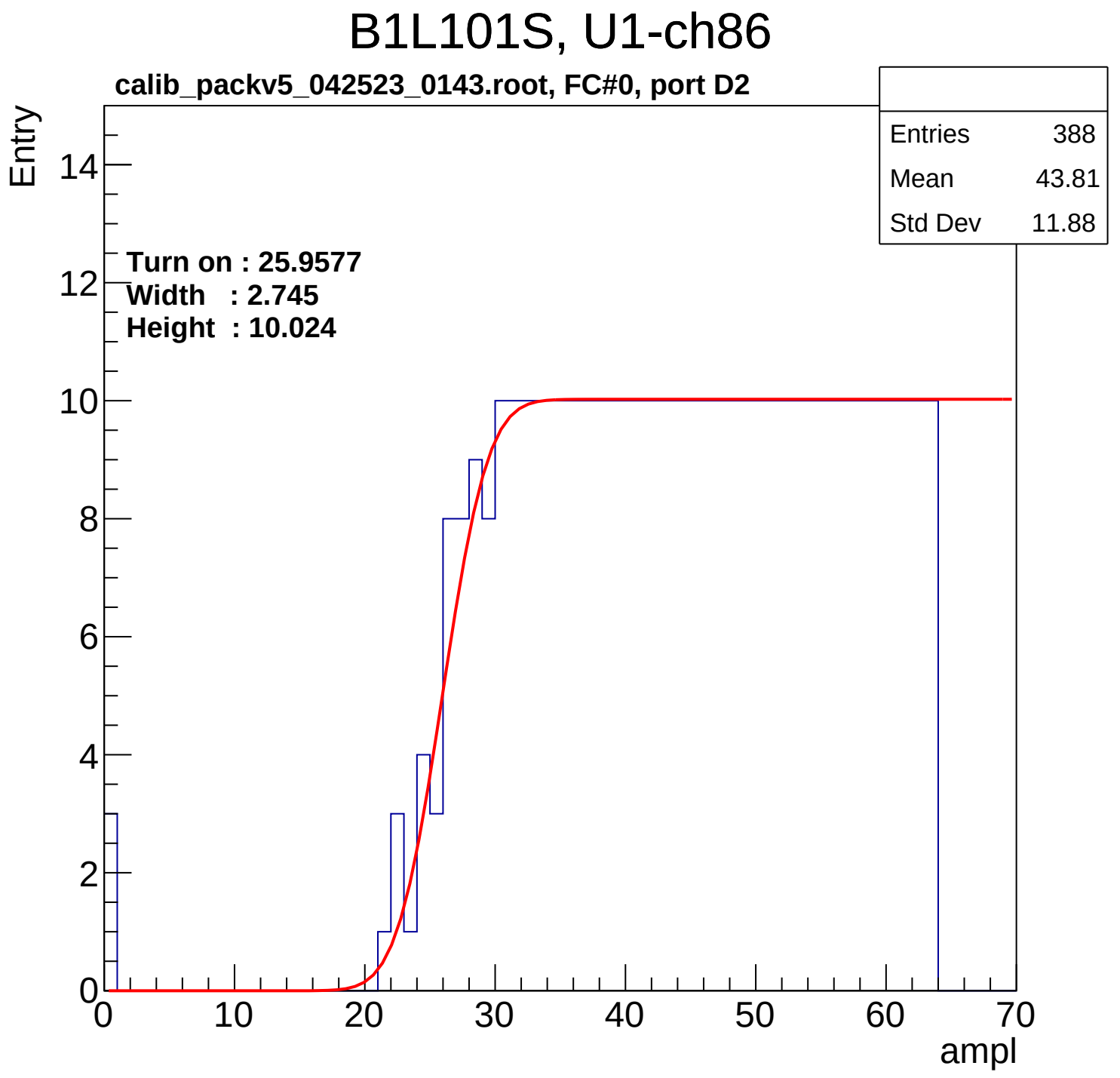
B1L101S, U1-ch86
calib_packv5_042523_0143.root, FC#0, port D2
Entries 388
Mean 43.81
Std Dev 11.88
Turn on : 25.9577
Width : 2.745
Height : 10.024
Entry
ampl
0
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6
8
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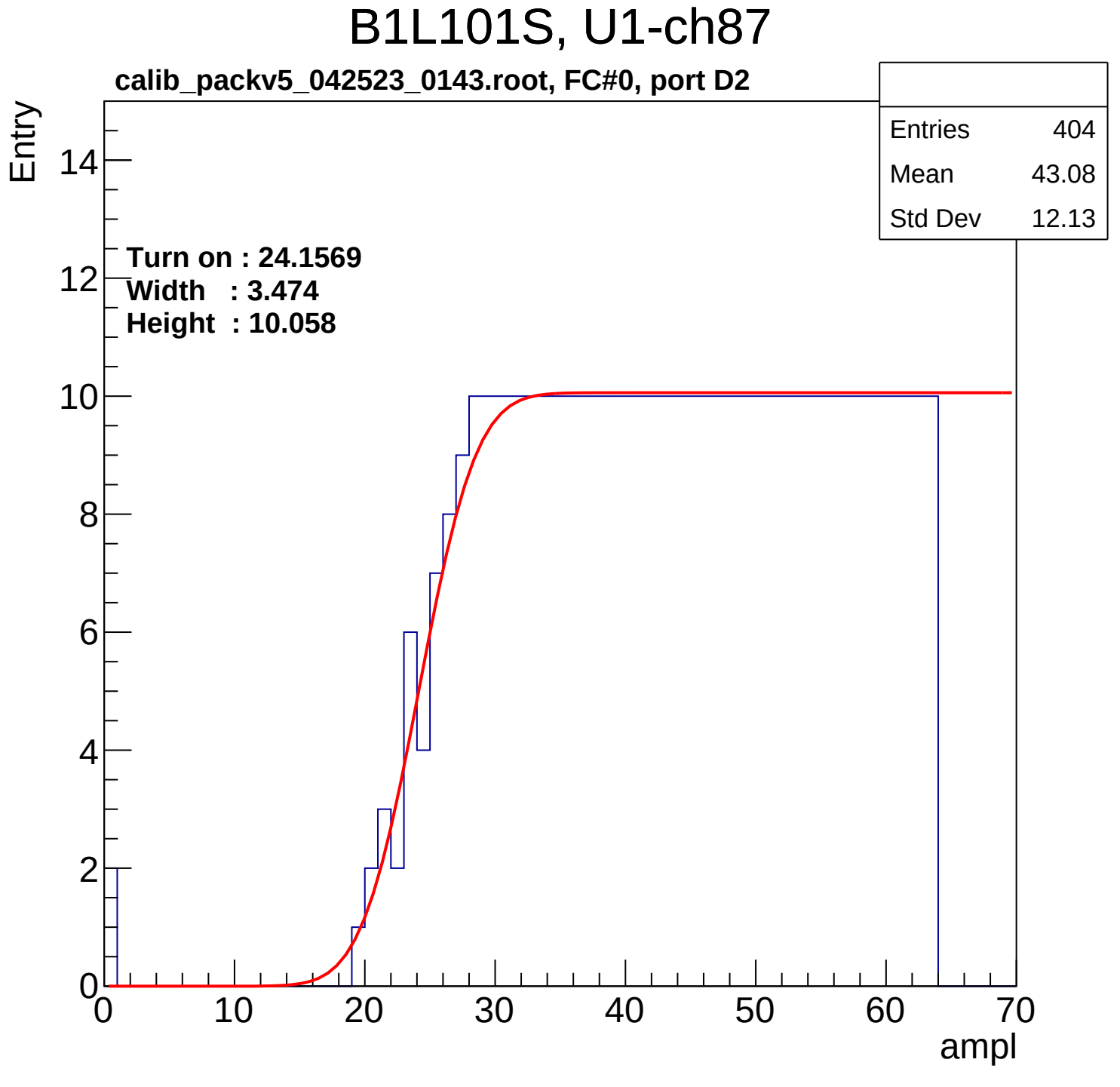
B1L101S, U1-ch87
calib_packv5_042523_0143.root, FC#0, port D2
Entries 404
Mean 43.08
Std Dev 12.13
Turn on : 24.1569
Width : 3.474
Height : 10.058
Entry
ampl
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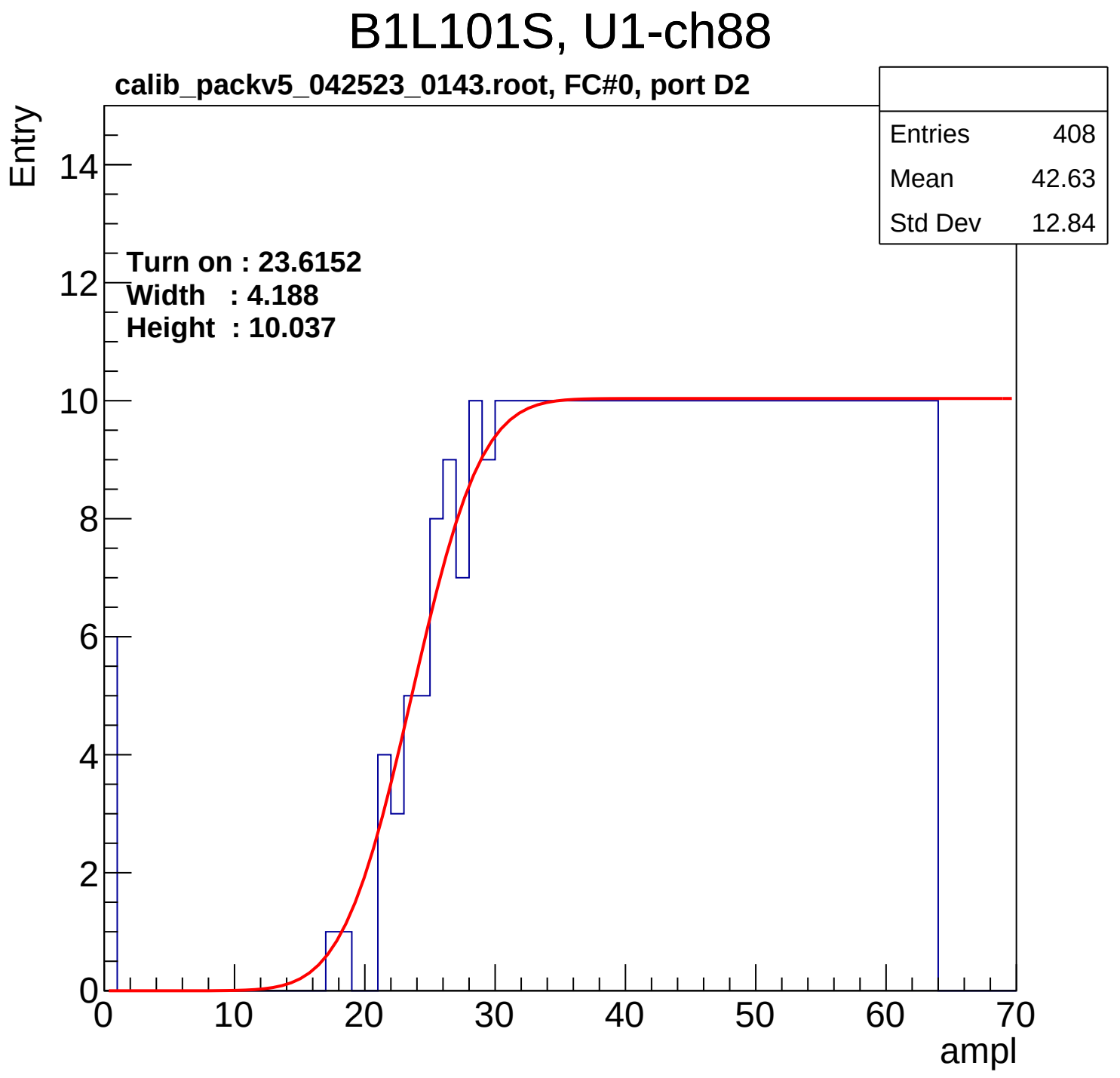
B1L101S, U1-ch88
calib_packv5_042523_0143.root, FC#0, port D2
Entries 408
Mean 42.63
Std Dev 12.84
Turn on : 23.6152
Width : 4.188
Height : 10.037
Entry
ampl
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2
4
6
8
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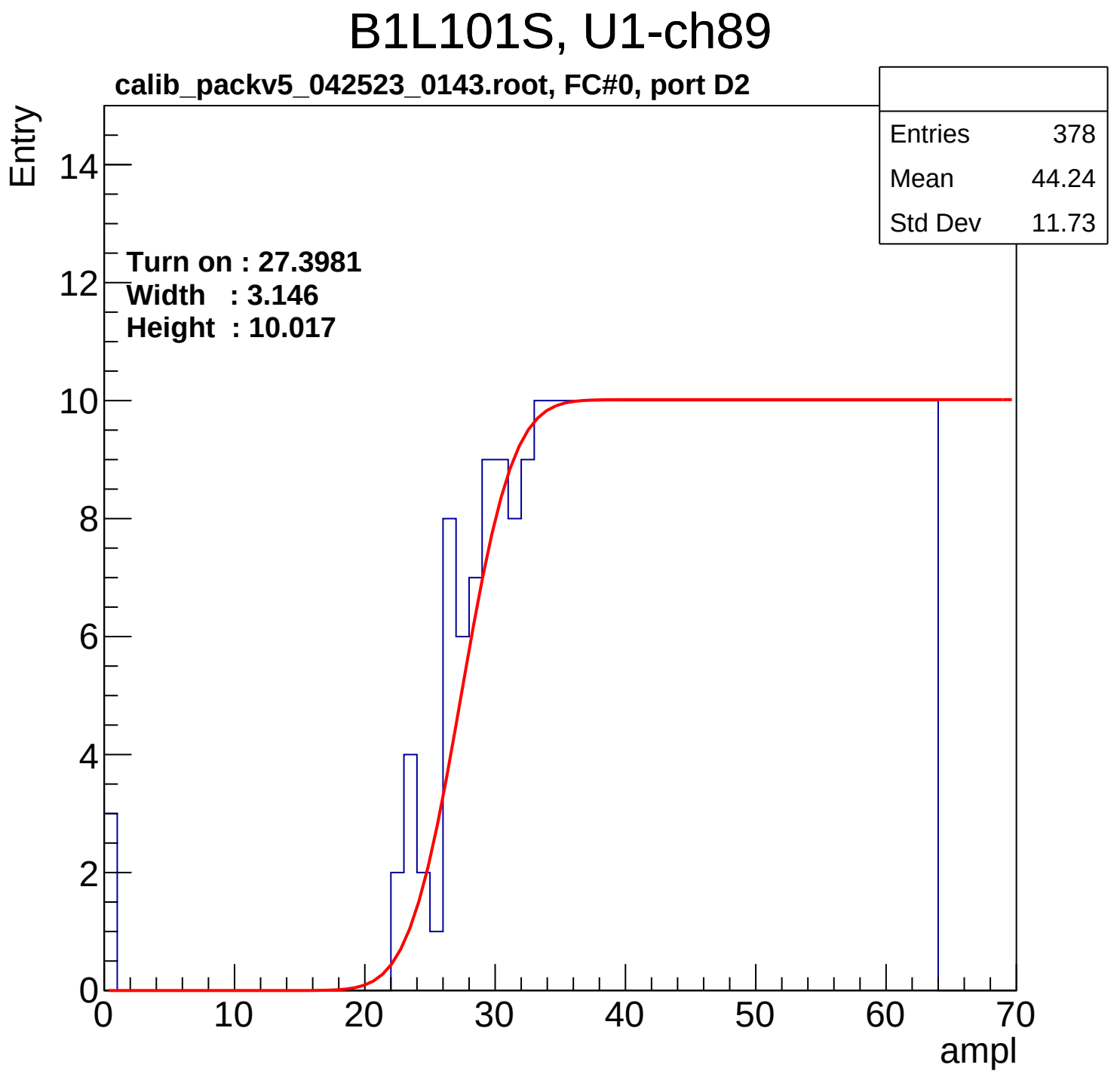
B1L101S, U1-ch89
calib_packv5_042523_0143.root, FC#0, port D2
Entries 378
Mean 44.24
Std Dev 11.73
Turn on : 27.3981
Width : 3.146
Height : 10.017
Entry
ampl
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2
4
6
8
10
12
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0
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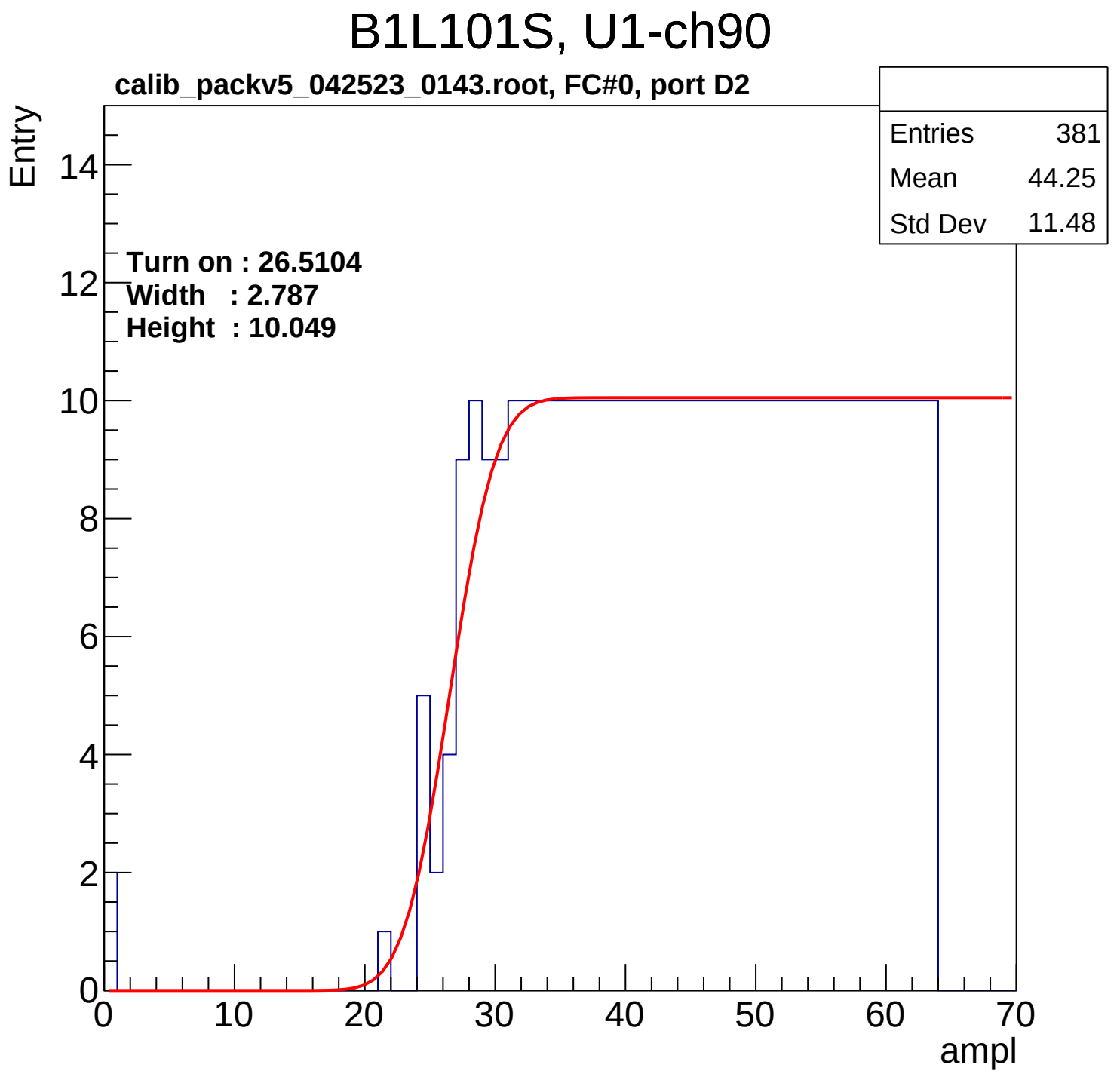
B1L101S, U1-ch90
calib_packv5_042523_0143.root, FC#0, port D2
Entries 381
Mean 44.25
Std Dev 11.48
Turn on : 26.5104
Width : 2.787
Height : 10.049
Entry
ampl
0
2
4
6
8
10
12
14
0
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40
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60
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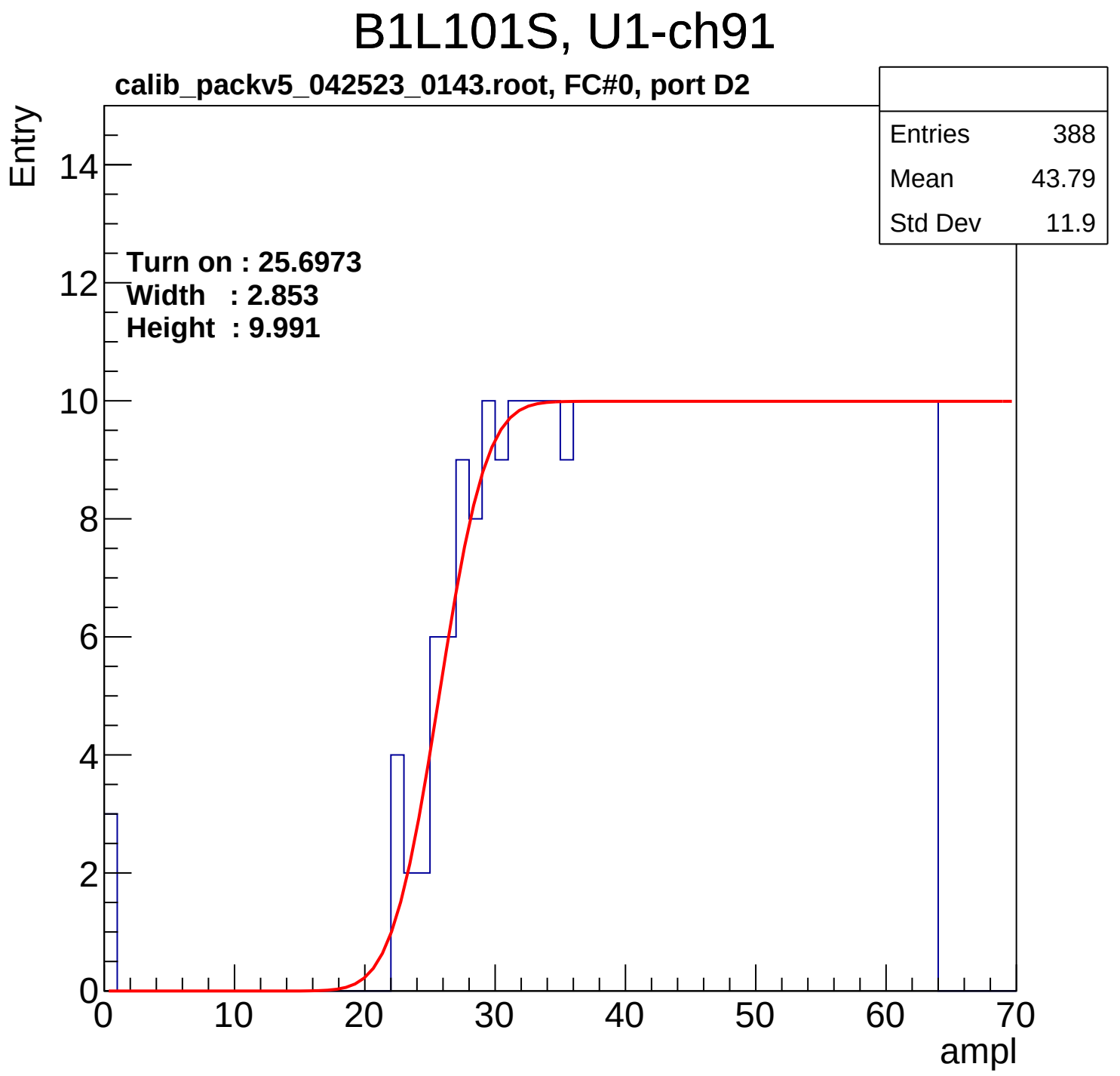
B1L101S, U1-ch91
calib_packv5_042523_0143.root, FC#0, port D2
Entries 388
Mean 43.79
Std Dev 11.9
Turn on : 25.6973
Width : 2.853
Height : 9.991
Entry
ampl
0
2
4
6
8
10
12
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0
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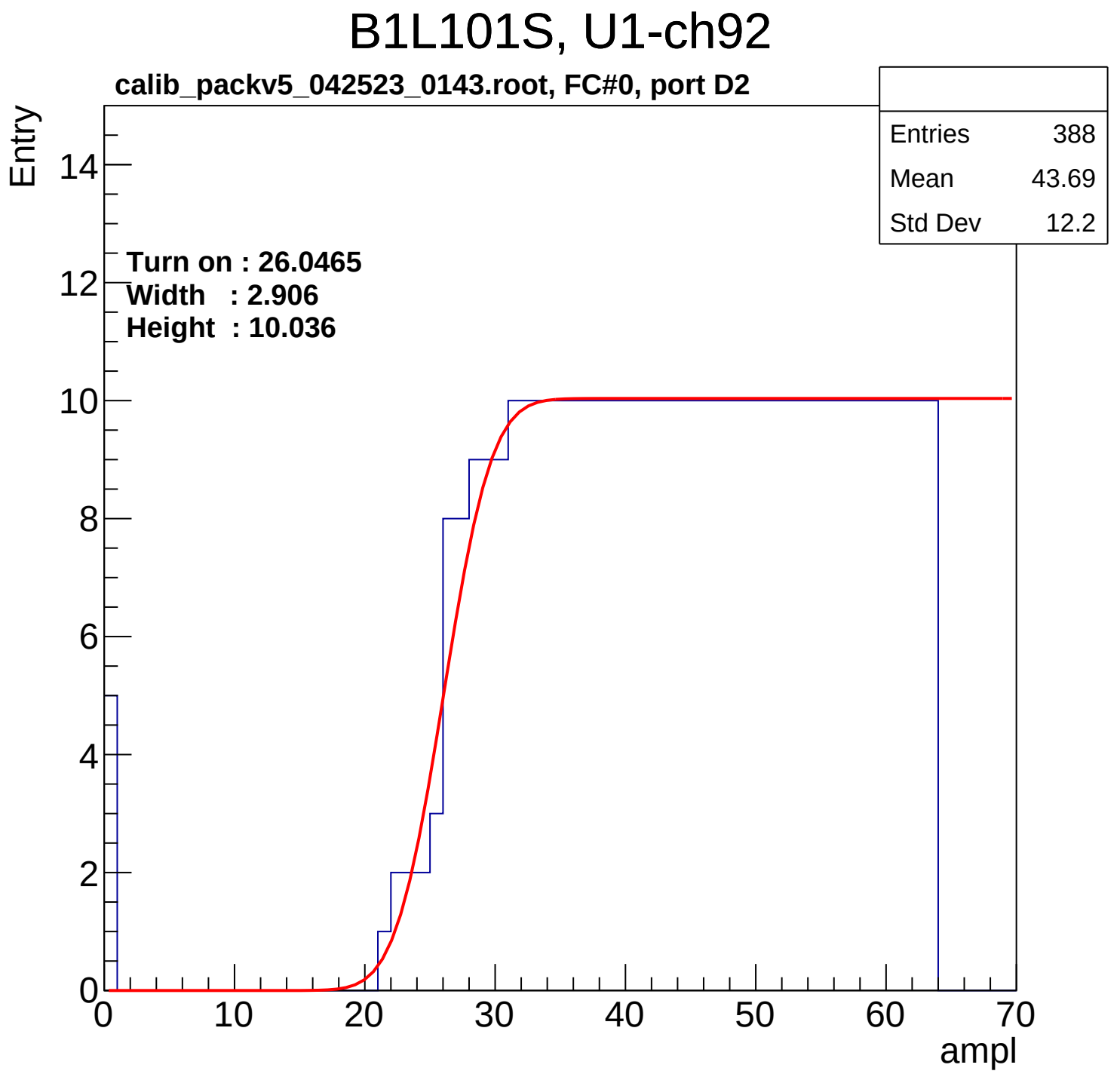
B1L101S, U1-ch92
calib_packv5_042523_0143.root, FC#0, port D2
Entries 388
Mean 43.69
Std Dev 12.2
Turn on : 26.0465
Width : 2.906
Height : 10.036
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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40
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60
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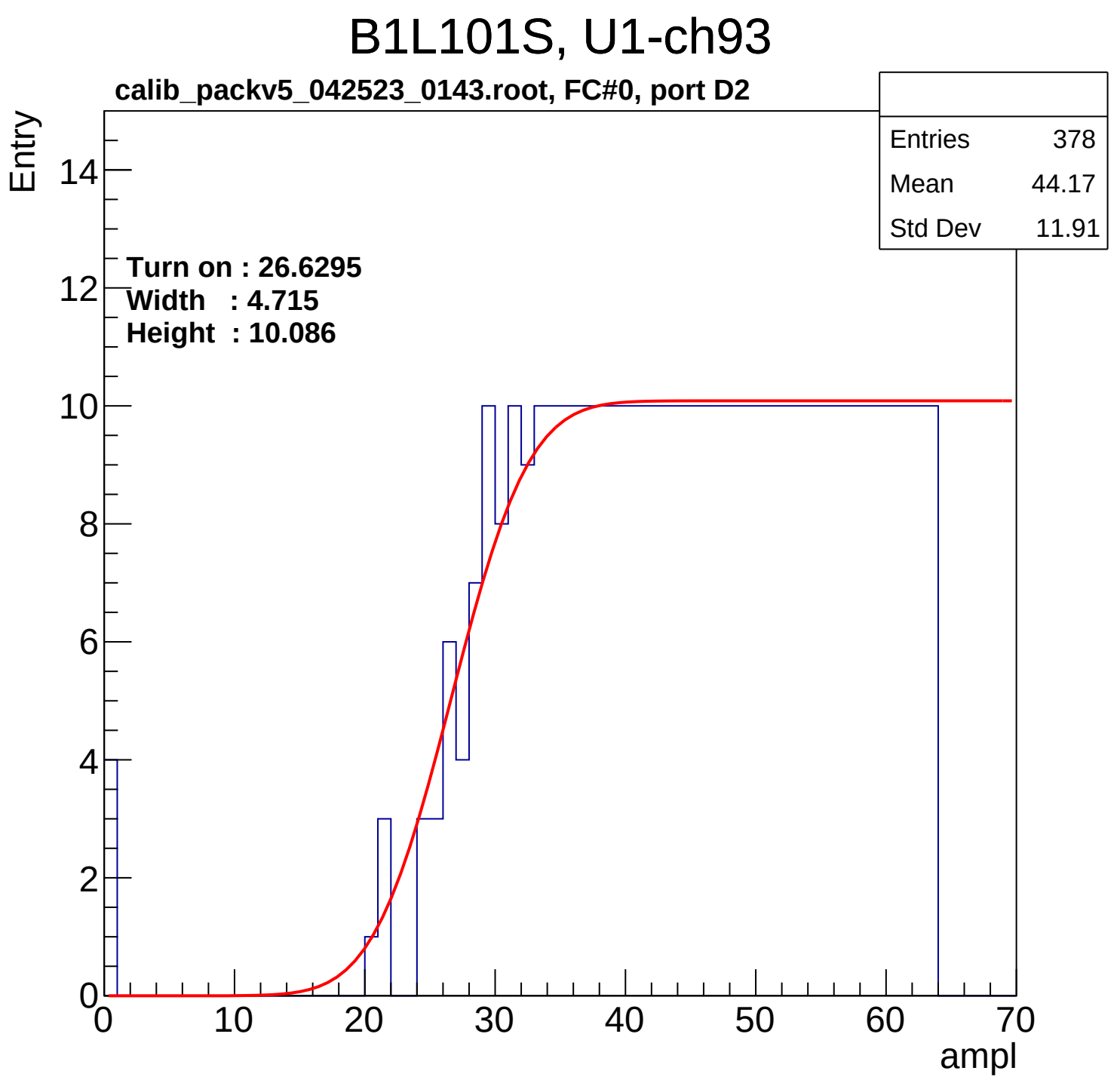
B1L101S, U1-ch93
calib_packv5_042523_0143.root, FC#0, port D2
Entries 378
Mean 44.17
Std Dev 11.91
Turn on : 26.6295
Width : 4.715
Height : 10.086
Entry
ampl
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2
4
6
8
10
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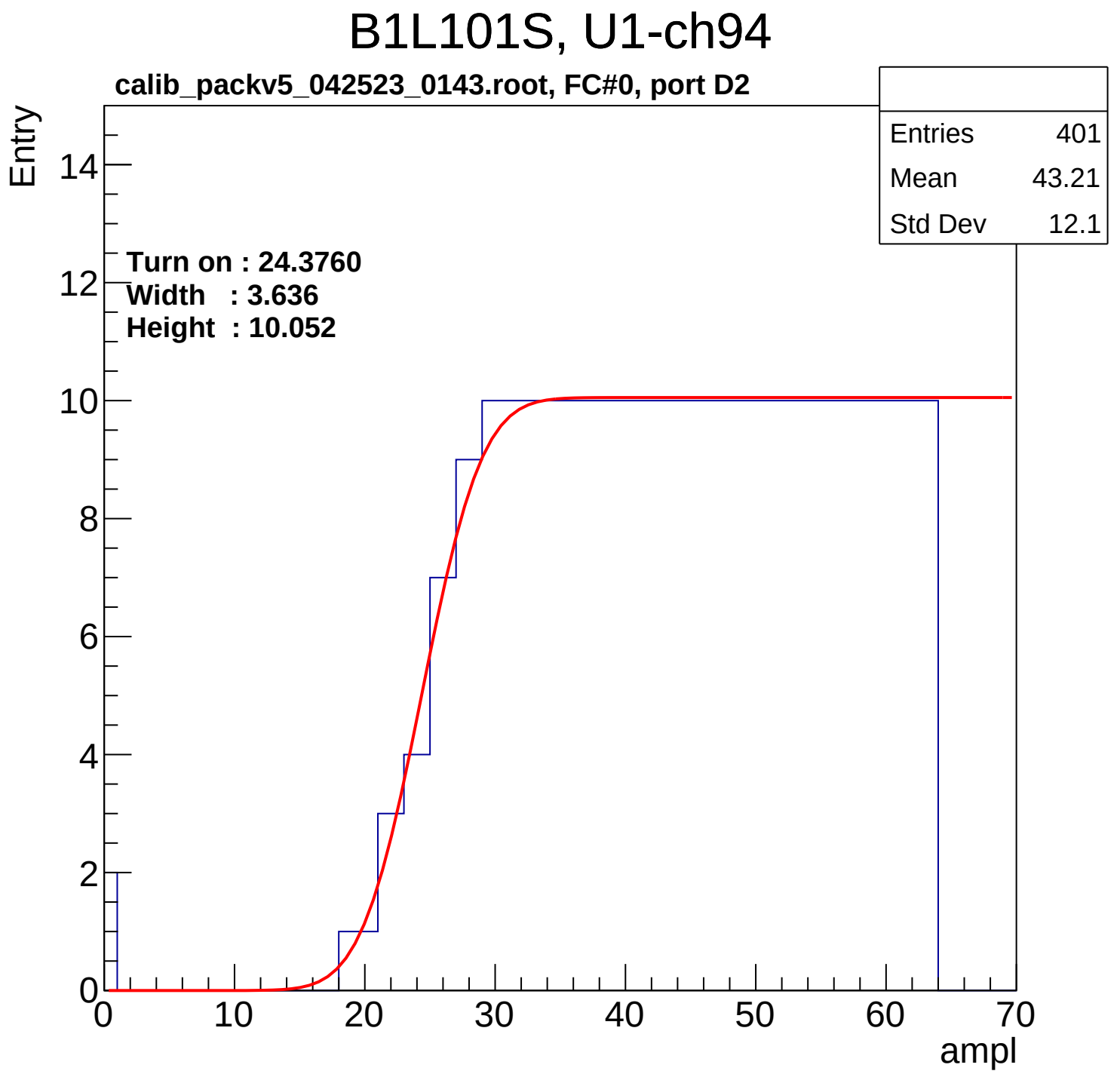
B1L101S, U1-ch94
calib_packv5_042523_0143.root, FC#0, port D2
Entries 401
Mean 43.21
Std Dev 12.1
Turn on : 24.3760
Width : 3.636
Height : 10.052
Entry
ampl
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2
4
6
8
10
12
14
0
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60
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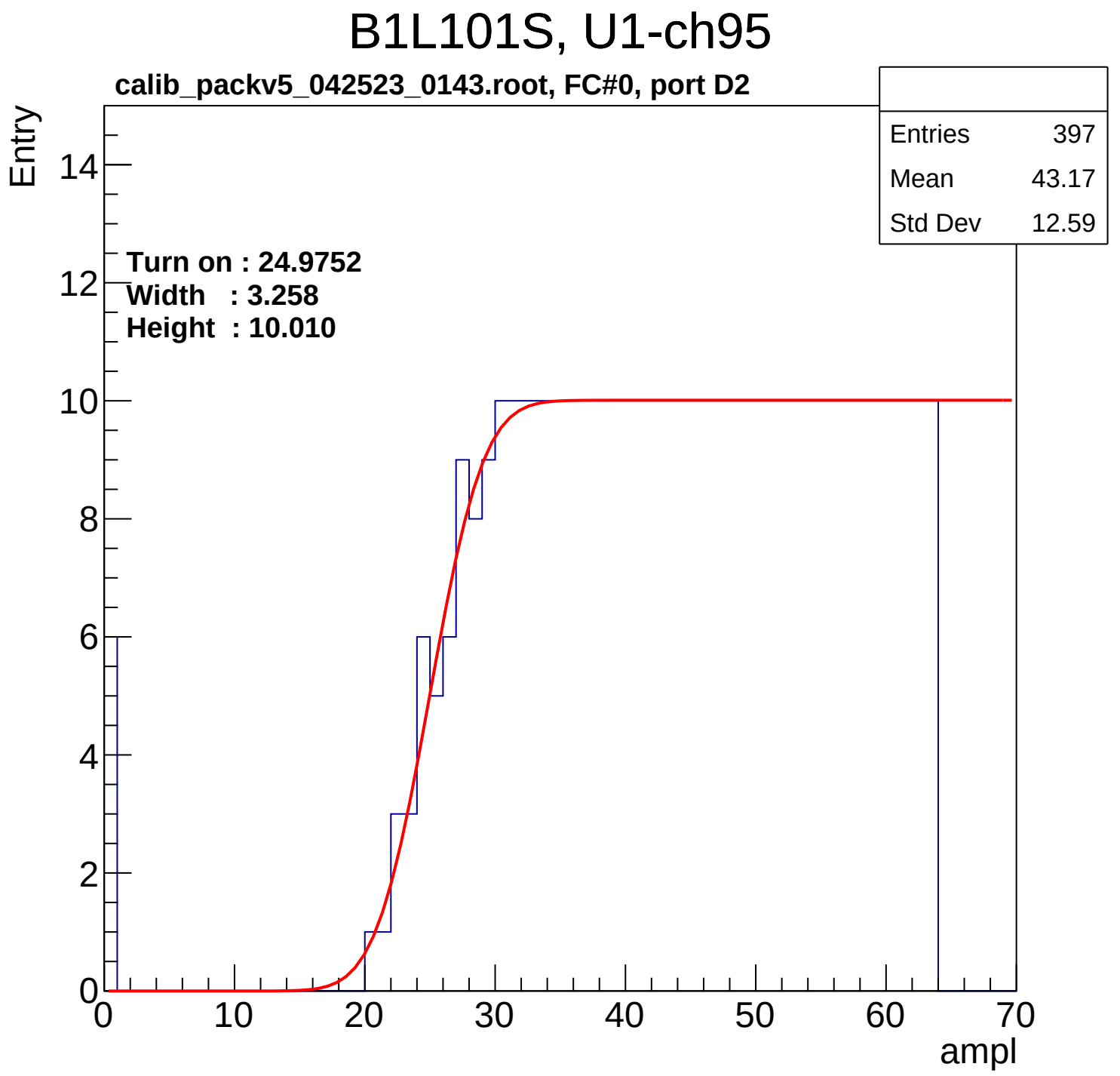
B1L101S, U1-ch95
calib_packv5_042523_0143.root, FC#0, port D2
Entries 397
Mean 43.17
Std Dev 12.59
Turn on : 24.9752
Width : 3.258
Height : 10.010
Entry
ampl
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4
6
8
10
12
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0
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20
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60
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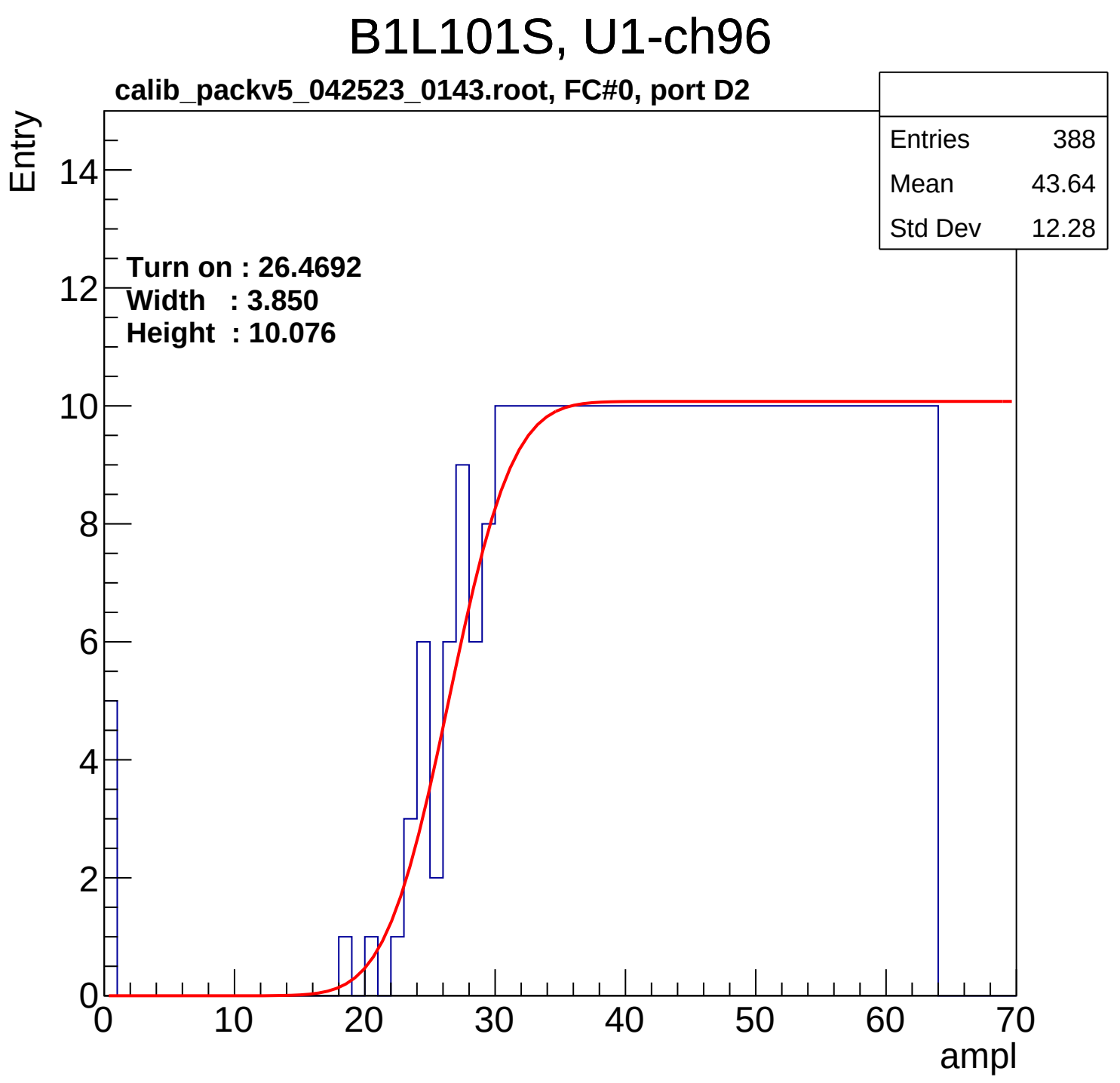
B1L101S, U1-ch96
calib_packv5_042523_0143.root, FC#0, port D2
Entries 388
Mean 43.64
Std Dev 12.28
Turn on : 26.4692
Width : 3.850
Height : 10.076
Entry
ampl
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2
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6
8
10
12
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0
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60
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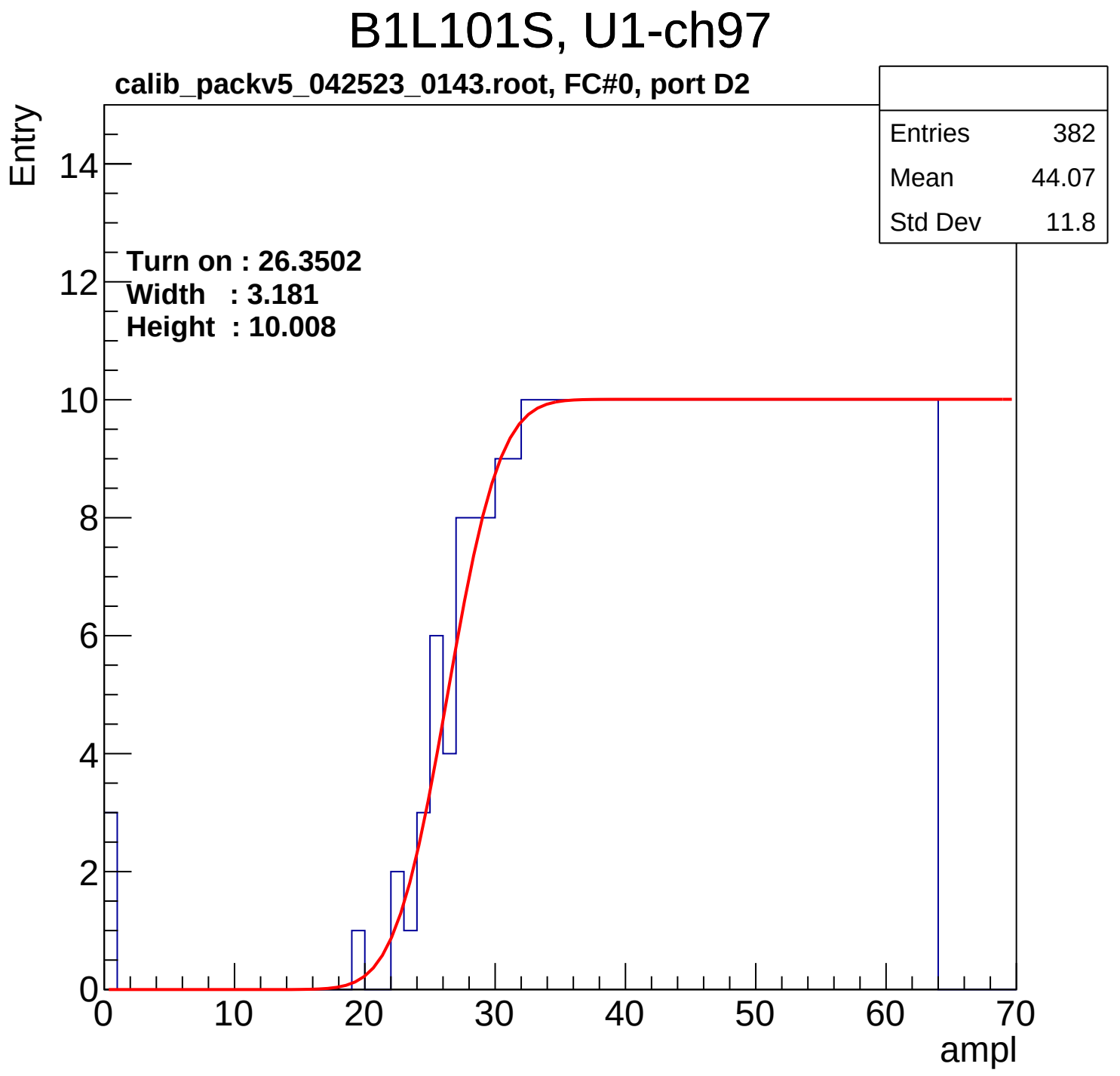
B1L101S, U1-ch97
calib_packv5_042523_0143.root, FC#0, port D2
Entries 382
Mean 44.07
Std Dev 11.8
Turn on : 26.3502
Width : 3.181
Height : 10.008
Entry
ampl
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2
4
6
8
10
12
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0
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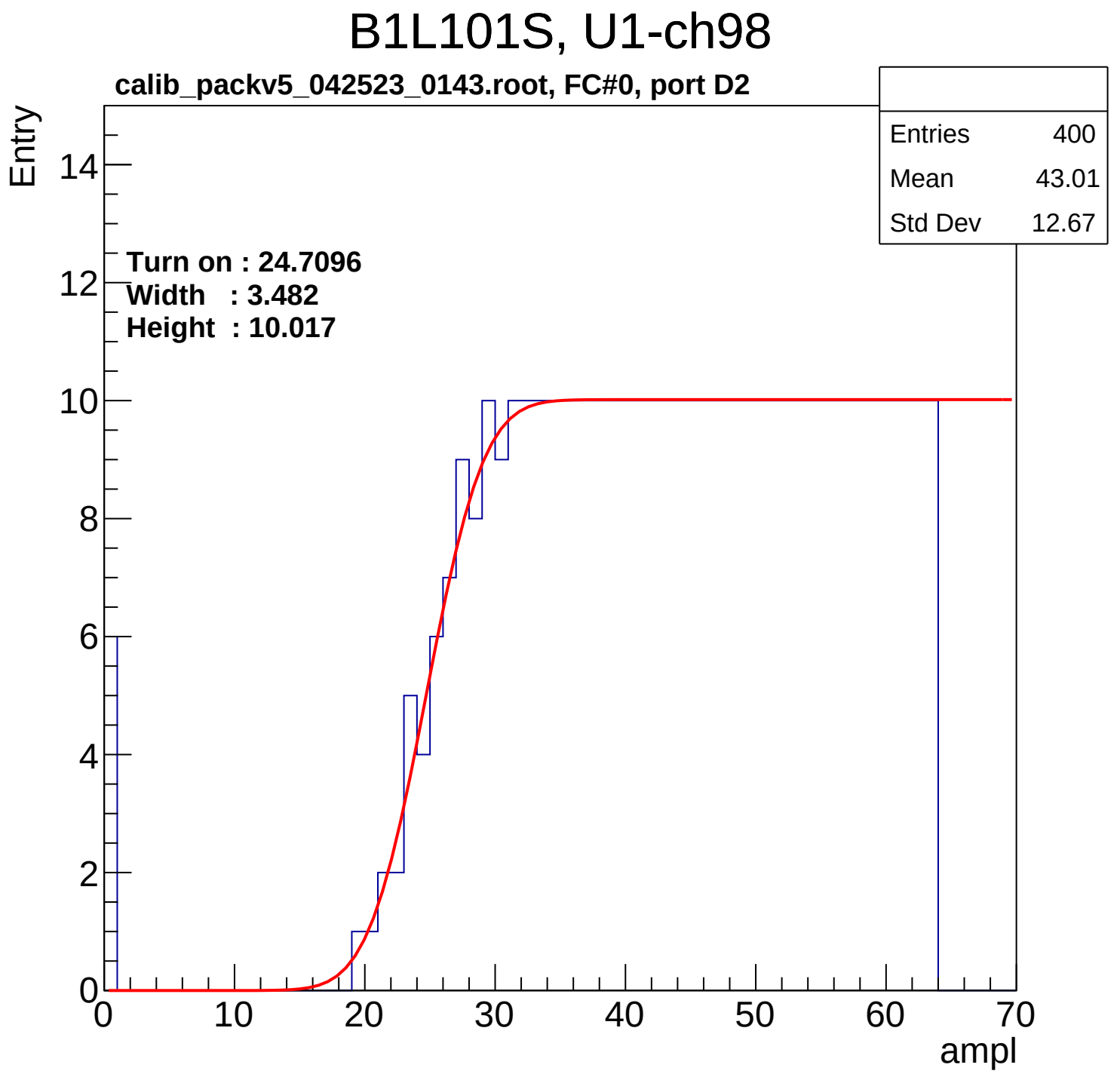
B1L101S, U1-ch98
calib_packv5_042523_0143.root, FC#0, port D2
Entries 400
Mean 43.01
Std Dev 12.67
Turn on : 24.7096
Width : 3.482
Height : 10.017
Entry
ampl
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4
6
8
10
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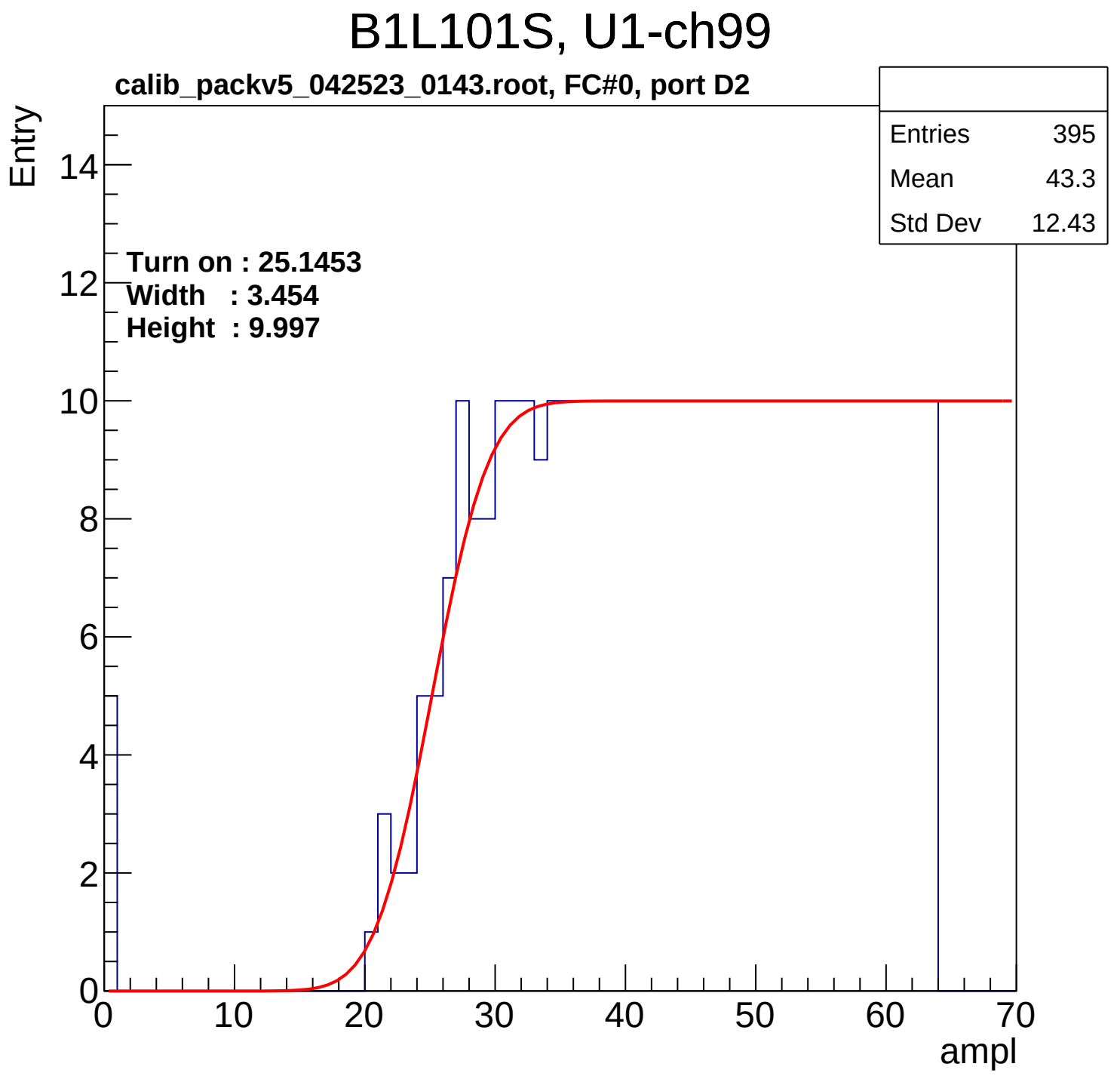
B1L101S, U1-ch99
calib_packv5_042523_0143.root, FC#0, port D2
Entries 395
Mean 43.3
Std Dev 12.43
Turn on : 25.1453
Width : 3.454
Height : 9.997
Entry
ampl
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4
6
8
10
12
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0
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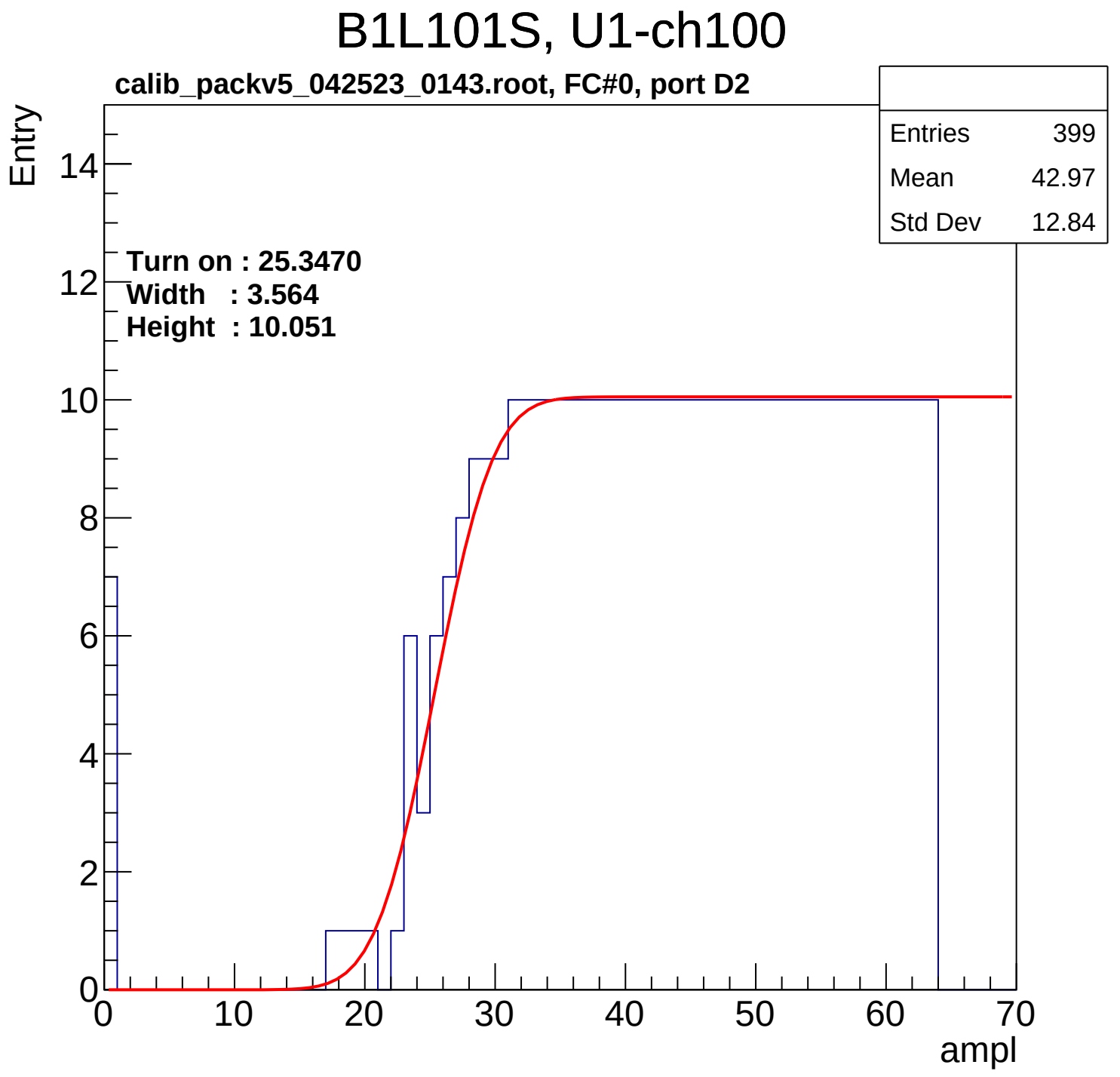
B1L101S, U1-ch100
calib_packv5_042523_0143.root, FC#0, port D2
Entries 399
Mean 42.97
Std Dev 12.84
Turn on : 25.3470
Width : 3.564
Height : 10.051
Entry
ampl
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4
6
8
10
12
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0
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20
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60
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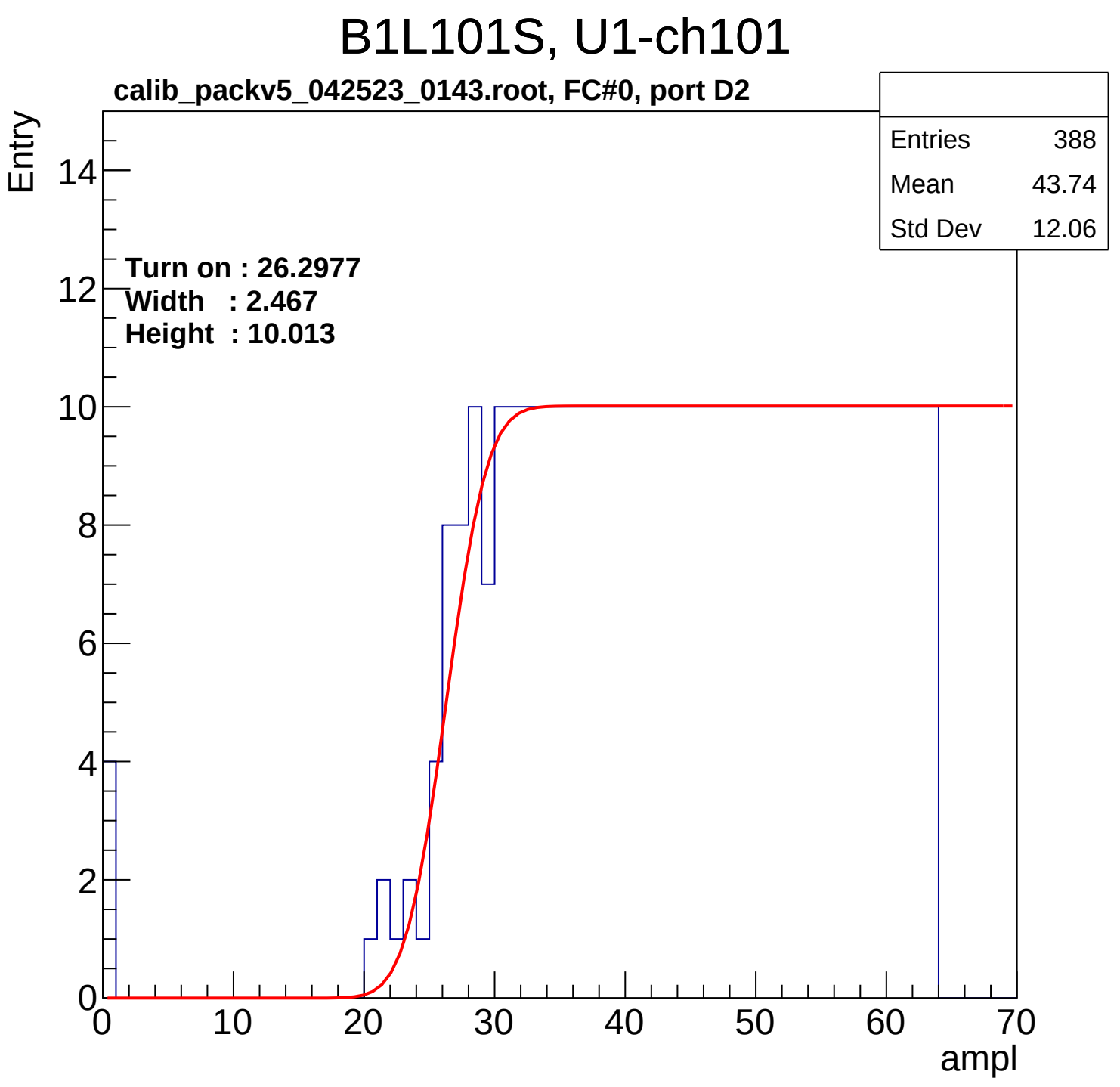
B1L101S, U1-ch101
calib_packv5_042523_0143.root, FC#0, port D2
Entries 388
Mean 43.74
Std Dev 12.06
Turn on : 26.2977
Width : 2.467
Height : 10.013
Entry
ampl
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6
8
10
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0
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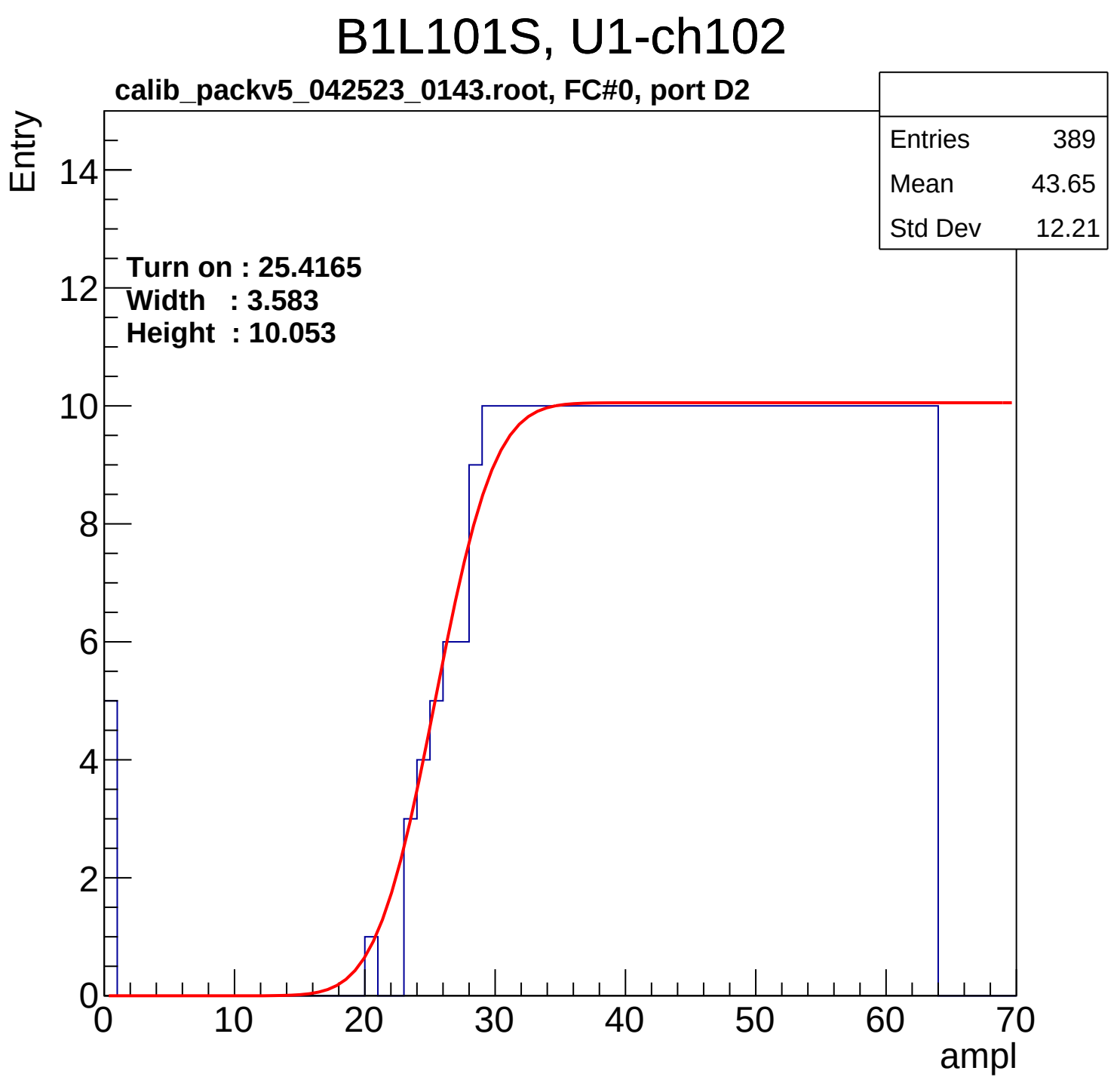
B1L101S, U1-ch102
calib_packv5_042523_0143.root, FC#0, port D2
Entries 389
Mean 43.65
Std Dev 12.21
Turn on : 25.4165
Width : 3.583
Height : 10.053
Entry
ampl
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8
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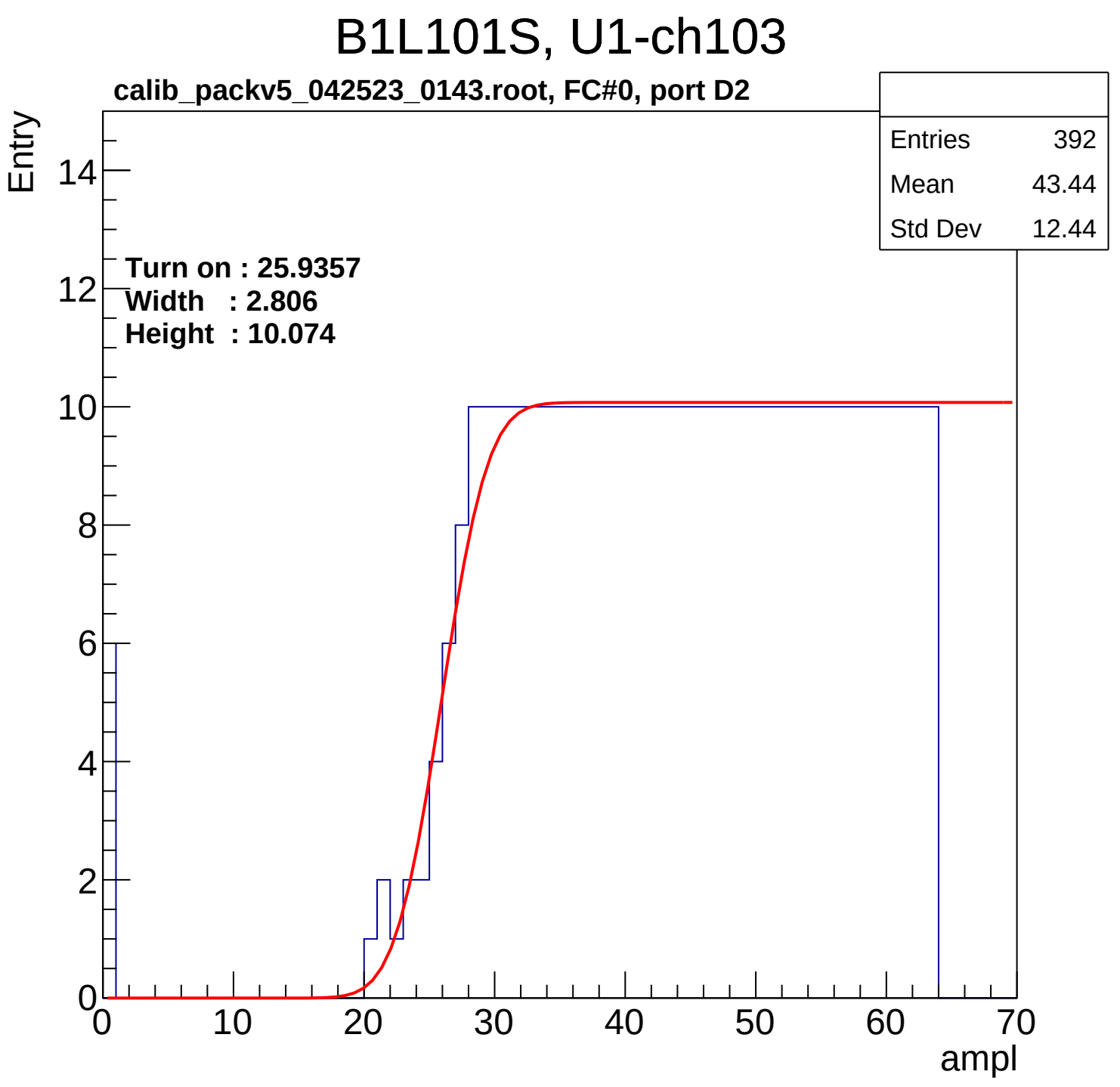
B1L101S, U1-ch103
calib_packv5_042523_0143.root, FC#0, port D2
Entries 392
Mean 43.44
Std Dev 12.44
Turn on : 25.9357
Width : 2.806
Height : 10.074
Entry
ampl
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8
10
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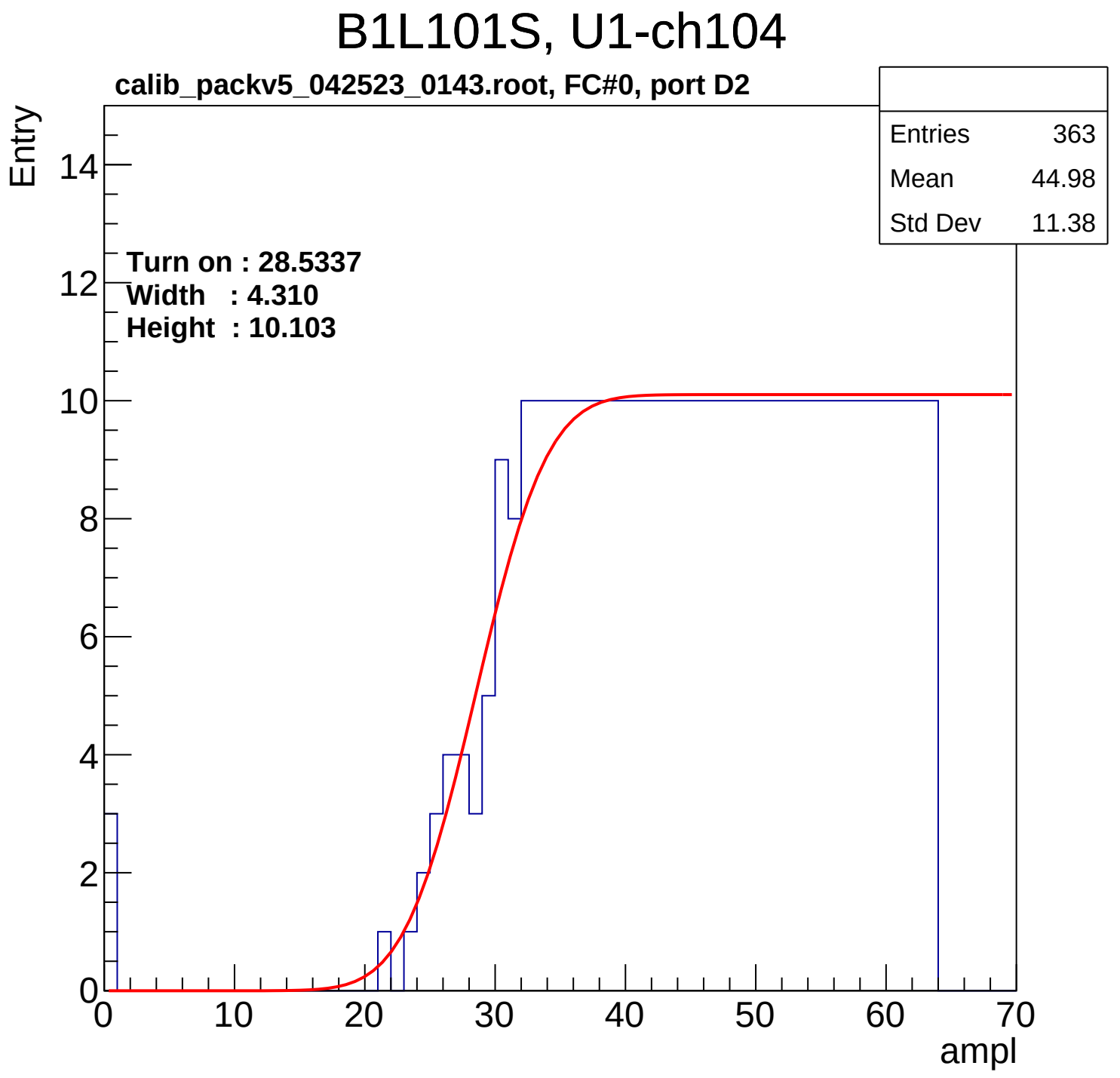
B1L101S, U1-ch104
calib_packv5_042523_0143.root, FC#0, port D2
Entries 363
Mean 44.98
Std Dev 11.38
Turn on : 28.5337
Width : 4.310
Height : 10.103
Entry
ampl
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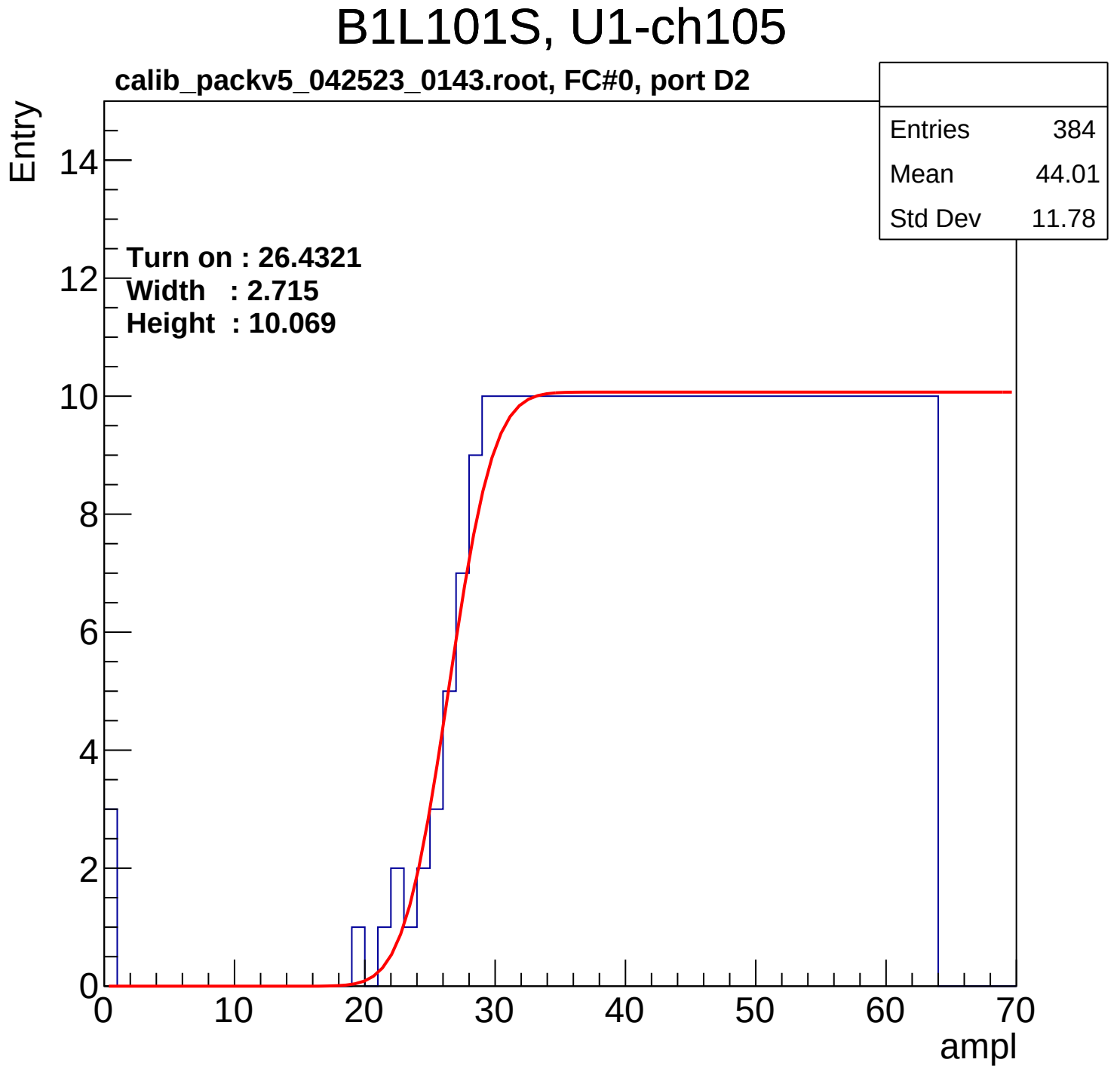
B1L101S, U1-ch105
calib_packv5_042523_0143.root, FC#0, port D2
Entries 384
Mean 44.01
Std Dev 11.78
Turn on : 26.4321
Width : 2.715
Height : 10.069
Entry
ampl
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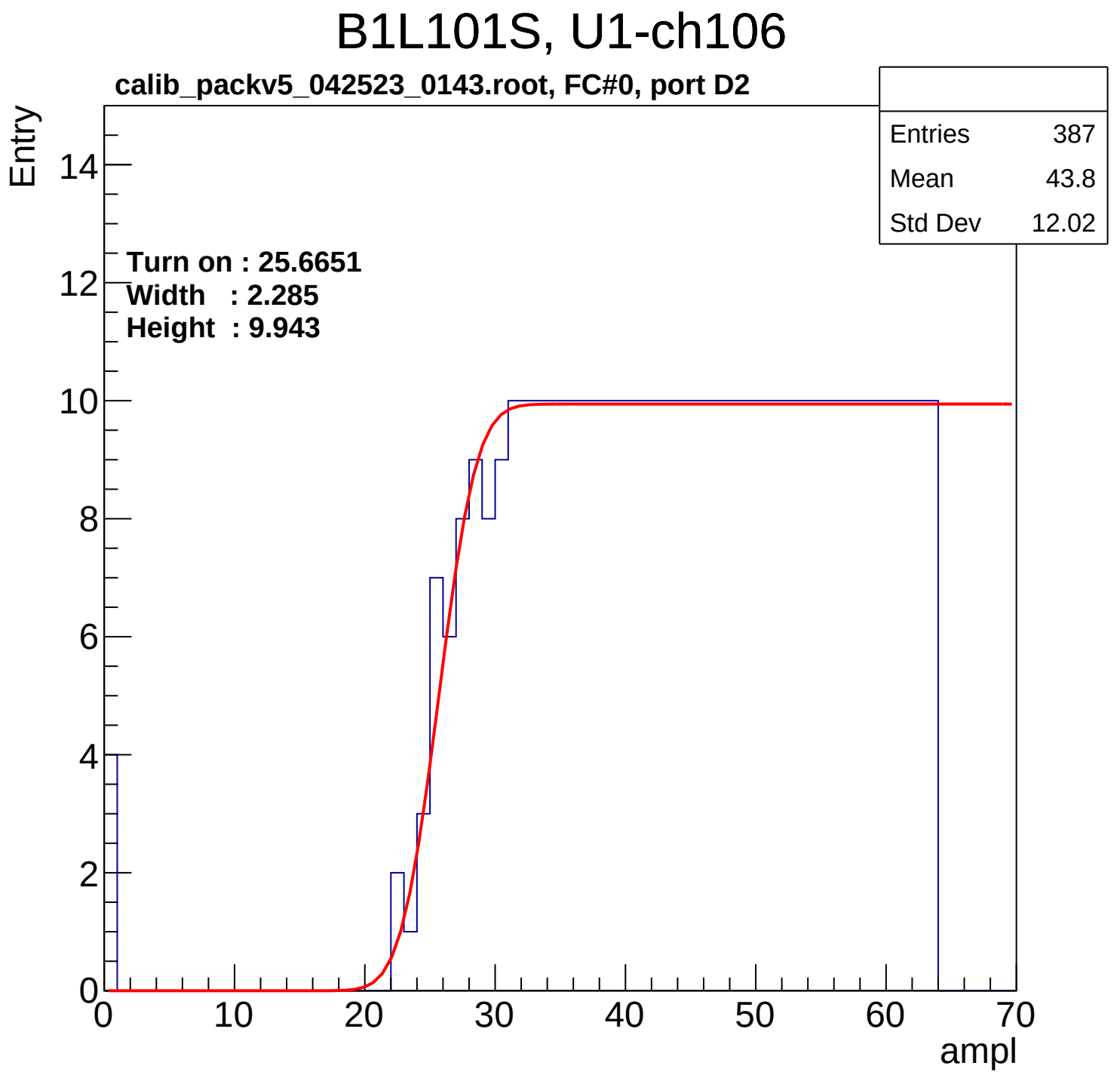
B1L101S, U1-ch106
calib_packv5_042523_0143.root, FC#0, port D2
Entries 387
Mean 43.8
Std Dev 12.02
Turn on : 25.6651
Width : 2.285
Height : 9.943
Entry
ampl
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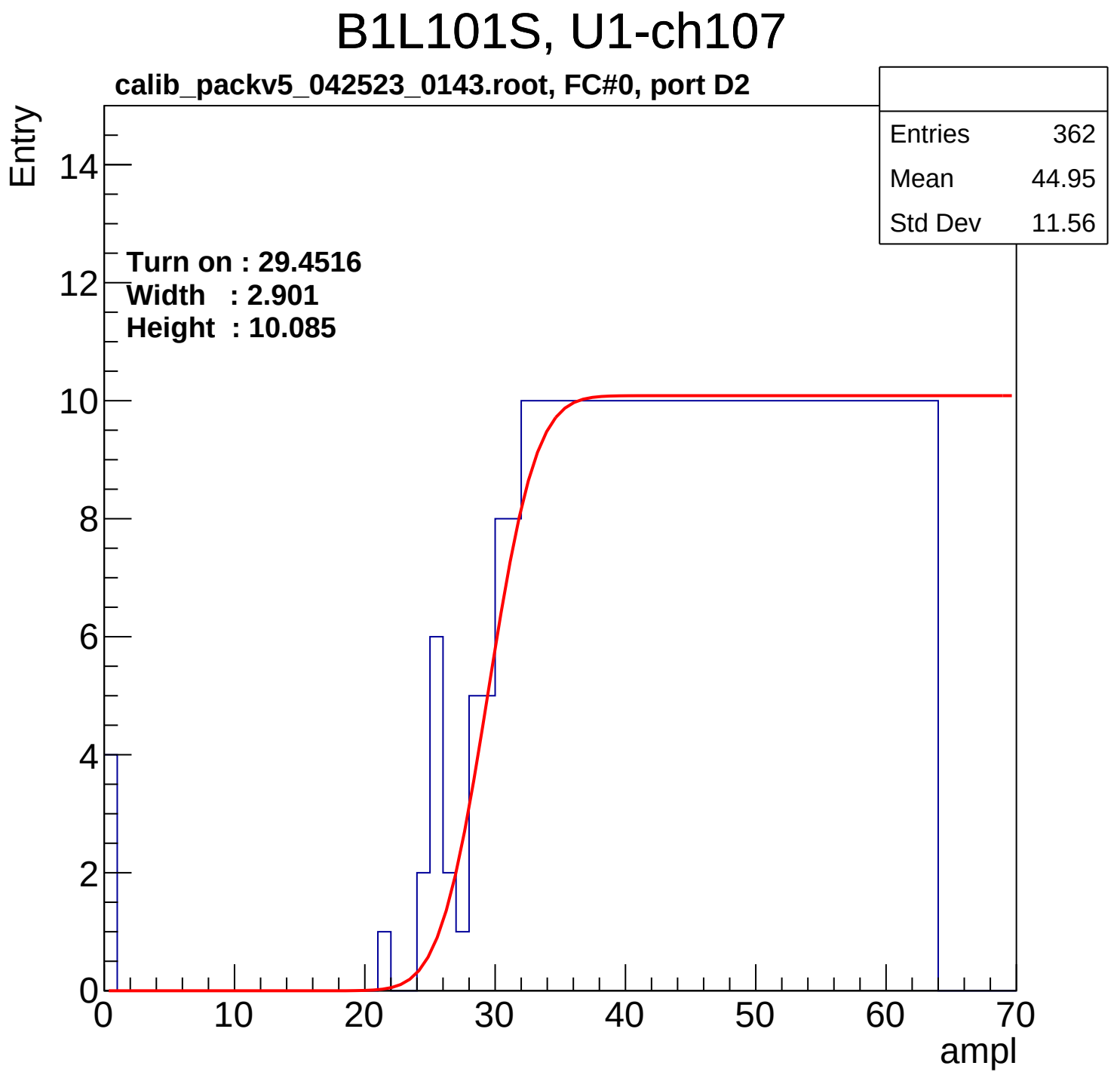
B1L101S, U1-ch107
calib_packv5_042523_0143.root, FC#0, port D2
Entries 362
Mean 44.95
Std Dev 11.56
Turn on : 29.4516
Width : 2.901
Height : 10.085
Entry
ampl
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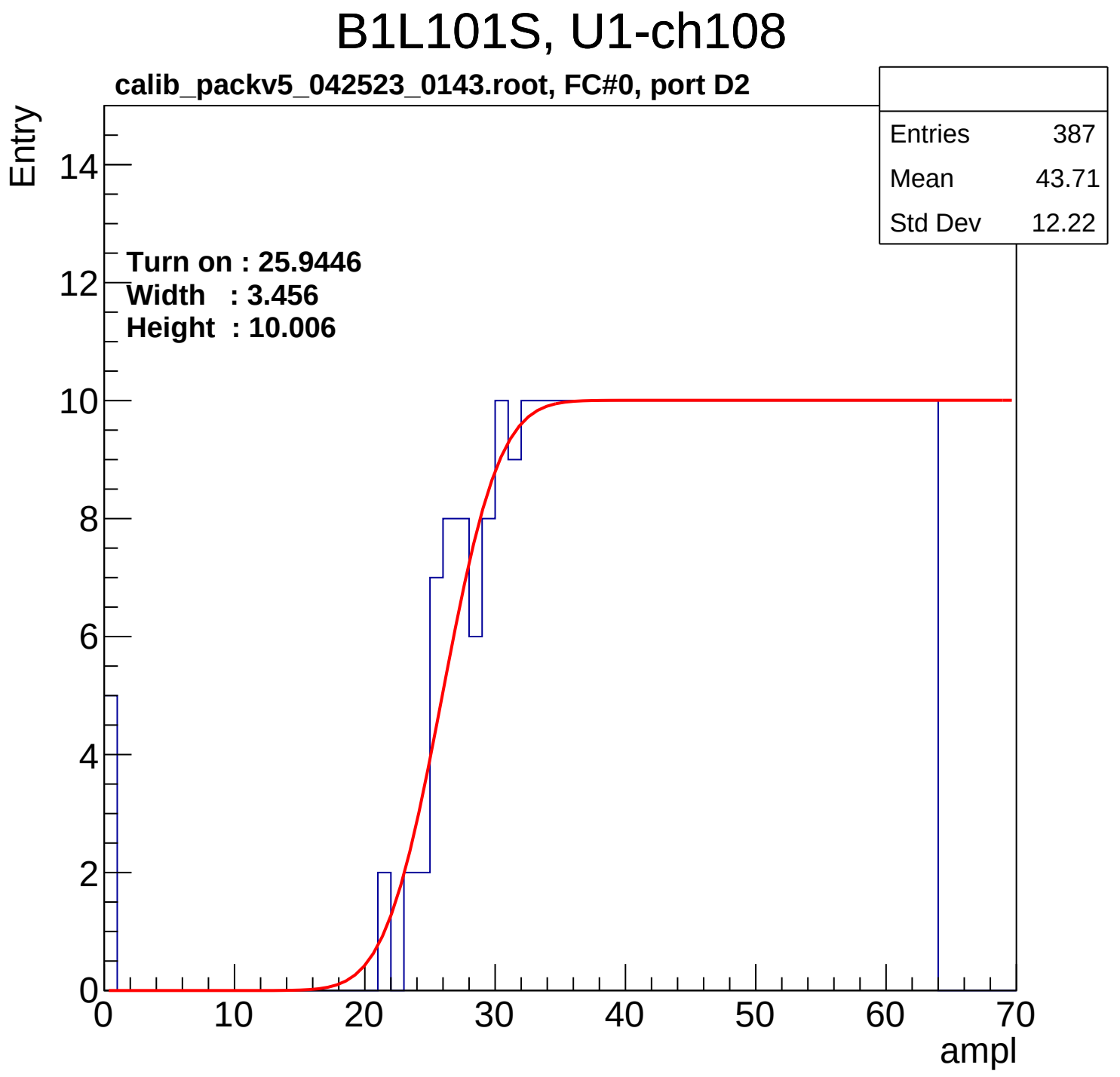
B1L101S, U1-ch108
calib_packv5_042523_0143.root, FC#0, port D2
Entries 387
Mean 43.71
Std Dev 12.22
Turn on : 25.9446
Width : 3.456
Height : 10.006
Entry
ampl
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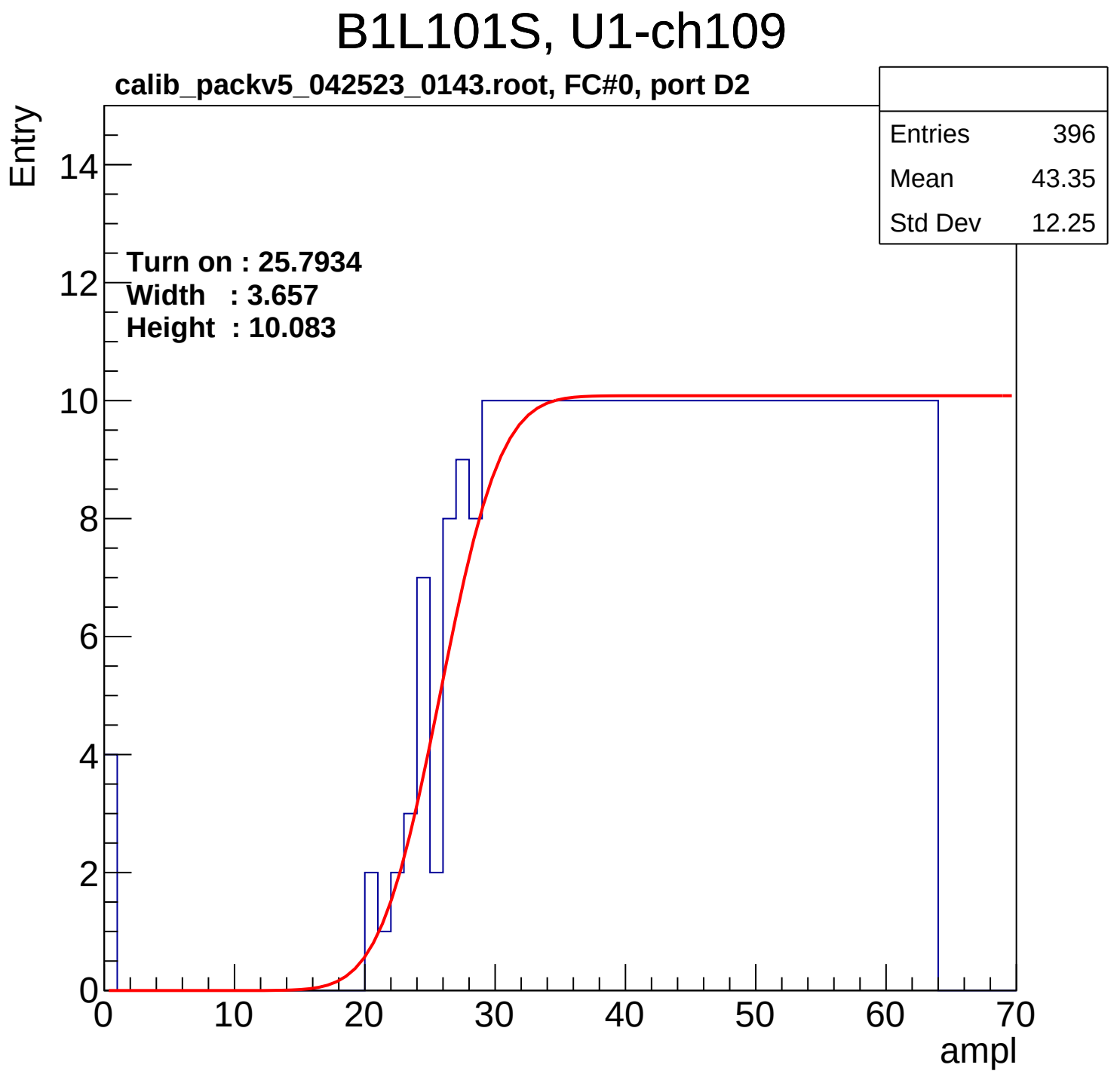
B1L101S, U1-ch109
calib_packv5_042523_0143.root, FC#0, port D2
Entries 396
Mean 43.35
Std Dev 12.25
Turn on : 25.7934
Width : 3.657
Height : 10.083
Entry
ampl
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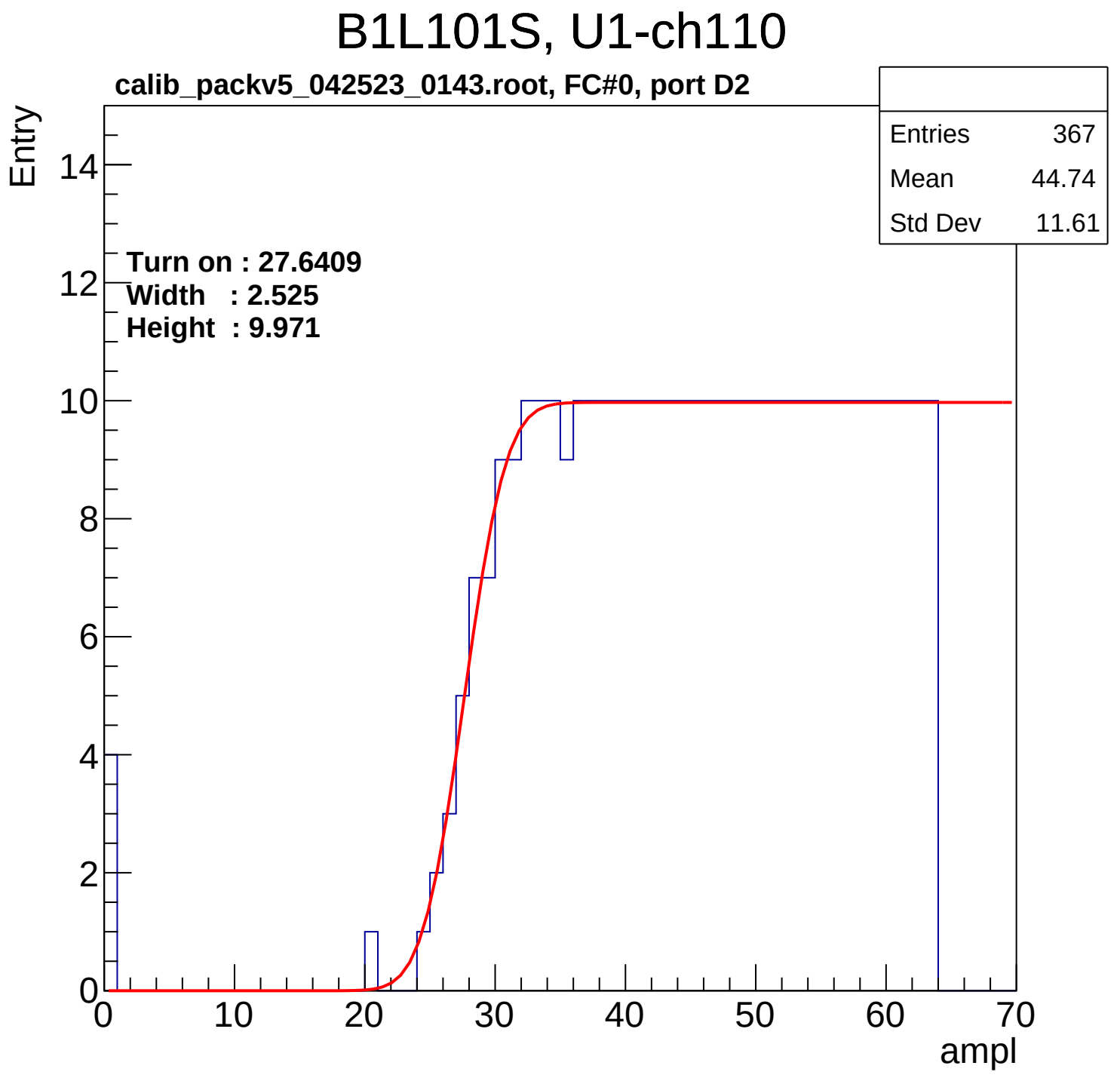
B1L101S, U1-ch110
calib_packv5_042523_0143.root, FC#0, port D2
Entries 367
Mean 44.74
Std Dev 11.61
Turn on : 27.6409
Width : 2.525
Height : 9.971
Entry
ampl
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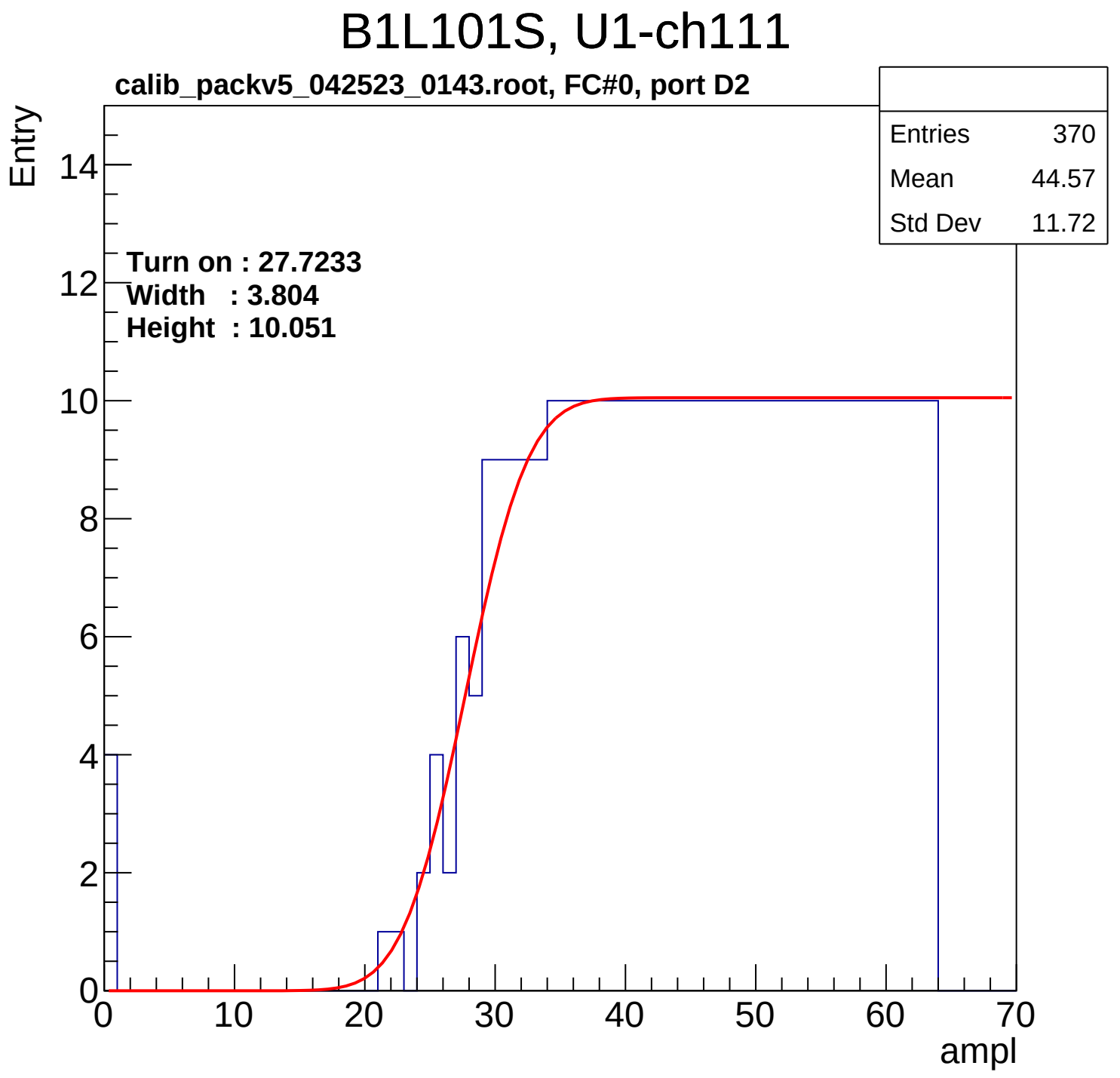
B1L101S, U1-ch111
calib_packv5_042523_0143.root, FC#0, port D2
Entries 370
Mean 44.57
Std Dev 11.72
Turn on : 27.7233
Width : 3.804
Height : 10.051
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ampl
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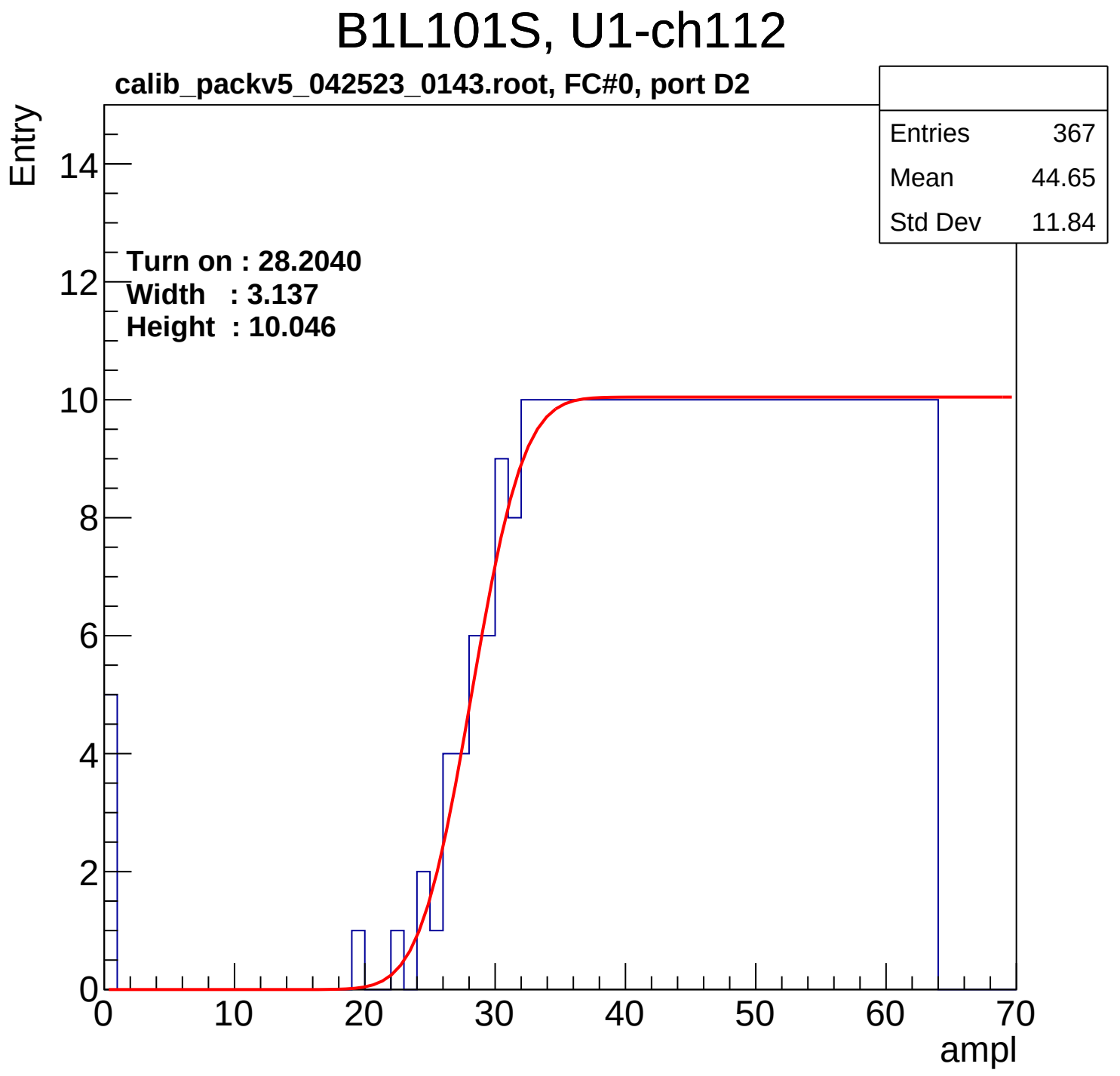
B1L101S, U1-ch112
calib_packv5_042523_0143.root, FC#0, port D2
Entries 367
Mean 44.65
Std Dev 11.84
Turn on : 28.2040
Width : 3.137
Height : 10.046
Entry
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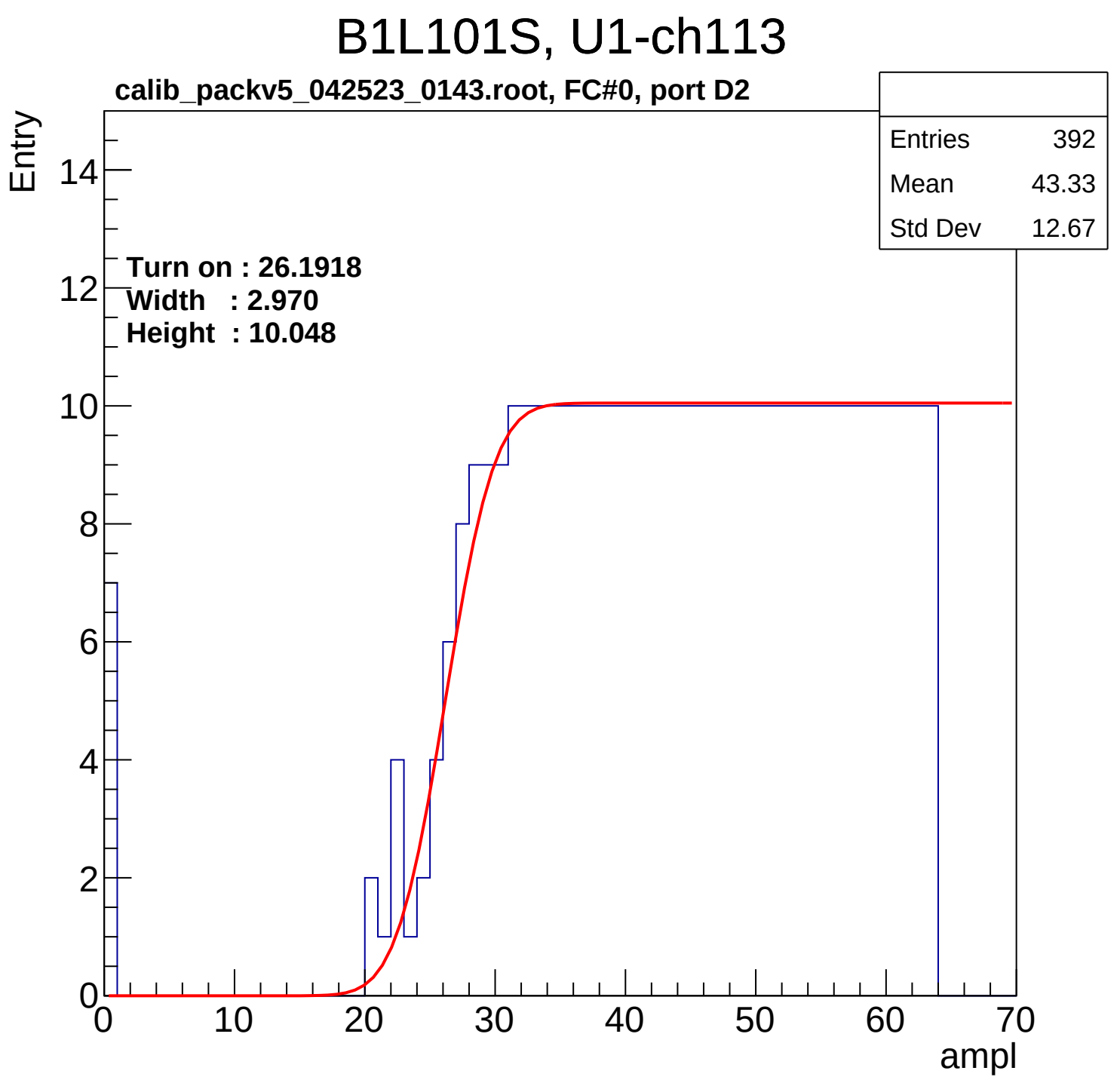
B1L101S, U1-ch113
calib_packv5_042523_0143.root, FC#0, port D2
Entries 392
Mean 43.33
Std Dev 12.67
Turn on : 26.1918
Width : 2.970
Height : 10.048
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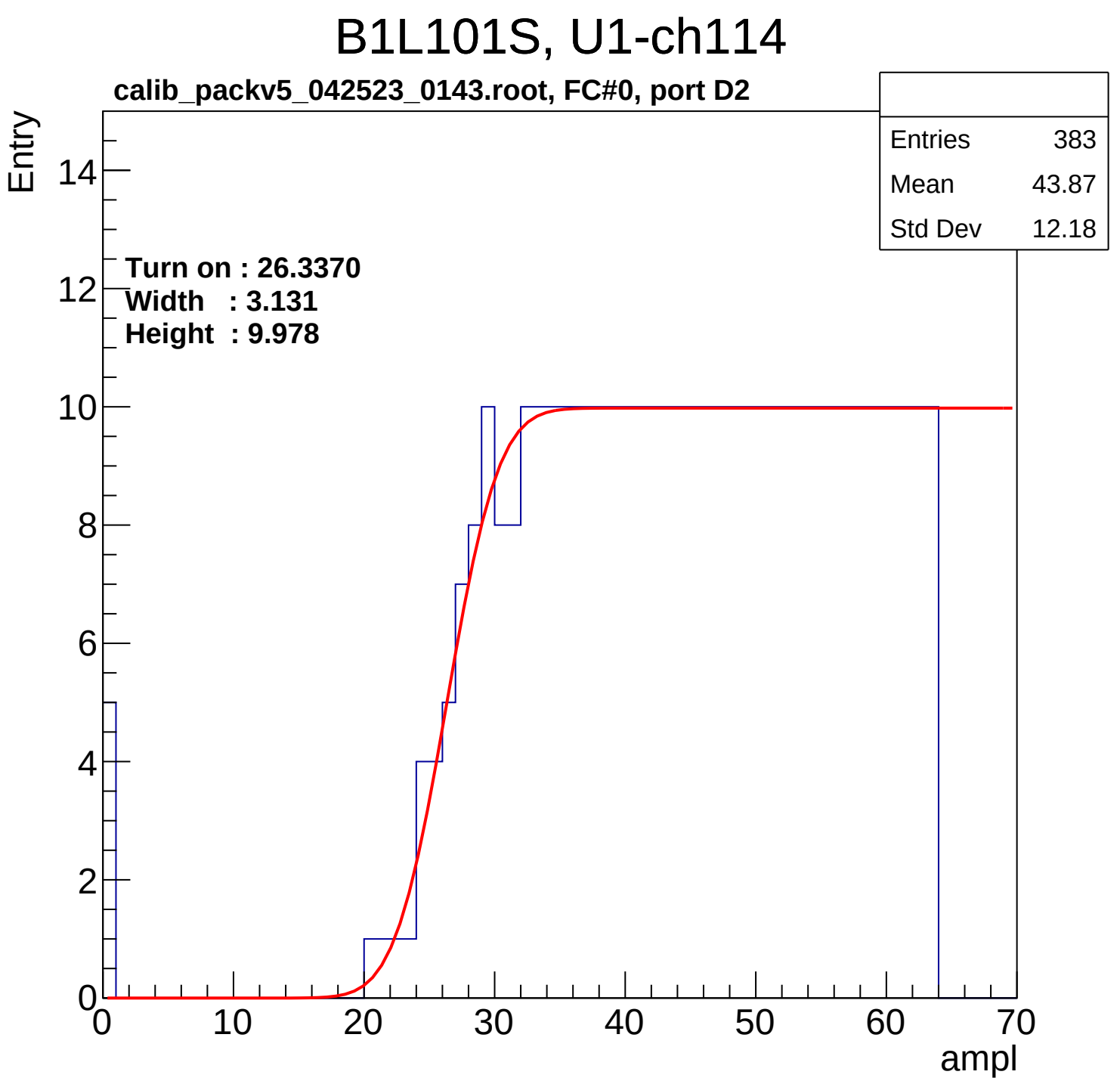
B1L101S, U1-ch114
calib_packv5_042523_0143.root, FC#0, port D2
Entries 383
Mean 43.87
Std Dev 12.18
Turn on : 26.3370
Width : 3.131
Height : 9.978
Entry
ampl
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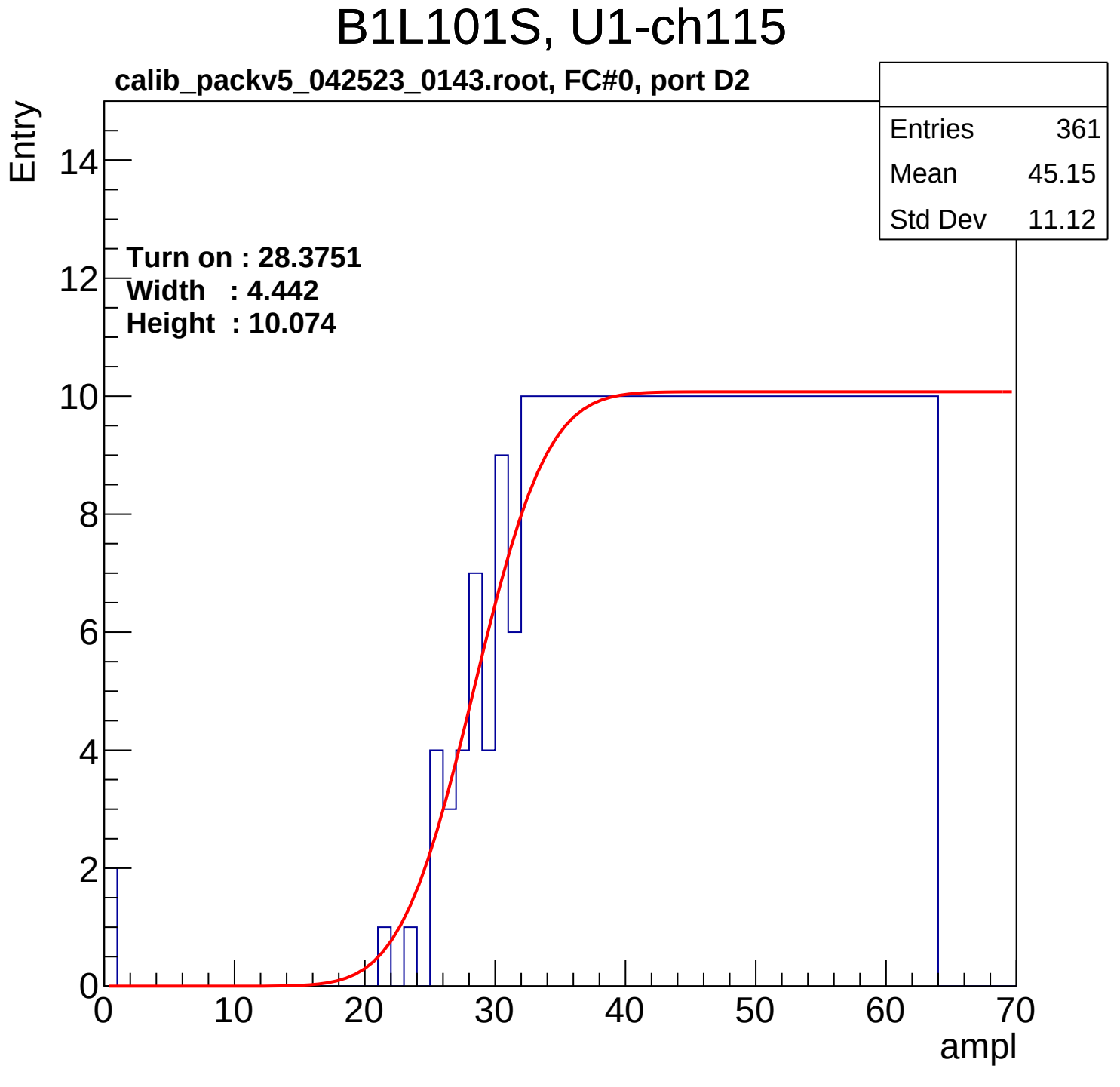
B1L101S, U1-ch115
calib_packv5_042523_0143.root, FC#0, port D2
Entries 361
Mean 45.15
Std Dev 11.12
Turn on : 28.3751
Width : 4.442
Height : 10.074
Entry
ampl
0
2
4
6
8
10
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14
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20
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40
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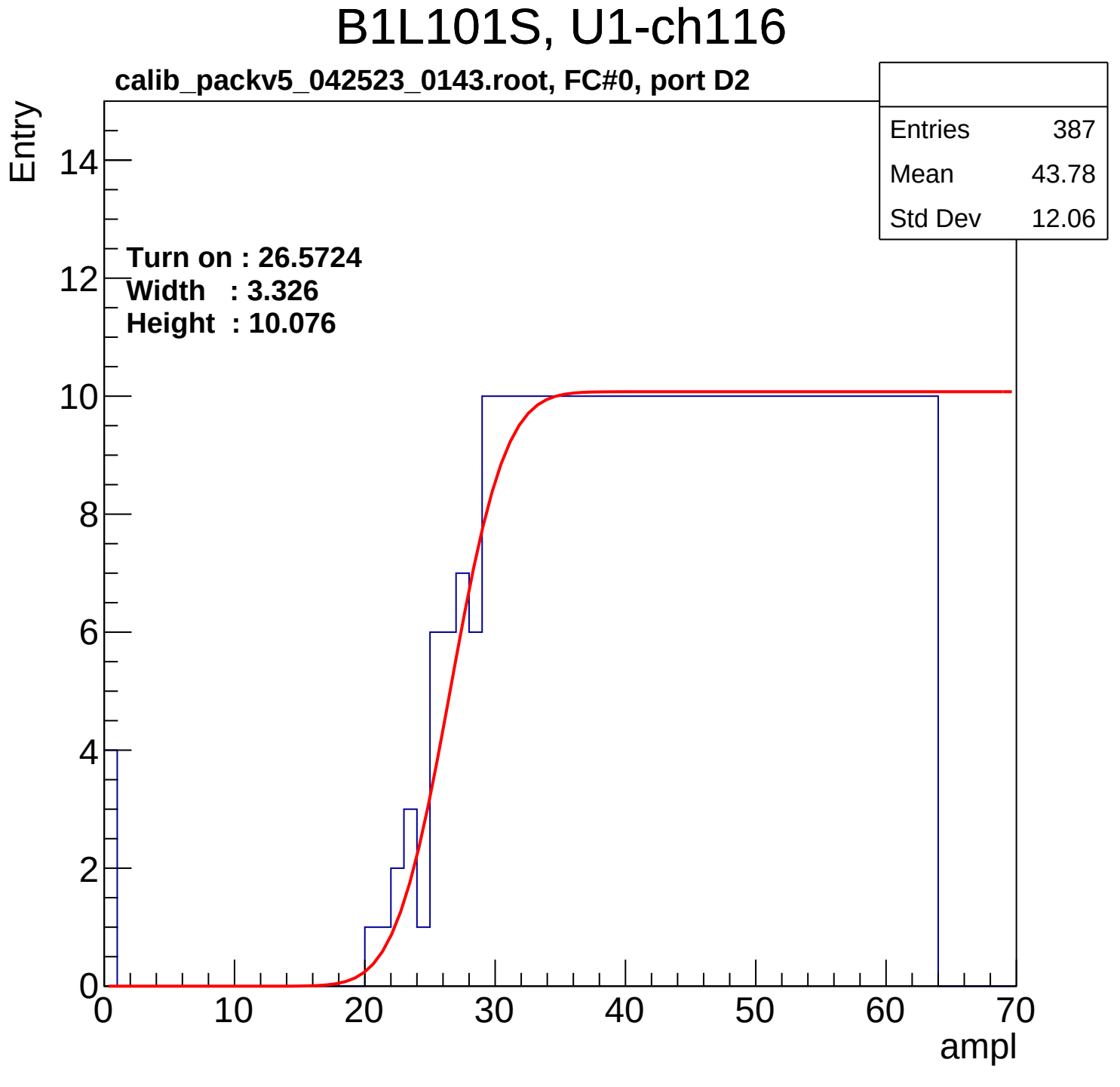
B1L101S, U1-ch116
calib_packv5_042523_0143.root, FC#0, port D2
Entries 387
Mean 43.78
Std Dev 12.06
Turn on : 26.5724
Width : 3.326
Height : 10.076
Entry
ampl
0
2
4
6
8
10
12
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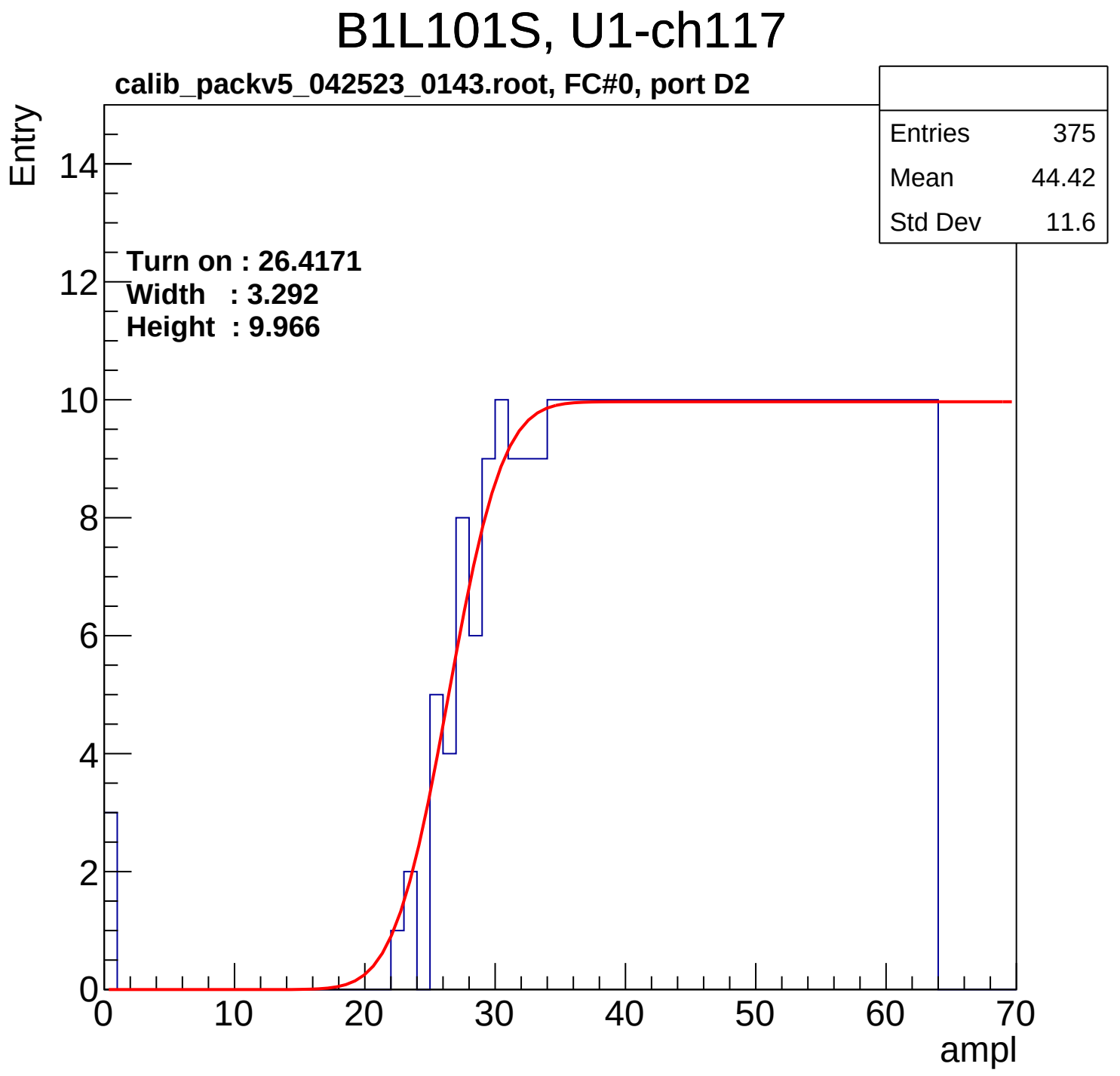
B1L101S, U1-ch117
calib_packv5_042523_0143.root, FC#0, port D2
Entries 375
Mean 44.42
Std Dev 11.6
Turn on : 26.4171
Width : 3.292
Height : 9.966
Entry
ampl
0
2
4
6
8
10
12
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0
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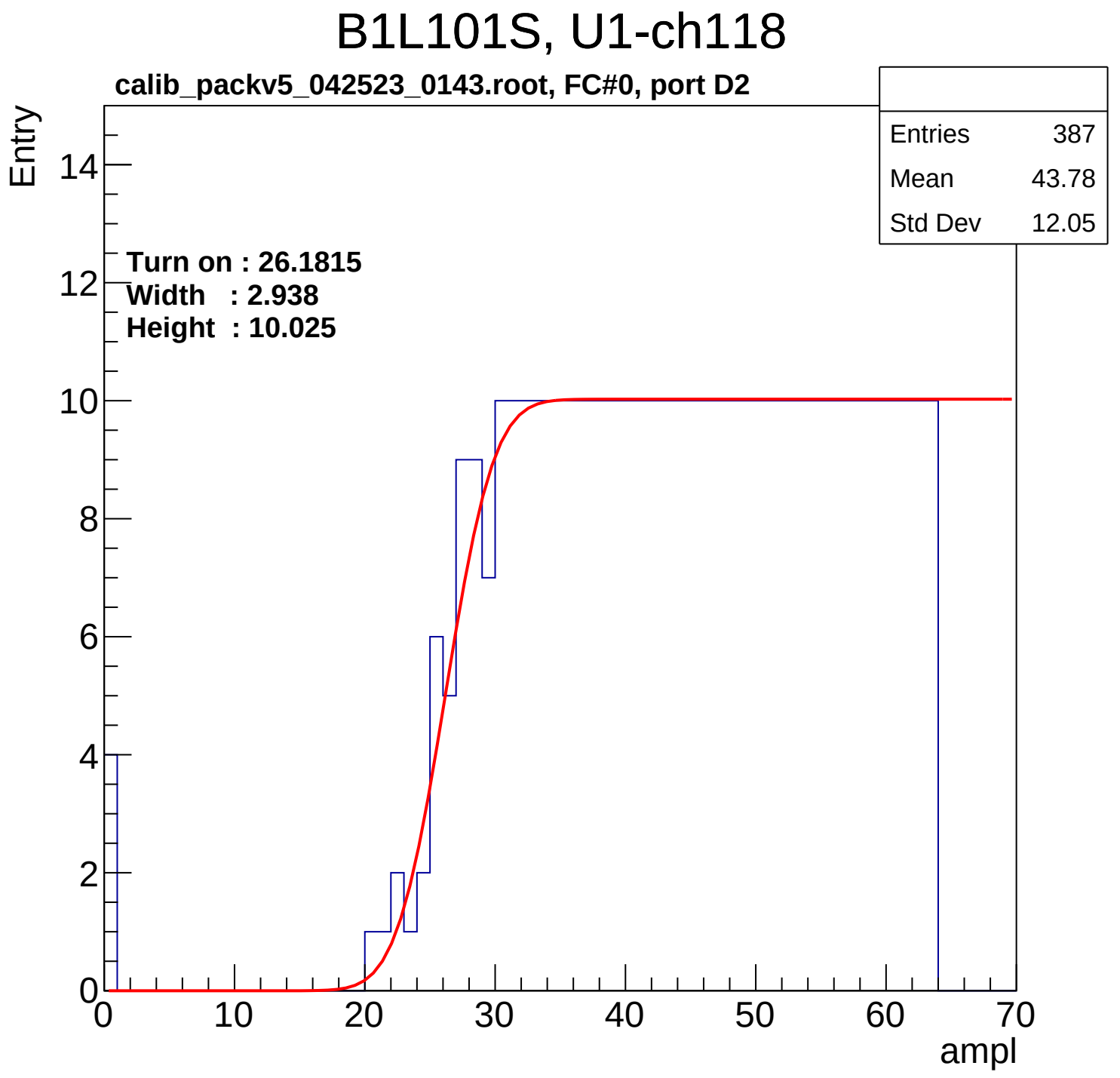
B1L101S, U1-ch118
calib_packv5_042523_0143.root, FC#0, port D2
Entries 387
Mean 43.78
Std Dev 12.05
Turn on : 26.1815
Width : 2.938
Height : 10.025
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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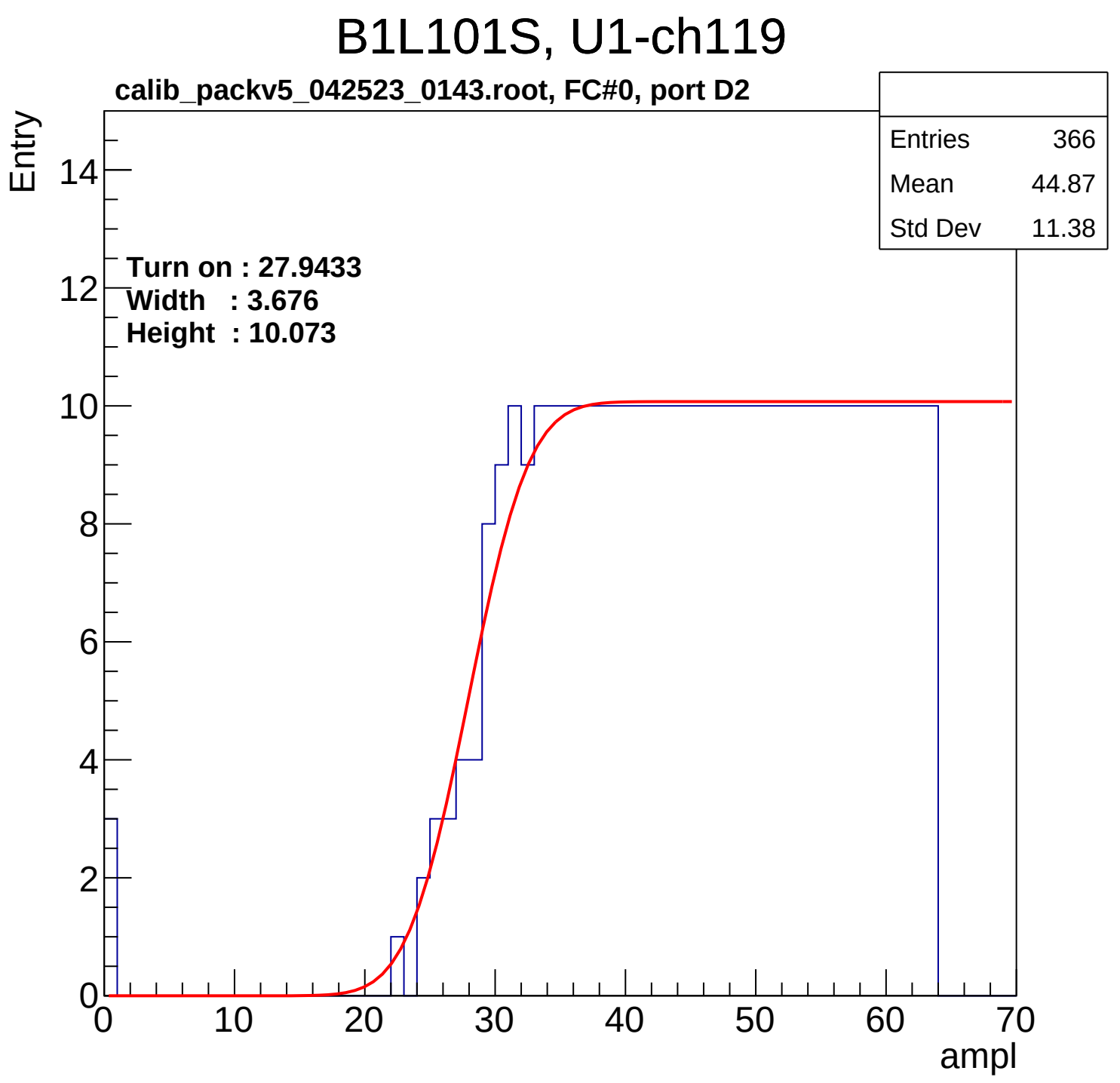
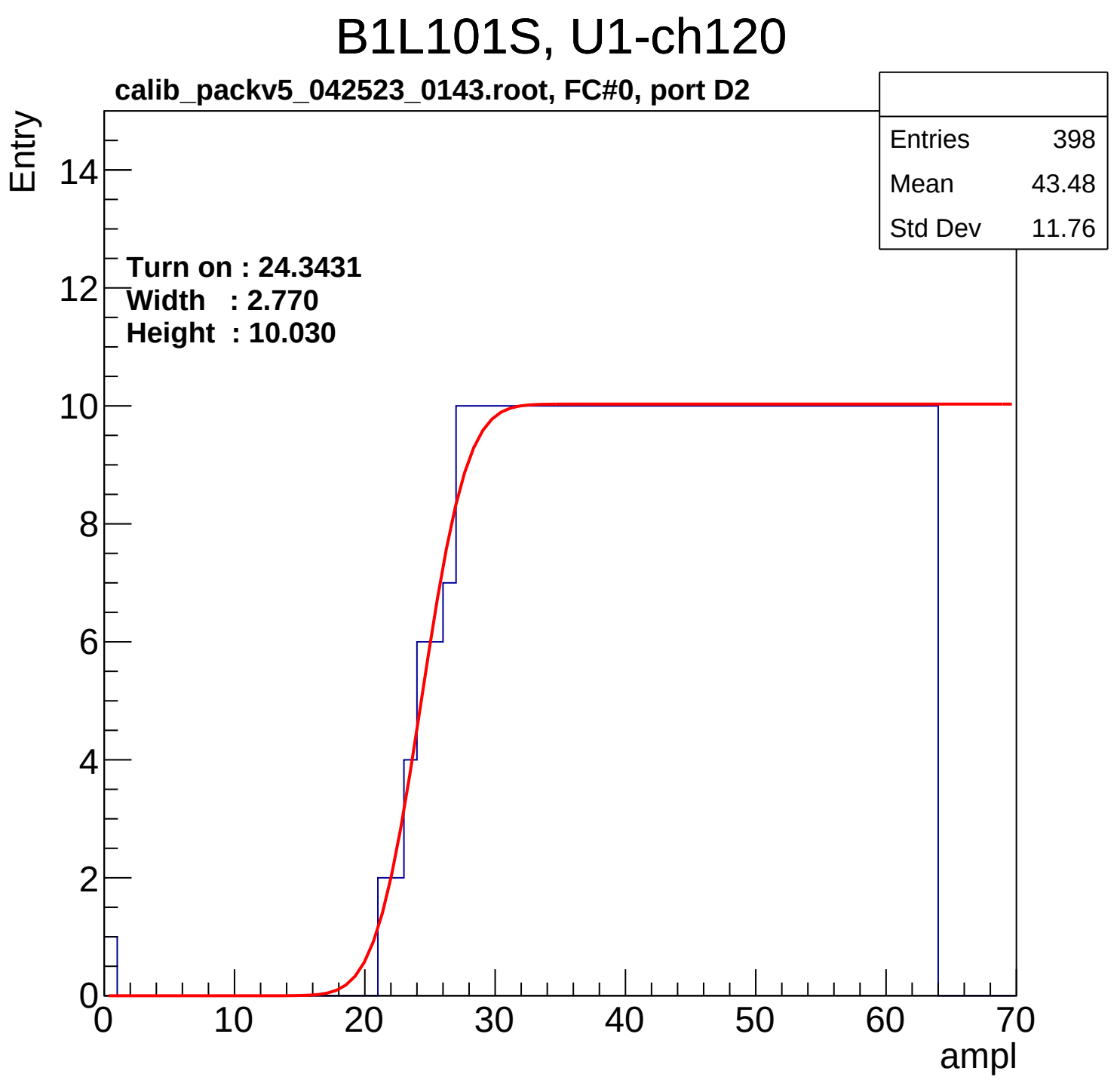

B1L101S, U1-ch119
calib_packv5_042523_0143.root, FC#0, port D2
Entries 366
Mean 44.87
Std Dev 11.38
Turn on : 27.9433
Width : 3.676
Height : 10.073
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L101S, U1-ch120
calib_packv5_042523_0143.root, FC#0, port D2
Entries 398
Mean 43.48
Std Dev 11.76
Turn on : 24.3431
Width : 2.770
Height : 10.030
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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60
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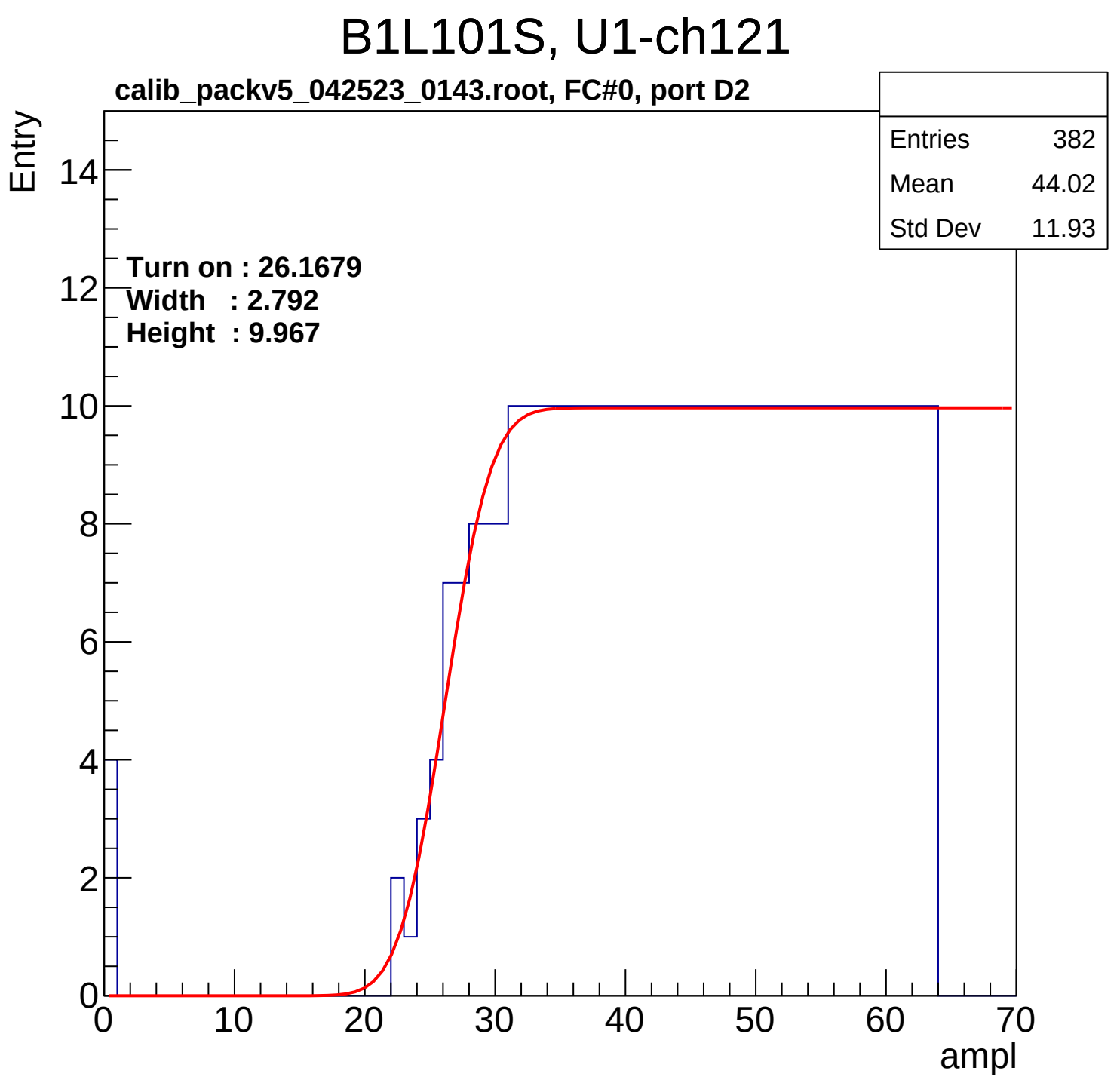
B1L101S, U1-ch121
calib_packv5_042523_0143.root, FC#0, port D2
Entries 382
Mean 44.02
Std Dev 11.93
Turn on : 26.1679
Width : 2.792
Height : 9.967
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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60
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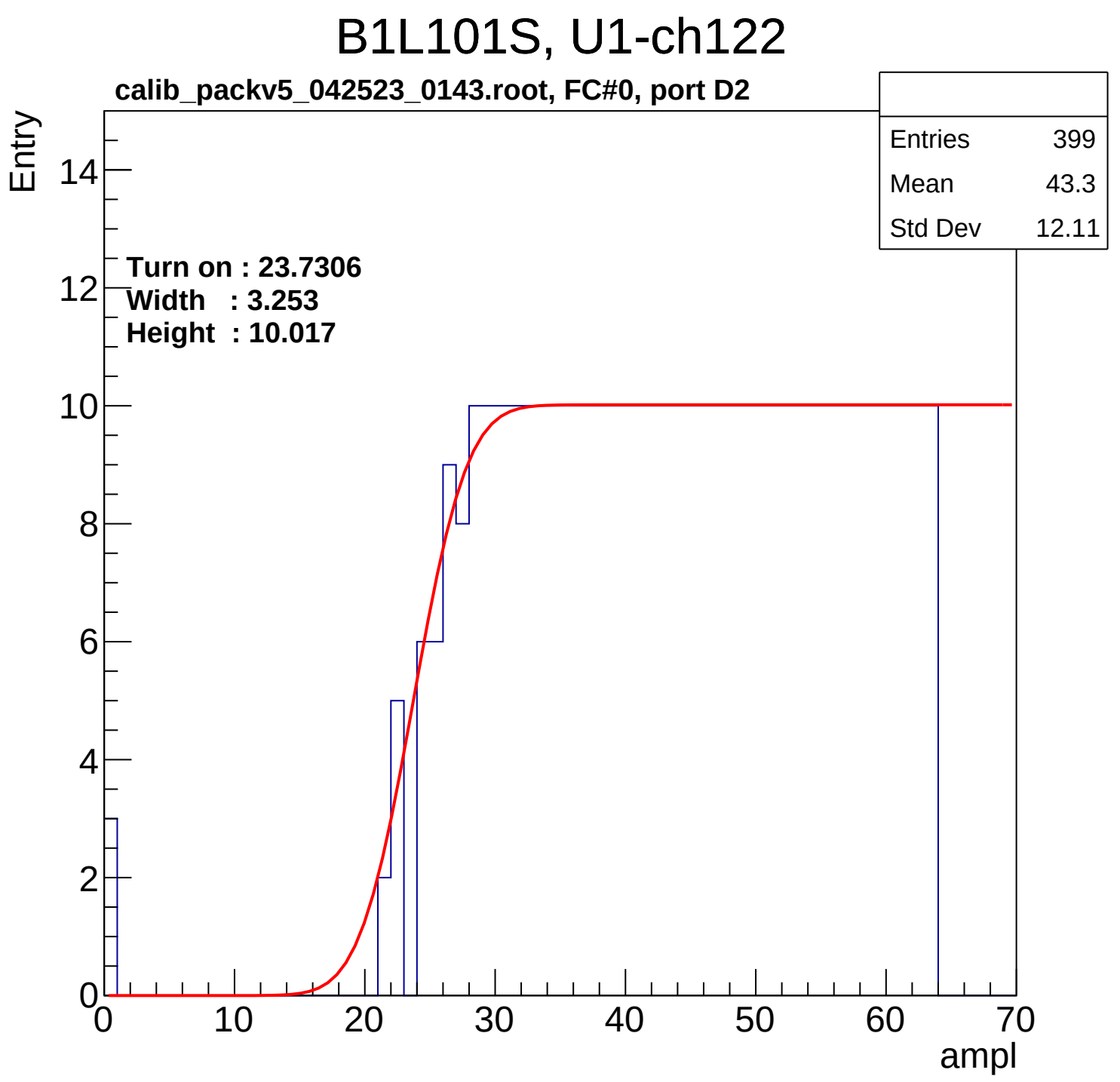
B1L101S, U1-ch122
calib_packv5_042523_0143.root, FC#0, port D2
Entries 399
Mean 43.3
Std Dev 12.11
Turn on : 23.7306
Width : 3.253
Height : 10.017
Entry
ampl
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2
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6
8
10
12
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0
10
20
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40
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60
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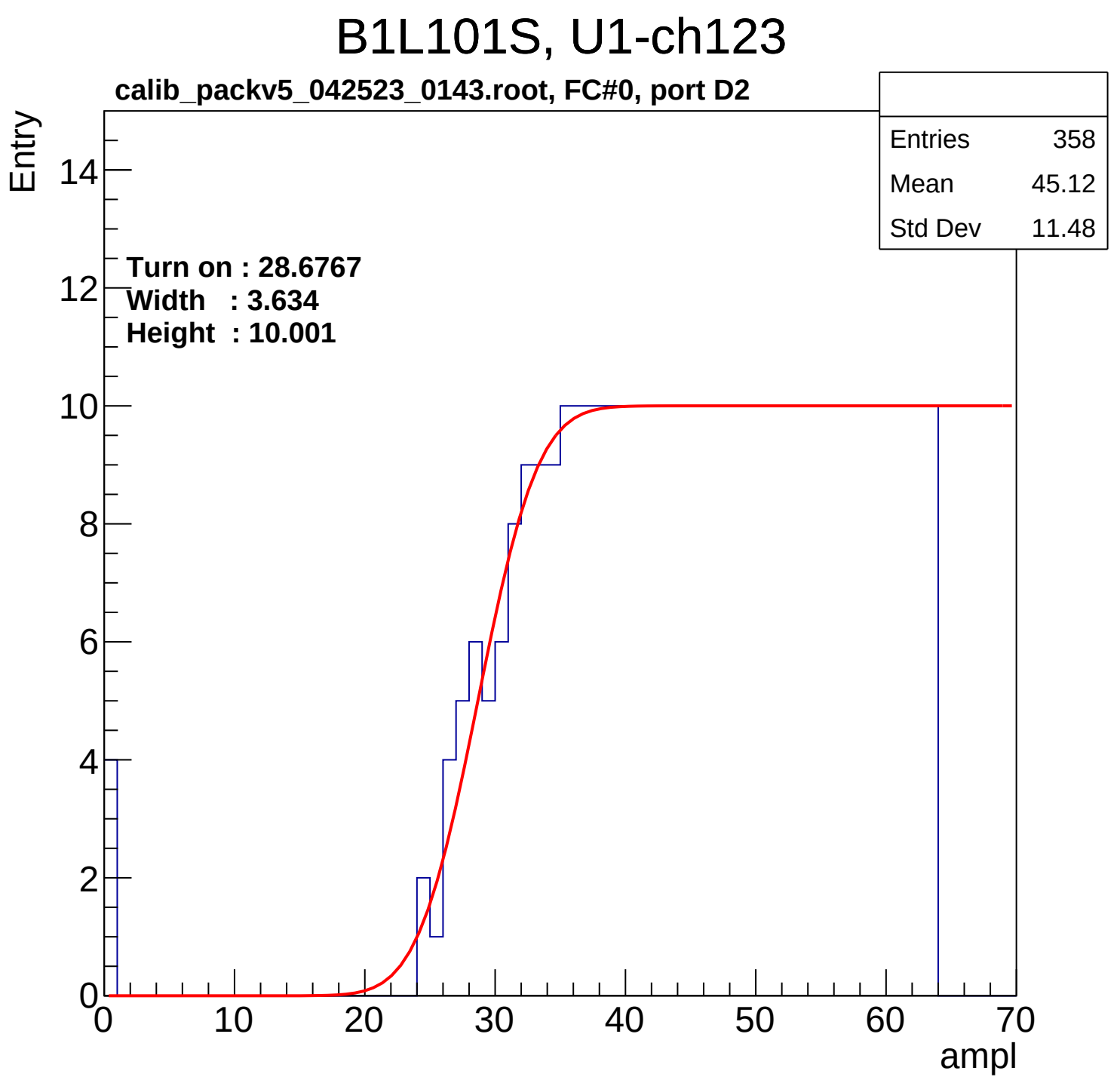
B1L101S, U1-ch123
calib_packv5_042523_0143.root, FC#0, port D2
Entries 358
Mean 45.12
Std Dev 11.48
Turn on : 28.6767
Width : 3.634
Height : 10.001
Entry
ampl
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2
4
6
8
10
12
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0
10
20
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40
50
60
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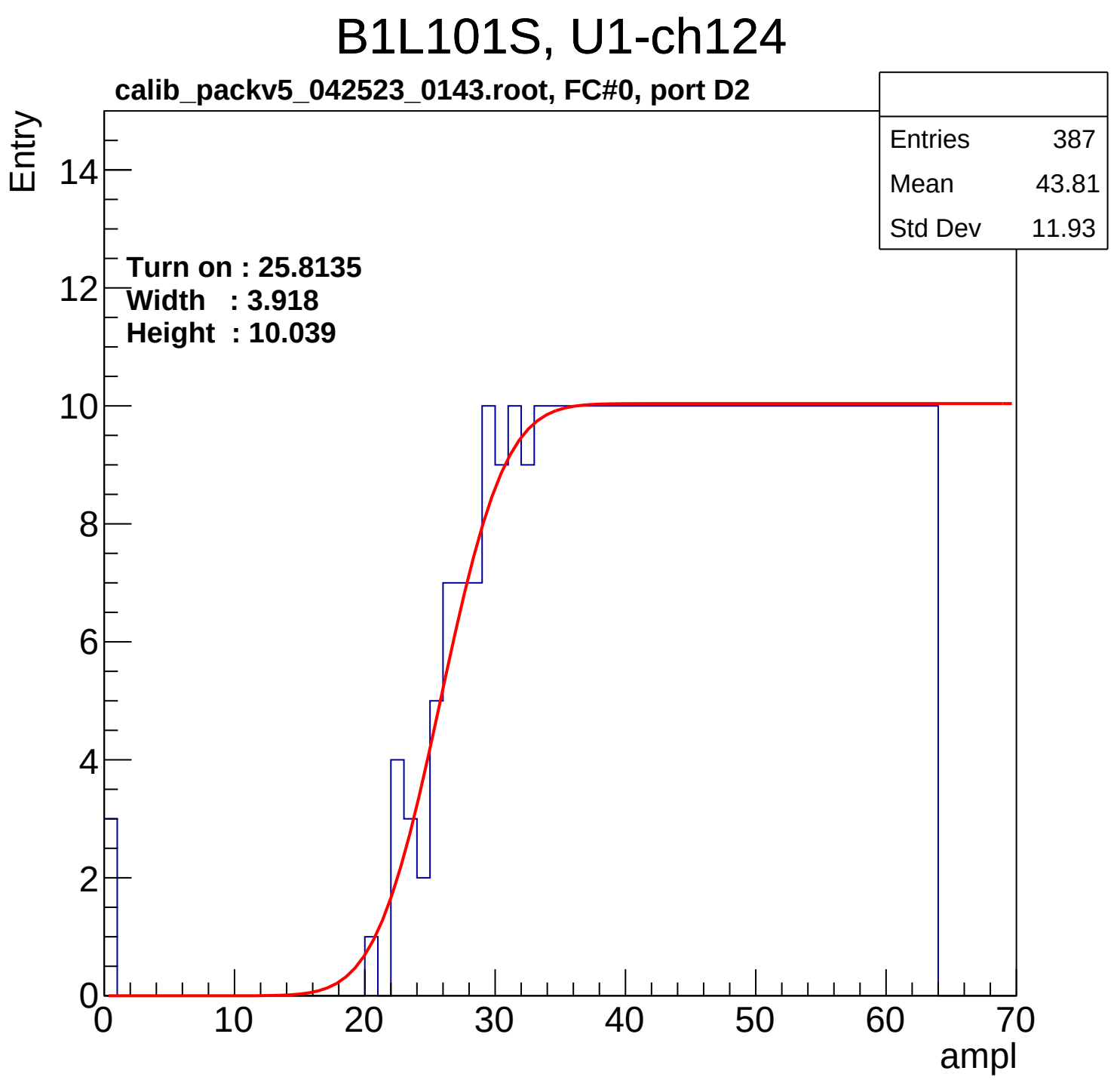
B1L101S, U1-ch124
calib_packv5_042523_0143.root, FC#0, port D2
Entries 387
Mean 43.81
Std Dev 11.93
Turn on : 25.8135
Width : 3.918
Height : 10.039
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
30
40
50
60
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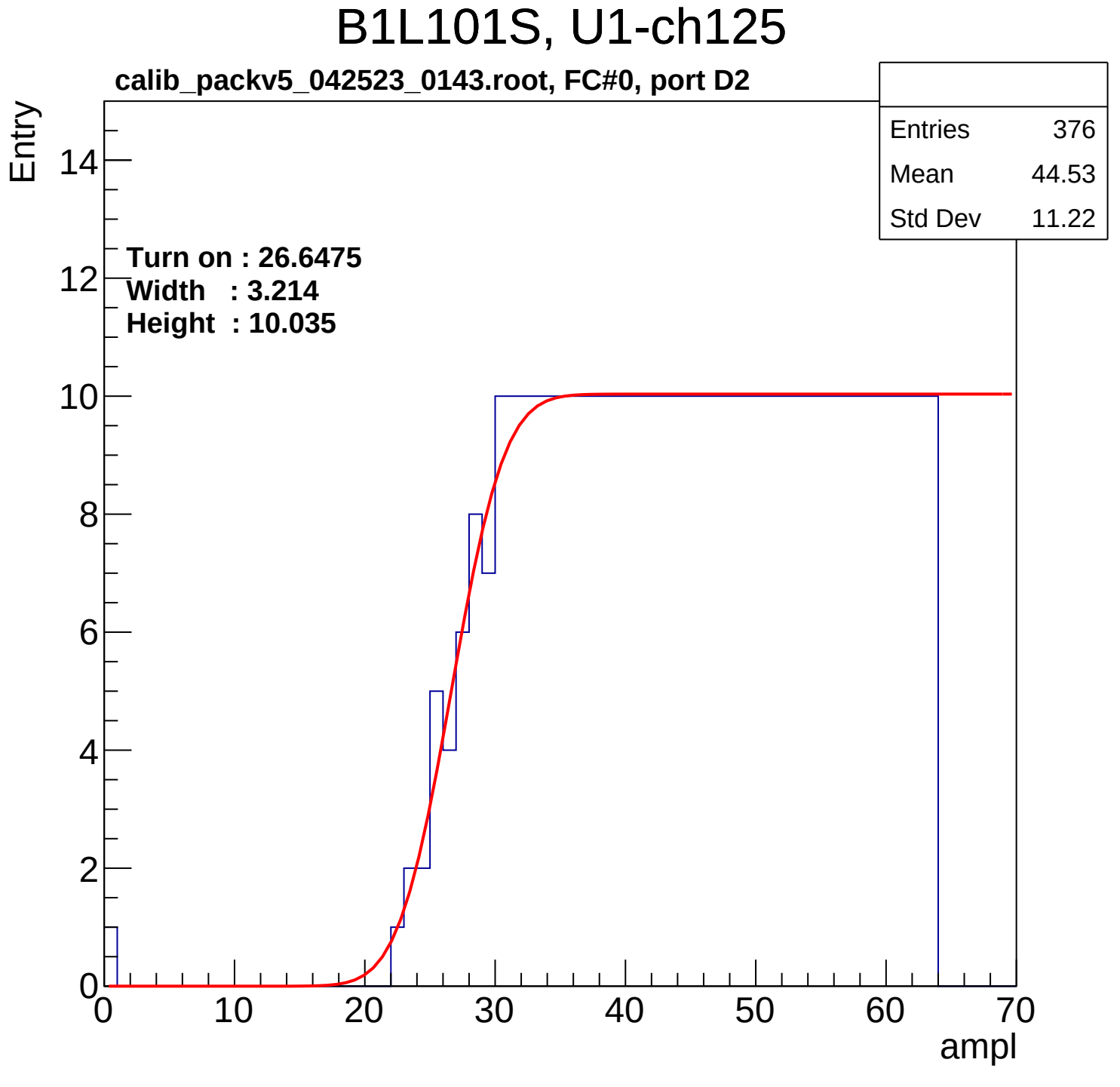
B1L101S, U1-ch125
calib_packv5_042523_0143.root, FC#0, port D2
Entries 376
Mean 44.53
Std Dev 11.22
Turn on : 26.6475
Width : 3.214
Height : 10.035
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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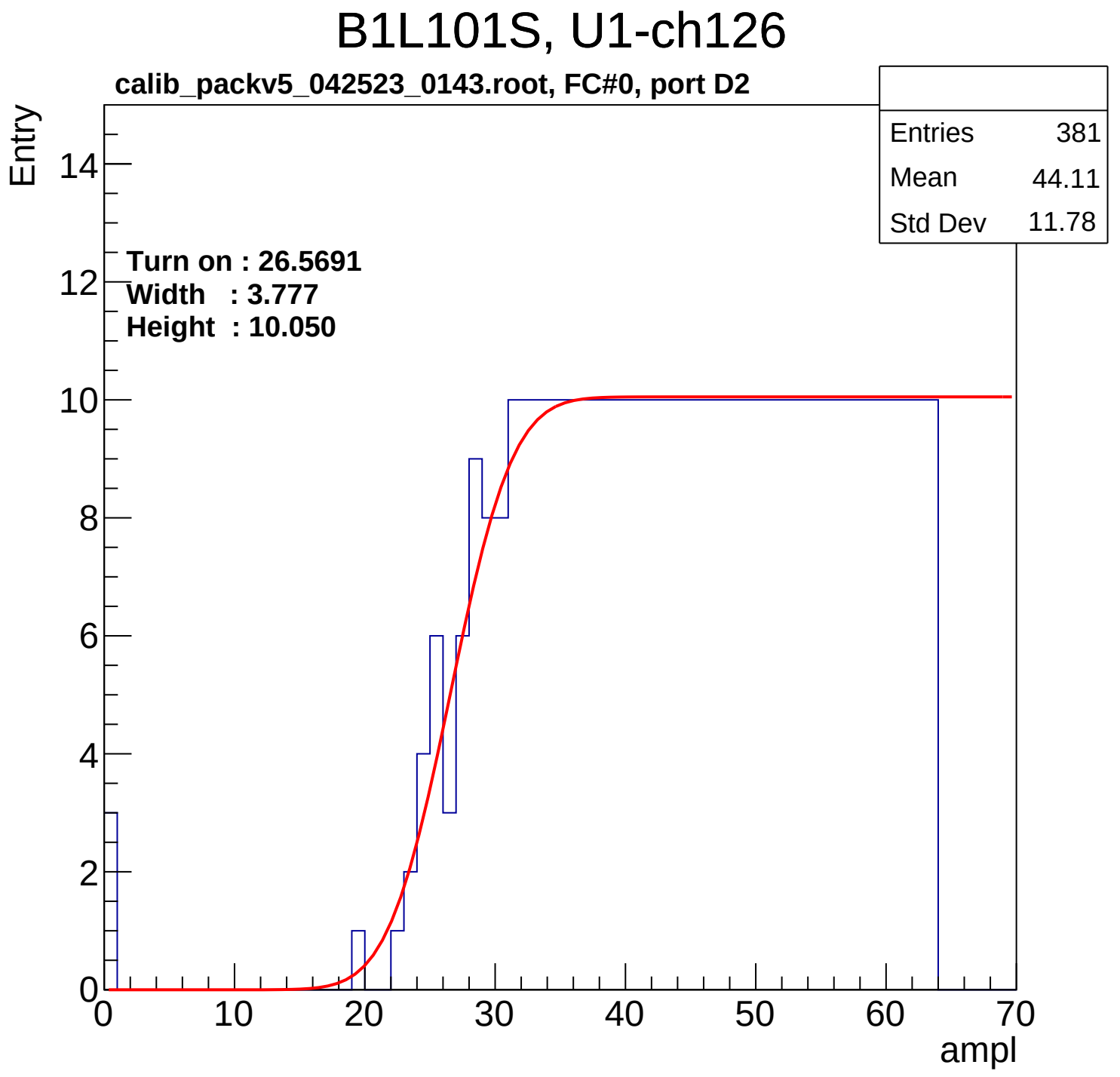
40
50
60
70


B1L101S, U1-ch126
calib_packv5_042523_0143.root, FC#0, port D2
Entries 381
Mean 44.11
Std Dev 11.78
Turn on : 26.5691
Width : 3.777
Height : 10.050
Entry
ampl
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4
6
8
10
12
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0
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20
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60
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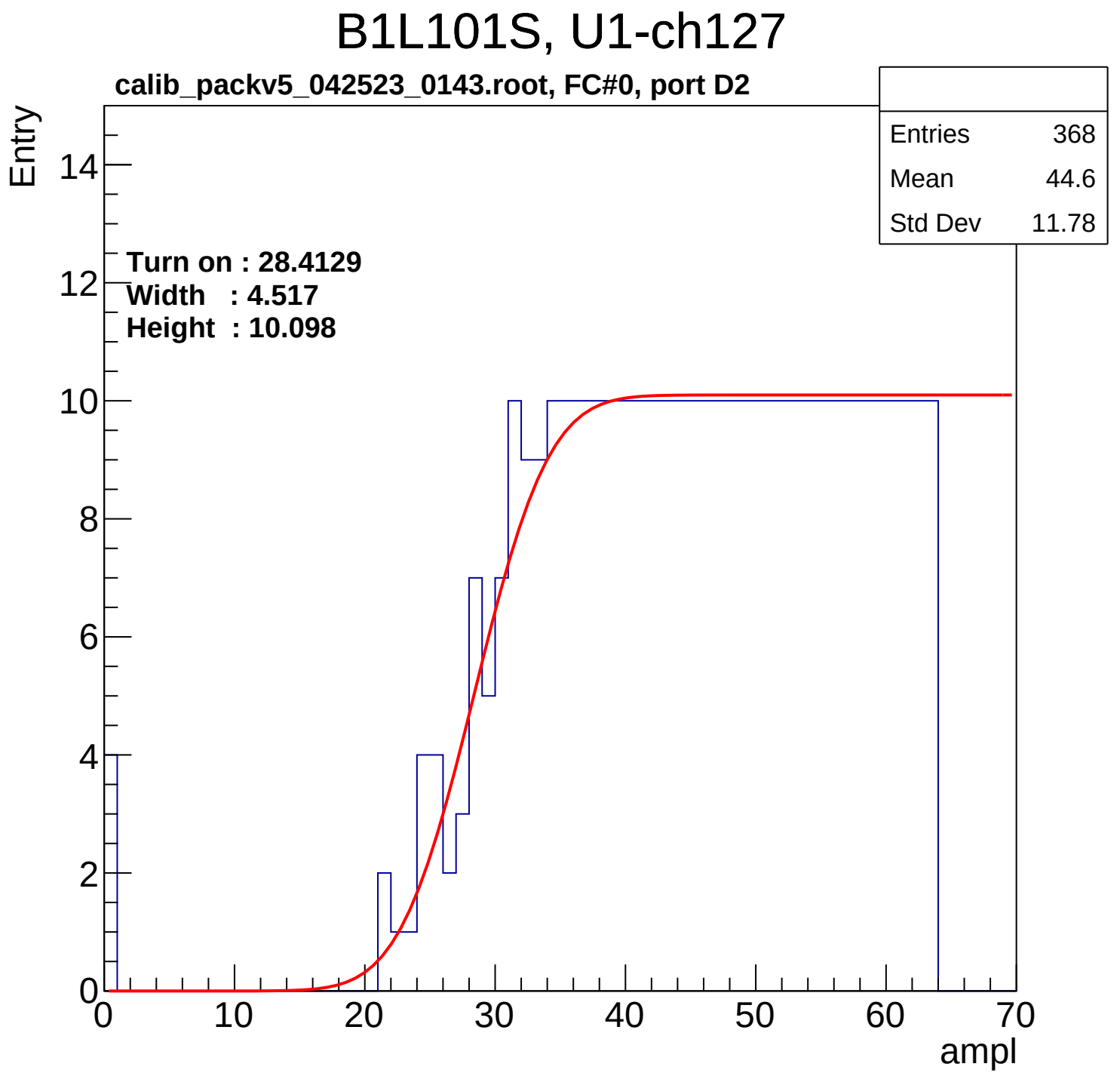
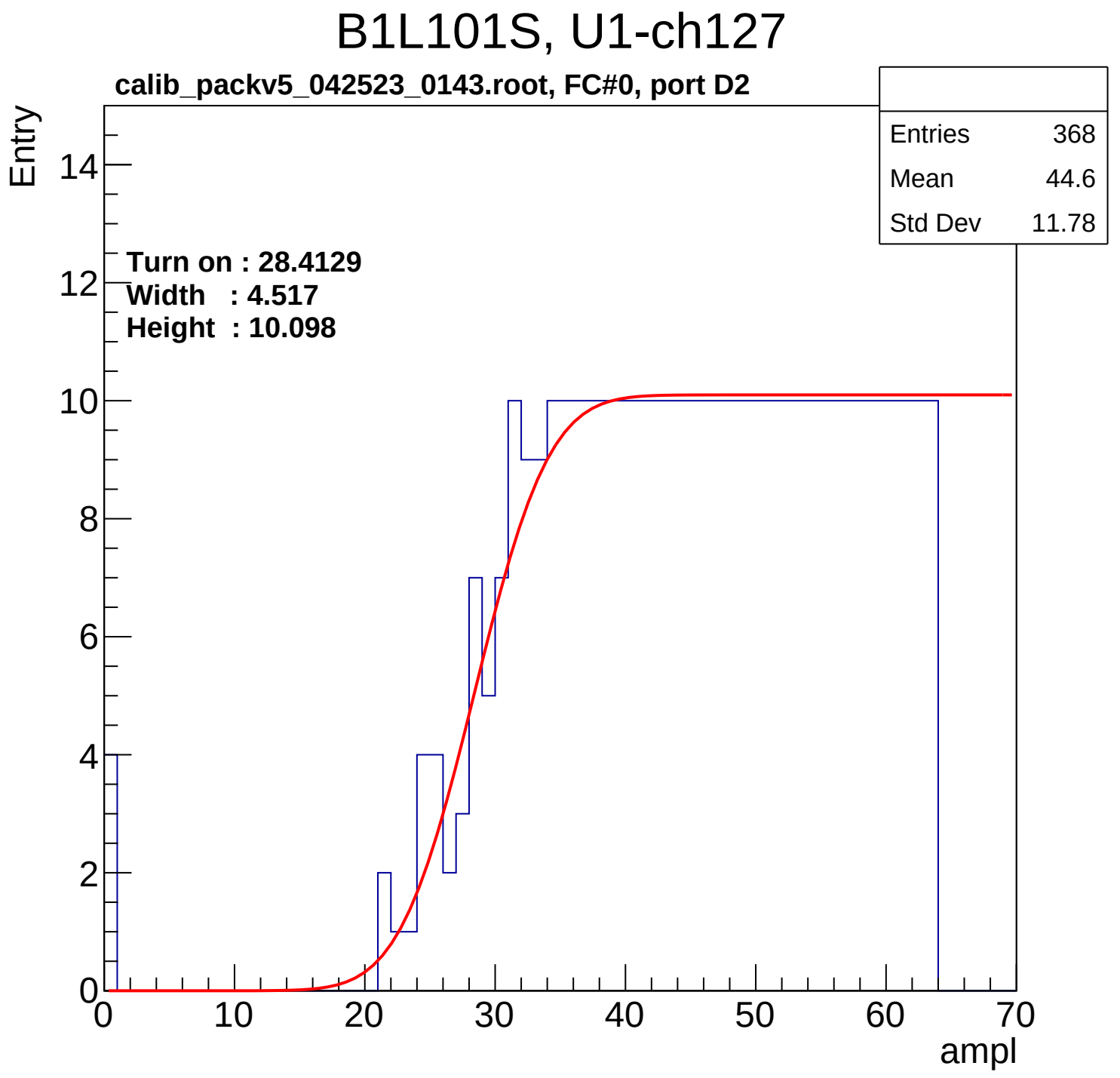

B1L101S, U1-ch127
calib_packv5_042523_0143.root, FC#0, port D2
Entries 368
Mean 44.6
Std Dev 11.78
Turn on : 28.4129
Width : 4.517
Height : 10.098
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L101S, U1-ch127
calib_packv5_042523_0143.root, FC#0, port D2
Entries 368
Mean 44.6
Std Dev 11.78
Turn on : 28.4129
Width : 4.517
Height : 10.098
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
30
40
50
60
70