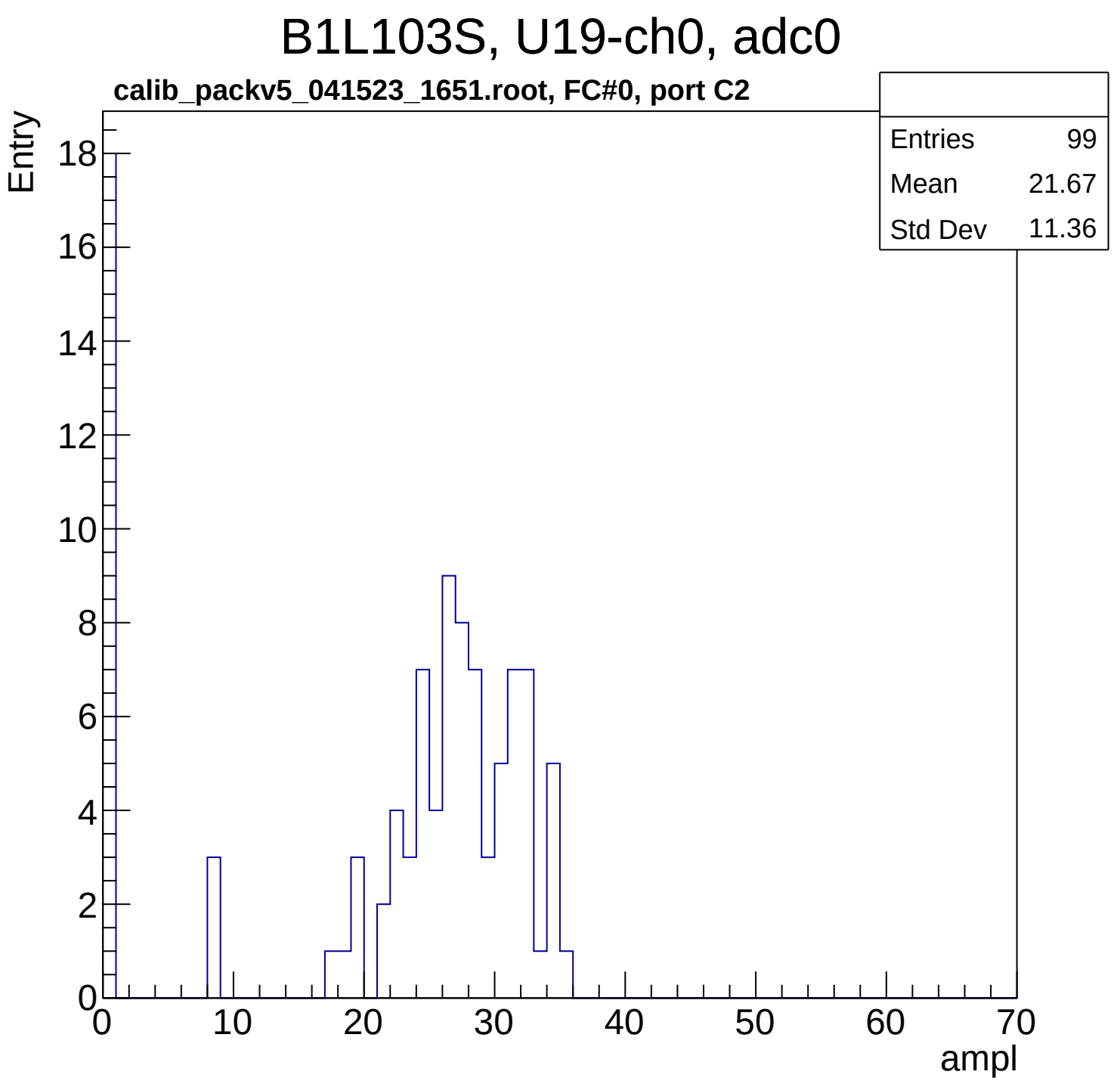
B1L103S, U19-ch0, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 21.67
Std Dev 11.36
Entry
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6
8
10
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14
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18
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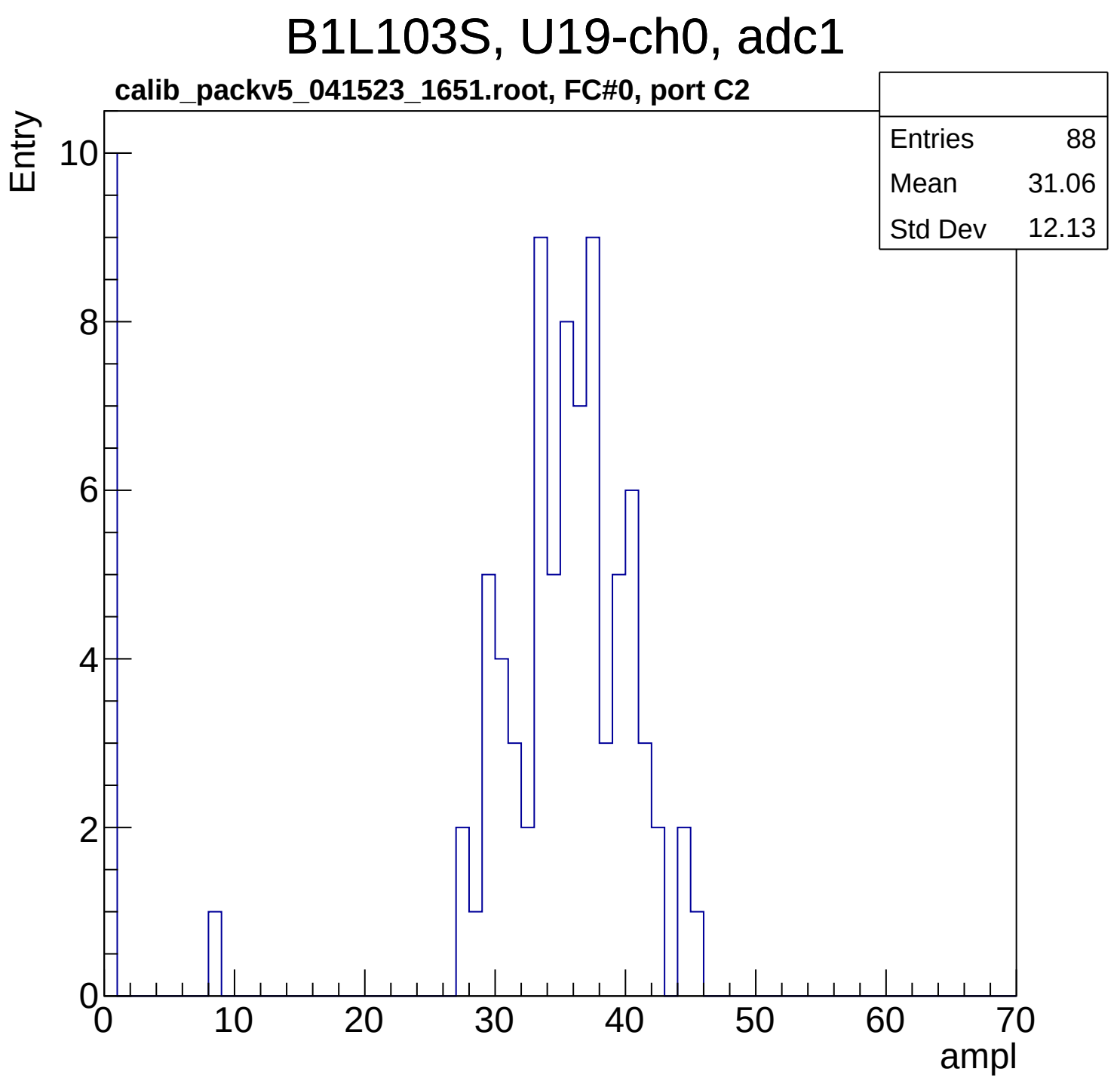
70
ampl


B1L103S, U19-ch0, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 31.06
Std Dev 12.13
Entry
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6
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10
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10
20
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50
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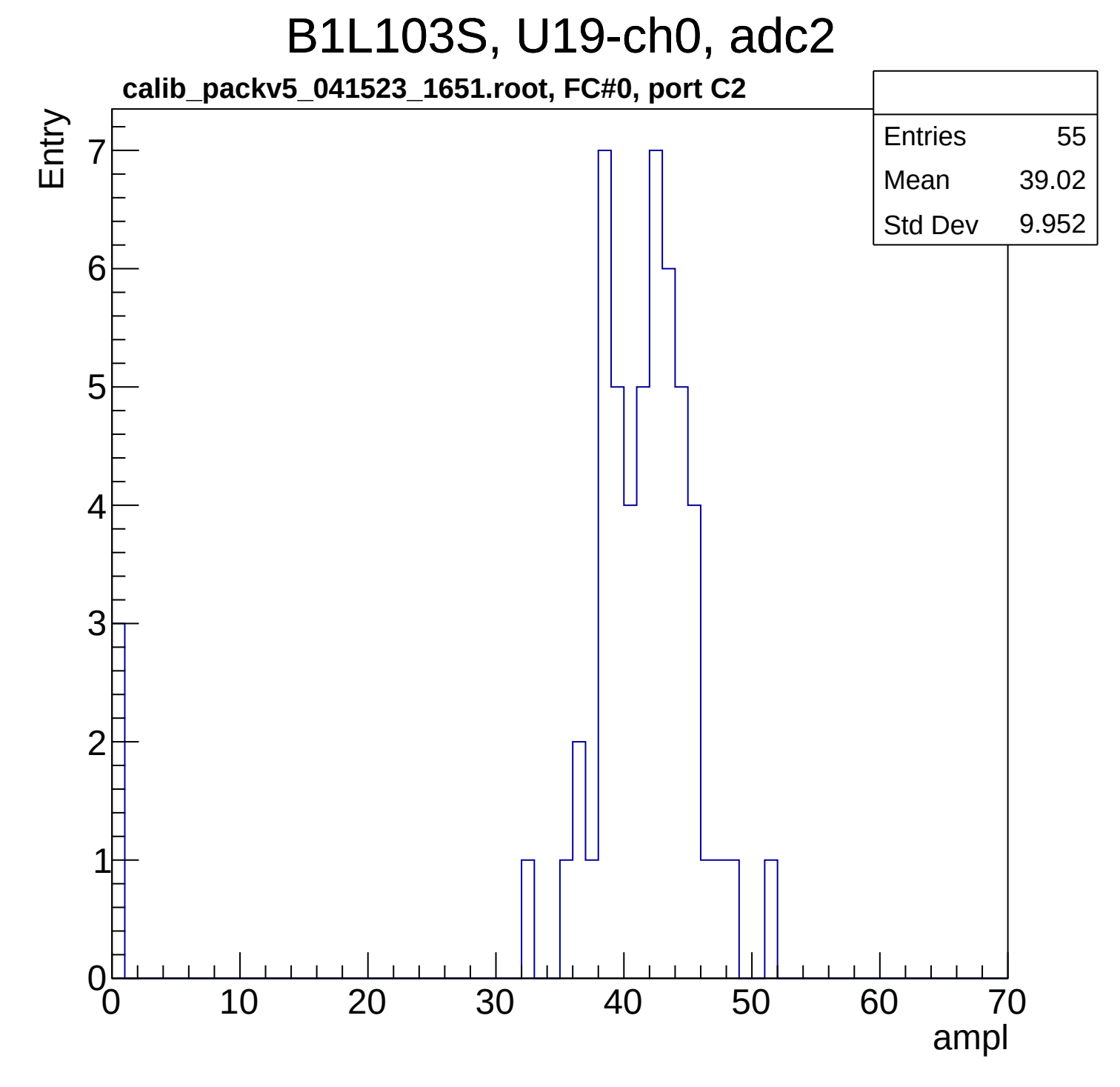
70
ampl


B1L103S, U19-ch0, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 39.02
Std Dev 9.952
Entry
ampl
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0
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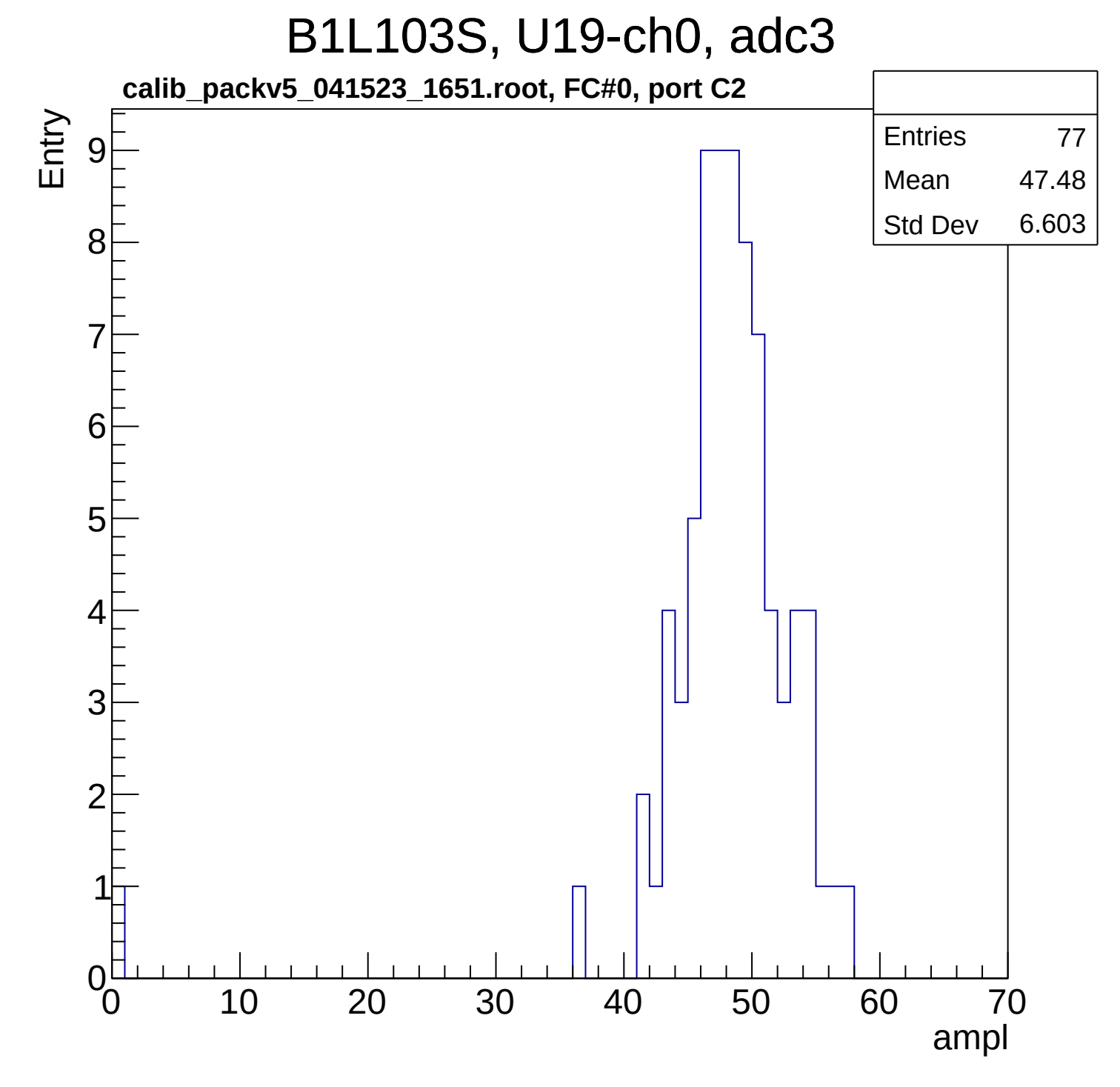
B1L103S, U19-ch0, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 47.48
Std Dev 6.603
Entry
ampl
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4
5
6
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0
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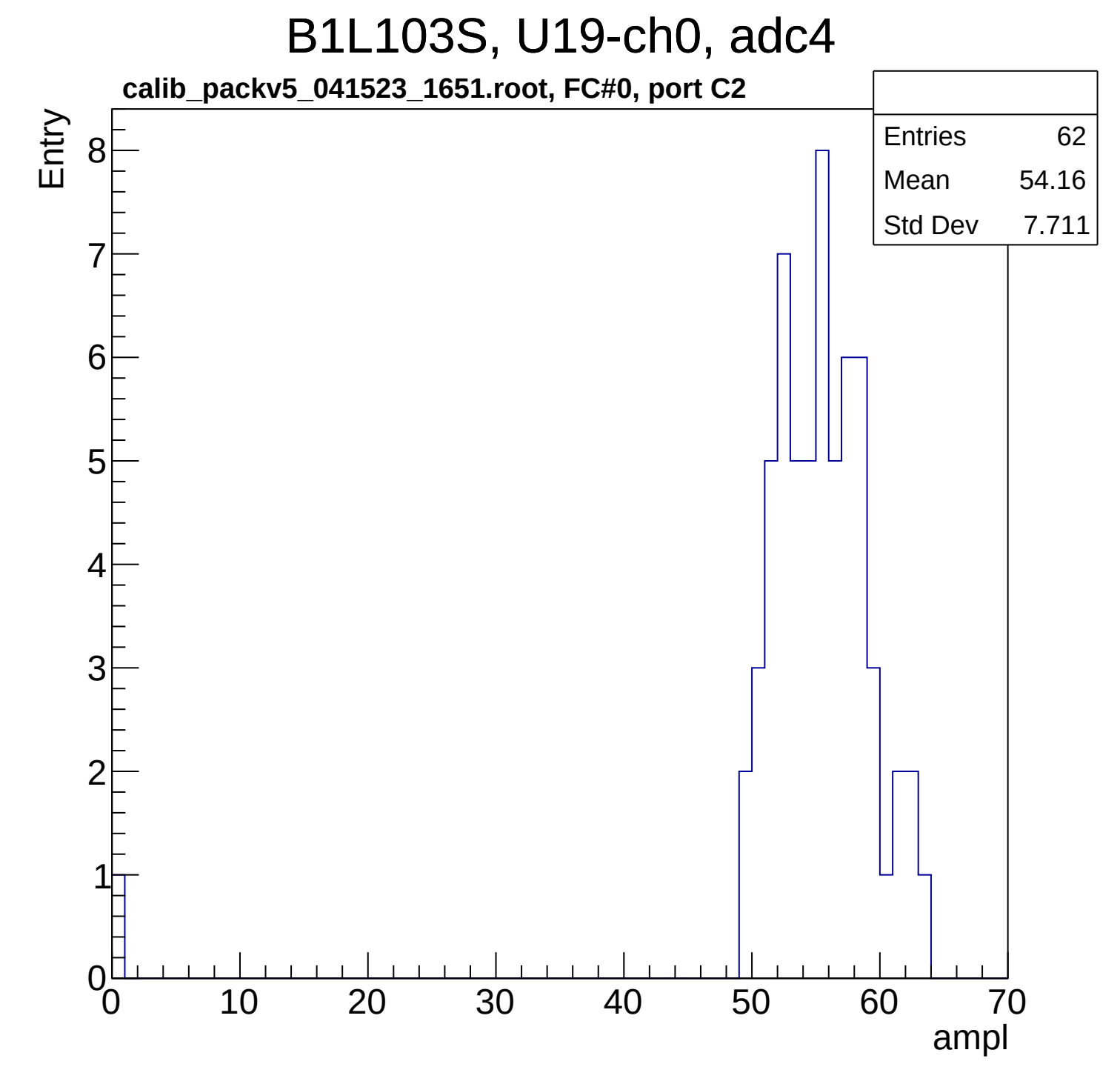
B1L103S, U19-ch0, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 54.16
Std Dev 7.711
Entry
ampl
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2
3
4
5
6
7
8
0
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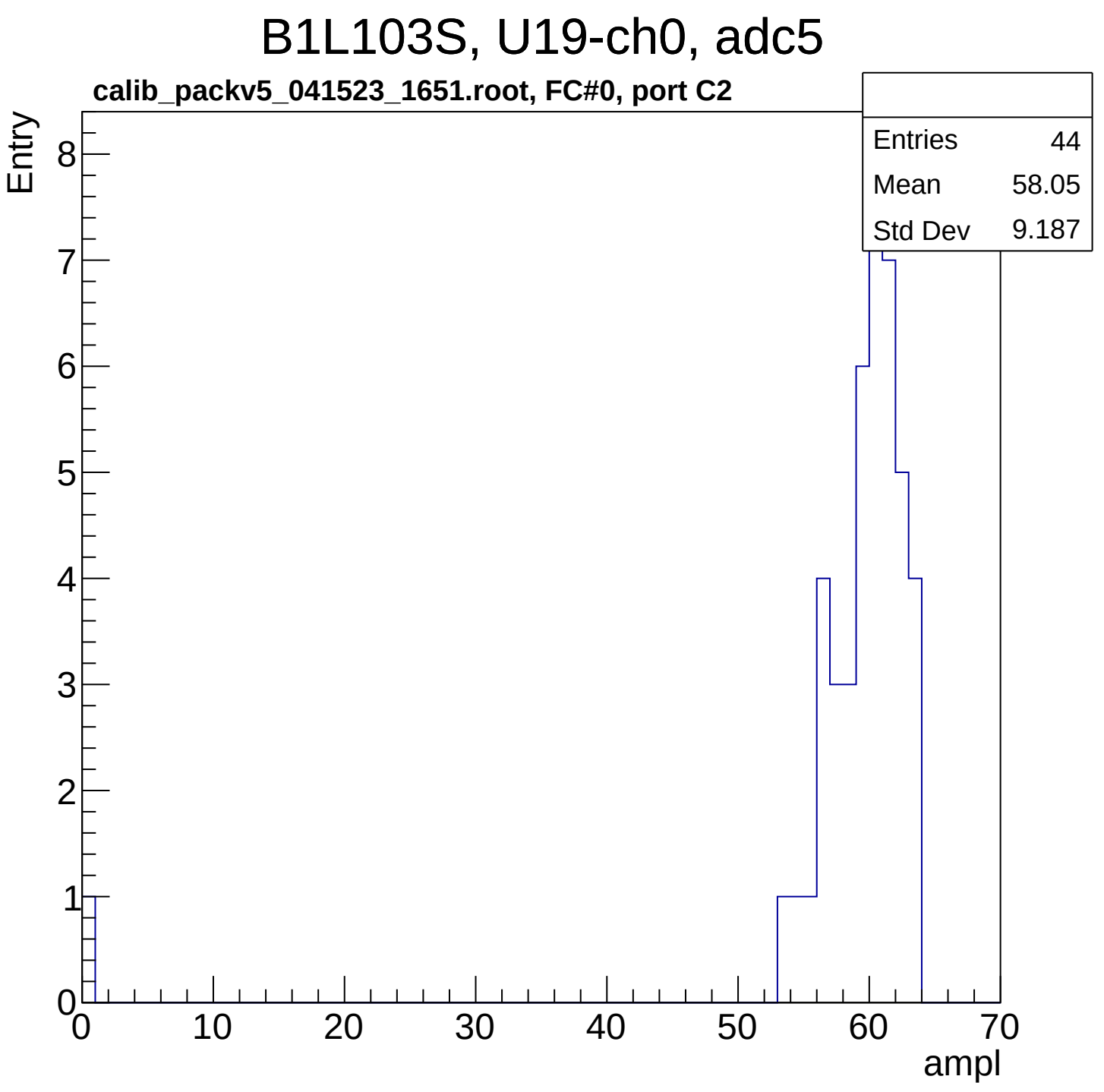
B1L103S, U19-ch0, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 58.05
Std Dev 9.187
Entry
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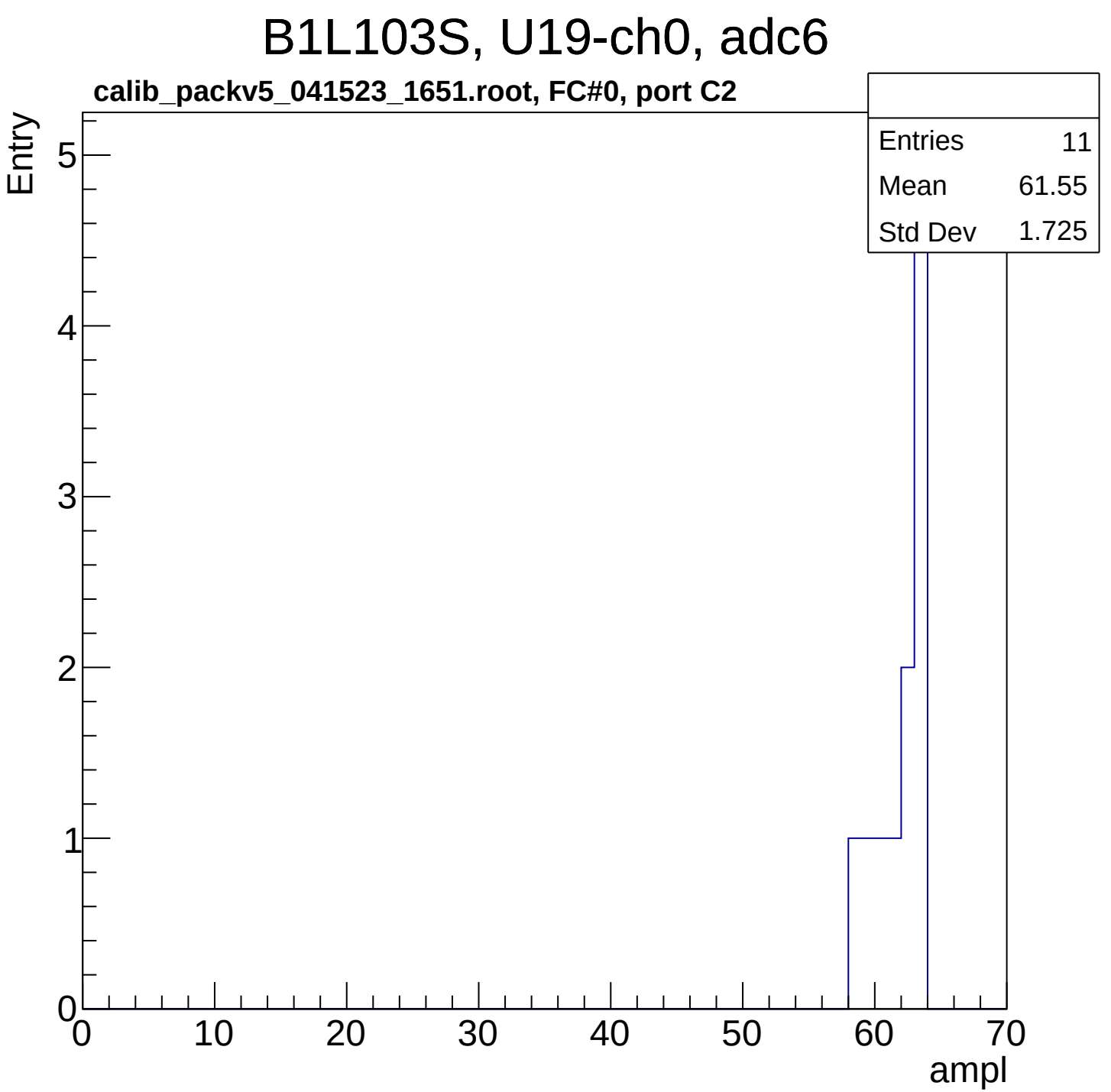
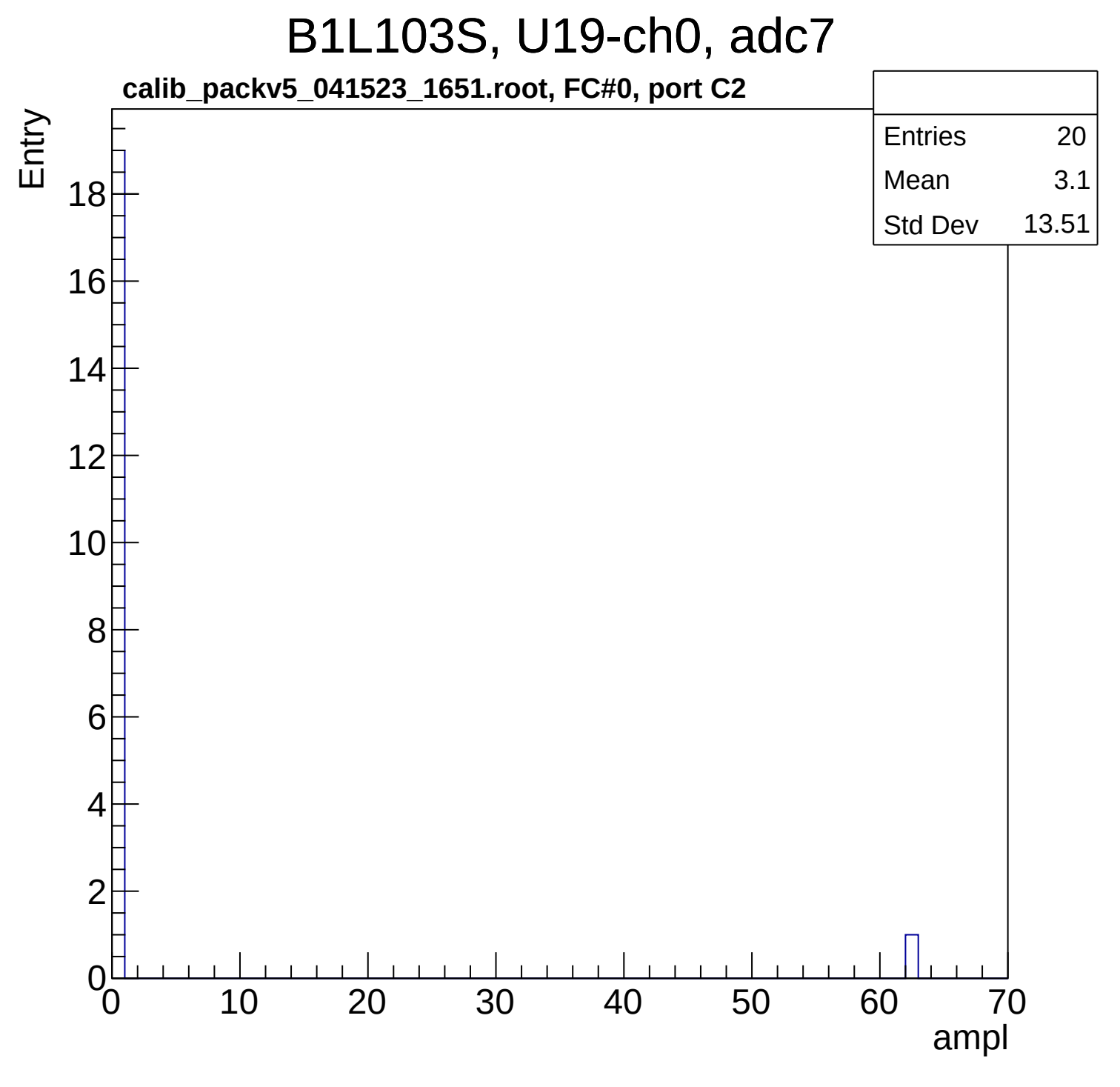
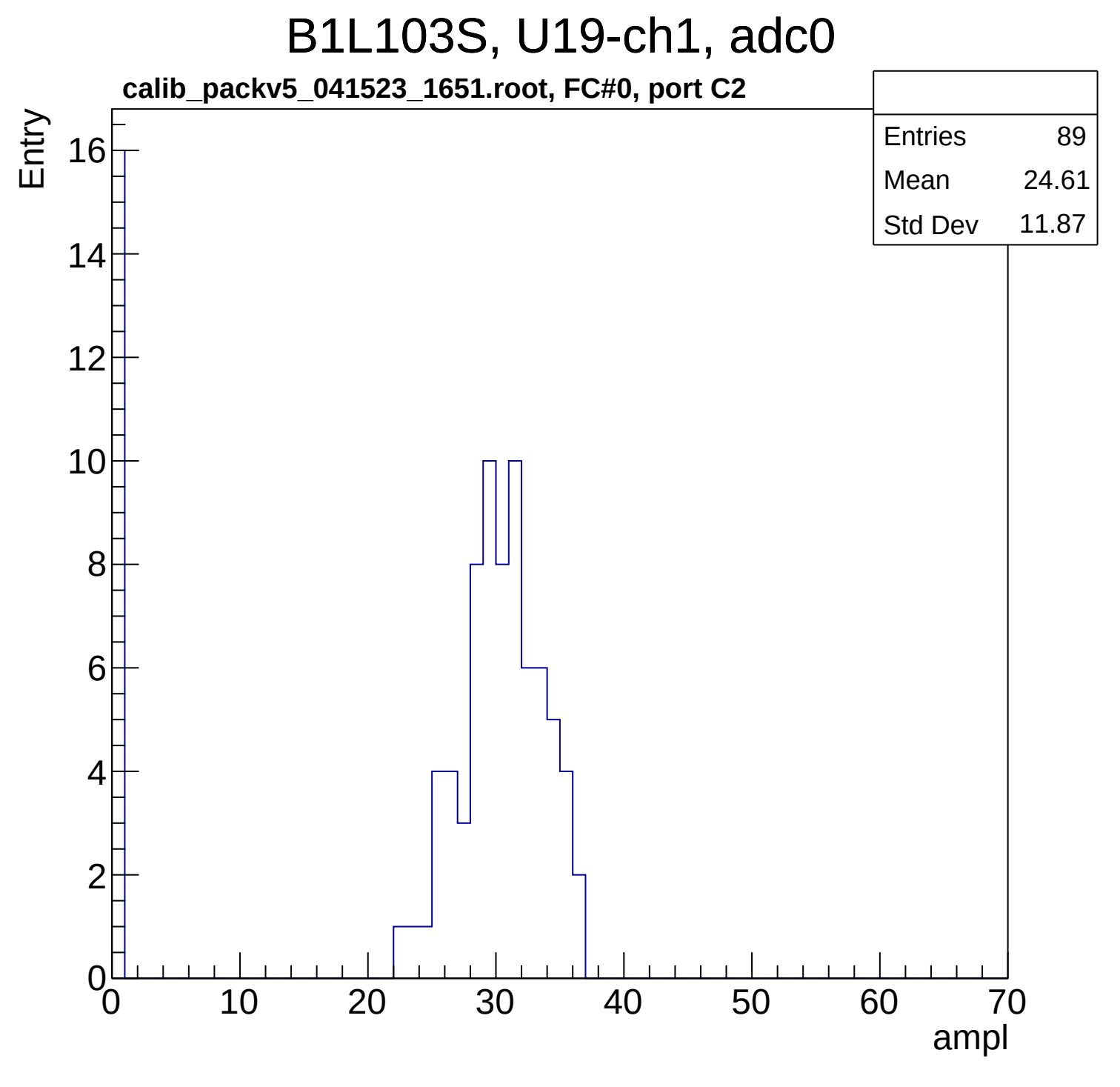
ampl


B1L103S, U19-ch0, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 61.55
Std Dev 1.725
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch0, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch1, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 24.61
Std Dev 11.87
Entry
ampl
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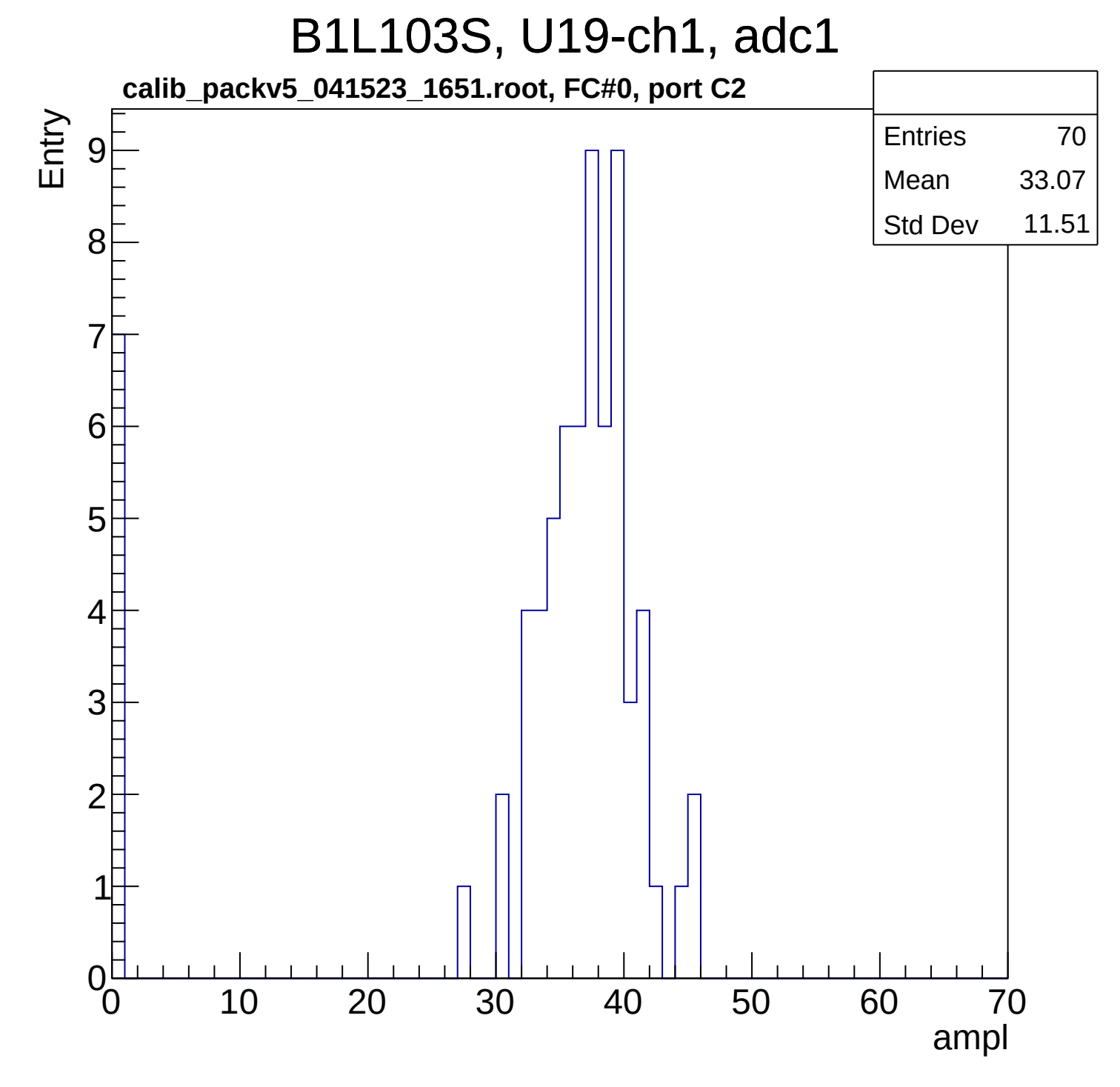
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L103S, U19-ch1, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 33.07
Std Dev 11.51
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
50
60
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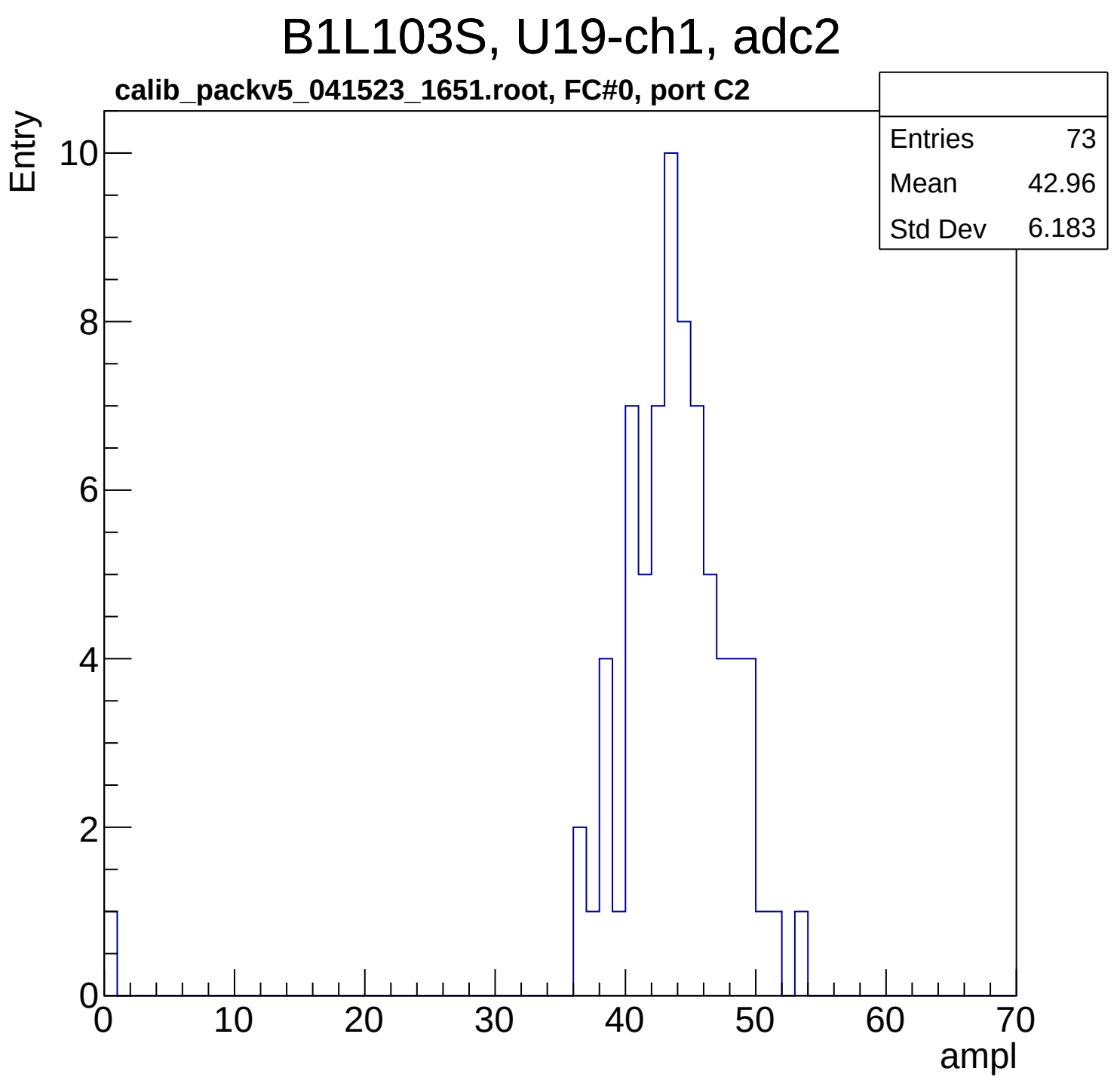
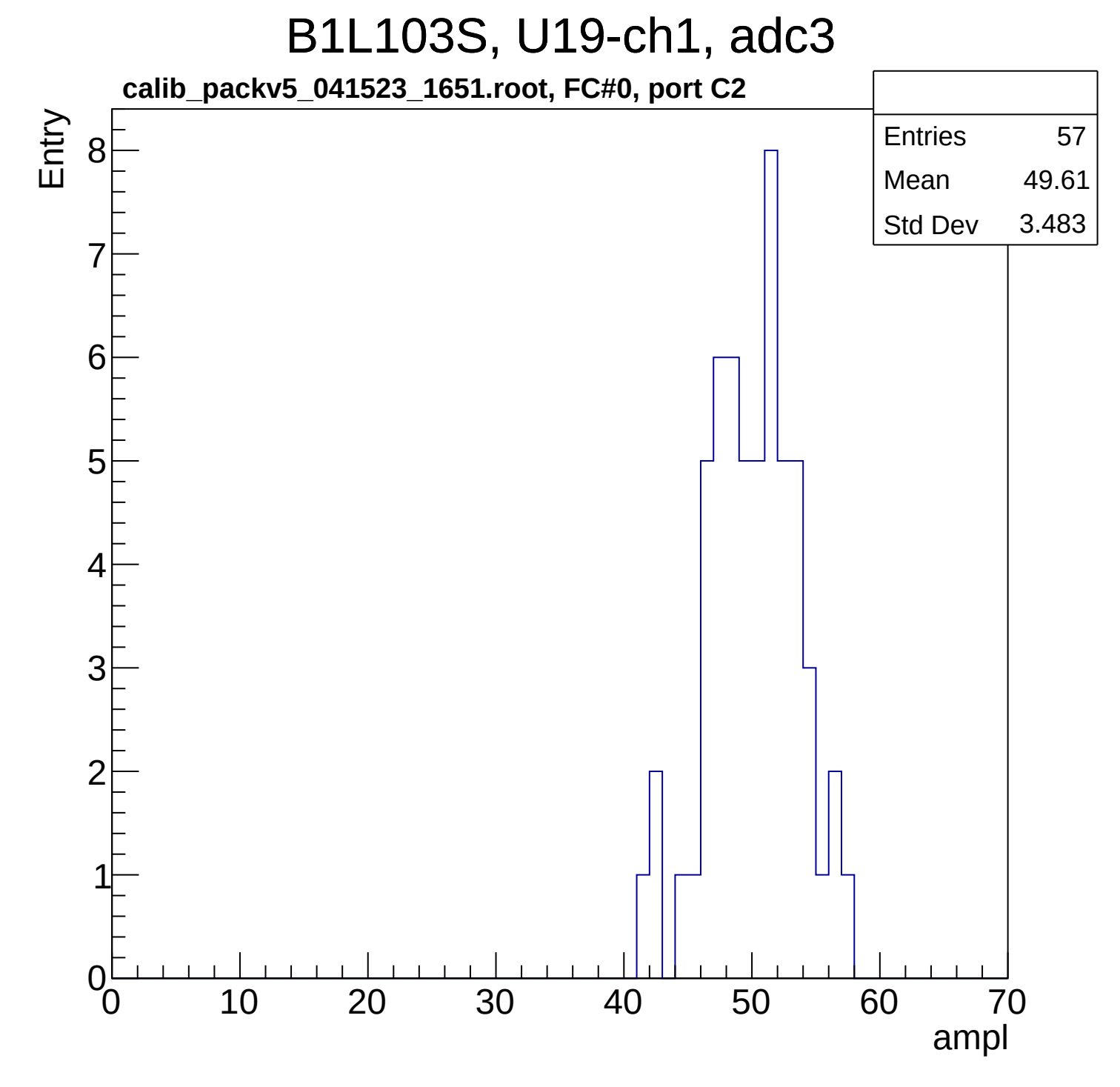

B1L103S, U19-ch1, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 42.96
Std Dev 6.183
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch1, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 49.61
Std Dev 3.483
Entry
ampl
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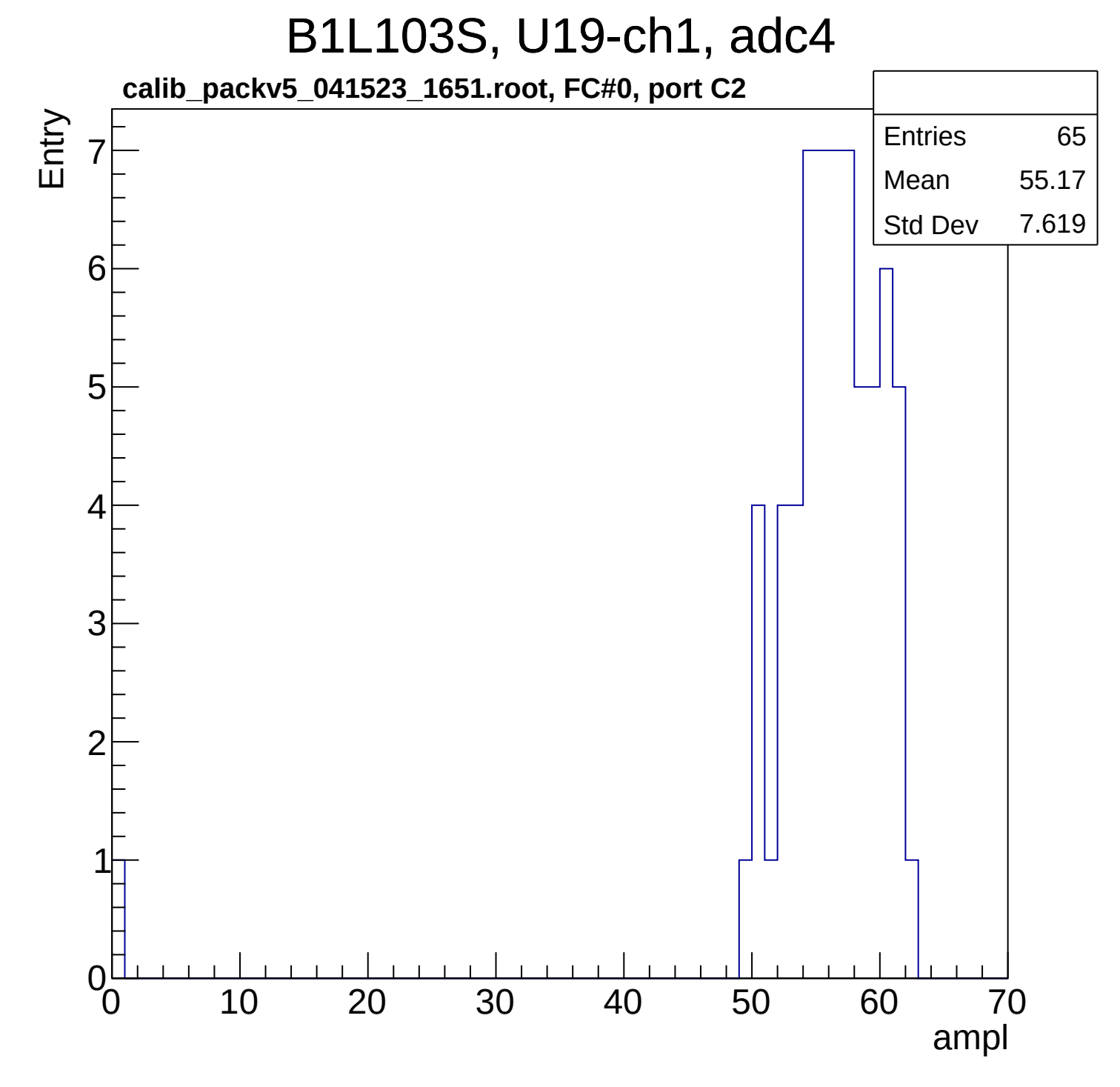
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch1, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 55.17
Std Dev 7.619
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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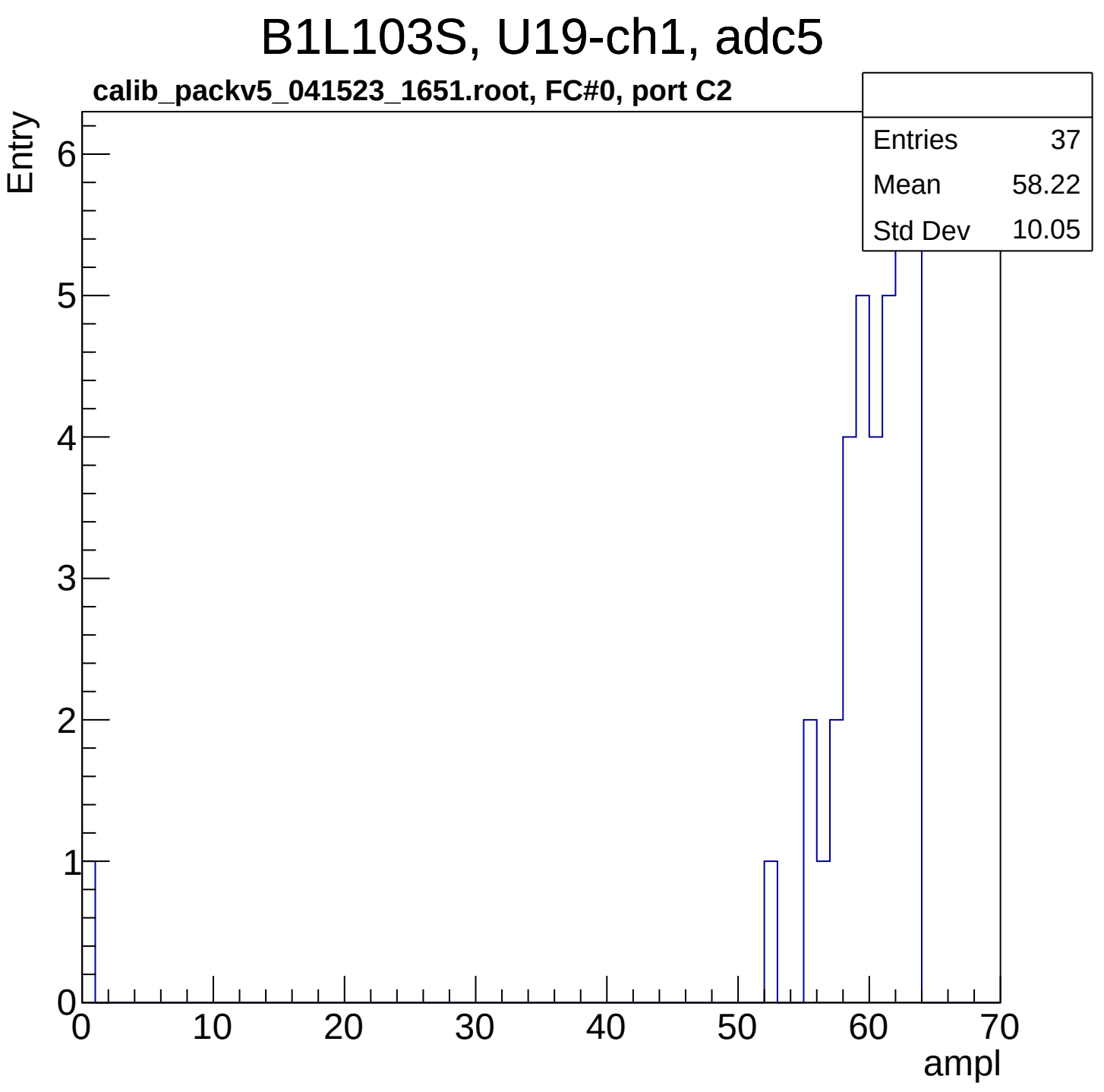
B1L103S, U19-ch1, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 58.22
Std Dev 10.05
Entry
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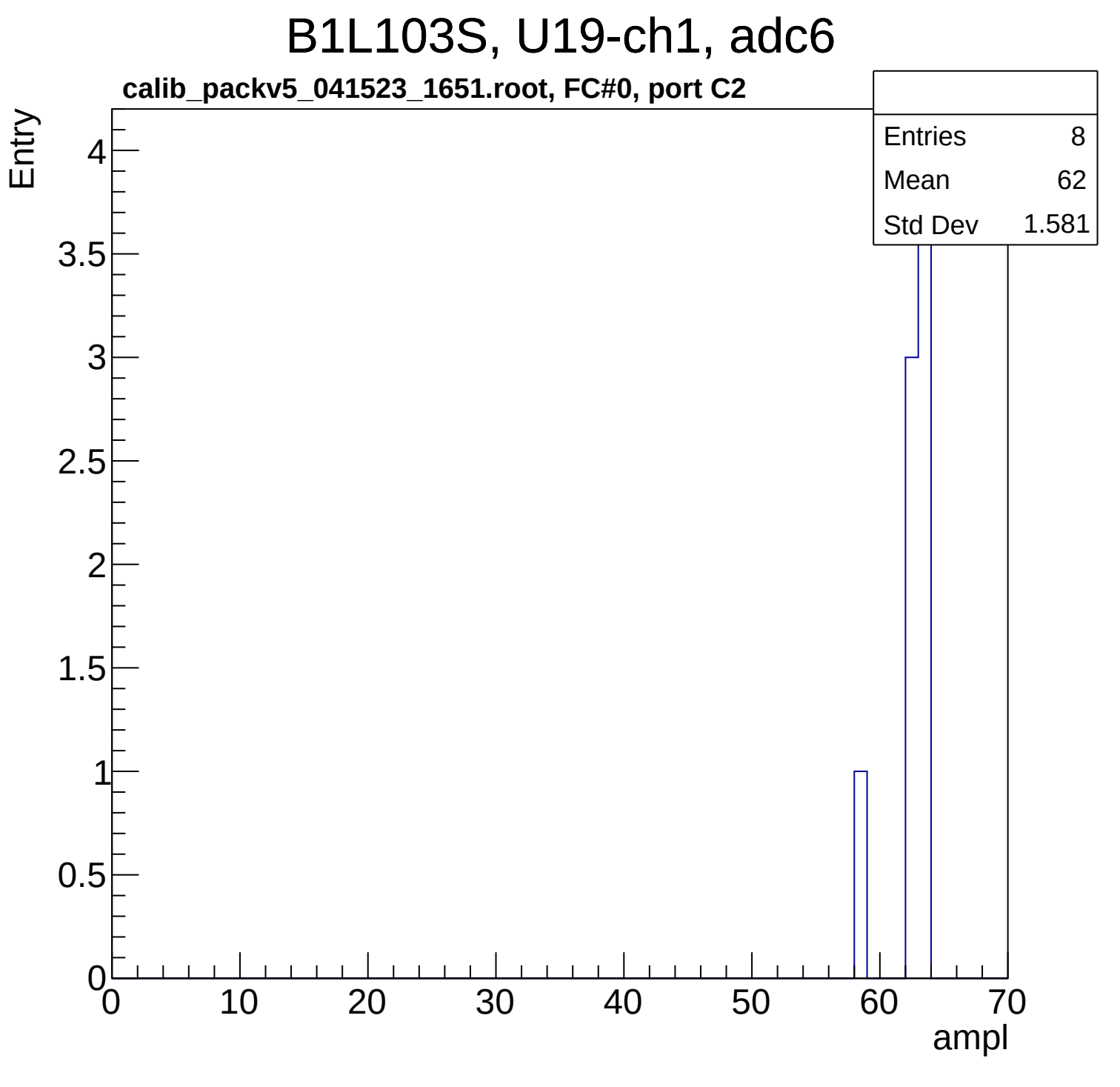
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch1, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 62
Std Dev 1.581
Entry
ampl
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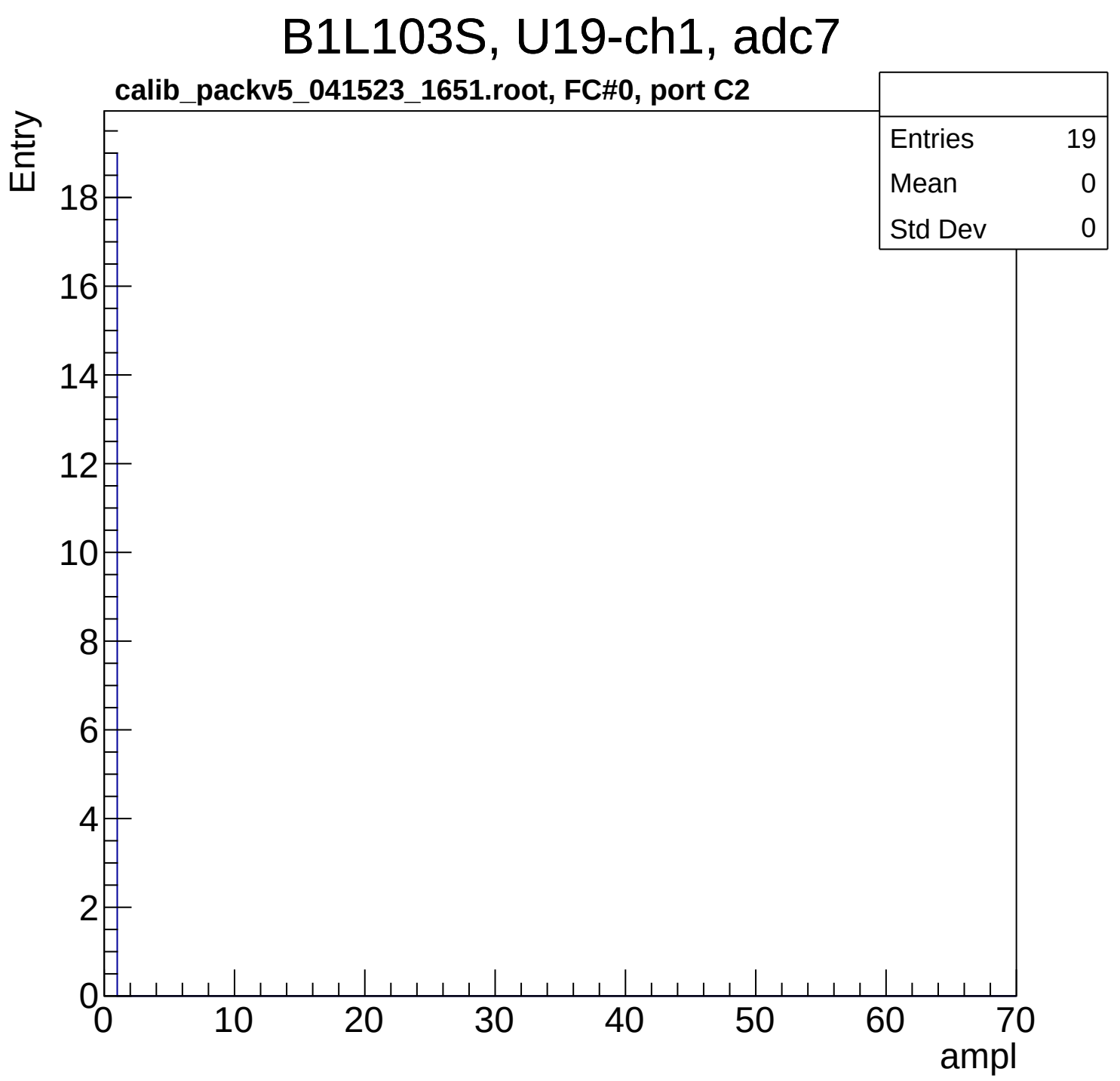
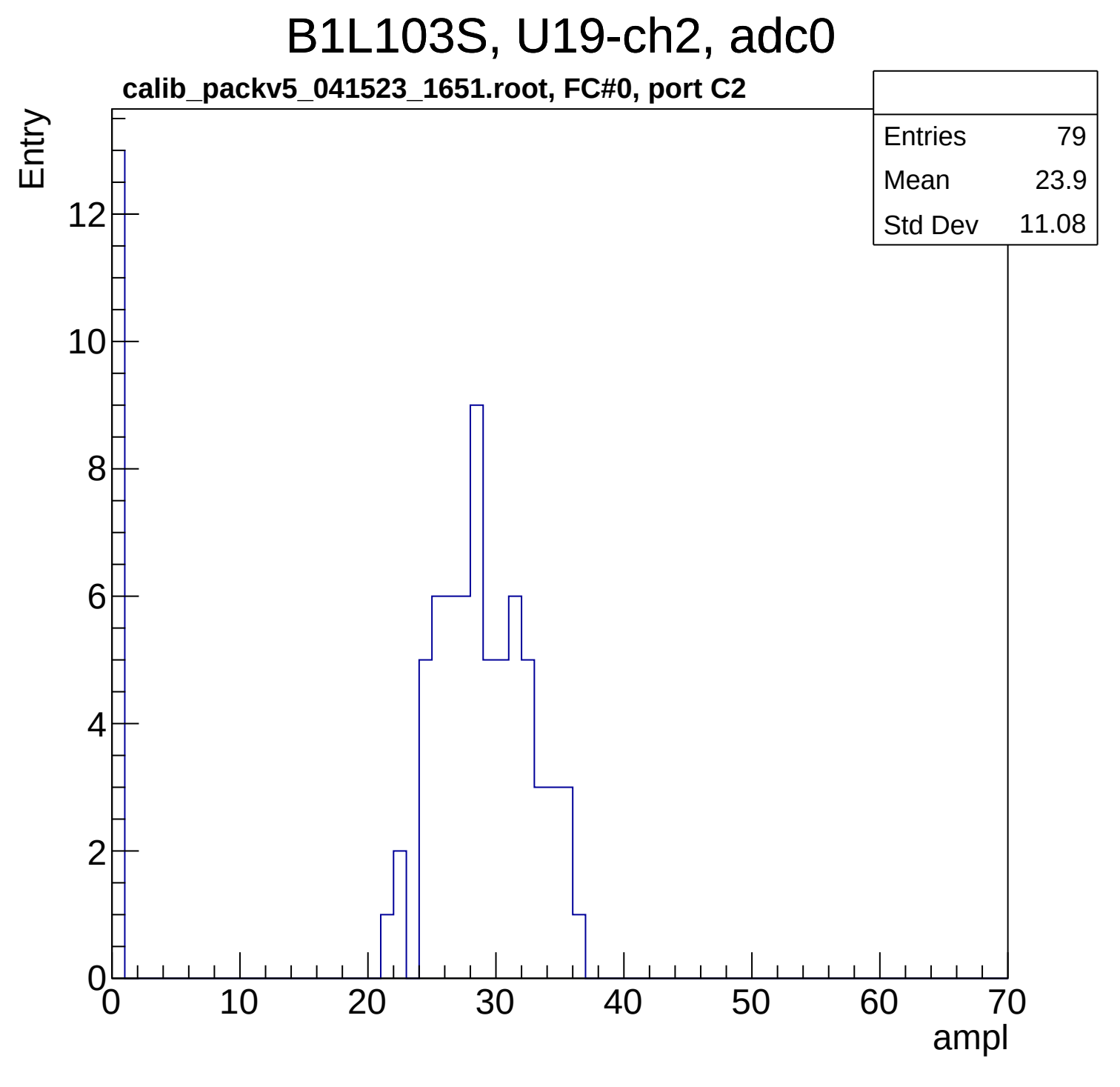
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U19-ch1, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch2, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 23.9
Std Dev 11.08
Entry
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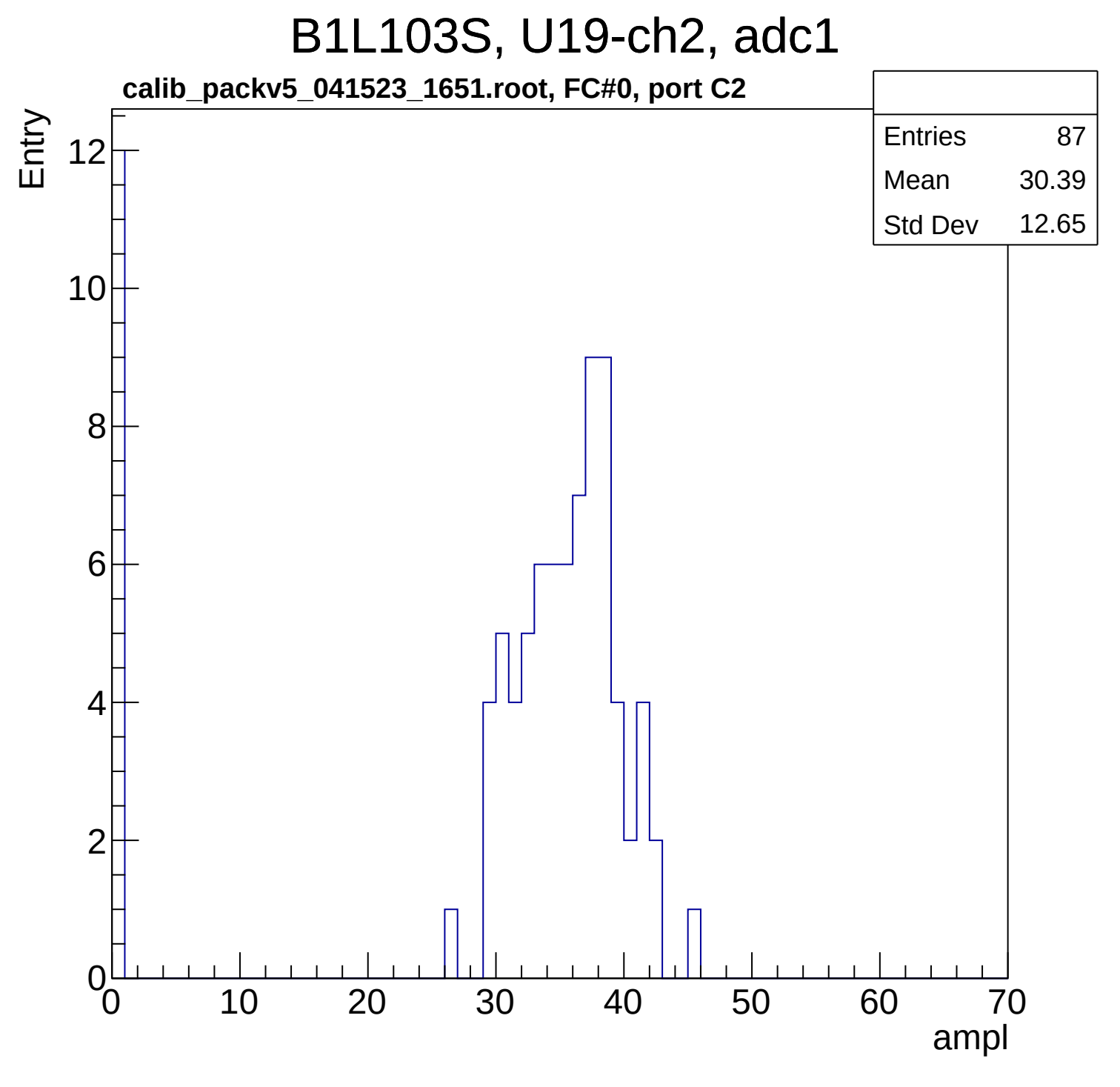
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch2, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 30.39
Std Dev 12.65
Entry
ampl
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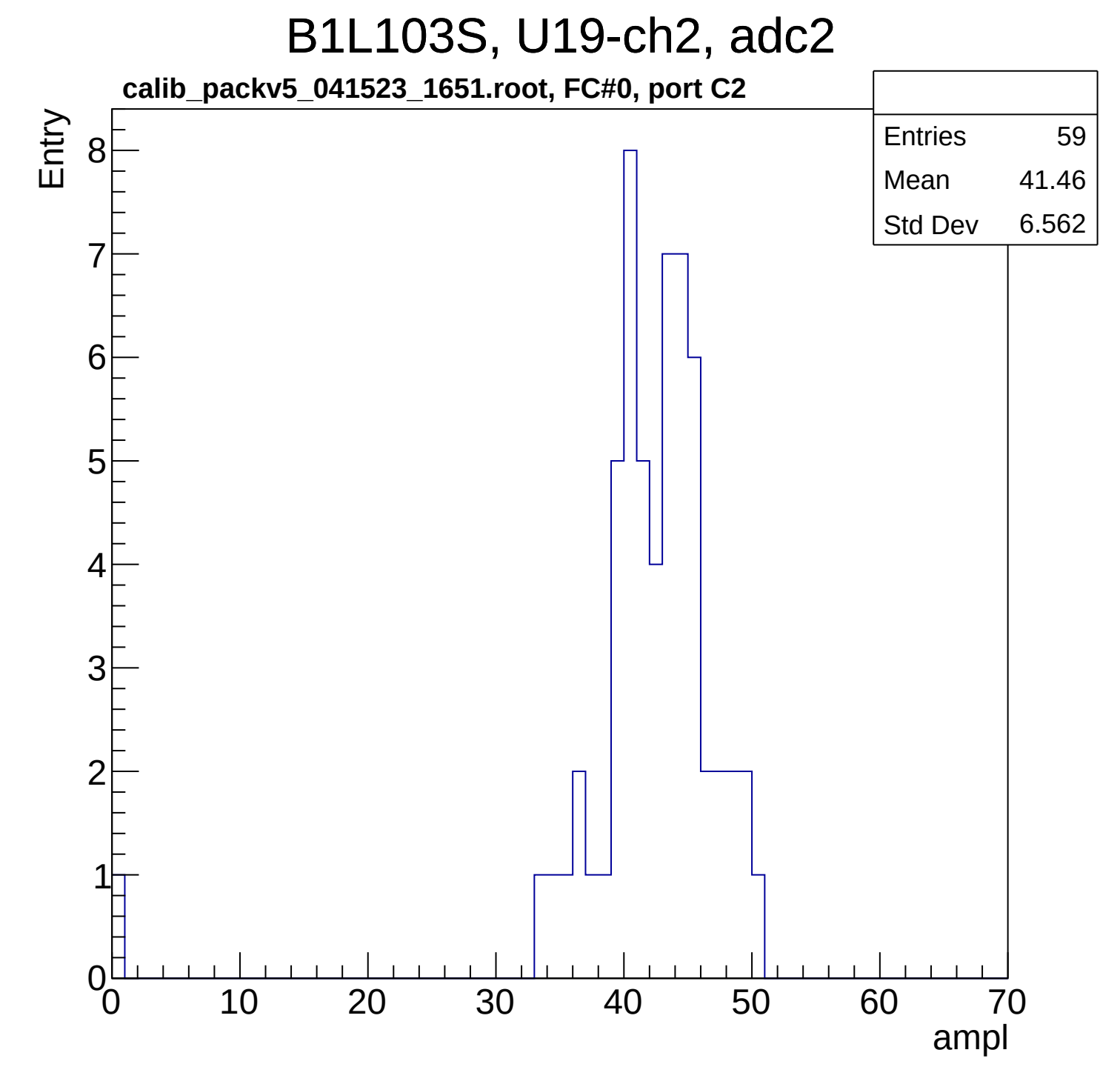
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U19-ch2, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 41.46
Std Dev 6.562
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
50
60
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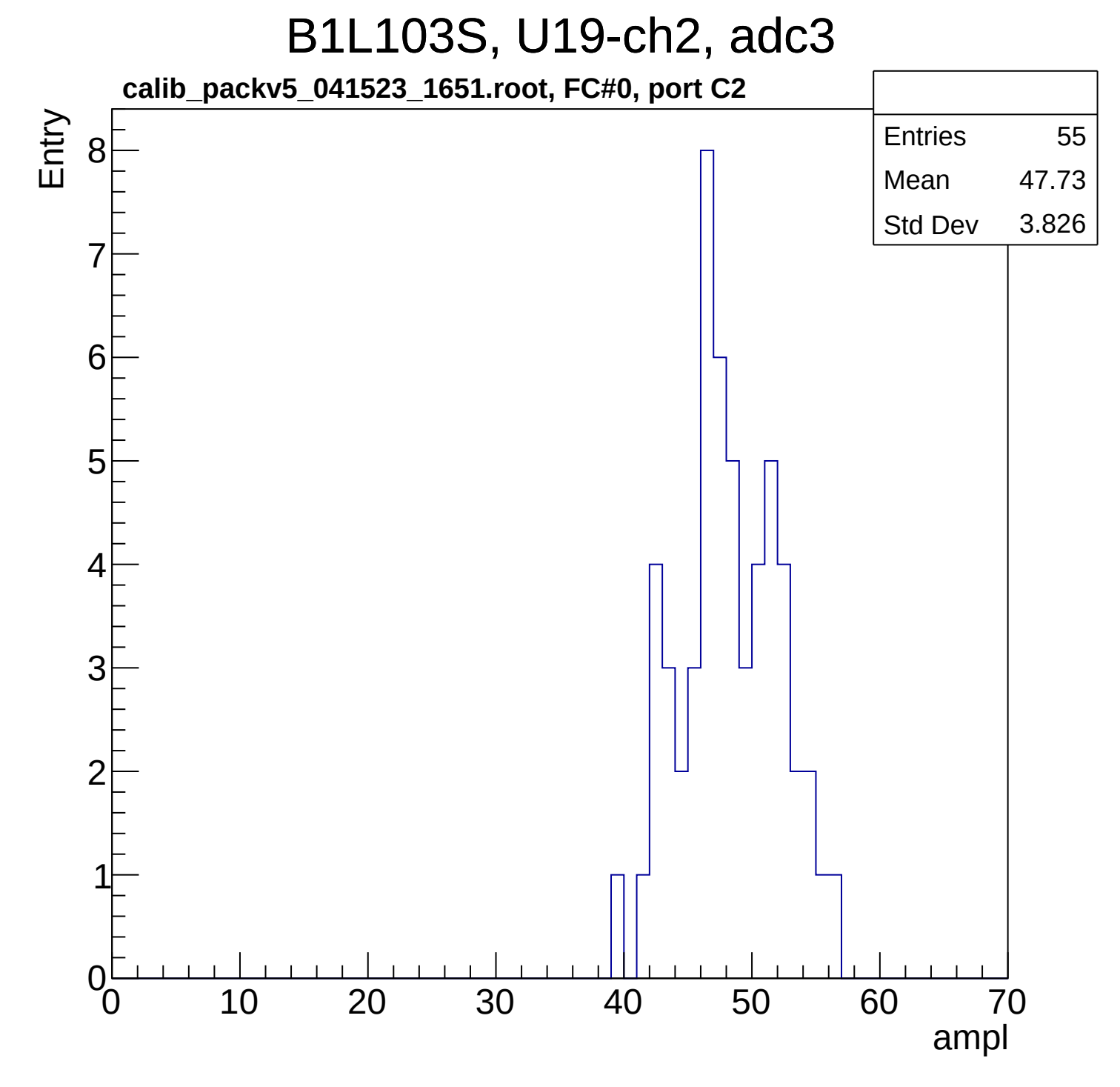
B1L103S, U19-ch2, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 47.73
Std Dev 3.826
Entry
ampl
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2
3
4
5
6
7
8
0
10
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40
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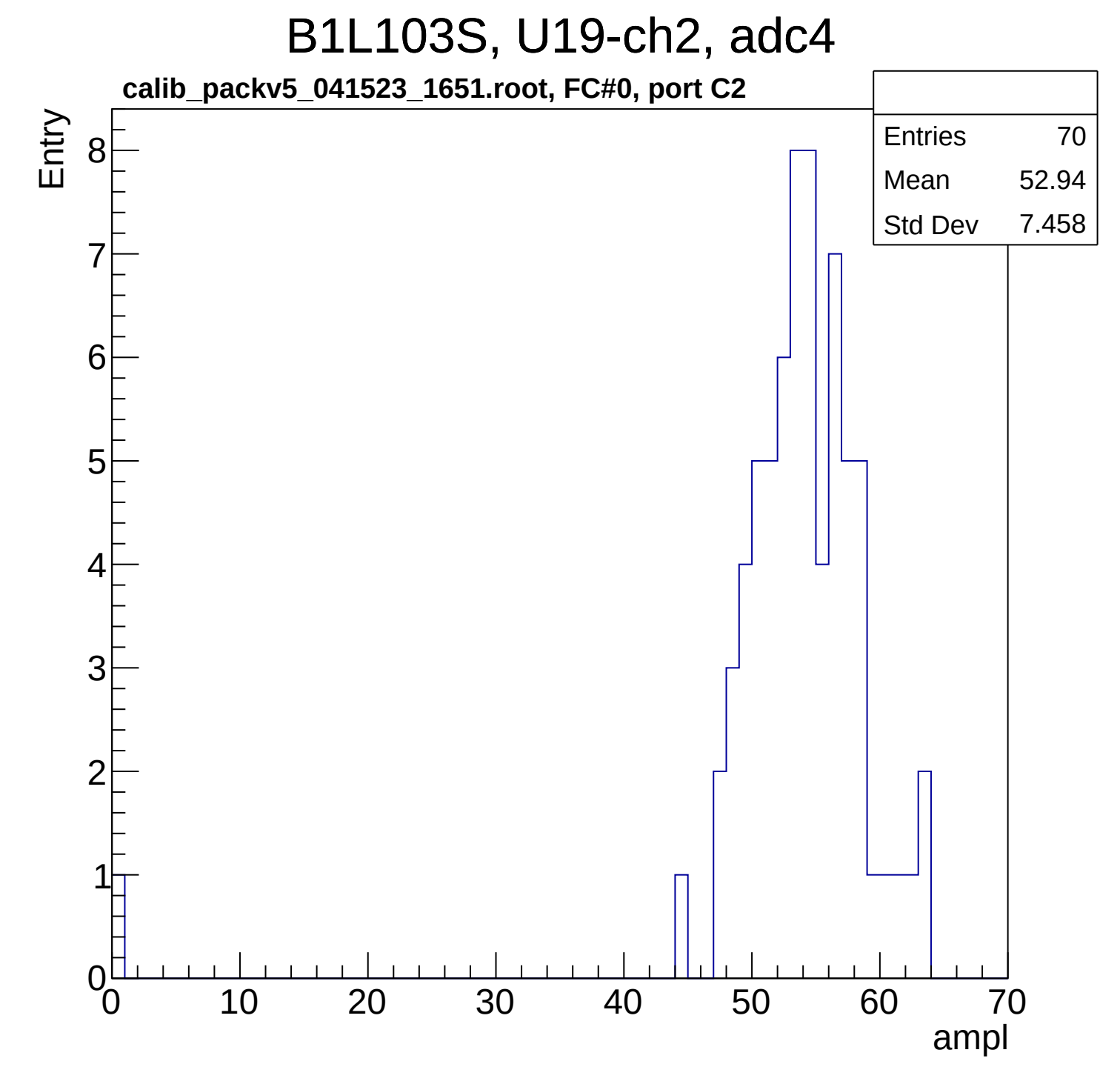
60
70


B1L103S, U19-ch2, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 52.94
Std Dev 7.458
Entry
ampl
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2
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0
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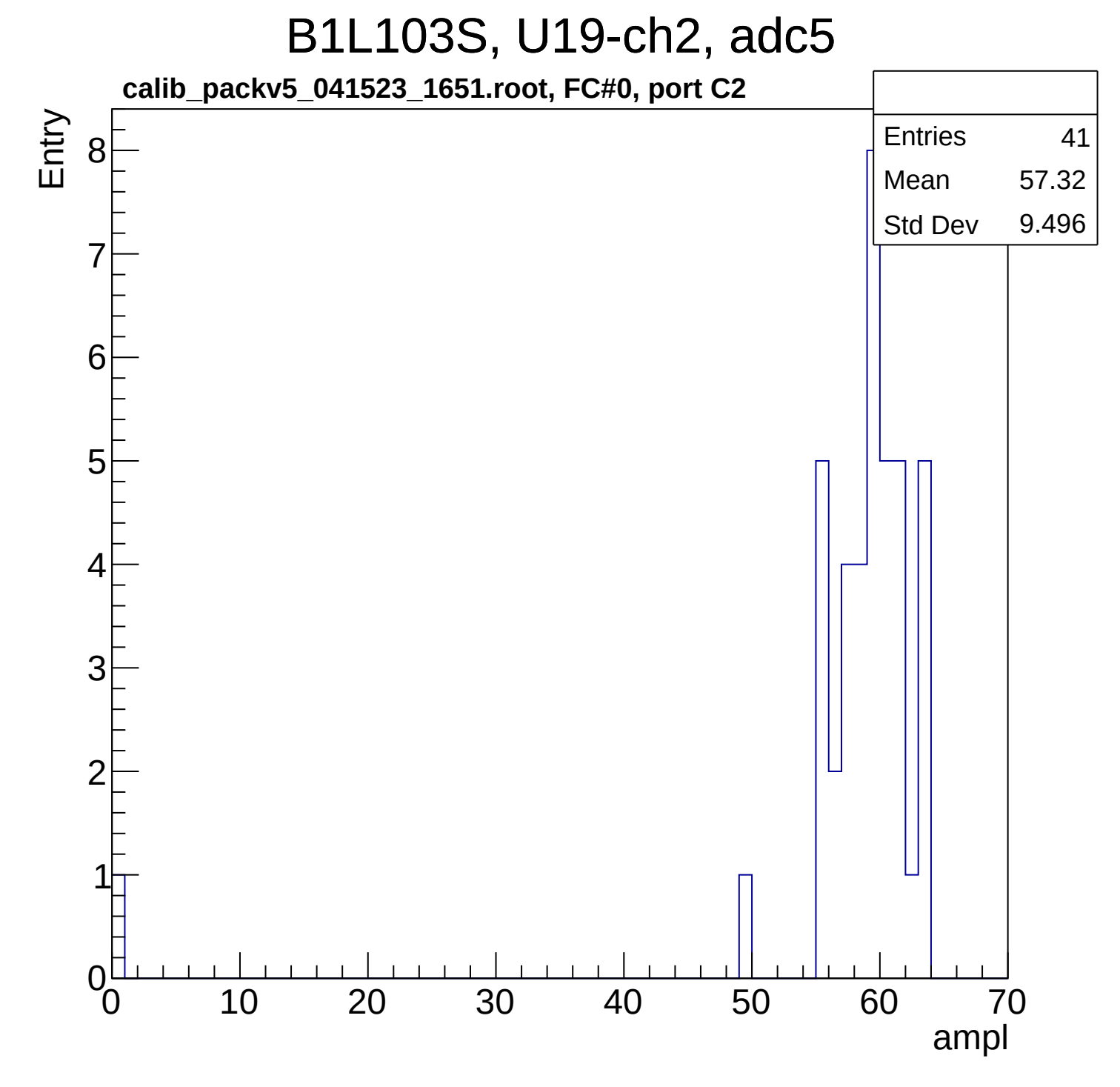
B1L103S, U19-ch2, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 57.32
Std Dev 9.496
Entry
ampl
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2
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4
5
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0
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60
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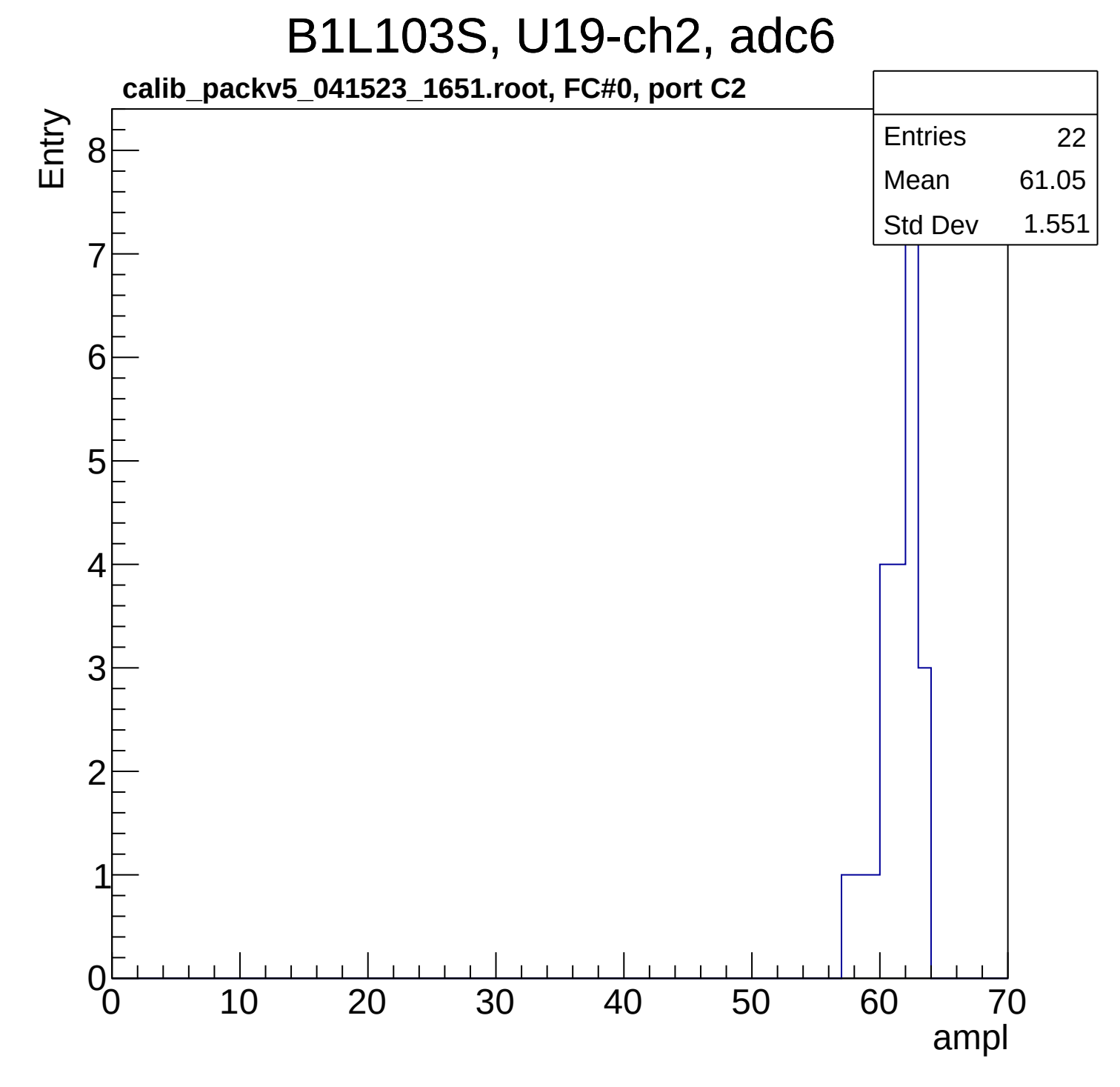
B1L103S, U19-ch2, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 61.05
Std Dev 1.551
Entry
ampl
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5
6
7
8
0
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60
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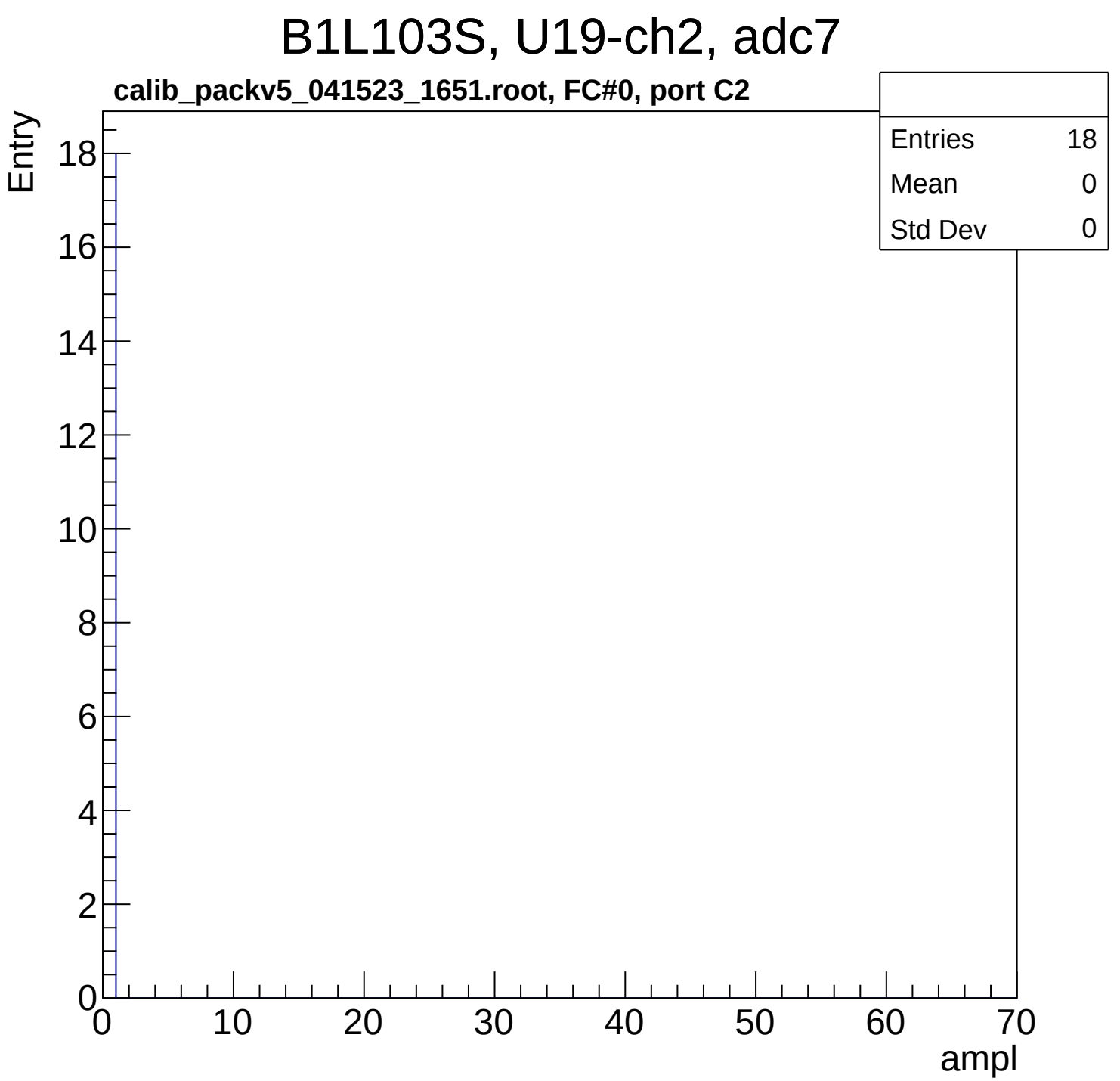
B1L103S, U19-ch2, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
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6
8
10
12
14
16
18
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10
20
30
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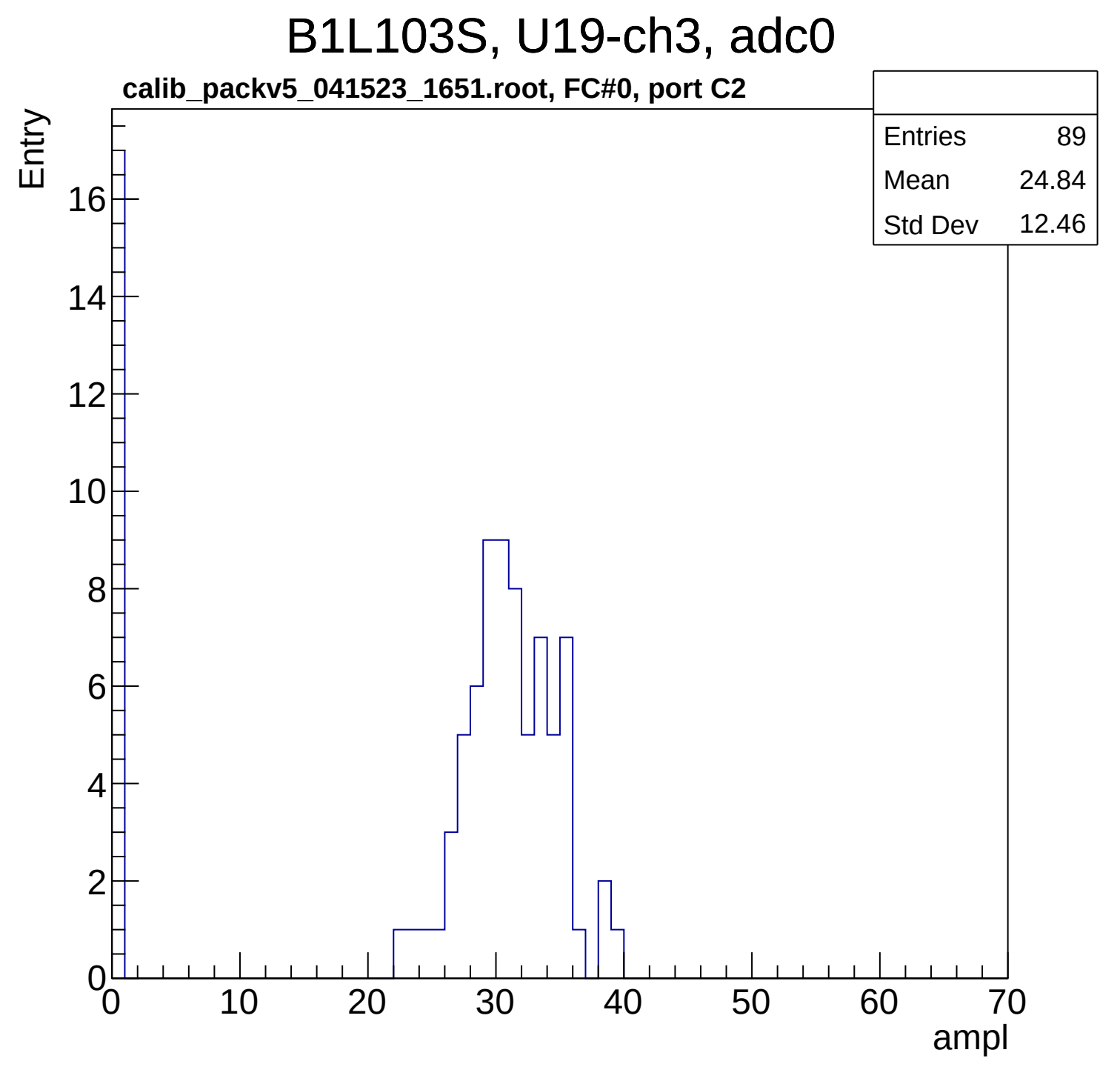
50
60
70
ampl


B1L103S, U19-ch3, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 24.84
Std Dev 12.46
Entry
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6
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12
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16
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10
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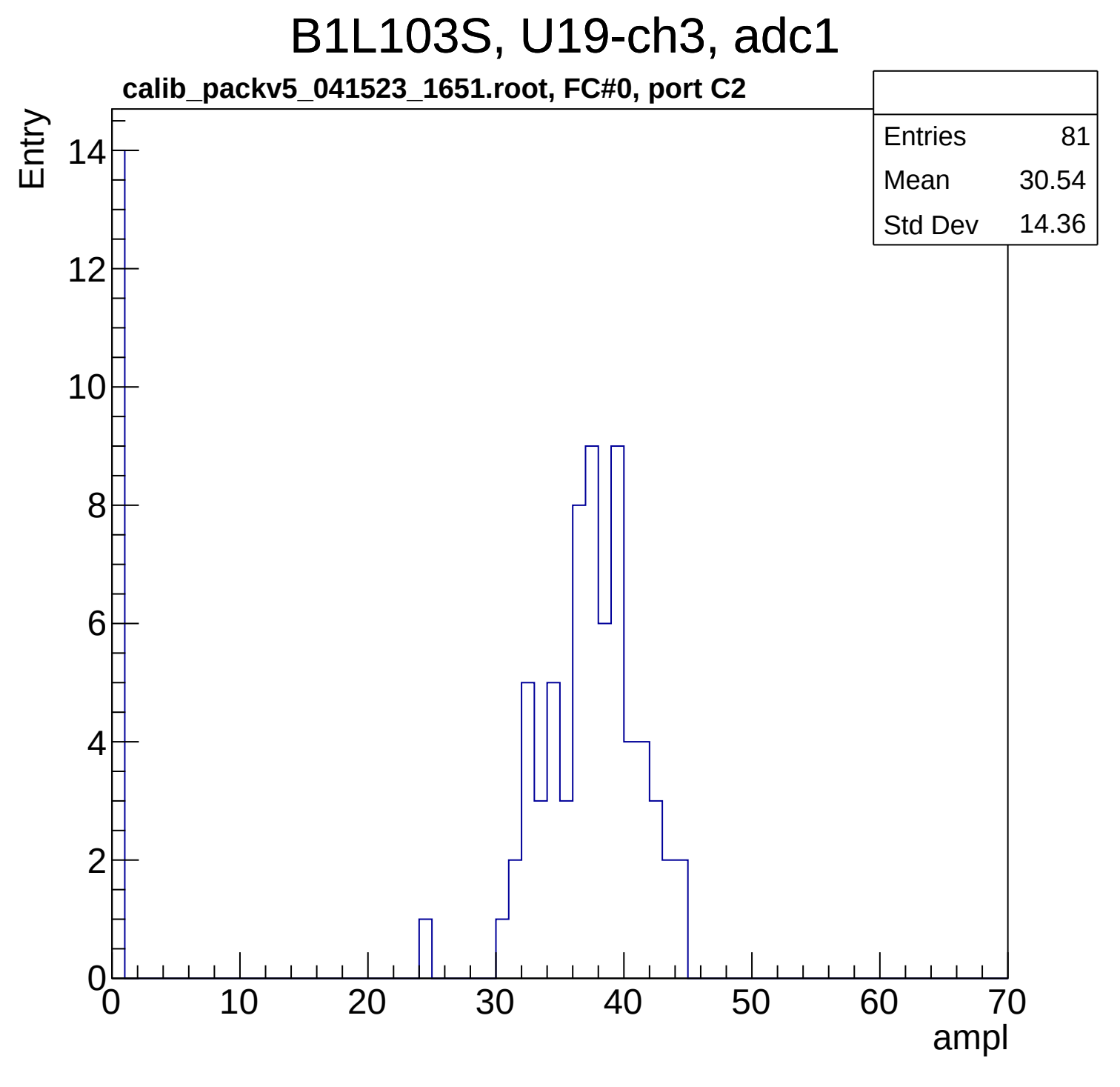
70
ampl


B1L103S, U19-ch3, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 30.54
Std Dev 14.36
Entry
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10
12
14
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10
20
30
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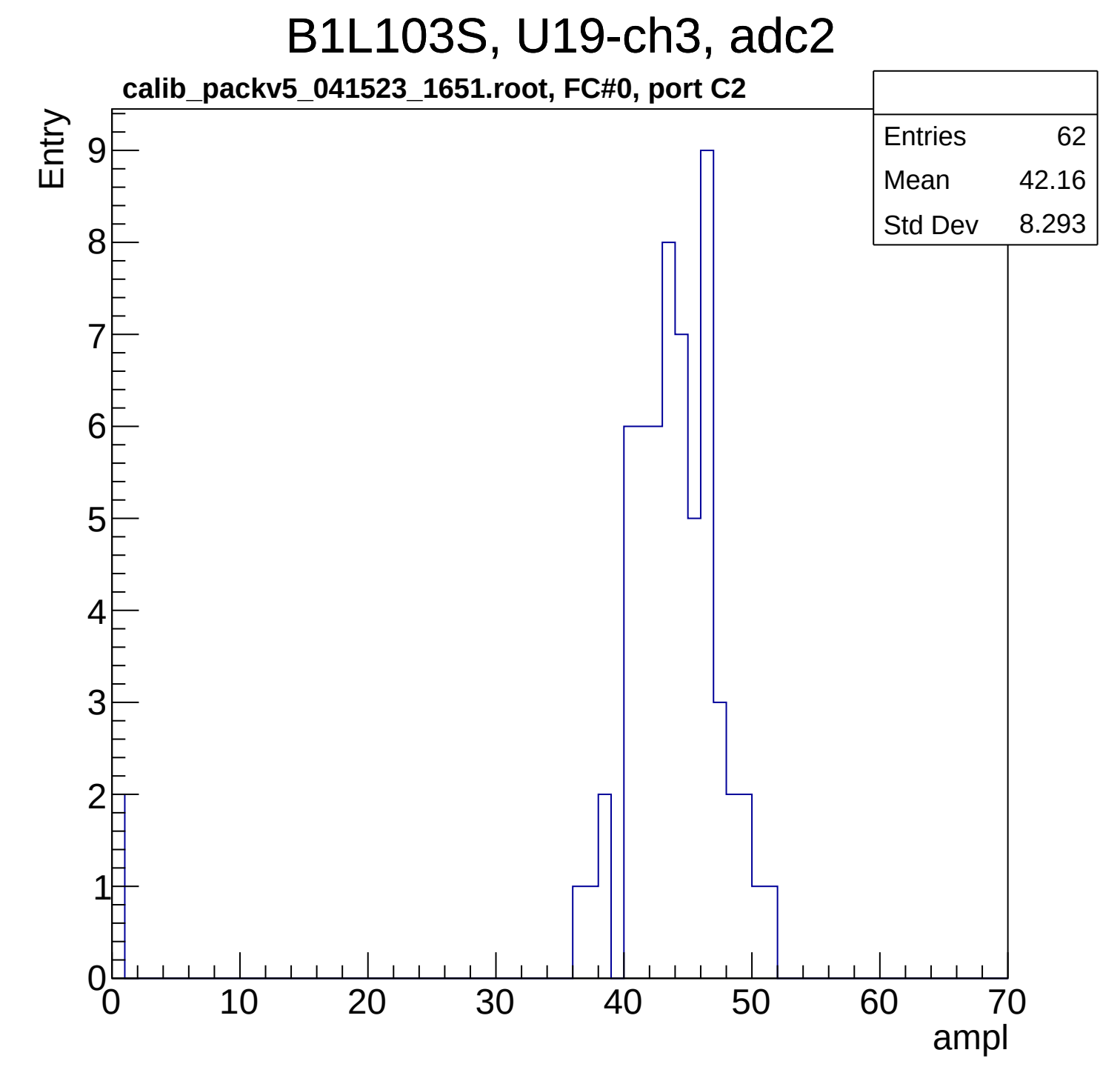
50
60
70
ampl


B1L103S, U19-ch3, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 42.16
Std Dev 8.293
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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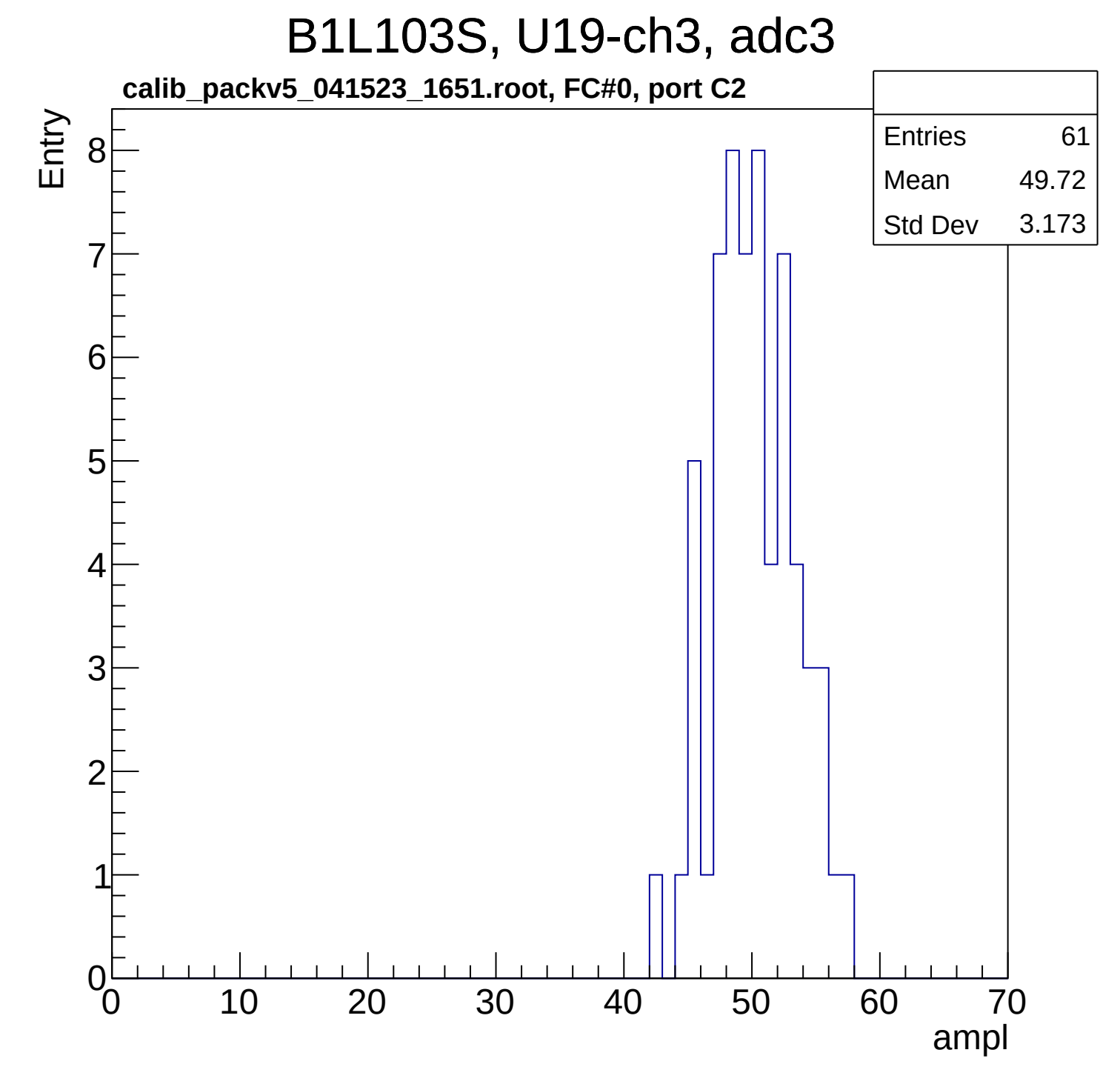
50
60
70


B1L103S, U19-ch3, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 49.72
Std Dev 3.173
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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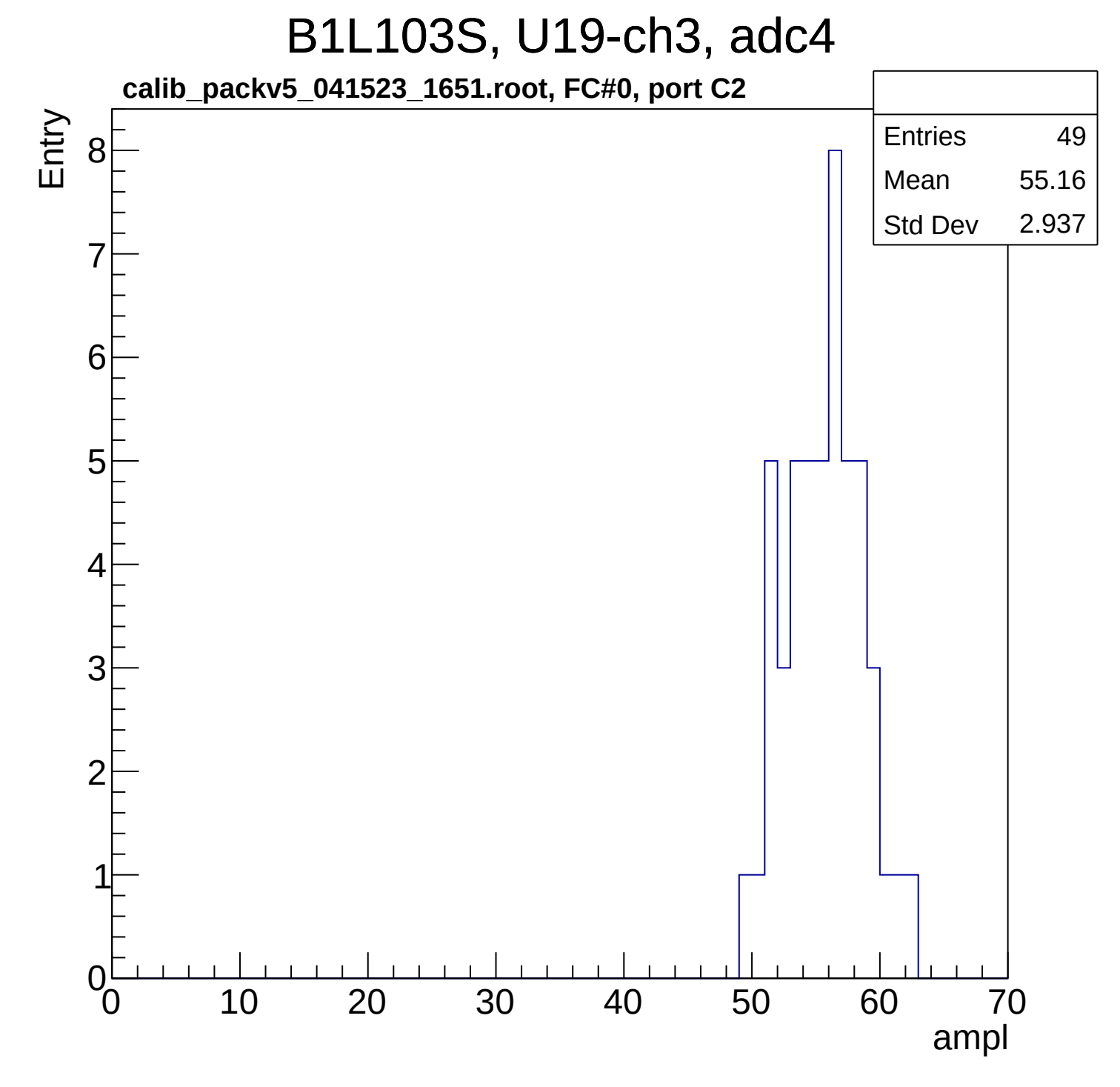
40
50
60
70


B1L103S, U19-ch3, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 55.16
Std Dev 2.937
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
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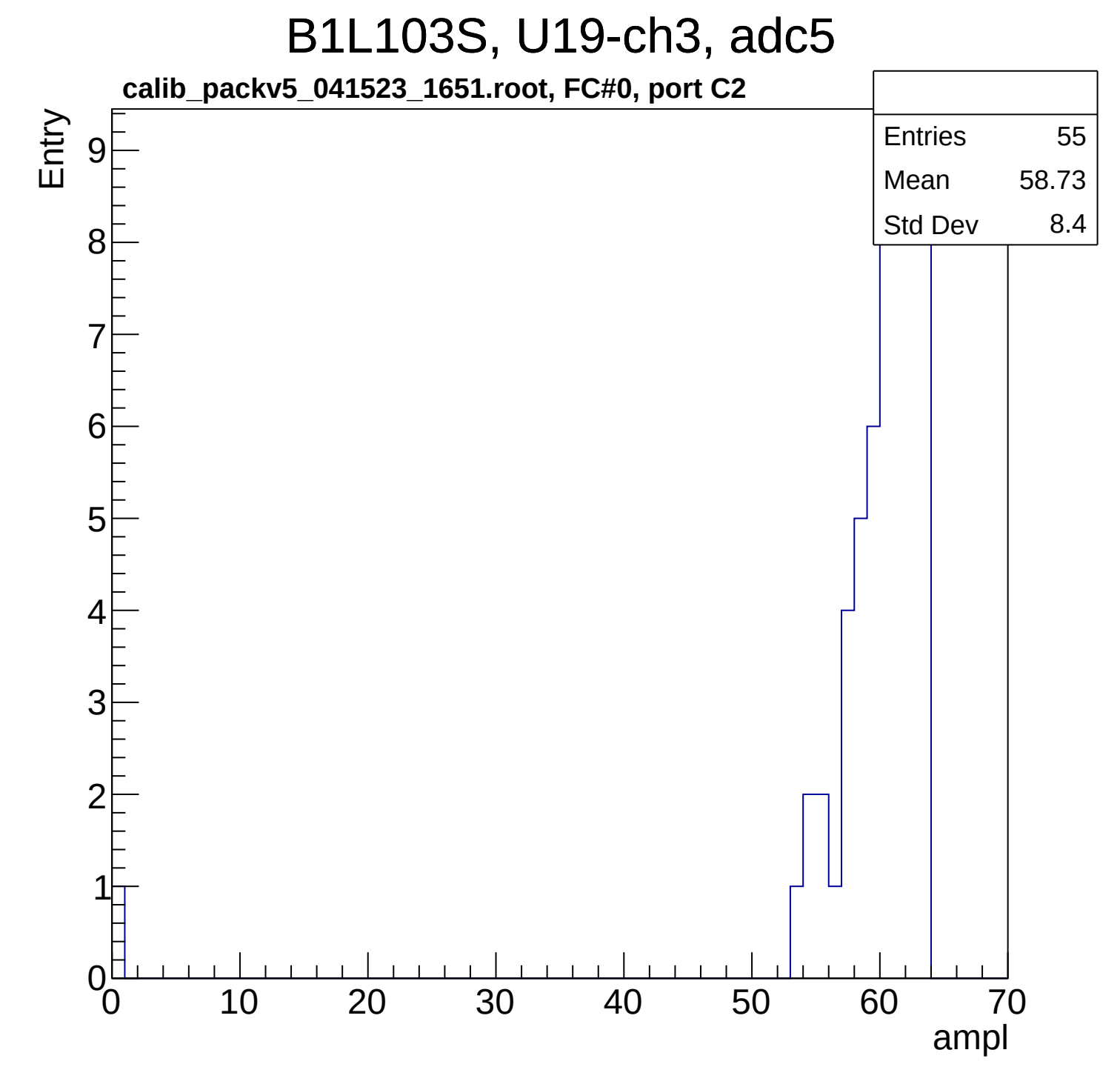
60
70


B1L103S, U19-ch3, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 58.73
Std Dev 8.4
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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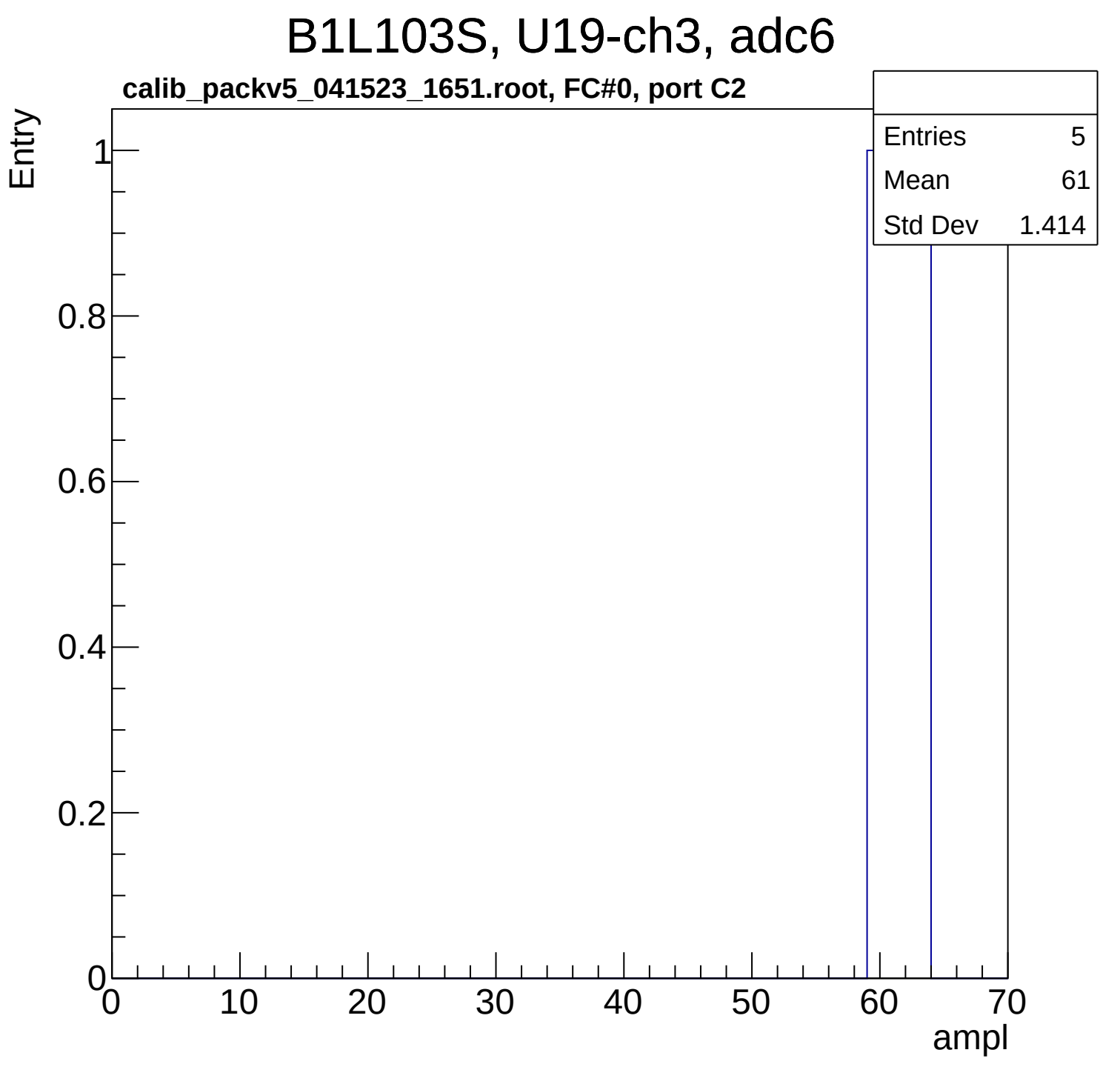
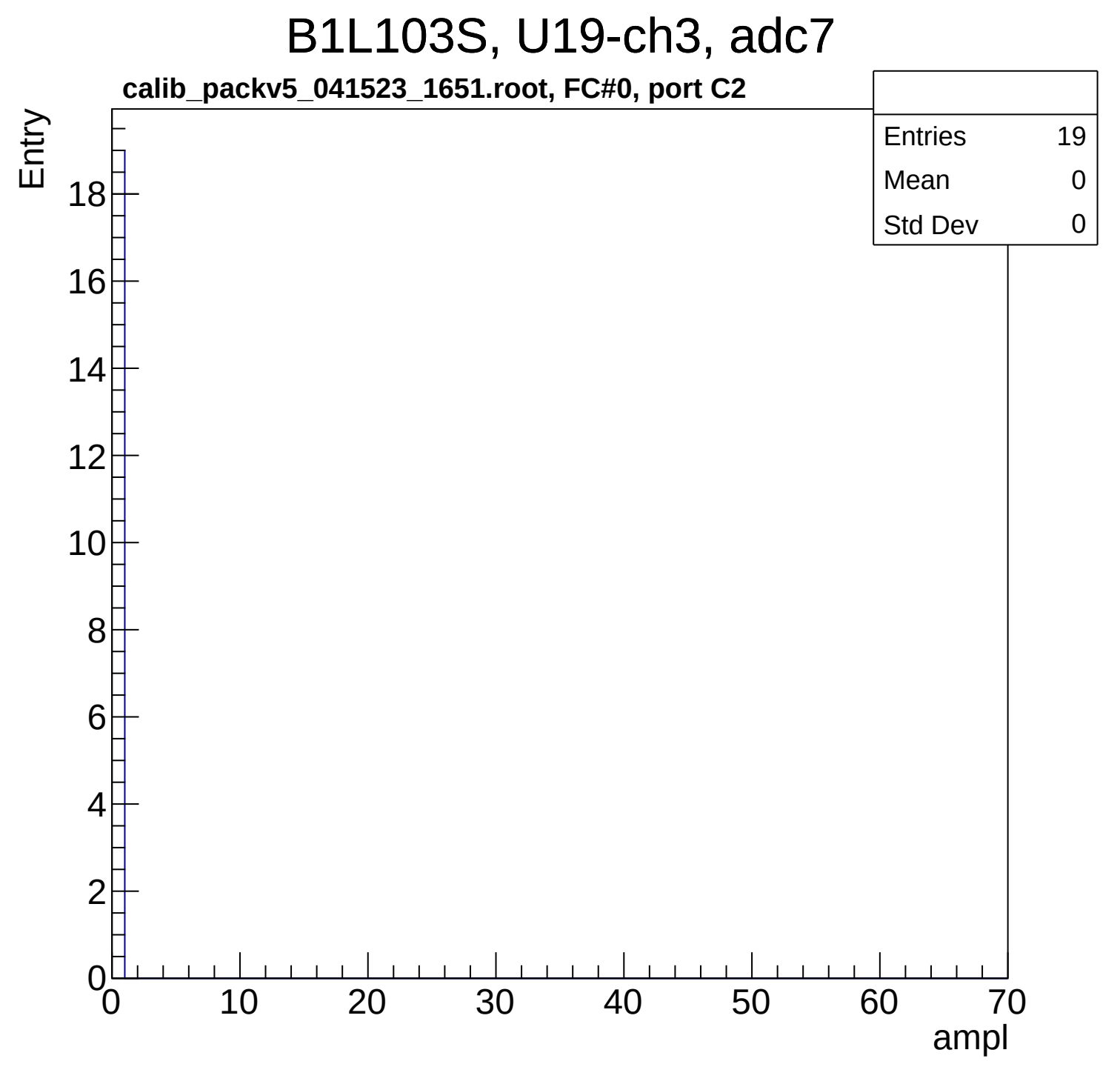
40
50
60
70


B1L103S, U19-ch3, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 61
Std Dev 1.414
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch3, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
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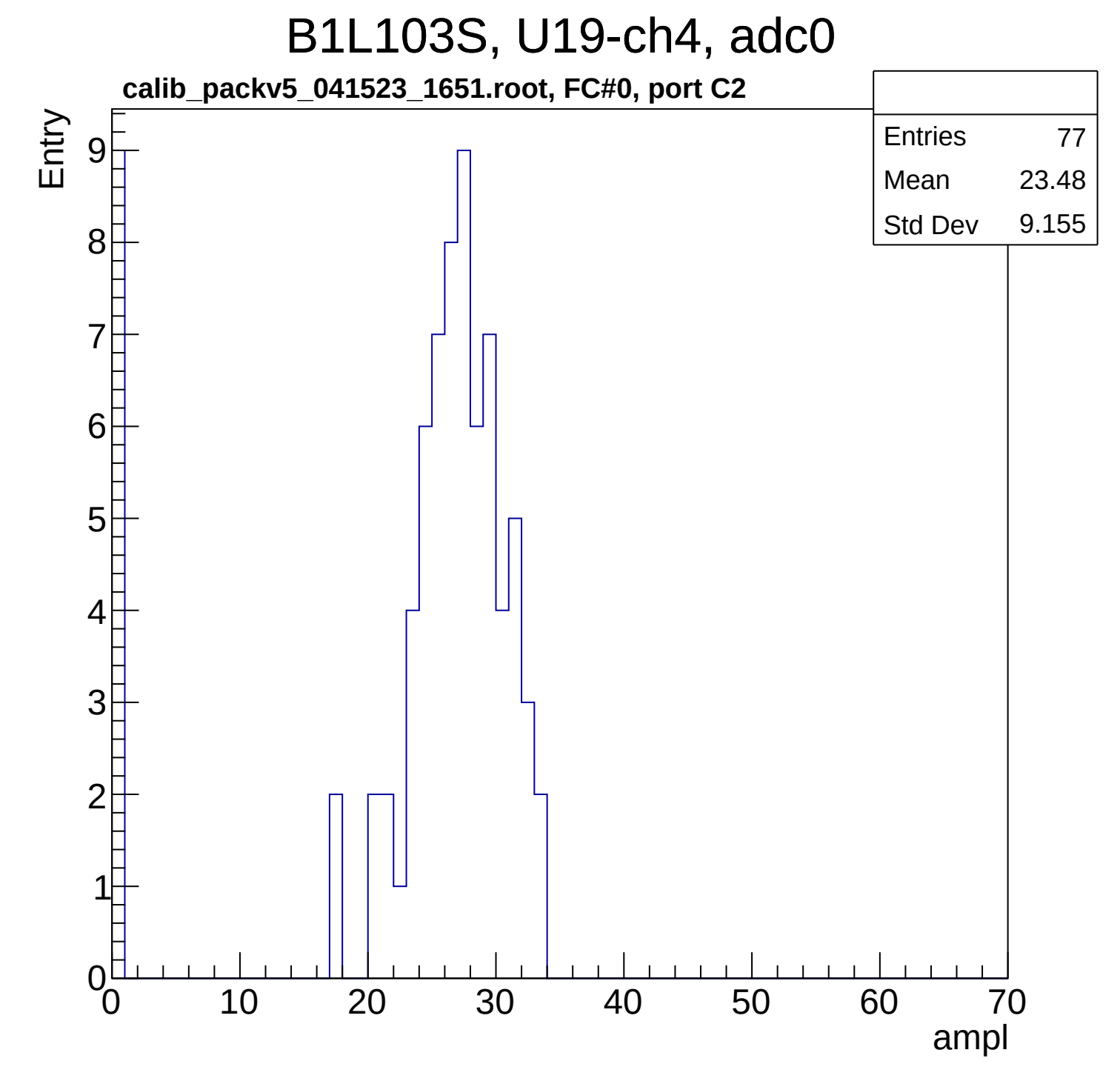
50
60
70
ampl


B1L103S, U19-ch4, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 23.48
Std Dev 9.155
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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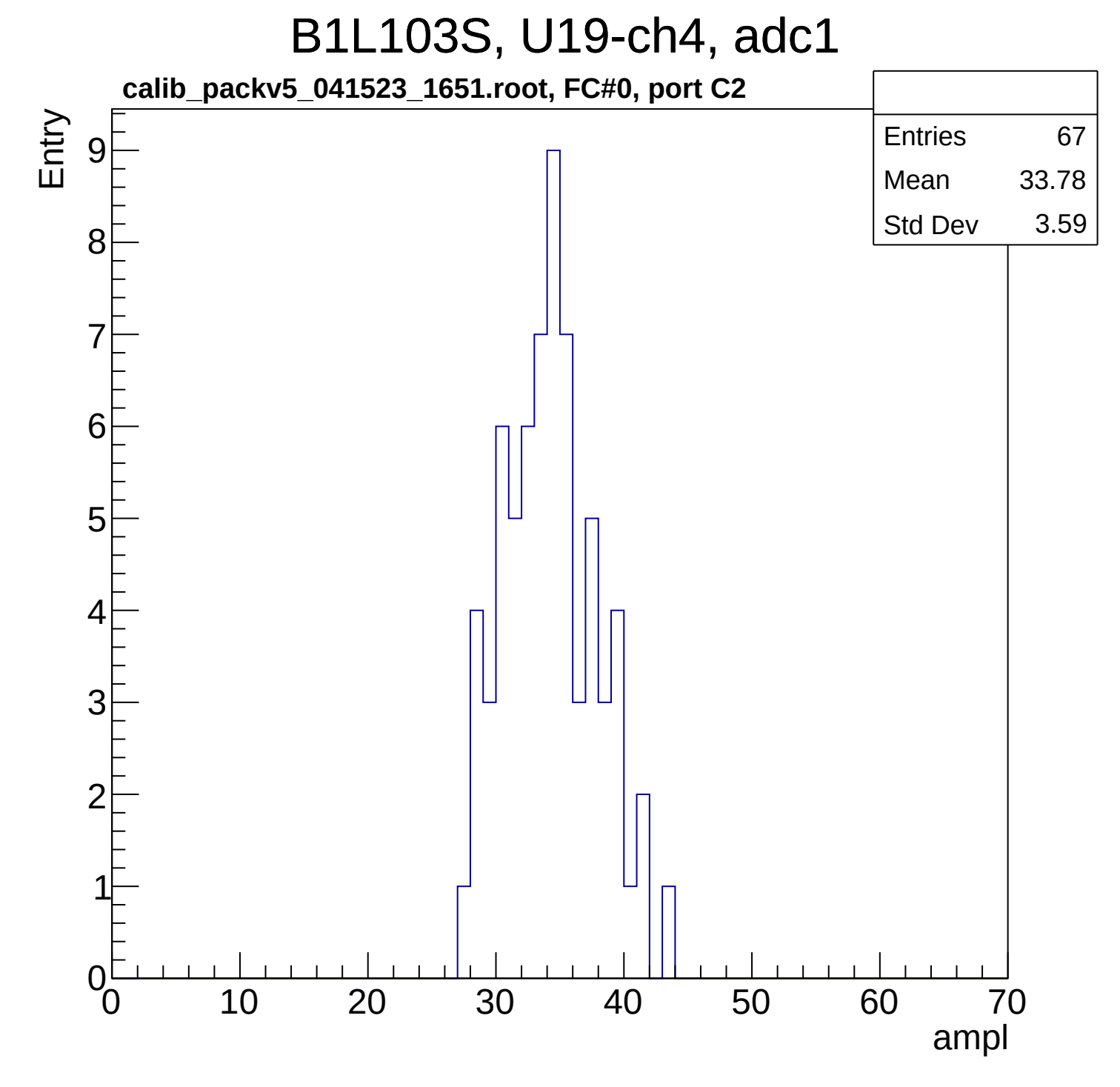
40
50
60
70


B1L103S, U19-ch4, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 33.78
Std Dev 3.59
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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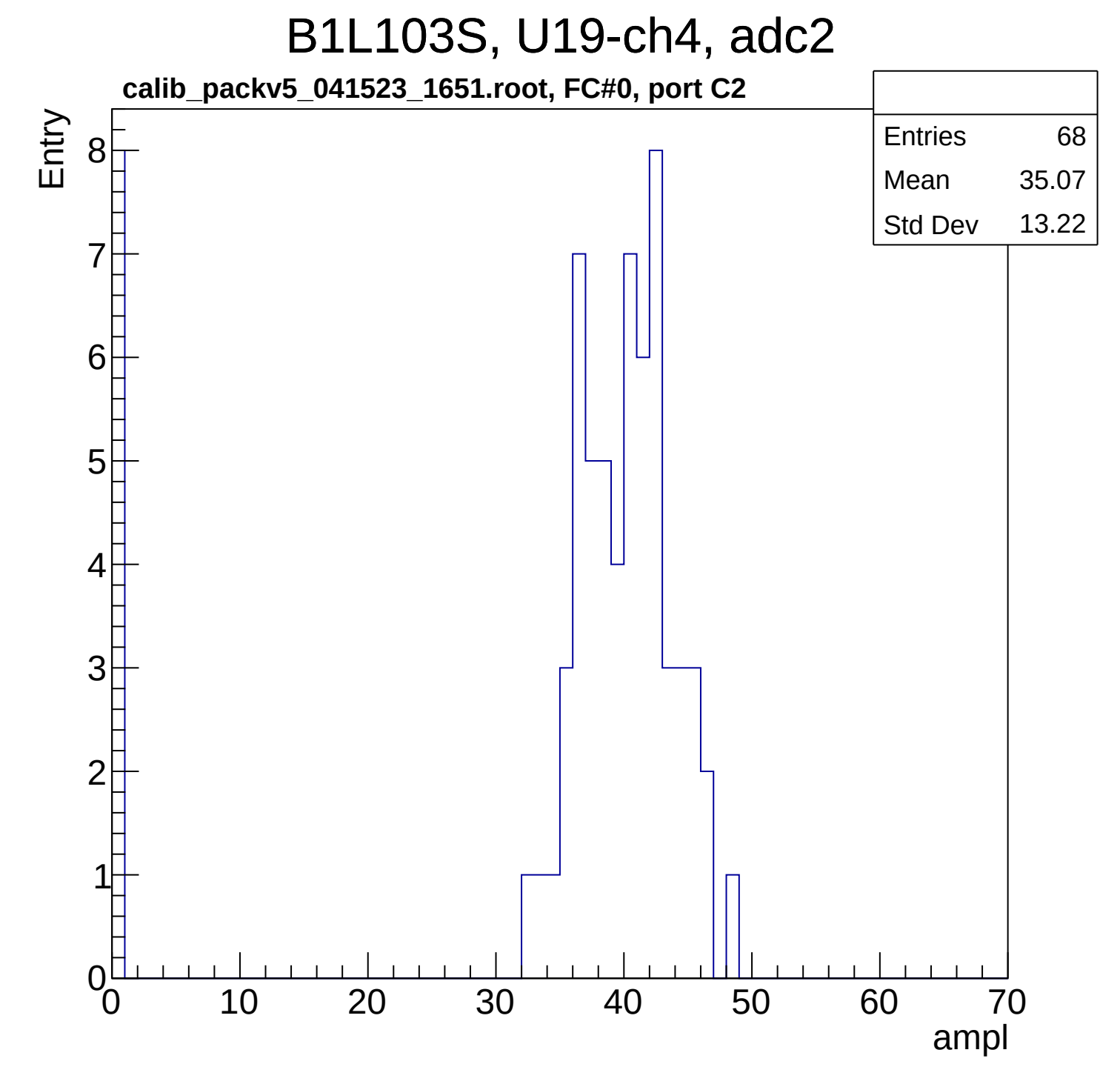
40
50
60
70


B1L103S, U19-ch4, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 35.07
Std Dev 13.22
Entry
ampl
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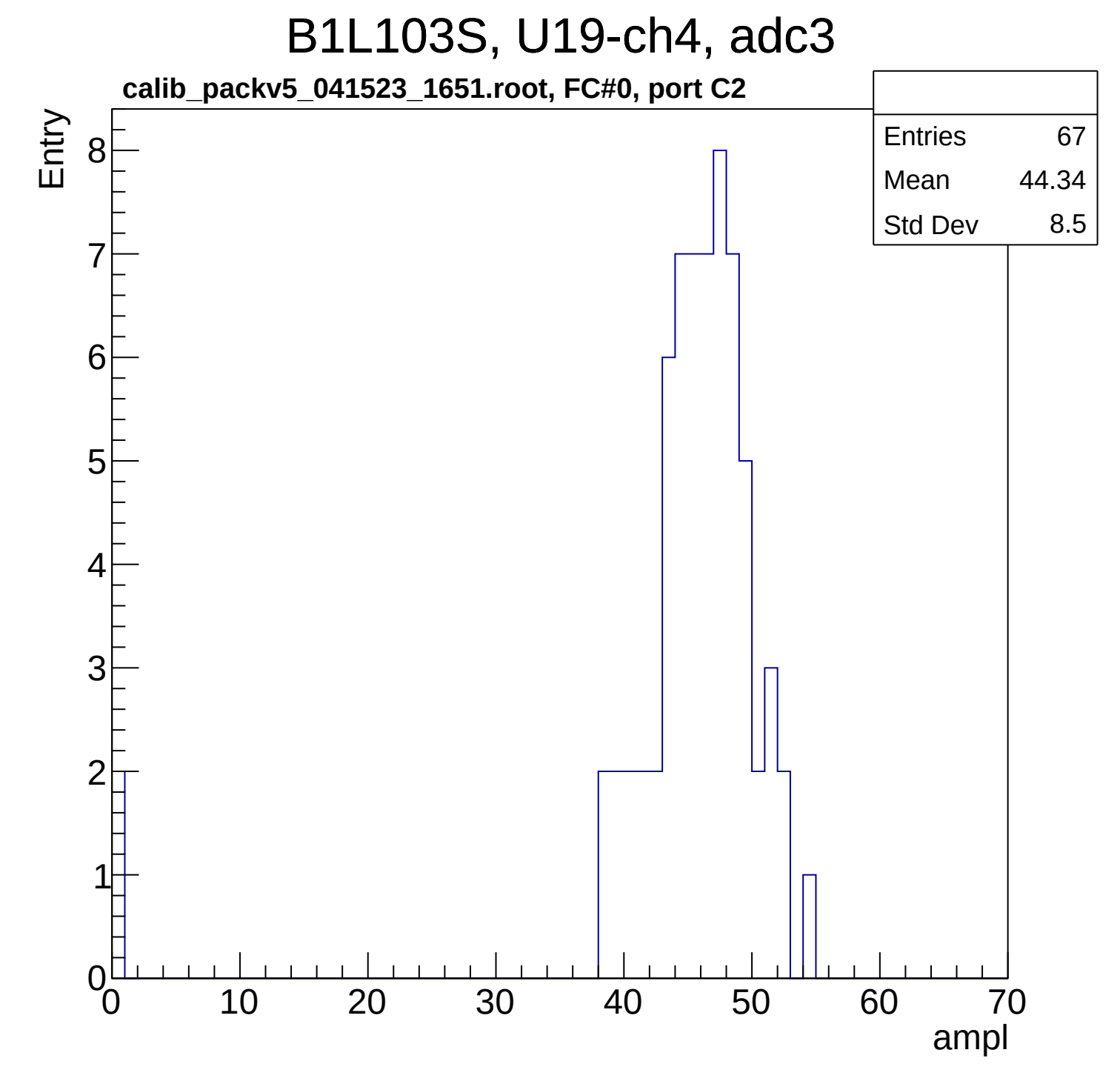
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch4, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 44.34
Std Dev 8.5
Entry
ampl
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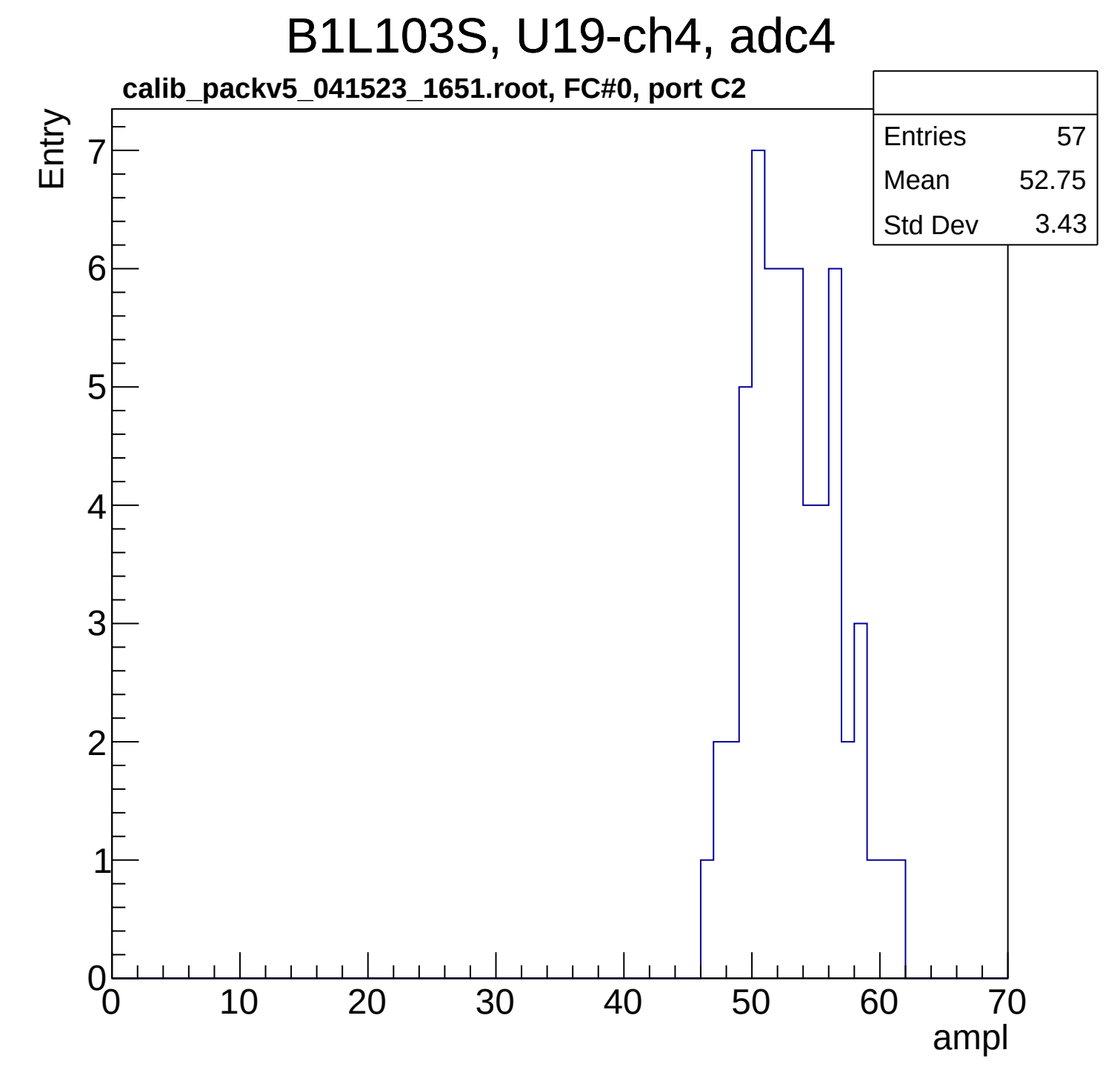
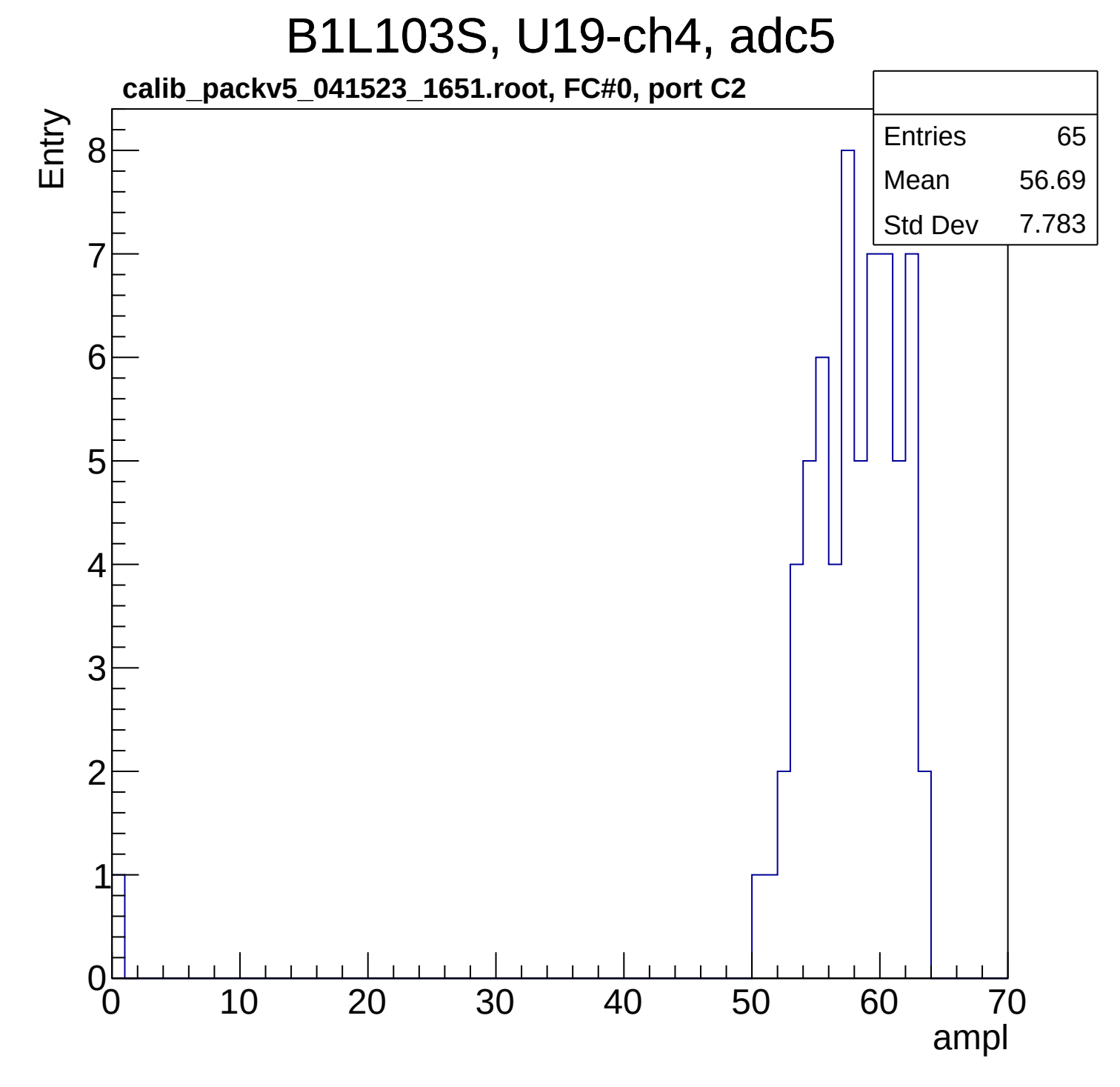
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch4, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 52.75
Std Dev 3.43
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch4, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 56.69
Std Dev 7.783
Entry
ampl
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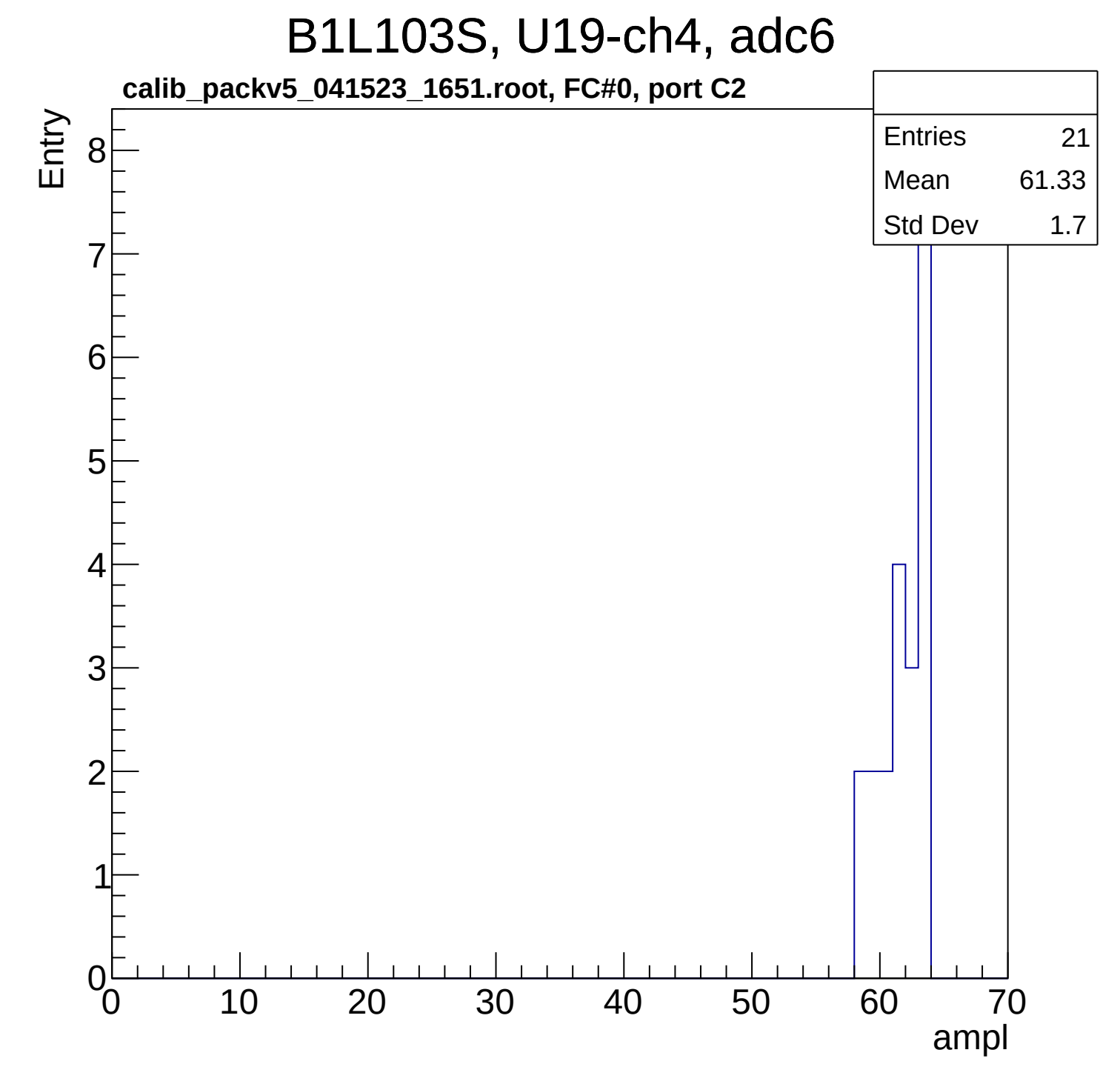
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch4, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 61.33
Std Dev 1.7
Entry
ampl
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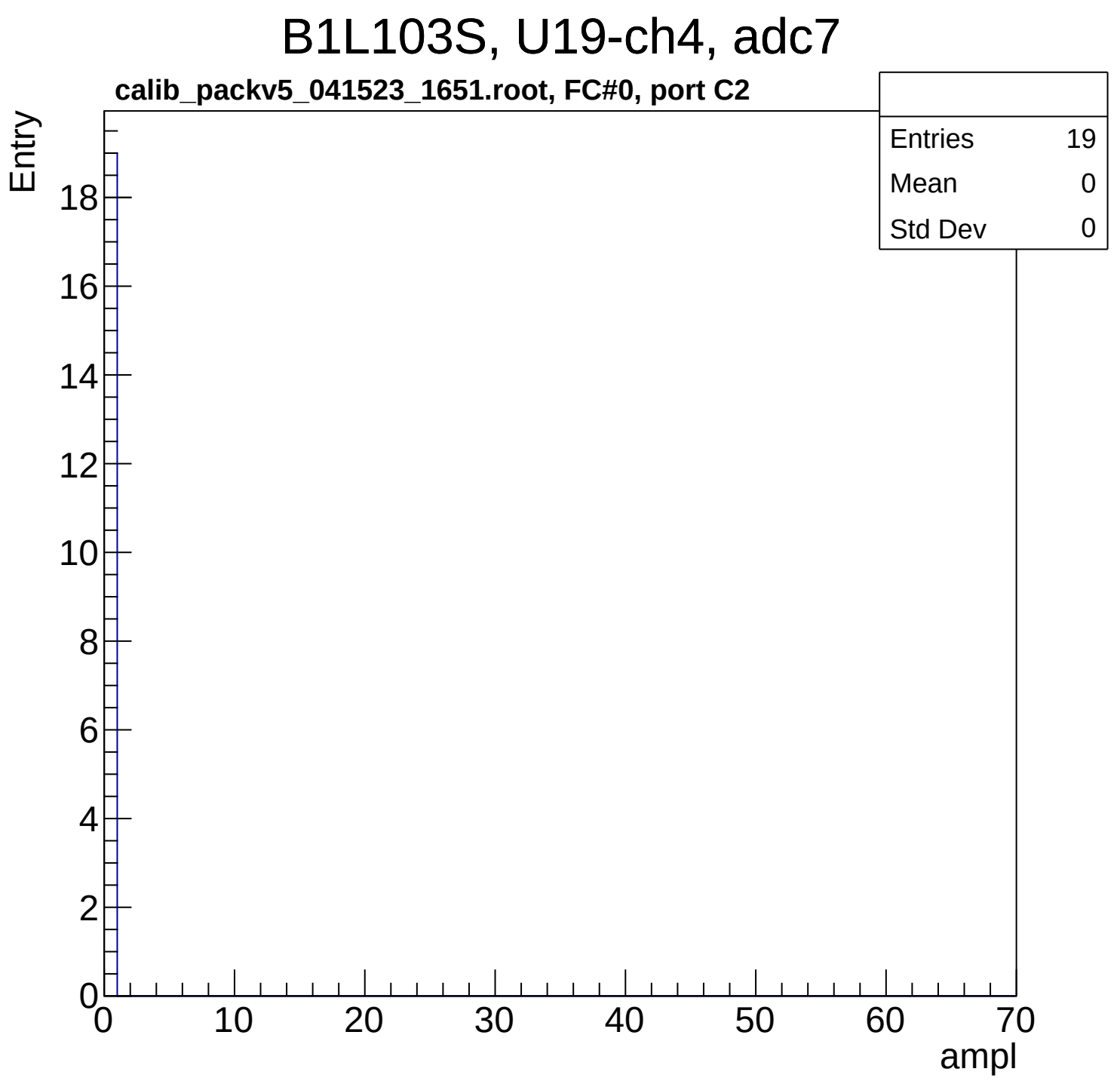
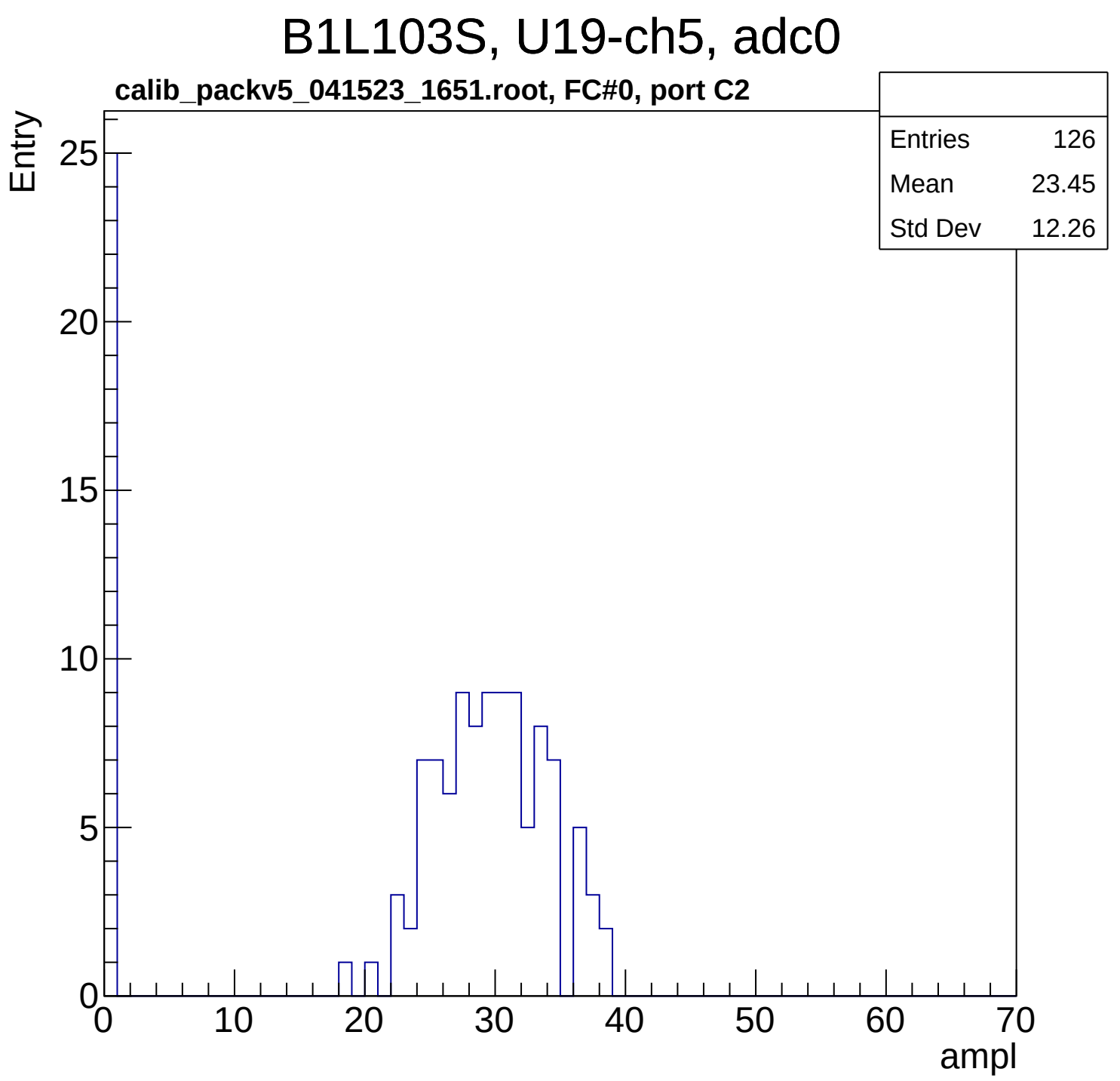
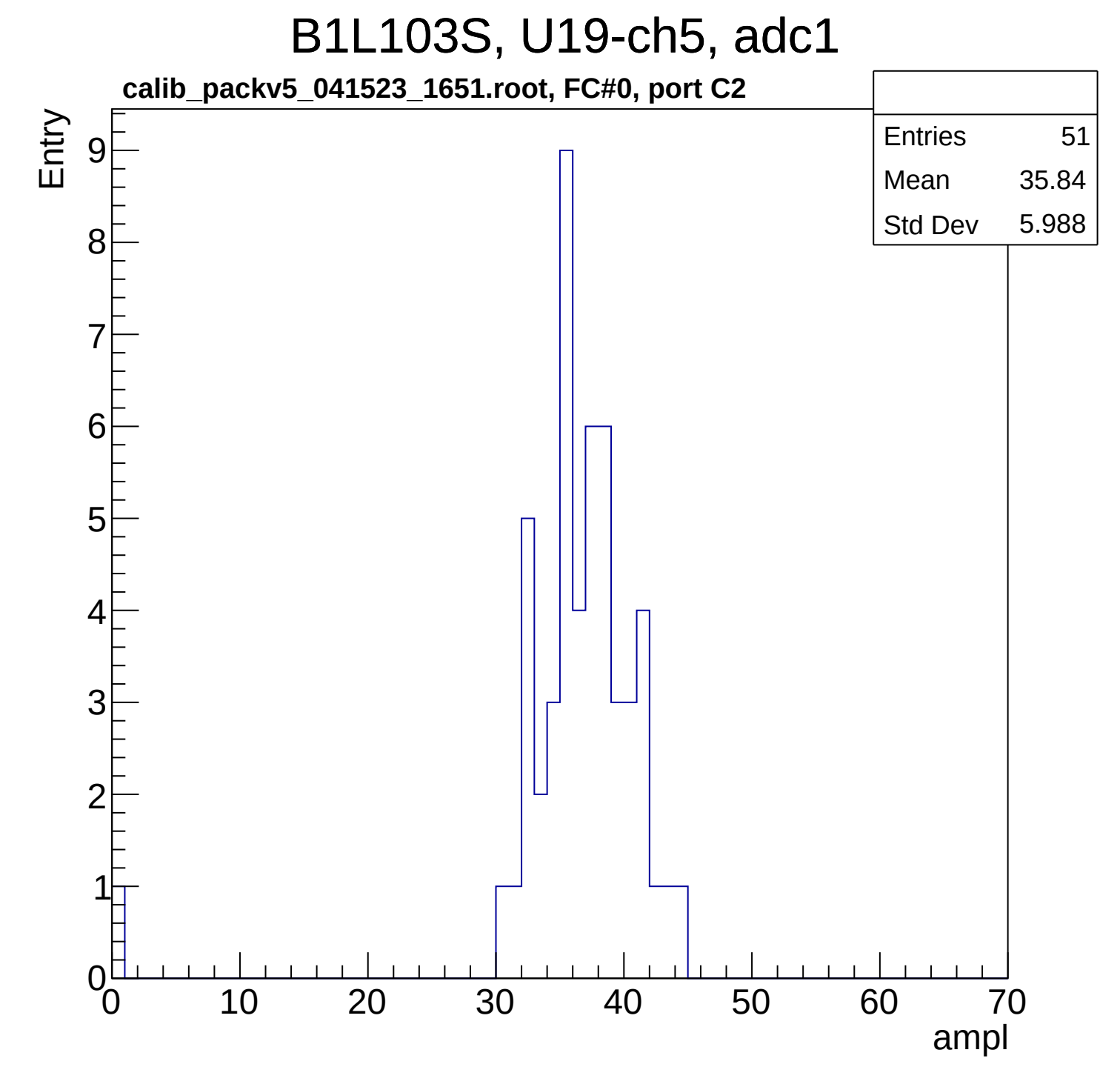
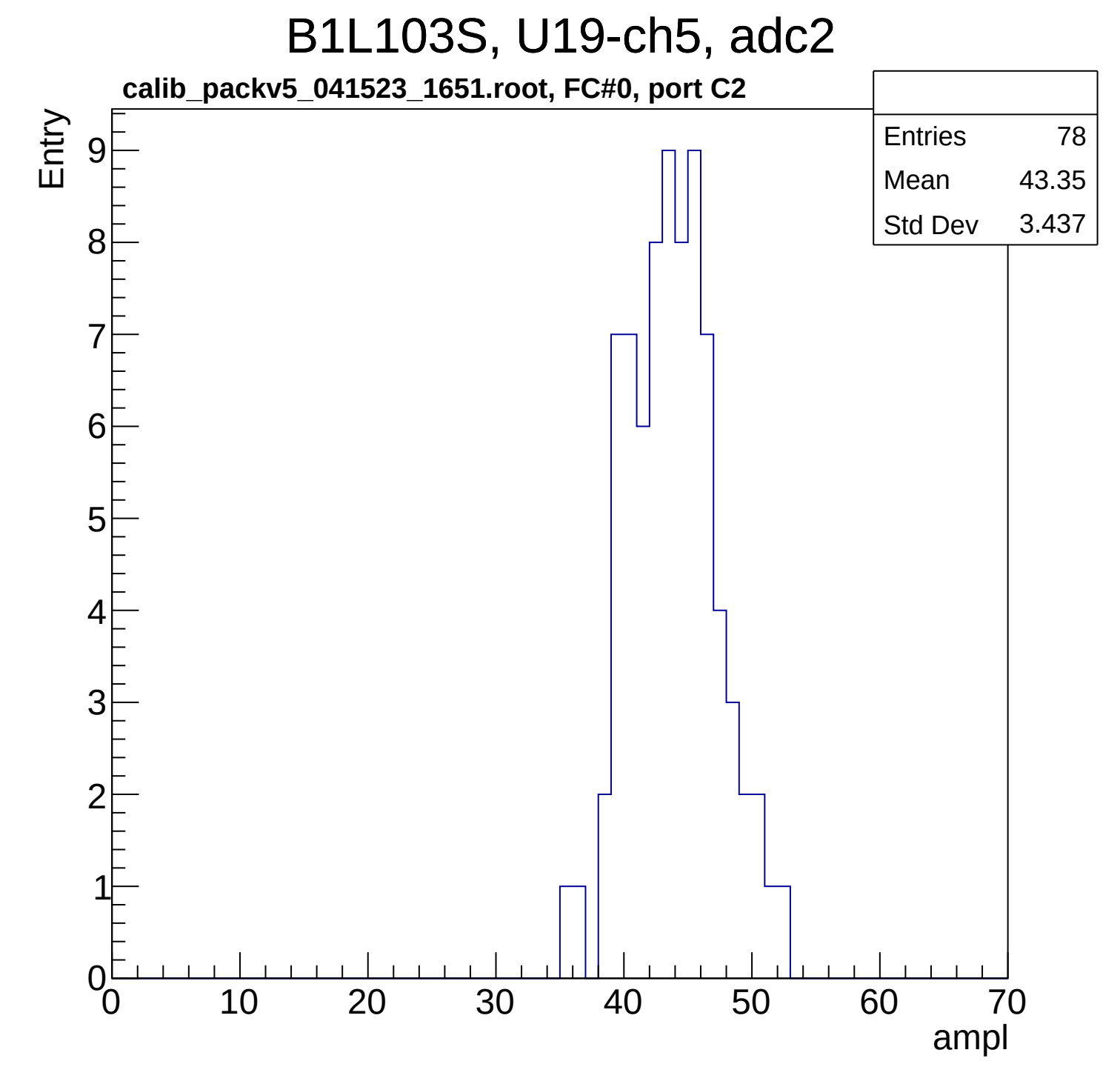
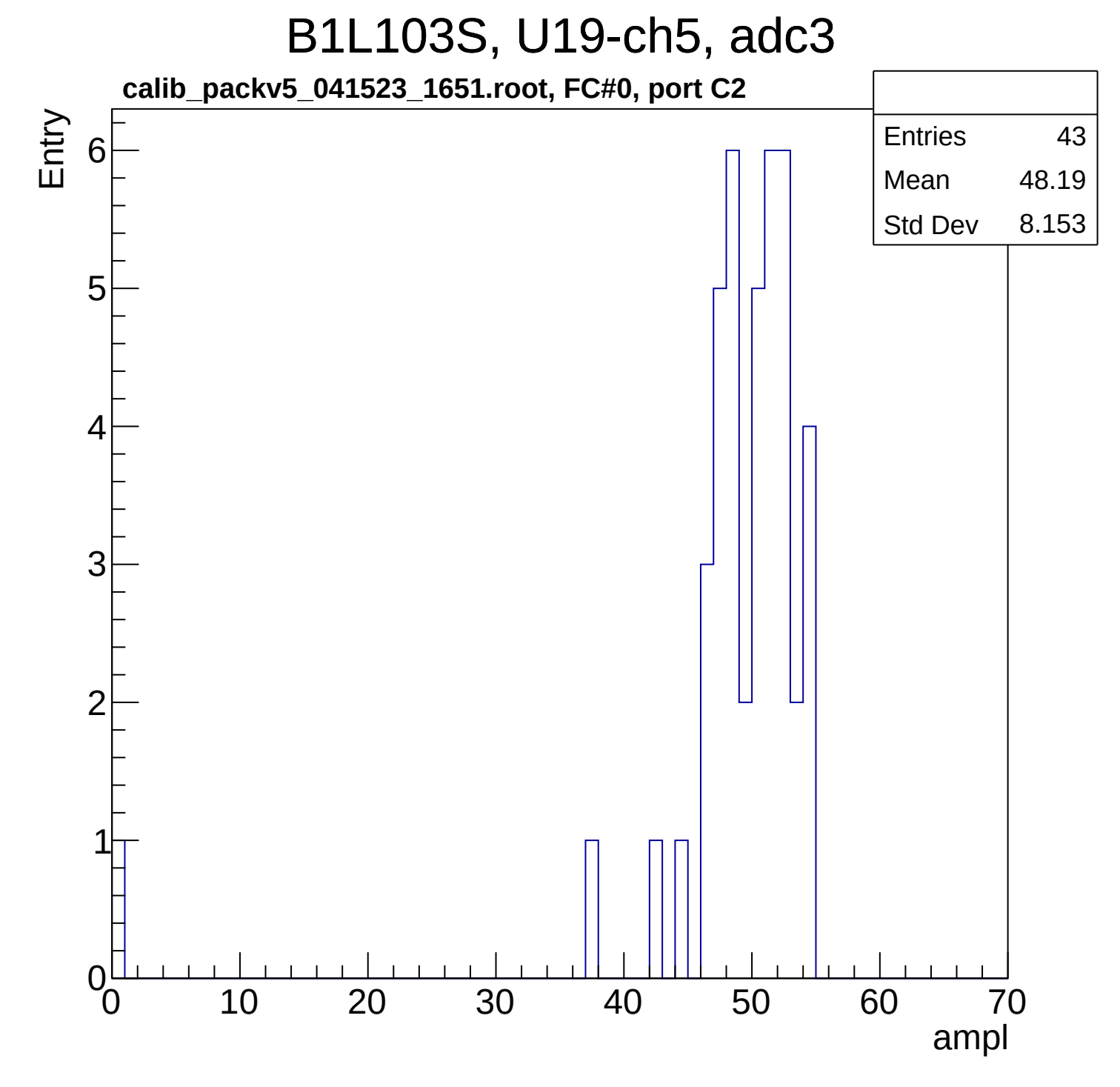
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

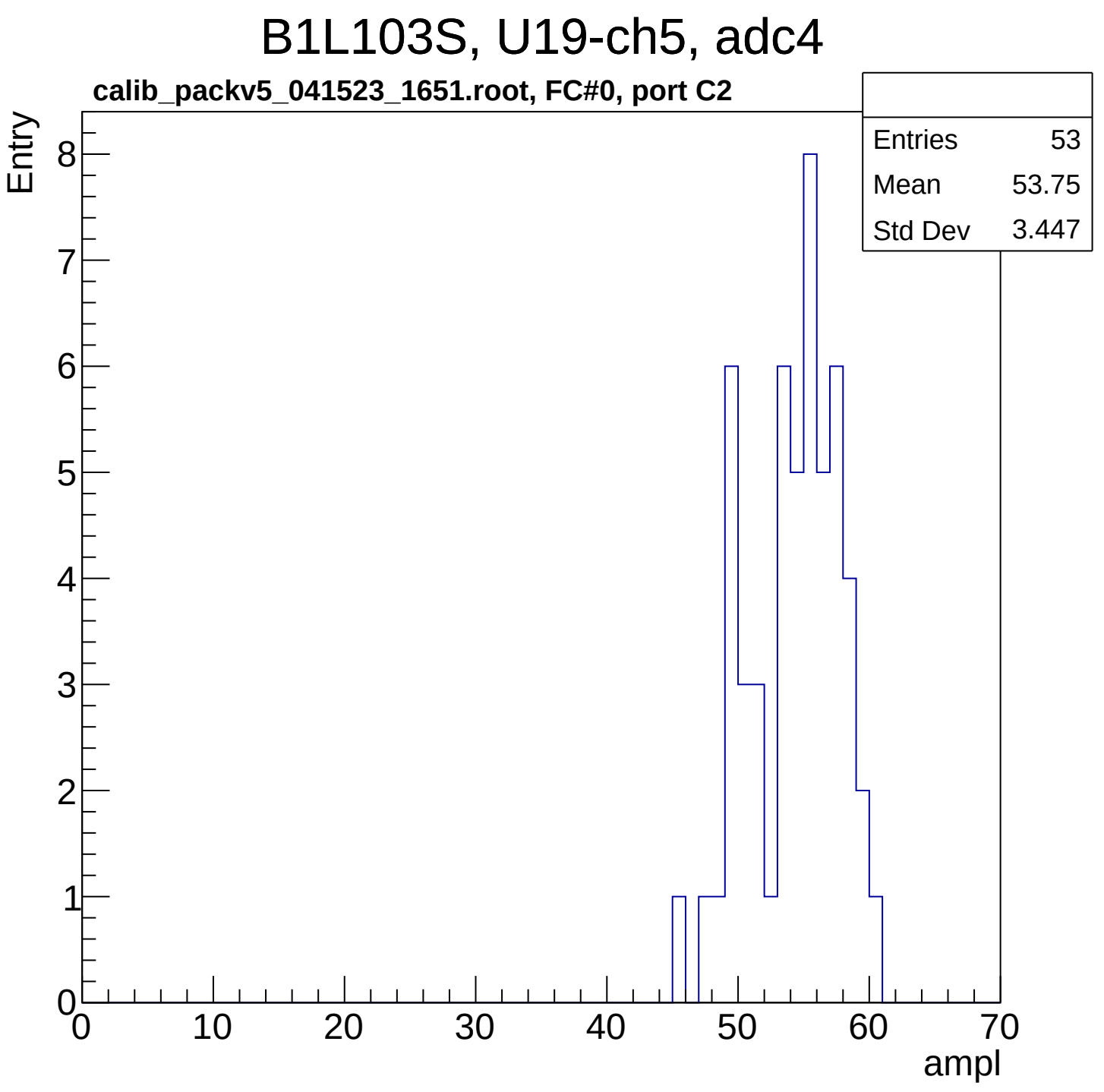

B1L103S, U19-ch4, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

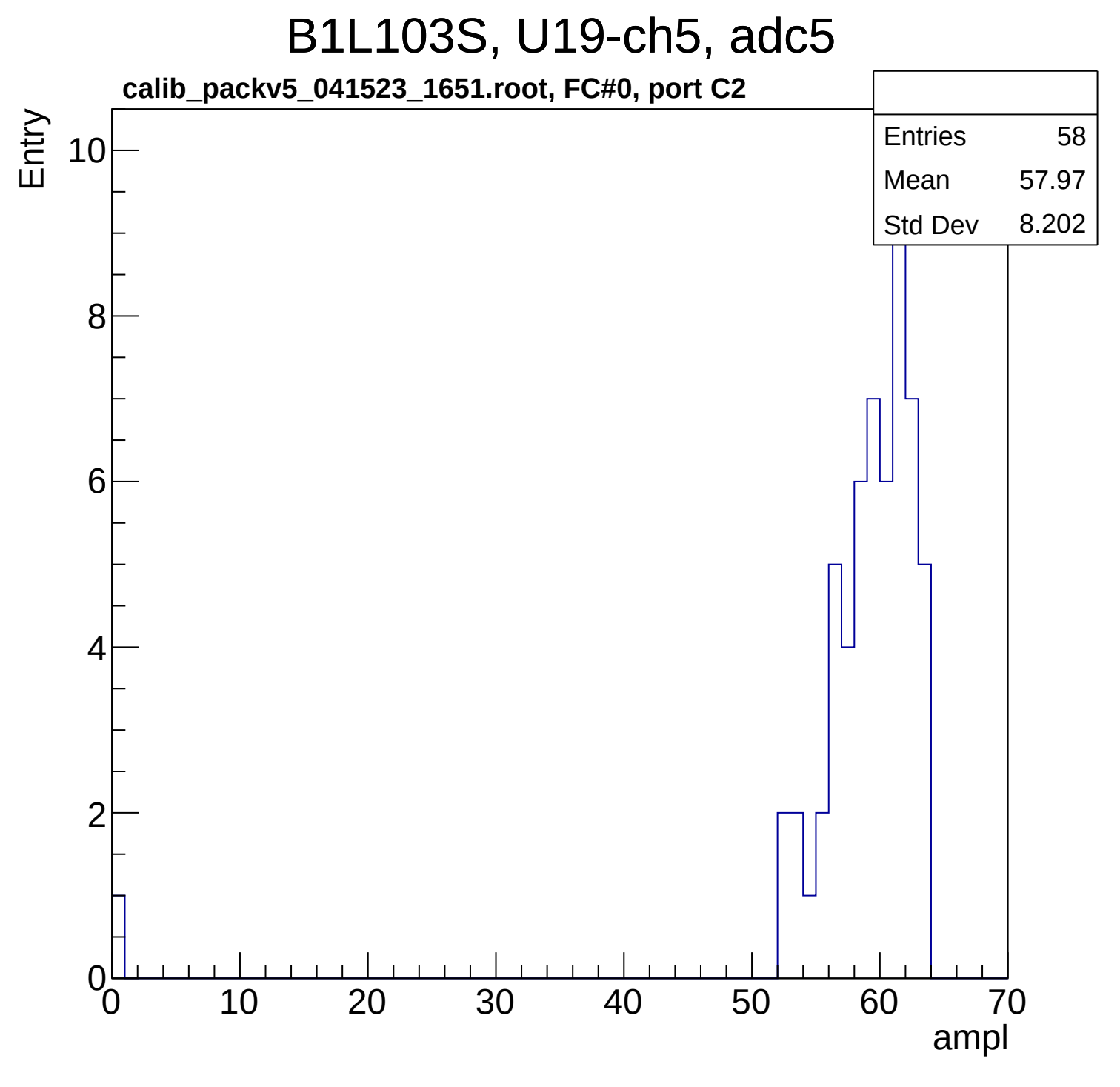

B1L103S, U19-ch5, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 126
Mean 23.45
Std Dev 12.26
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl

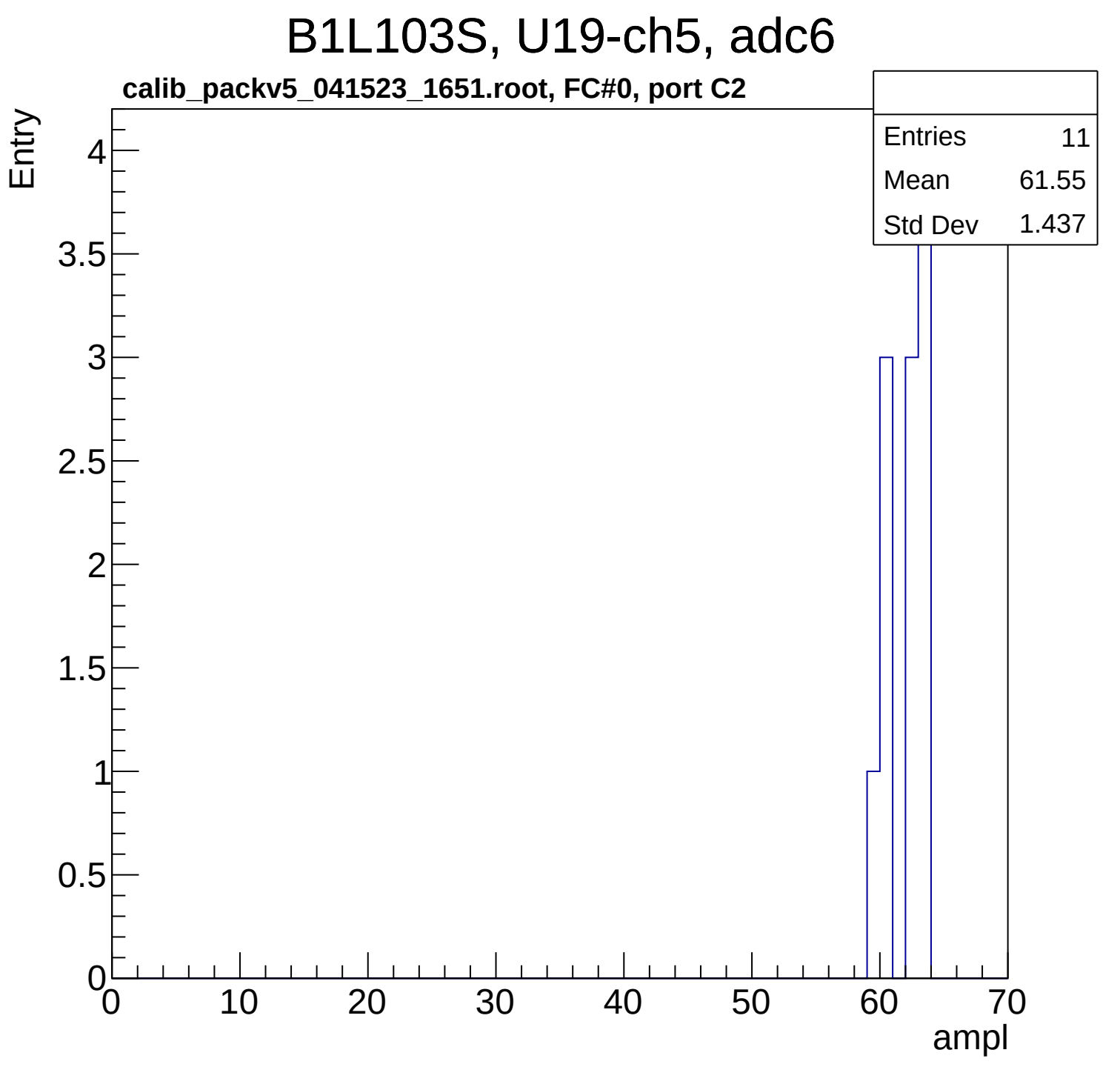

B1L103S, U19-ch5, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 35.84
Std Dev 5.988
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

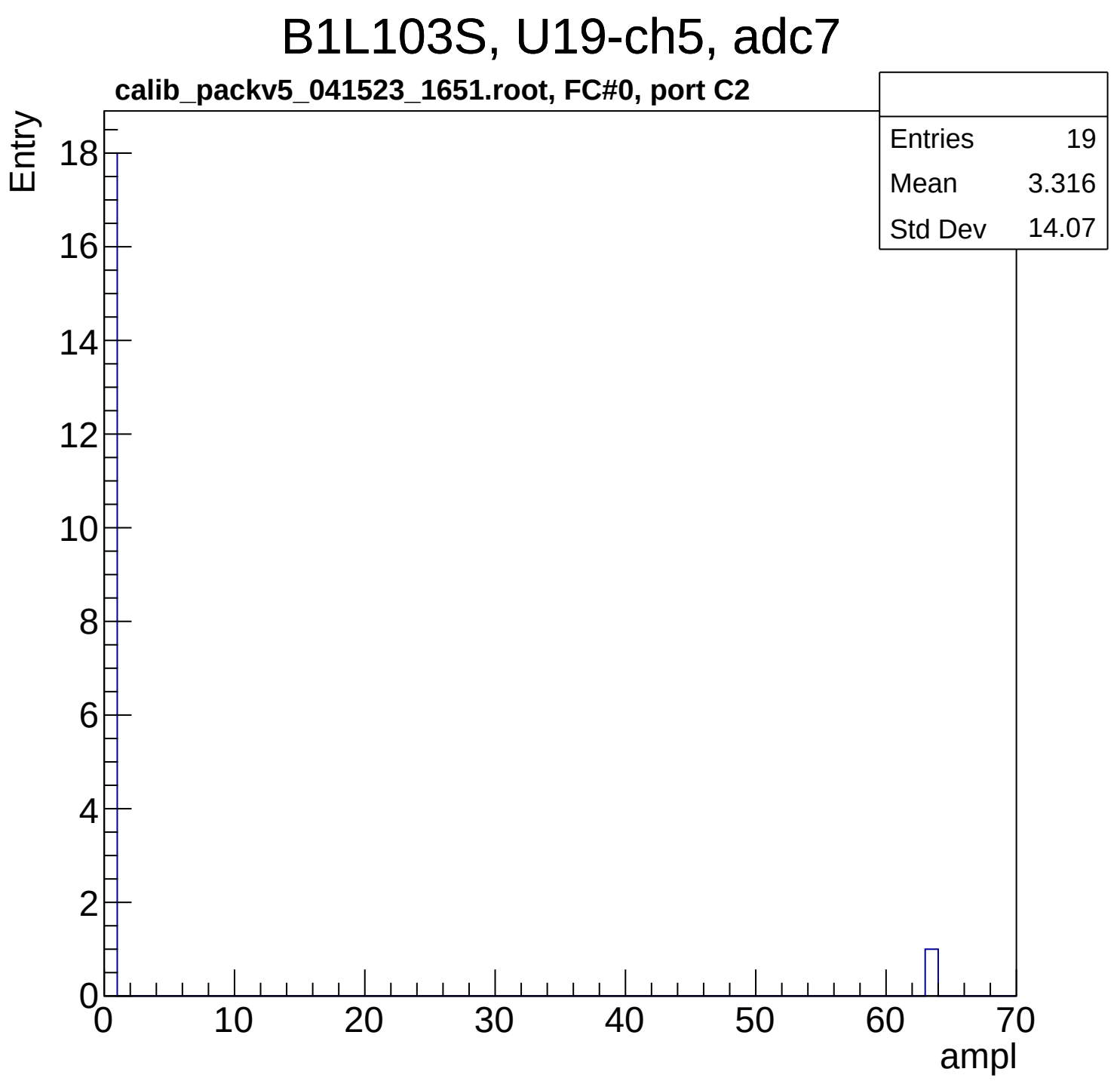

B1L103S, U19-ch5, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 43.35
Std Dev 3.437
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

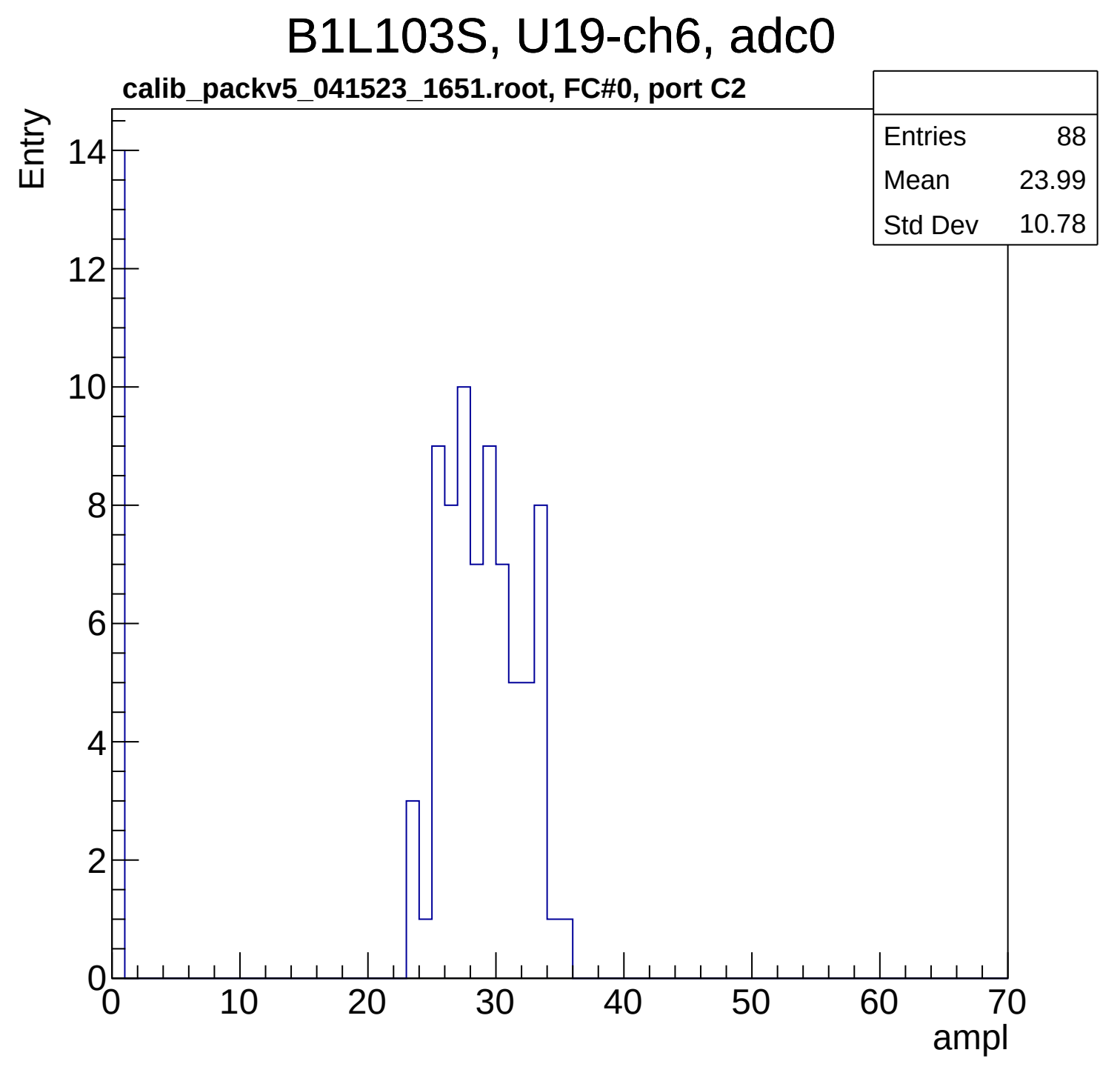

B1L103S, U19-ch5, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 48.19
Std Dev 8.153
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

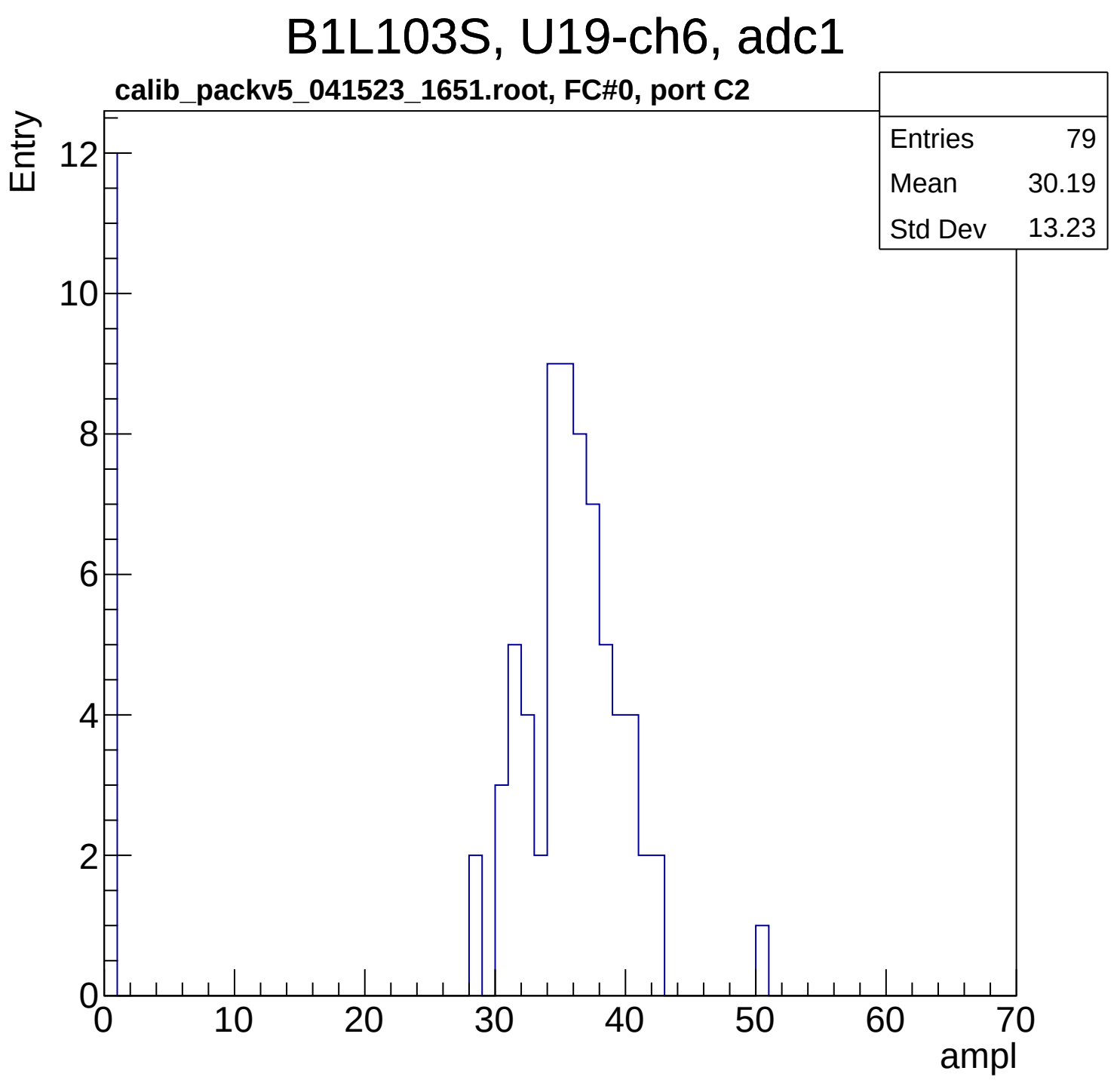

B1L103S, U19-ch5, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 53.75
Std Dev 3.447
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

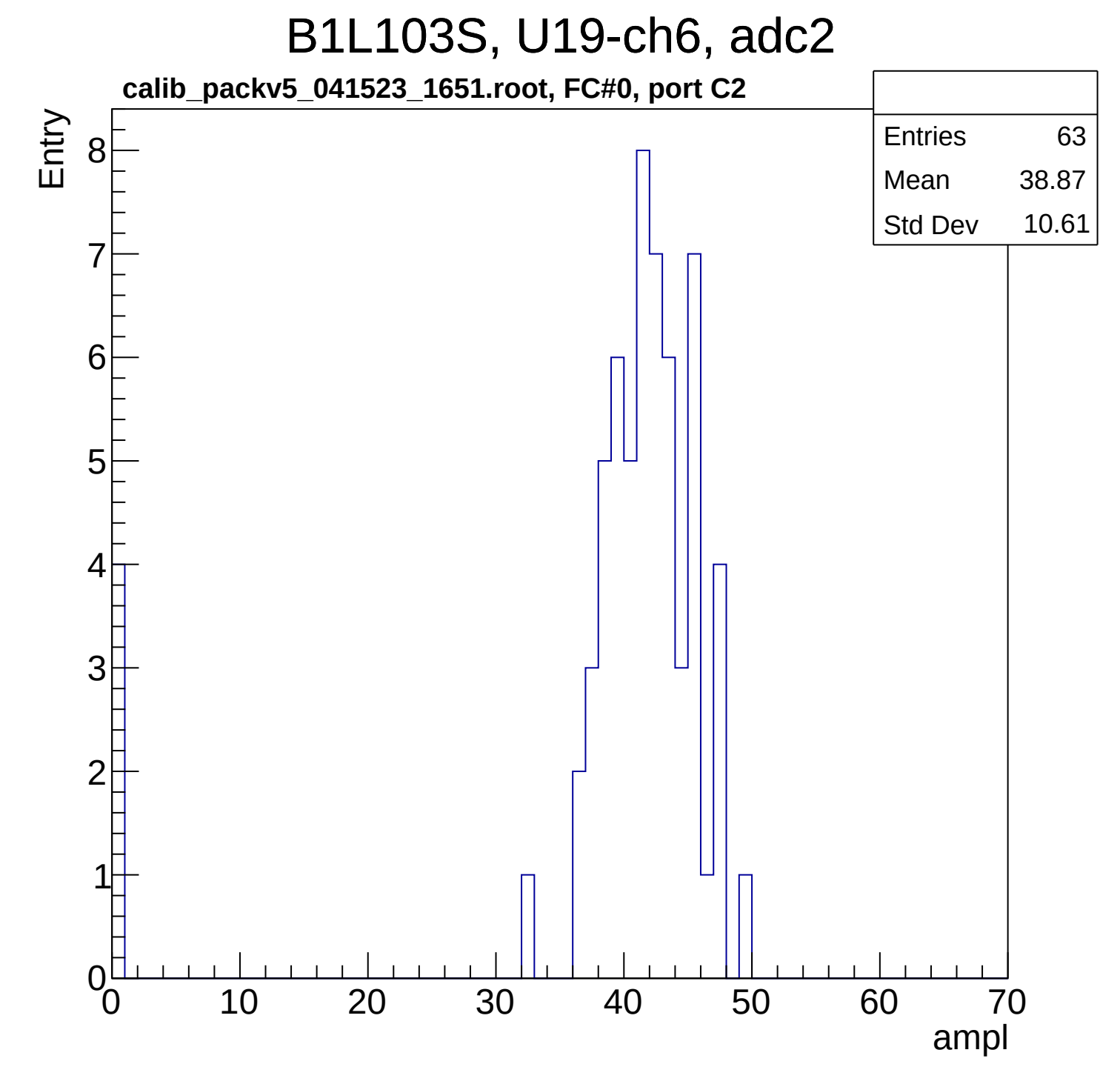

B1L103S, U19-ch5, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 57.97
Std Dev 8.202
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch5, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 61.55
Std Dev 1.437
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U19-ch5, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.316
Std Dev 14.07
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch6, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 23.99
Std Dev 10.78
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U19-ch6, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 30.19
Std Dev 13.23
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch6, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 38.87
Std Dev 10.61
Entry
ampl
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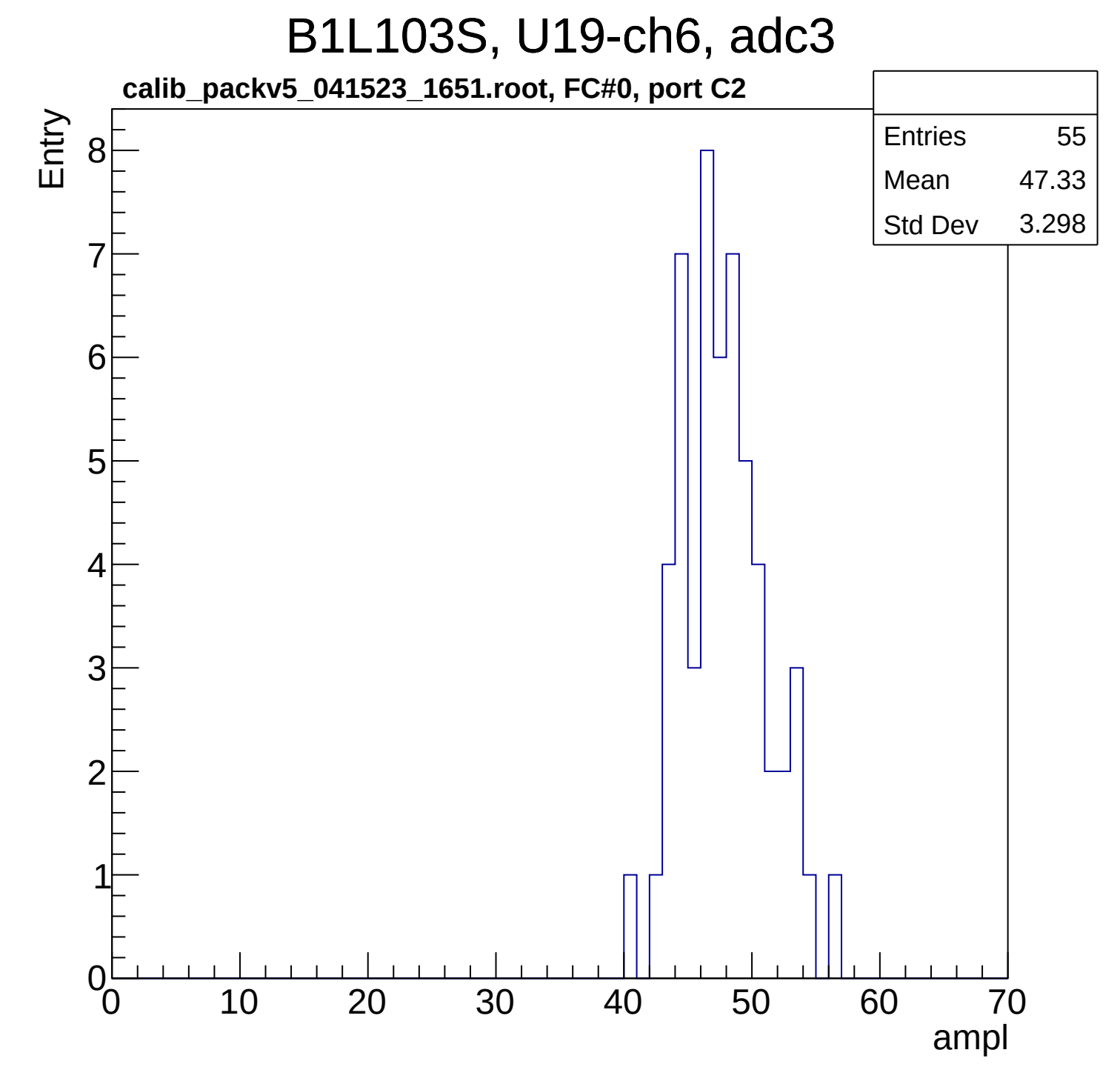
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch6, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 47.33
Std Dev 3.298
Entry
ampl
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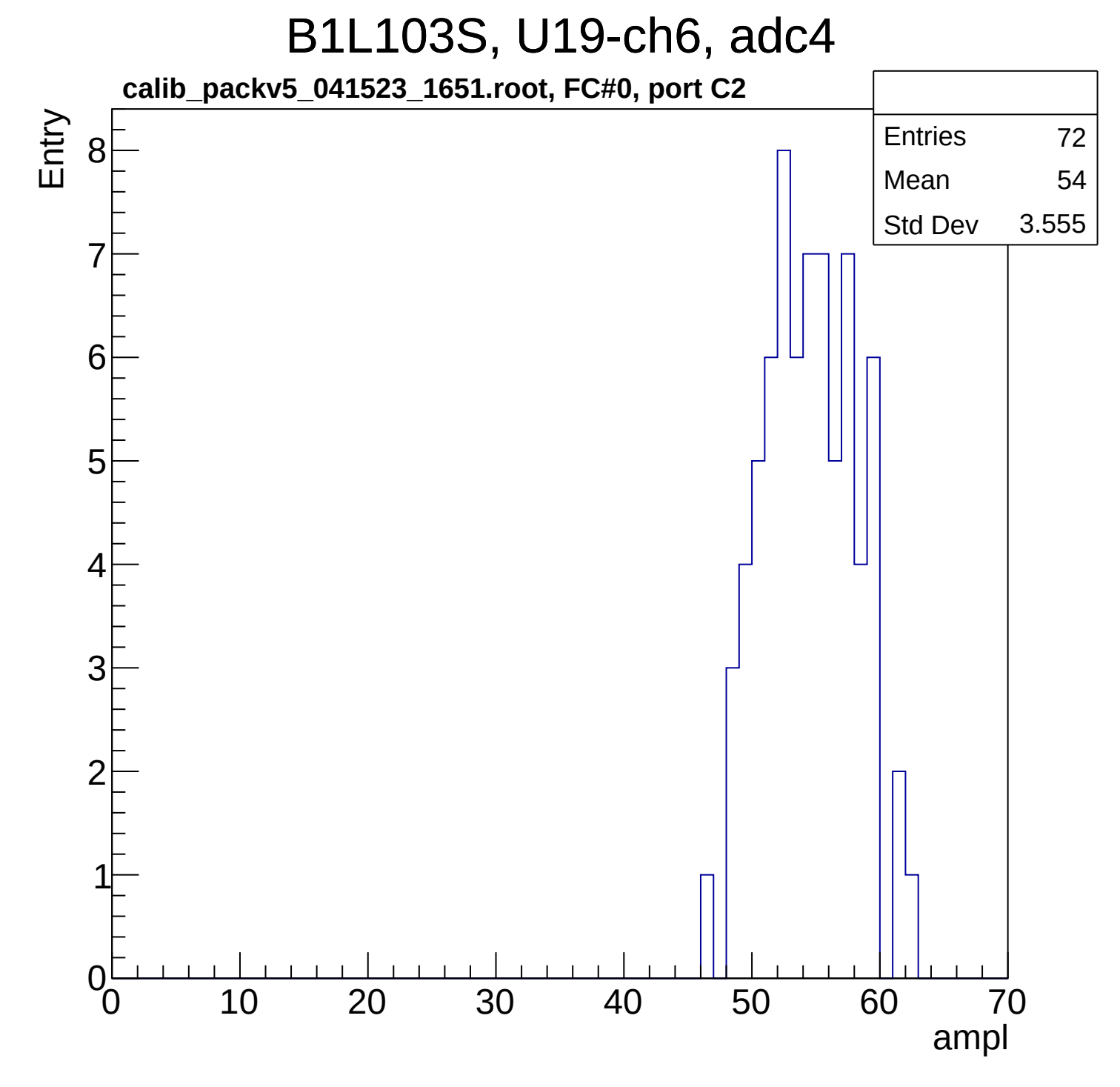
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch6, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 54
Std Dev 3.555
Entry
ampl
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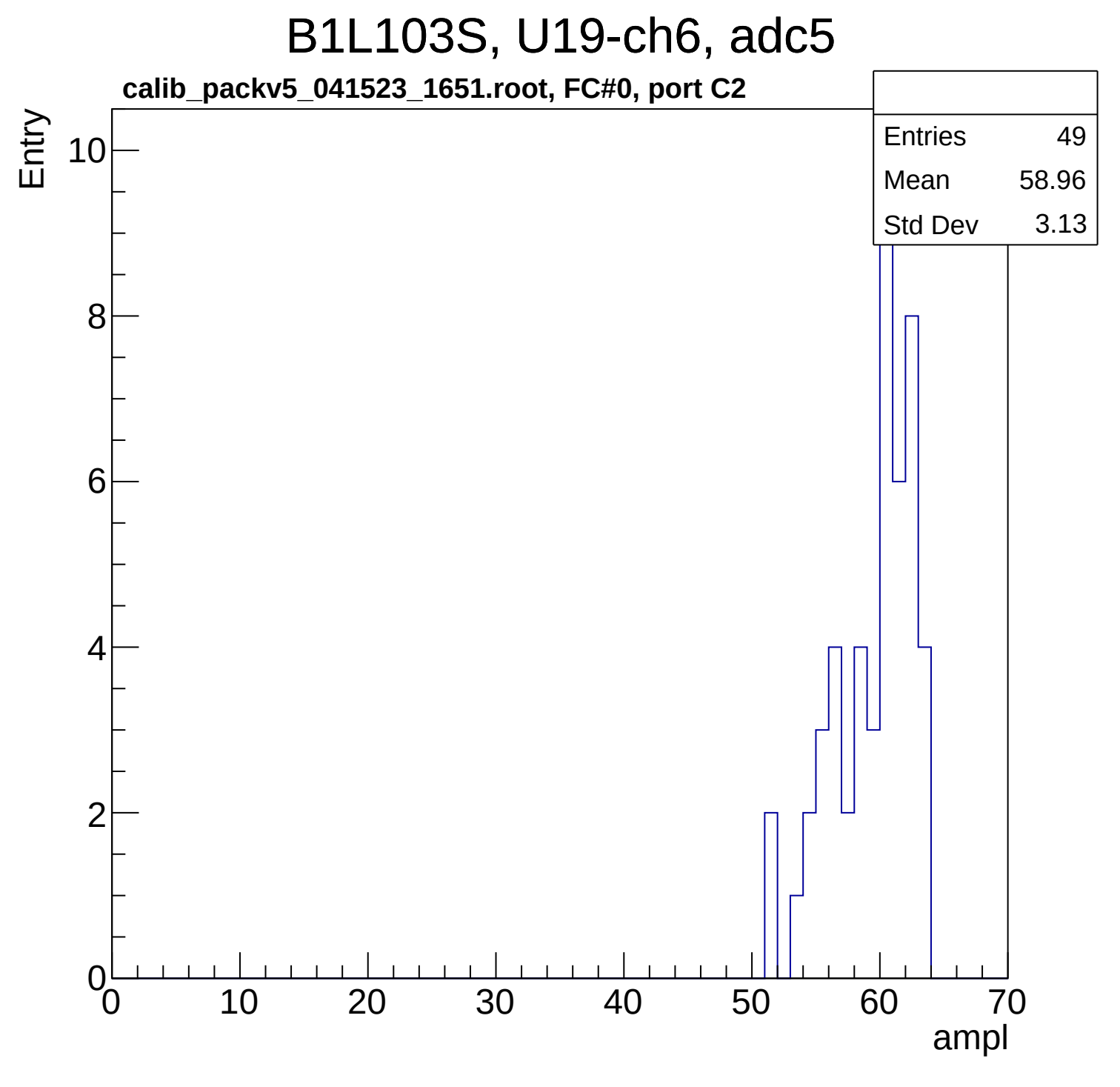
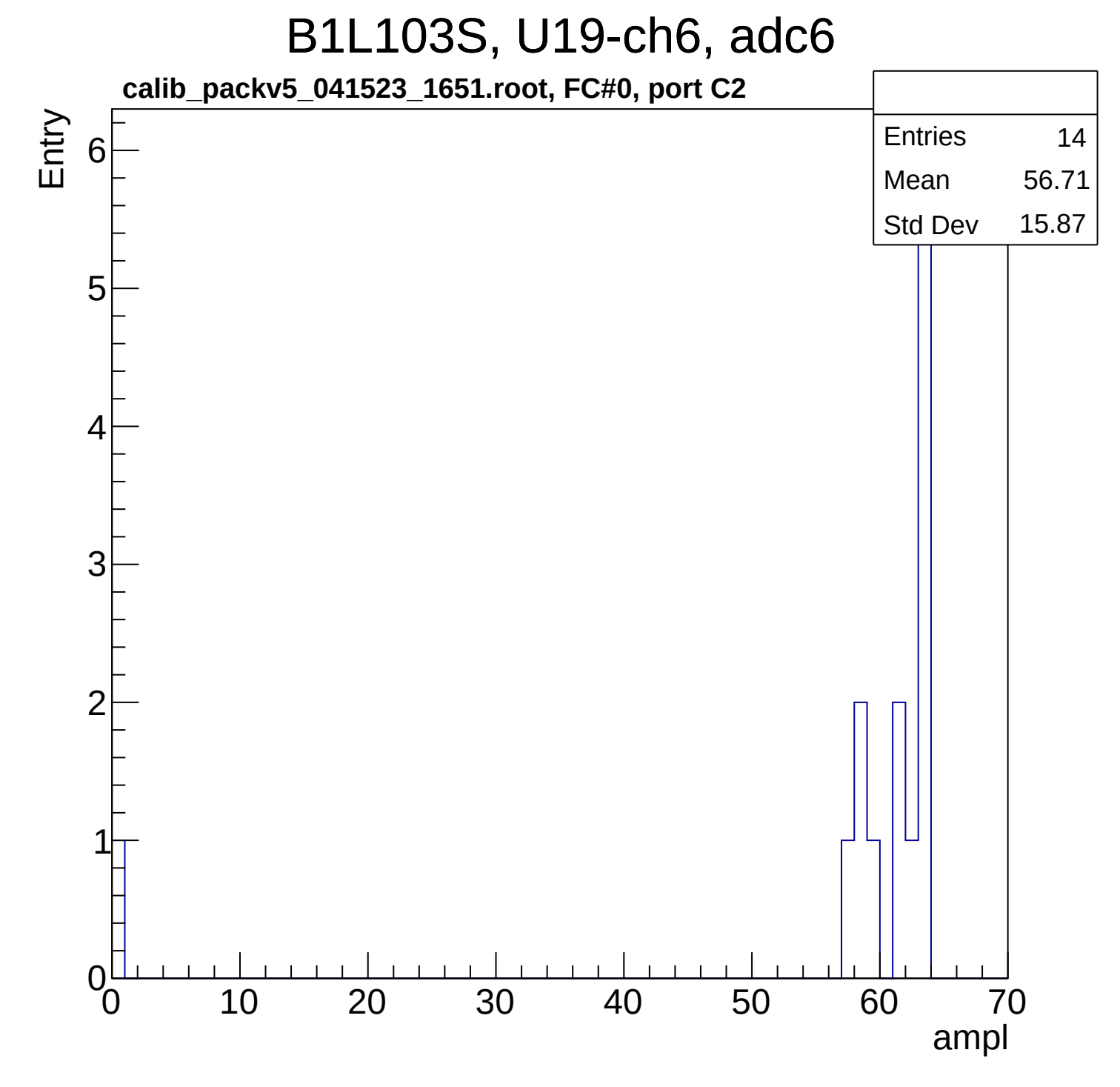
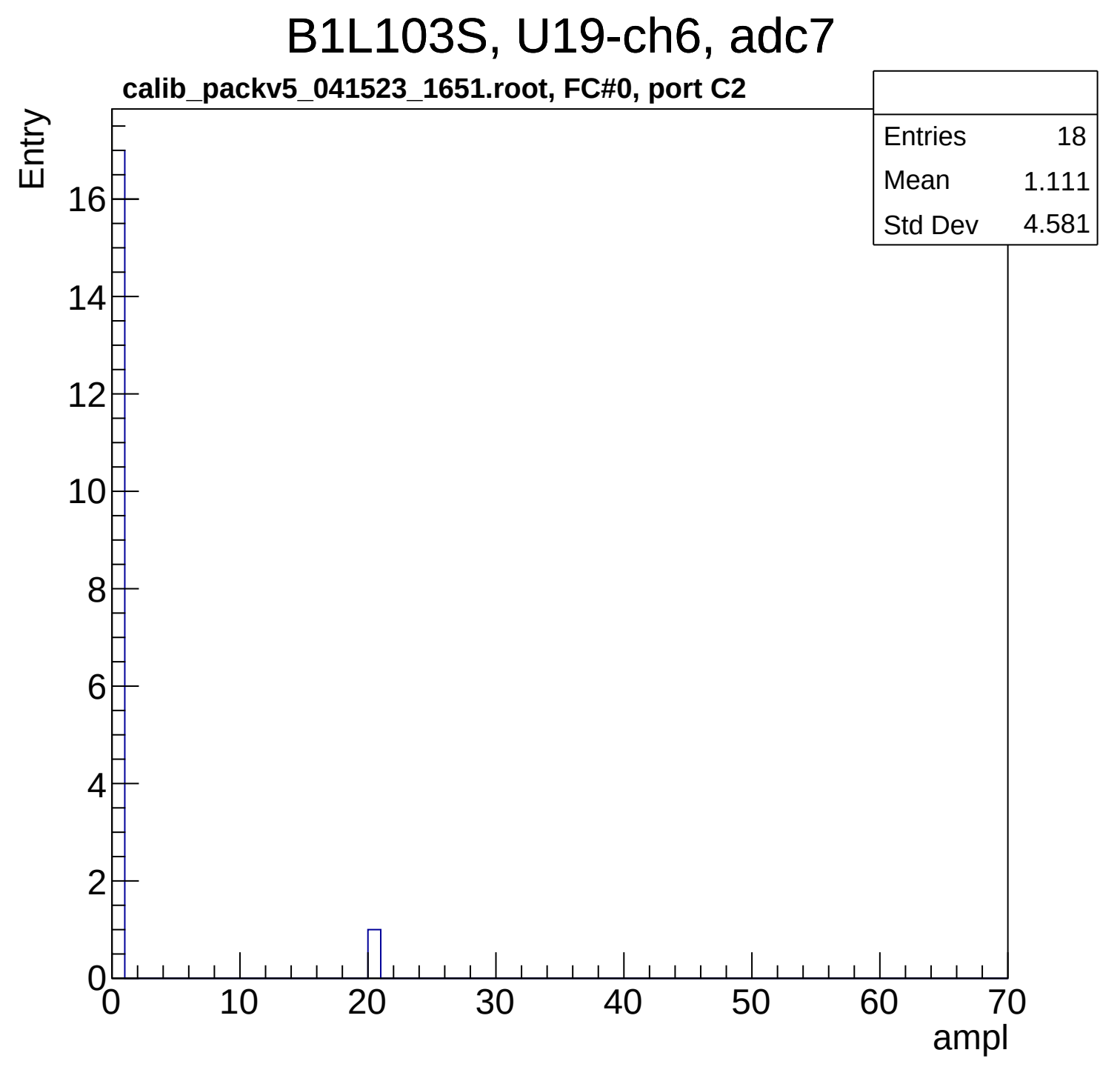
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch6, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 58.96
Std Dev 3.13
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U19-ch6, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 56.71
Std Dev 15.87
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U19-ch6, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.111
Std Dev 4.581
Entry
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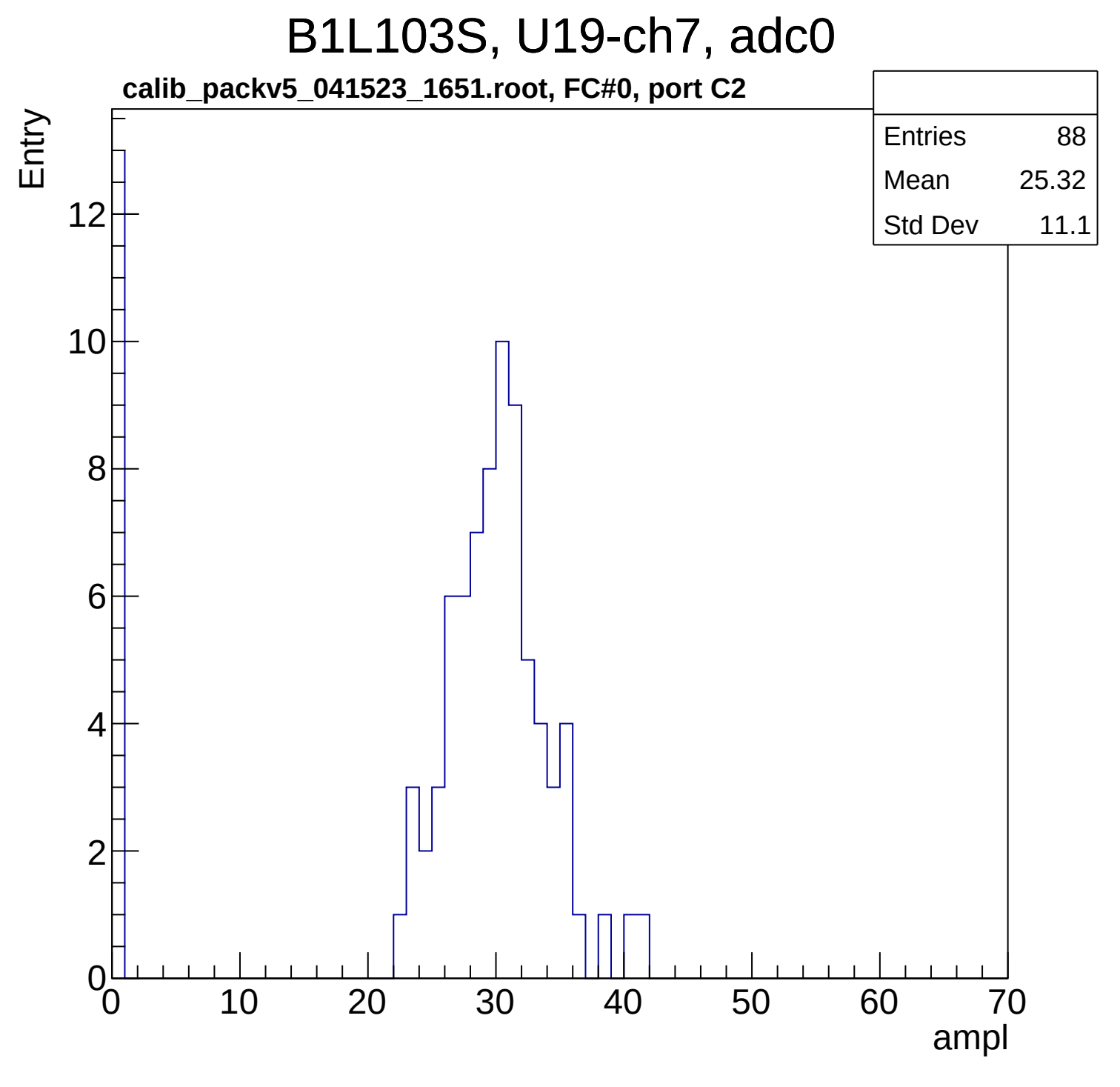
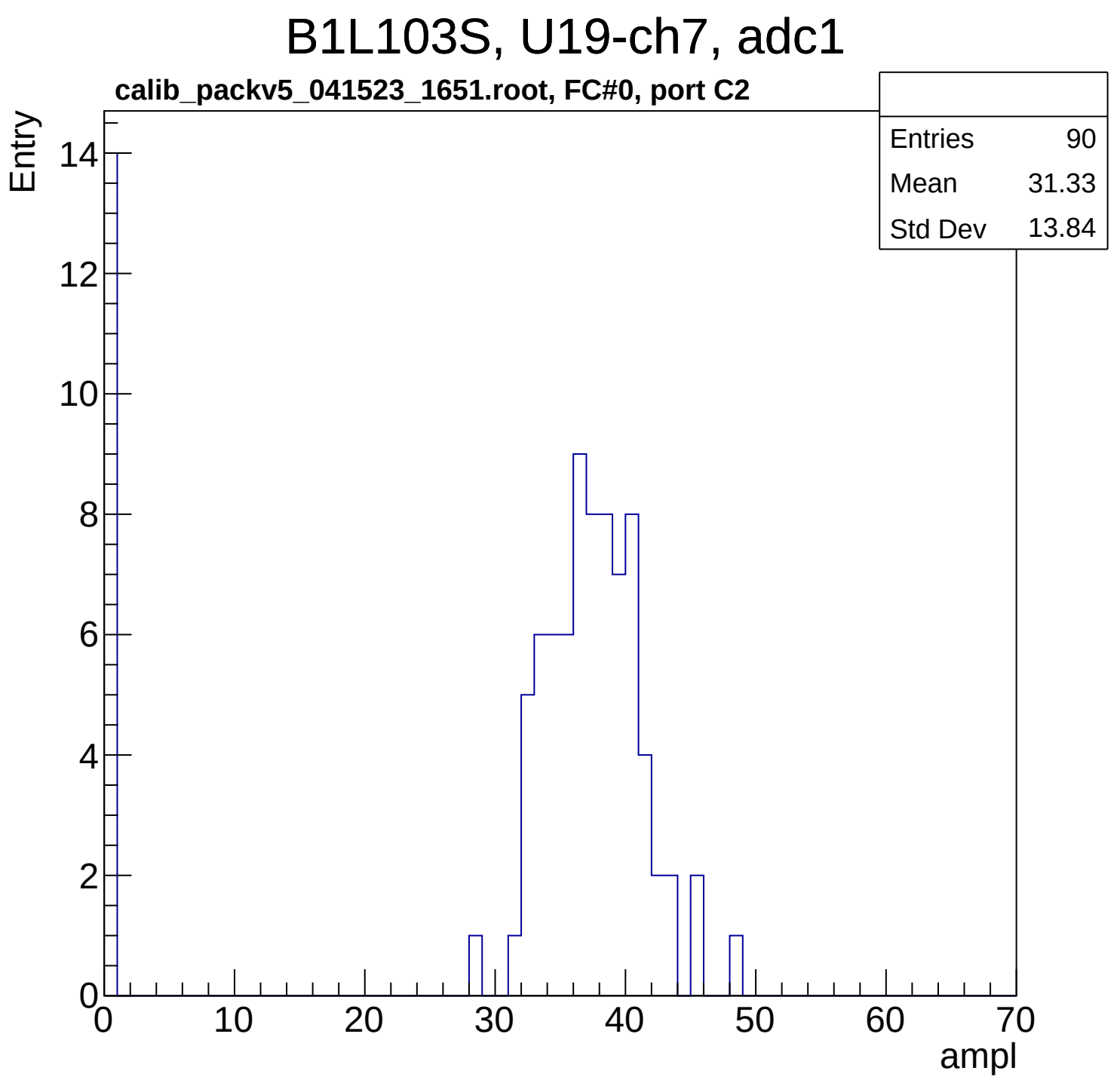
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch7, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 25.32
Std Dev 11.1
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch7, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 31.33
Std Dev 13.84
Entry
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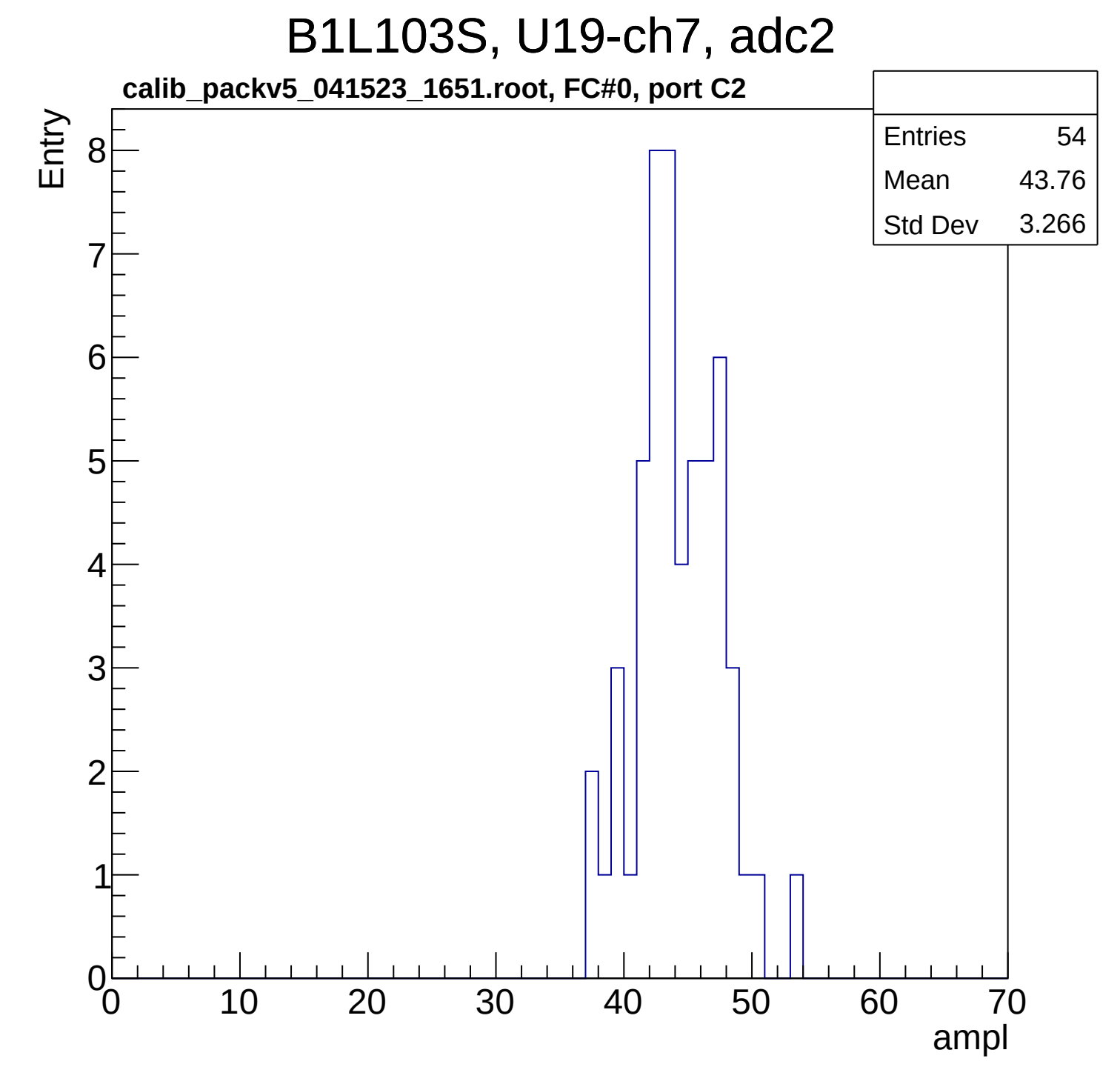
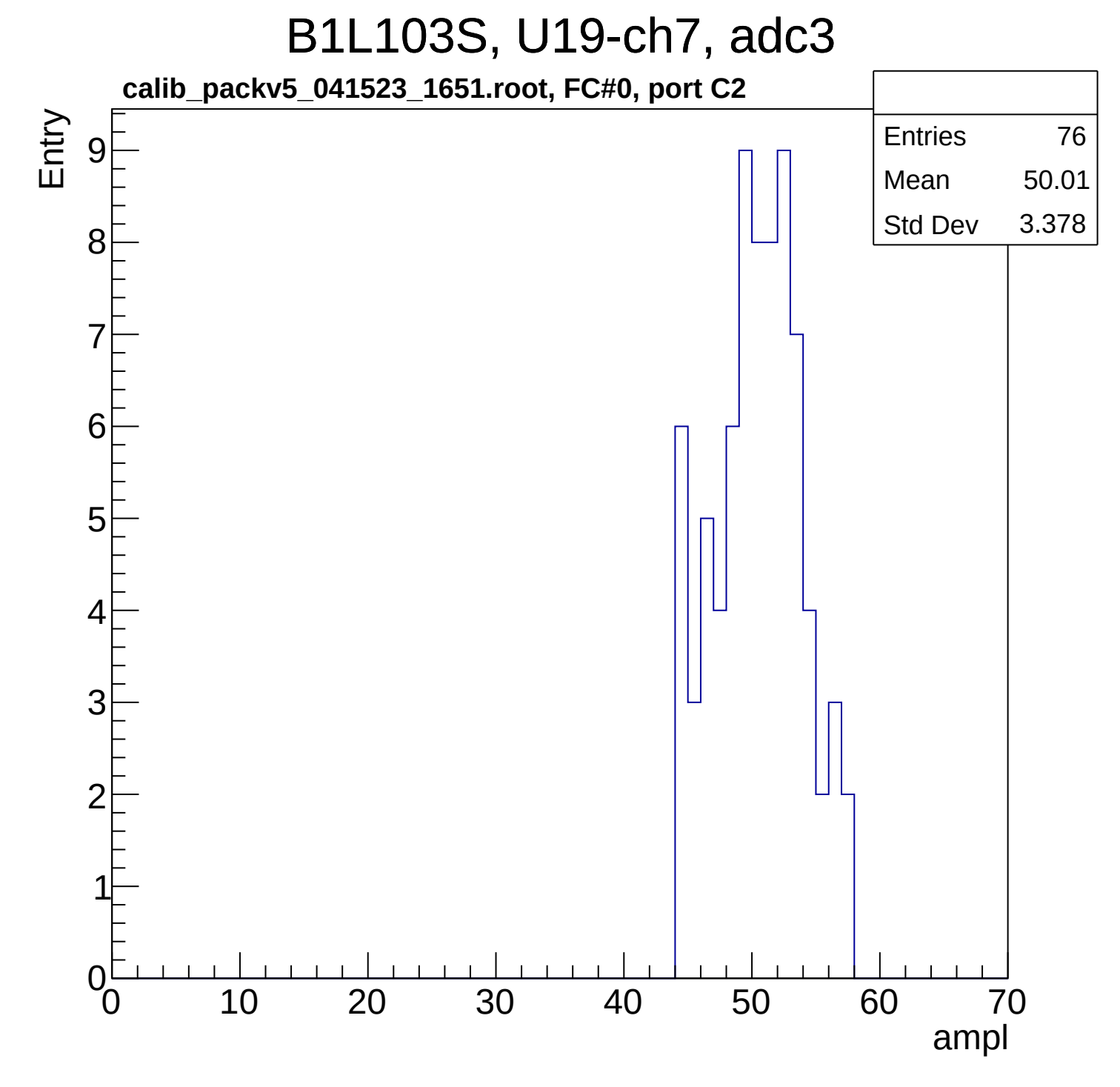
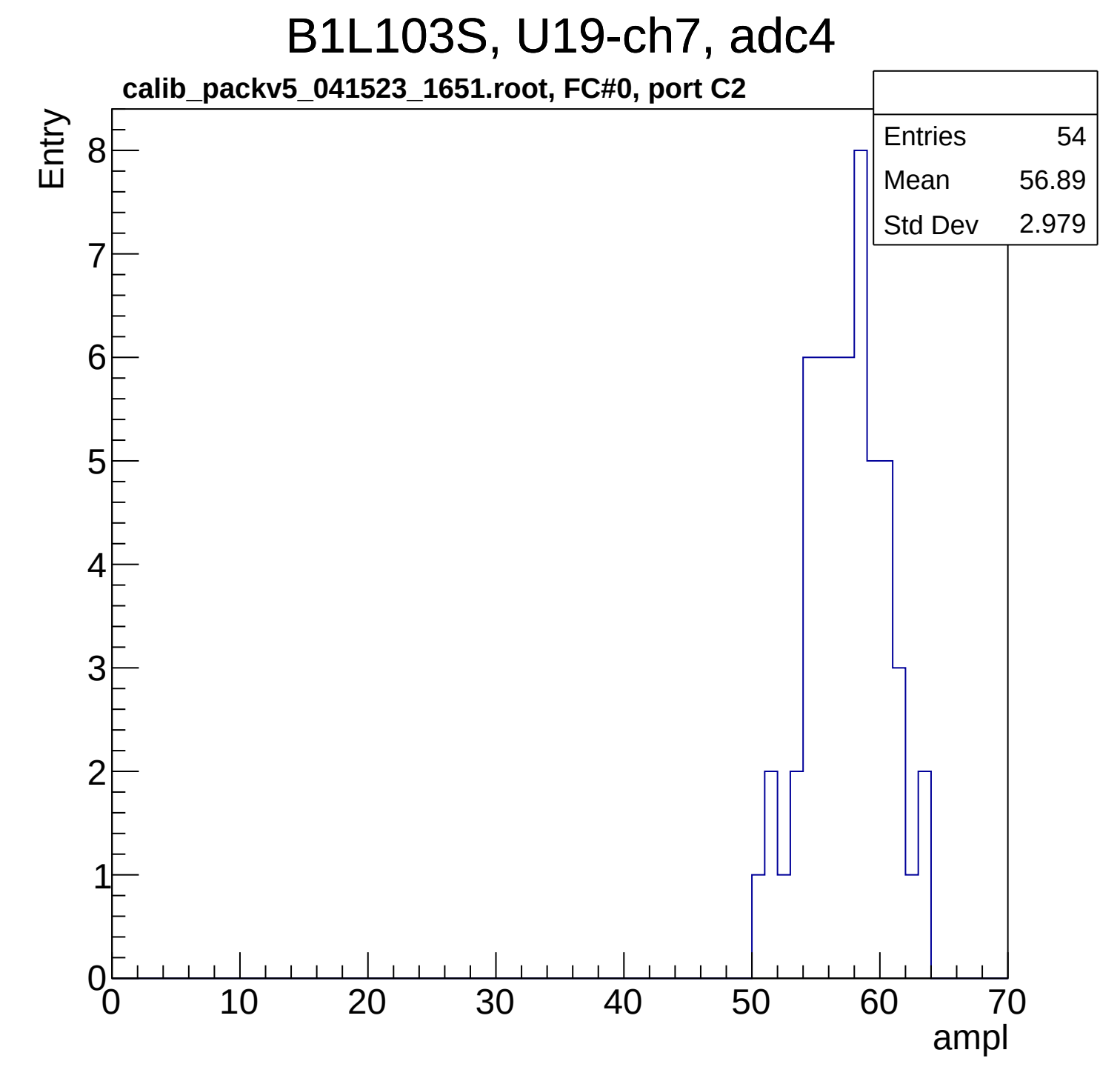
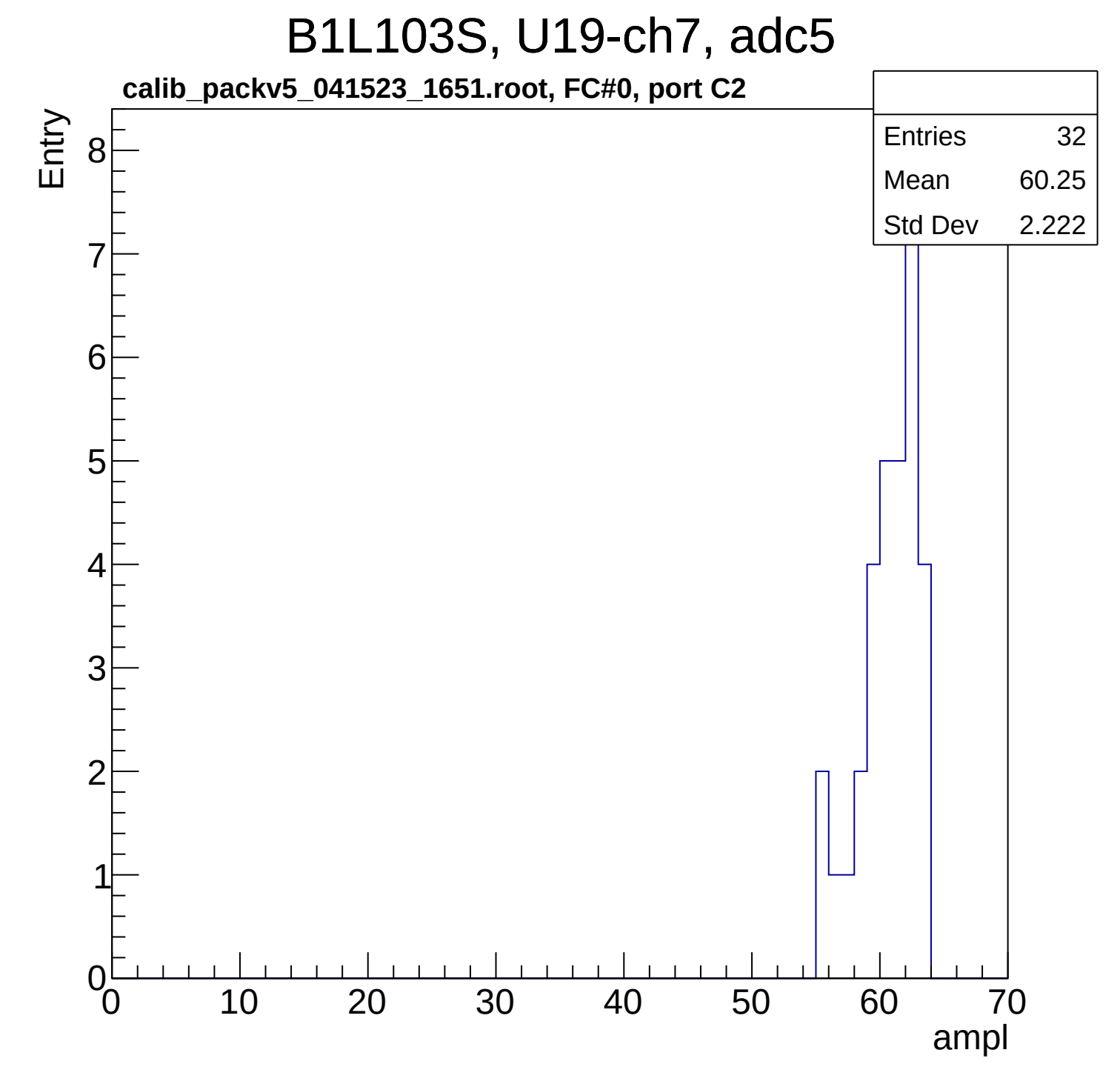
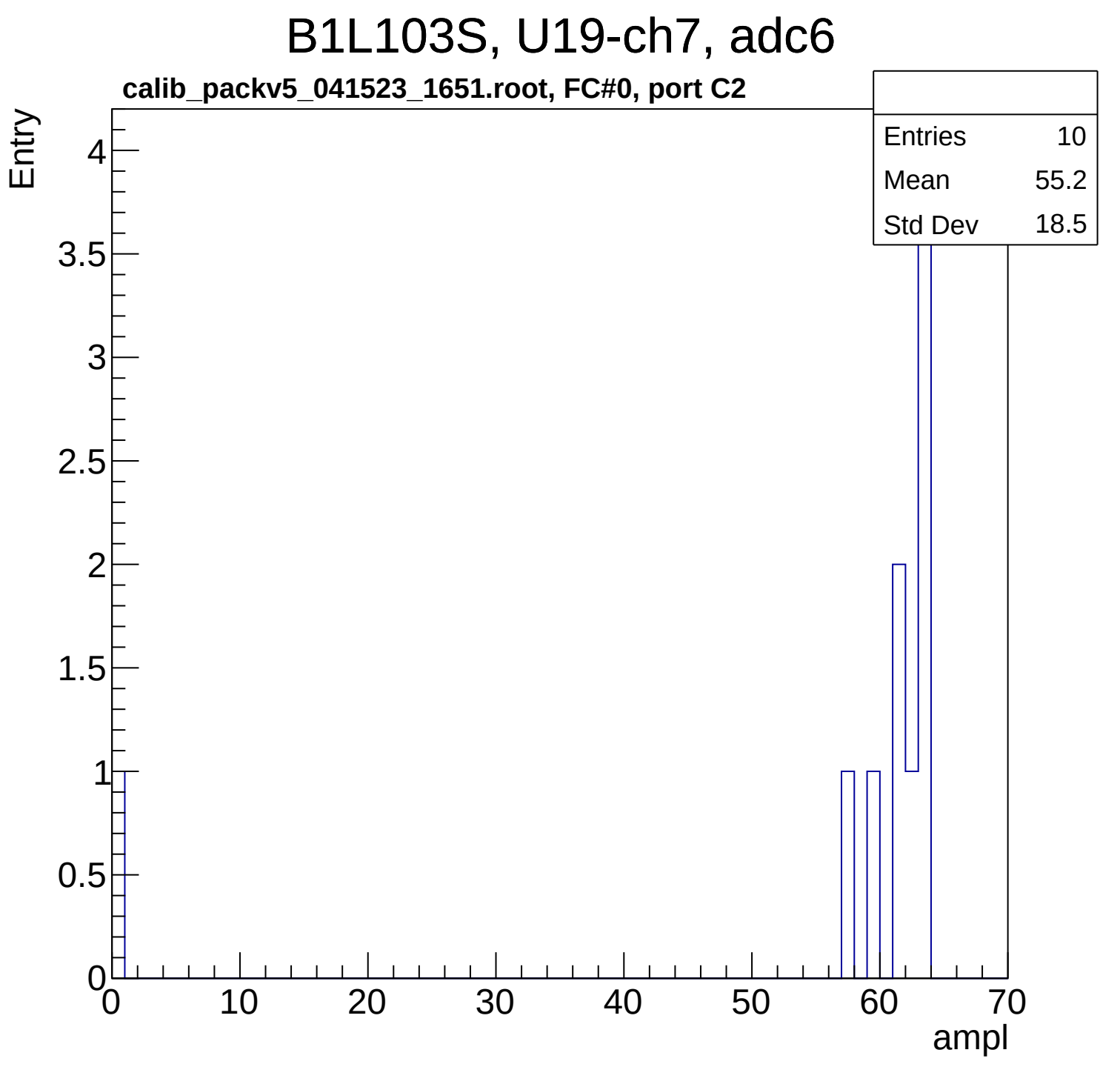
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch7, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 43.76
Std Dev 3.266
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch7, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 50.01
Std Dev 3.378
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch7, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 56.89
Std Dev 2.979
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch7, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 60.25
Std Dev 2.222
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch7, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 55.2
Std Dev 18.5
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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40
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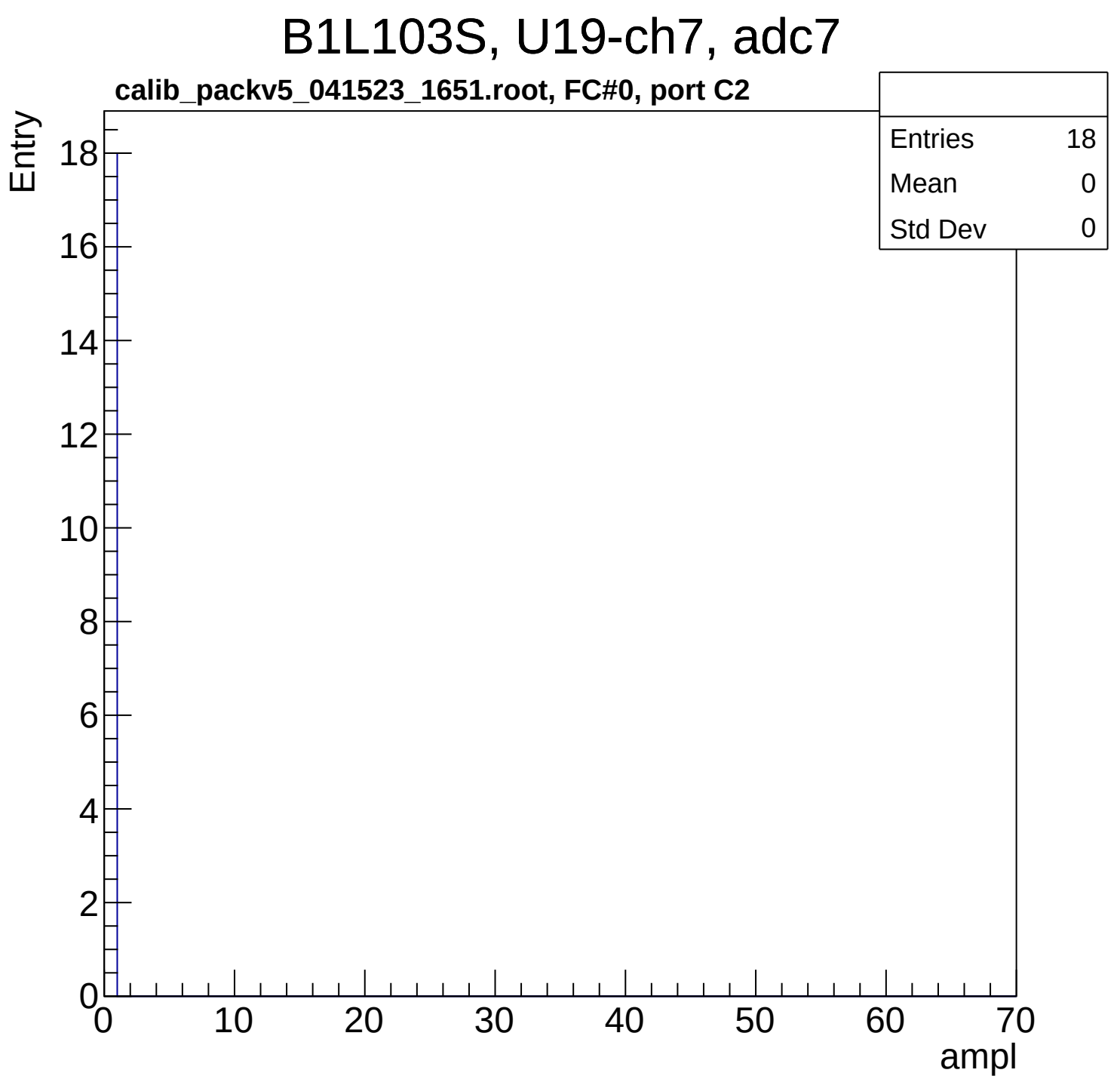
60
70


B1L103S, U19-ch7, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
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4
6
8
10
12
14
16
18
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10
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40
50
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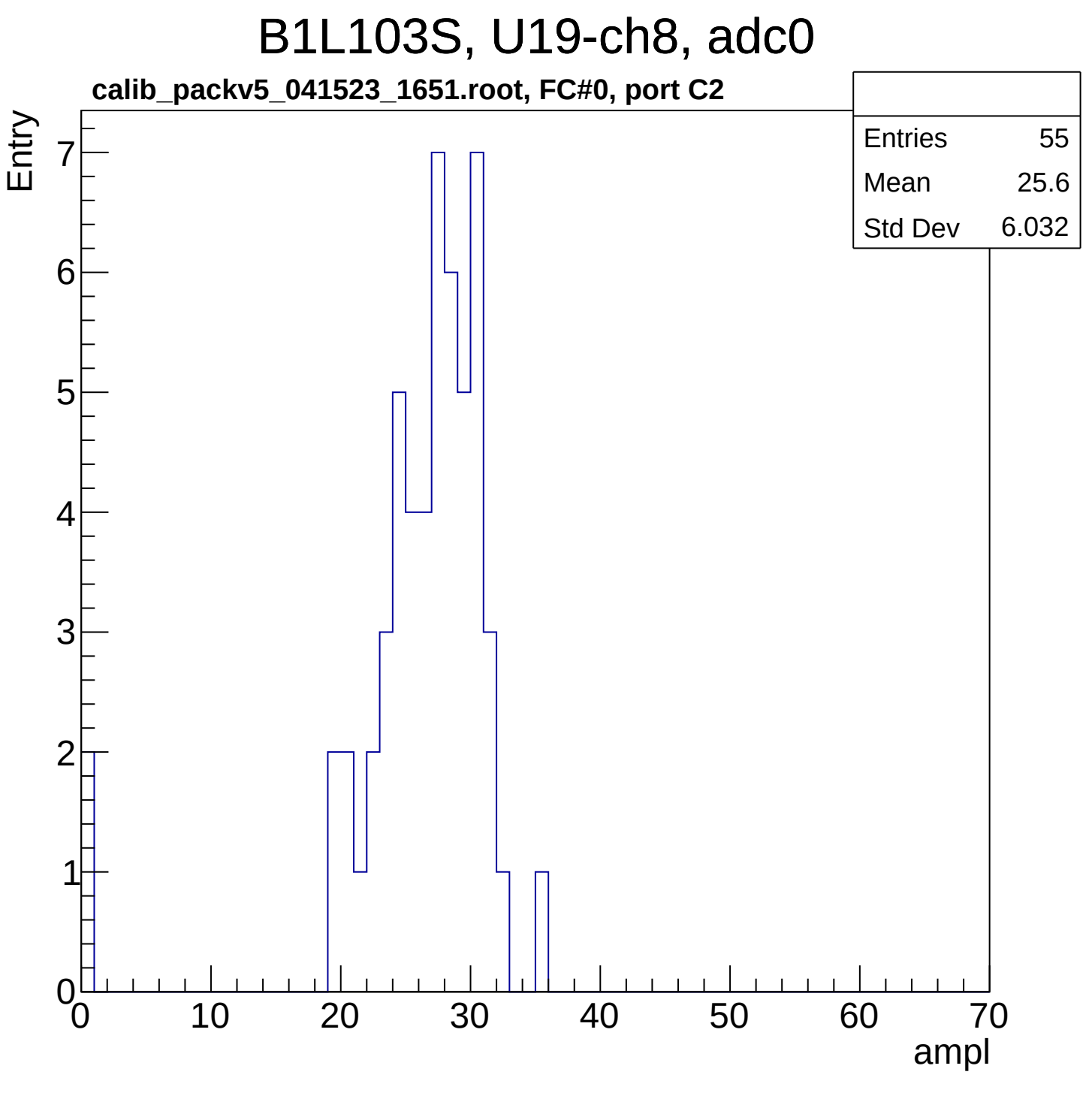
70
ampl


B1L103S, U19-ch8, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 25.6
Std Dev 6.032
Entry
ampl
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1
2
3
4
5
6
7
0
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60
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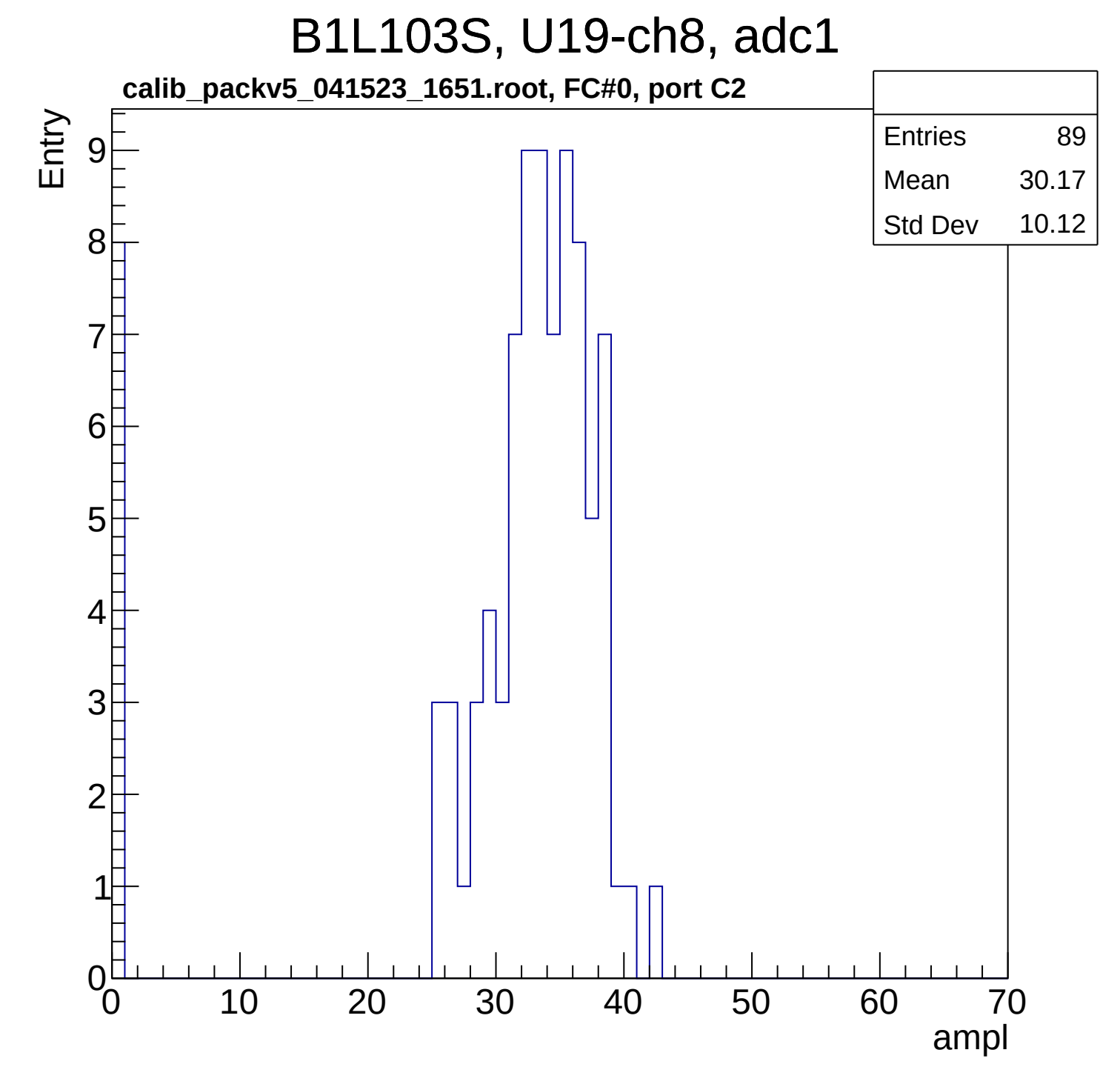
B1L103S, U19-ch8, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 30.17
Std Dev 10.12
Entry
ampl
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2
3
4
5
6
7
8
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0
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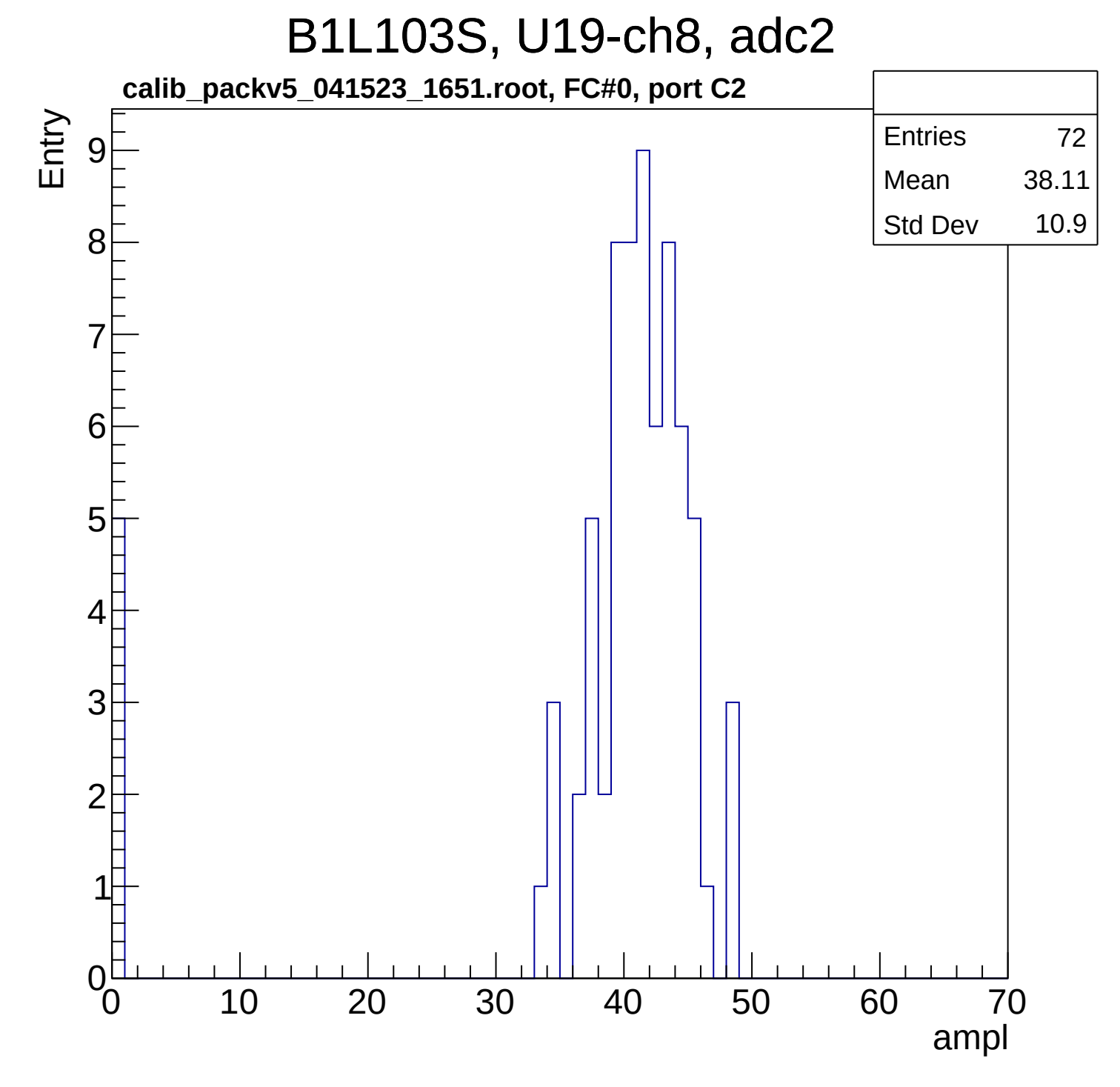
B1L103S, U19-ch8, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 38.11
Std Dev 10.9
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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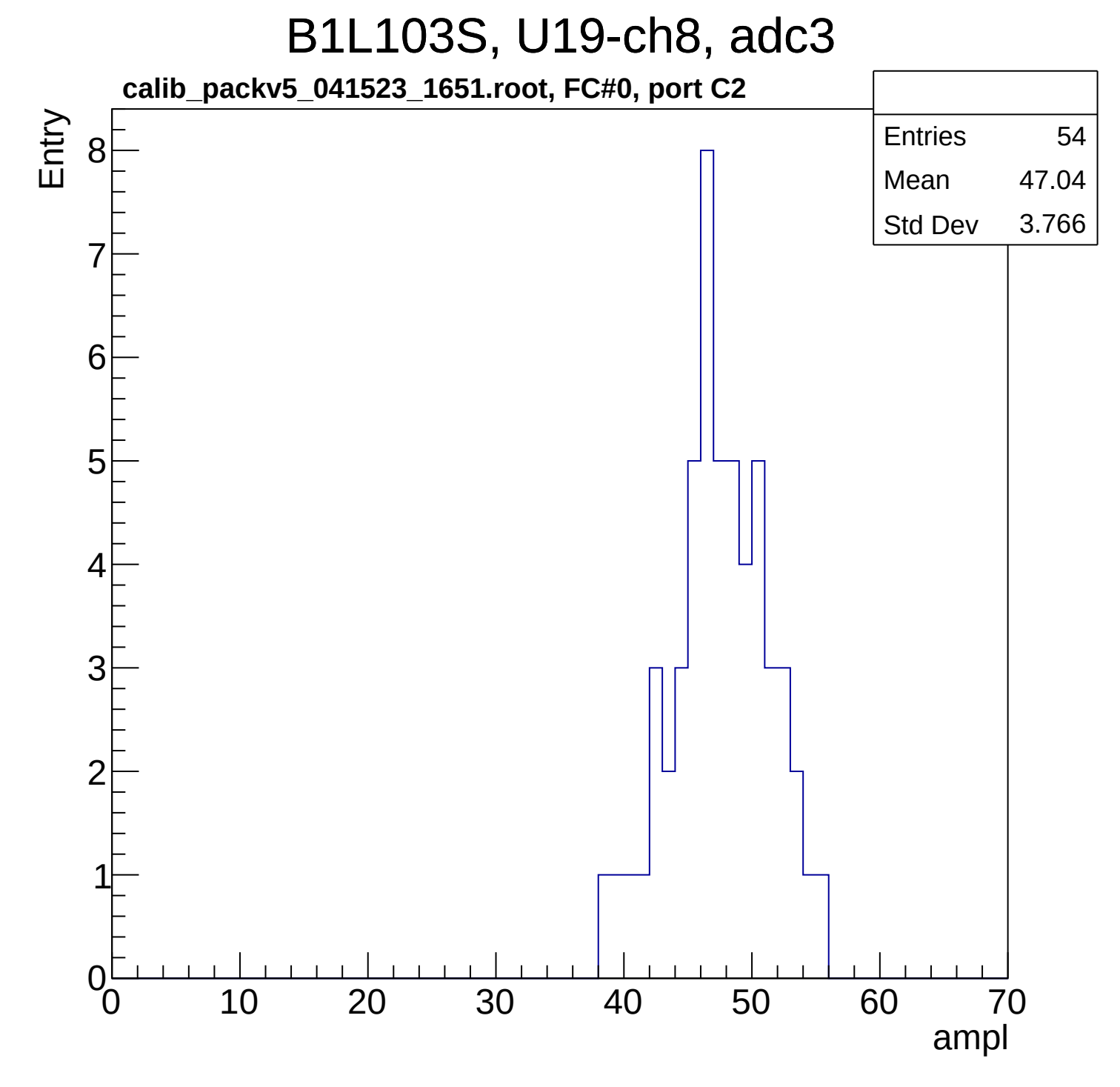
B1L103S, U19-ch8, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 47.04
Std Dev 3.766
Entry
ampl
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1
2
3
4
5
6
7
8
0
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60
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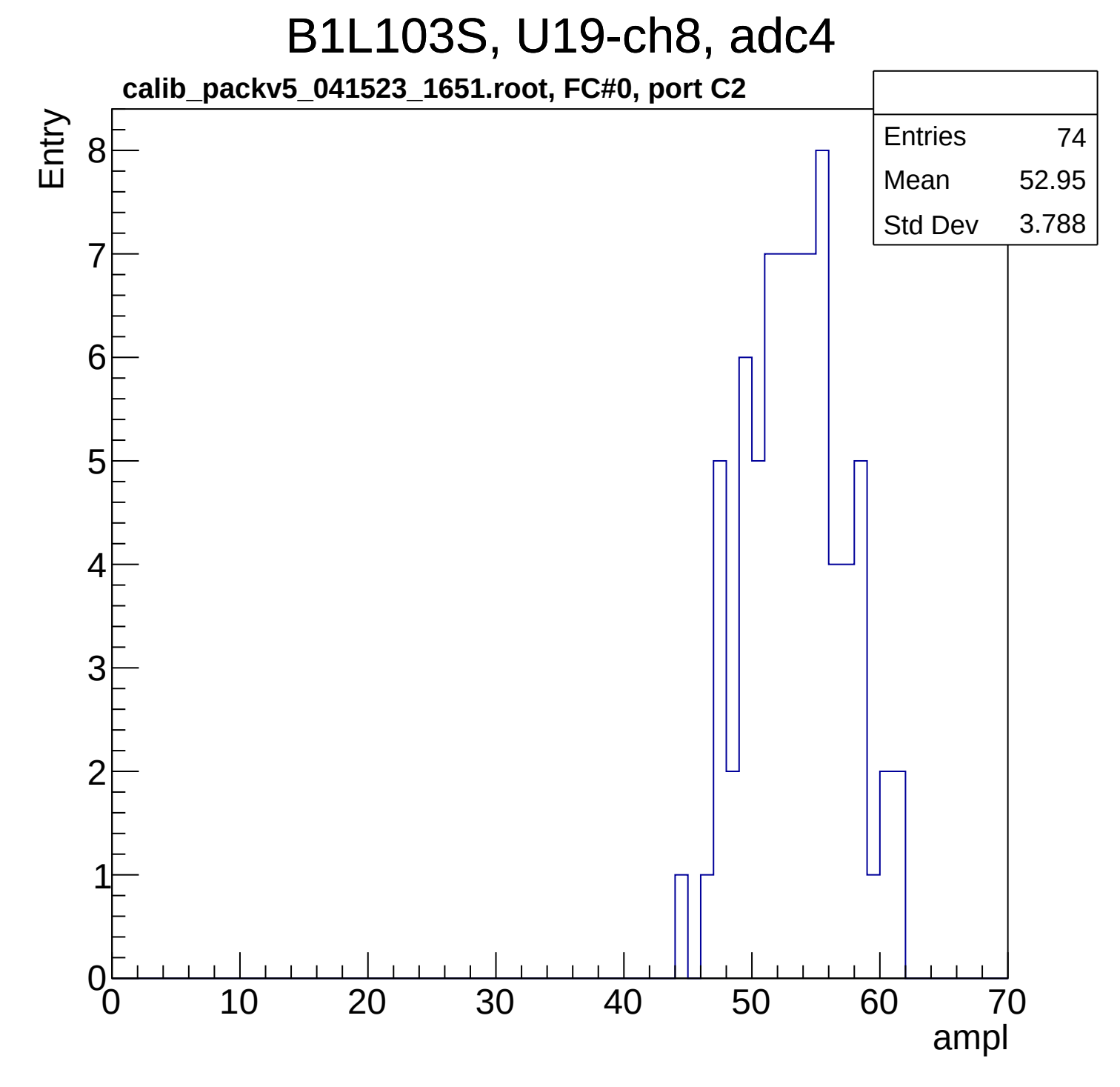
B1L103S, U19-ch8, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 52.95
Std Dev 3.788
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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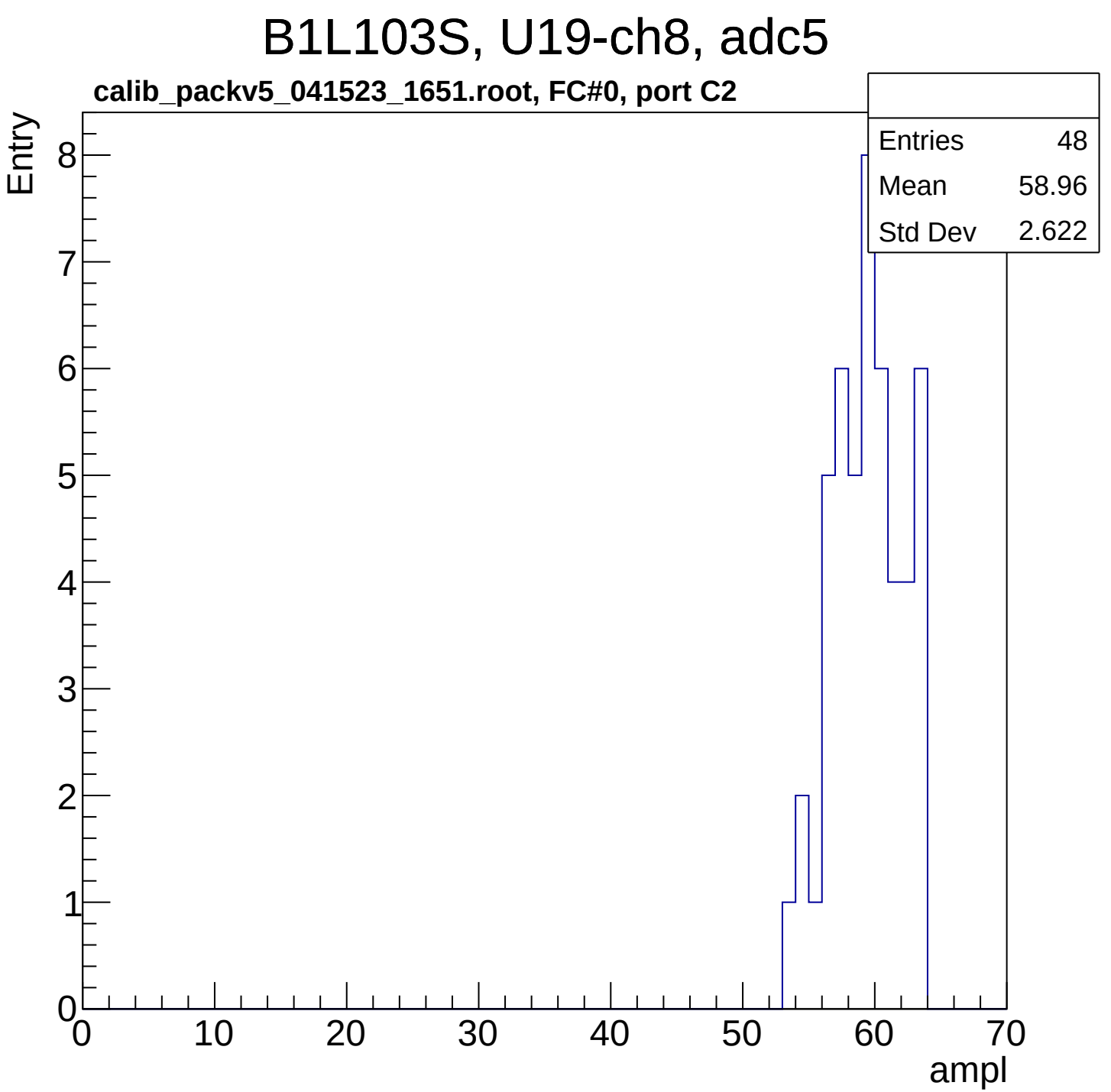
B1L103S, U19-ch8, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 58.96
Std Dev 2.622
Entry
ampl
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2
3
4
5
6
7
8
0
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40
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60
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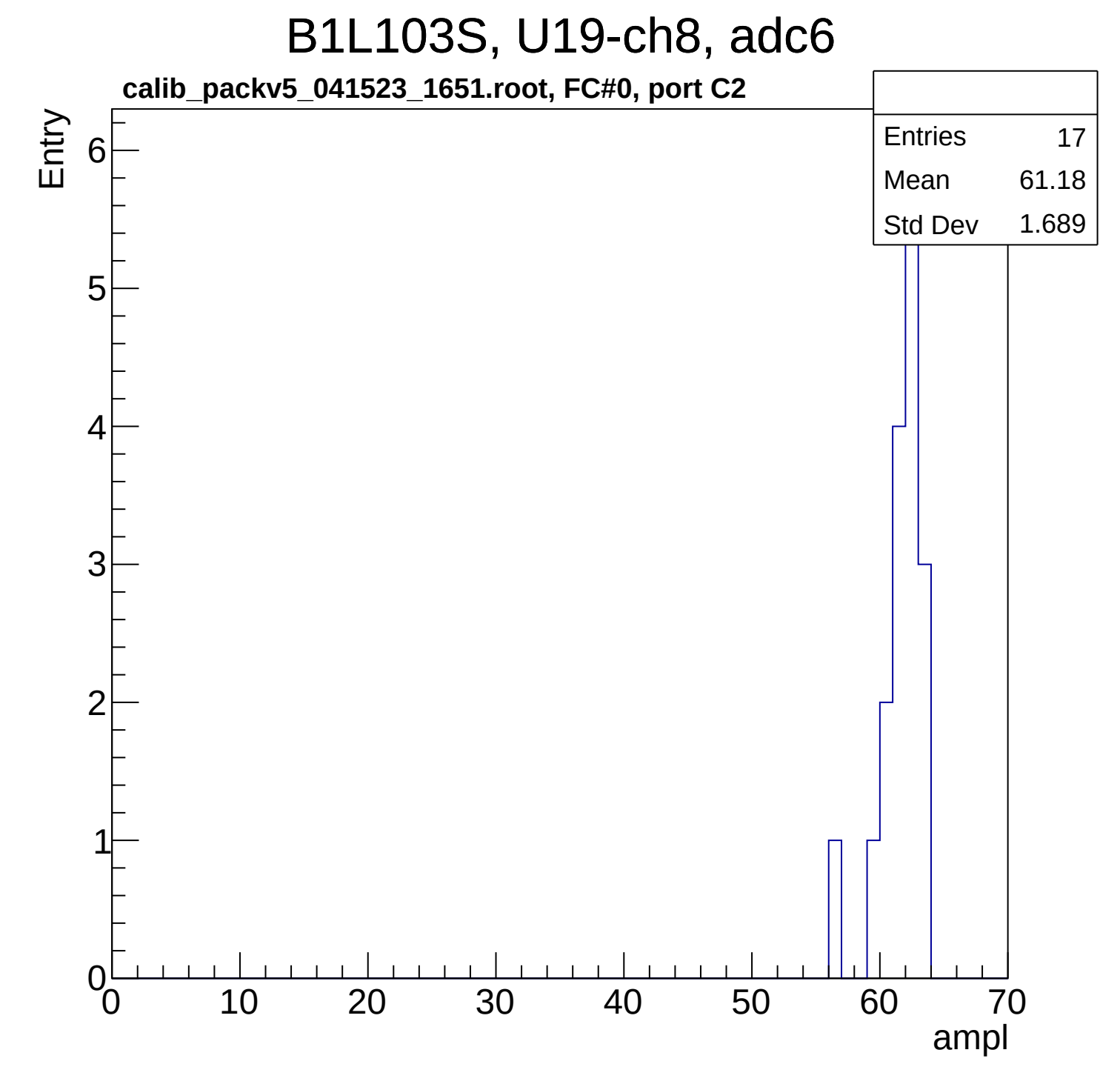
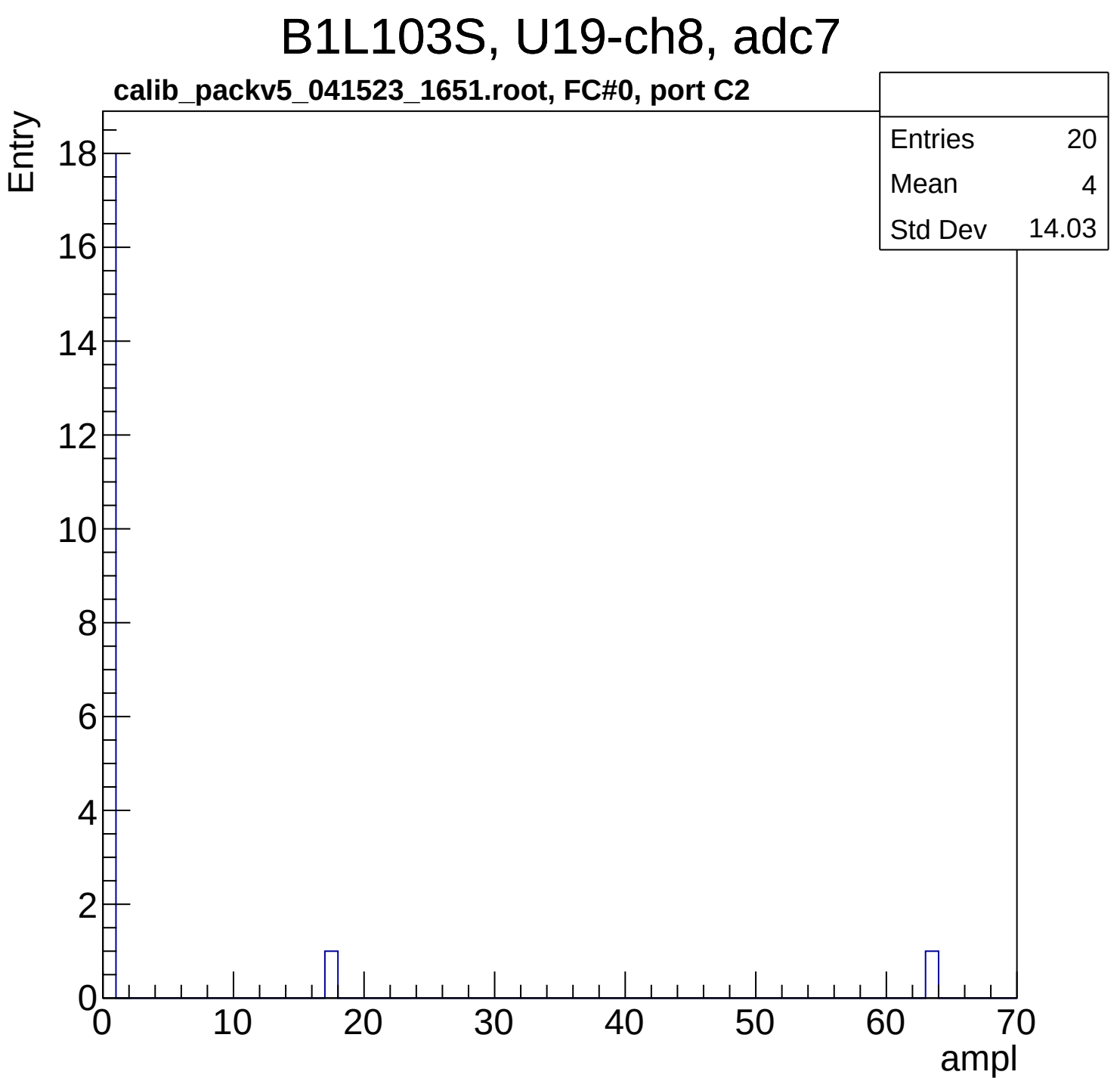
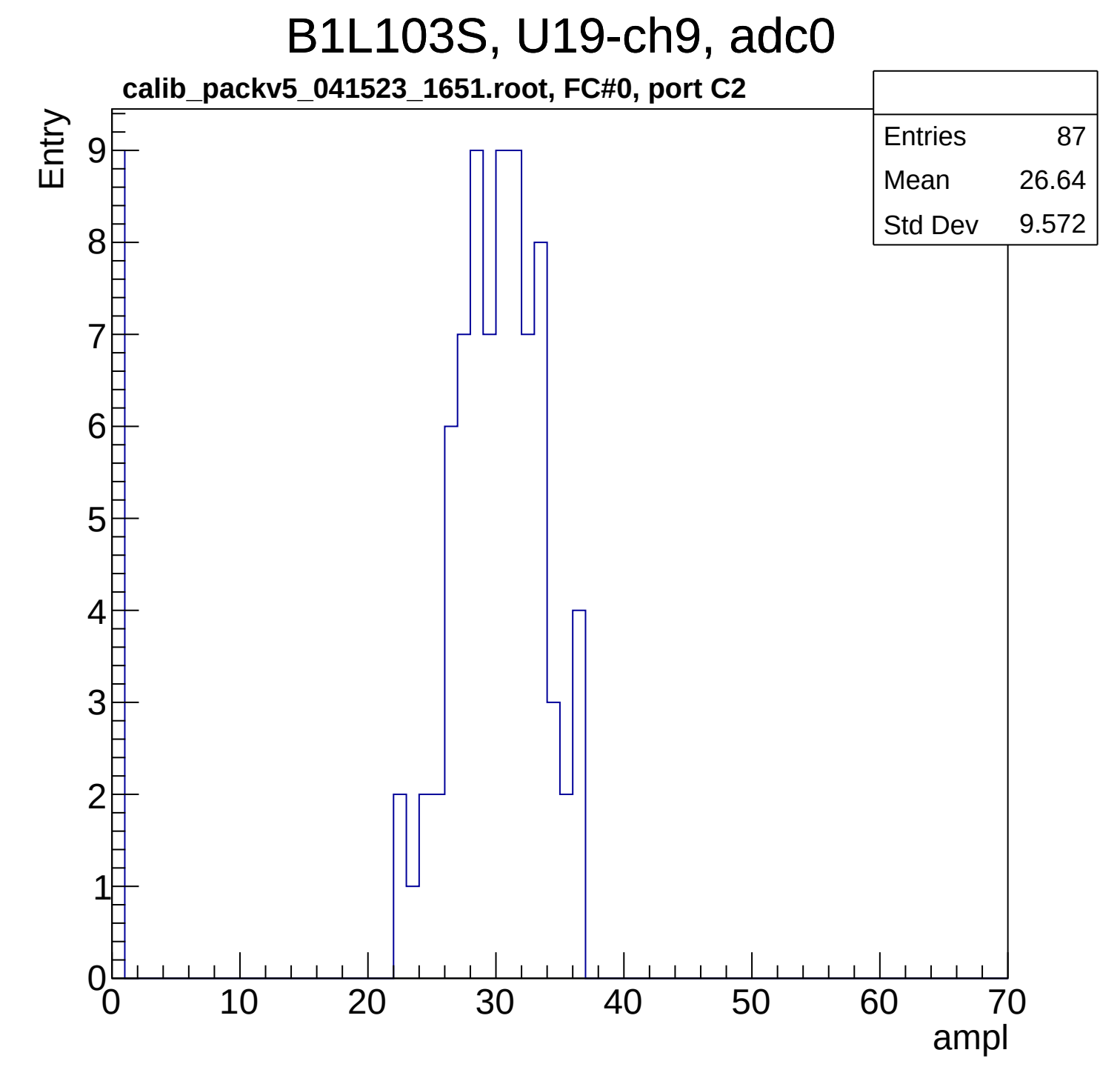

B1L103S, U19-ch8, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 61.18
Std Dev 1.689
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U19-ch8, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4
Std Dev 14.03
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch9, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 26.64
Std Dev 9.572
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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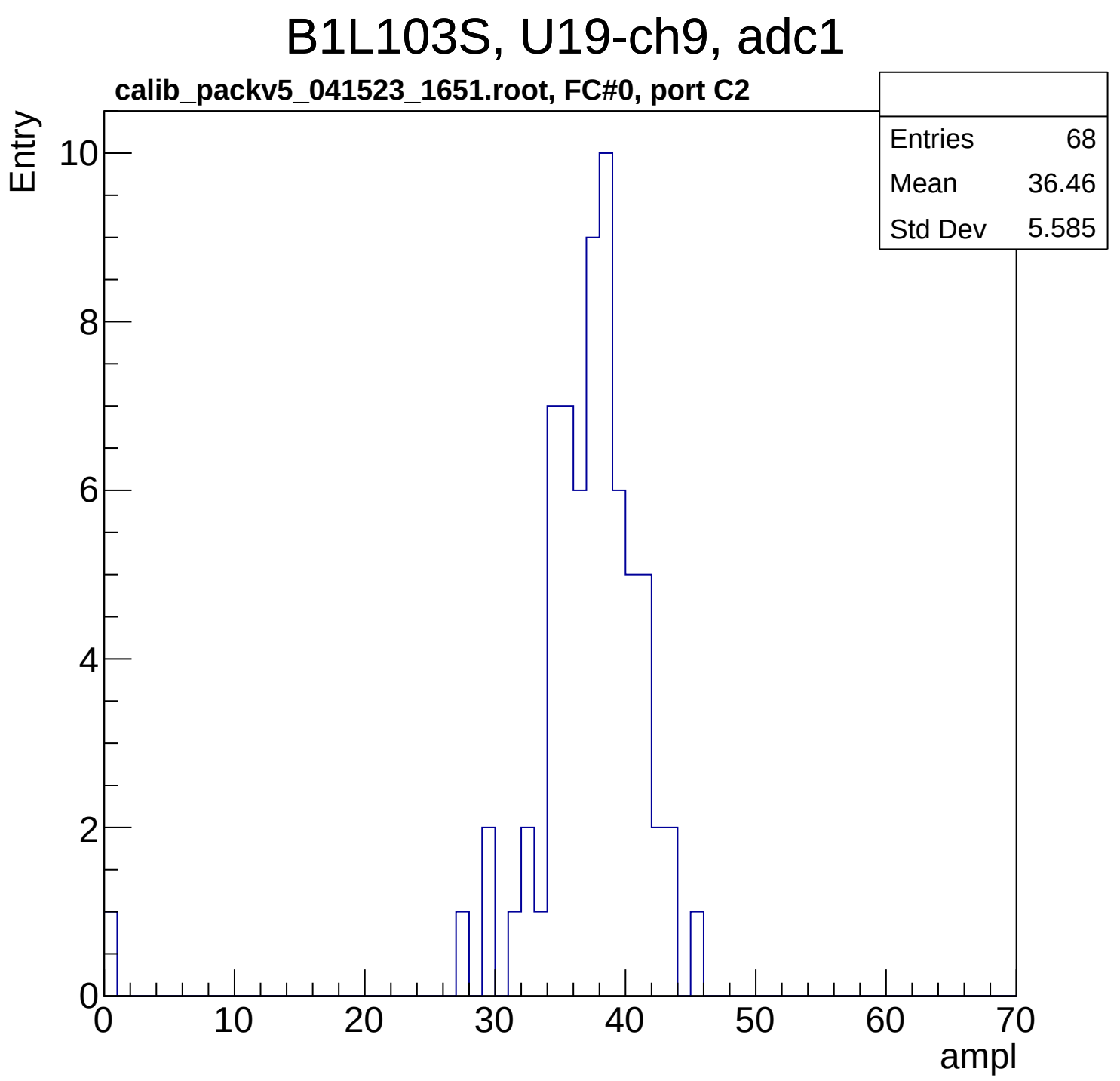
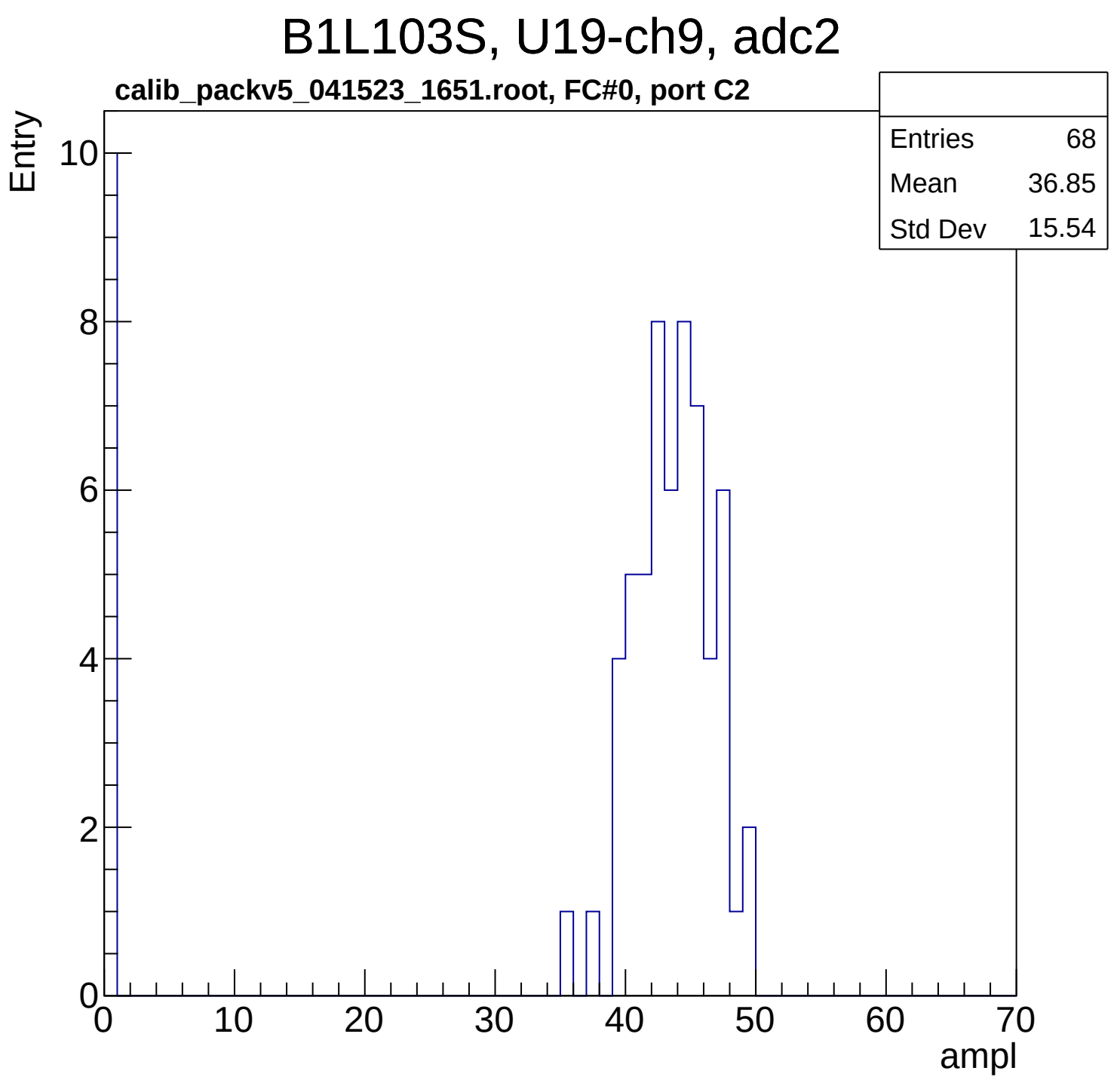
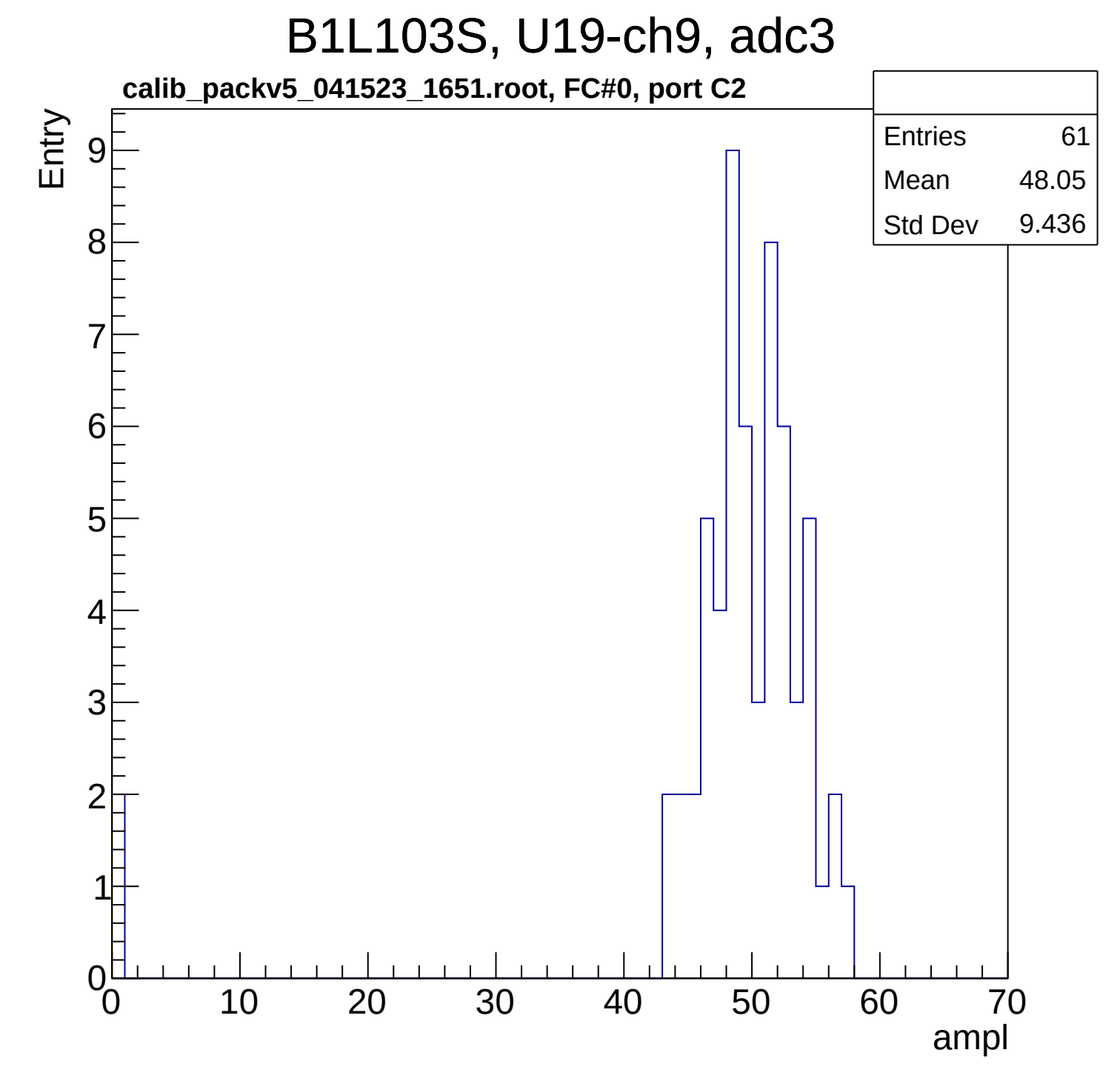

B1L103S, U19-ch9, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 36.46
Std Dev 5.585
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U19-ch9, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 36.85
Std Dev 15.54
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch9, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 48.05
Std Dev 9.436
Entry
ampl
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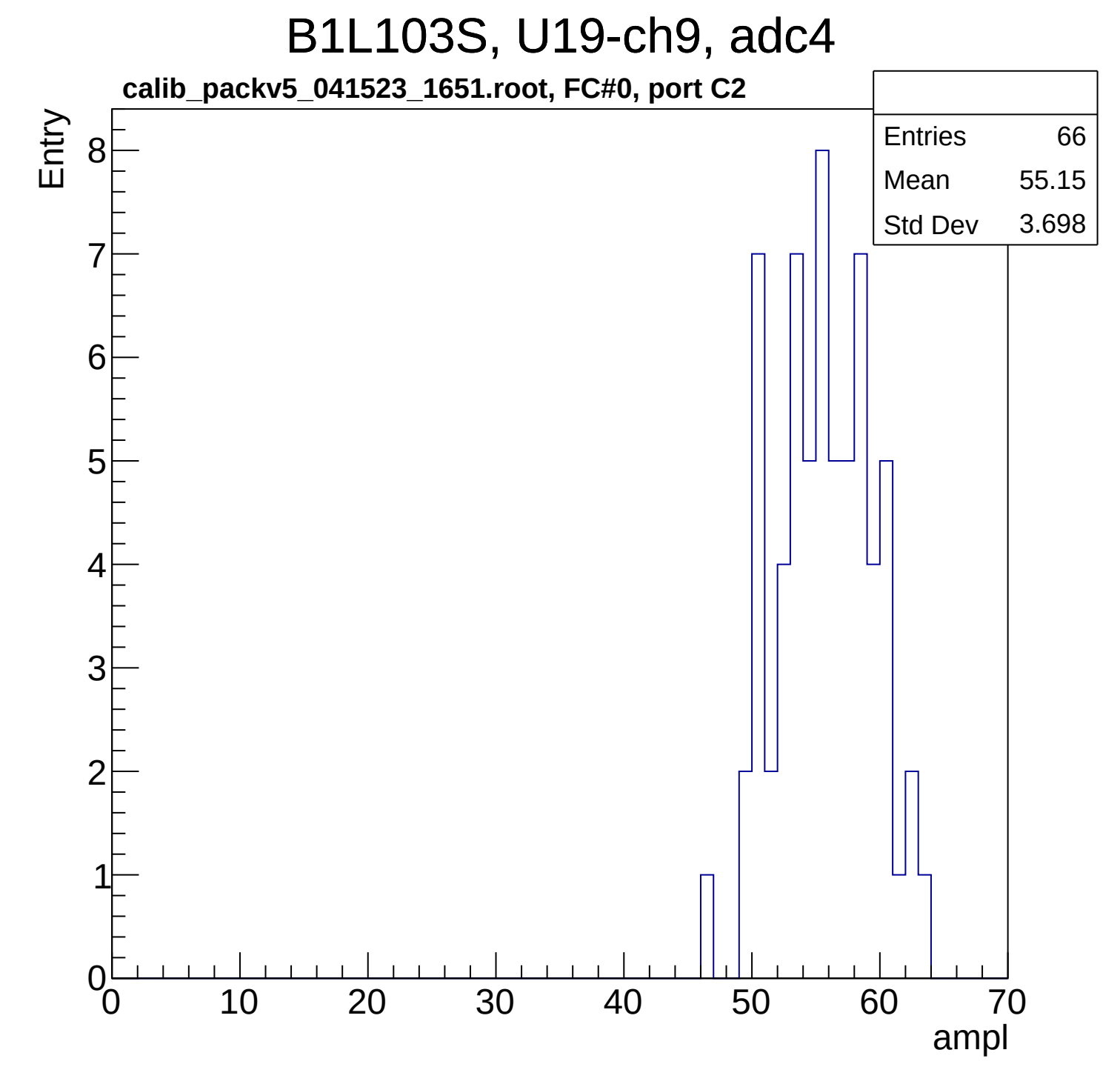
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch9, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 55.15
Std Dev 3.698
Entry
ampl
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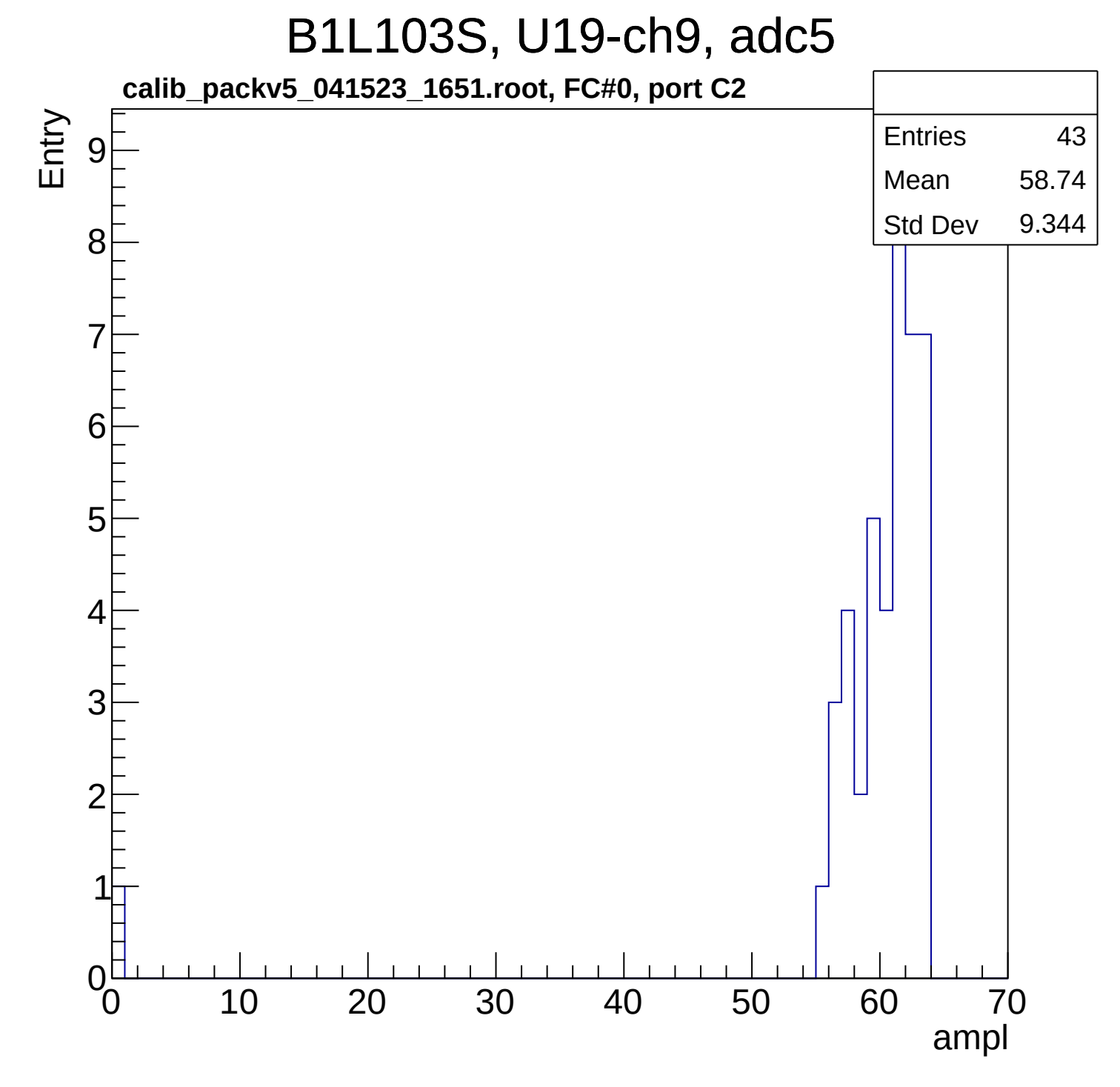
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch9, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 58.74
Std Dev 9.344
Entry
ampl
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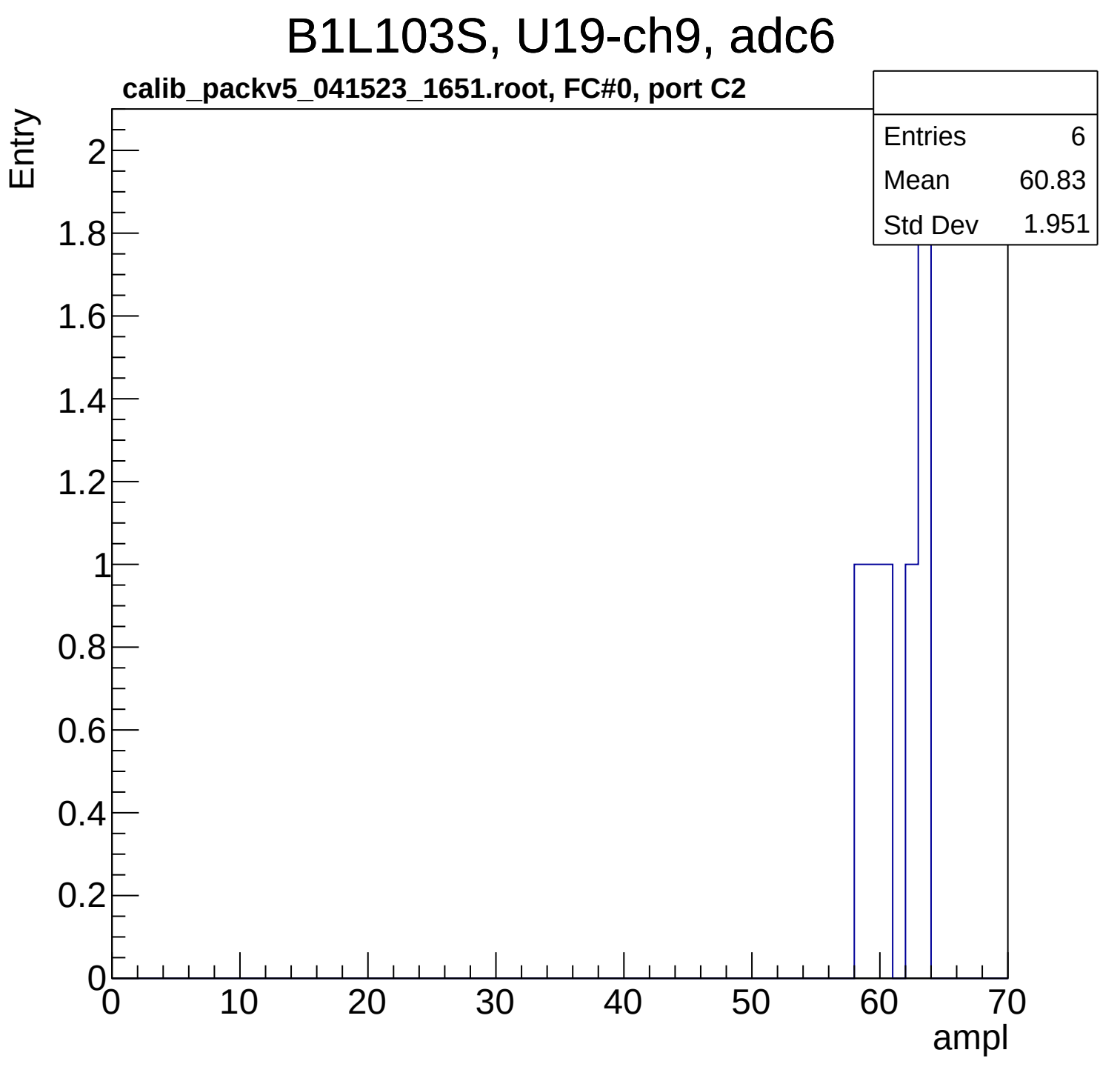
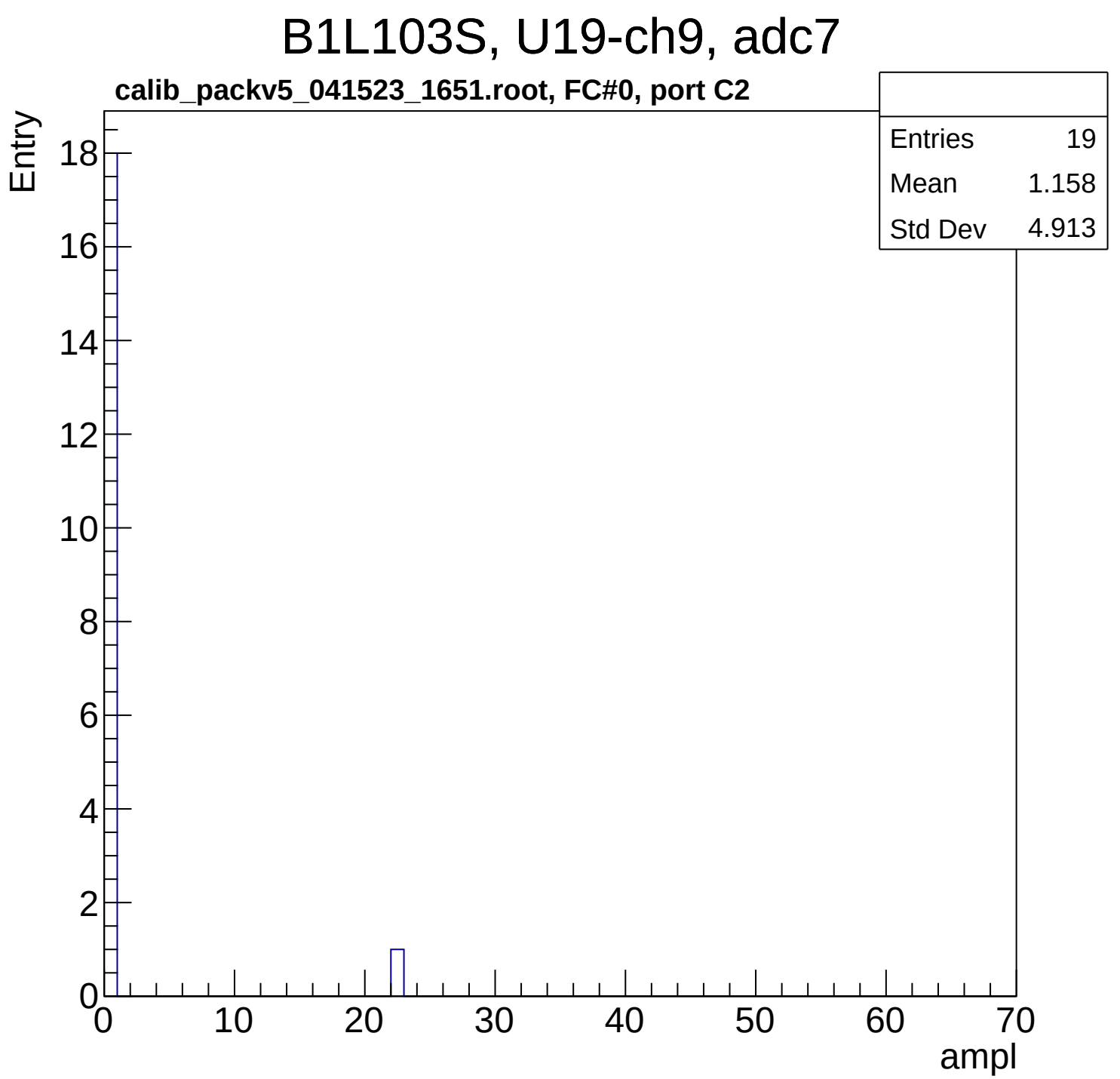
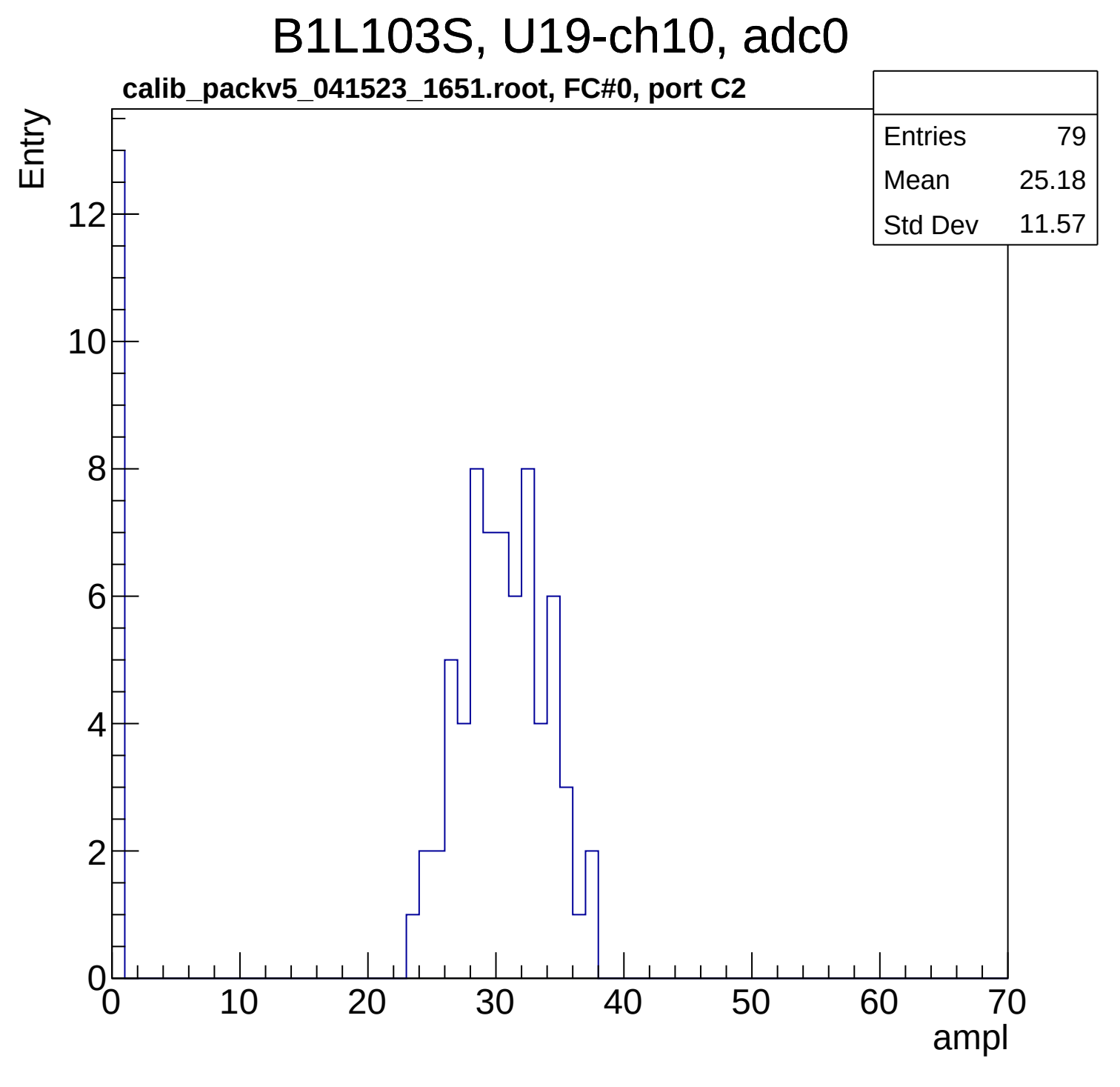
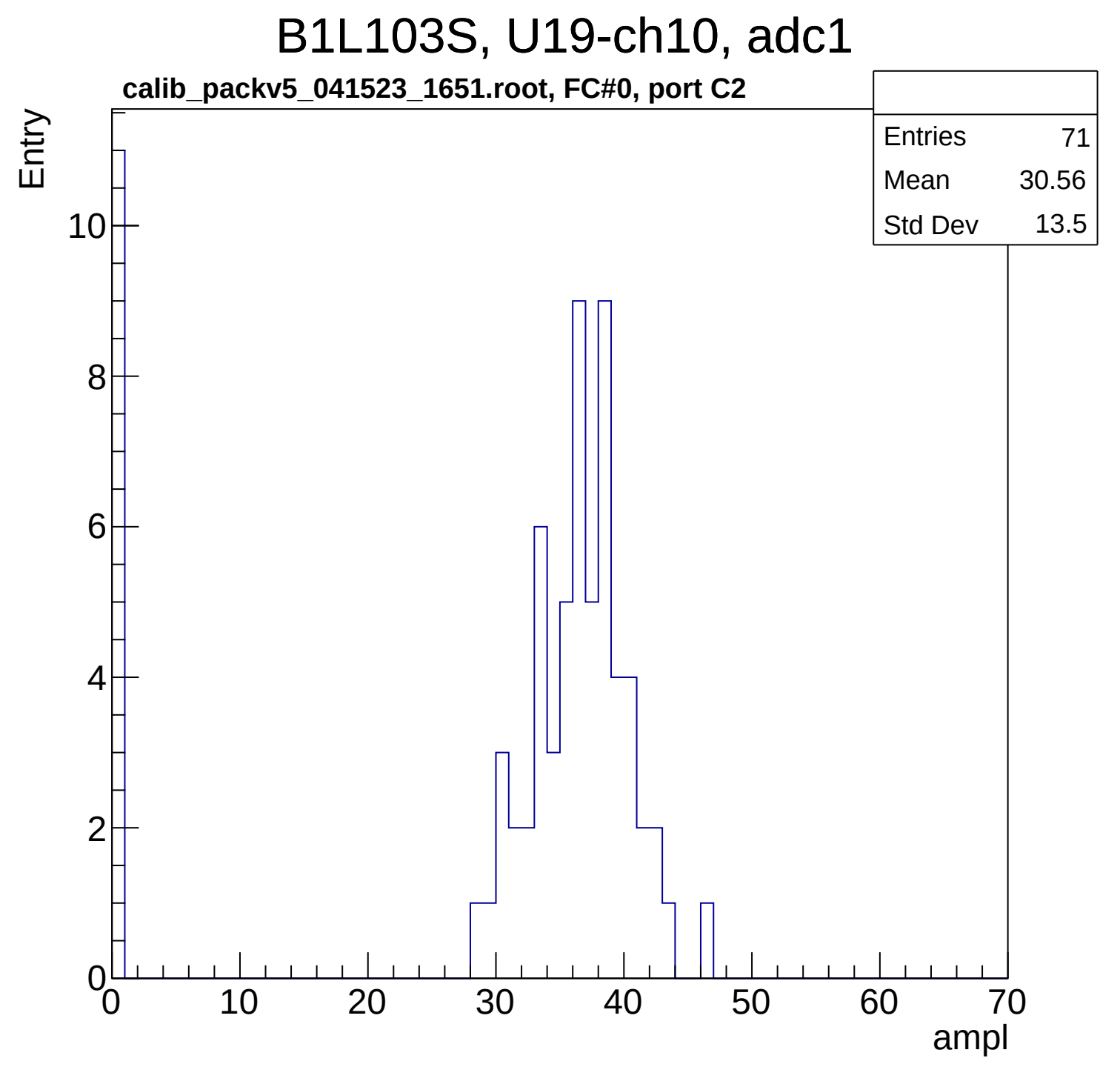
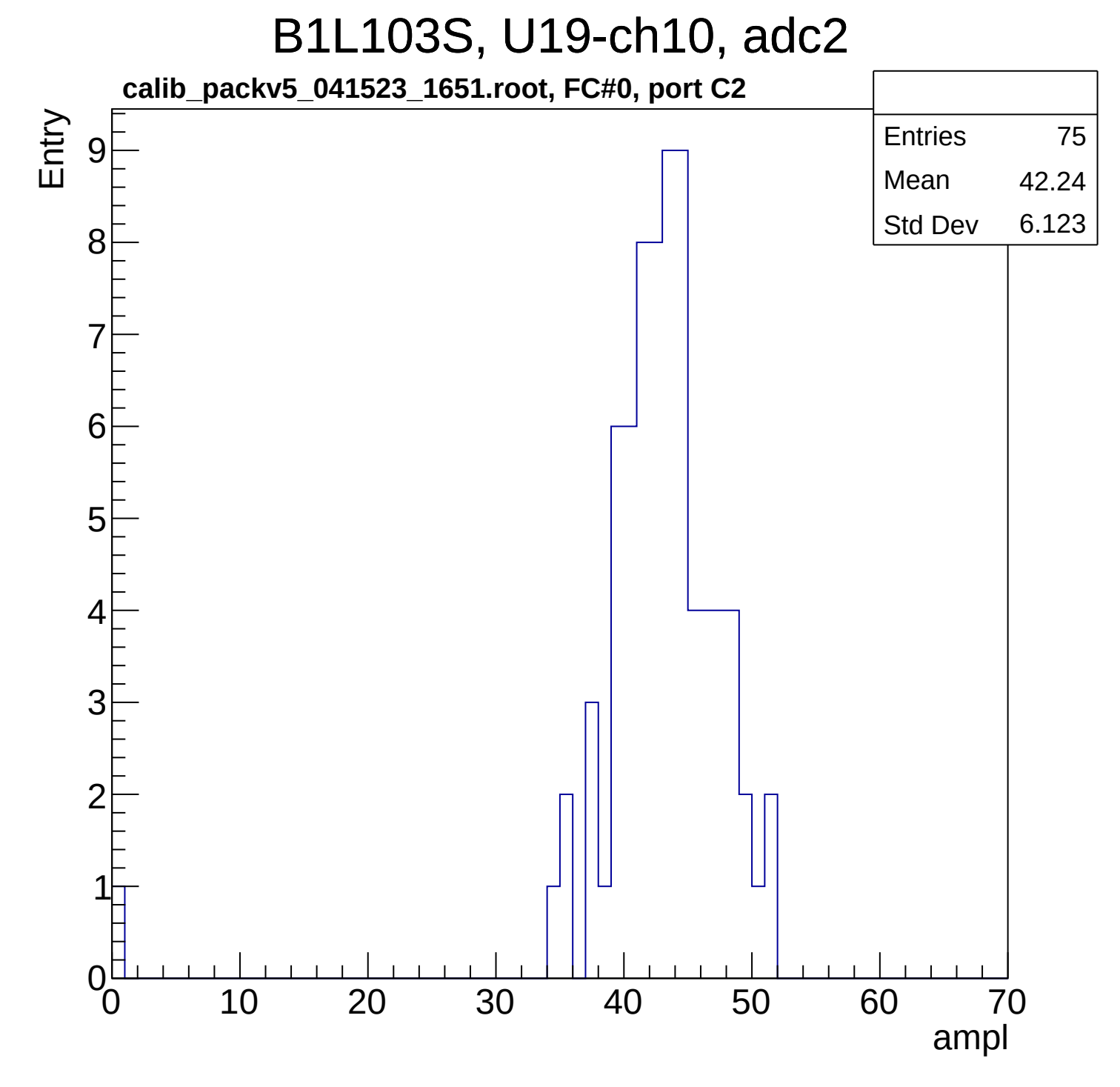
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch9, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 60.83
Std Dev 1.951
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U19-ch9, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.158
Std Dev 4.913
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch10, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 25.18
Std Dev 11.57
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch10, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 30.56
Std Dev 13.5
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch10, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 42.24
Std Dev 6.123
Entry
ampl
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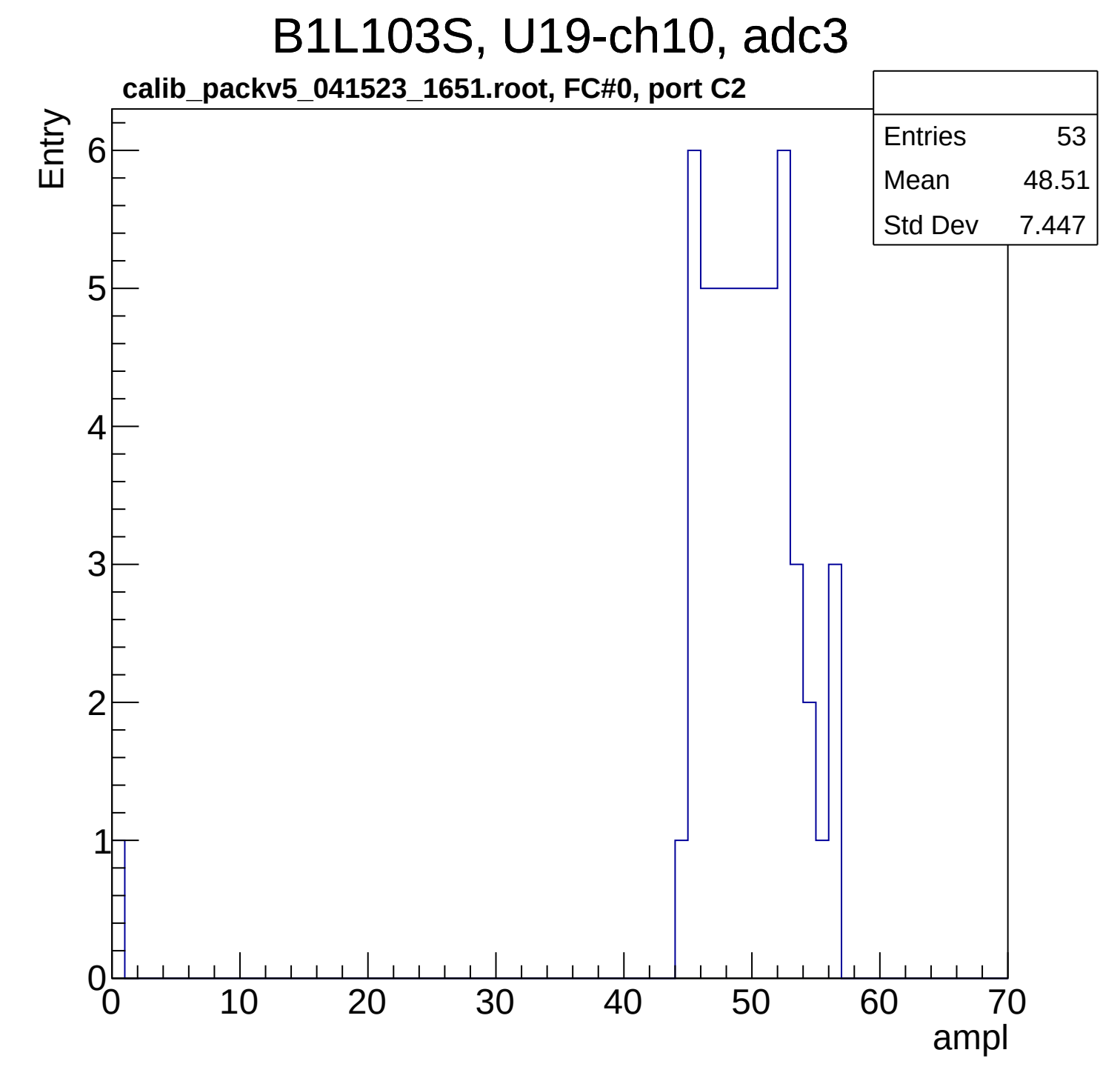
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch10, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 48.51
Std Dev 7.447
Entry
ampl
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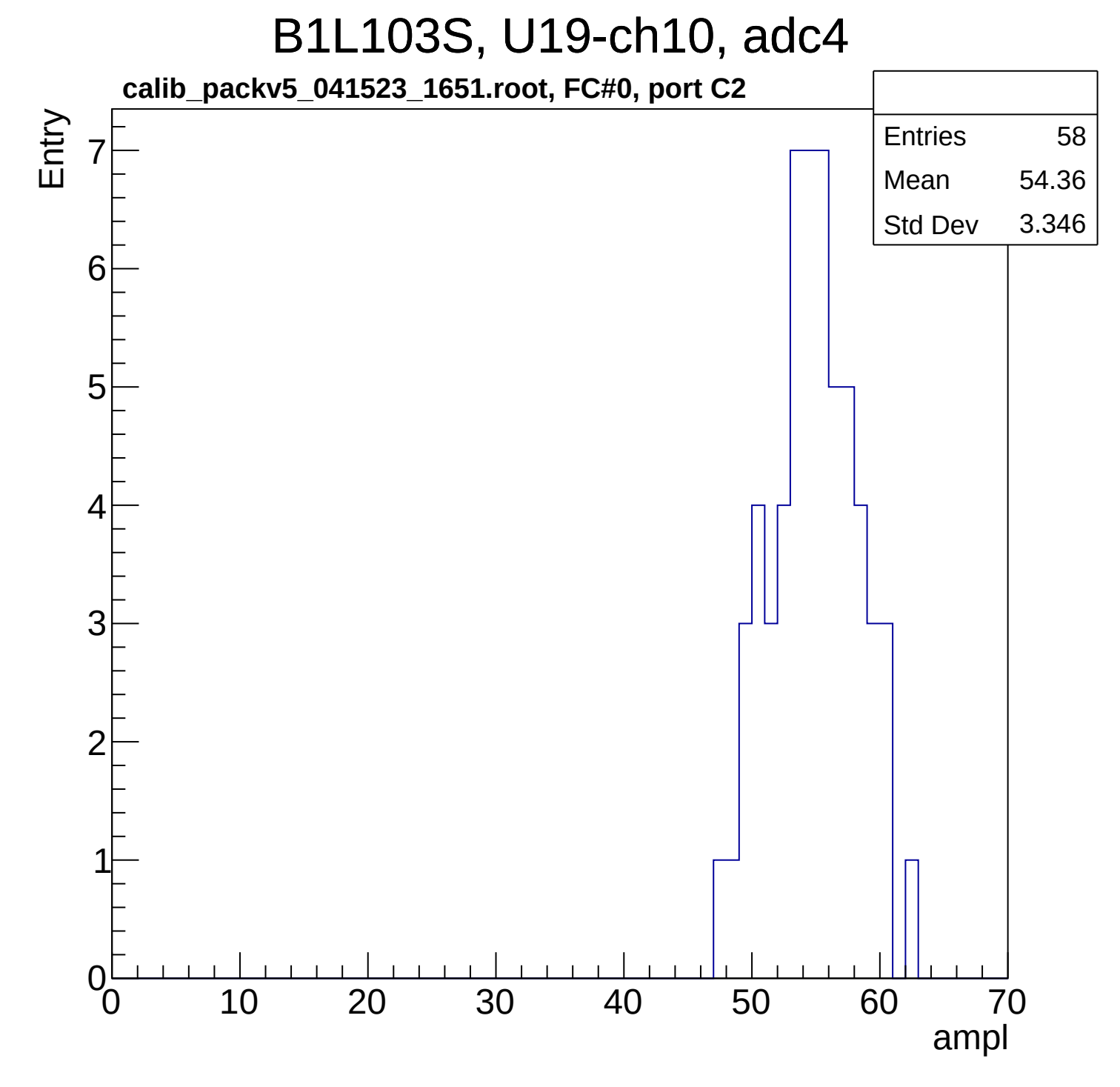
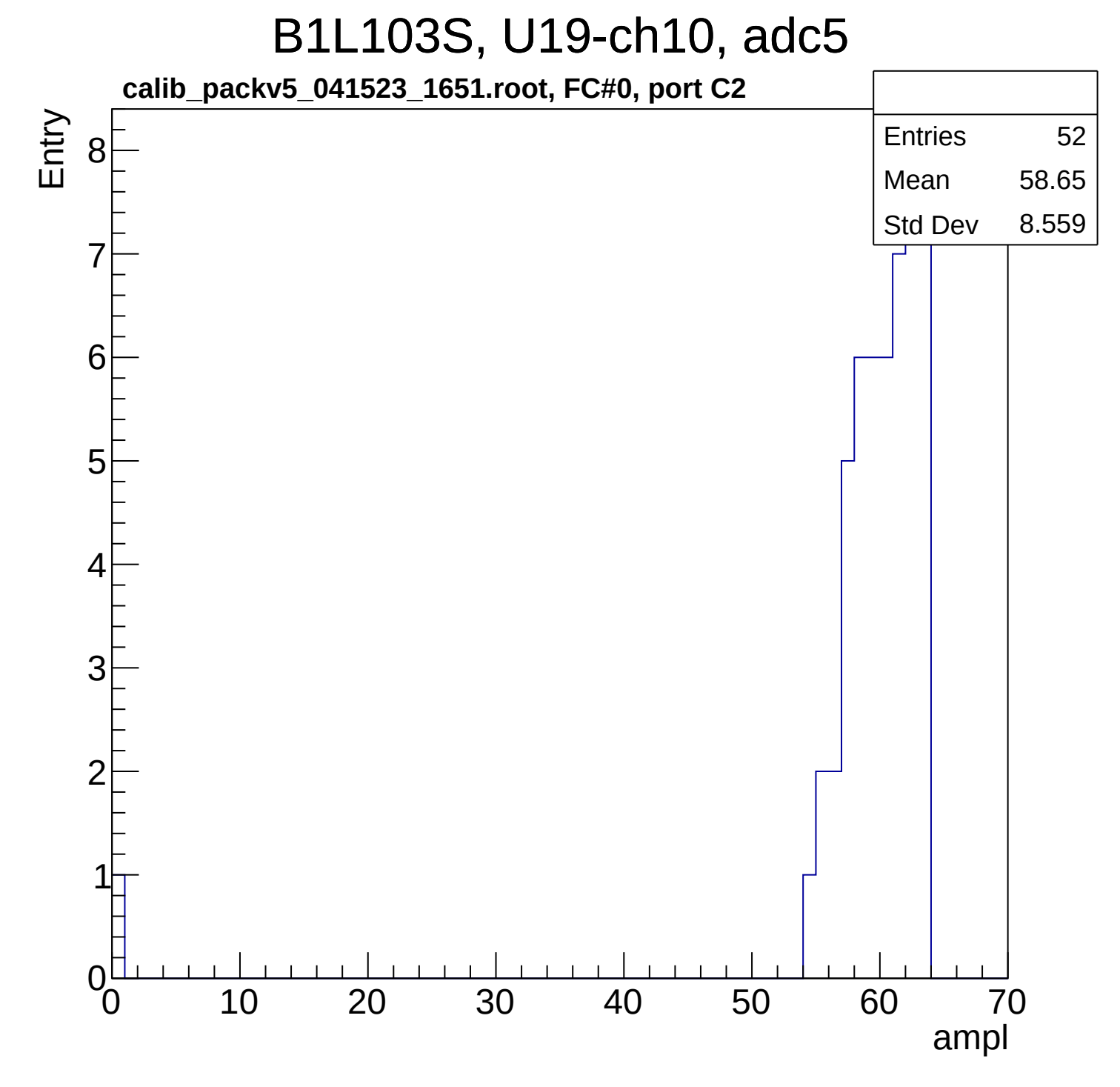
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U19-ch10, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 54.36
Std Dev 3.346
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch10, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 58.65
Std Dev 8.559
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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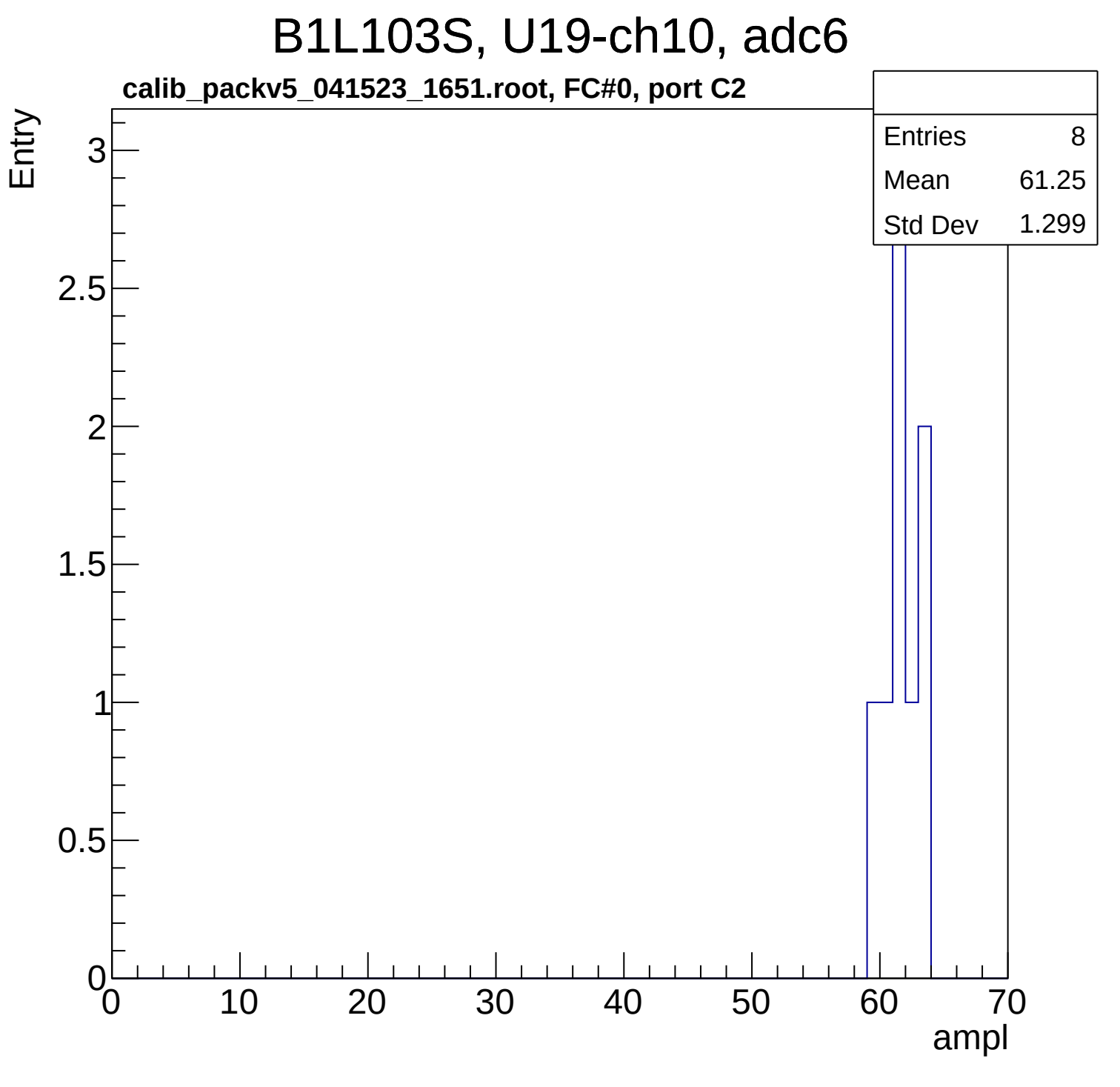
40
50
60
70


B1L103S, U19-ch10, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 61.25
Std Dev 1.299
Entry
ampl
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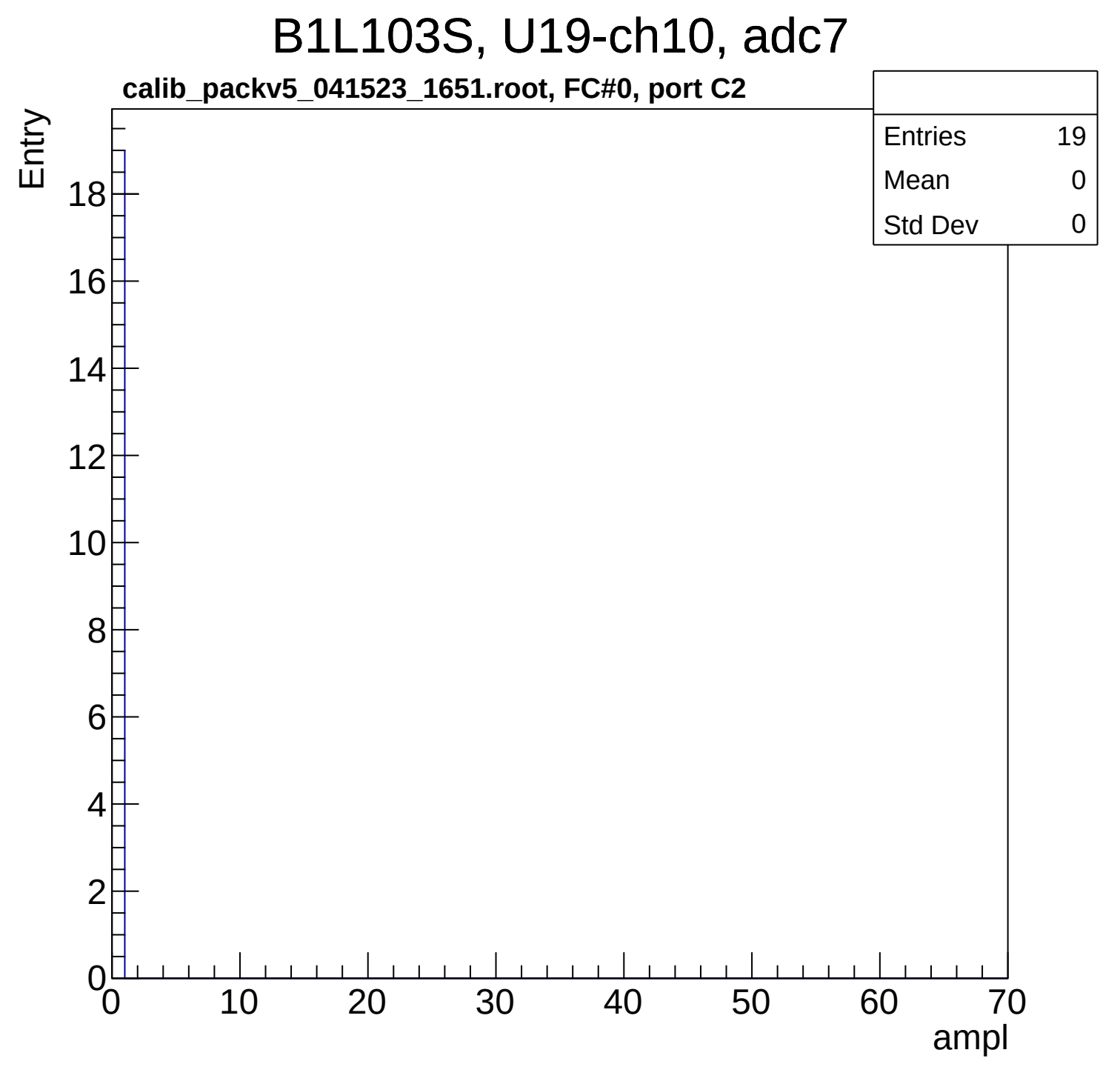
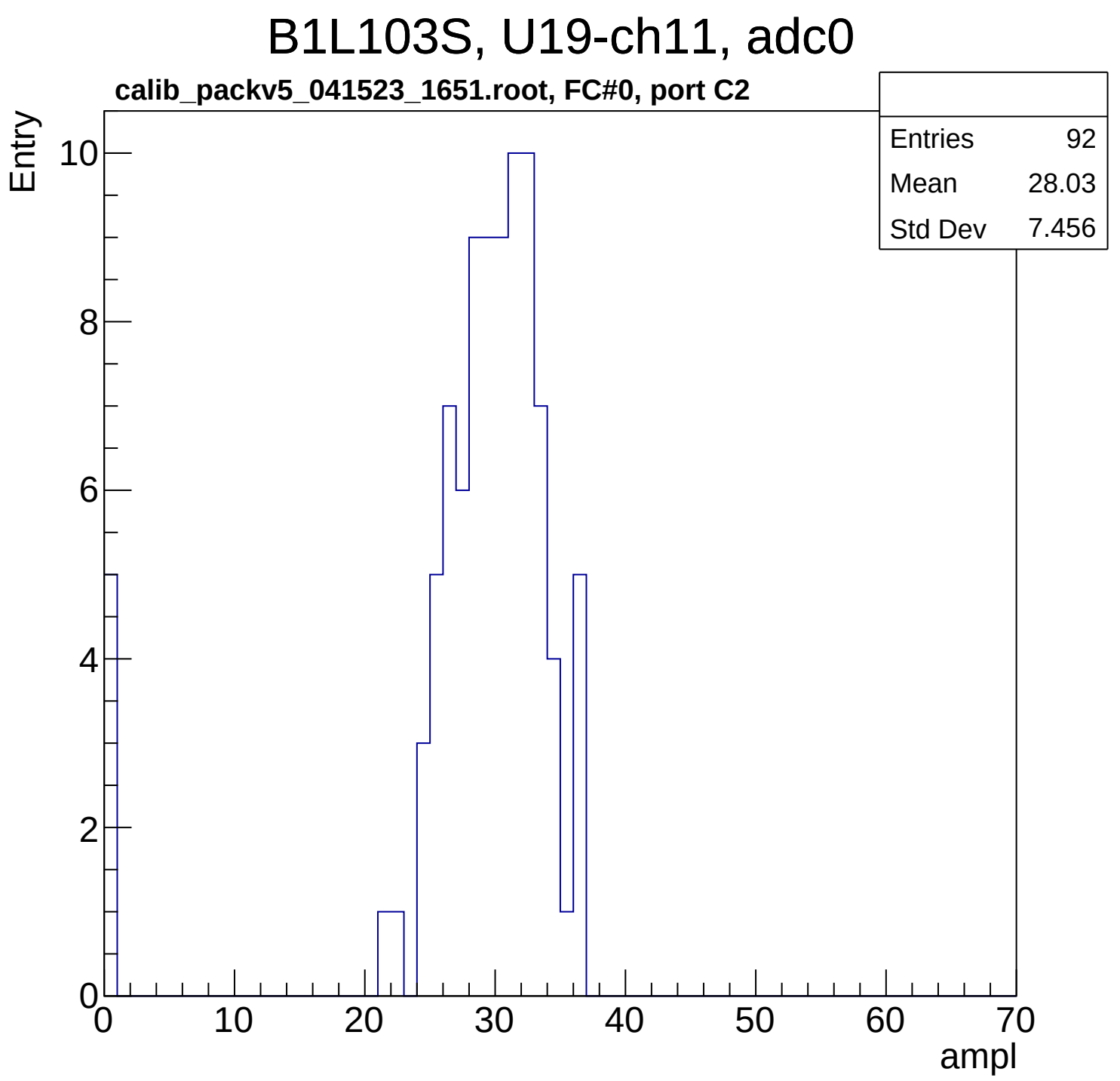
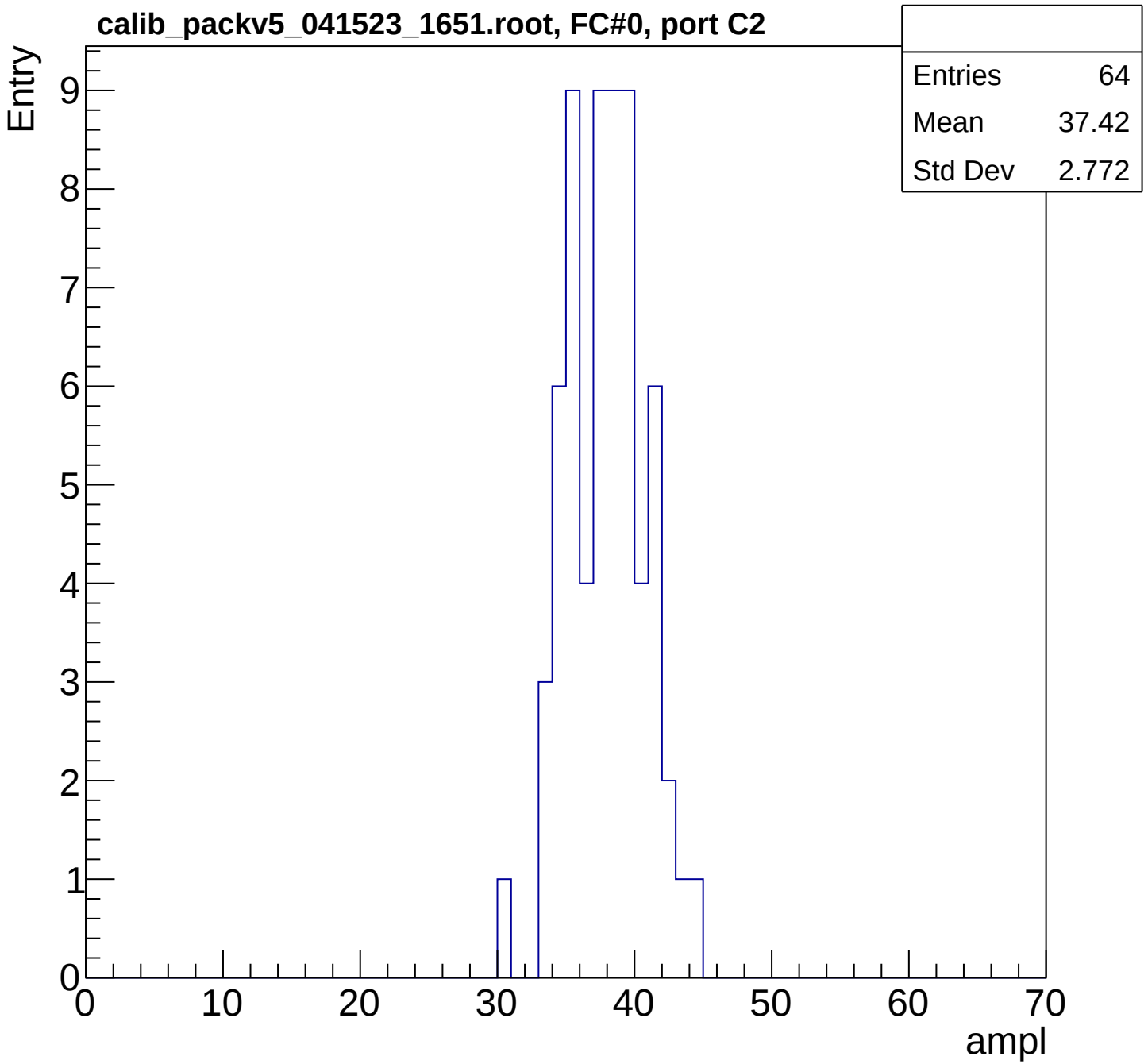
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U19-ch10, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch11, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 28.03
Std Dev 7.456
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch11, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 37.42
Std Dev 2.772
Entry
ampl
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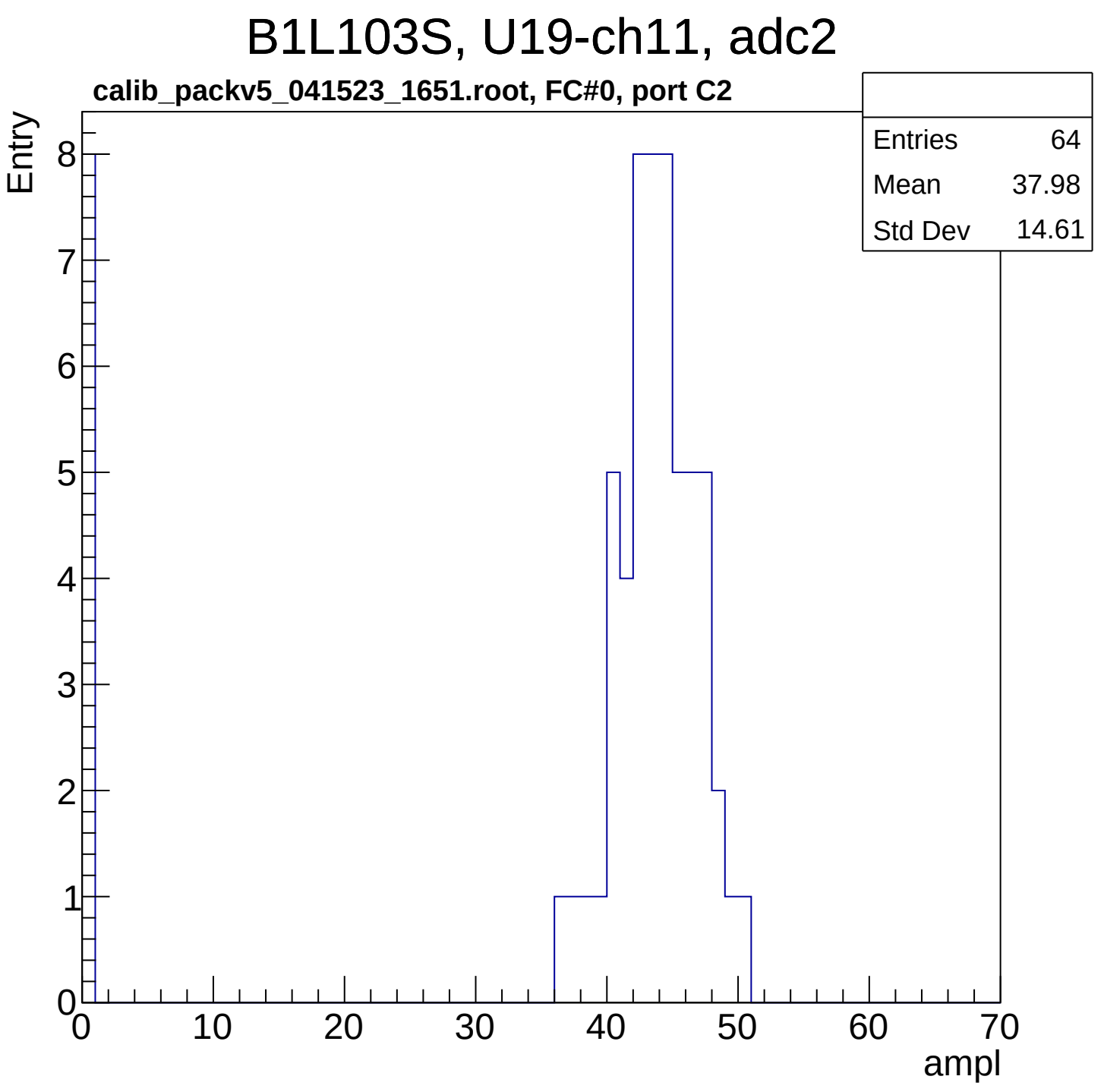
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch11, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 37.98
Std Dev 14.61
Entry
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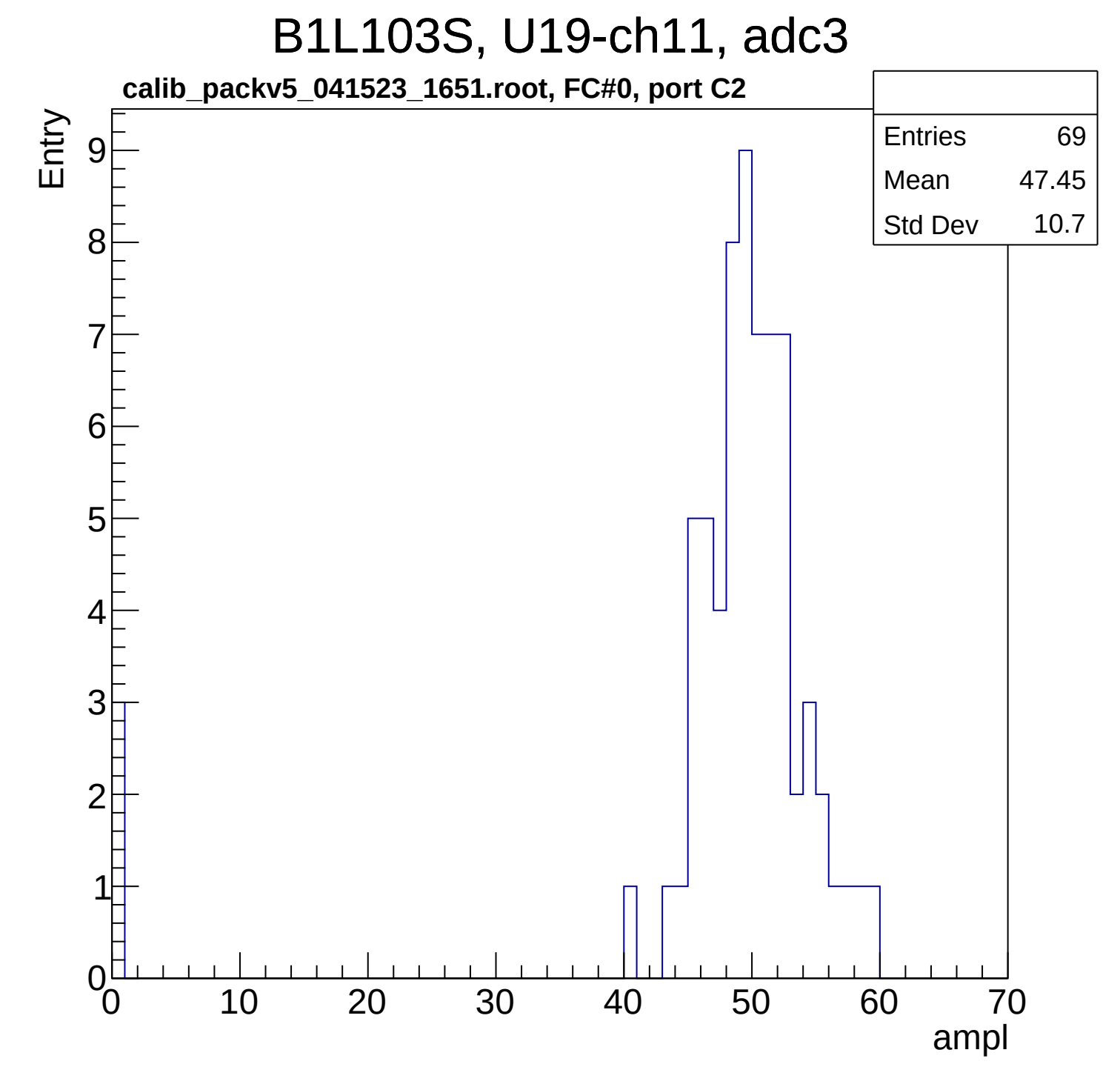
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch11, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 47.45
Std Dev 10.7
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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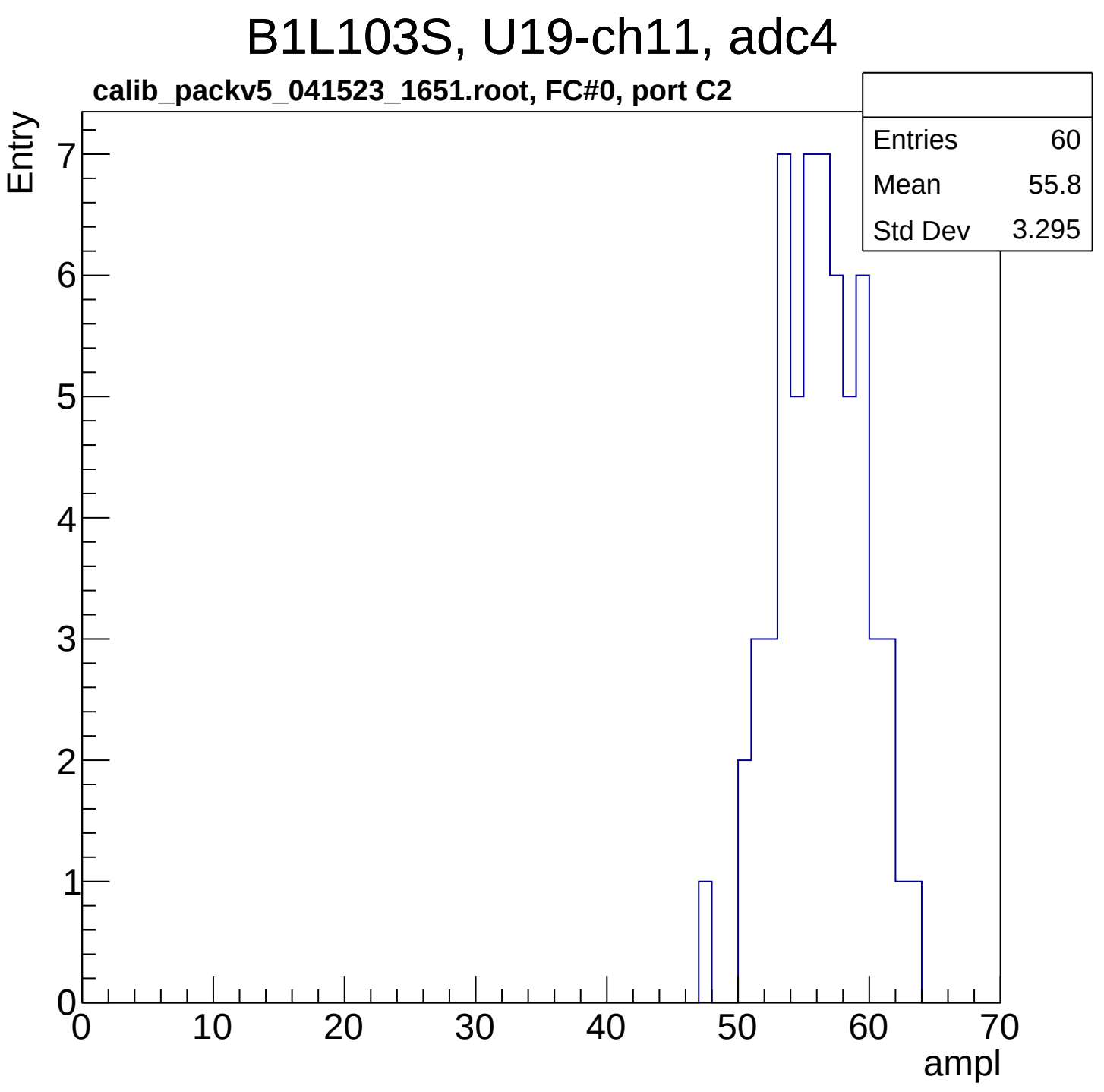
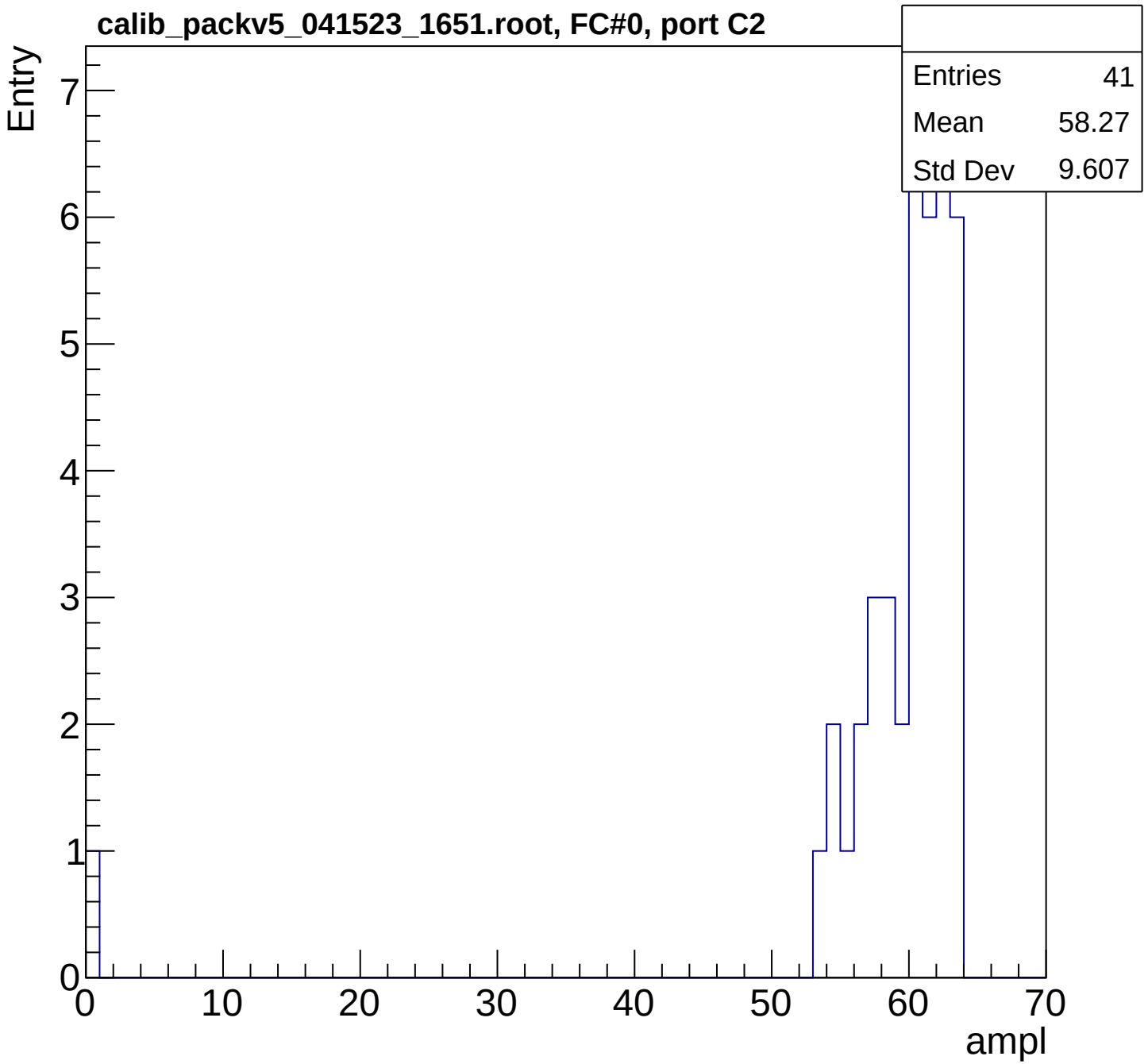
40
50
60
70


B1L103S, U19-ch11, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 55.8
Std Dev 3.295
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch11, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 58.27
Std Dev 9.607
Entry
ampl
0
1
2
3
4
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0
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40
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60
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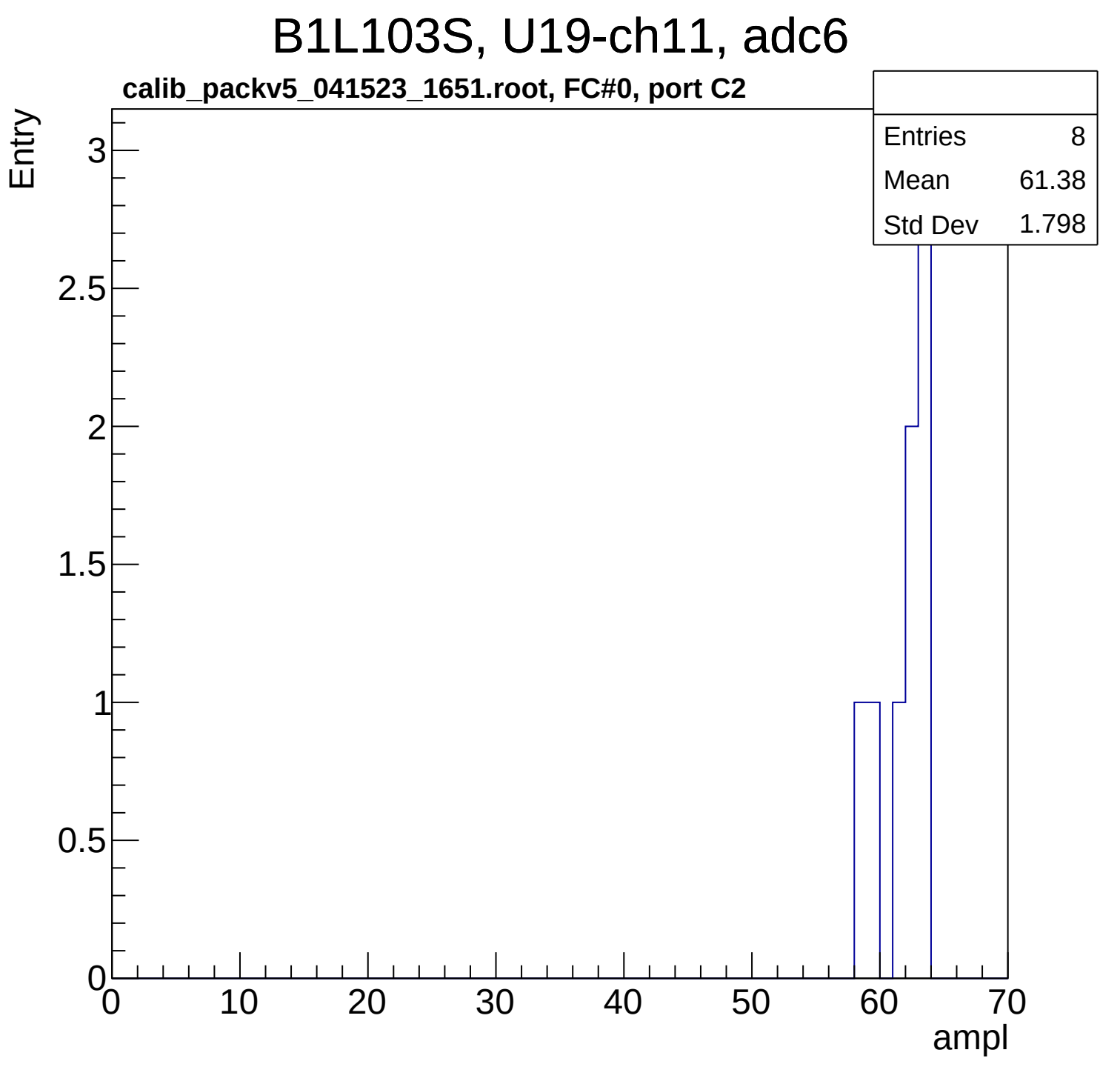
B1L103S, U19-ch11, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 61.38
Std Dev 1.798
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
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40
50
60
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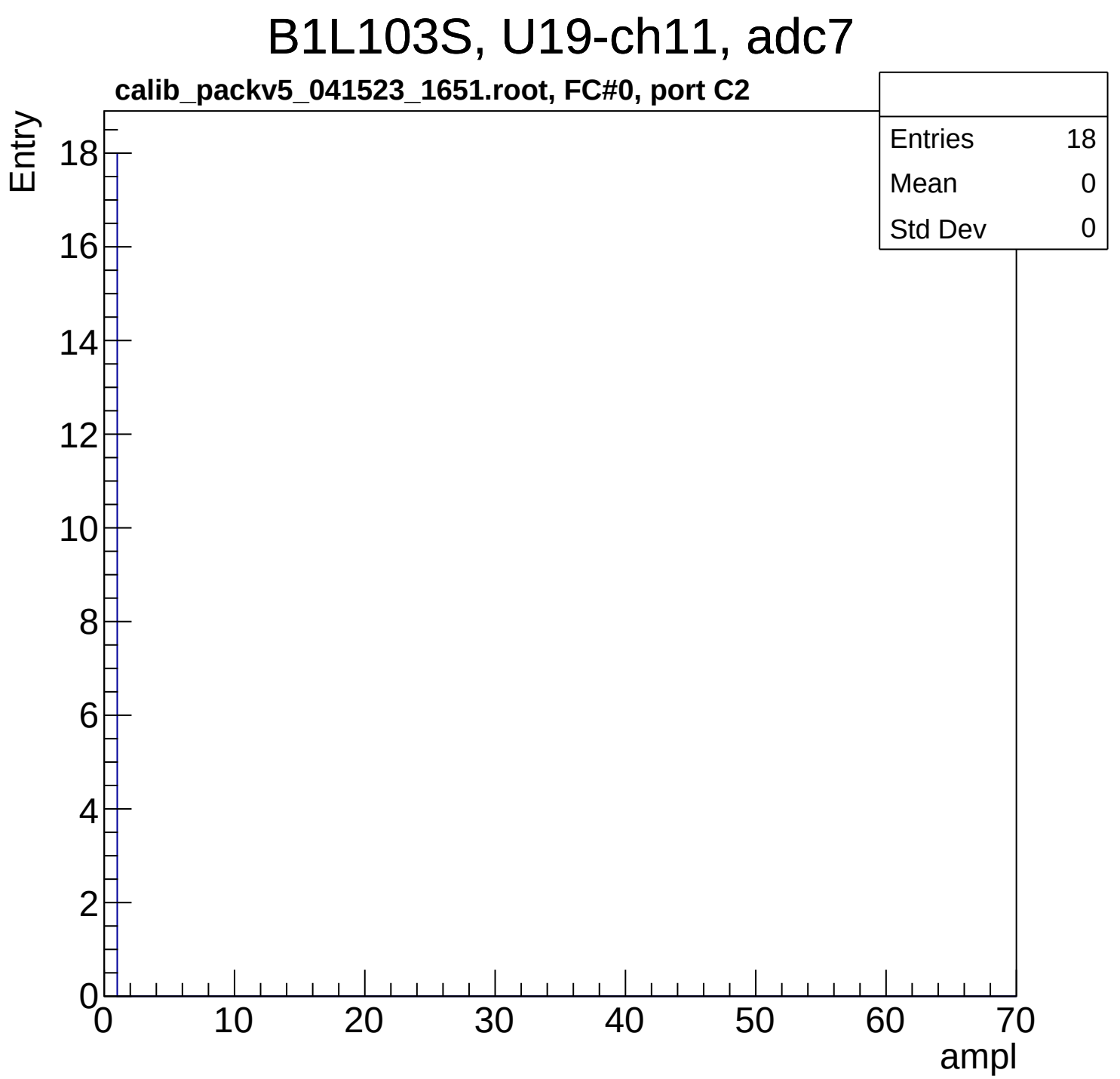
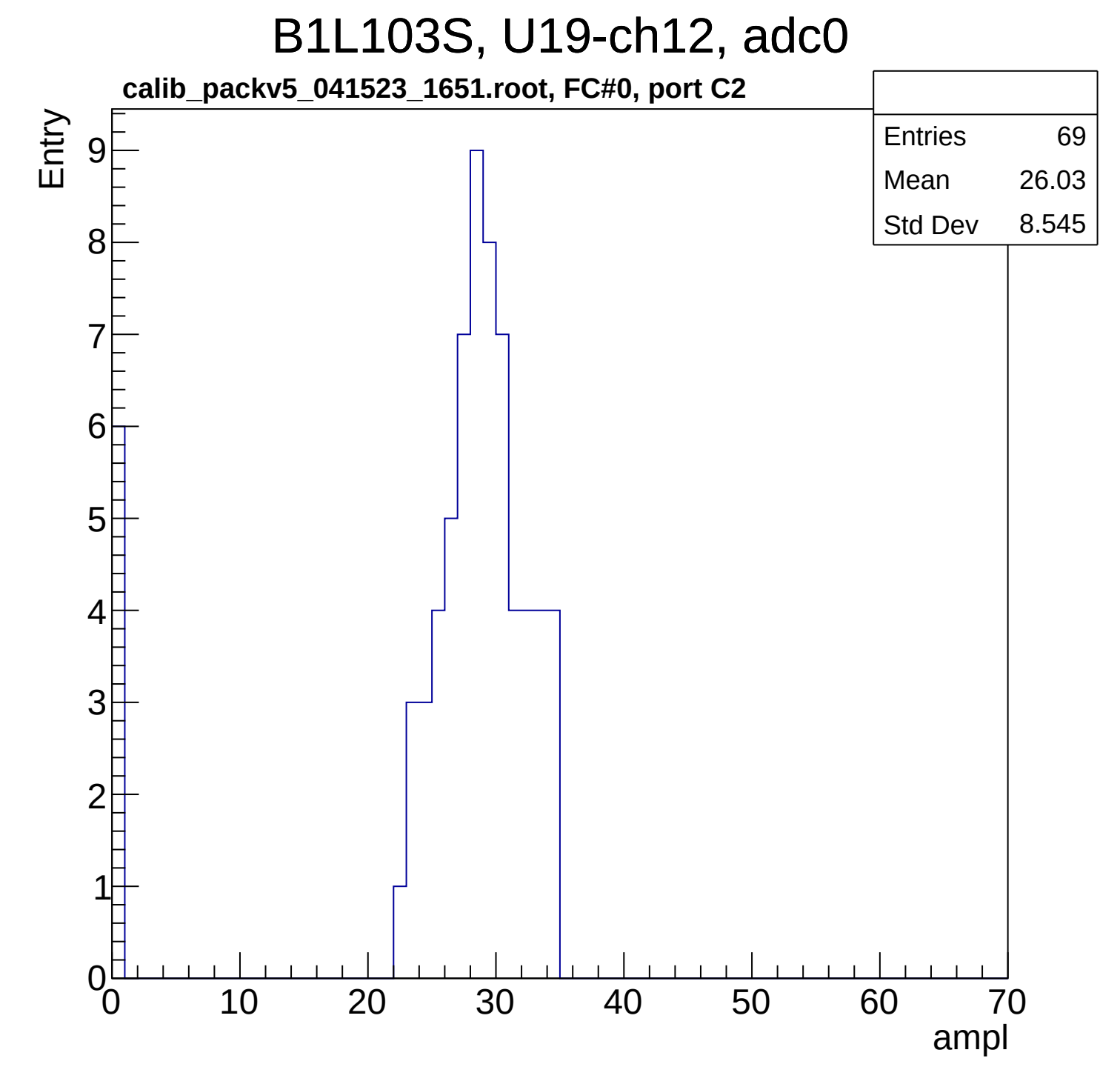

B1L103S, U19-ch11, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch12, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 26.03
Std Dev 8.545
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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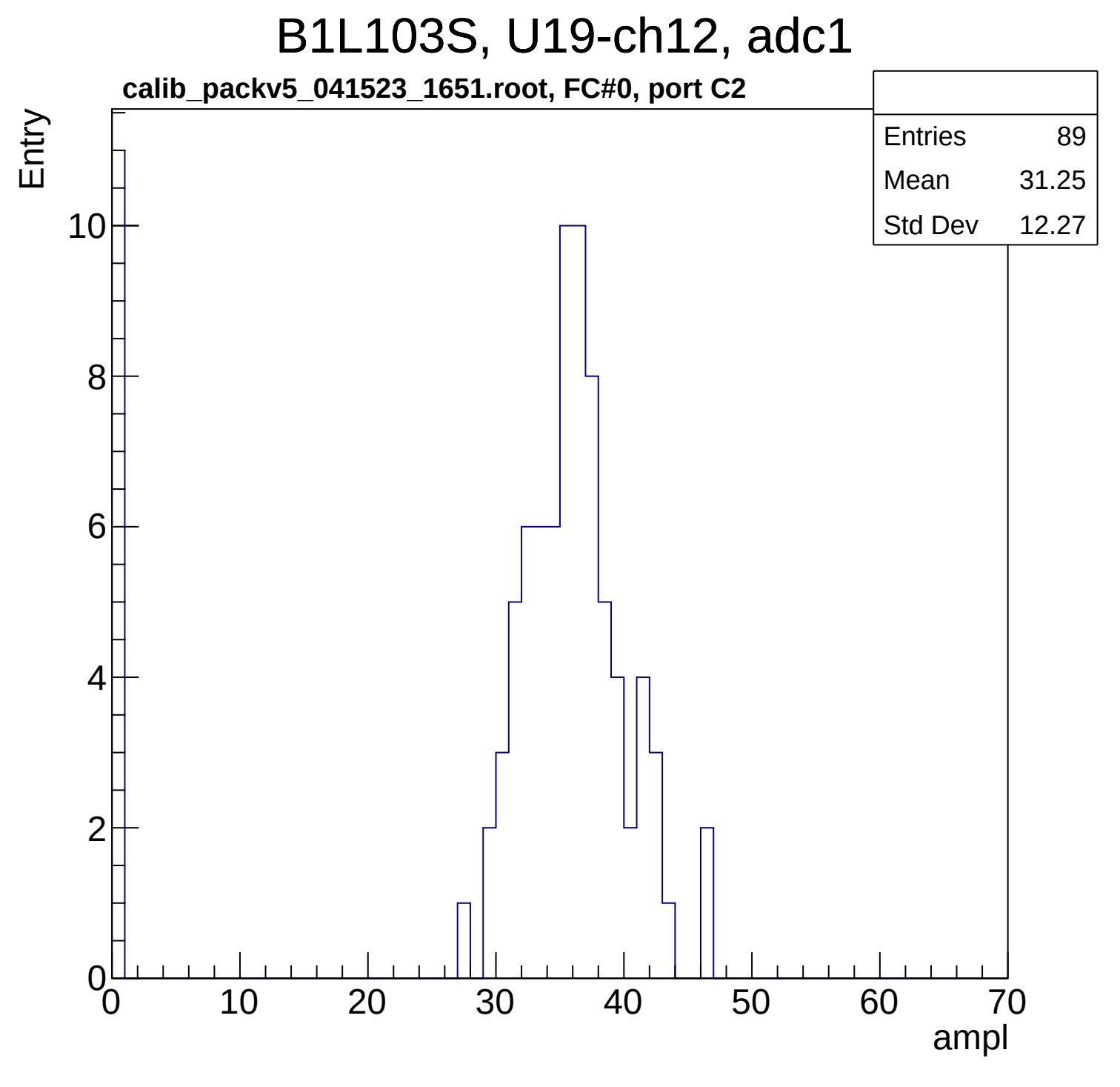
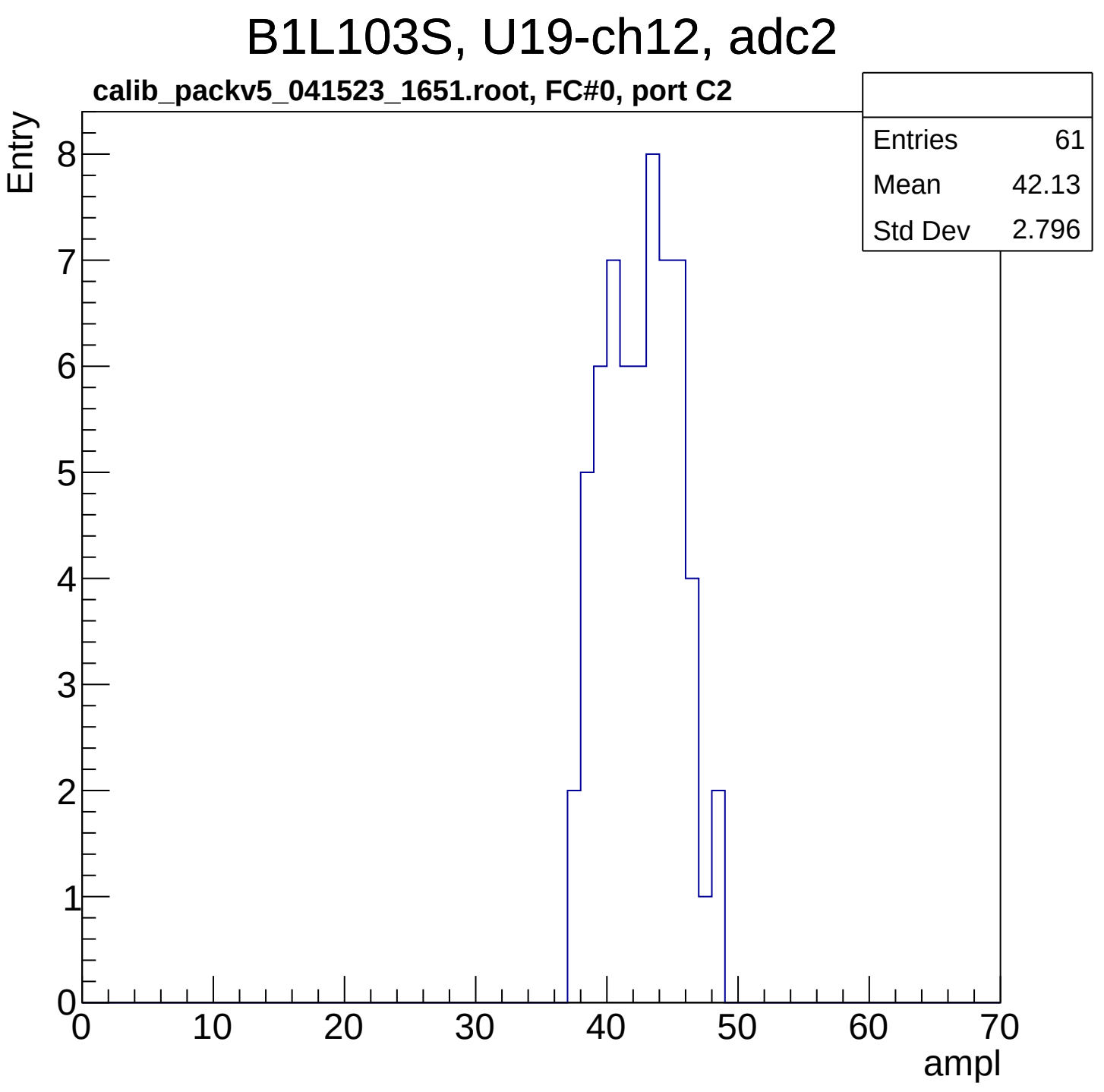

B1L103S, U19-ch12, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 31.25
Std Dev 12.27
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch12, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 42.13
Std Dev 2.796
Entry
ampl
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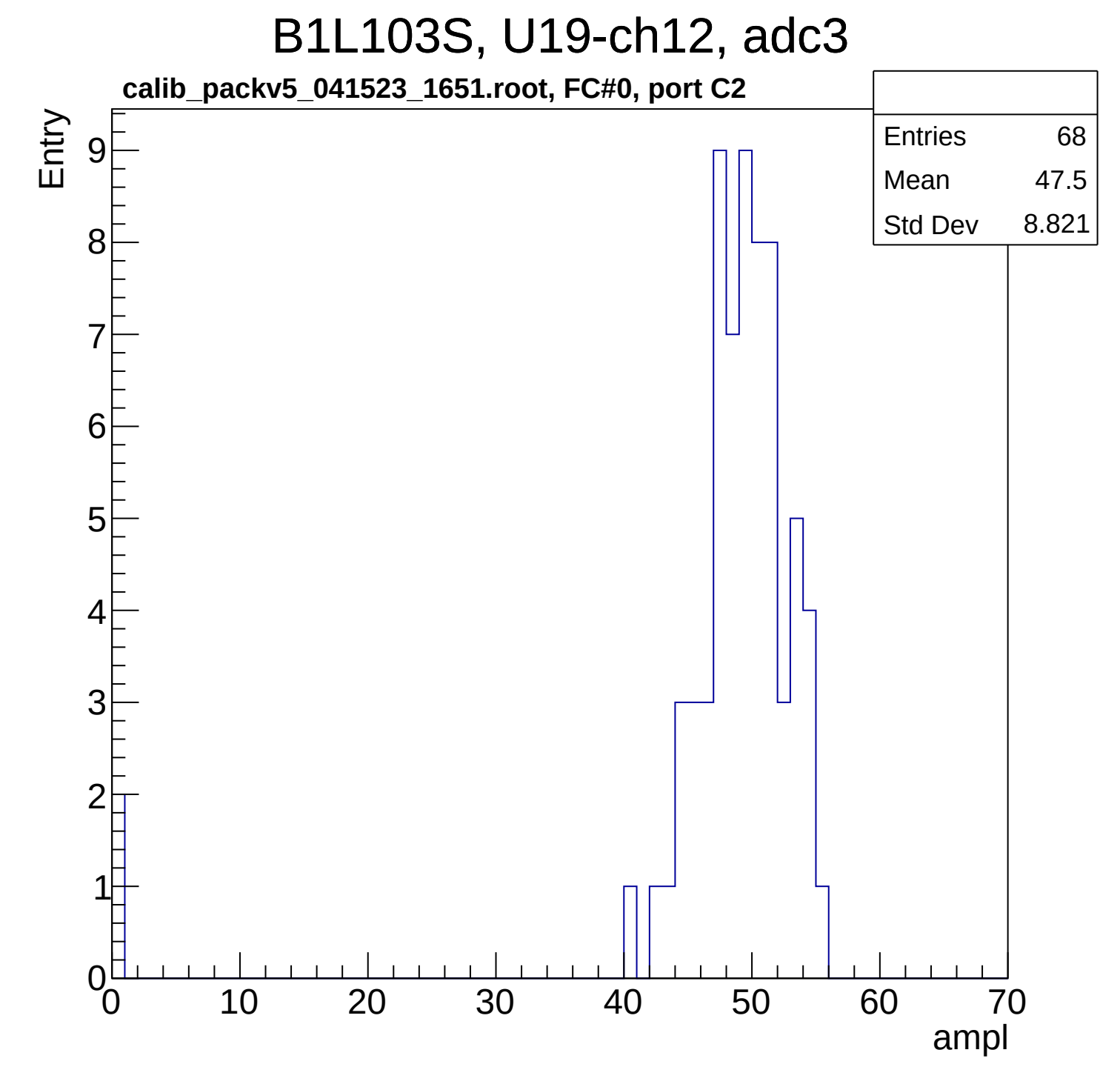
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch12, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 47.5
Std Dev 8.821
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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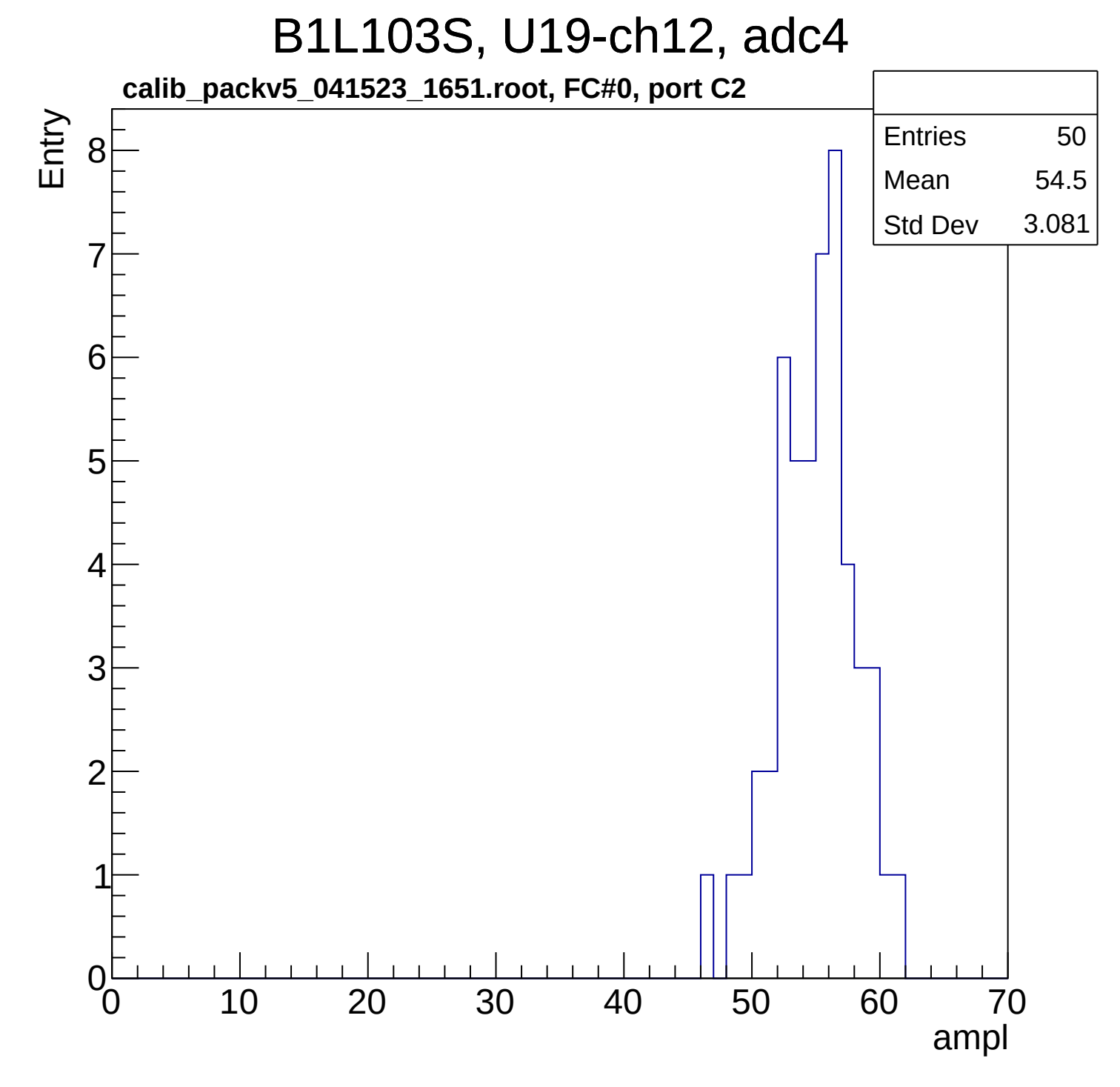
B1L103S, U19-ch12, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 54.5
Std Dev 3.081
Entry
ampl
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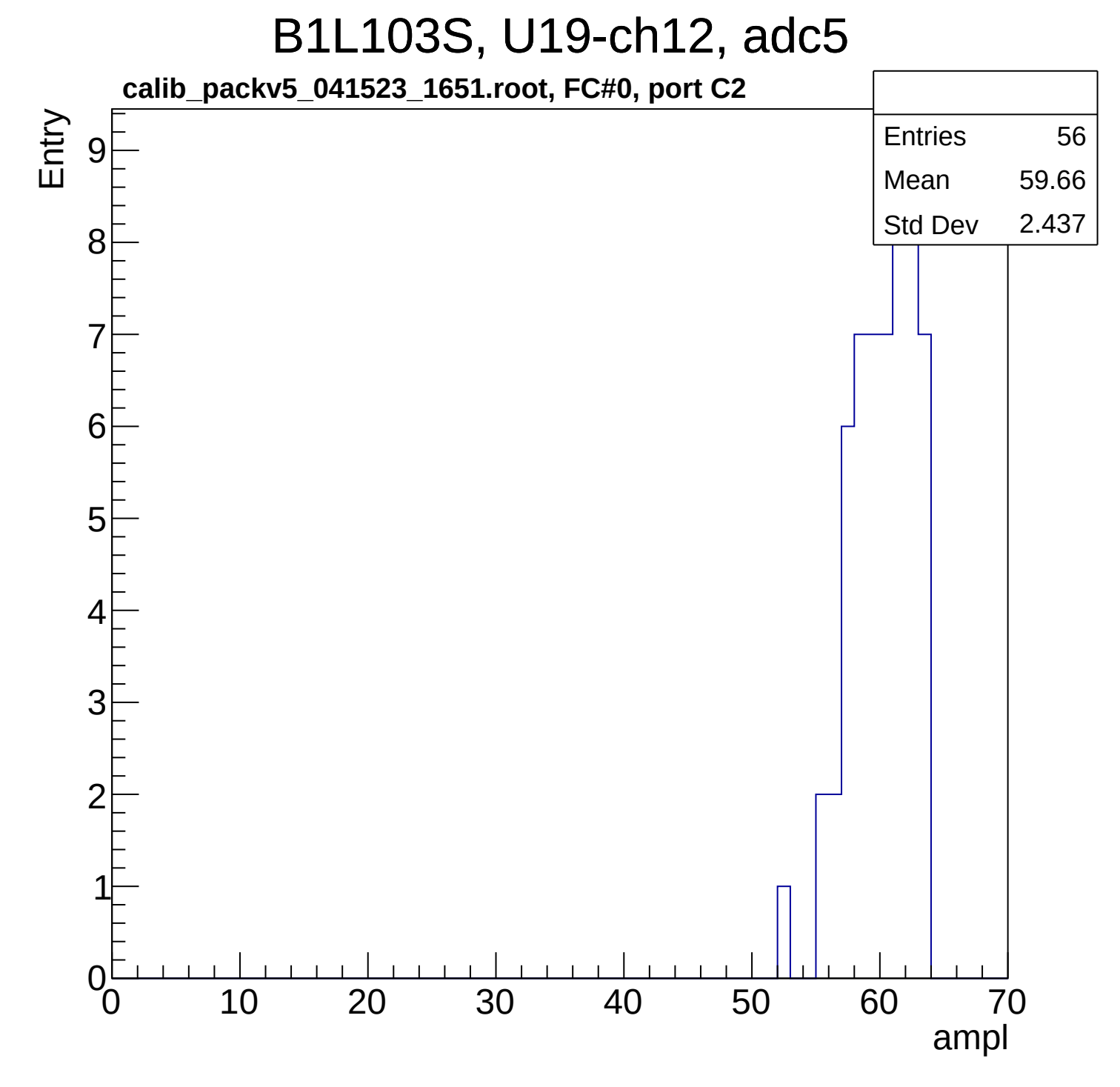
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch12, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 59.66
Std Dev 2.437
Entry
ampl
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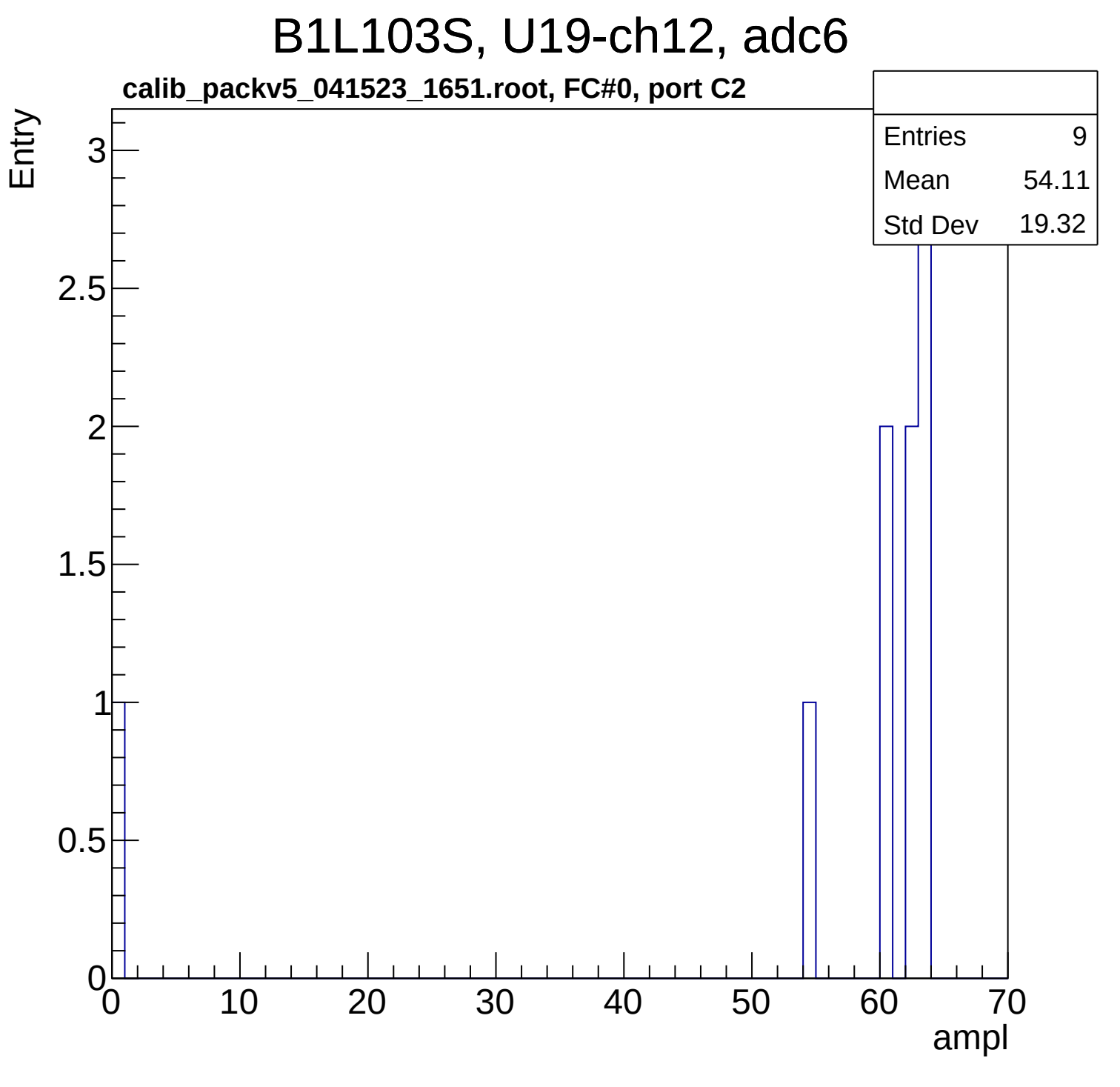
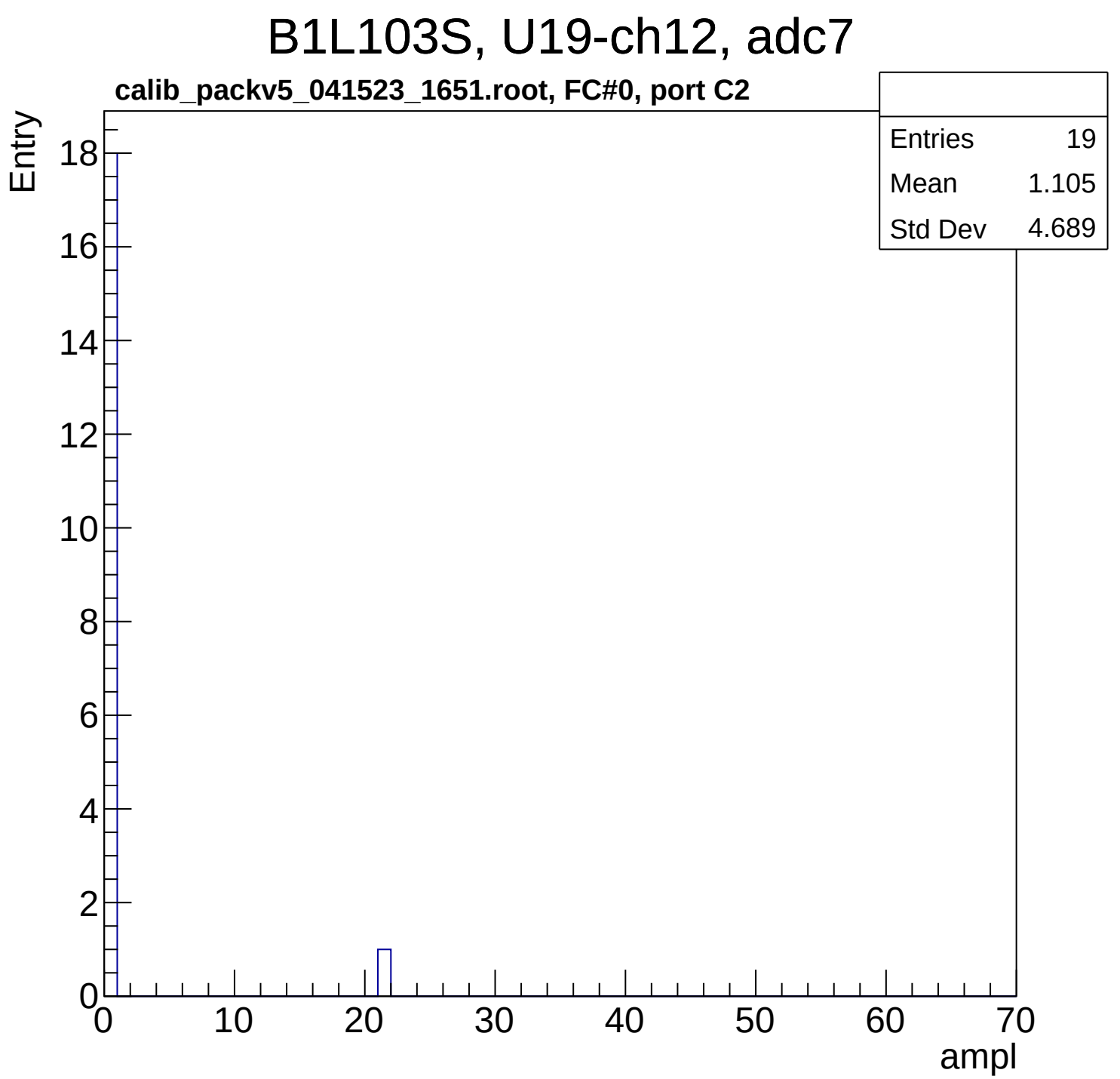
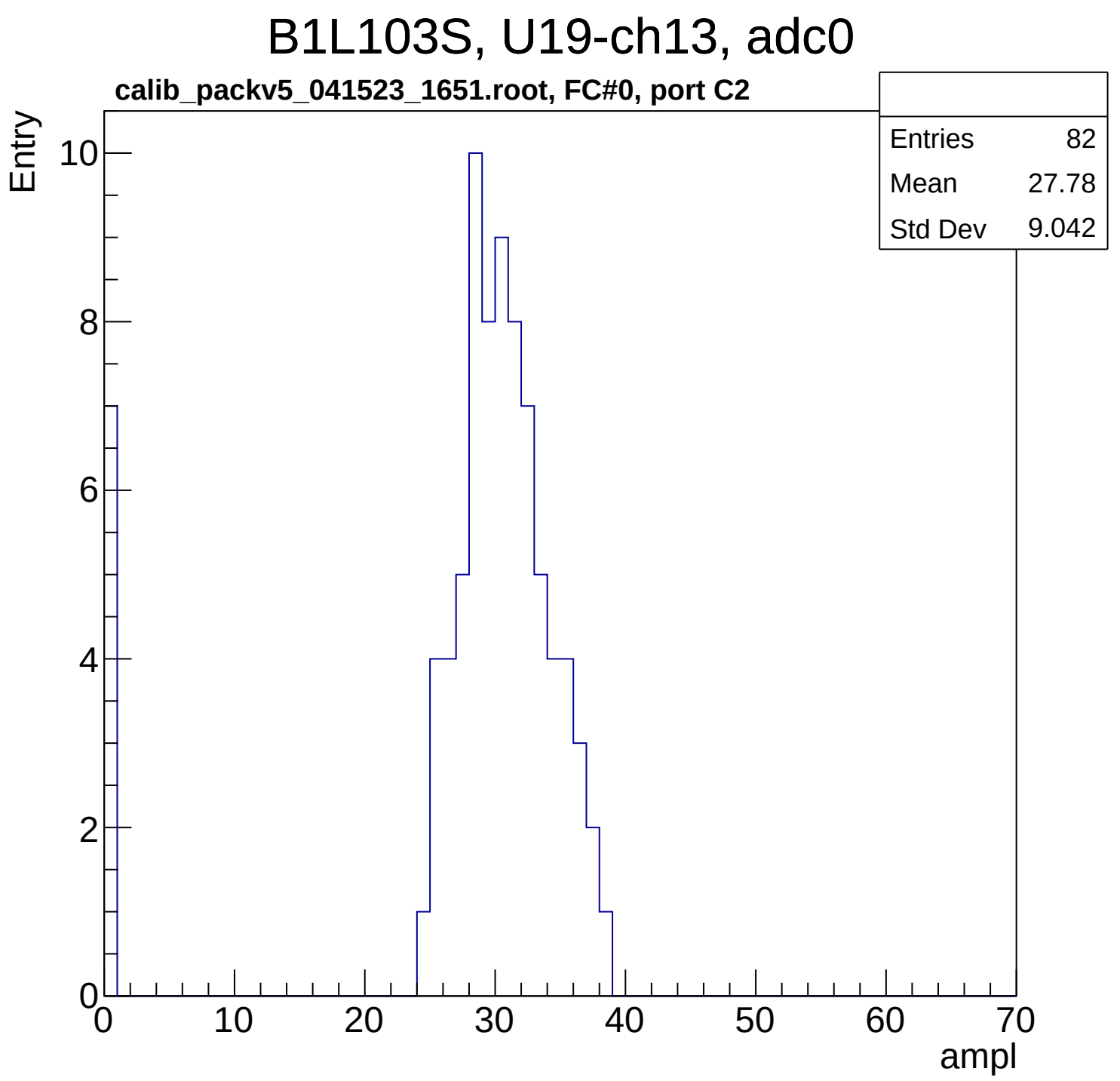
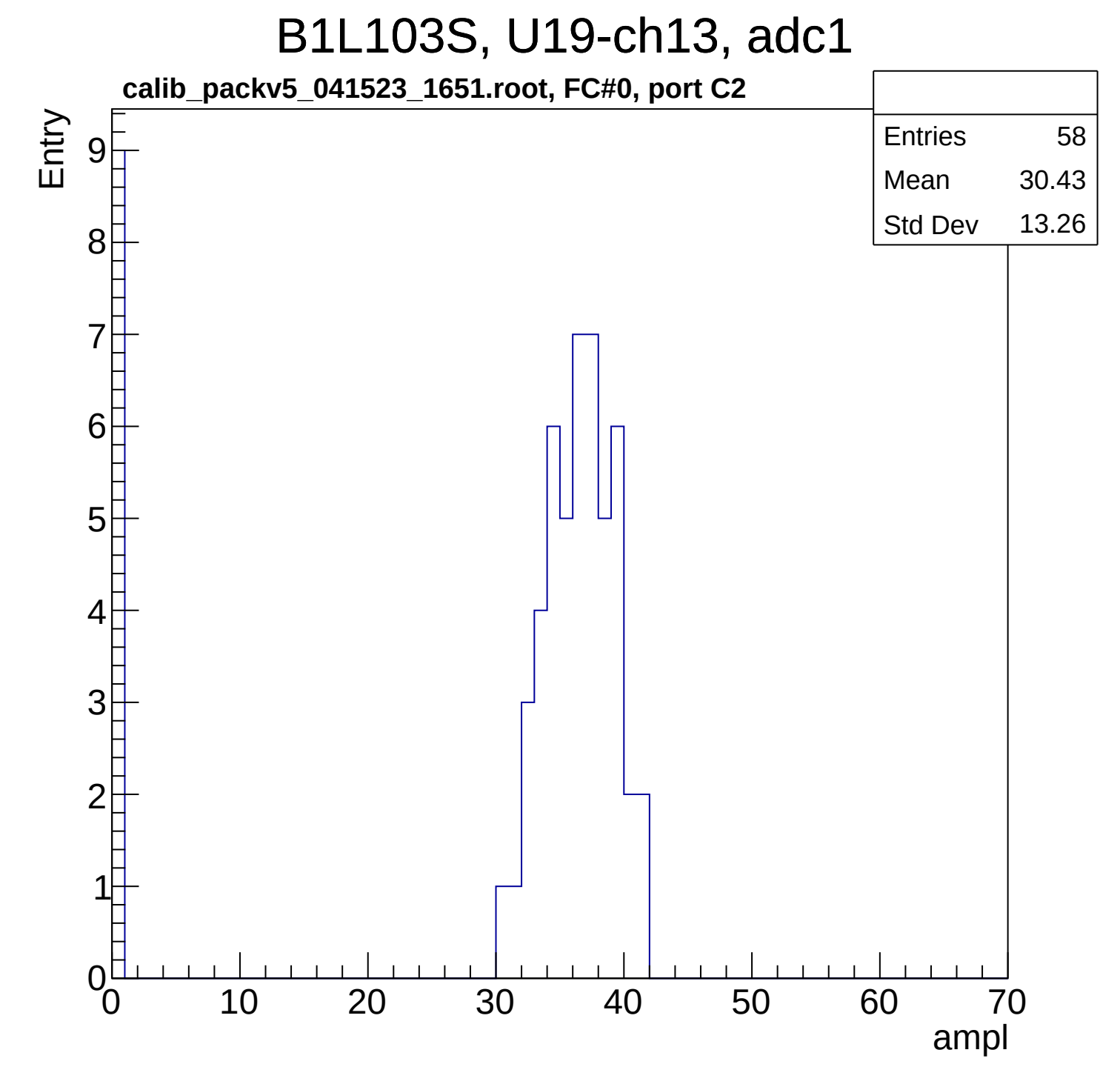
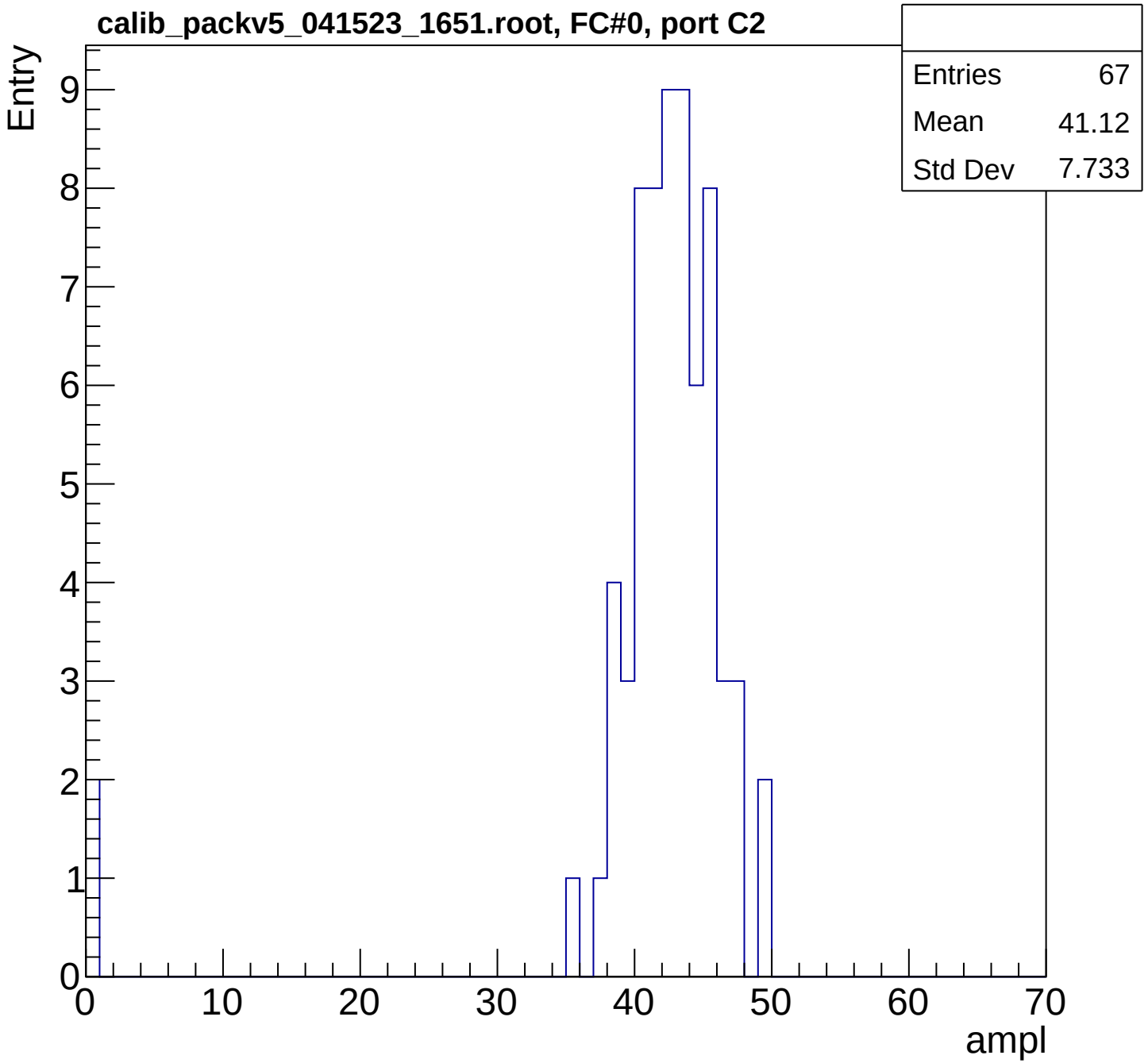
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch12, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 54.11
Std Dev 19.32
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U19-ch12, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.105
Std Dev 4.689
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch13, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 27.78
Std Dev 9.042
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch13, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 30.43
Std Dev 13.26
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch13, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 41.12
Std Dev 7.733
Entry
ampl
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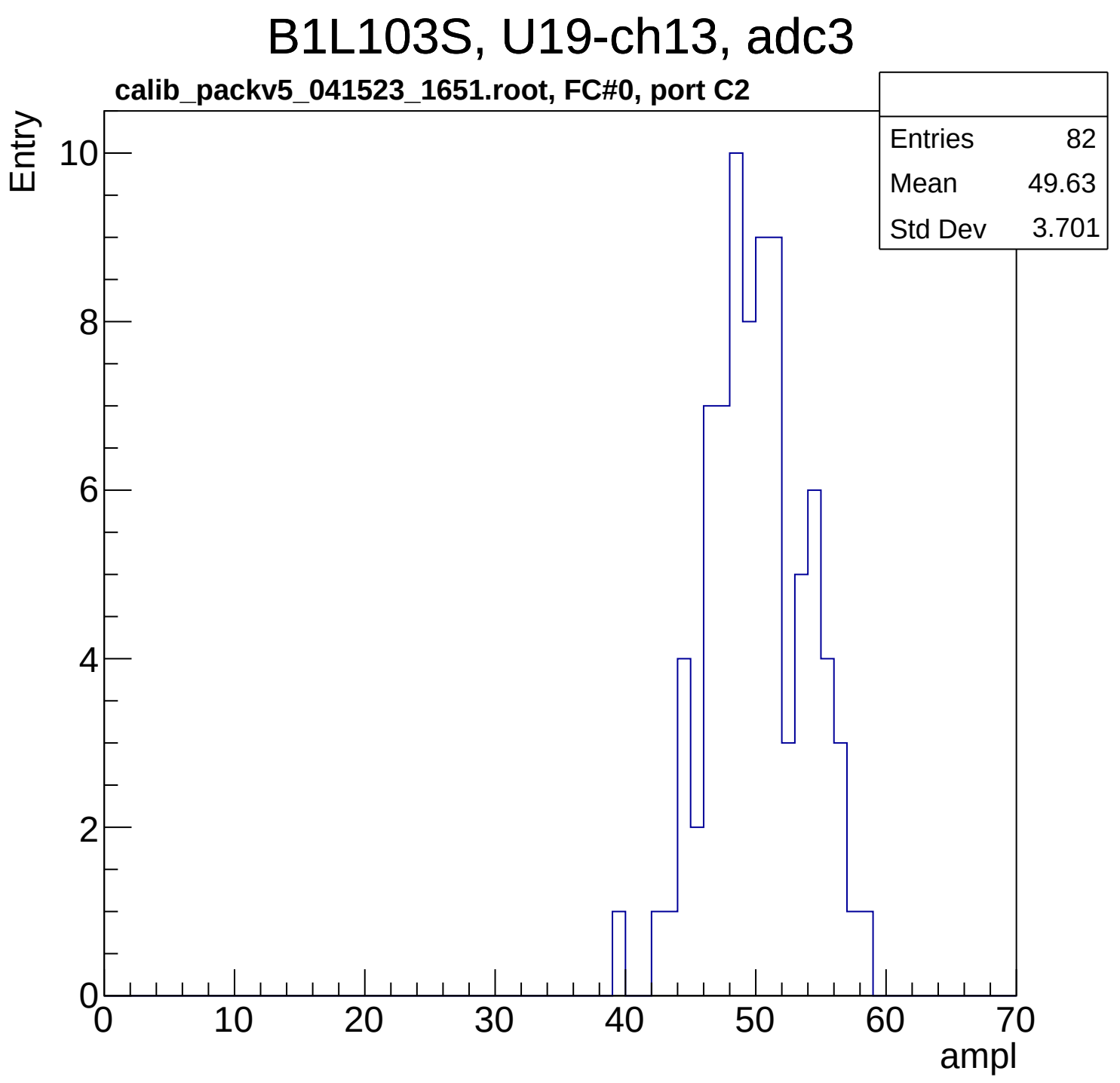
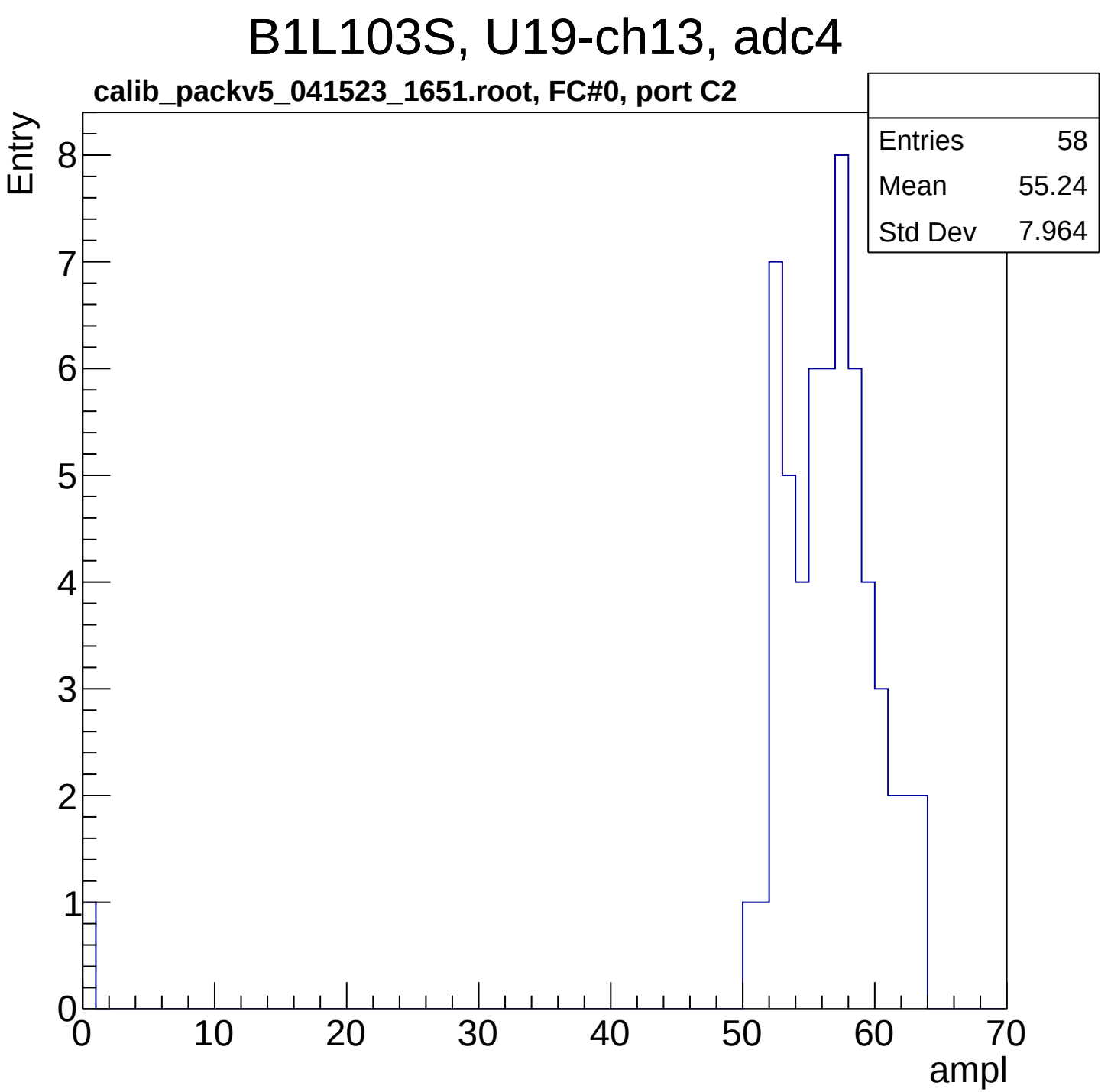
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch13, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 49.63
Std Dev 3.701
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch13, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 55.24
Std Dev 7.964
Entry
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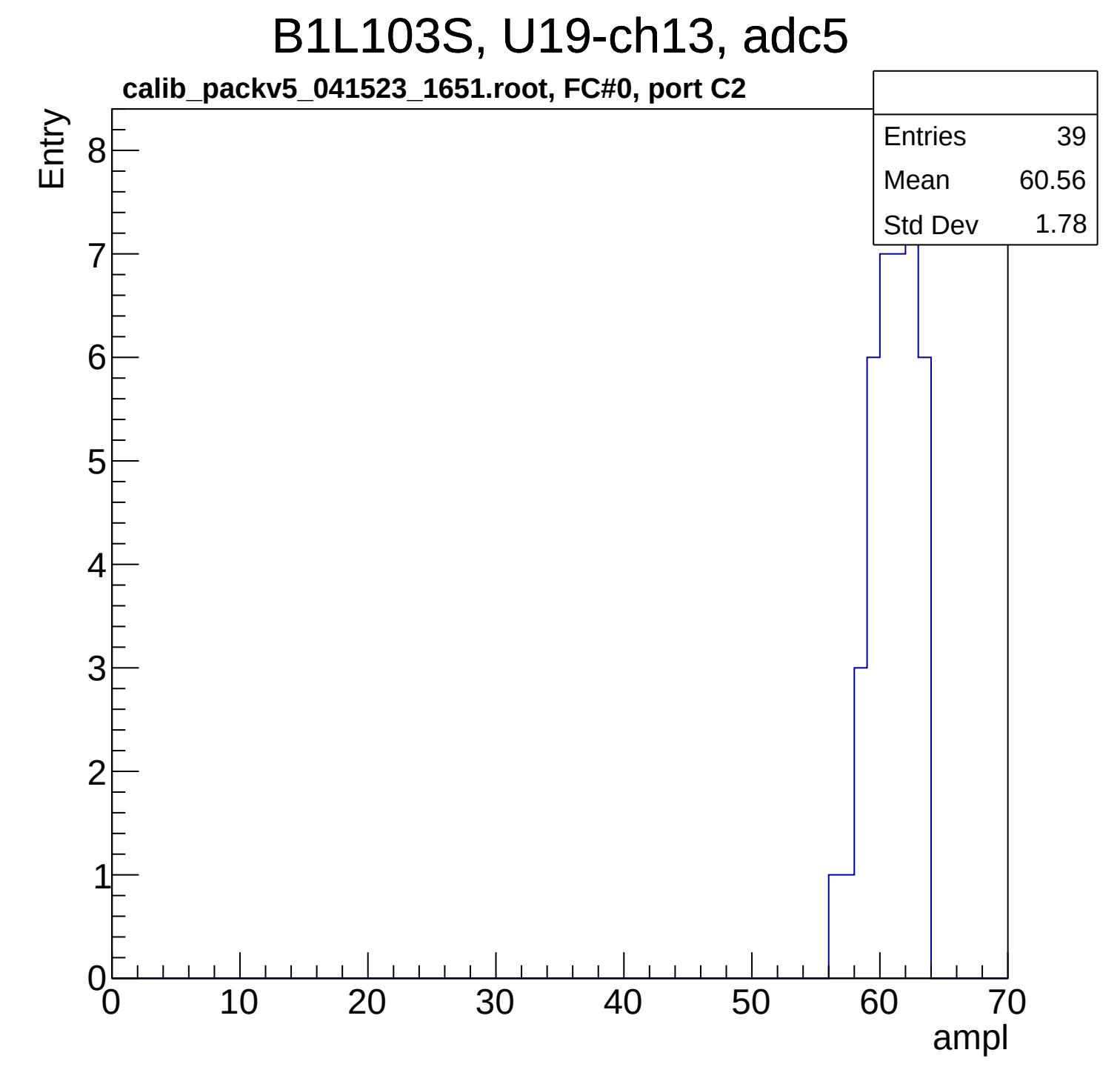
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch13, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 60.56
Std Dev 1.78
Entry
ampl
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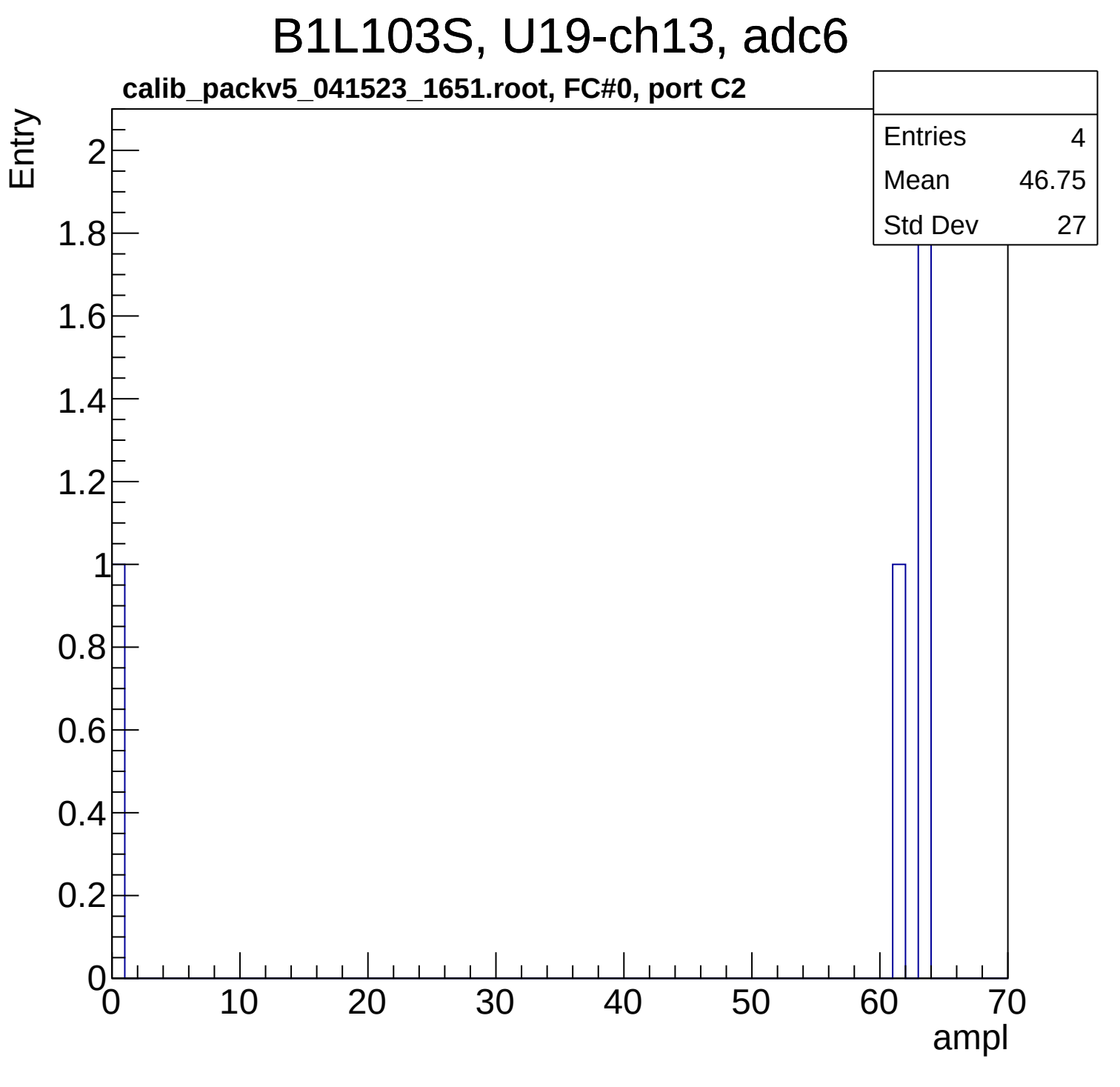
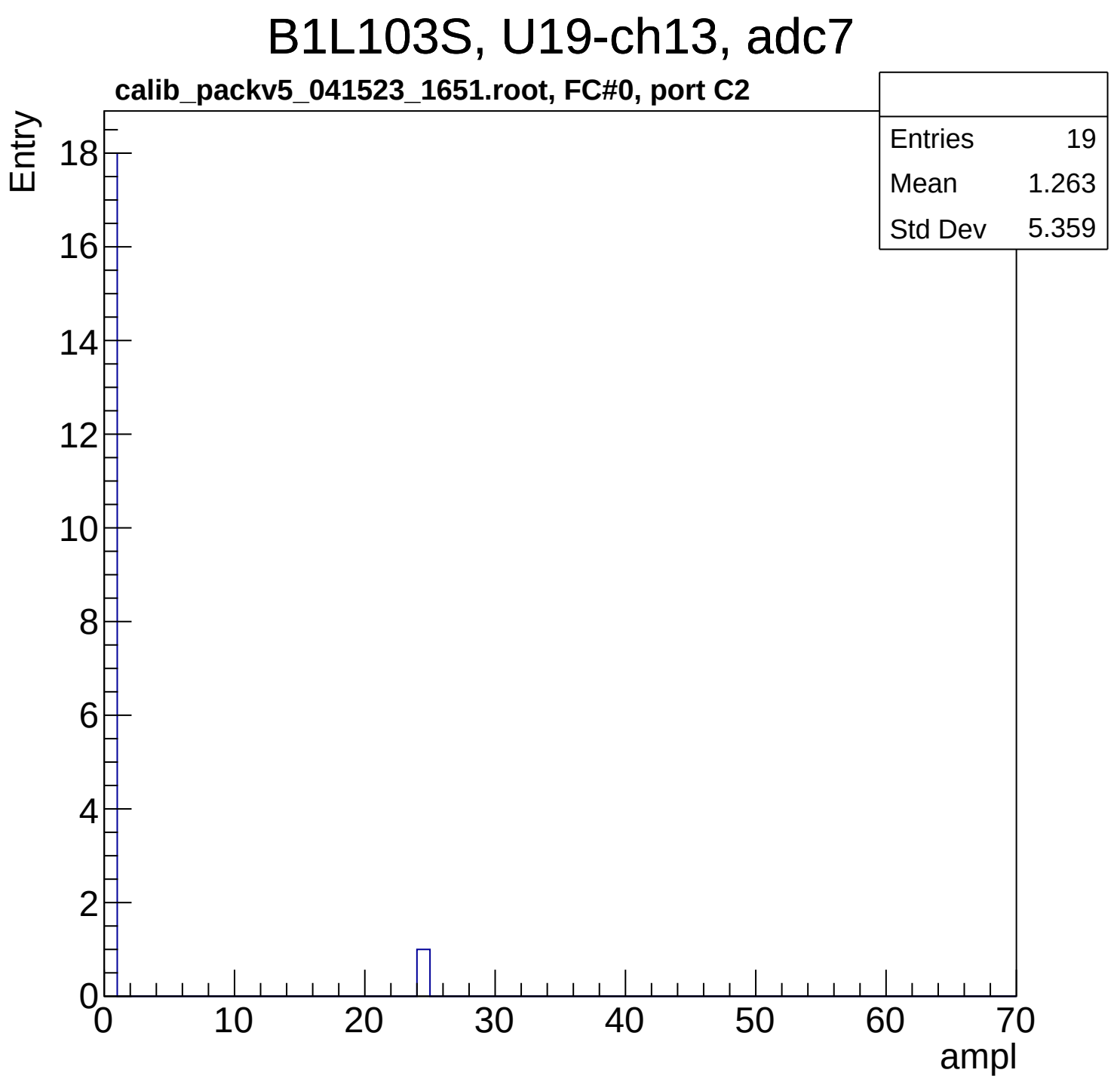
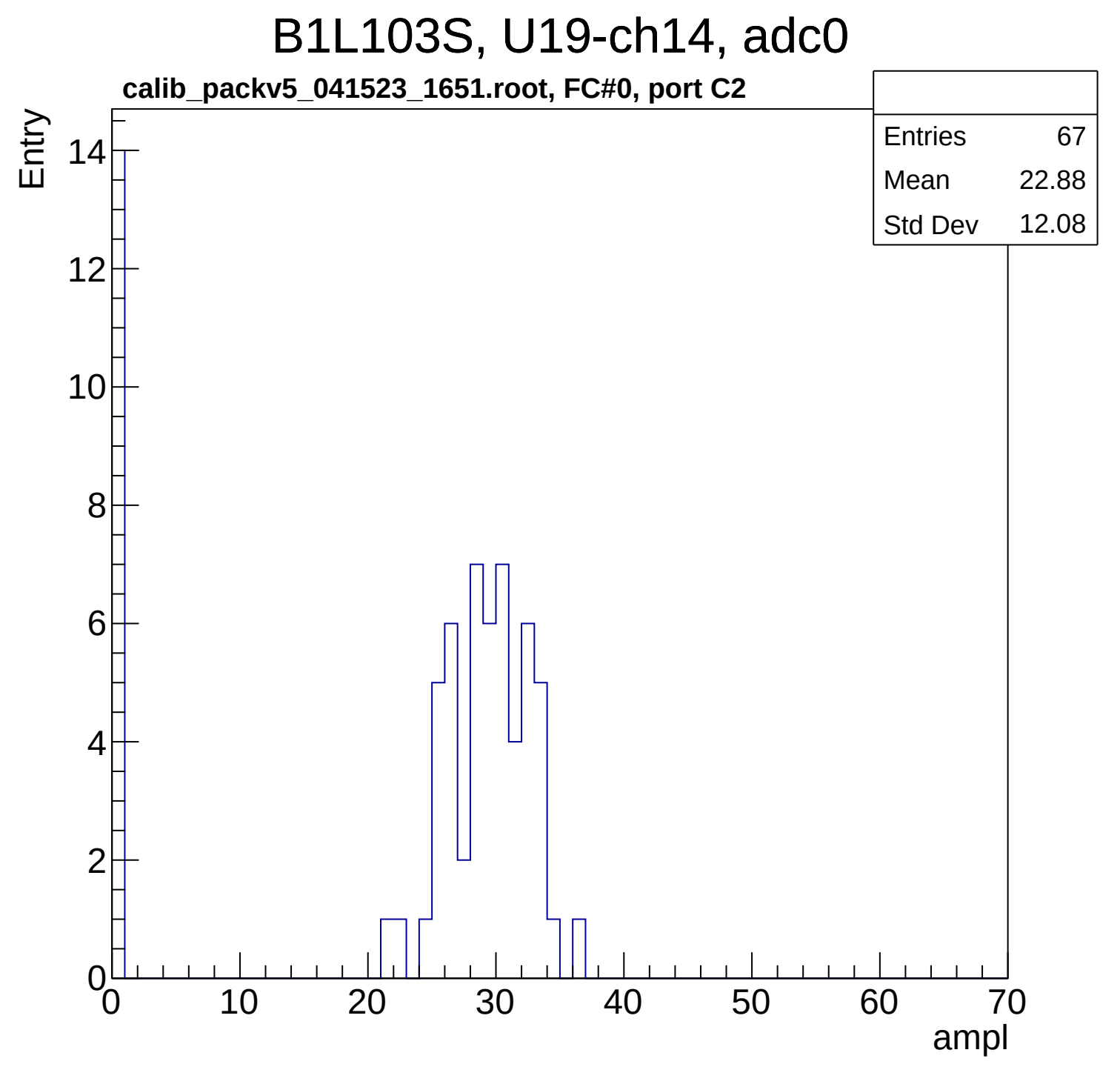
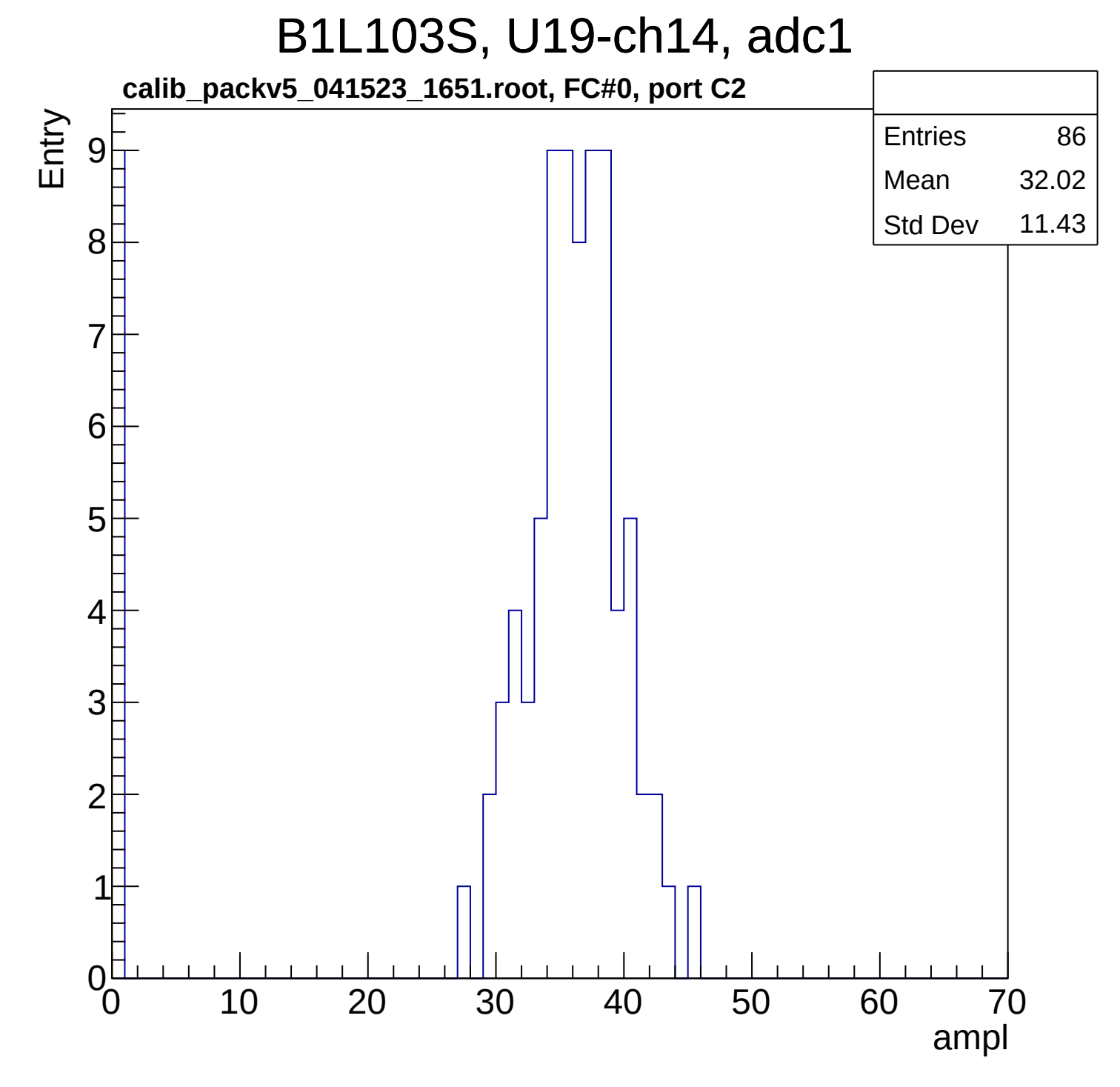
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch13, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 46.75
Std Dev 27
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U19-ch13, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.263
Std Dev 5.359
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch14, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 22.88
Std Dev 12.08
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch14, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 32.02
Std Dev 11.43
Entry
ampl
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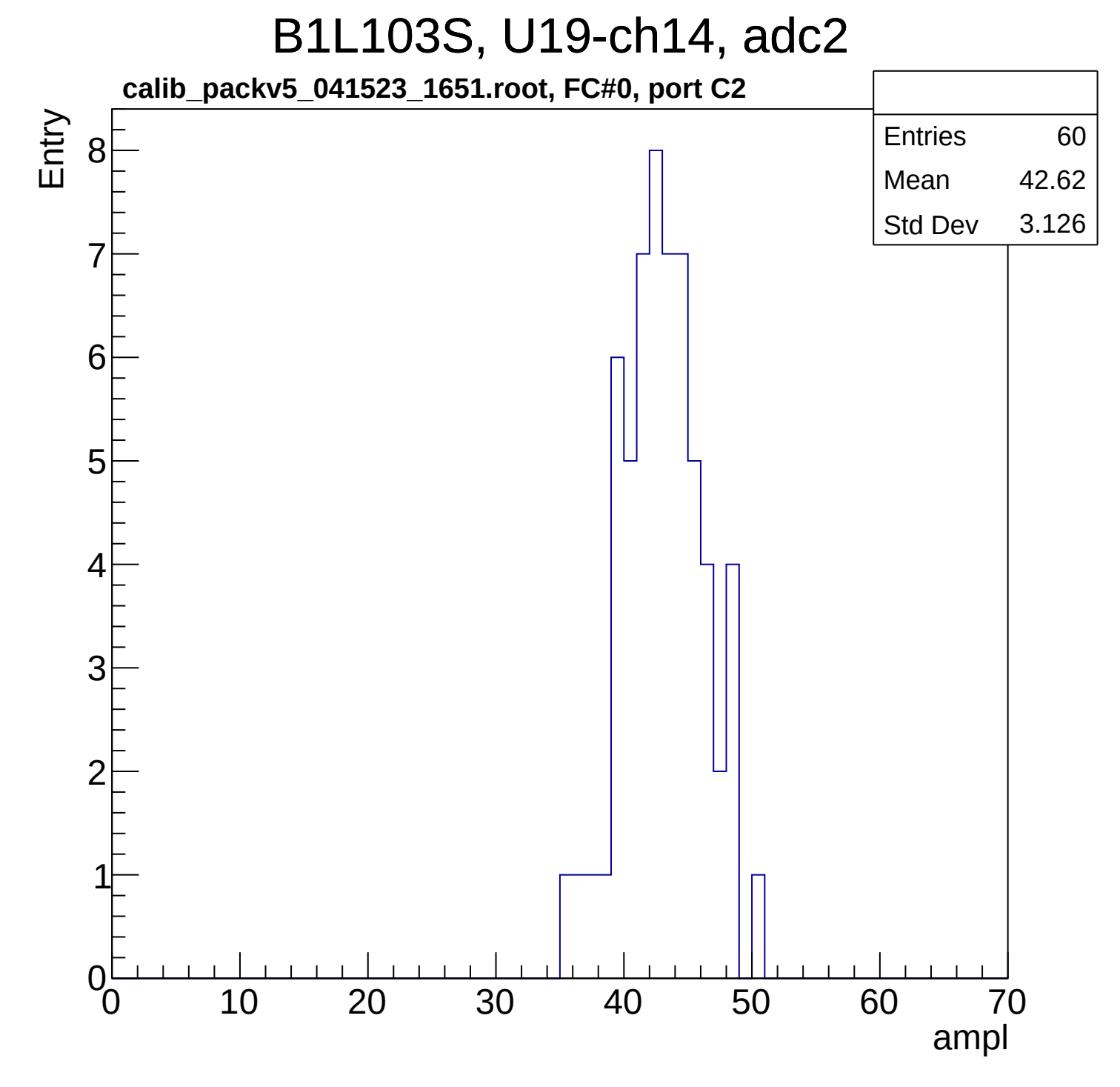
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch14, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 42.62
Std Dev 3.126
Entry
ampl
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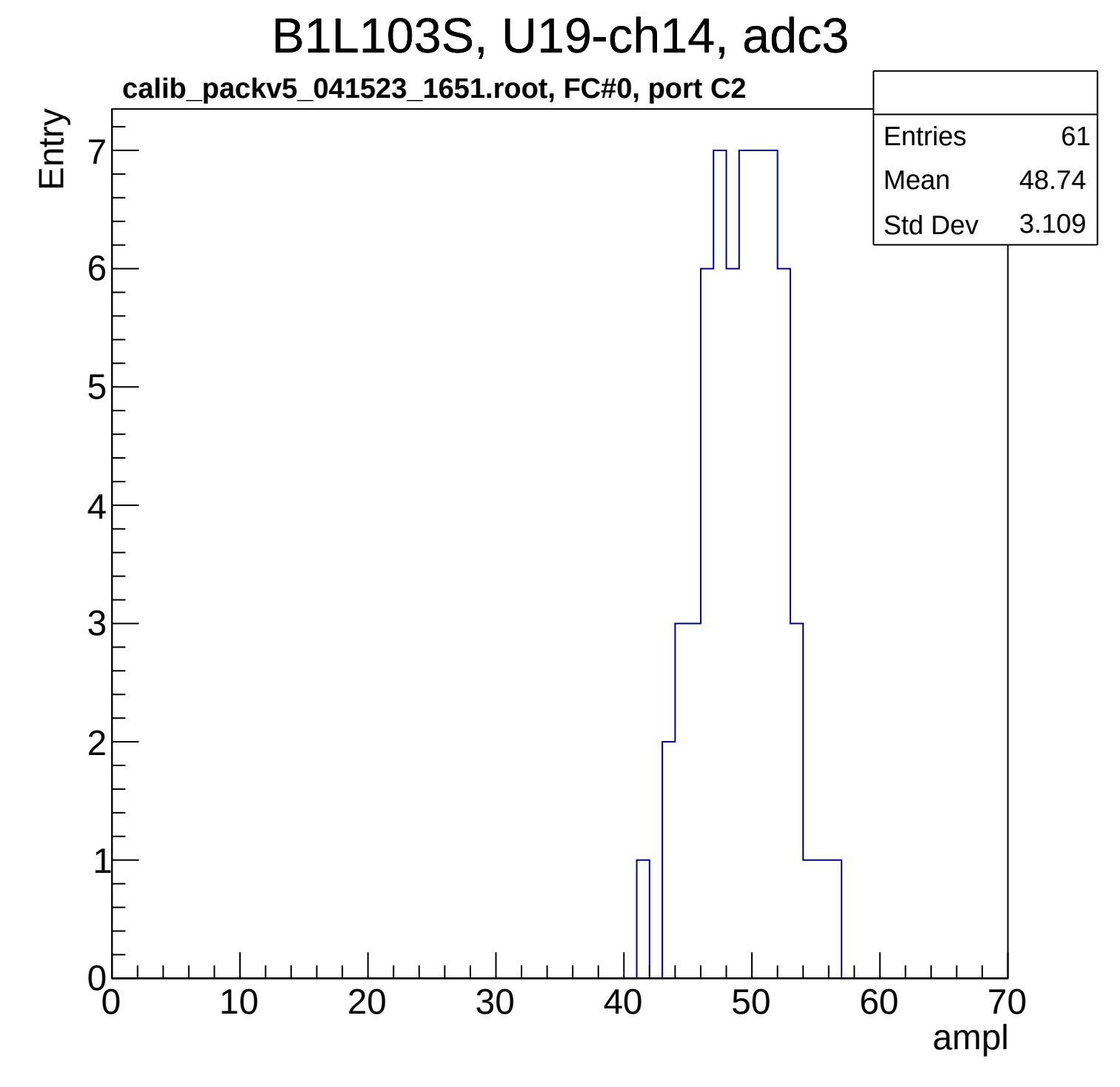
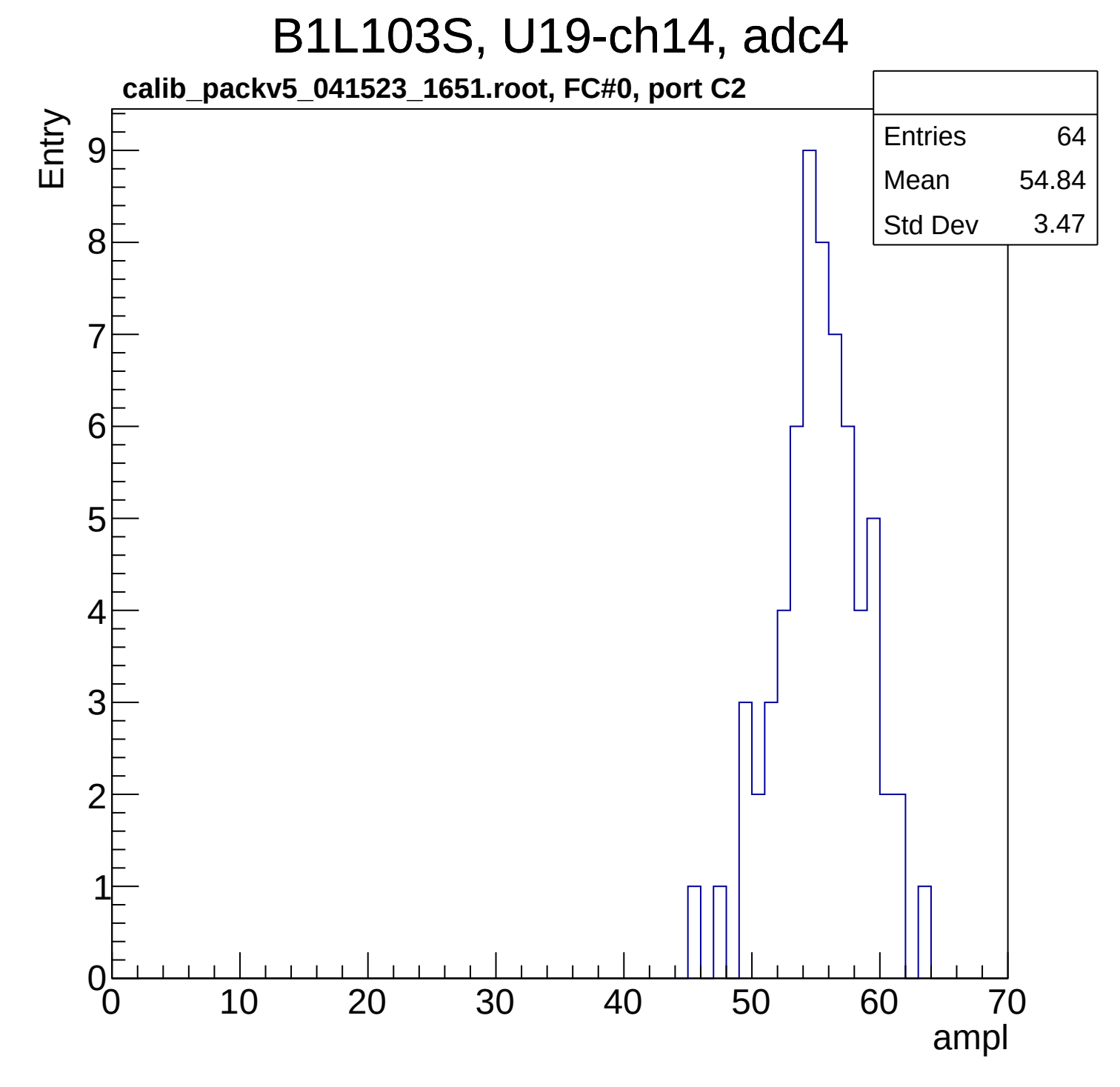
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch14, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 48.74
Std Dev 3.109
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch14, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 54.84
Std Dev 3.47
Entry
ampl
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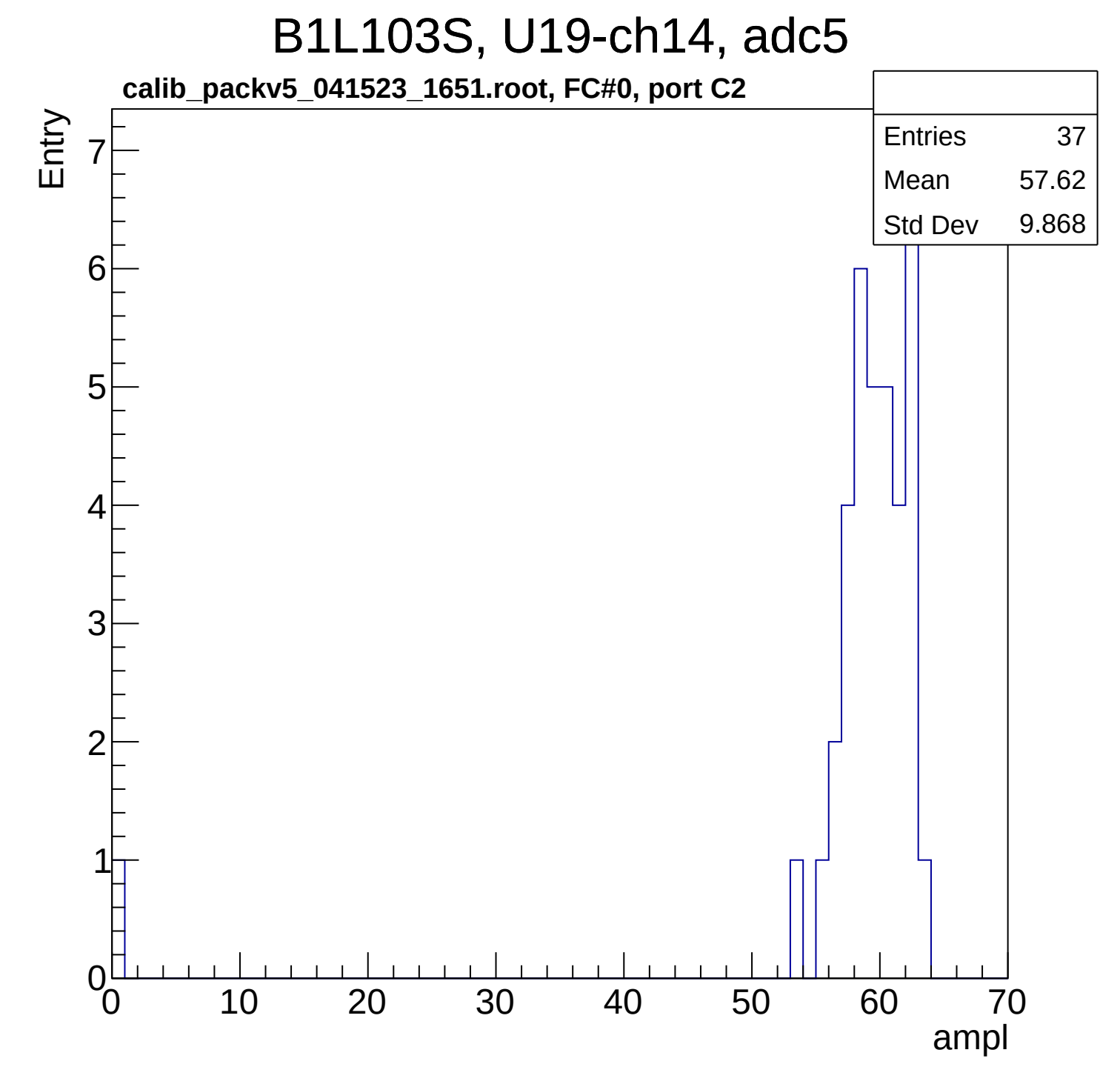
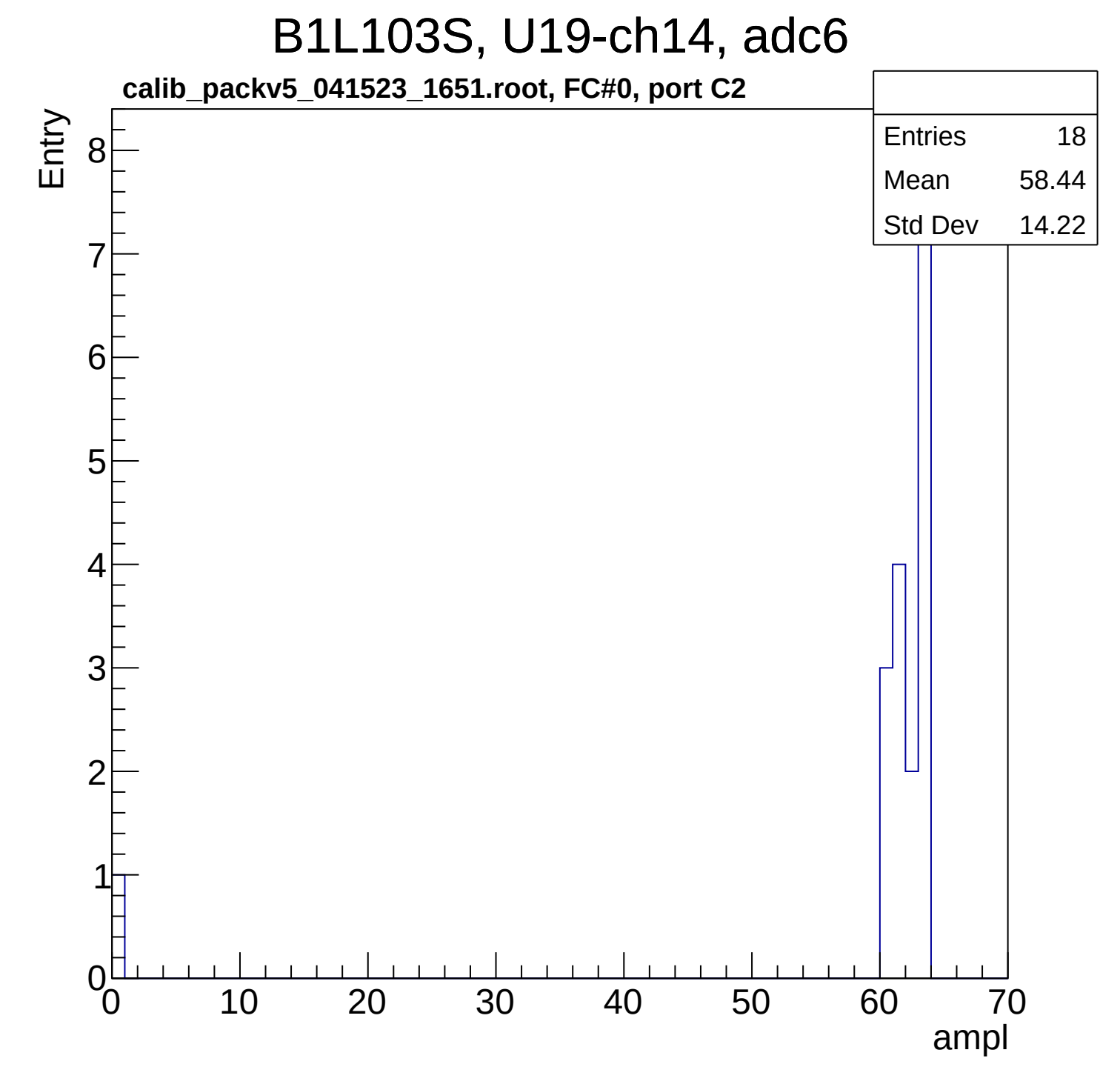
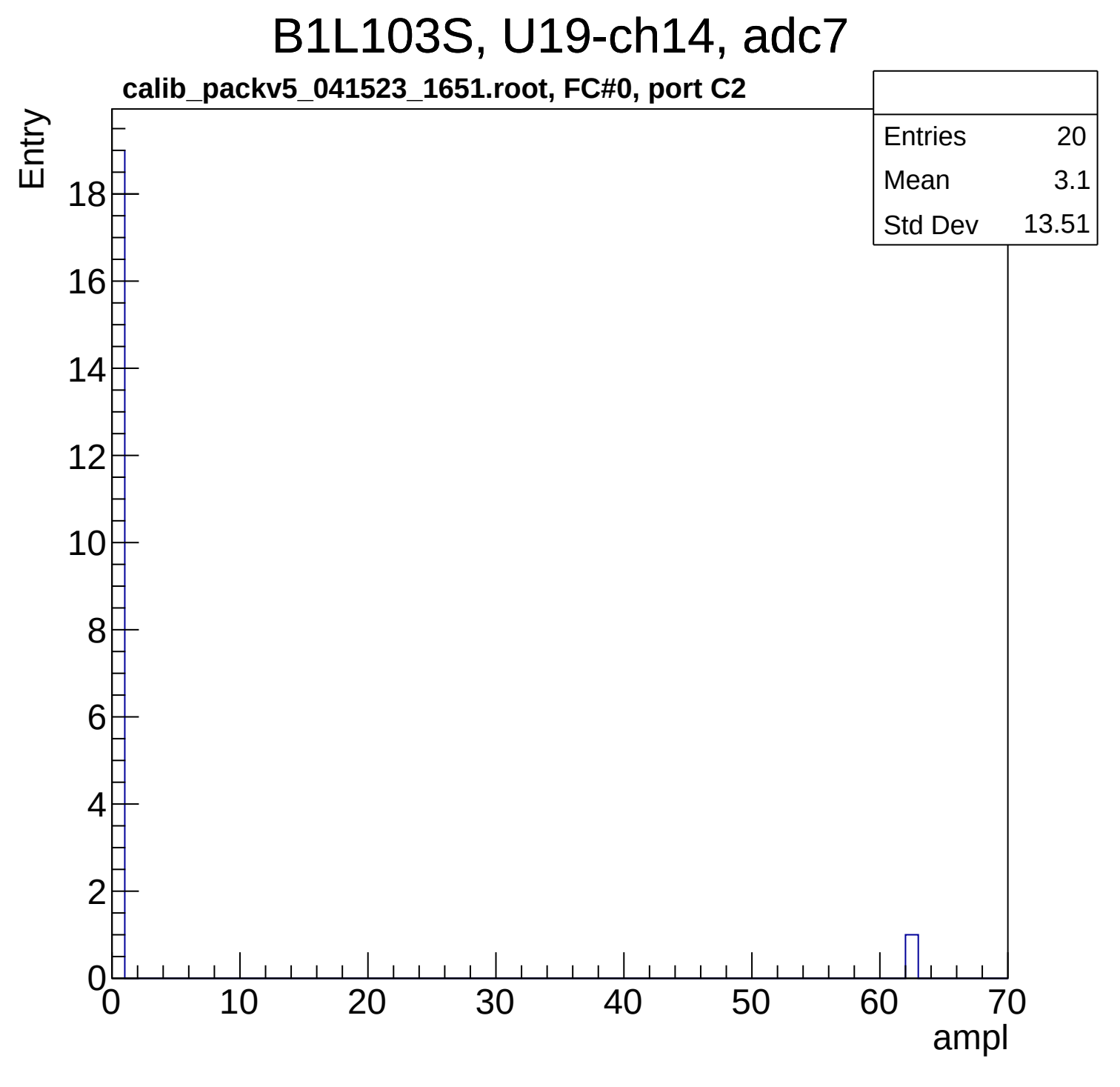
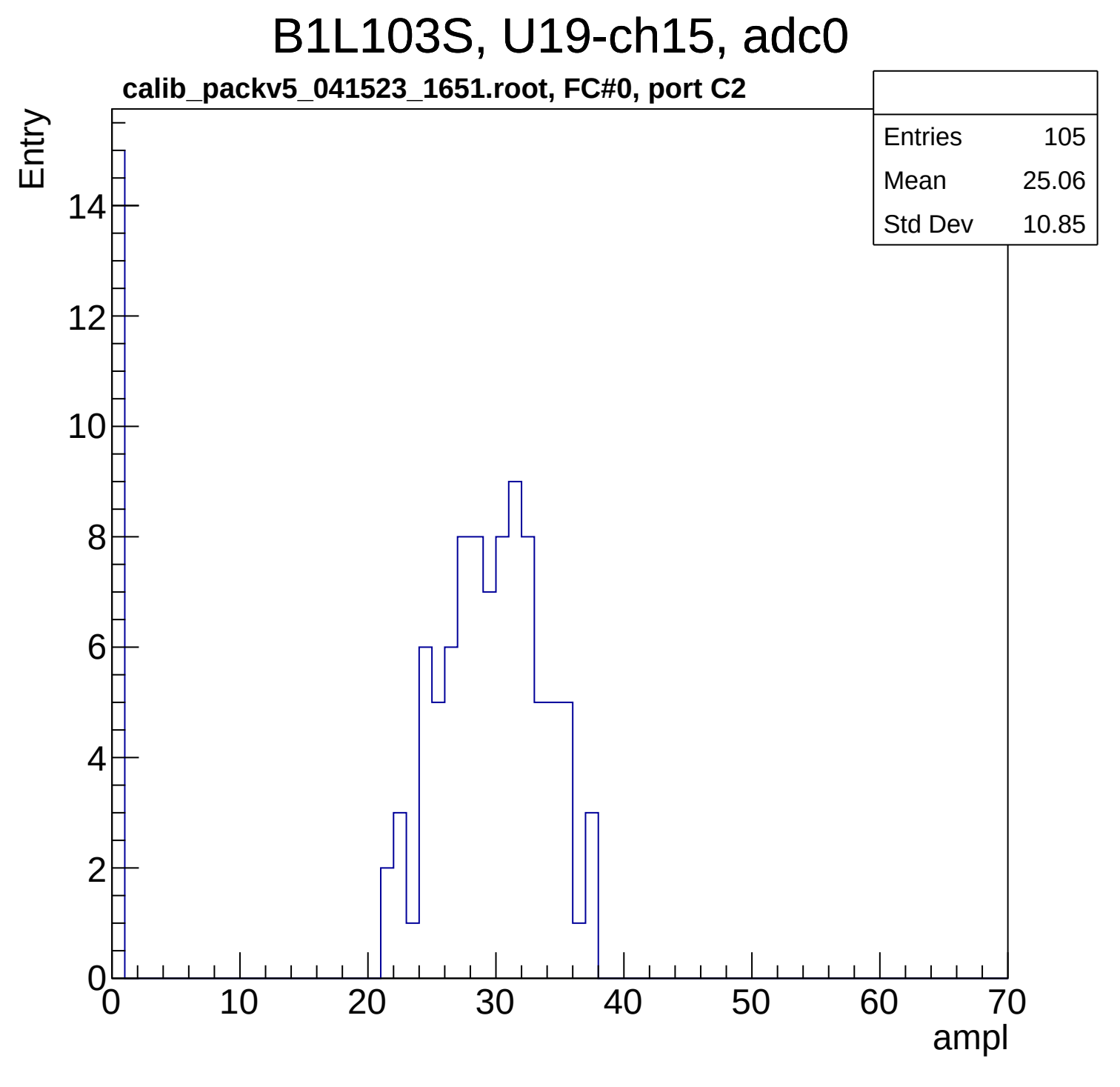
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch14, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 57.62
Std Dev 9.868
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch14, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 58.44
Std Dev 14.22
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch14, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch15, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 105
Mean 25.06
Std Dev 10.85
Entry
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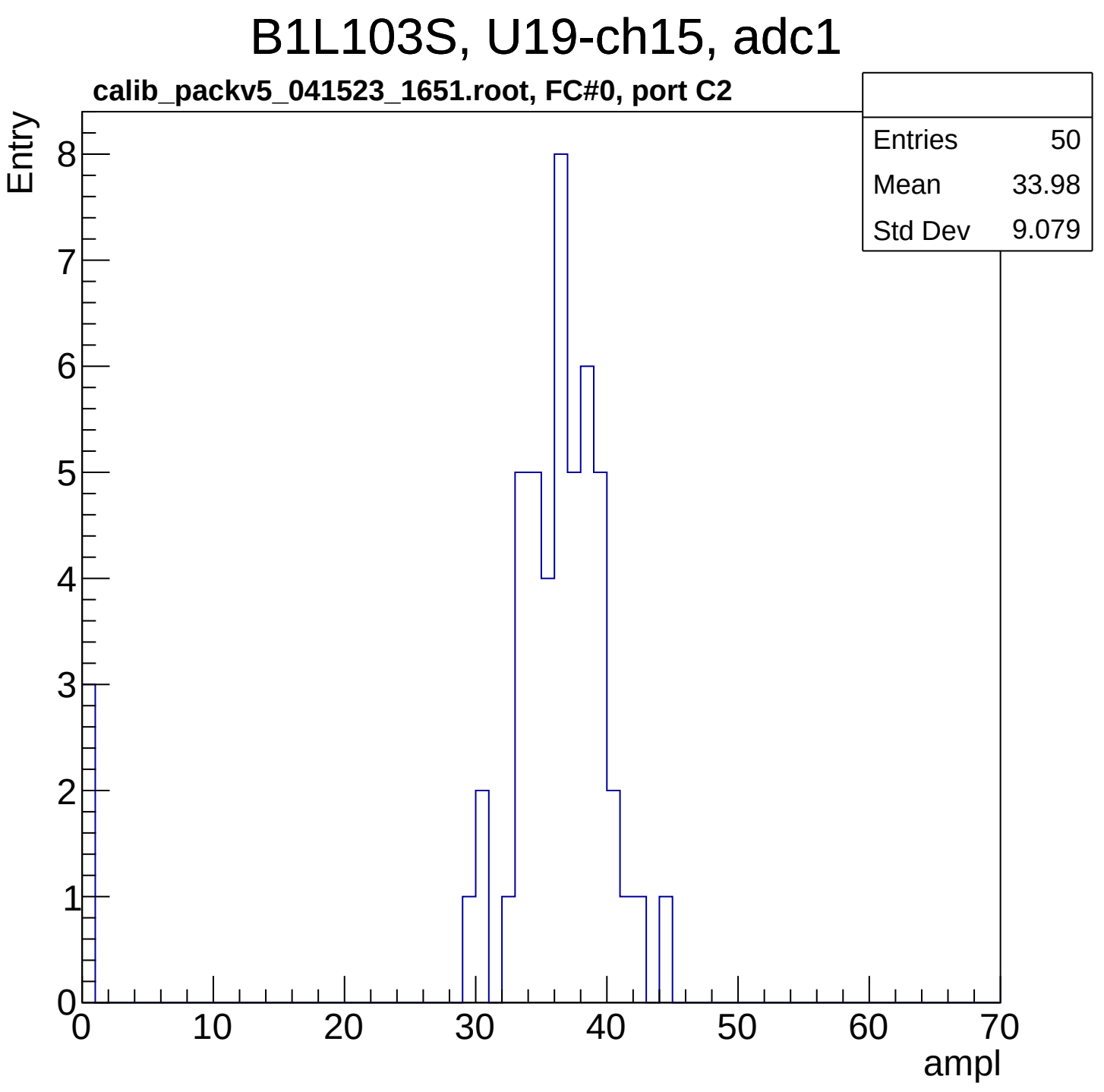
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch15, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 33.98
Std Dev 9.079
Entry
ampl
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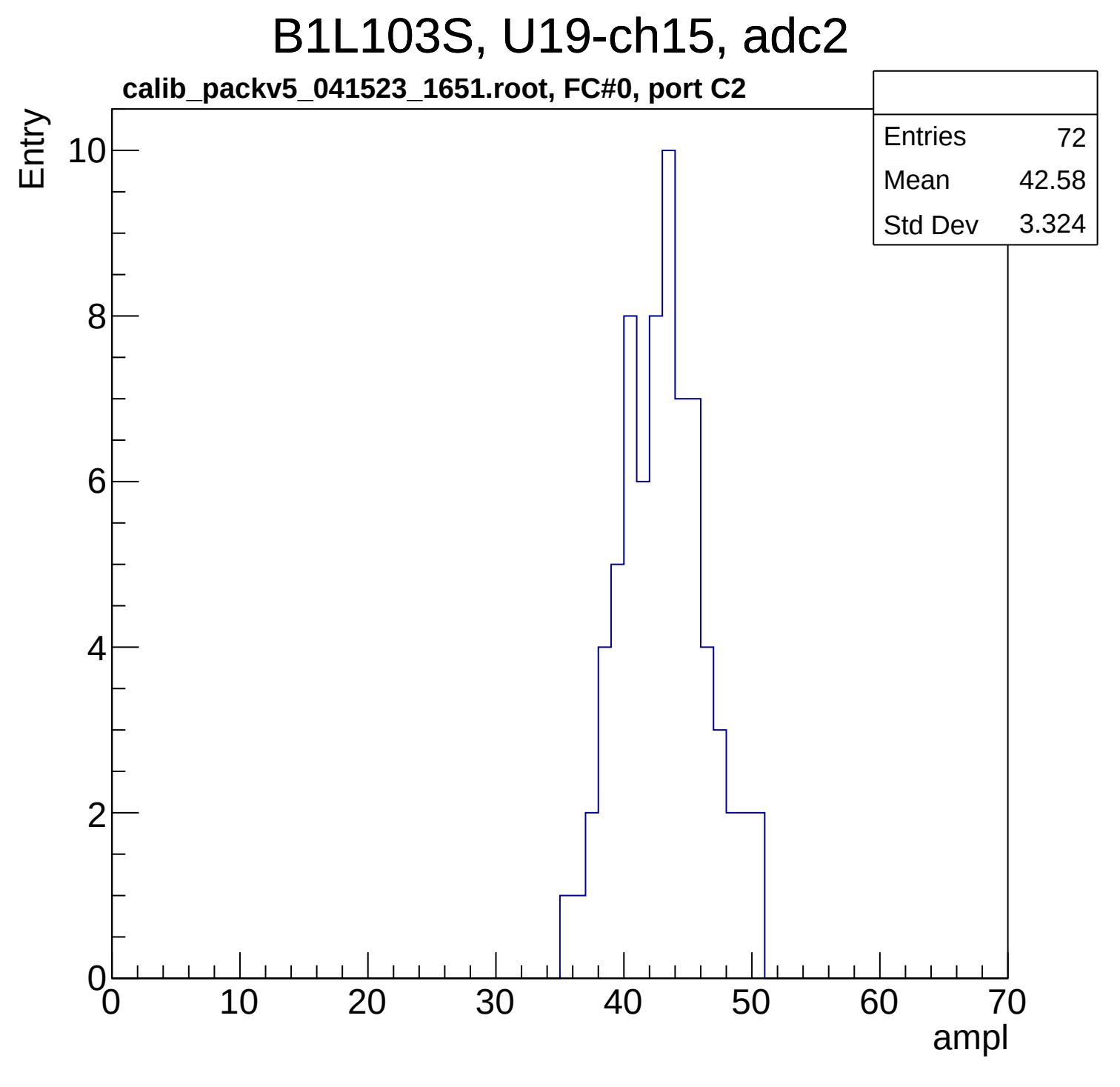
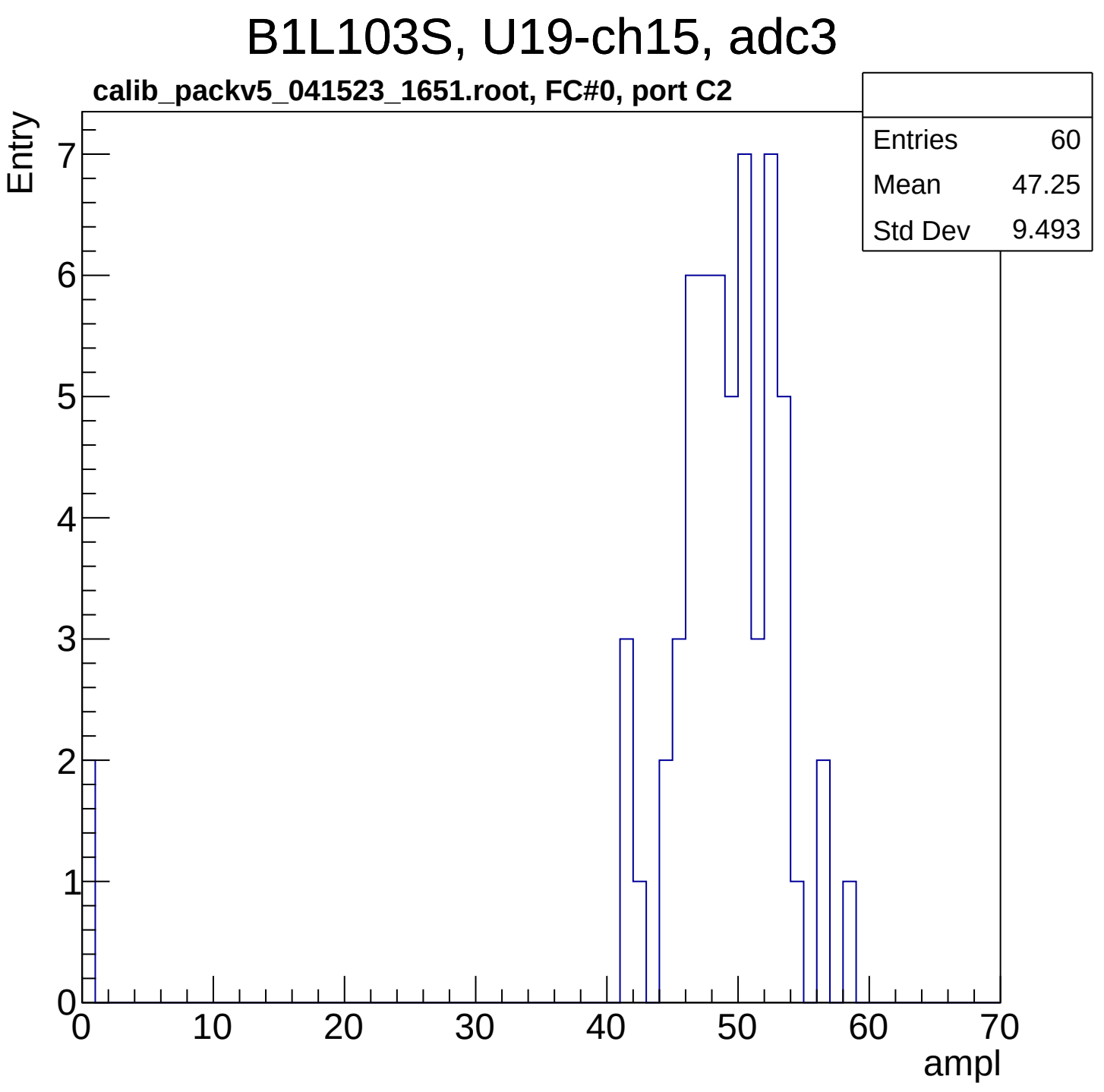
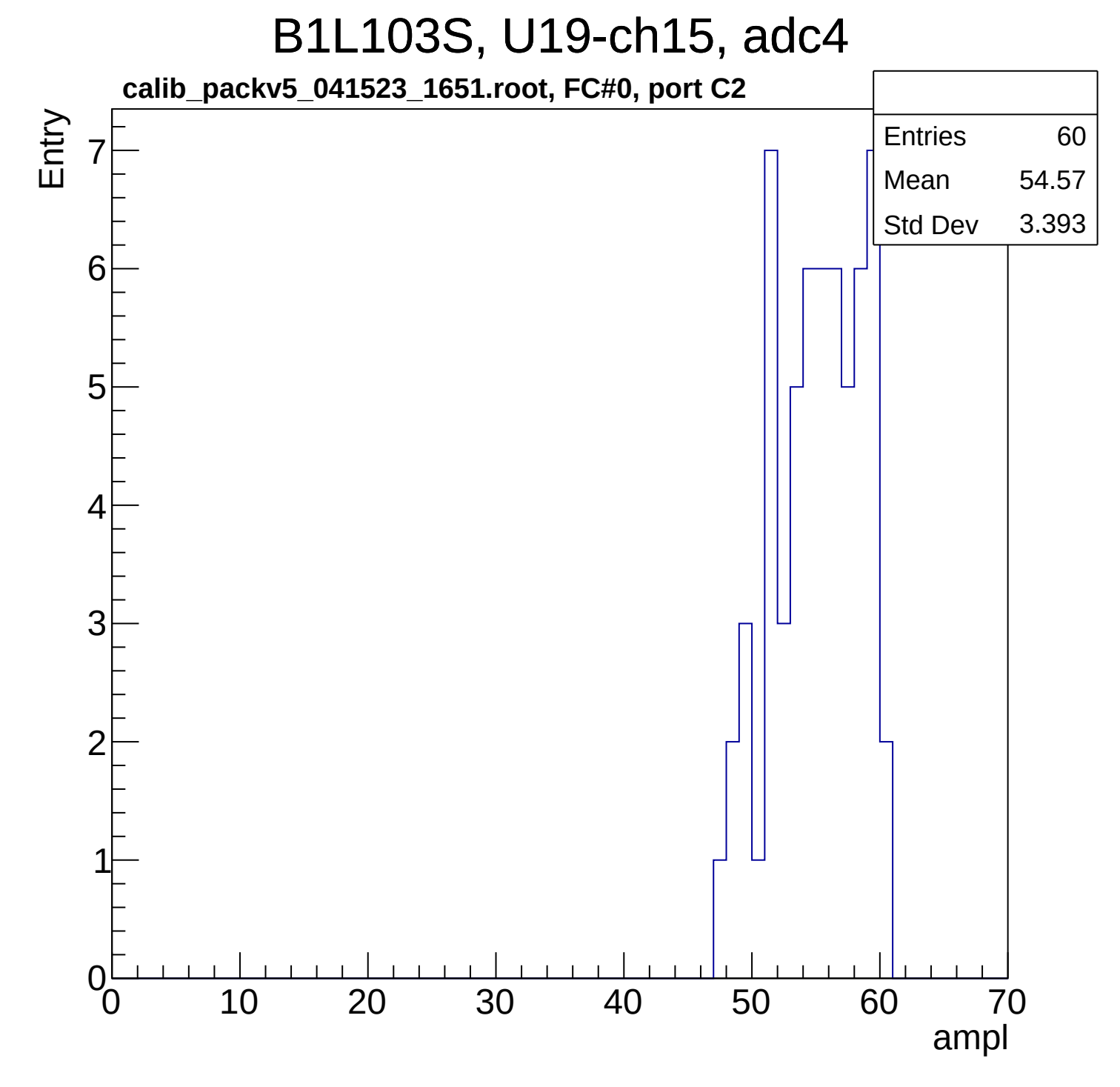
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch15, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 42.58
Std Dev 3.324
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U19-ch15, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 47.25
Std Dev 9.493
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch15, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 54.57
Std Dev 3.393
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
30
40
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60
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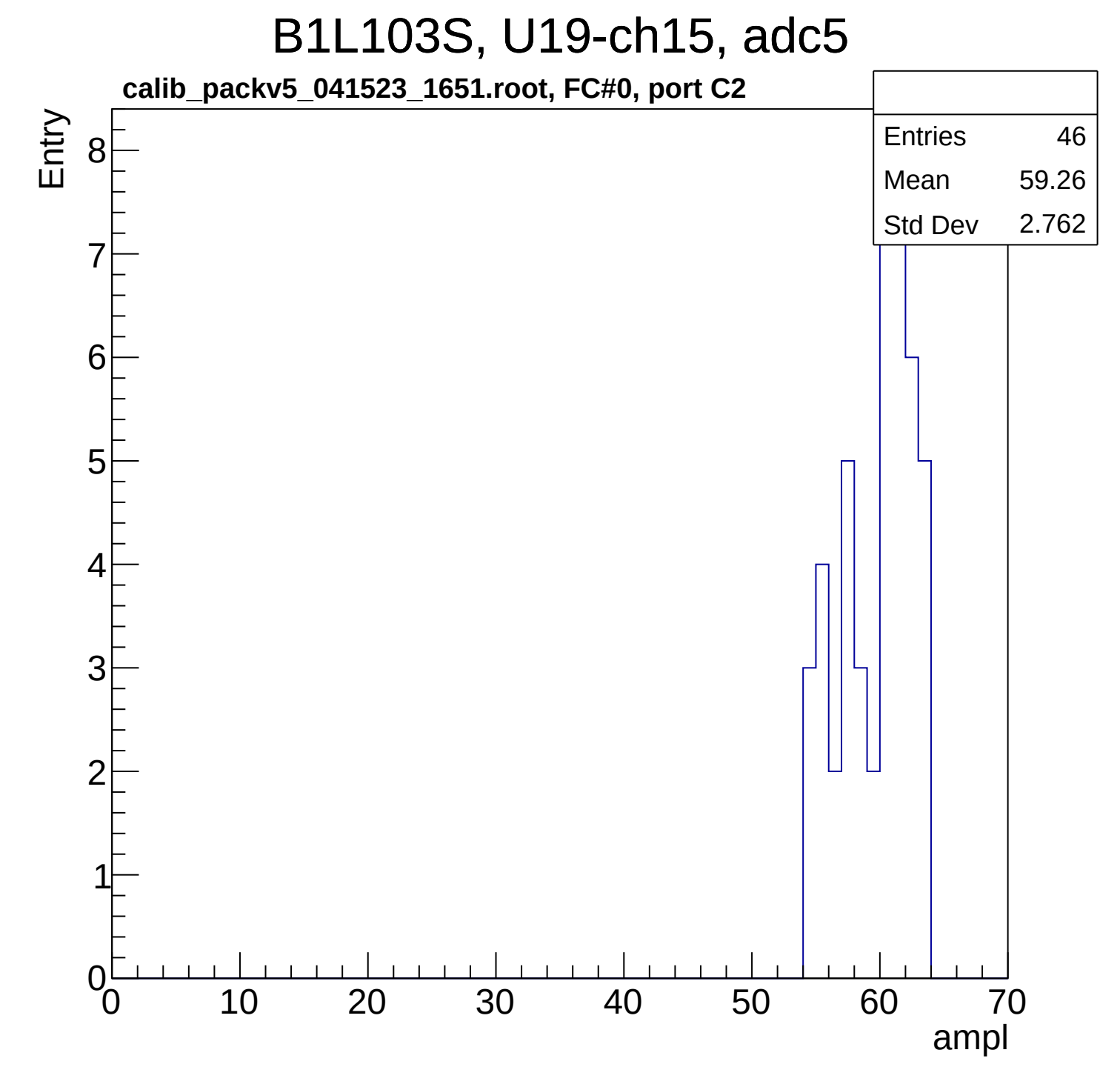
B1L103S, U19-ch15, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 59.26
Std Dev 2.762
Entry
ampl
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2
3
4
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6
7
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0
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40
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60
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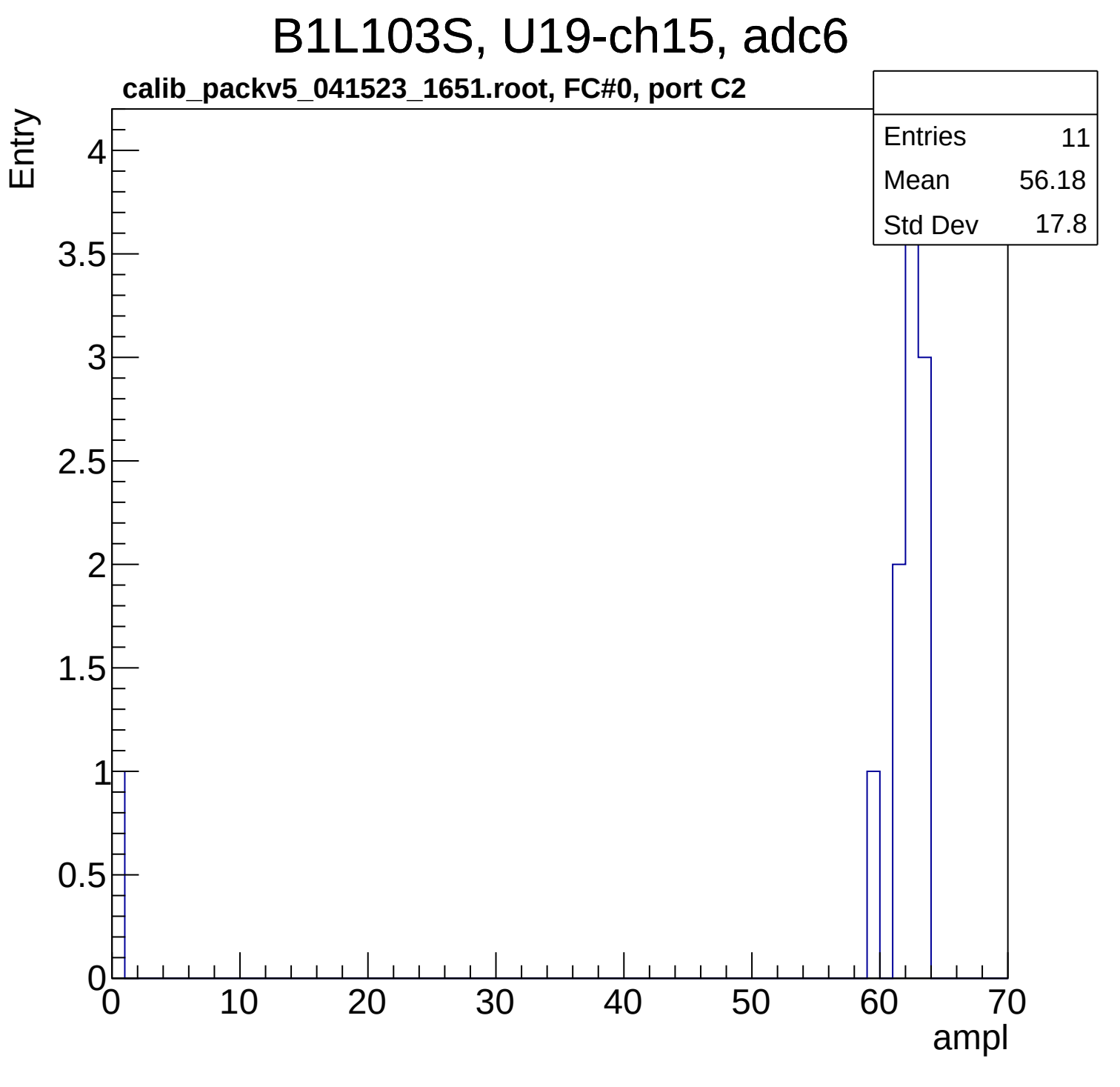
B1L103S, U19-ch15, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 56.18
Std Dev 17.8
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
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60
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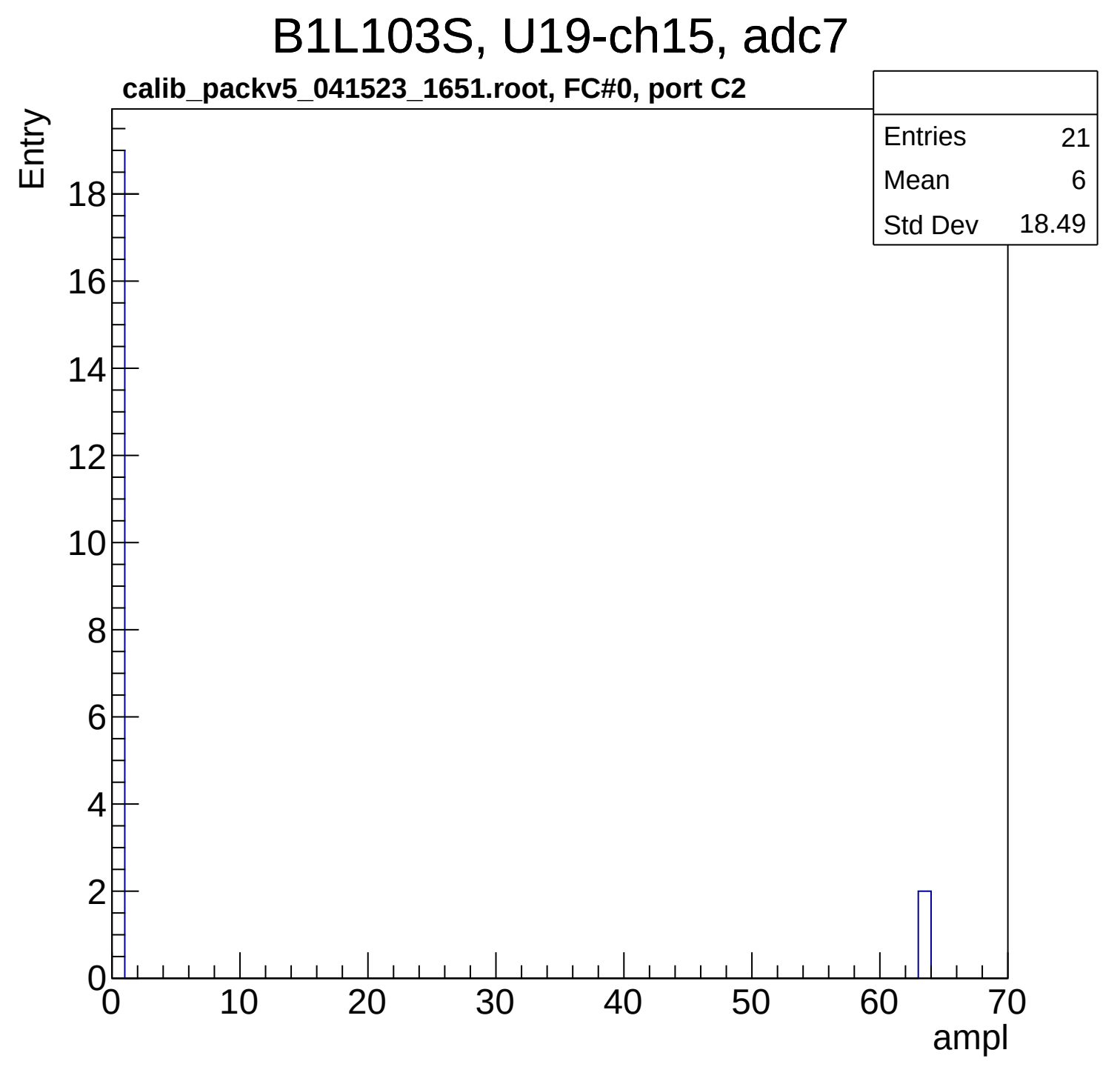
B1L103S, U19-ch15, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 6
Std Dev 18.49
Entry
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6
8
10
12
14
16
18
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10
20
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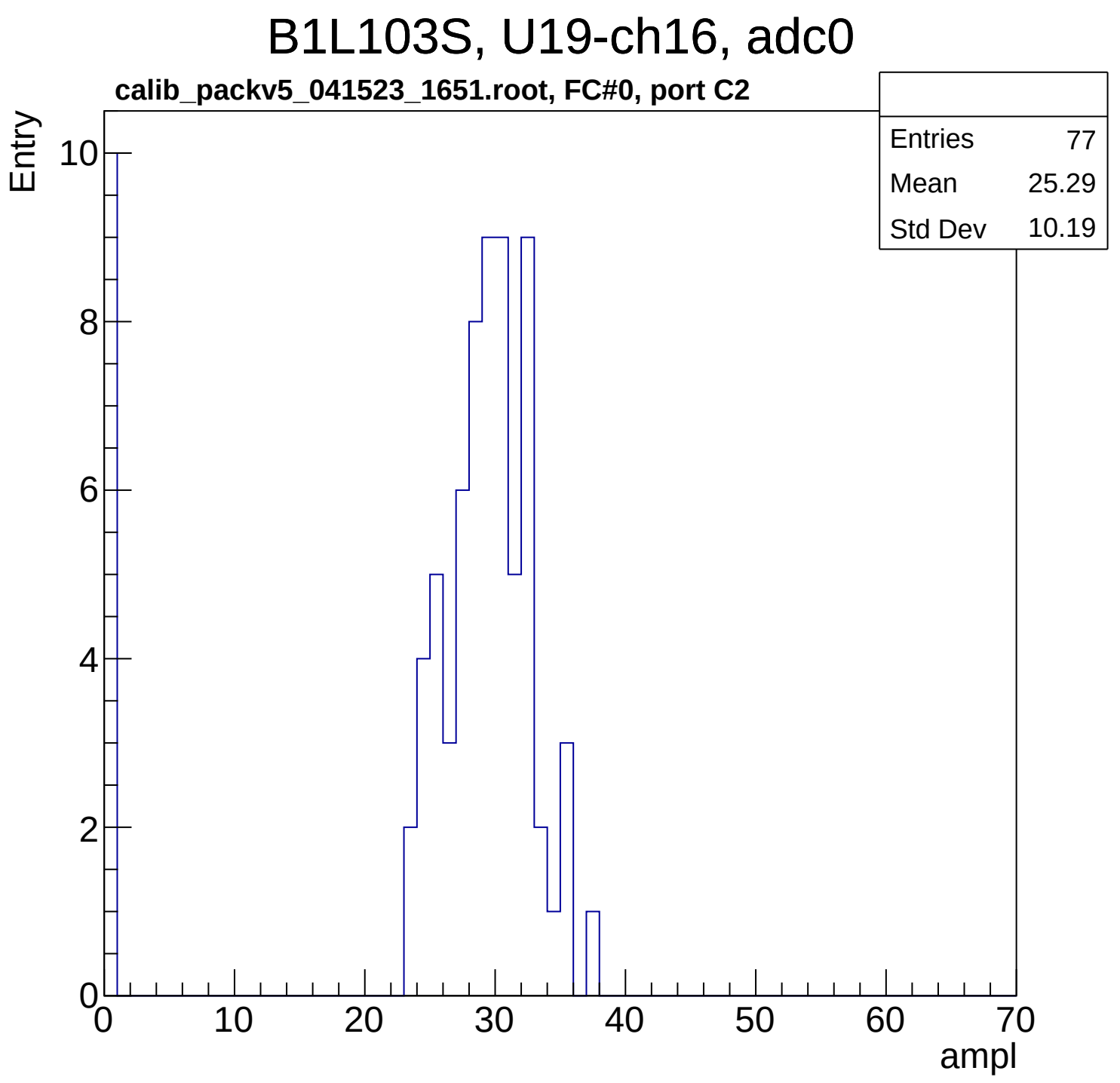
50
60
70
ampl


B1L103S, U19-ch16, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 25.29
Std Dev 10.19
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
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60
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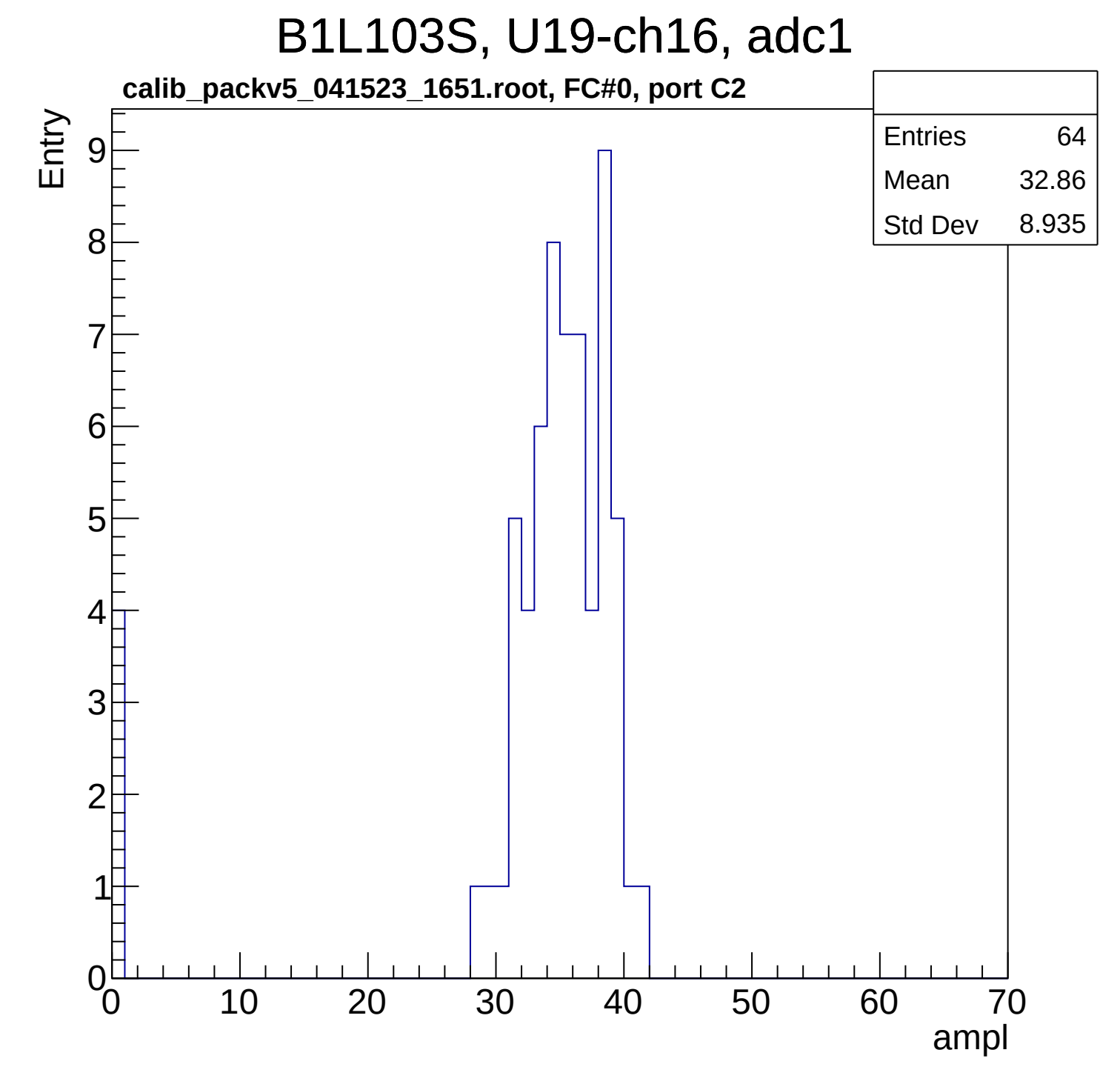
B1L103S, U19-ch16, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 32.86
Std Dev 8.935
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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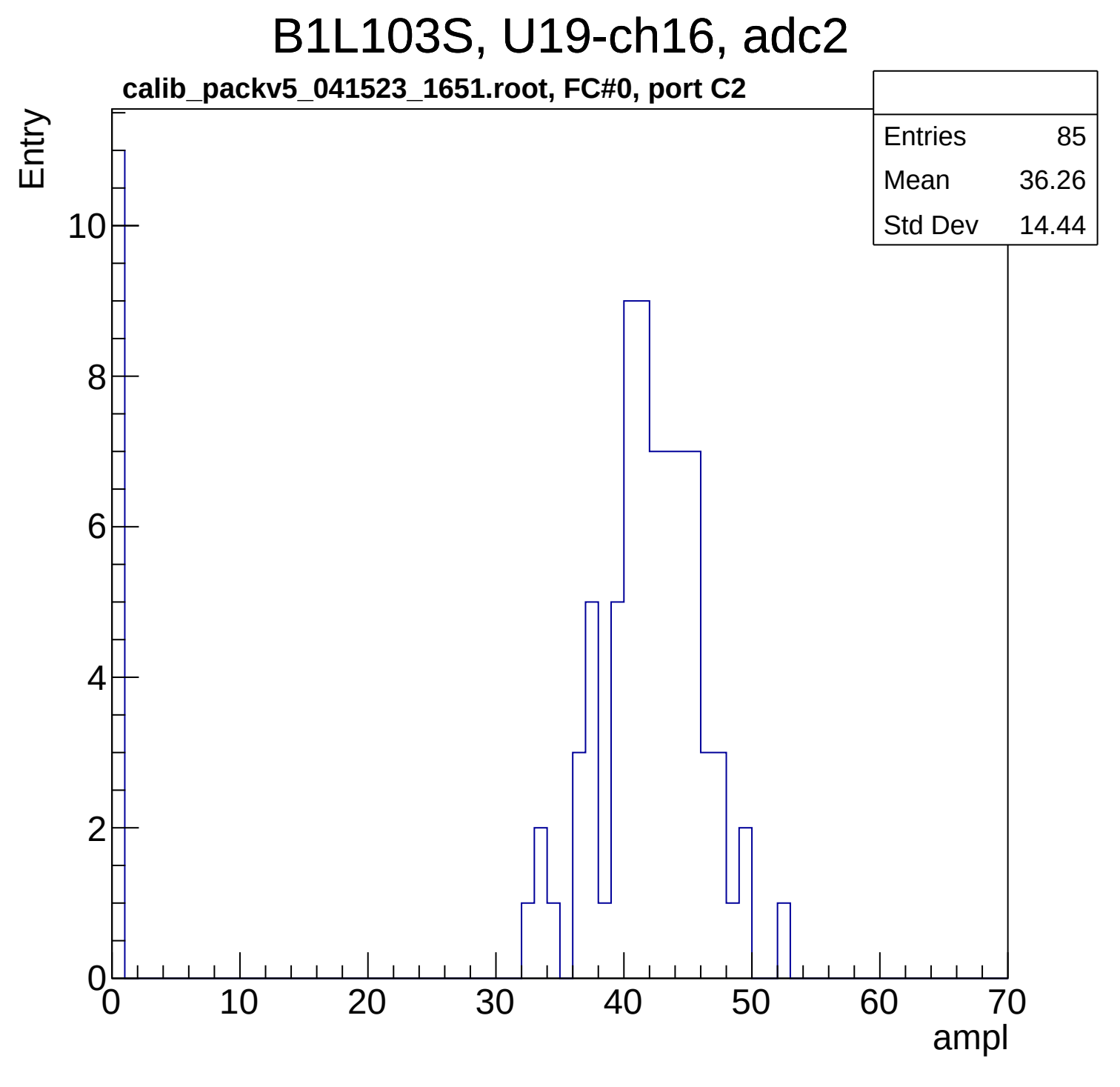
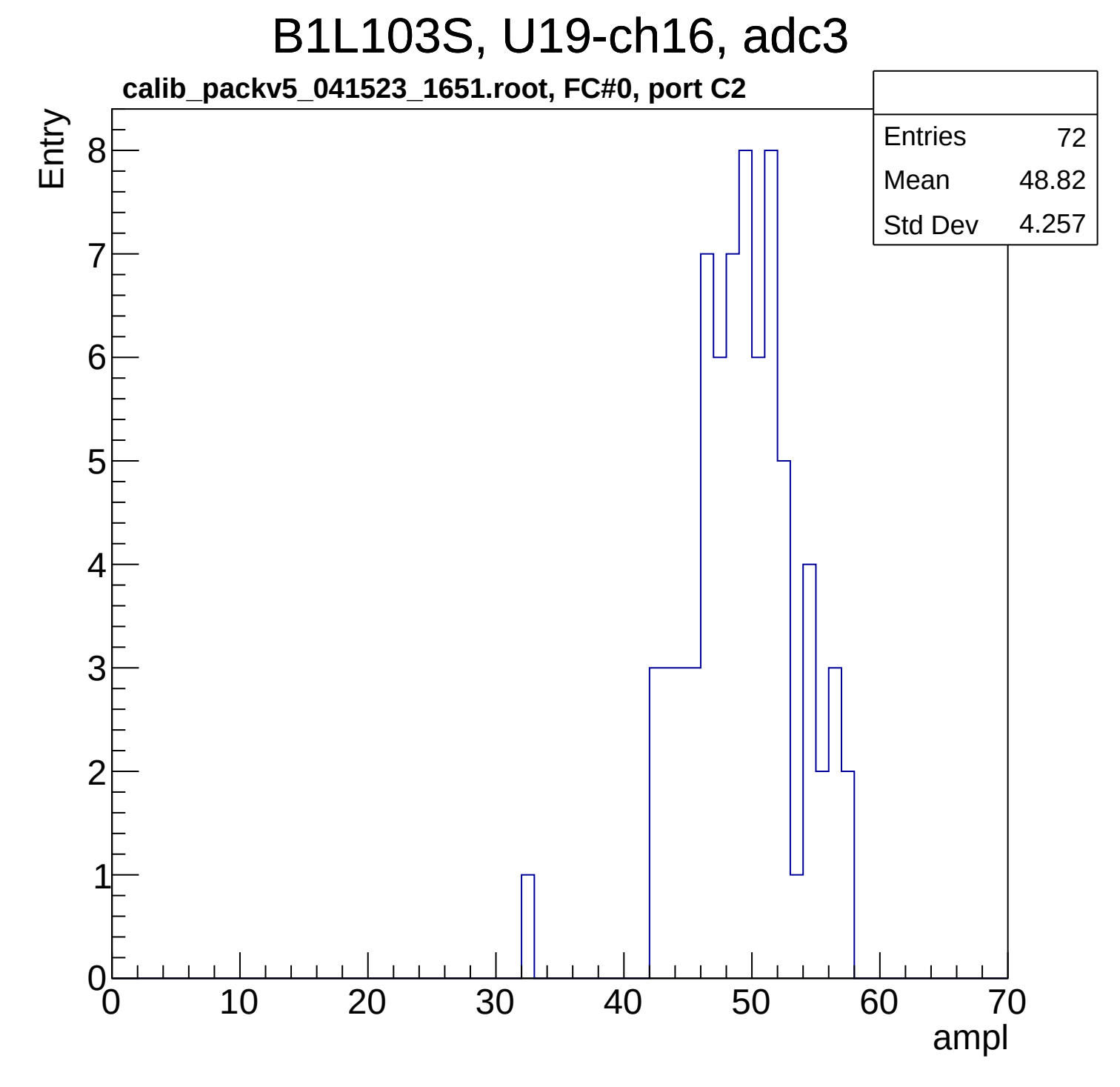

B1L103S, U19-ch16, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 36.26
Std Dev 14.44
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch16, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 48.82
Std Dev 4.257
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
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60
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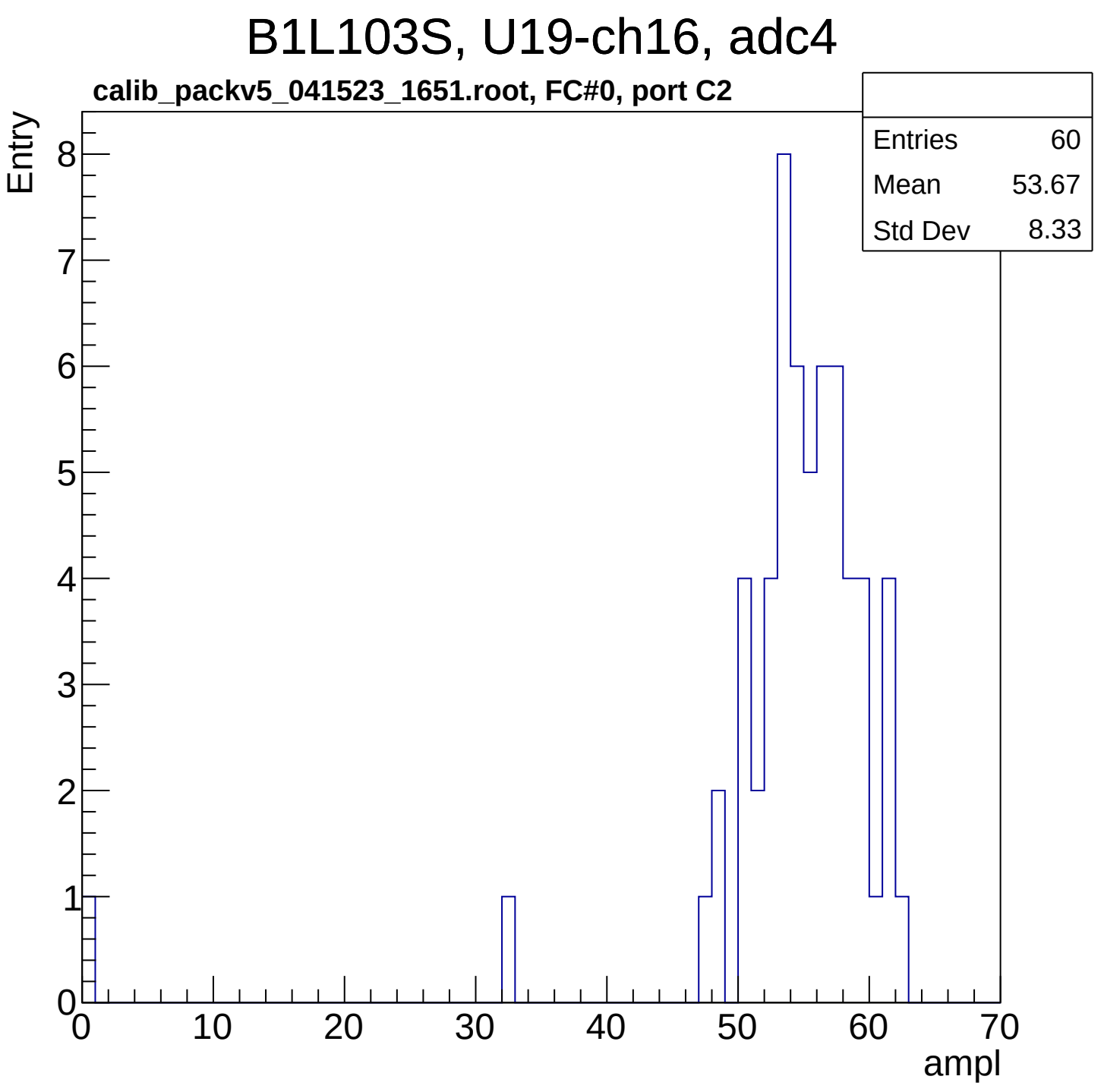
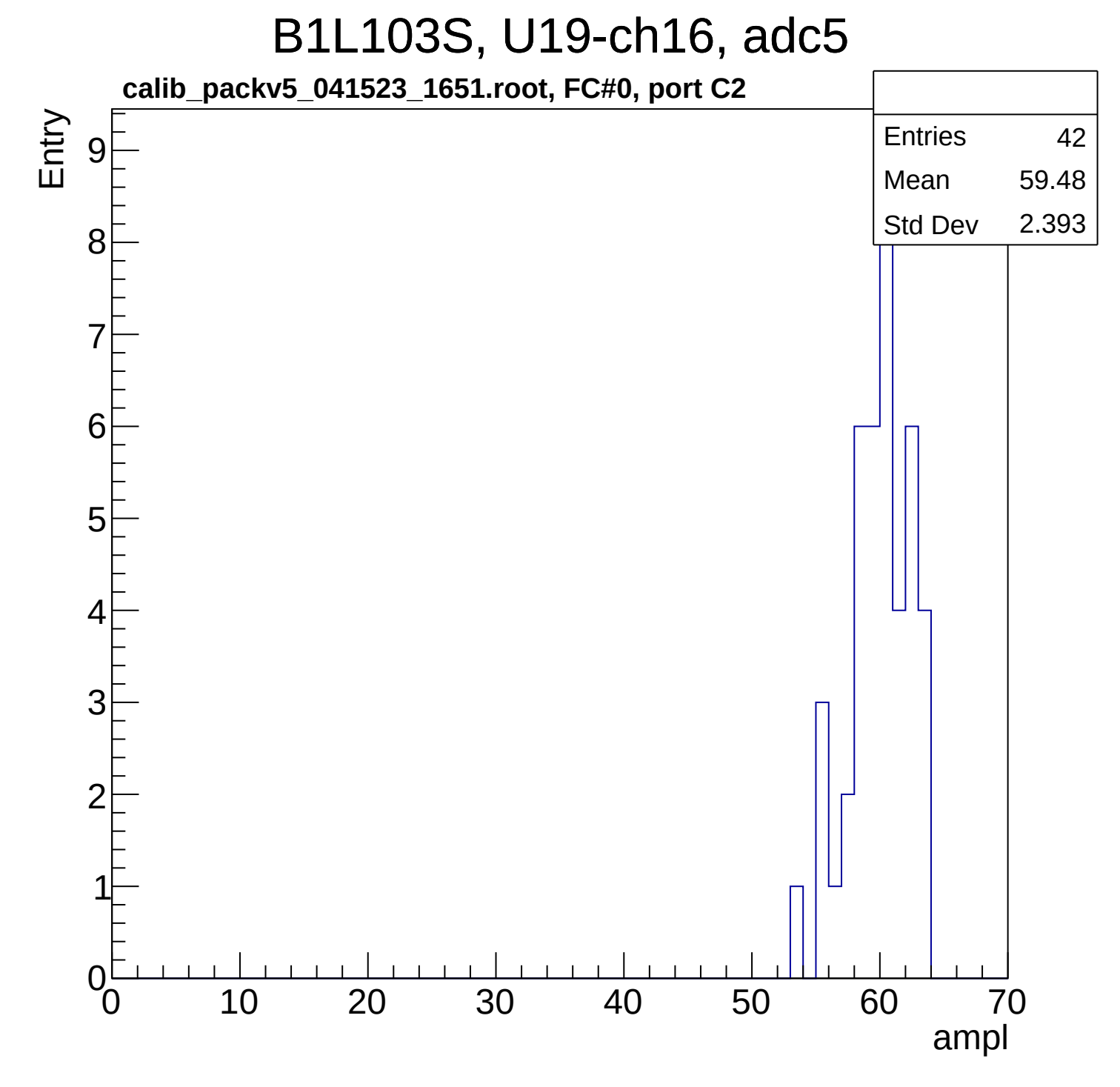
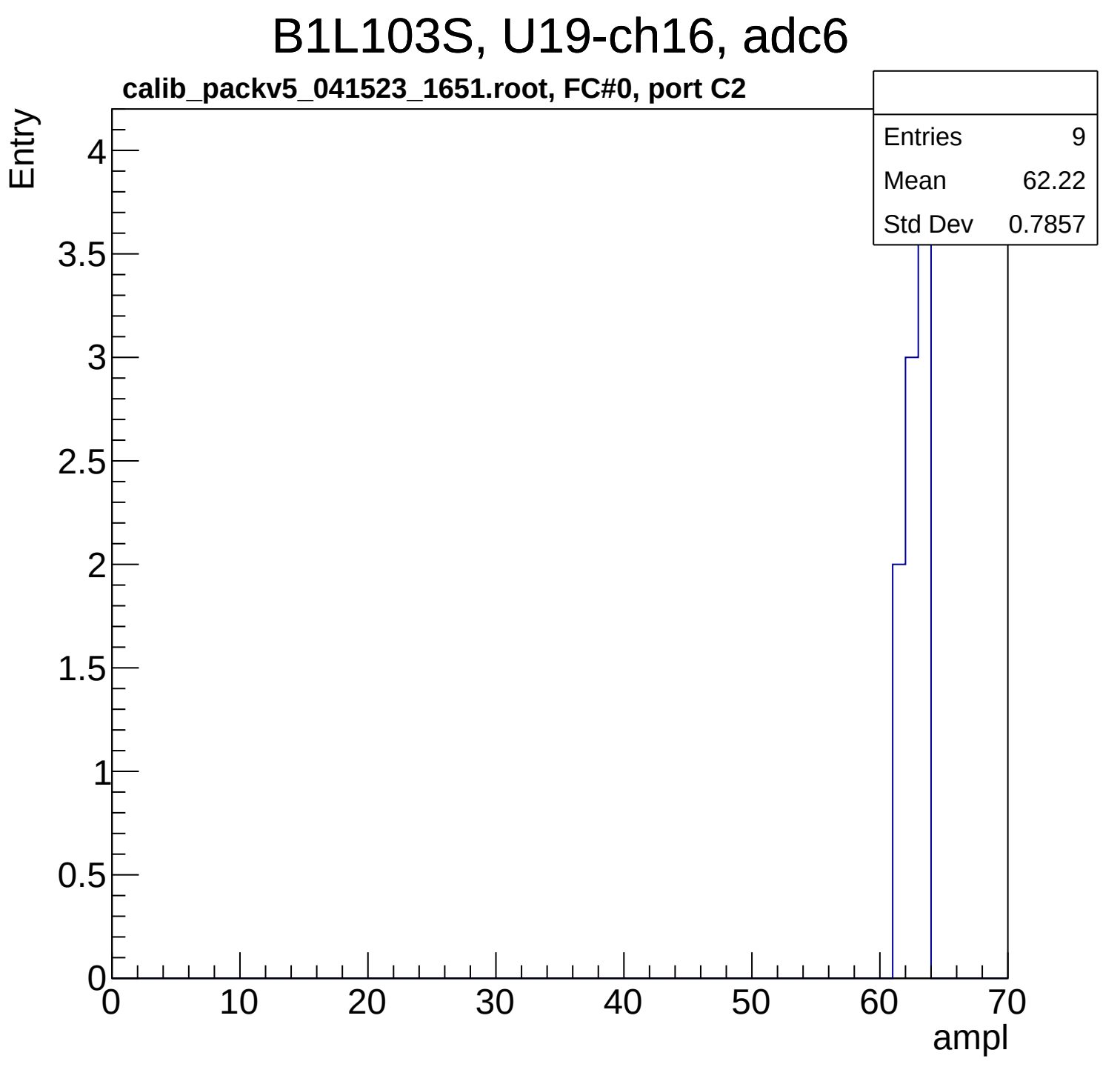
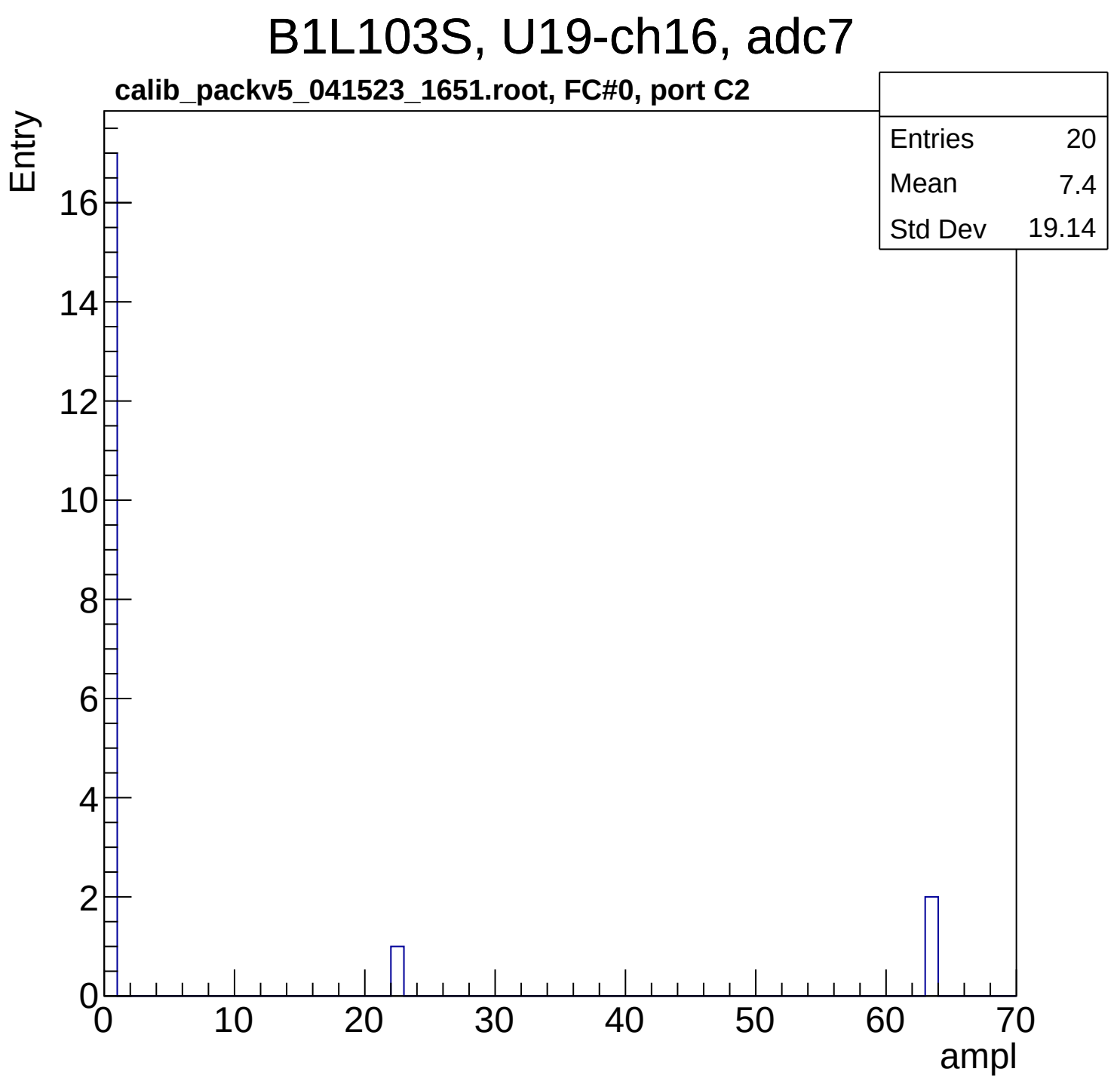
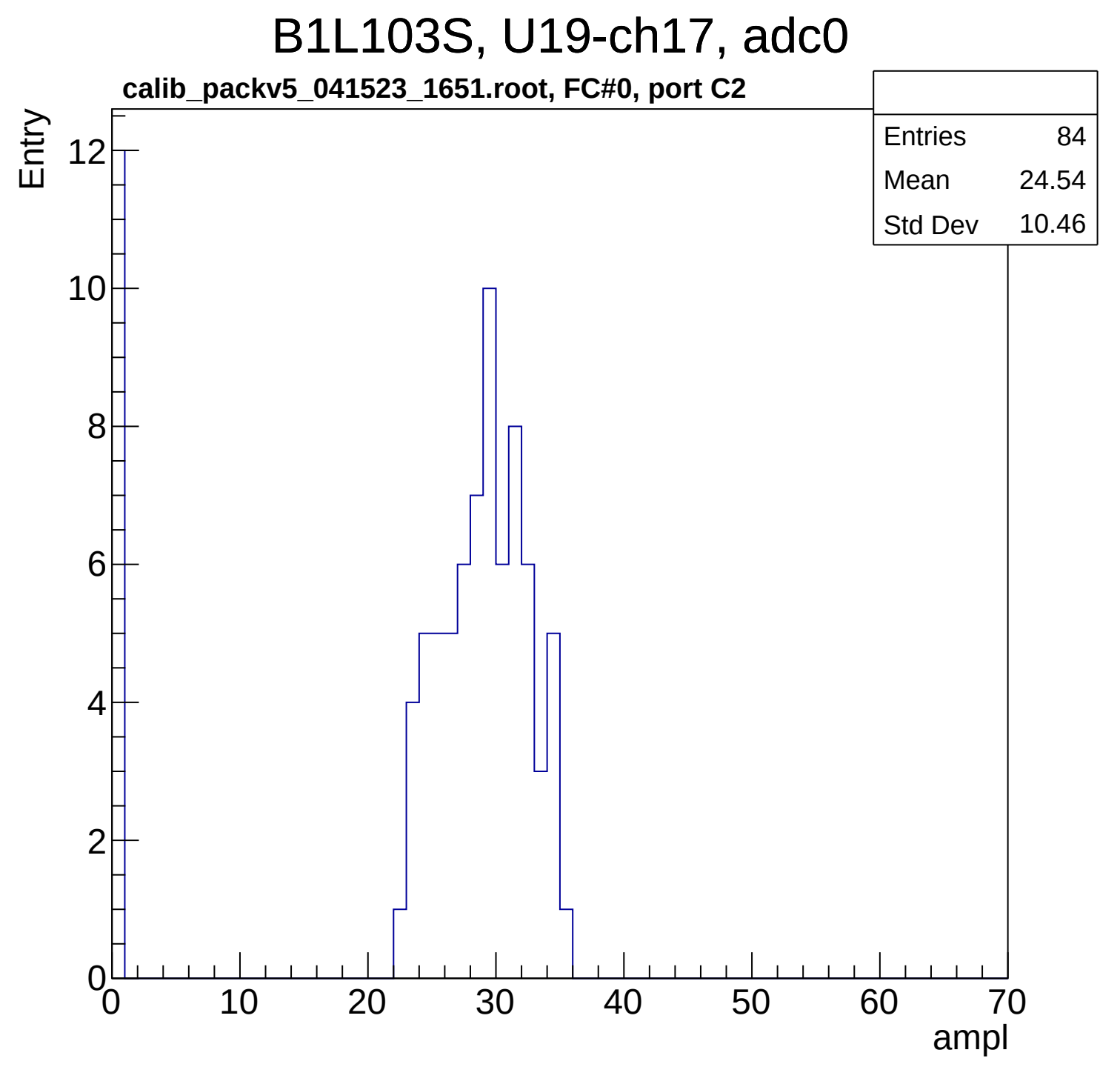
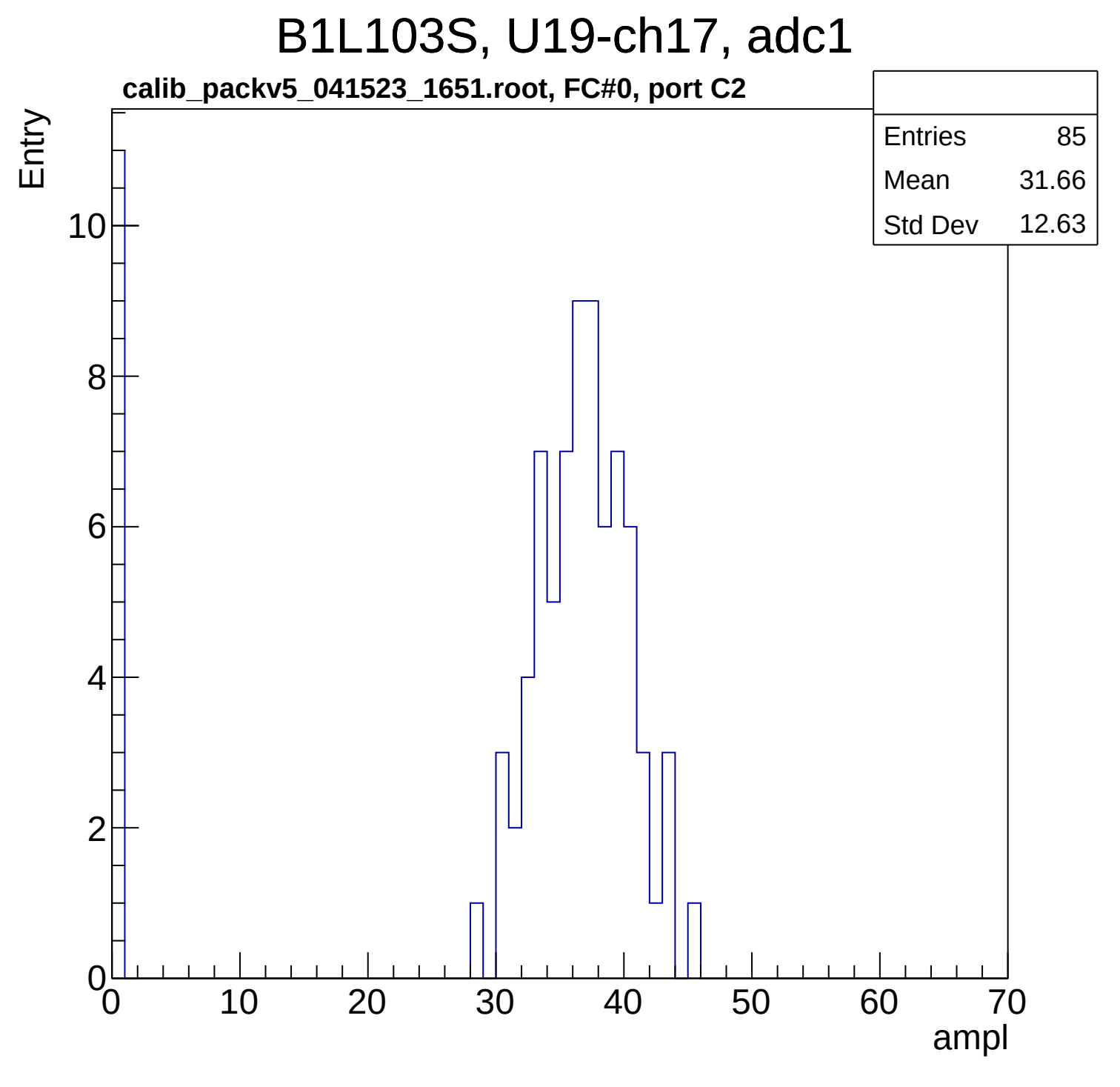

B1L103S, U19-ch16, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 53.67
Std Dev 8.33
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

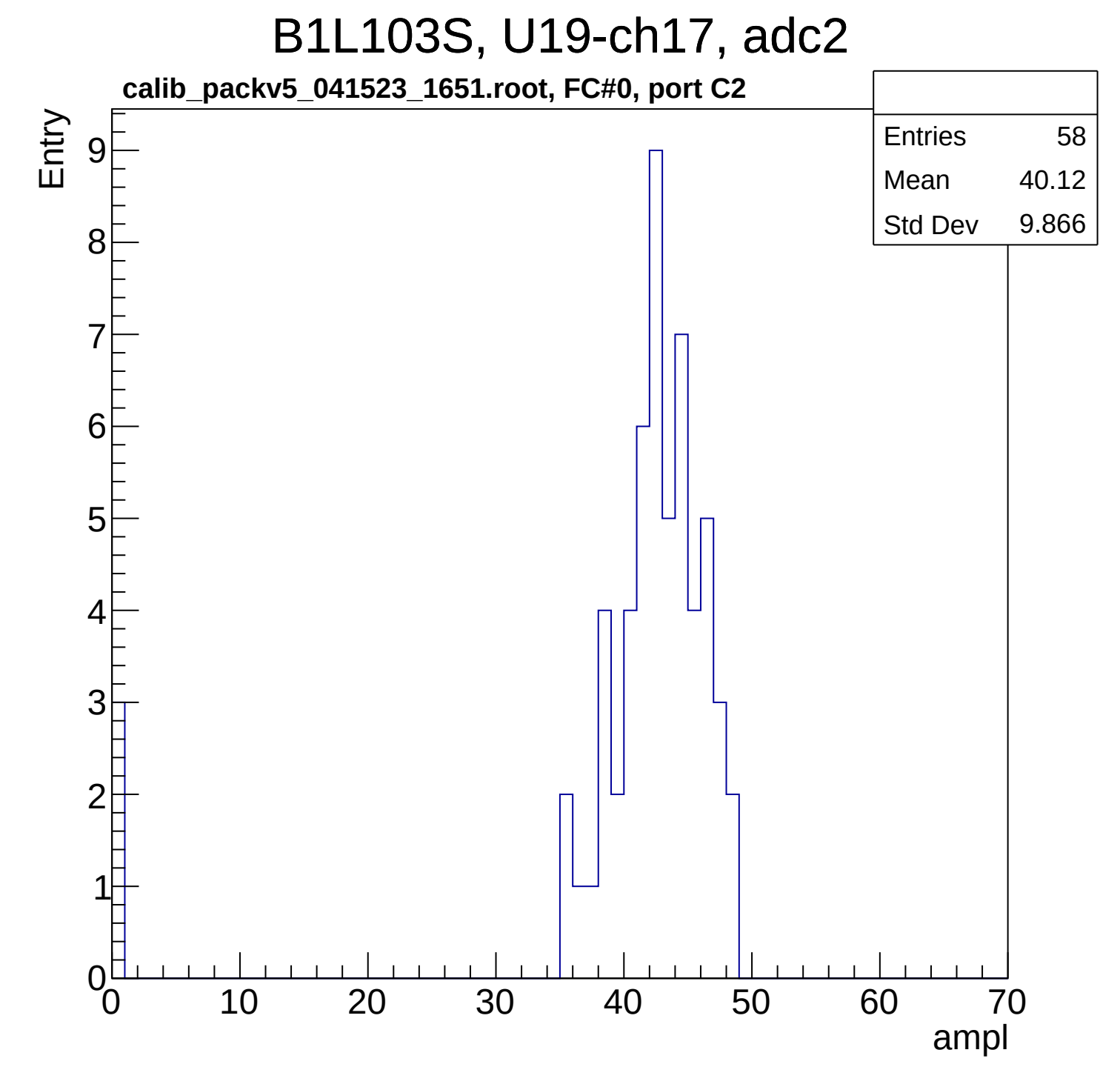

B1L103S, U19-ch16, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 59.48
Std Dev 2.393
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch16, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 62.22
Std Dev 0.7857
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U19-ch16, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 7.4
Std Dev 19.14
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch17, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 24.54
Std Dev 10.46
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U19-ch17, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 31.66
Std Dev 12.63
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch17, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 40.12
Std Dev 9.866
Entry
ampl
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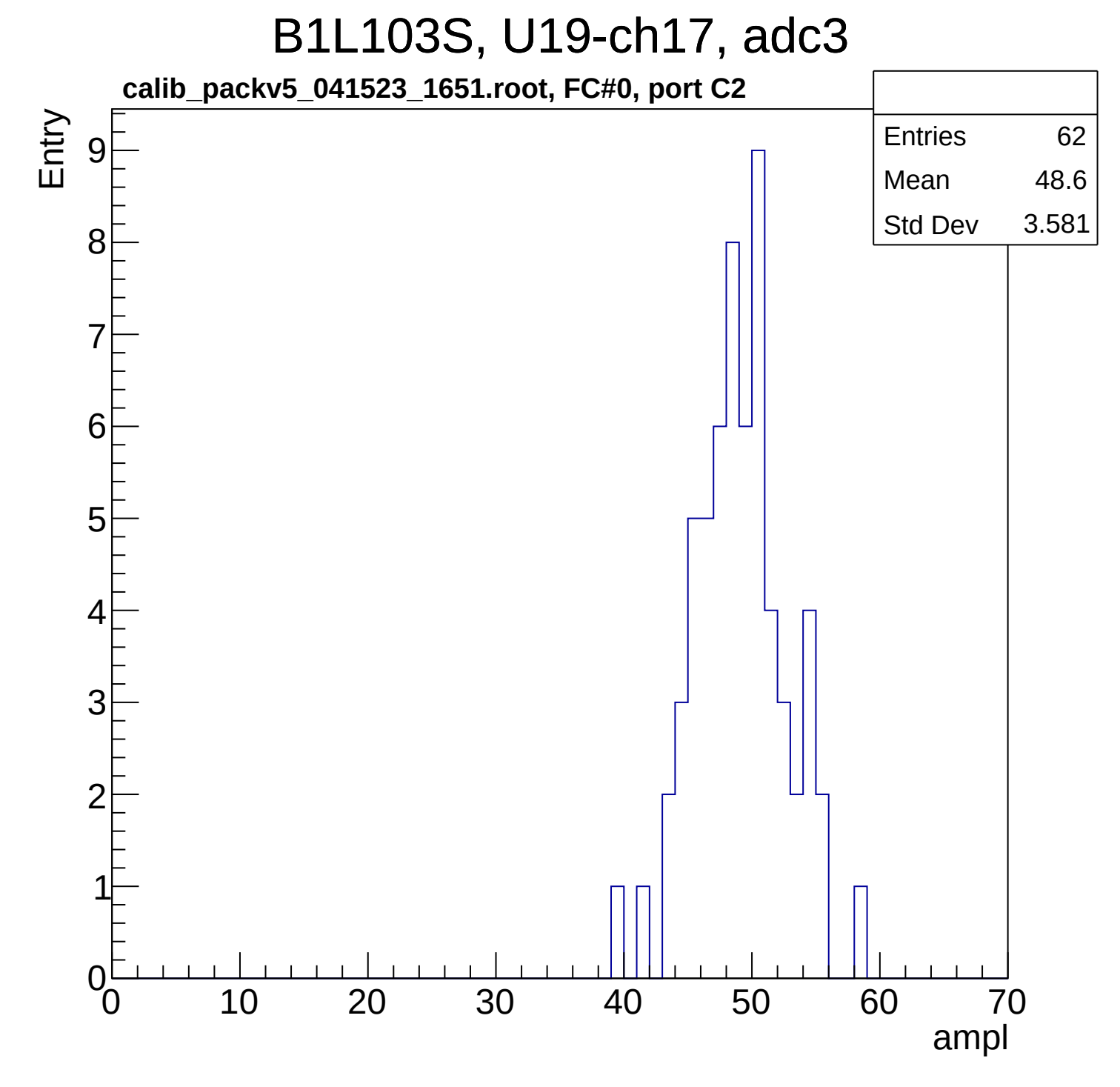
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch17, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 48.6
Std Dev 3.581
Entry
ampl
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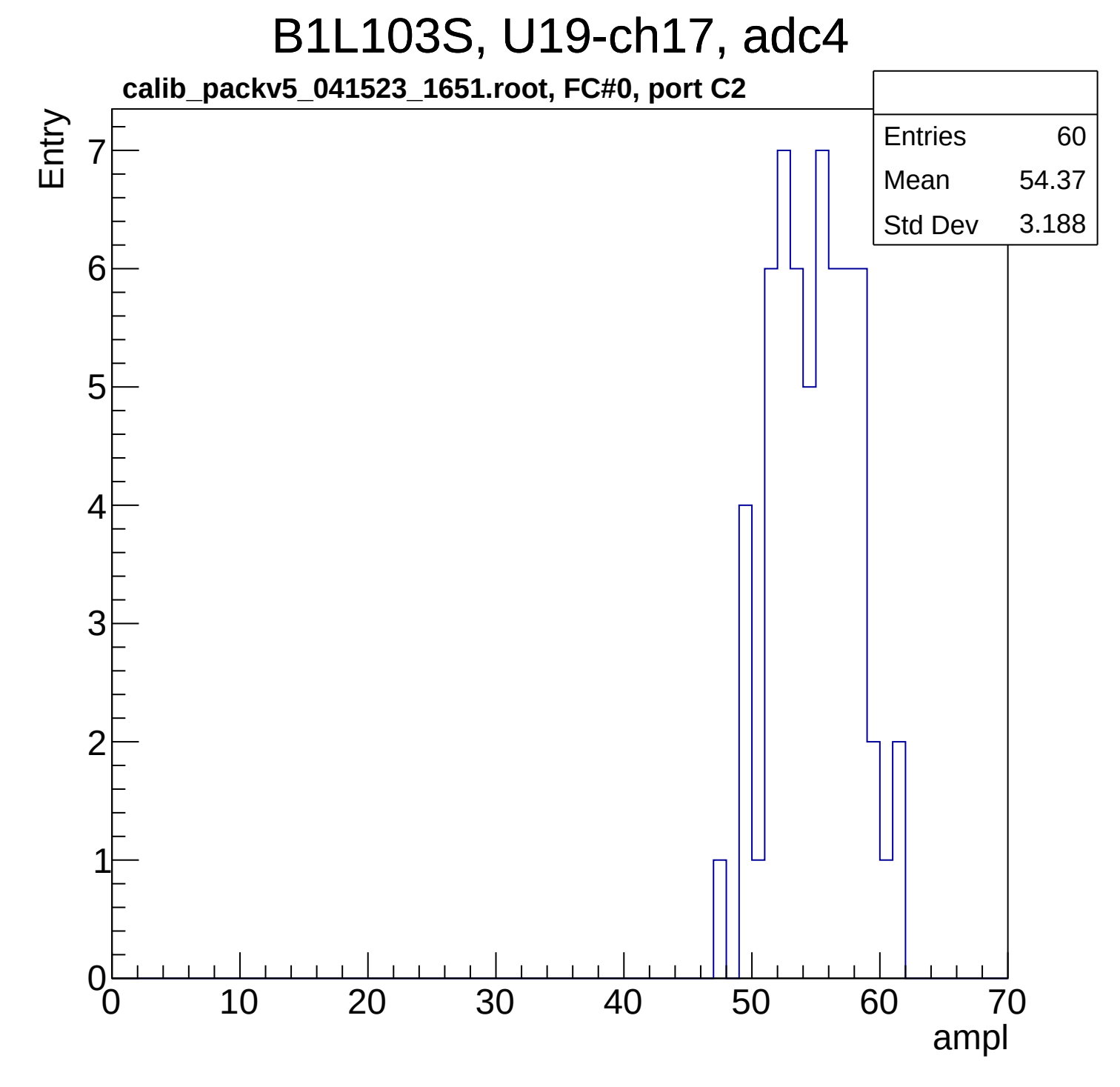
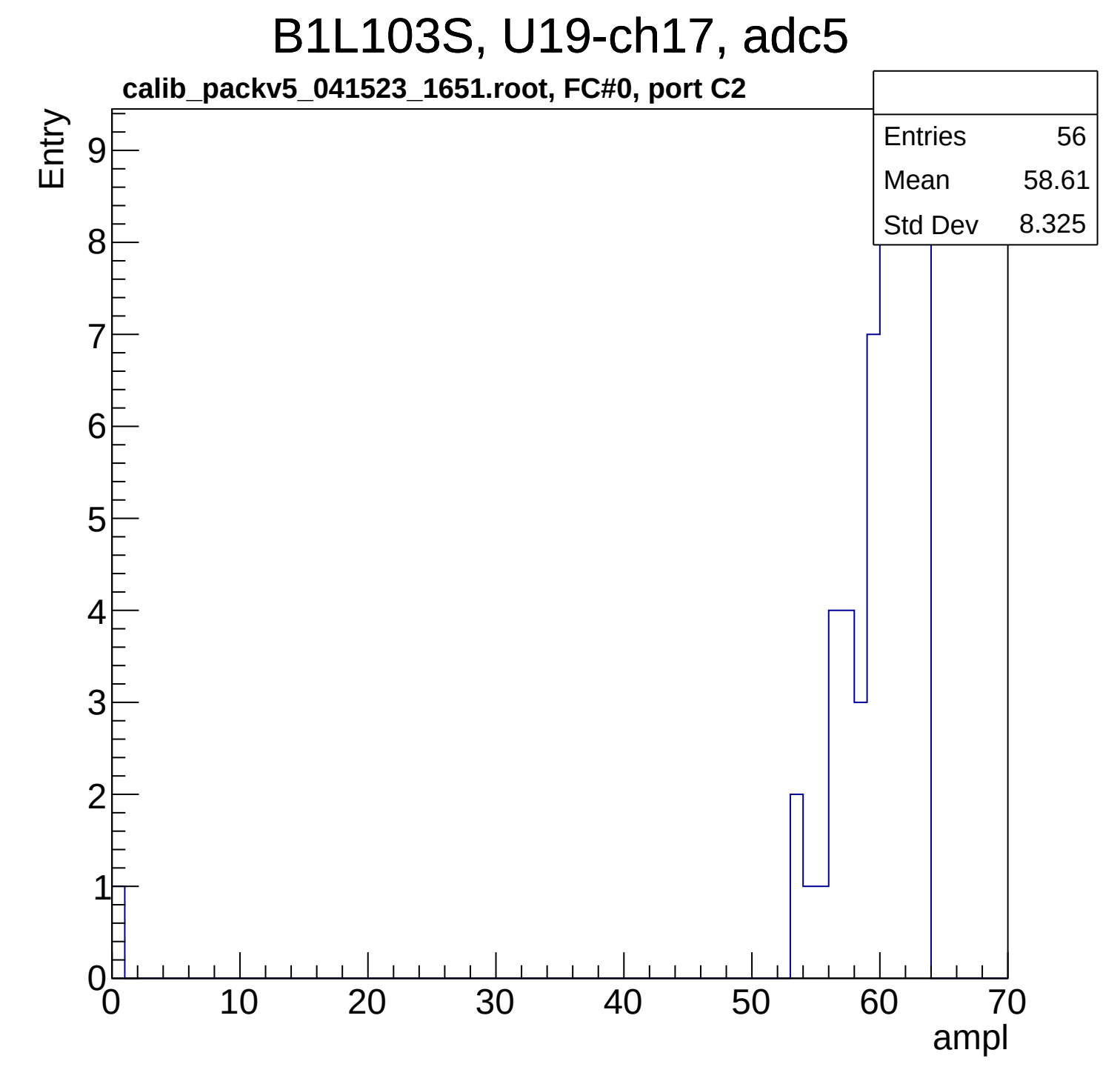
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch17, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 54.37
Std Dev 3.188
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch17, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 58.61
Std Dev 8.325
Entry
ampl
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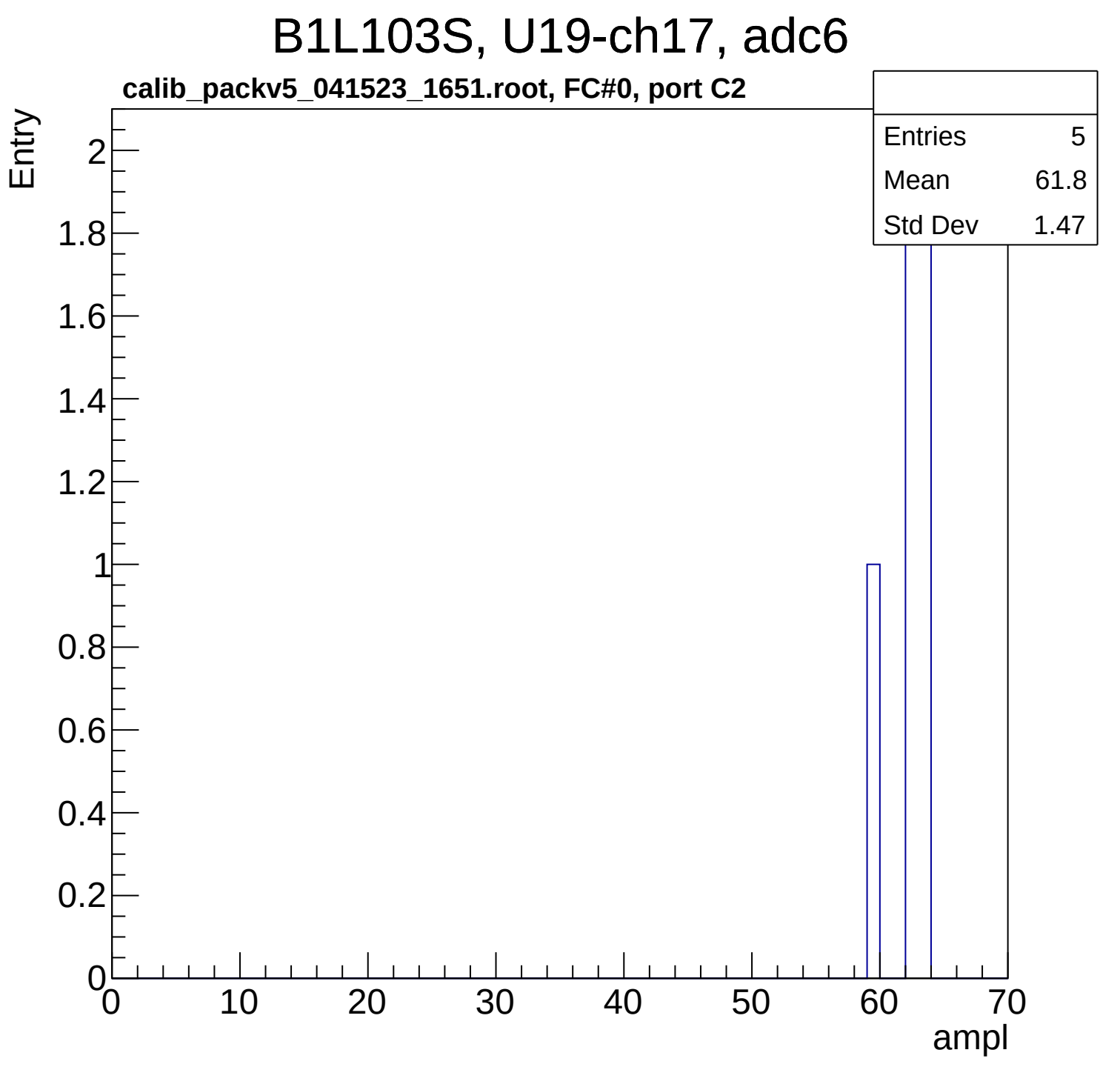
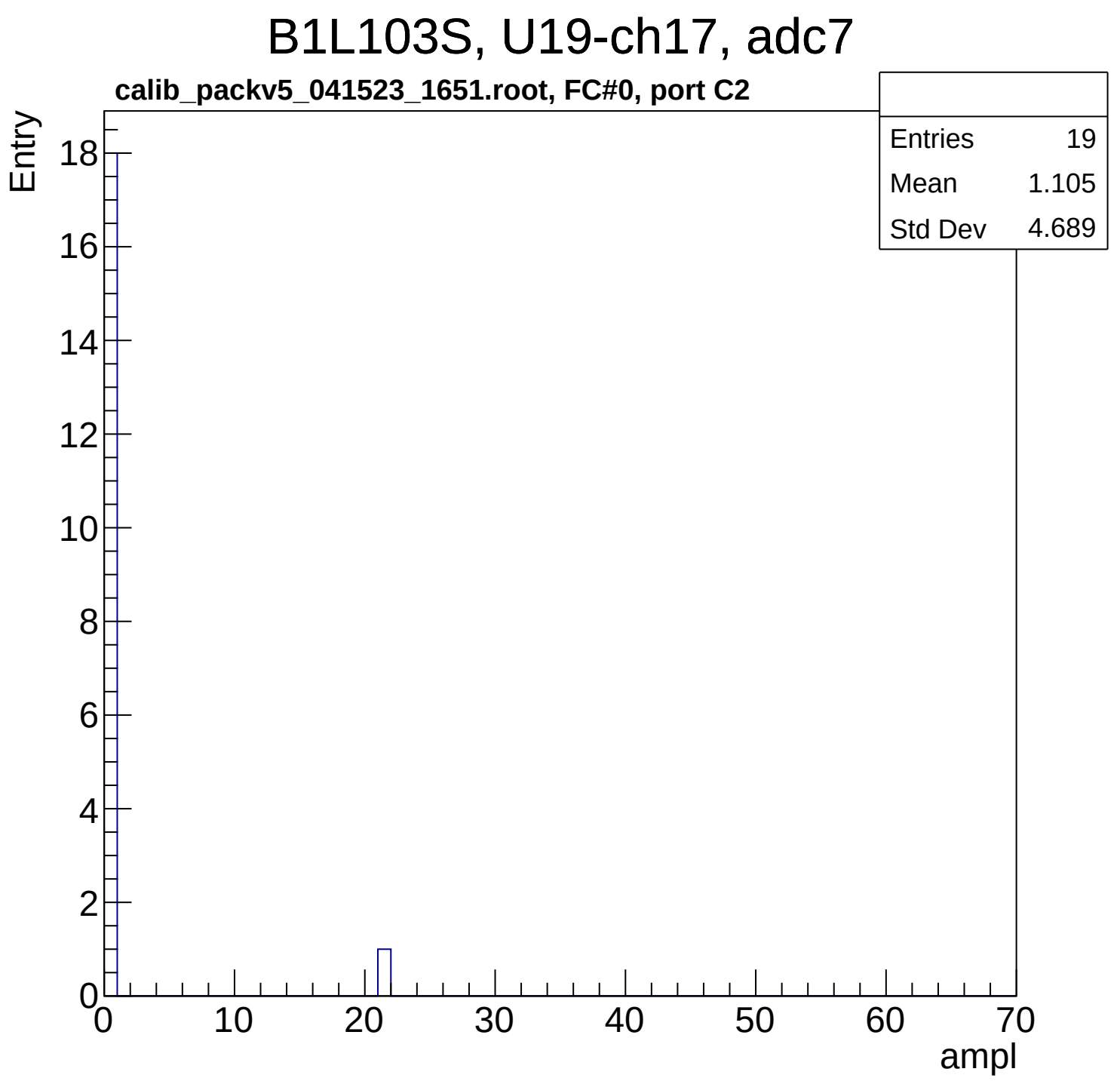
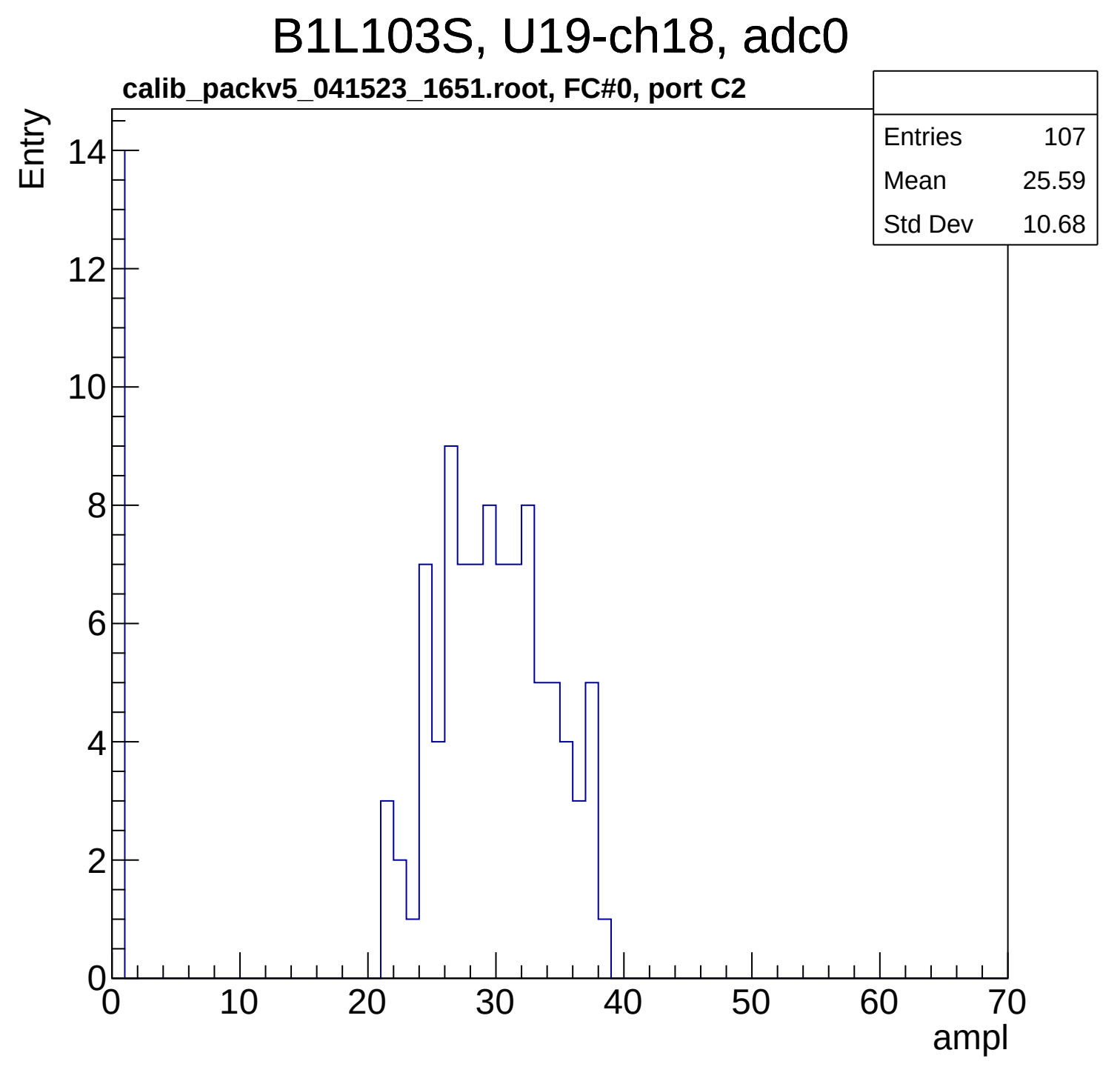
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch17, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 61.8
Std Dev 1.47
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U19-ch17, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.105
Std Dev 4.689
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch18, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 107
Mean 25.59
Std Dev 10.68
Entry
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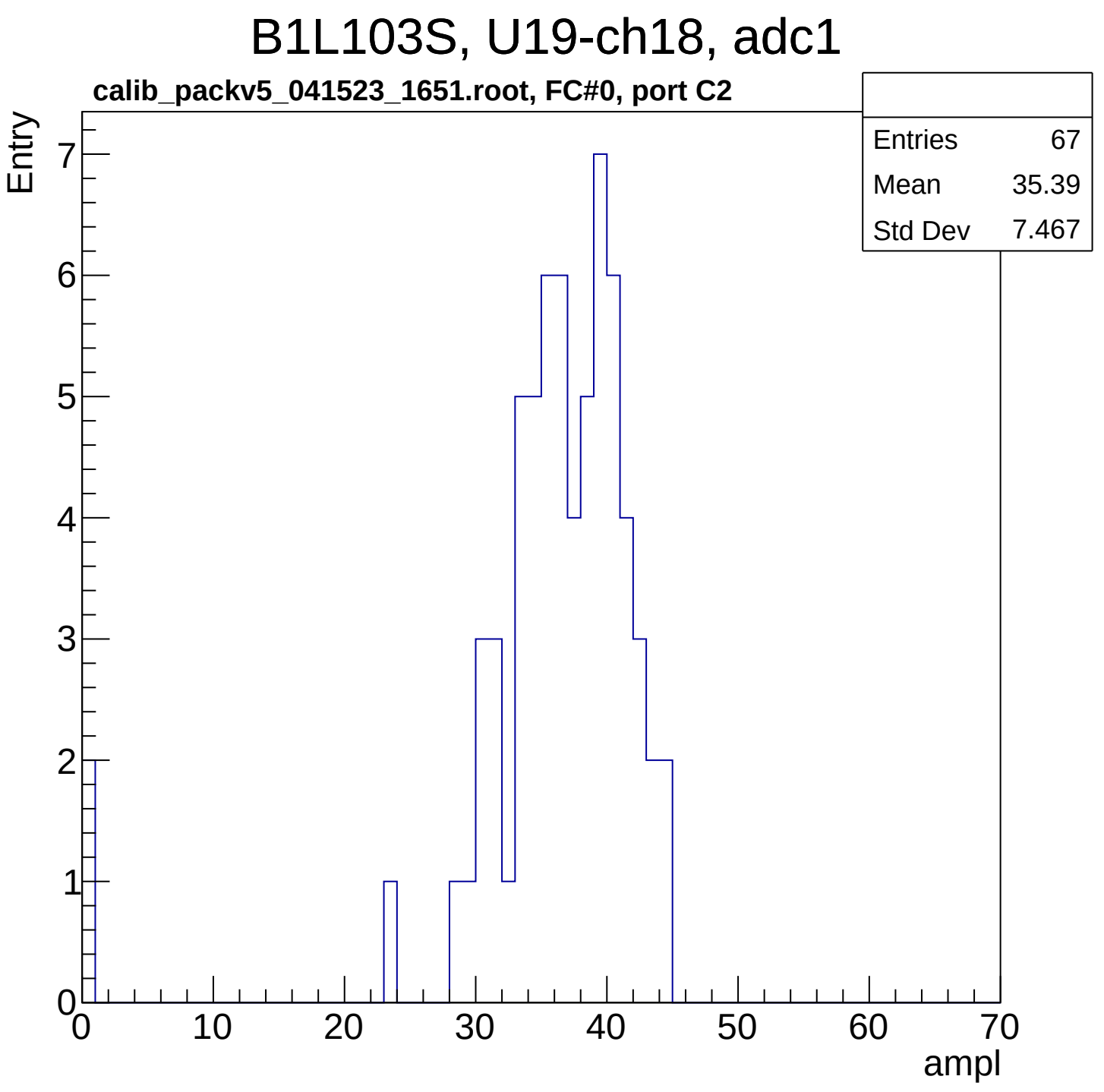
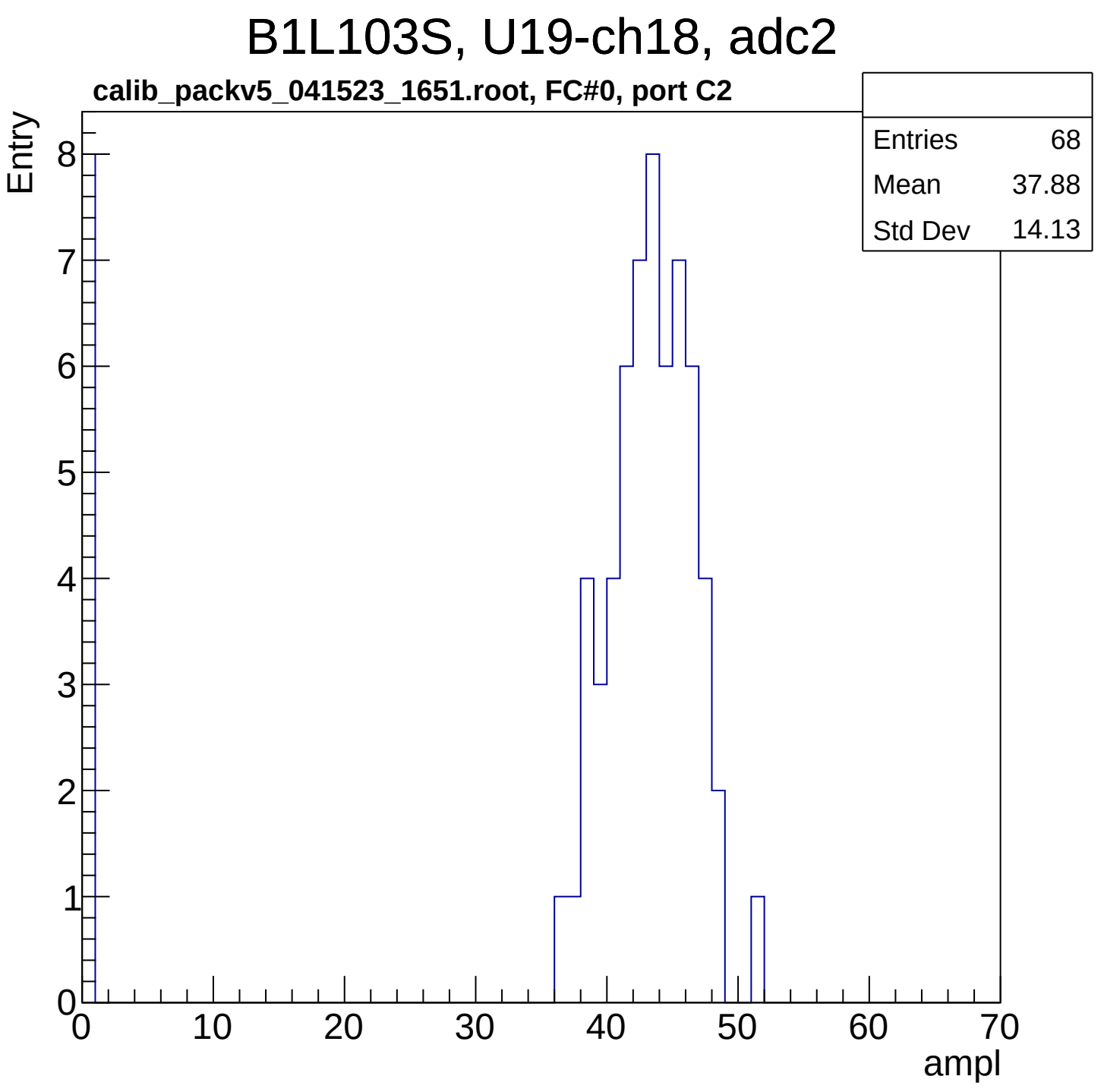
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch18, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 35.39
Std Dev 7.467
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch18, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 37.88
Std Dev 14.13
Entry
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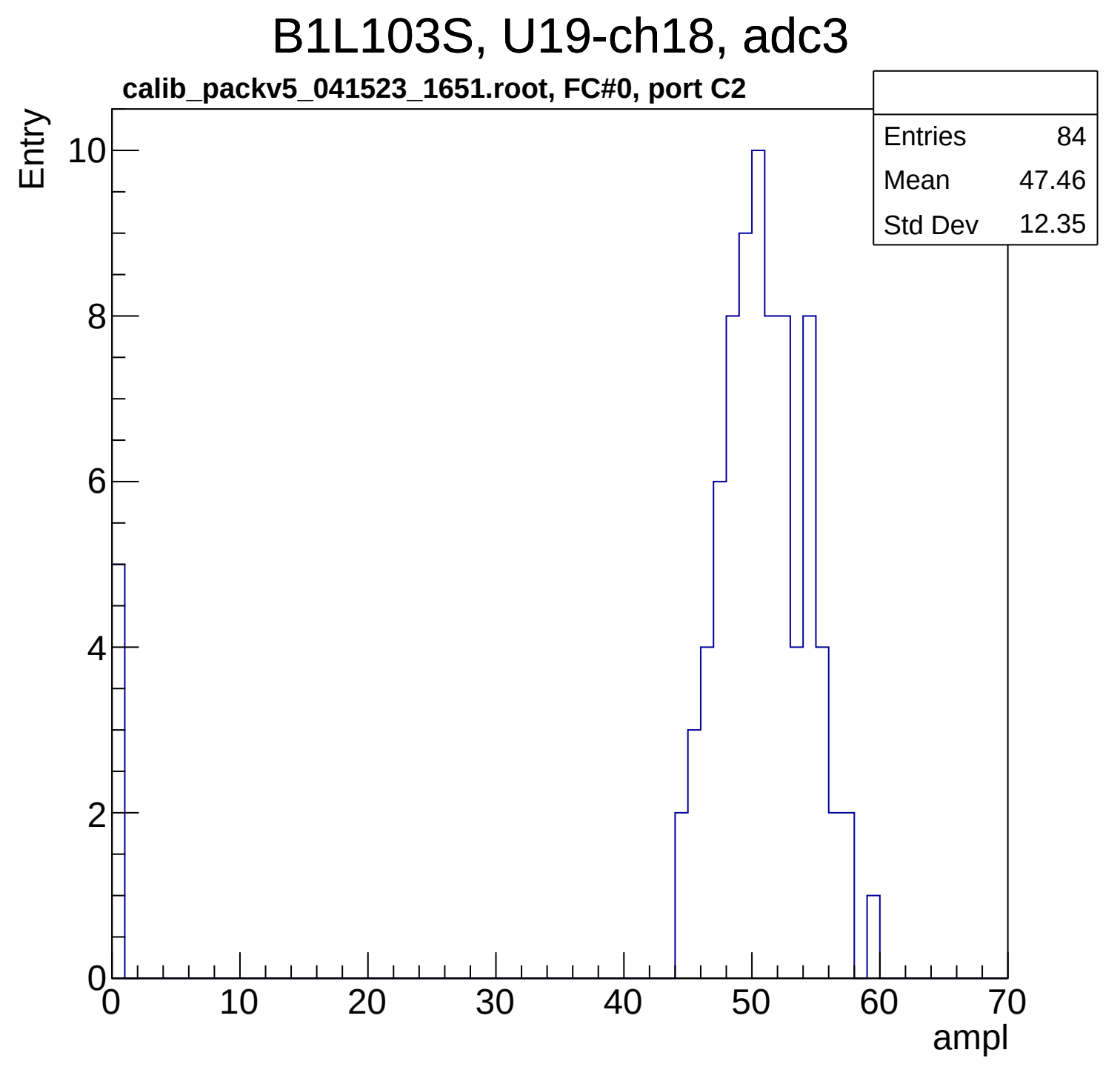
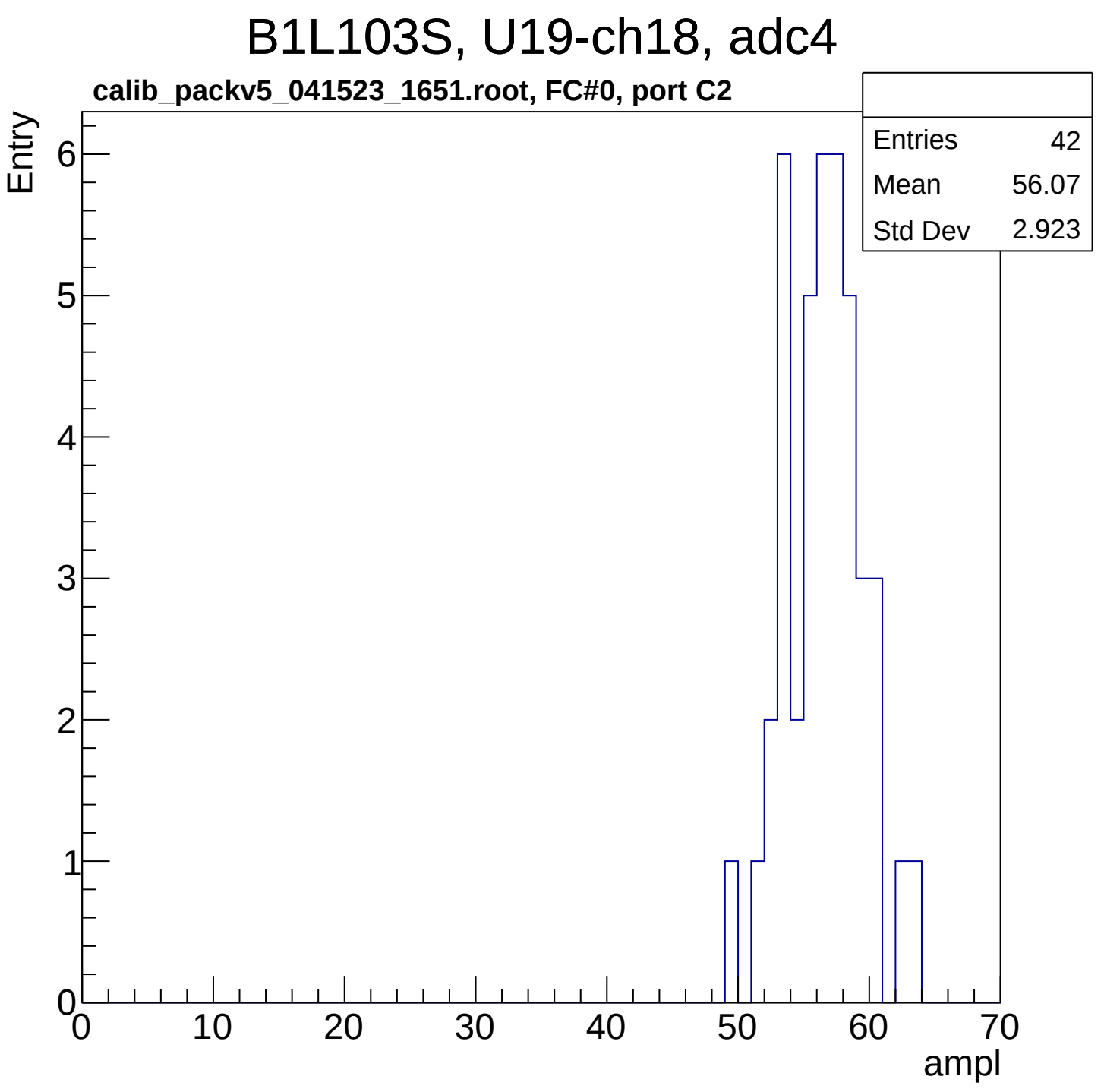
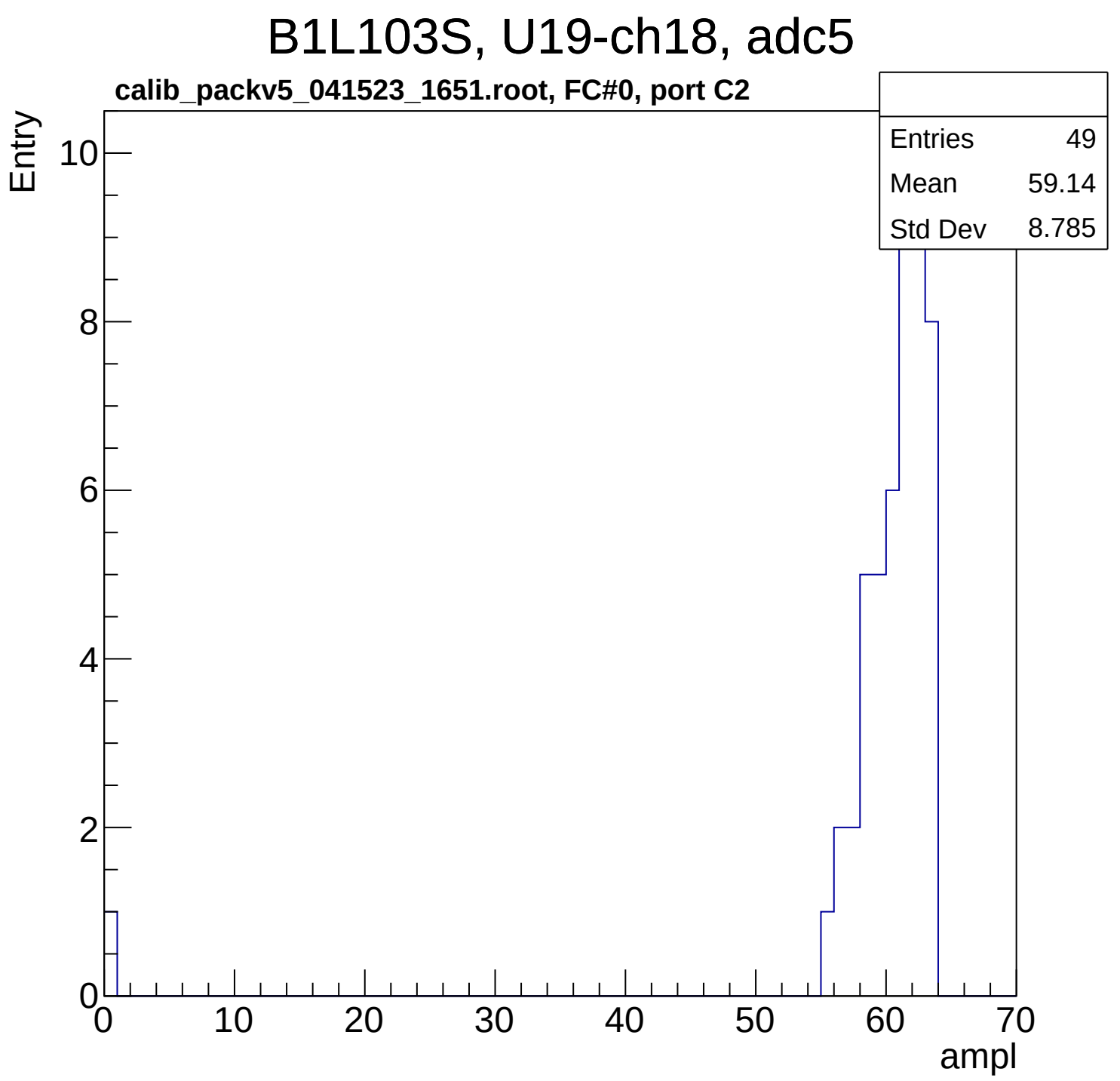
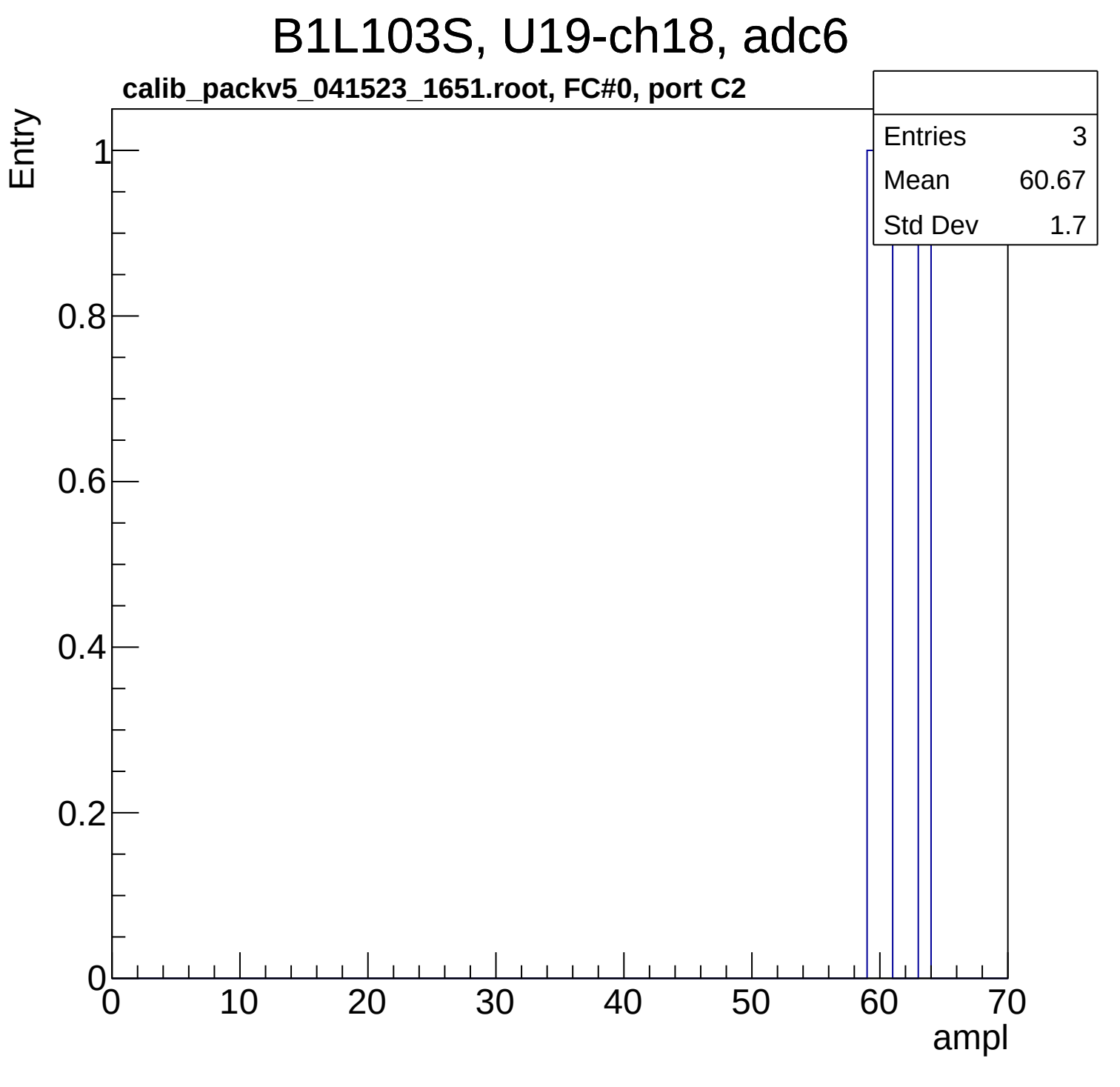
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch18, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 47.46
Std Dev 12.35
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U19-ch18, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 56.07
Std Dev 2.923
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U19-ch18, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 59.14
Std Dev 8.785
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch18, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 60.67
Std Dev 1.7
Entry
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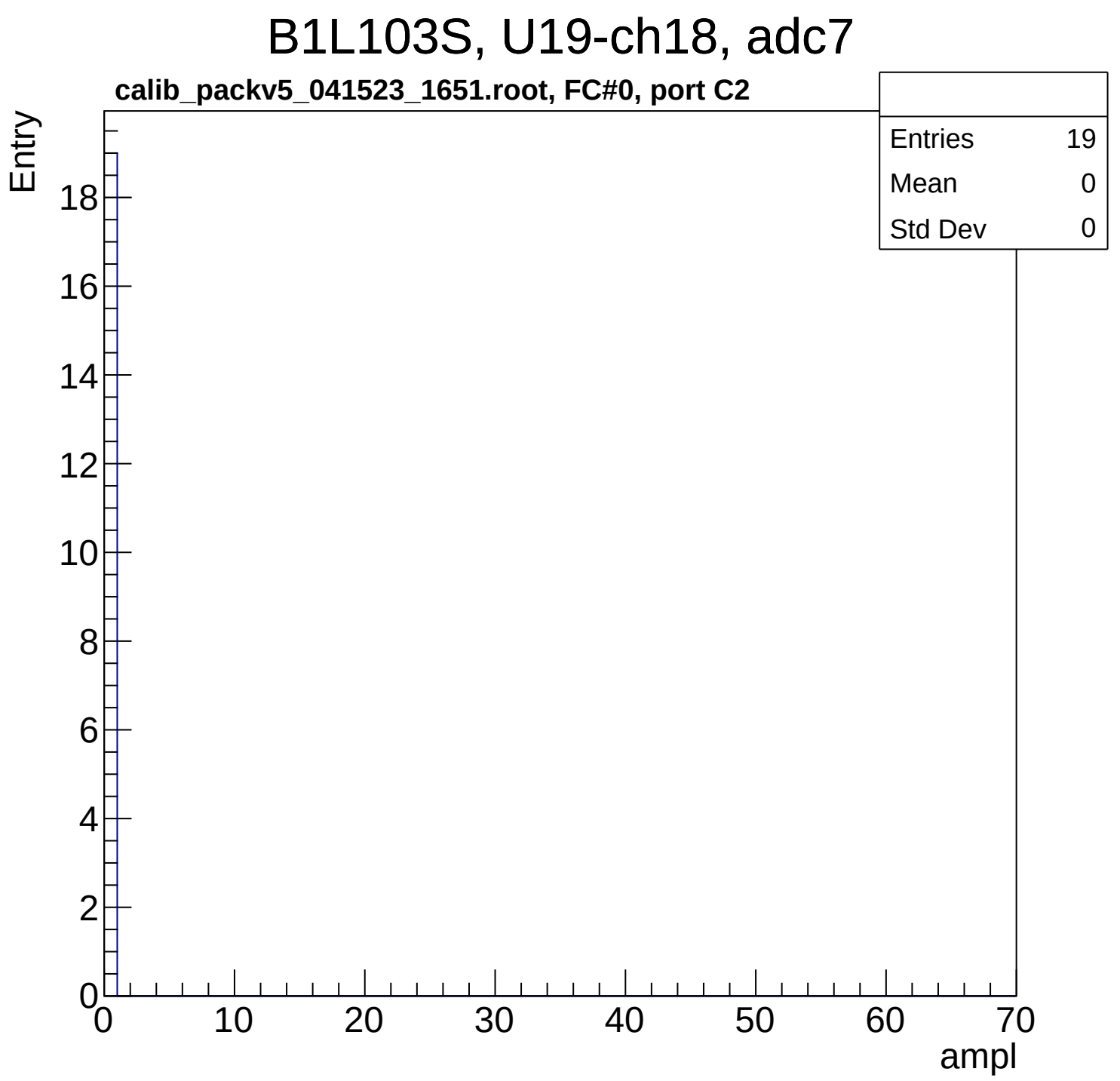
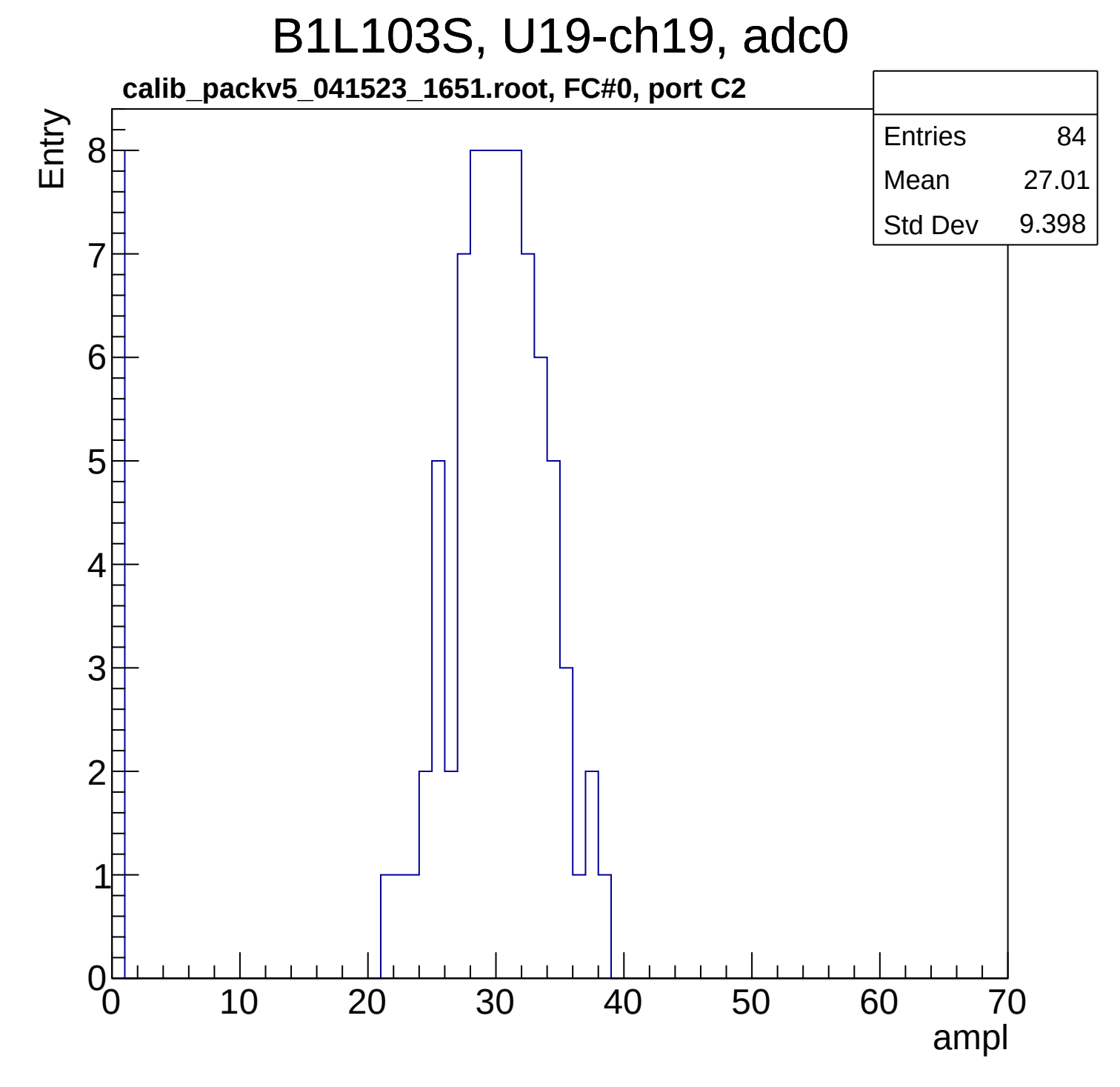
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch18, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch19, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 27.01
Std Dev 9.398
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
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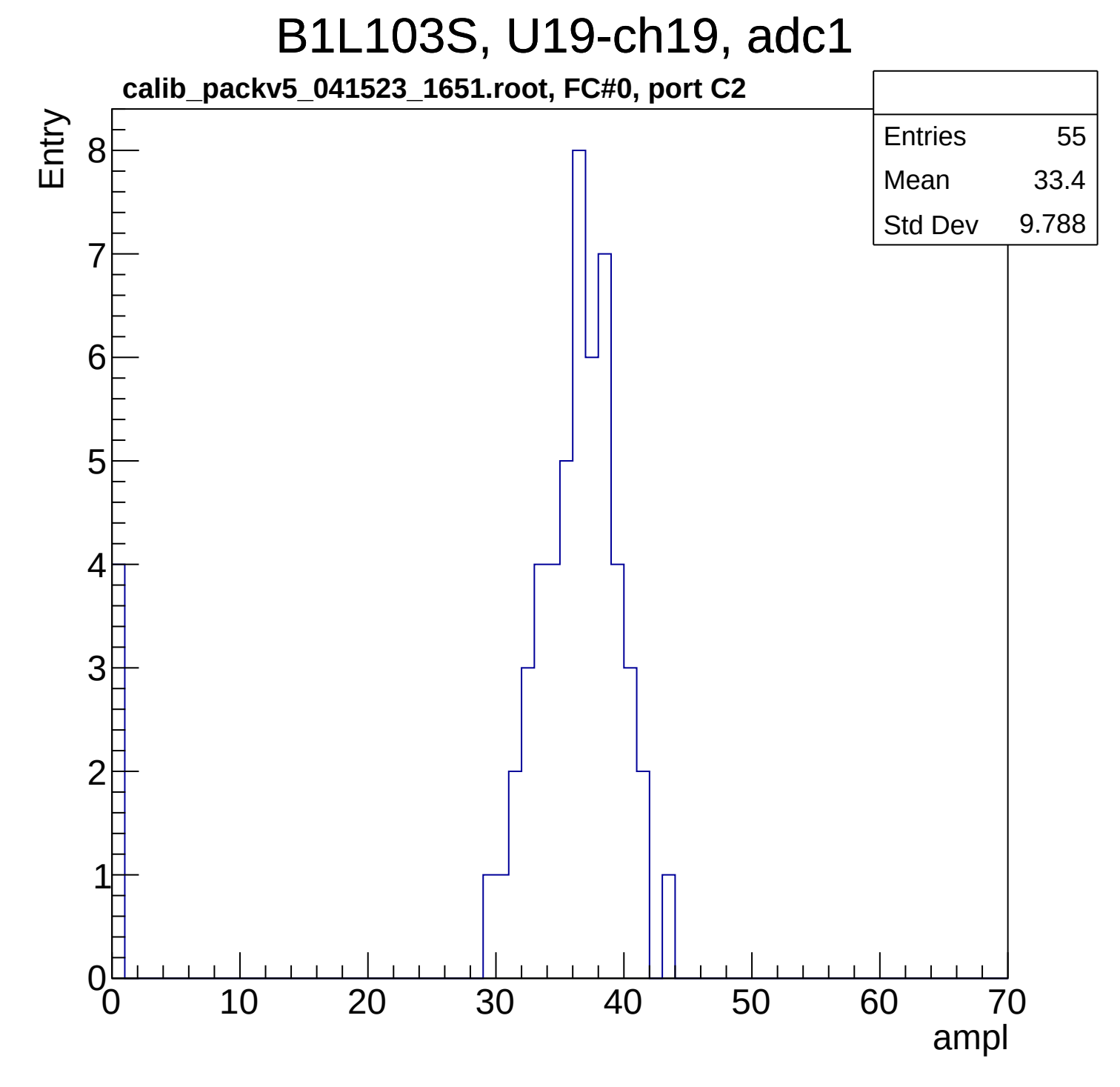
40
50
60
70


B1L103S, U19-ch19, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 33.4
Std Dev 9.788
Entry
ampl
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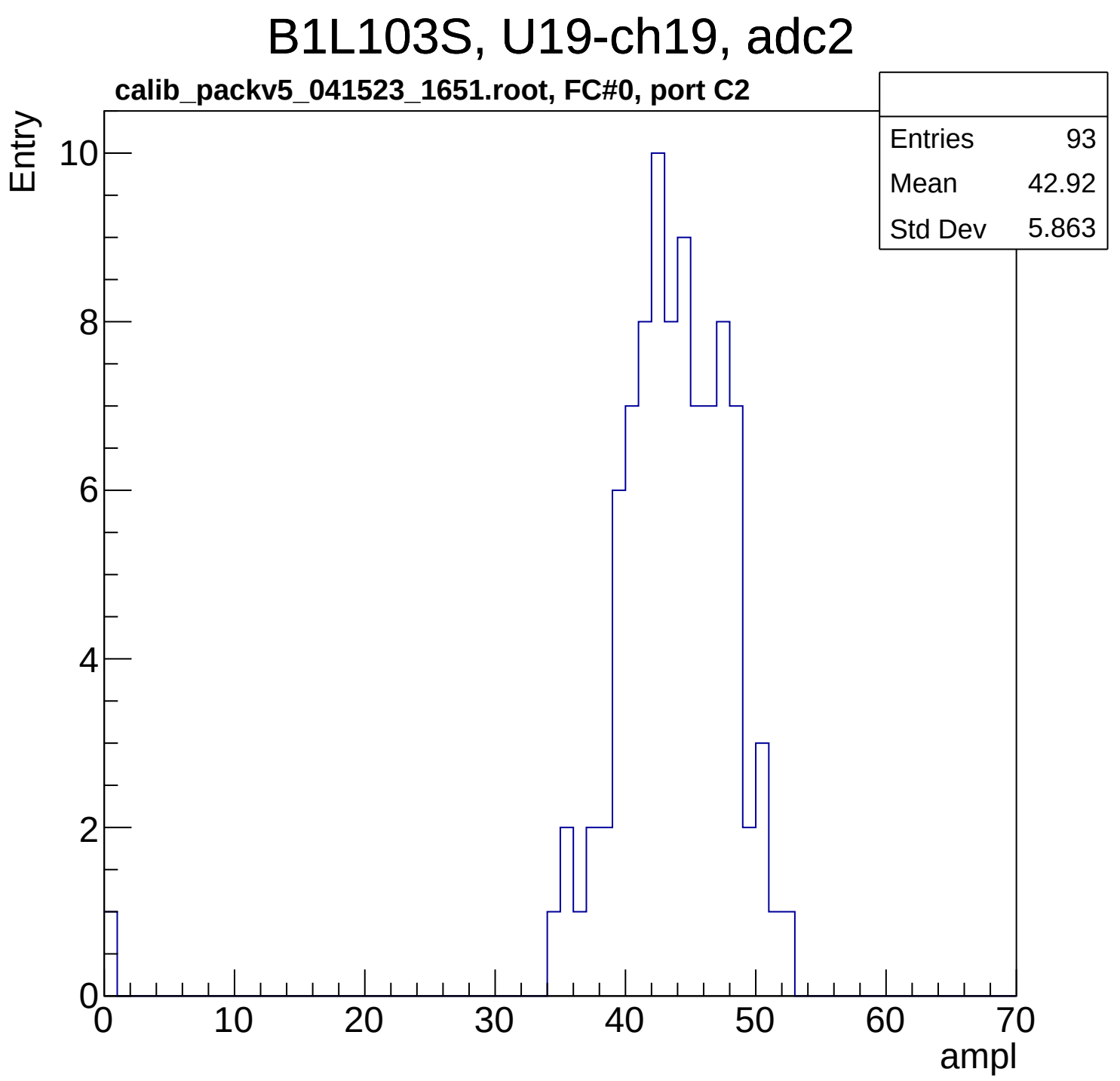
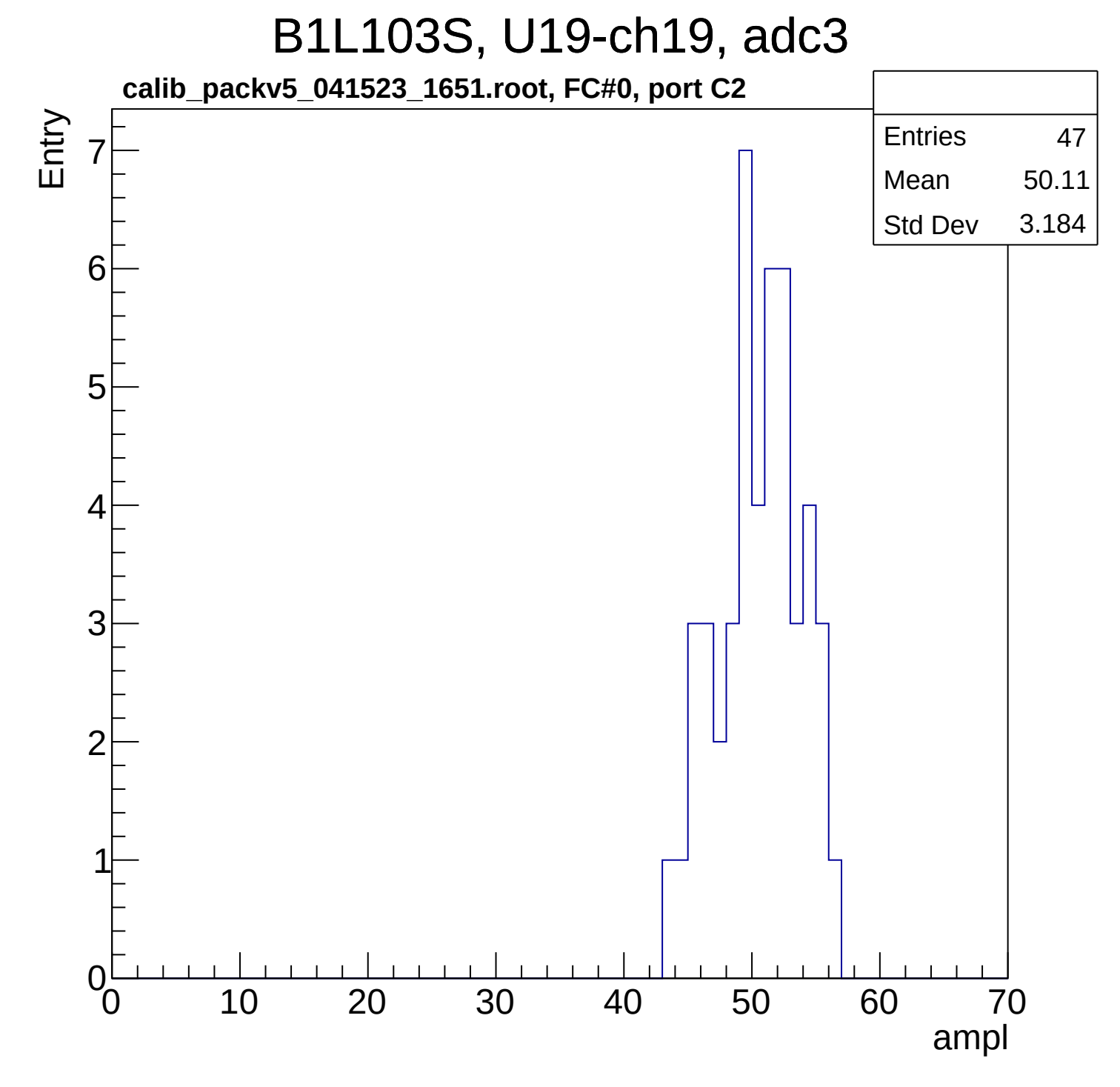
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch19, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 42.92
Std Dev 5.863
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U19-ch19, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 50.11
Std Dev 3.184
Entry
ampl
0
1
2
3
4
5
6
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0
10
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40
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60
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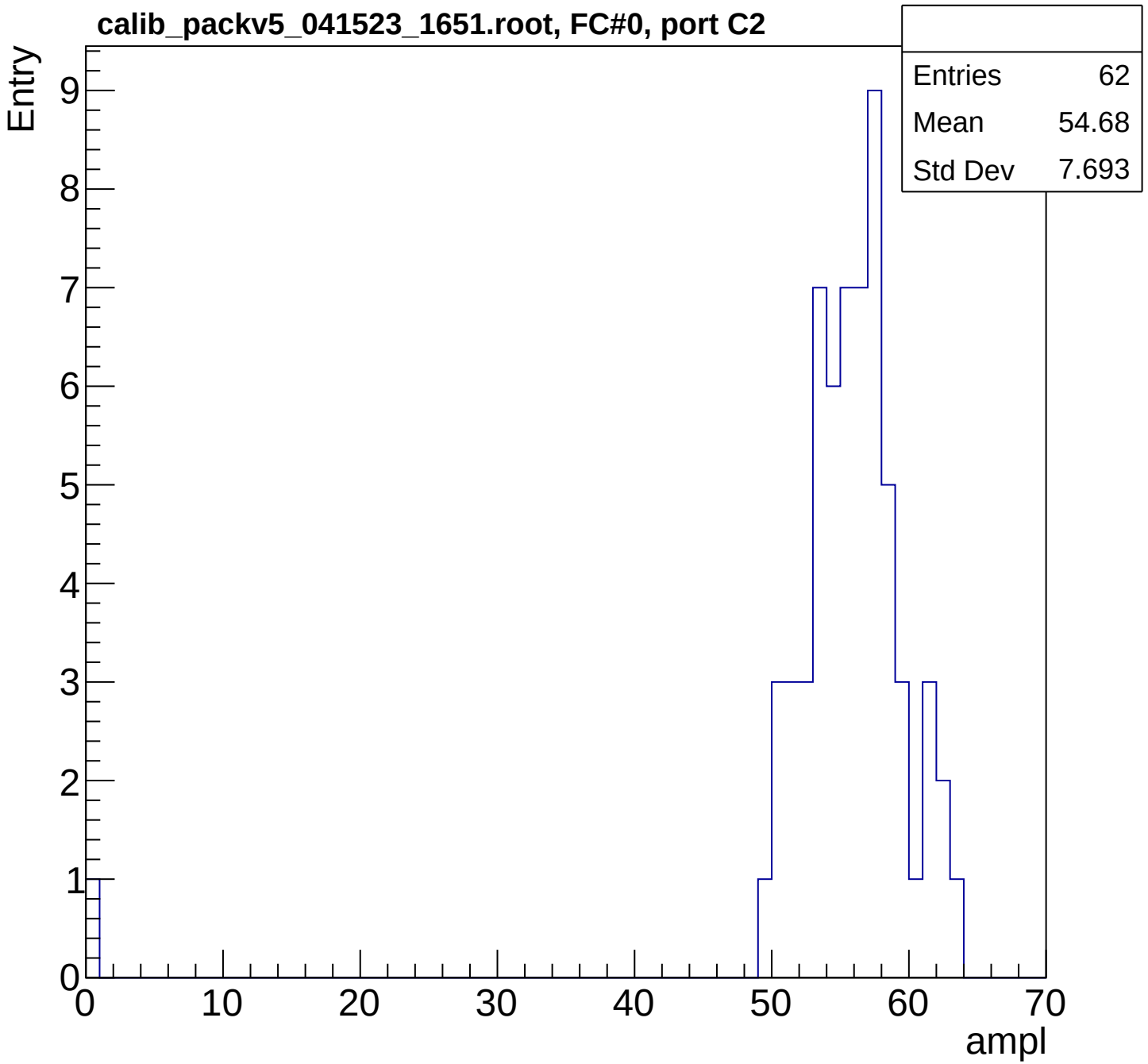
B1L103S, U19-ch19, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 54.68
Std Dev 7.693
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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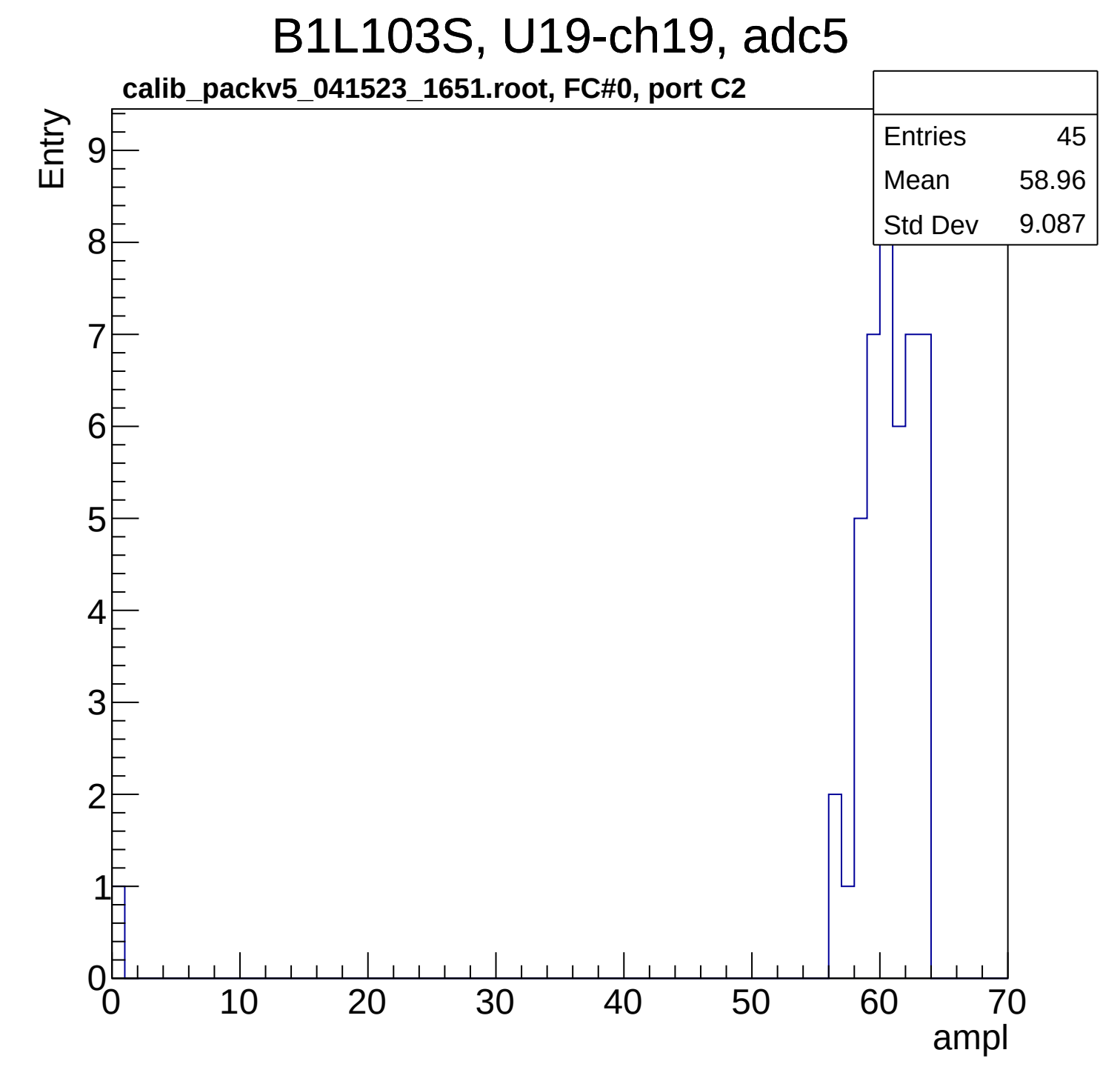
B1L103S, U19-ch19, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 58.96
Std Dev 9.087
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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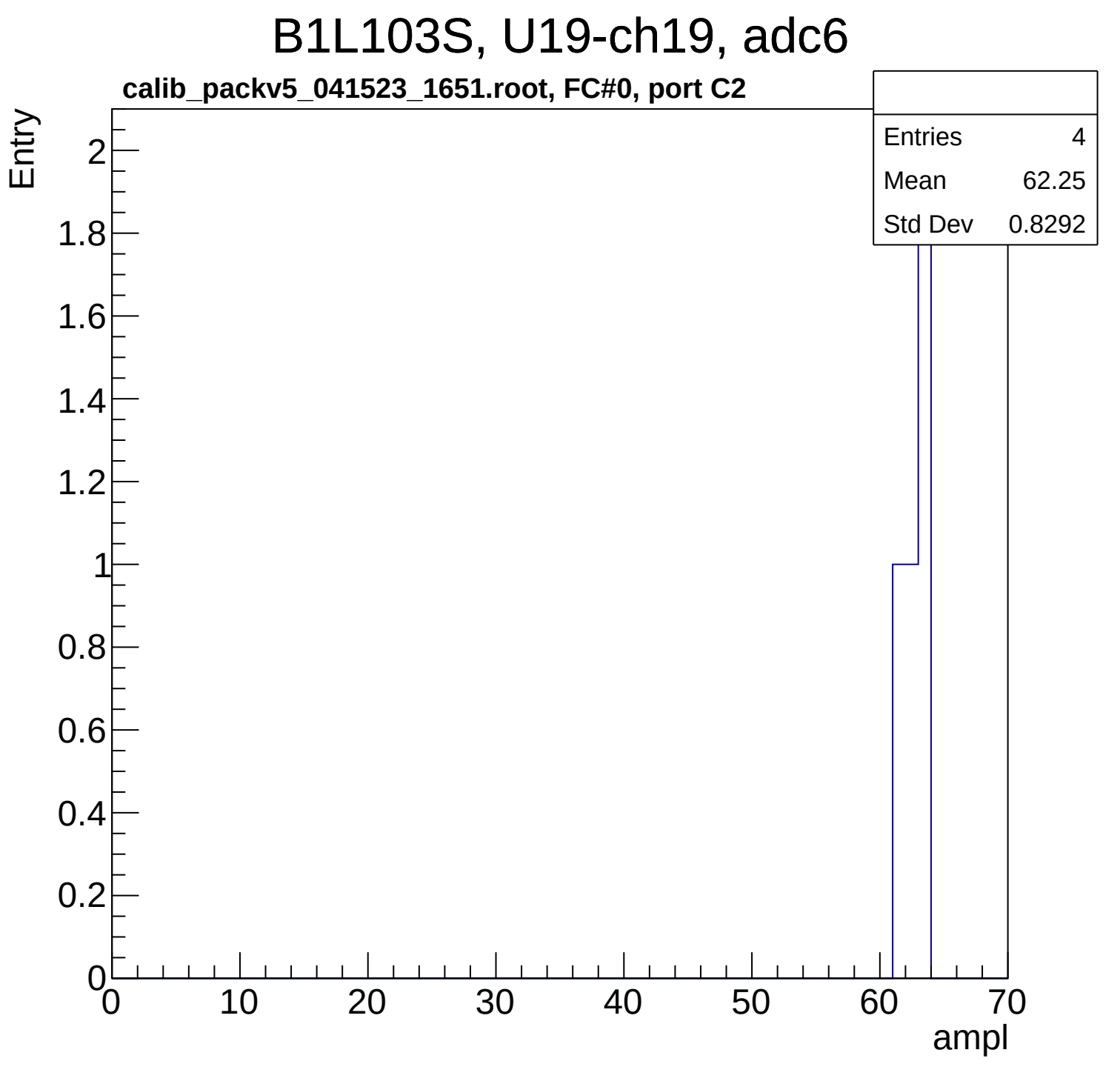
B1L103S, U19-ch19, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 62.25
Std Dev 0.8292
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
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30
40
50
60
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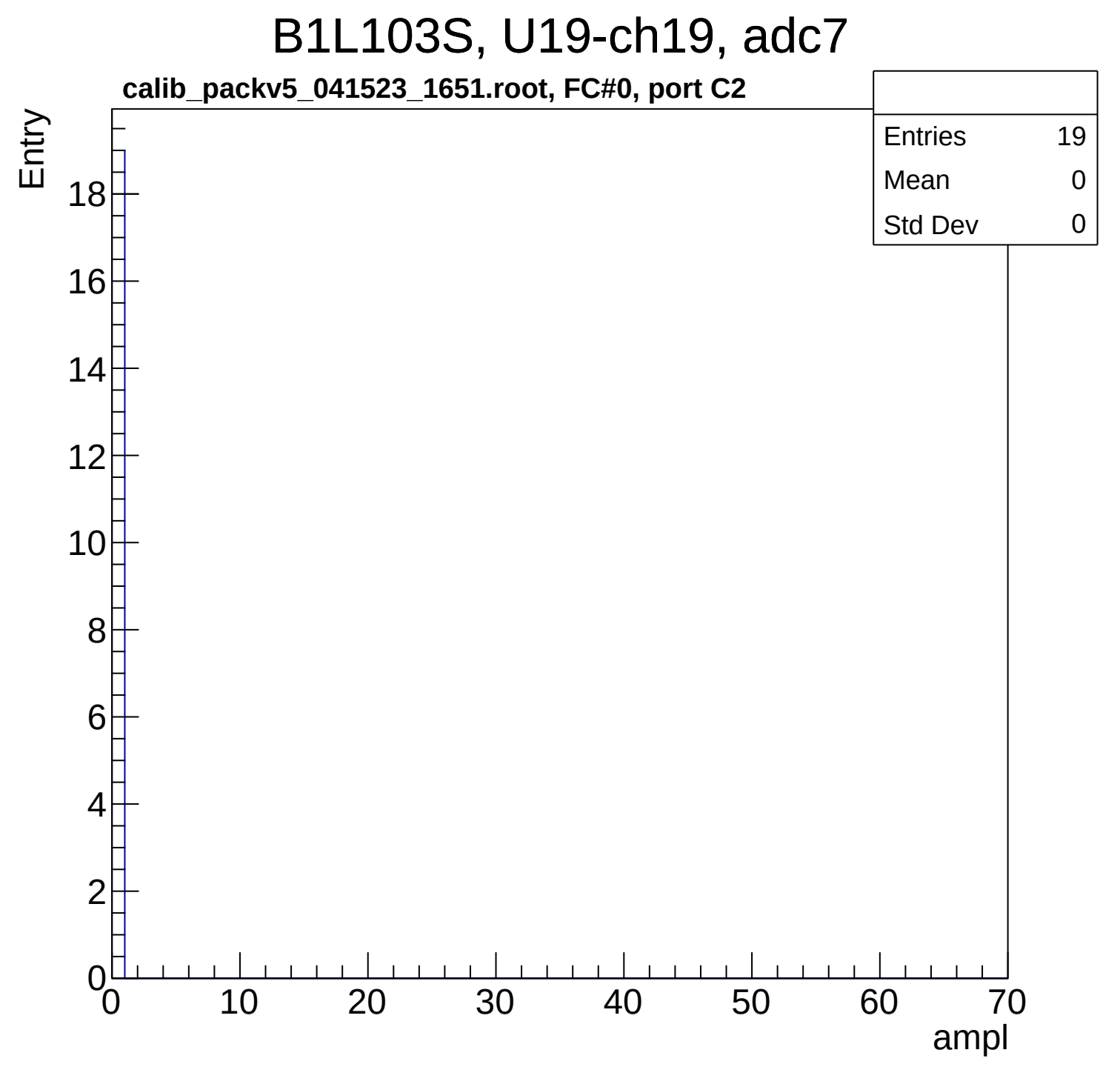
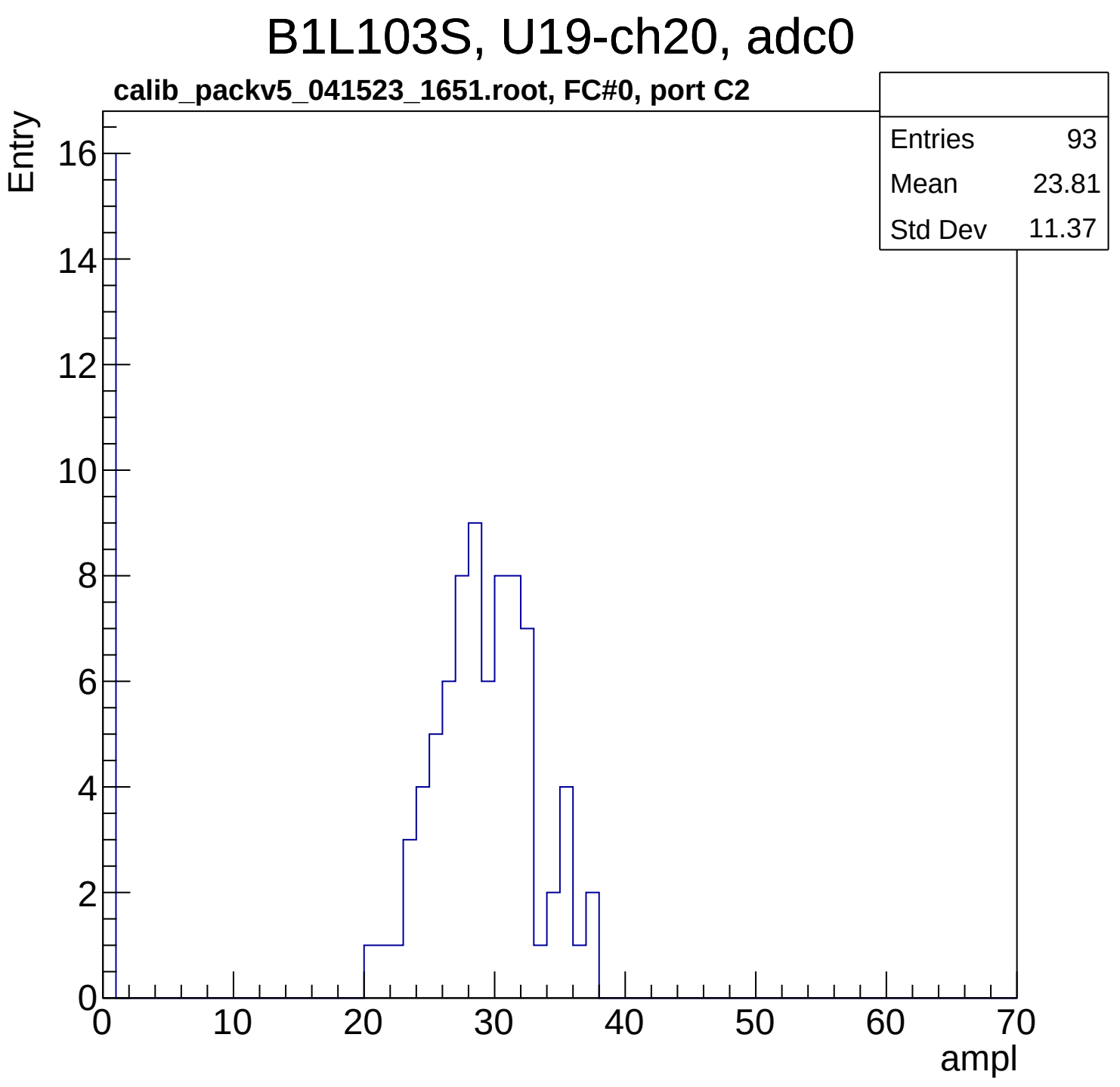

B1L103S, U19-ch19, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch20, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 23.81
Std Dev 11.37
Entry
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4
6
8
10
12
14
16
0
10
20
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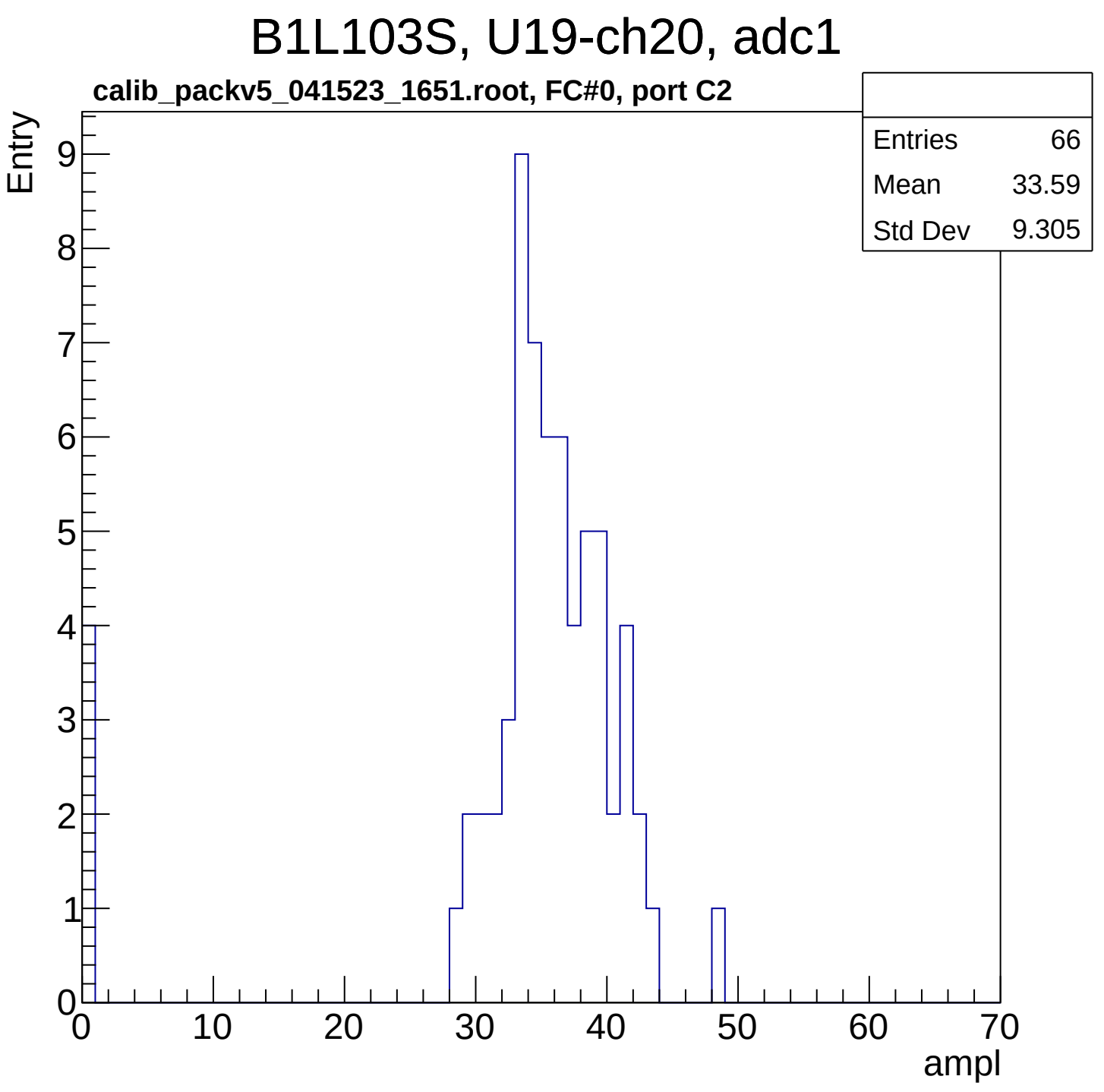
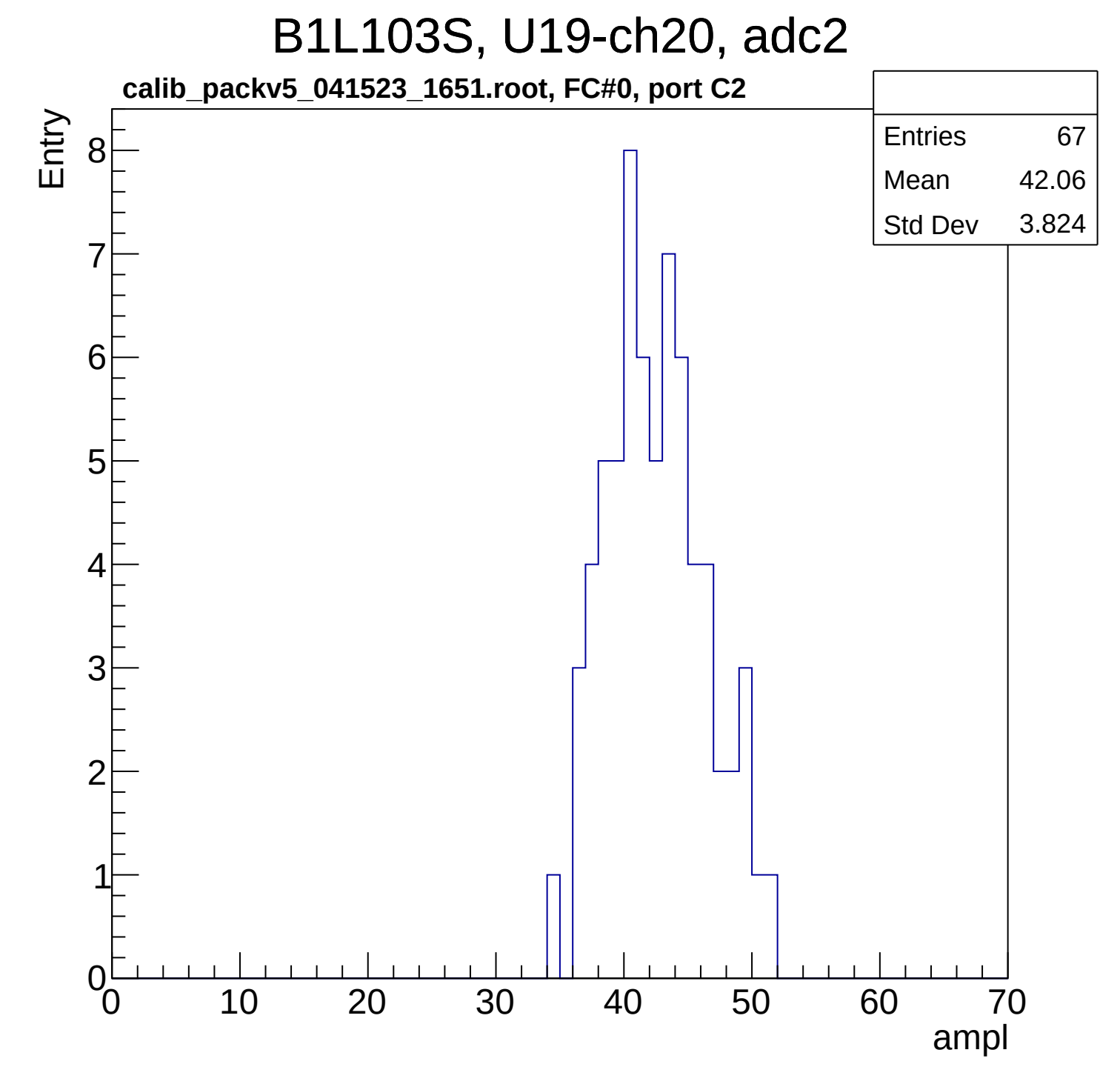
40
50
60
70
ampl


B1L103S, U19-ch20, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 33.59
Std Dev 9.305
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch20, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 42.06
Std Dev 3.824
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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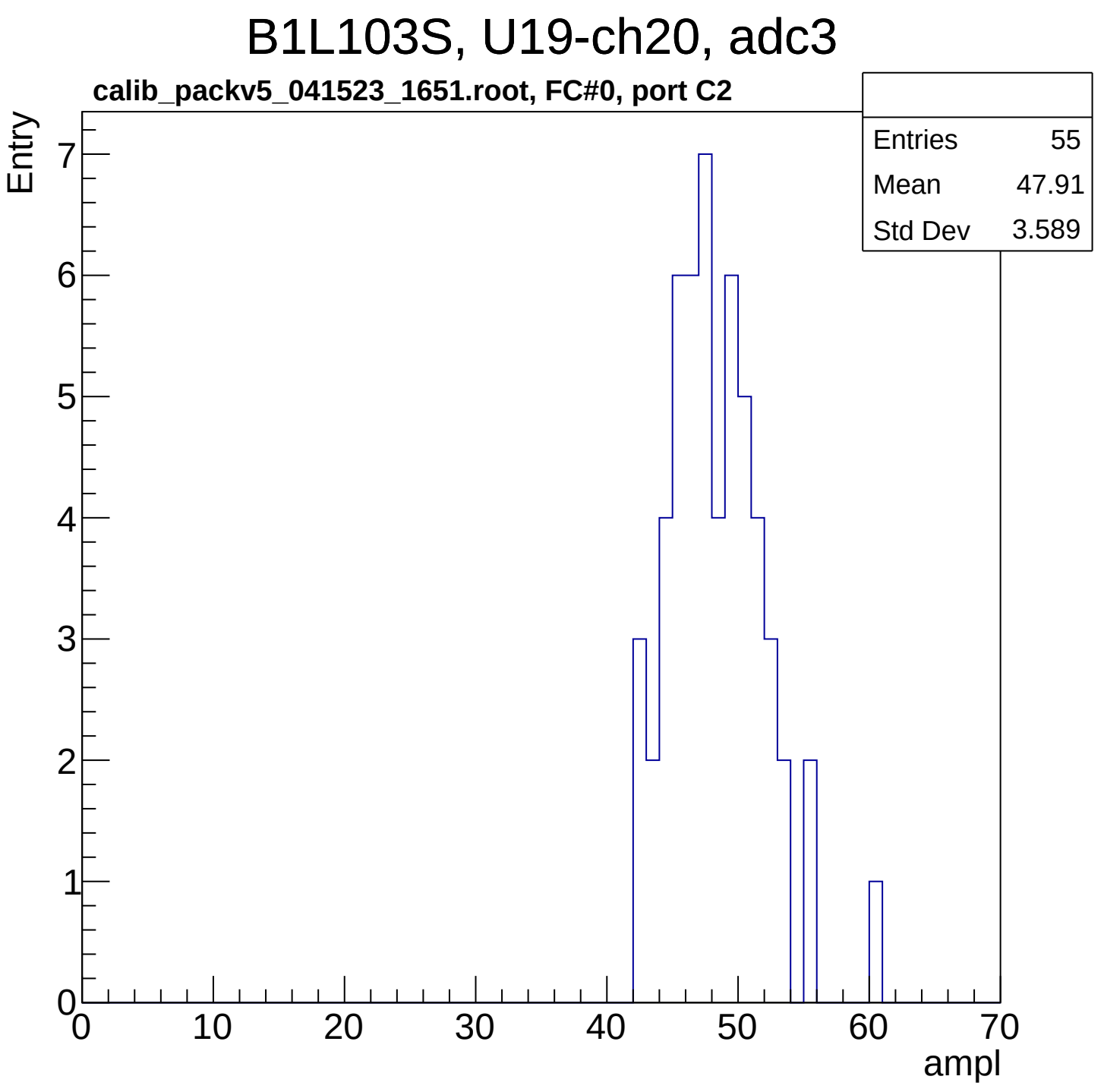
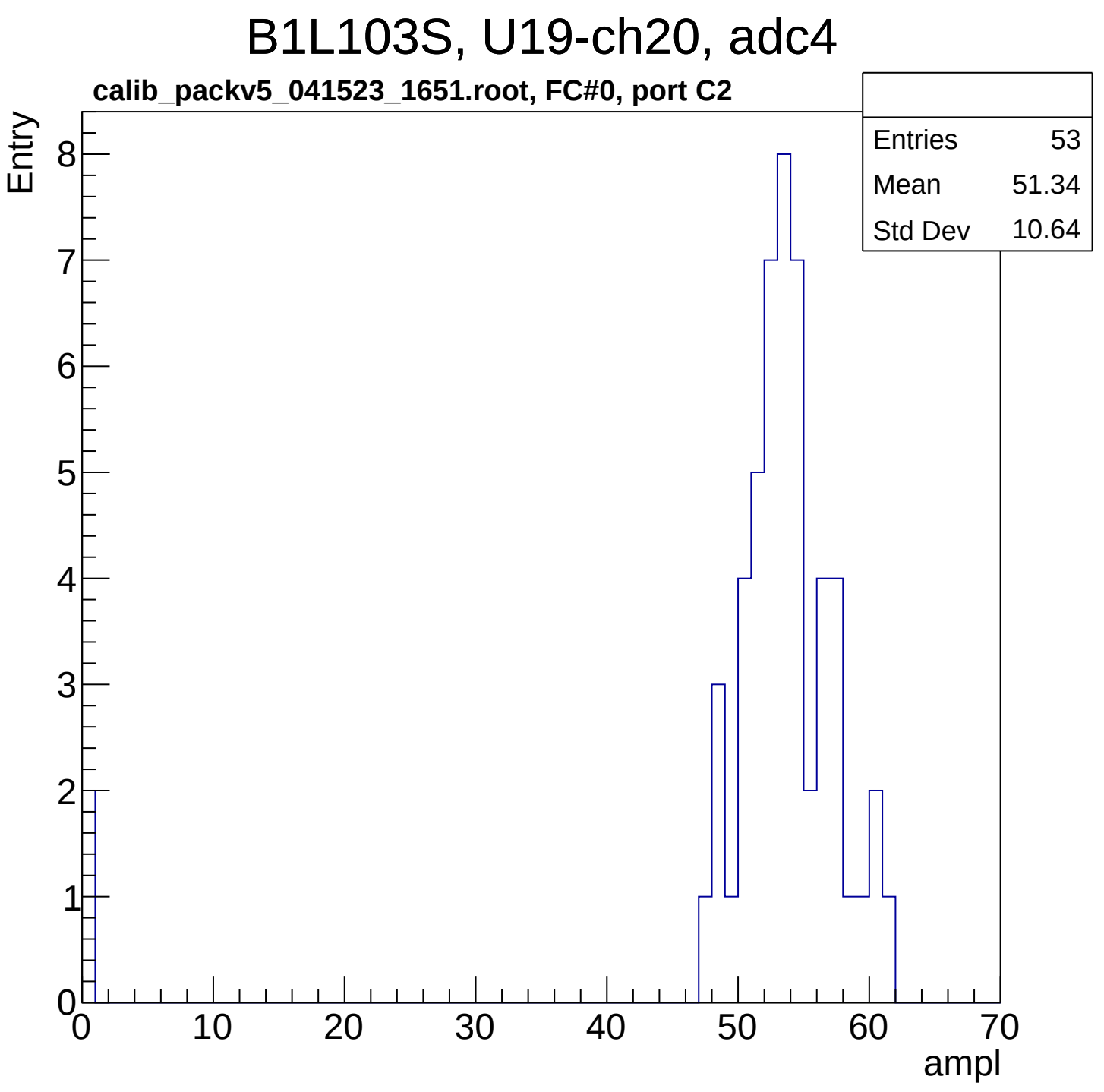
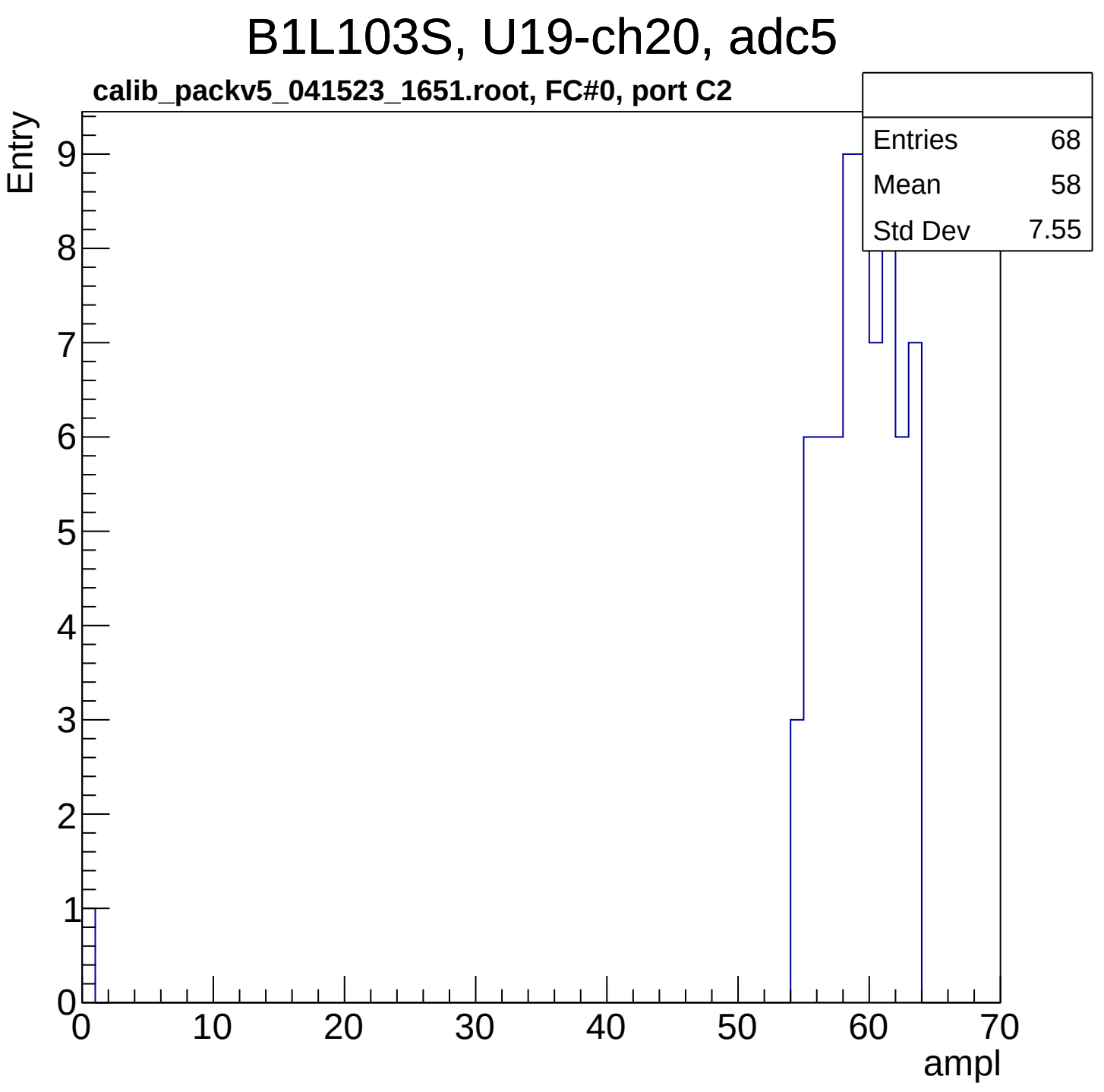
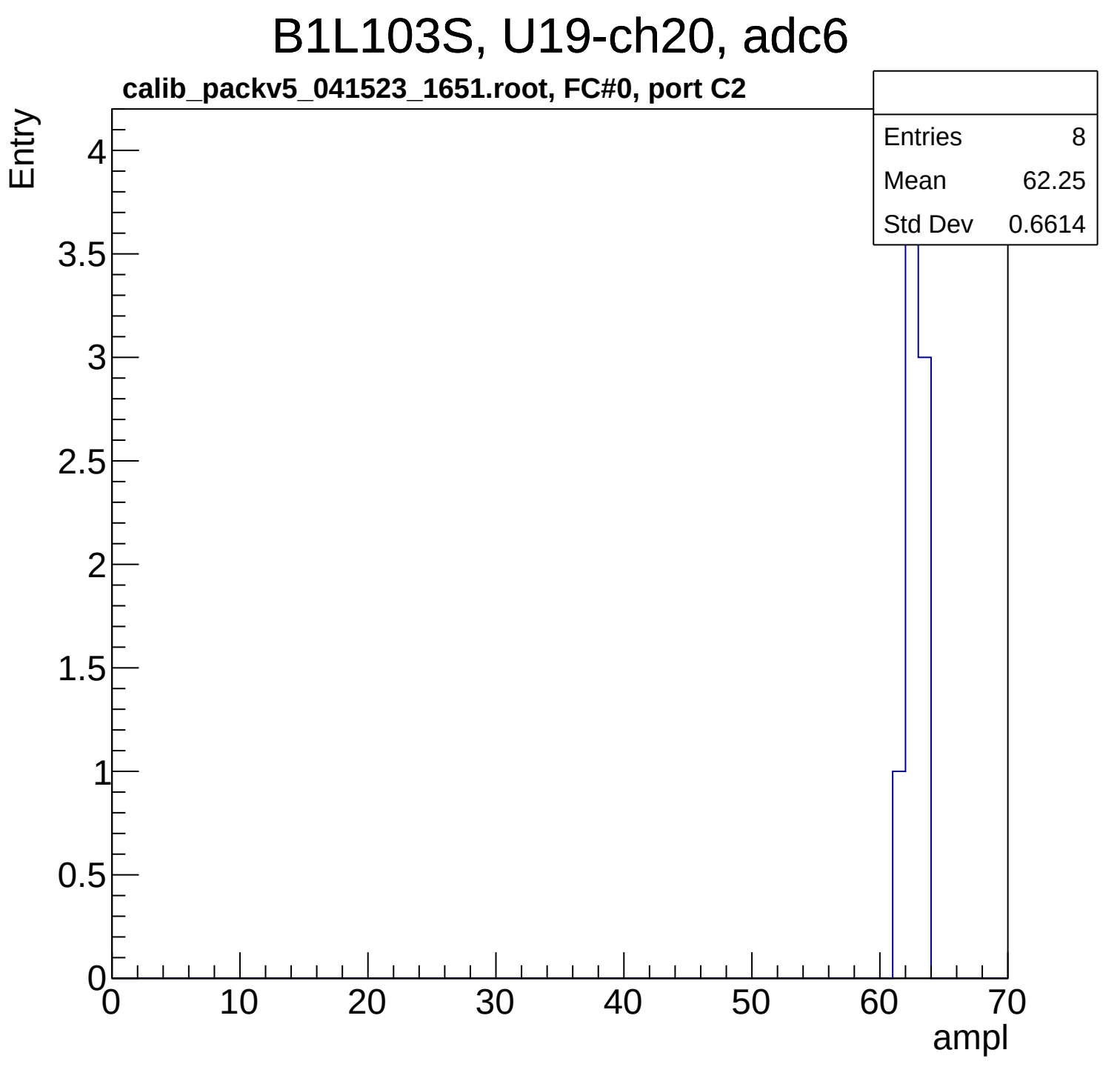

B1L103S, U19-ch20, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 47.91
Std Dev 3.589
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch20, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 51.34
Std Dev 10.64
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch20, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 58
Std Dev 7.55
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch20, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 62.25
Std Dev 0.6614
Entry
ampl
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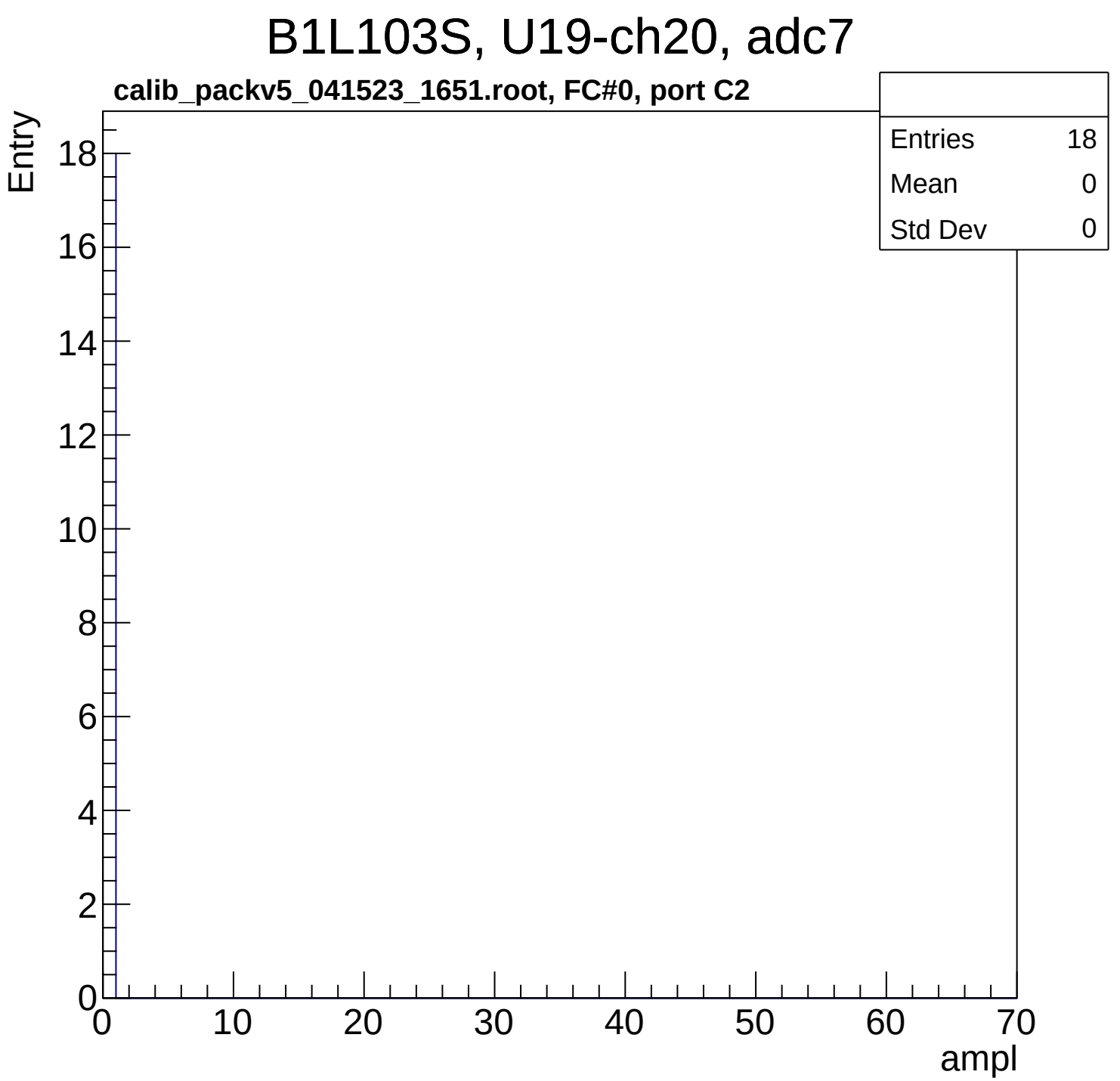
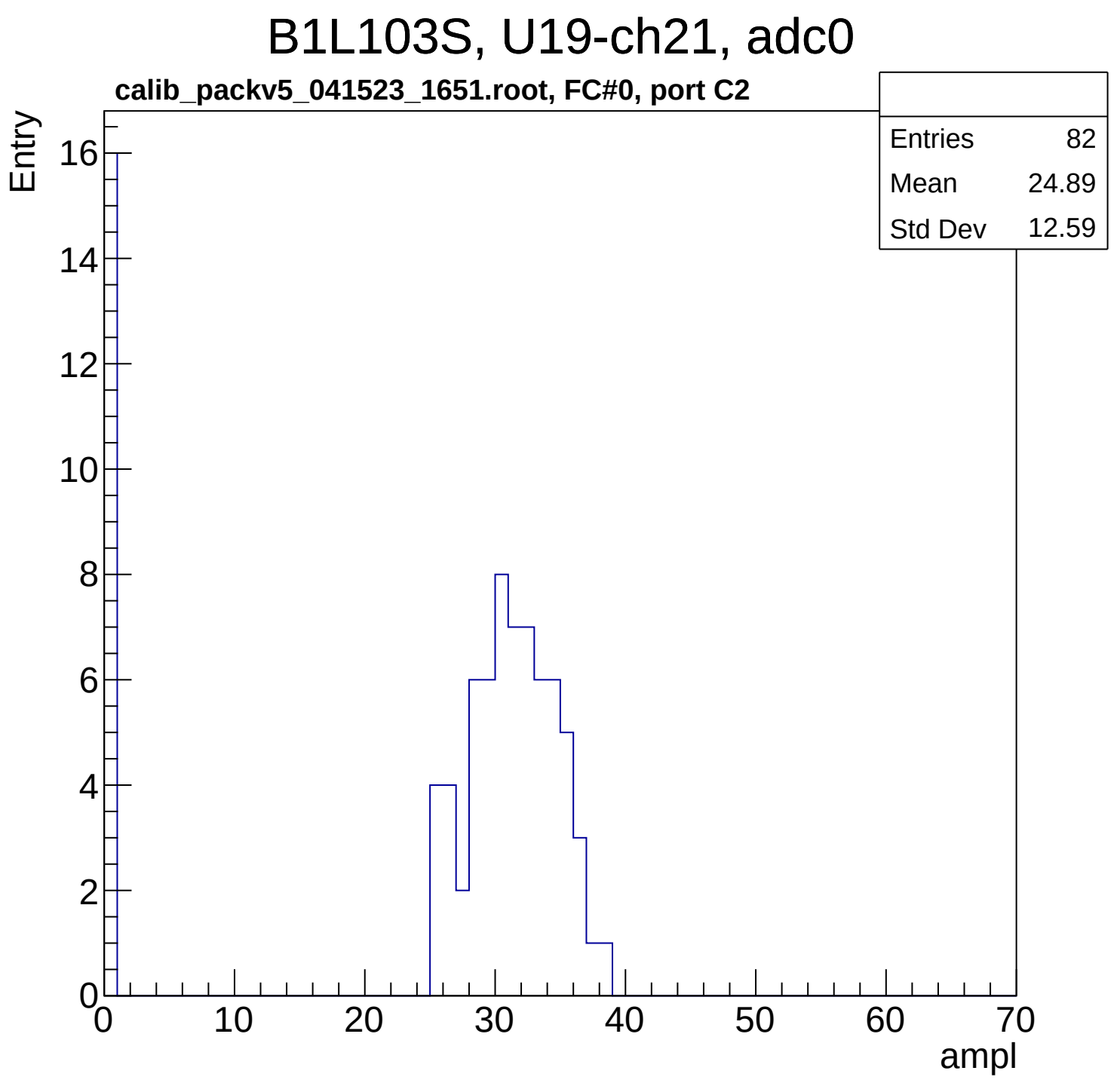
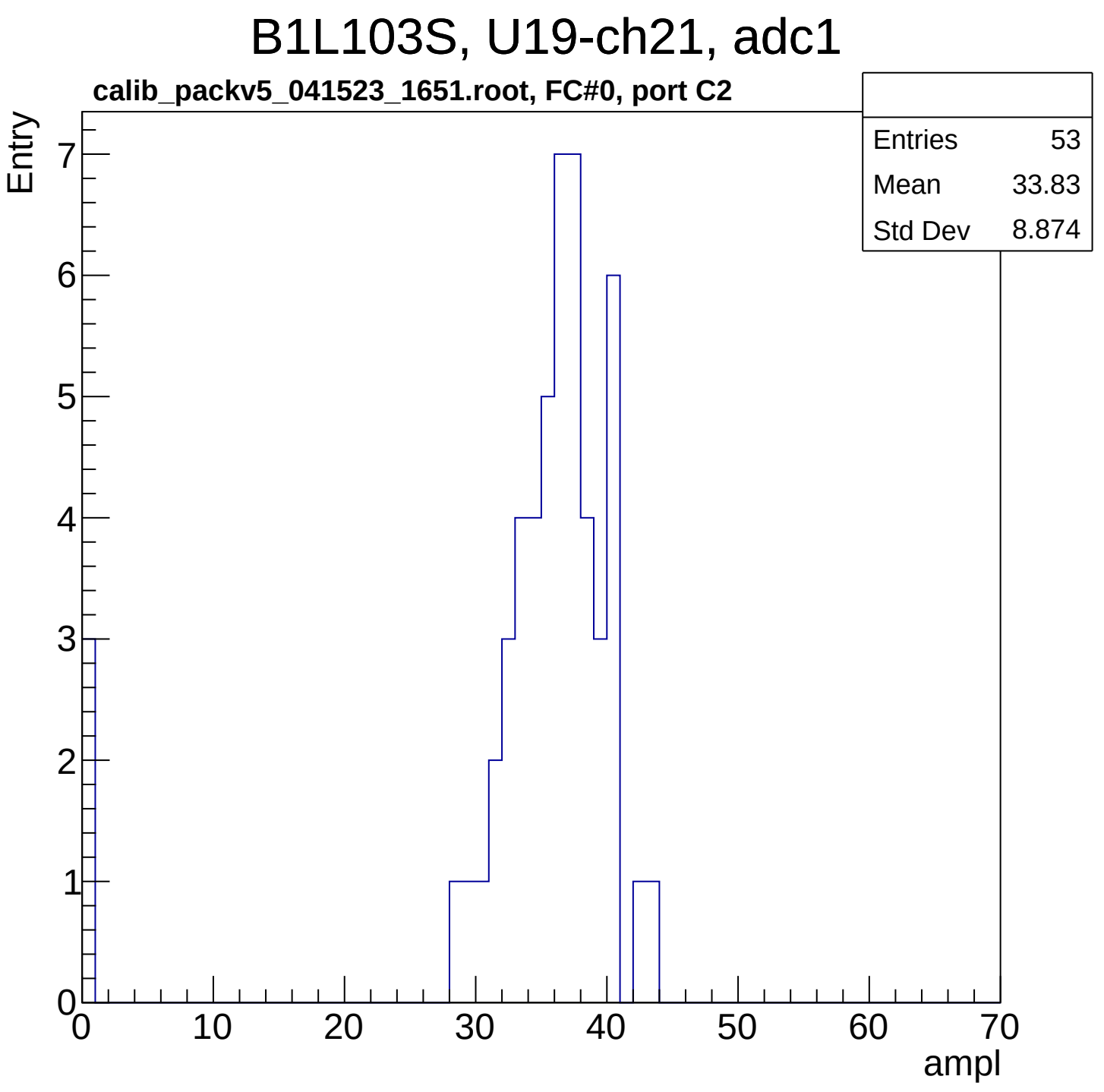
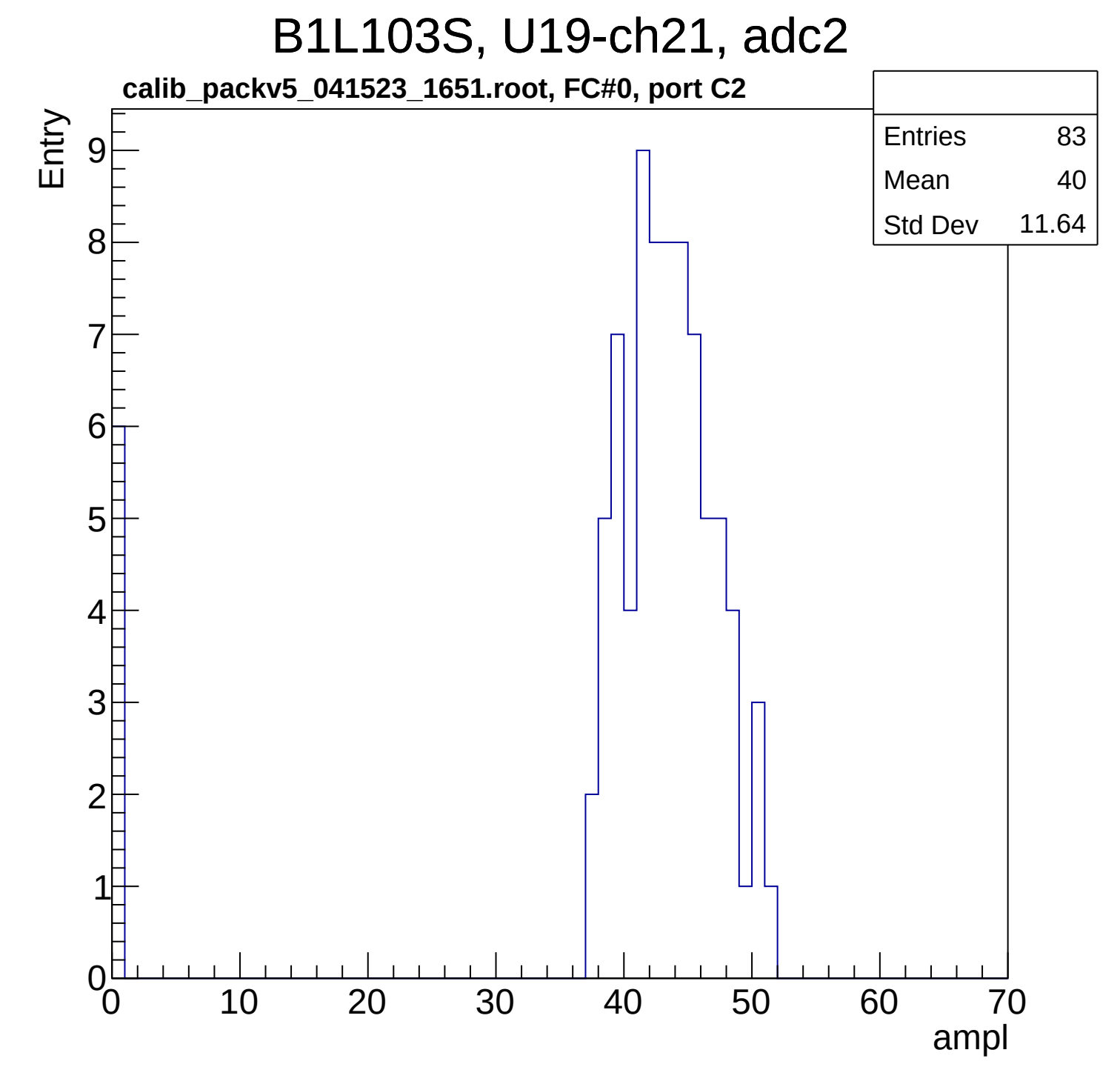
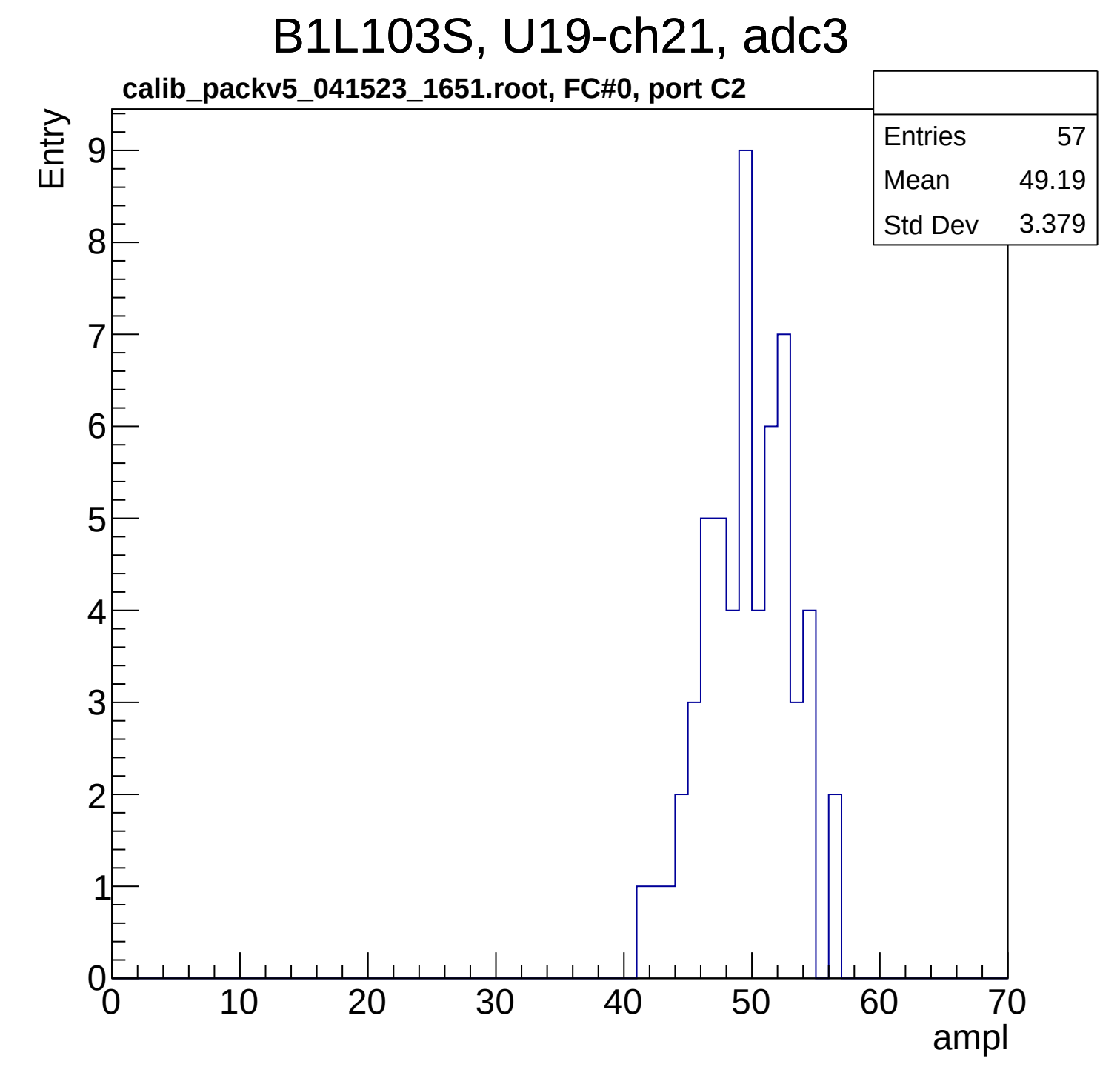
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

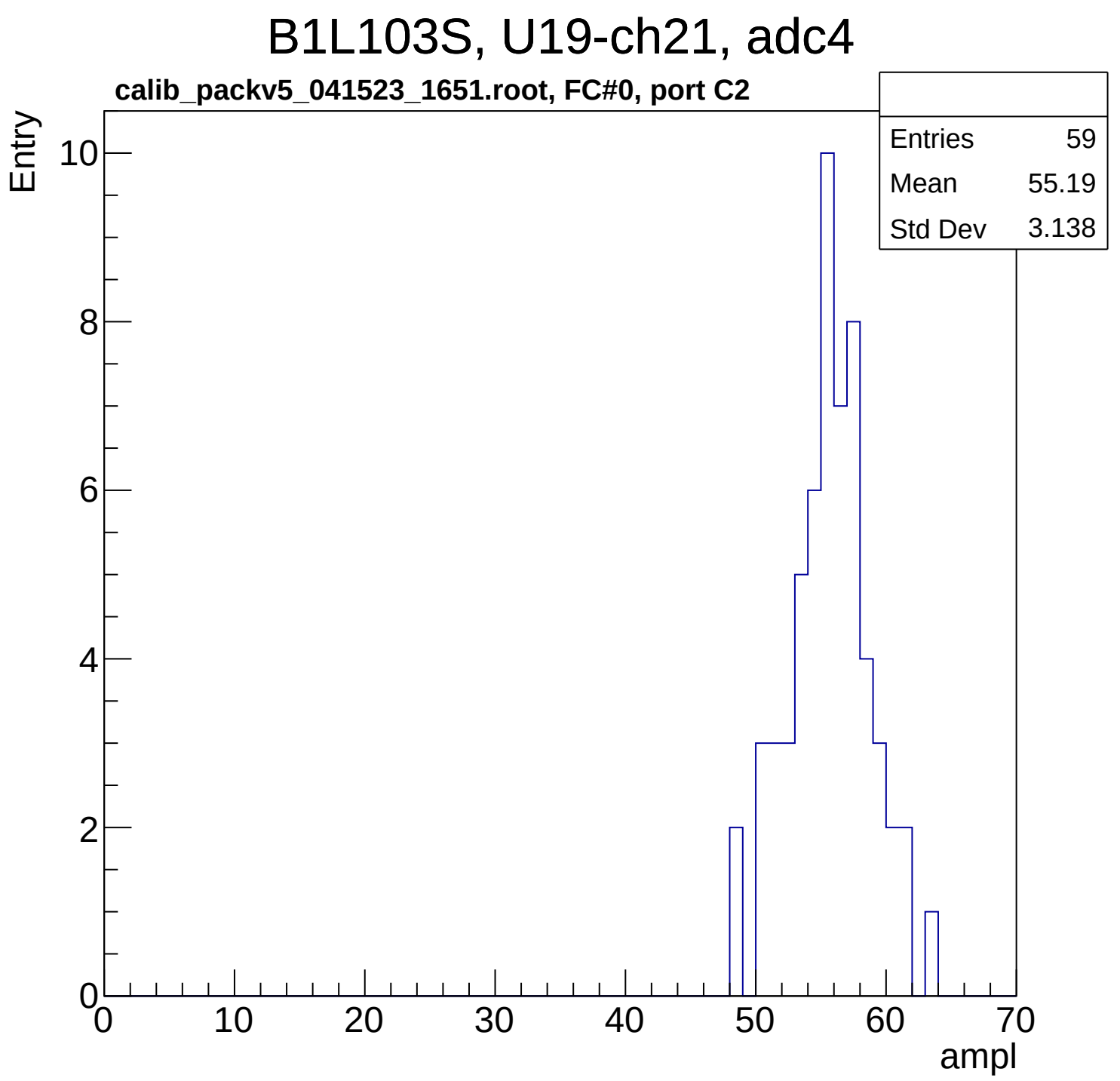

B1L103S, U19-ch20, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

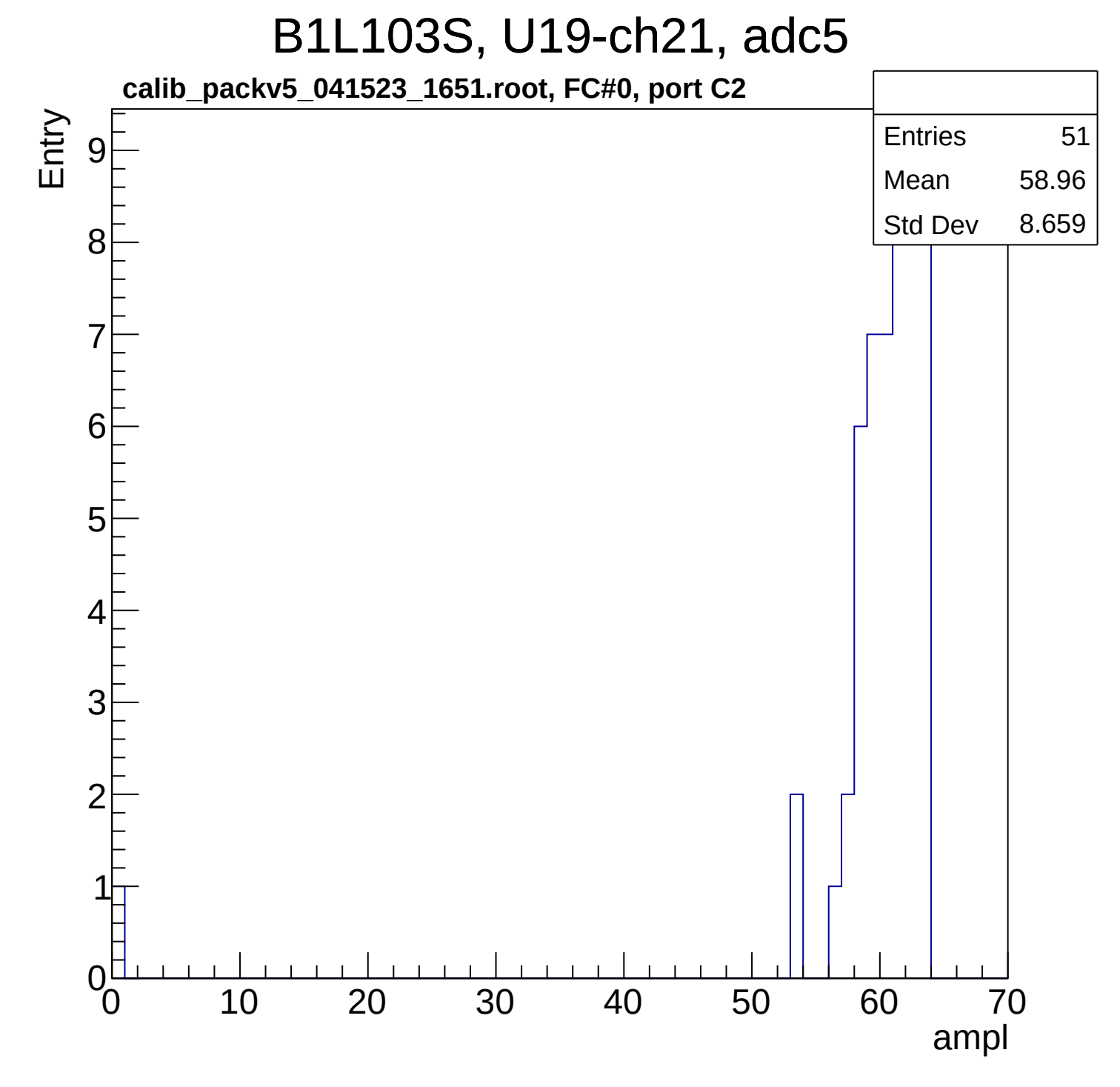

B1L103S, U19-ch21, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 24.89
Std Dev 12.59
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

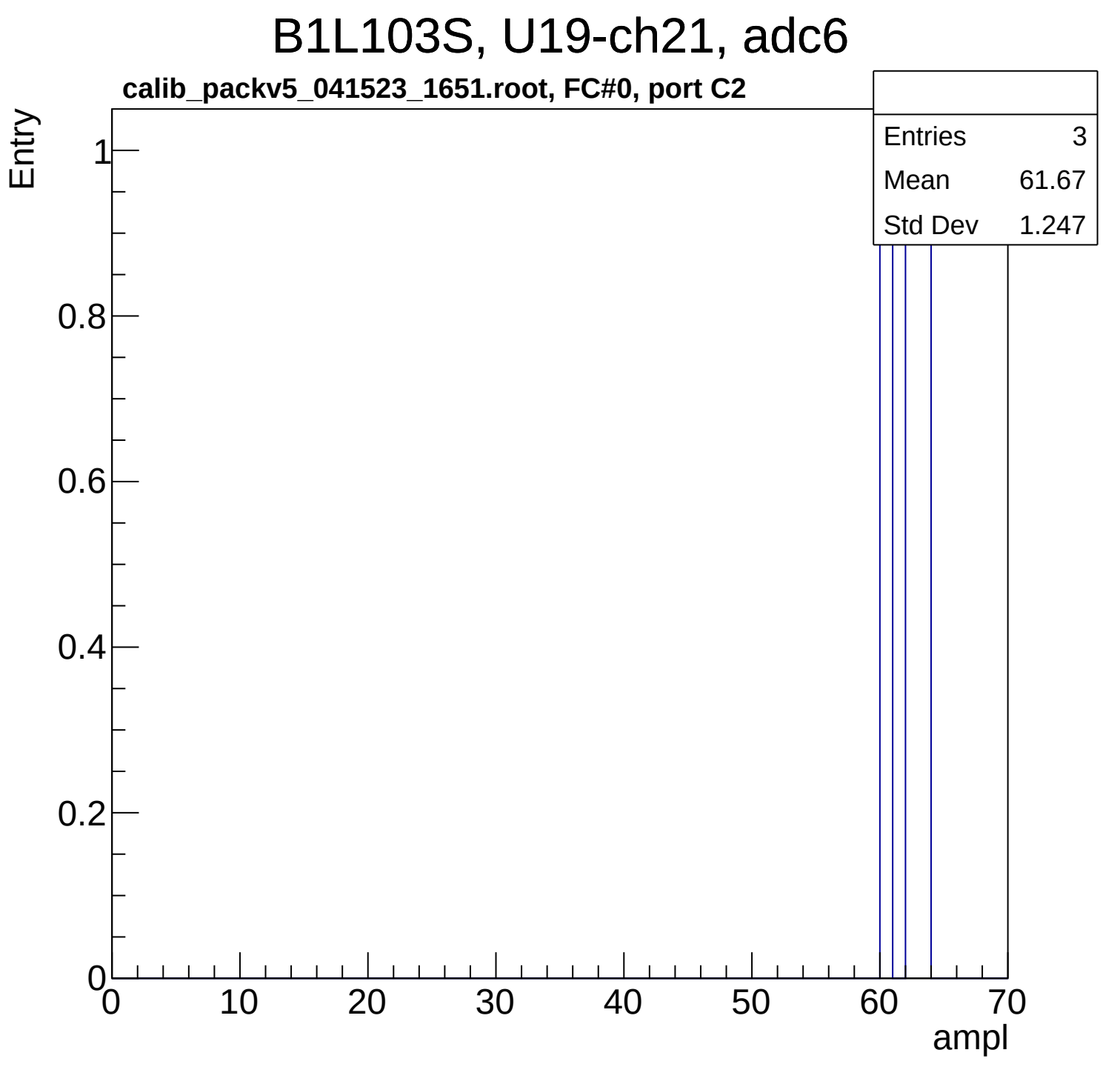

B1L103S, U19-ch21, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 33.83
Std Dev 8.874
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch21, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 40
Std Dev 11.64
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch21, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 49.19
Std Dev 3.379
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch21, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 55.19
Std Dev 3.138
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch21, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 58.96
Std Dev 8.659
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch21, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 61.67
Std Dev 1.247
Entry
ampl
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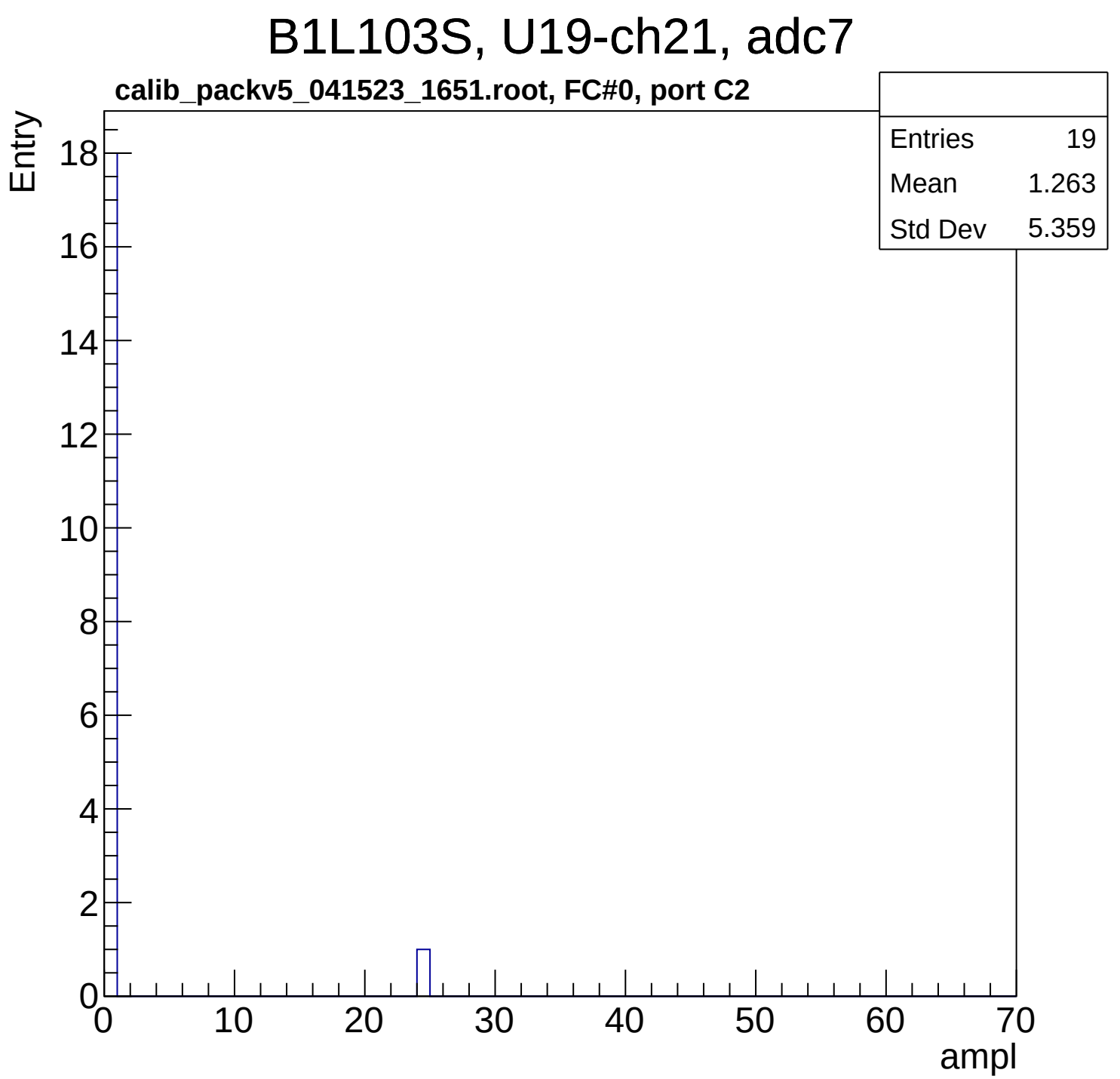
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B1L103S, U19-ch21, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.263
Std Dev 5.359
Entry
0
2
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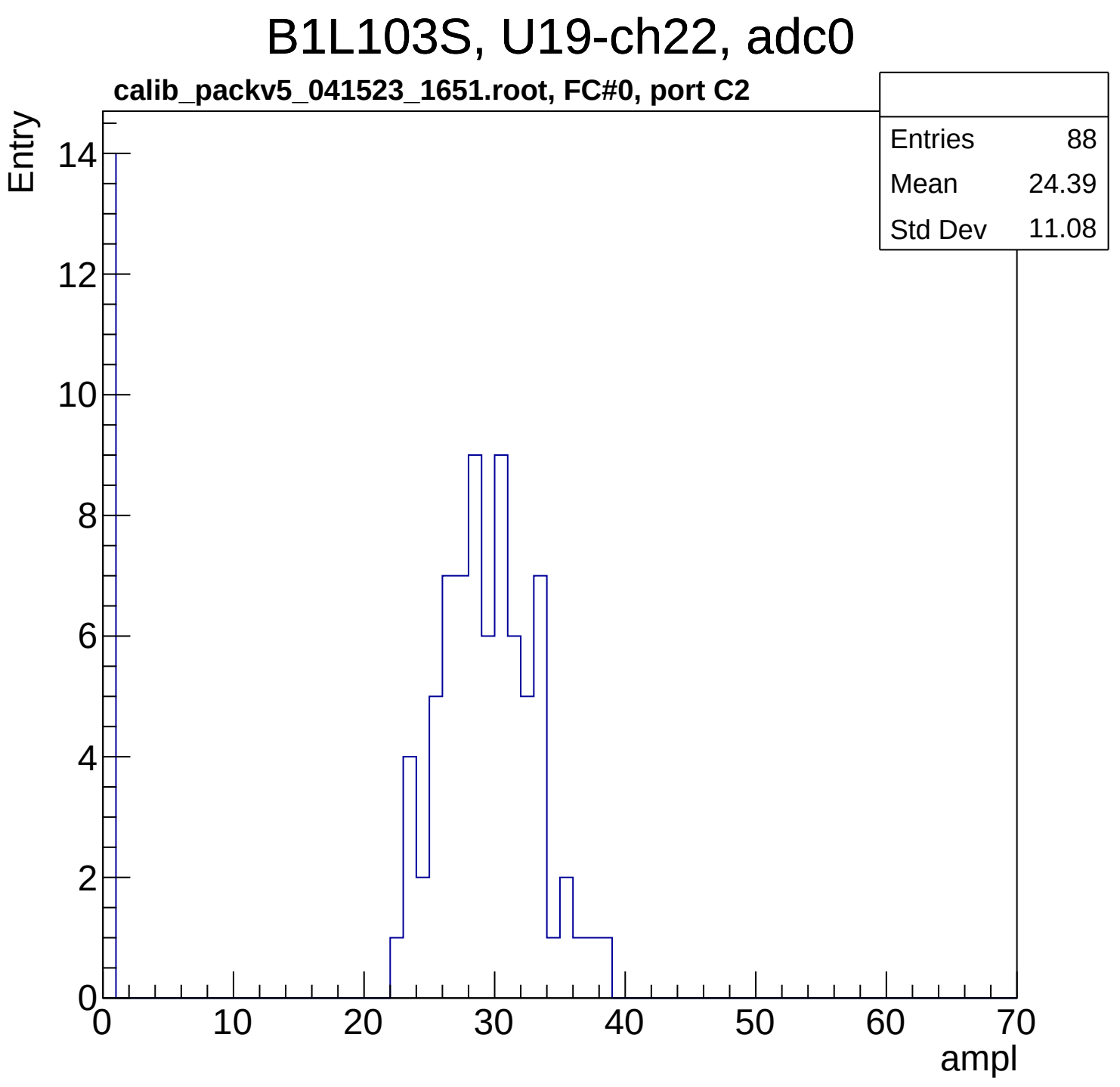
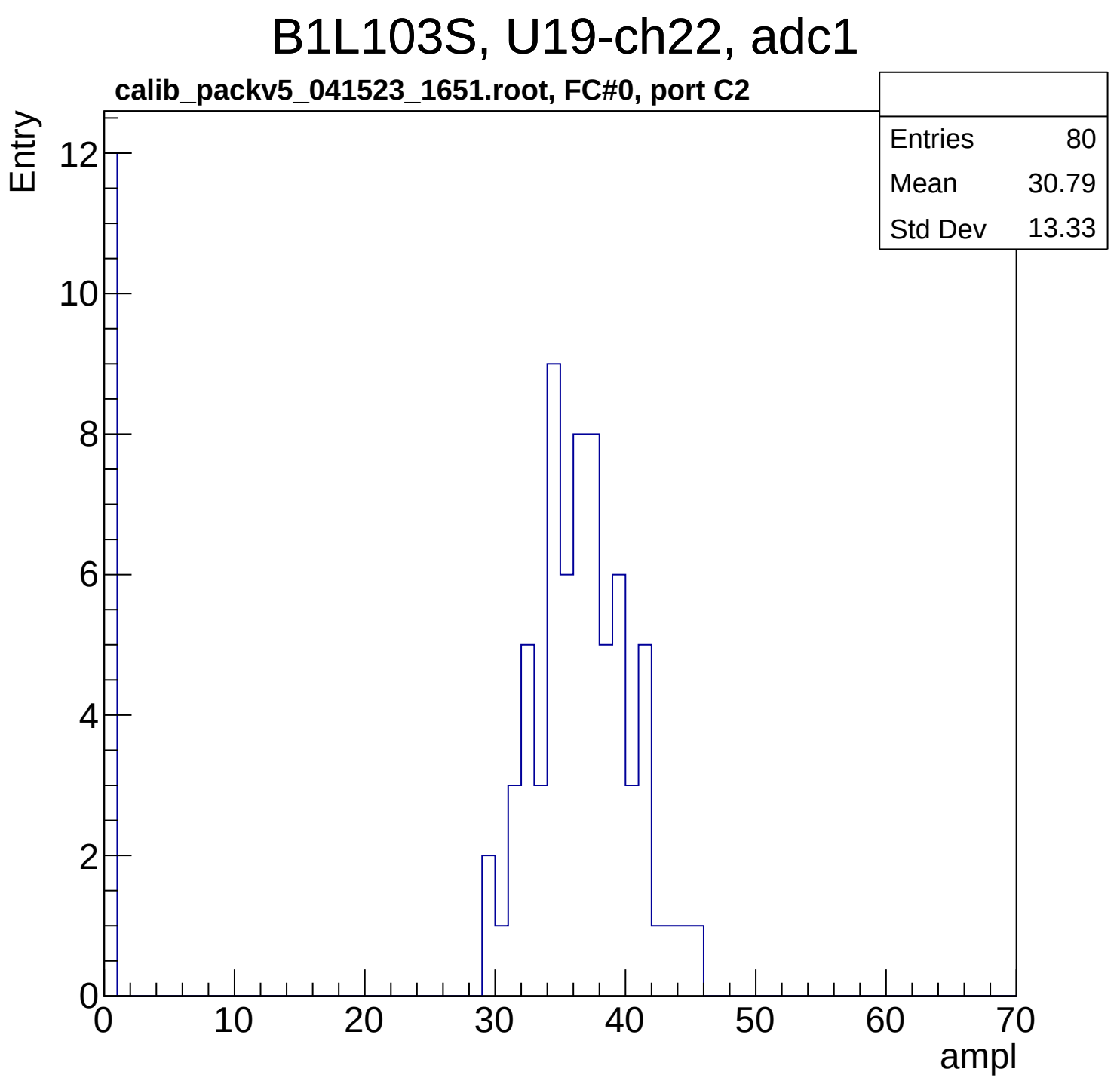
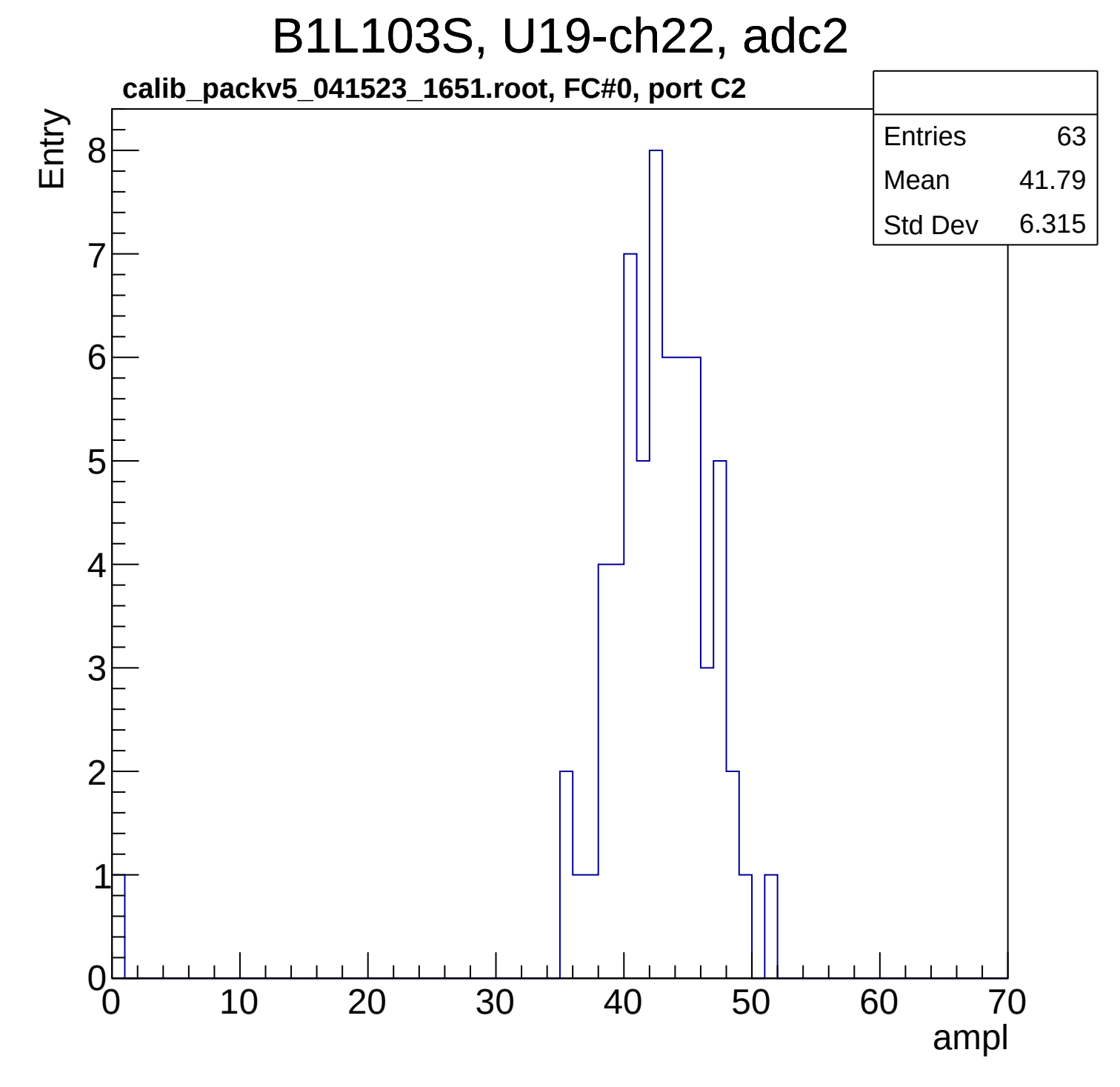
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch22, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 24.39
Std Dev 11.08
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U19-ch22, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 30.79
Std Dev 13.33
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch22, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 41.79
Std Dev 6.315
Entry
ampl
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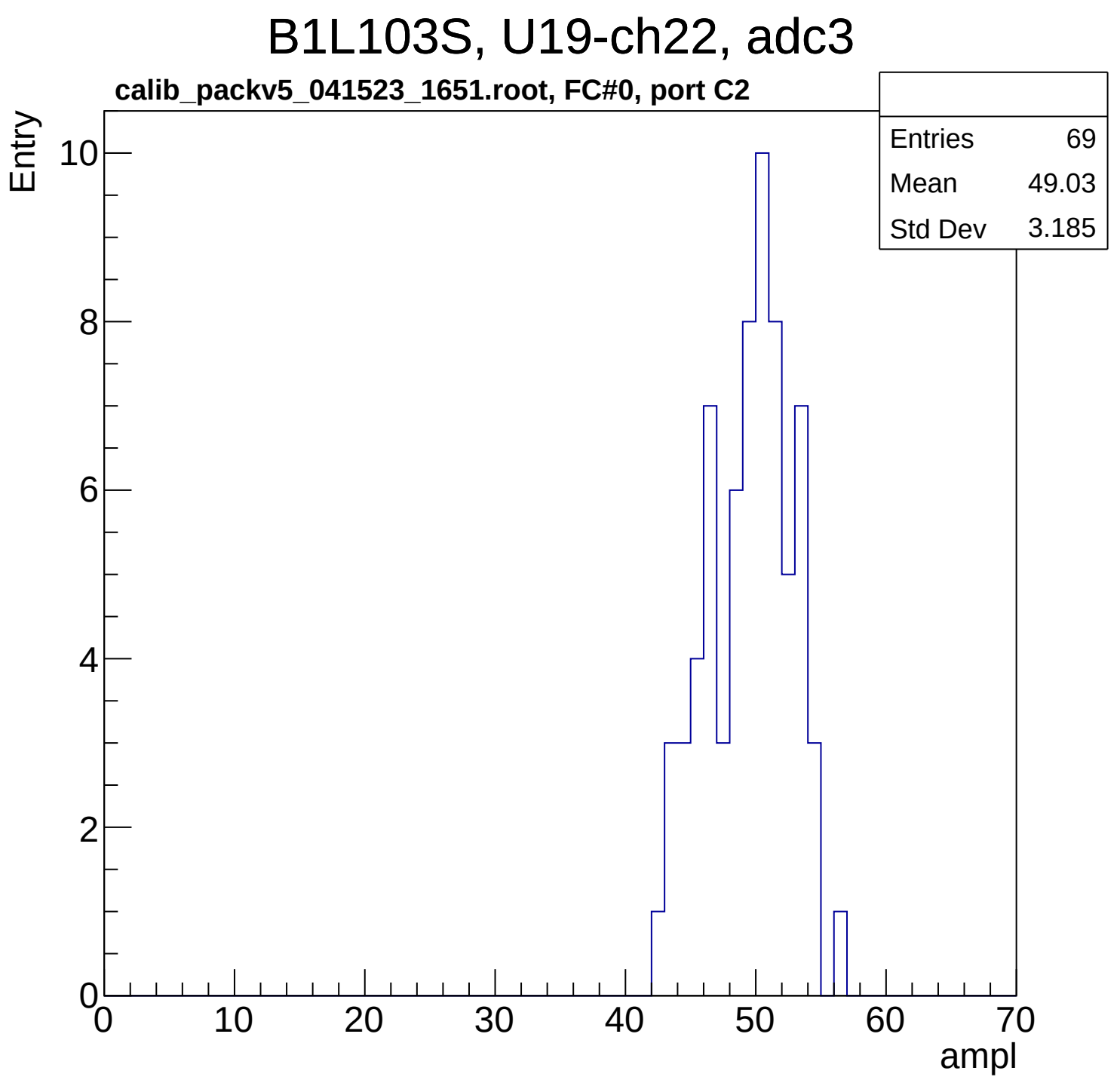
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch22, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 49.03
Std Dev 3.185
Entry
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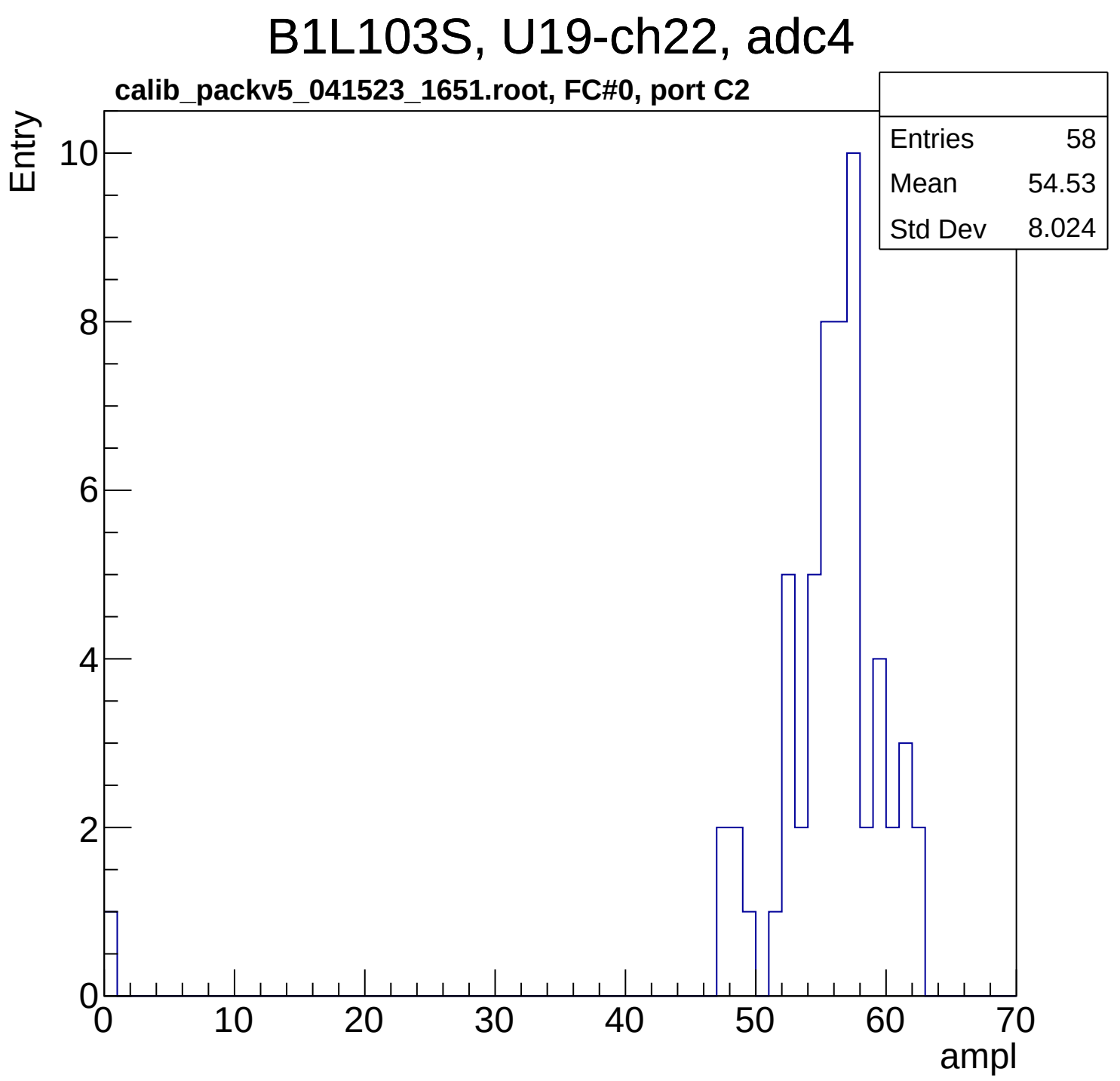
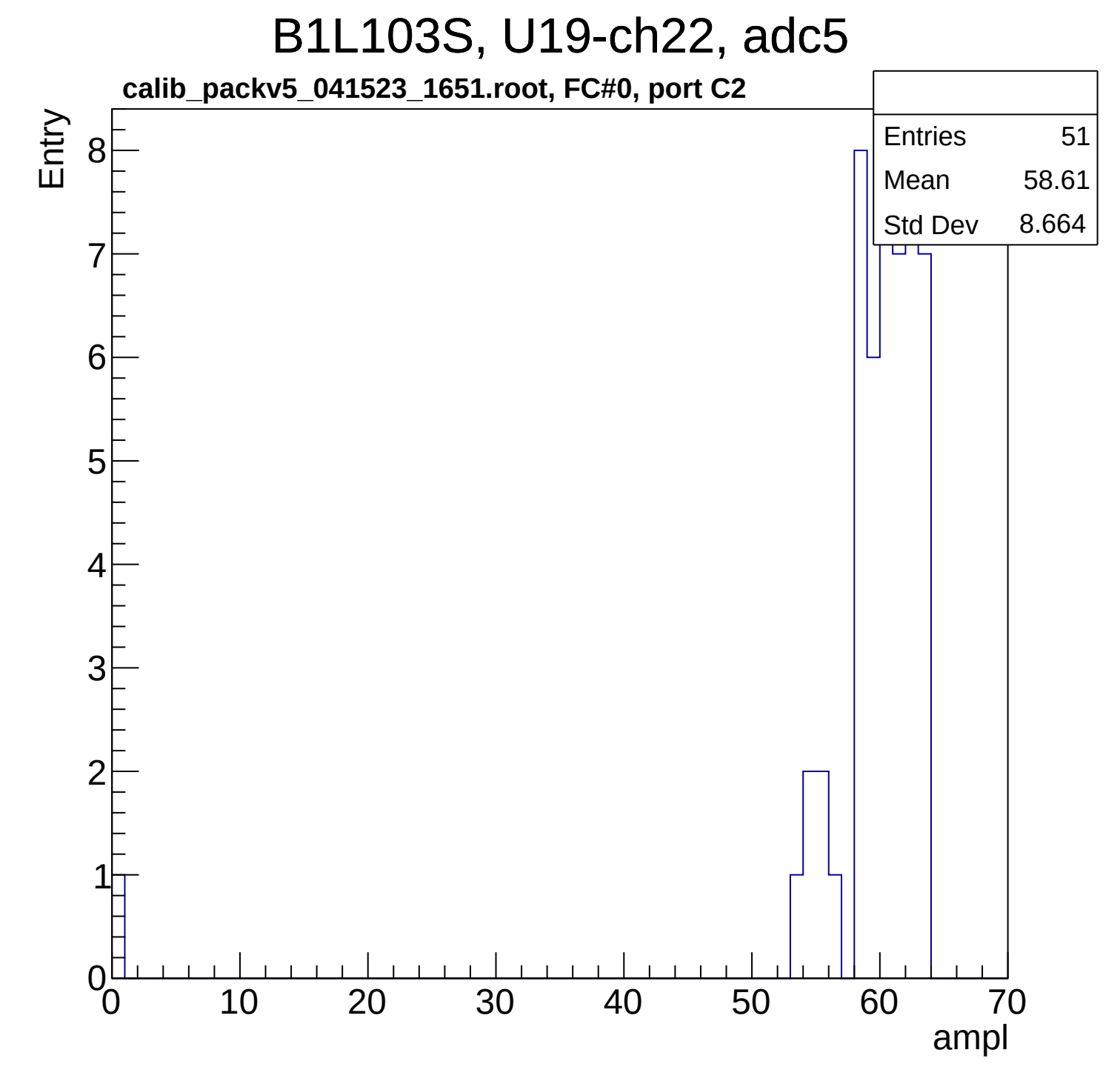
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch22, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 54.53
Std Dev 8.024
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch22, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 58.61
Std Dev 8.664
Entry
ampl
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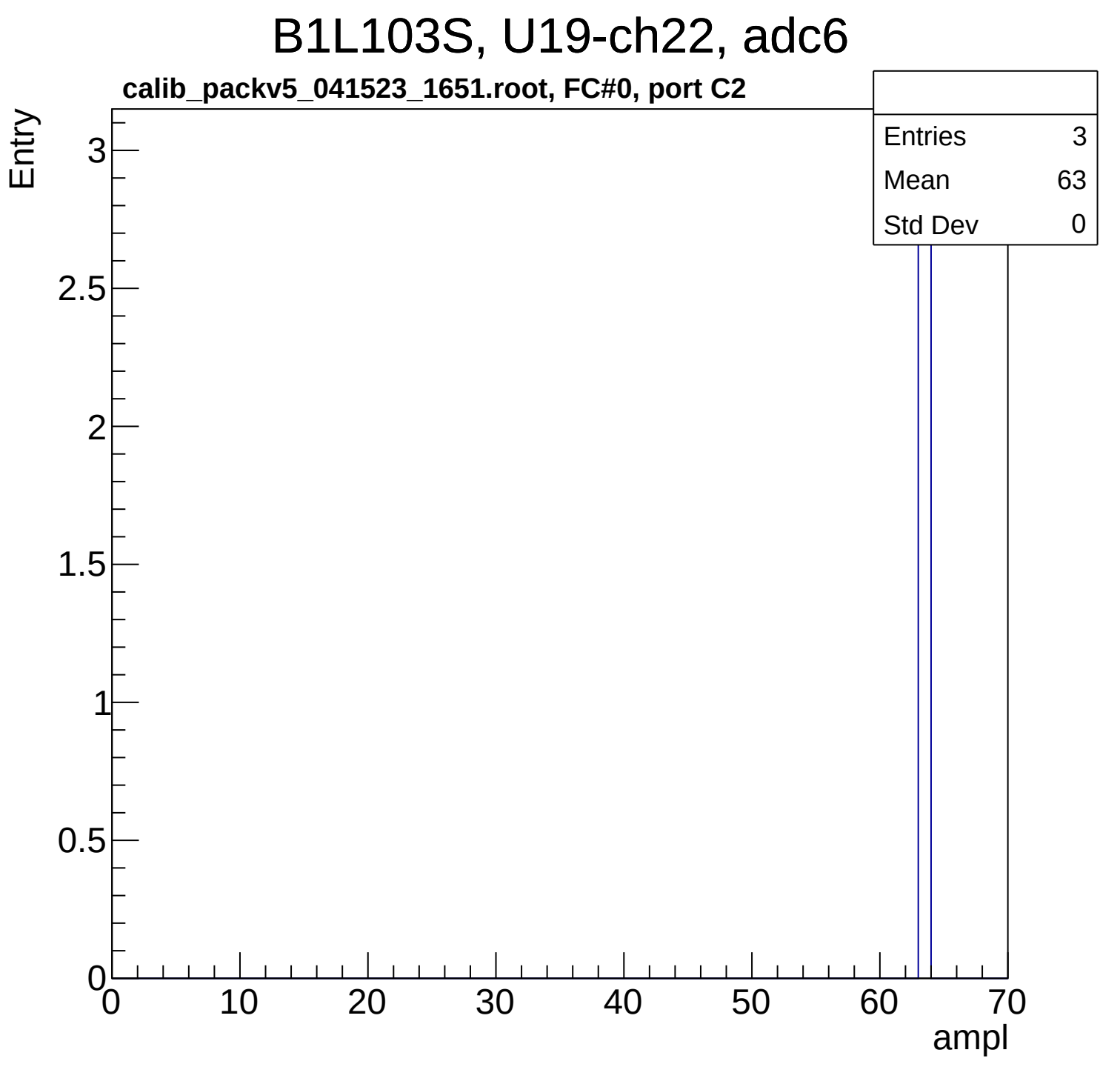
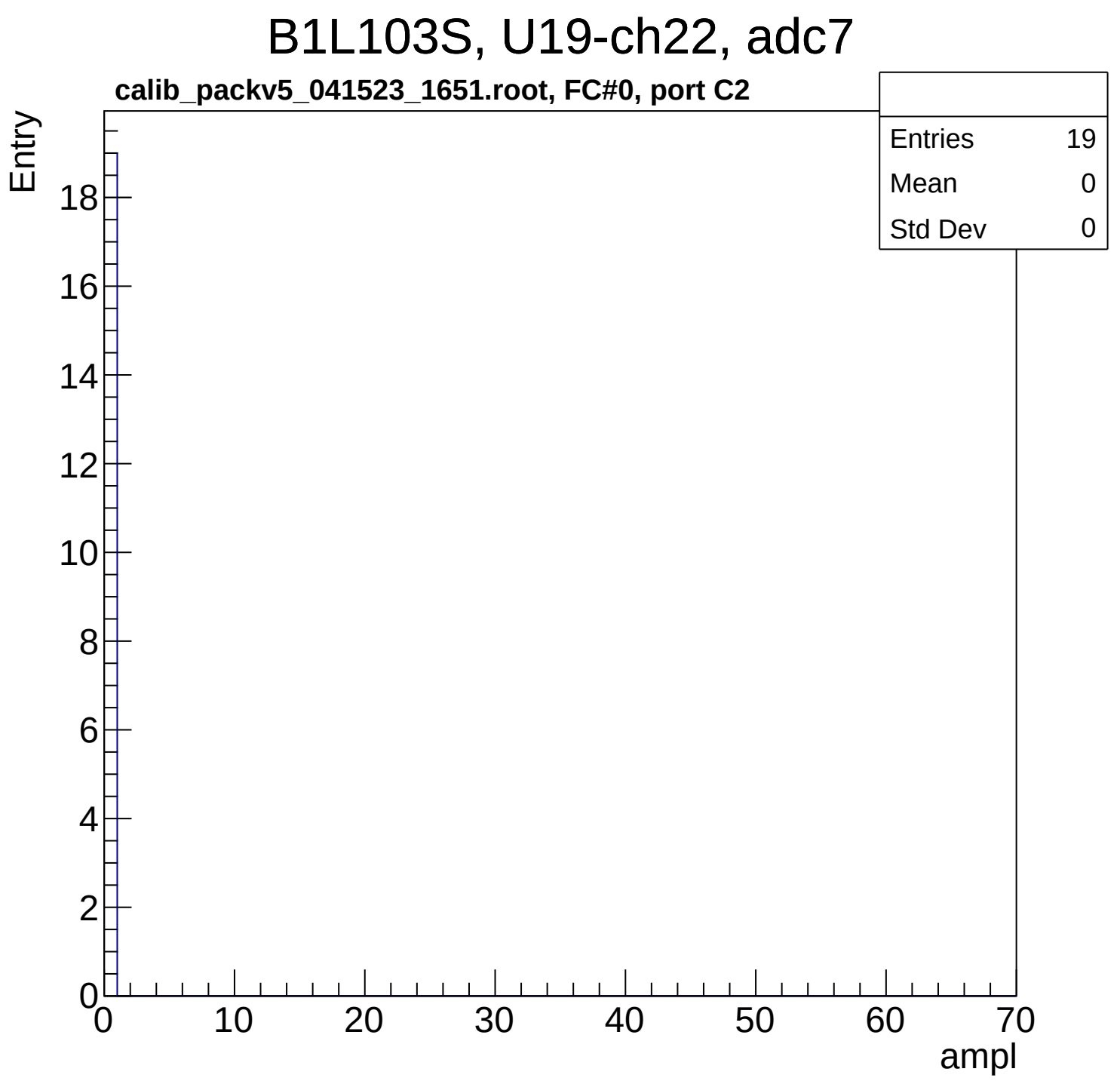
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch22, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 63
Std Dev 0
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U19-ch22, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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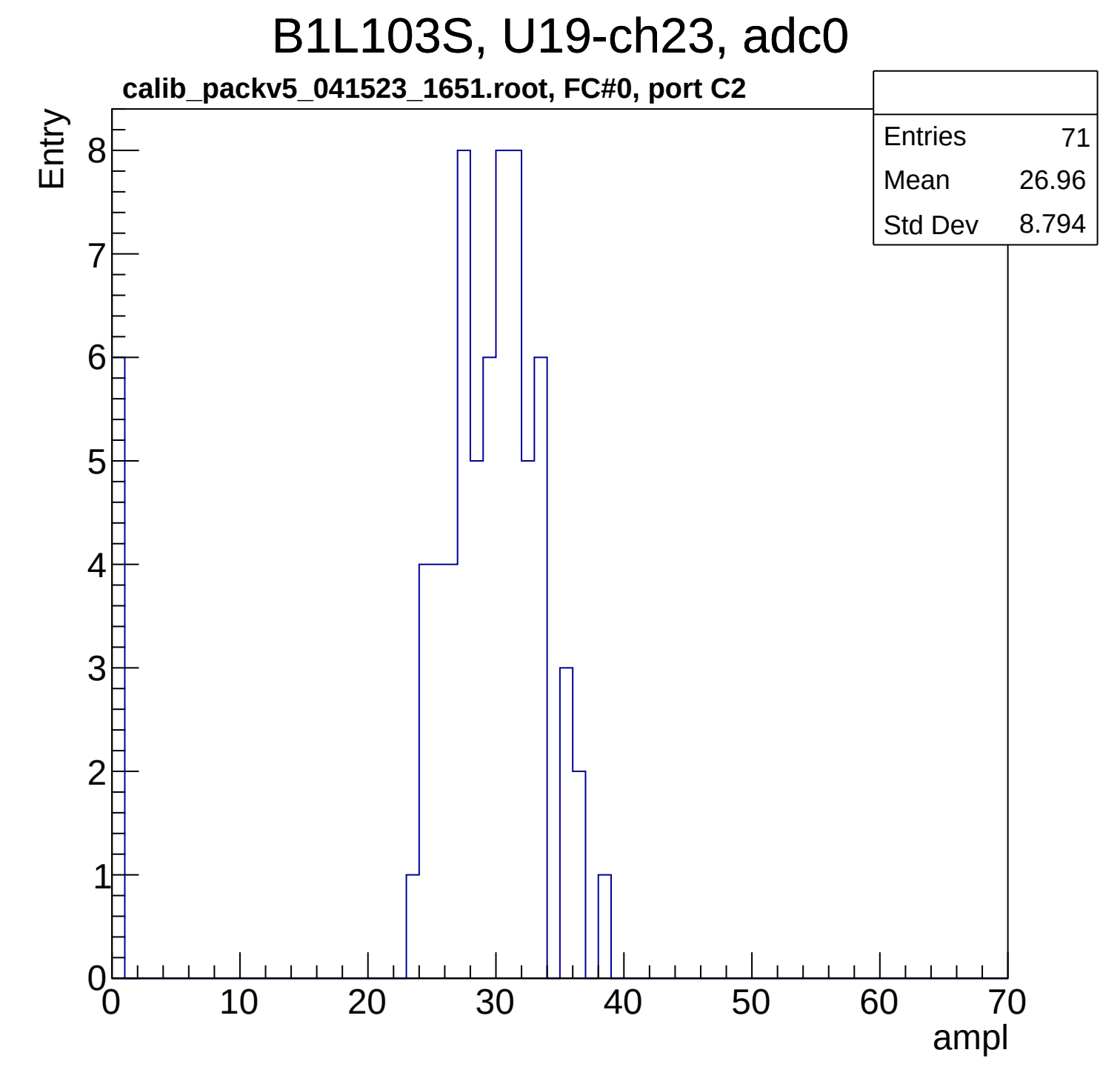
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch23, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 26.96
Std Dev 8.794
Entry
ampl
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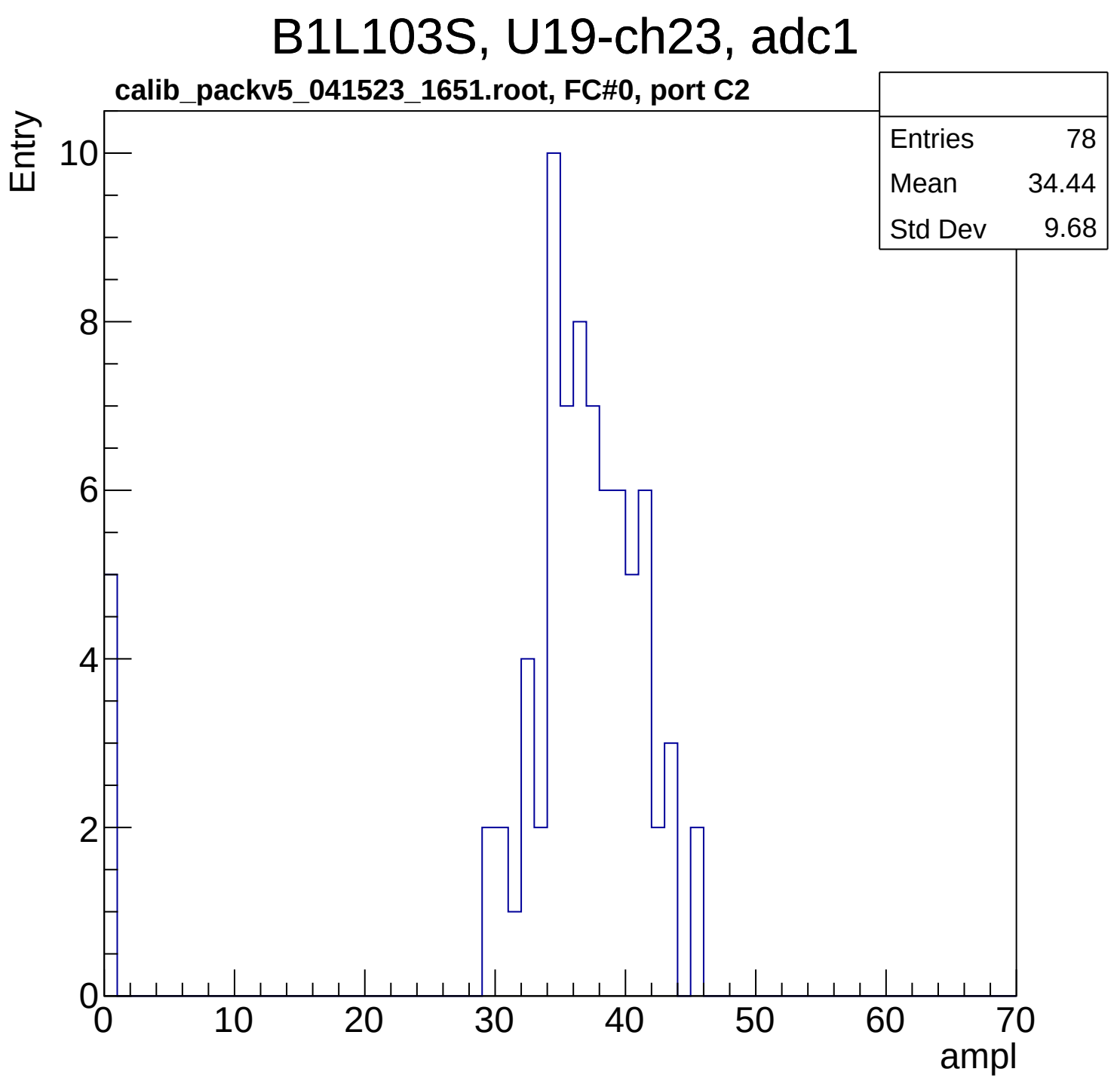
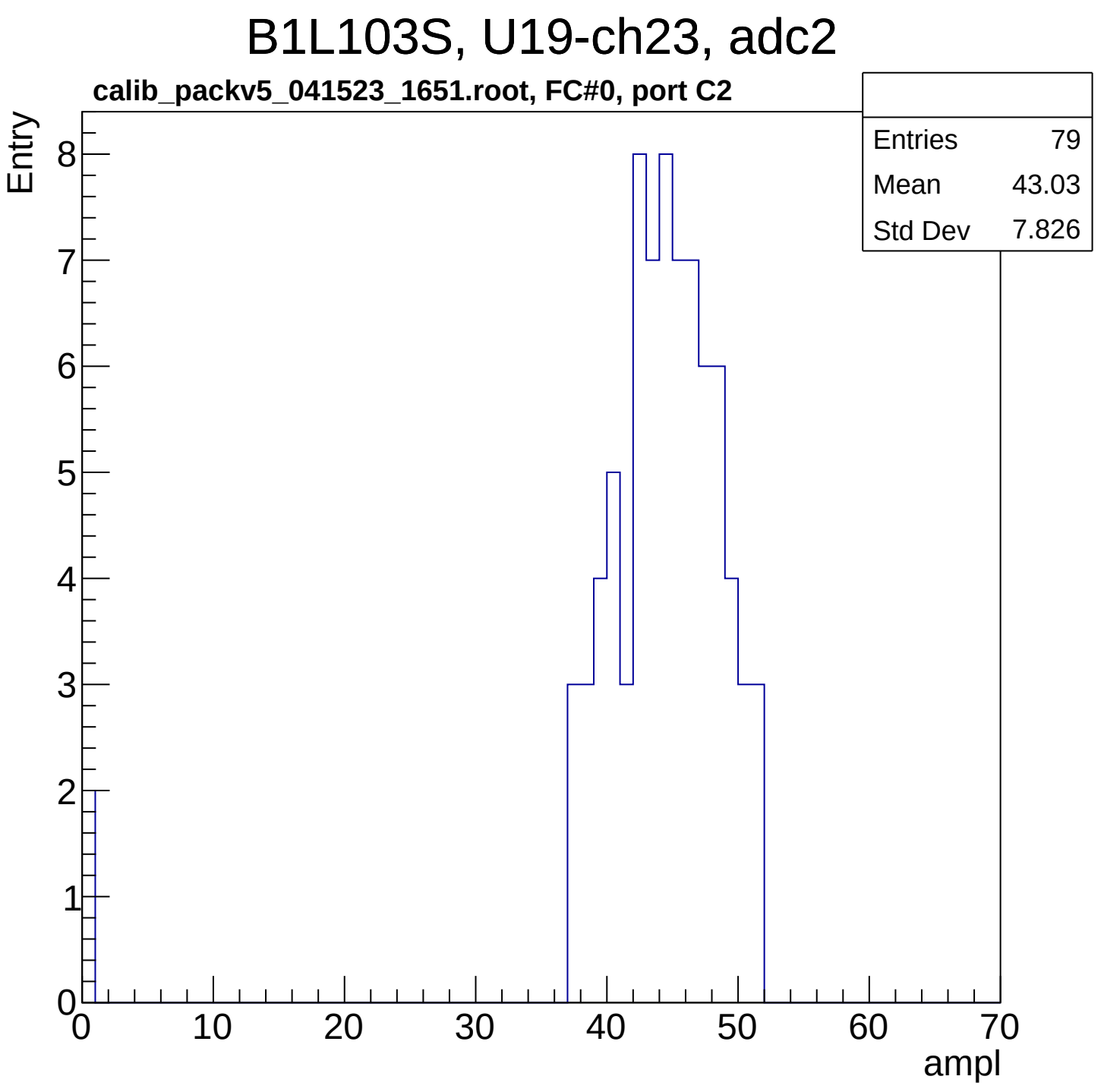
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch23, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 34.44
Std Dev 9.68
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U19-ch23, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 43.03
Std Dev 7.826
Entry
ampl
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5
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0
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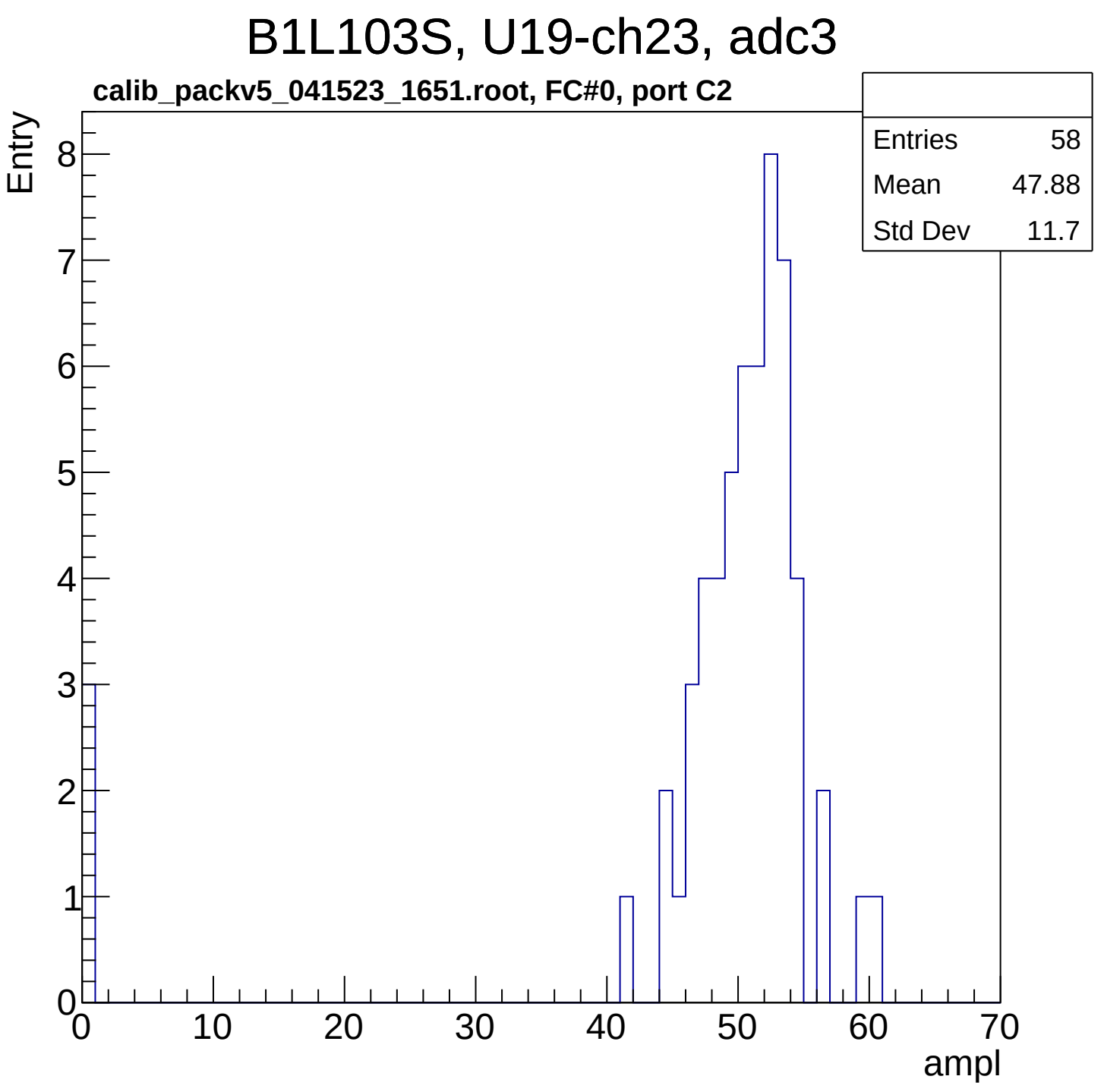
B1L103S, U19-ch23, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 47.88
Std Dev 11.7
Entry
ampl
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4
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7
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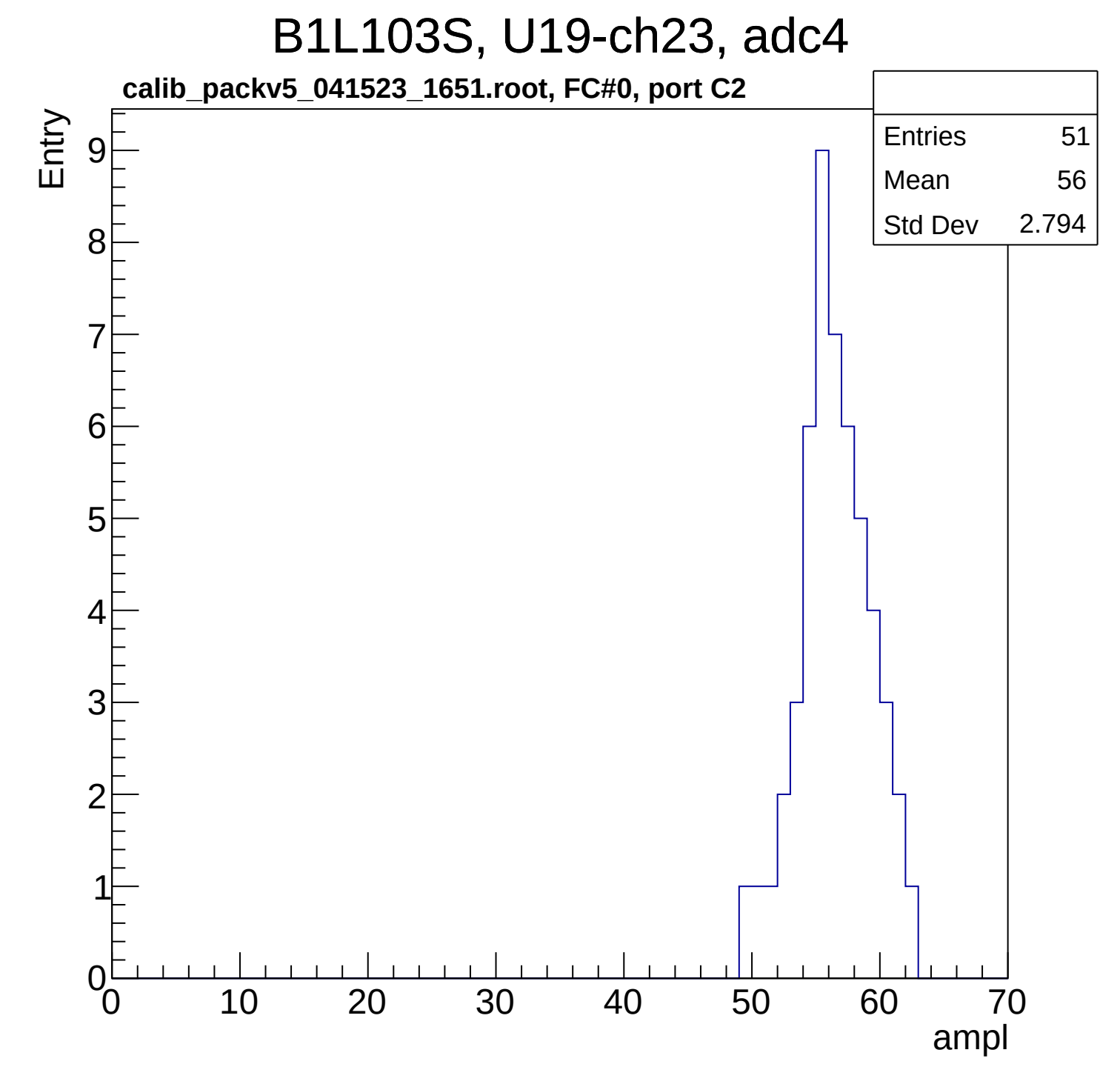
B1L103S, U19-ch23, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 56
Std Dev 2.794
Entry
ampl
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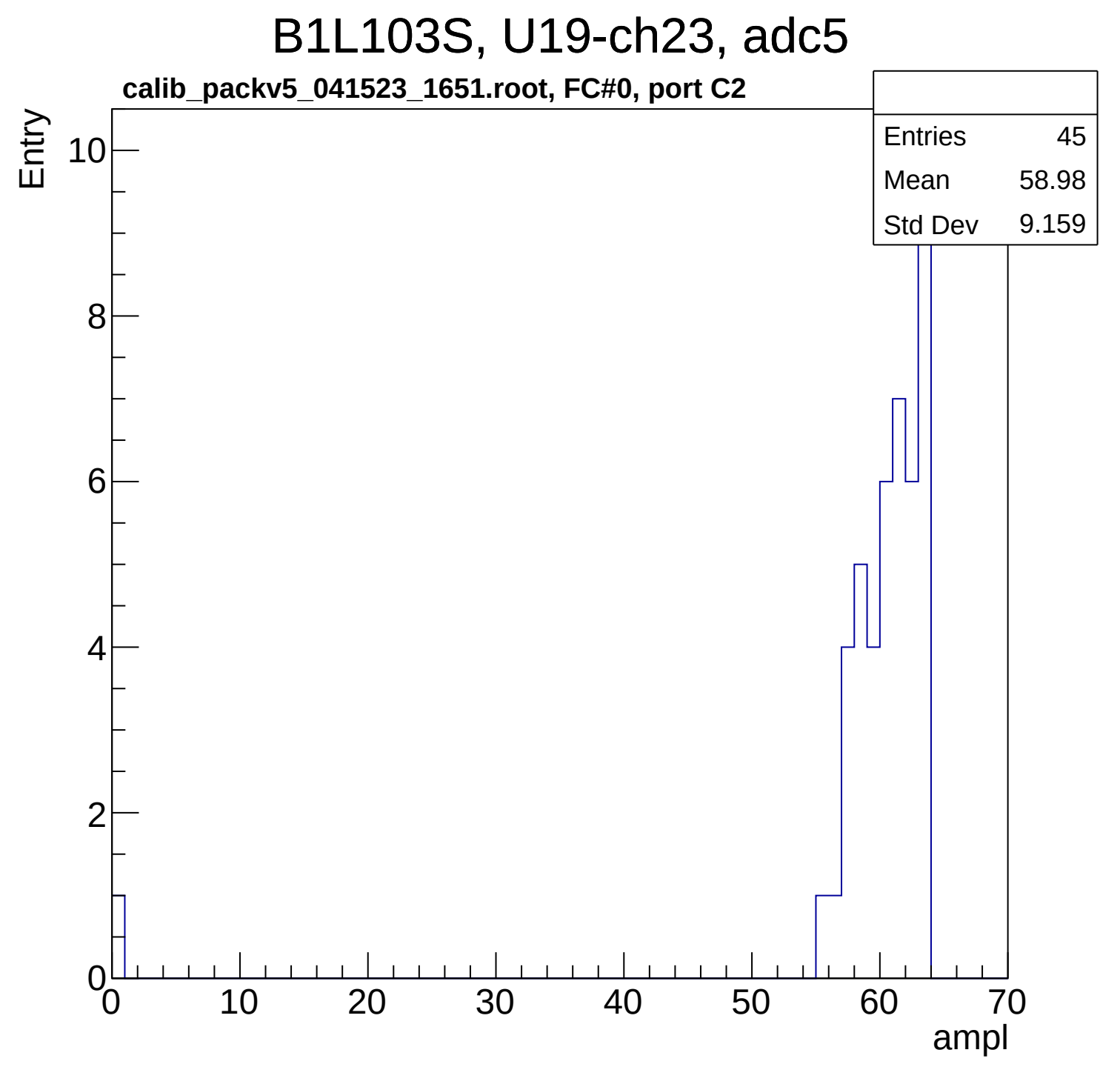
B1L103S, U19-ch23, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 58.98
Std Dev 9.159
Entry
ampl
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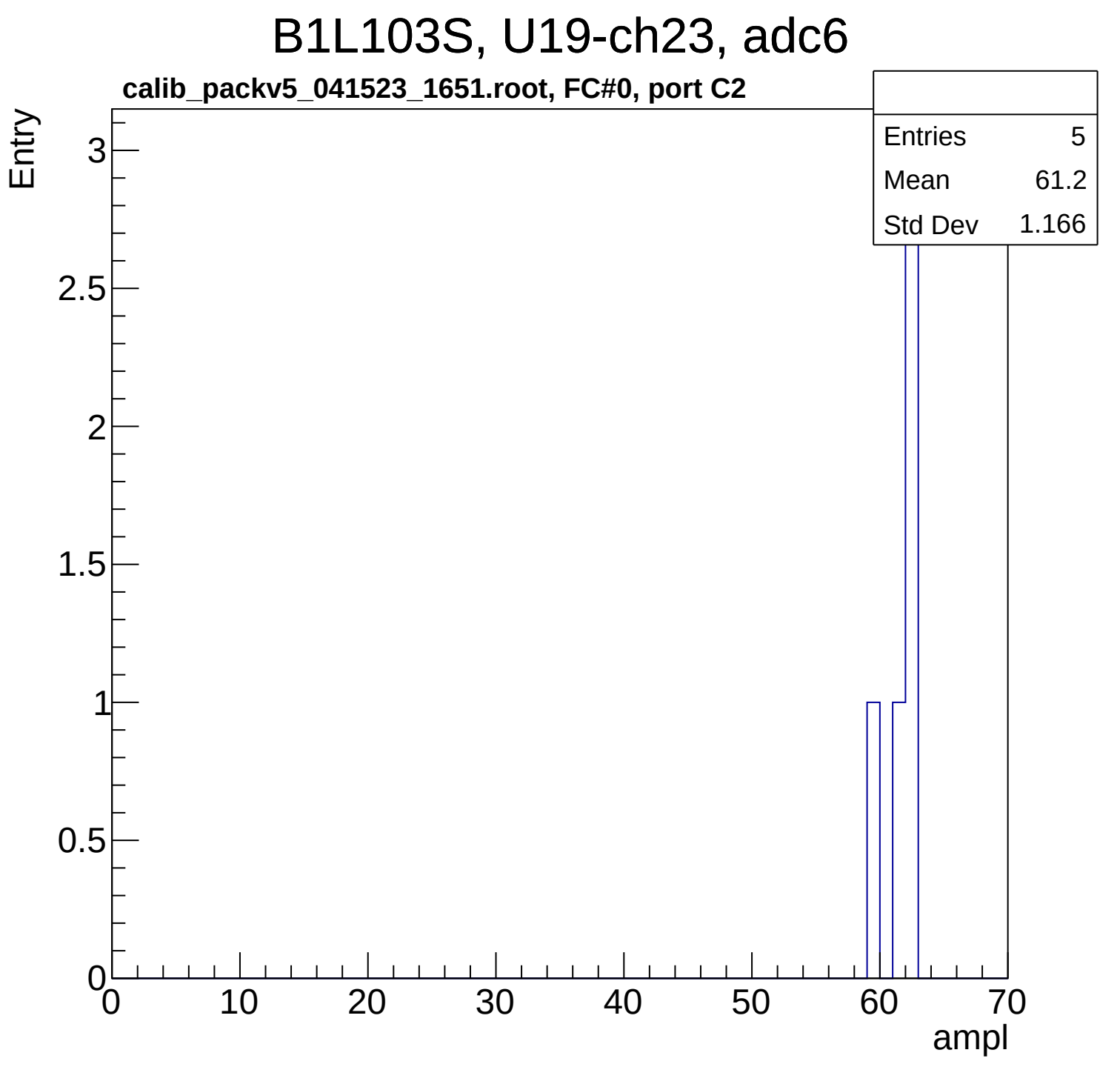
B1L103S, U19-ch23, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 61.2
Std Dev 1.166
Entry
ampl
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1
1.5
2
2.5
3
0
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20
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40
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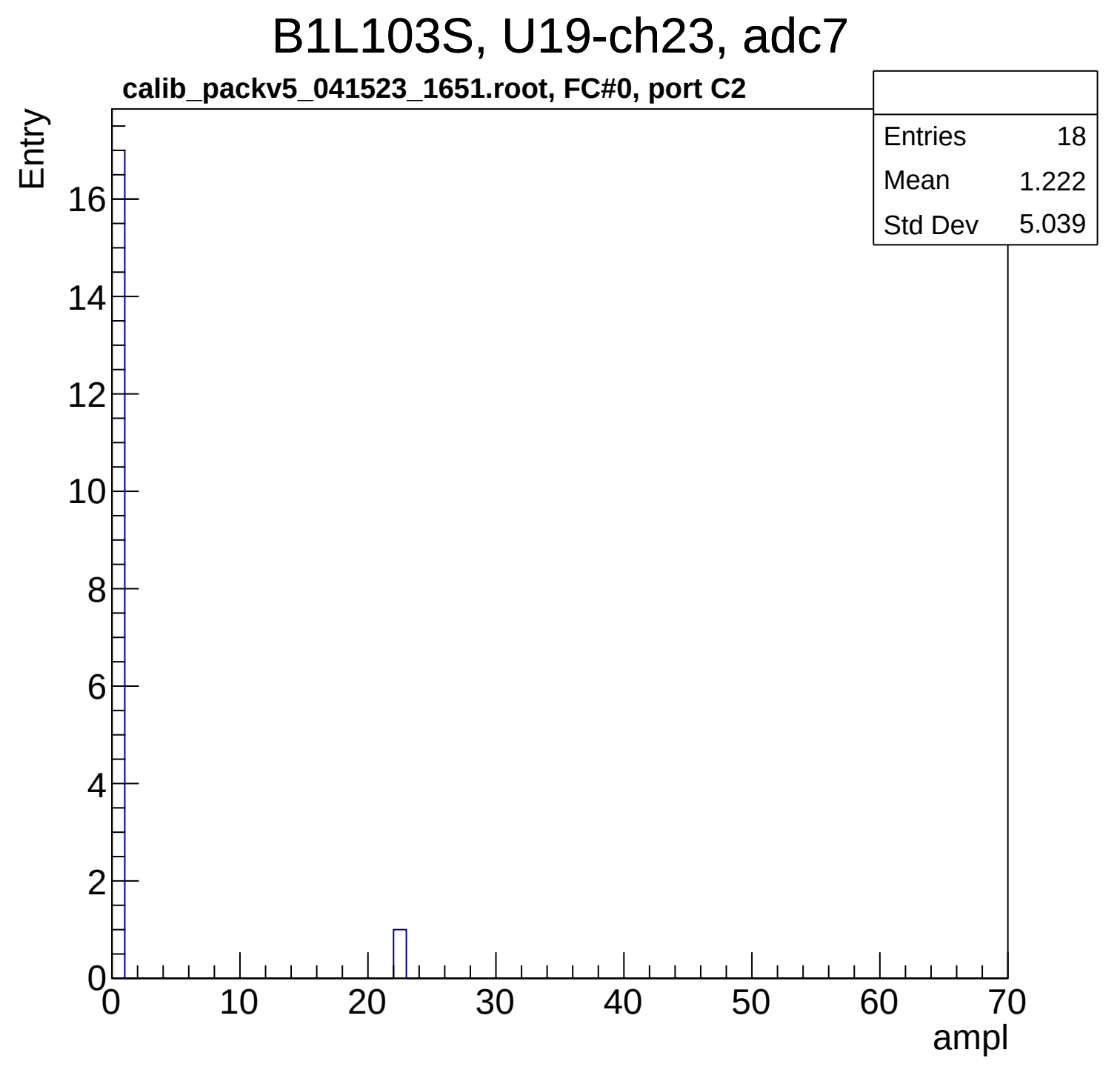
B1L103S, U19-ch23, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.222
Std Dev 5.039
Entry
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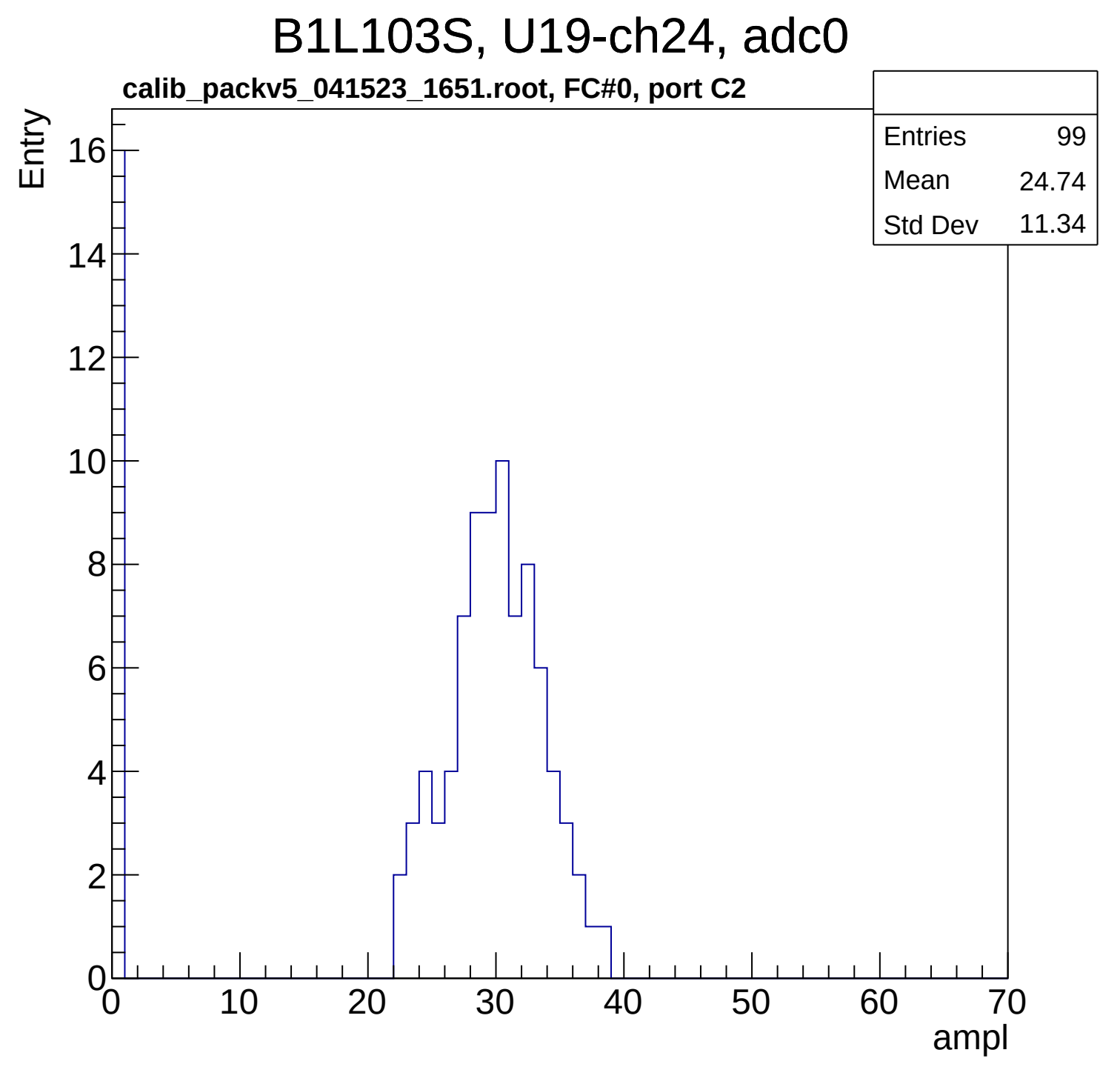
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch24, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 24.74
Std Dev 11.34
Entry
ampl
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4
6
8
10
12
14
16
0
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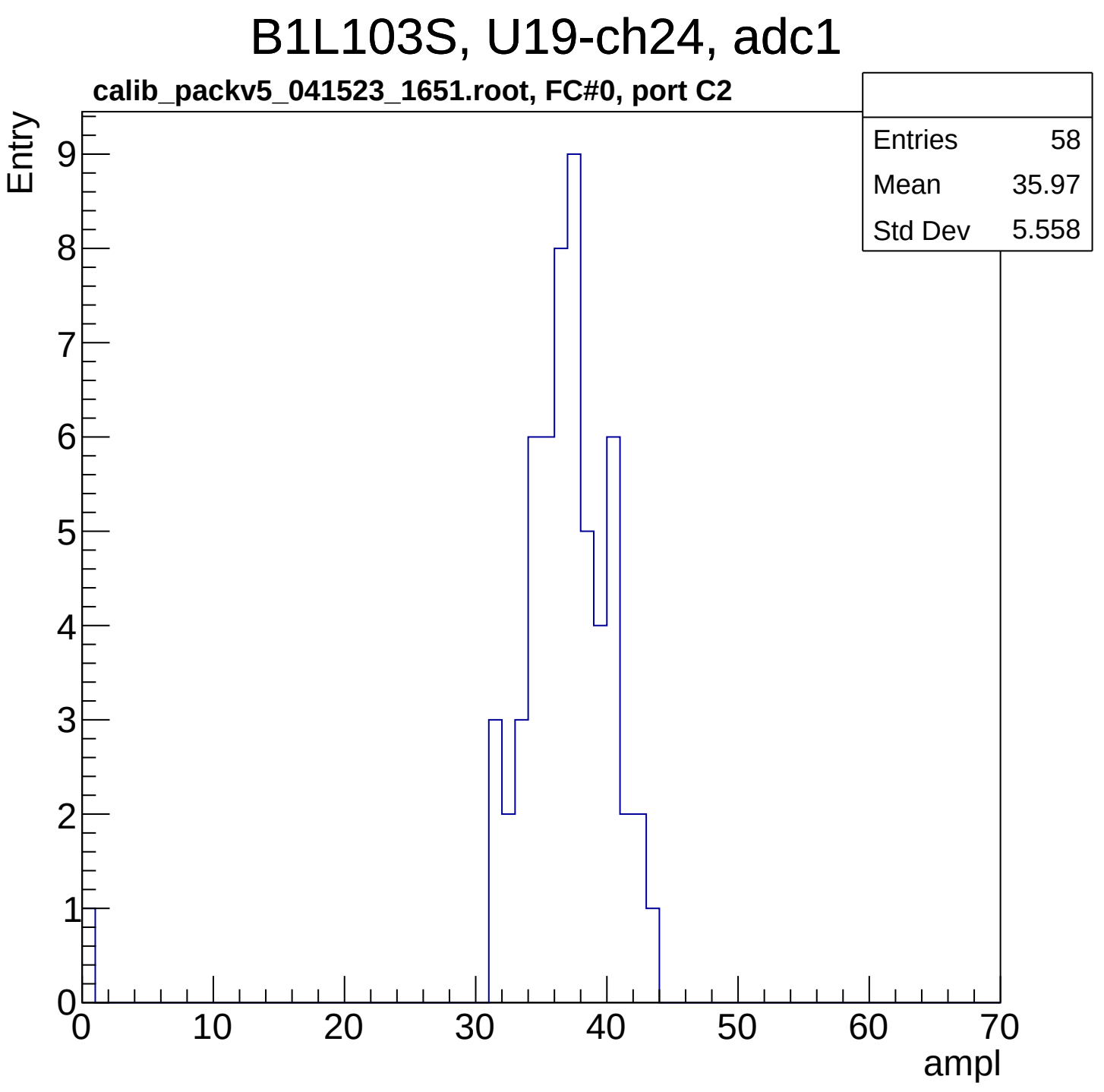
B1L103S, U19-ch24, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 35.97
Std Dev 5.558
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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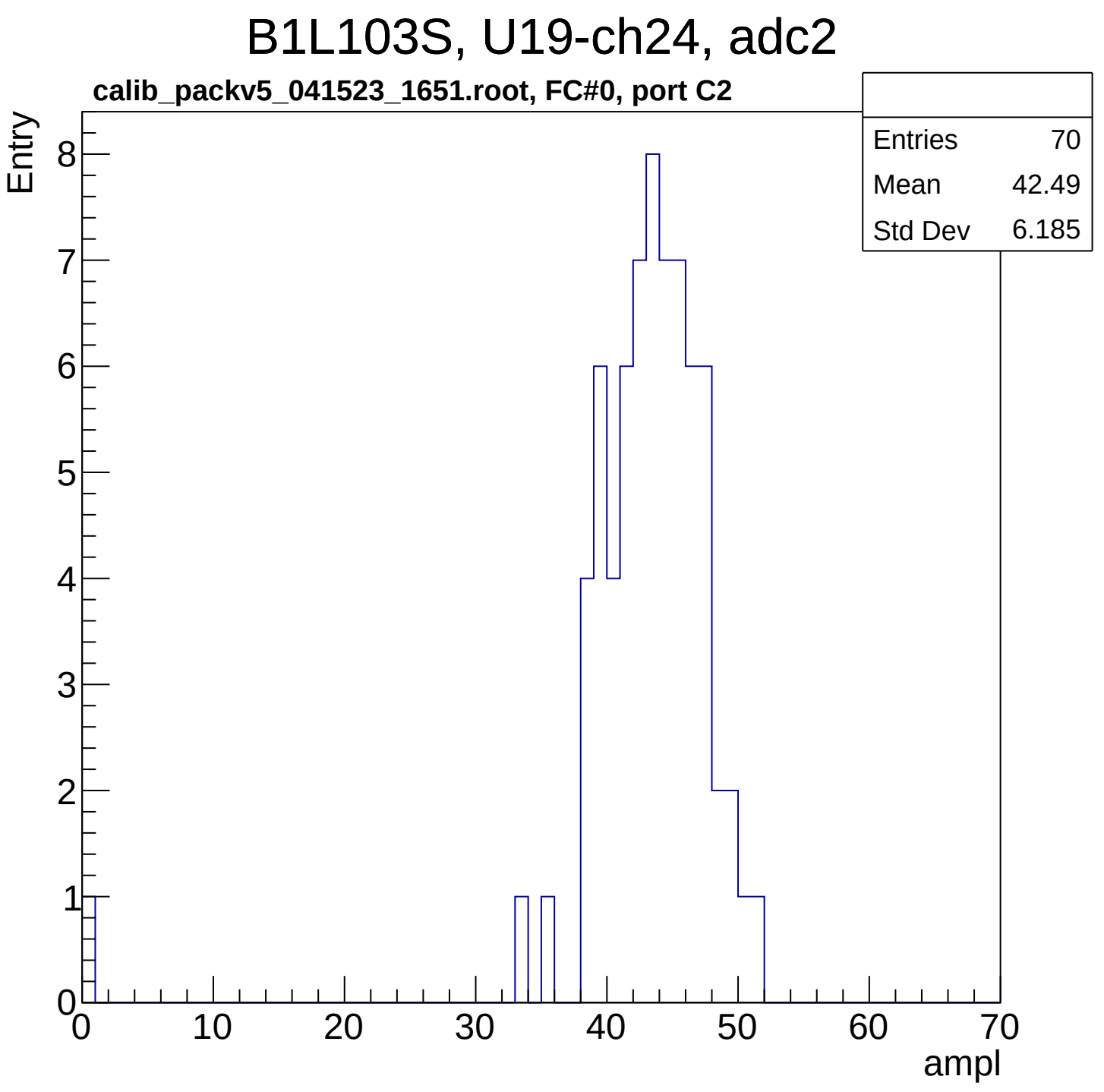
B1L103S, U19-ch24, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 42.49
Std Dev 6.185
Entry
ampl
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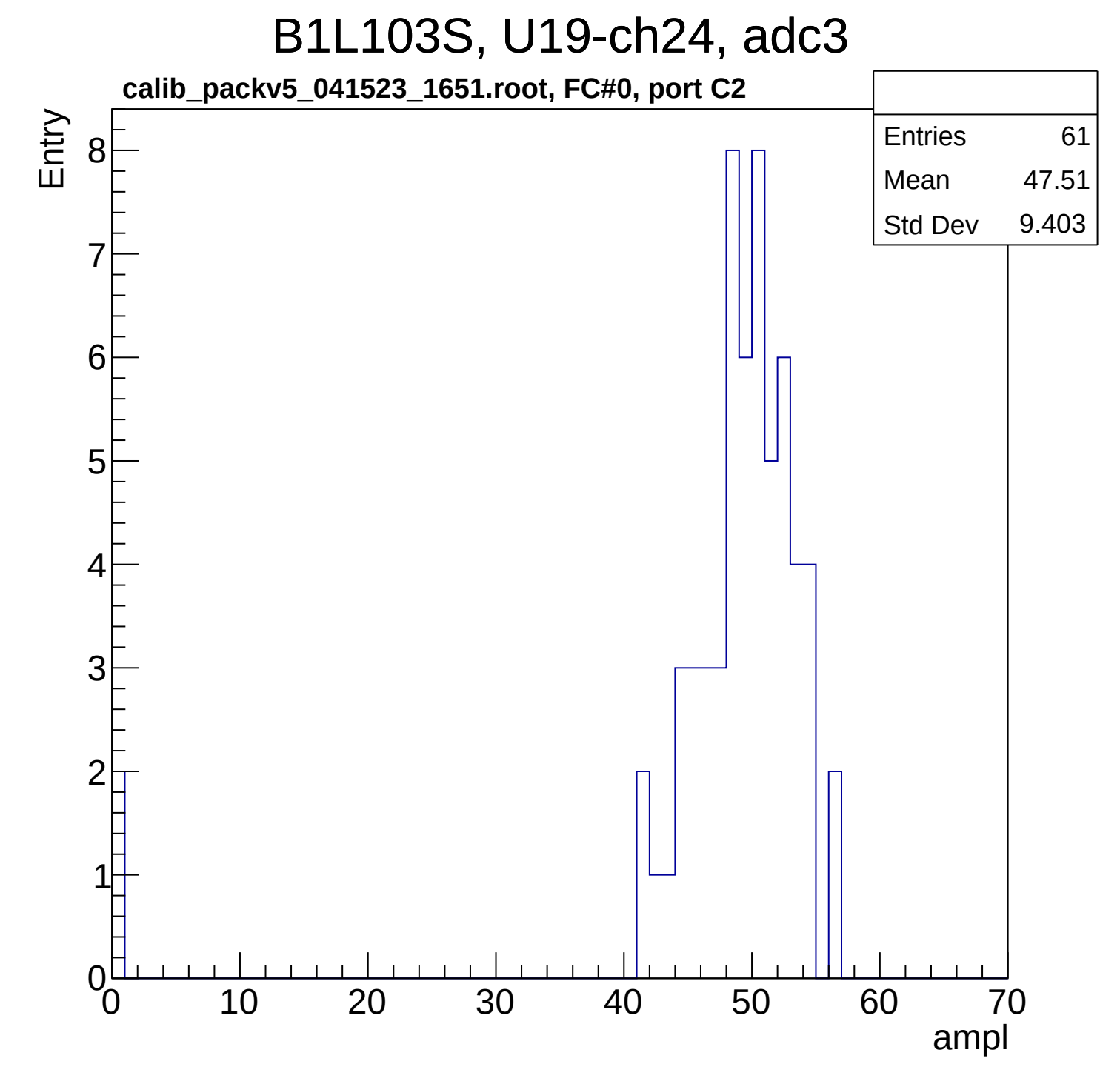
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch24, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 47.51
Std Dev 9.403
Entry
ampl
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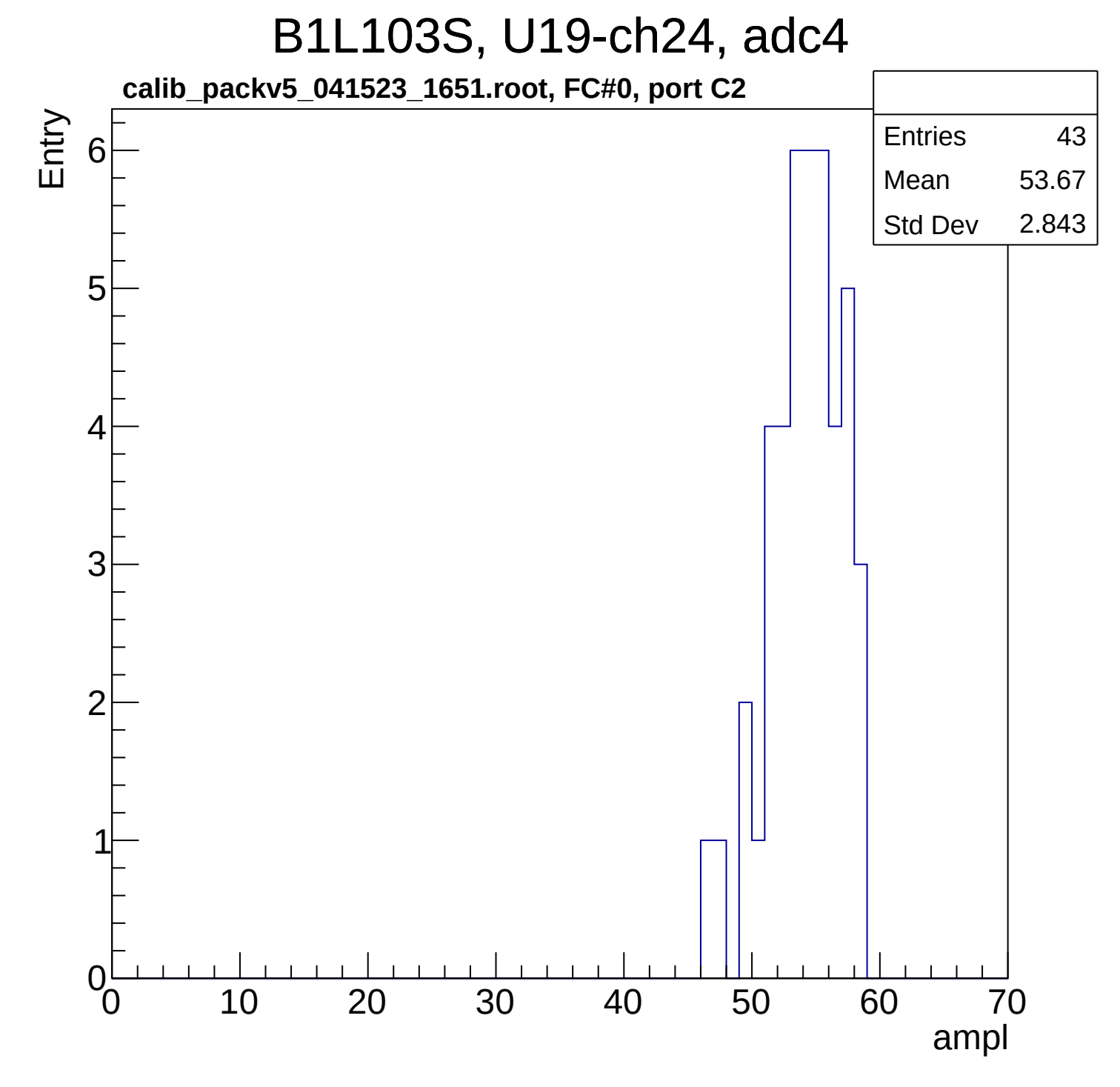
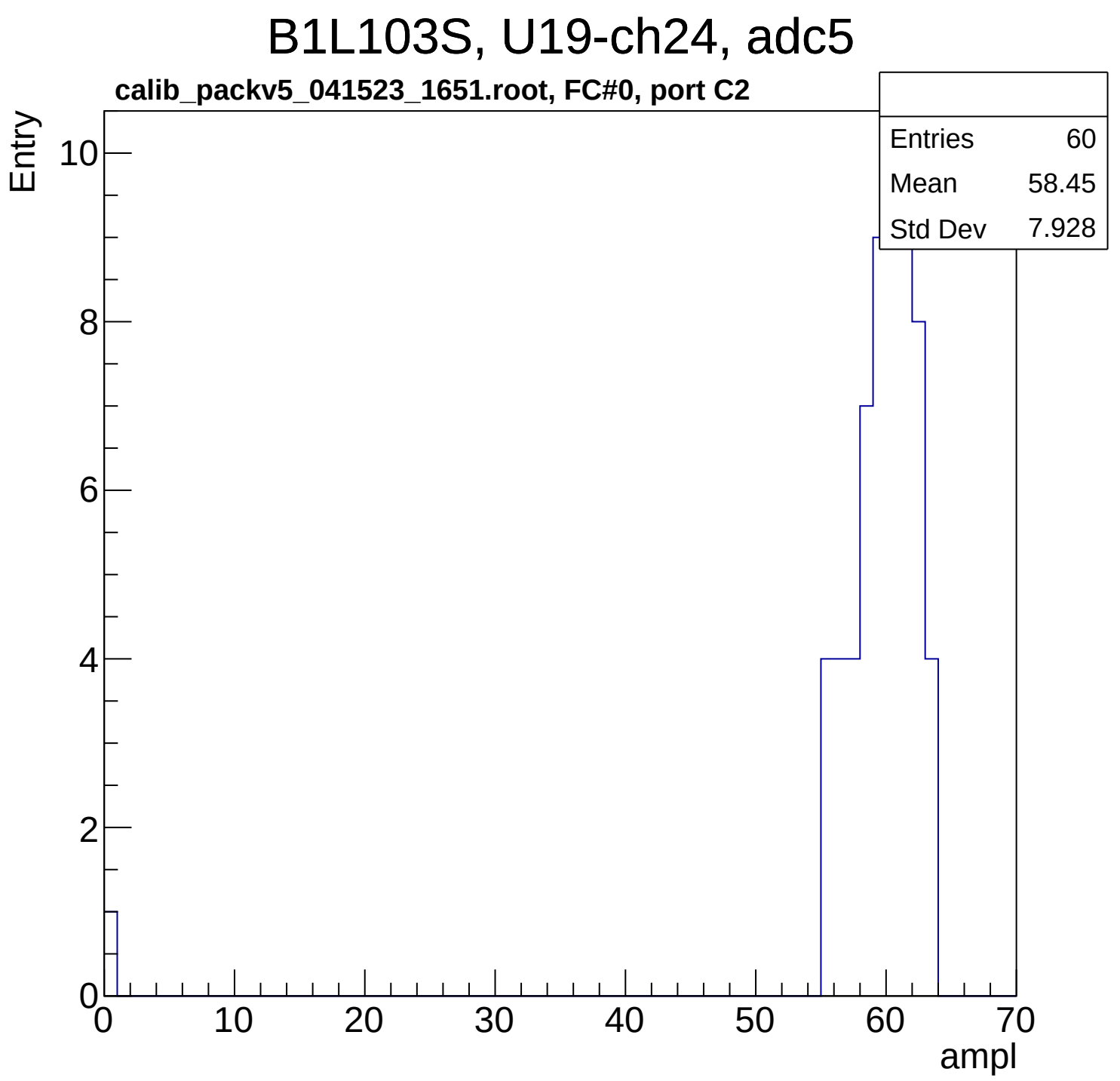
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch24, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 53.67
Std Dev 2.843
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U19-ch24, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 58.45
Std Dev 7.928
Entry
ampl
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2
4
6
8
10
0
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40
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60
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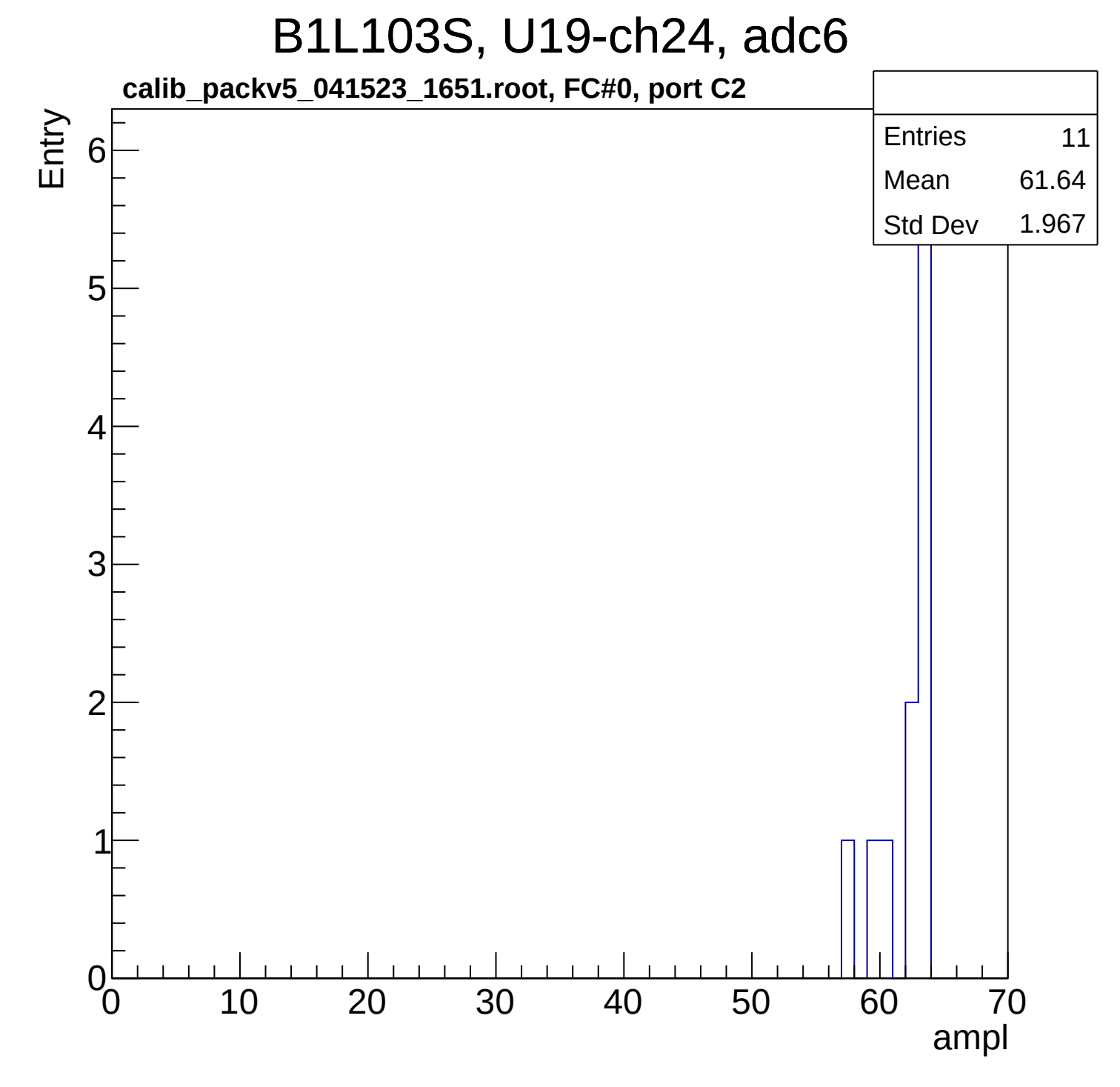
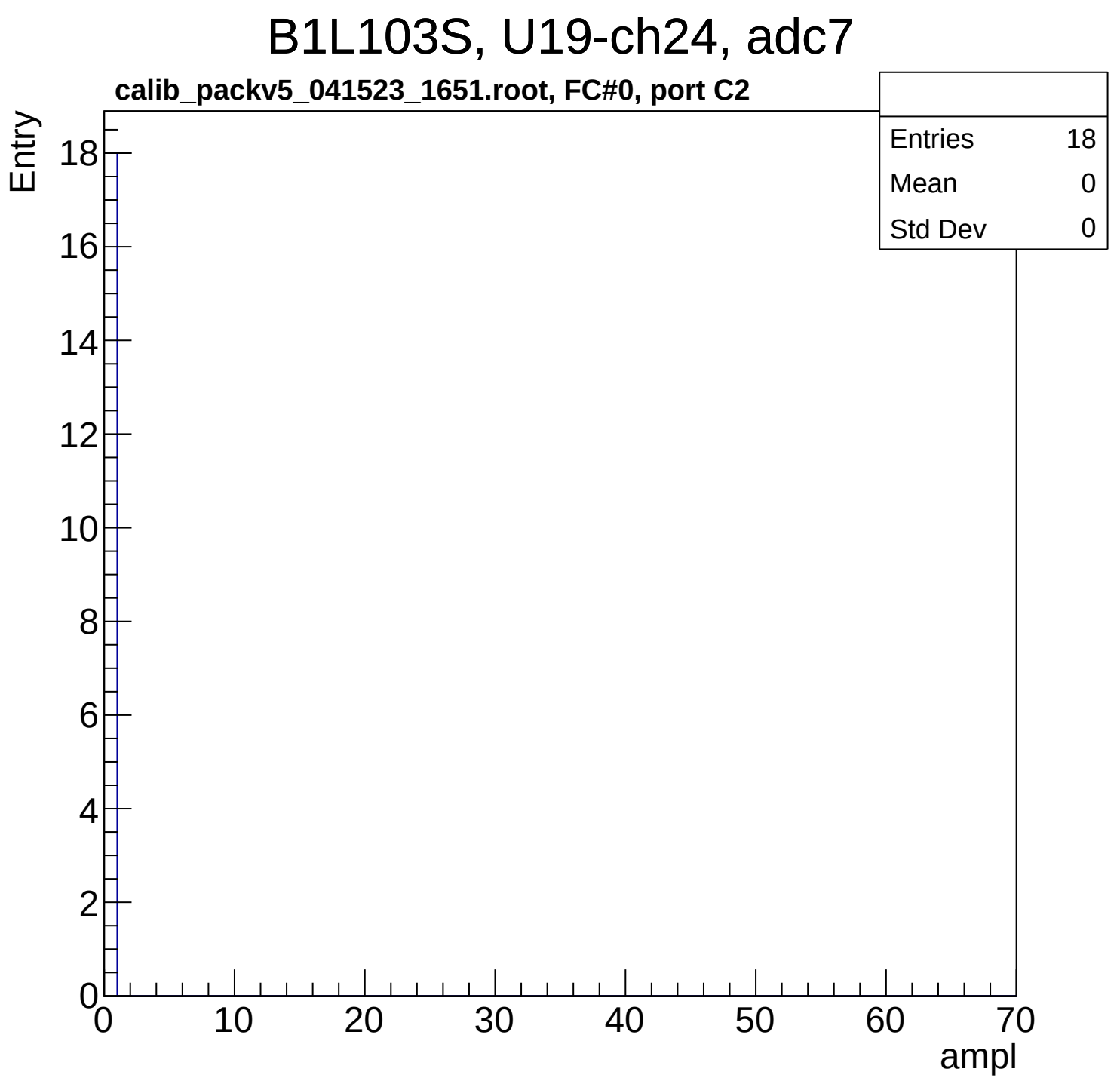
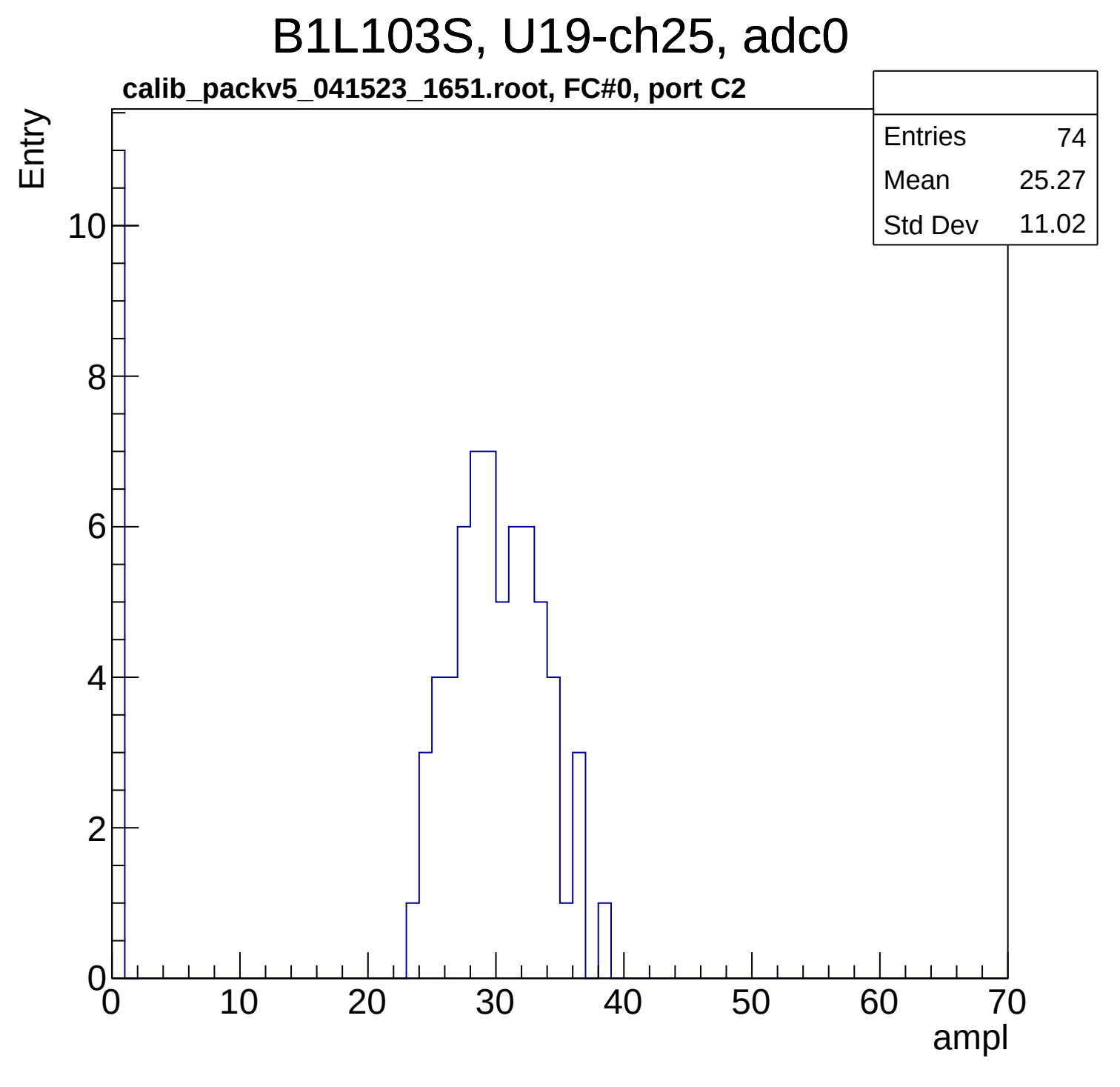

B1L103S, U19-ch24, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 61.64
Std Dev 1.967
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U19-ch24, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch25, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 25.27
Std Dev 11.02
Entry
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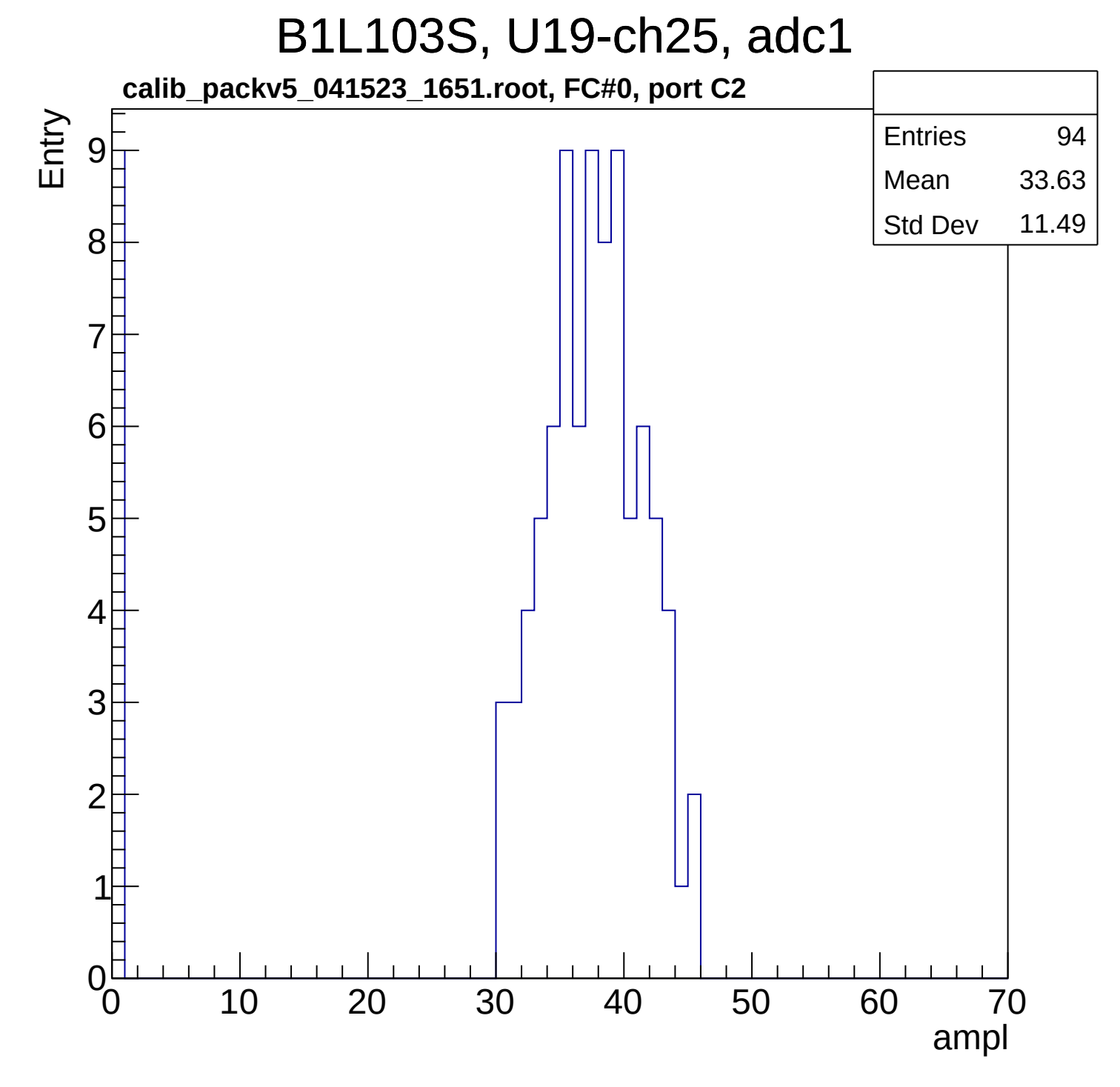
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch25, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 33.63
Std Dev 11.49
Entry
ampl
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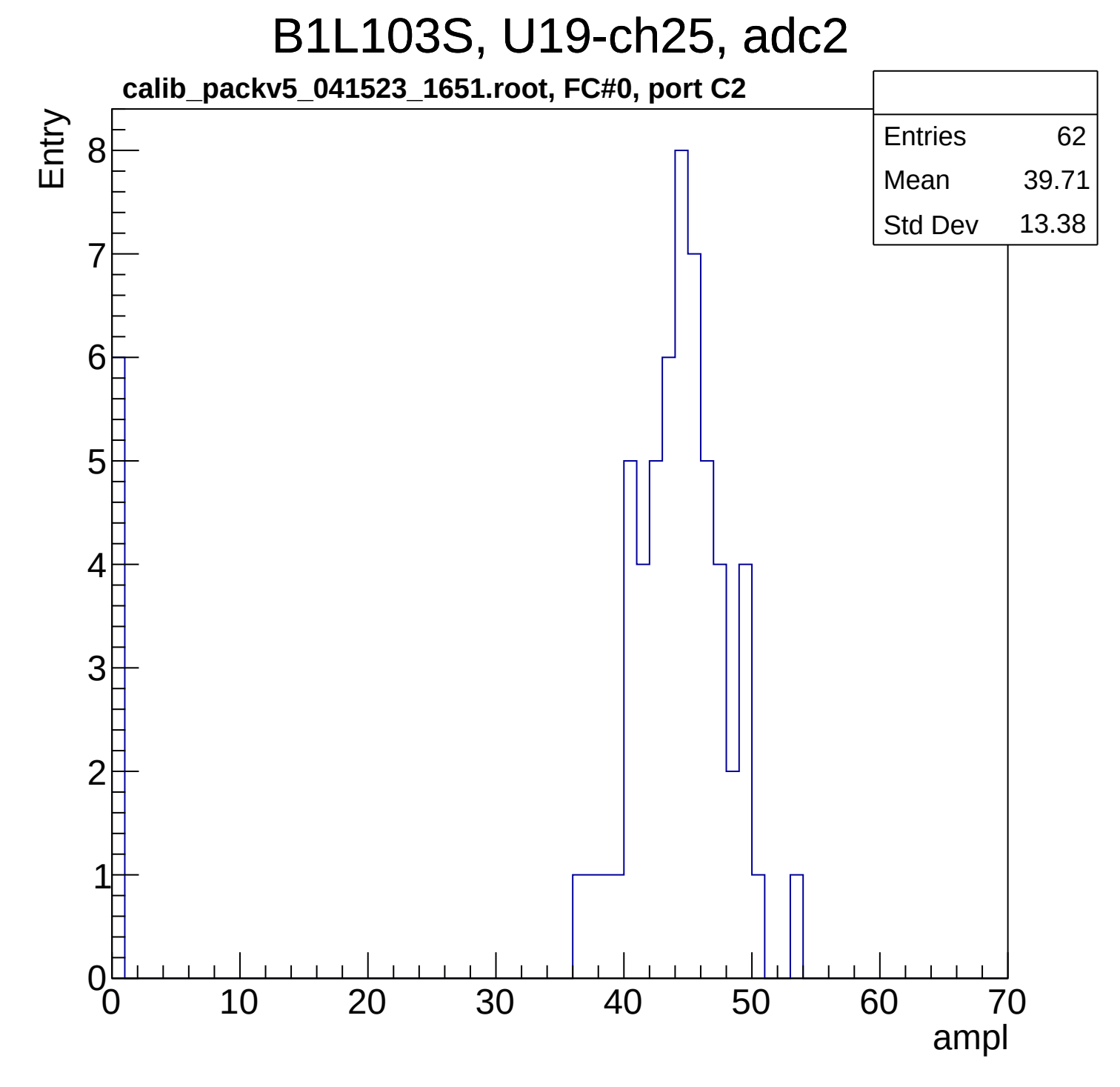
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch25, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 39.71
Std Dev 13.38
Entry
ampl
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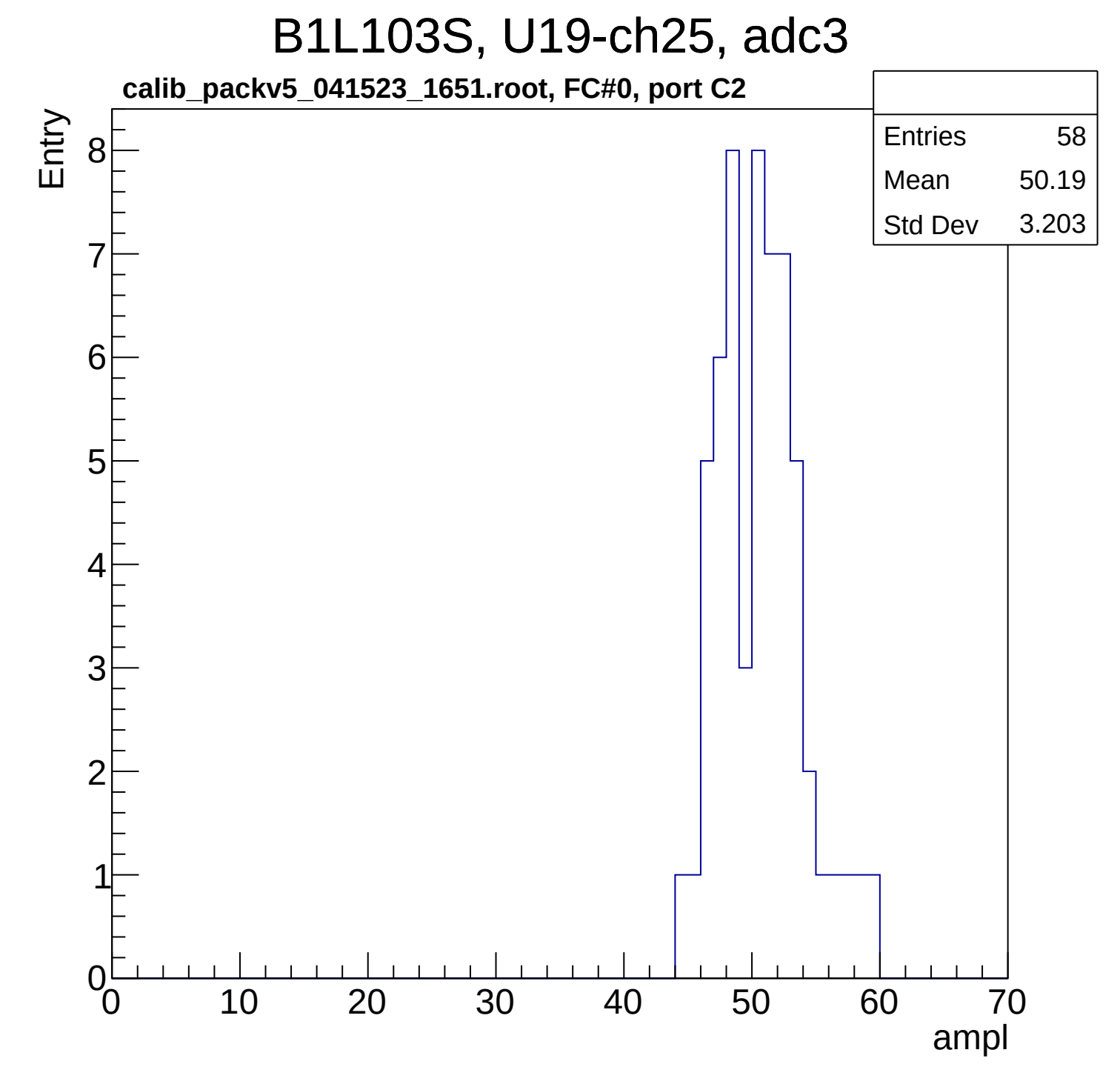
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch25, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 50.19
Std Dev 3.203
Entry
ampl
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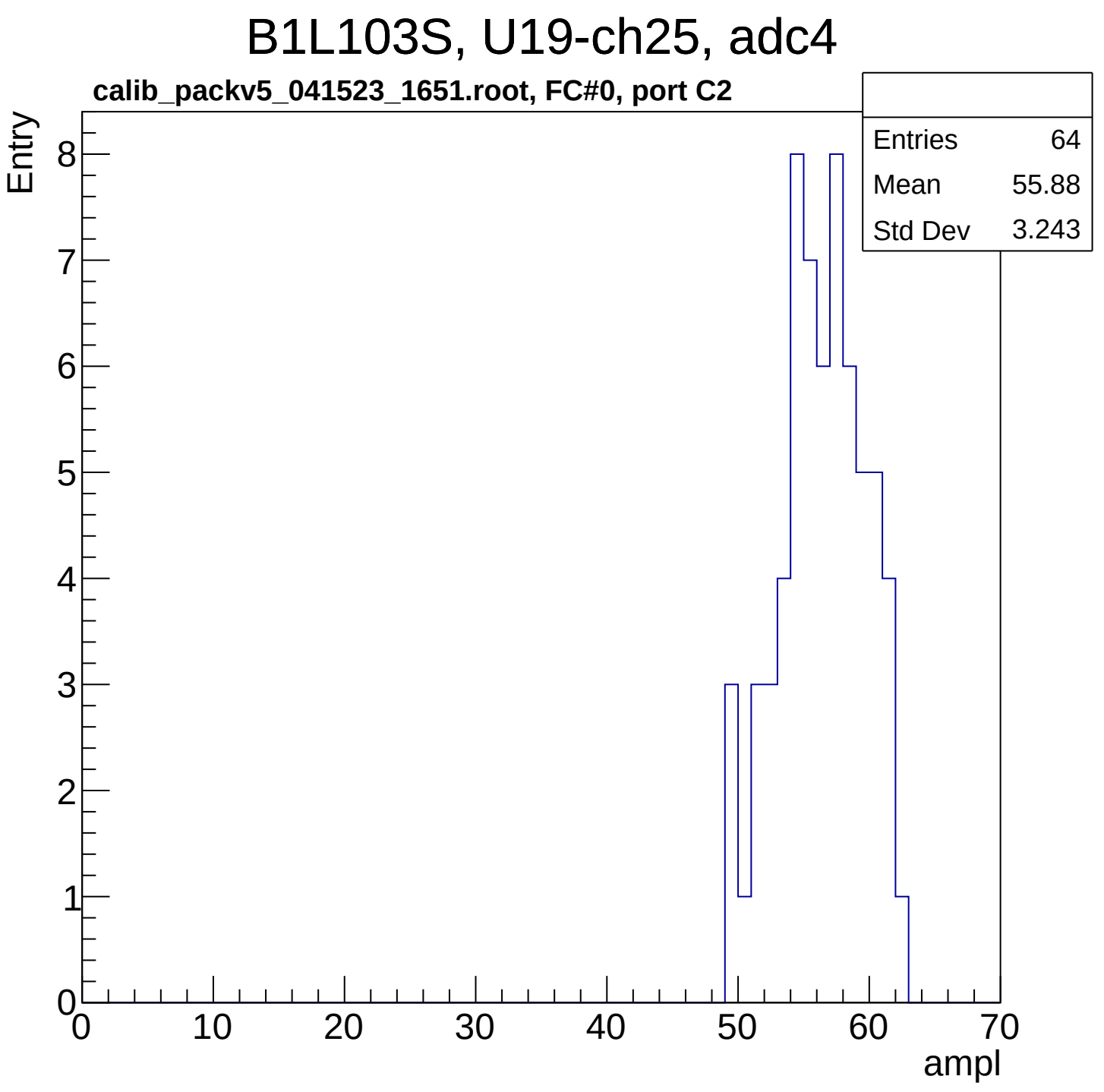
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch25, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 55.88
Std Dev 3.243
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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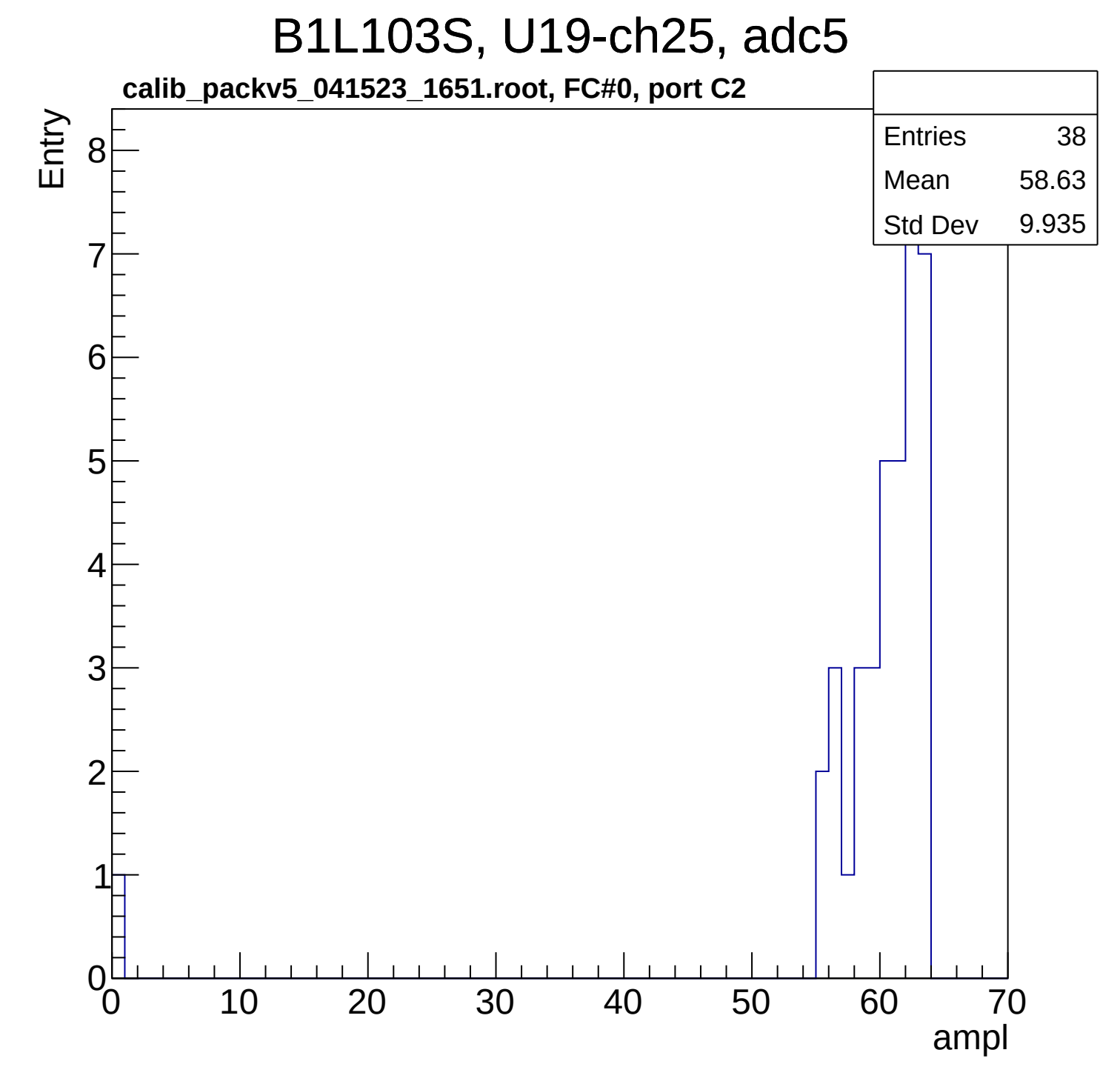
B1L103S, U19-ch25, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 58.63
Std Dev 9.935
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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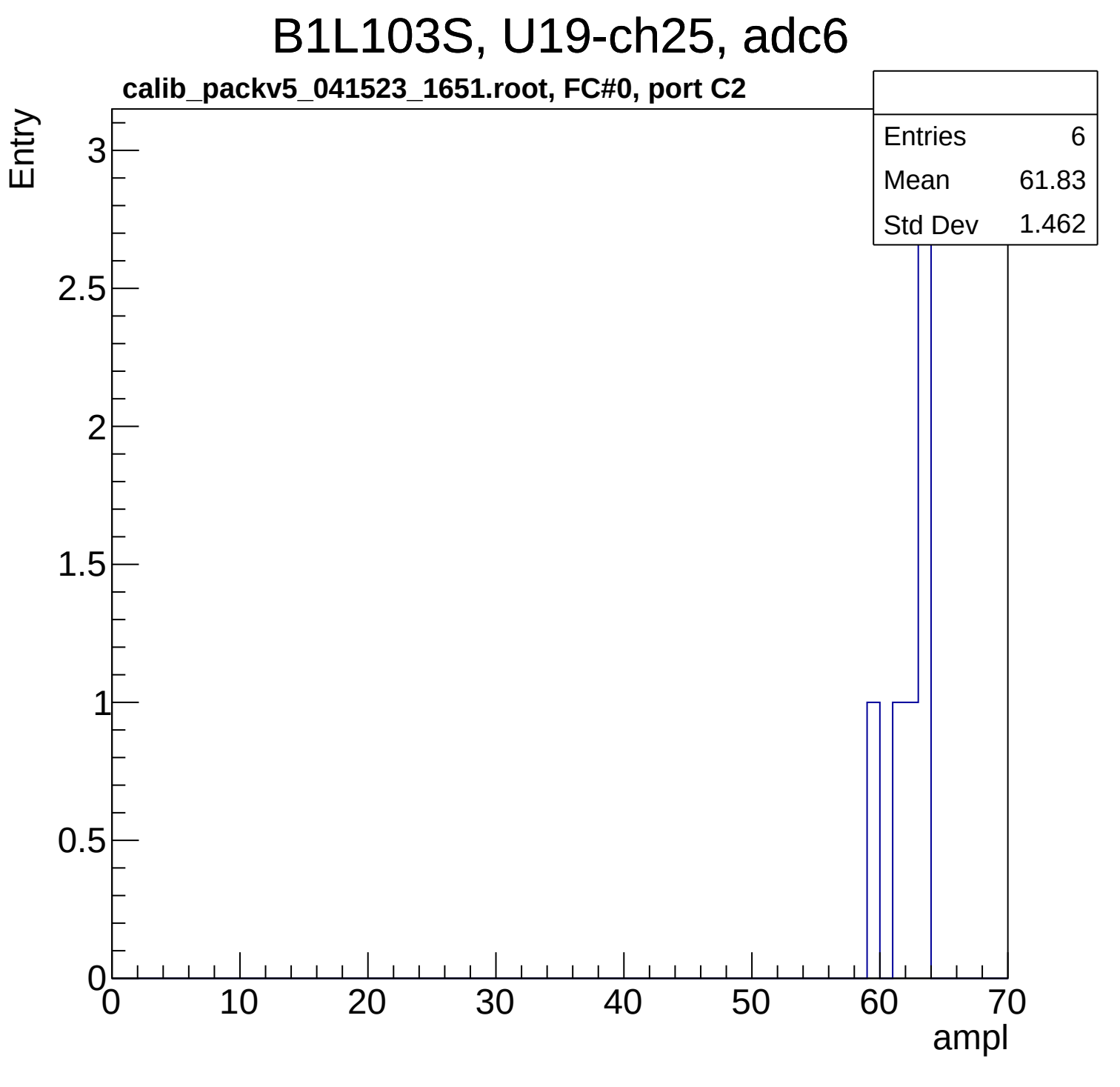
B1L103S, U19-ch25, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 61.83
Std Dev 1.462
Entry
ampl
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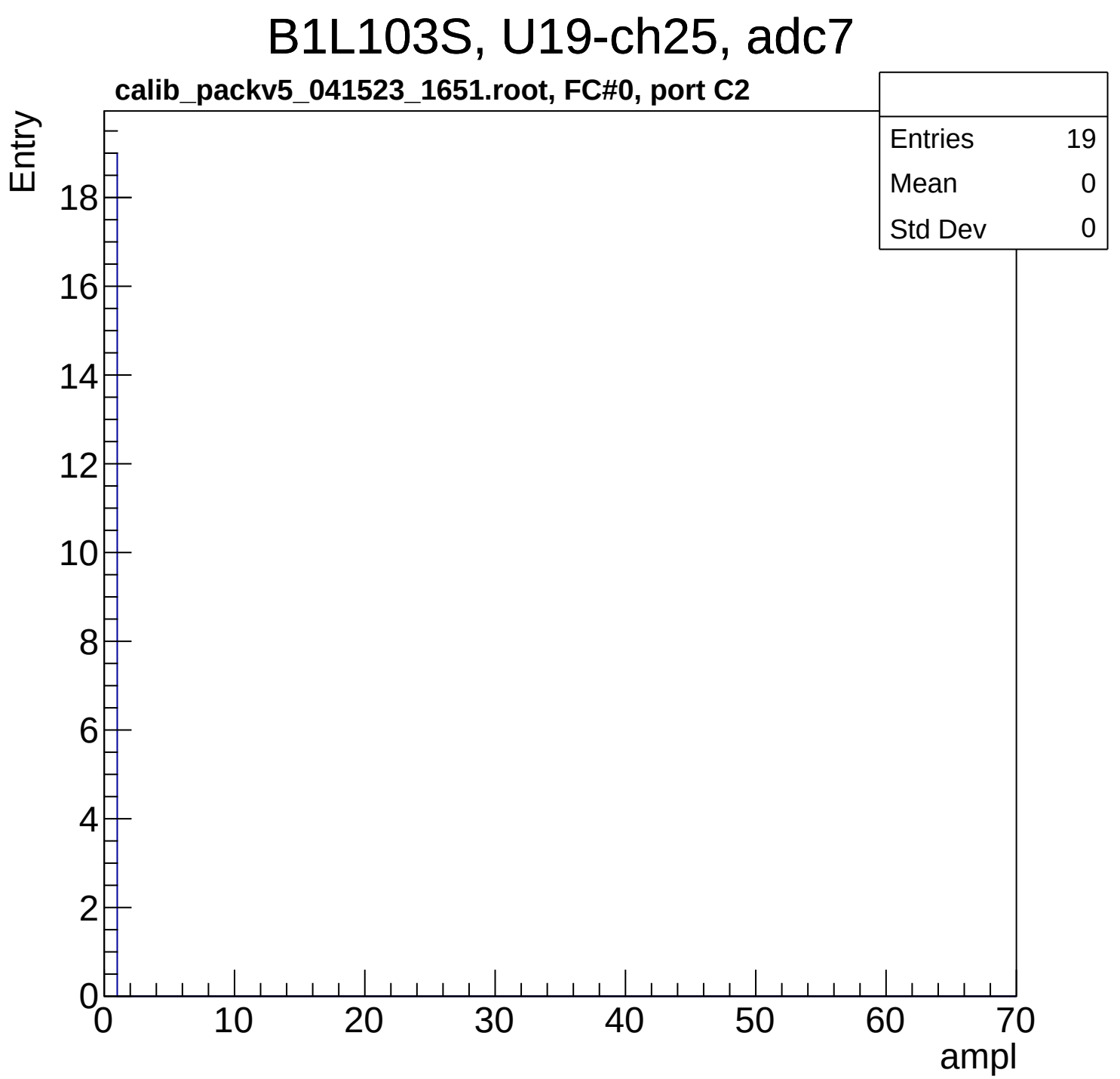
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U19-ch25, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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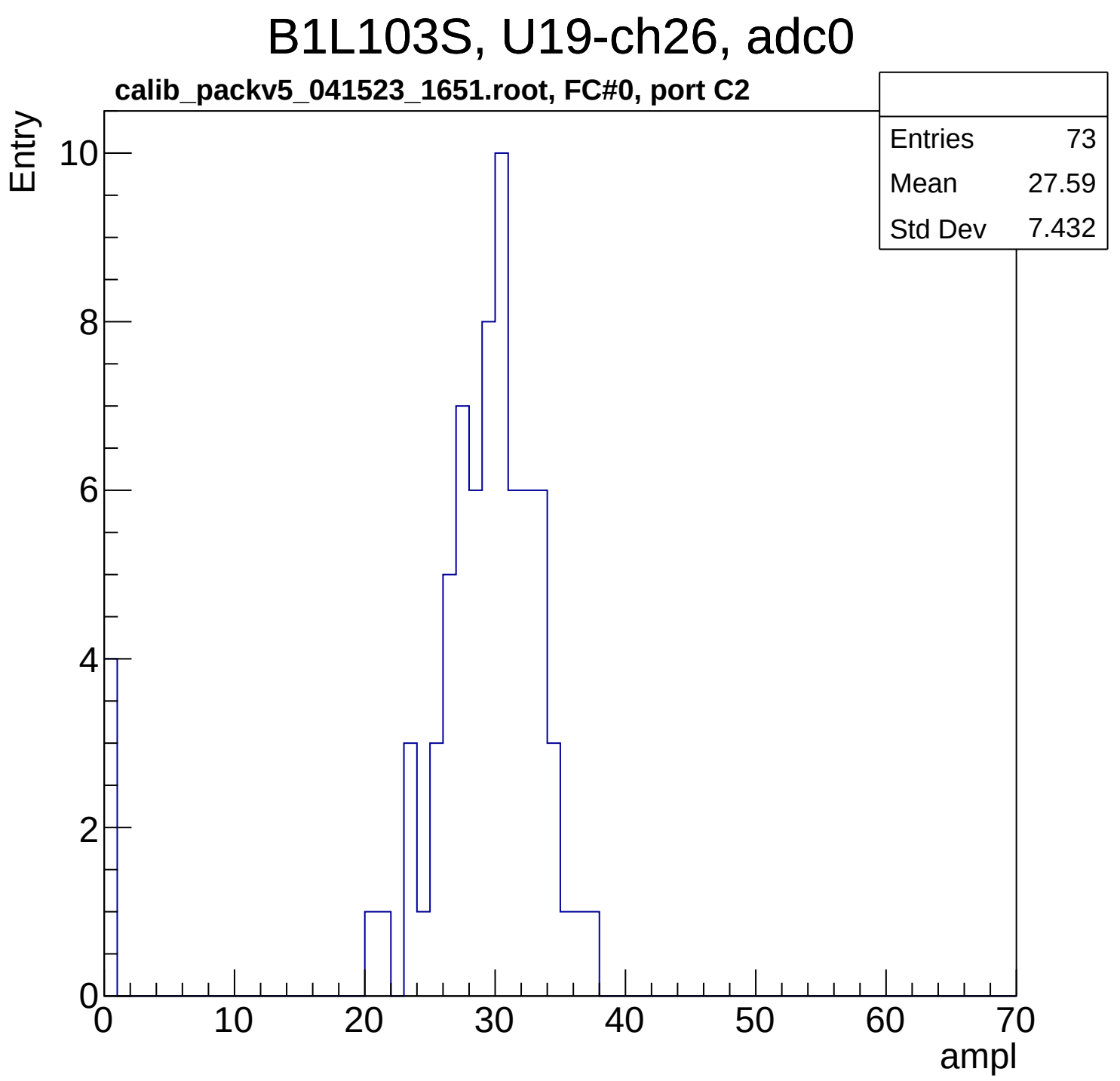
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch26, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 27.59
Std Dev 7.432
Entry
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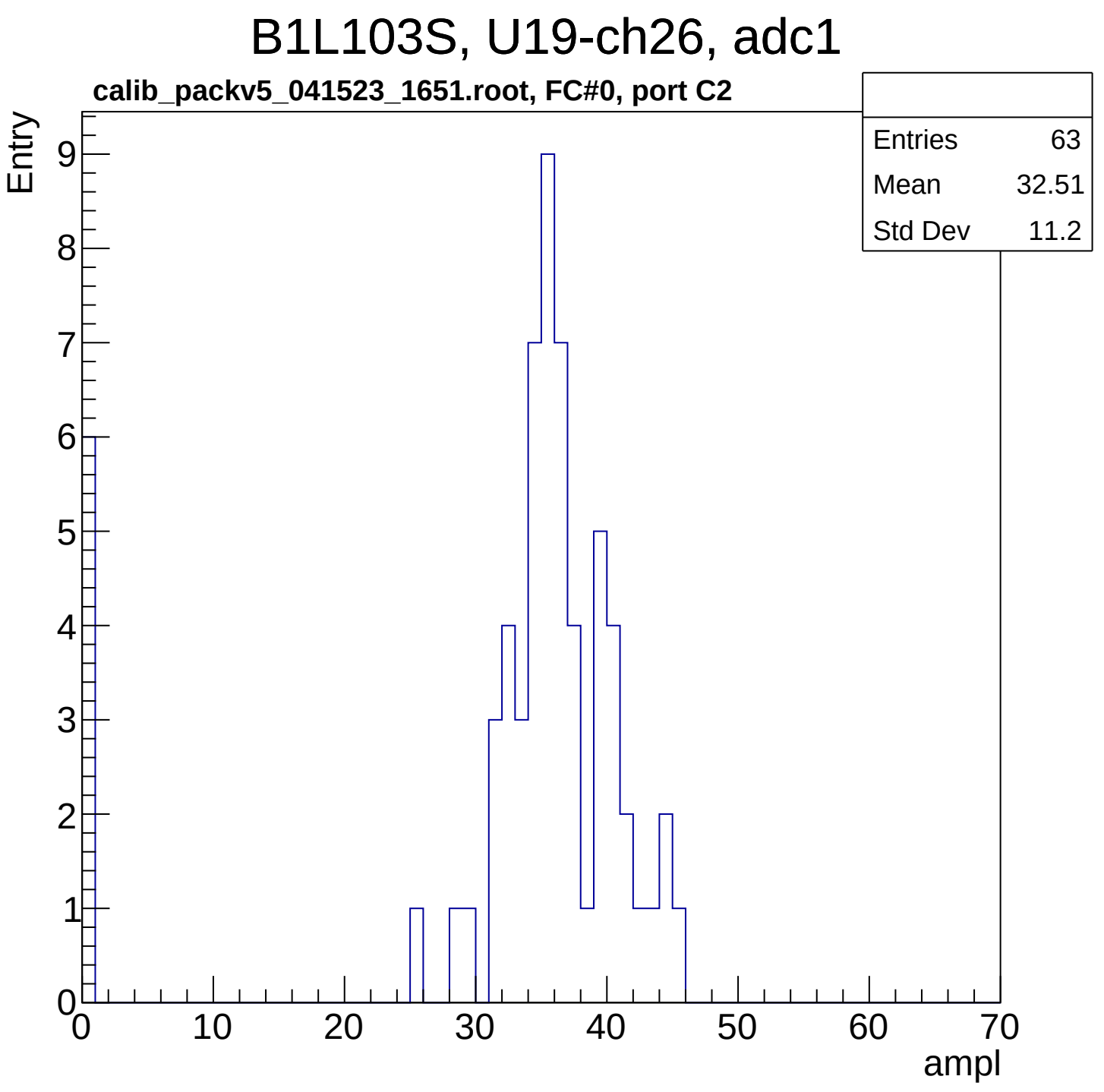
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch26, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 32.51
Std Dev 11.2
Entry
ampl
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2
3
4
5
6
7
8
9
0
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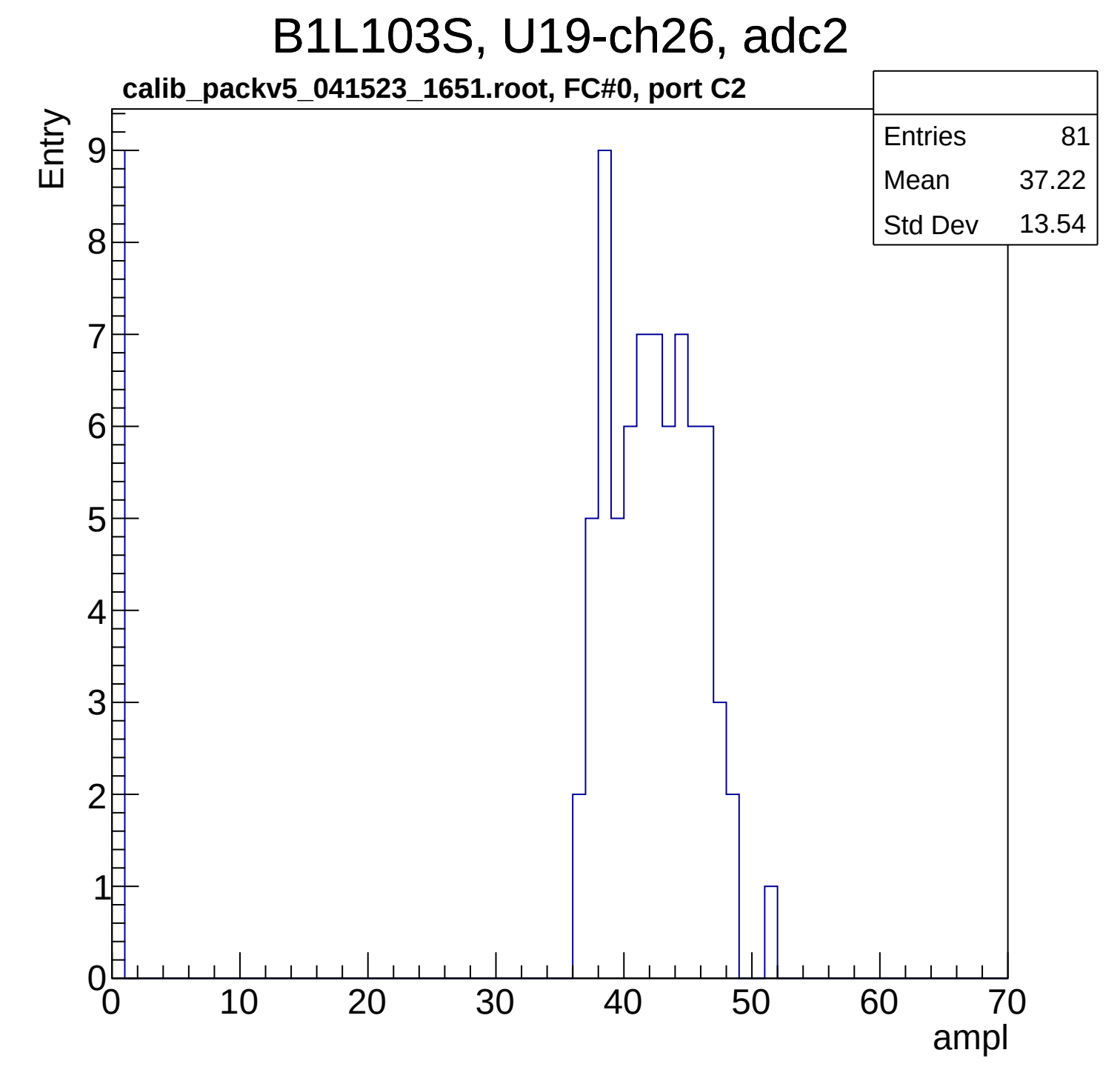
20
30
40
50
60
70


B1L103S, U19-ch26, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 37.22
Std Dev 13.54
Entry
ampl
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2
3
4
5
6
7
8
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0
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60
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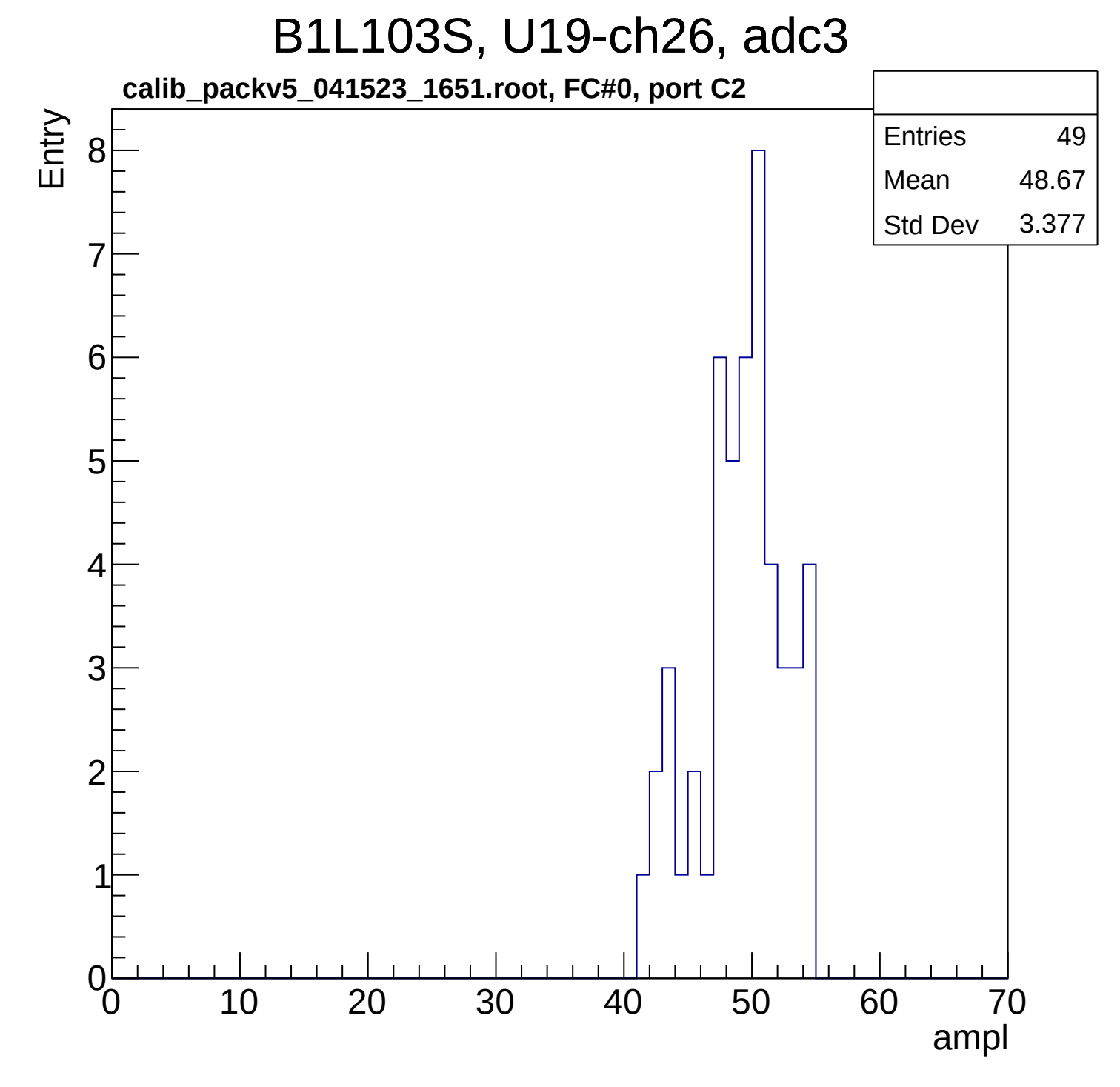
B1L103S, U19-ch26, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 48.67
Std Dev 3.377
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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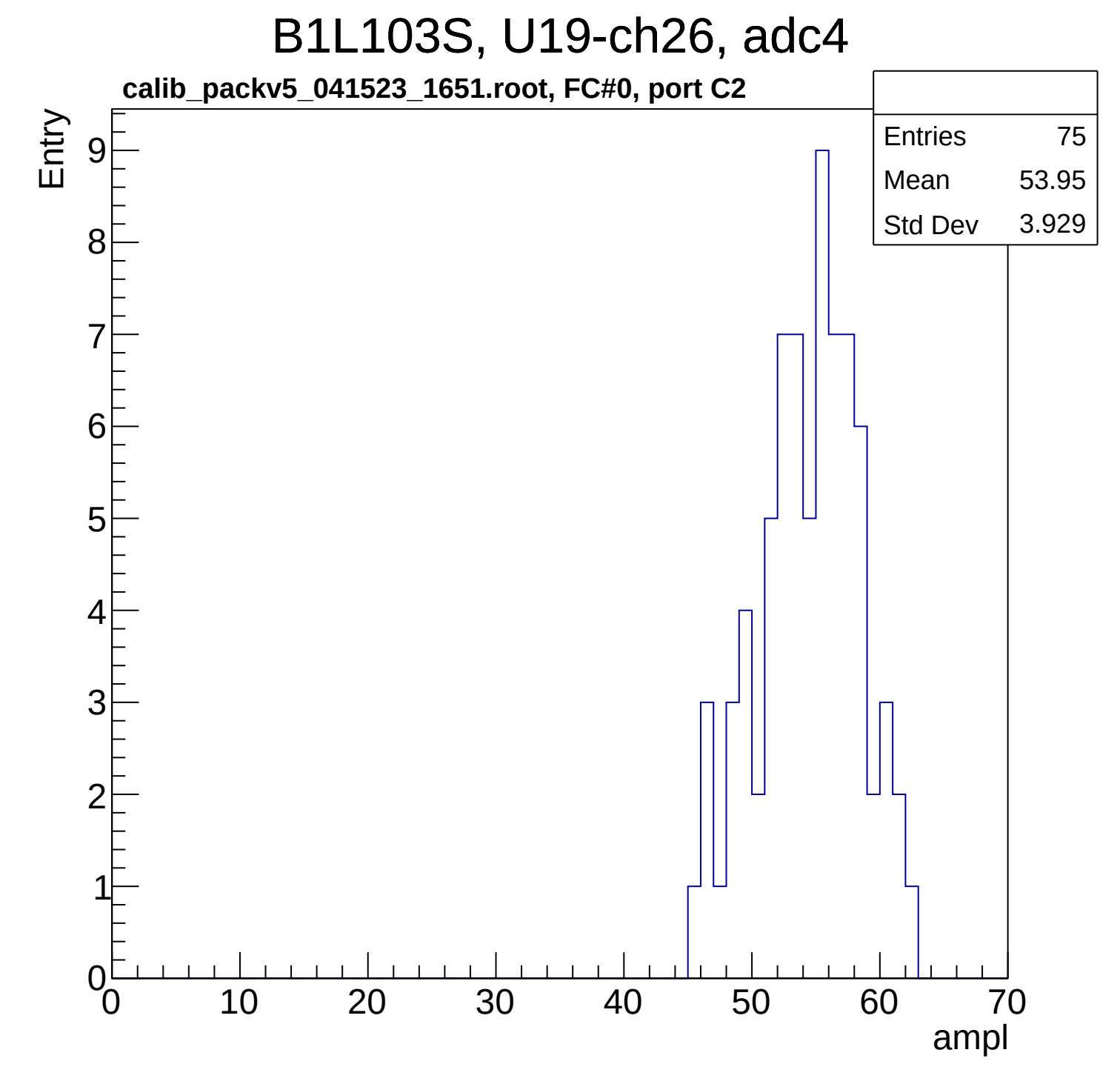
40
50
60
70


B1L103S, U19-ch26, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 53.95
Std Dev 3.929
Entry
ampl
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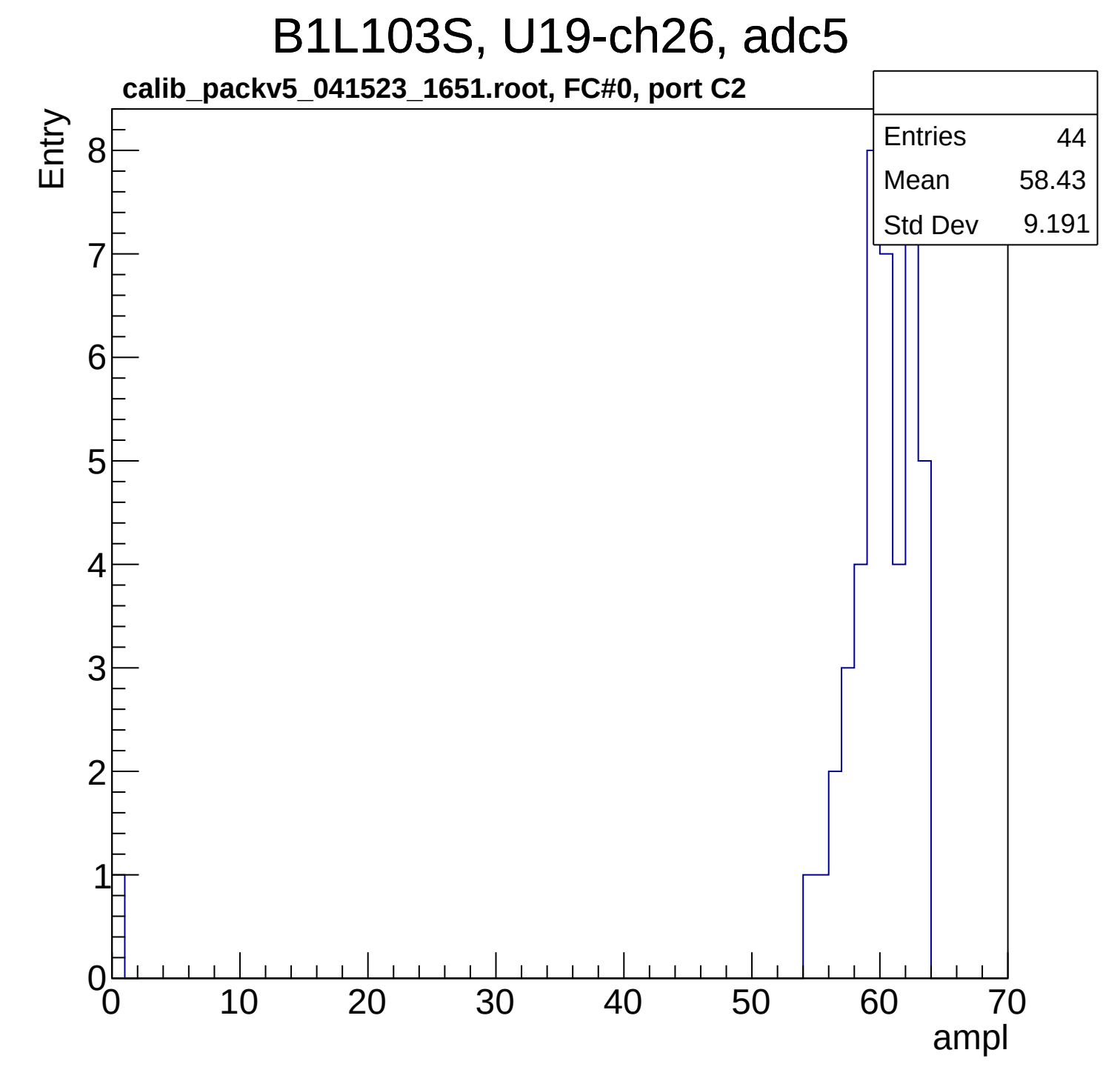
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch26, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 58.43
Std Dev 9.191
Entry
ampl
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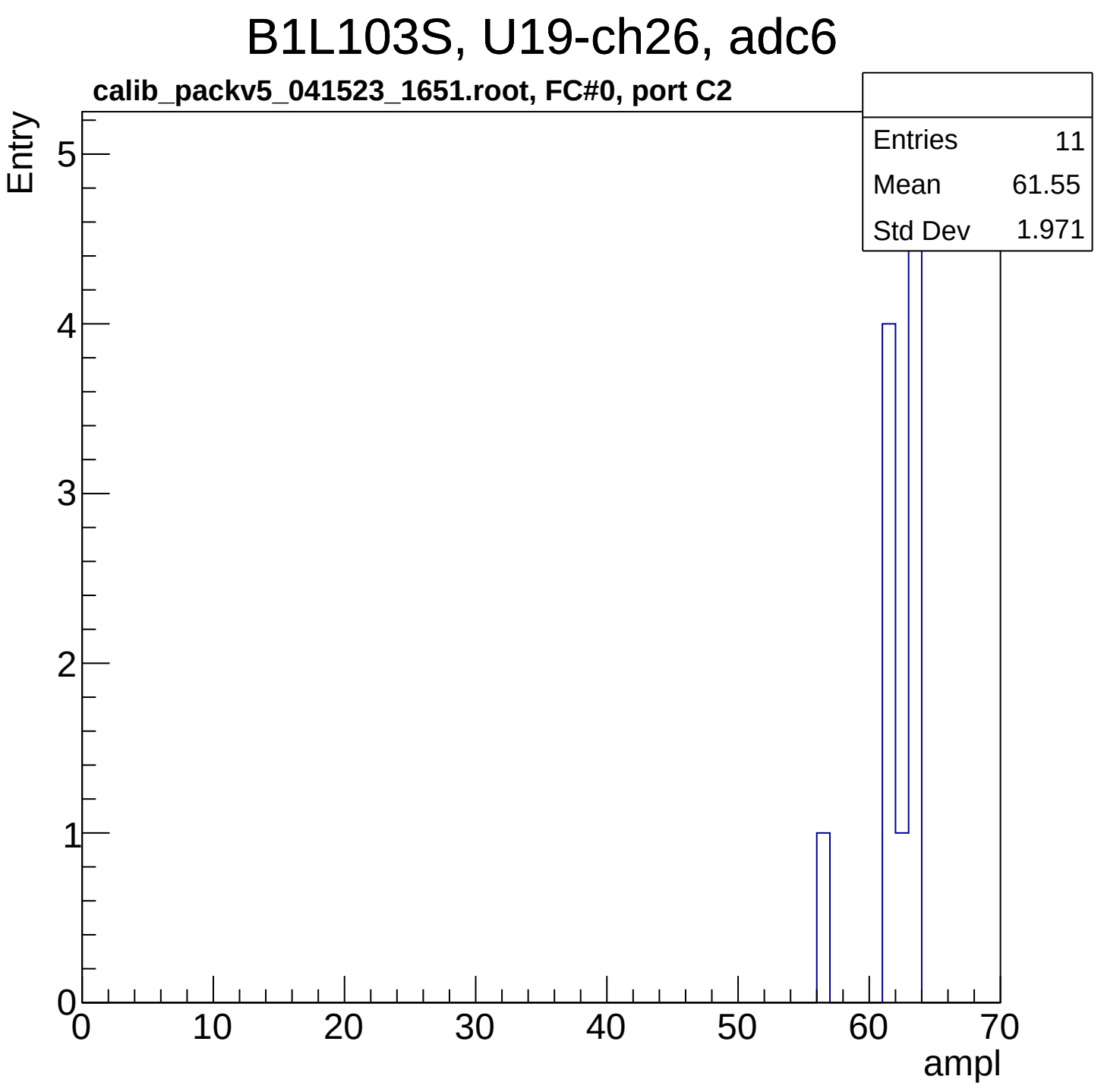
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch26, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 61.55
Std Dev 1.971
Entry
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1
2
3
4
5
0
10
20
30
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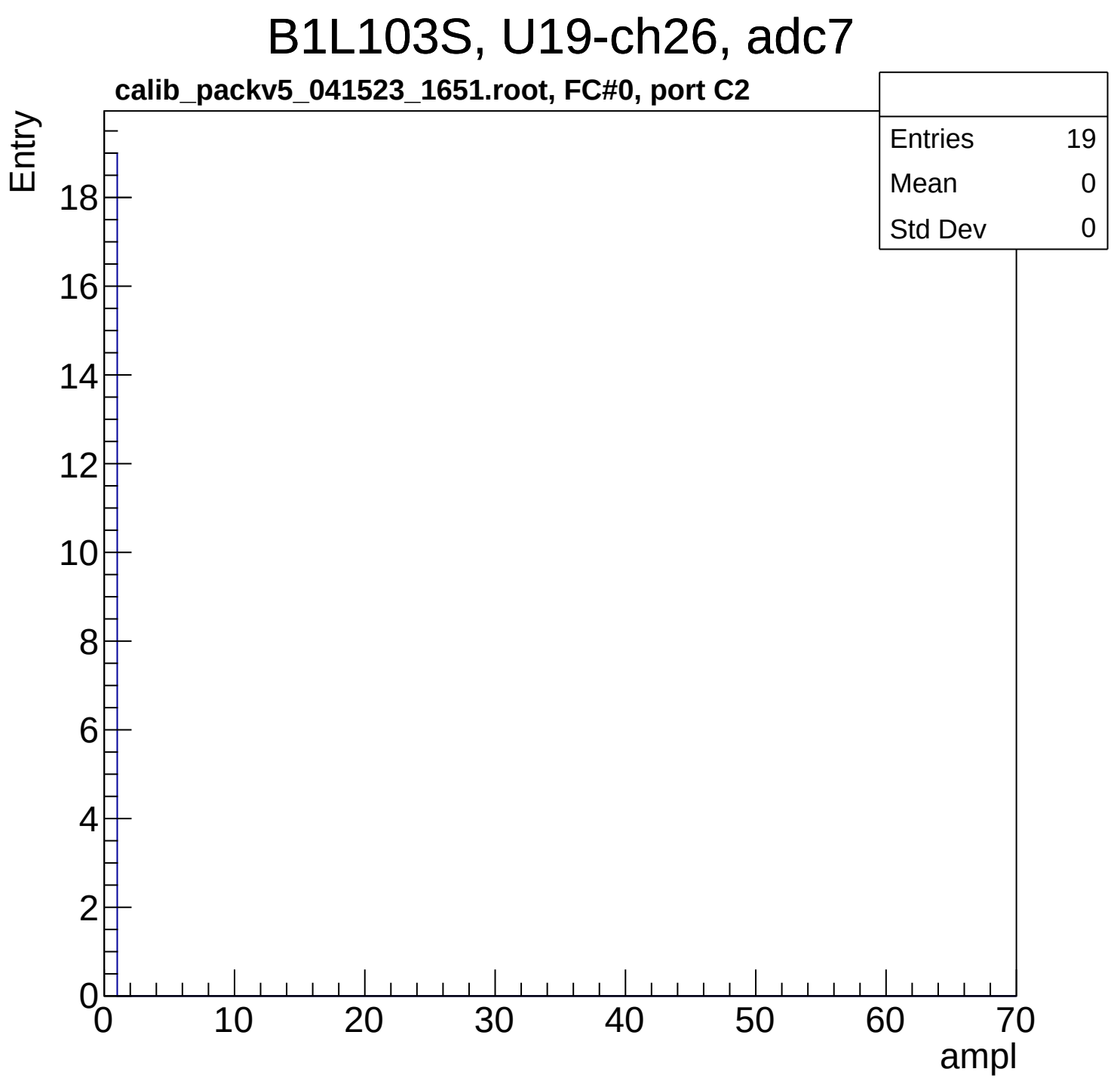
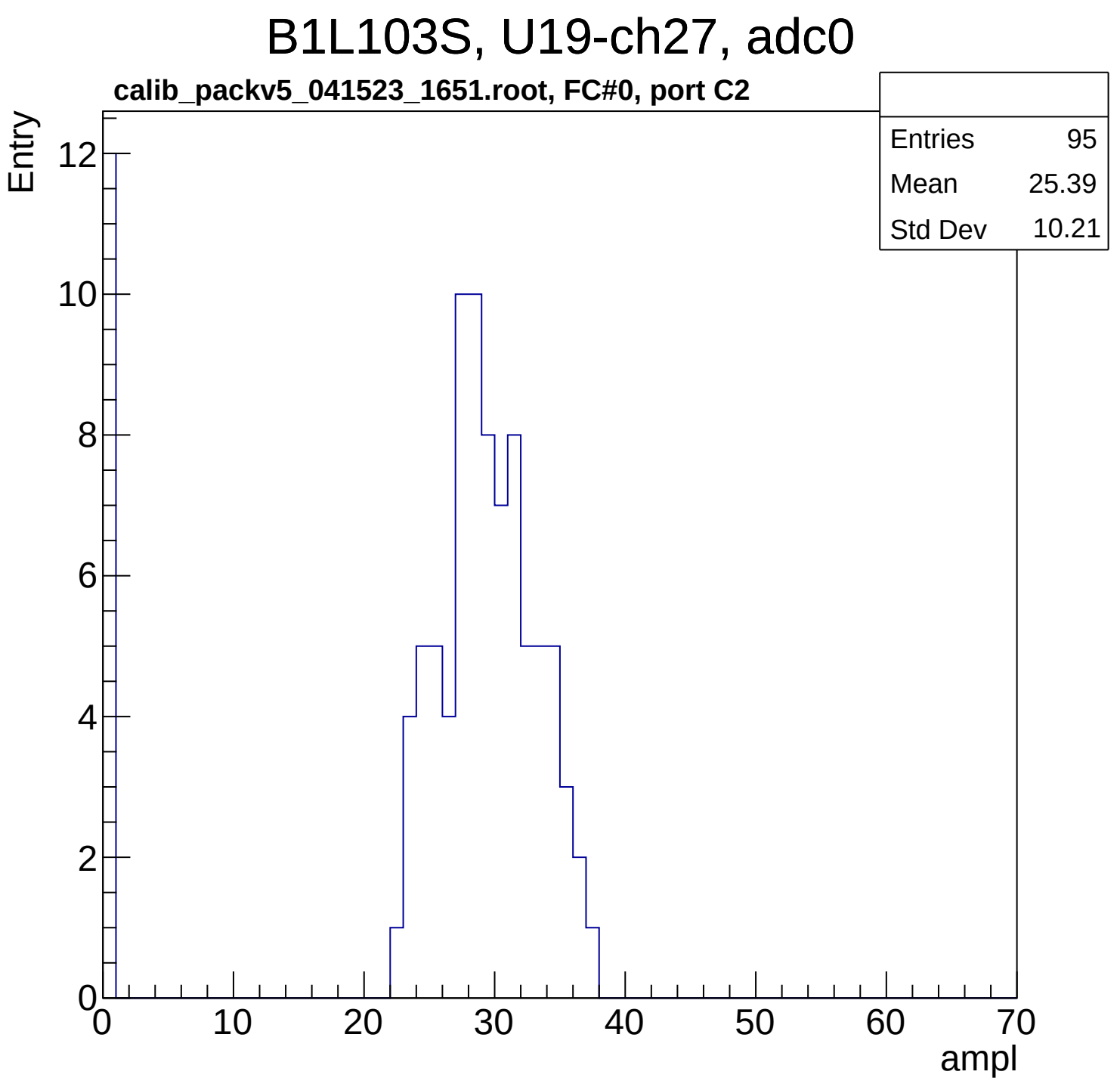
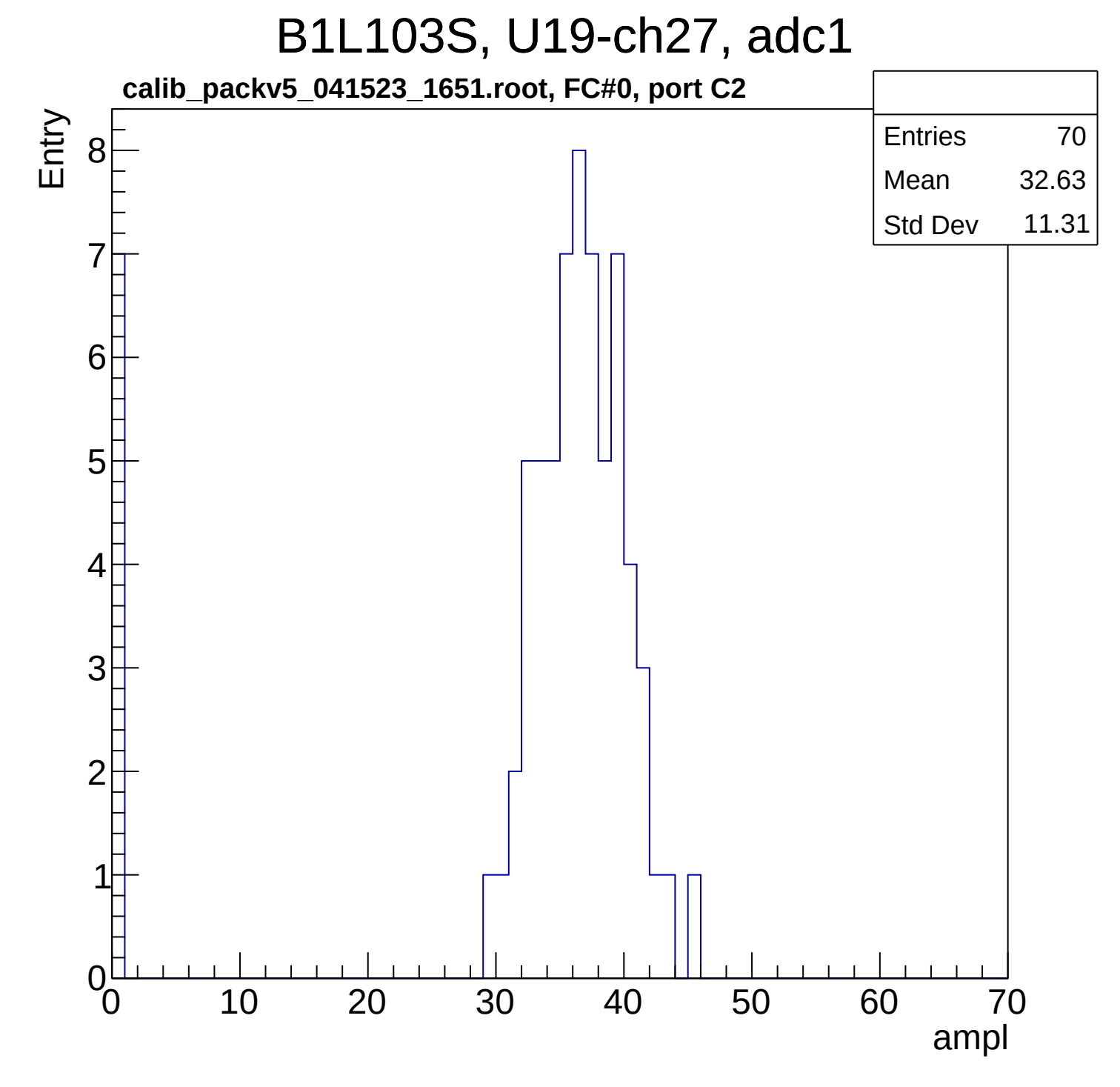
50
60
70
ampl


B1L103S, U19-ch26, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch27, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 25.39
Std Dev 10.21
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch27, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 32.63
Std Dev 11.31
Entry
ampl
0
1
2
3
4
5
6
7
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0
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40
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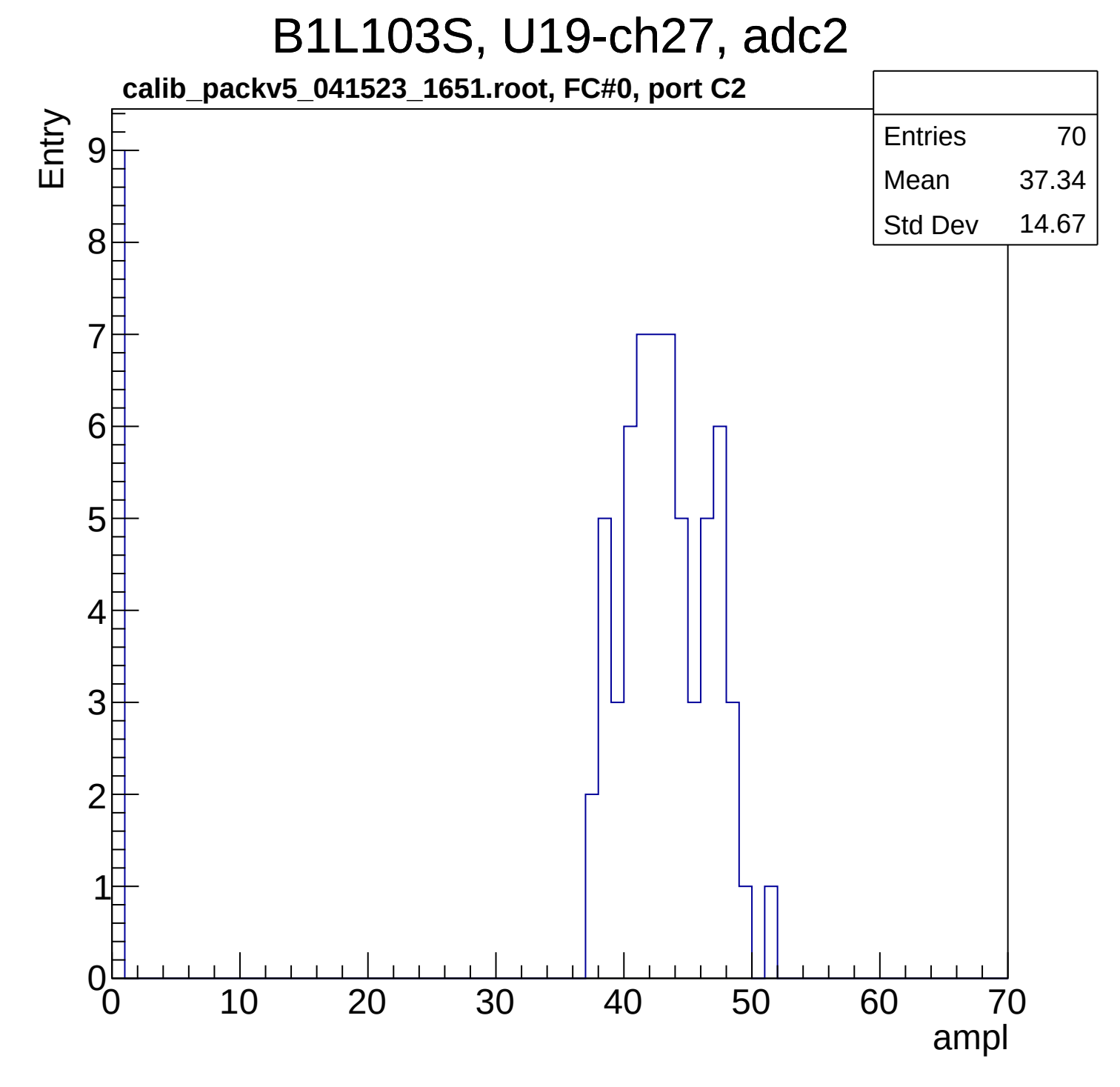
60
70


B1L103S, U19-ch27, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 37.34
Std Dev 14.67
Entry
ampl
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2
3
4
5
6
7
8
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0
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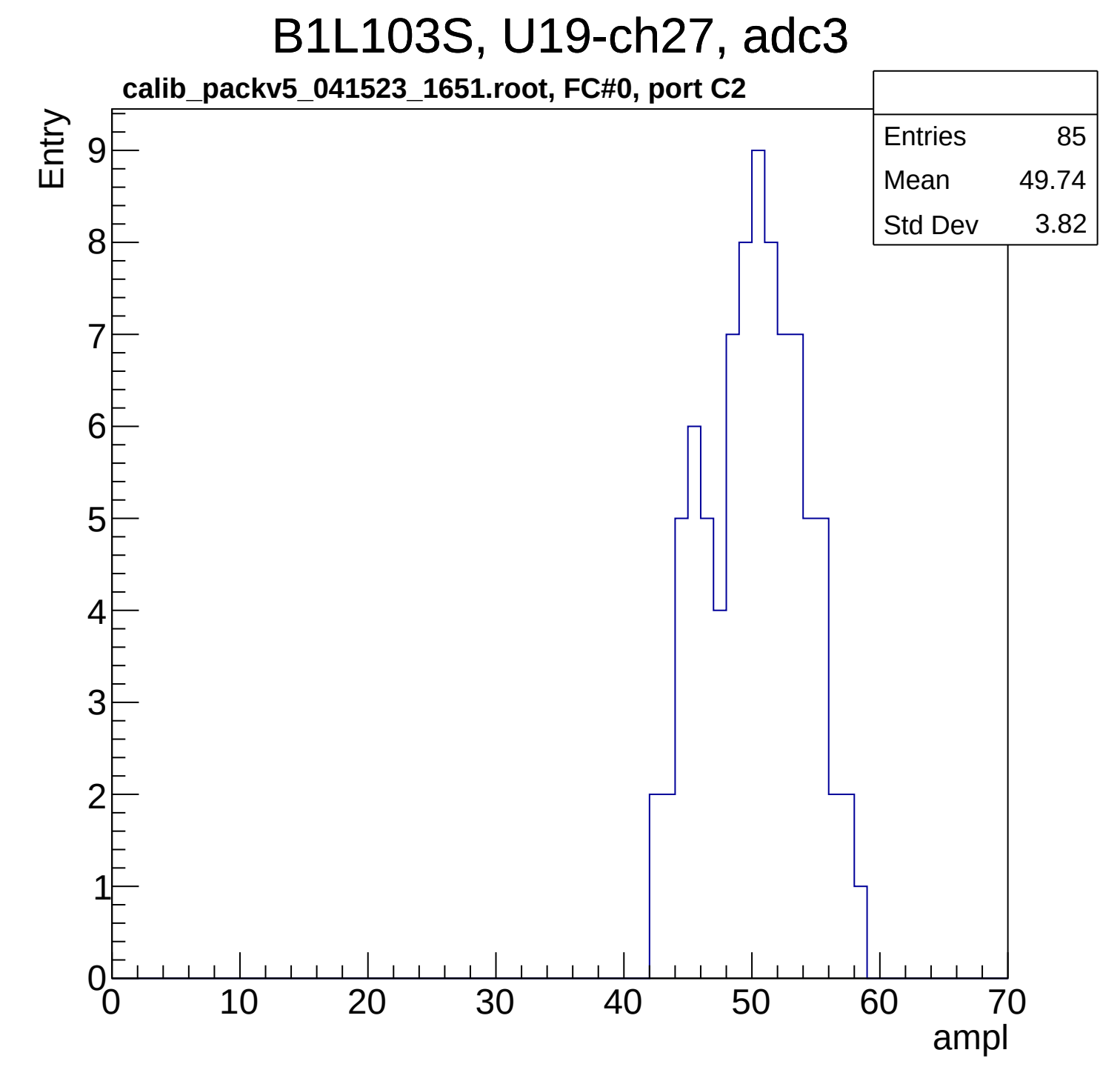
40
50
60
70


B1L103S, U19-ch27, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 49.74
Std Dev 3.82
Entry
ampl
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2
3
4
5
6
7
8
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0
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40
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60
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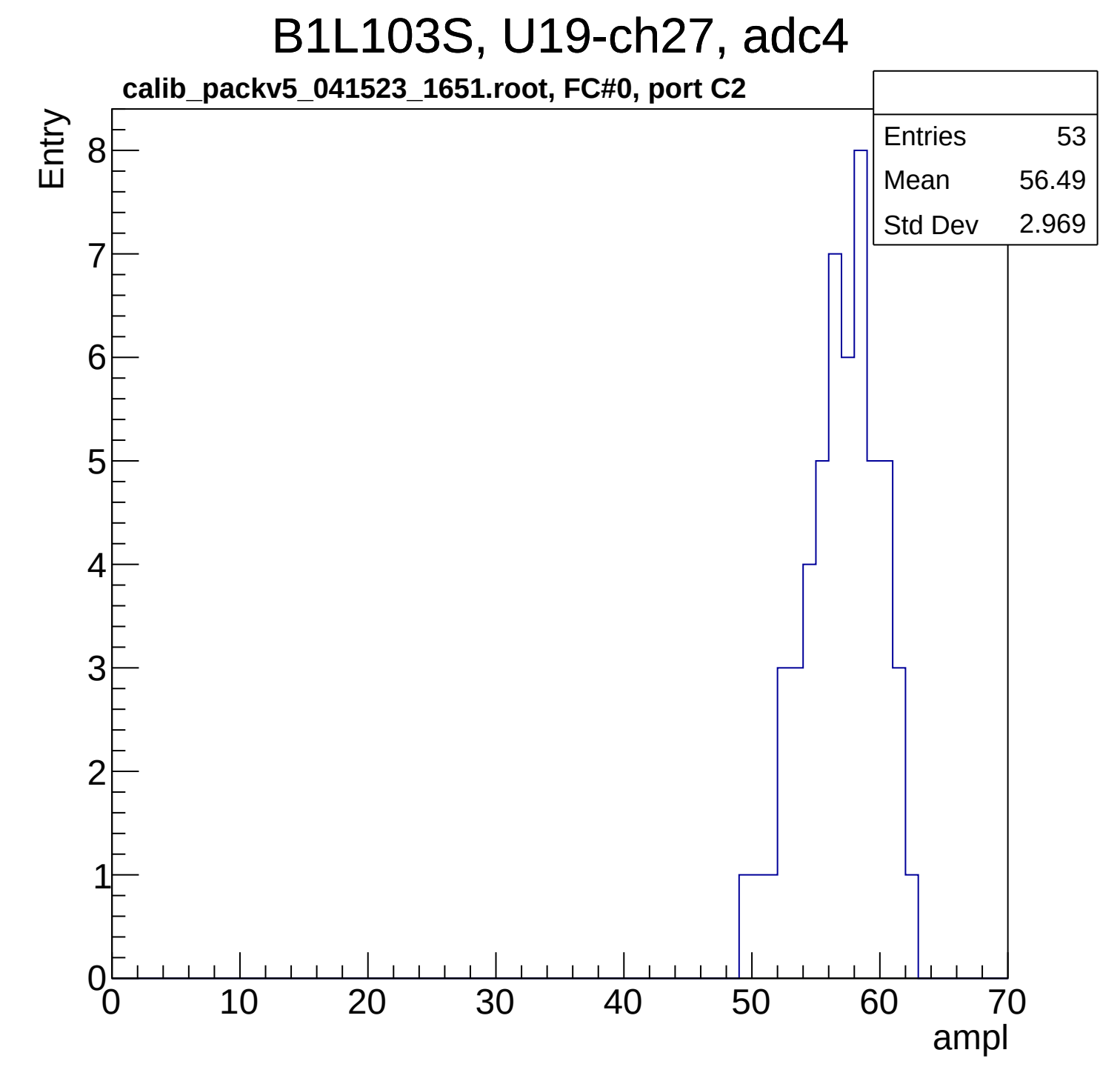
B1L103S, U19-ch27, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 56.49
Std Dev 2.969
Entry
ampl
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1
2
3
4
5
6
7
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0
10
20
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40
50
60
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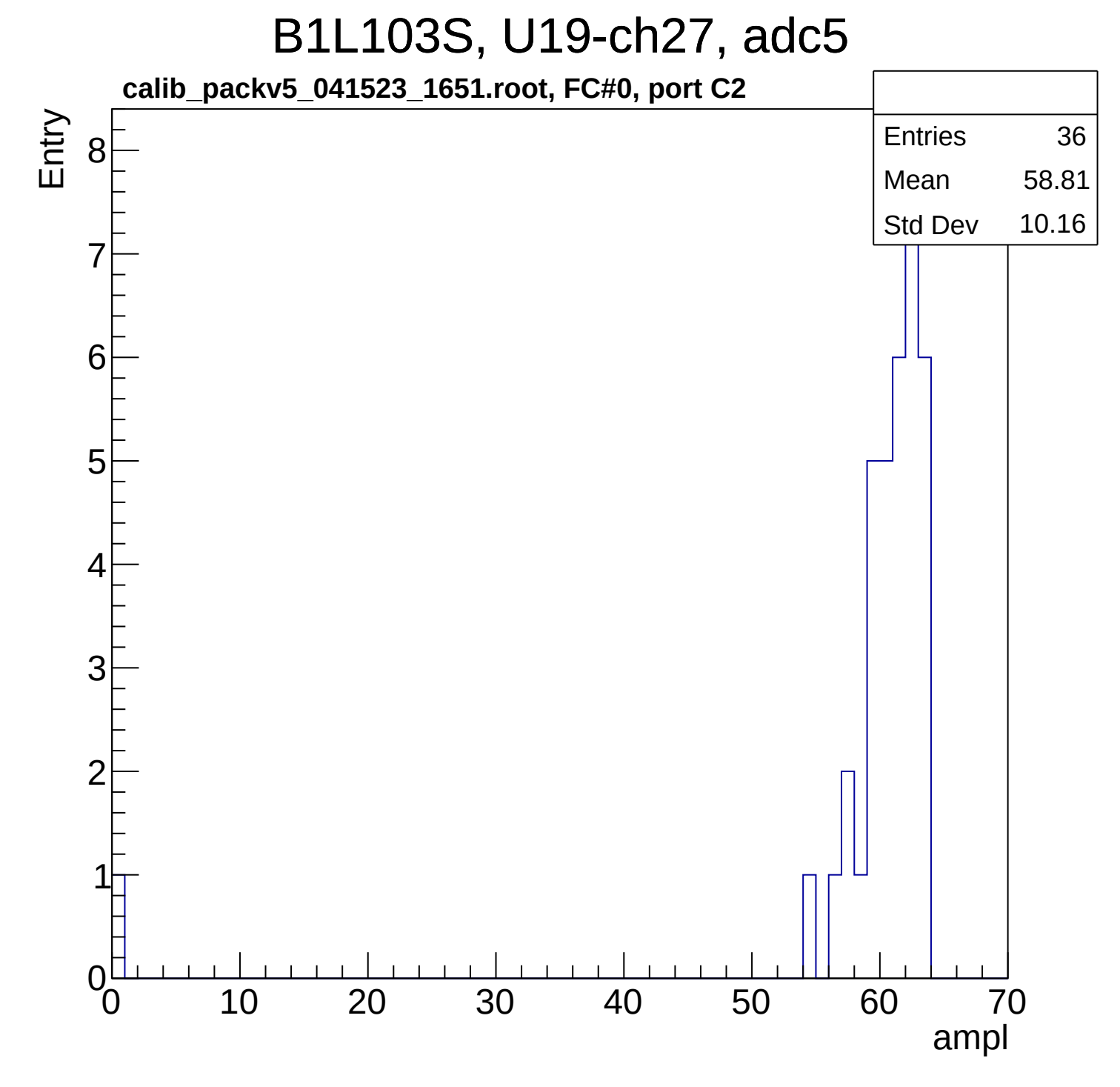
B1L103S, U19-ch27, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 58.81
Std Dev 10.16
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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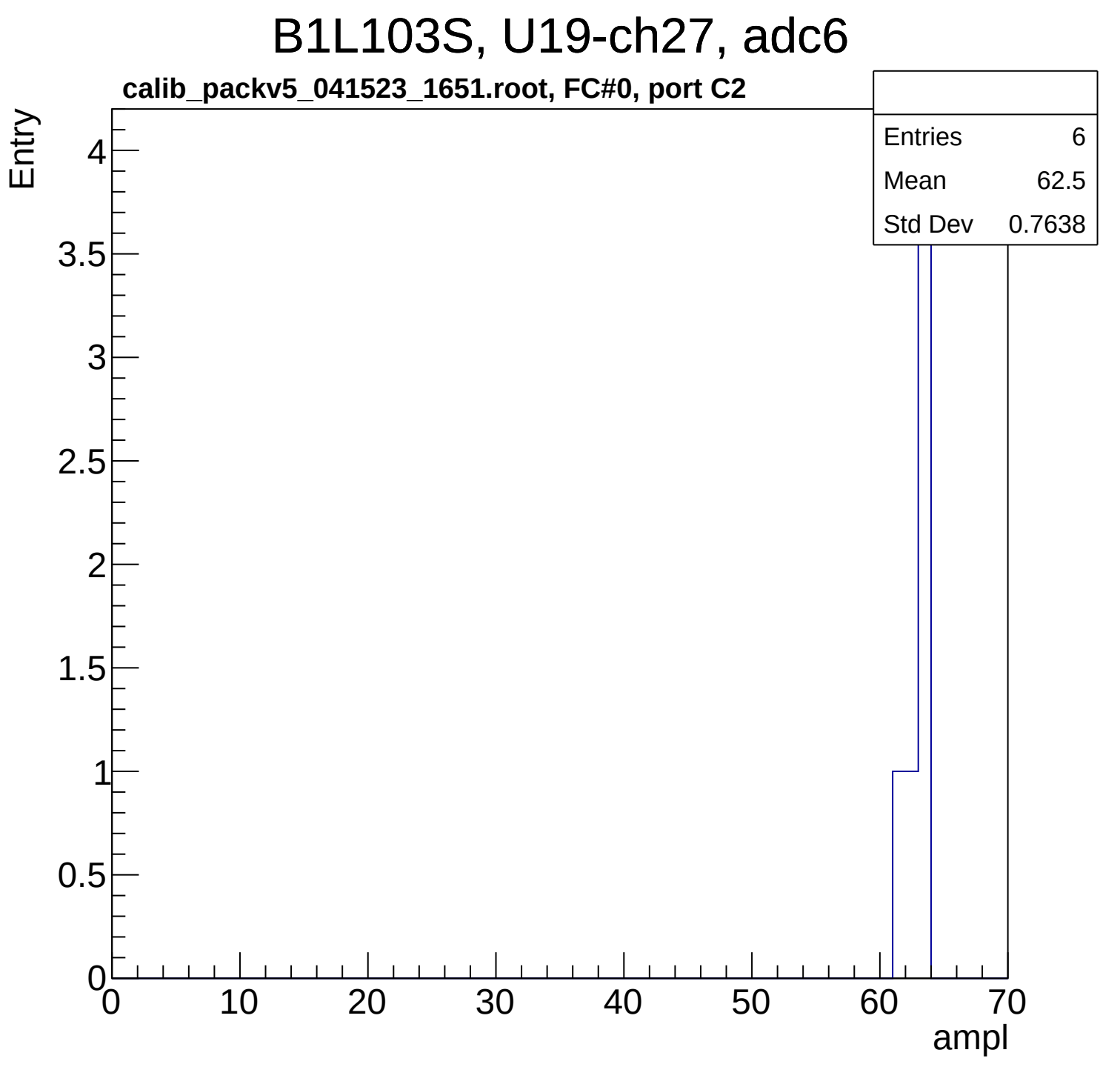
B1L103S, U19-ch27, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 62.5
Std Dev 0.7638
Entry
ampl
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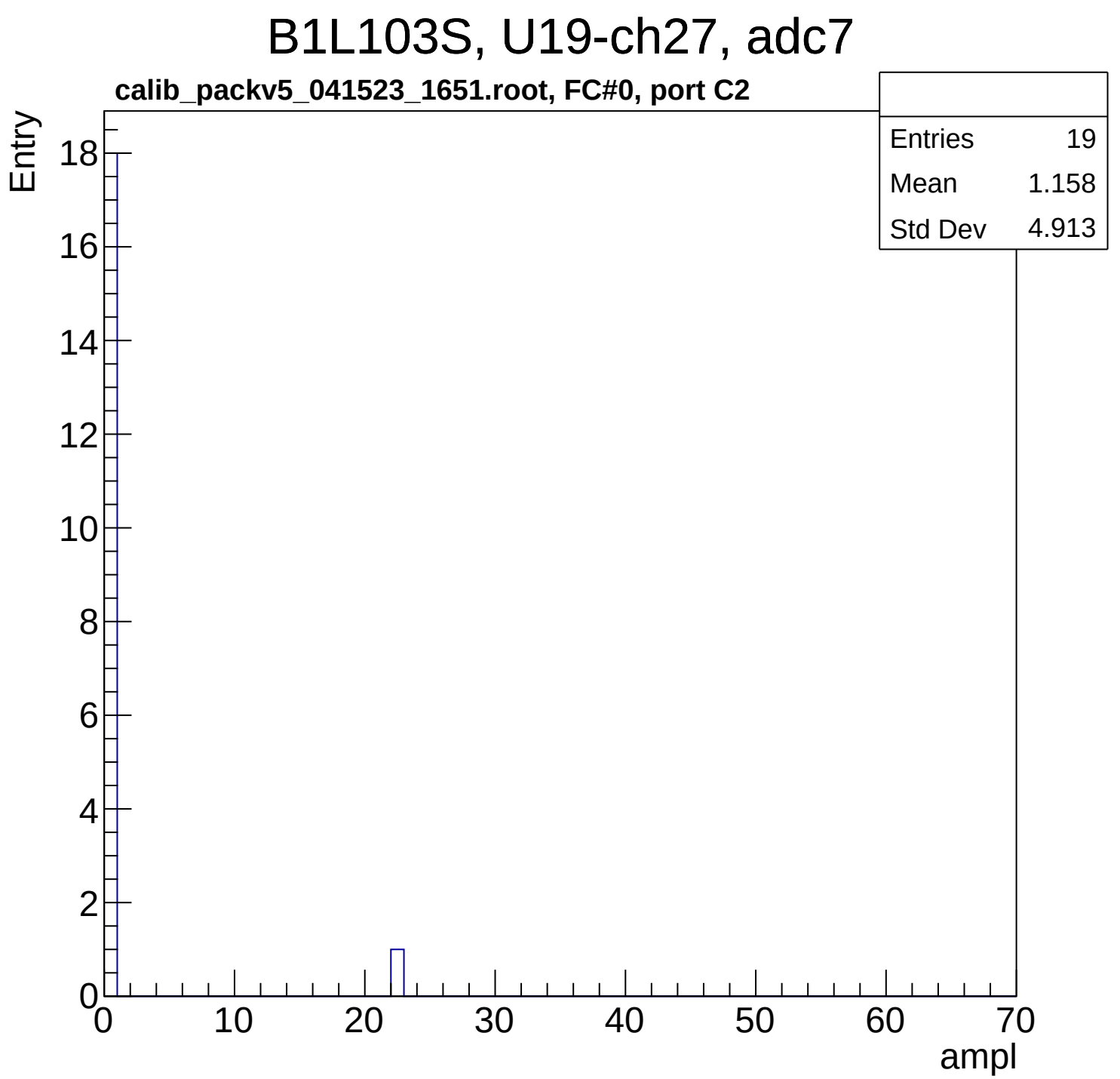
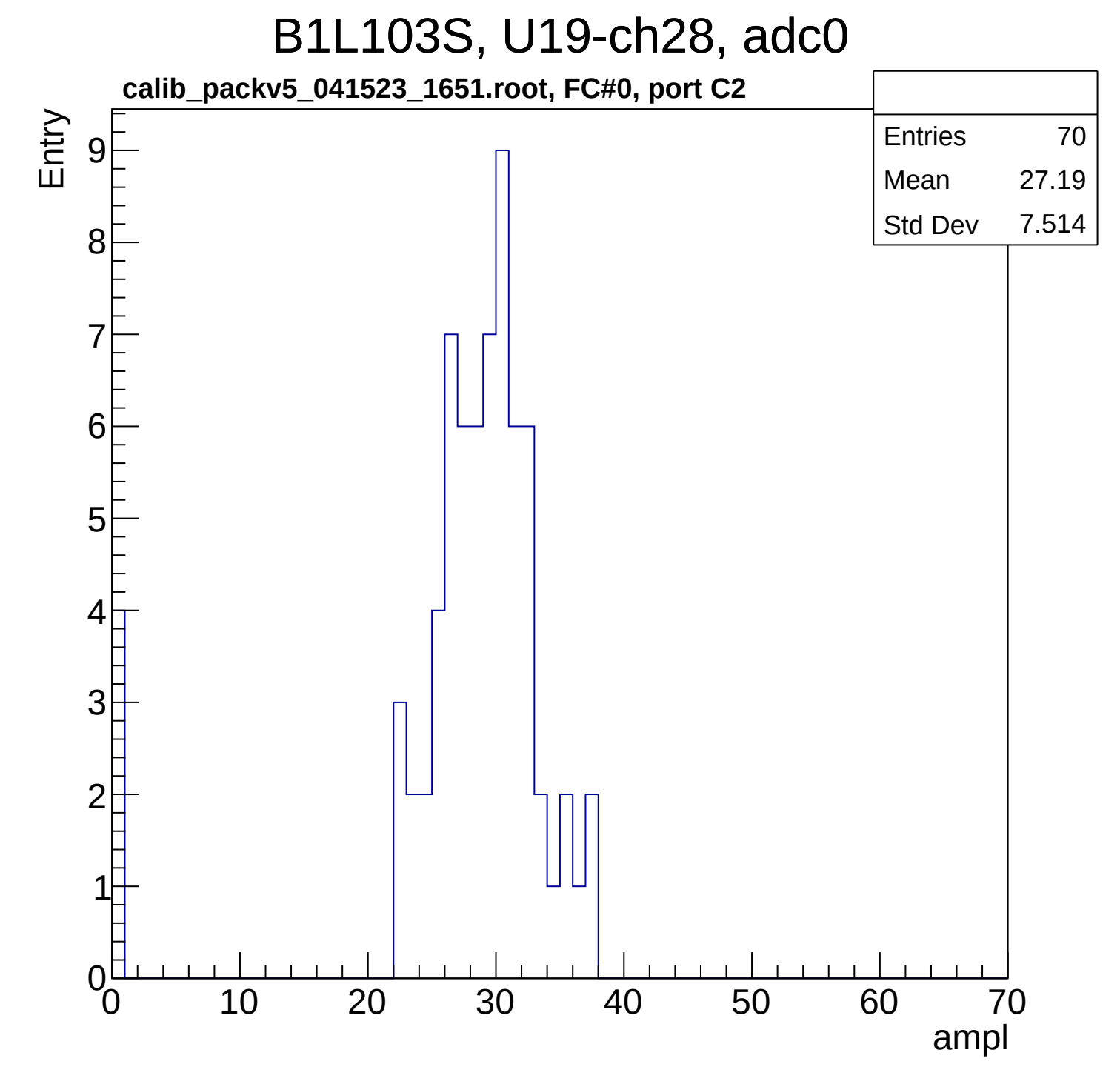
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U19-ch27, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.158
Std Dev 4.913
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch28, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 27.19
Std Dev 7.514
Entry
ampl
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2
3
4
5
6
7
8
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0
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40
50
60
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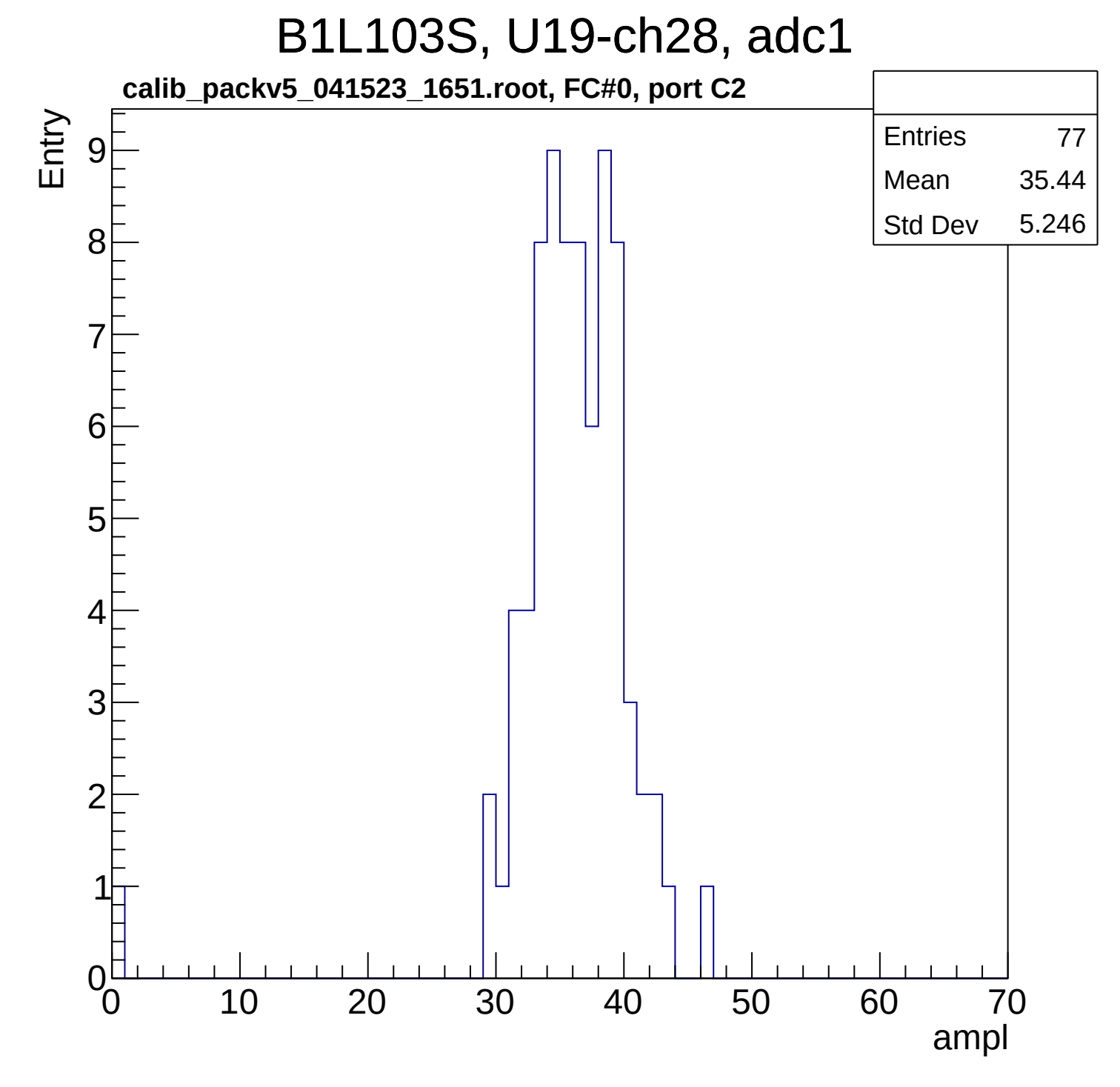
B1L103S, U19-ch28, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 35.44
Std Dev 5.246
Entry
ampl
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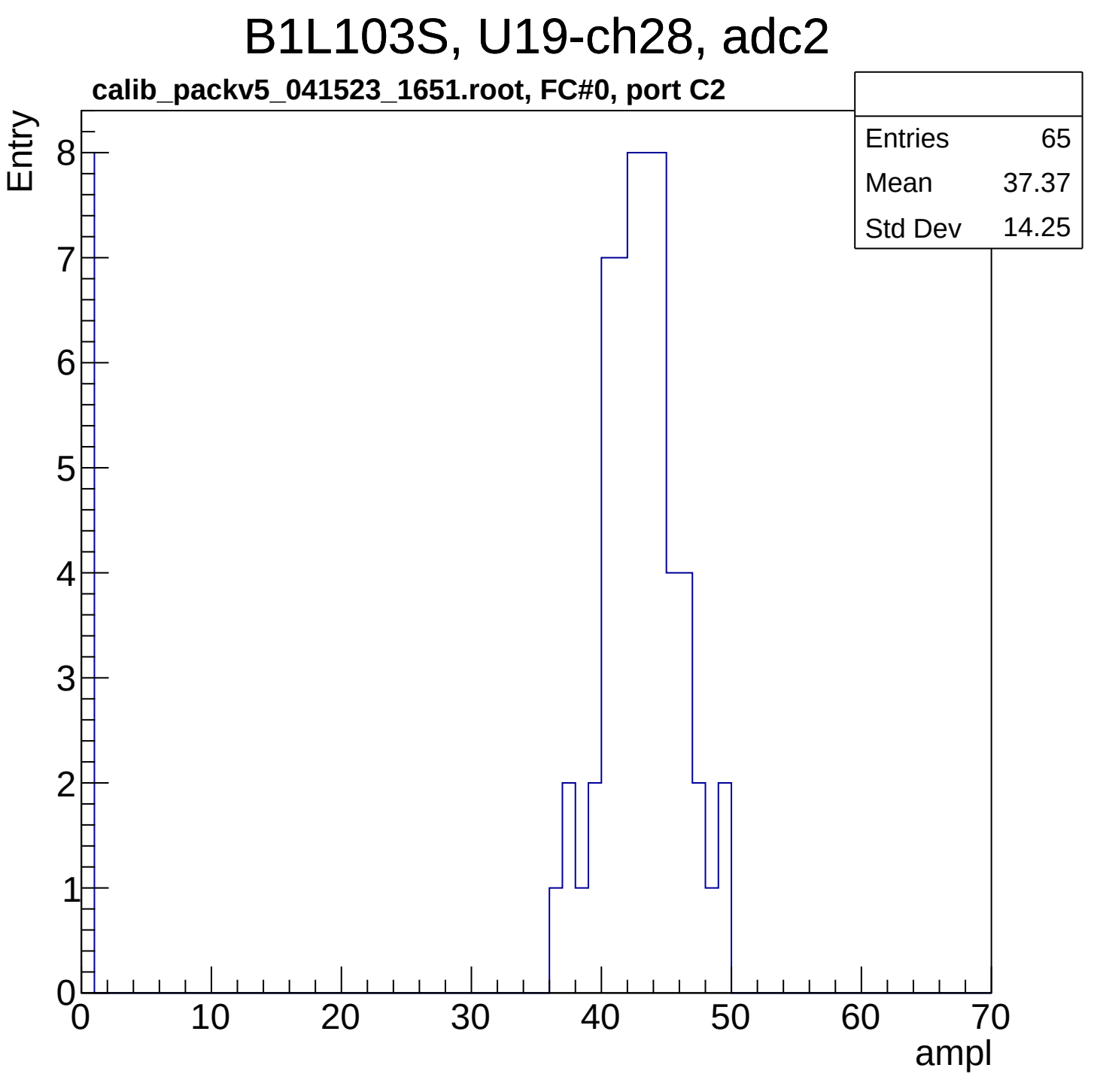
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch28, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 37.37
Std Dev 14.25
Entry
ampl
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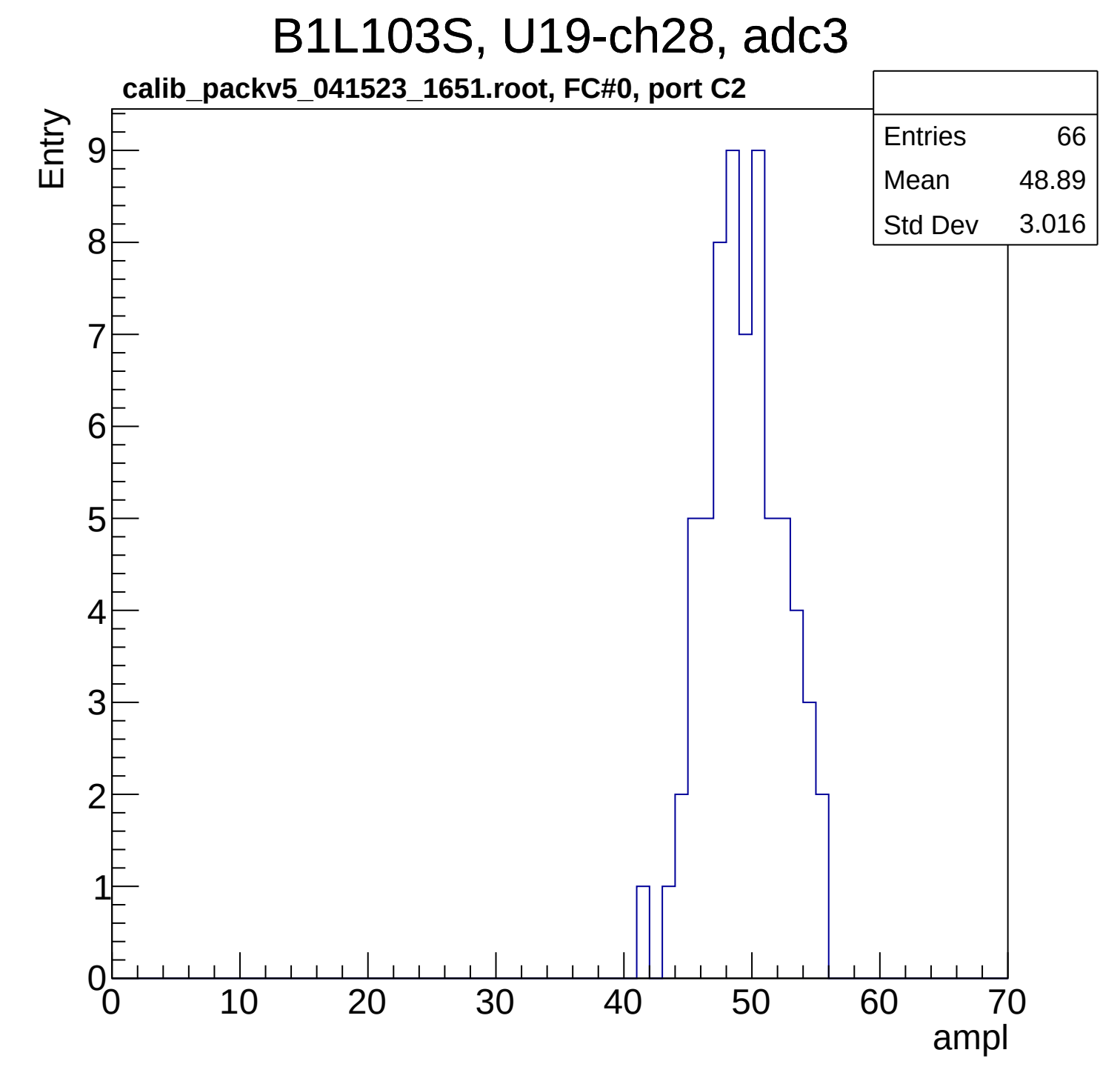
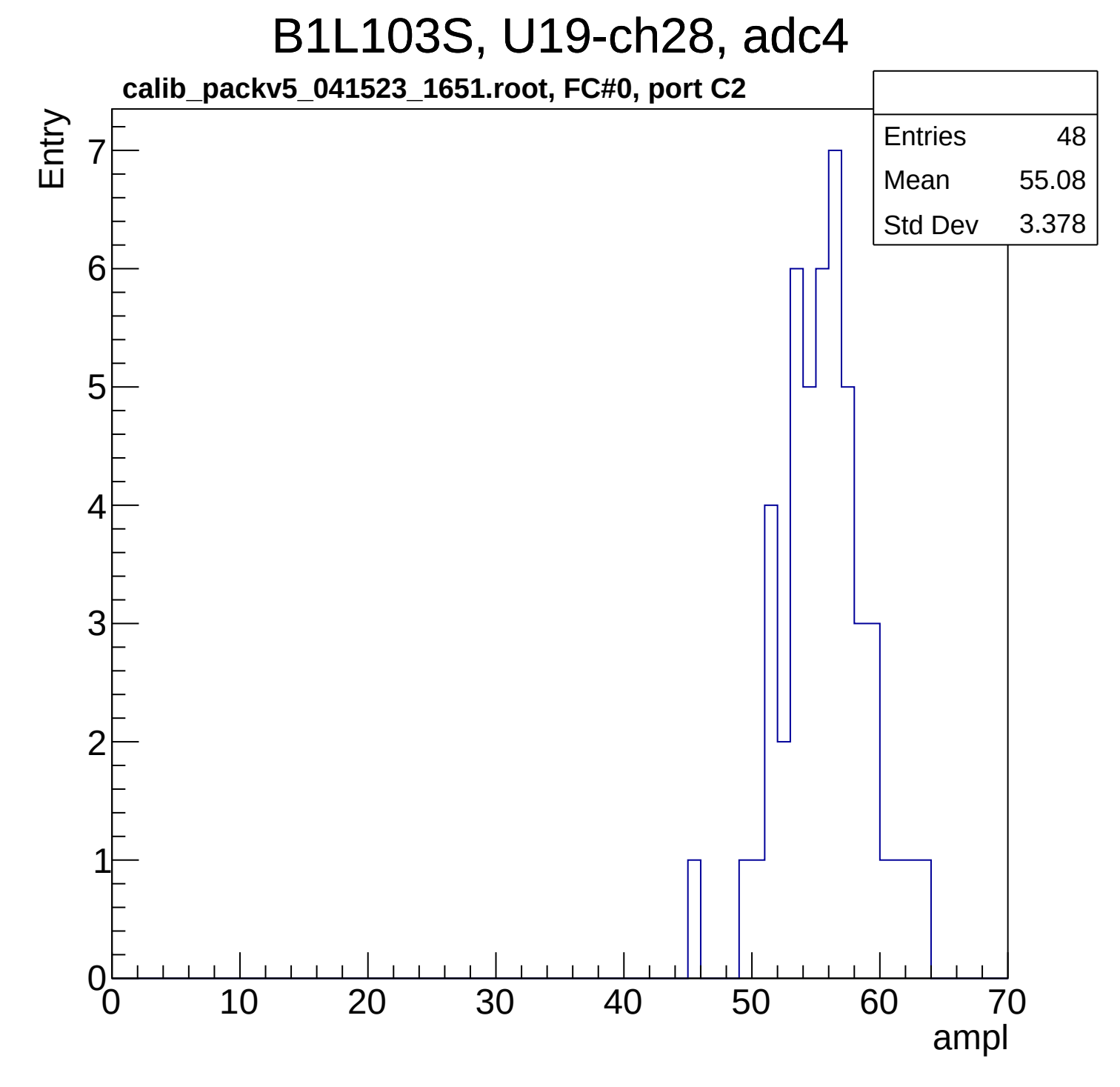
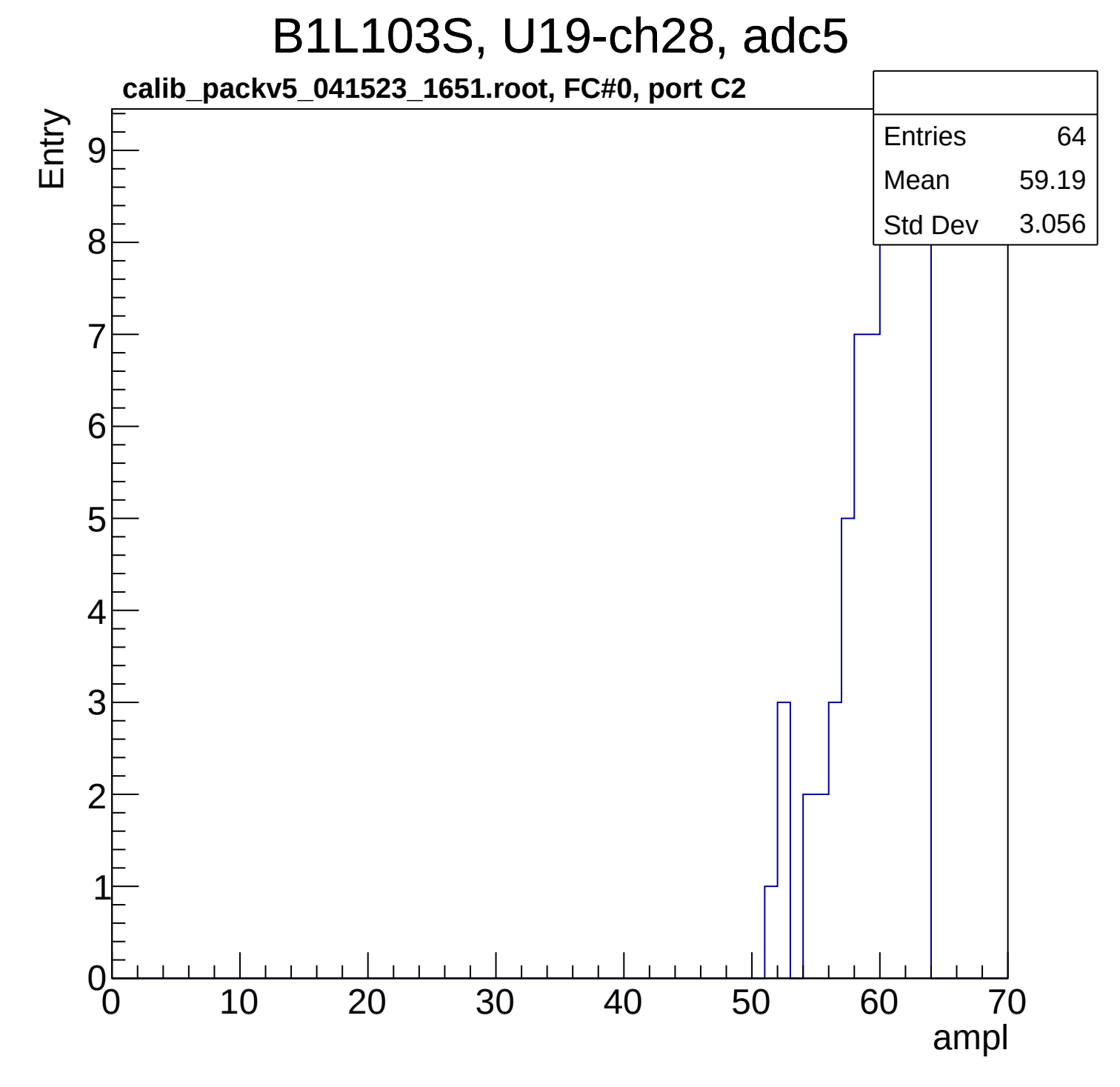
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch28, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 48.89
Std Dev 3.016
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch28, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 55.08
Std Dev 3.378
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch28, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 59.19
Std Dev 3.056
Entry
ampl
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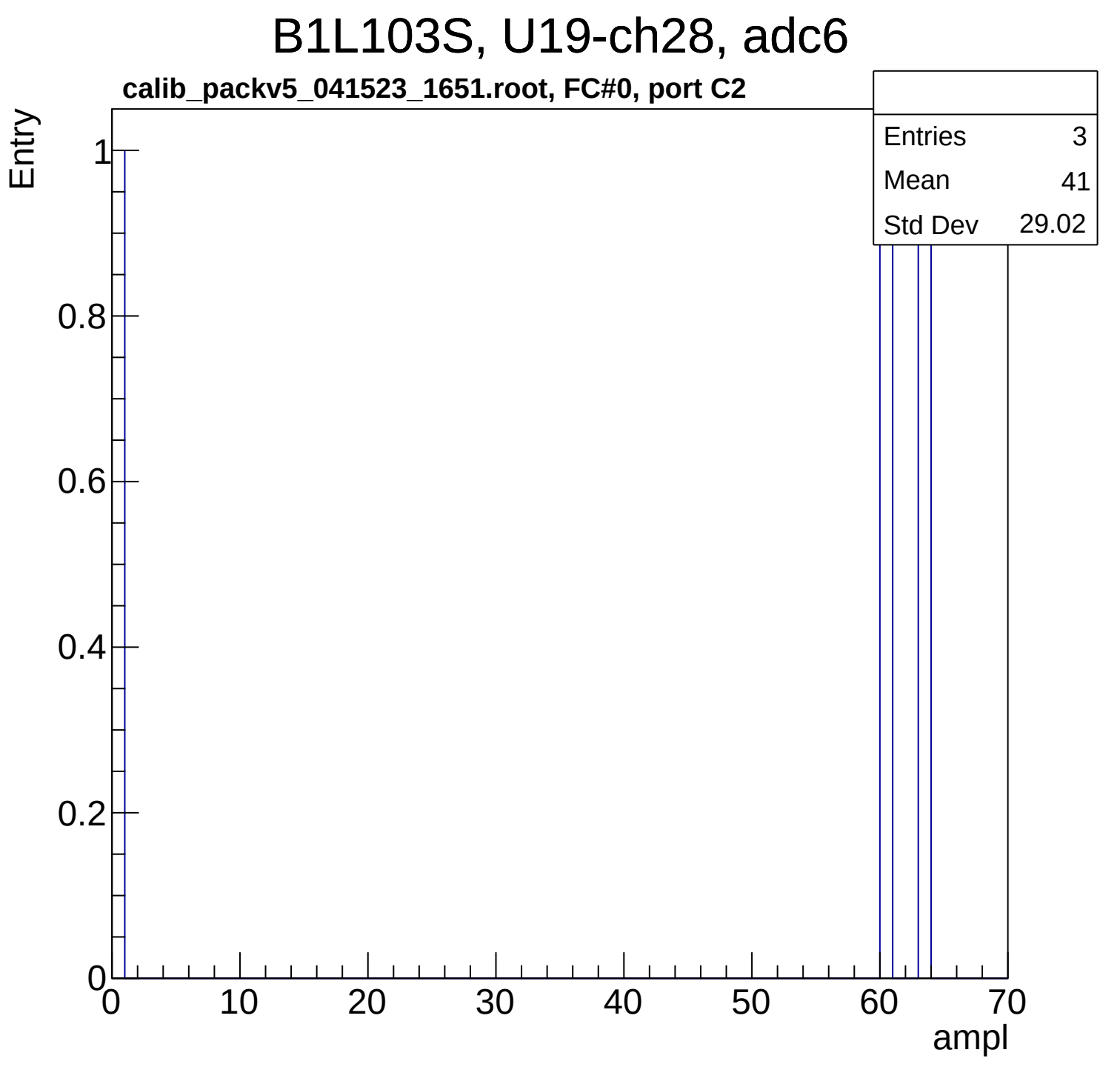
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch28, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 41
Std Dev 29.02
Entry
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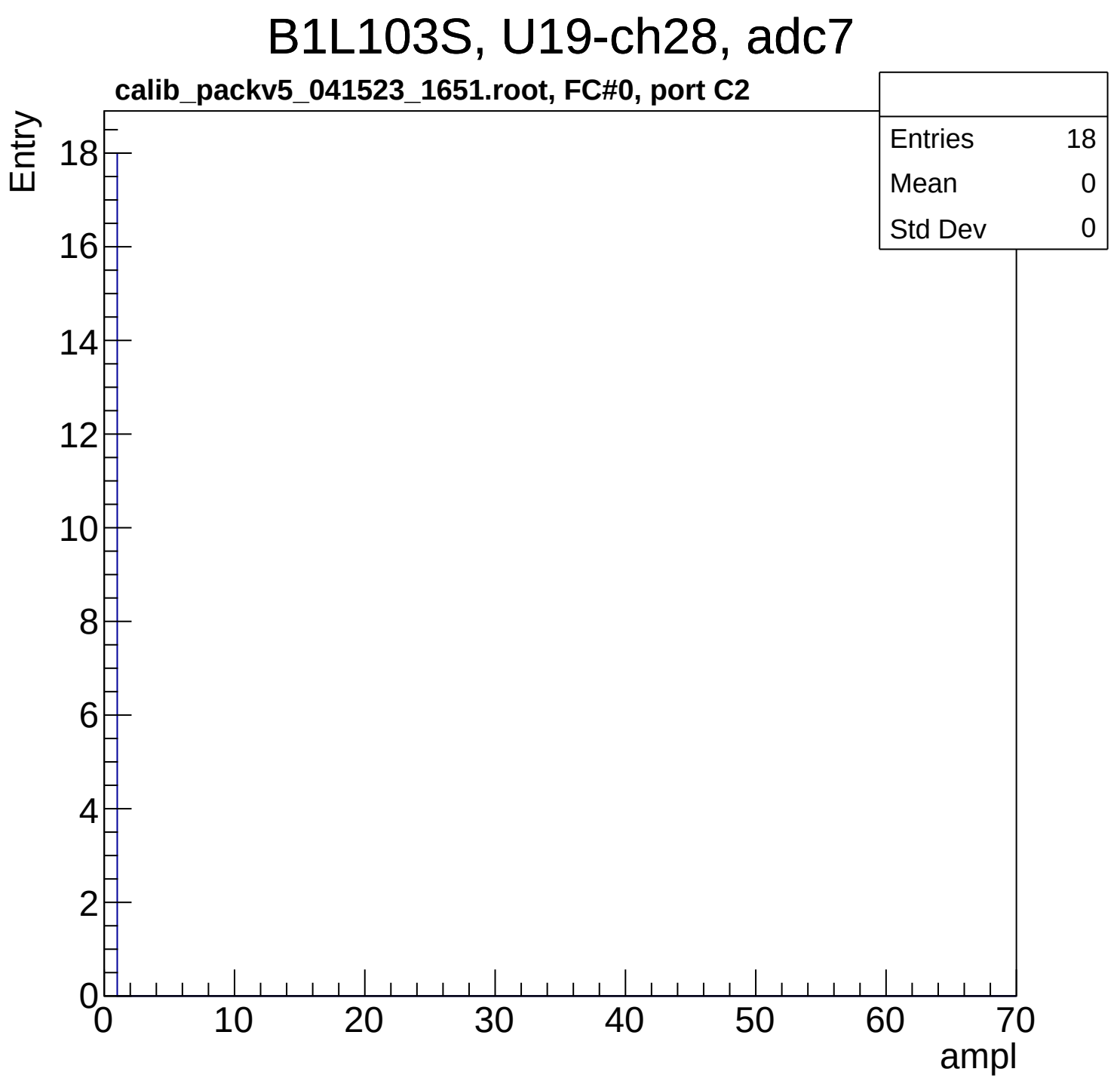
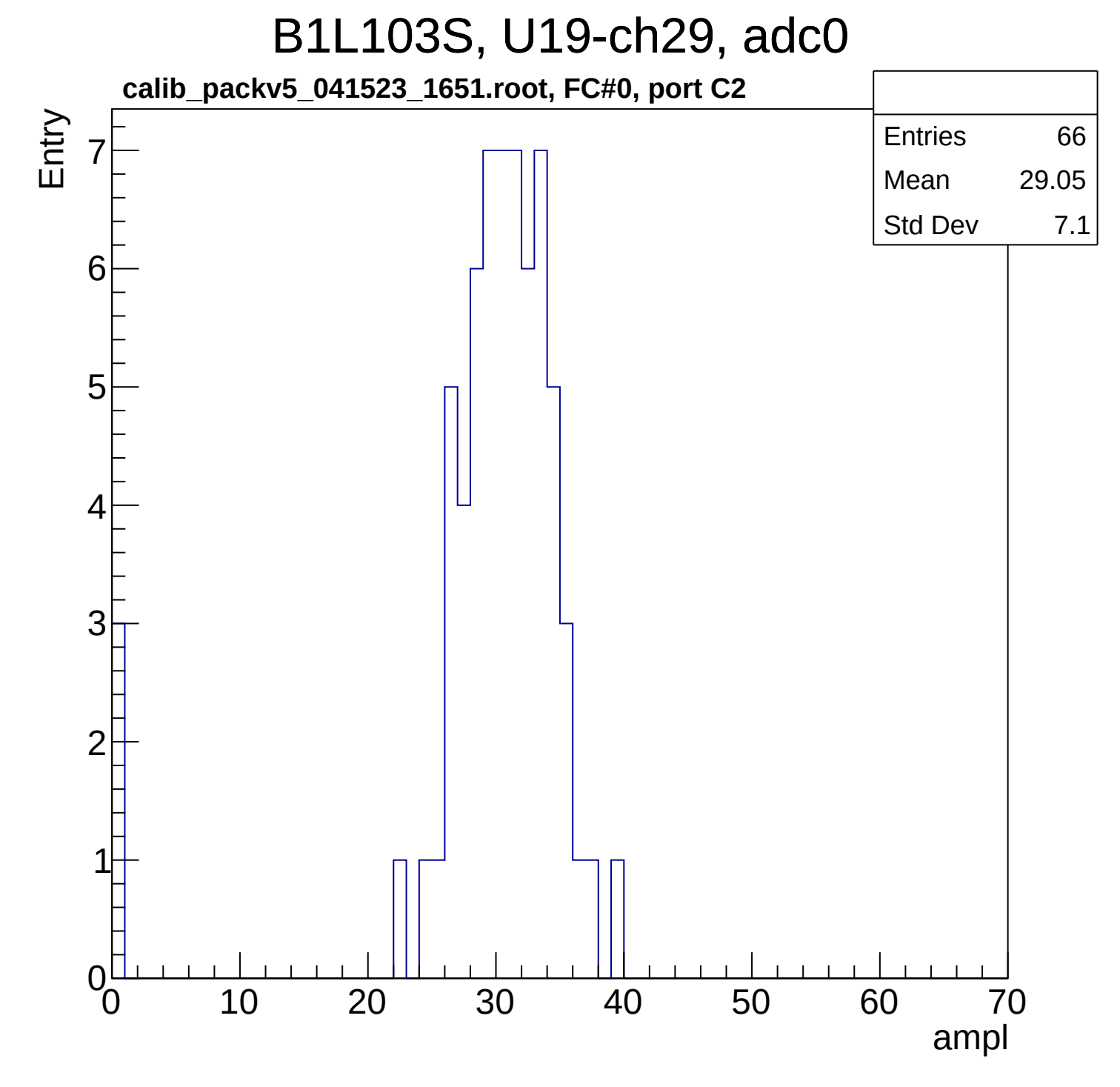
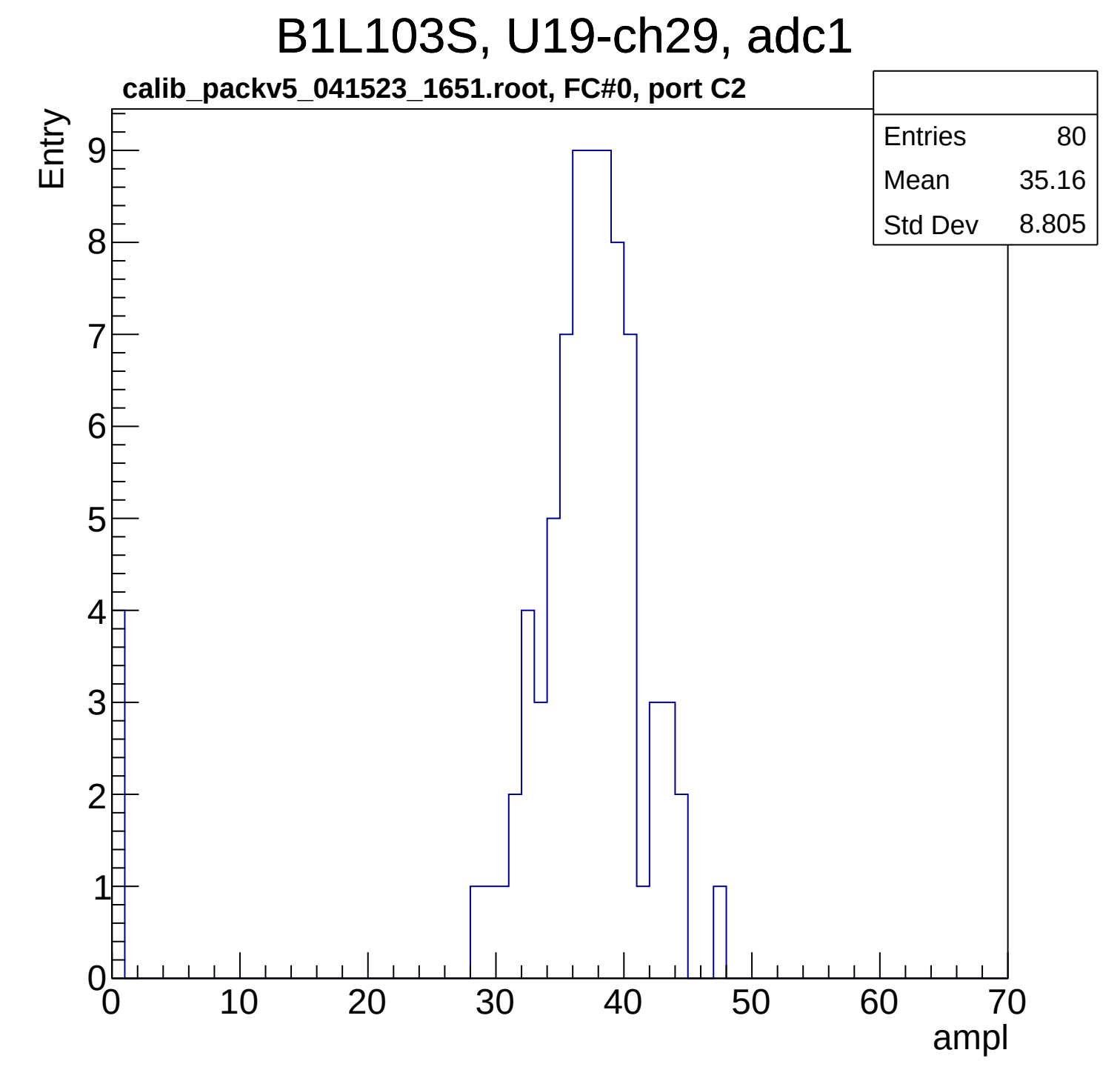
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch28, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch29, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 29.05
Std Dev 7.1
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch29, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 35.16
Std Dev 8.805
Entry
ampl
0
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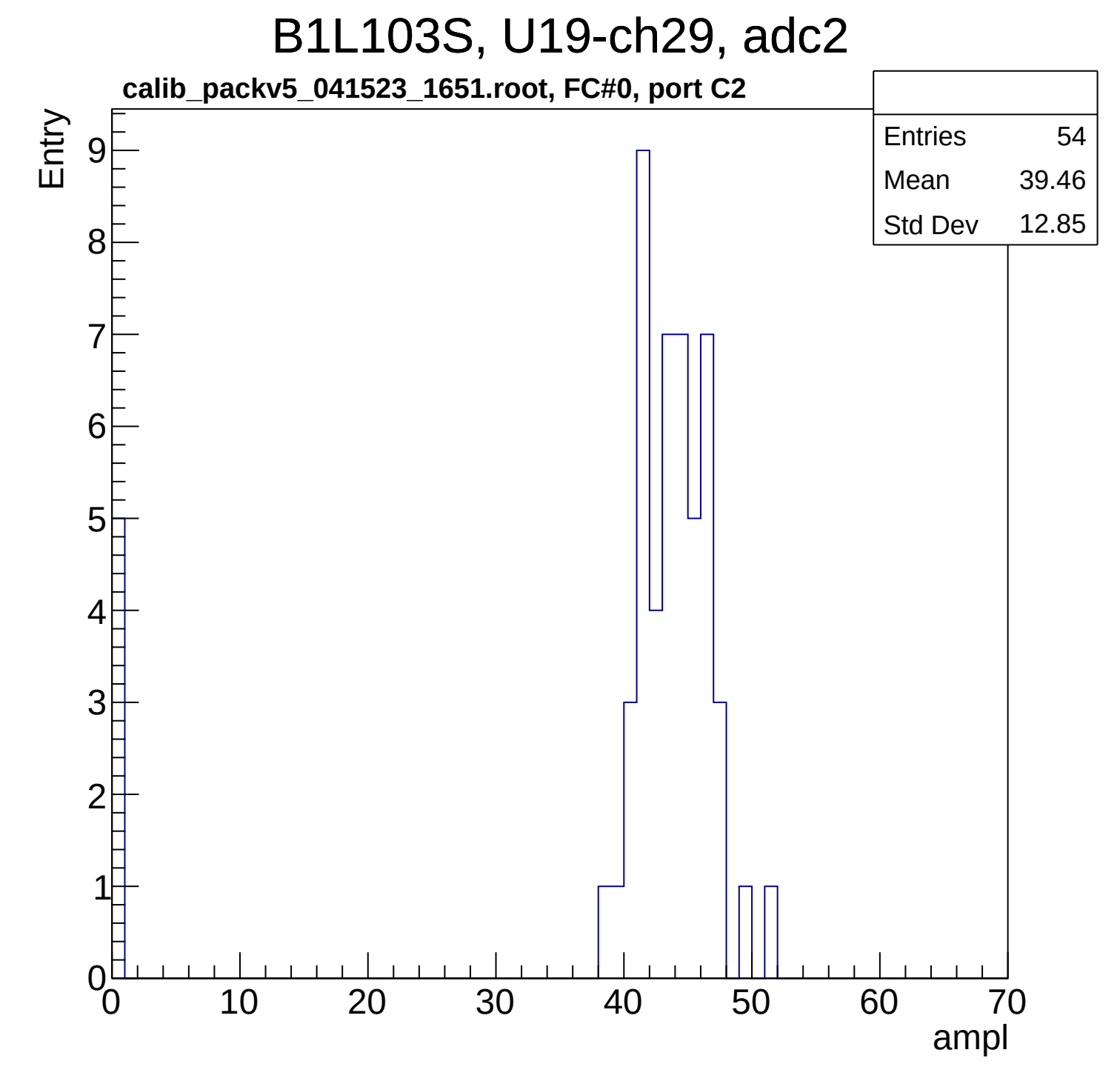
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch29, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 39.46
Std Dev 12.85
Entry
ampl
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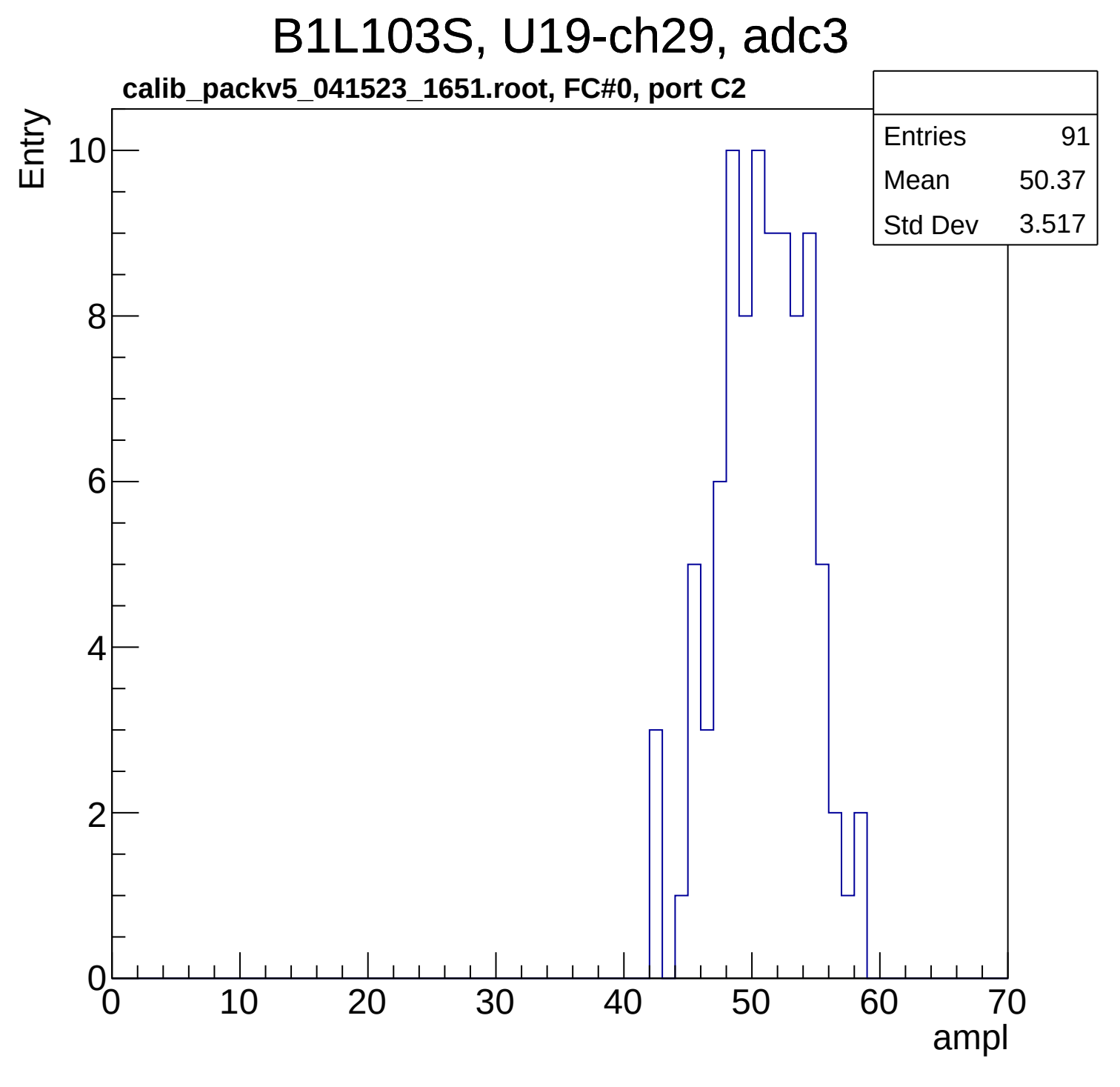
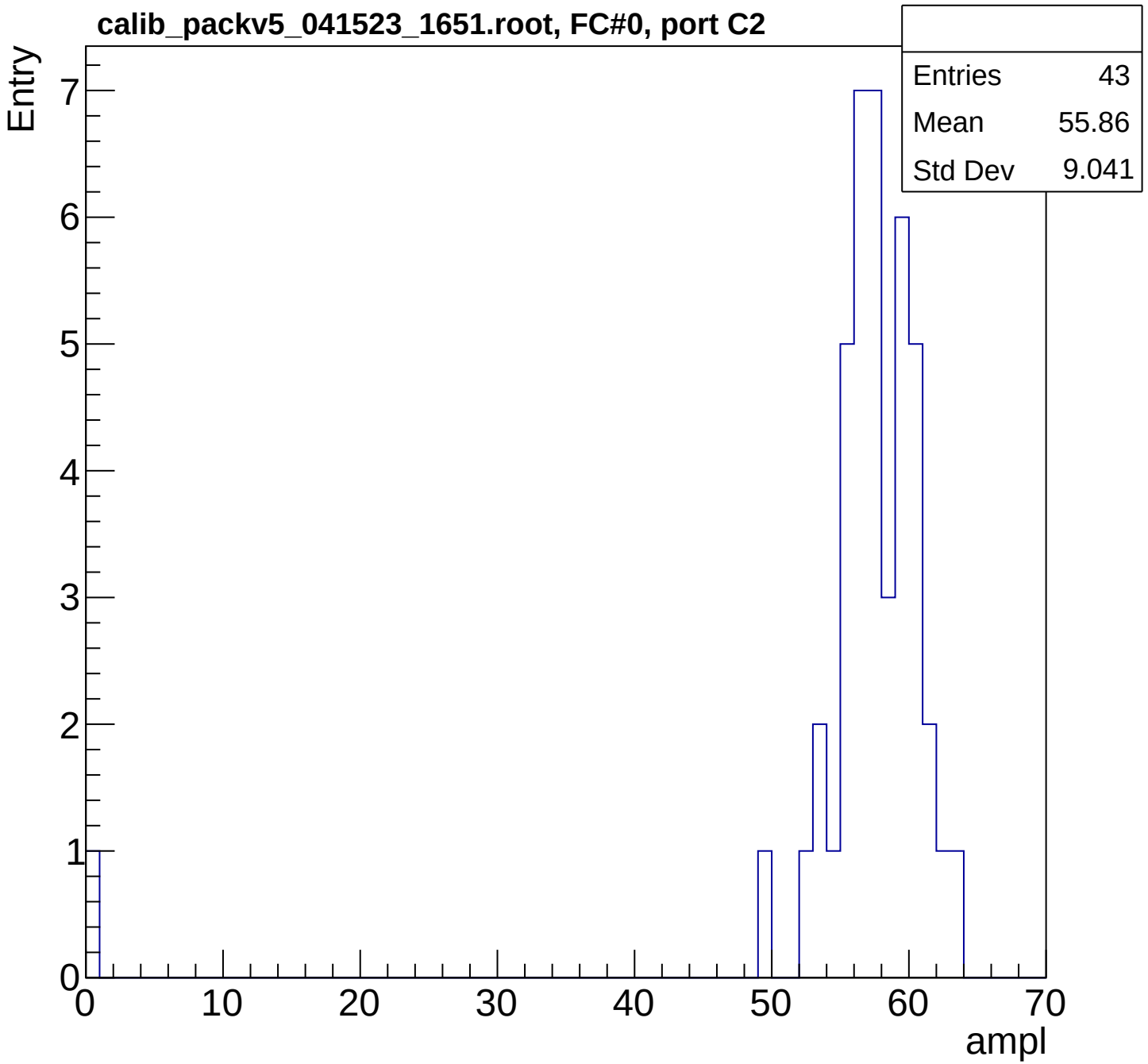
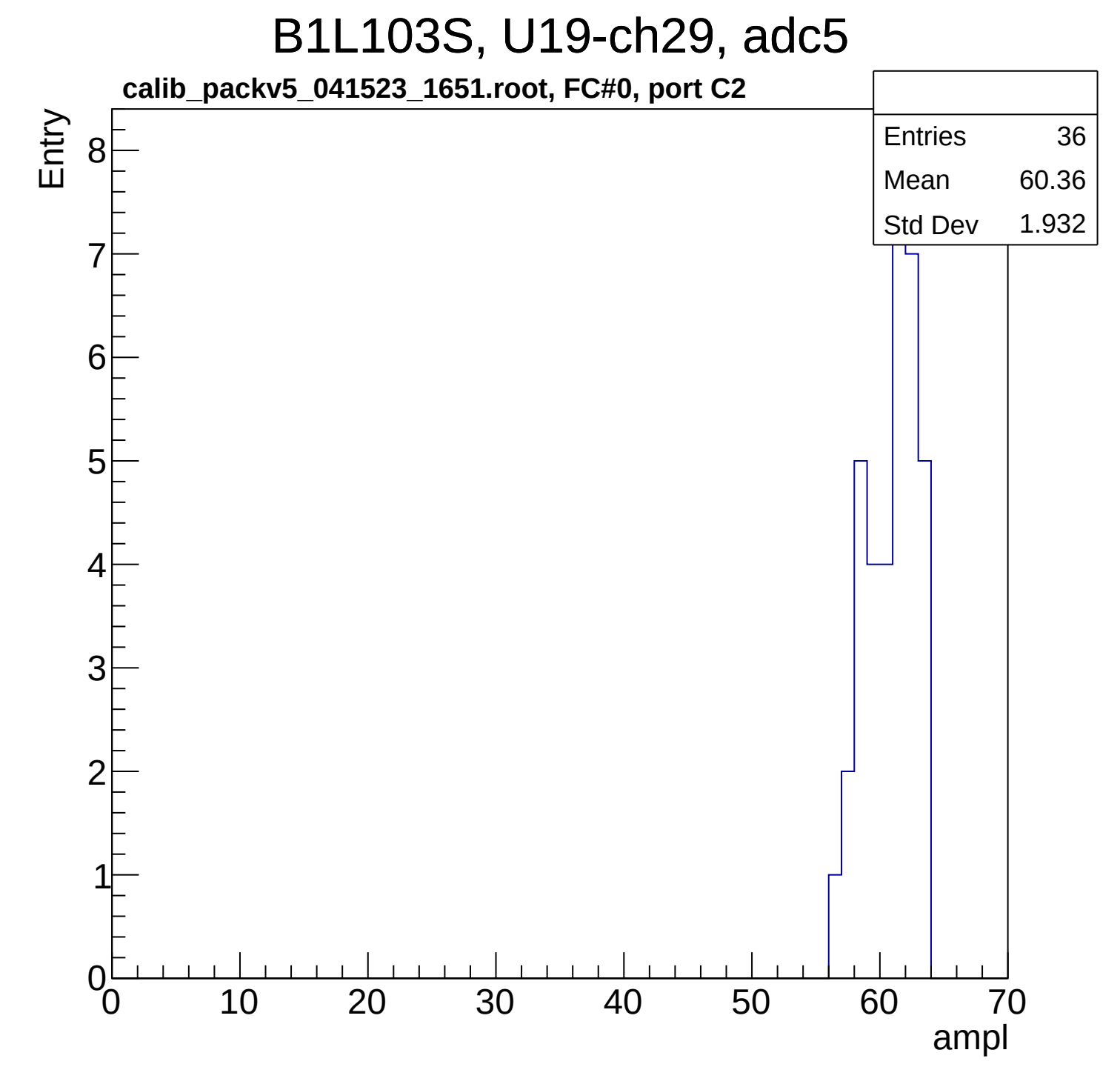
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch29, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 50.37
Std Dev 3.517
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch29, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 55.86
Std Dev 9.041
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch29, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 60.36
Std Dev 1.932
Entry
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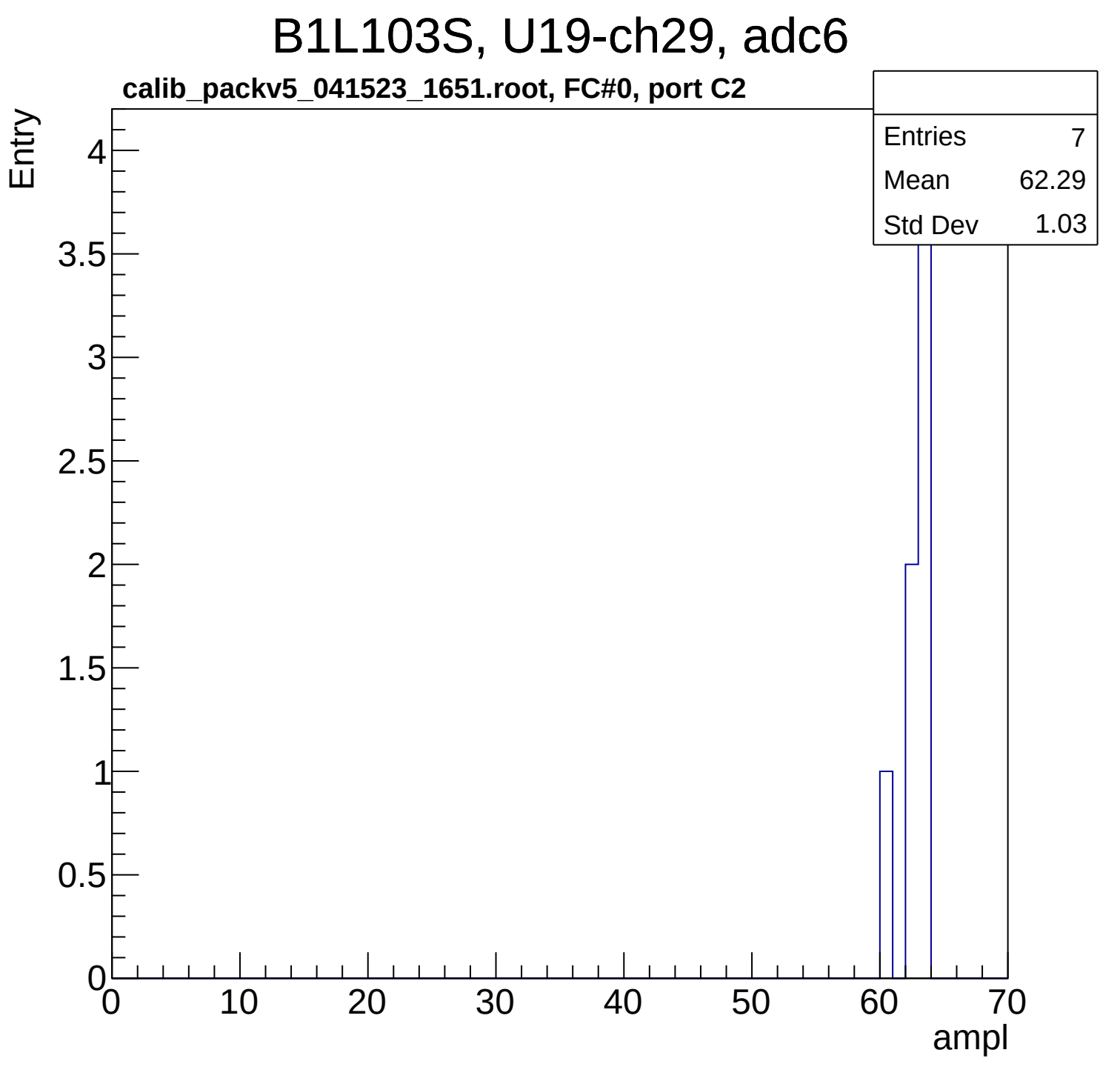
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch29, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 62.29
Std Dev 1.03
Entry
ampl
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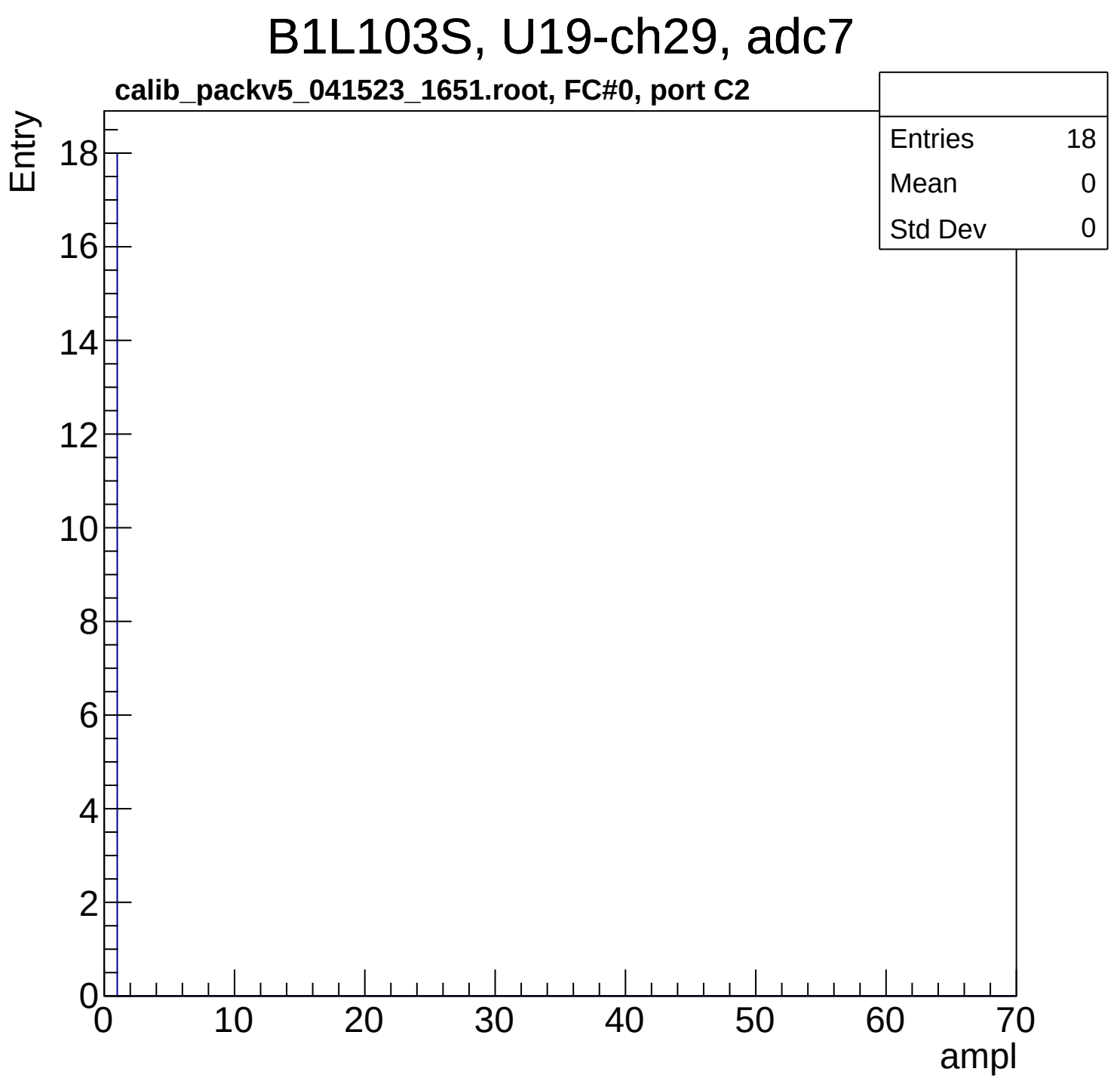
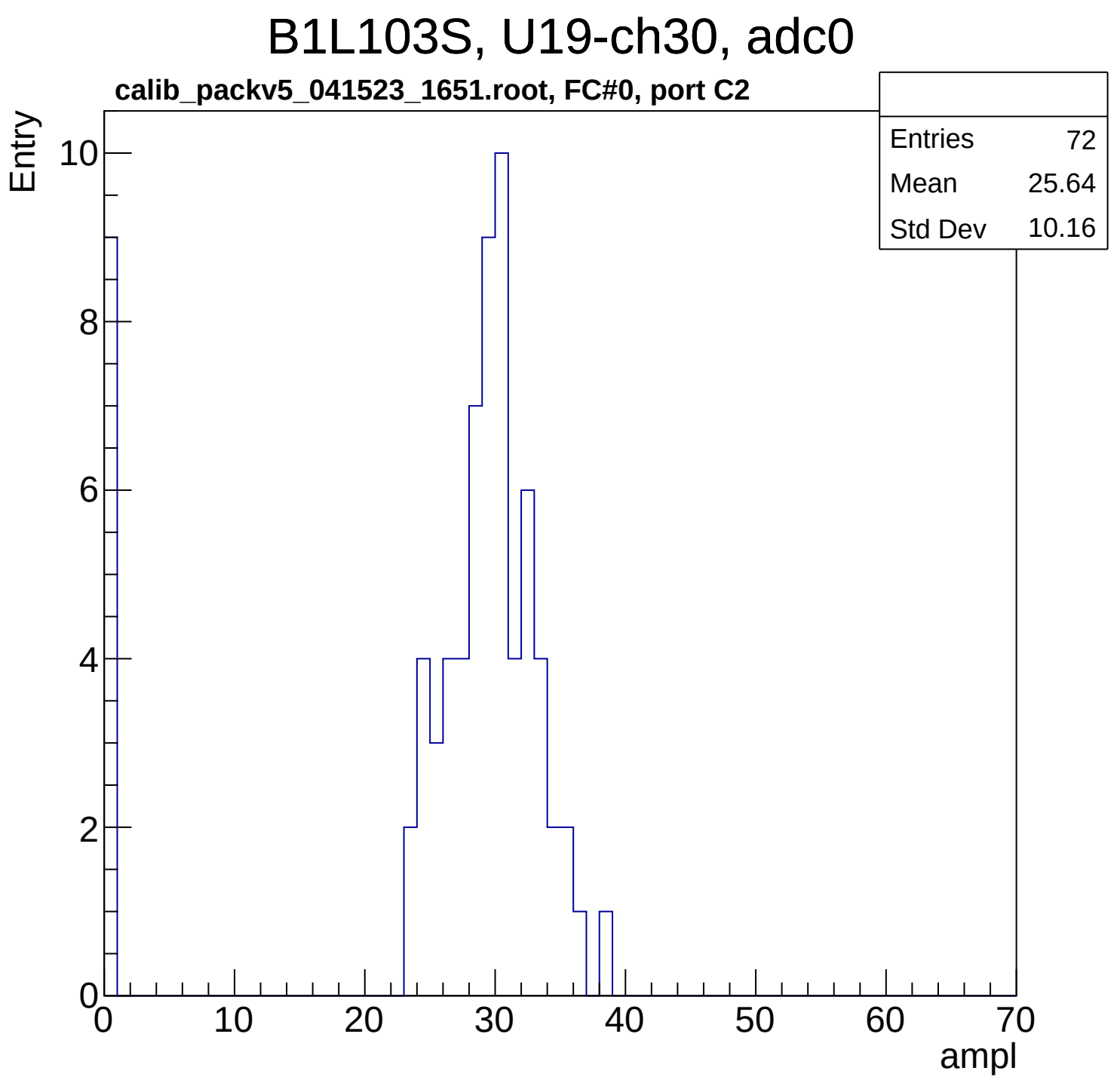
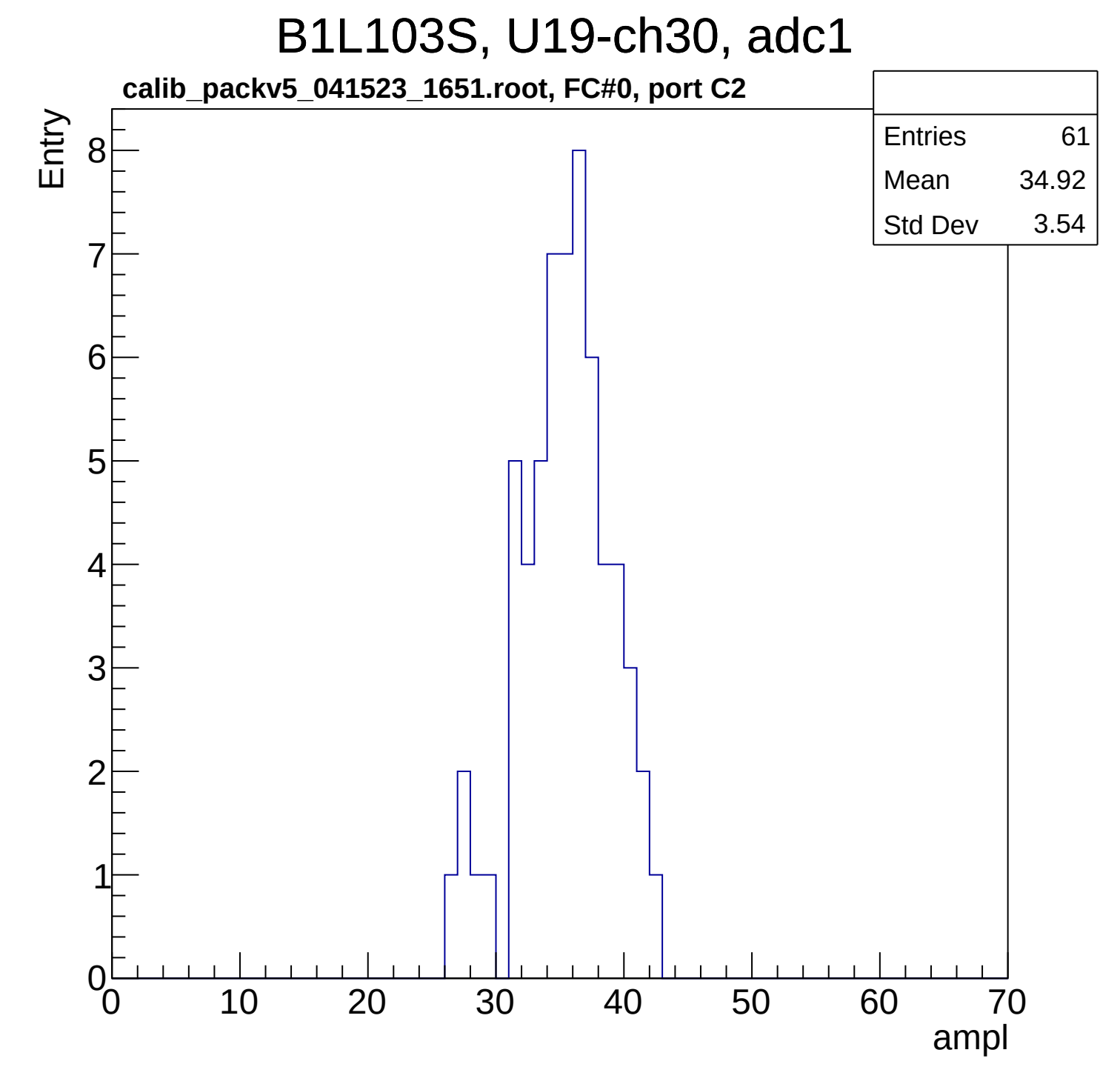
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U19-ch29, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch30, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 25.64
Std Dev 10.16
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch30, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 34.92
Std Dev 3.54
Entry
ampl
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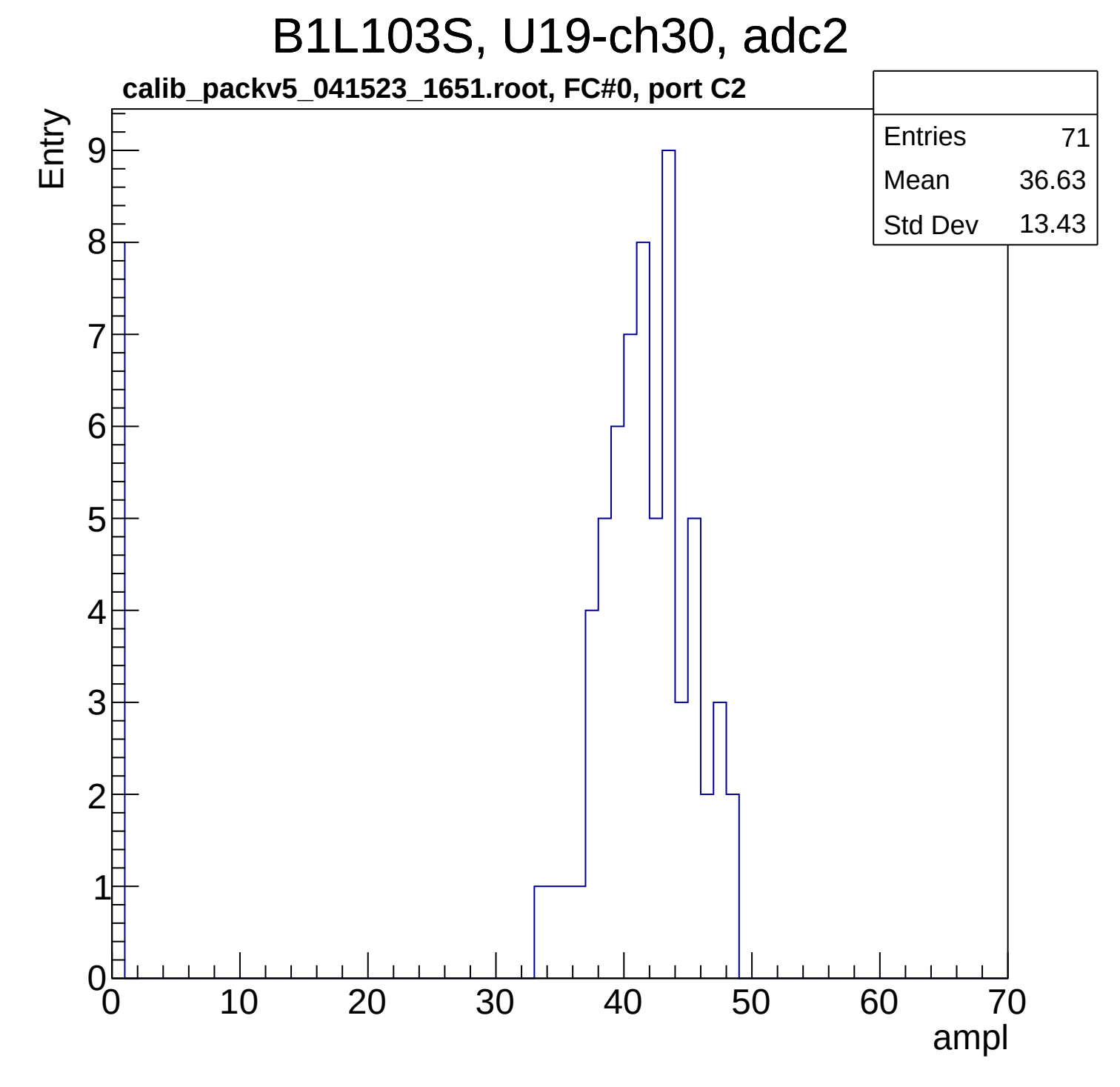
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch30, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 36.63
Std Dev 13.43
Entry
ampl
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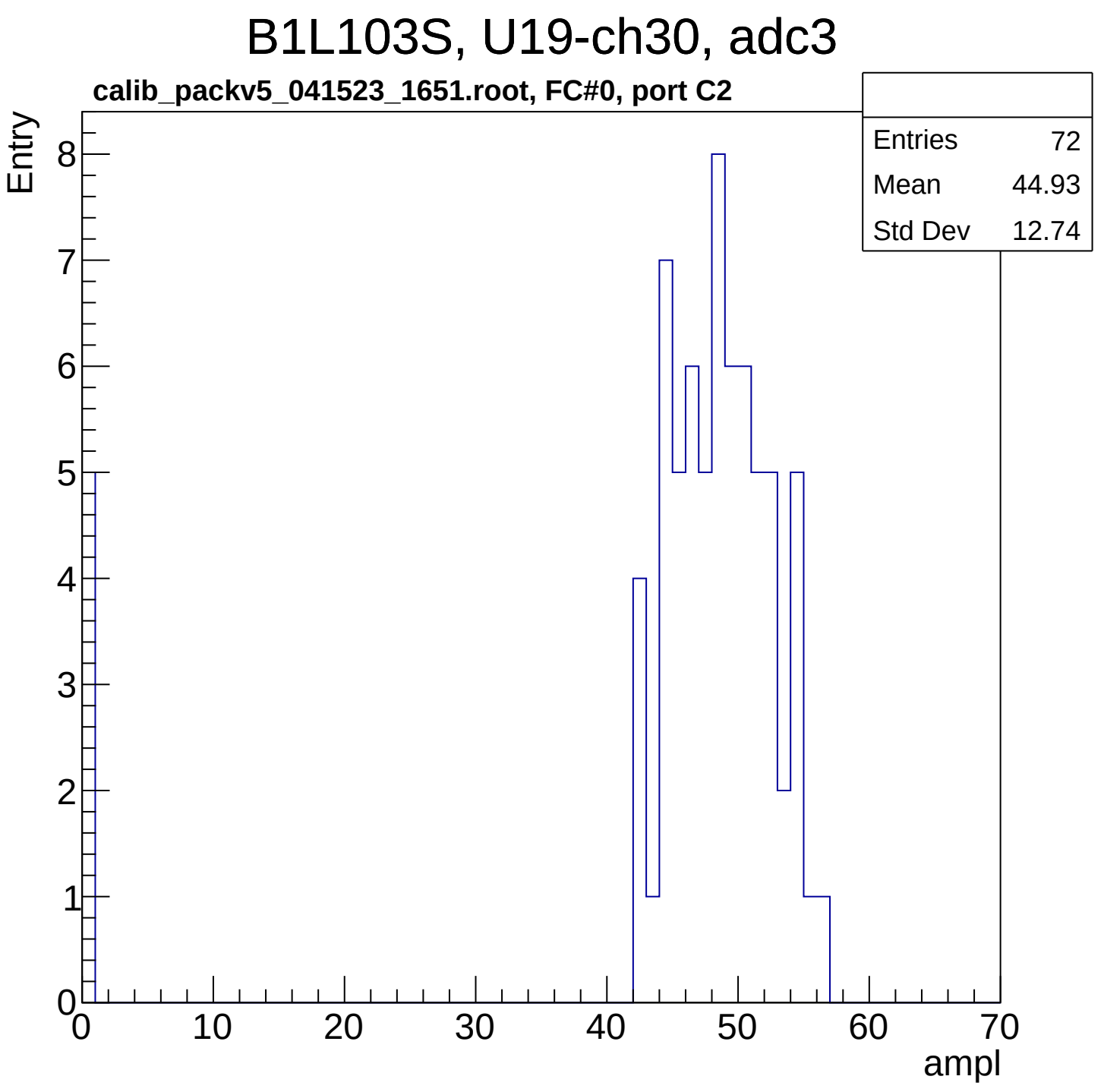
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch30, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 44.93
Std Dev 12.74
Entry
ampl
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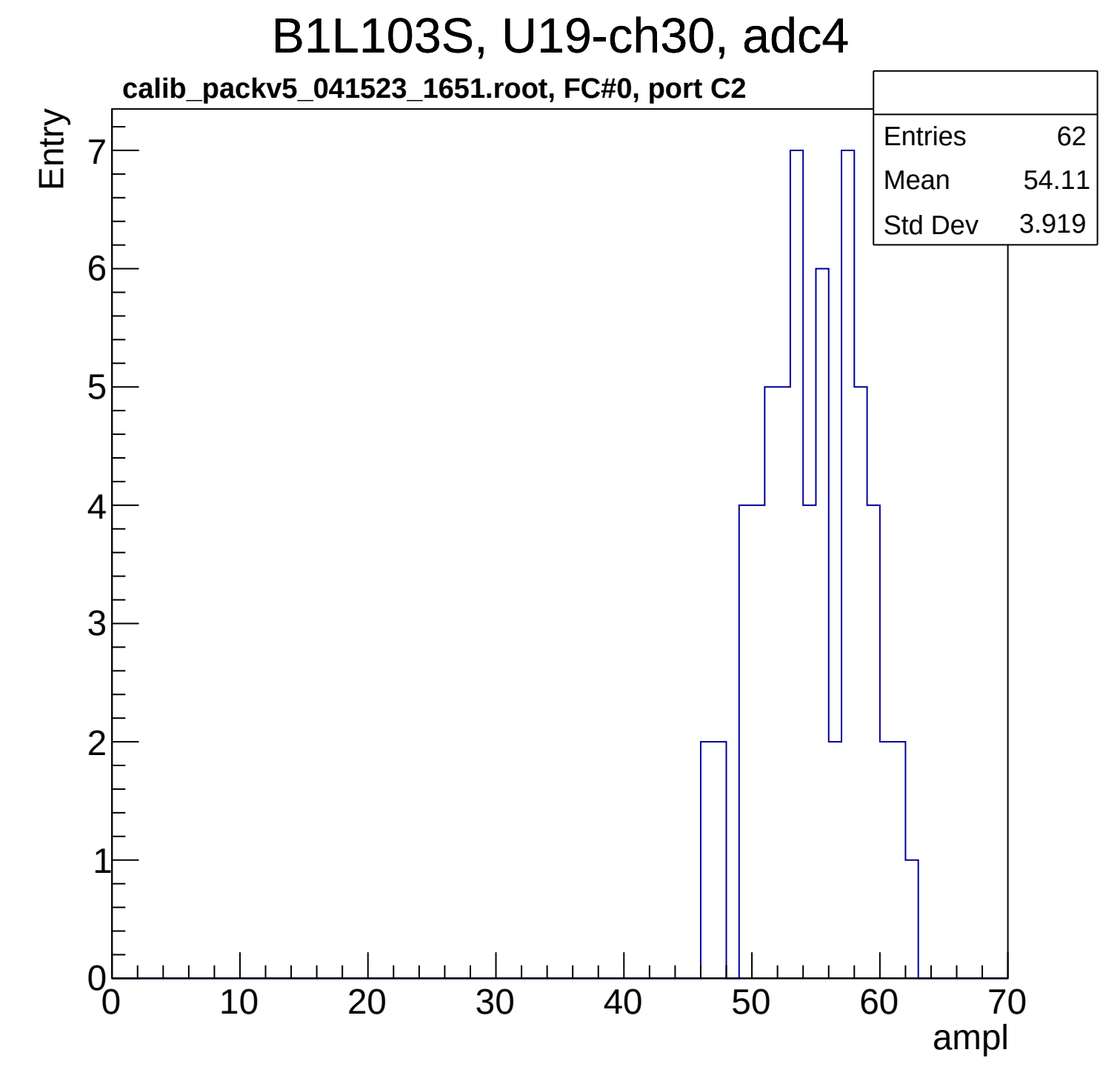
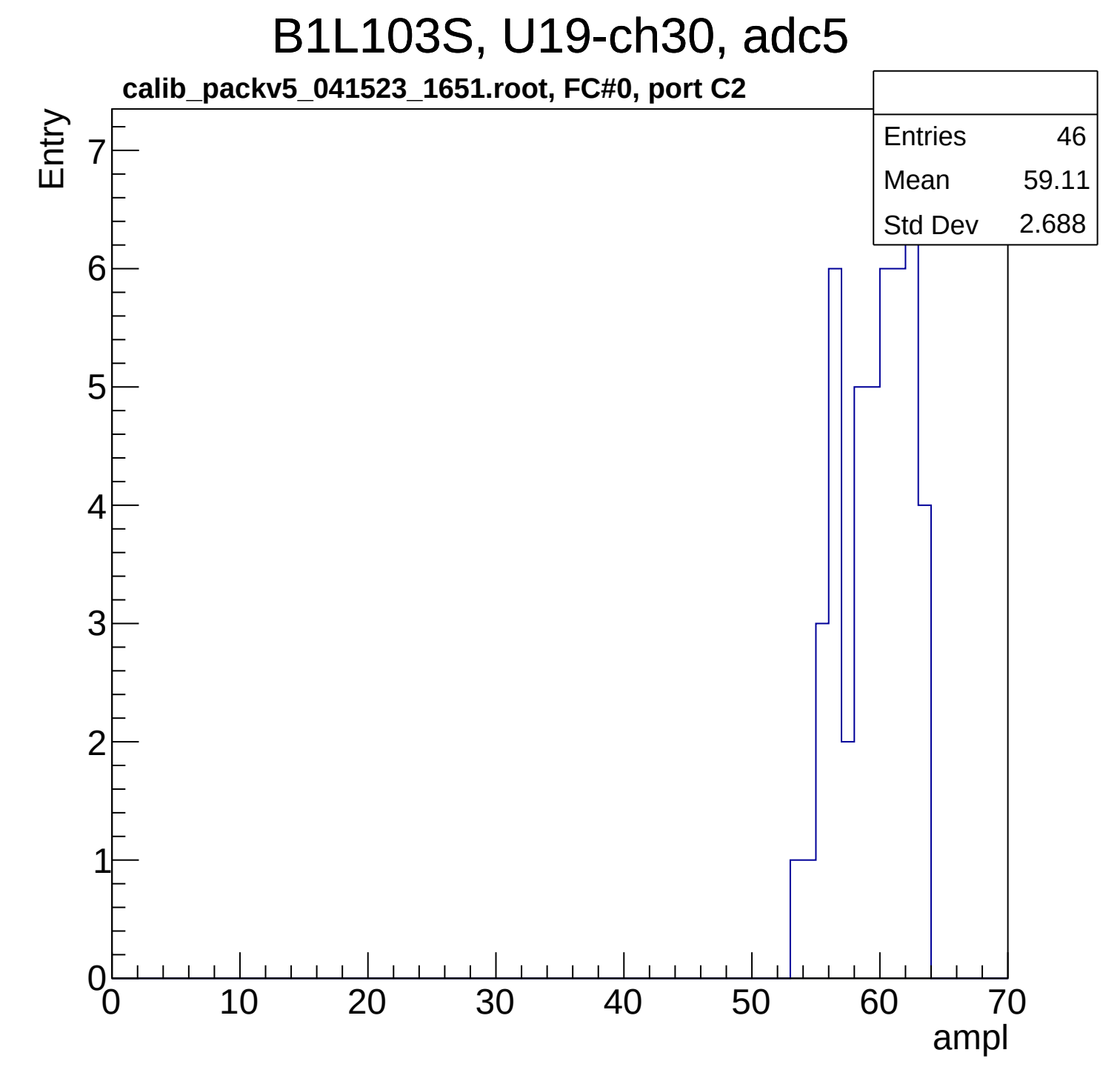
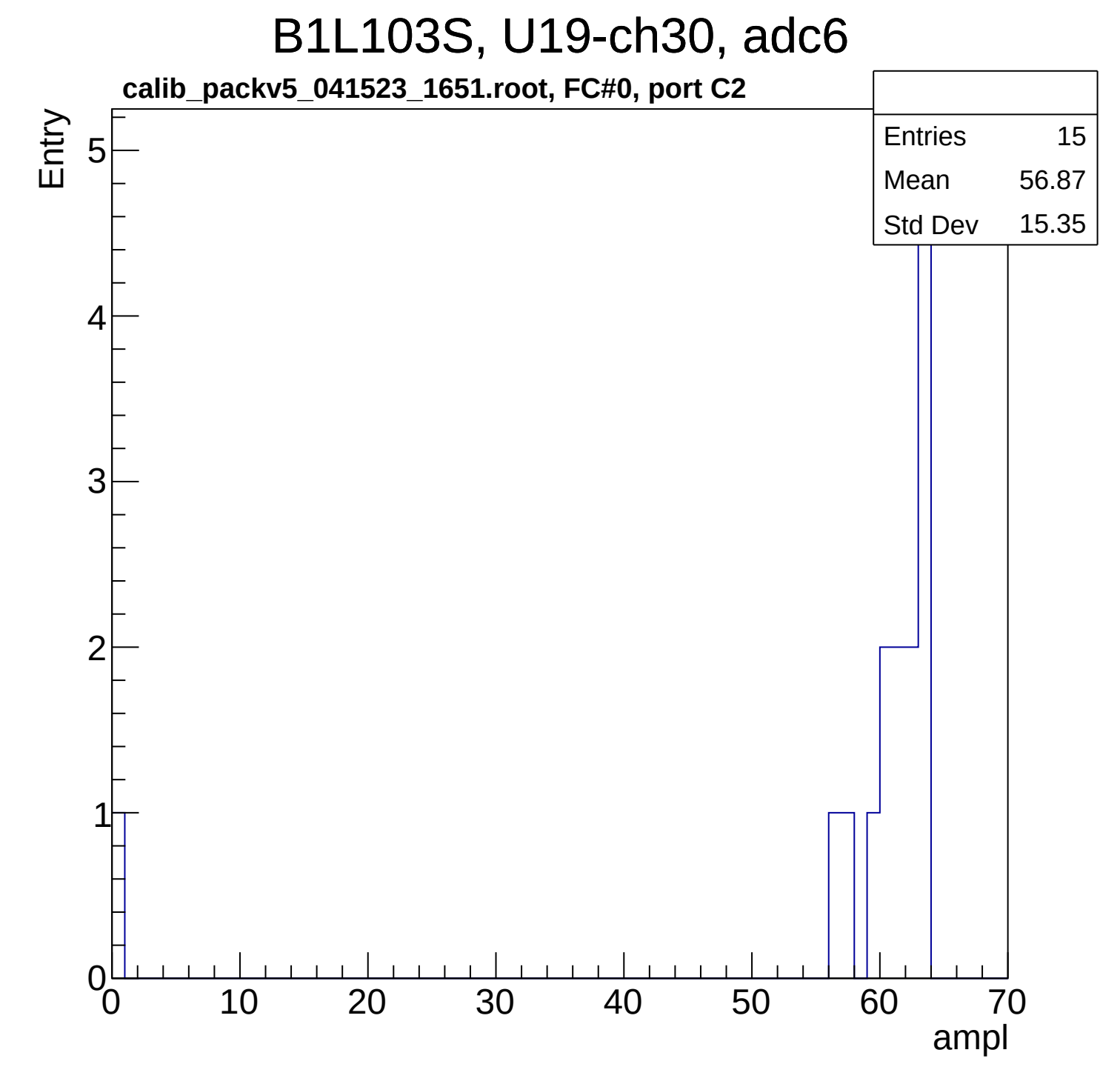
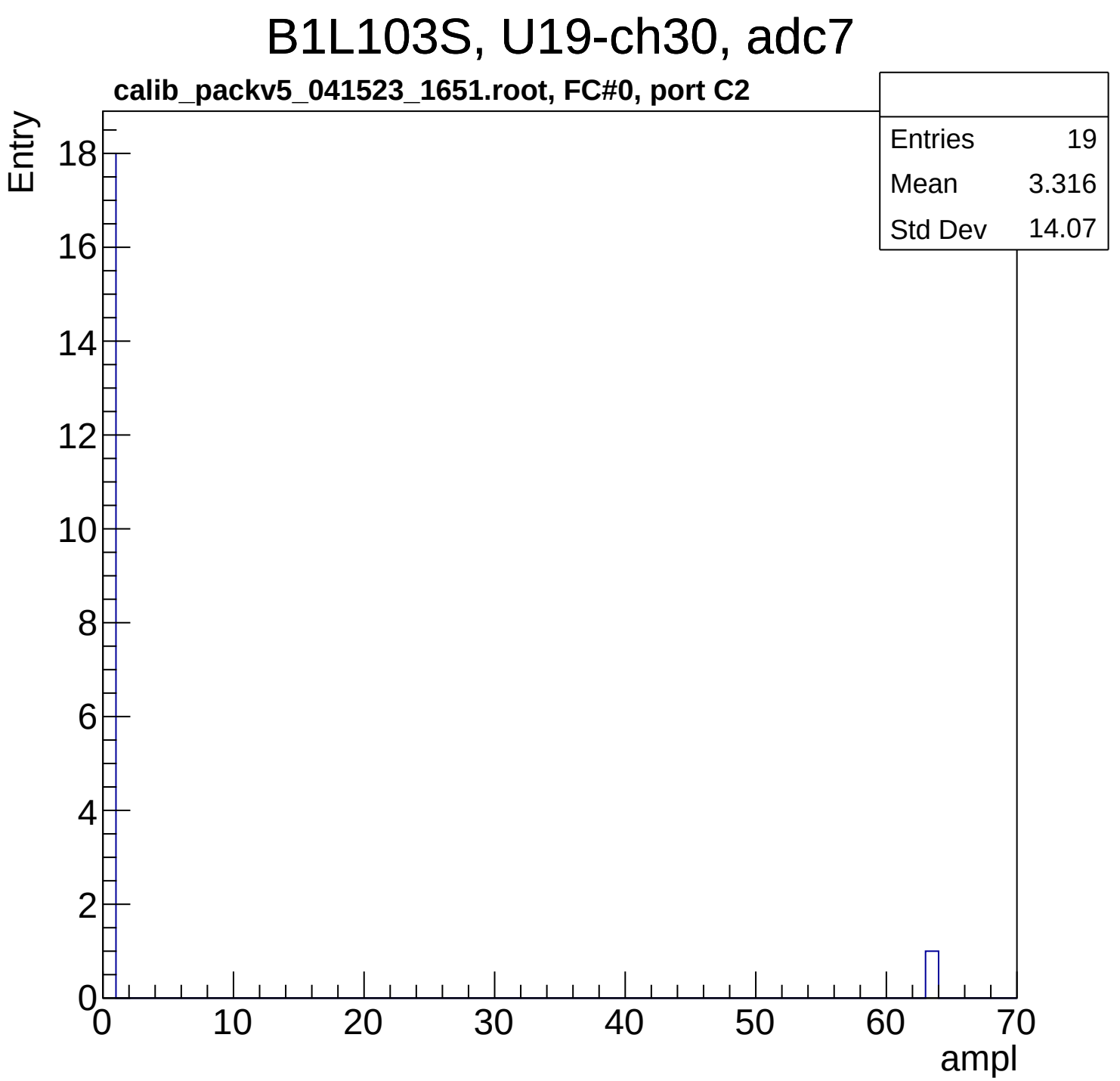
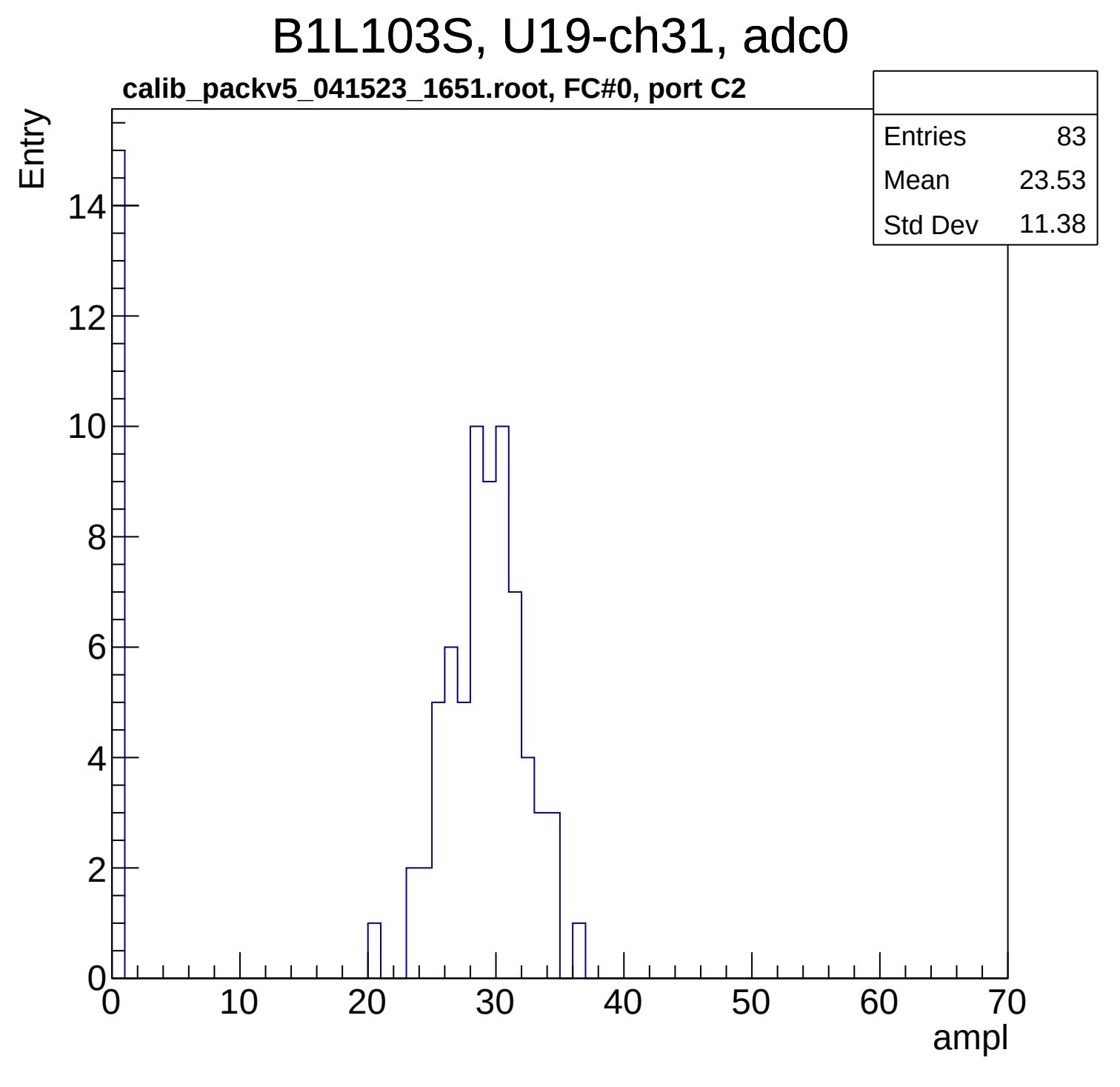
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch30, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 54.11
Std Dev 3.919
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch30, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 59.11
Std Dev 2.688
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch30, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 56.87
Std Dev 15.35
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U19-ch30, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.316
Std Dev 14.07
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch31, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 23.53
Std Dev 11.38
Entry
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2
4
6
8
10
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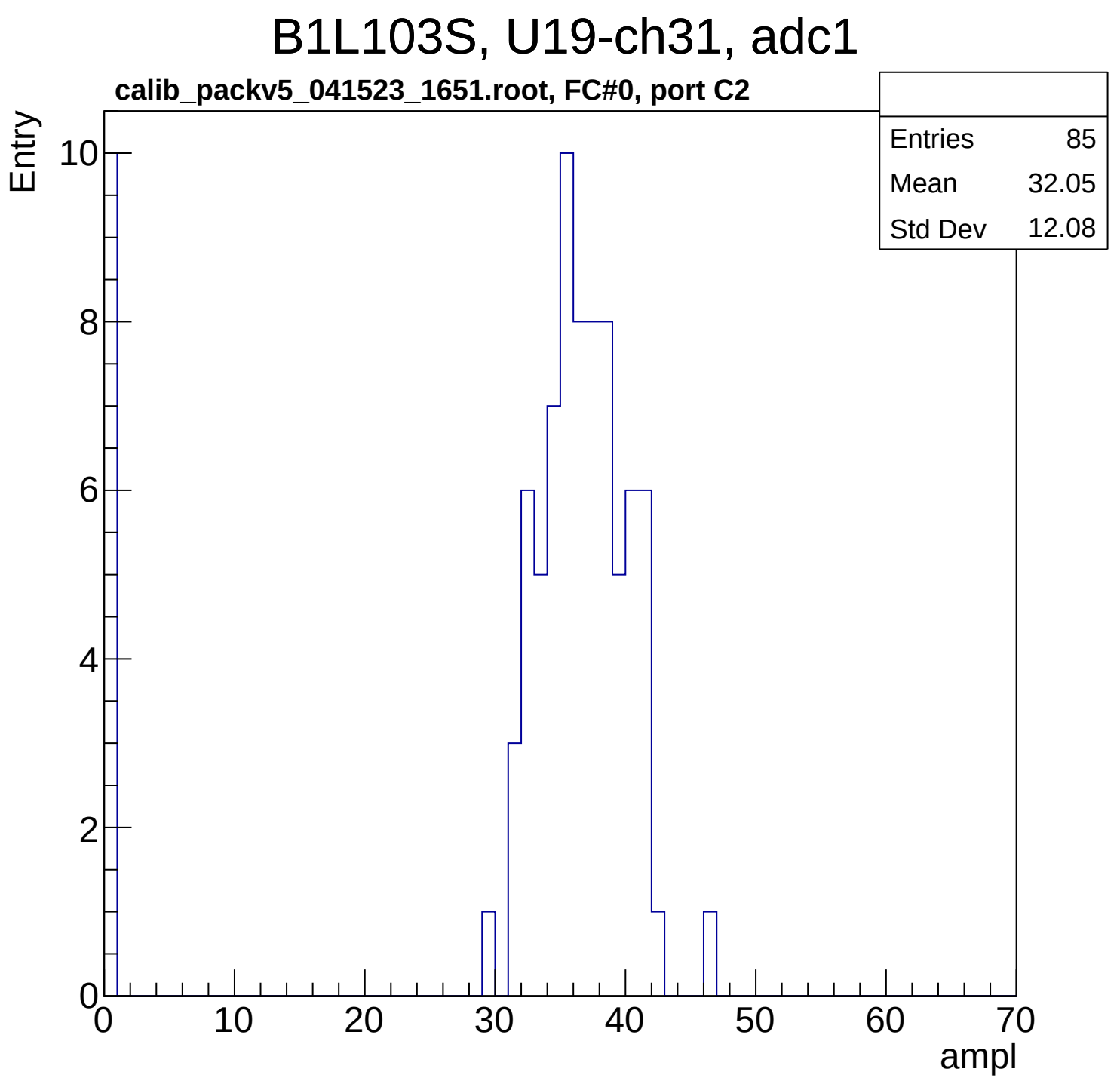
ampl


B1L103S, U19-ch31, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 32.05
Std Dev 12.08
Entry
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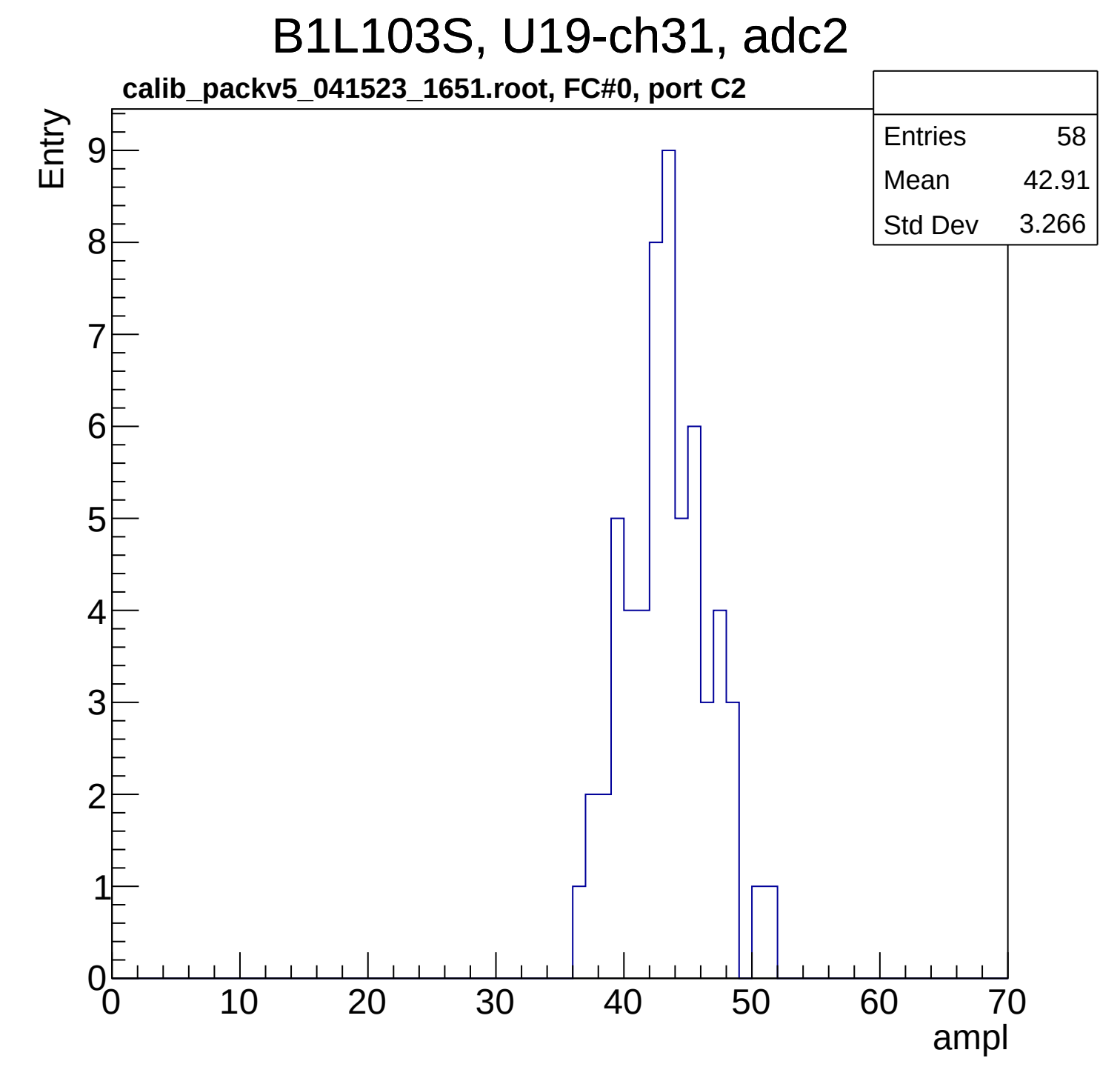
ampl


B1L103S, U19-ch31, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 42.91
Std Dev 3.266
Entry
ampl
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4
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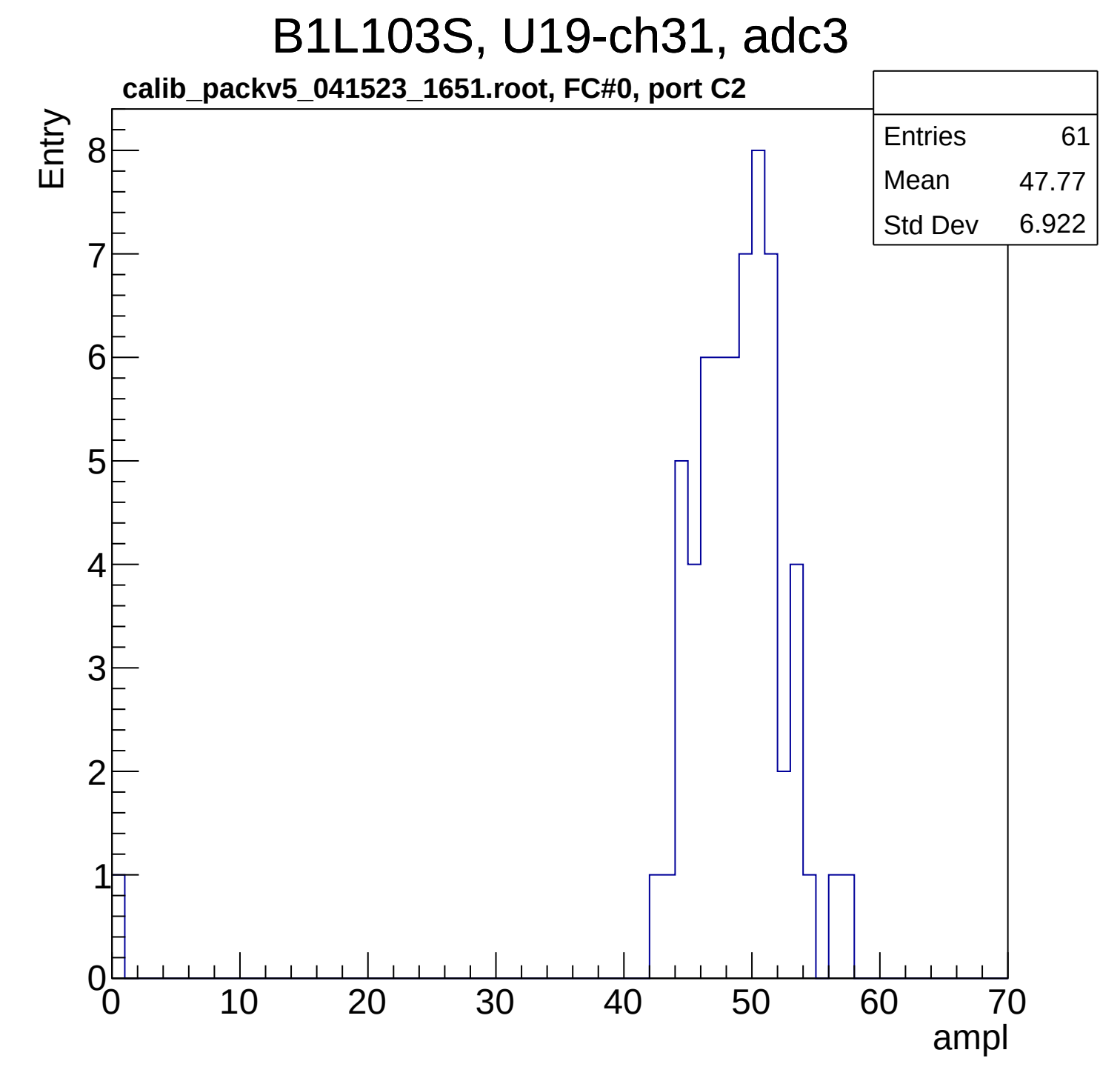
B1L103S, U19-ch31, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 47.77
Std Dev 6.922
Entry
ampl
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2
3
4
5
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7
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0
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40
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60
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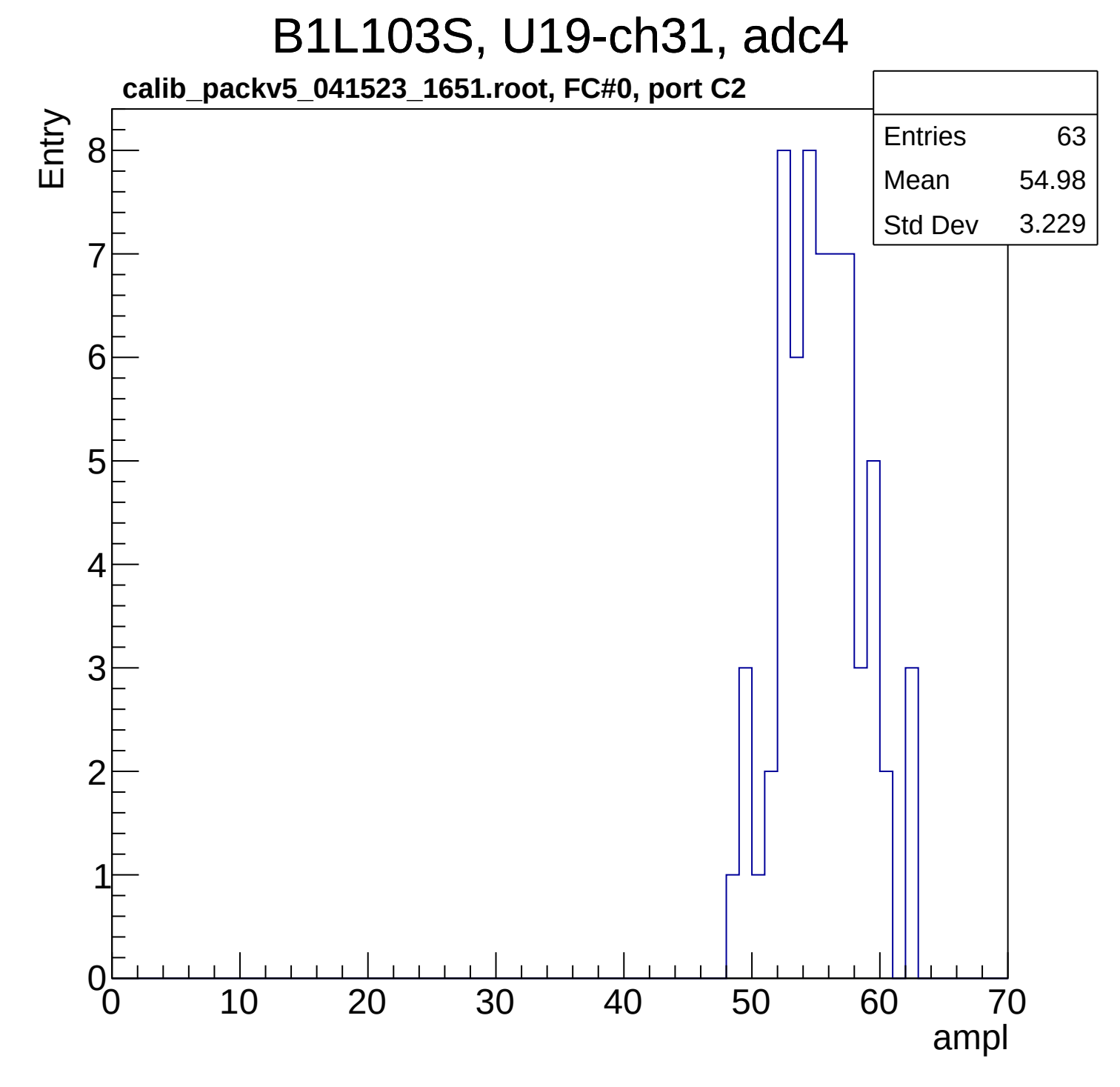
B1L103S, U19-ch31, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 54.98
Std Dev 3.229
Entry
ampl
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3
4
5
6
7
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0
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40
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60
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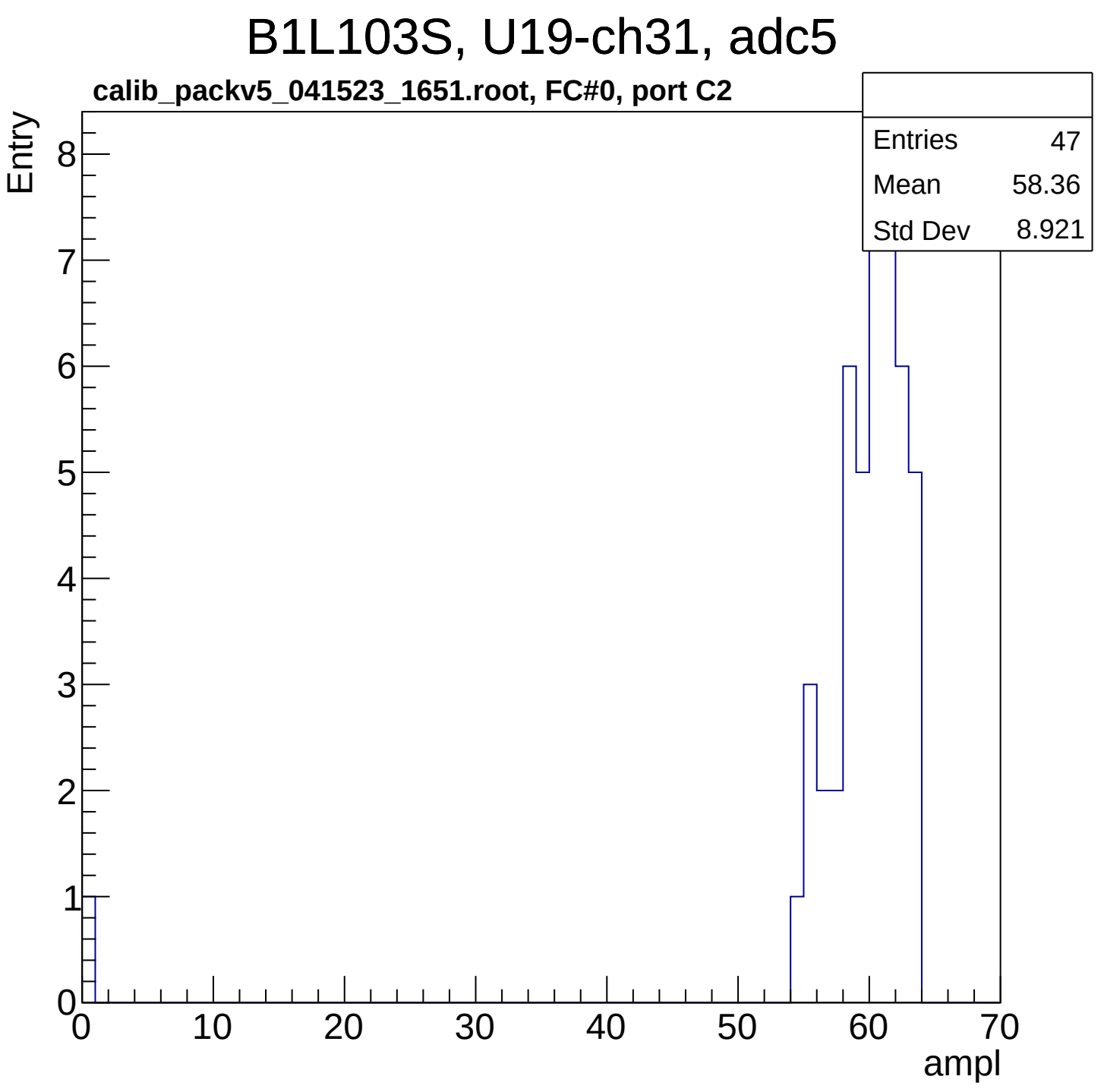
B1L103S, U19-ch31, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 58.36
Std Dev 8.921
Entry
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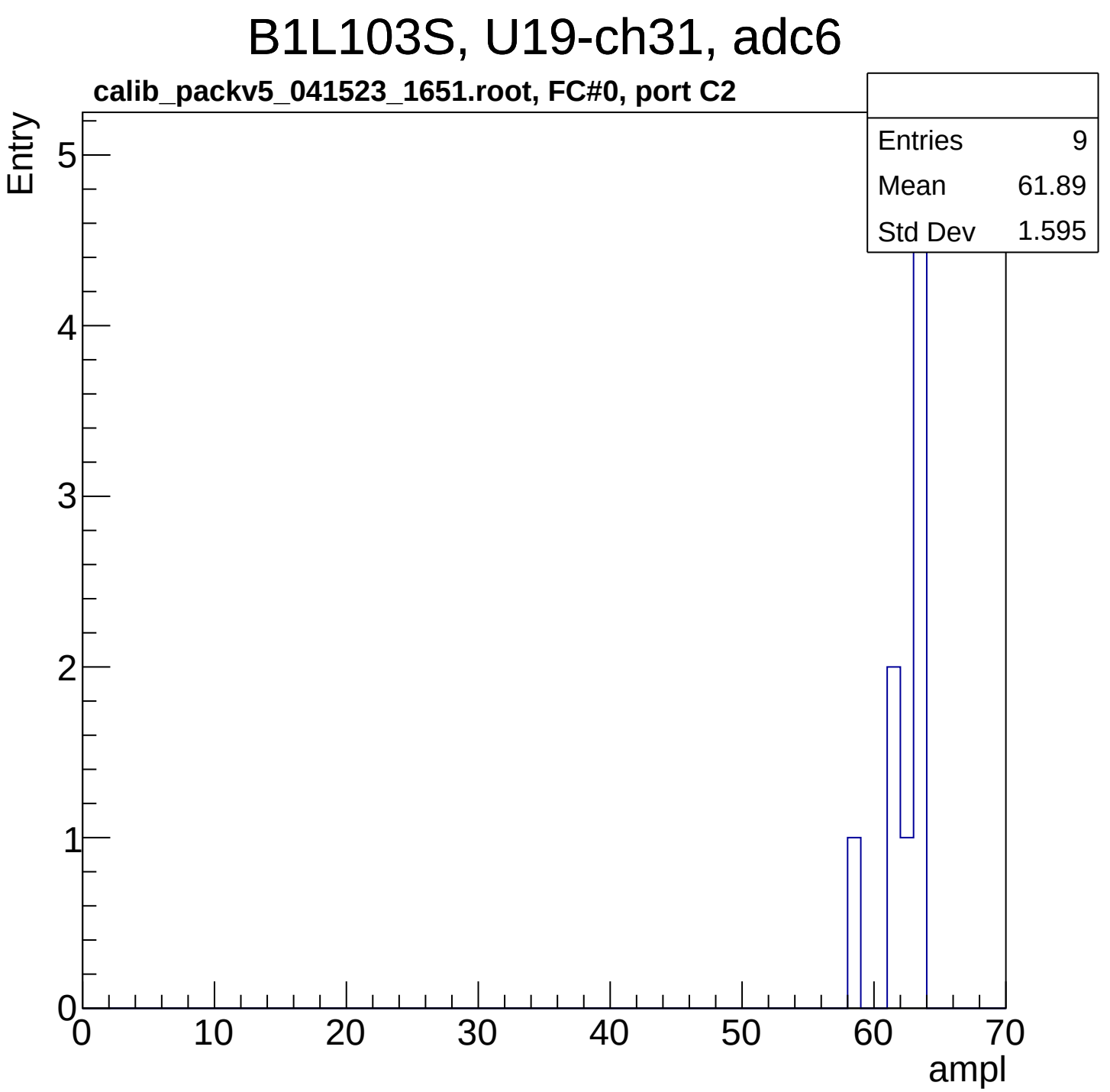
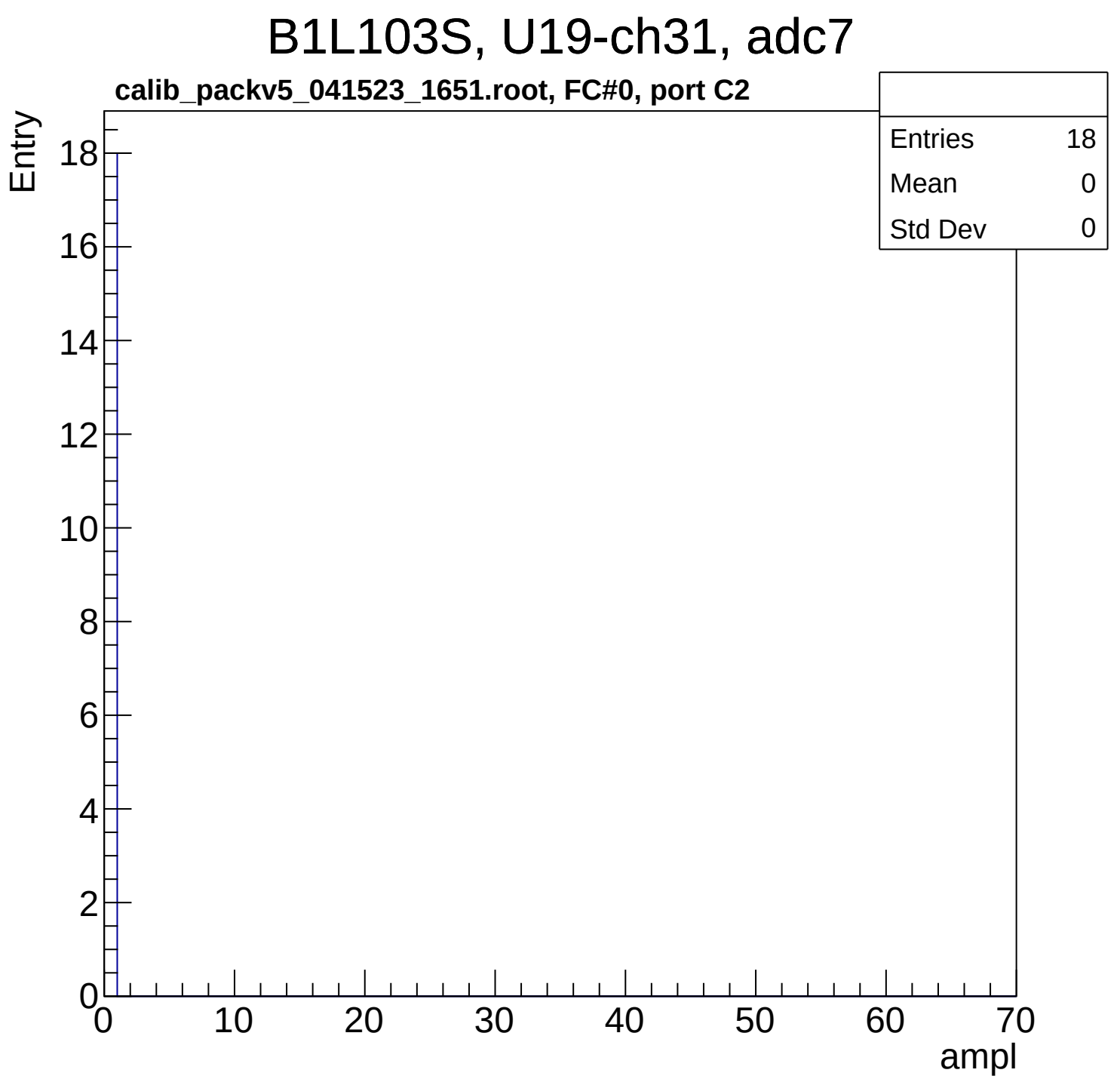
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch31, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 61.89
Std Dev 1.595
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch31, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
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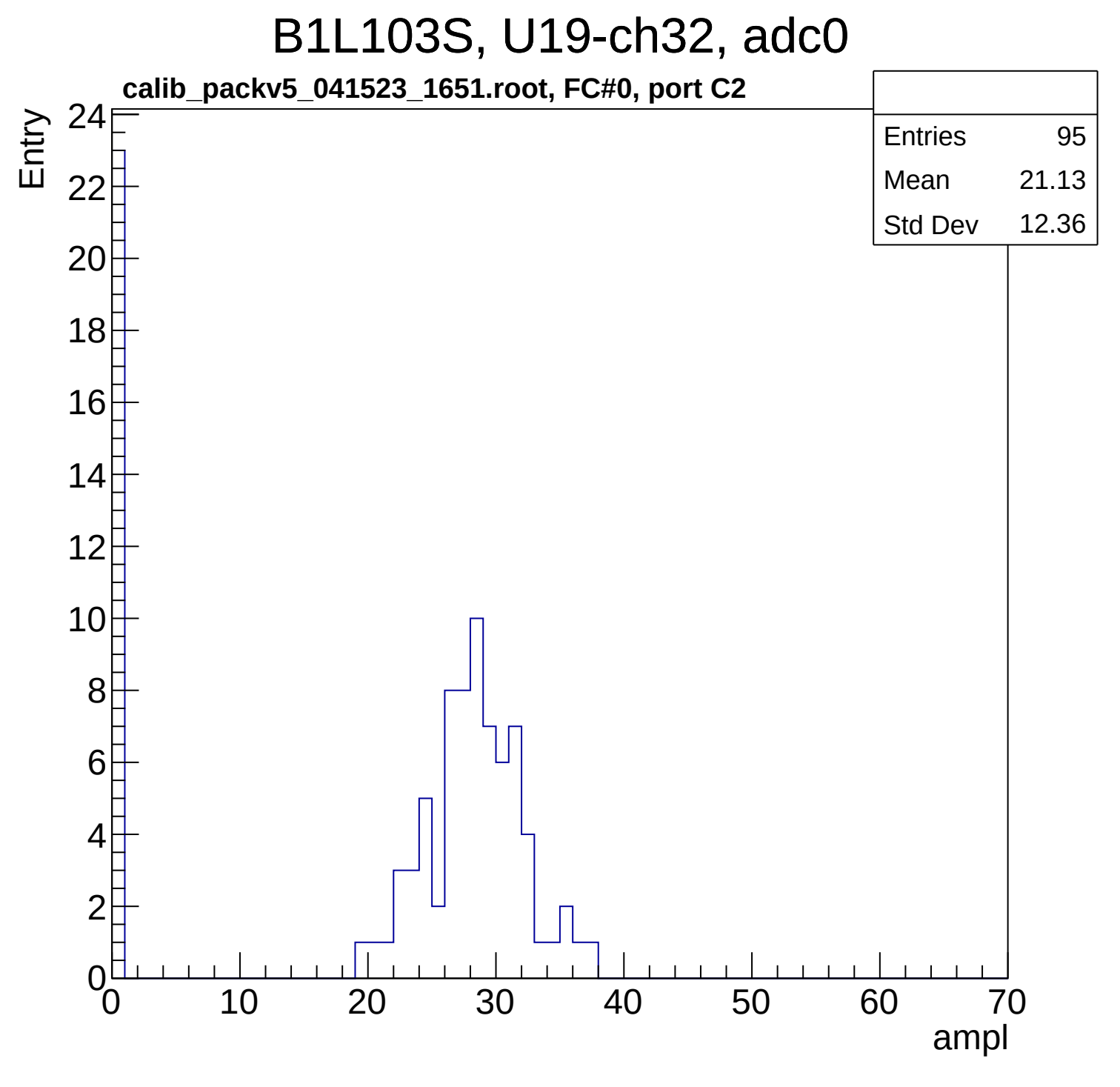
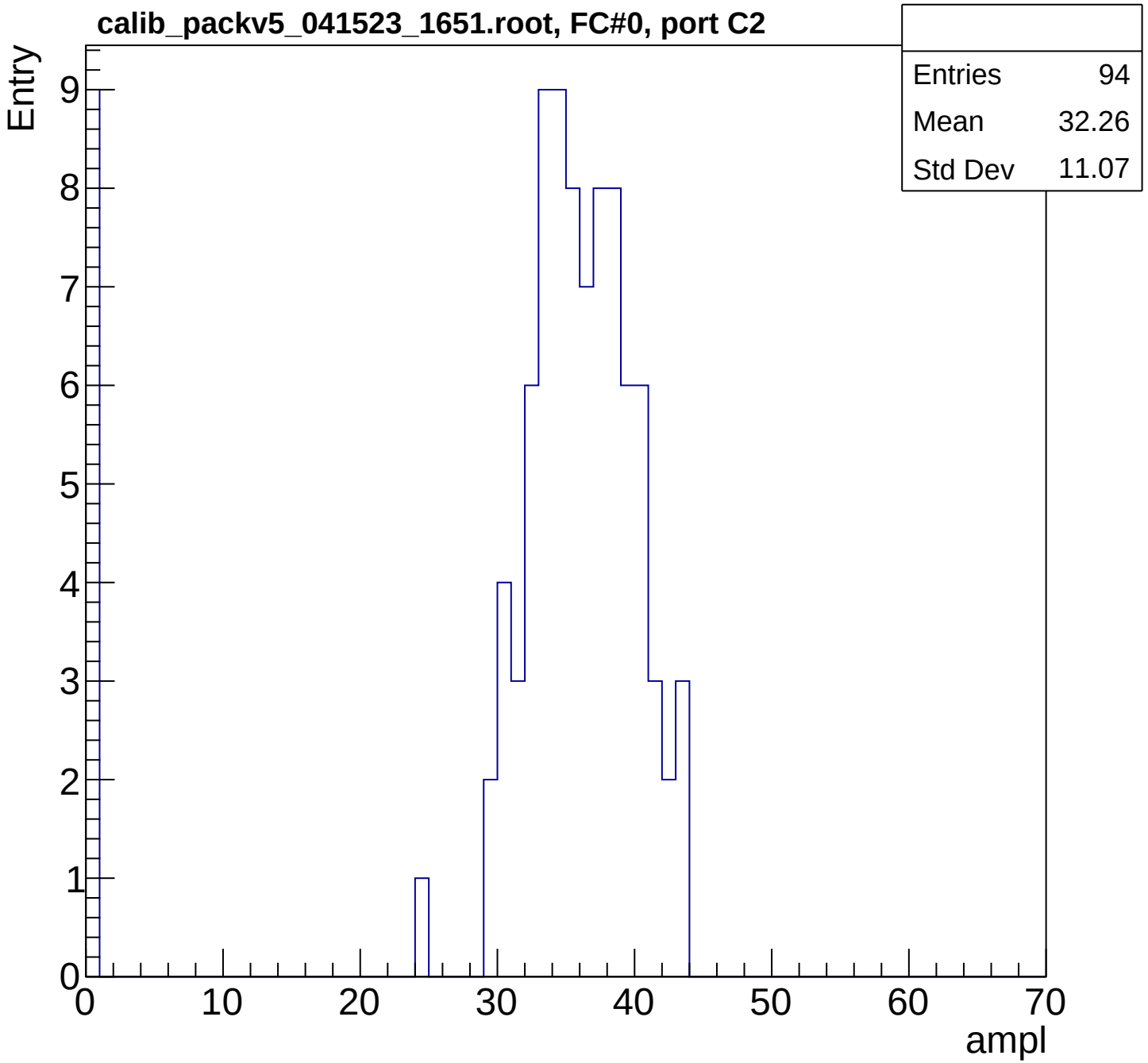
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch32, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 21.13
Std Dev 12.36
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
24
0
10
20
30
40
50
60
70


B1L103S, U19-ch32, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 32.26
Std Dev 11.07
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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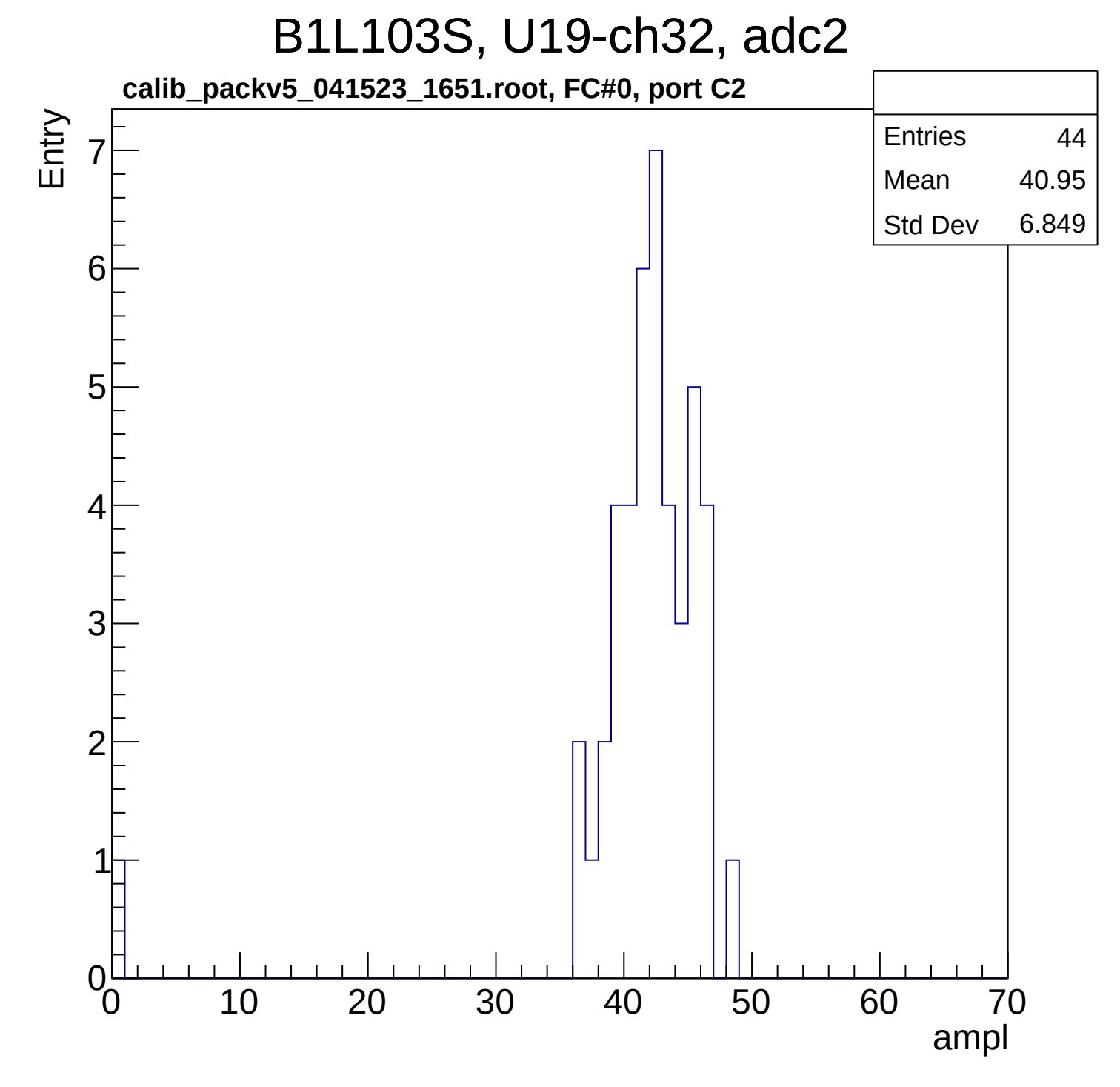
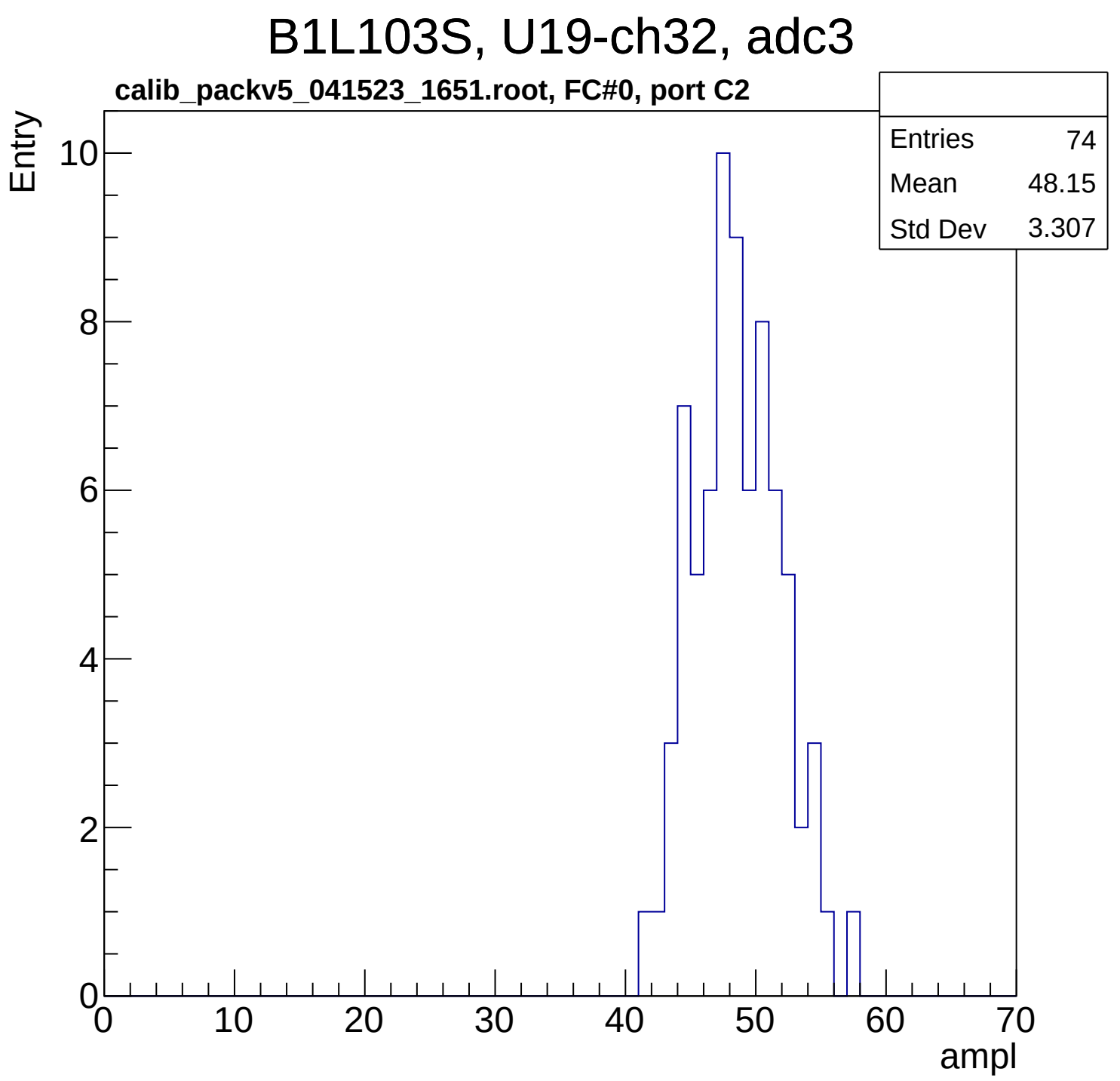
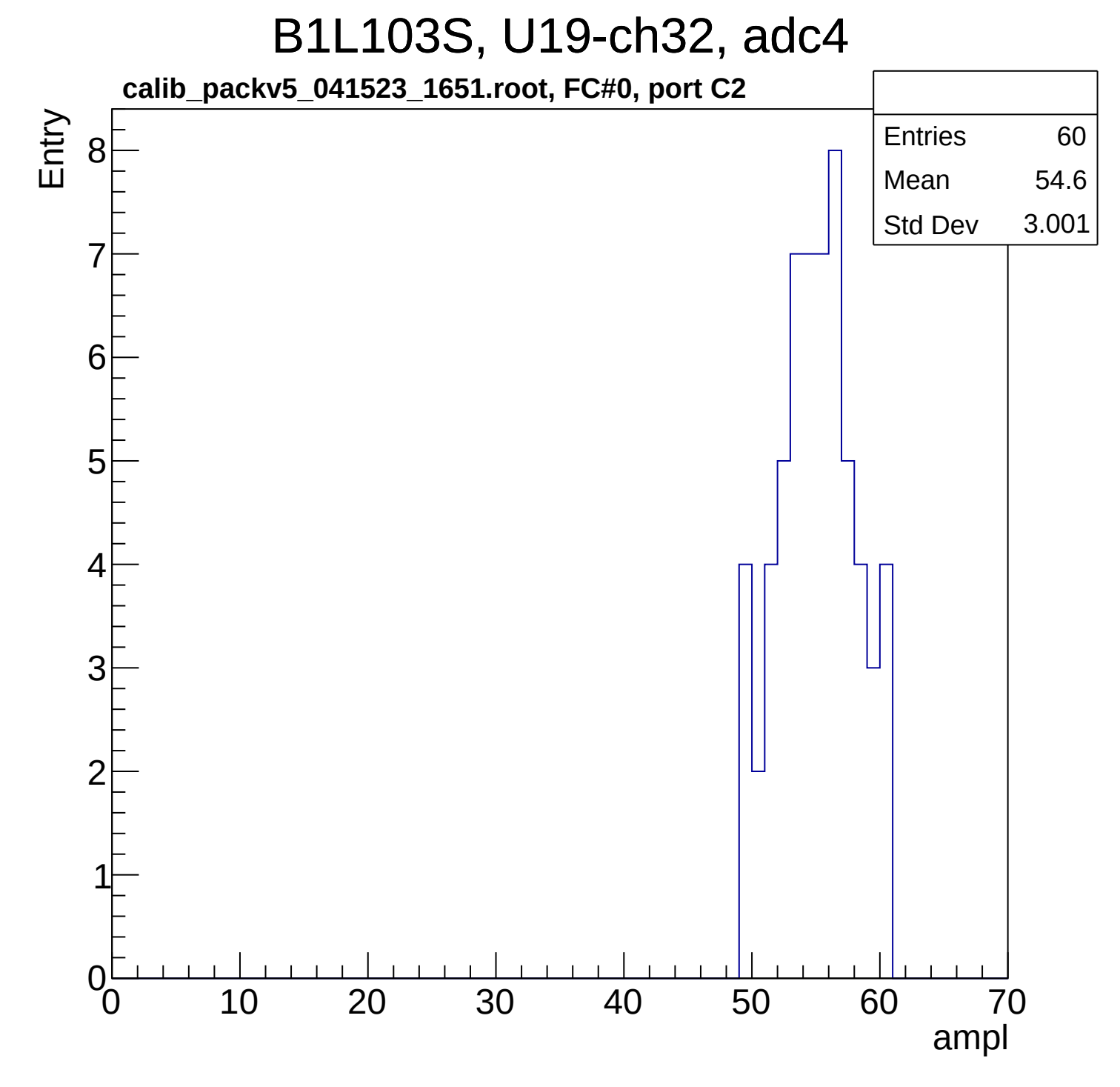
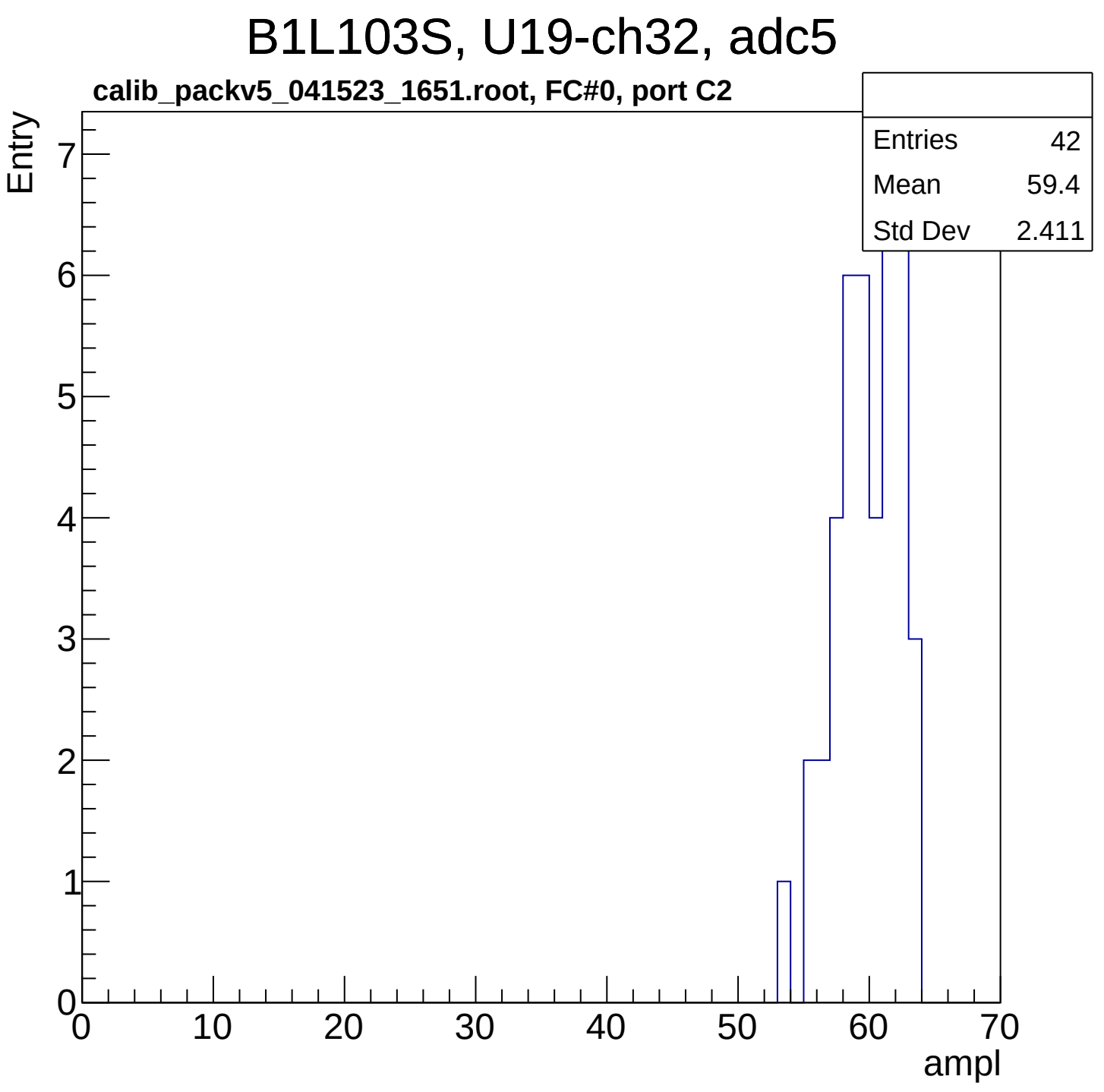

B1L103S, U19-ch32, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 40.95
Std Dev 6.849
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch32, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 48.15
Std Dev 3.307
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U19-ch32, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 54.6
Std Dev 3.001
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch32, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 59.4
Std Dev 2.411
Entry
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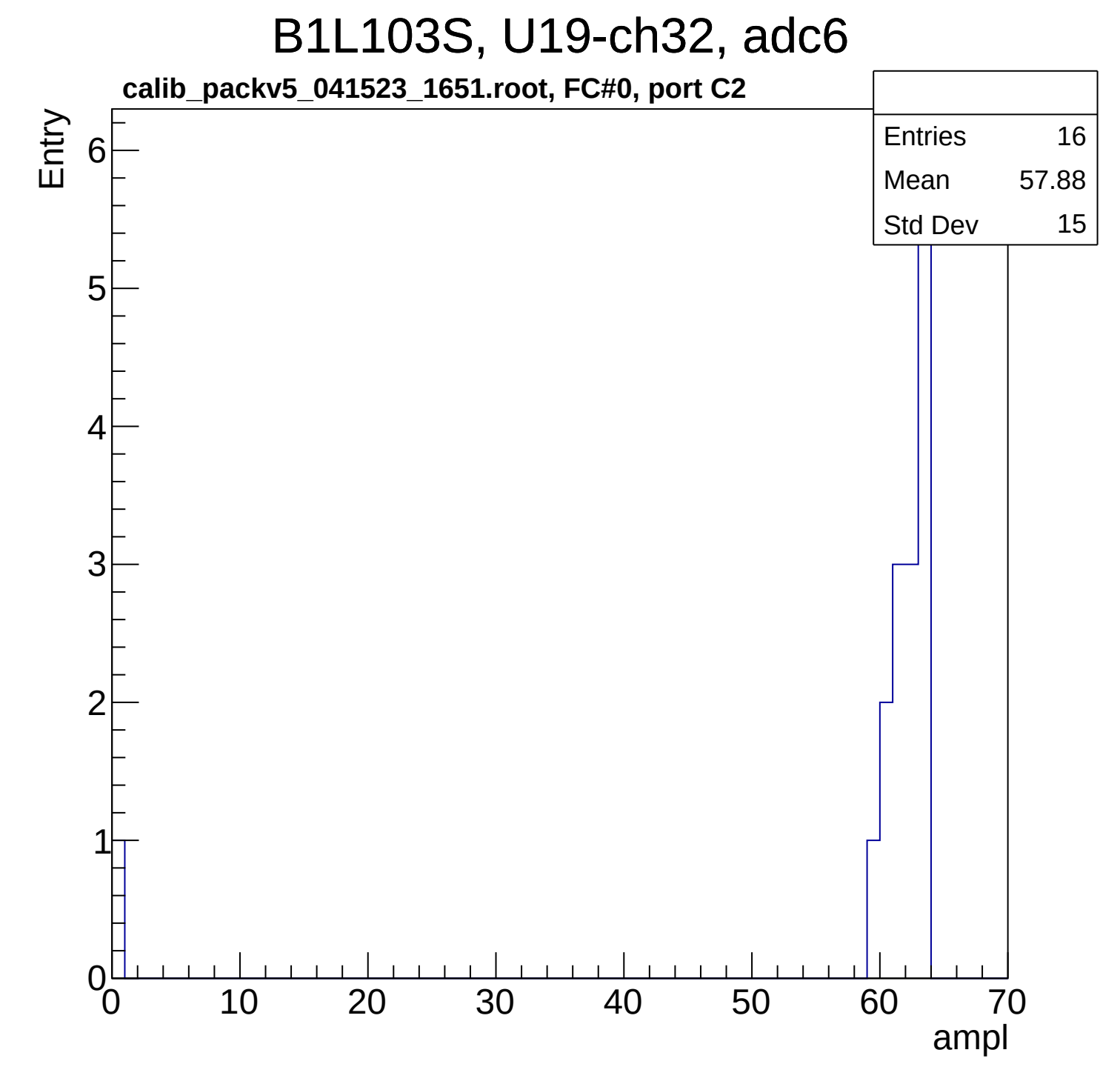
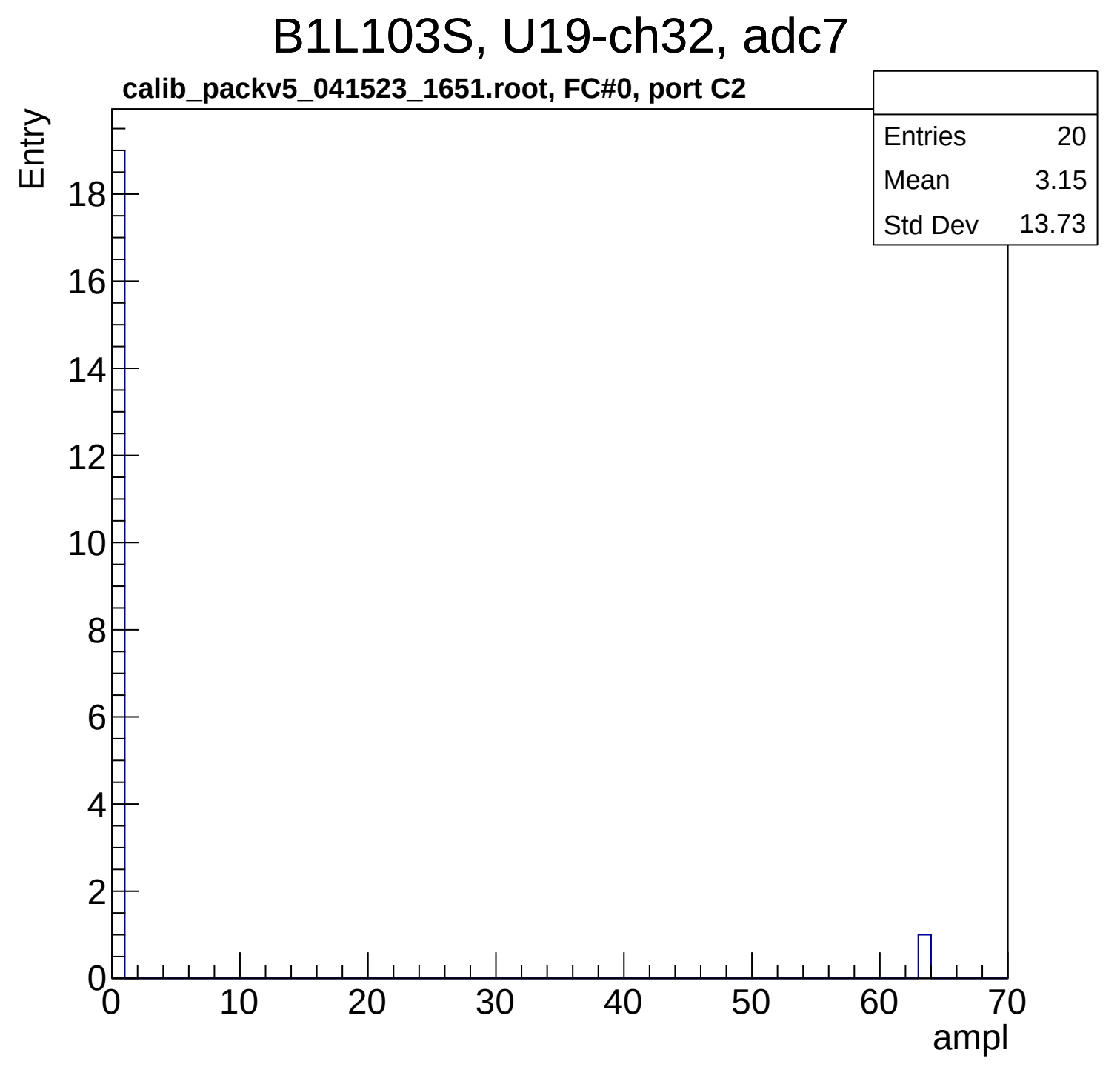
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch32, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 57.88
Std Dev 15
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U19-ch32, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
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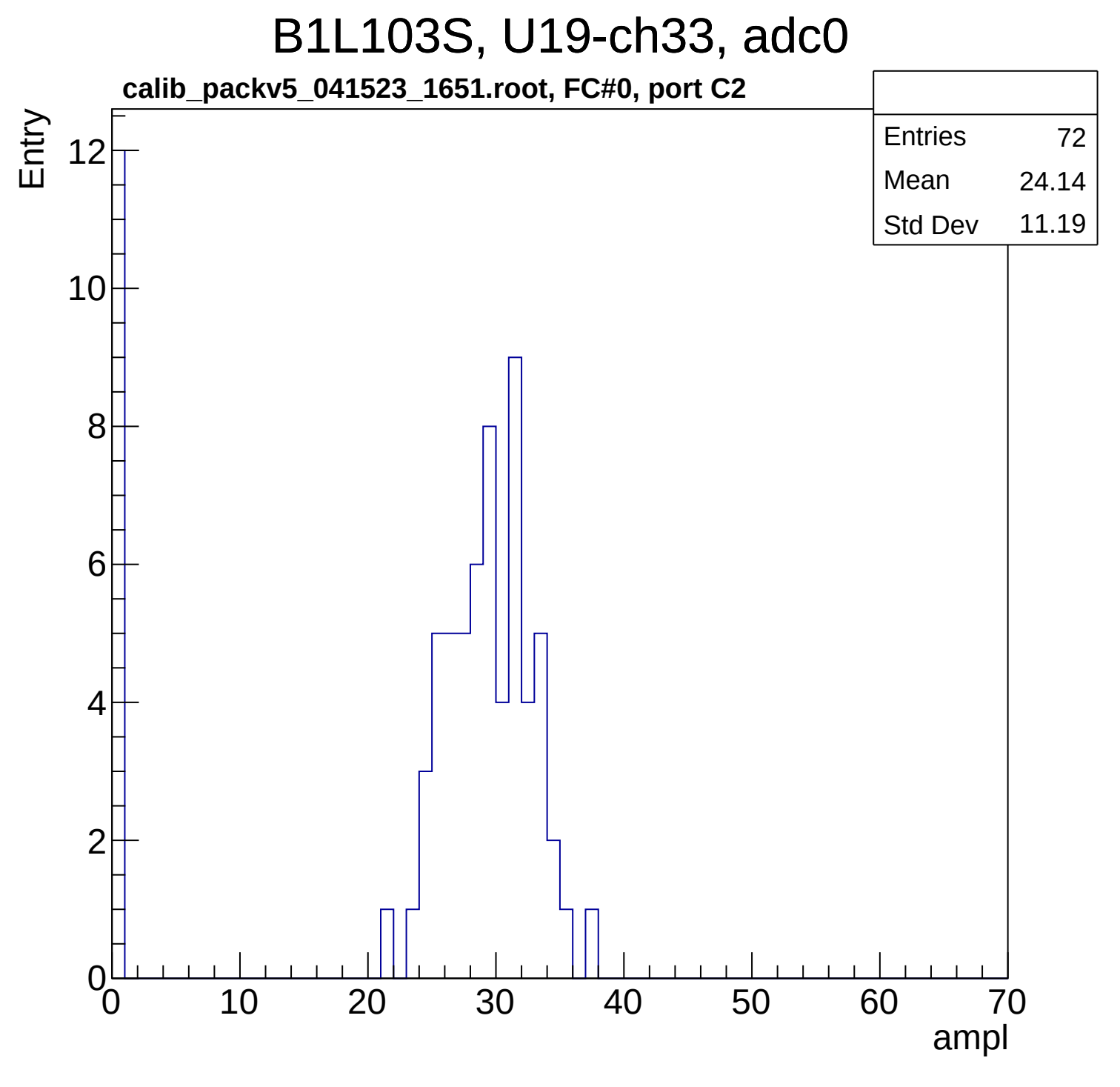
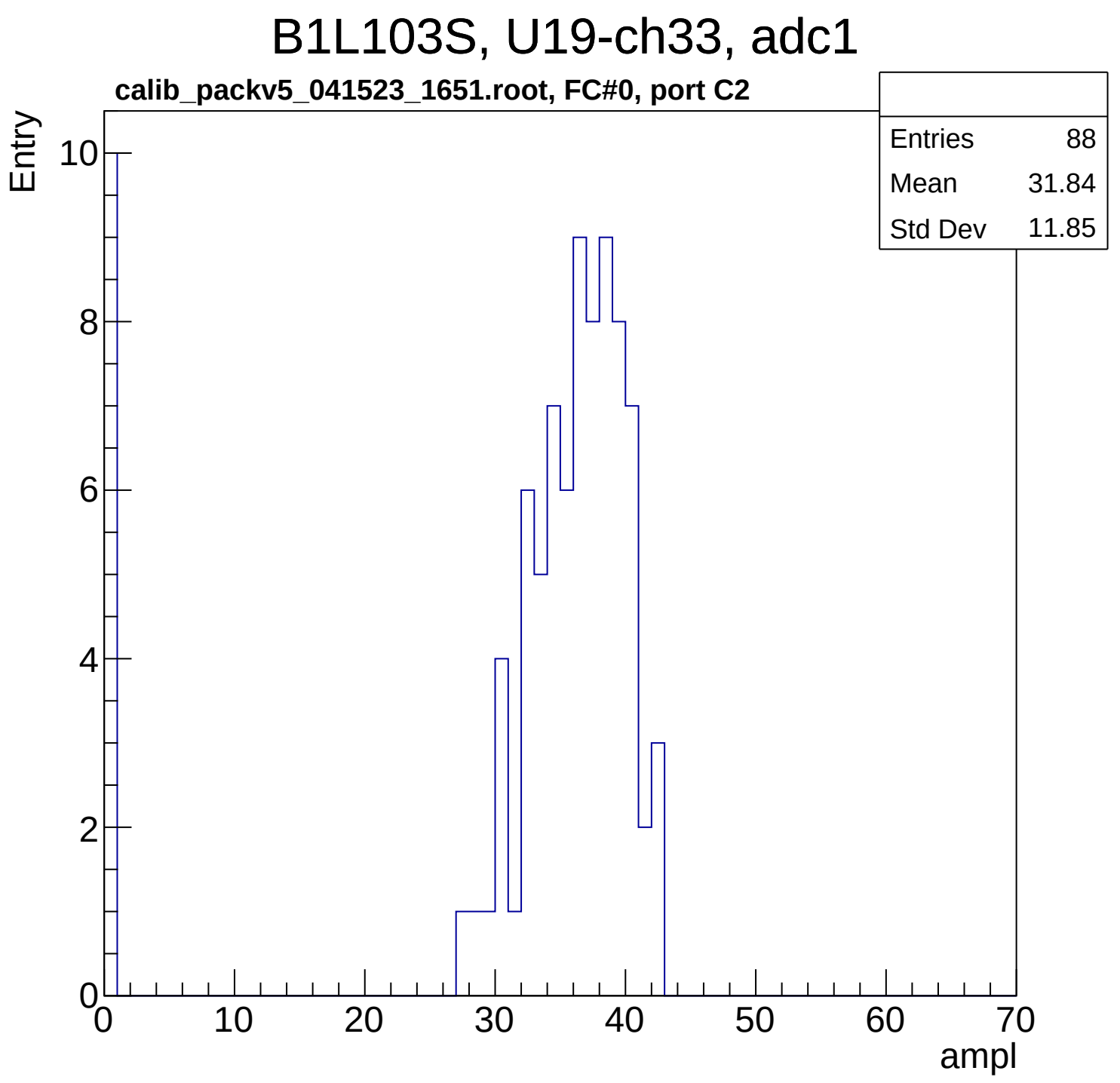
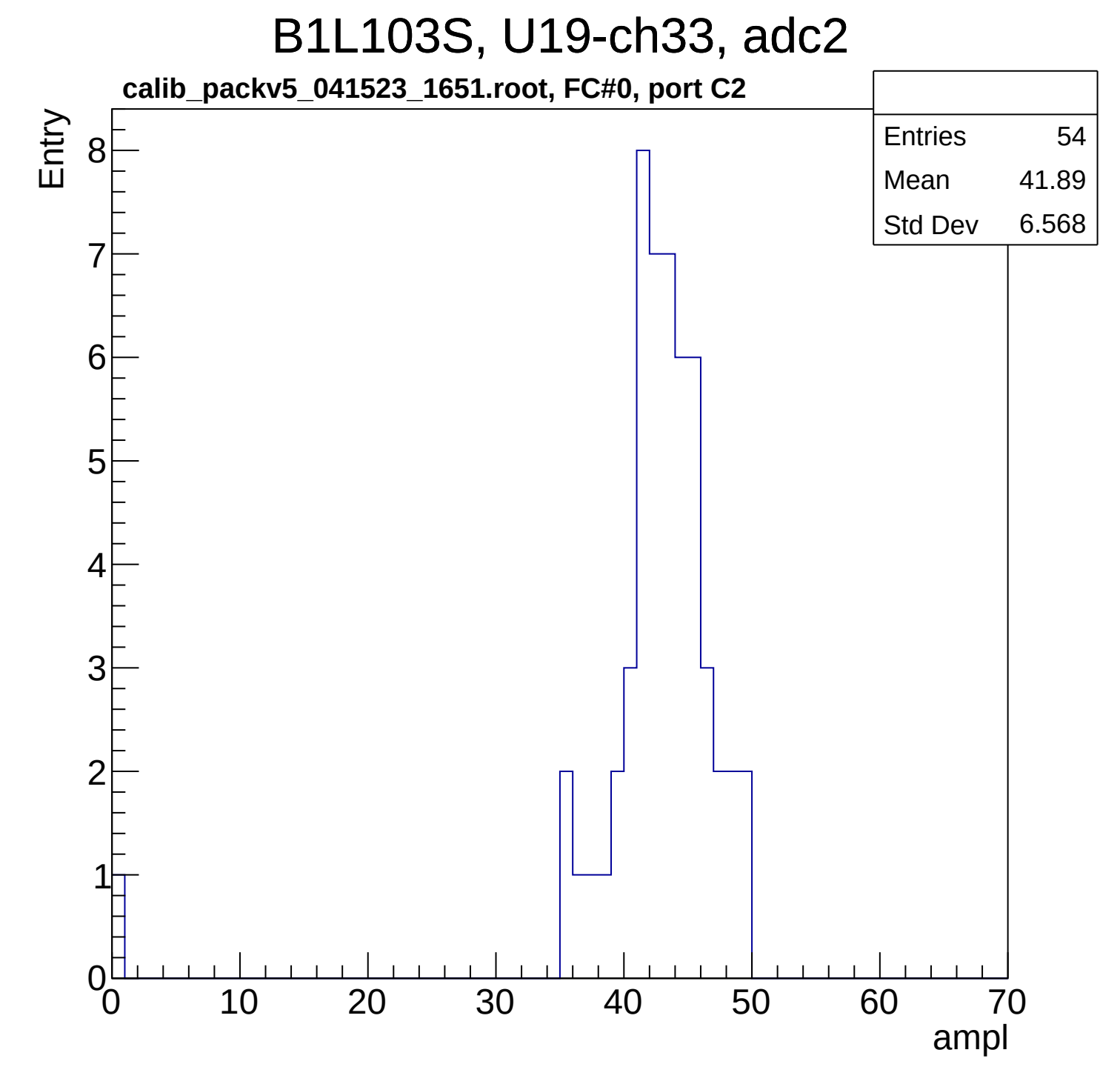
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch33, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 24.14
Std Dev 11.19
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch33, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 31.84
Std Dev 11.85
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch33, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 41.89
Std Dev 6.568
Entry
ampl
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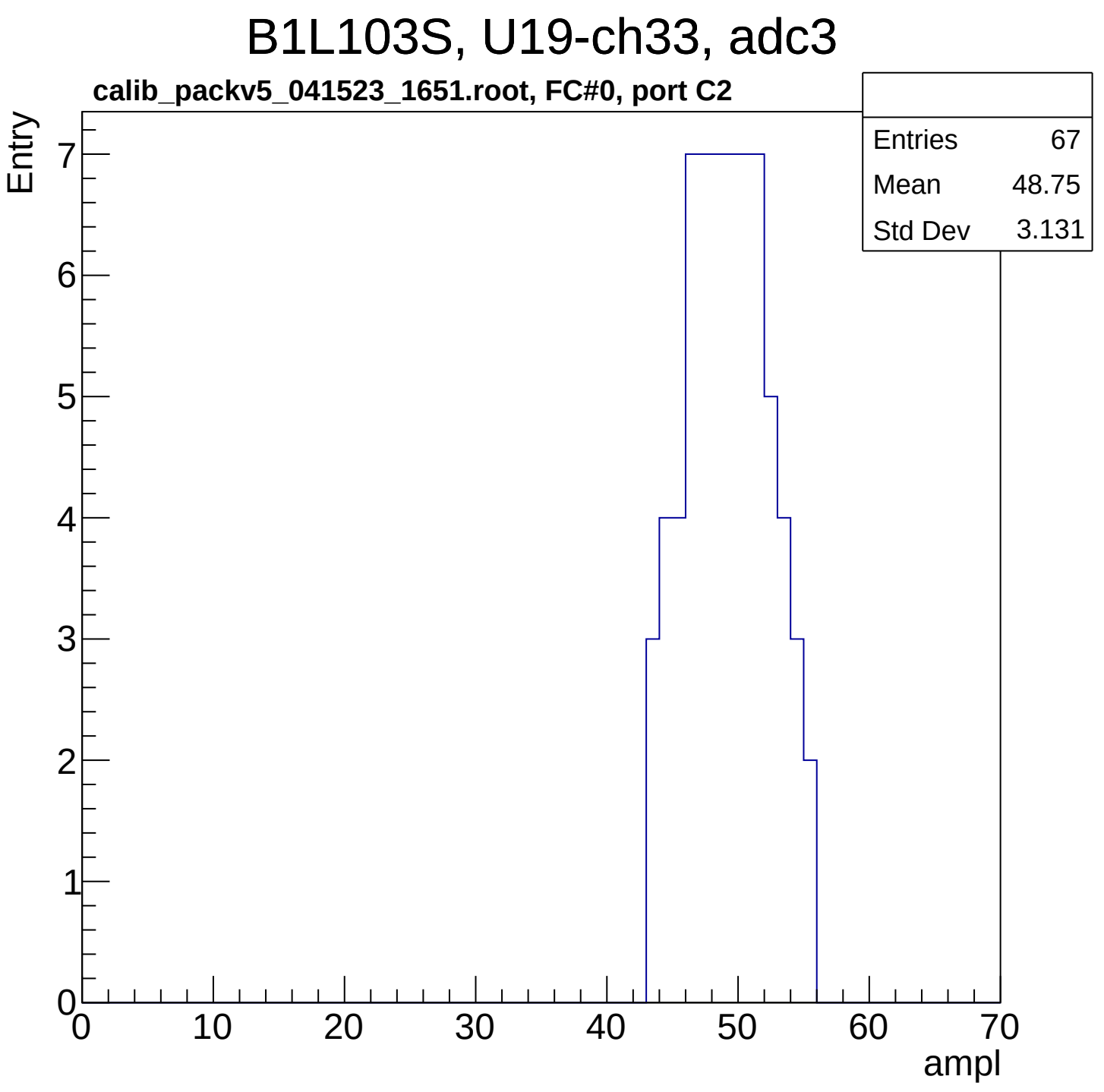
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch33, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 48.75
Std Dev 3.131
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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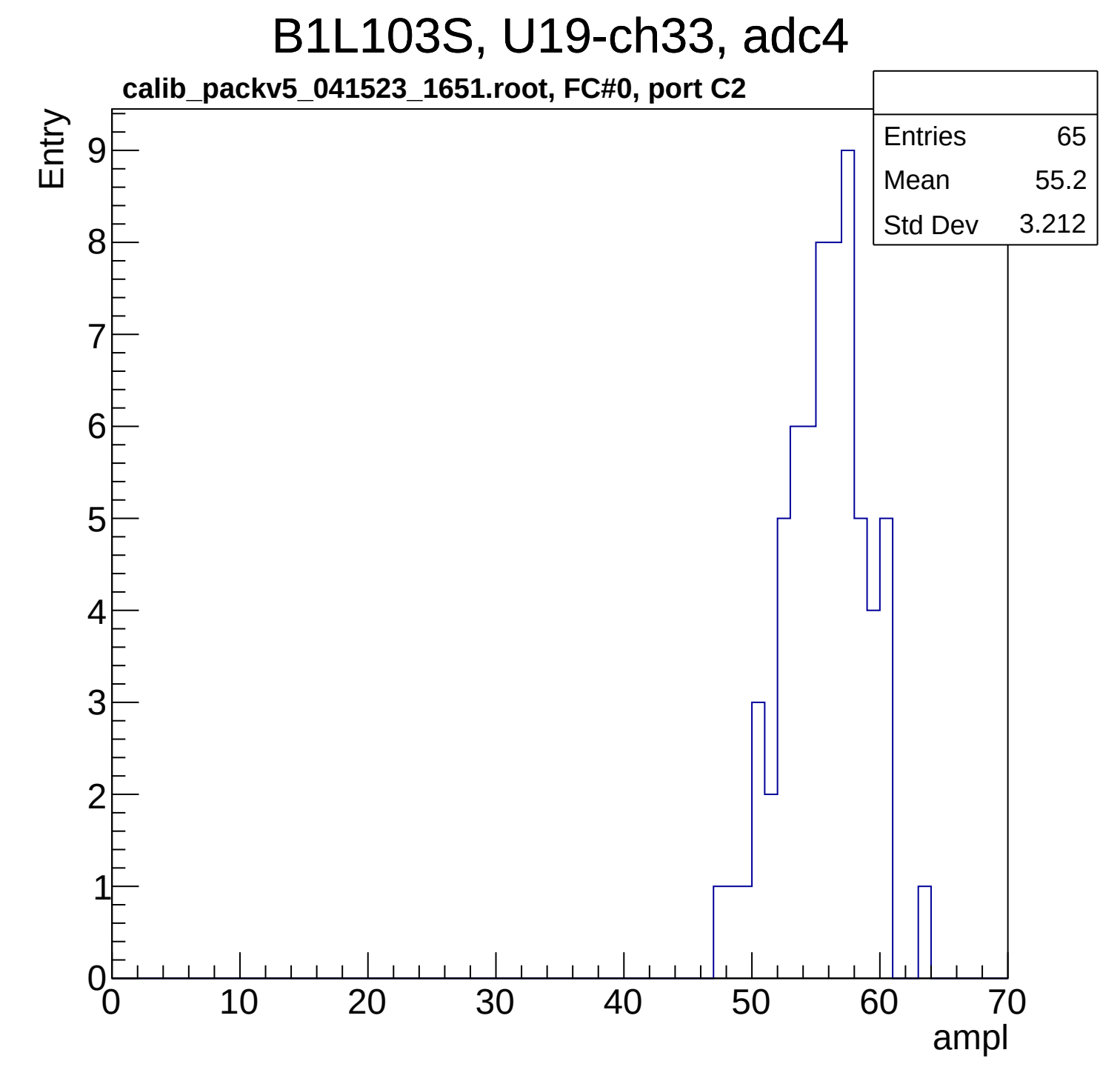
40
50
60
70


B1L103S, U19-ch33, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 55.2
Std Dev 3.212
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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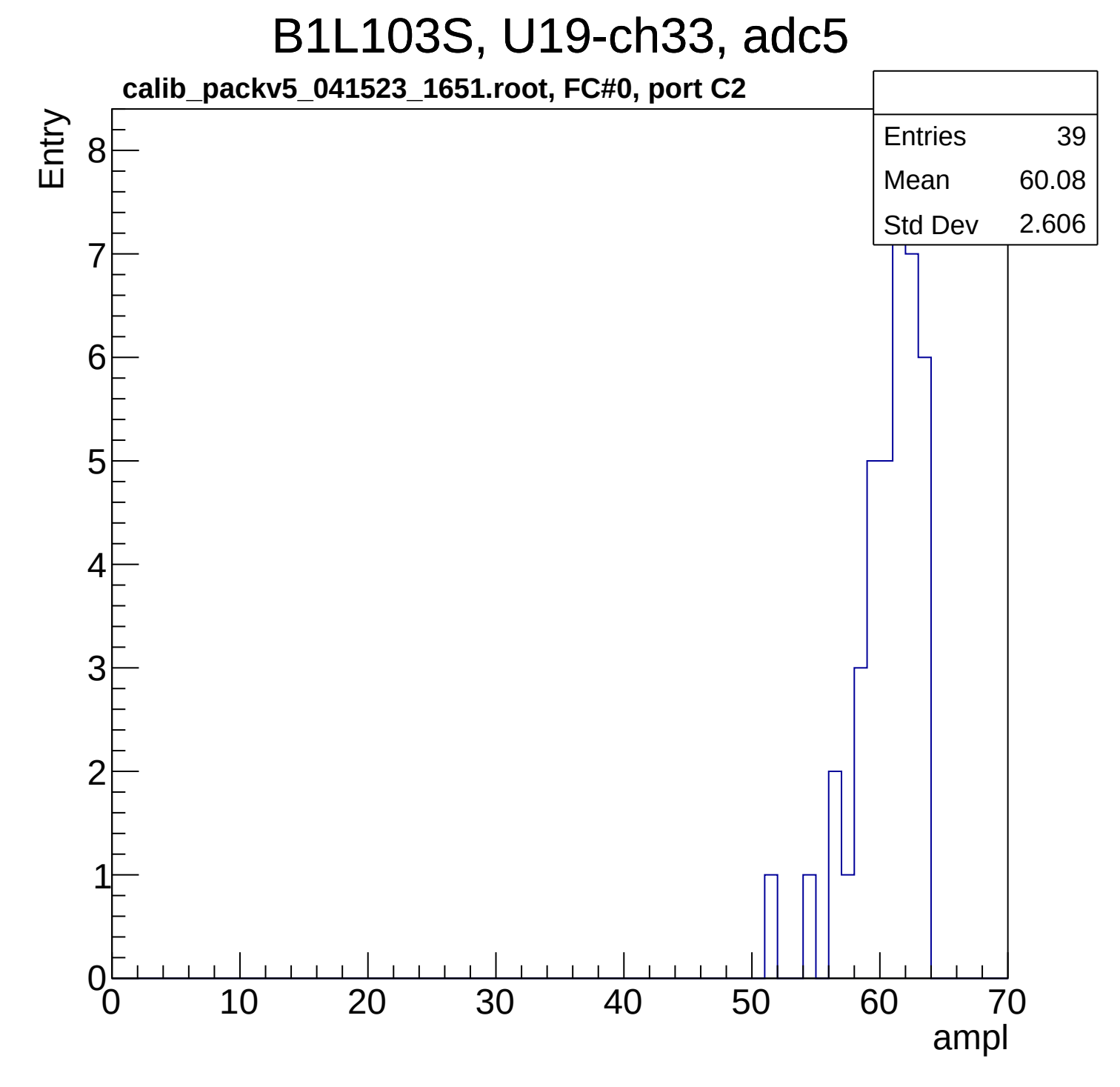
B1L103S, U19-ch33, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 60.08
Std Dev 2.606
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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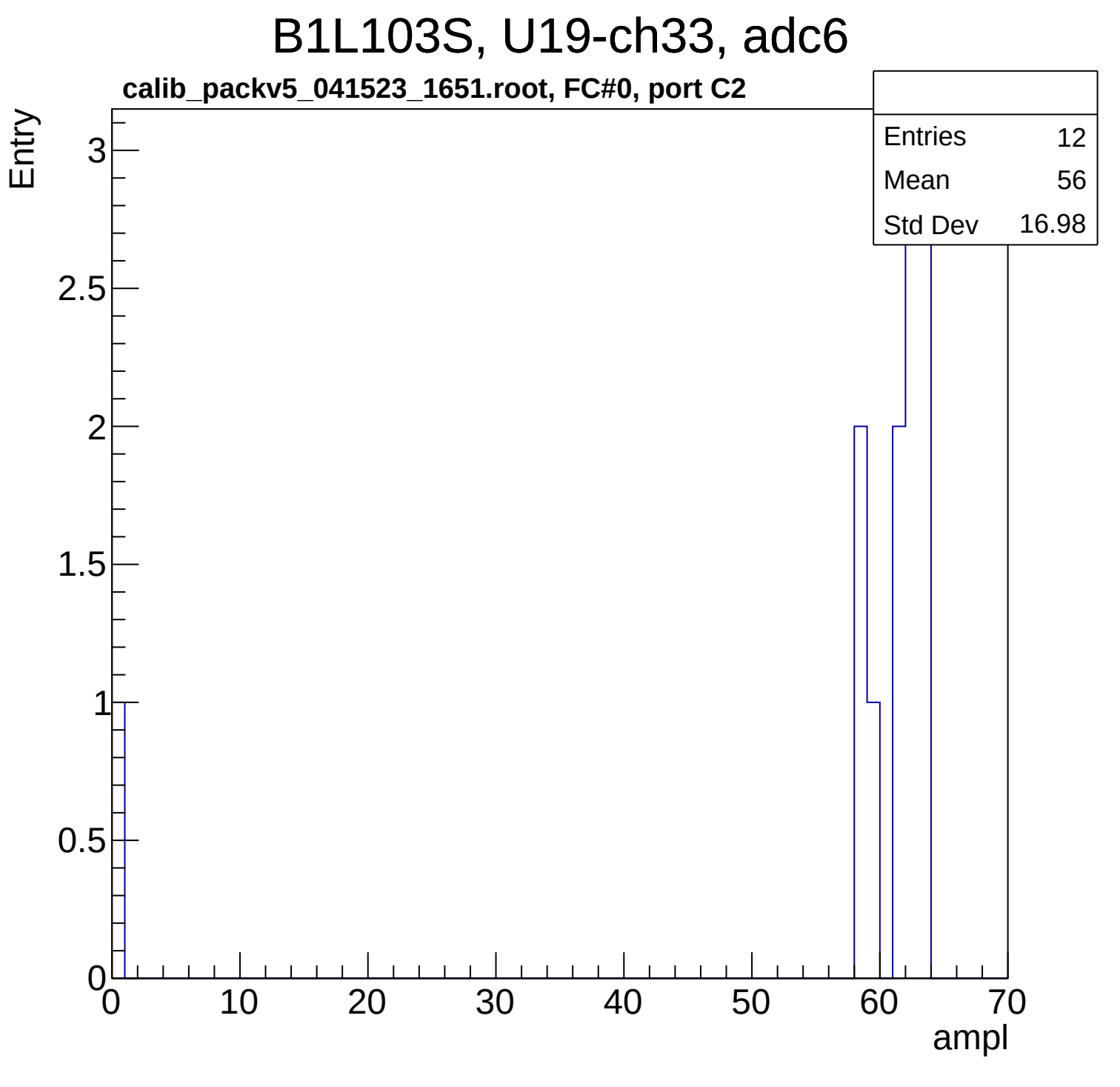
B1L103S, U19-ch33, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 56
Std Dev 16.98
Entry
ampl
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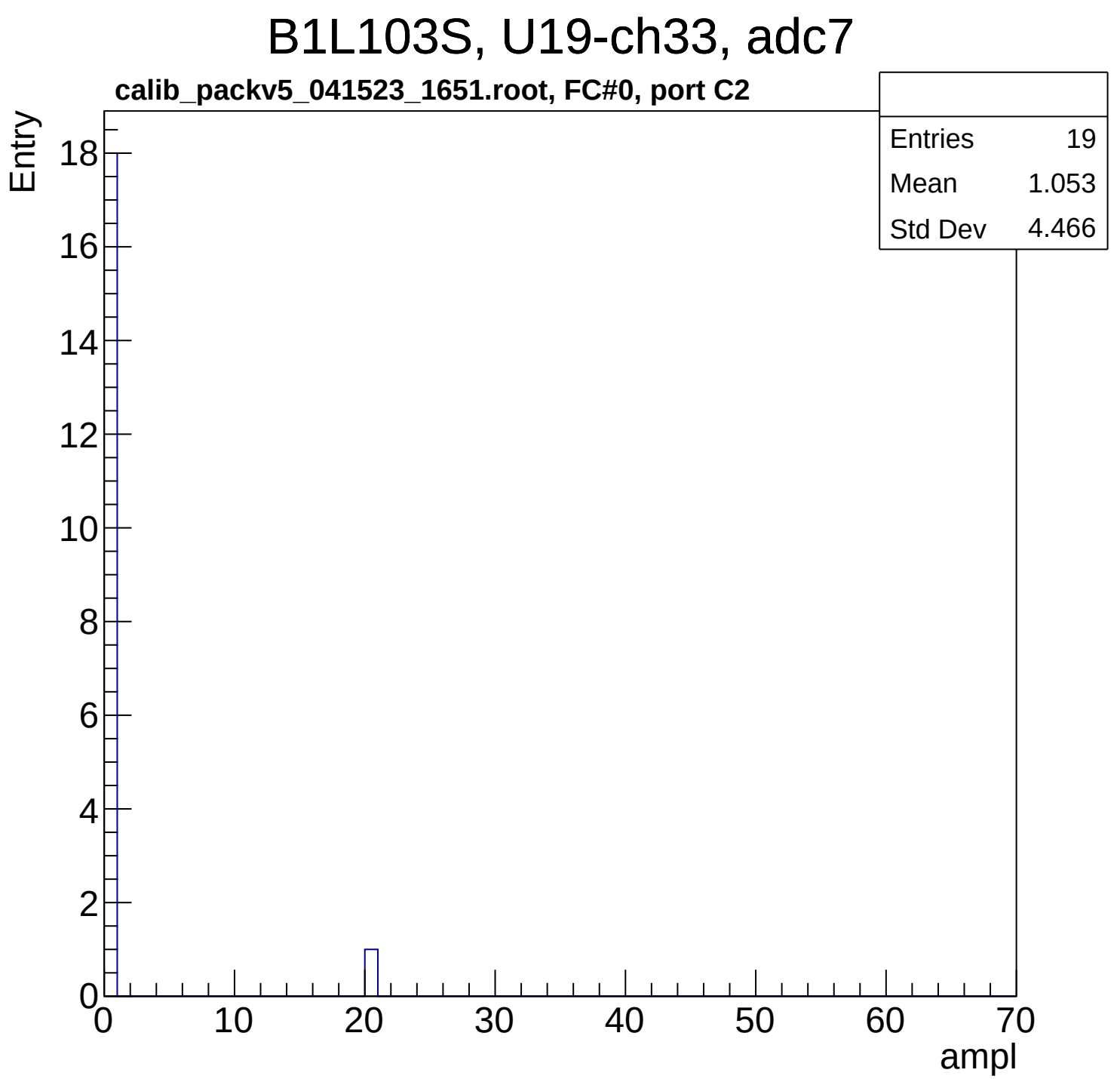
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U19-ch33, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.053
Std Dev 4.466
Entry
0
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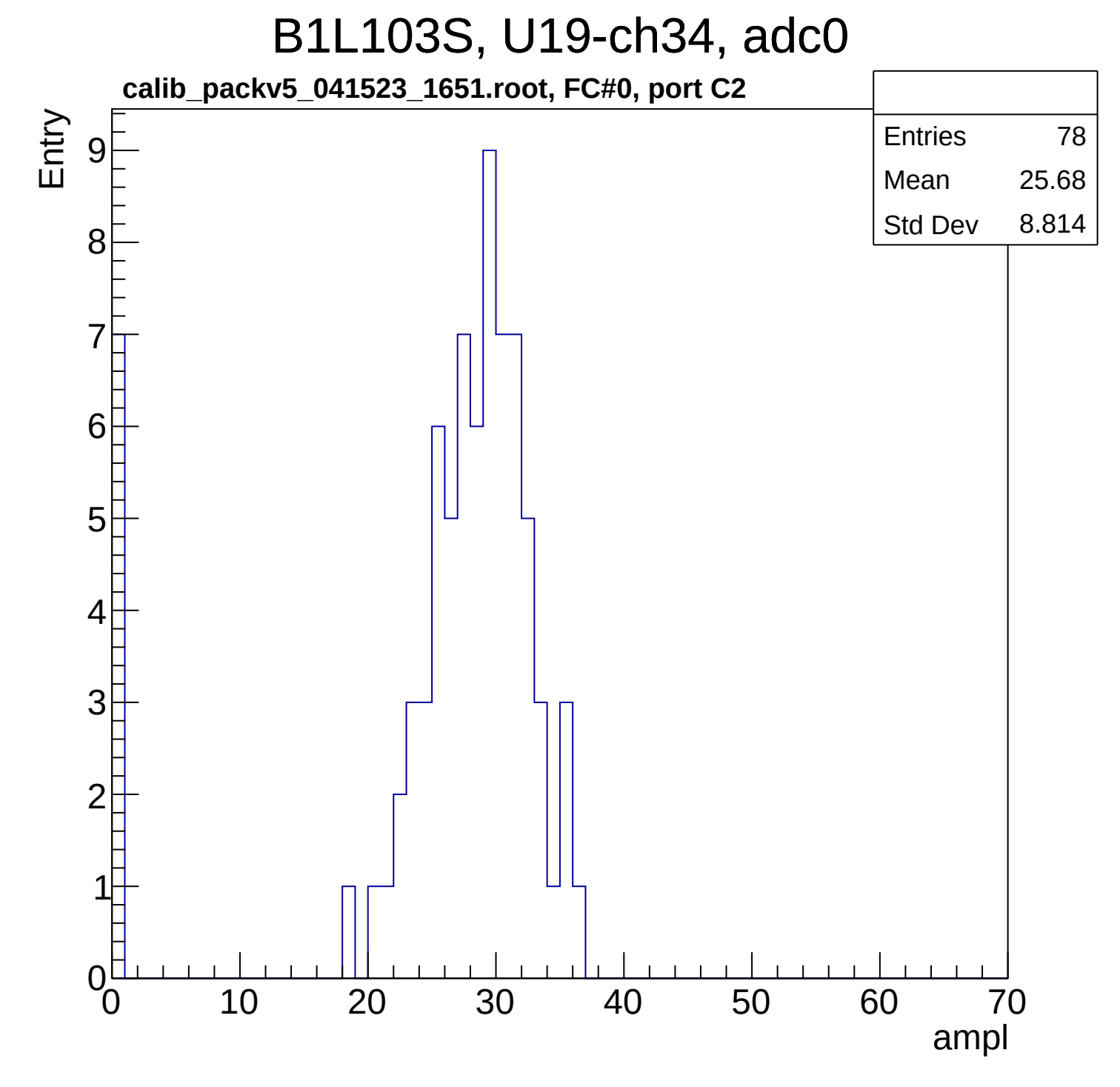
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch34, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 25.68
Std Dev 8.814
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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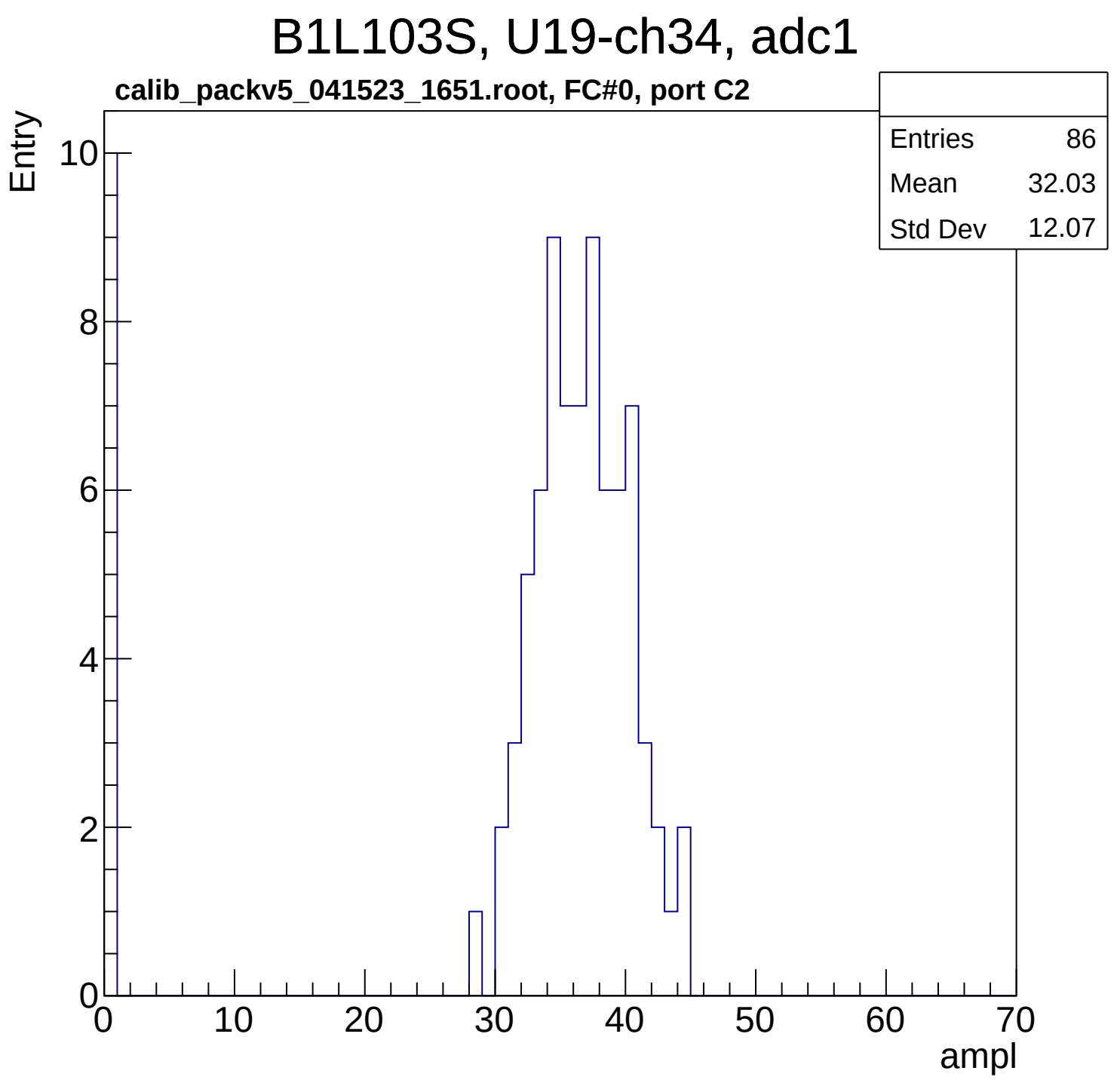
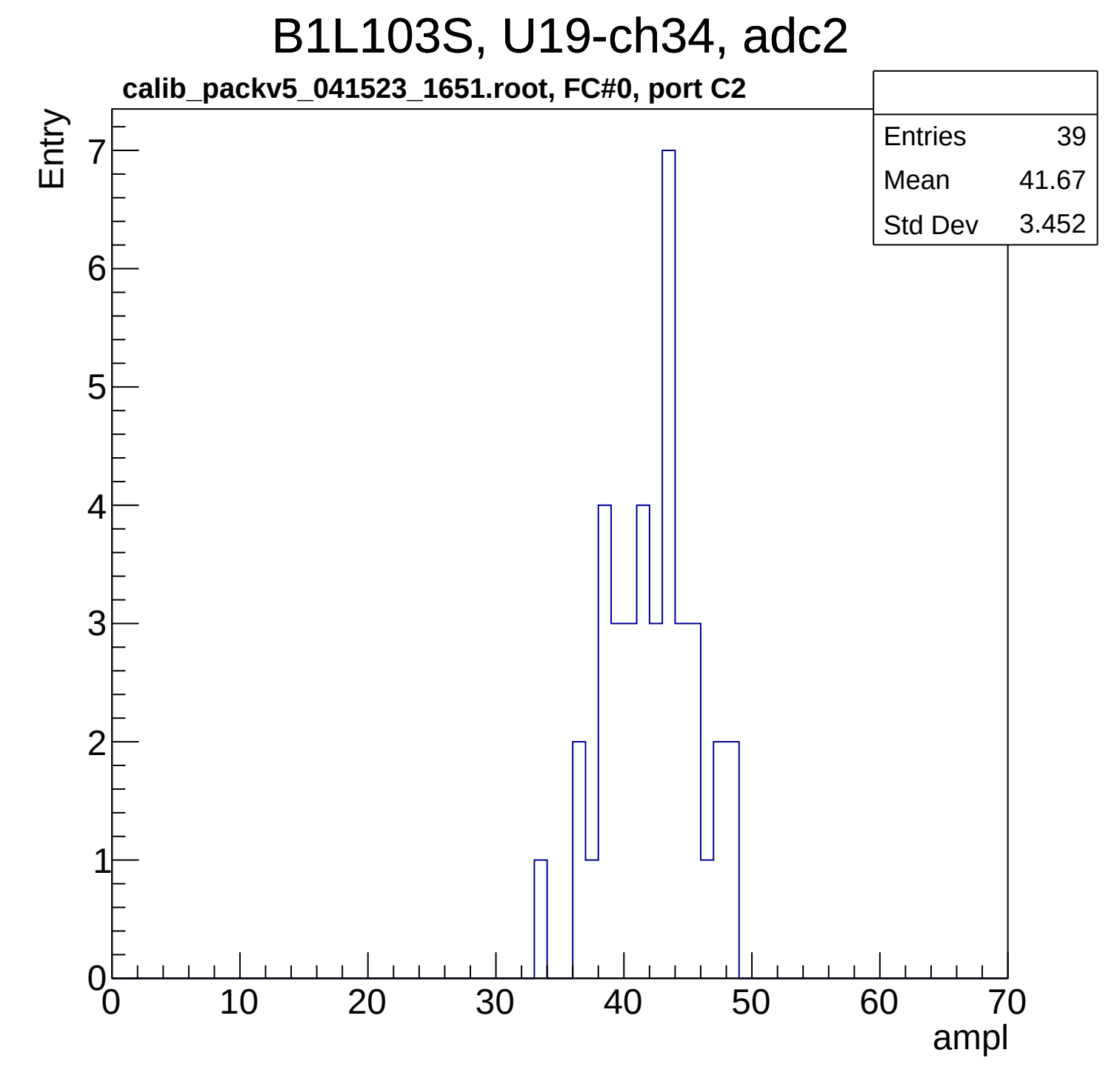

B1L103S, U19-ch34, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 32.03
Std Dev 12.07
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch34, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 41.67
Std Dev 3.452
Entry
ampl
0
1
2
3
4
5
6
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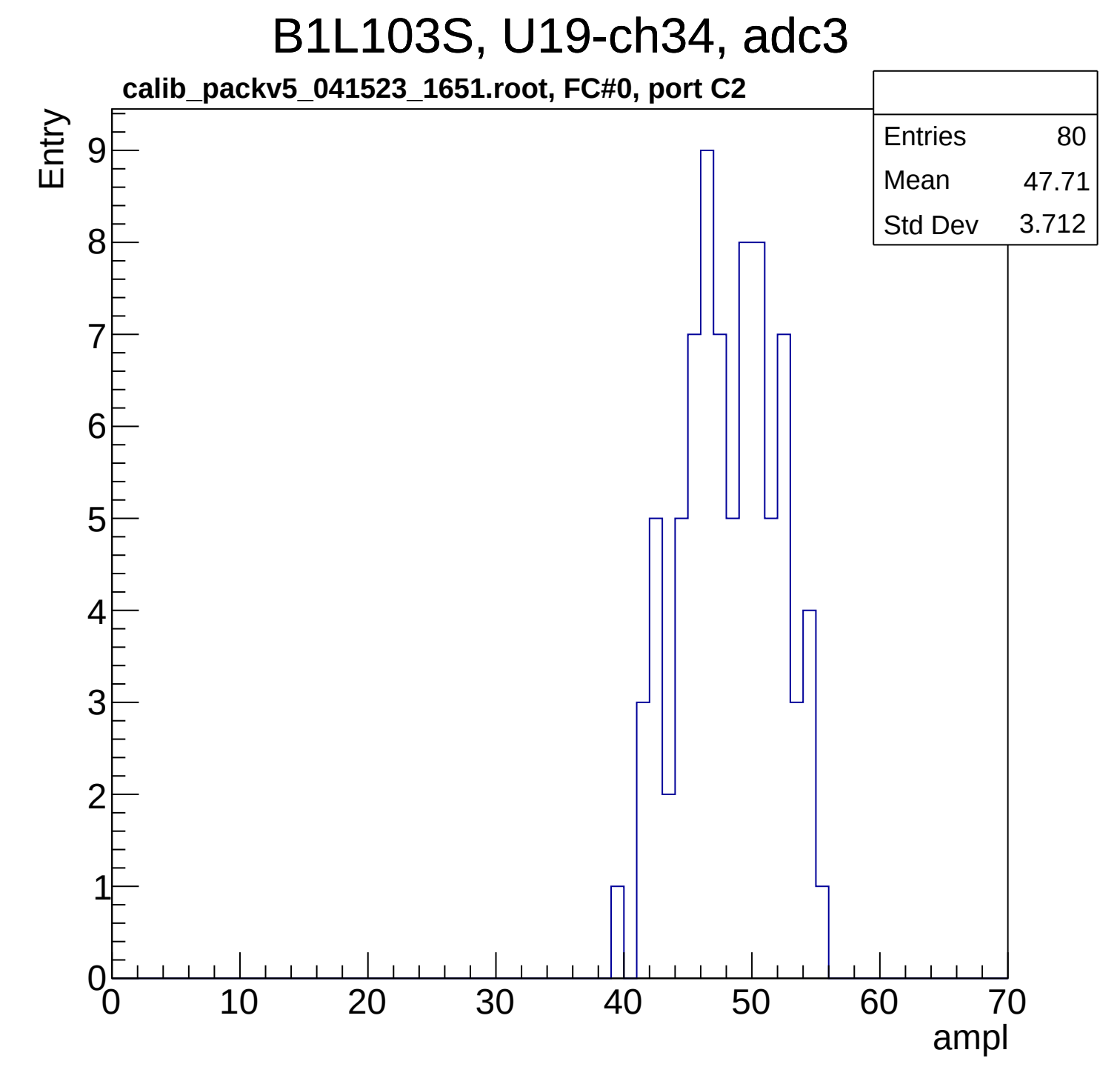
0
10
20
30
40
50
60
70


B1L103S, U19-ch34, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 47.71
Std Dev 3.712
Entry
ampl
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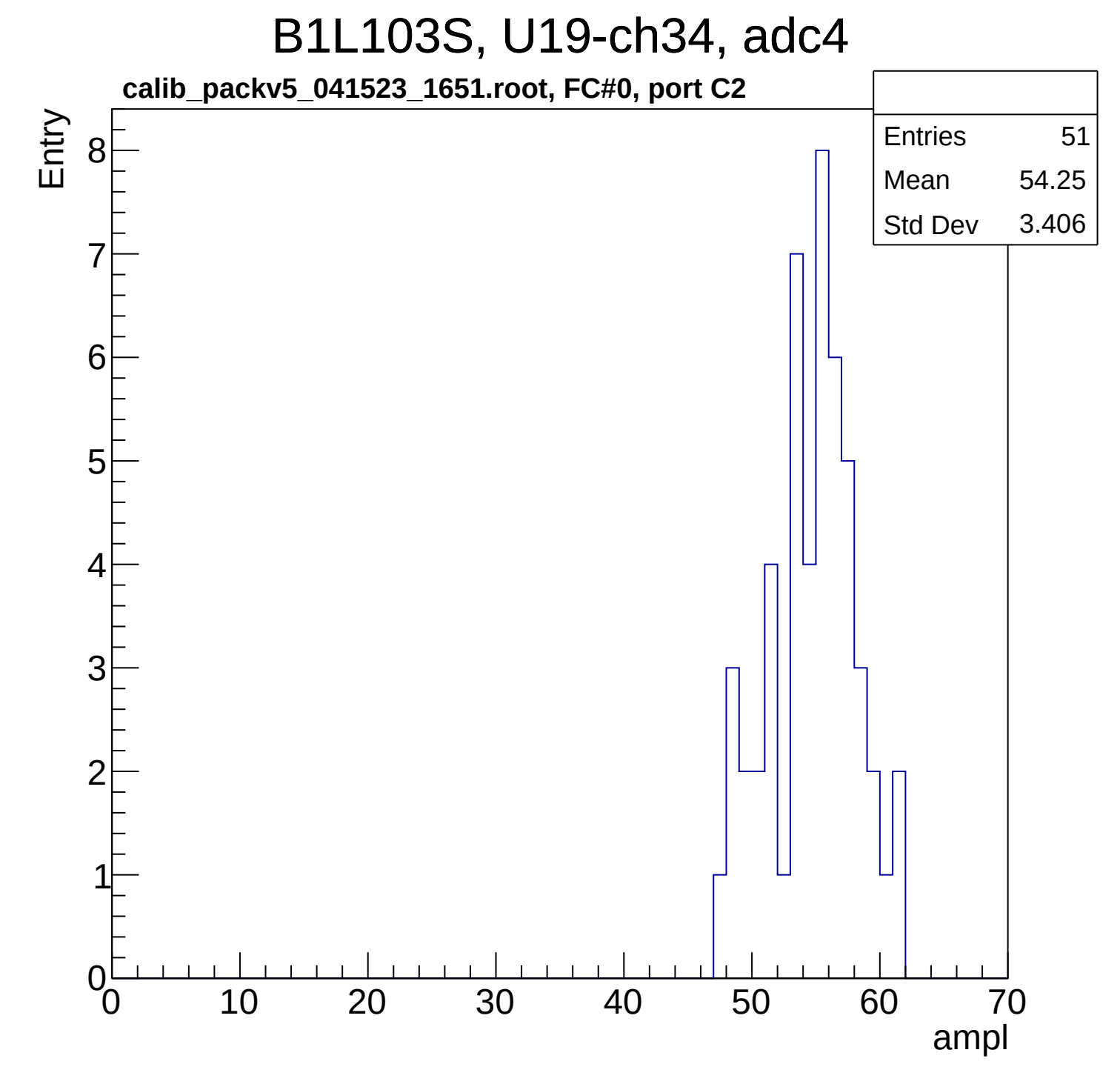
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch34, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 54.25
Std Dev 3.406
Entry
ampl
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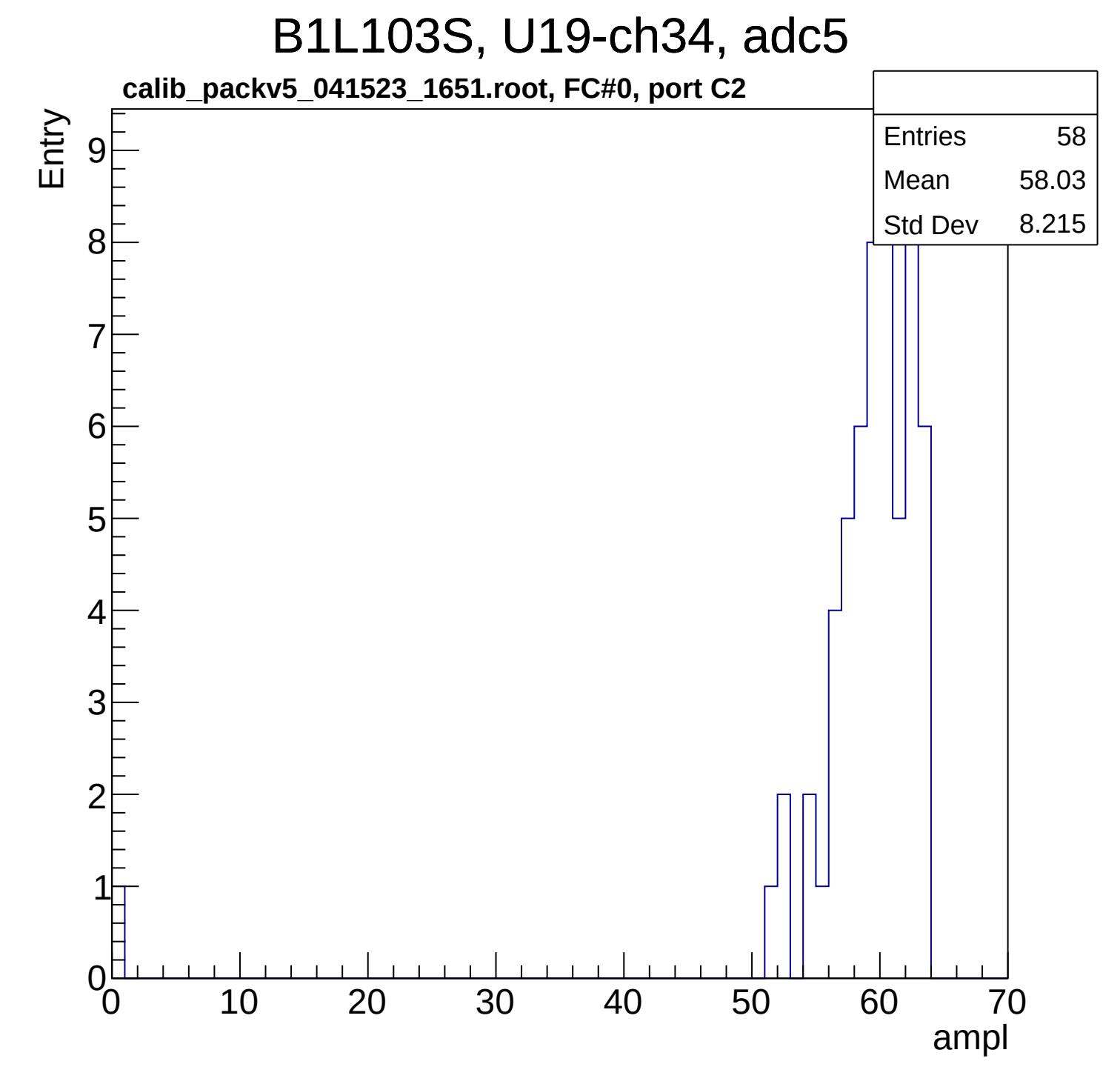
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch34, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 58.03
Std Dev 8.215
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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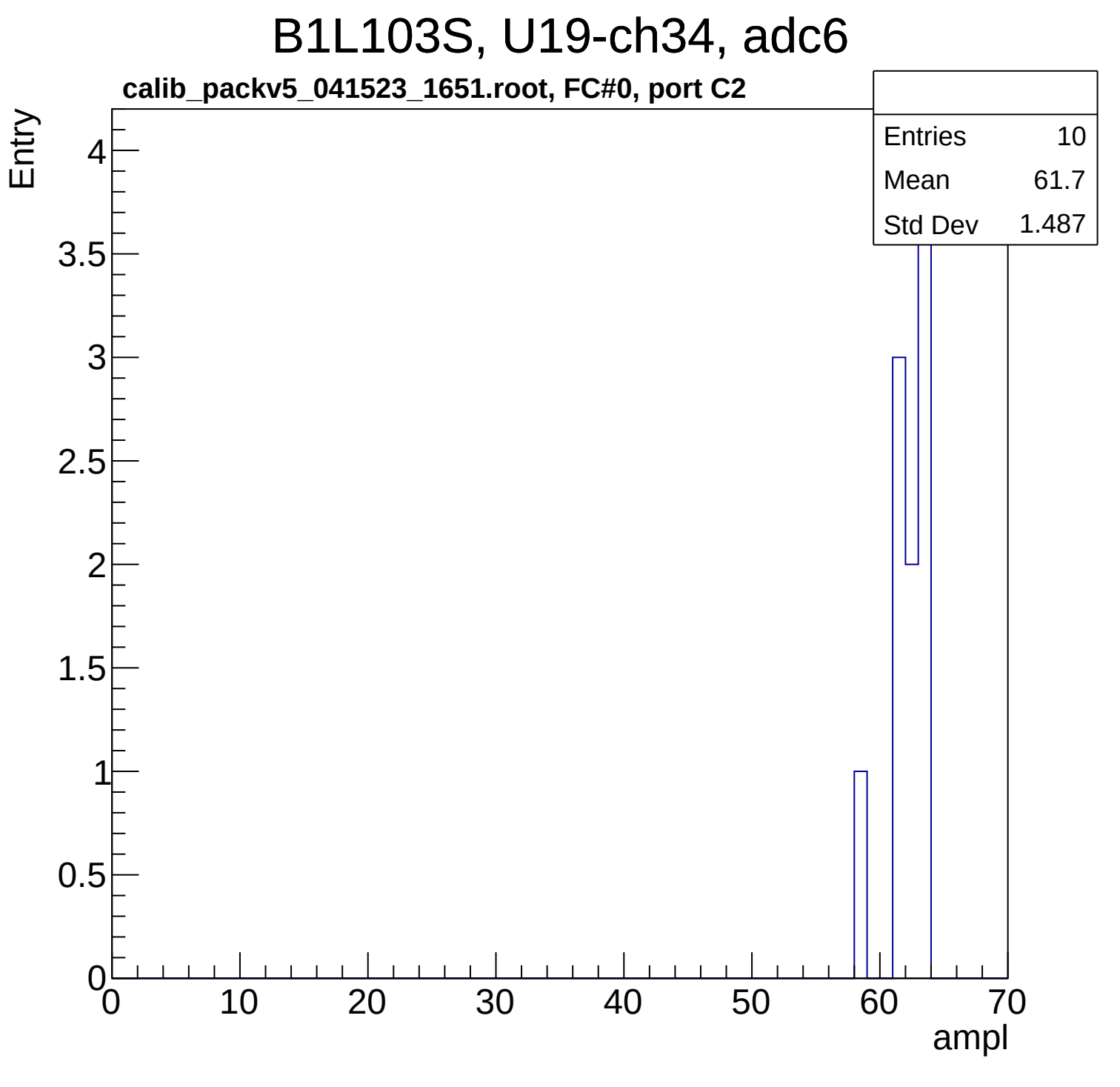
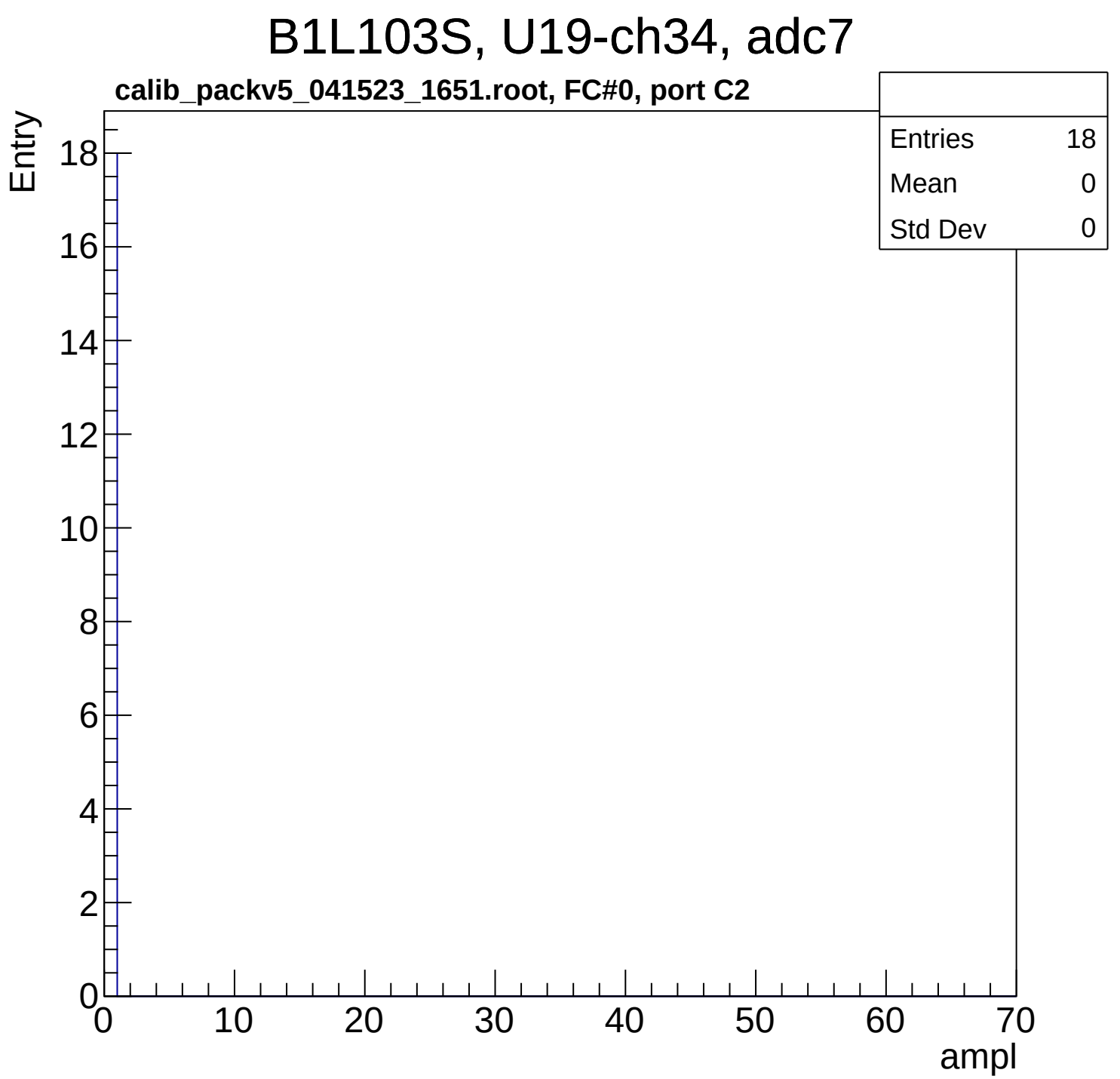

B1L103S, U19-ch34, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61.7
Std Dev 1.487
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U19-ch34, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
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10
20
30
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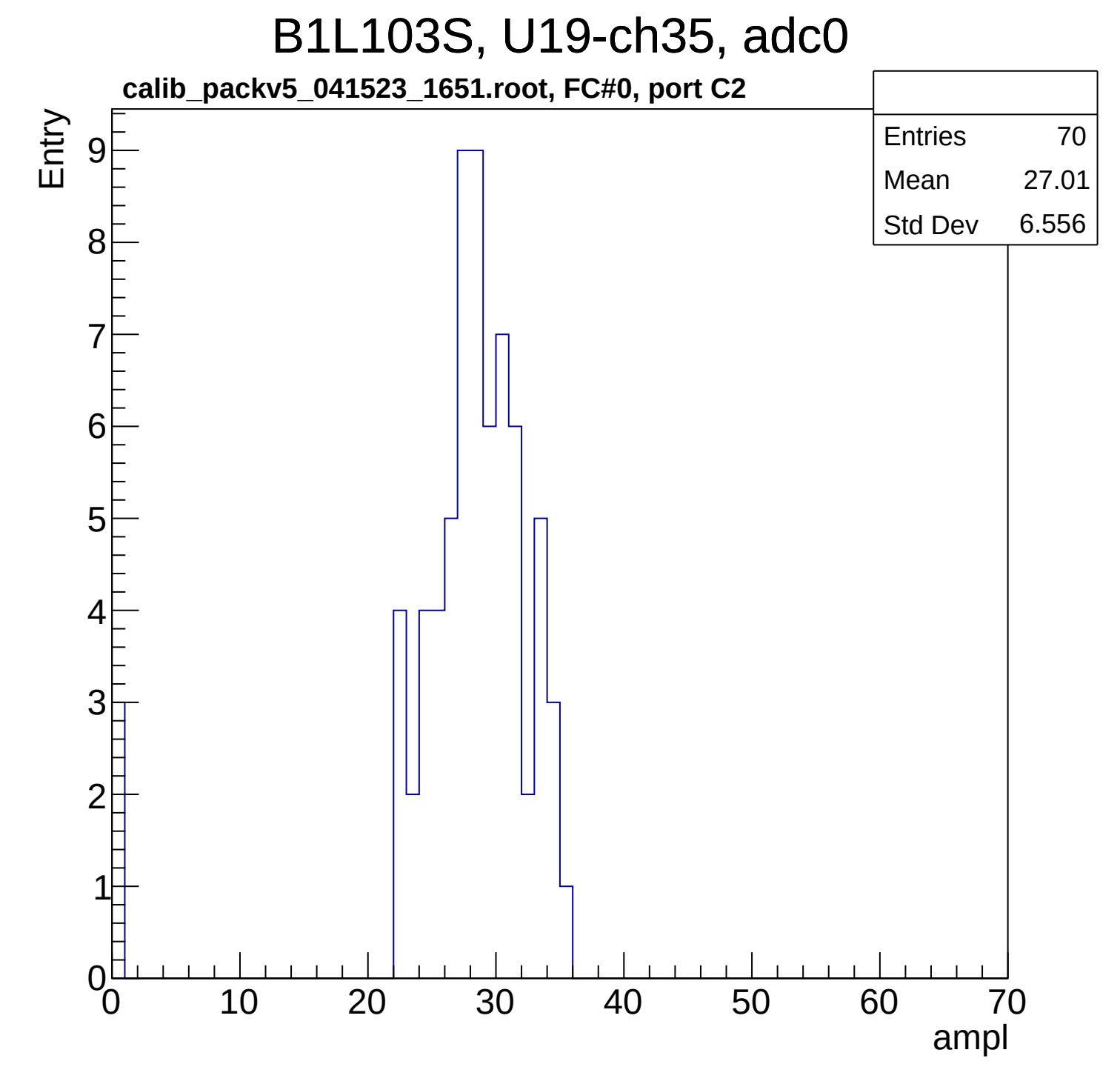
50
60
70
ampl


B1L103S, U19-ch35, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 27.01
Std Dev 6.556
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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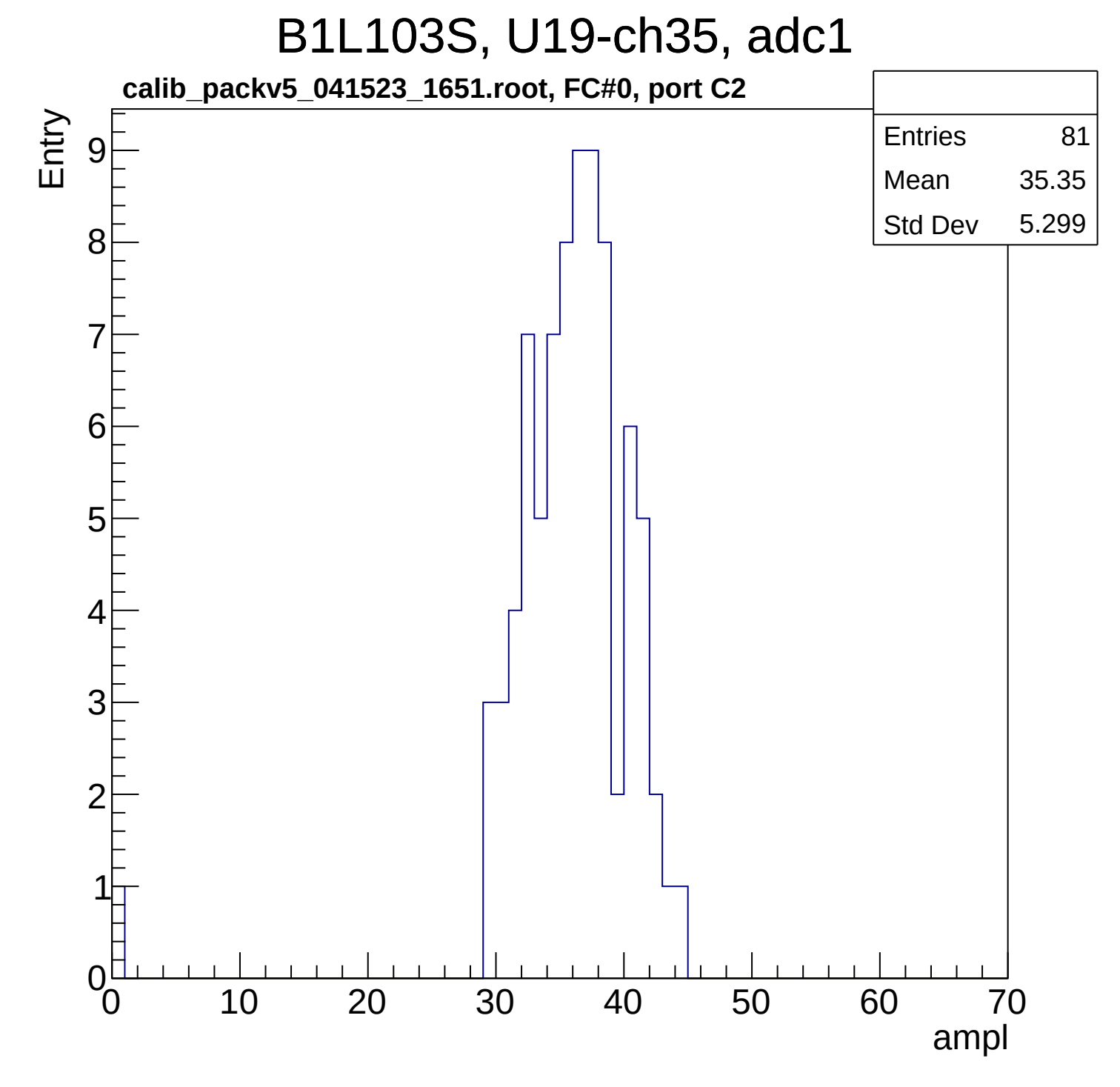
B1L103S, U19-ch35, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 35.35
Std Dev 5.299
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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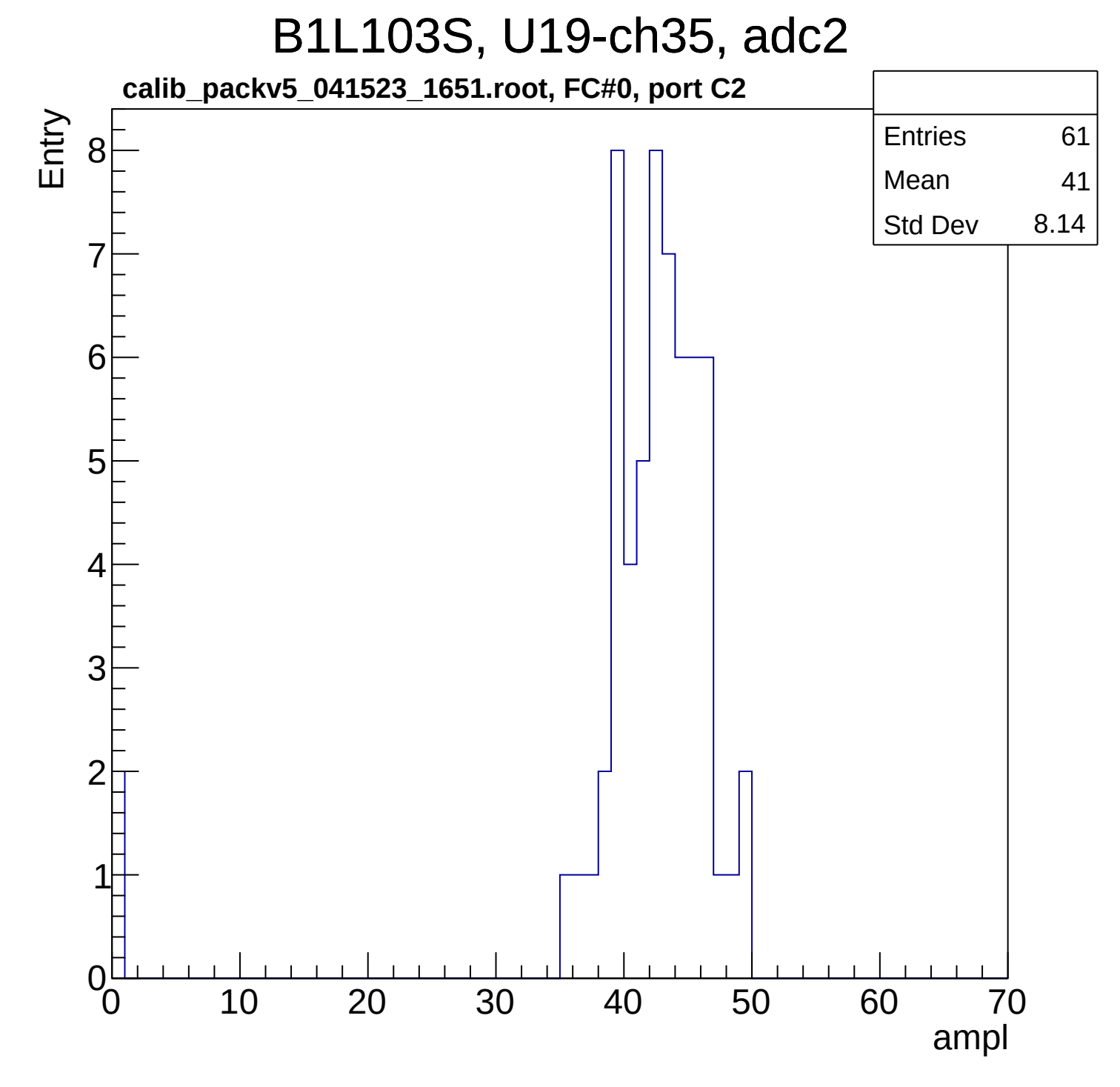
B1L103S, U19-ch35, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 41
Std Dev 8.14
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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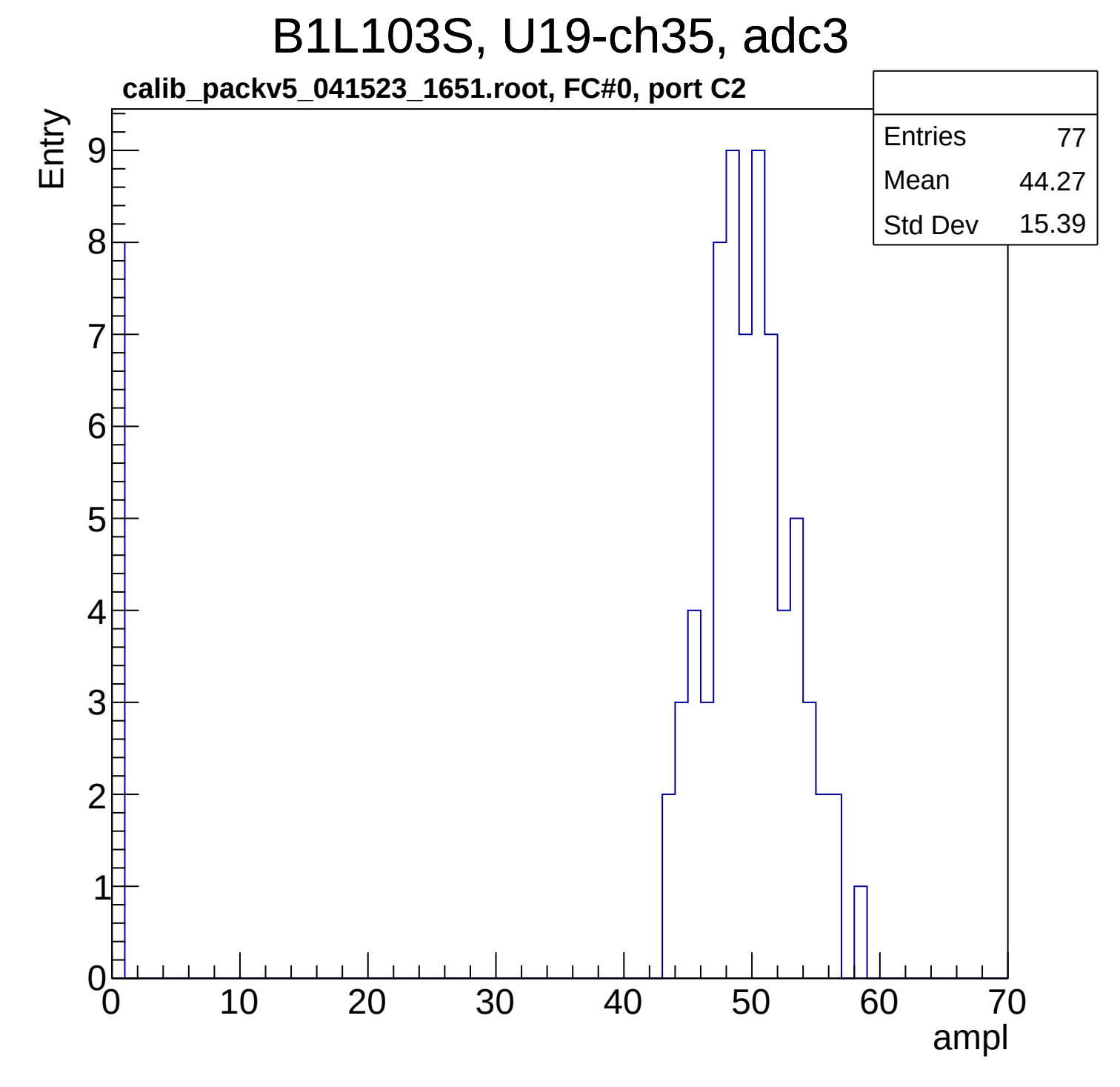
B1L103S, U19-ch35, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 44.27
Std Dev 15.39
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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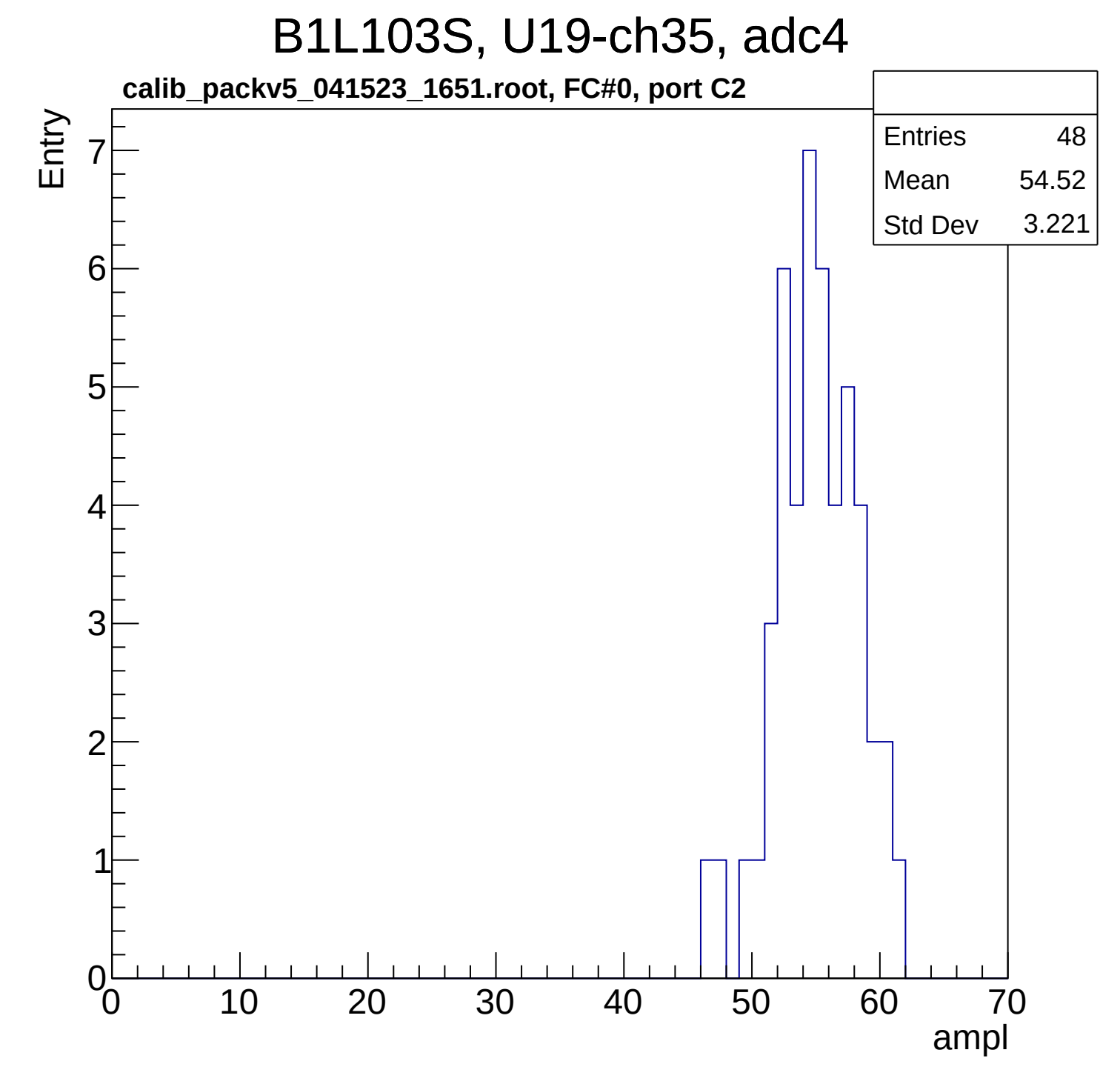
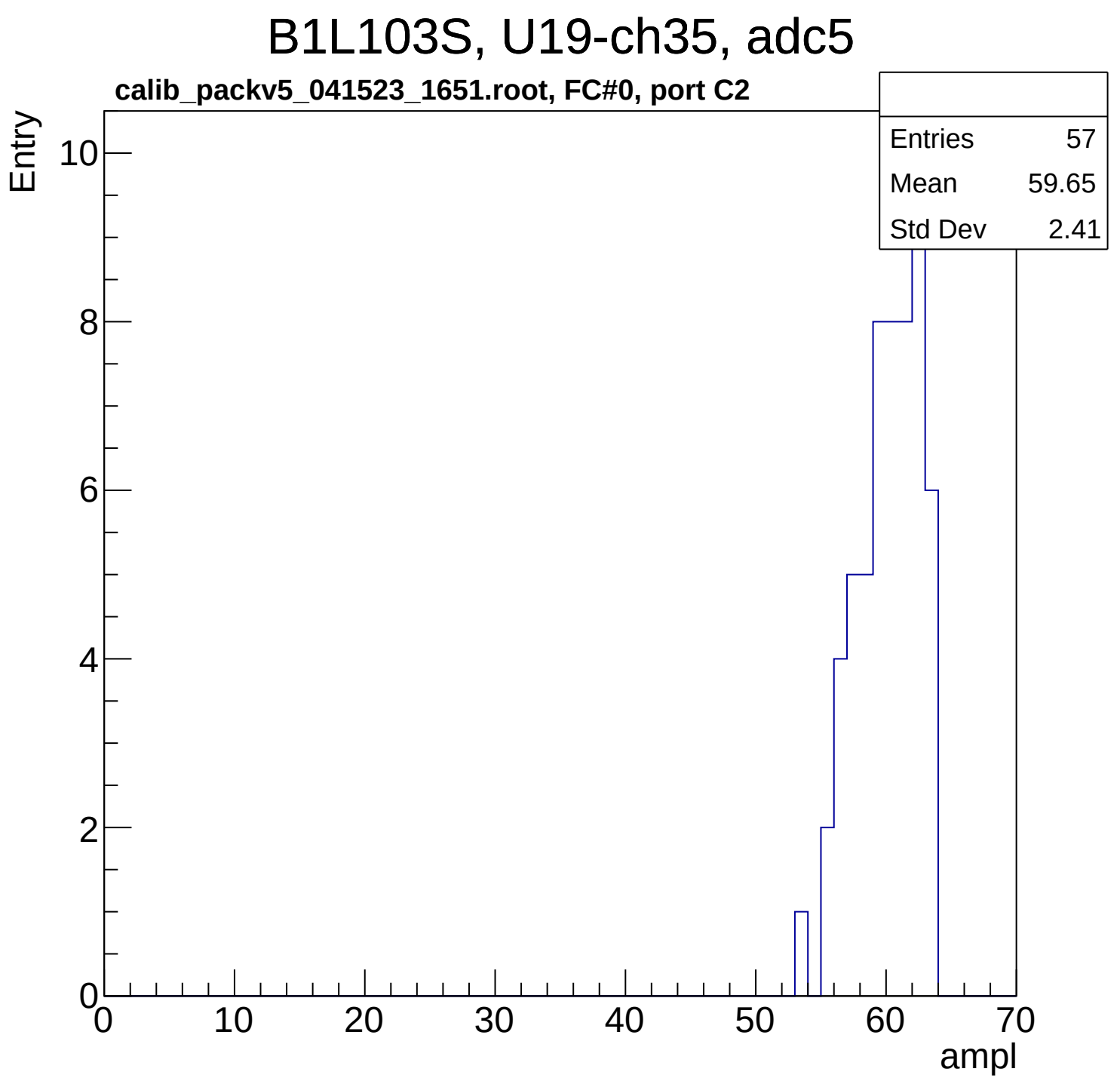
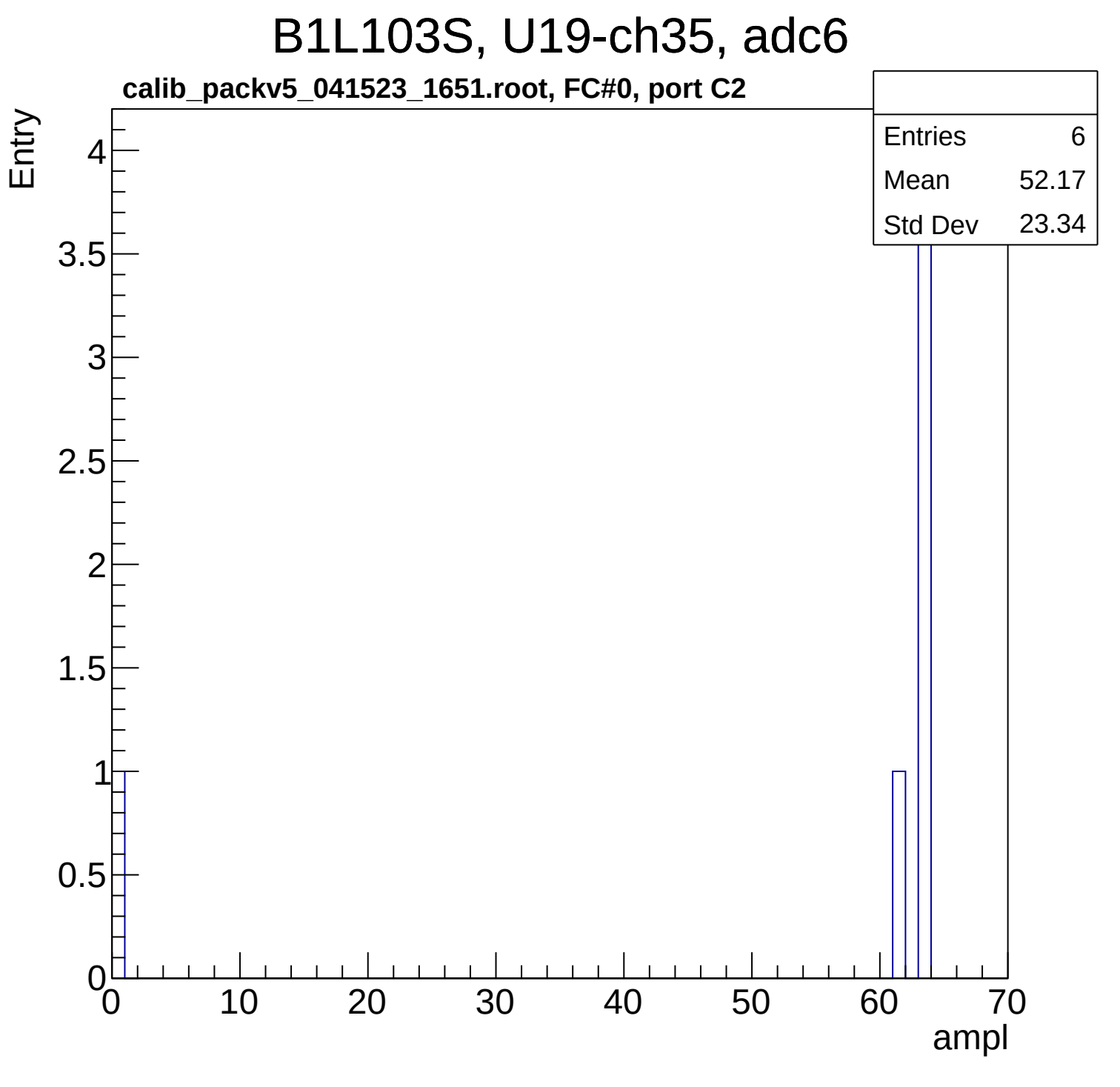
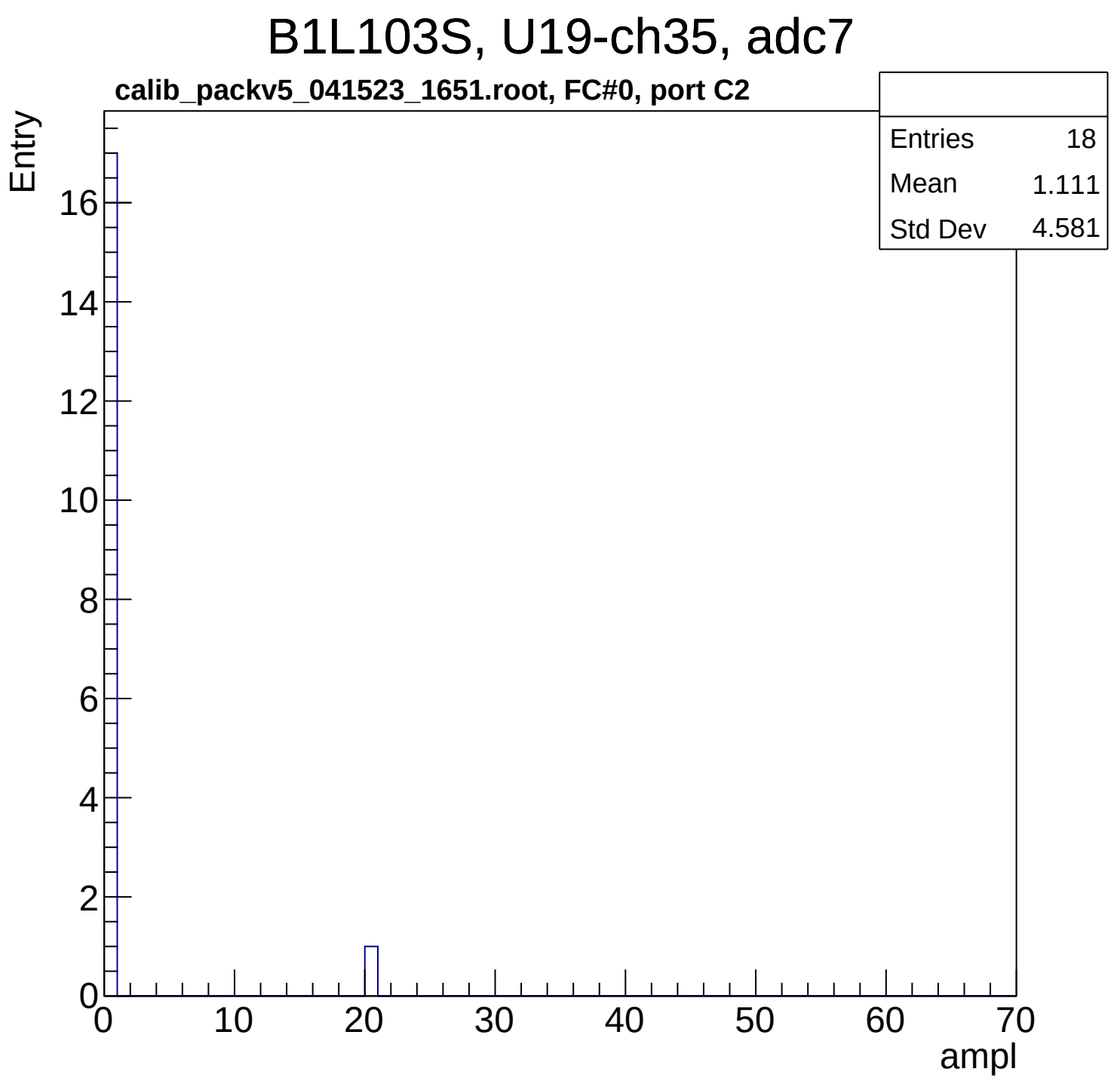
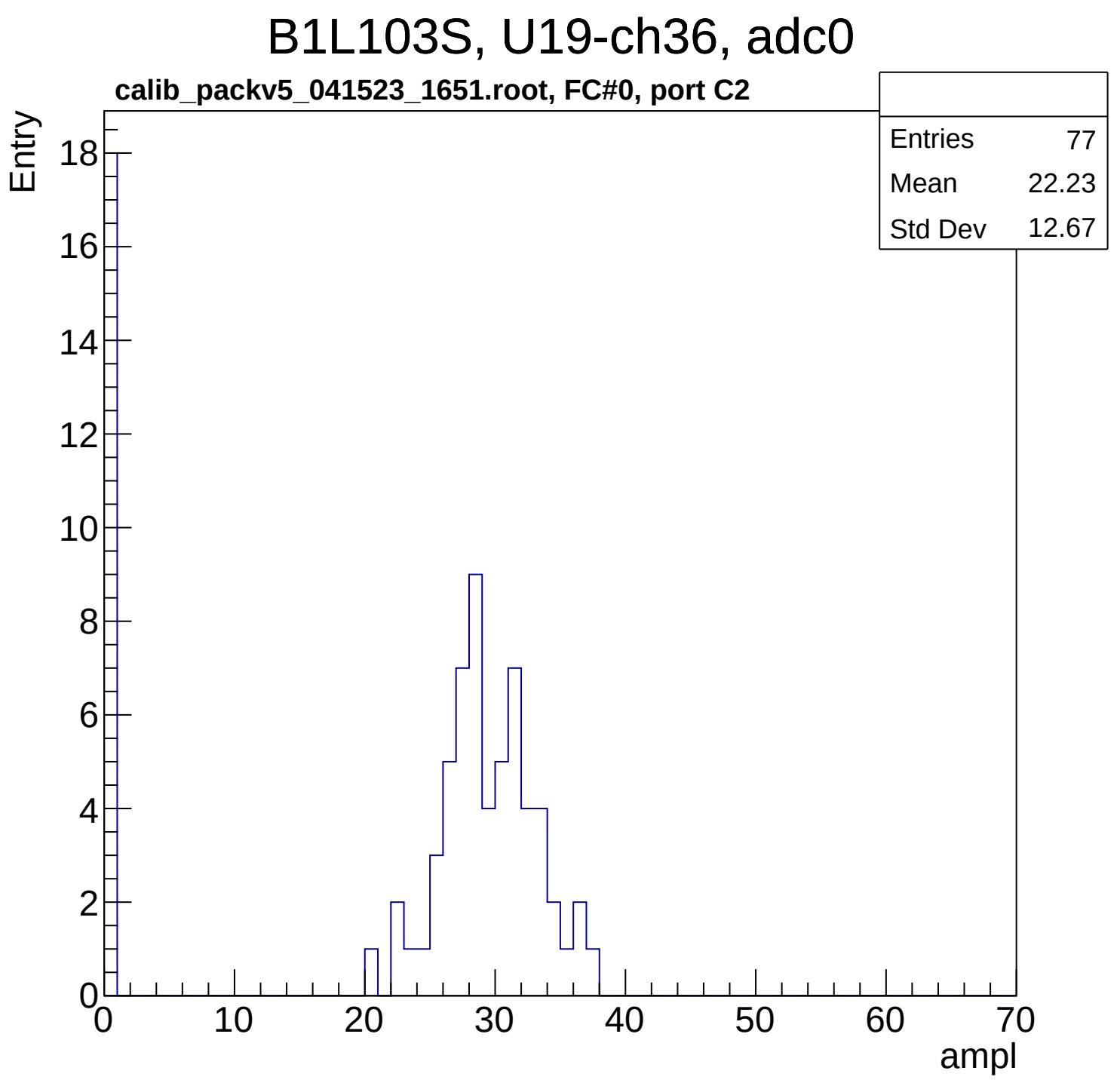
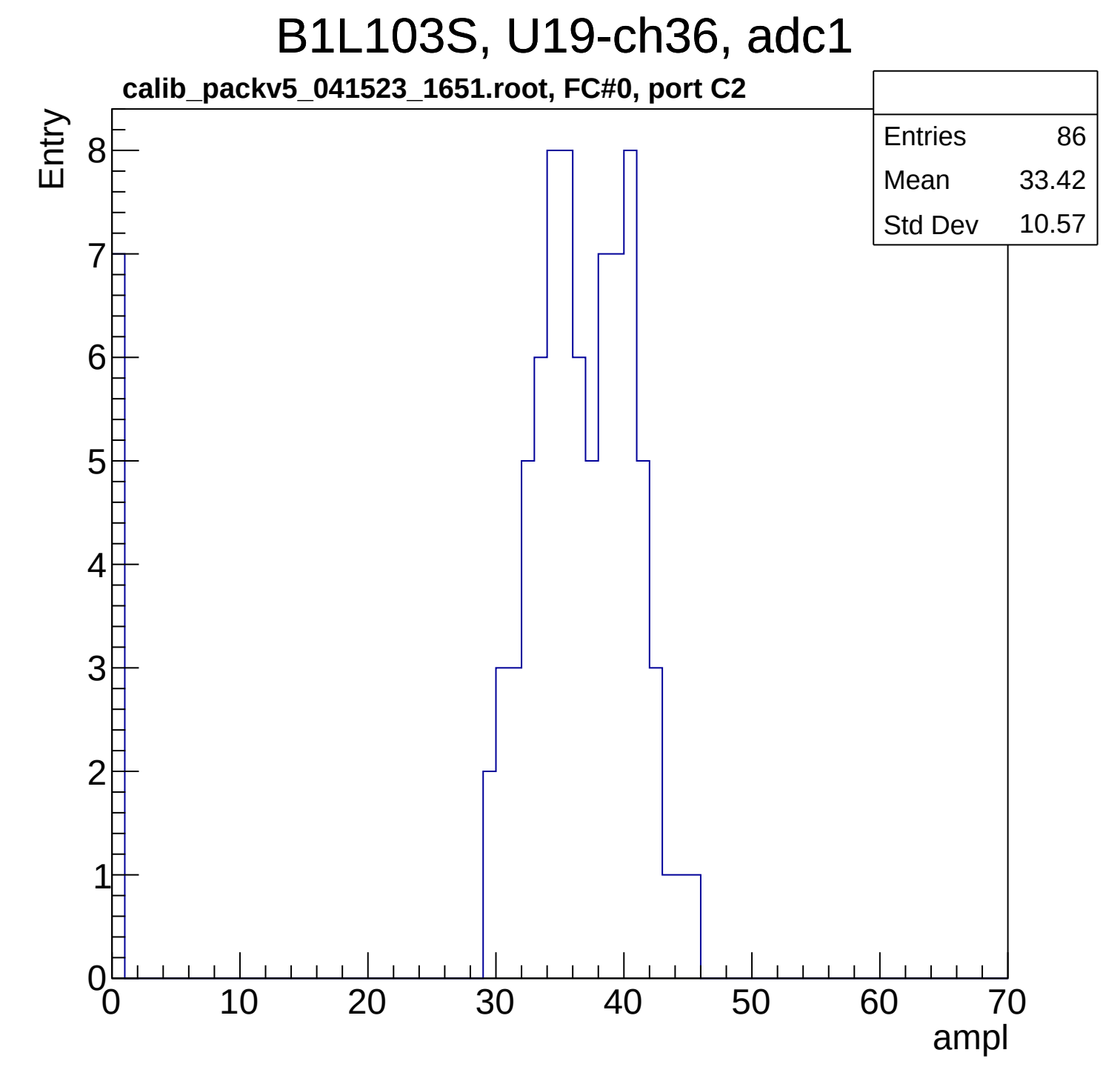

B1L103S, U19-ch35, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 54.52
Std Dev 3.221
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

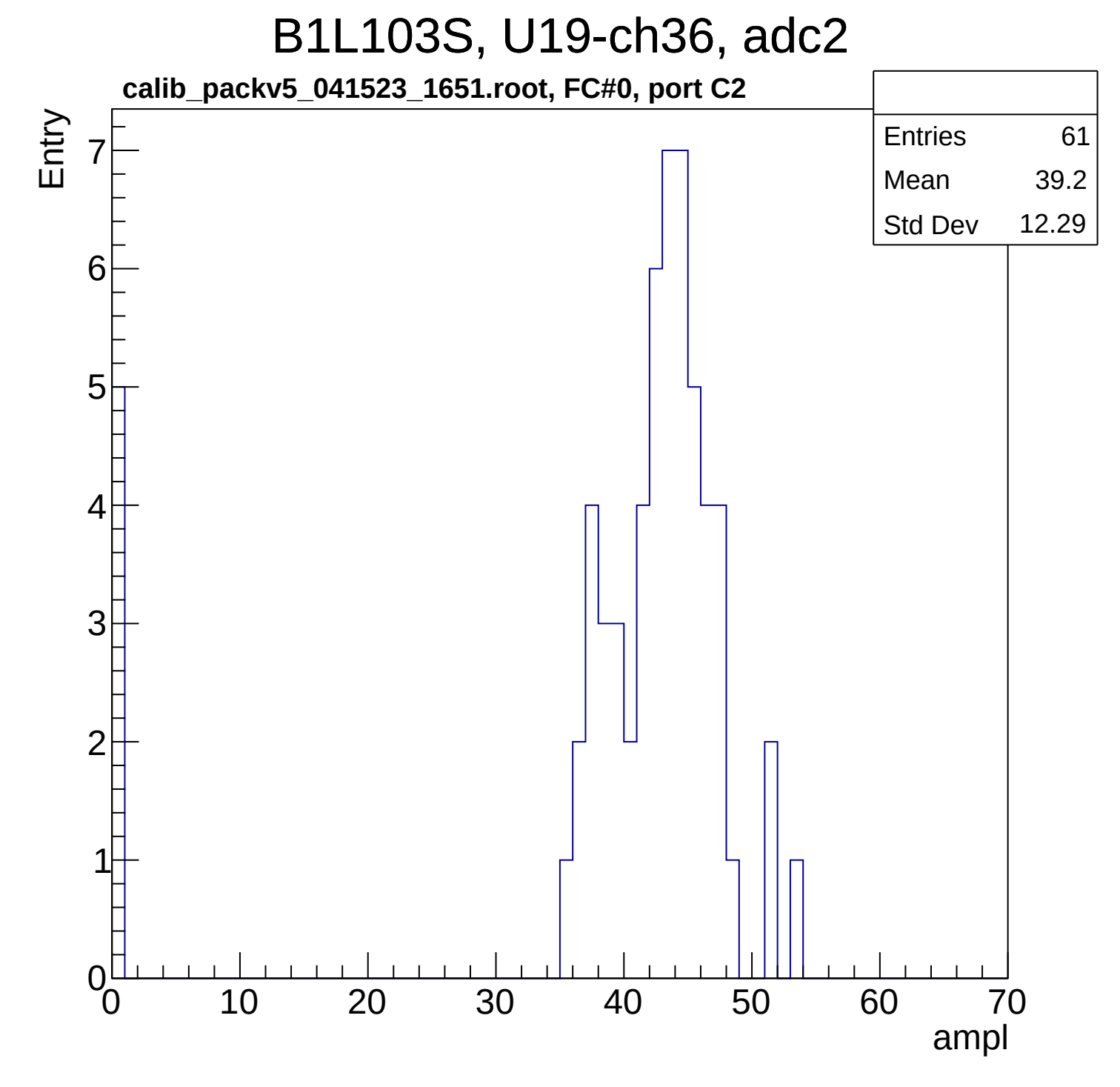

B1L103S, U19-ch35, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 59.65
Std Dev 2.41
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

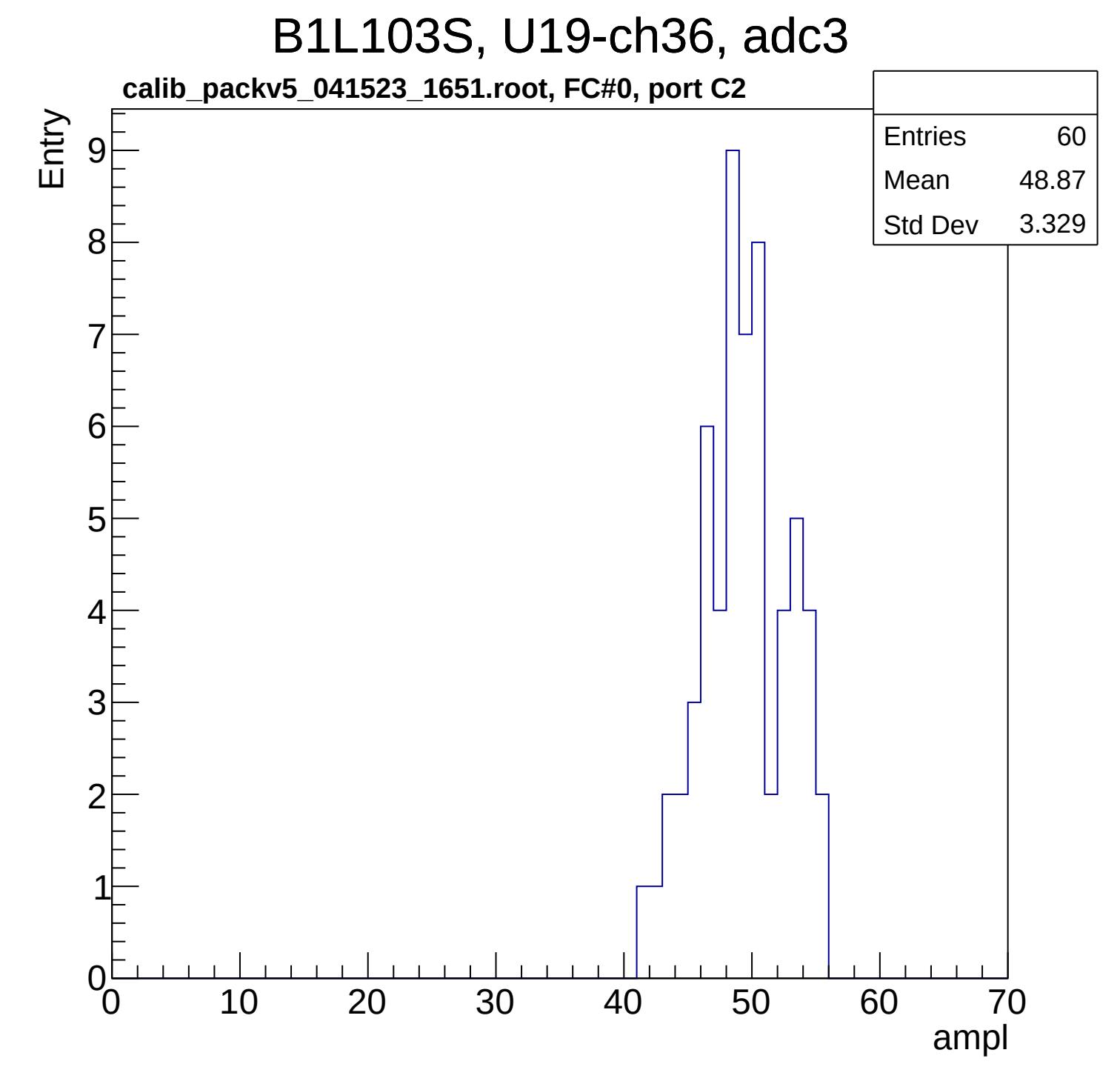

B1L103S, U19-ch35, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 52.17
Std Dev 23.34
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

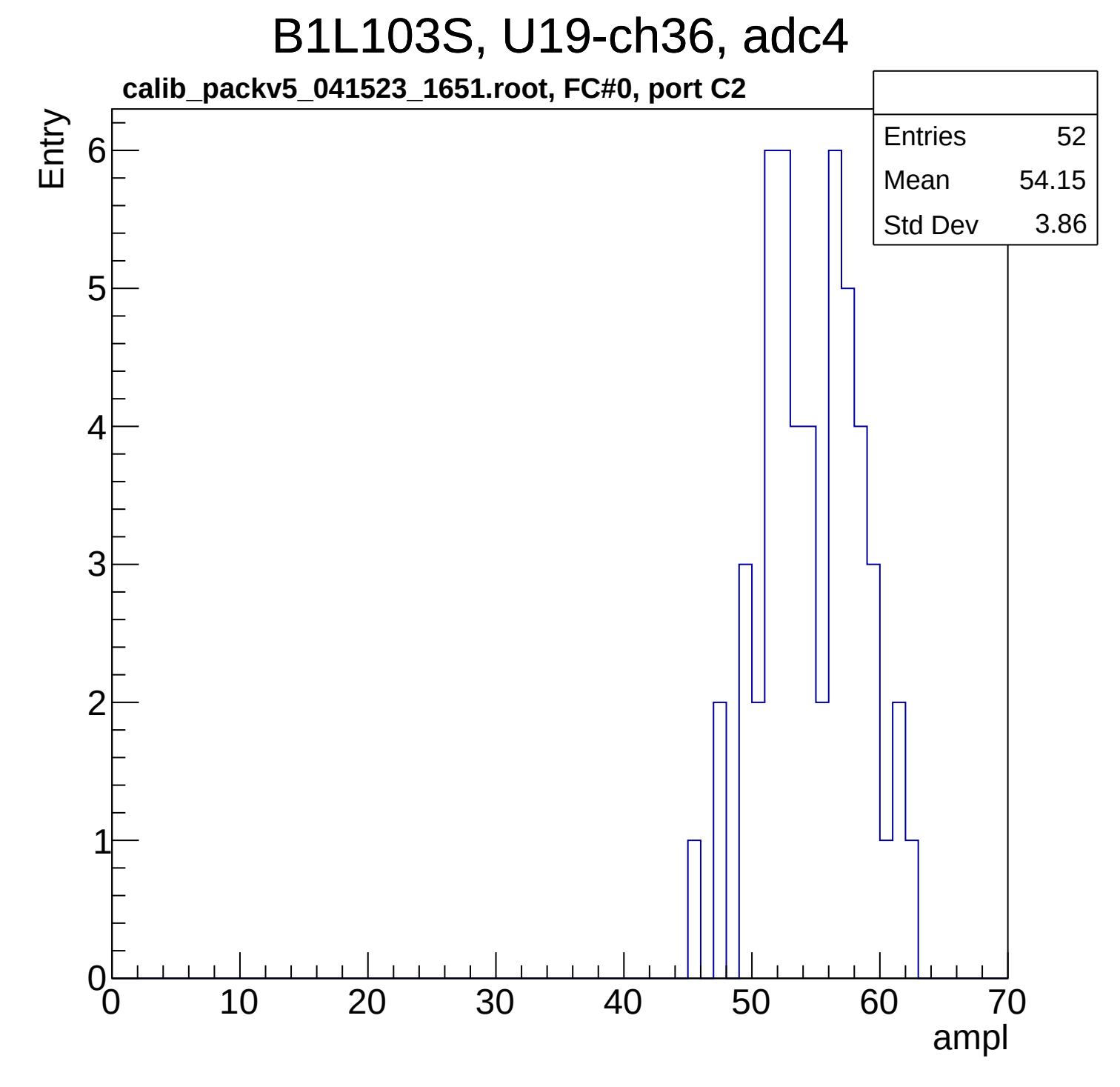

B1L103S, U19-ch35, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.111
Std Dev 4.581
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

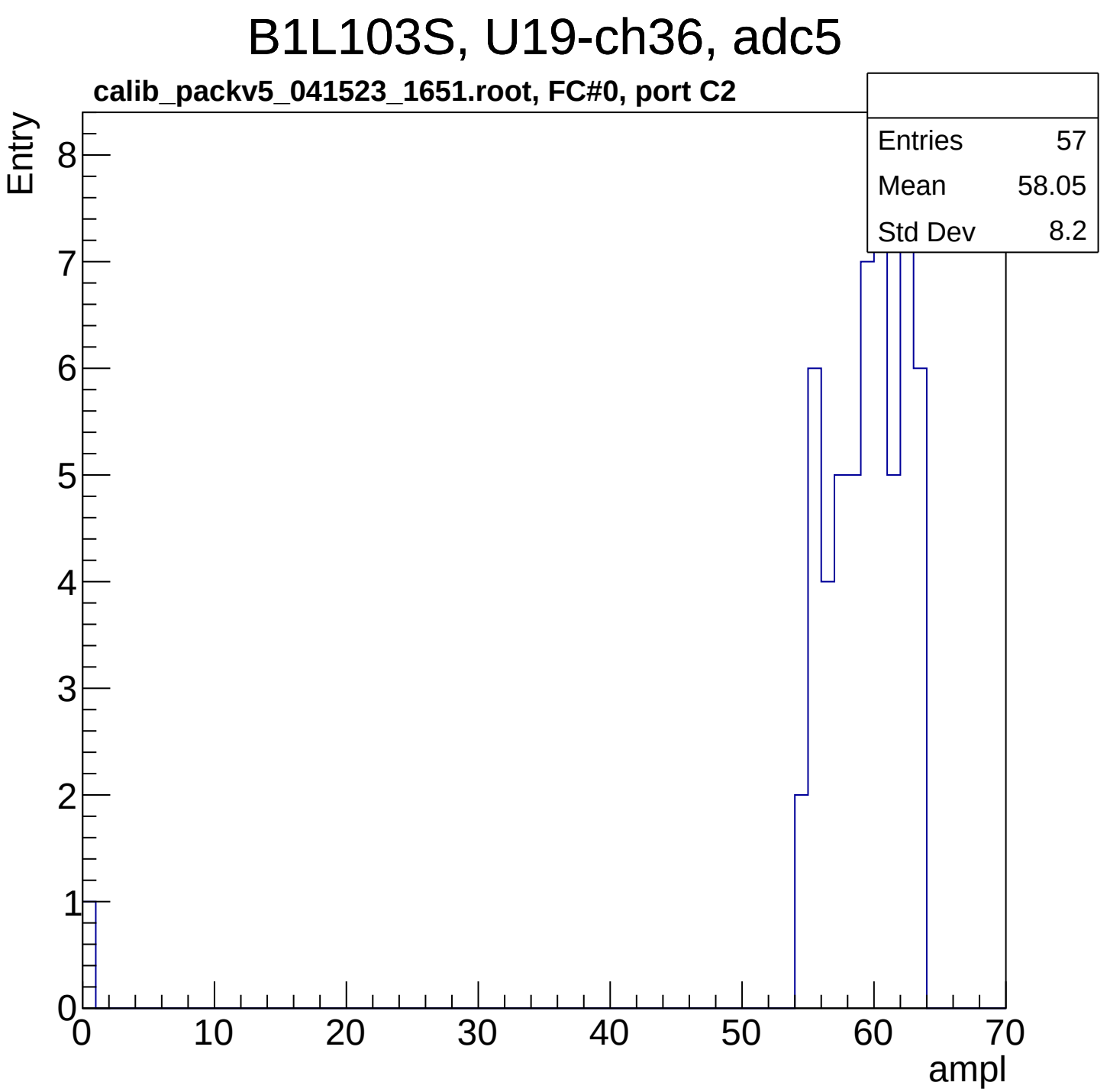

B1L103S, U19-ch36, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 22.23
Std Dev 12.67
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

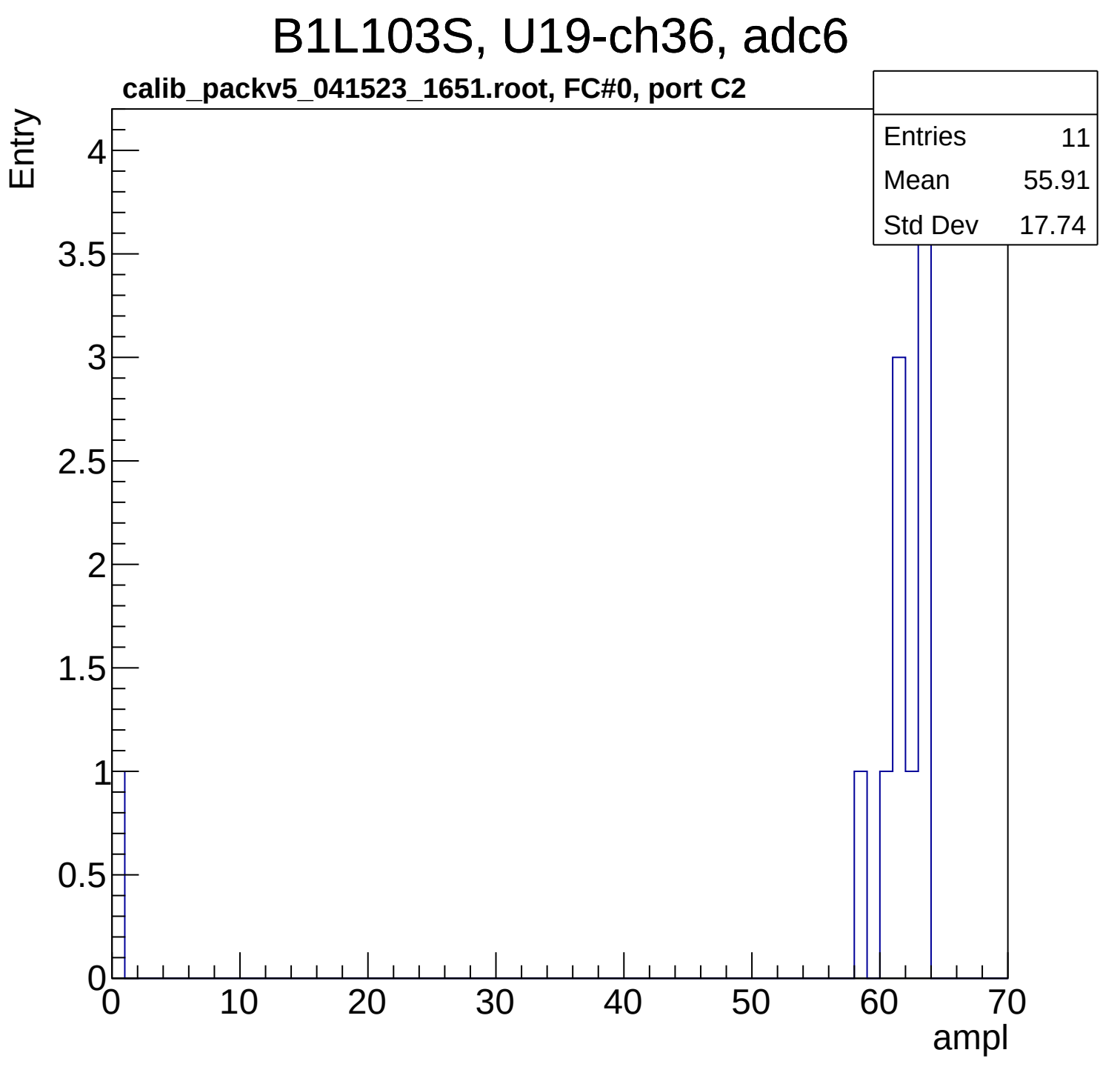

B1L103S, U19-ch36, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 33.42
Std Dev 10.57
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch36, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 39.2
Std Dev 12.29
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch36, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 48.87
Std Dev 3.329
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch36, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 54.15
Std Dev 3.86
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U19-ch36, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 58.05
Std Dev 8.2
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch36, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 55.91
Std Dev 17.74
Entry
ampl
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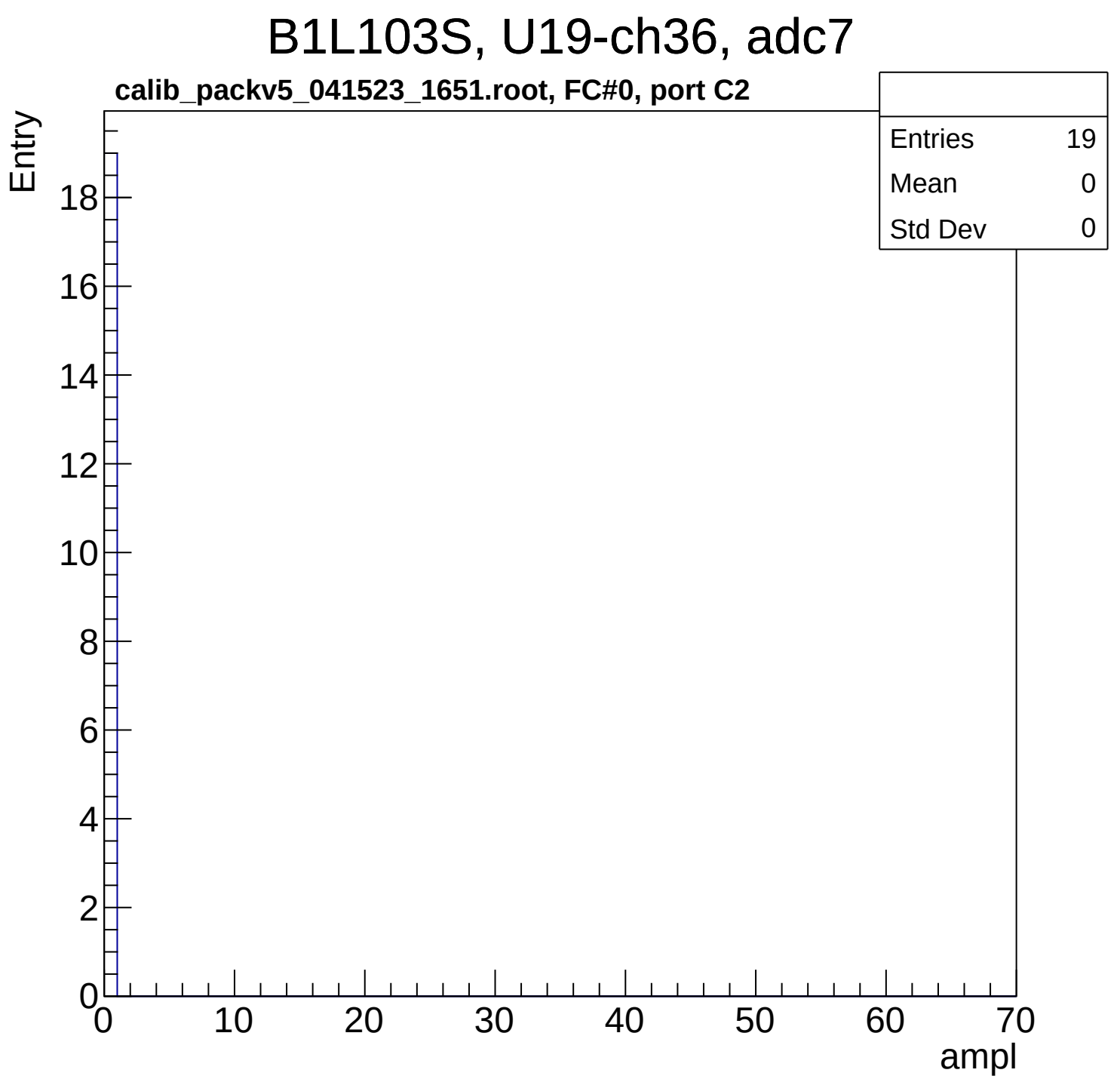
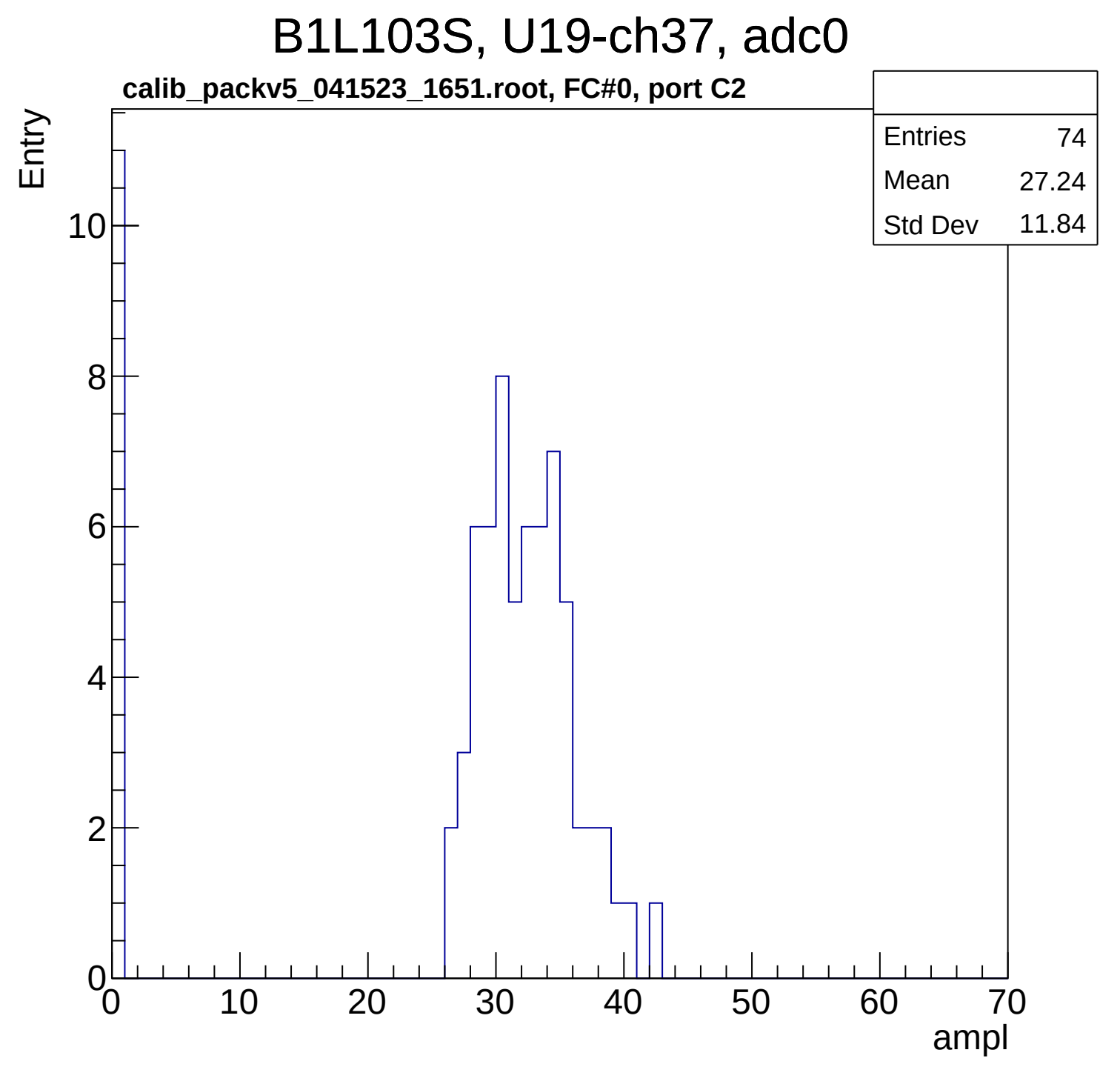
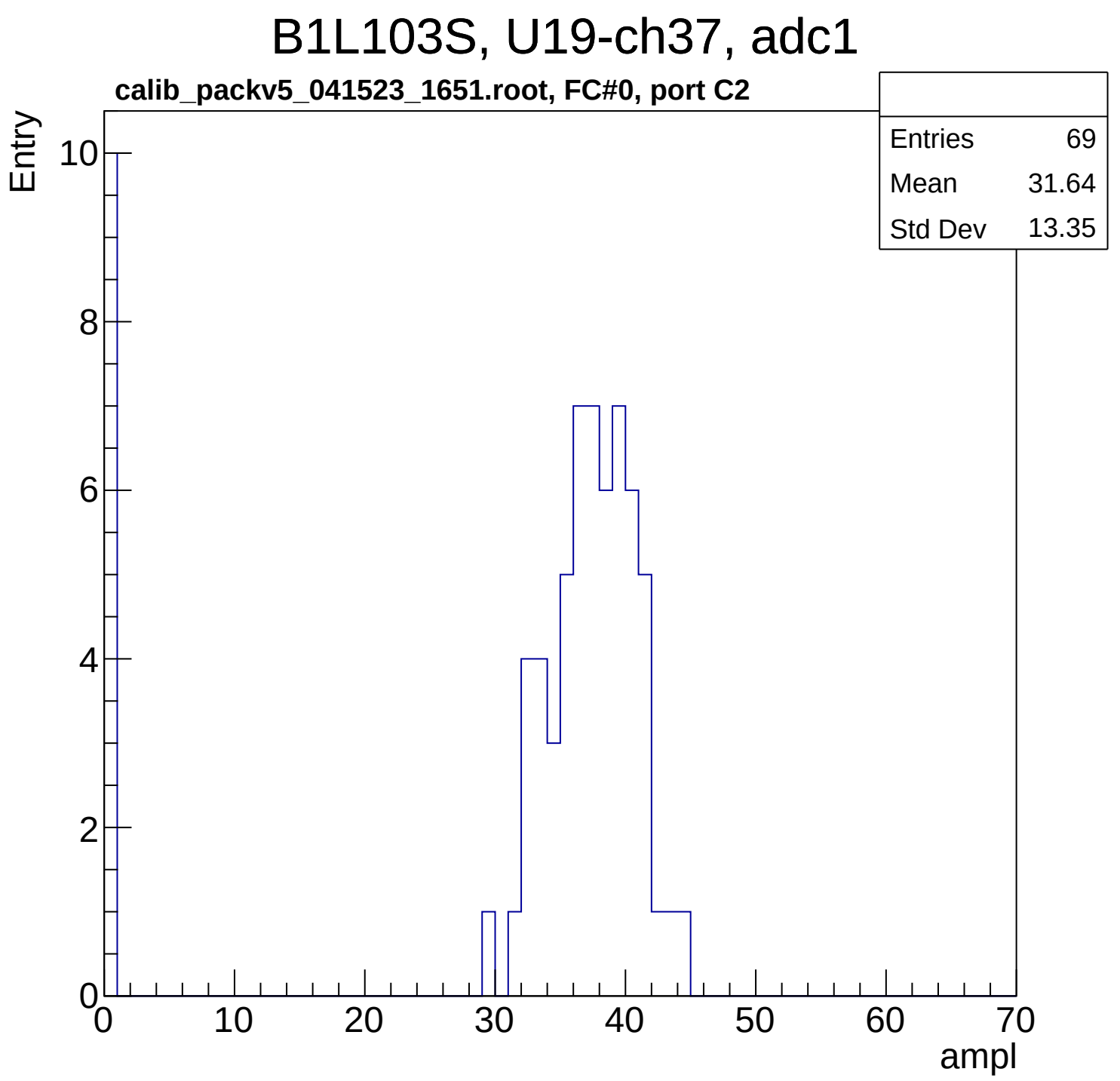
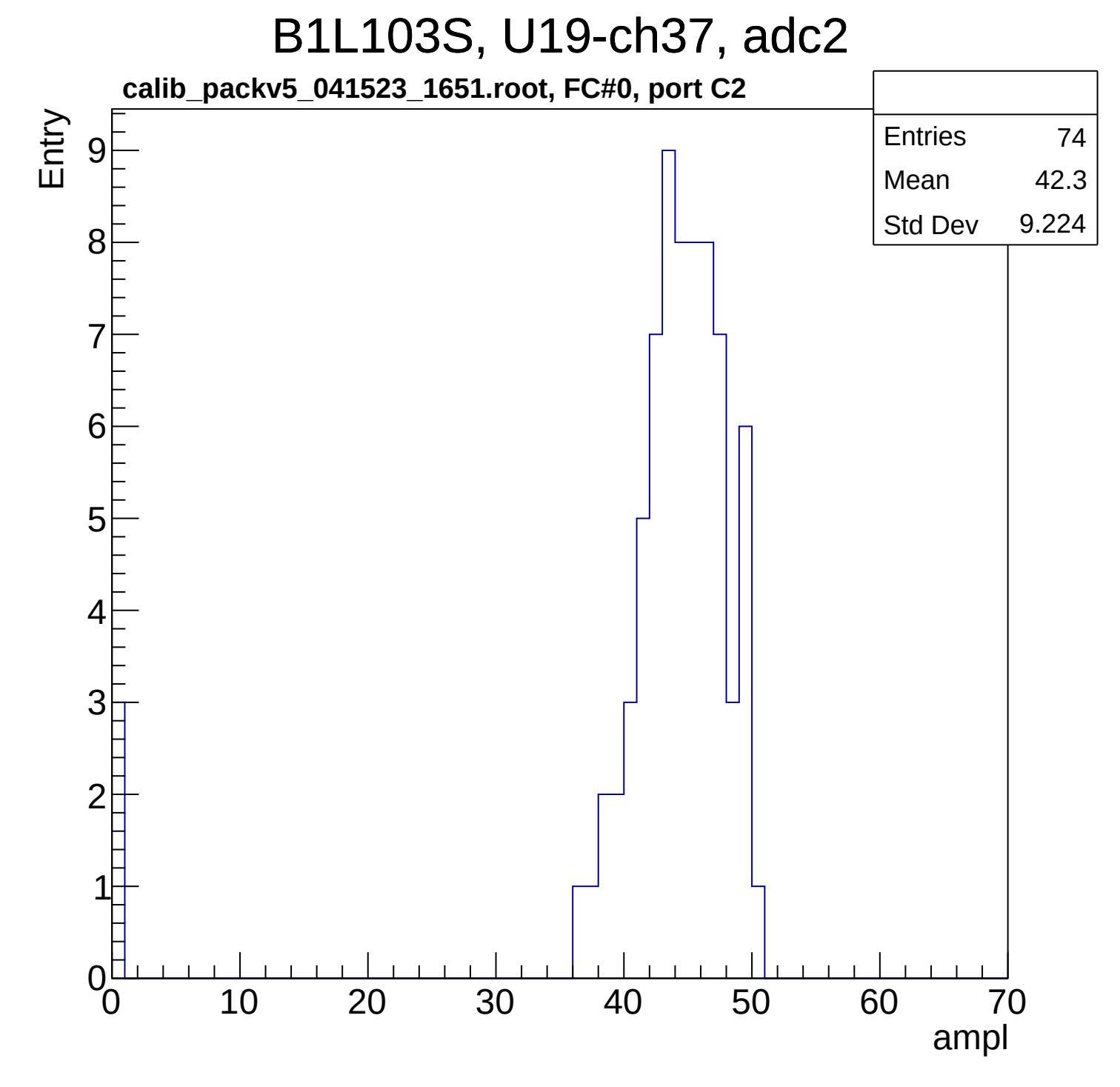
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U19-ch36, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch37, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 27.24
Std Dev 11.84
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch37, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 31.64
Std Dev 13.35
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch37, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 42.3
Std Dev 9.224
Entry
ampl
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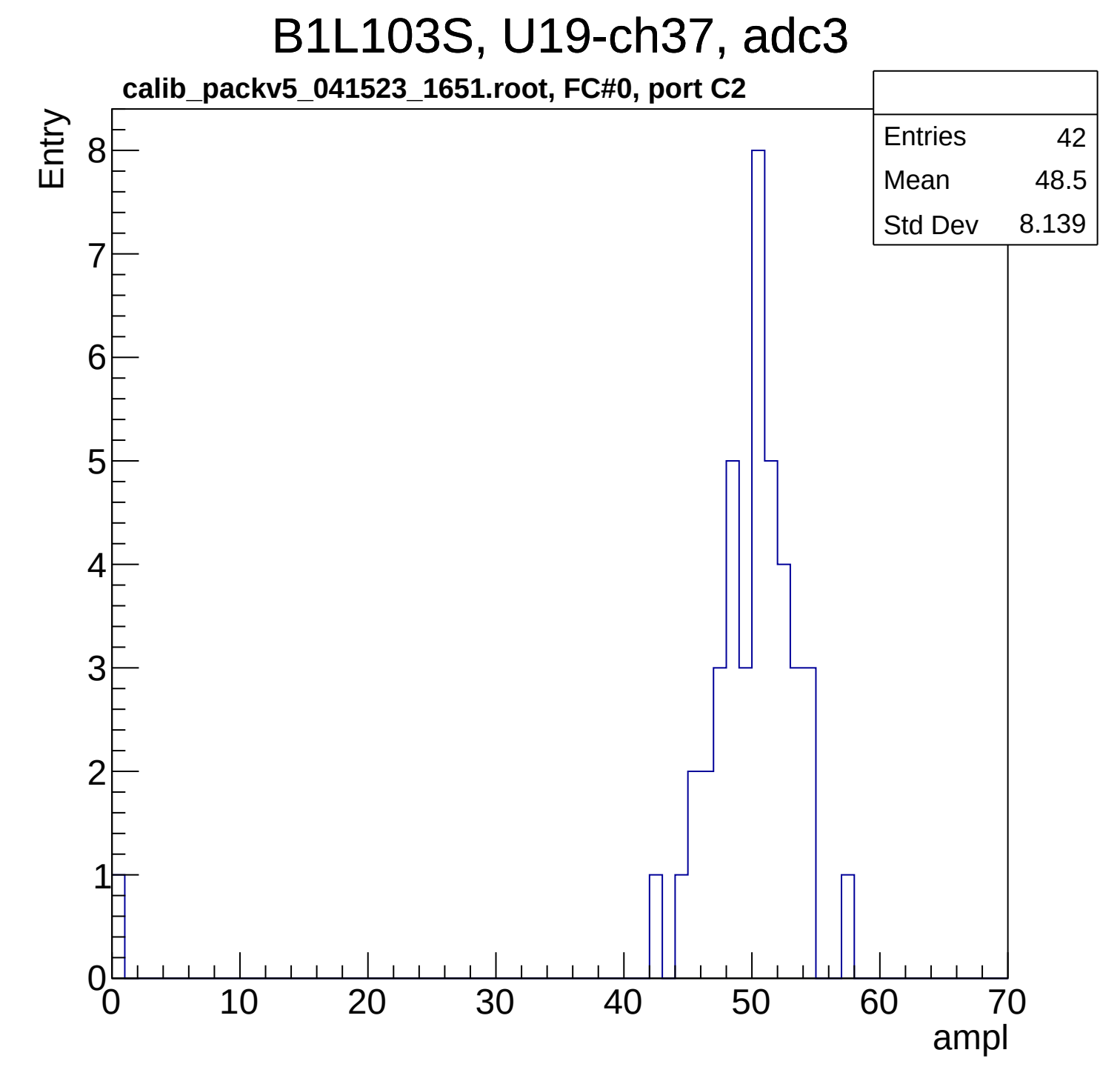
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch37, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 48.5
Std Dev 8.139
Entry
ampl
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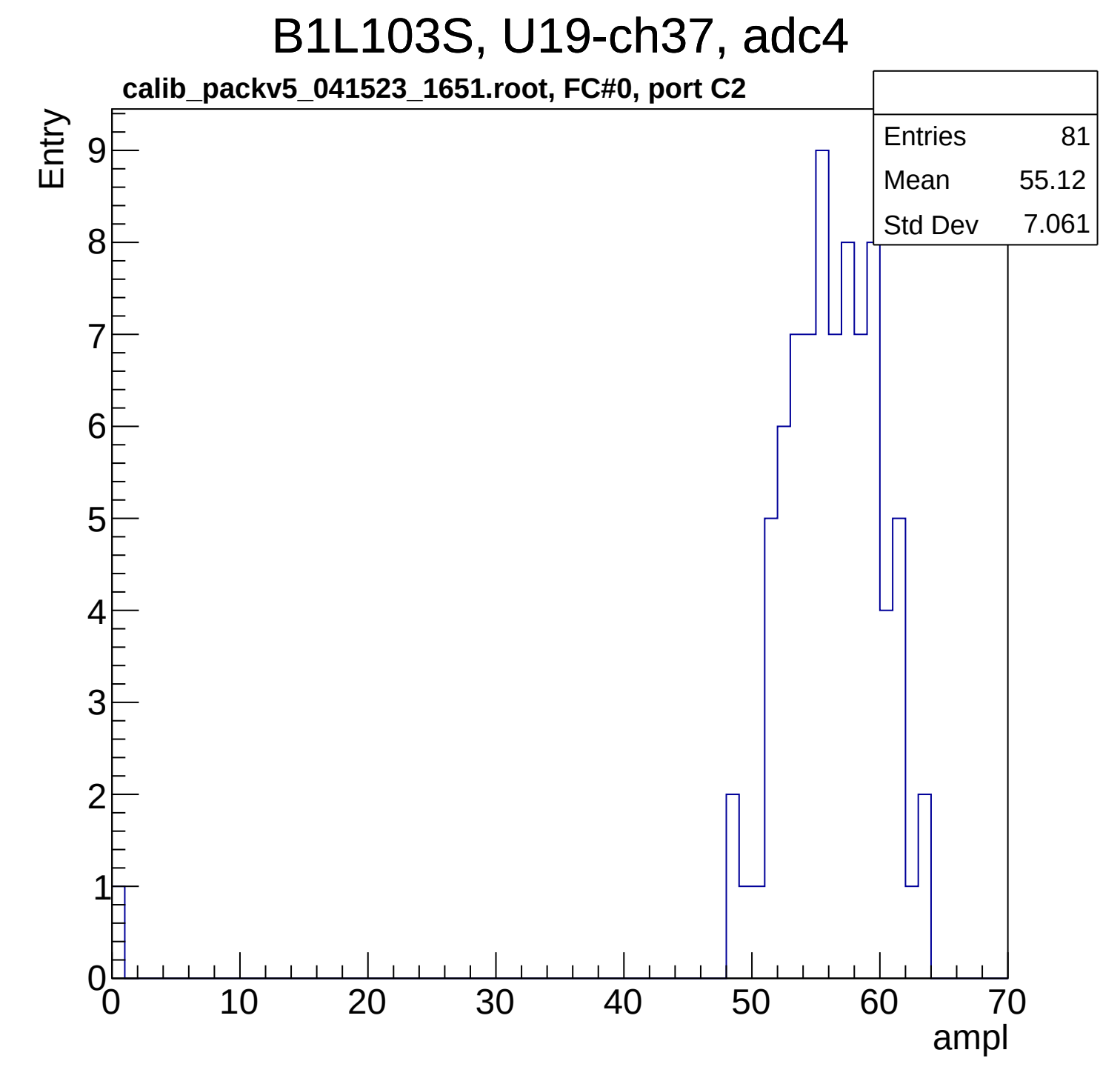
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch37, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 55.12
Std Dev 7.061
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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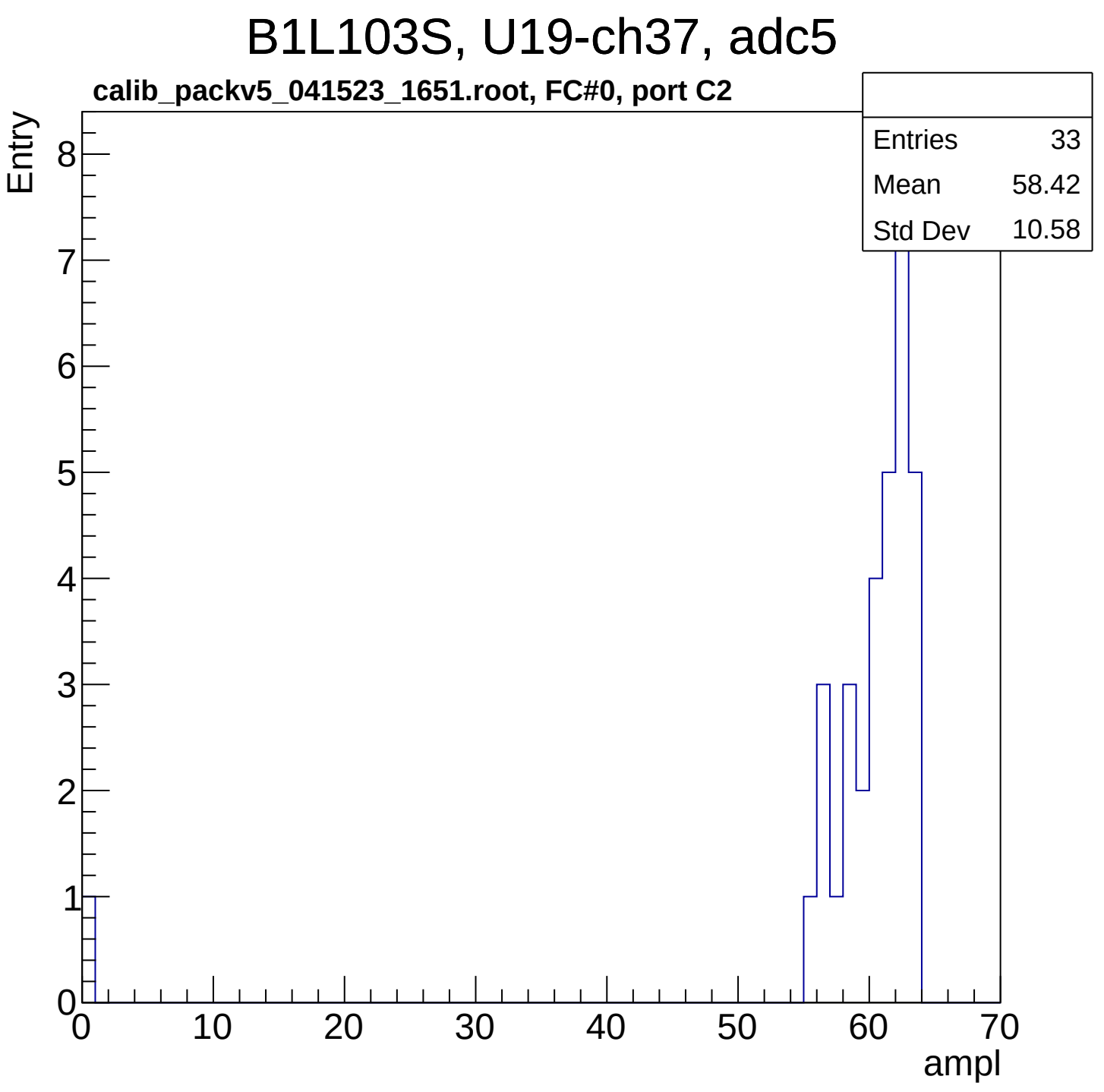
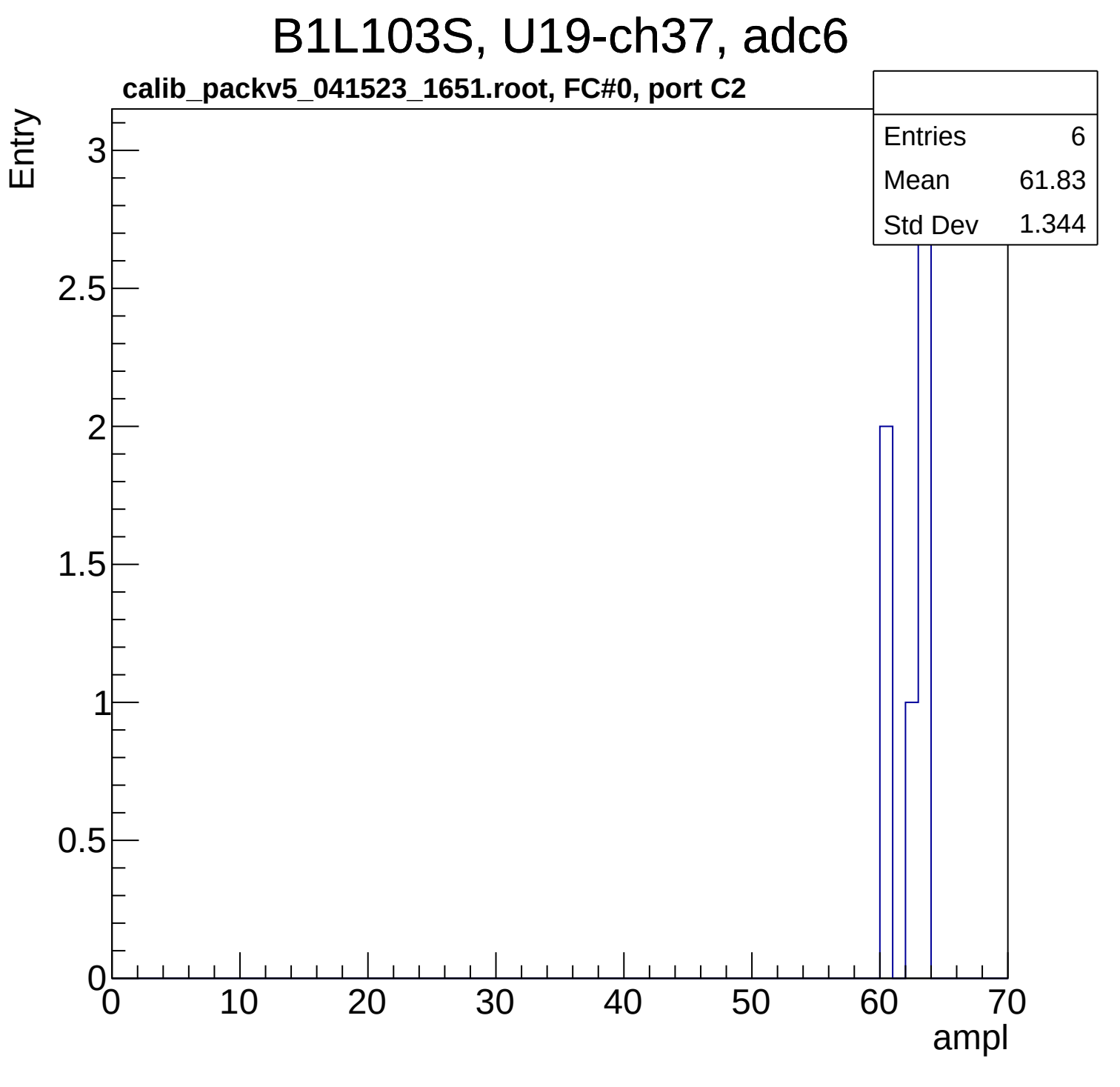

B1L103S, U19-ch37, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 58.42
Std Dev 10.58
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch37, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 61.83
Std Dev 1.344
Entry
ampl
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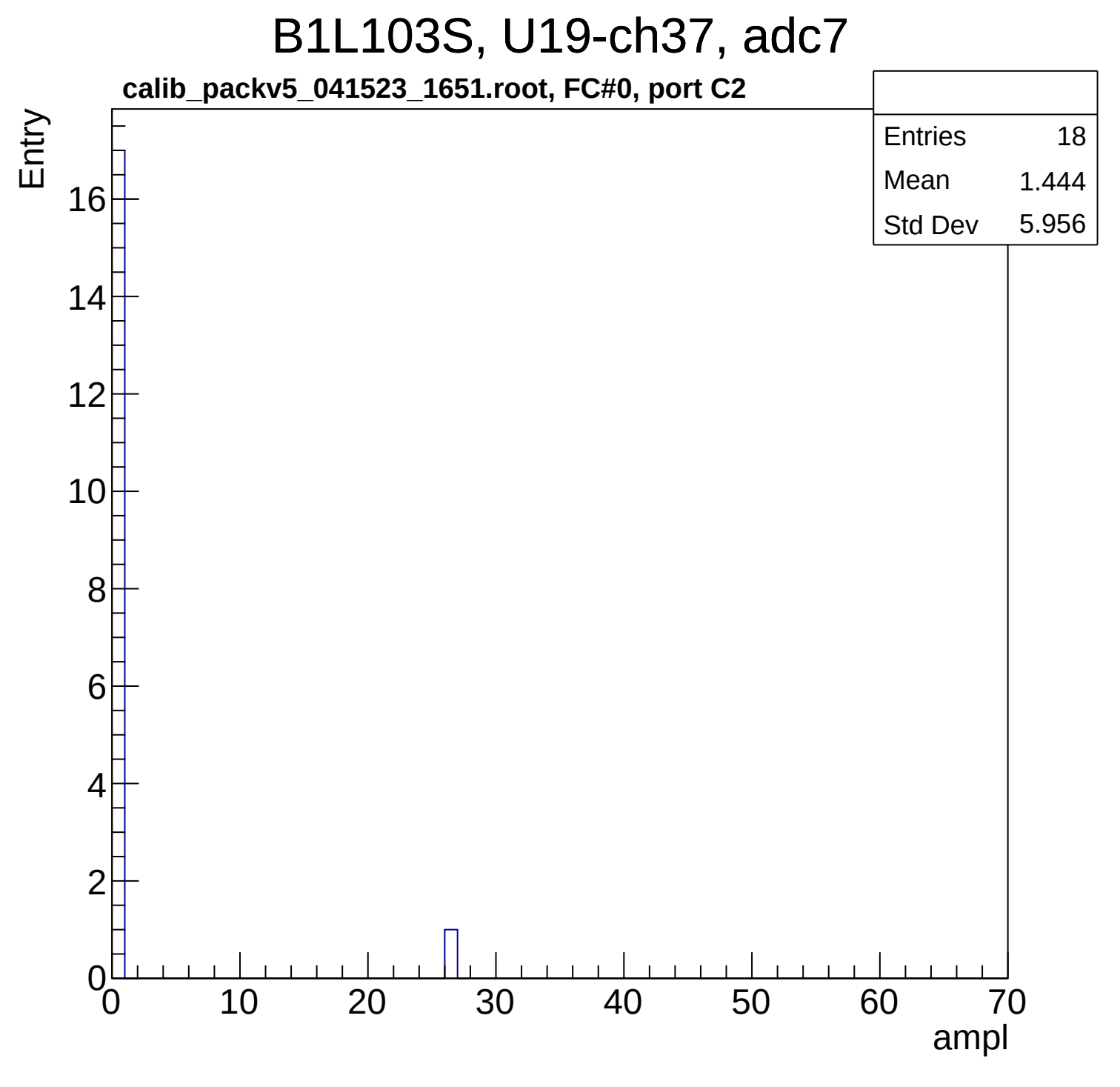
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U19-ch37, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.444
Std Dev 5.956
Entry
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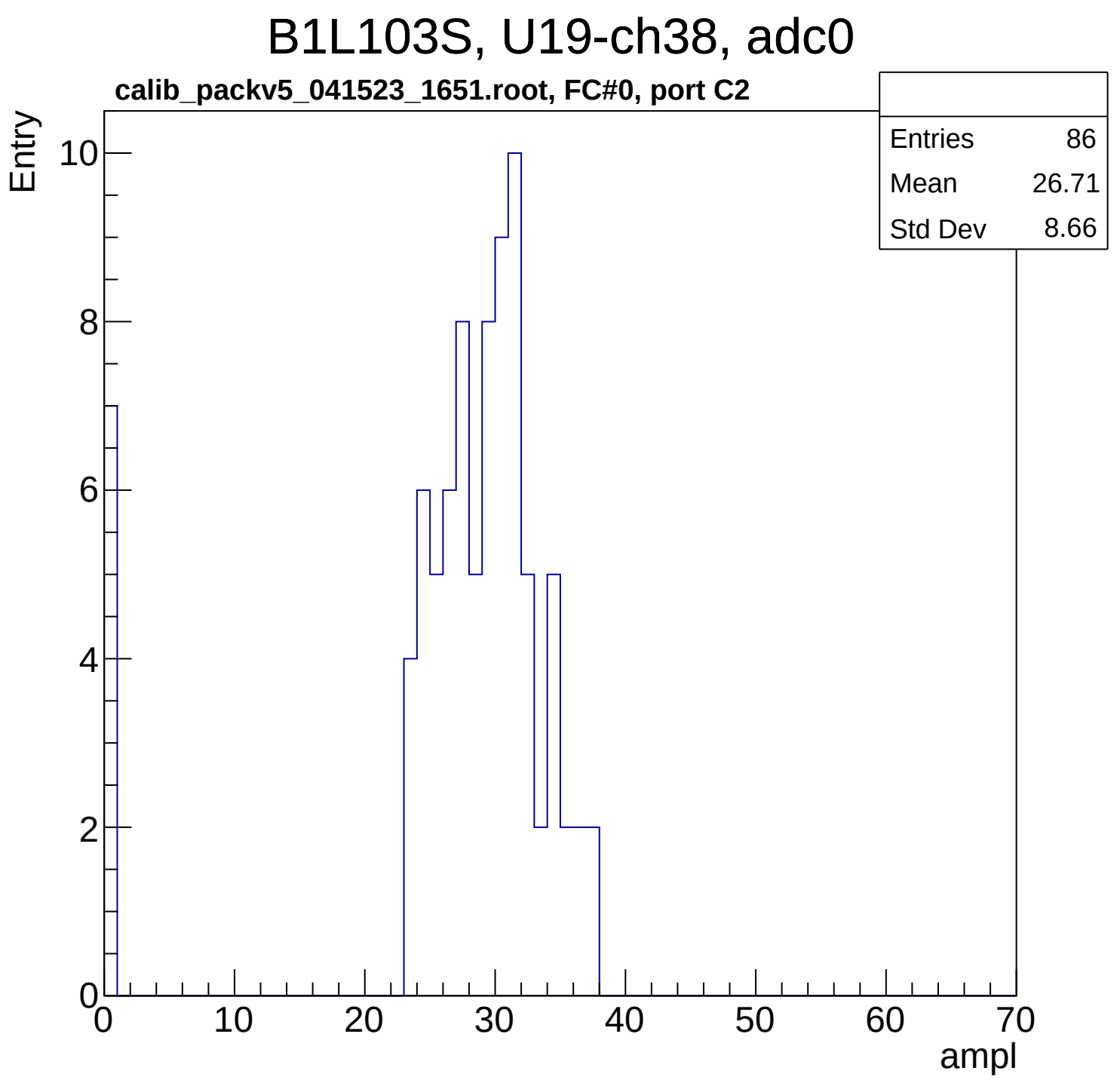
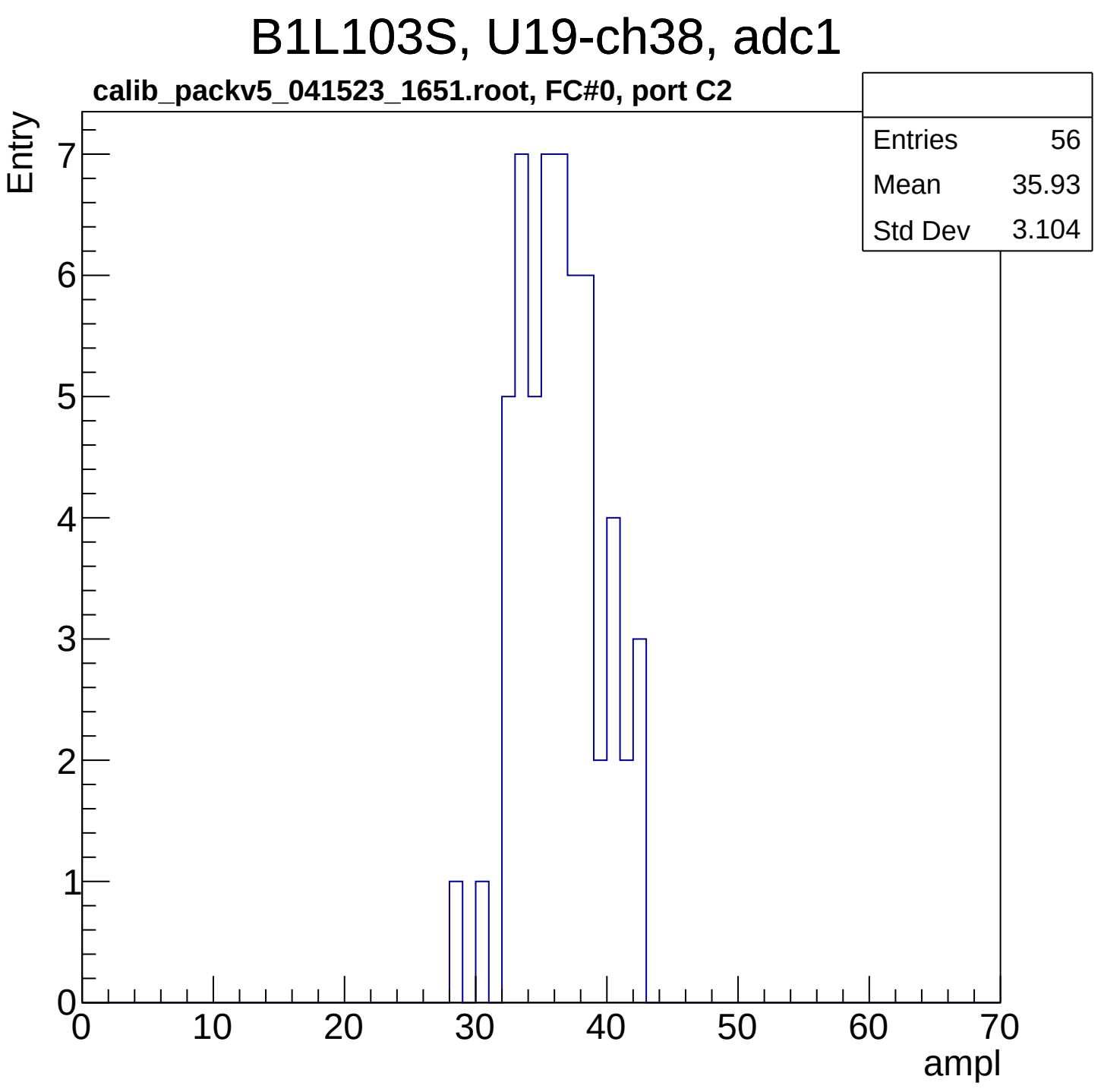
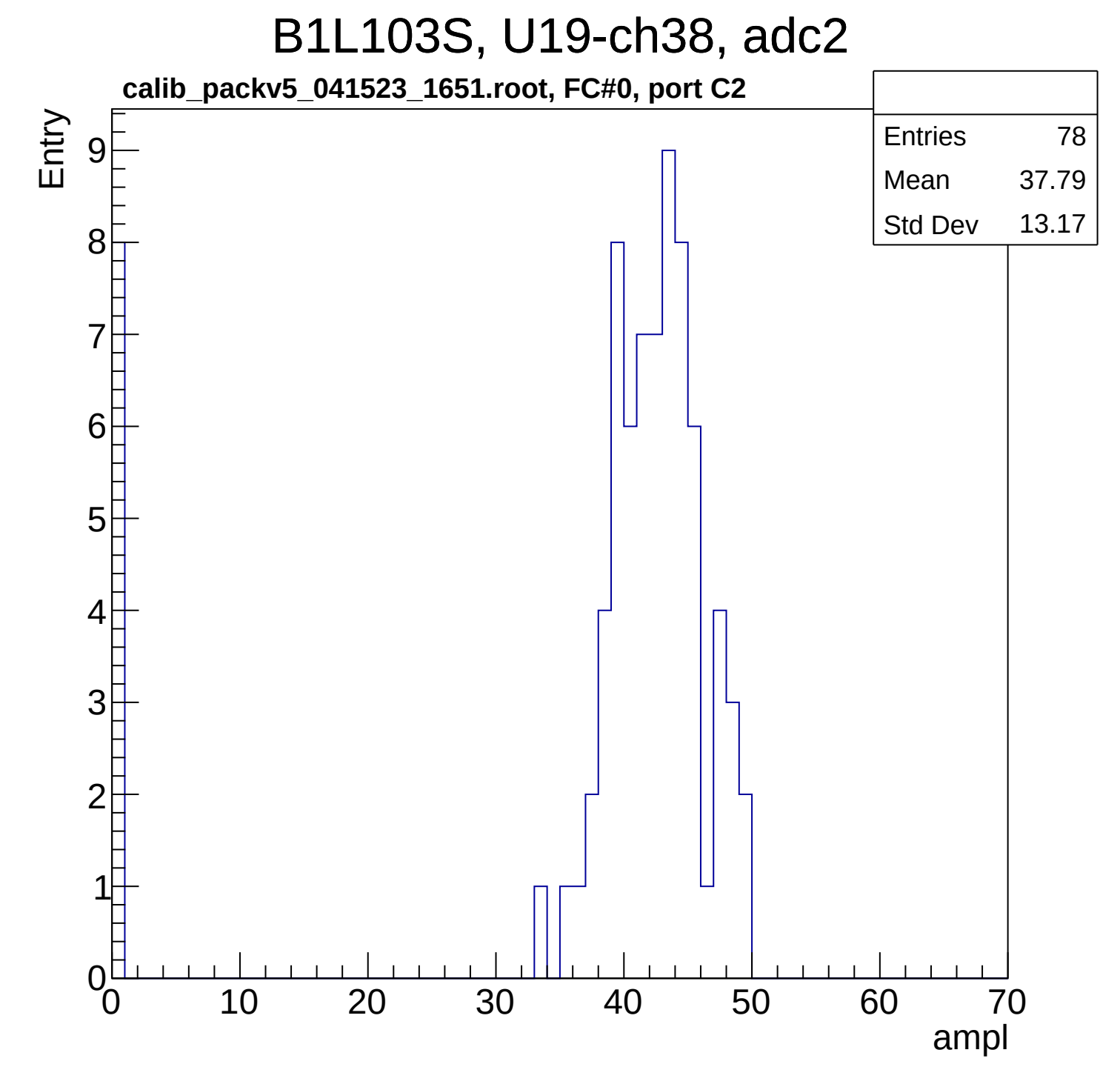
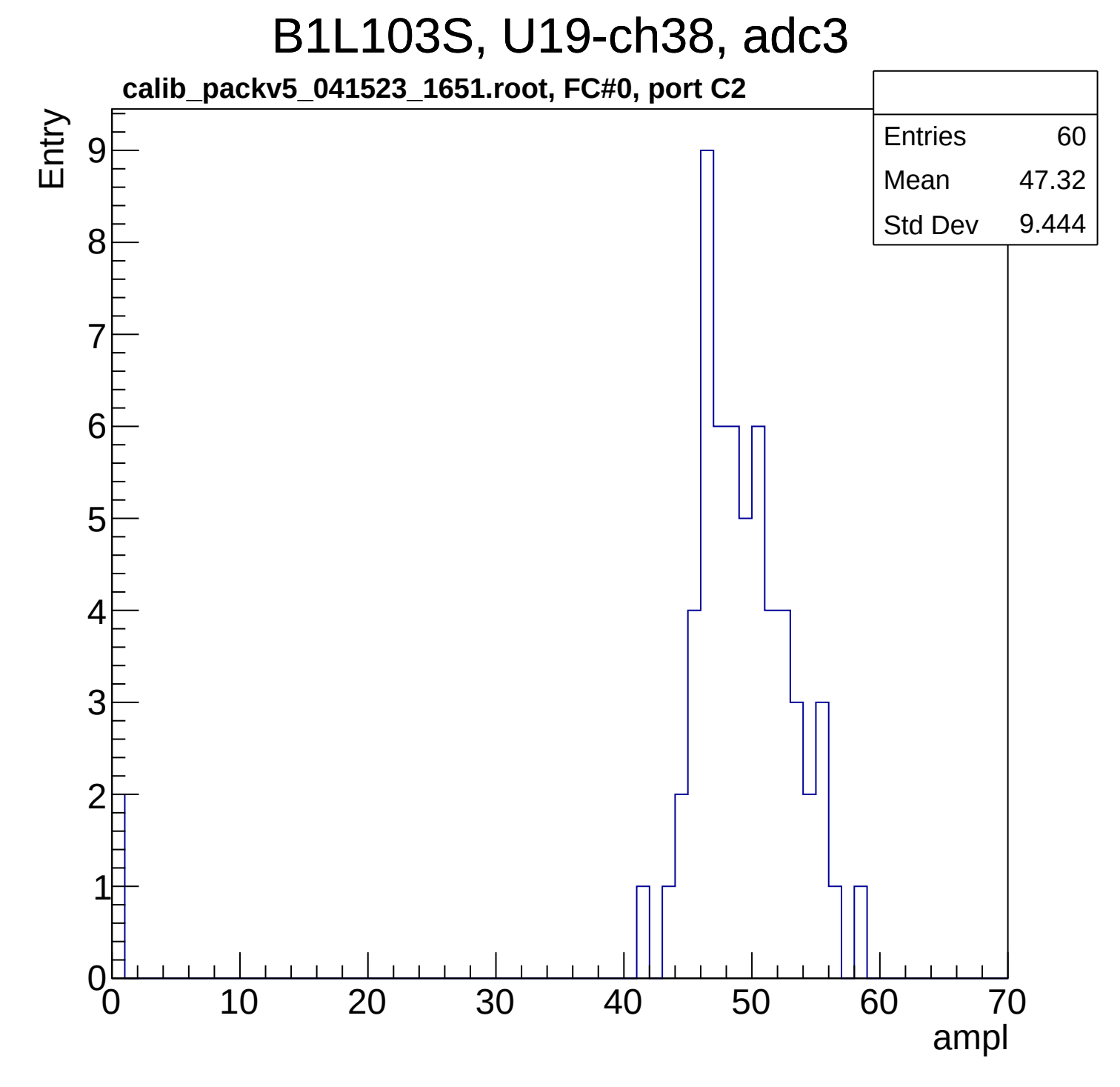
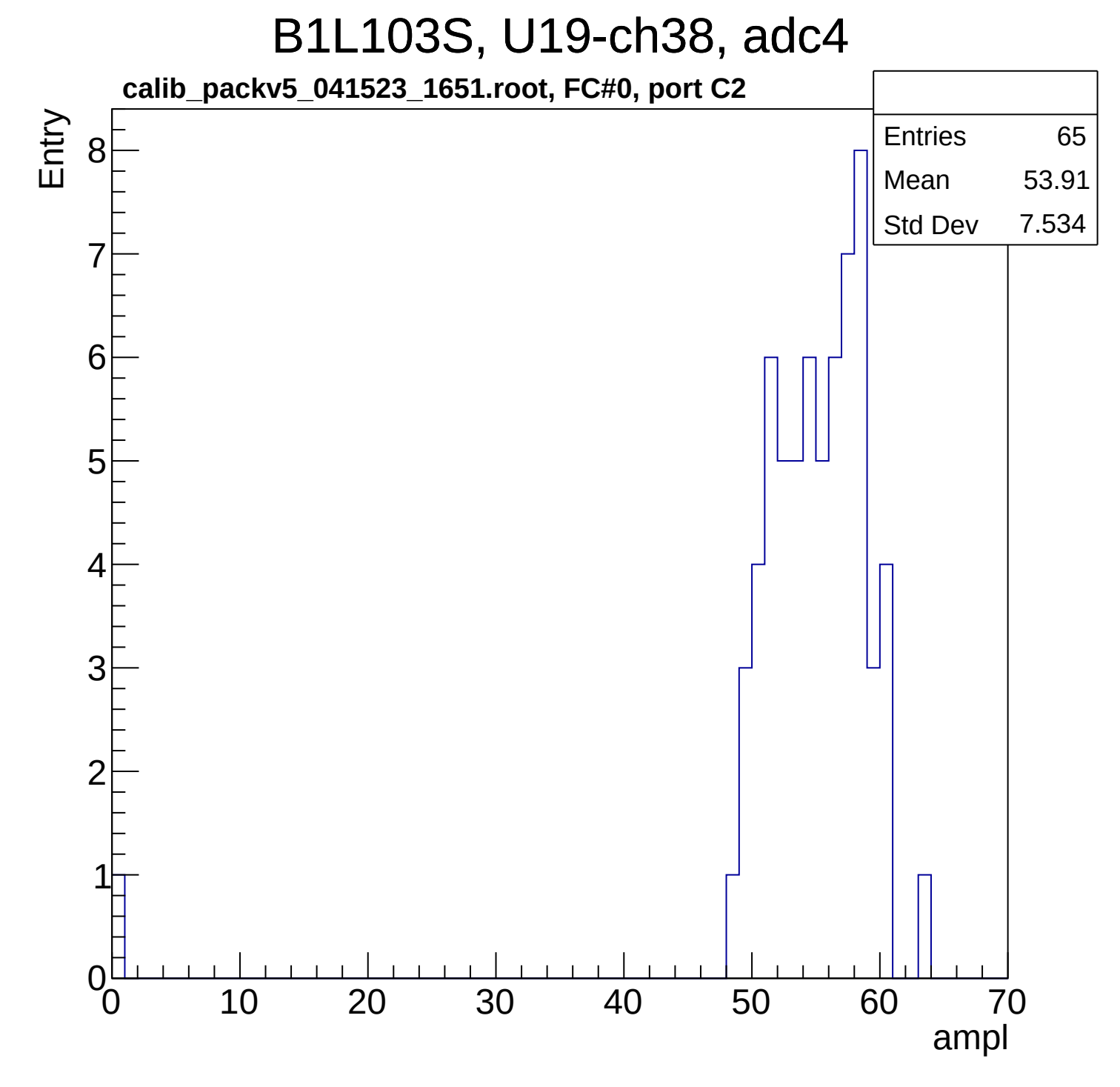
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

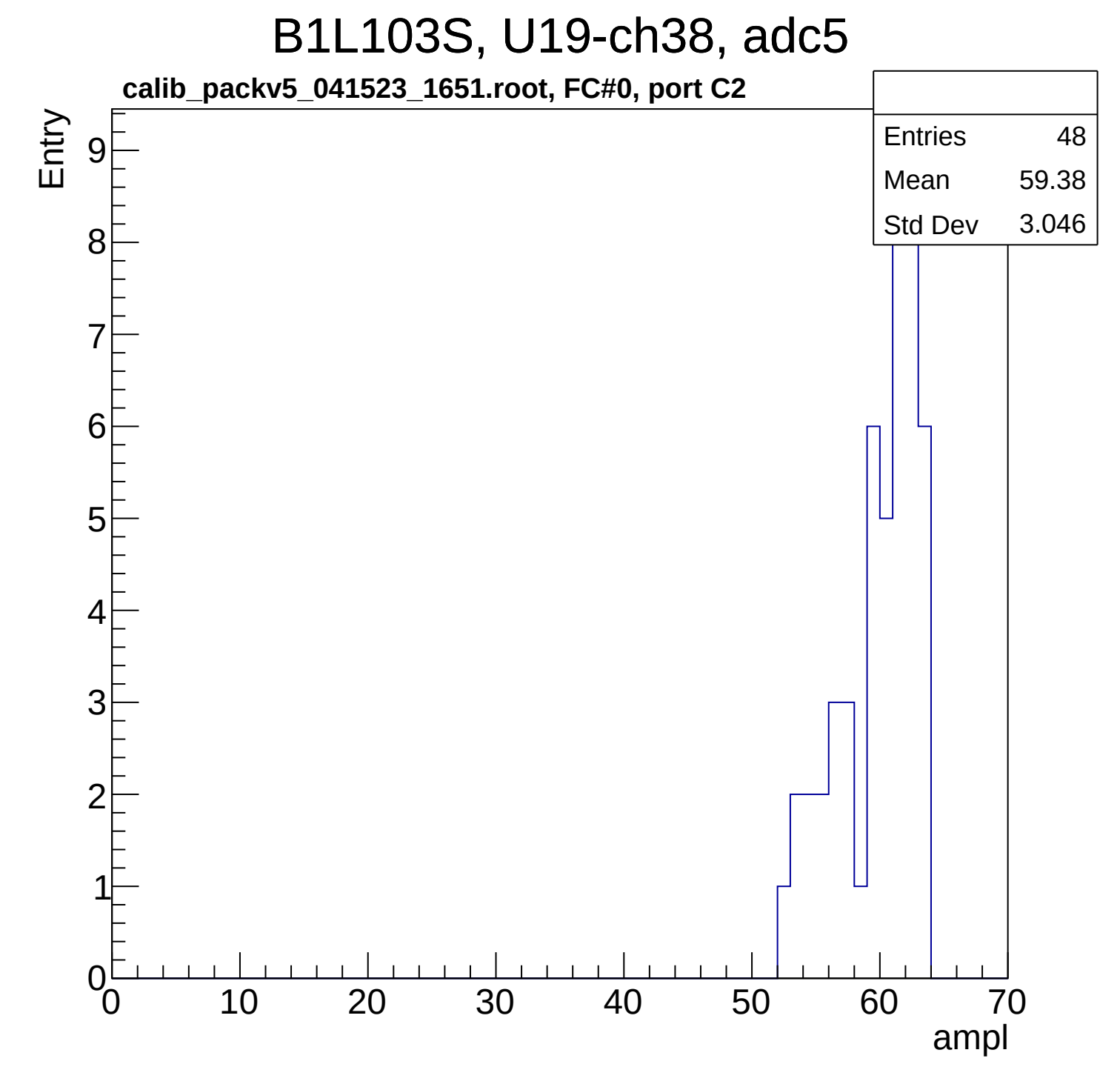

B1L103S, U19-ch38, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 26.71
Std Dev 8.66
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

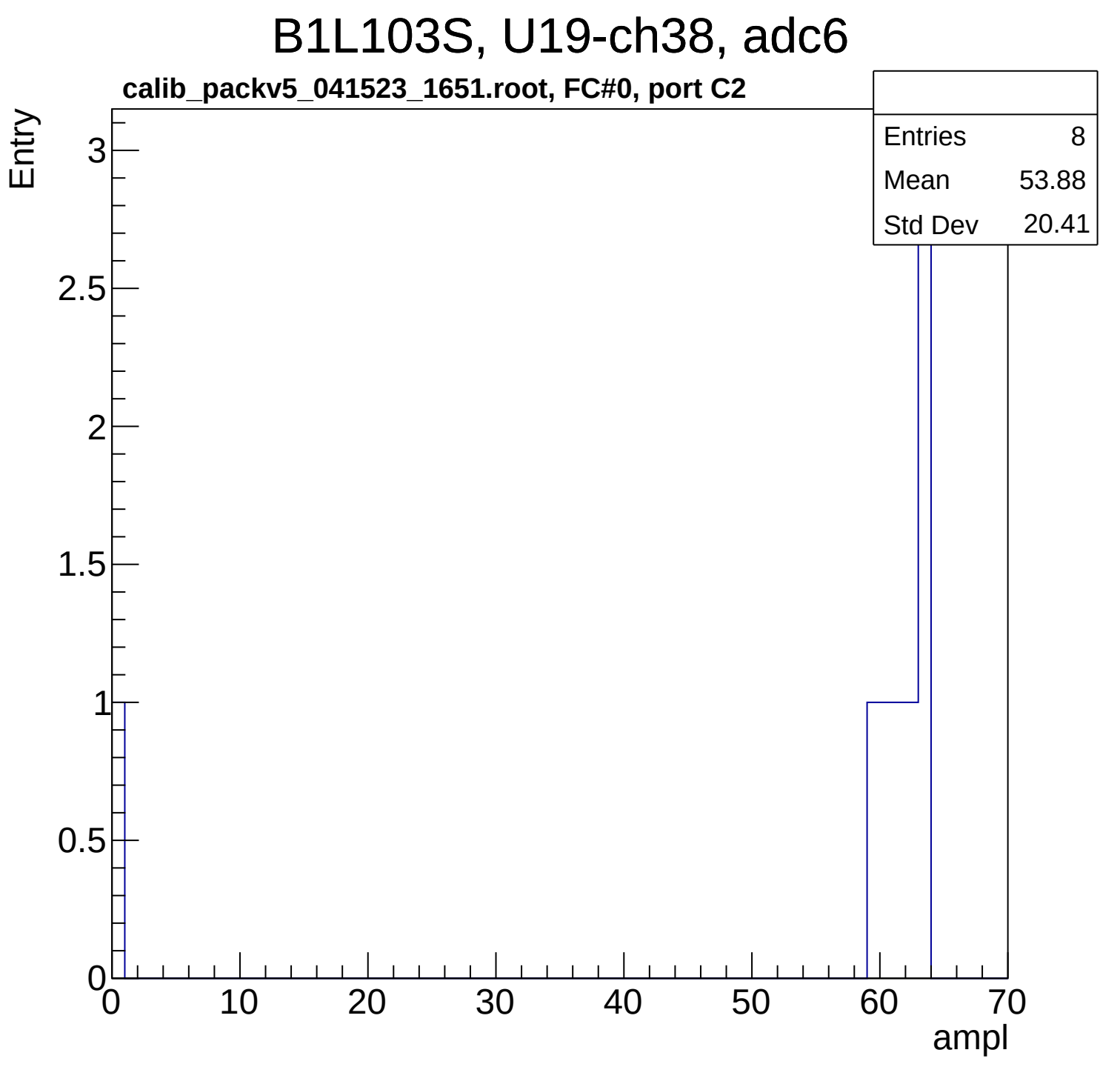

B1L103S, U19-ch38, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 35.93
Std Dev 3.104
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch38, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 37.79
Std Dev 13.17
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch38, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 47.32
Std Dev 9.444
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch38, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 53.91
Std Dev 7.534
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch38, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 59.38
Std Dev 3.046
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch38, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 53.88
Std Dev 20.41
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
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20
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40
50
60
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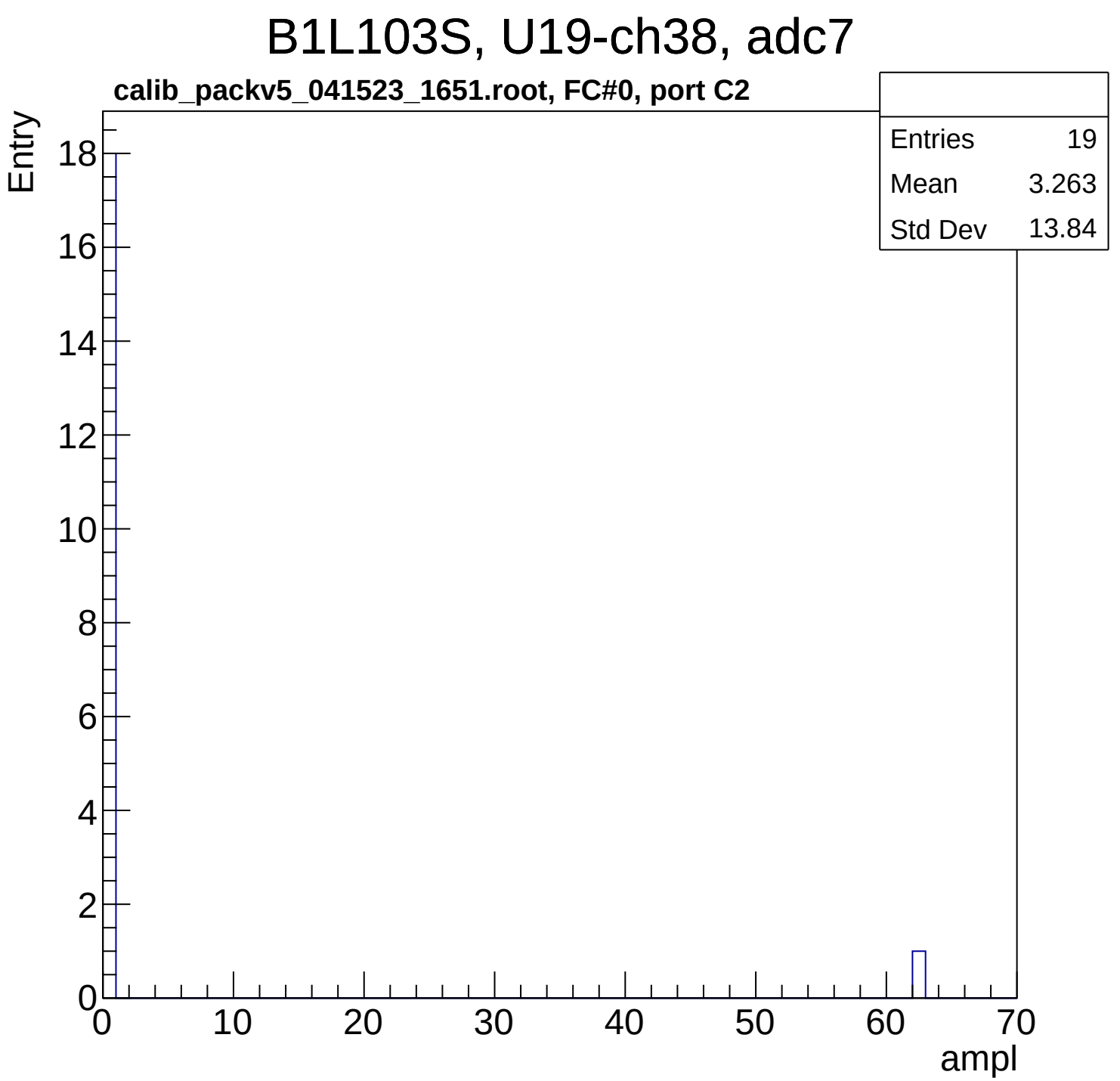
B1L103S, U19-ch38, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.263
Std Dev 13.84
Entry
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6
8
10
12
14
16
18
0
10
20
30
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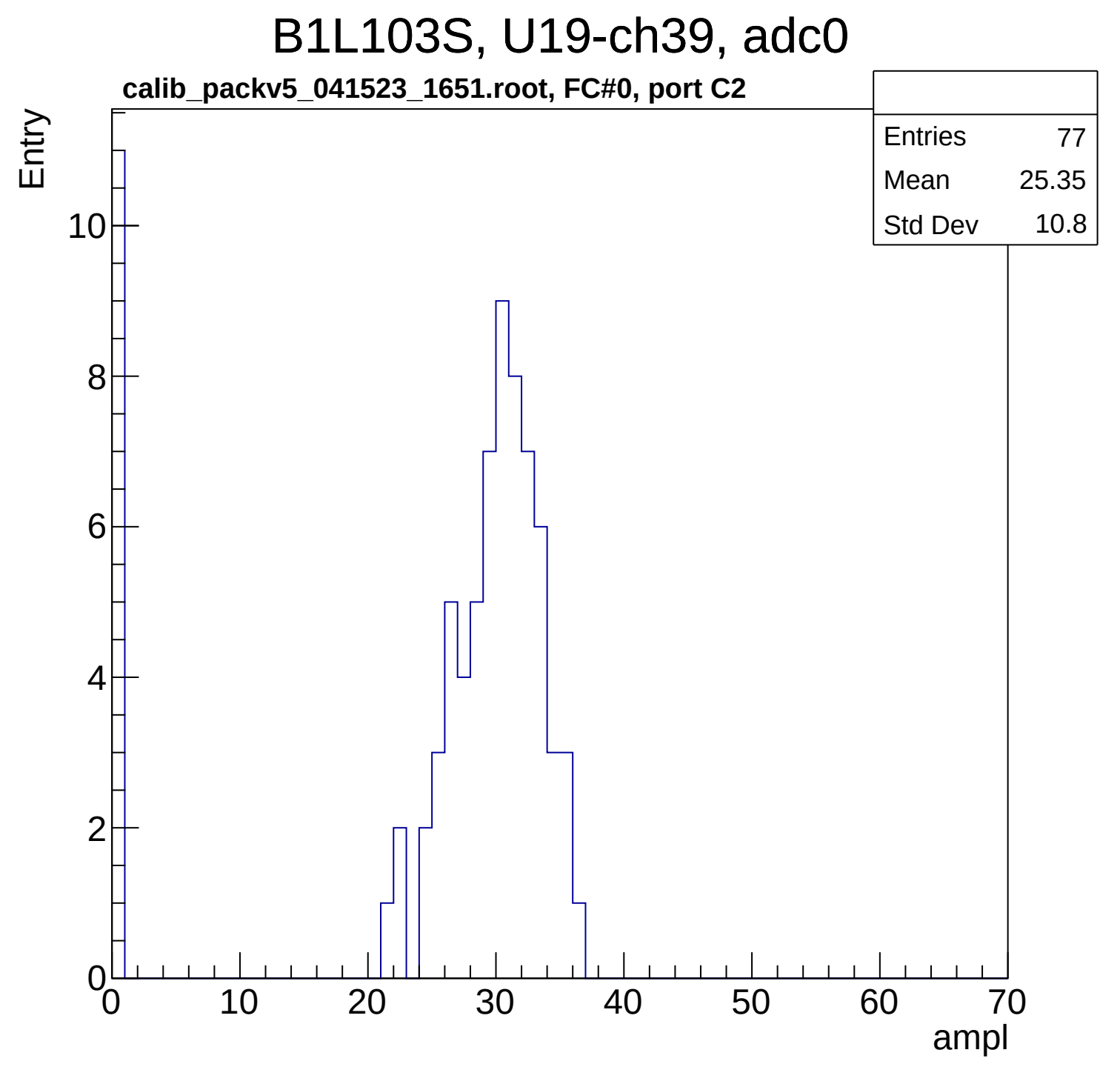
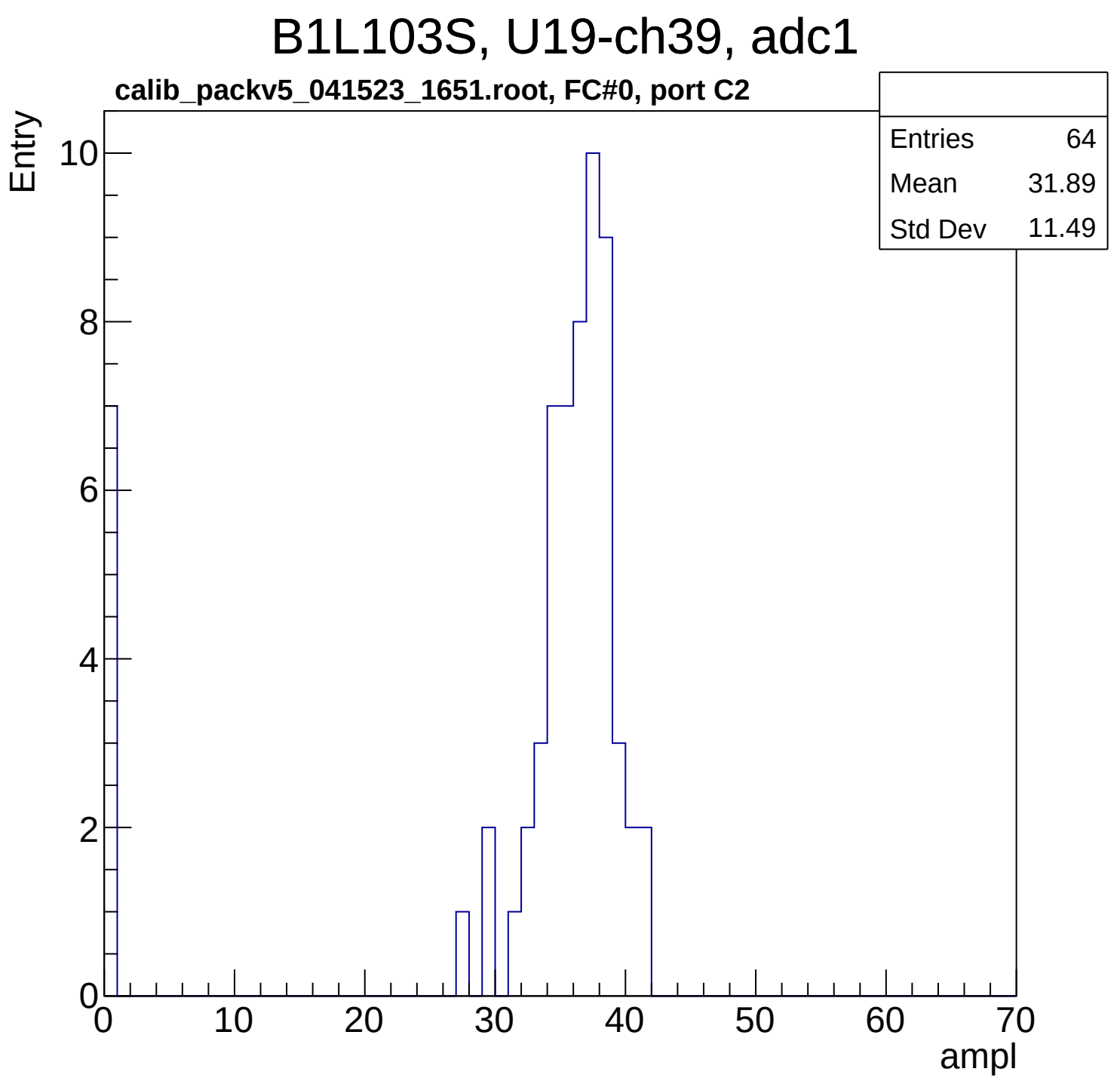
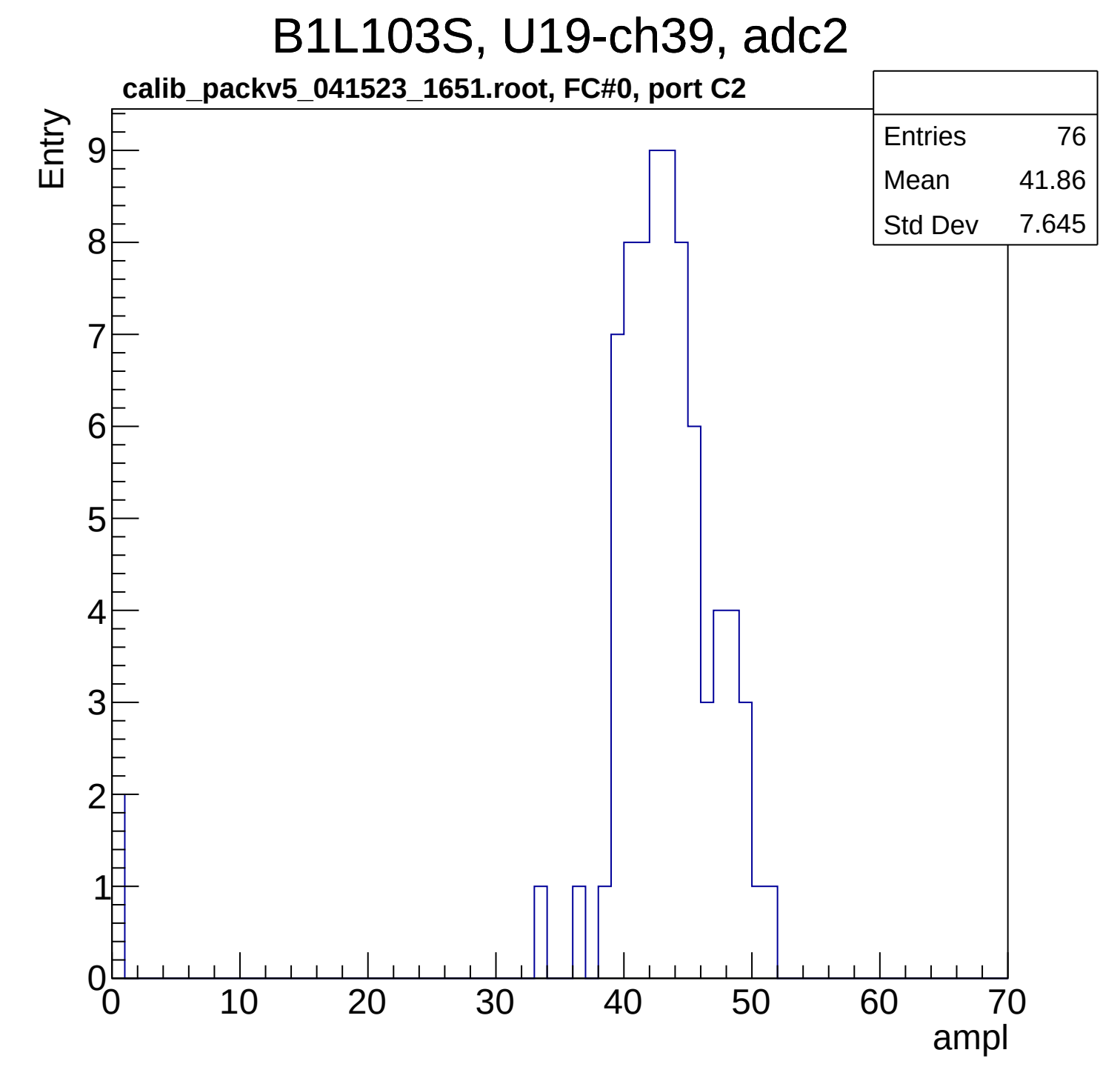
50
60
70
ampl


B1L103S, U19-ch39, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 25.35
Std Dev 10.8
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch39, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 31.89
Std Dev 11.49
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch39, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 41.86
Std Dev 7.645
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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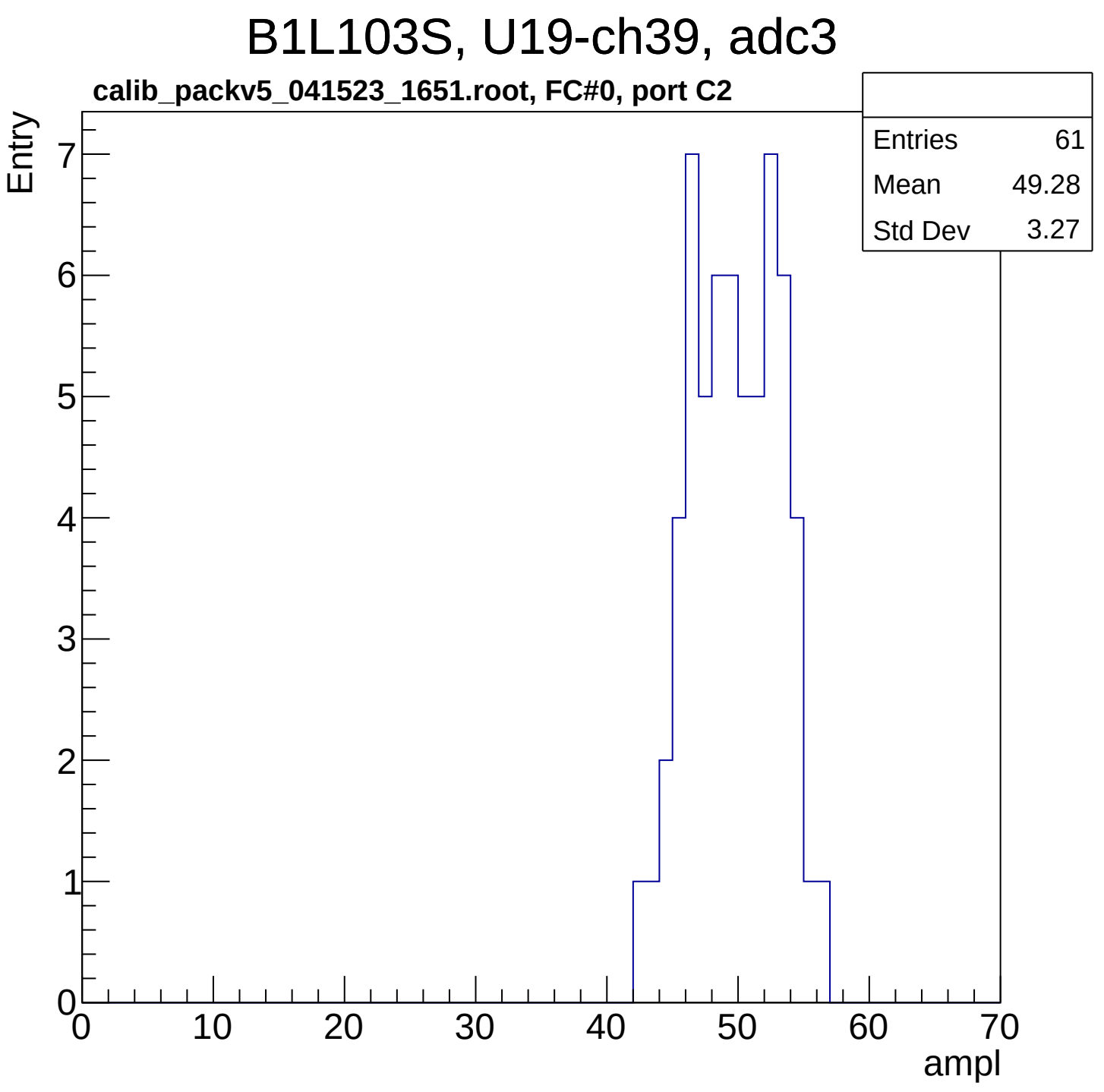
B1L103S, U19-ch39, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 49.28
Std Dev 3.27
Entry
ampl
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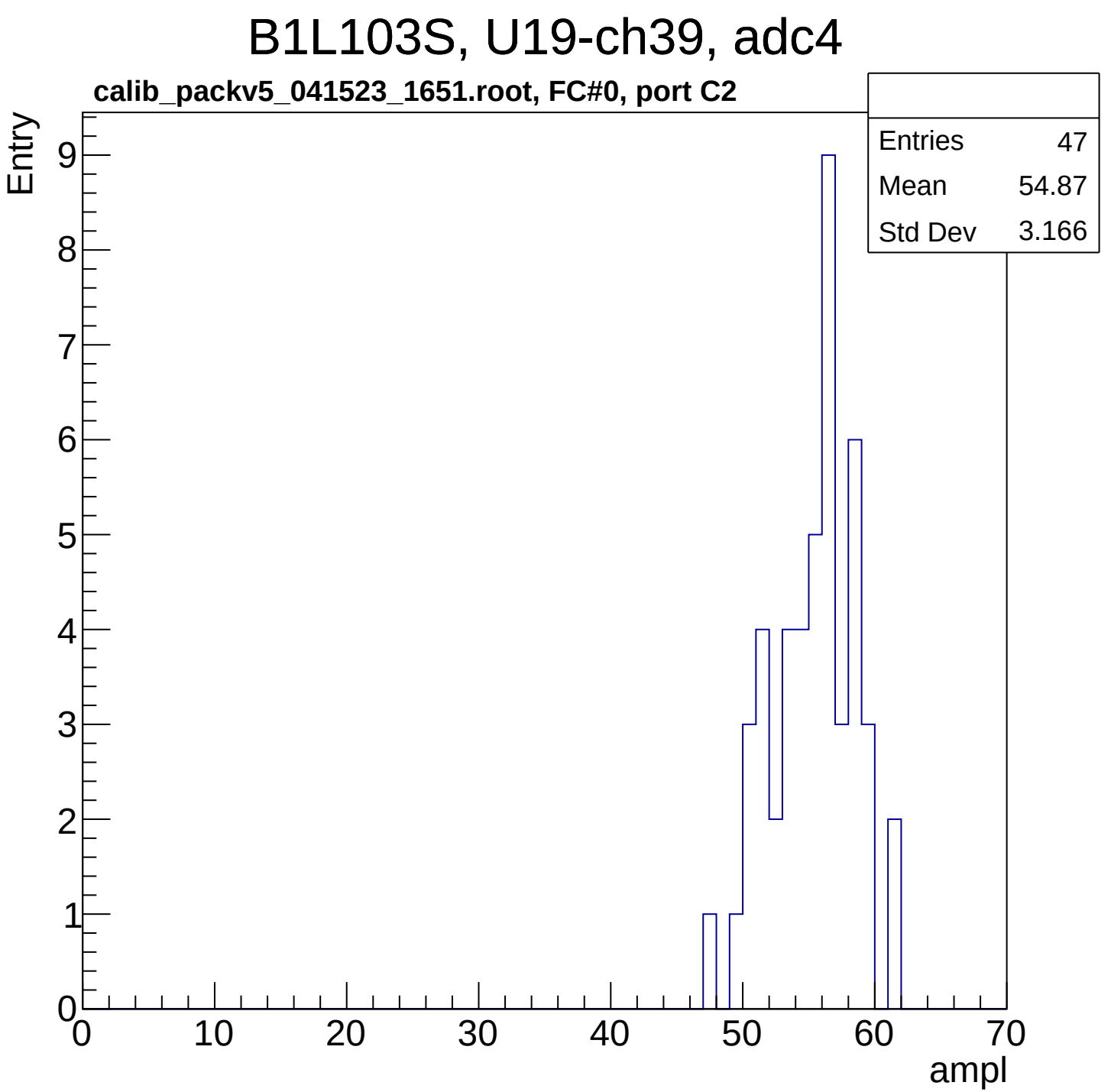
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch39, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 54.87
Std Dev 3.166
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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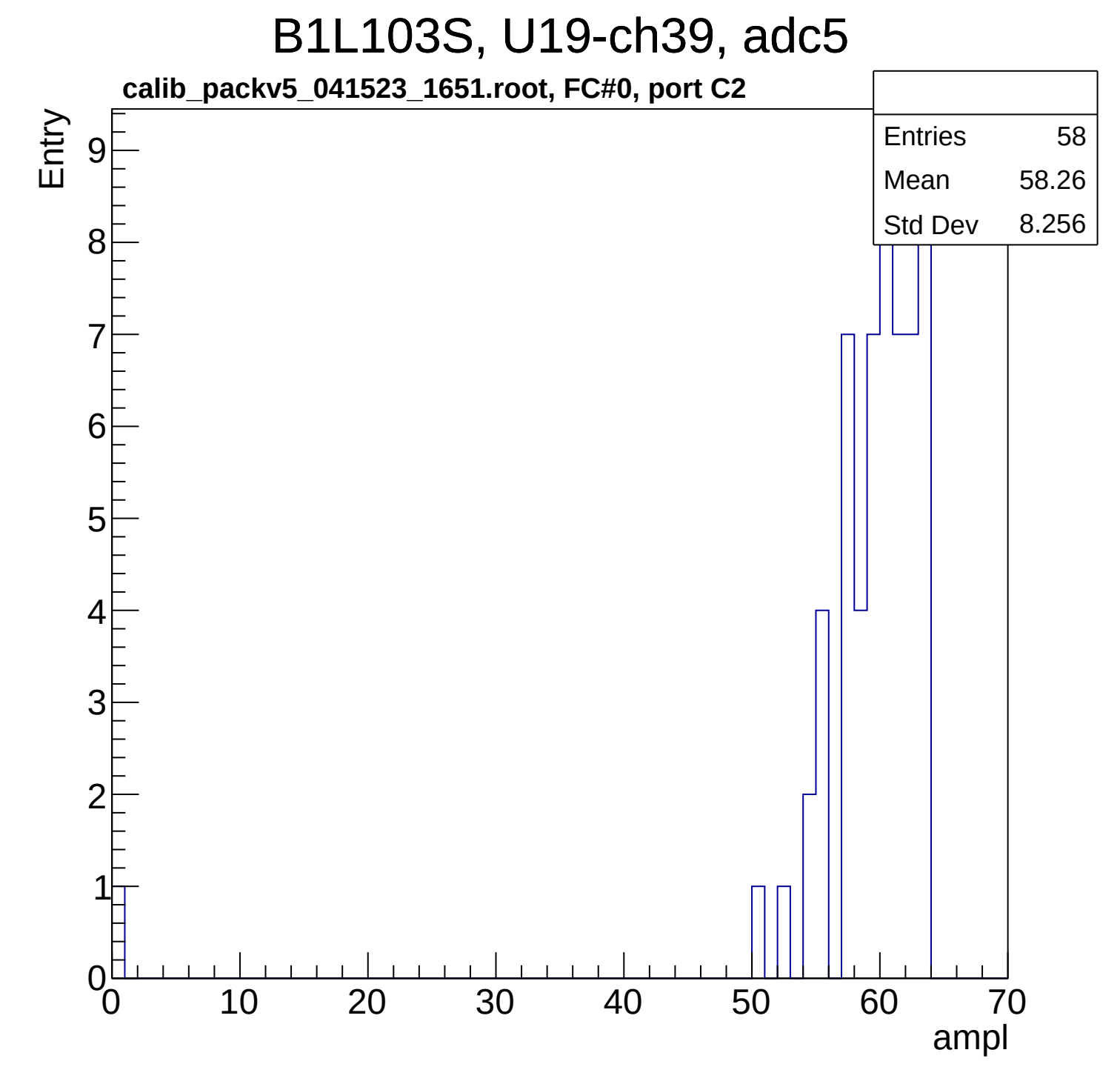
B1L103S, U19-ch39, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 58.26
Std Dev 8.256
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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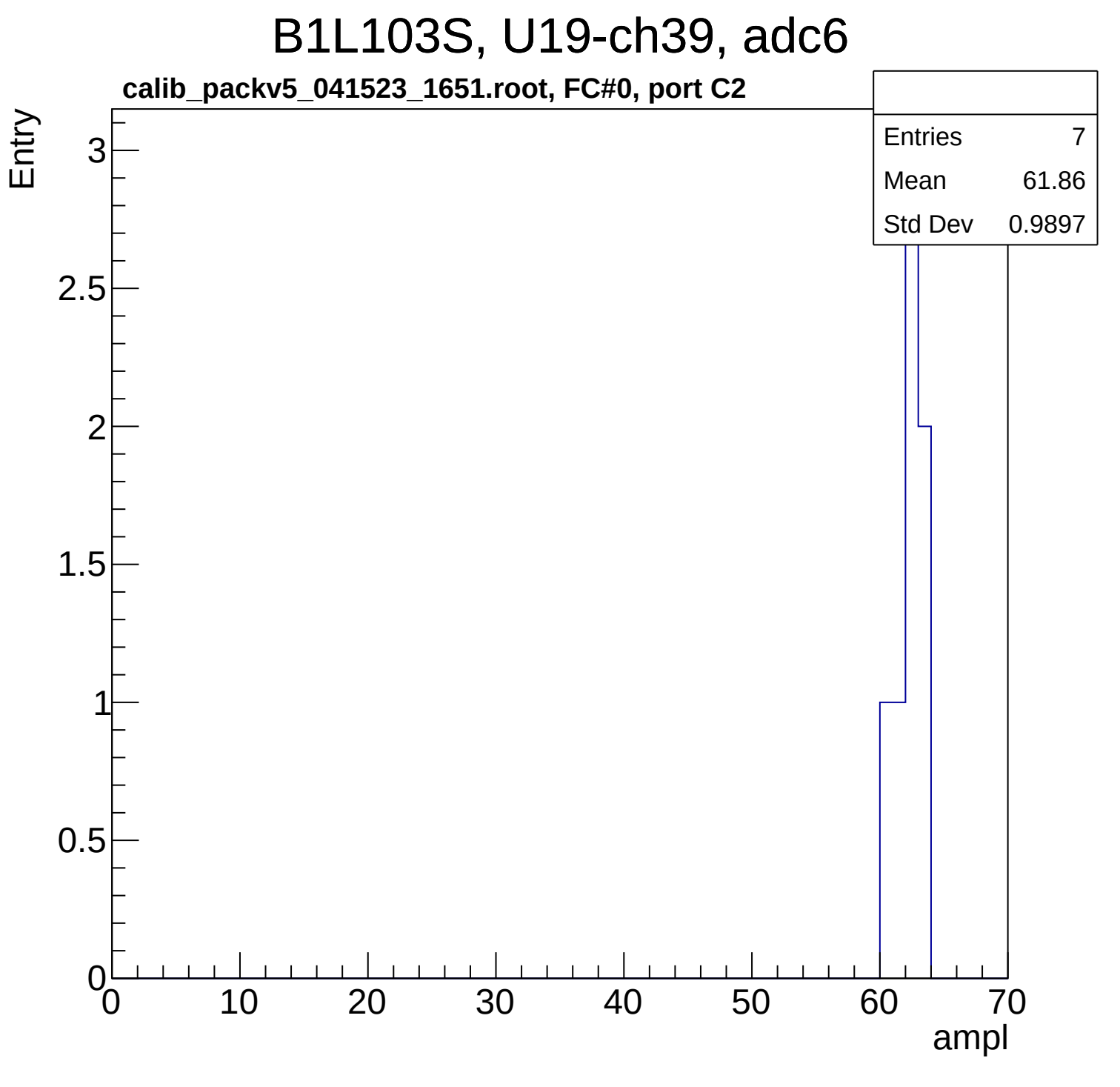
B1L103S, U19-ch39, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 61.86
Std Dev 0.9897
Entry
ampl
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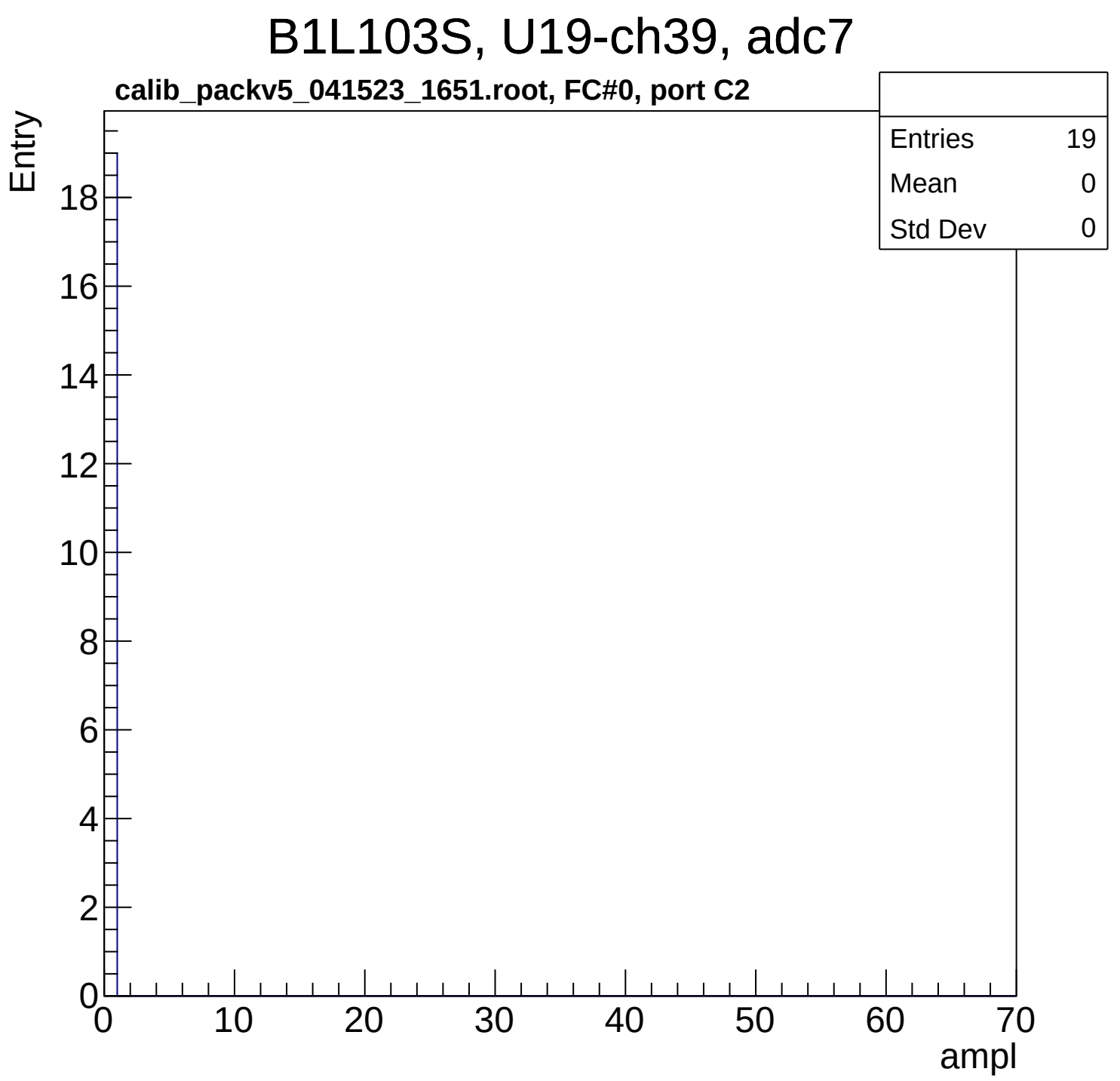
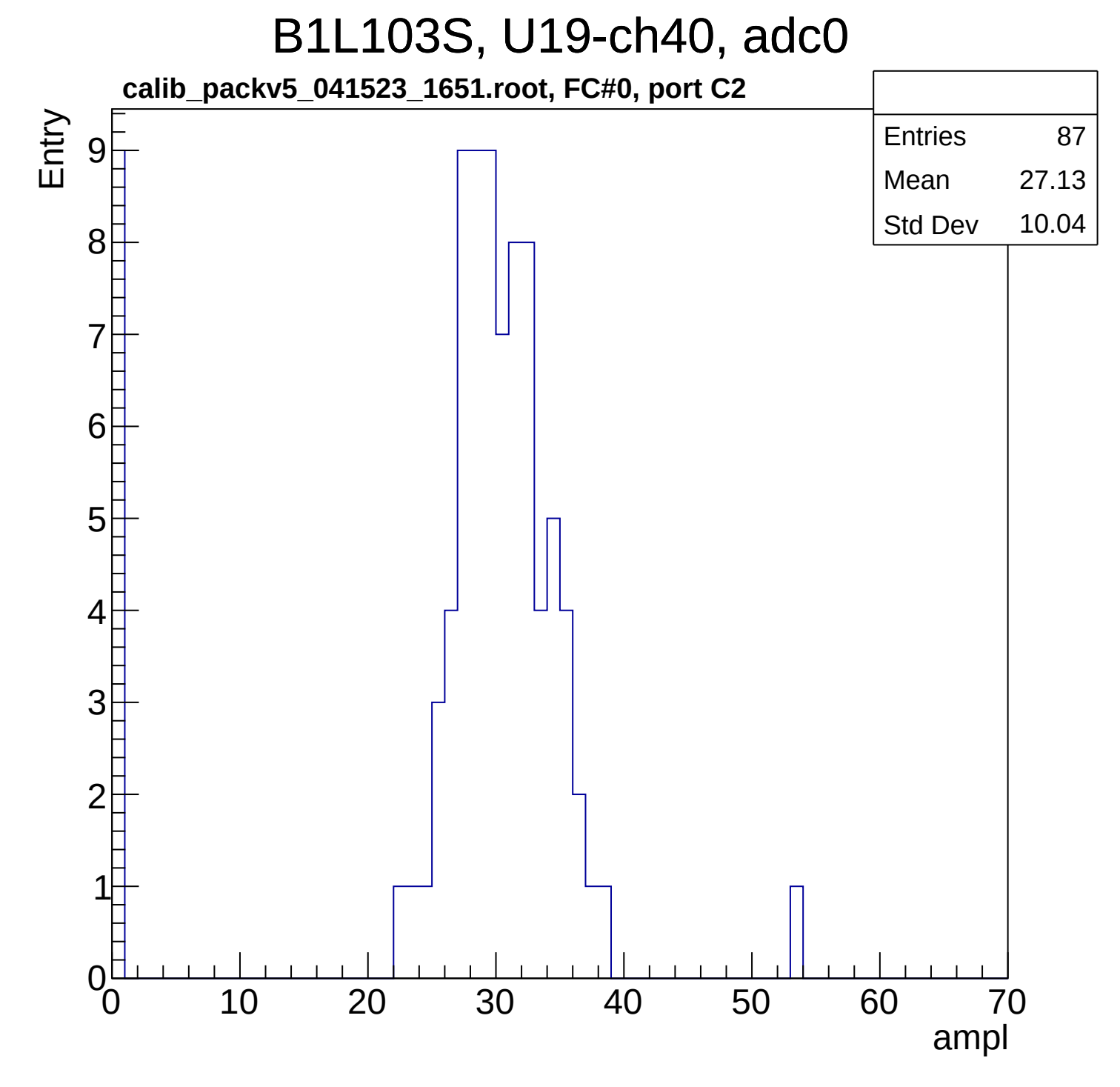
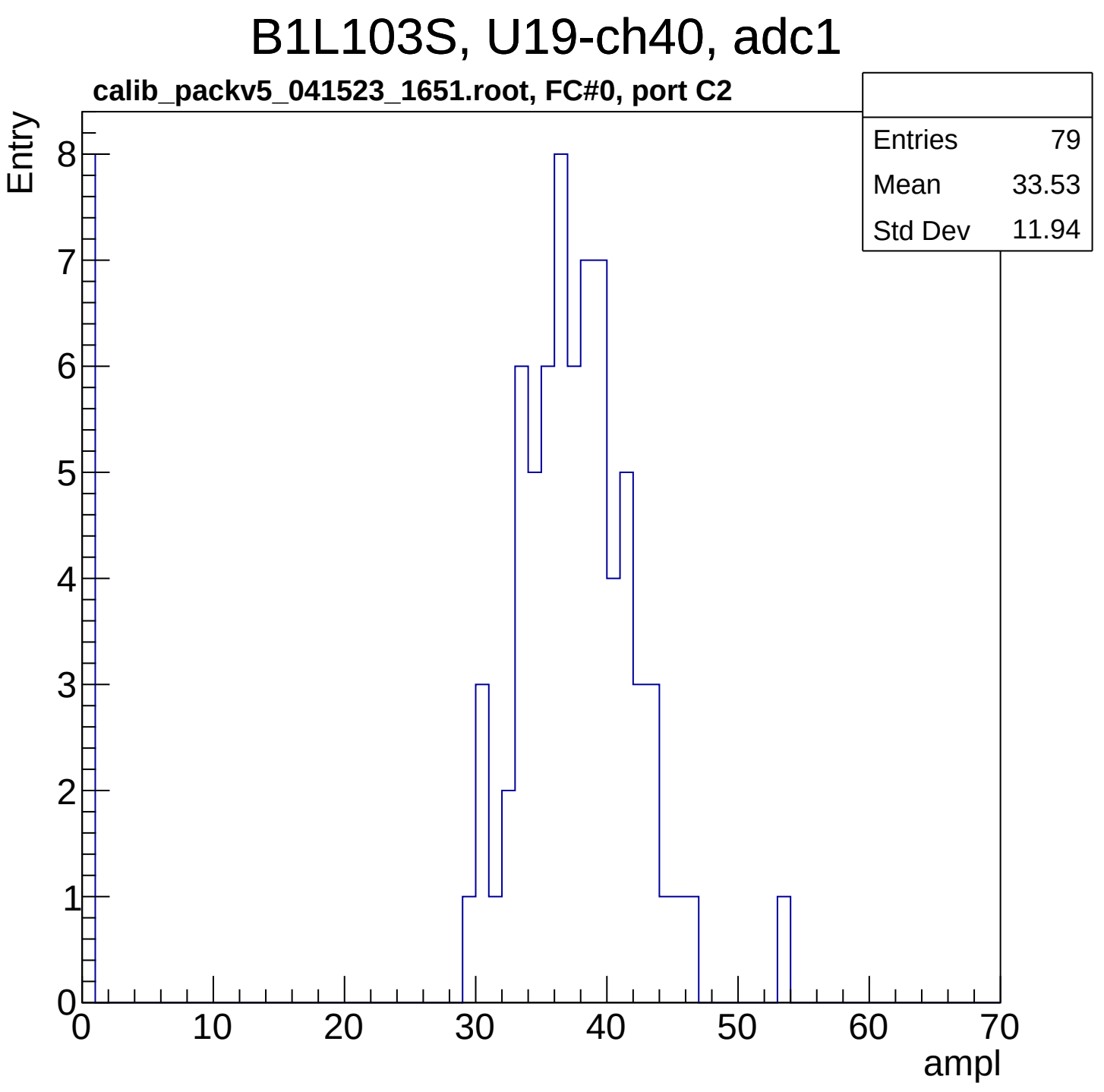
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U19-ch39, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch40, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 27.13
Std Dev 10.04
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch40, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 33.53
Std Dev 11.94
Entry
ampl
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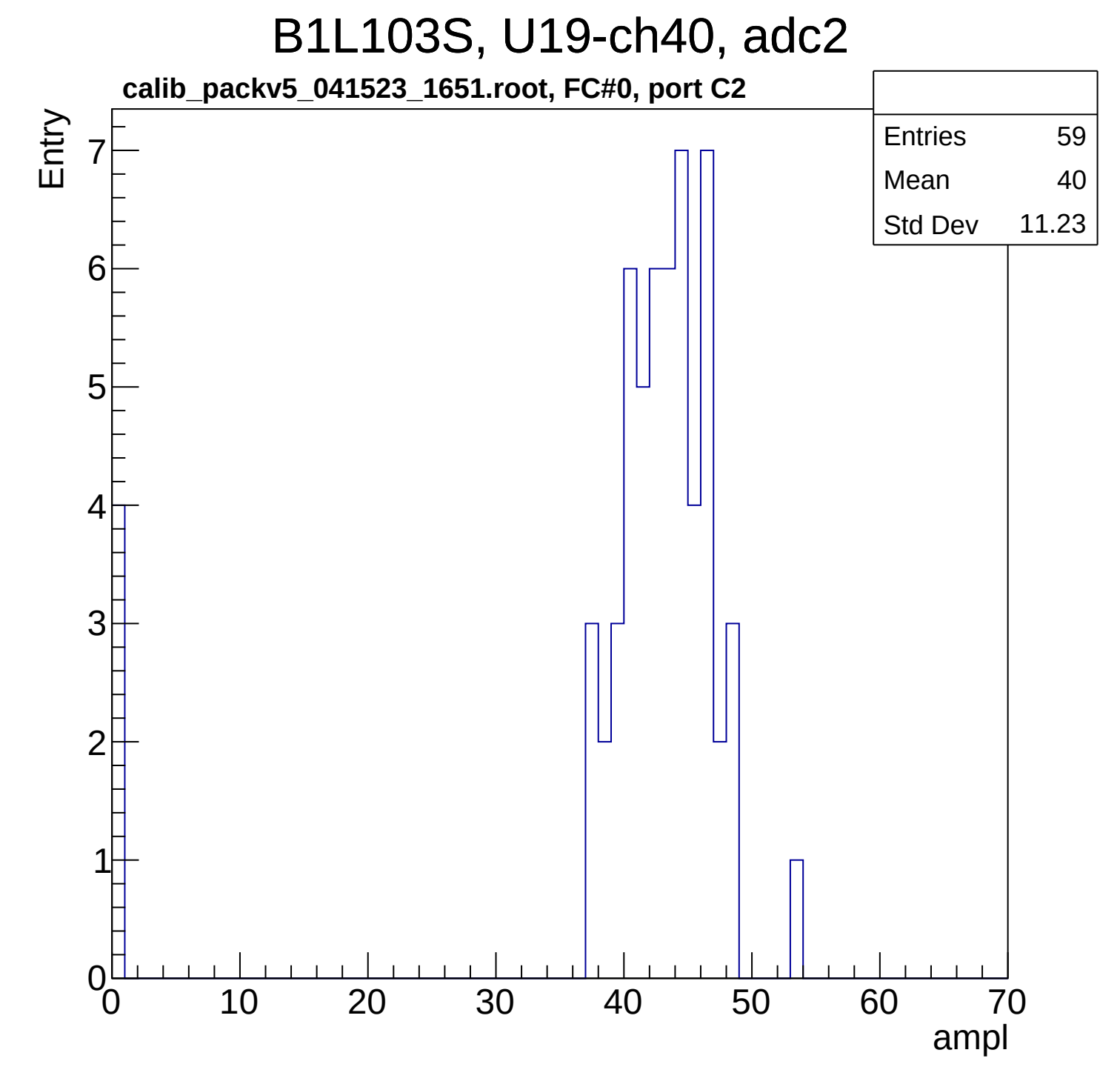
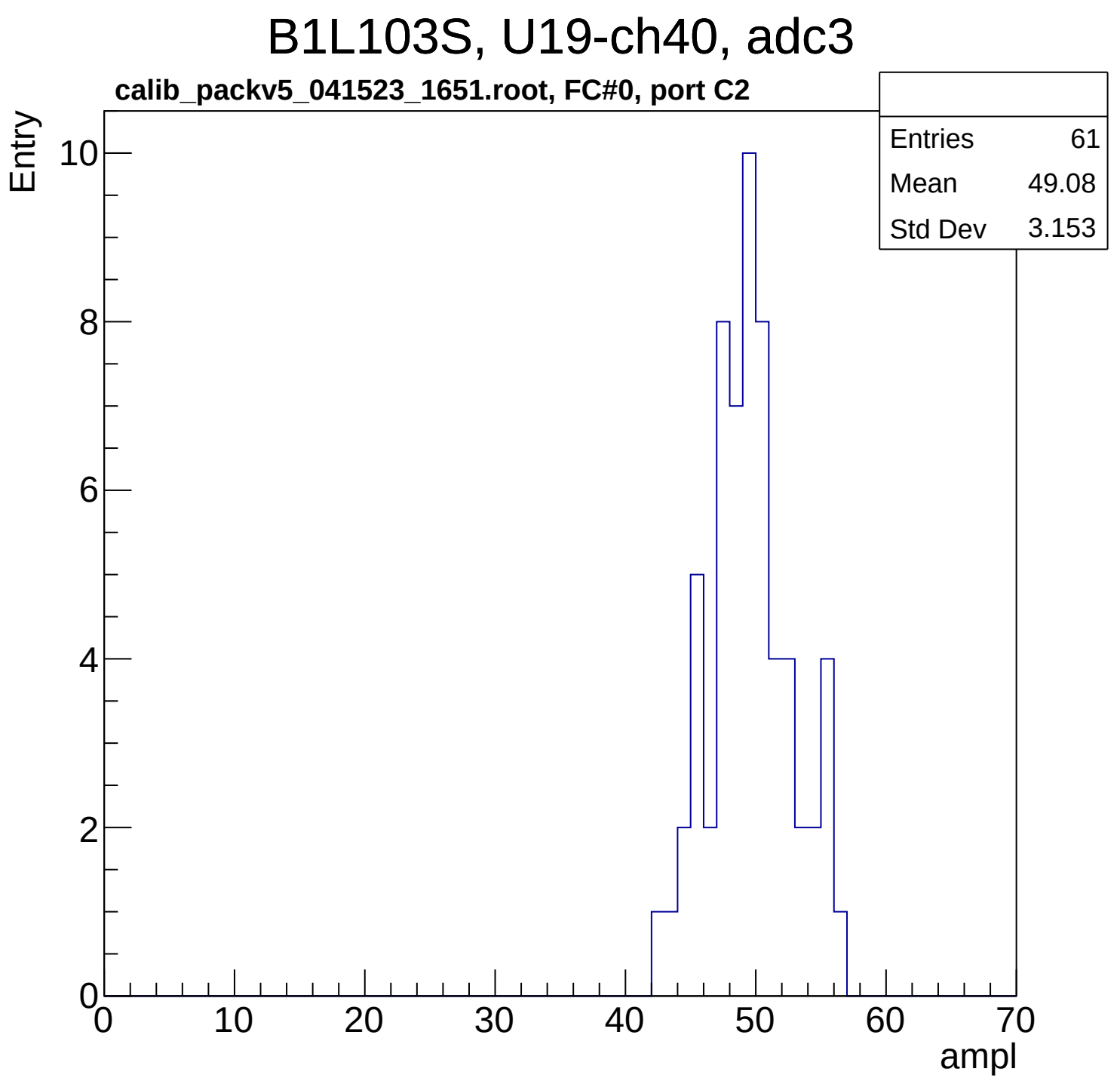
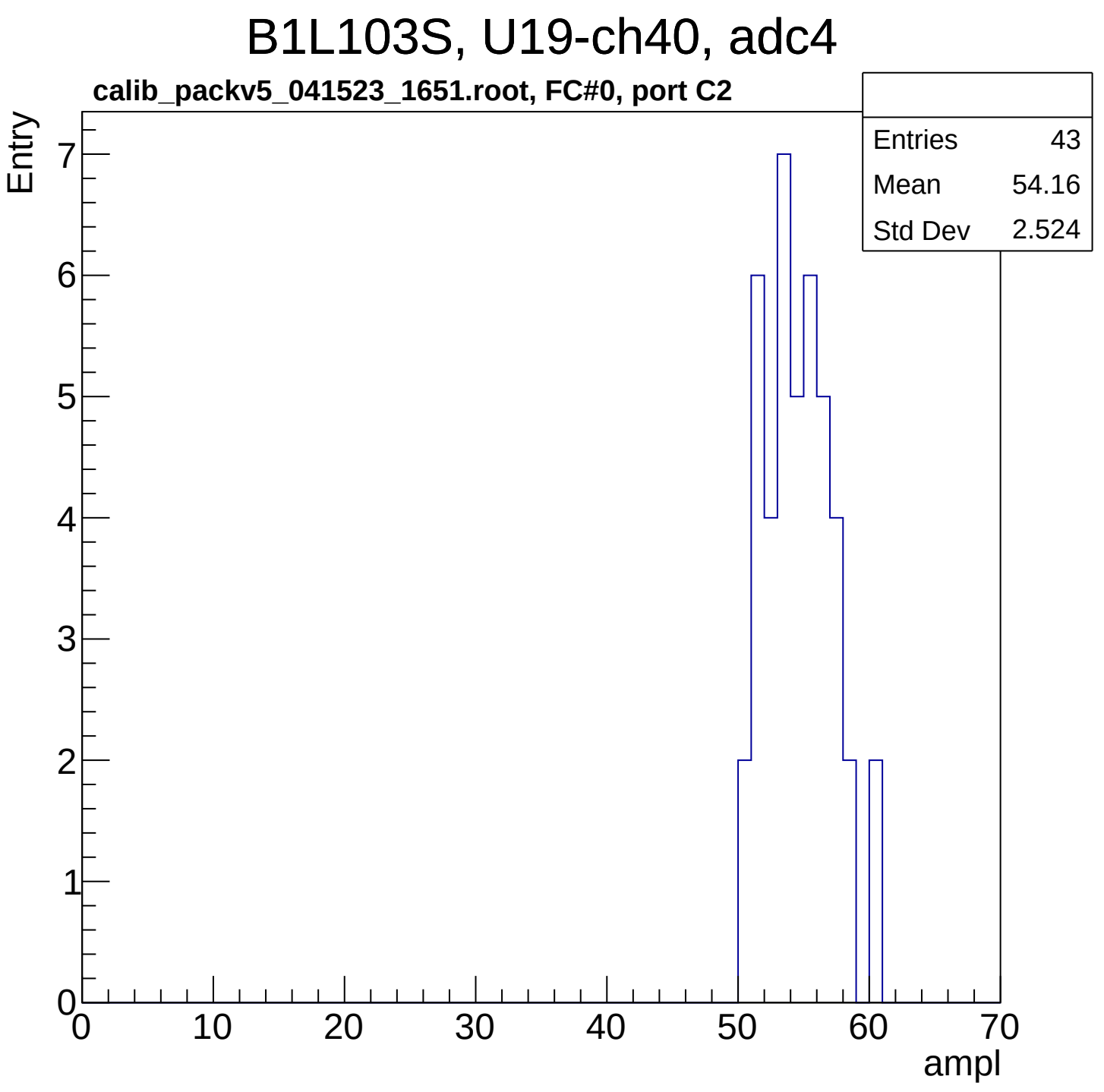
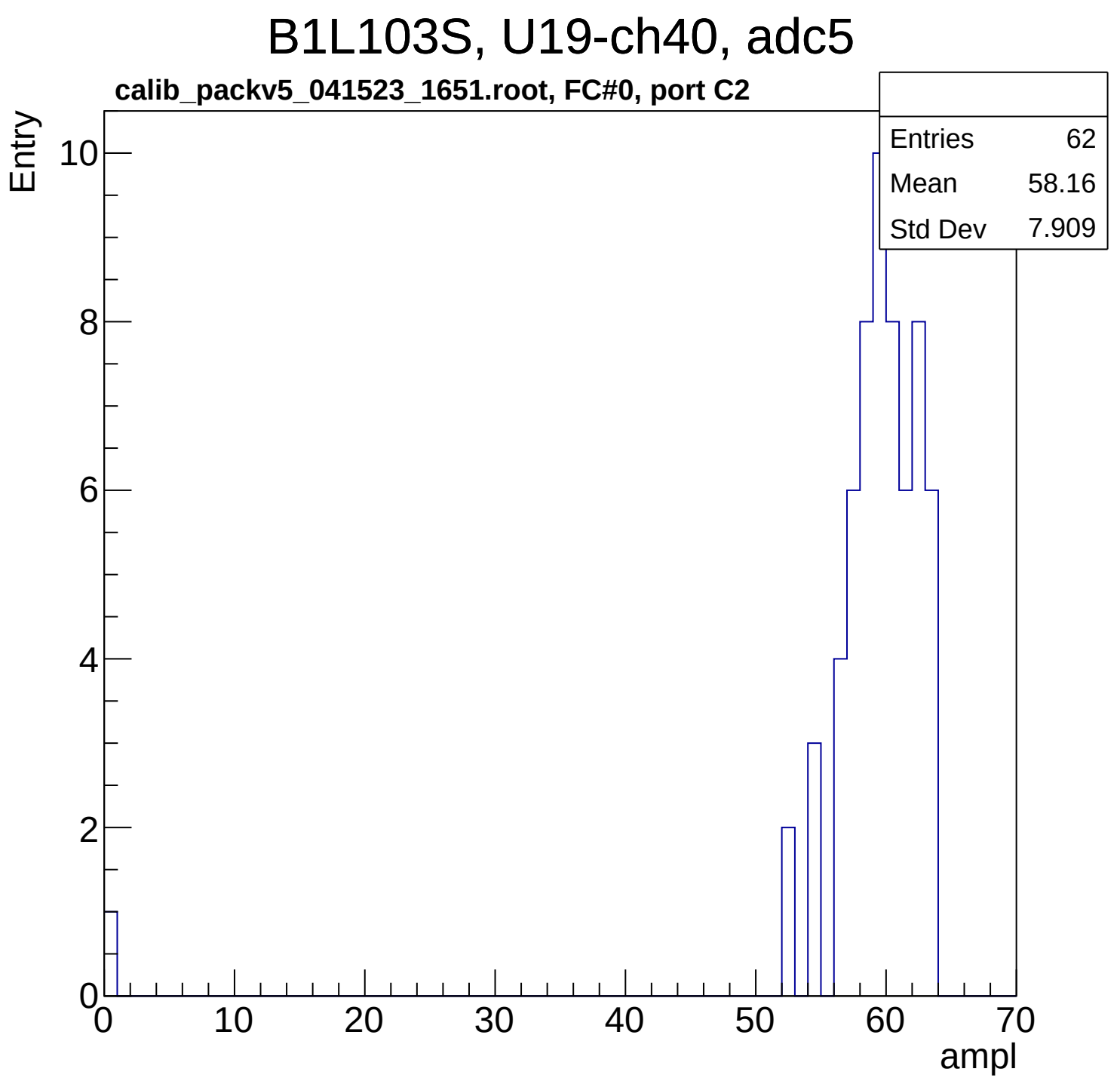
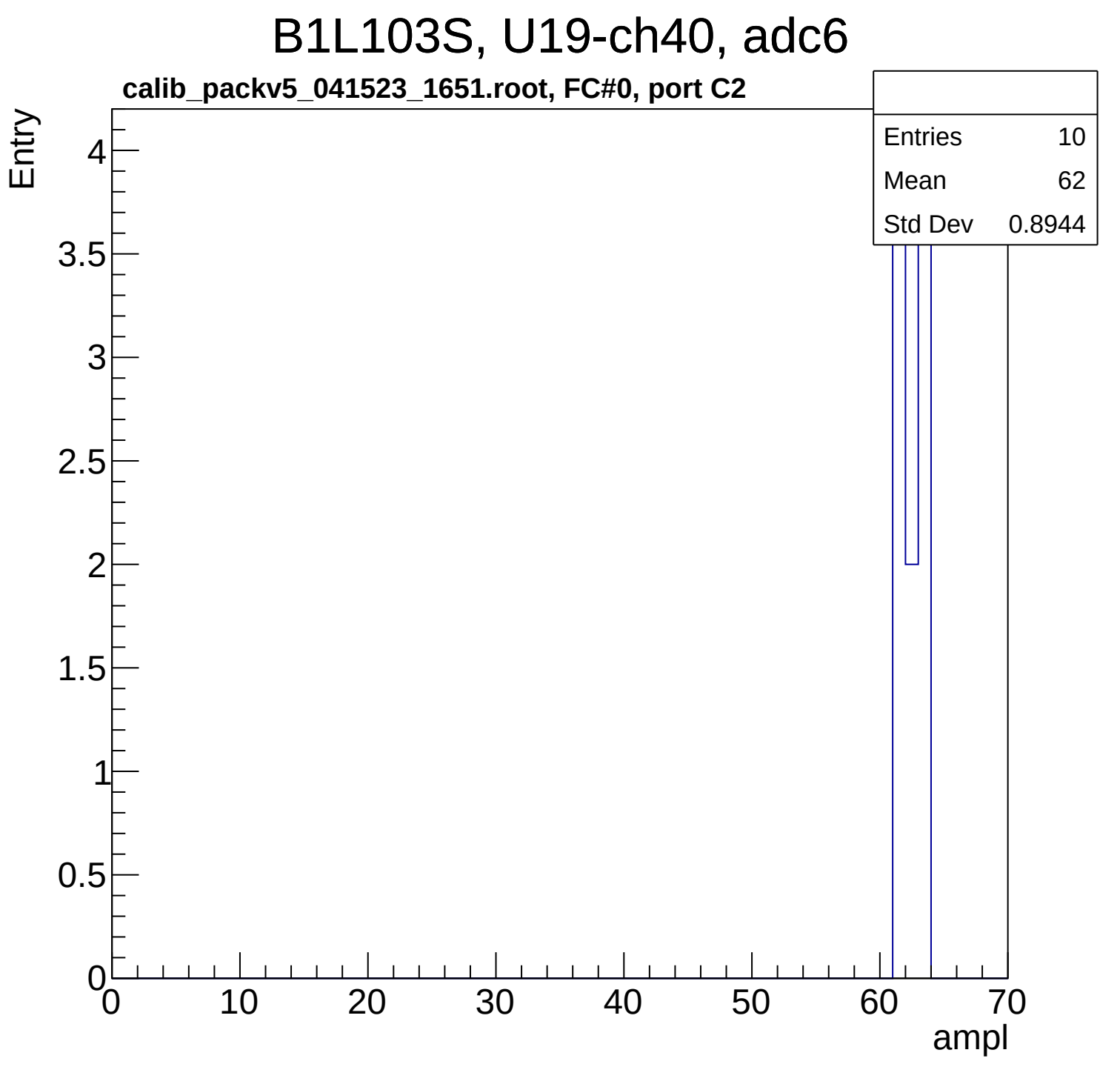
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch40, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 40
Std Dev 11.23
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch40, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 49.08
Std Dev 3.153
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U19-ch40, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 54.16
Std Dev 2.524
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch40, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 58.16
Std Dev 7.909
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch40, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 62
Std Dev 0.8944
Entry
ampl
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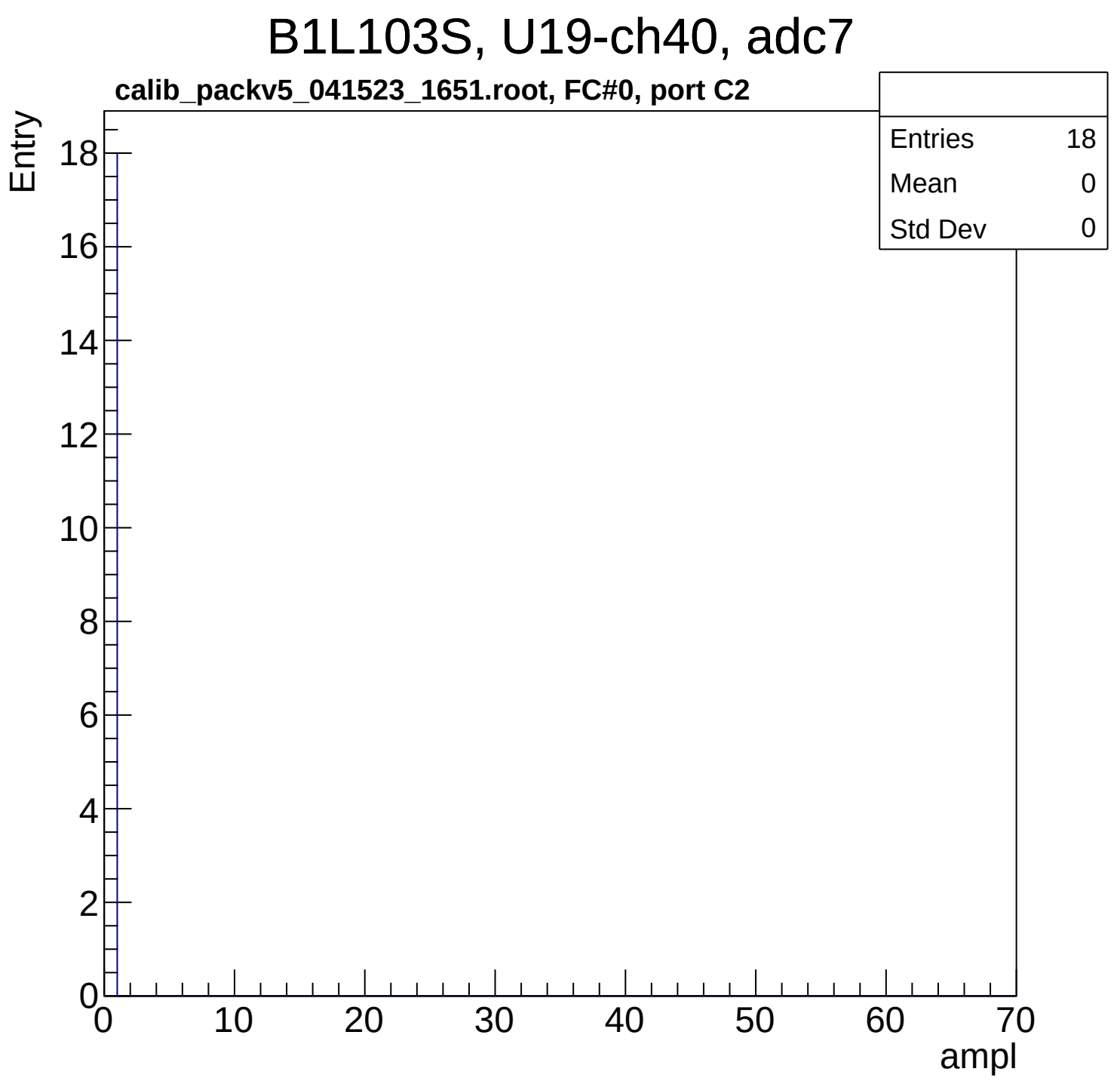
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U19-ch40, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
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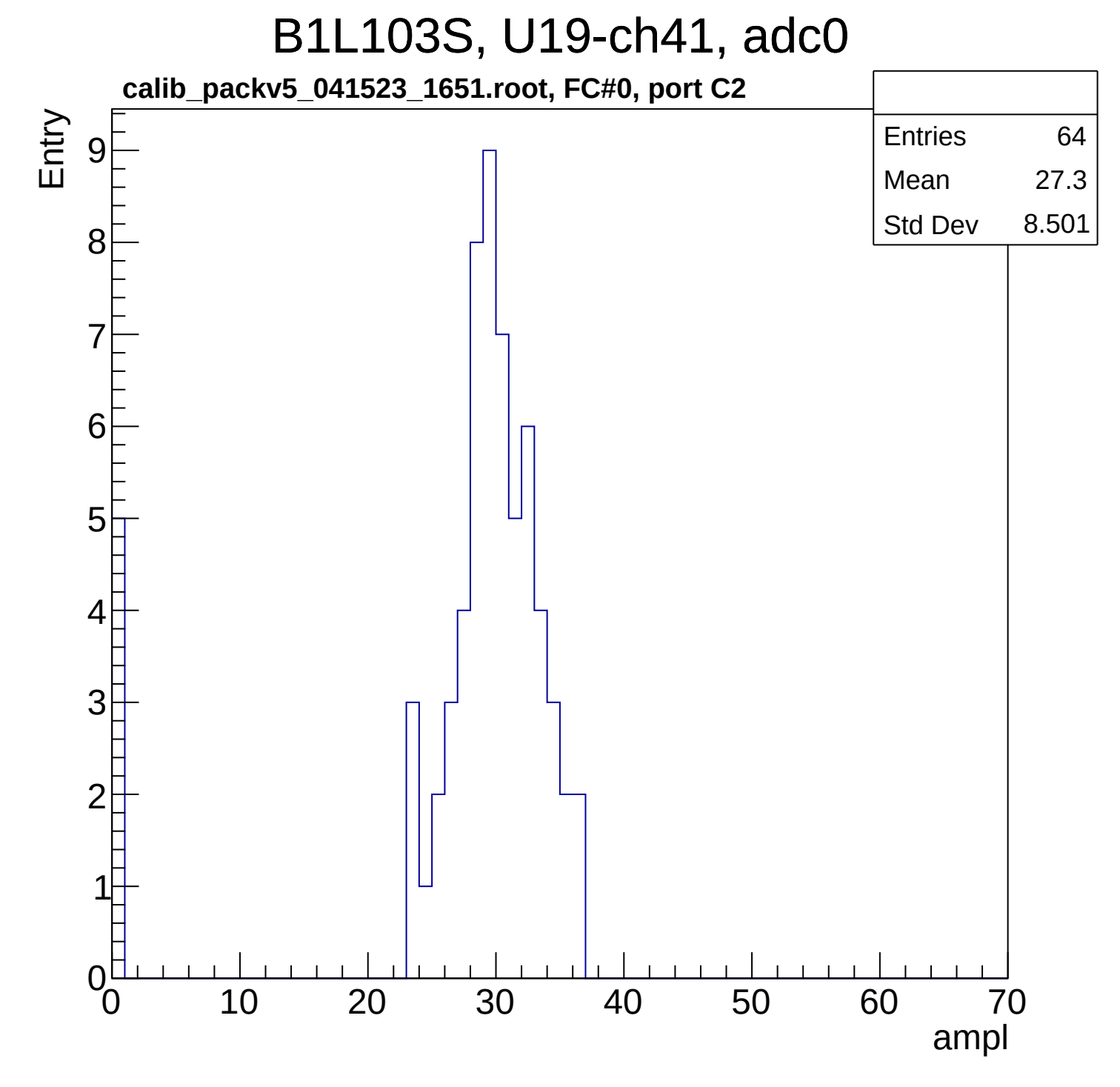
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch41, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 27.3
Std Dev 8.501
Entry
ampl
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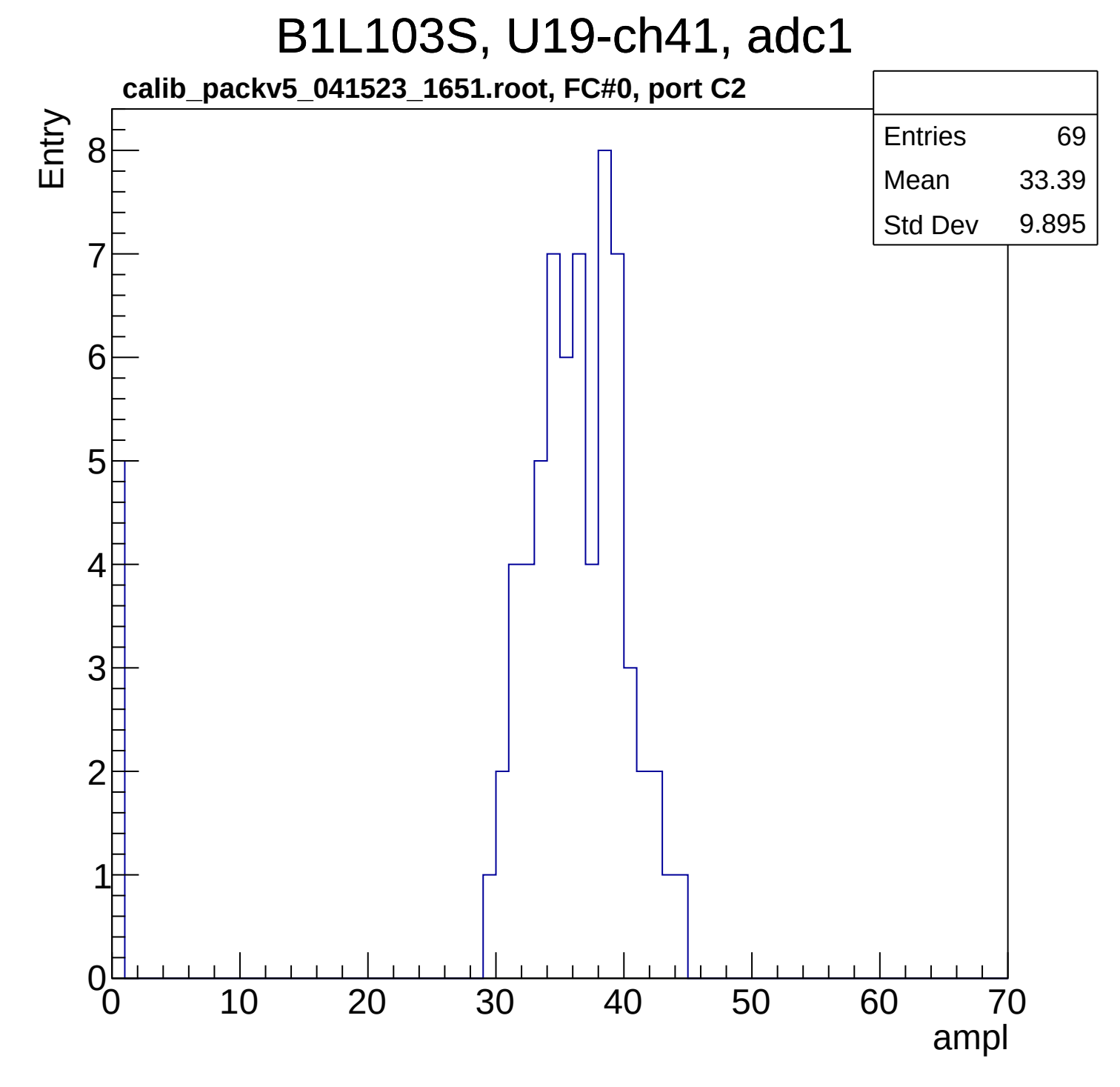
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch41, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 33.39
Std Dev 9.895
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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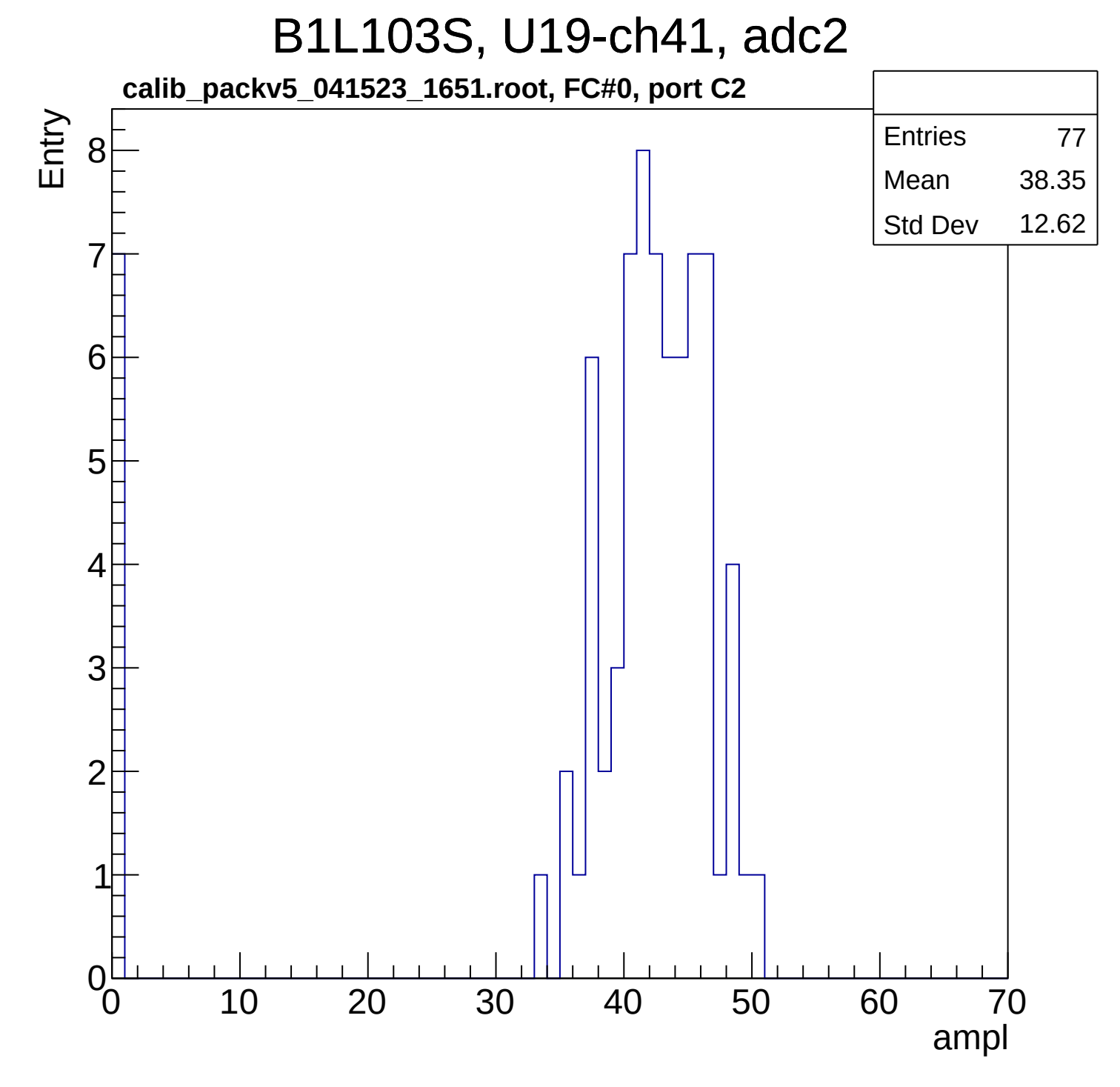
B1L103S, U19-ch41, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 38.35
Std Dev 12.62
Entry
ampl
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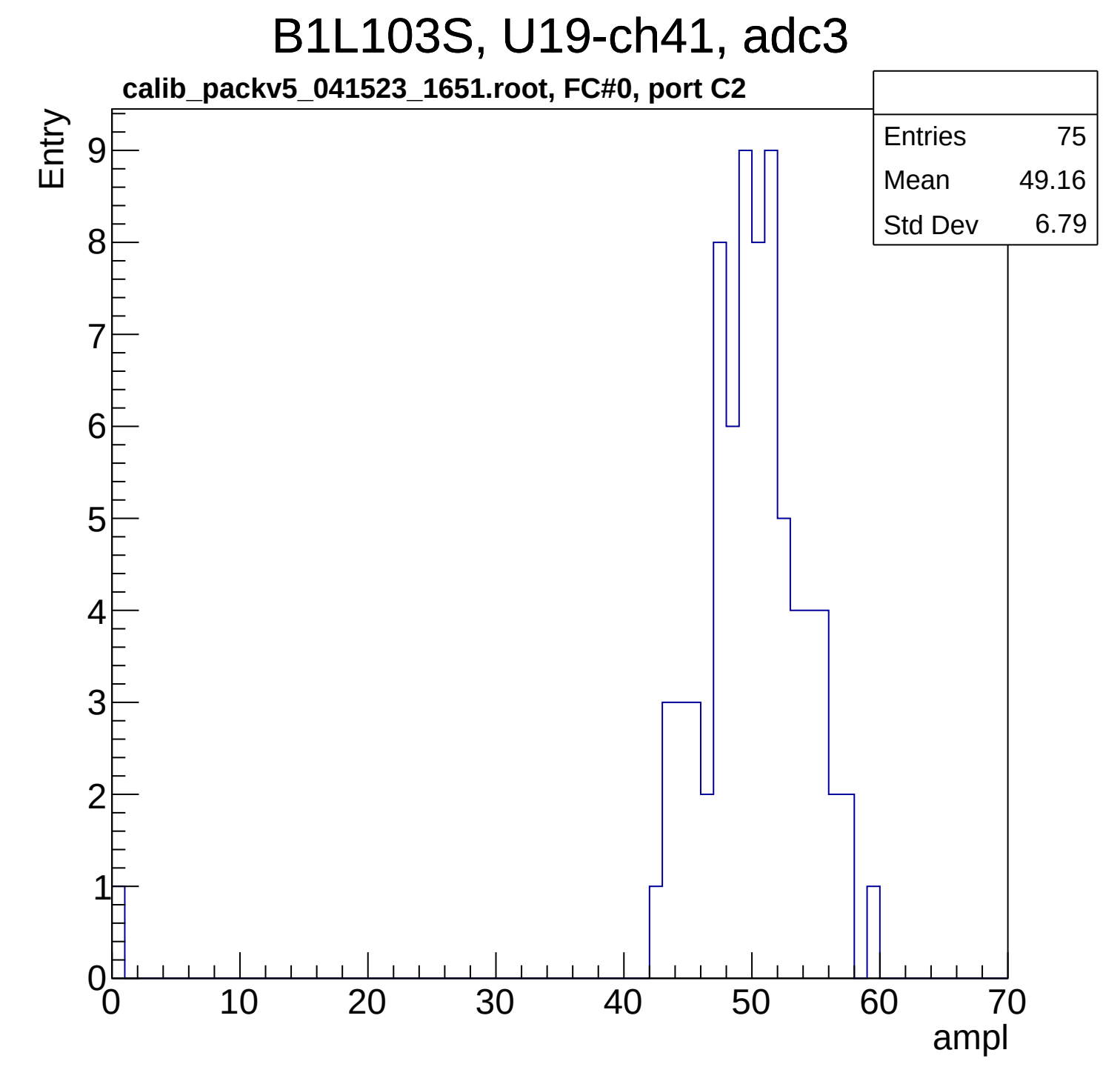
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch41, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 49.16
Std Dev 6.79
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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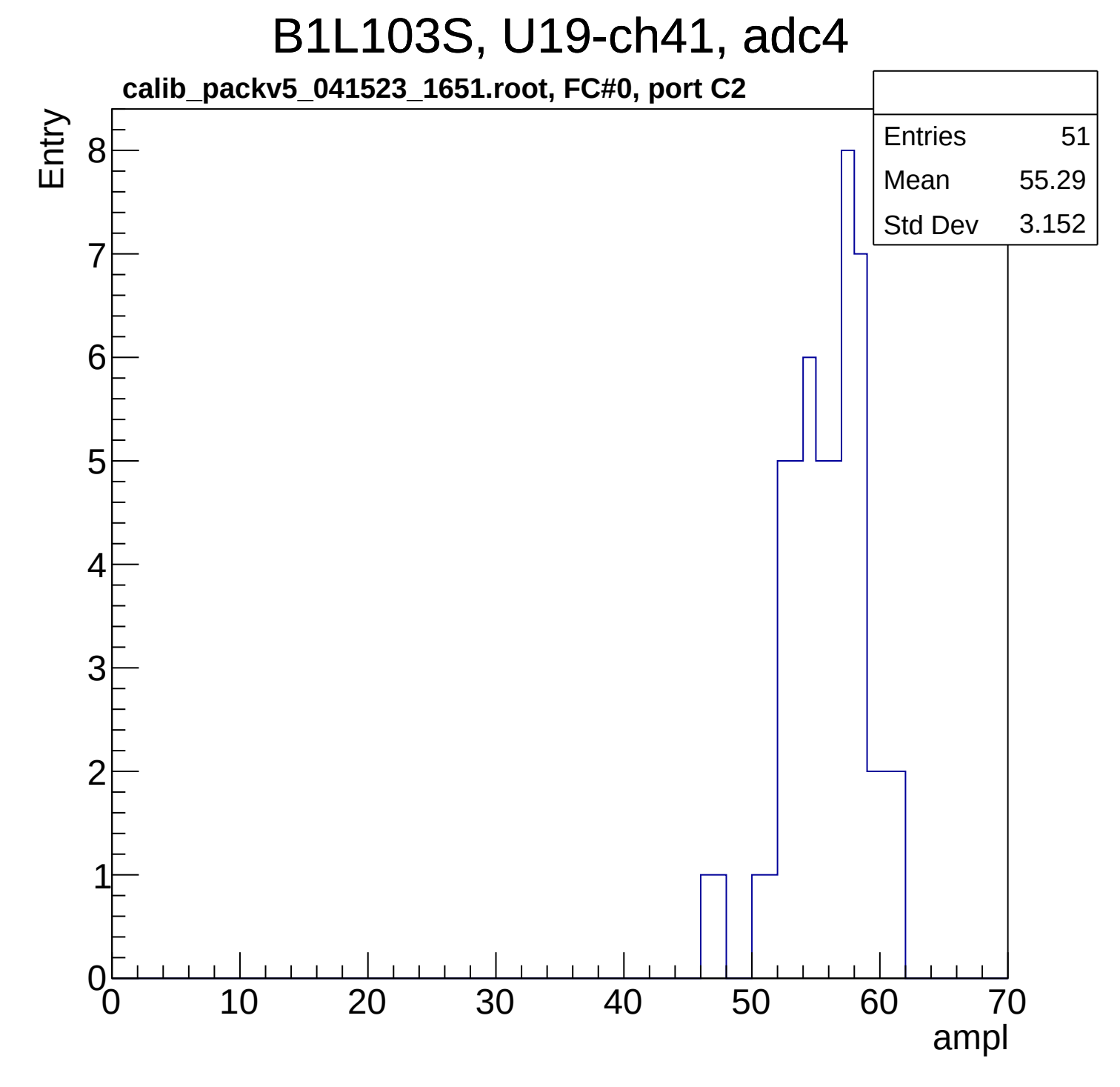
40
50
60
70


B1L103S, U19-ch41, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 55.29
Std Dev 3.152
Entry
ampl
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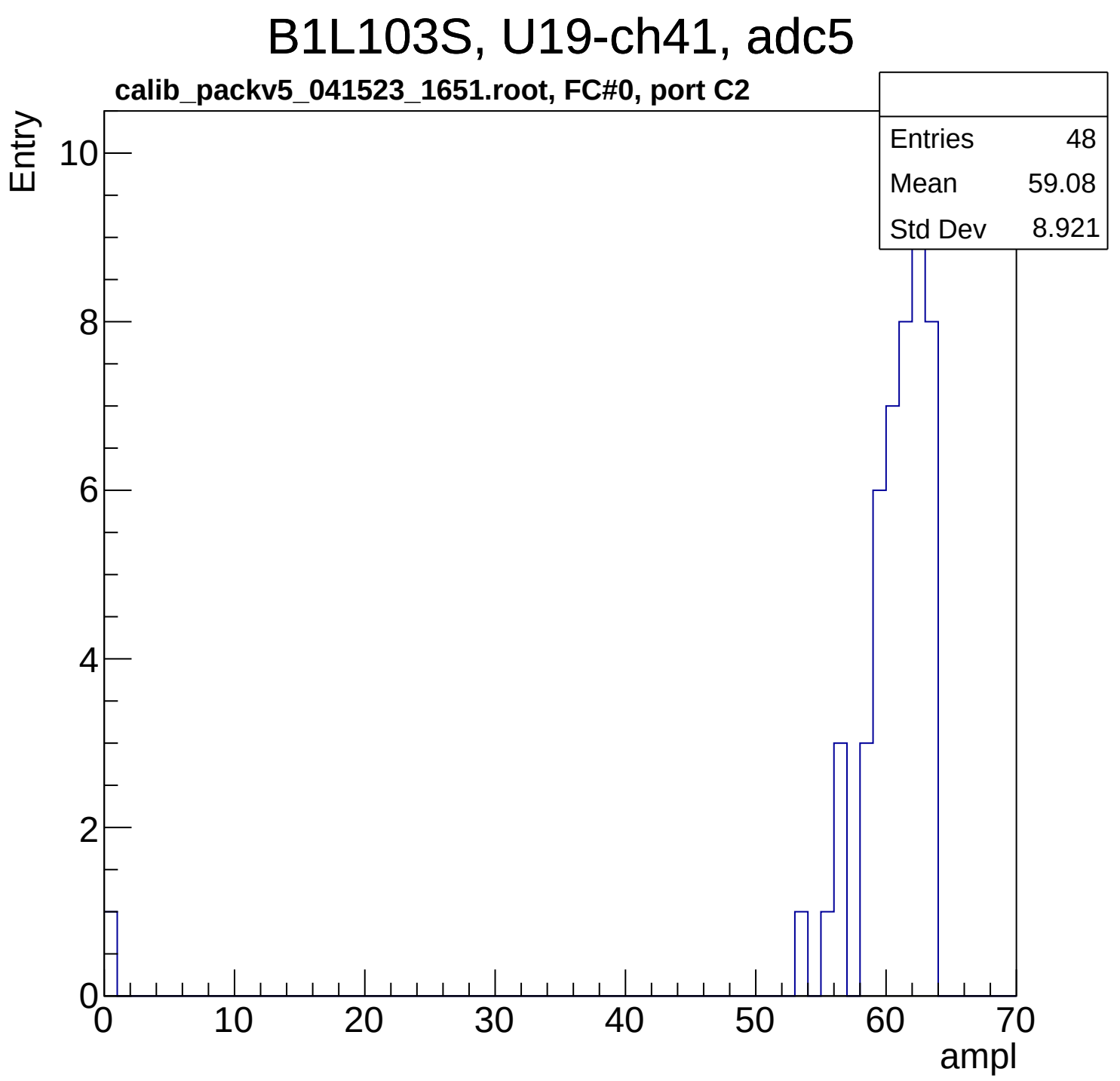
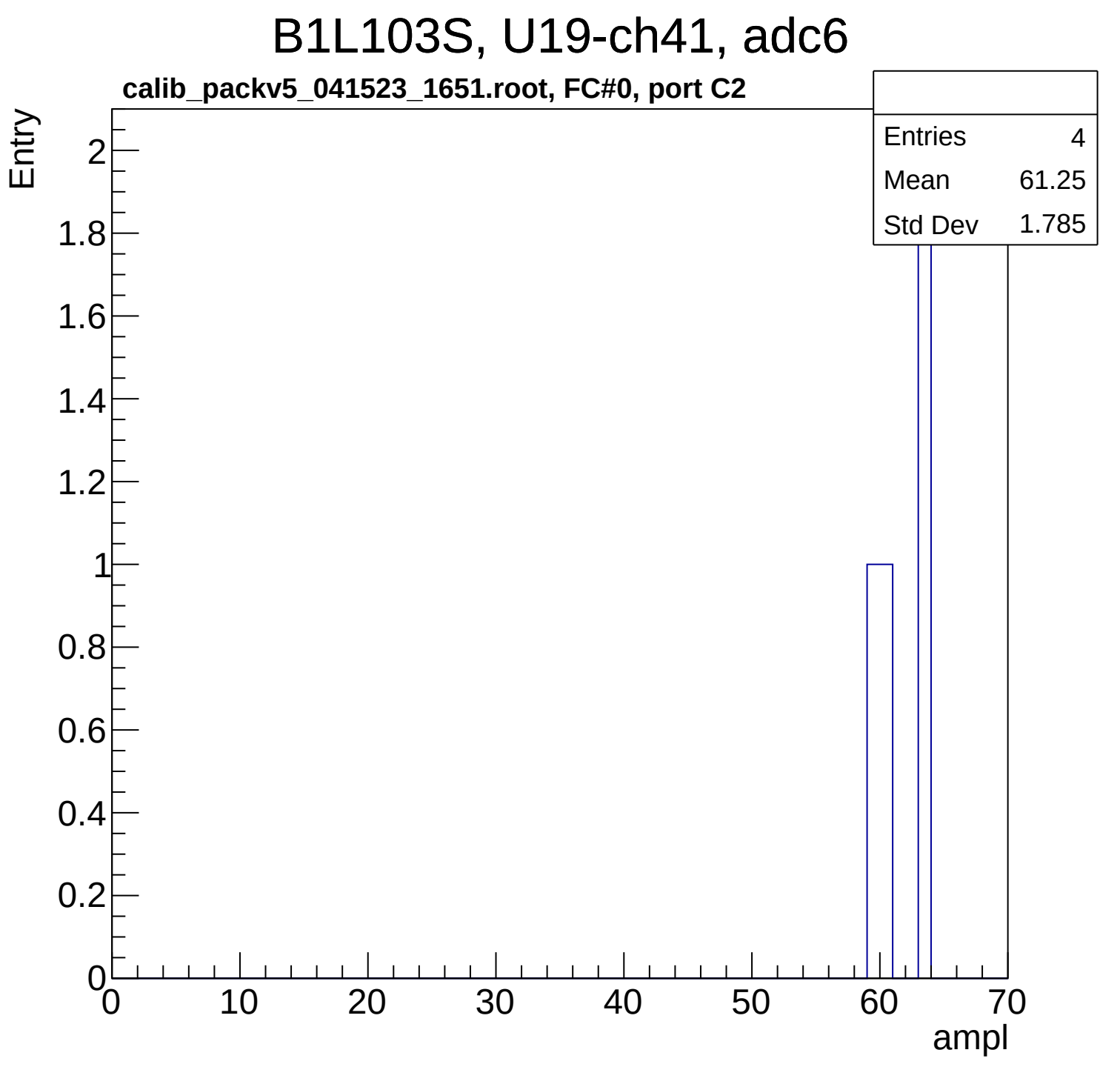
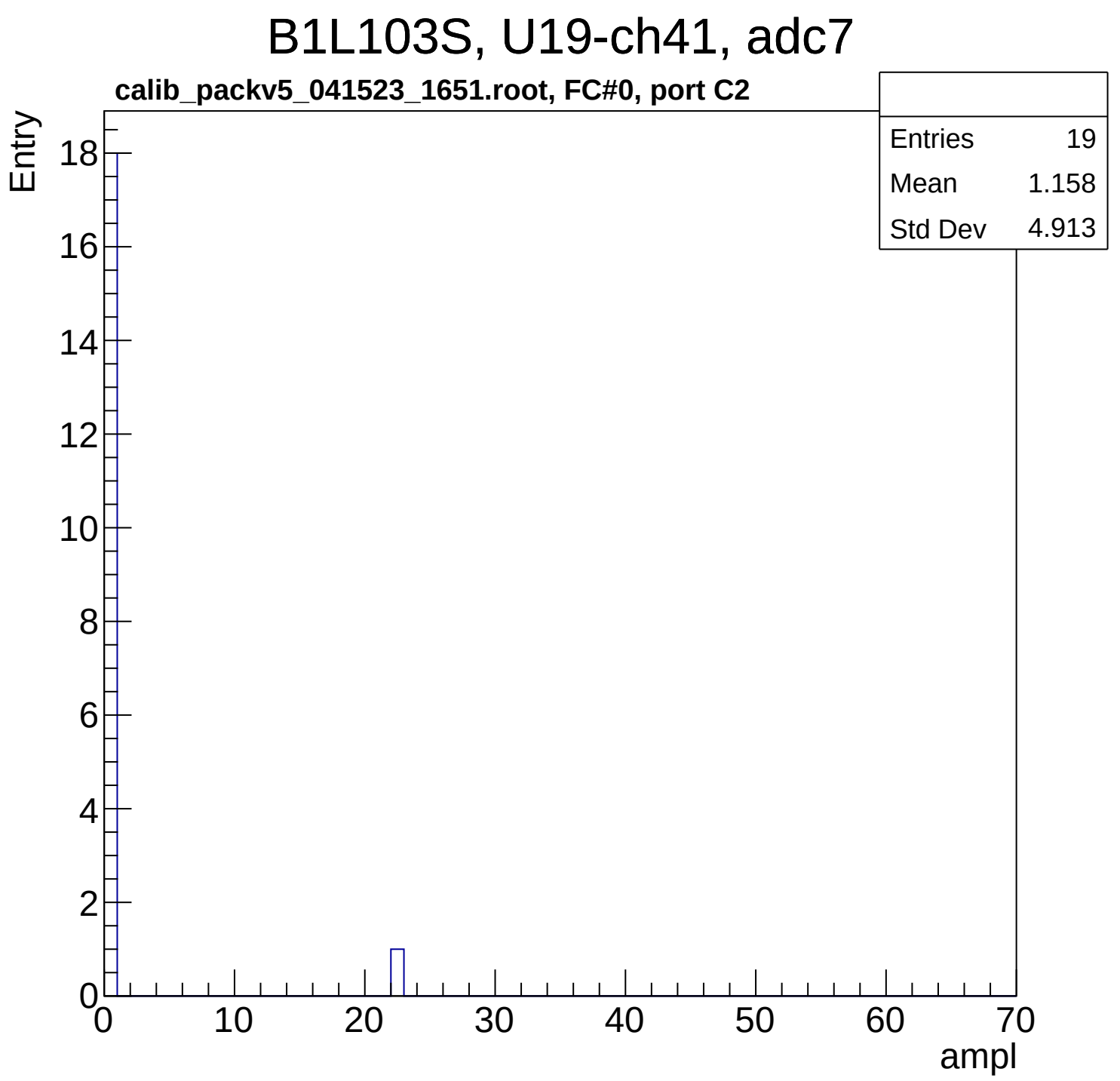
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch41, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 59.08
Std Dev 8.921
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch41, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 61.25
Std Dev 1.785
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U19-ch41, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.158
Std Dev 4.913
Entry
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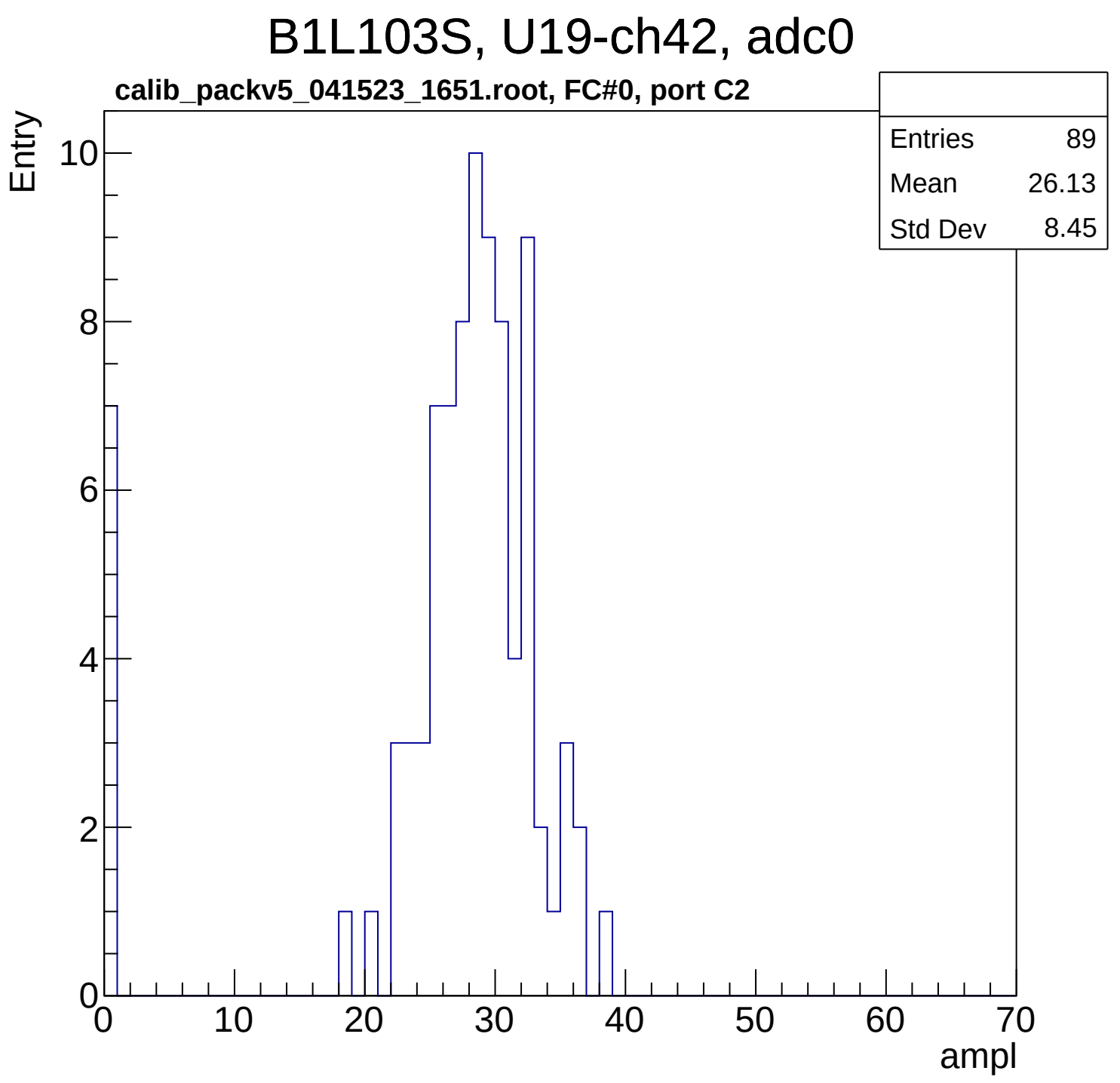
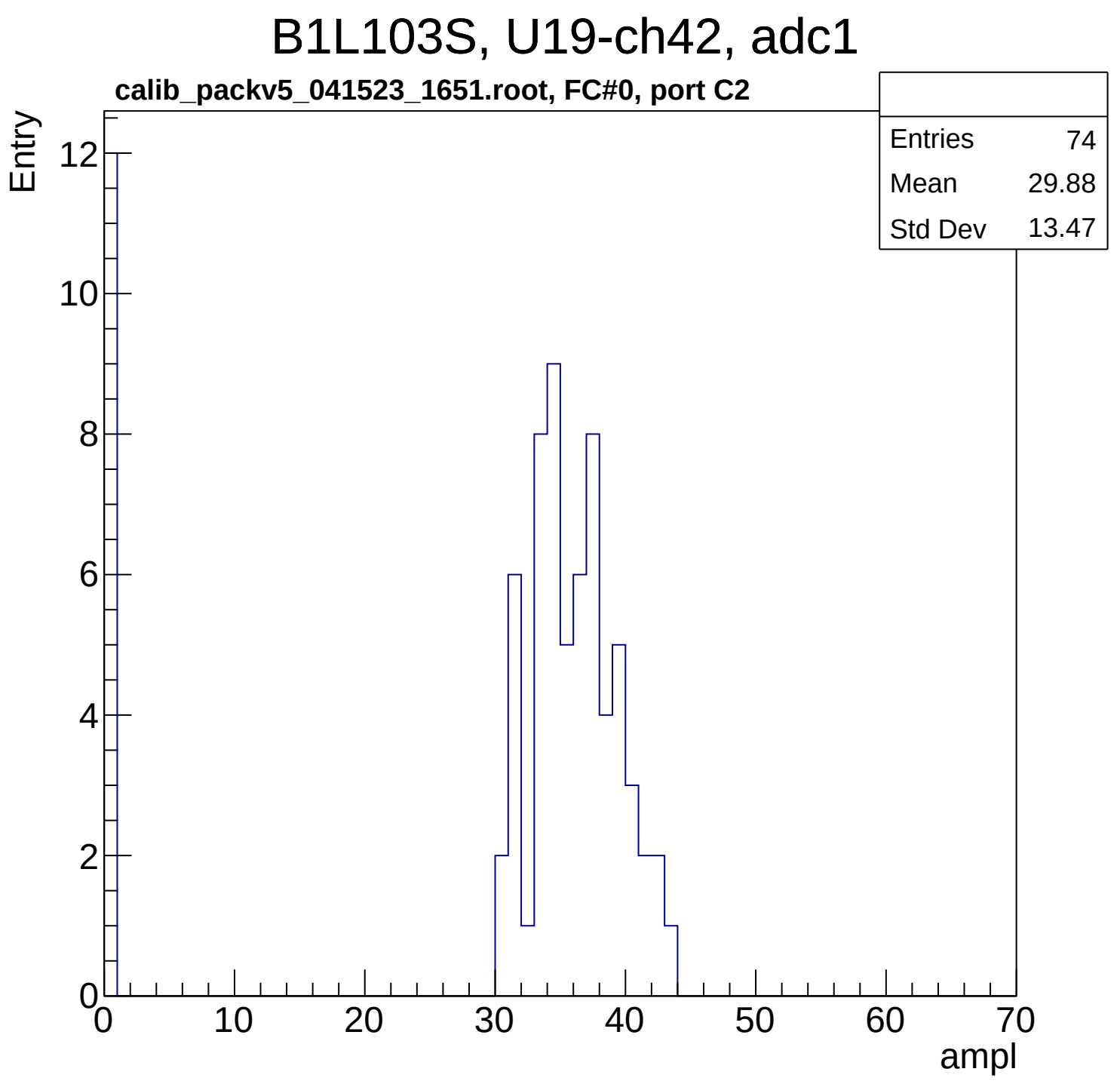
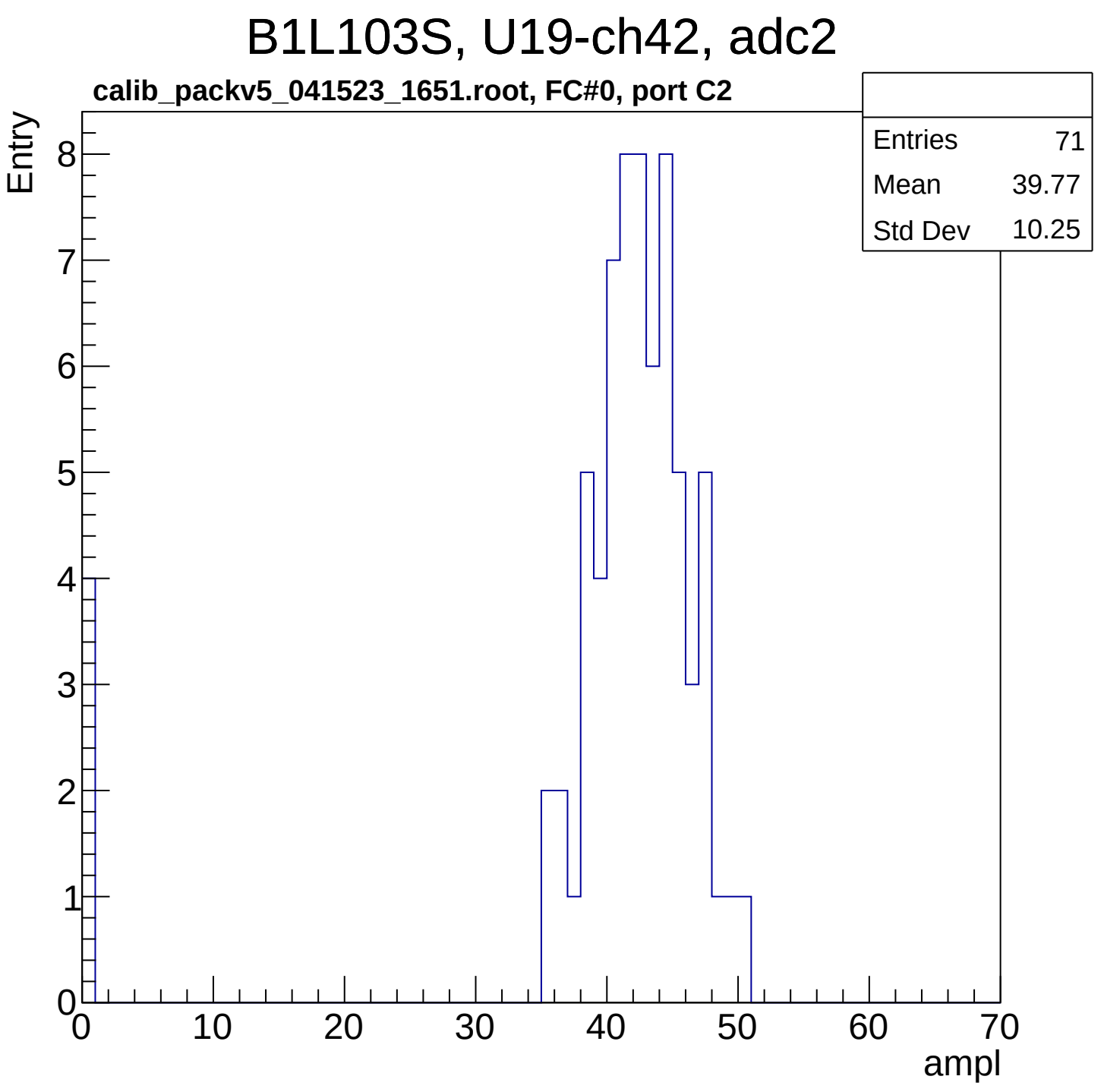
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch42, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 26.13
Std Dev 8.45
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U19-ch42, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 29.88
Std Dev 13.47
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch42, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 39.77
Std Dev 10.25
Entry
ampl
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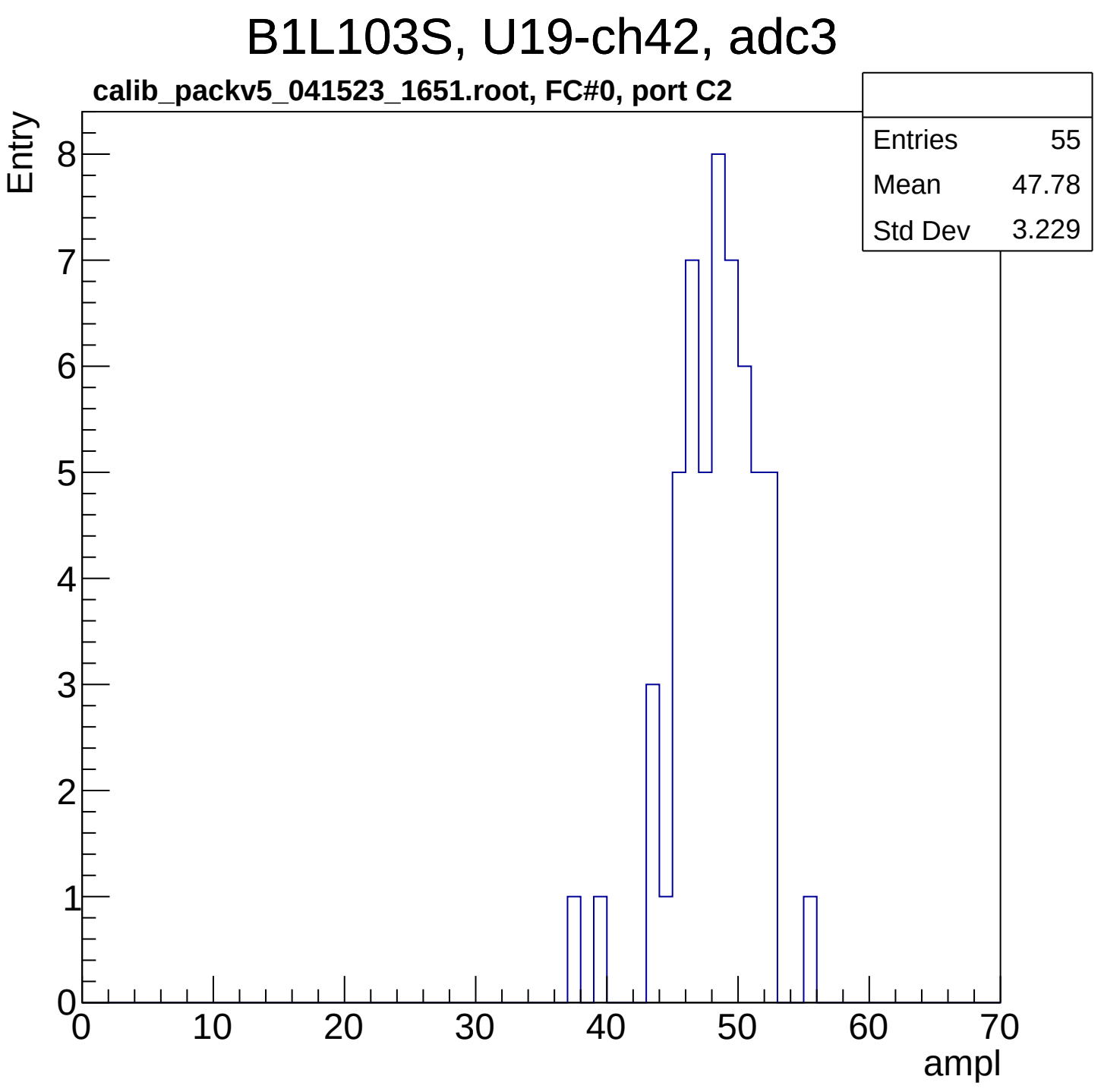
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch42, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 47.78
Std Dev 3.229
Entry
ampl
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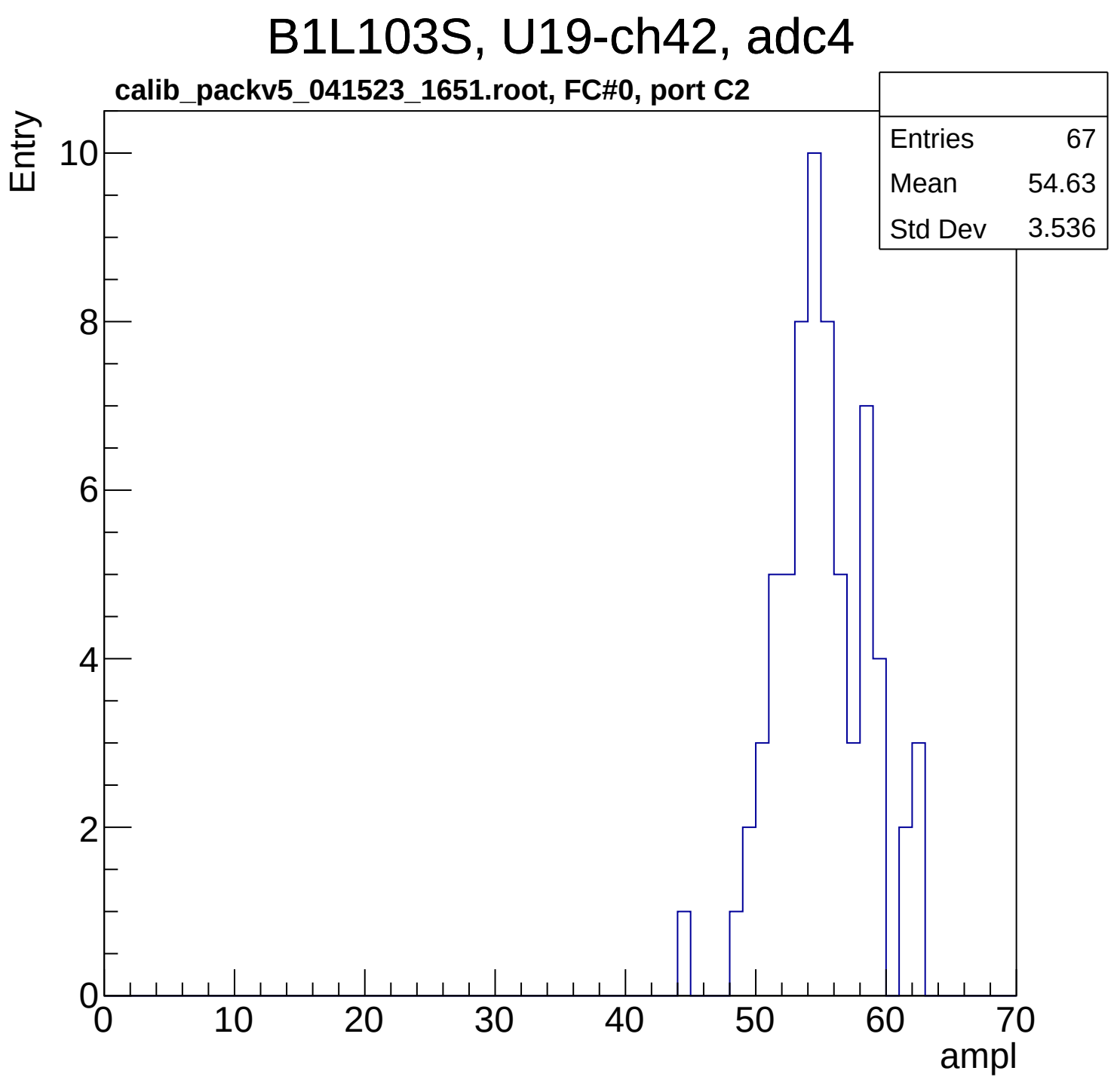
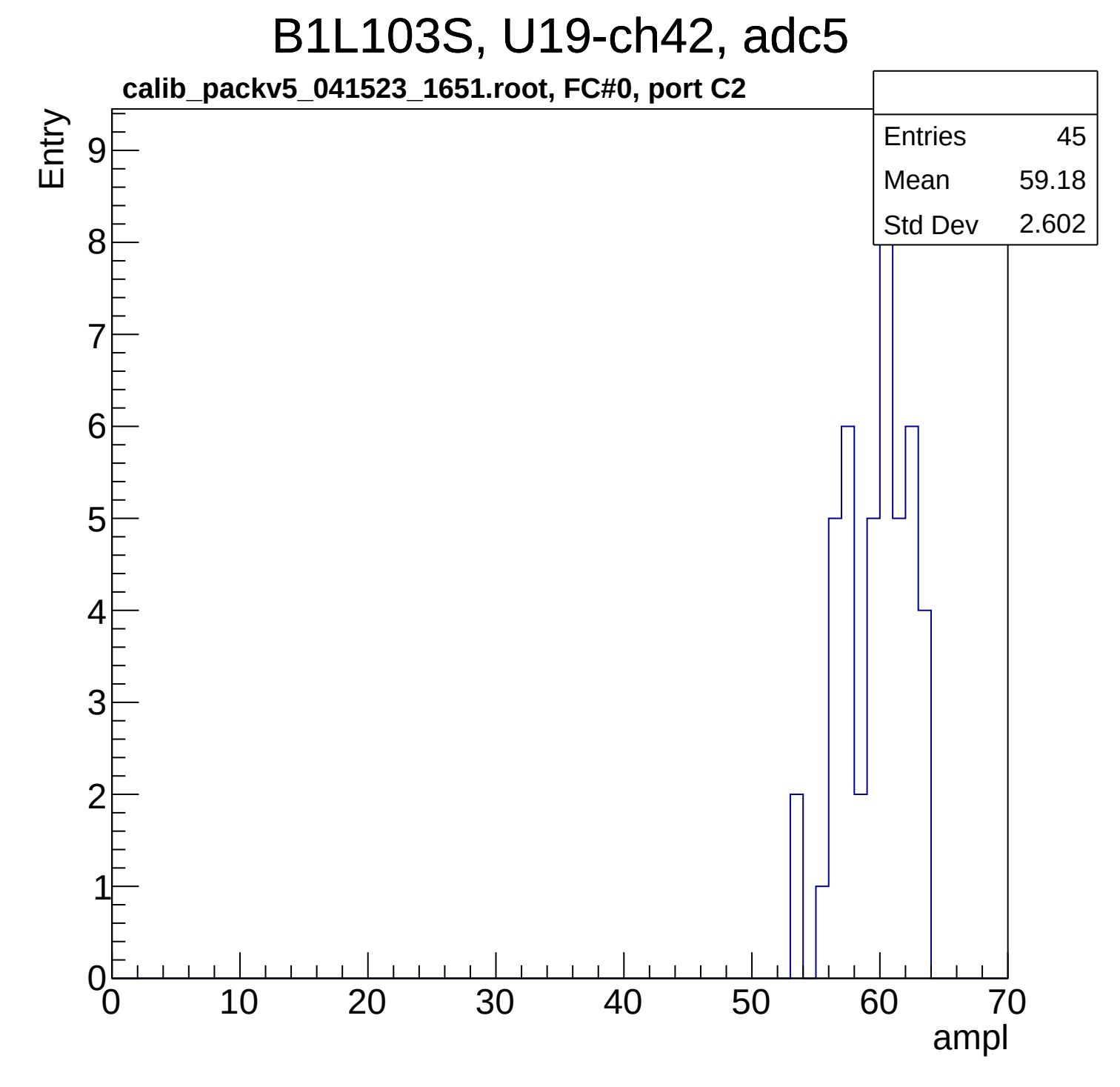
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch42, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 54.63
Std Dev 3.536
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch42, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 59.18
Std Dev 2.602
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
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40
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60
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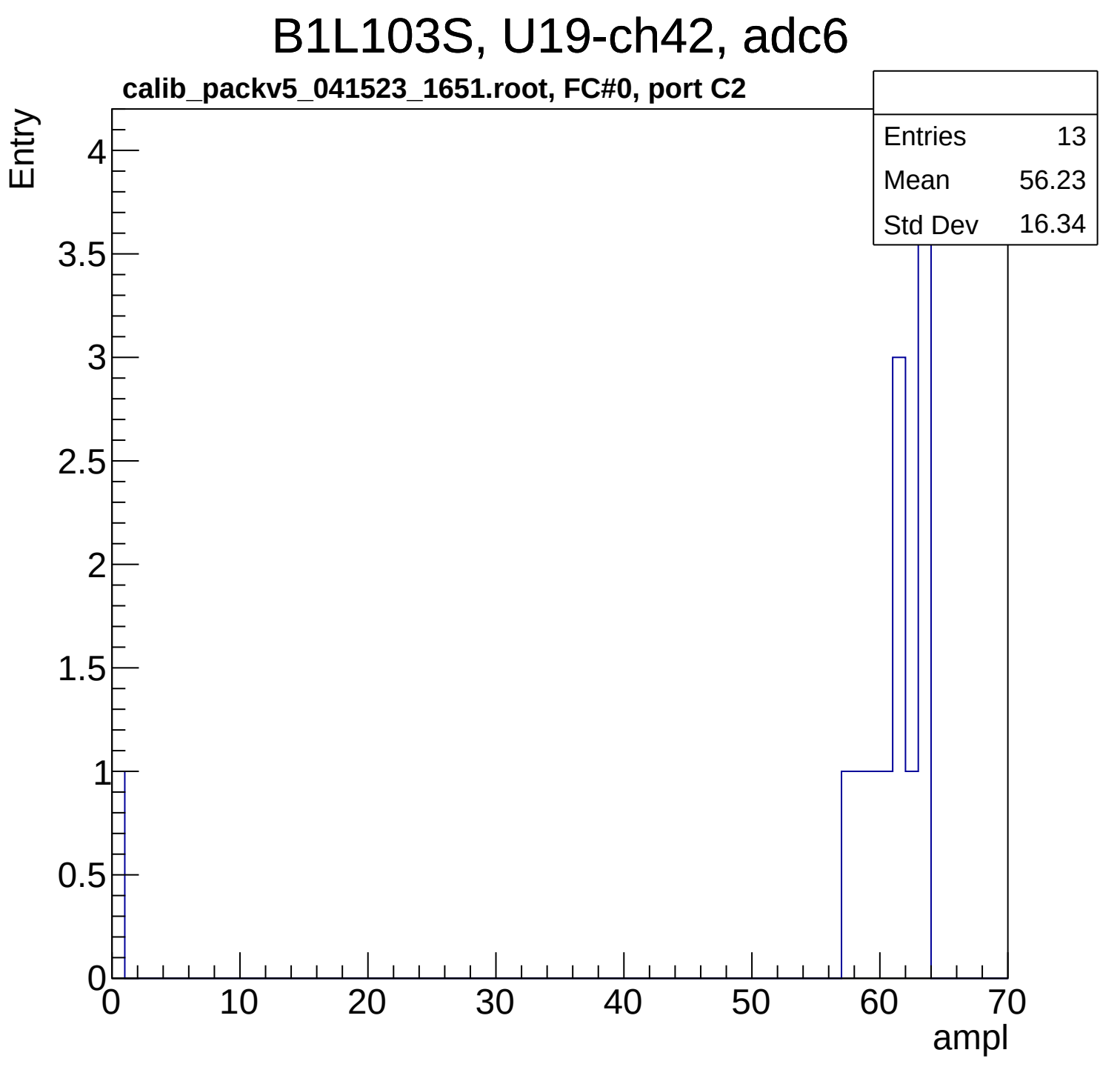
B1L103S, U19-ch42, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 56.23
Std Dev 16.34
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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40
50
60
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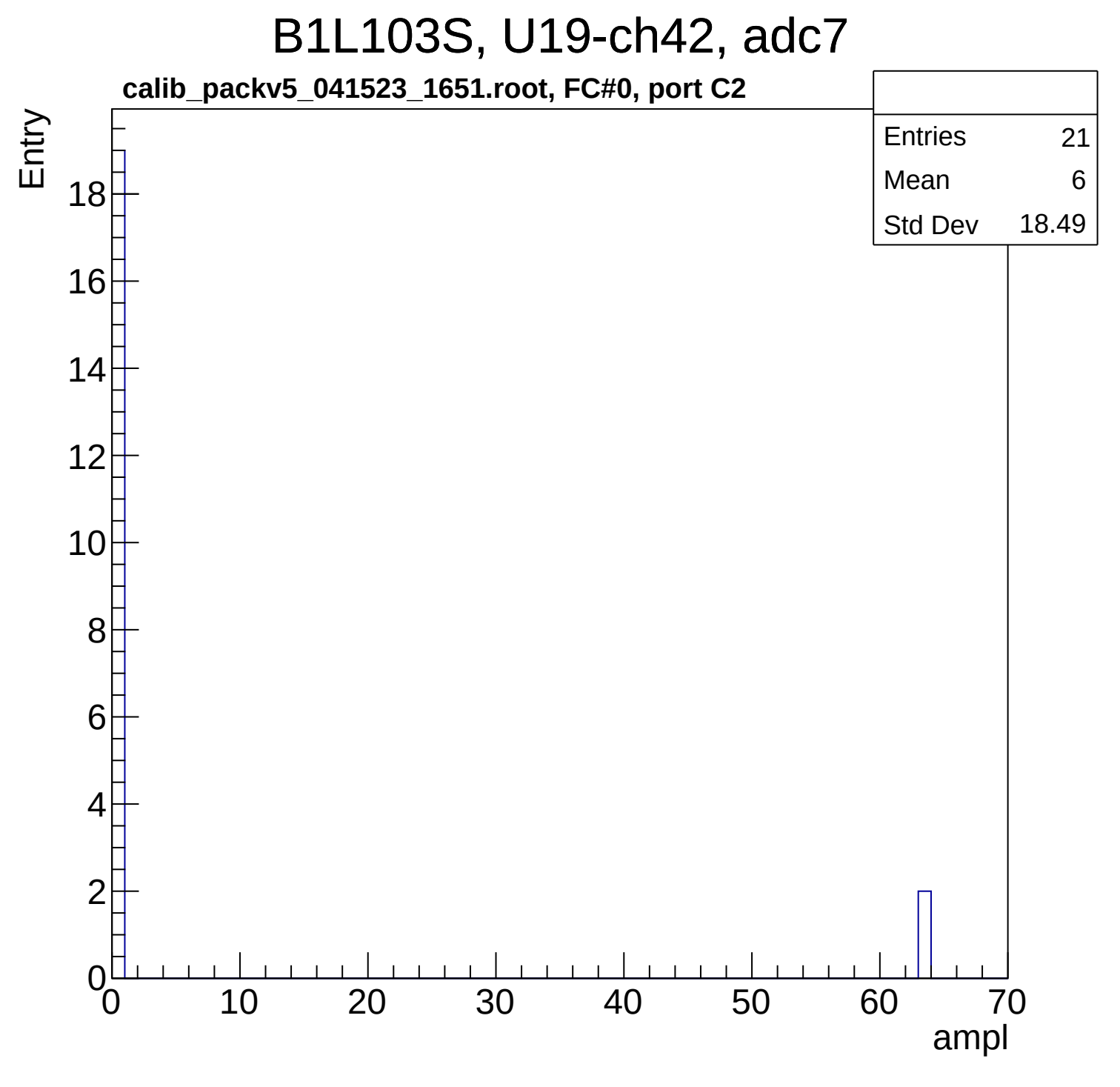
B1L103S, U19-ch42, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 6
Std Dev 18.49
Entry
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6
8
10
12
14
16
18
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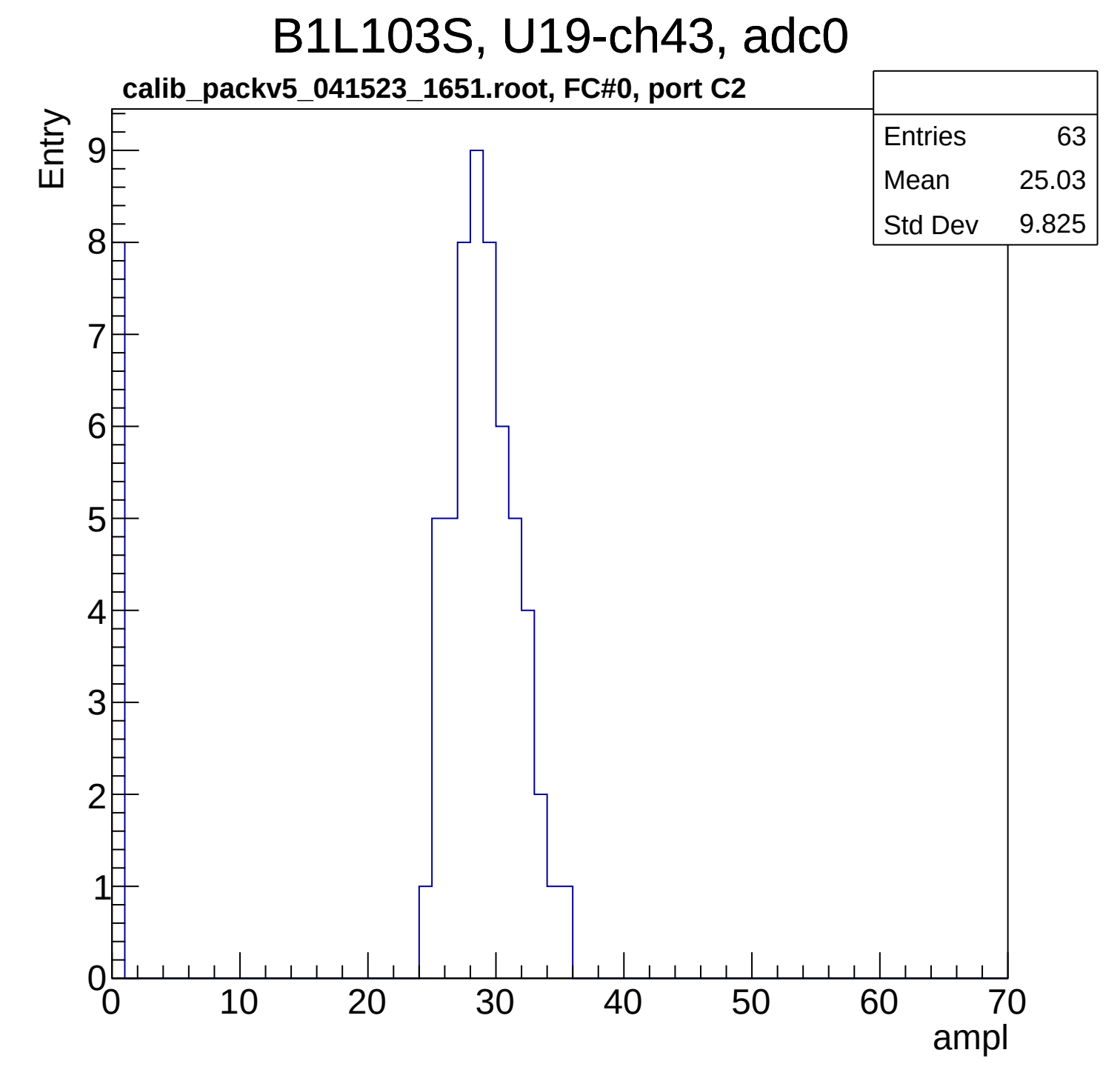
50
60
70
ampl


B1L103S, U19-ch43, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 25.03
Std Dev 9.825
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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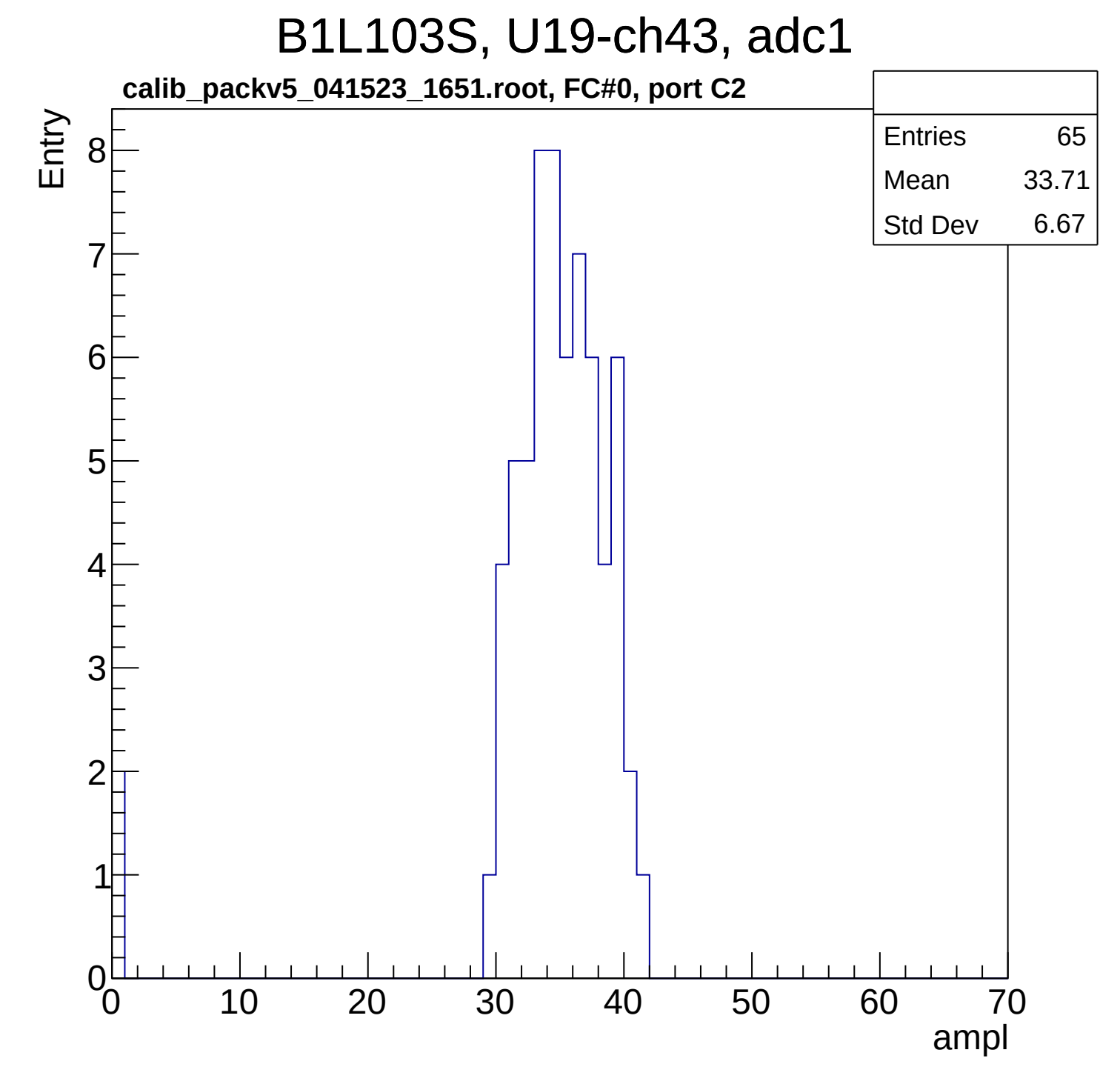
B1L103S, U19-ch43, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 33.71
Std Dev 6.67
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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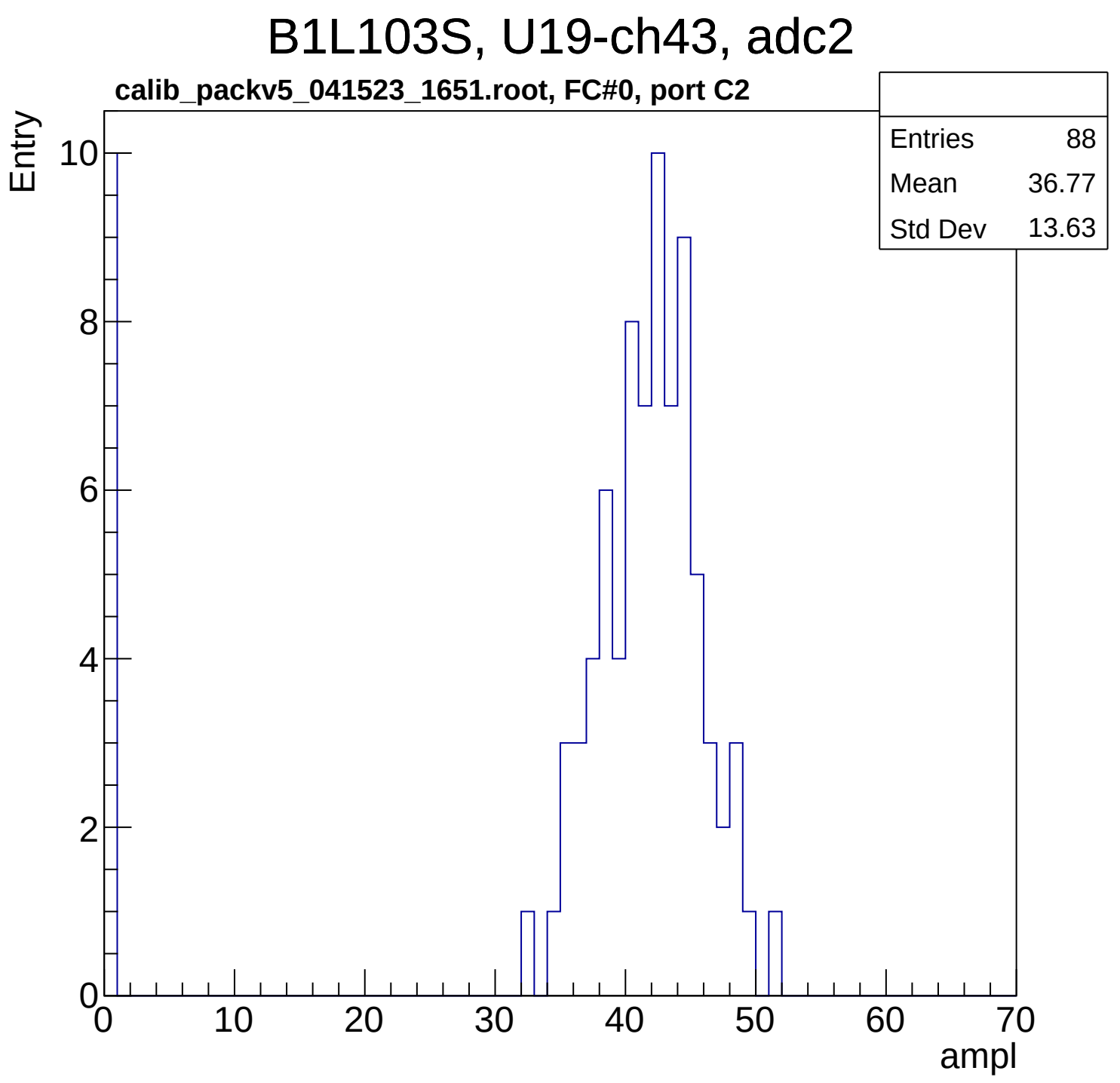
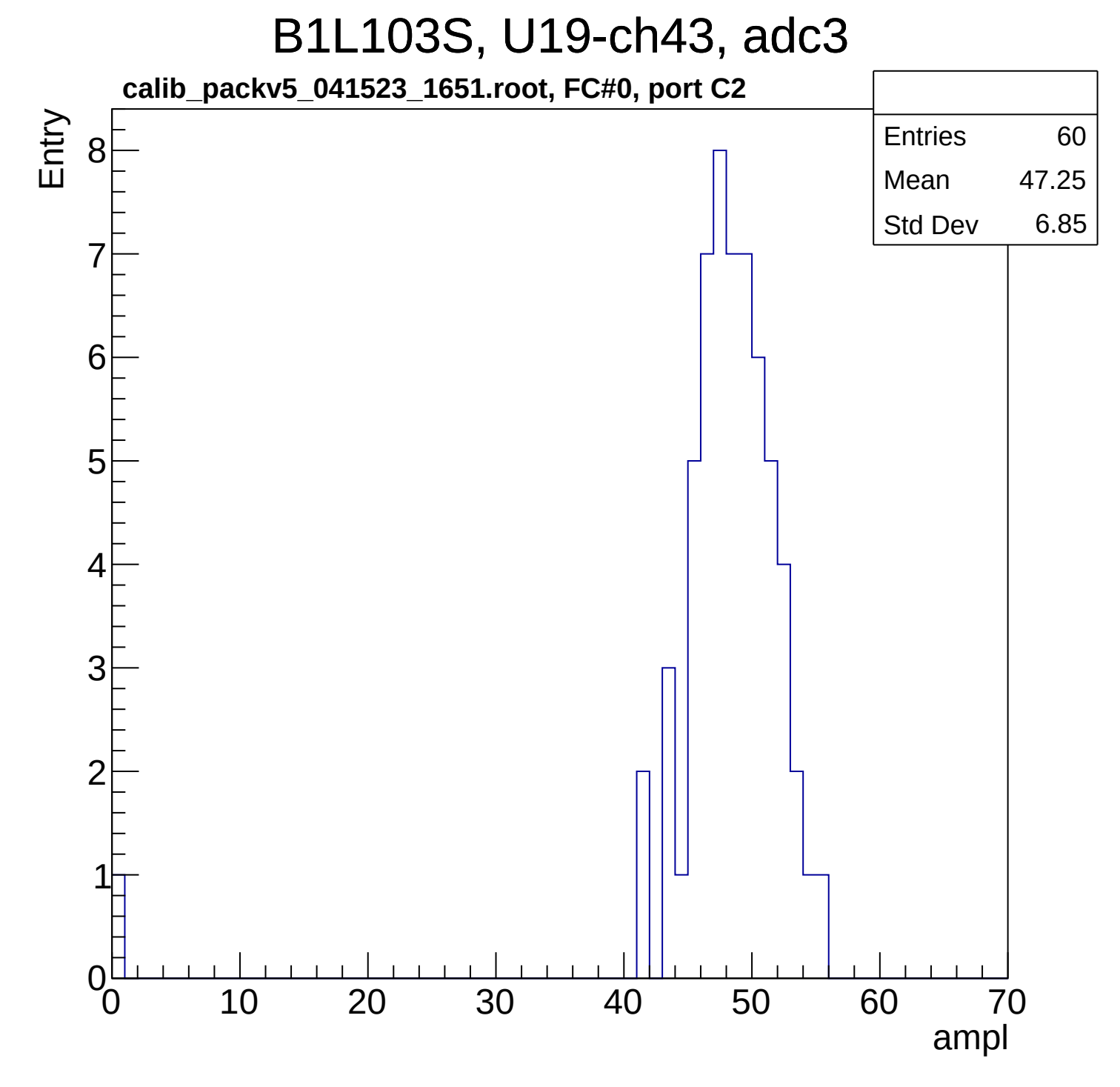
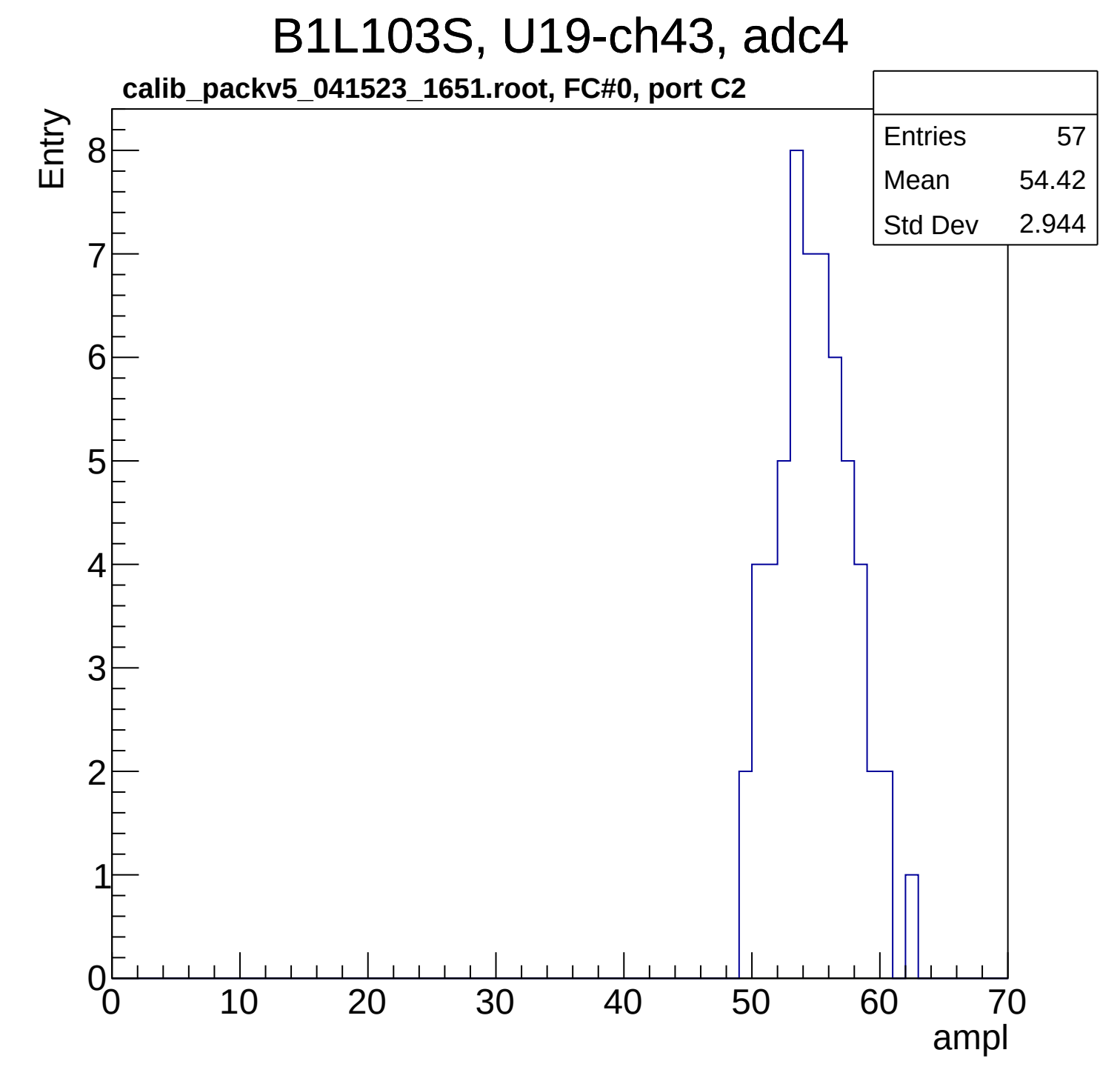

B1L103S, U19-ch43, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 36.77
Std Dev 13.63
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch43, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 47.25
Std Dev 6.85
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch43, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 54.42
Std Dev 2.944
Entry
ampl
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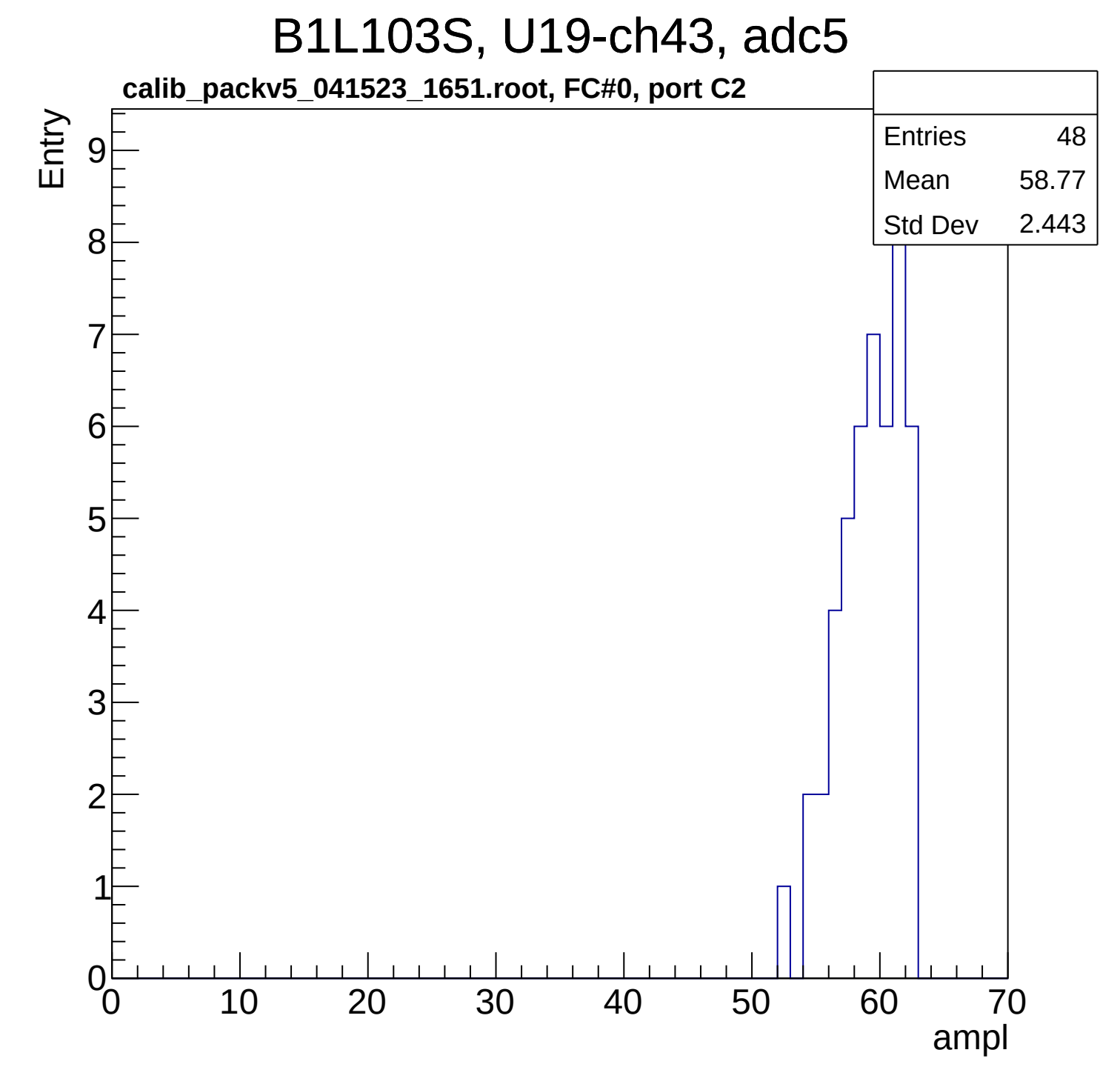
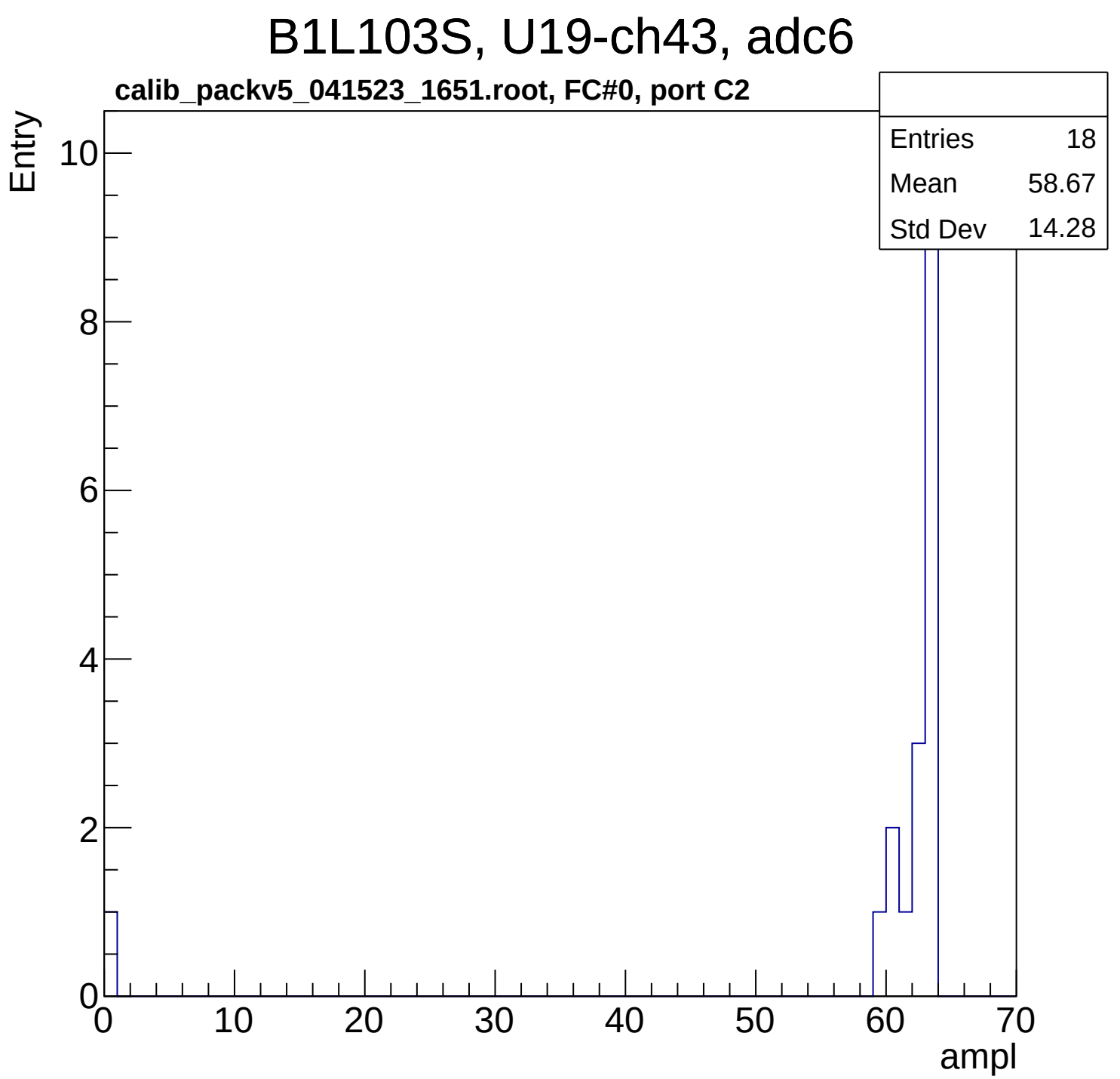
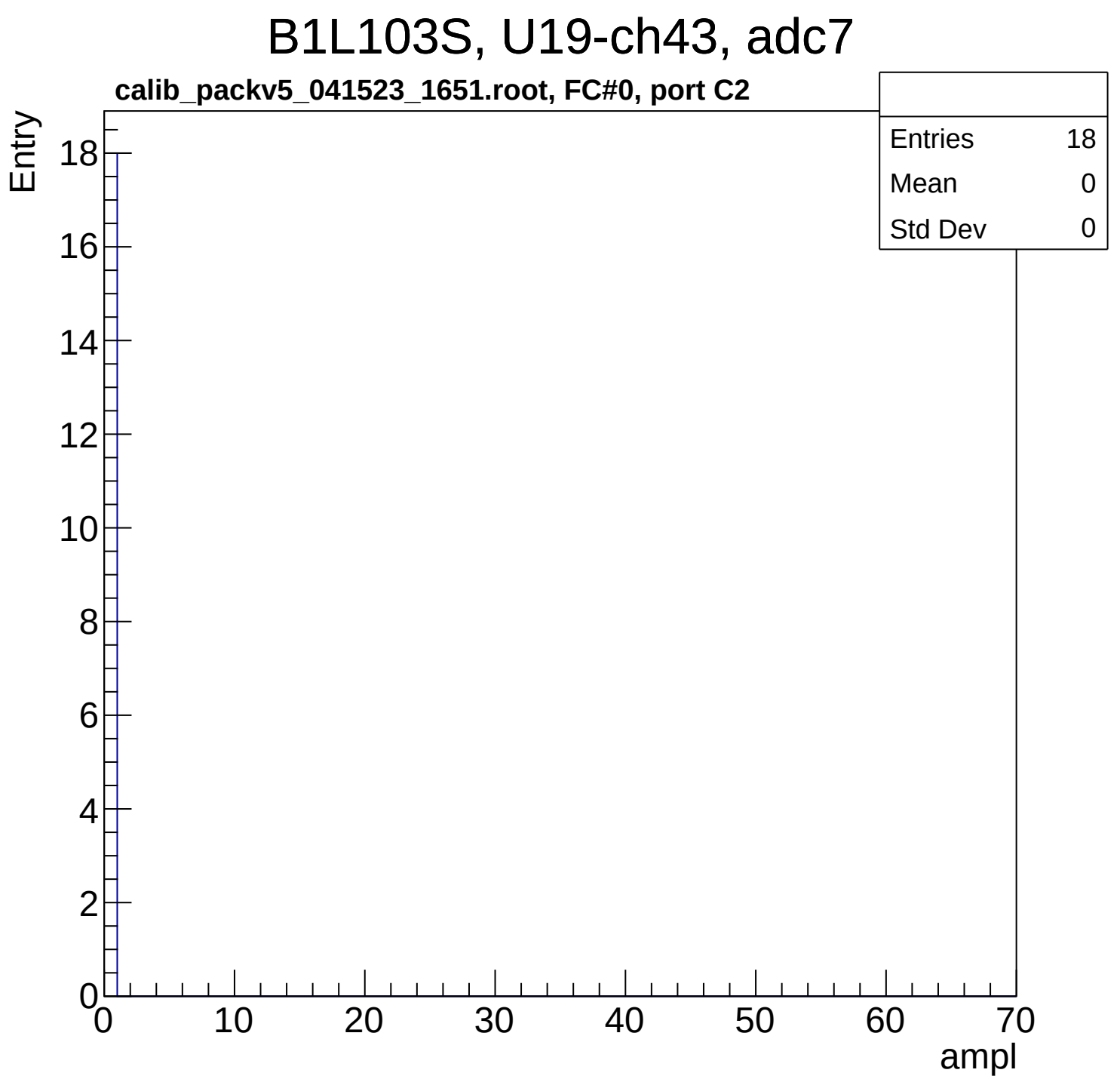
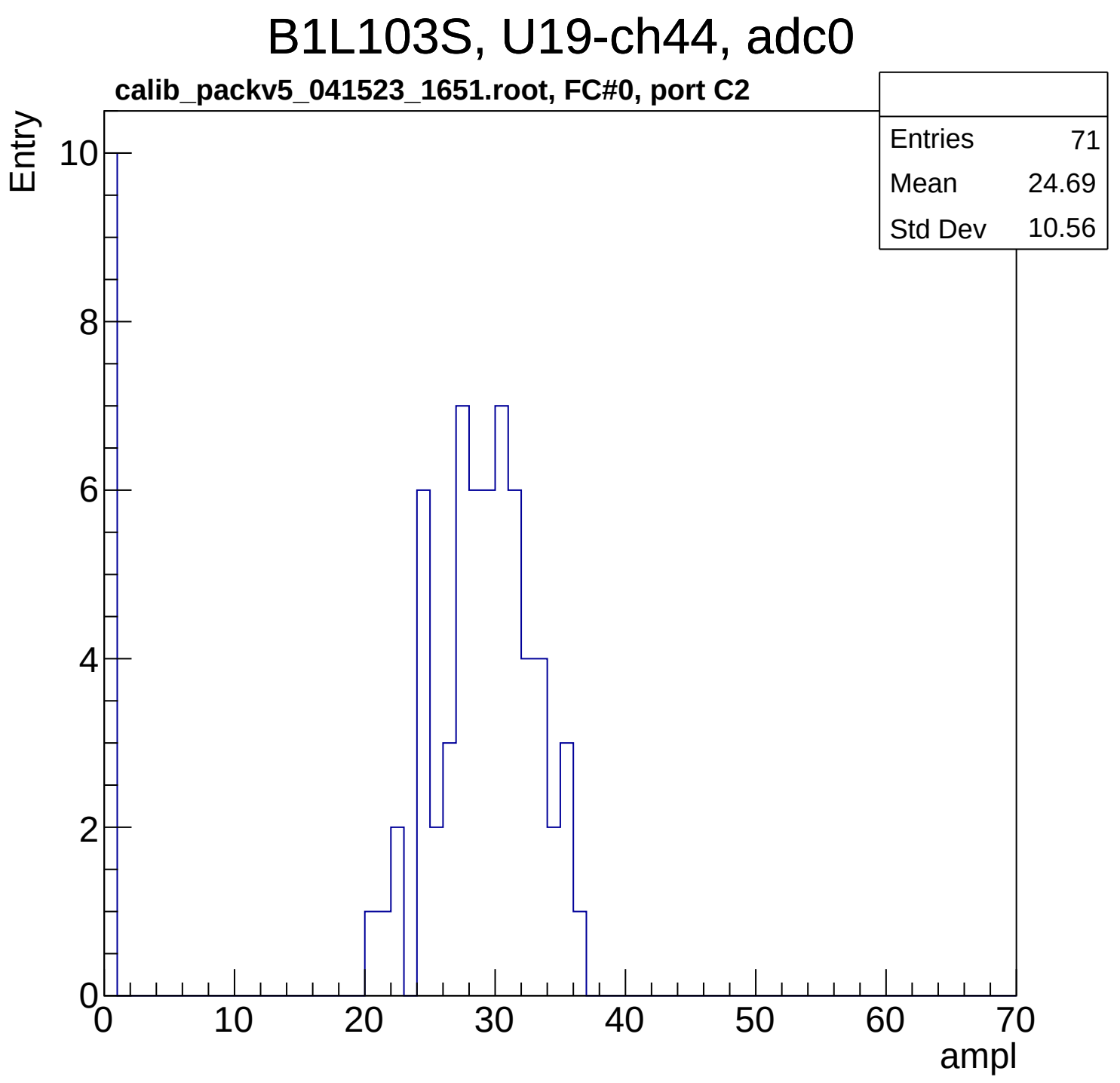
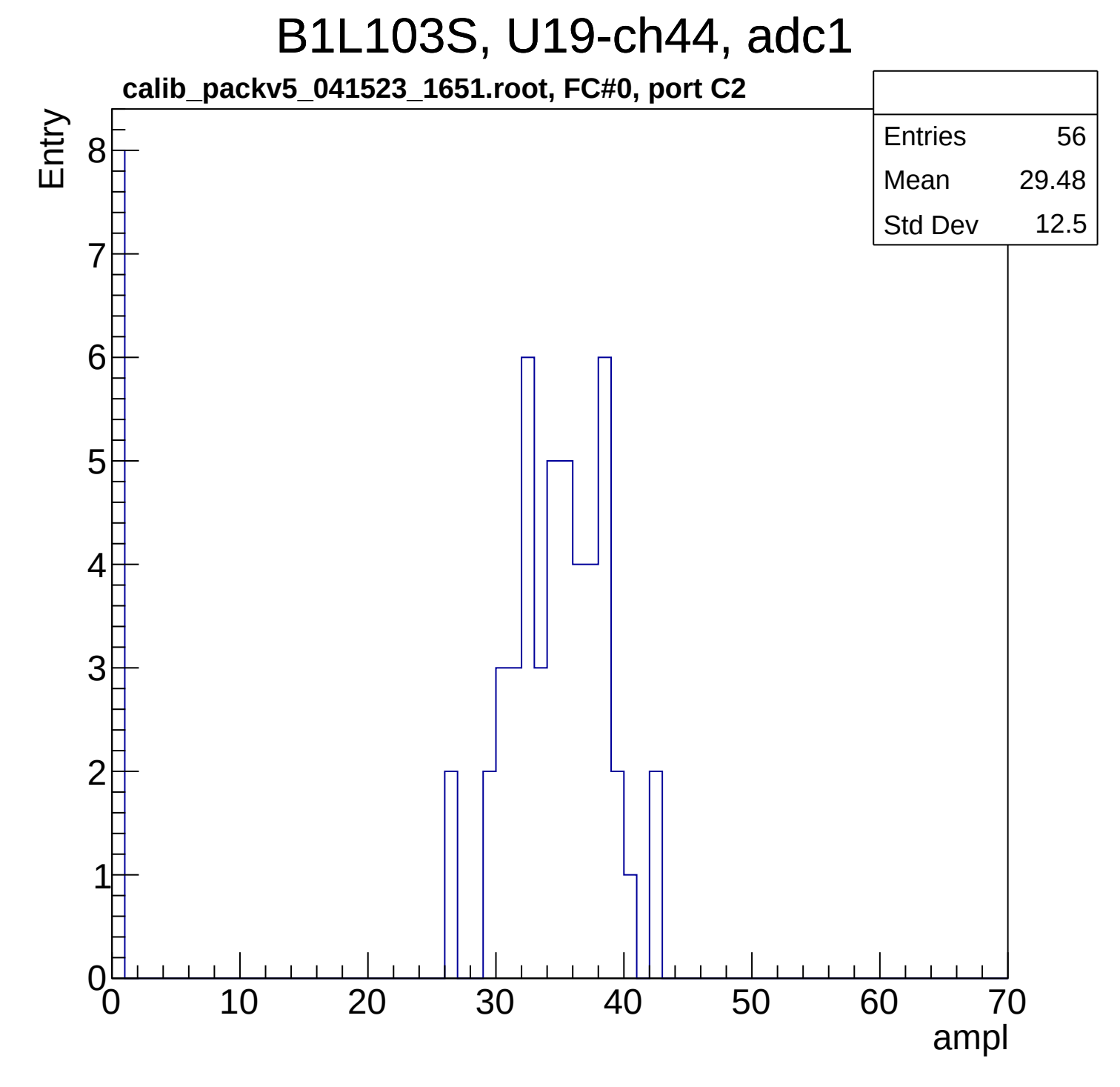
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

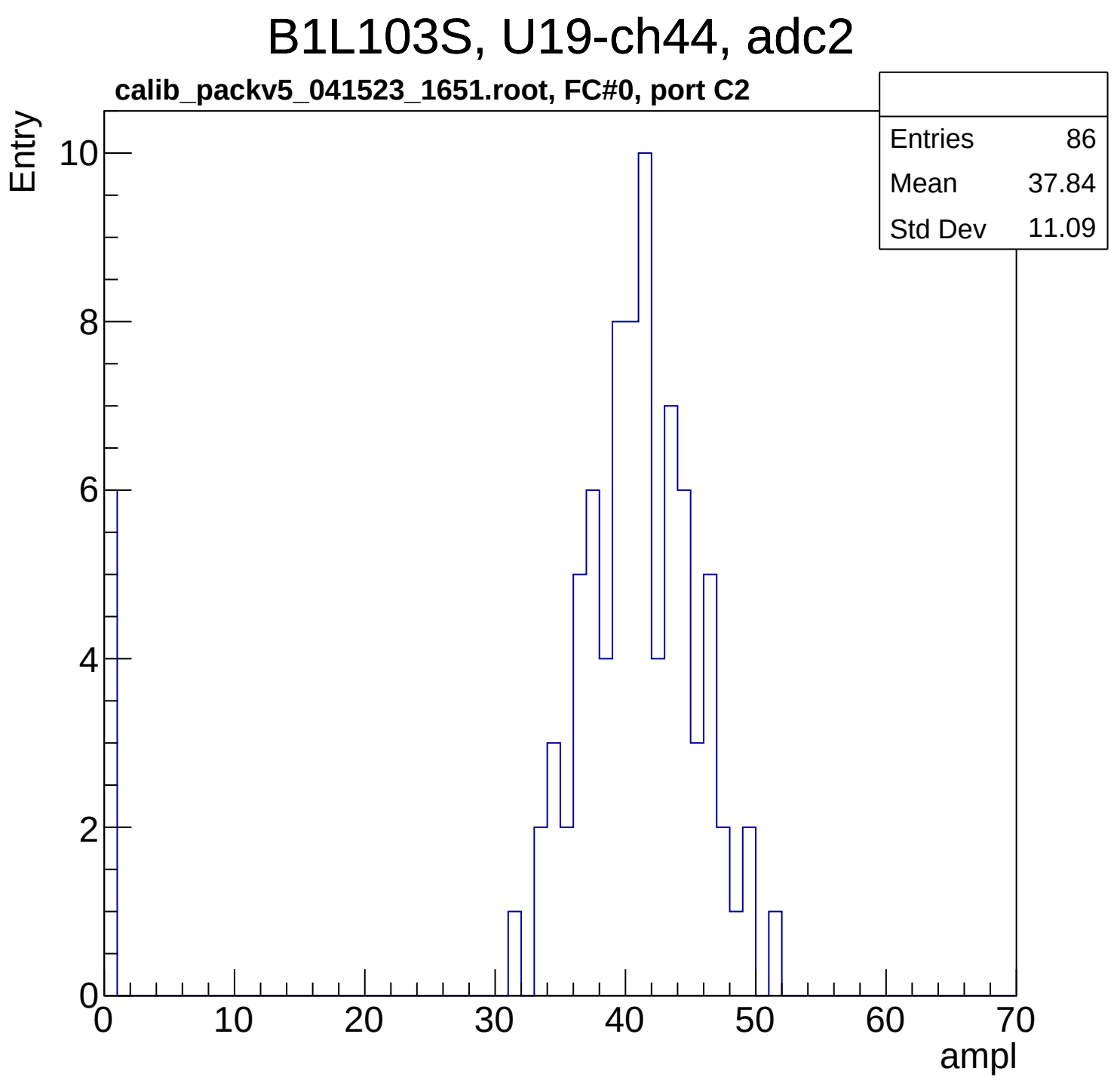

B1L103S, U19-ch43, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 58.77
Std Dev 2.443
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

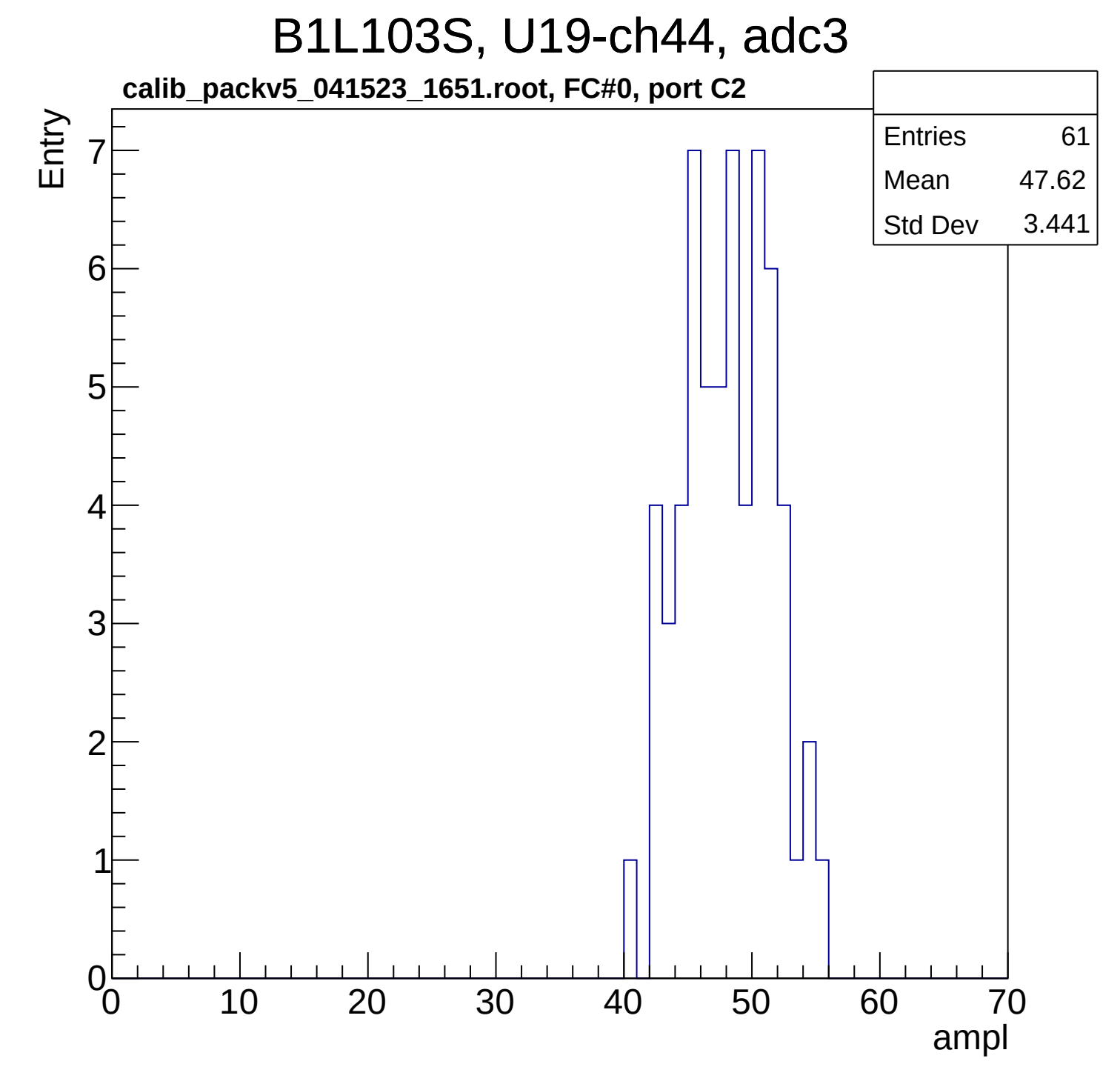

B1L103S, U19-ch43, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 58.67
Std Dev 14.28
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

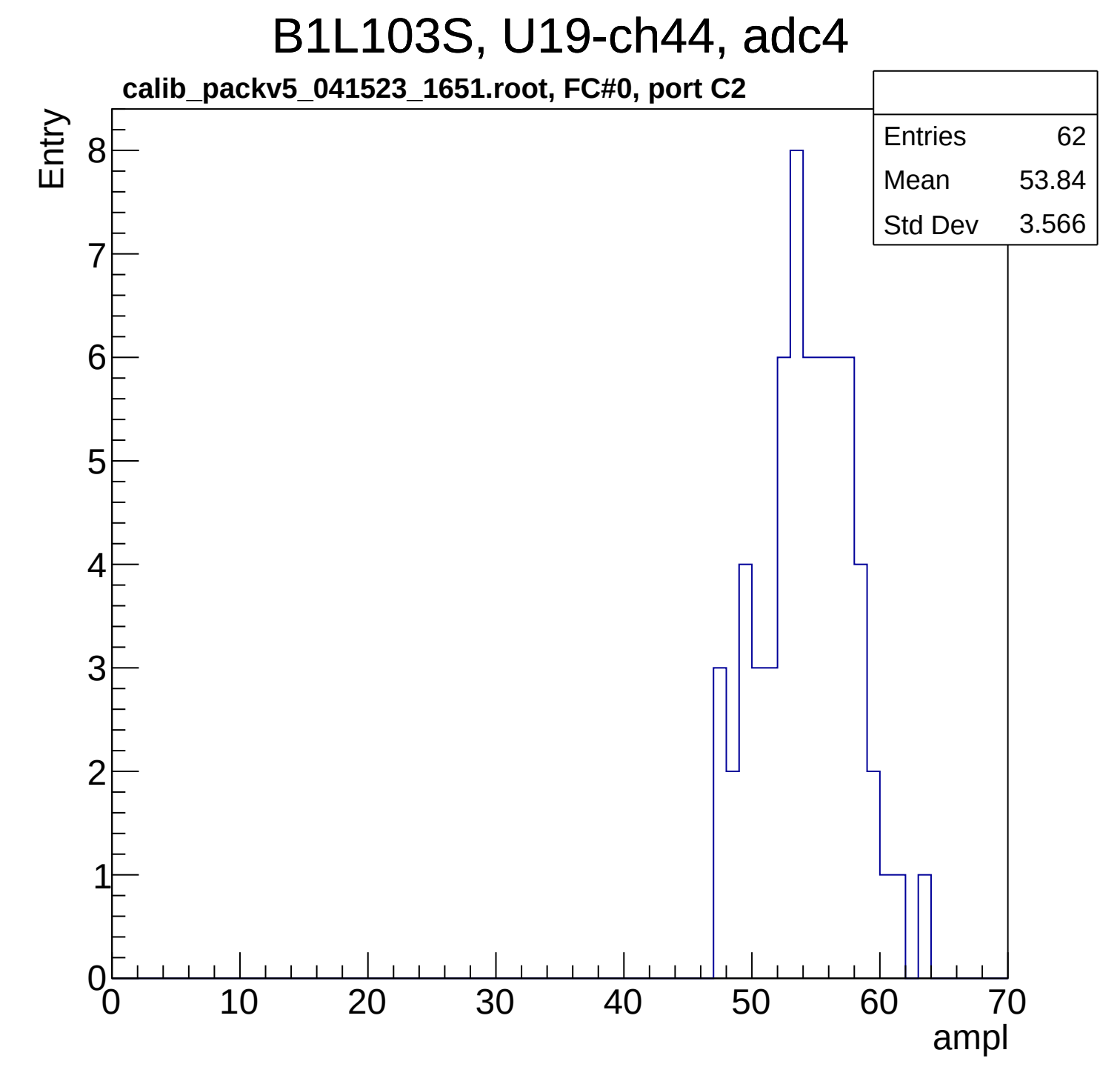

B1L103S, U19-ch43, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

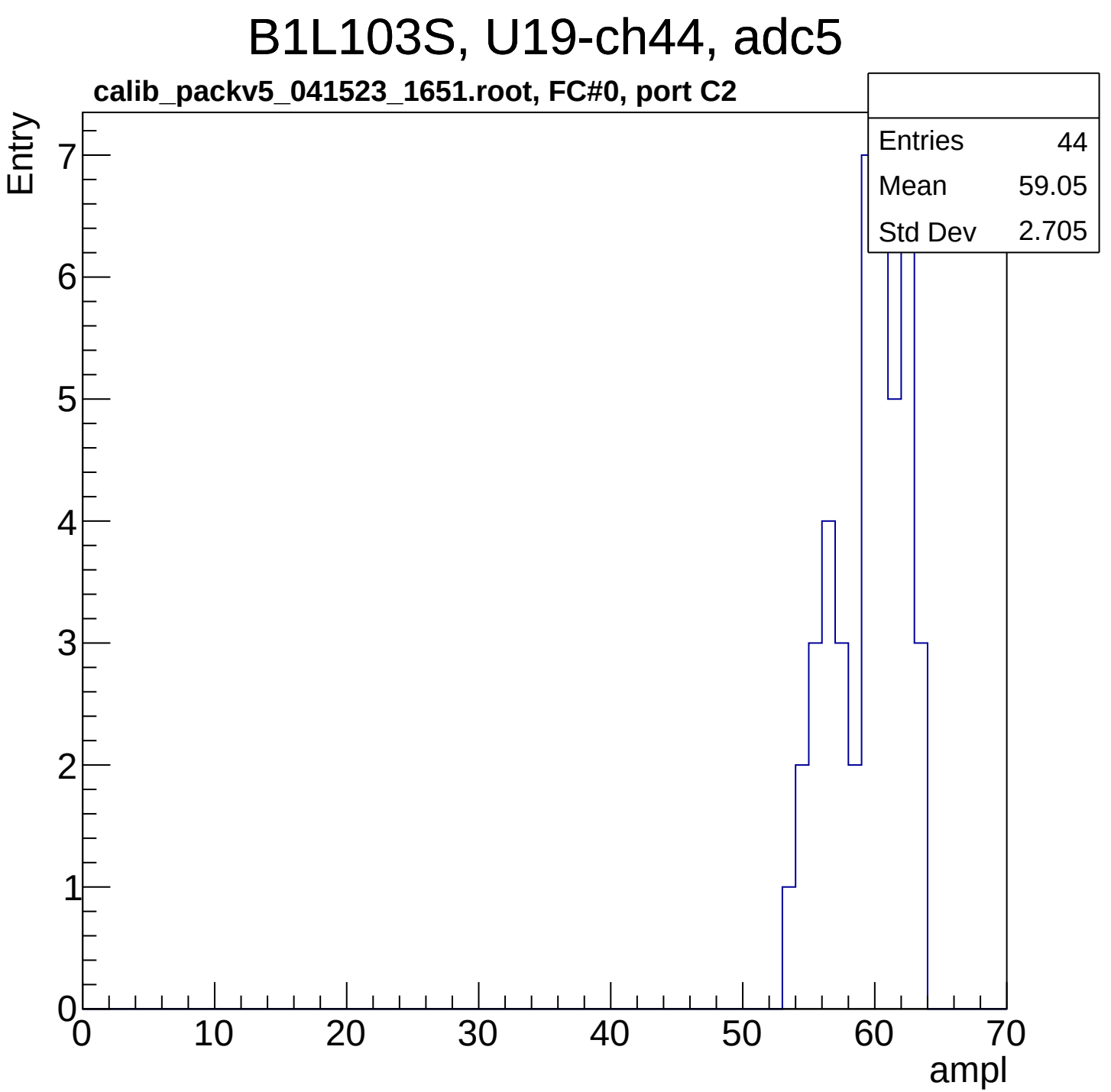

B1L103S, U19-ch44, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 24.69
Std Dev 10.56
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

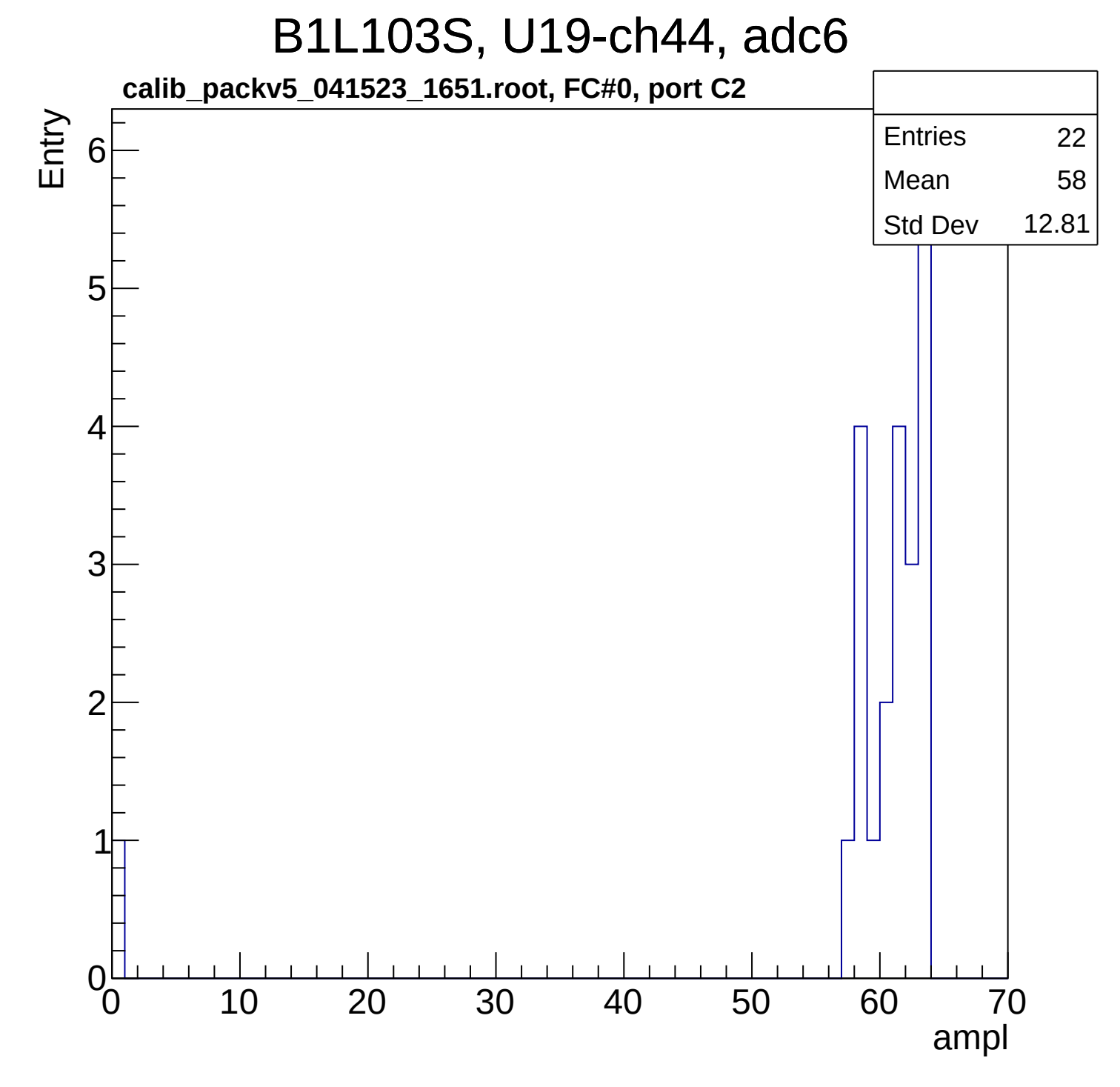

B1L103S, U19-ch44, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 29.48
Std Dev 12.5
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

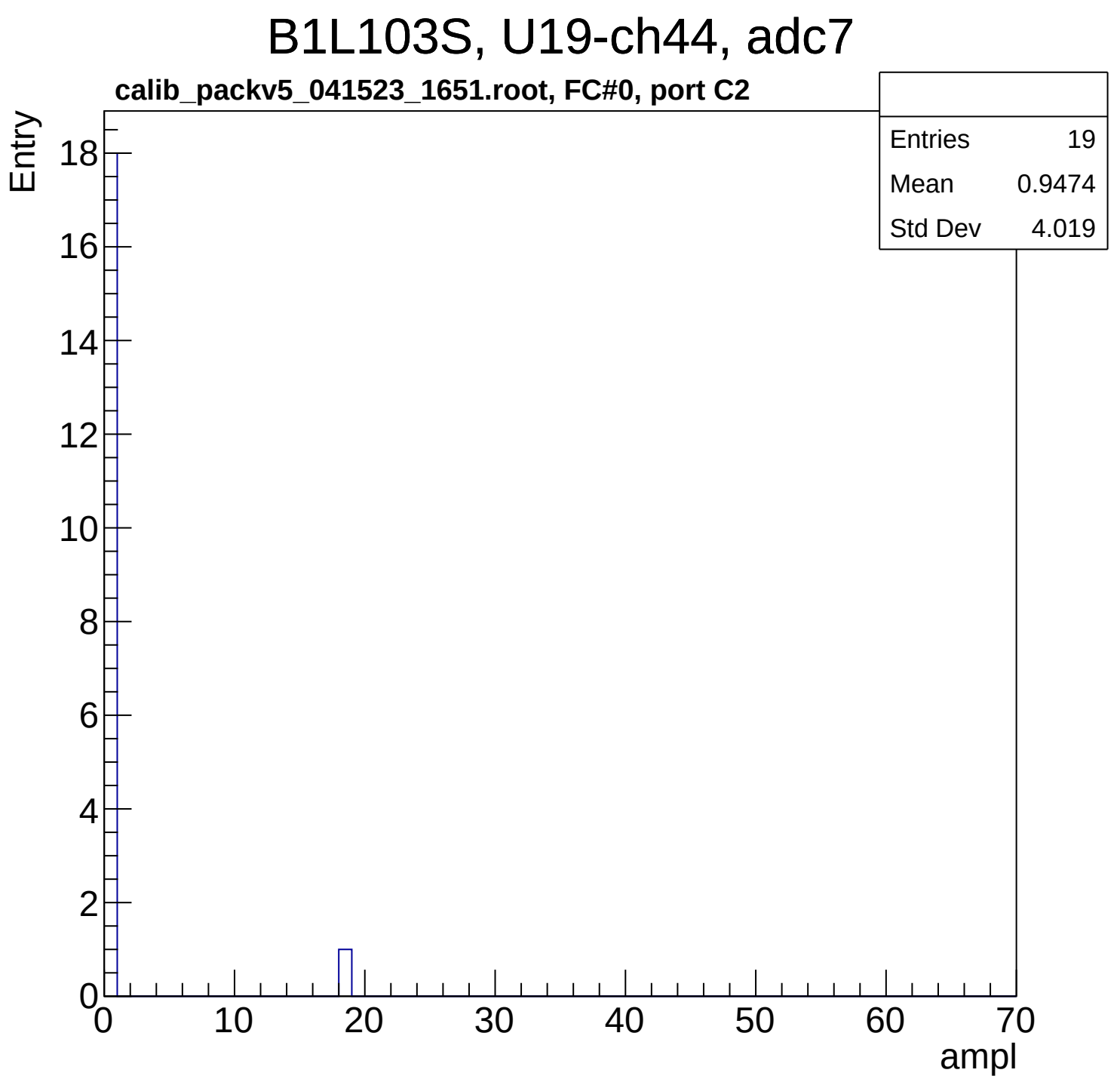

B1L103S, U19-ch44, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 37.84
Std Dev 11.09
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch44, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 47.62
Std Dev 3.441
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch44, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 53.84
Std Dev 3.566
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch44, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 59.05
Std Dev 2.705
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch44, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 58
Std Dev 12.81
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U19-ch44, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0.9474
Std Dev 4.019
Entry
0
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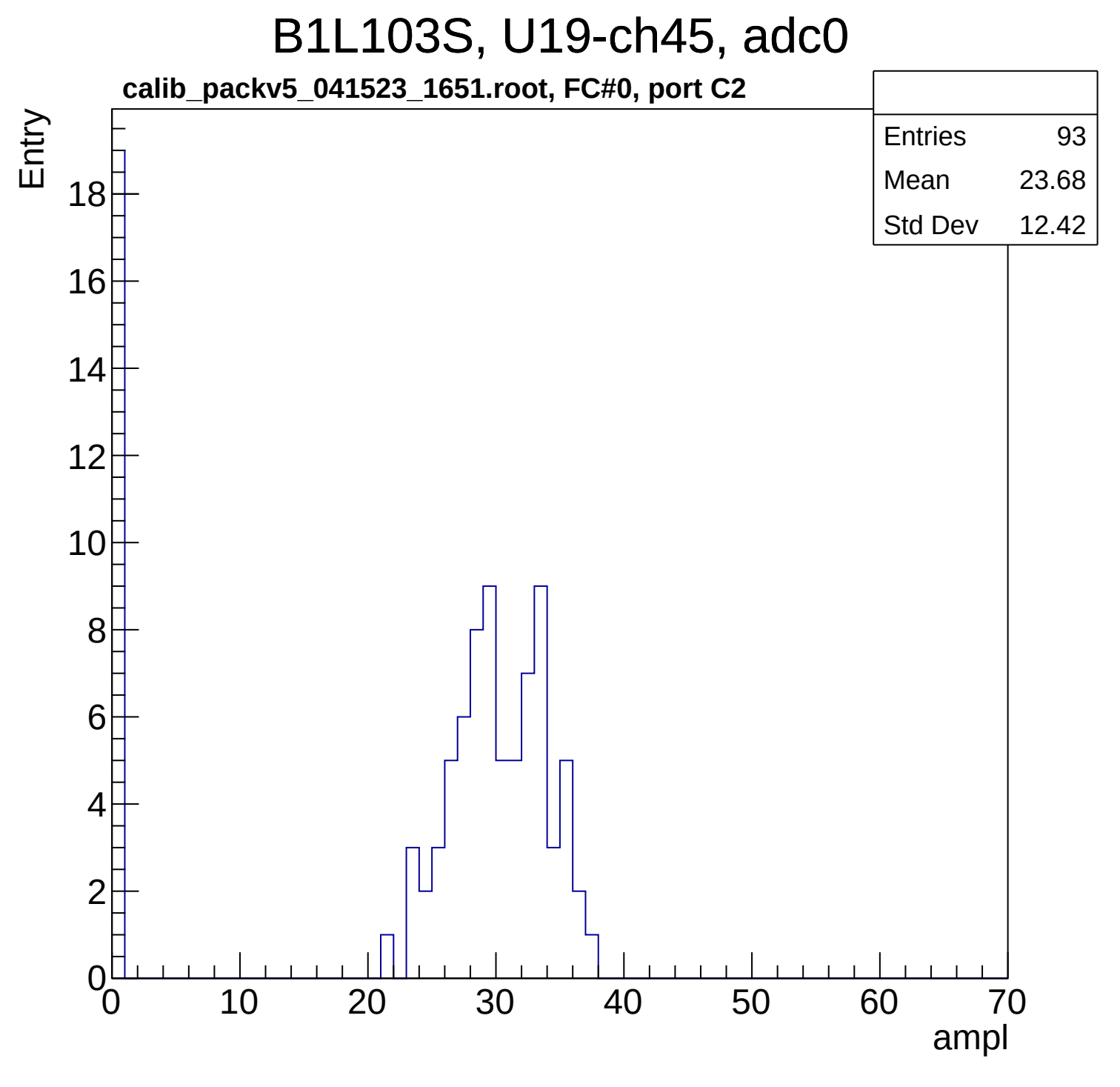
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch45, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 23.68
Std Dev 12.42
Entry
0
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6
8
10
12
14
16
18
0
10
20
30
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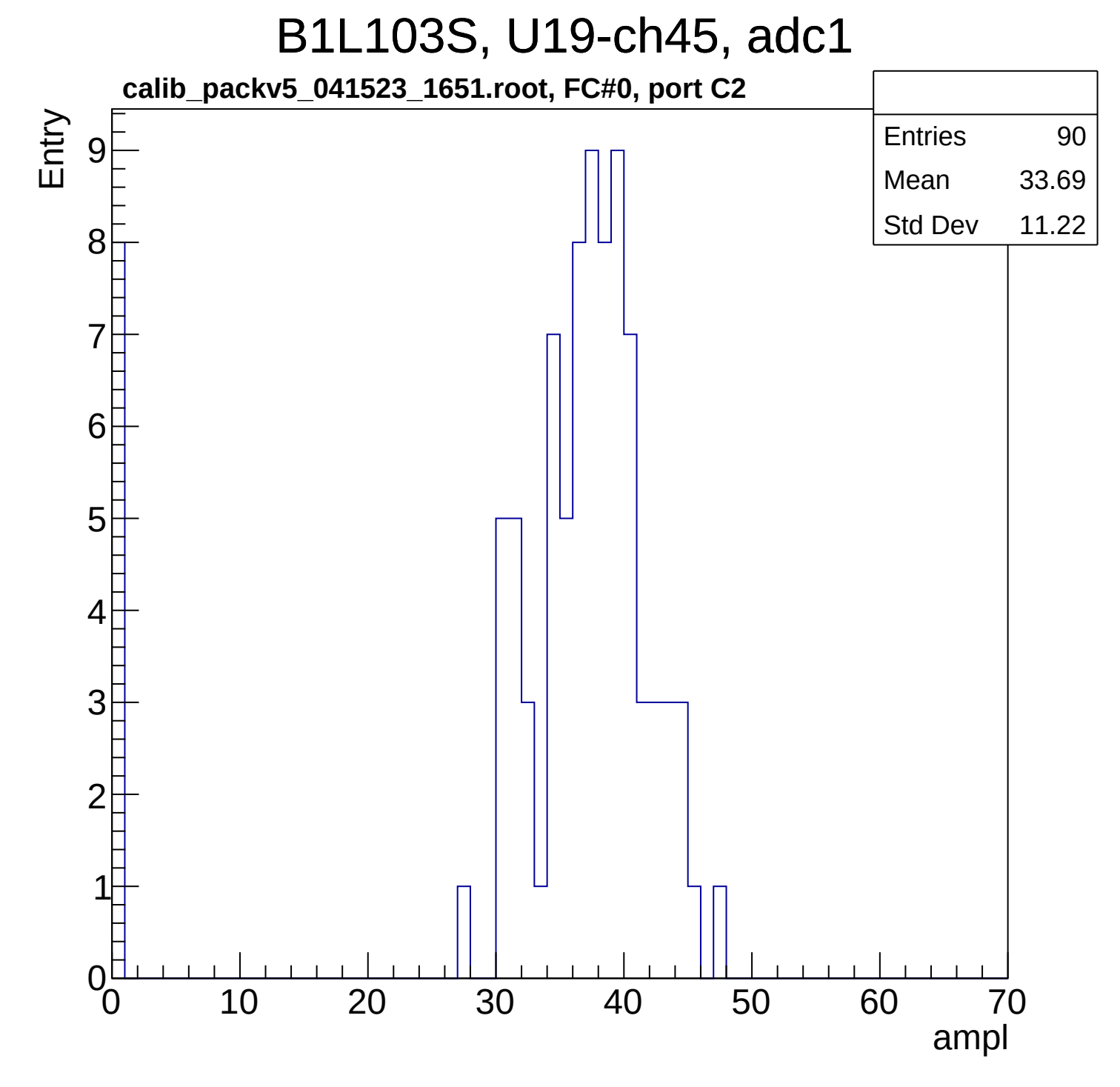
50
60
70
ampl


B1L103S, U19-ch45, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 33.69
Std Dev 11.22
Entry
ampl
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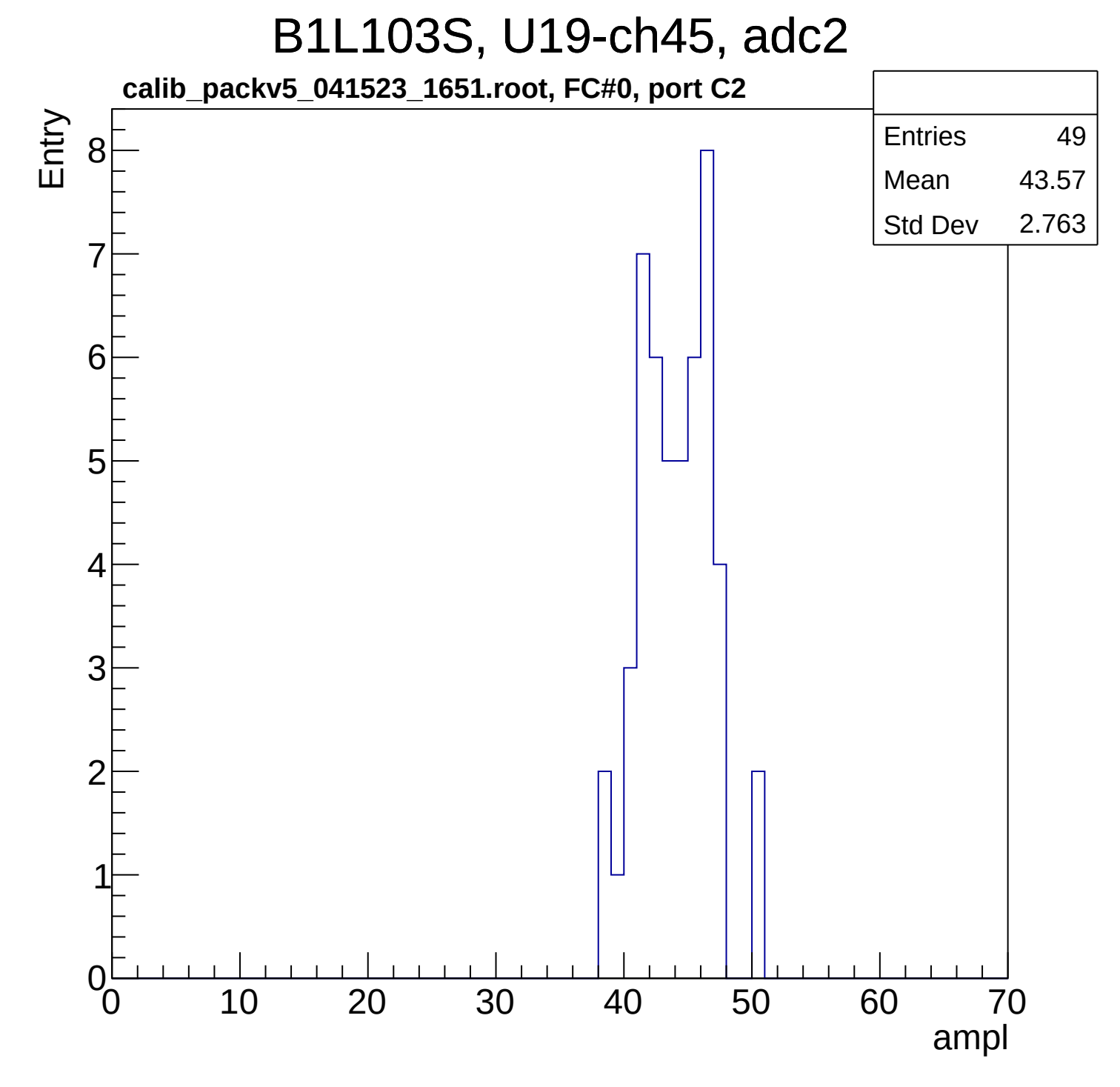
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch45, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 43.57
Std Dev 2.763
Entry
ampl
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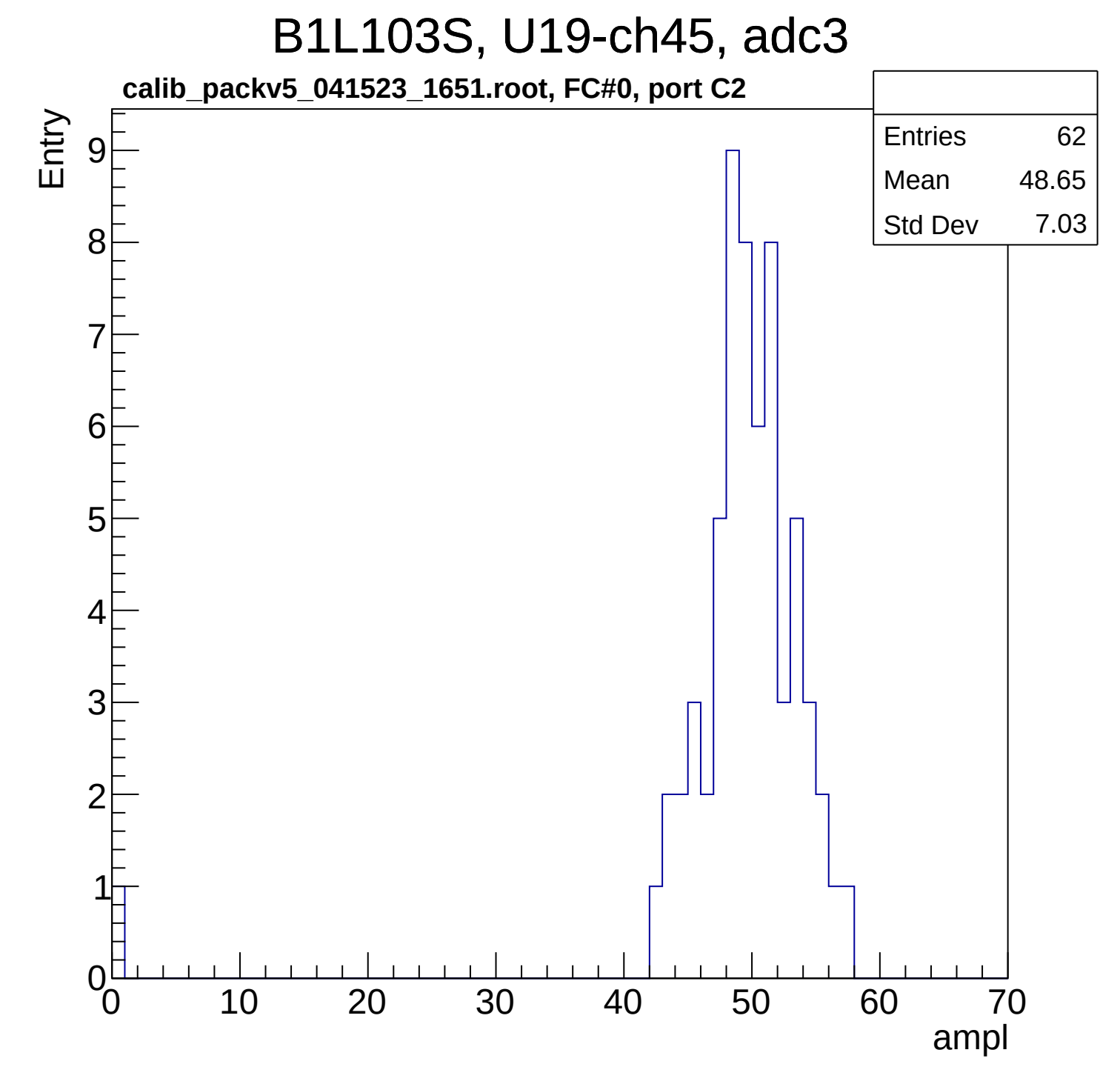
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch45, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 48.65
Std Dev 7.03
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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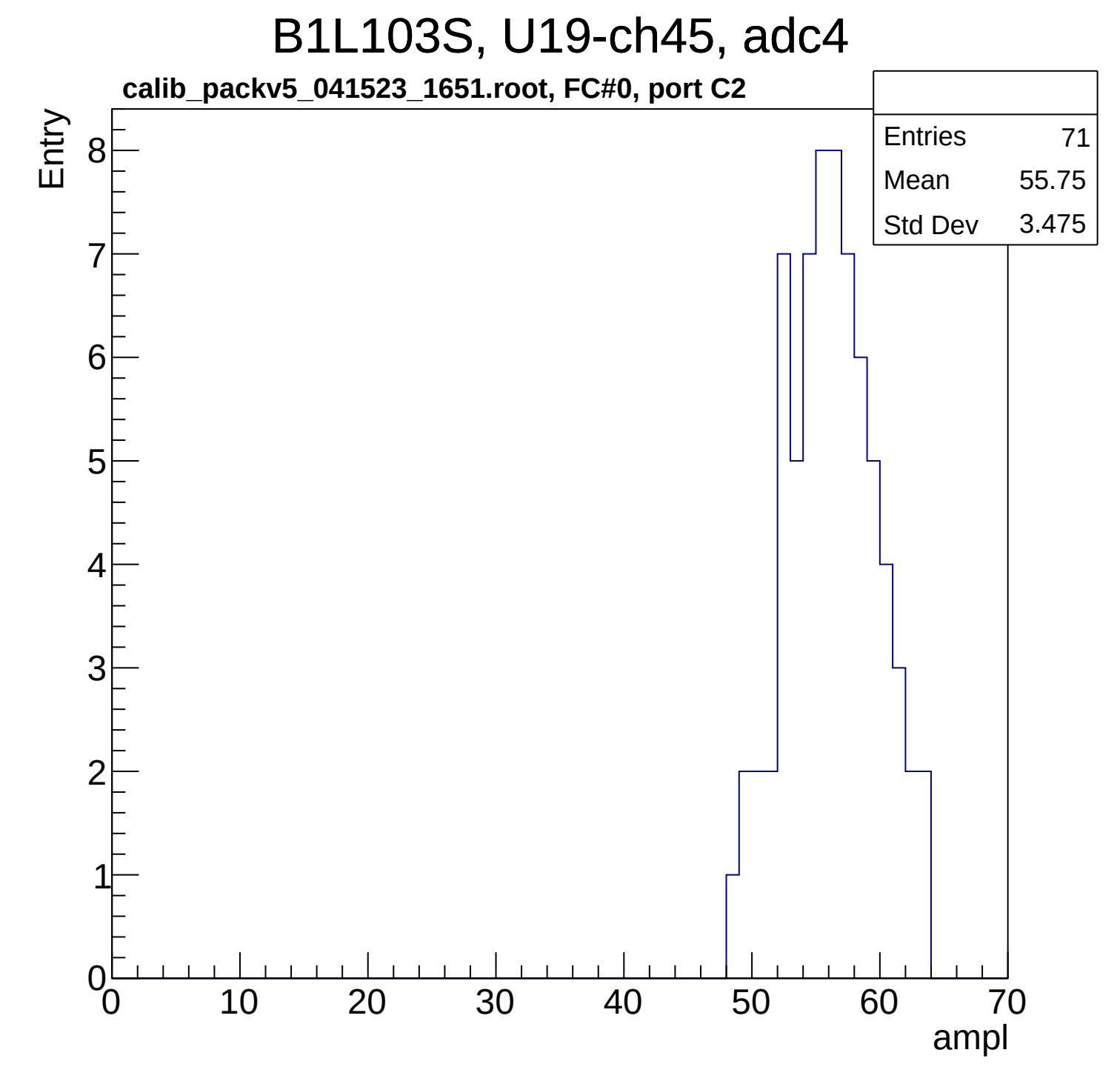
40
50
60
70


B1L103S, U19-ch45, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 55.75
Std Dev 3.475
Entry
ampl
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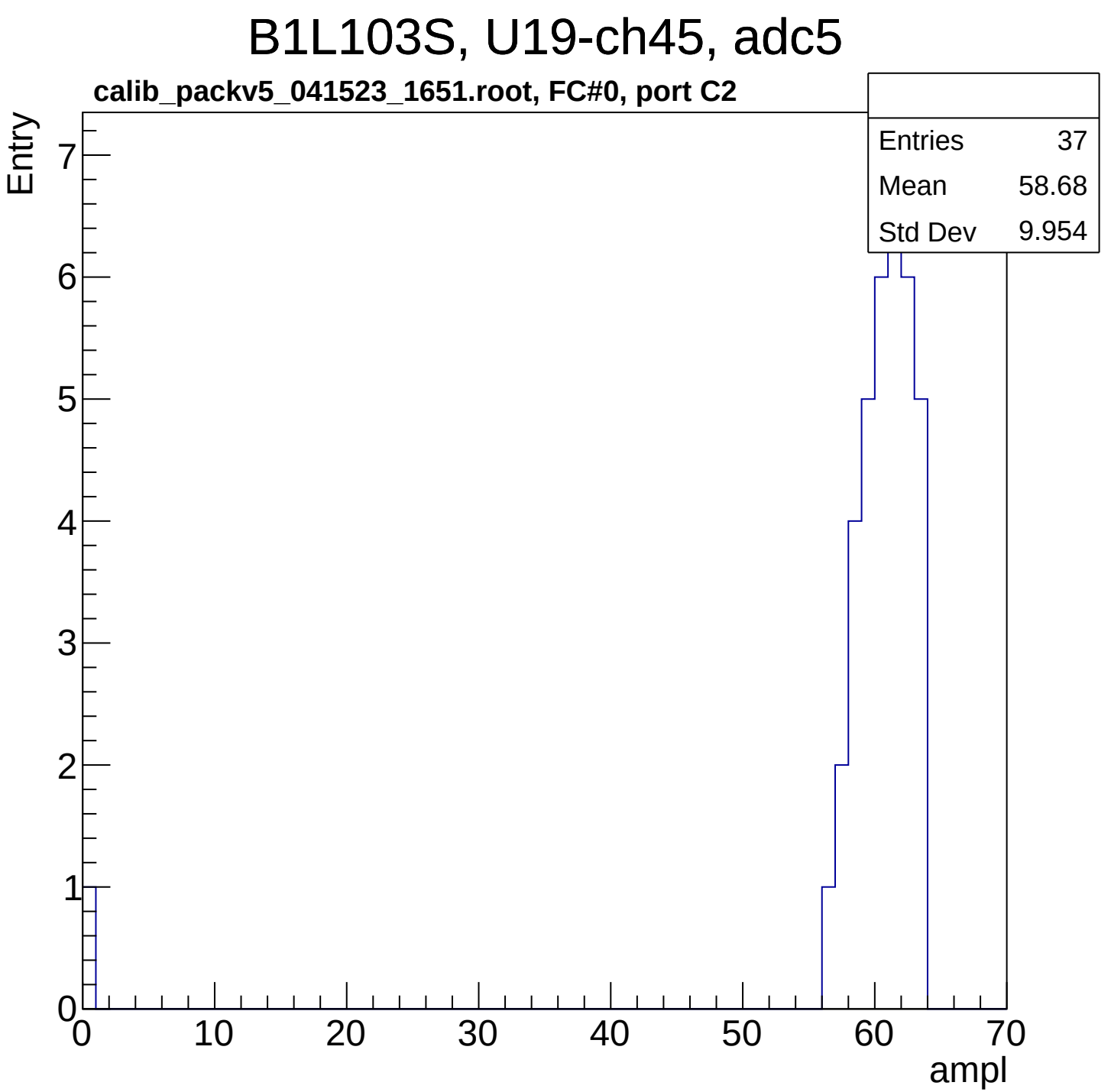
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch45, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 58.68
Std Dev 9.954
Entry
ampl
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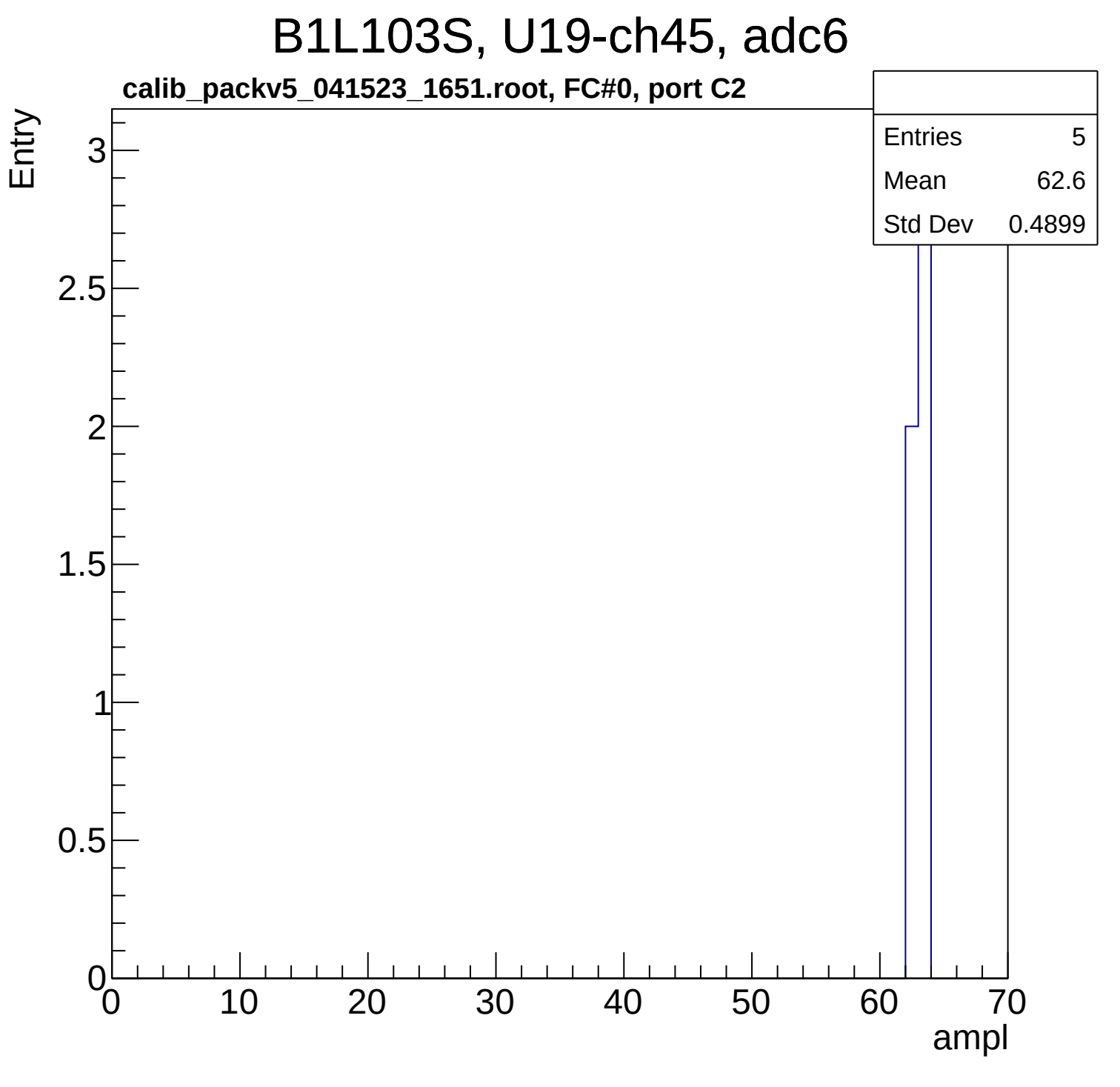
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch45, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 62.6
Std Dev 0.4899
Entry
ampl
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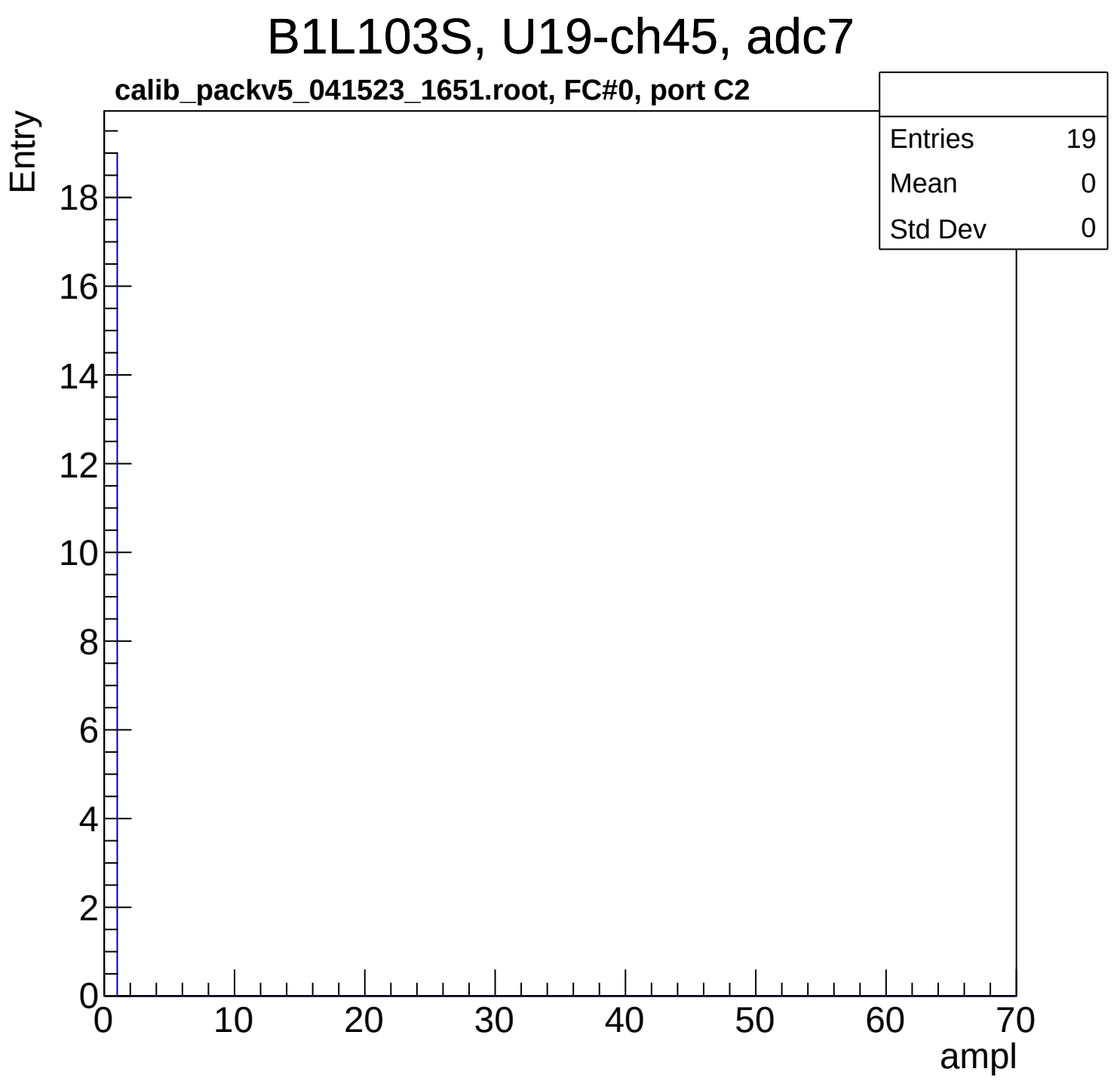
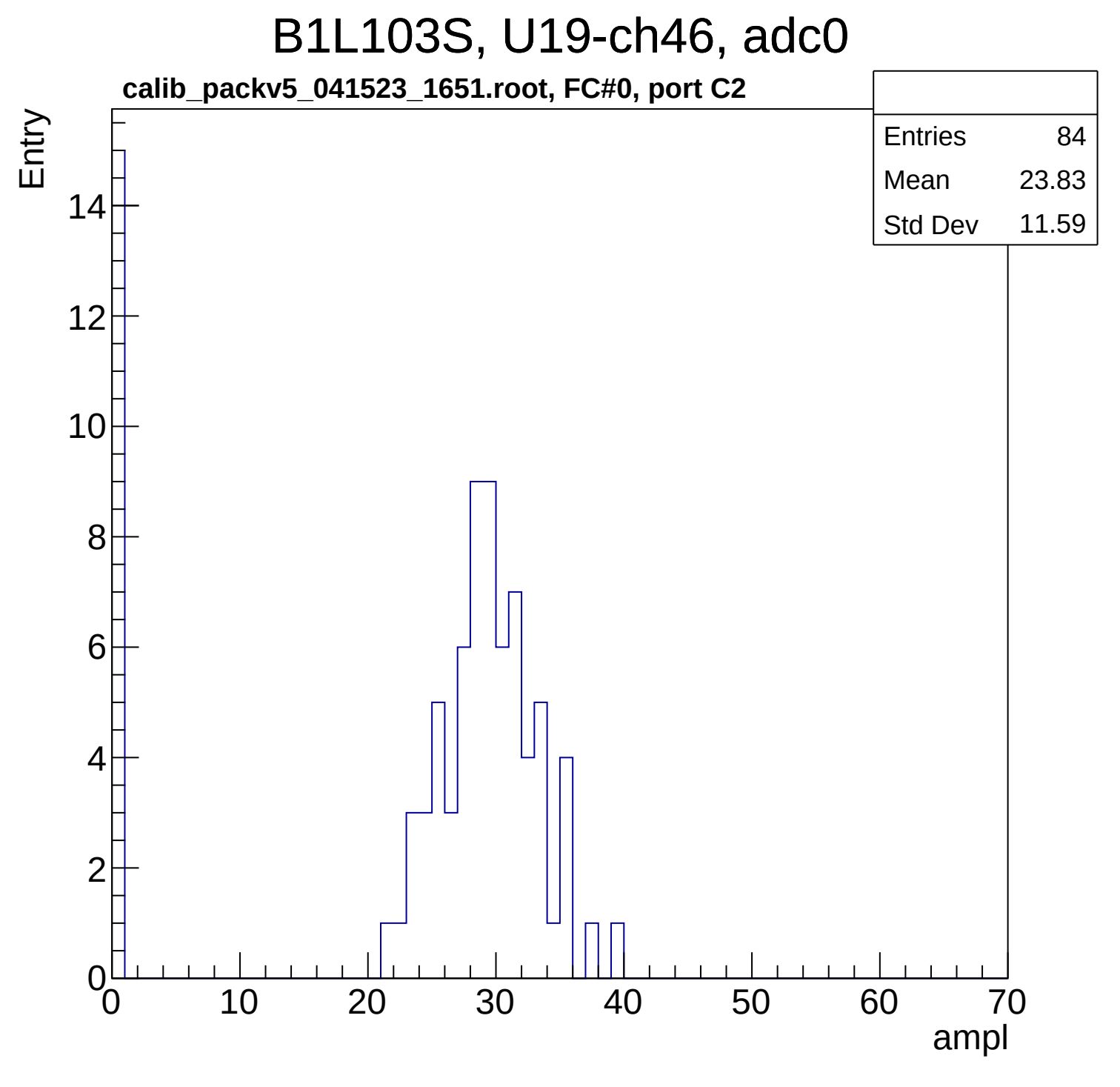
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U19-ch45, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch46, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 23.83
Std Dev 11.59
Entry
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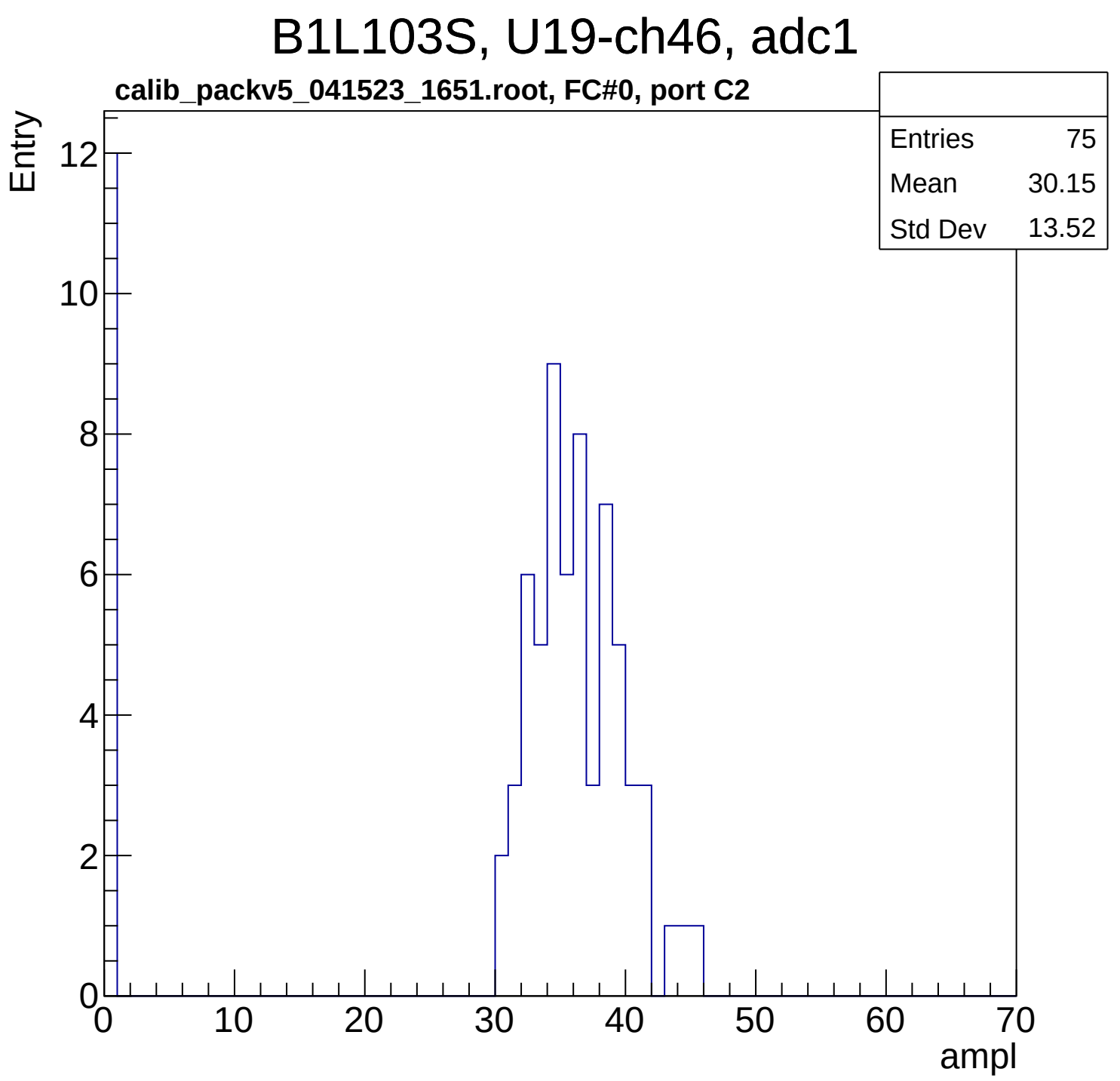
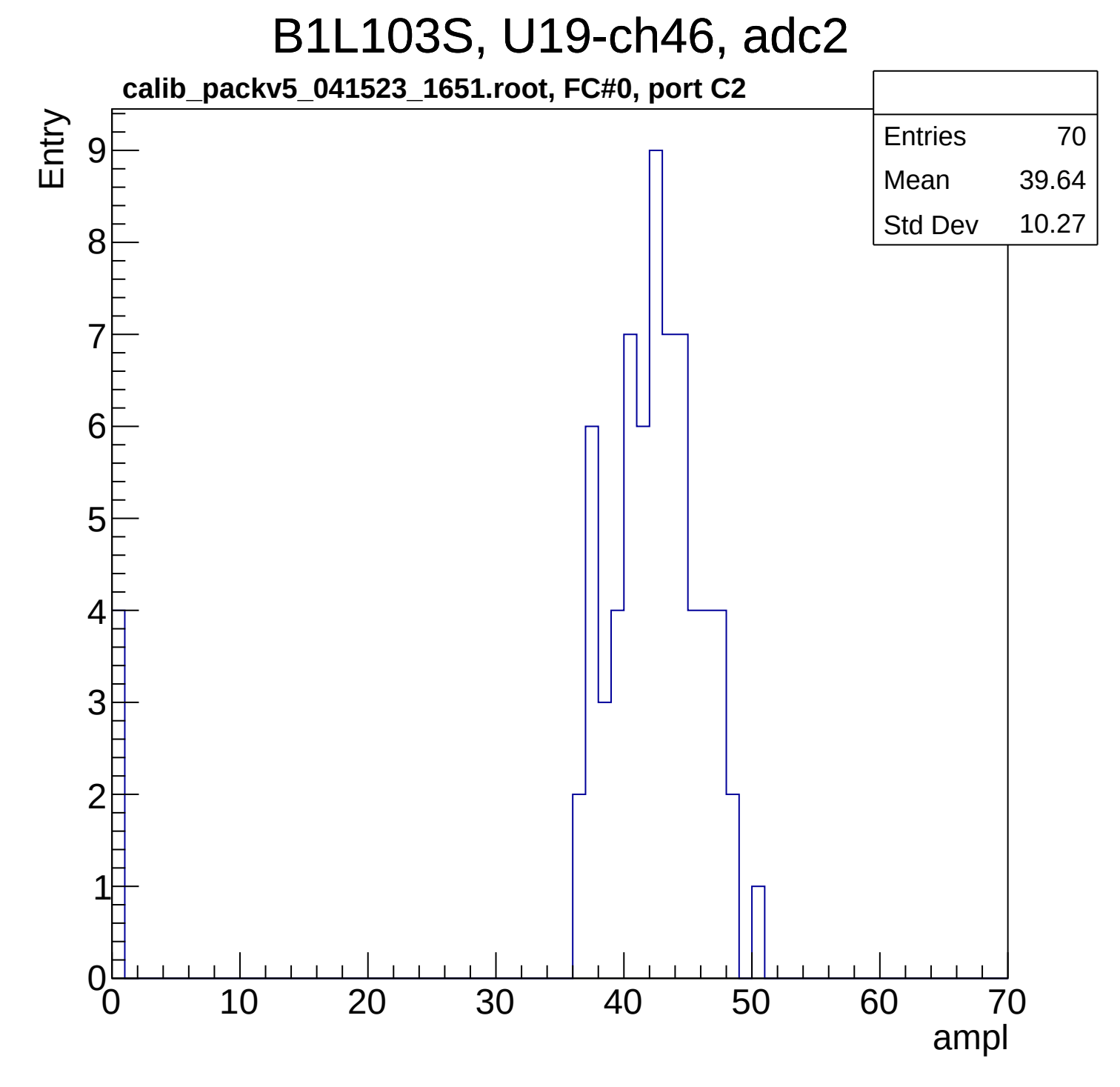
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch46, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 30.15
Std Dev 13.52
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch46, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 39.64
Std Dev 10.27
Entry
ampl
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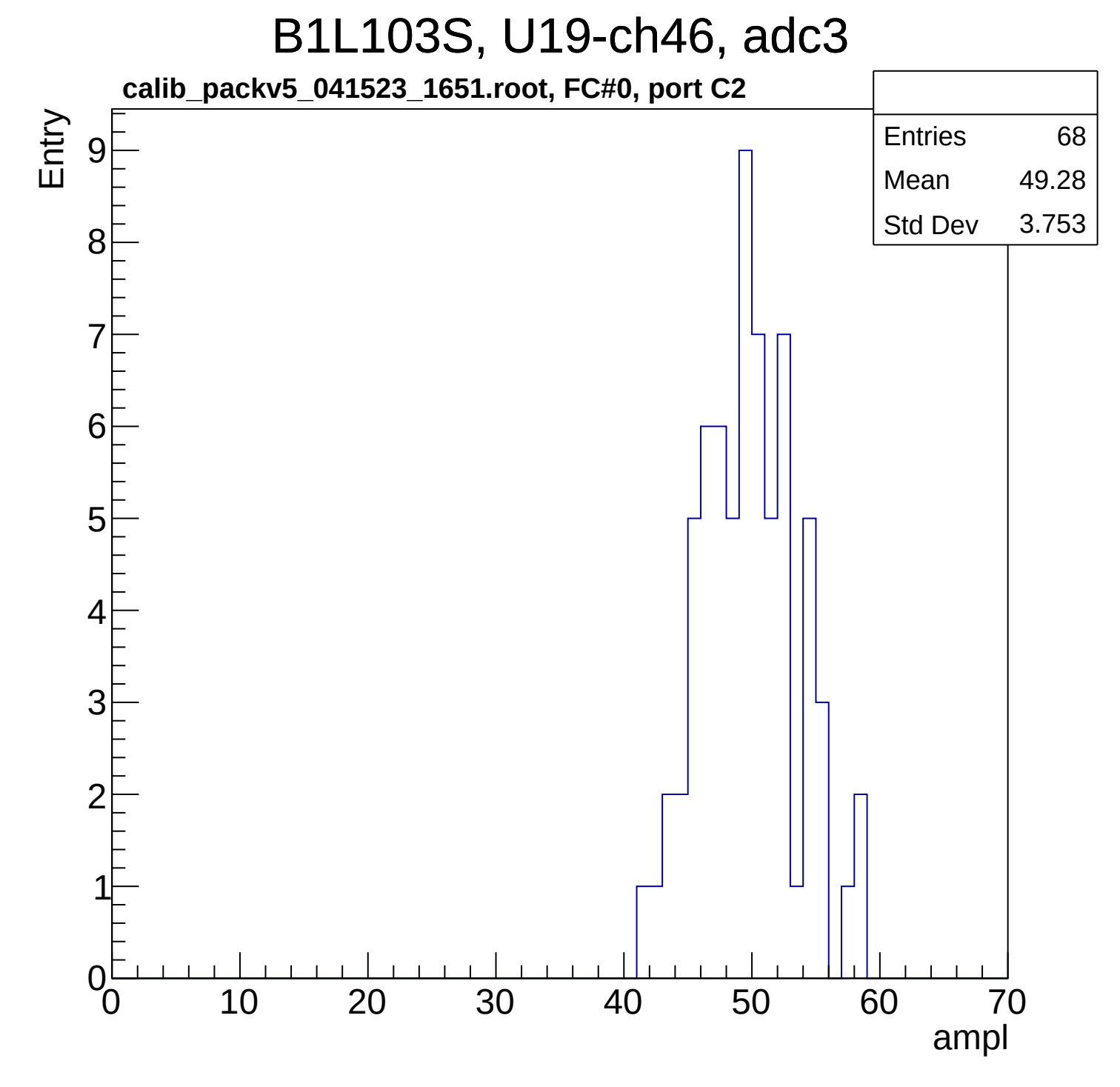
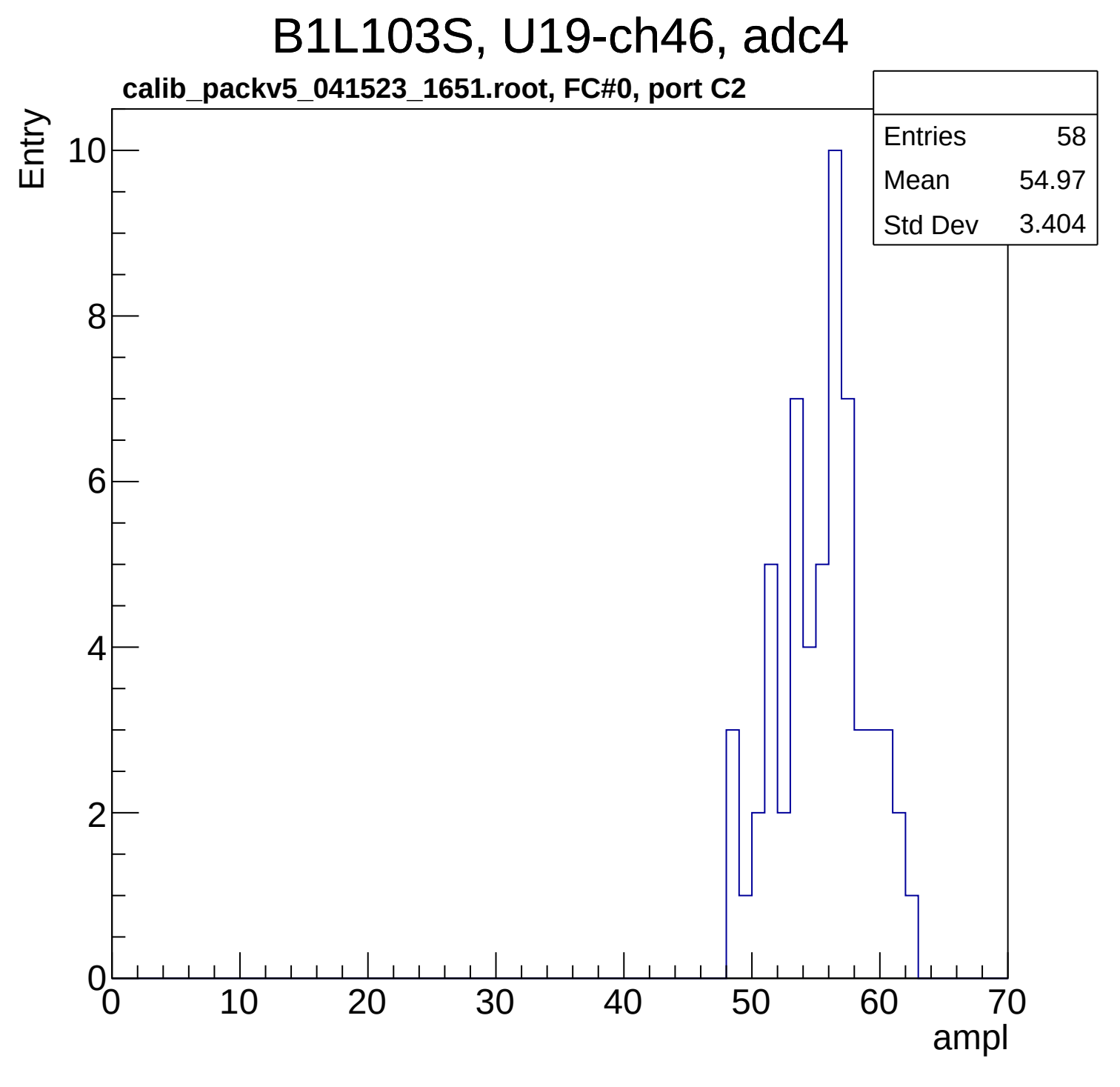
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch46, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 49.28
Std Dev 3.753
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch46, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 54.97
Std Dev 3.404
Entry
ampl
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2
4
6
8
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0
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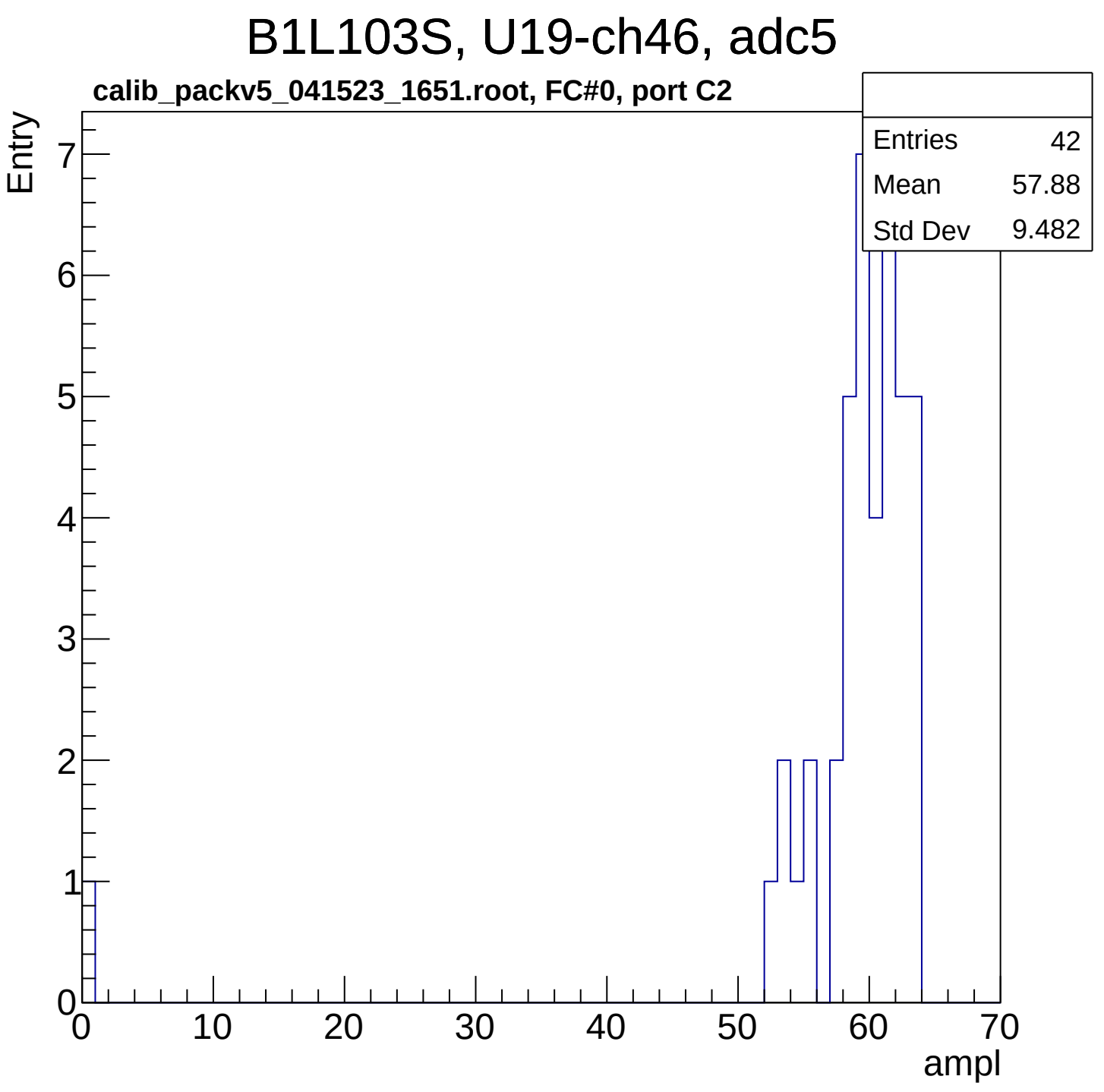
B1L103S, U19-ch46, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 57.88
Std Dev 9.482
Entry
ampl
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4
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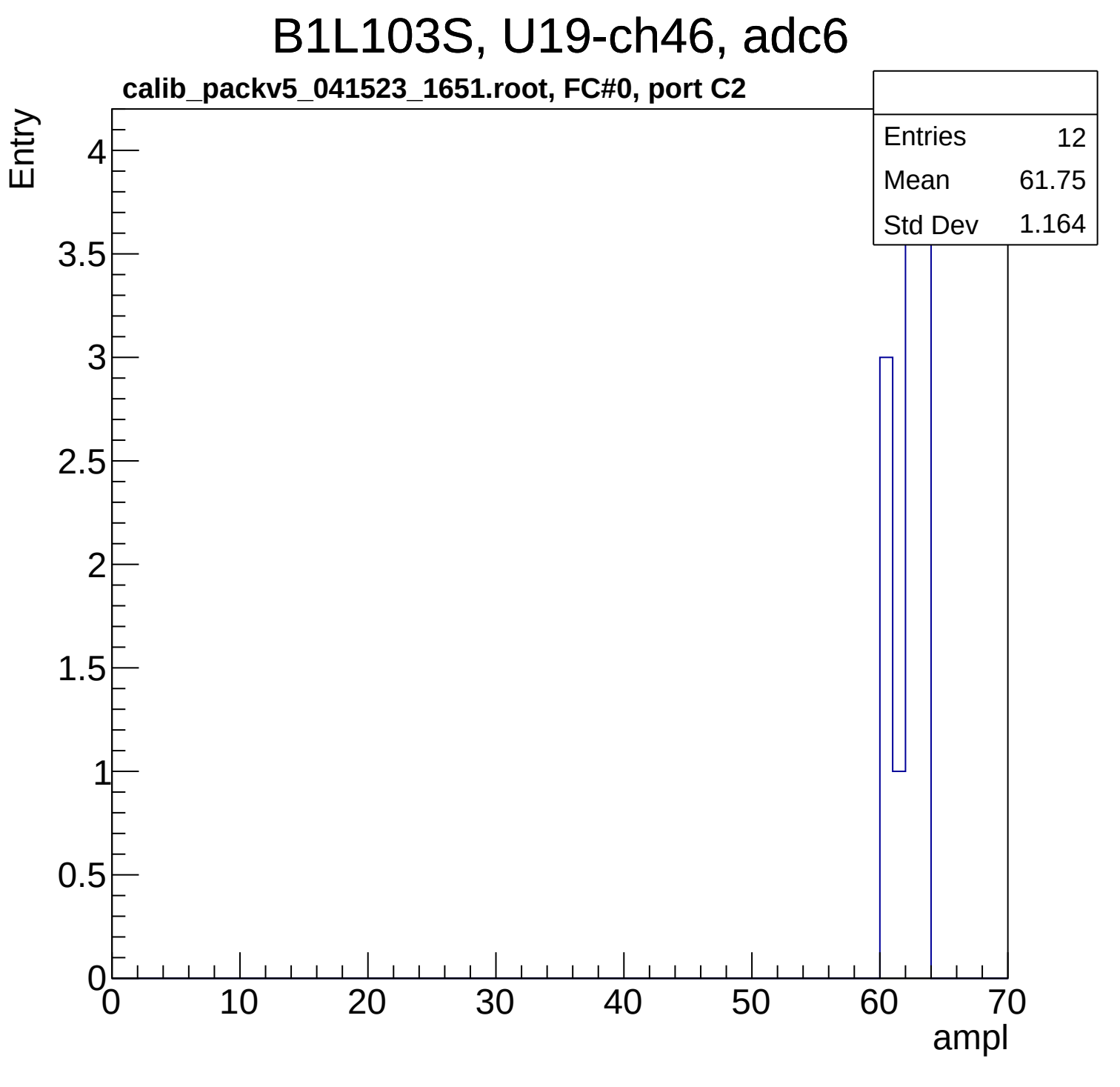
B1L103S, U19-ch46, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.75
Std Dev 1.164
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
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40
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60
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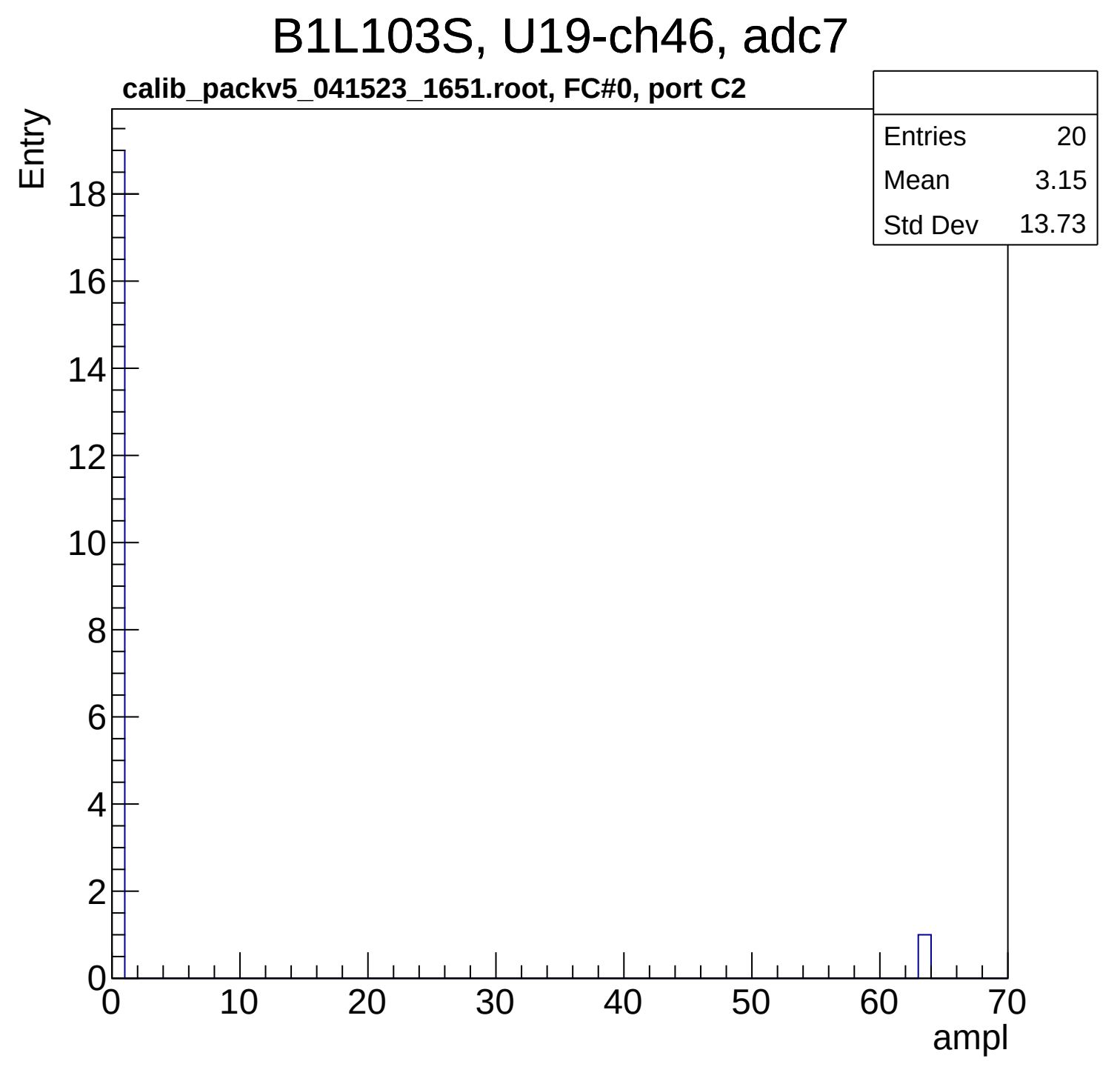
B1L103S, U19-ch46, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
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6
8
10
12
14
16
18
0
10
20
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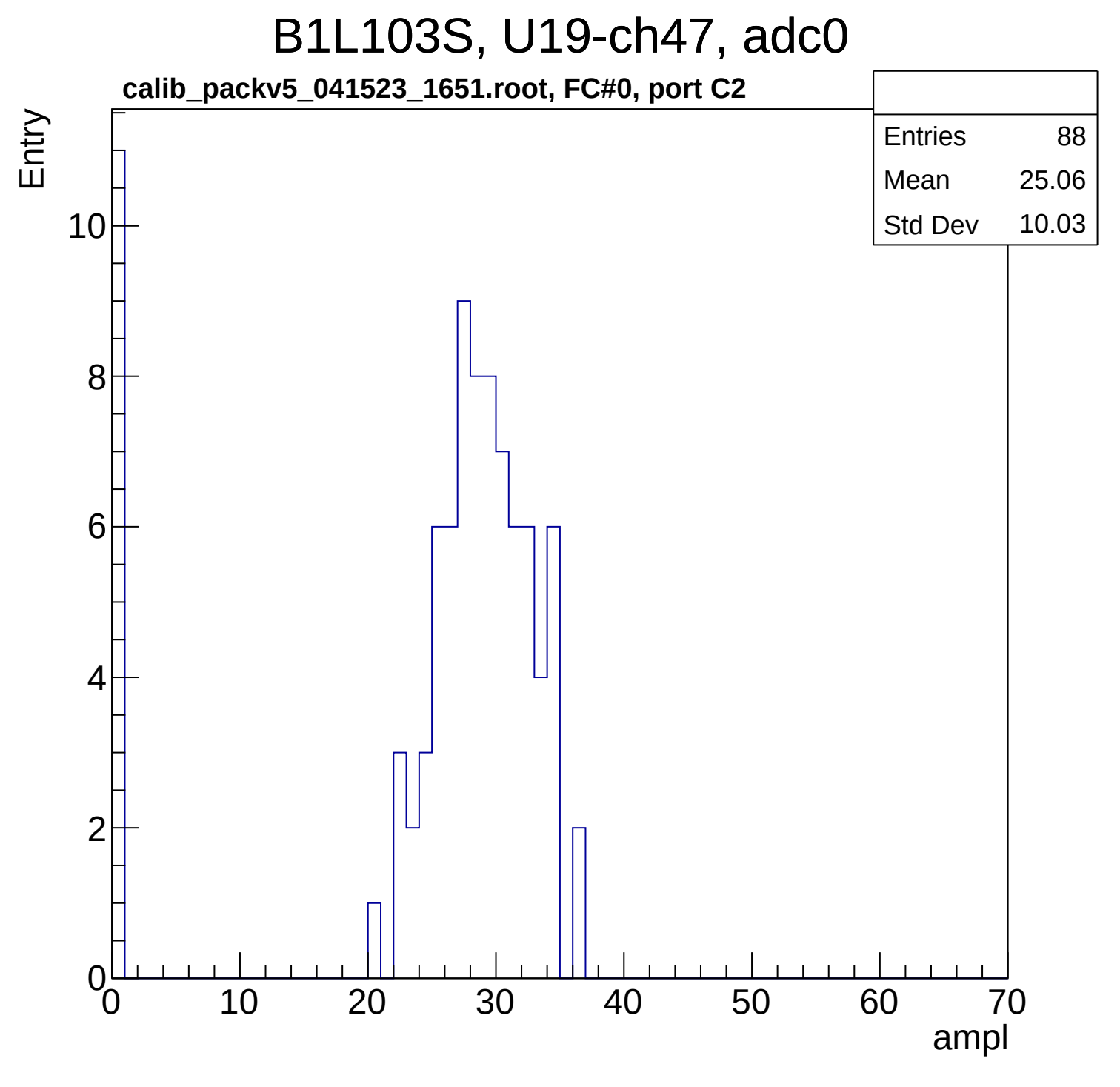
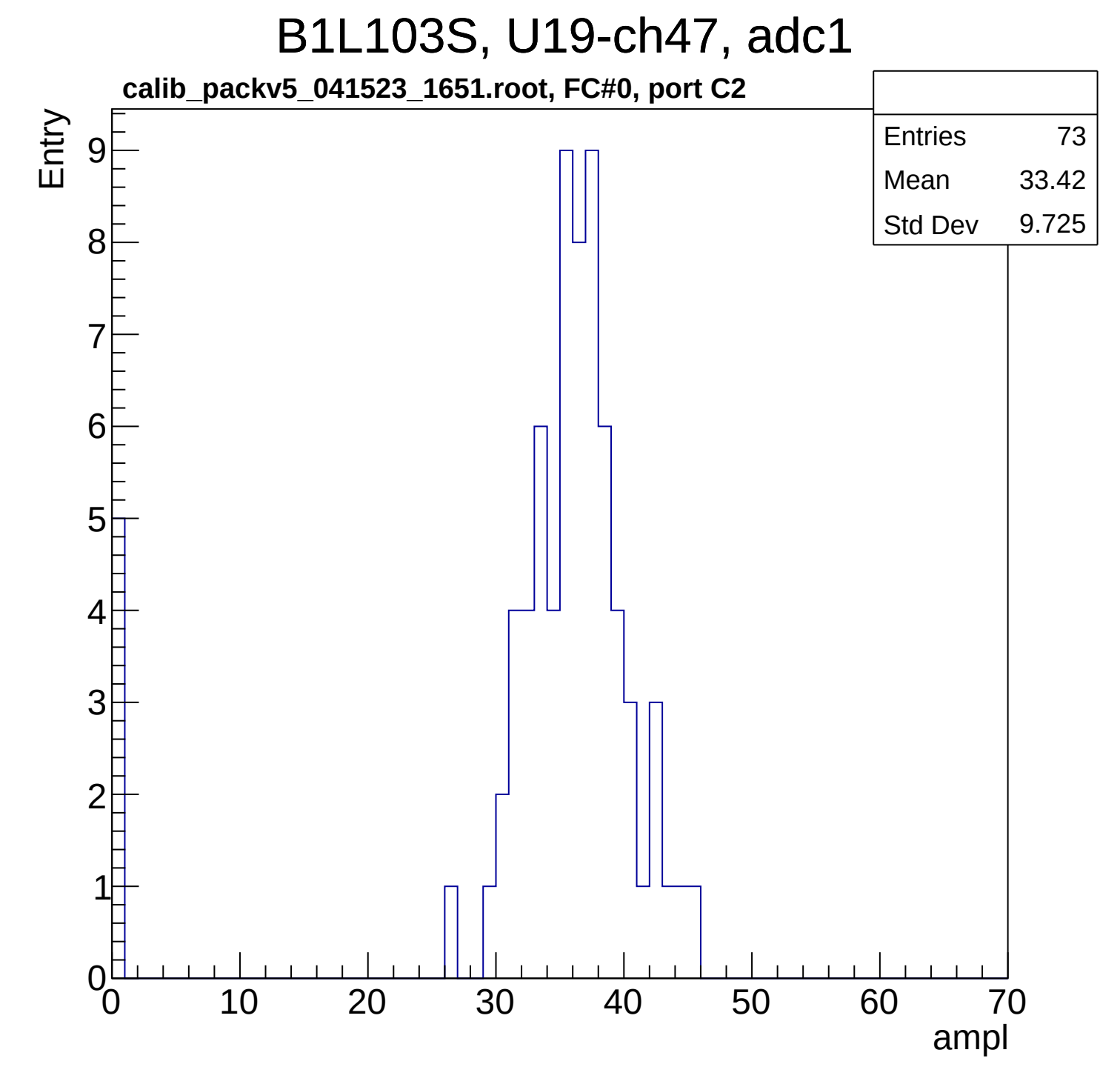
50
60
70
ampl


B1L103S, U19-ch47, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 25.06
Std Dev 10.03
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch47, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 33.42
Std Dev 9.725
Entry
ampl
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3
4
5
6
7
8
9
0
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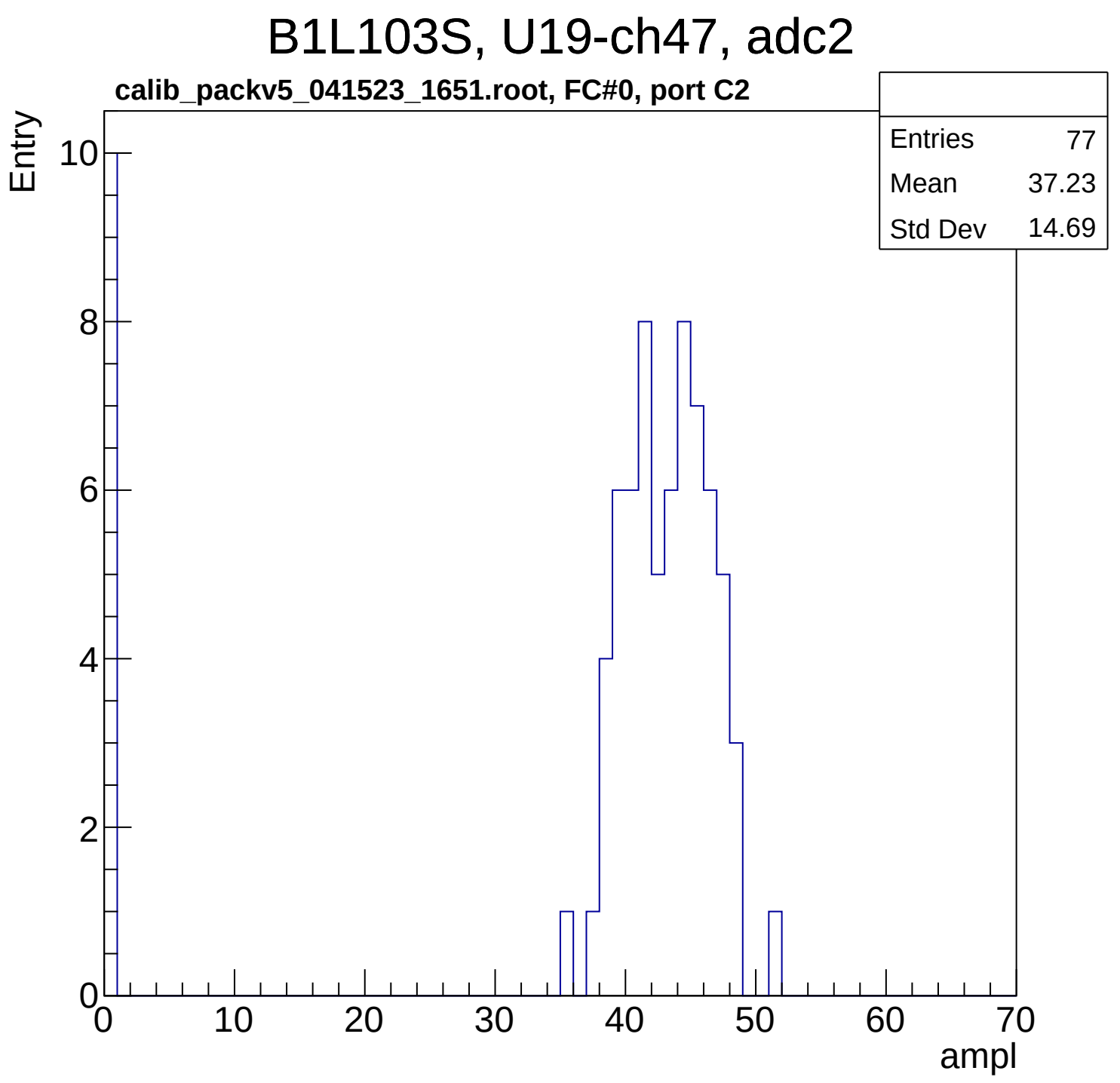
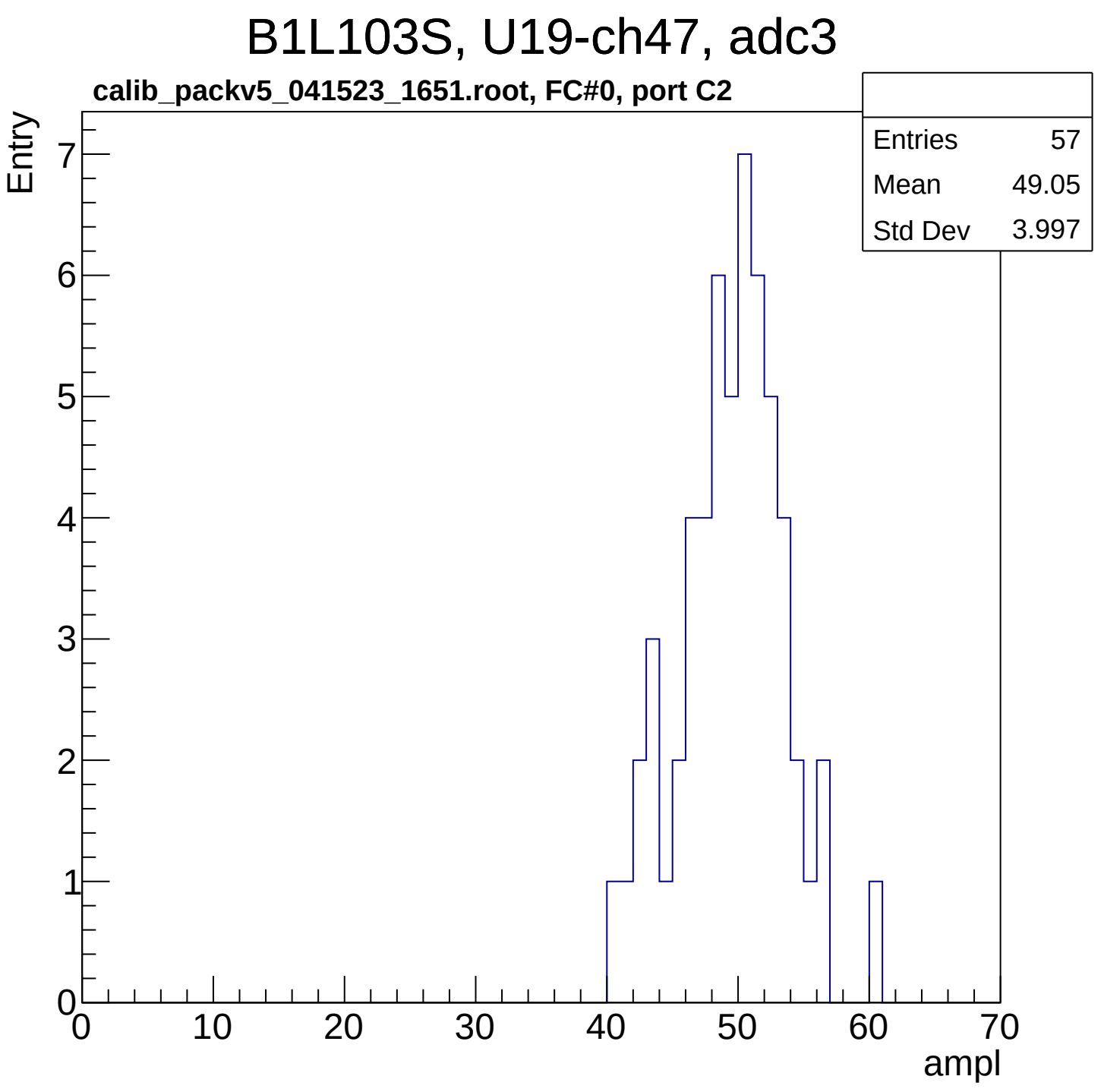

B1L103S, U19-ch47, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 37.23
Std Dev 14.69
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch47, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 49.05
Std Dev 3.997
Entry
ampl
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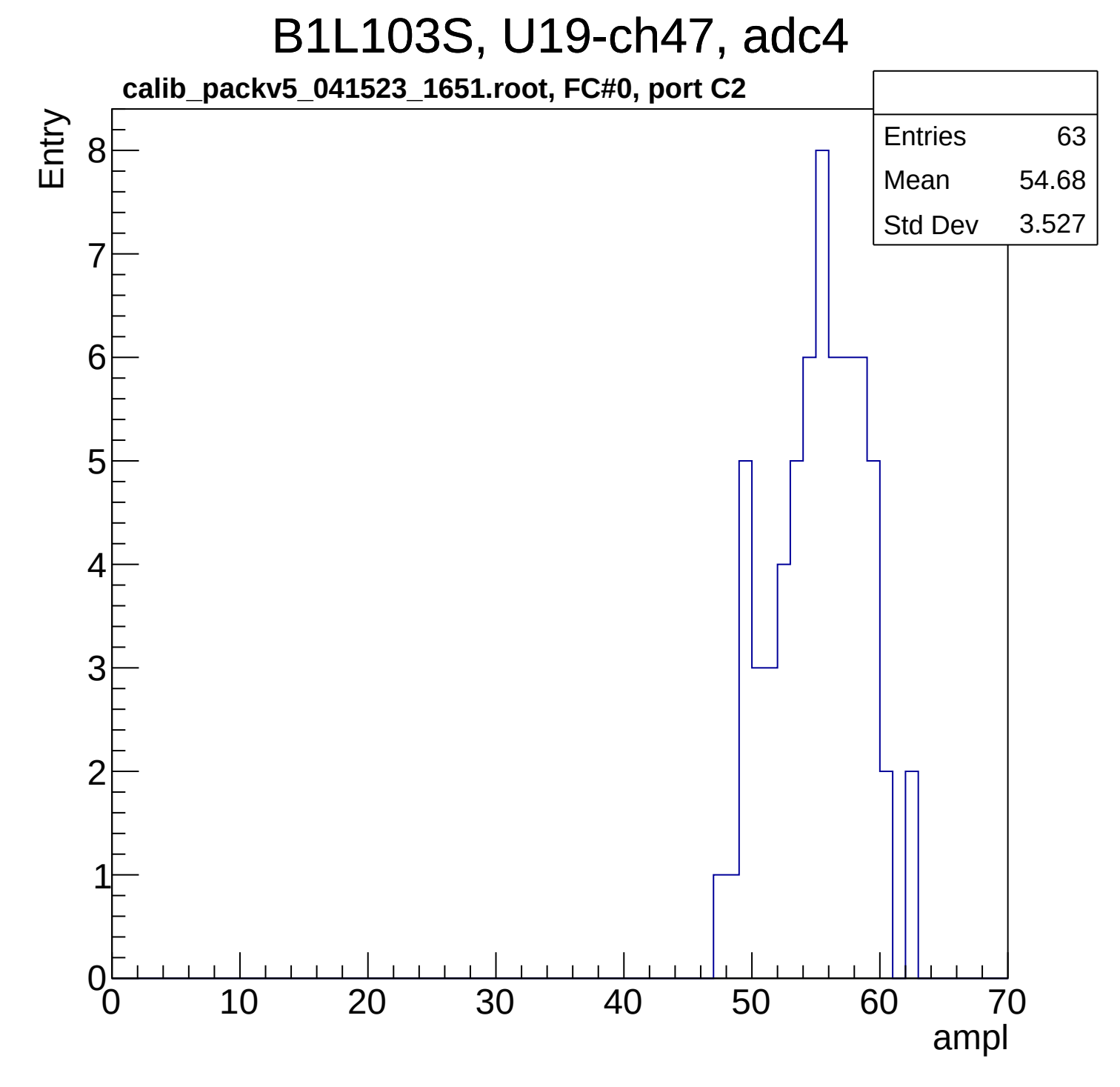
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch47, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 54.68
Std Dev 3.527
Entry
ampl
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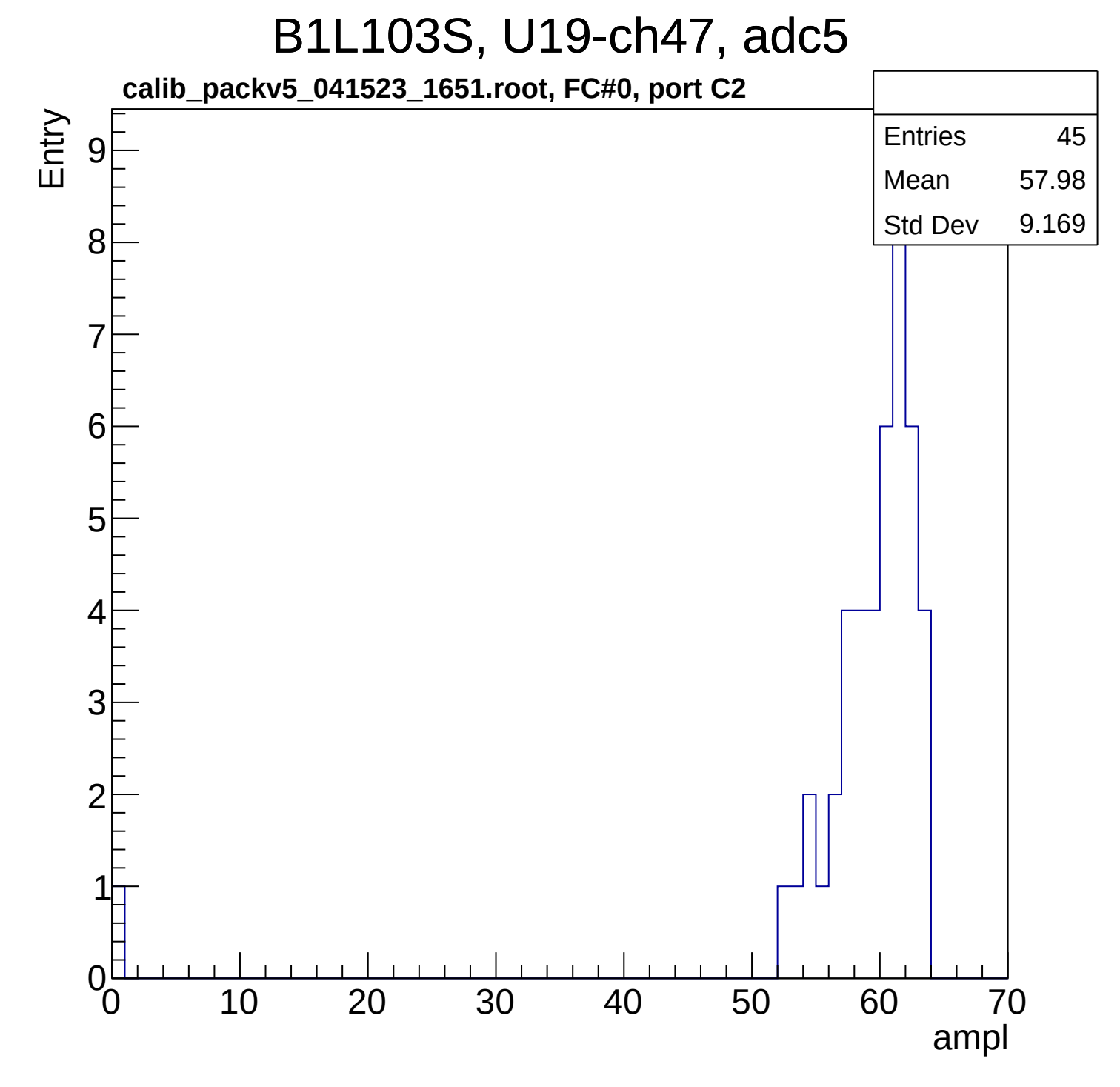
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch47, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 57.98
Std Dev 9.169
Entry
ampl
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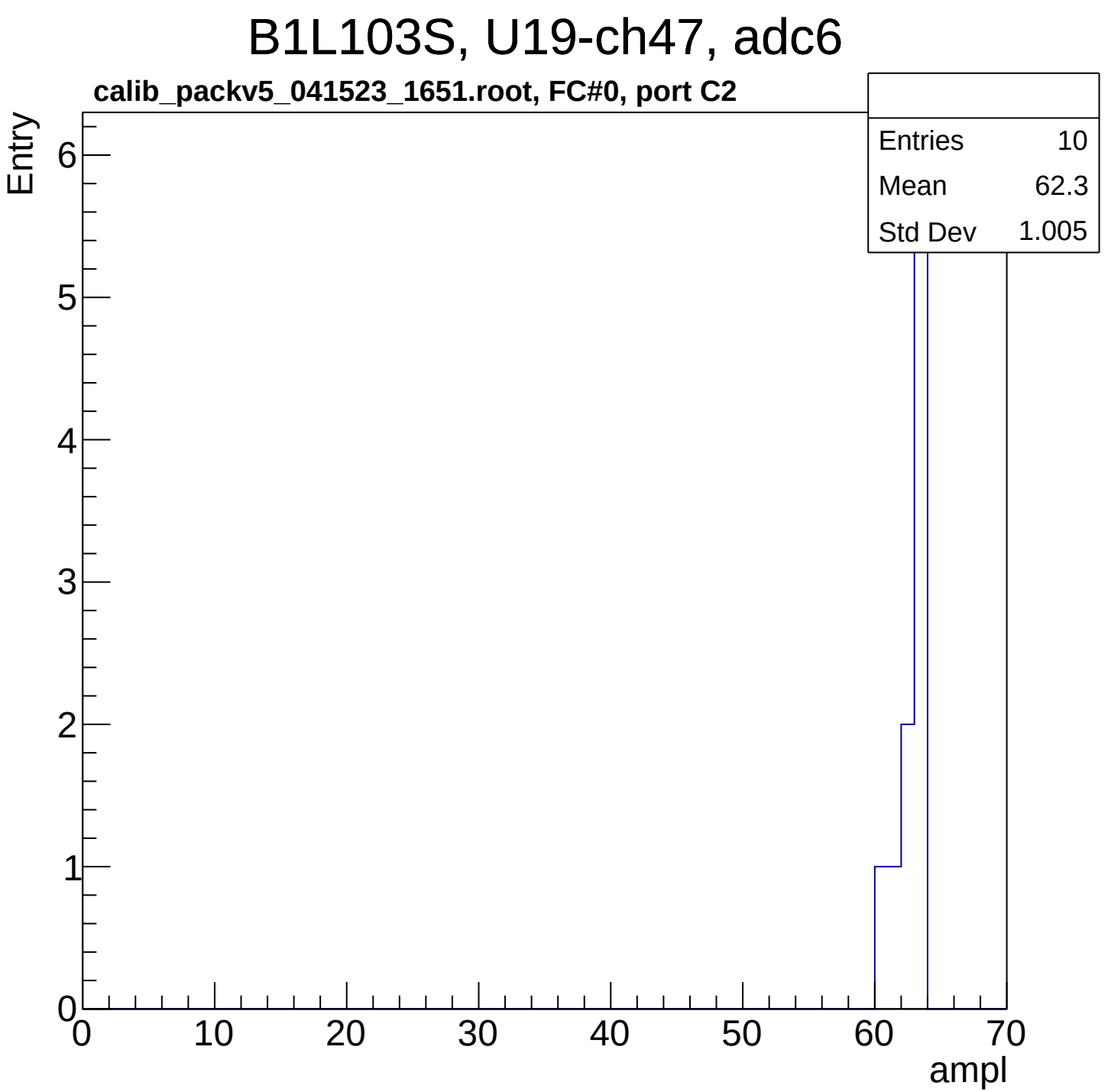
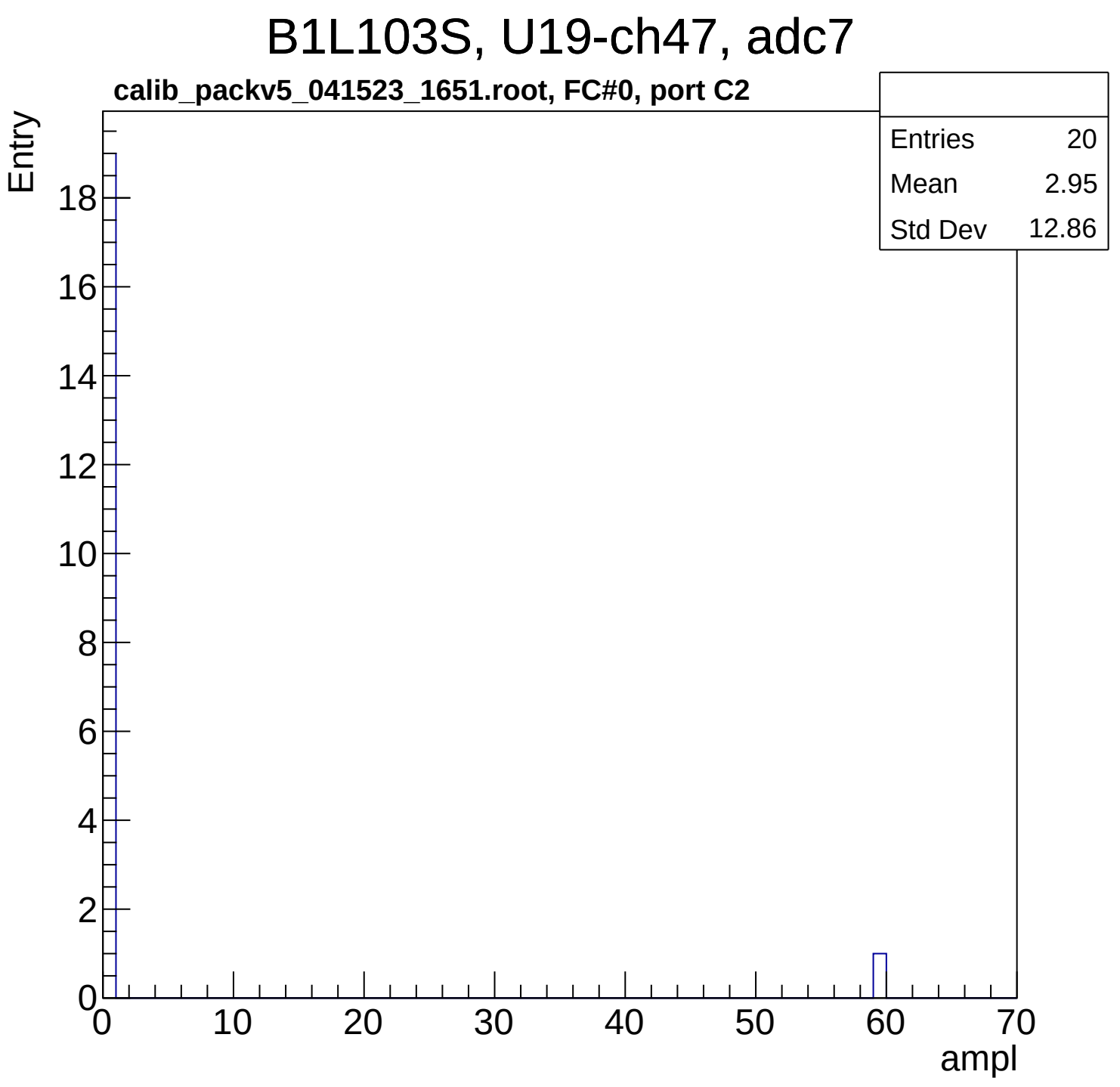
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch47, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 62.3
Std Dev 1.005
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch47, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 2.95
Std Dev 12.86
Entry
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4
6
8
10
12
14
16
18
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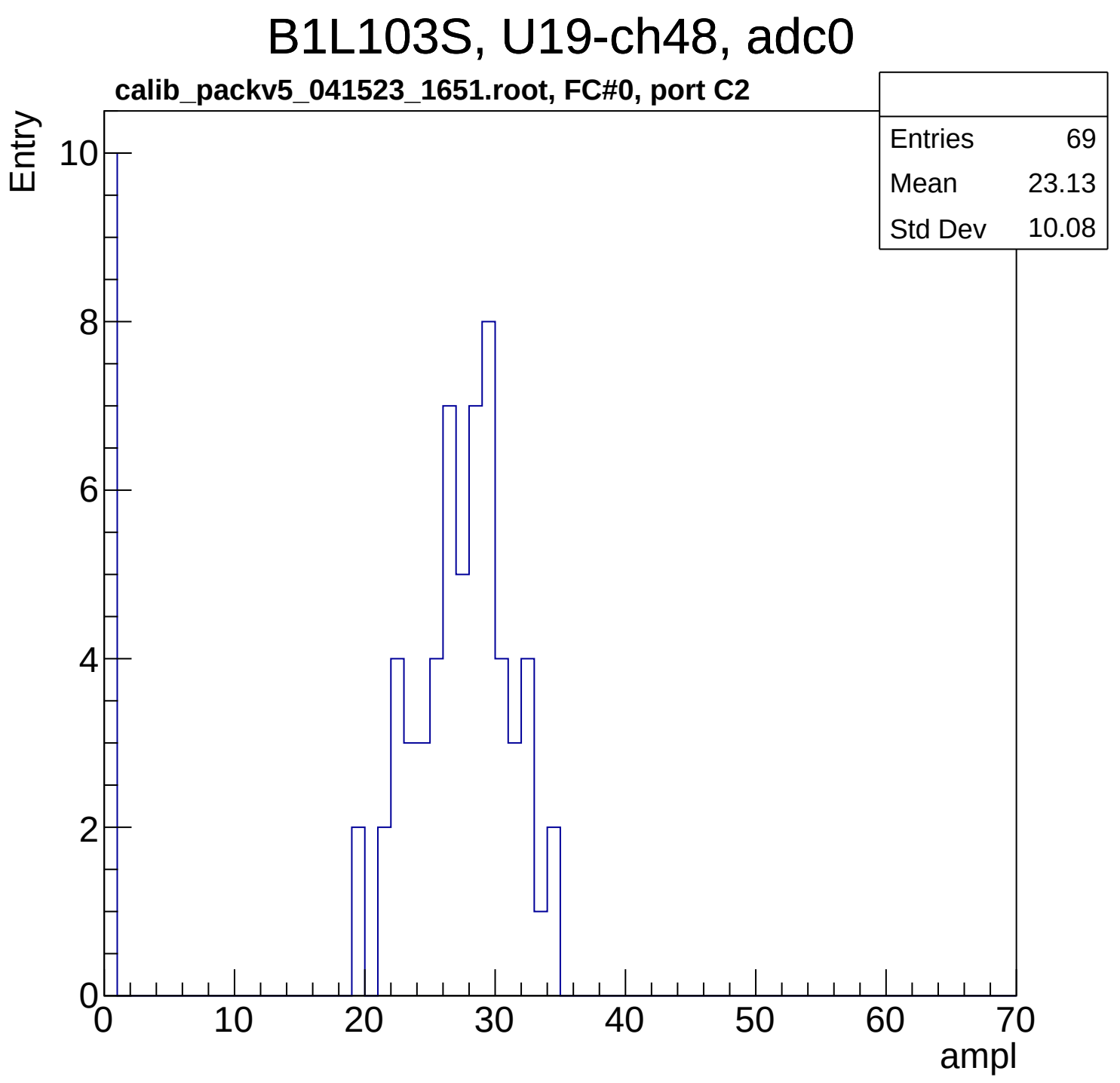
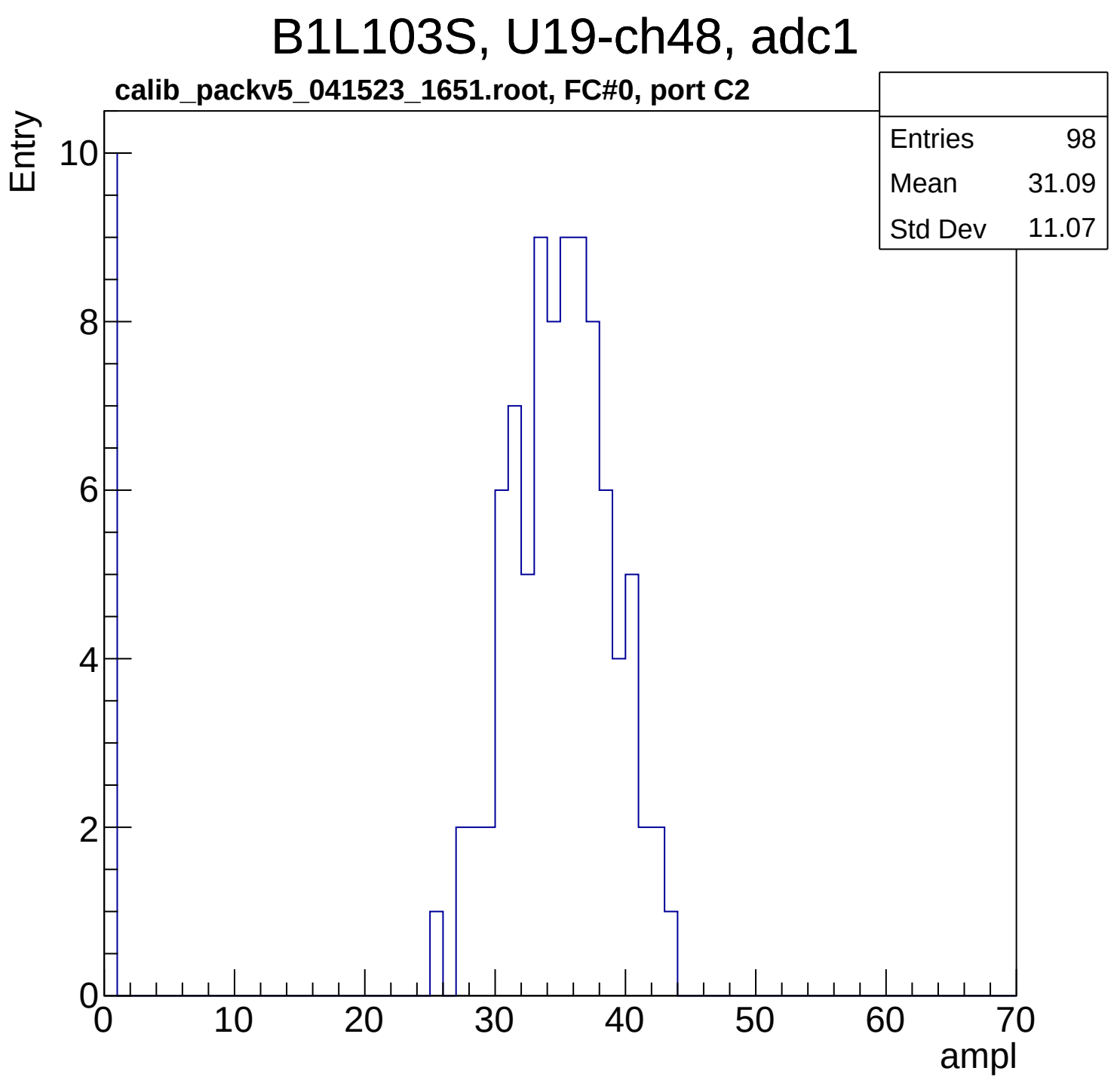
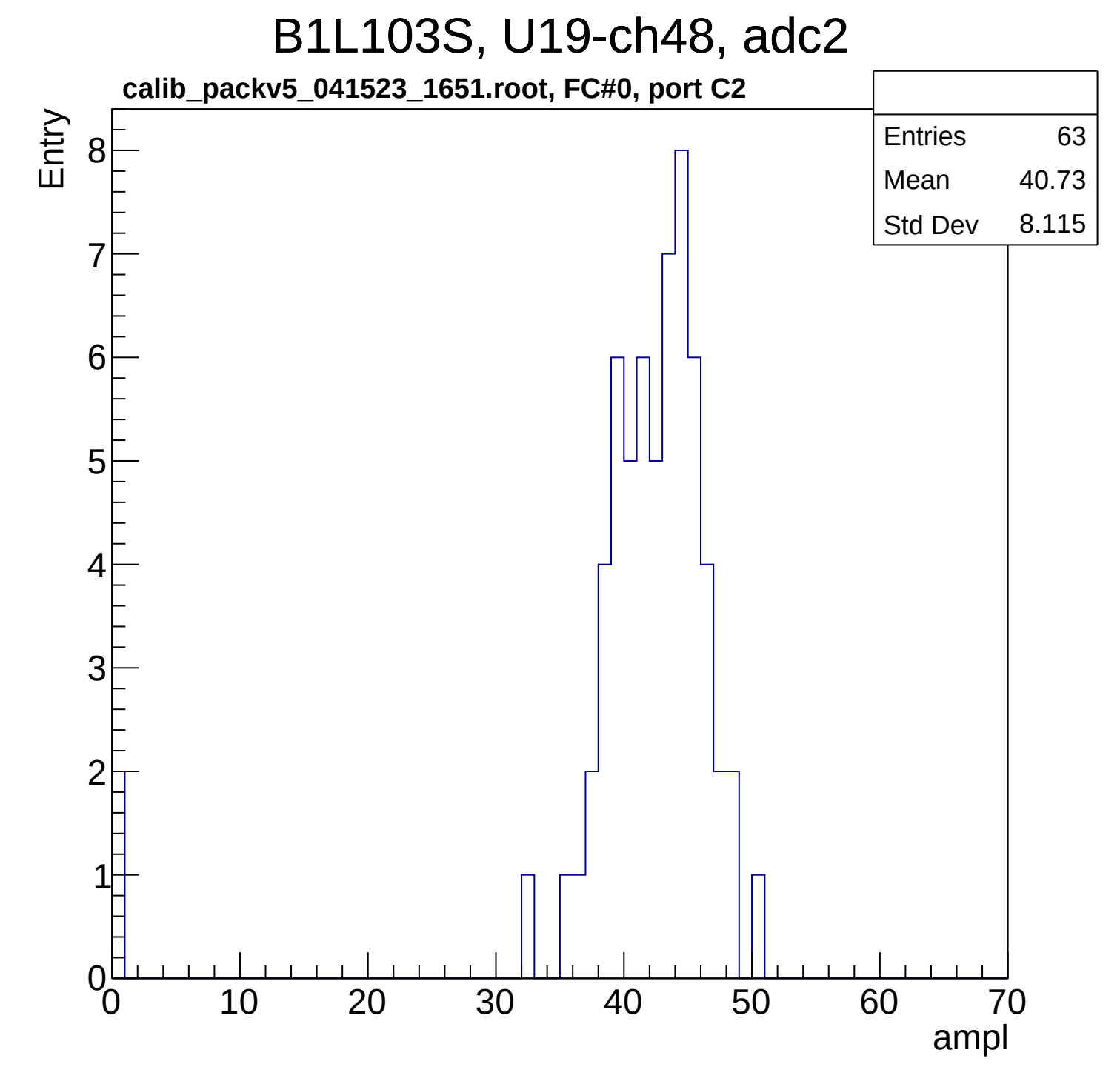
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch48, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 23.13
Std Dev 10.08
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch48, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 98
Mean 31.09
Std Dev 11.07
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch48, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 40.73
Std Dev 8.115
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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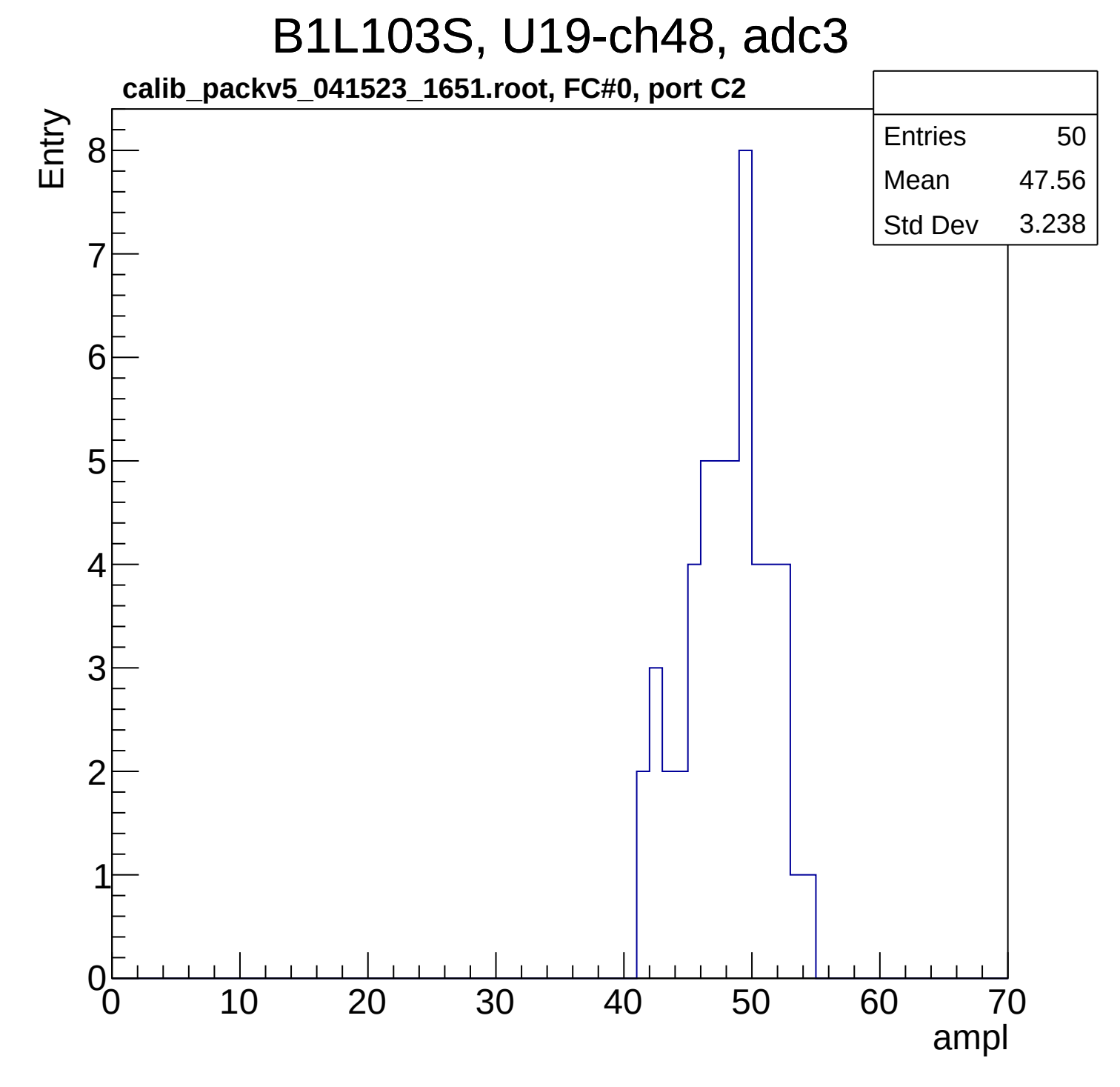
40
50
60
70


B1L103S, U19-ch48, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 47.56
Std Dev 3.238
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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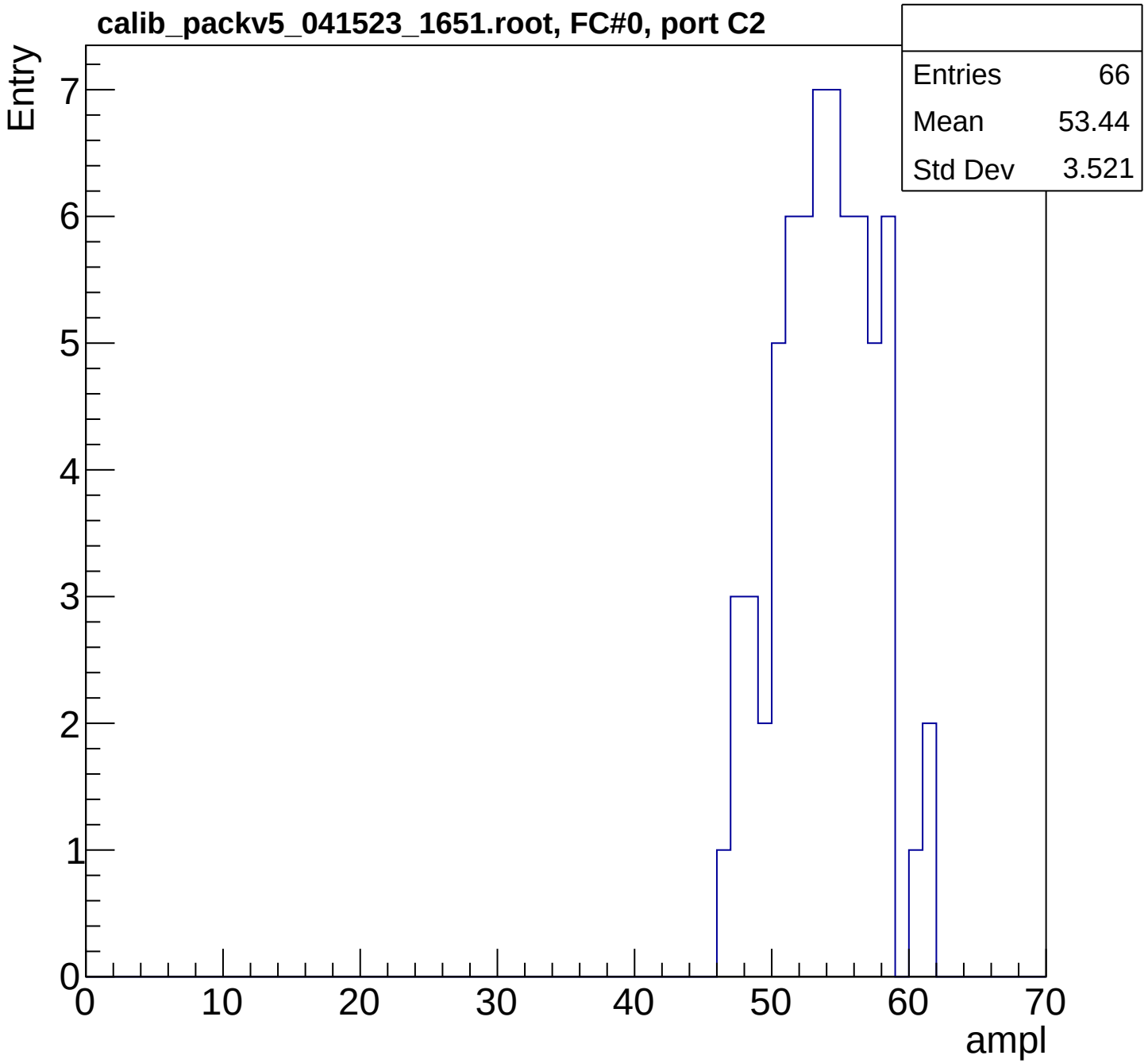
B1L103S, U19-ch48, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 53.44
Std Dev 3.521
Entry
ampl
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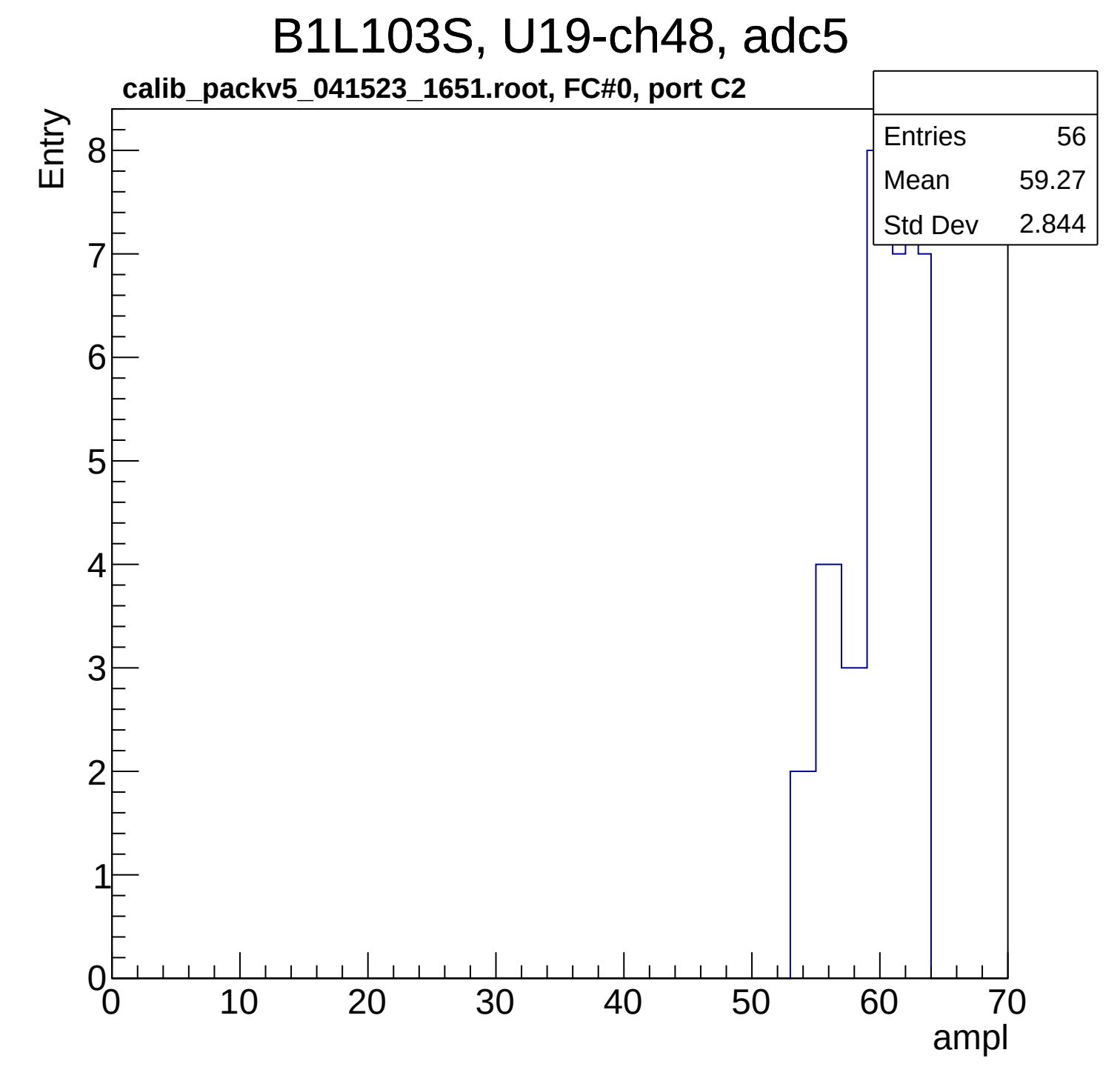
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch48, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 59.27
Std Dev 2.844
Entry
ampl
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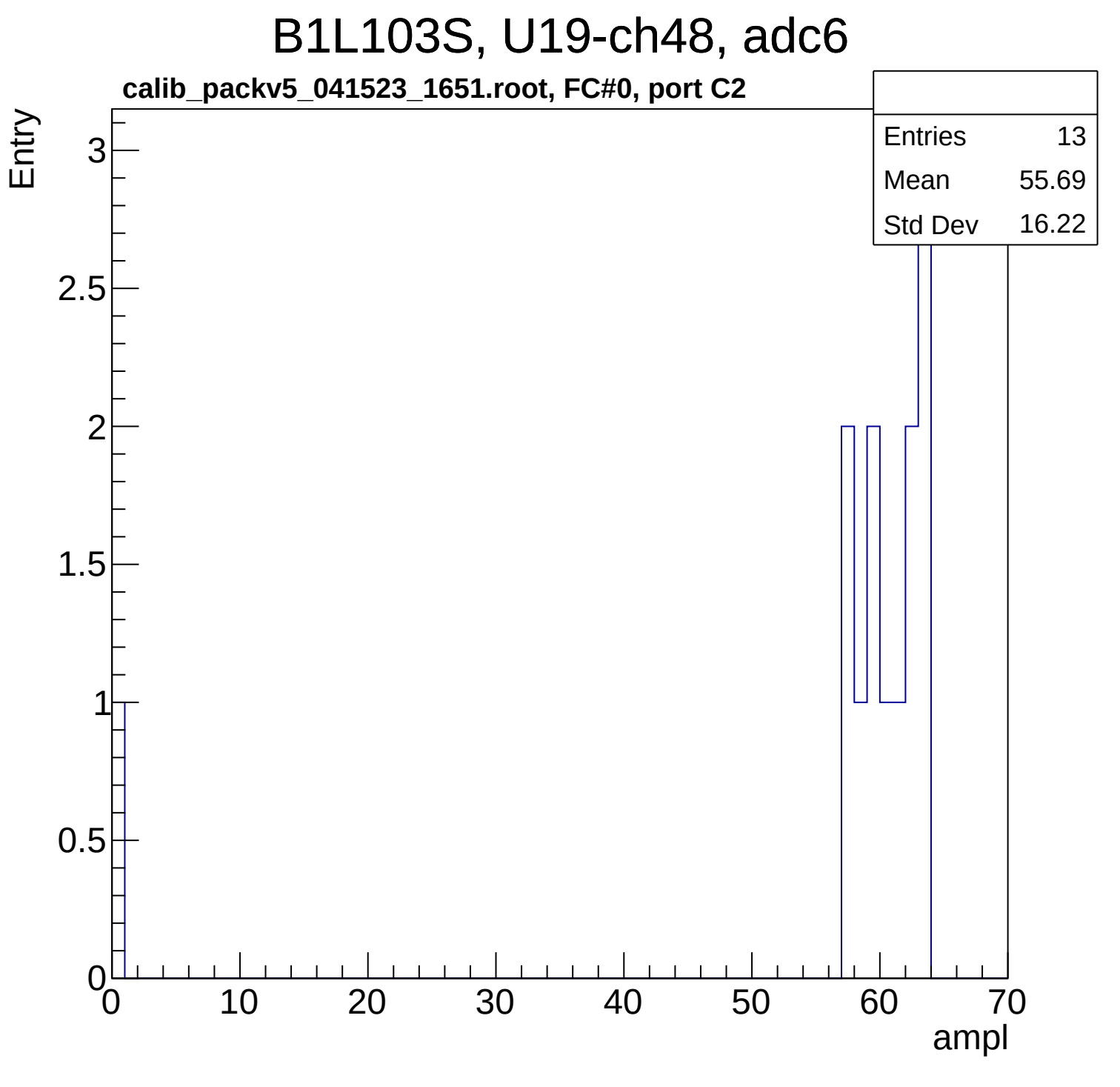
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch48, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 55.69
Std Dev 16.22
Entry
ampl
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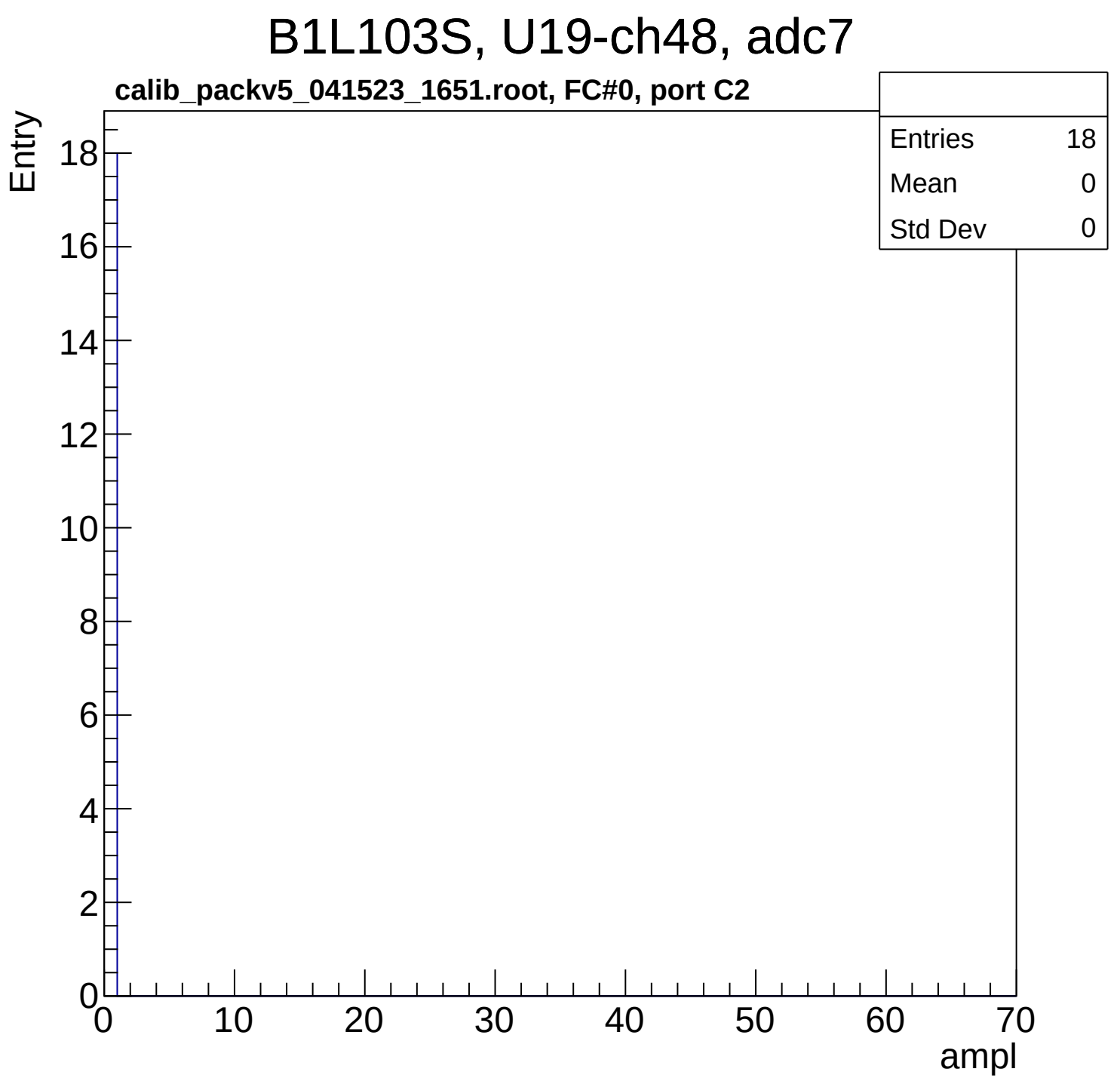
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U19-ch48, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
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6
8
10
12
14
16
18
0
10
20
30
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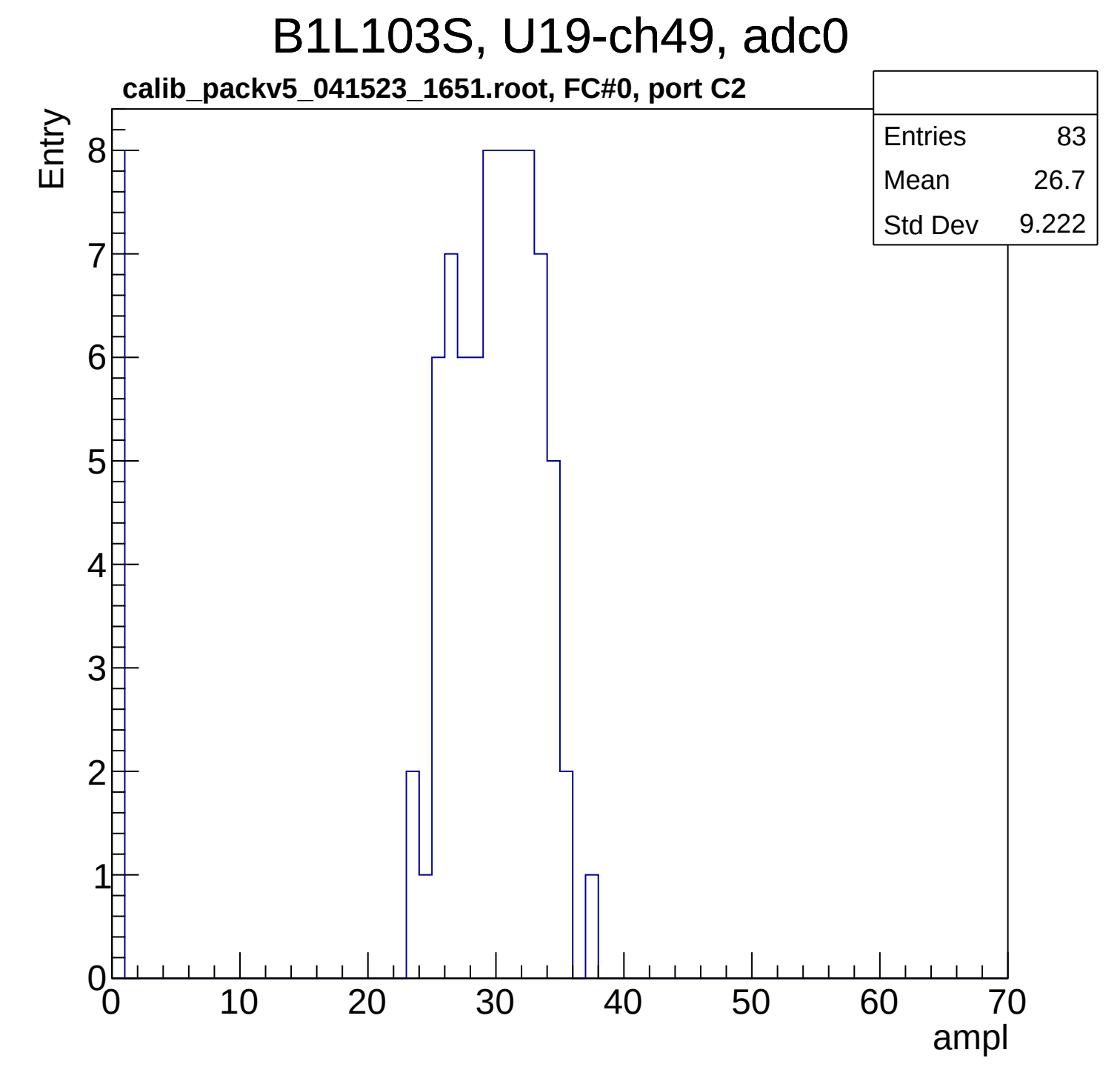
50
60
70
ampl


B1L103S, U19-ch49, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 26.7
Std Dev 9.222
Entry
ampl
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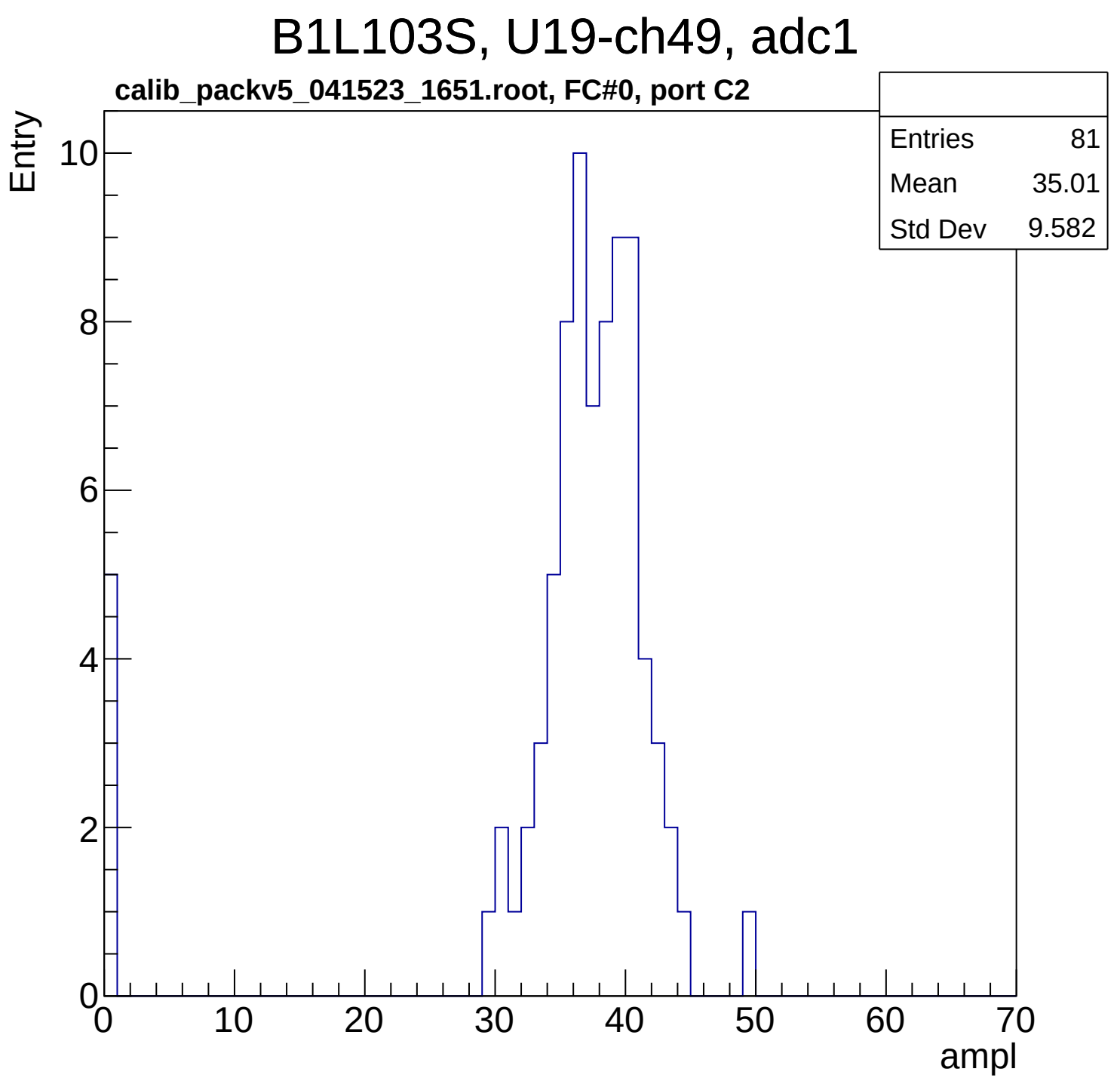
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch49, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 35.01
Std Dev 9.582
Entry
ampl
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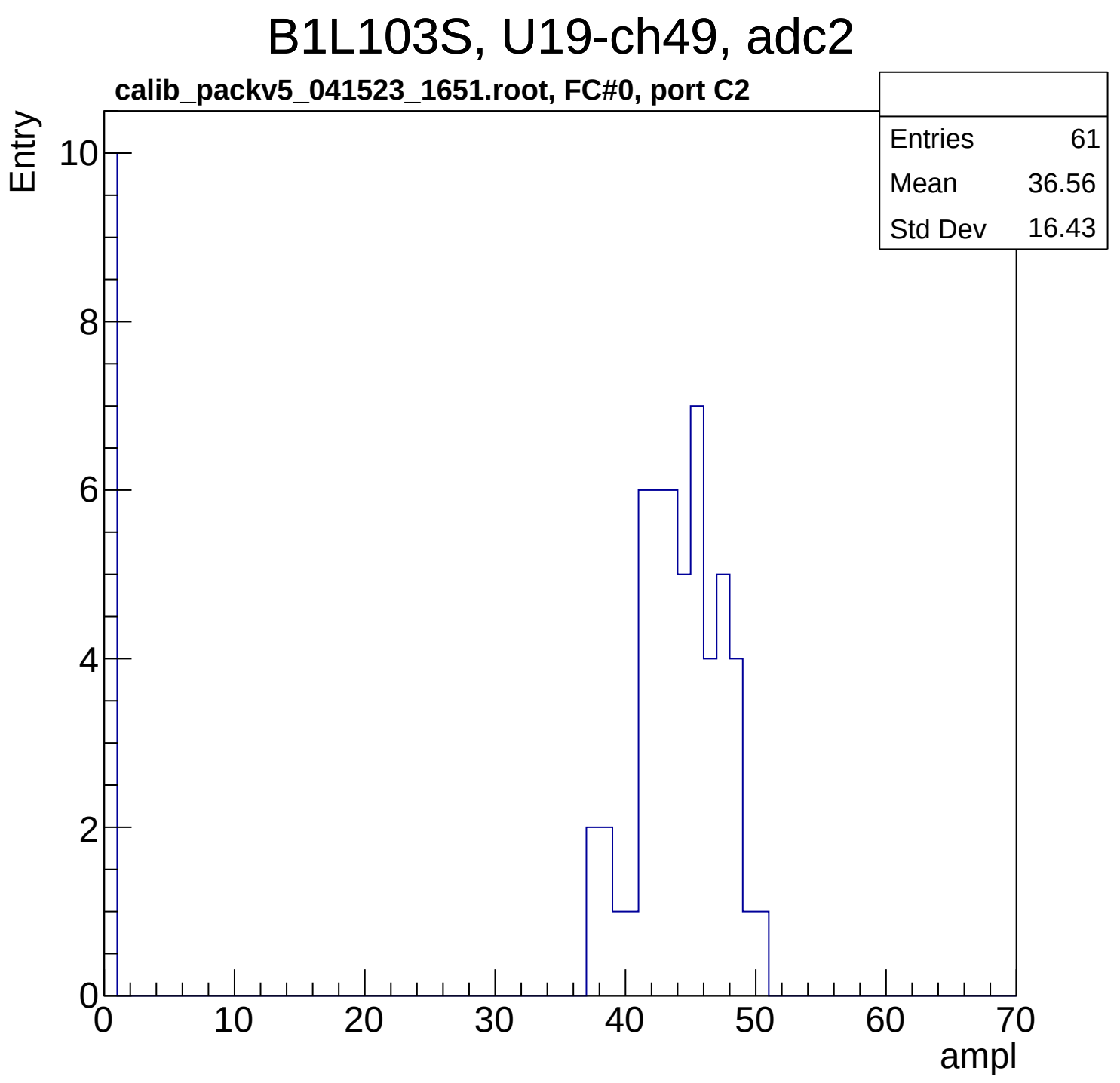
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U19-ch49, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 36.56
Std Dev 16.43
Entry
ampl
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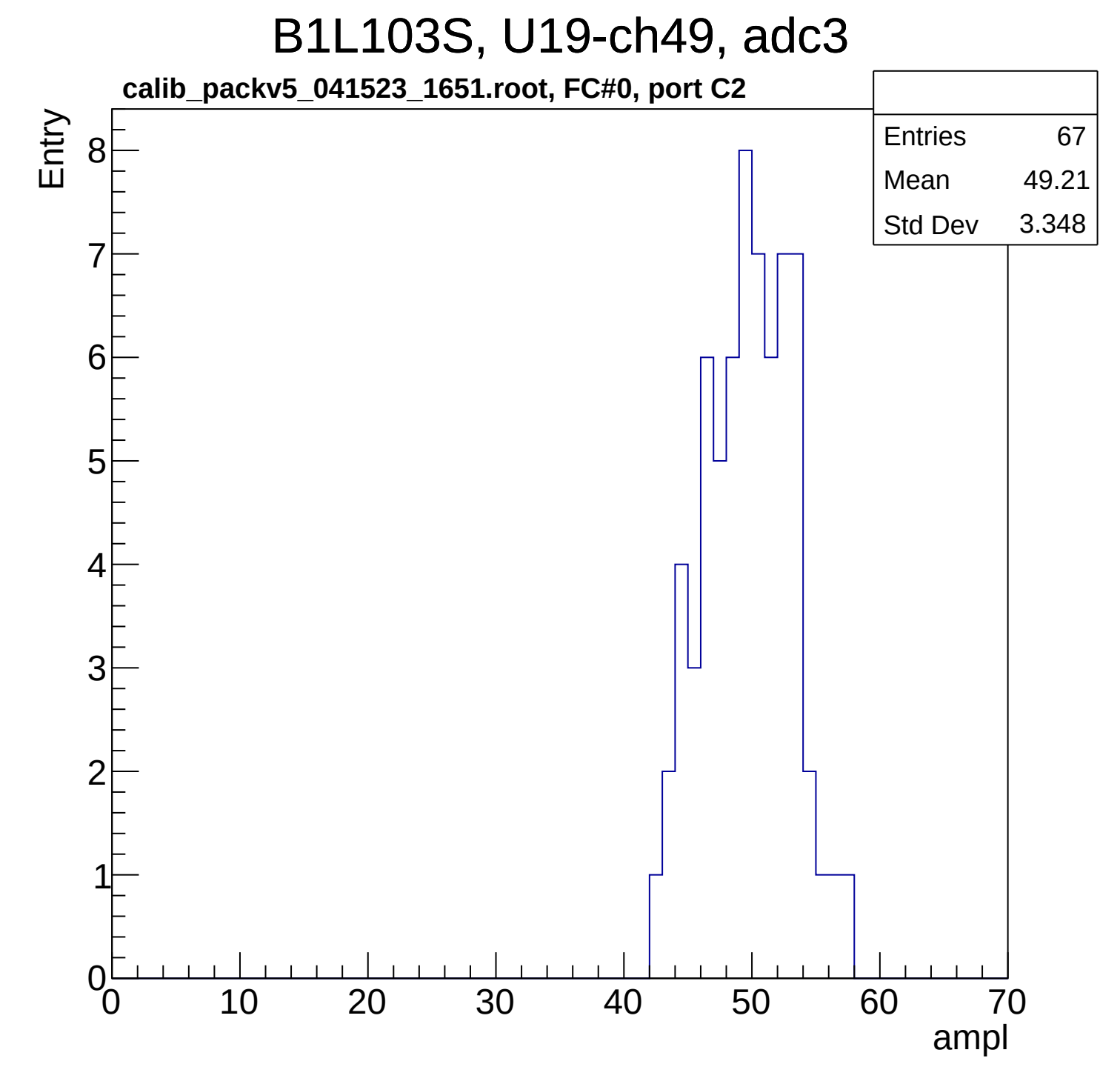
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U19-ch49, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 49.21
Std Dev 3.348
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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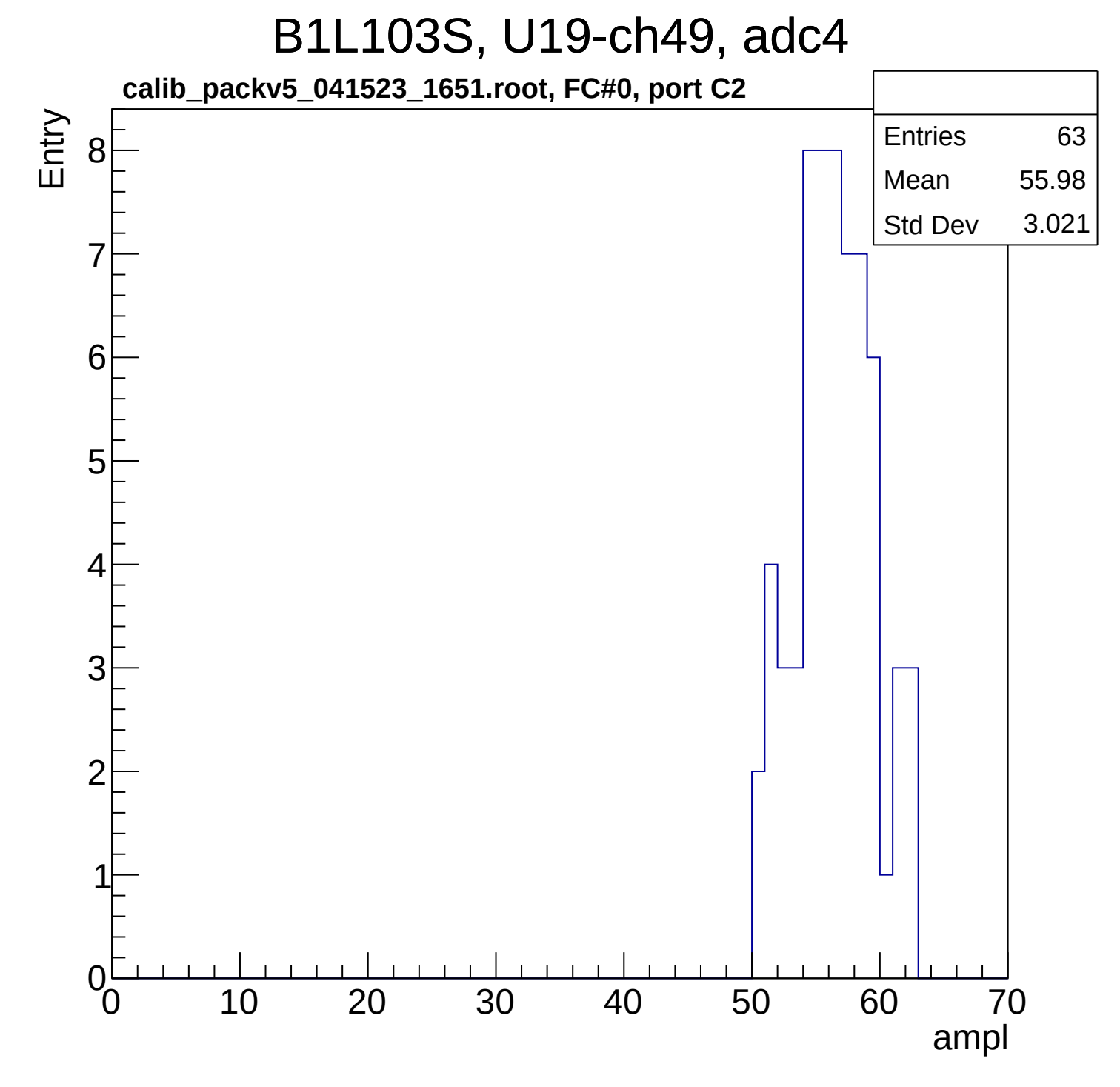
60
70


B1L103S, U19-ch49, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 55.98
Std Dev 3.021
Entry
ampl
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1
2
3
4
5
6
7
8
0
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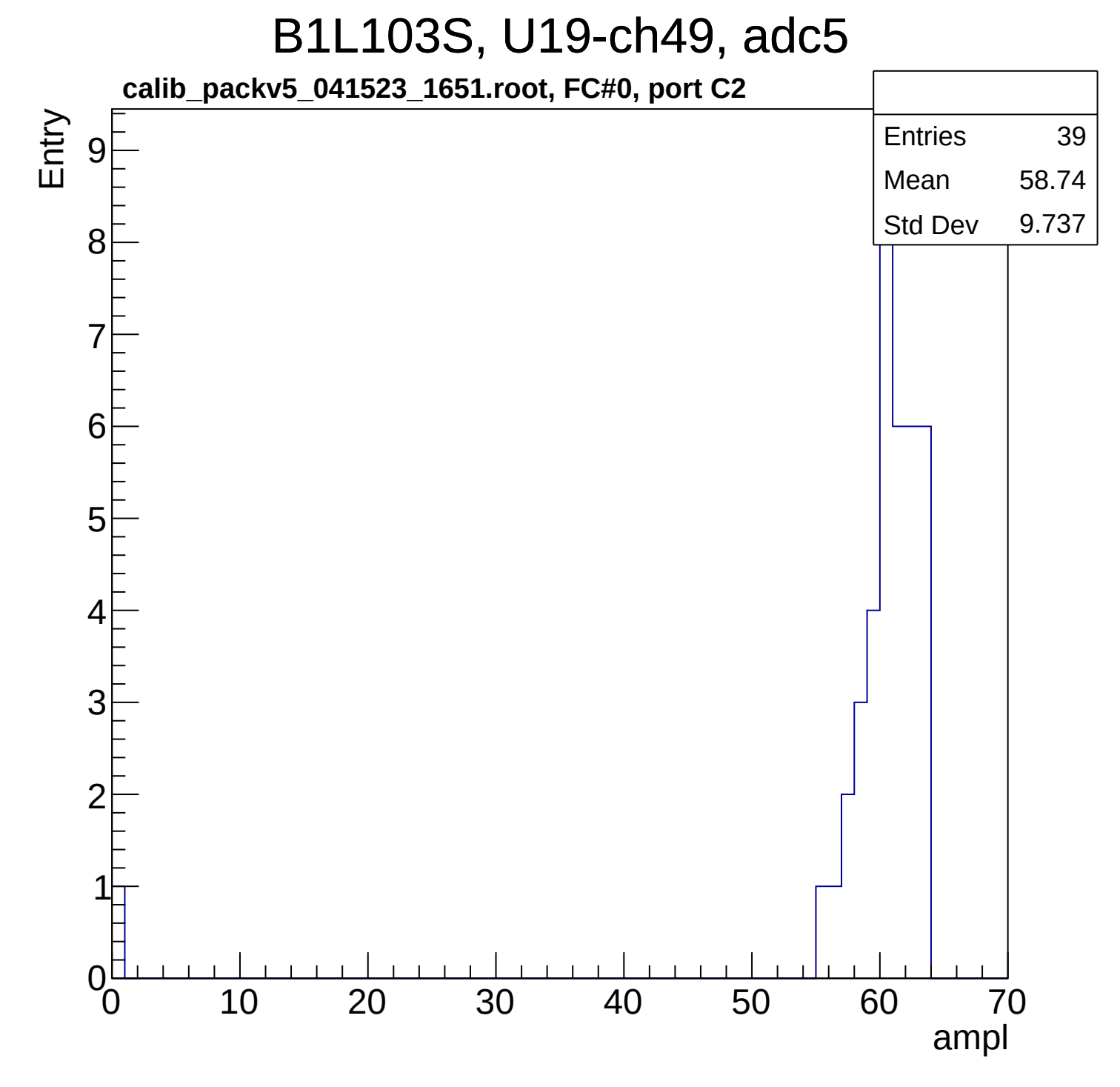
40
50
60
70


B1L103S, U19-ch49, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 58.74
Std Dev 9.737
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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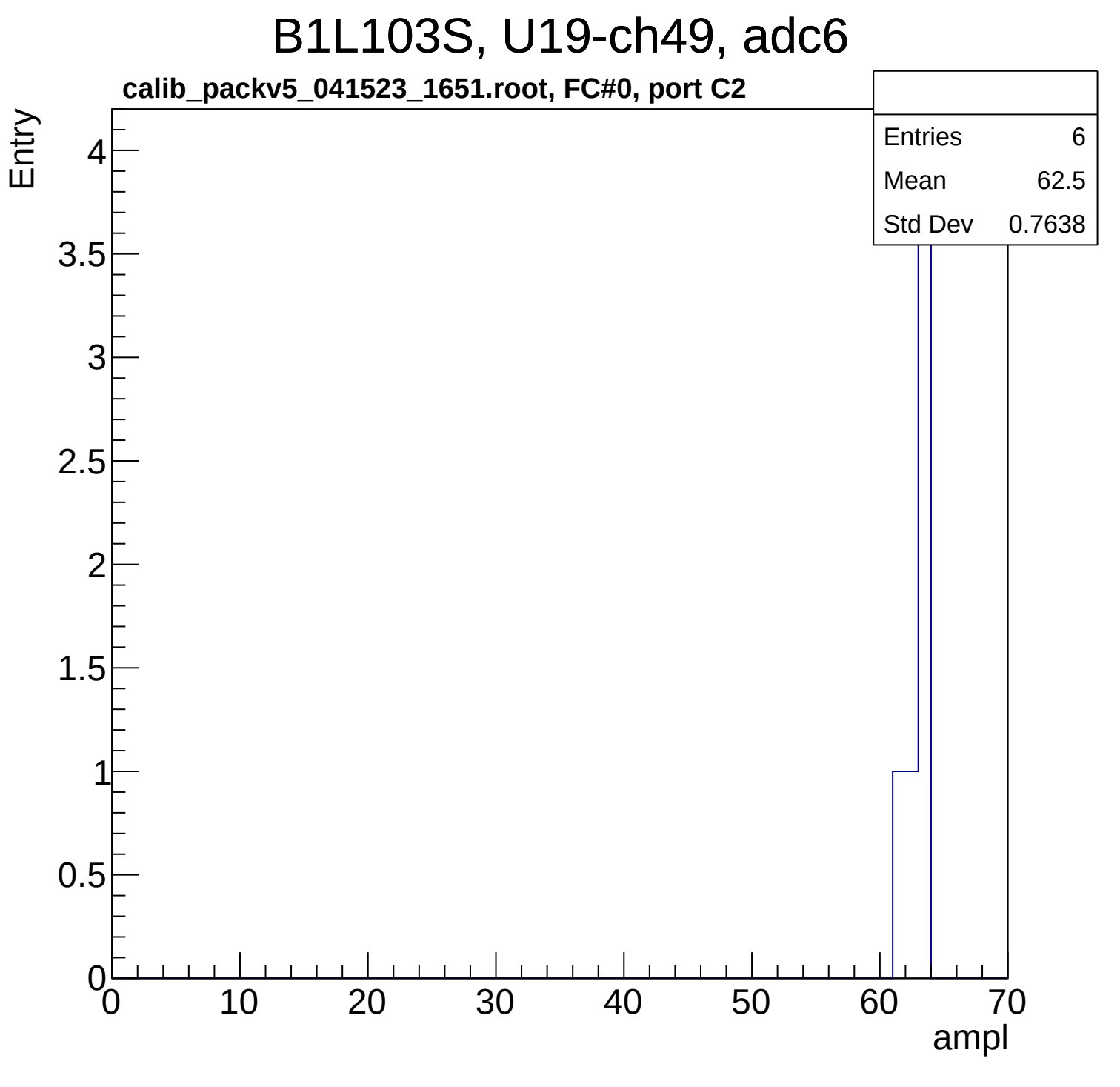
60
70


B1L103S, U19-ch49, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 62.5
Std Dev 0.7638
Entry
ampl
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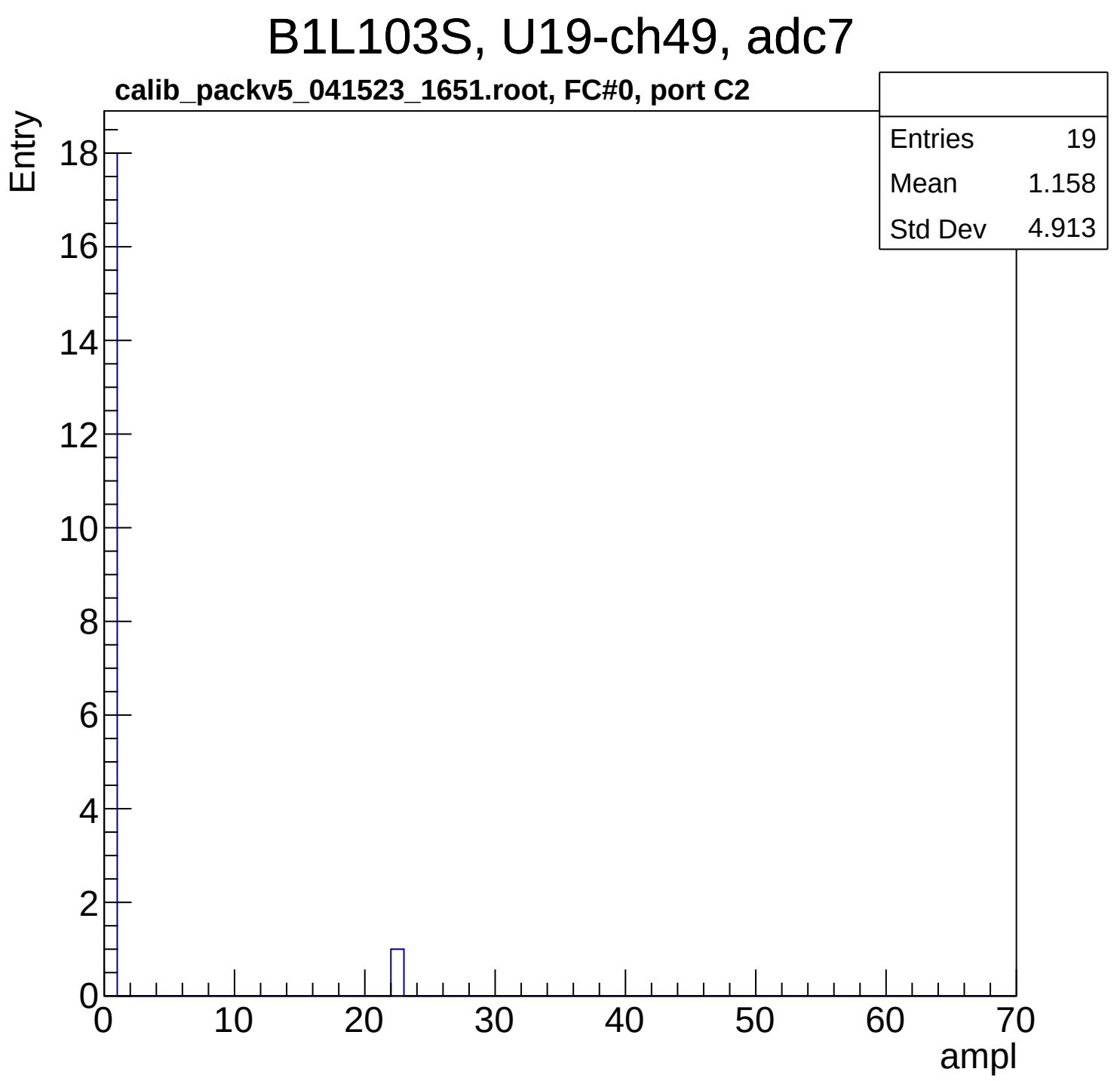
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U19-ch49, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.158
Std Dev 4.913
Entry
0
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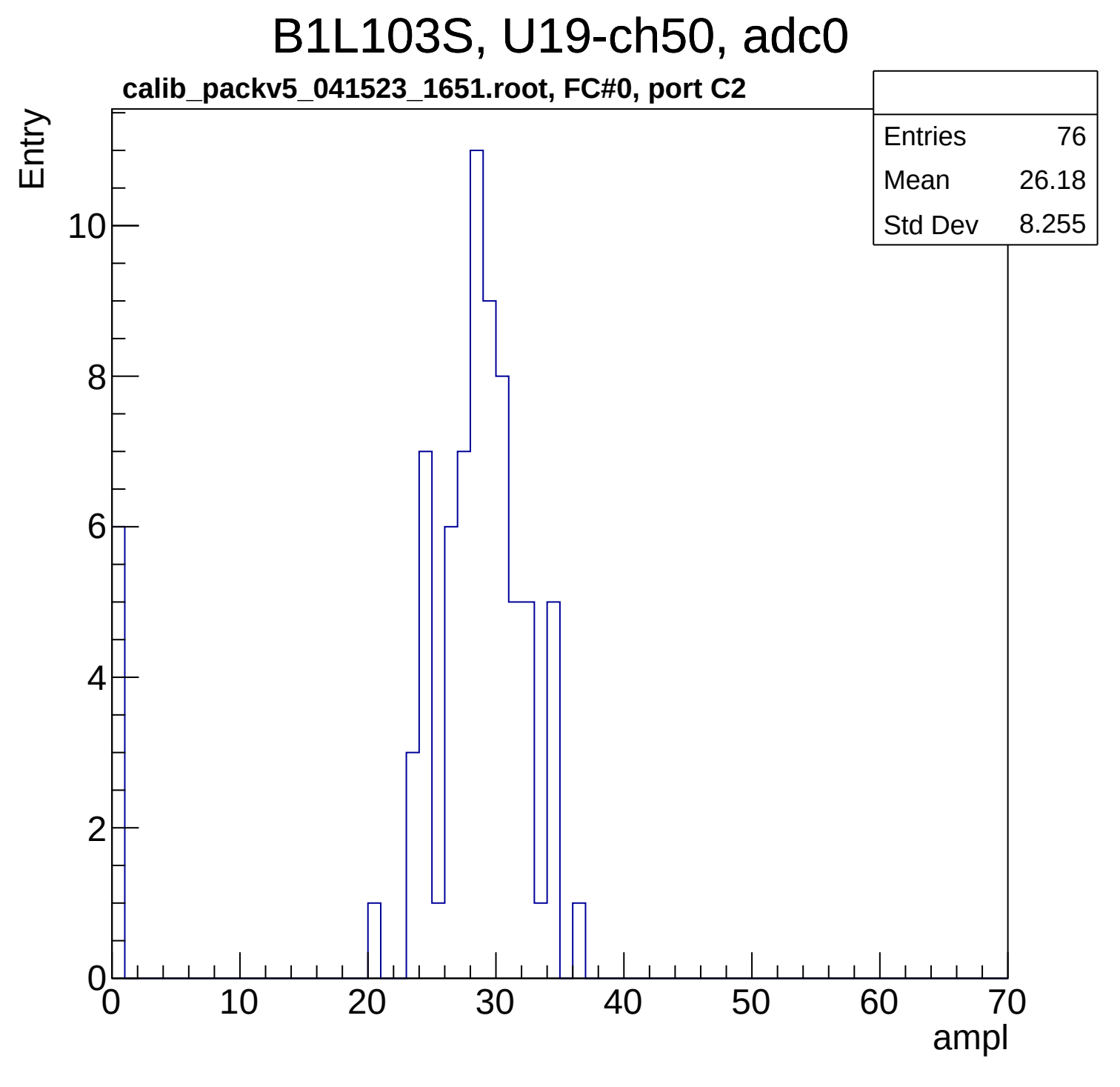
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch50, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 26.18
Std Dev 8.255
Entry
0
2
4
6
8
10
0
10
20
30
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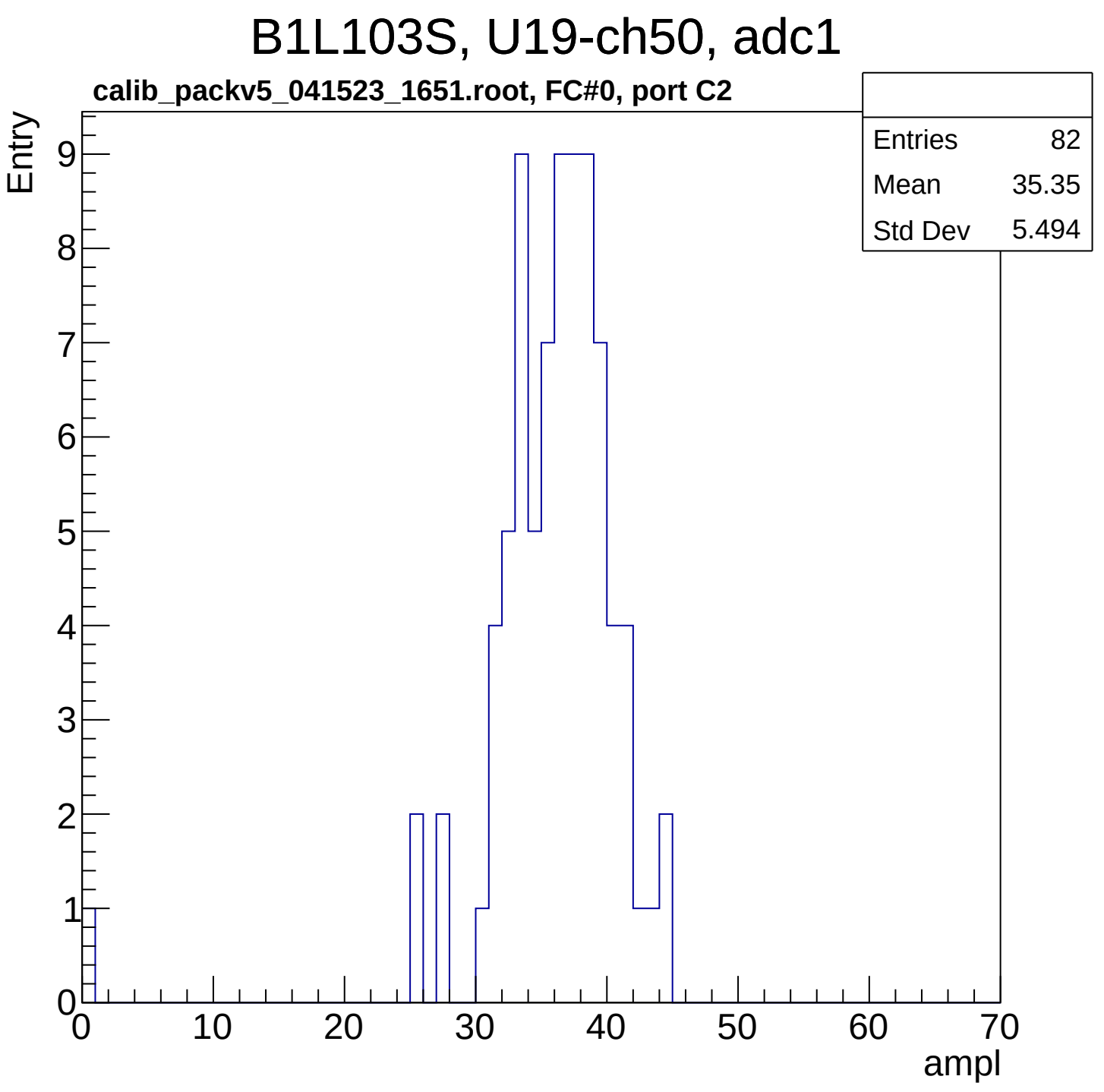
50
60
70
ampl


B1L103S, U19-ch50, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 35.35
Std Dev 5.494
Entry
ampl
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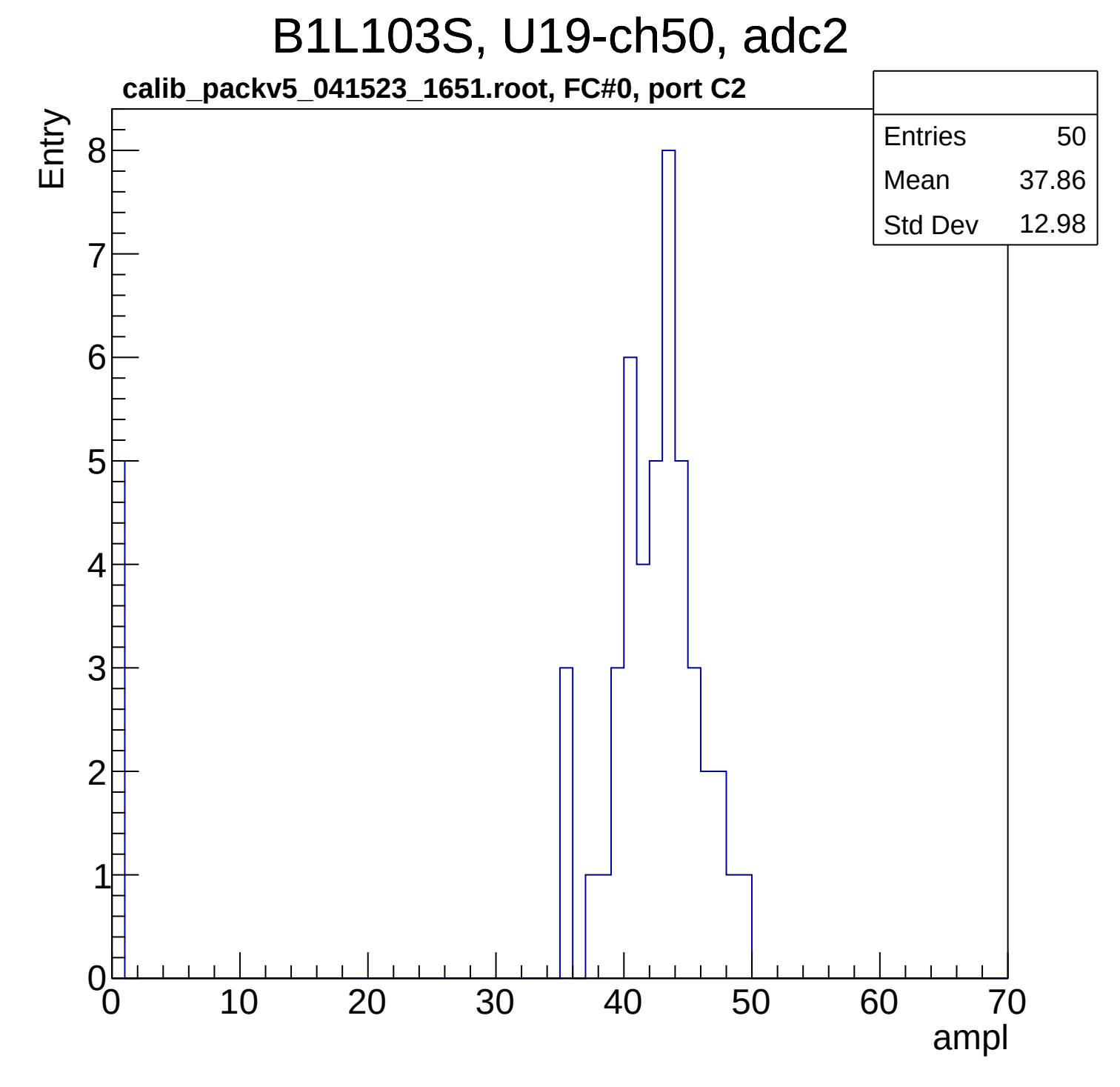
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch50, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 37.86
Std Dev 12.98
Entry
ampl
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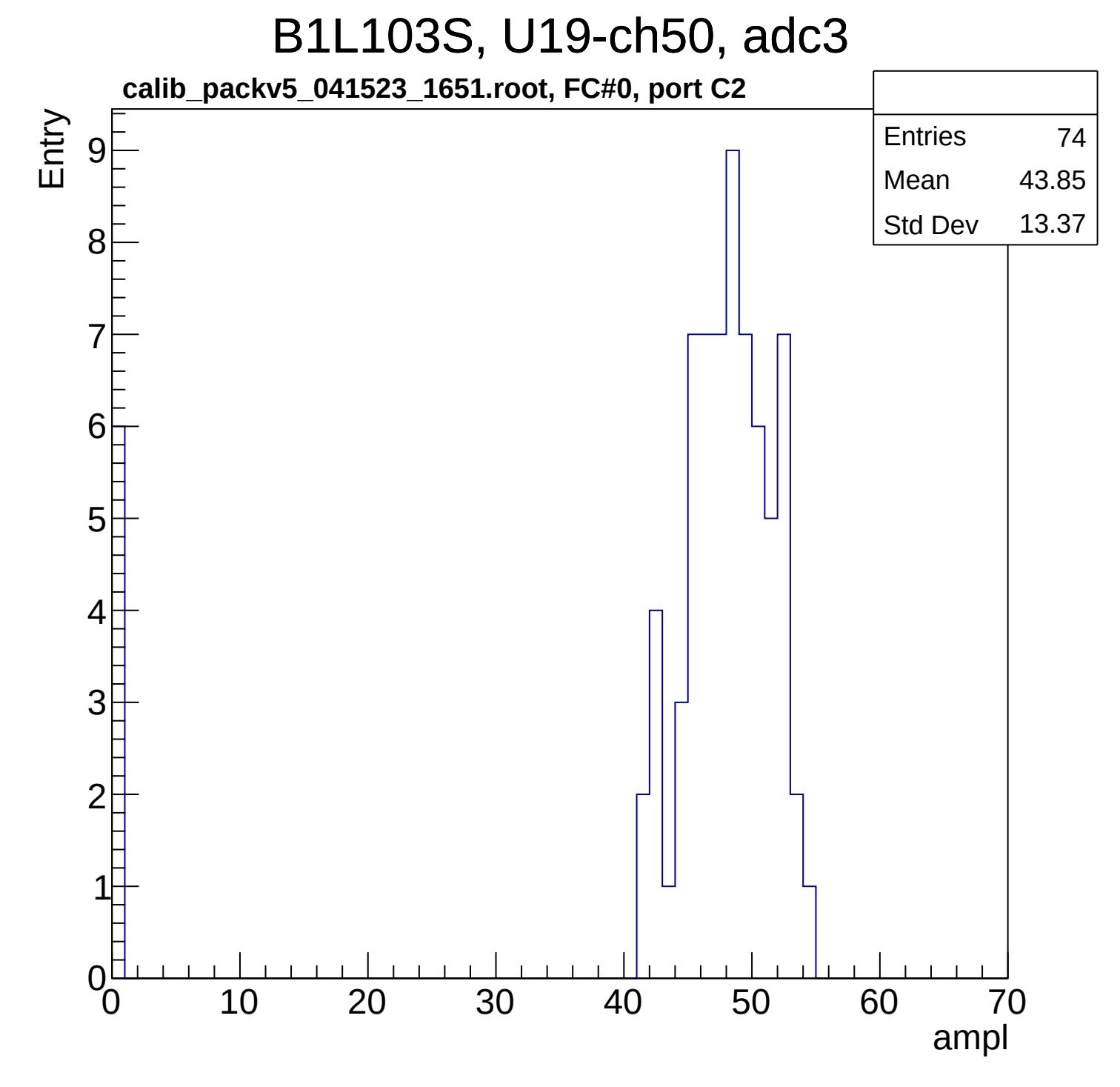
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch50, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 43.85
Std Dev 13.37
Entry
ampl
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2
3
4
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6
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0
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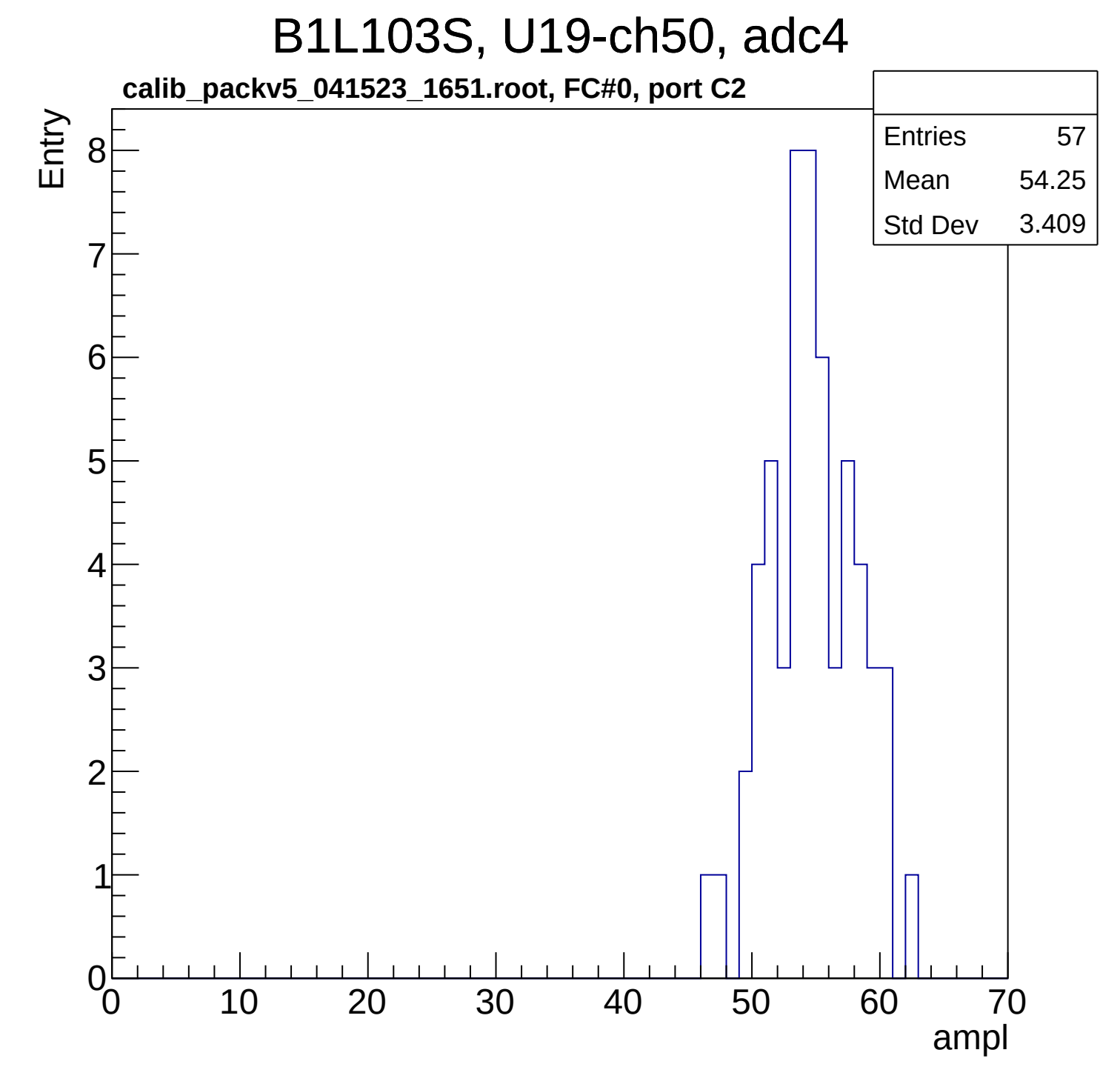
B1L103S, U19-ch50, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 54.25
Std Dev 3.409
Entry
ampl
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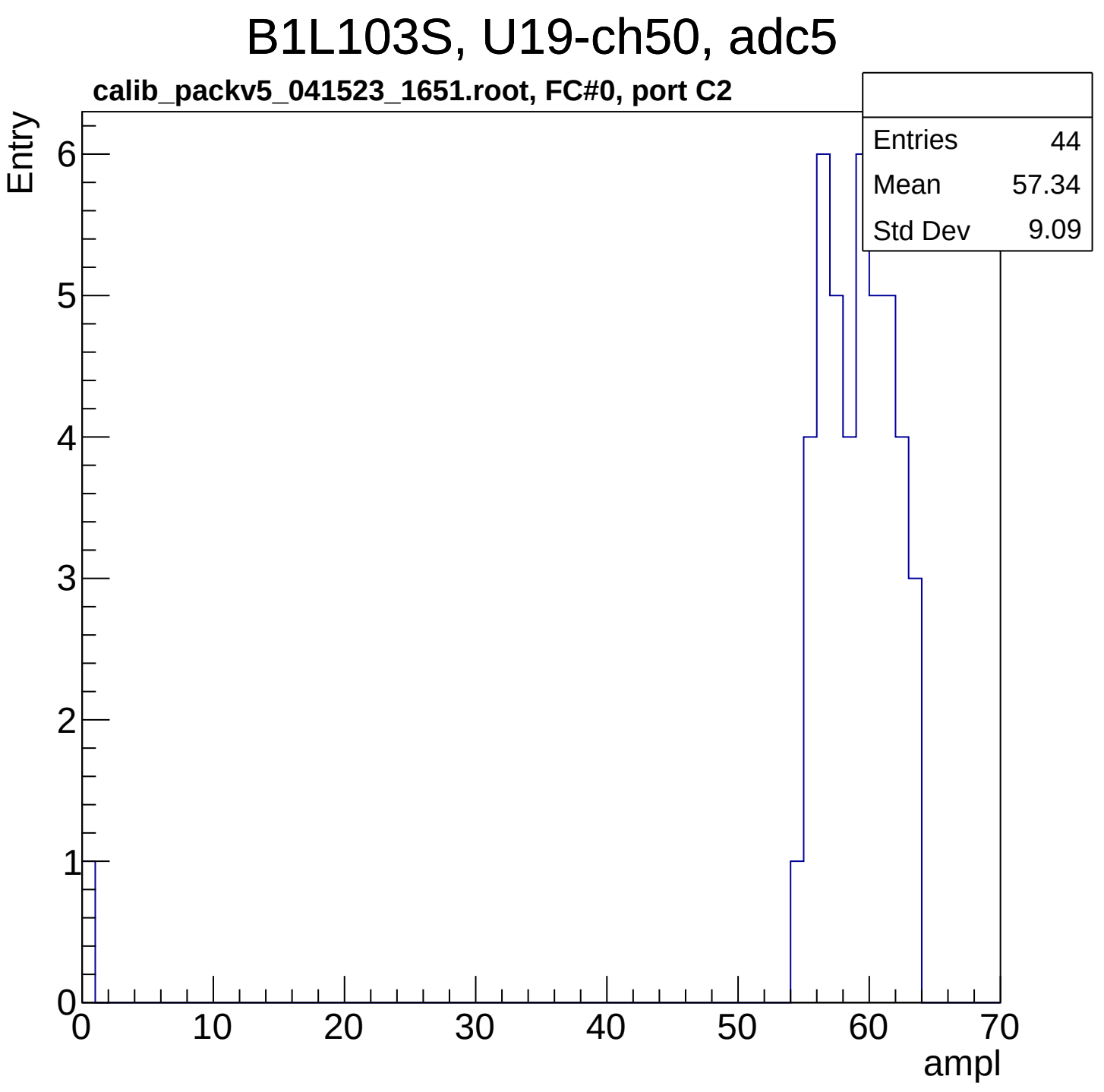
B1L103S, U19-ch50, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 57.34
Std Dev 9.09
Entry
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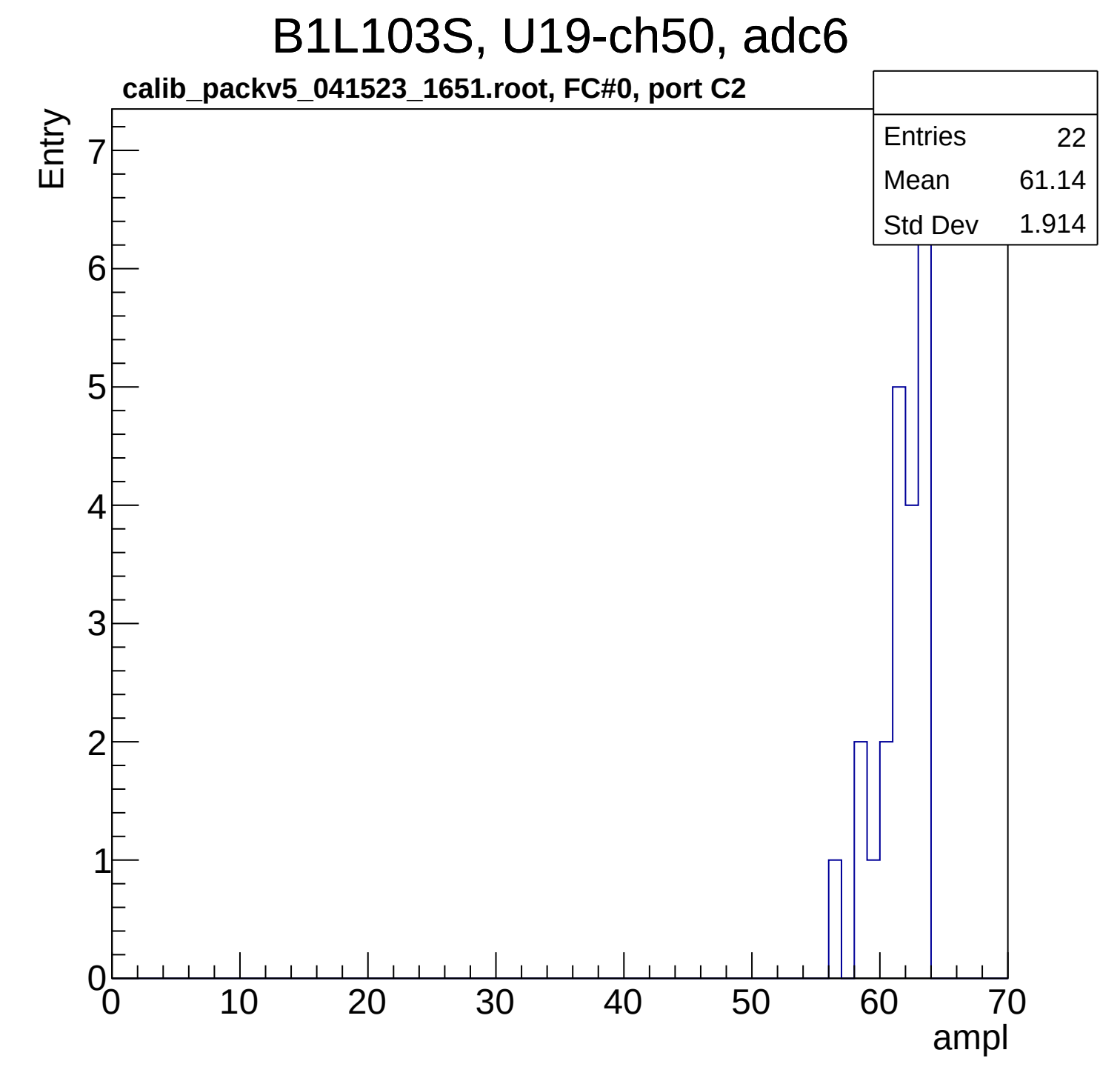
70
ampl


B1L103S, U19-ch50, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 61.14
Std Dev 1.914
Entry
ampl
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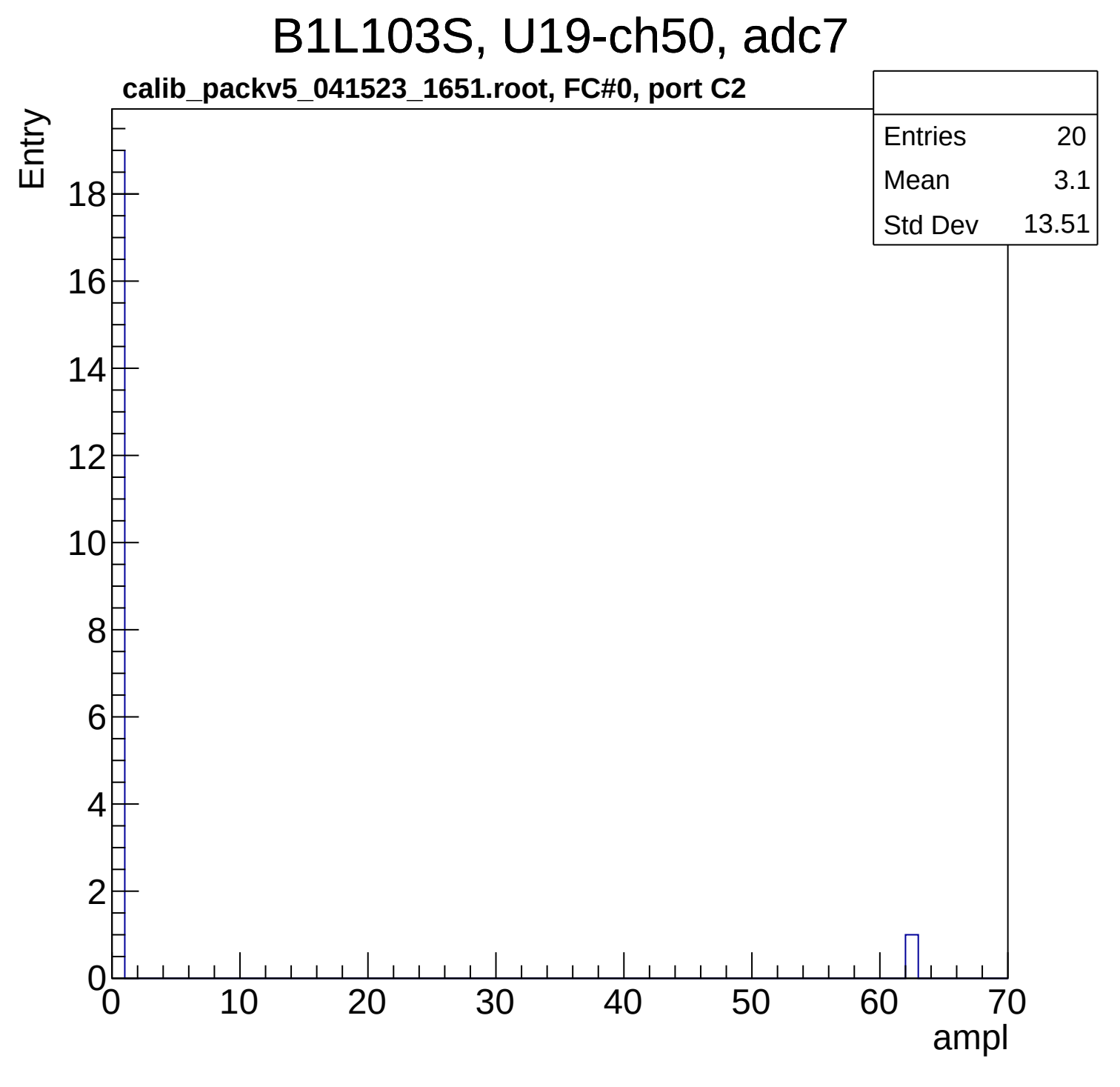
B1L103S, U19-ch50, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
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6
8
10
12
14
16
18
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10
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30
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50
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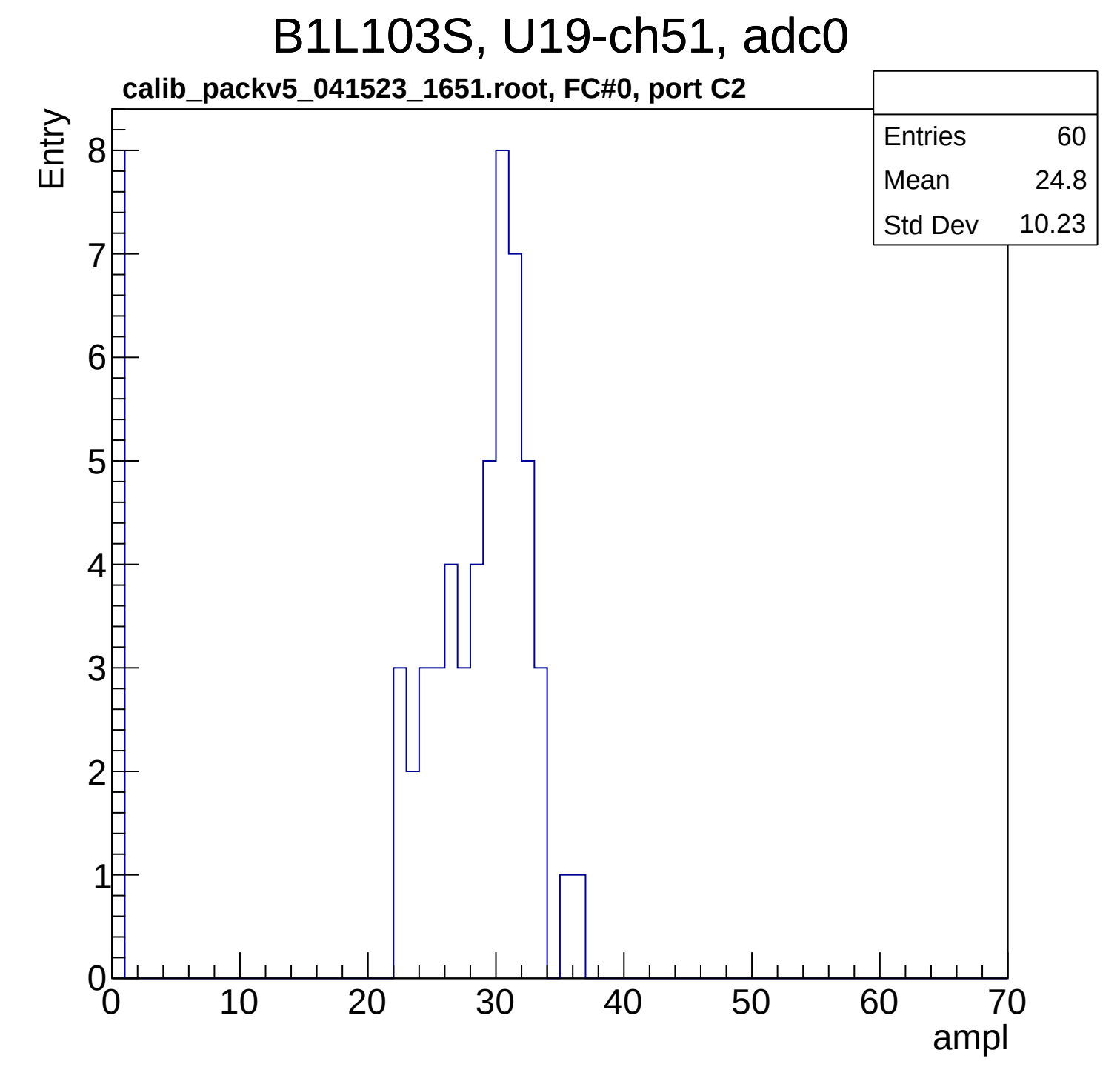
70
ampl


B1L103S, U19-ch51, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 24.8
Std Dev 10.23
Entry
ampl
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7
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40
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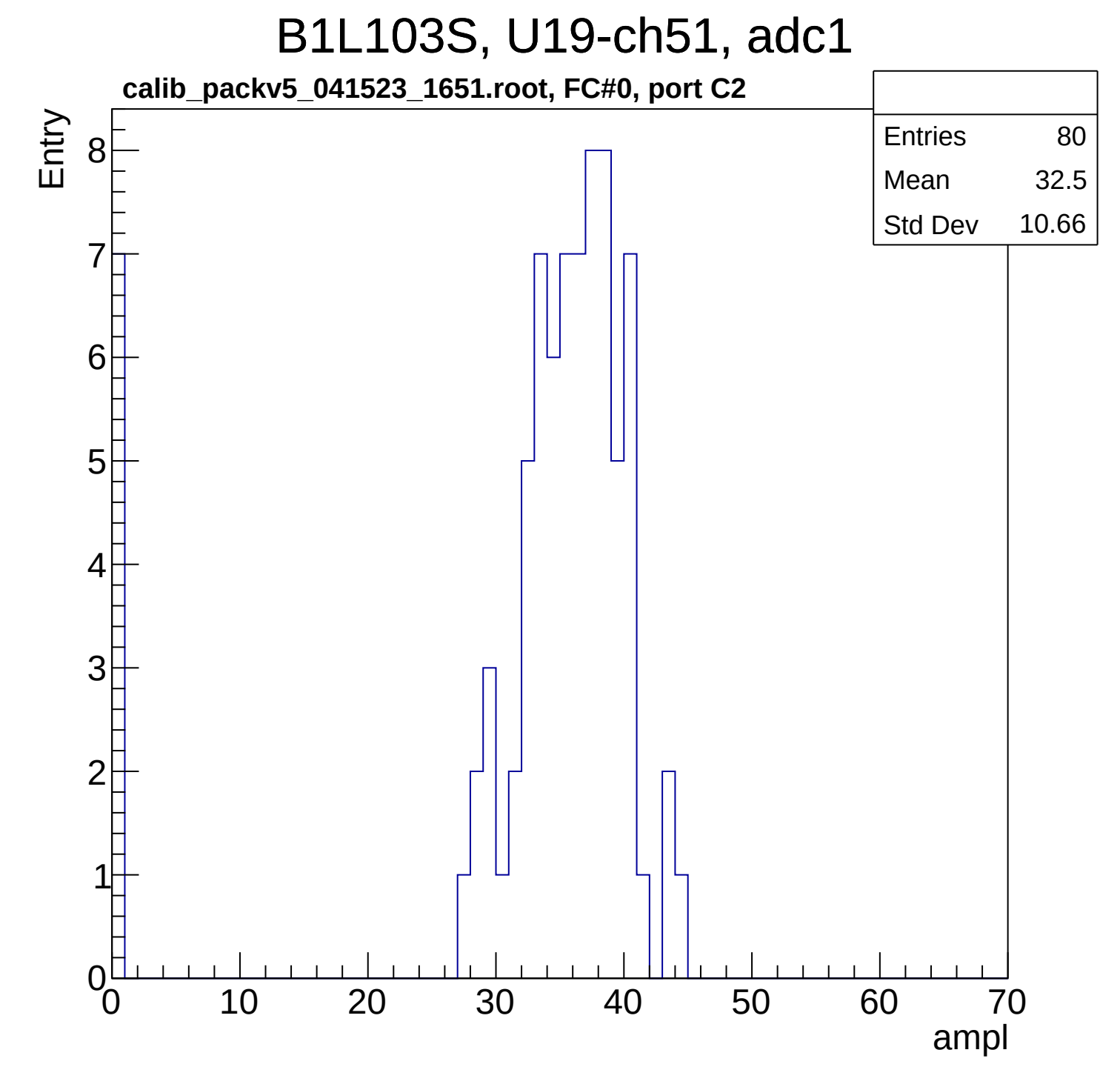
B1L103S, U19-ch51, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 32.5
Std Dev 10.66
Entry
ampl
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2
3
4
5
6
7
8
0
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40
50
60
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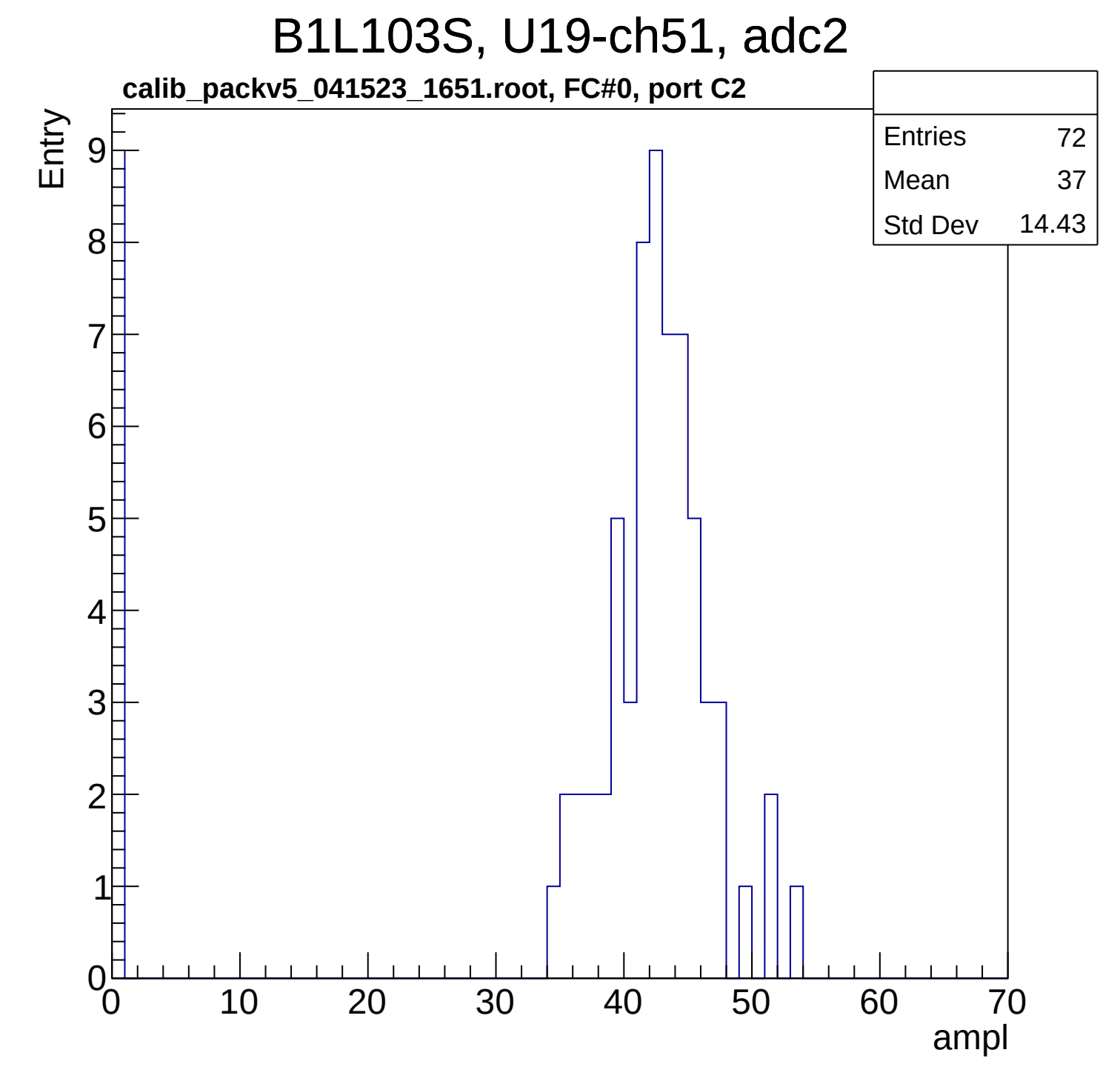
B1L103S, U19-ch51, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 37
Std Dev 14.43
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
50
60
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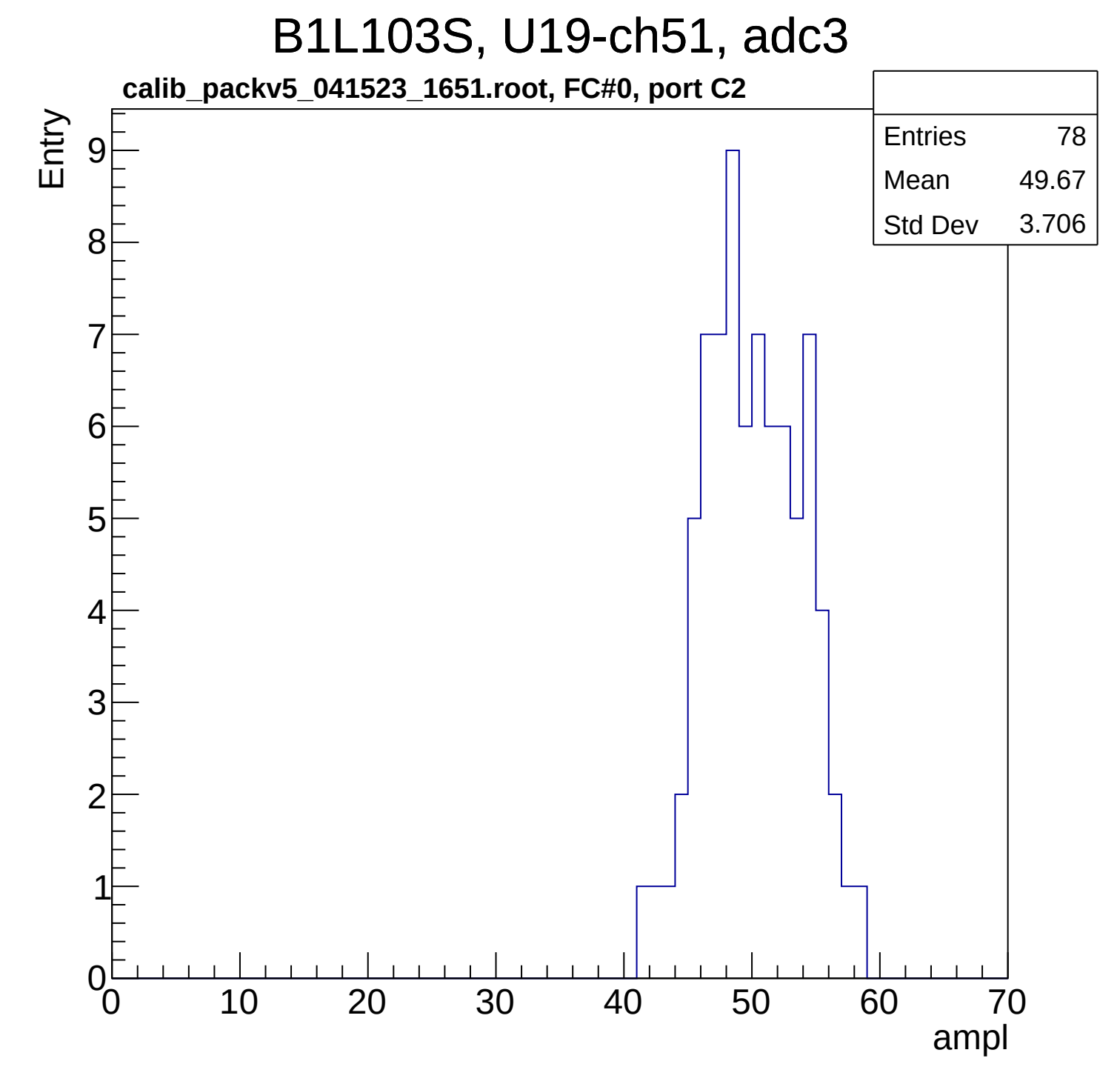
B1L103S, U19-ch51, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 49.67
Std Dev 3.706
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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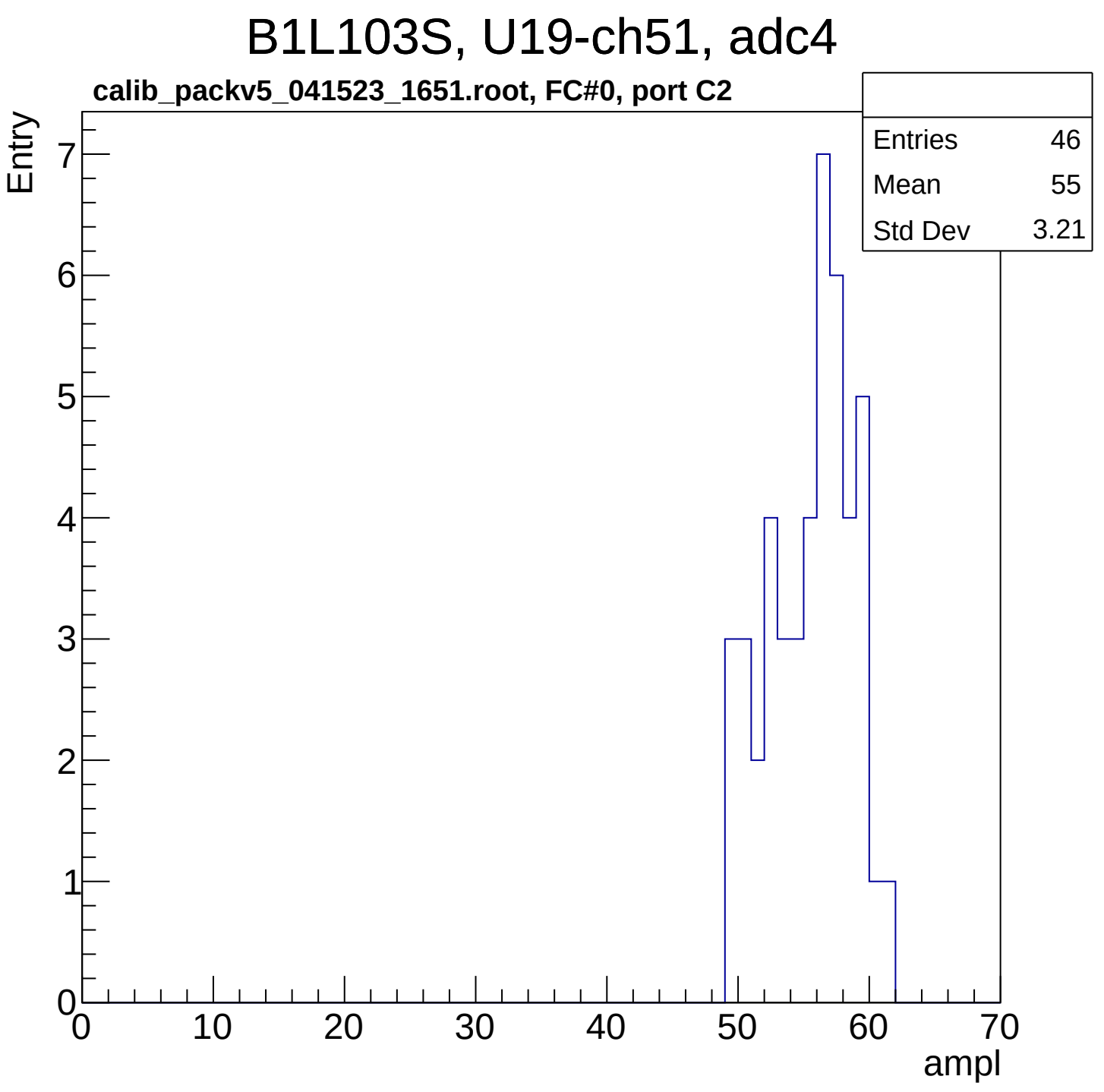
B1L103S, U19-ch51, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 55
Std Dev 3.21
Entry
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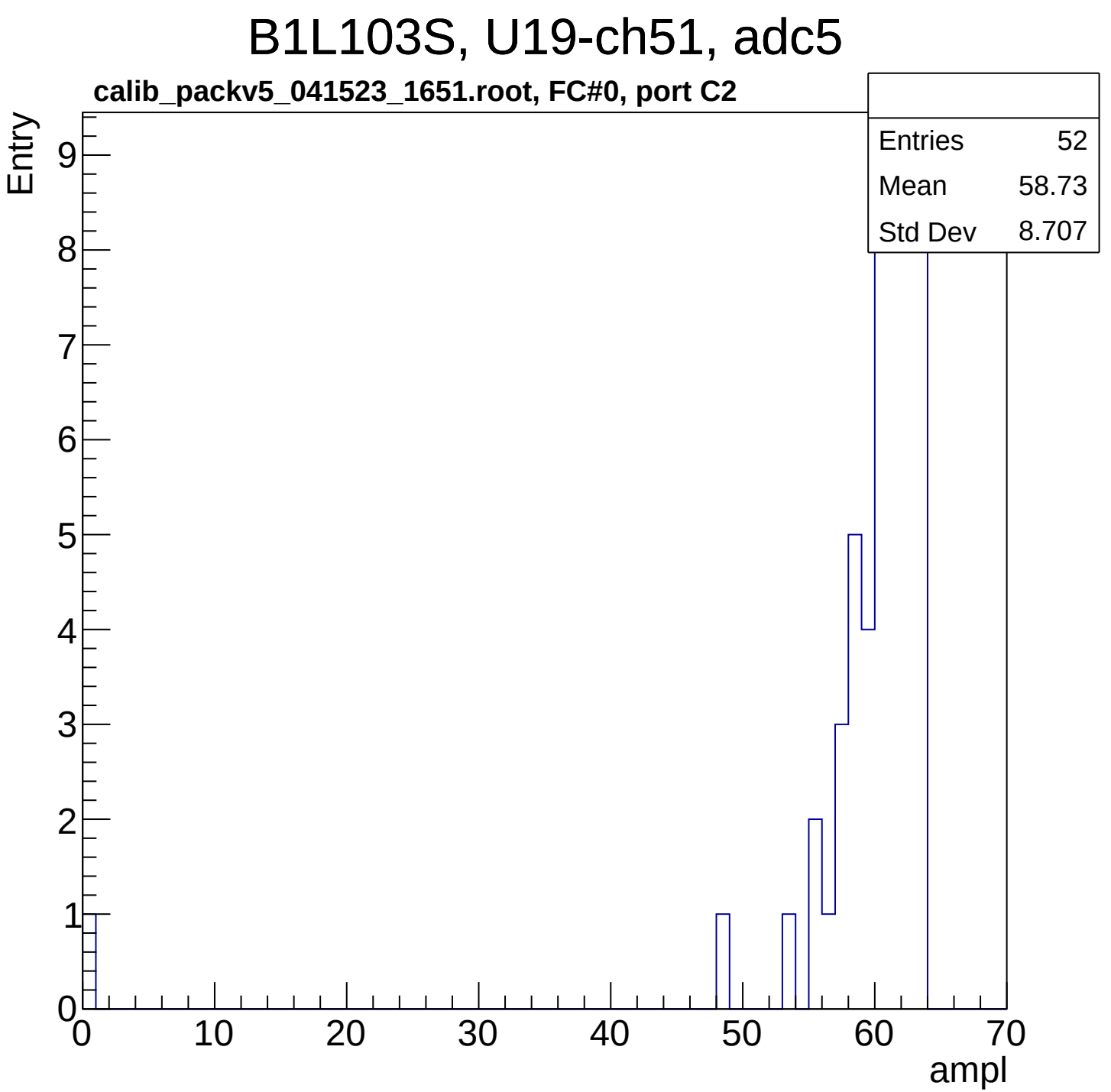
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch51, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 58.73
Std Dev 8.707
Entry
ampl
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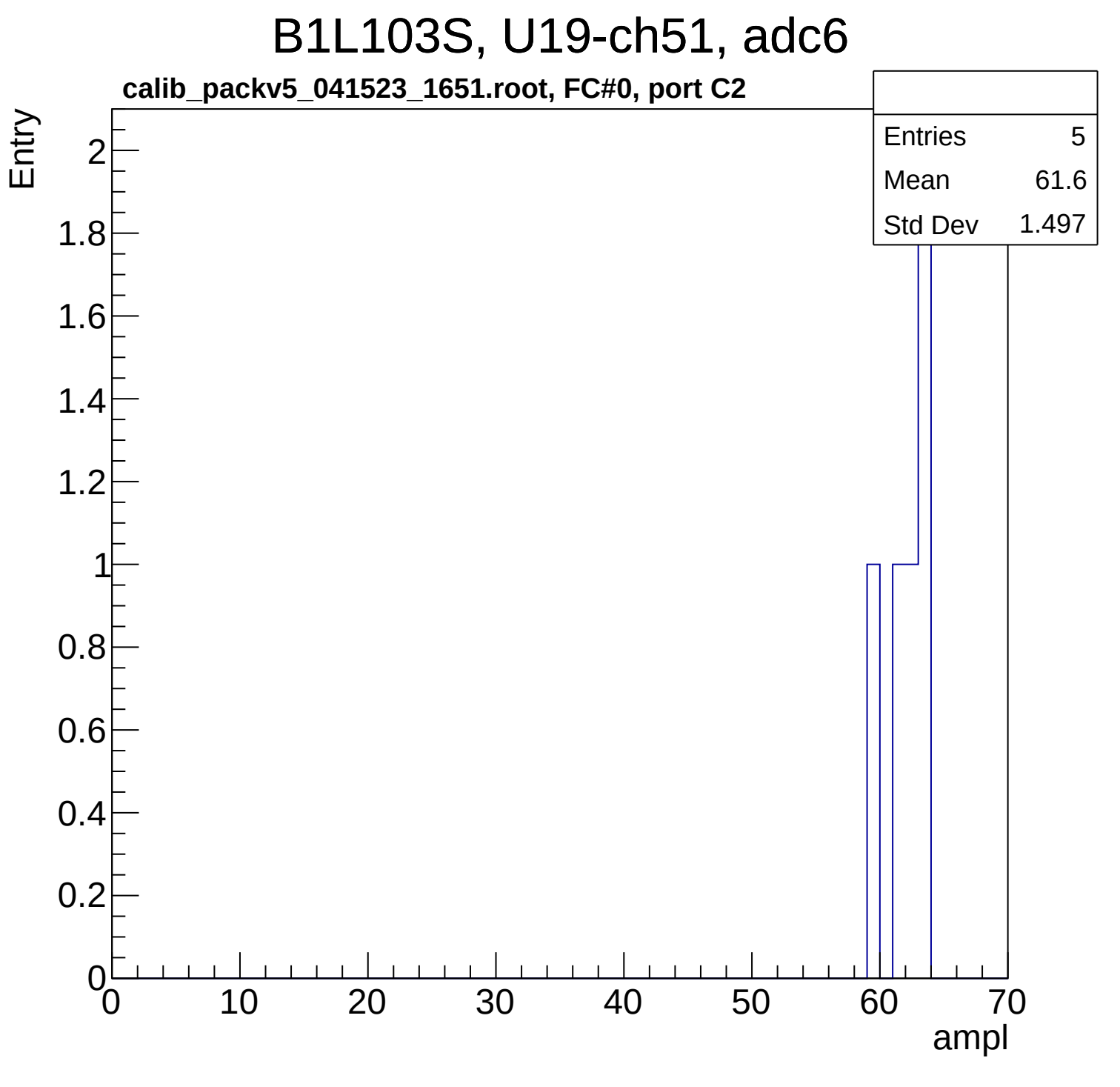
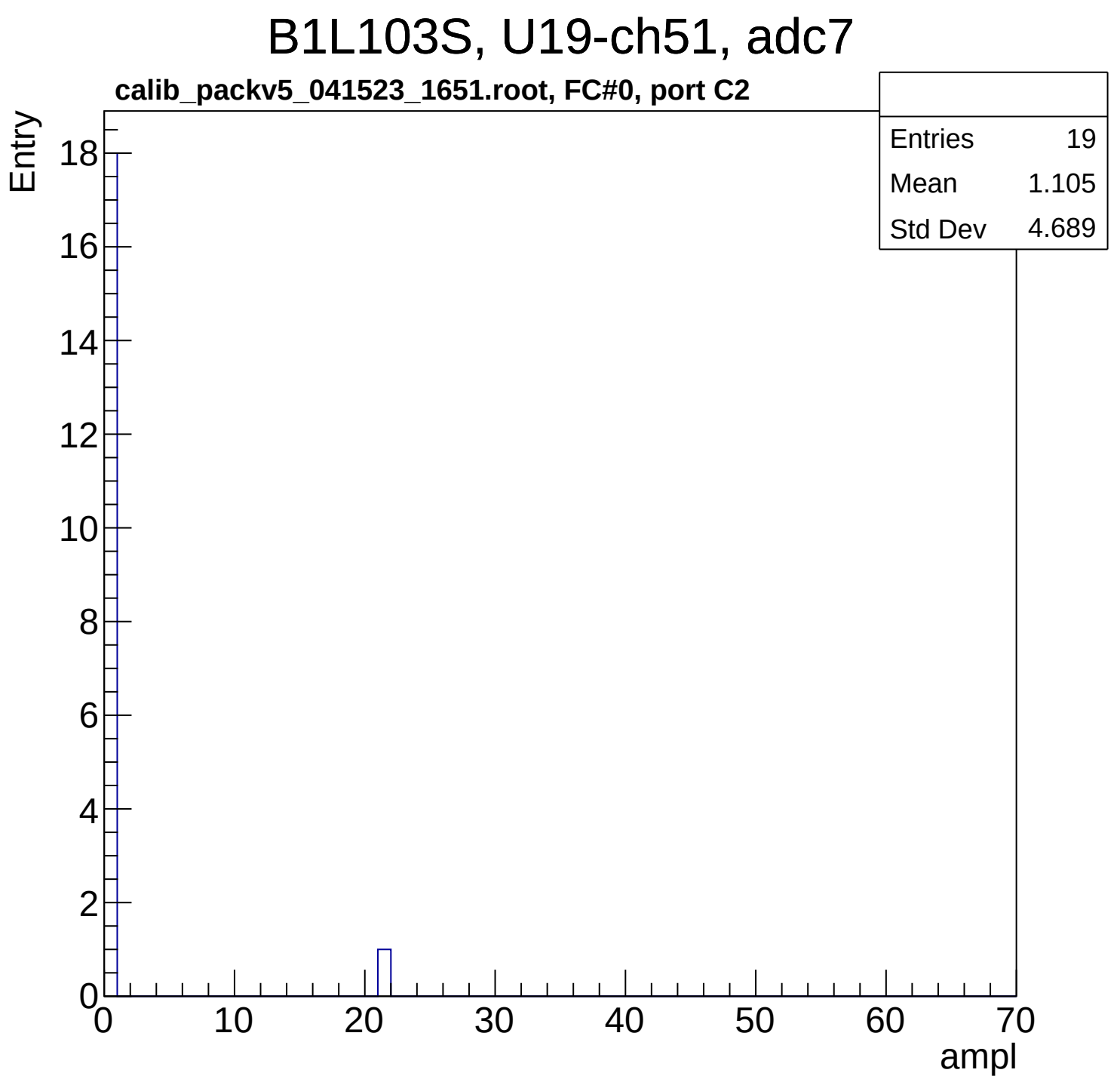
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch51, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 61.6
Std Dev 1.497
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U19-ch51, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.105
Std Dev 4.689
Entry
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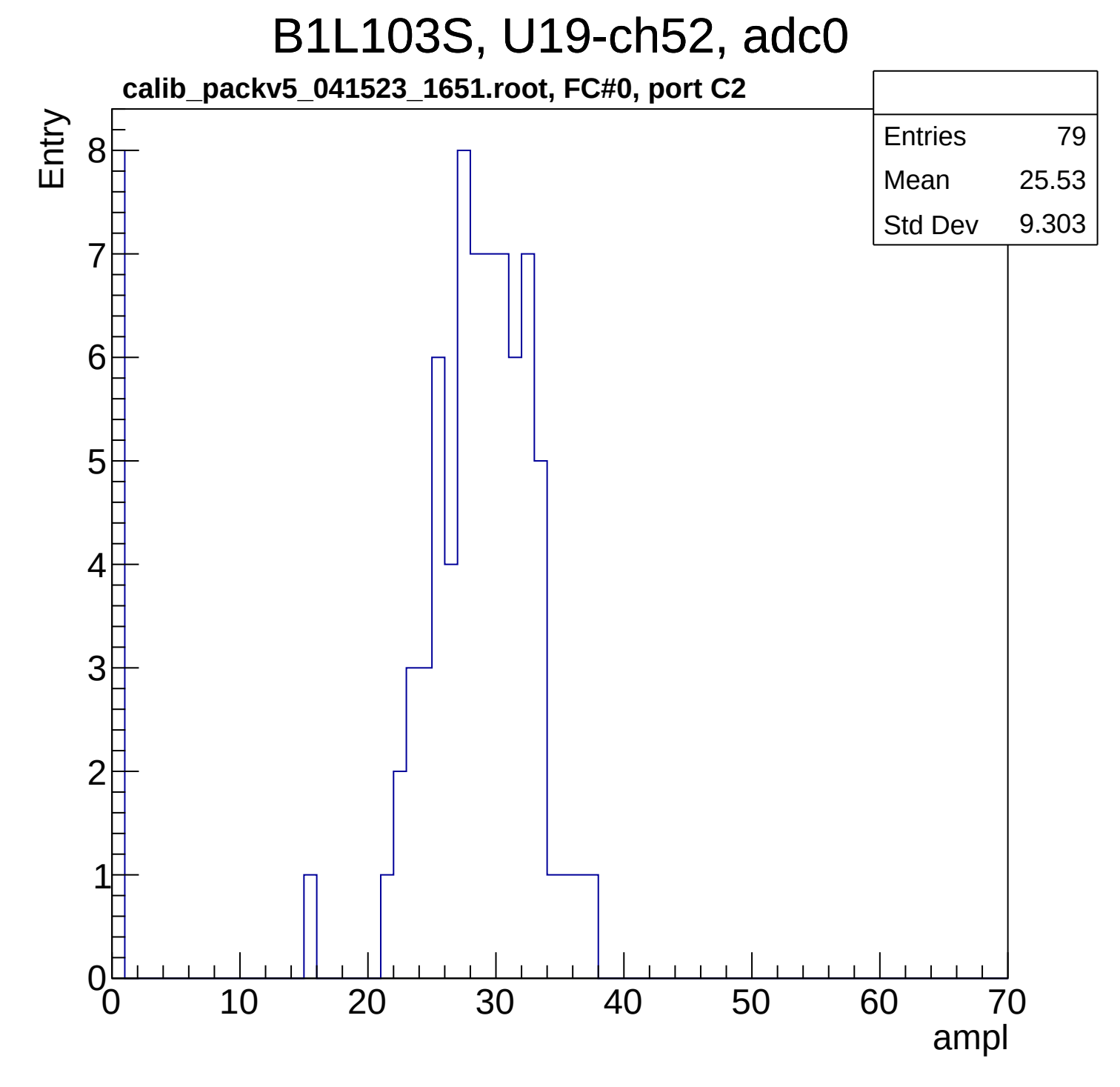
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch52, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 25.53
Std Dev 9.303
Entry
ampl
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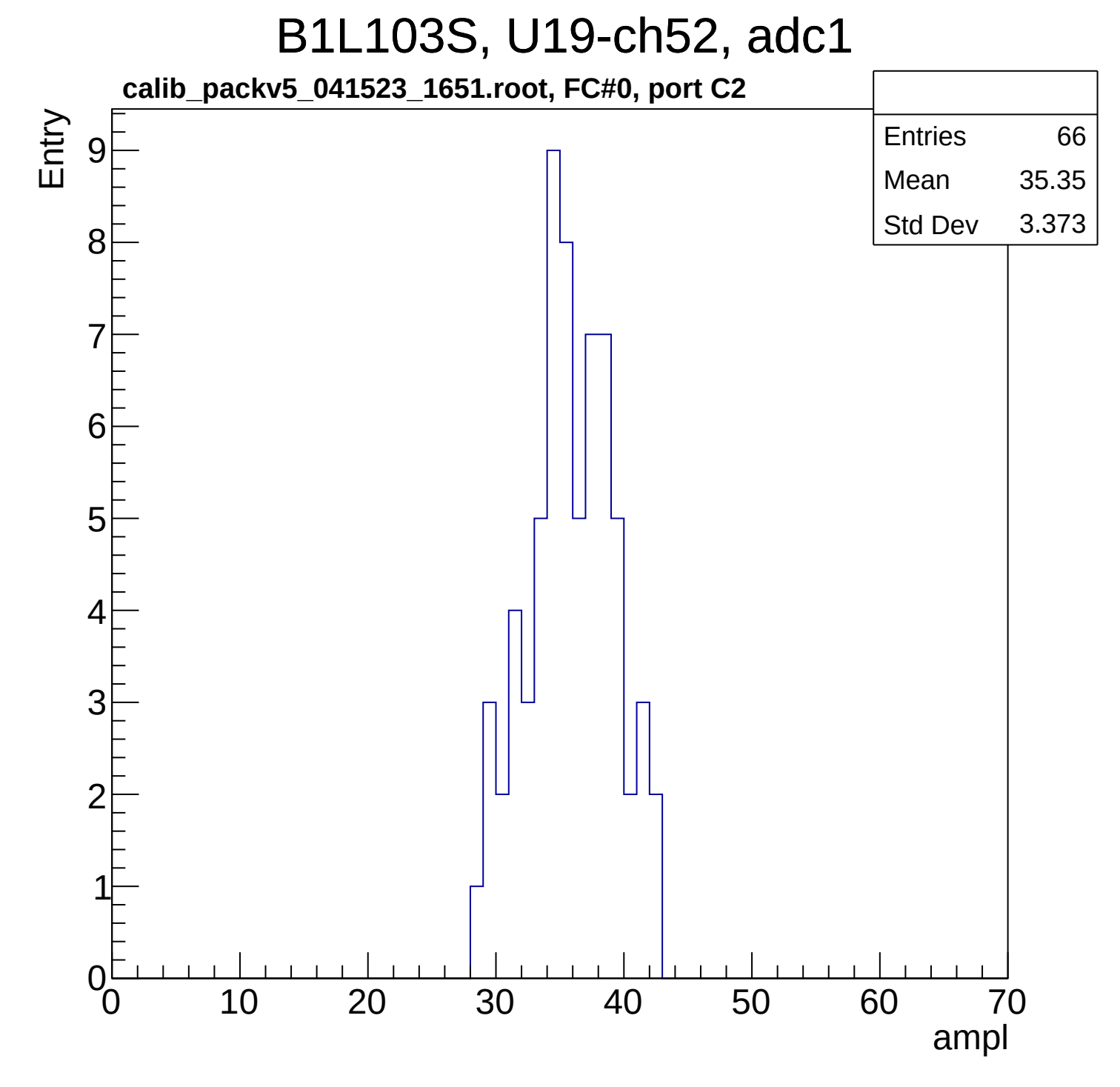
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch52, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 35.35
Std Dev 3.373
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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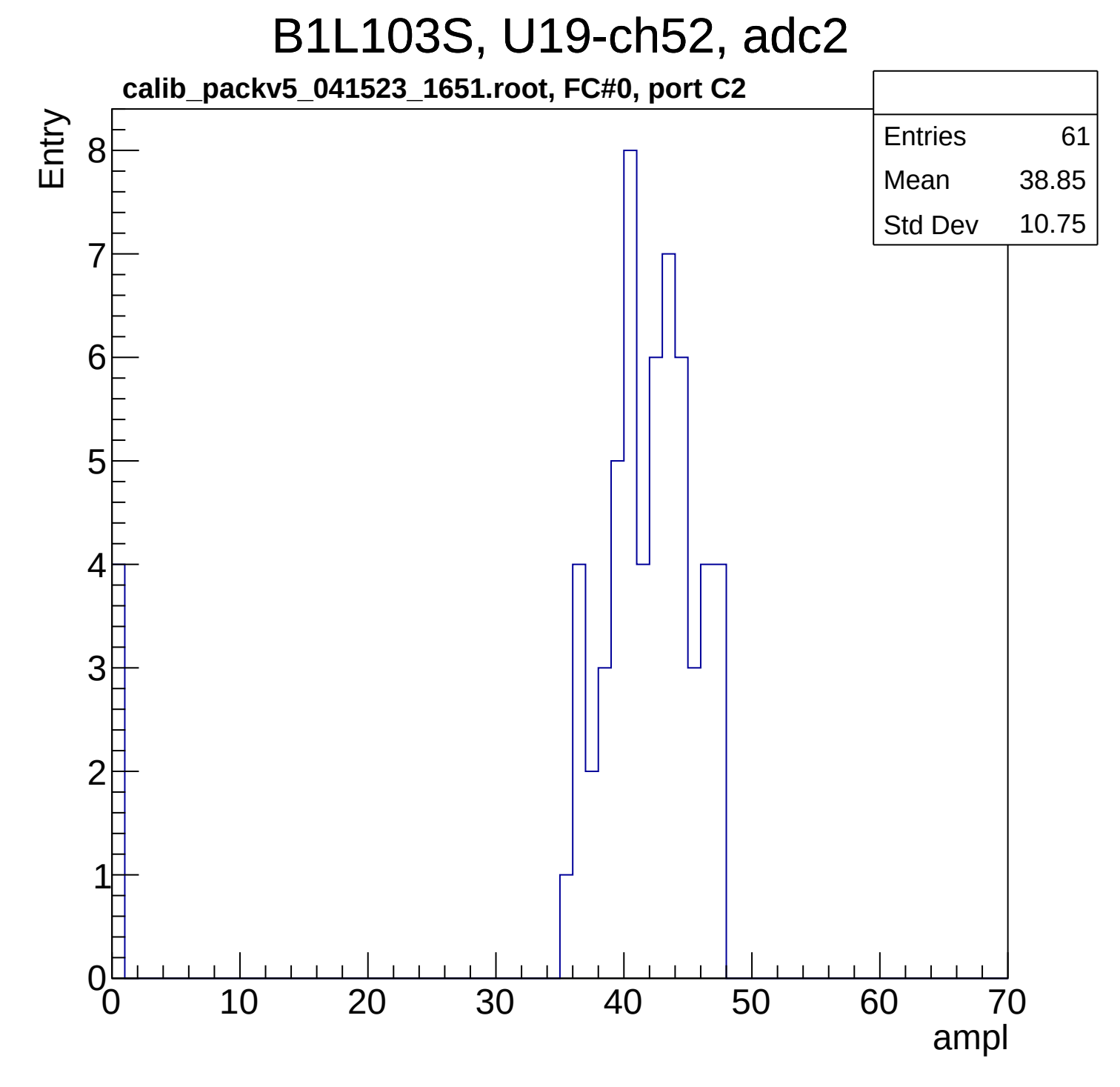
B1L103S, U19-ch52, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 38.85
Std Dev 10.75
Entry
ampl
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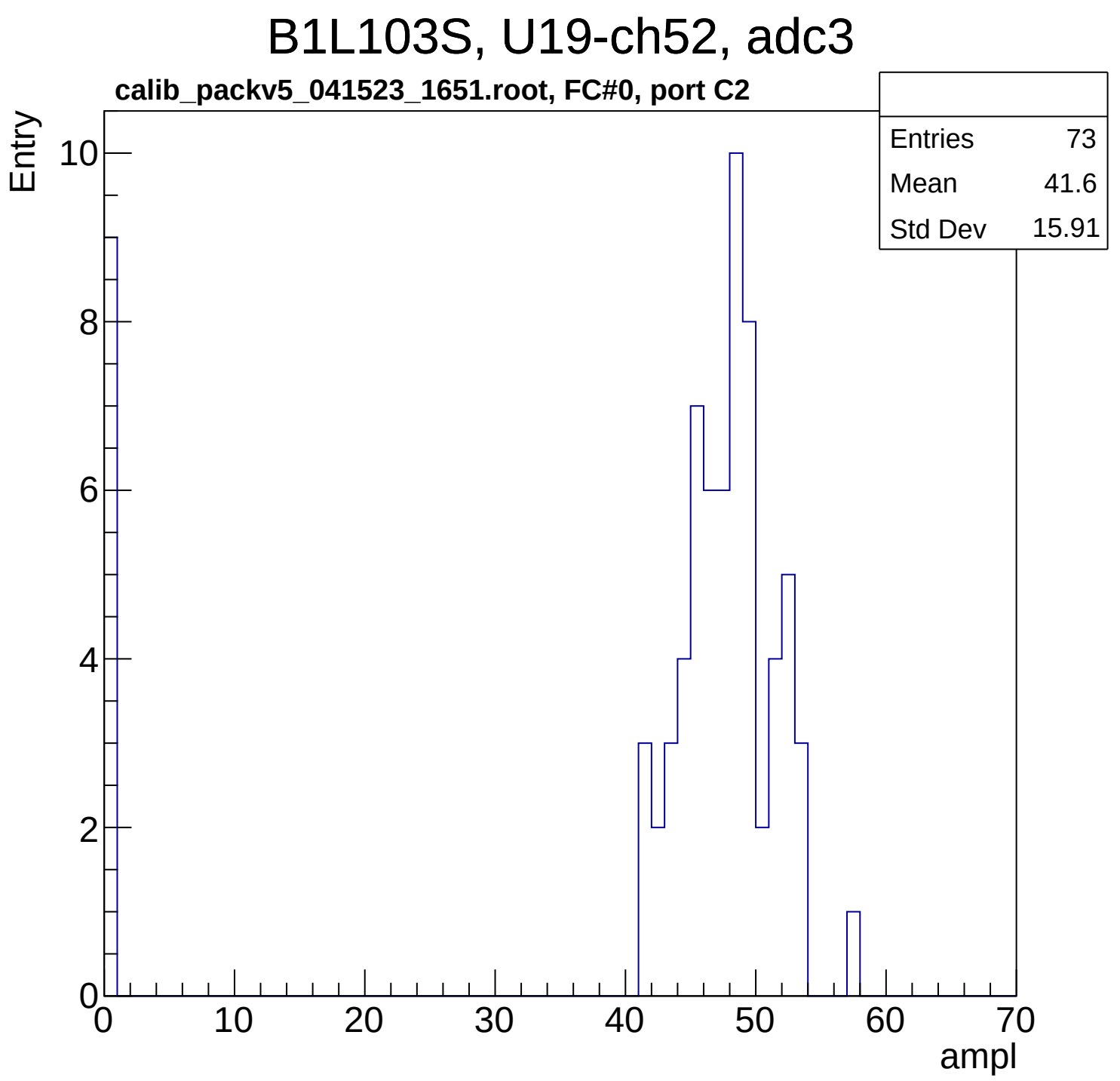
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch52, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 41.6
Std Dev 15.91
Entry
ampl
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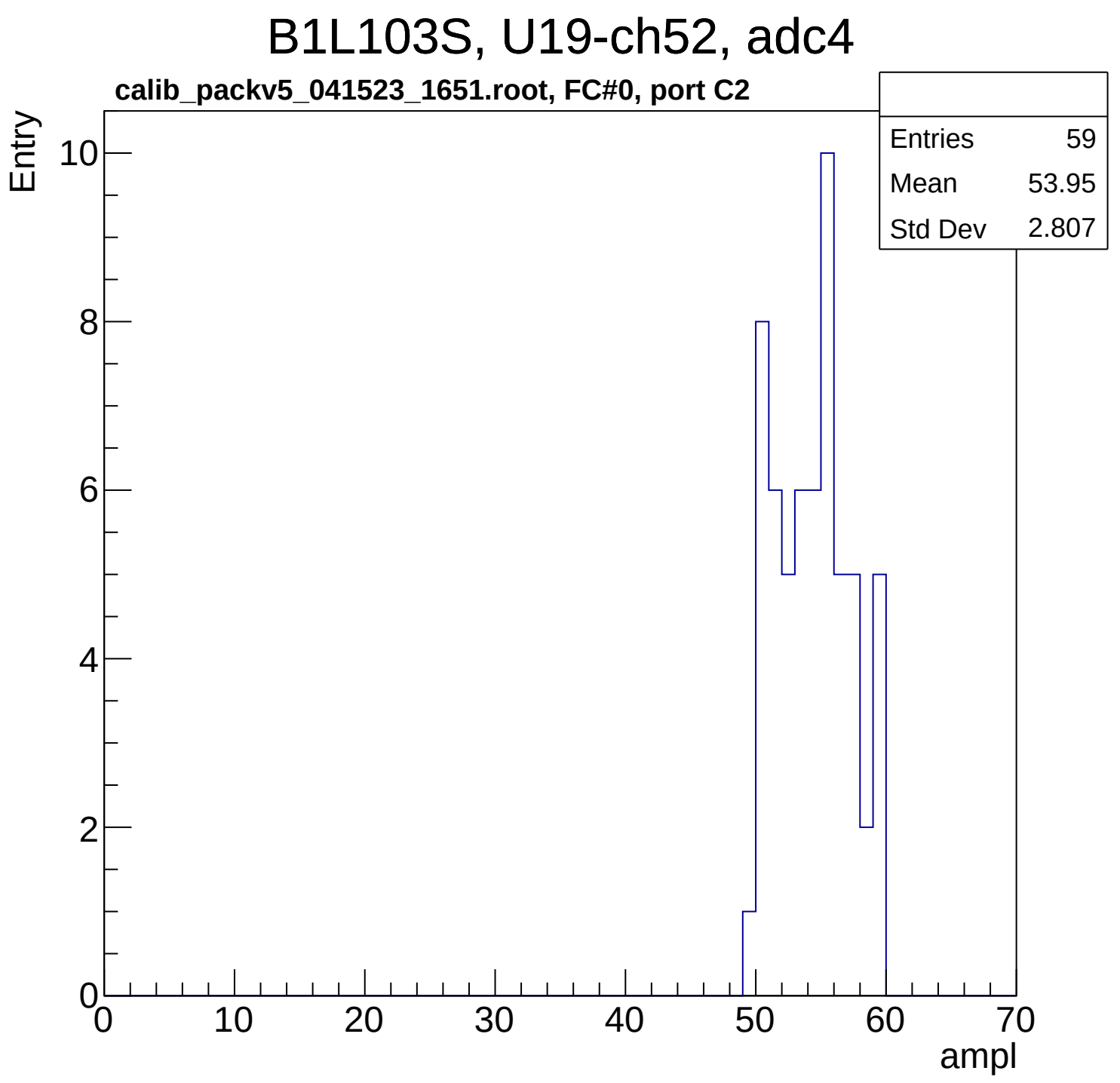
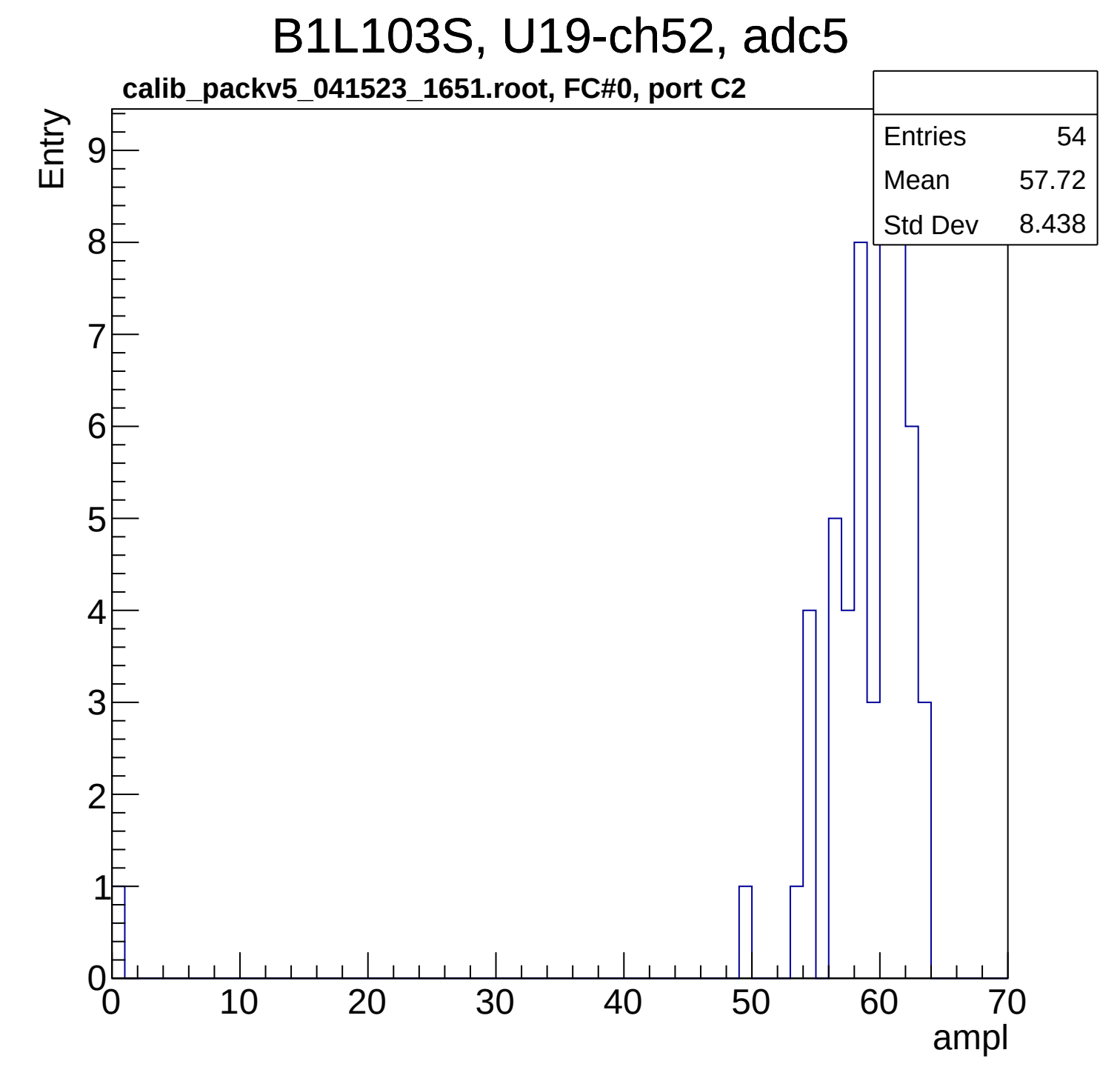
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U19-ch52, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 53.95
Std Dev 2.807
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch52, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 57.72
Std Dev 8.438
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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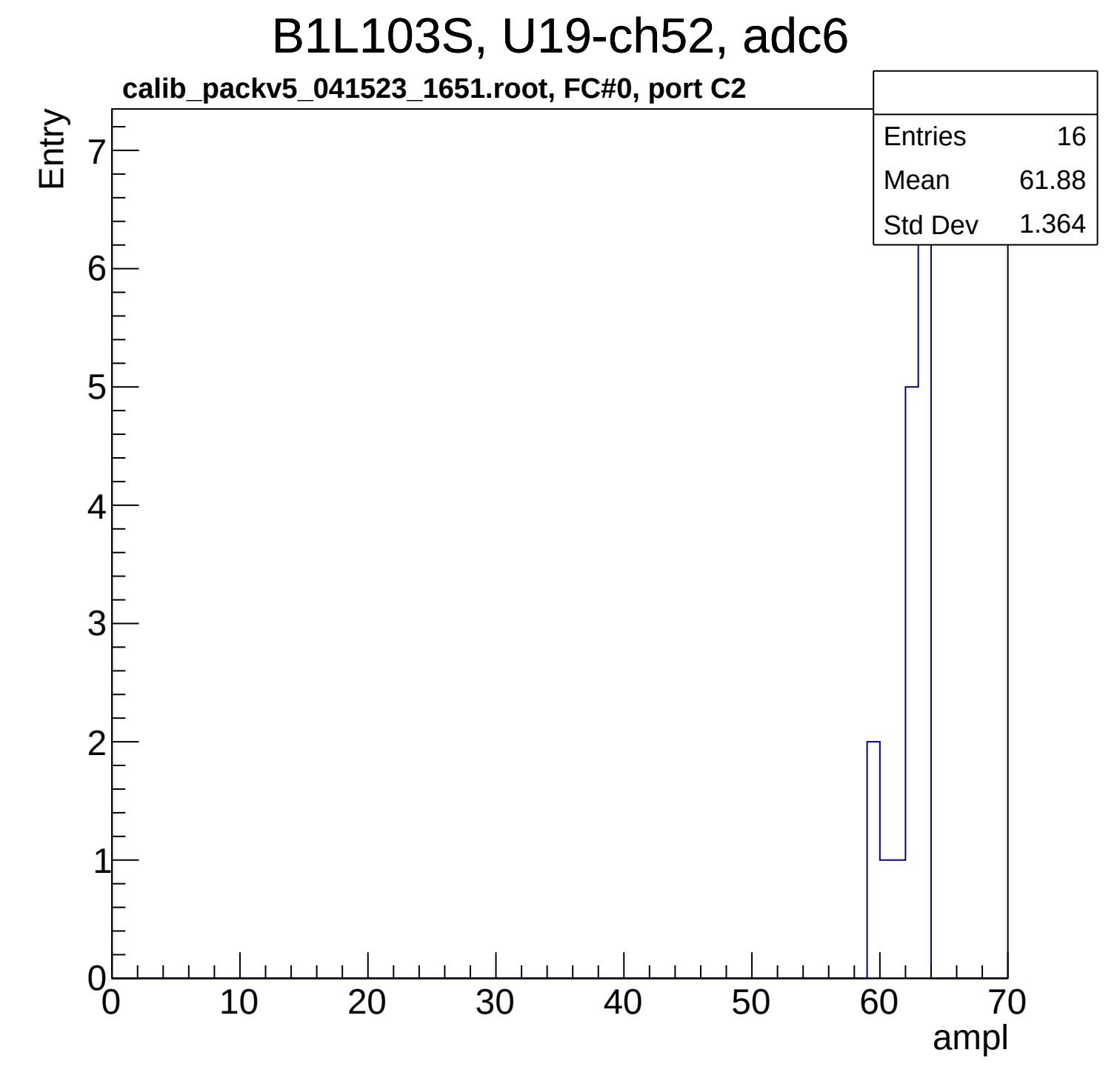
40
50
60
70


B1L103S, U19-ch52, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 61.88
Std Dev 1.364
Entry
ampl
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1
2
3
4
5
6
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0
10
20
30
40
50
60
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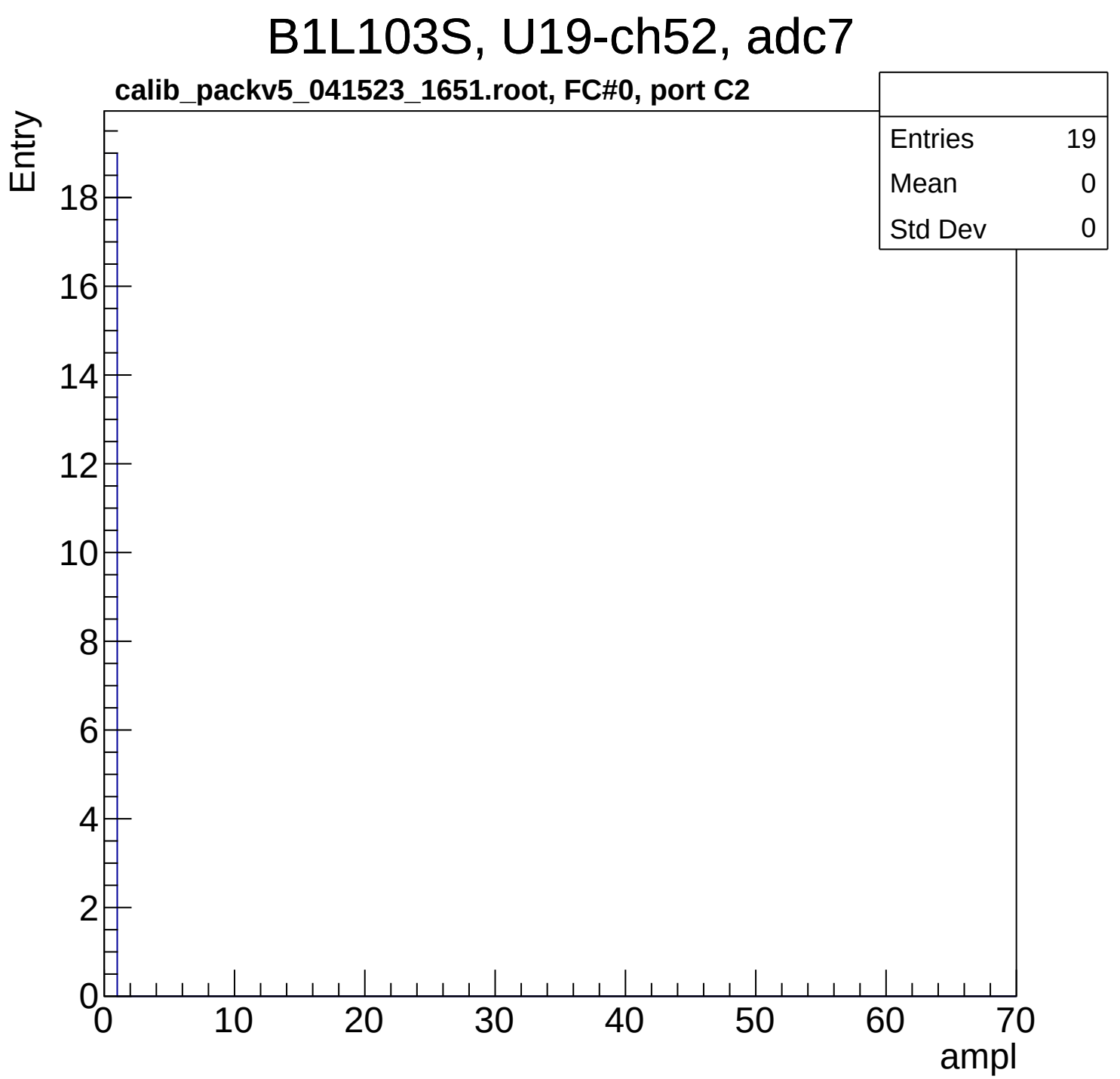
B1L103S, U19-ch52, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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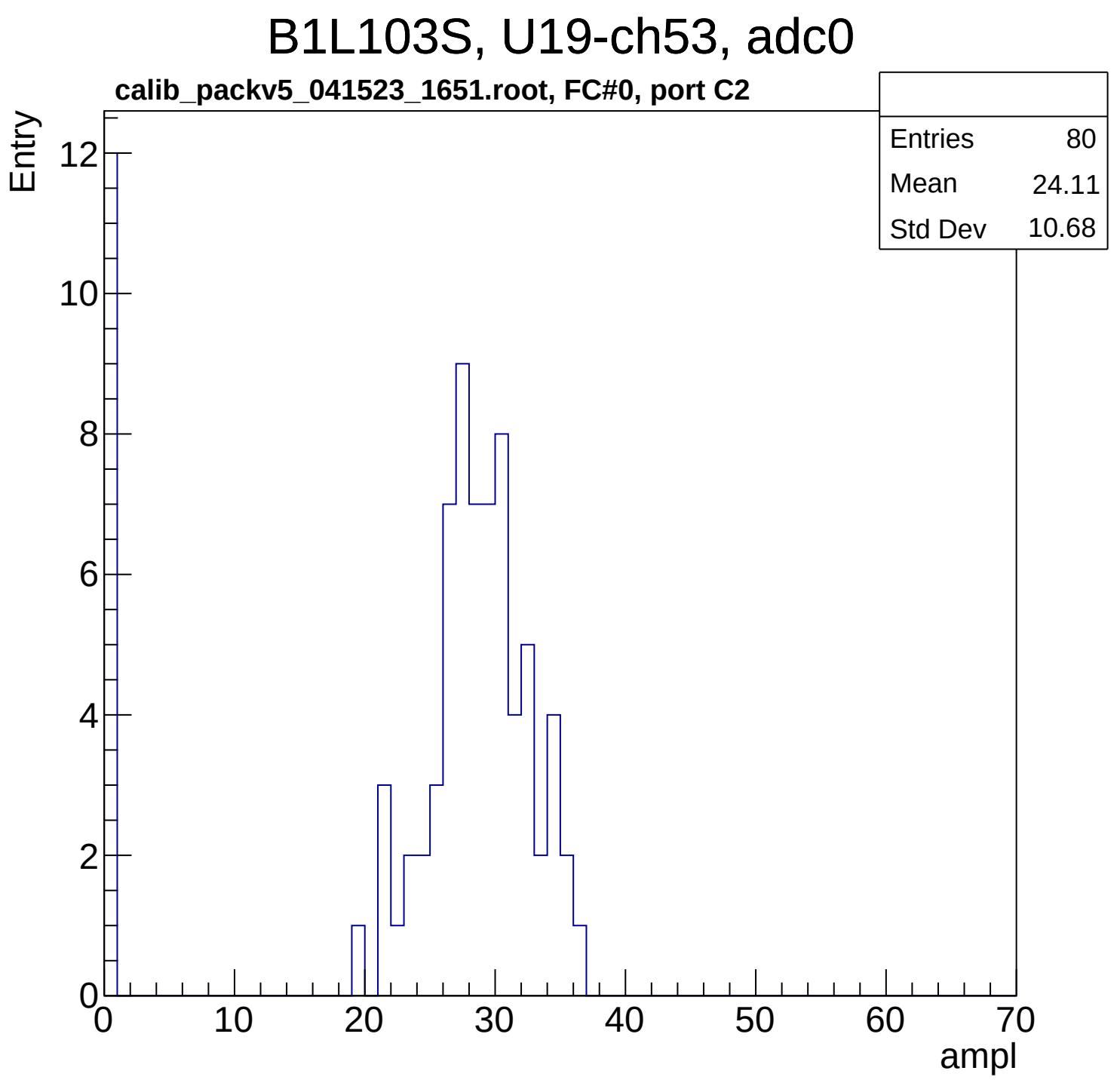
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch53, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 24.11
Std Dev 10.68
Entry
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2
4
6
8
10
12
0
10
20
30
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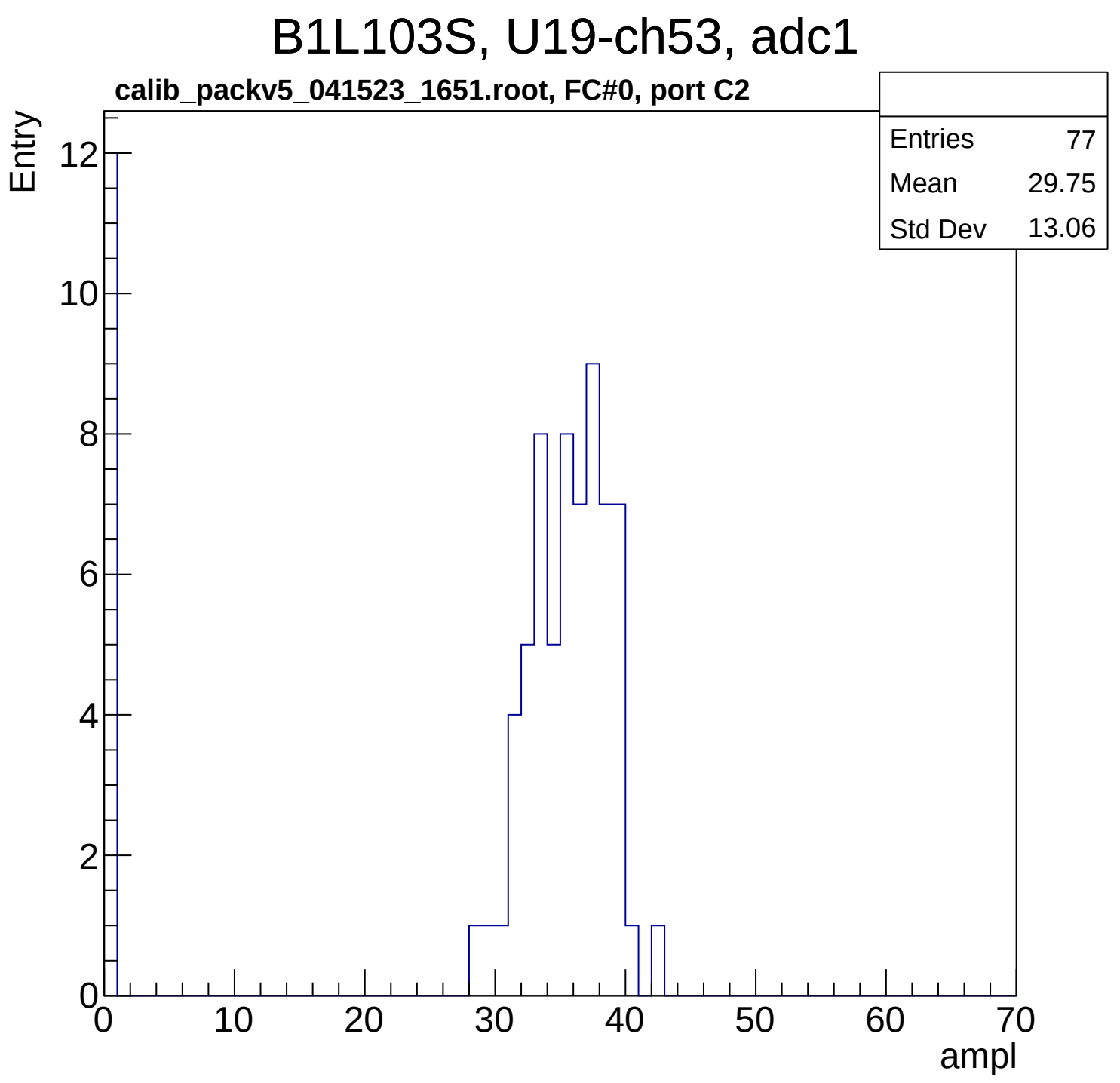
50
60
70
ampl


B1L103S, U19-ch53, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 29.75
Std Dev 13.06
Entry
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4
6
8
10
12
0
10
20
30
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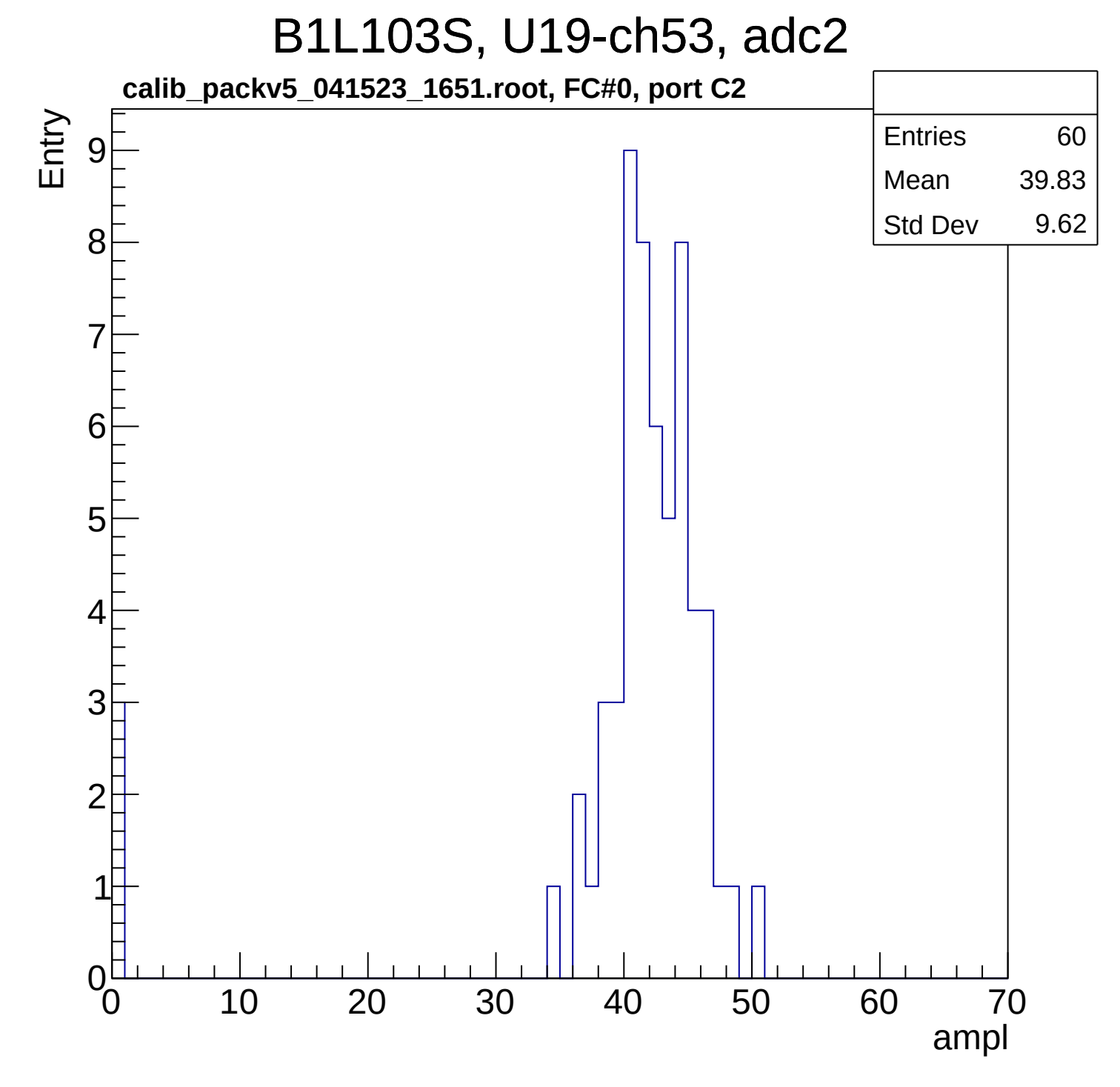
50
60
70
ampl


B1L103S, U19-ch53, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 39.83
Std Dev 9.62
Entry
ampl
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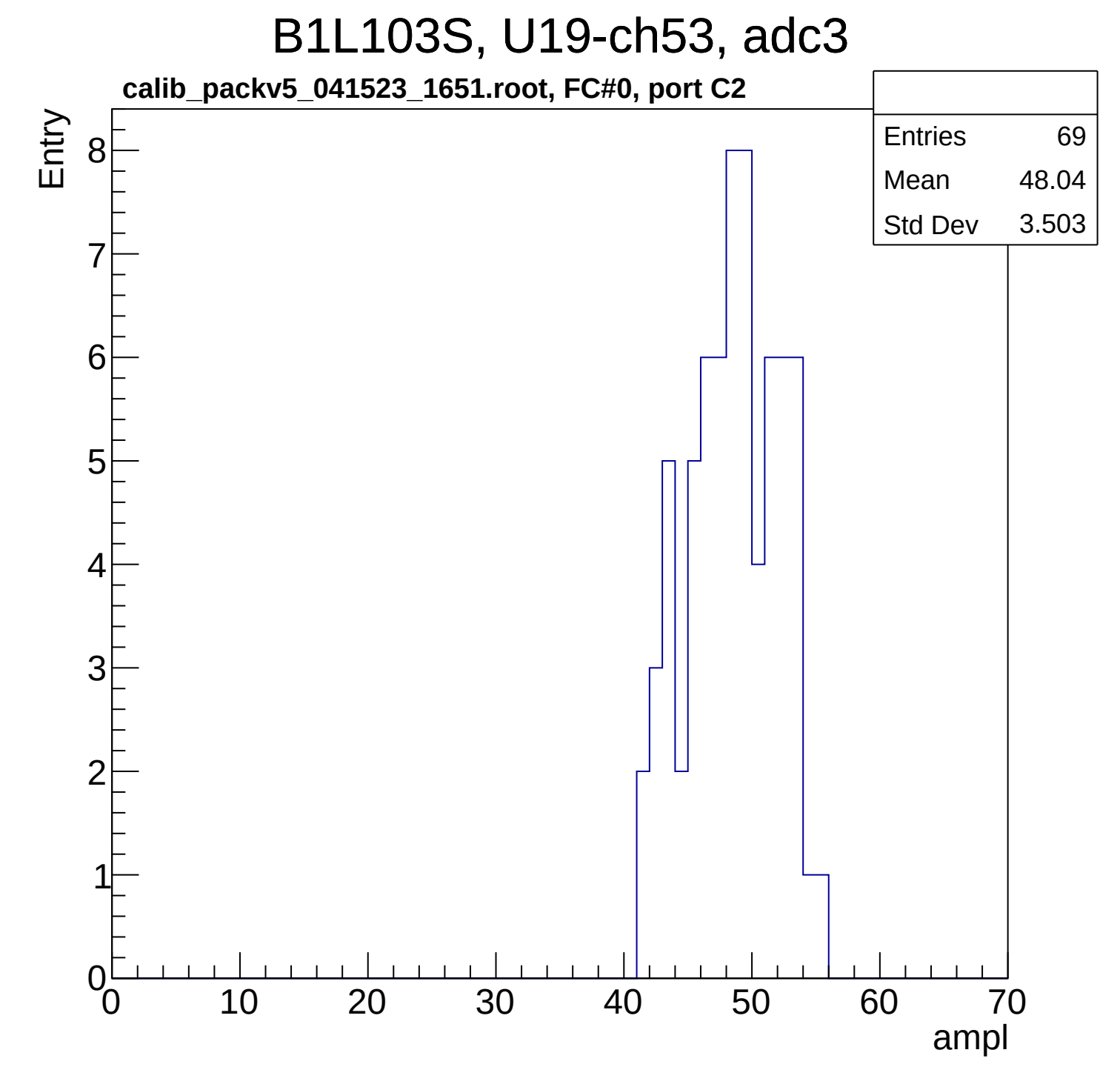
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch53, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 48.04
Std Dev 3.503
Entry
ampl
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2
3
4
5
6
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0
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60
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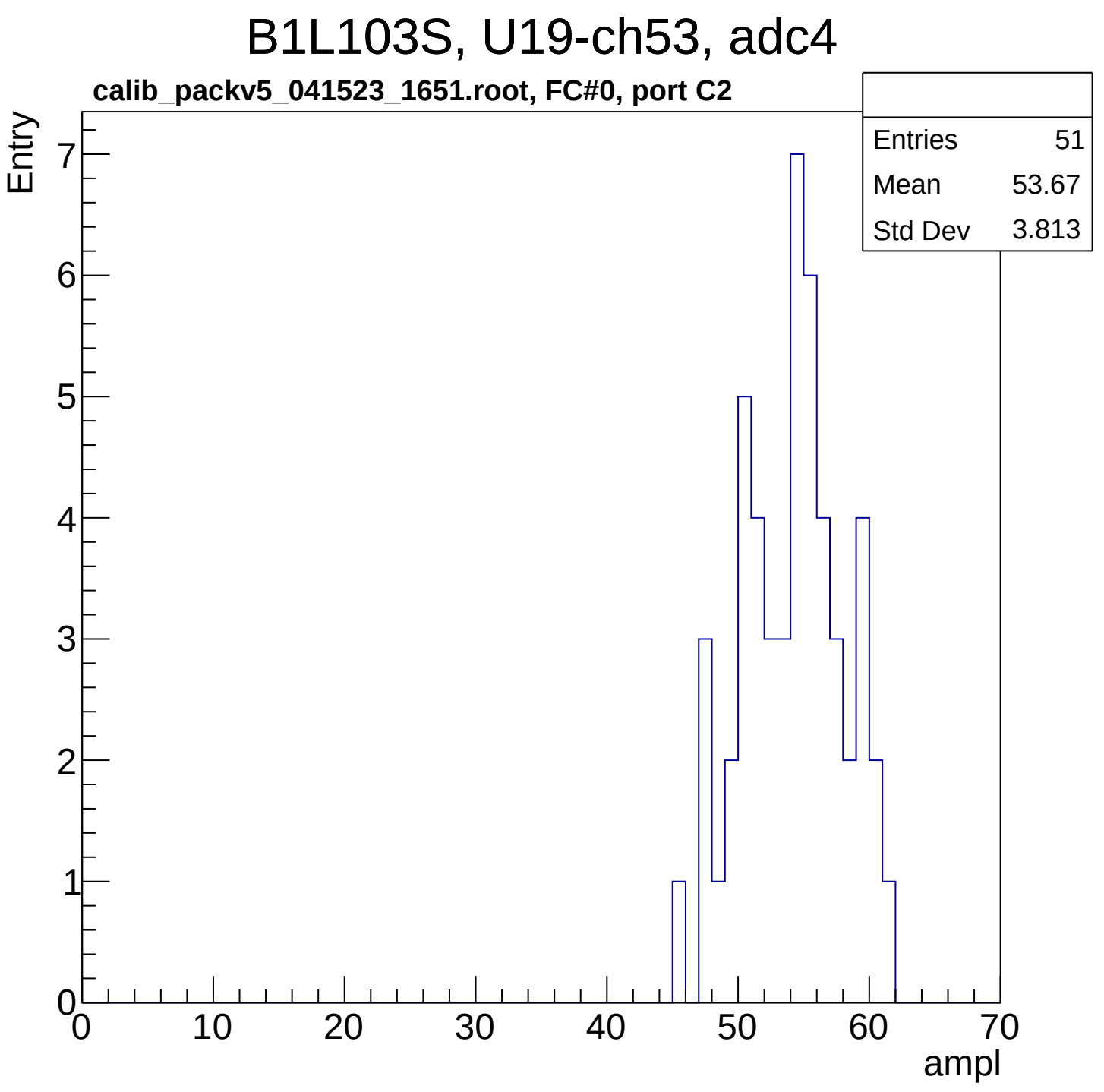
B1L103S, U19-ch53, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 53.67
Std Dev 3.813
Entry
ampl
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1
2
3
4
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0
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60
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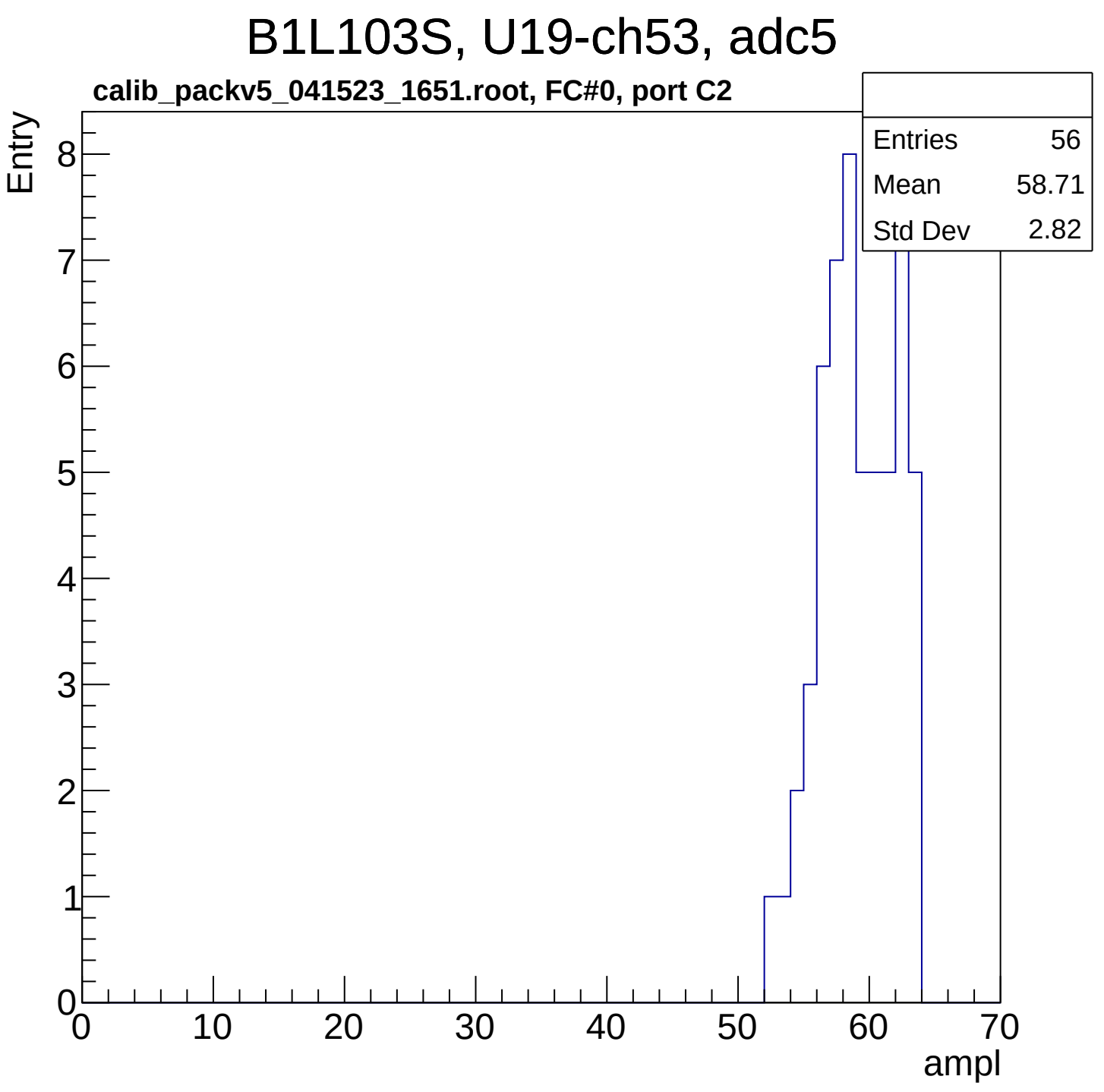
B1L103S, U19-ch53, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 58.71
Std Dev 2.82
Entry
ampl
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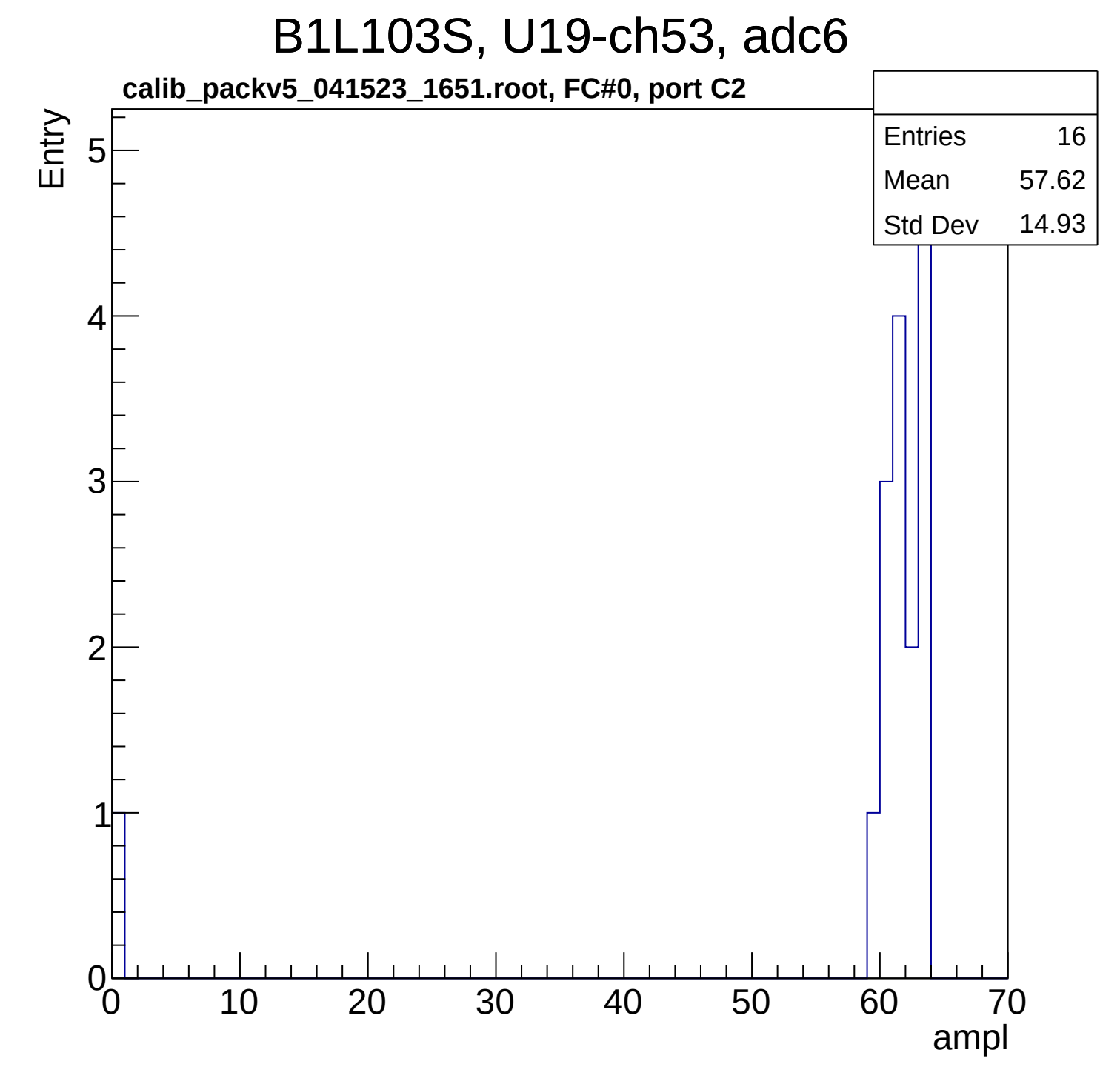
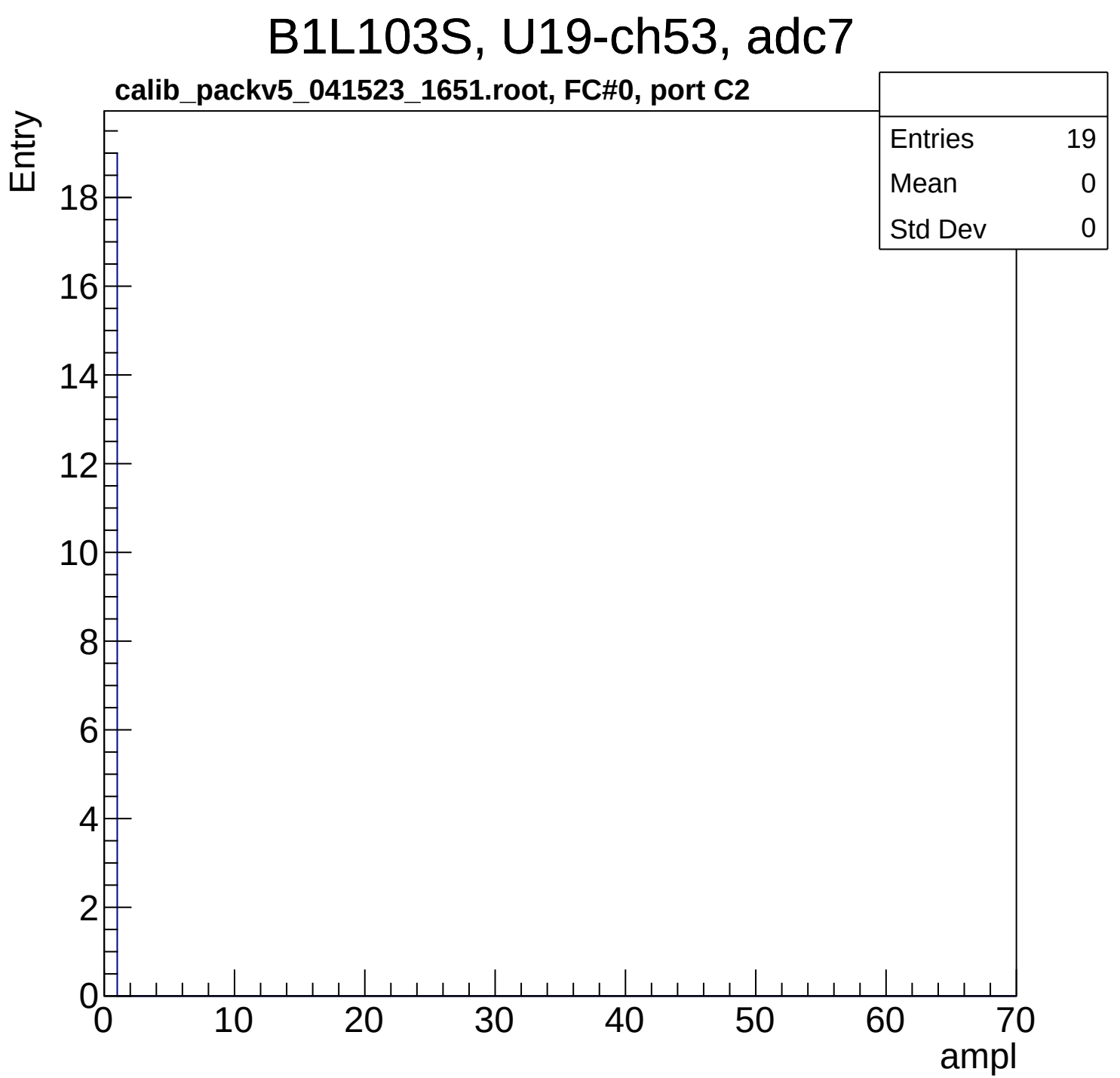
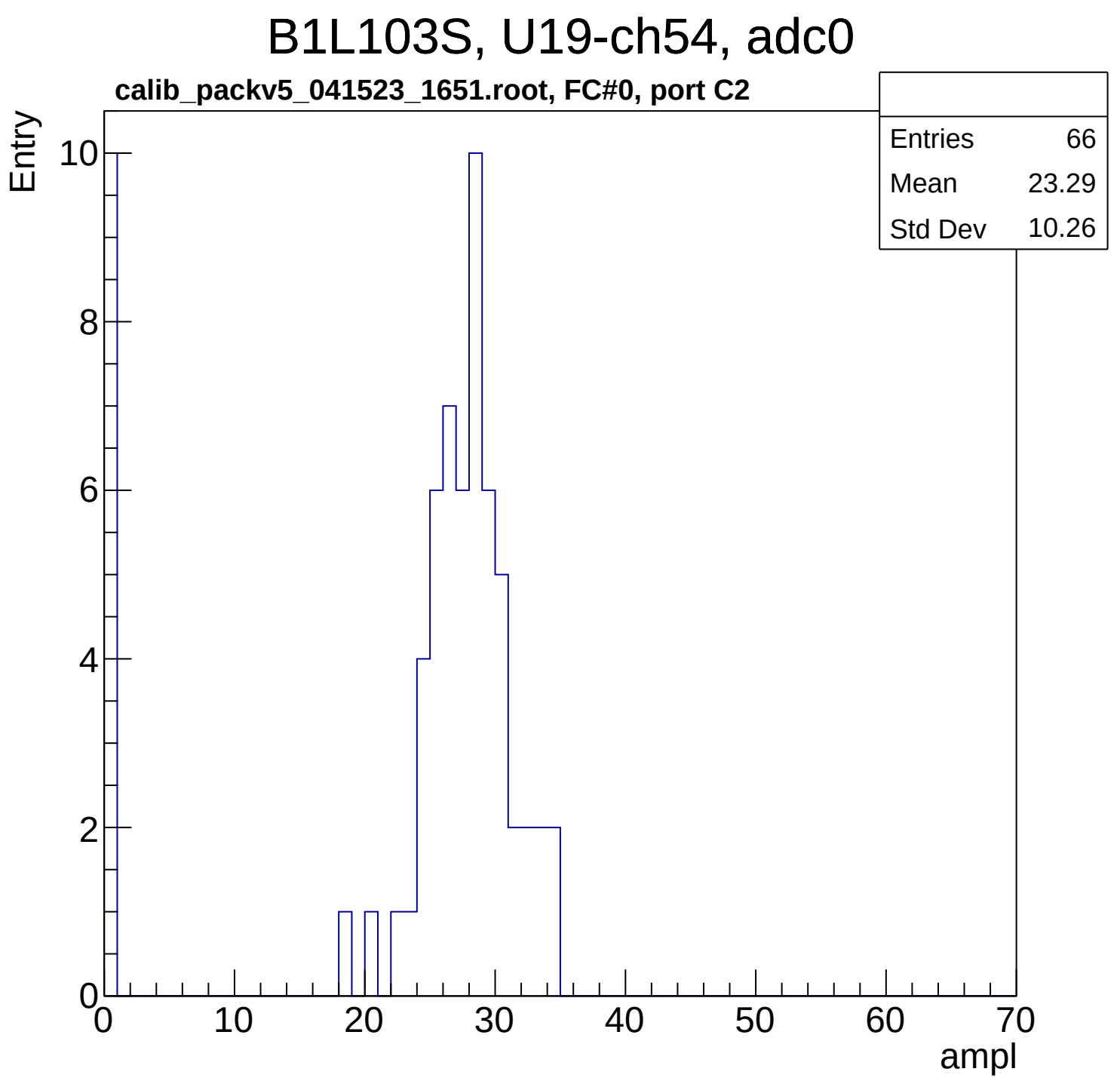
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch53, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 57.62
Std Dev 14.93
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch53, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch54, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 23.29
Std Dev 10.26
Entry
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6
8
10
0
10
20
30
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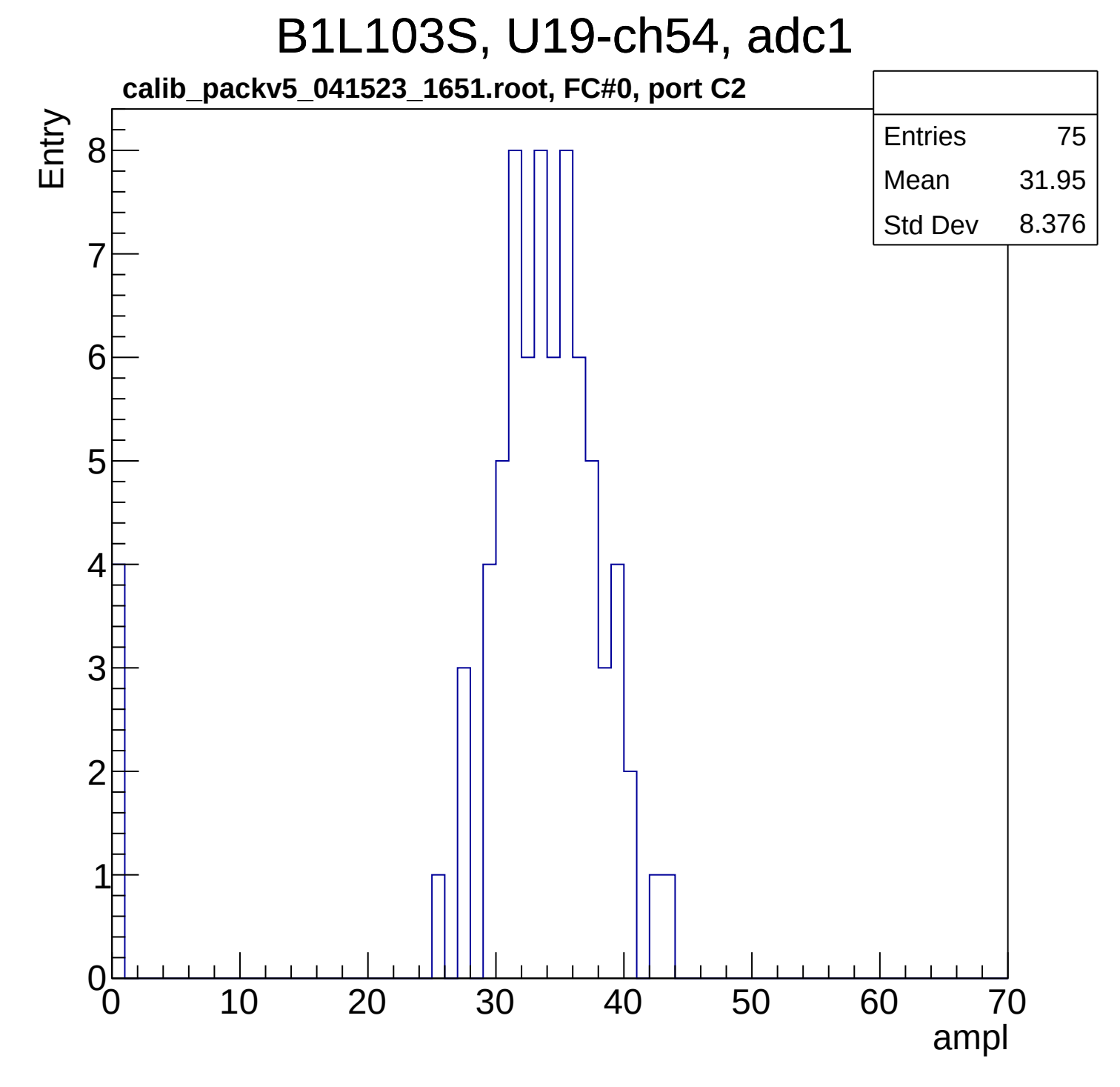
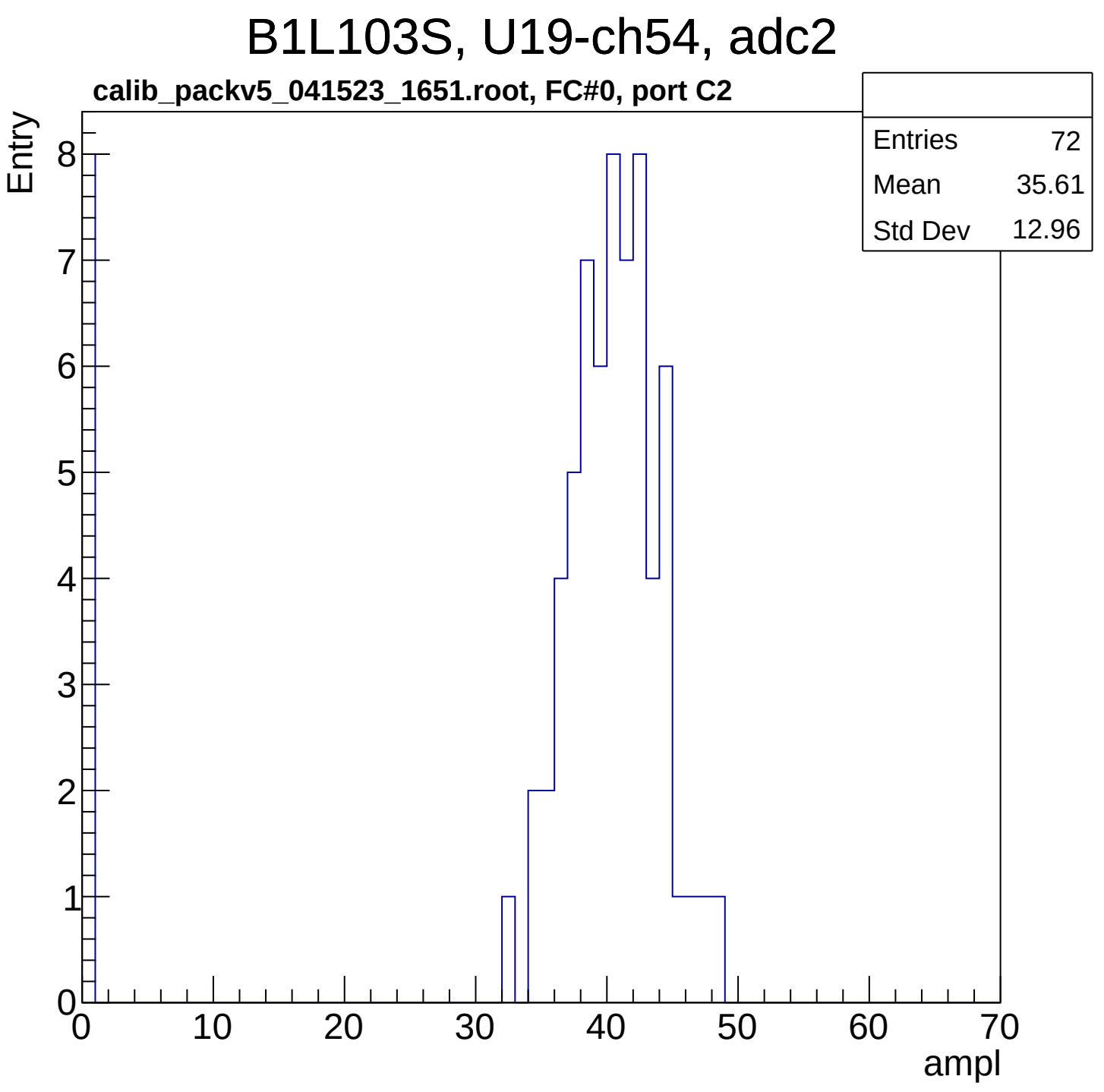
50
60
70
ampl


B1L103S, U19-ch54, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 31.95
Std Dev 8.376
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch54, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 35.61
Std Dev 12.96
Entry
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2
3
4
5
6
7
8
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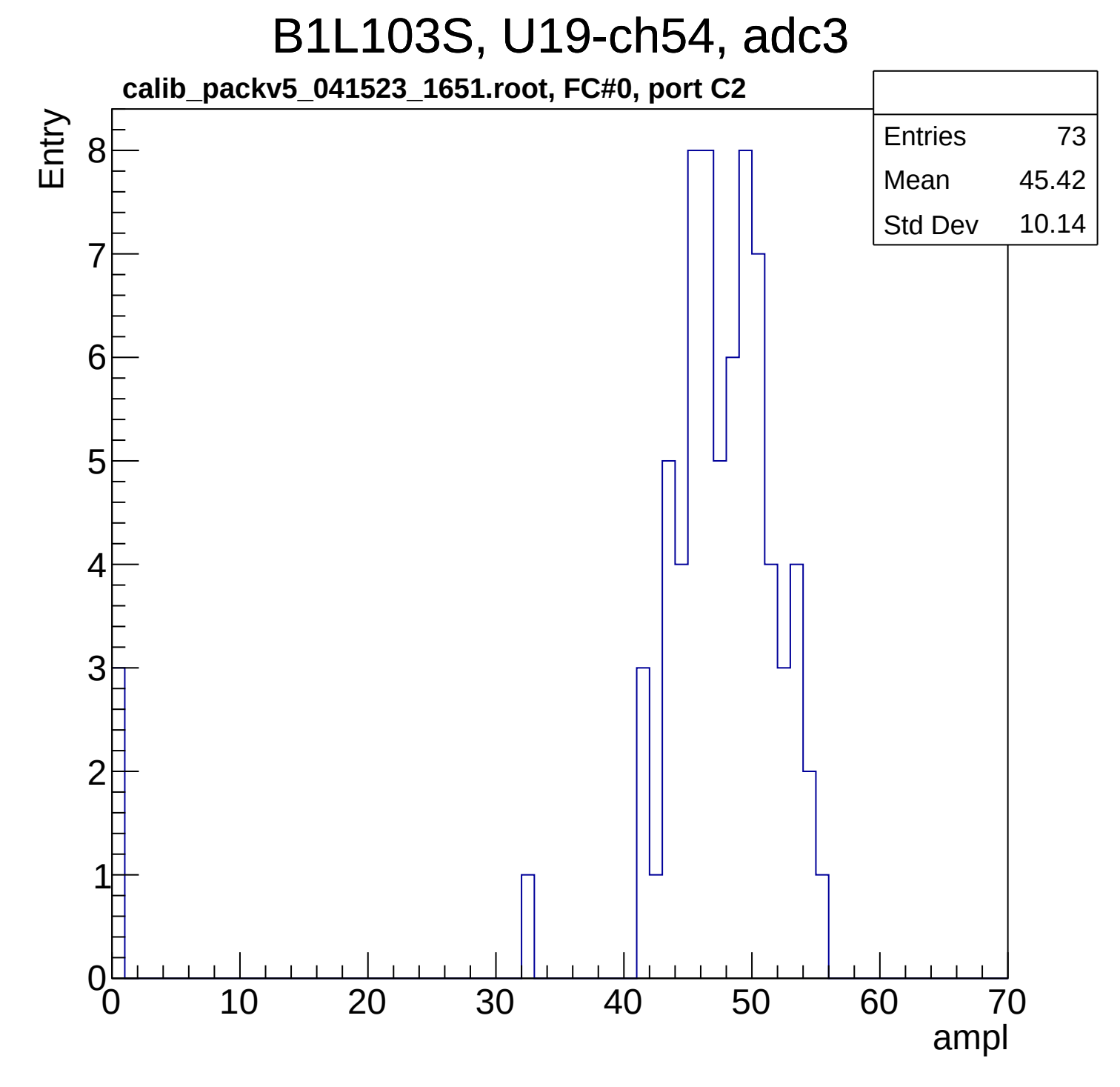
ampl


B1L103S, U19-ch54, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 45.42
Std Dev 10.14
Entry
ampl
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1
2
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4
5
6
7
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0
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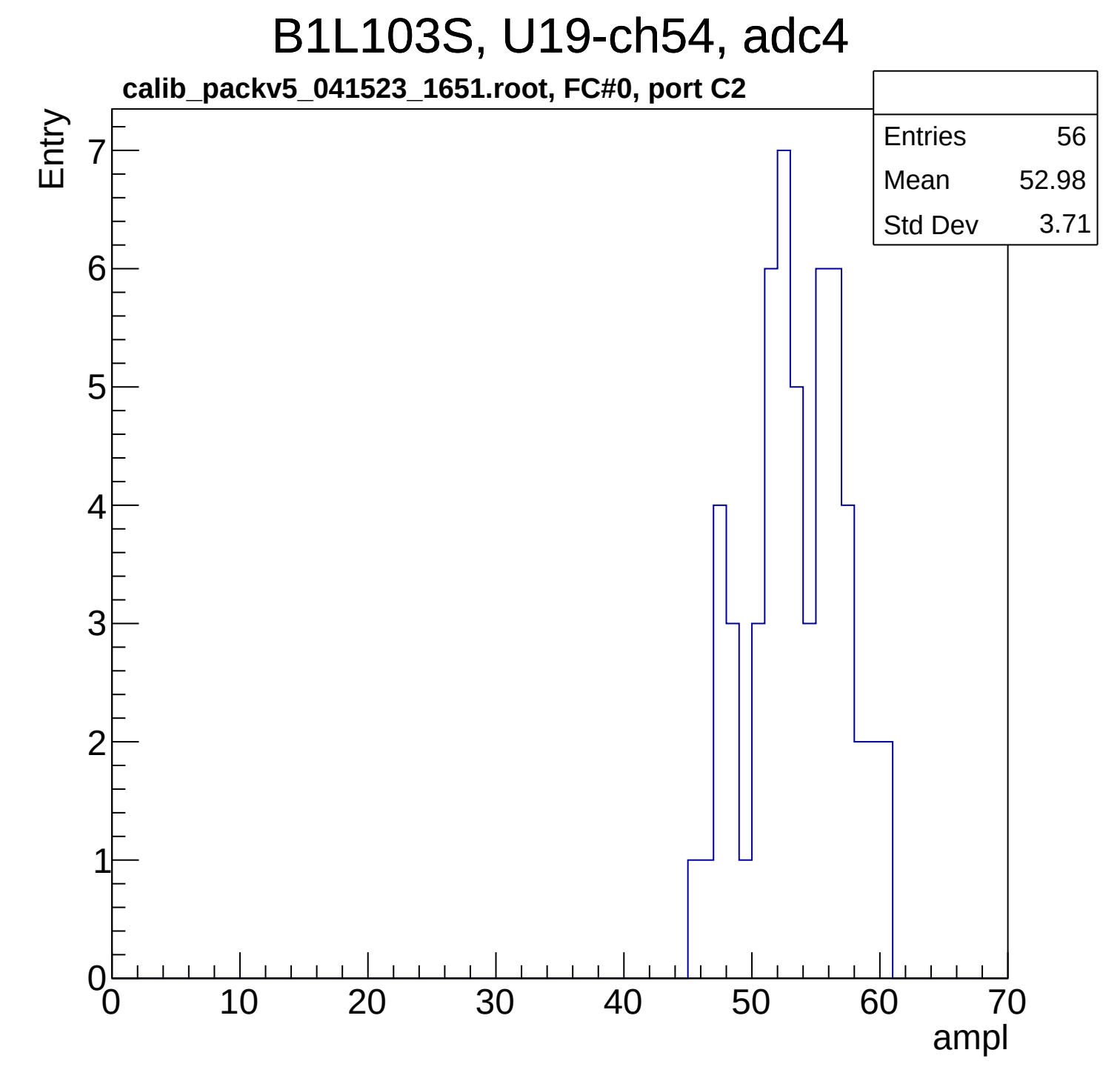
B1L103S, U19-ch54, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 52.98
Std Dev 3.71
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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40
50
60
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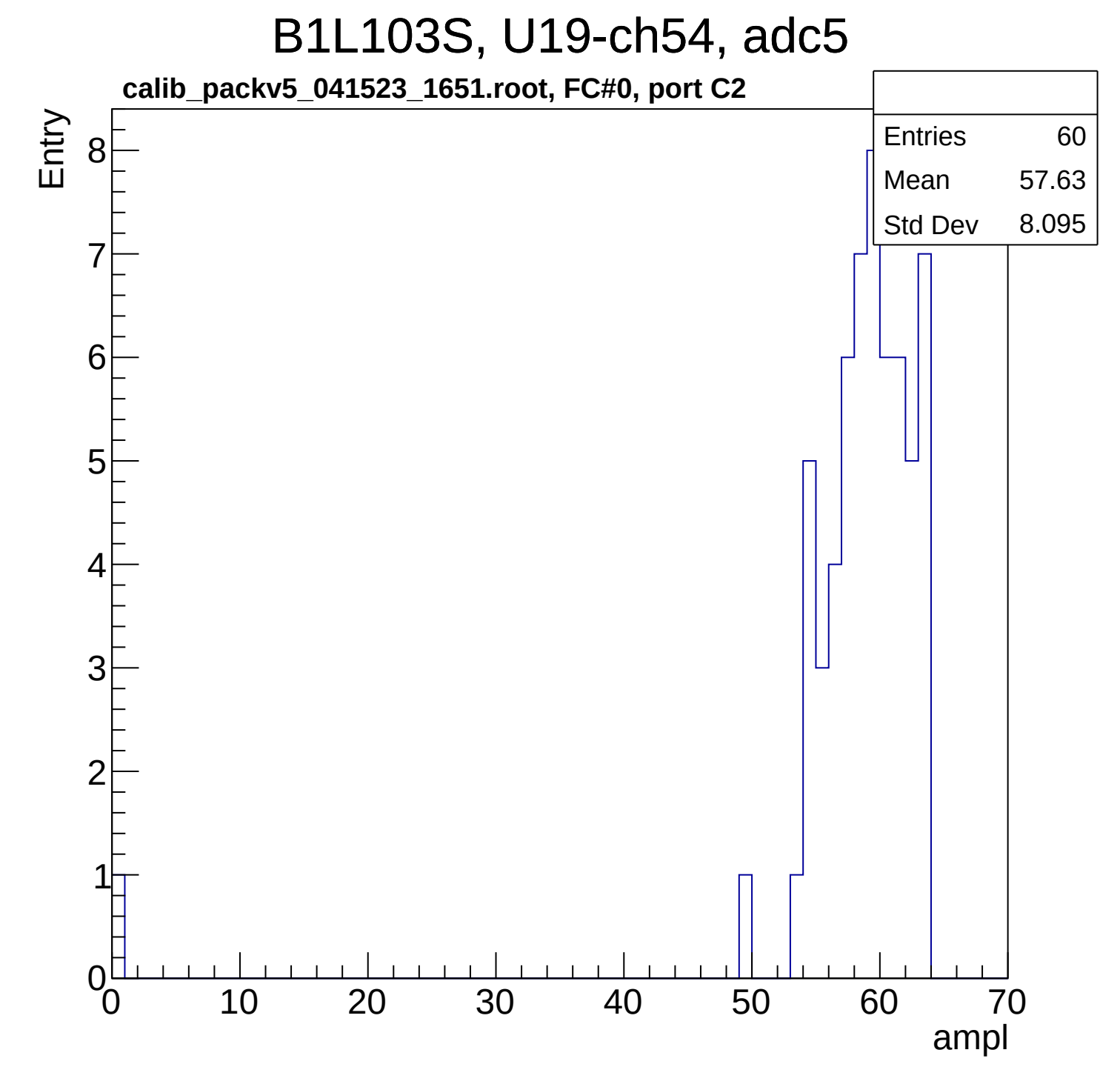
B1L103S, U19-ch54, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 57.63
Std Dev 8.095
Entry
ampl
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1
2
3
4
5
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7
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0
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40
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60
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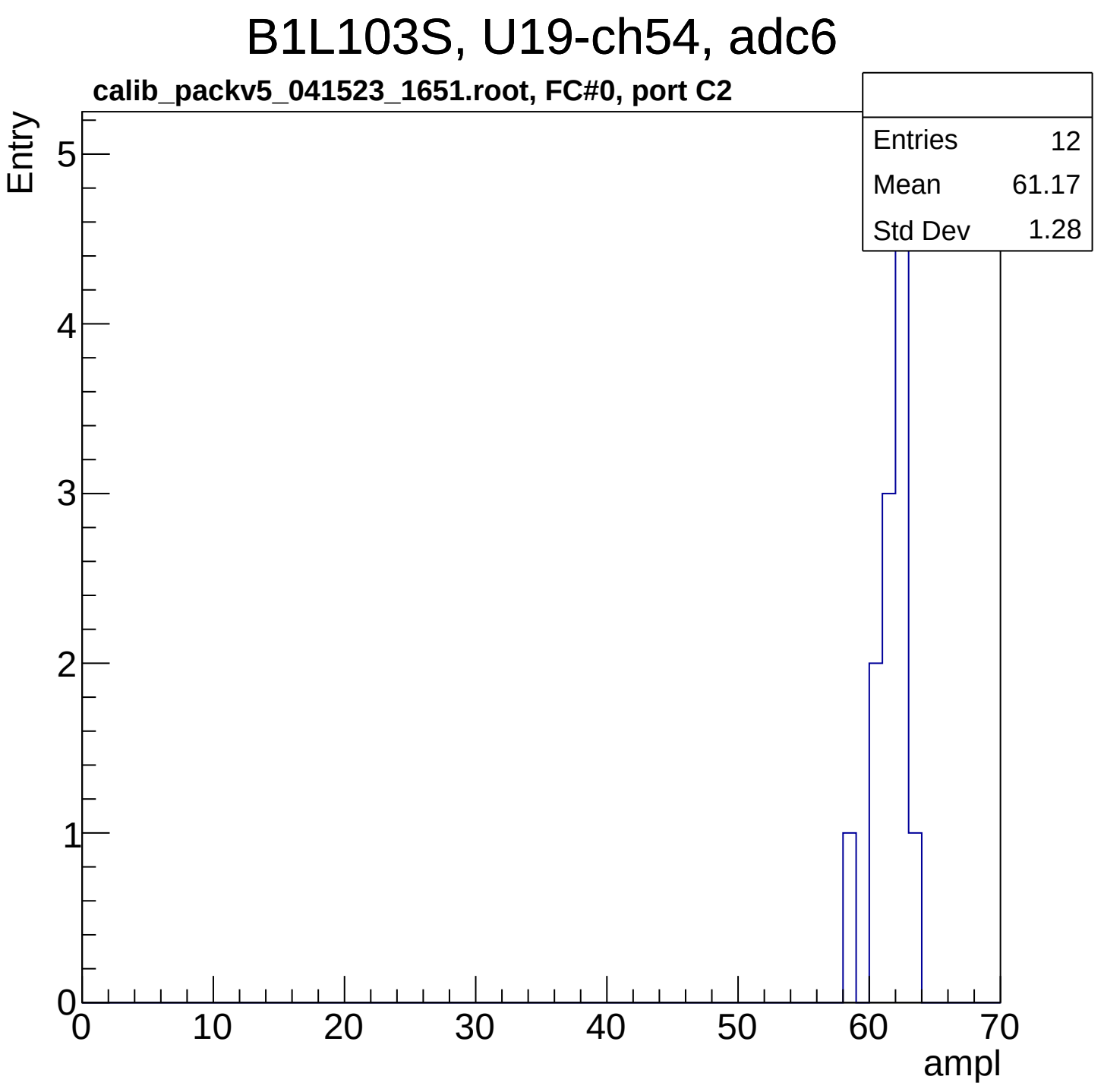
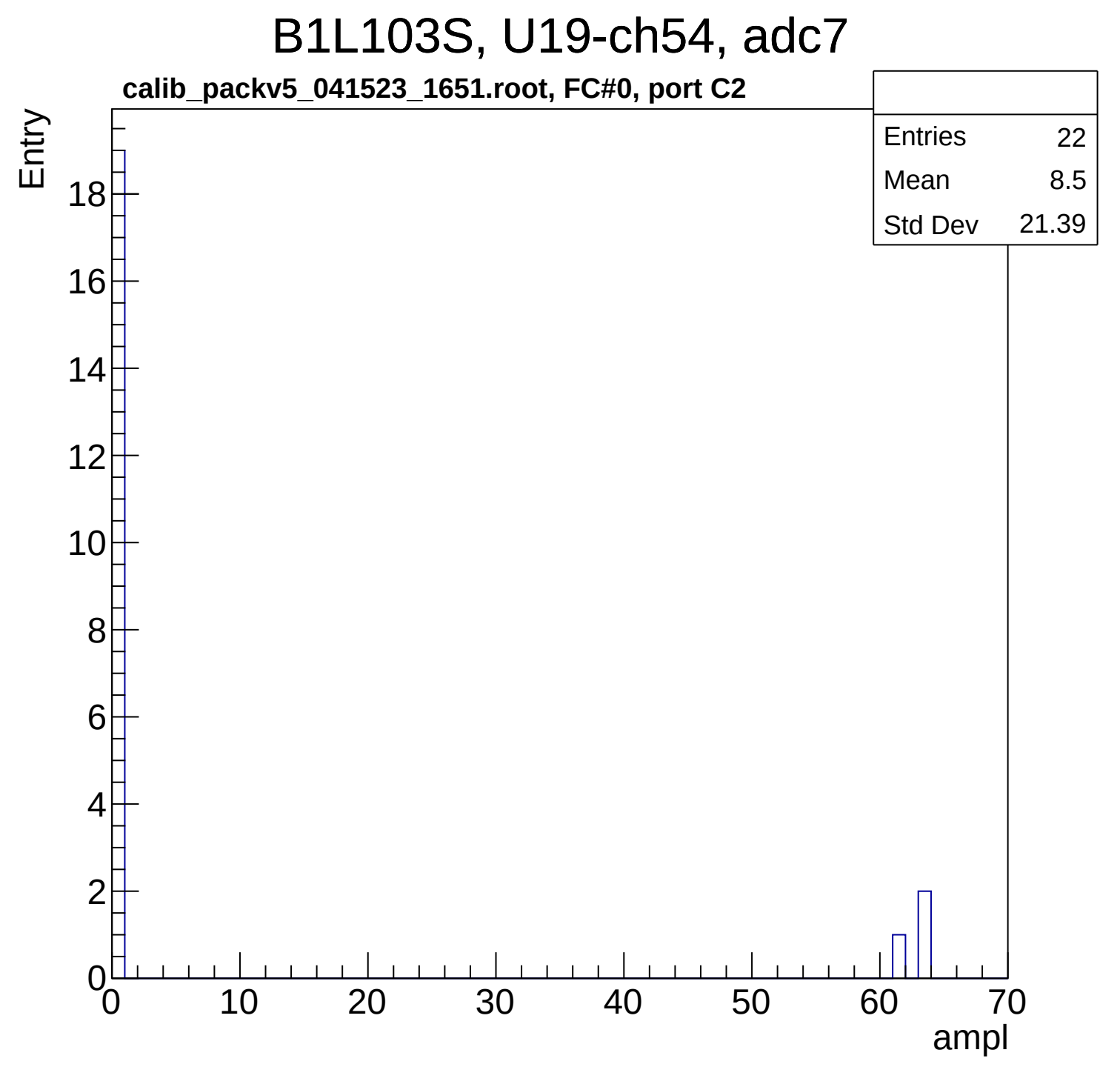

B1L103S, U19-ch54, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.17
Std Dev 1.28
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch54, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.5
Std Dev 21.39
Entry
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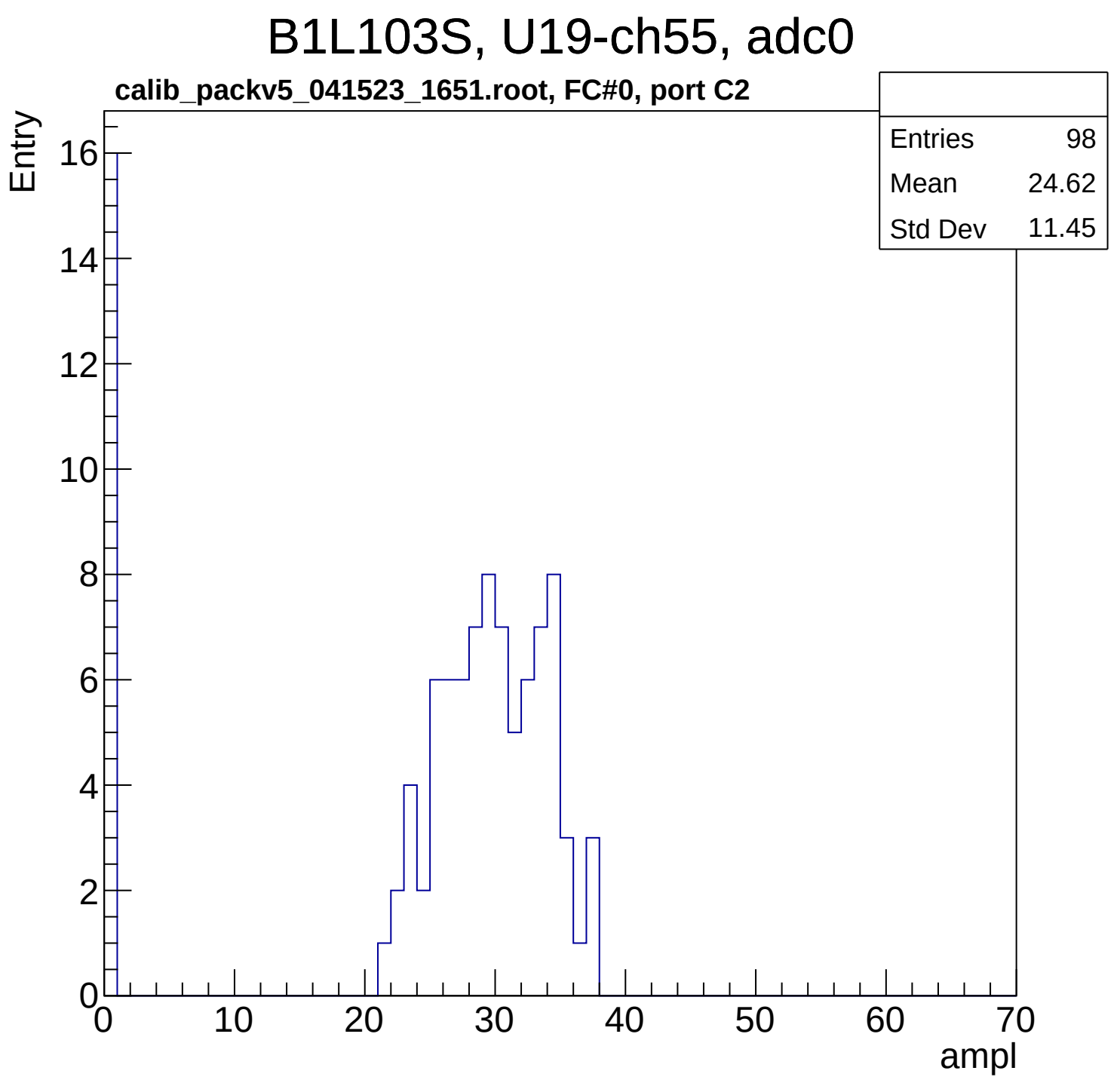
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch55, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 98
Mean 24.62
Std Dev 11.45
Entry
ampl
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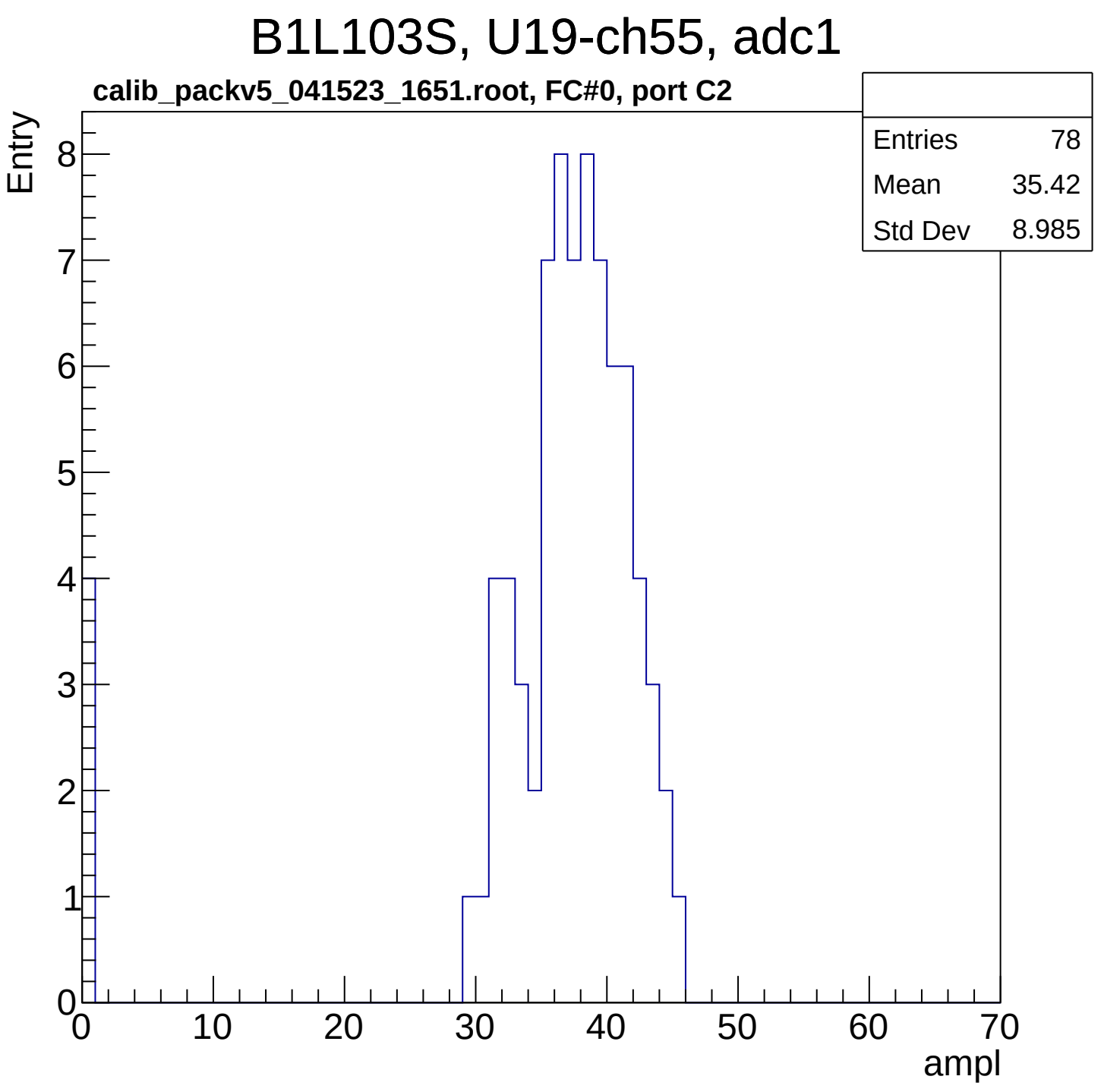
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L103S, U19-ch55, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 35.42
Std Dev 8.985
Entry
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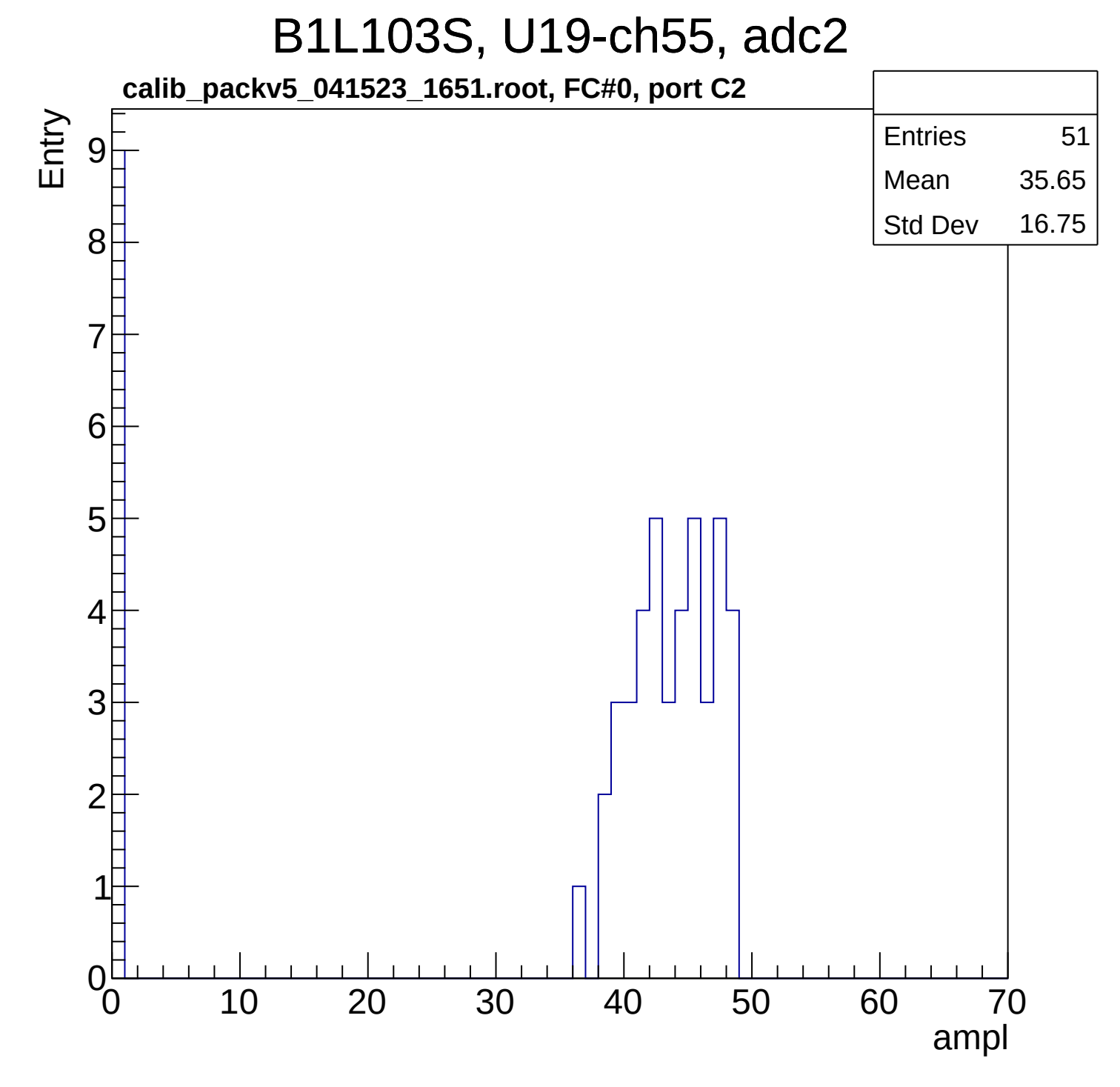
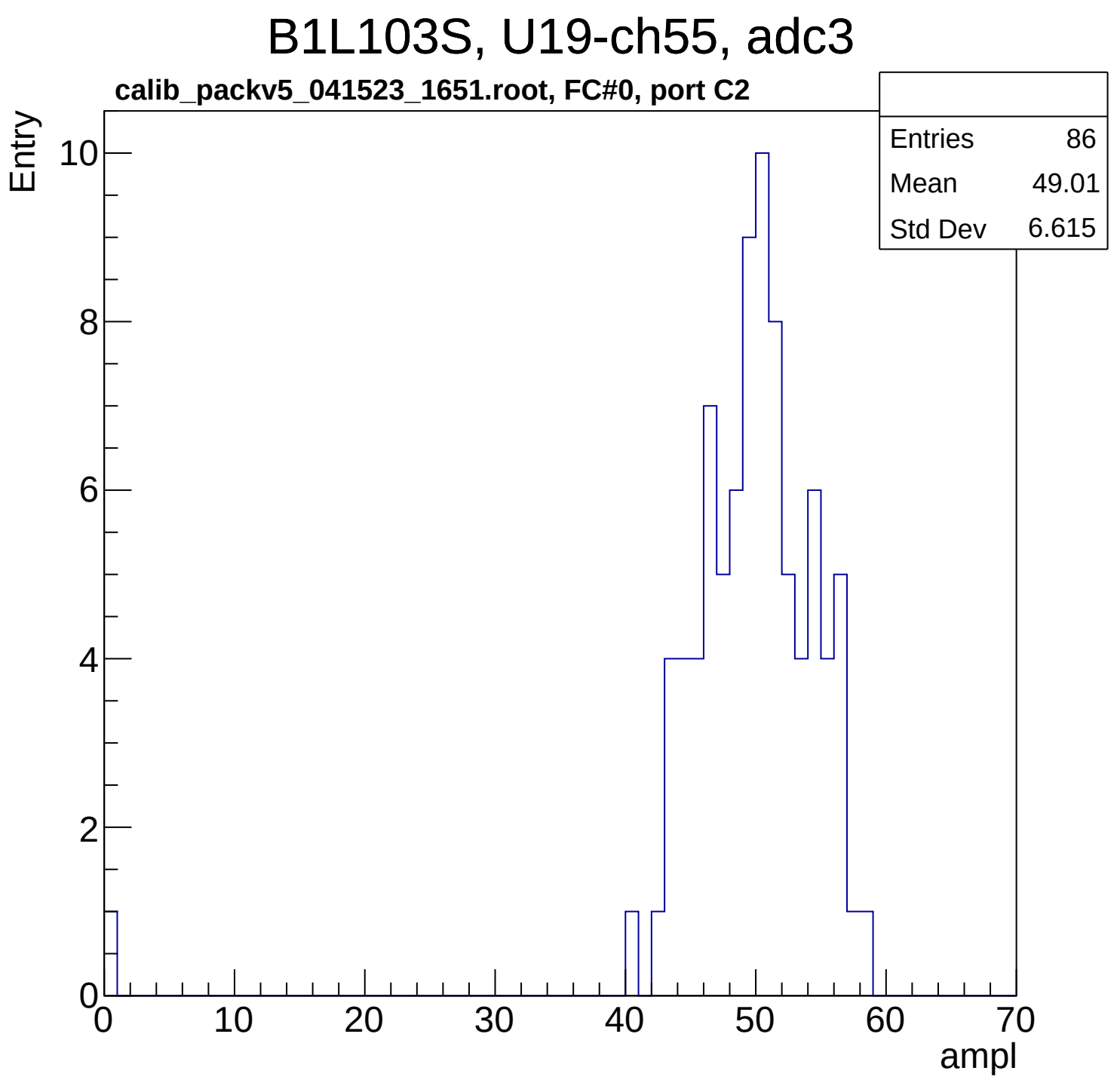
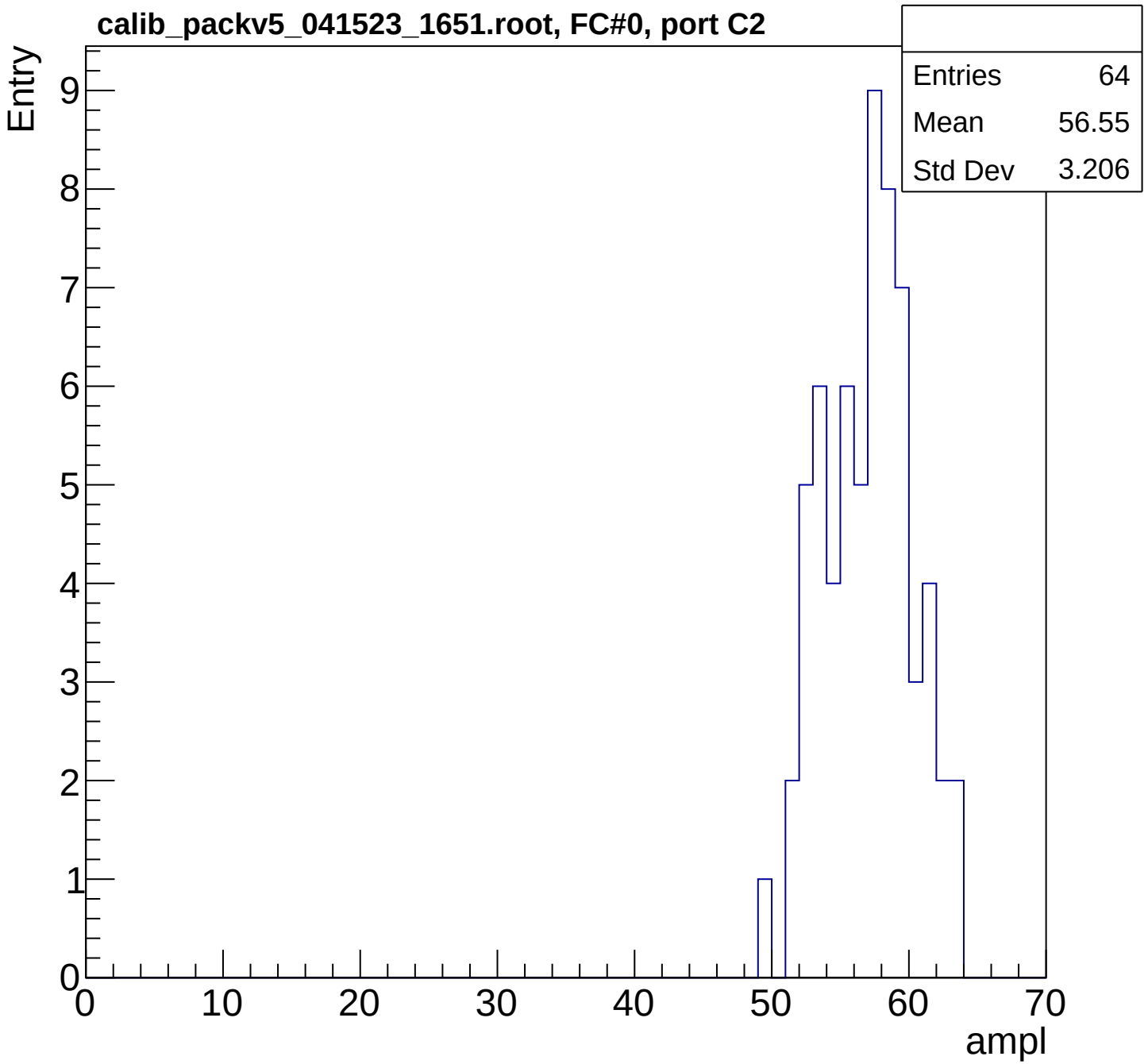
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch55, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 35.65
Std Dev 16.75
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch55, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 49.01
Std Dev 6.615
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch55, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 56.55
Std Dev 3.206
Entry
ampl
0
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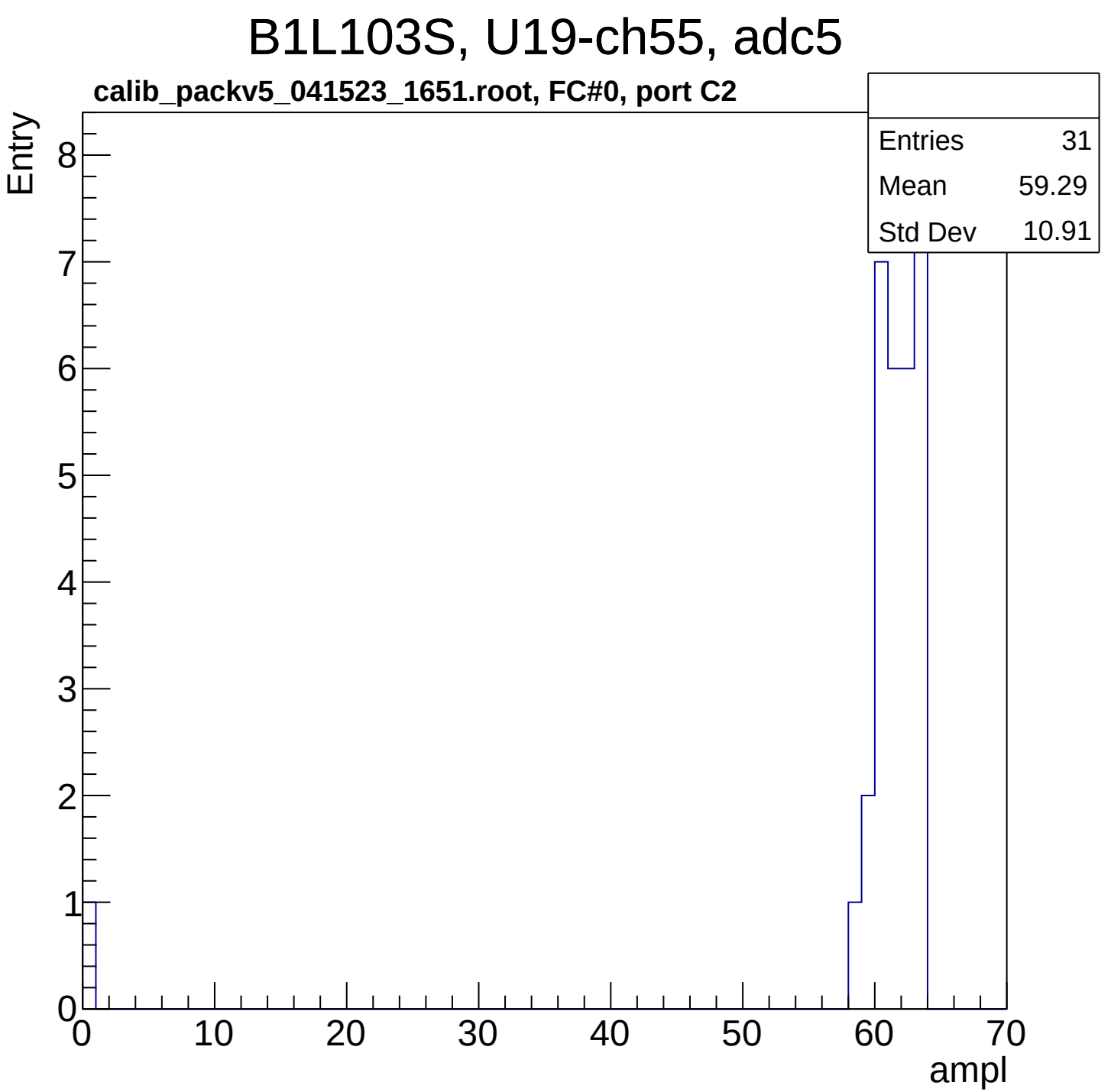
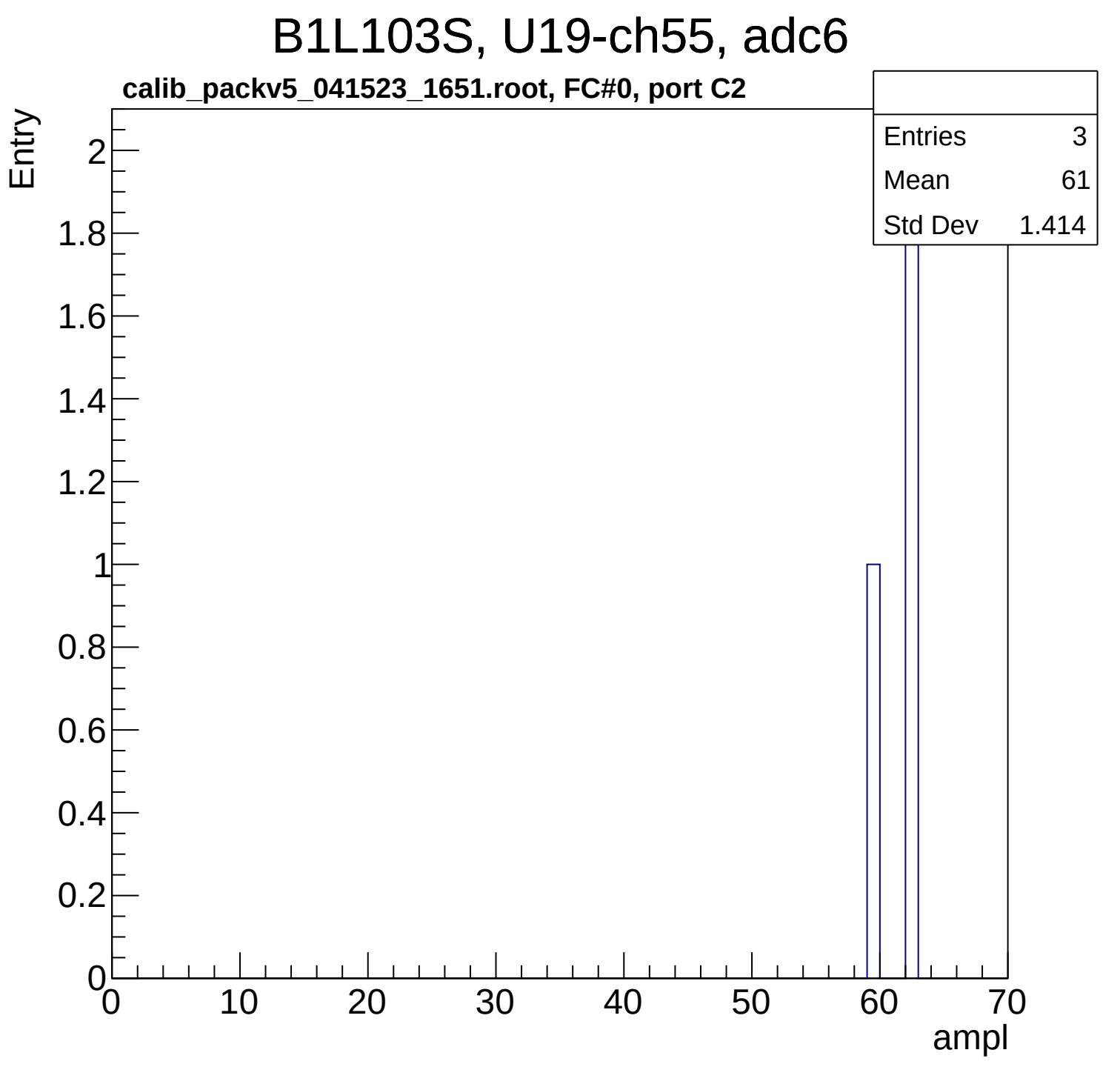
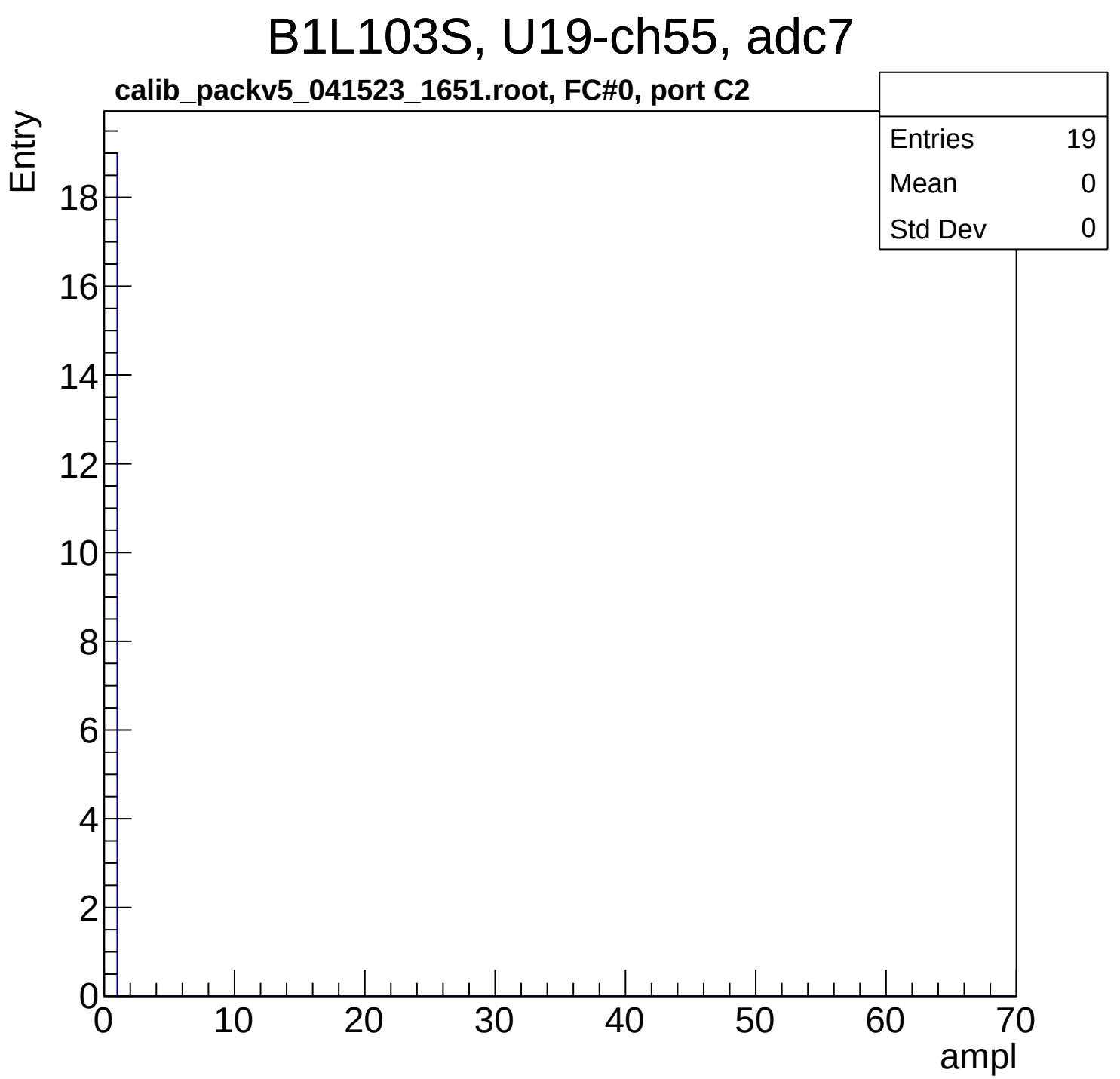
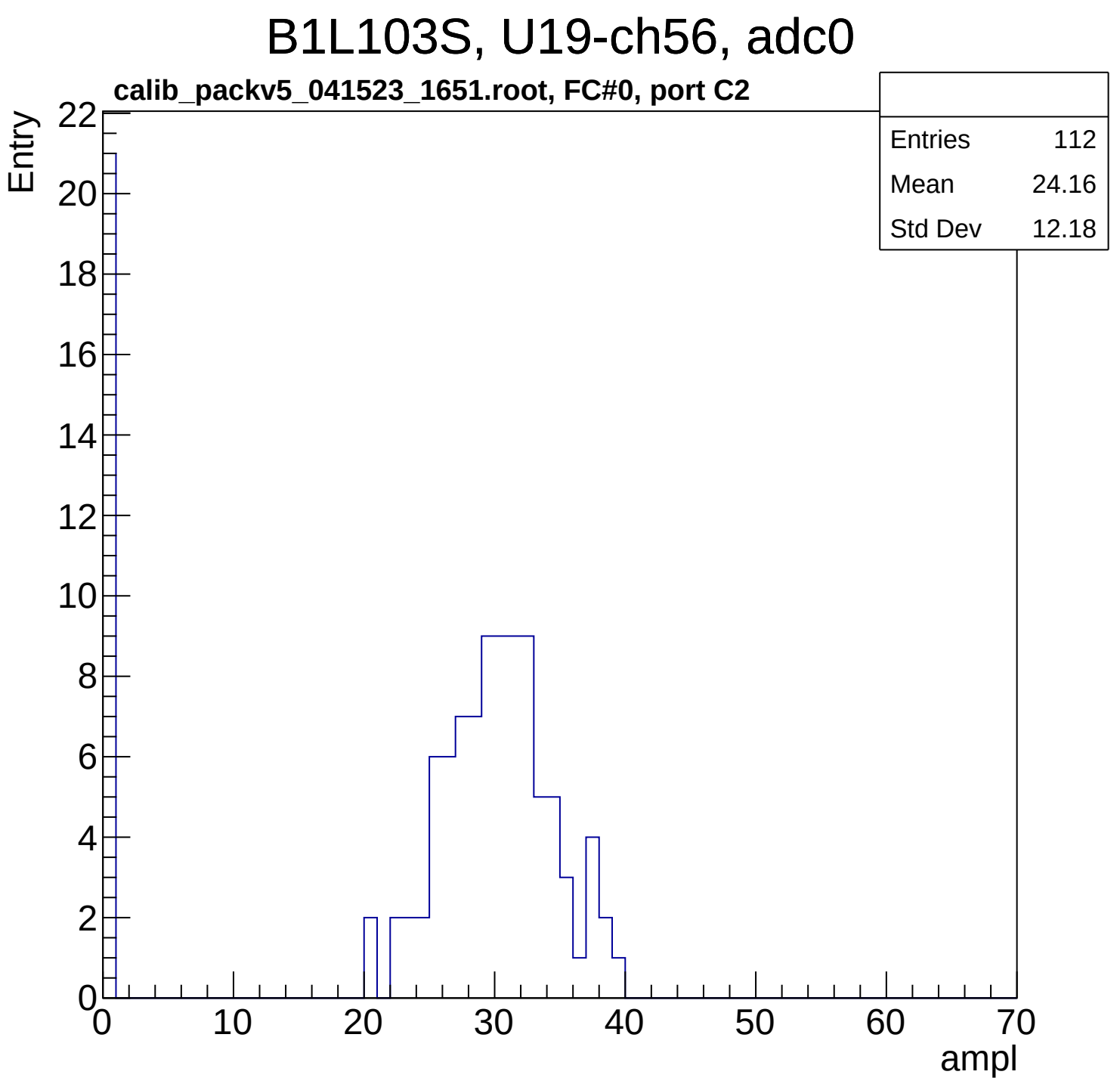
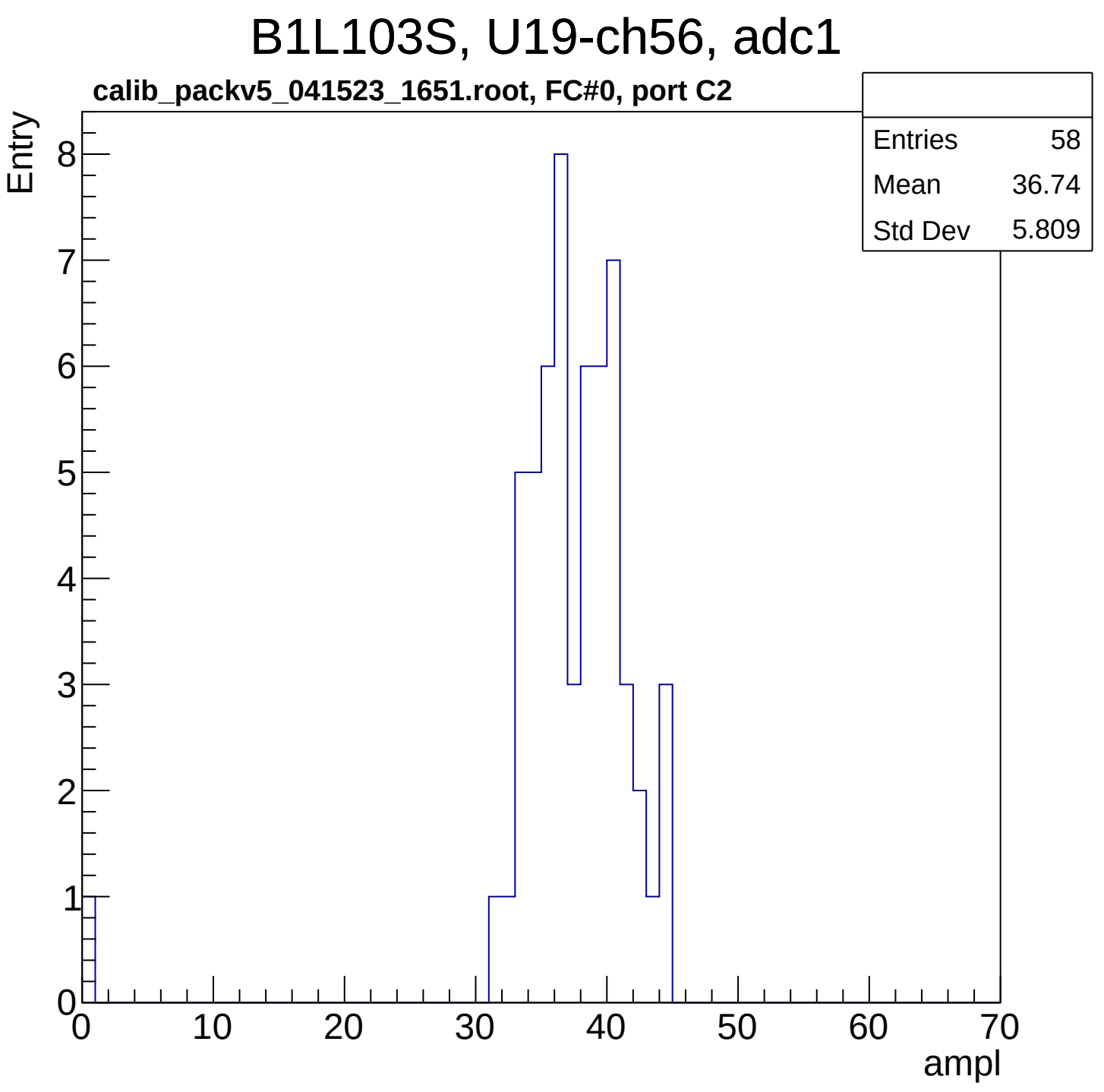
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

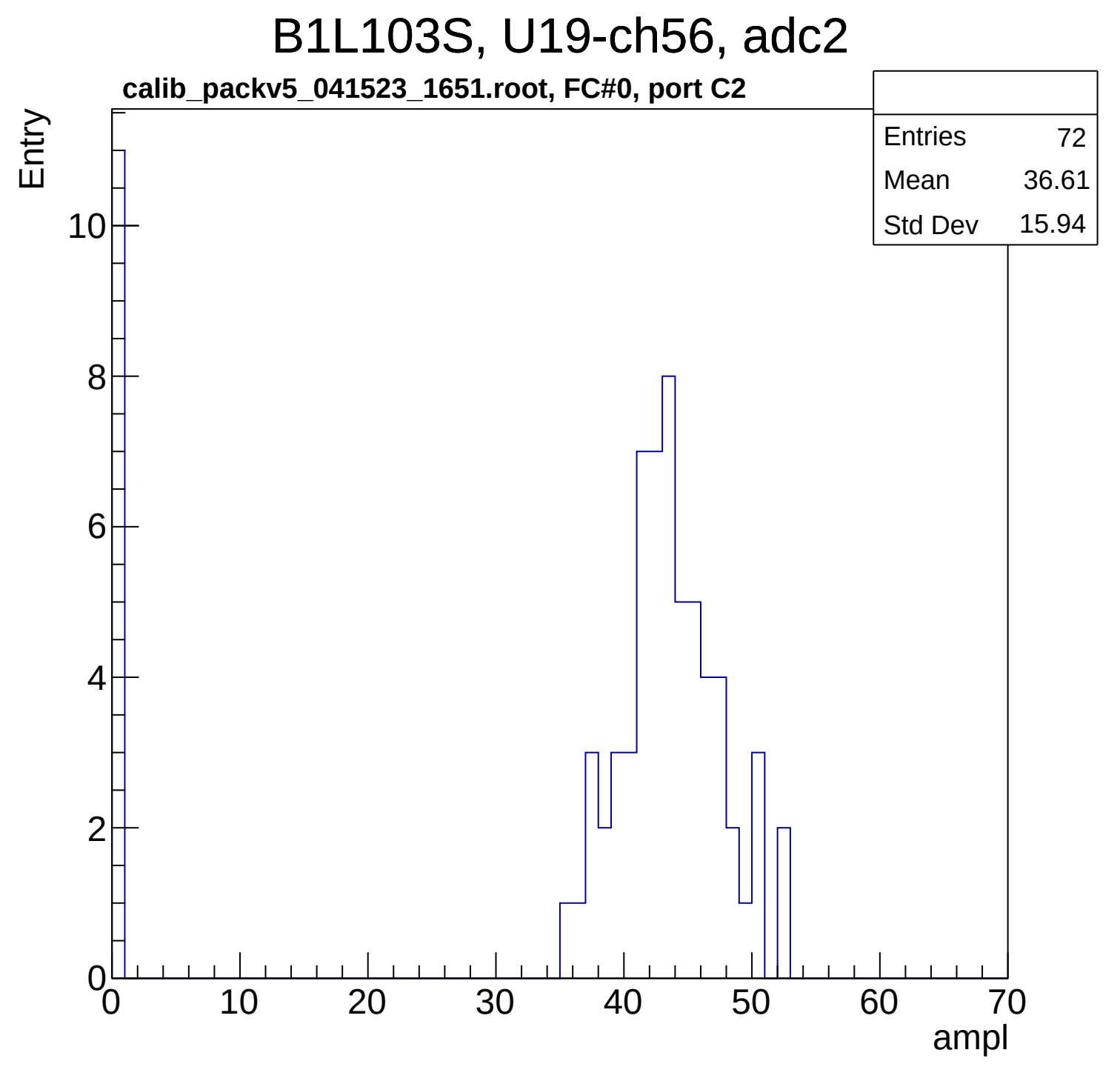

B1L103S, U19-ch55, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 59.29
Std Dev 10.91
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

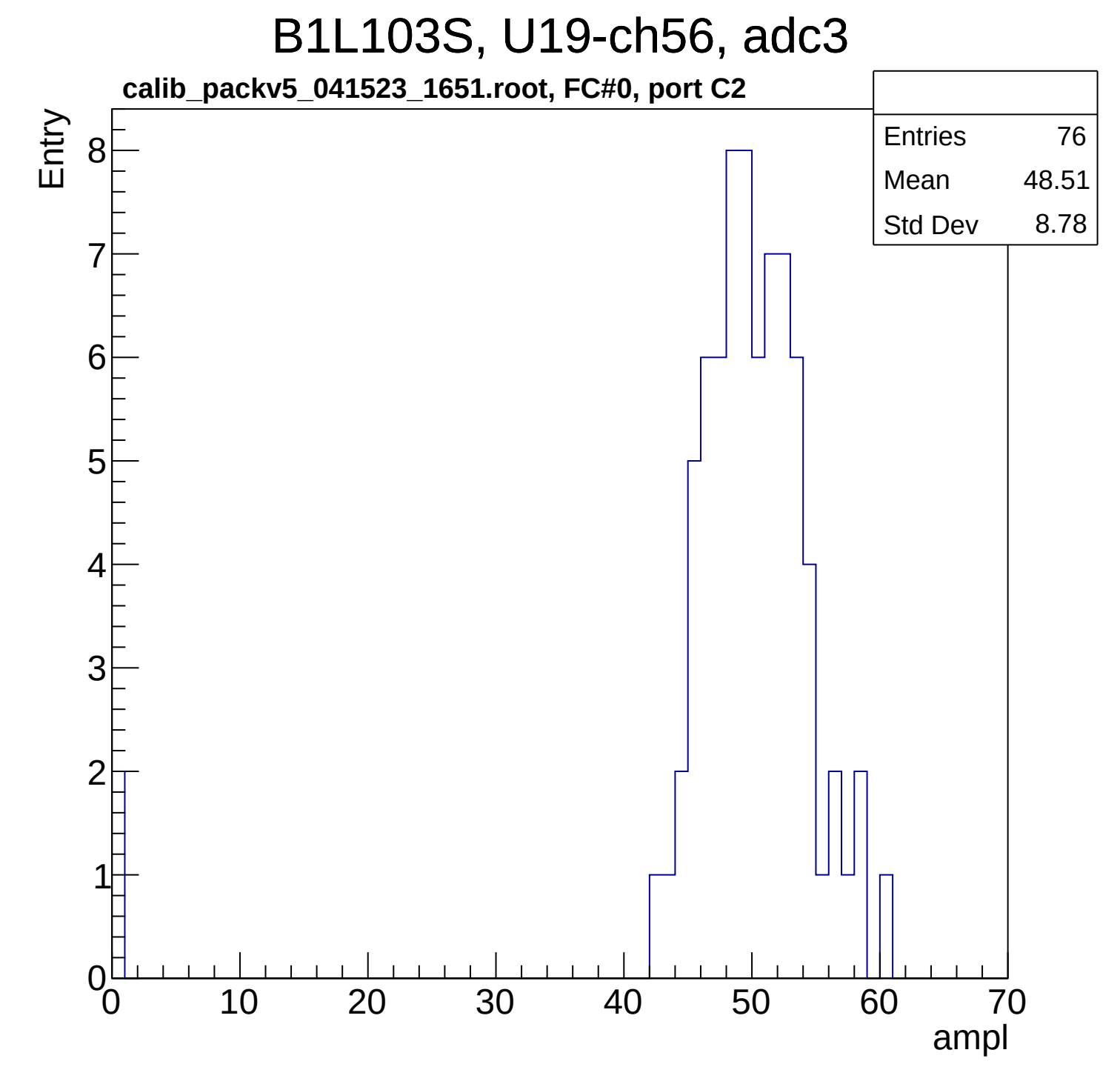

B1L103S, U19-ch55, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 61
Std Dev 1.414
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U19-ch55, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch56, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 112
Mean 24.16
Std Dev 12.18
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70


B1L103S, U19-ch56, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 36.74
Std Dev 5.809
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch56, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 36.61
Std Dev 15.94
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch56, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 48.51
Std Dev 8.78
Entry
ampl
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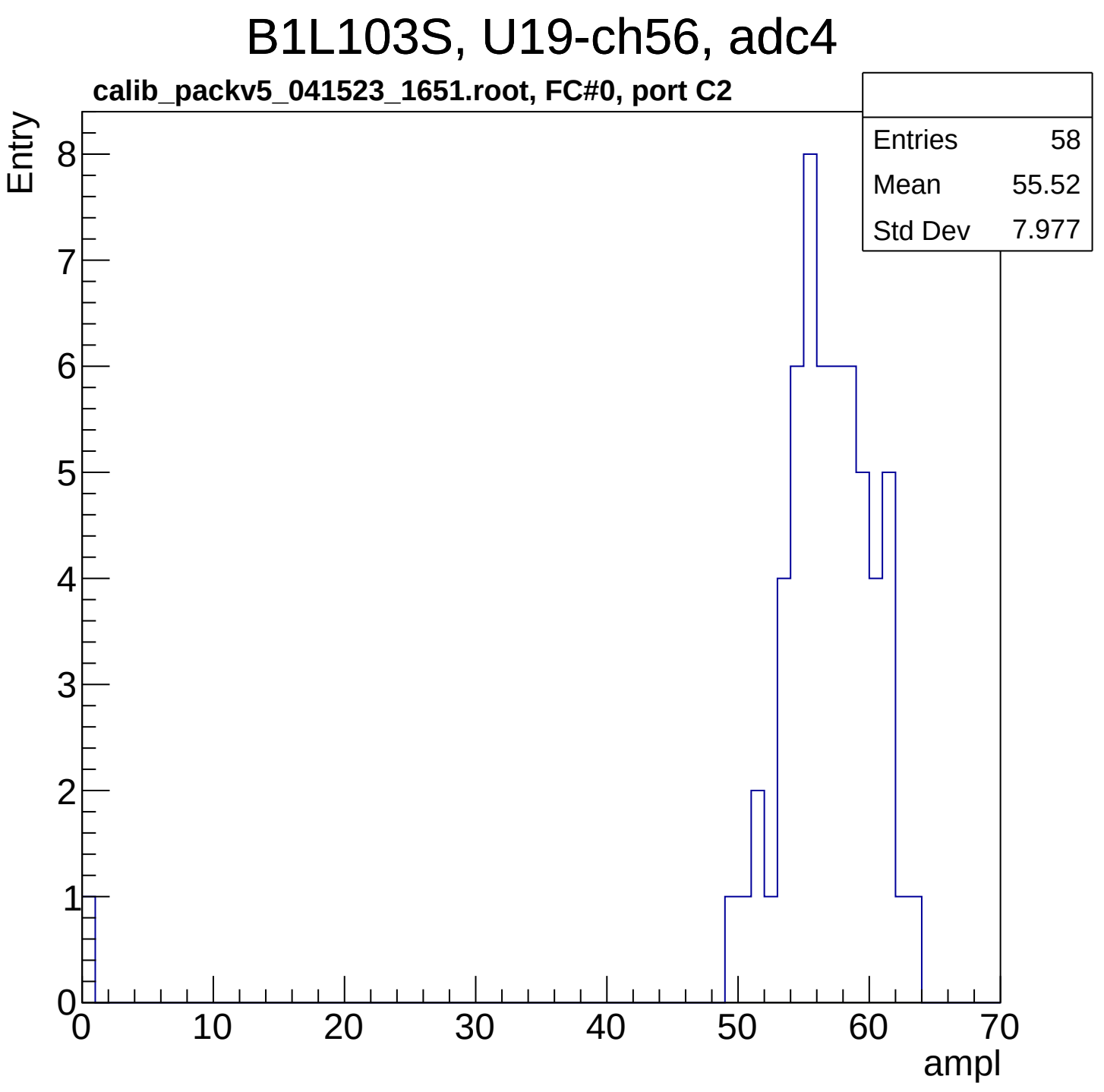
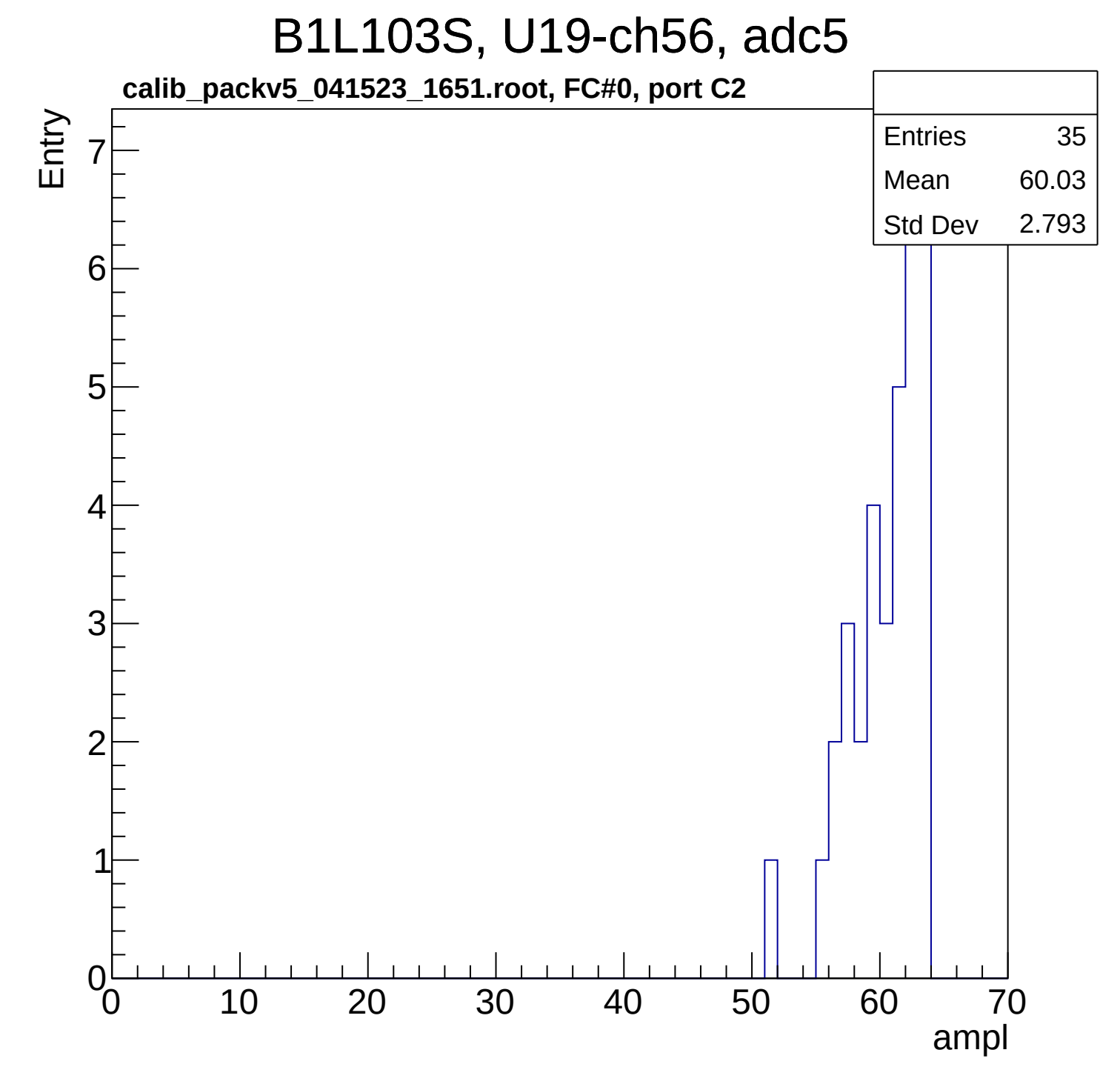
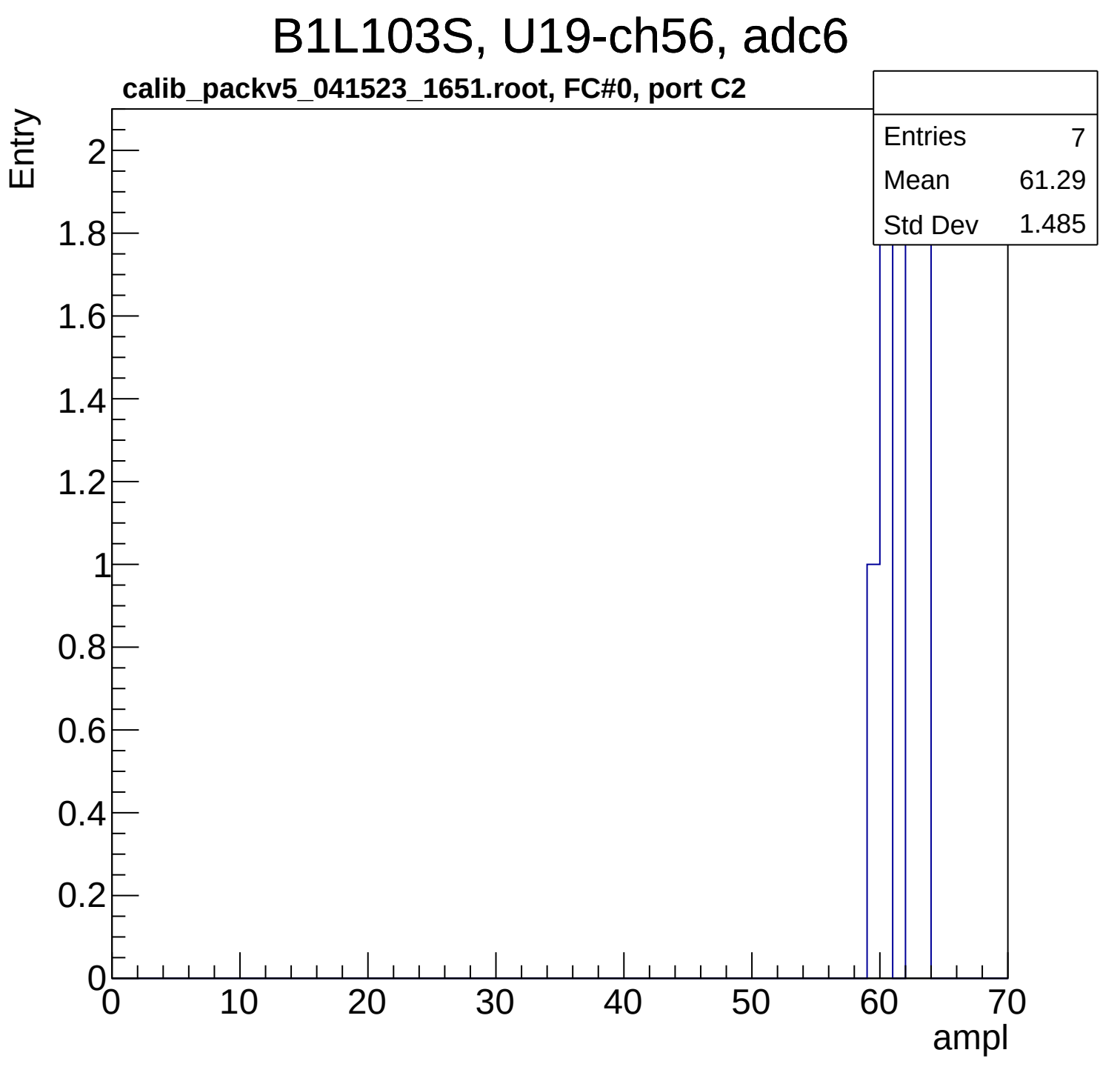
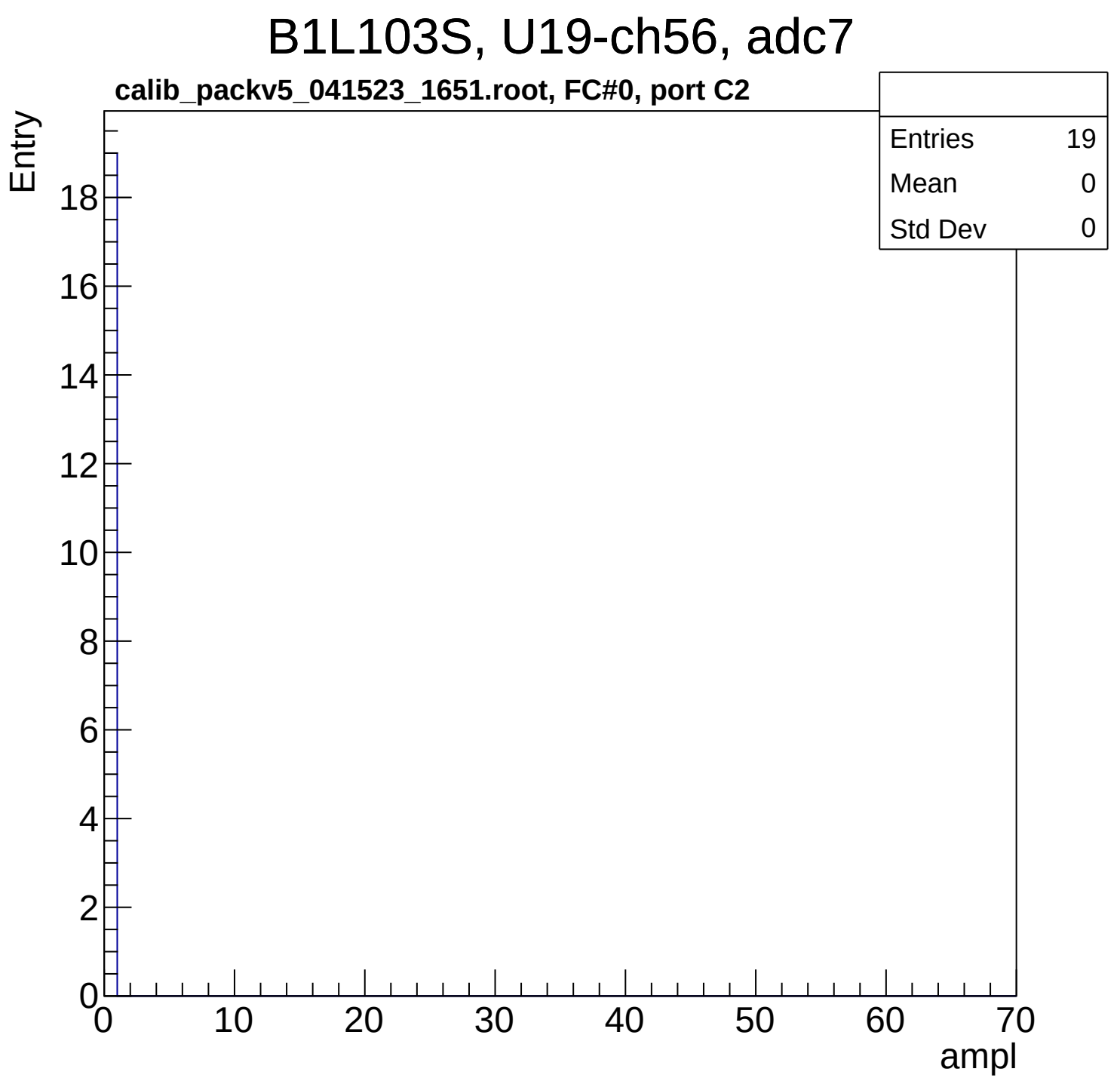
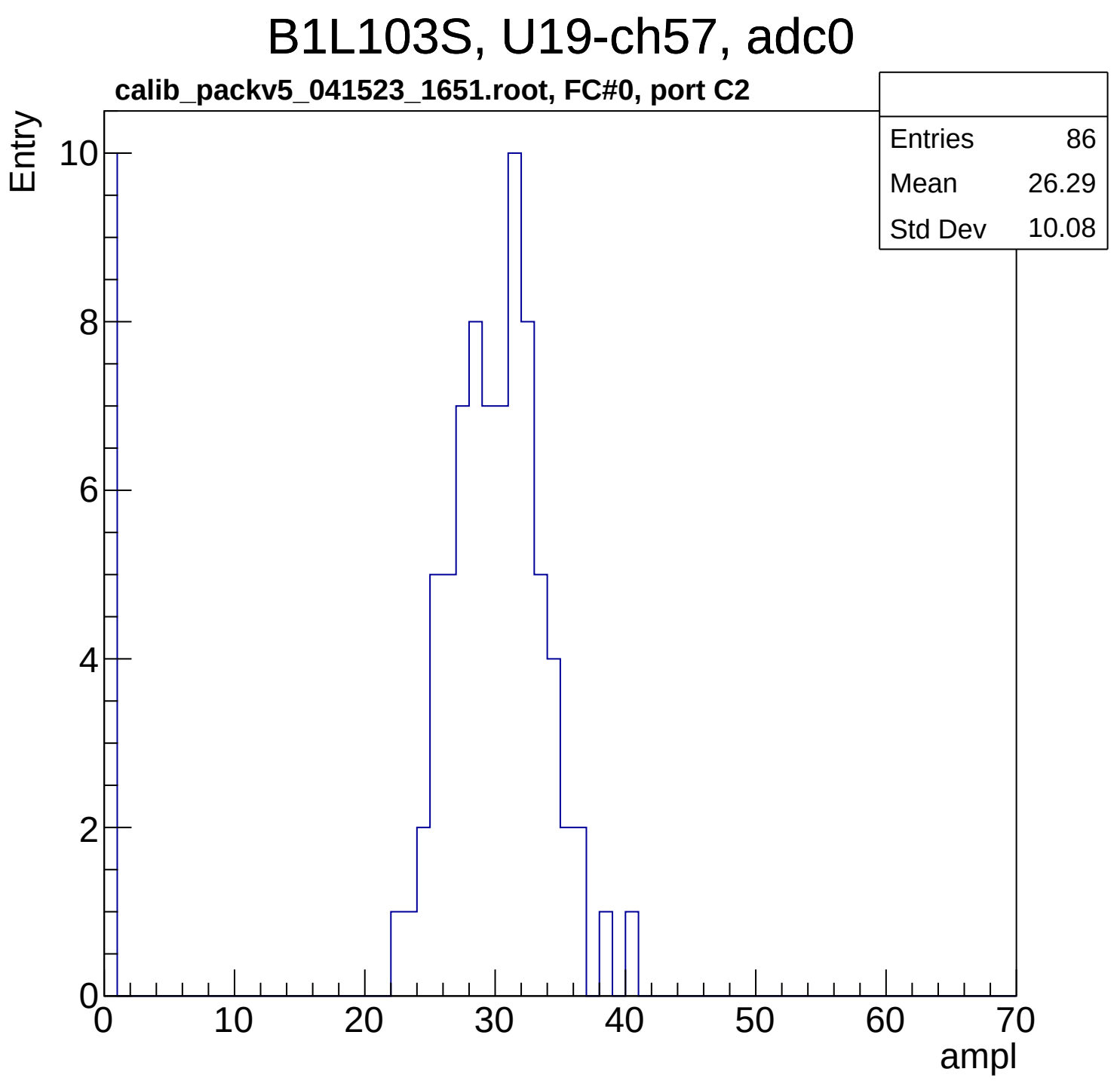
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

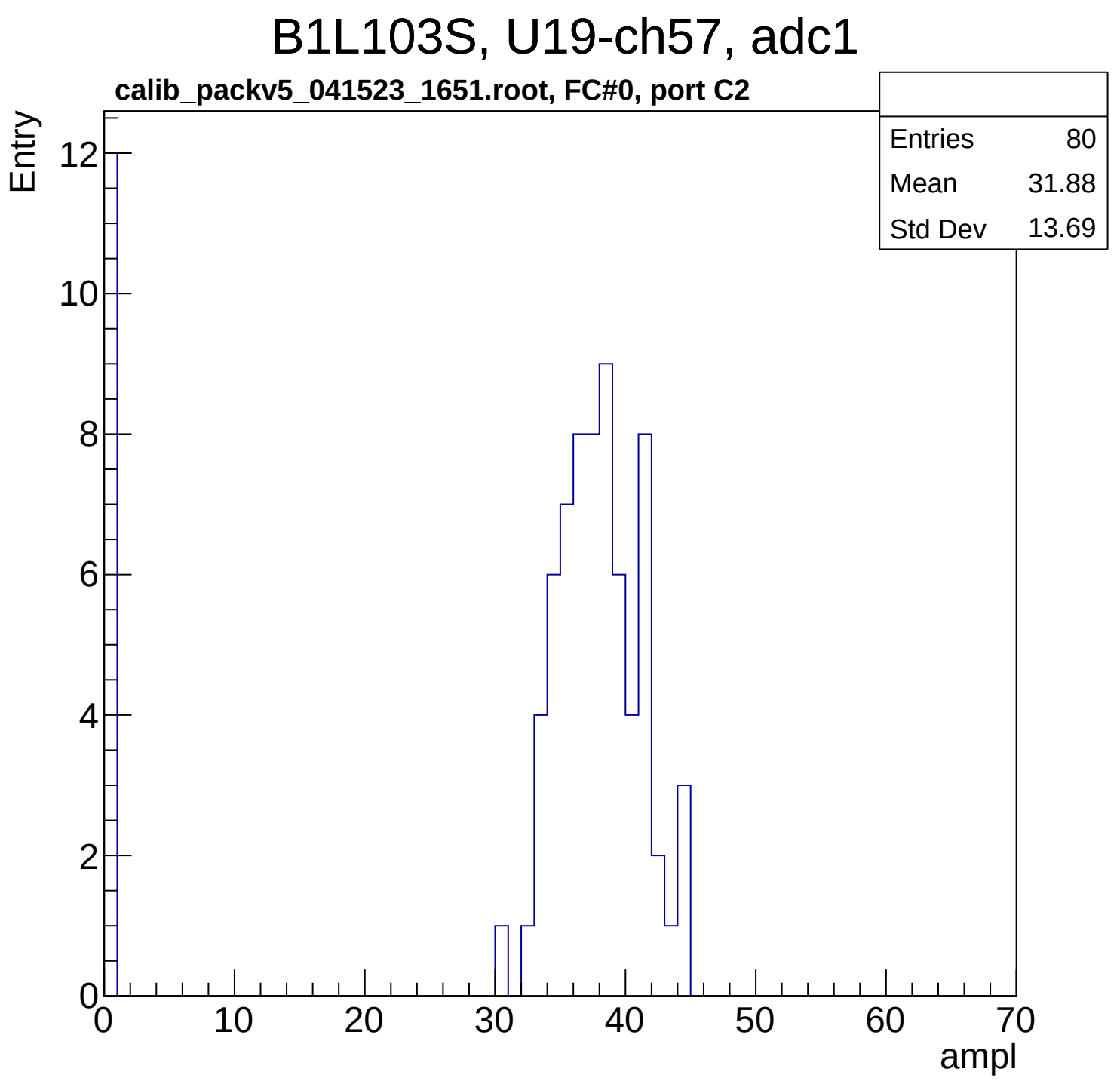

B1L103S, U19-ch56, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 55.52
Std Dev 7.977
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

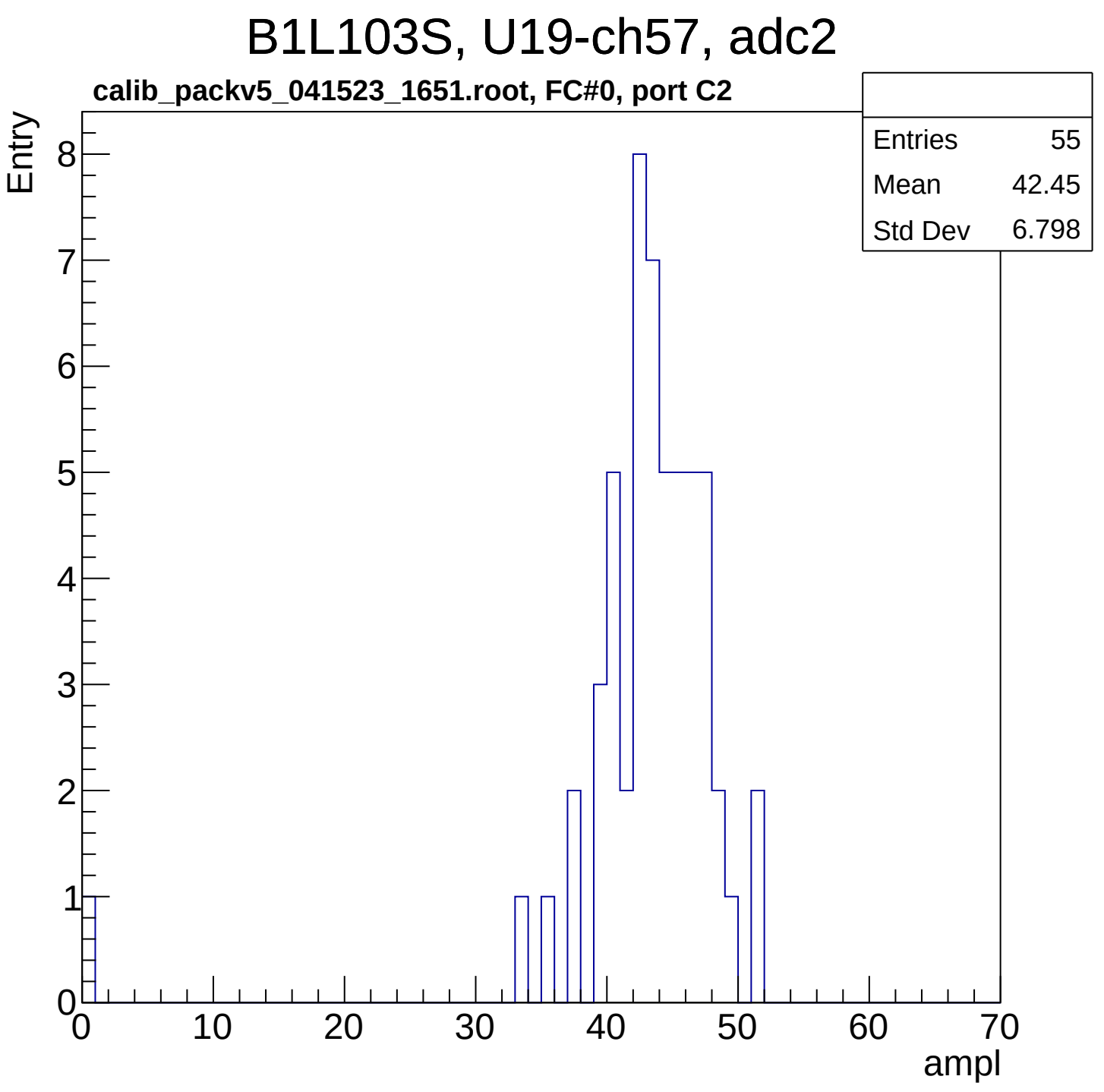

B1L103S, U19-ch56, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 60.03
Std Dev 2.793
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch56, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 61.29
Std Dev 1.485
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U19-ch56, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch57, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 26.29
Std Dev 10.08
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch57, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 31.88
Std Dev 13.69
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch57, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 42.45
Std Dev 6.798
Entry
ampl
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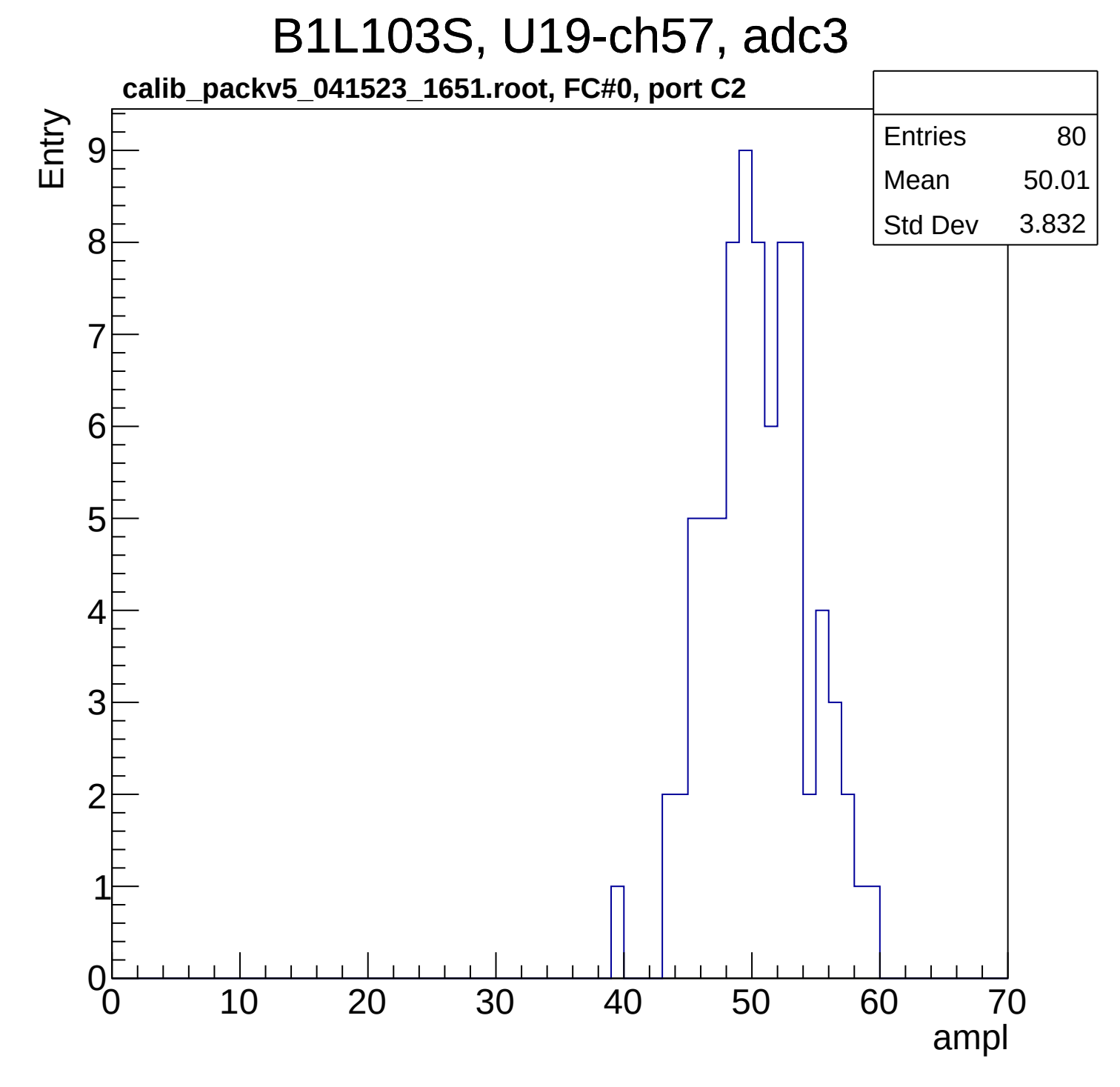
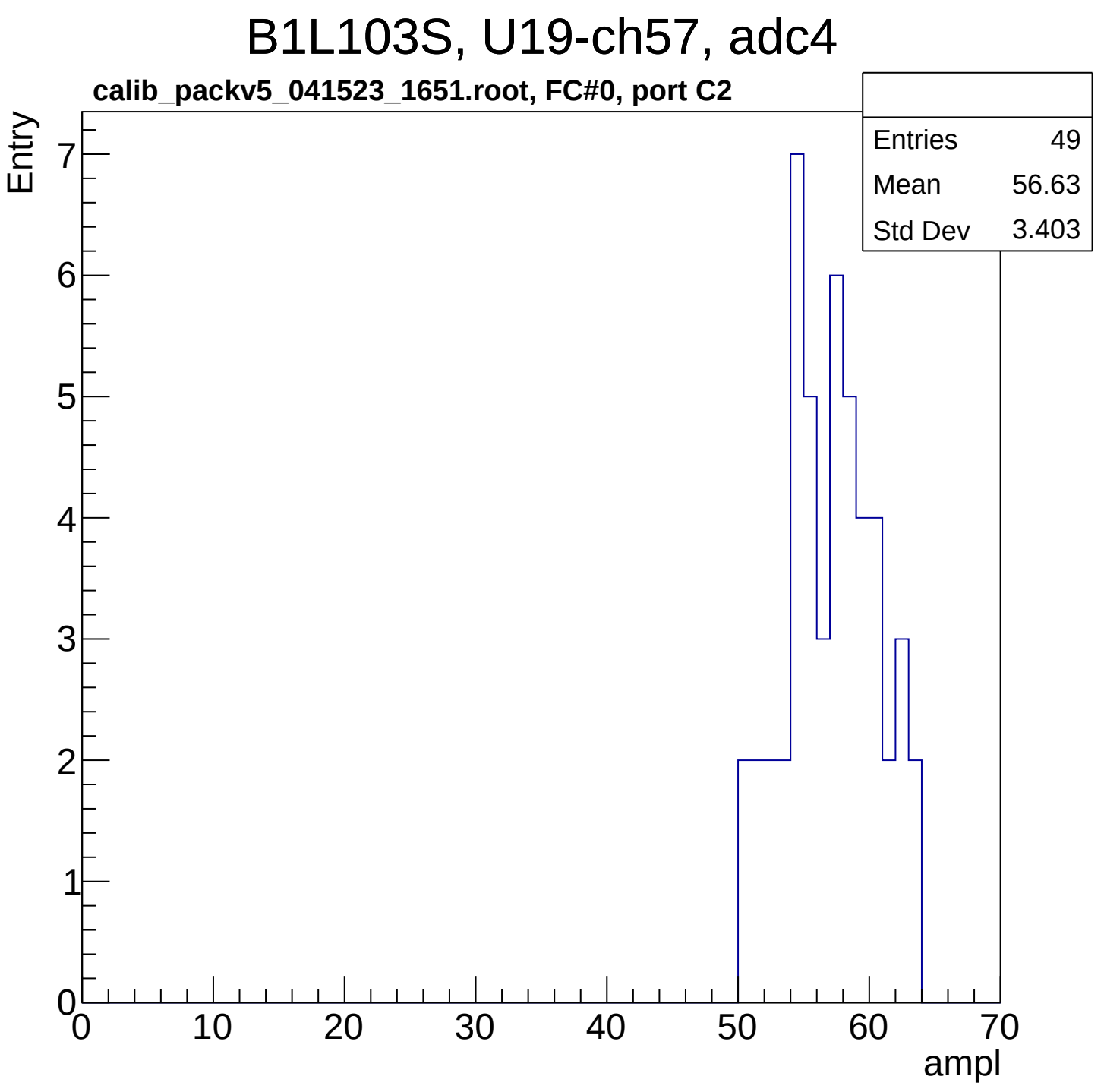
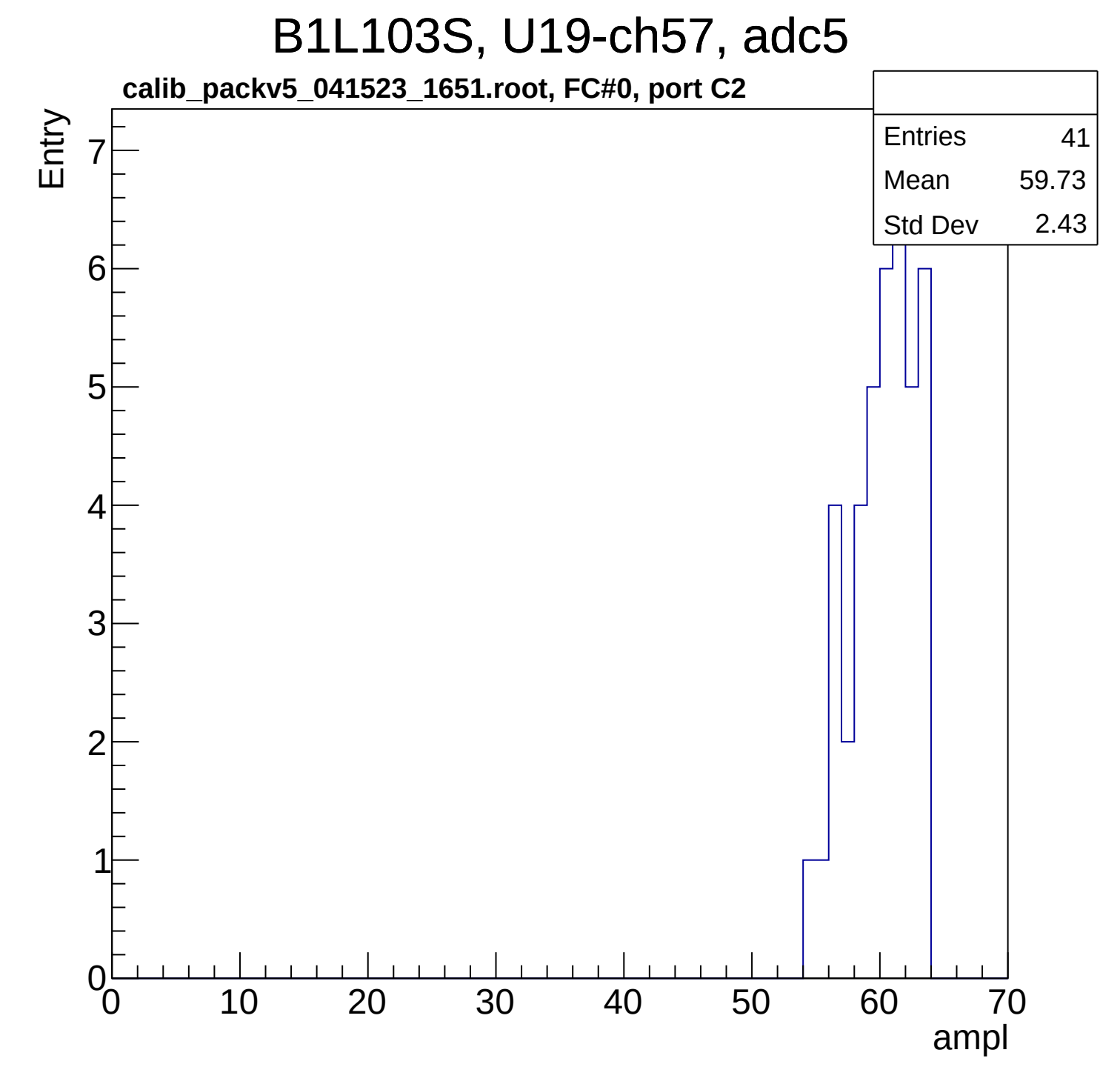
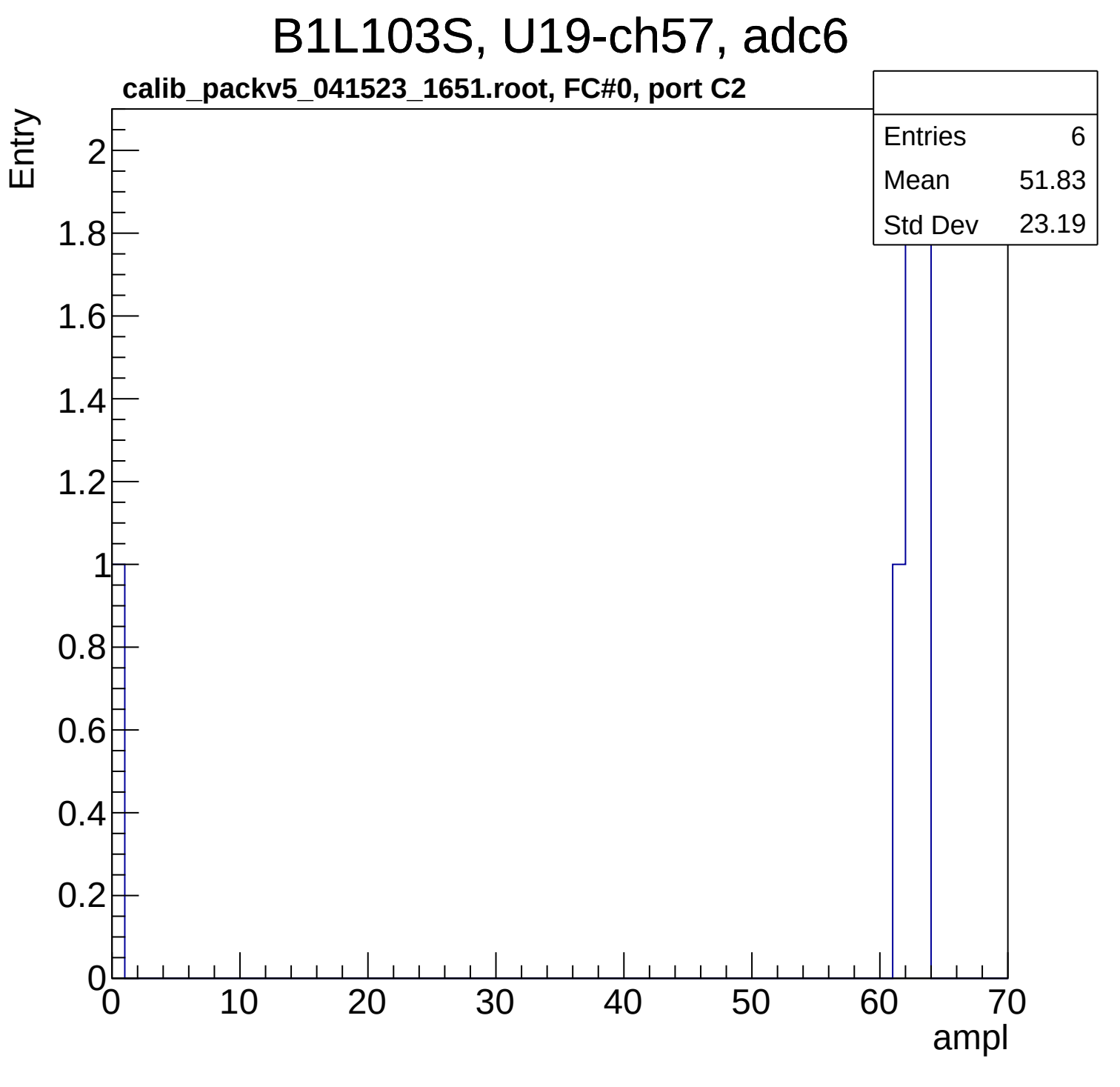
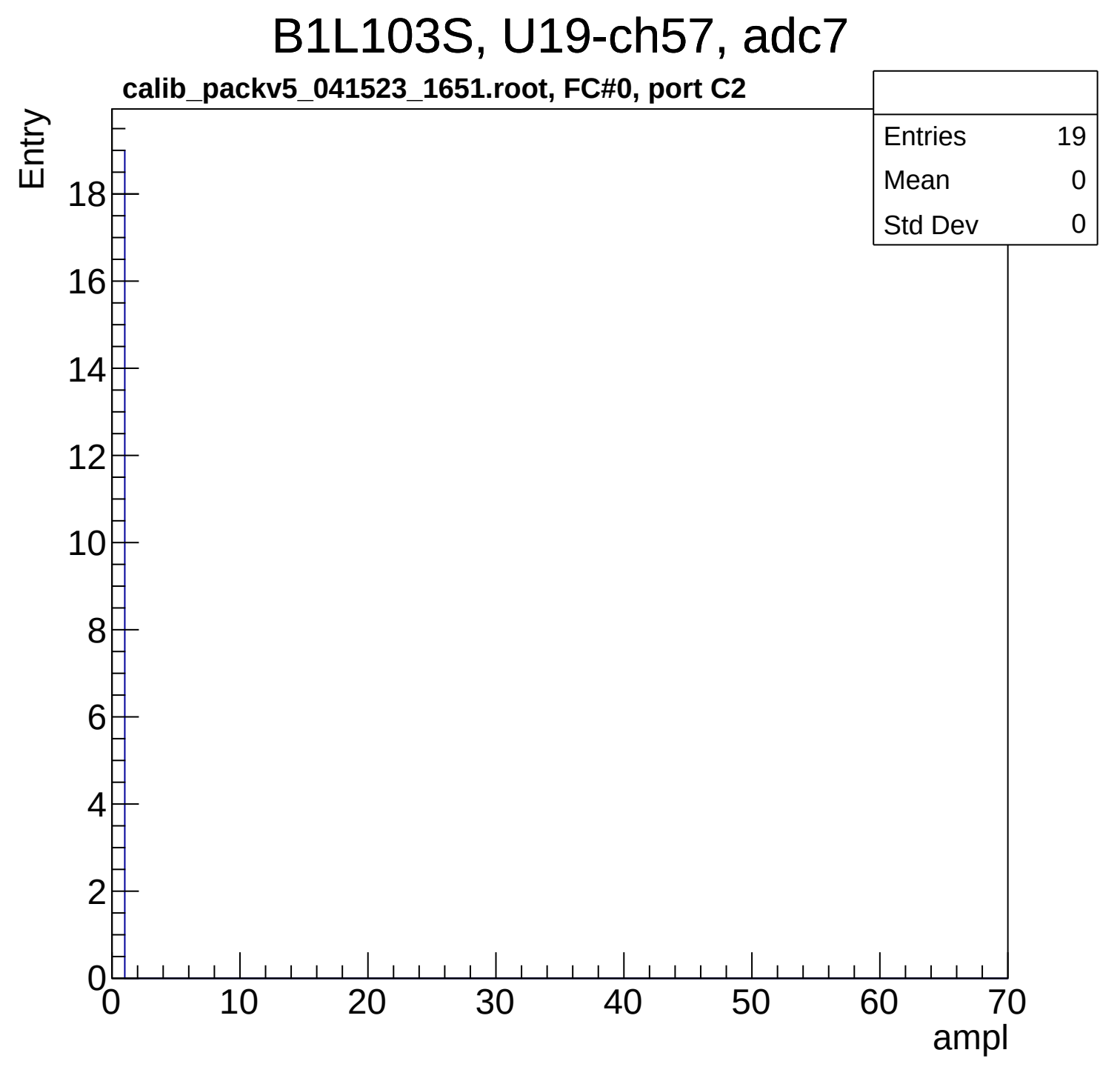
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

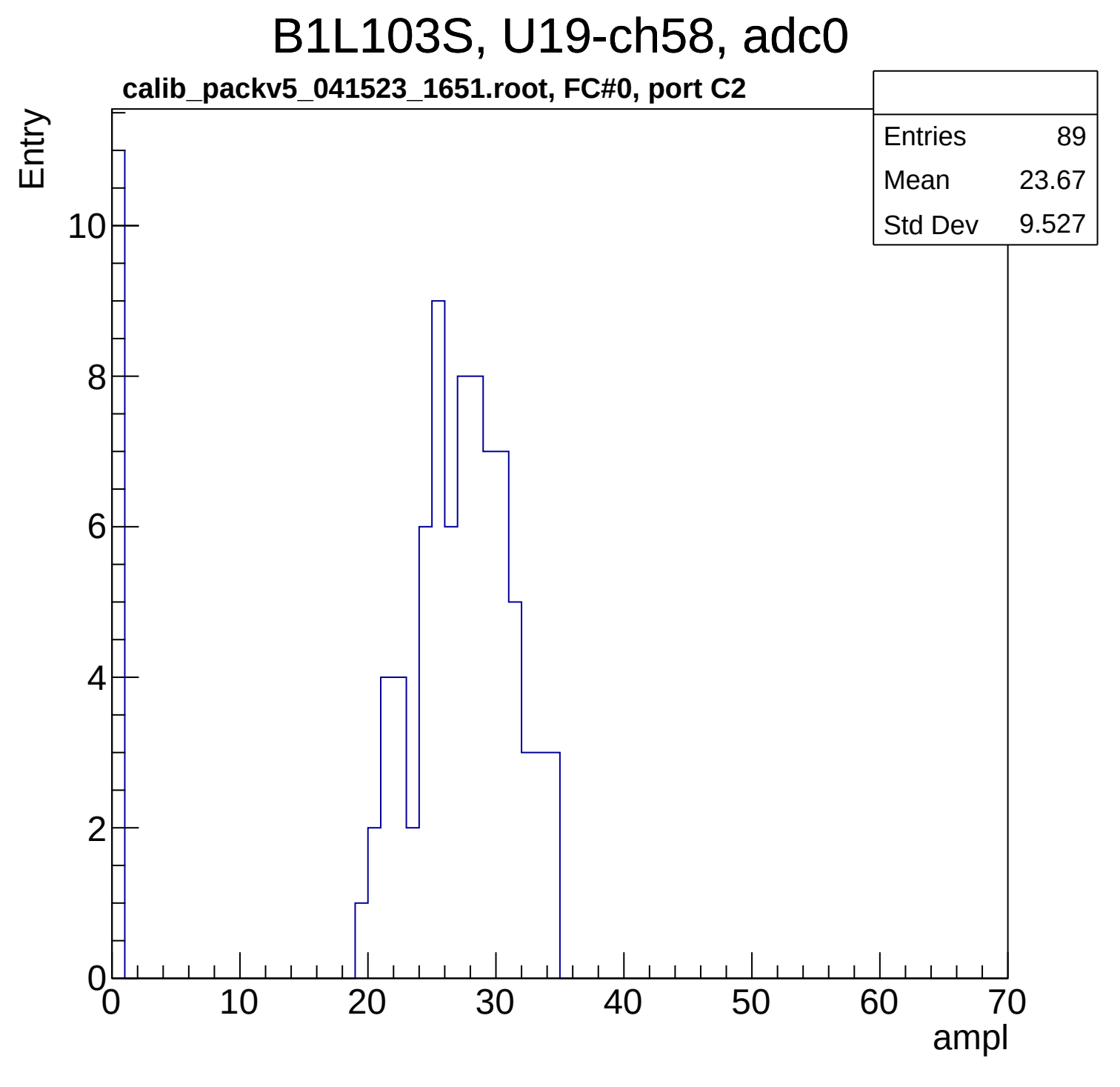

B1L103S, U19-ch57, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 50.01
Std Dev 3.832
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

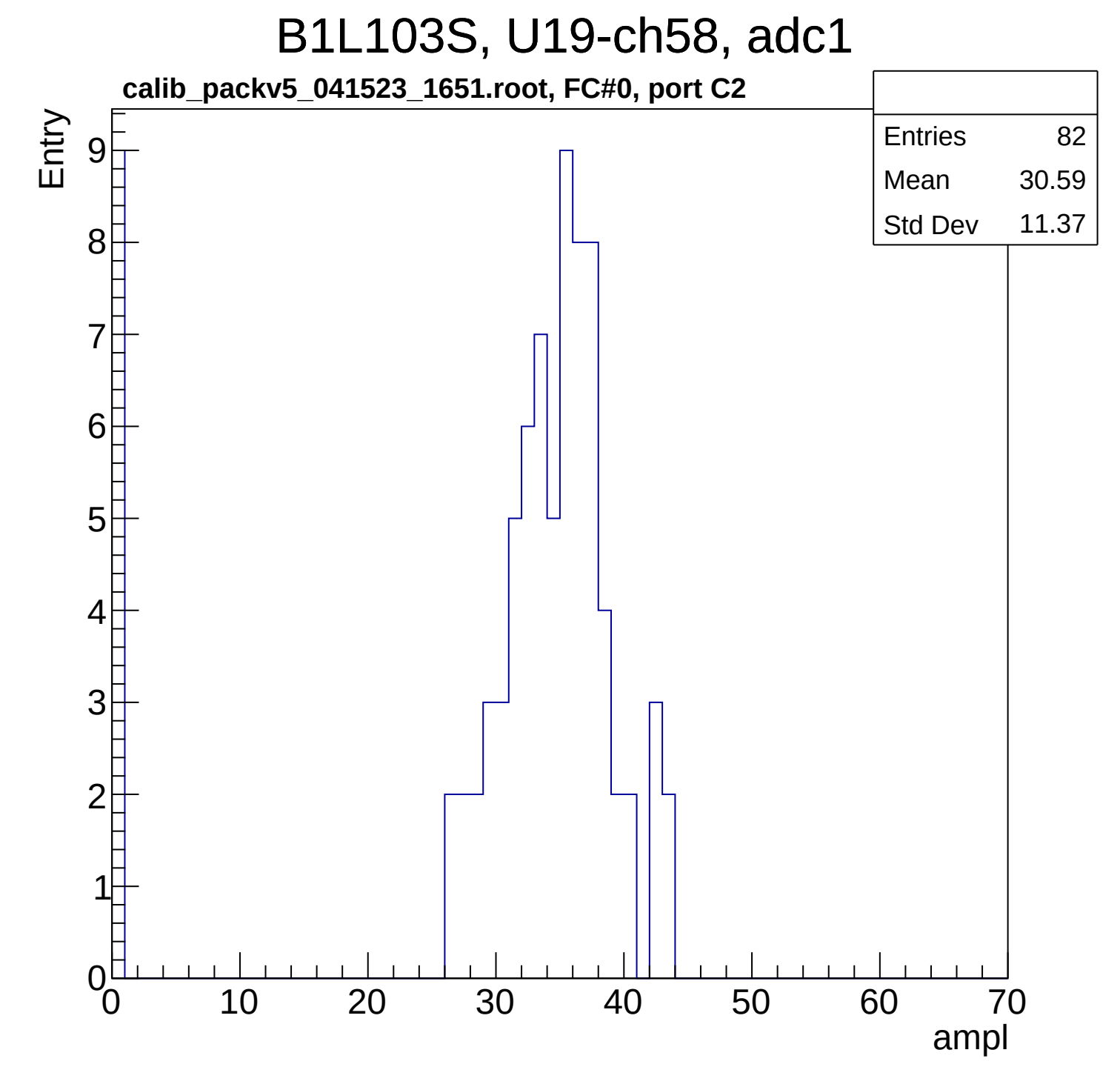

B1L103S, U19-ch57, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 56.63
Std Dev 3.403
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch57, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 59.73
Std Dev 2.43
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch57, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 51.83
Std Dev 23.19
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U19-ch57, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch58, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 23.67
Std Dev 9.527
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch58, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 30.59
Std Dev 11.37
Entry
ampl
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2
3
4
5
6
7
8
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0
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40
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60
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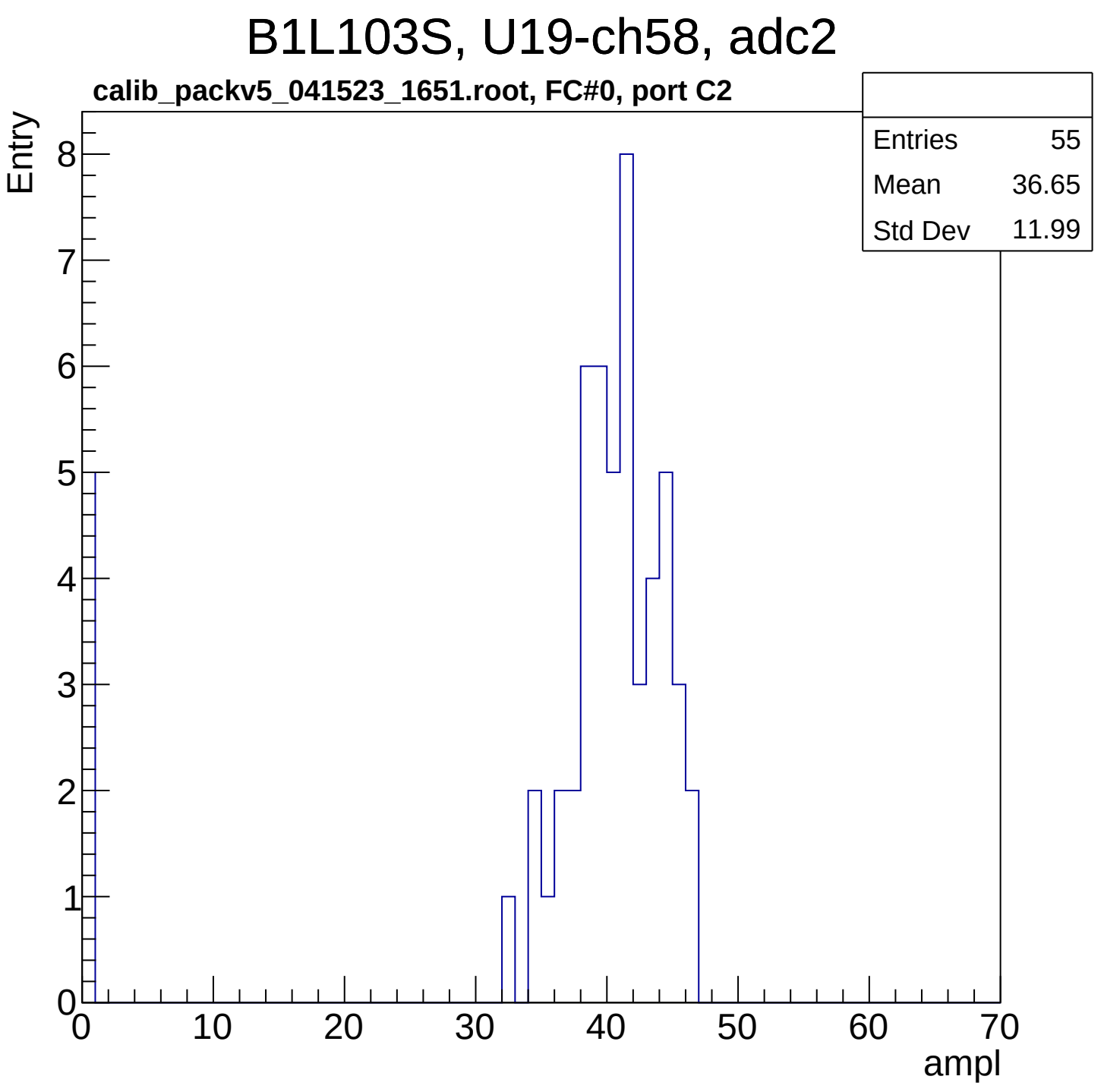
B1L103S, U19-ch58, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 36.65
Std Dev 11.99
Entry
ampl
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5
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7
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0
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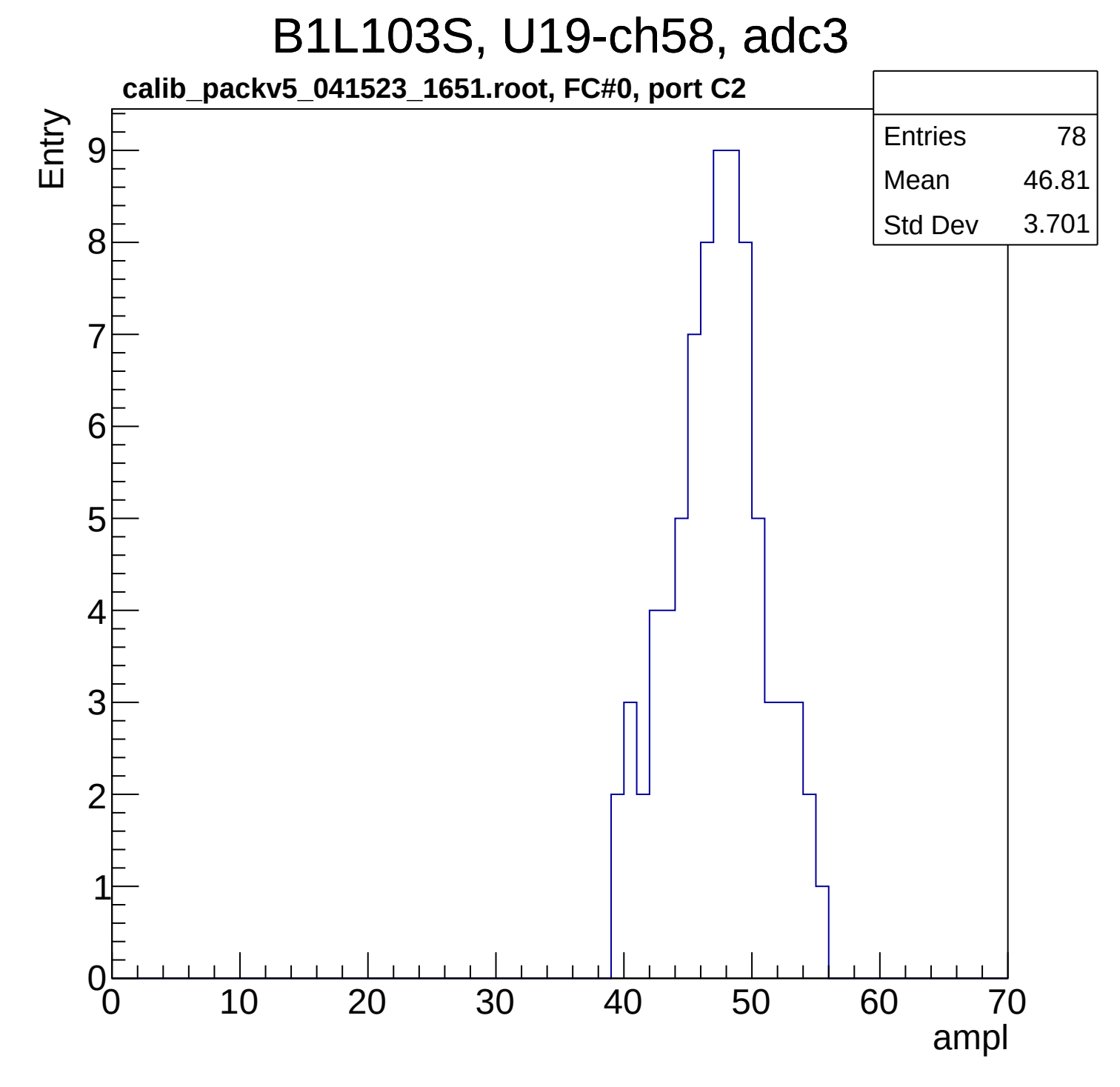
B1L103S, U19-ch58, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 46.81
Std Dev 3.701
Entry
ampl
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2
3
4
5
6
7
8
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0
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60
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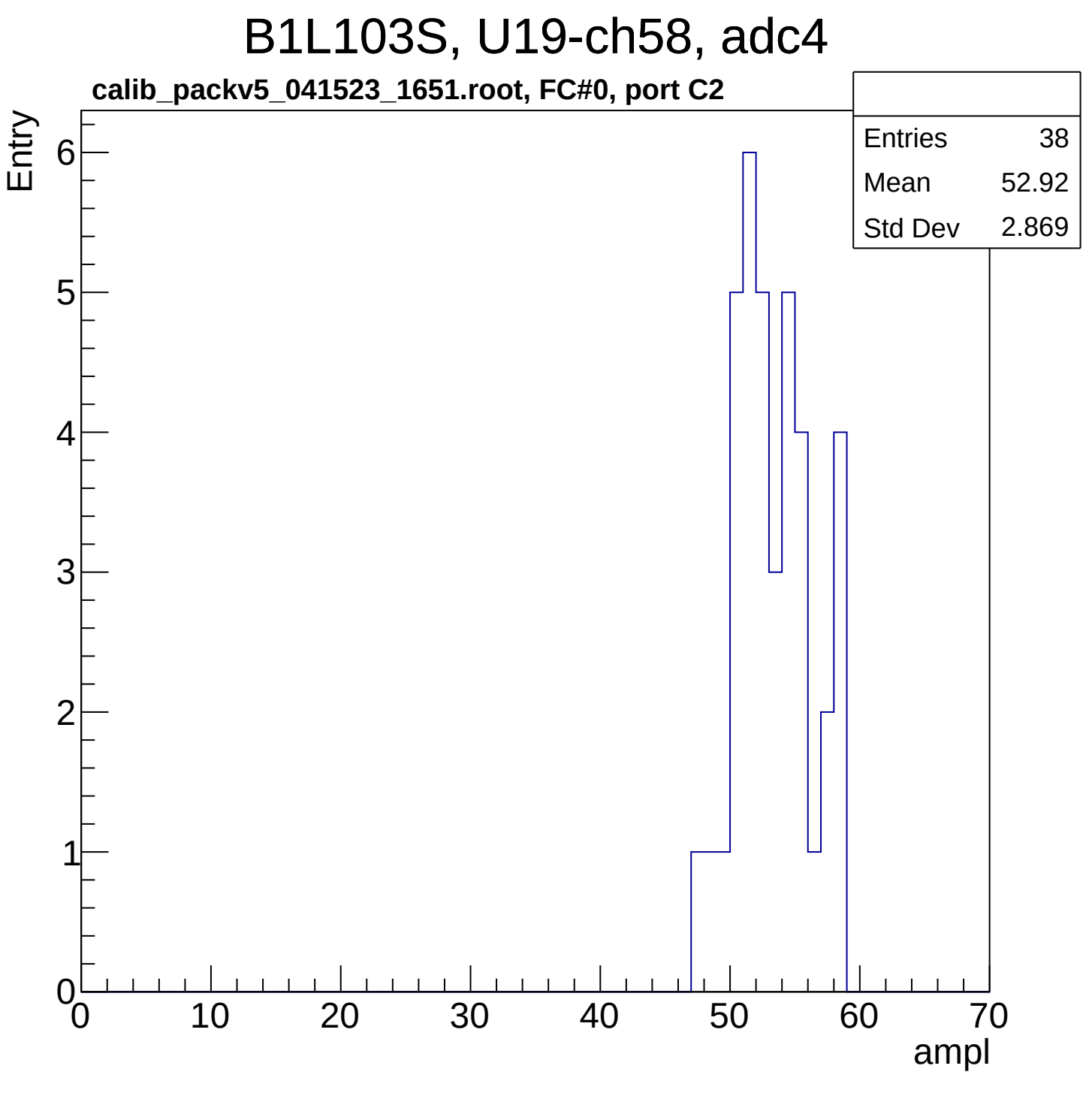
B1L103S, U19-ch58, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 52.92
Std Dev 2.869
Entry
0
1
2
3
4
5
6
0
10
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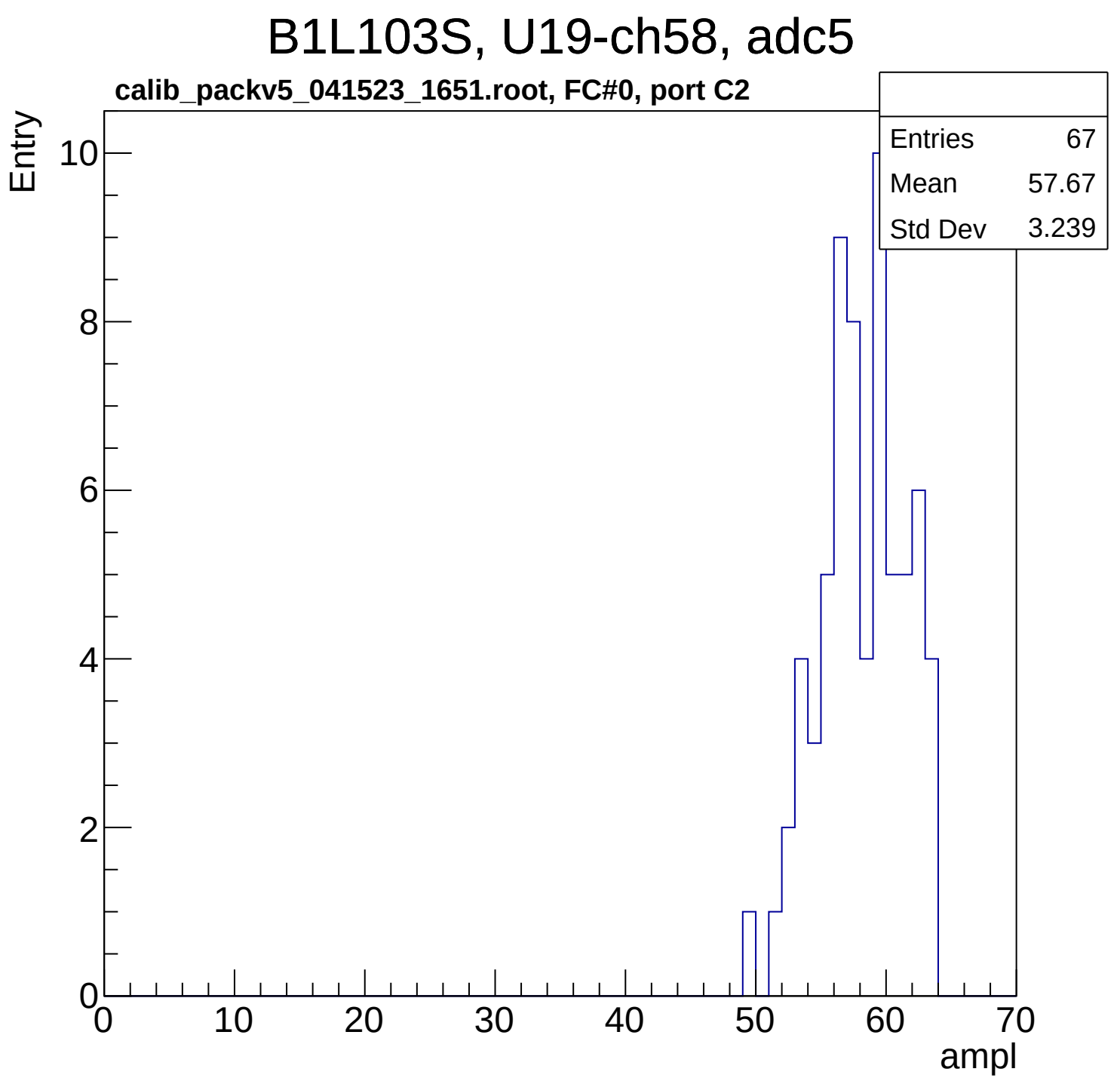
50
60
70
ampl


B1L103S, U19-ch58, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 57.67
Std Dev 3.239
Entry
0
2
4
6
8
10
0
10
20
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50
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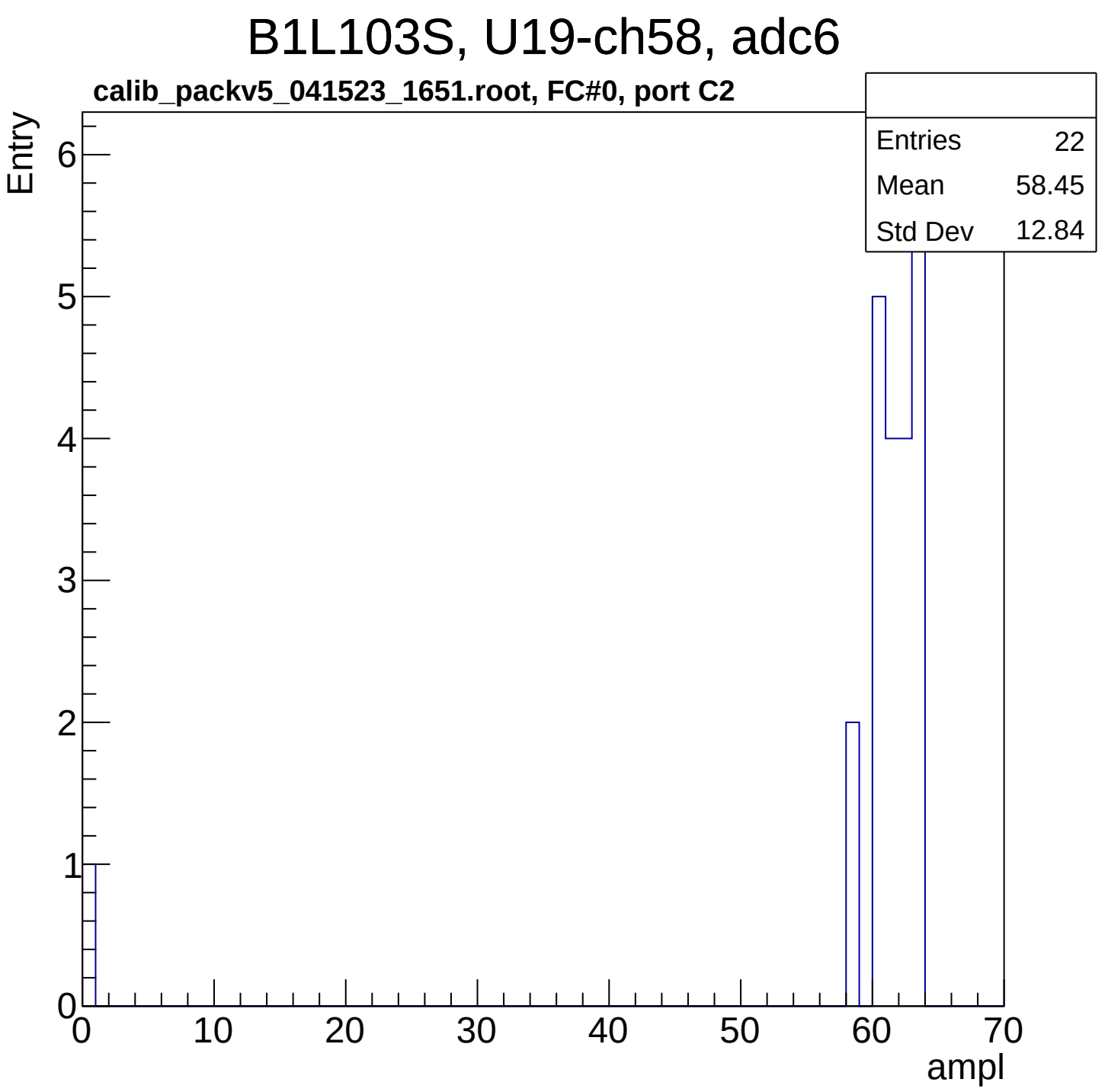
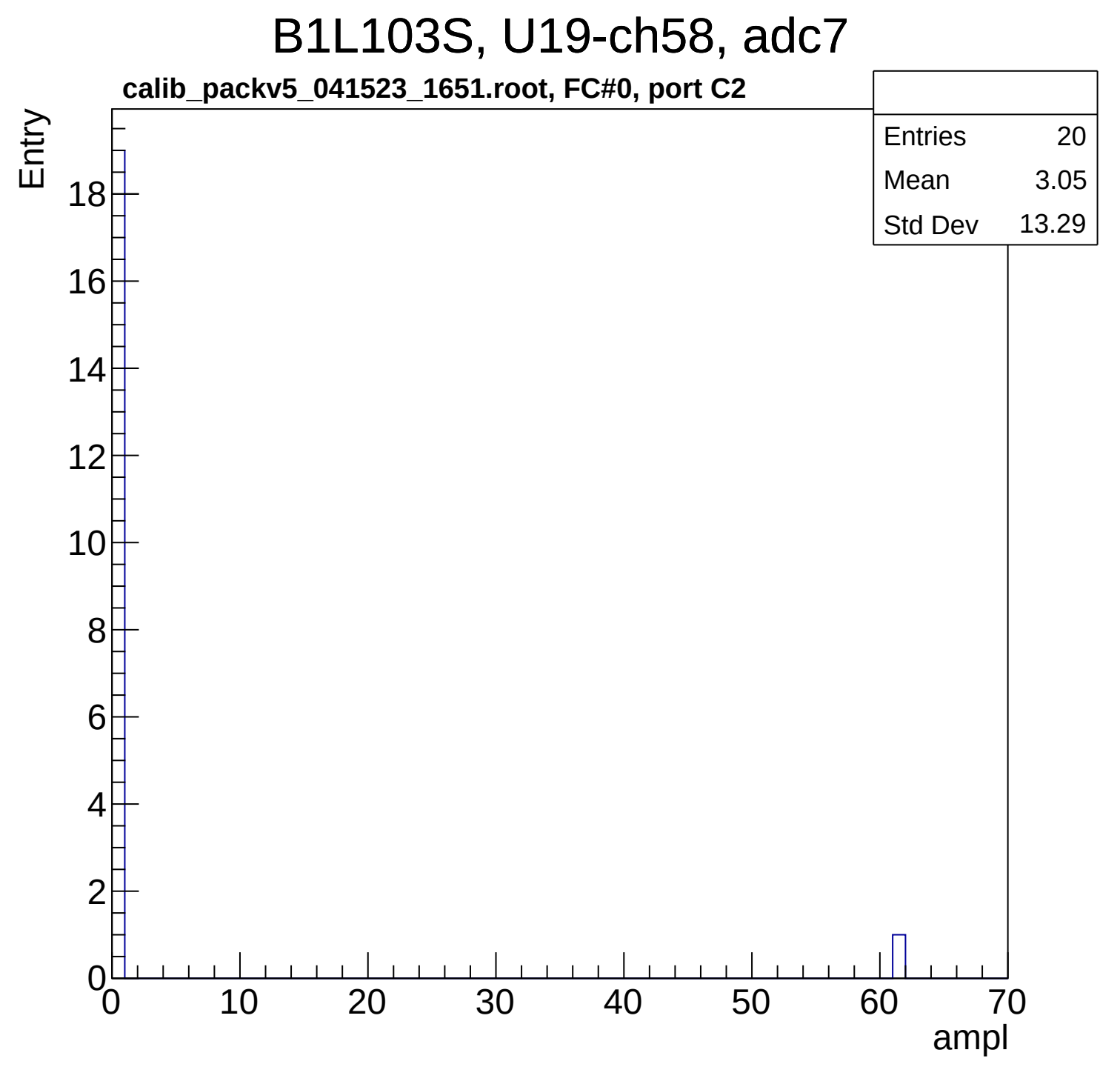
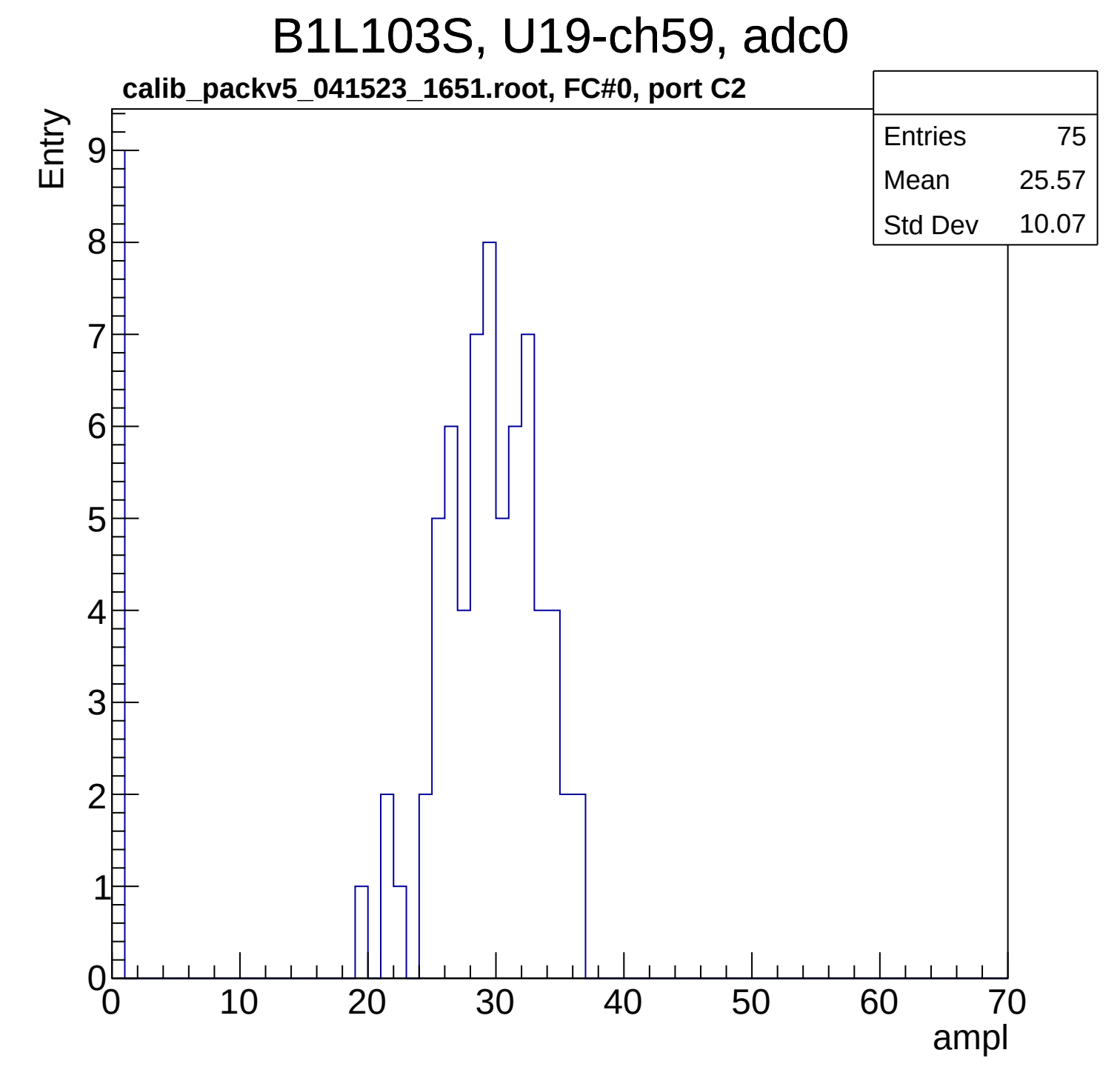
70
ampl


B1L103S, U19-ch58, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 58.45
Std Dev 12.84
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch58, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.05
Std Dev 13.29
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch59, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 25.57
Std Dev 10.07
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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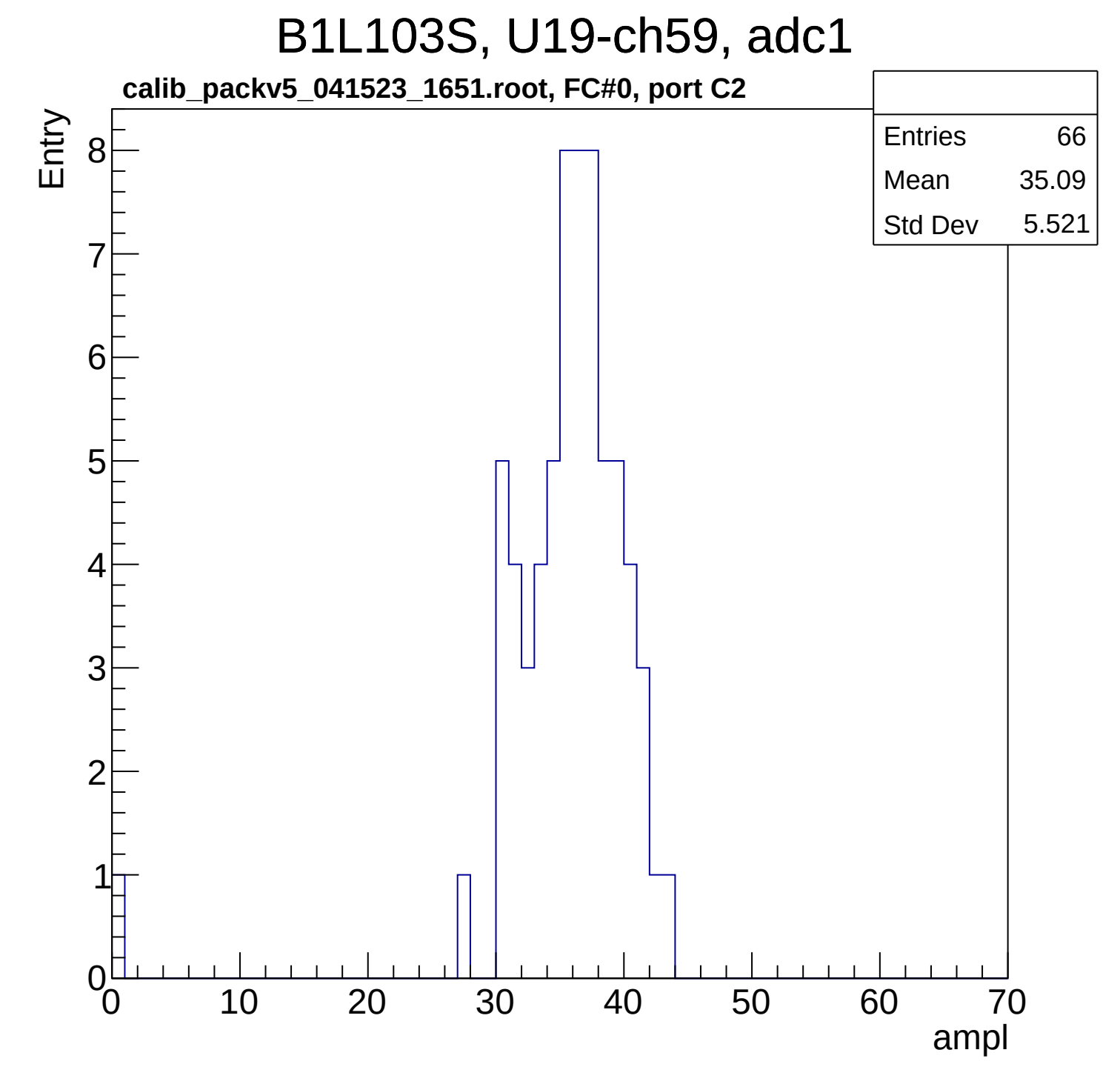
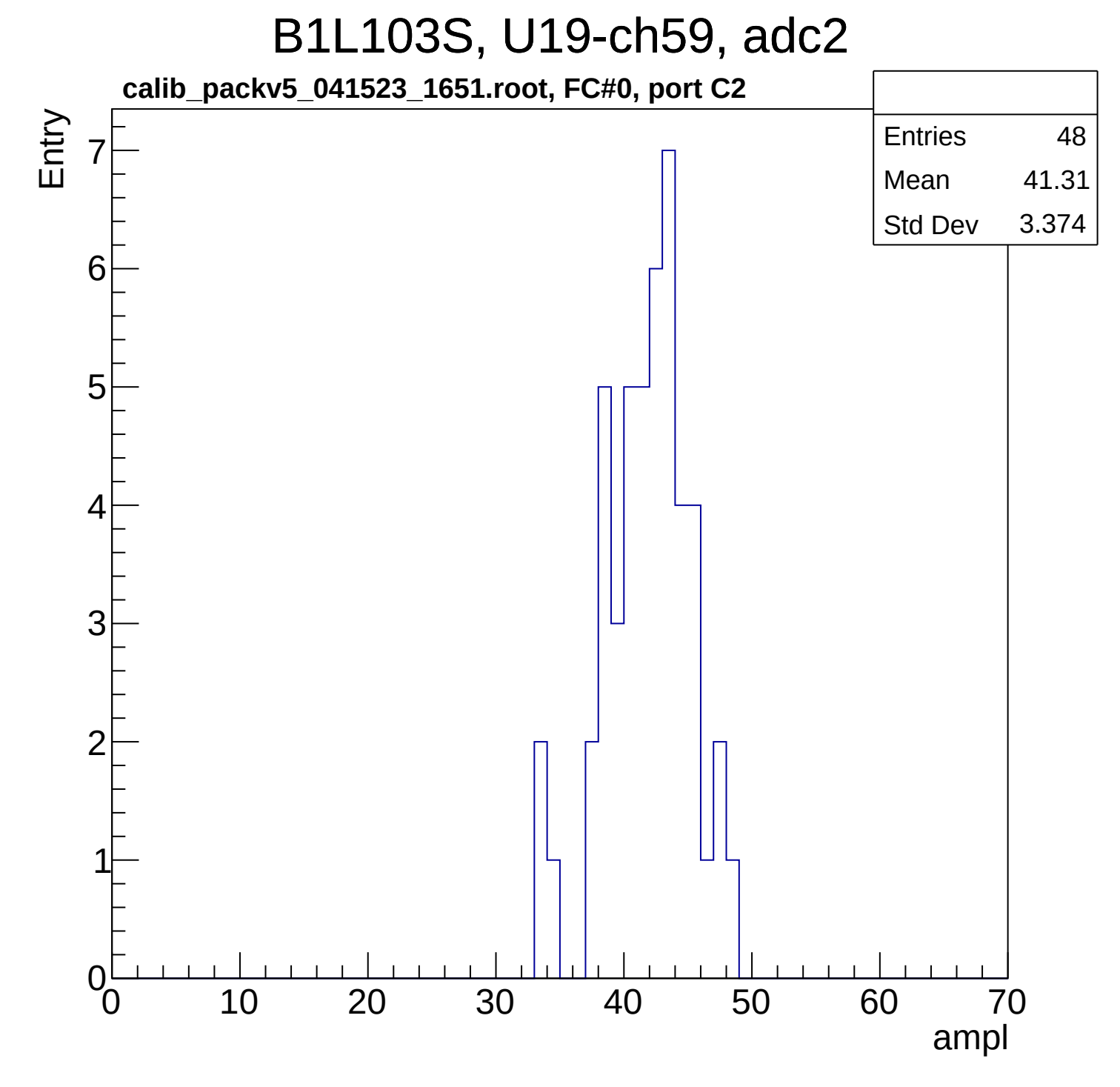
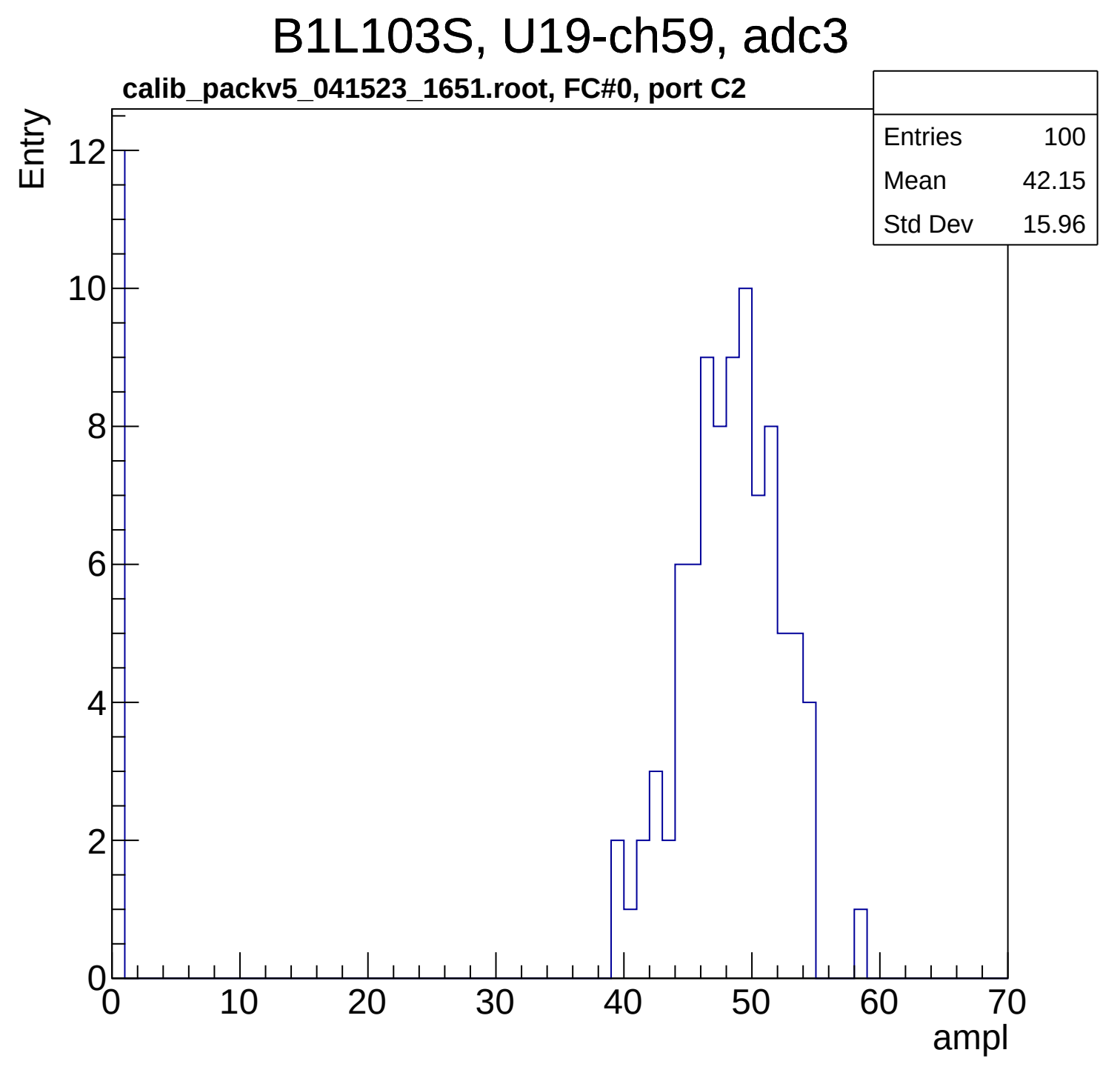
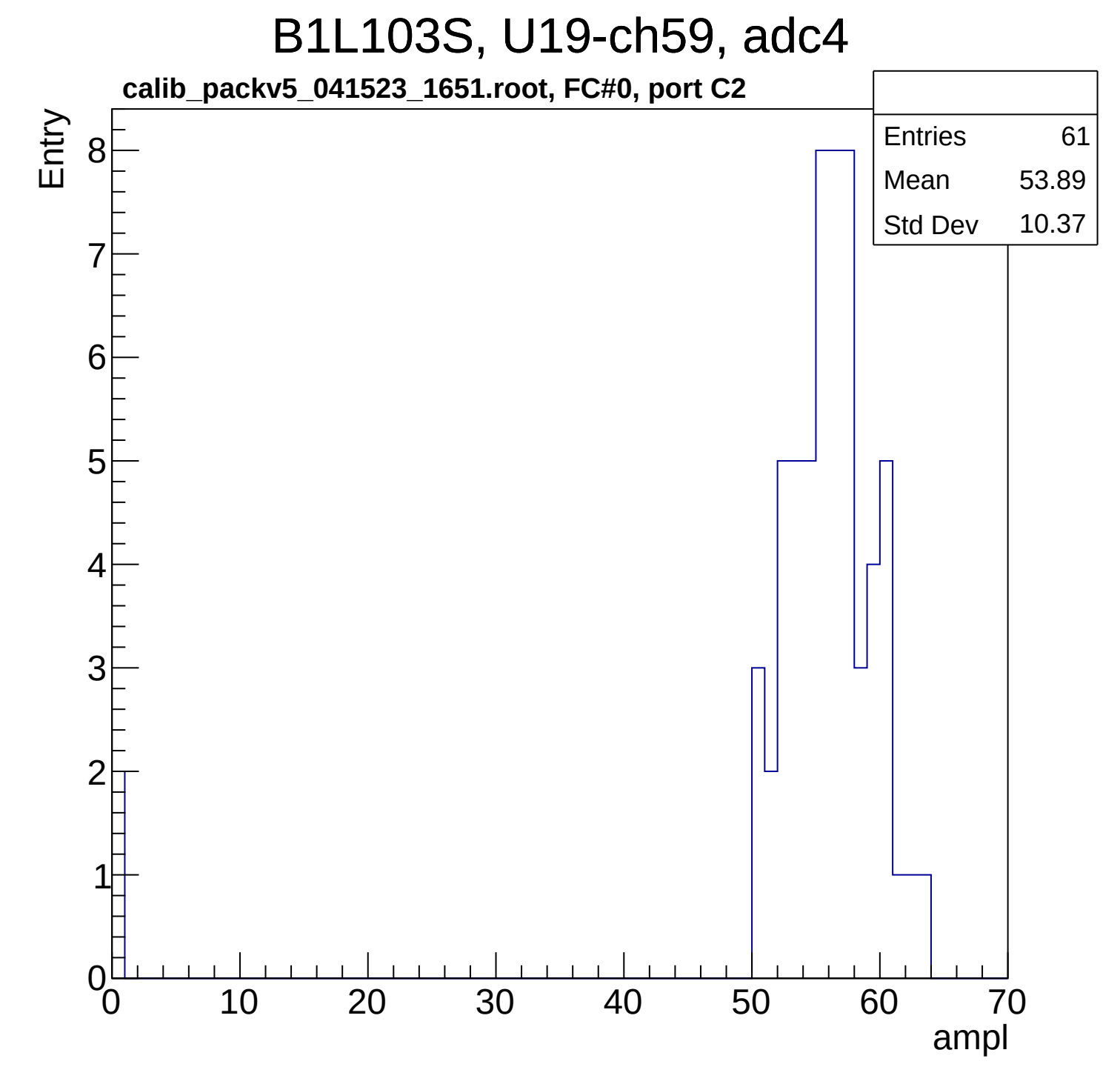

B1L103S, U19-ch59, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 35.09
Std Dev 5.521
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch59, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 41.31
Std Dev 3.374
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch59, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 100
Mean 42.15
Std Dev 15.96
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch59, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 53.89
Std Dev 10.37
Entry
0
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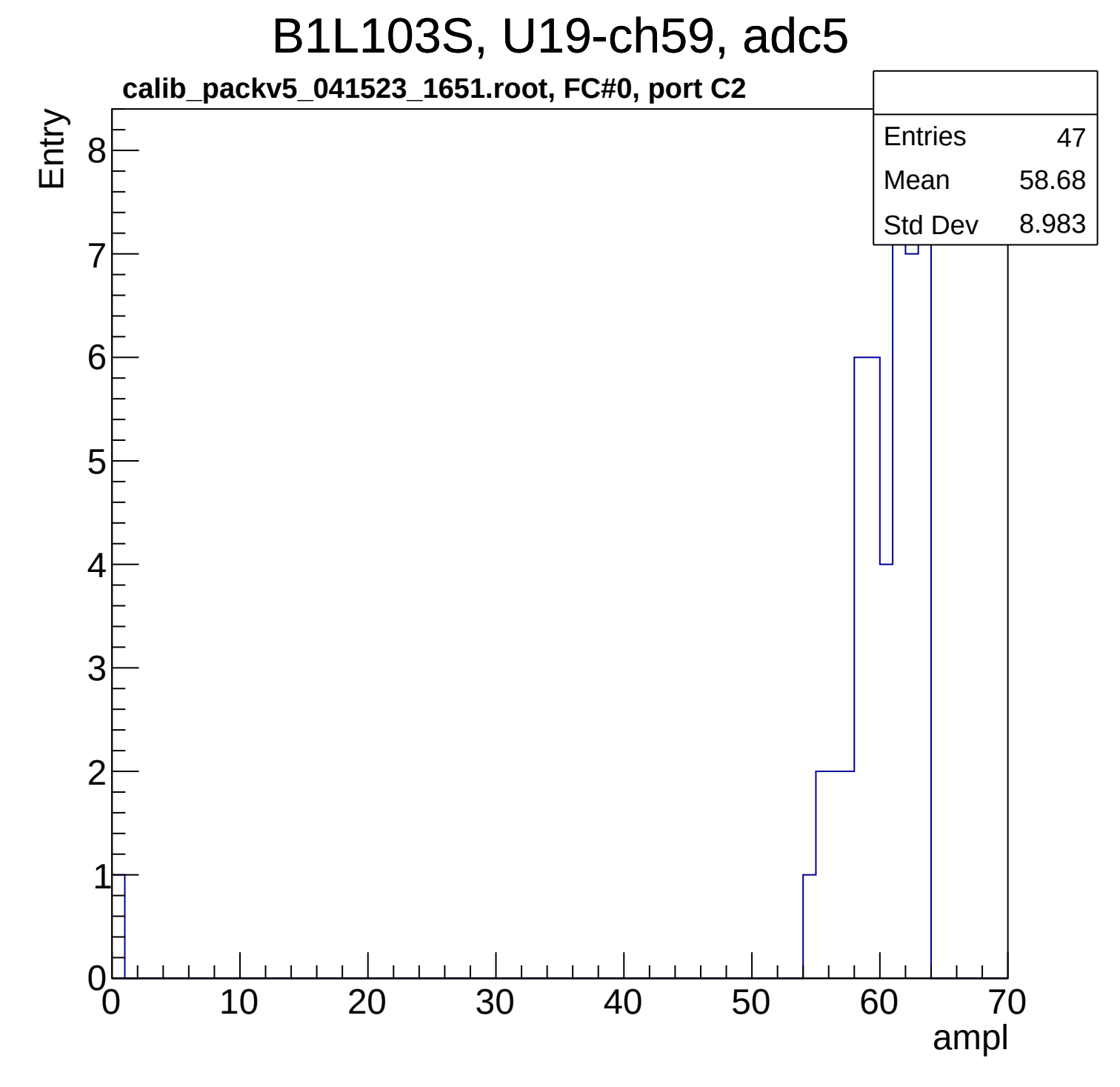
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch59, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 58.68
Std Dev 8.983
Entry
ampl
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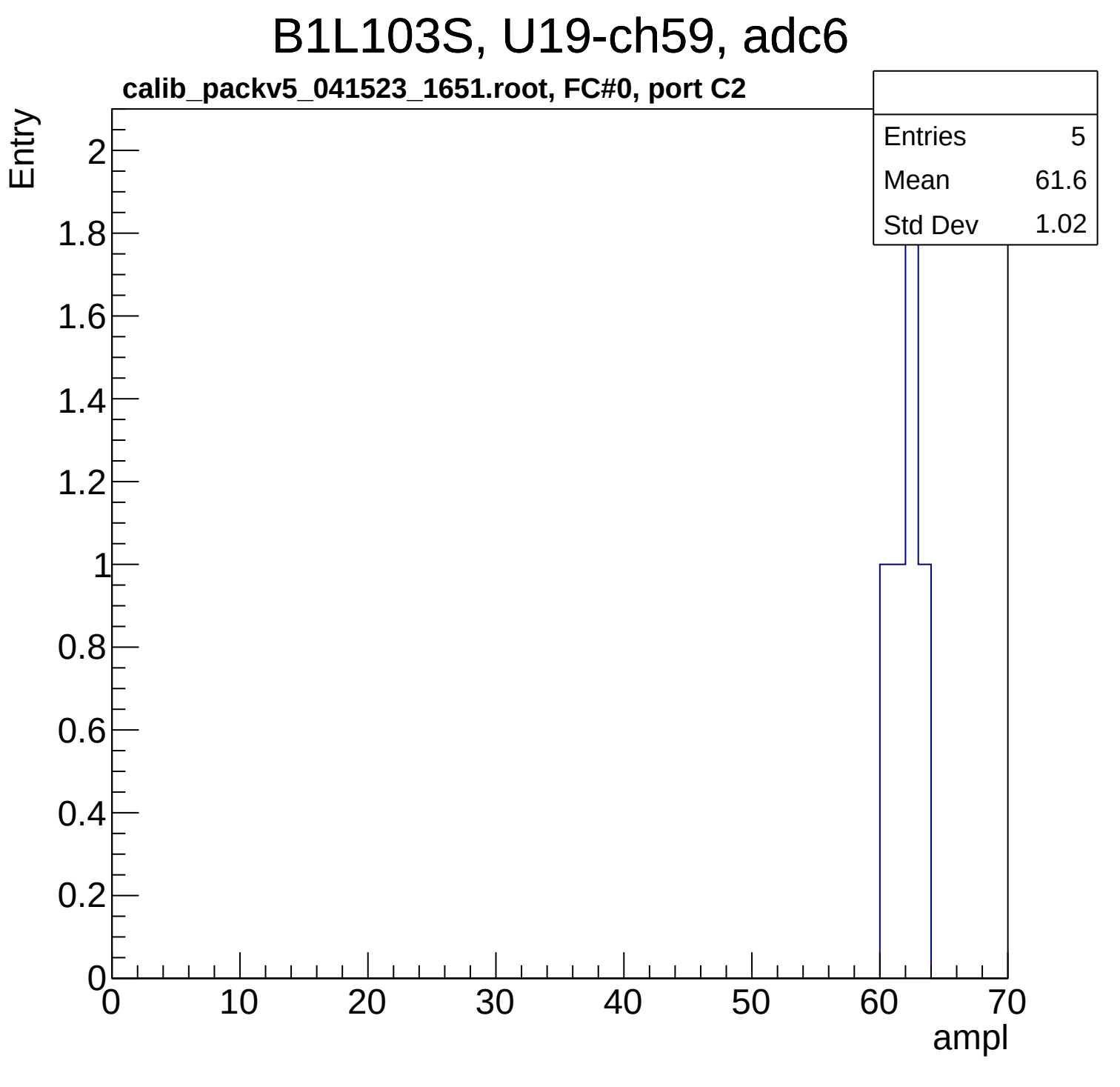
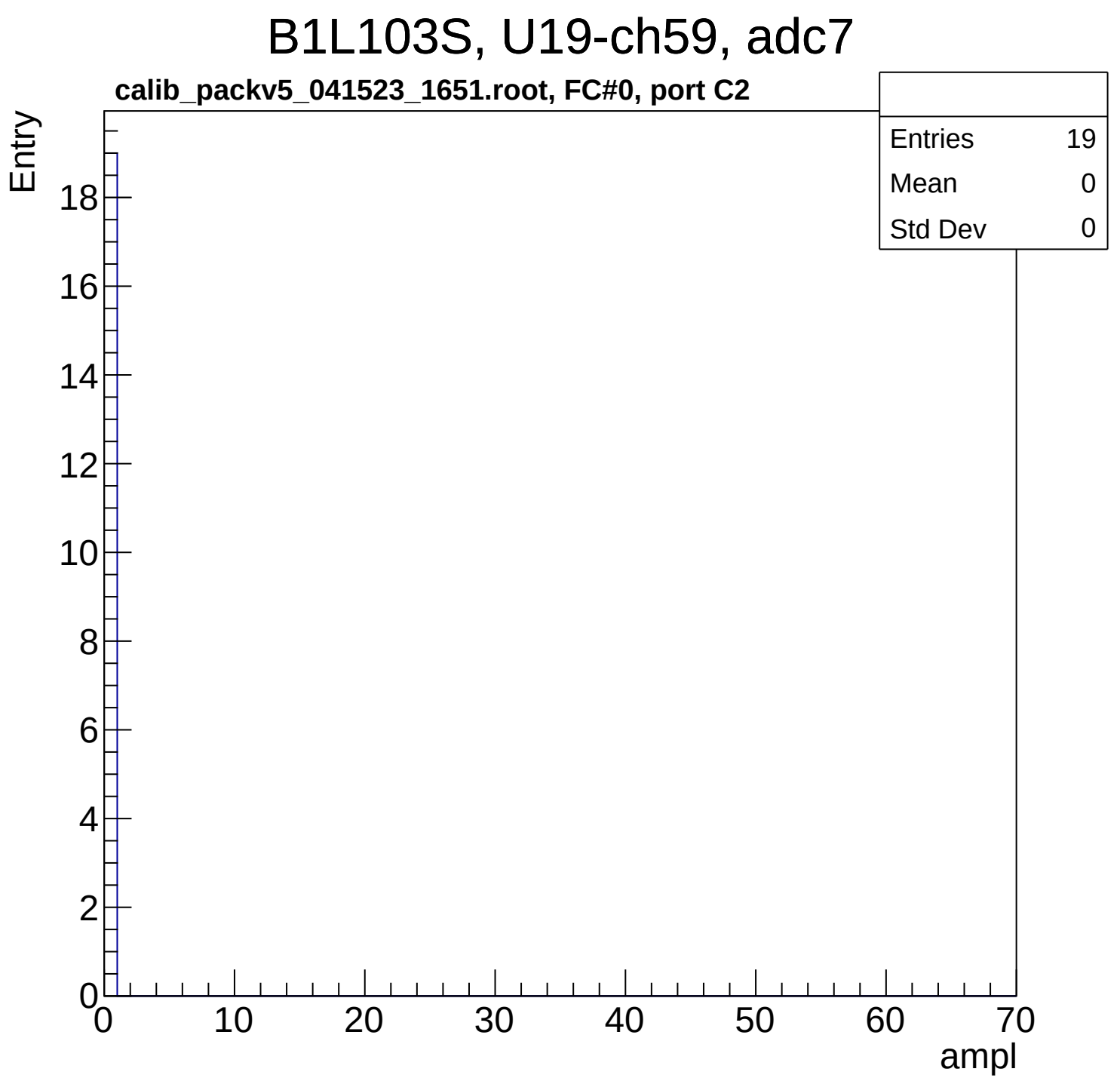
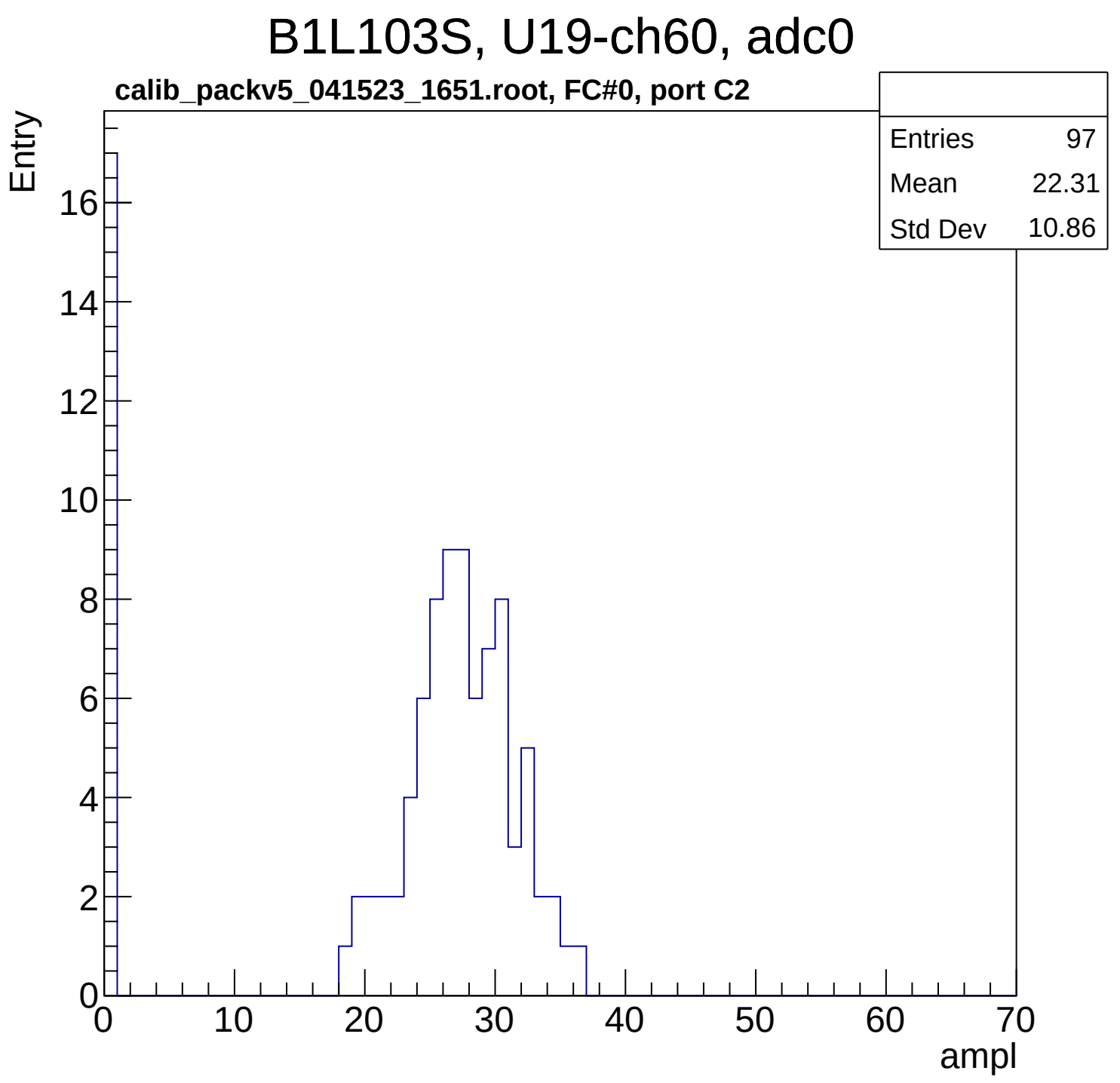
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch59, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 61.6
Std Dev 1.02
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U19-ch59, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch60, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 22.31
Std Dev 10.86
Entry
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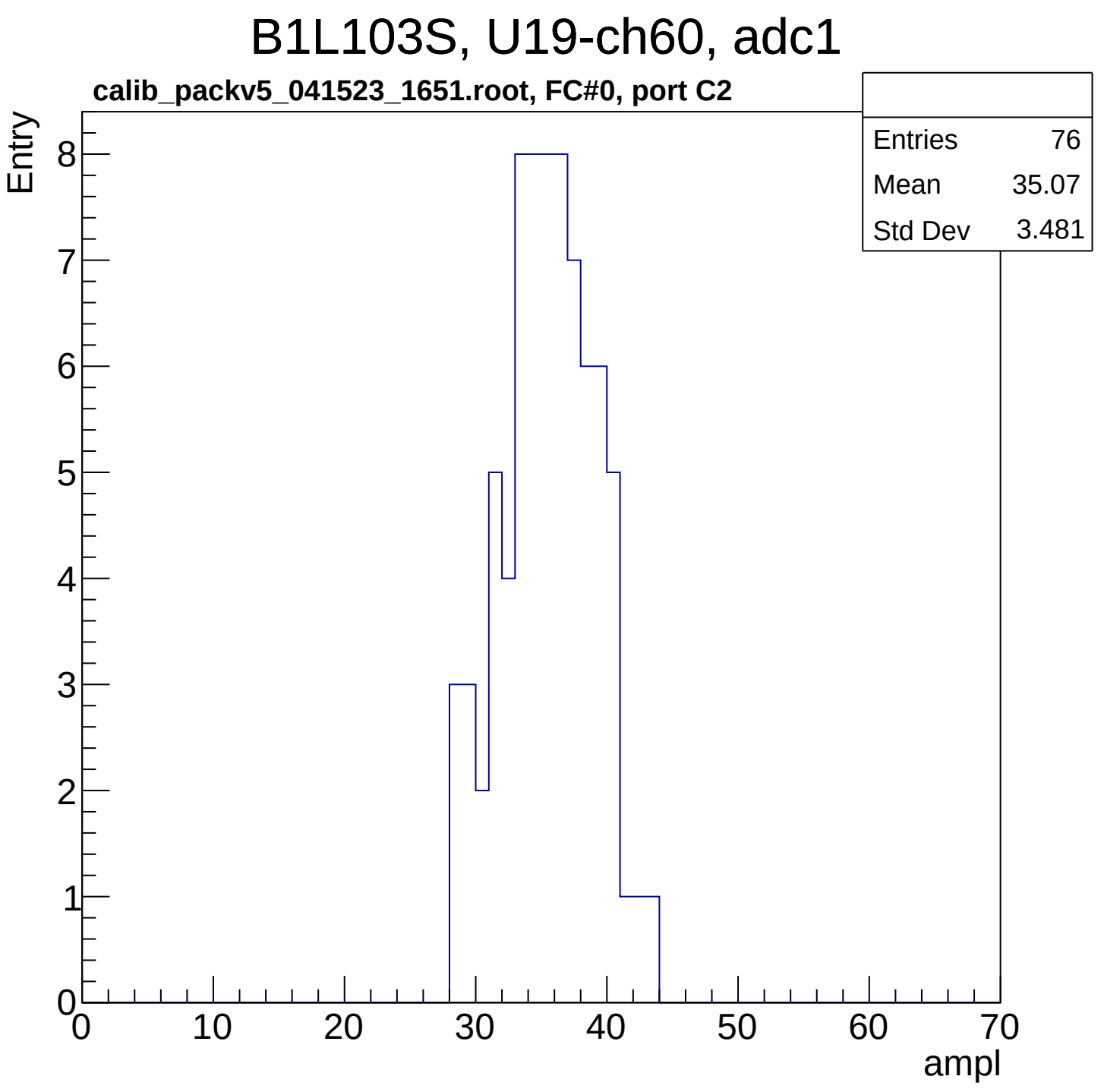
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch60, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 35.07
Std Dev 3.481
Entry
ampl
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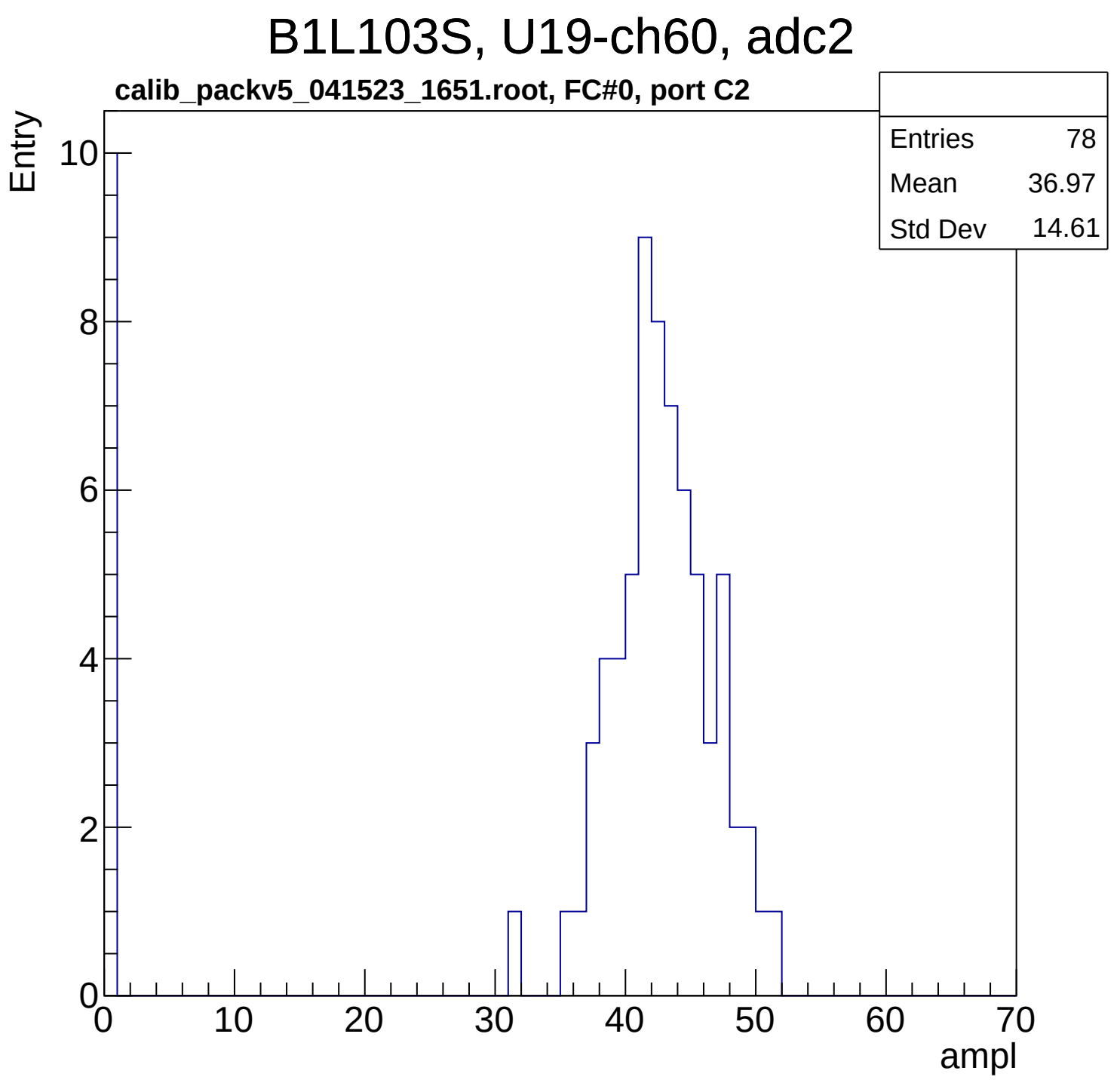
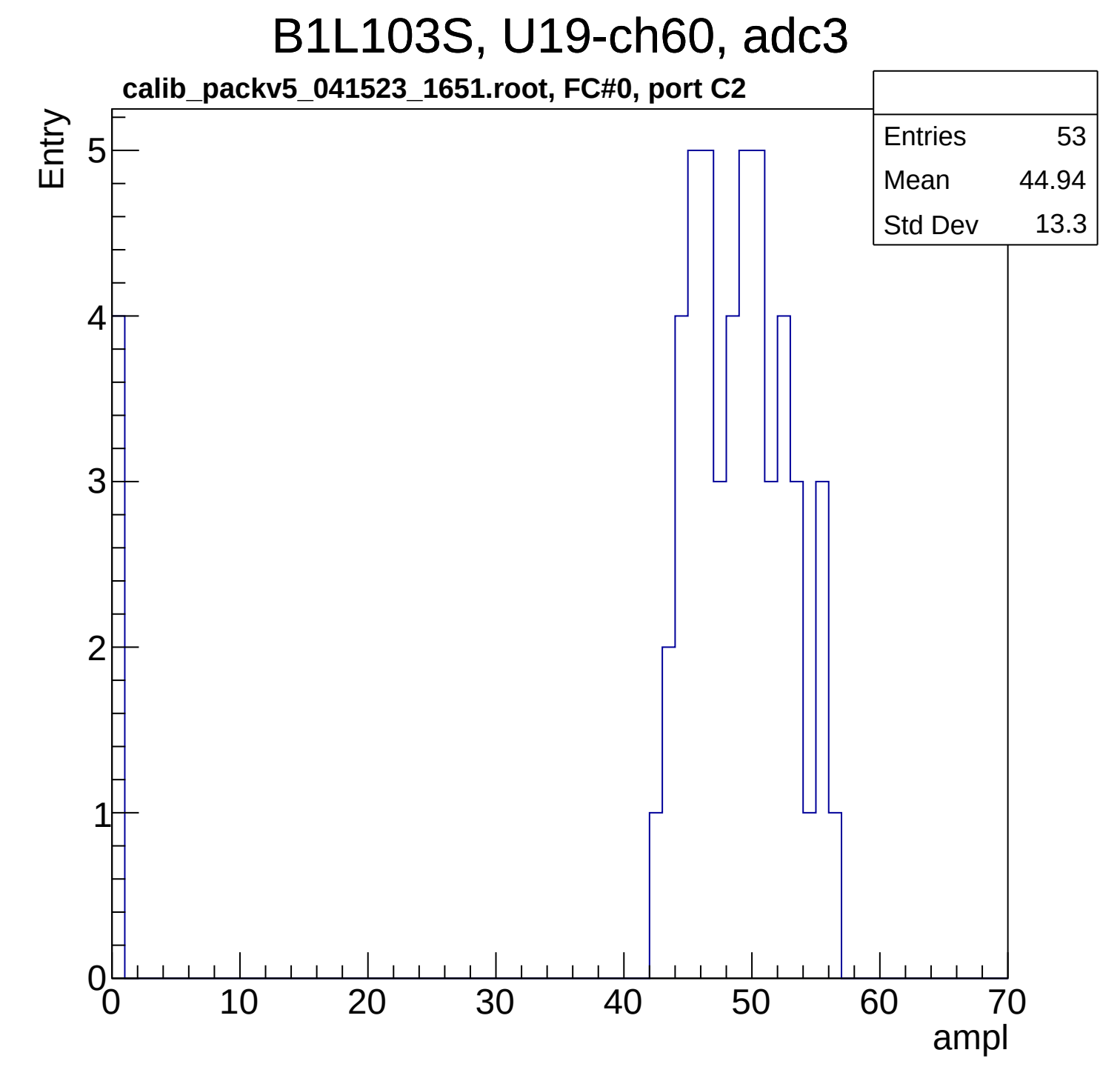
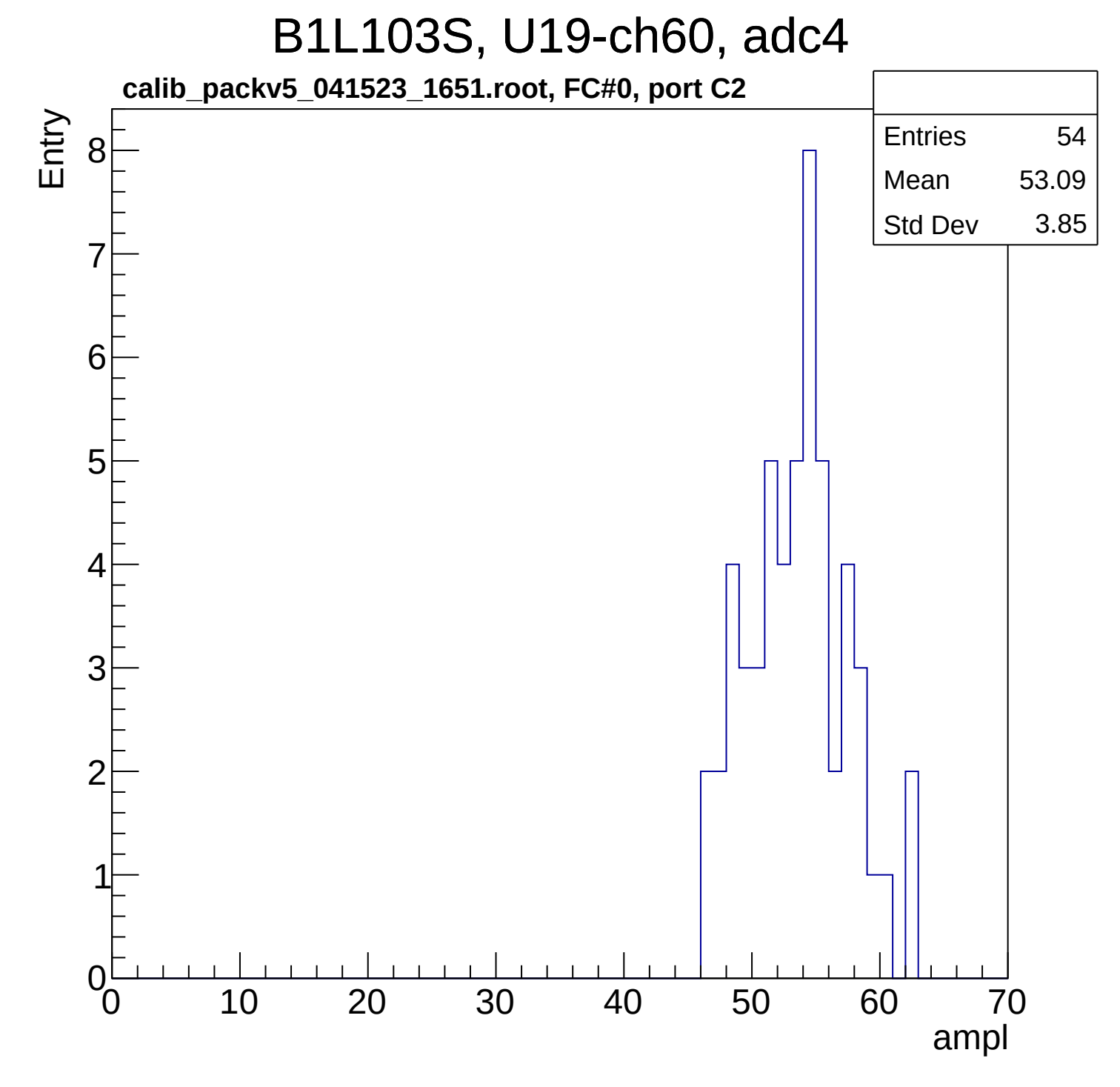
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch60, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 36.97
Std Dev 14.61
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch60, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 44.94
Std Dev 13.3
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U19-ch60, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 53.09
Std Dev 3.85
Entry
ampl
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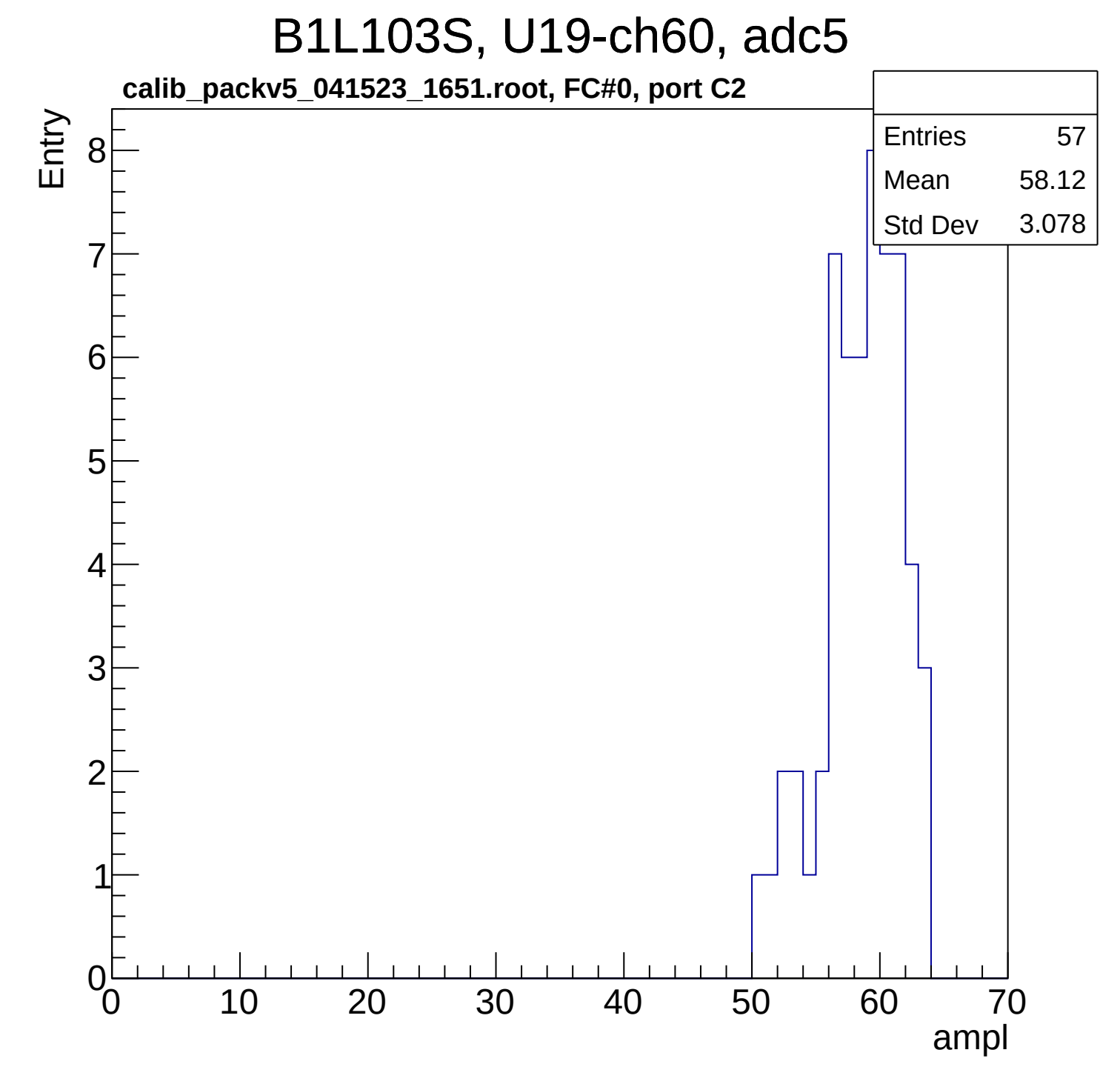
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch60, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 58.12
Std Dev 3.078
Entry
ampl
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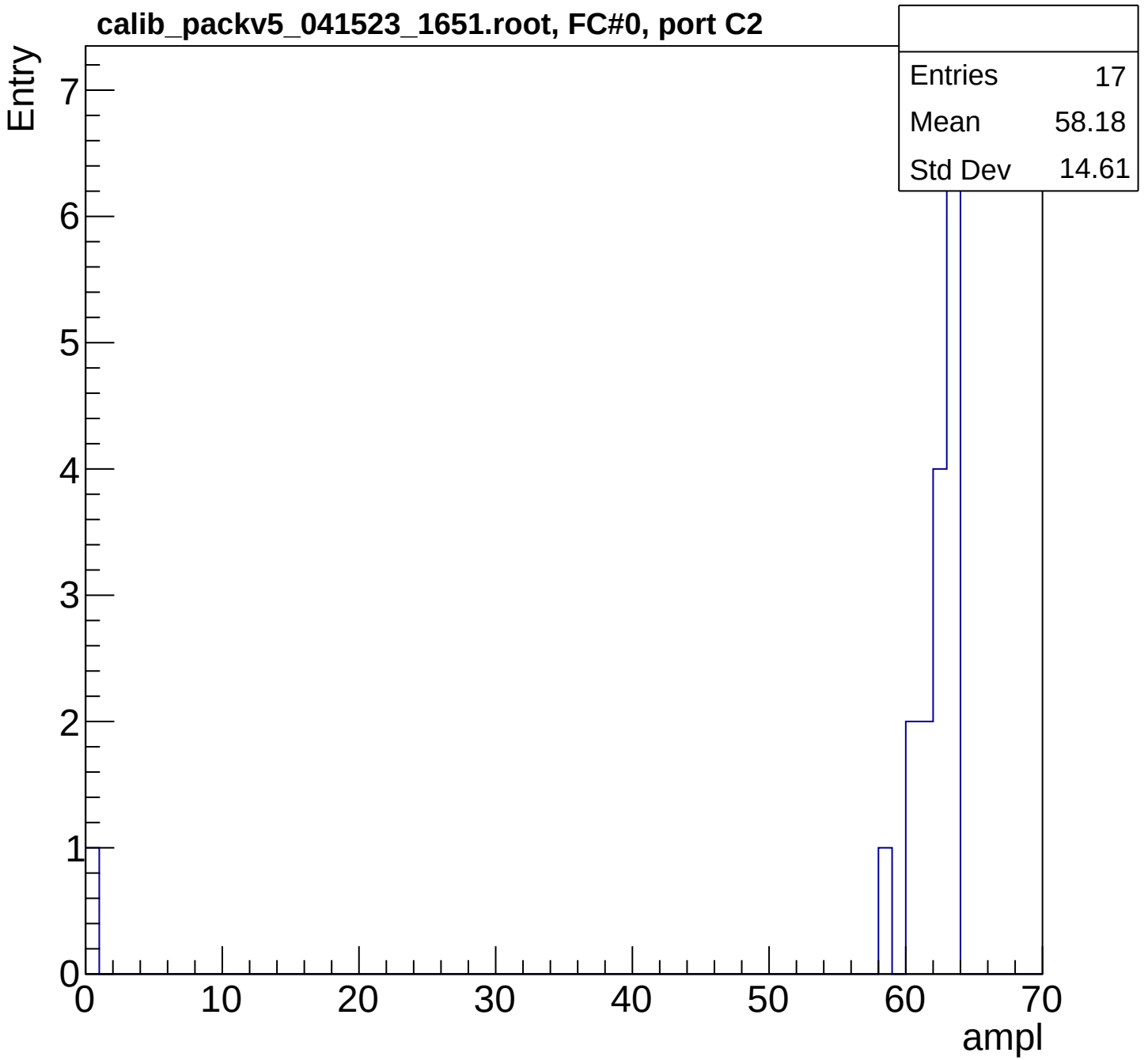
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch60, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 58.18
Std Dev 14.61
Entry
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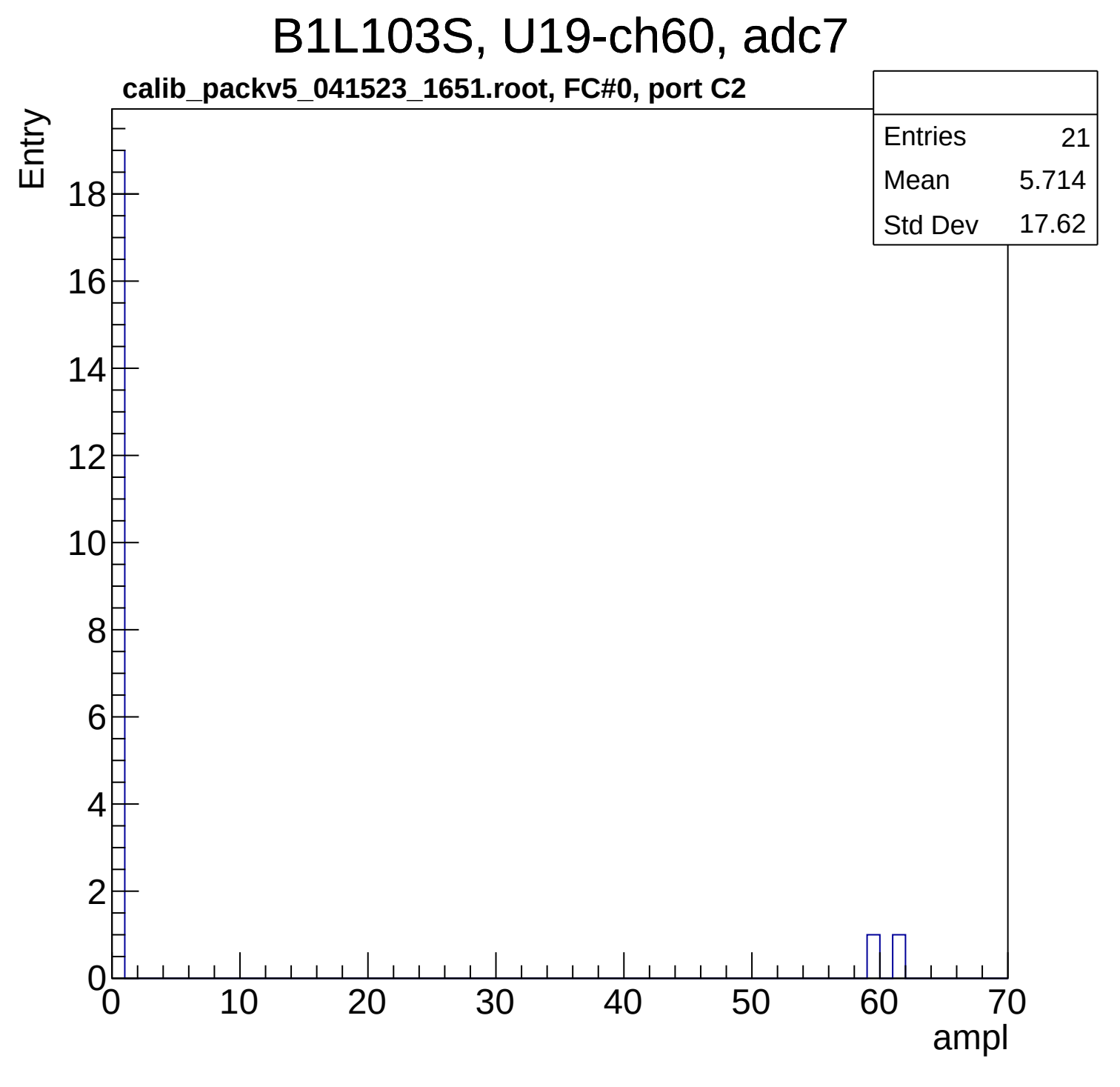
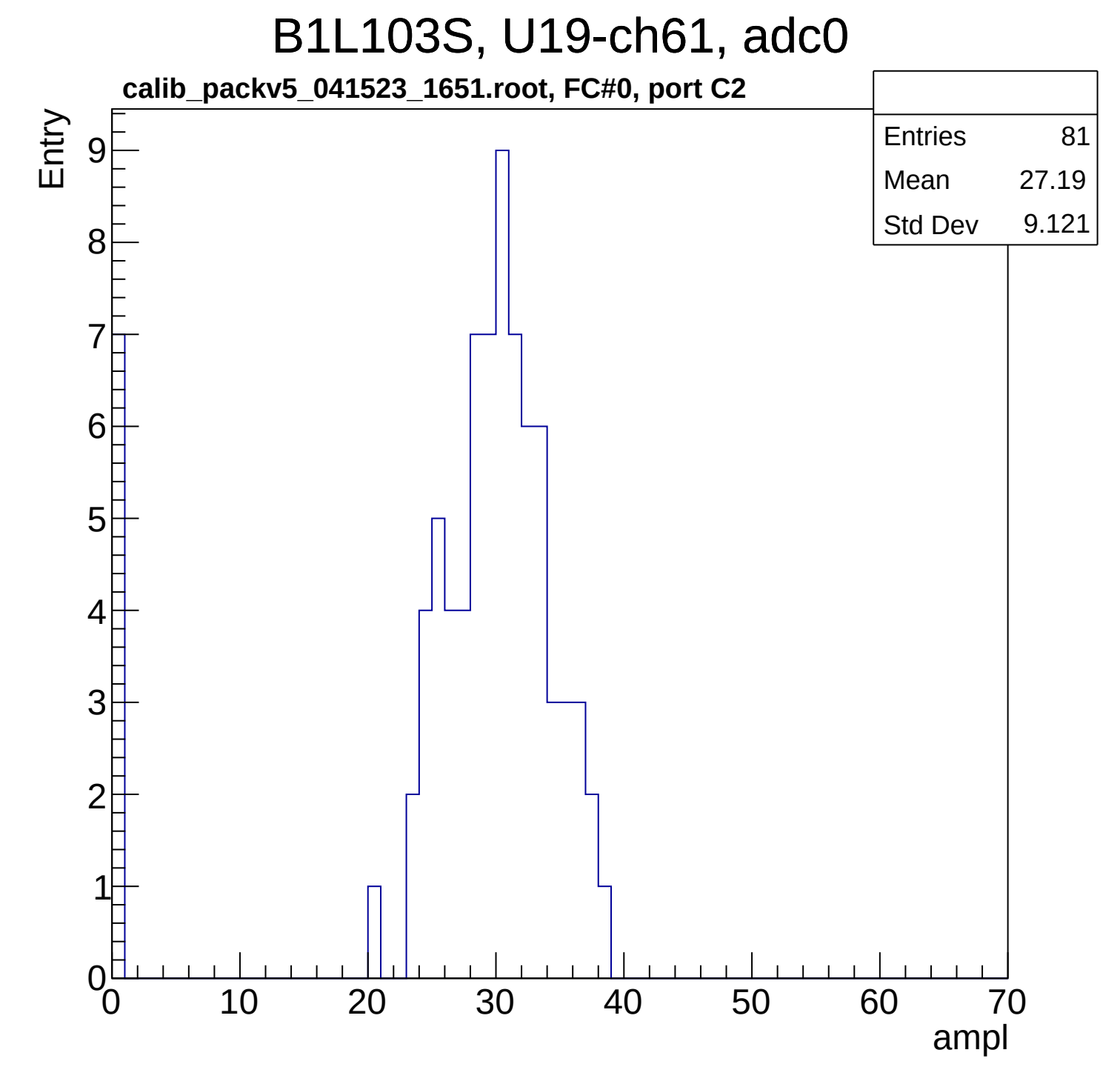
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch60, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.714
Std Dev 17.62
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch61, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 27.19
Std Dev 9.121
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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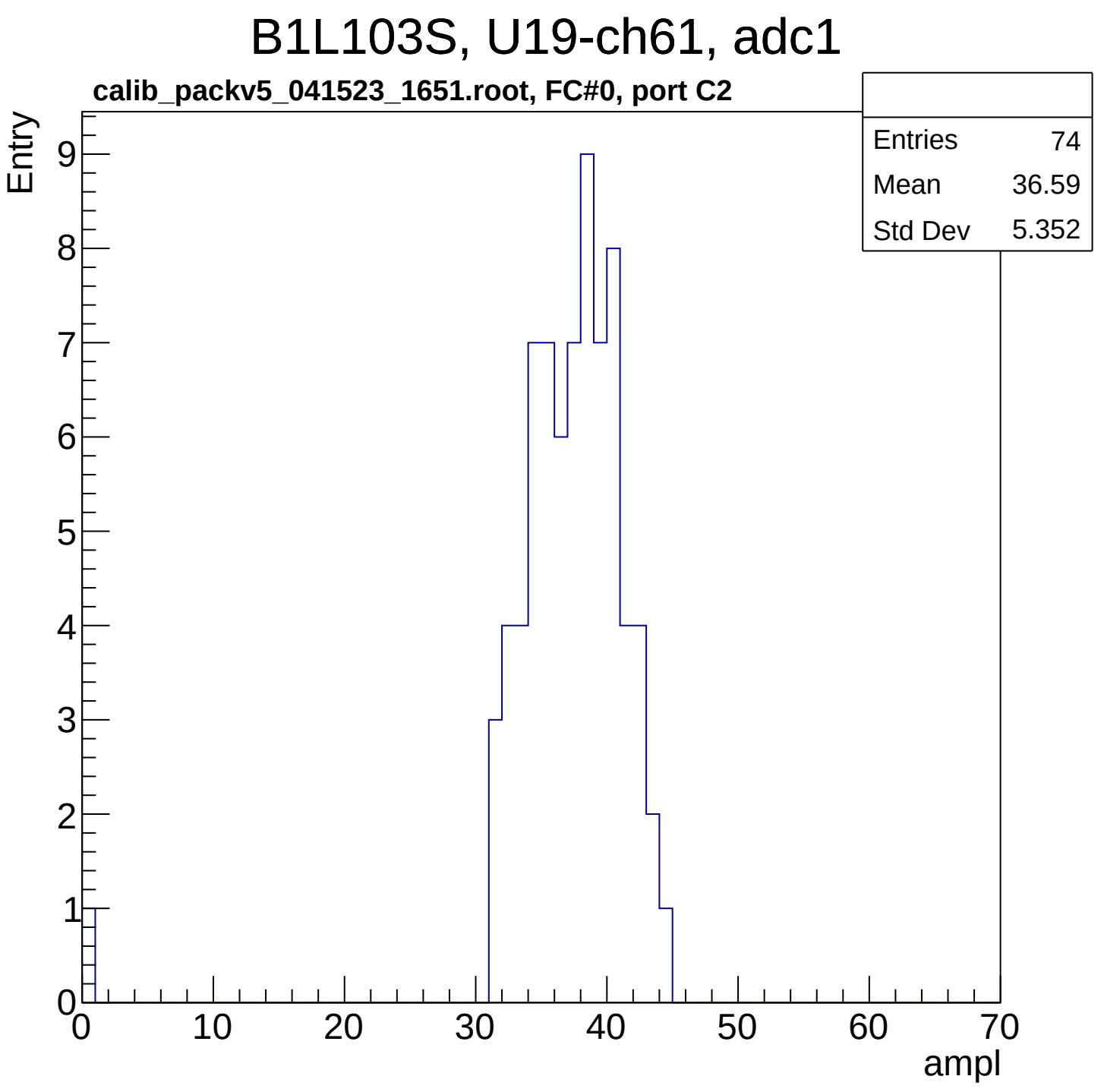
40
50
60
70


B1L103S, U19-ch61, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 36.59
Std Dev 5.352
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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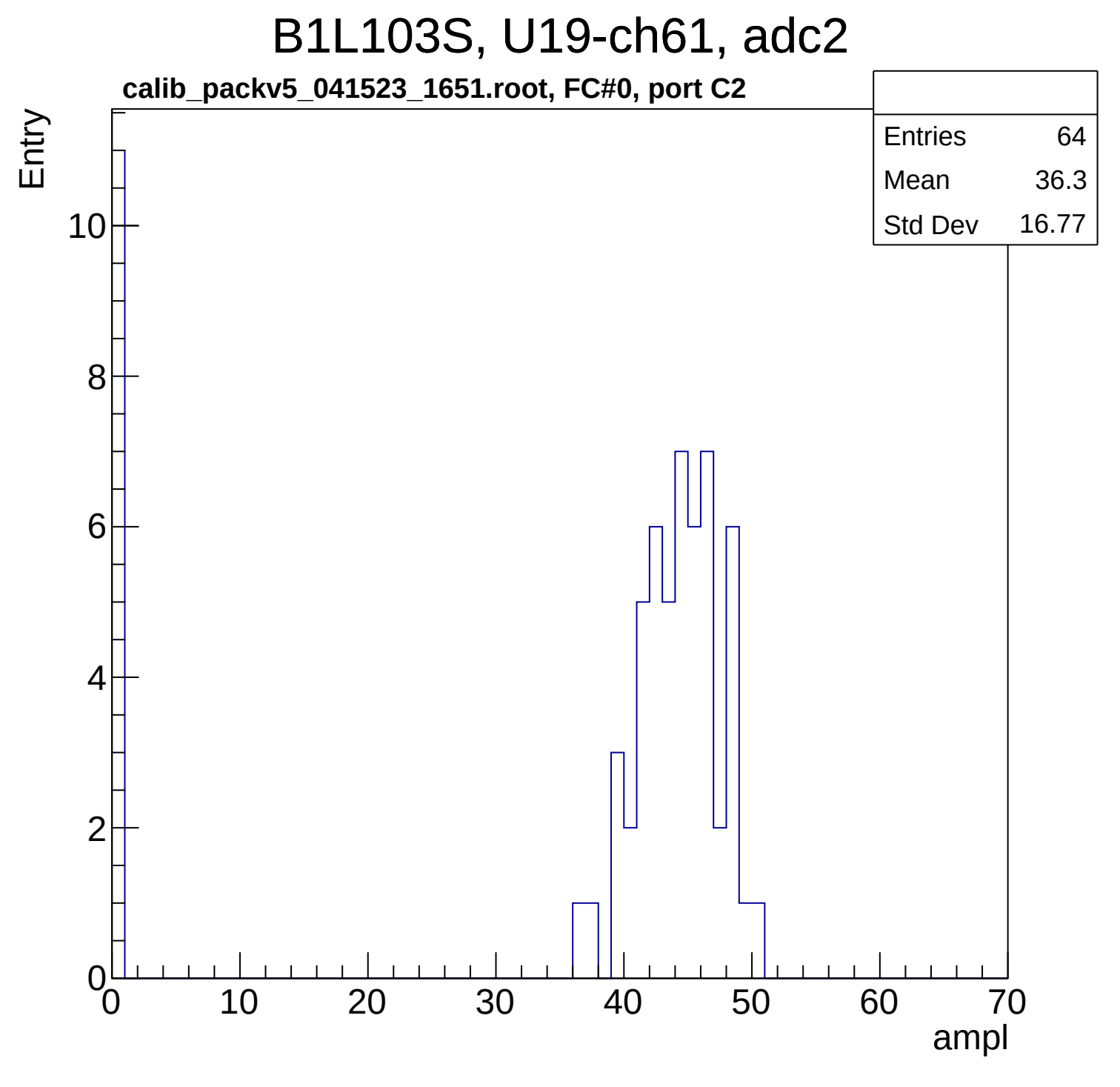
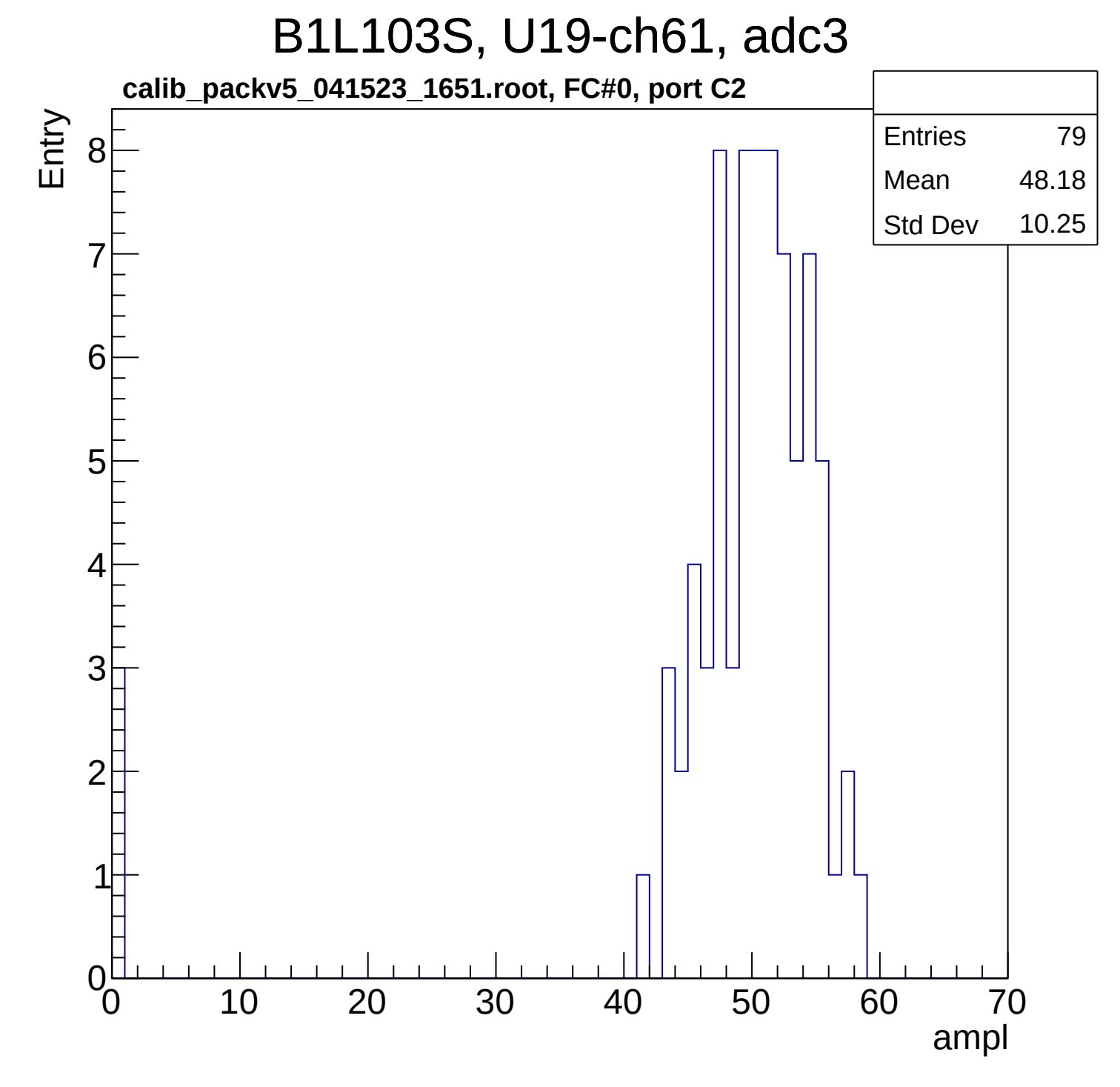
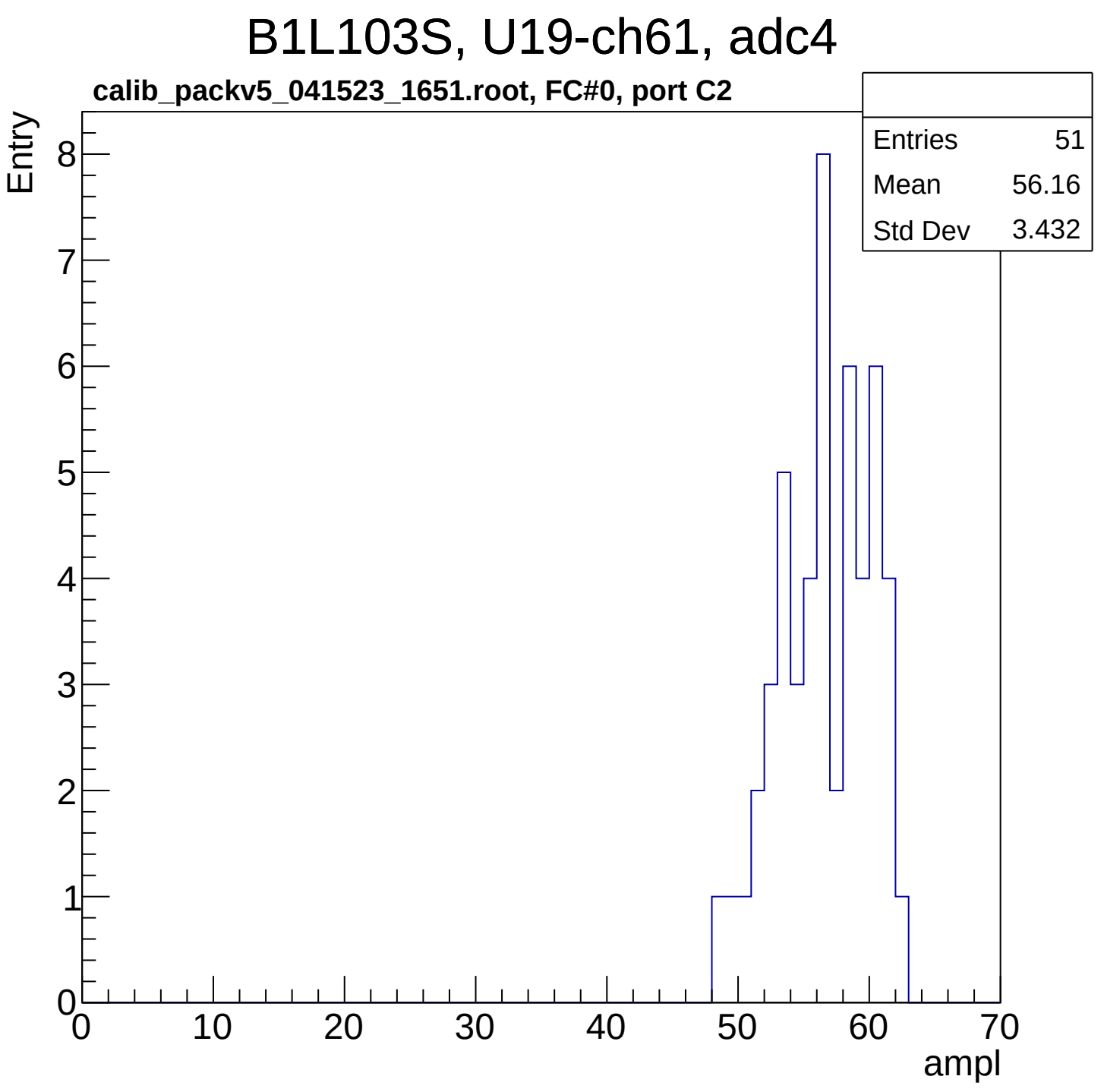
40
50
60
70


B1L103S, U19-ch61, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 36.3
Std Dev 16.77
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U19-ch61, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 48.18
Std Dev 10.25
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch61, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 56.16
Std Dev 3.432
Entry
ampl
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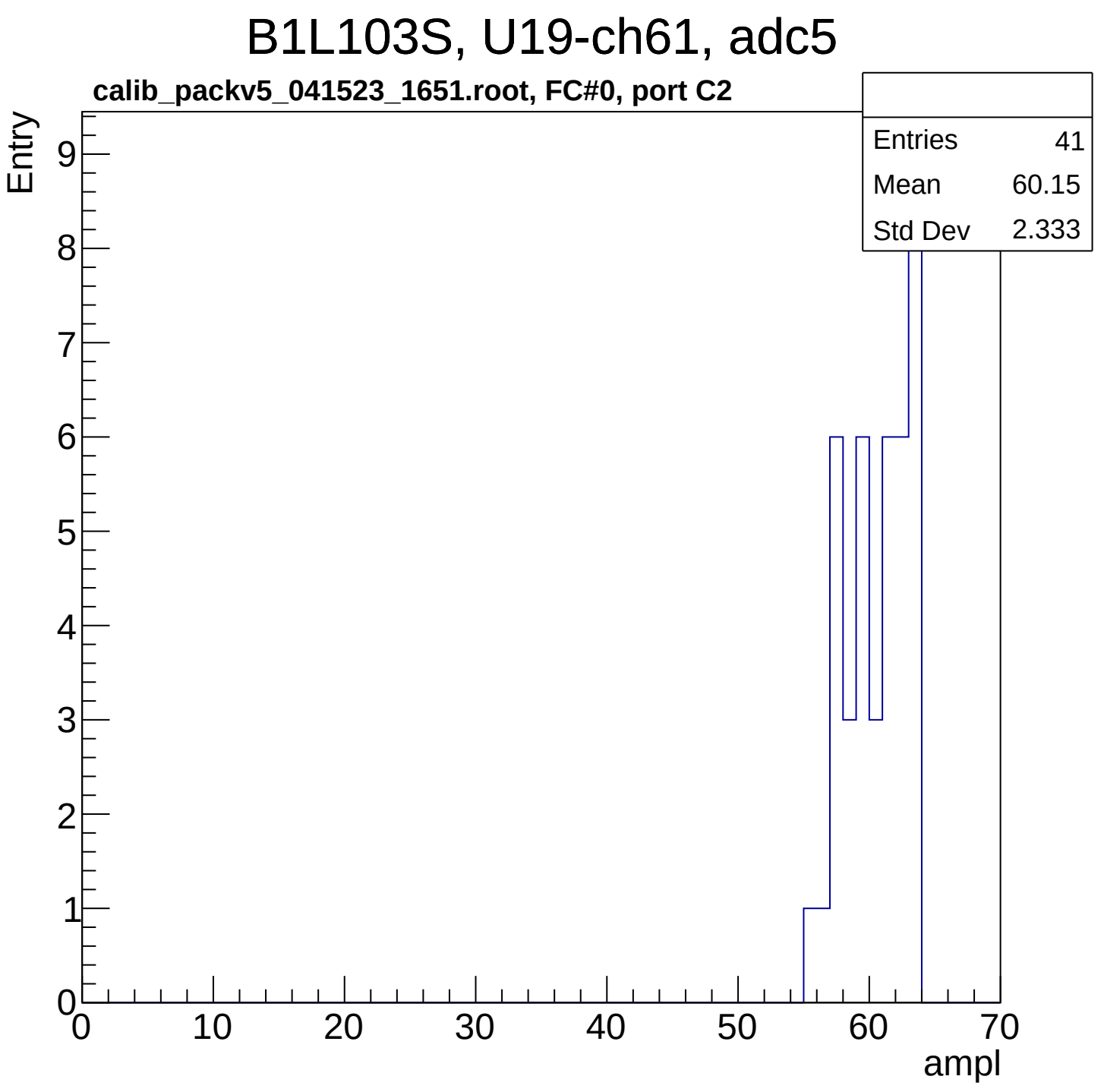
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch61, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 60.15
Std Dev 2.333
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
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40
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60
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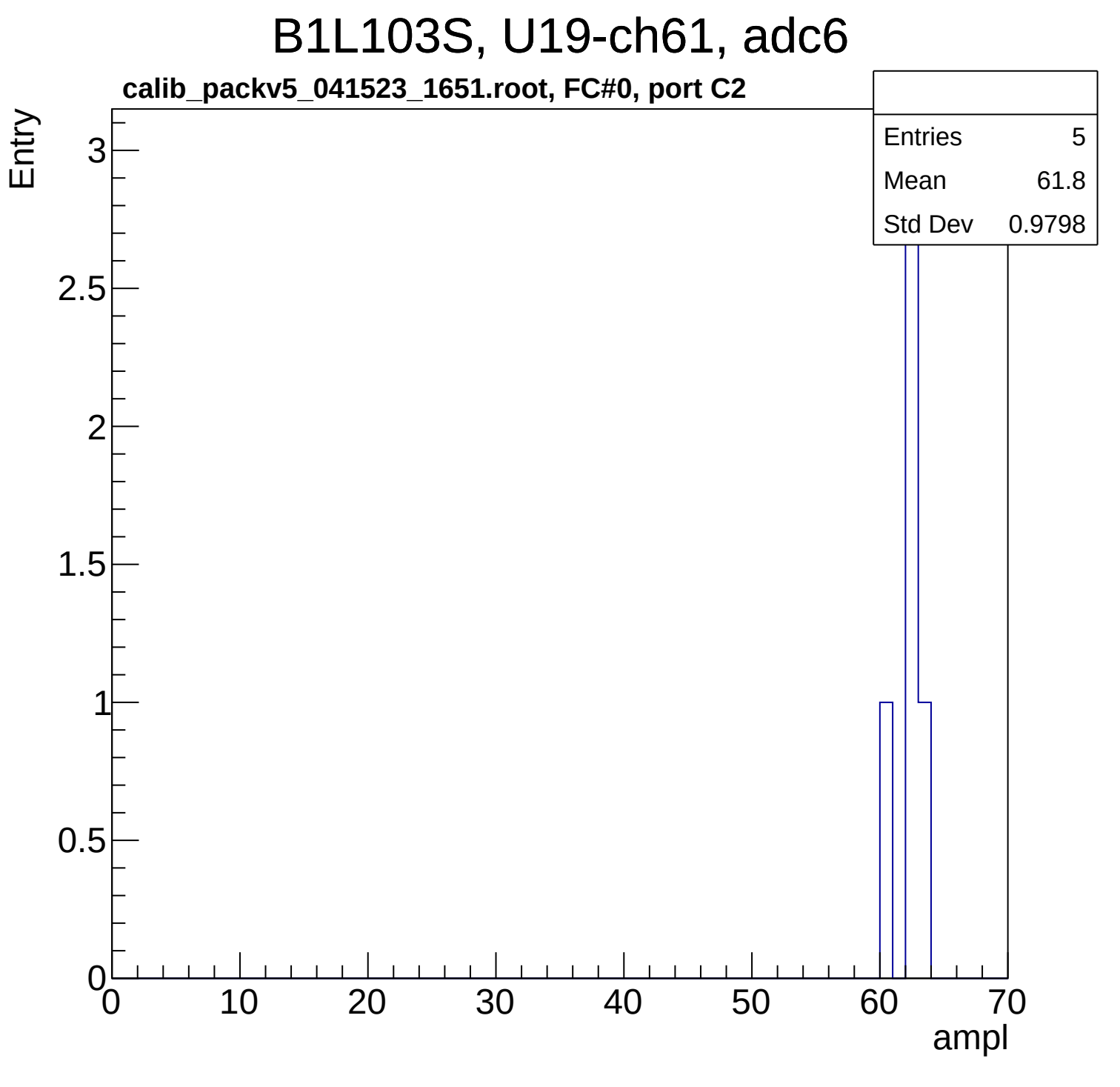
B1L103S, U19-ch61, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 61.8
Std Dev 0.9798
Entry
ampl
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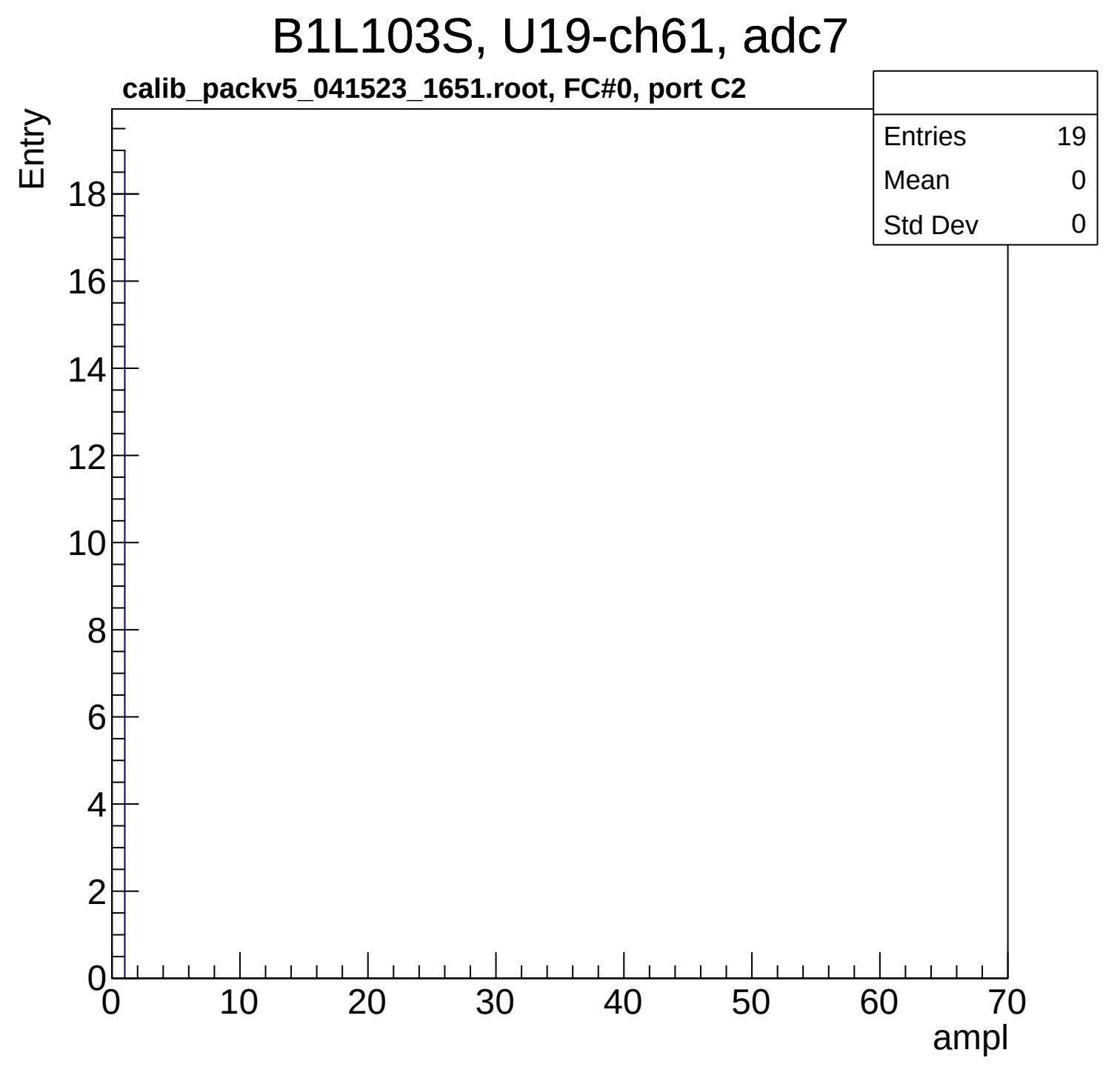
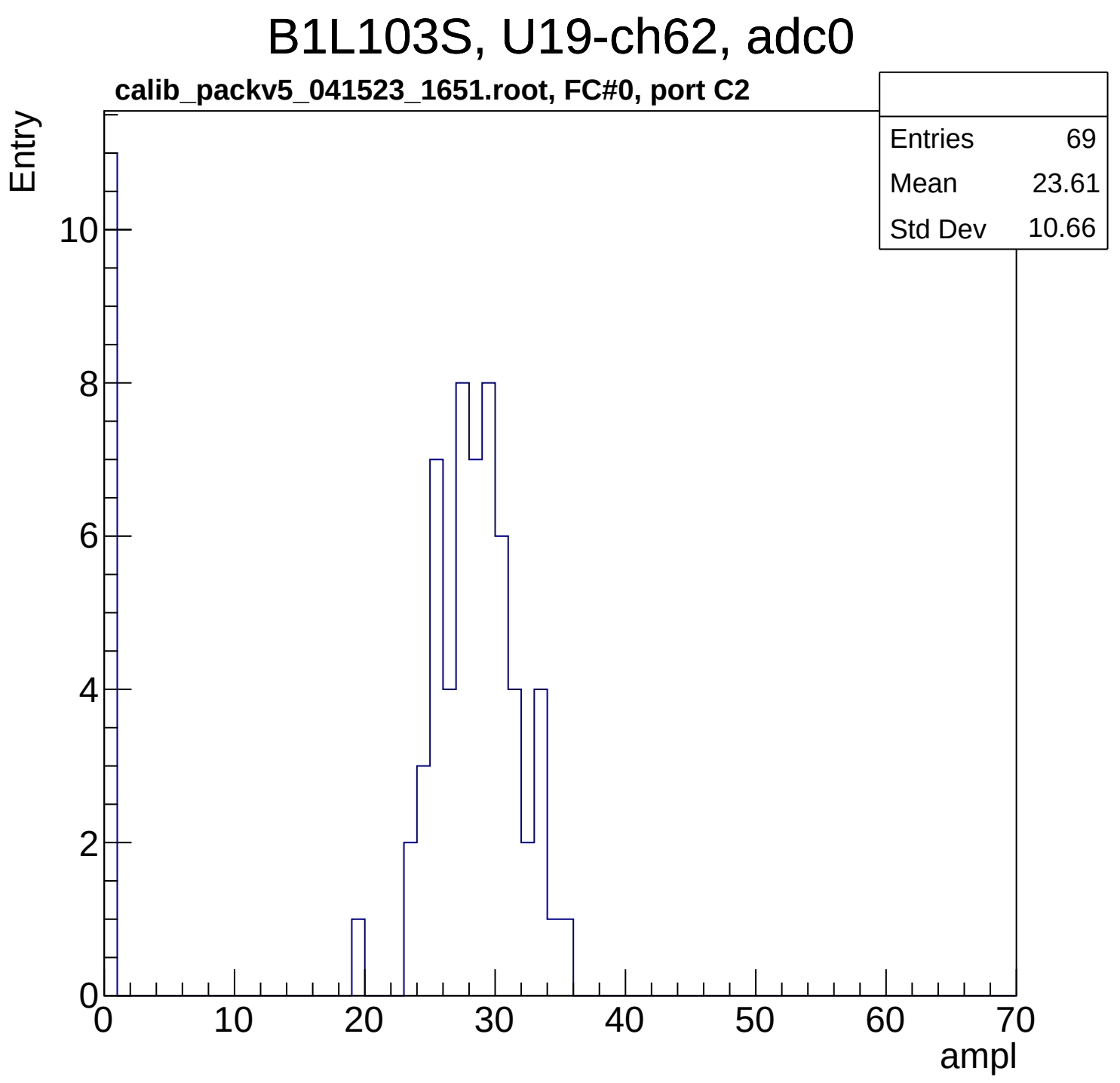
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U19-ch61, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch62, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 23.61
Std Dev 10.66
Entry
0
2
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6
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10
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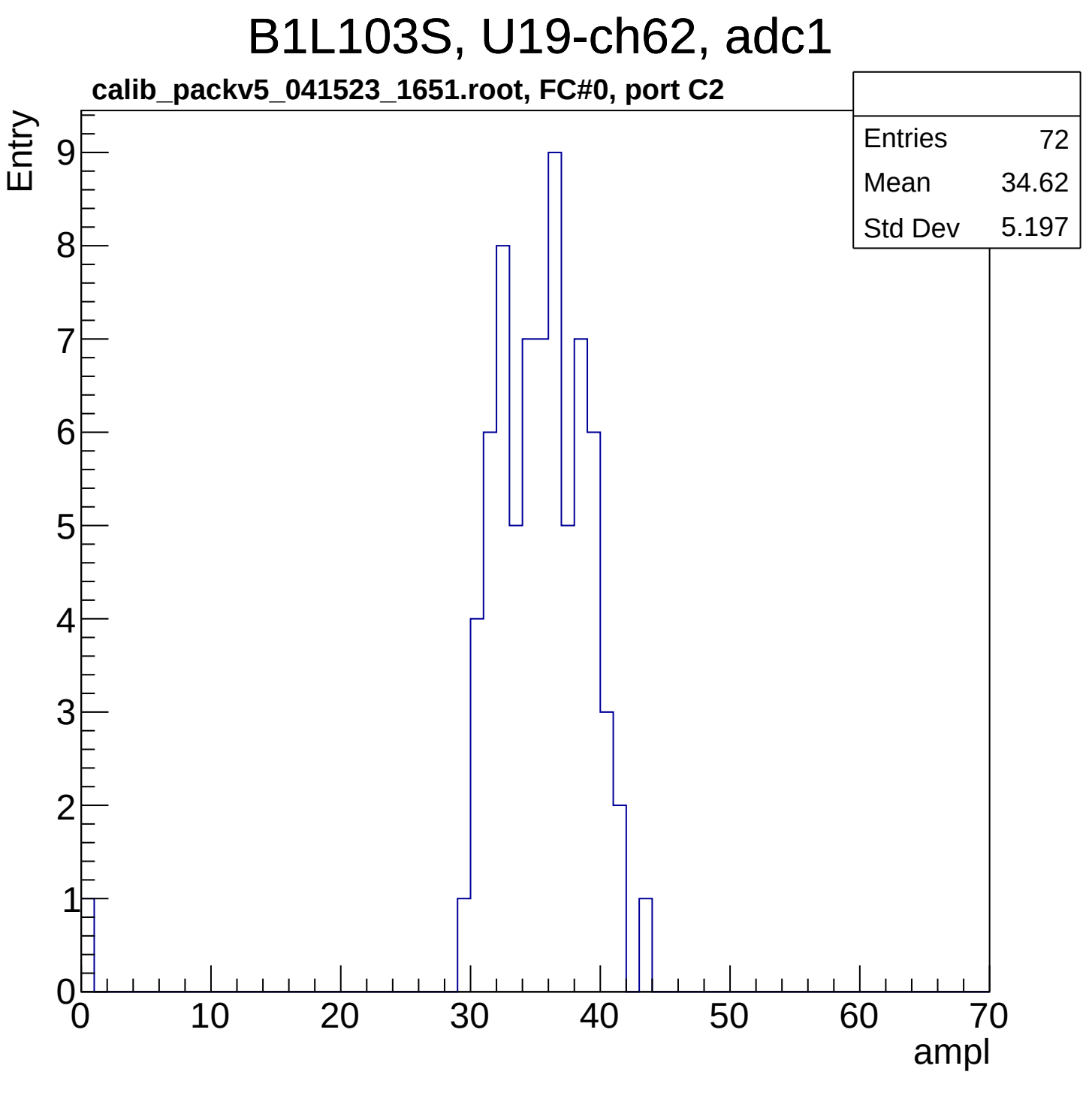
ampl


B1L103S, U19-ch62, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 34.62
Std Dev 5.197
Entry
ampl
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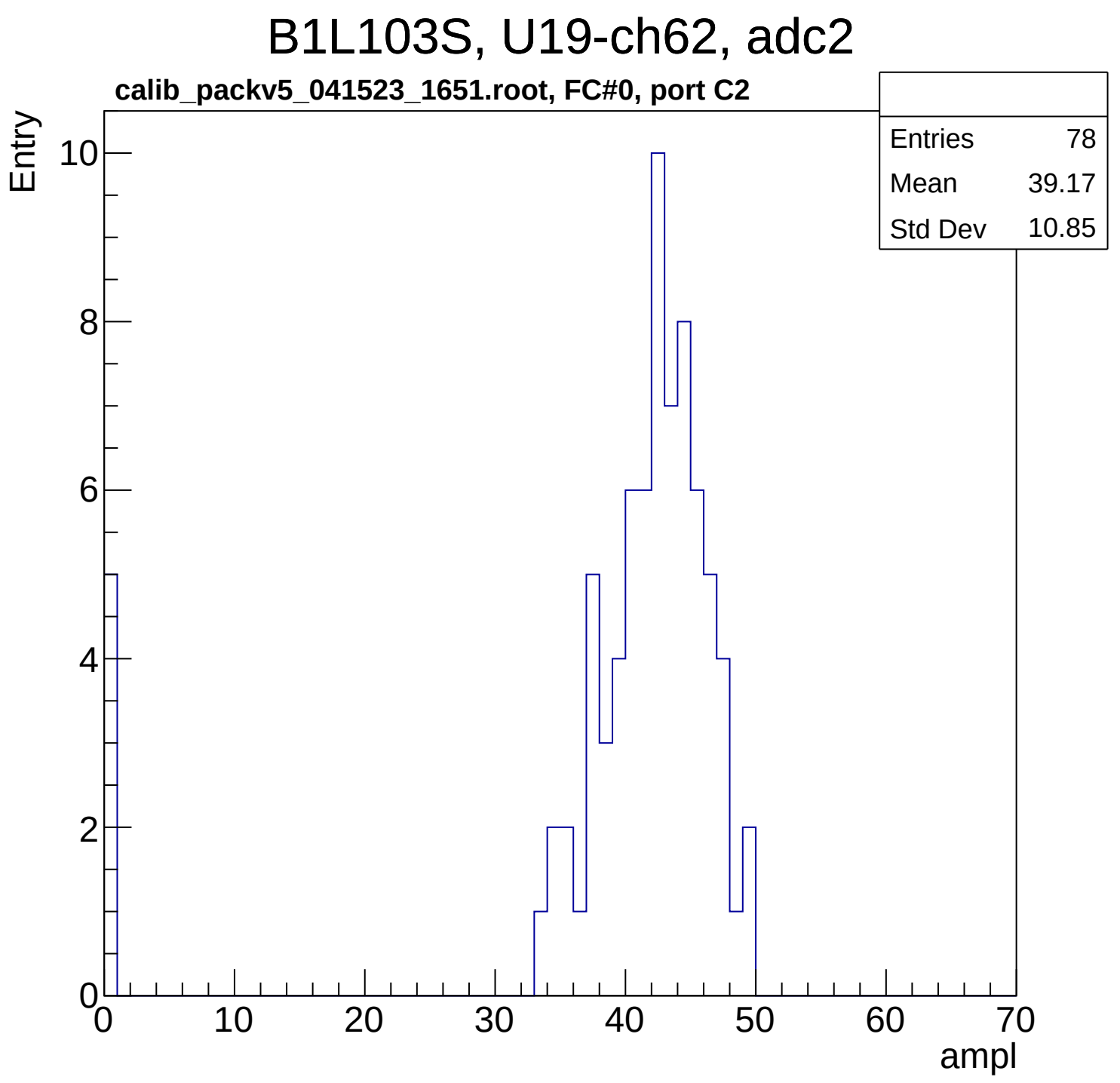
B1L103S, U19-ch62, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 39.17
Std Dev 10.85
Entry
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2
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6
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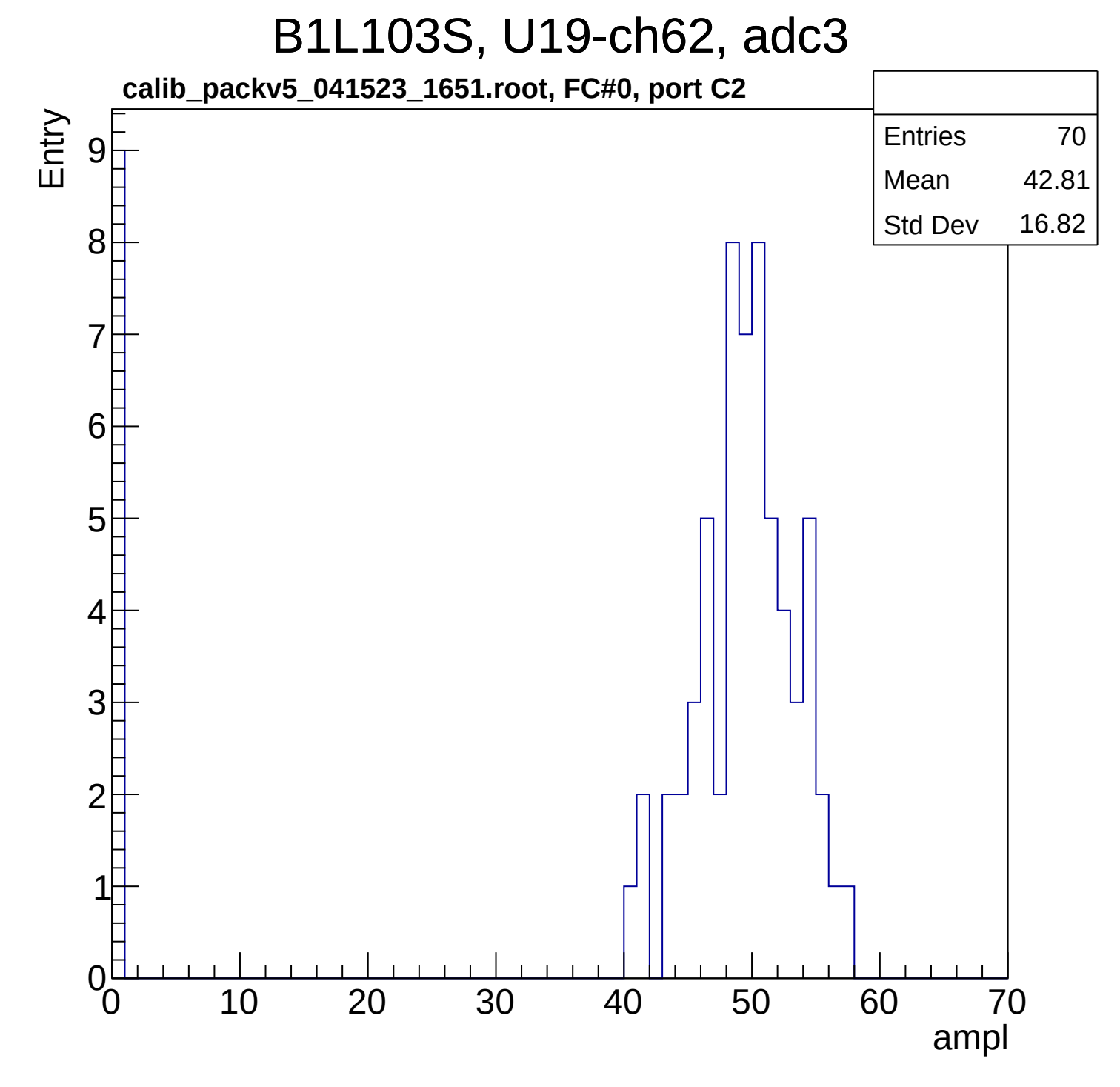
ampl


B1L103S, U19-ch62, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 42.81
Std Dev 16.82
Entry
ampl
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0
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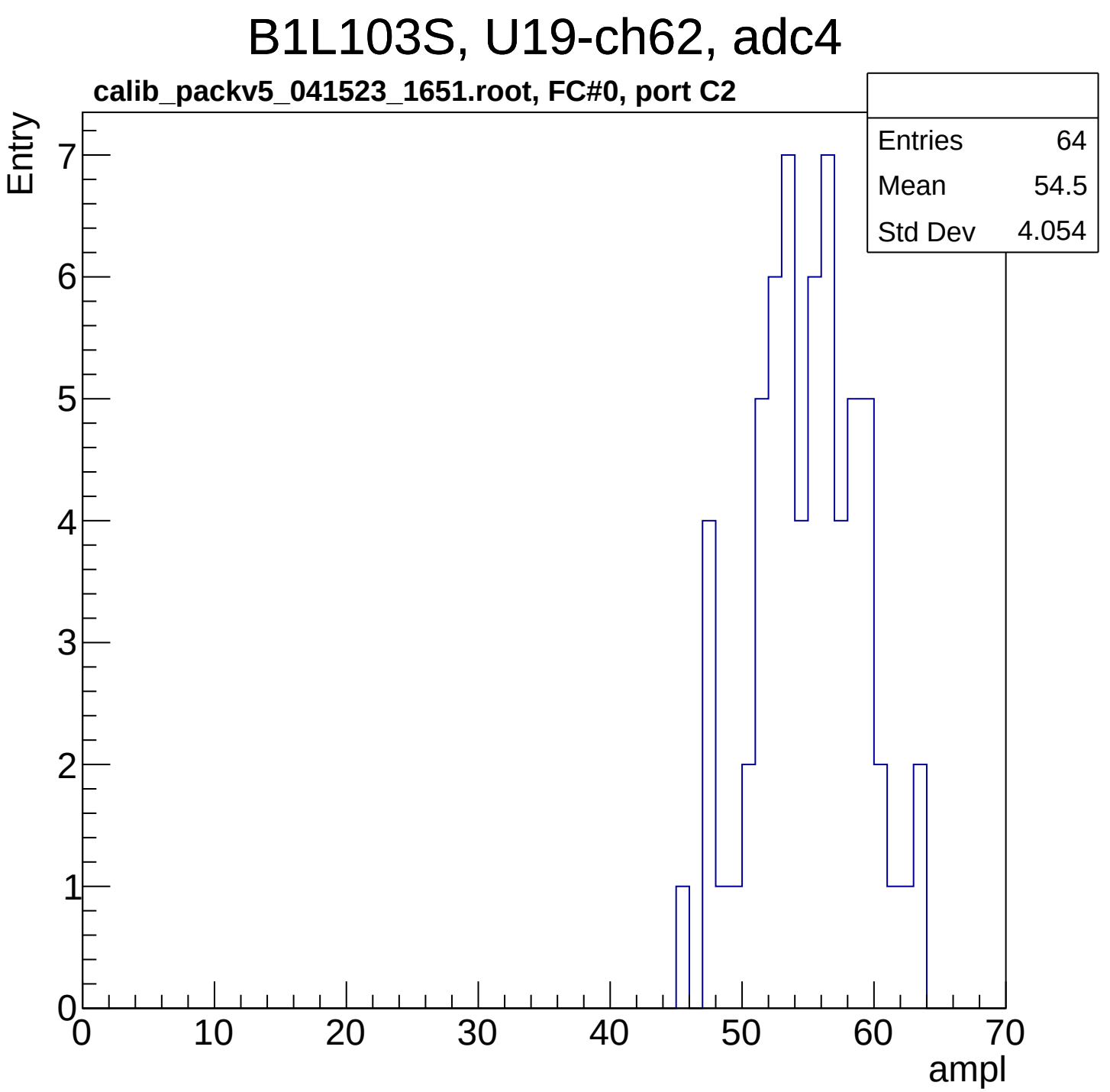
B1L103S, U19-ch62, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 54.5
Std Dev 4.054
Entry
ampl
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1
2
3
4
5
6
7
0
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20
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40
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60
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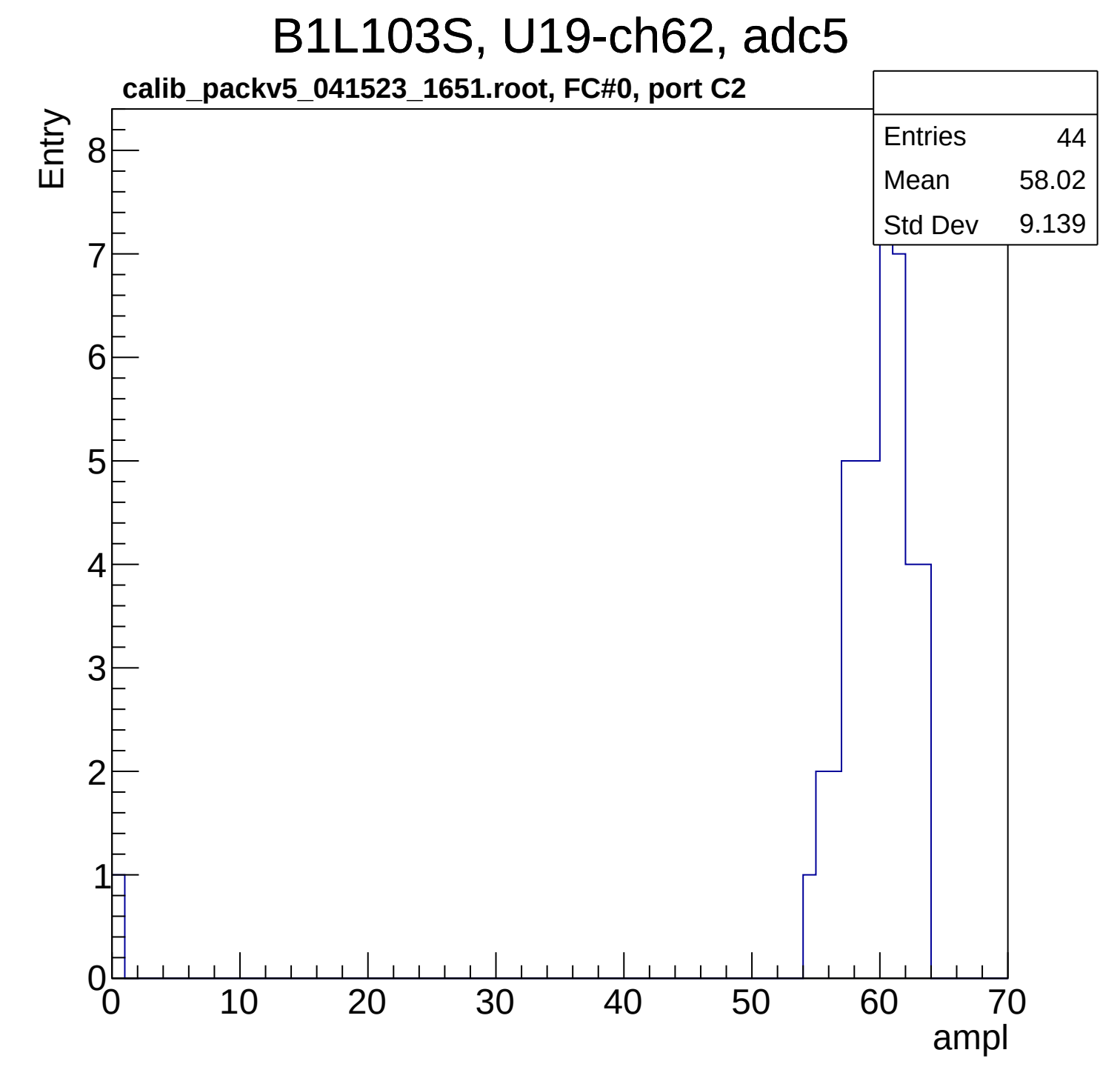
B1L103S, U19-ch62, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 58.02
Std Dev 9.139
Entry
ampl
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3
4
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7
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0
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40
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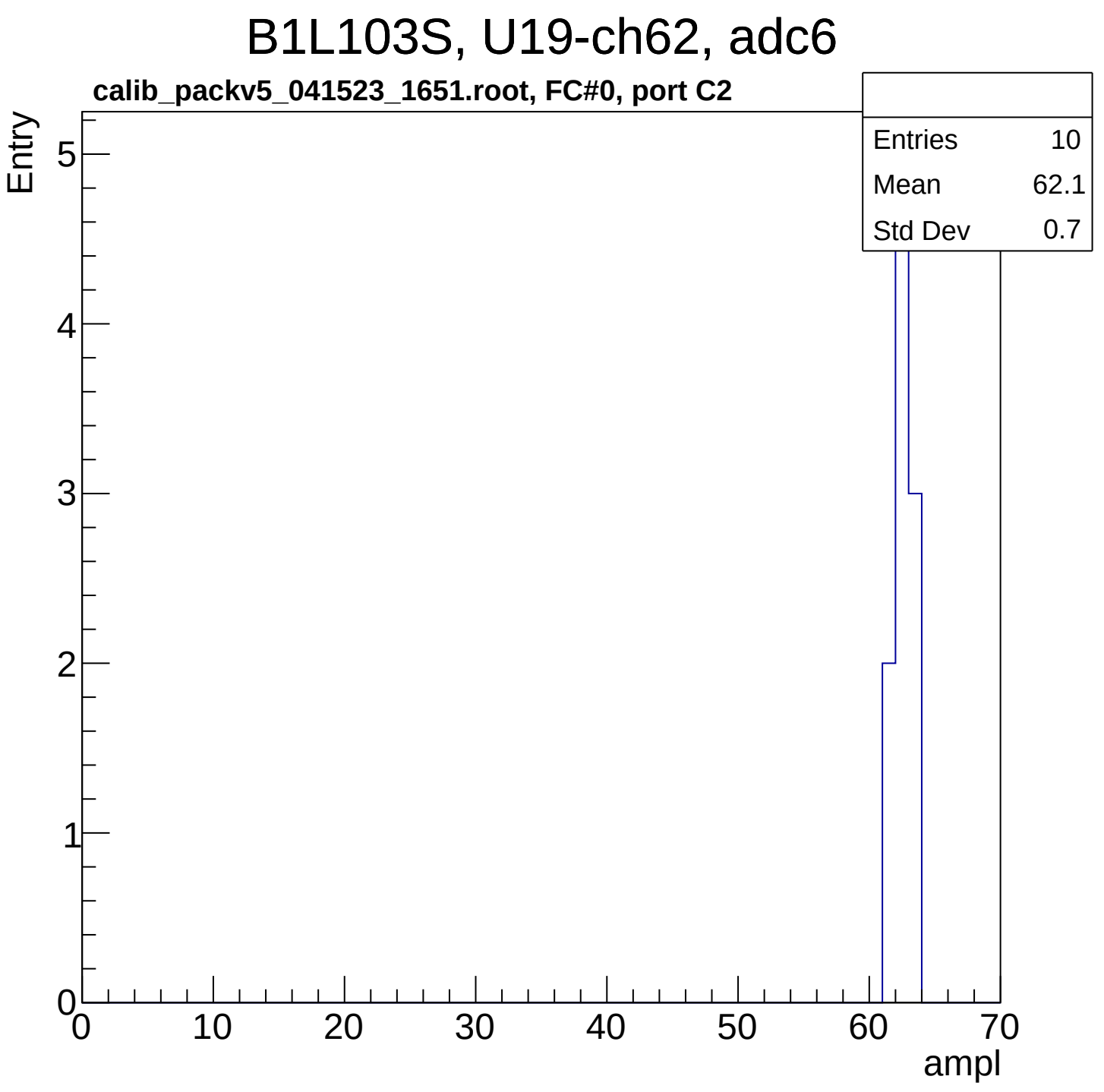
B1L103S, U19-ch62, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 62.1
Std Dev 0.7
Entry
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3
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5
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30
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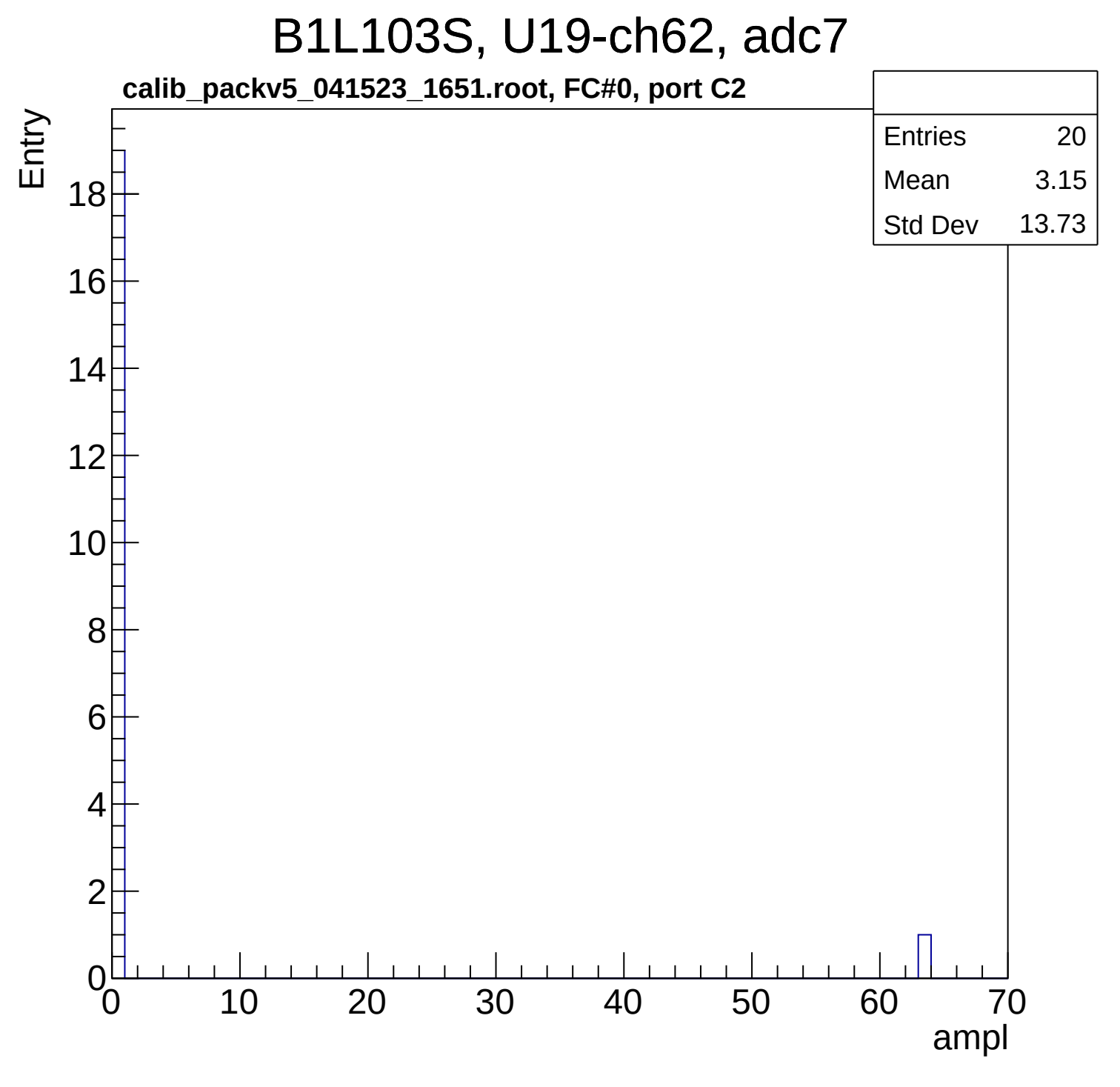
50
60
70
ampl


B1L103S, U19-ch62, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
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10
20
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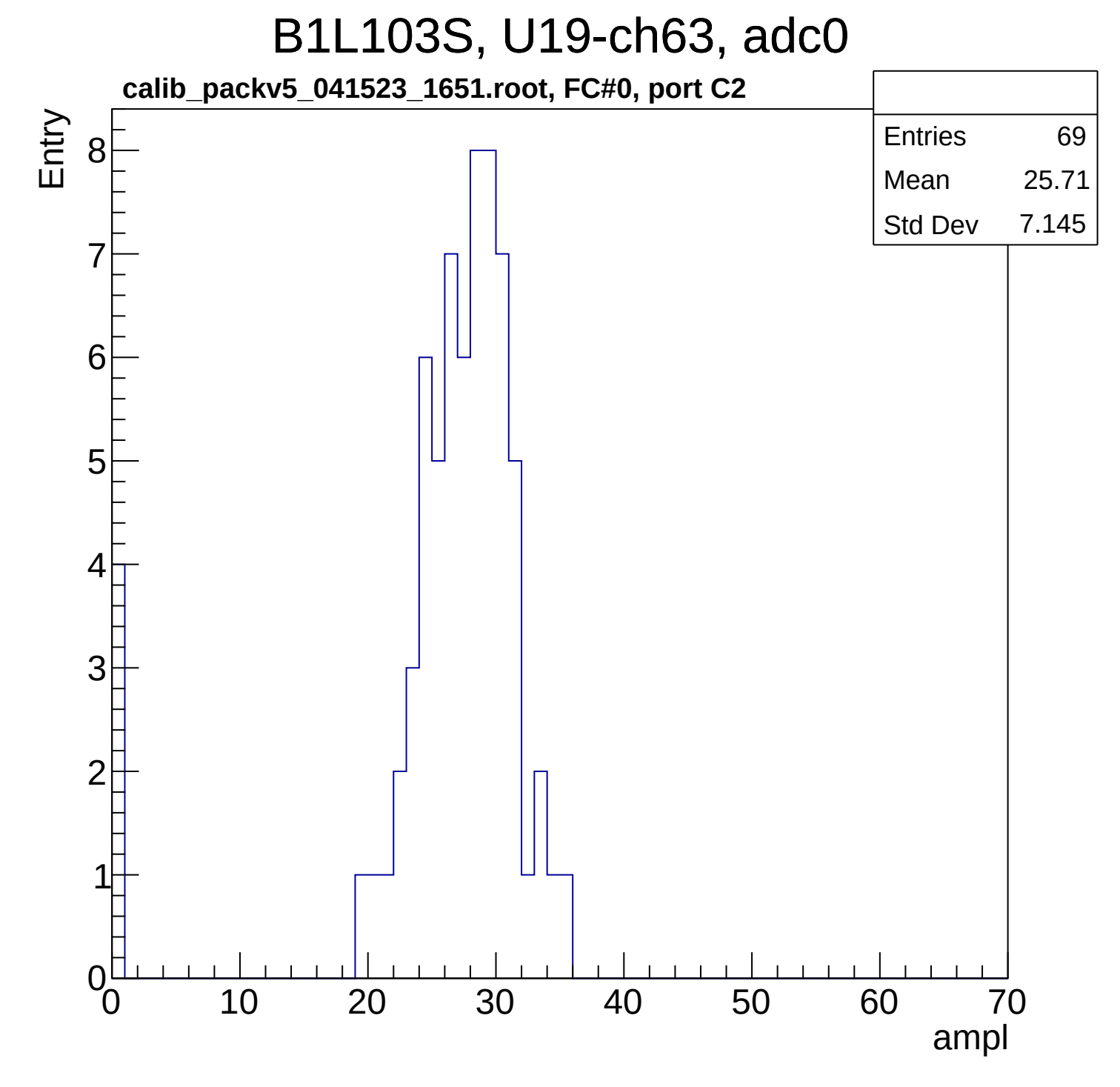
40
50
60
70
ampl


B1L103S, U19-ch63, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 25.71
Std Dev 7.145
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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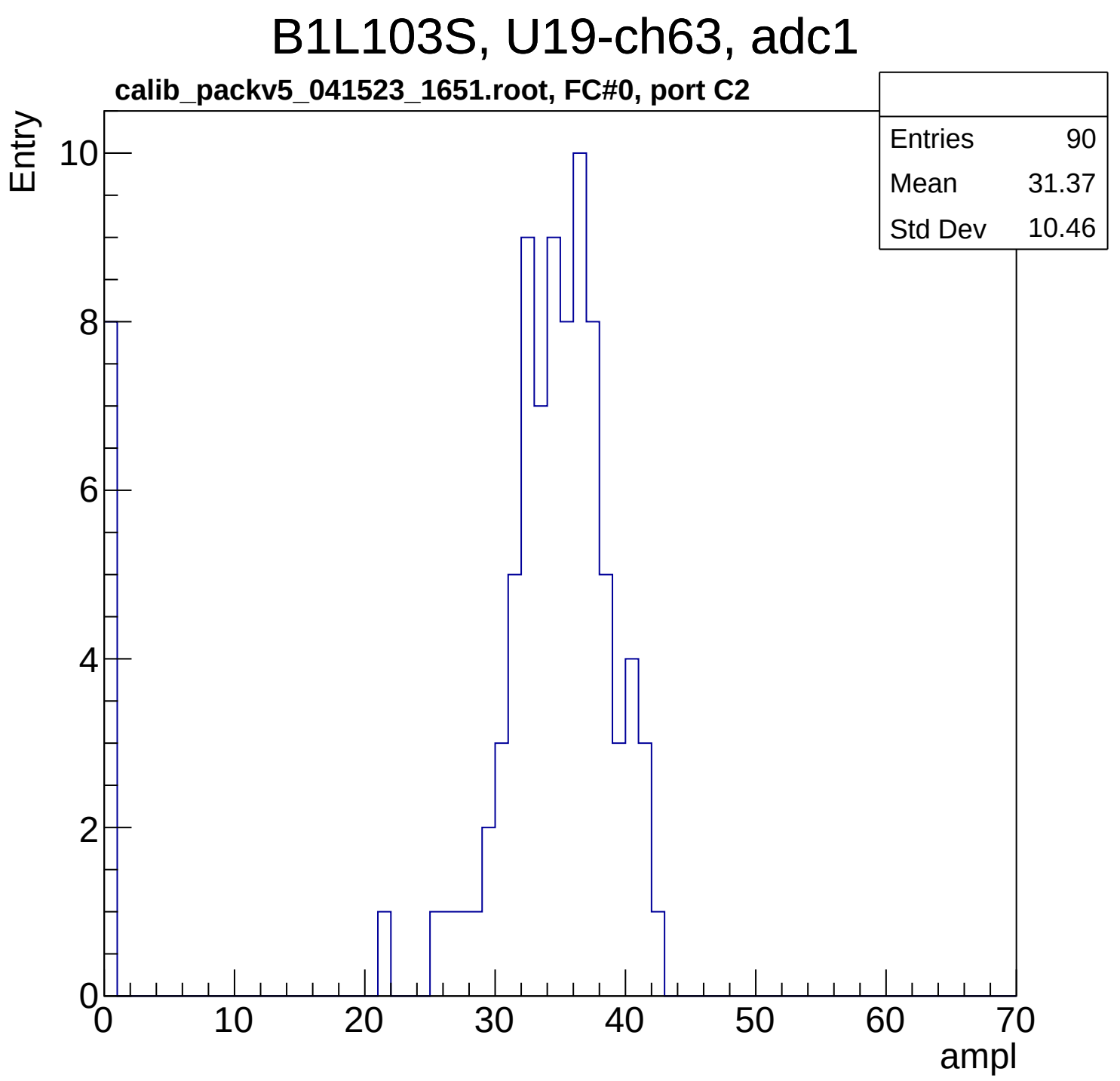
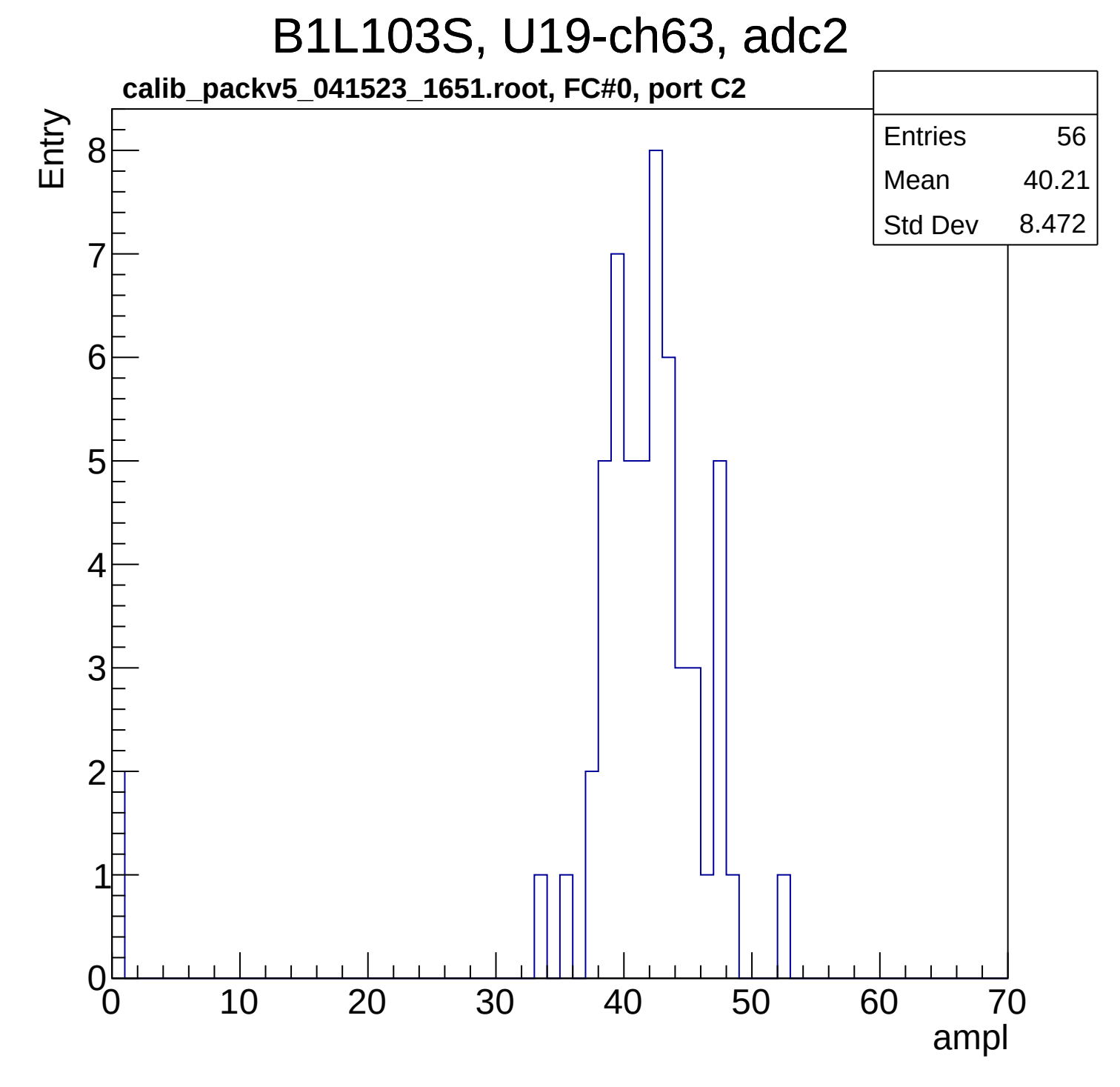
40
50
60
70


B1L103S, U19-ch63, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 31.37
Std Dev 10.46
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U19-ch63, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 40.21
Std Dev 8.472
Entry
ampl
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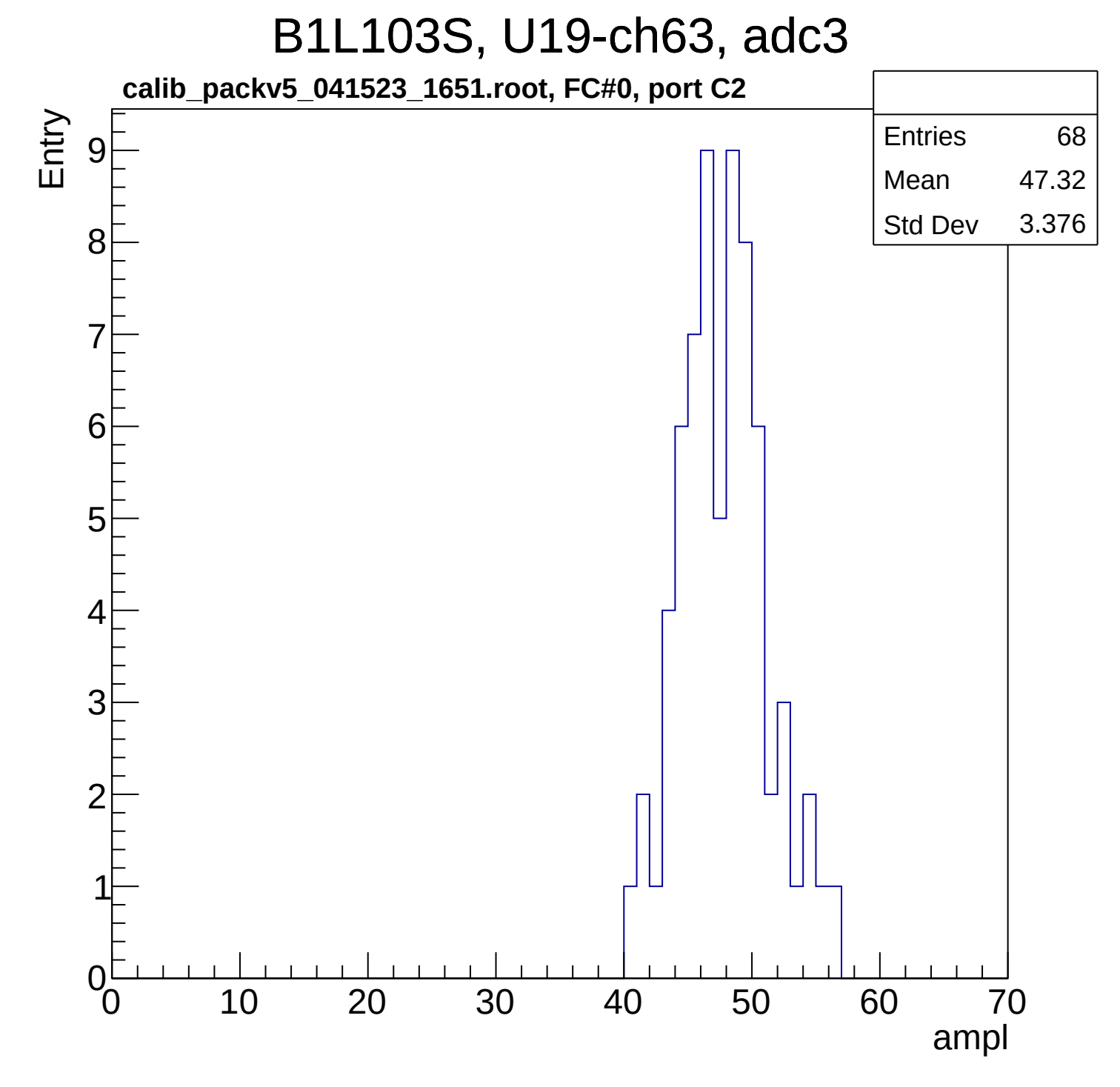
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch63, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 47.32
Std Dev 3.376
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
50
60
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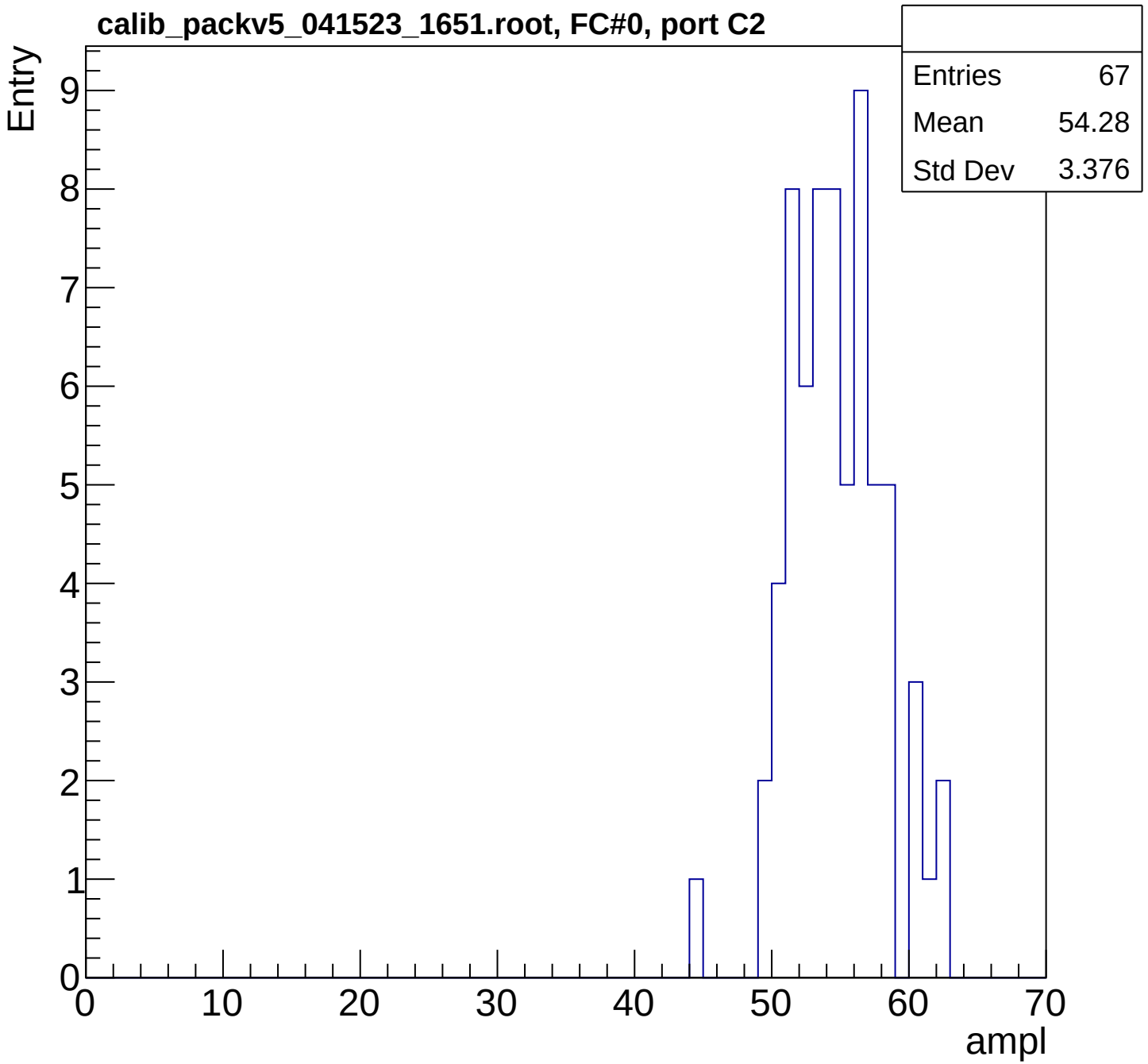
B1L103S, U19-ch63, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 54.28
Std Dev 3.376
Entry
ampl
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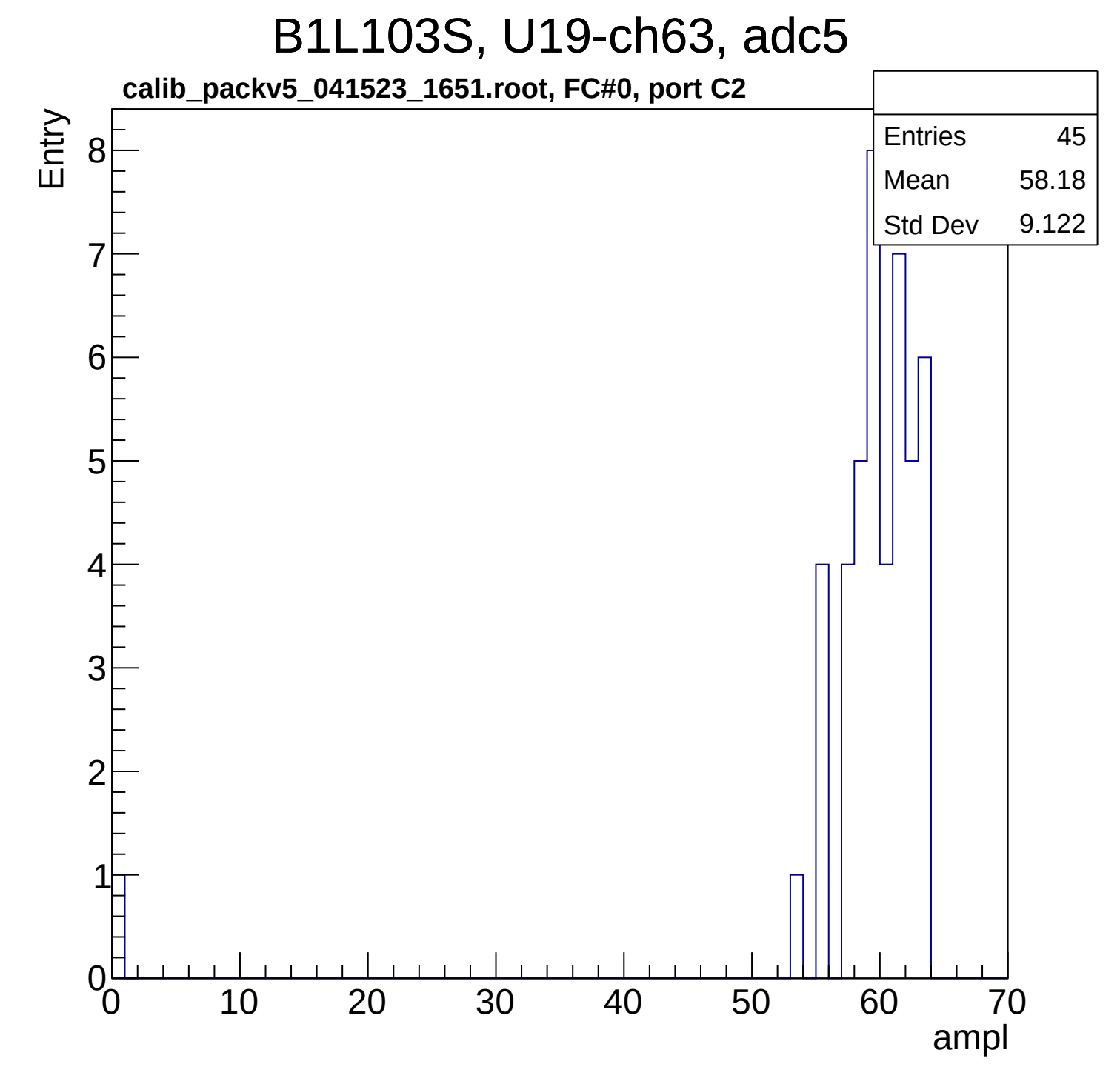
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch63, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 58.18
Std Dev 9.122
Entry
ampl
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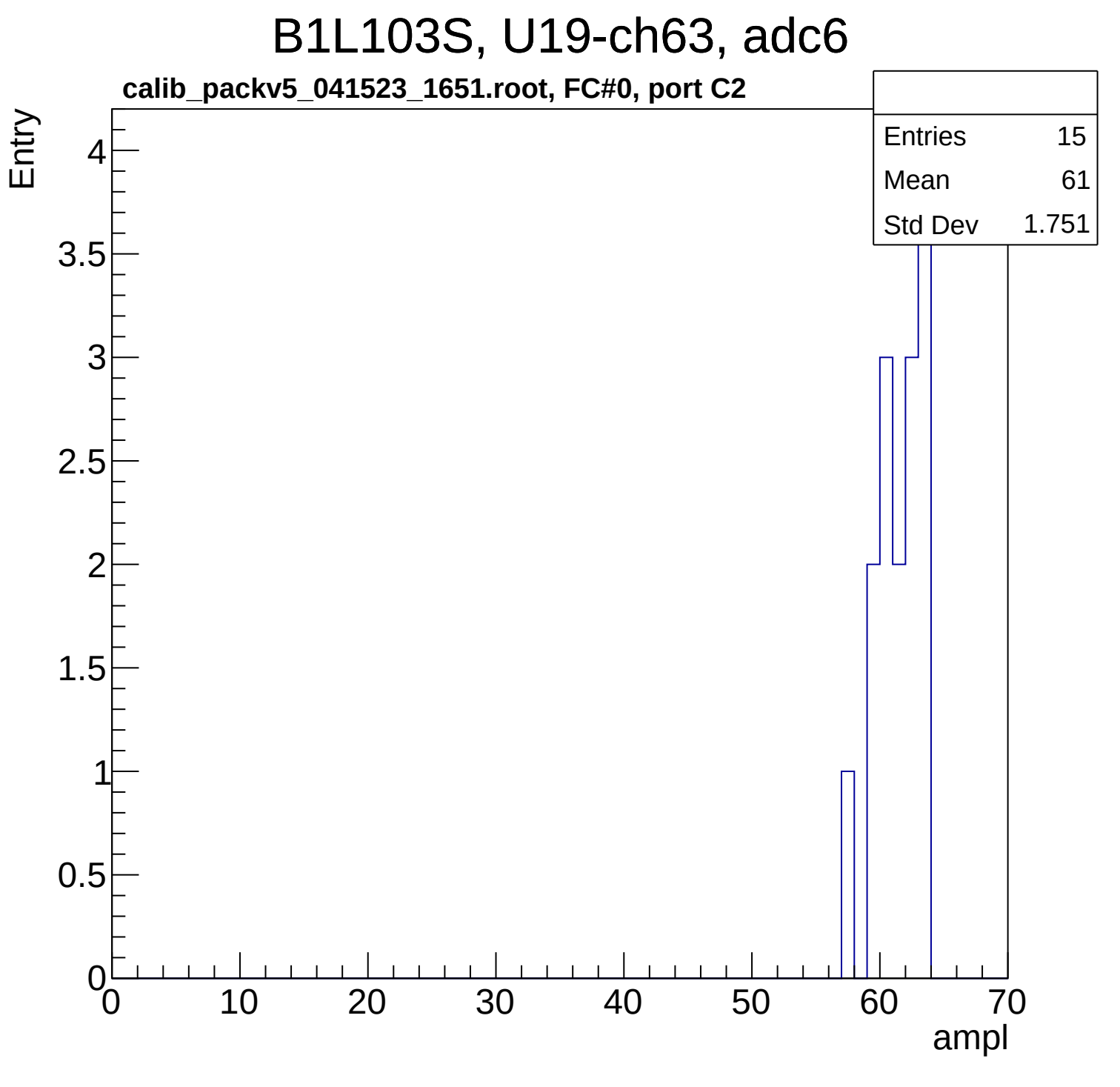
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch63, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 61
Std Dev 1.751
Entry
ampl
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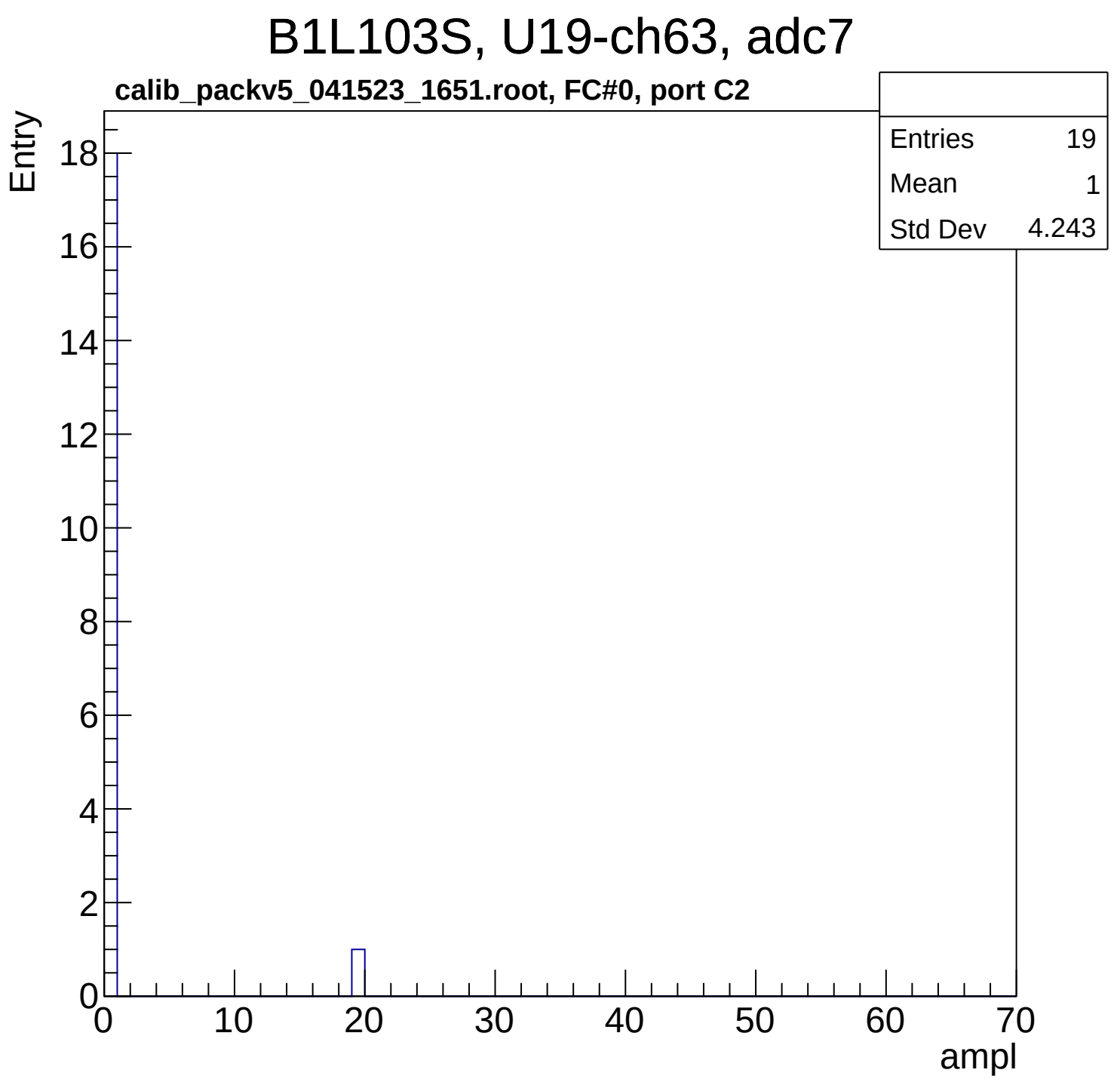
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U19-ch63, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1
Std Dev 4.243
Entry
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6
8
10
12
14
16
18
0
10
20
30
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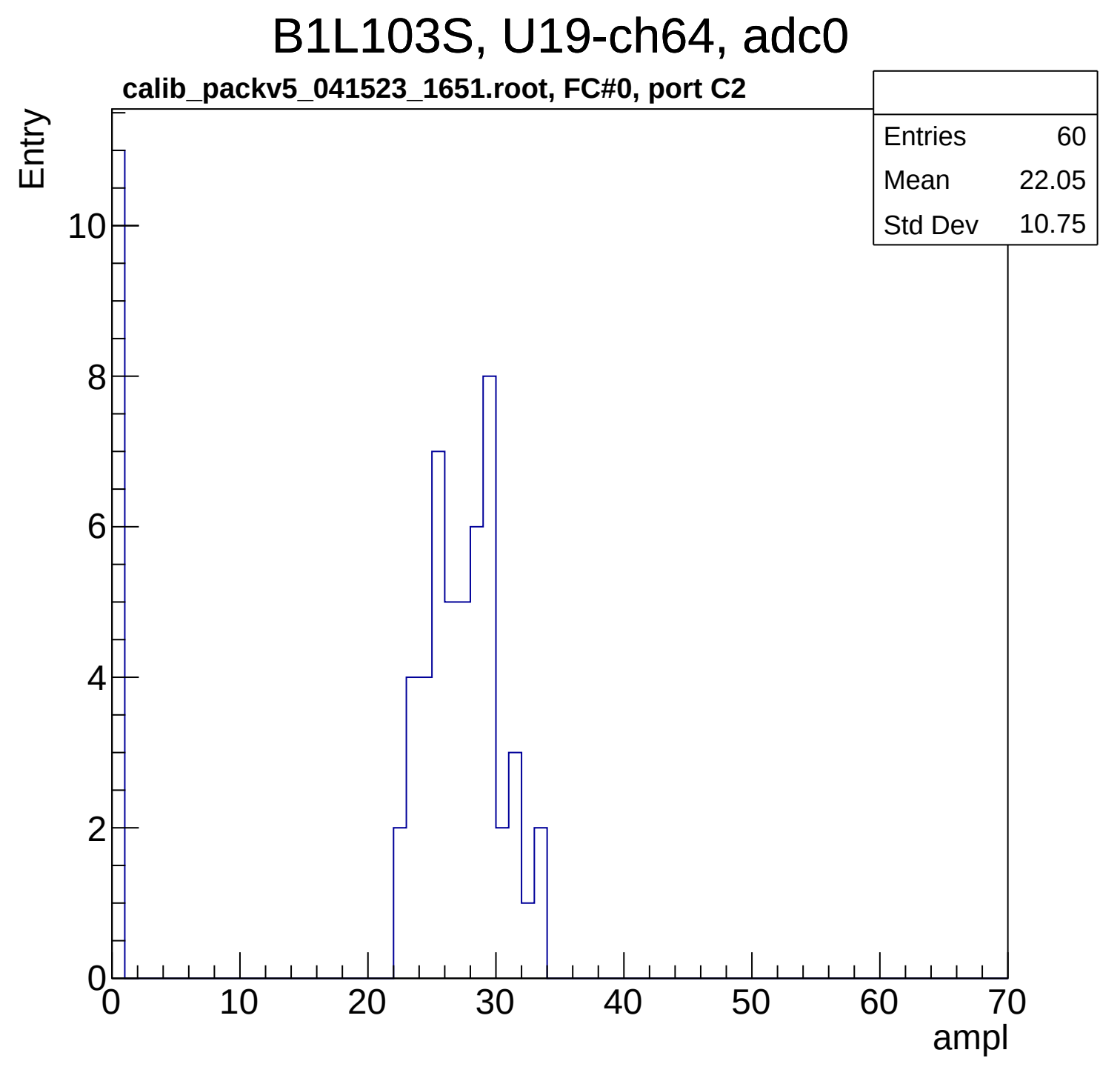
50
60
70
ampl


B1L103S, U19-ch64, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 22.05
Std Dev 10.75
Entry
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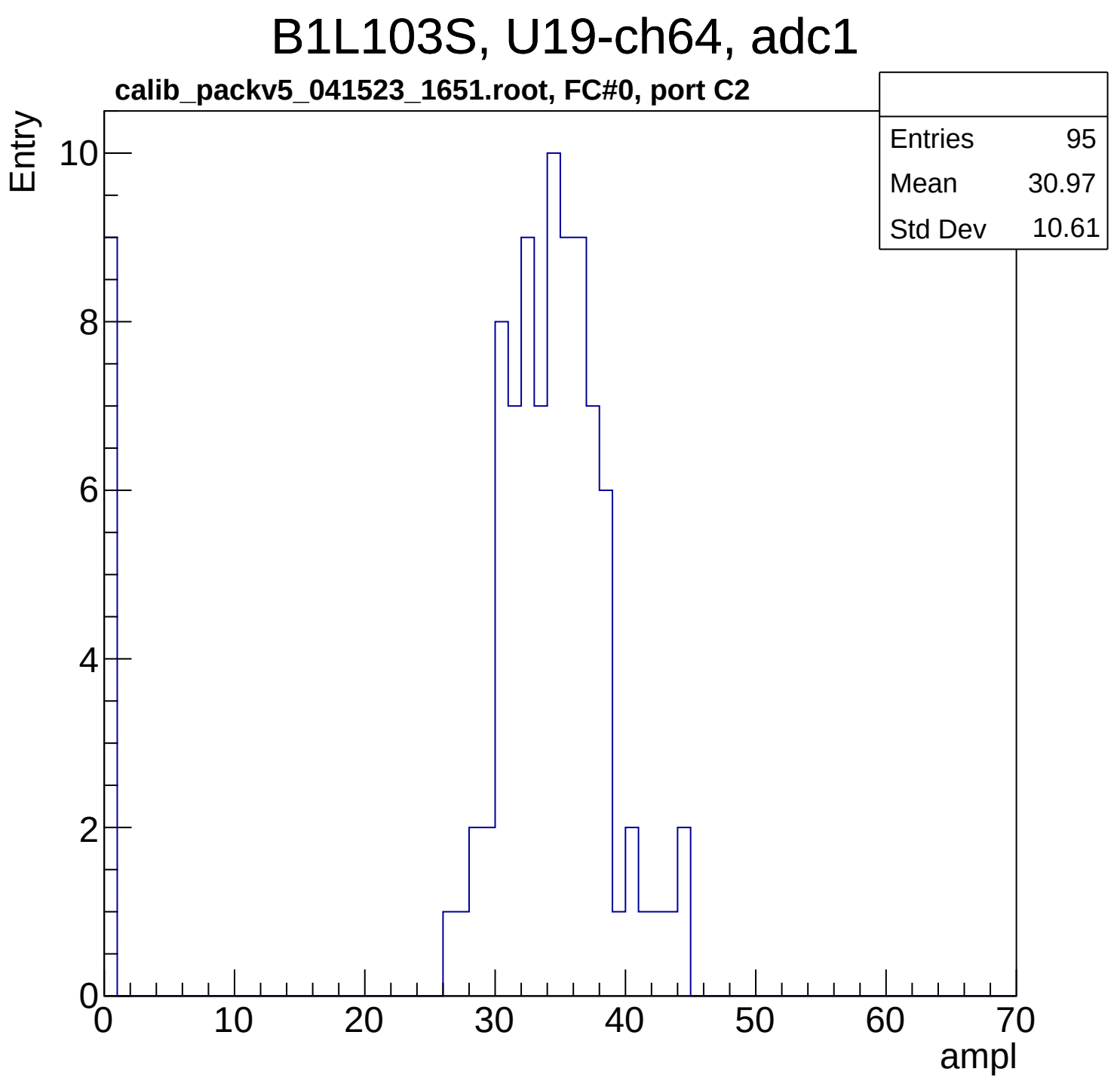
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch64, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 30.97
Std Dev 10.61
Entry
ampl
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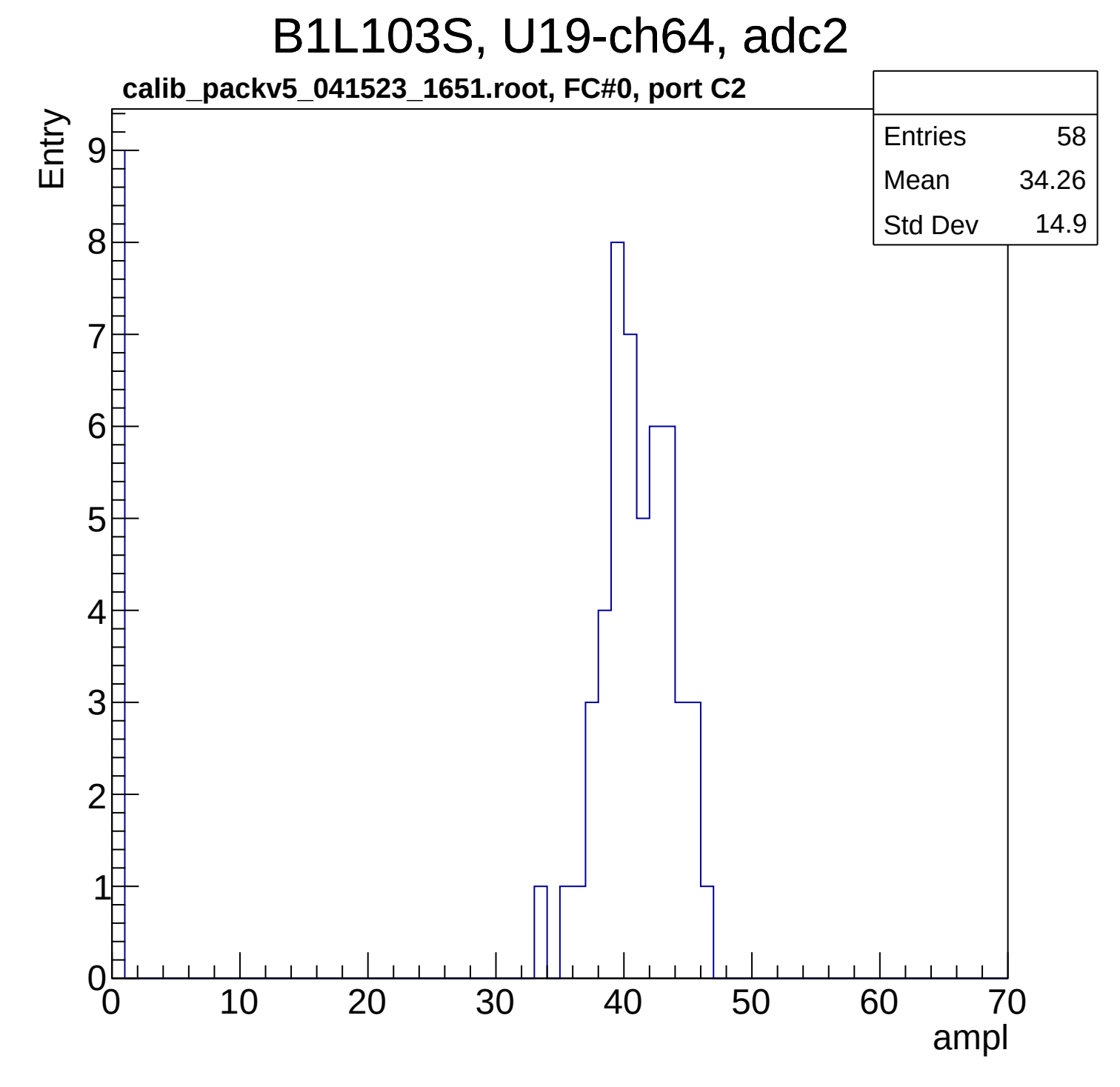
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U19-ch64, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 34.26
Std Dev 14.9
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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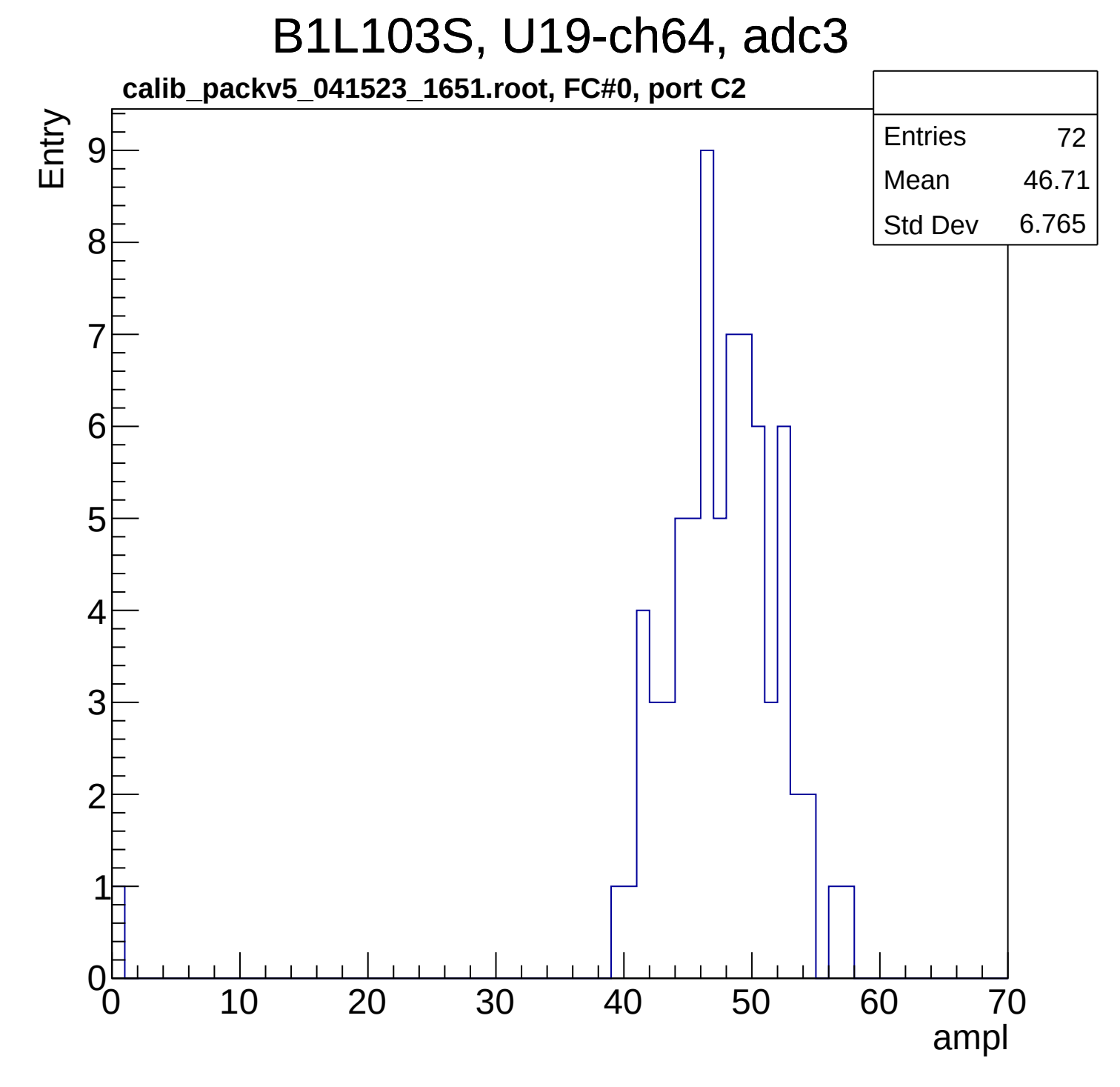
40
50
60
70


B1L103S, U19-ch64, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 46.71
Std Dev 6.765
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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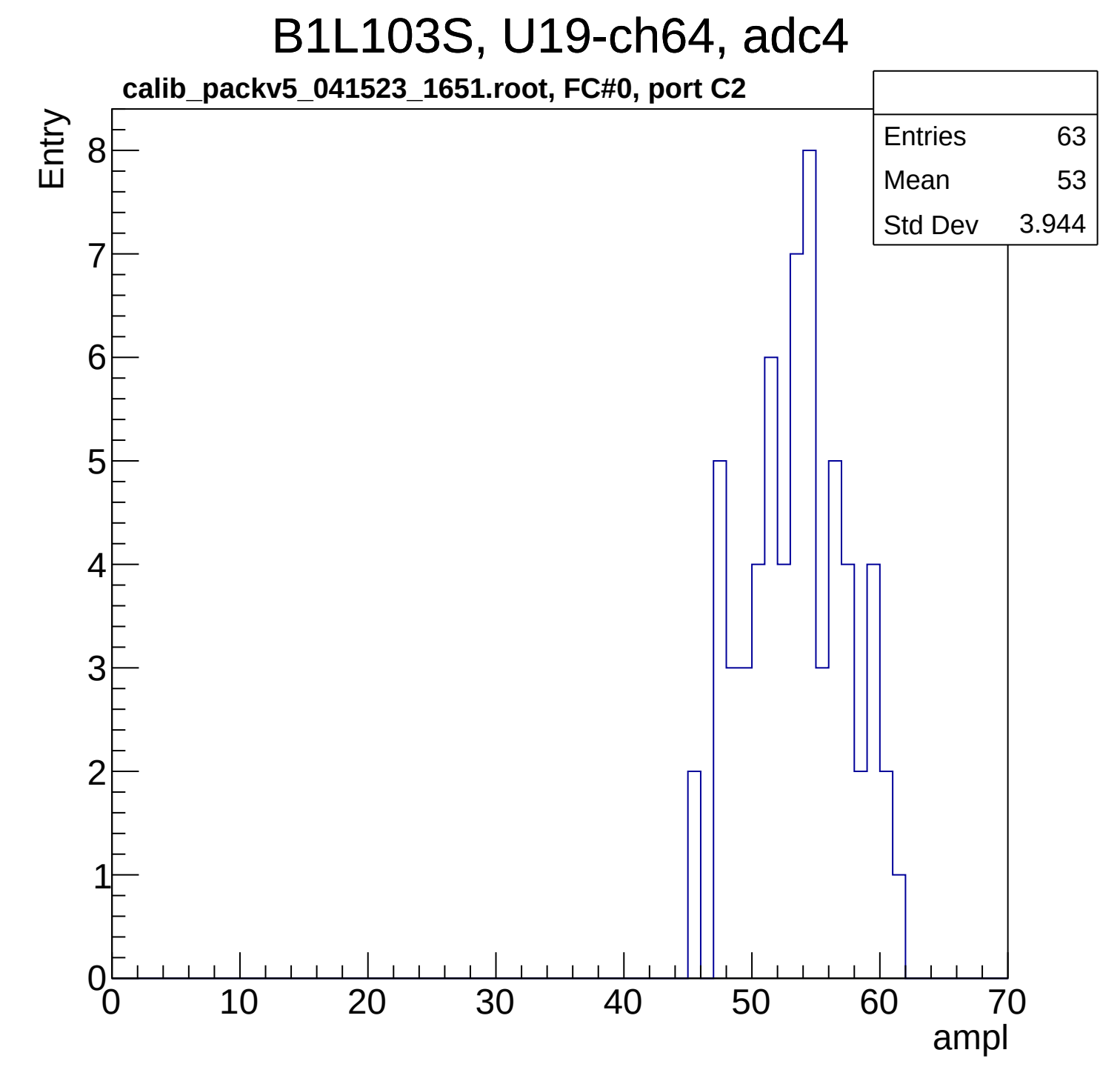
B1L103S, U19-ch64, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 53
Std Dev 3.944
Entry
ampl
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2
3
4
5
6
7
8
0
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60
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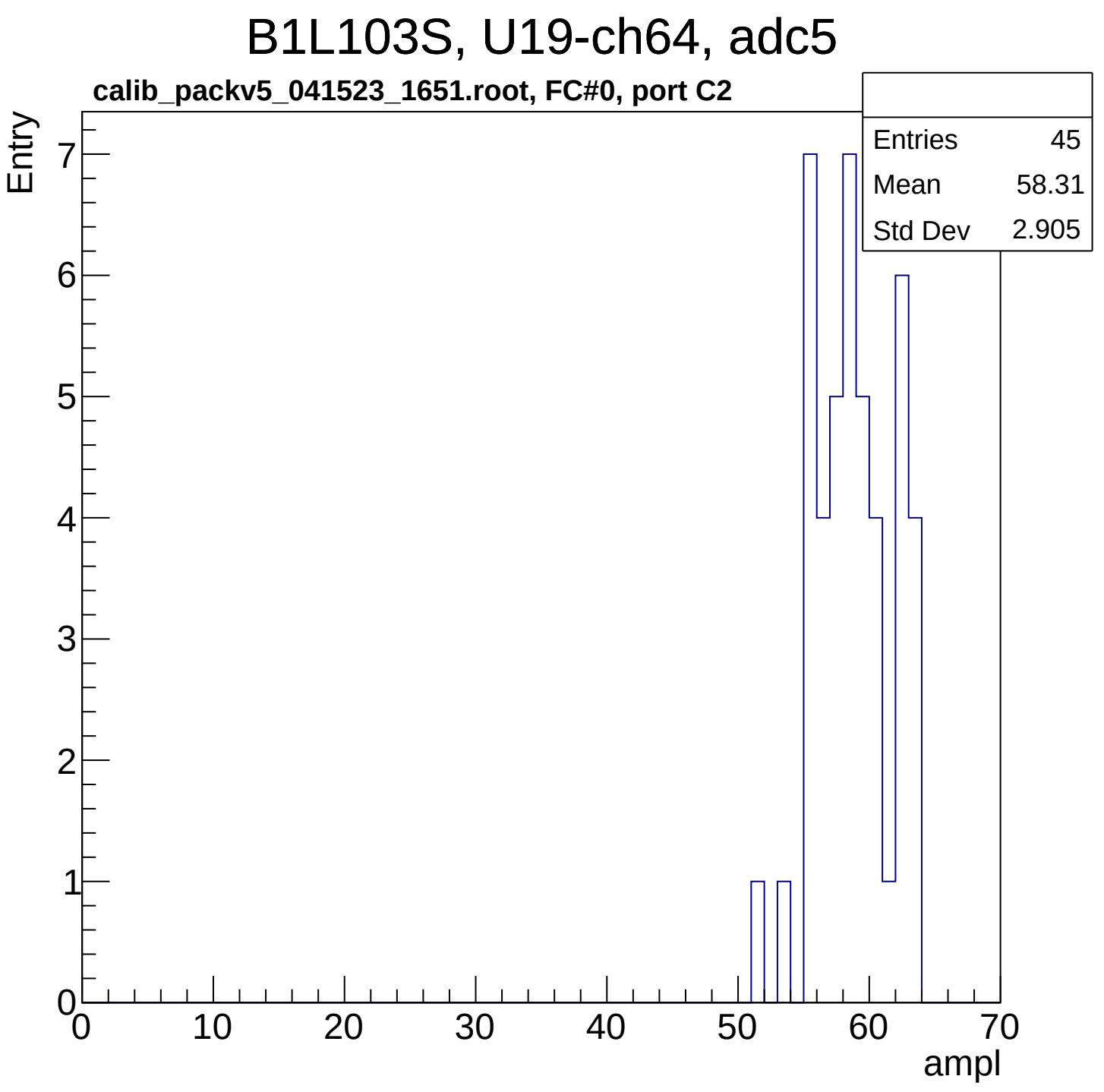
B1L103S, U19-ch64, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 58.31
Std Dev 2.905
Entry
ampl
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1
2
3
4
5
6
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0
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60
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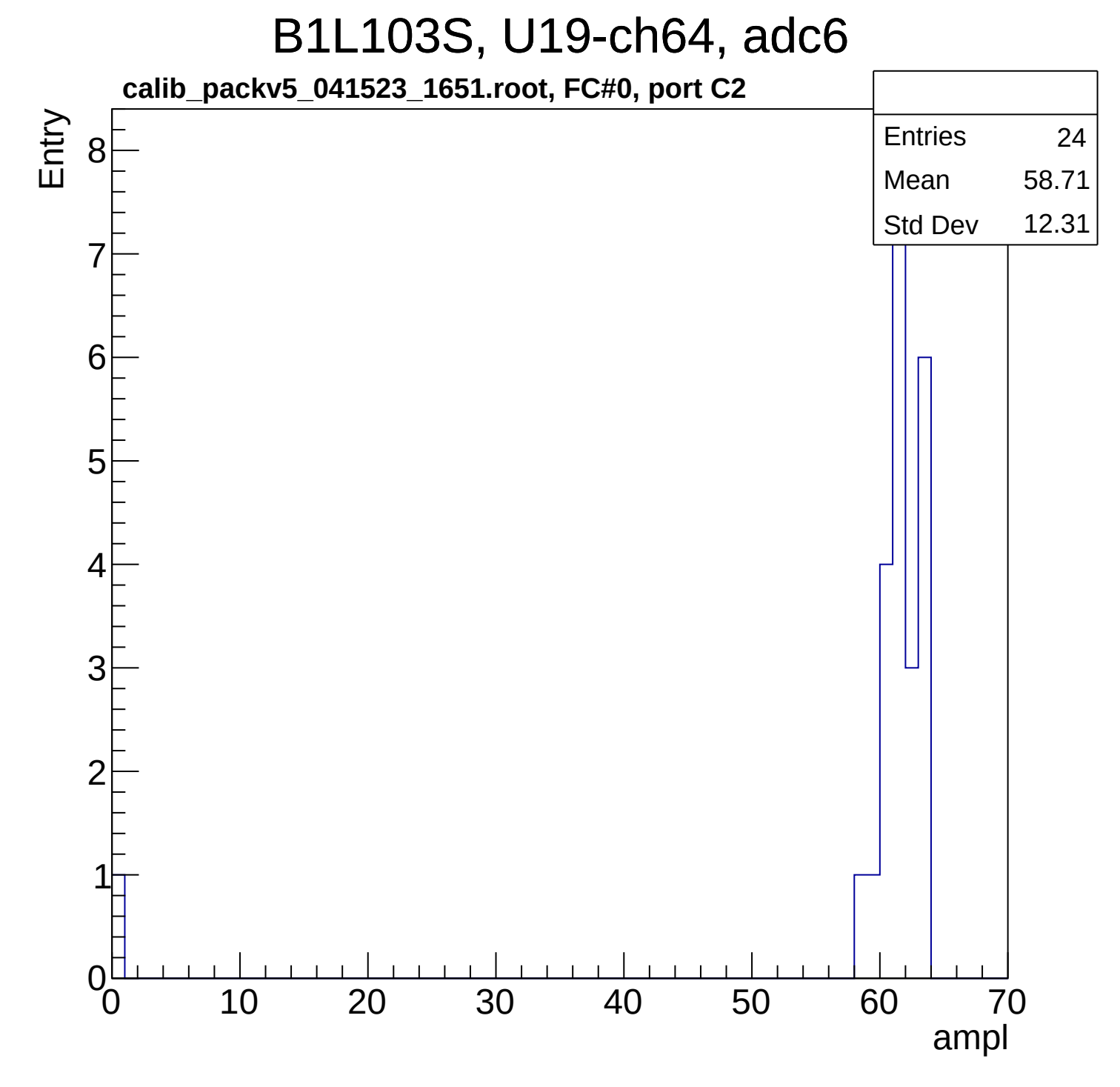
B1L103S, U19-ch64, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 58.71
Std Dev 12.31
Entry
ampl
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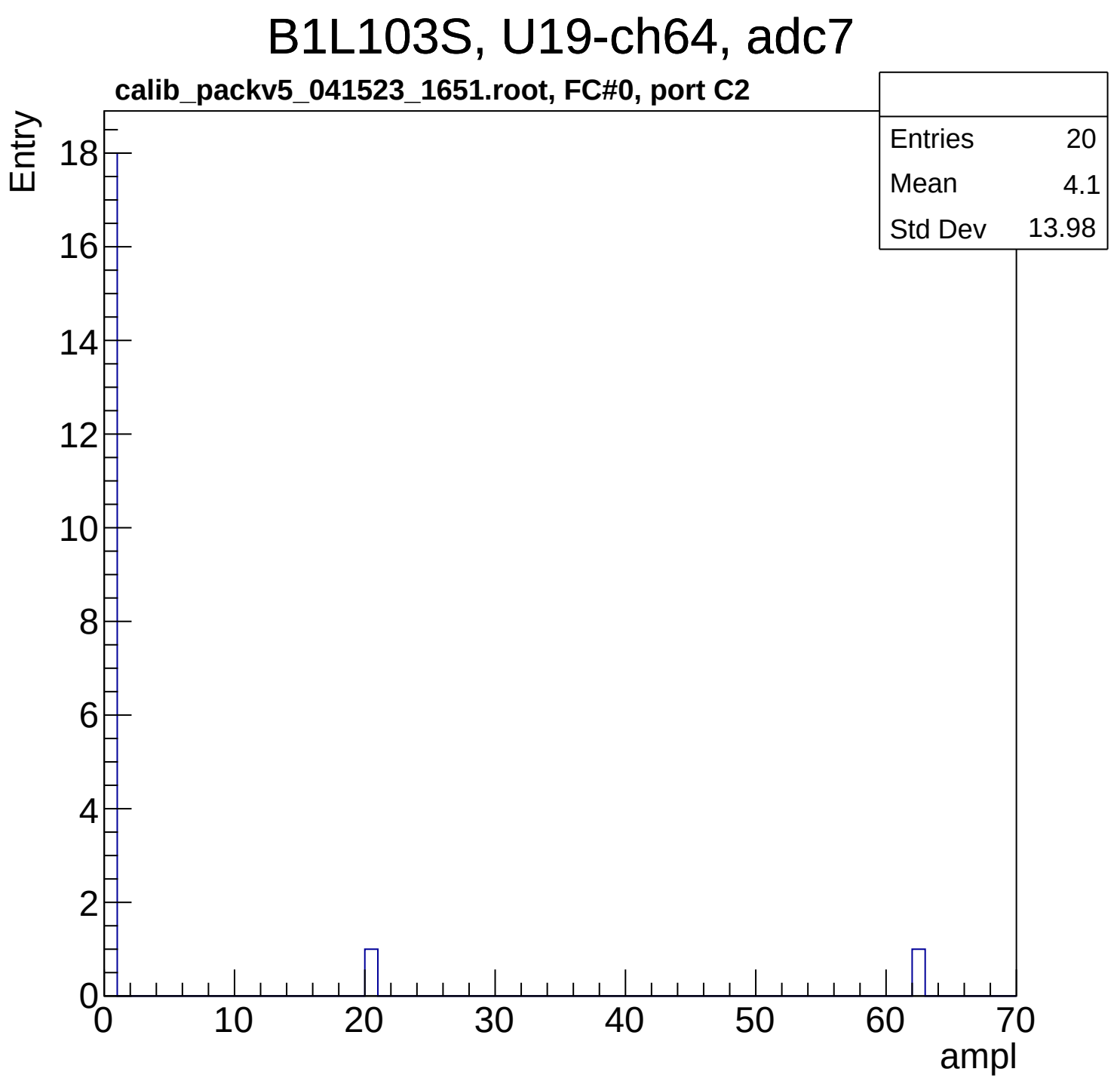
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch64, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4.1
Std Dev 13.98
Entry
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6
8
10
12
14
16
18
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10
20
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50
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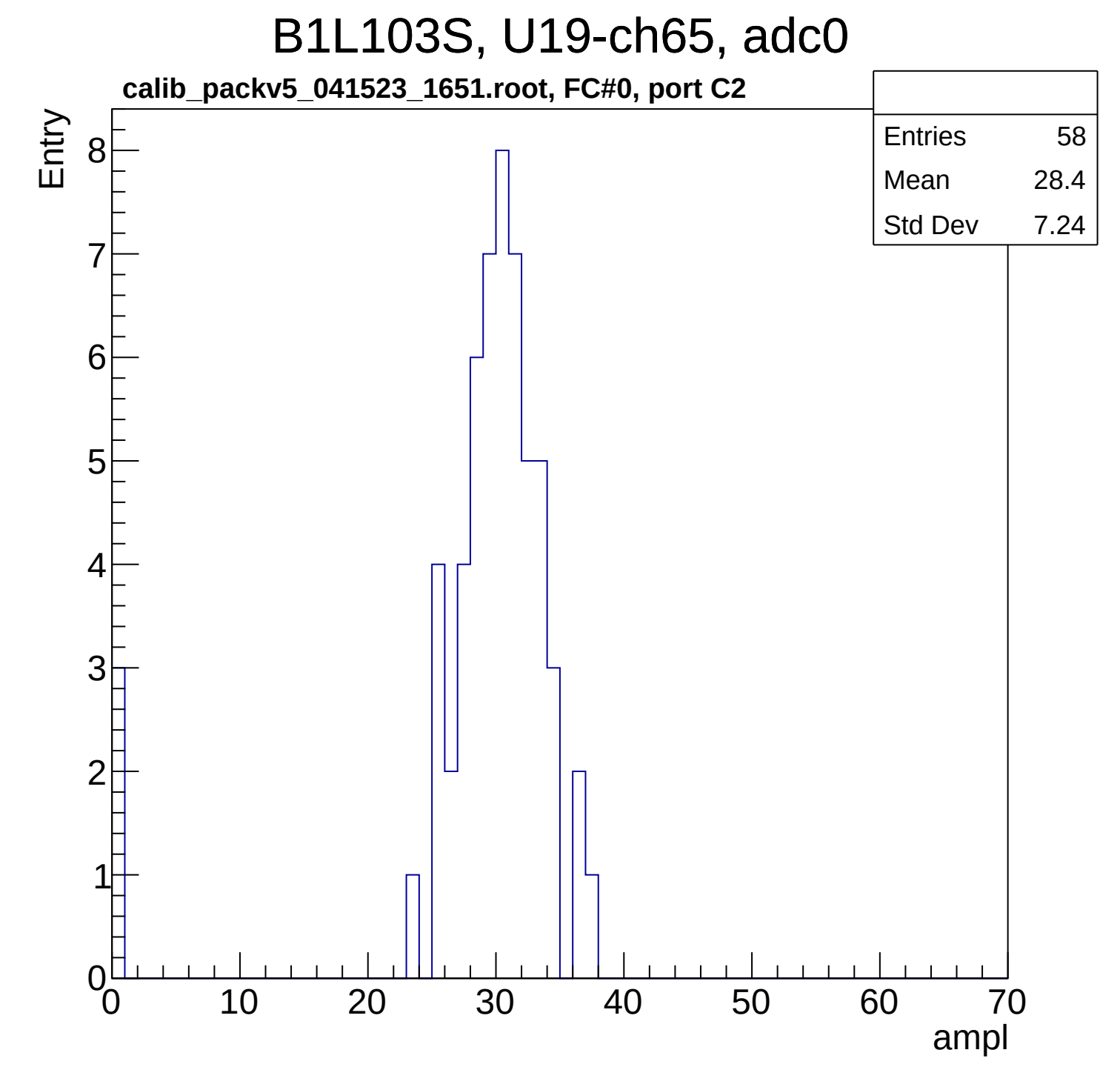
70
ampl


B1L103S, U19-ch65, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 28.4
Std Dev 7.24
Entry
ampl
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2
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5
6
7
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0
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60
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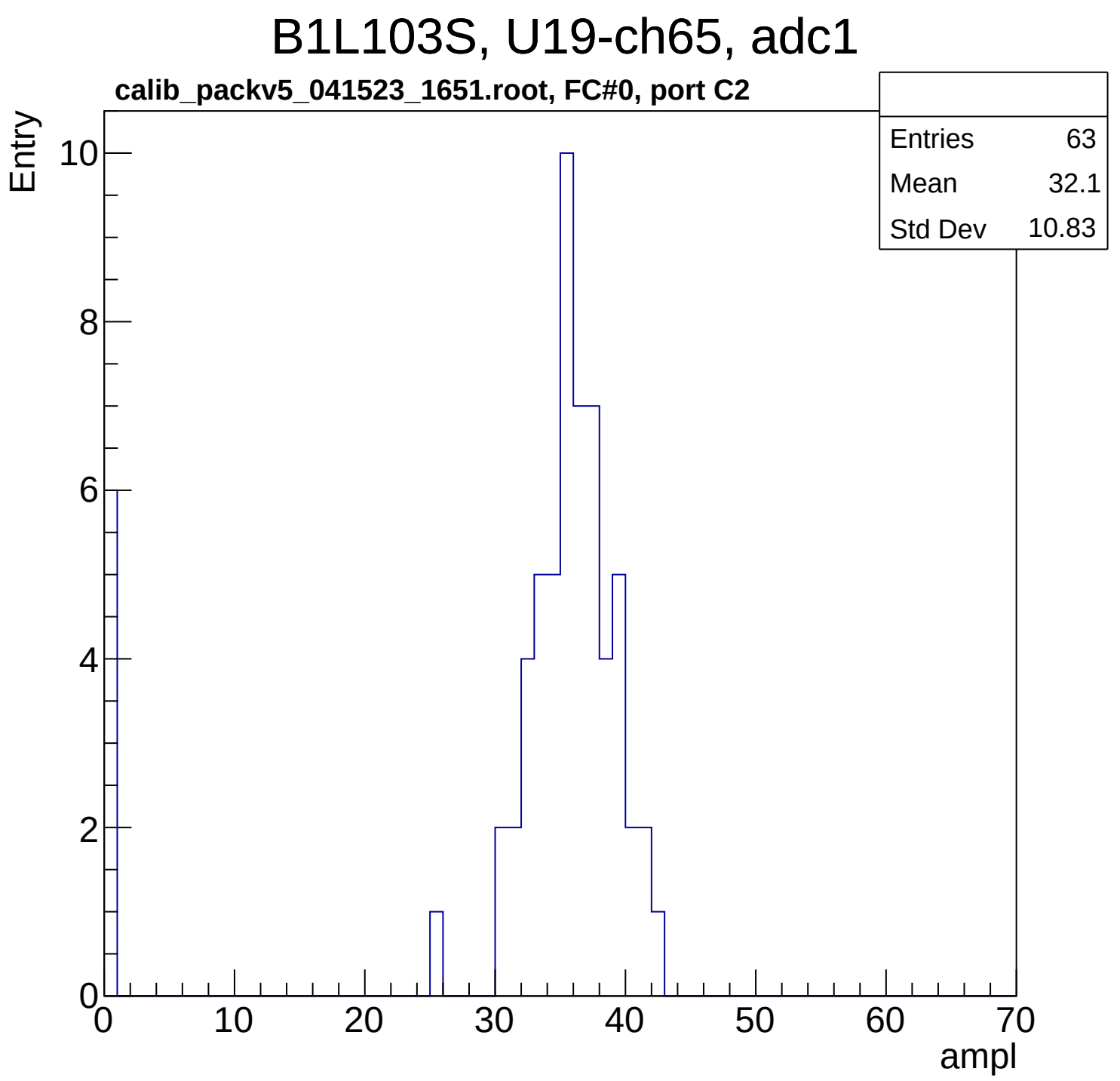
B1L103S, U19-ch65, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 32.1
Std Dev 10.83
Entry
ampl
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2
4
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8
10
0
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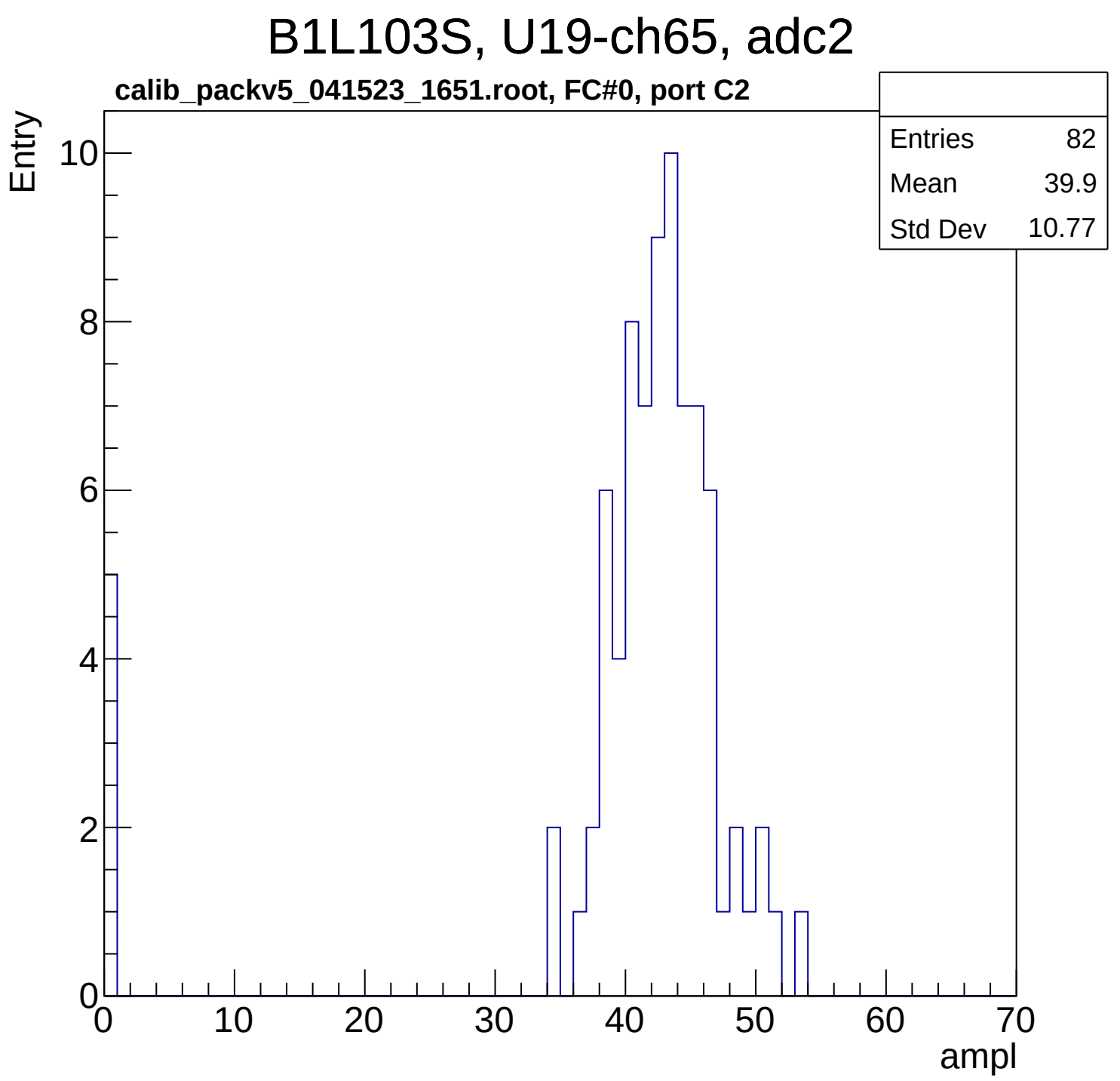
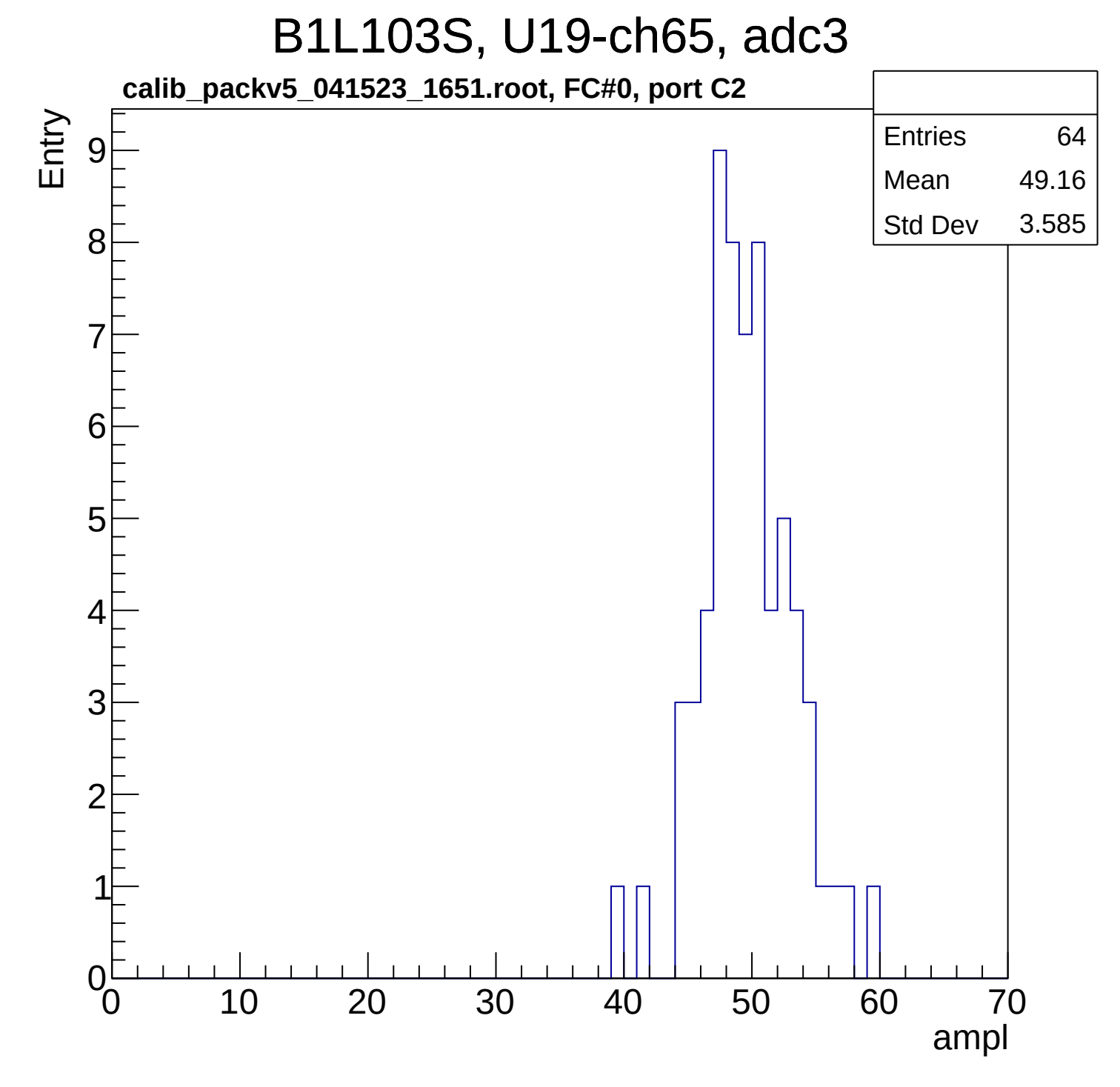
30
40
50
60
70


B1L103S, U19-ch65, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 39.9
Std Dev 10.77
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch65, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 49.16
Std Dev 3.585
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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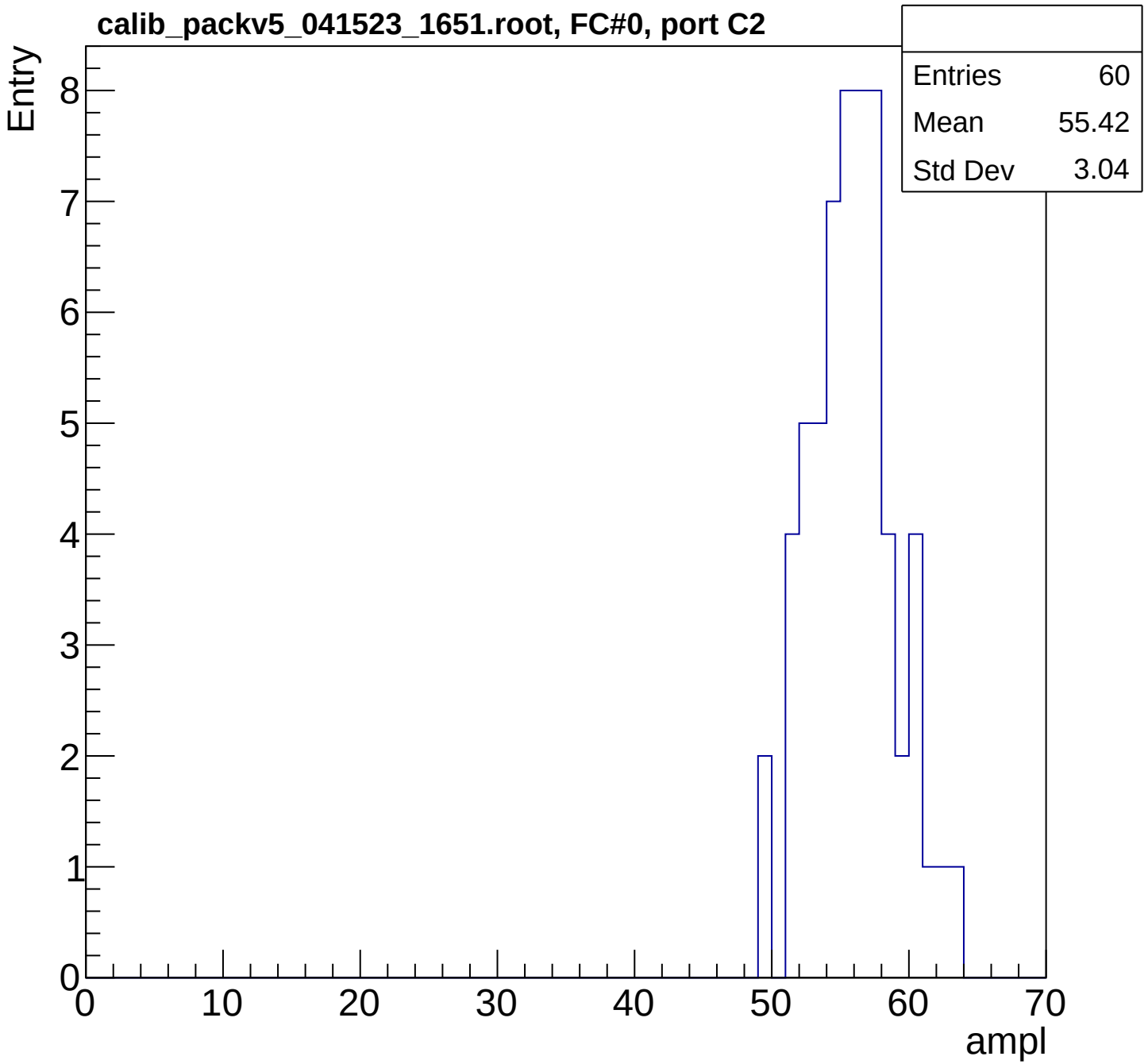
60
70


B1L103S, U19-ch65, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 55.42
Std Dev 3.04
Entry
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2
3
4
5
6
7
8
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50
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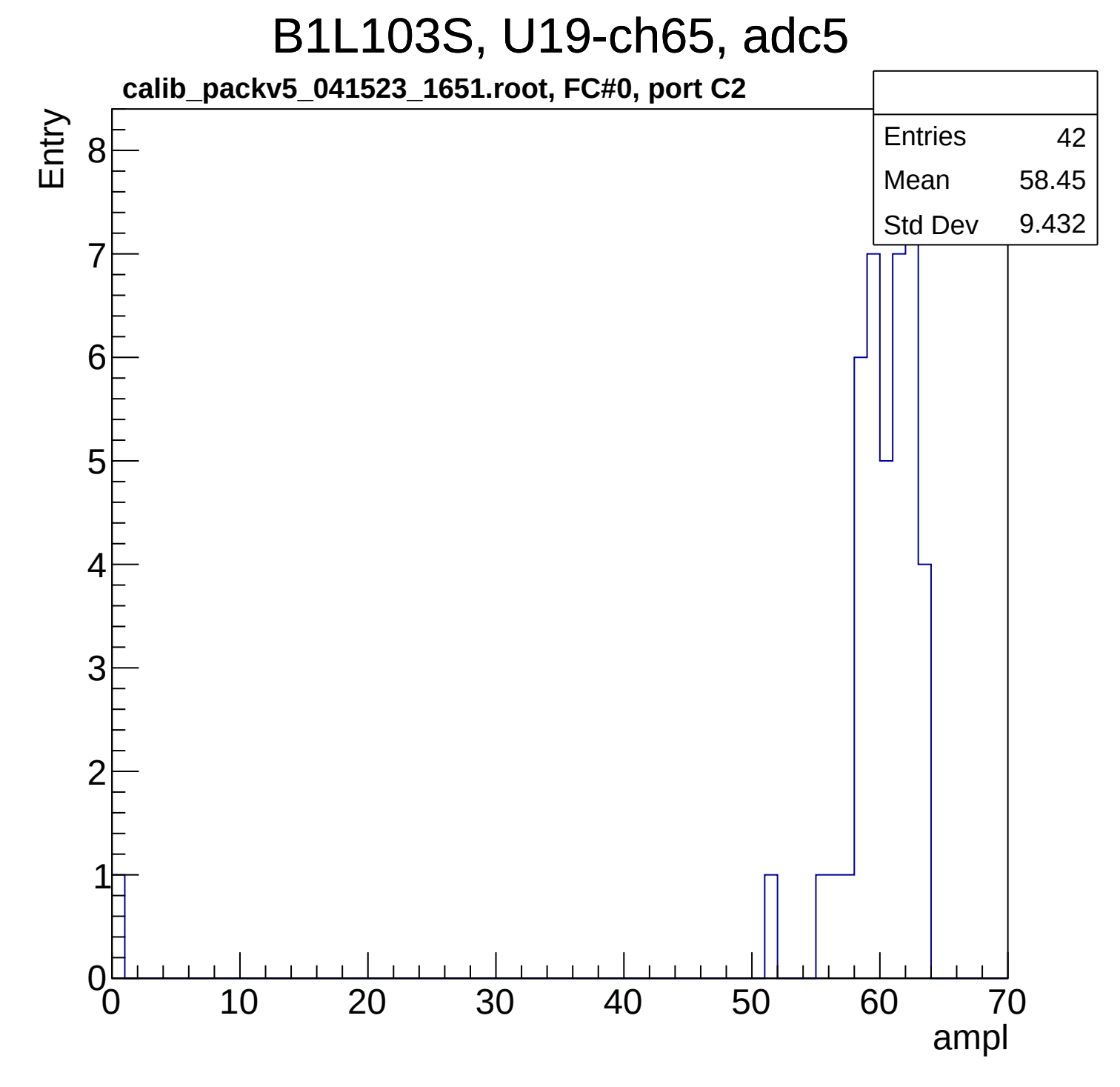
70
ampl


B1L103S, U19-ch65, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 58.45
Std Dev 9.432
Entry
ampl
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2
3
4
5
6
7
8
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10
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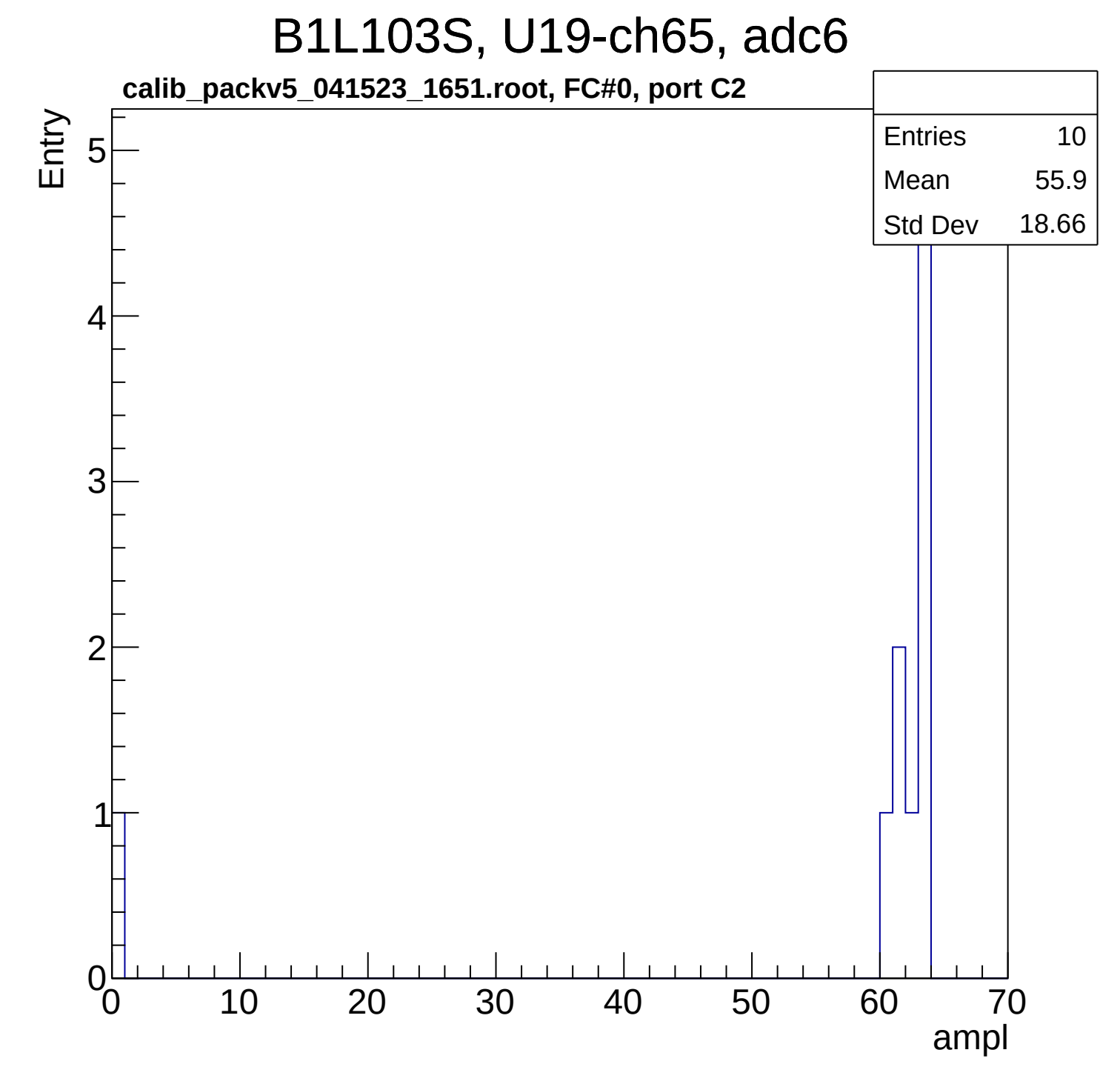
50
60
70


B1L103S, U19-ch65, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 55.9
Std Dev 18.66
Entry
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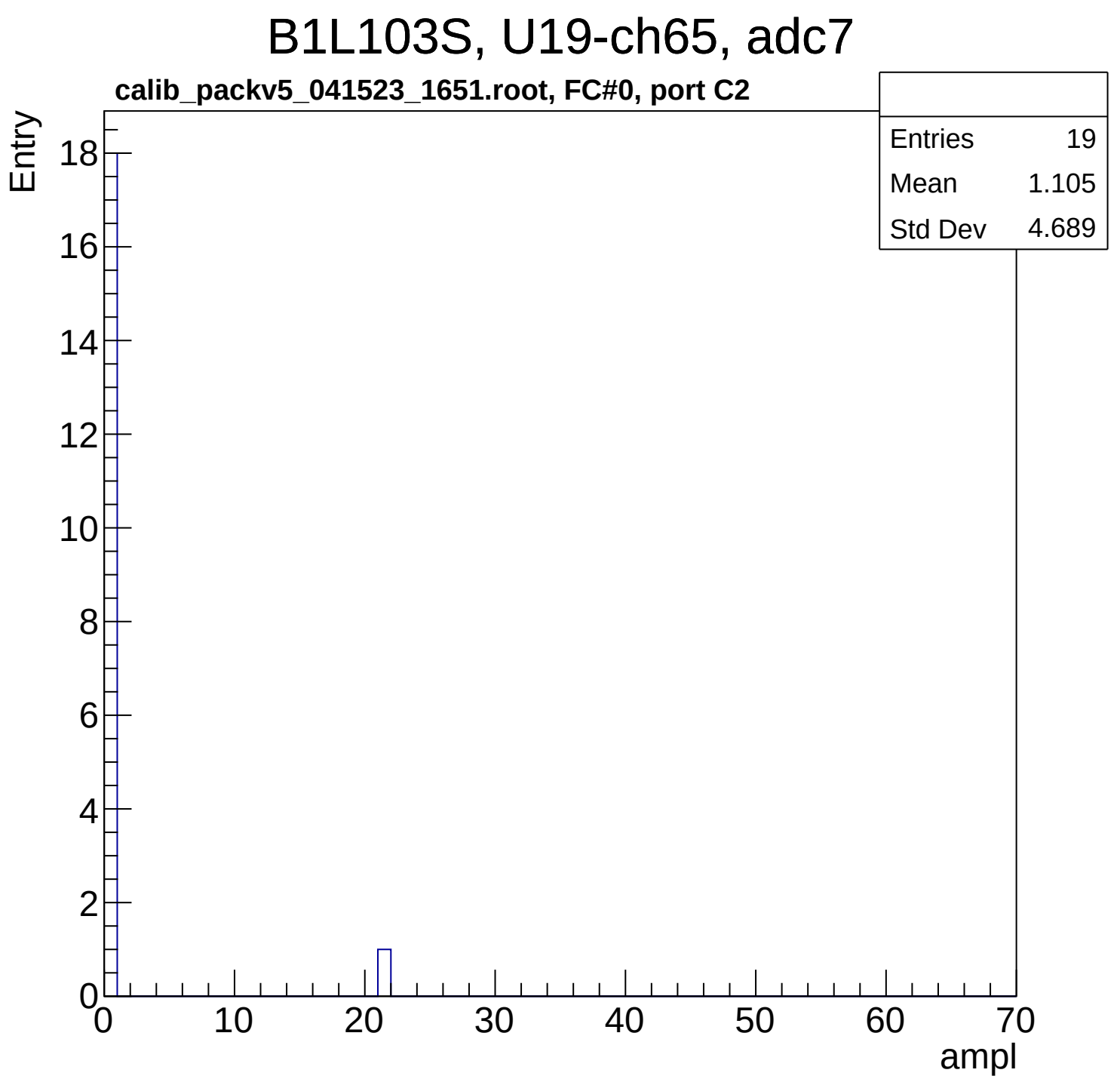
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch65, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.105
Std Dev 4.689
Entry
0
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6
8
10
12
14
16
18
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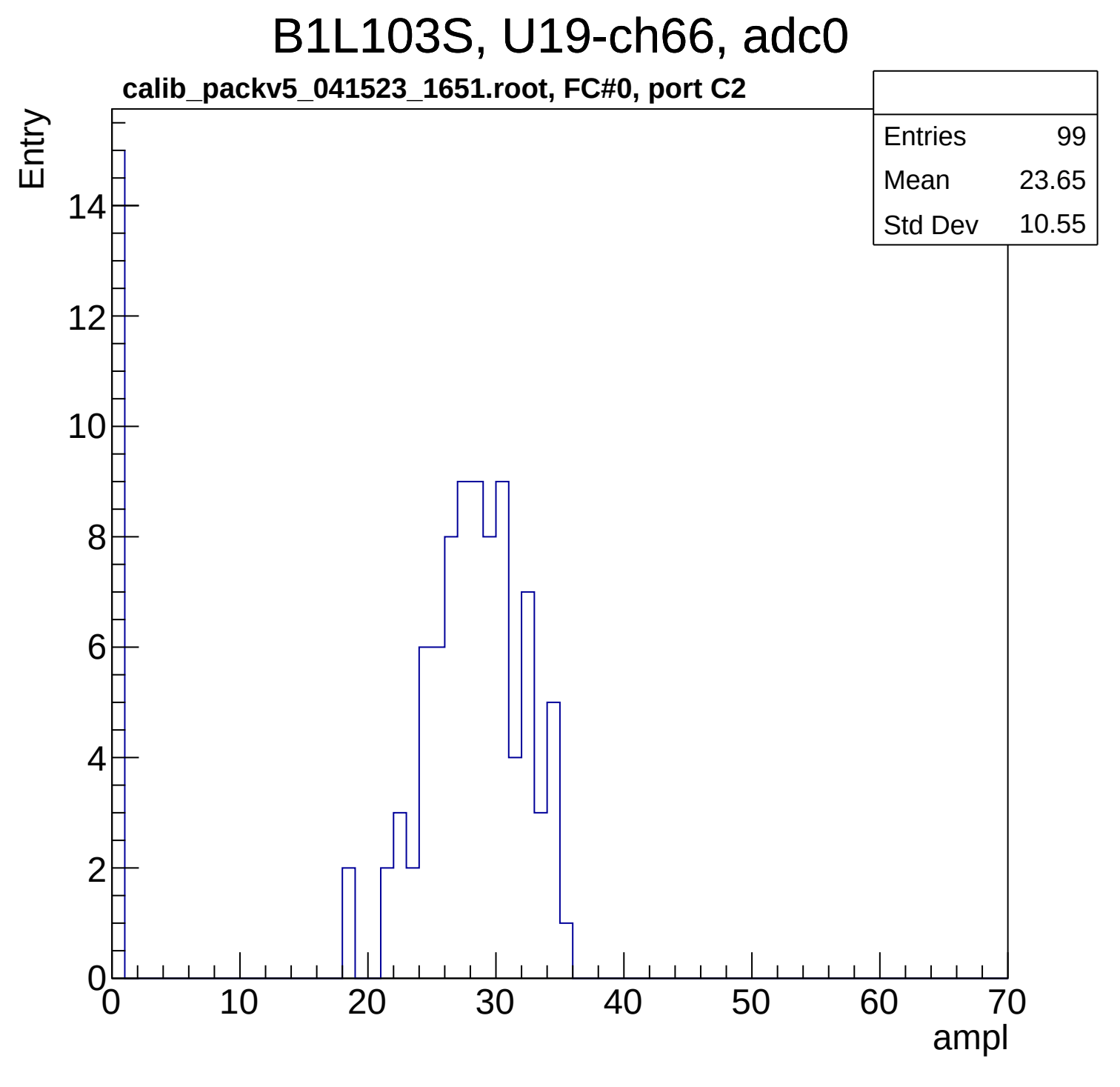
70
ampl


B1L103S, U19-ch66, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 23.65
Std Dev 10.55
Entry
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2
4
6
8
10
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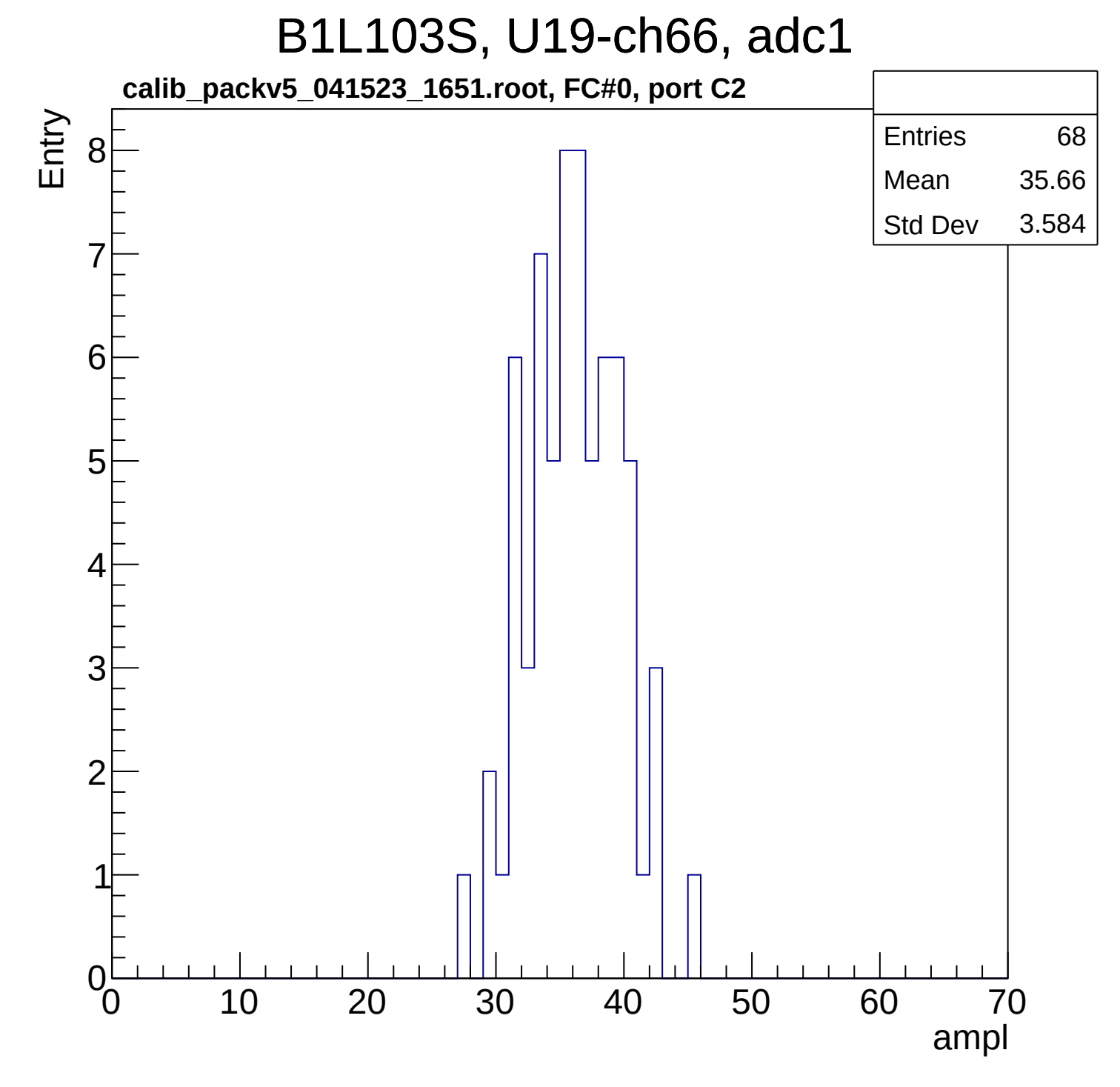
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch66, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 35.66
Std Dev 3.584
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
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40
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60
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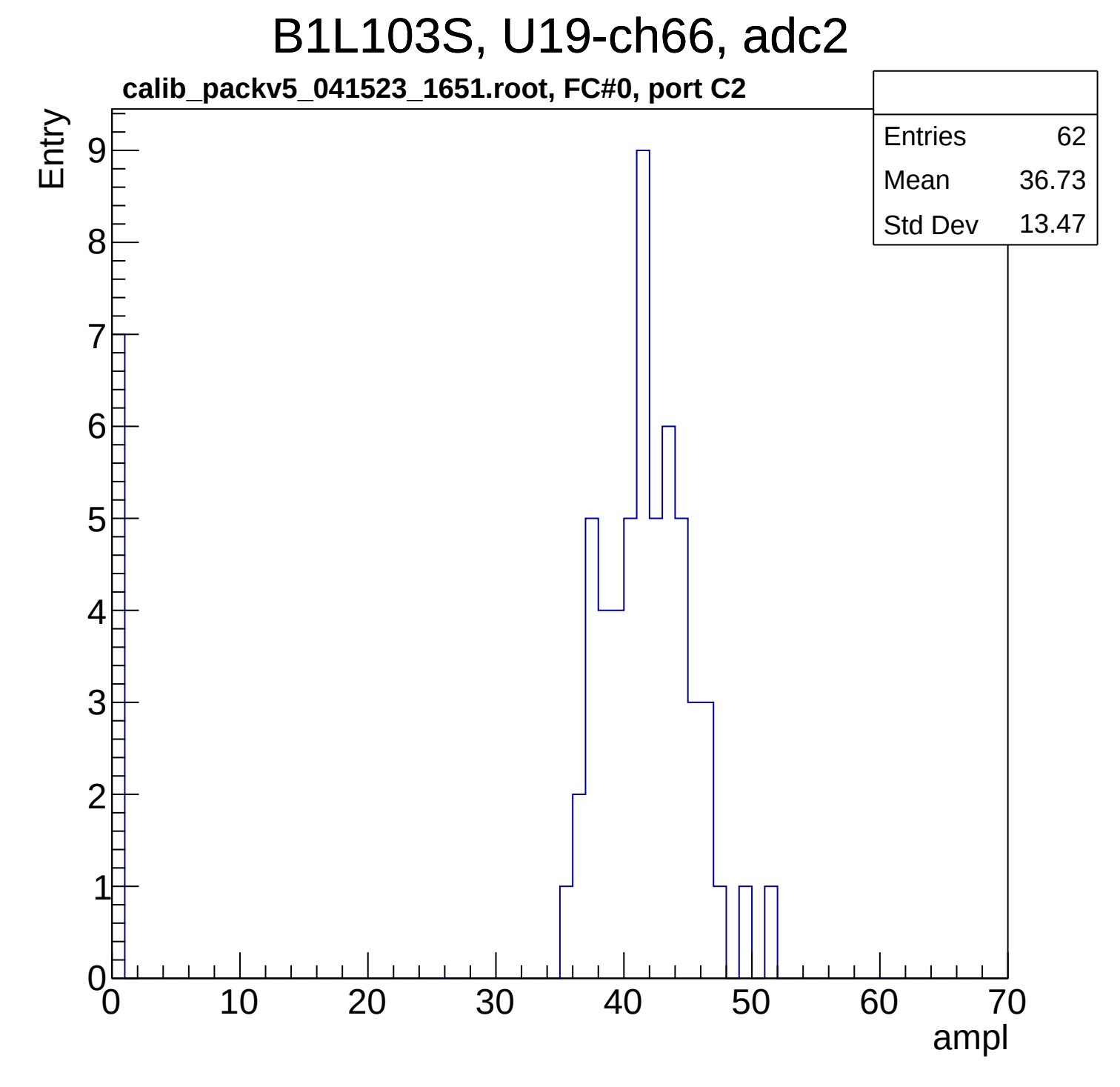
B1L103S, U19-ch66, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 36.73
Std Dev 13.47
Entry
ampl
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2
3
4
5
6
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8
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0
10
20
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40
50
60
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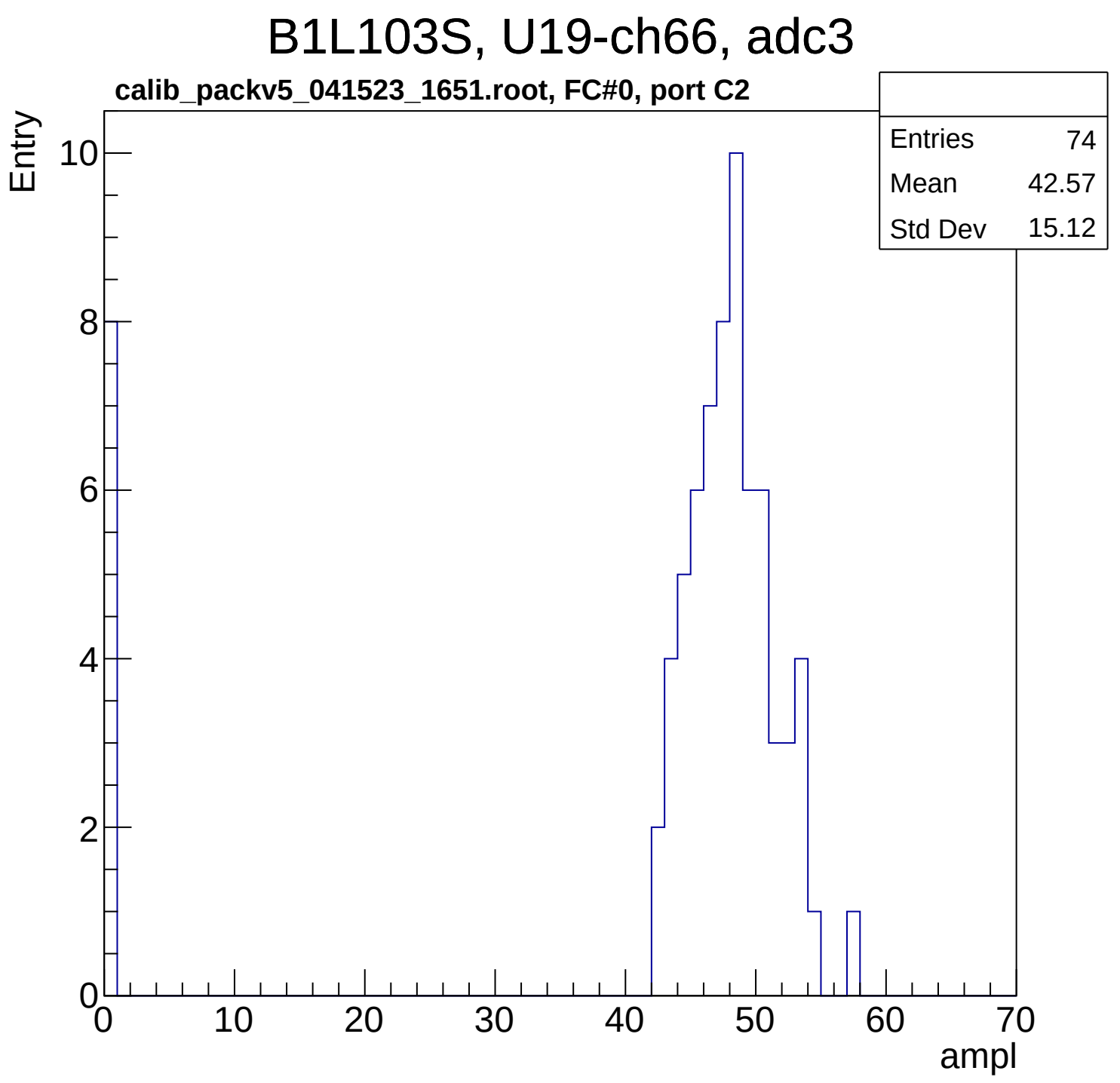
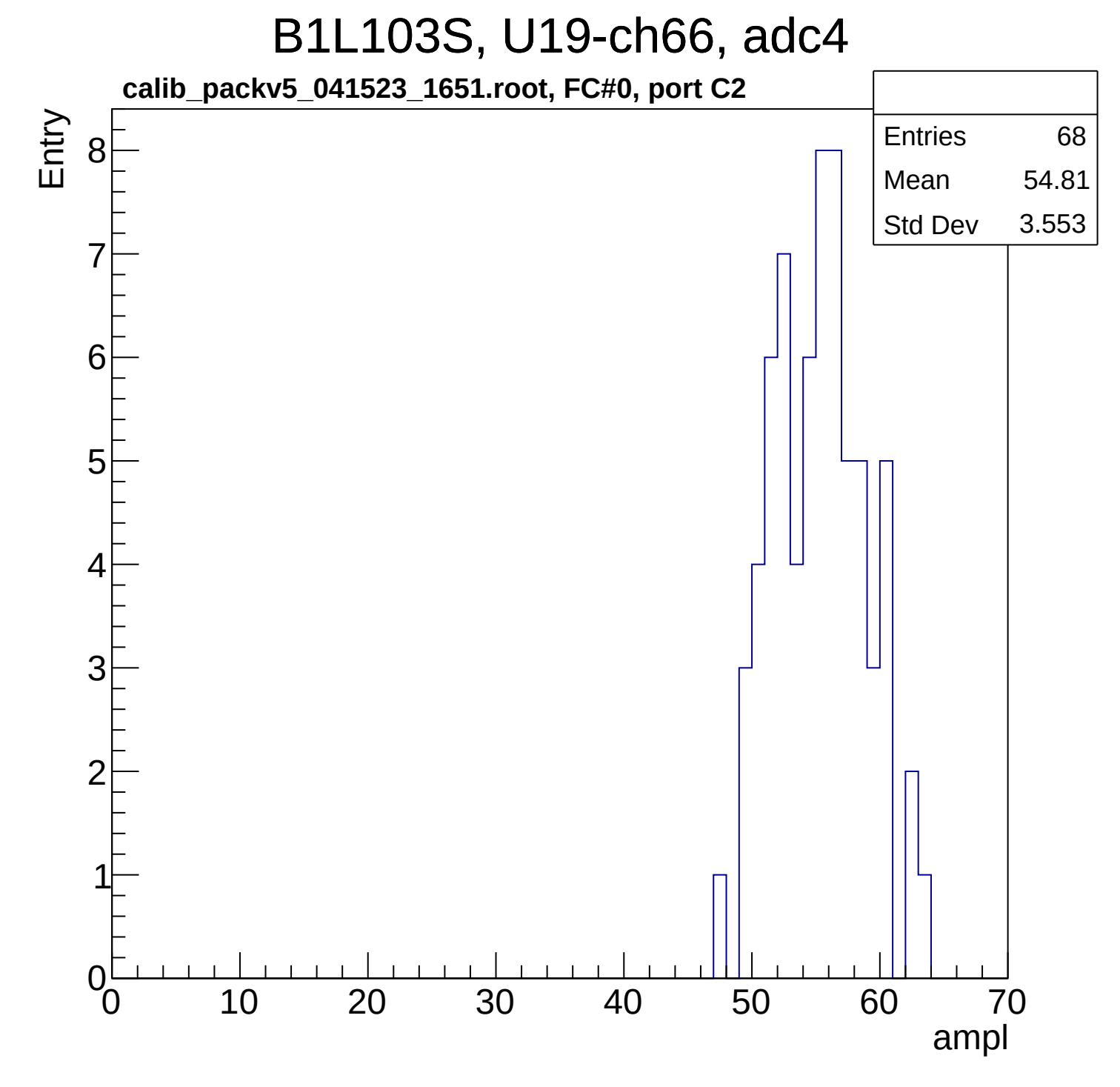

B1L103S, U19-ch66, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 42.57
Std Dev 15.12
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch66, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 54.81
Std Dev 3.553
Entry
ampl
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1
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4
5
6
7
8
0
10
20
30
40
50
60
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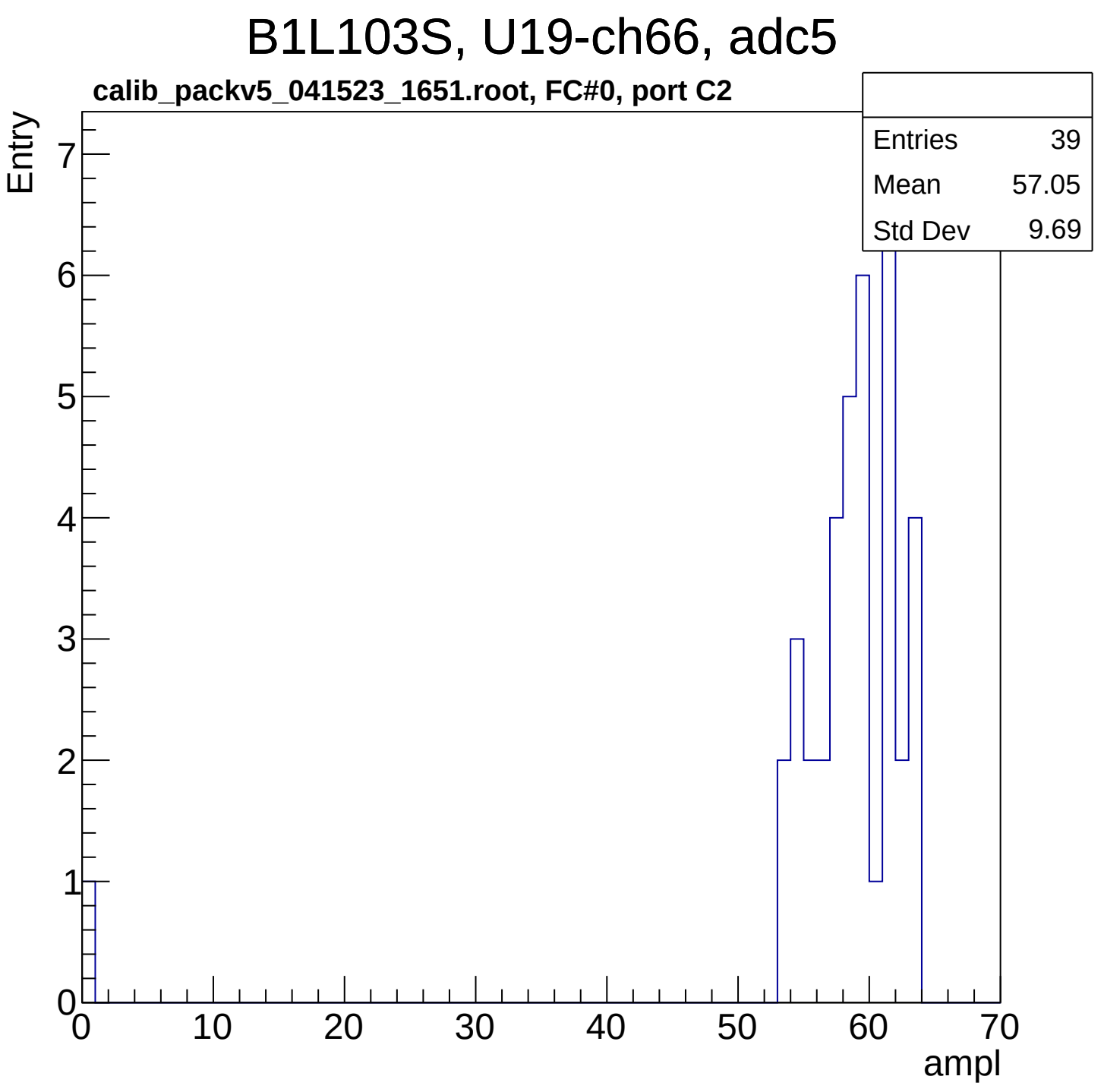
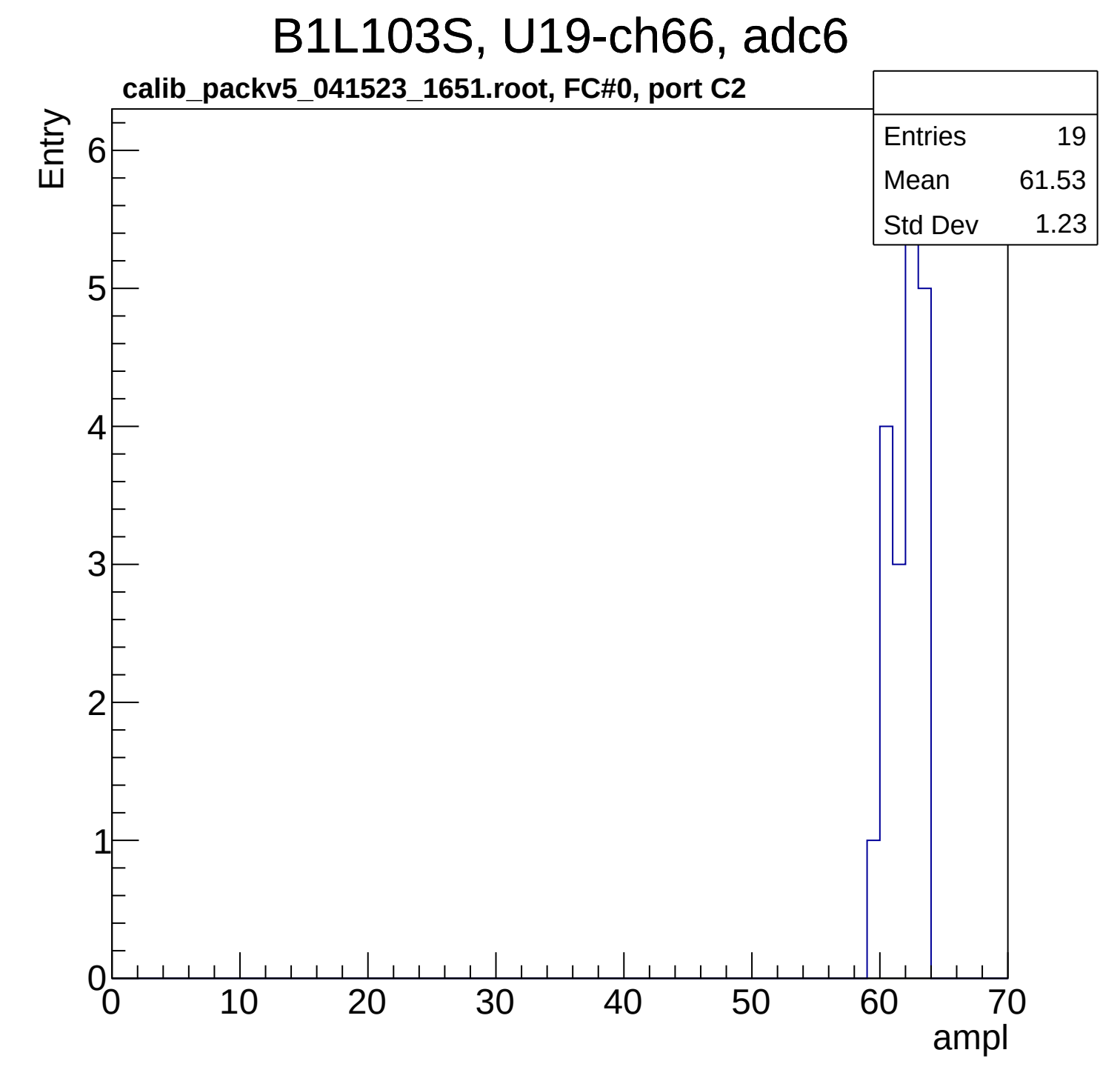
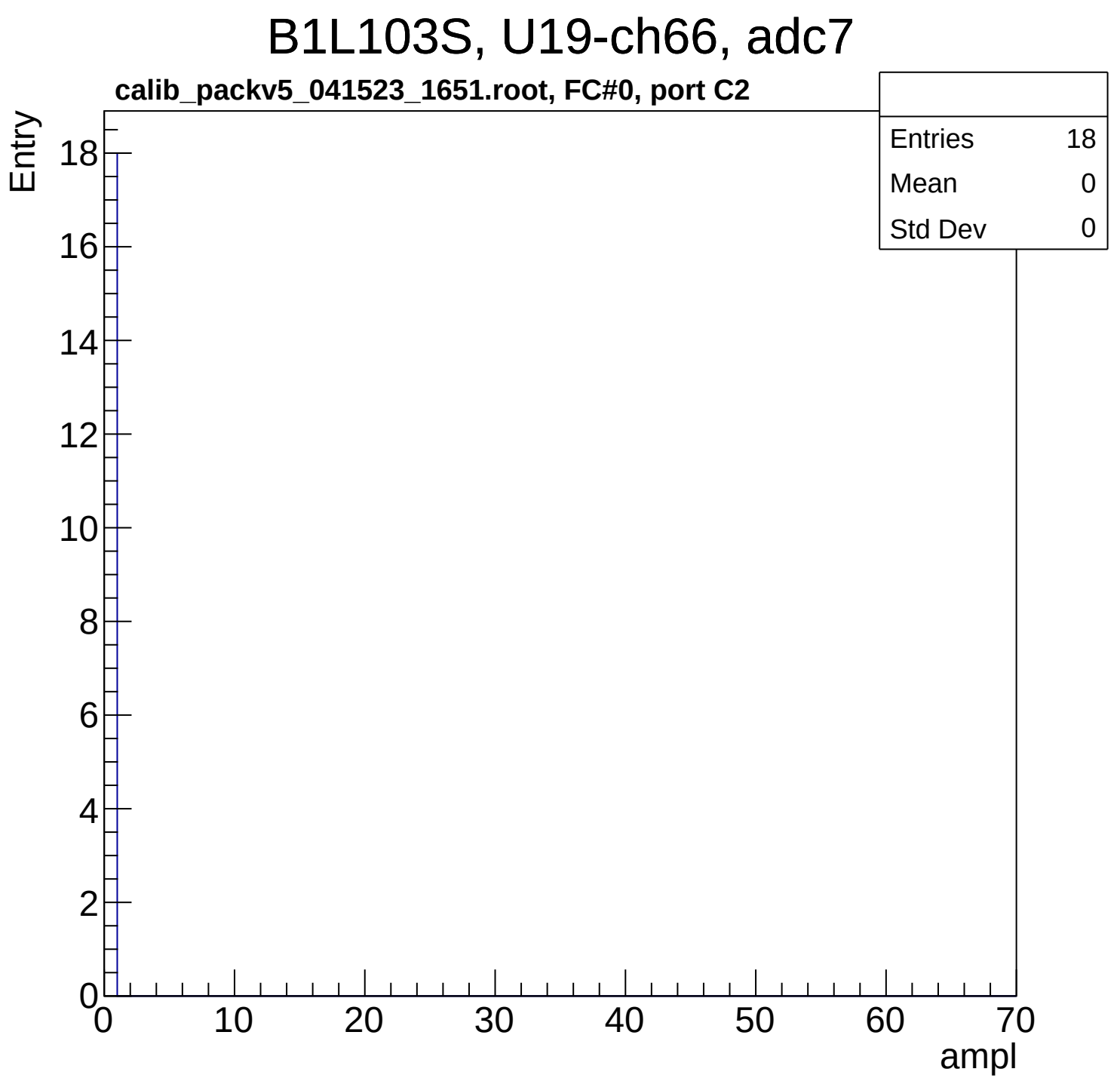
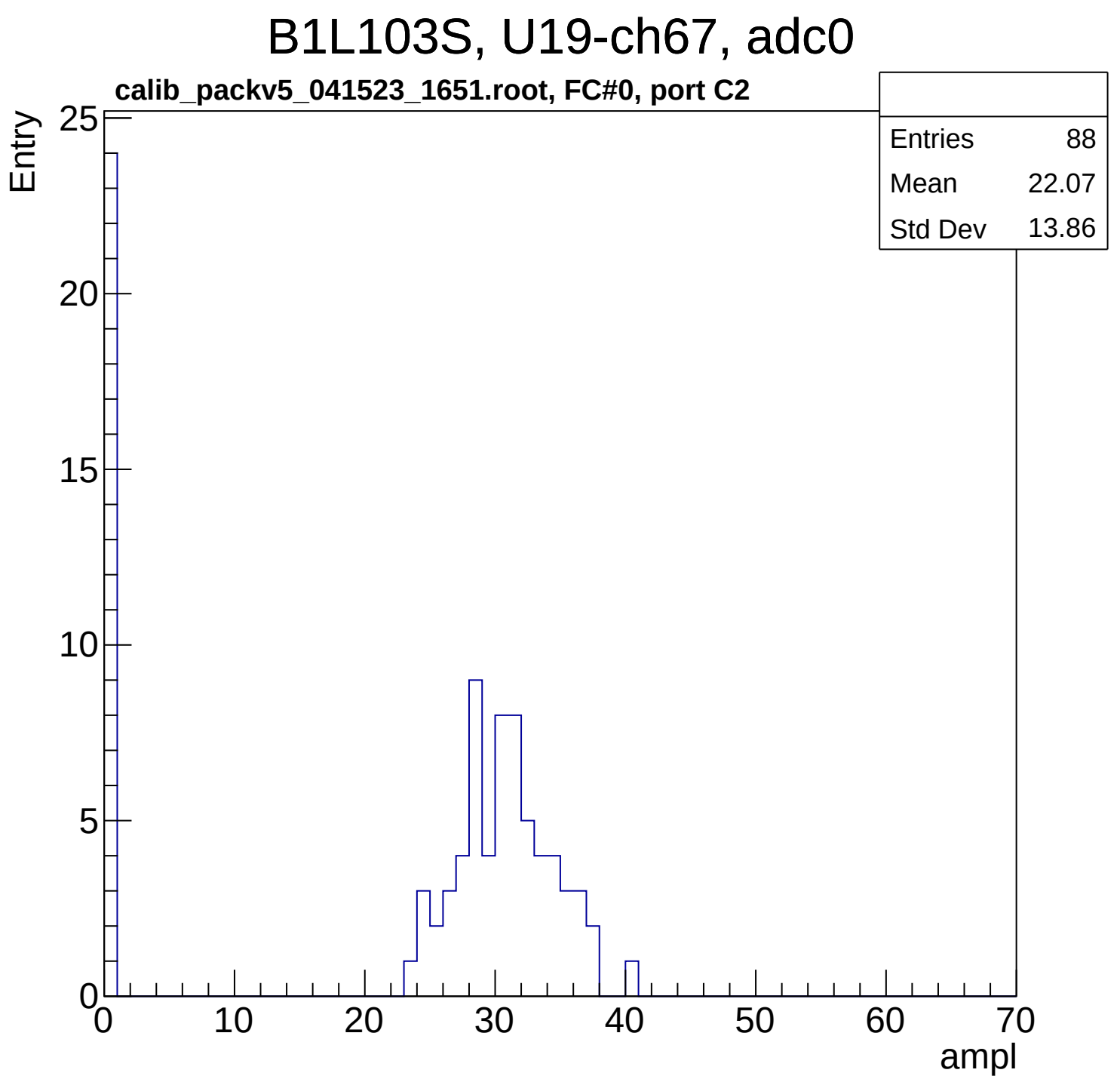
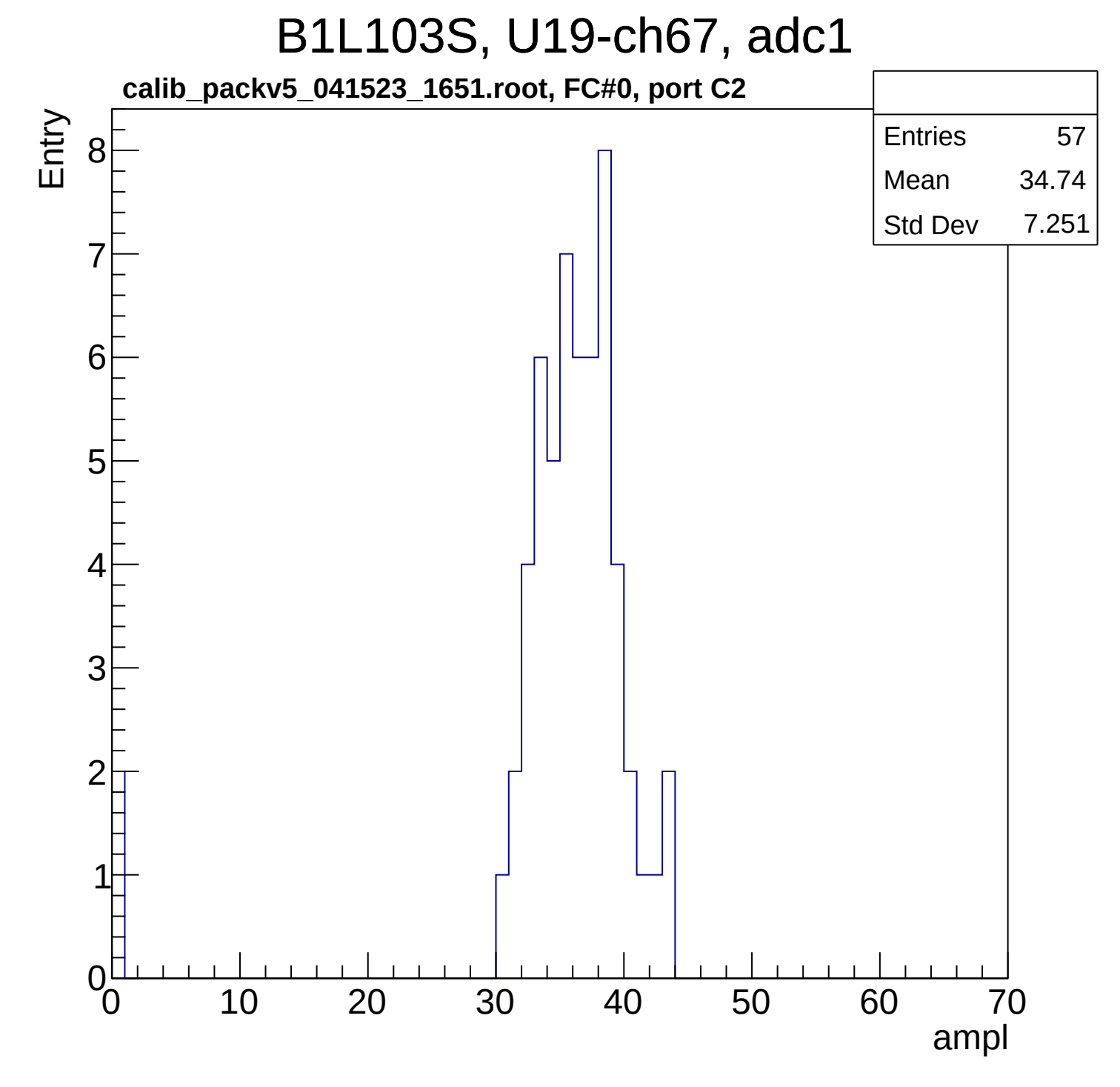
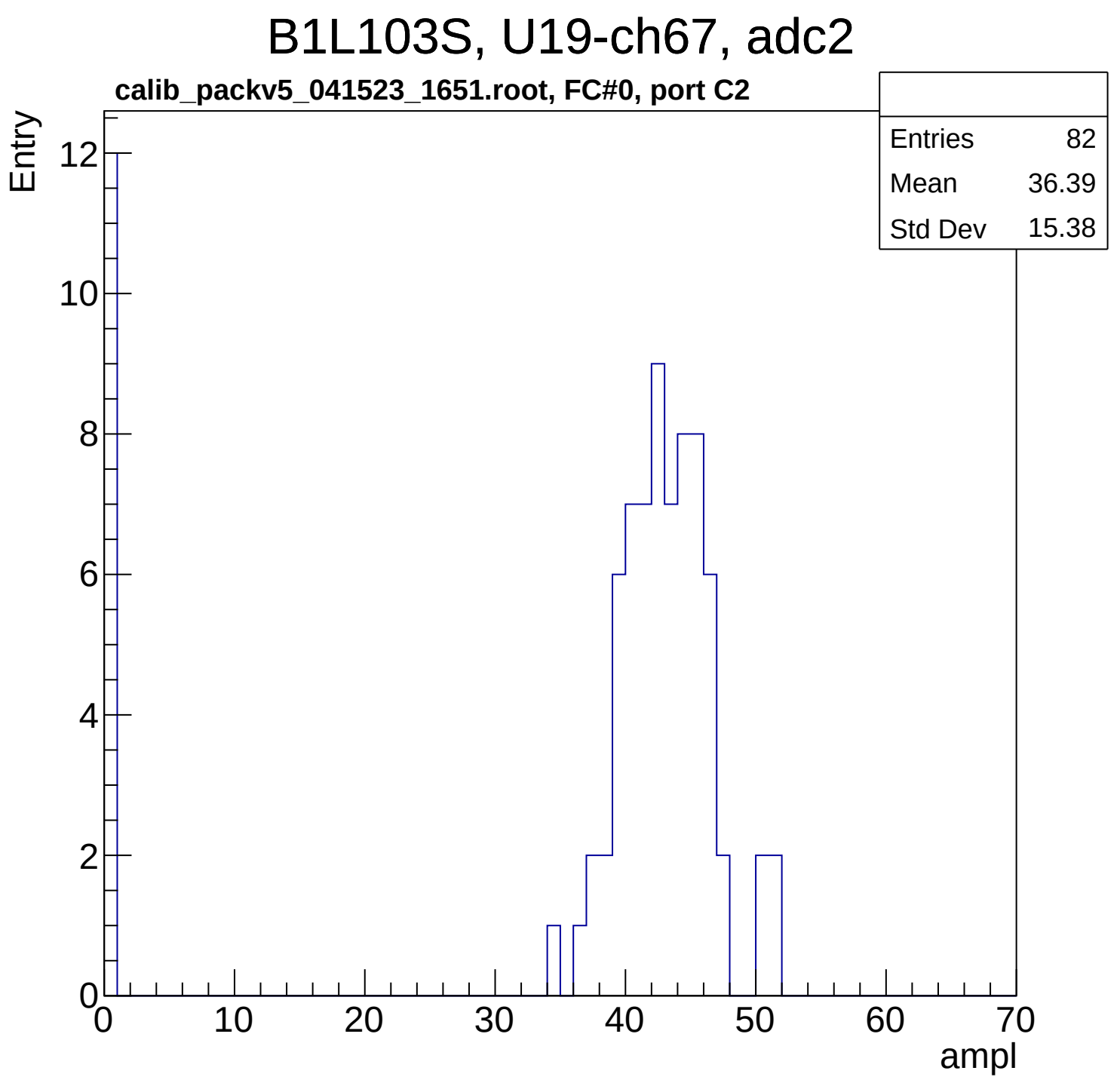

B1L103S, U19-ch66, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 57.05
Std Dev 9.69
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

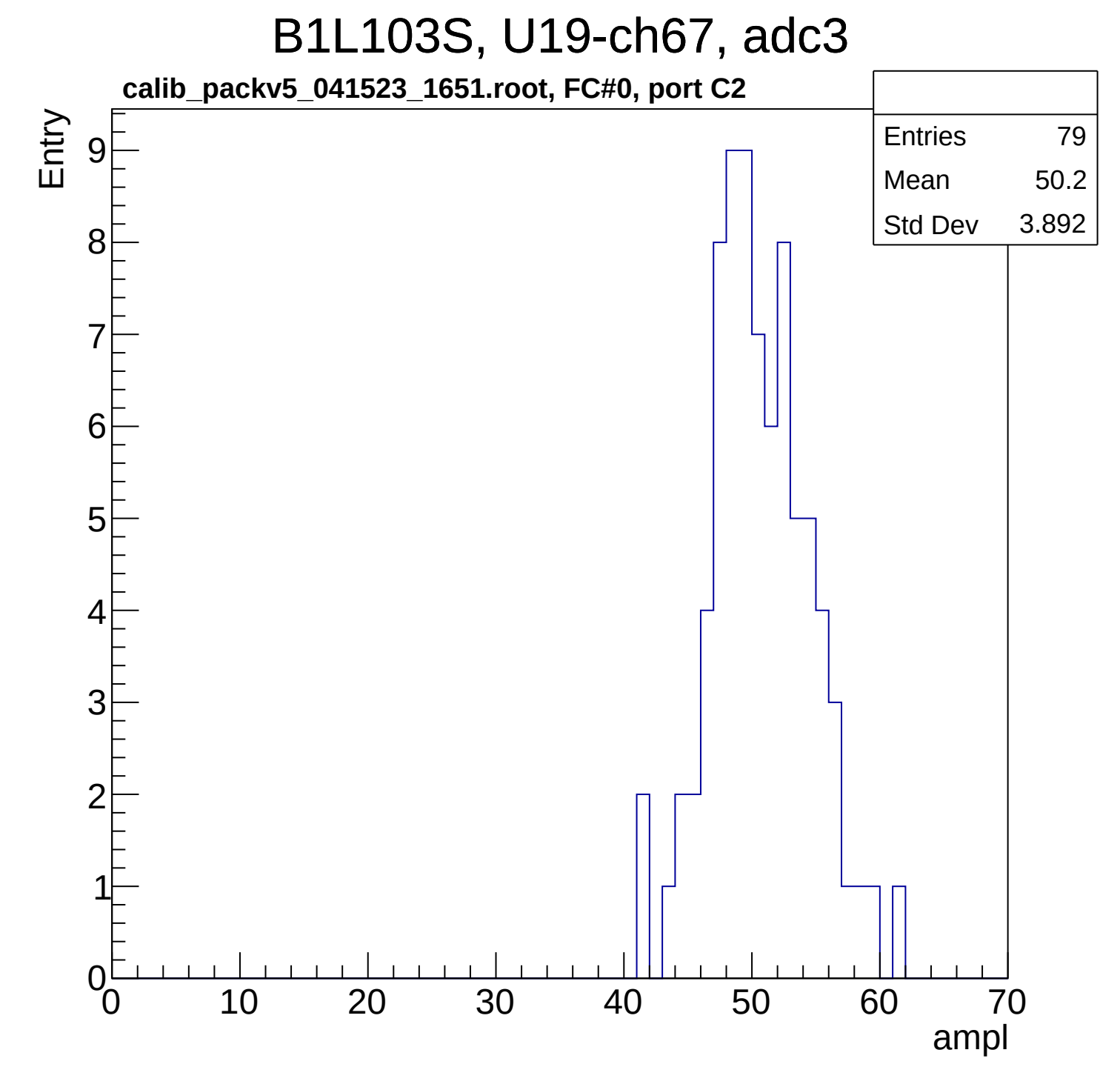

B1L103S, U19-ch66, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 61.53
Std Dev 1.23
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

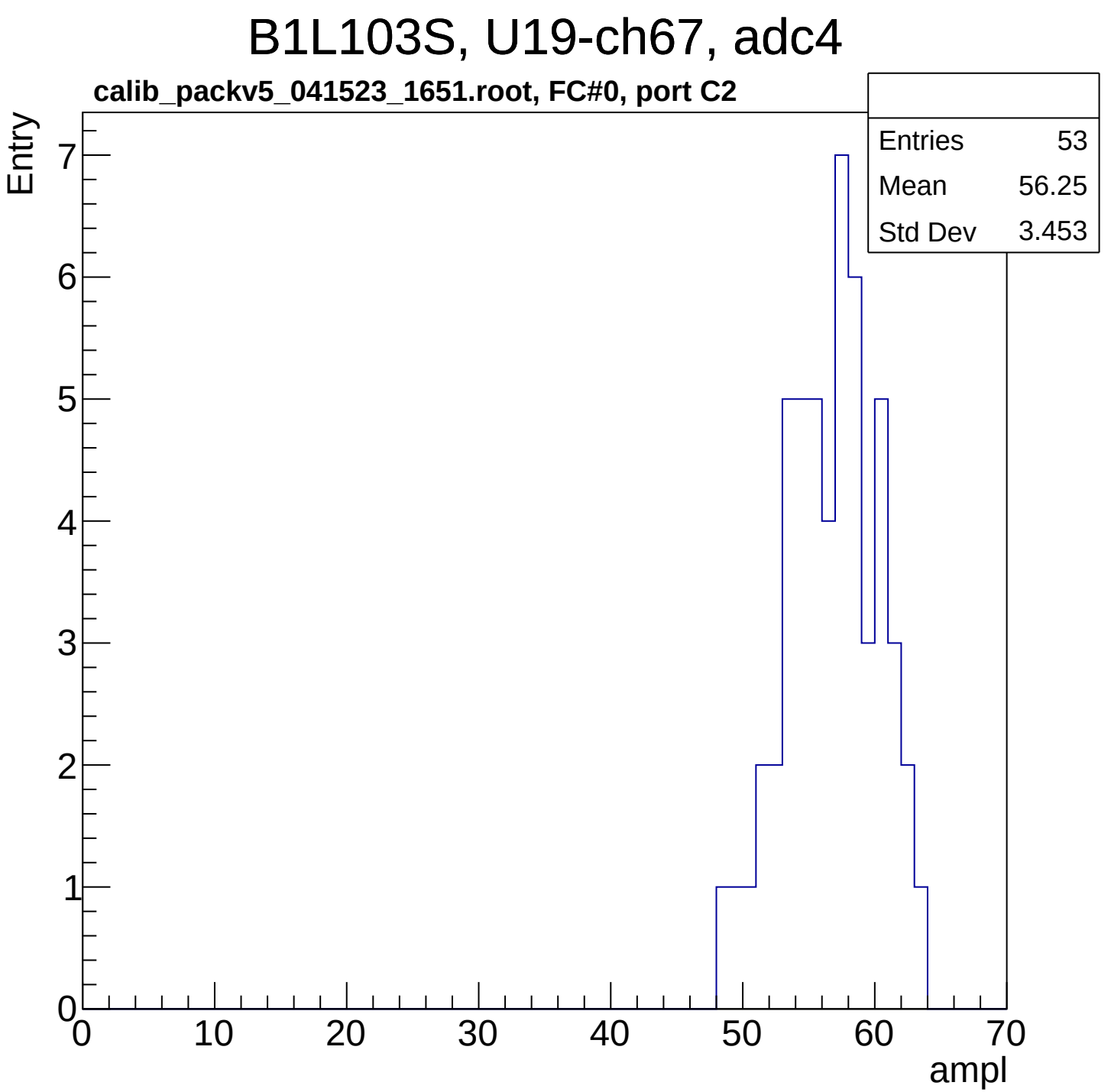

B1L103S, U19-ch66, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

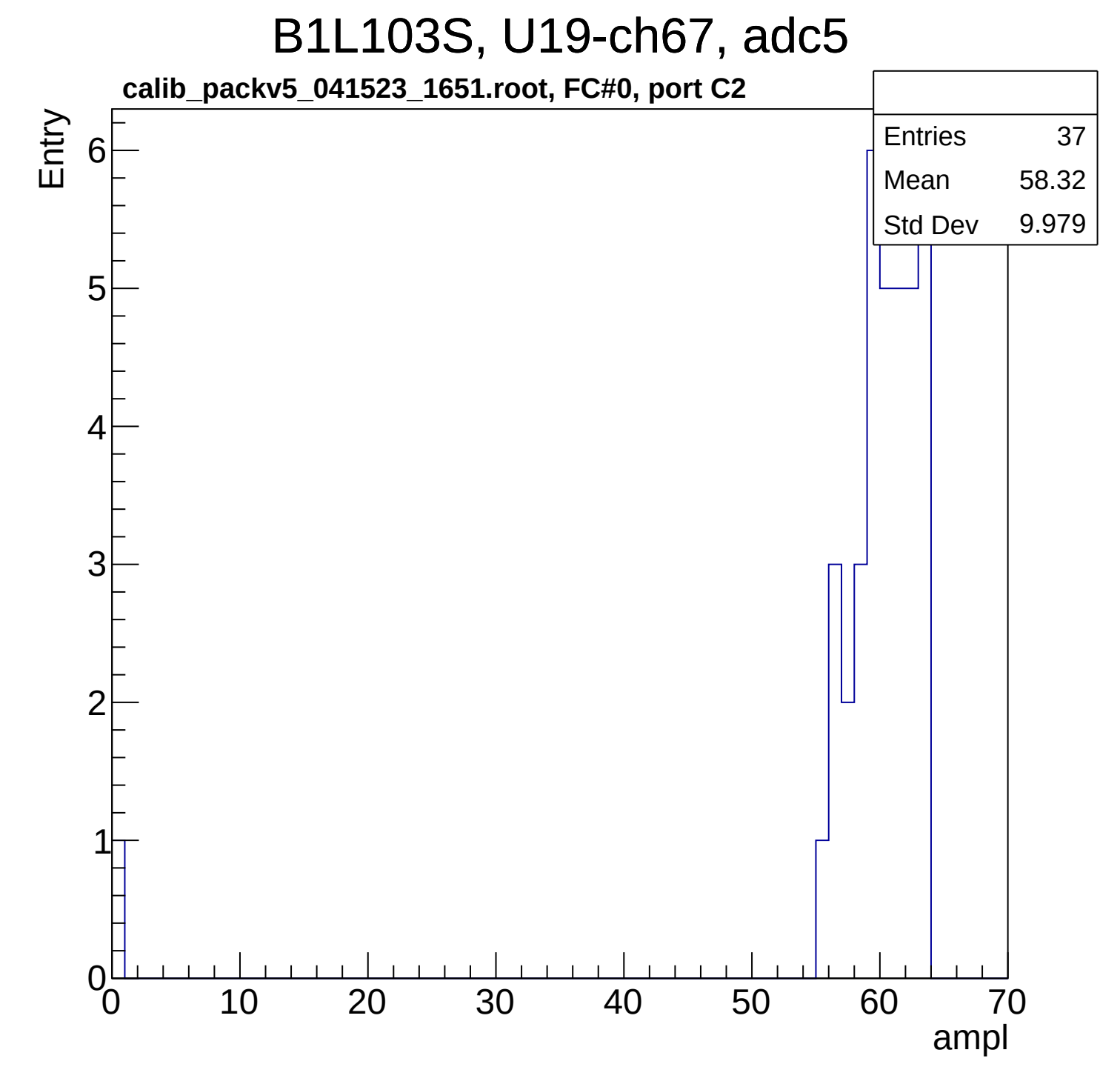

B1L103S, U19-ch67, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 22.07
Std Dev 13.86
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl

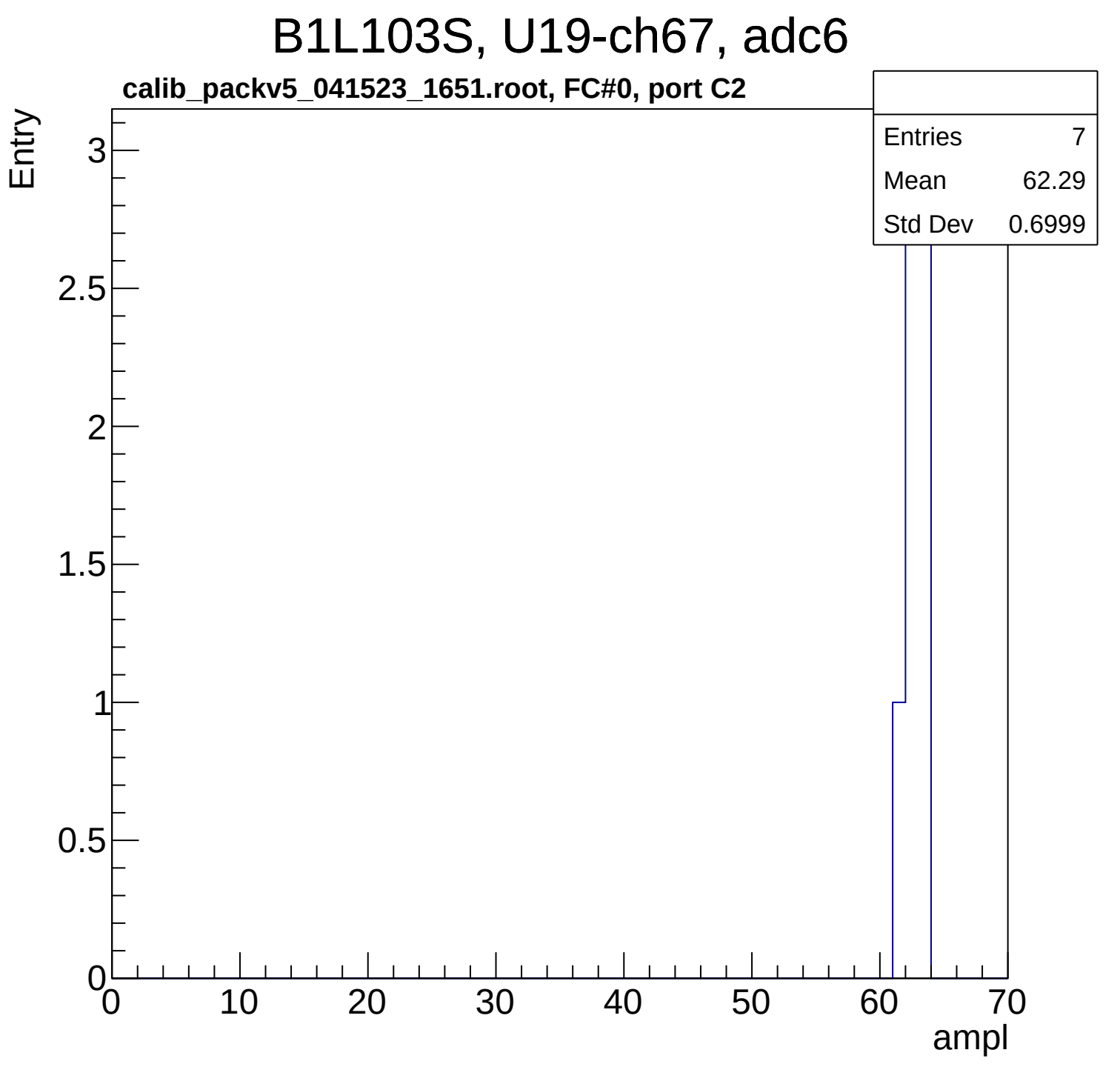

B1L103S, U19-ch67, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 34.74
Std Dev 7.251
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch67, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 36.39
Std Dev 15.38
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch67, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 50.2
Std Dev 3.892
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch67, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 56.25
Std Dev 3.453
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch67, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 58.32
Std Dev 9.979
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U19-ch67, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 62.29
Std Dev 0.6999
Entry
ampl
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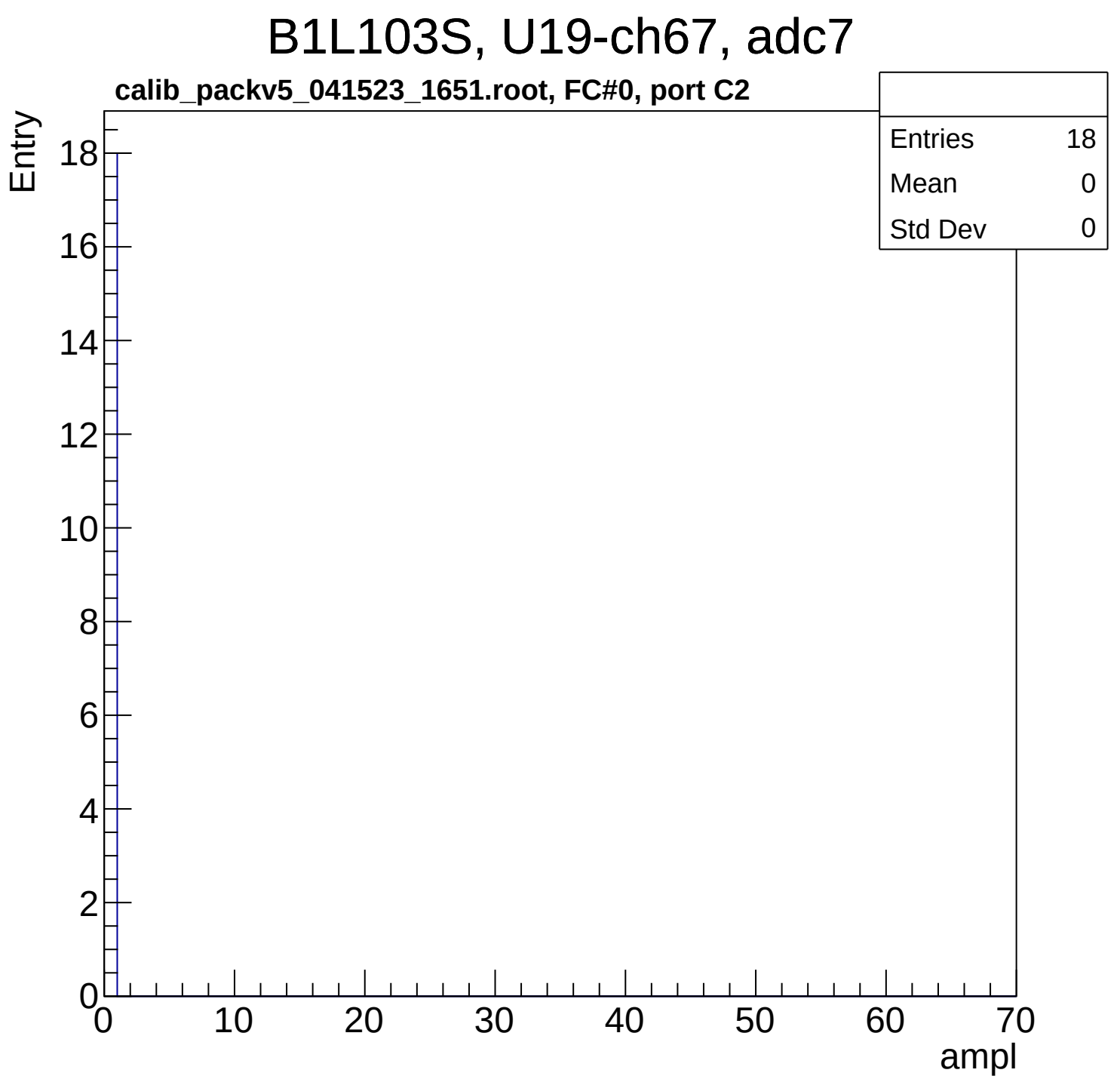
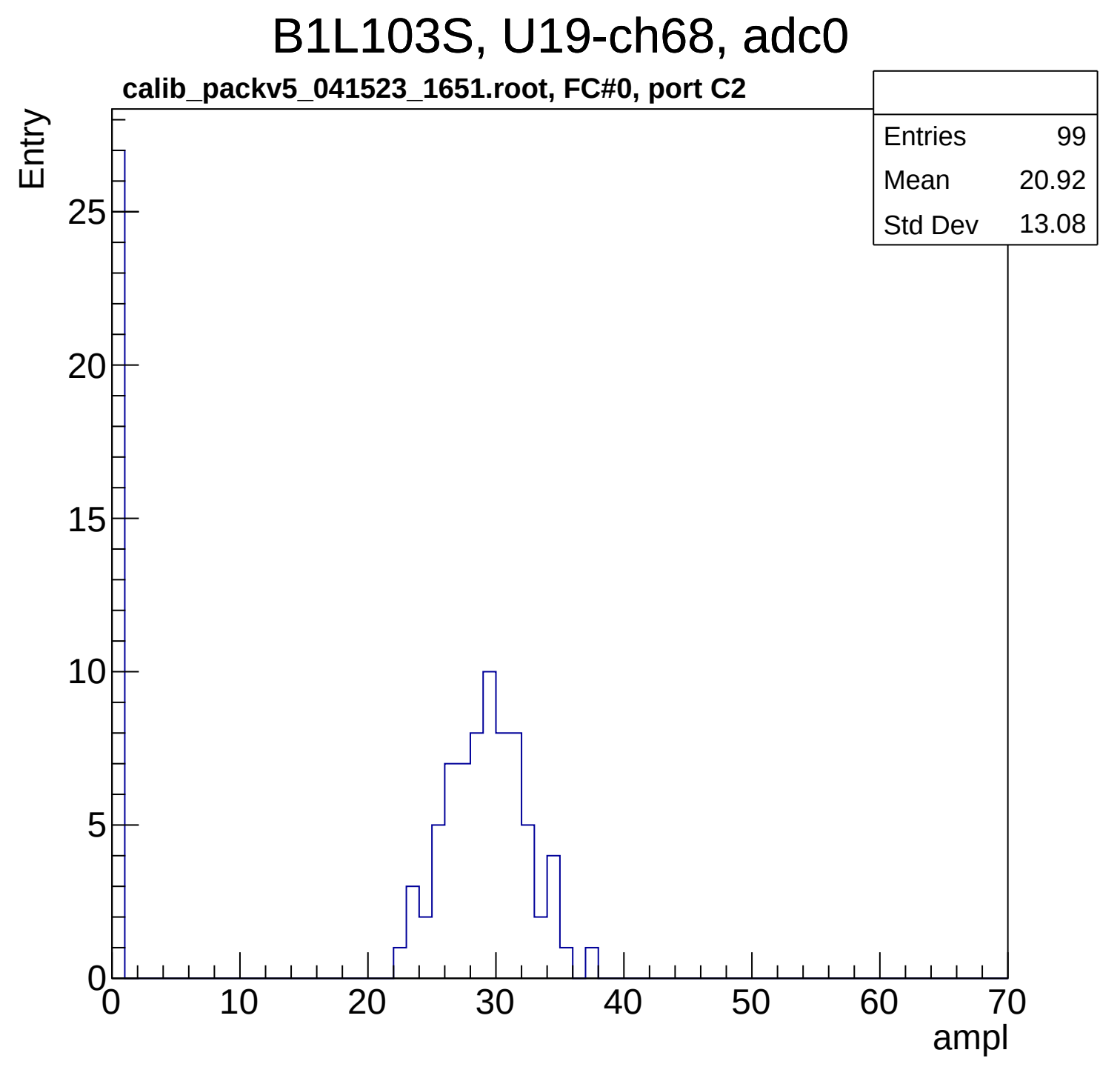
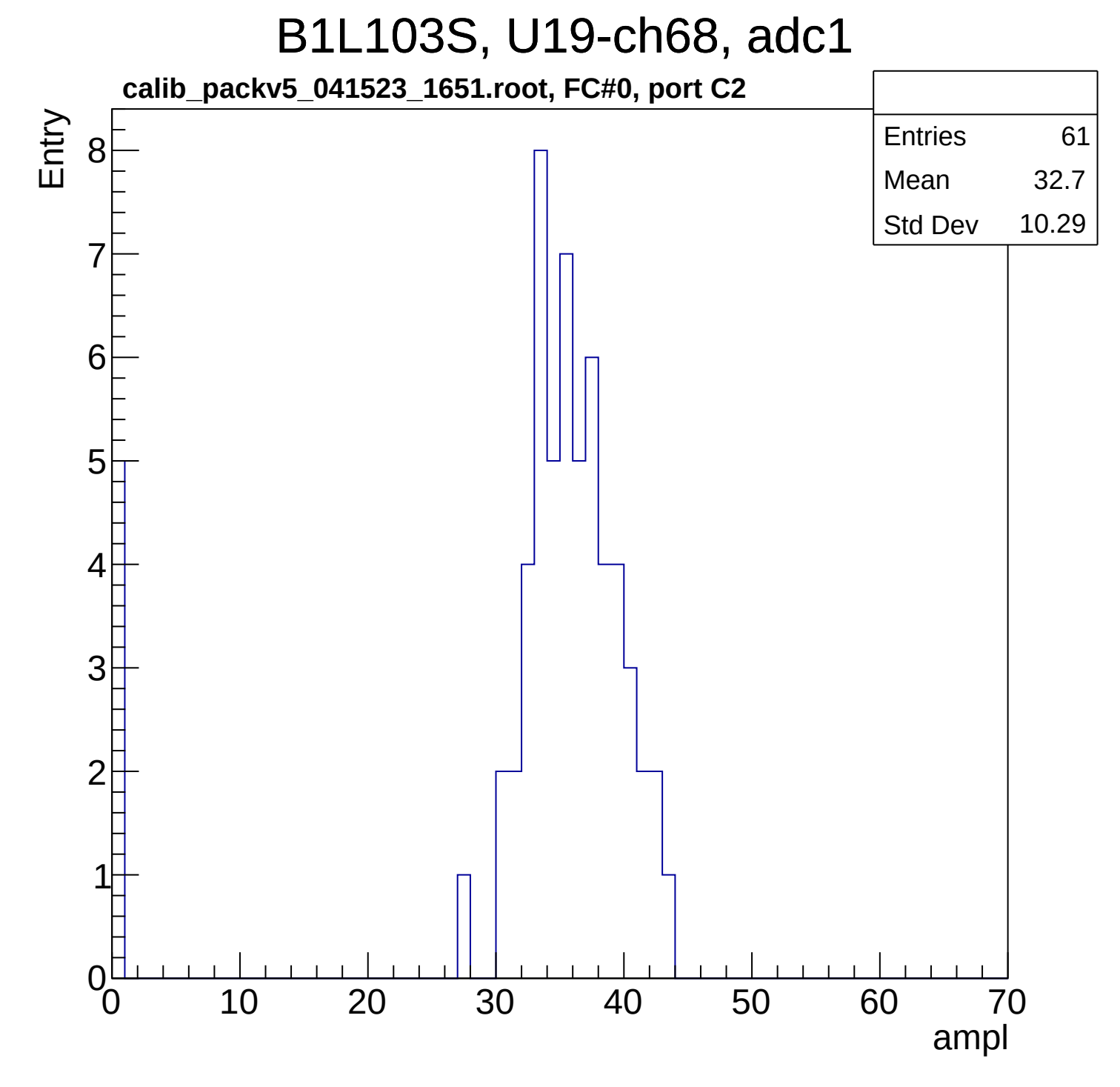
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U19-ch67, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch68, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 20.92
Std Dev 13.08
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch68, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 32.7
Std Dev 10.29
Entry
ampl
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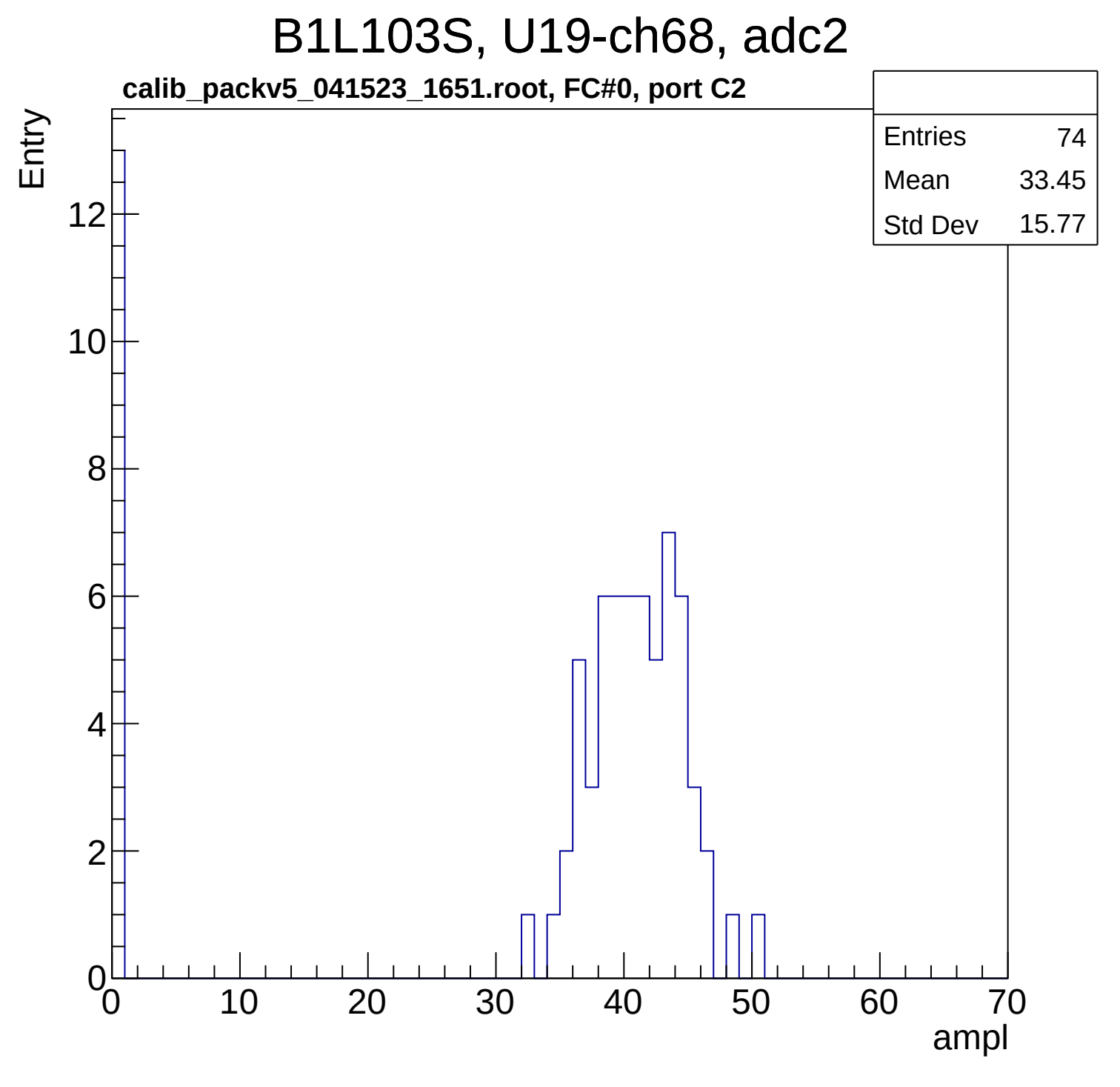
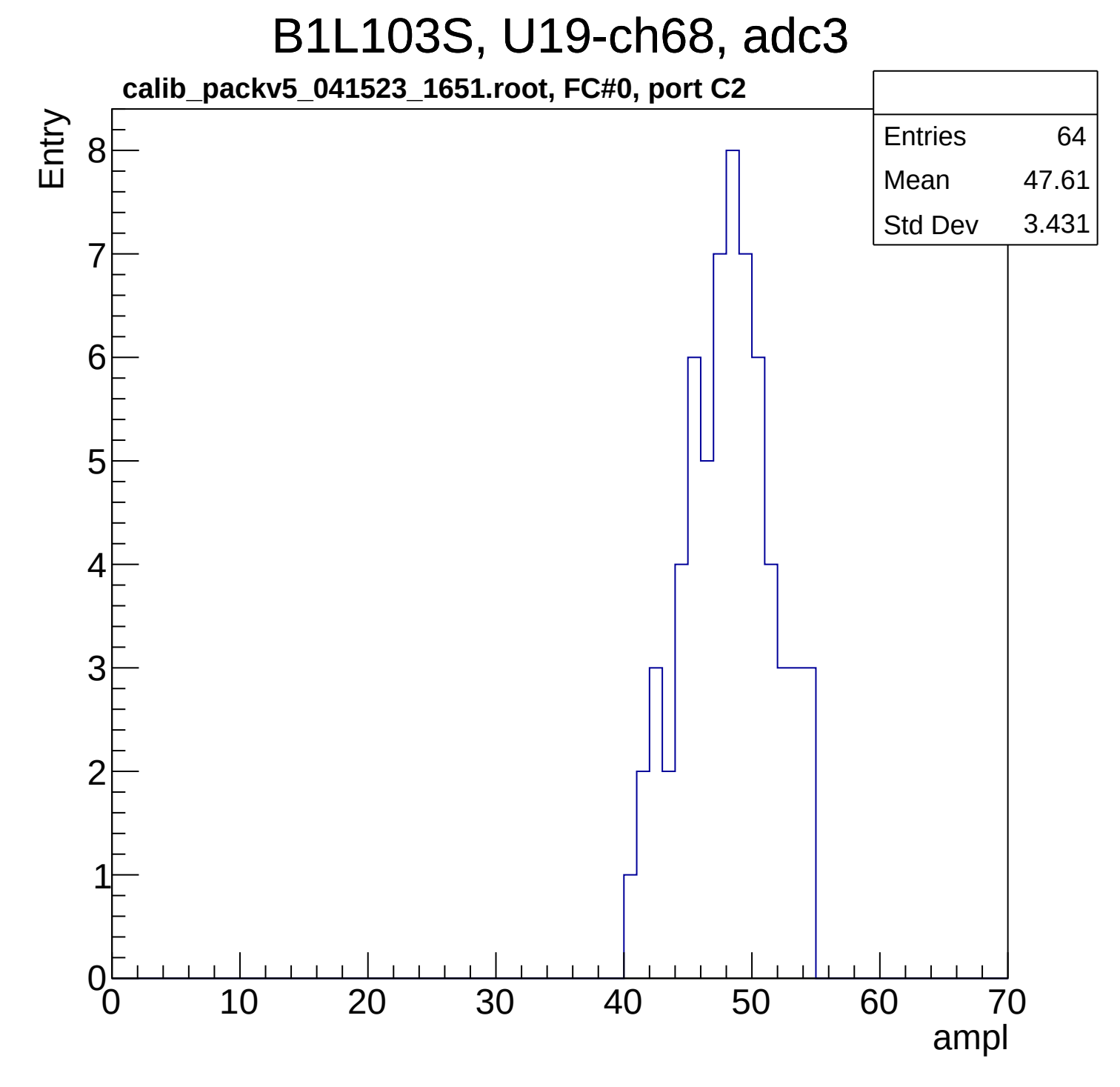
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch68, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 33.45
Std Dev 15.77
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch68, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 47.61
Std Dev 3.431
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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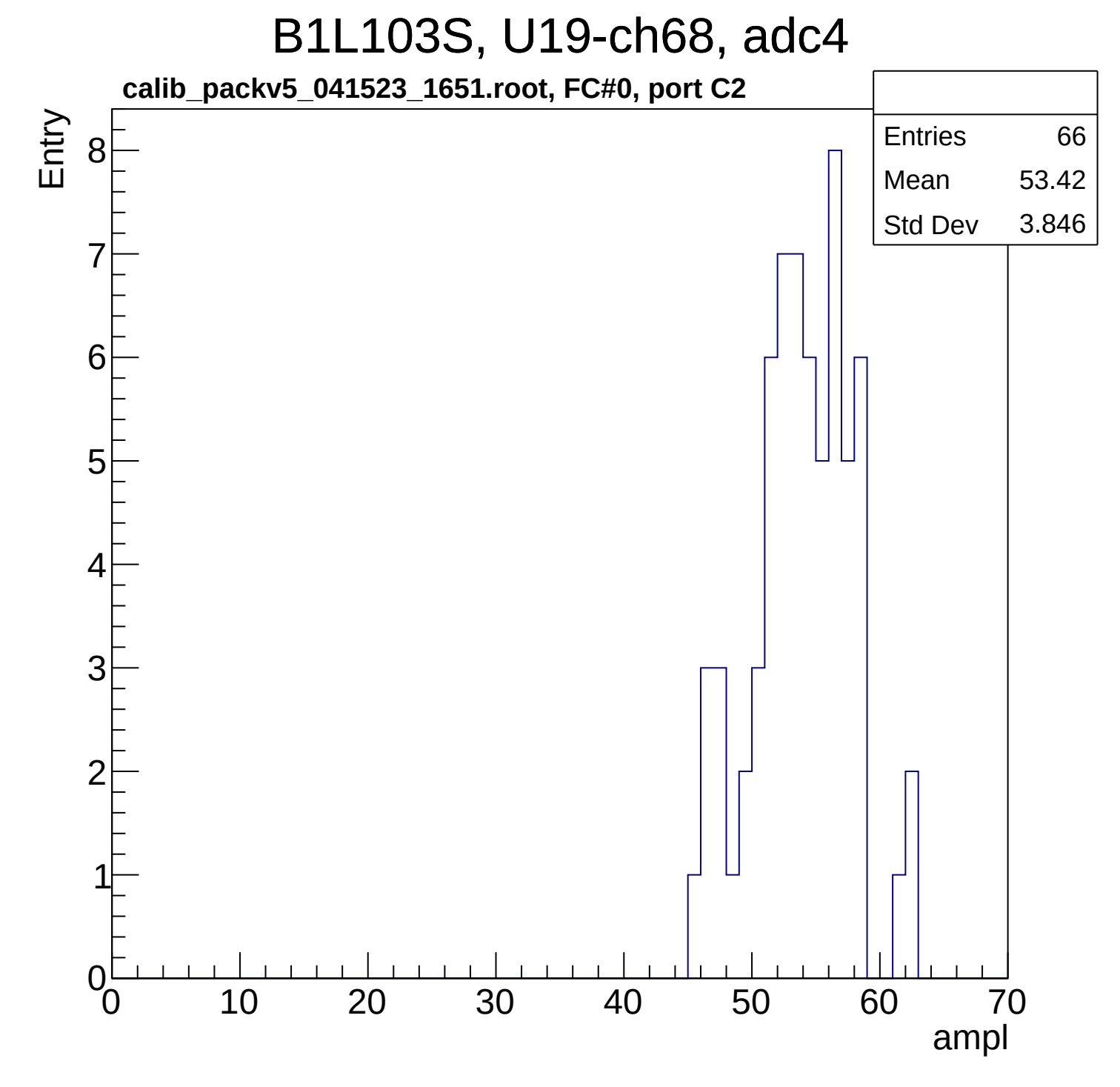
40
50
60
70


B1L103S, U19-ch68, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 53.42
Std Dev 3.846
Entry
ampl
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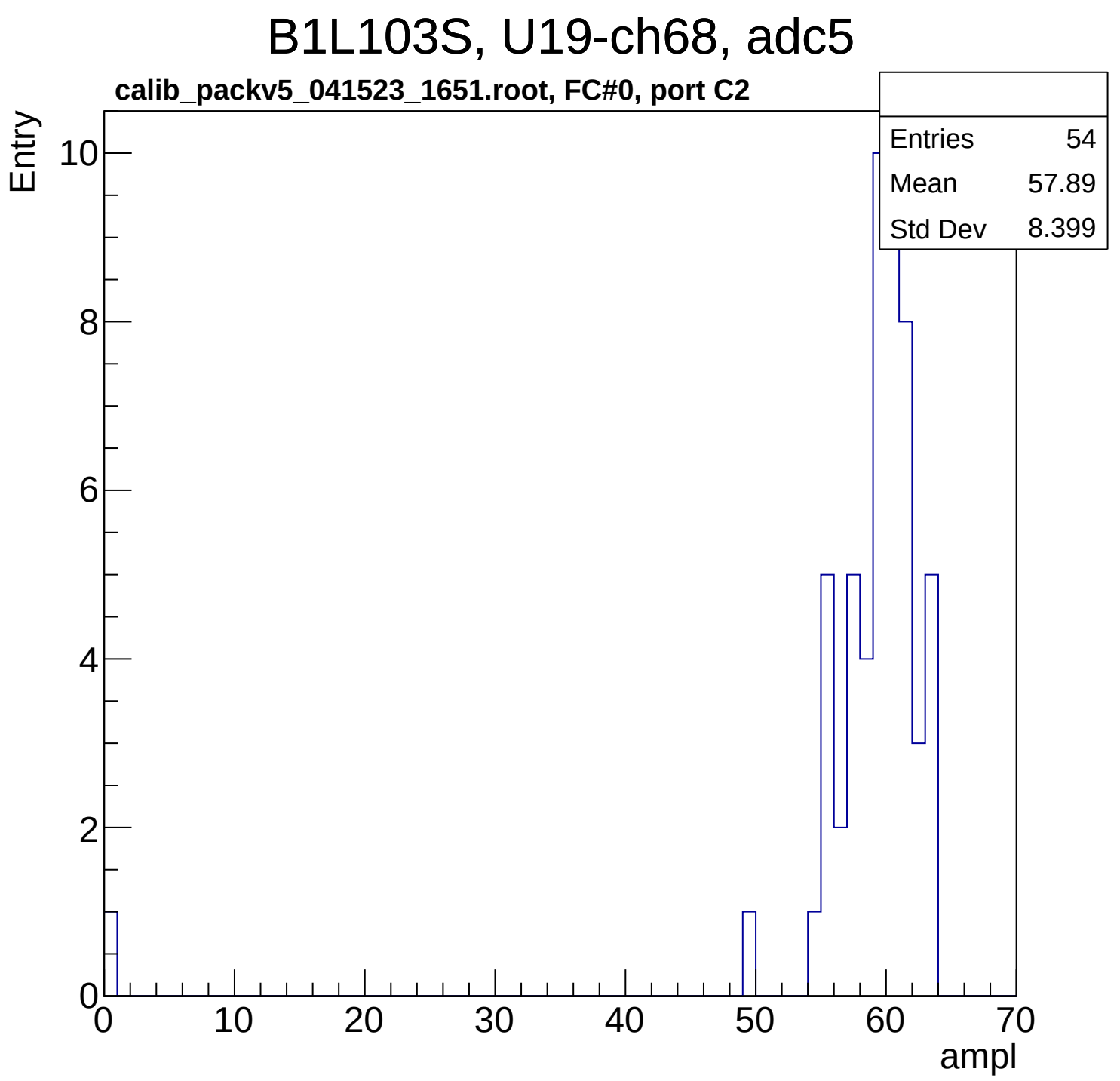
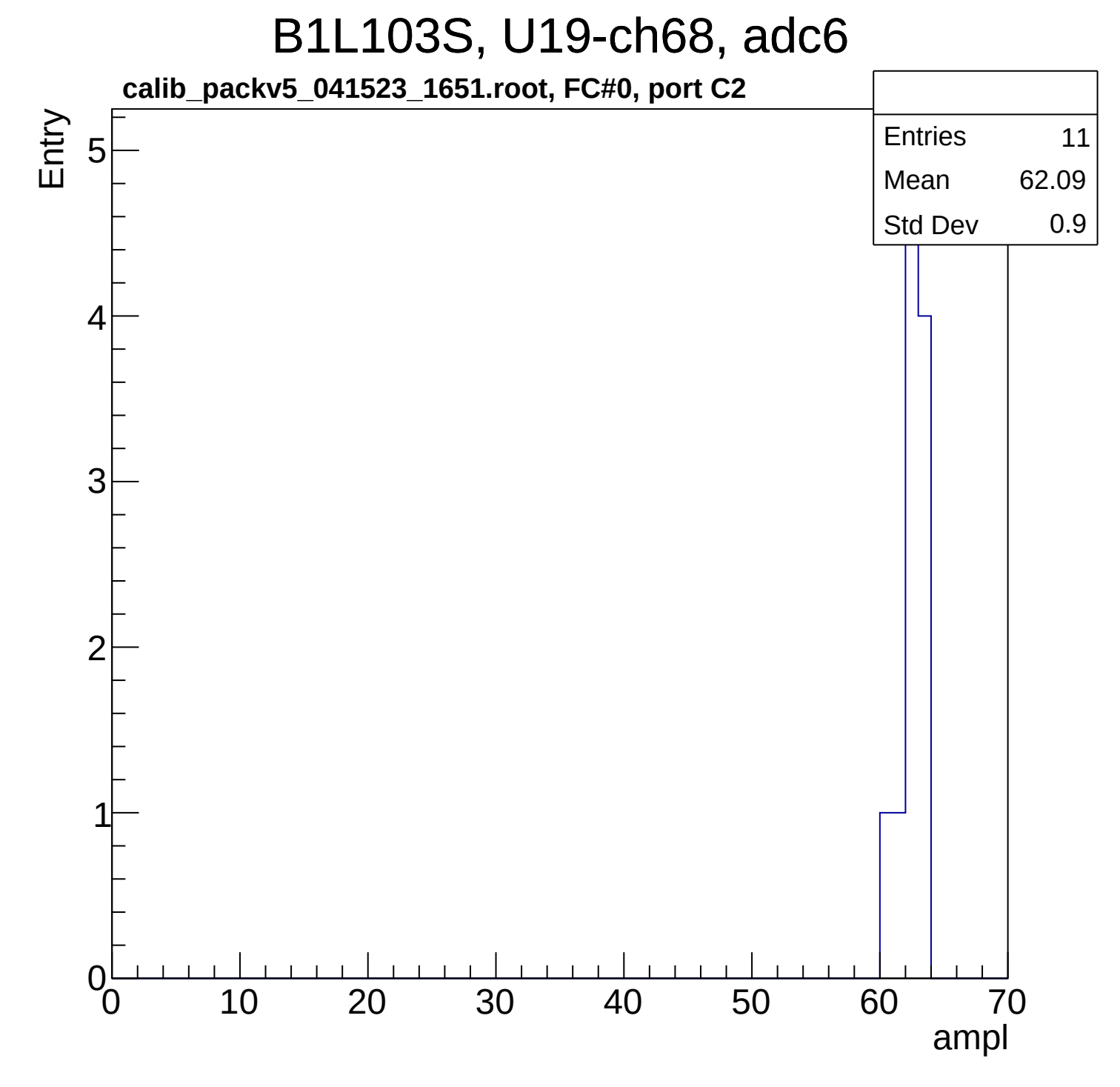
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch68, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 57.89
Std Dev 8.399
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch68, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 62.09
Std Dev 0.9
Entry
ampl
0
1
2
3
4
5
0
10
20
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40
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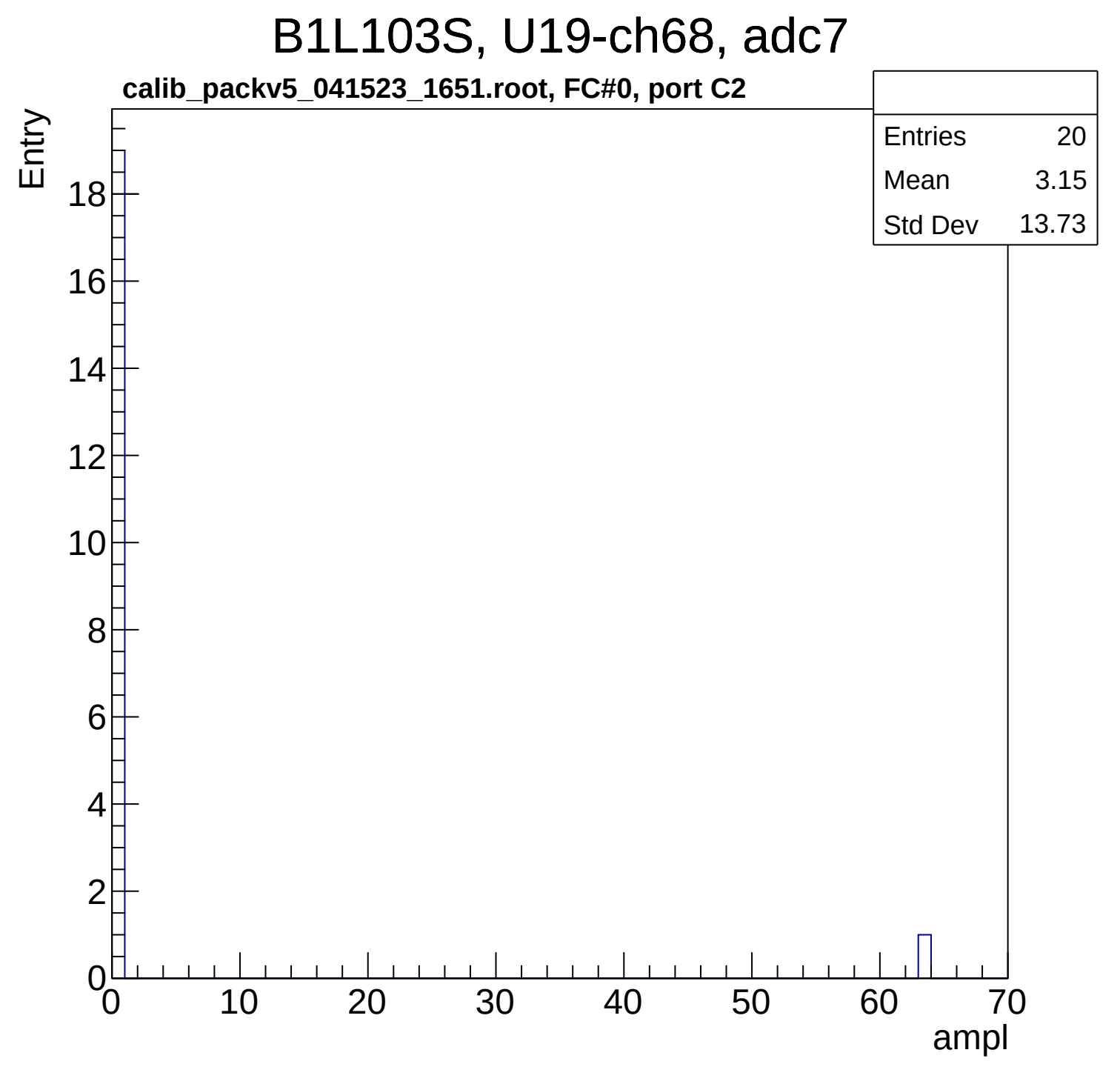
60
70


B1L103S, U19-ch68, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
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6
8
10
12
14
16
18
0
10
20
30
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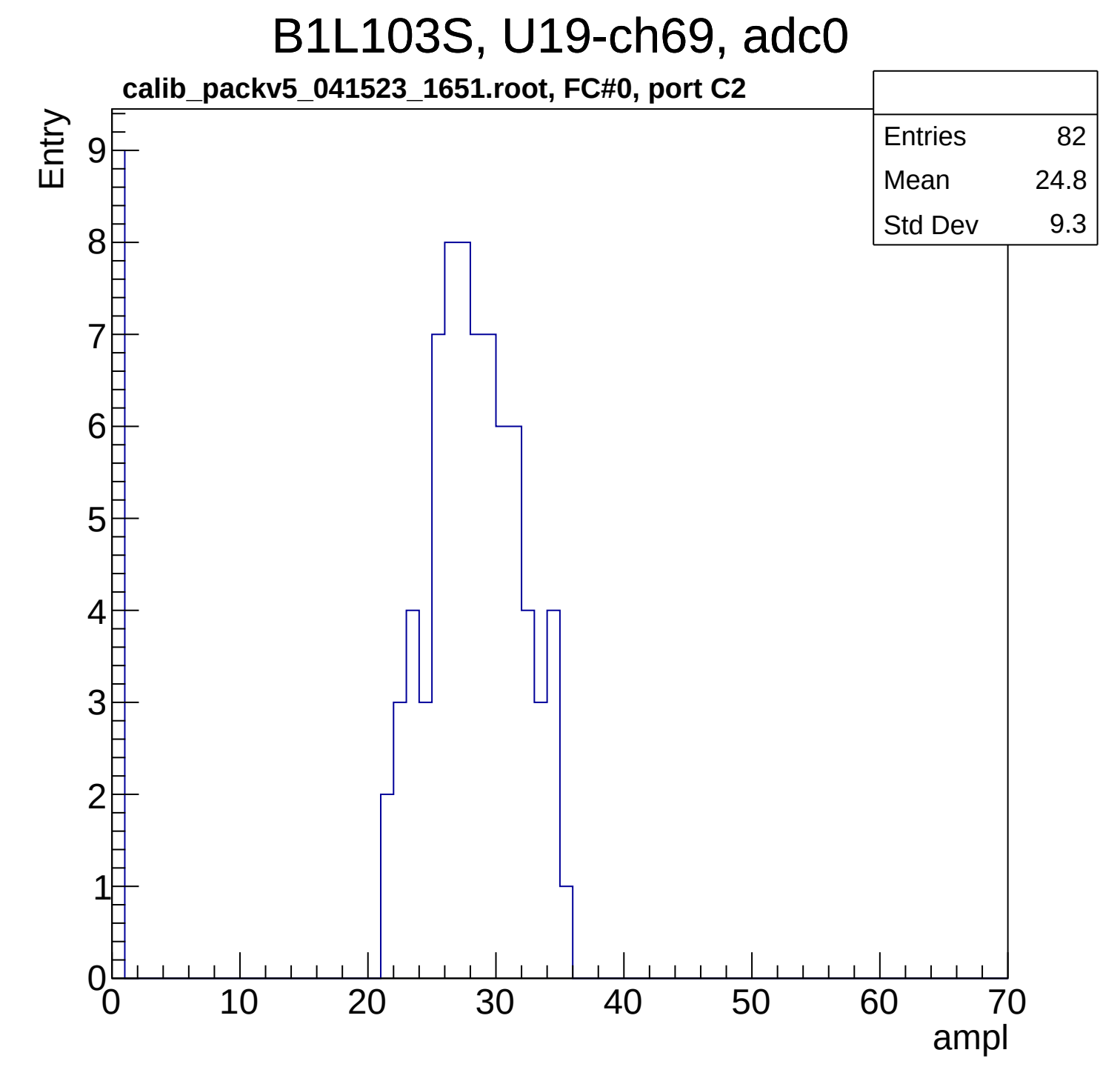
50
60
70
ampl


B1L103S, U19-ch69, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 24.8
Std Dev 9.3
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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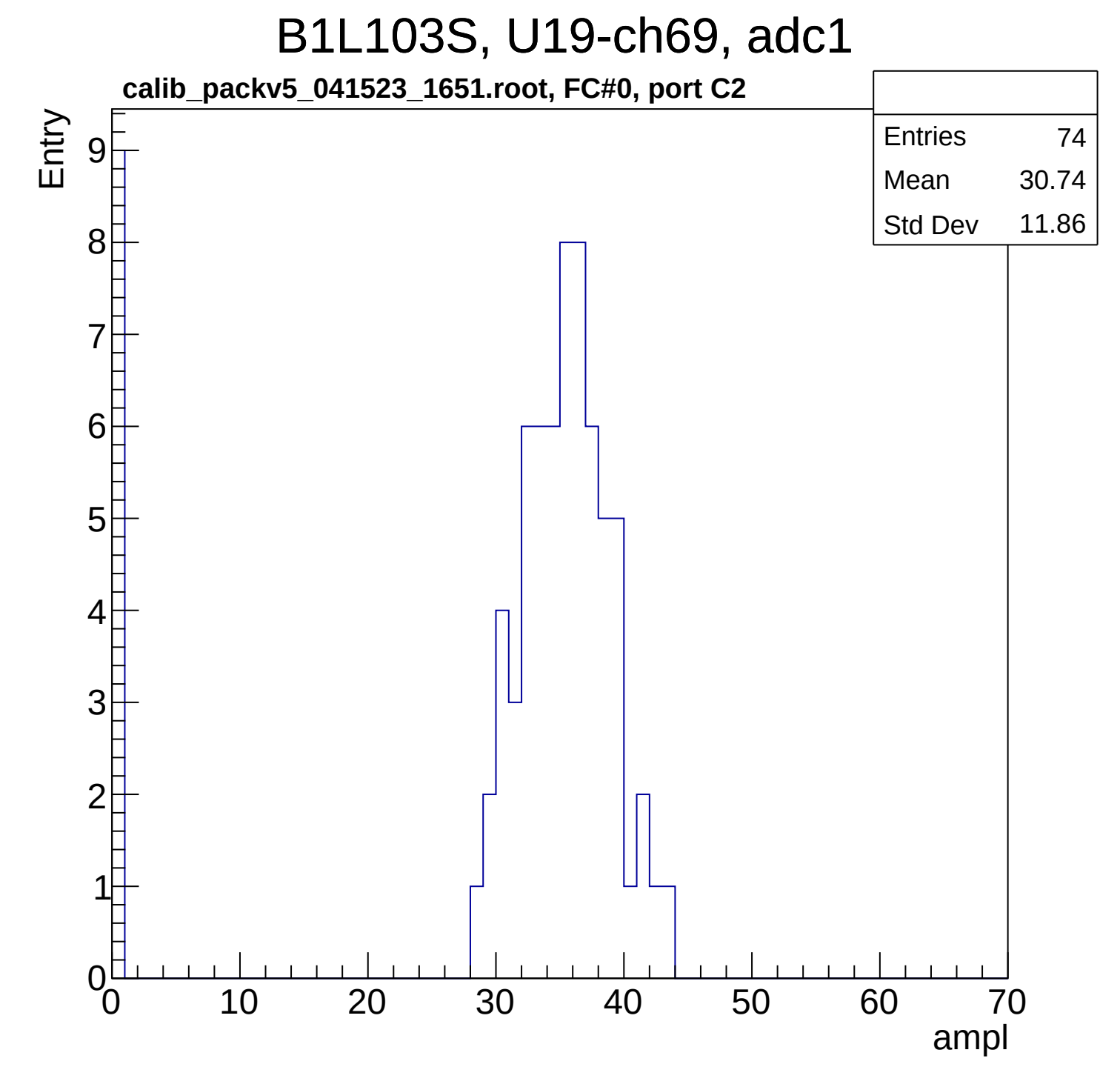
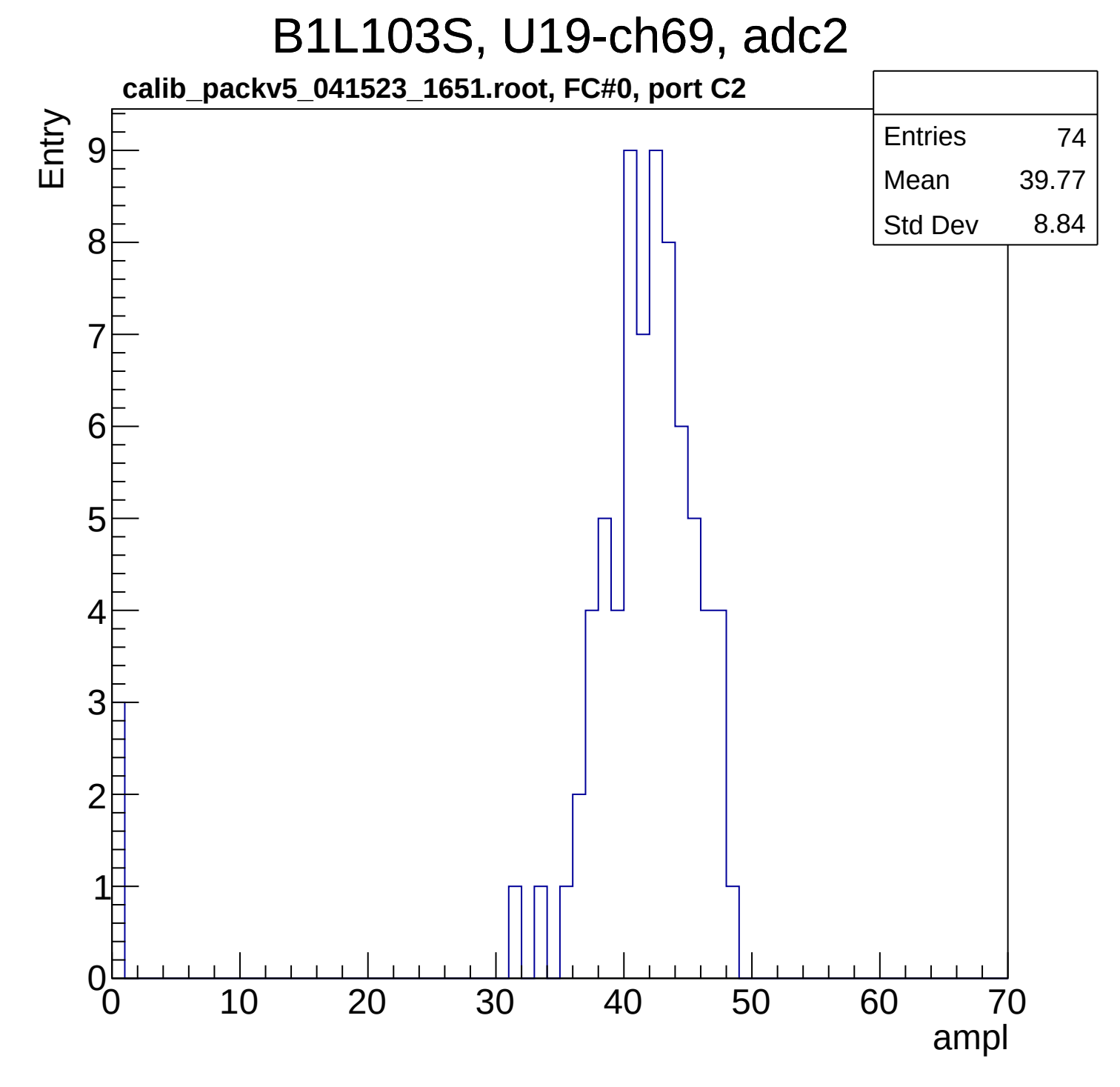

B1L103S, U19-ch69, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 30.74
Std Dev 11.86
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch69, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 39.77
Std Dev 8.84
Entry
ampl
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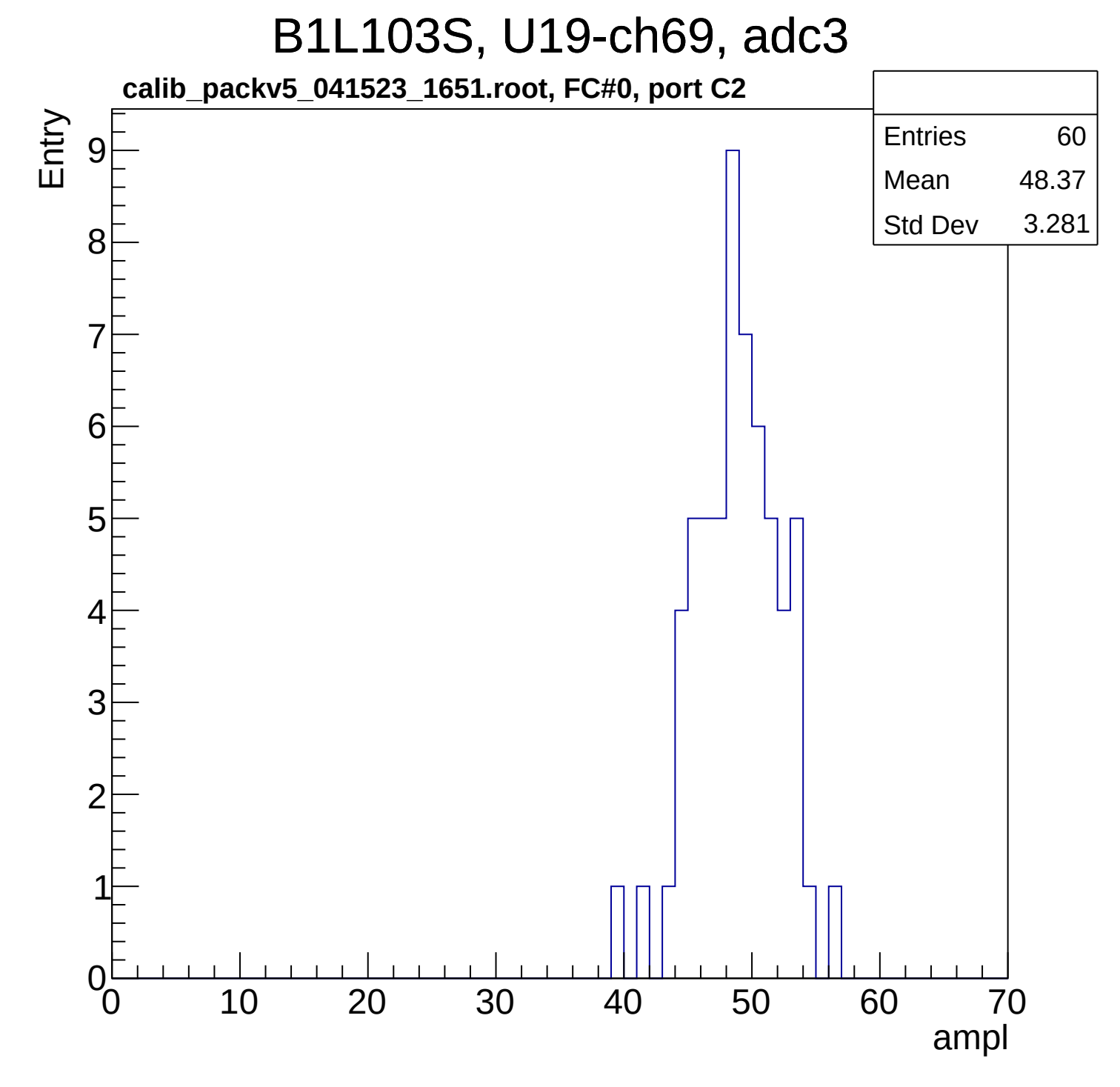
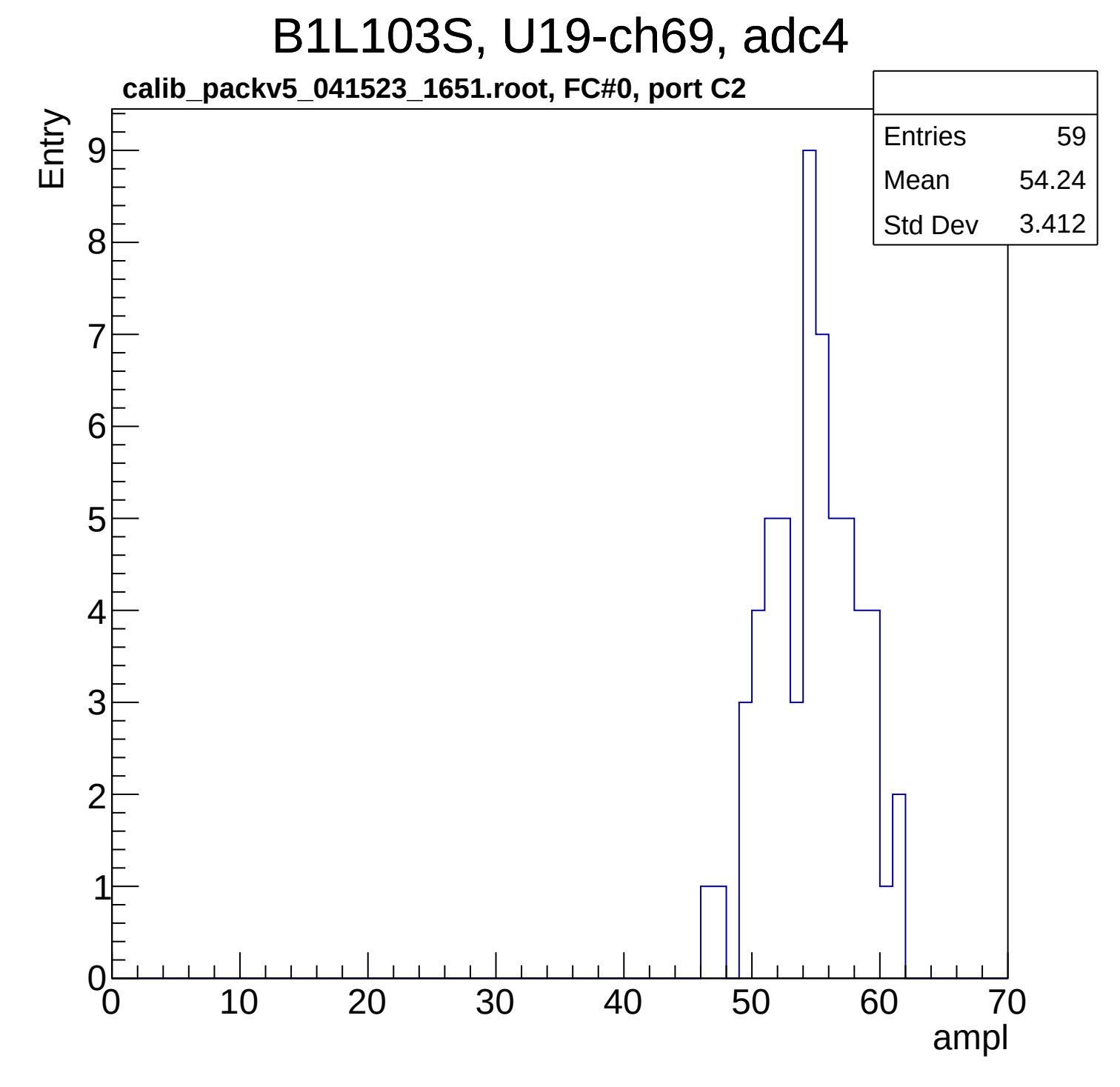
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch69, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 48.37
Std Dev 3.281
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch69, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 54.24
Std Dev 3.412
Entry
ampl
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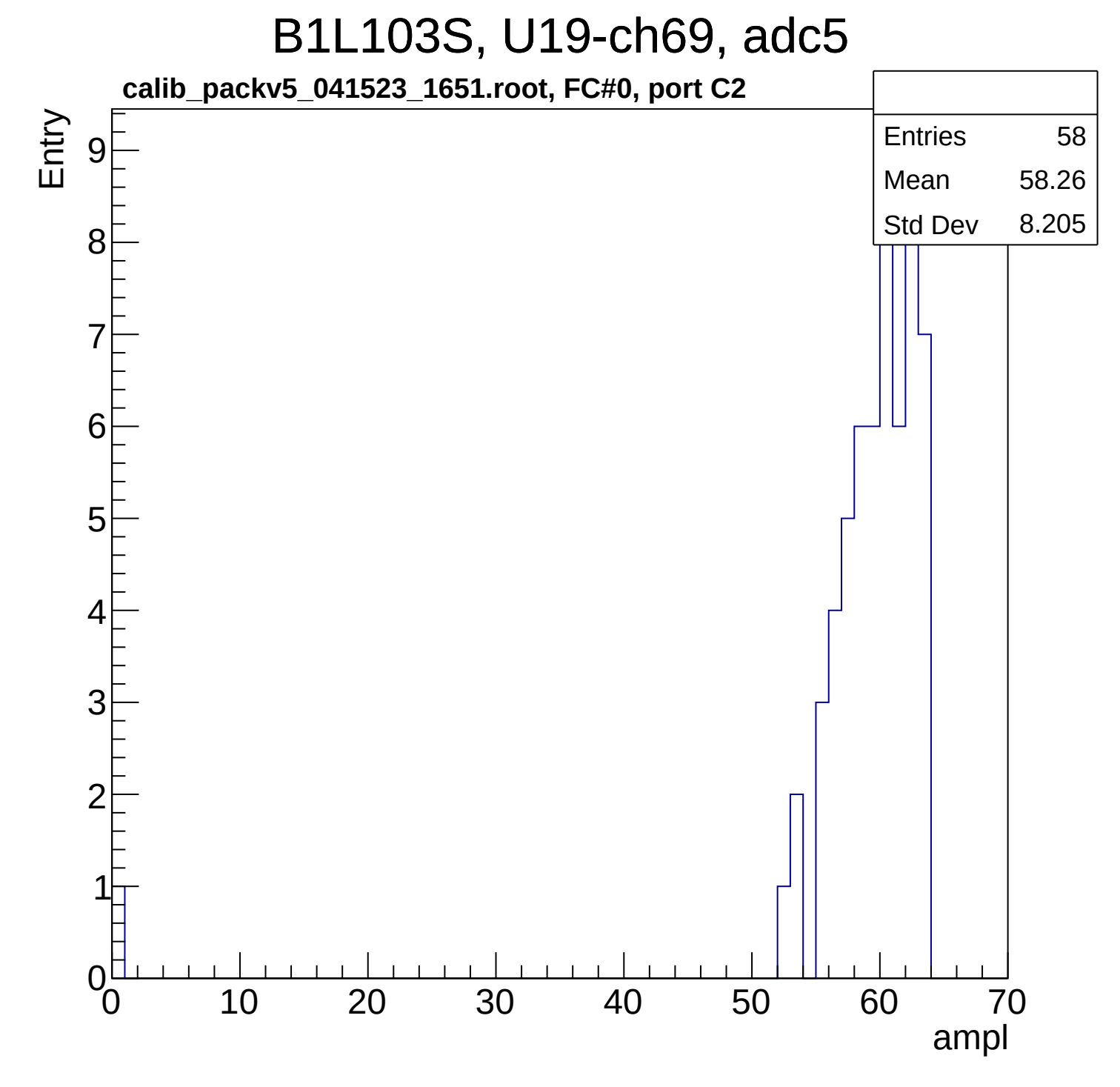
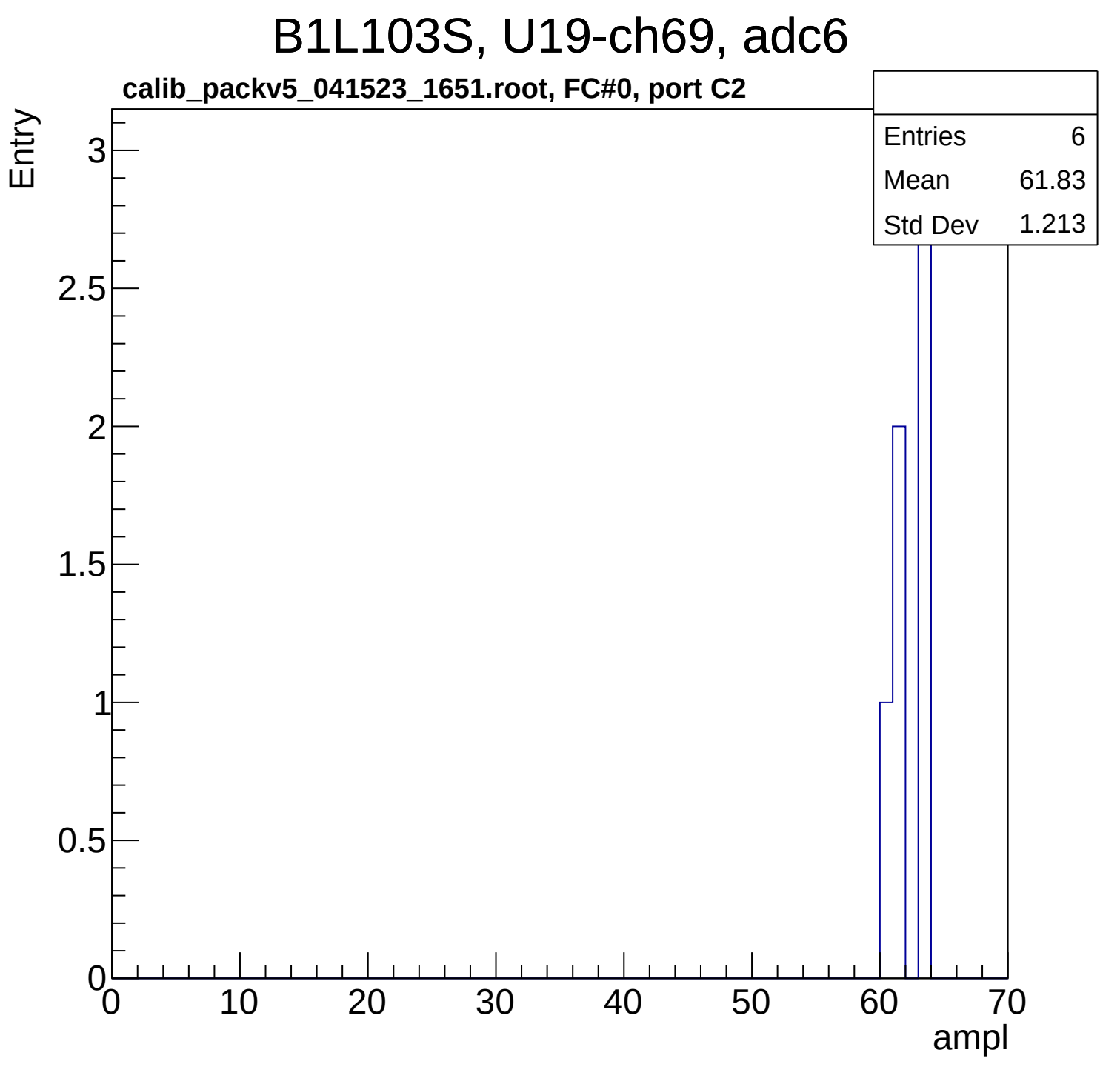
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch69, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 58.26
Std Dev 8.205
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch69, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 61.83
Std Dev 1.213
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
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40
50
60
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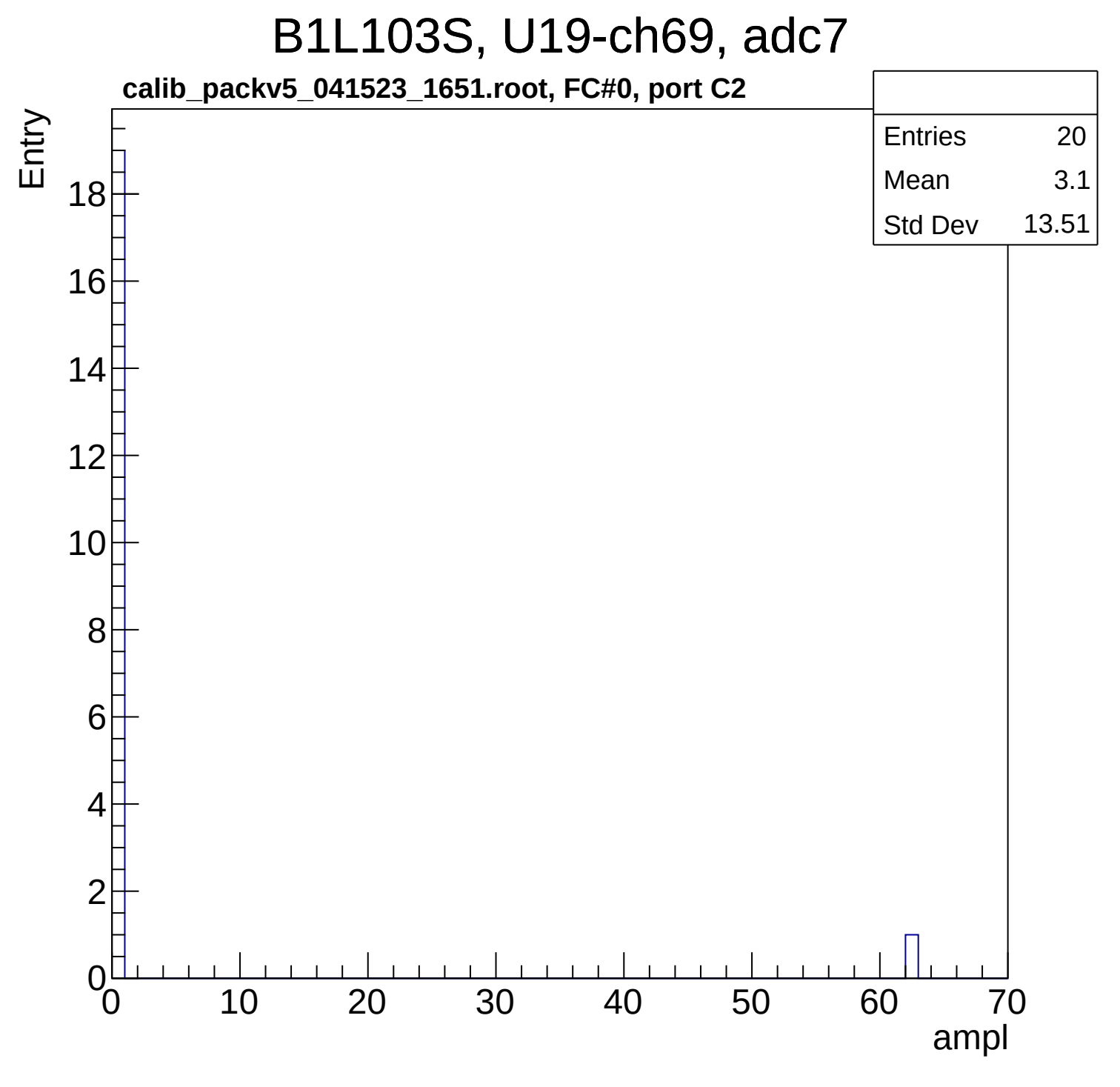
B1L103S, U19-ch69, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
2
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6
8
10
12
14
16
18
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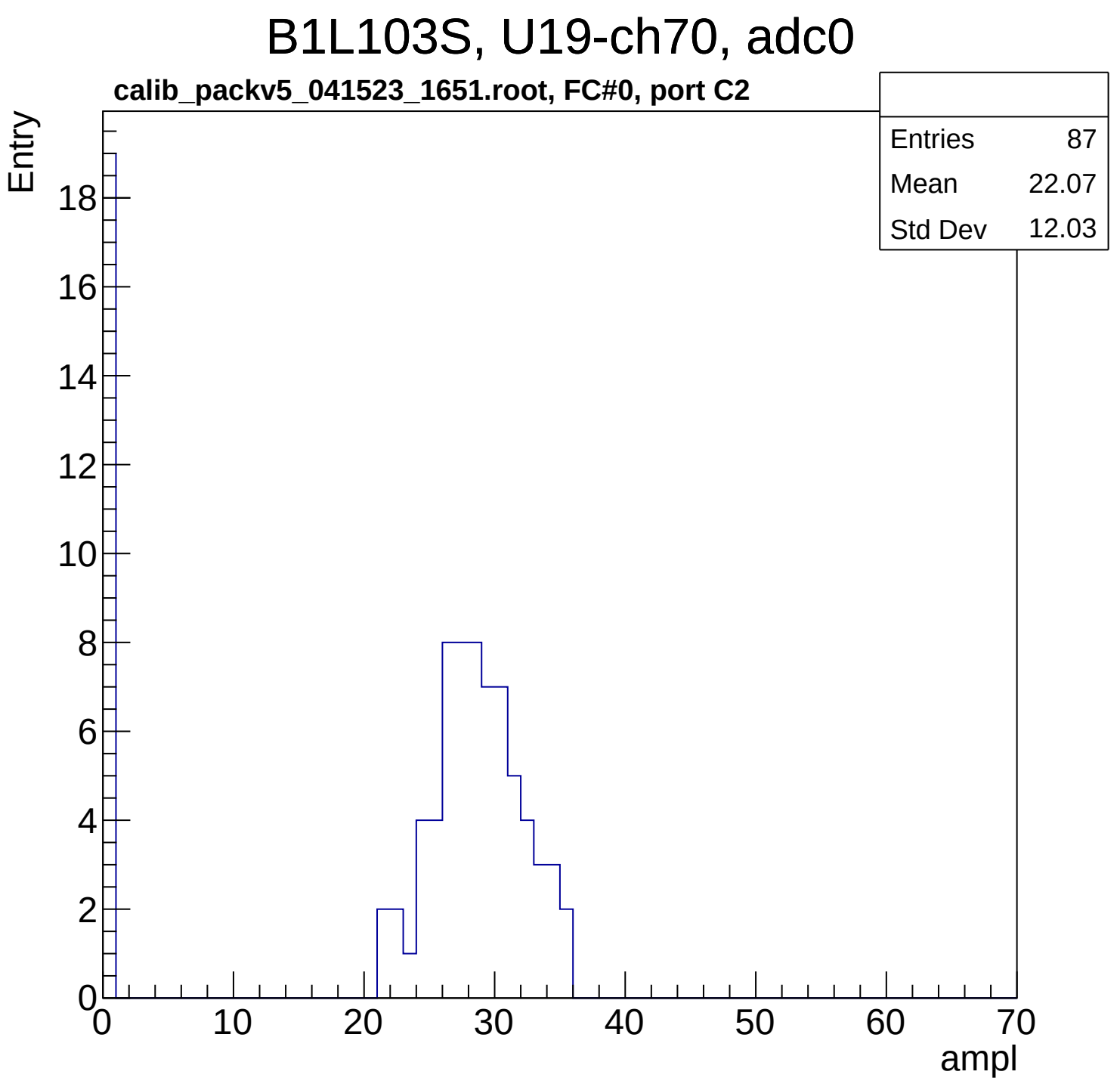
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch70, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 22.07
Std Dev 12.03
Entry
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2
4
6
8
10
12
14
16
18
0
10
20
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50
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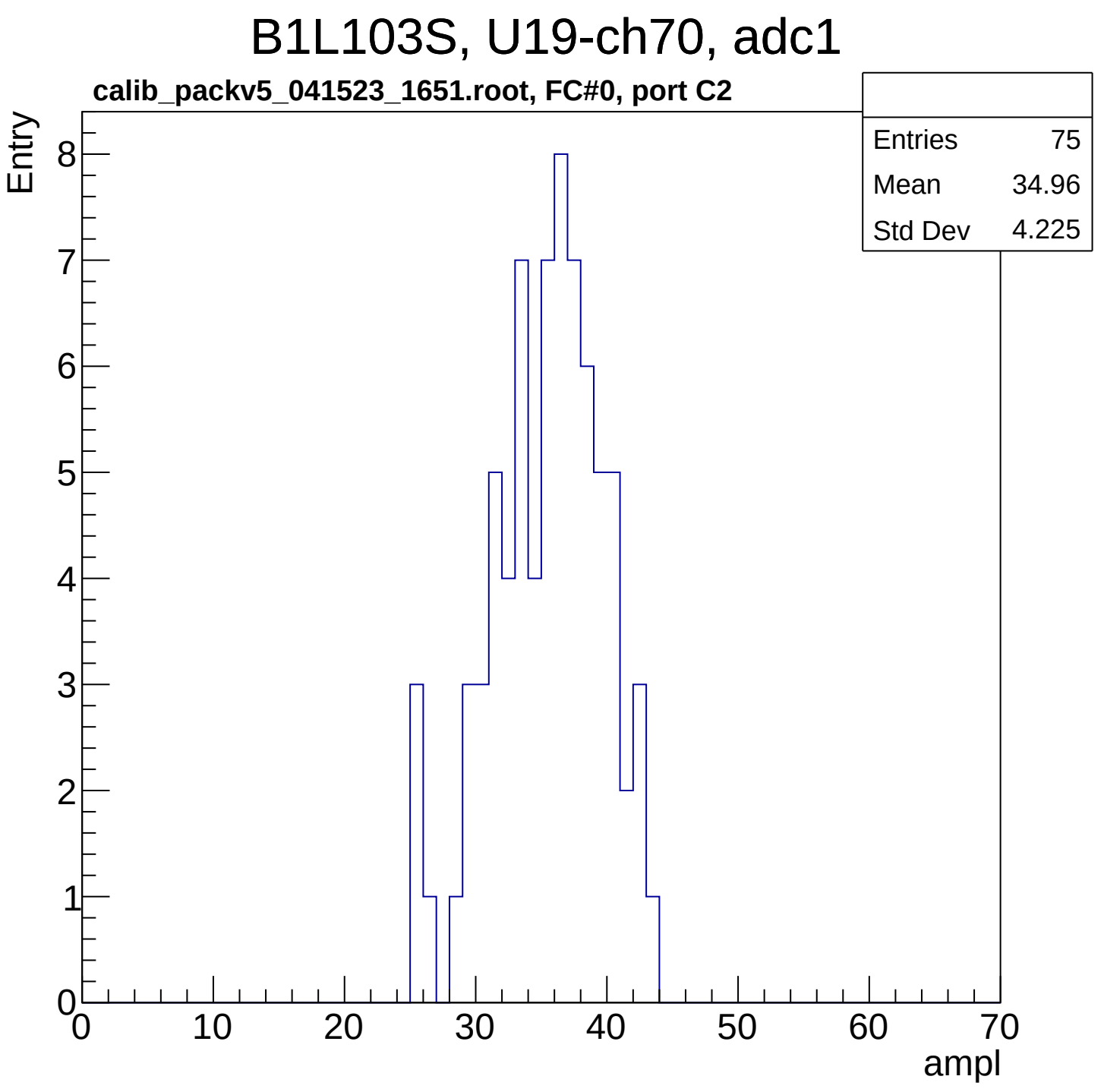
70
ampl


B1L103S, U19-ch70, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 34.96
Std Dev 4.225
Entry
ampl
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1
2
3
4
5
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7
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0
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60
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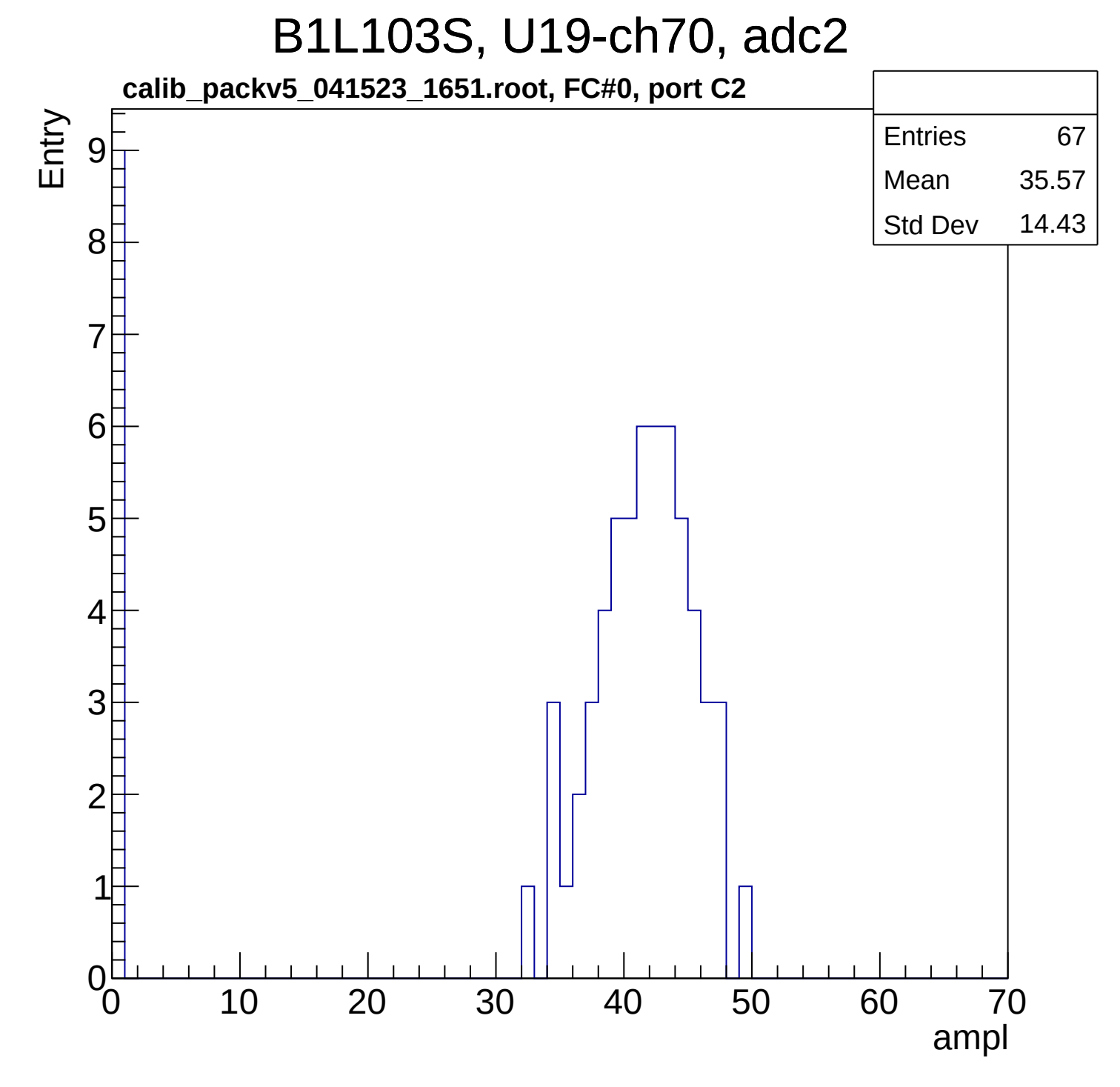
B1L103S, U19-ch70, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 35.57
Std Dev 14.43
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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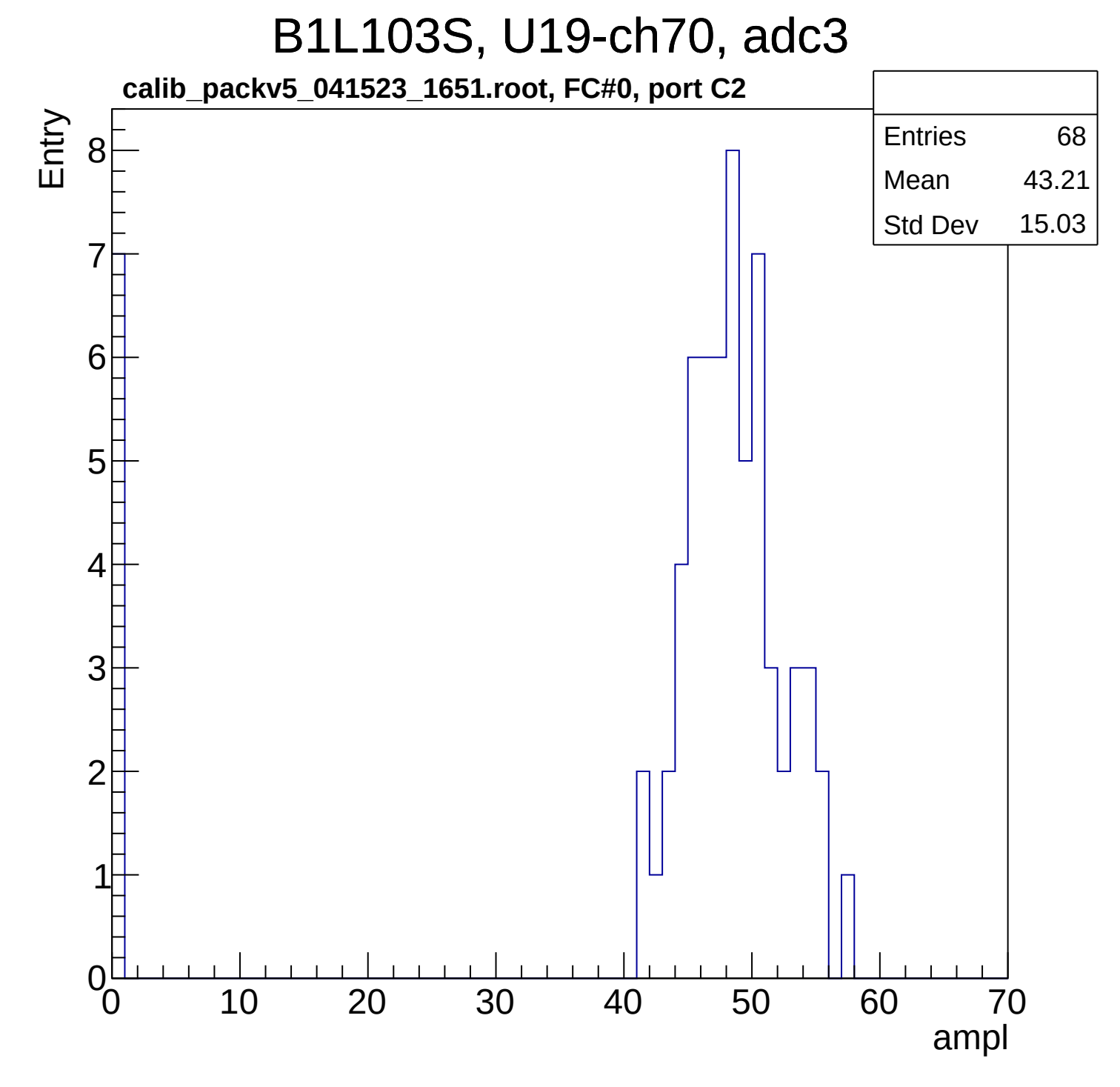
B1L103S, U19-ch70, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 43.21
Std Dev 15.03
Entry
ampl
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1
2
3
4
5
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7
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0
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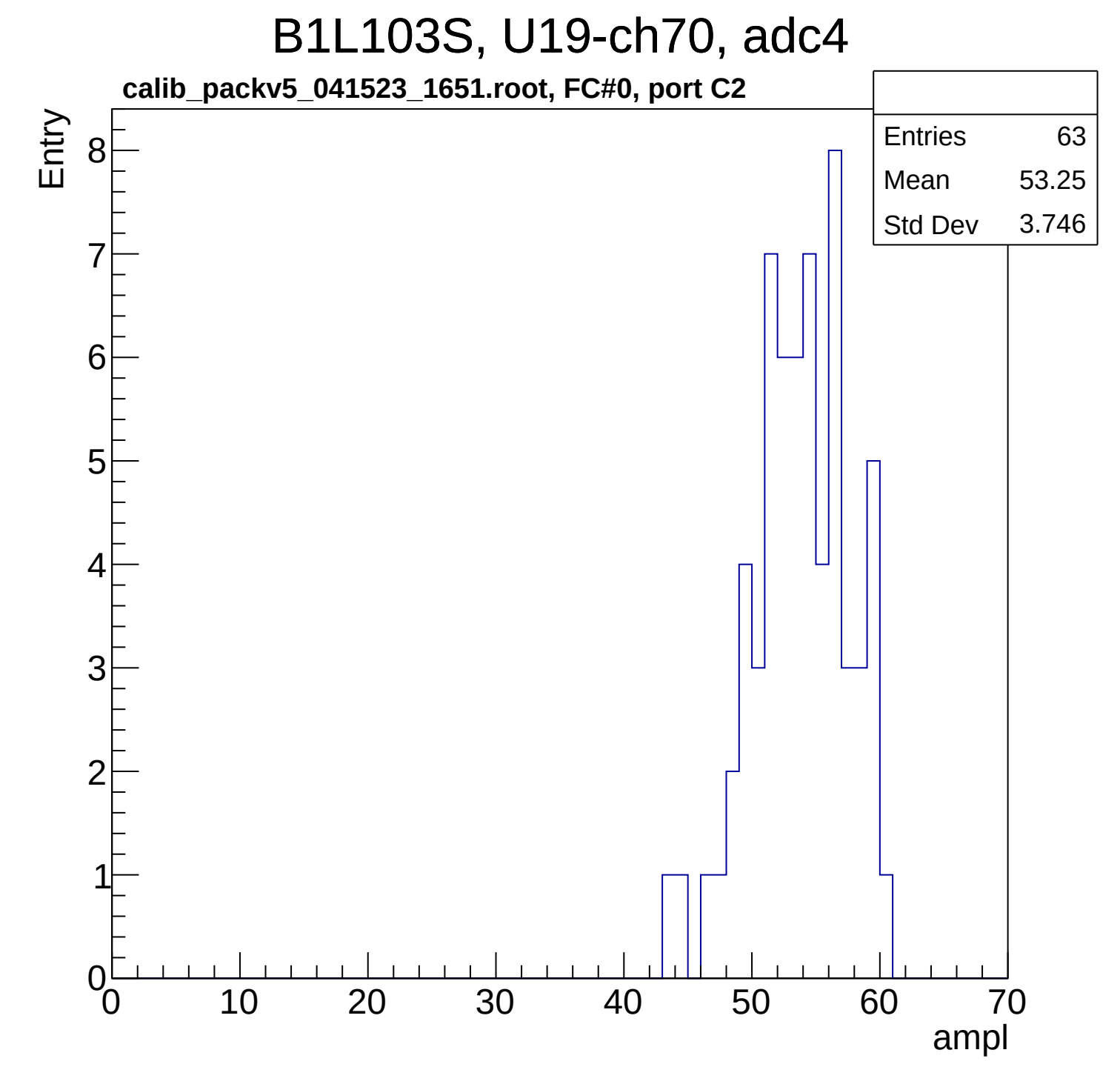
B1L103S, U19-ch70, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 53.25
Std Dev 3.746
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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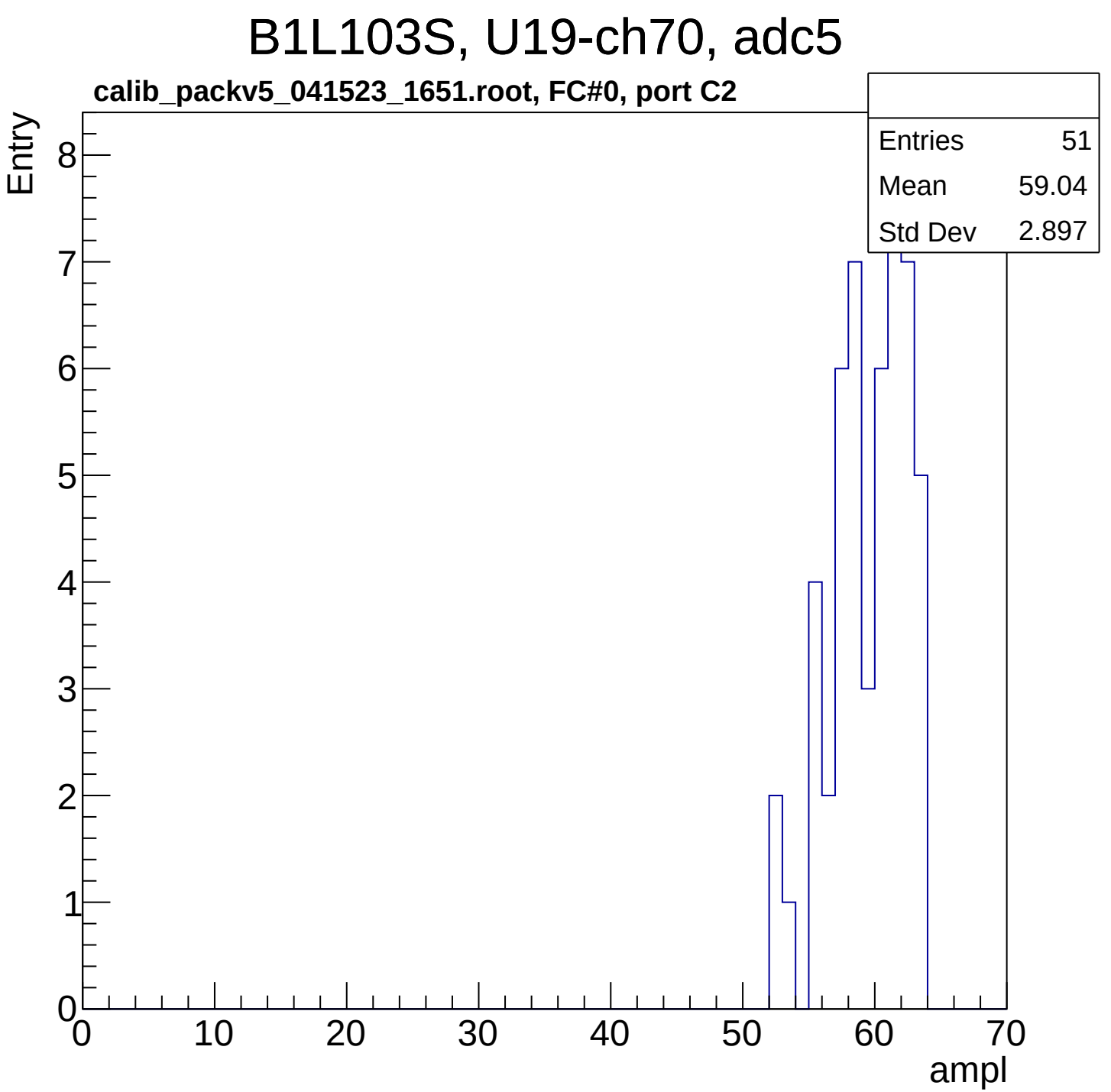
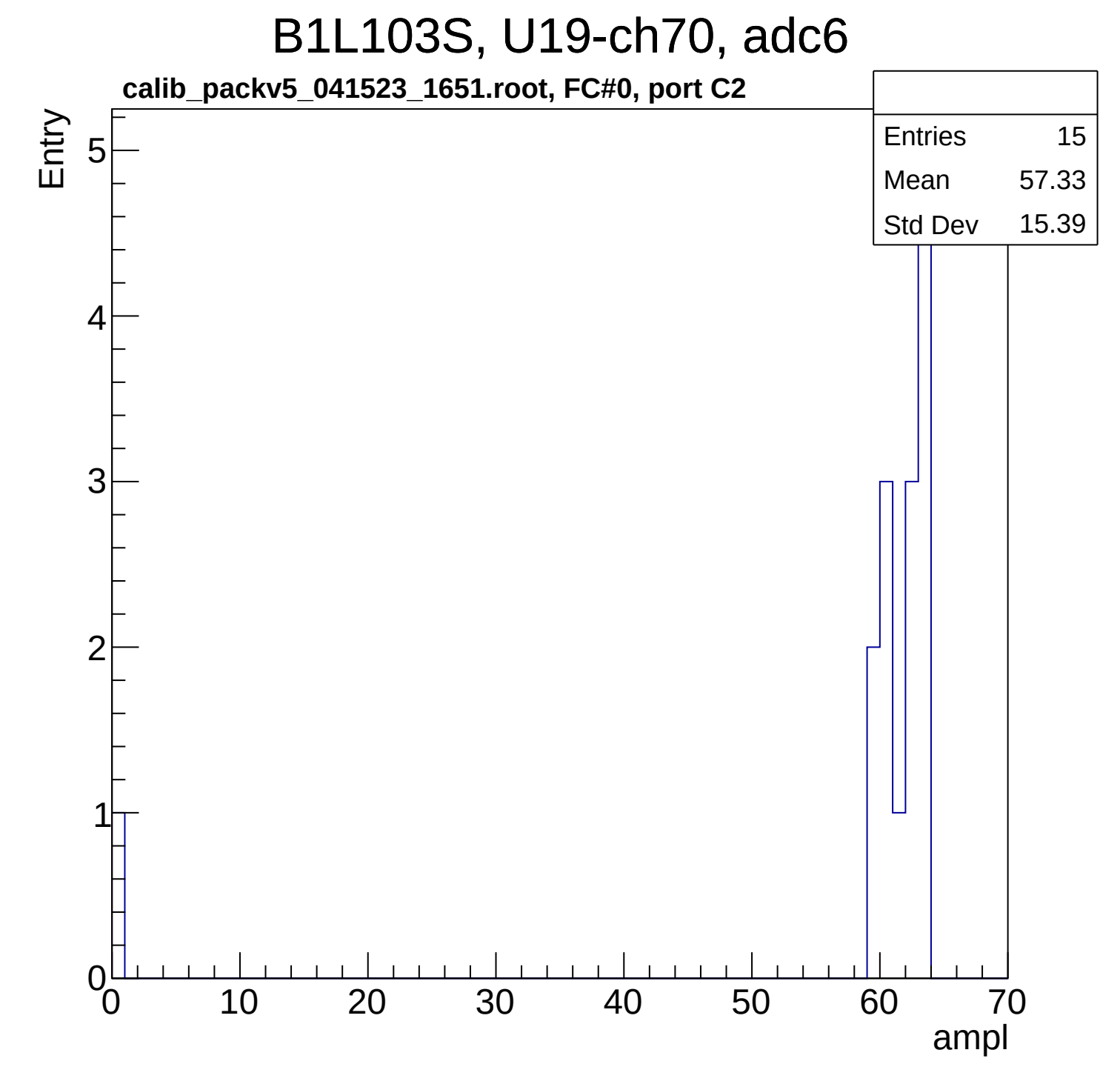
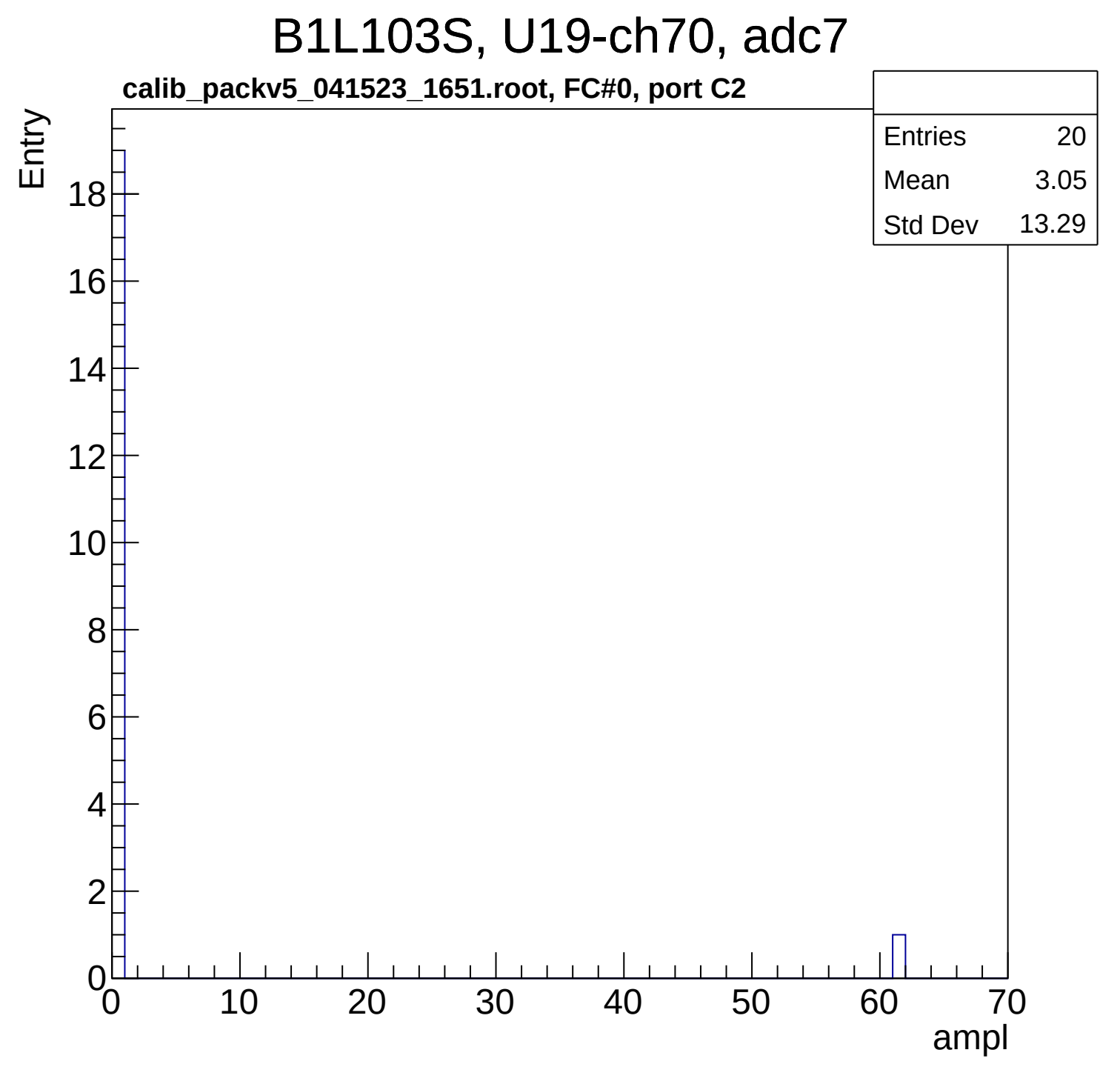
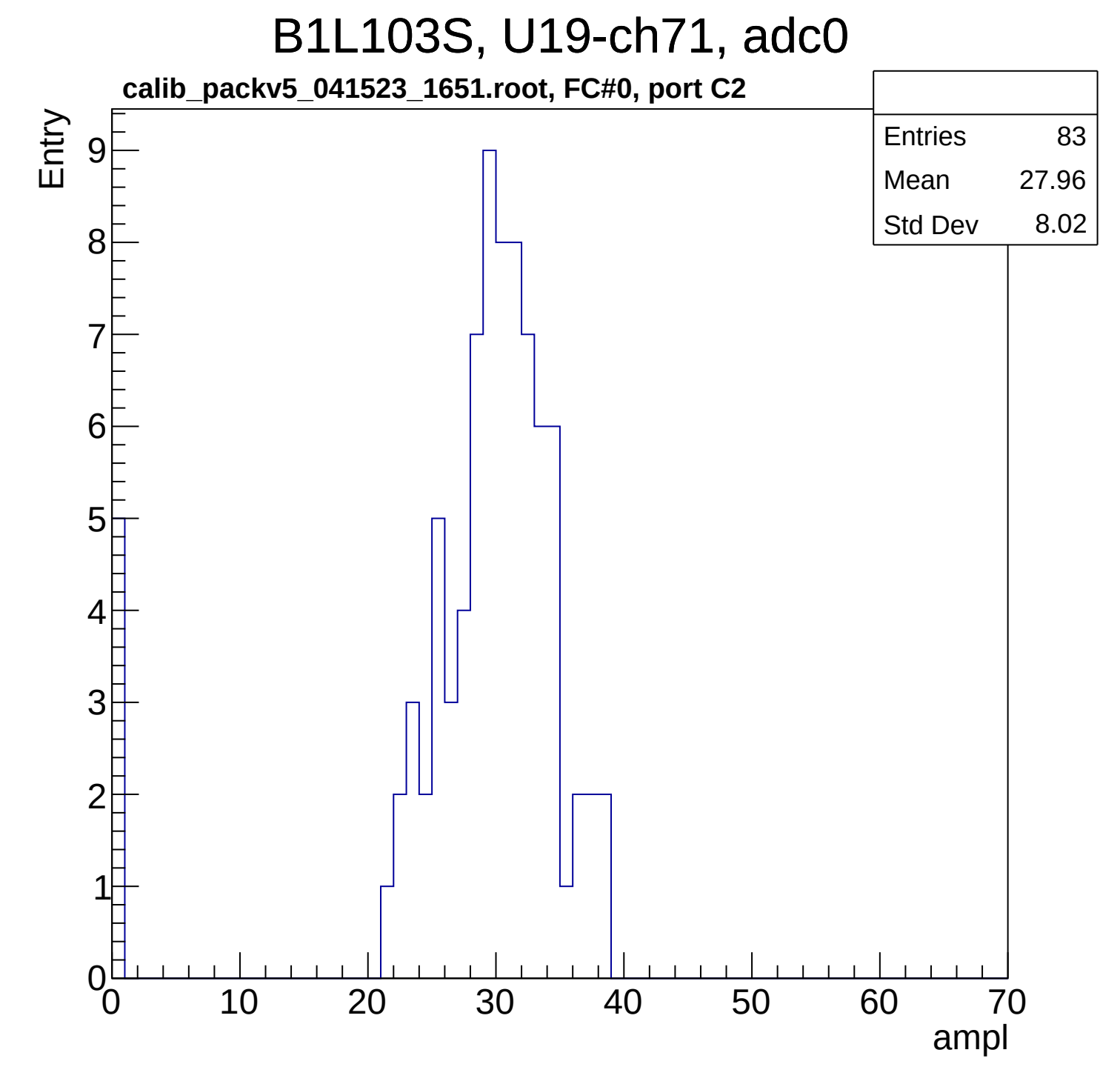
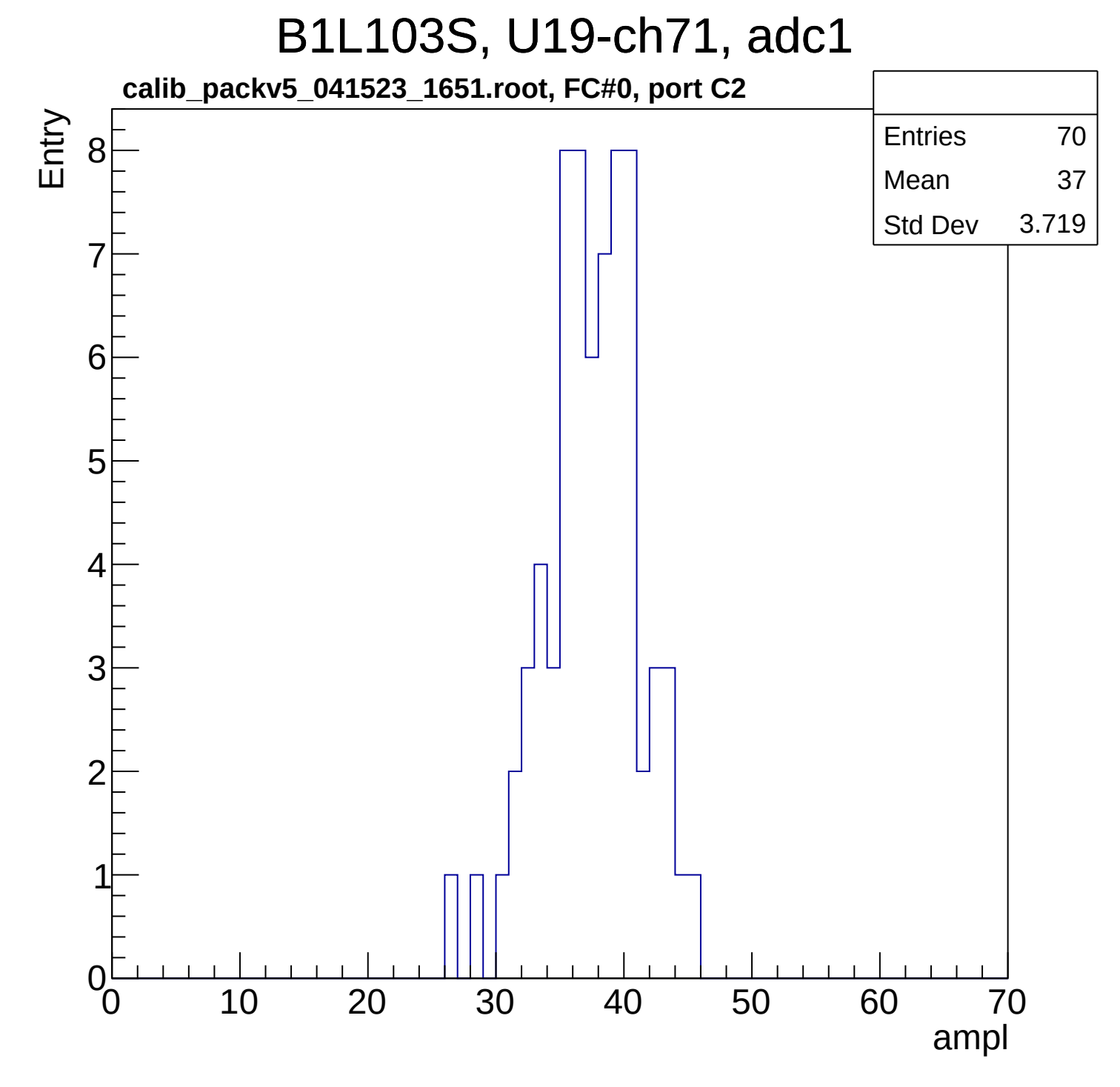

B1L103S, U19-ch70, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 59.04
Std Dev 2.897
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch70, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 57.33
Std Dev 15.39
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch70, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.05
Std Dev 13.29
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch71, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 27.96
Std Dev 8.02
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch71, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 37
Std Dev 3.719
Entry
ampl
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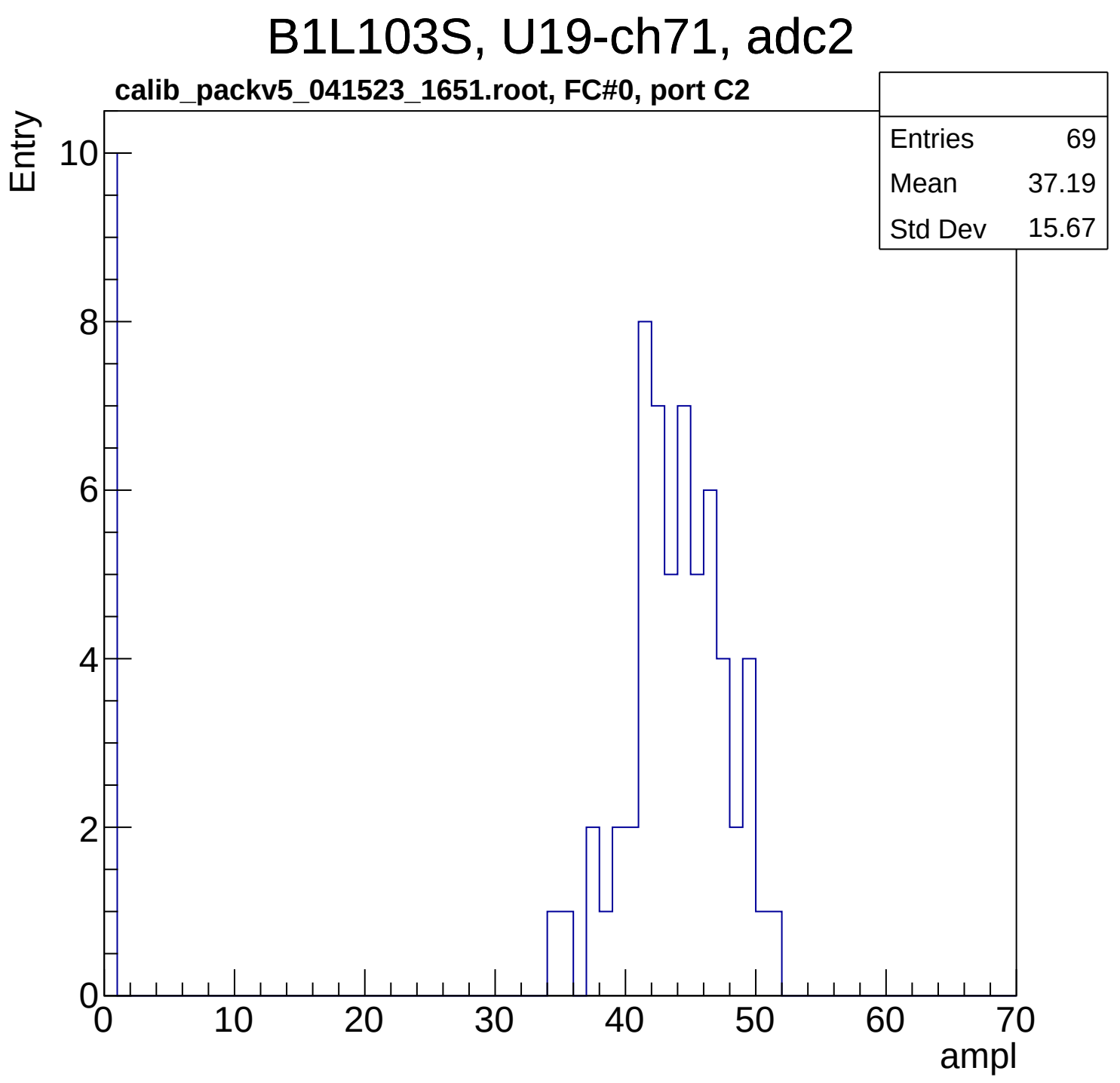
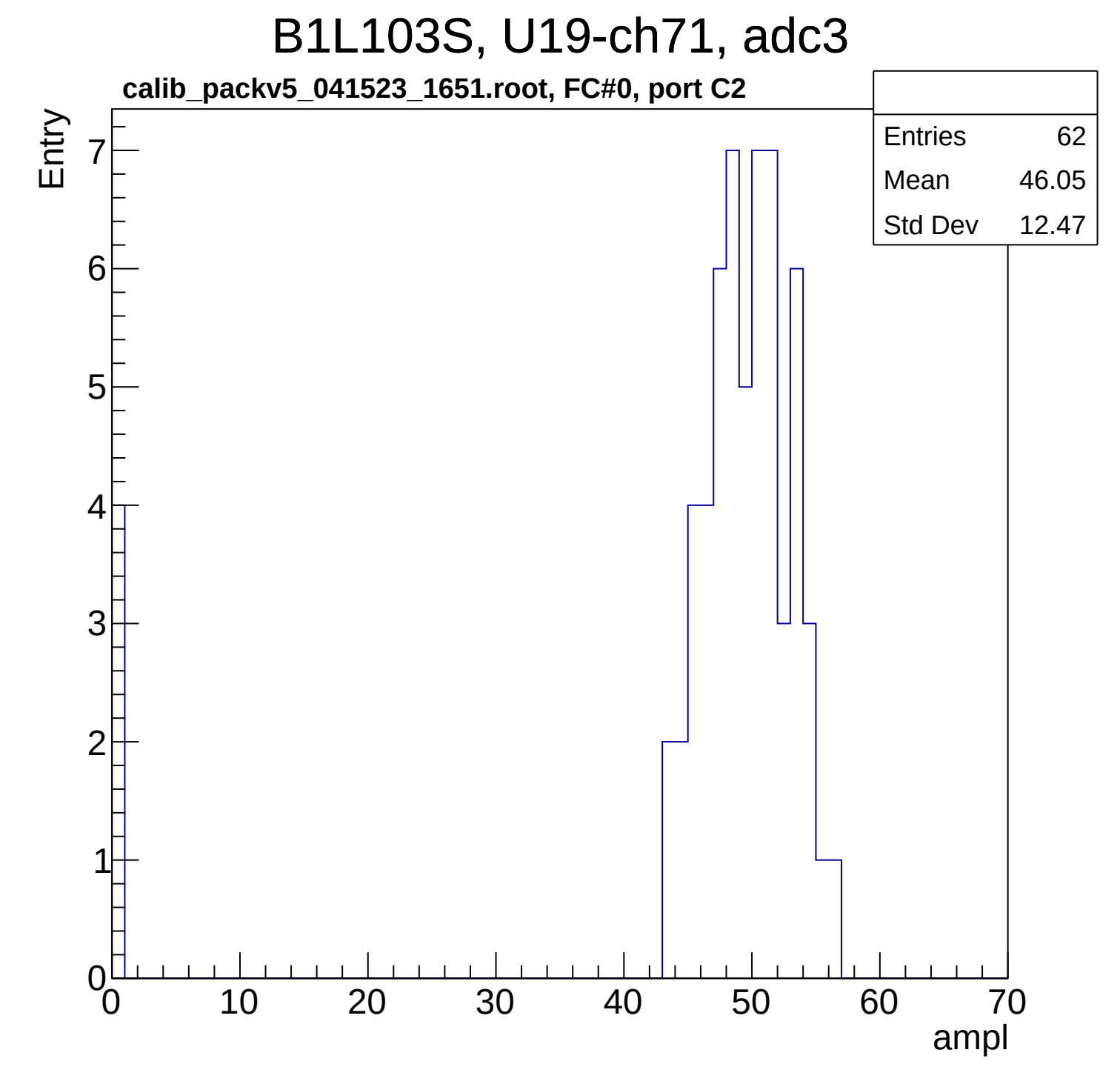
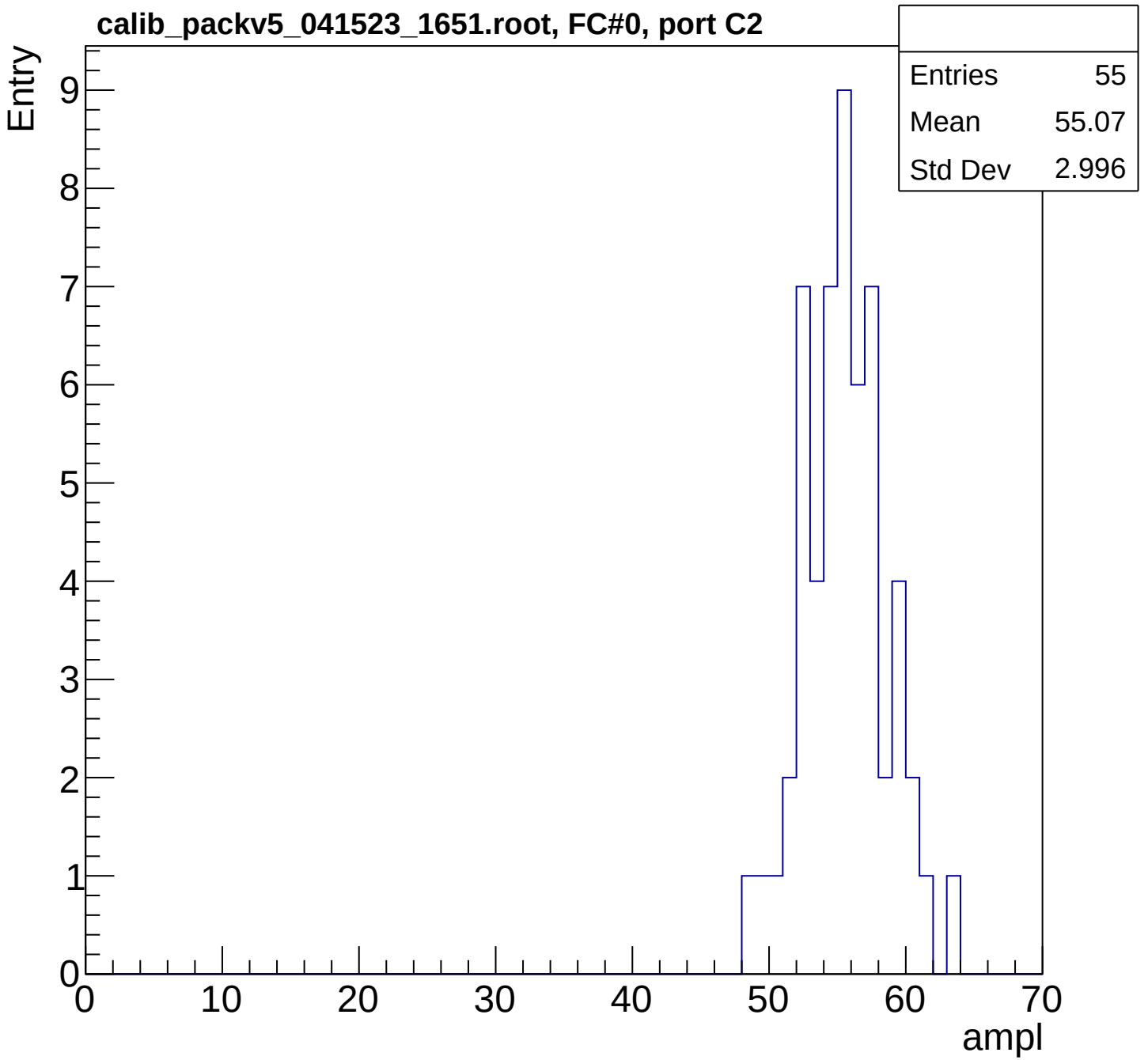
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch71, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 37.19
Std Dev 15.67
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch71, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 46.05
Std Dev 12.47
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch71, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 55.07
Std Dev 2.996
Entry
ampl
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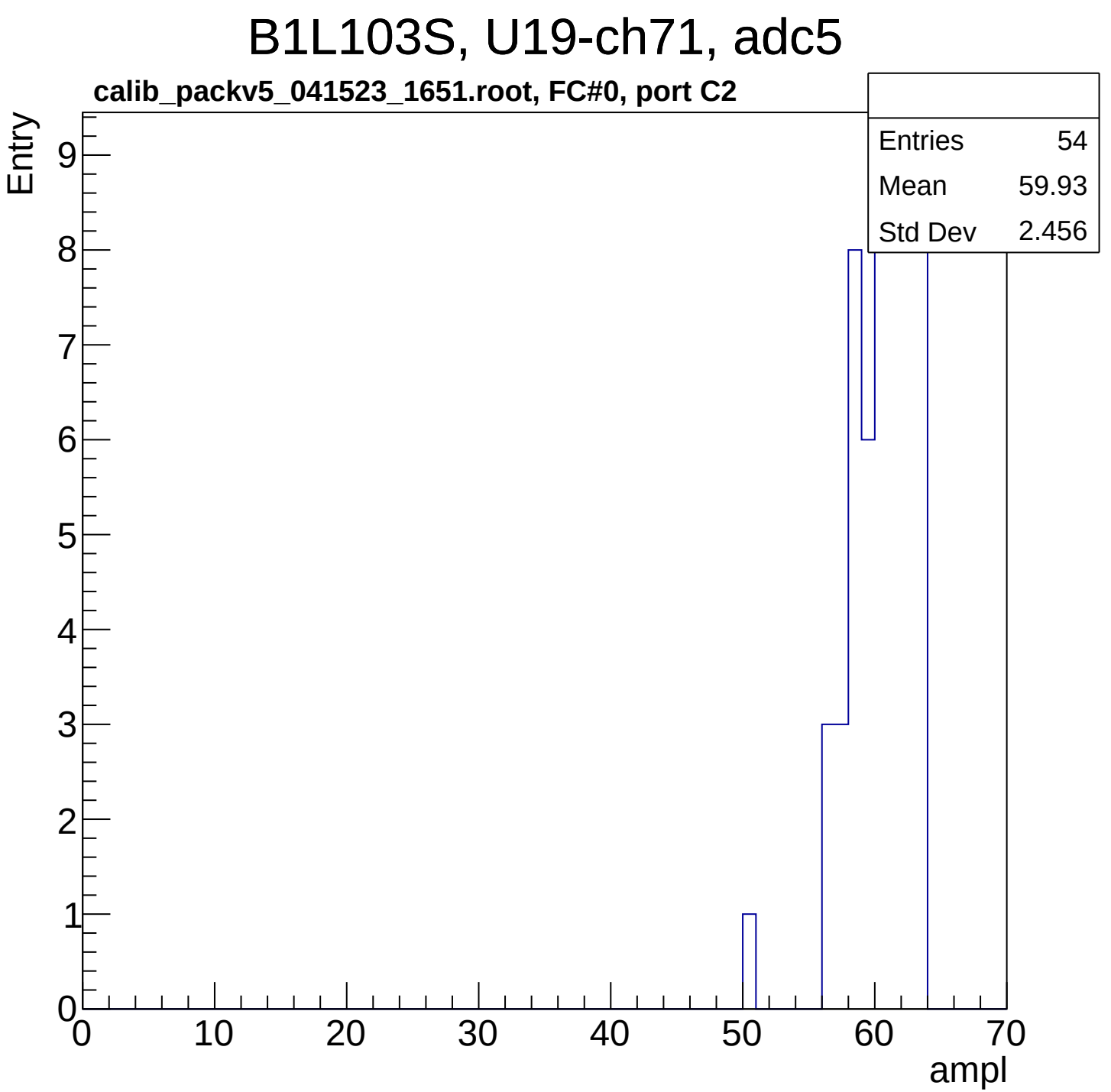
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch71, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 59.93
Std Dev 2.456
Entry
ampl
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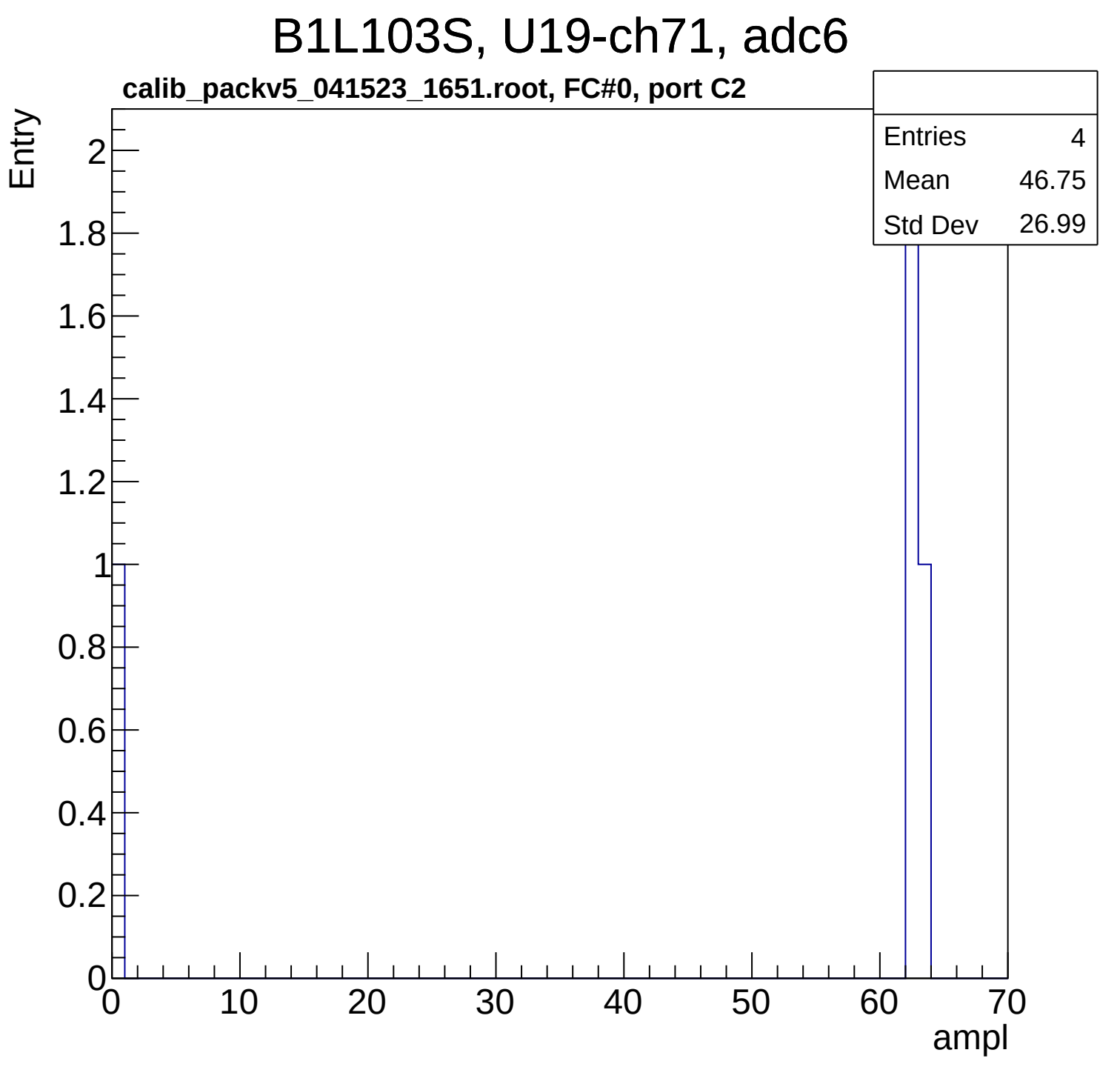
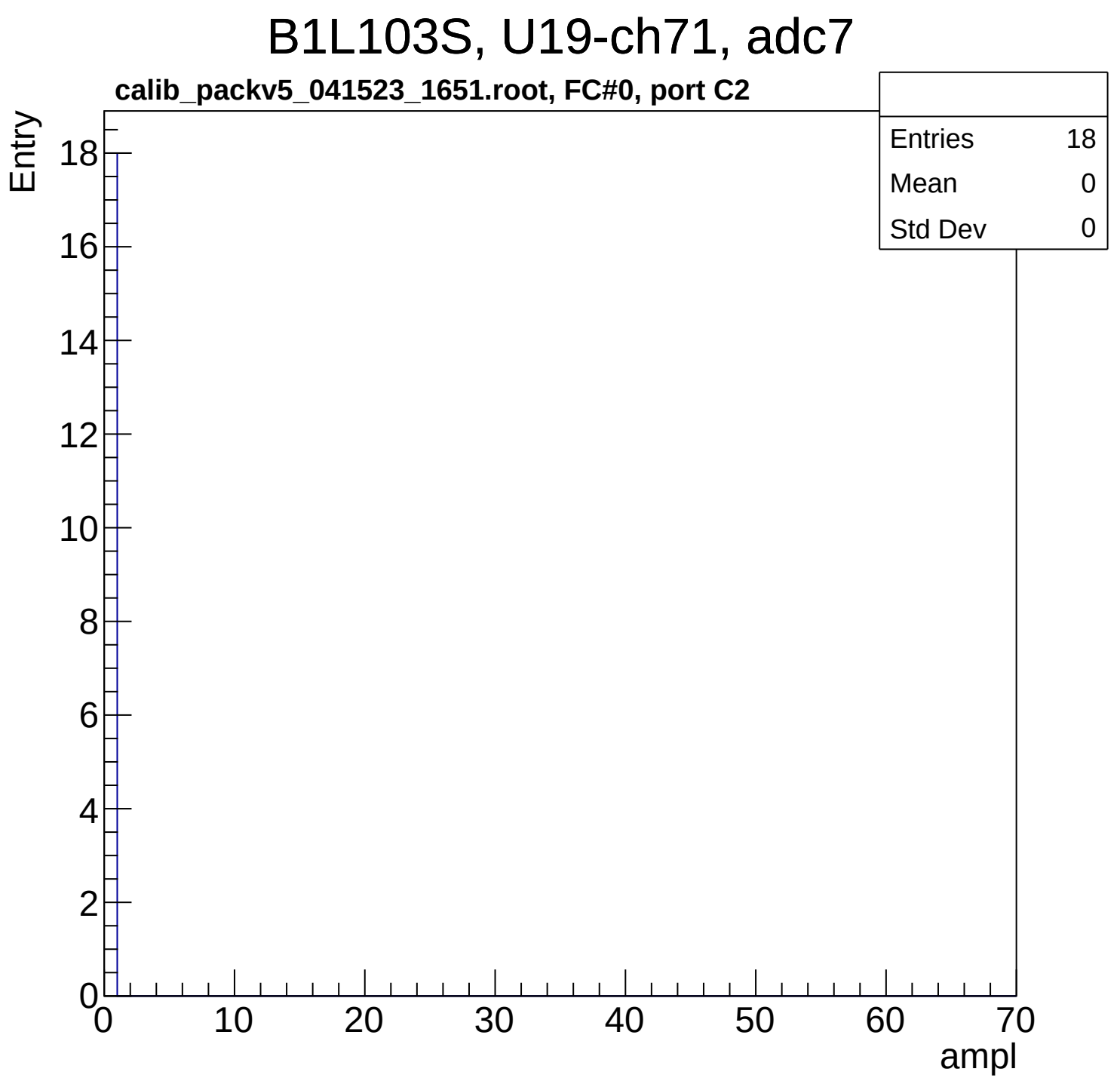
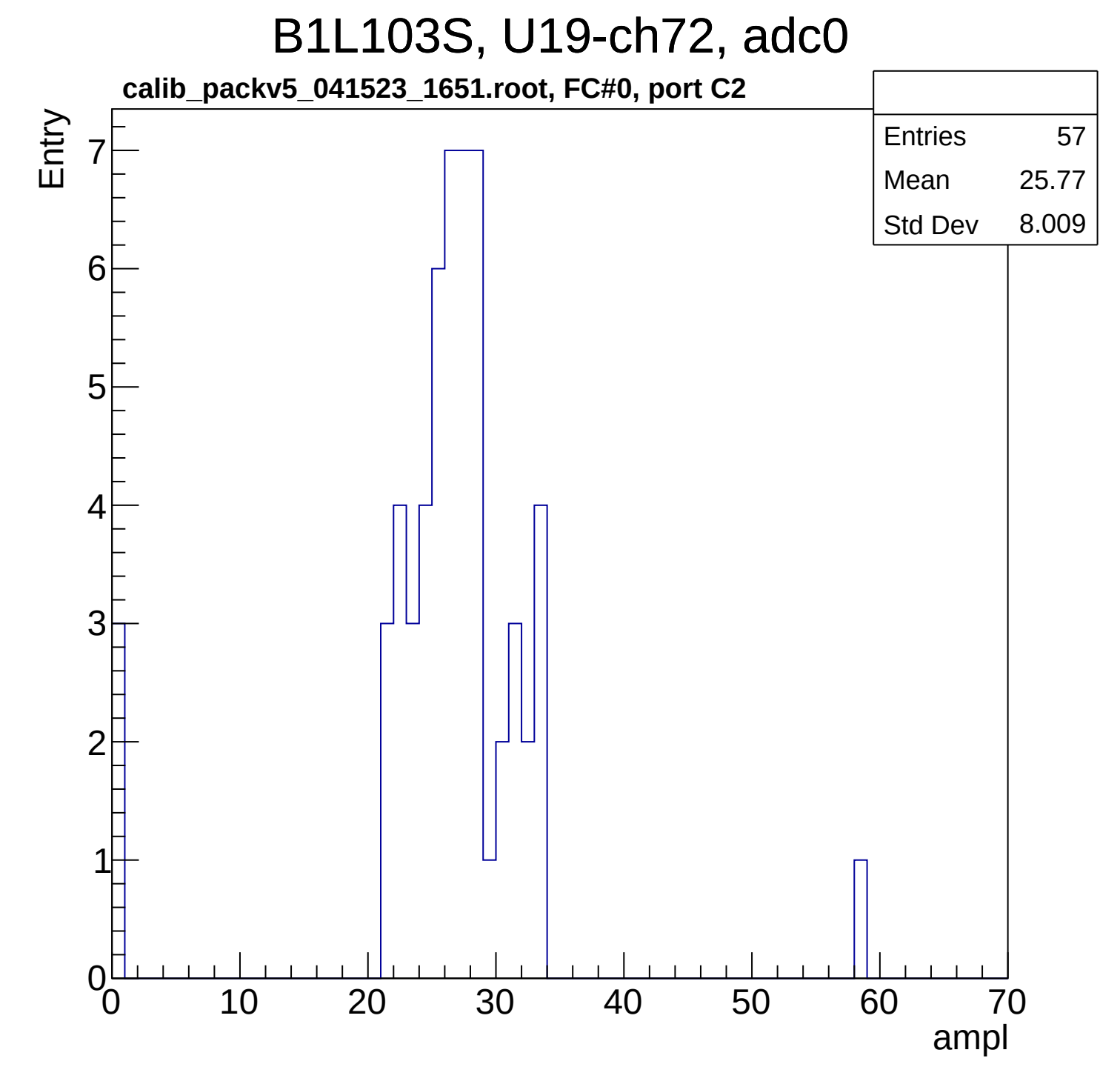
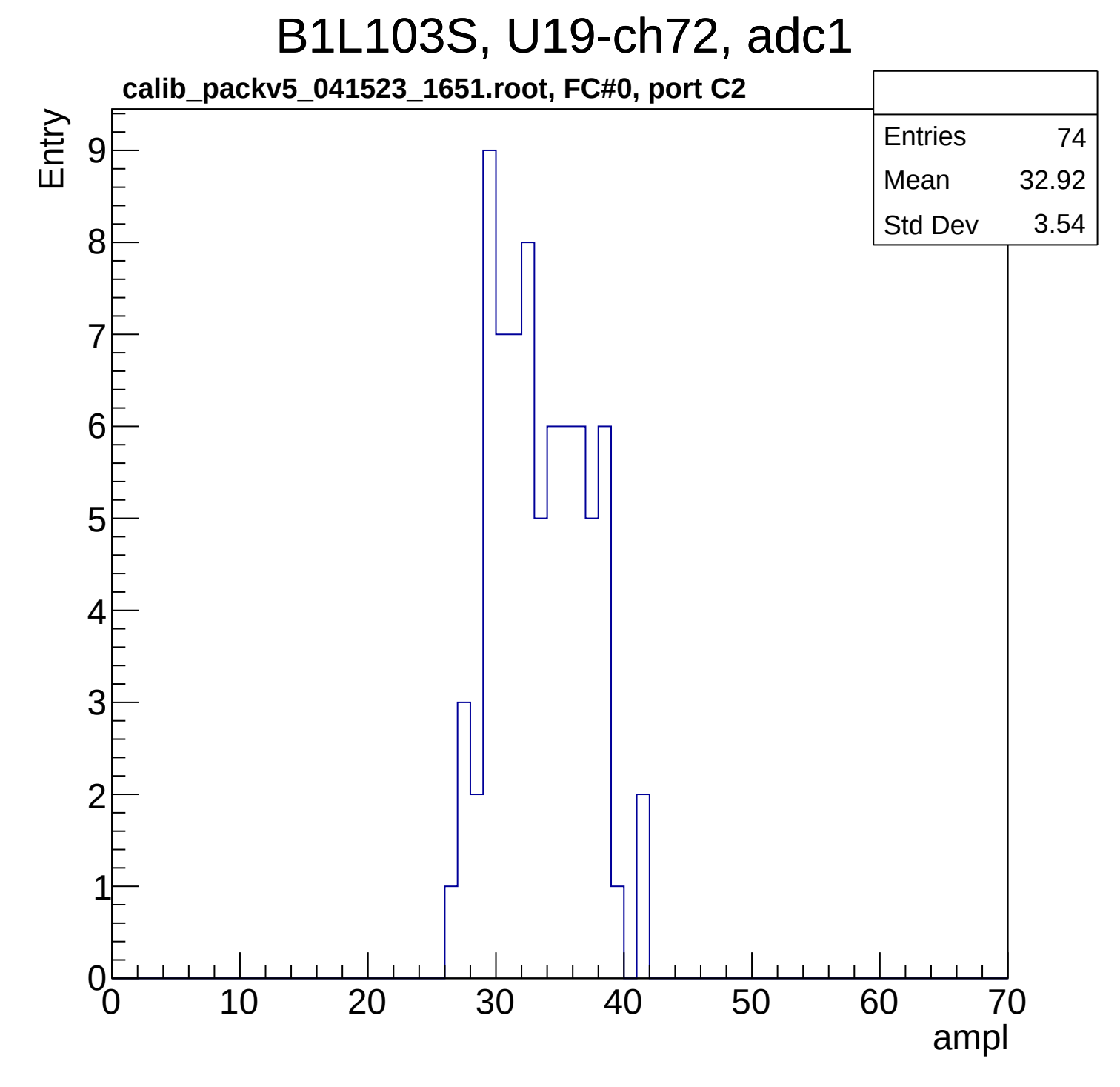
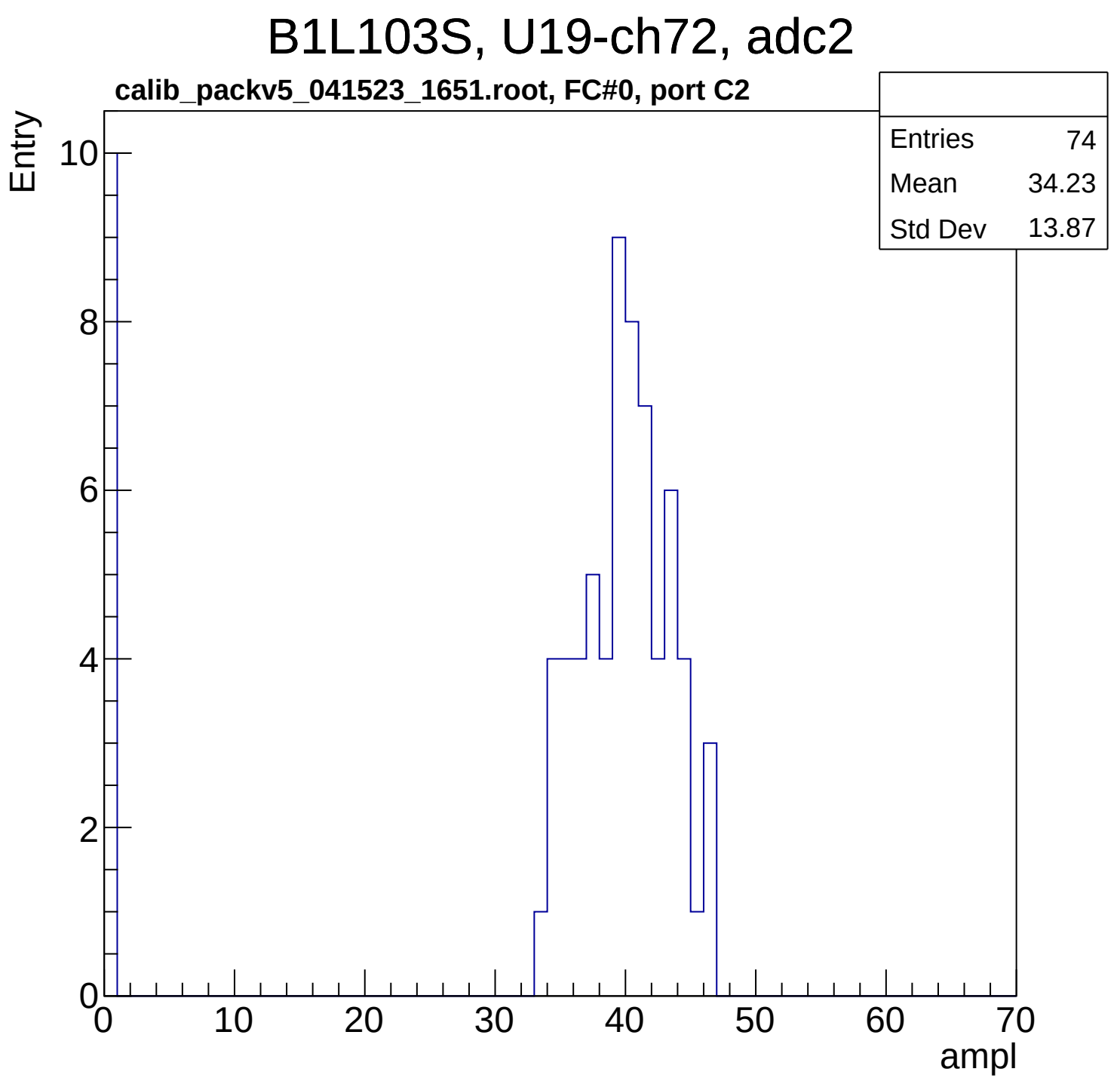
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

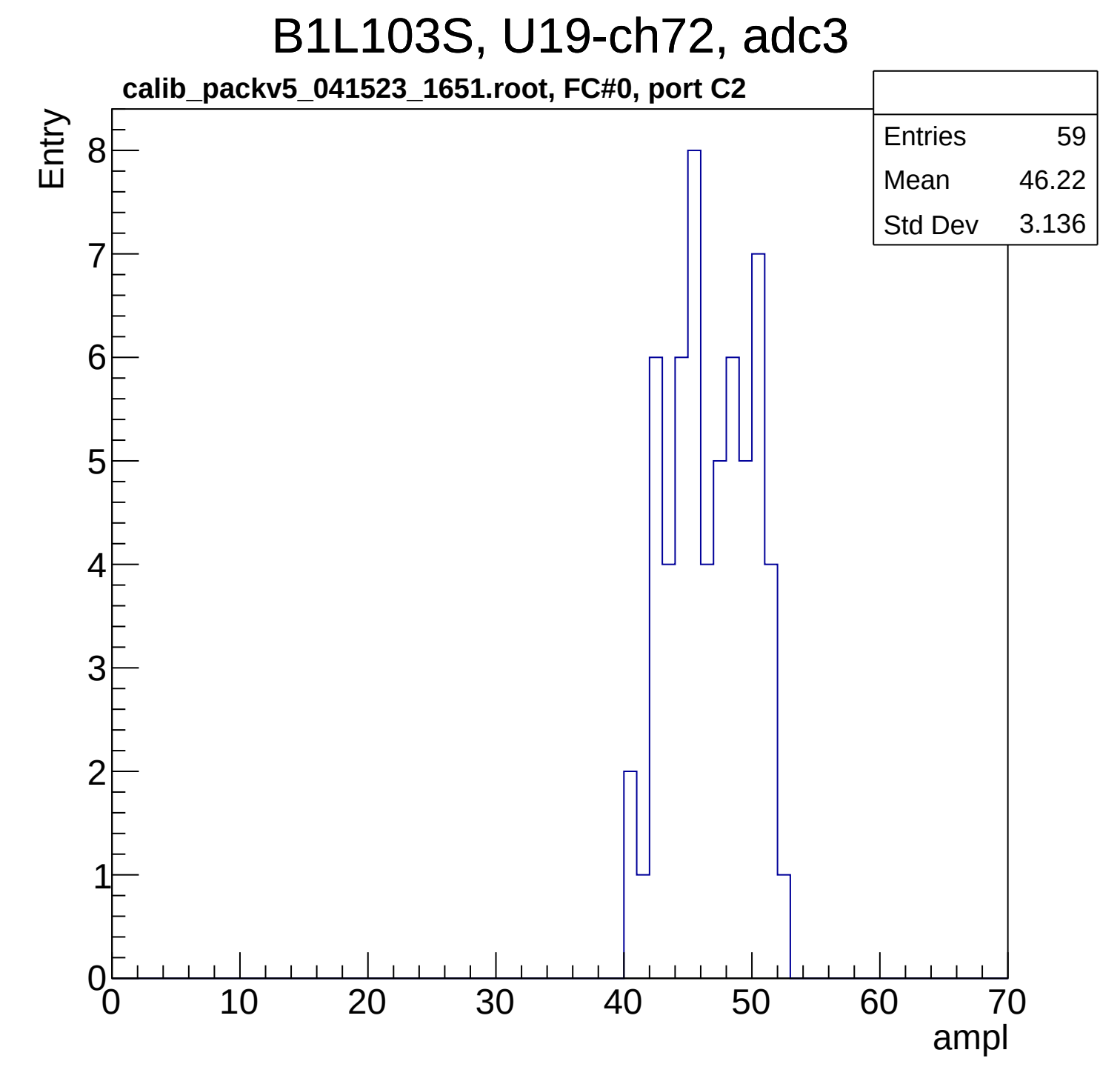

B1L103S, U19-ch71, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 46.75
Std Dev 26.99
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U19-ch71, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch72, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 25.77
Std Dev 8.009
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch72, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 32.92
Std Dev 3.54
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch72, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 34.23
Std Dev 13.87
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch72, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 46.22
Std Dev 3.136
Entry
ampl
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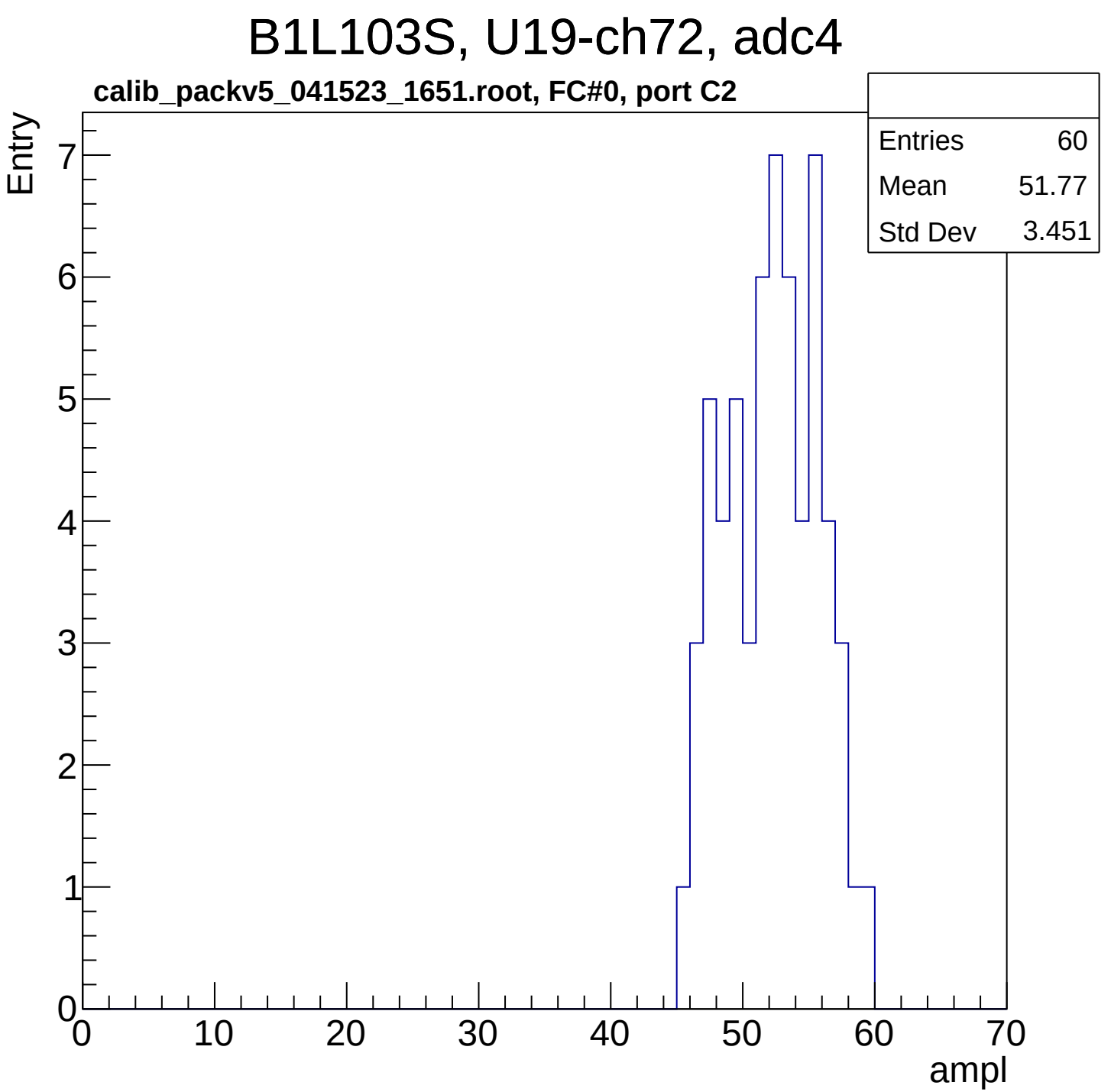
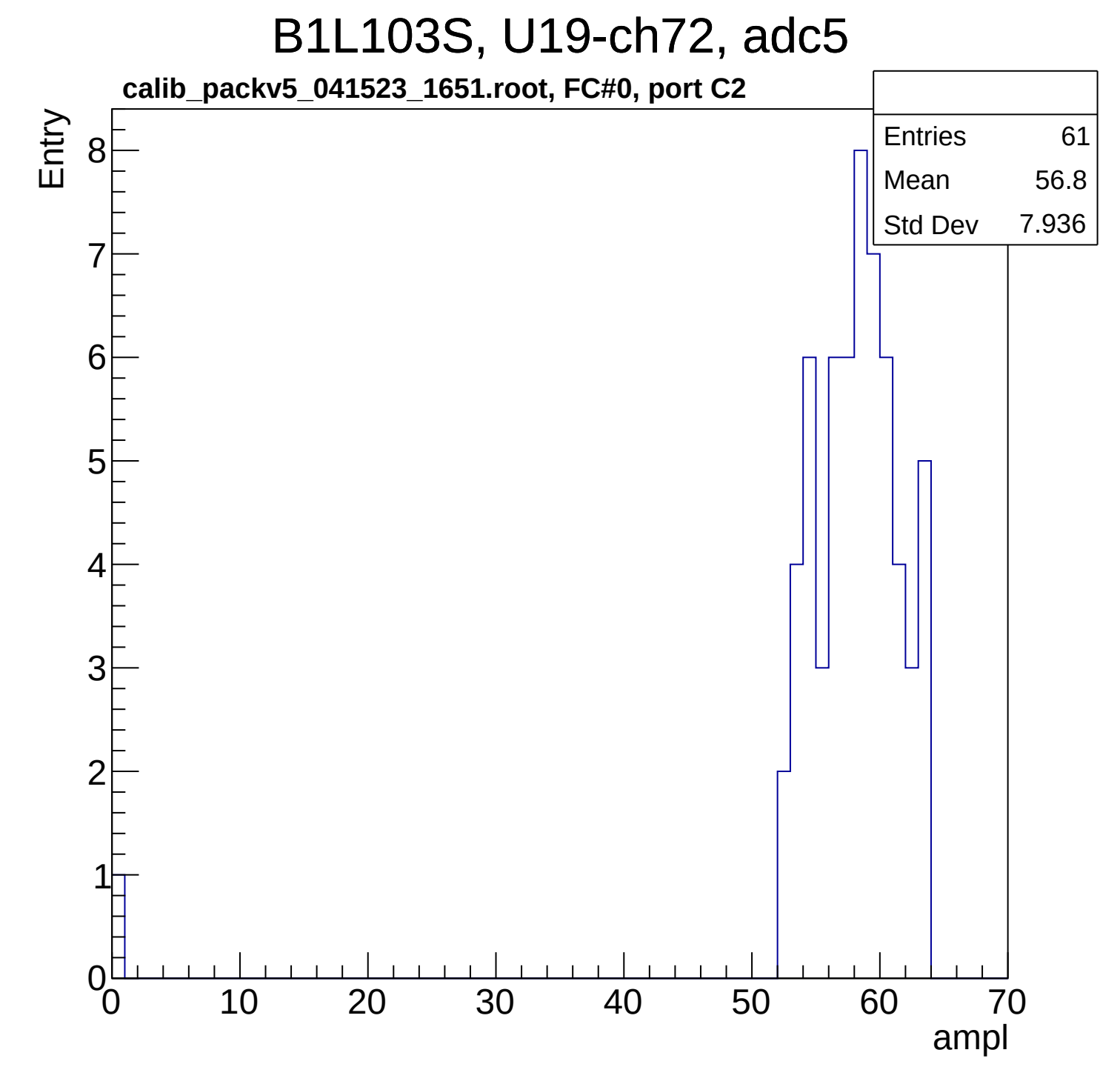
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch72, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 51.77
Std Dev 3.451
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch72, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 56.8
Std Dev 7.936
Entry
ampl
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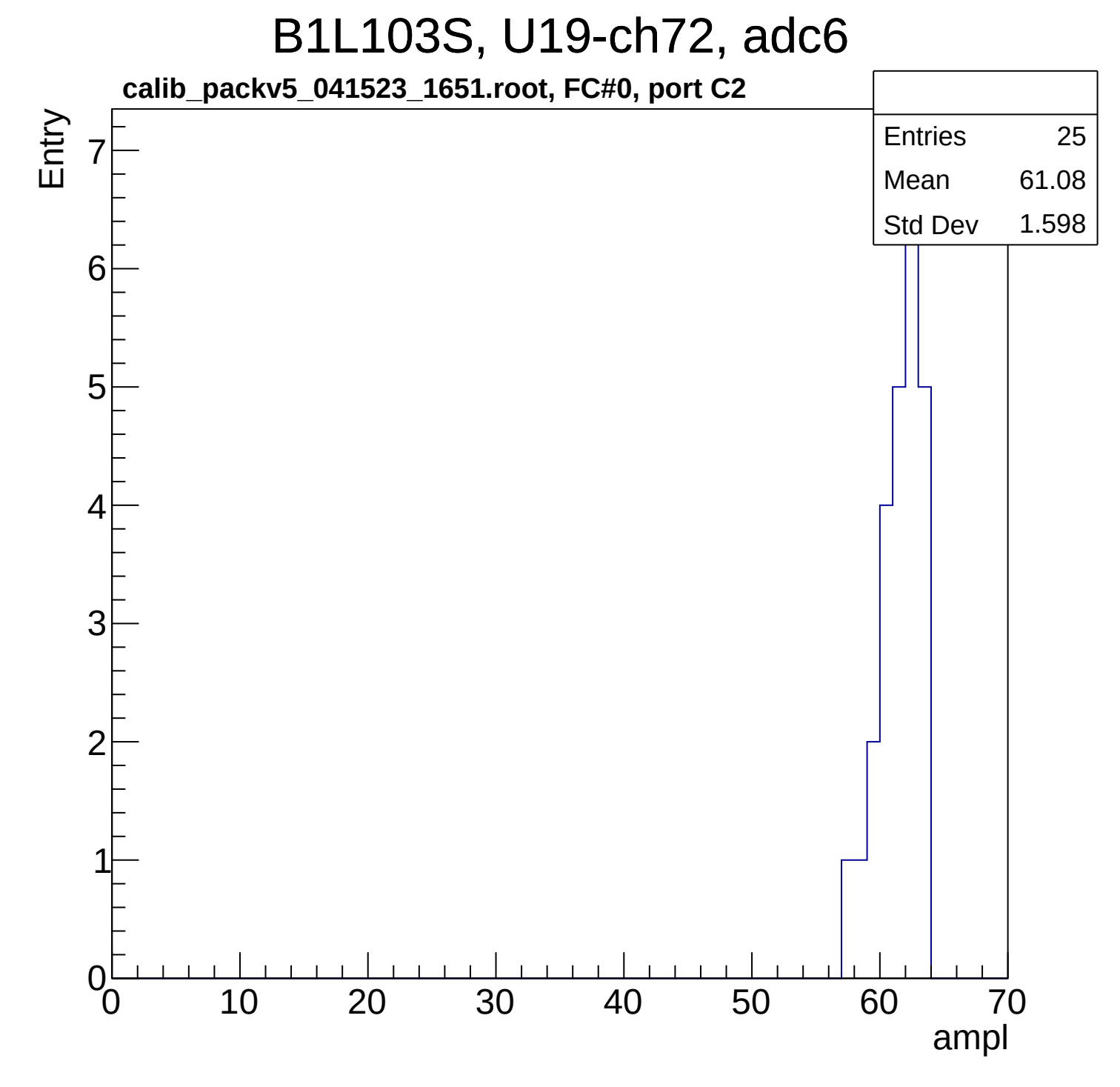
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch72, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 61.08
Std Dev 1.598
Entry
ampl
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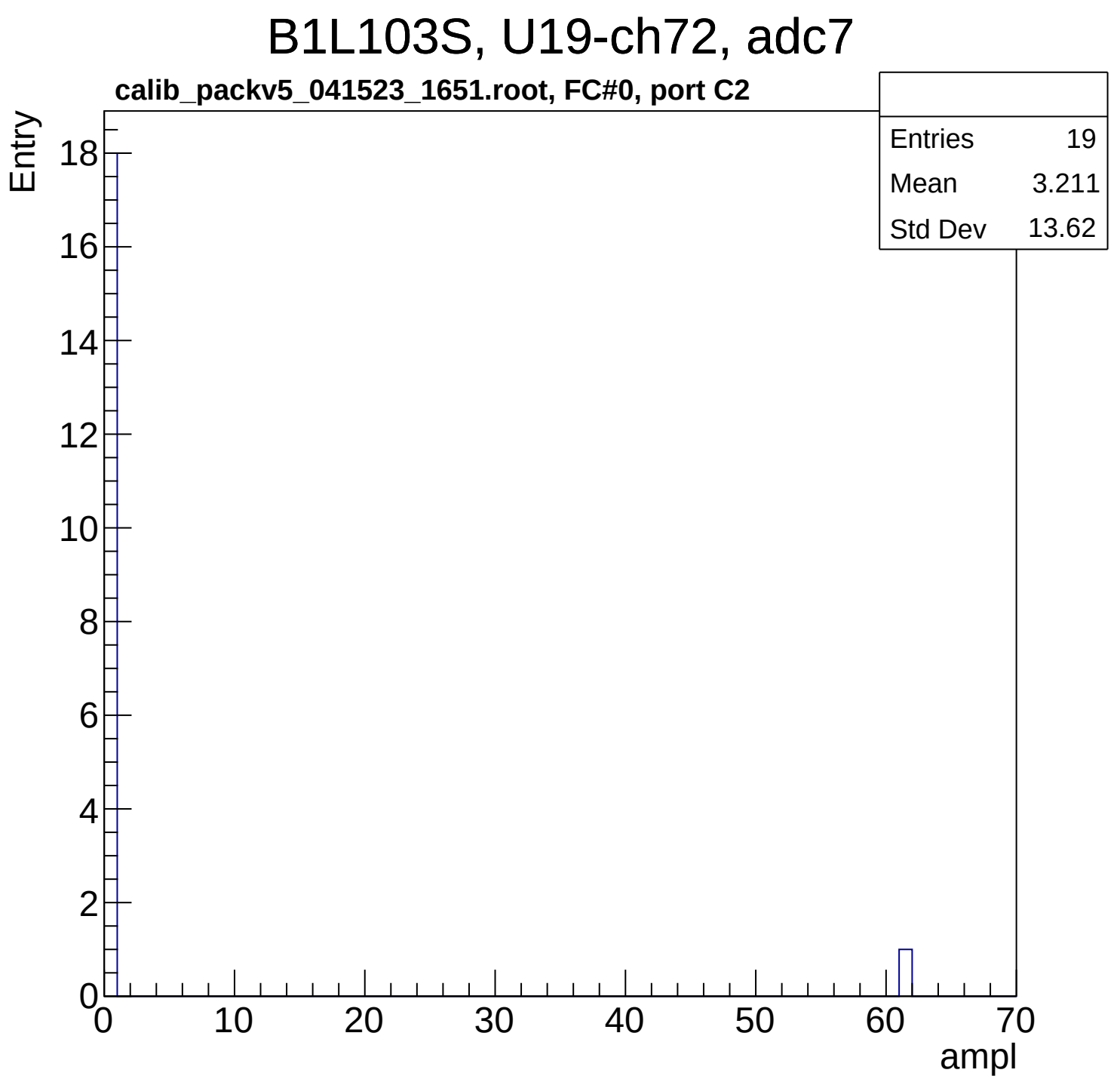
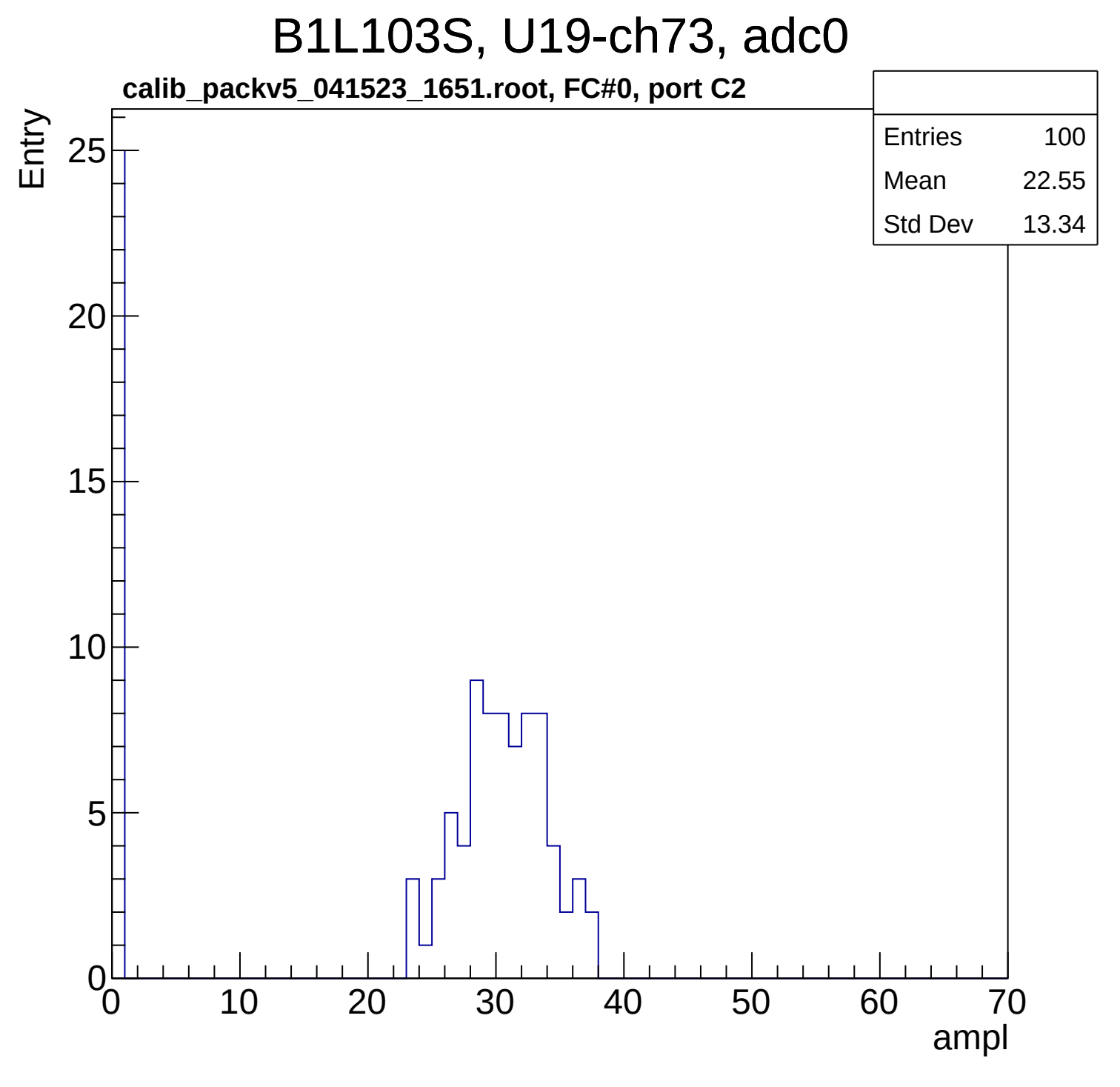
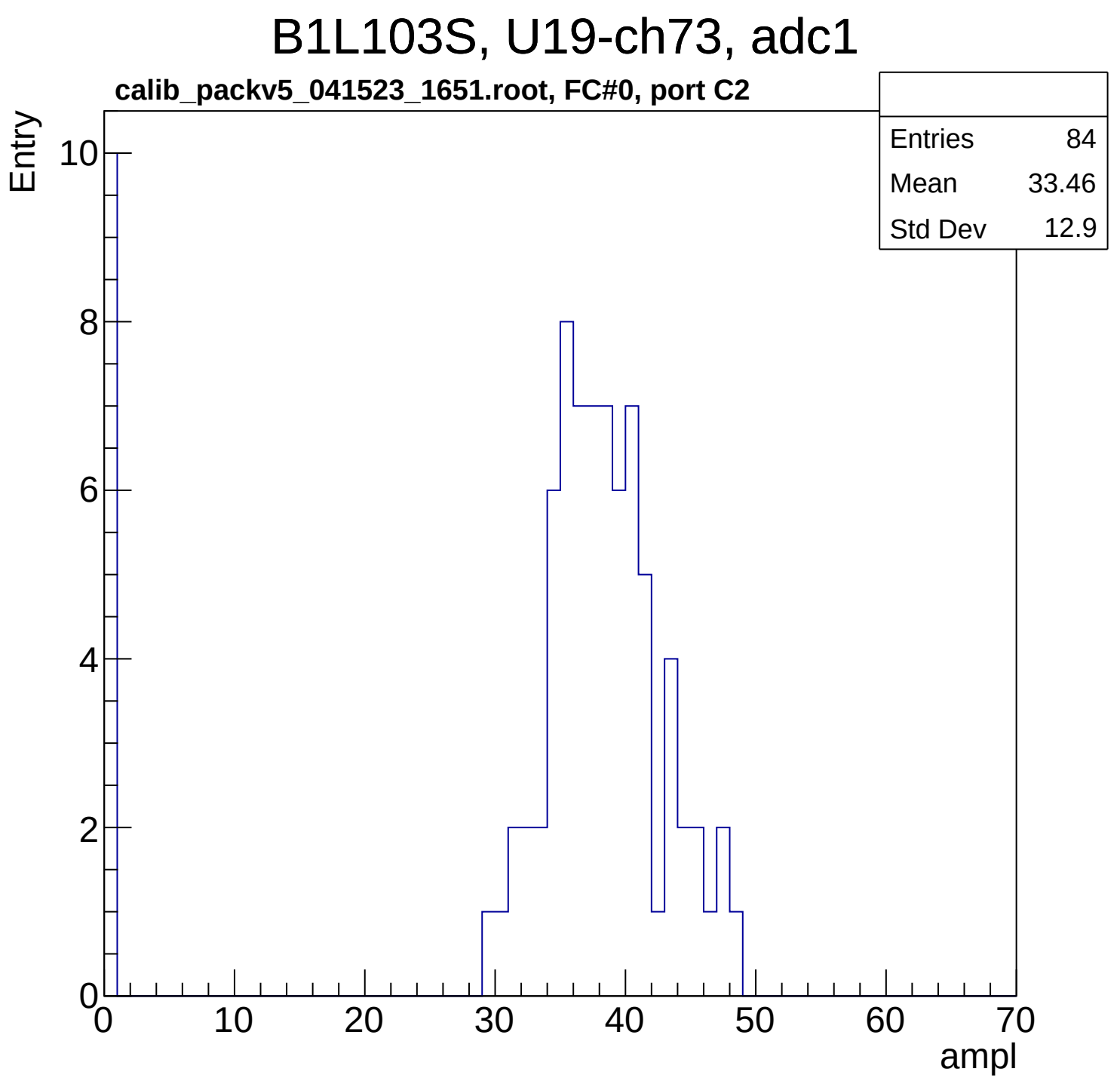
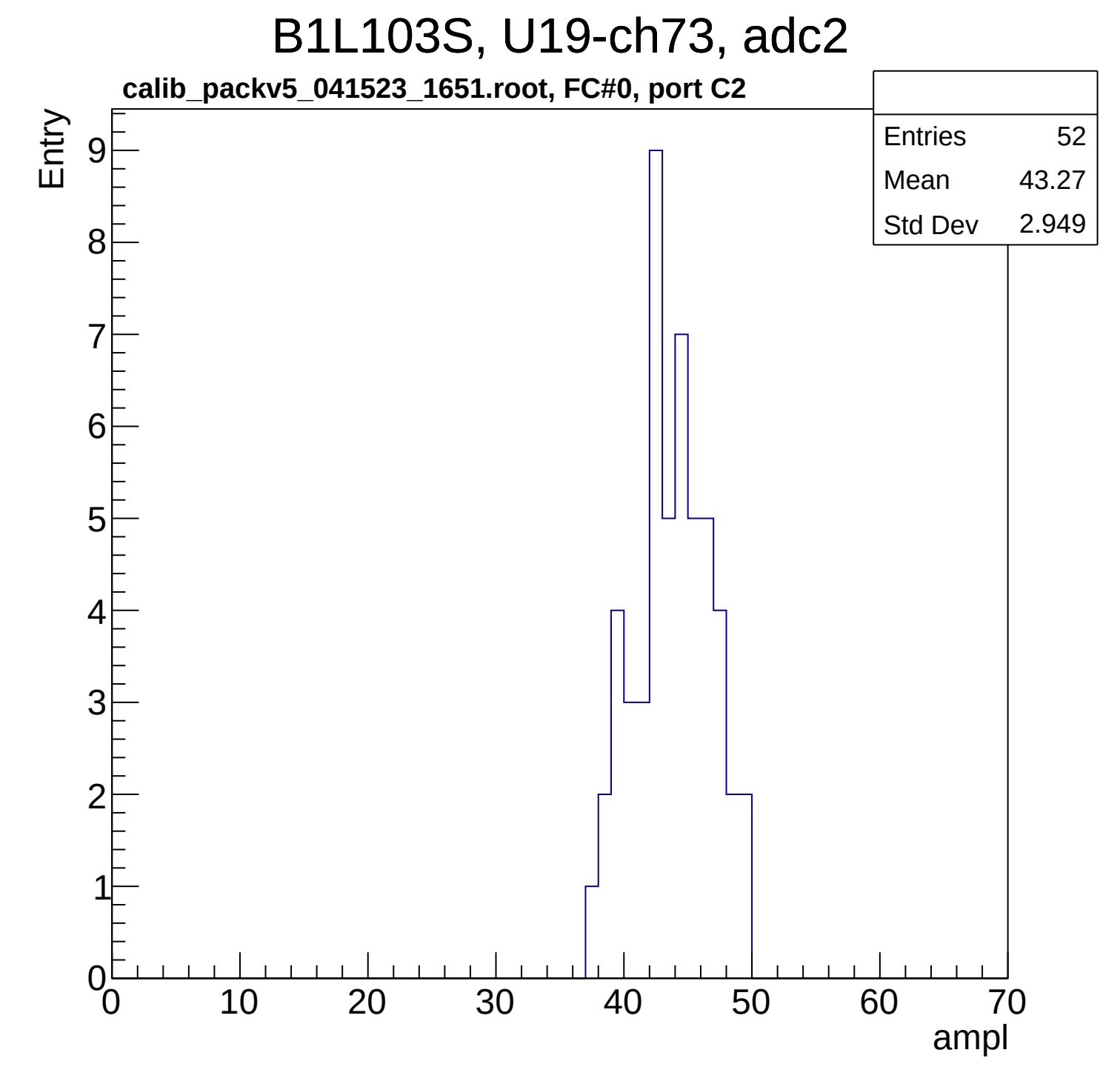
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch72, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.211
Std Dev 13.62
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch73, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 100
Mean 22.55
Std Dev 13.34
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch73, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 33.46
Std Dev 12.9
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U19-ch73, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 43.27
Std Dev 2.949
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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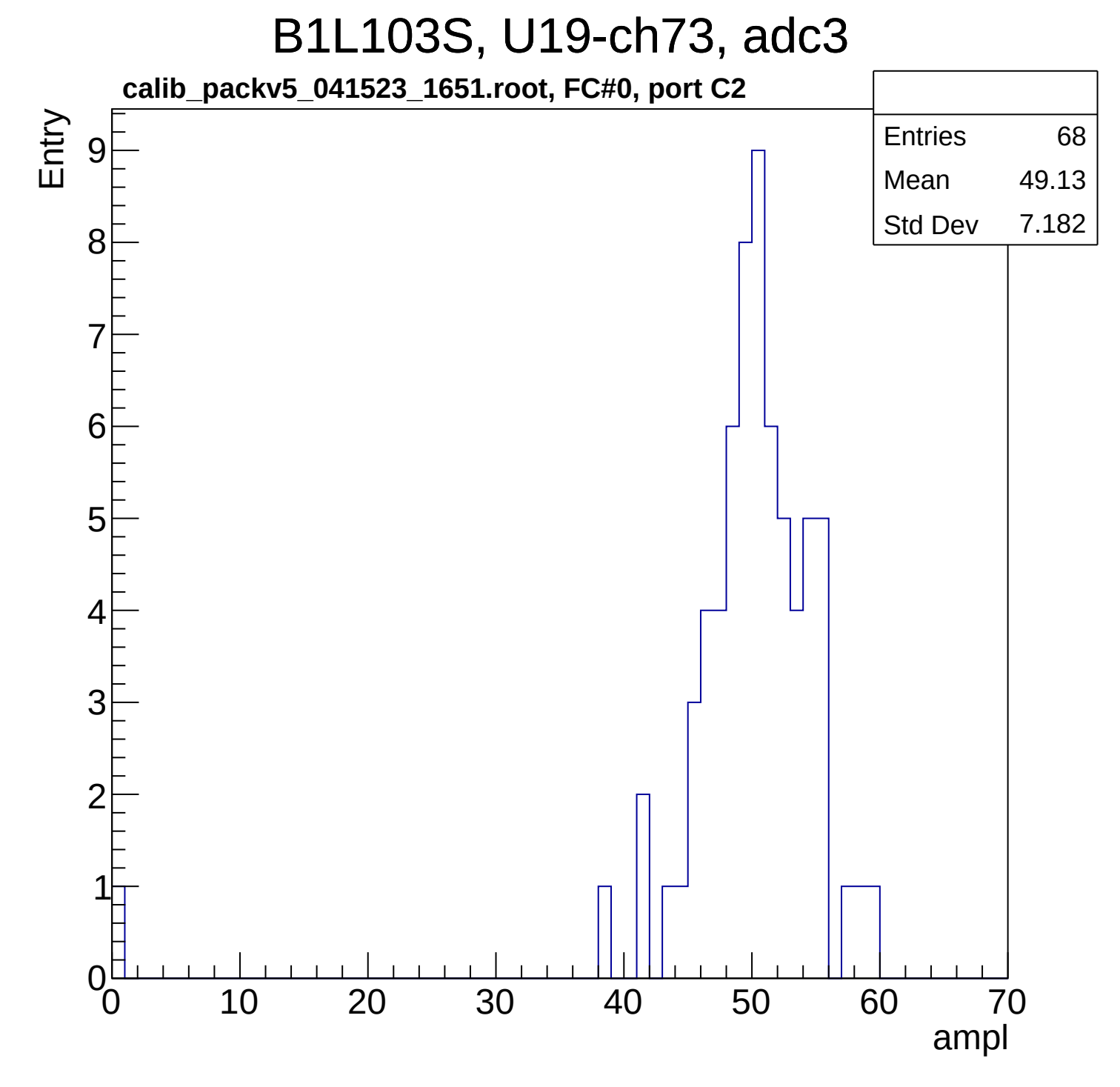
B1L103S, U19-ch73, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 49.13
Std Dev 7.182
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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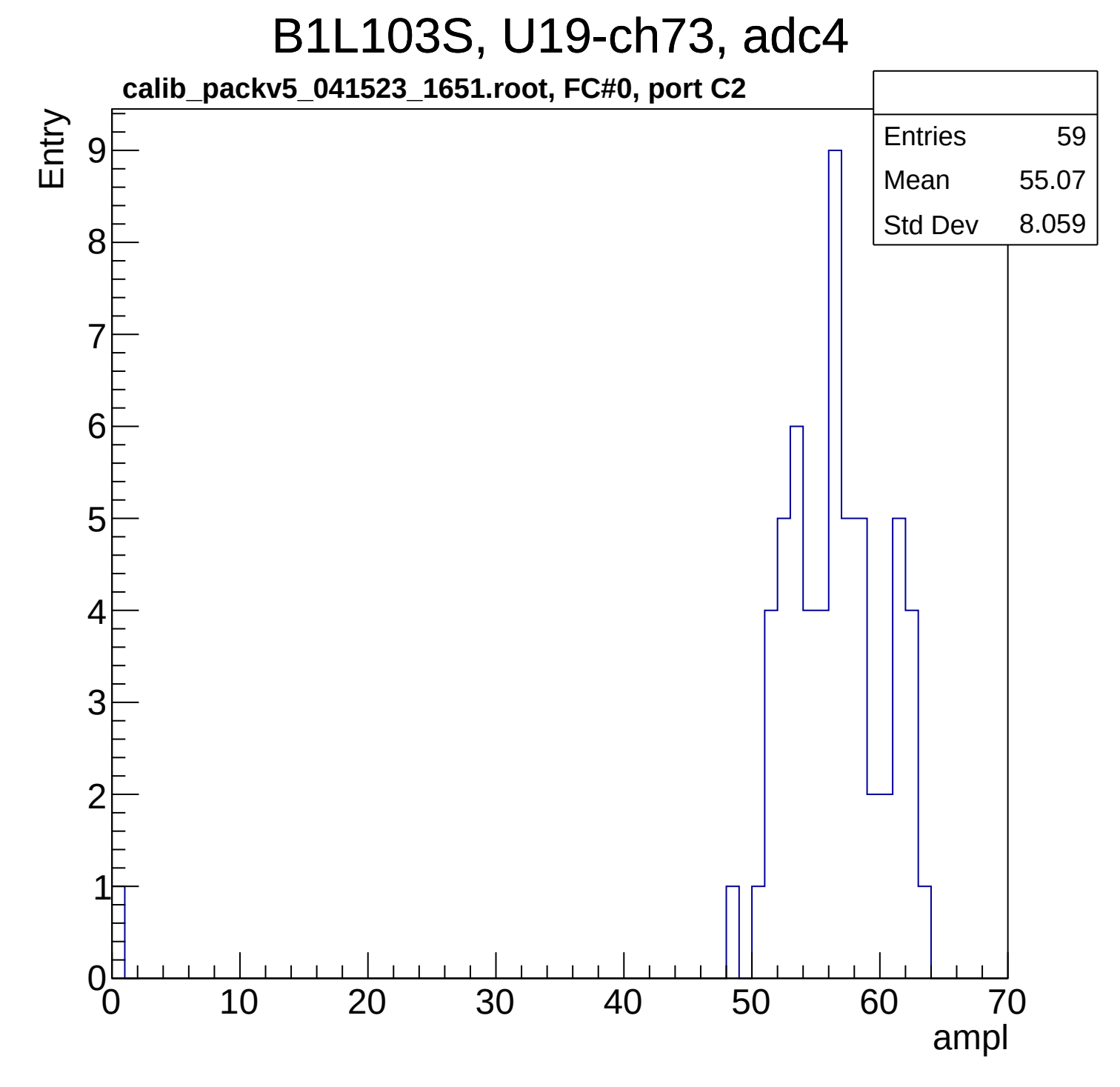
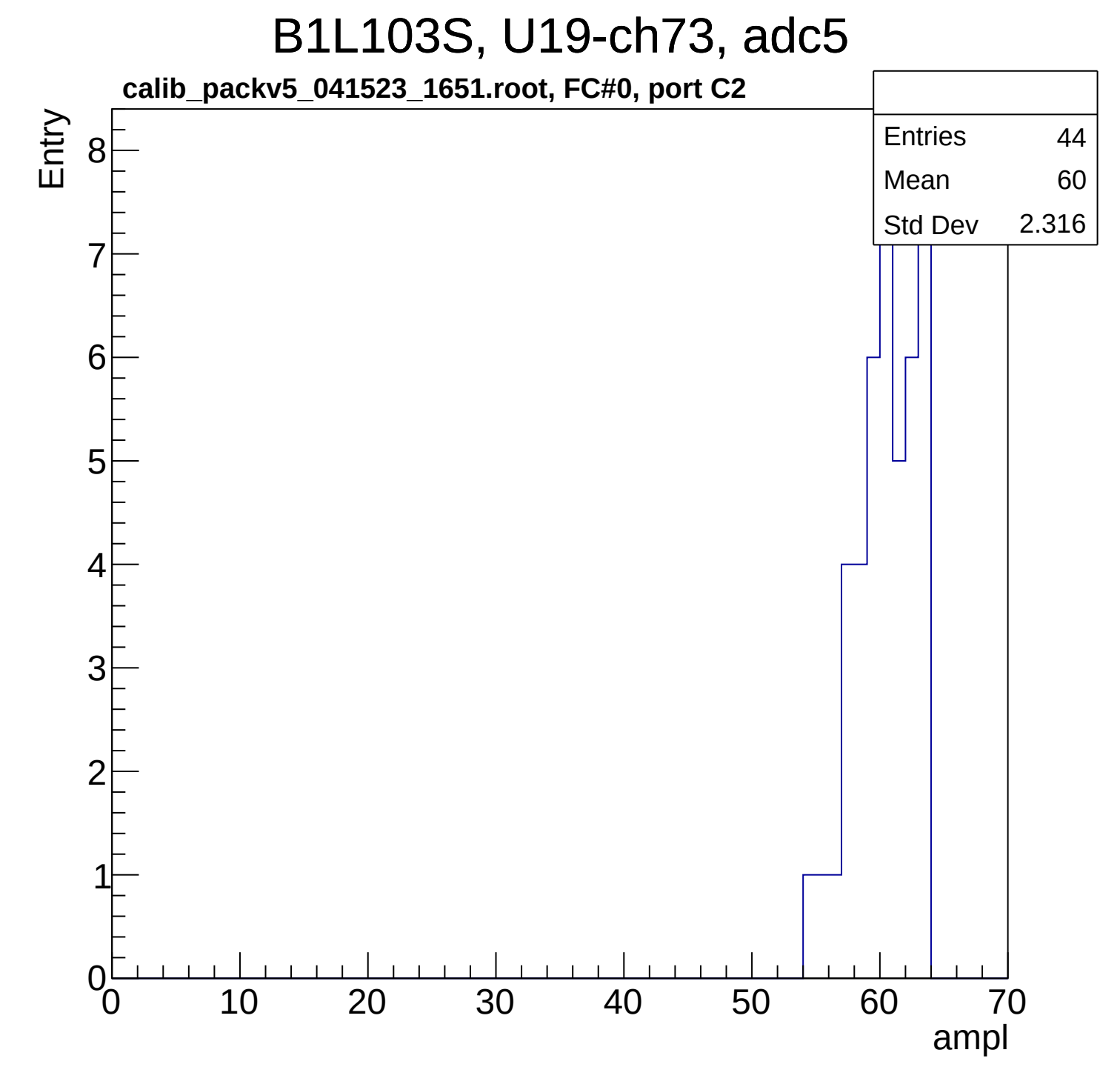
60
70


B1L103S, U19-ch73, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 55.07
Std Dev 8.059
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch73, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 60
Std Dev 2.316
Entry
ampl
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1
2
3
4
5
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7
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0
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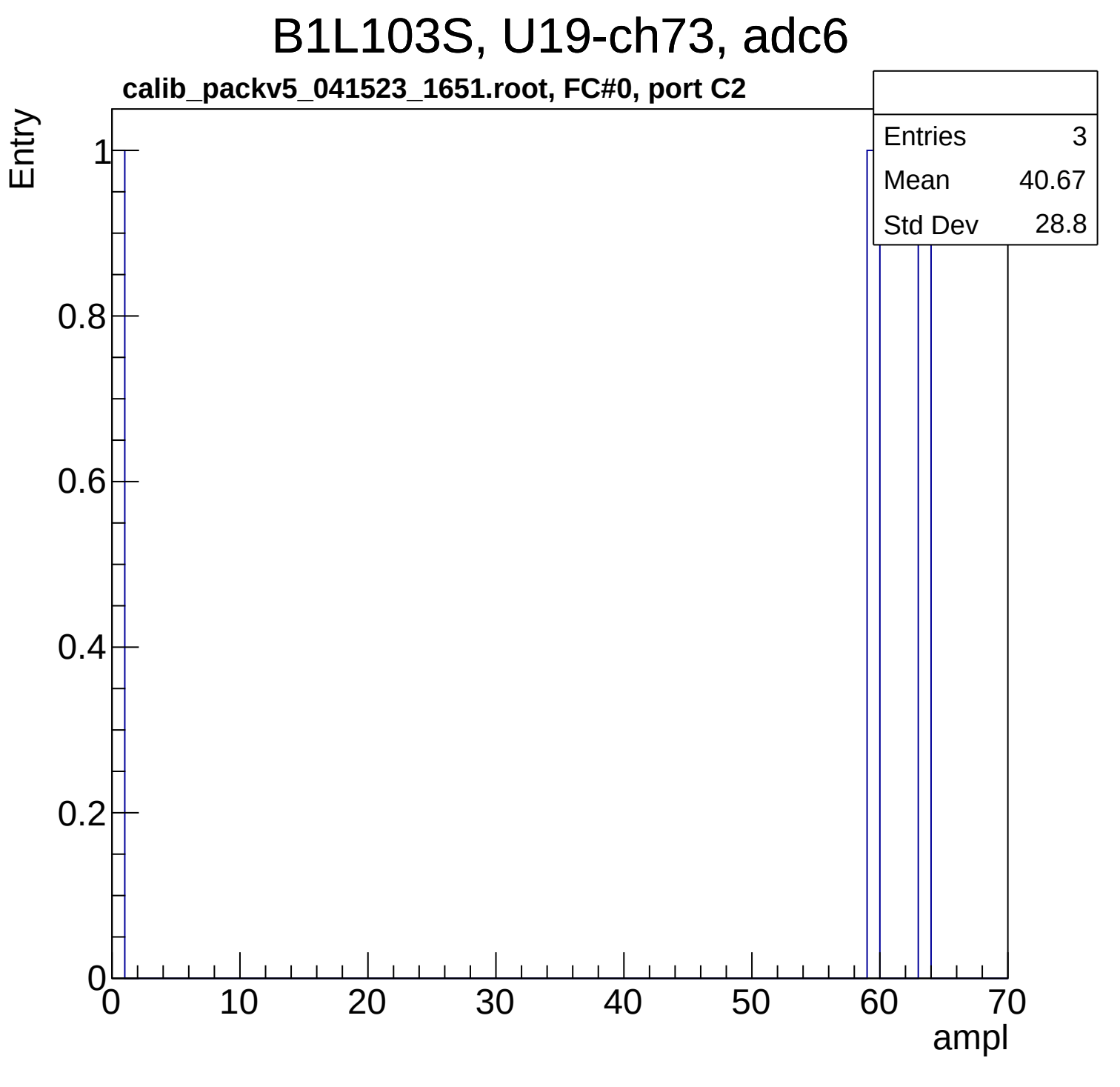
B1L103S, U19-ch73, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 40.67
Std Dev 28.8
Entry
ampl
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0.2
0.4
0.6
0.8
1
0
10
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40
50
60
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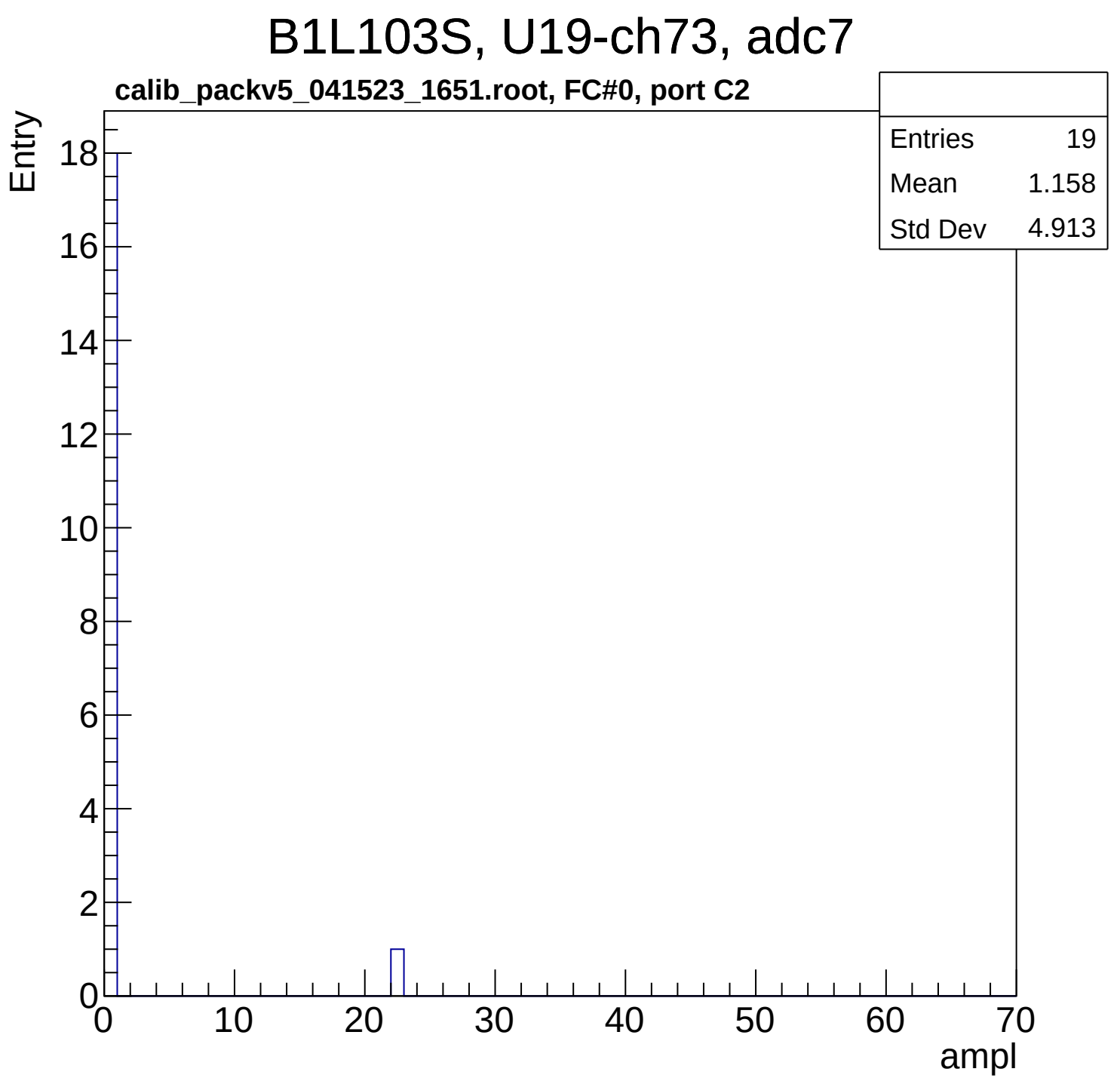
B1L103S, U19-ch73, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.158
Std Dev 4.913
Entry
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6
8
10
12
14
16
18
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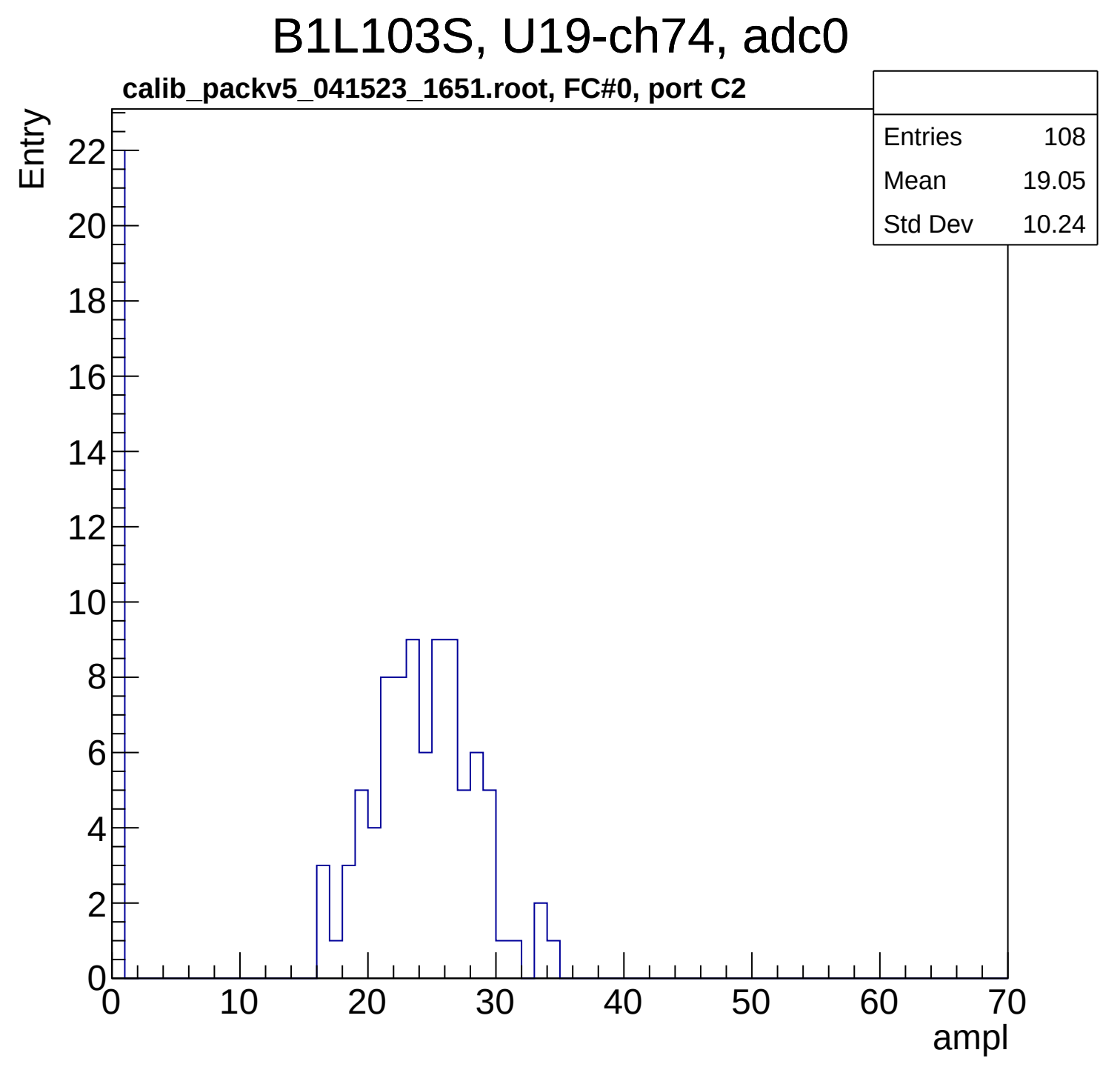
70
ampl


B1L103S, U19-ch74, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 108
Mean 19.05
Std Dev 10.24
Entry
ampl
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8
10
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14
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60
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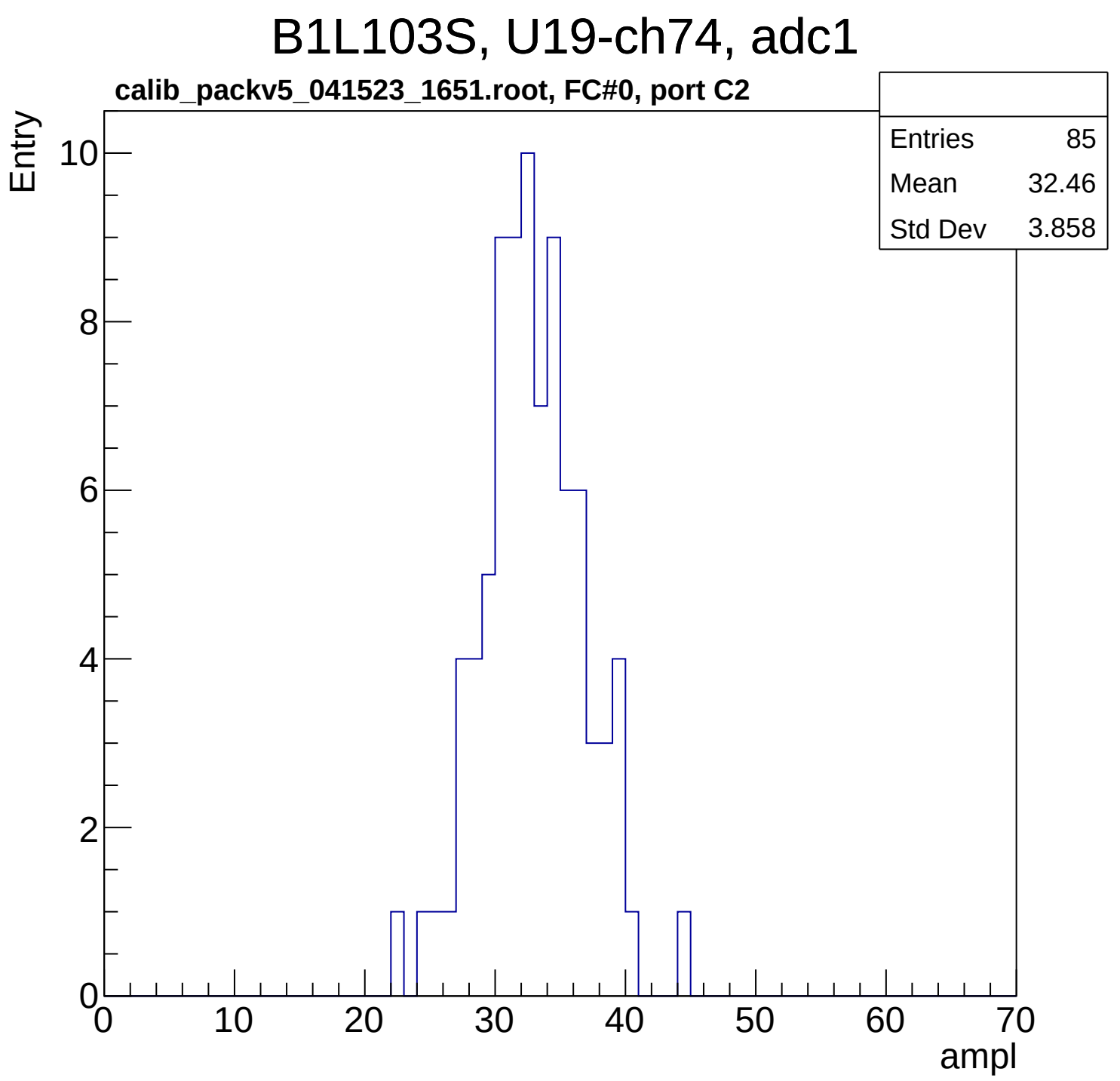
B1L103S, U19-ch74, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 32.46
Std Dev 3.858
Entry
ampl
0
2
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6
8
10
0
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40
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60
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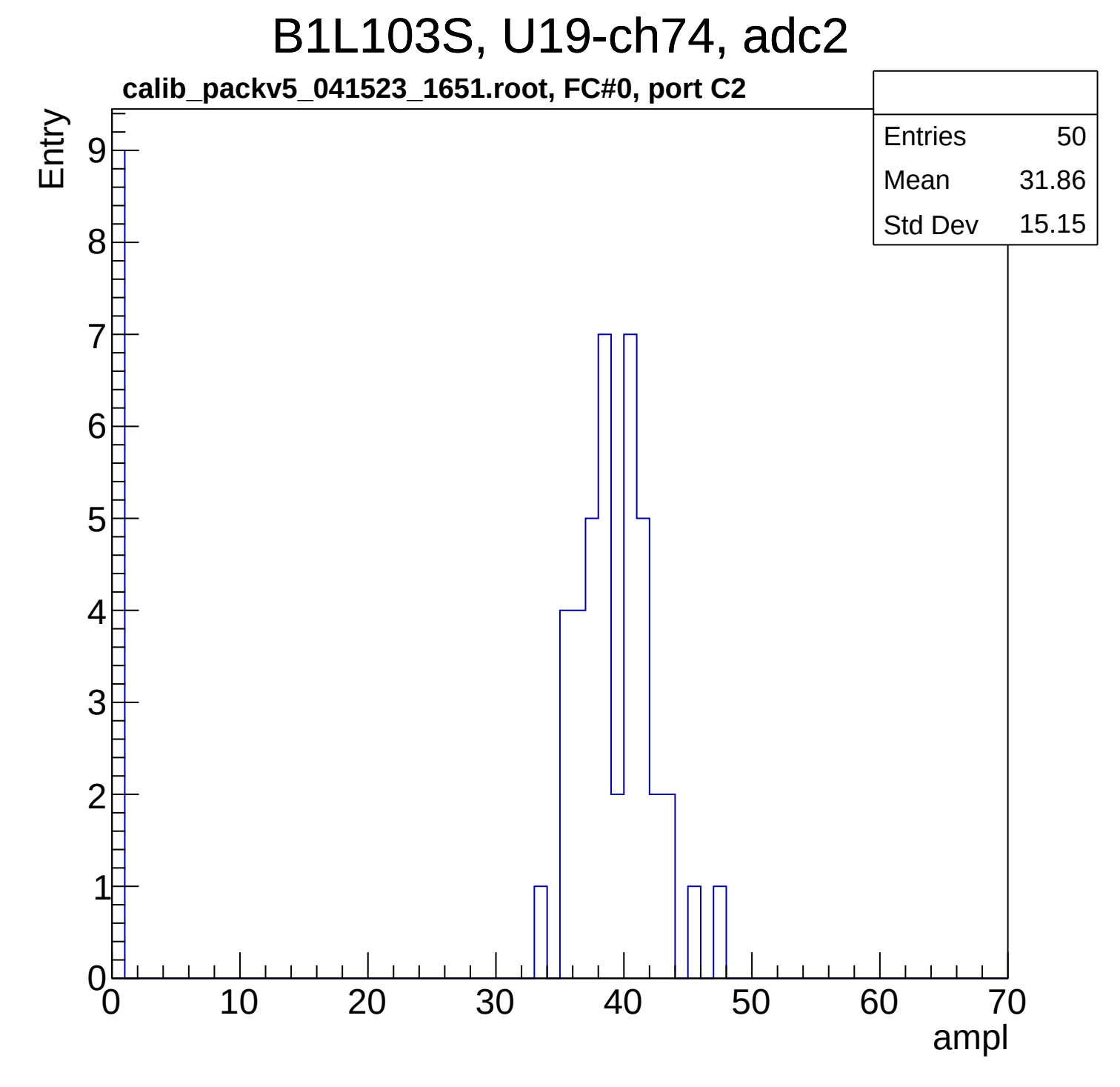
B1L103S, U19-ch74, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 31.86
Std Dev 15.15
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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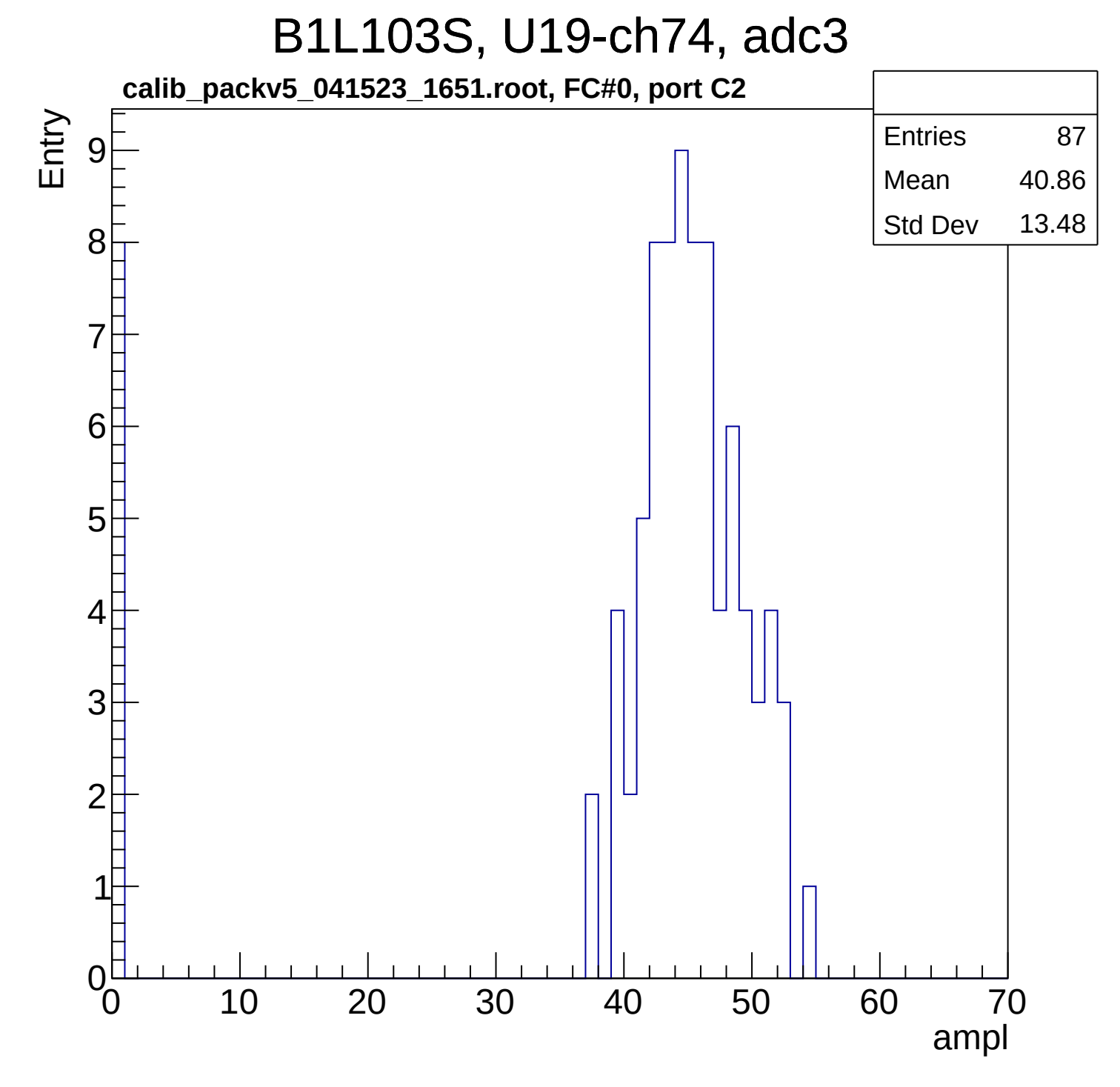
B1L103S, U19-ch74, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 40.86
Std Dev 13.48
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
50
60
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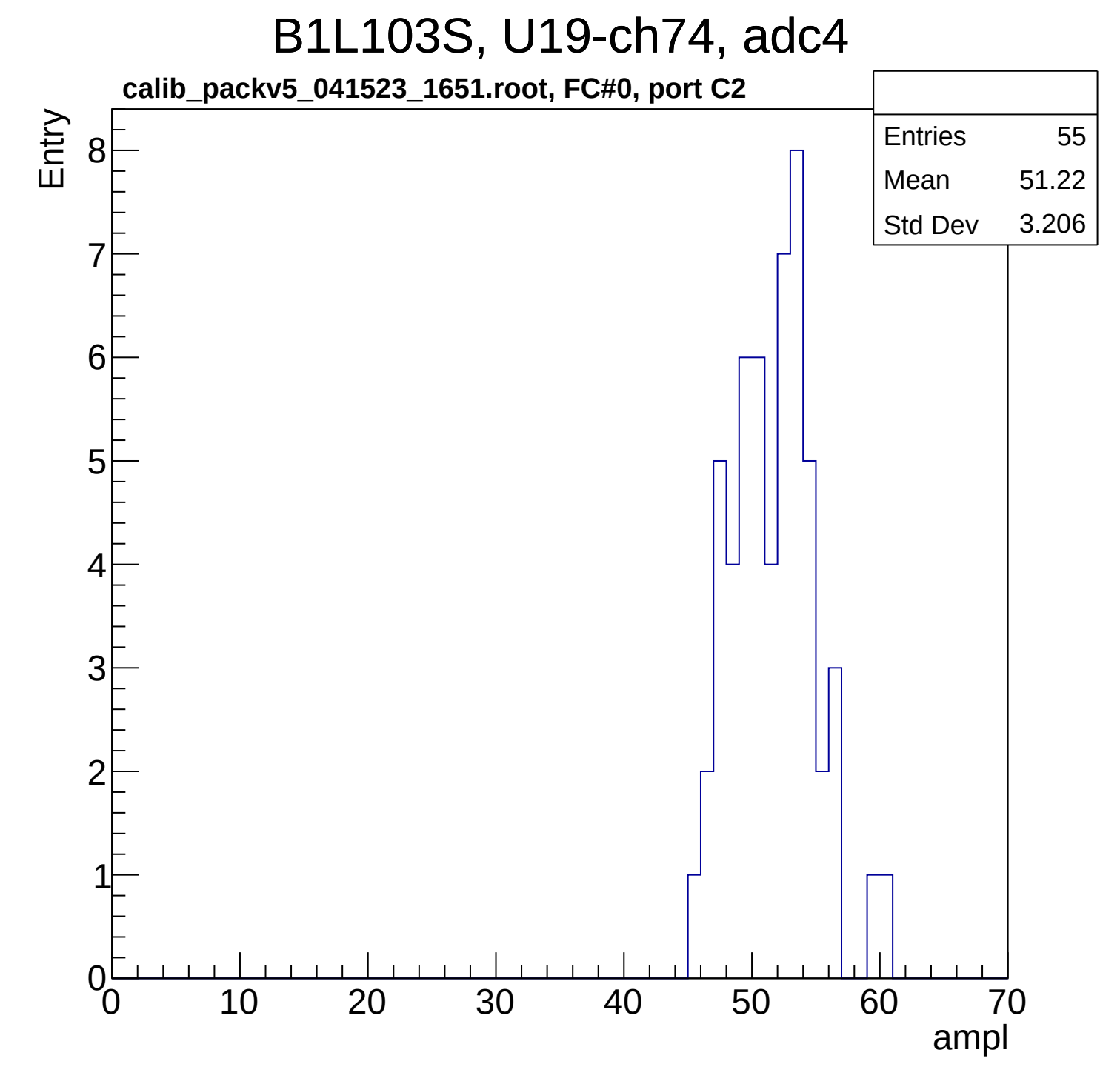
B1L103S, U19-ch74, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 51.22
Std Dev 3.206
Entry
ampl
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1
2
3
4
5
6
7
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0
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40
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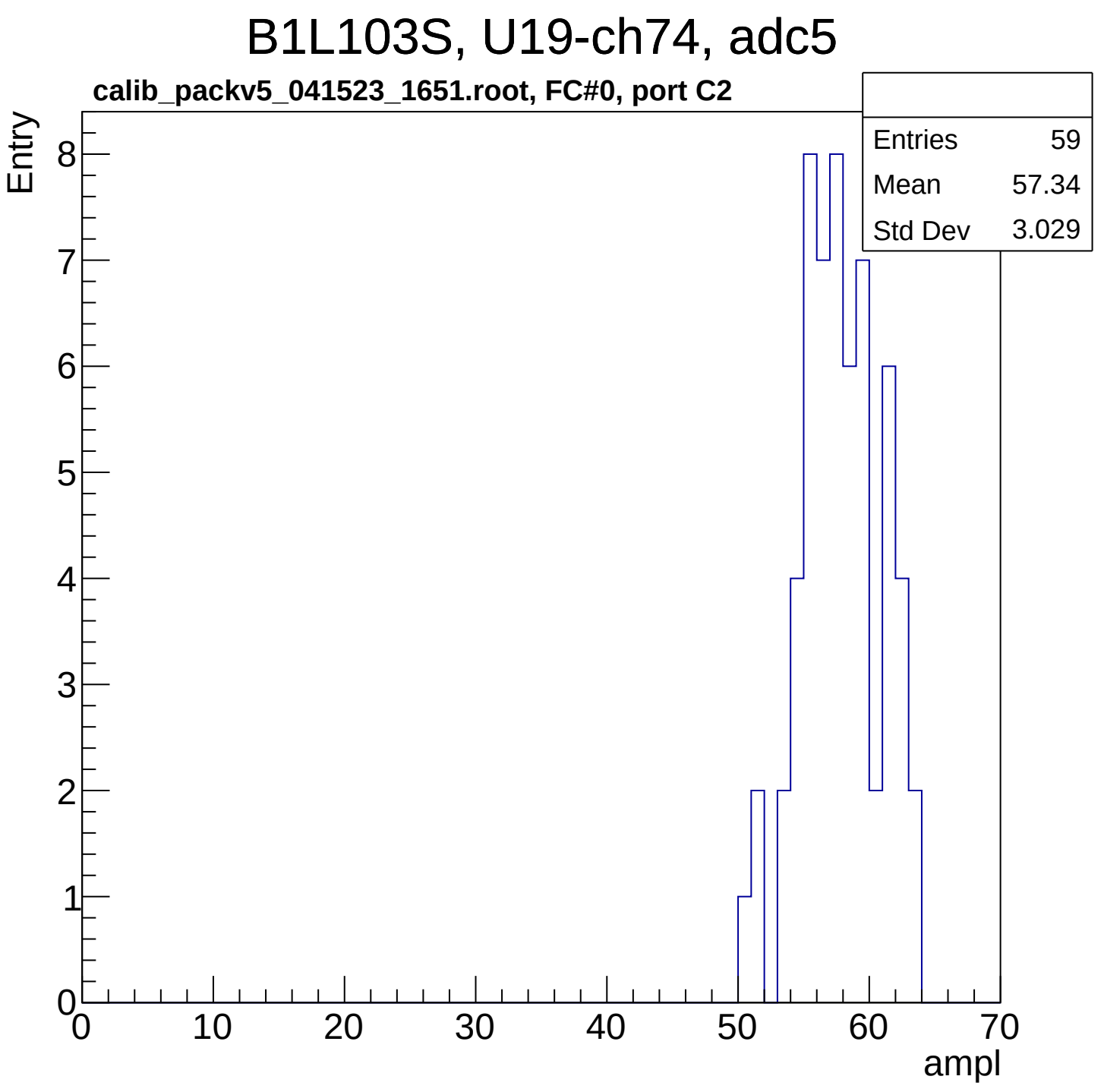
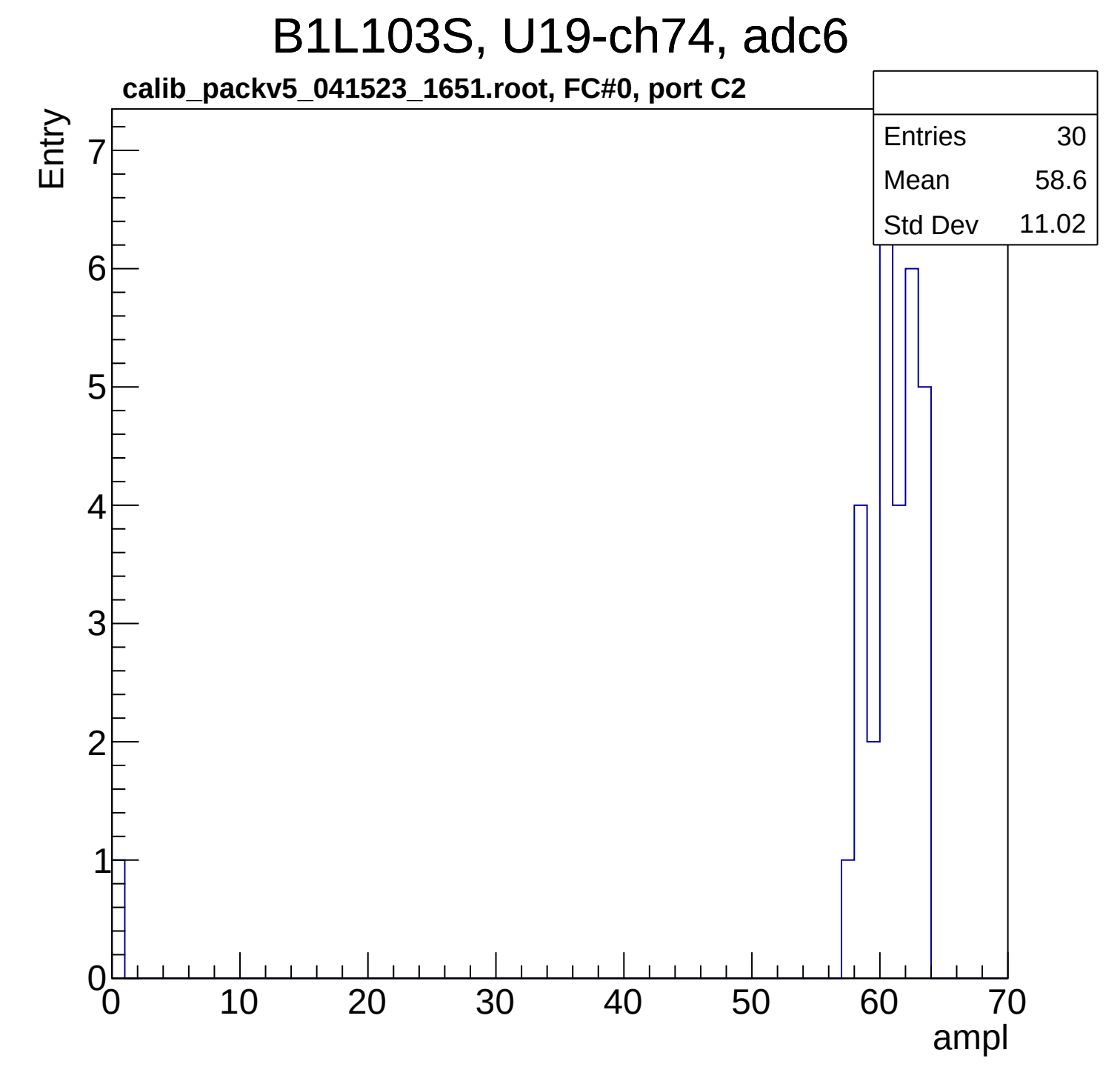
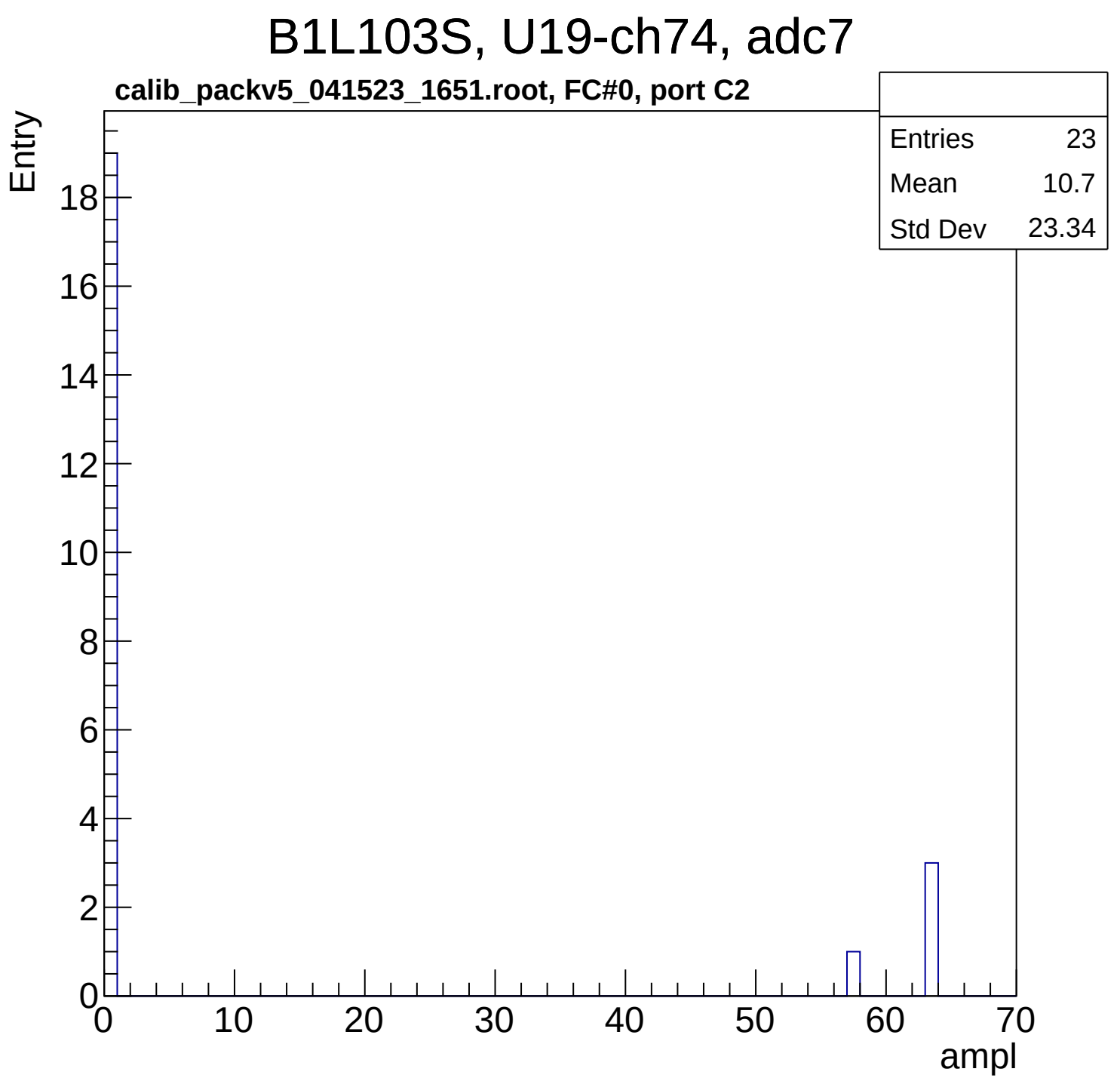
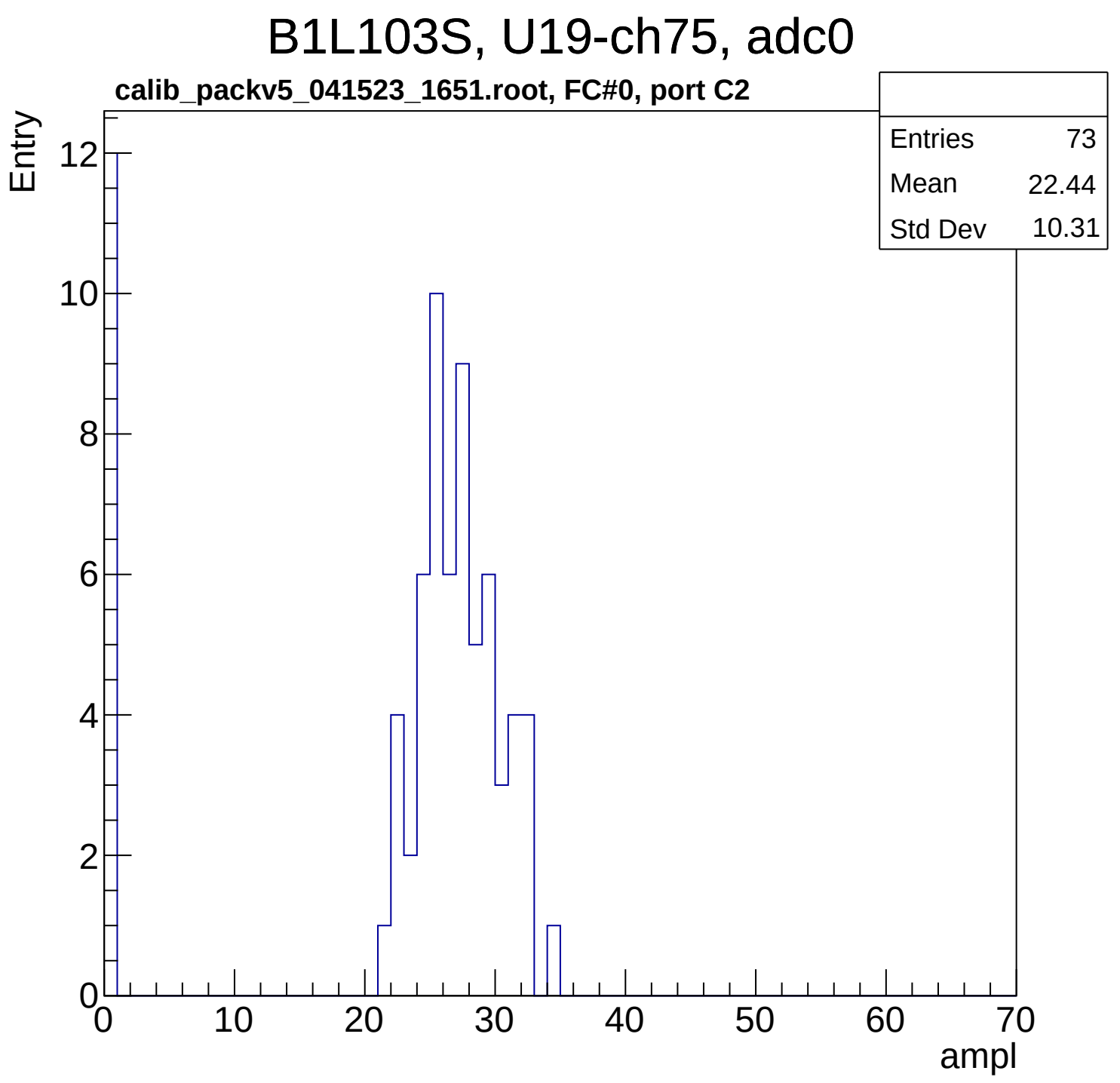
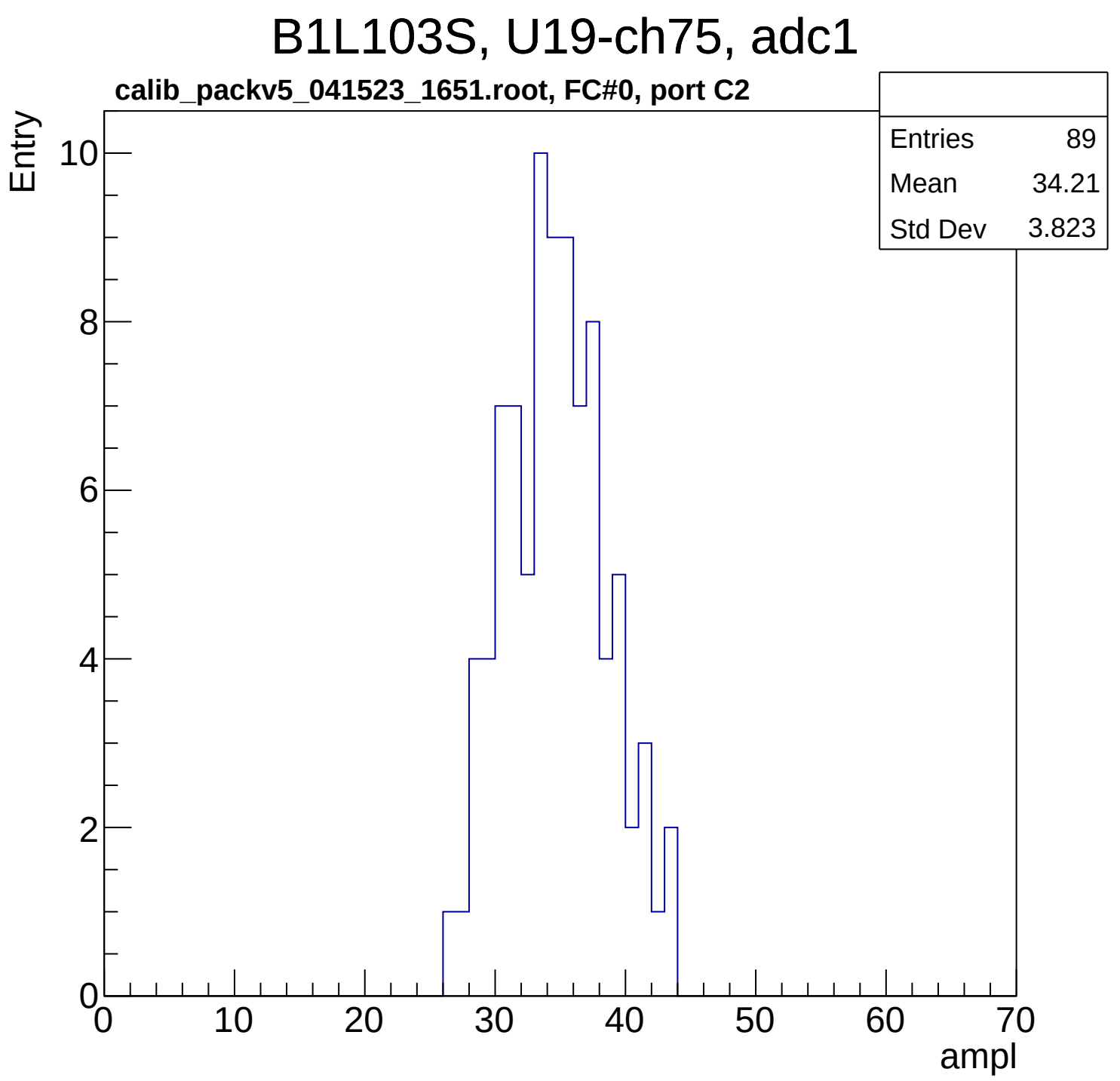
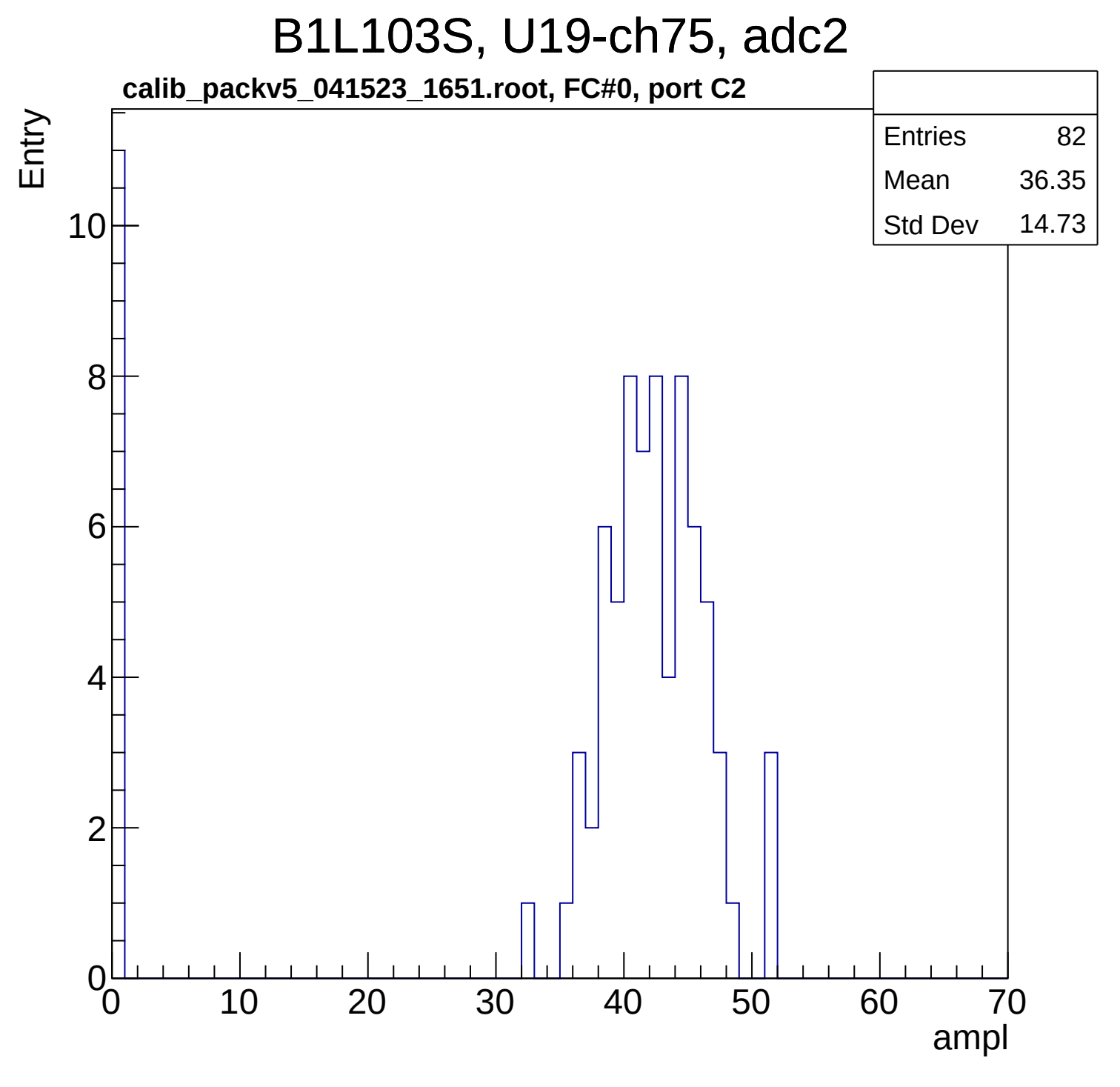

B1L103S, U19-ch74, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 57.34
Std Dev 3.029
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

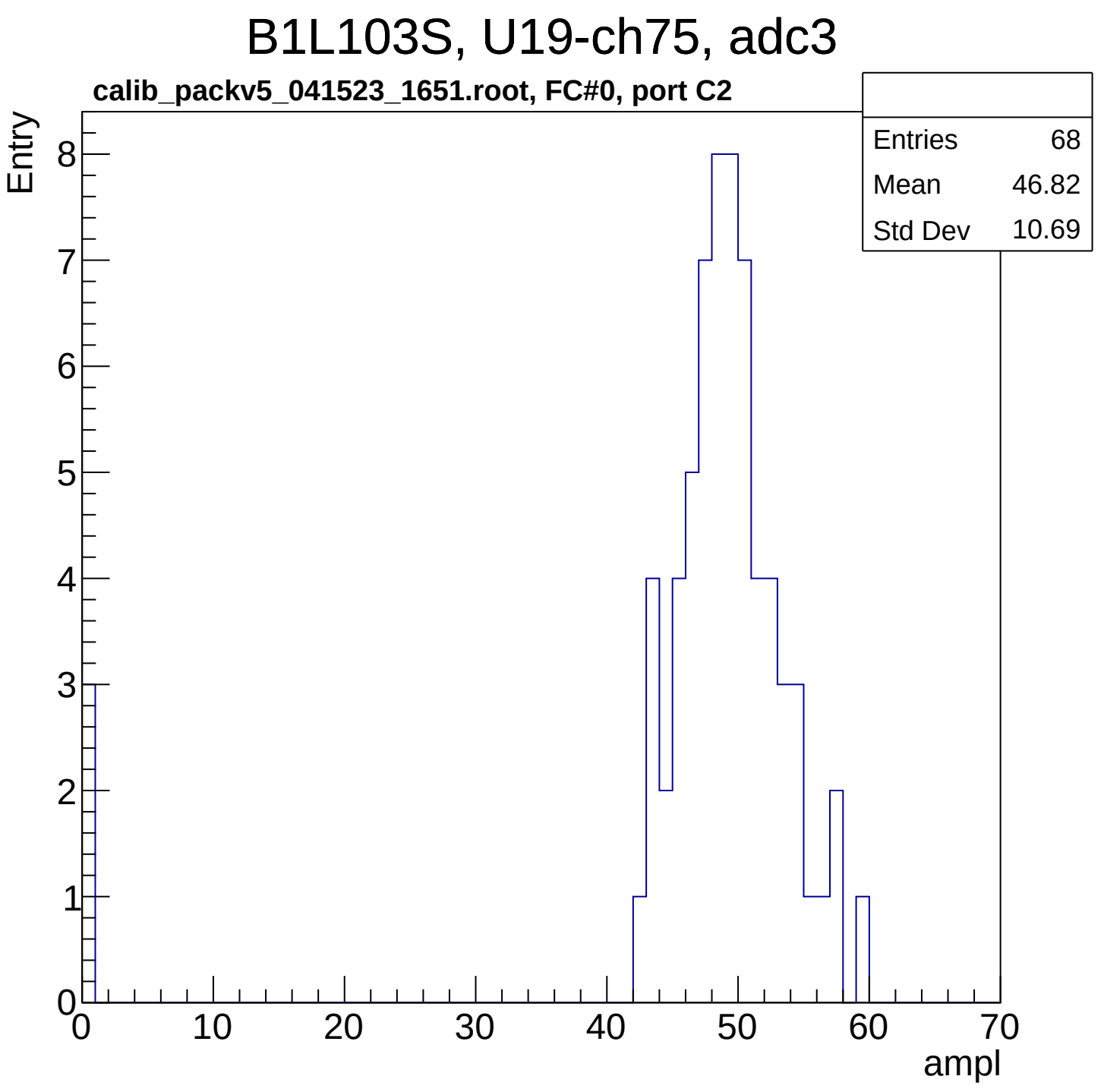

B1L103S, U19-ch74, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 58.6
Std Dev 11.02
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch74, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 10.7
Std Dev 23.34
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch75, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 22.44
Std Dev 10.31
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch75, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 34.21
Std Dev 3.823
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U19-ch75, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 36.35
Std Dev 14.73
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch75, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 46.82
Std Dev 10.69
Entry
ampl
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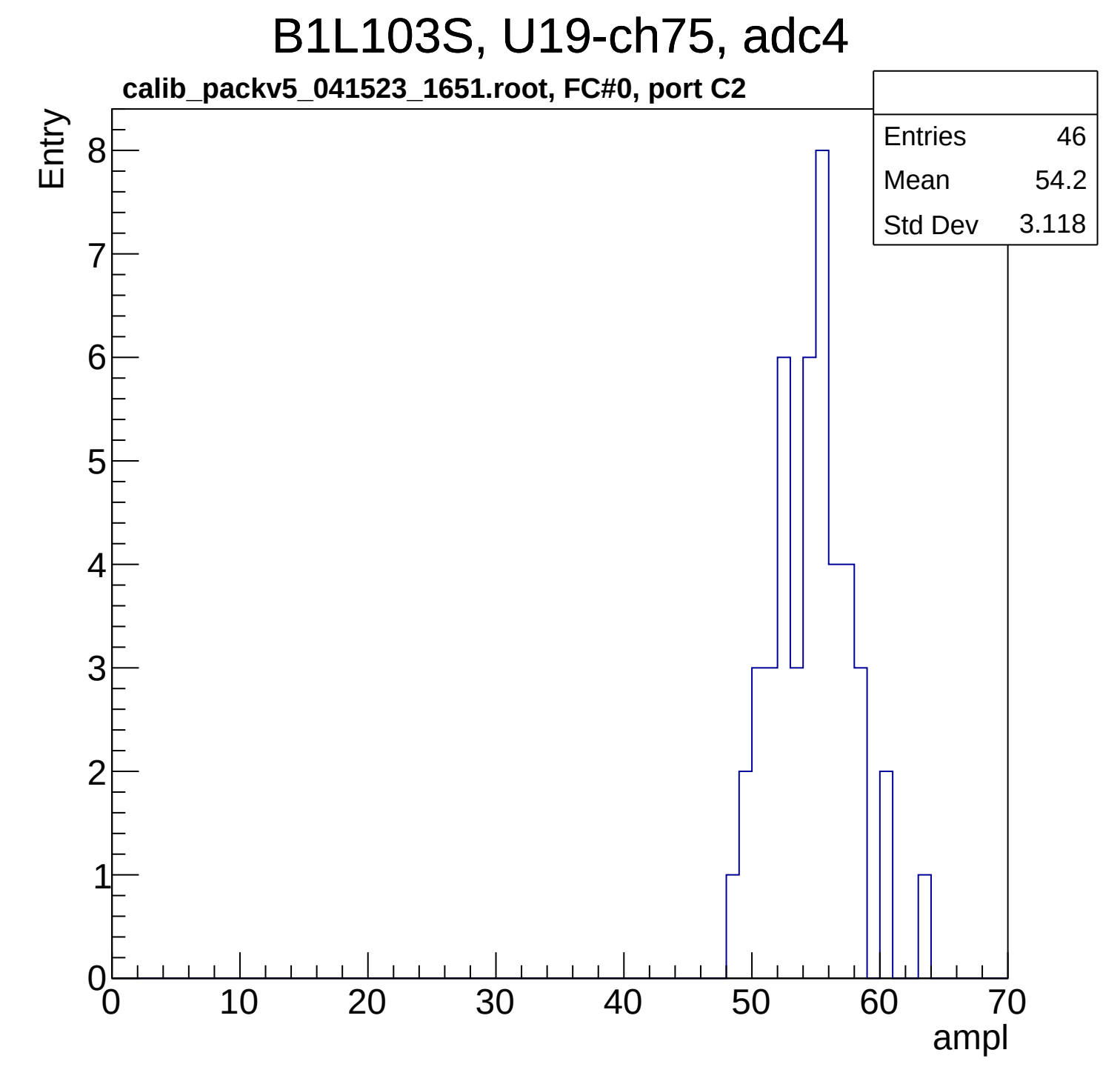
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch75, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 54.2
Std Dev 3.118
Entry
ampl
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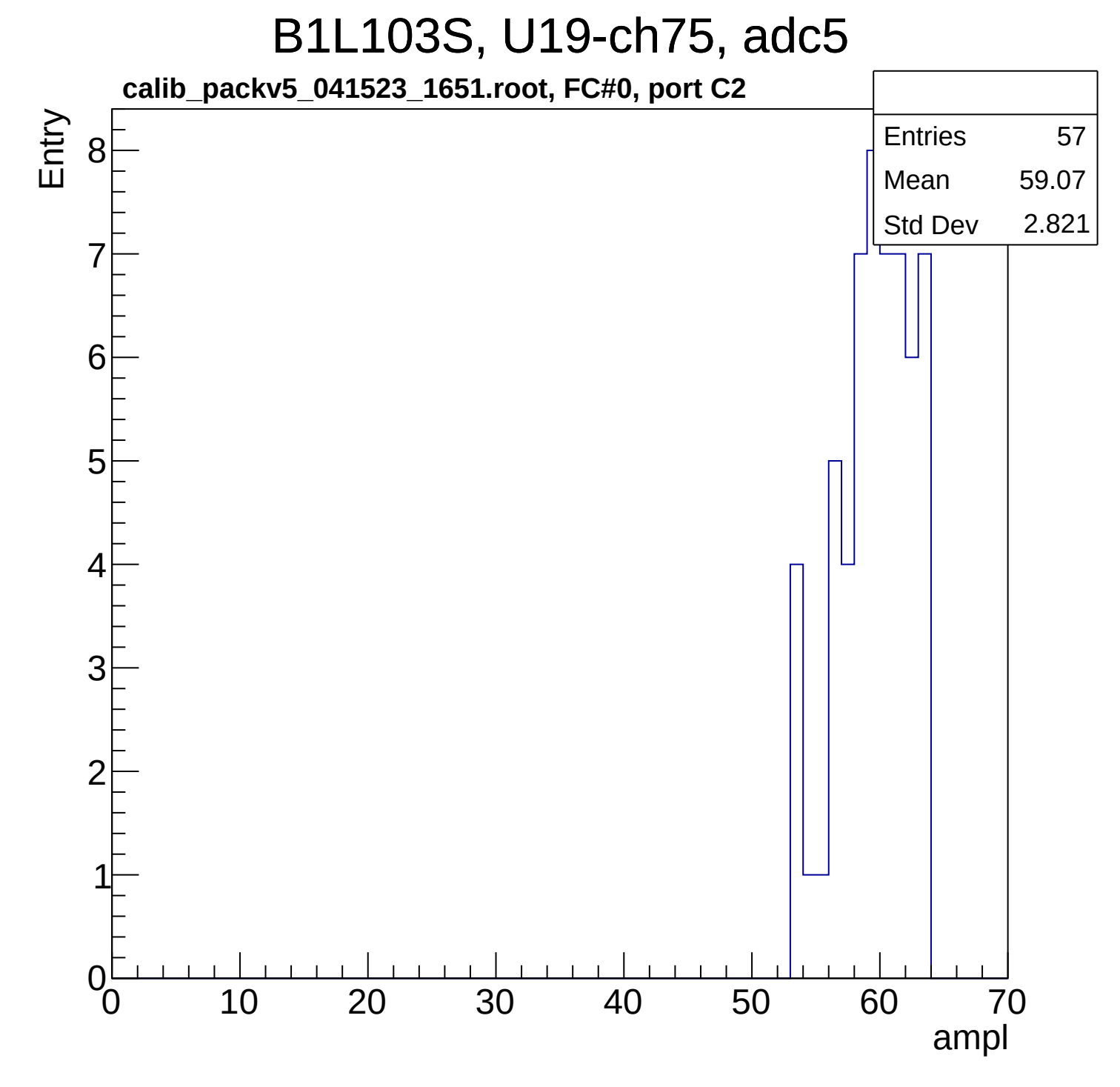
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch75, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 59.07
Std Dev 2.821
Entry
ampl
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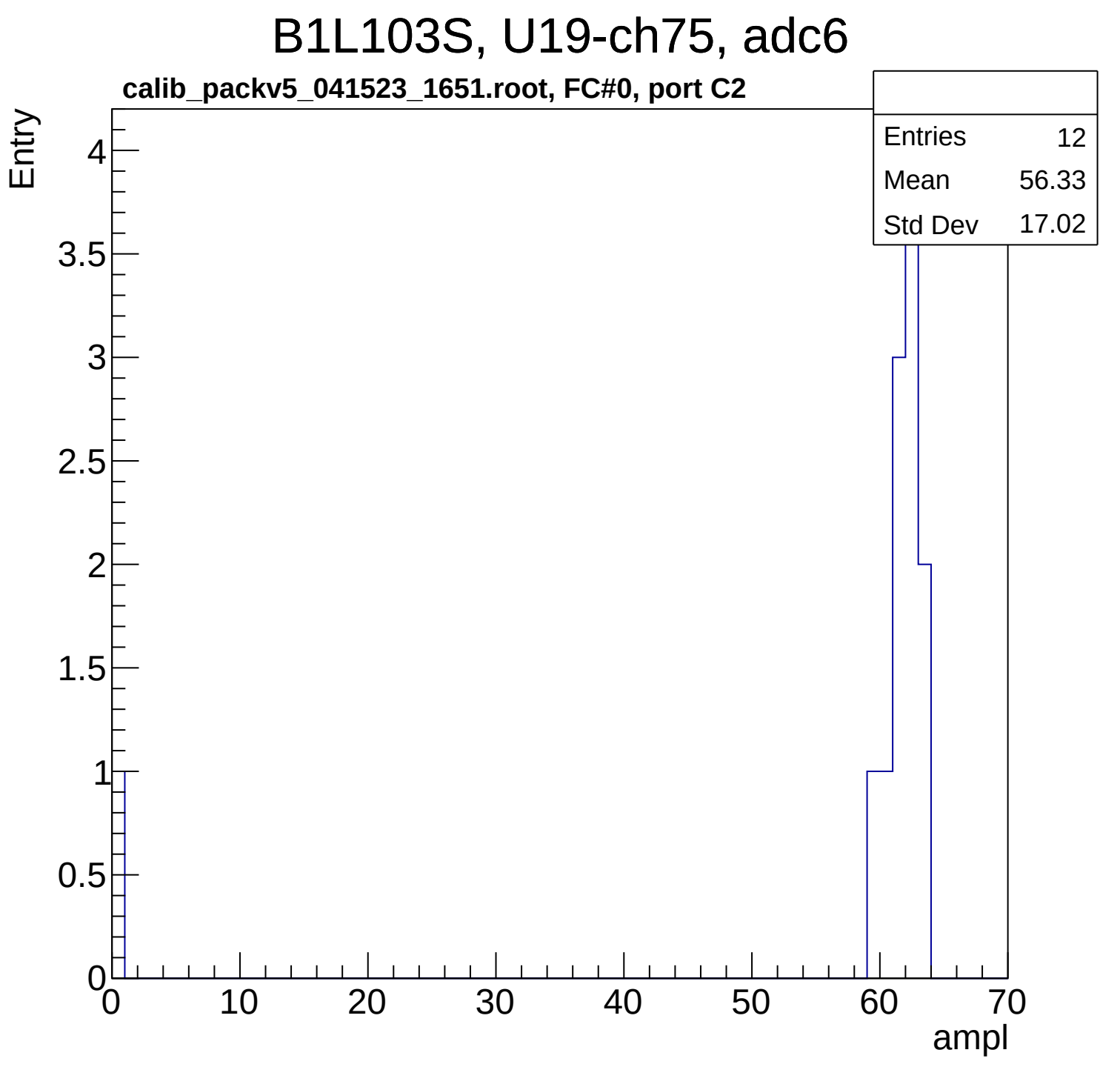
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch75, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 56.33
Std Dev 17.02
Entry
ampl
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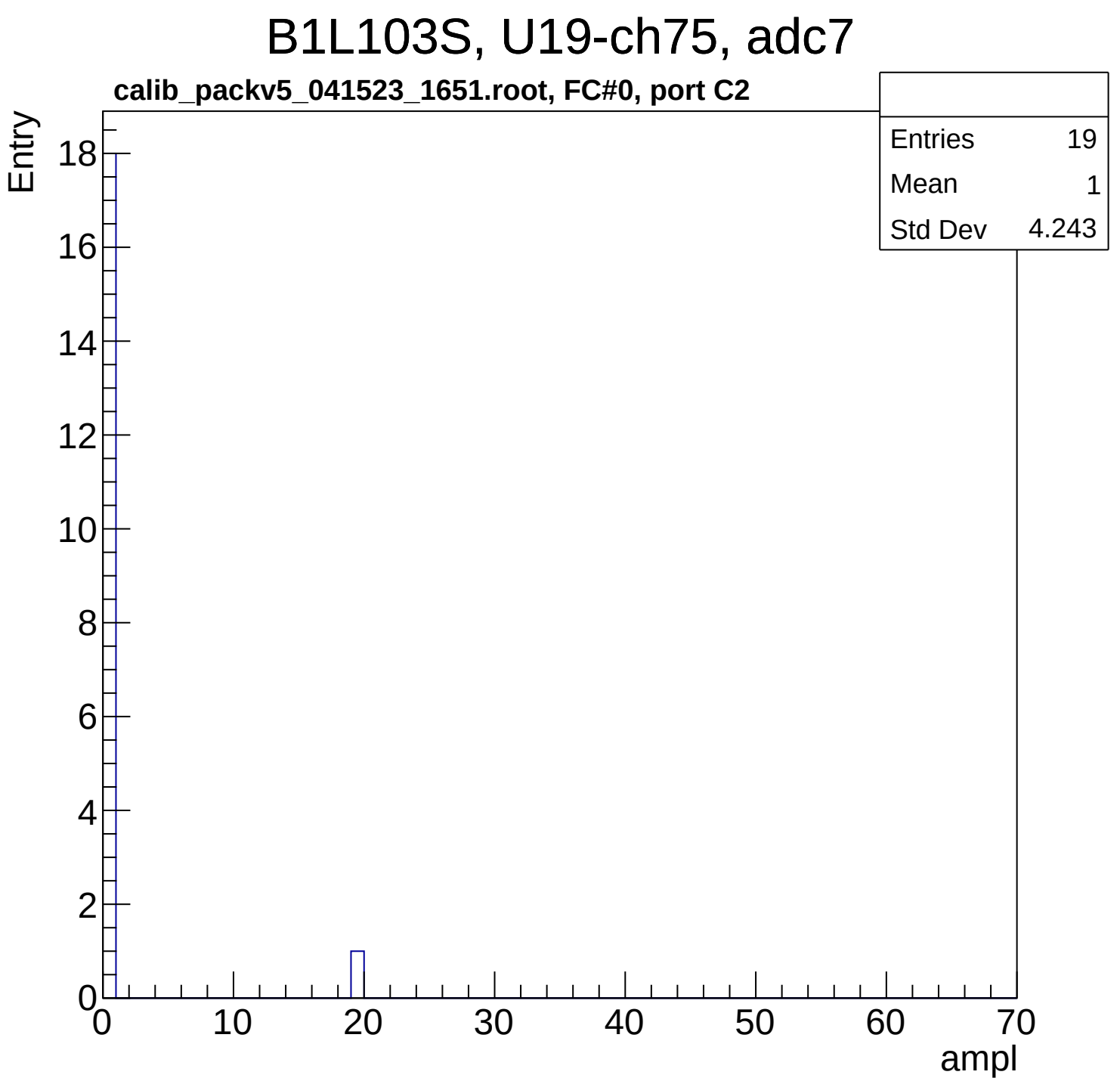
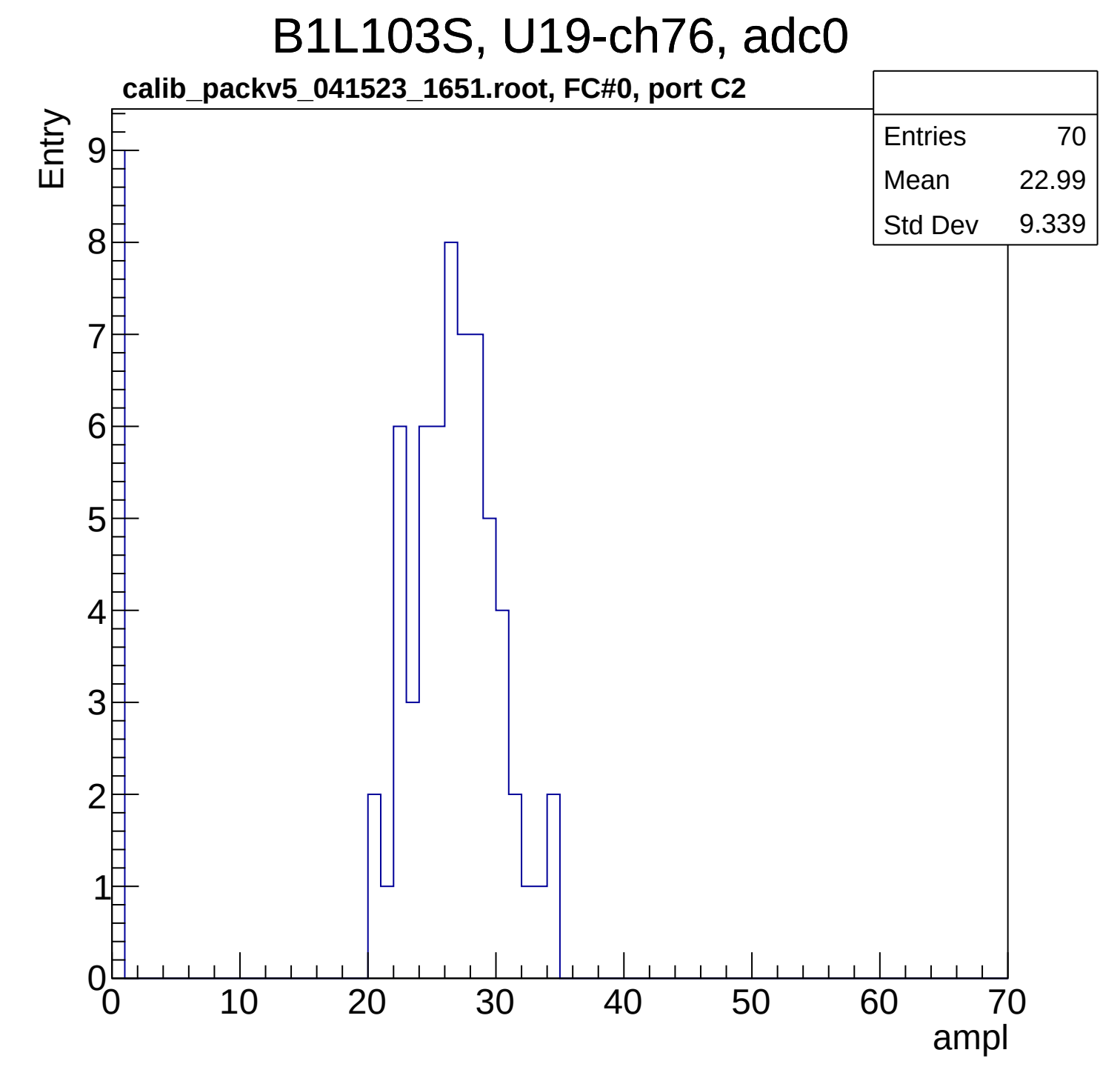
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U19-ch75, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1
Std Dev 4.243
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch76, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 22.99
Std Dev 9.339
Entry
ampl
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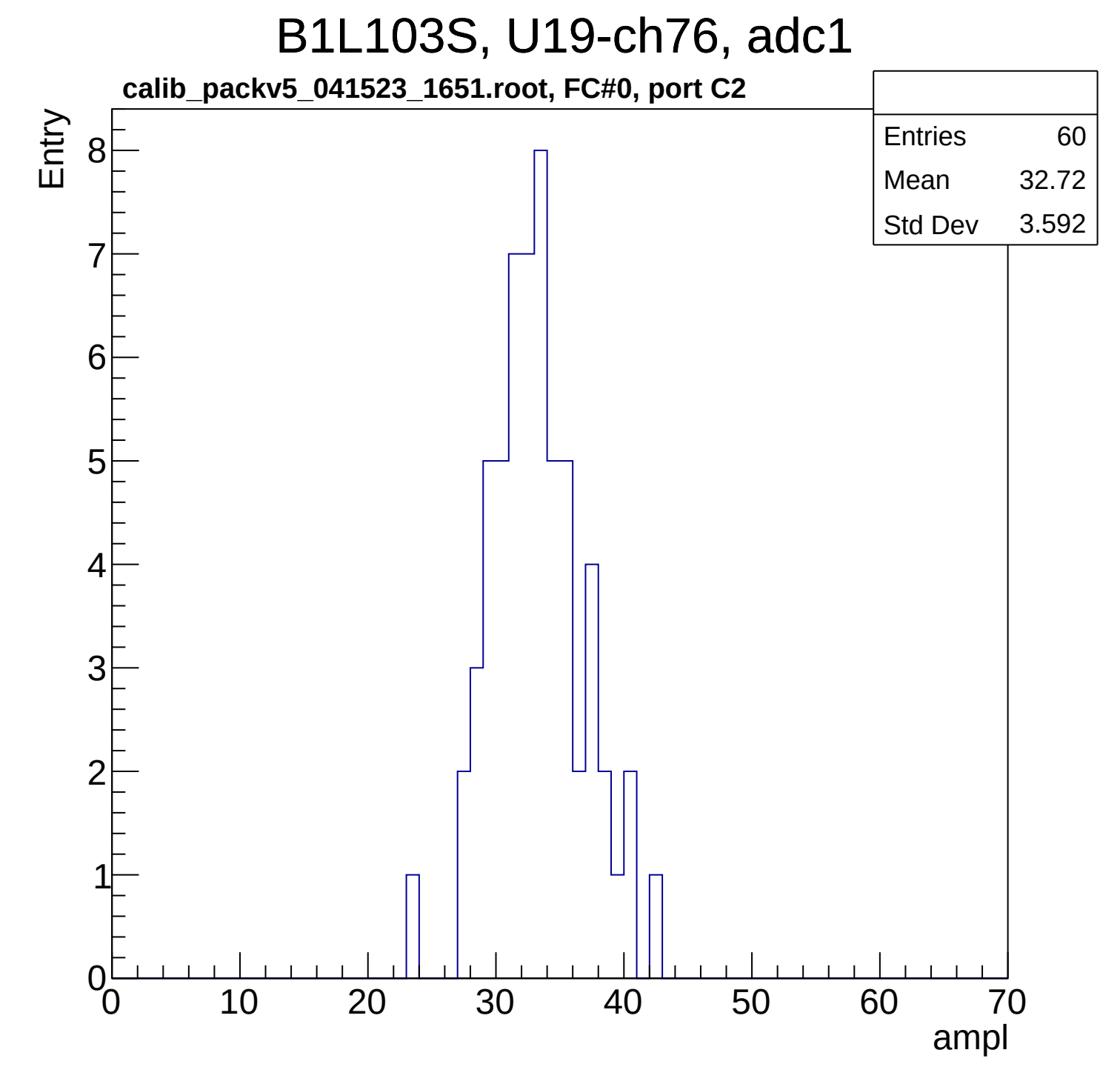
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch76, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 32.72
Std Dev 3.592
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
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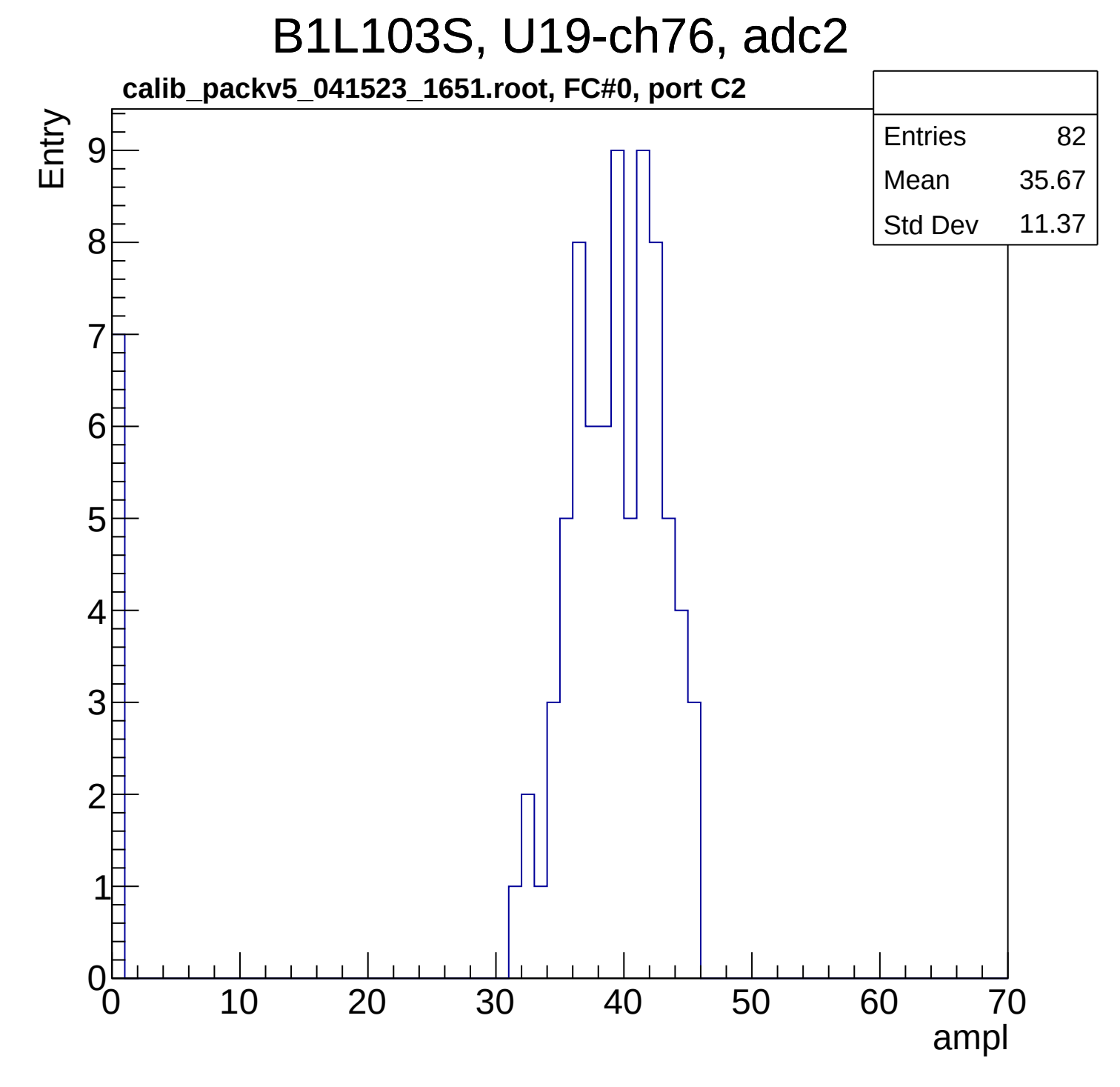
40
50
60
70


B1L103S, U19-ch76, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 35.67
Std Dev 11.37
Entry
ampl
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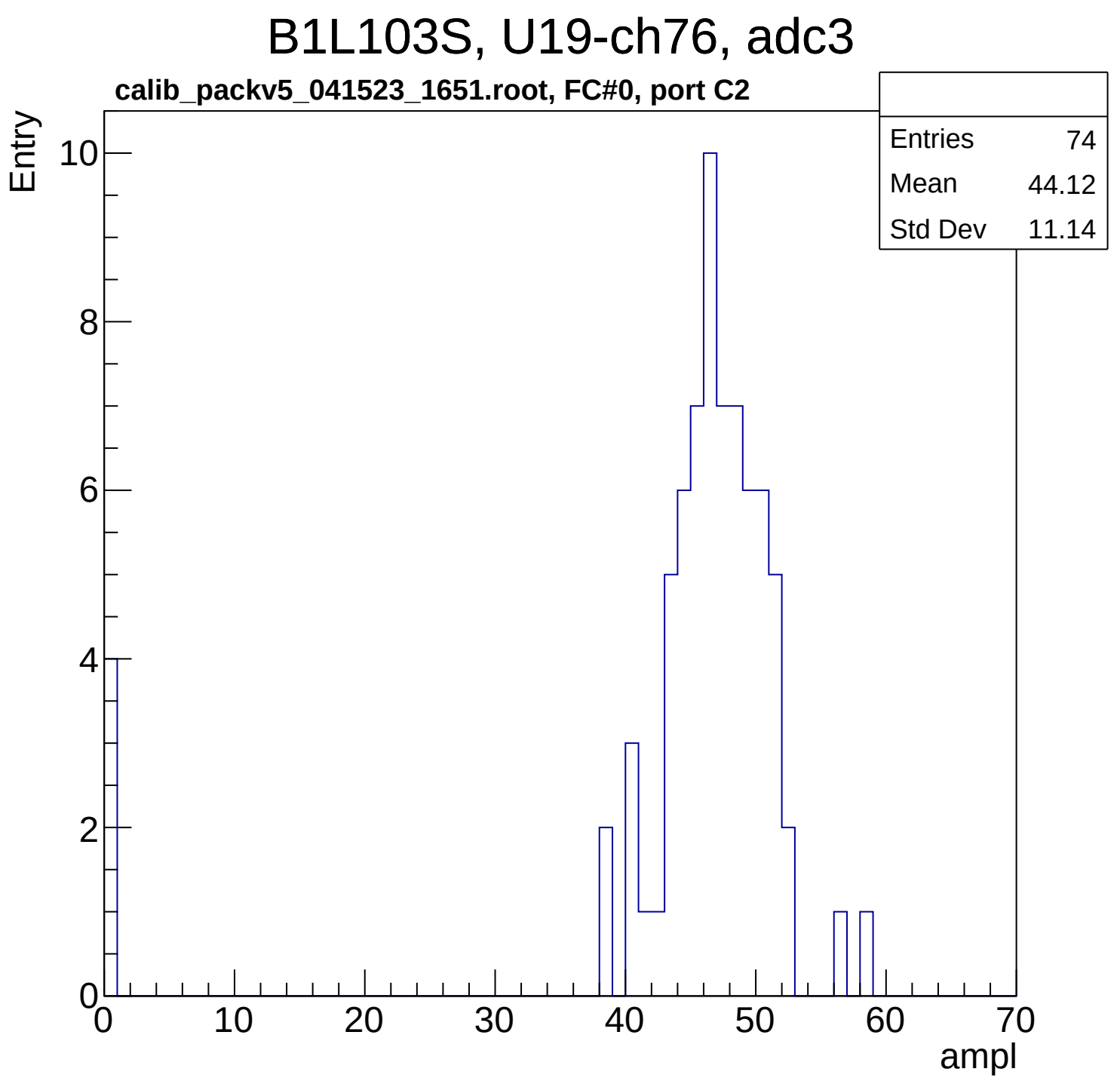
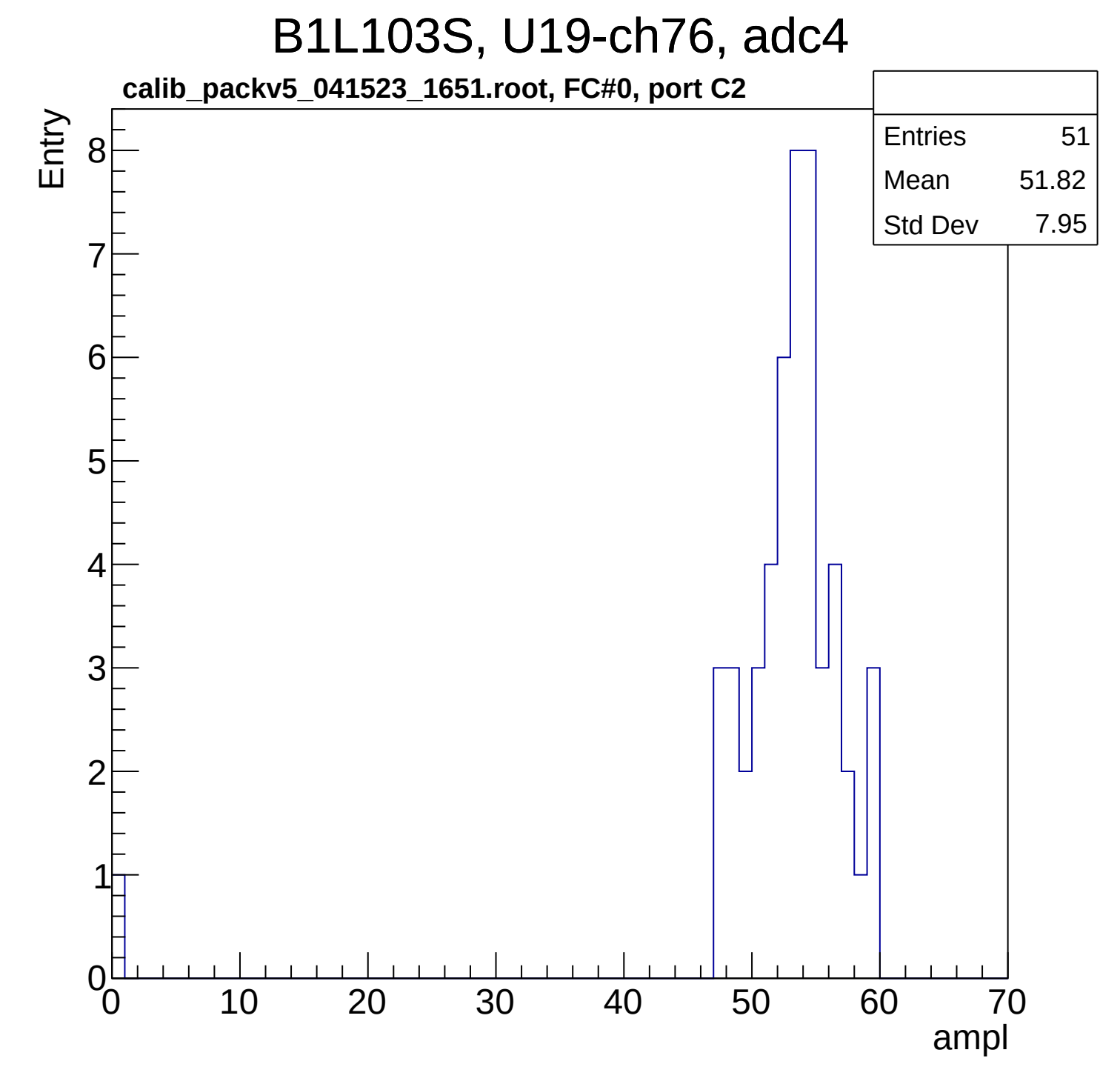
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch76, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 44.12
Std Dev 11.14
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch76, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 51.82
Std Dev 7.95
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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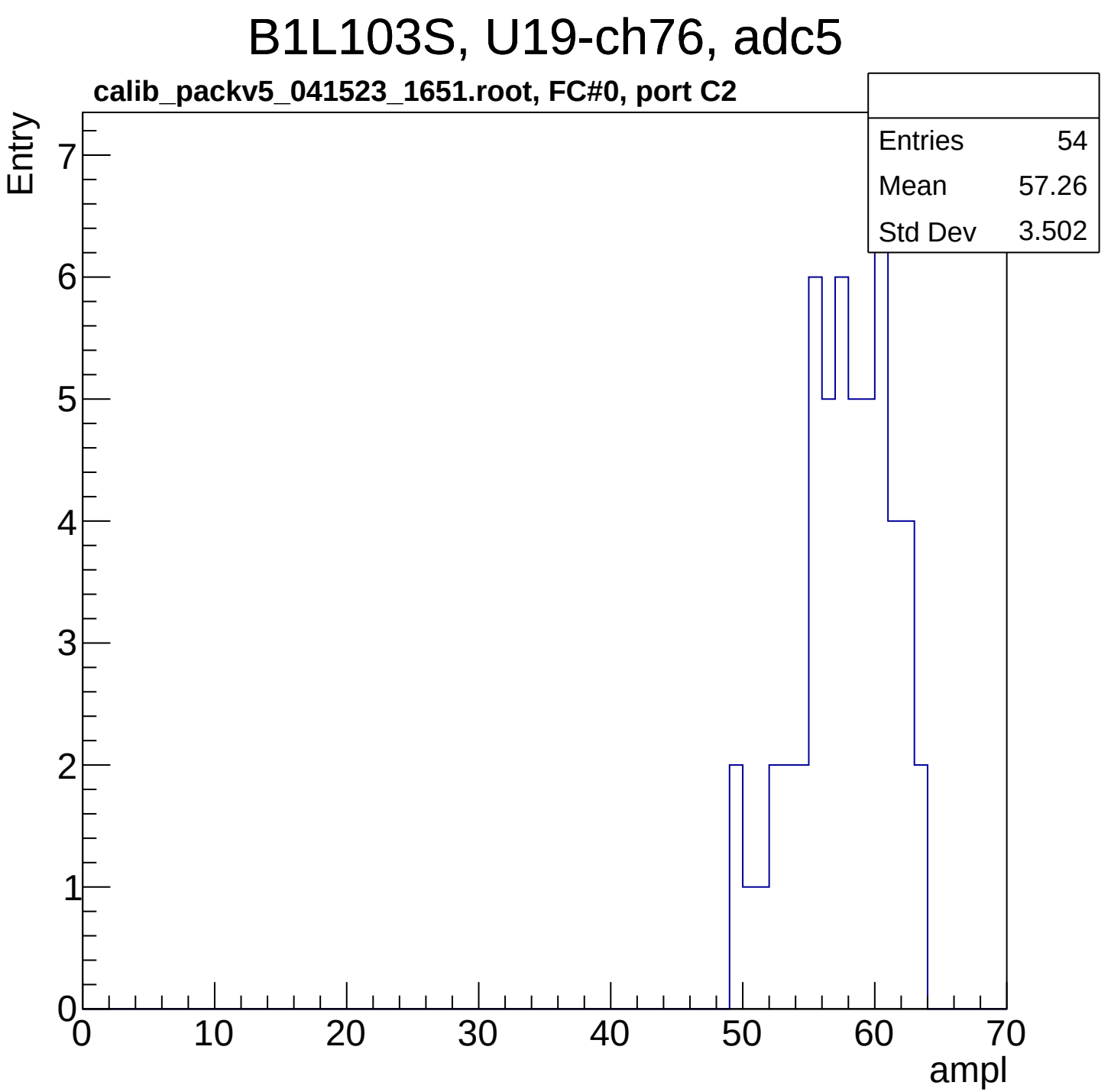
40
50
60
70


B1L103S, U19-ch76, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 57.26
Std Dev 3.502
Entry
ampl
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1
2
3
4
5
6
7
0
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40
50
60
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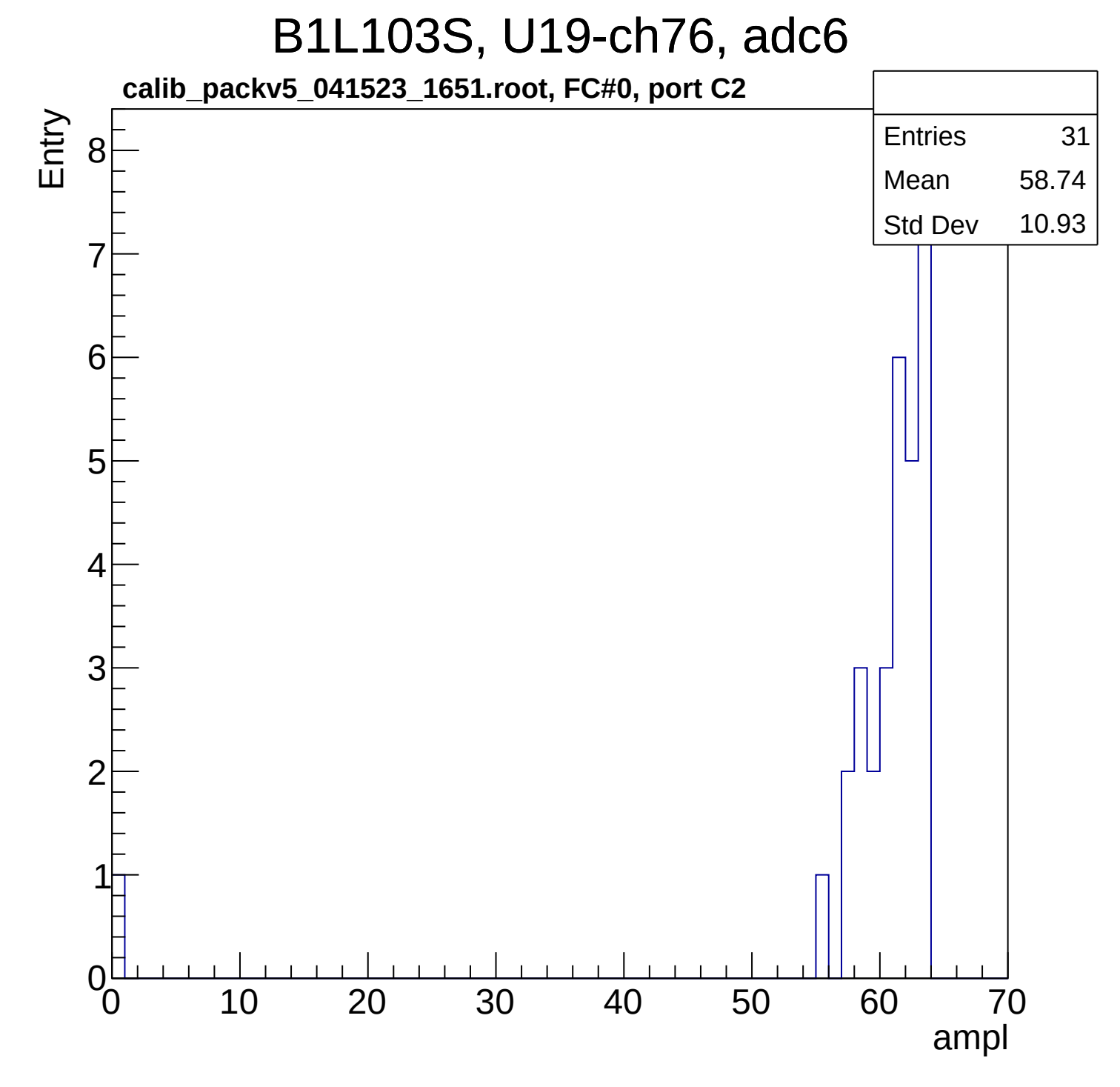
B1L103S, U19-ch76, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 58.74
Std Dev 10.93
Entry
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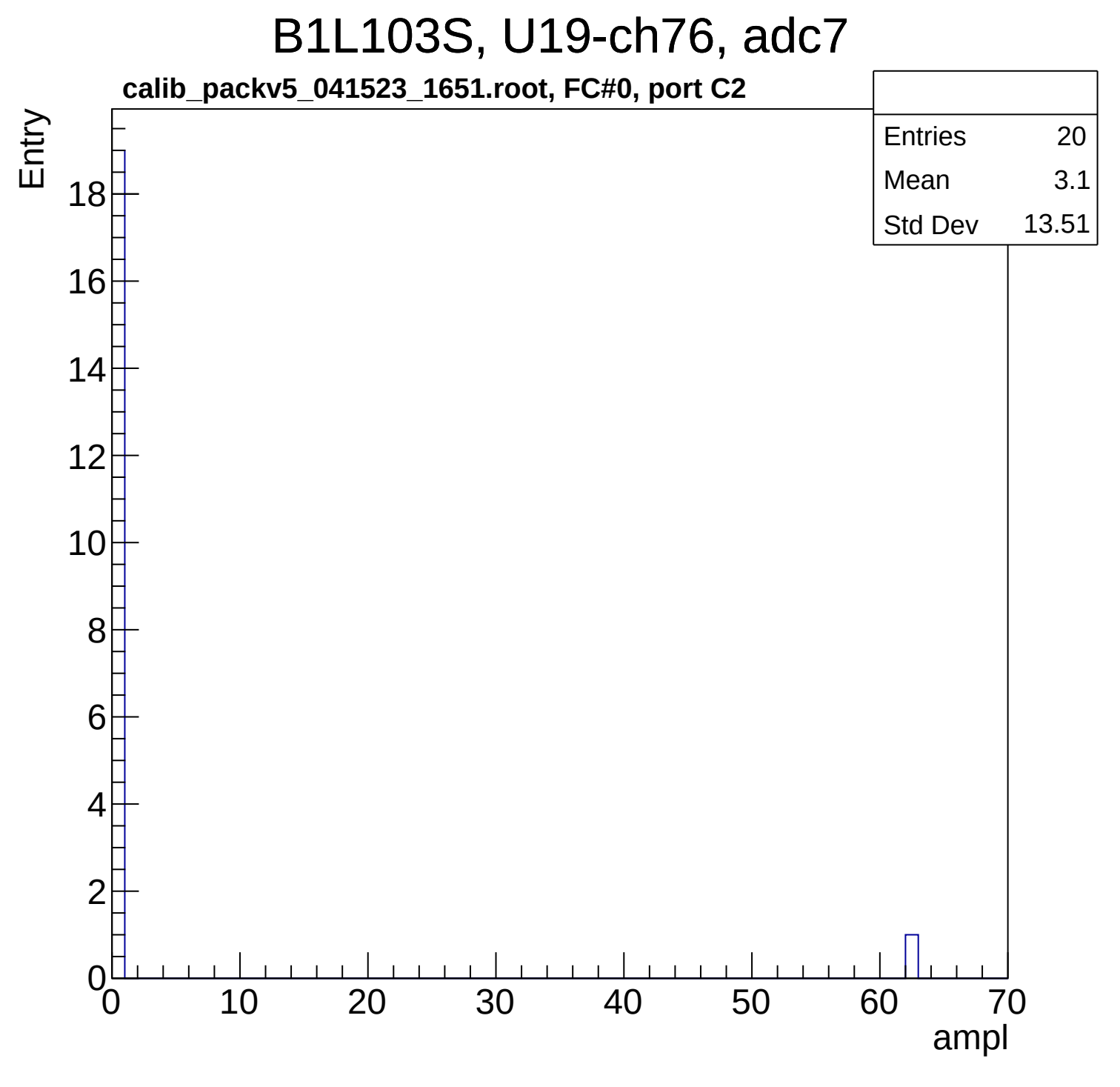
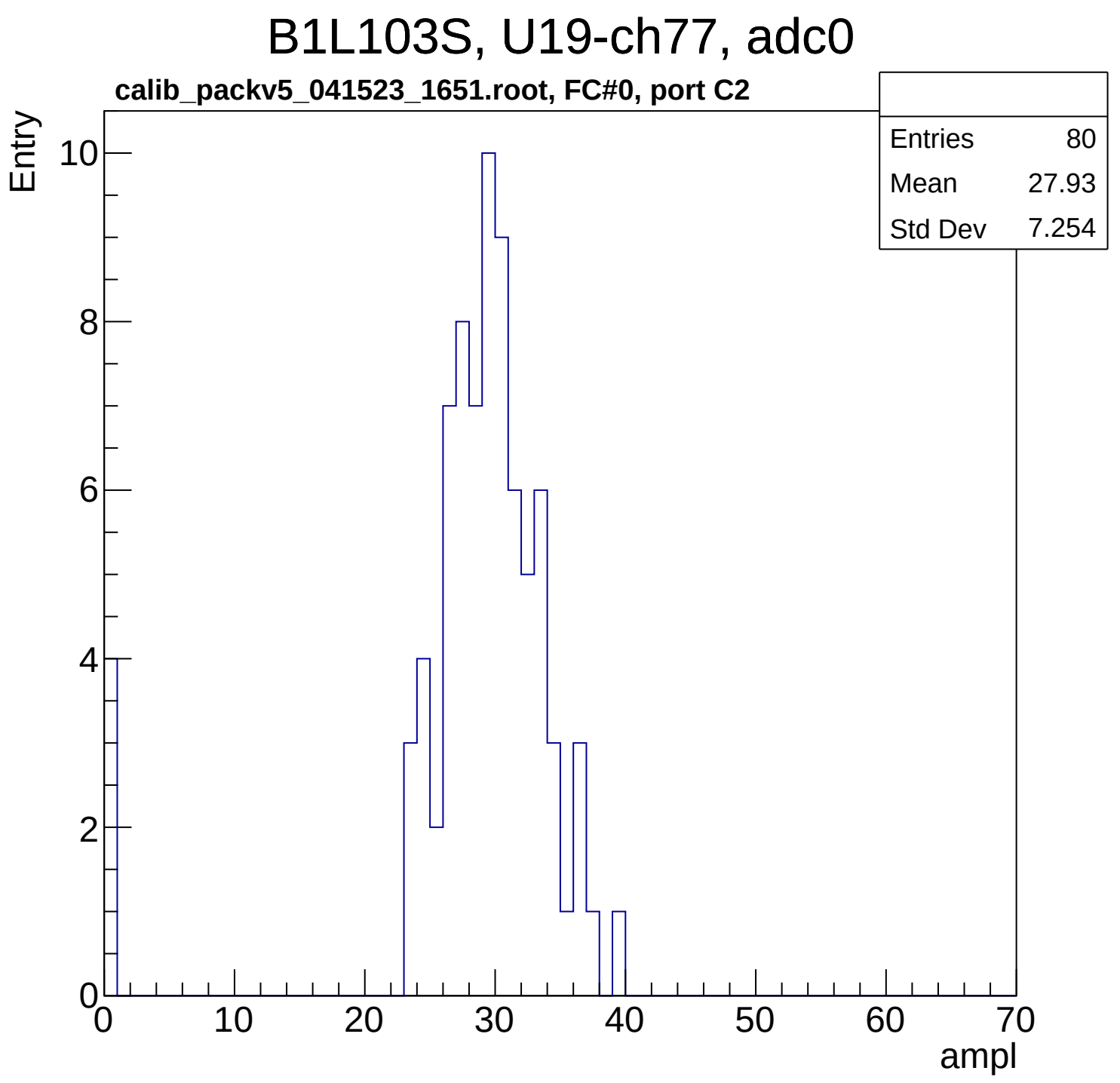
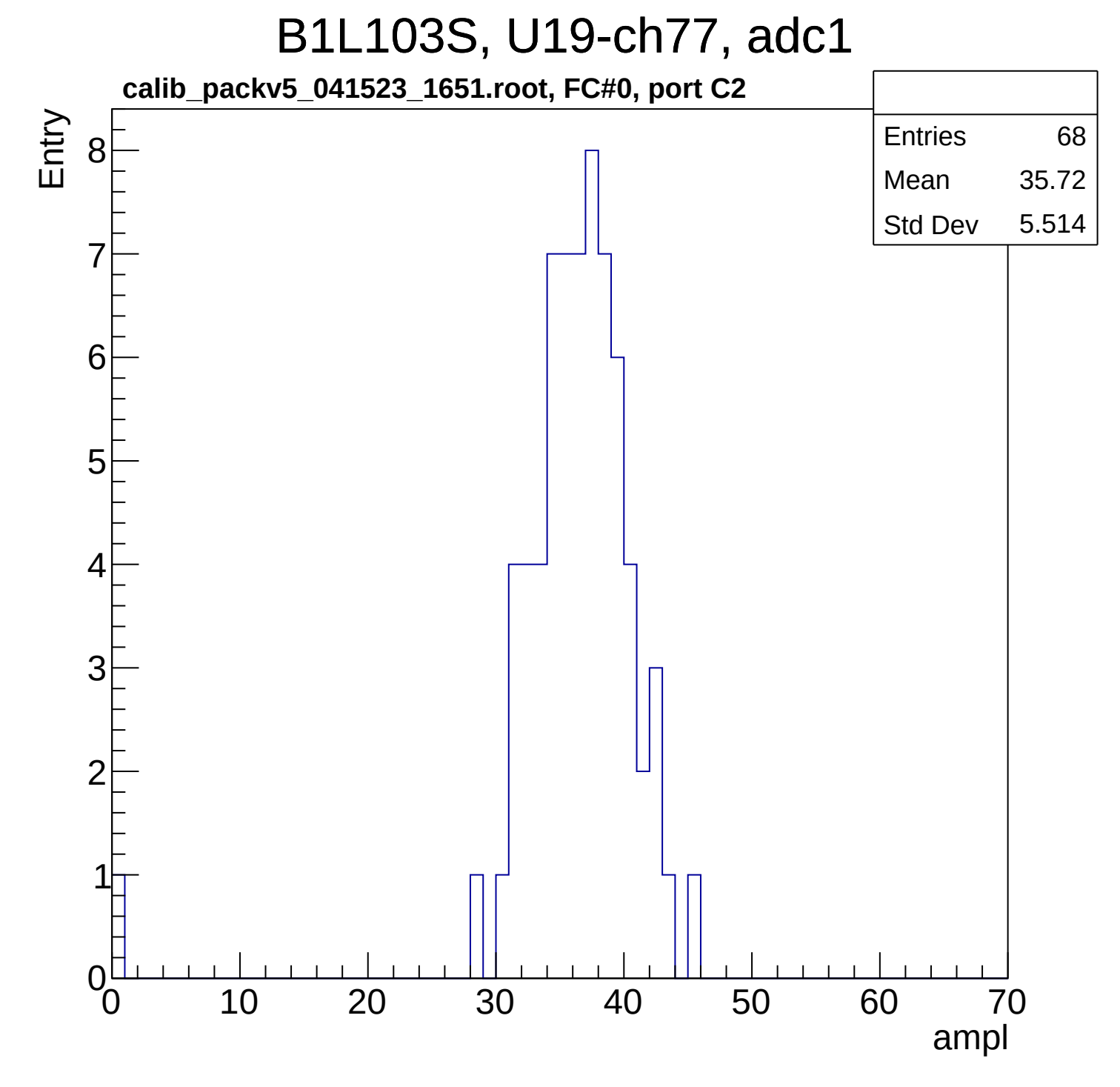
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch76, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch77, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 27.93
Std Dev 7.254
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U19-ch77, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 35.72
Std Dev 5.514
Entry
ampl
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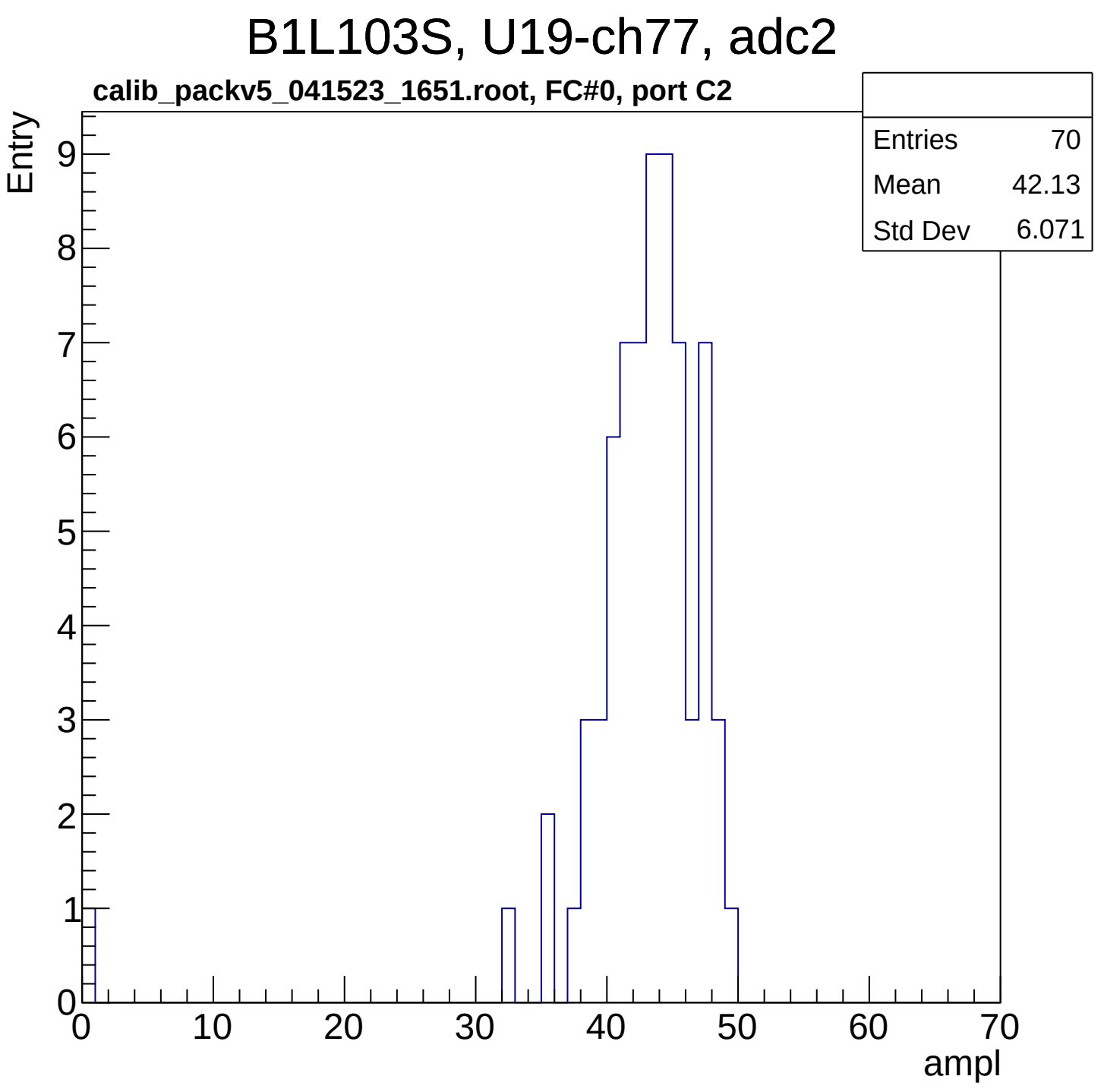
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch77, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 42.13
Std Dev 6.071
Entry
ampl
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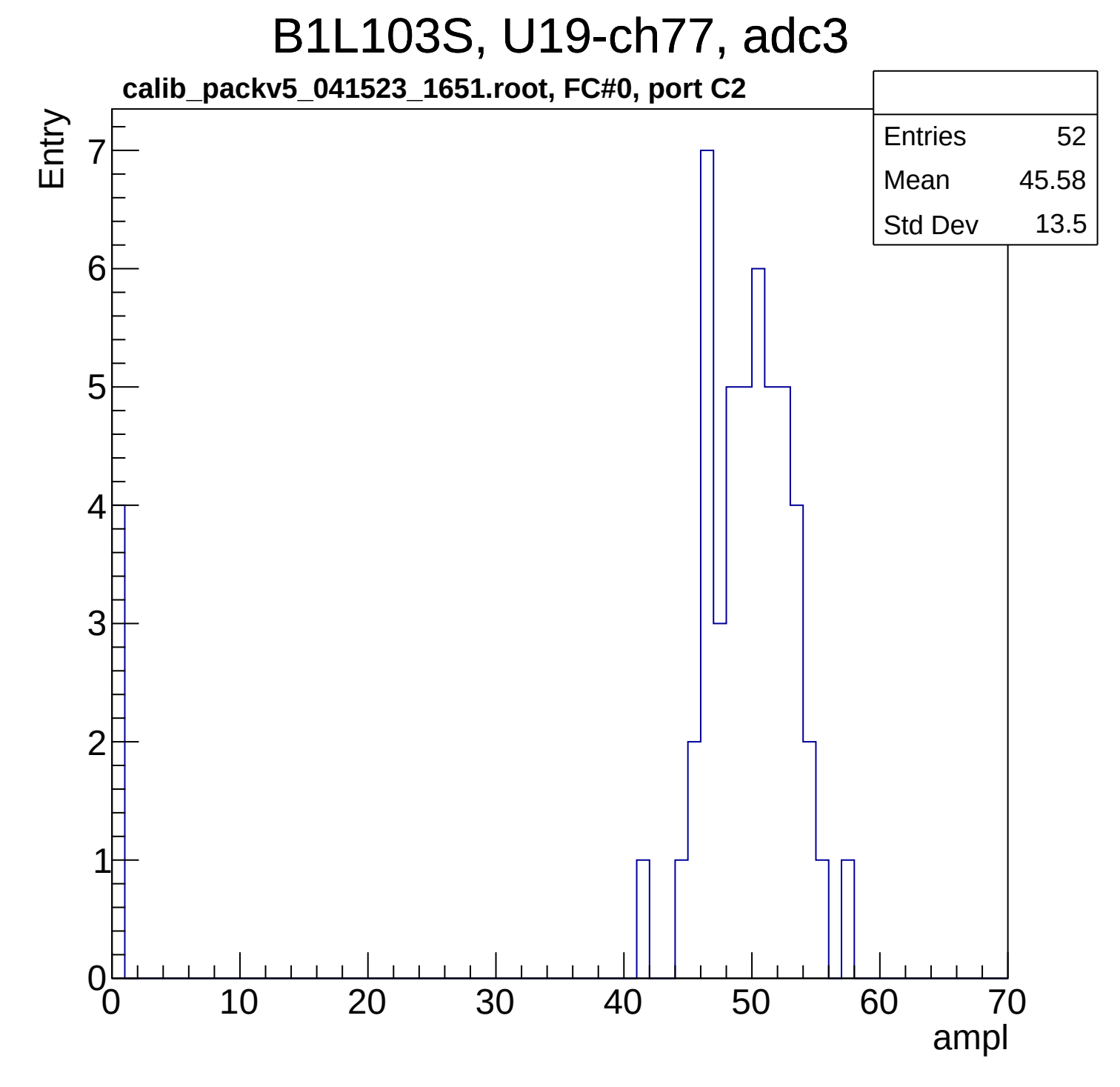
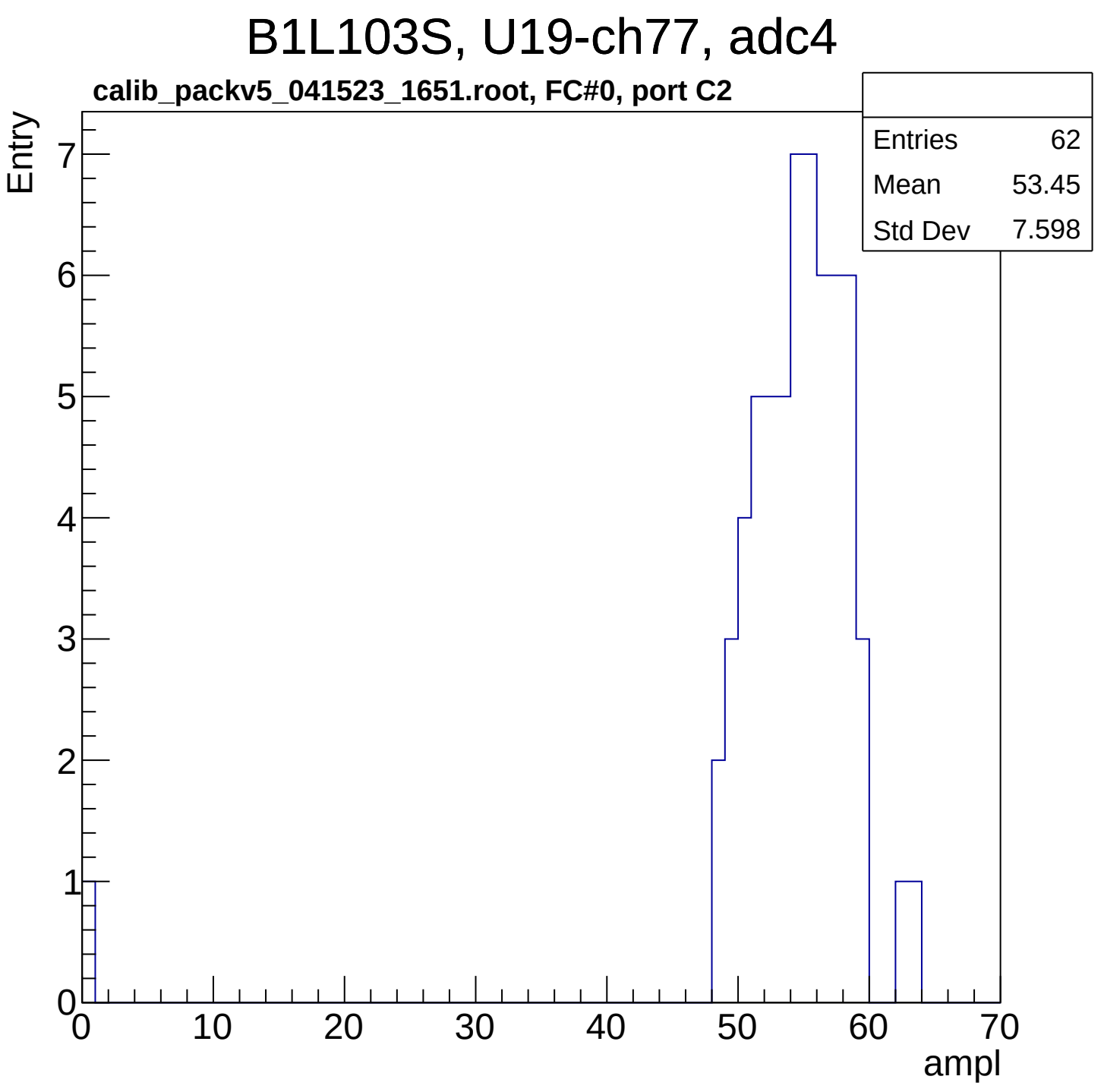
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch77, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 45.58
Std Dev 13.5
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch77, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 53.45
Std Dev 7.598
Entry
ampl
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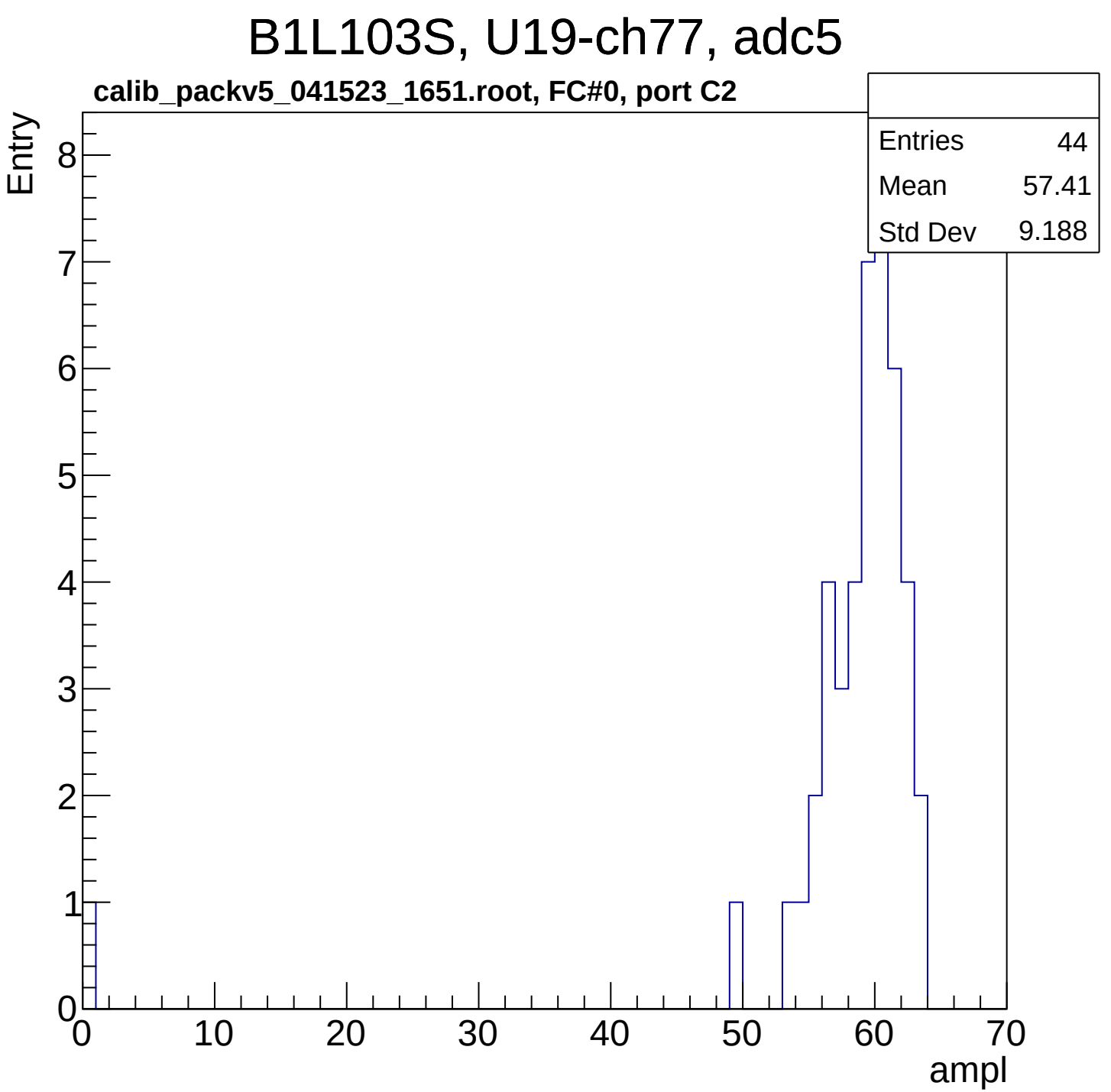
B1L103S, U19-ch77, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 57.41
Std Dev 9.188
Entry
ampl
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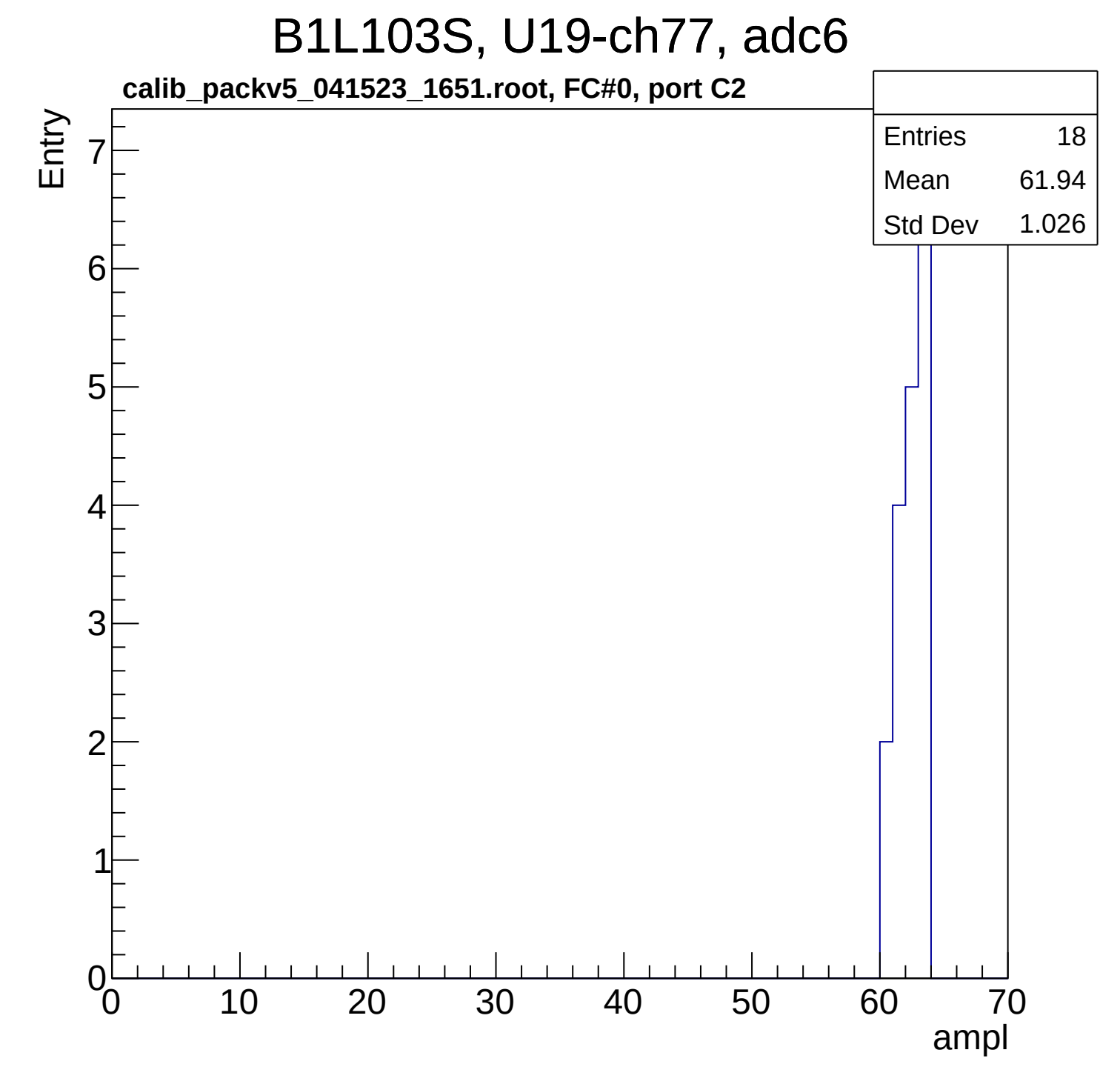
B1L103S, U19-ch77, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 61.94
Std Dev 1.026
Entry
ampl
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2
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4
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6
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0
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40
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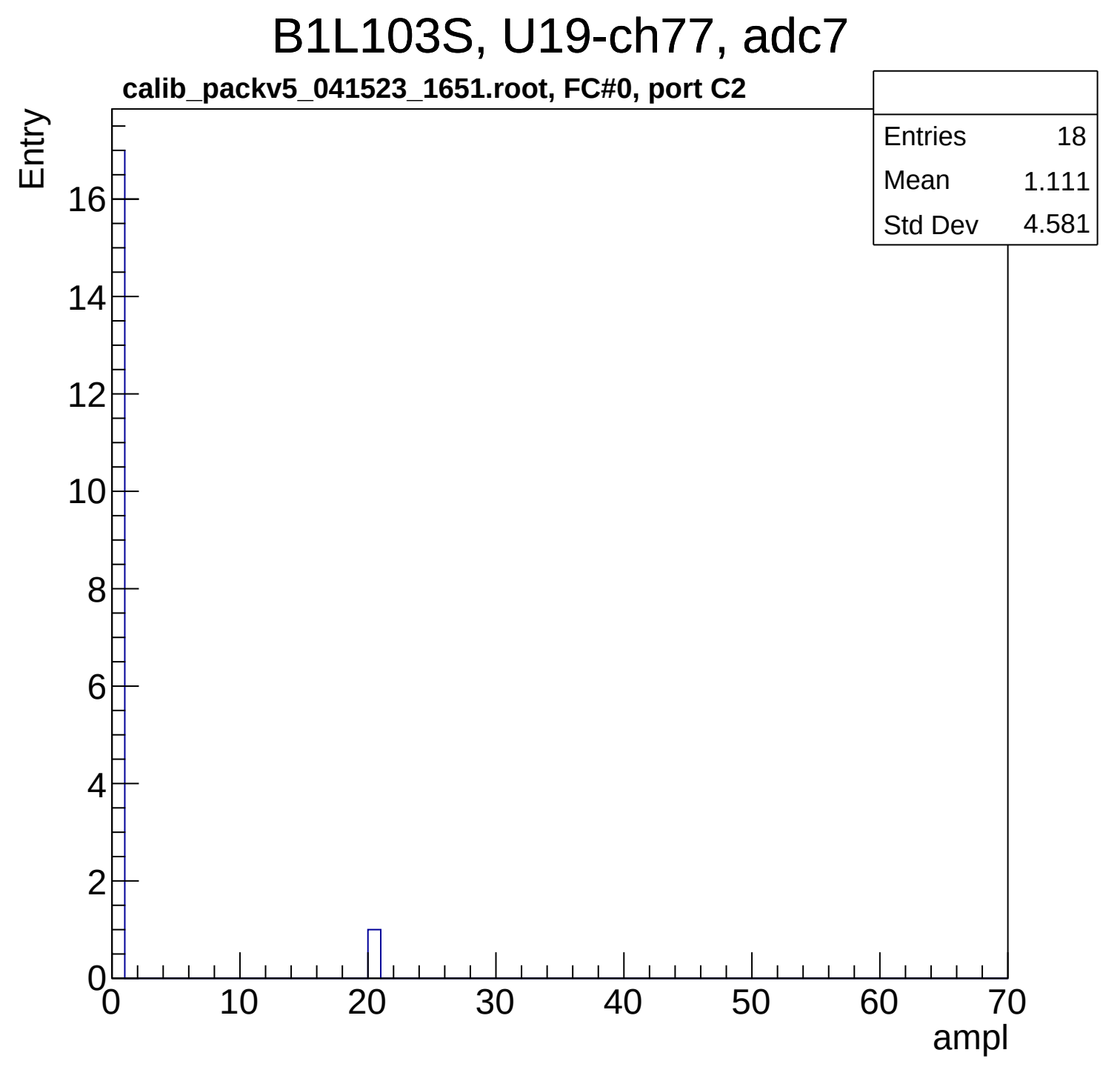
B1L103S, U19-ch77, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.111
Std Dev 4.581
Entry
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16
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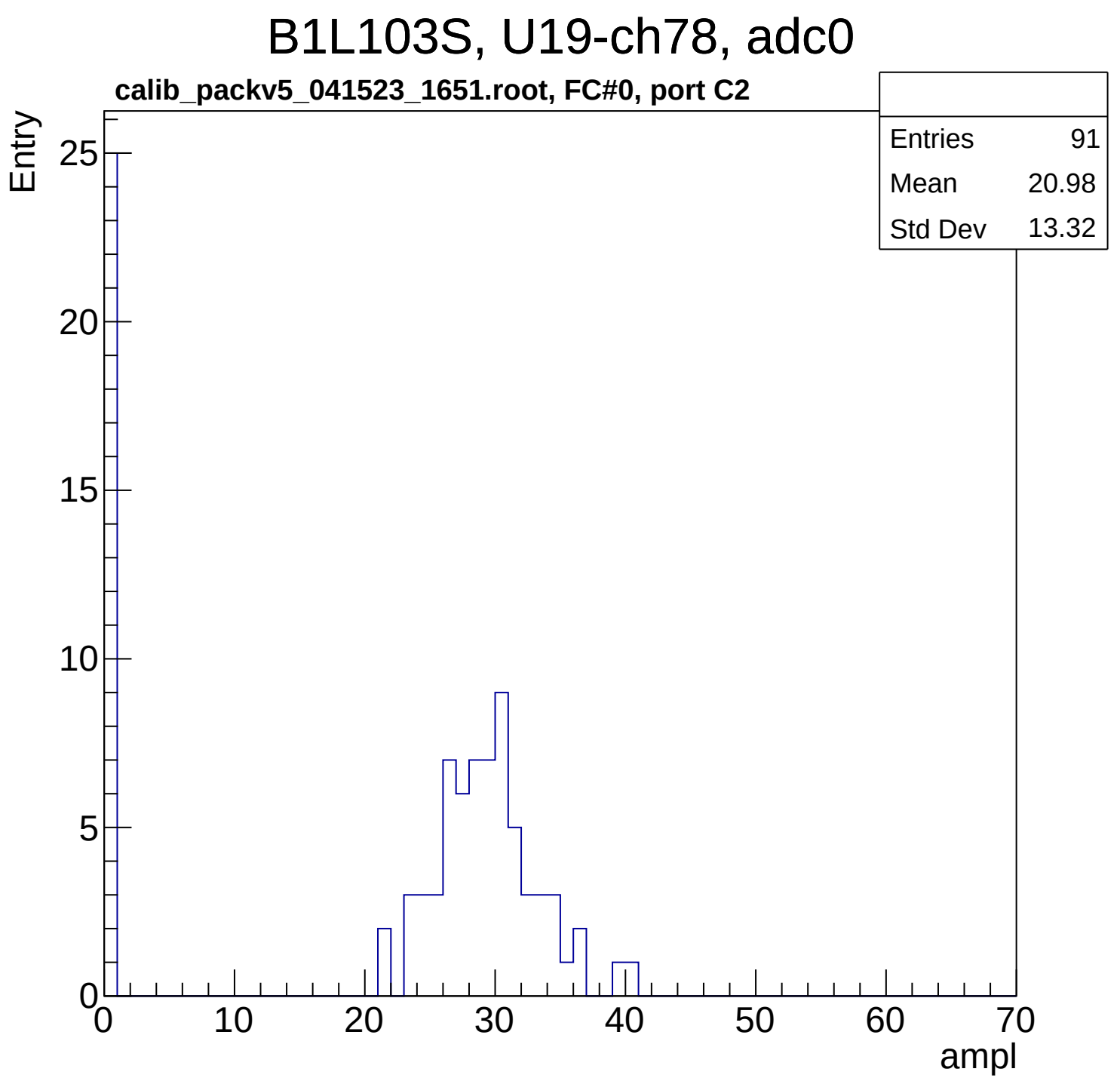
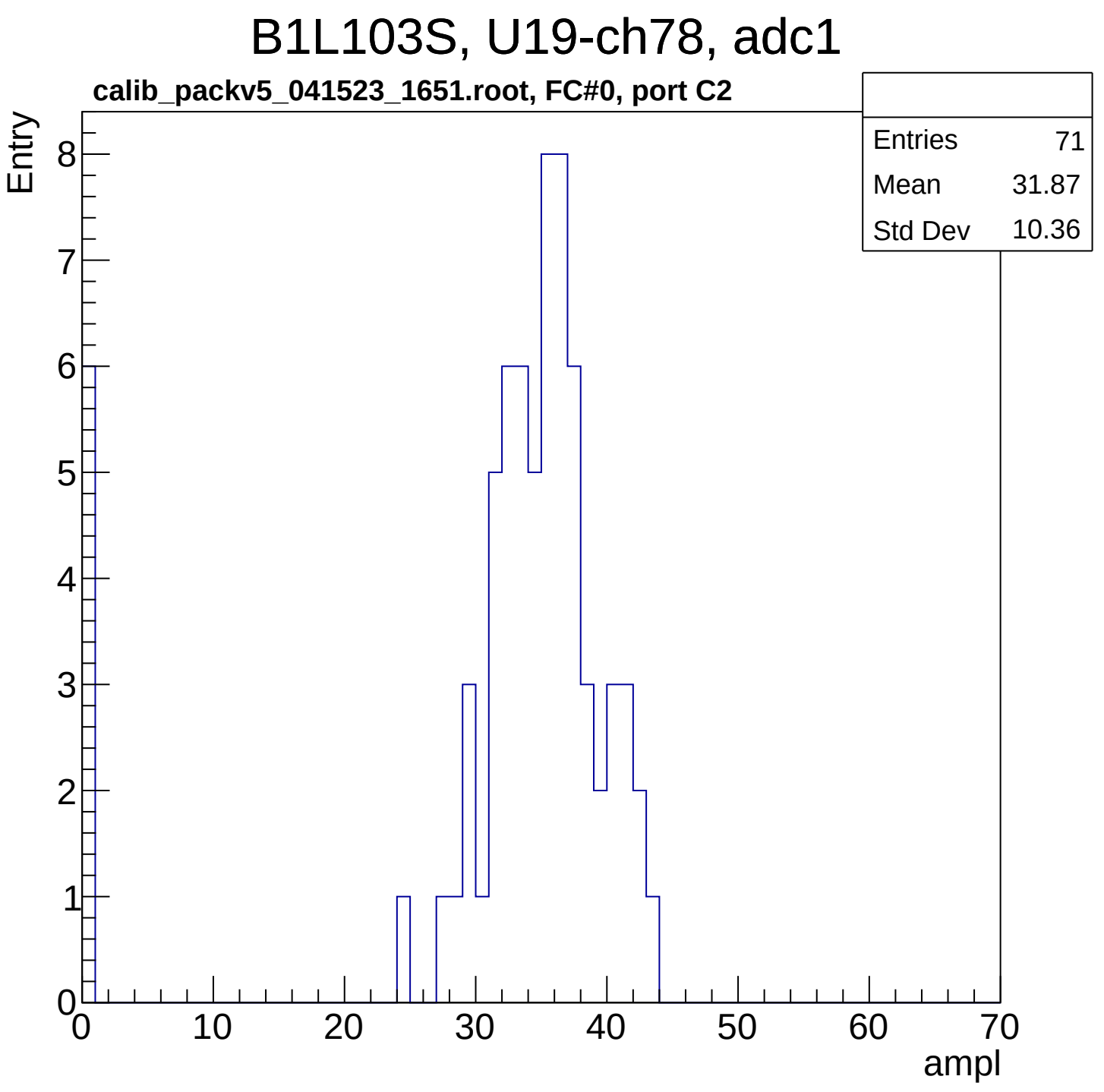
70
ampl


B1L103S, U19-ch78, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 20.98
Std Dev 13.32
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch78, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 31.87
Std Dev 10.36
Entry
ampl
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4
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7
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0
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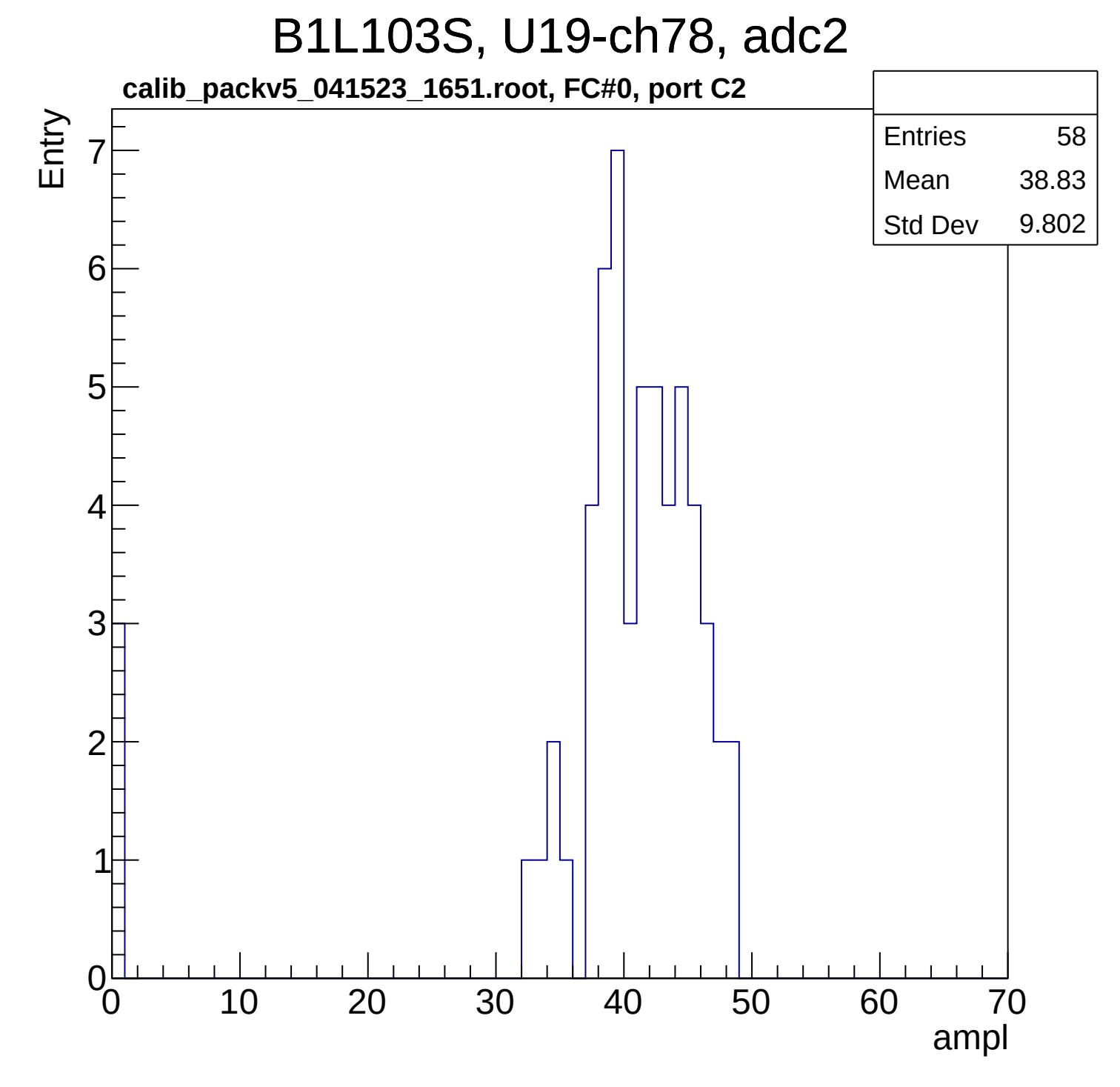
B1L103S, U19-ch78, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 38.83
Std Dev 9.802
Entry
ampl
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2
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0
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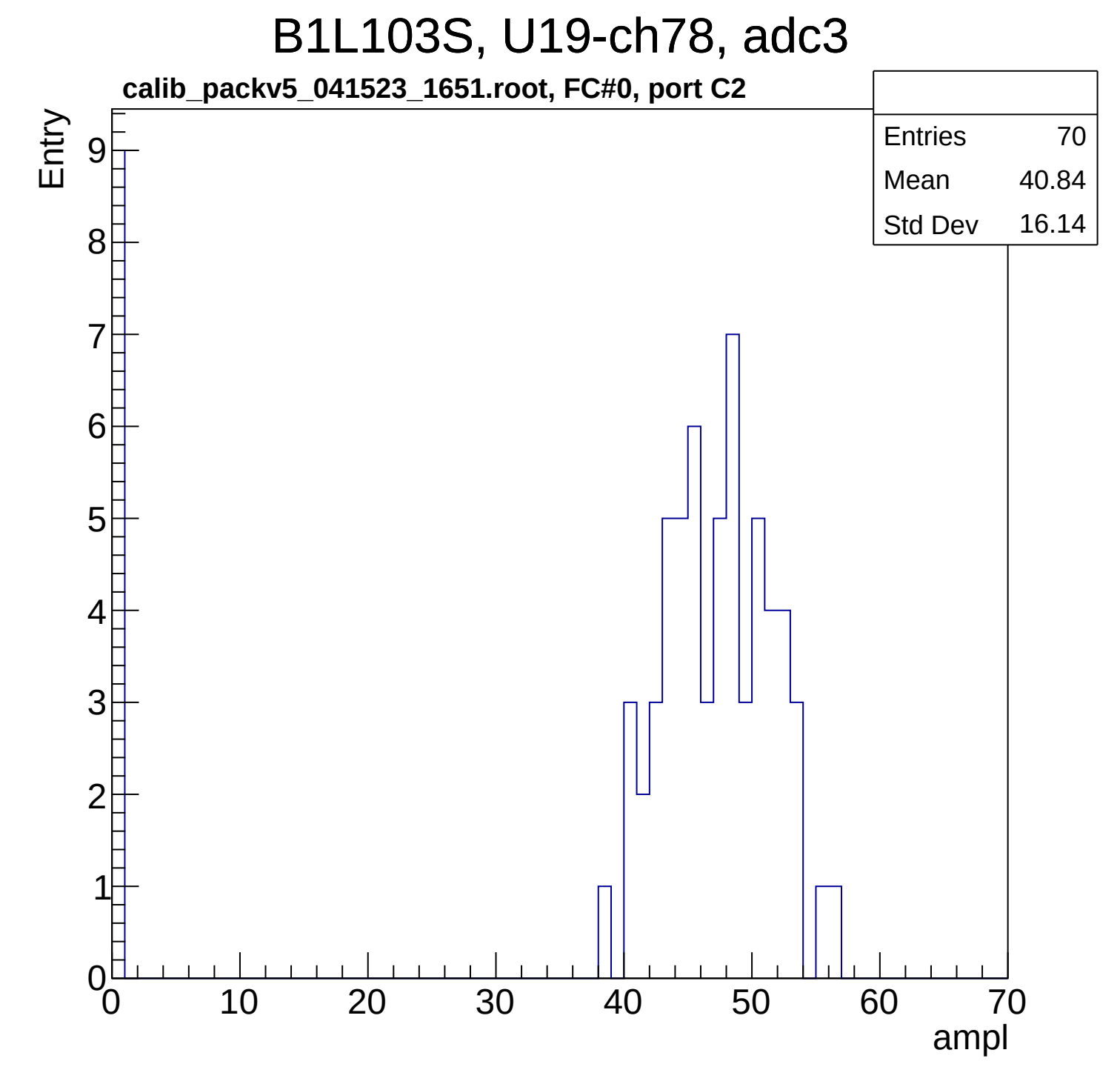
B1L103S, U19-ch78, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 40.84
Std Dev 16.14
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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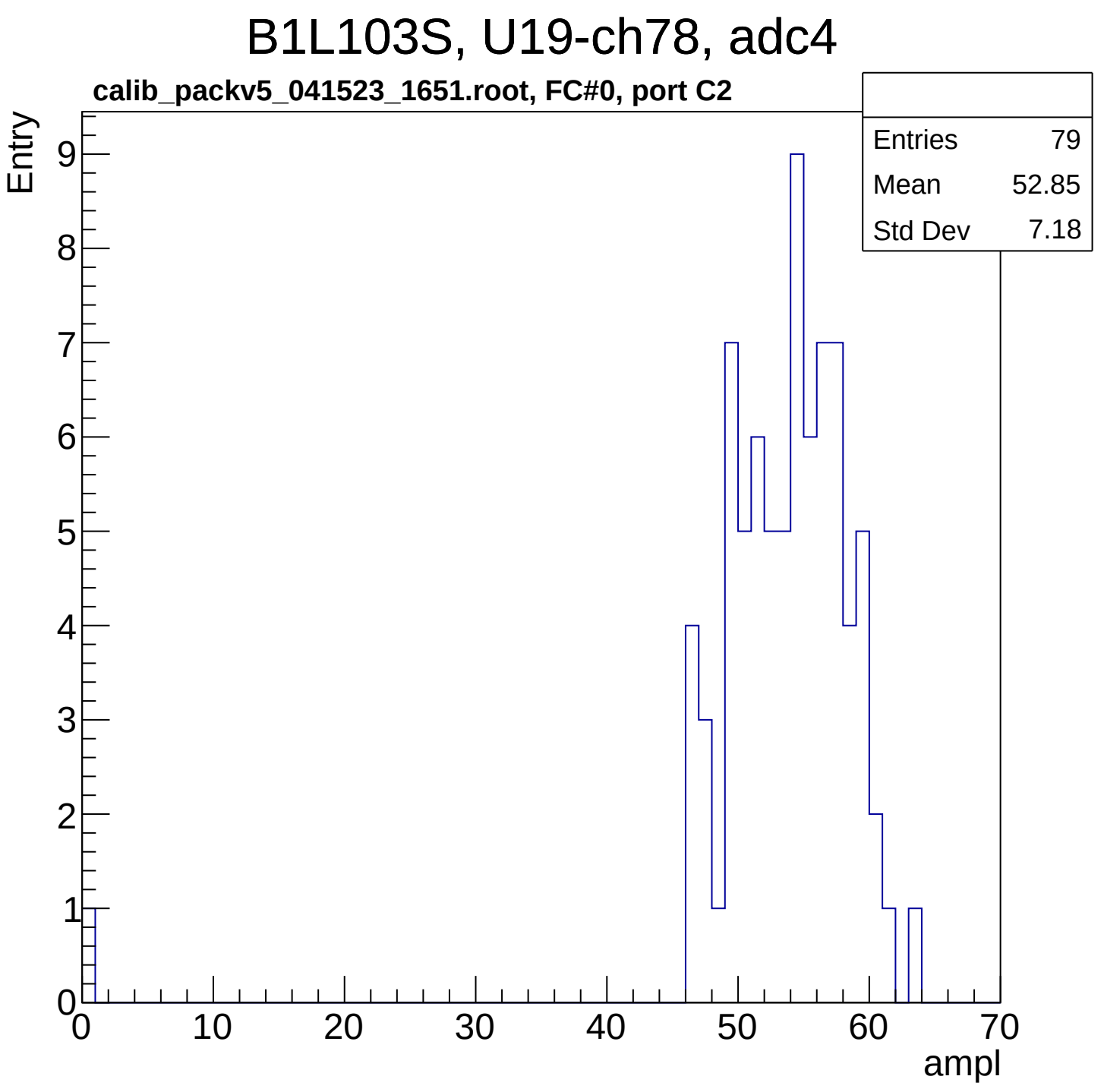
B1L103S, U19-ch78, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 52.85
Std Dev 7.18
Entry
ampl
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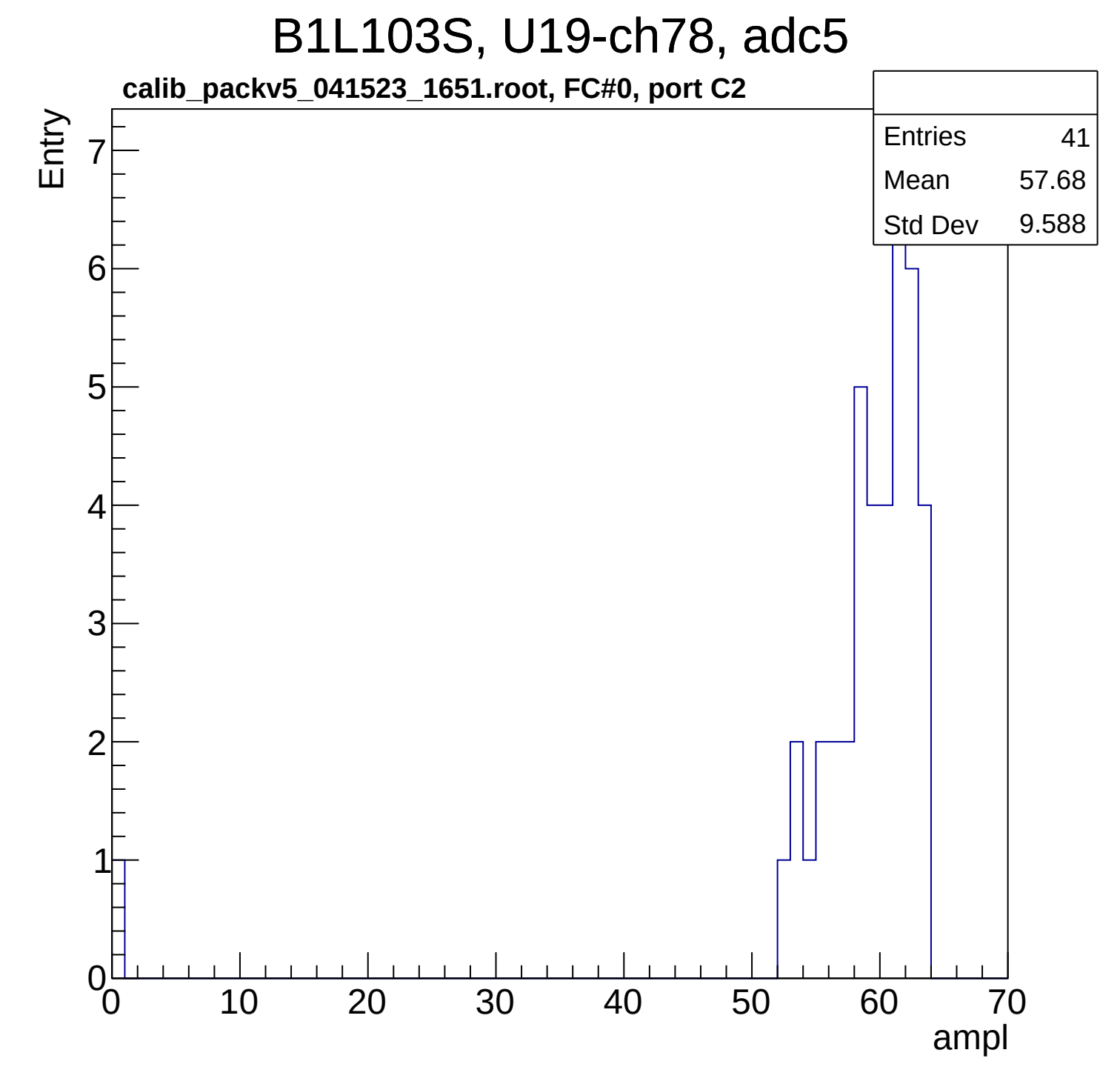
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch78, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 57.68
Std Dev 9.588
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
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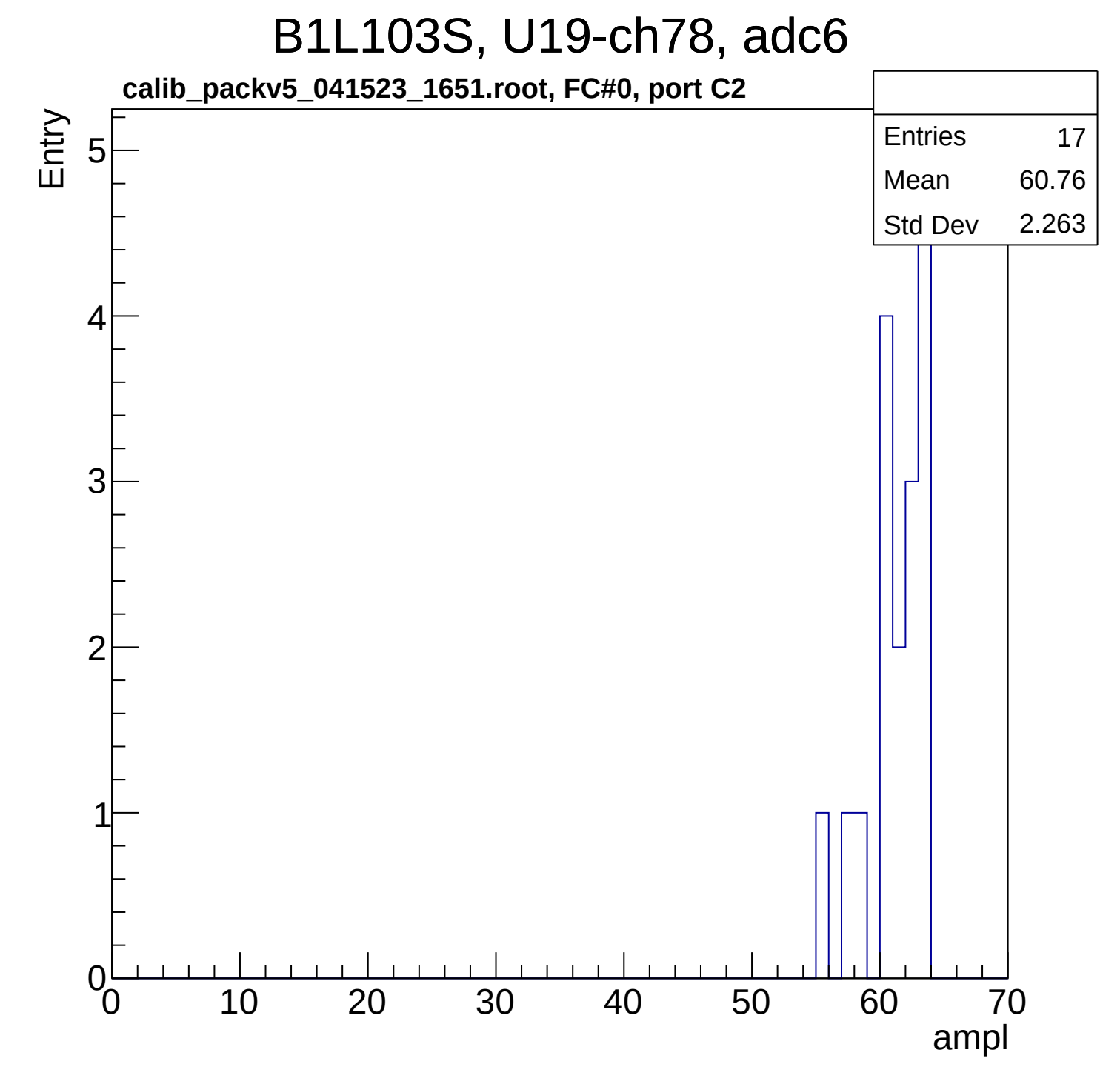
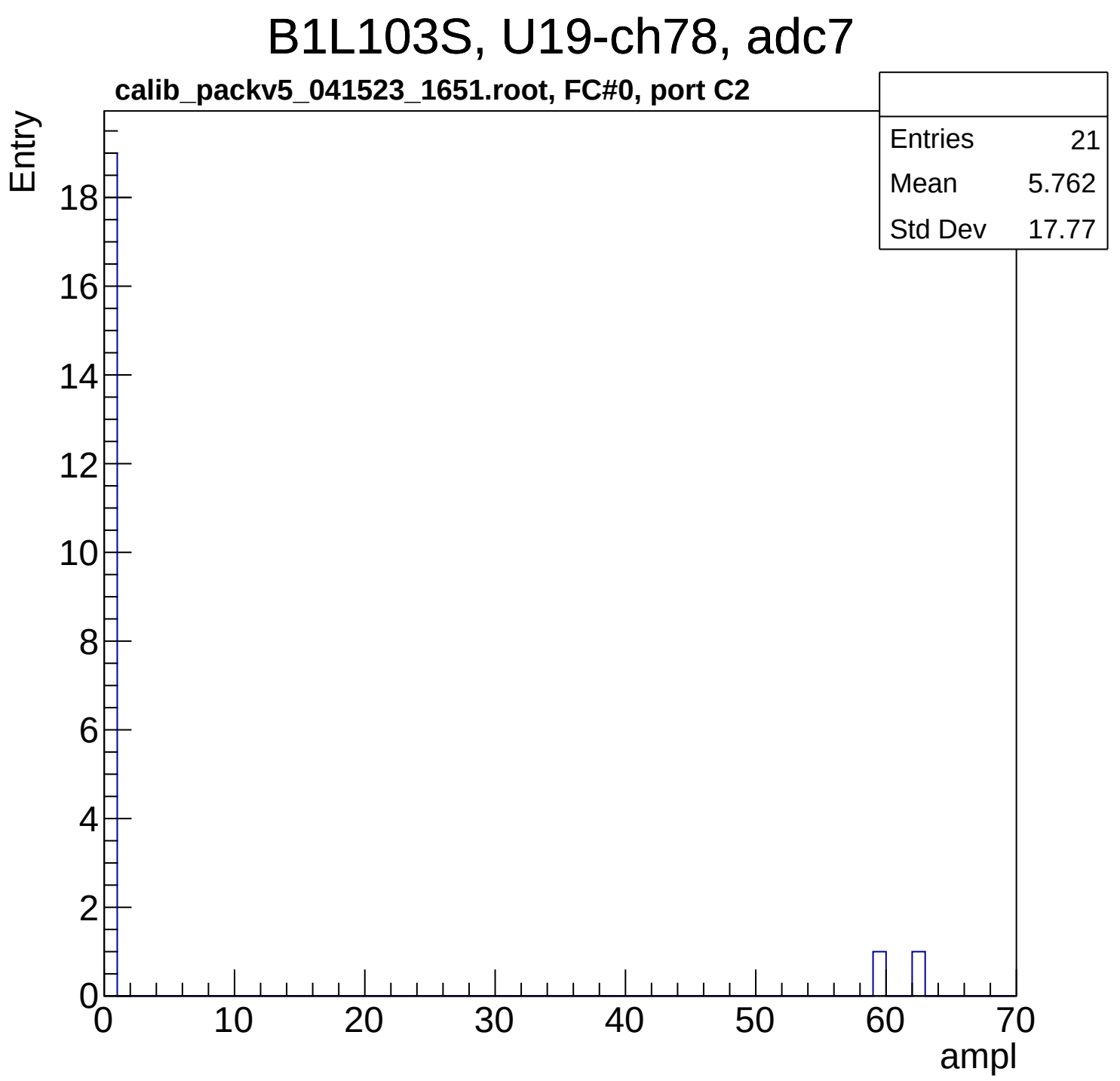
60
70


B1L103S, U19-ch78, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 60.76
Std Dev 2.263
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U19-ch78, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.762
Std Dev 17.77
Entry
0
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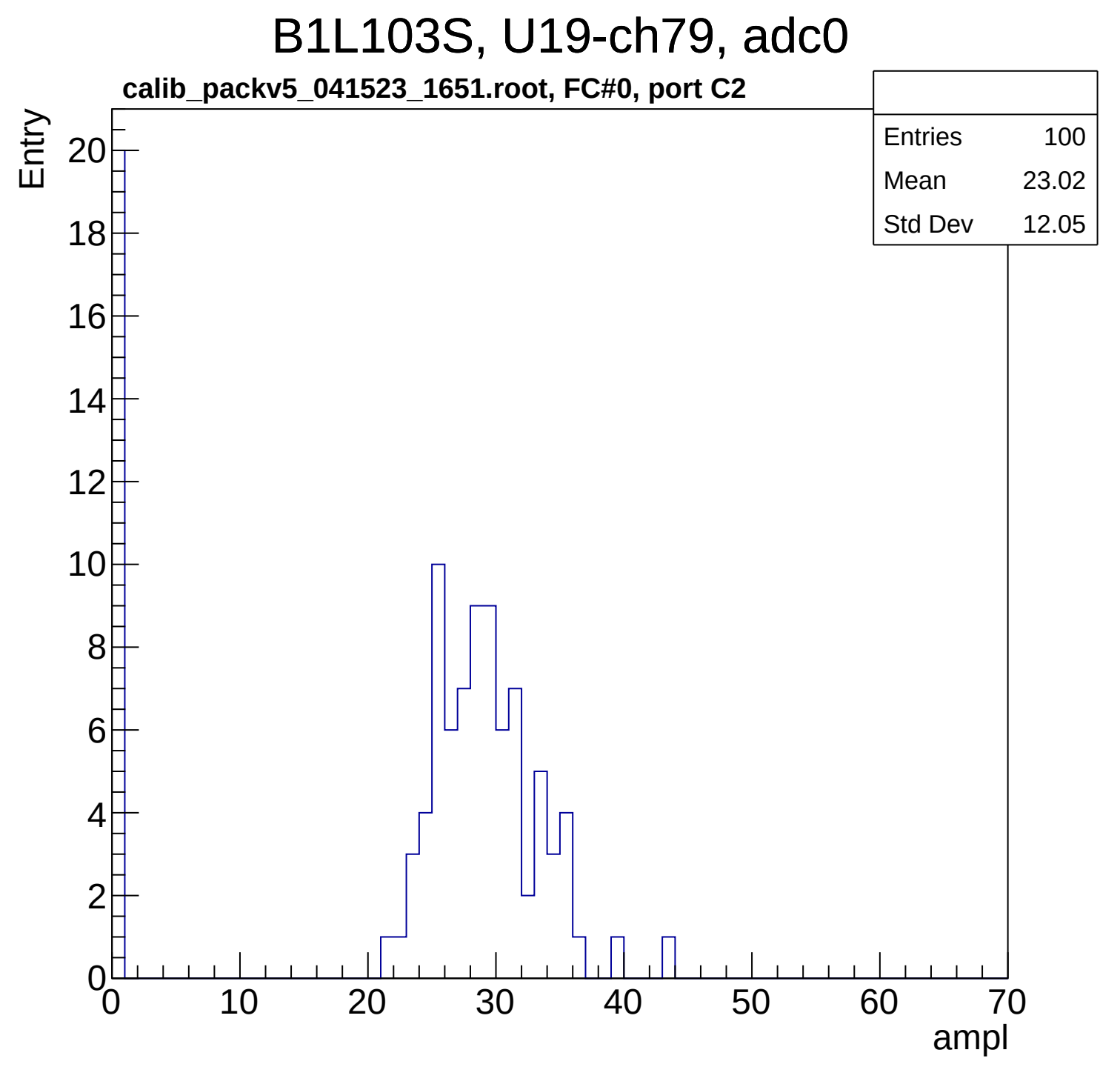
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch79, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 100
Mean 23.02
Std Dev 12.05
Entry
ampl
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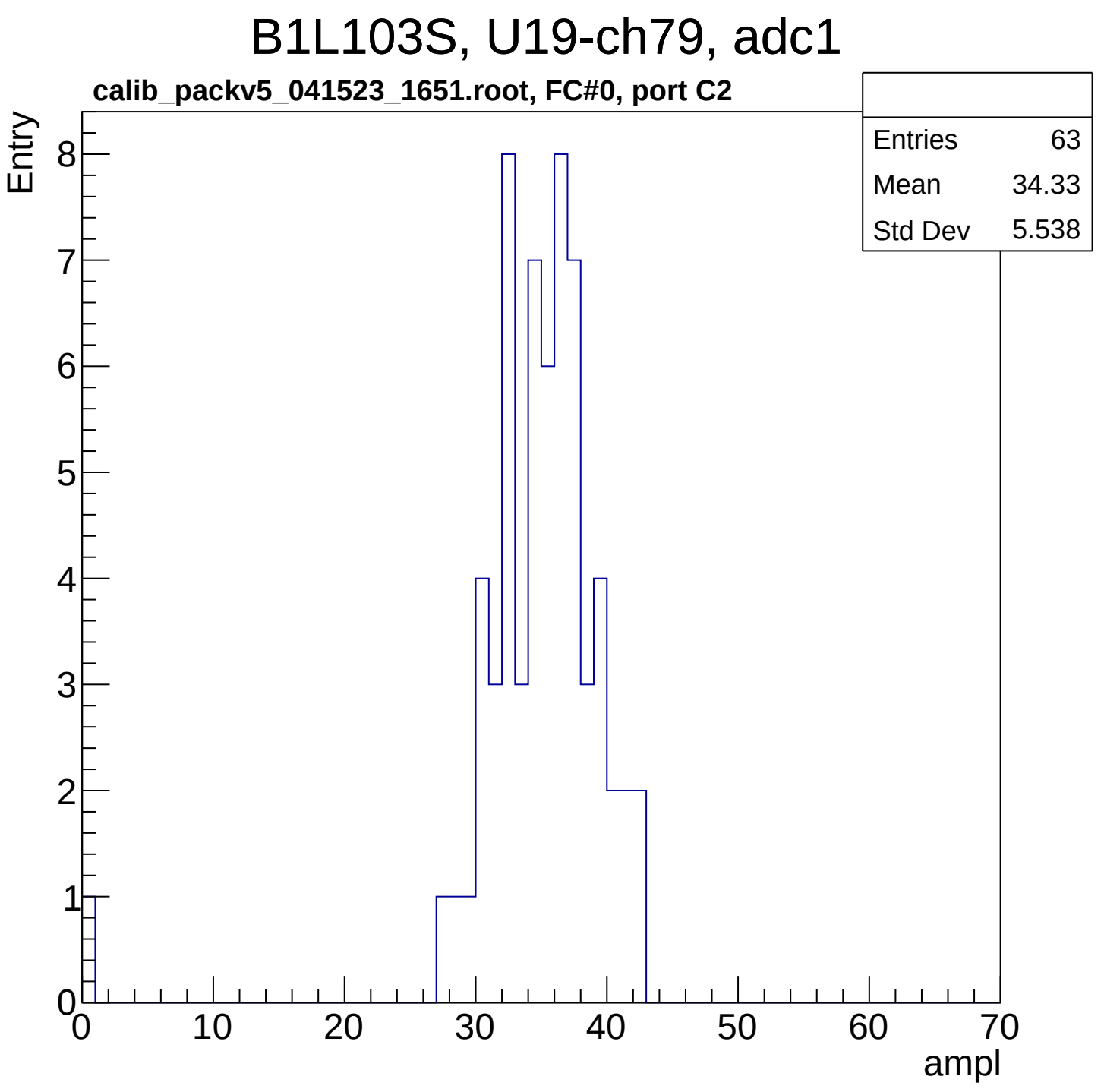
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70


B1L103S, U19-ch79, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 34.33
Std Dev 5.538
Entry
ampl
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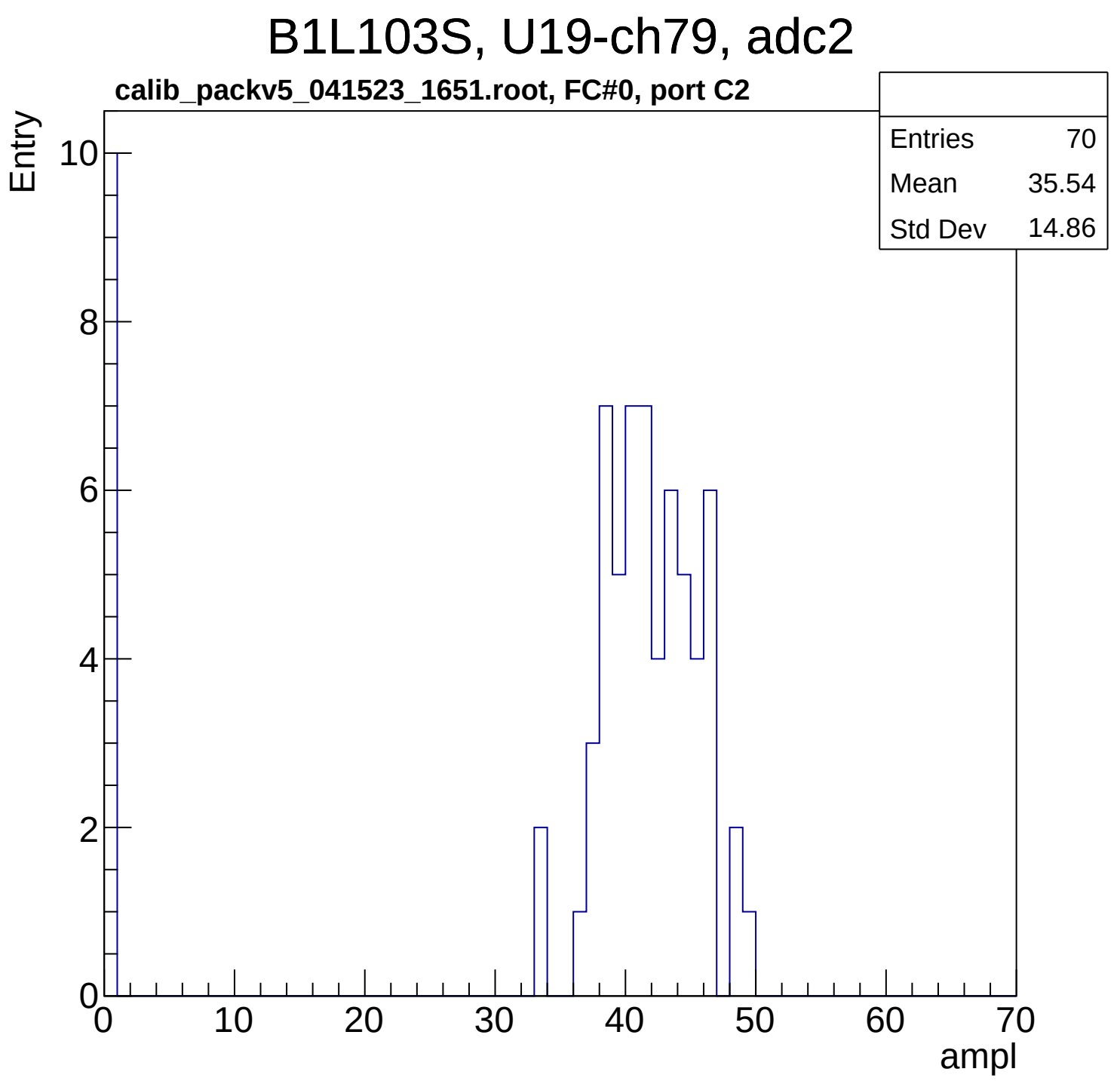
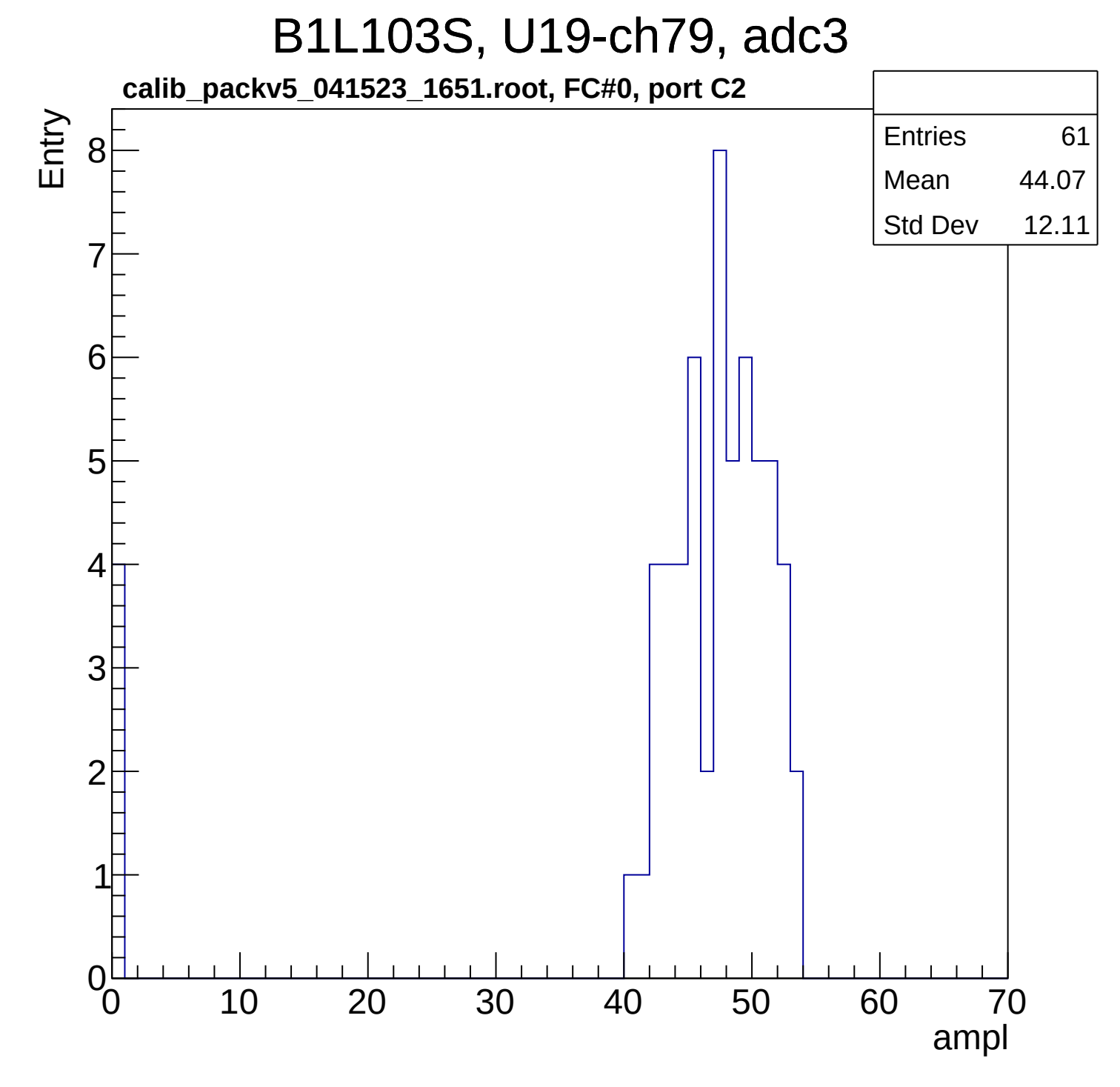
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch79, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 35.54
Std Dev 14.86
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch79, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 44.07
Std Dev 12.11
Entry
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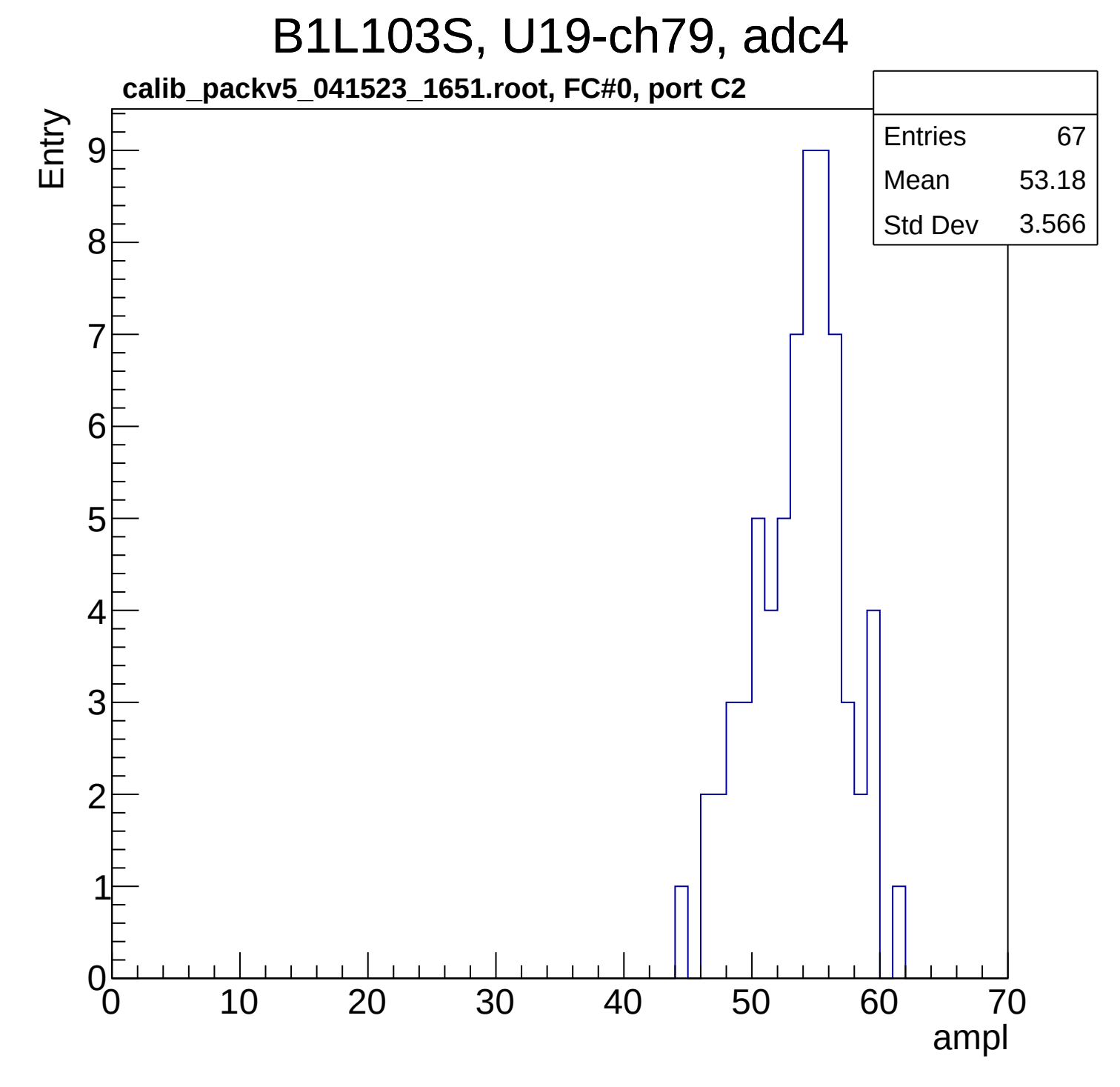
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch79, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 53.18
Std Dev 3.566
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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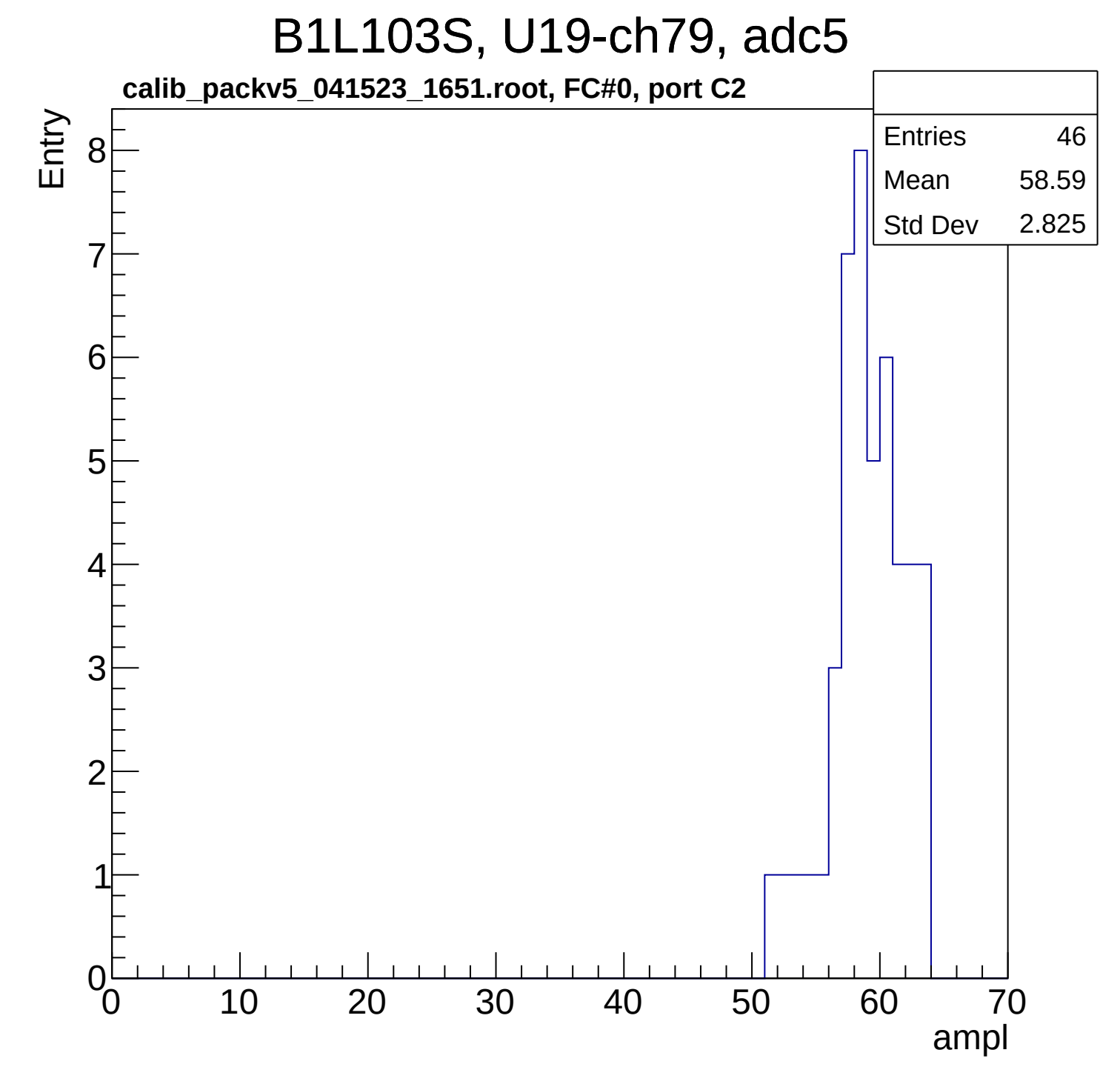
40
50
60
70


B1L103S, U19-ch79, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 58.59
Std Dev 2.825
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
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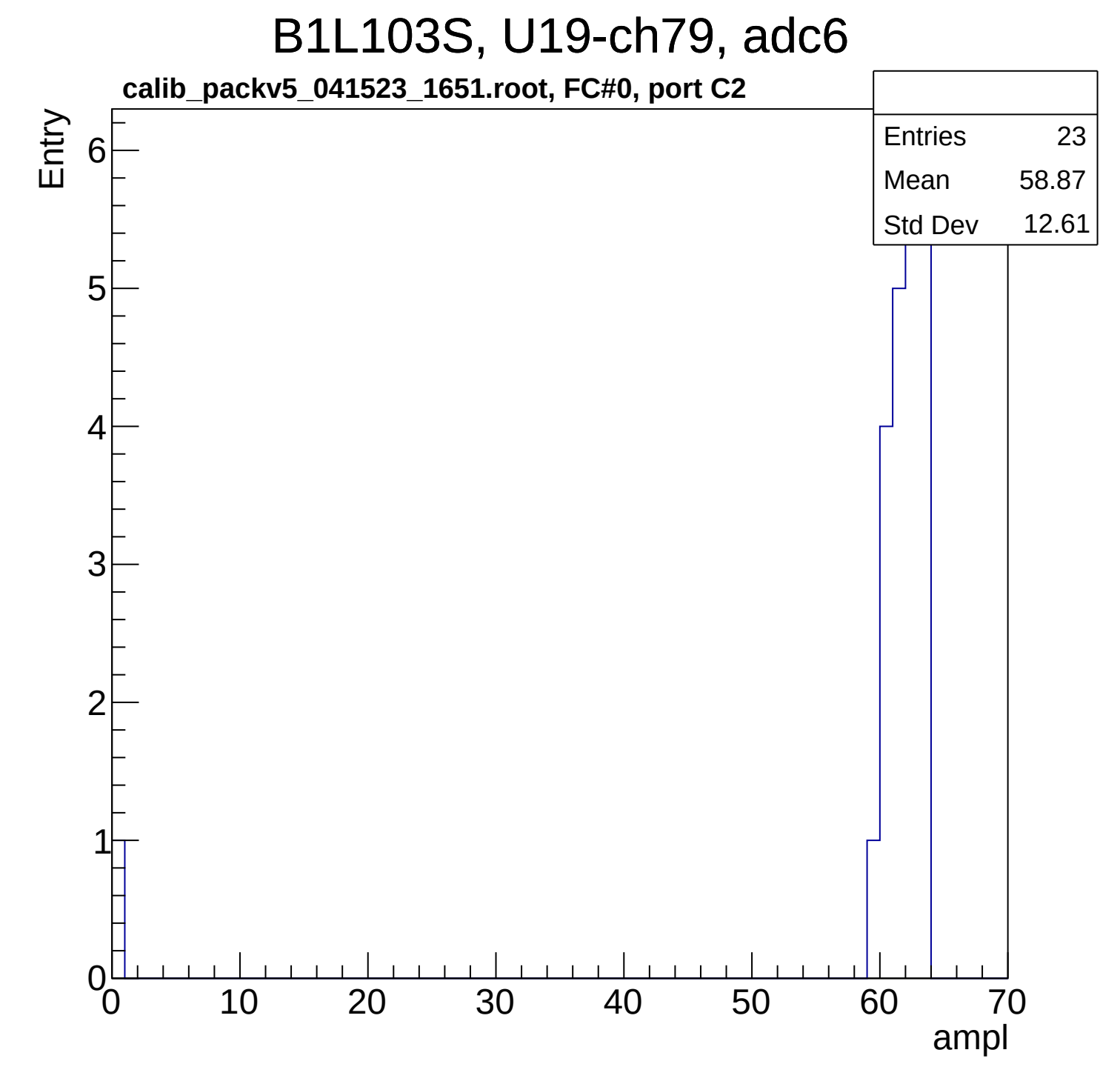
60
70


B1L103S, U19-ch79, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 58.87
Std Dev 12.61
Entry
ampl
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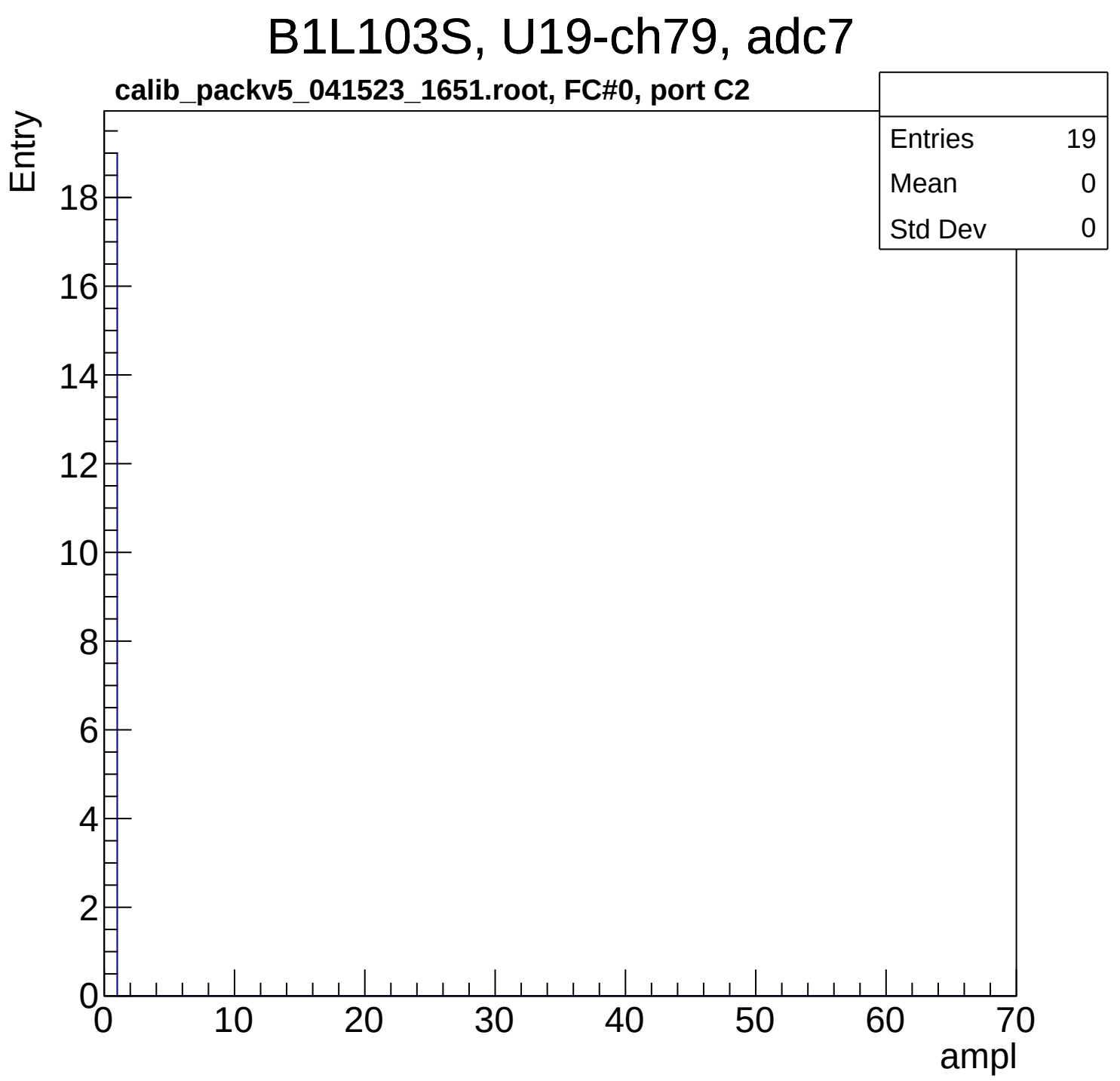
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U19-ch79, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
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6
8
10
12
14
16
18
0
10
20
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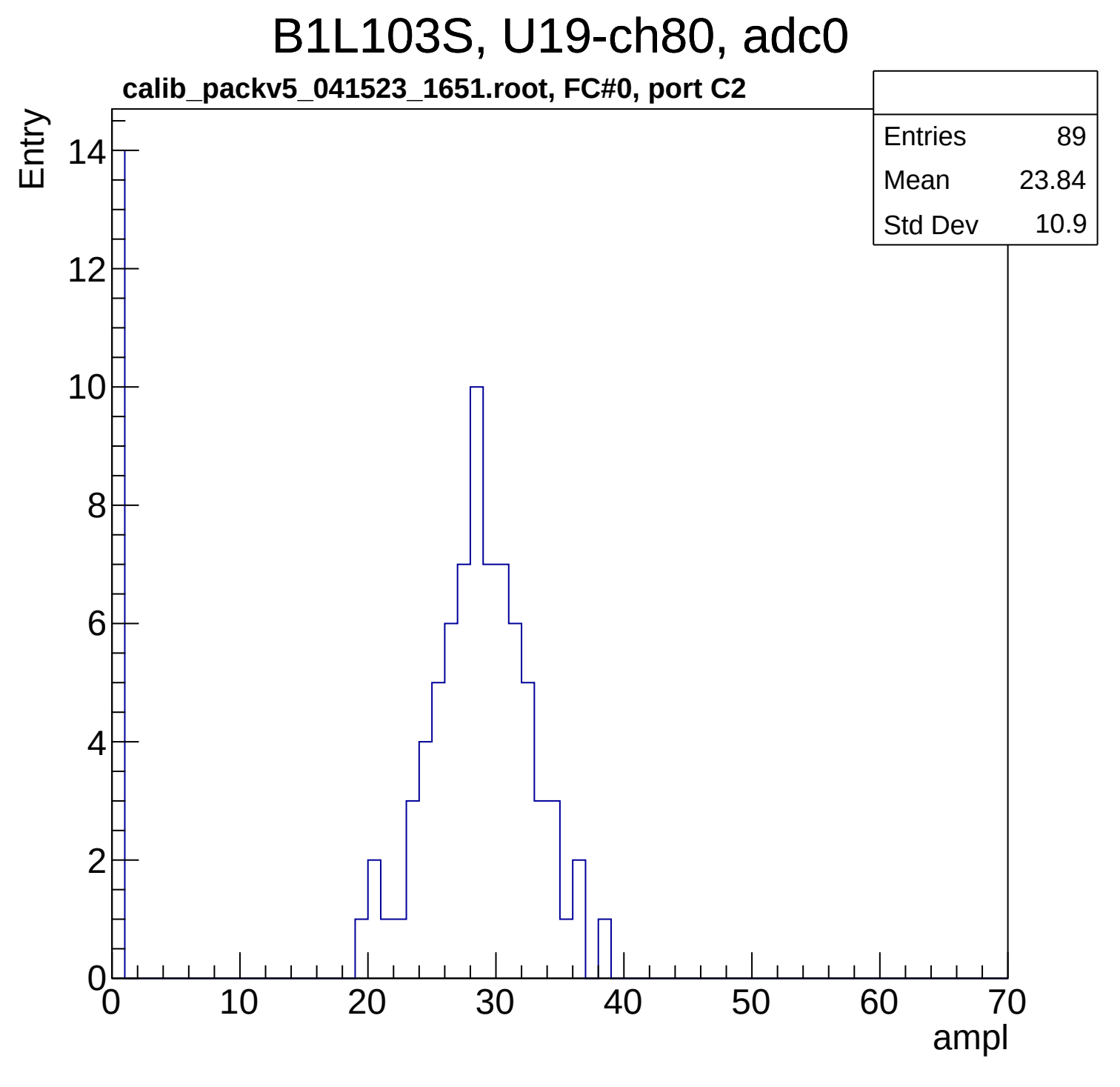
60
70
ampl


B1L103S, U19-ch80, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 23.84
Std Dev 10.9
Entry
ampl
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8
10
12
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0
10
20
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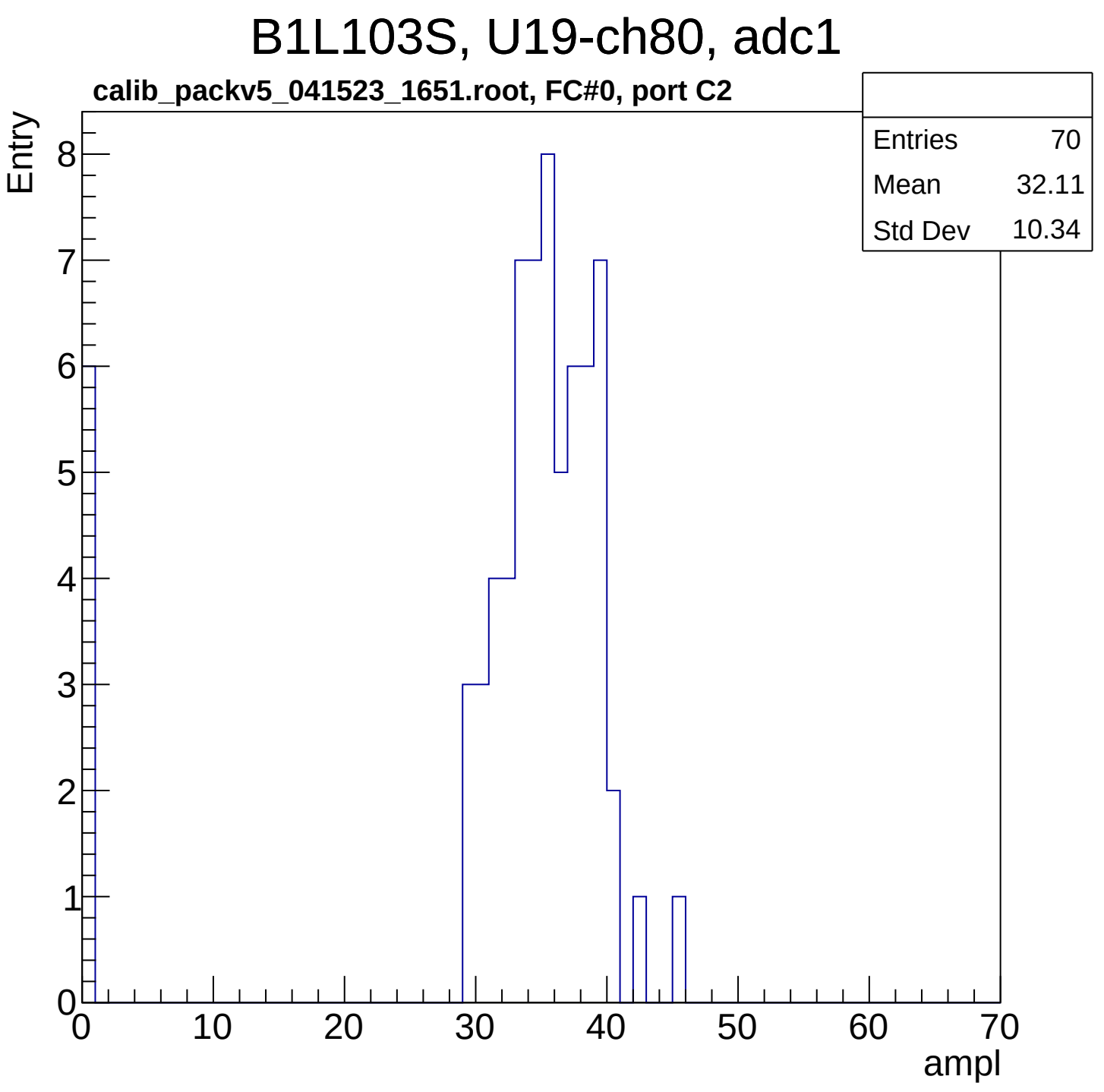
B1L103S, U19-ch80, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 32.11
Std Dev 10.34
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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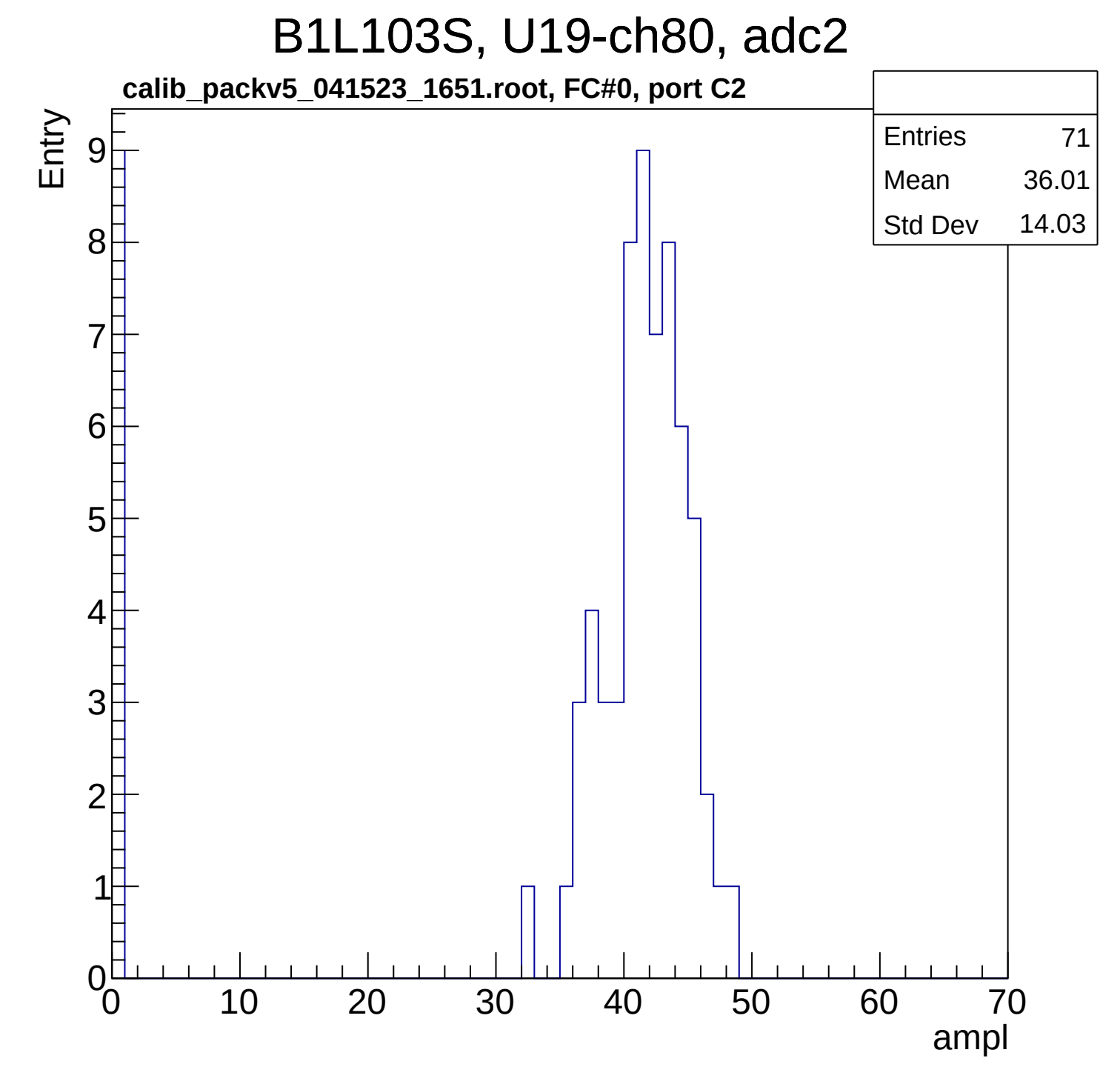
40
50
60
70


B1L103S, U19-ch80, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 36.01
Std Dev 14.03
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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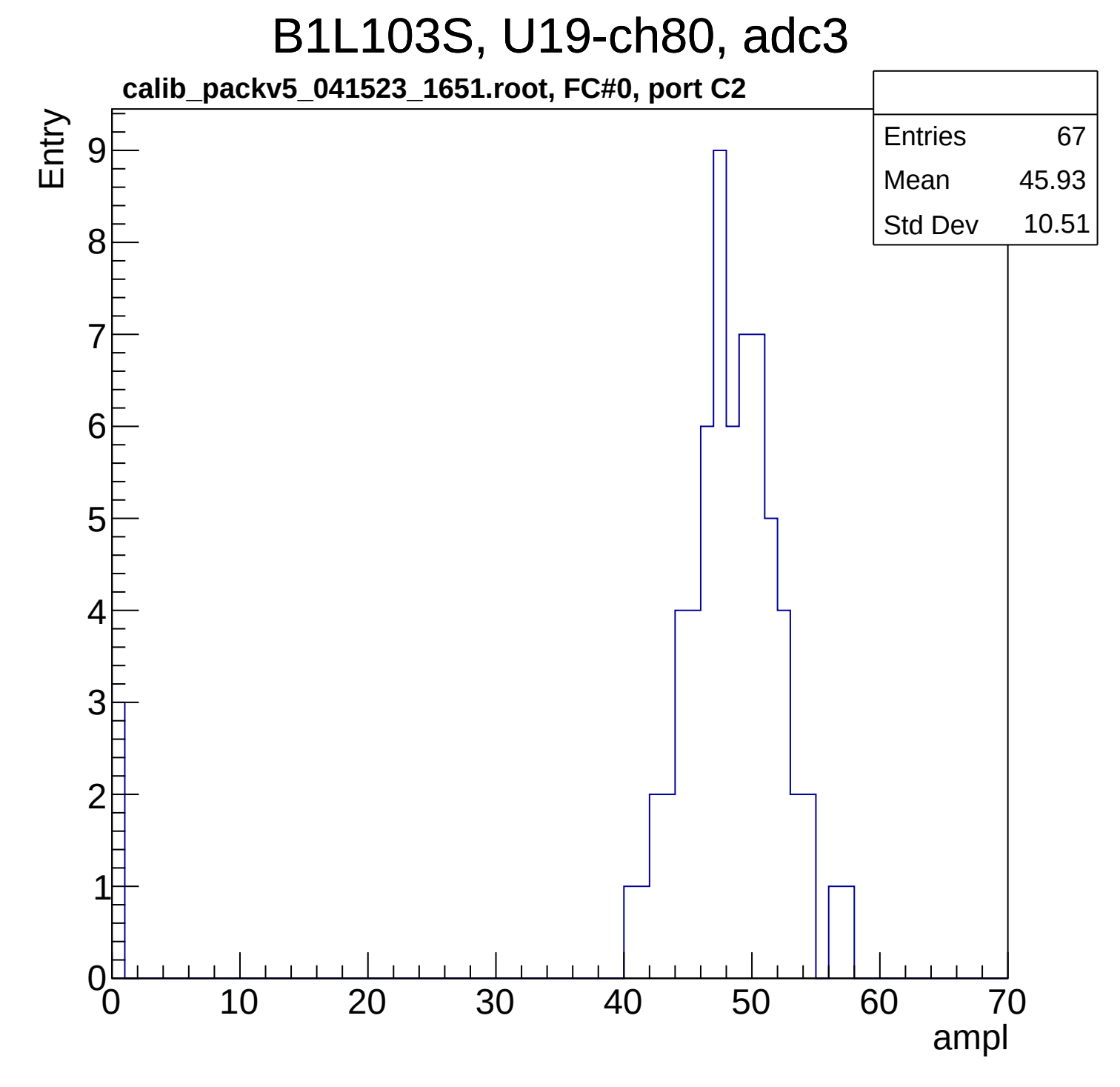
B1L103S, U19-ch80, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 45.93
Std Dev 10.51
Entry
ampl
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2
3
4
5
6
7
8
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0
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60
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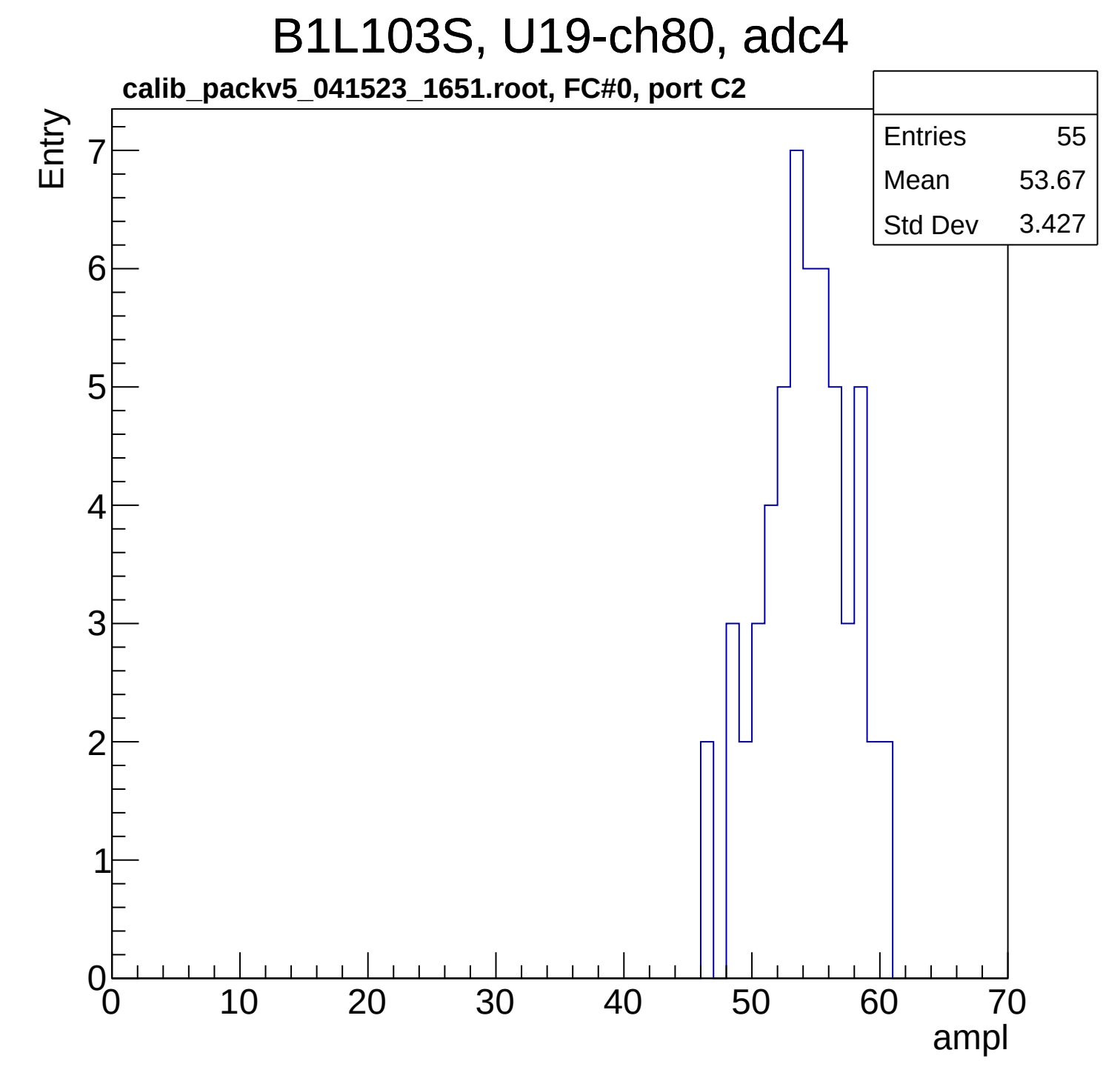
B1L103S, U19-ch80, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 53.67
Std Dev 3.427
Entry
ampl
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3
4
5
6
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0
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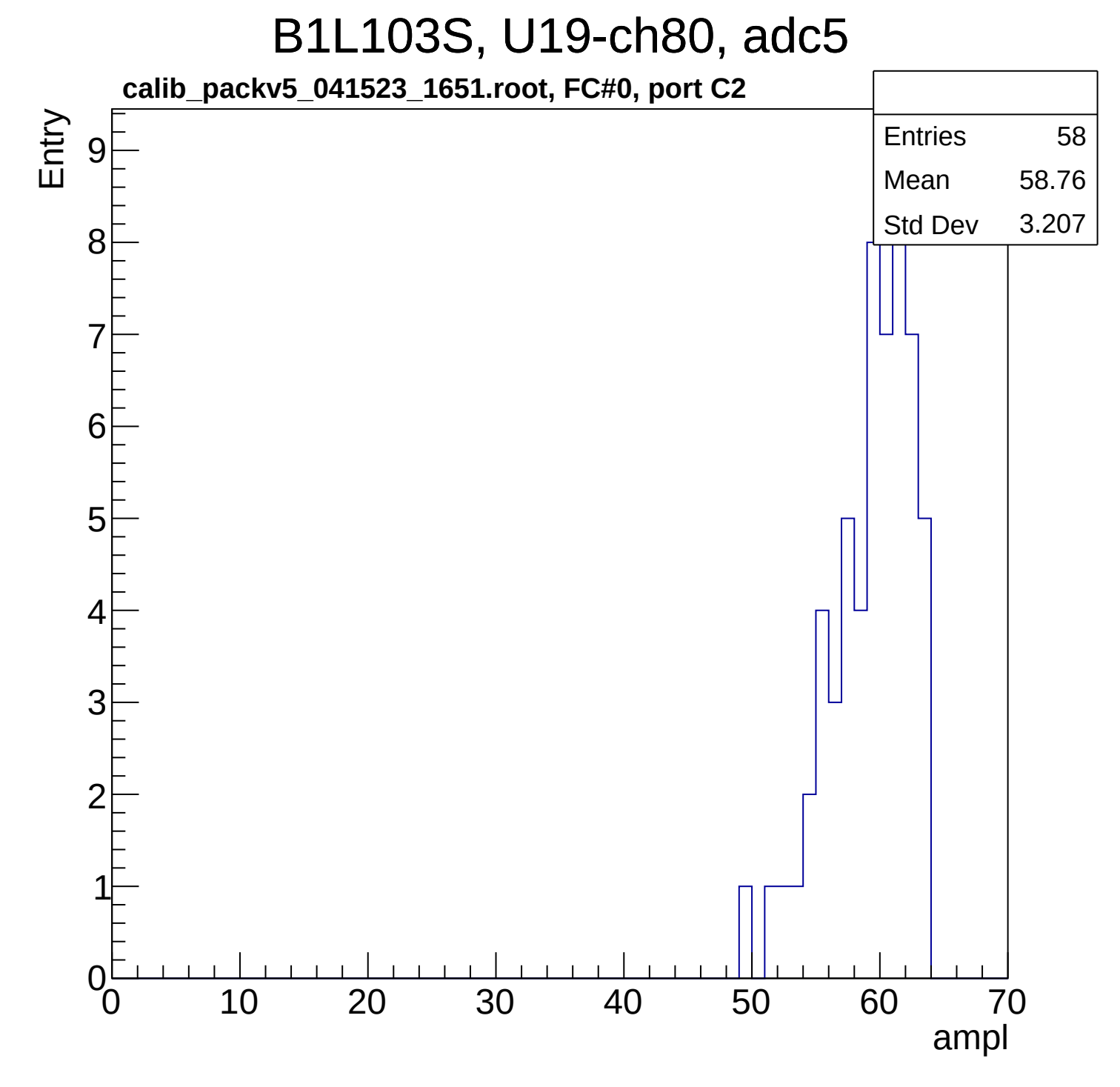
B1L103S, U19-ch80, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 58.76
Std Dev 3.207
Entry
ampl
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3
4
5
6
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8
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0
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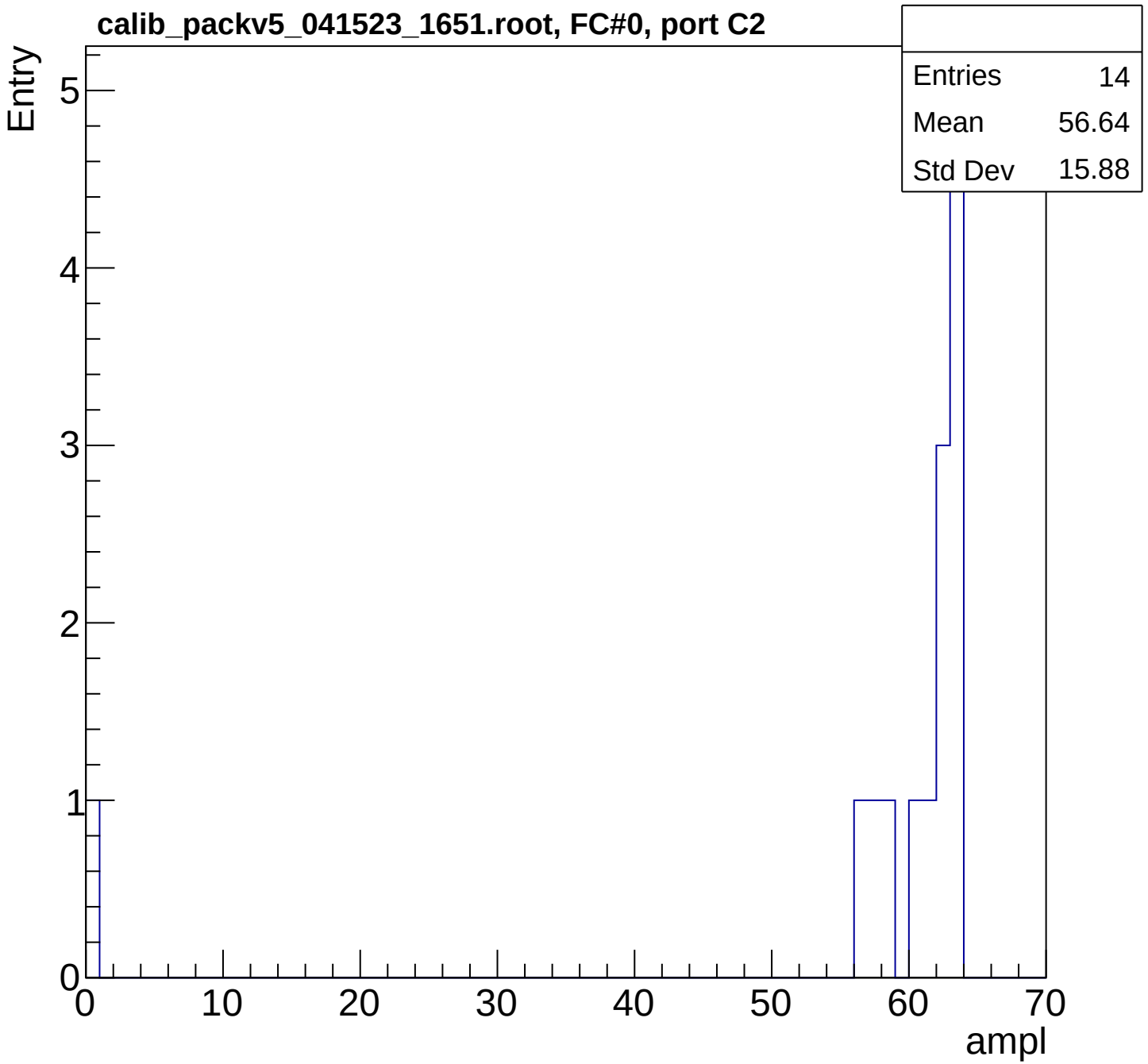
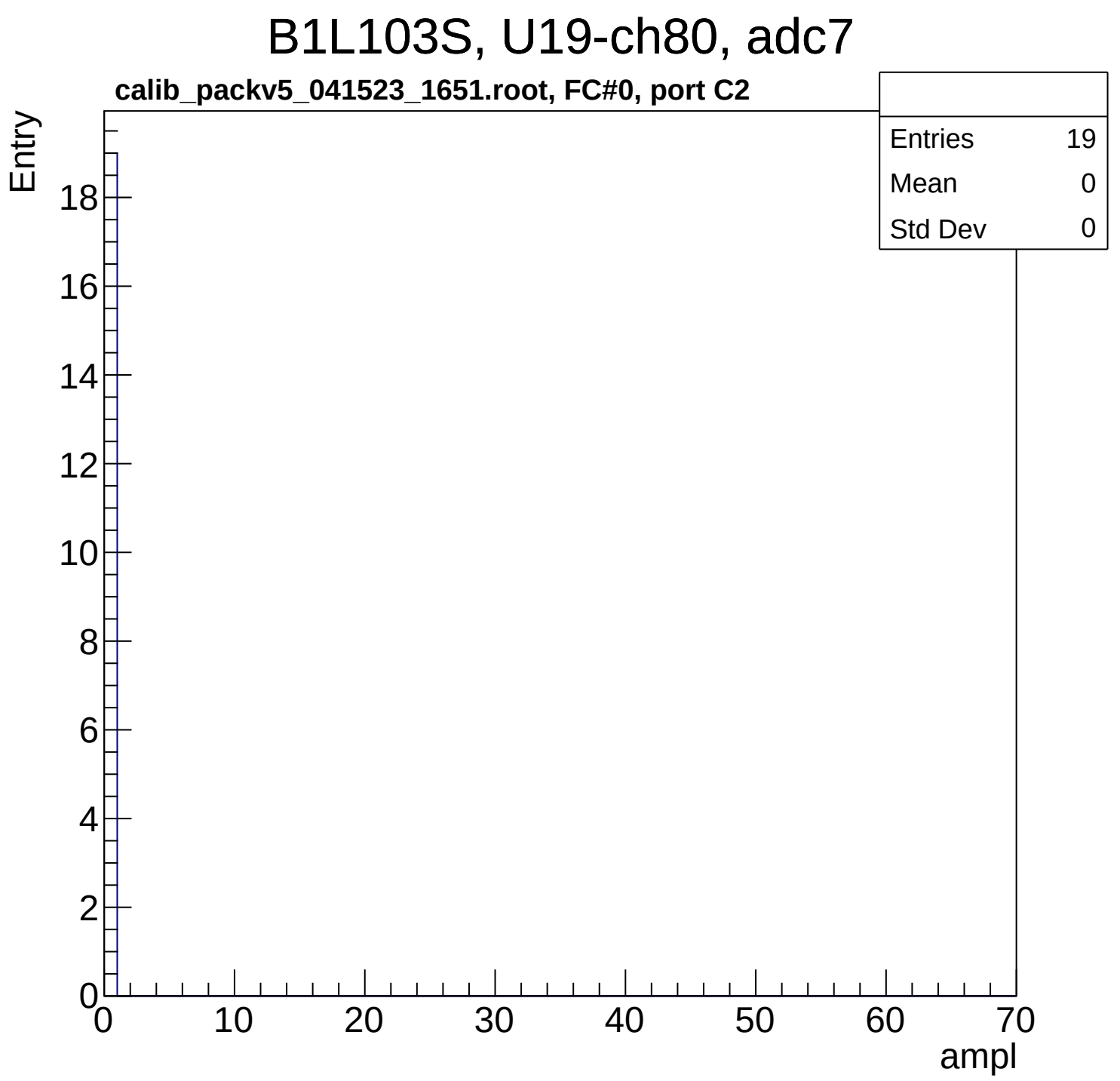
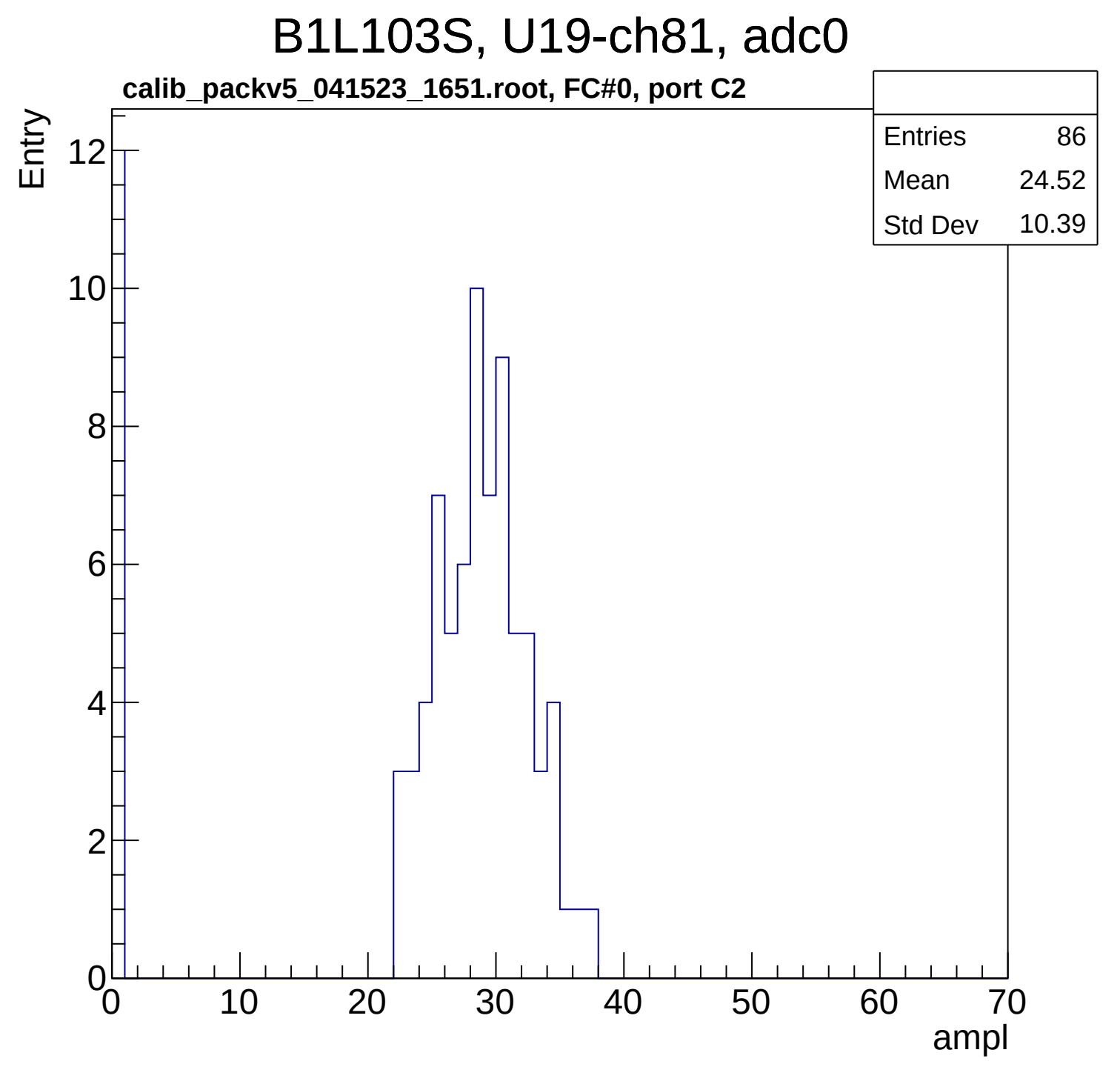

B1L103S, U19-ch80, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 56.64
Std Dev 15.88
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch80, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch81, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 24.52
Std Dev 10.39
Entry
0
2
4
6
8
10
12
0
10
20
30
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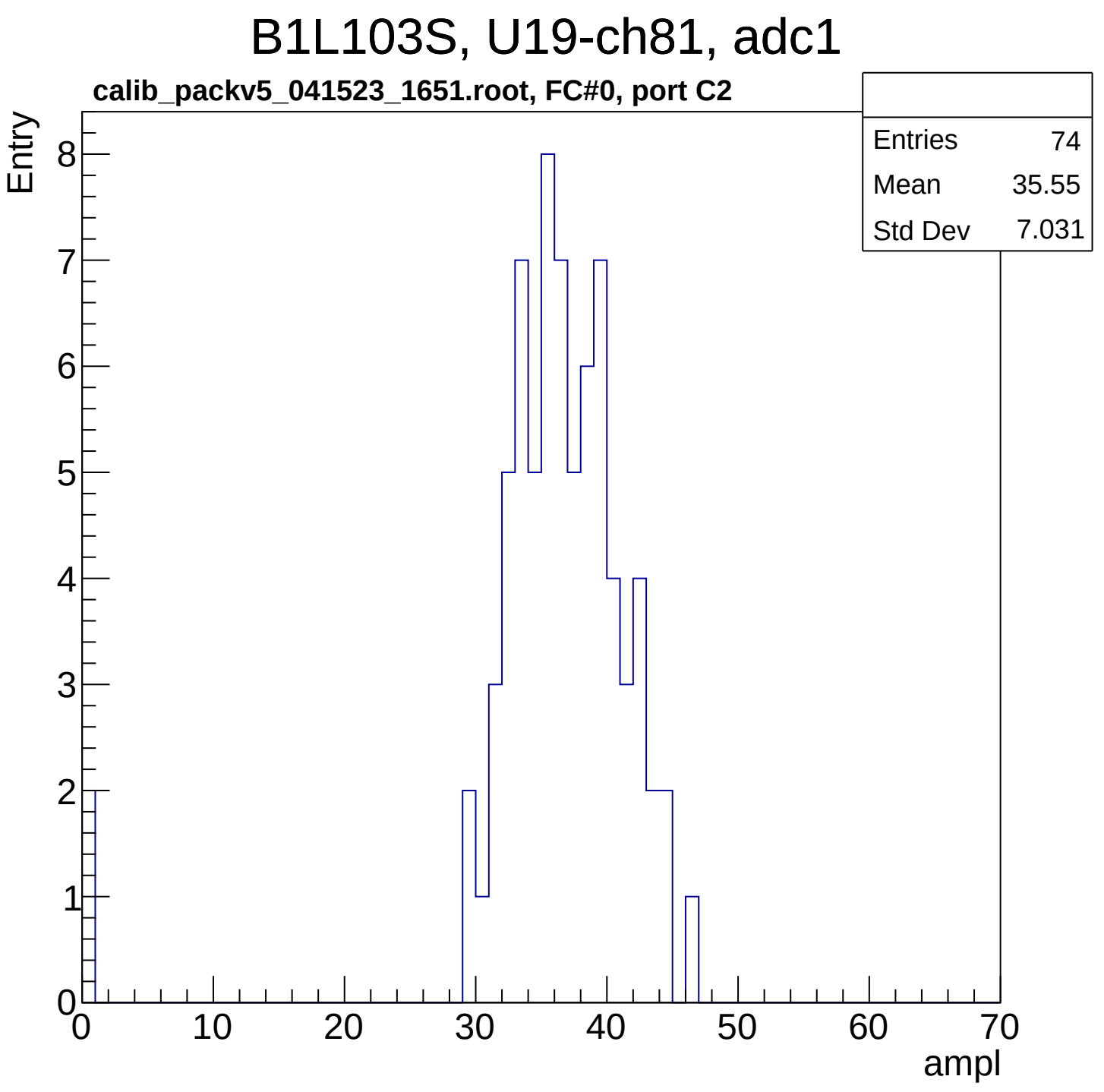
60
70
ampl


B1L103S, U19-ch81, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 35.55
Std Dev 7.031
Entry
ampl
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3
4
5
6
7
8
0
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60
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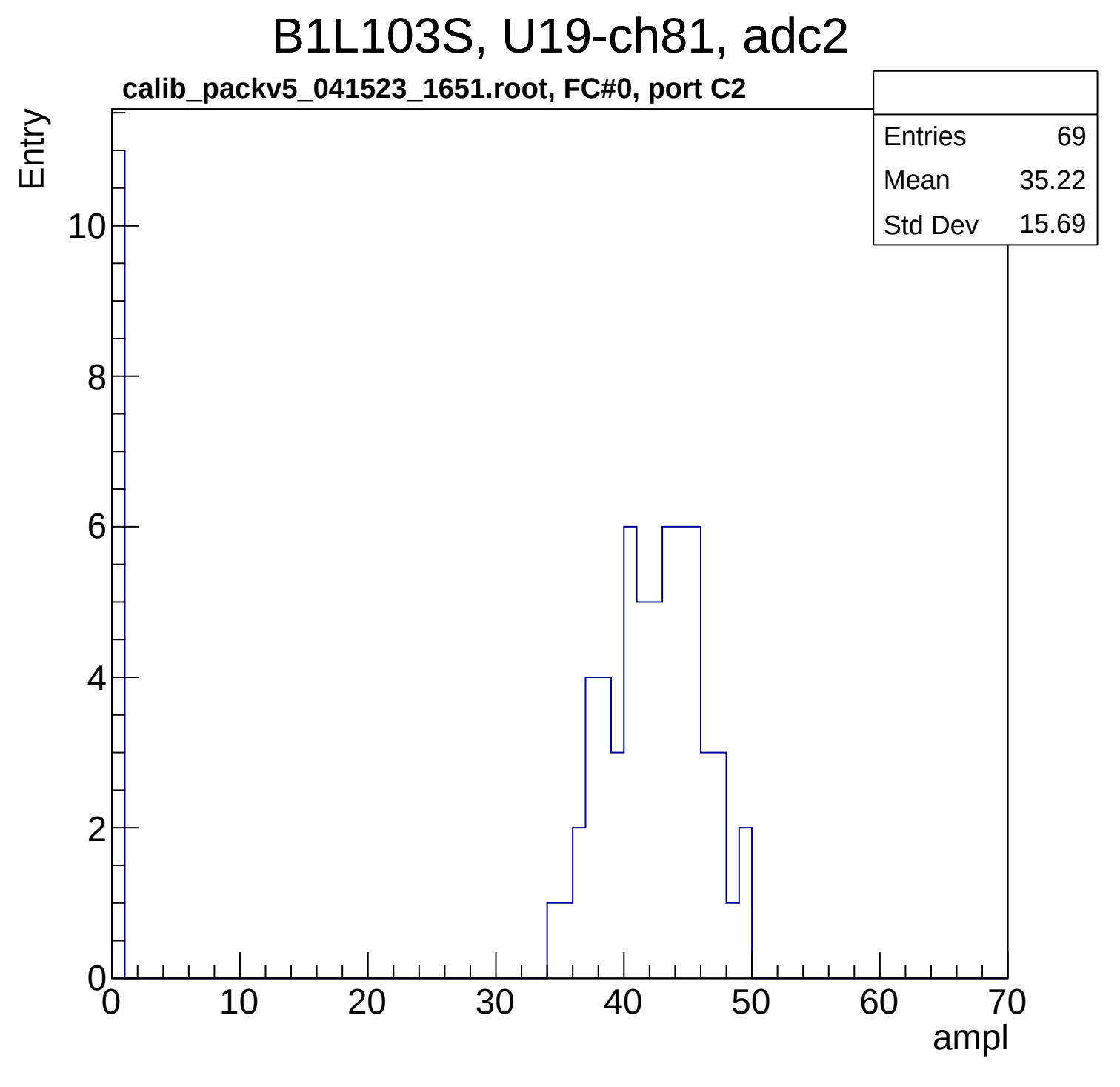
B1L103S, U19-ch81, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 35.22
Std Dev 15.69
Entry
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6
8
10
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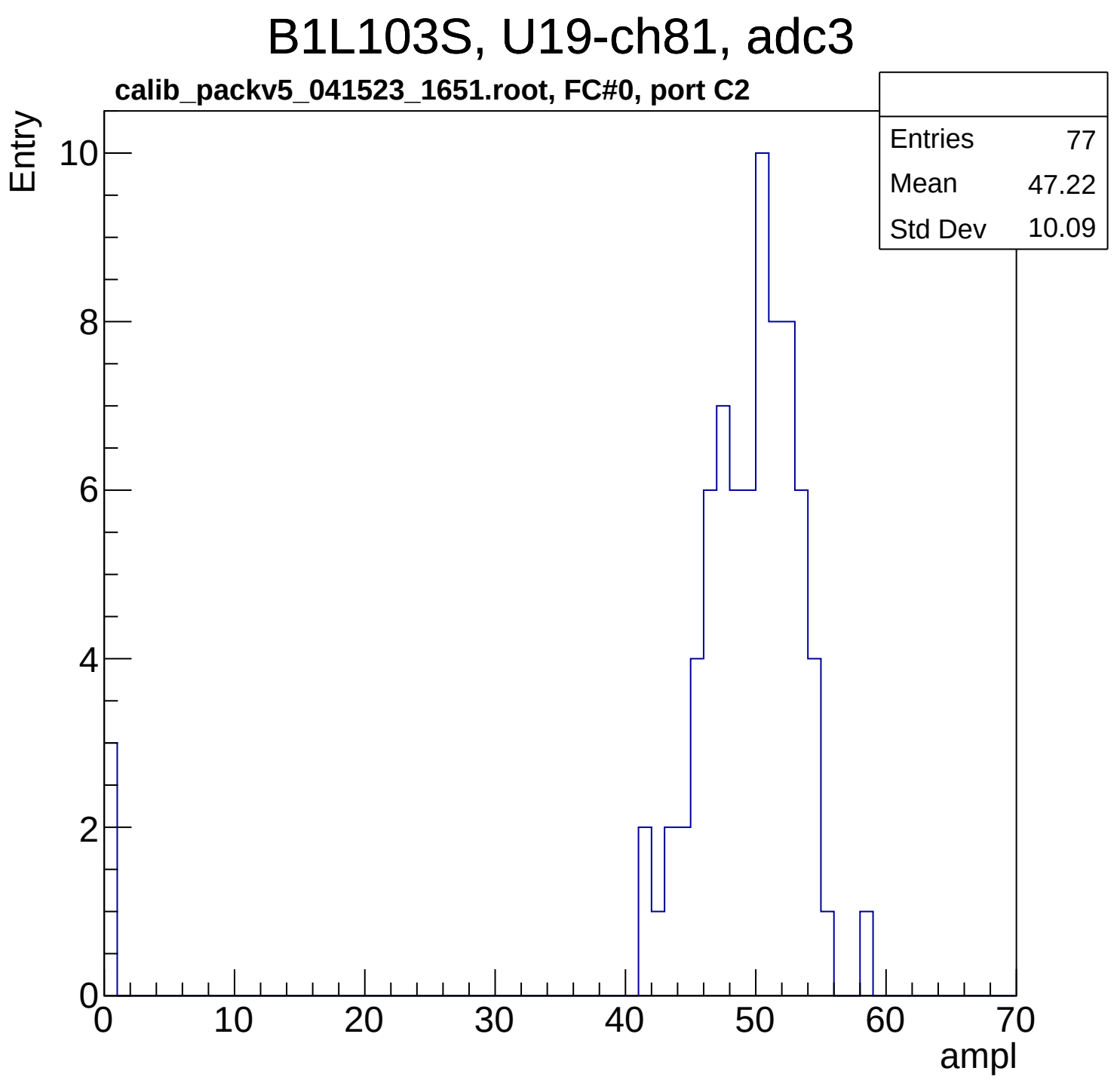
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch81, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 47.22
Std Dev 10.09
Entry
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2
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6
8
10
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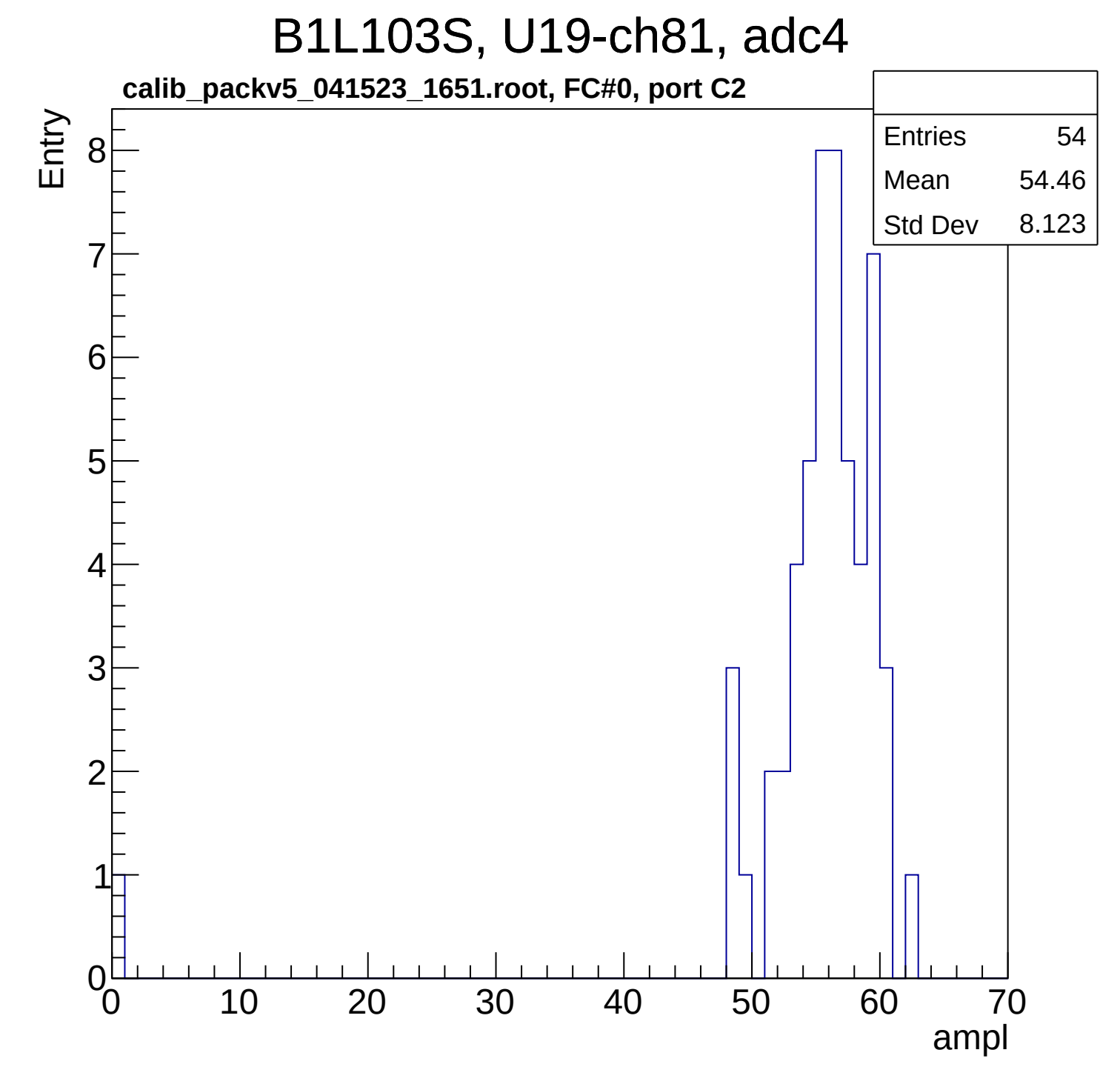
ampl


B1L103S, U19-ch81, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 54.46
Std Dev 8.123
Entry
ampl
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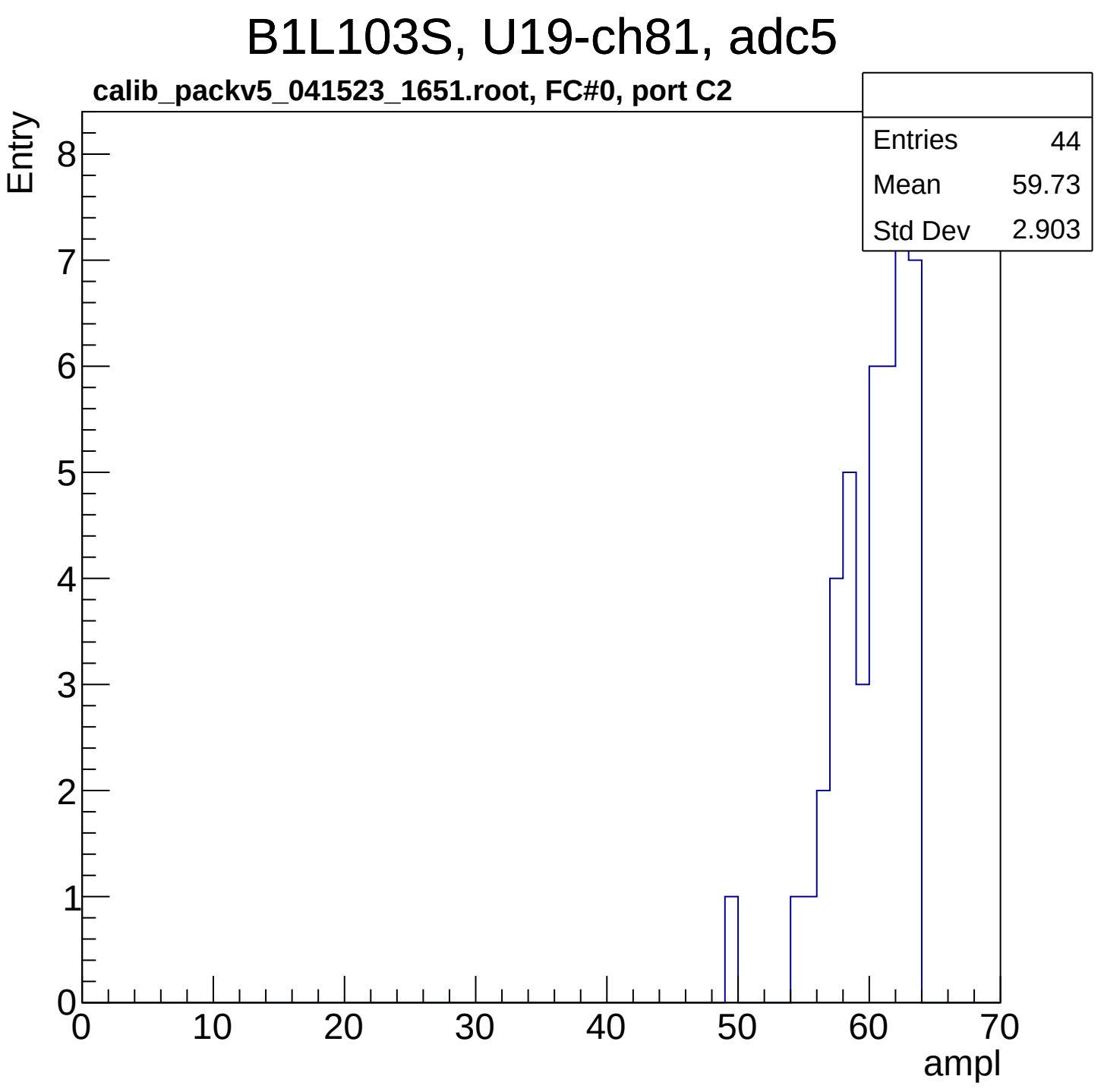
B1L103S, U19-ch81, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 59.73
Std Dev 2.903
Entry
ampl
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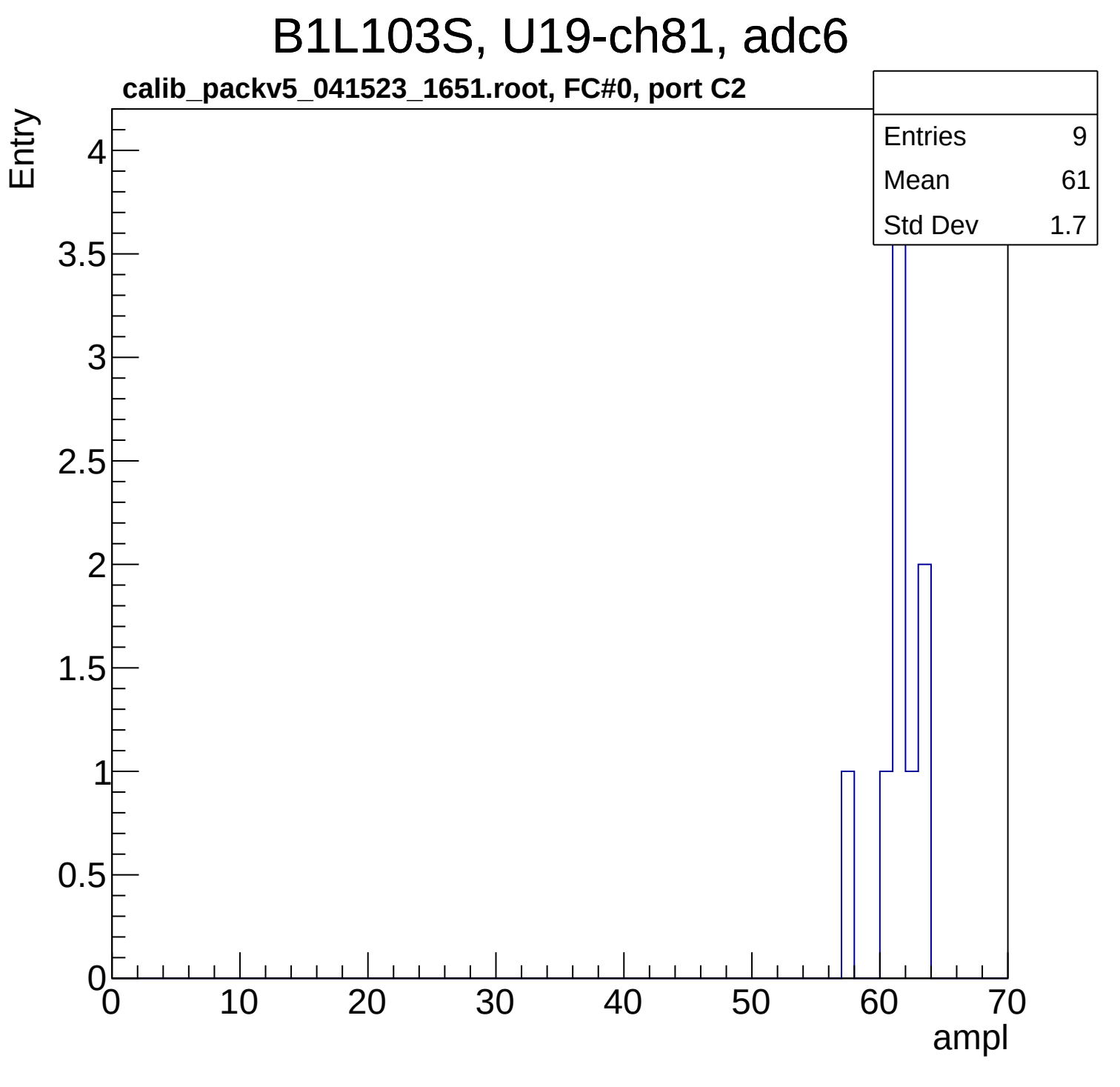
B1L103S, U19-ch81, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 61
Std Dev 1.7
Entry
ampl
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1.5
2
2.5
3
3.5
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0
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40
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60
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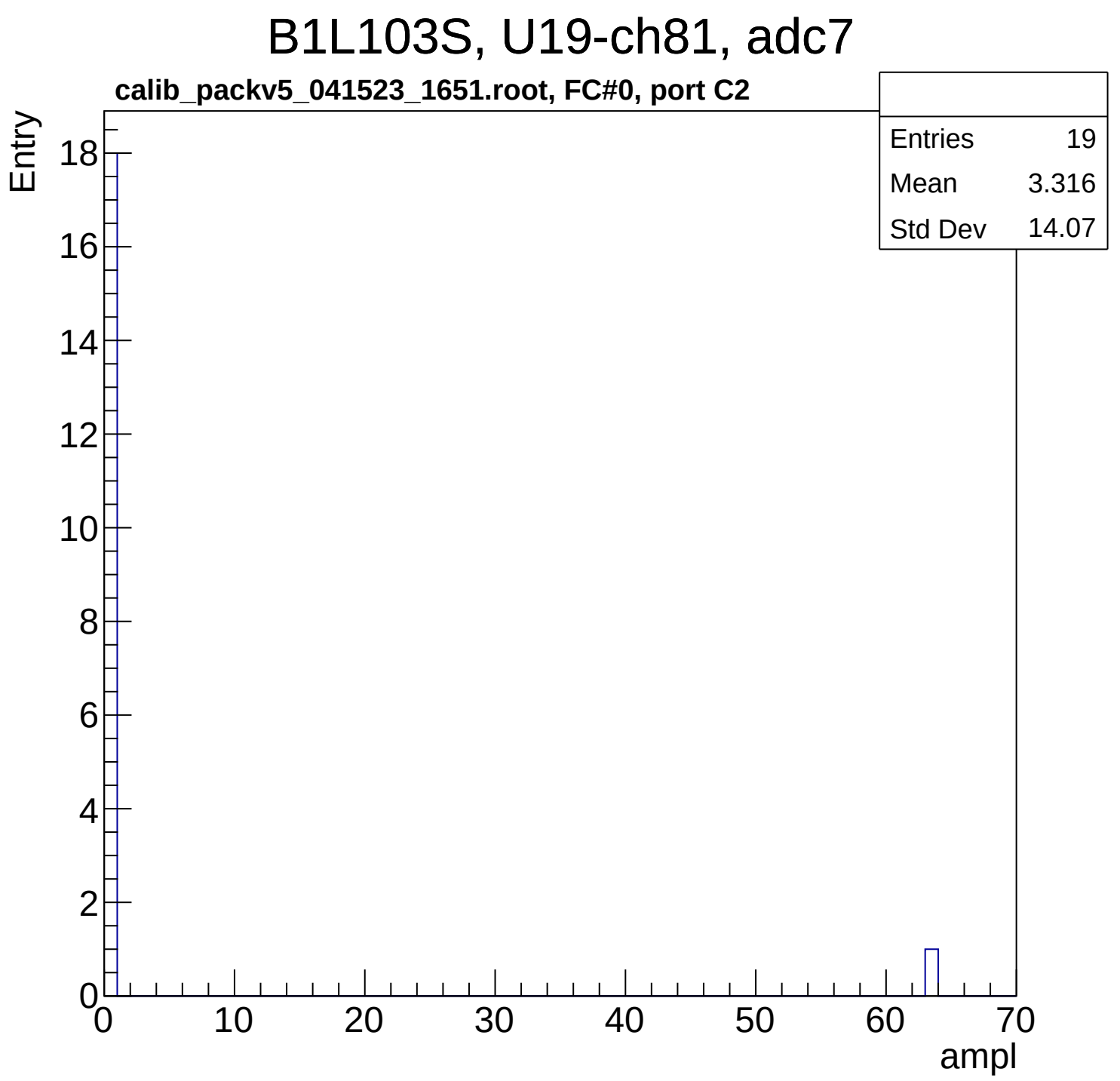
B1L103S, U19-ch81, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.316
Std Dev 14.07
Entry
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6
8
10
12
14
16
18
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10
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50
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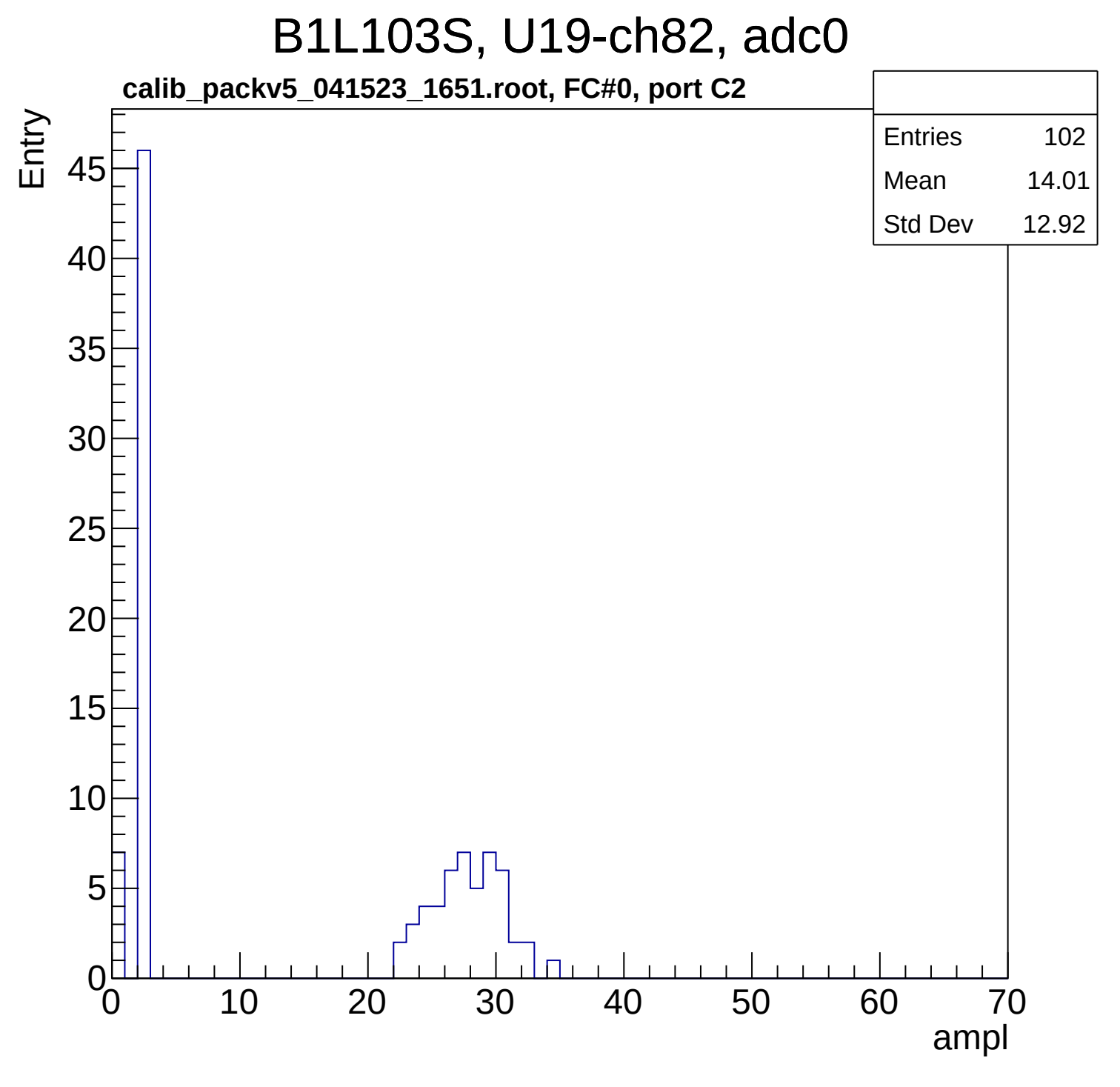
70
ampl


B1L103S, U19-ch82, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 102
Mean 14.01
Std Dev 12.92
Entry
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10
15
20
25
30
35
40
45
0
10
20
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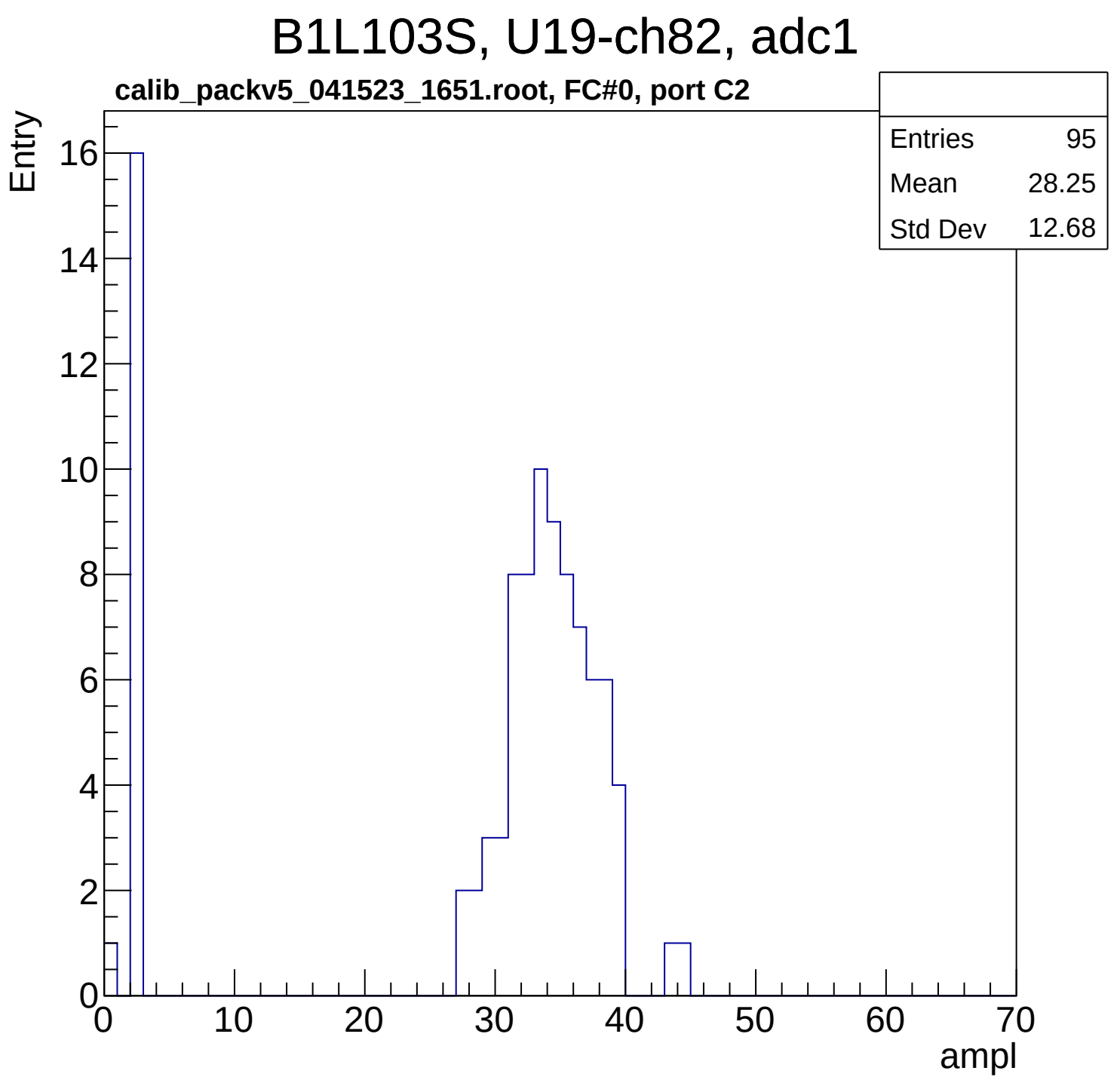
40
50
60
70
ampl


B1L103S, U19-ch82, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 28.25
Std Dev 12.68
Entry
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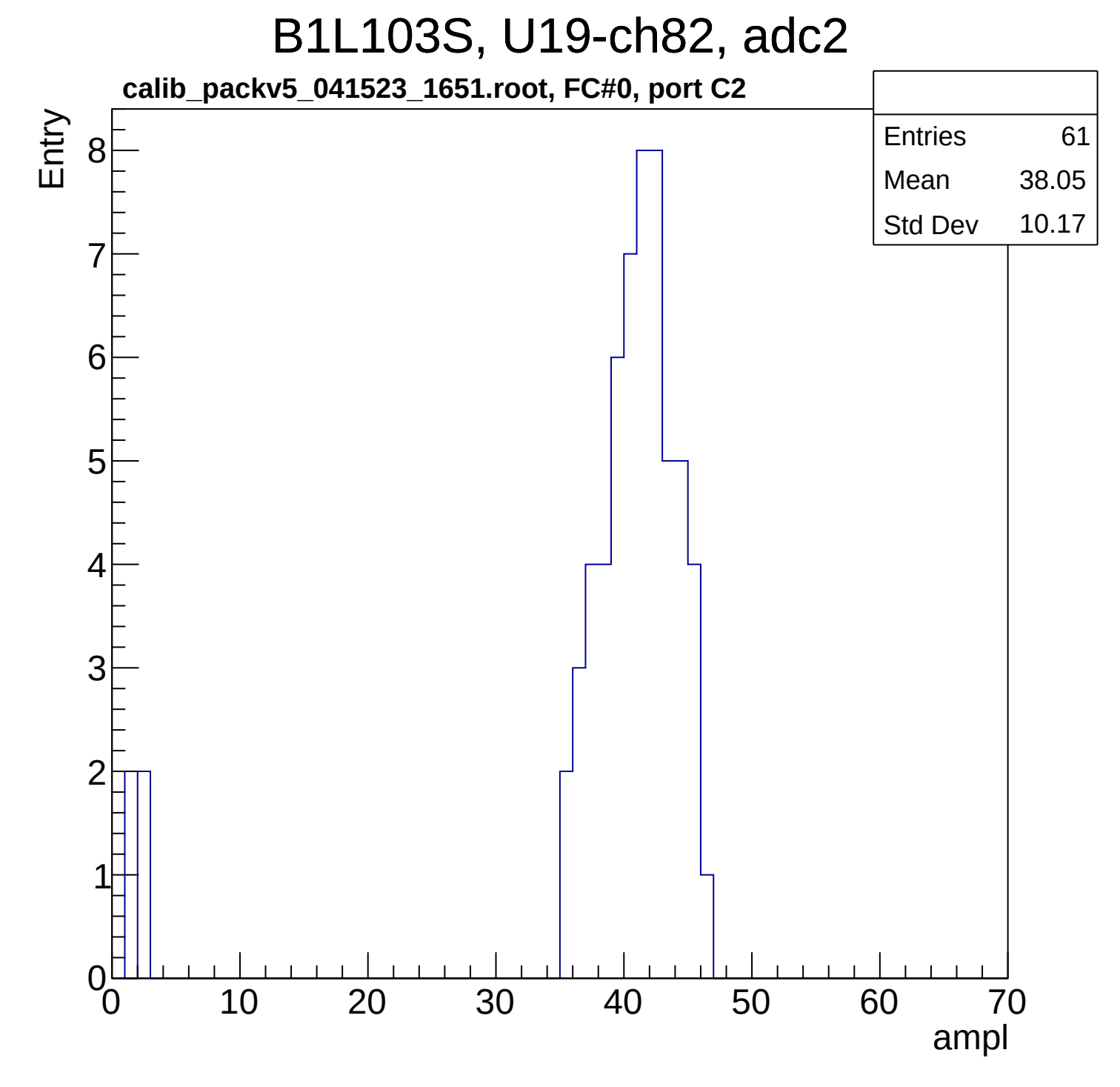
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch82, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 38.05
Std Dev 10.17
Entry
ampl
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3
4
5
6
7
8
0
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40
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60
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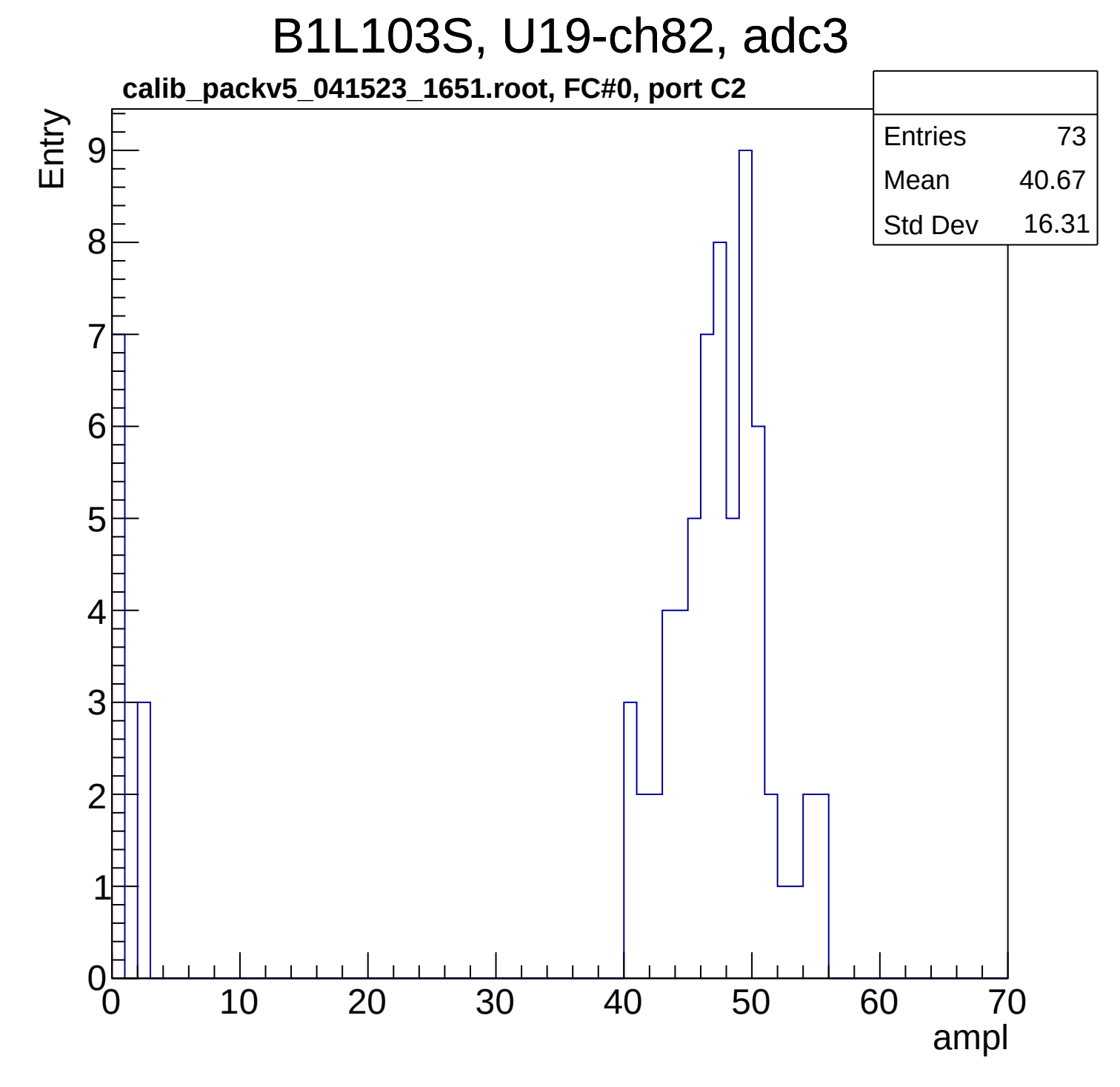
B1L103S, U19-ch82, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 40.67
Std Dev 16.31
Entry
ampl
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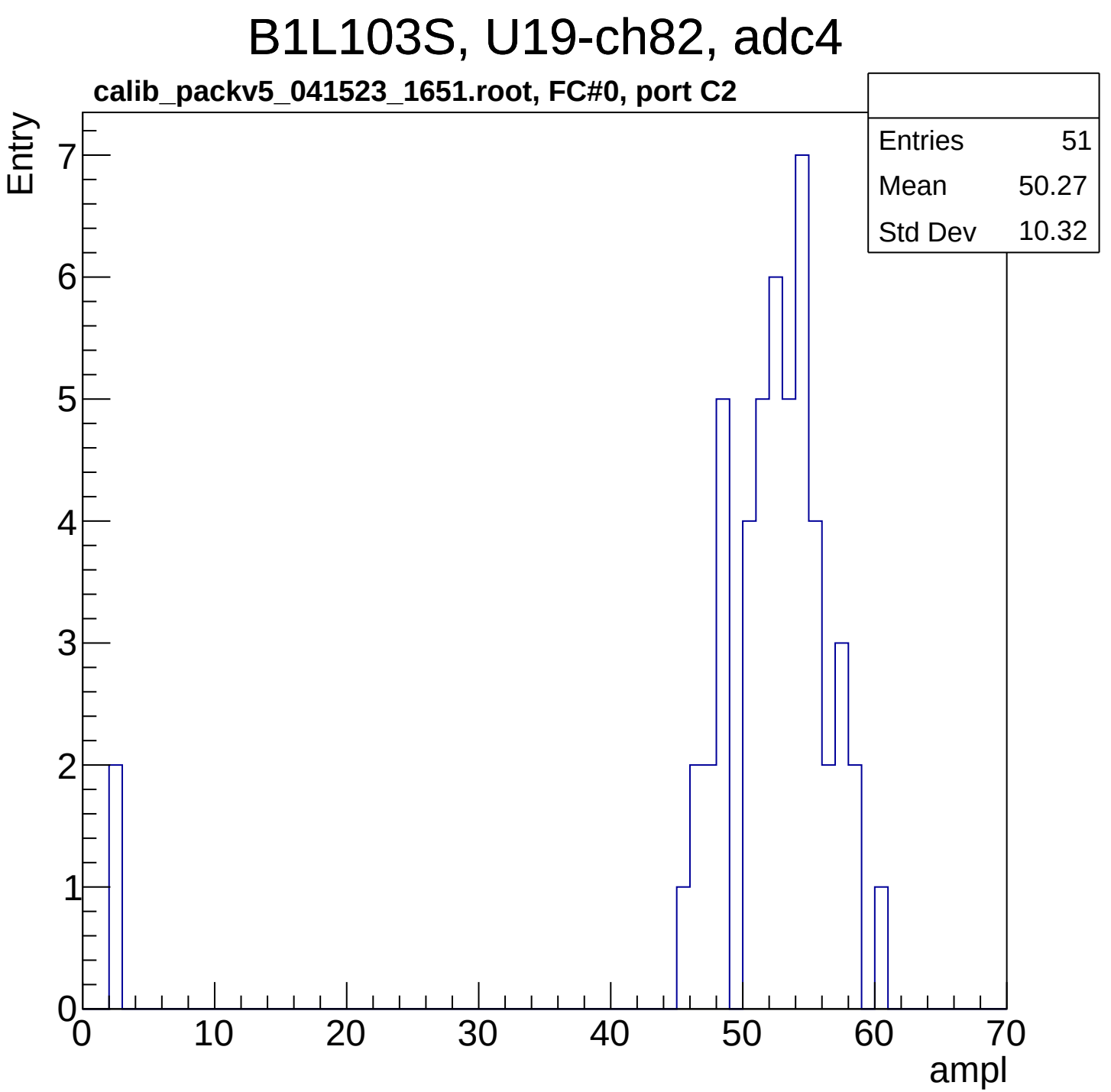
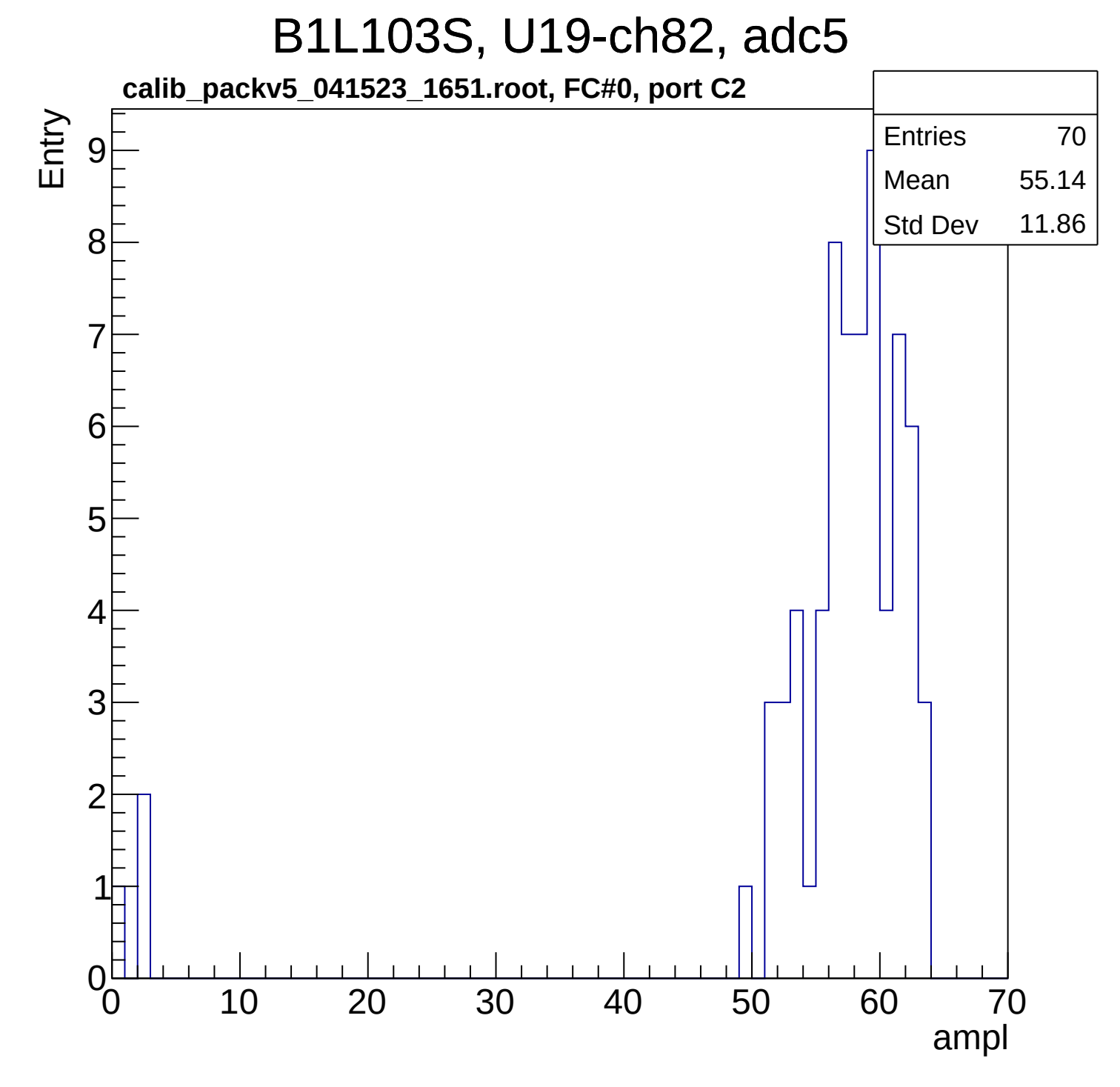
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L103S, U19-ch82, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 50.27
Std Dev 10.32
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch82, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 55.14
Std Dev 11.86
Entry
ampl
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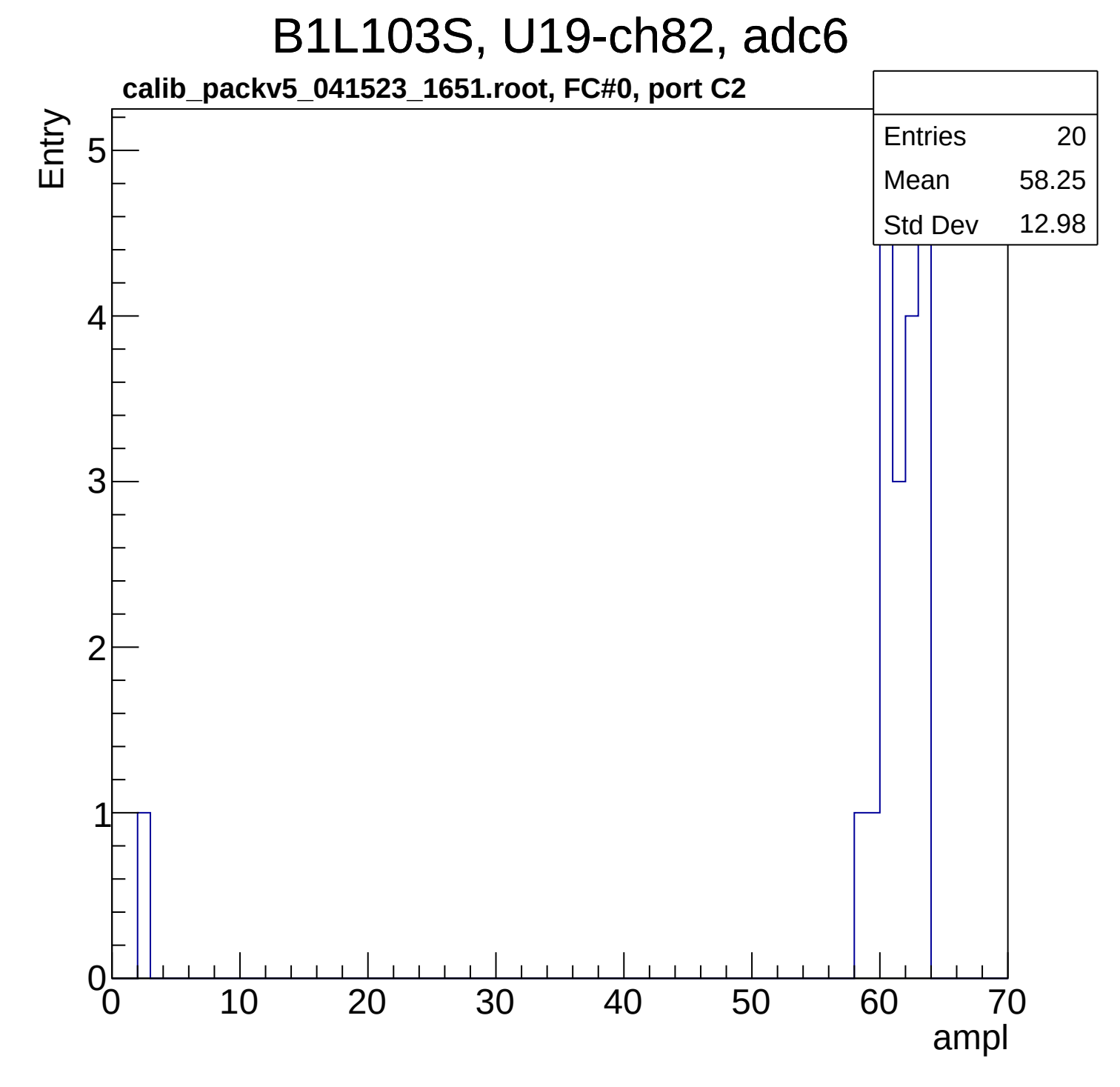
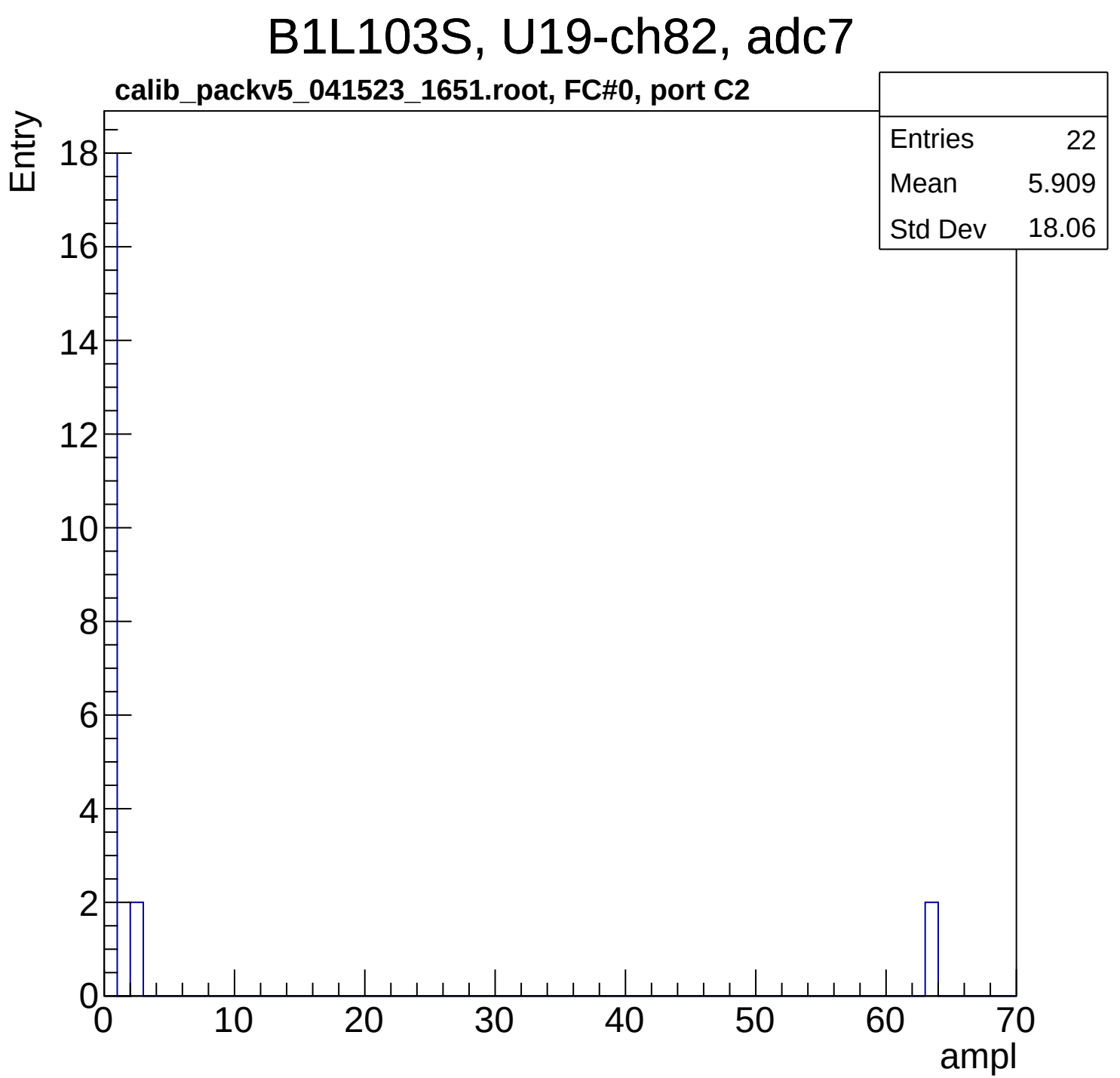
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch82, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 58.25
Std Dev 12.98
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U19-ch82, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 5.909
Std Dev 18.06
Entry
0
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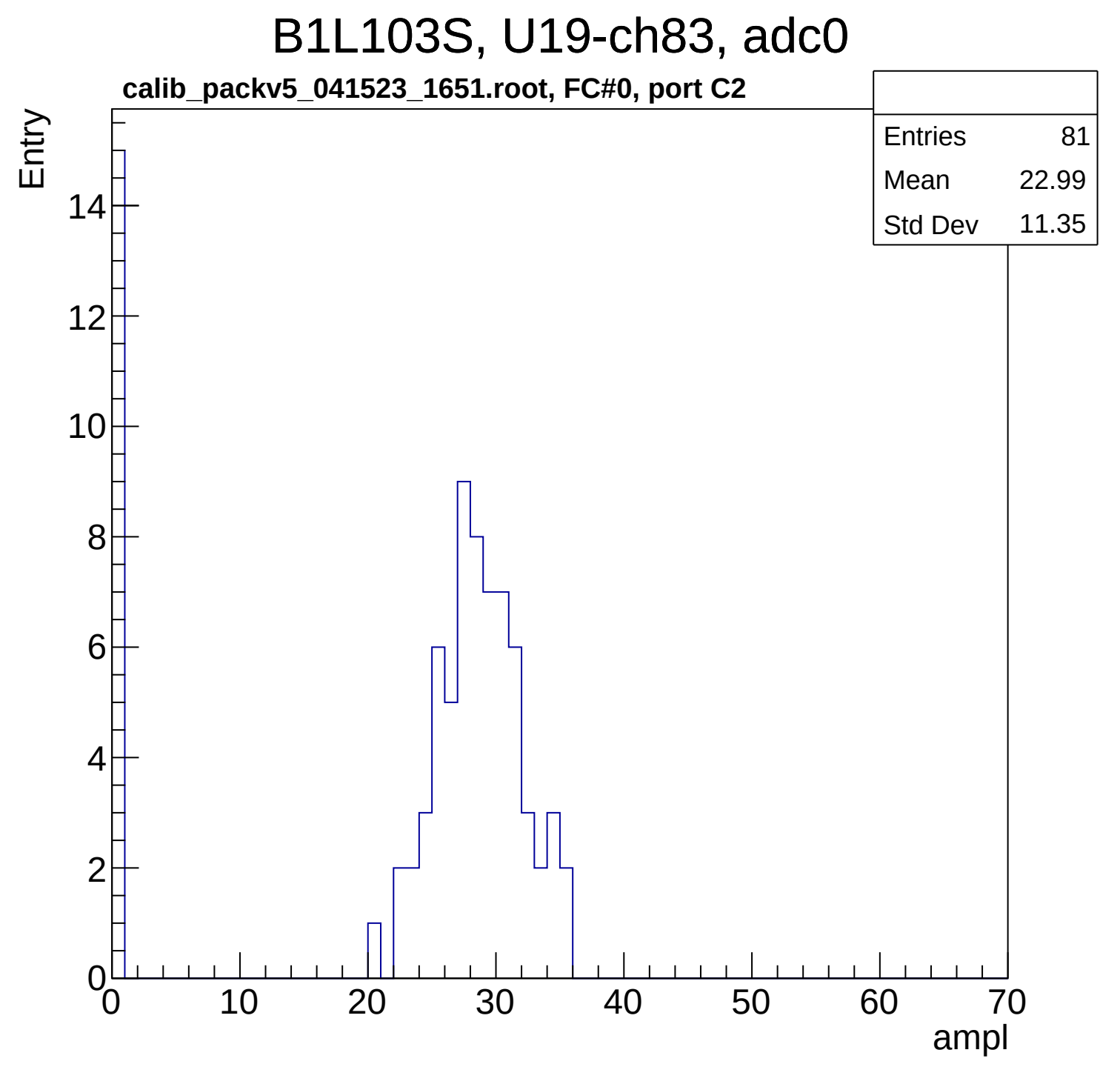
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch83, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 22.99
Std Dev 11.35
Entry
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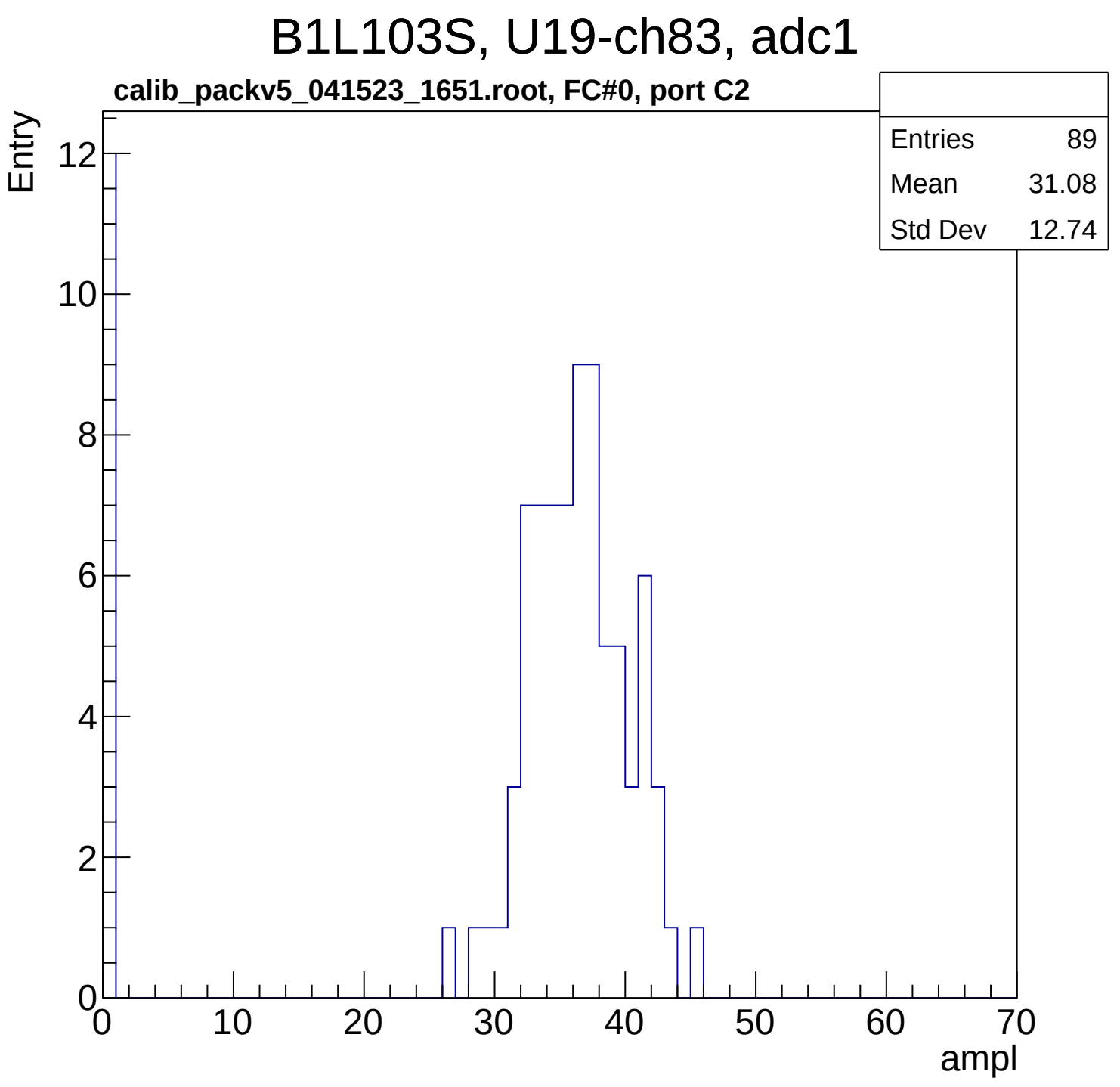
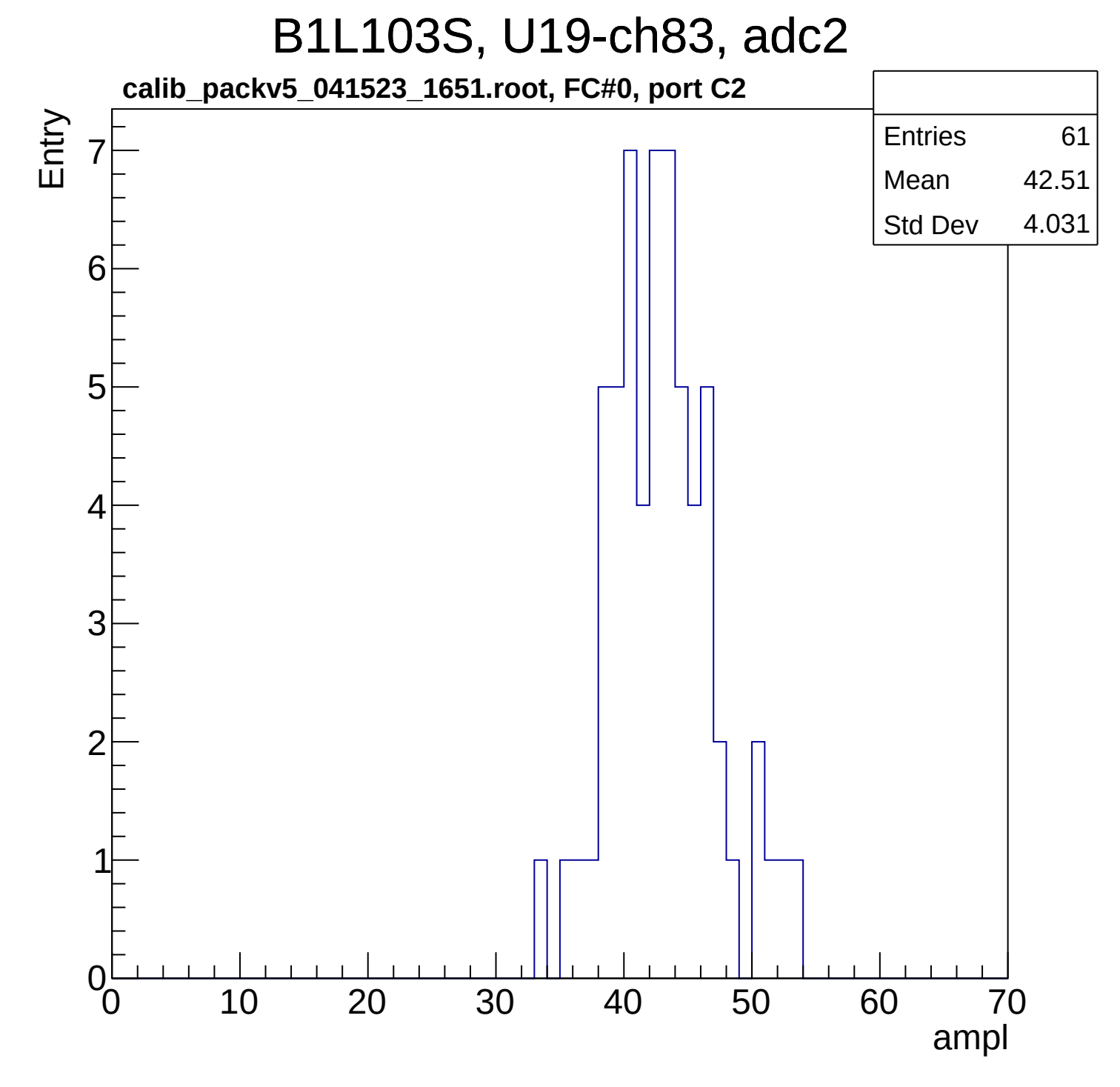
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch83, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 31.08
Std Dev 12.74
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch83, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 42.51
Std Dev 4.031
Entry
ampl
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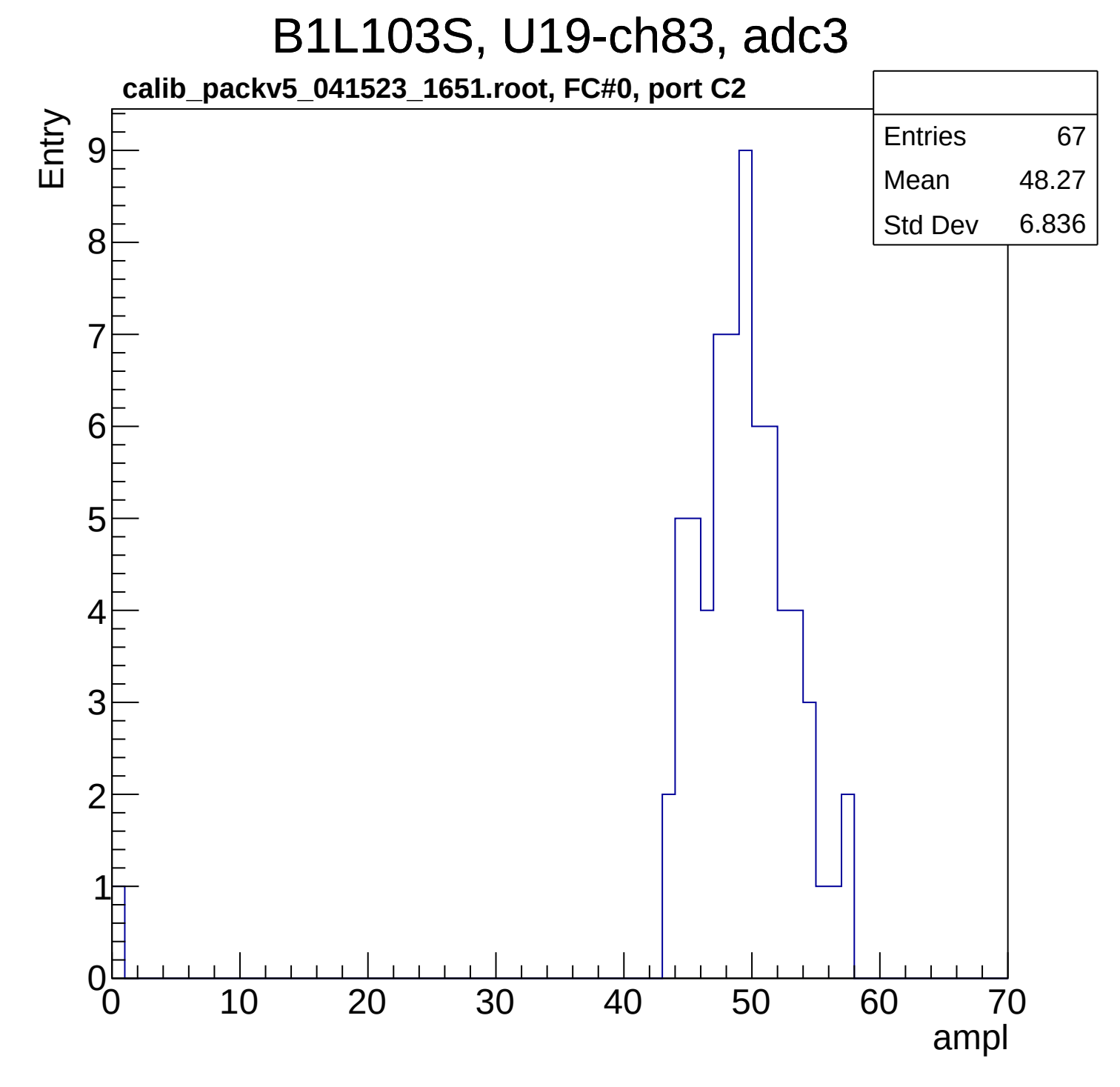
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch83, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 48.27
Std Dev 6.836
Entry
ampl
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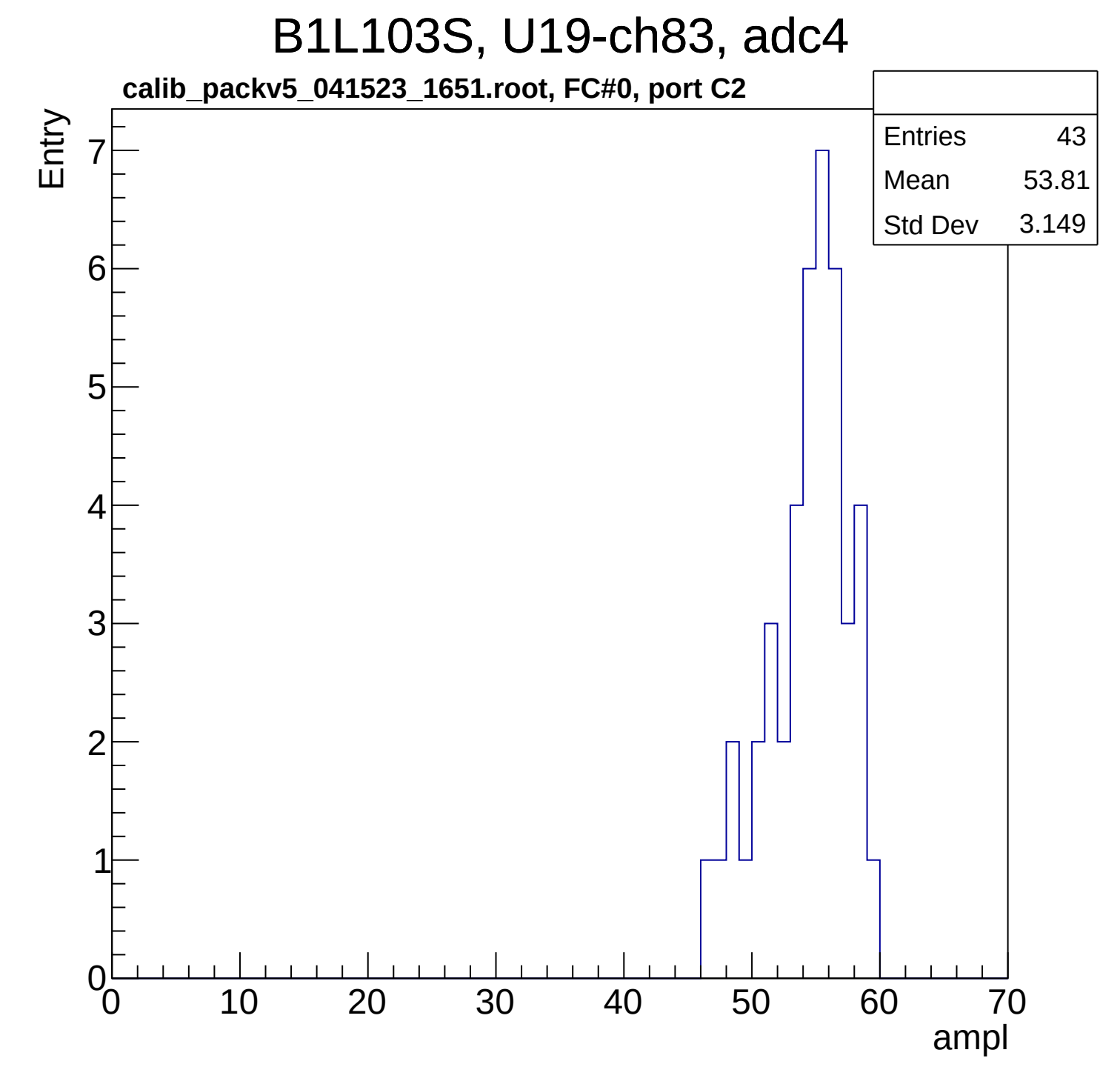
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L103S, U19-ch83, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 53.81
Std Dev 3.149
Entry
ampl
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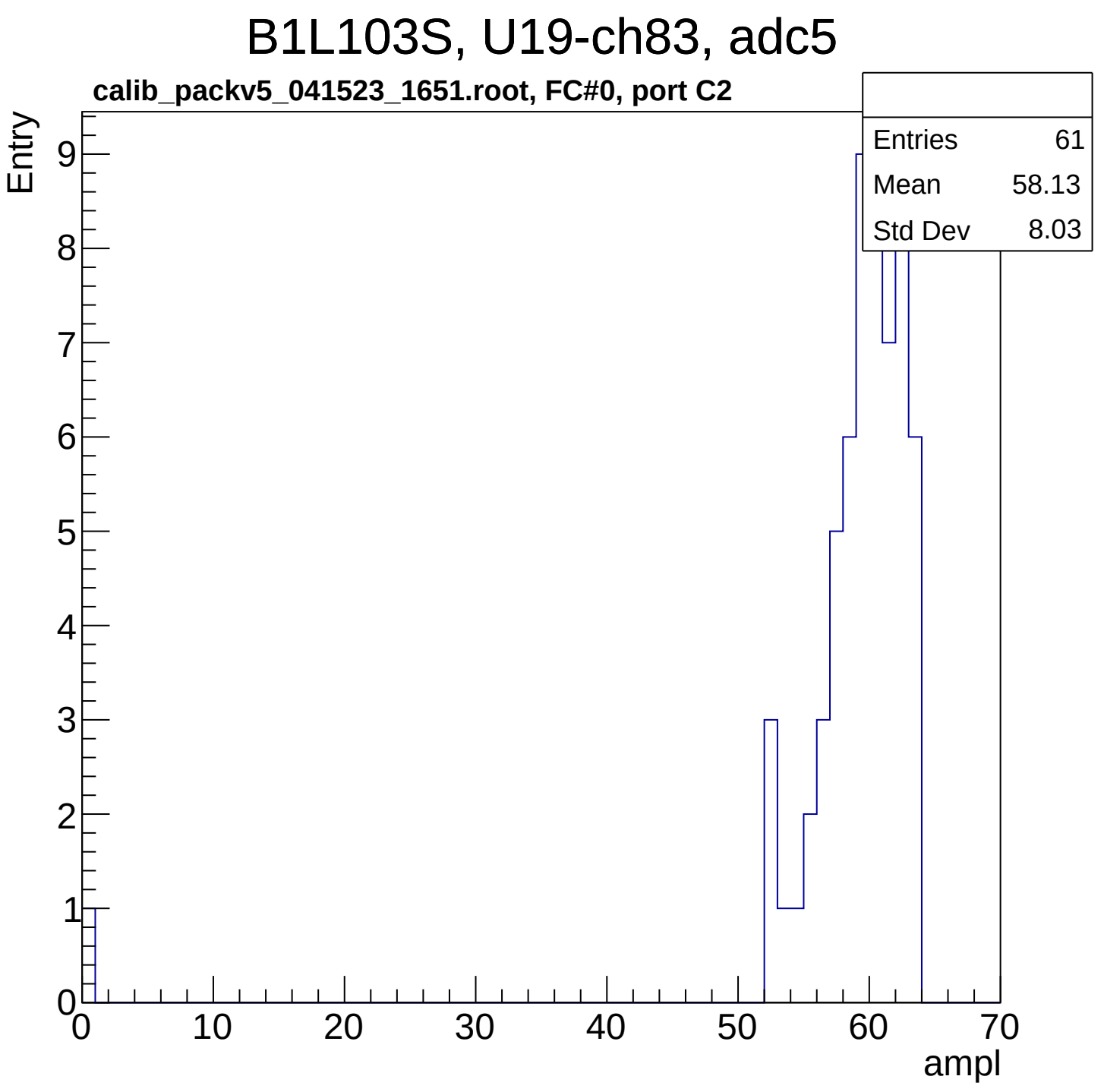
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch83, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 58.13
Std Dev 8.03
Entry
ampl
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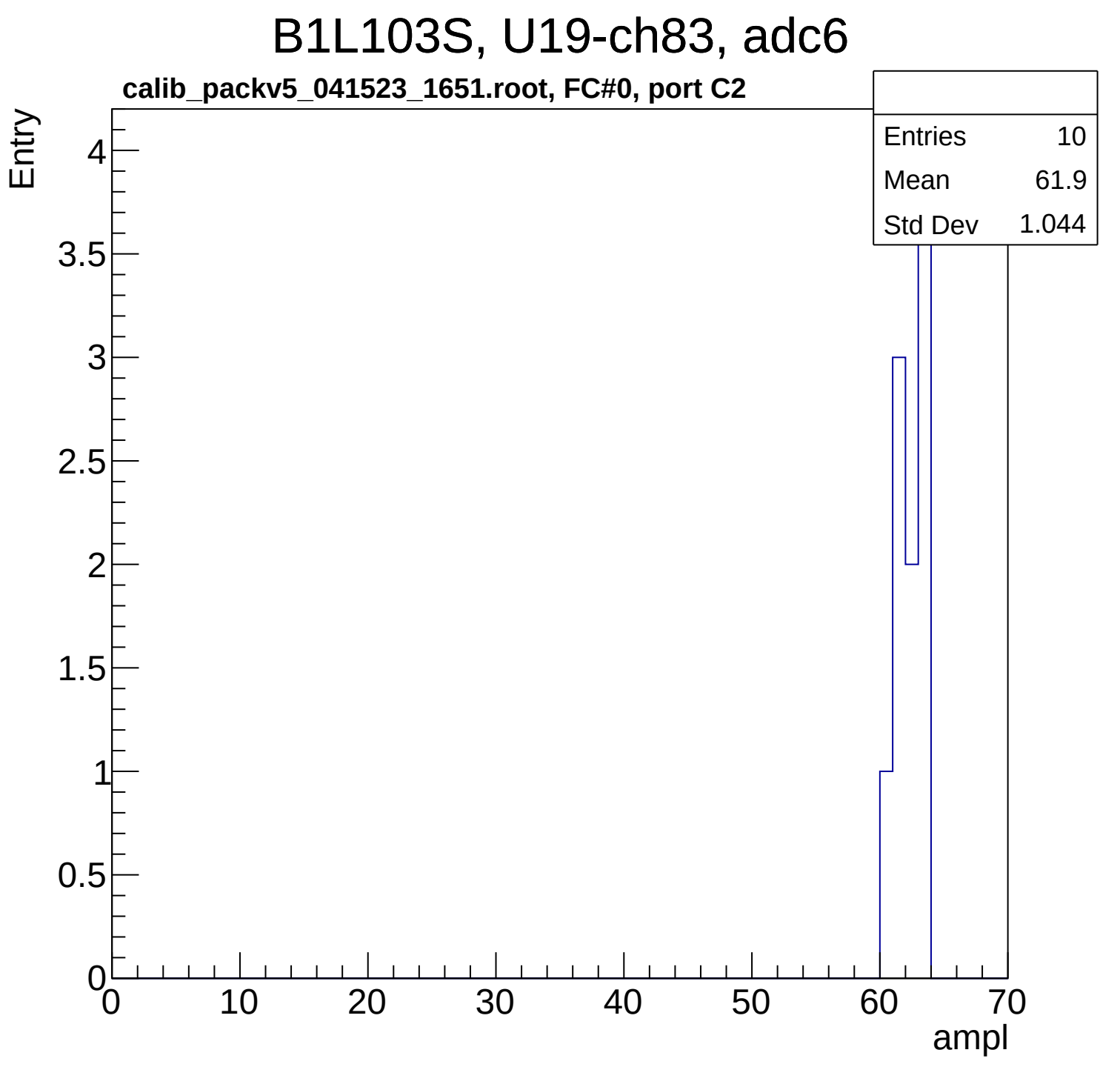
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L103S, U19-ch83, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61.9
Std Dev 1.044
Entry
ampl
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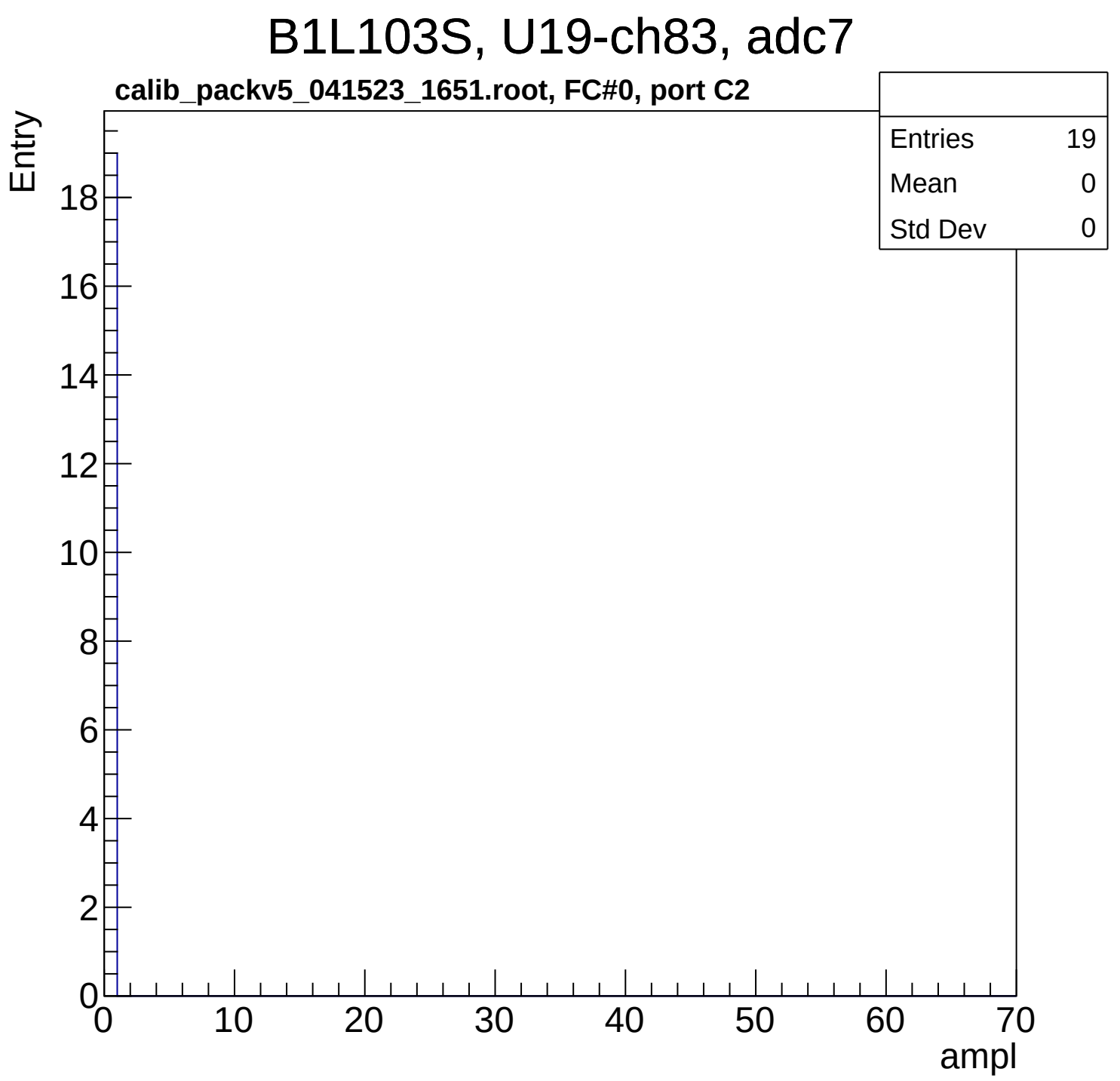
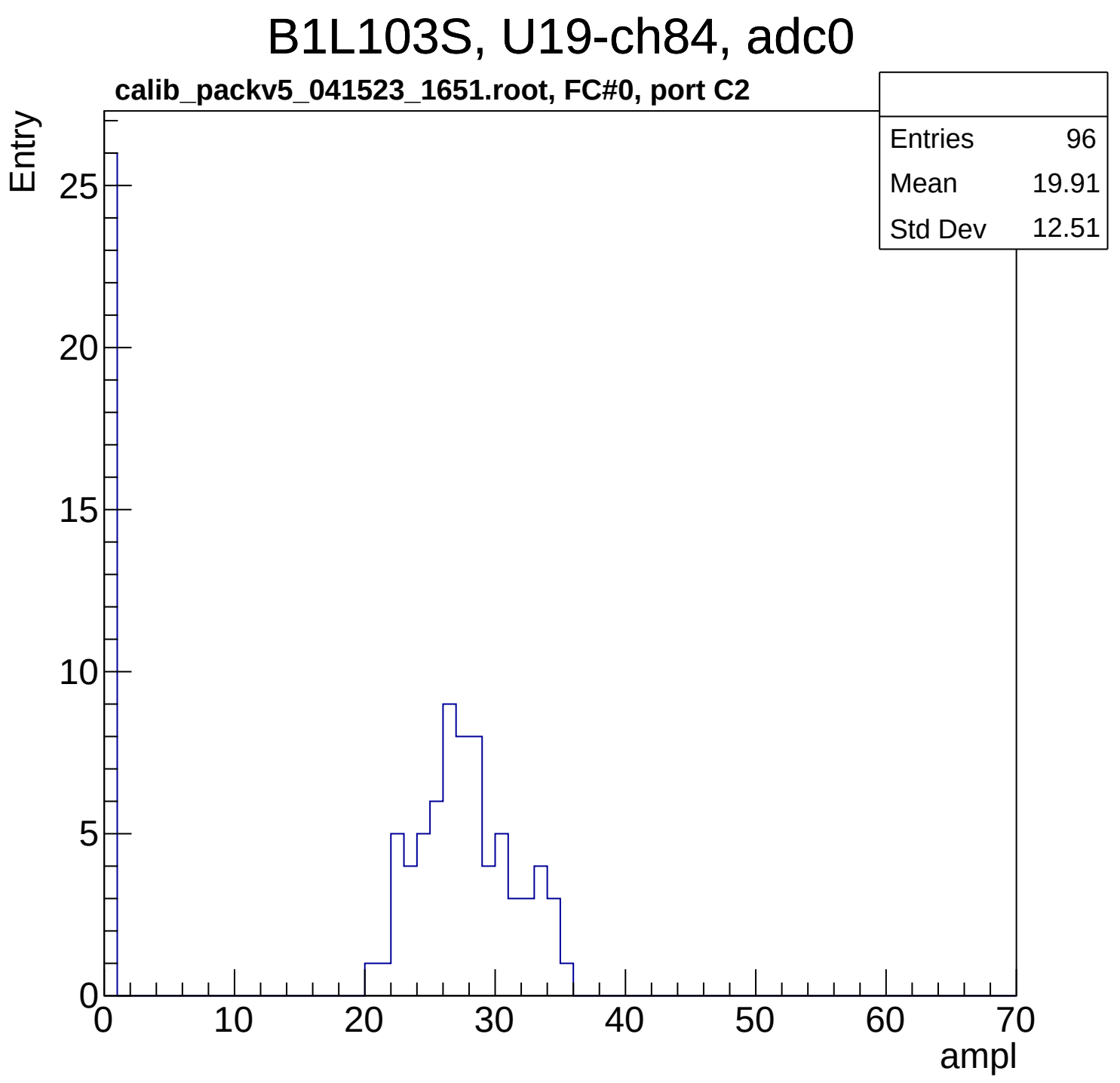
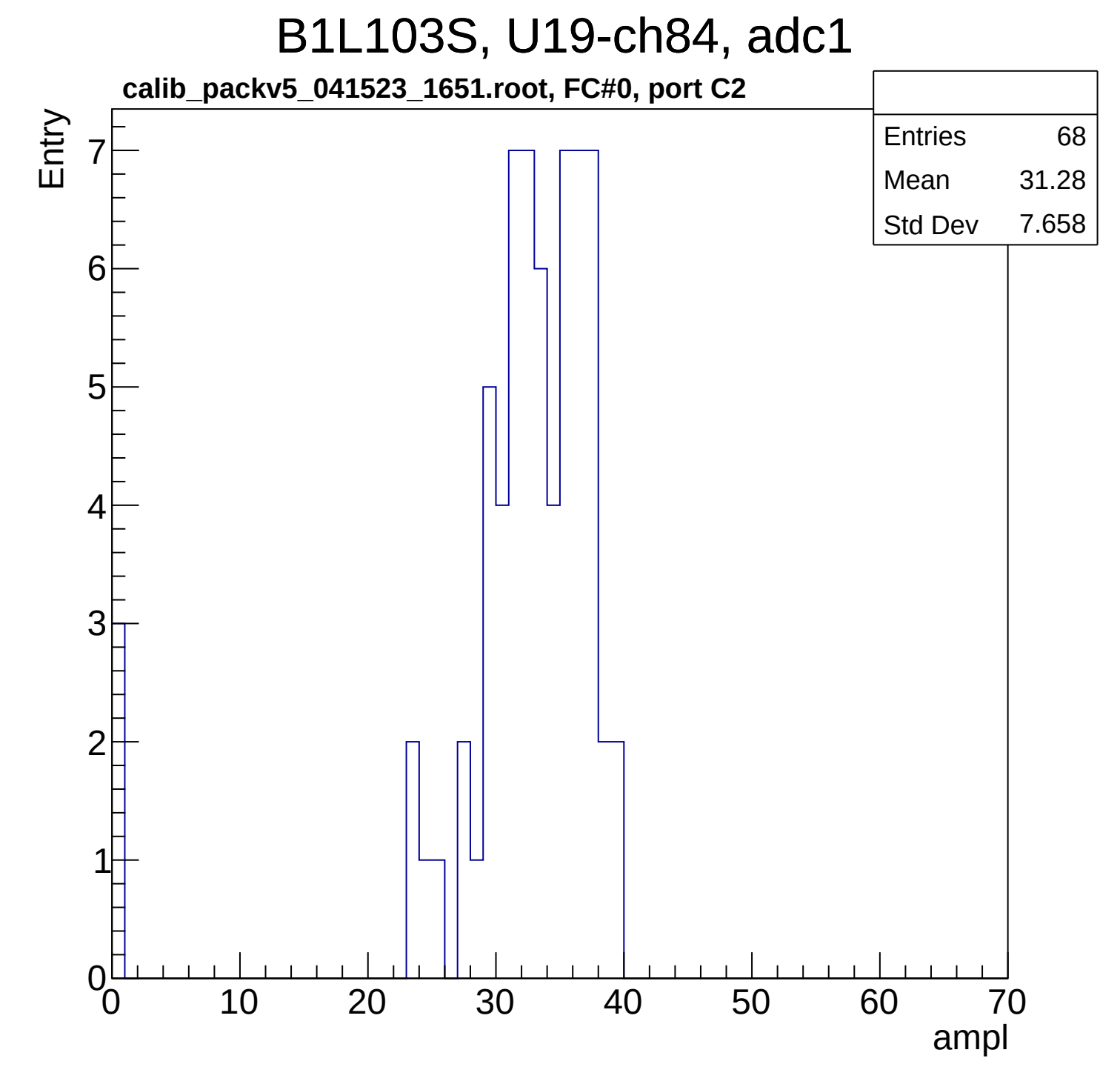
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U19-ch83, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch84, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 96
Mean 19.91
Std Dev 12.51
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch84, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 31.28
Std Dev 7.658
Entry
ampl
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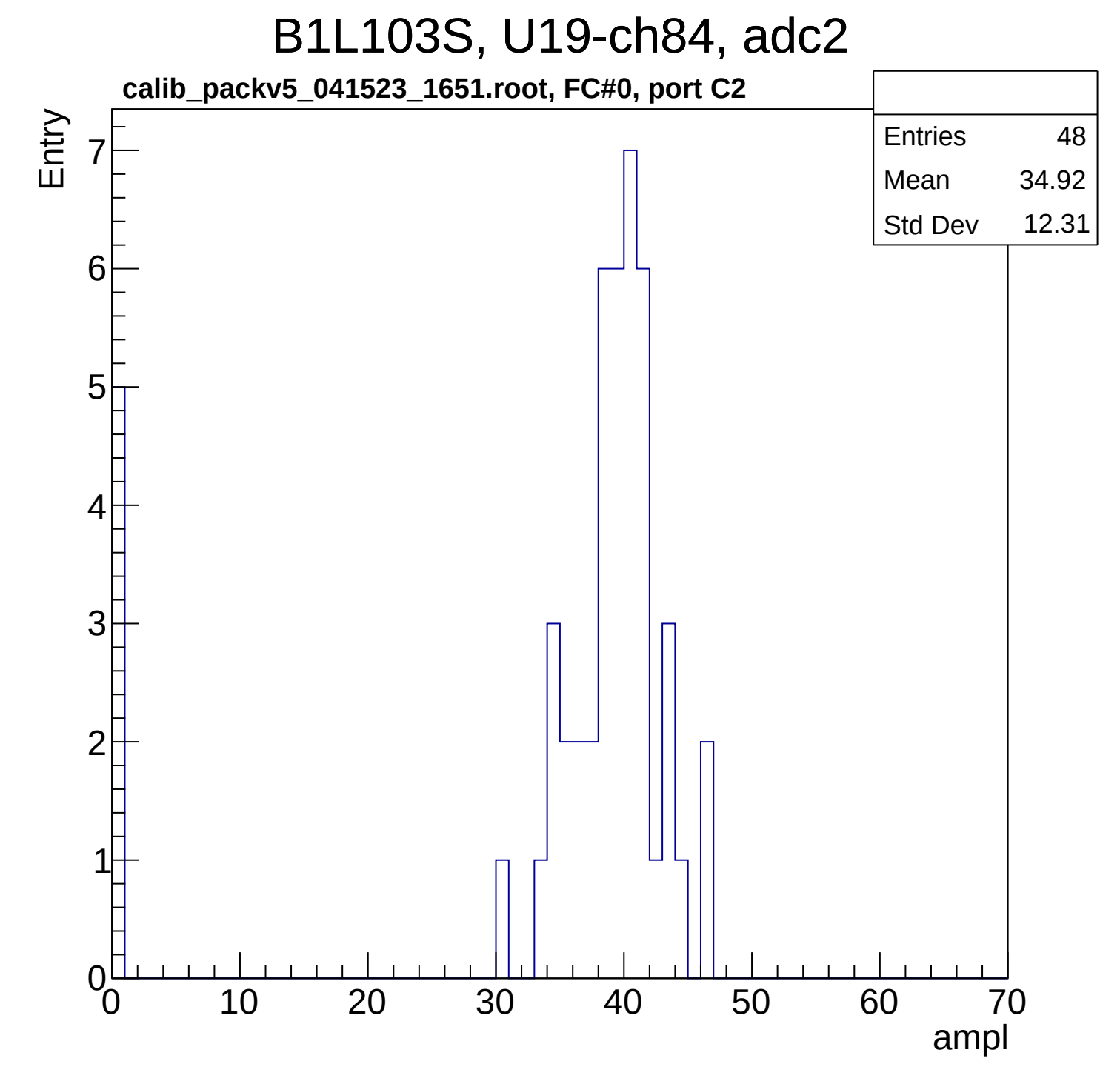
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch84, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 34.92
Std Dev 12.31
Entry
ampl
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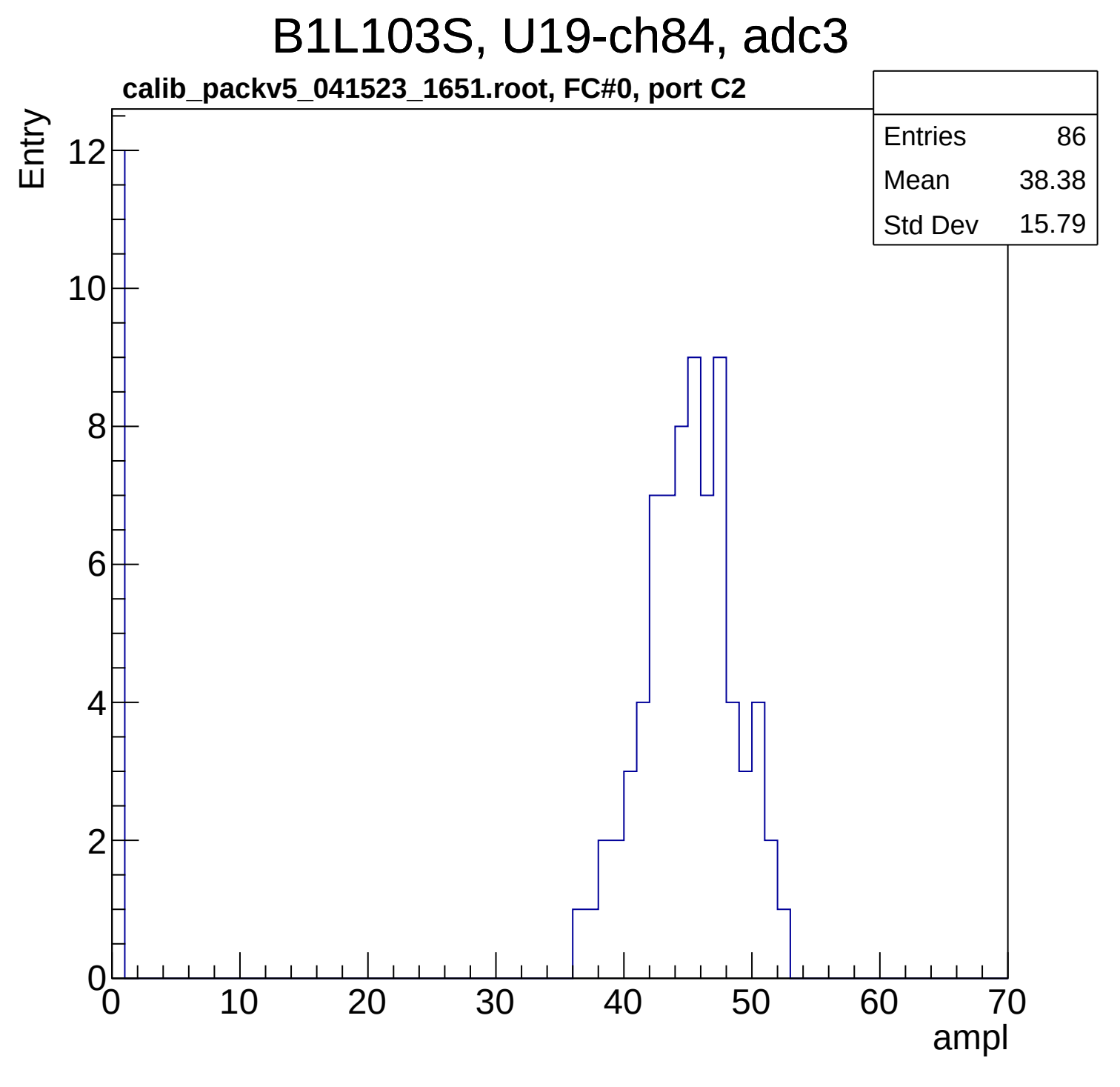
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch84, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 38.38
Std Dev 15.79
Entry
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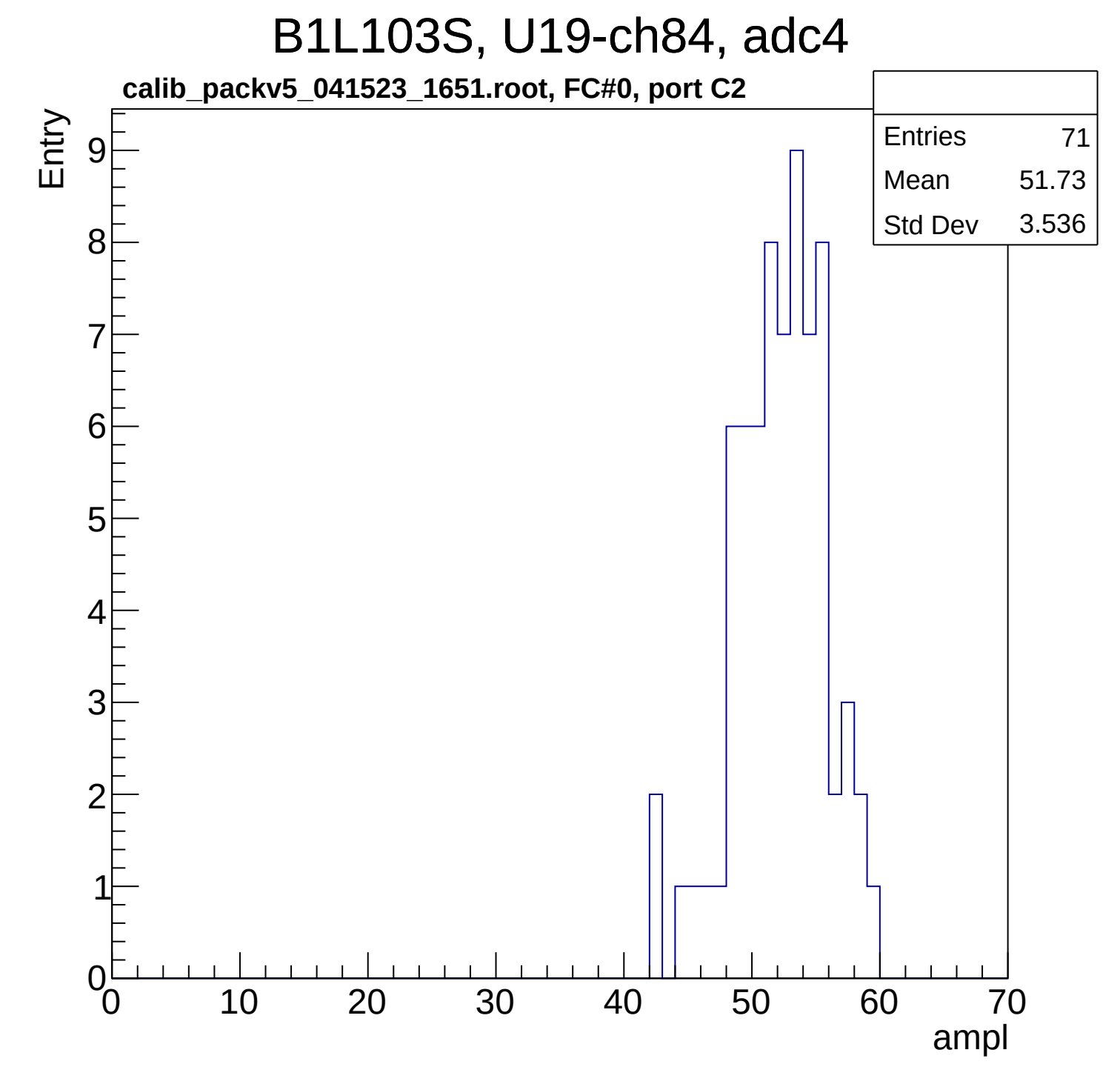
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch84, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 51.73
Std Dev 3.536
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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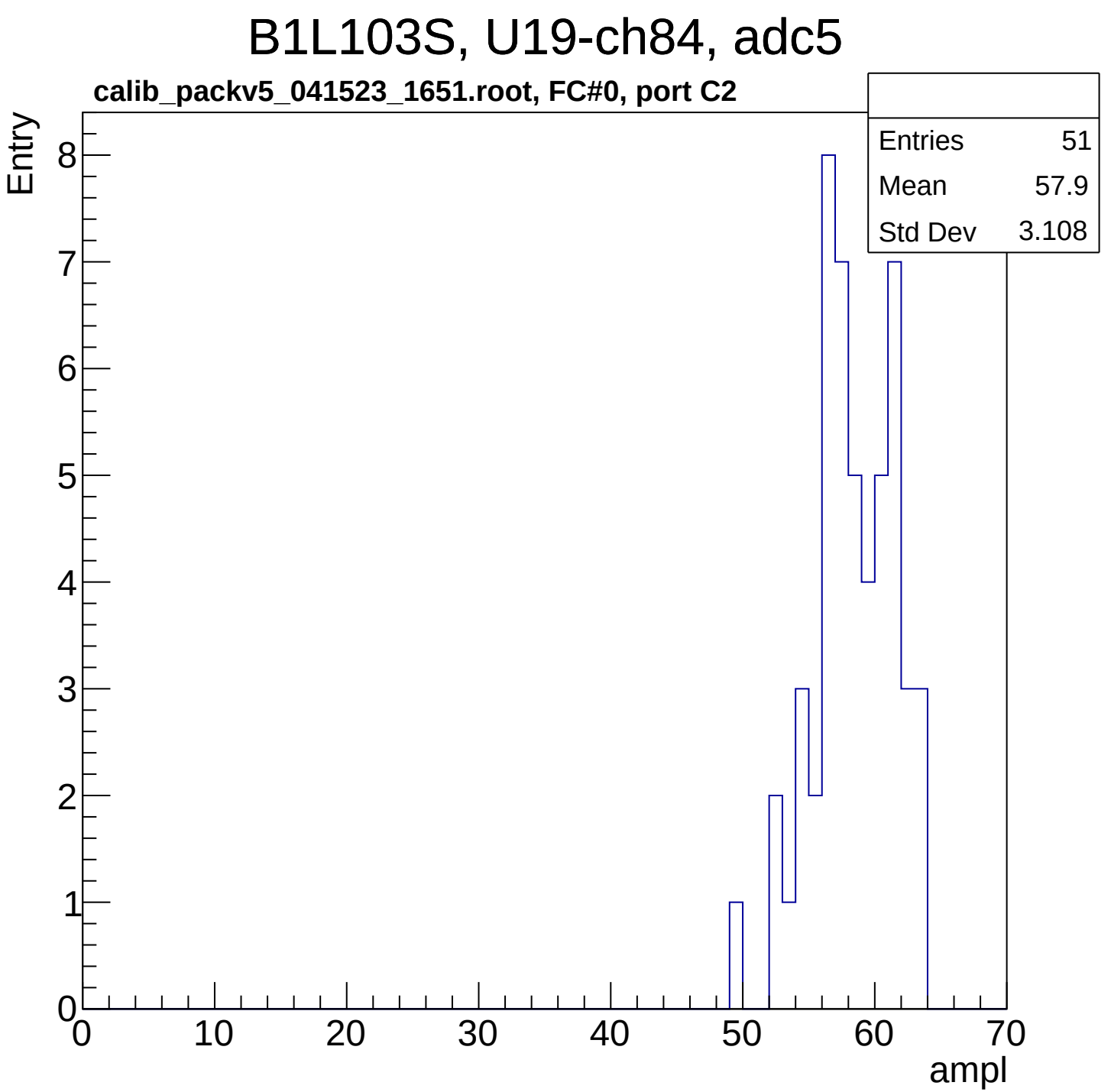
B1L103S, U19-ch84, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 57.9
Std Dev 3.108
Entry
ampl
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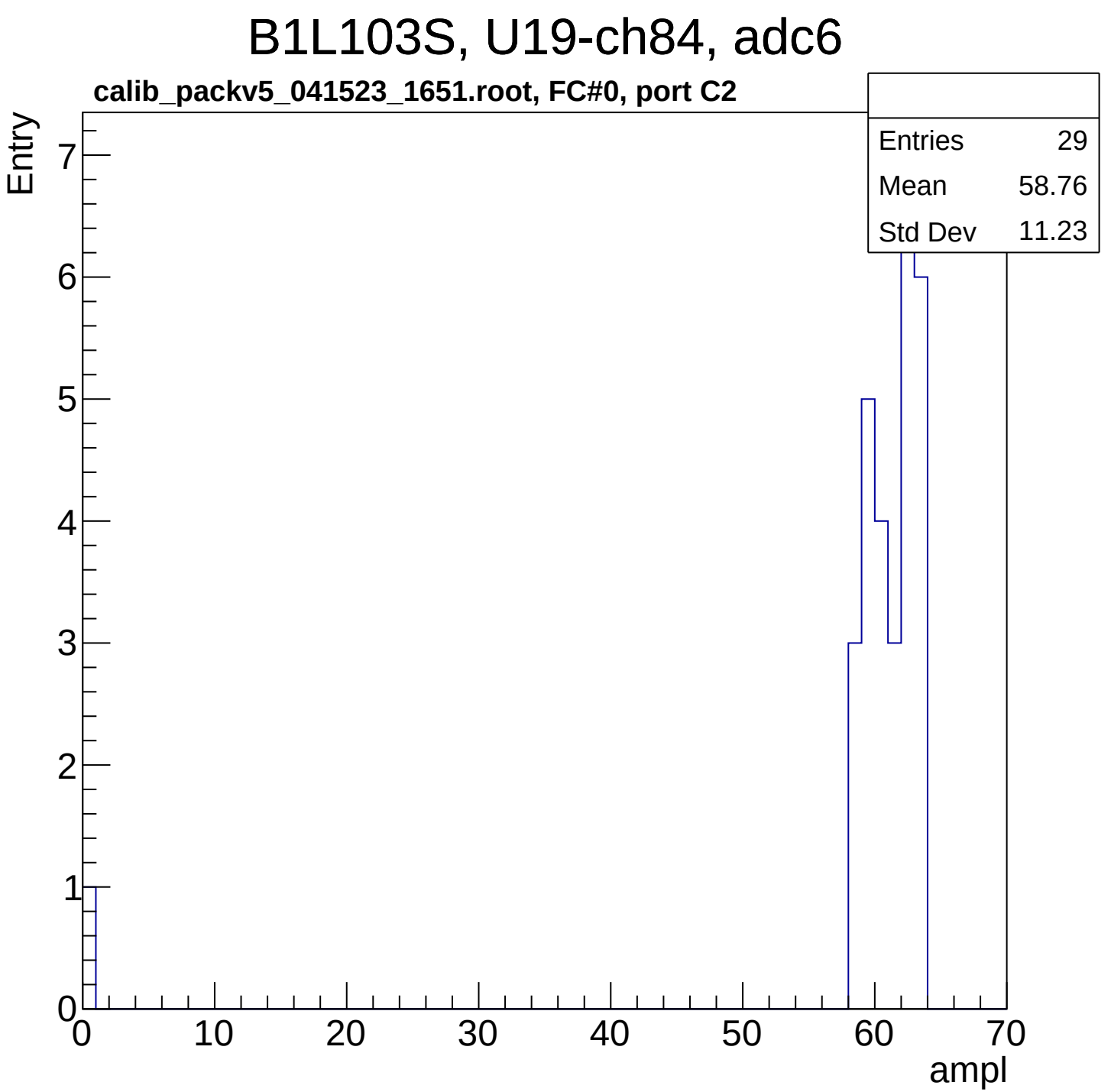
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch84, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 58.76
Std Dev 11.23
Entry
ampl
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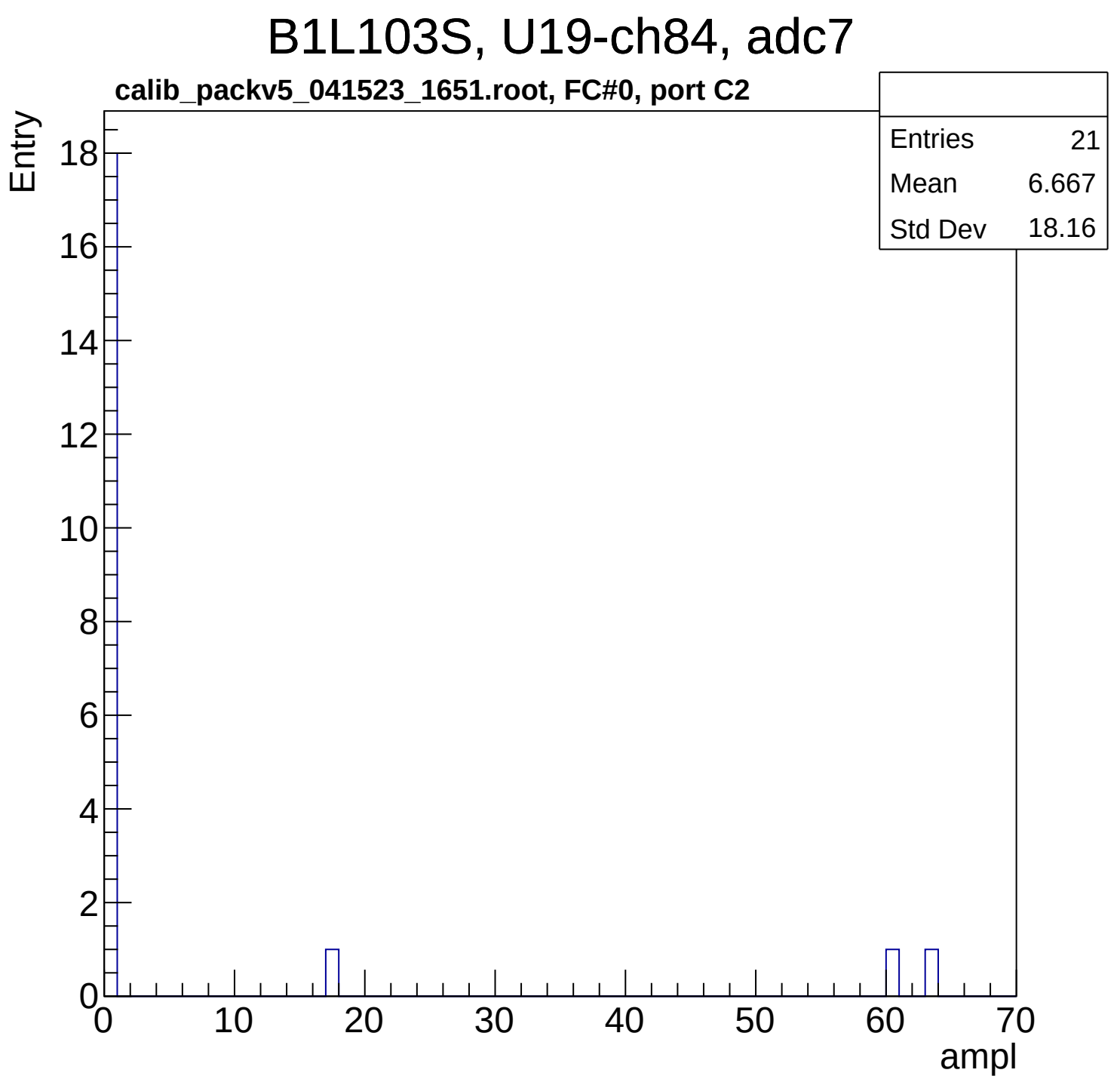
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch84, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 6.667
Std Dev 18.16
Entry
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4
6
8
10
12
14
16
18
0
10
20
30
40
50
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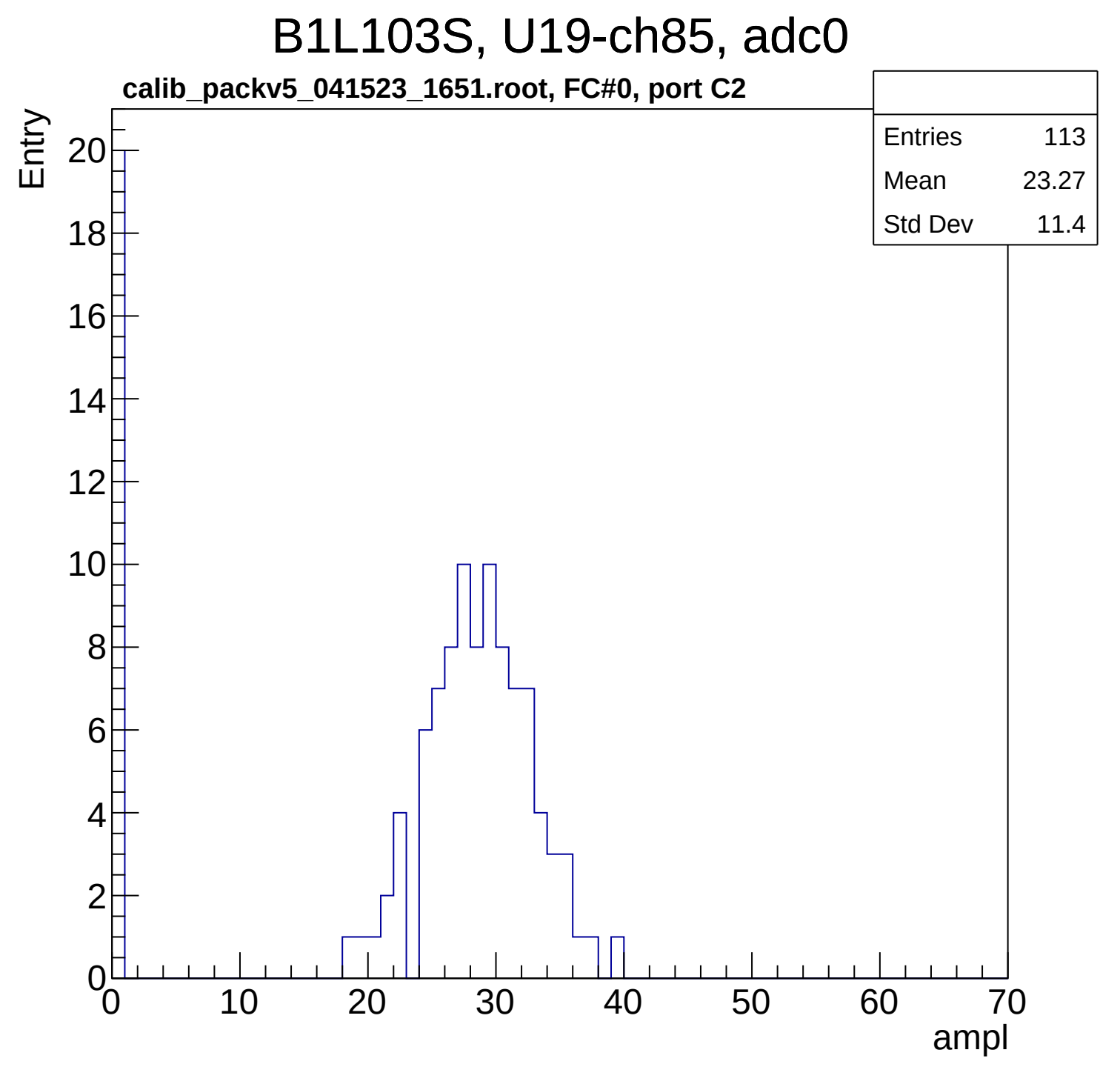
70
ampl


B1L103S, U19-ch85, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 113
Mean 23.27
Std Dev 11.4
Entry
ampl
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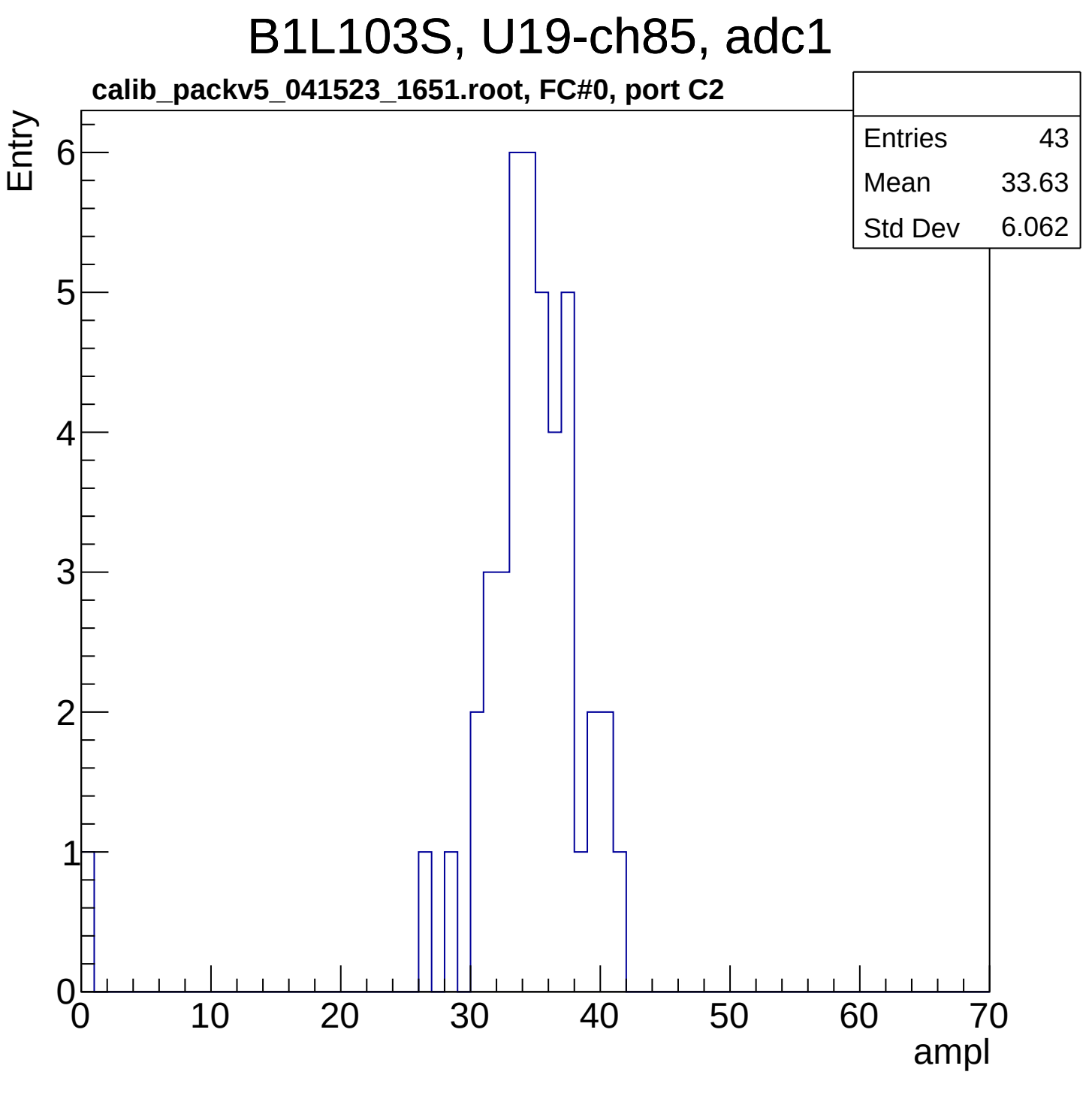
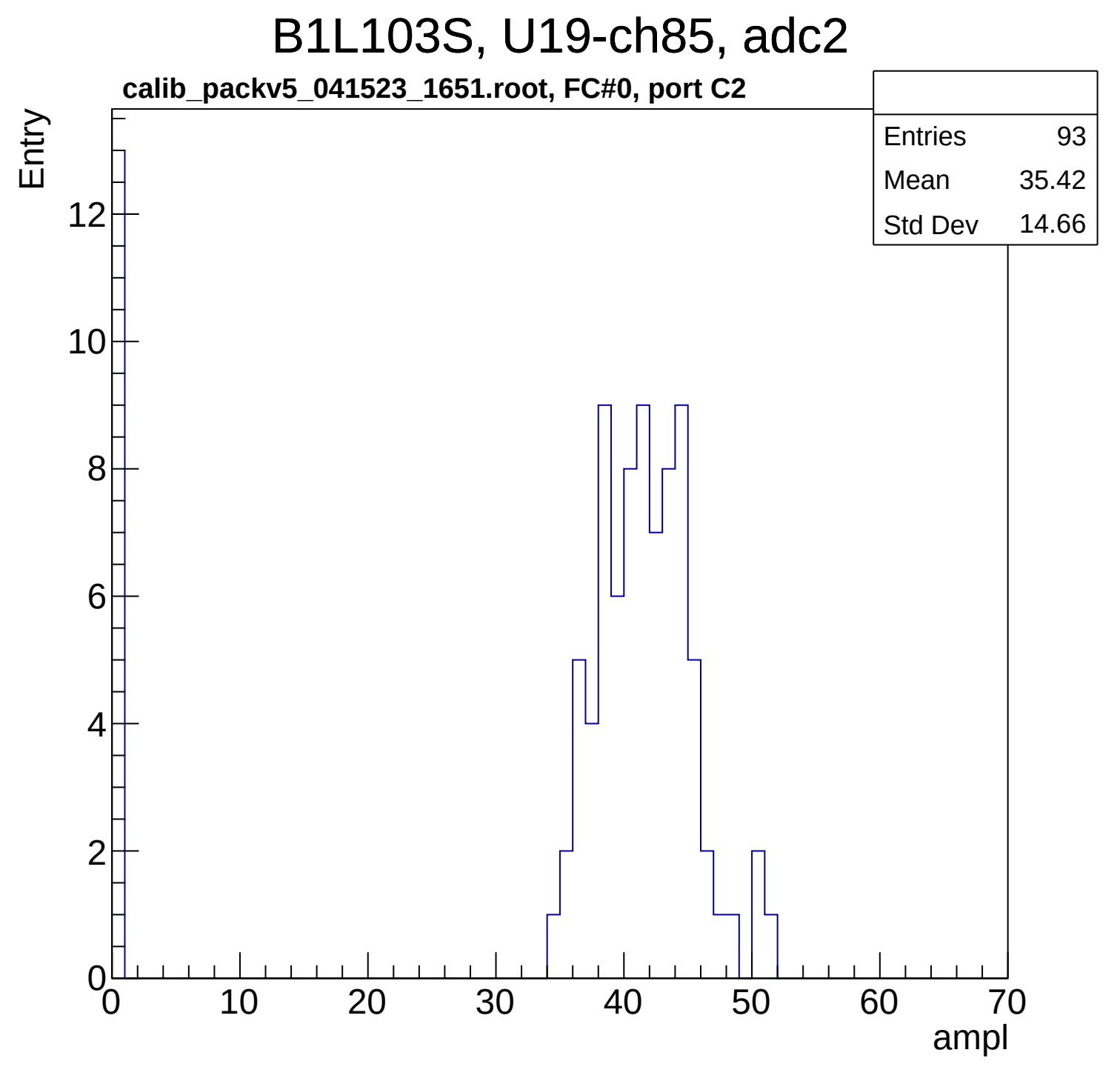
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70


B1L103S, U19-ch85, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 33.63
Std Dev 6.062
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch85, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 35.42
Std Dev 14.66
Entry
0
2
4
6
8
10
12
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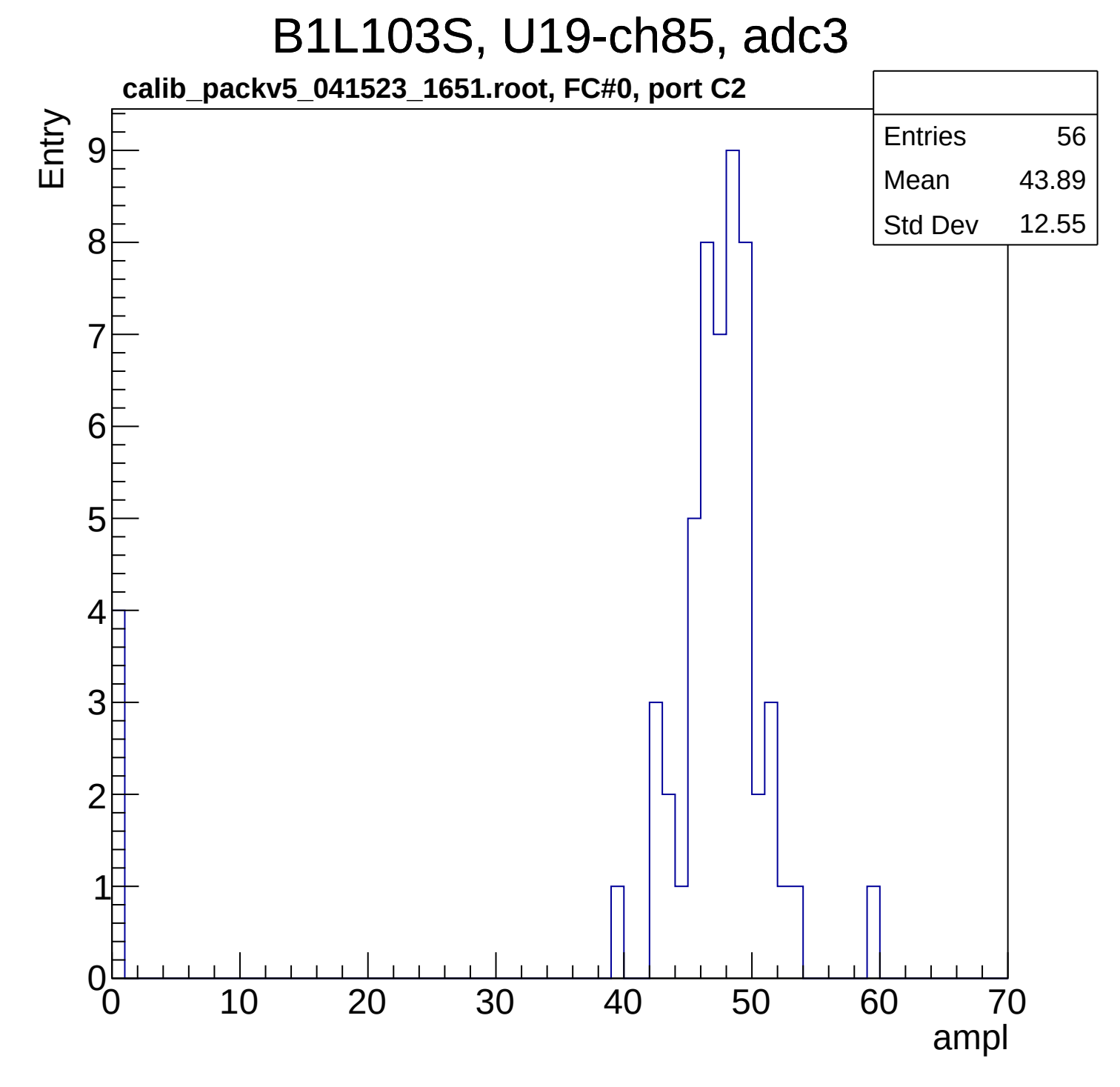
ampl


B1L103S, U19-ch85, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 43.89
Std Dev 12.55
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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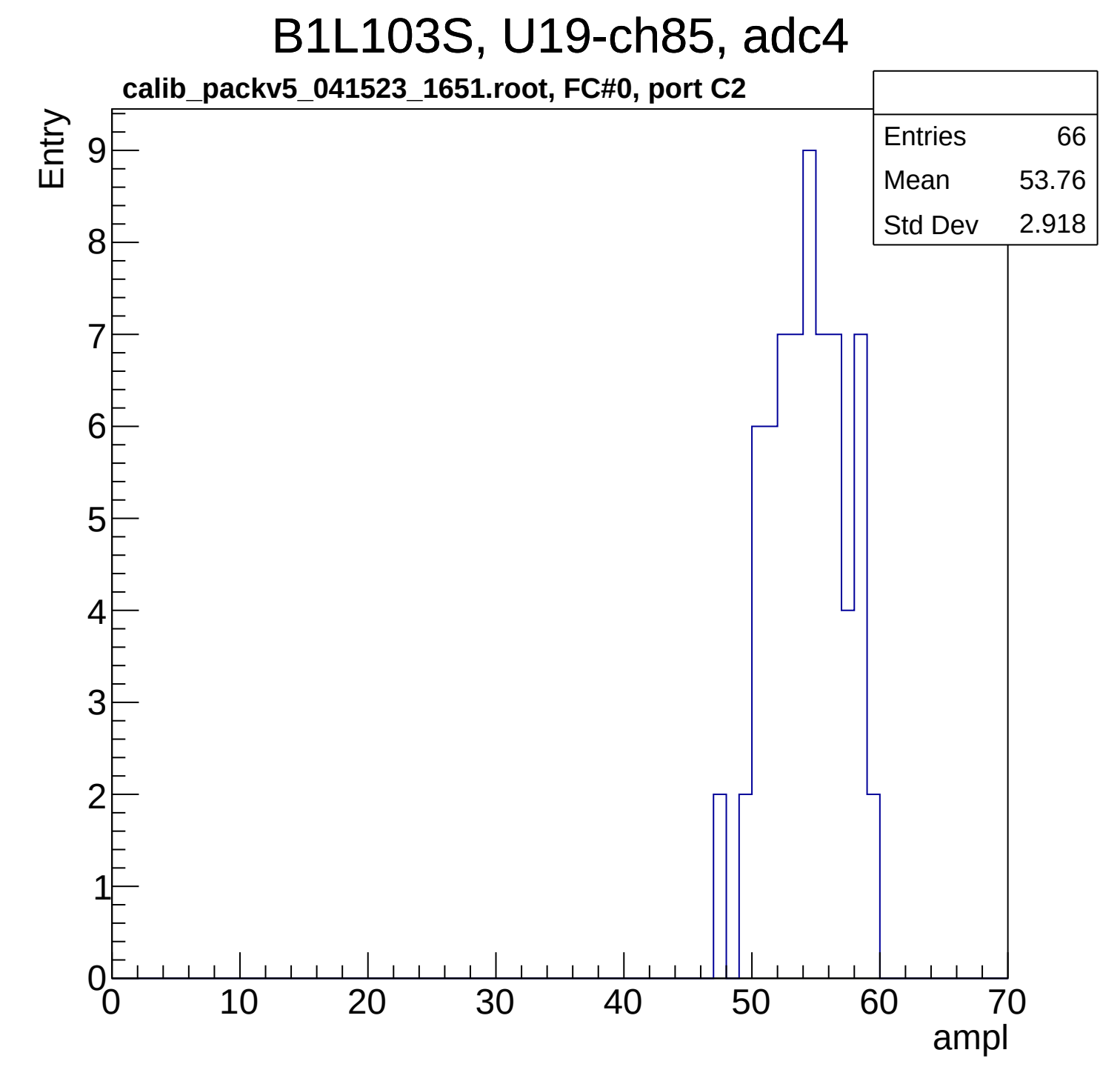
40
50
60
70


B1L103S, U19-ch85, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 53.76
Std Dev 2.918
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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60
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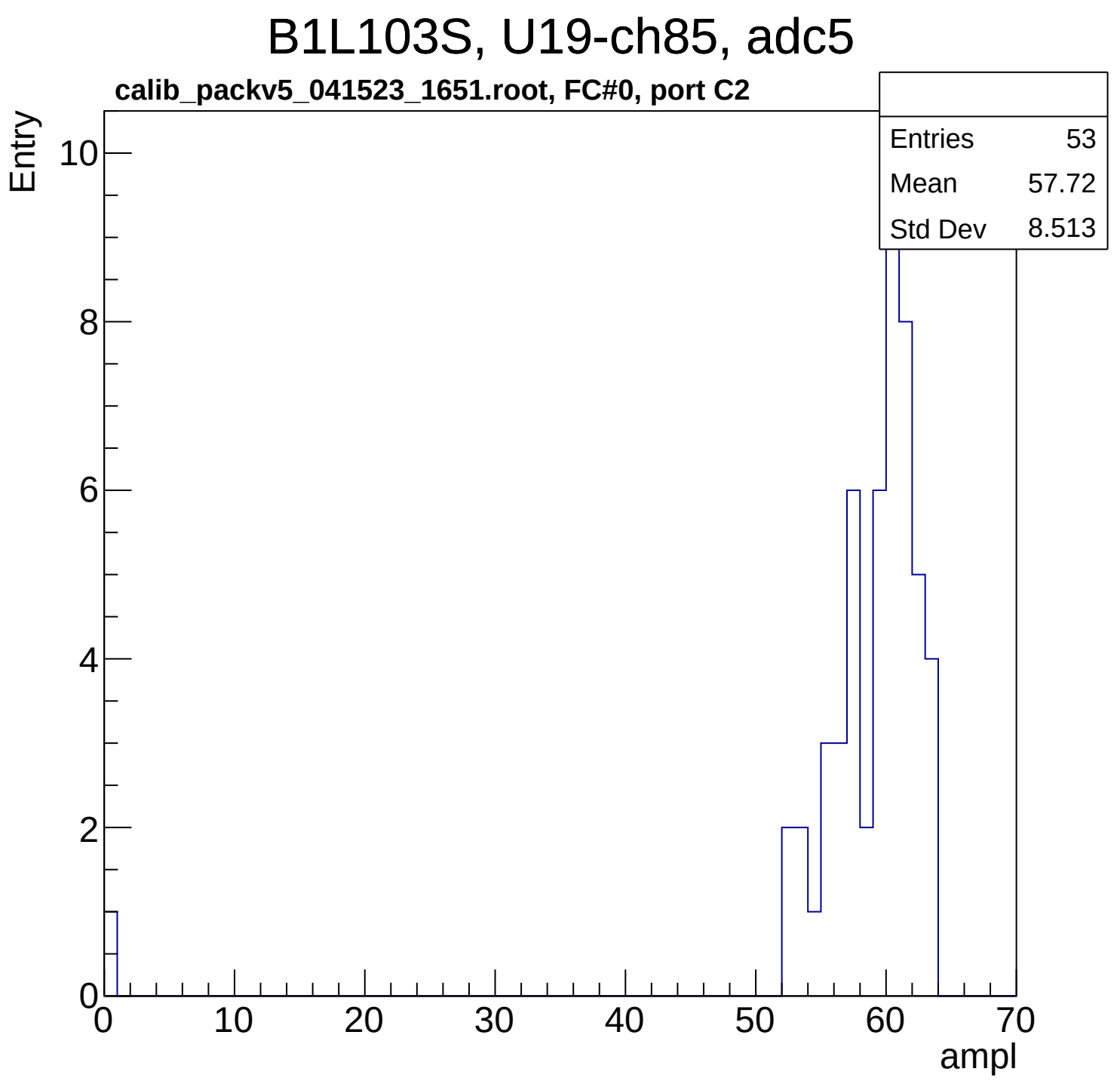
B1L103S, U19-ch85, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 57.72
Std Dev 8.513
Entry
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6
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10
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10
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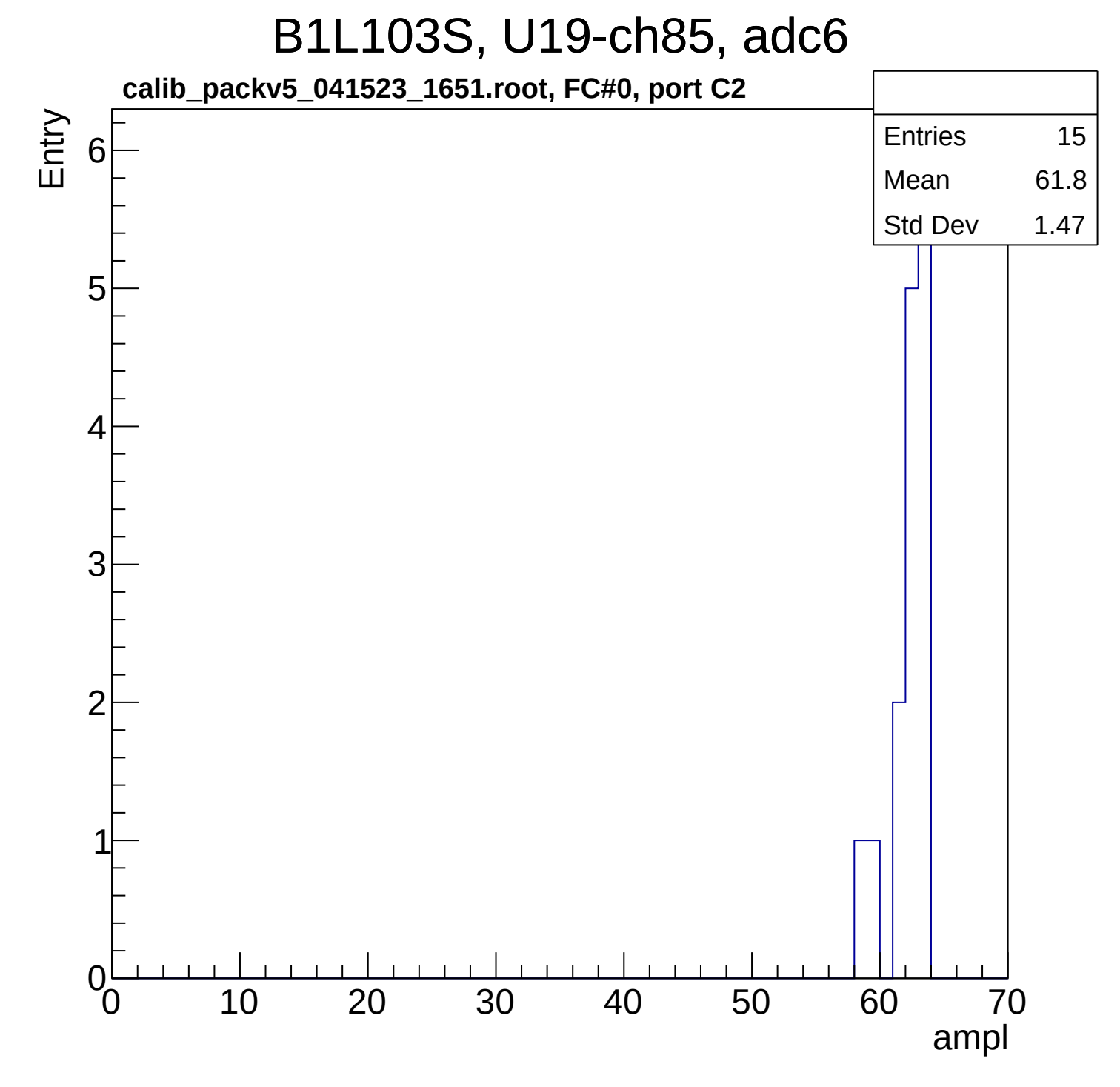
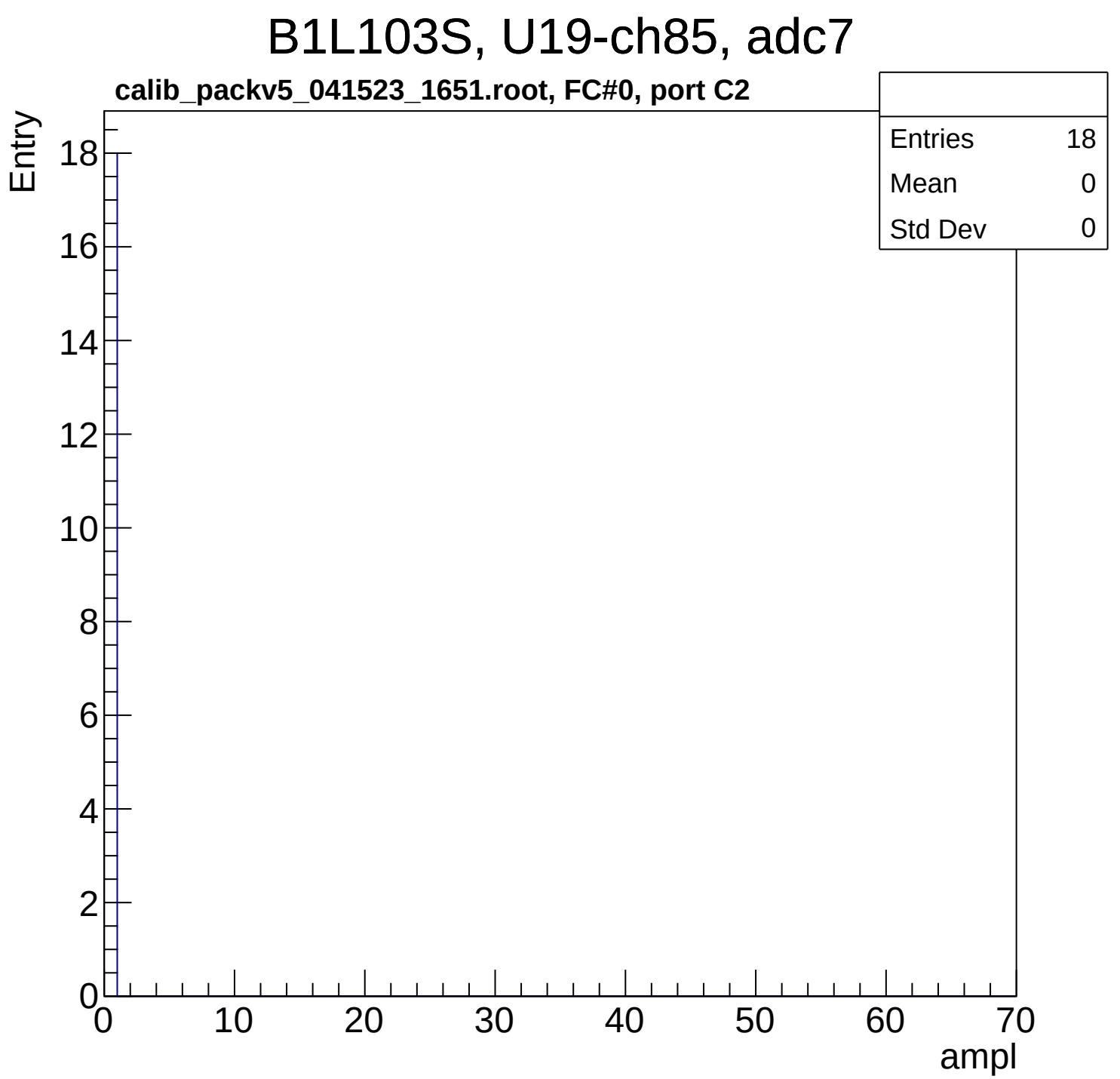
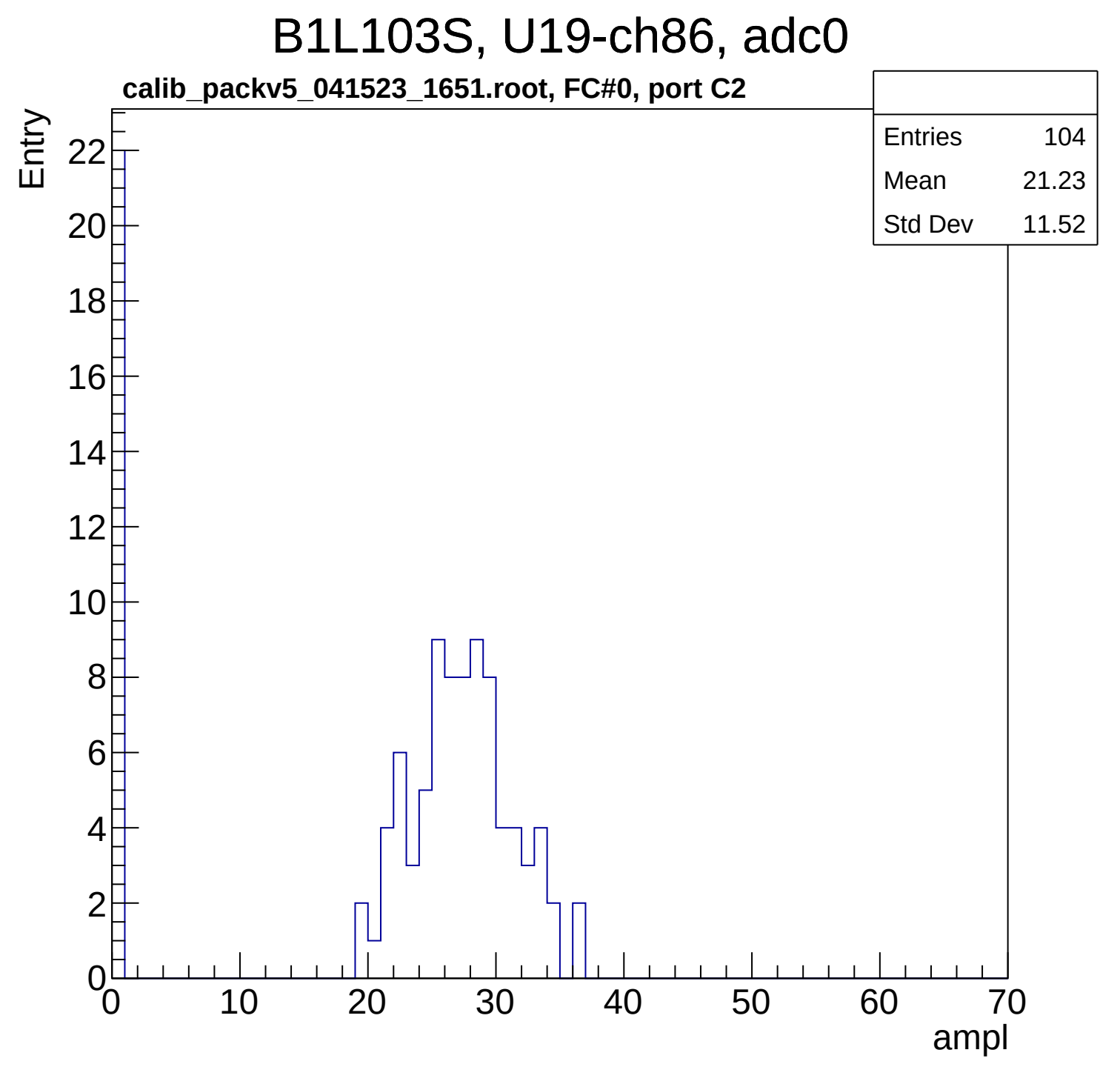
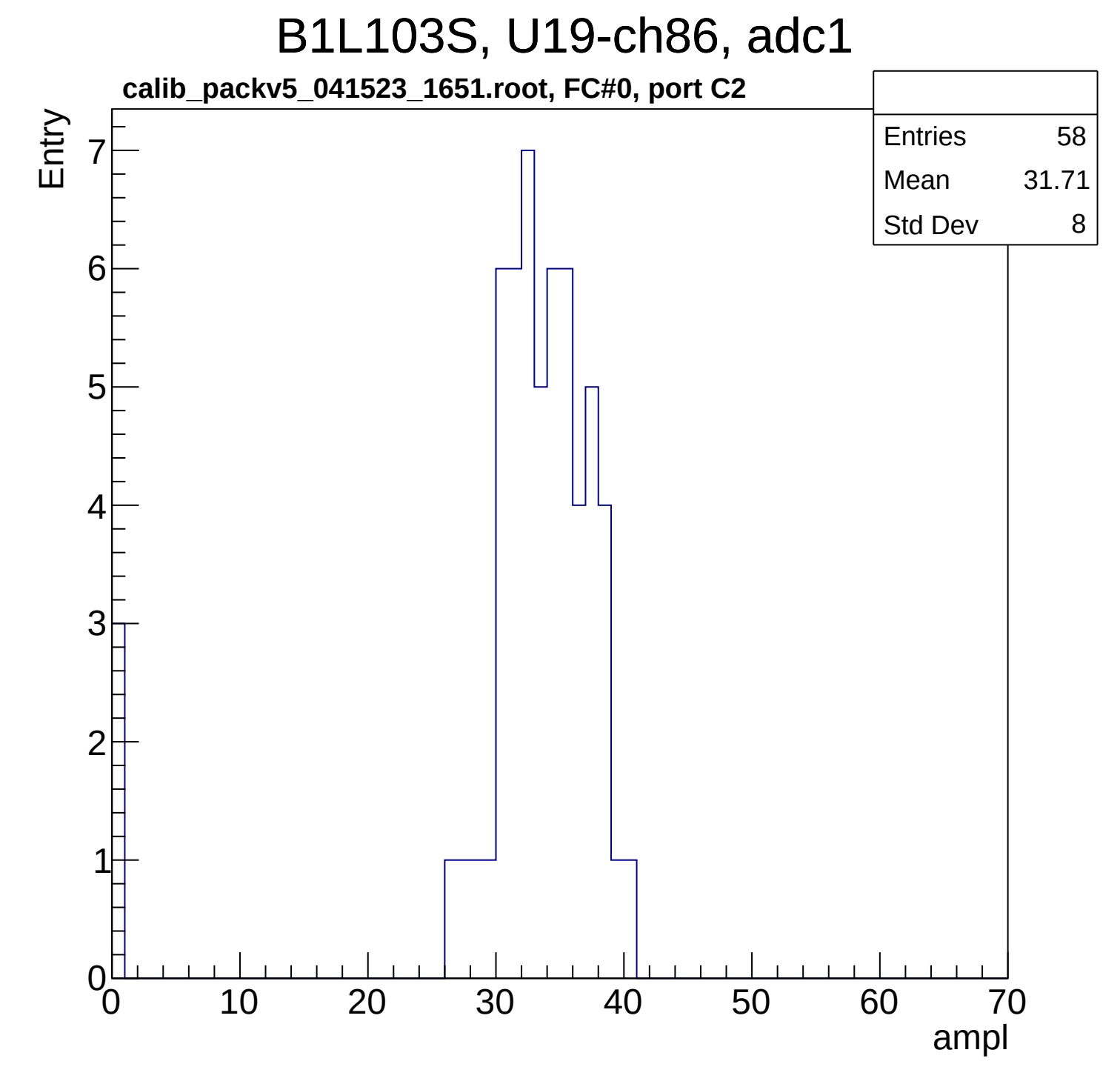
50
60
70
ampl


B1L103S, U19-ch85, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 61.8
Std Dev 1.47
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U19-ch85, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch86, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 104
Mean 21.23
Std Dev 11.52
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70


B1L103S, U19-ch86, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 31.71
Std Dev 8
Entry
ampl
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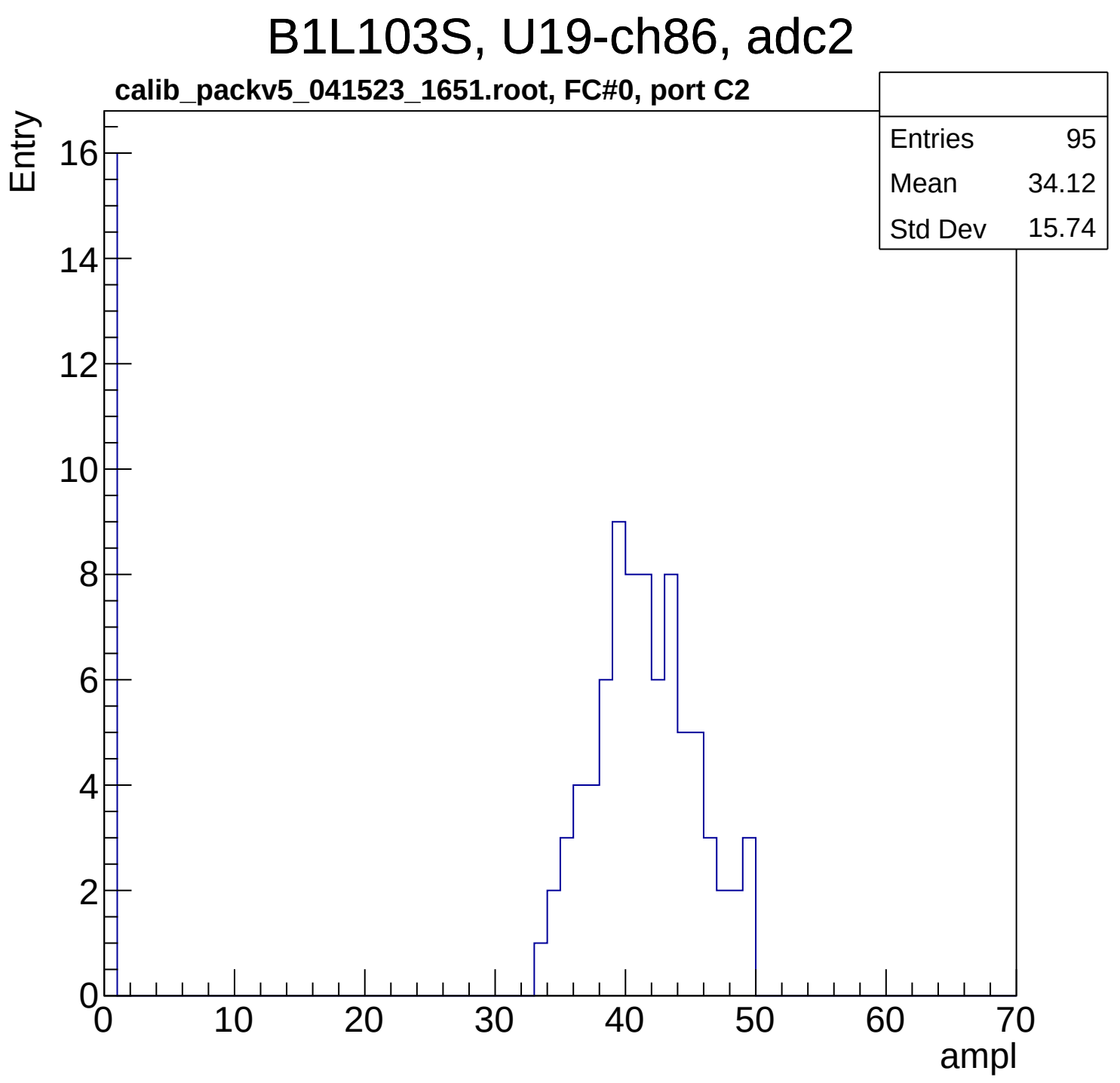
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch86, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 34.12
Std Dev 15.74
Entry
ampl
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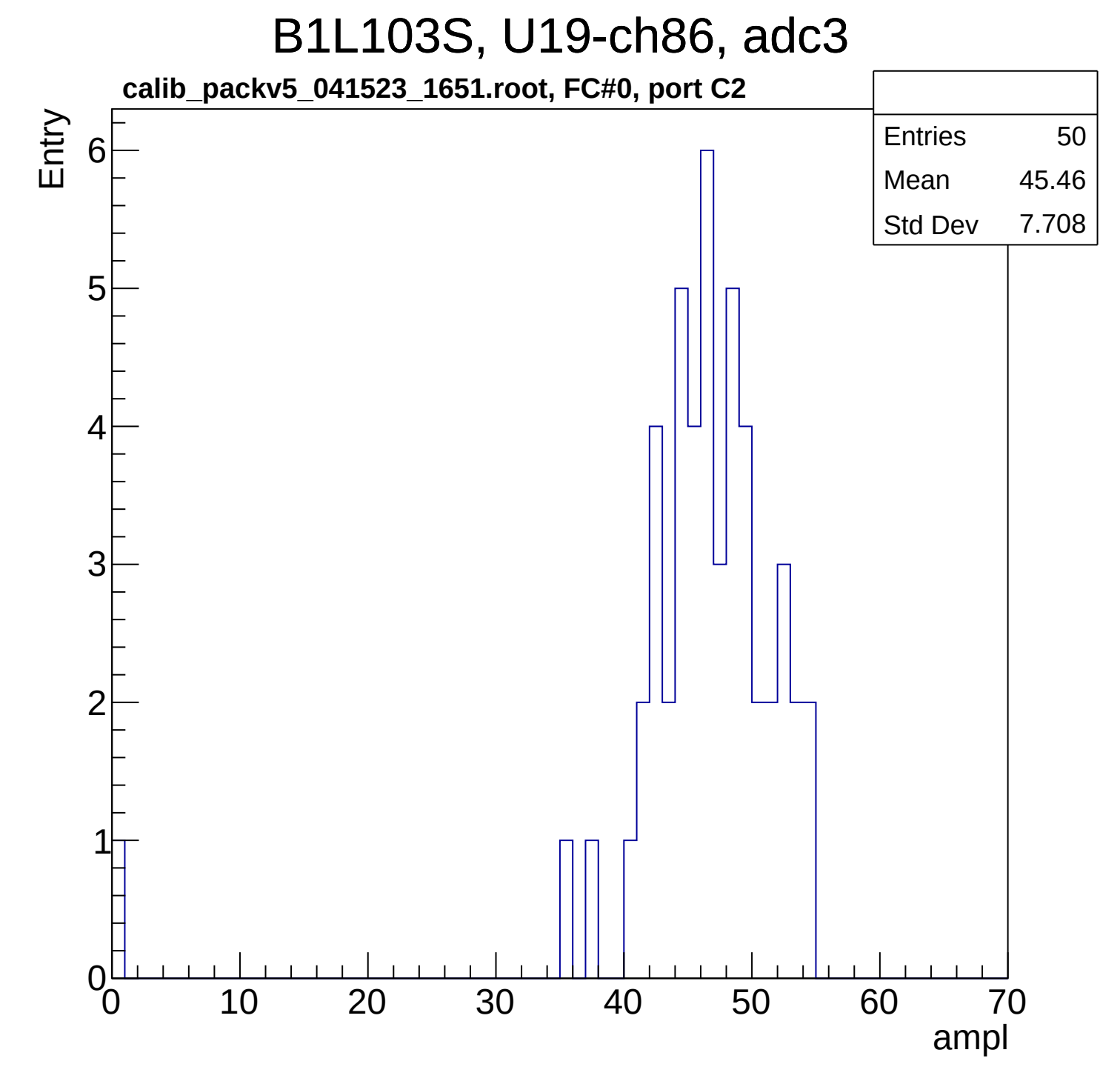
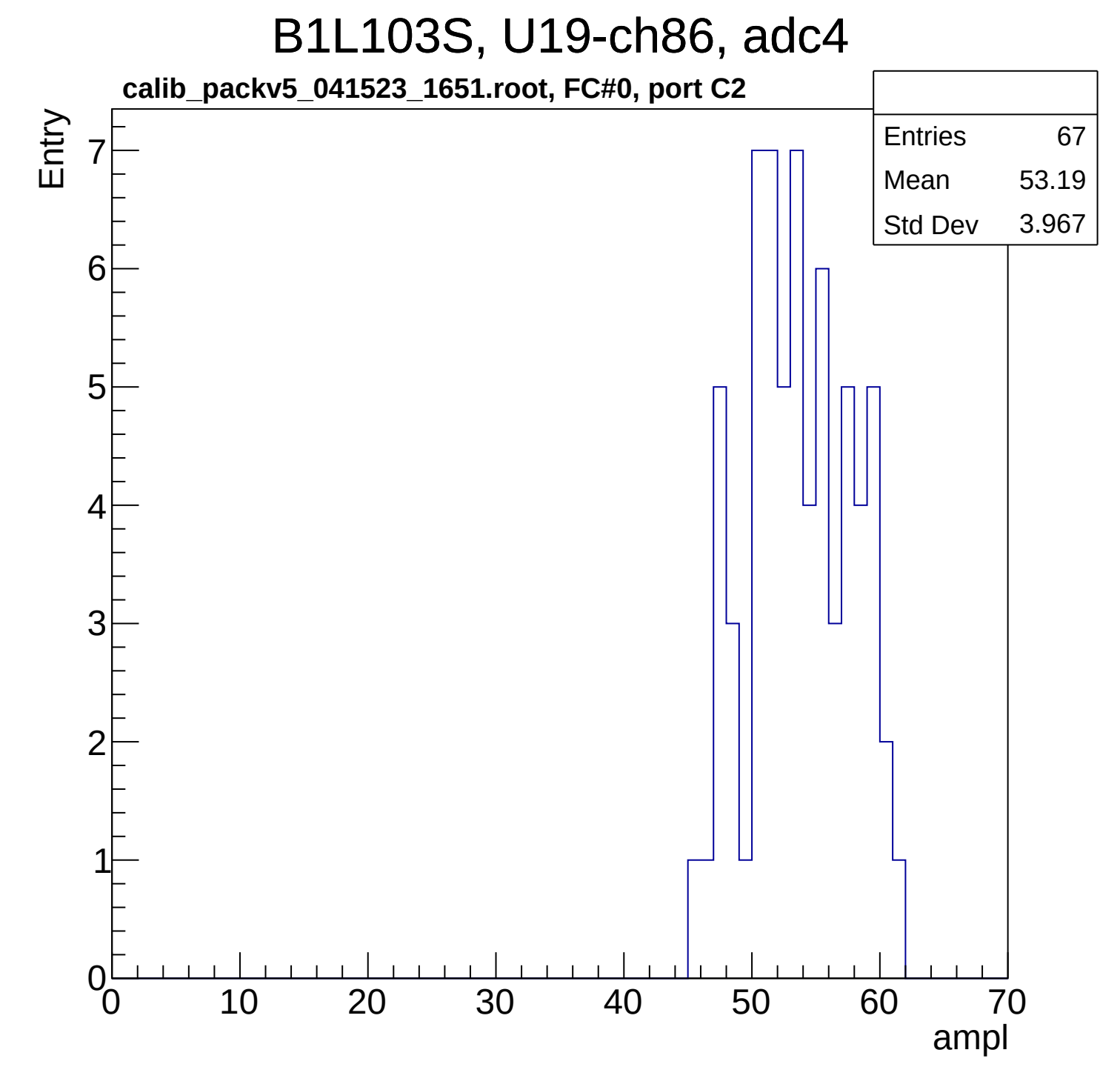
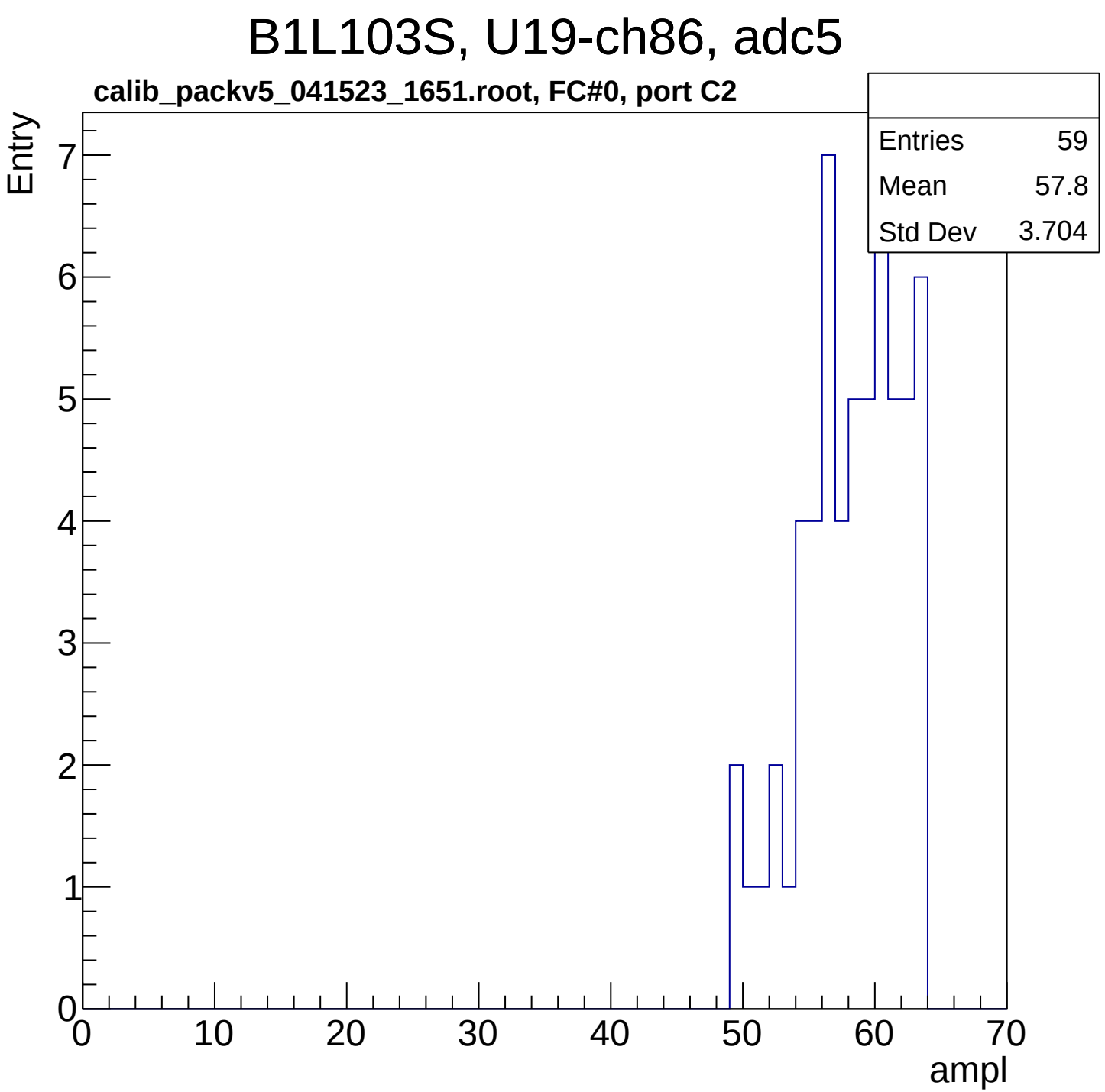
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L103S, U19-ch86, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 45.46
Std Dev 7.708
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U19-ch86, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 53.19
Std Dev 3.967
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch86, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 57.8
Std Dev 3.704
Entry
ampl
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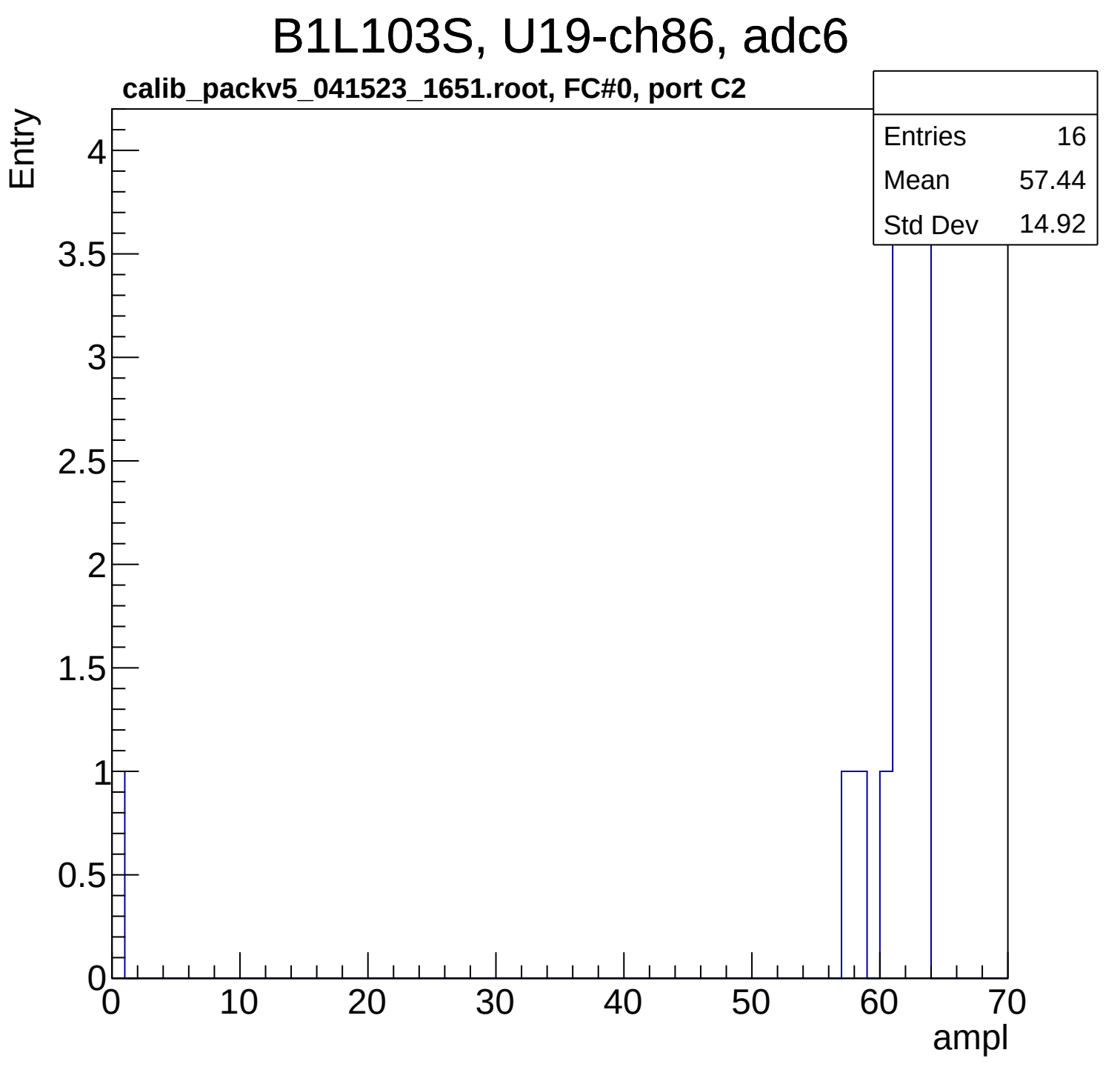
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch86, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 57.44
Std Dev 14.92
Entry
ampl
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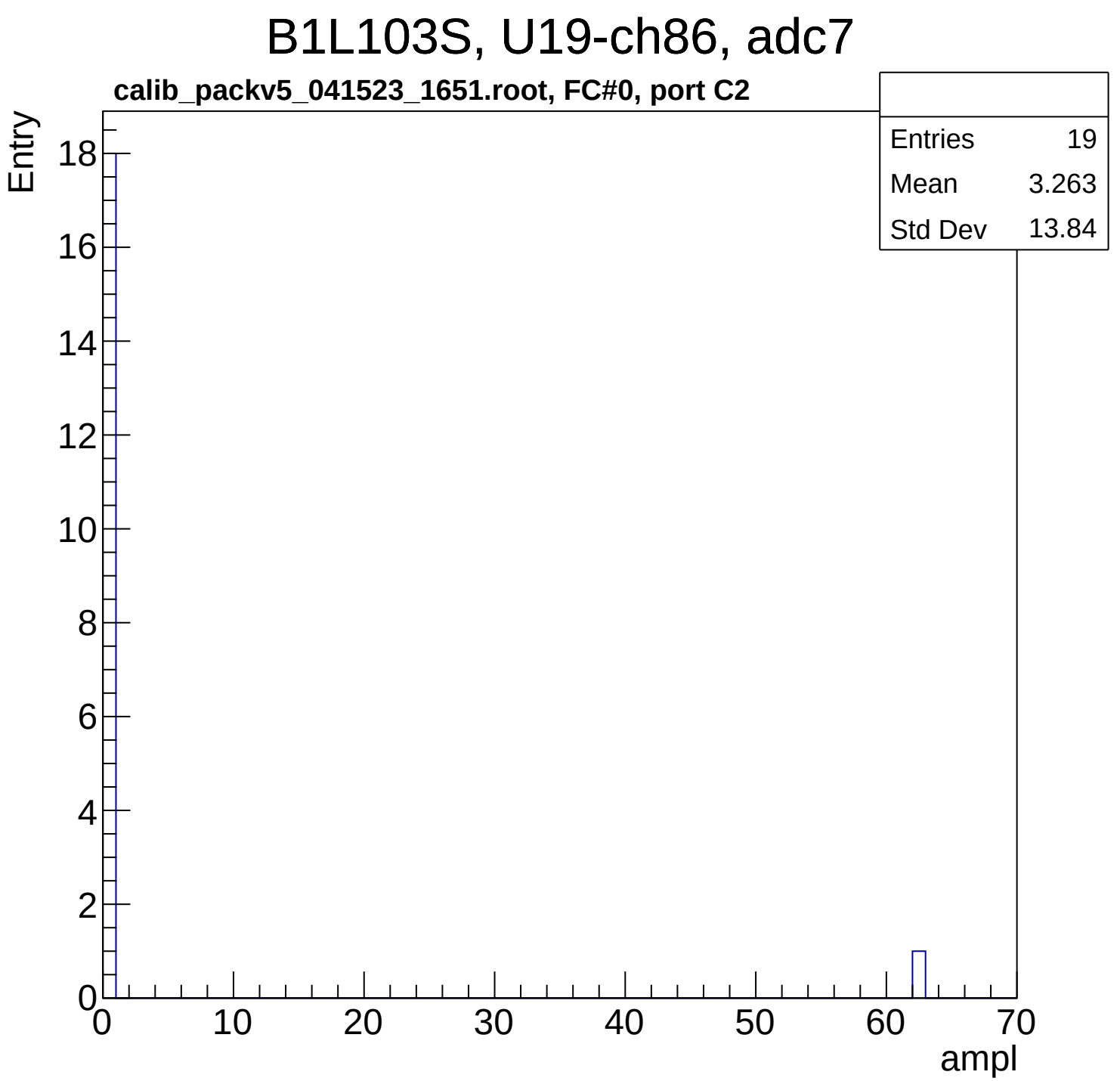
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U19-ch86, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.263
Std Dev 13.84
Entry
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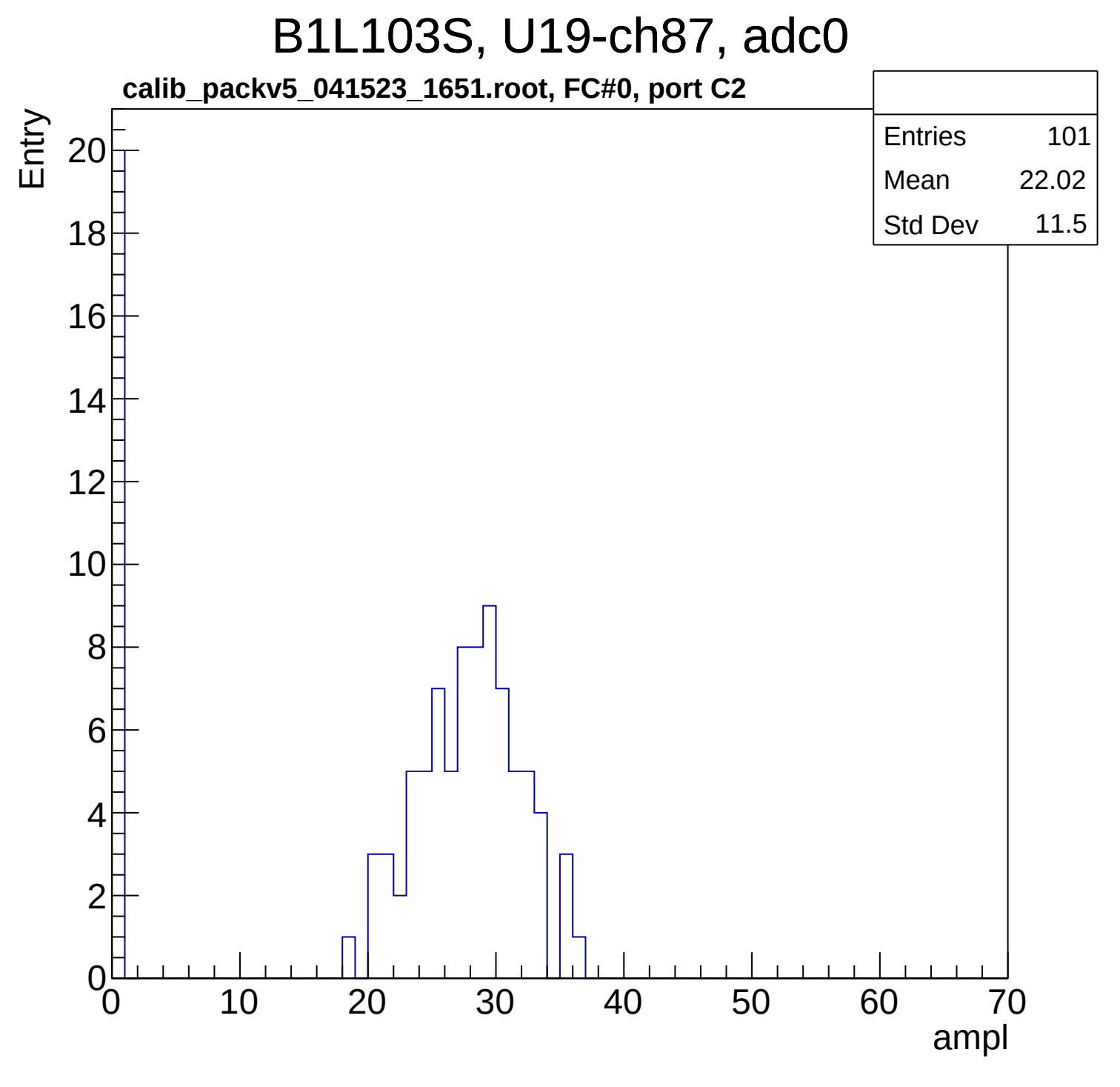
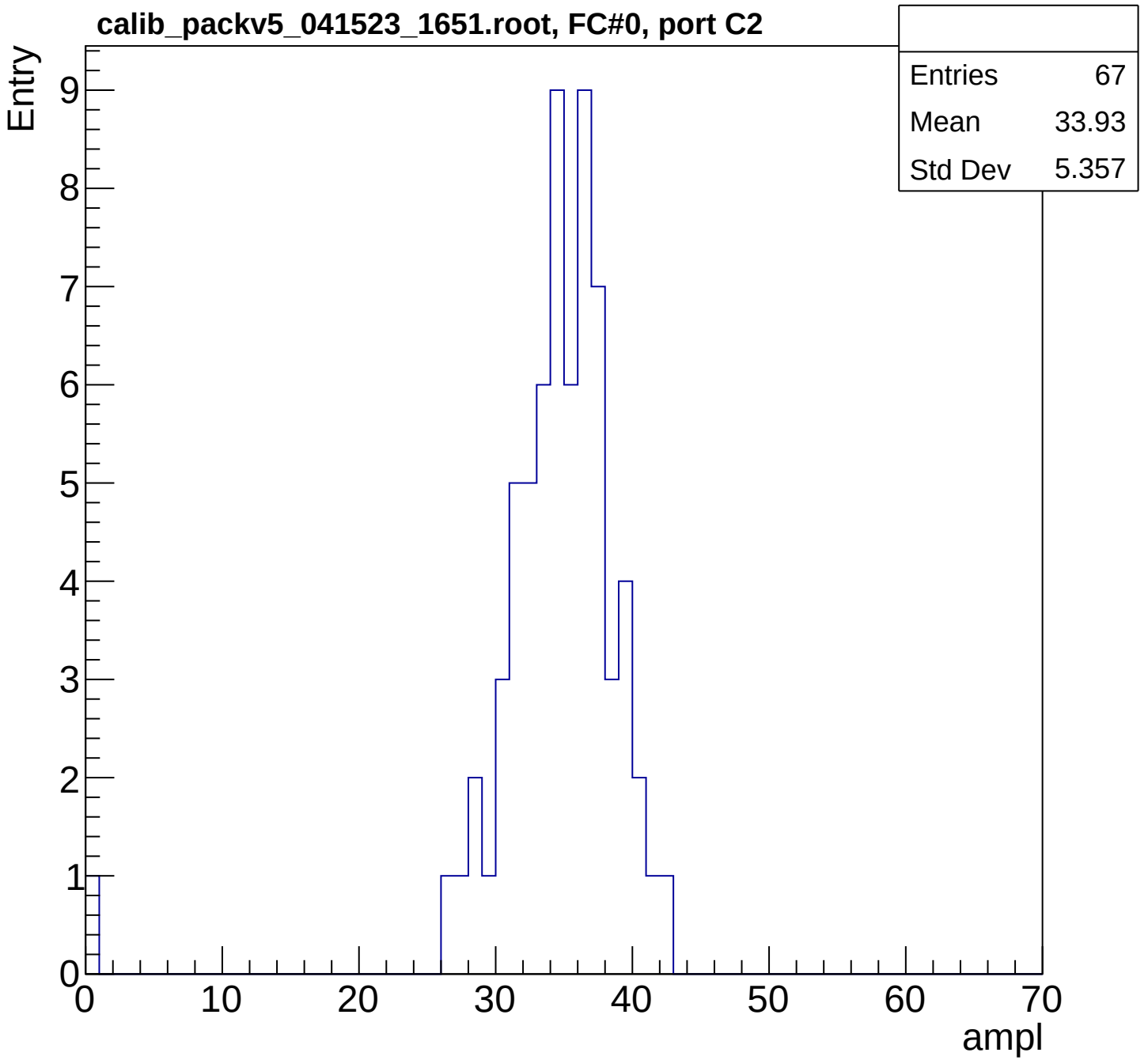
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch87, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 101
Mean 22.02
Std Dev 11.5
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70


B1L103S, U19-ch87, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 33.93
Std Dev 5.357
Entry
ampl
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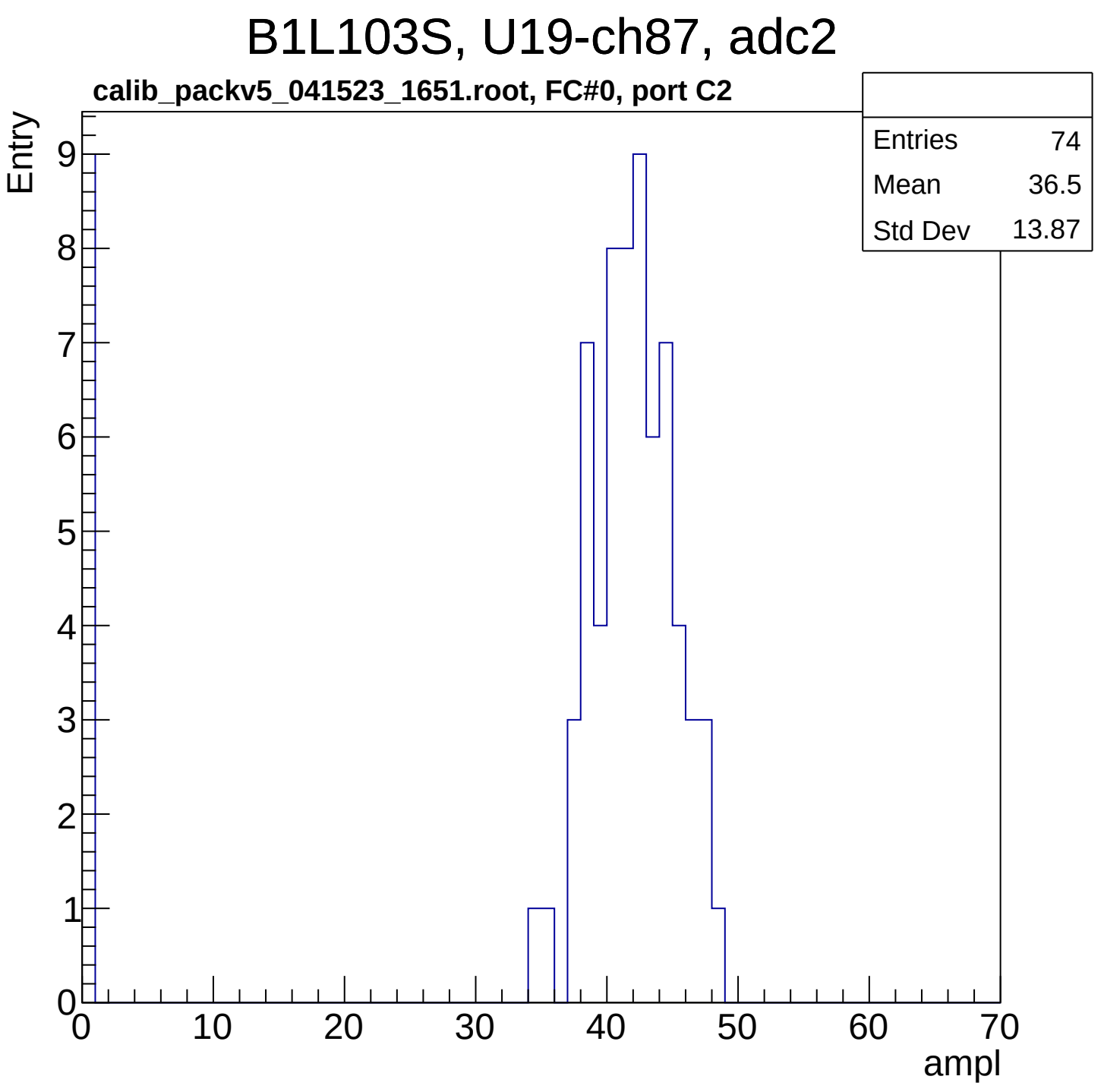
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch87, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 36.5
Std Dev 13.87
Entry
ampl
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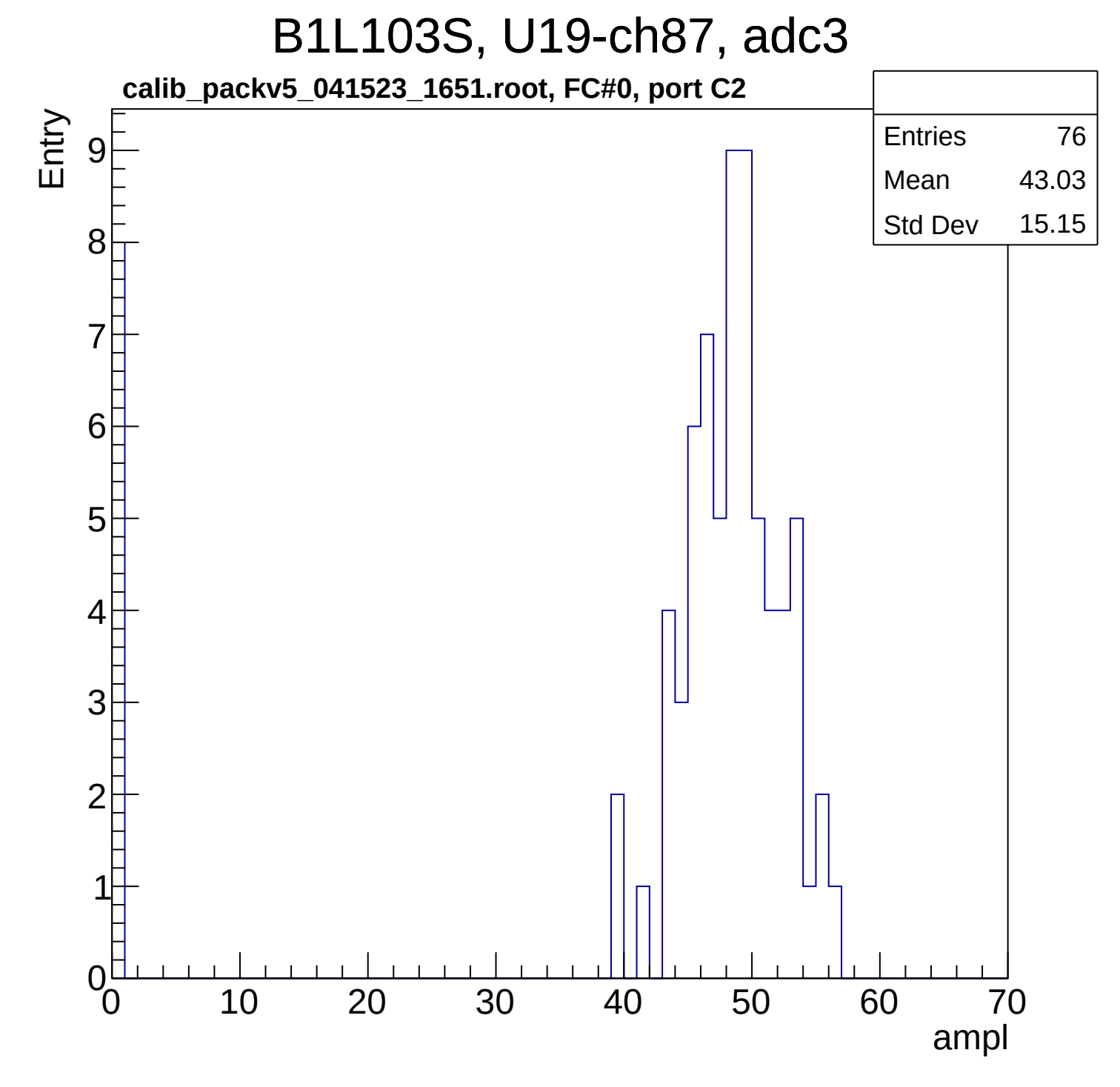
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch87, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 43.03
Std Dev 15.15
Entry
ampl
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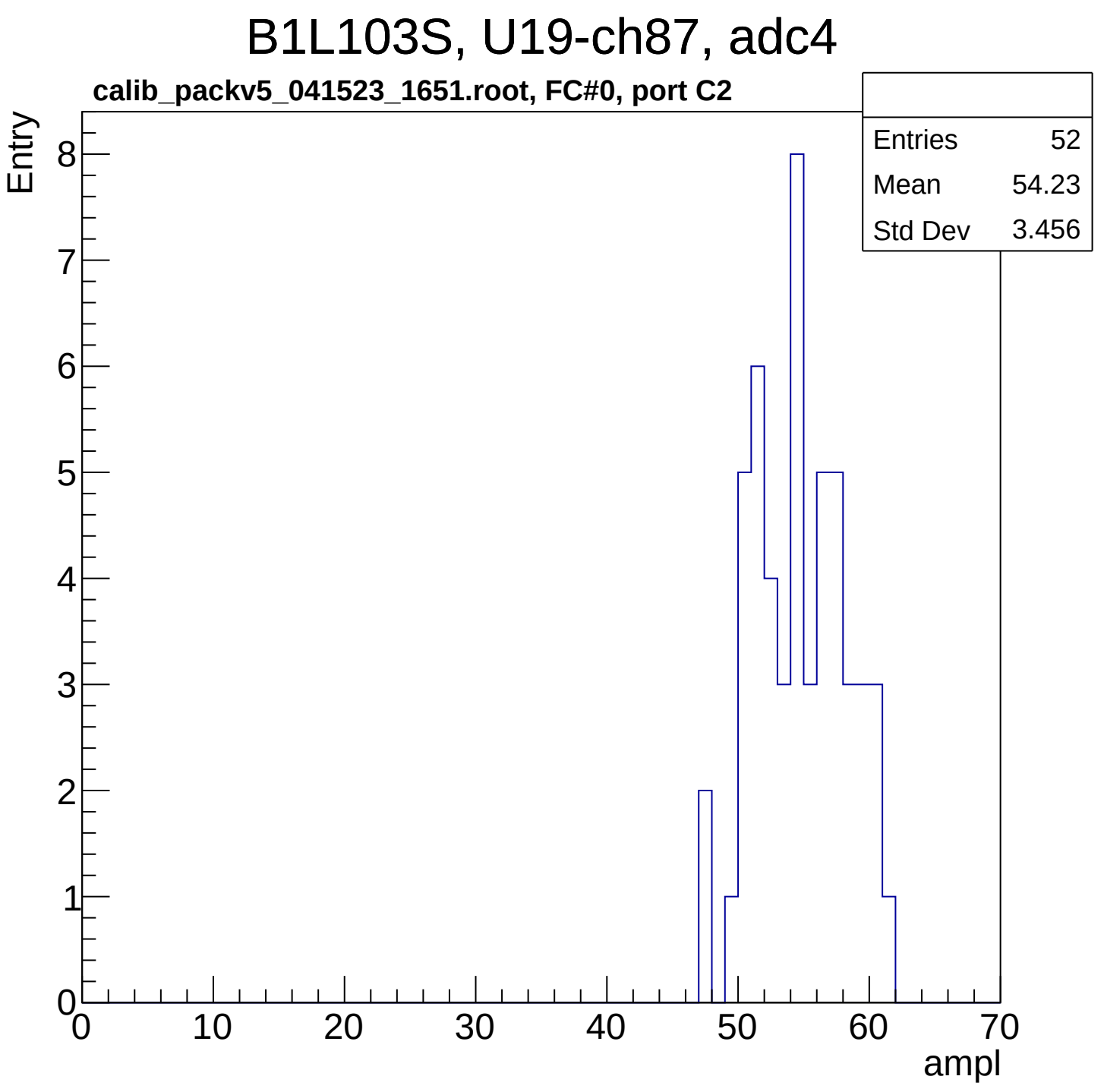
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch87, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 54.23
Std Dev 3.456
Entry
ampl
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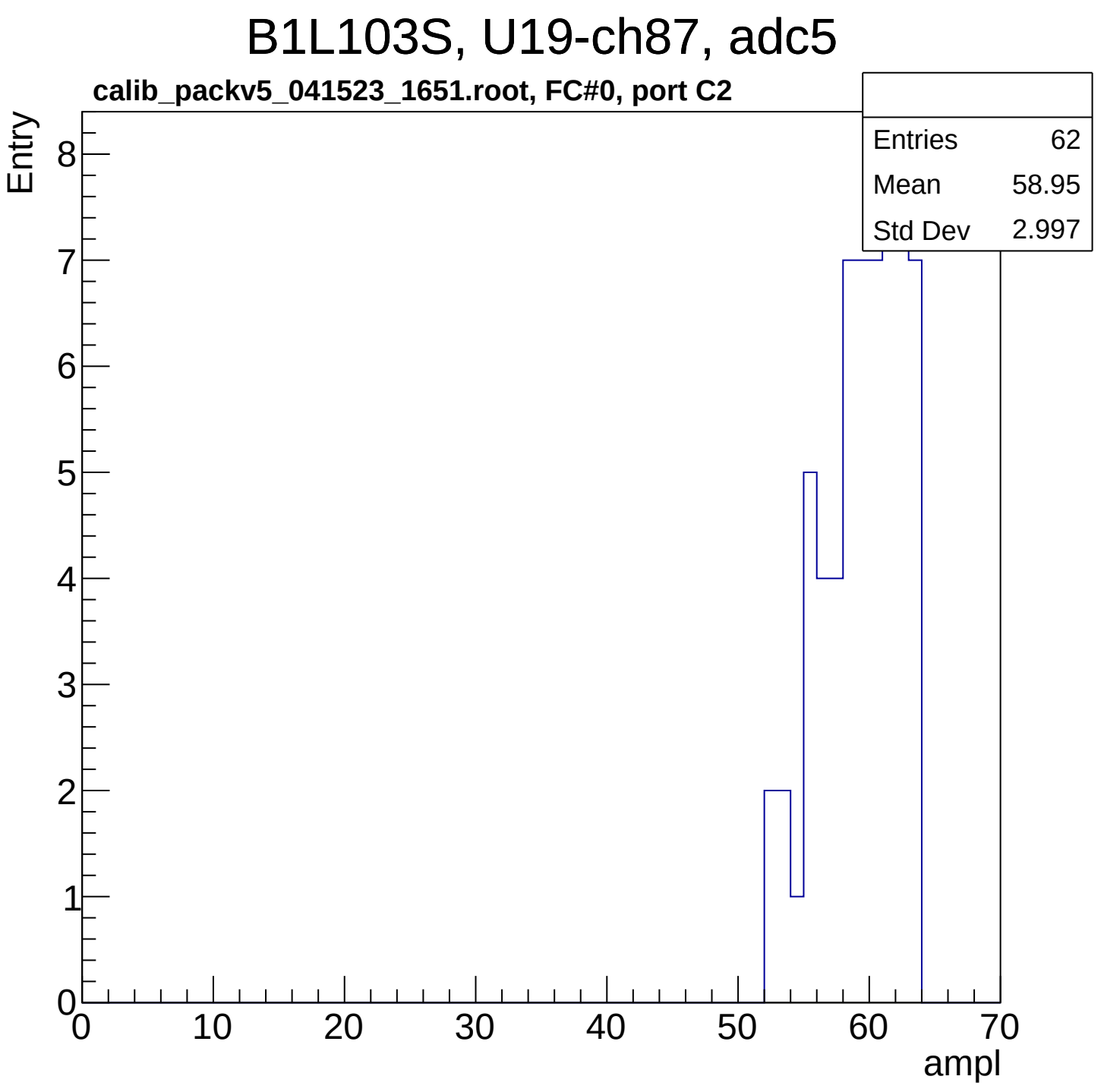
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch87, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 58.95
Std Dev 2.997
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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60
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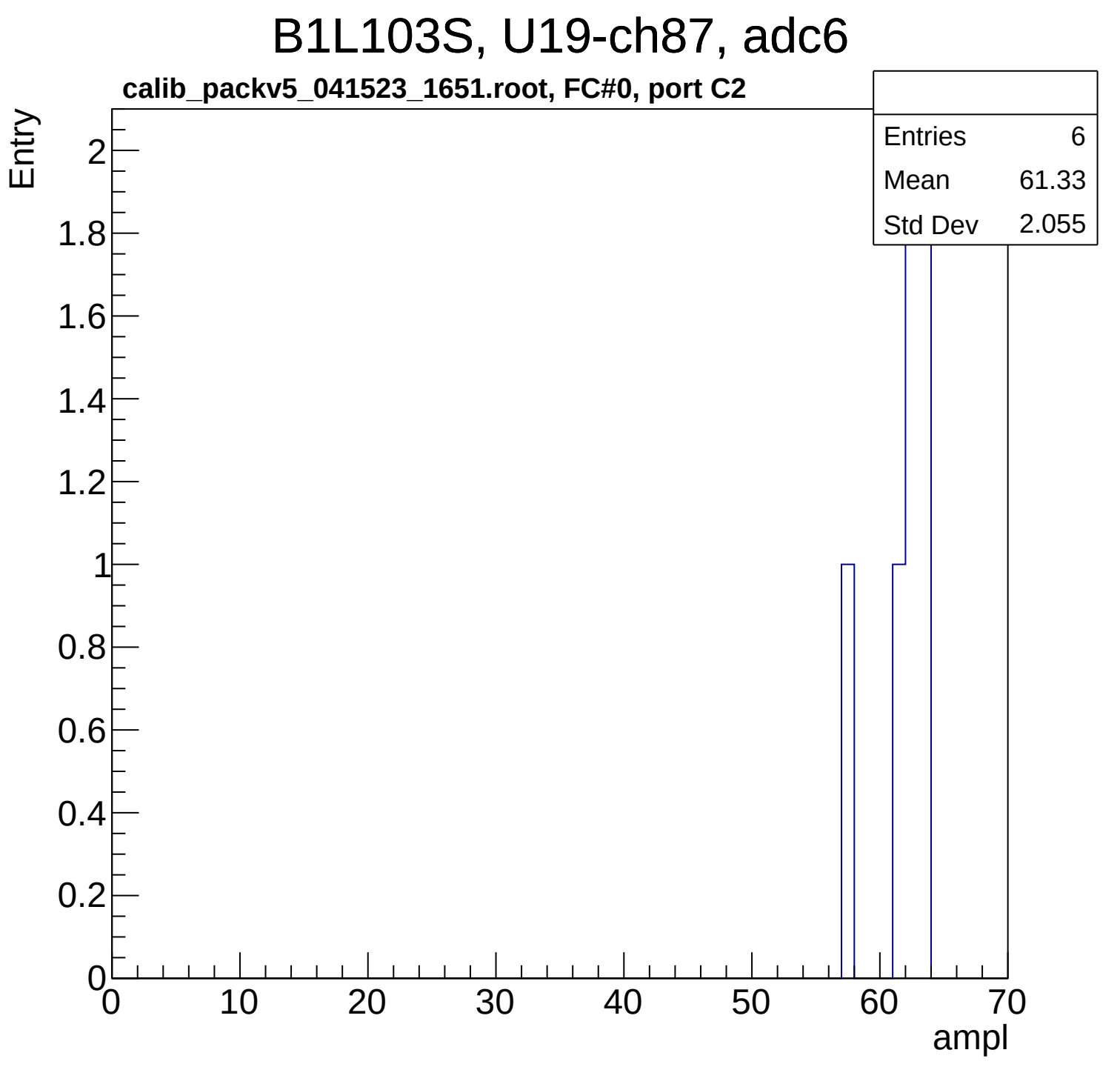
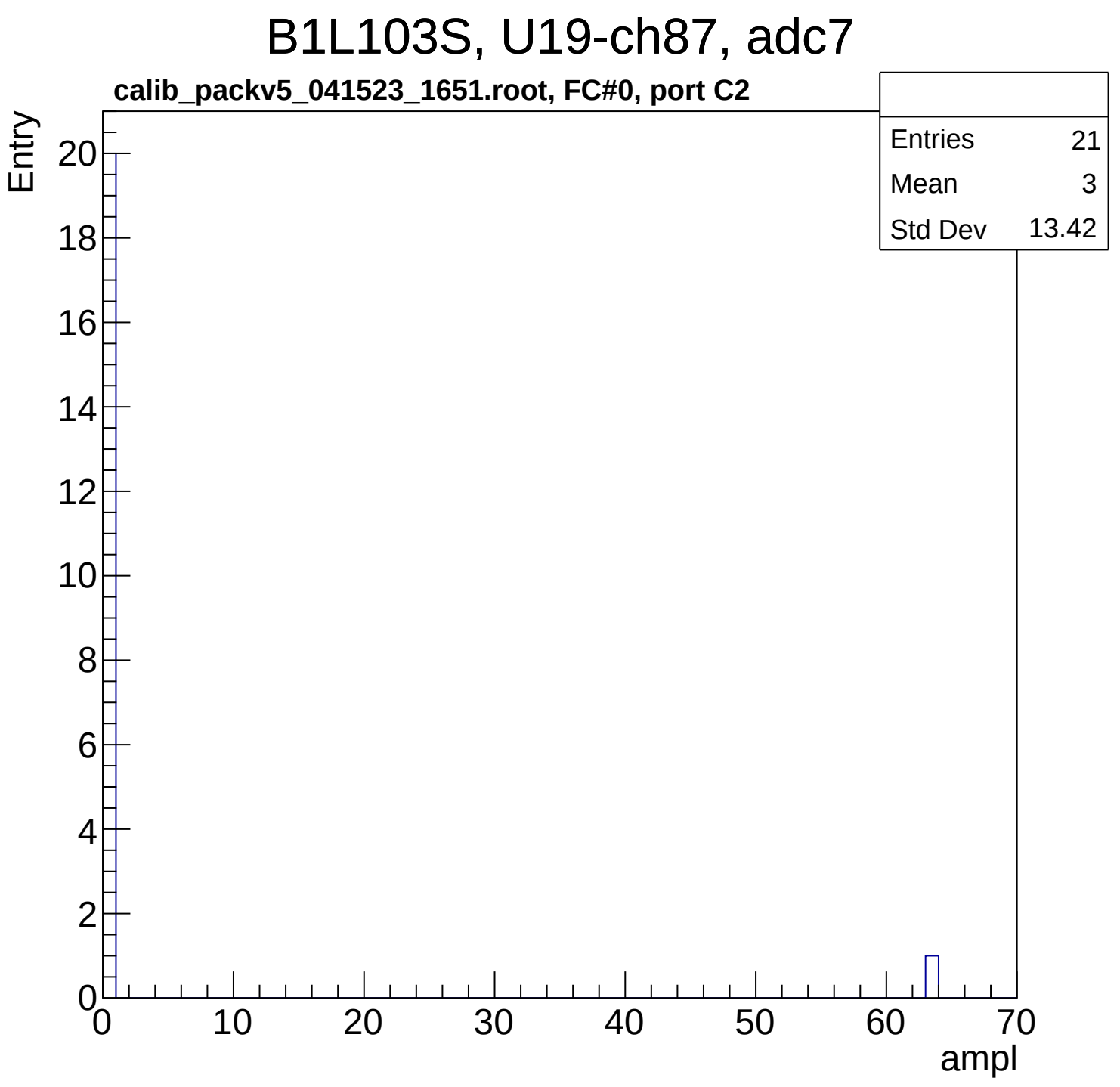
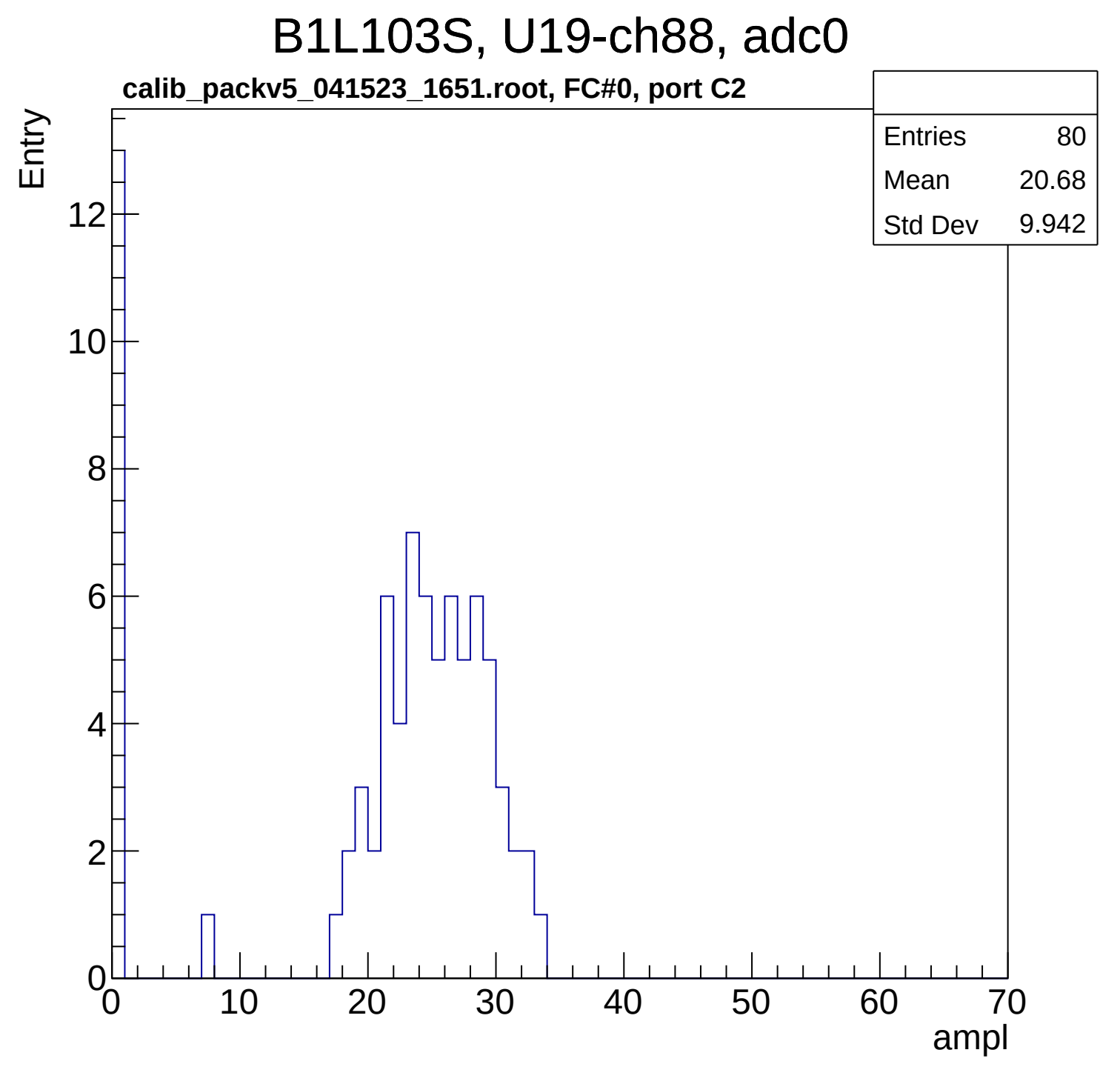
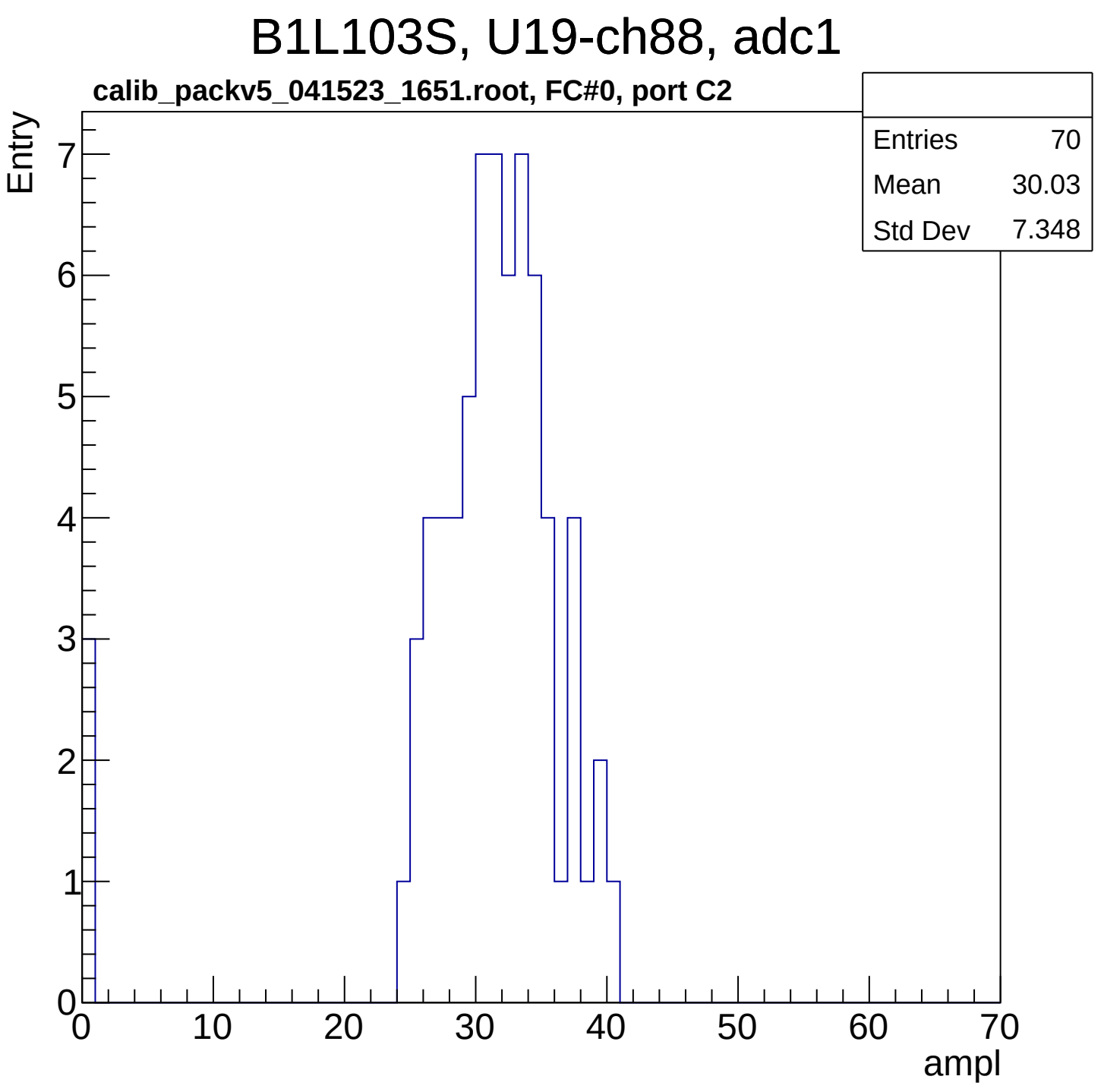
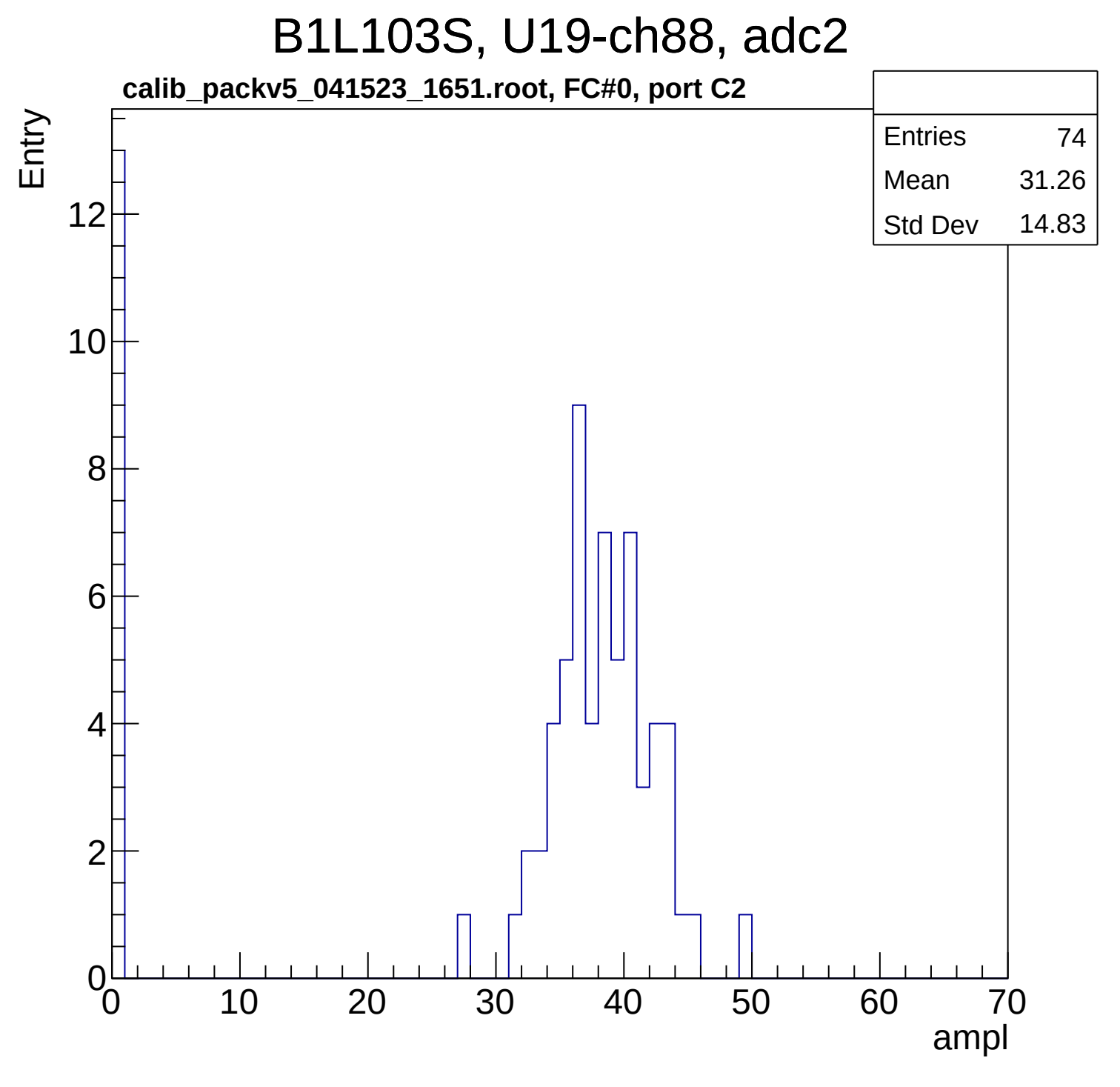
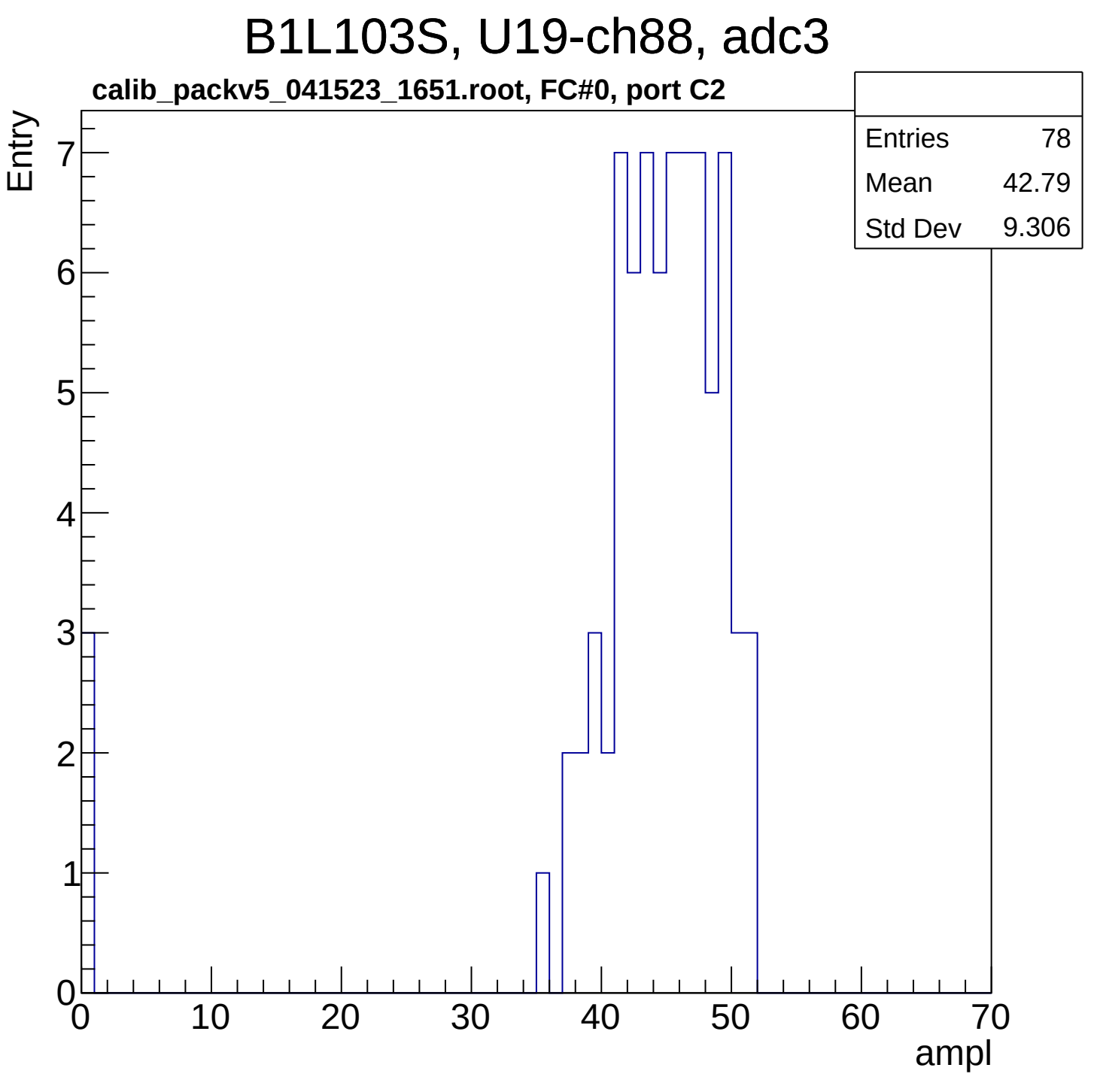

B1L103S, U19-ch87, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 61.33
Std Dev 2.055
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

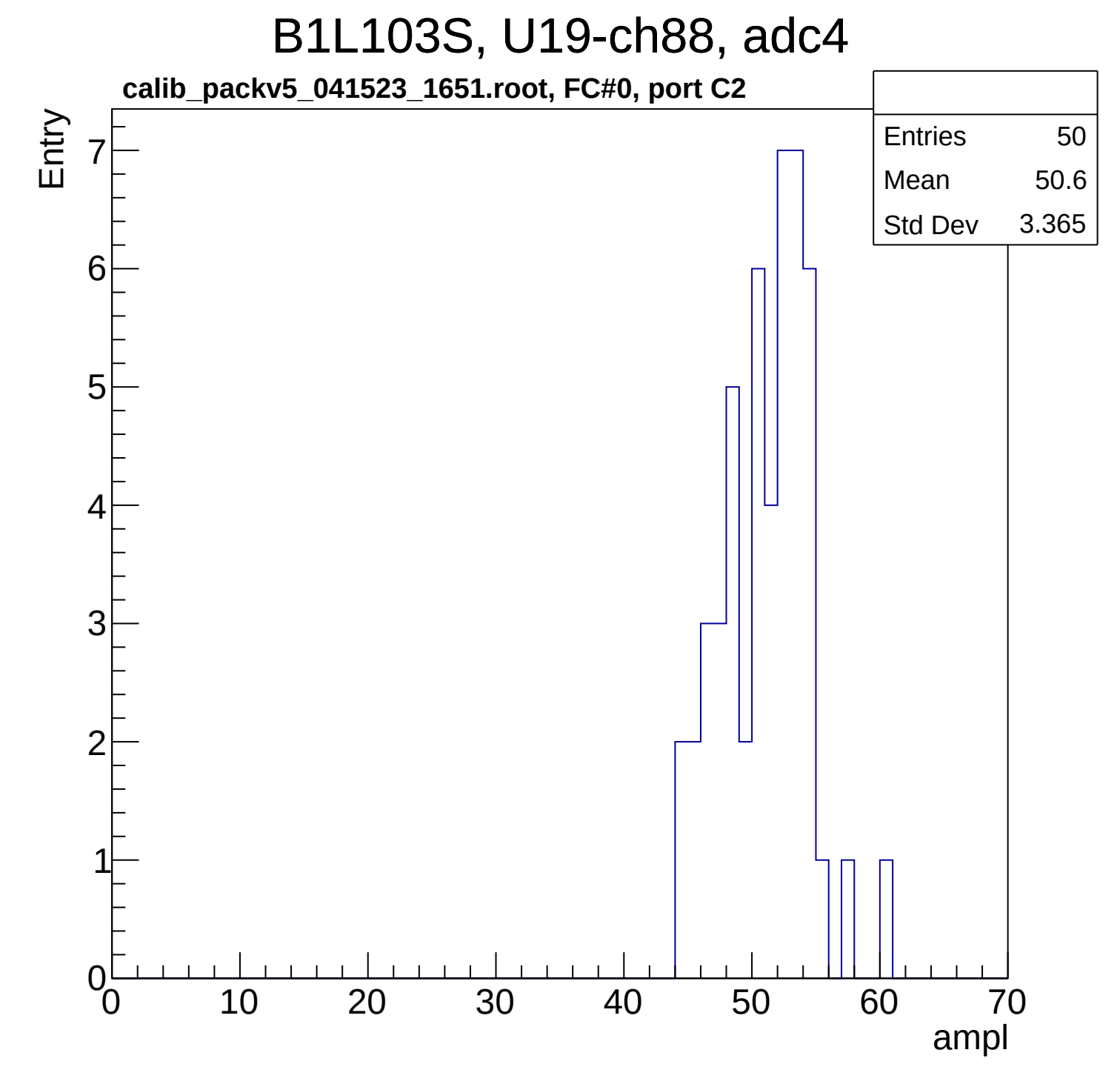

B1L103S, U19-ch87, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 3
Std Dev 13.42
Entry
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70
ampl

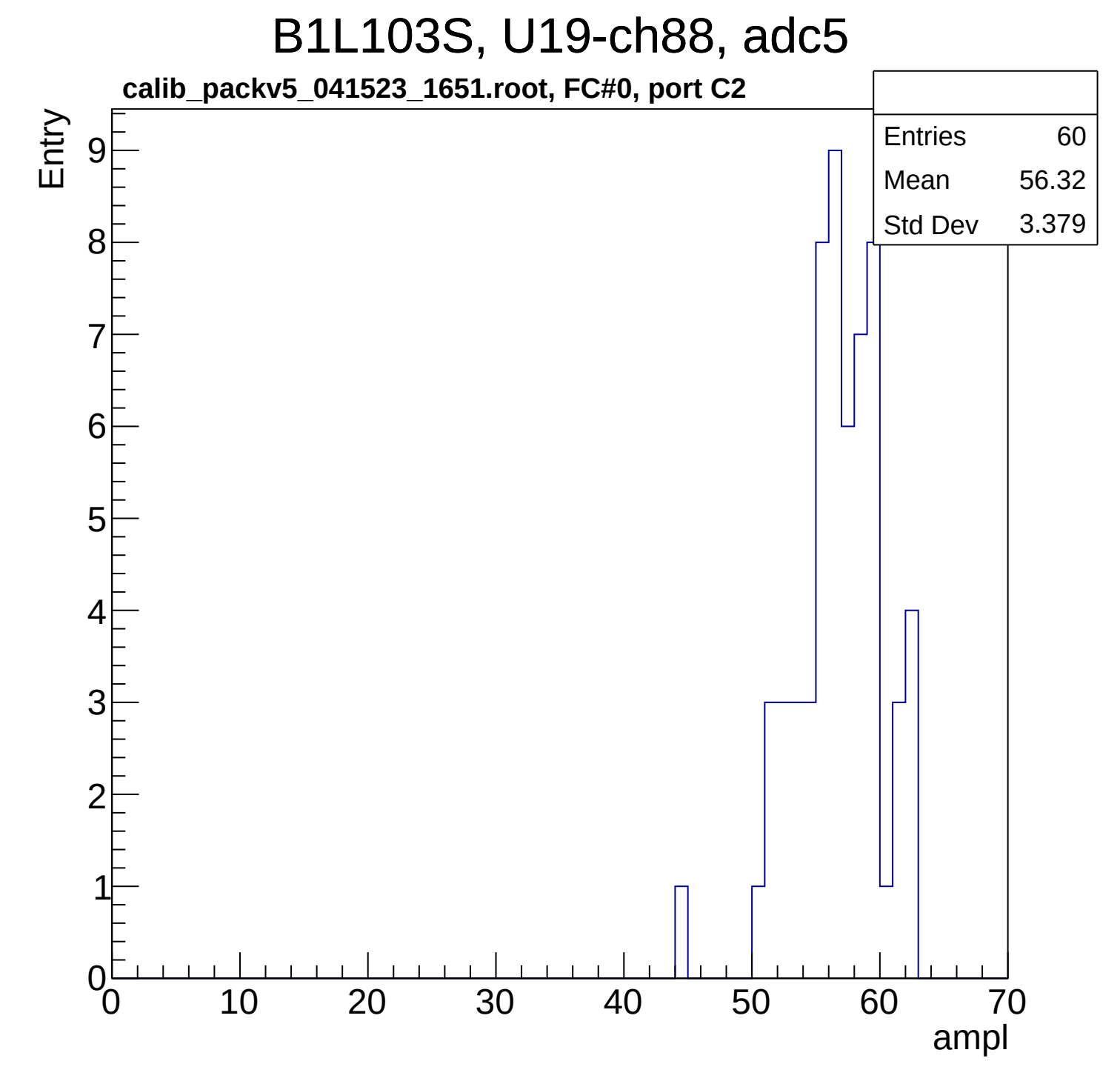

B1L103S, U19-ch88, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 20.68
Std Dev 9.942
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U19-ch88, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 30.03
Std Dev 7.348
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch88, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 31.26
Std Dev 14.83
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch88, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 42.79
Std Dev 9.306
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch88, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 50.6
Std Dev 3.365
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch88, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 56.32
Std Dev 3.379
Entry
ampl
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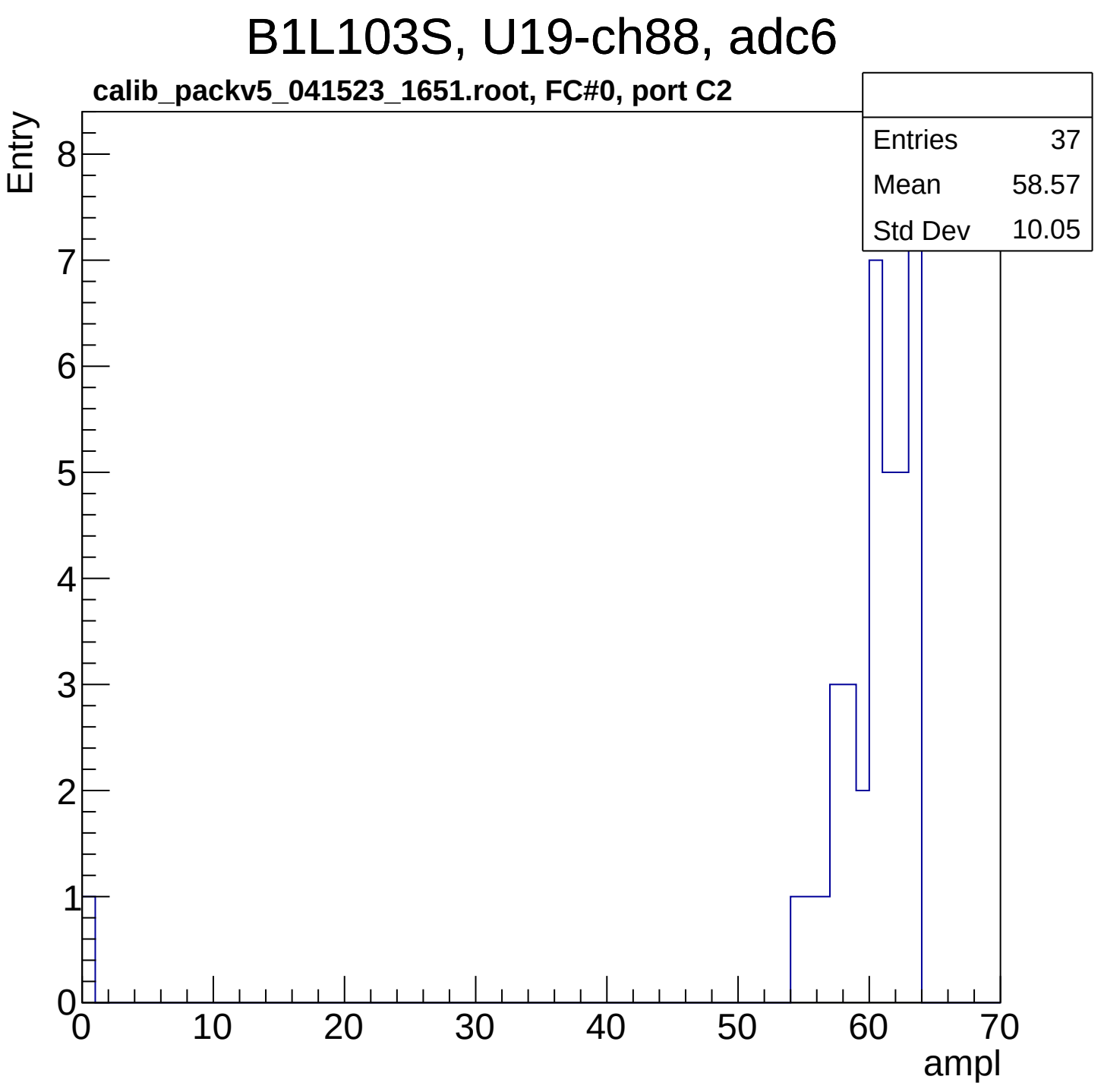
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch88, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 58.57
Std Dev 10.05
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
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40
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60
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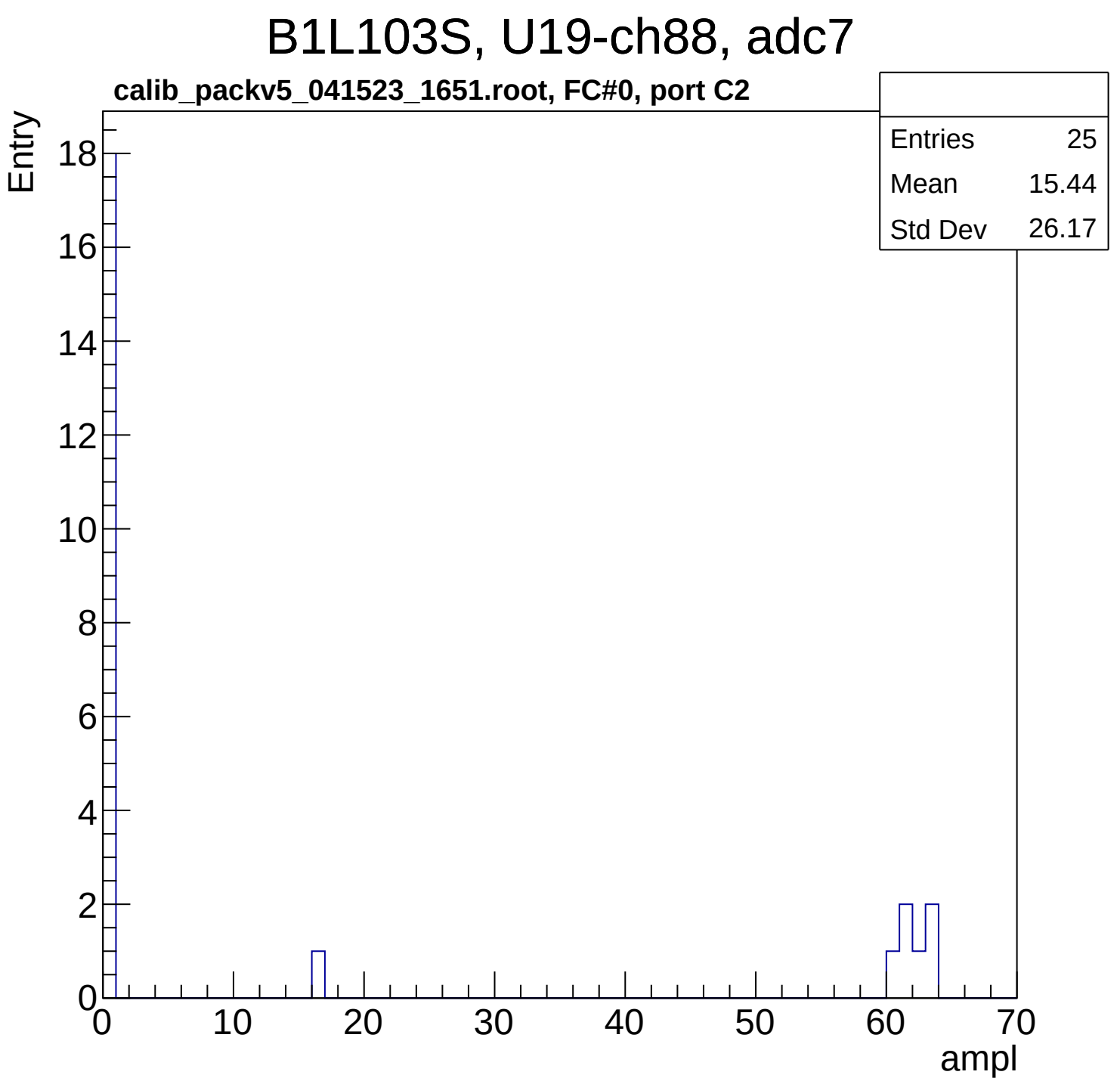
B1L103S, U19-ch88, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 15.44
Std Dev 26.17
Entry
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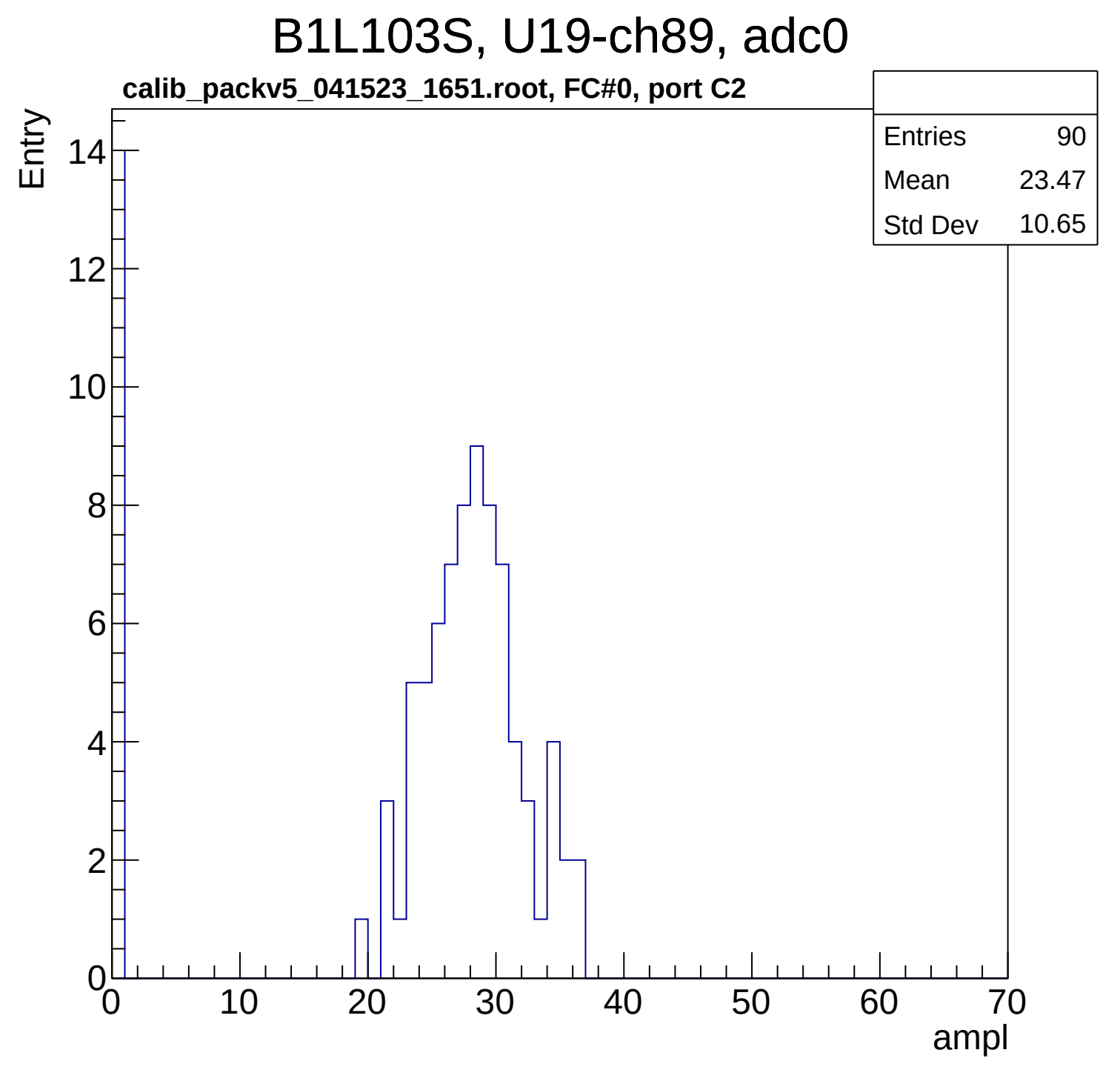
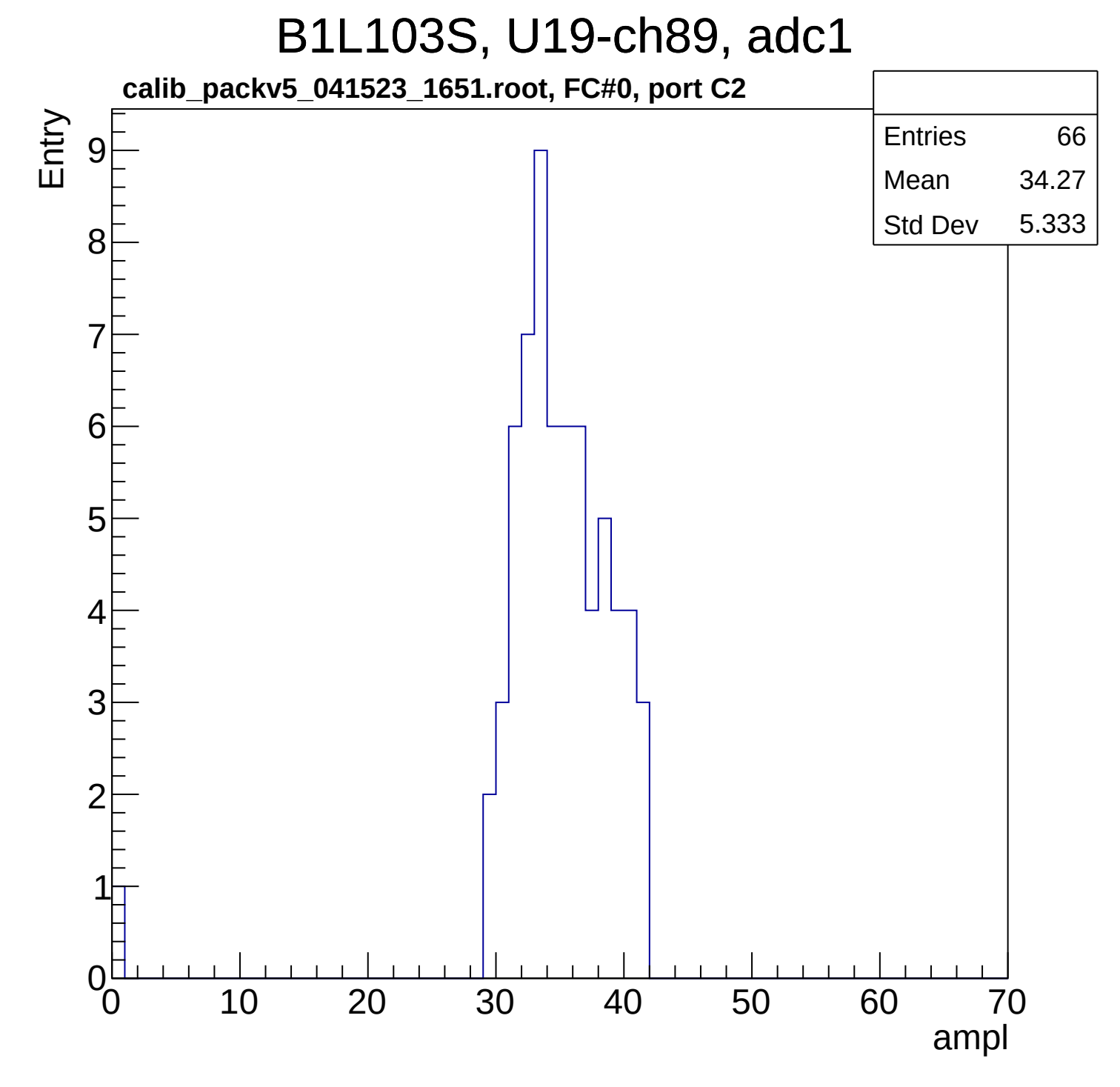
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch89, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 23.47
Std Dev 10.65
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U19-ch89, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 34.27
Std Dev 5.333
Entry
ampl
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6
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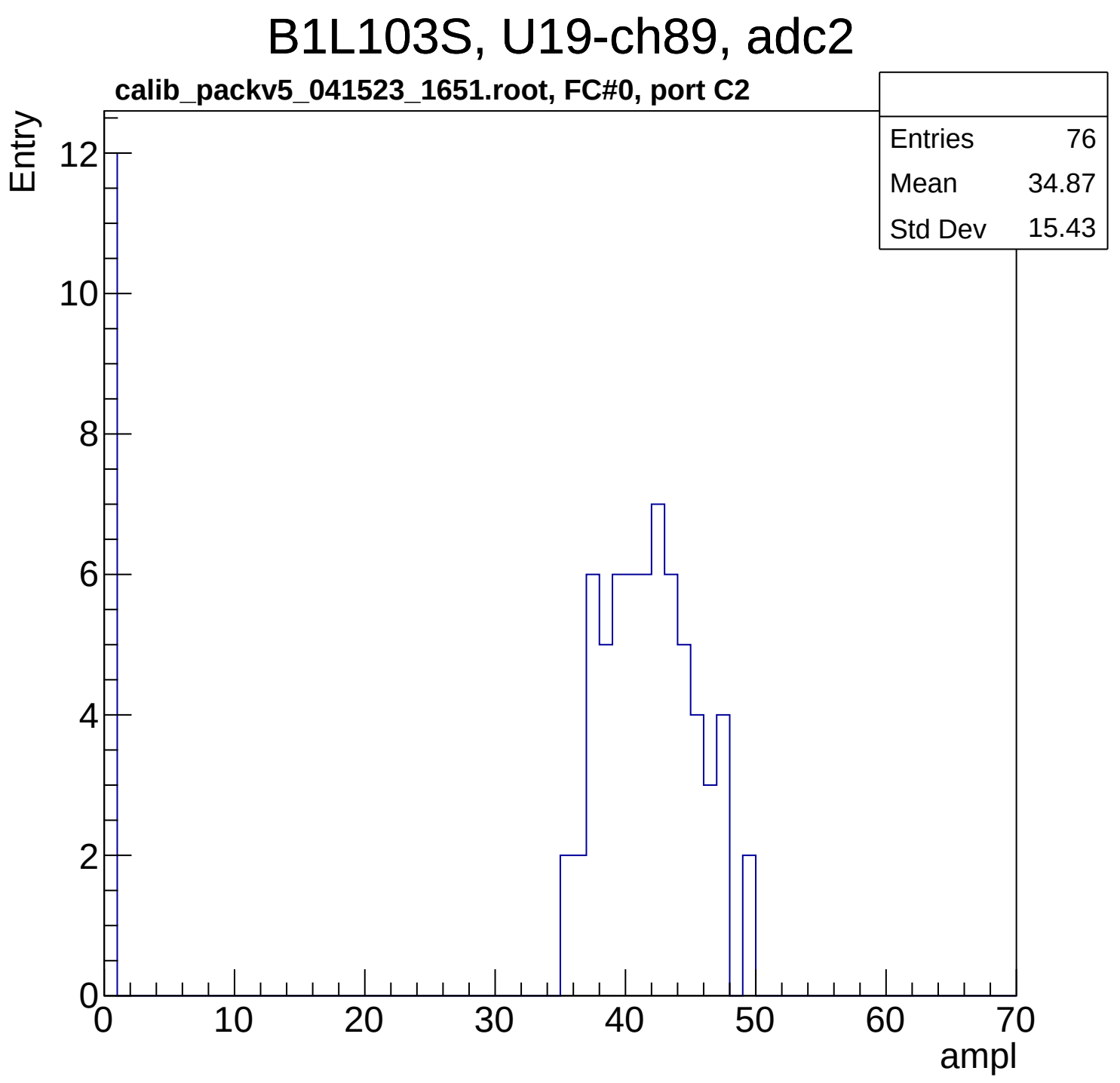
B1L103S, U19-ch89, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 34.87
Std Dev 15.43
Entry
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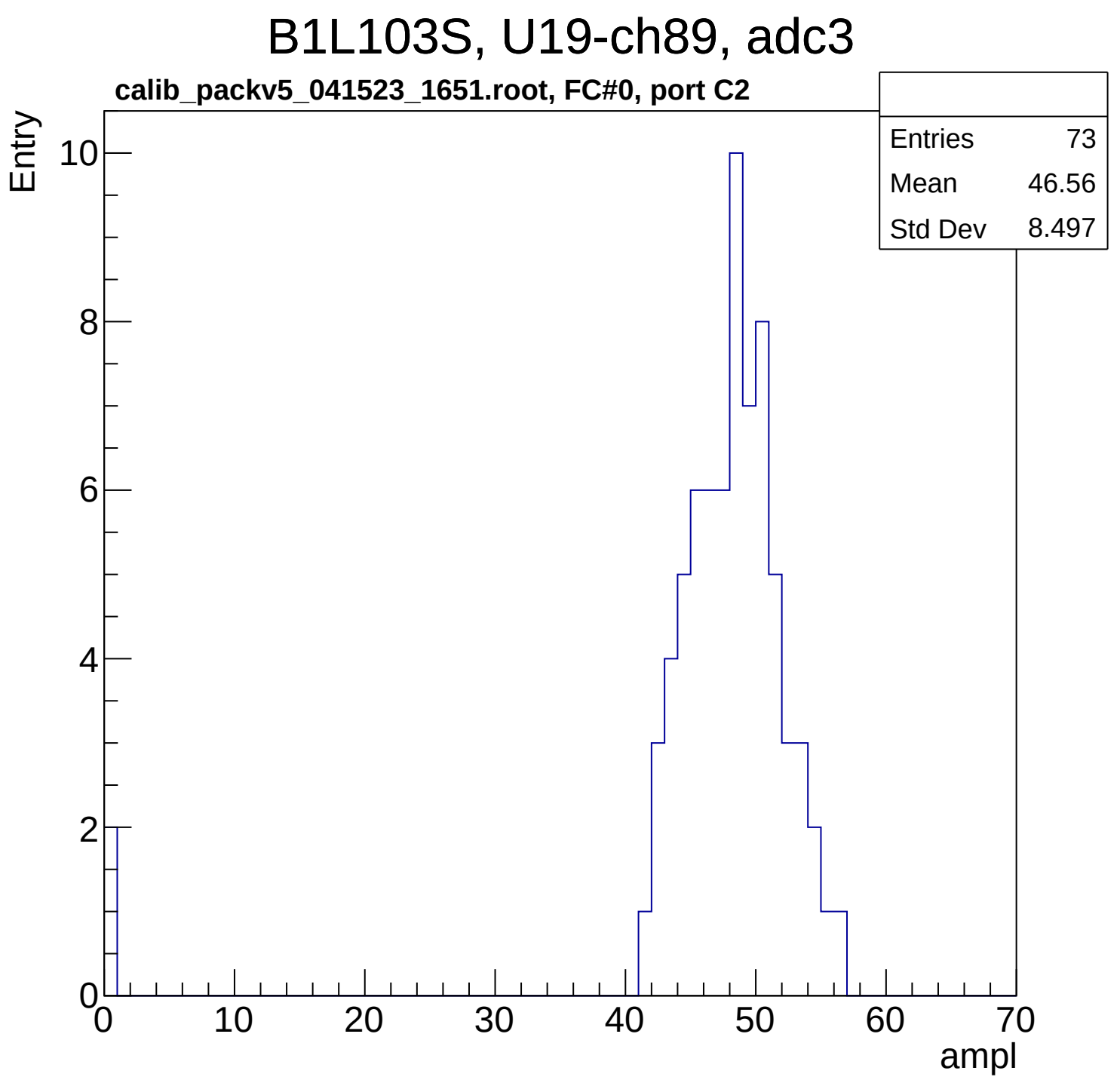
ampl


B1L103S, U19-ch89, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 46.56
Std Dev 8.497
Entry
ampl
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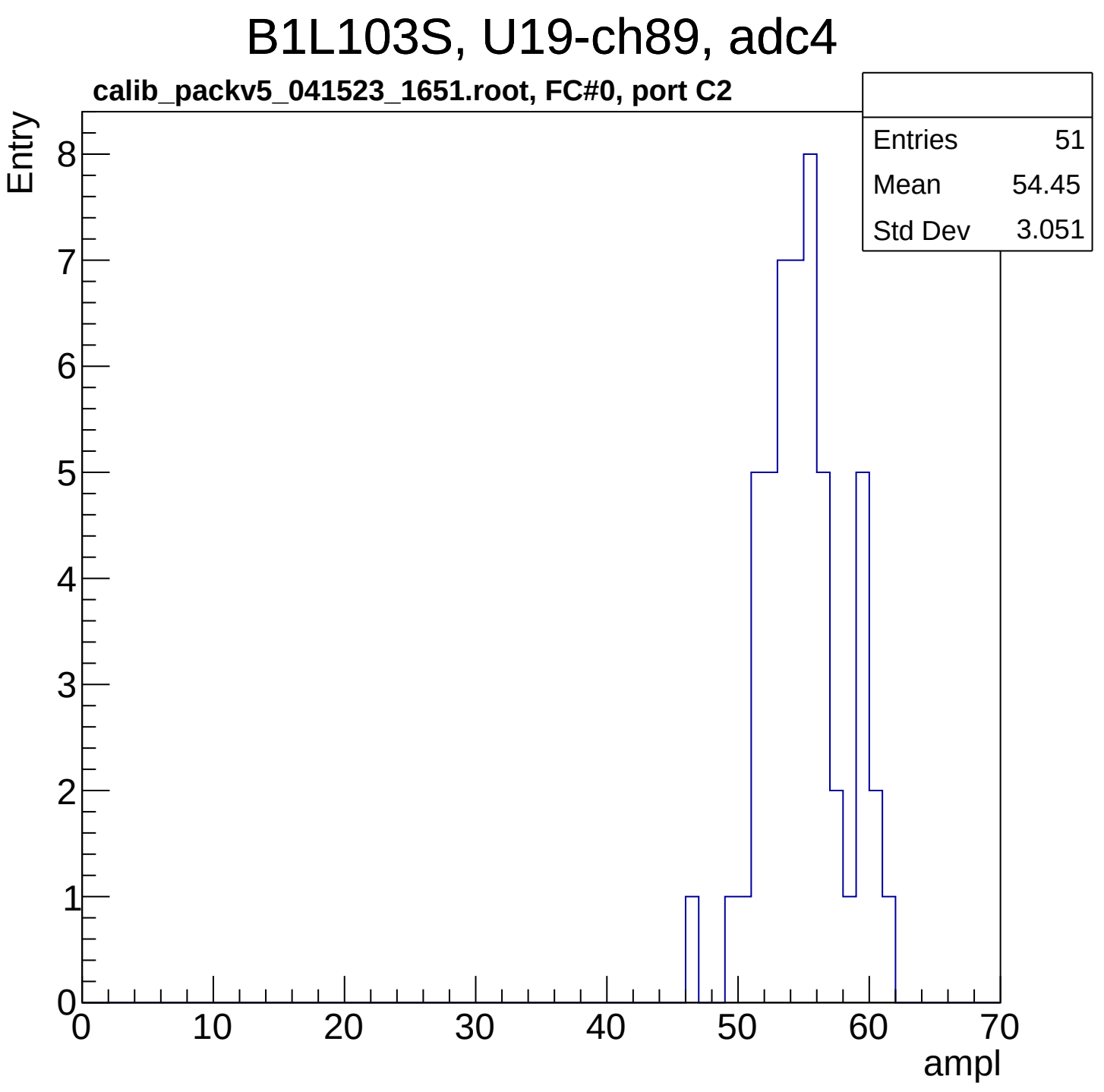
B1L103S, U19-ch89, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 54.45
Std Dev 3.051
Entry
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4
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6
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8
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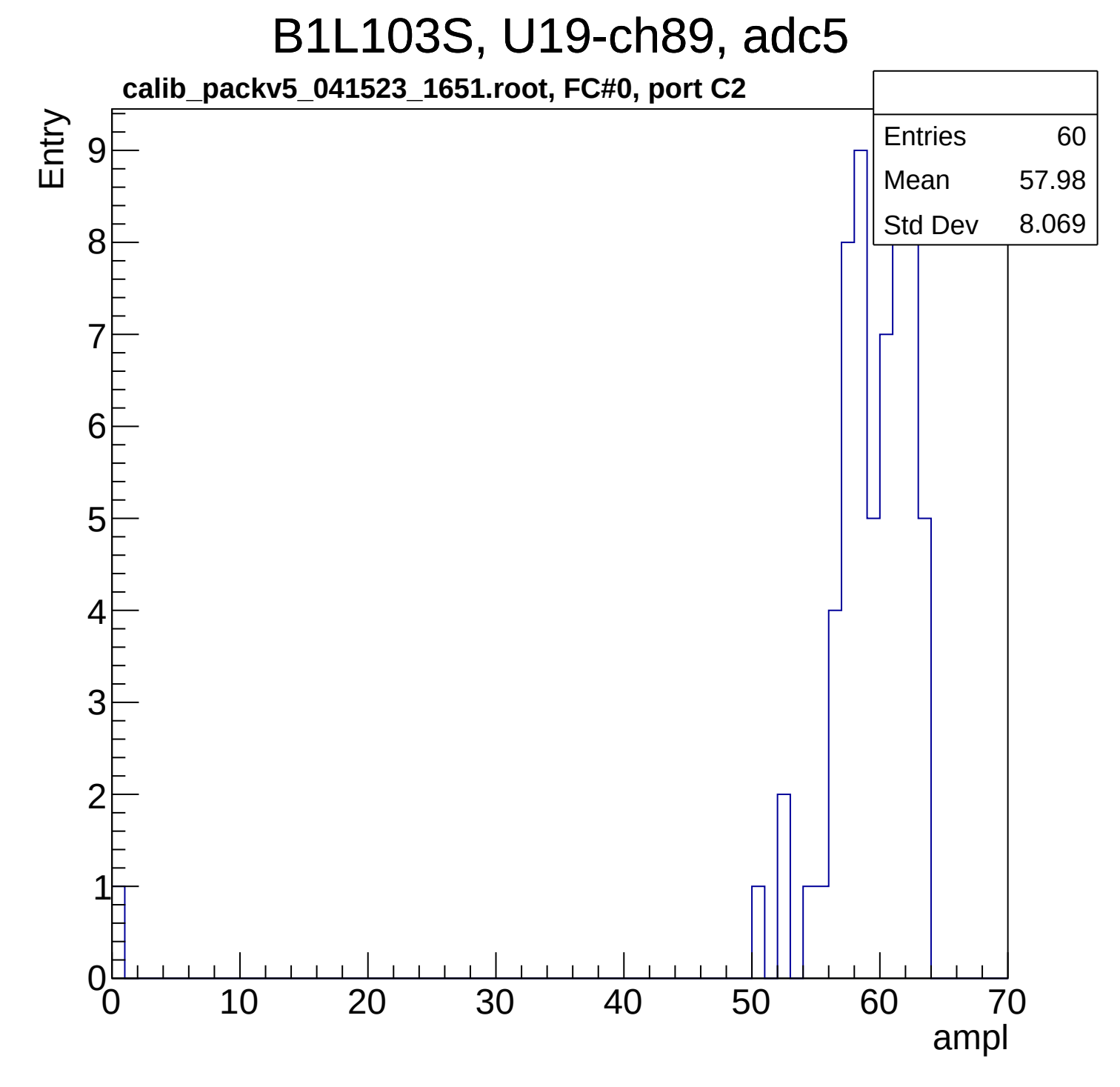
70
ampl


B1L103S, U19-ch89, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 57.98
Std Dev 8.069
Entry
ampl
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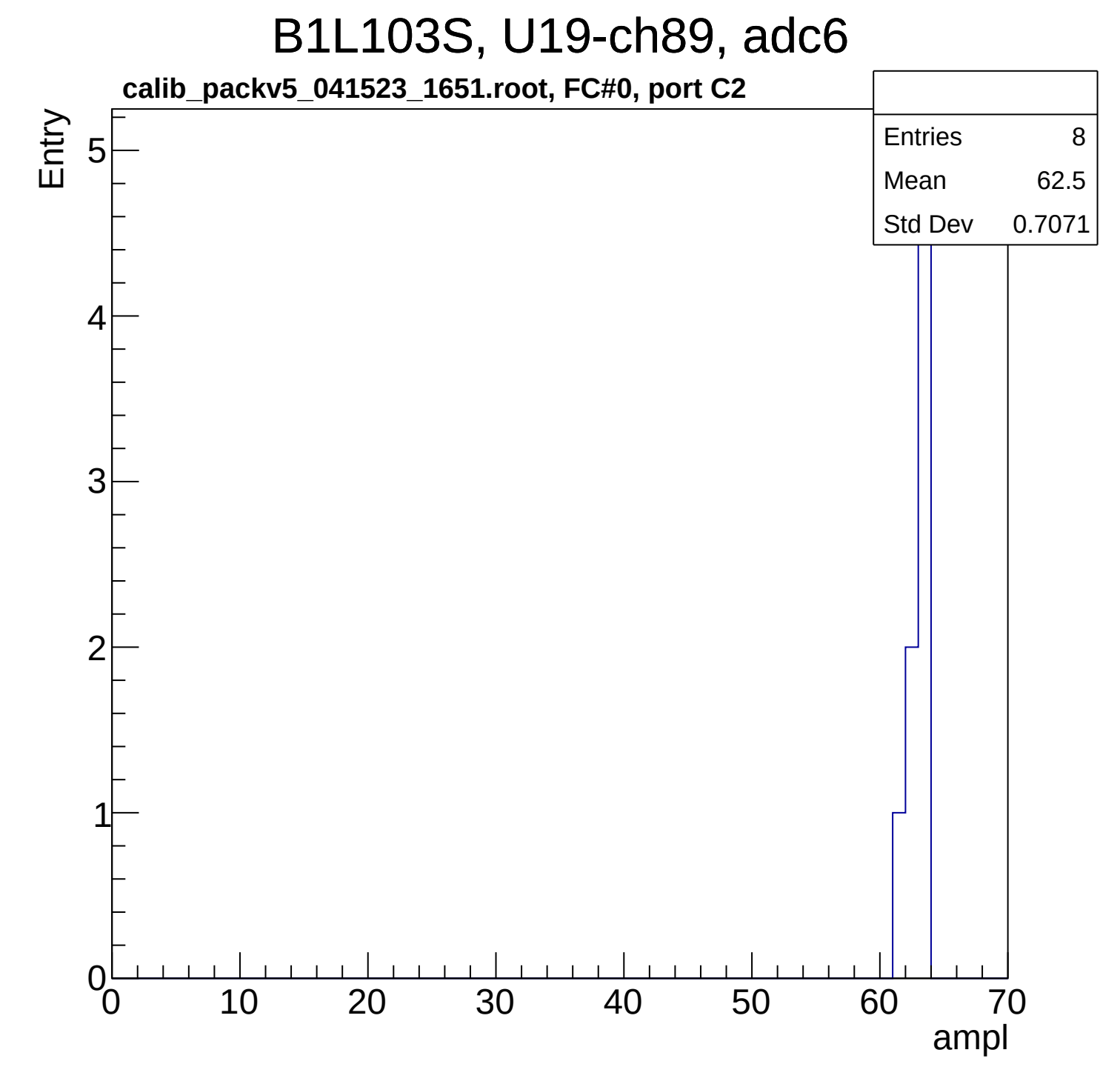
B1L103S, U19-ch89, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 62.5
Std Dev 0.7071
Entry
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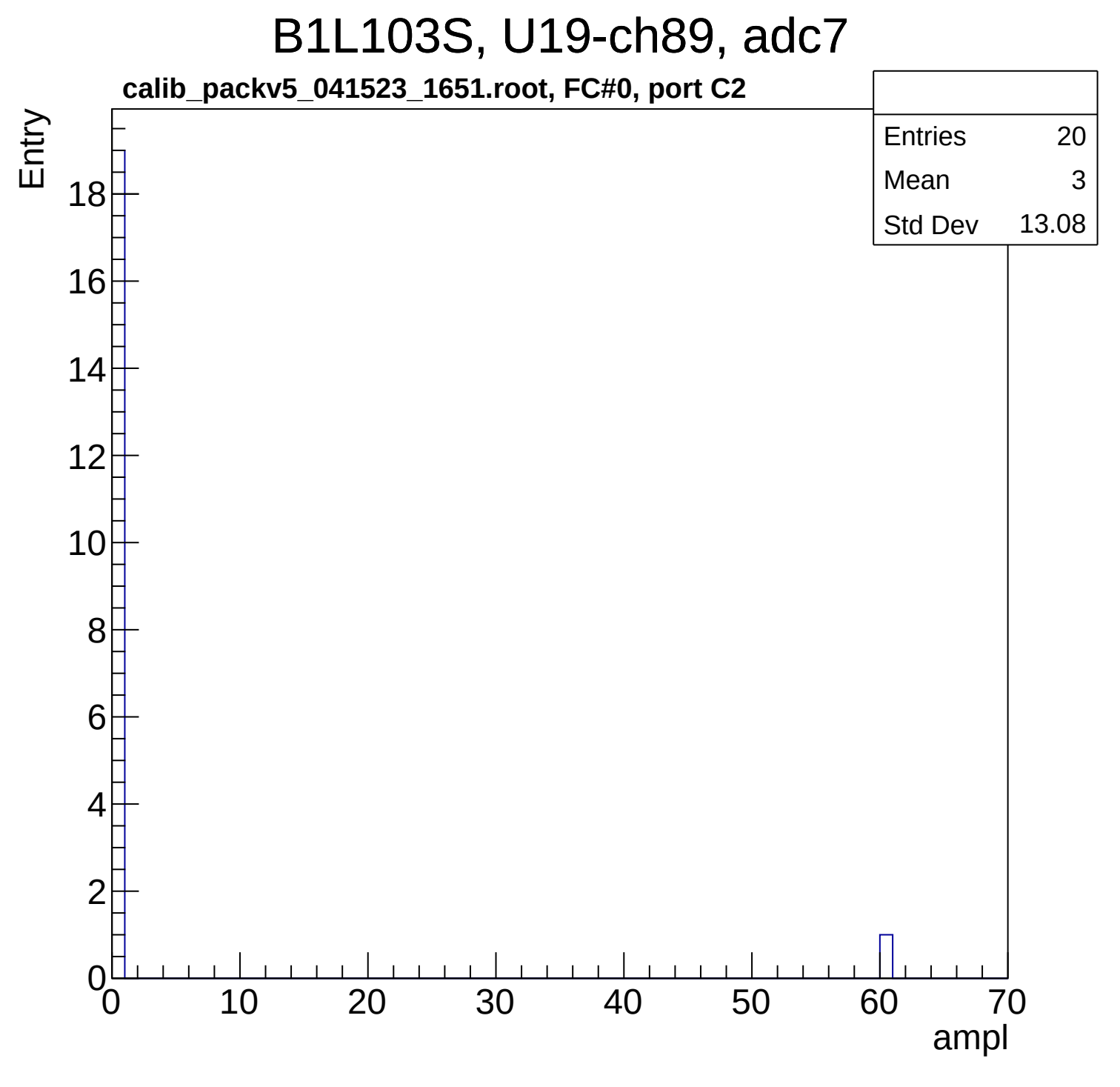
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch89, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3
Std Dev 13.08
Entry
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6
8
10
12
14
16
18
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10
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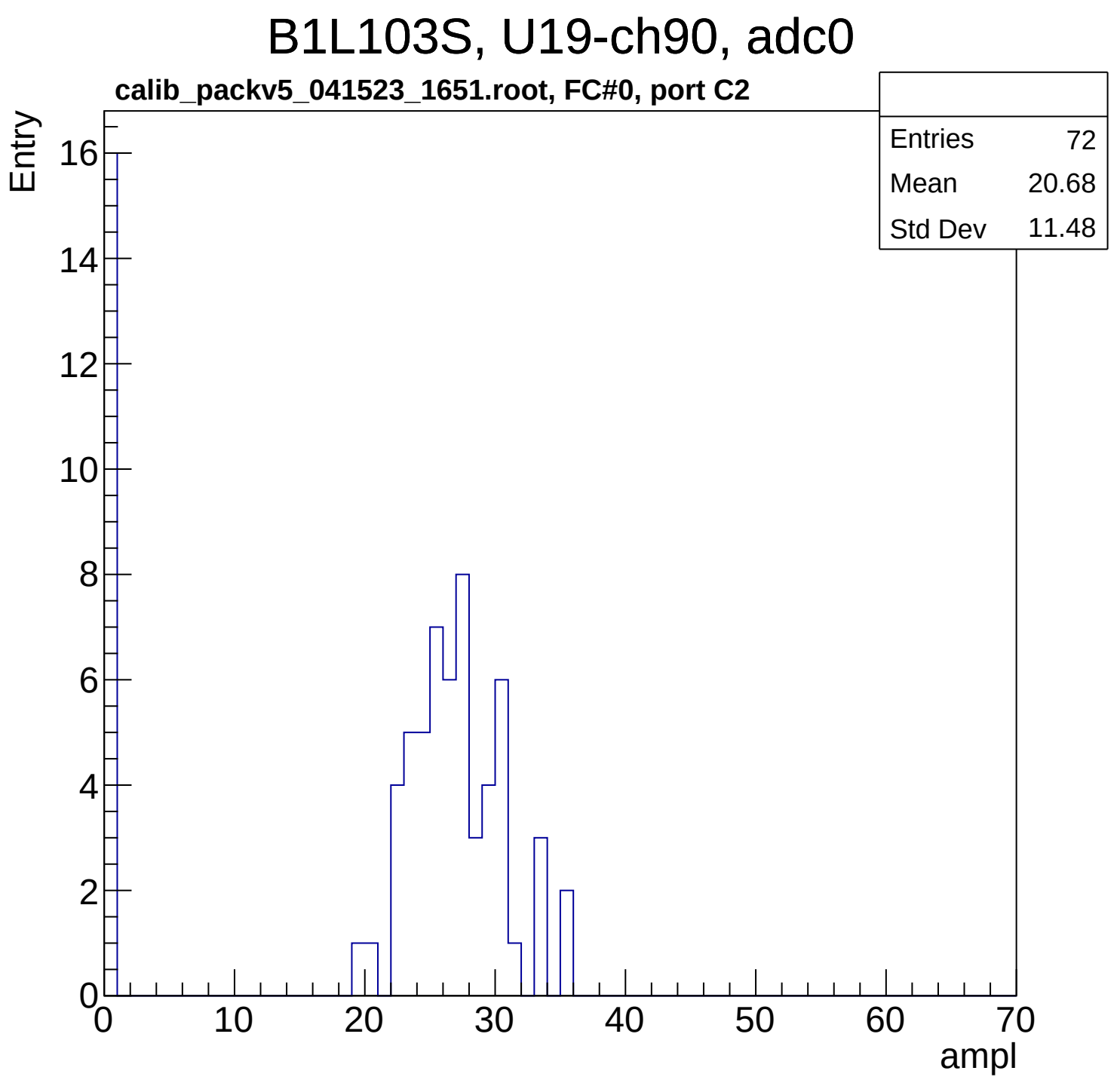
70
ampl


B1L103S, U19-ch90, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 20.68
Std Dev 11.48
Entry
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12
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50
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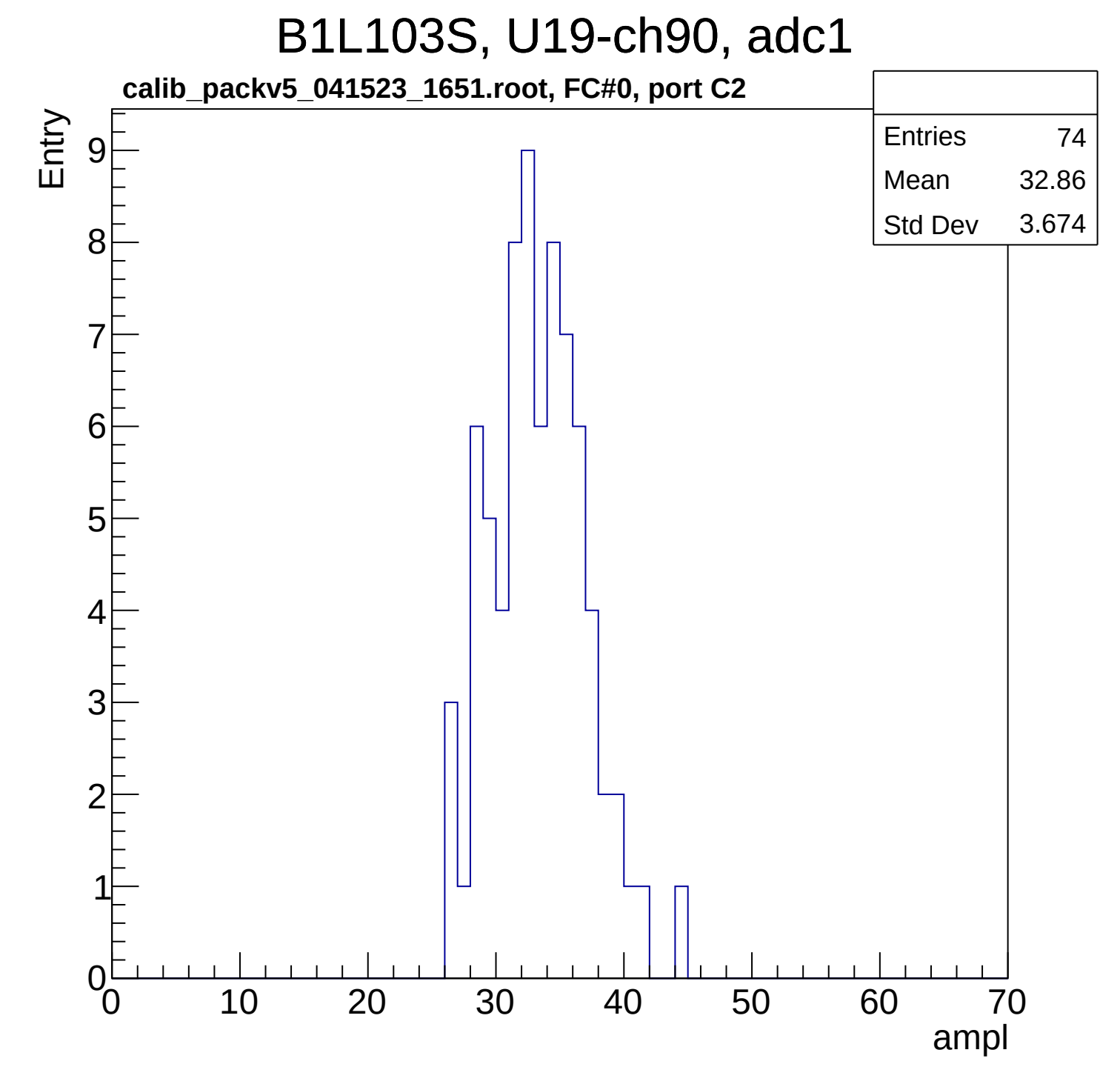
ampl


B1L103S, U19-ch90, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 32.86
Std Dev 3.674
Entry
ampl
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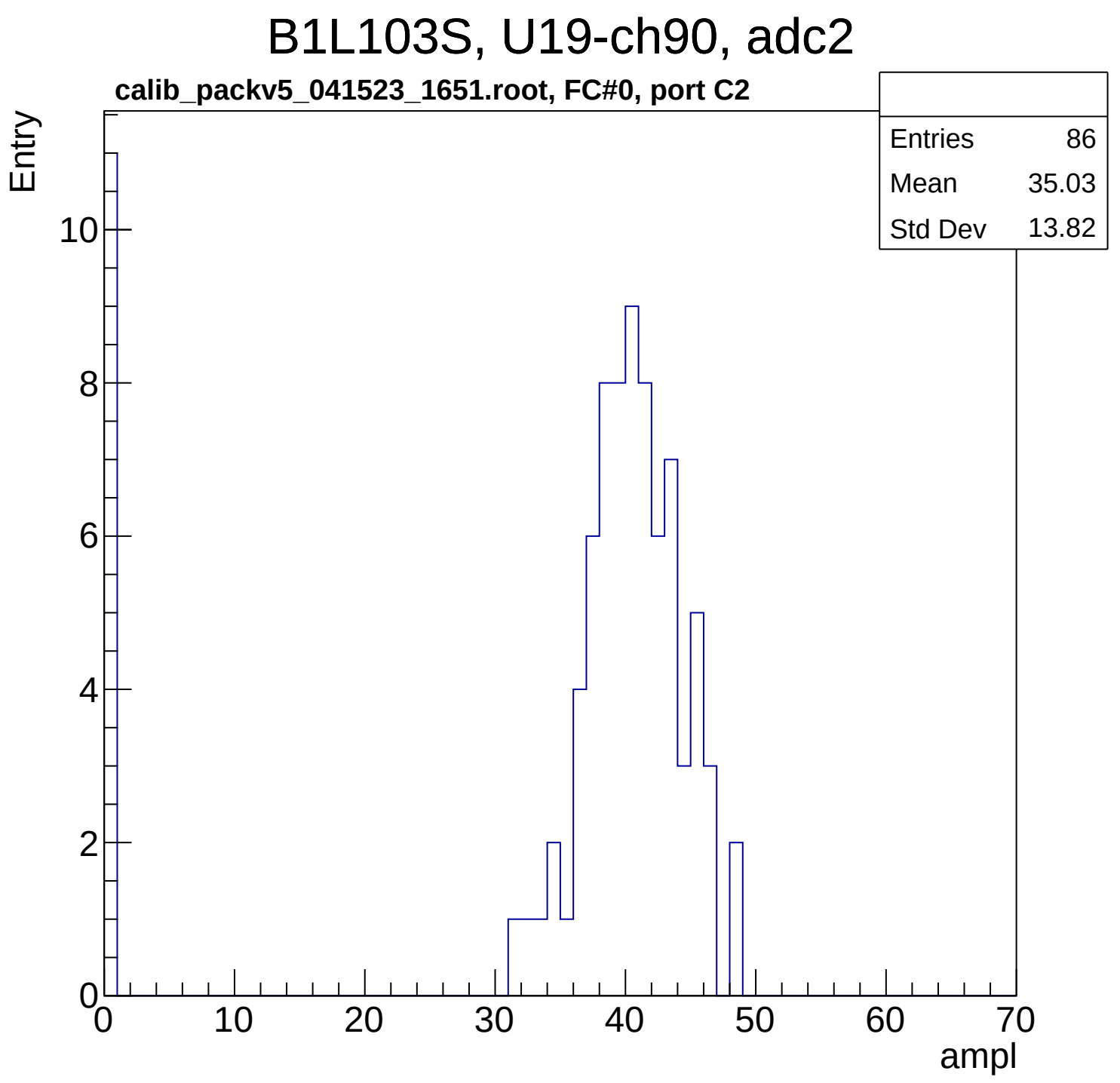
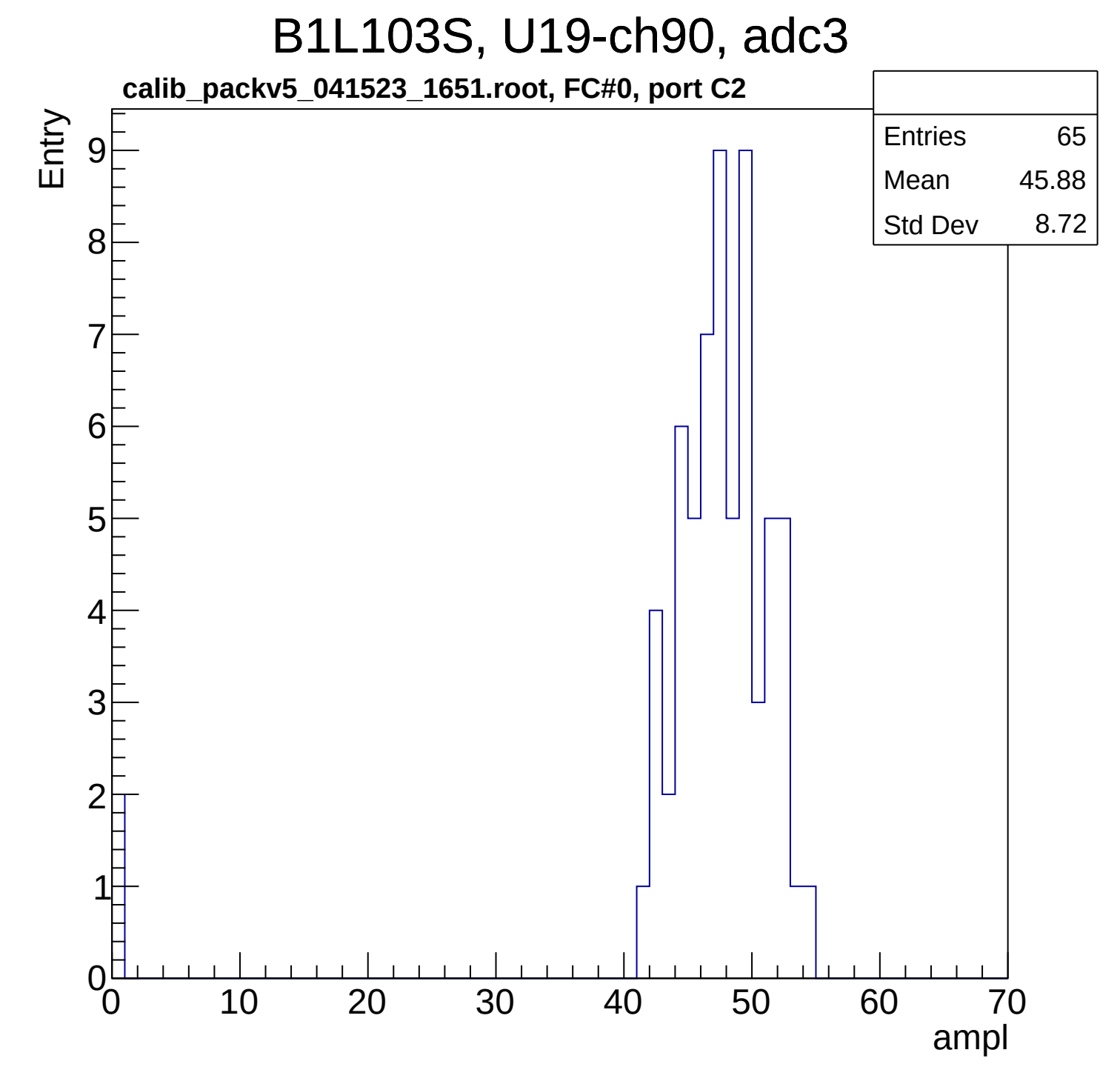
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch90, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 35.03
Std Dev 13.82
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch90, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 45.88
Std Dev 8.72
Entry
ampl
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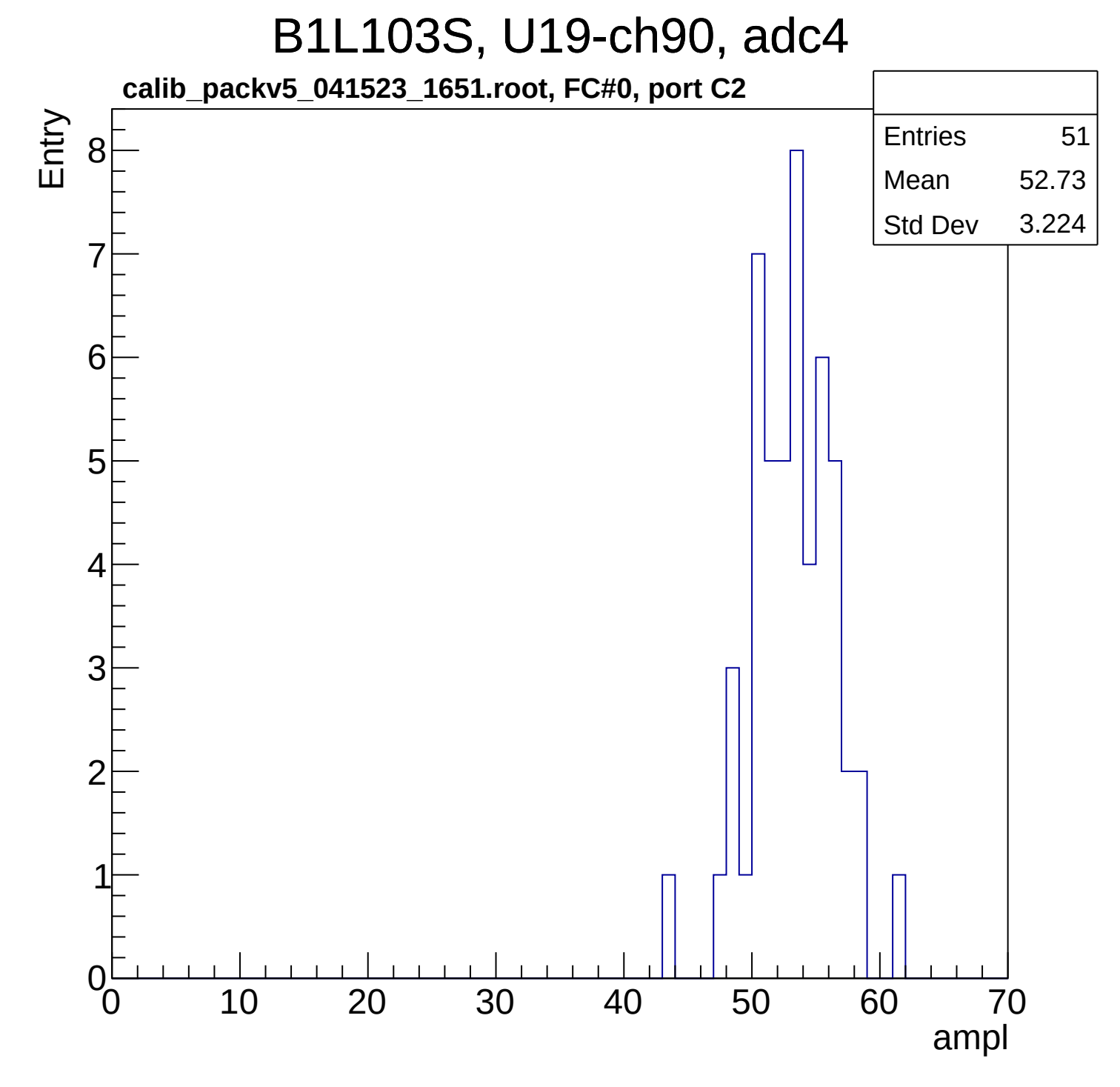
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch90, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 52.73
Std Dev 3.224
Entry
ampl
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2
3
4
5
6
7
8
0
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40
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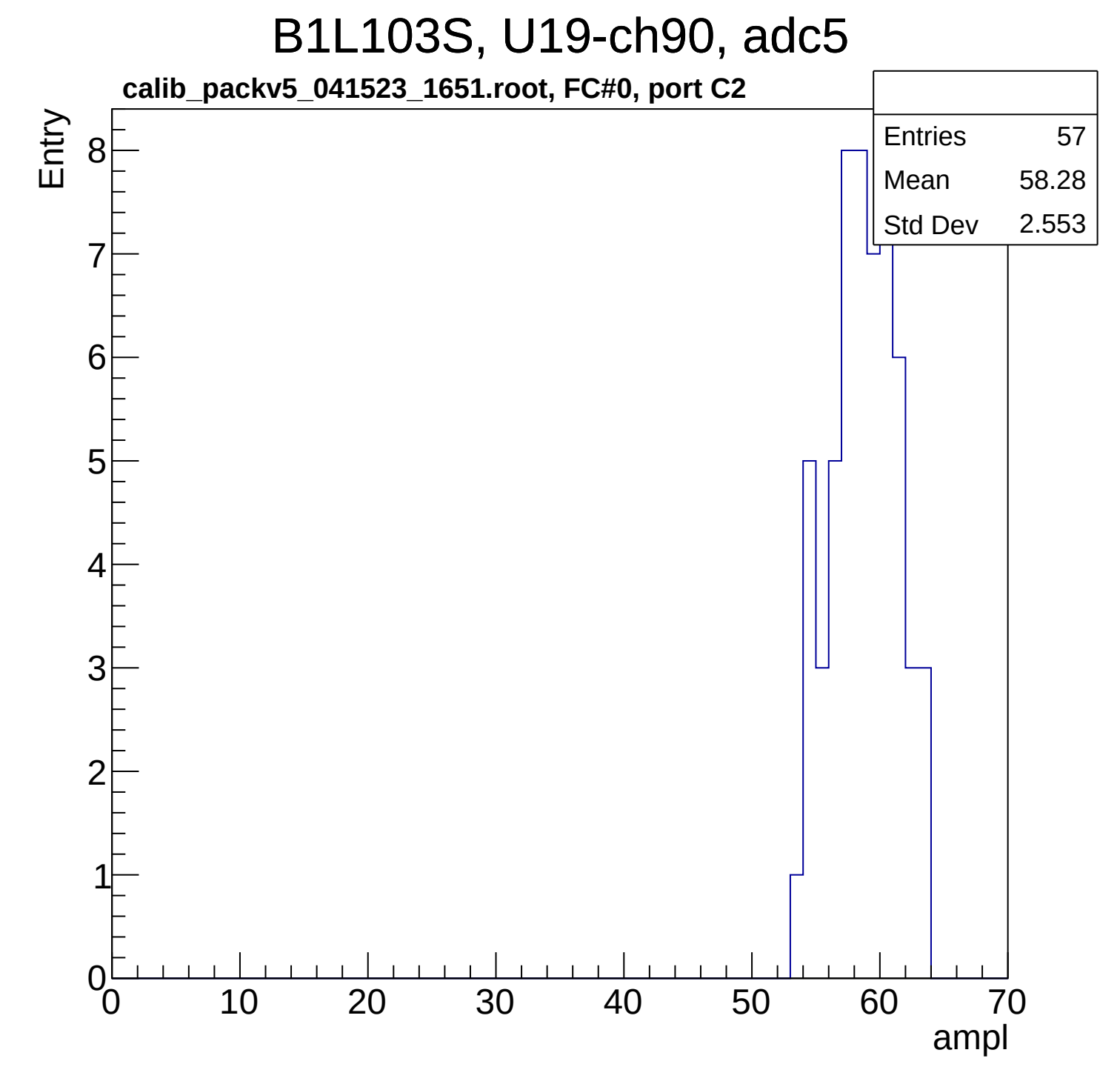
B1L103S, U19-ch90, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 58.28
Std Dev 2.553
Entry
ampl
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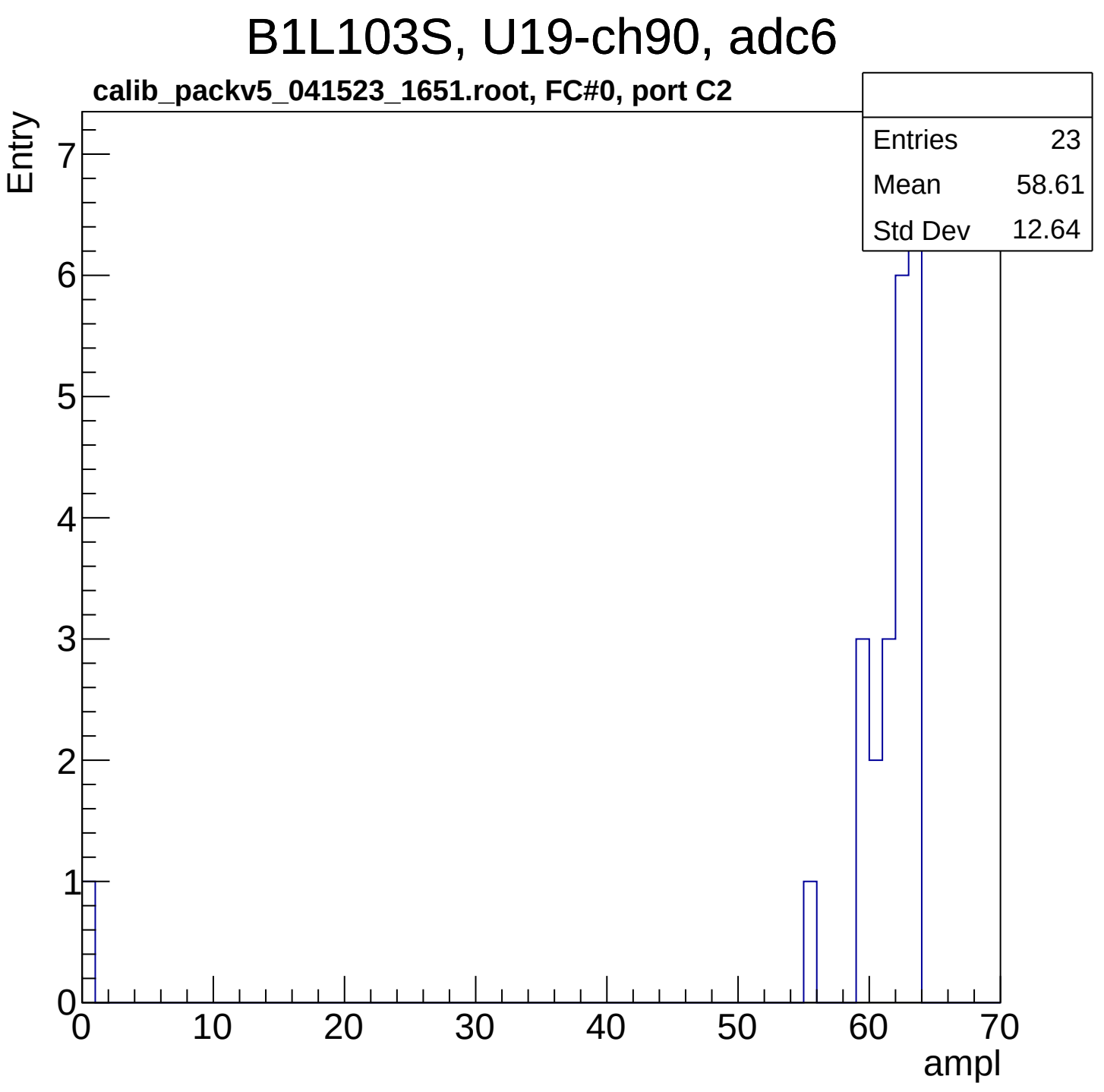
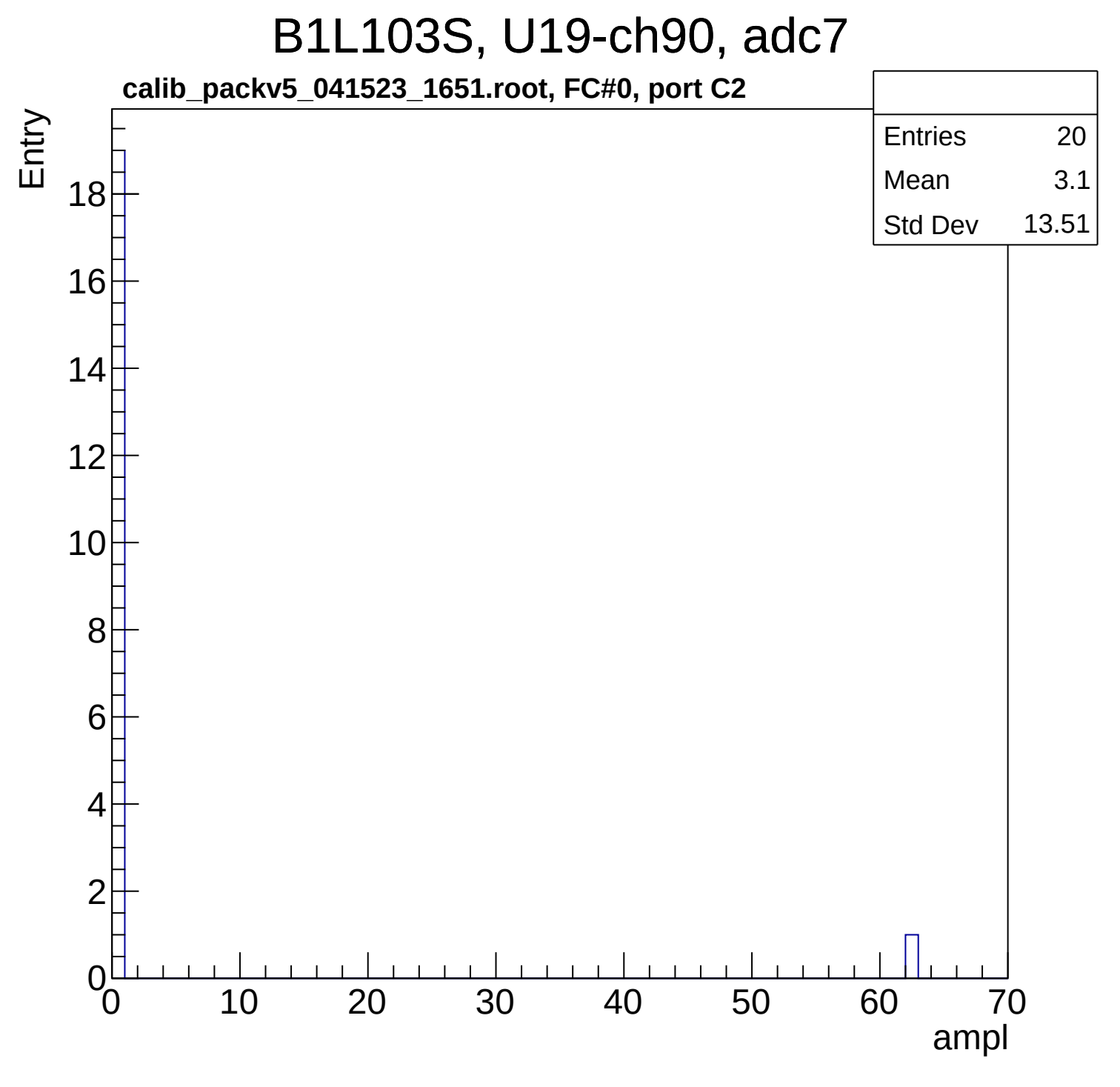
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch90, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 58.61
Std Dev 12.64
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch90, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
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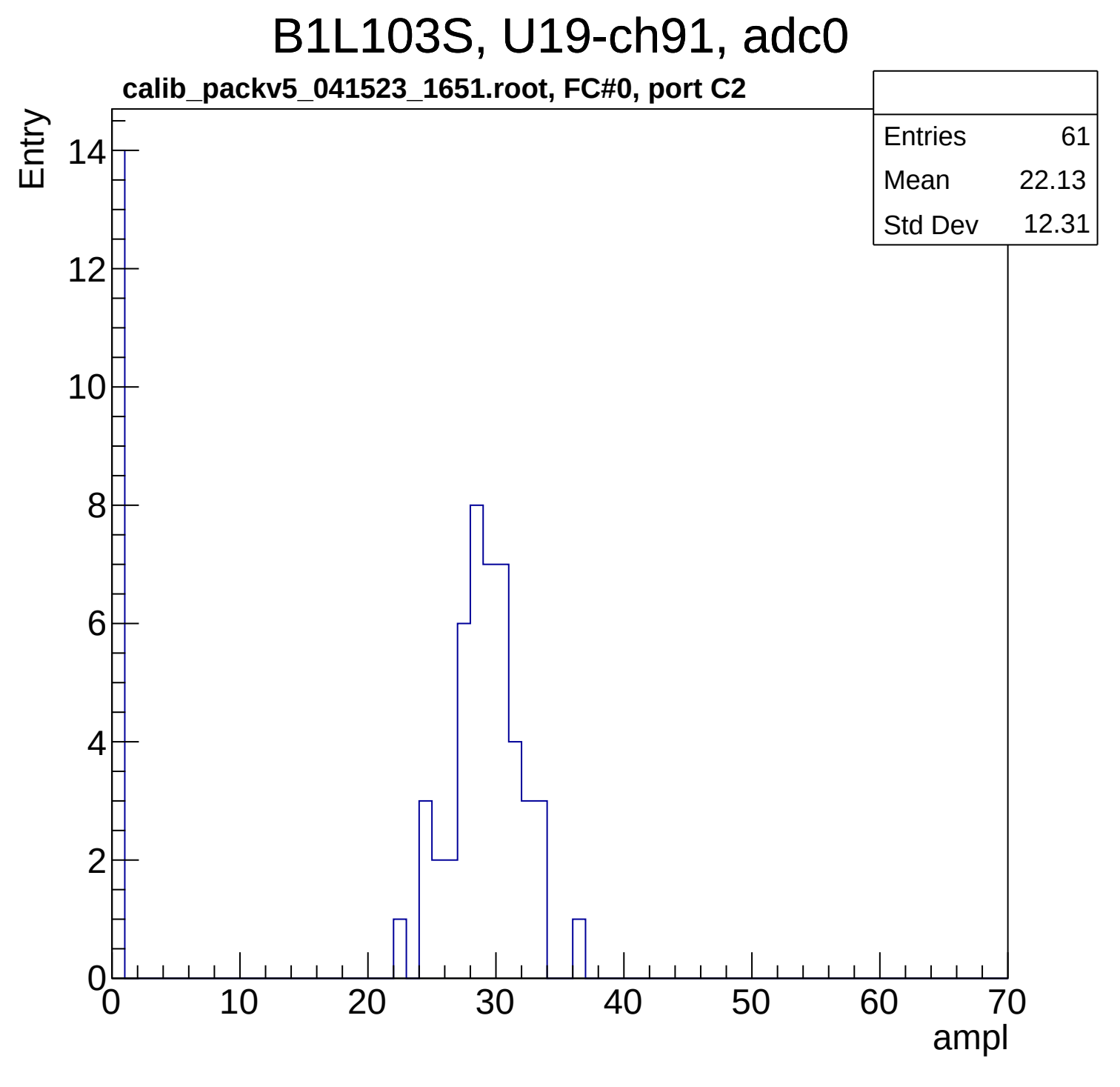
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch91, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 22.13
Std Dev 12.31
Entry
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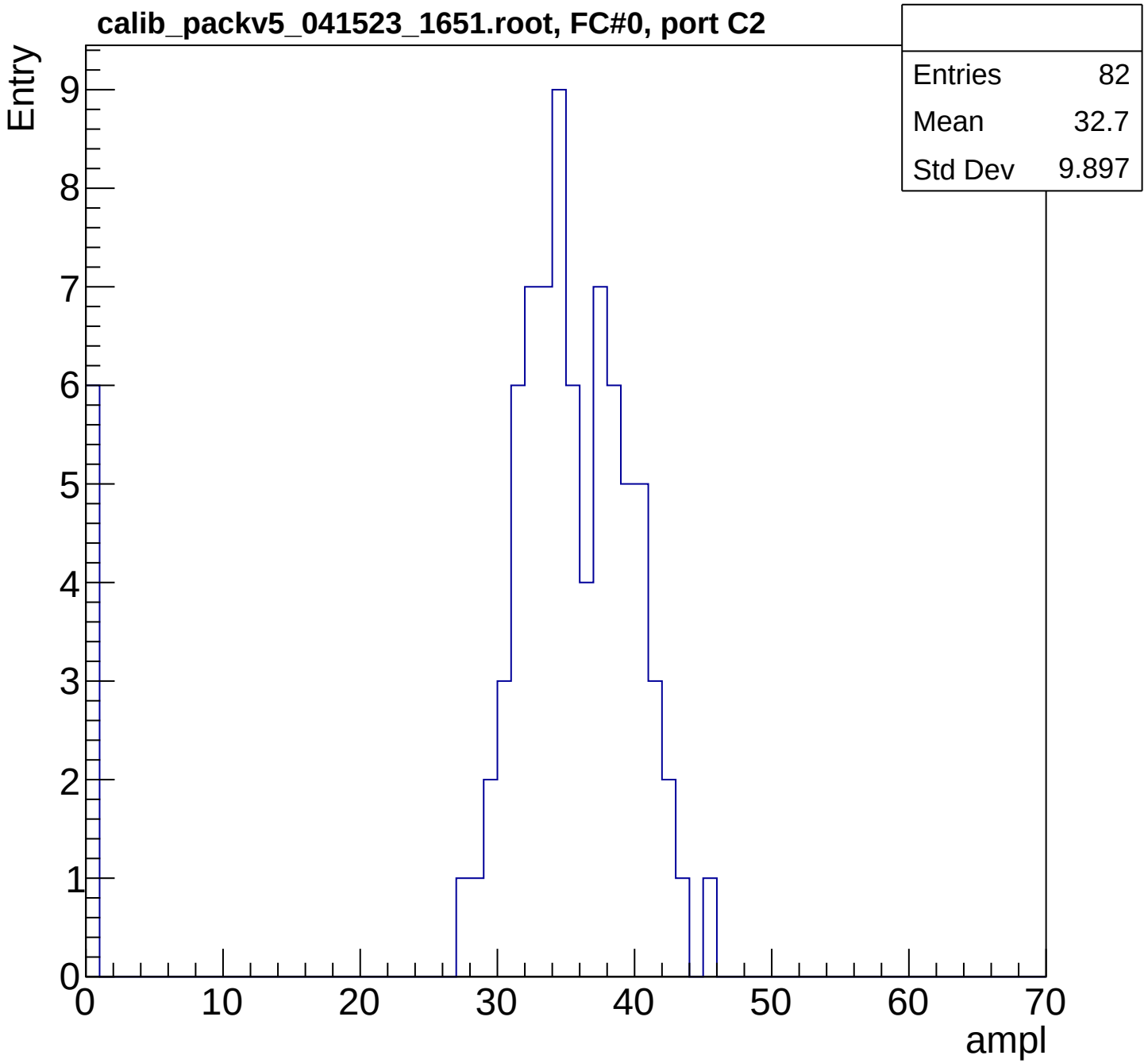
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch91, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 32.7
Std Dev 9.897
Entry
ampl
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3
4
5
6
7
8
9
0
10
20
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40
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60
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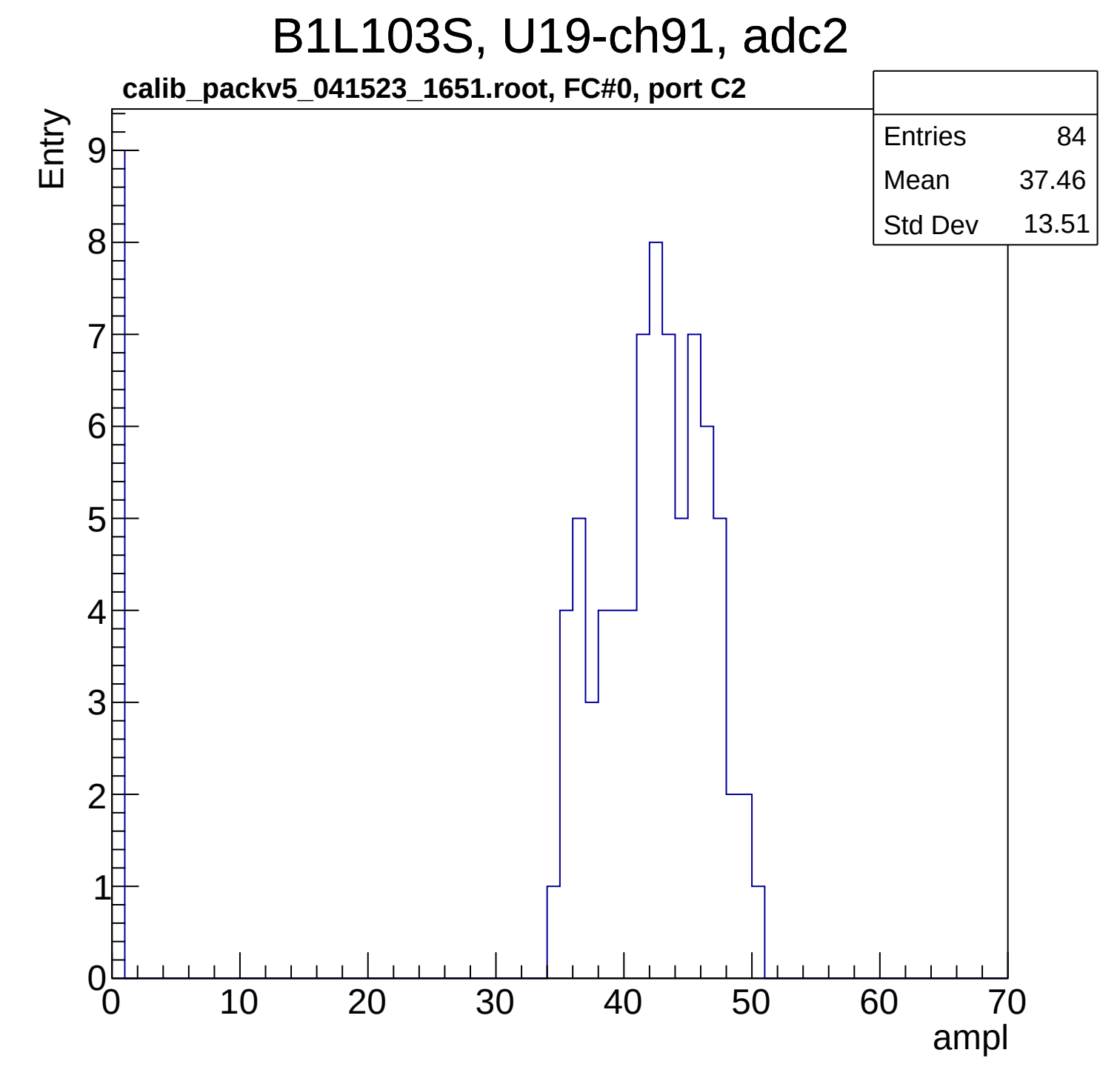
B1L103S, U19-ch91, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 37.46
Std Dev 13.51
Entry
ampl
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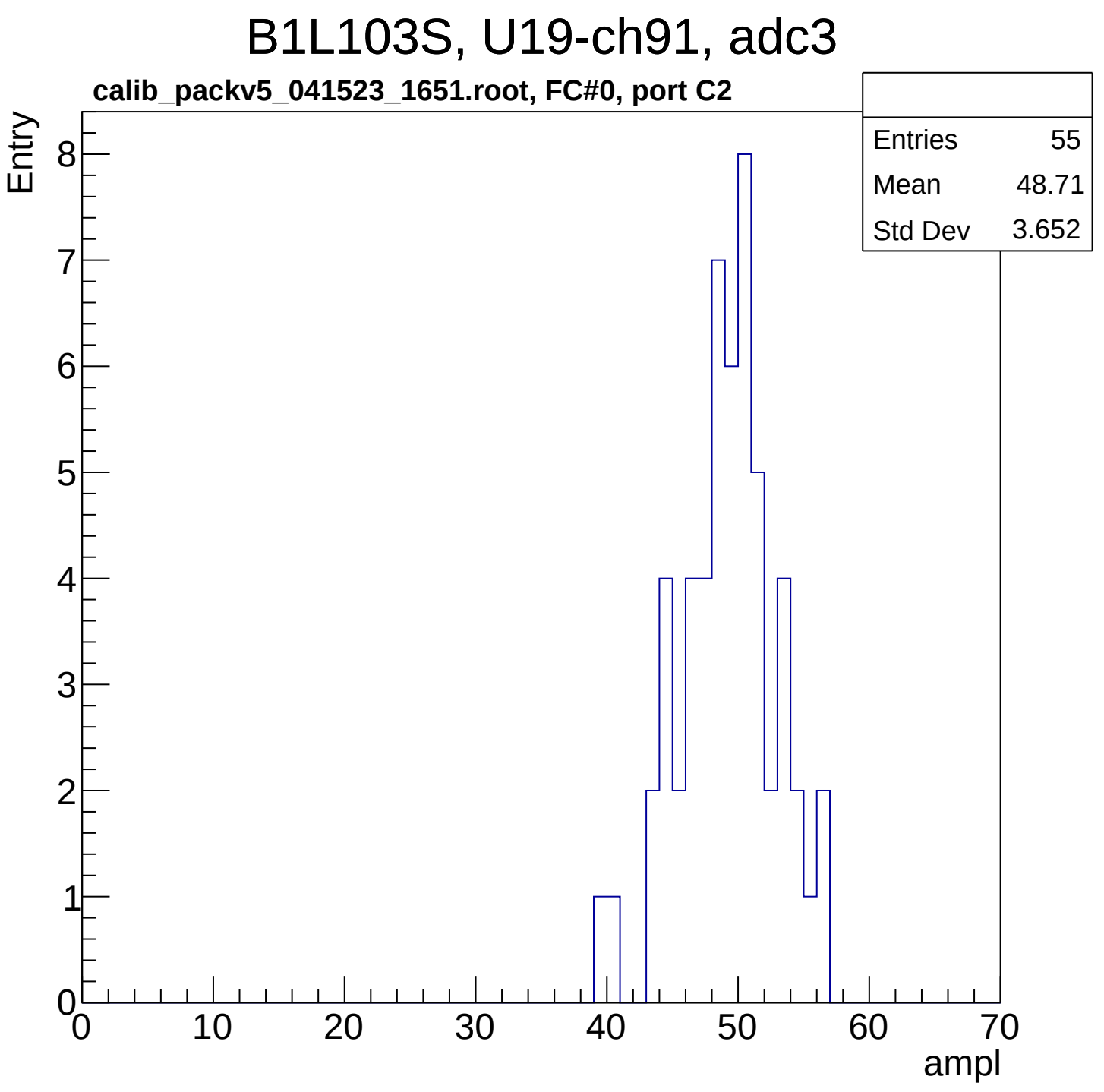
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch91, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 48.71
Std Dev 3.652
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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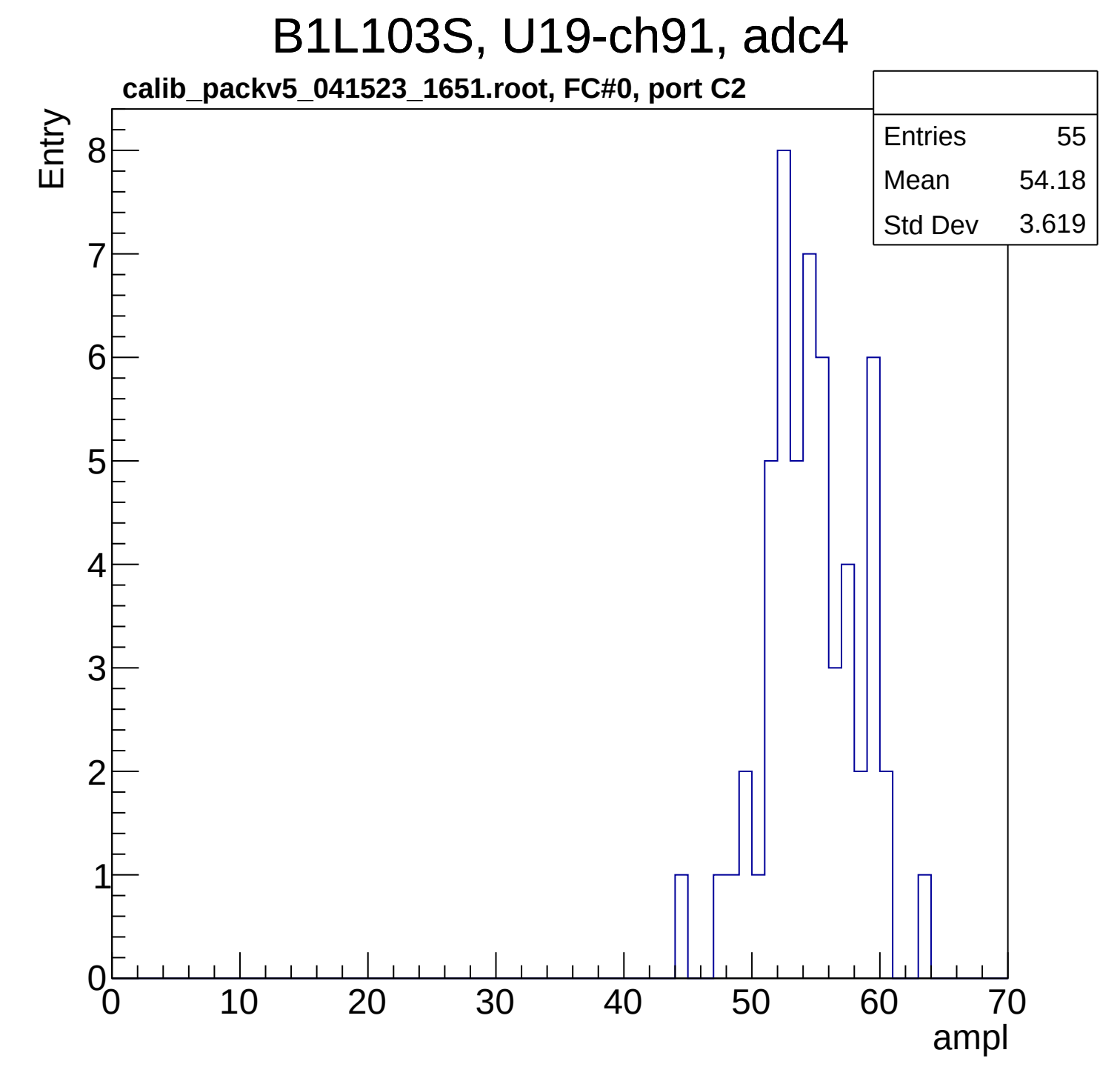
40
50
60
70


B1L103S, U19-ch91, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 54.18
Std Dev 3.619
Entry
ampl
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2
3
4
5
6
7
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0
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60
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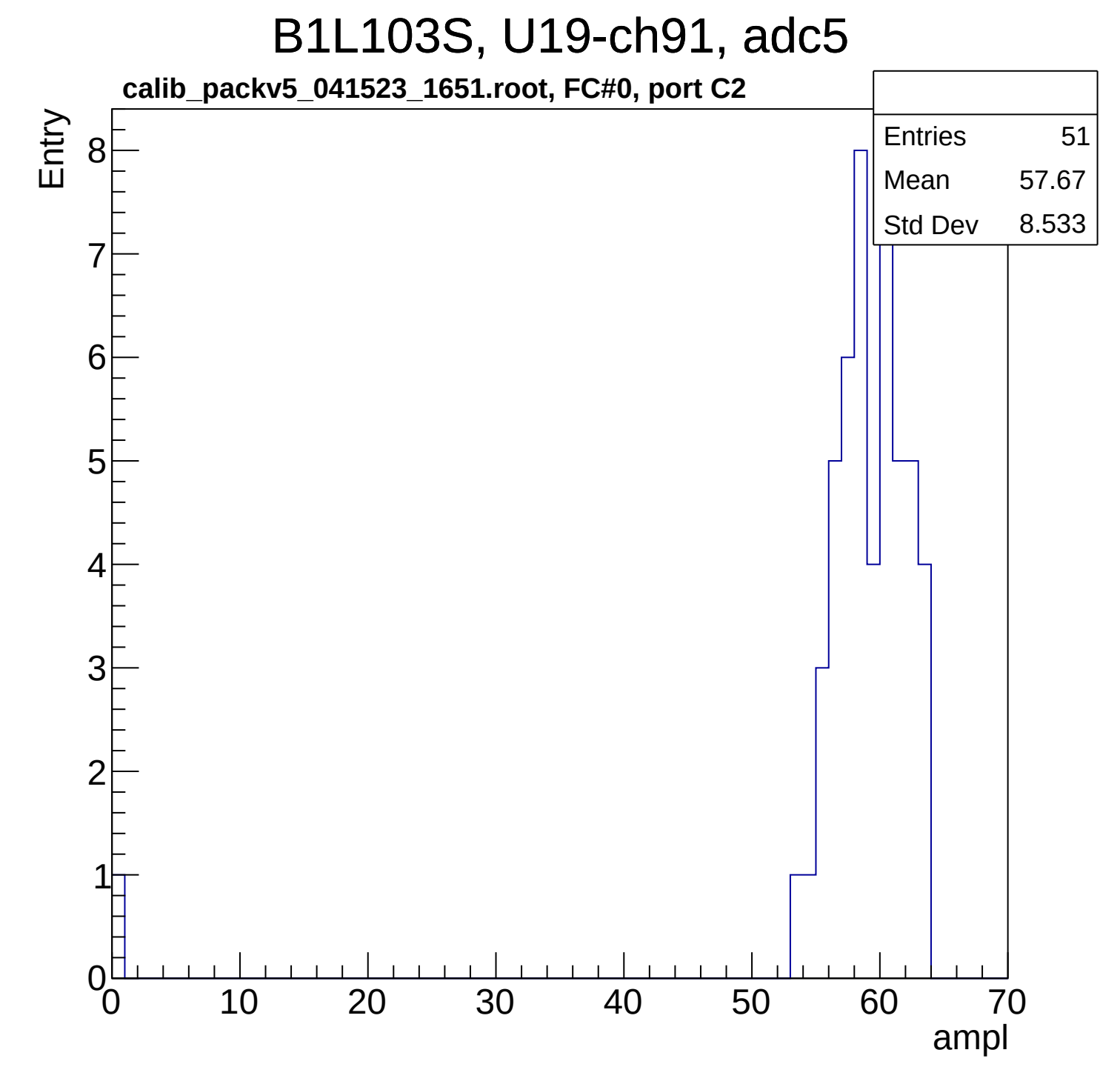
B1L103S, U19-ch91, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 57.67
Std Dev 8.533
Entry
ampl
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4
5
6
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0
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60
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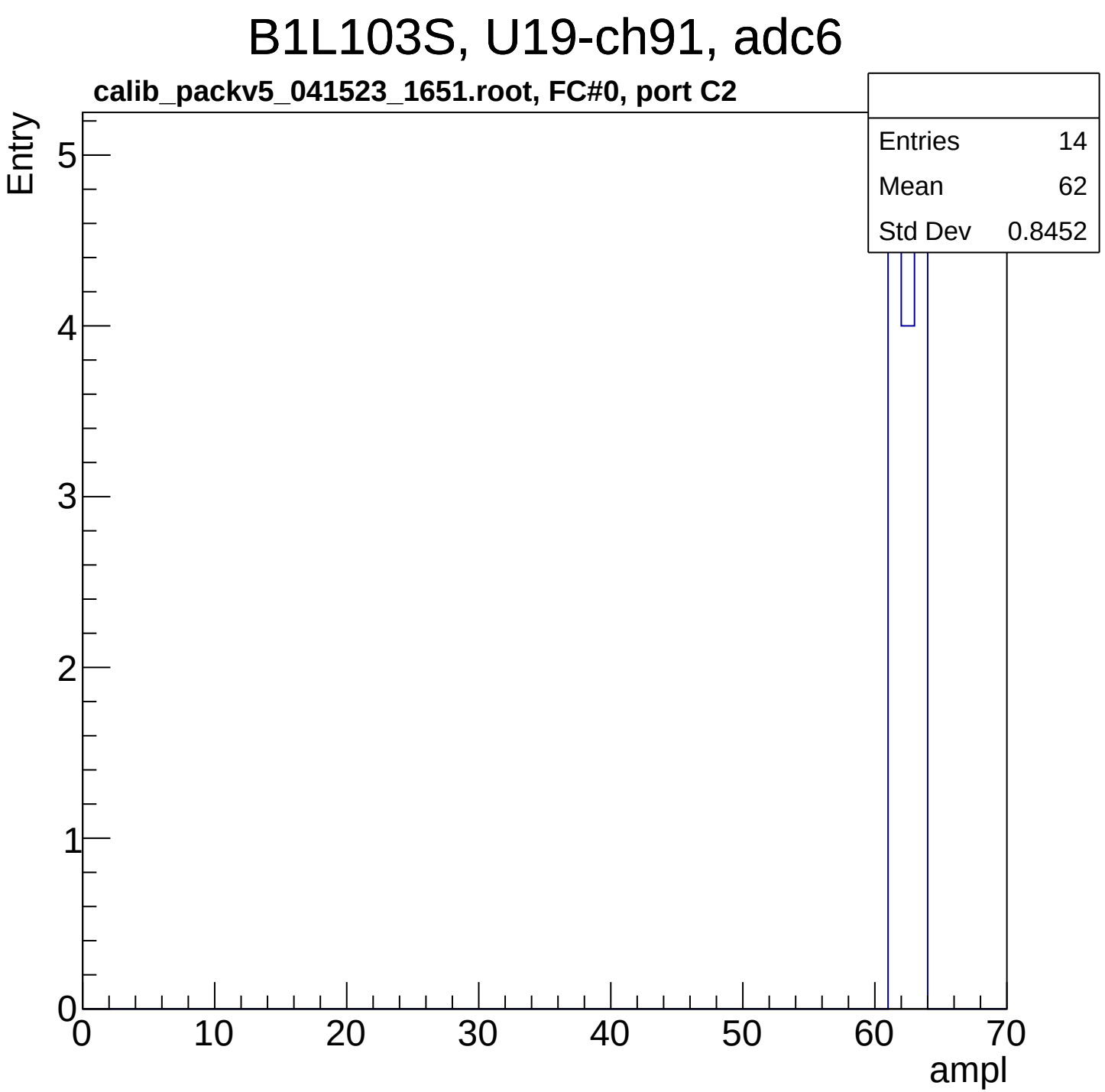
B1L103S, U19-ch91, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 62
Std Dev 0.8452
Entry
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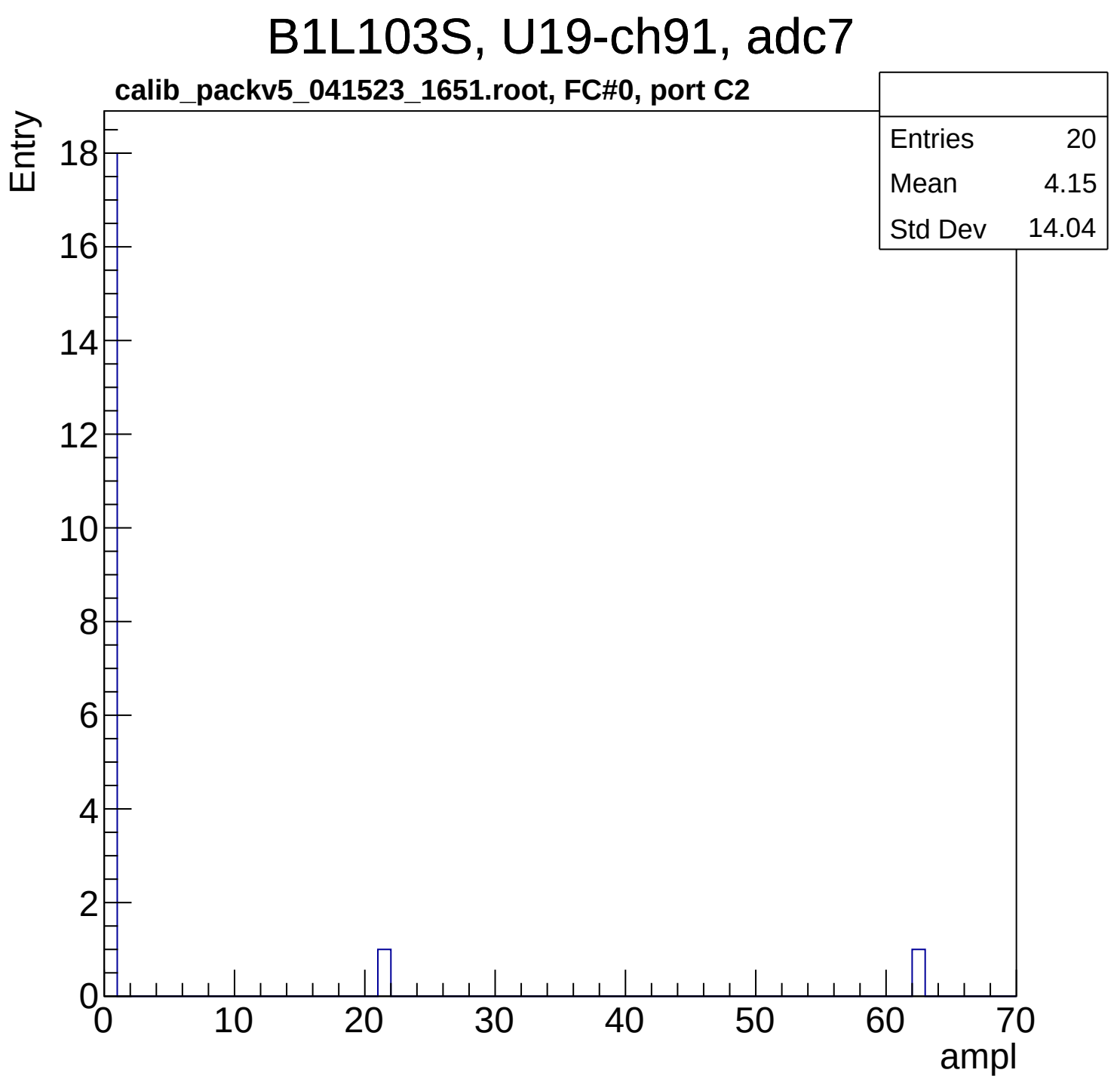
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch91, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4.15
Std Dev 14.04
Entry
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6
8
10
12
14
16
18
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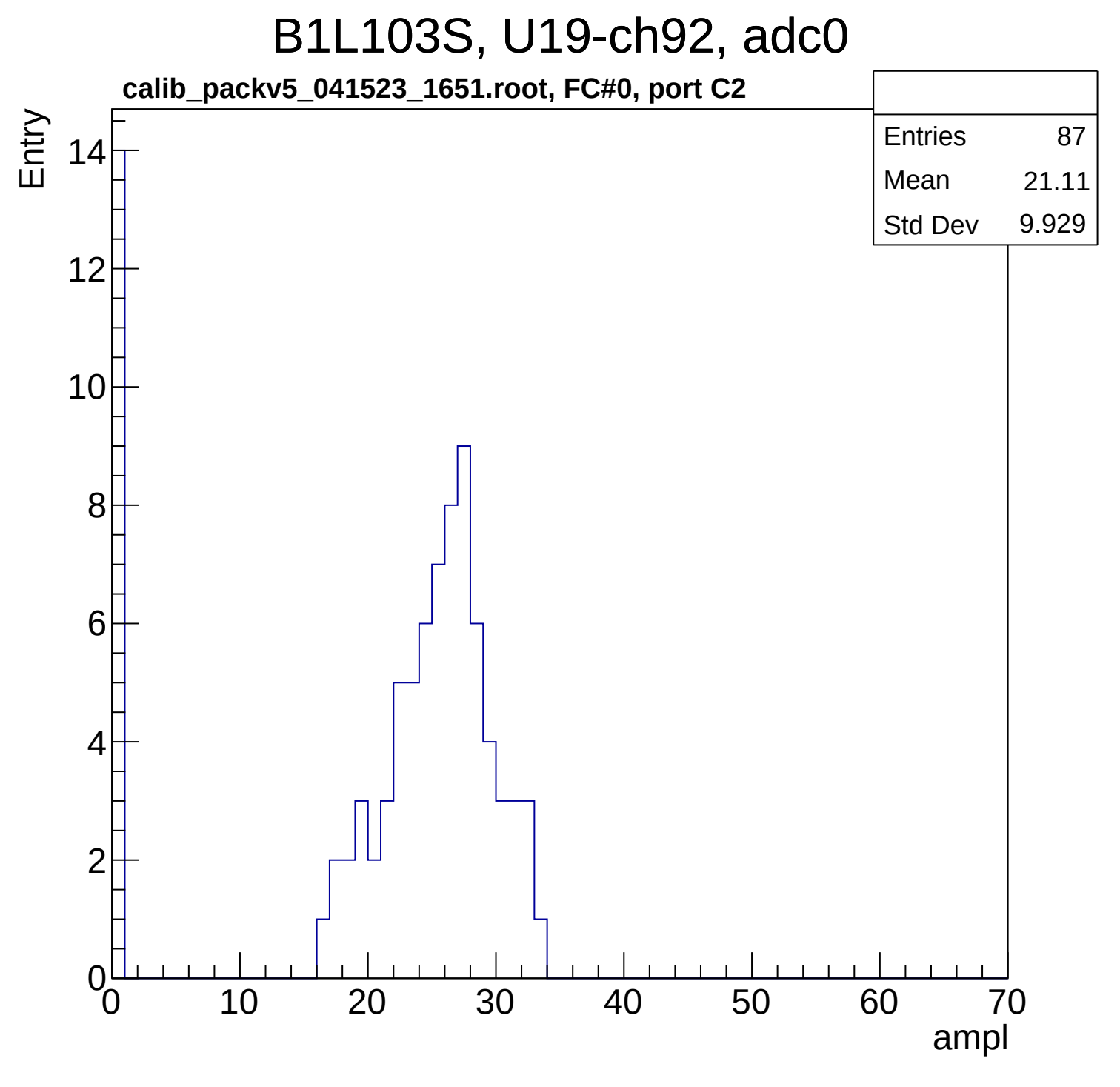
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch92, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 21.11
Std Dev 9.929
Entry
ampl
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2
4
6
8
10
12
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0
10
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40
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60
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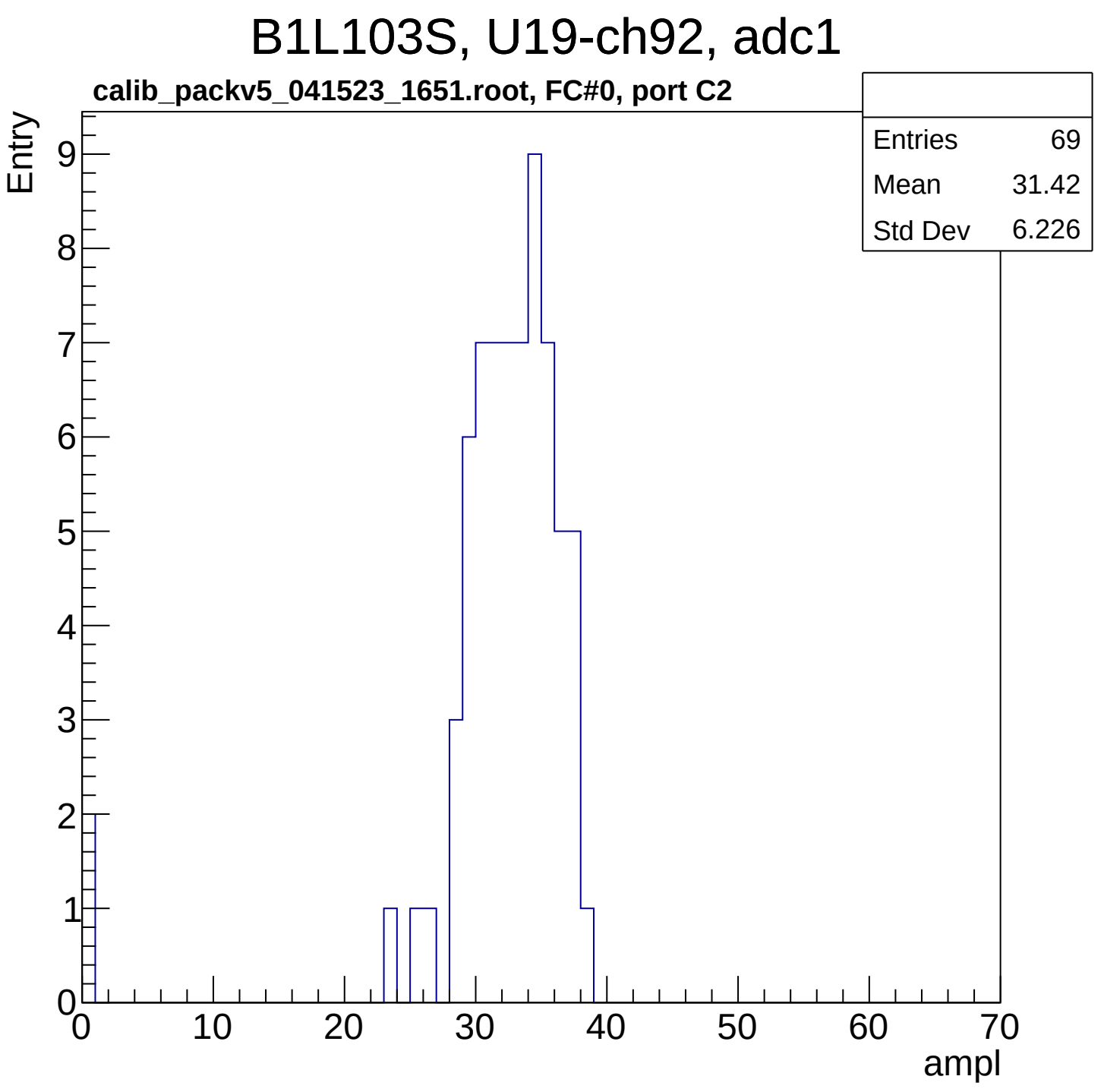
B1L103S, U19-ch92, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 31.42
Std Dev 6.226
Entry
ampl
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3
4
5
6
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0
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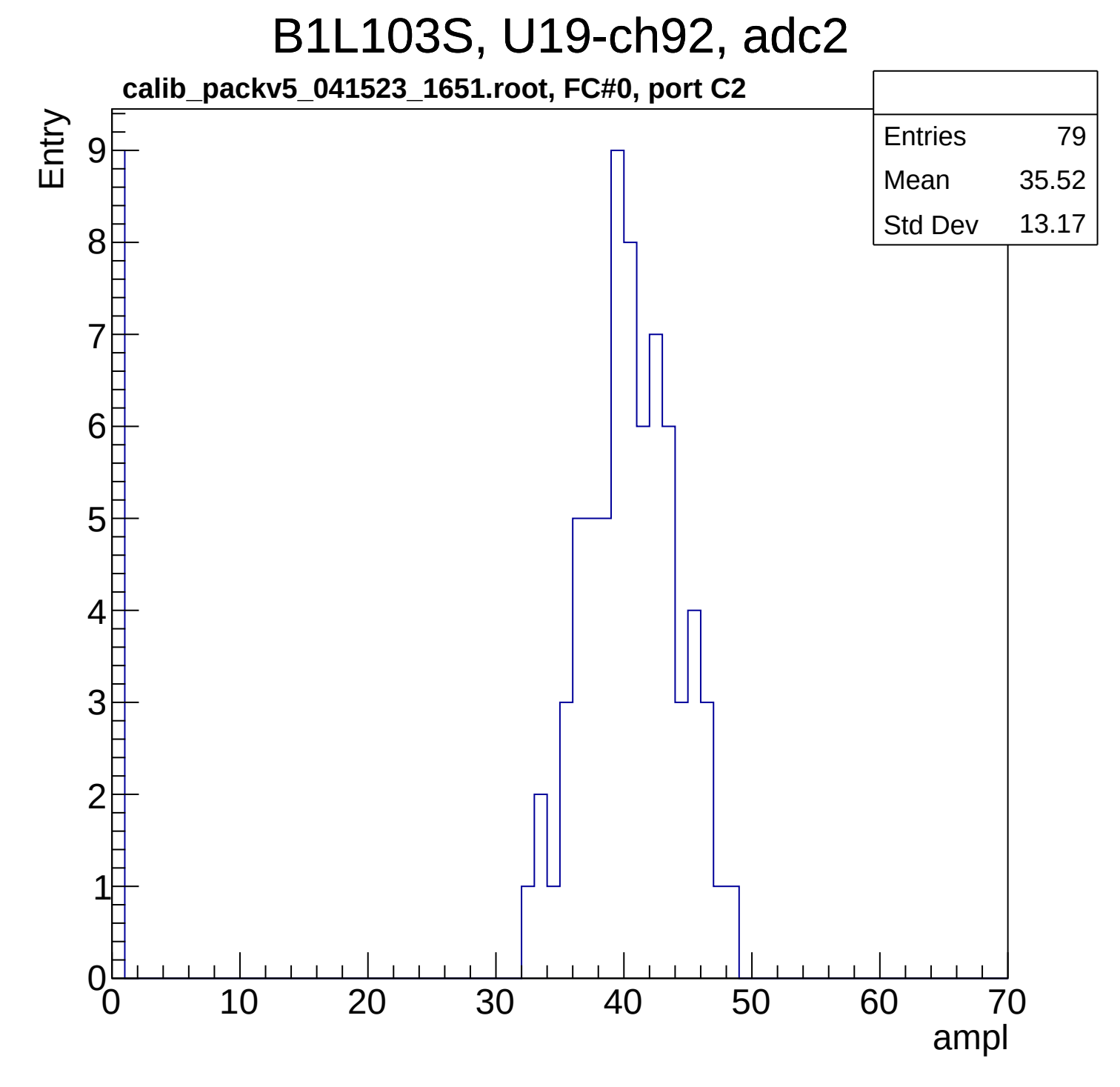
B1L103S, U19-ch92, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 35.52
Std Dev 13.17
Entry
ampl
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2
3
4
5
6
7
8
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0
10
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40
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60
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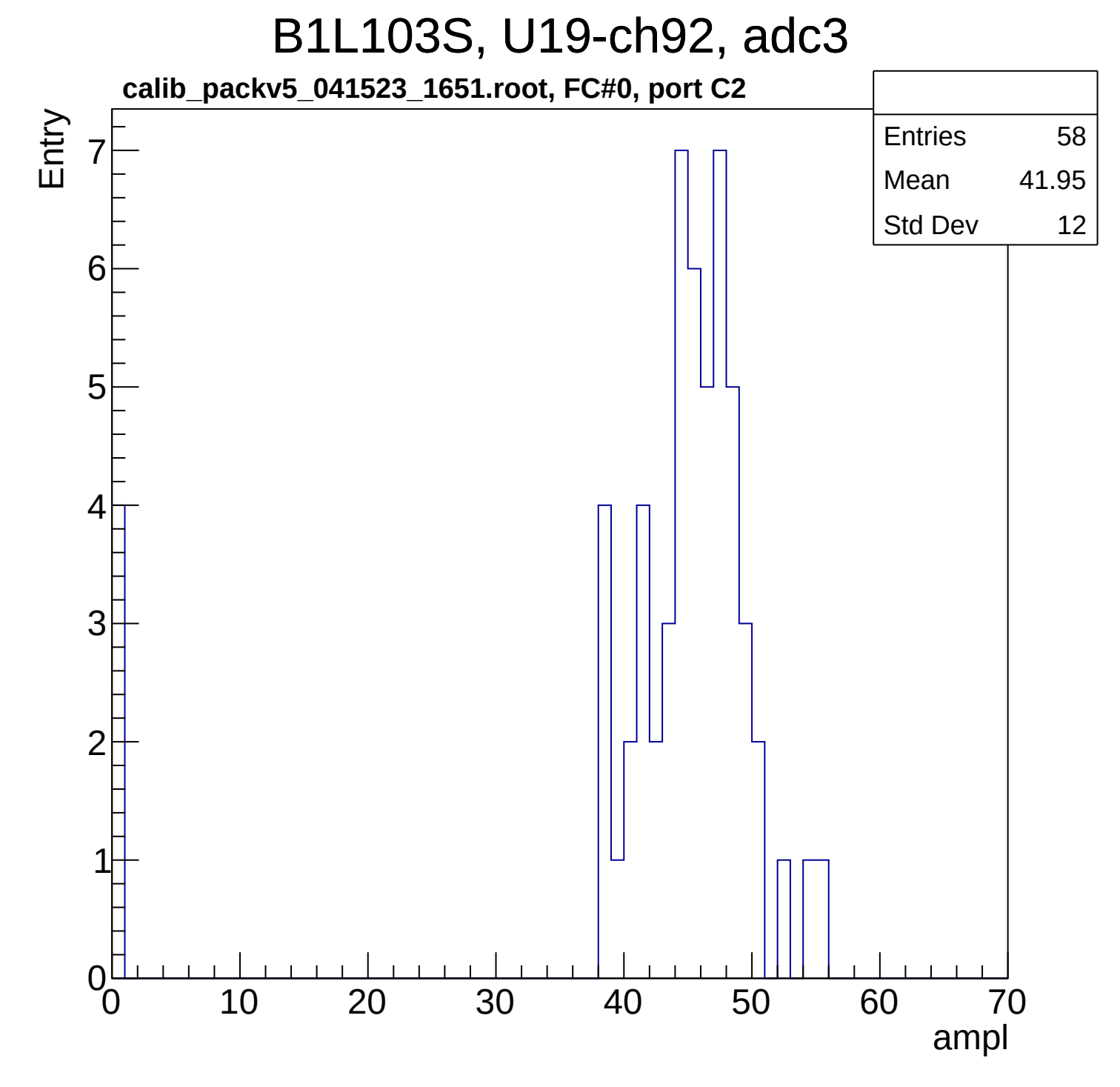
B1L103S, U19-ch92, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 41.95
Std Dev 12
Entry
ampl
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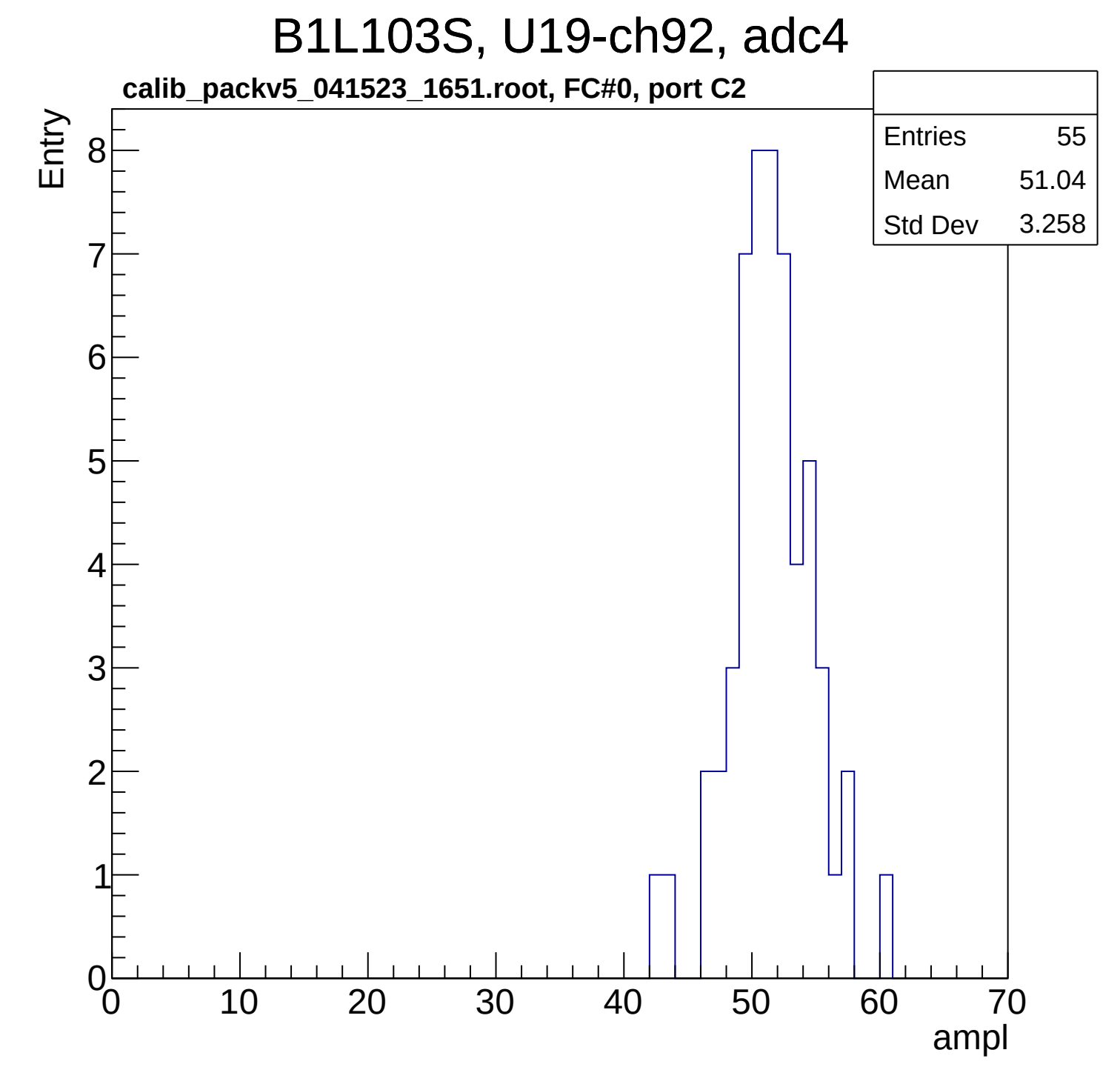
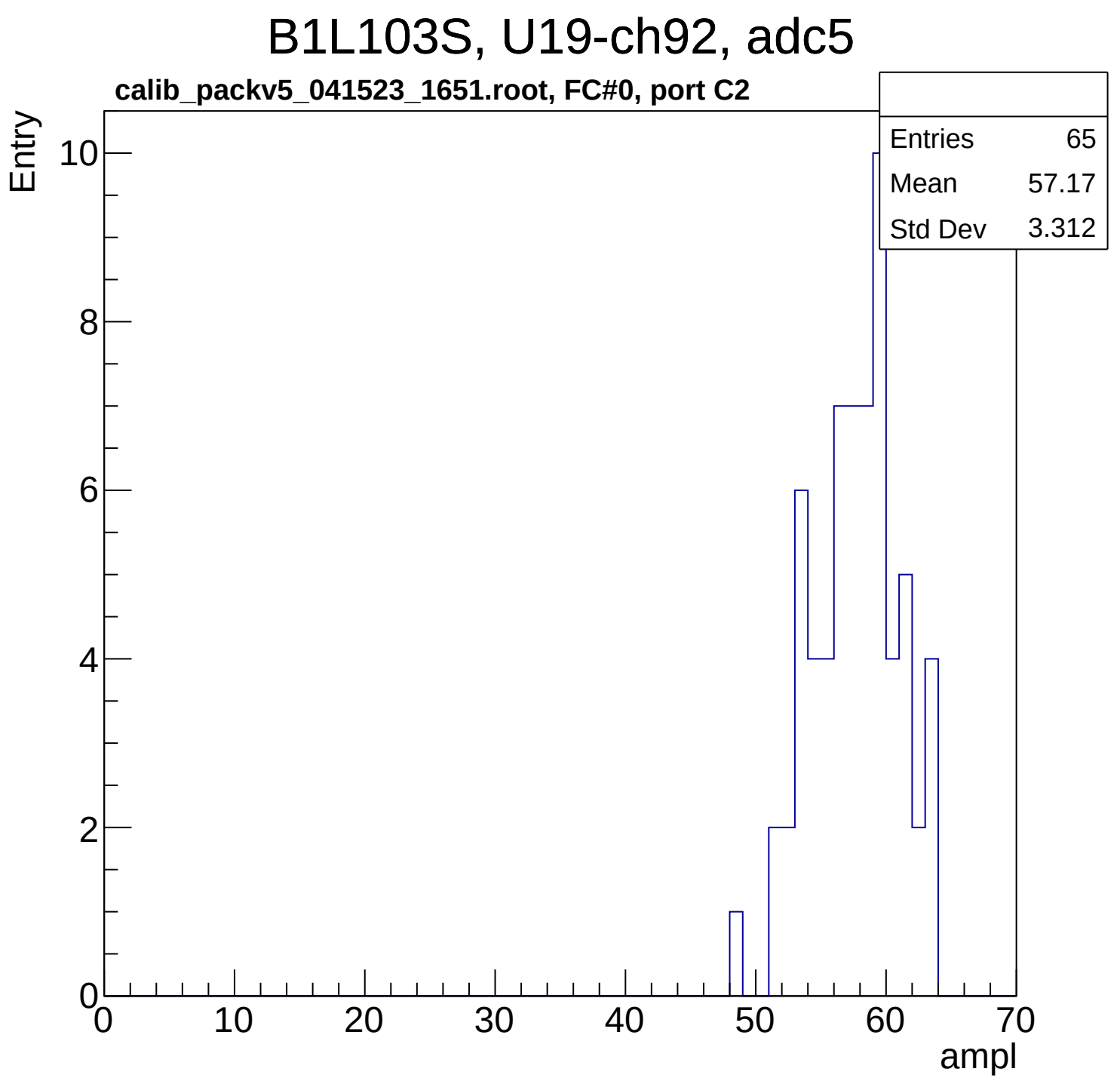
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch92, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 51.04
Std Dev 3.258
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch92, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 57.17
Std Dev 3.312
Entry
0
2
4
6
8
10
0
10
20
30
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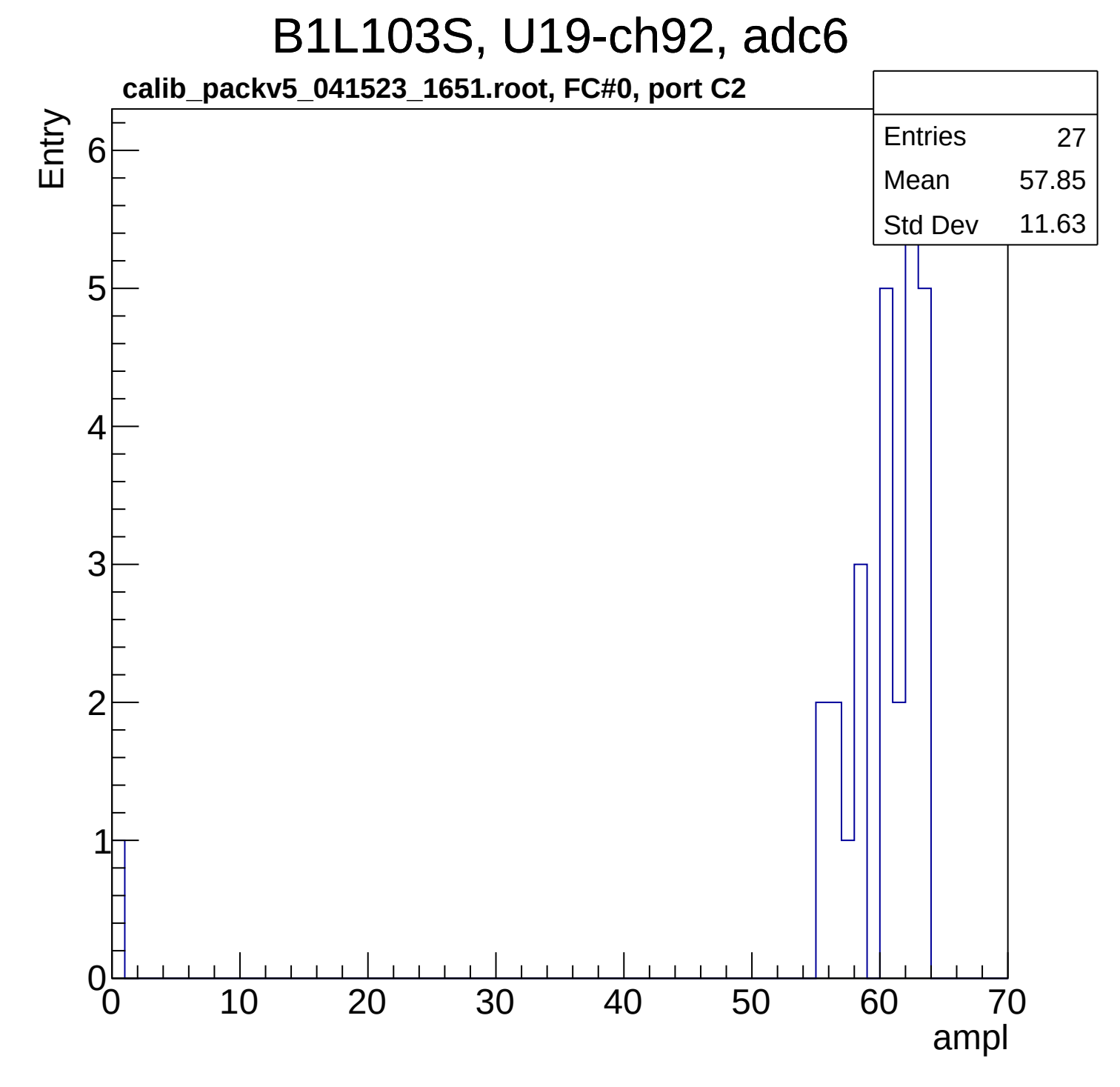
50
60
70
ampl


B1L103S, U19-ch92, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 57.85
Std Dev 11.63
Entry
ampl
0
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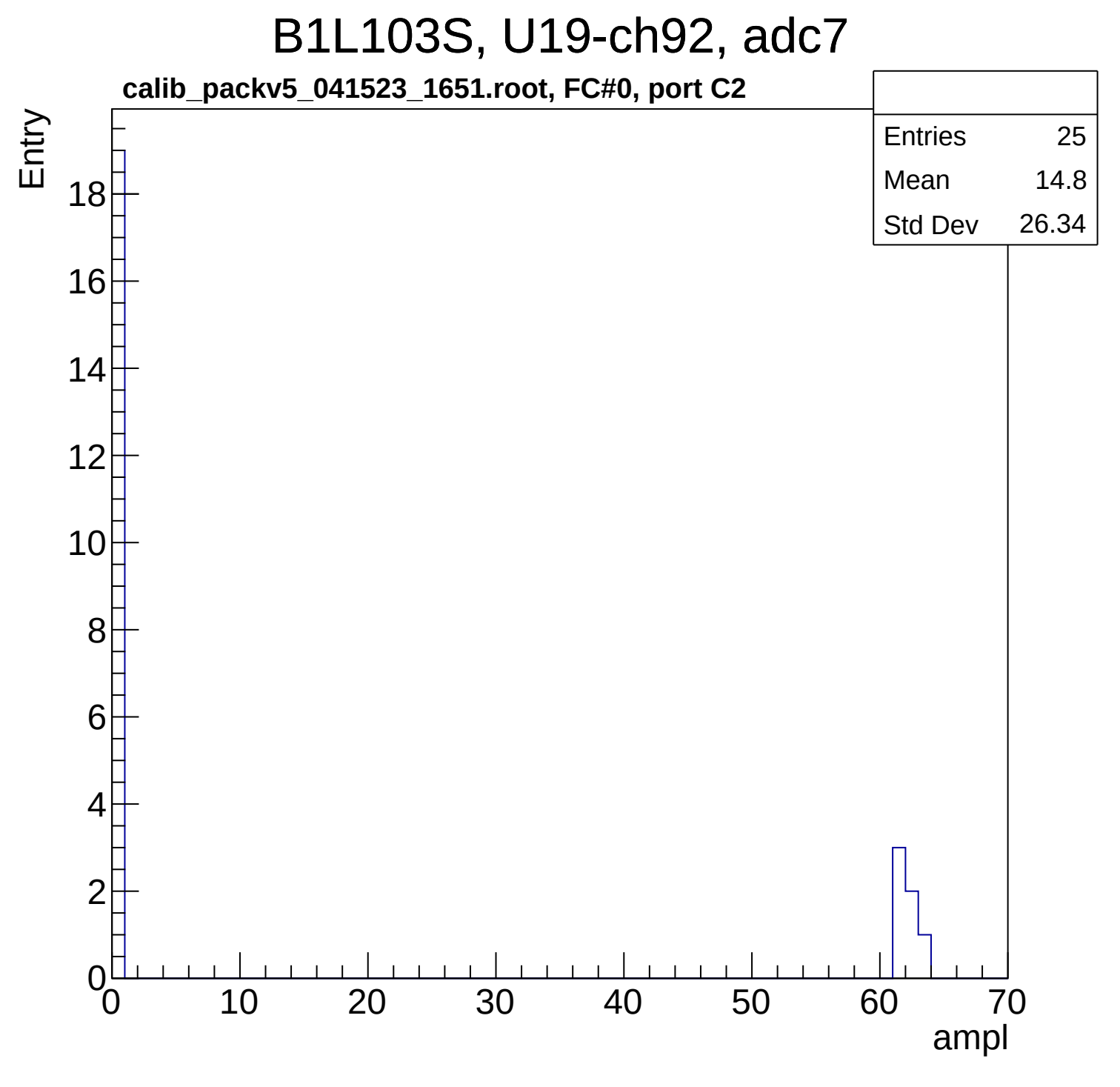
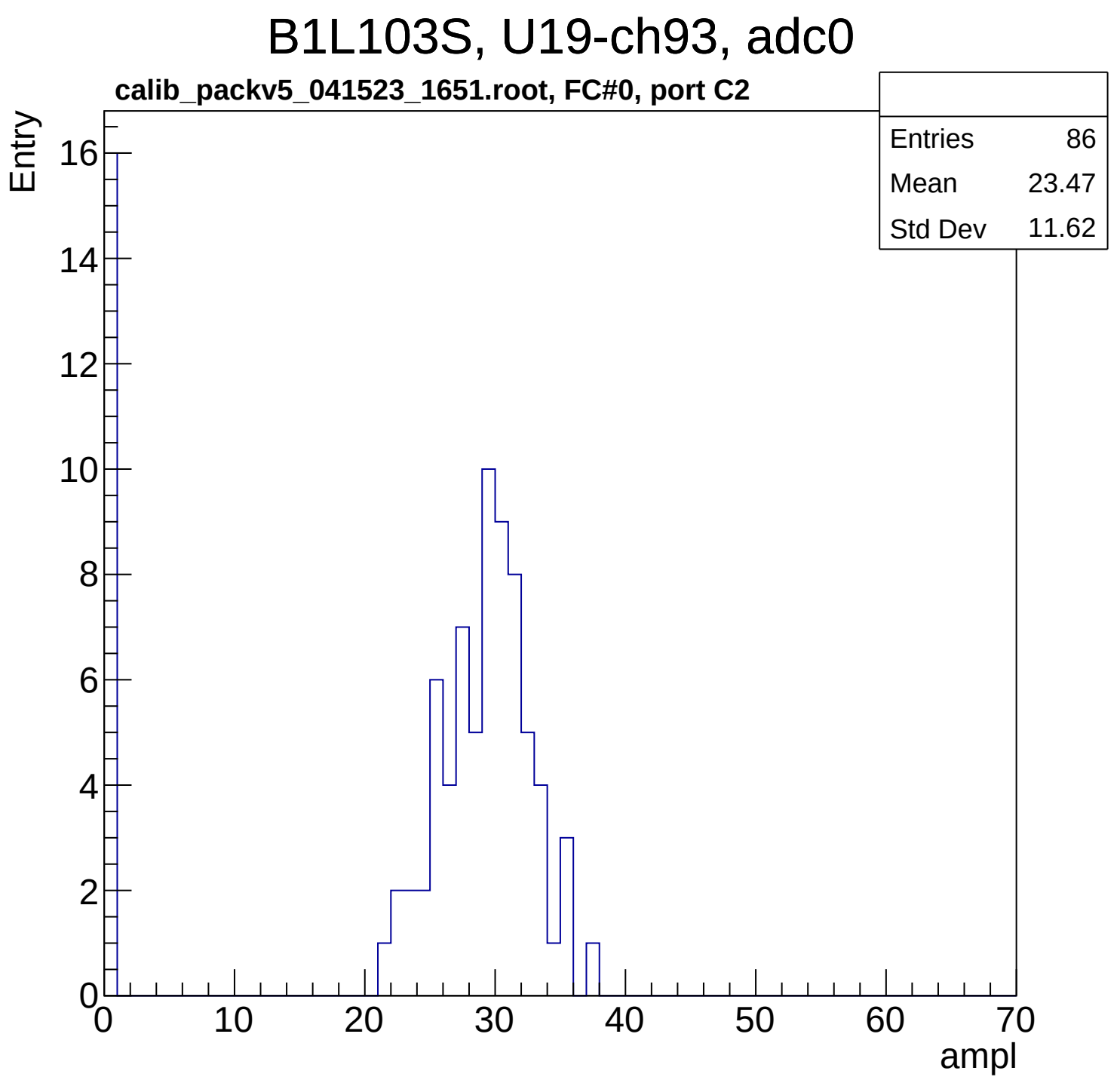
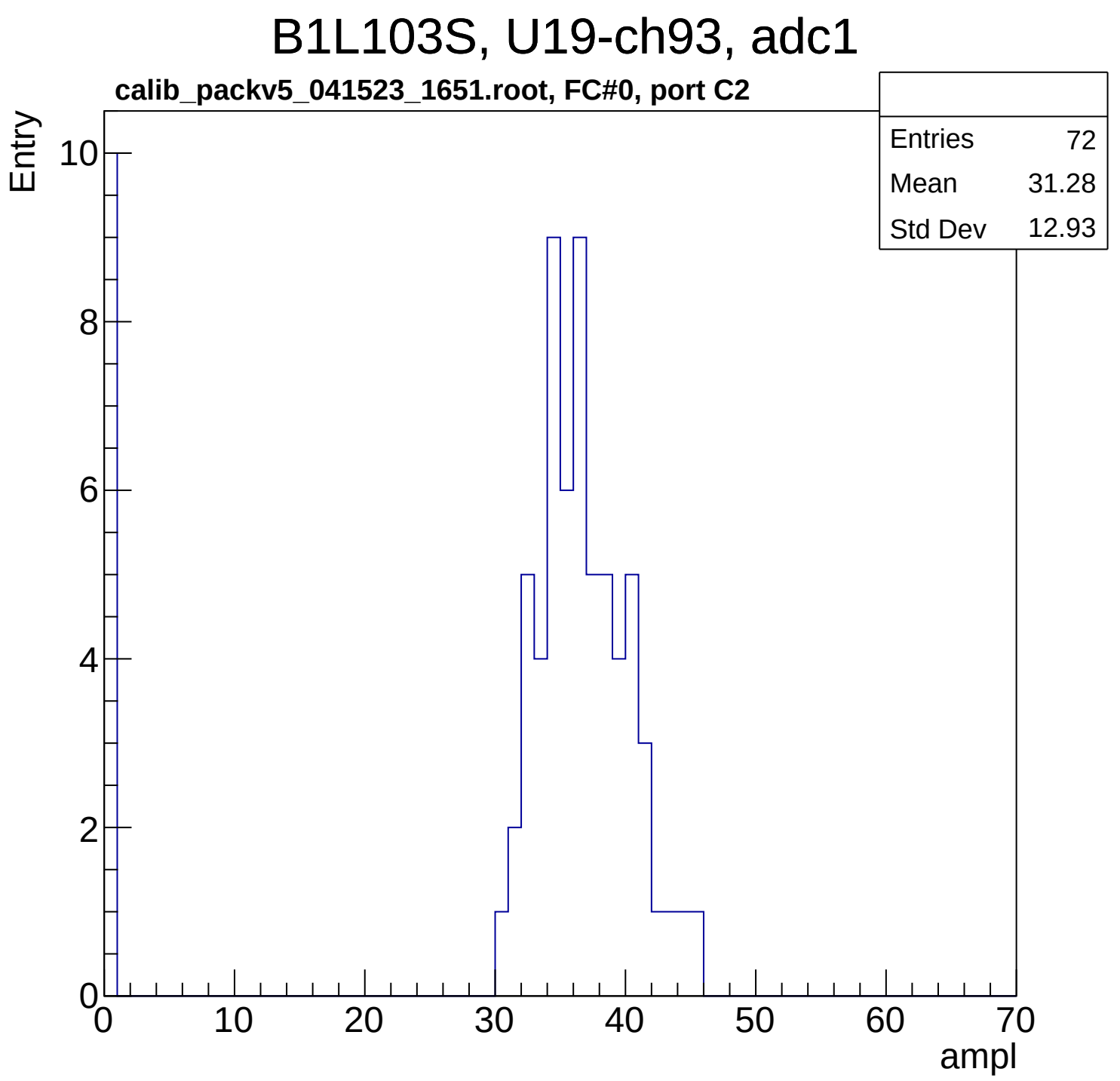
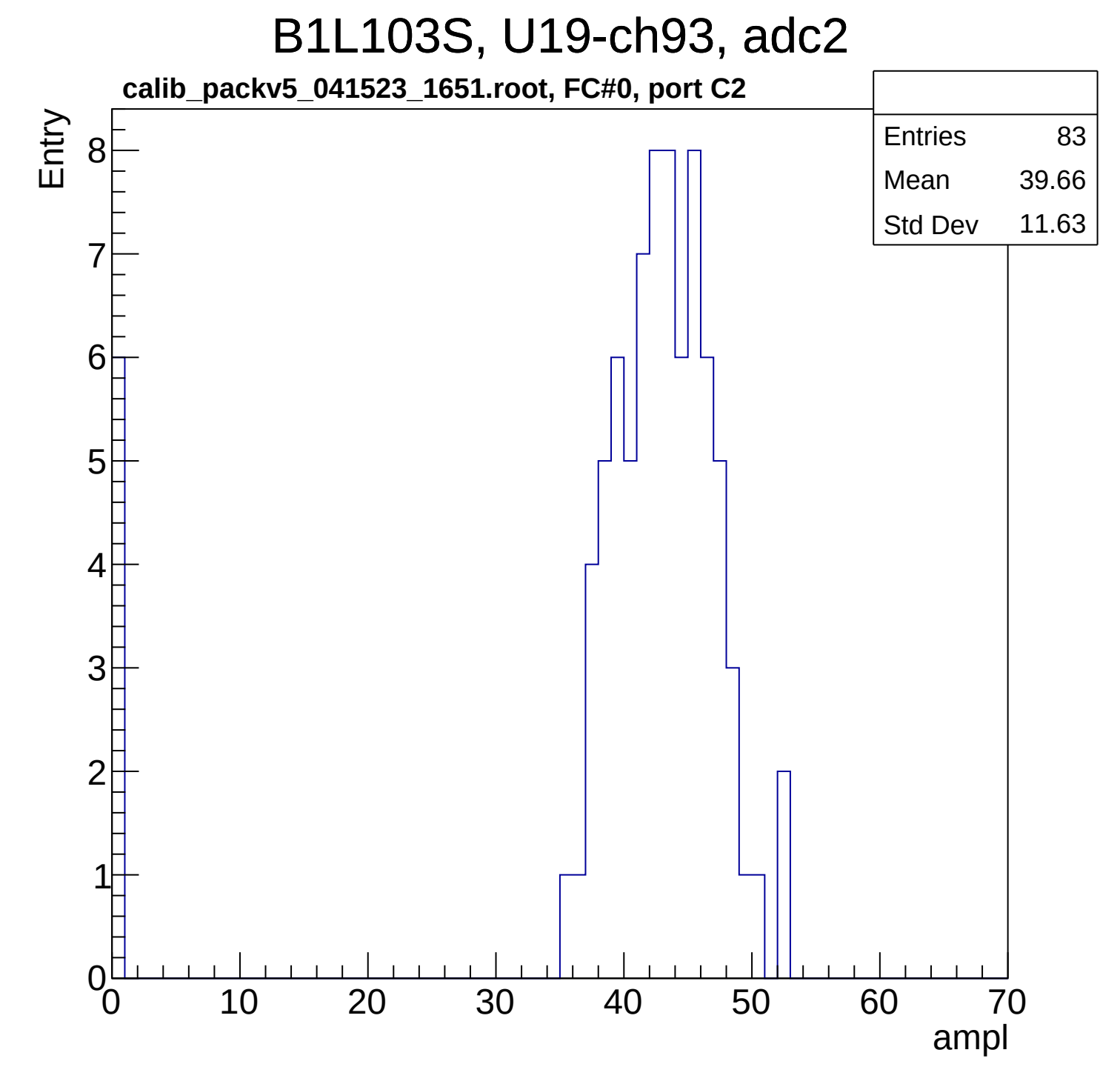
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U19-ch92, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 14.8
Std Dev 26.34
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch93, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 23.47
Std Dev 11.62
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch93, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 31.28
Std Dev 12.93
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch93, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 39.66
Std Dev 11.63
Entry
ampl
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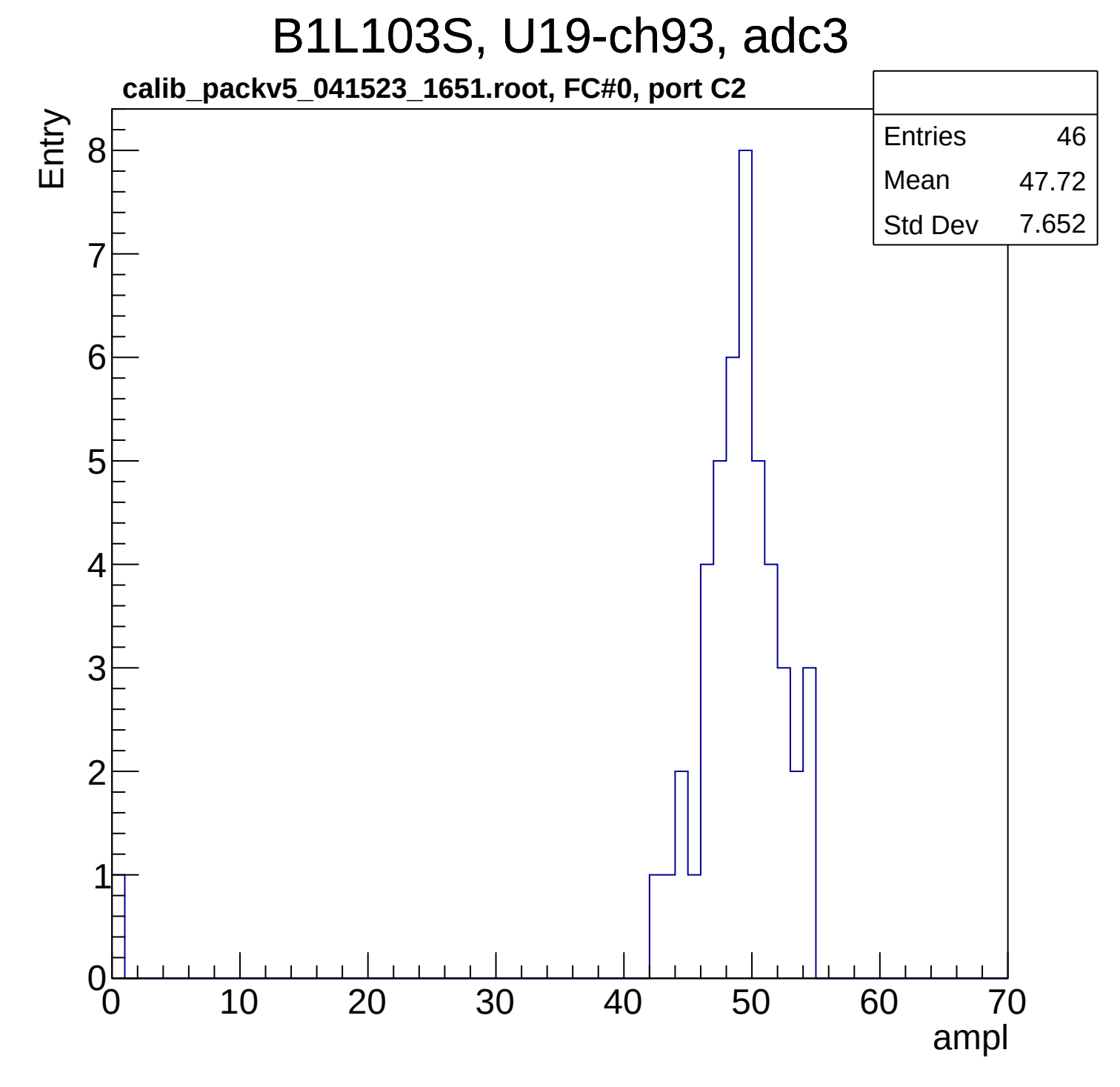
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch93, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 47.72
Std Dev 7.652
Entry
ampl
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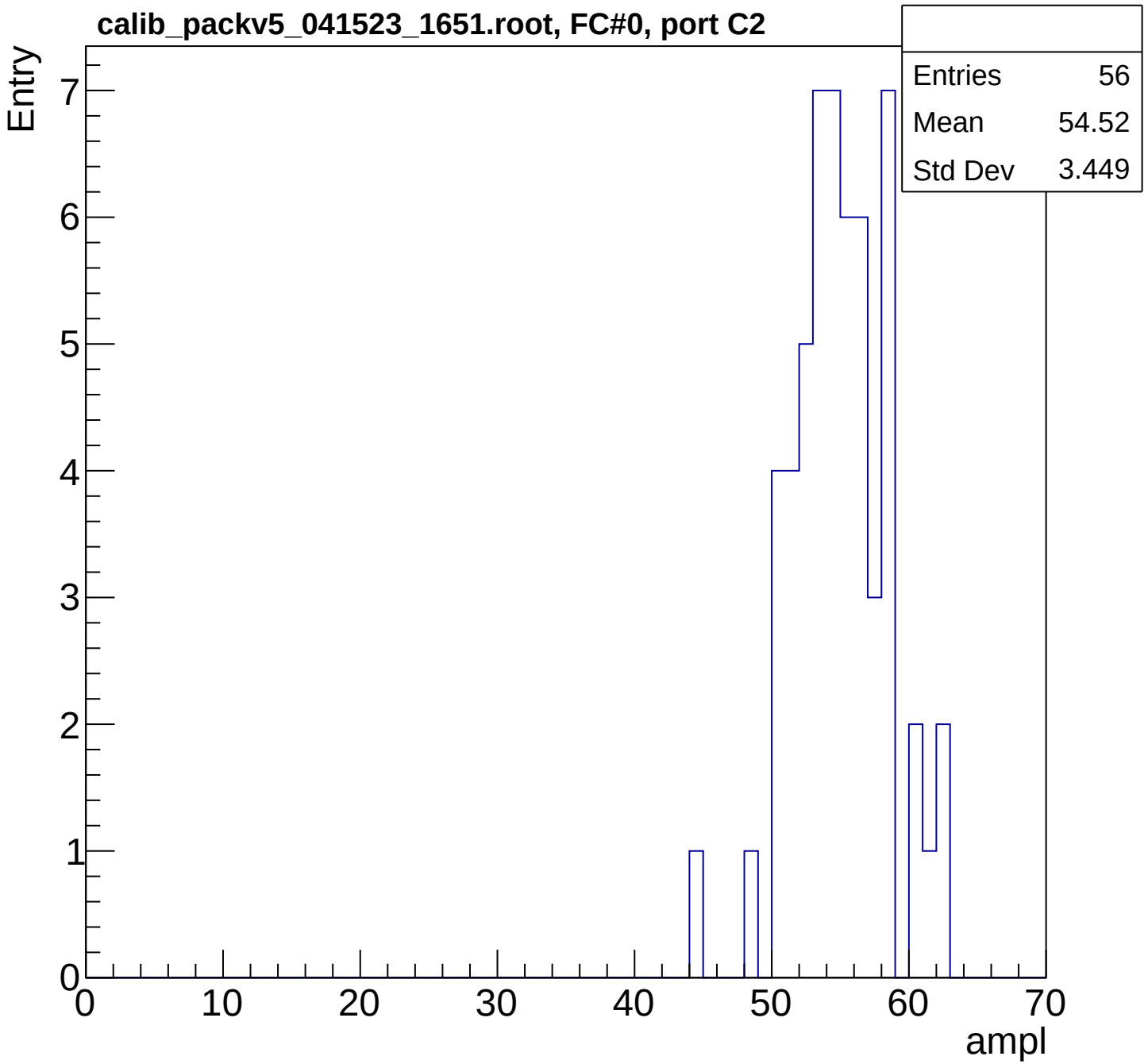
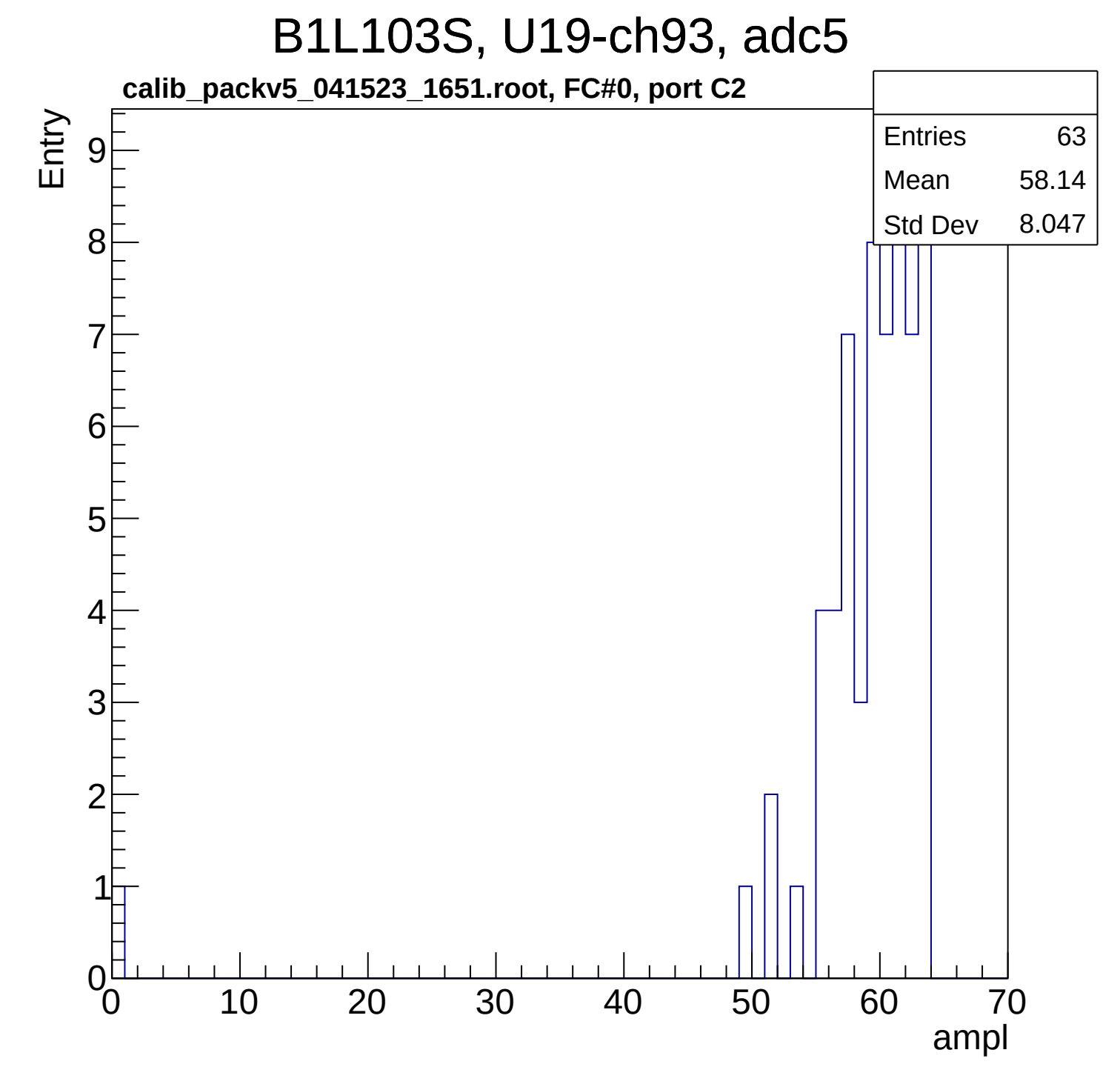
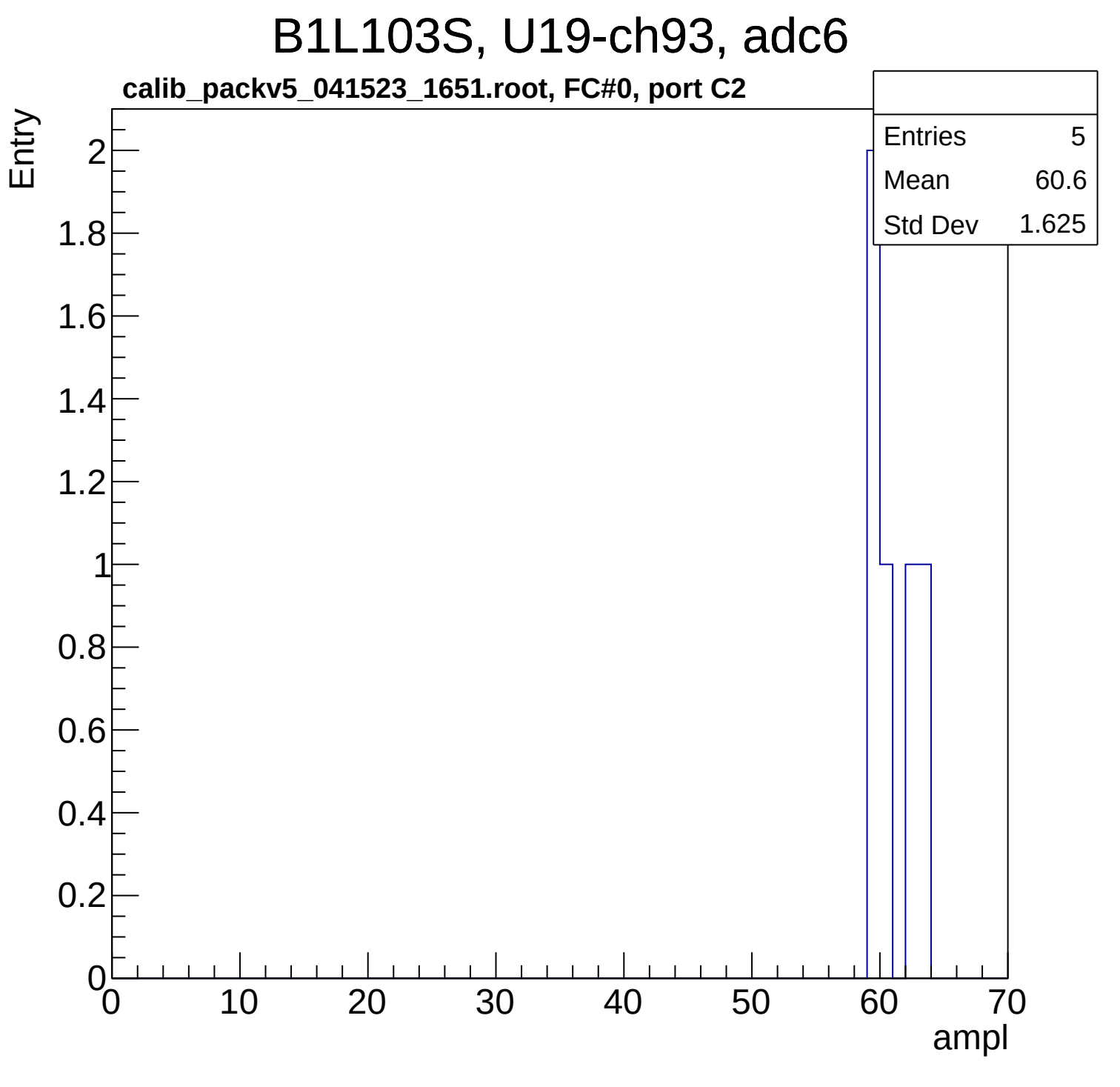
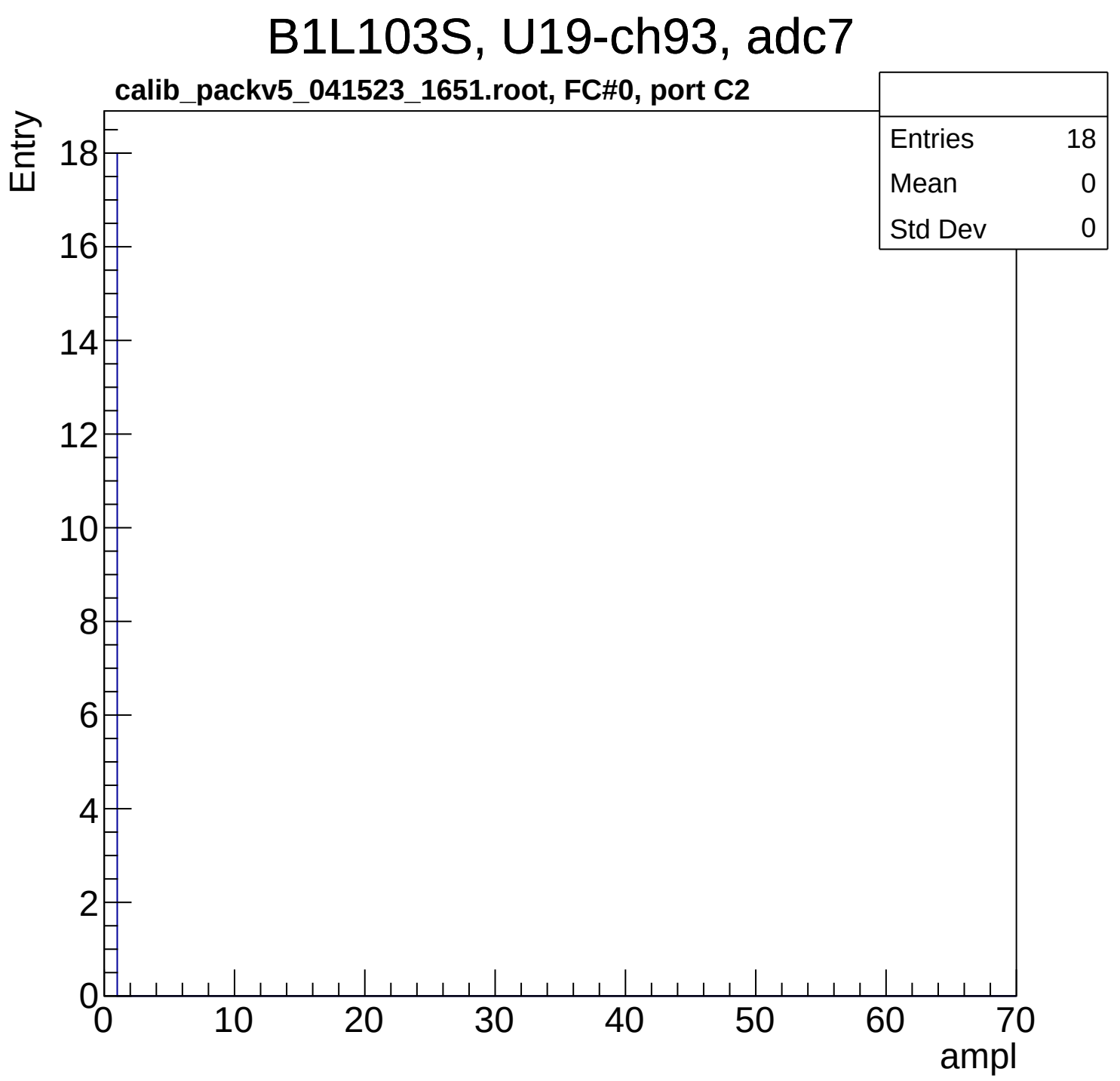
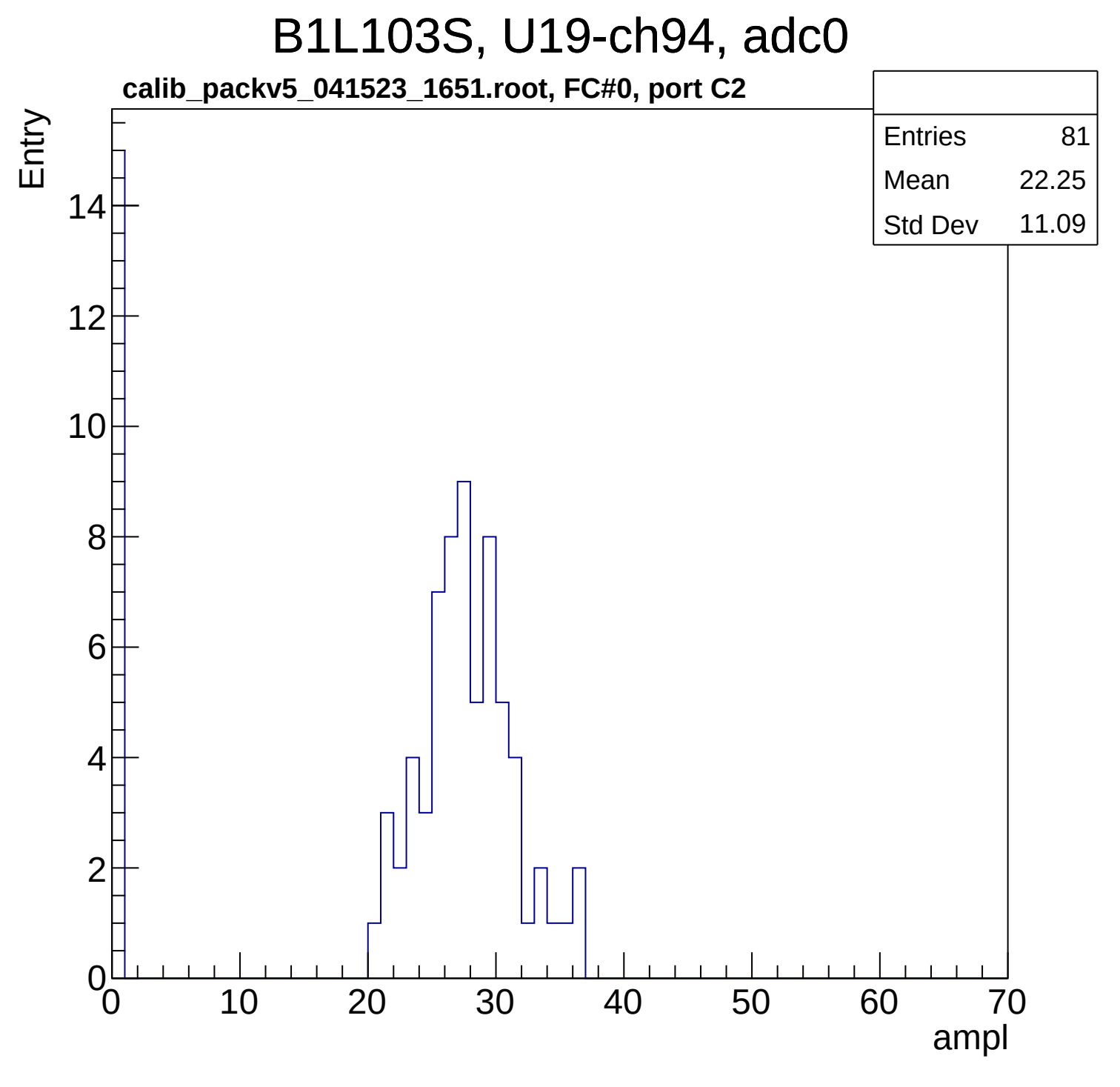
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

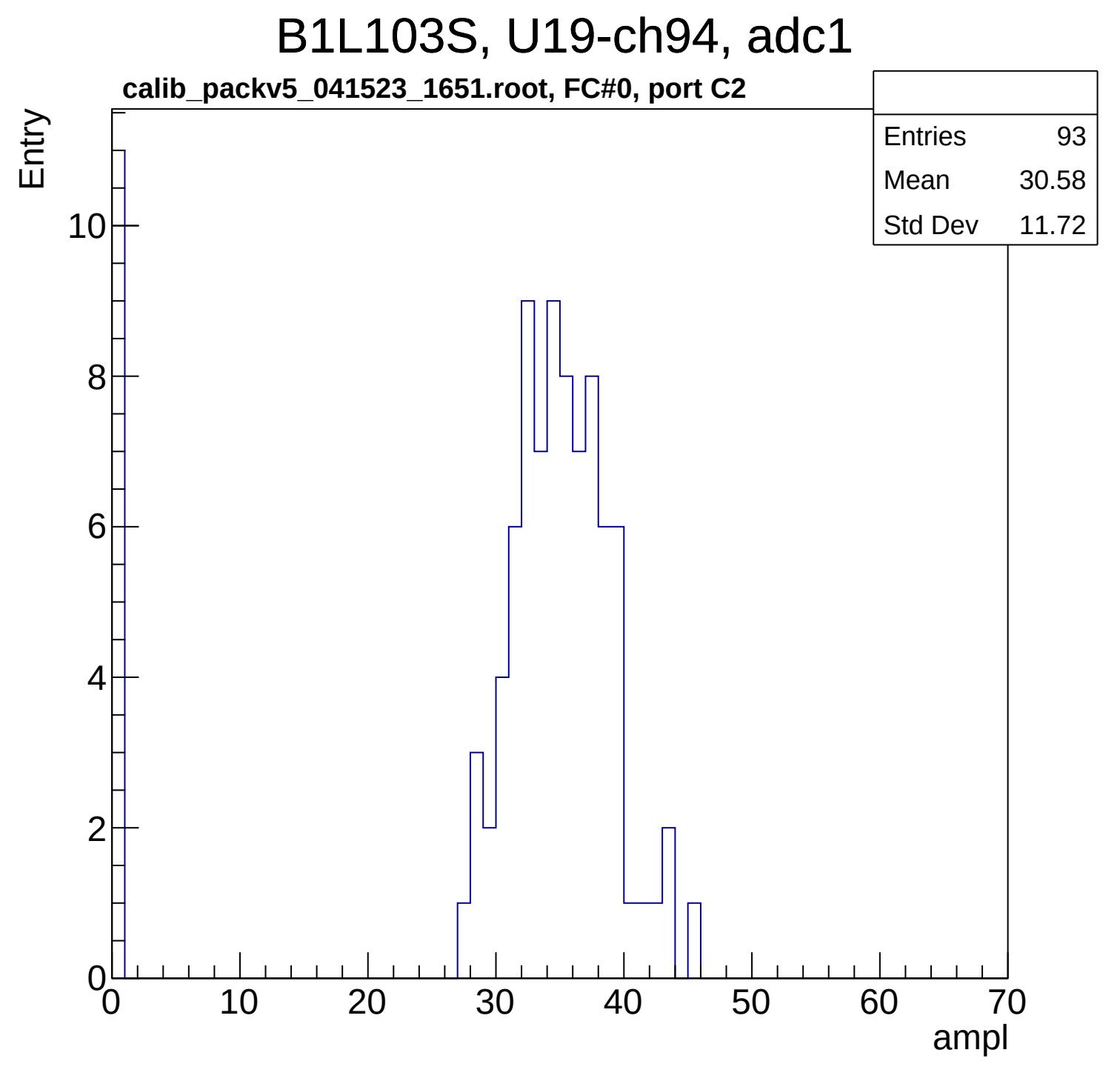

B1L103S, U19-ch93, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 54.52
Std Dev 3.449
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

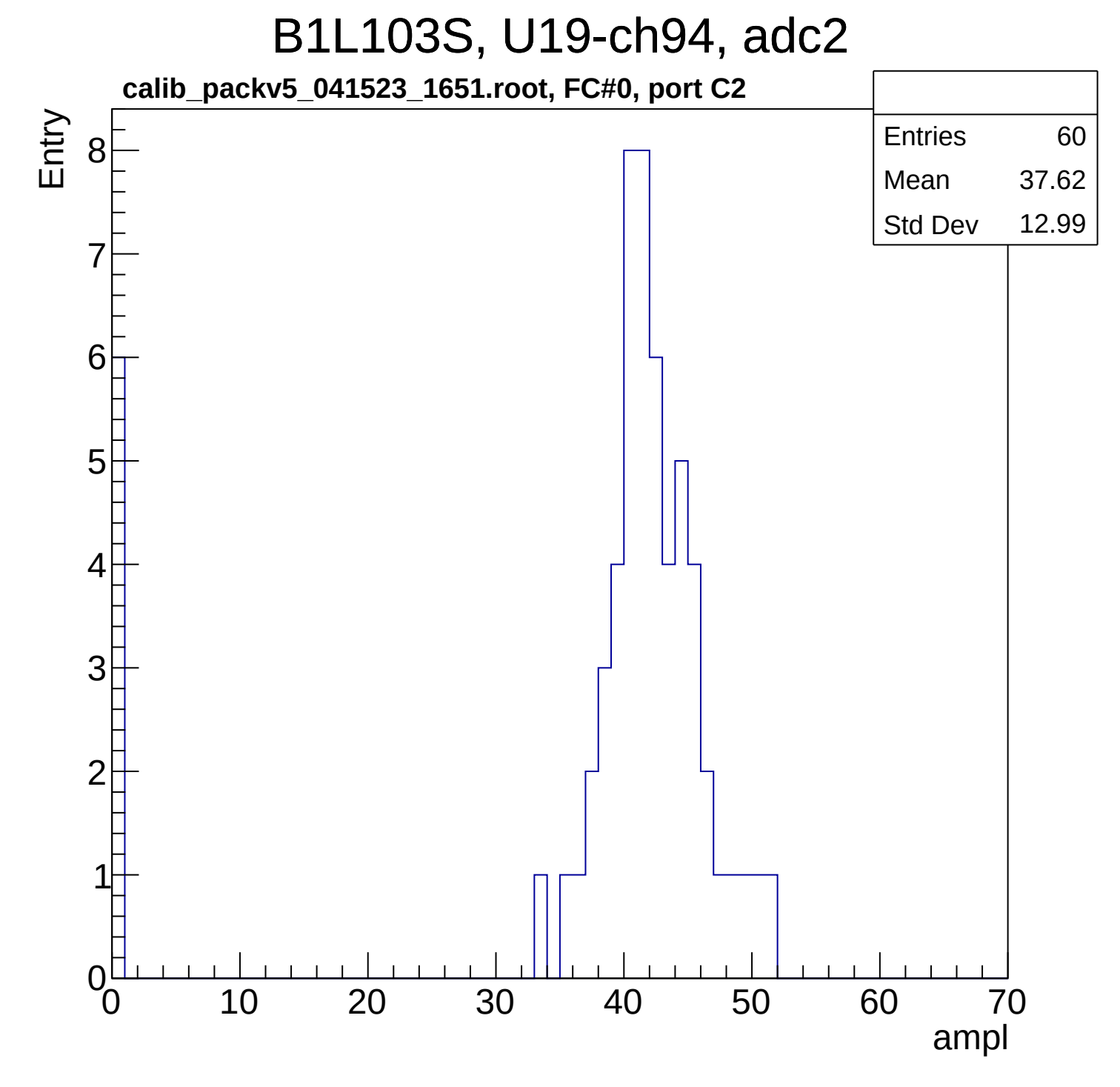

B1L103S, U19-ch93, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 58.14
Std Dev 8.047
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

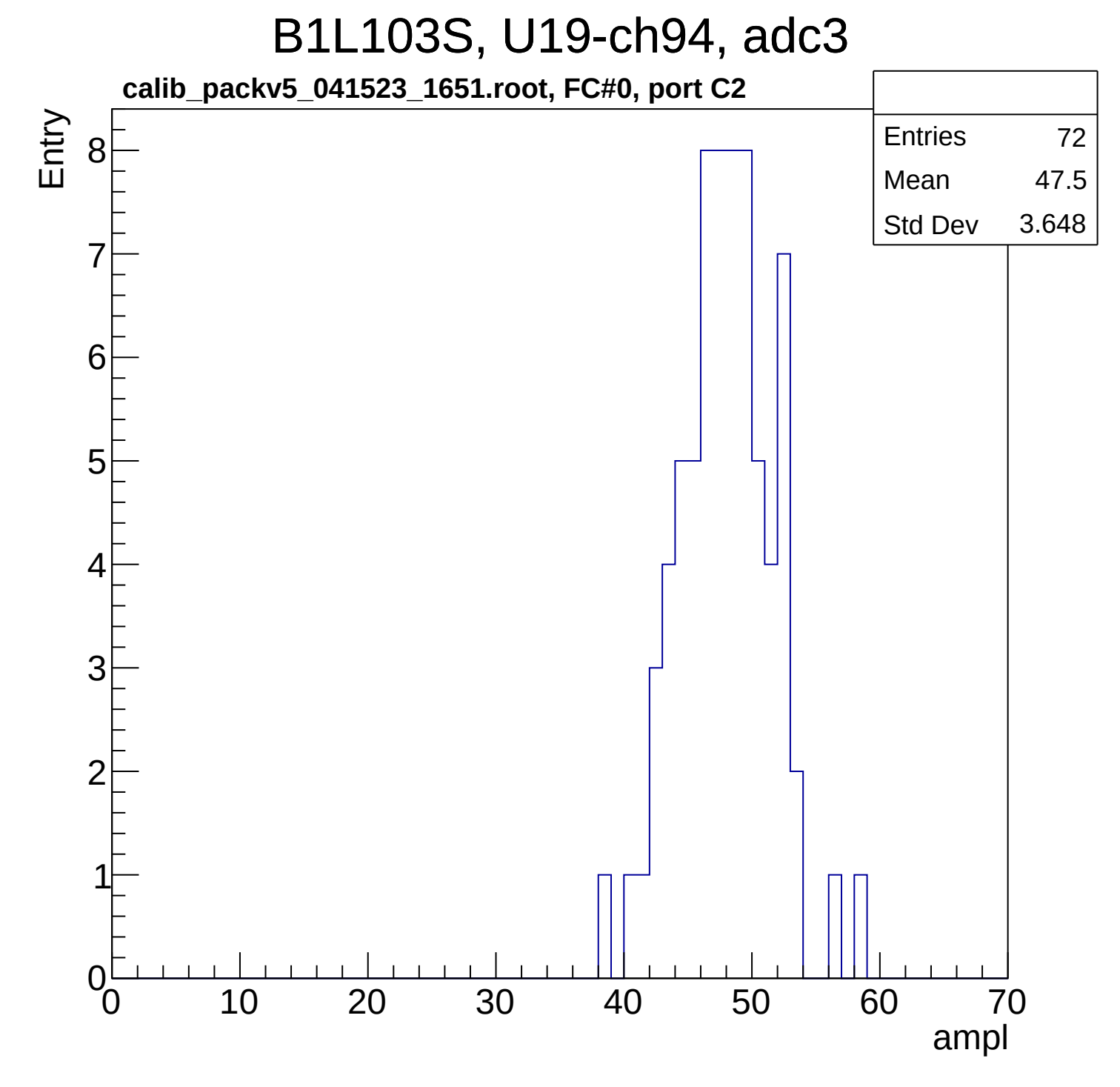

B1L103S, U19-ch93, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 60.6
Std Dev 1.625
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

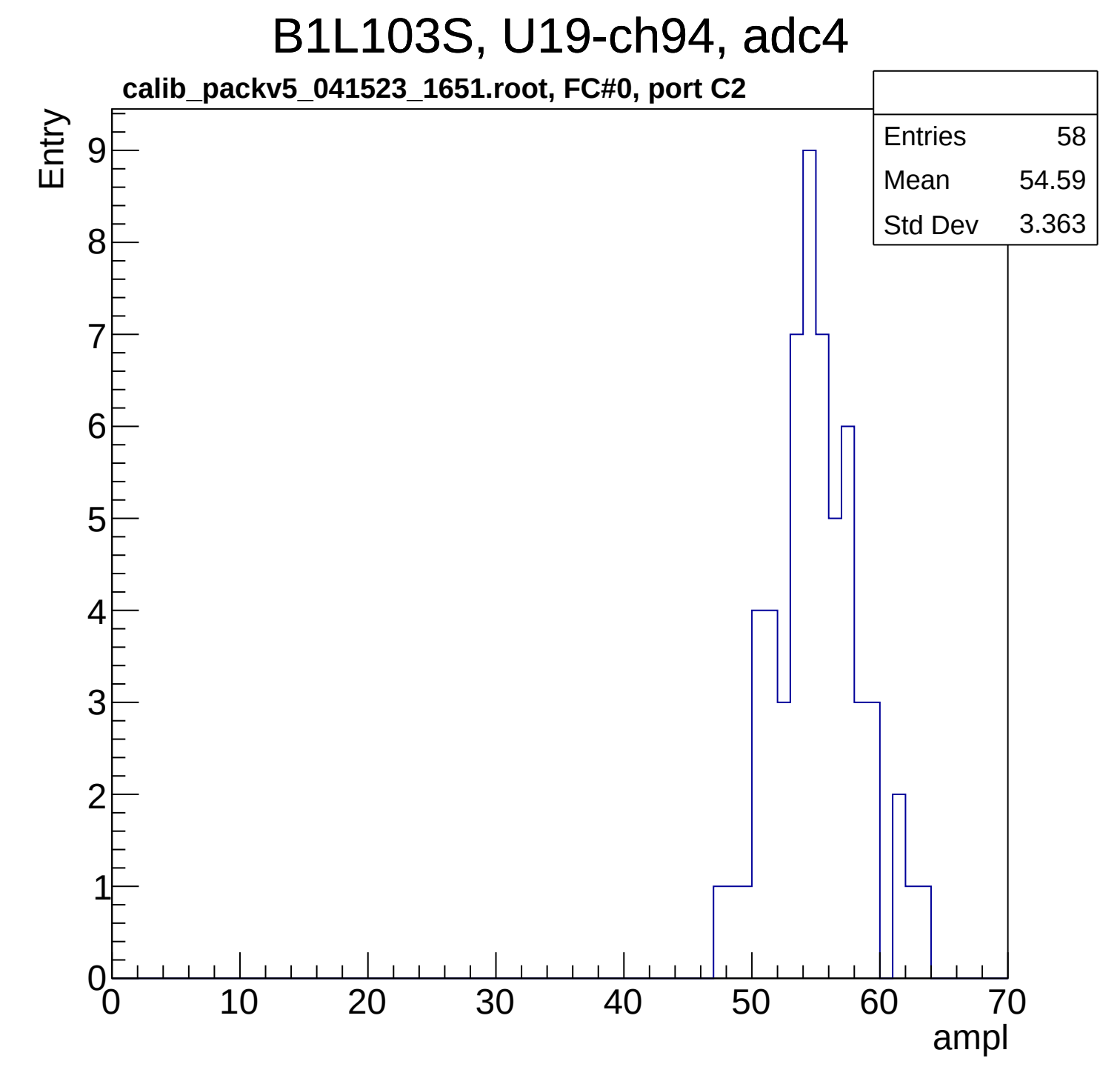

B1L103S, U19-ch93, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

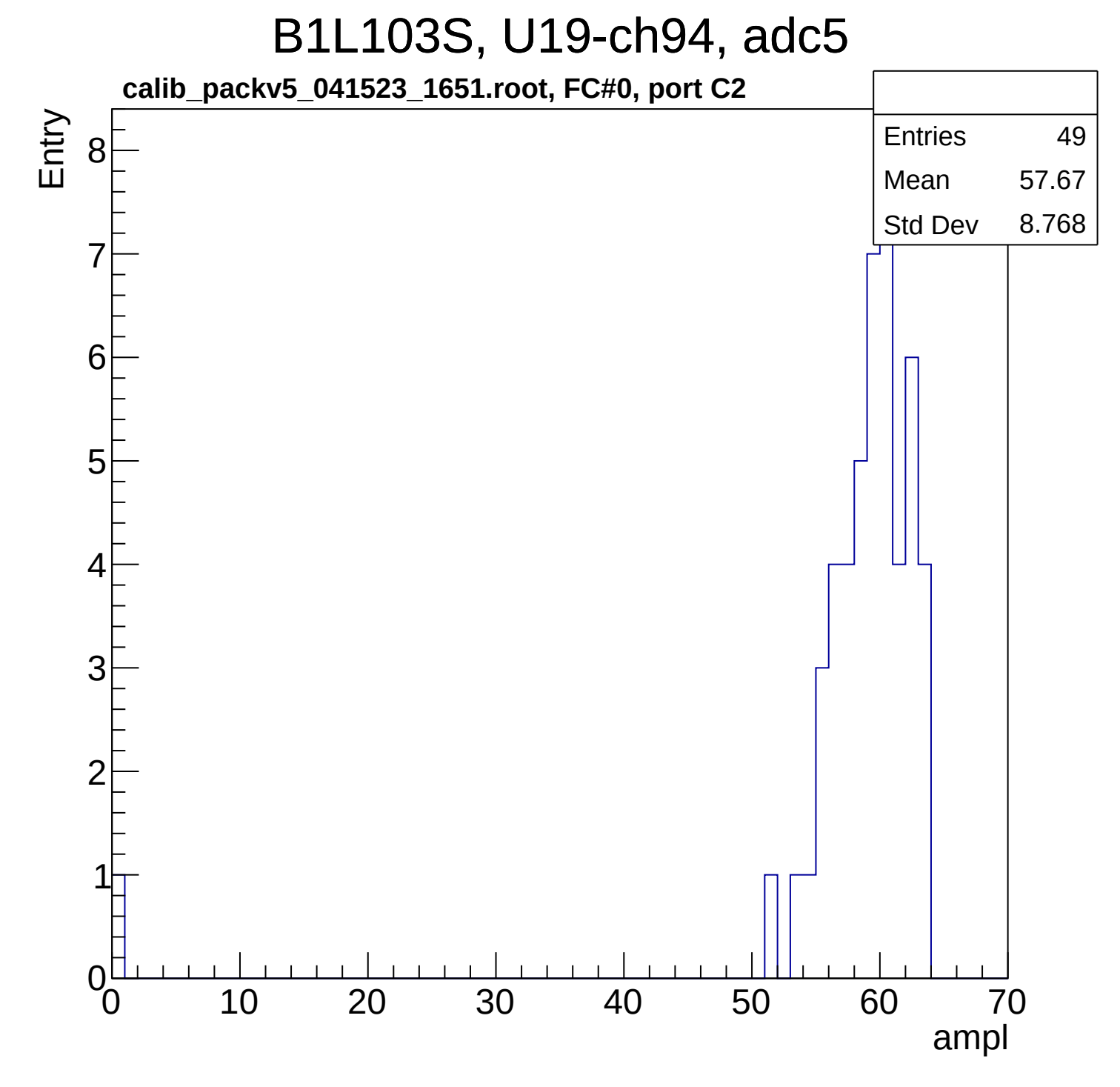

B1L103S, U19-ch94, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 22.25
Std Dev 11.09
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

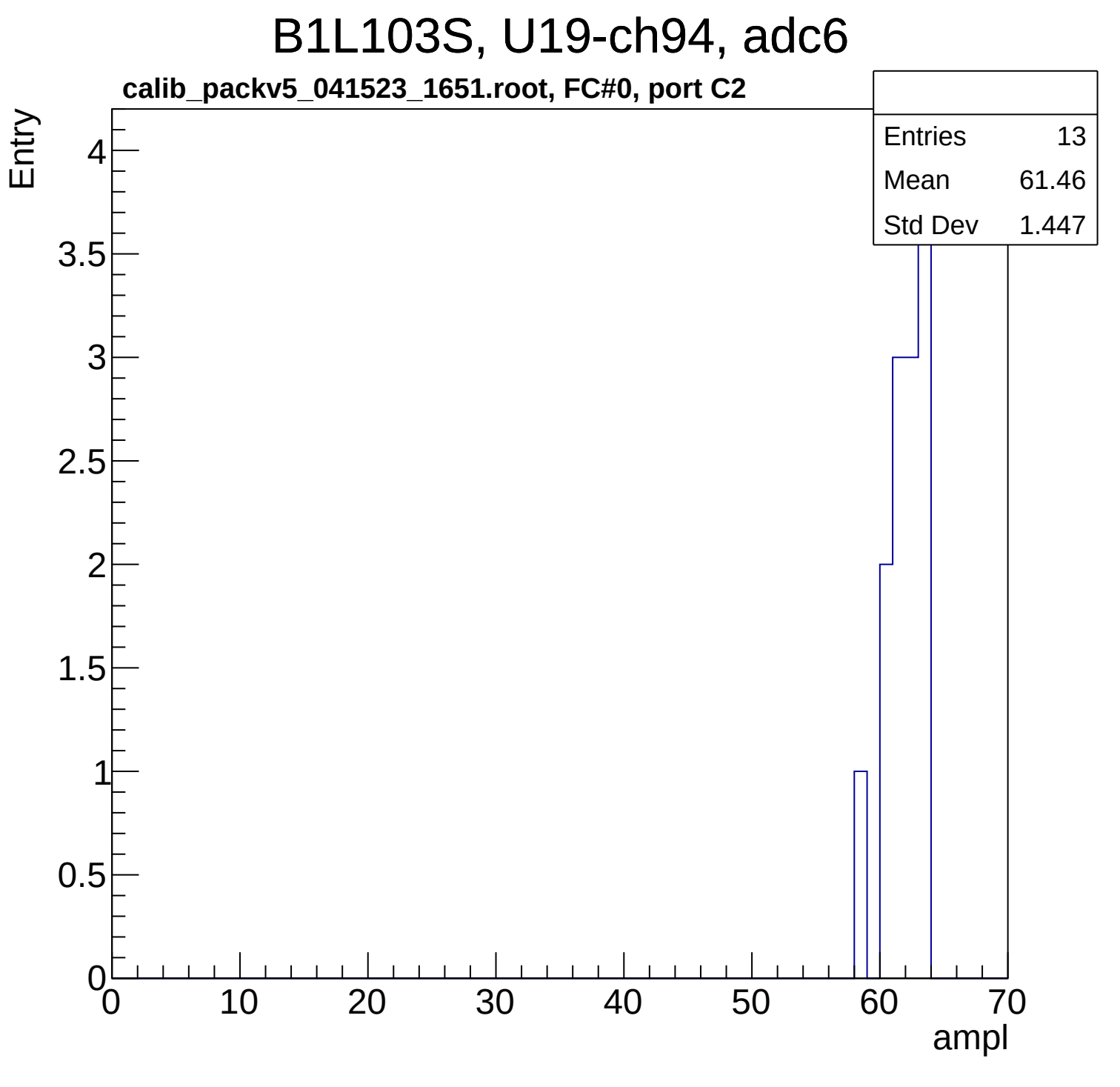

B1L103S, U19-ch94, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 30.58
Std Dev 11.72
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

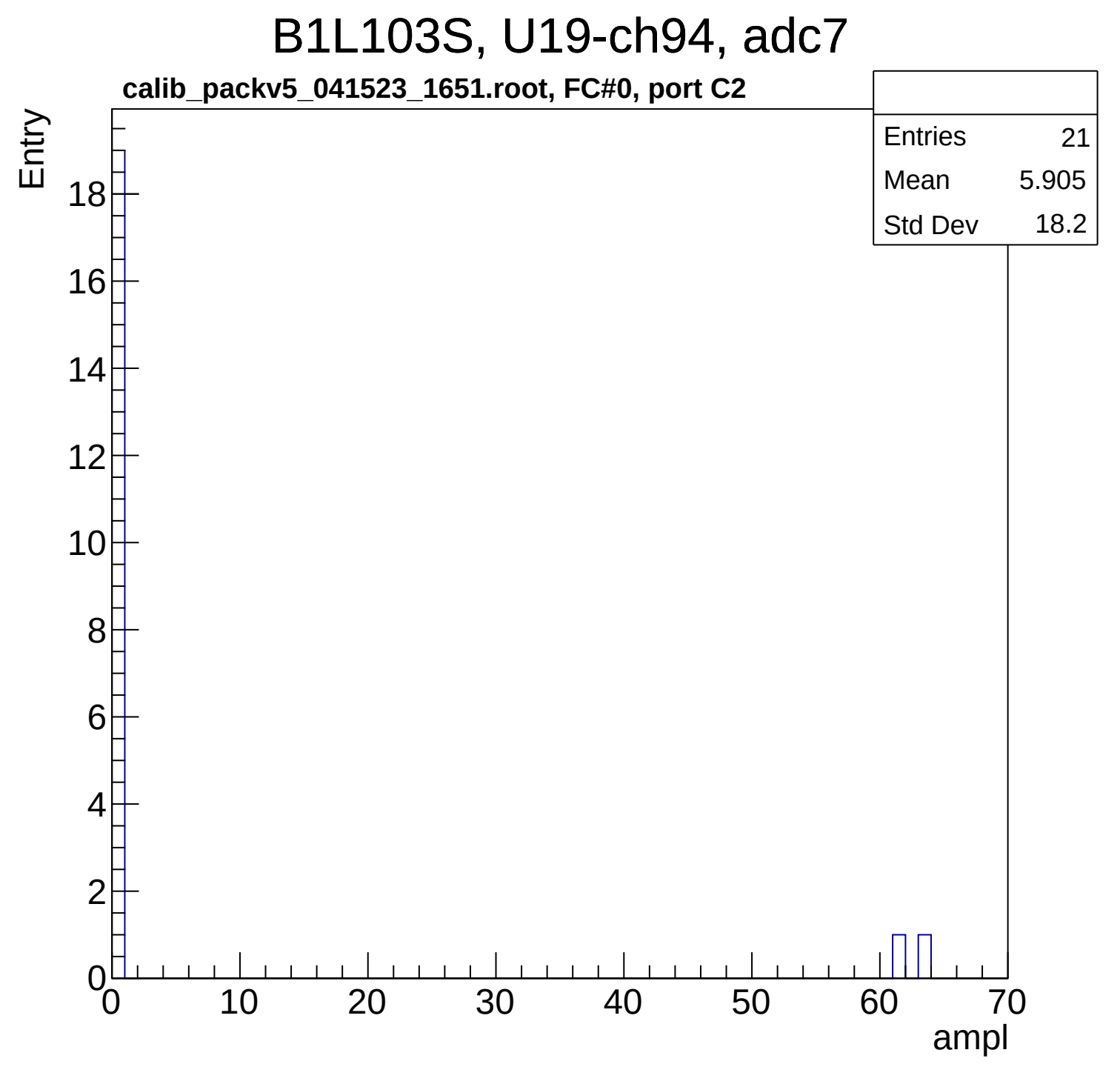

B1L103S, U19-ch94, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 37.62
Std Dev 12.99
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

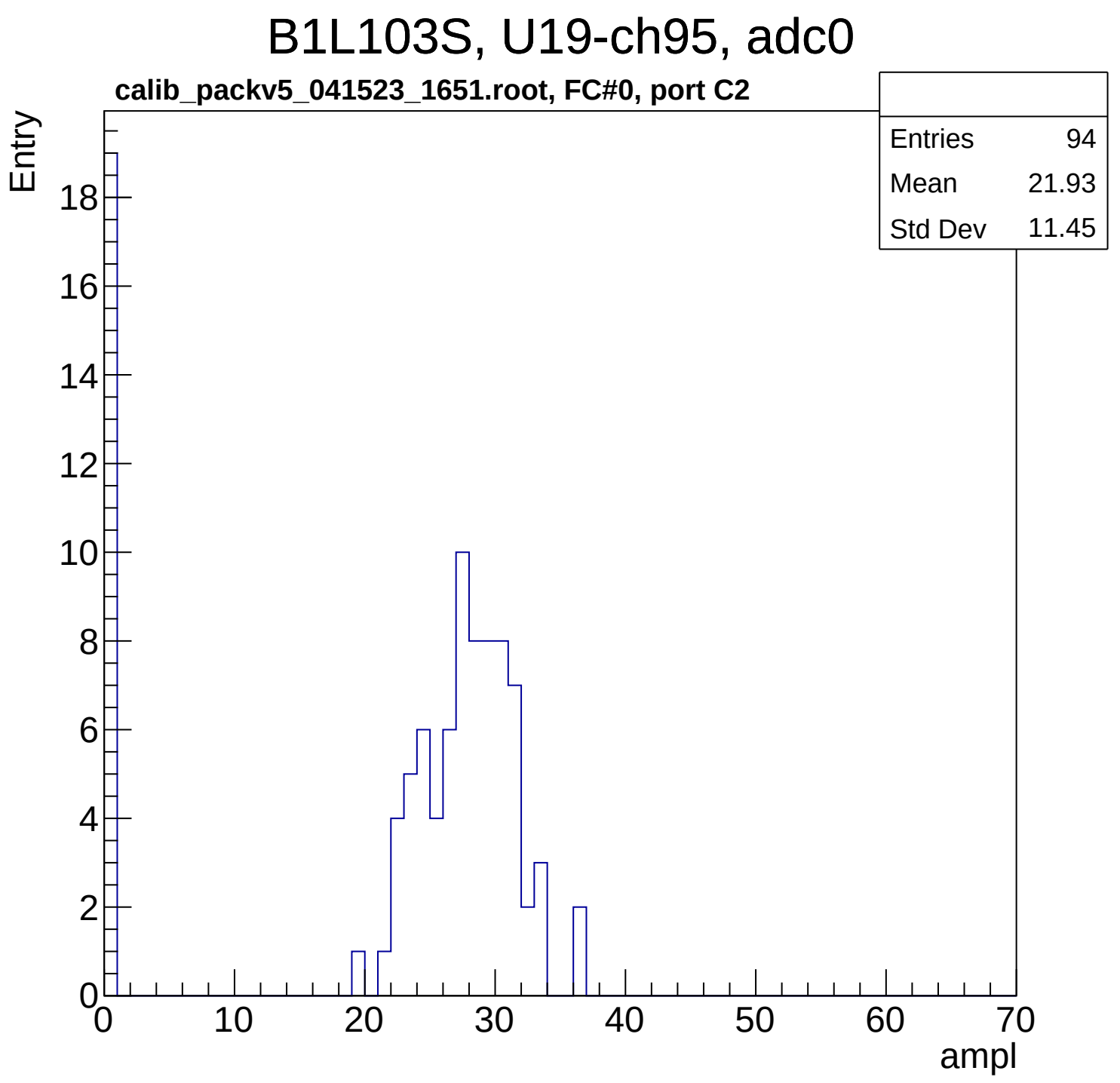

B1L103S, U19-ch94, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 47.5
Std Dev 3.648
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

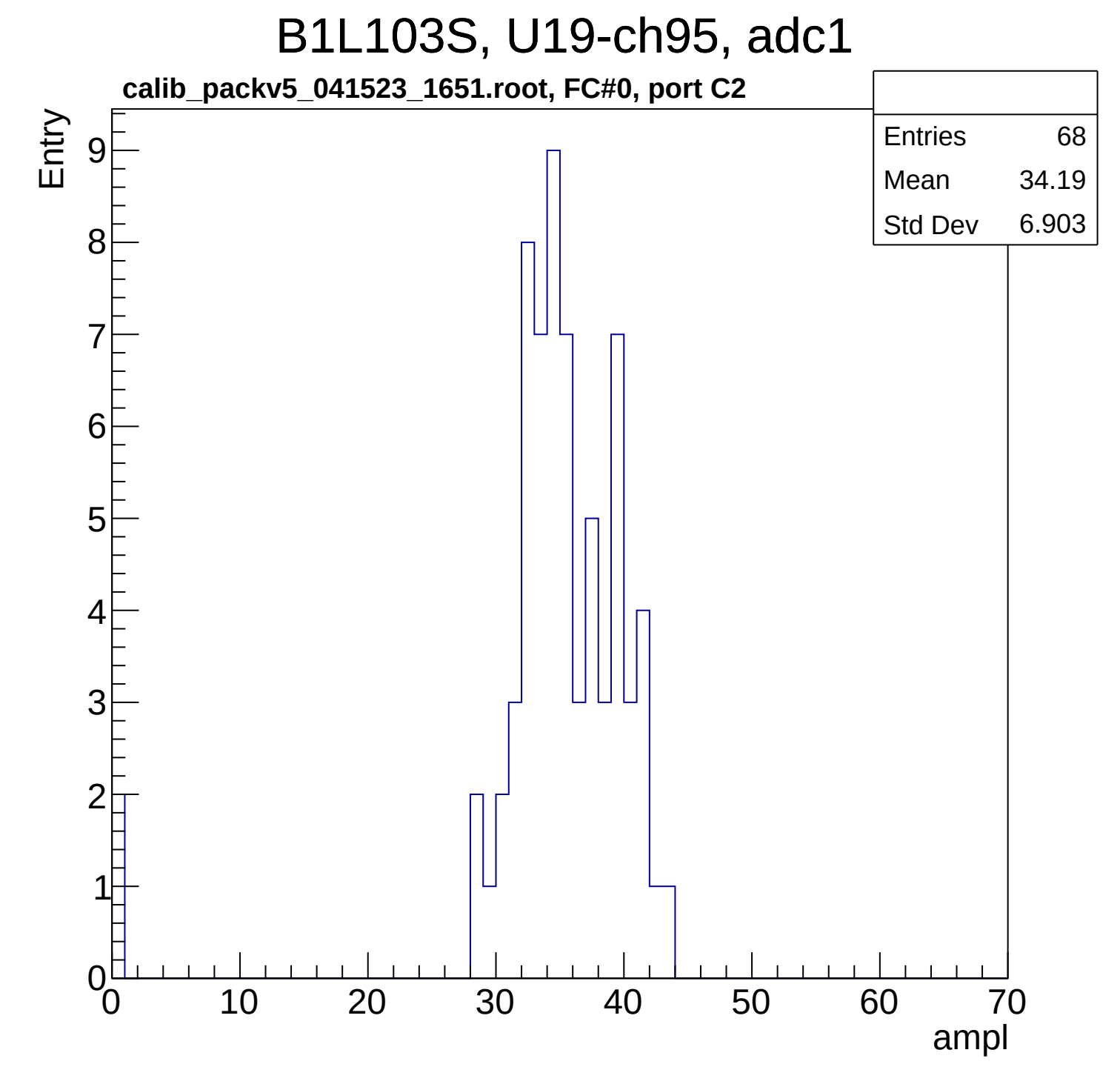

B1L103S, U19-ch94, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 54.59
Std Dev 3.363
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch94, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 57.67
Std Dev 8.768
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch94, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 61.46
Std Dev 1.447
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U19-ch94, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.905
Std Dev 18.2
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch95, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 21.93
Std Dev 11.45
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch95, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 34.19
Std Dev 6.903
Entry
ampl
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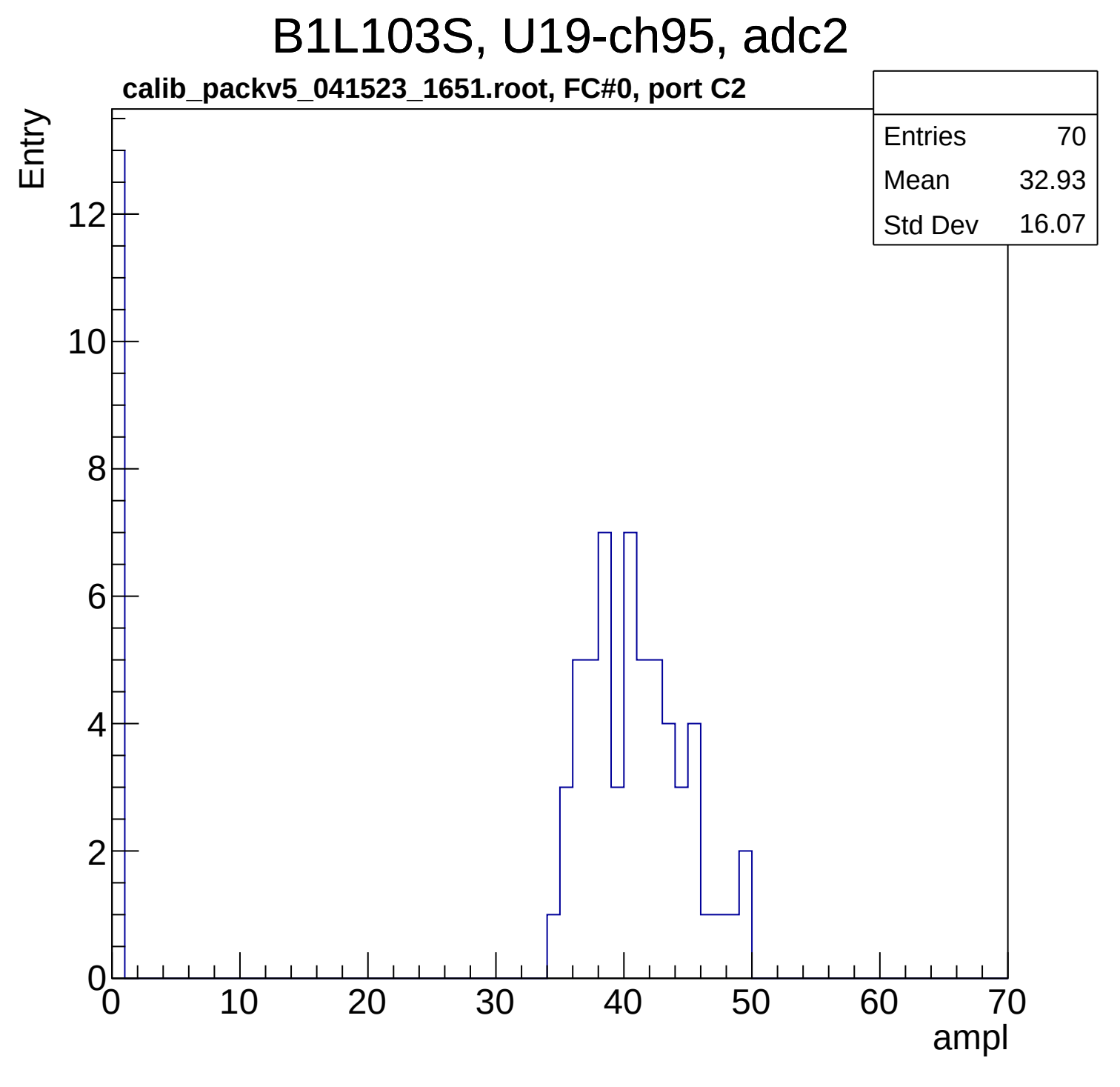
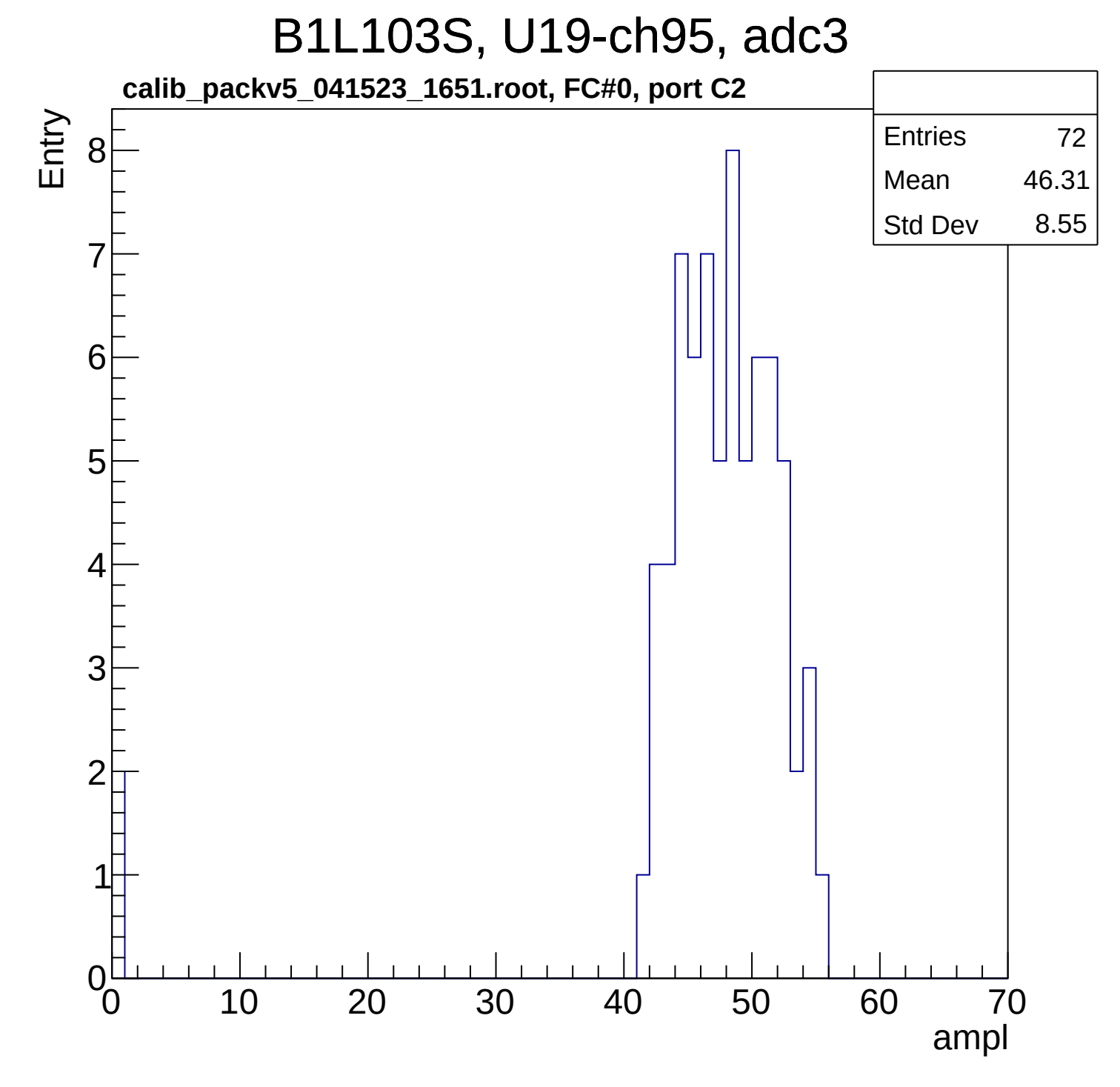
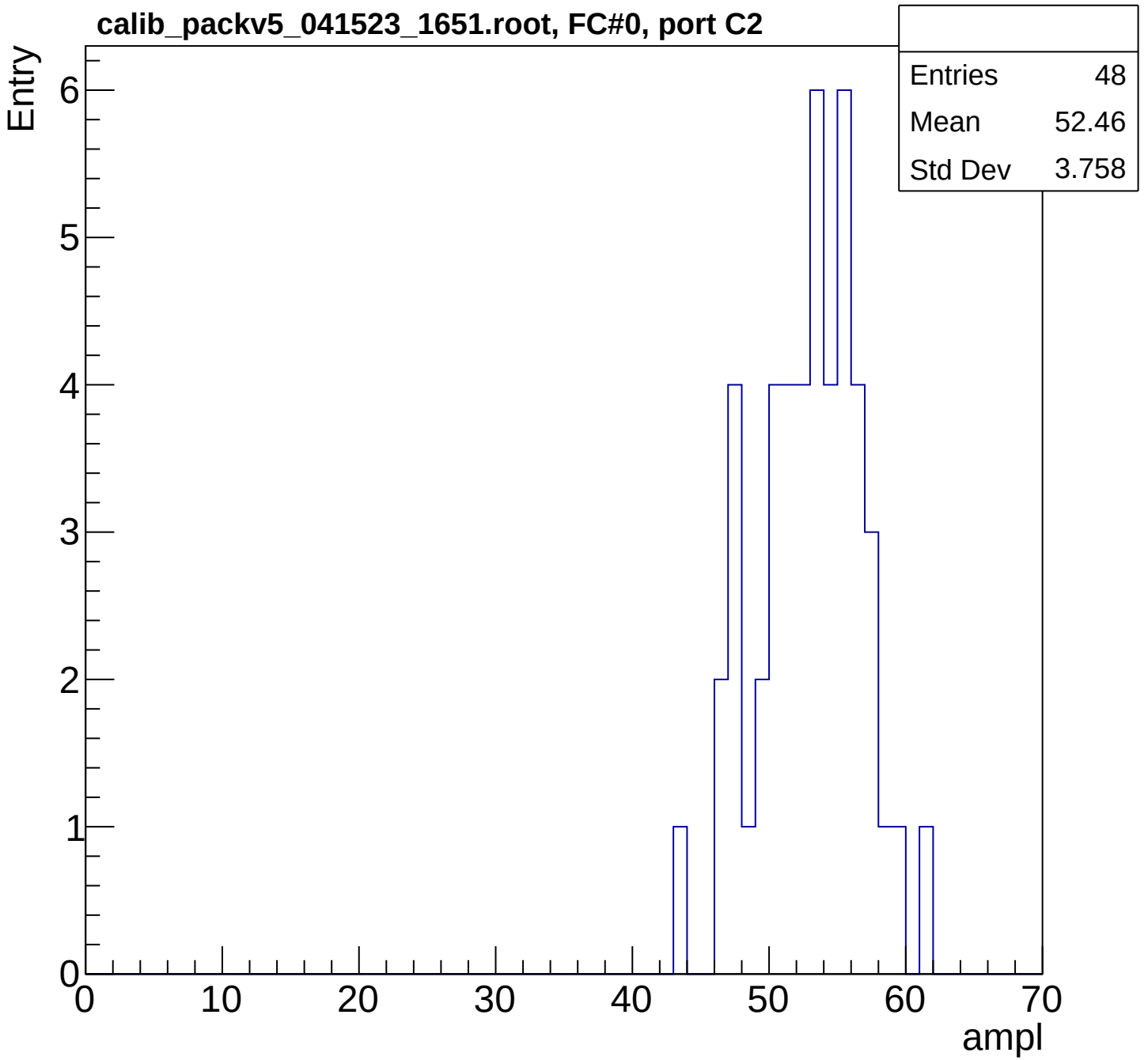
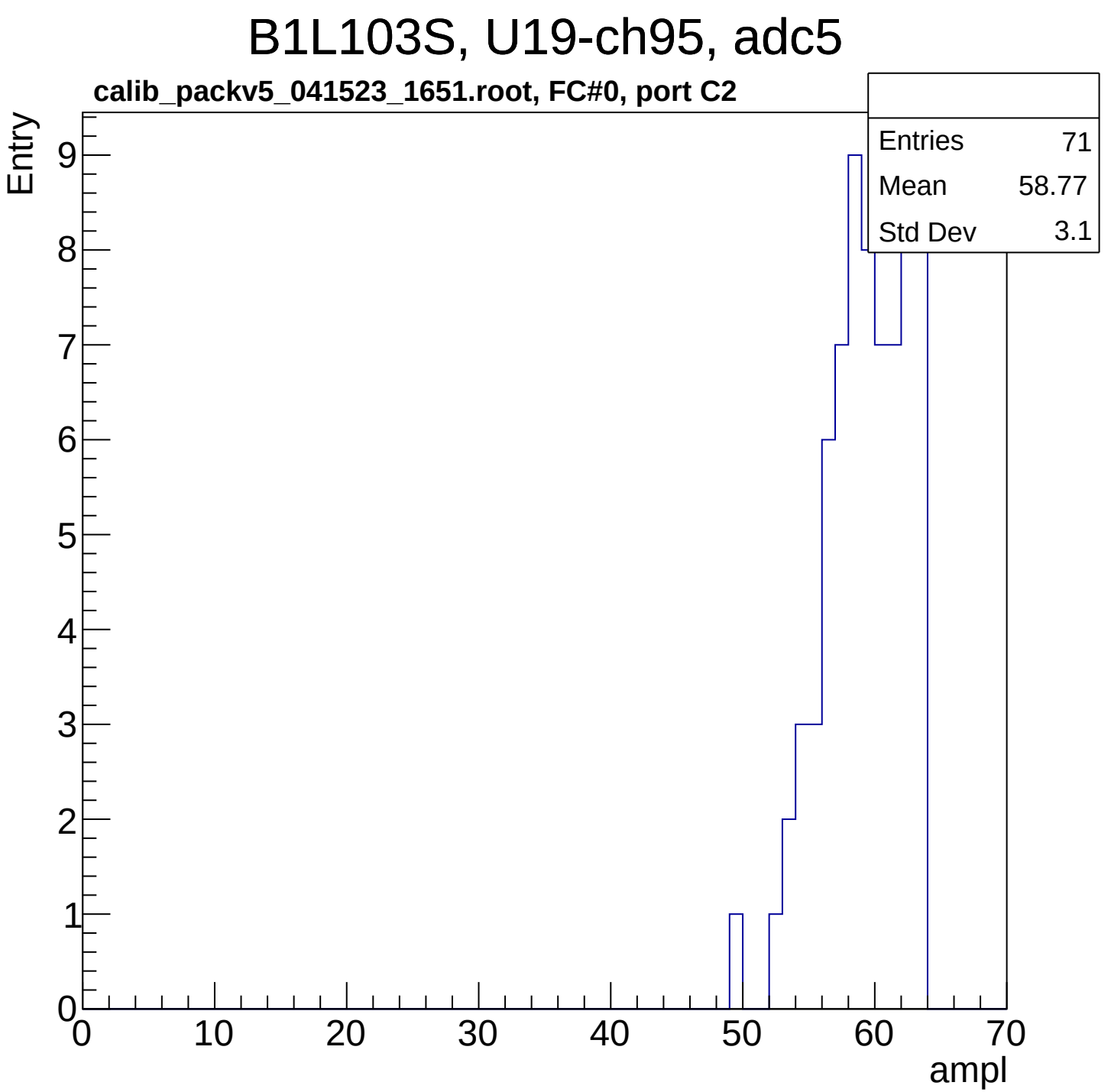
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch95, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 32.93
Std Dev 16.07
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch95, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 46.31
Std Dev 8.55
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch95, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 52.46
Std Dev 3.758
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U19-ch95, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 58.77
Std Dev 3.1
Entry
ampl
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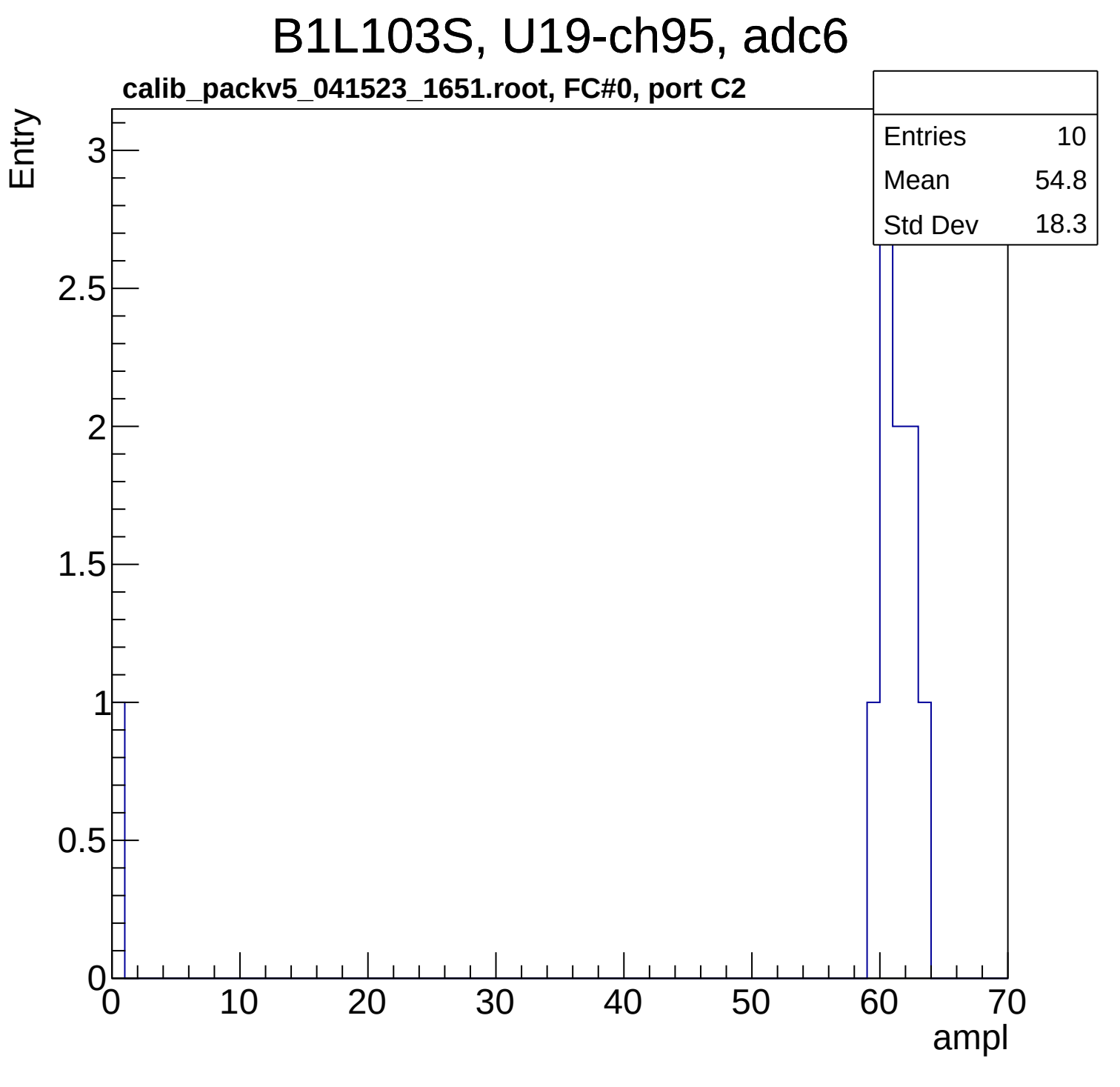
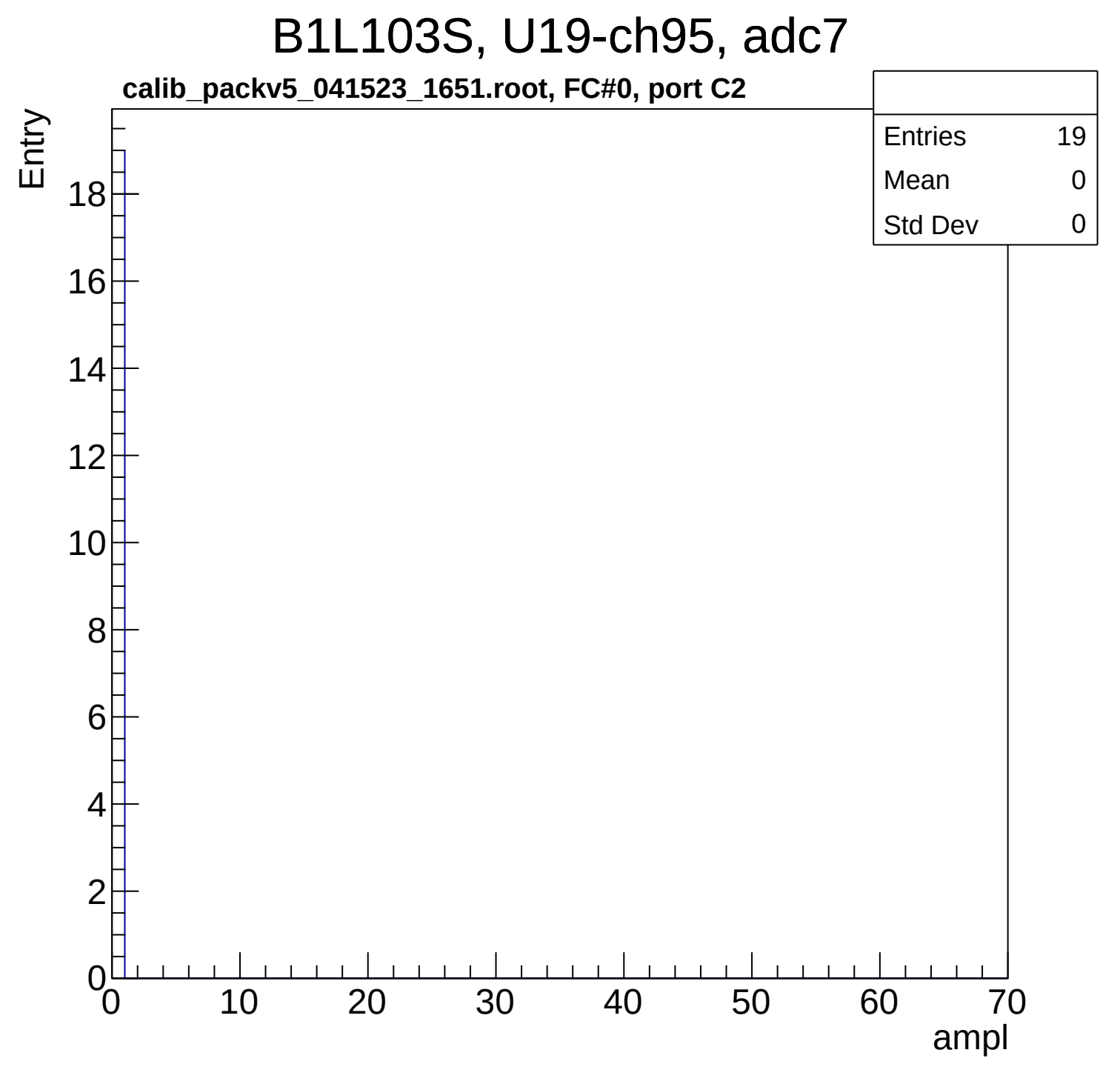
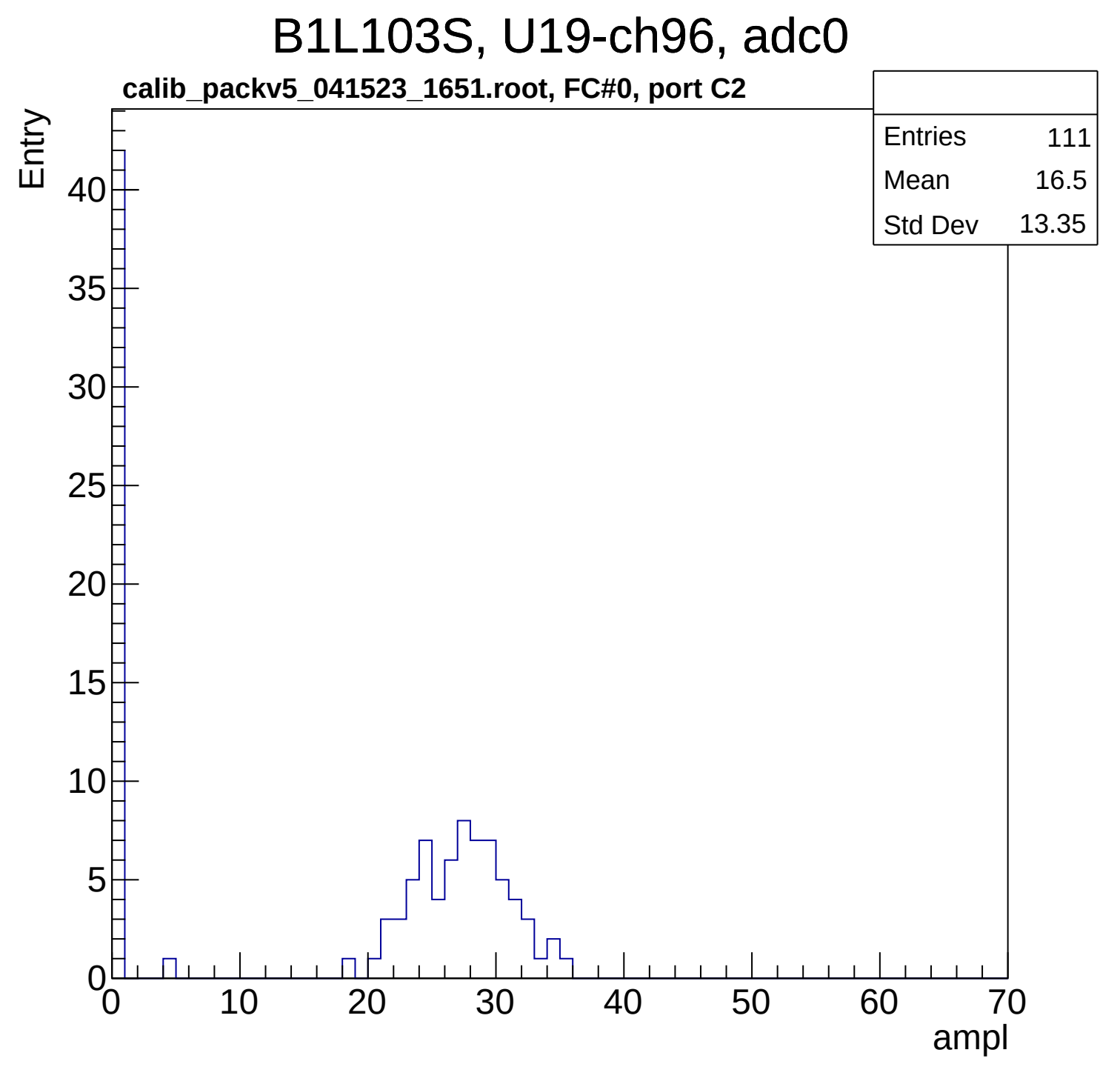
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch95, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 54.8
Std Dev 18.3
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U19-ch95, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch96, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 111
Mean 16.5
Std Dev 13.35
Entry
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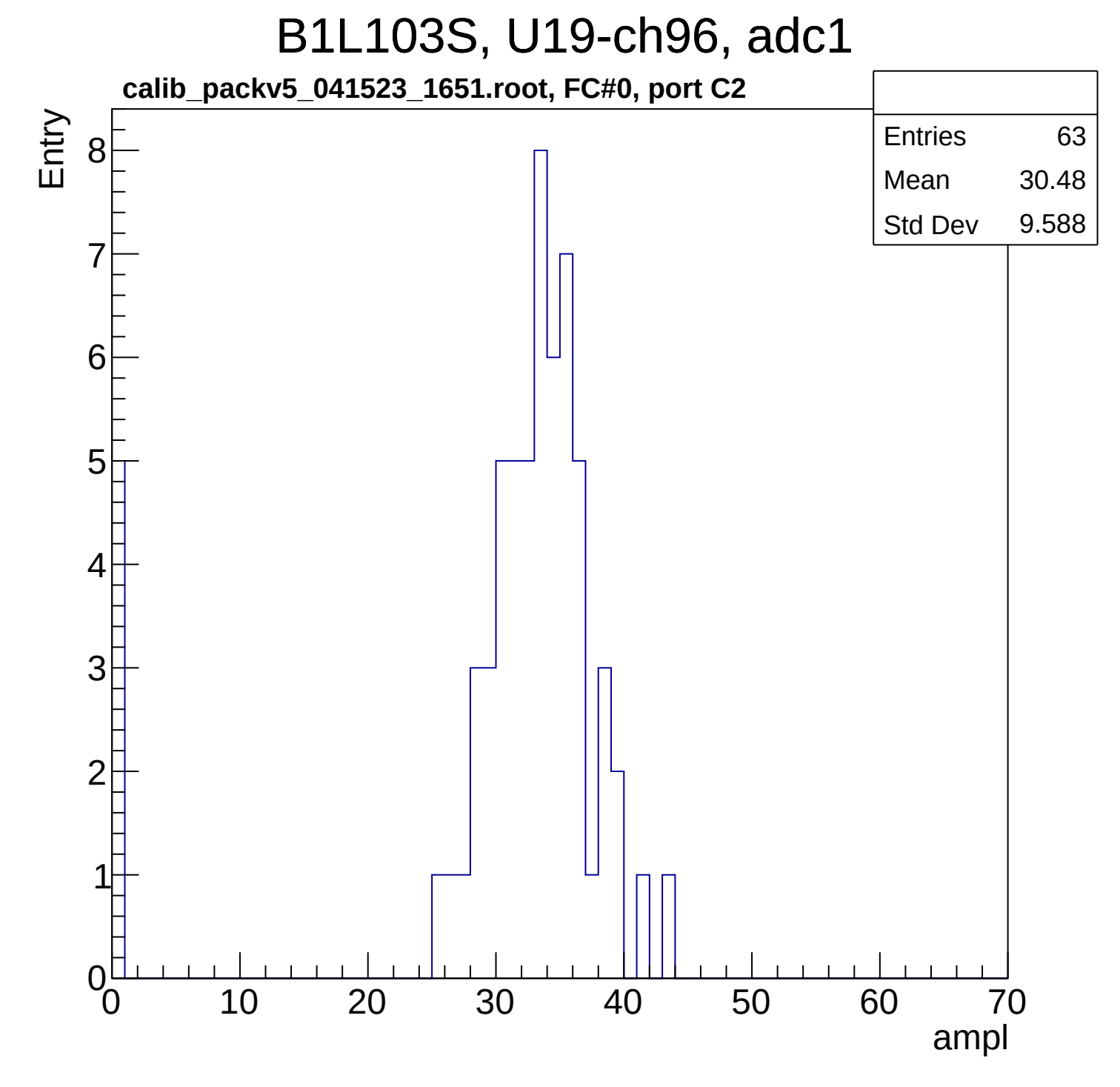
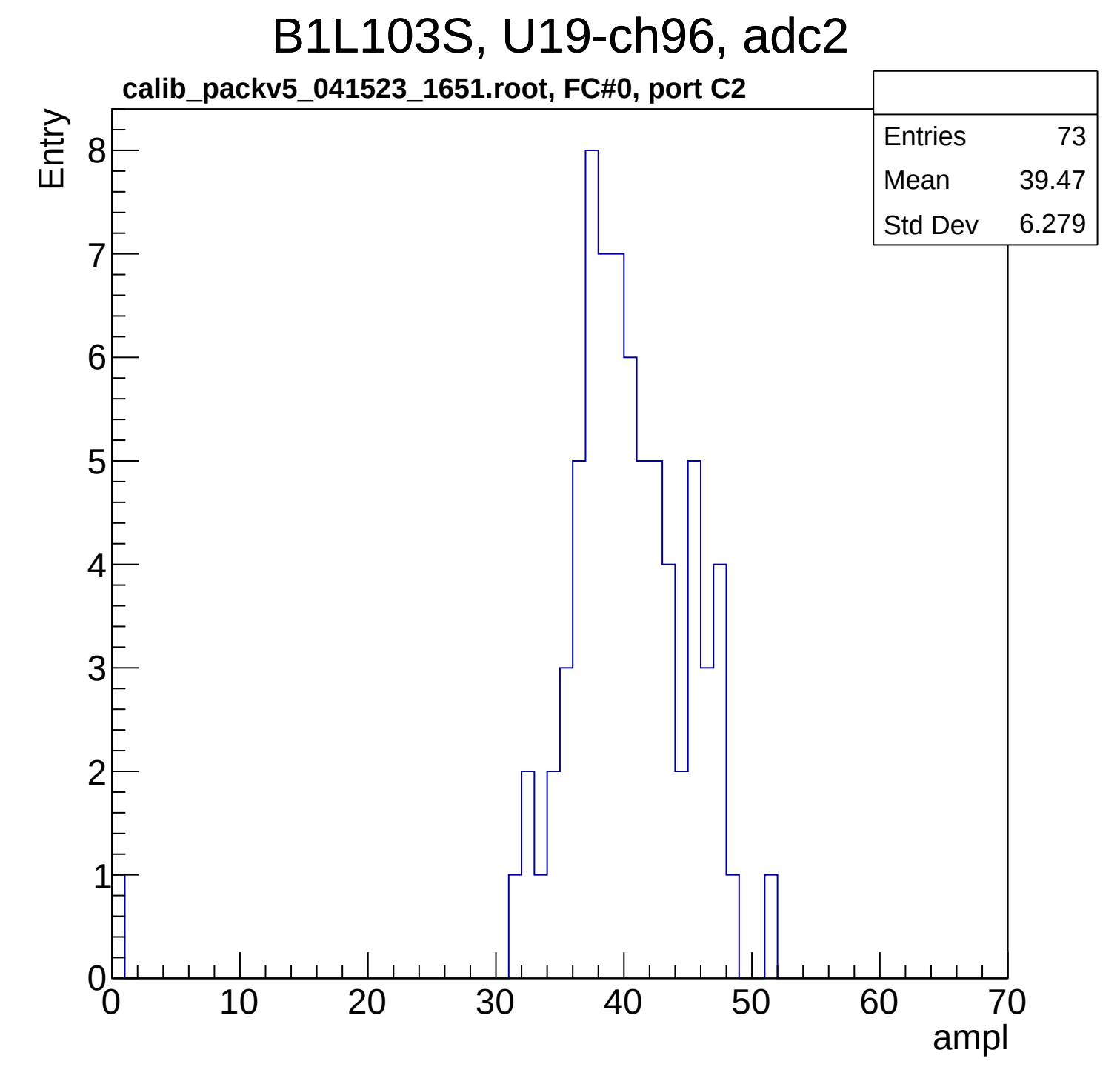
5
10
15
20
25
30
35
40
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch96, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 30.48
Std Dev 9.588
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch96, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 39.47
Std Dev 6.279
Entry
ampl
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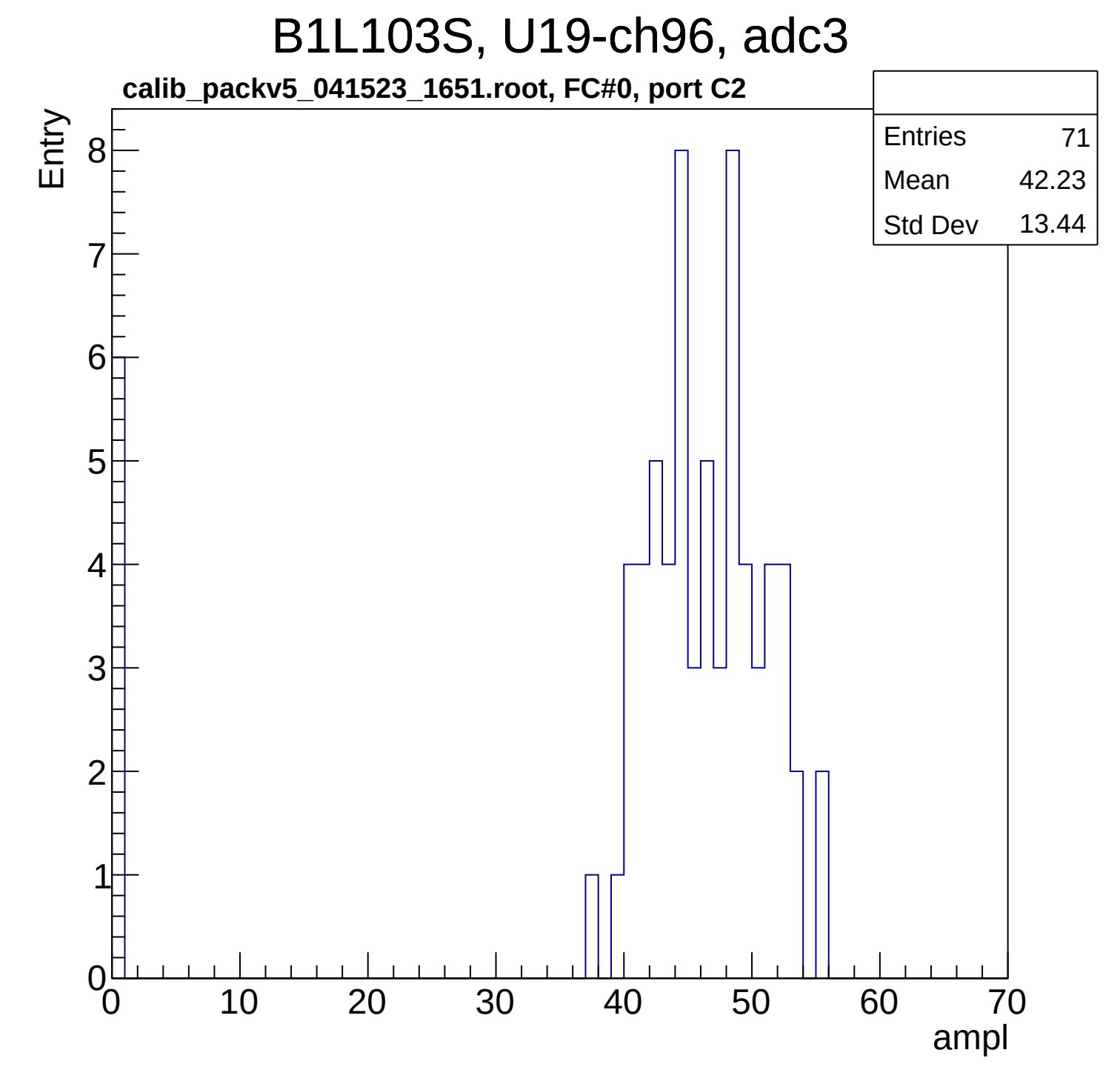
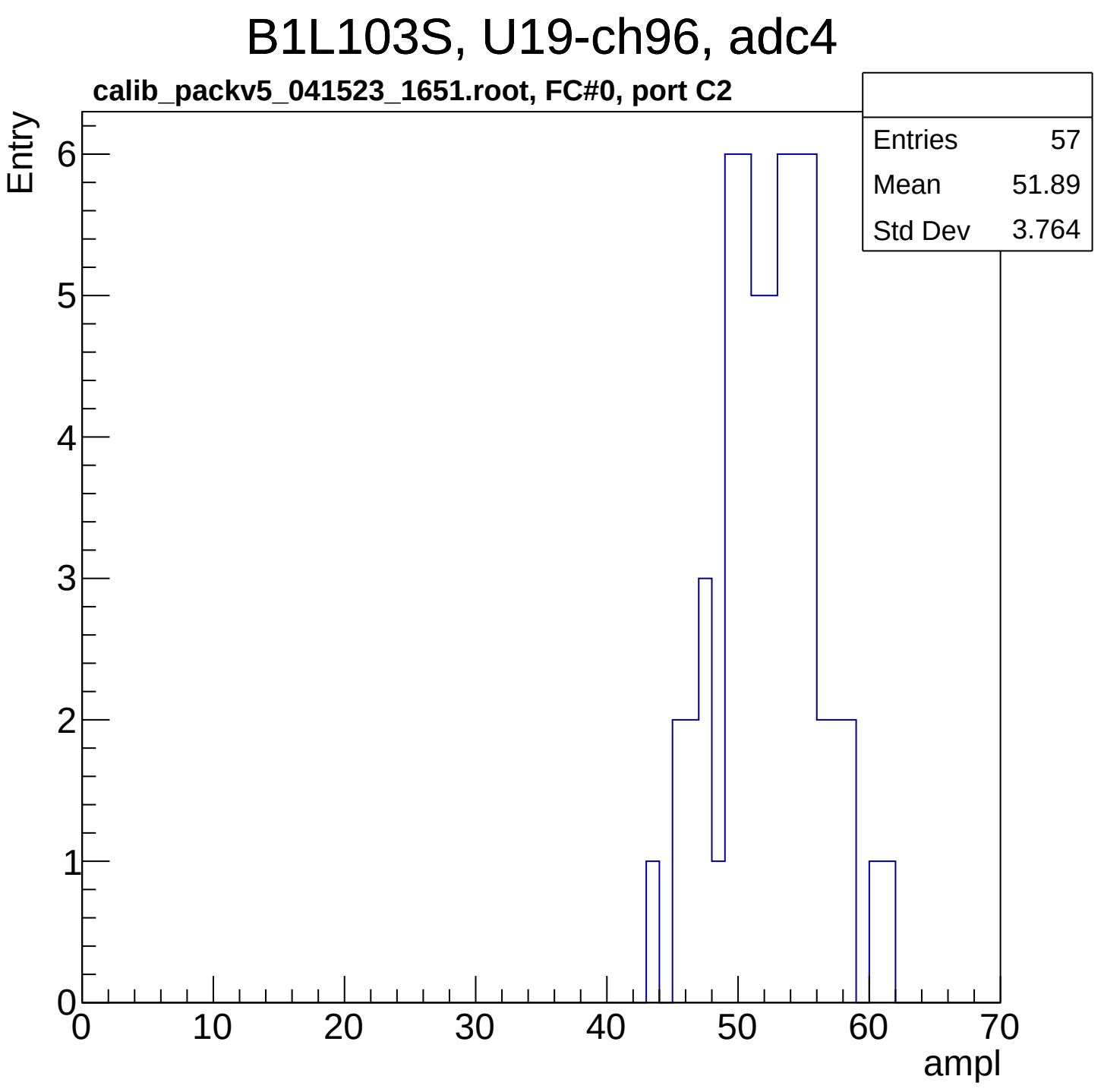
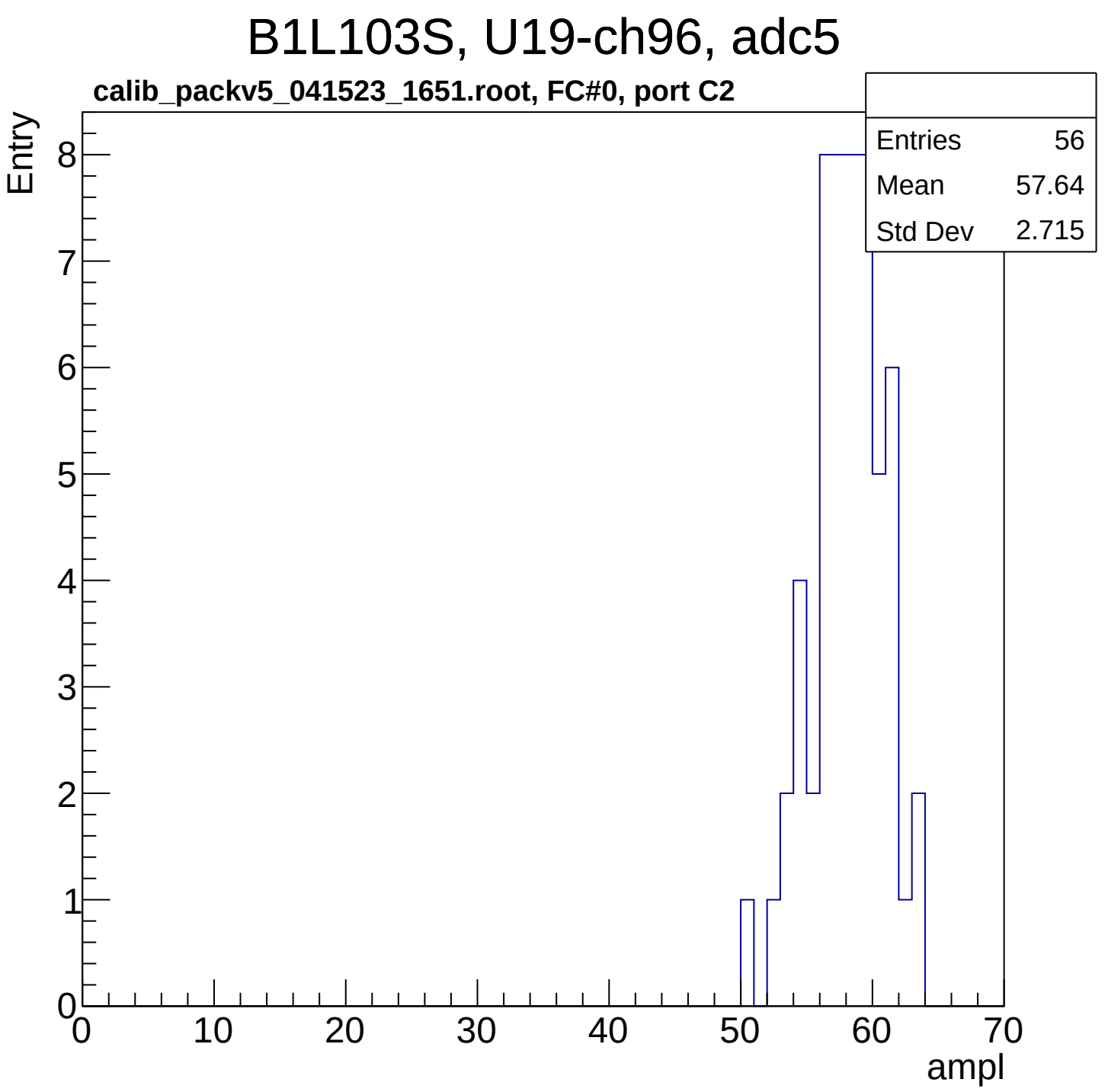
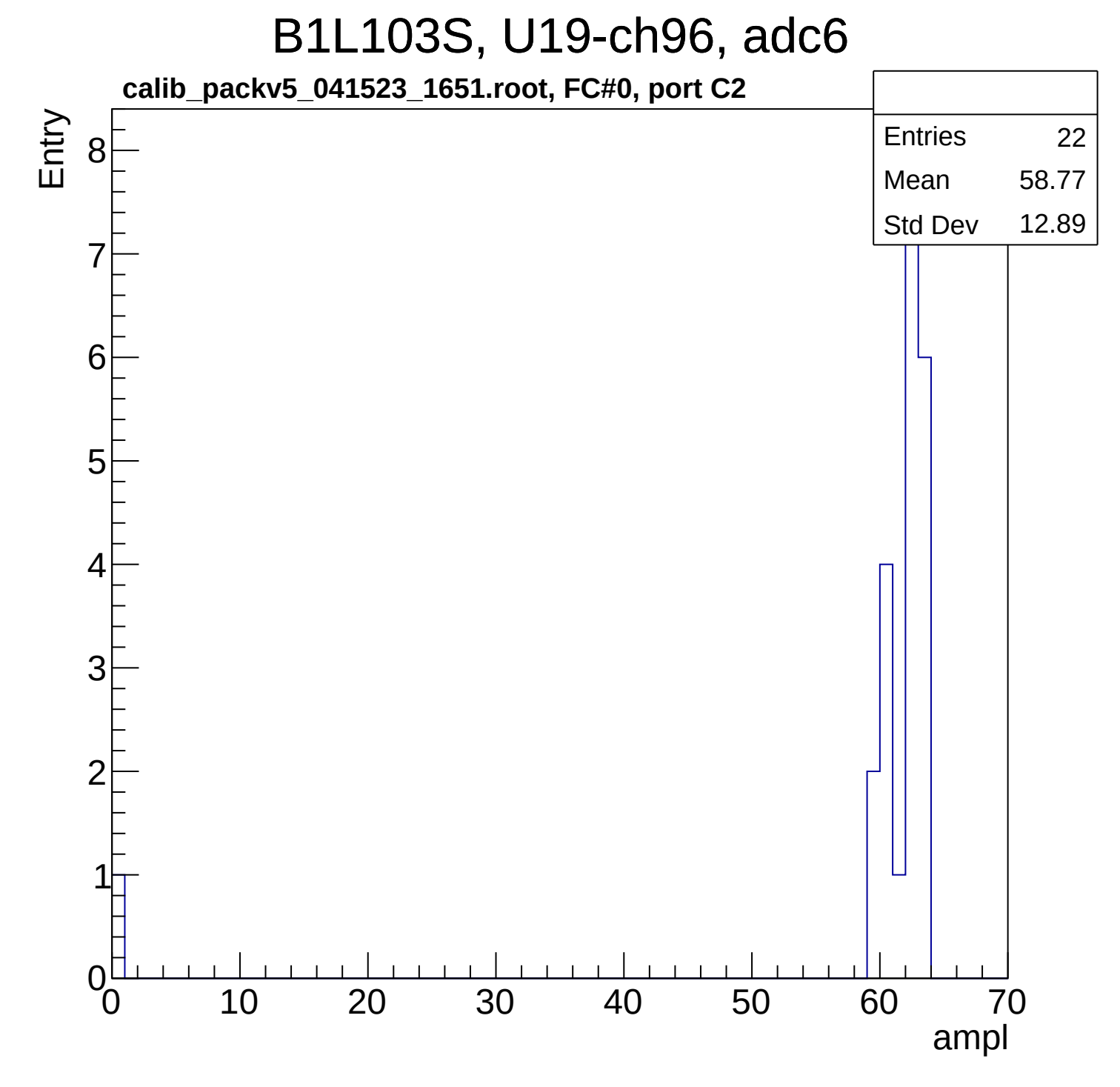
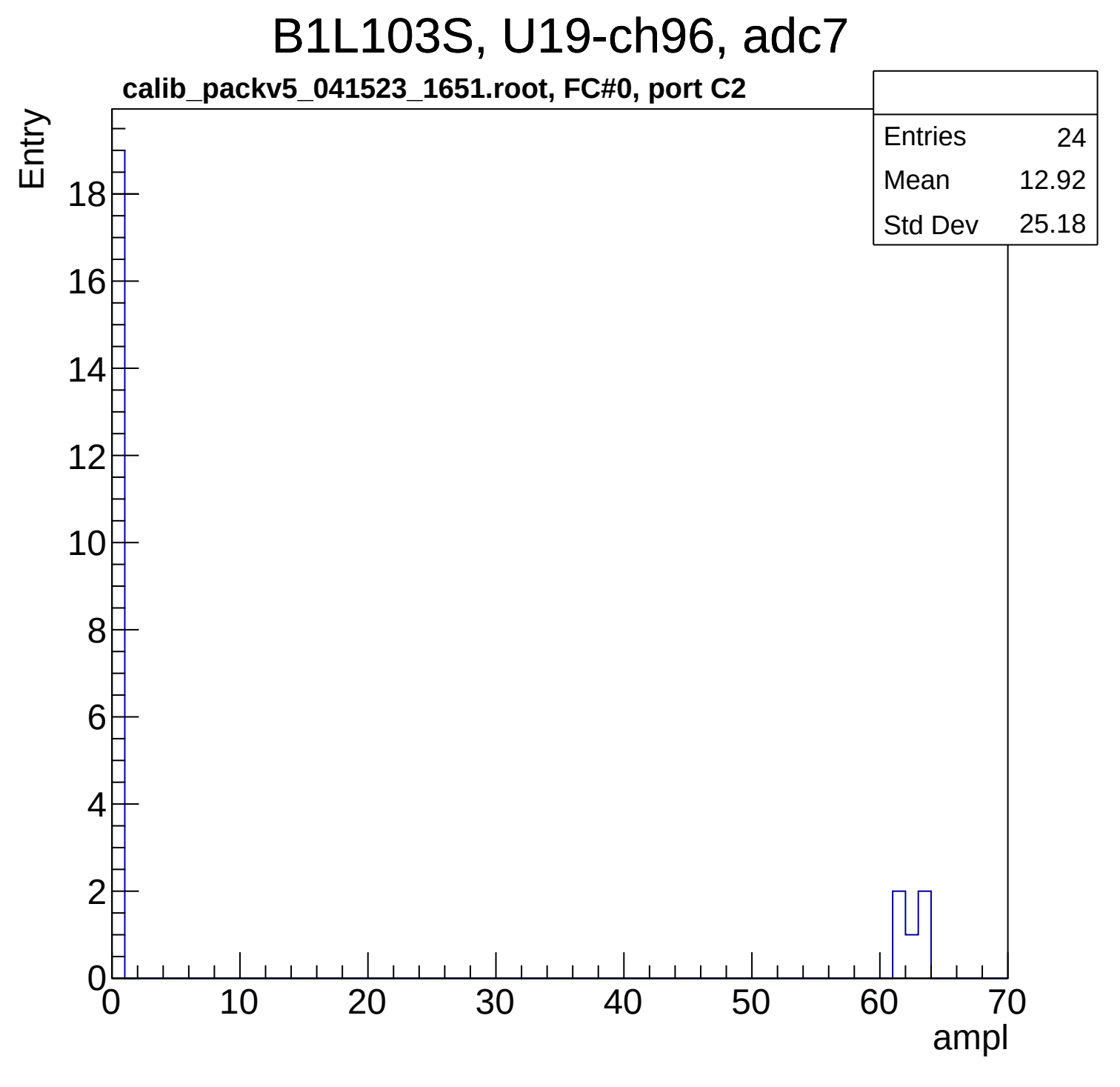
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch96, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 42.23
Std Dev 13.44
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch96, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 51.89
Std Dev 3.764
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U19-ch96, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 57.64
Std Dev 2.715
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch96, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 58.77
Std Dev 12.89
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch96, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 12.92
Std Dev 25.18
Entry
0
2
4
6
8
10
12
14
16
18
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10
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30
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50
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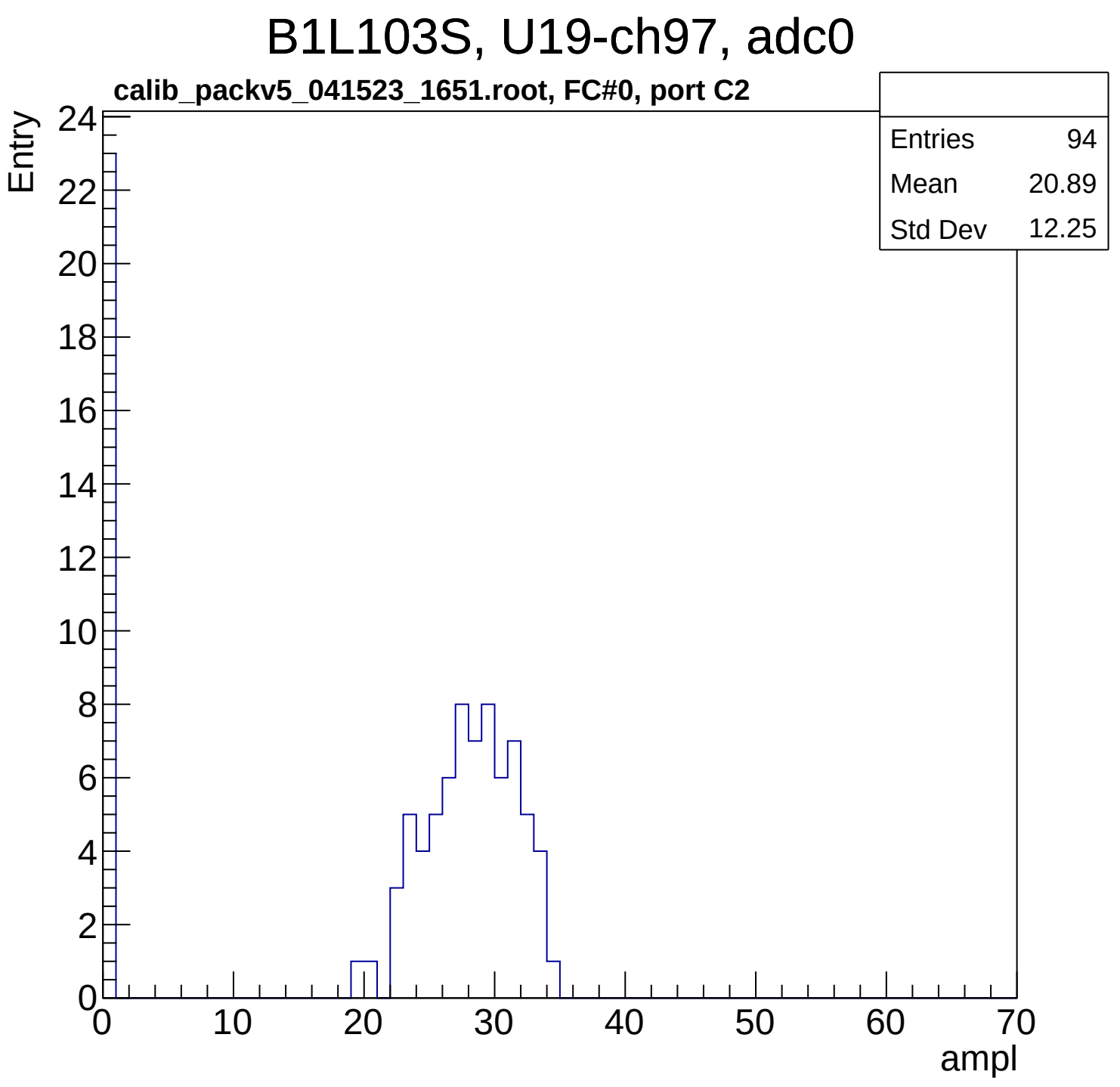
70
ampl


B1L103S, U19-ch97, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 20.89
Std Dev 12.25
Entry
ampl
0
2
4
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10
12
14
16
18
20
22
24
0
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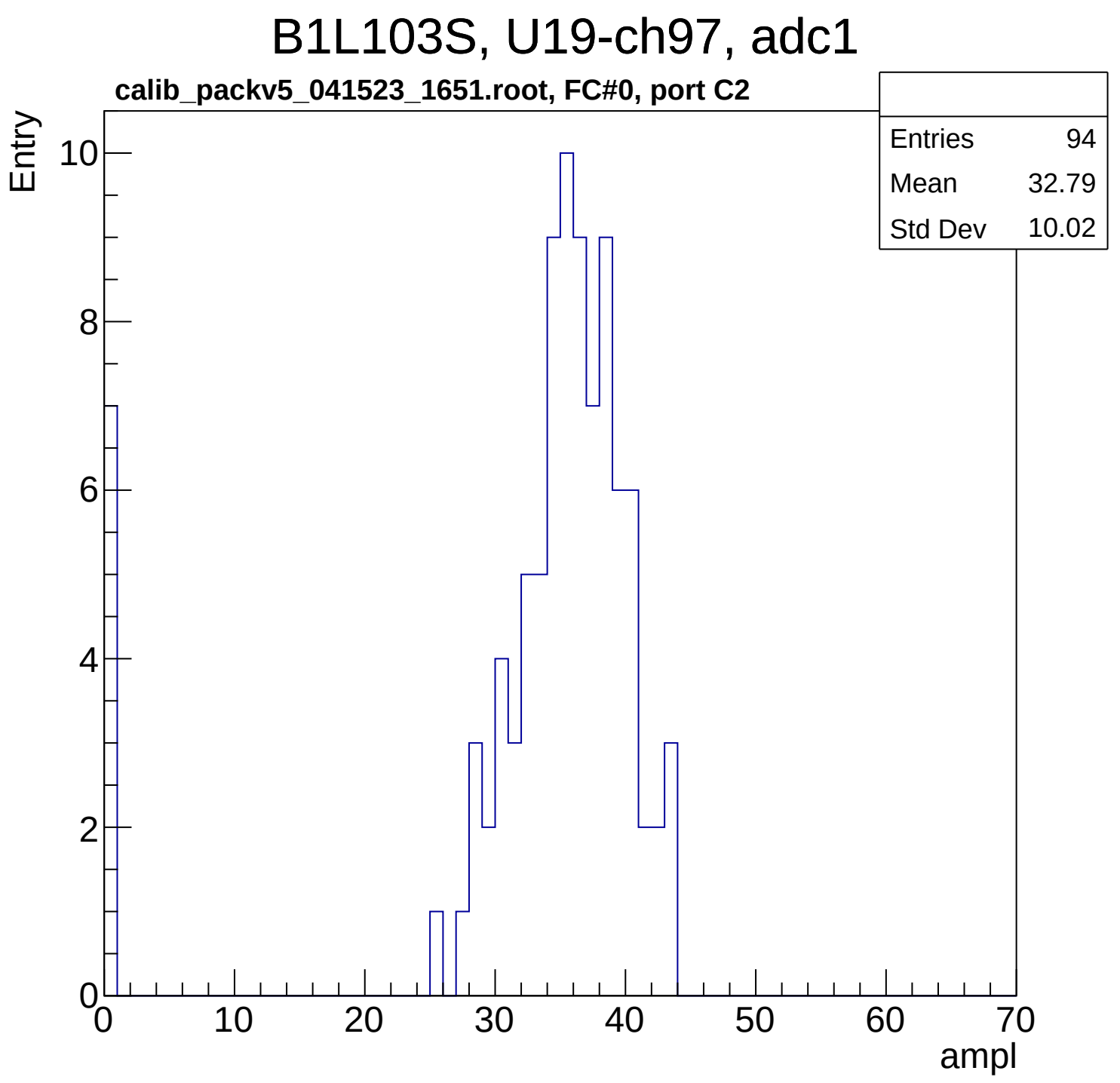
B1L103S, U19-ch97, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 32.79
Std Dev 10.02
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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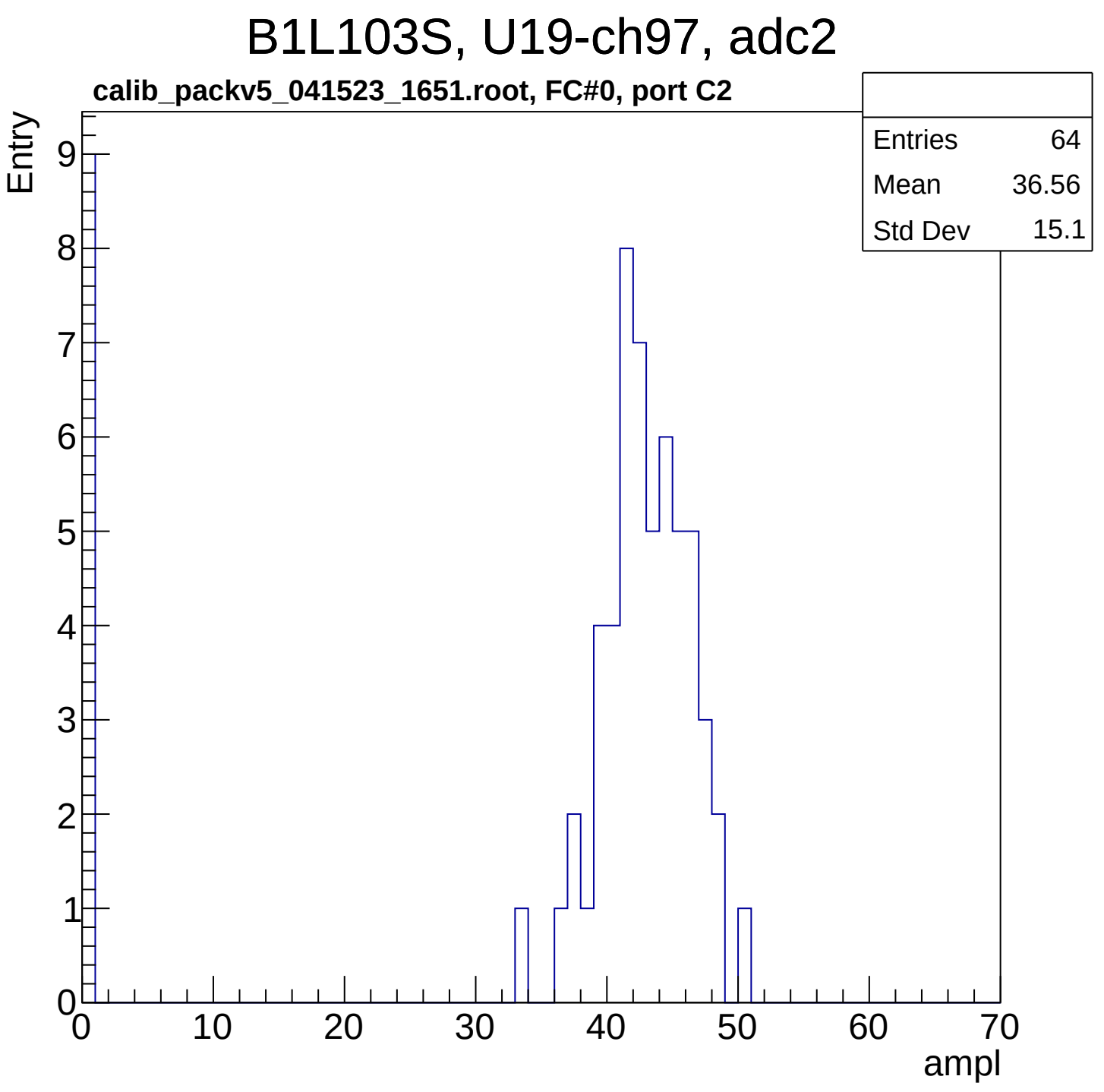
B1L103S, U19-ch97, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 36.56
Std Dev 15.1
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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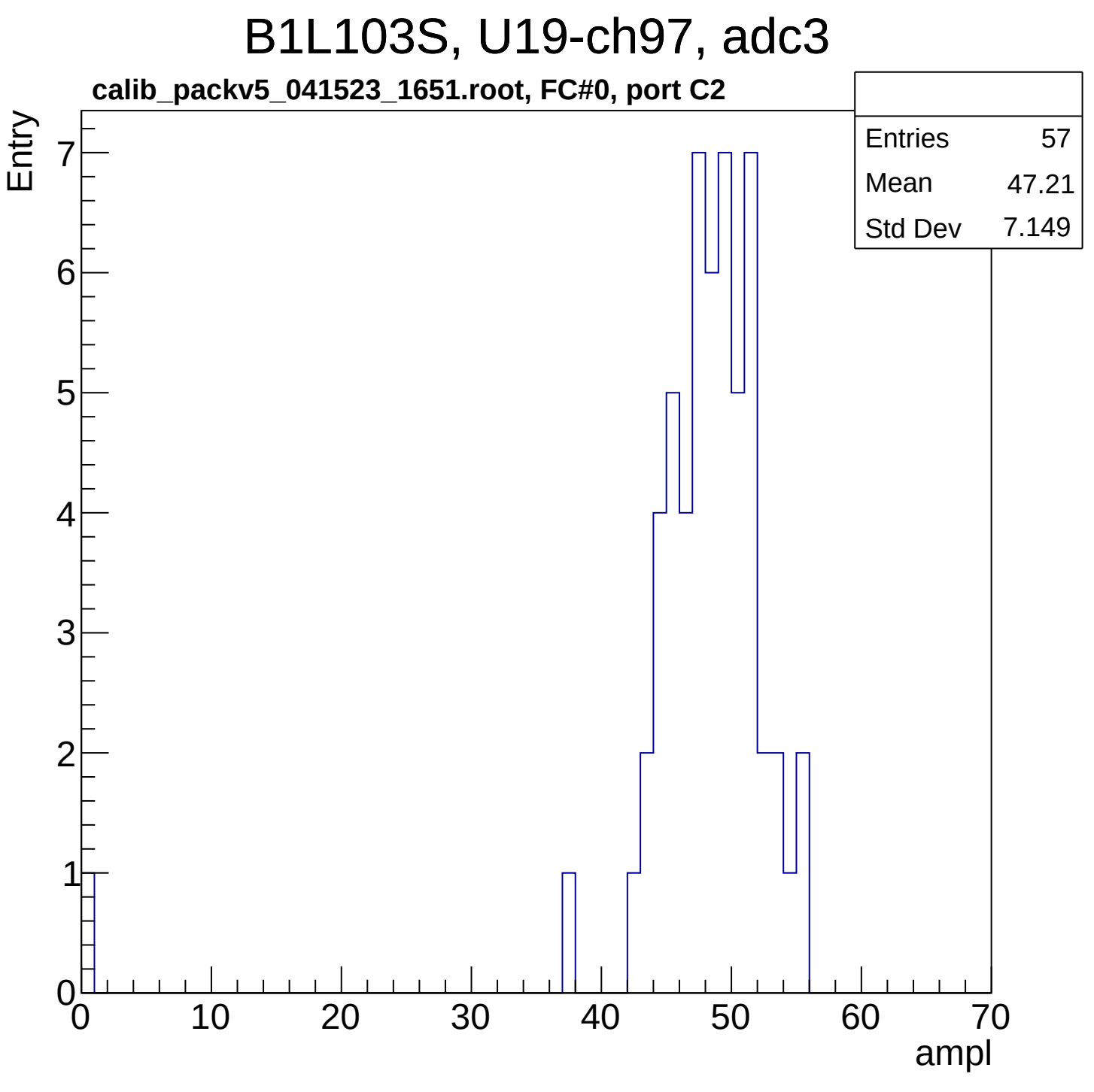
B1L103S, U19-ch97, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 47.21
Std Dev 7.149
Entry
ampl
0
1
2
3
4
5
6
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0
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60
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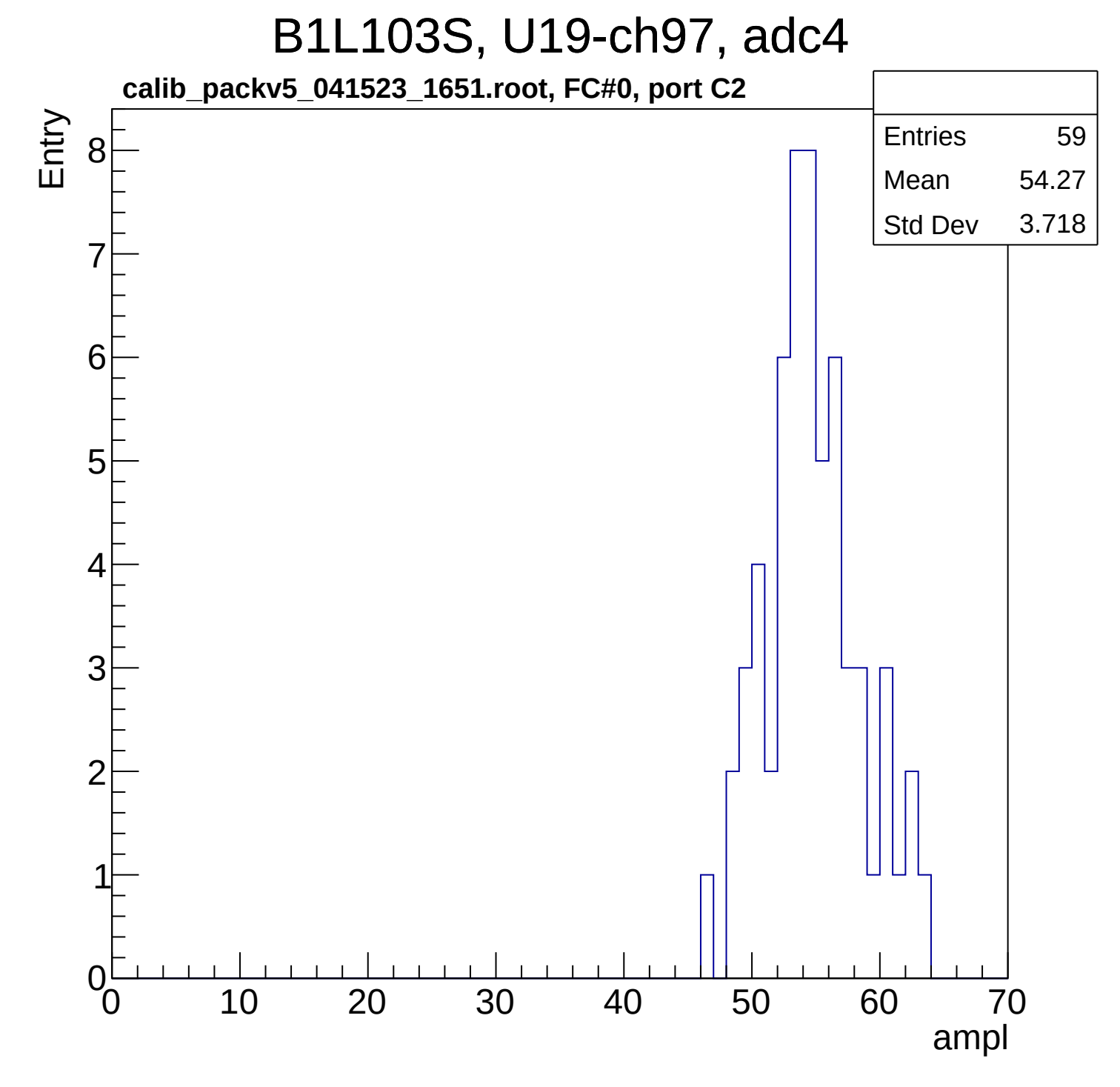
B1L103S, U19-ch97, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 54.27
Std Dev 3.718
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
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40
50
60
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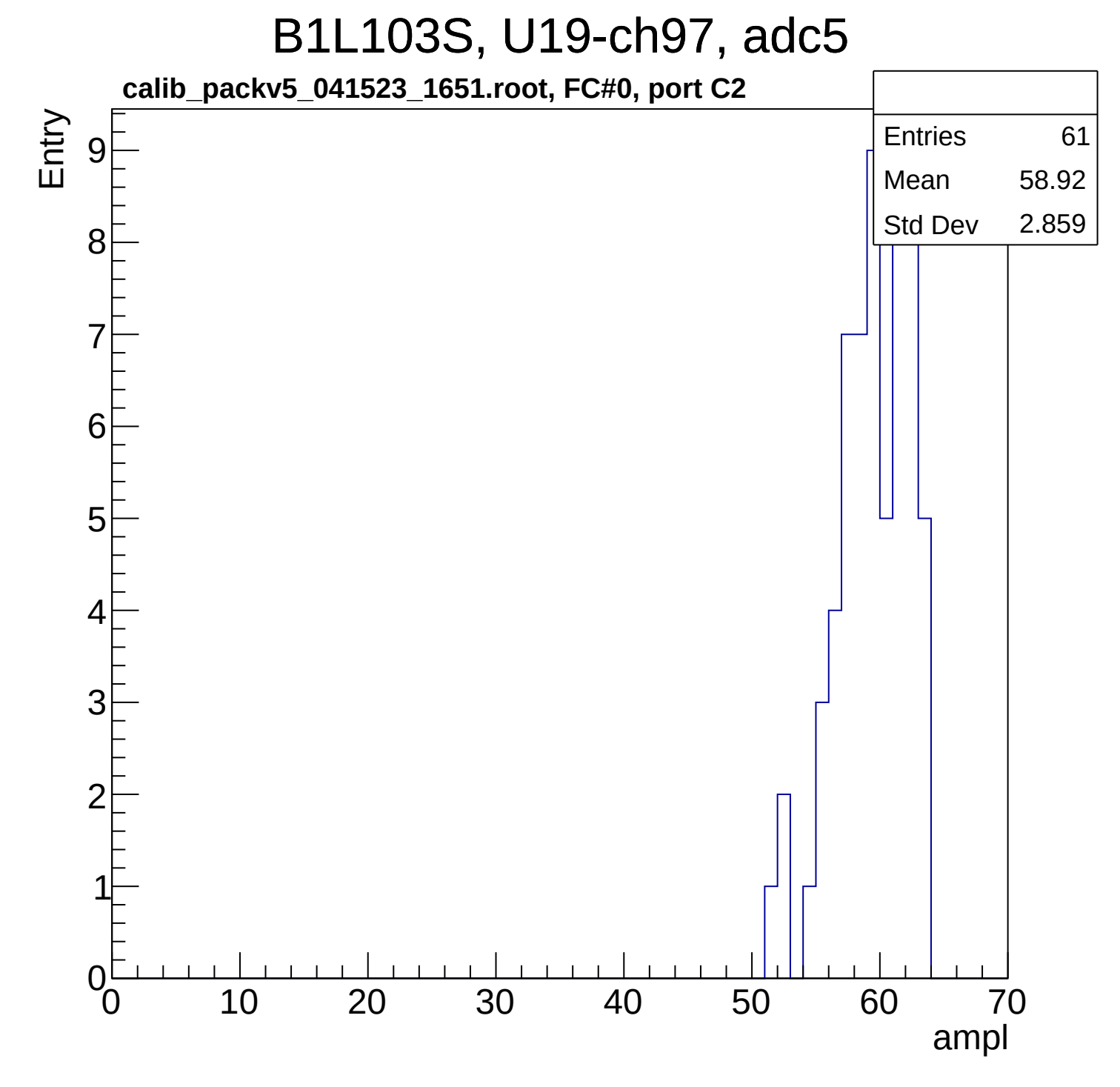
B1L103S, U19-ch97, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 58.92
Std Dev 2.859
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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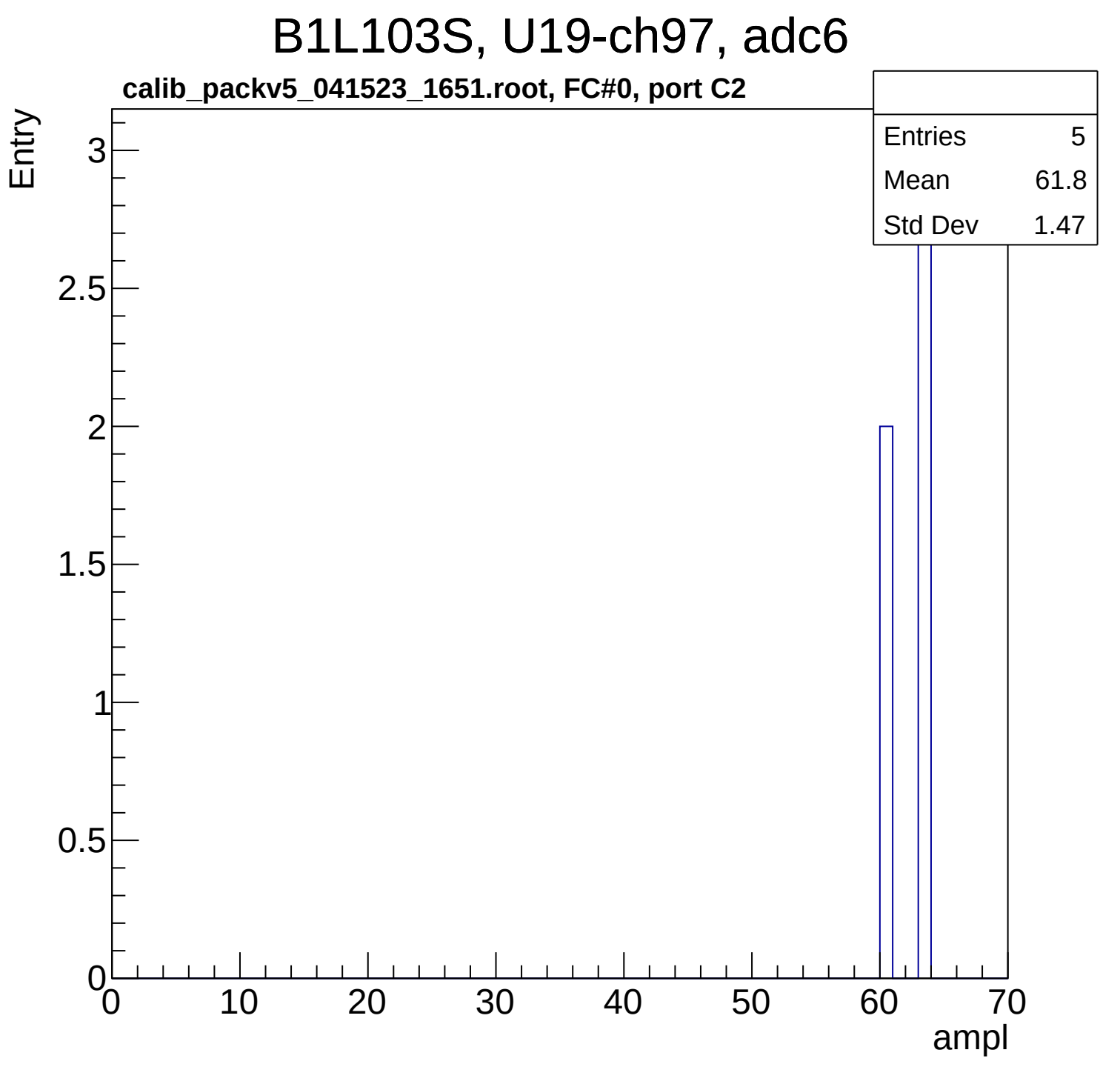
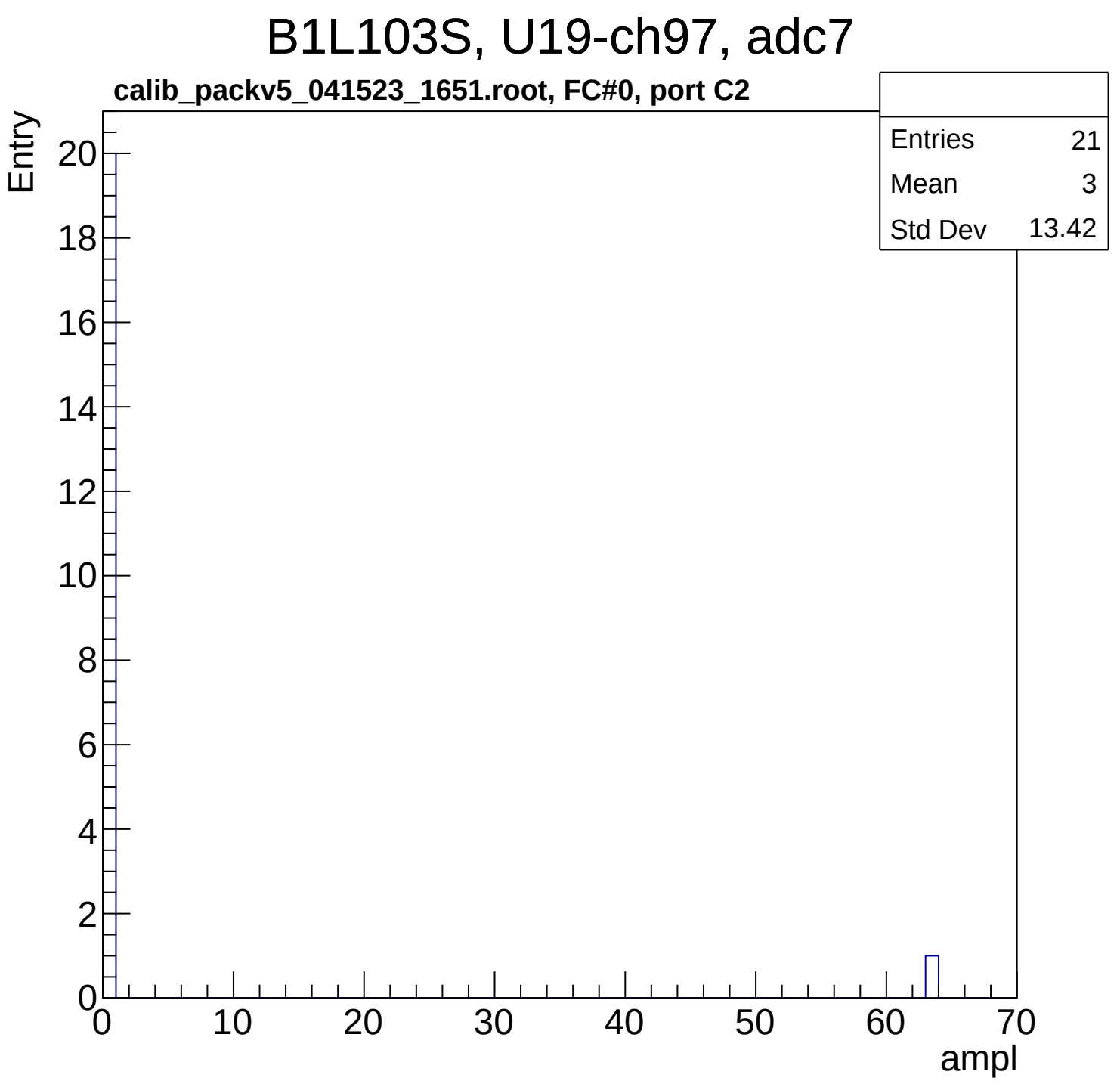
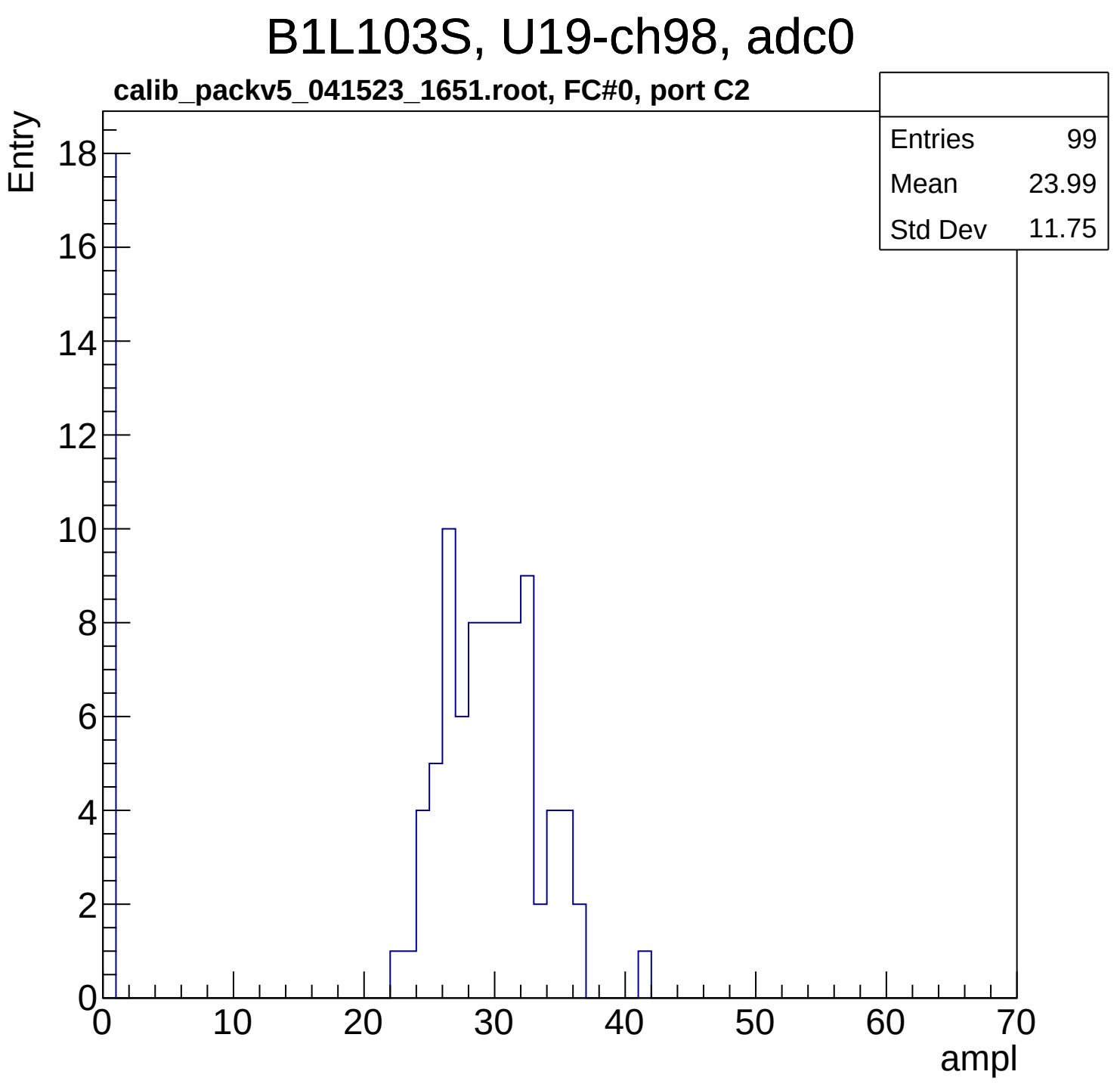
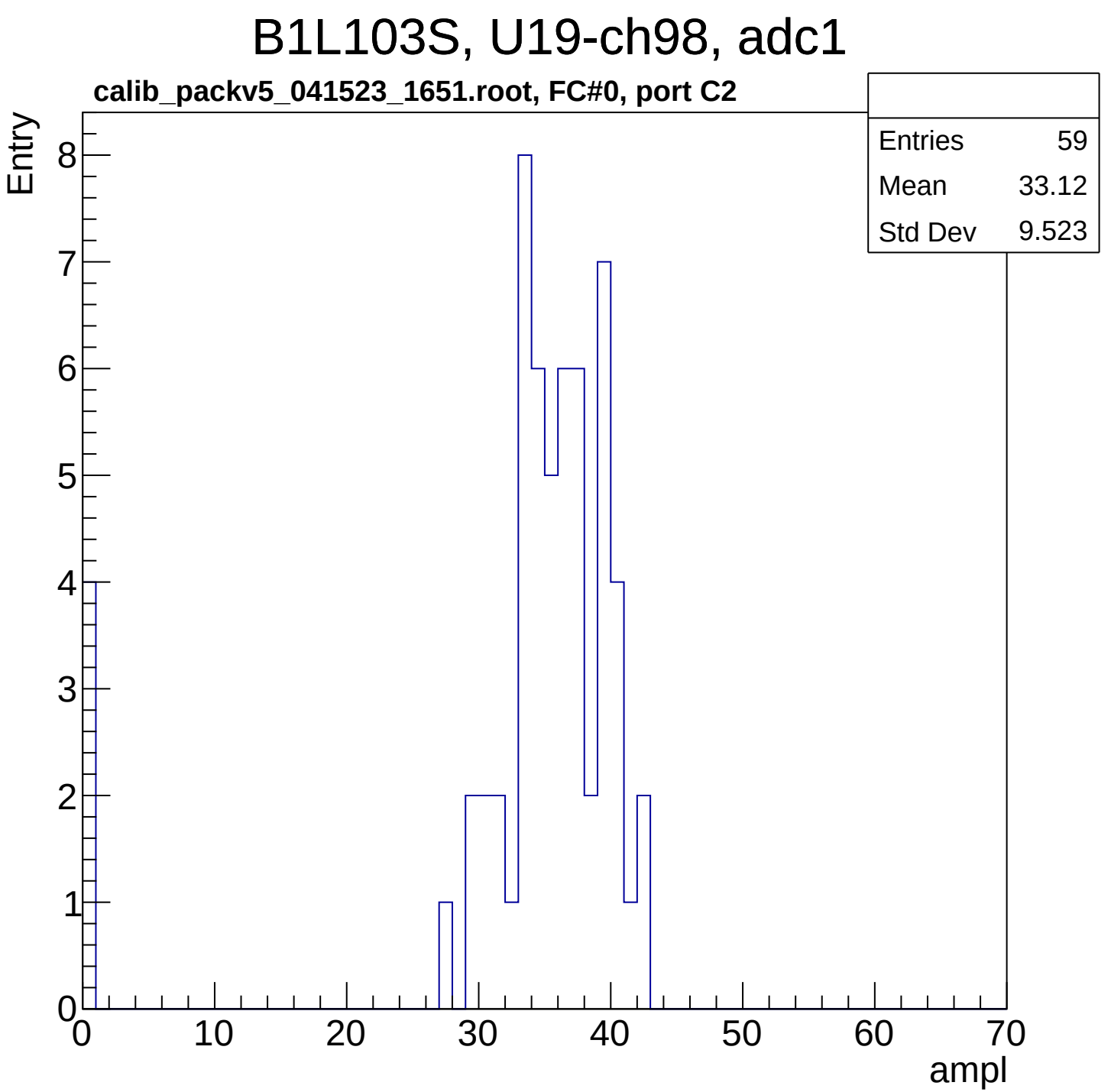
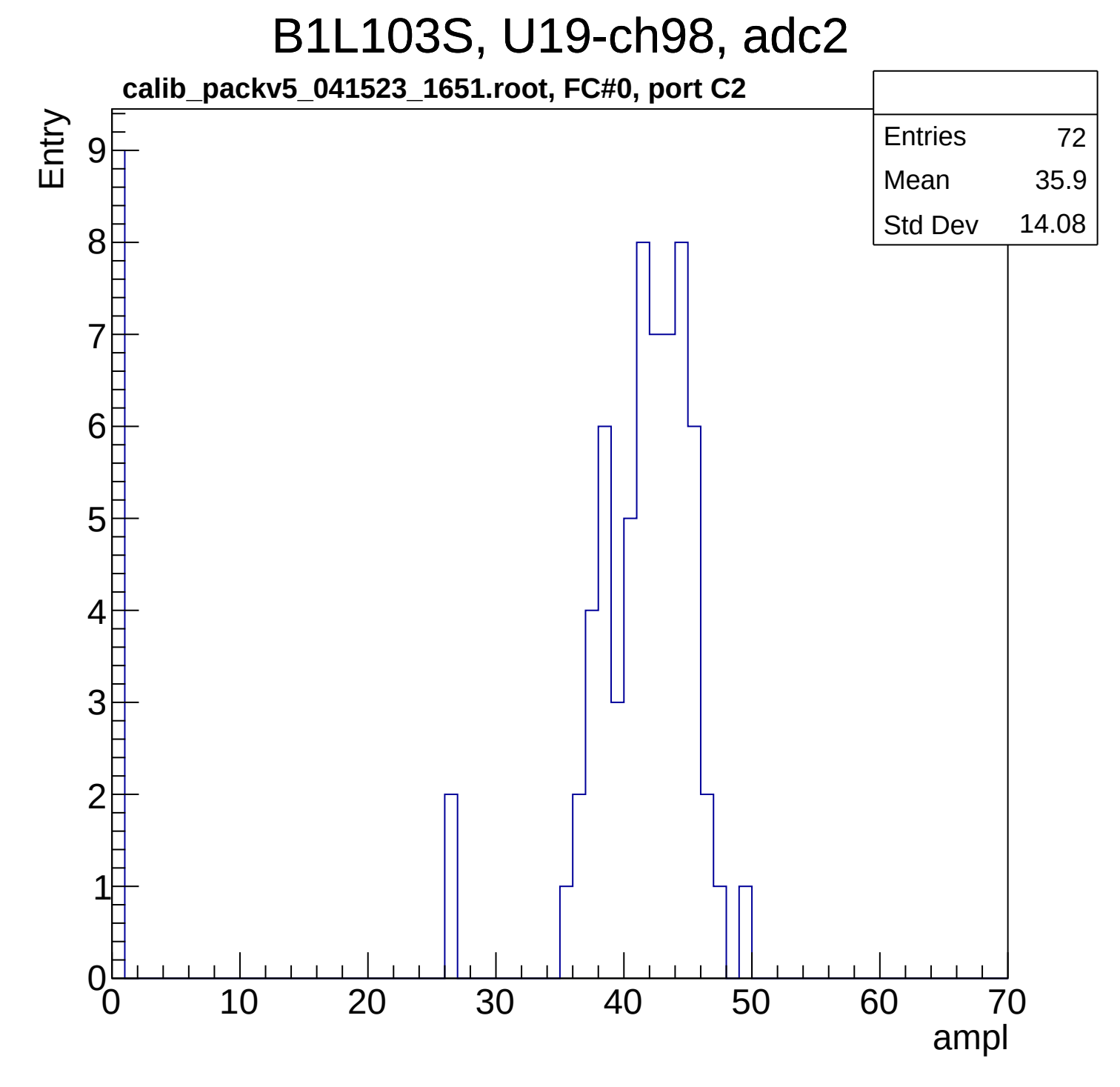
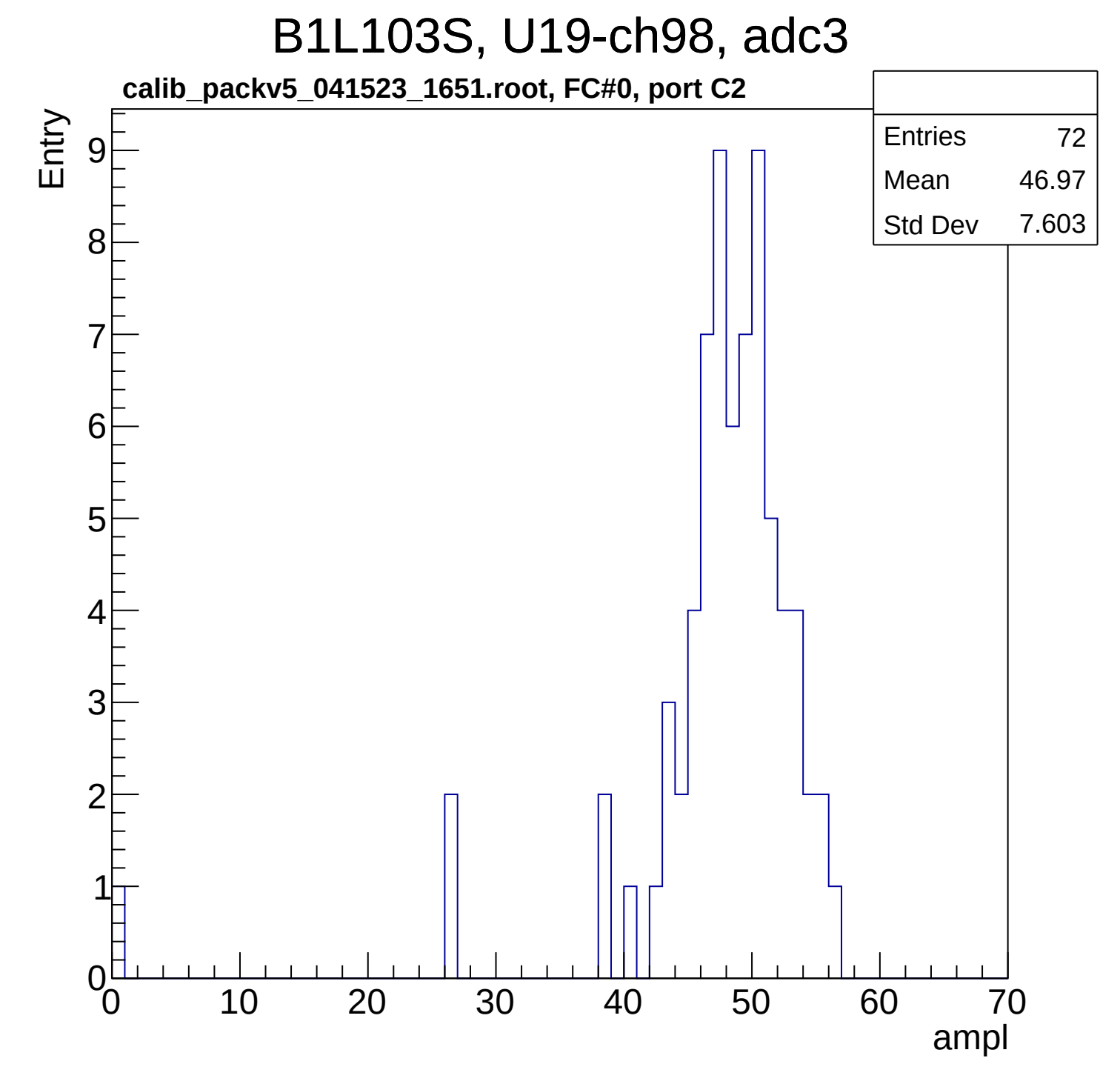

B1L103S, U19-ch97, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 61.8
Std Dev 1.47
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

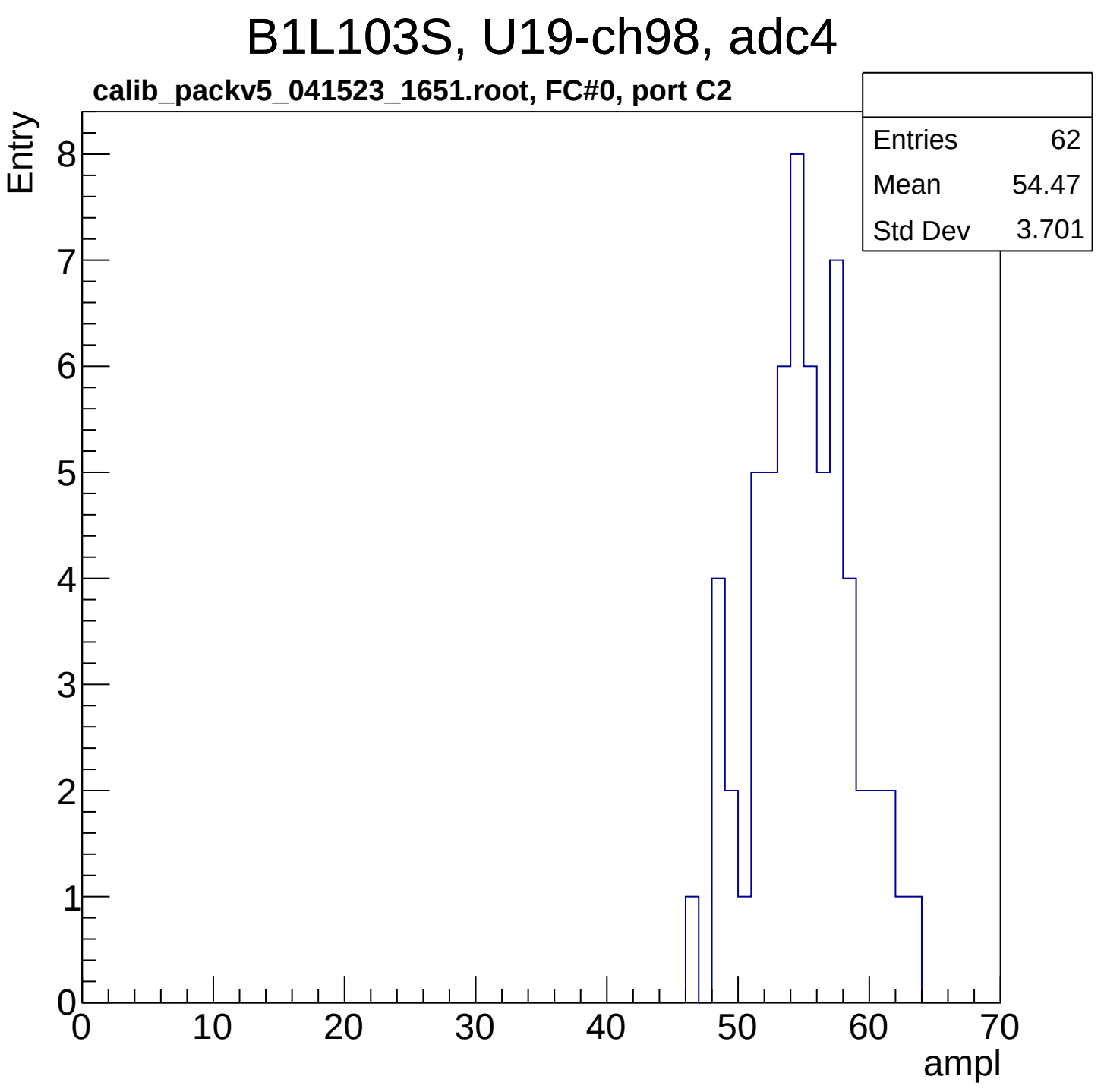

B1L103S, U19-ch97, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 3
Std Dev 13.42
Entry
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch98, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 23.99
Std Dev 11.75
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch98, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 33.12
Std Dev 9.523
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch98, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 35.9
Std Dev 14.08
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch98, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 46.97
Std Dev 7.603
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch98, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 54.47
Std Dev 3.701
Entry
ampl
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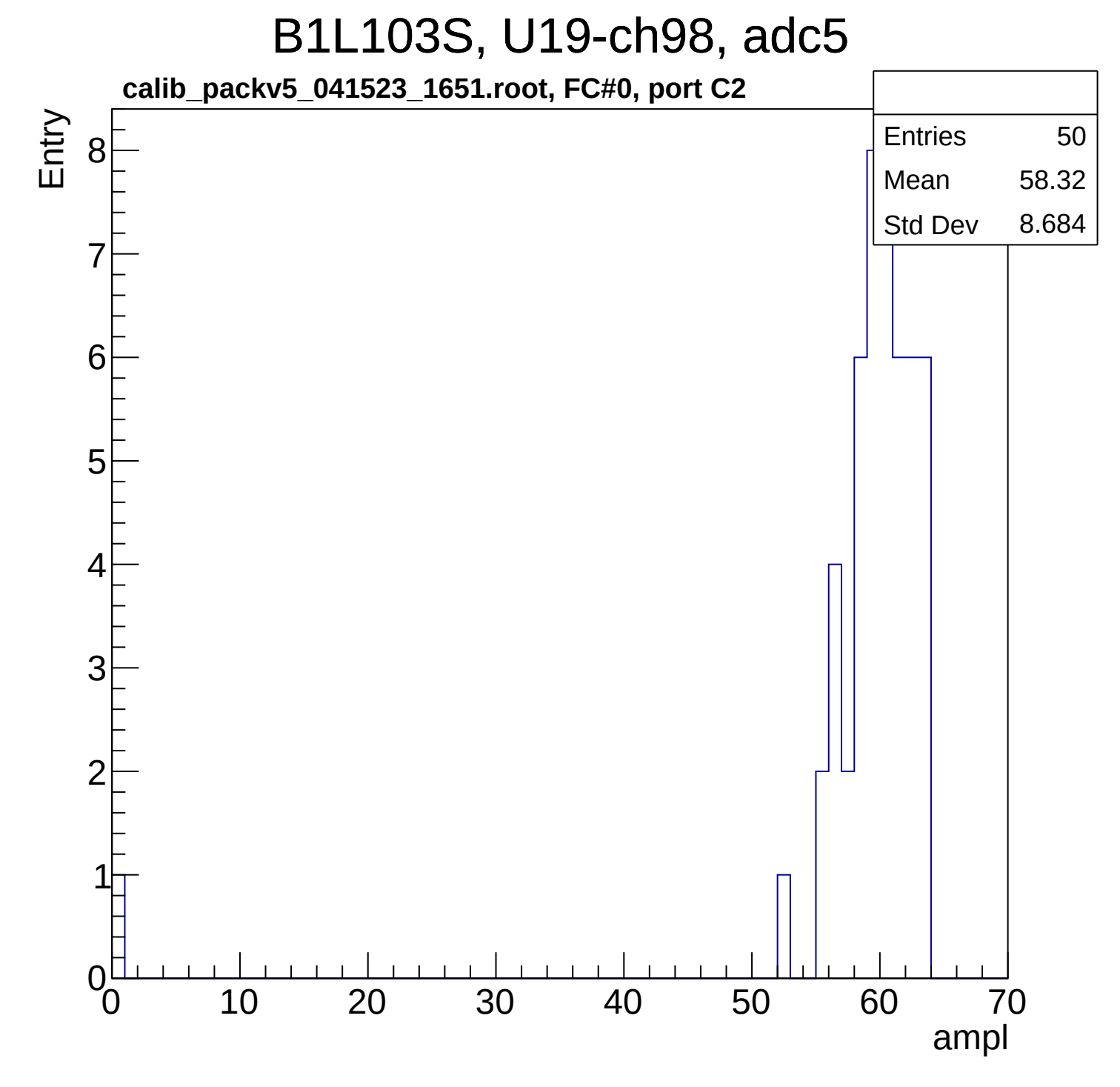
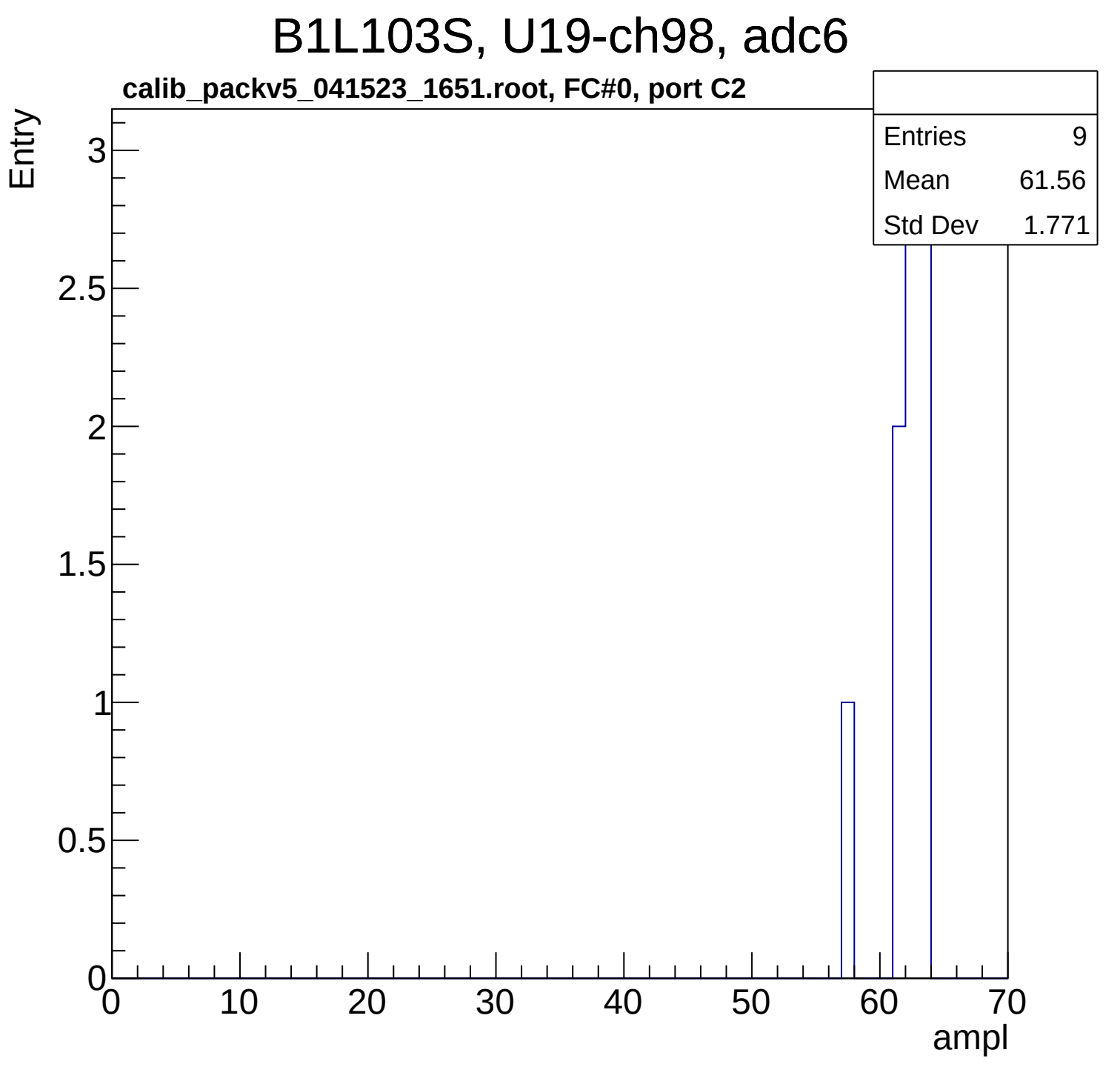
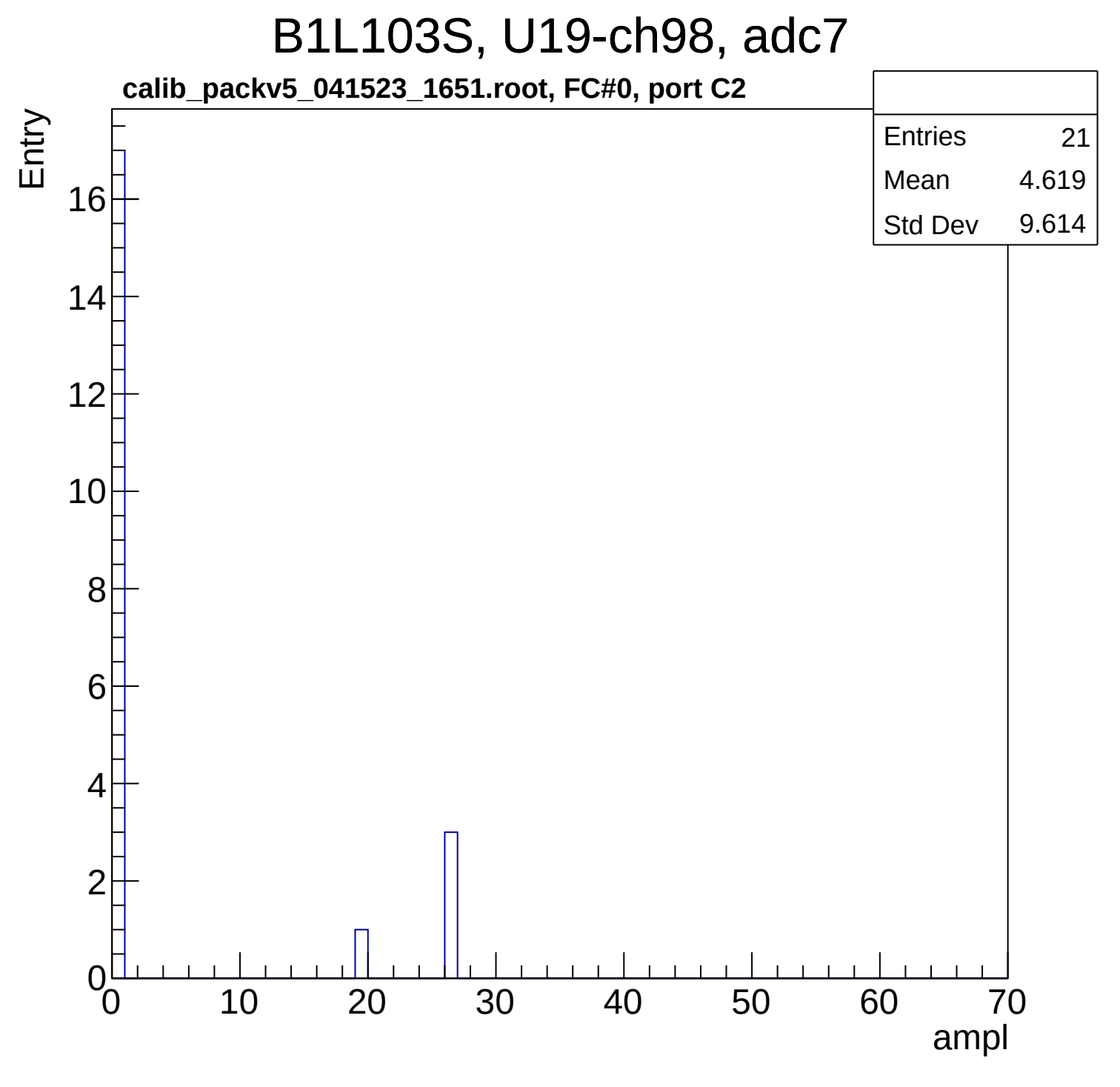
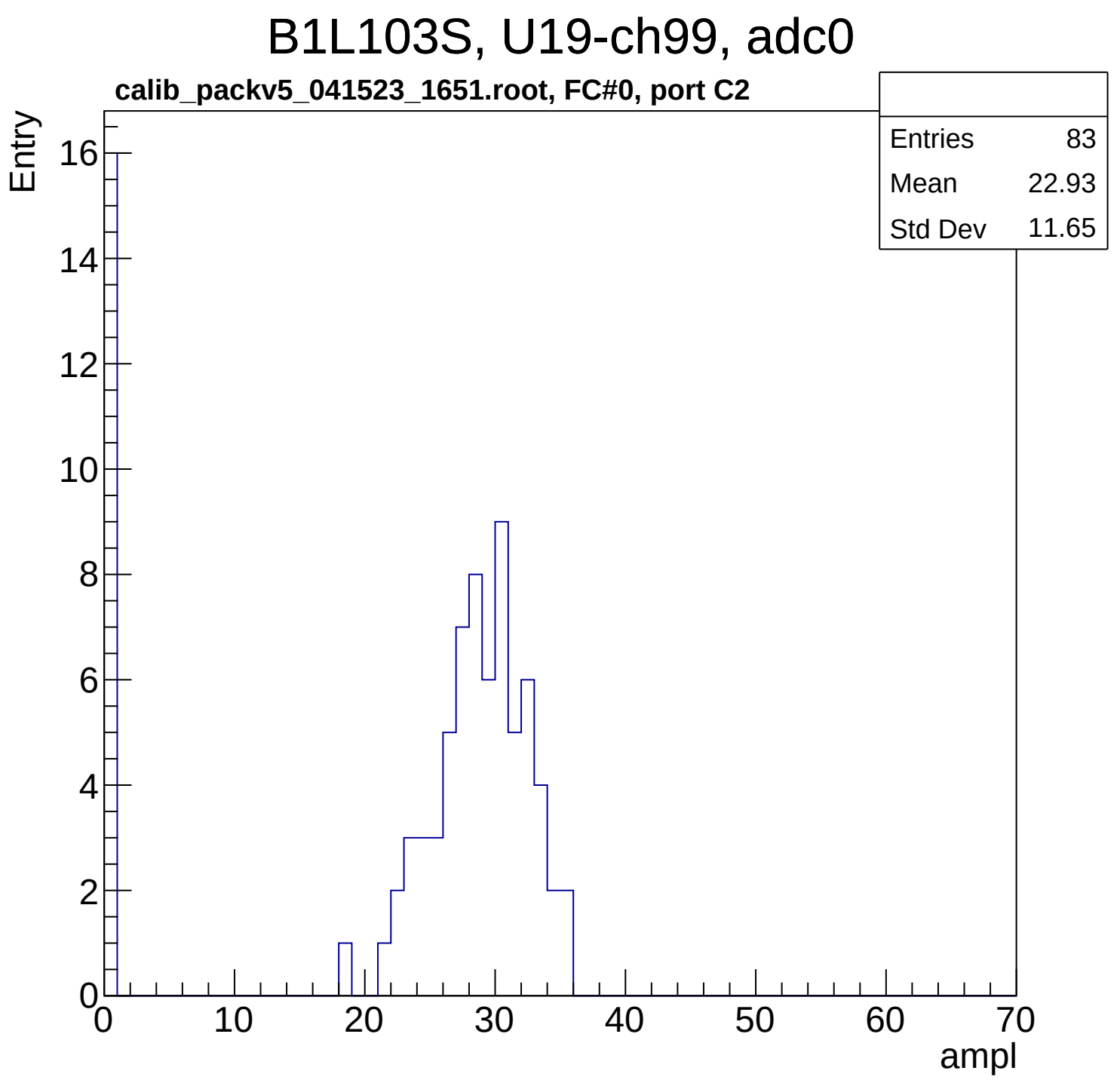
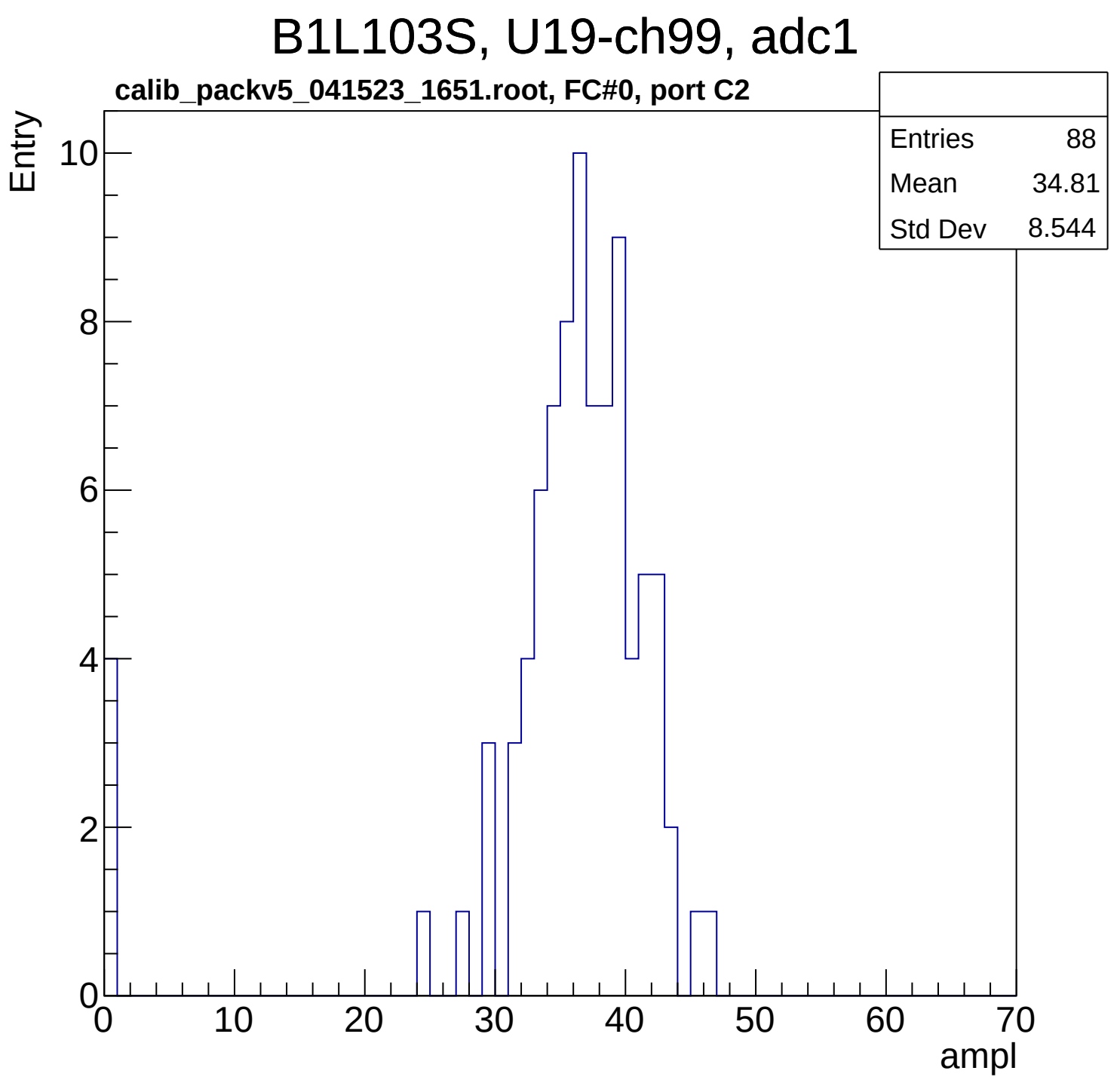
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

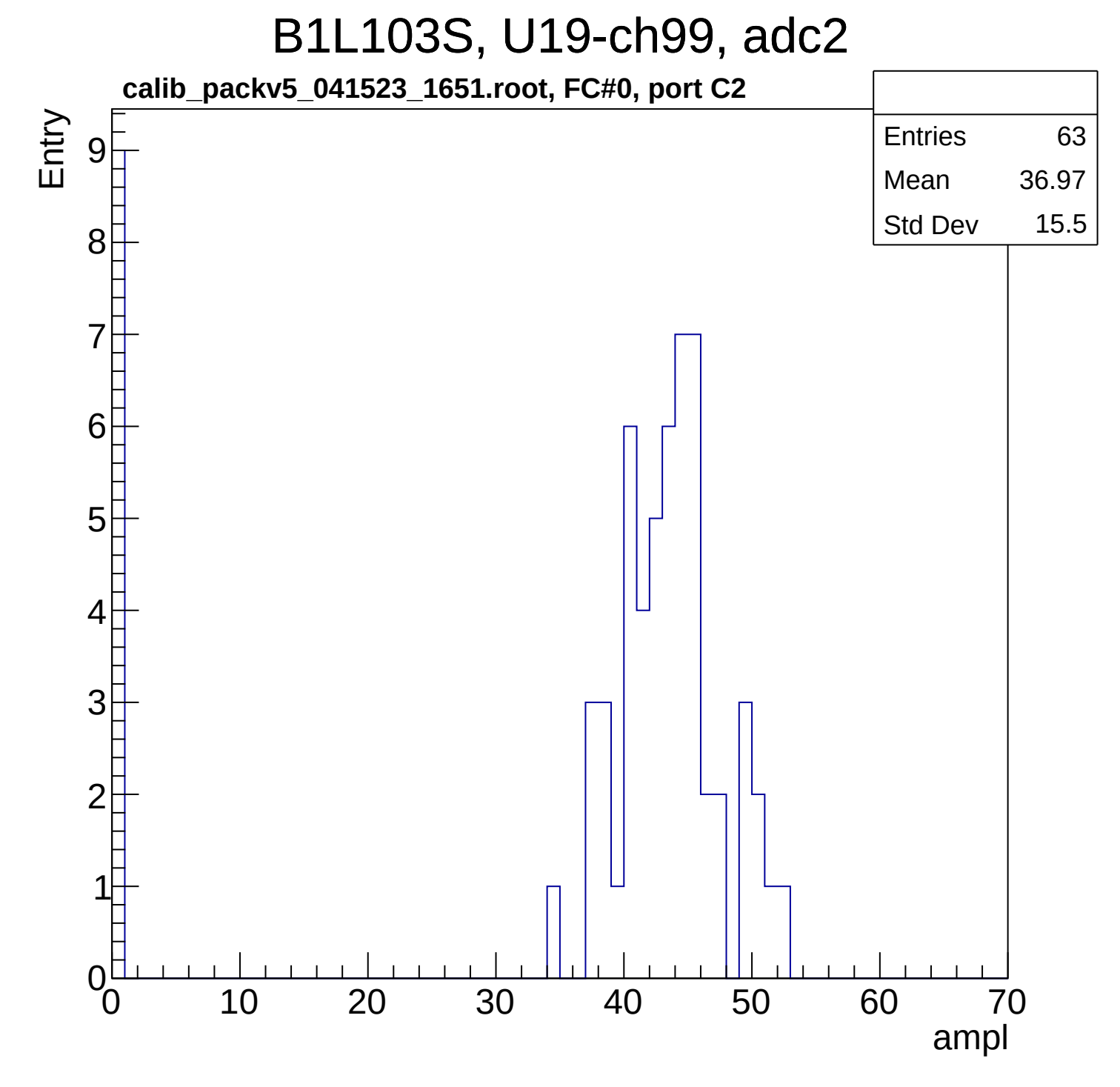

B1L103S, U19-ch98, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 58.32
Std Dev 8.684
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

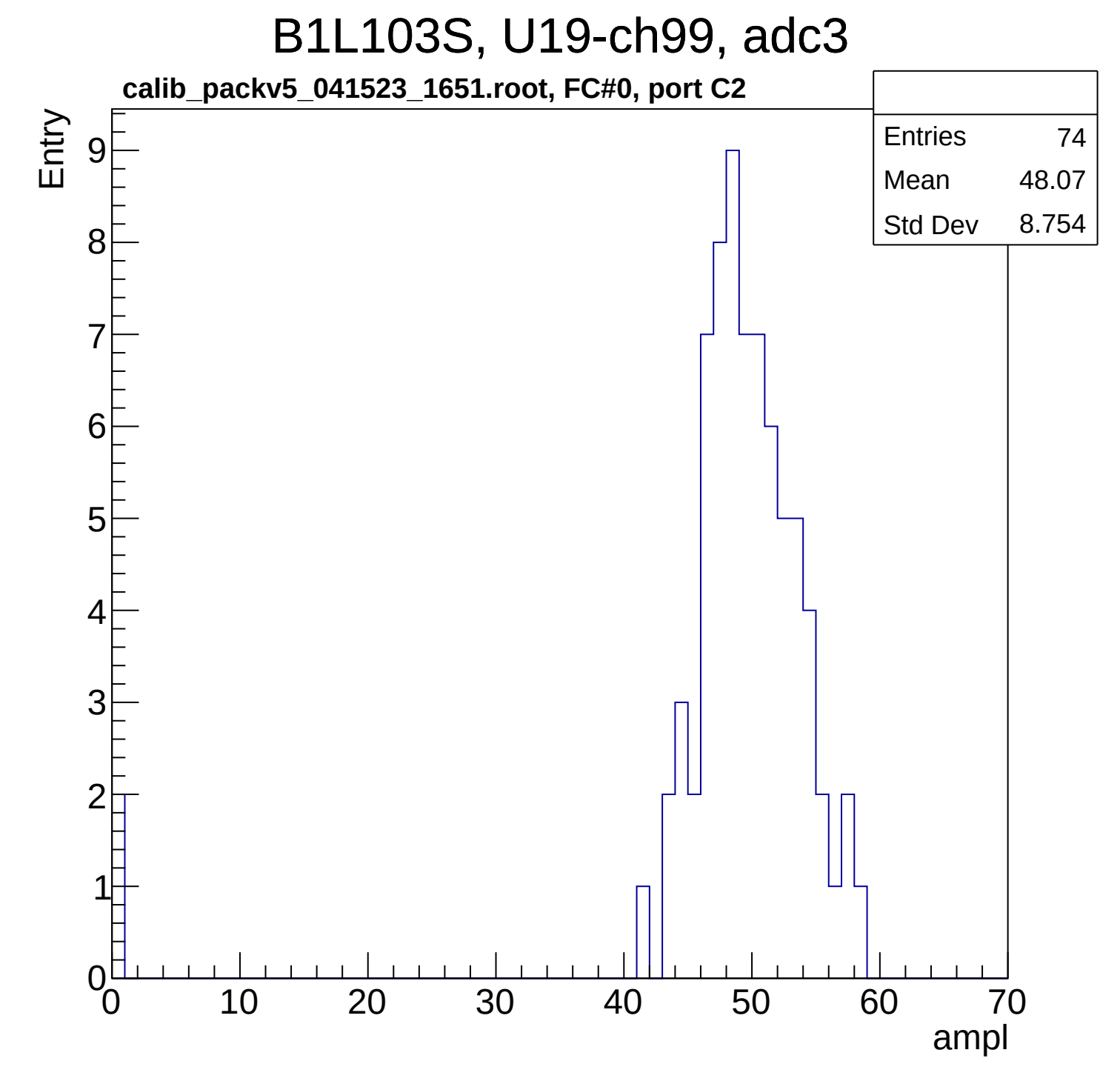

B1L103S, U19-ch98, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 61.56
Std Dev 1.771
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U19-ch98, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 4.619
Std Dev 9.614
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch99, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 22.93
Std Dev 11.65
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch99, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 34.81
Std Dev 8.544
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U19-ch99, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 36.97
Std Dev 15.5
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch99, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 48.07
Std Dev 8.754
Entry
ampl
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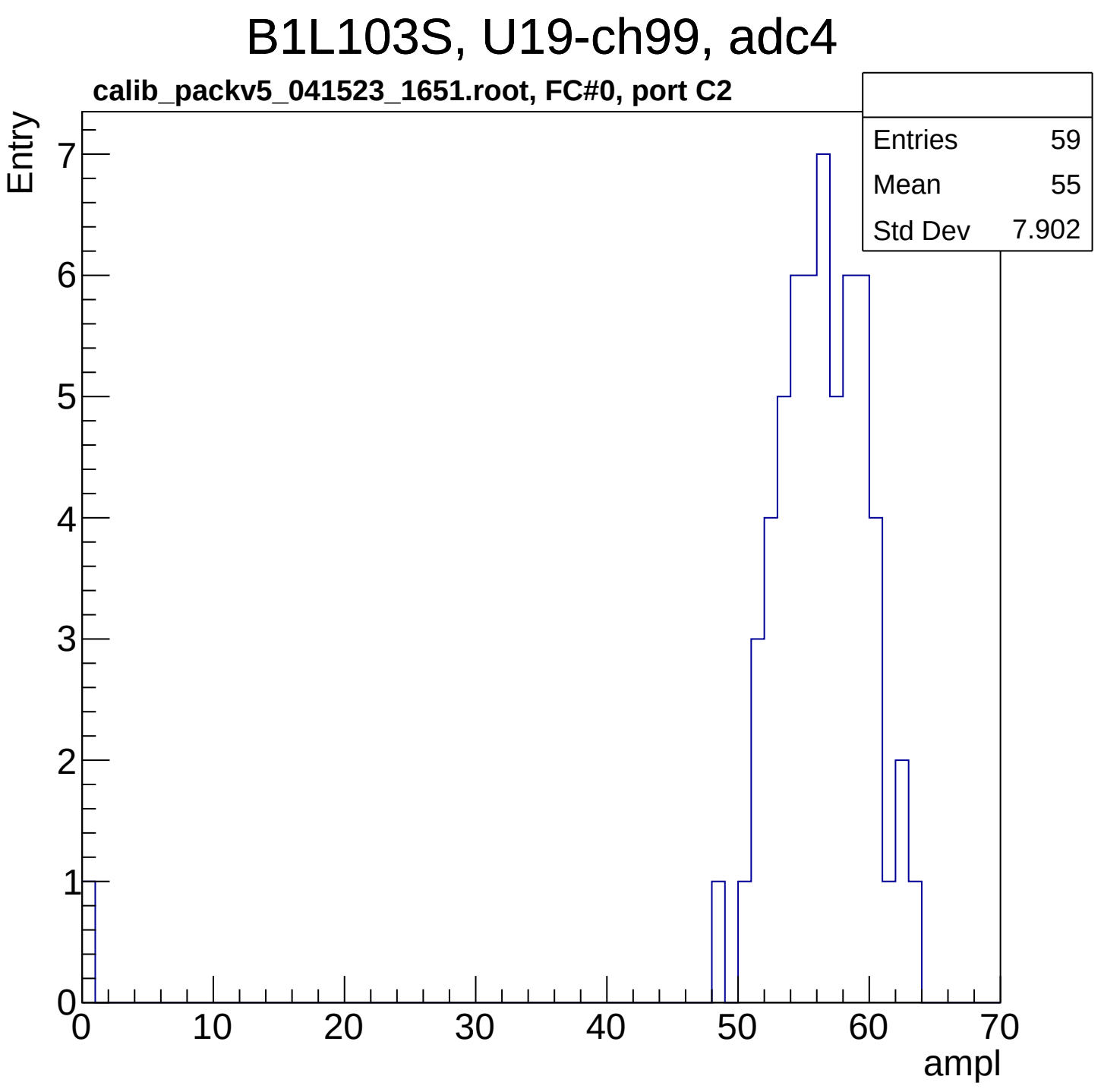
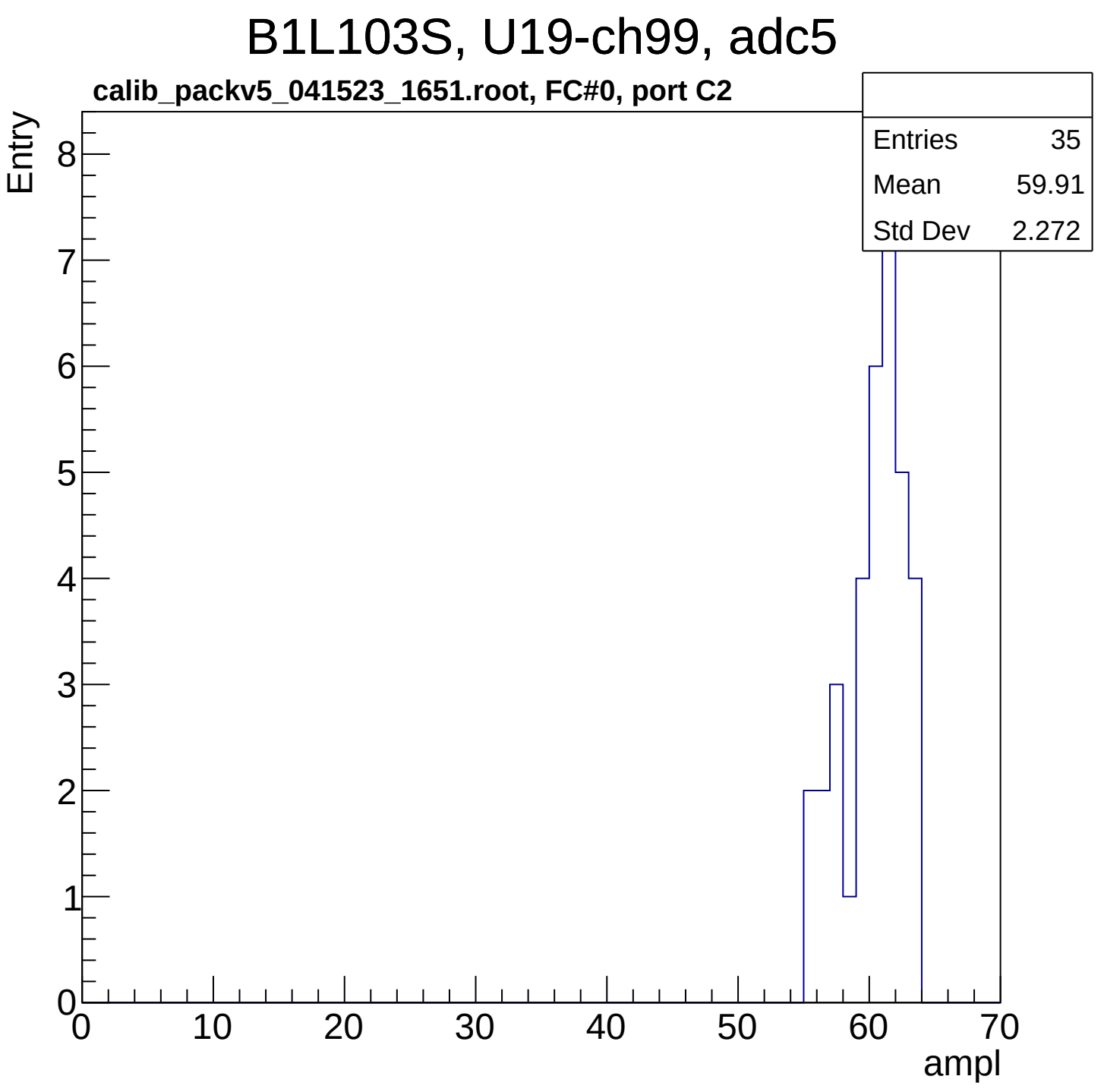
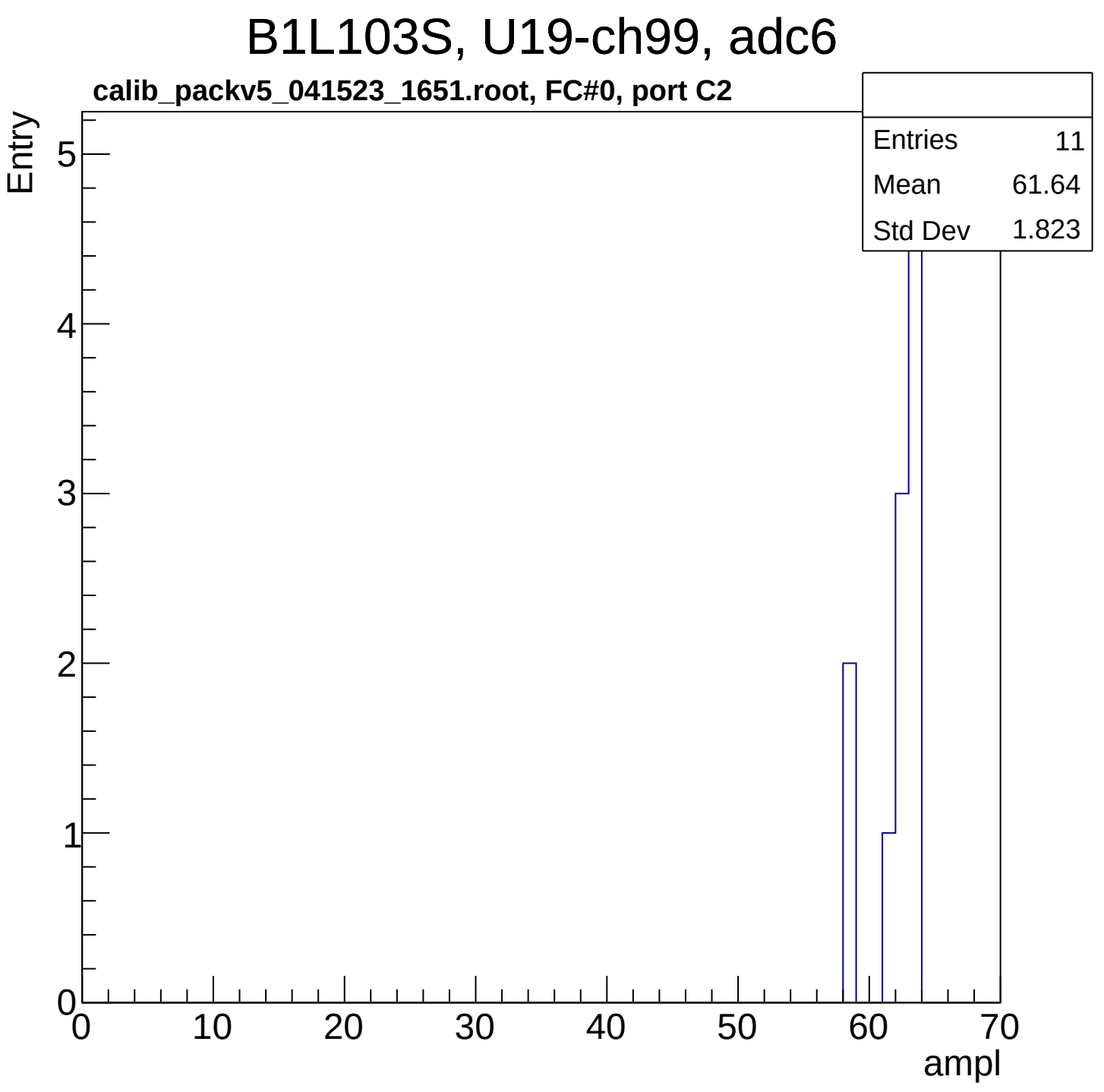
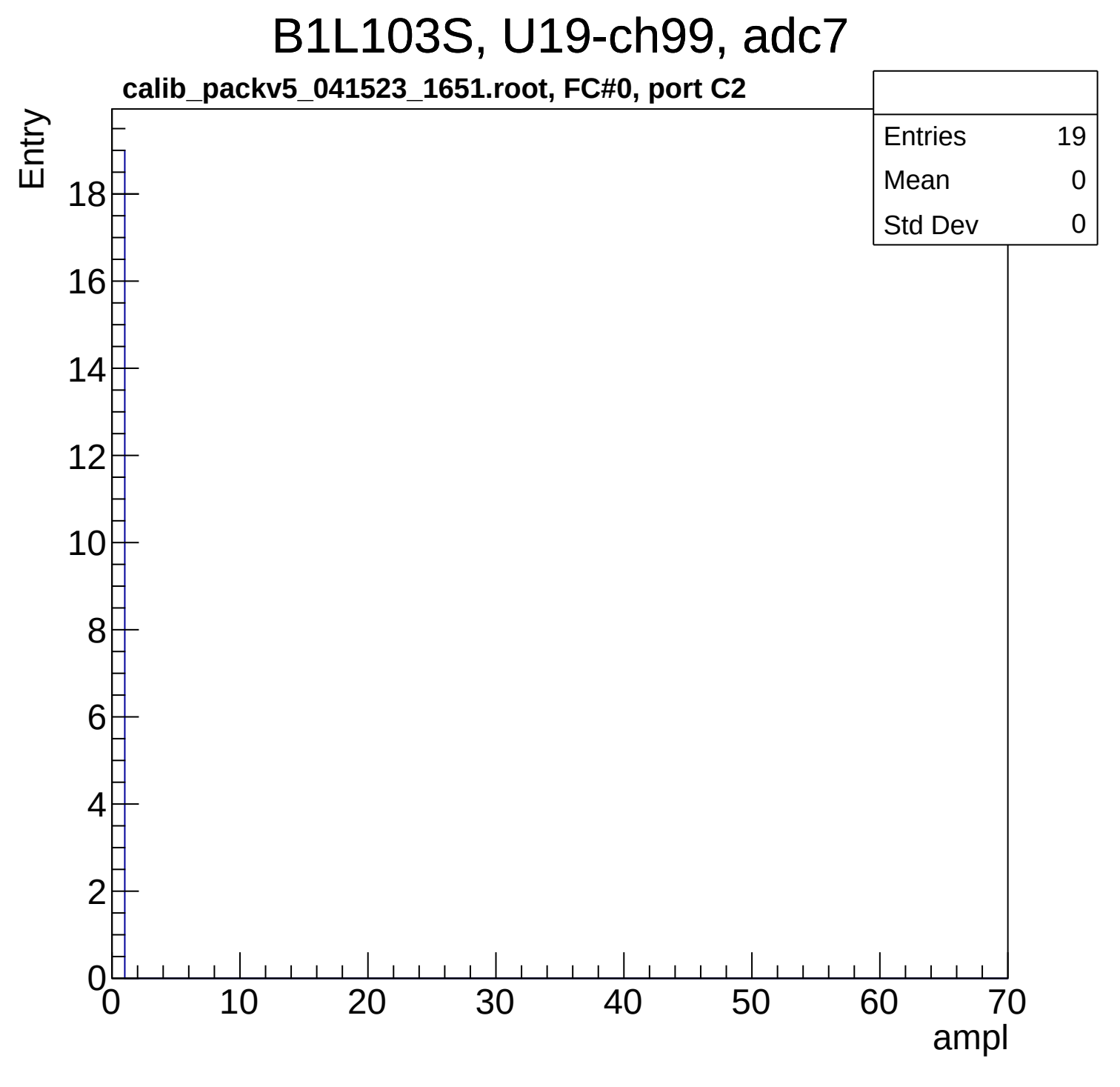
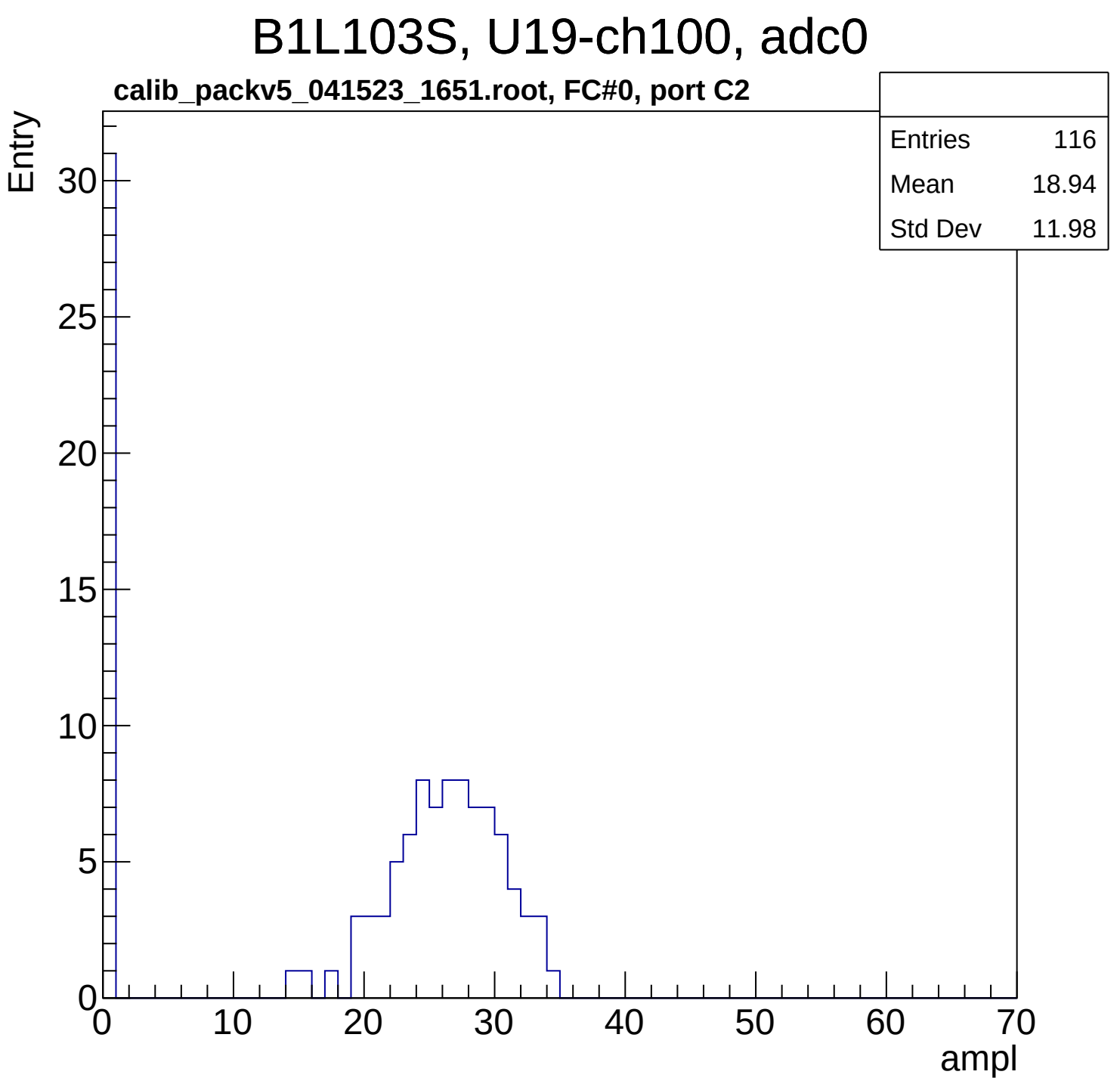
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

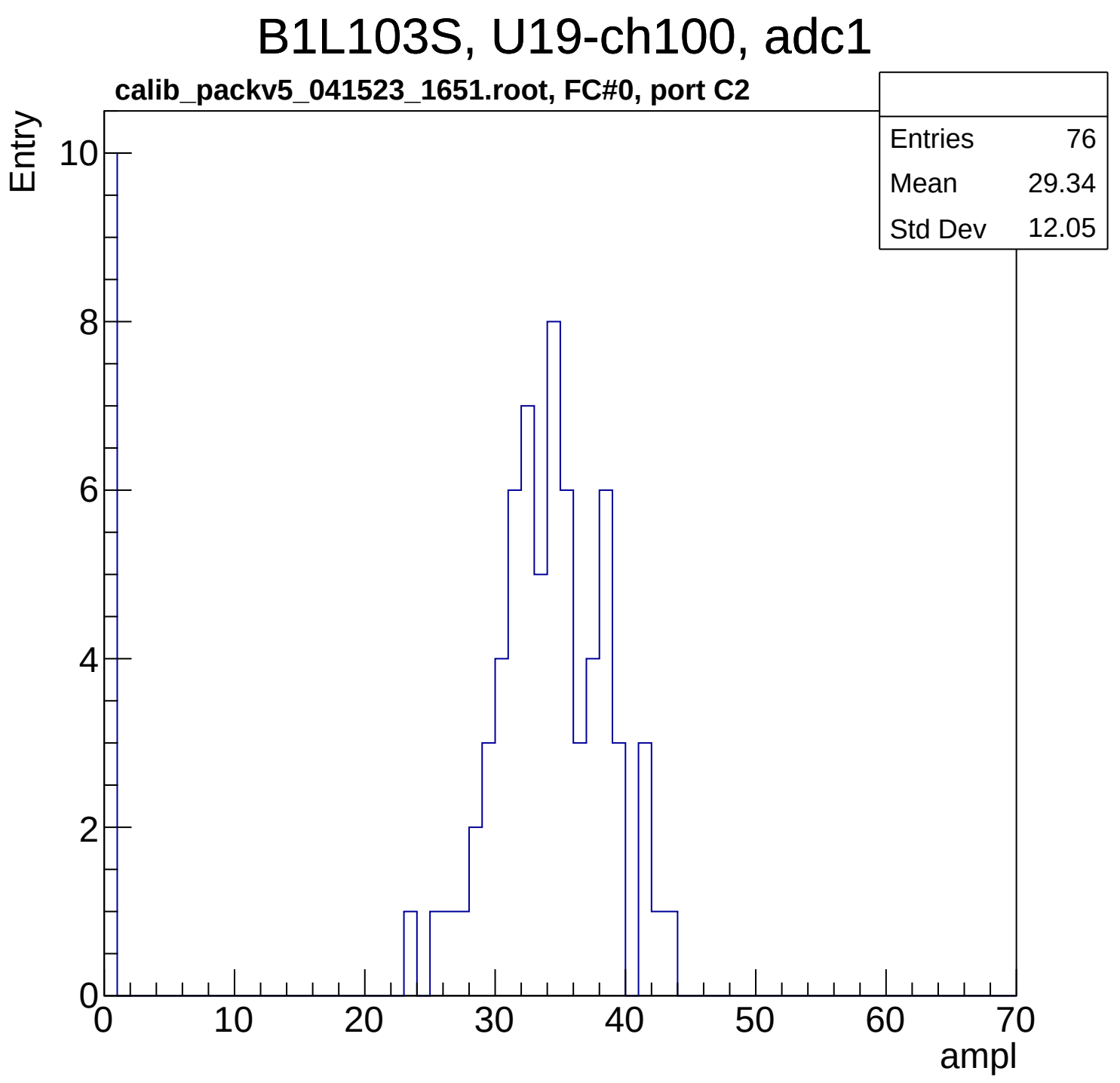

B1L103S, U19-ch99, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 55
Std Dev 7.902
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

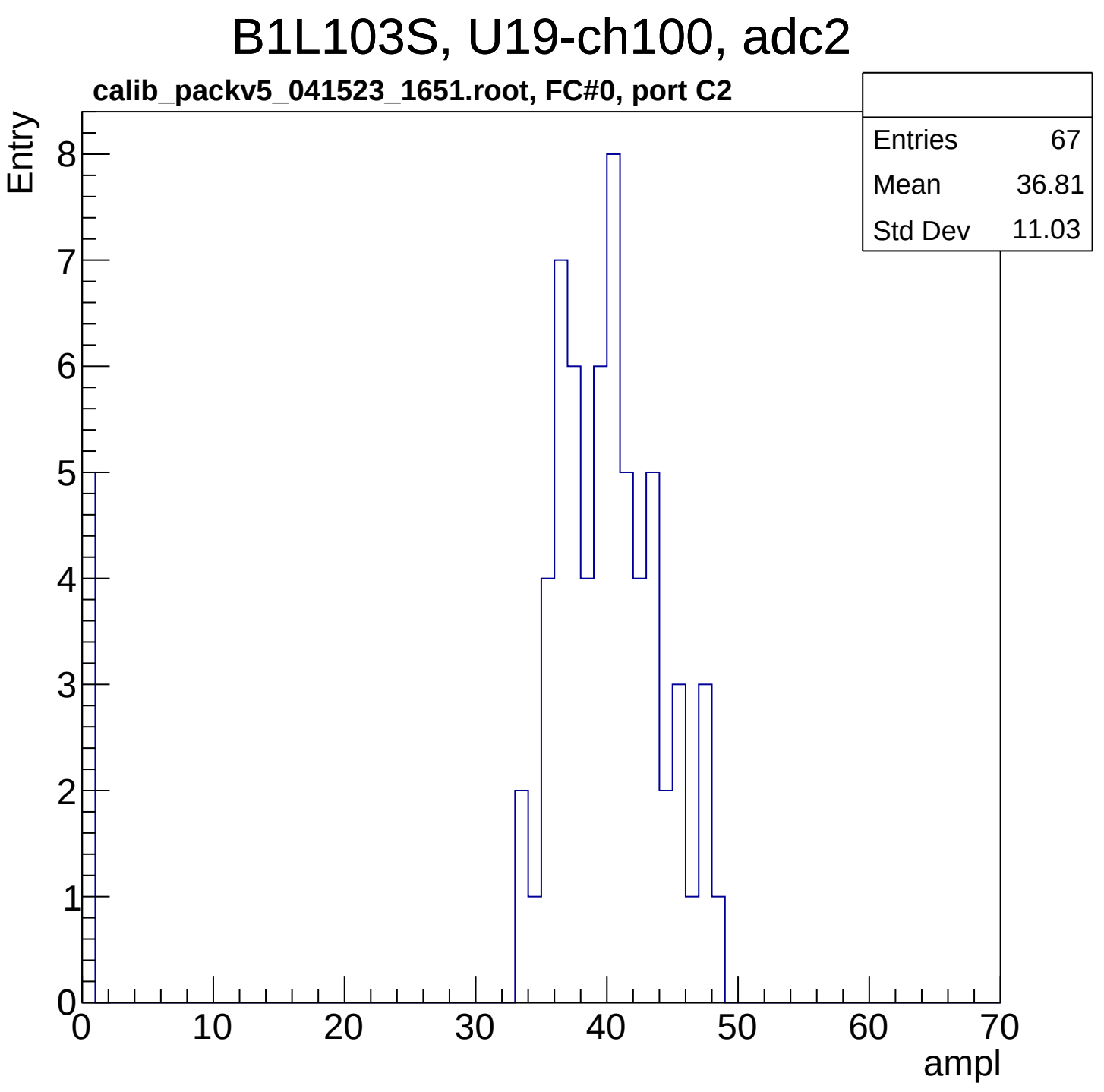

B1L103S, U19-ch99, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 59.91
Std Dev 2.272
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

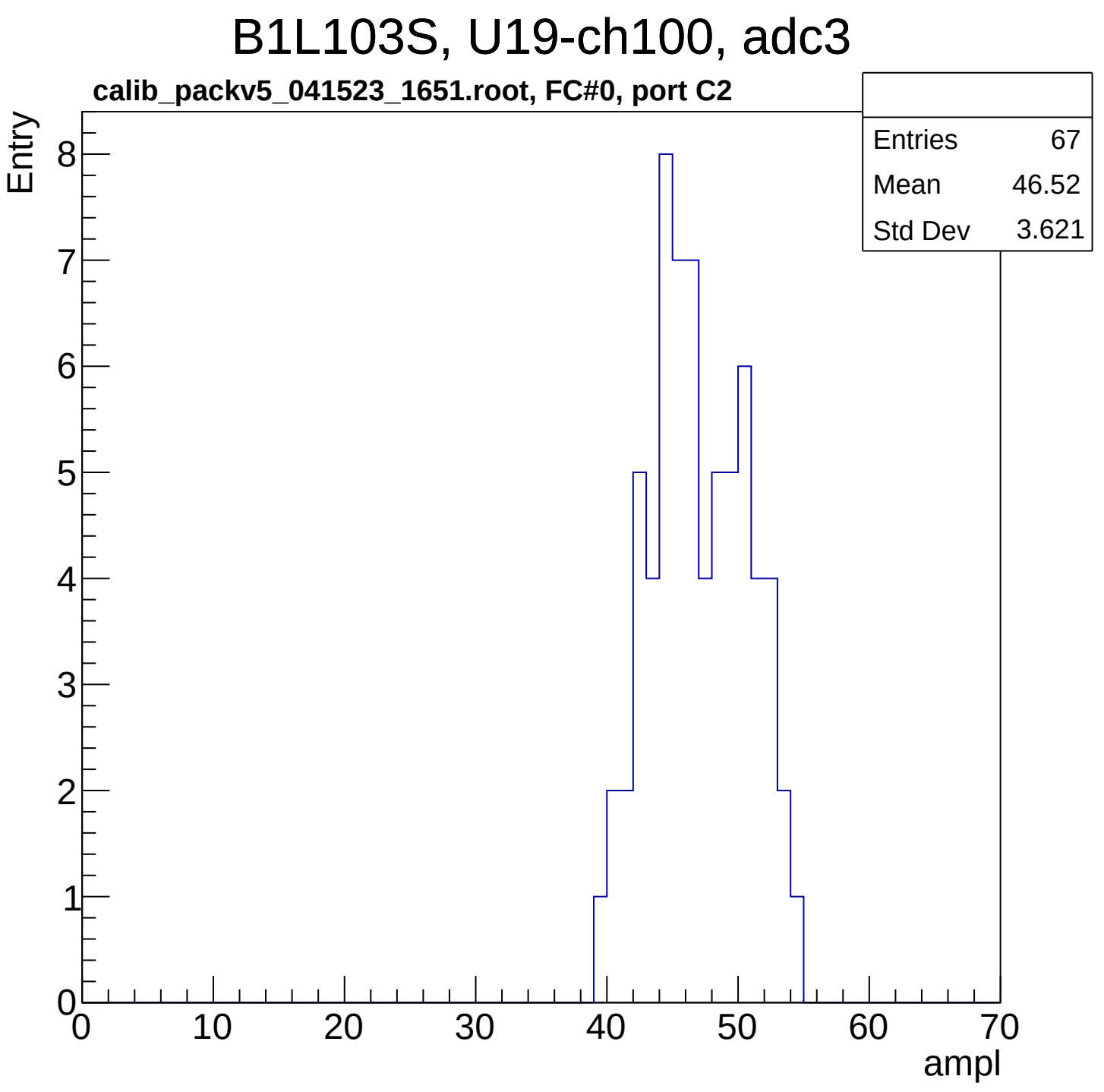

B1L103S, U19-ch99, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 61.64
Std Dev 1.823
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

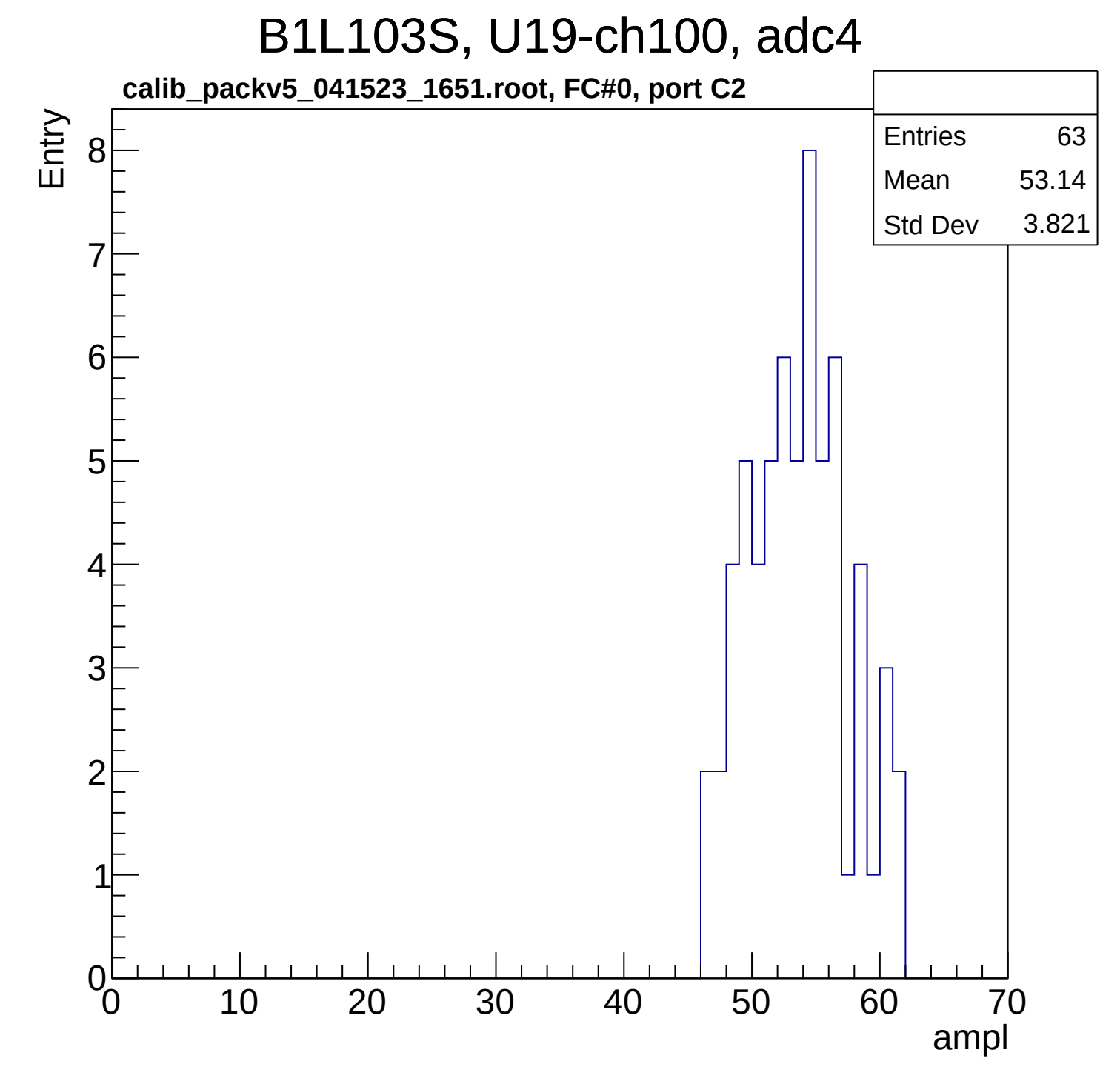

B1L103S, U19-ch99, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

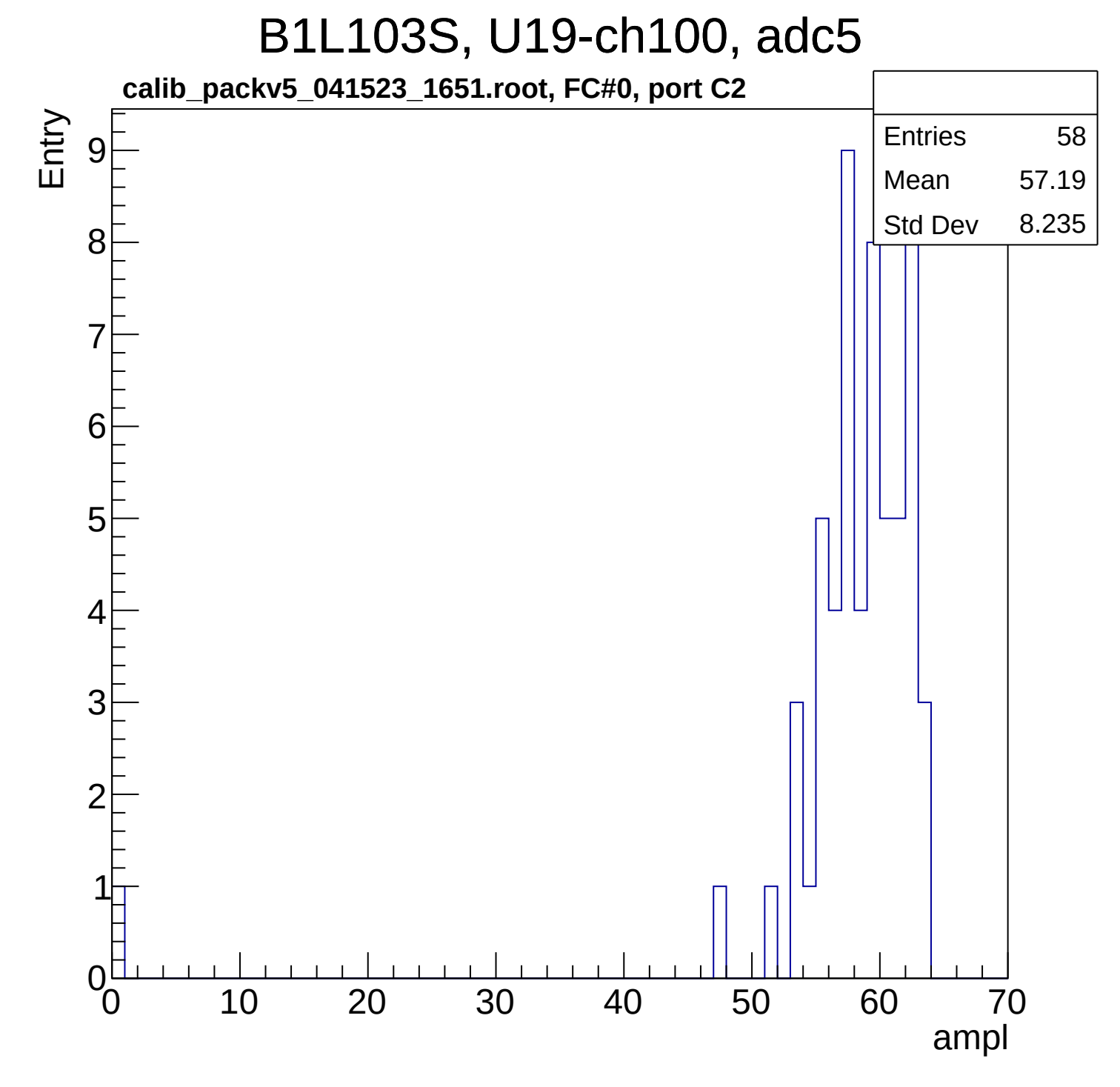

B1L103S, U19-ch100, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 116
Mean 18.94
Std Dev 11.98
Entry
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70
ampl

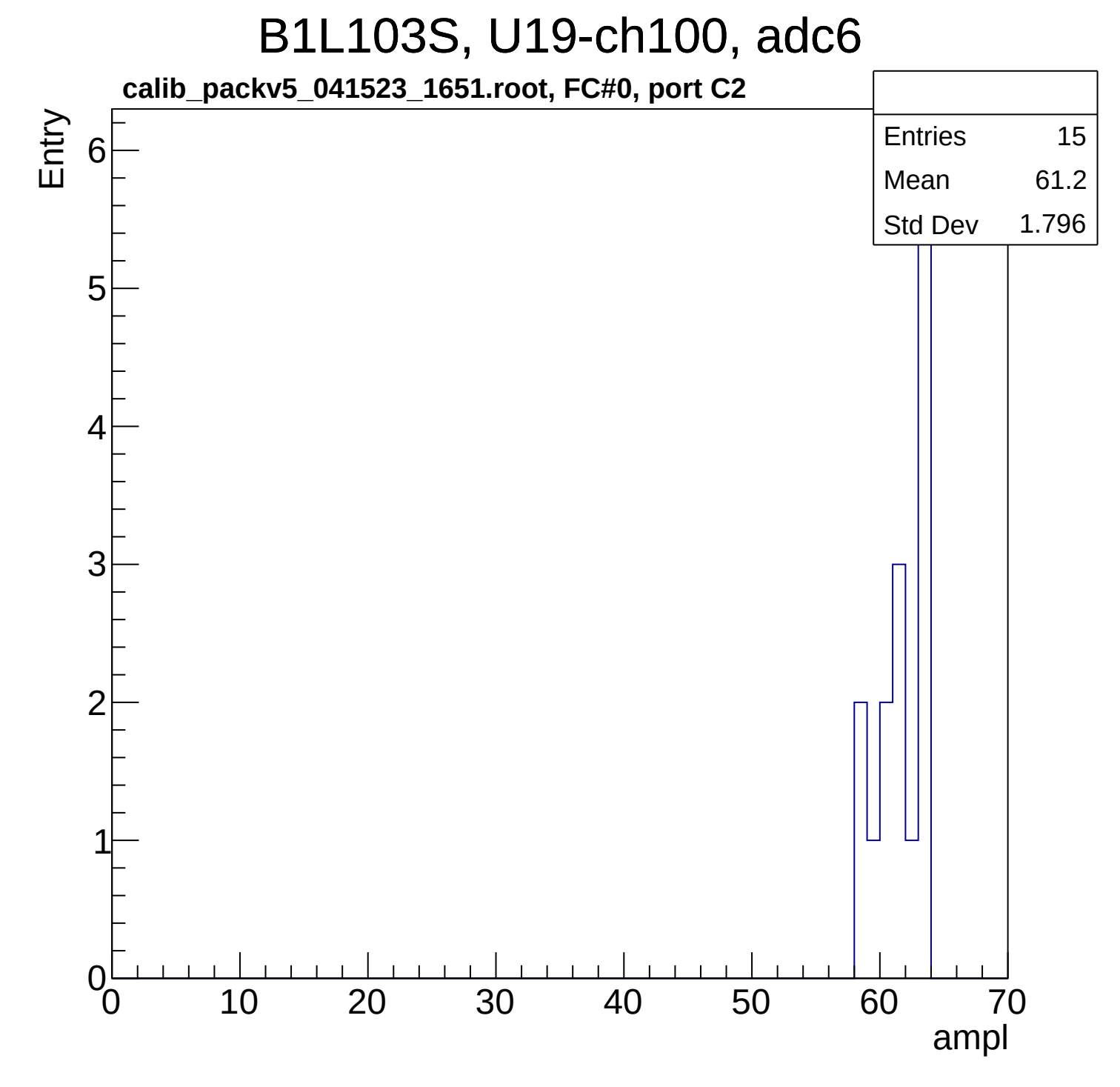

B1L103S, U19-ch100, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 29.34
Std Dev 12.05
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch100, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 36.81
Std Dev 11.03
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch100, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 46.52
Std Dev 3.621
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch100, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 53.14
Std Dev 3.821
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch100, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 57.19
Std Dev 8.235
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch100, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 61.2
Std Dev 1.796
Entry
ampl
0
1
2
3
4
5
6
0
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40
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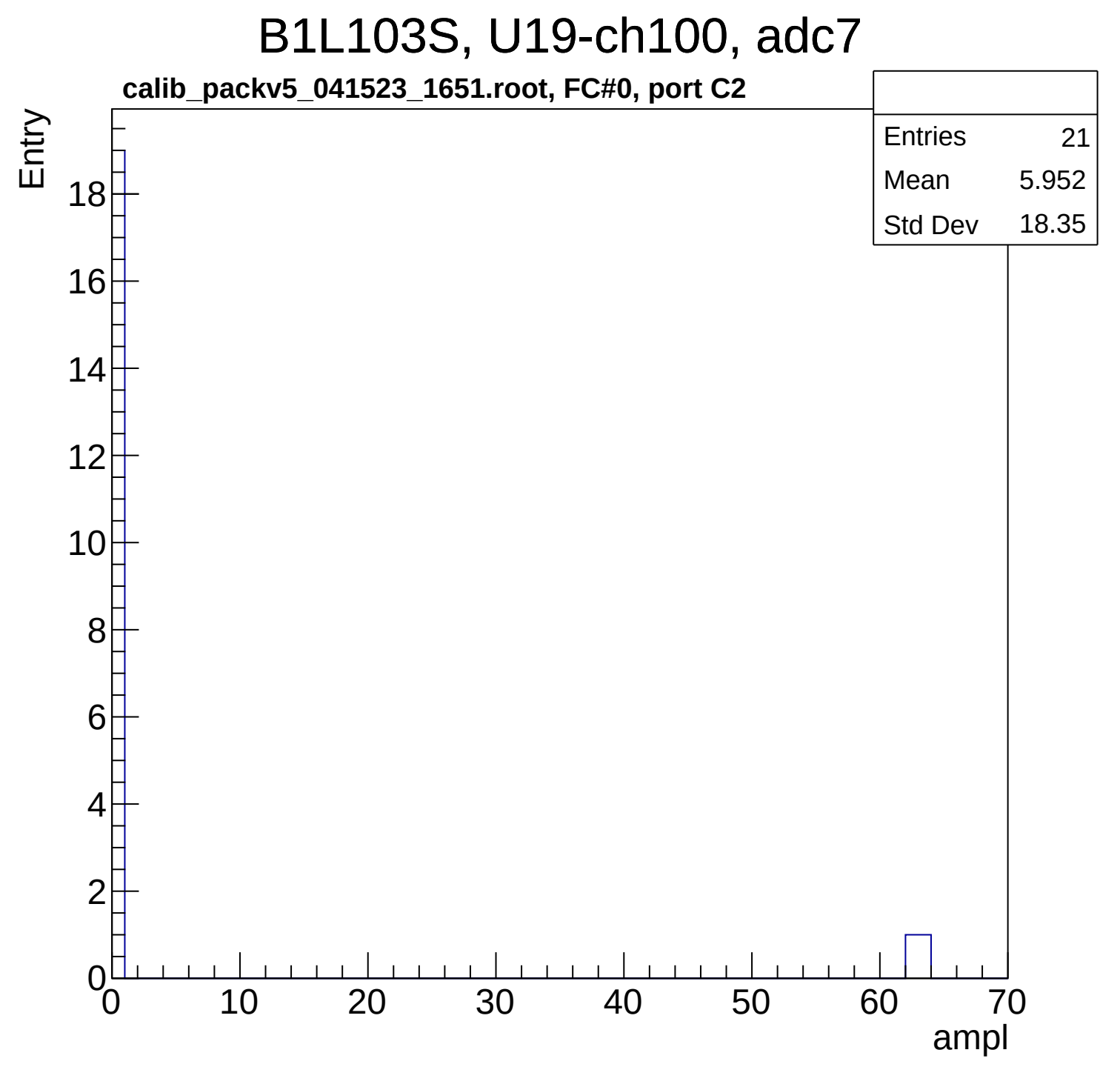
60
70


B1L103S, U19-ch100, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.952
Std Dev 18.35
Entry
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6
8
10
12
14
16
18
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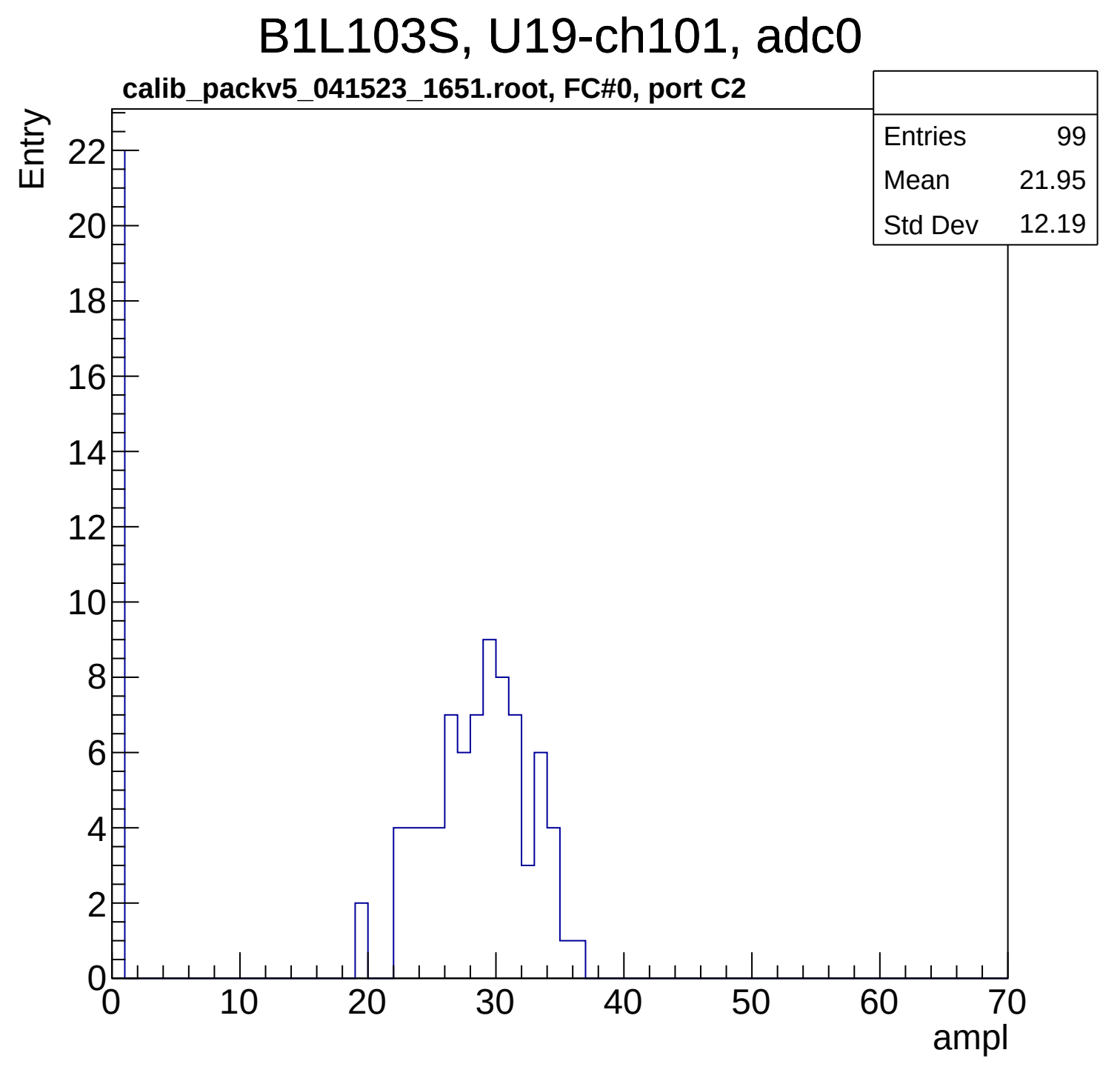
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch101, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 21.95
Std Dev 12.19
Entry
0
2
4
6
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10
12
14
16
18
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22
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10
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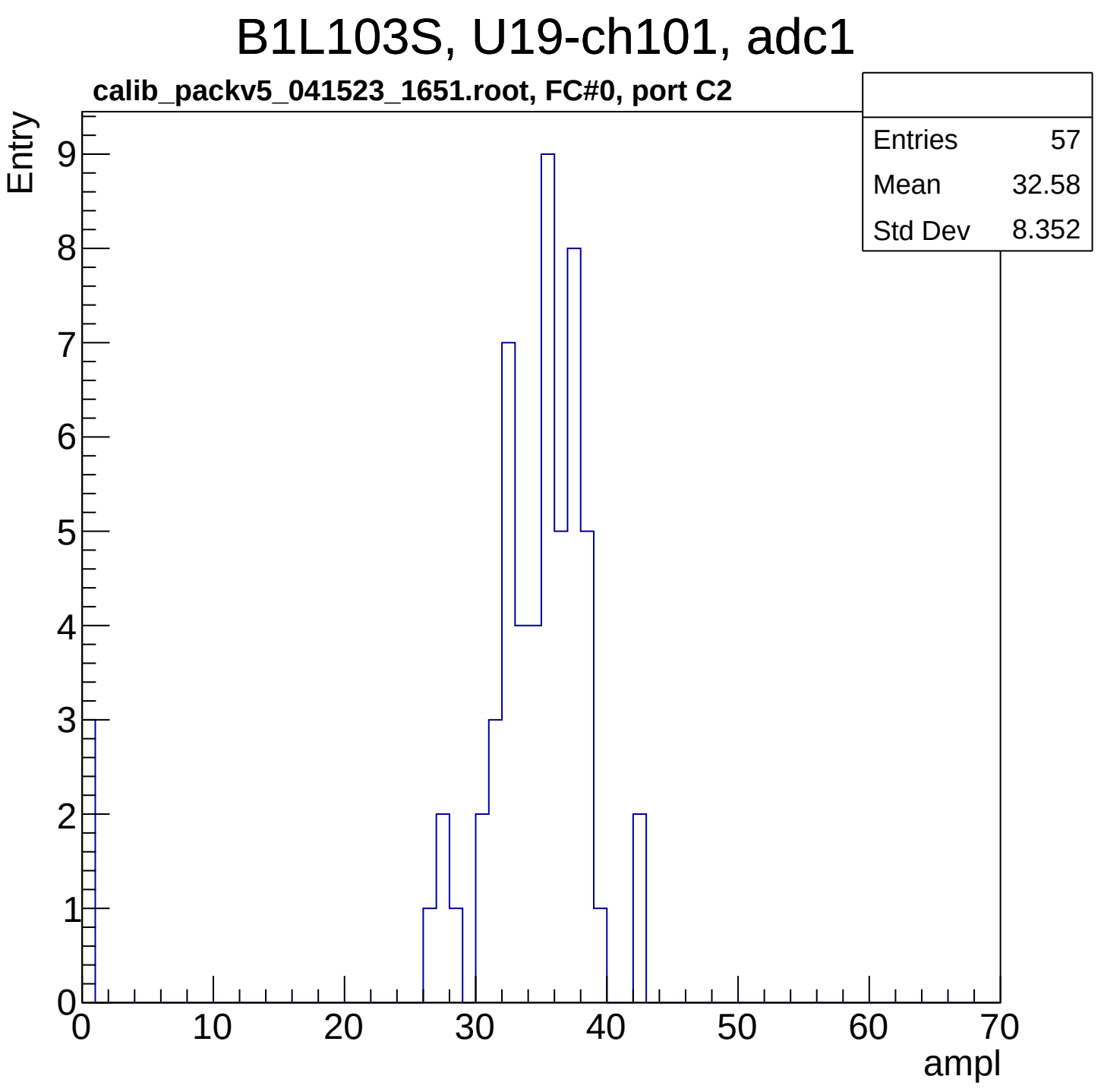
50
60
70
ampl


B1L103S, U19-ch101, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 32.58
Std Dev 8.352
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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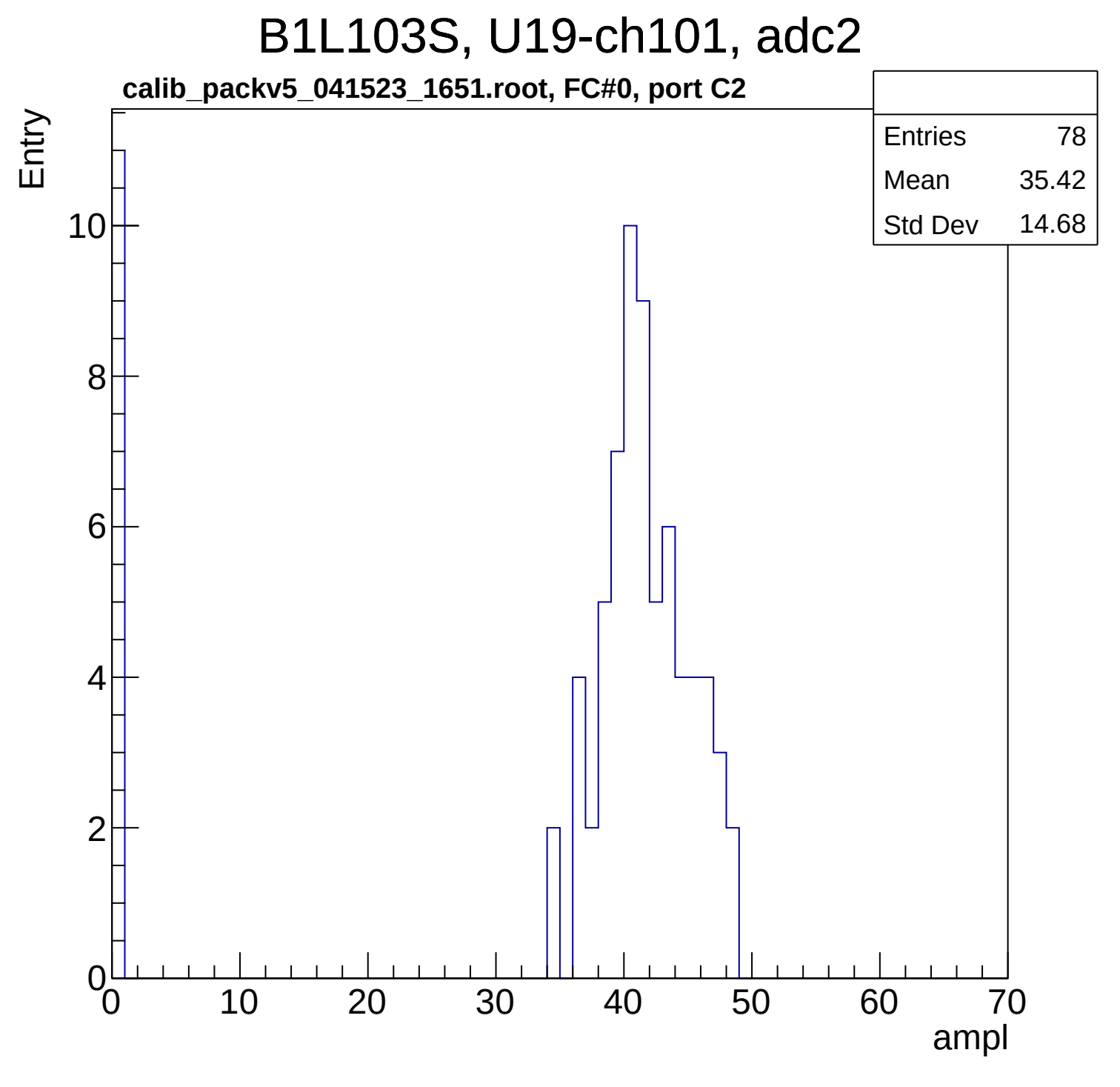
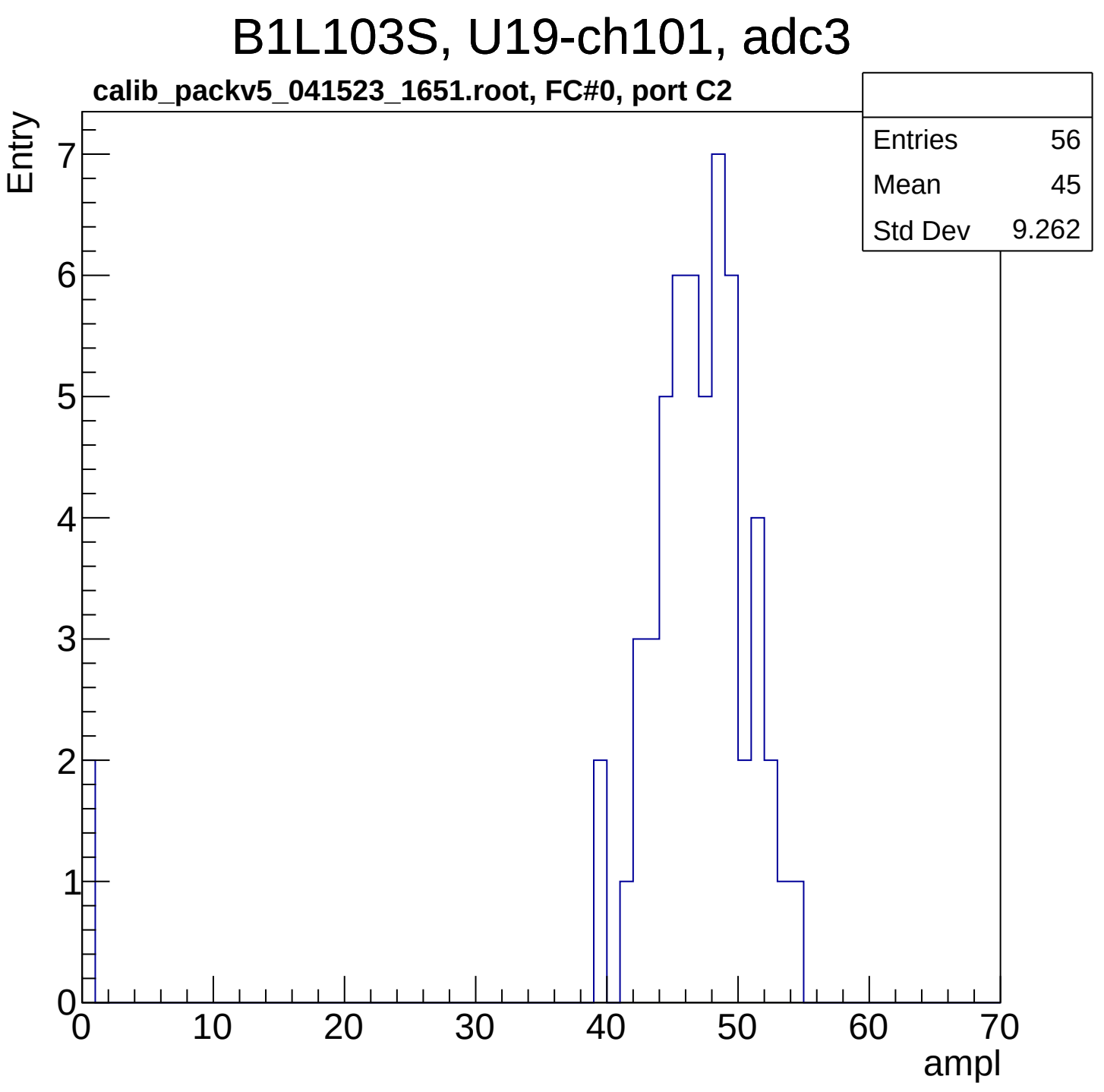

B1L103S, U19-ch101, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 35.42
Std Dev 14.68
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch101, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 45
Std Dev 9.262
Entry
ampl
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2
3
4
5
6
7
0
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40
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60
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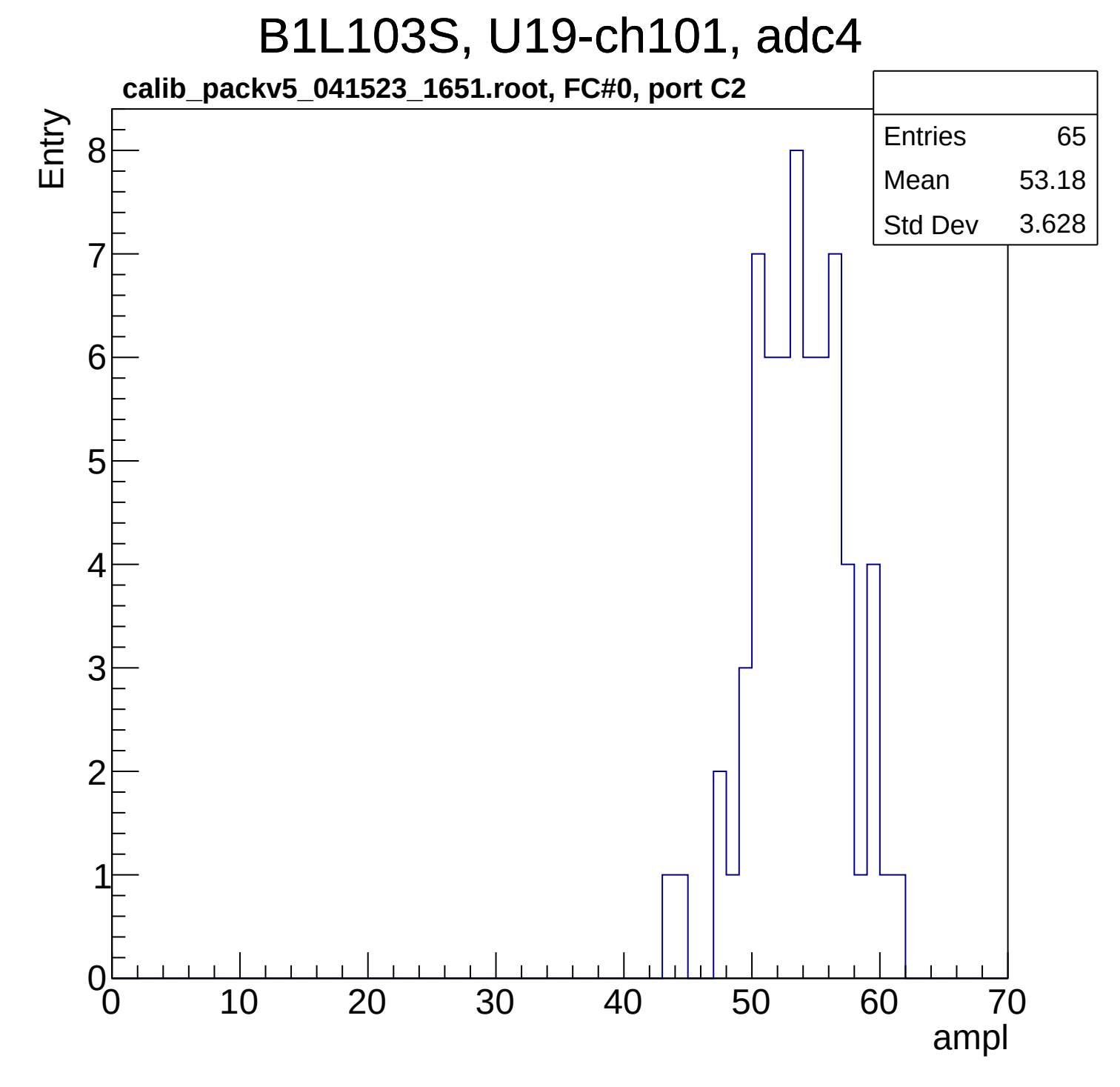
B1L103S, U19-ch101, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 53.18
Std Dev 3.628
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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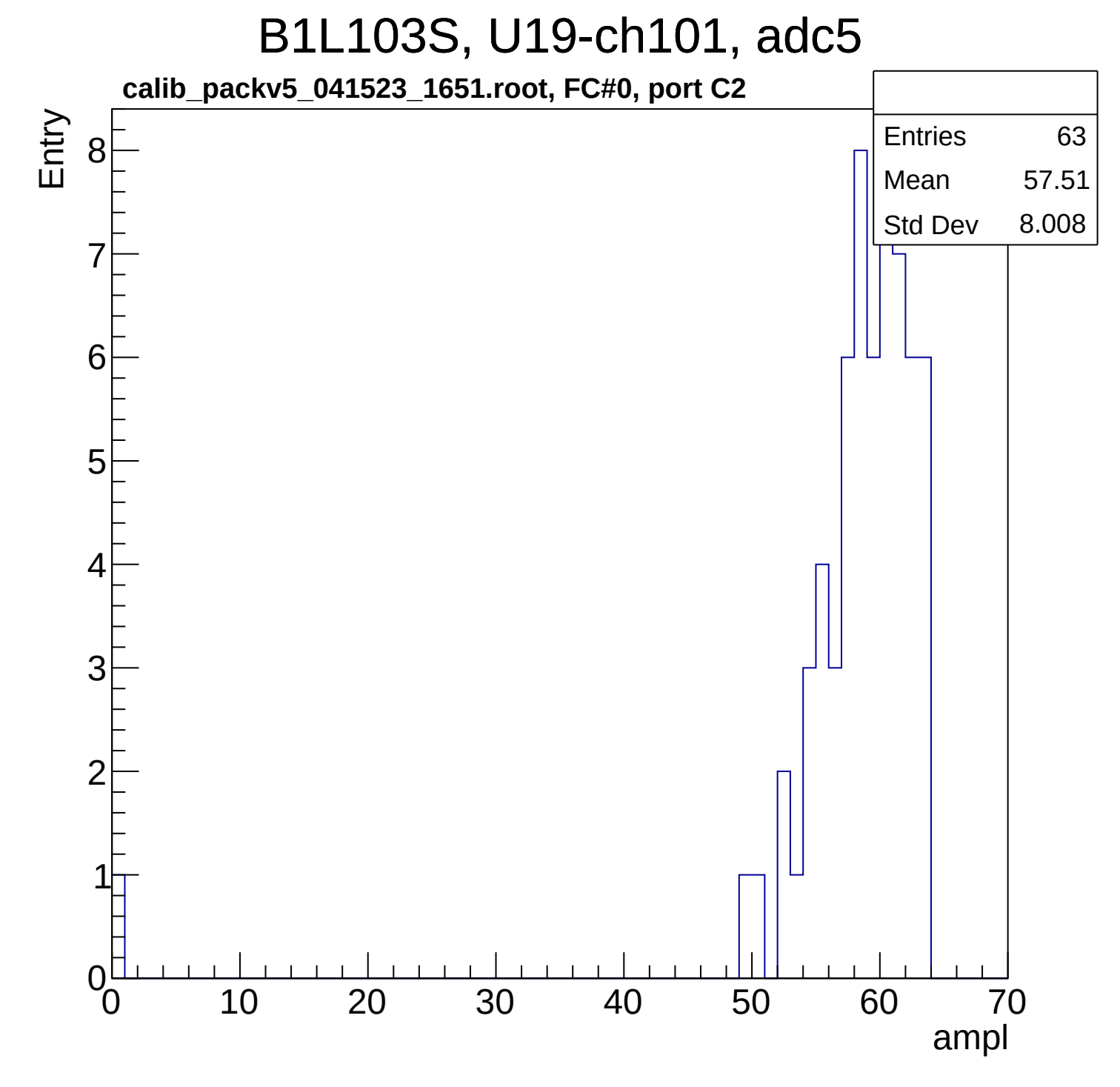
B1L103S, U19-ch101, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 57.51
Std Dev 8.008
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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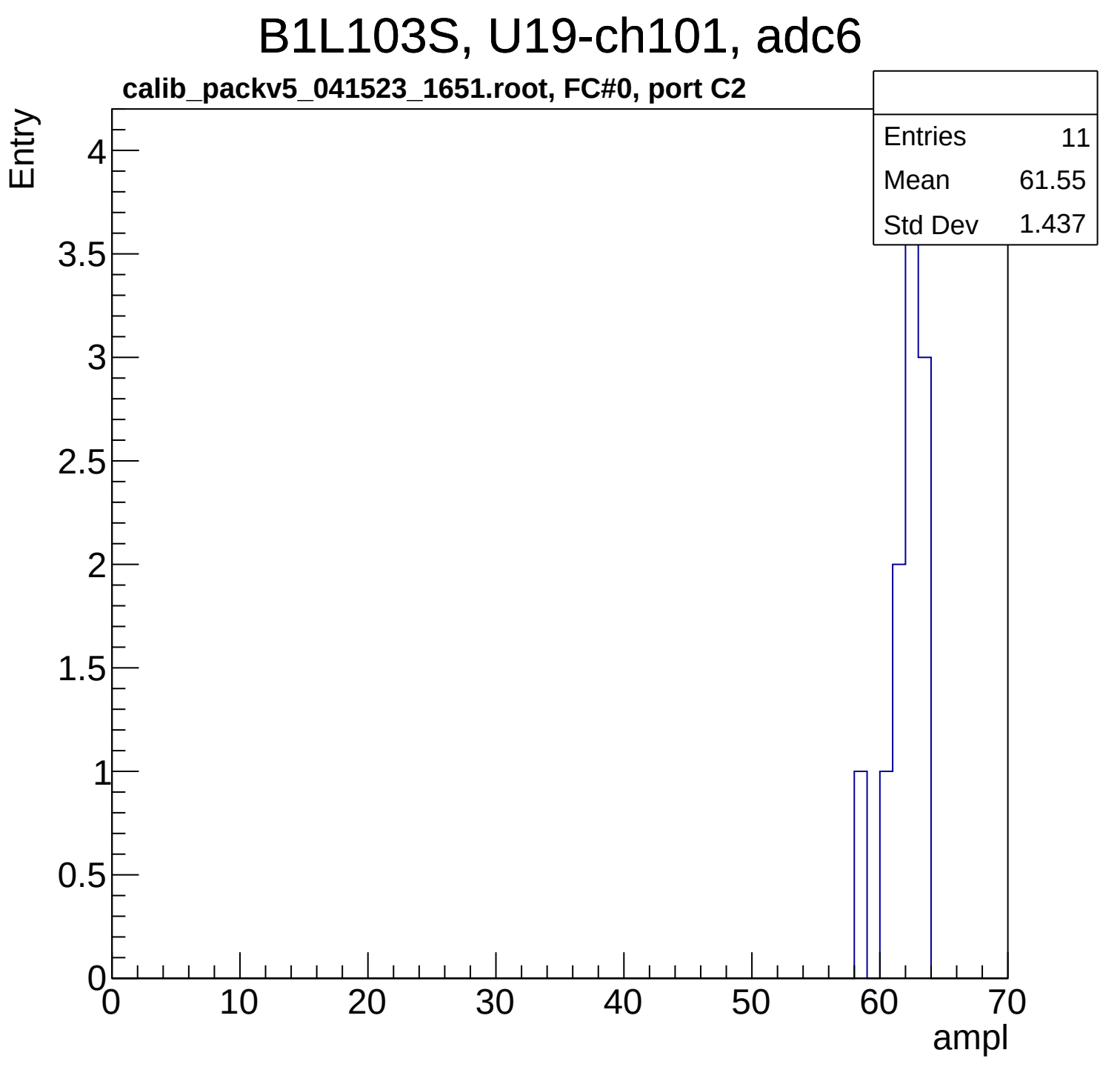
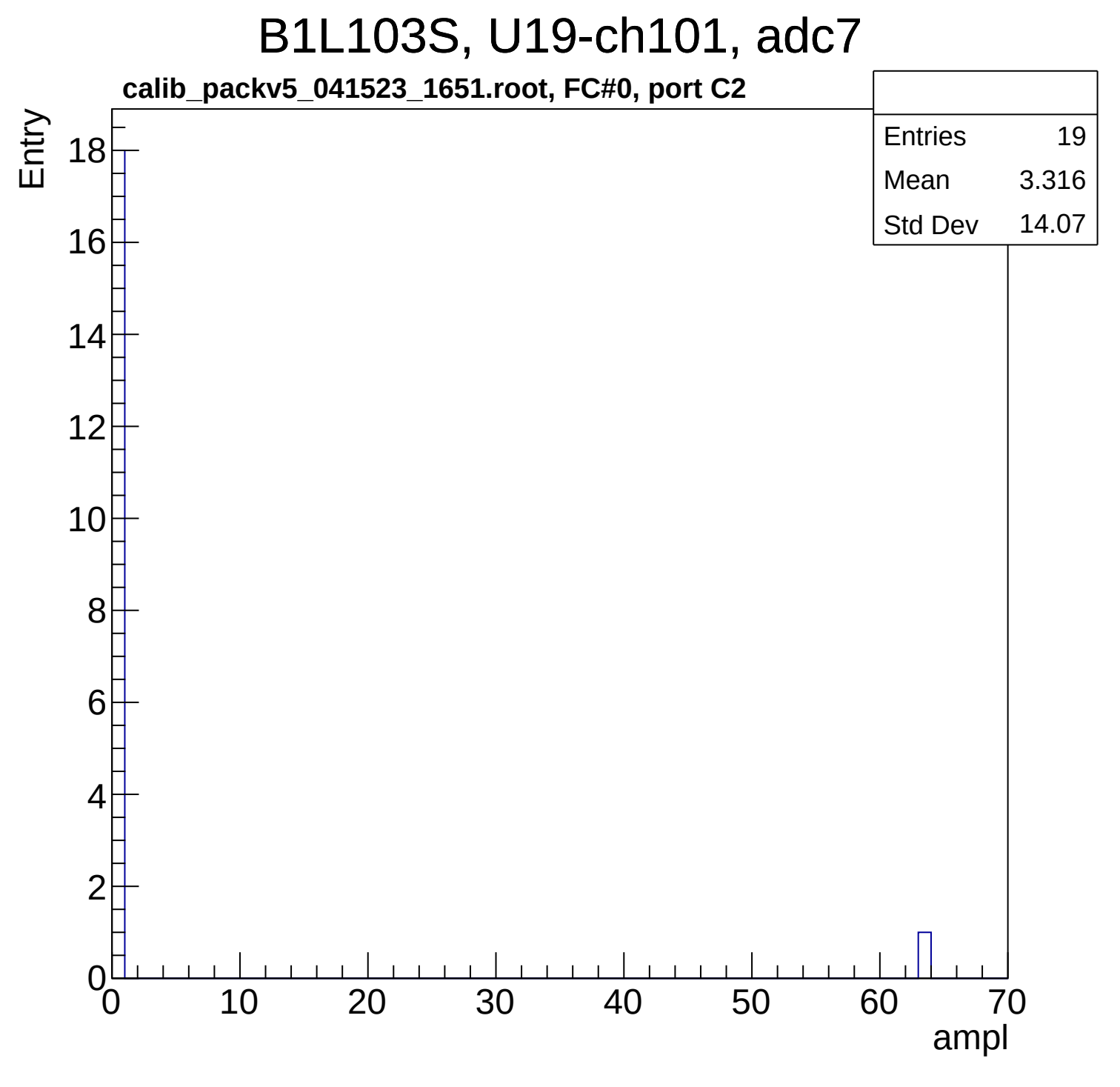
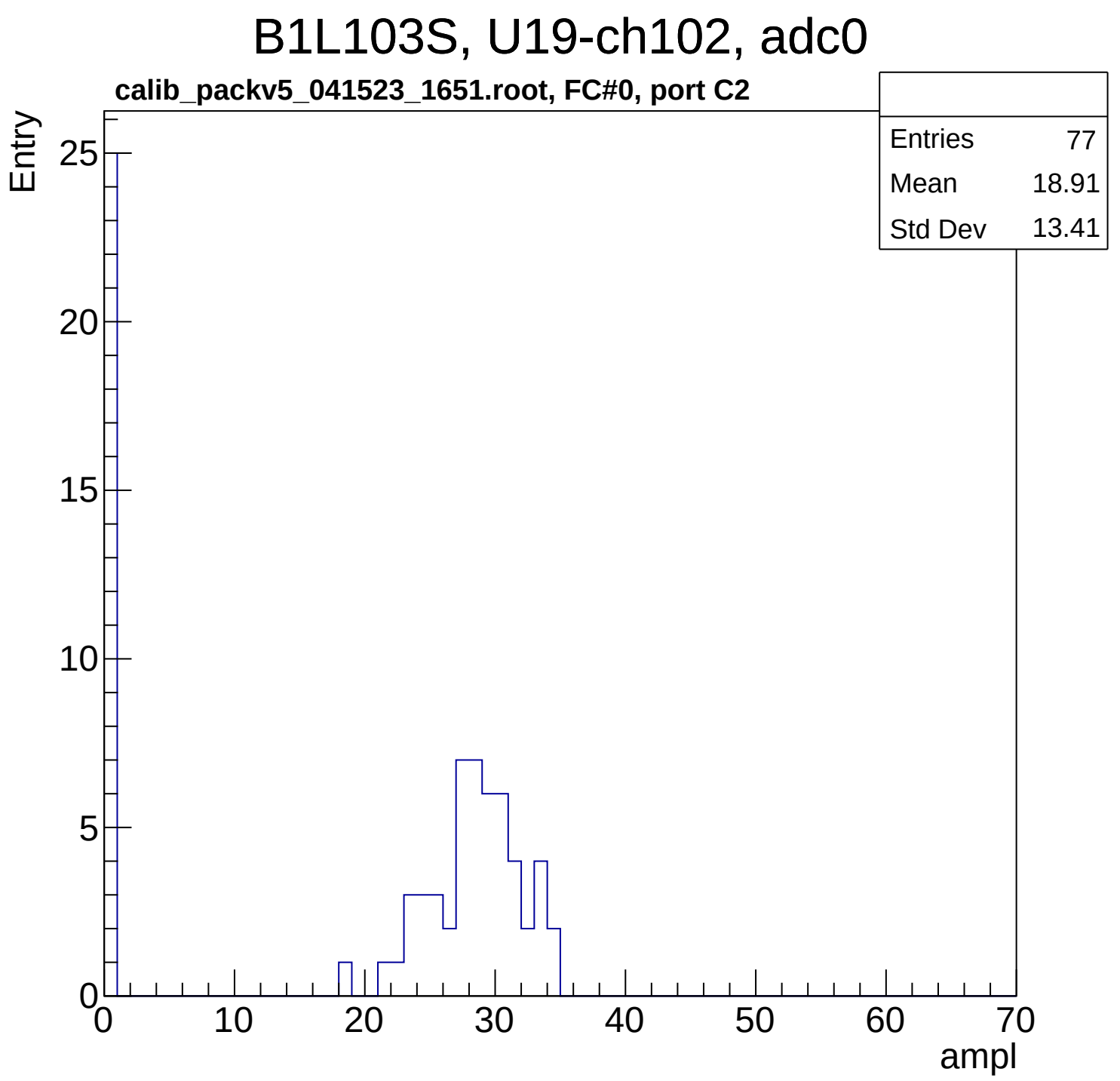
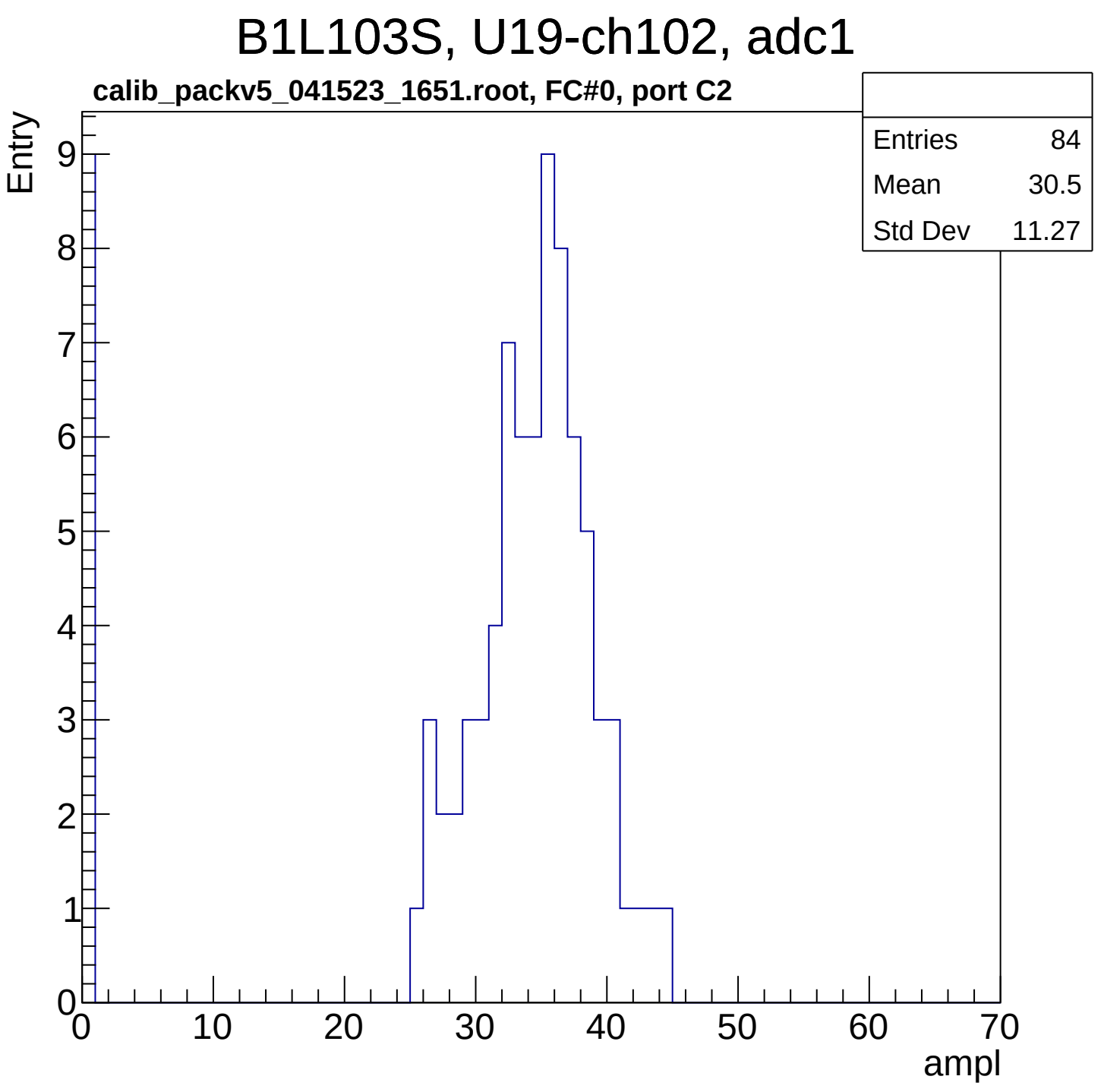

B1L103S, U19-ch101, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 61.55
Std Dev 1.437
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U19-ch101, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.316
Std Dev 14.07
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch102, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 18.91
Std Dev 13.41
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch102, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 30.5
Std Dev 11.27
Entry
ampl
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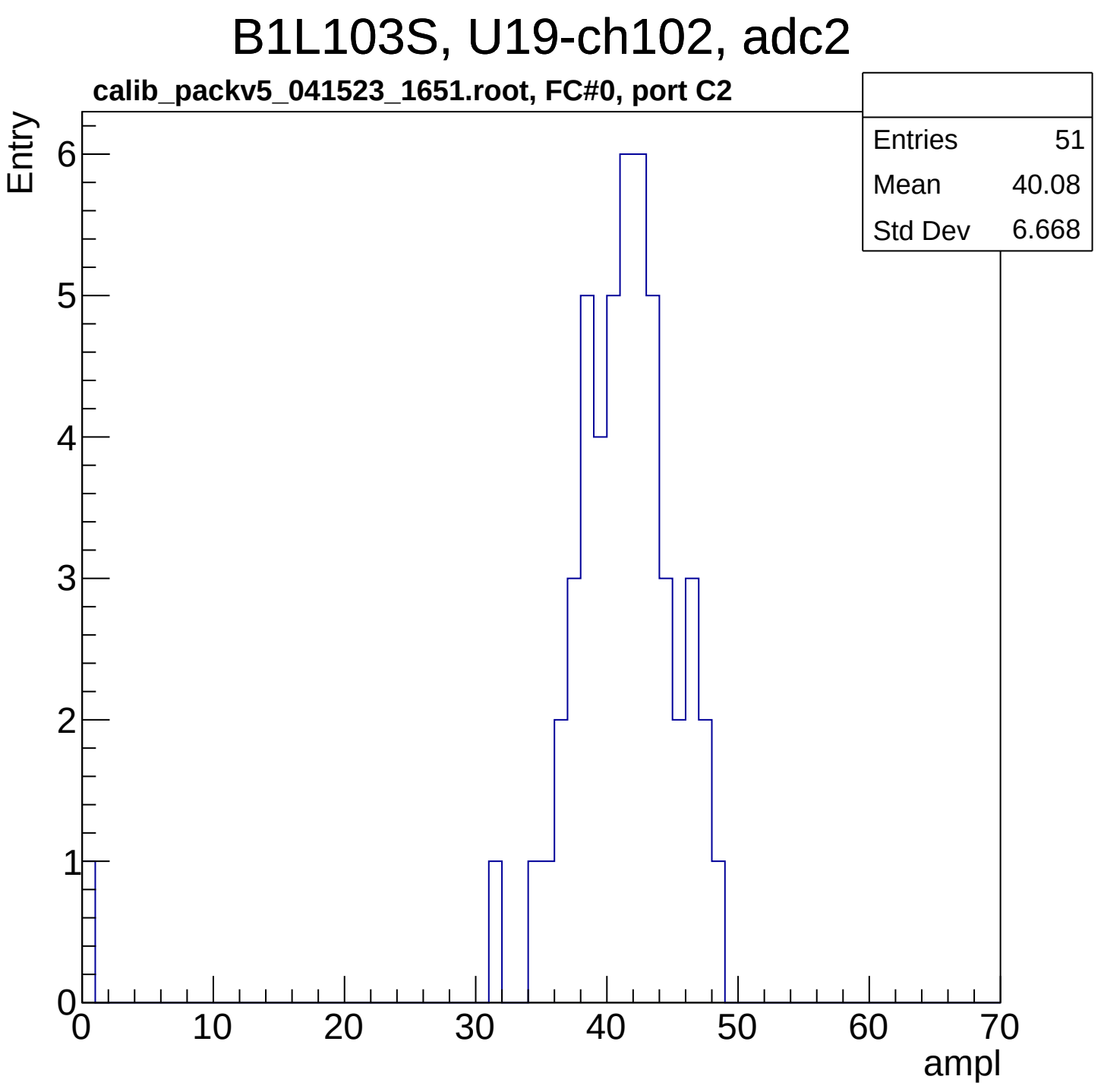
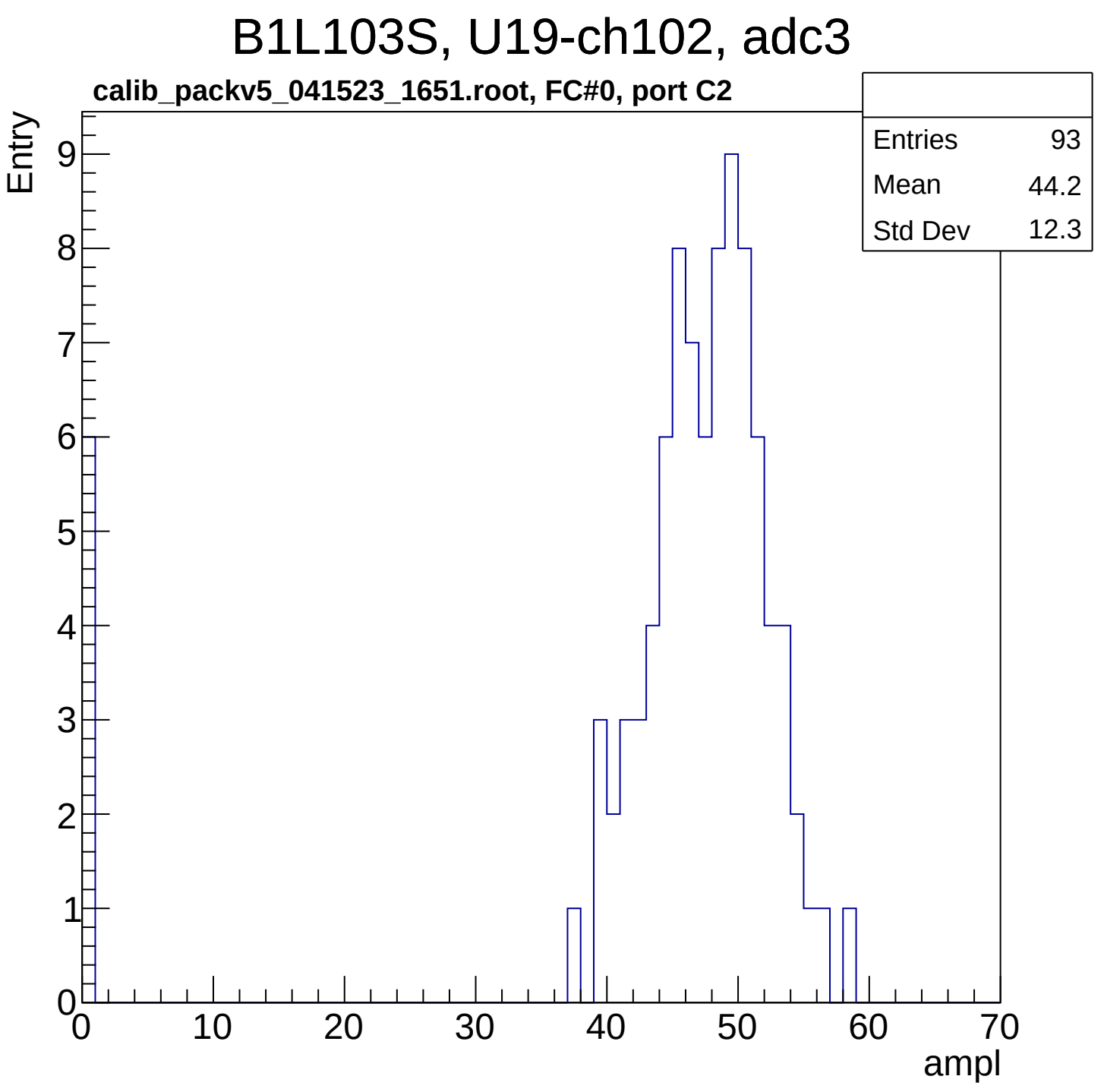
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch102, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 40.08
Std Dev 6.668
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch102, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 44.2
Std Dev 12.3
Entry
ampl
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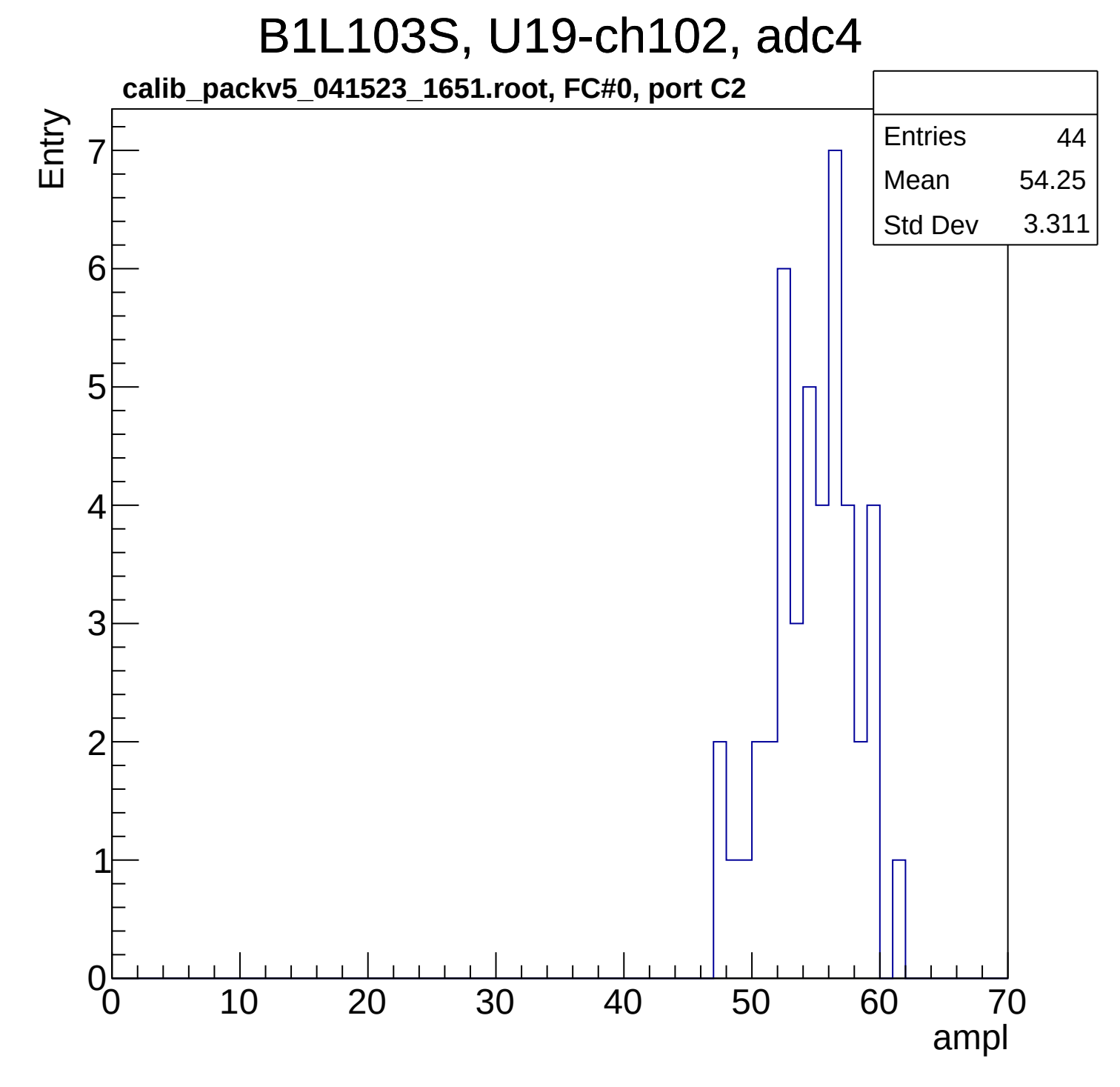
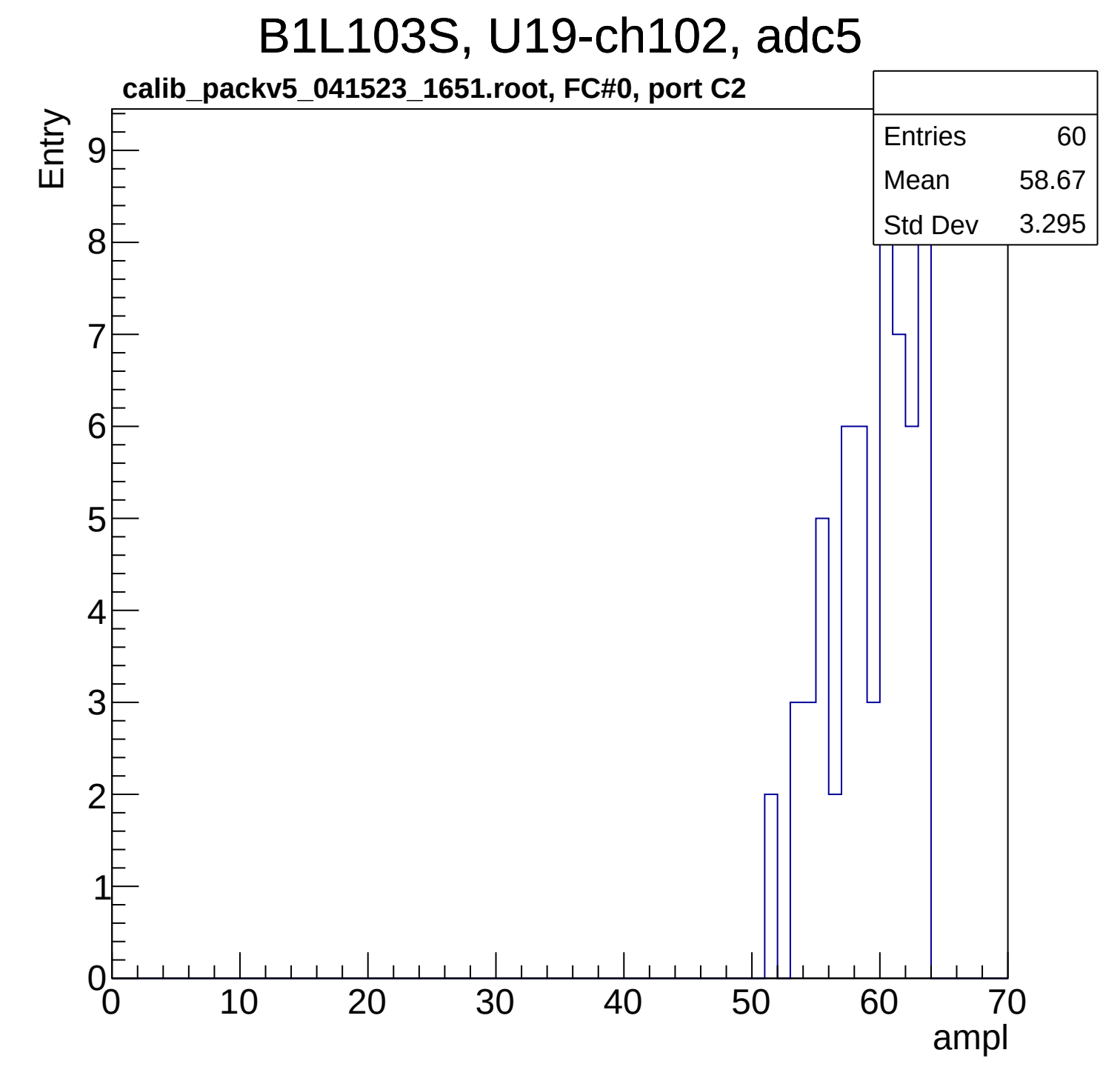
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch102, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 54.25
Std Dev 3.311
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch102, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 58.67
Std Dev 3.295
Entry
ampl
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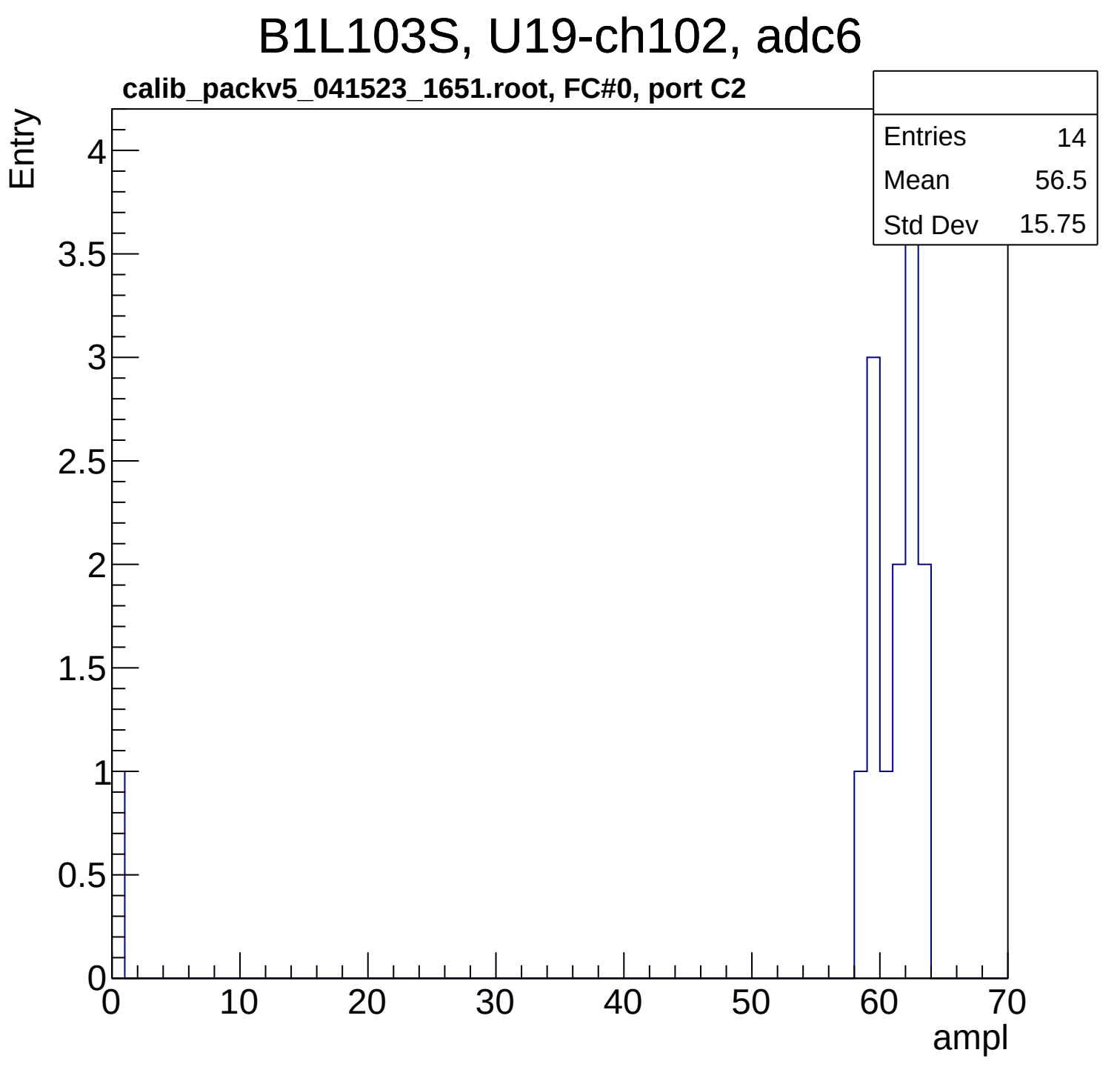
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch102, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 56.5
Std Dev 15.75
Entry
ampl
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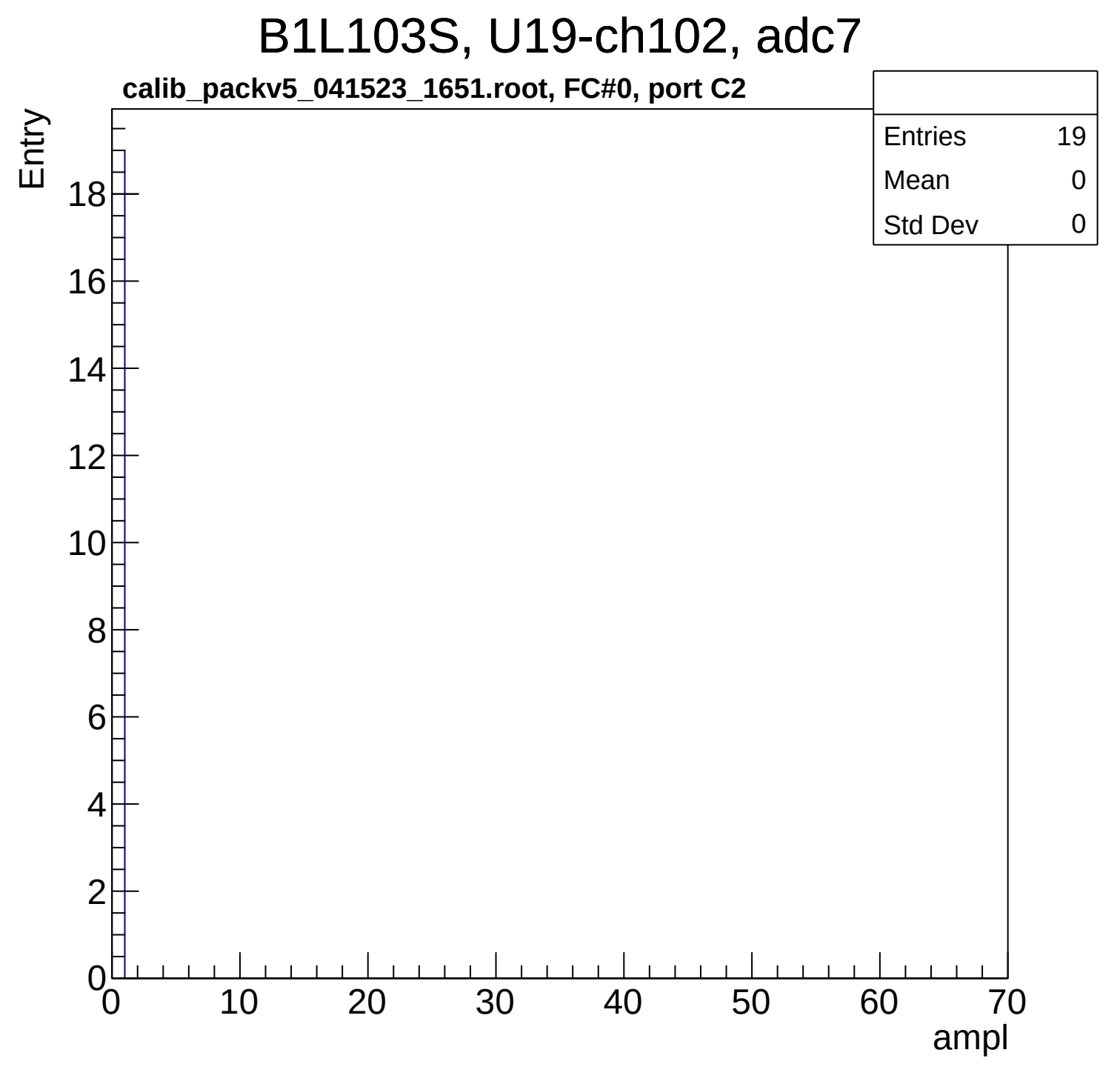
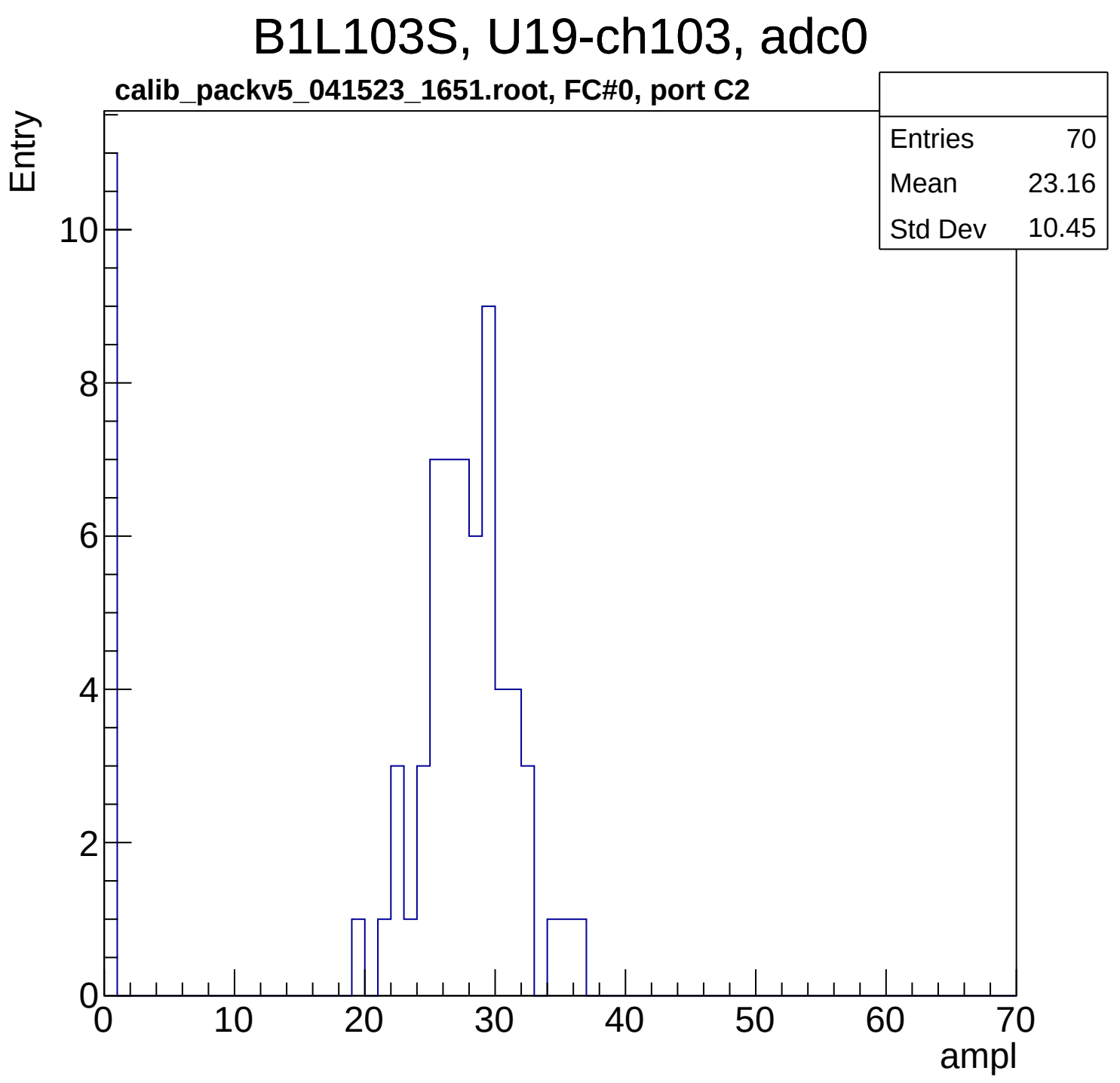
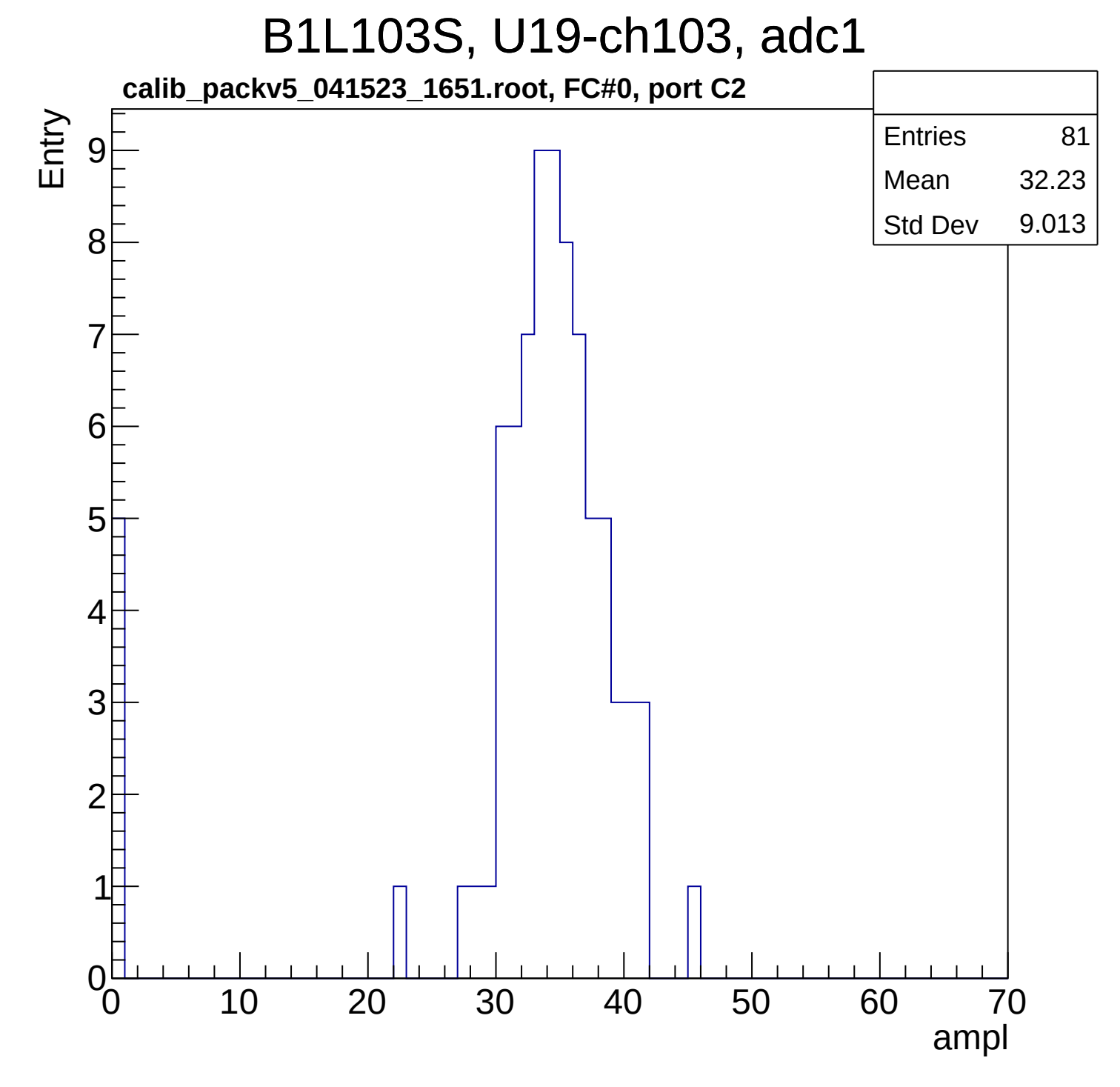
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U19-ch102, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch103, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 23.16
Std Dev 10.45
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch103, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 32.23
Std Dev 9.013
Entry
ampl
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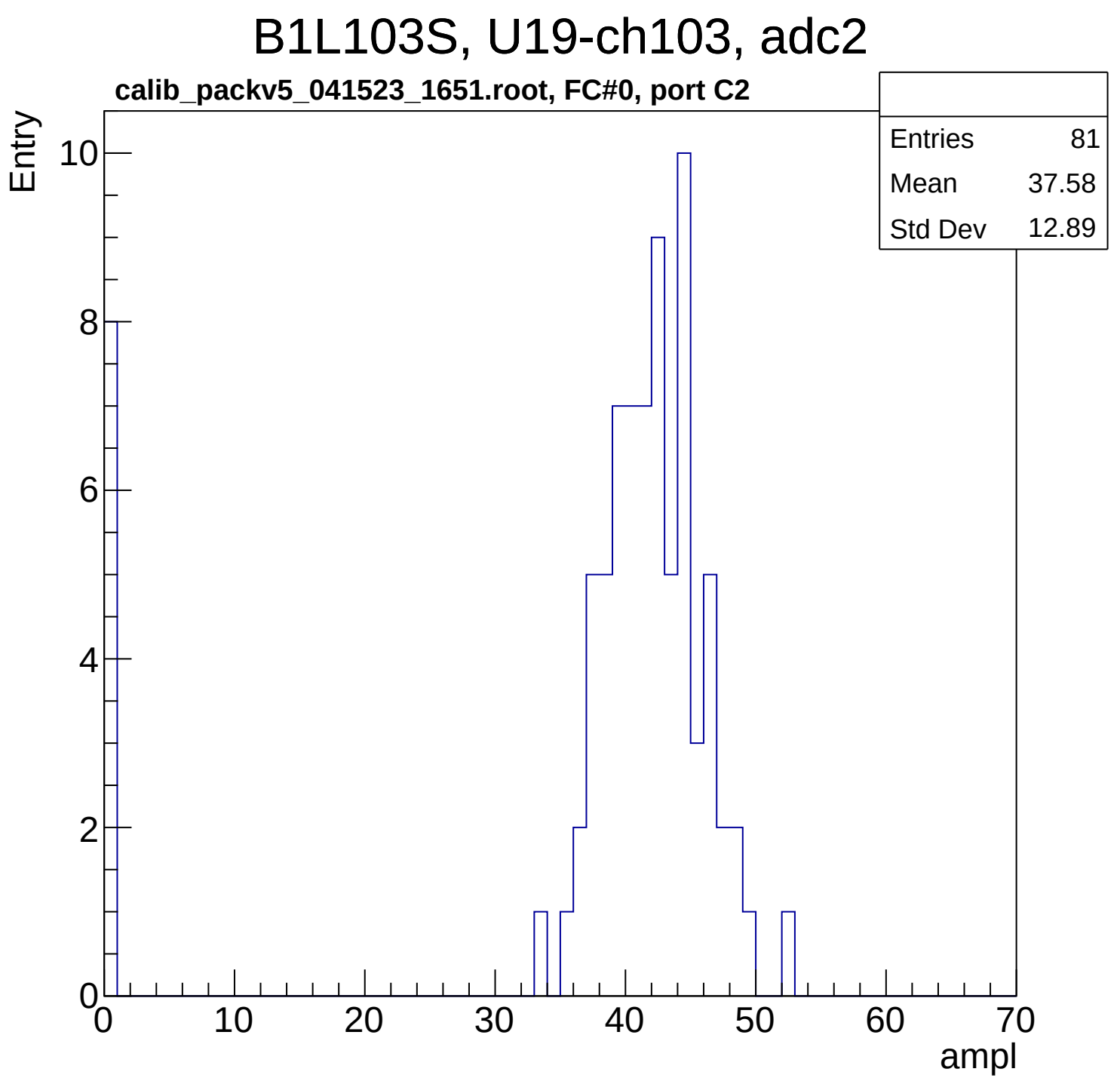
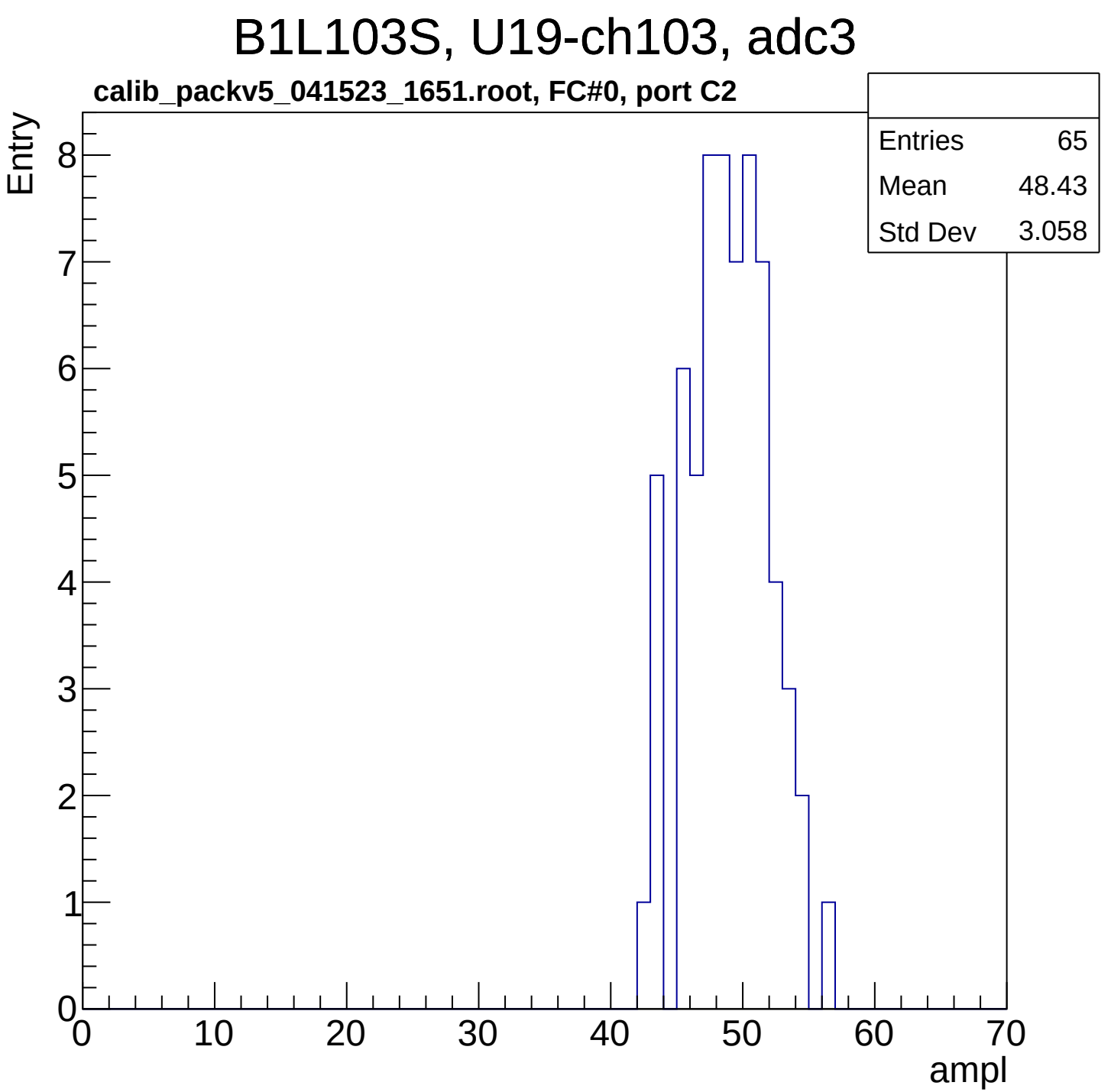
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch103, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 37.58
Std Dev 12.89
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch103, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 48.43
Std Dev 3.058
Entry
ampl
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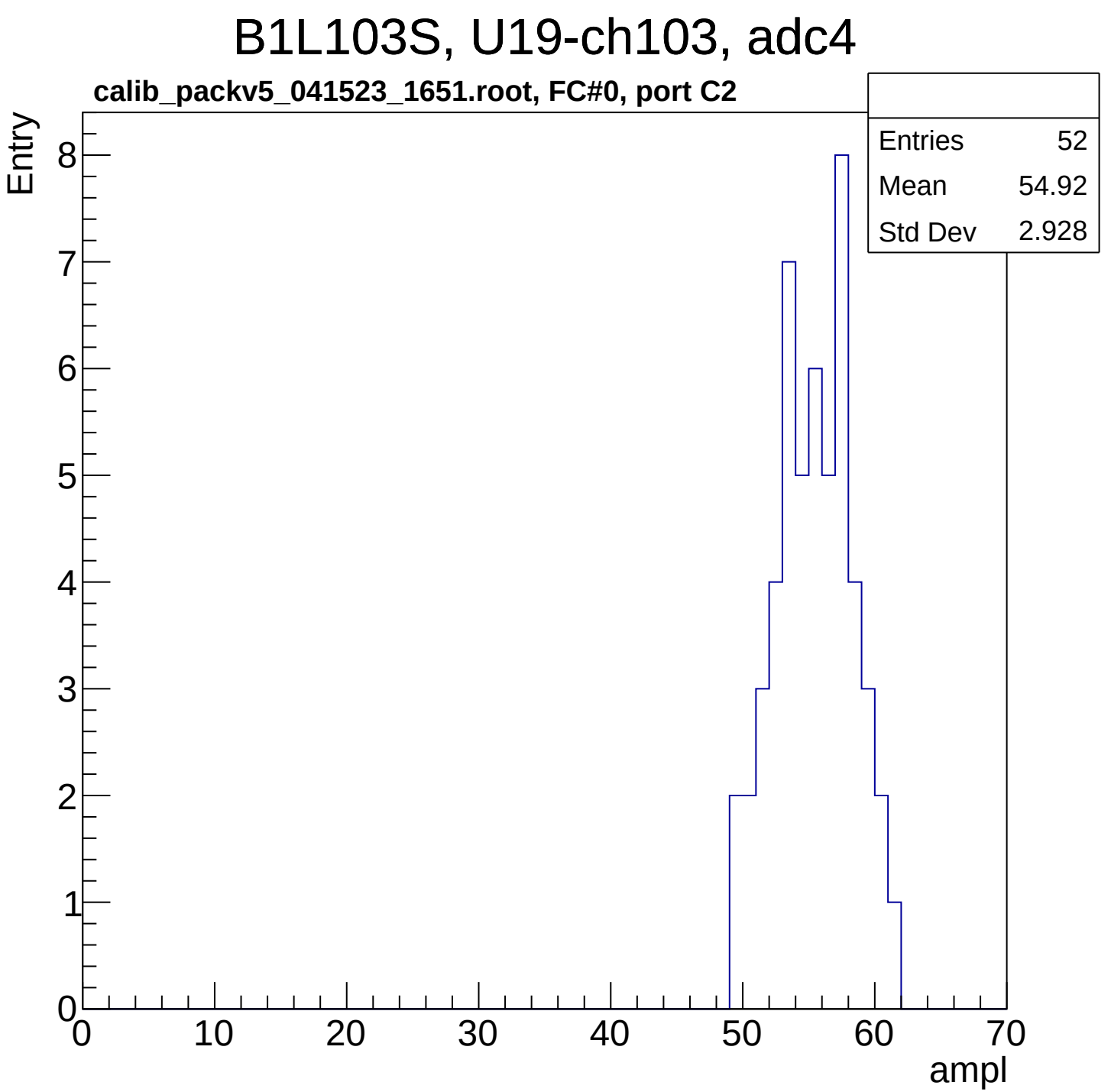
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch103, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 54.92
Std Dev 2.928
Entry
ampl
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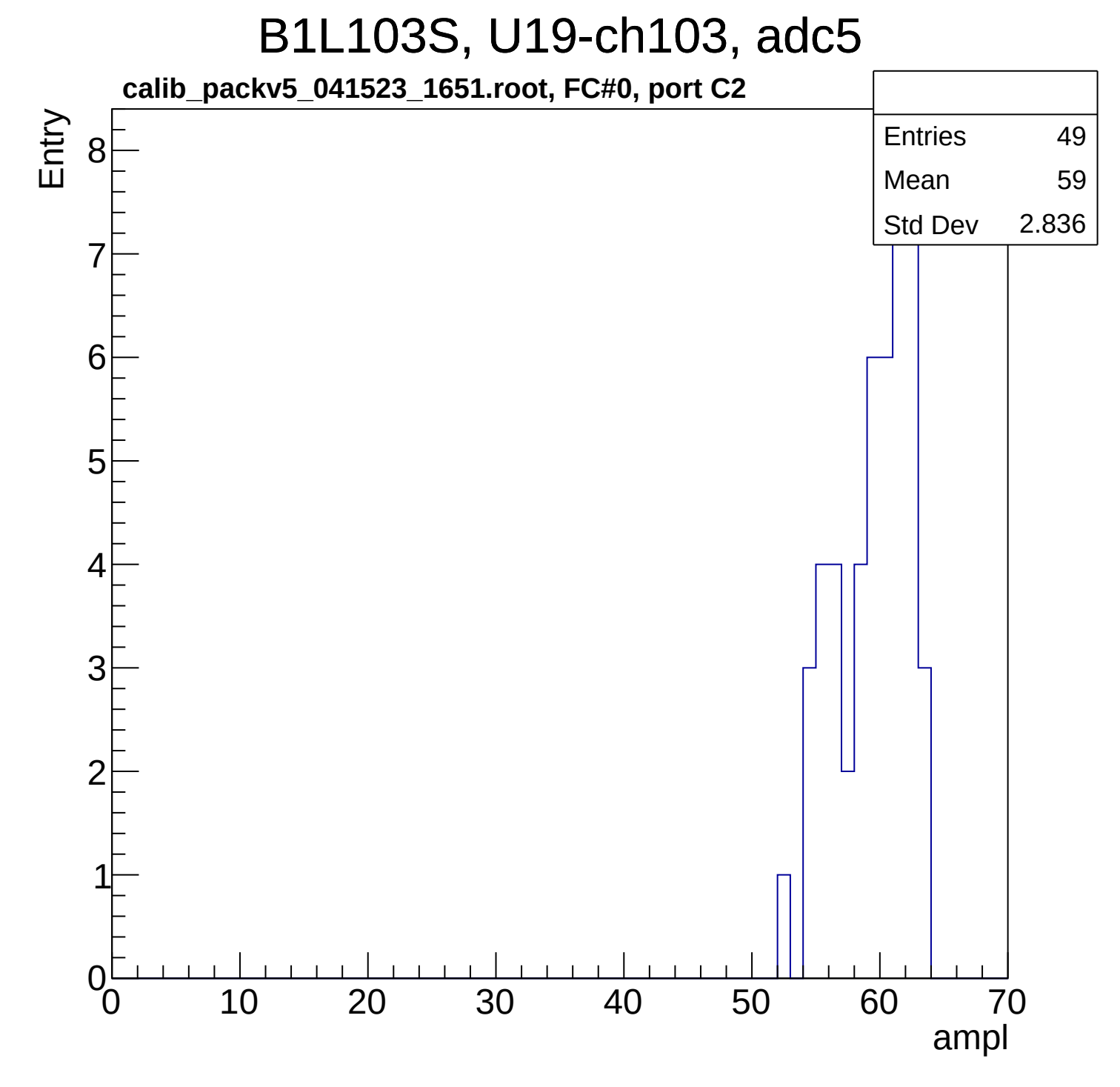
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch103, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 59
Std Dev 2.836
Entry
ampl
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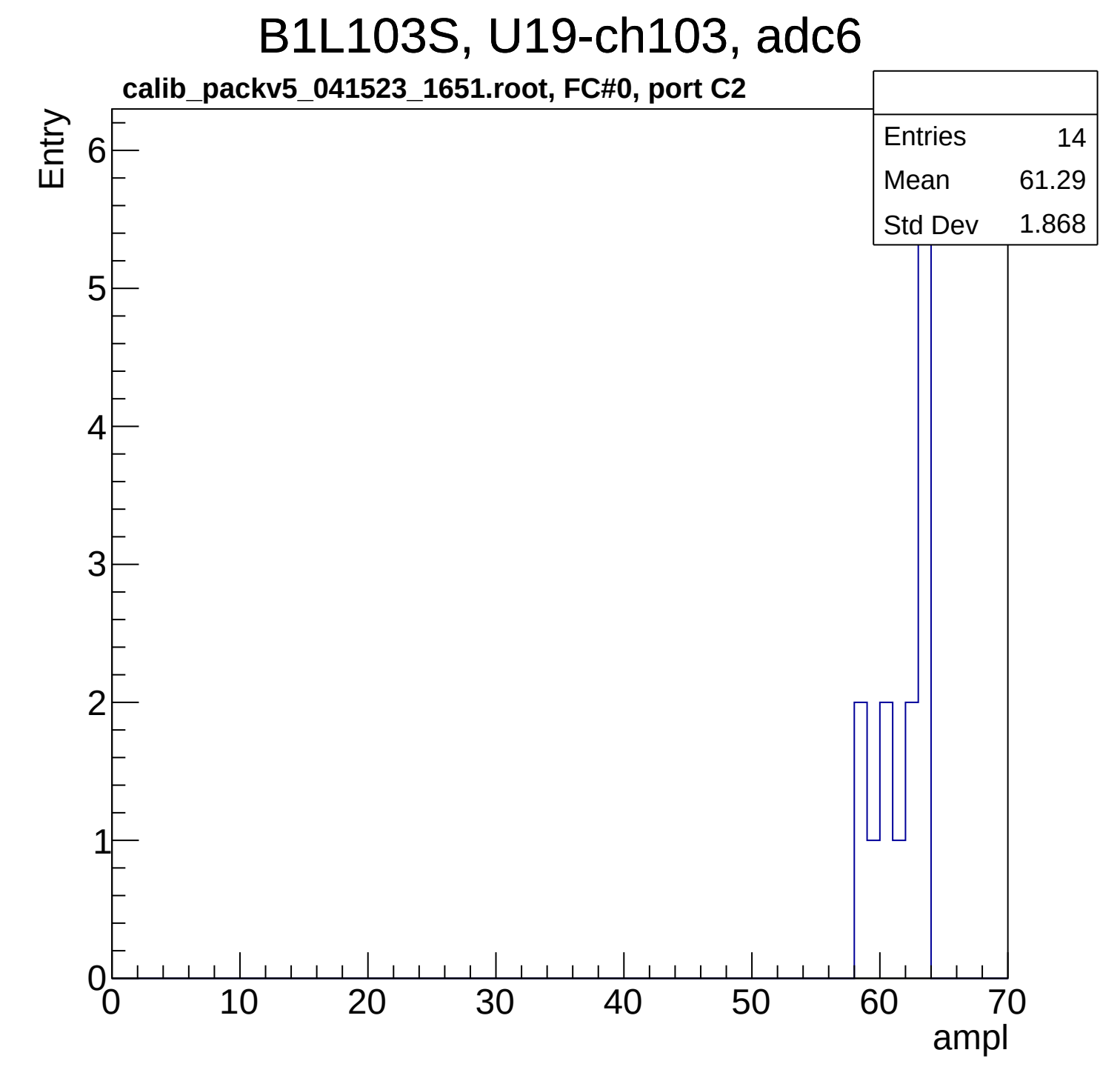
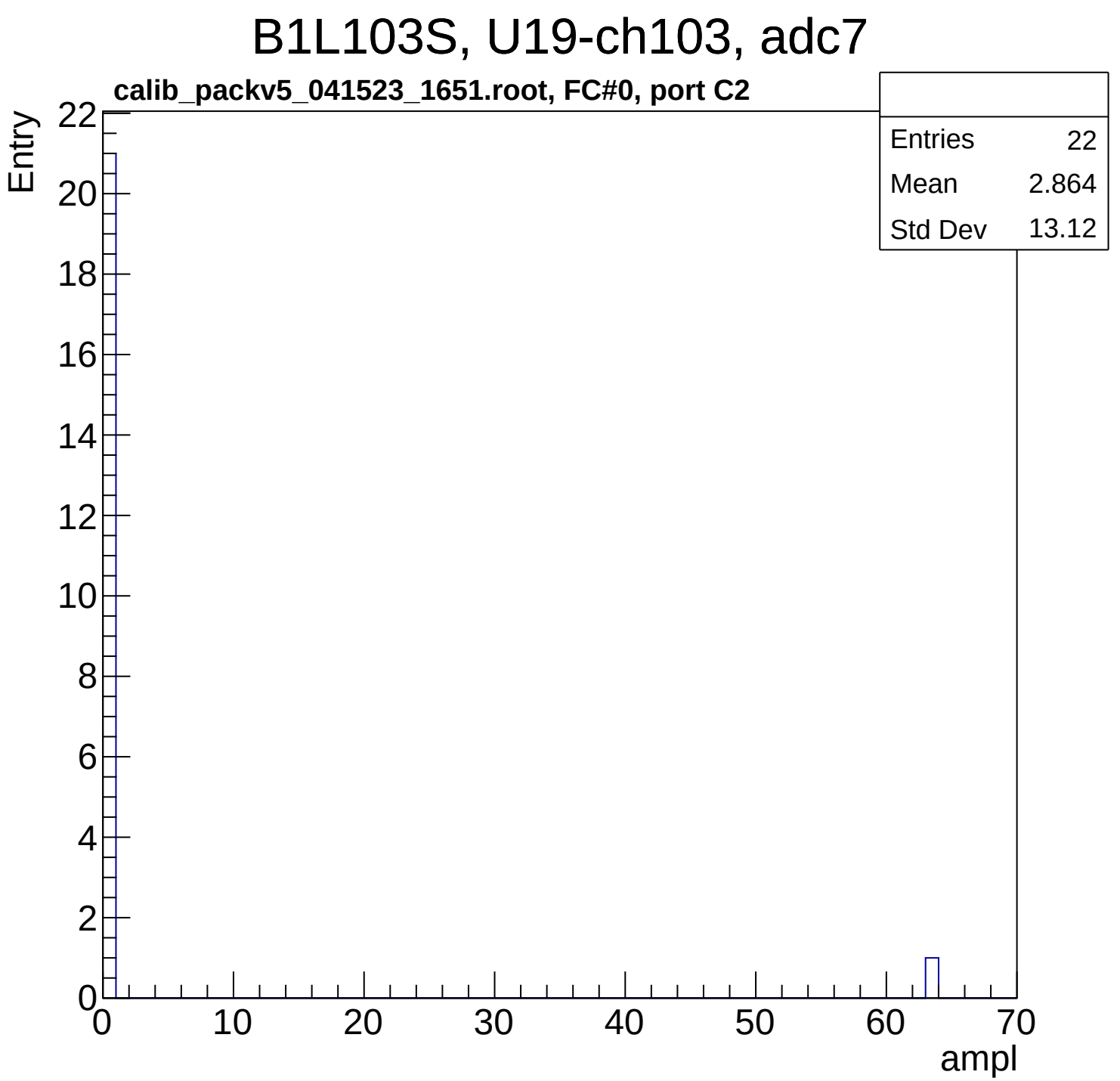
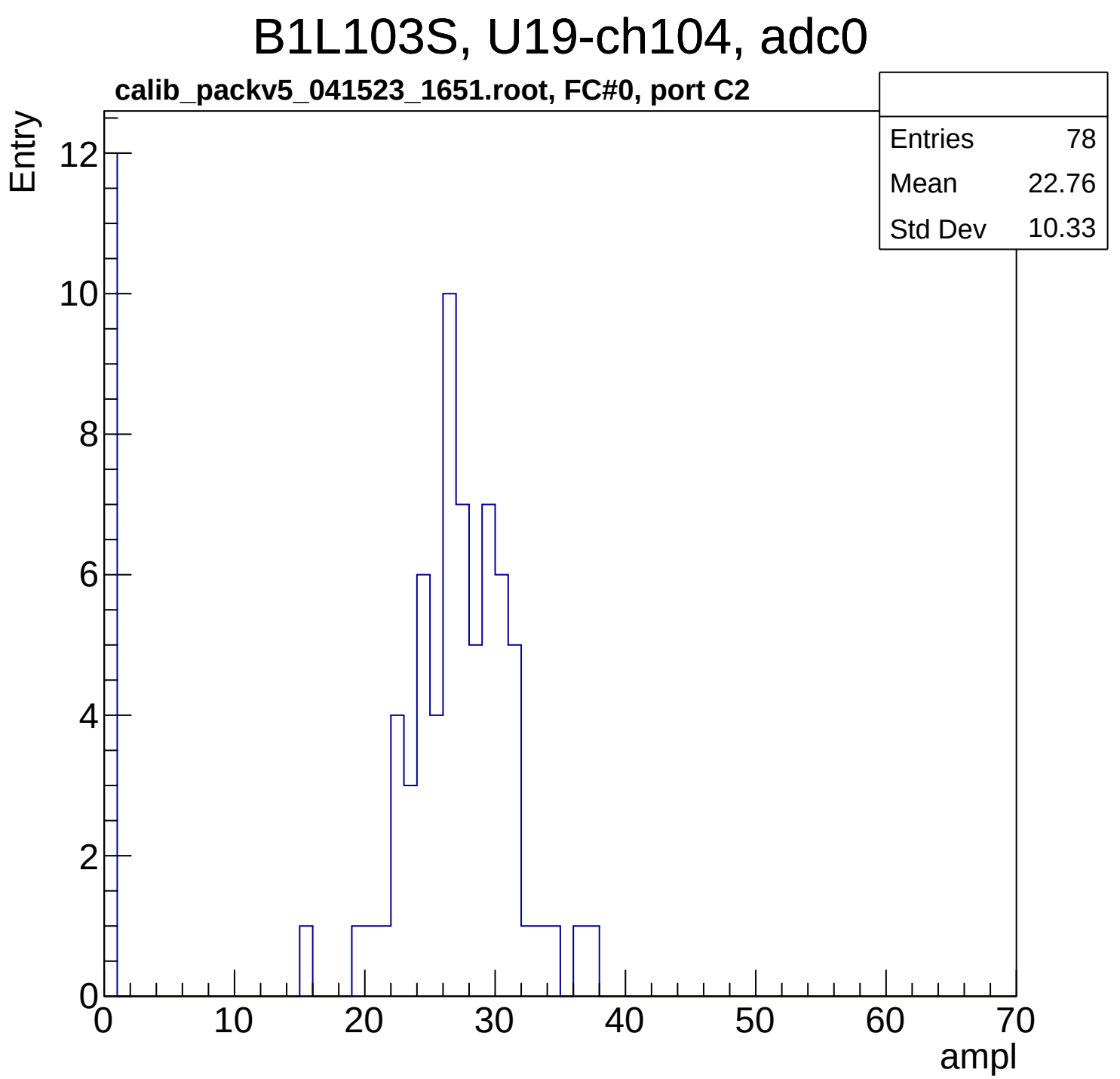
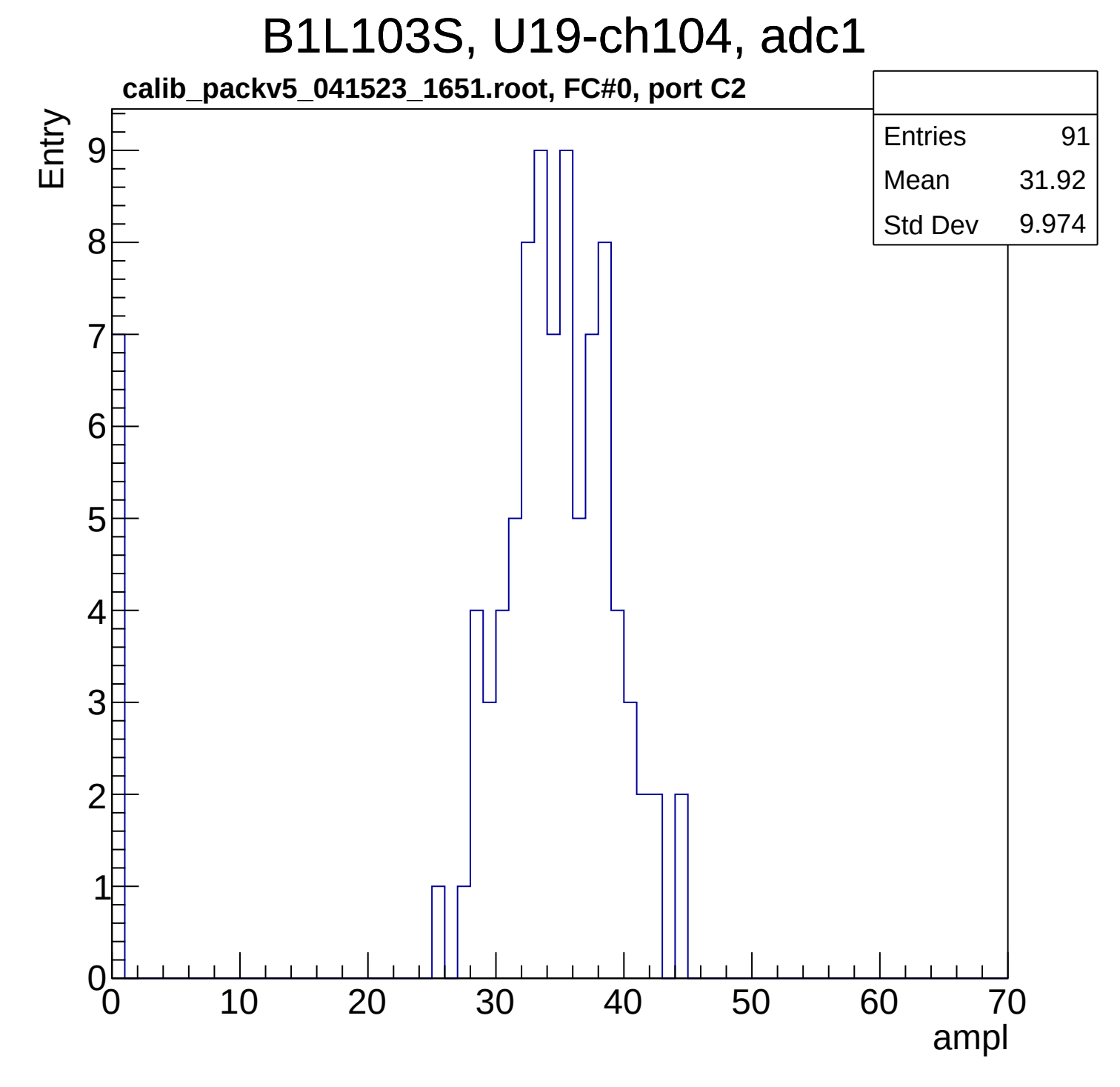
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch103, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 61.29
Std Dev 1.868
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U19-ch103, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 2.864
Std Dev 13.12
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70


B1L103S, U19-ch104, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 22.76
Std Dev 10.33
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch104, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 31.92
Std Dev 9.974
Entry
ampl
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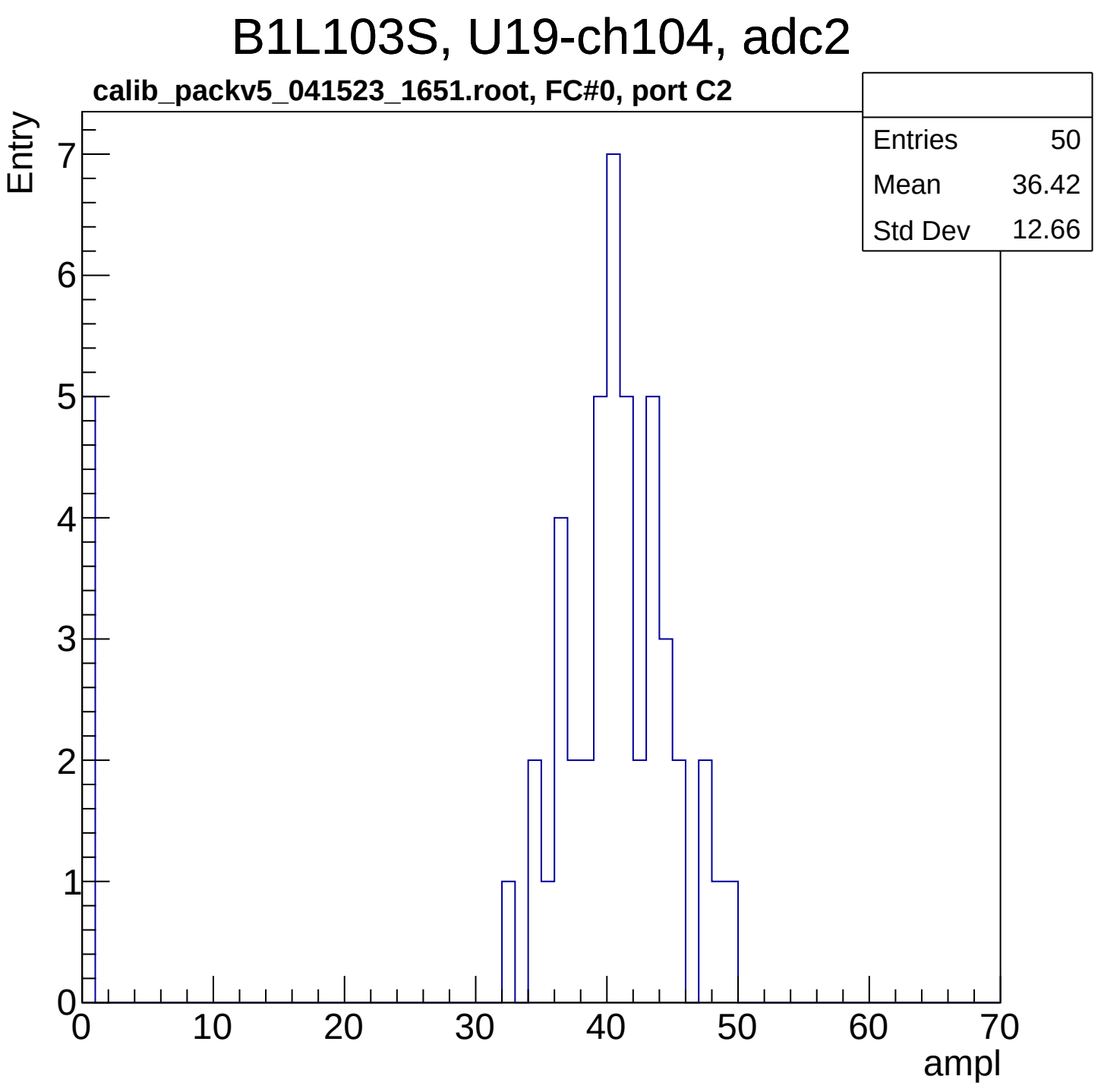
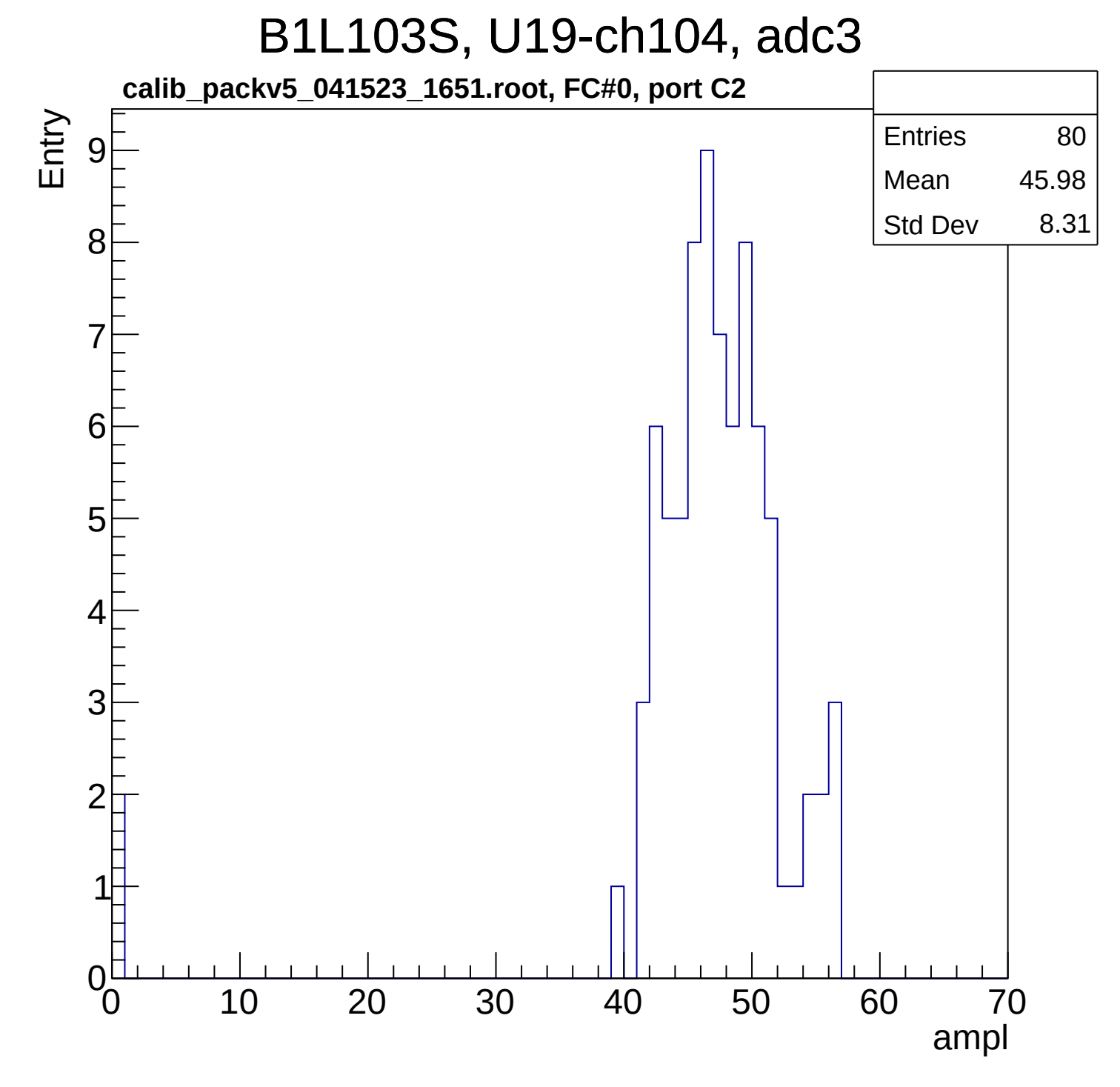
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch104, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 36.42
Std Dev 12.66
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch104, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 45.98
Std Dev 8.31
Entry
ampl
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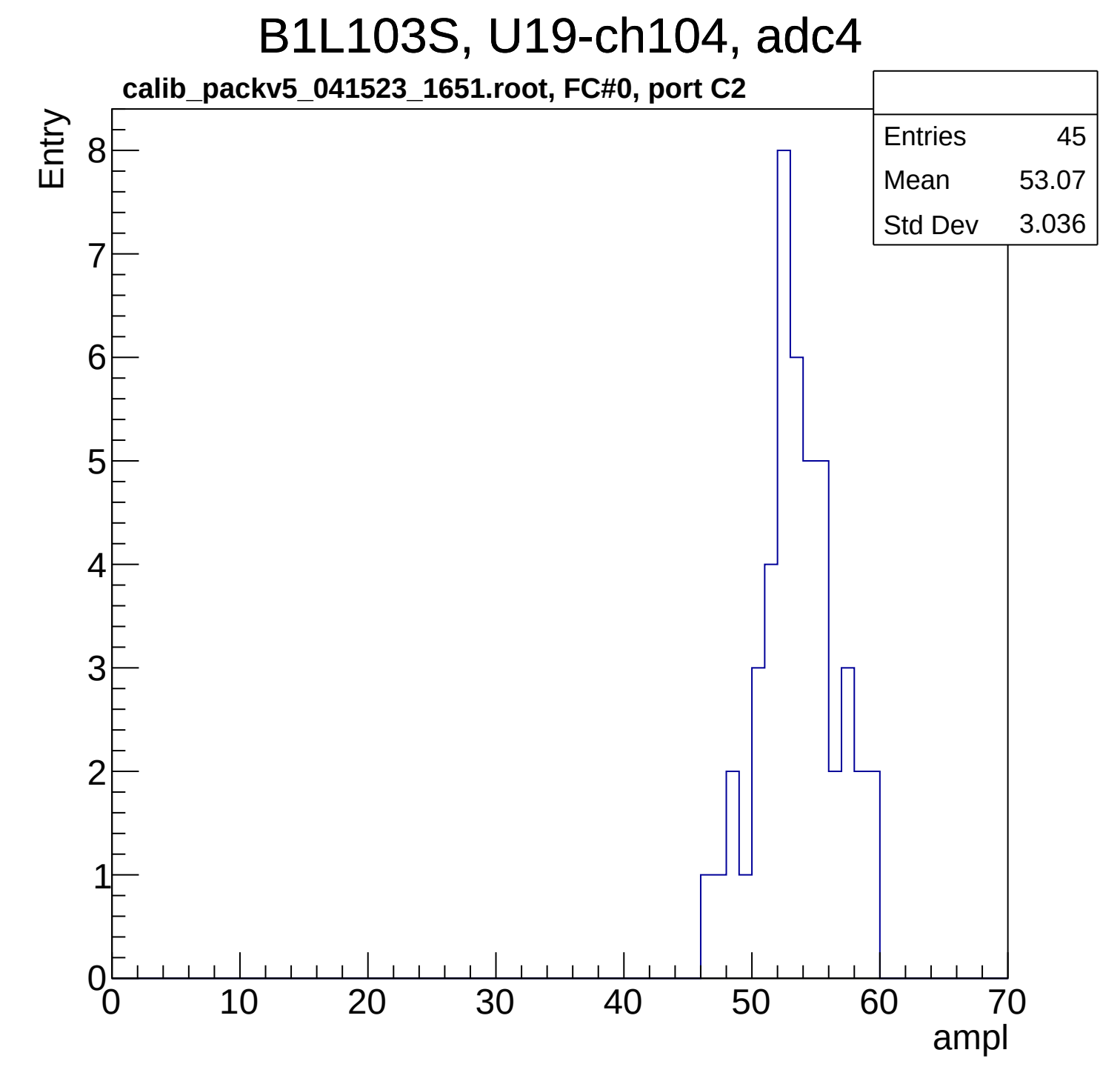
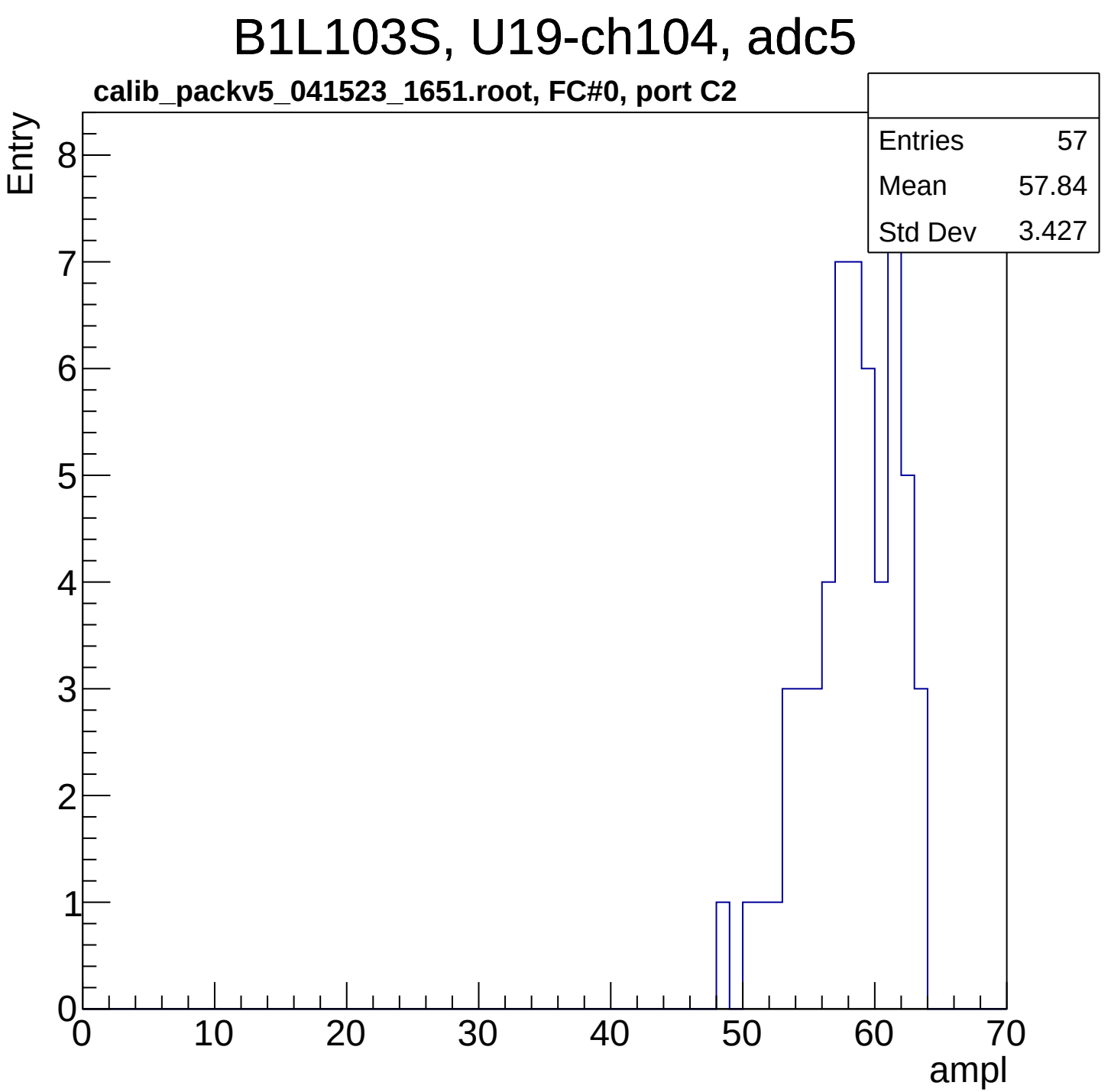
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch104, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 53.07
Std Dev 3.036
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch104, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 57.84
Std Dev 3.427
Entry
ampl
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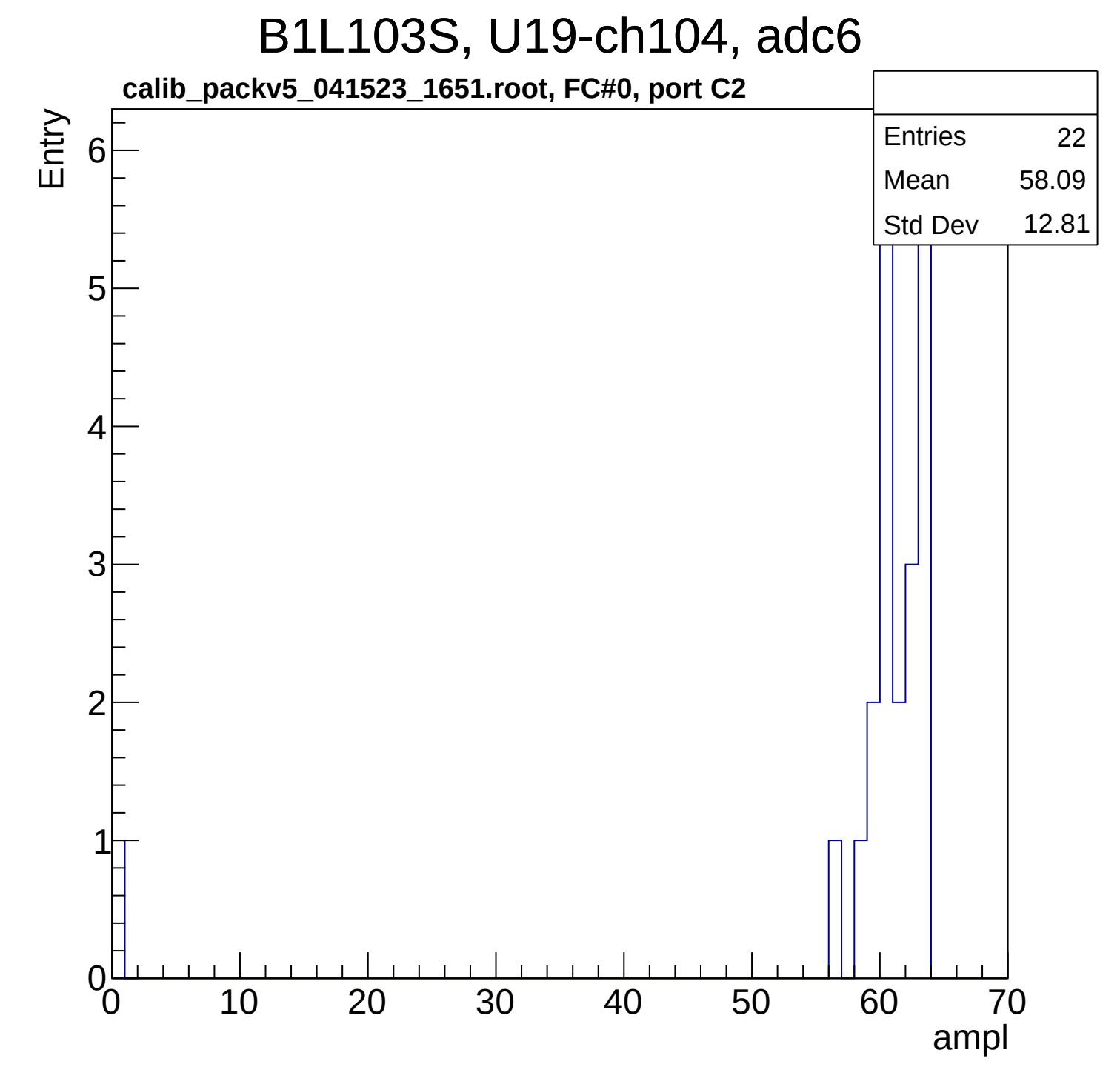
B1L103S, U19-ch104, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 58.09
Std Dev 12.81
Entry
ampl
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2
3
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0
10
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40
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60
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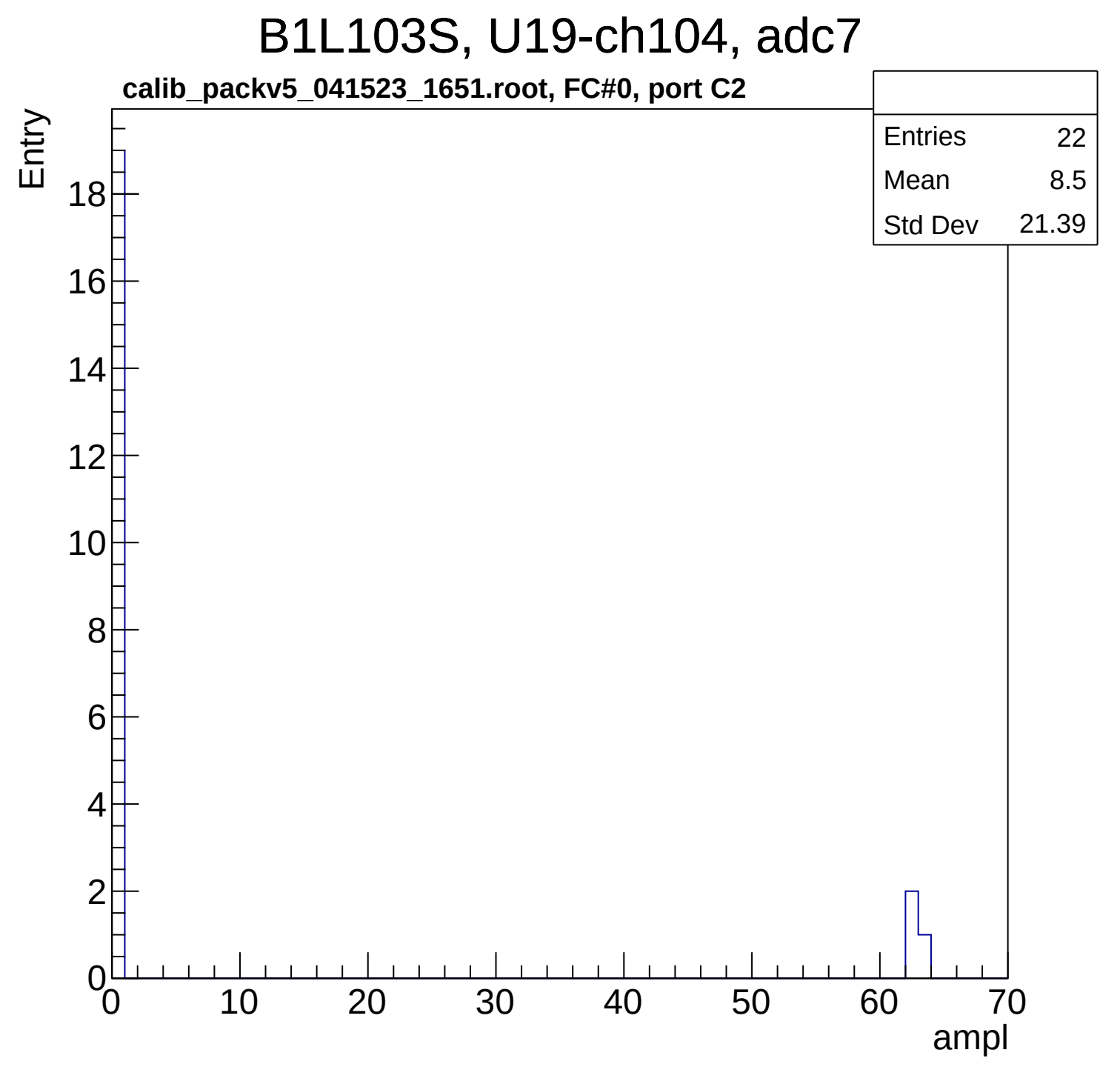
B1L103S, U19-ch104, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.5
Std Dev 21.39
Entry
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10
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14
16
18
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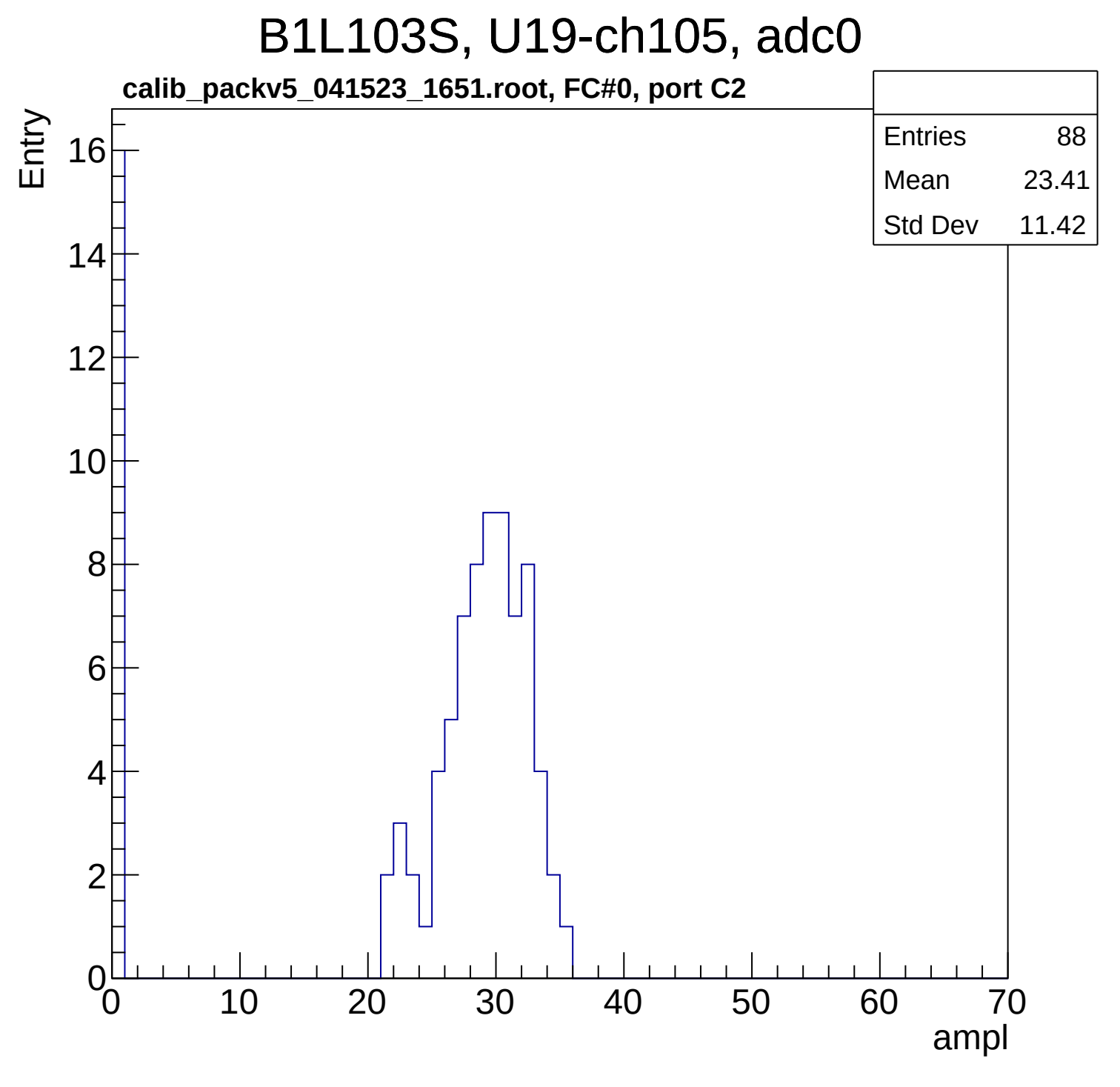
70
ampl


B1L103S, U19-ch105, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 23.41
Std Dev 11.42
Entry
ampl
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10
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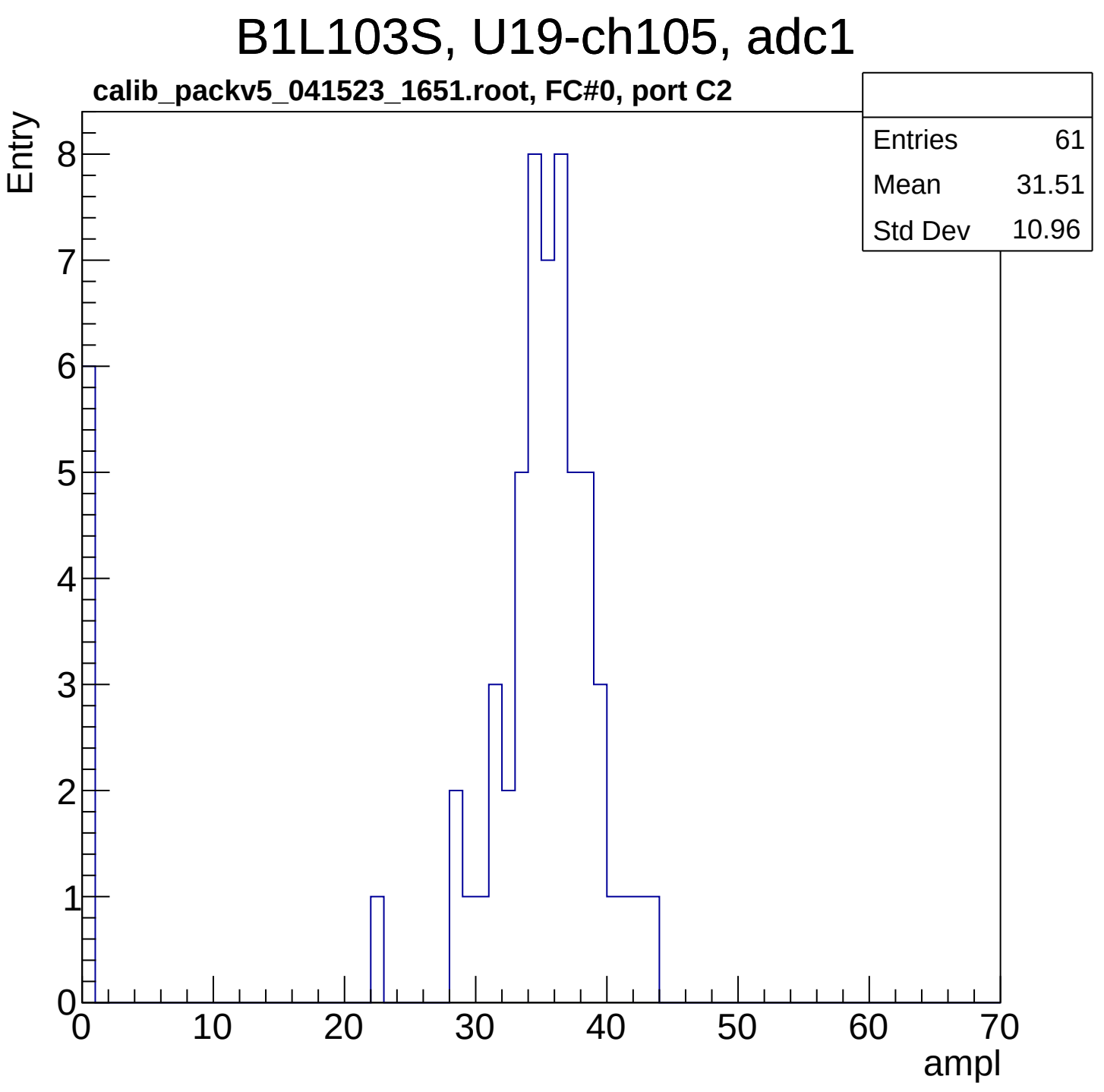
B1L103S, U19-ch105, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 31.51
Std Dev 10.96
Entry
ampl
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1
2
3
4
5
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7
8
0
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40
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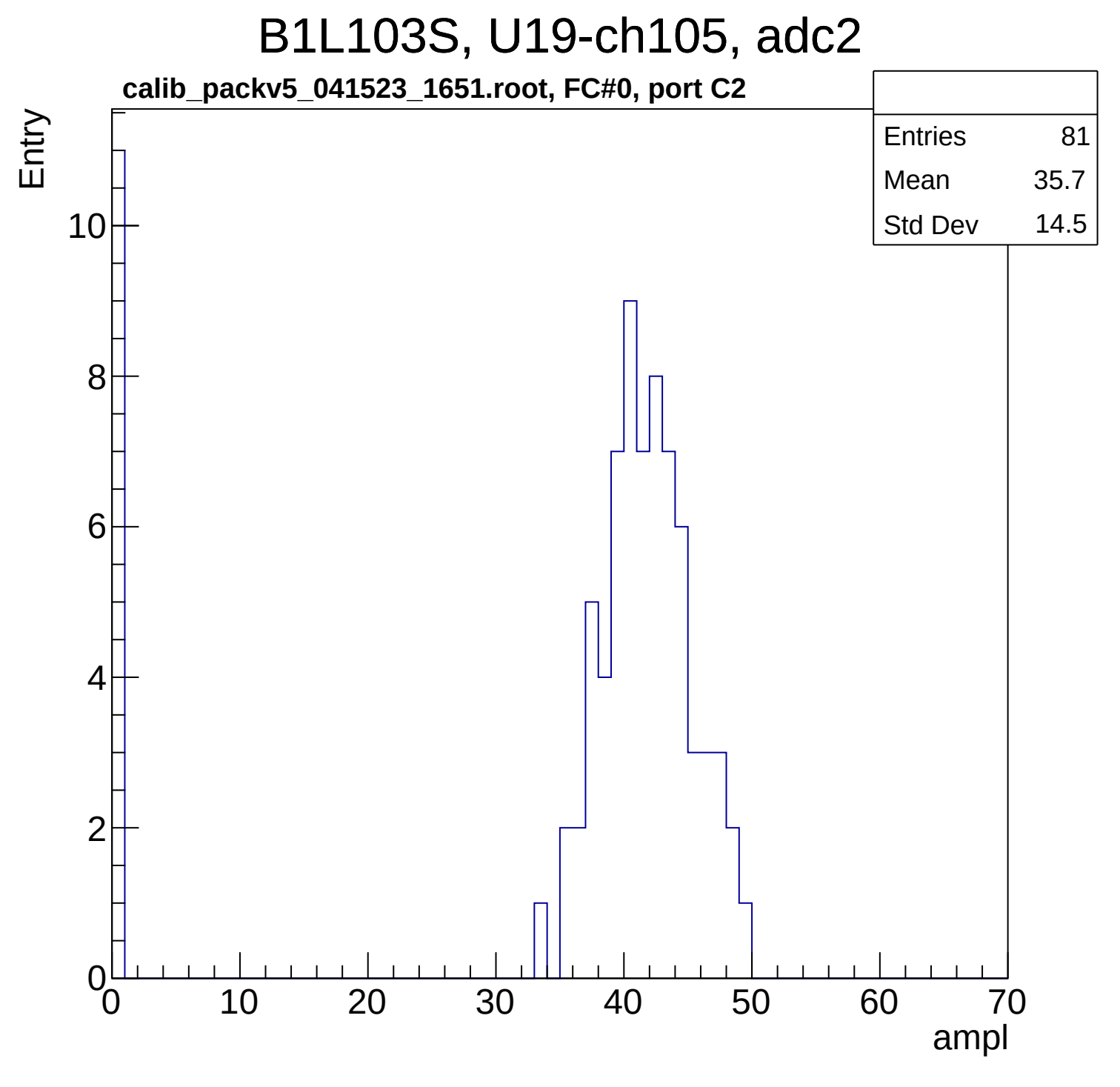
B1L103S, U19-ch105, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 35.7
Std Dev 14.5
Entry
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2
4
6
8
10
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10
20
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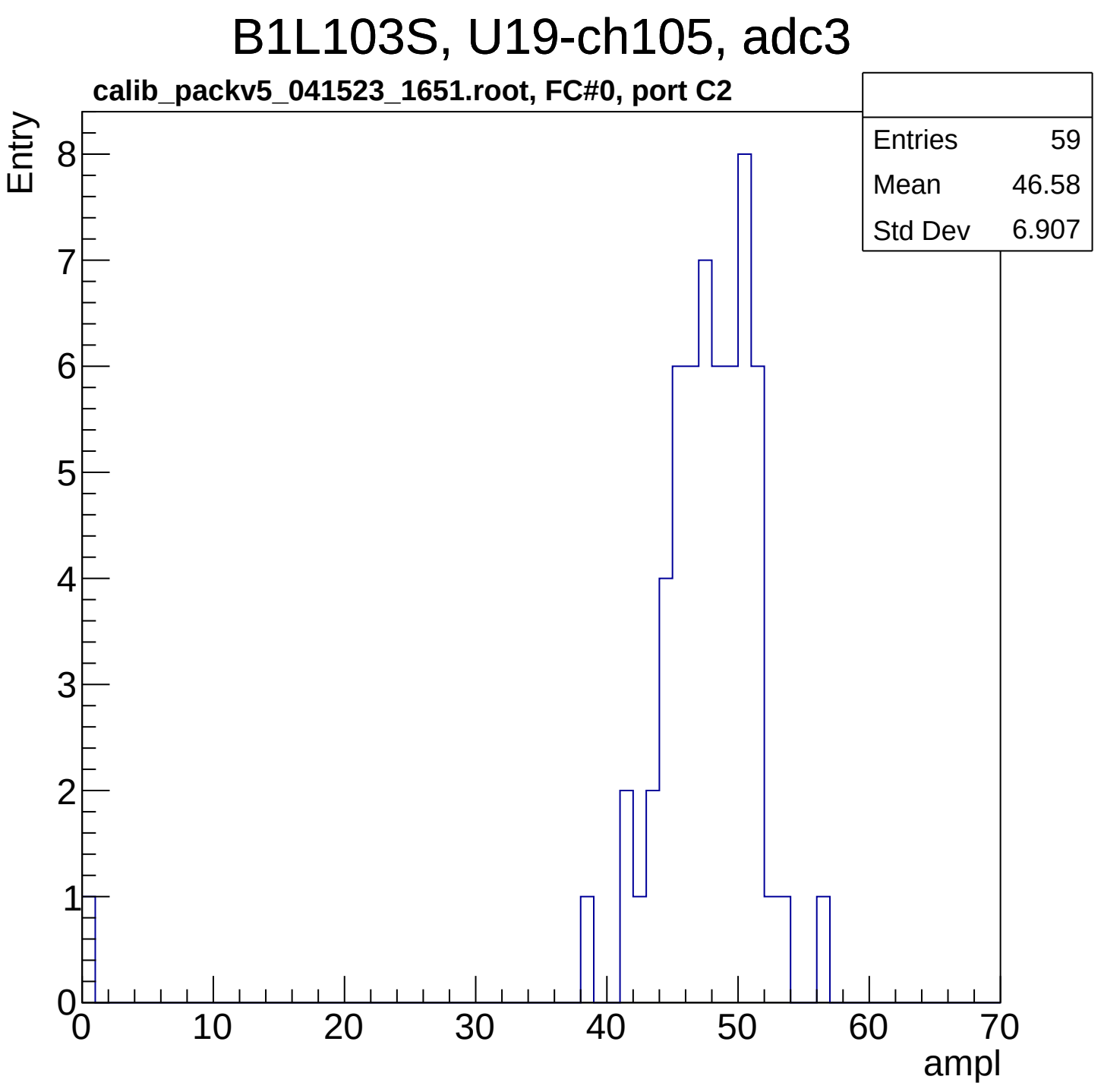
40
50
60
70
ampl


B1L103S, U19-ch105, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 46.58
Std Dev 6.907
Entry
ampl
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2
3
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5
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7
8
0
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40
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60
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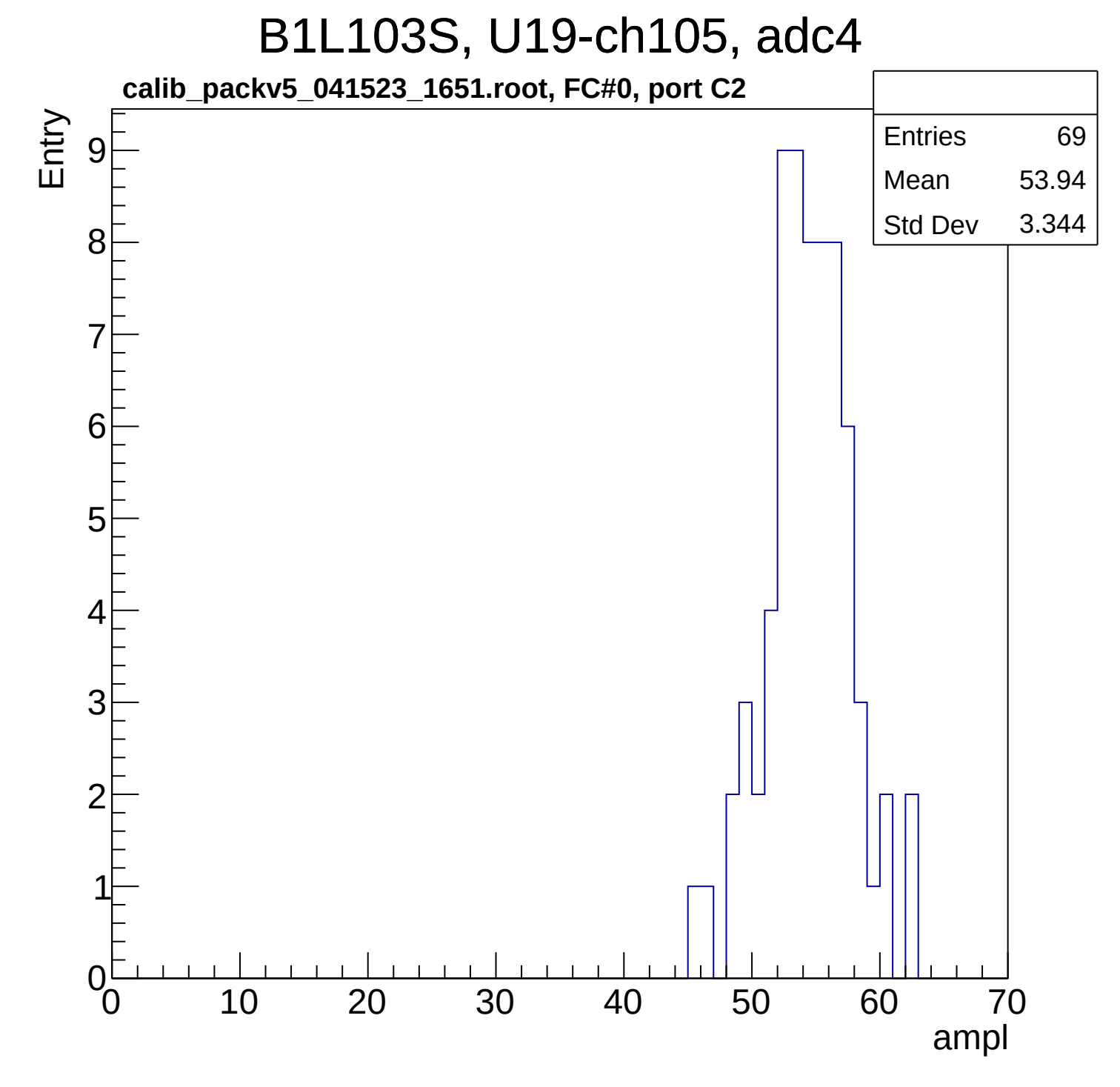
B1L103S, U19-ch105, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 53.94
Std Dev 3.344
Entry
ampl
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2
3
4
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7
8
9
0
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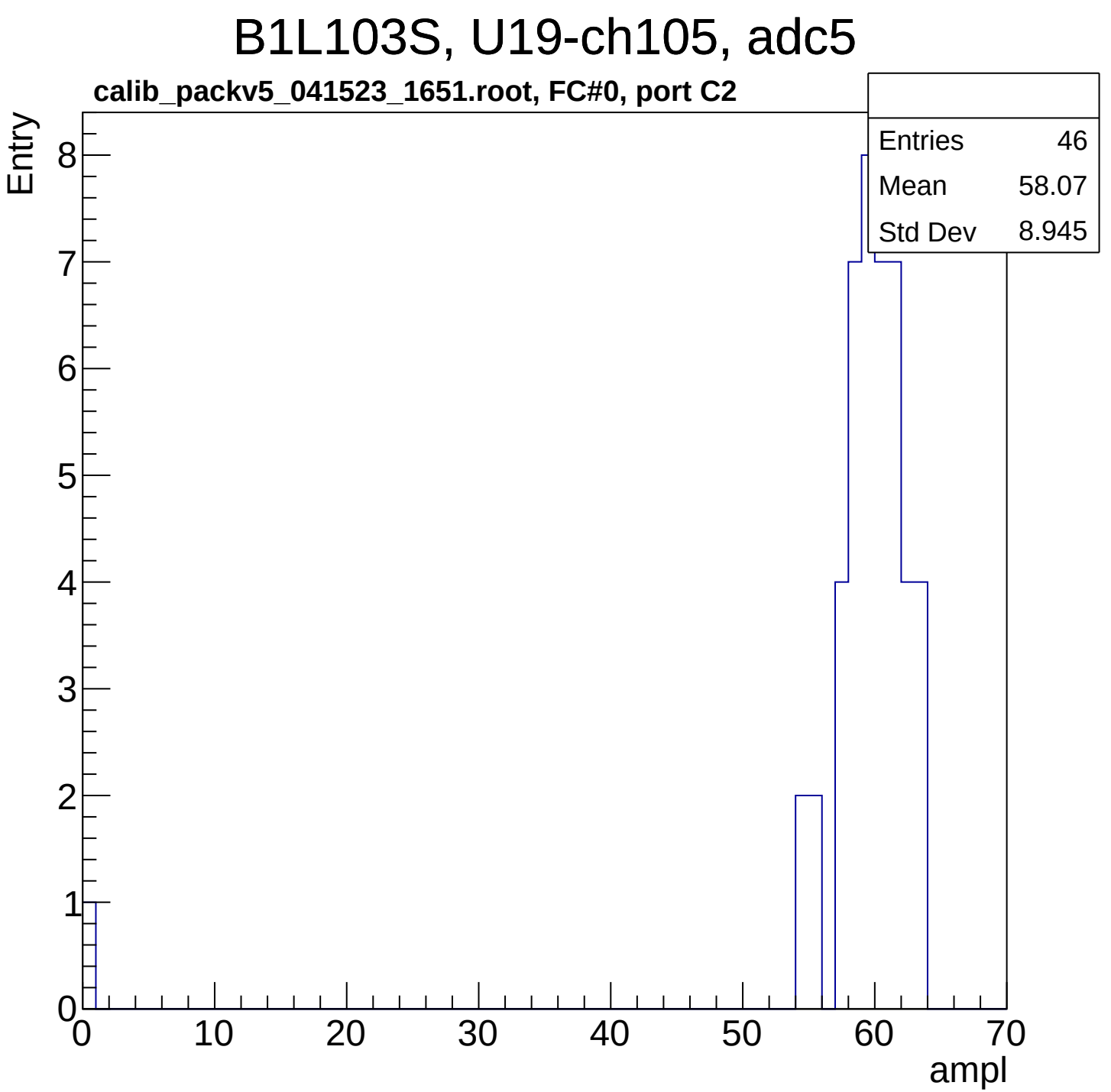
B1L103S, U19-ch105, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 58.07
Std Dev 8.945
Entry
ampl
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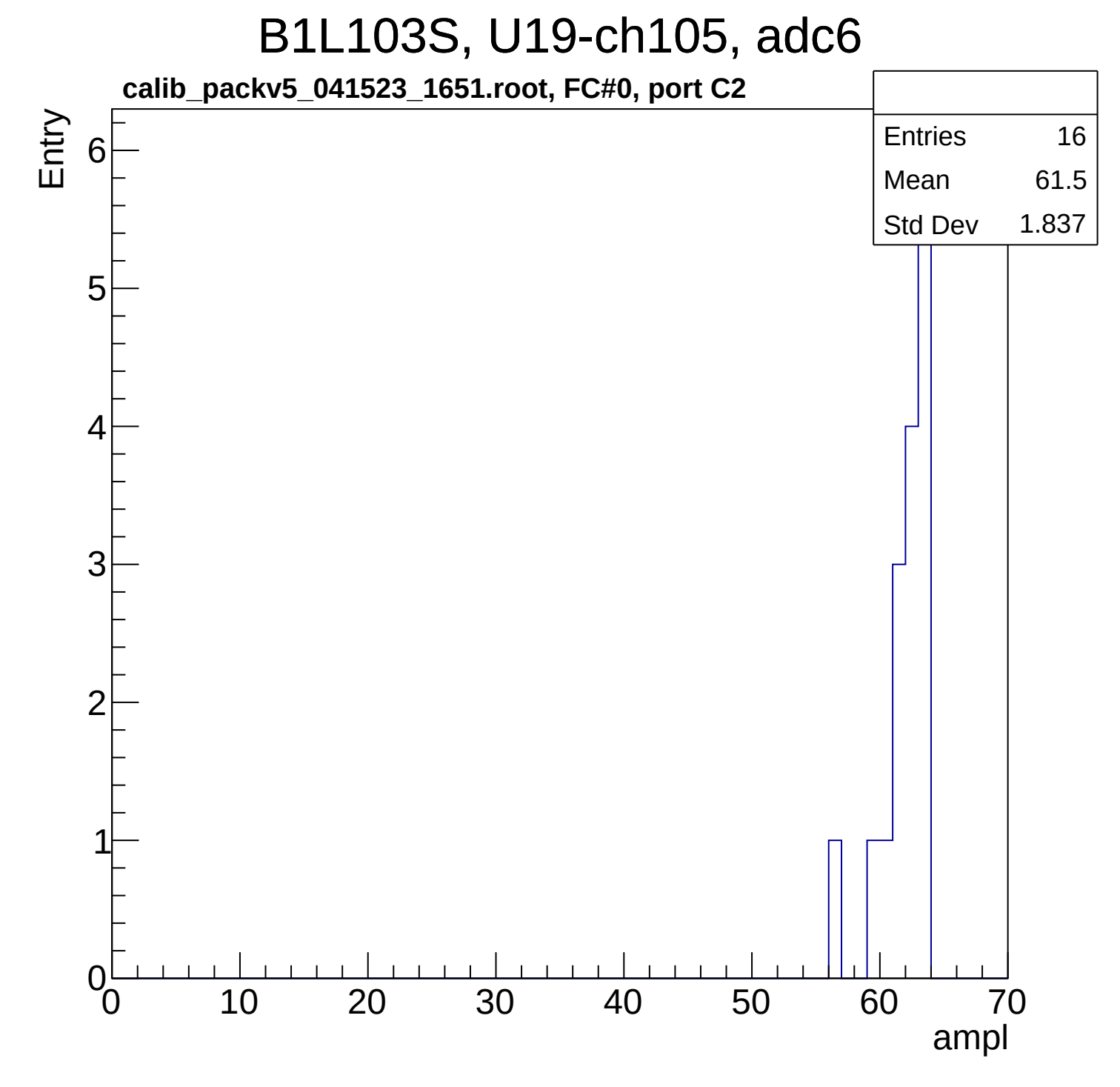
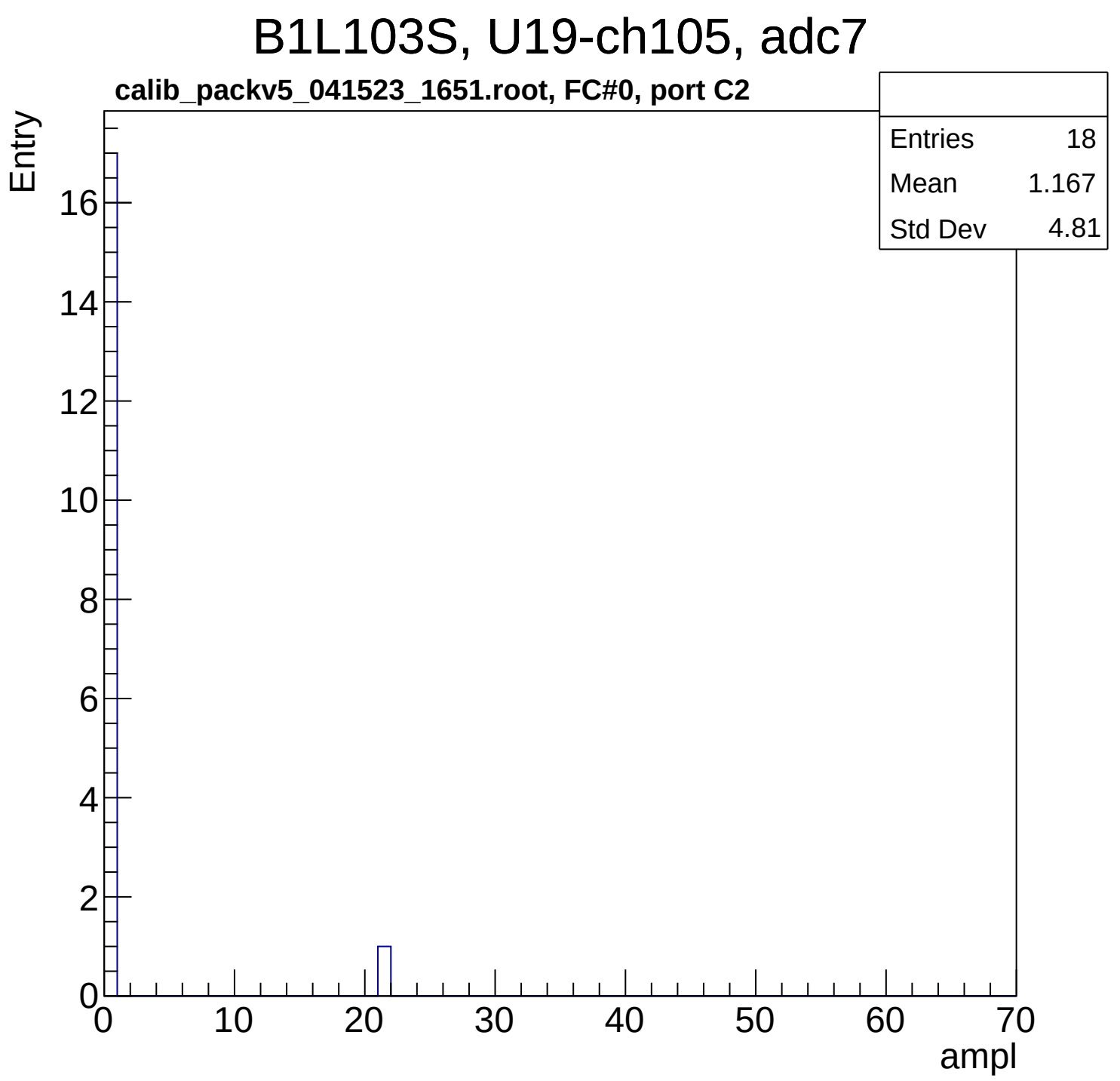
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch105, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 61.5
Std Dev 1.837
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U19-ch105, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.167
Std Dev 4.81
Entry
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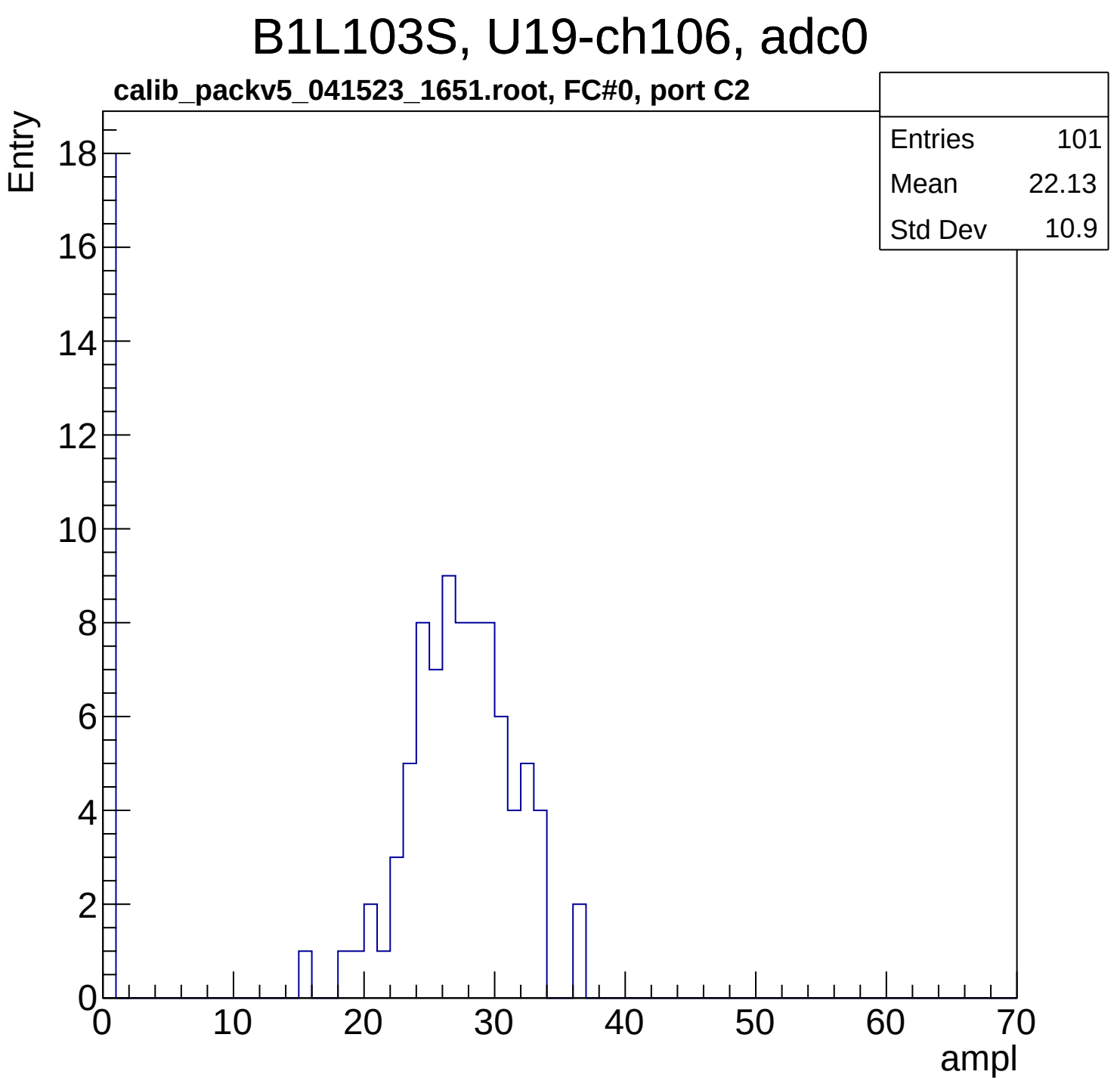
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch106, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 101
Mean 22.13
Std Dev 10.9
Entry
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6
8
10
12
14
16
18
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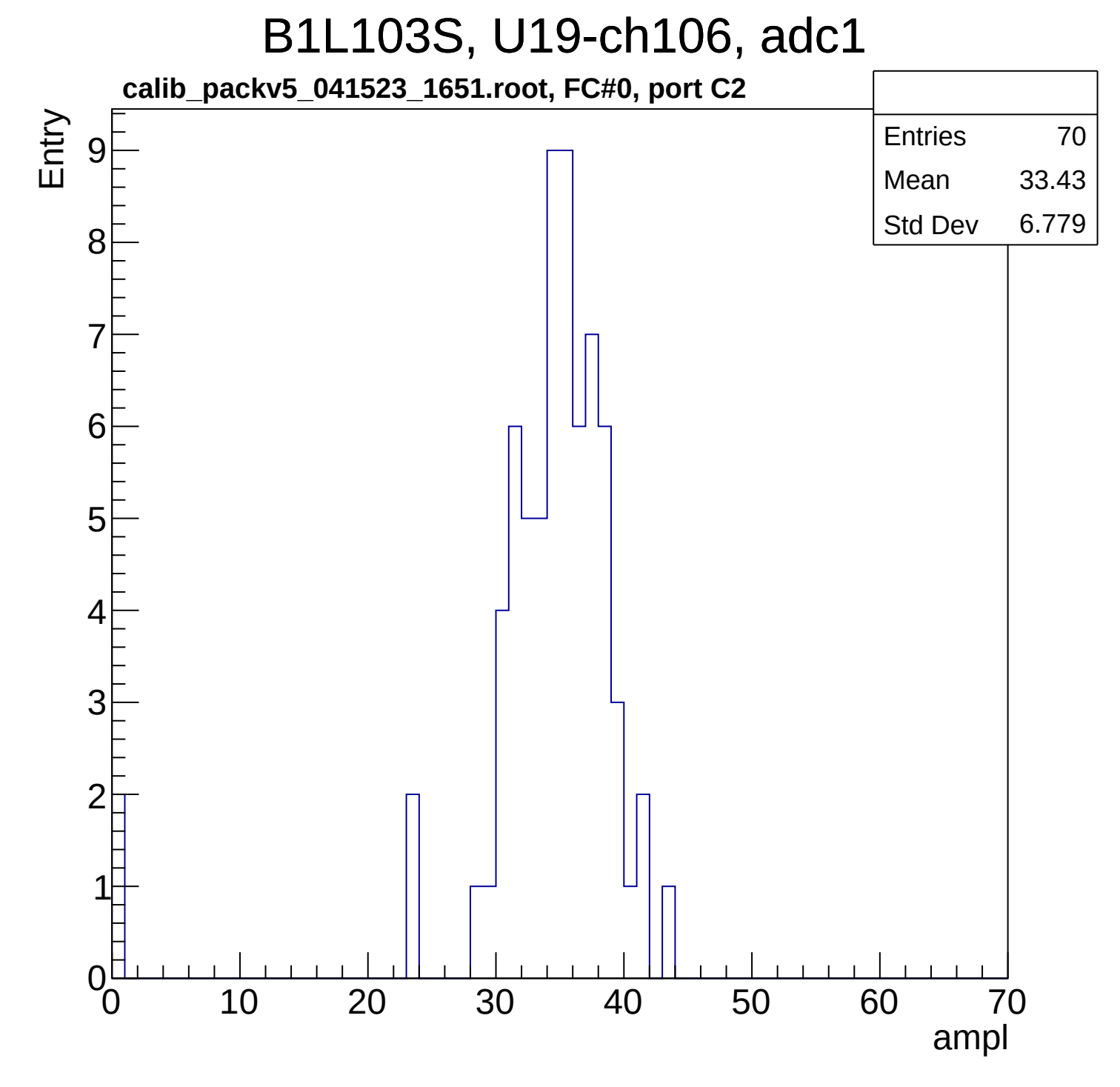
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch106, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 33.43
Std Dev 6.779
Entry
ampl
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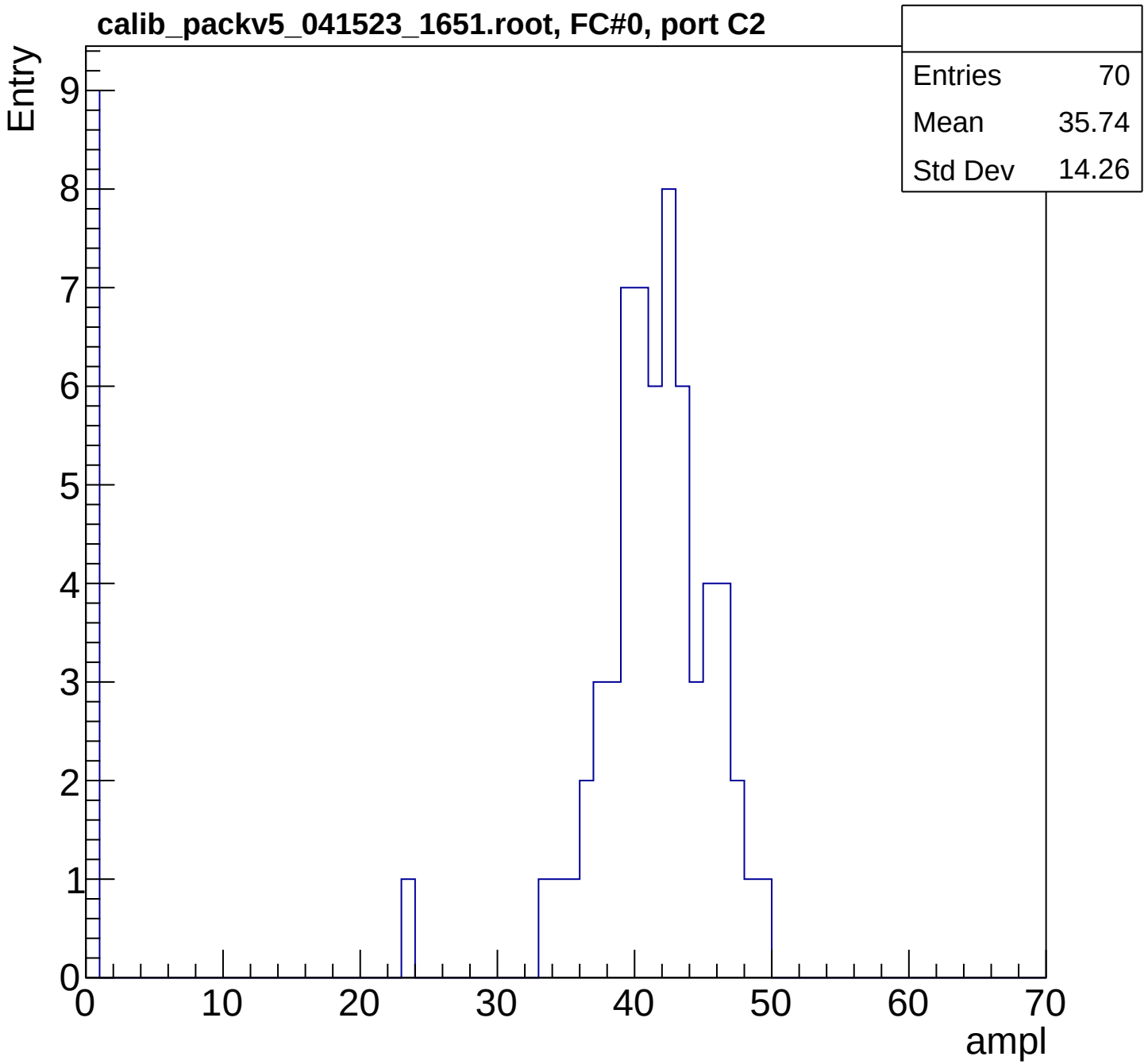
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch106, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 35.74
Std Dev 14.26
Entry
ampl
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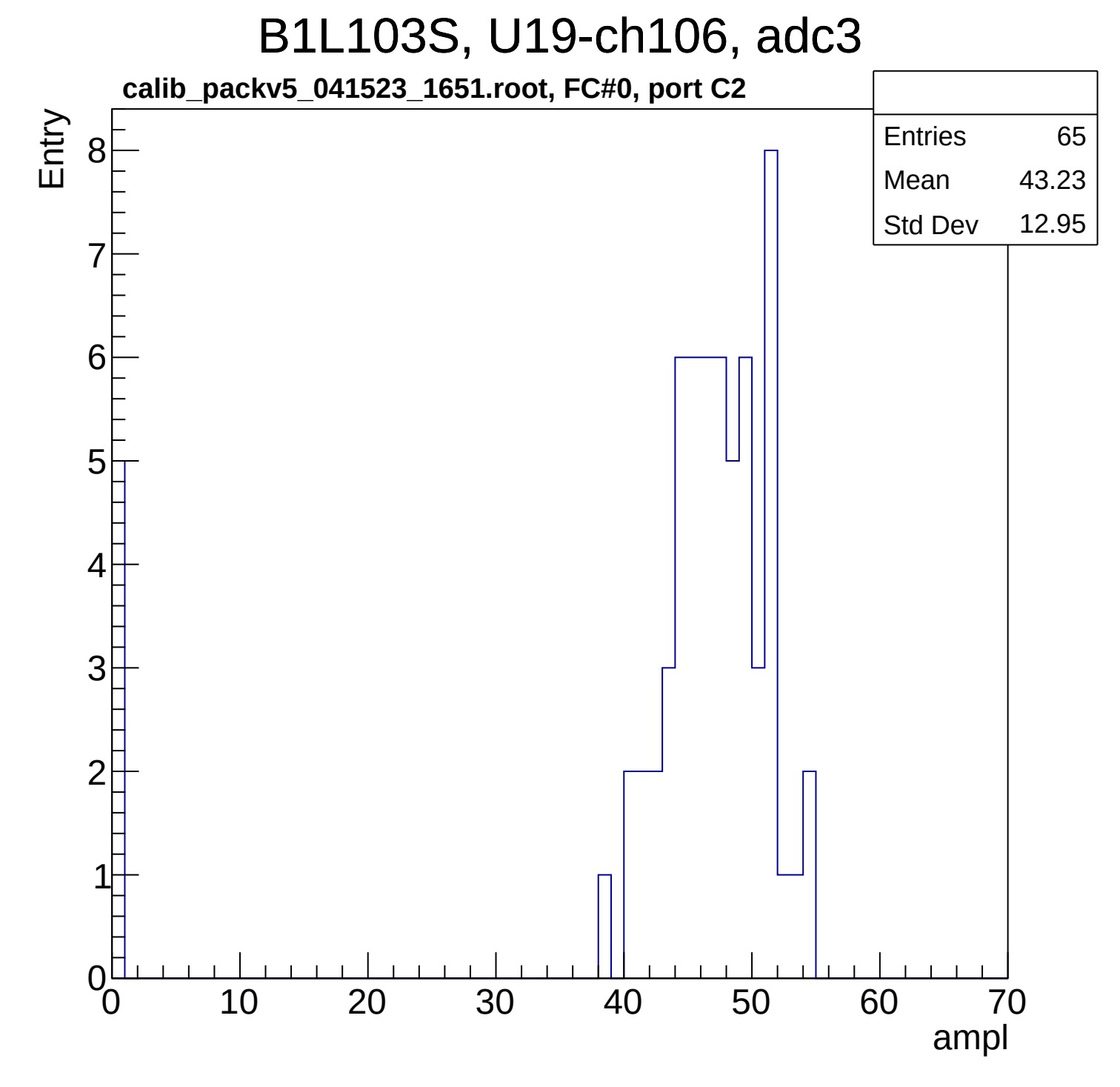
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch106, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 43.23
Std Dev 12.95
Entry
ampl
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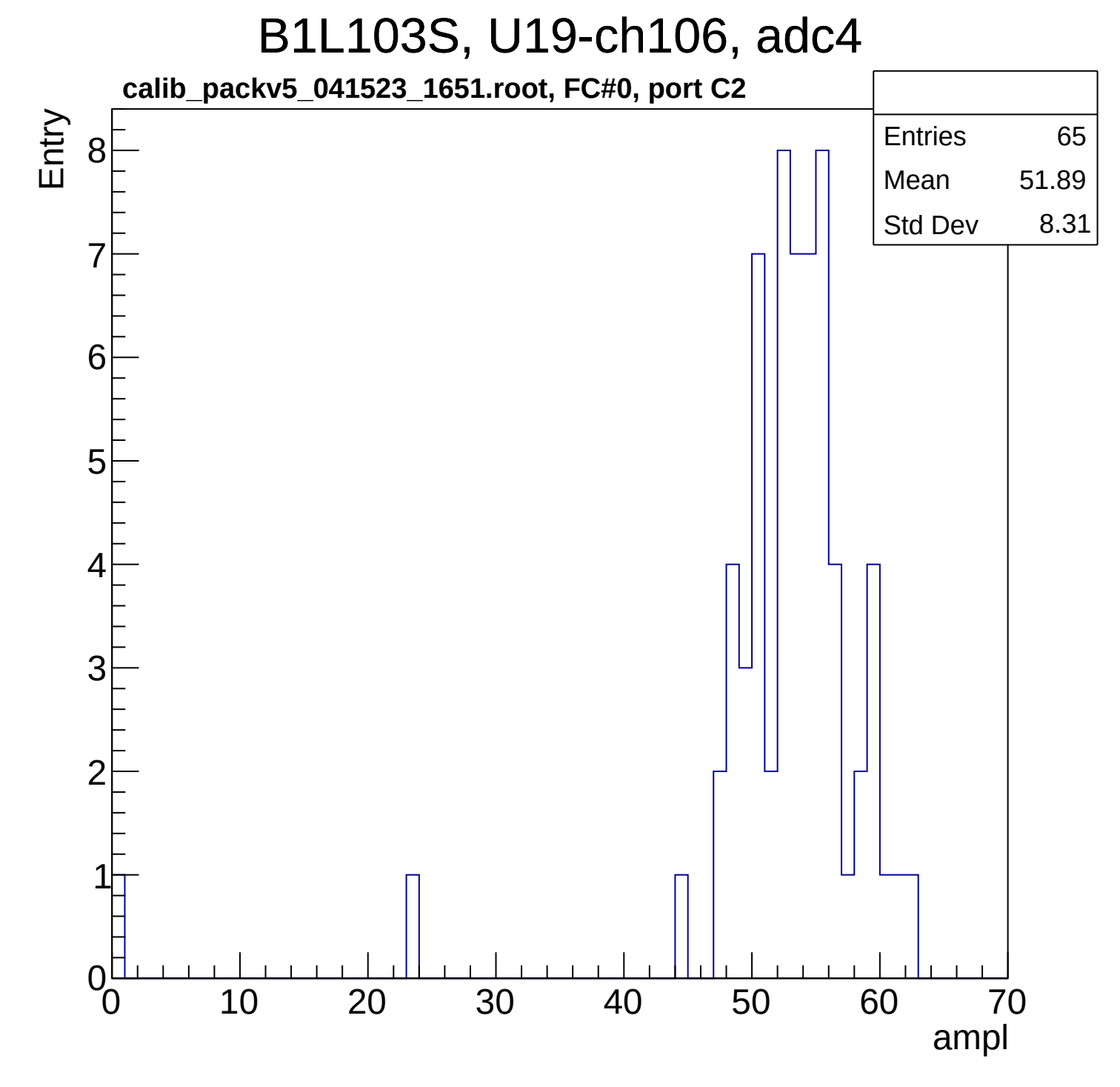
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch106, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 51.89
Std Dev 8.31
Entry
ampl
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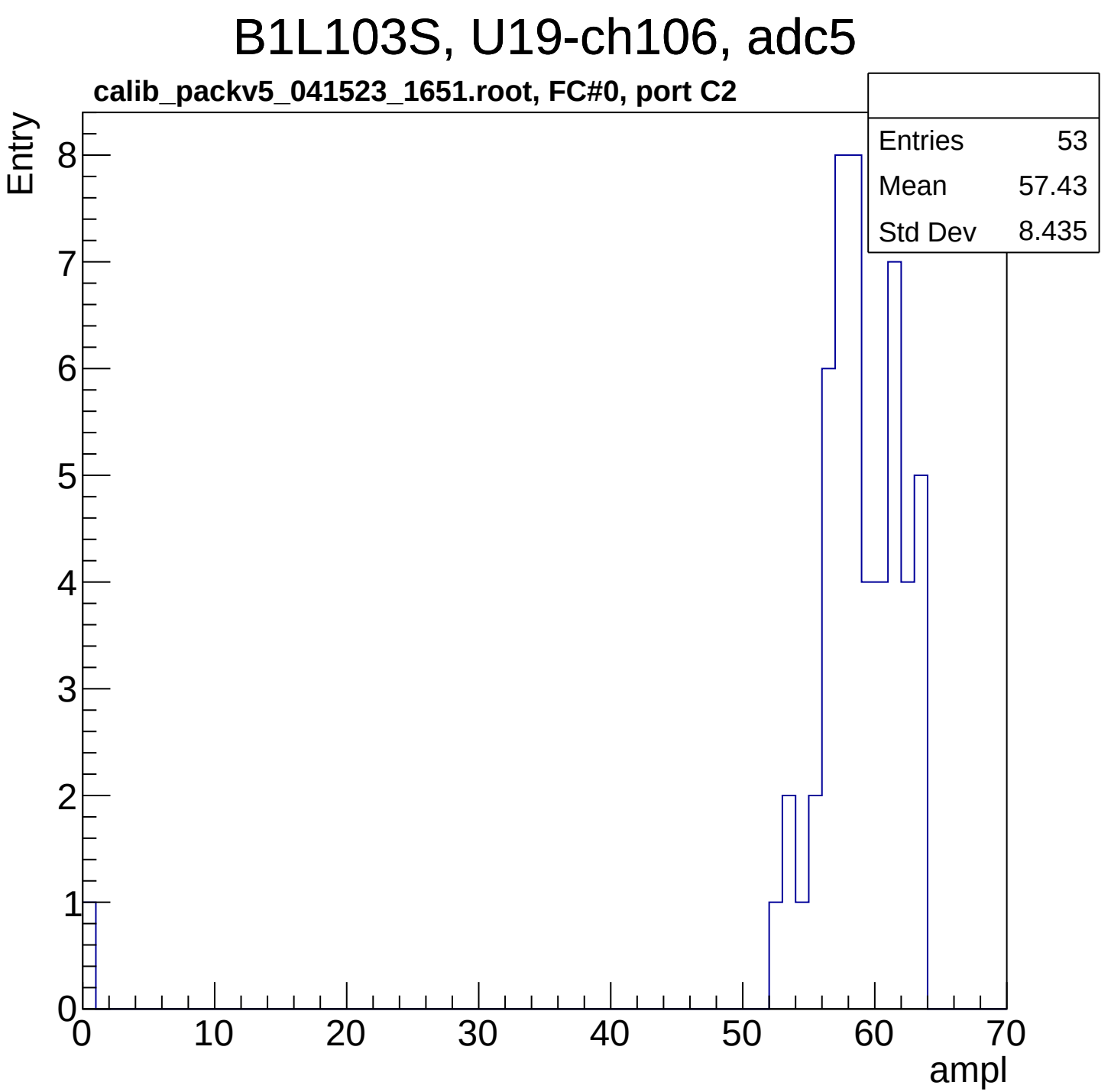
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch106, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 57.43
Std Dev 8.435
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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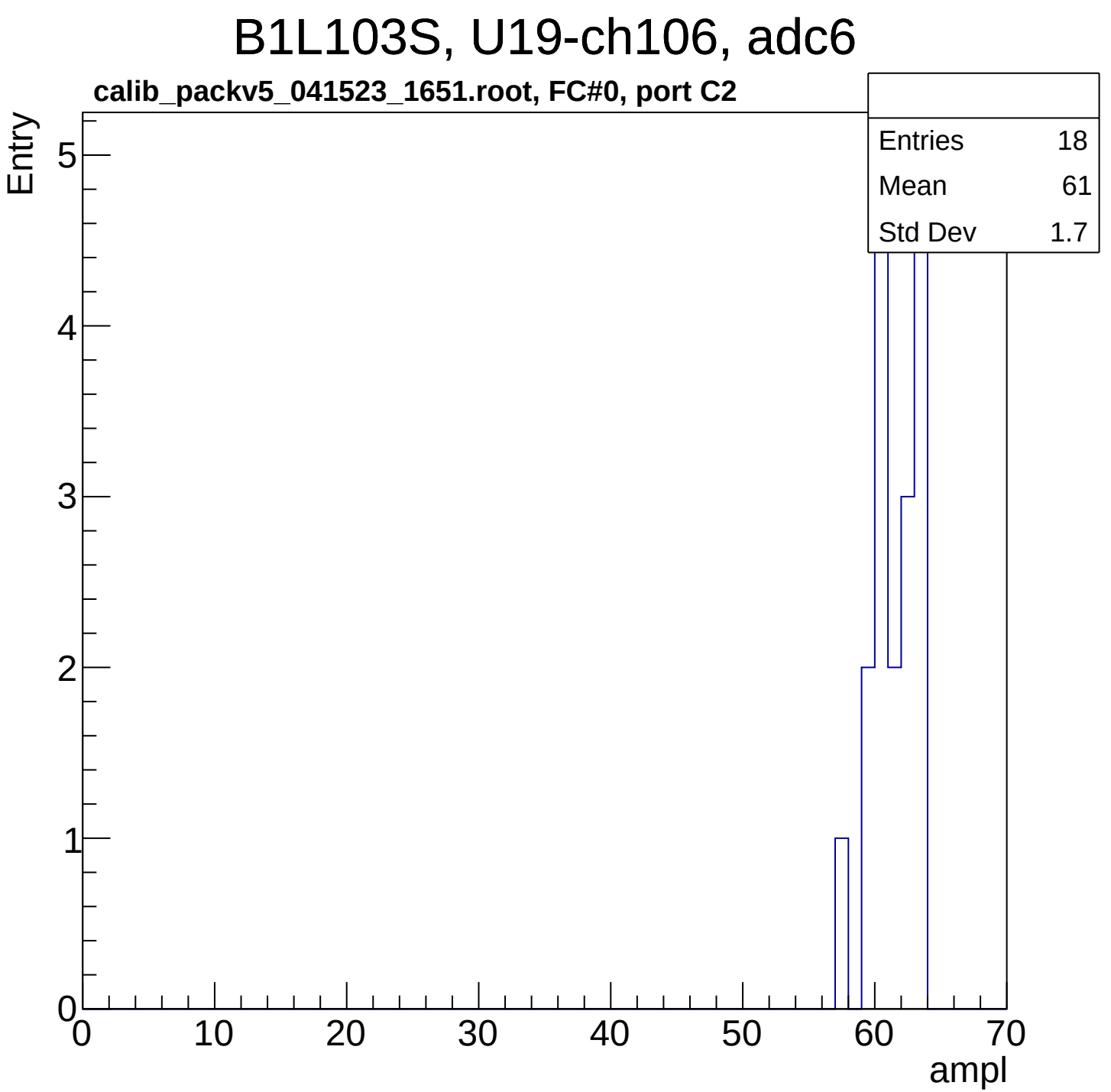
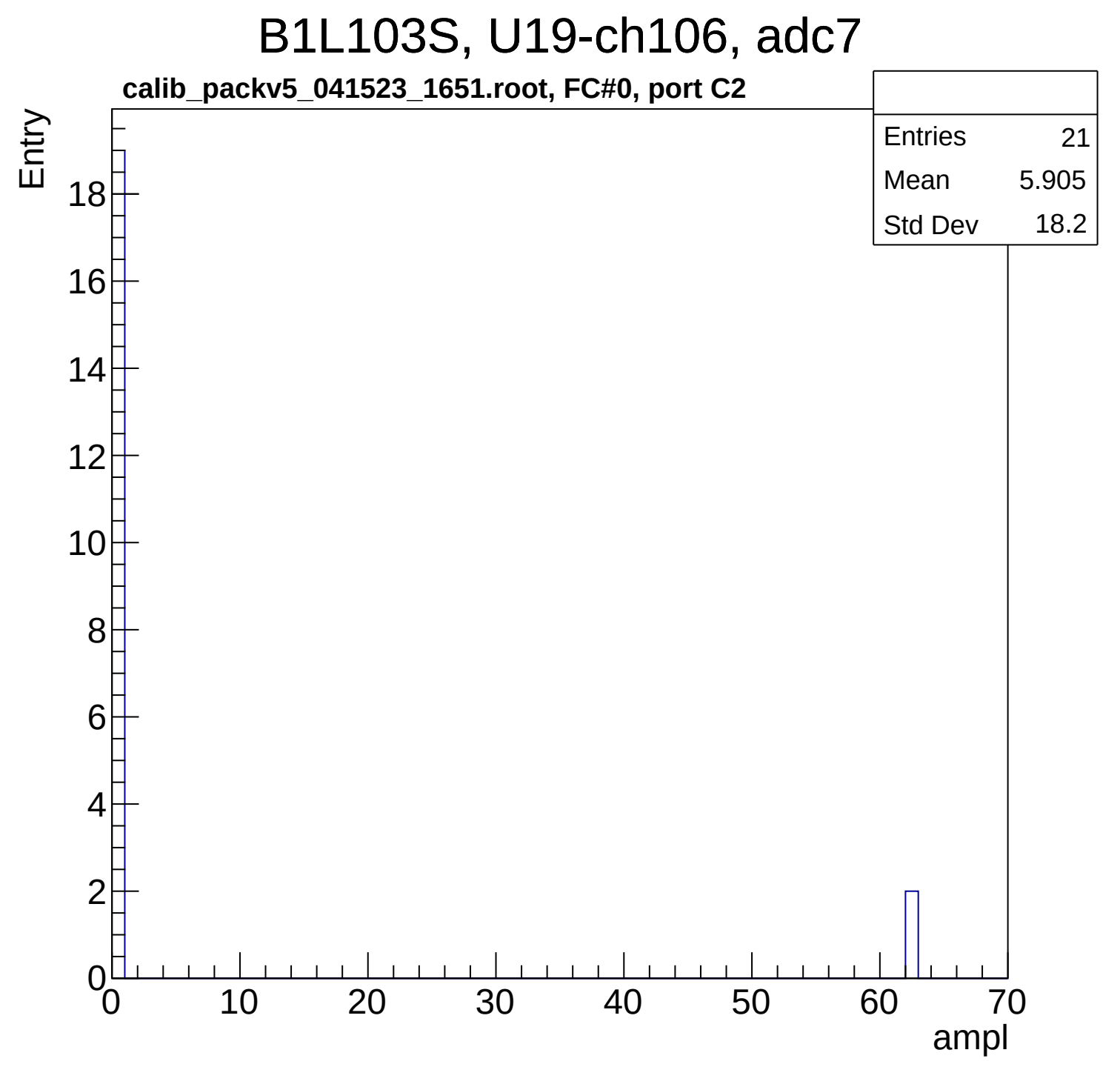

B1L103S, U19-ch106, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 61
Std Dev 1.7
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch106, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.905
Std Dev 18.2
Entry
0
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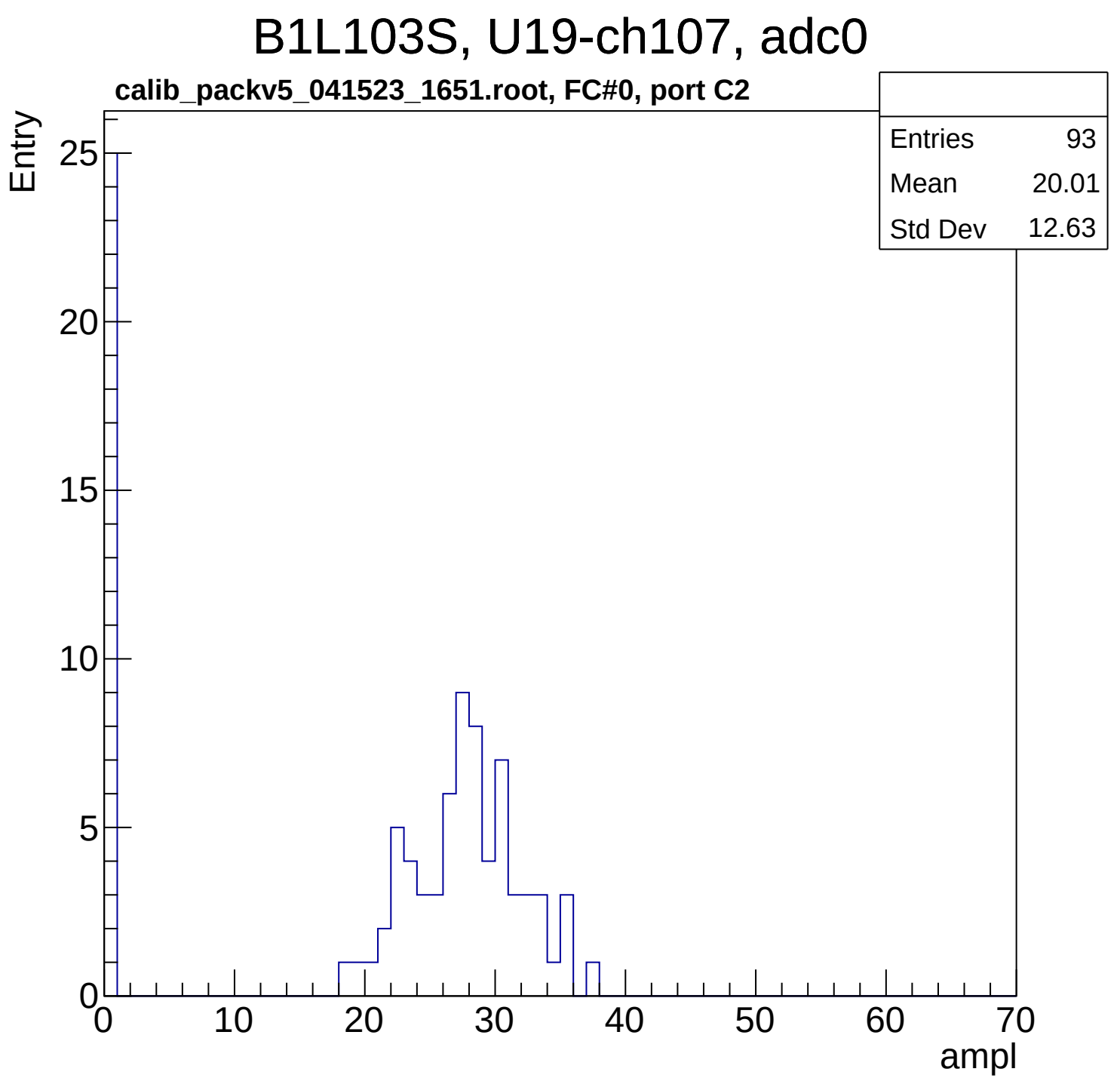
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch107, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 20.01
Std Dev 12.63
Entry
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15
20
25
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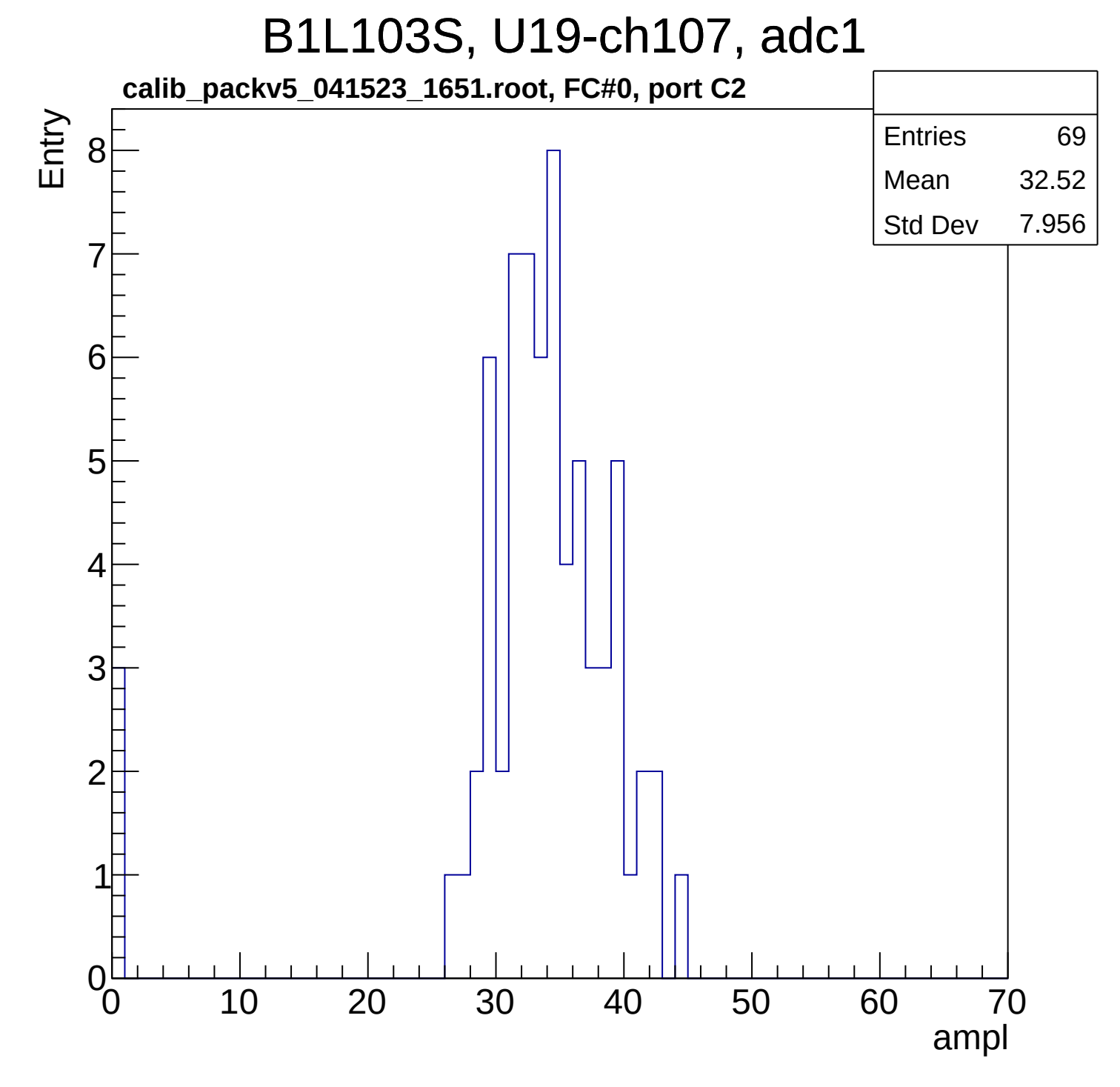
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch107, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 32.52
Std Dev 7.956
Entry
ampl
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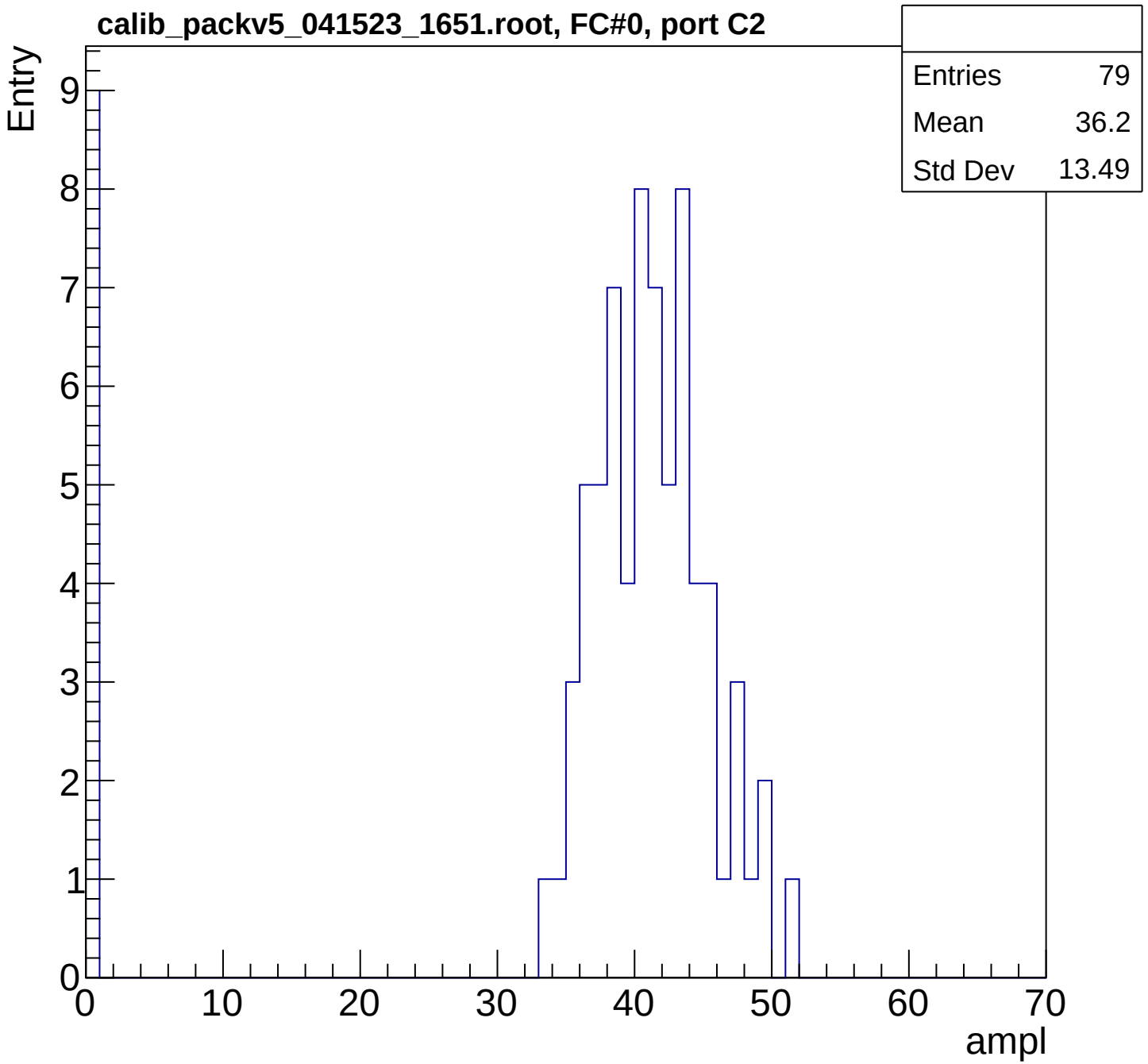
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch107, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 36.2
Std Dev 13.49
Entry
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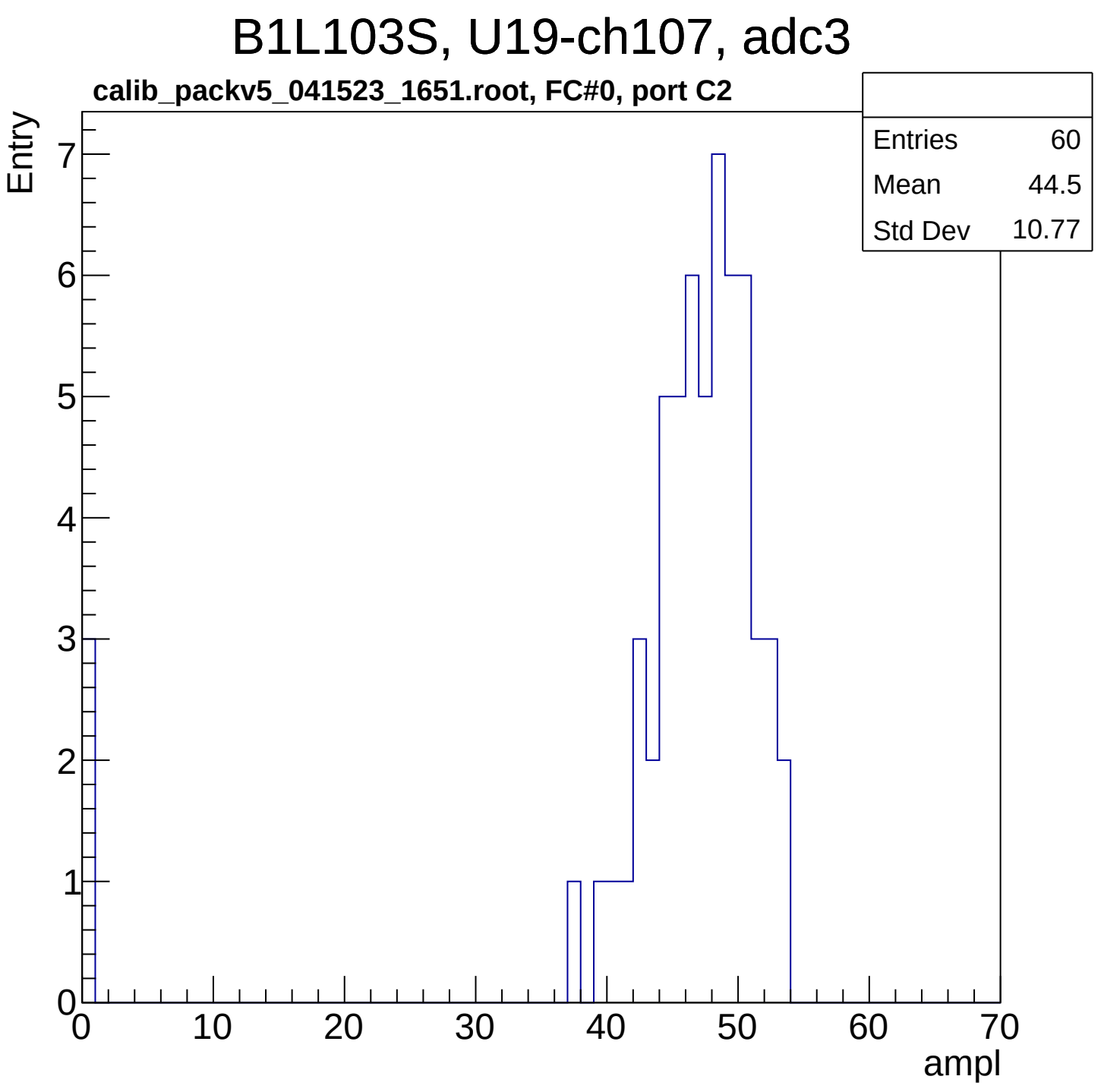
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch107, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 44.5
Std Dev 10.77
Entry
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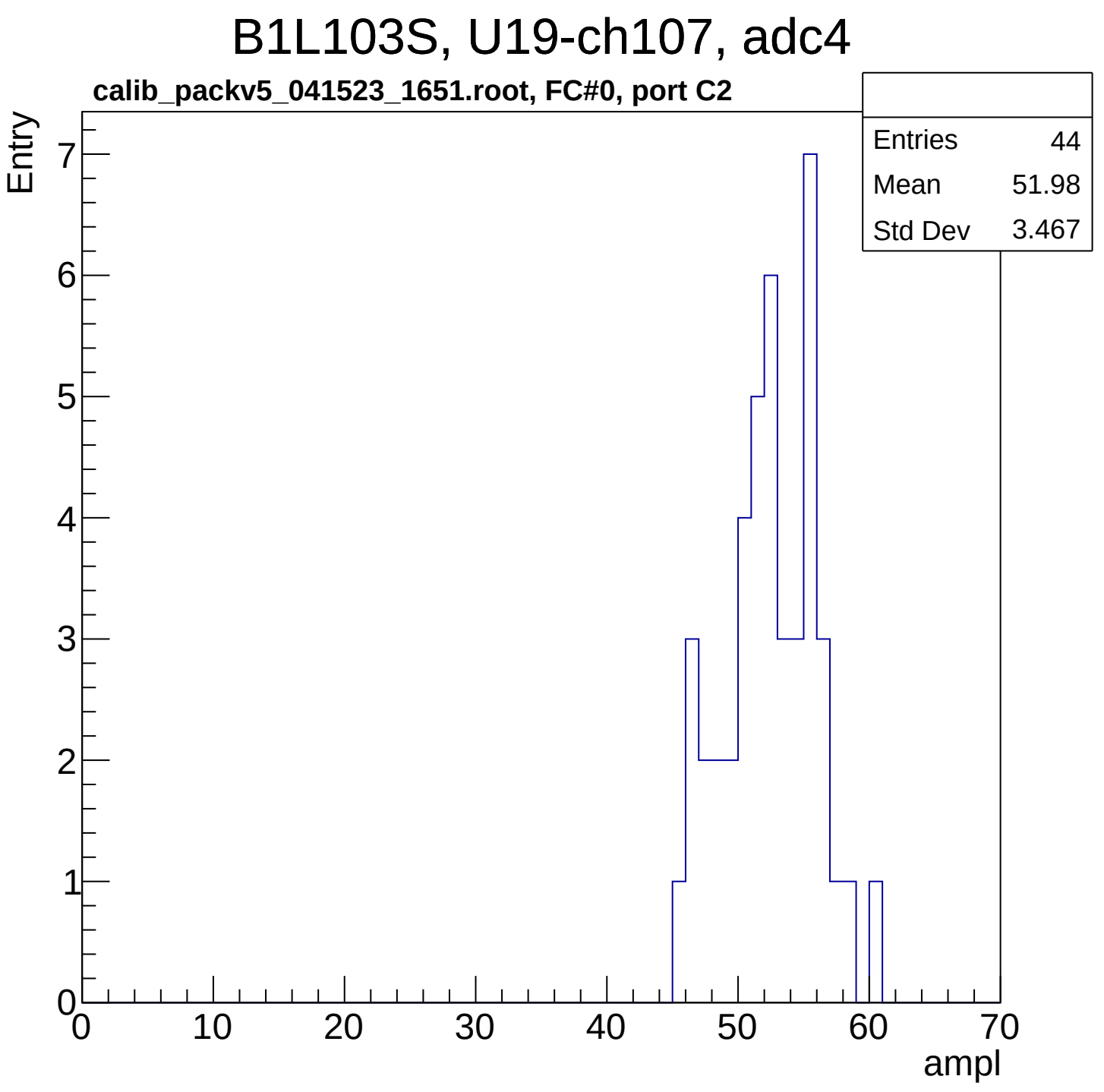
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch107, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 51.98
Std Dev 3.467
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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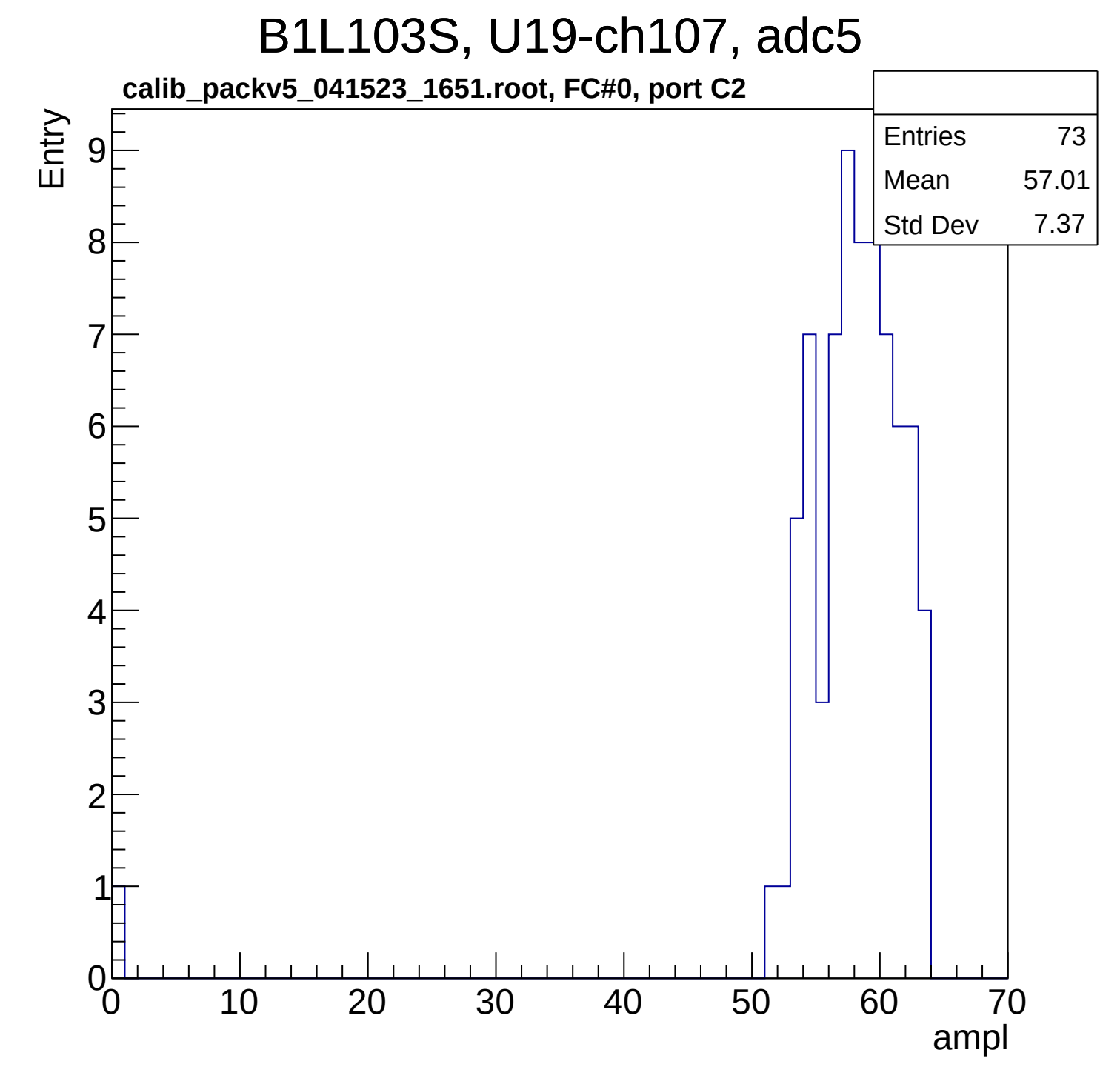
40
50
60
70


B1L103S, U19-ch107, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 57.01
Std Dev 7.37
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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60
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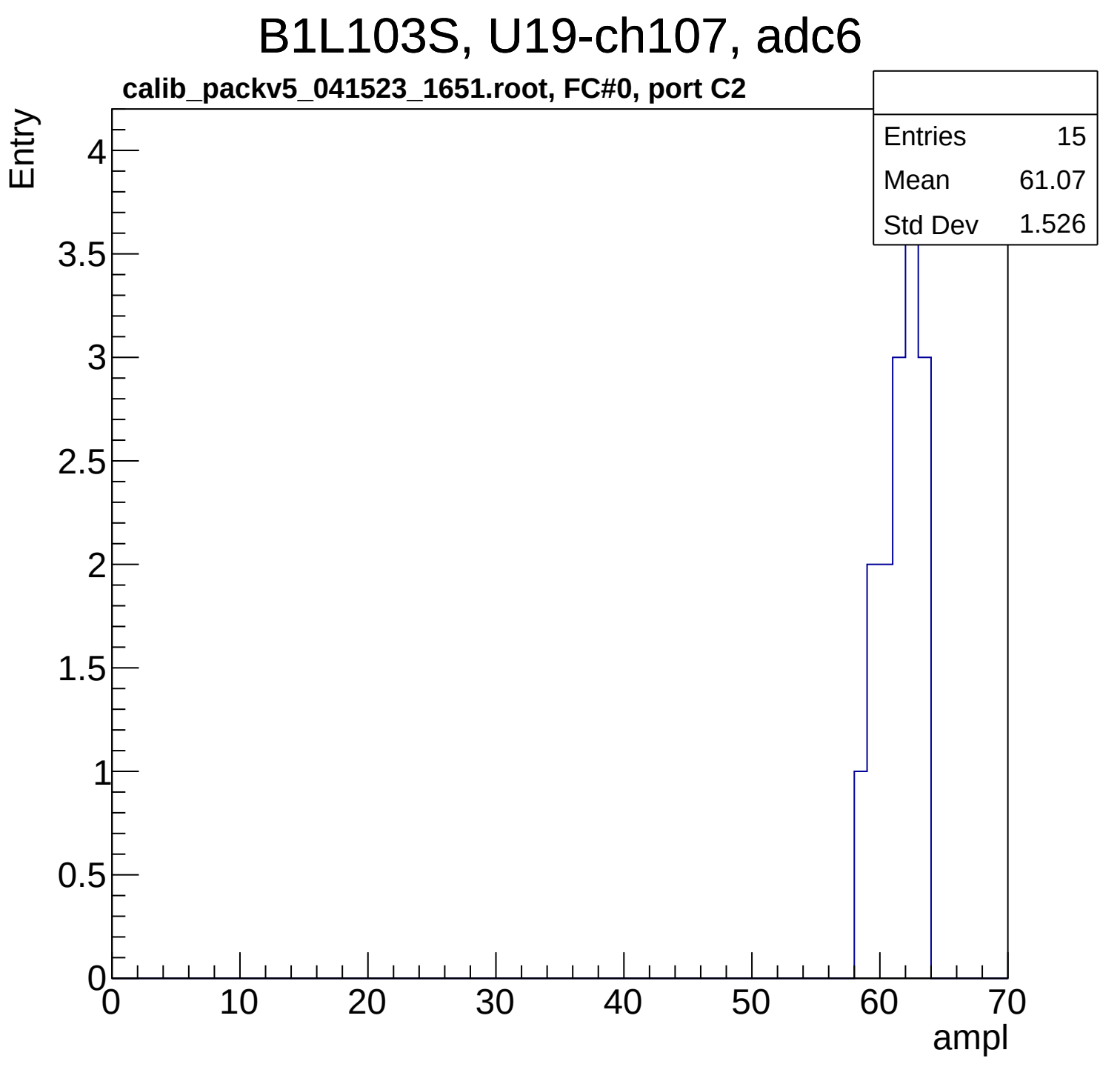
B1L103S, U19-ch107, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 61.07
Std Dev 1.526
Entry
ampl
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0.5
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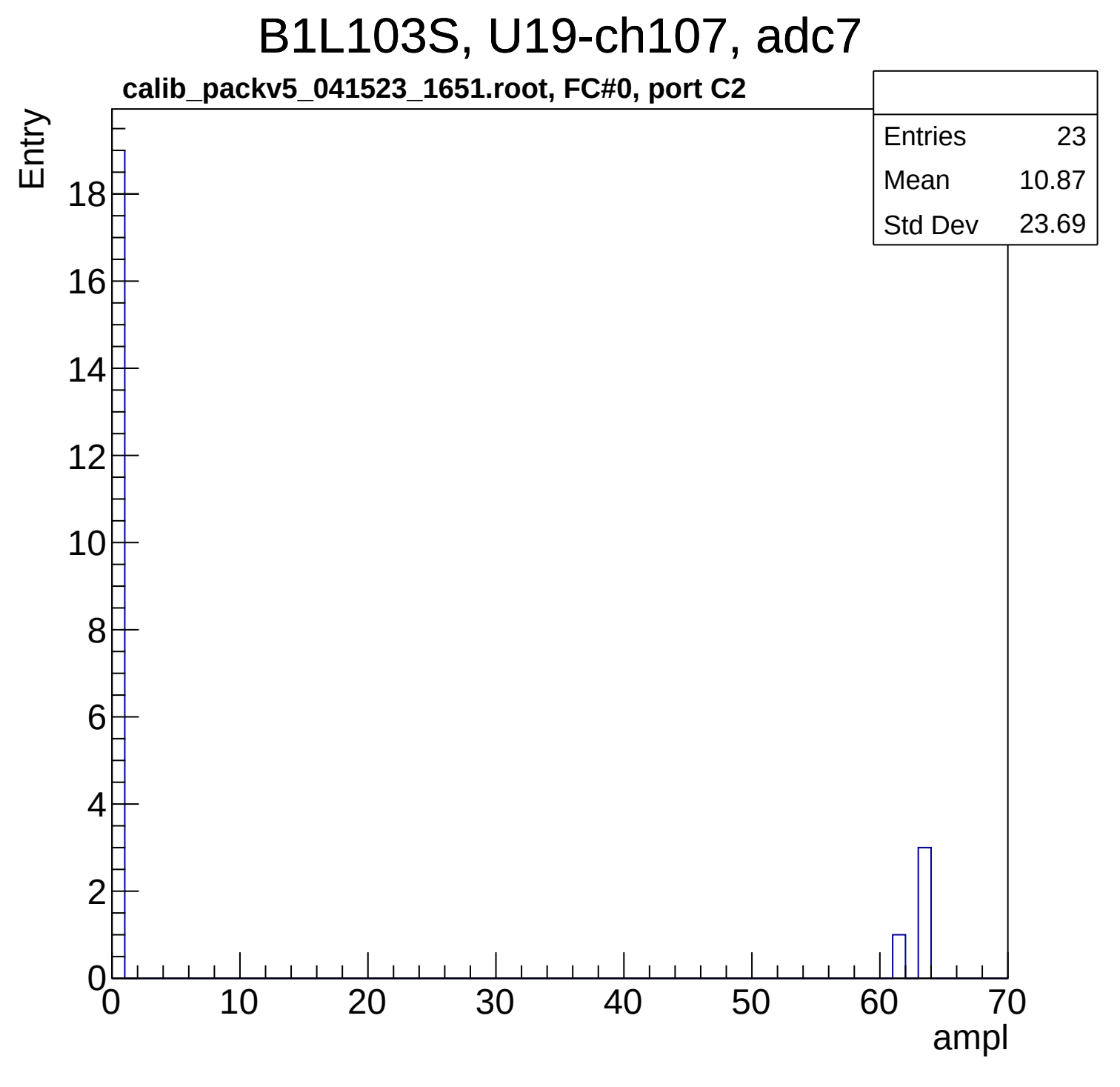
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U19-ch107, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 10.87
Std Dev 23.69
Entry
0
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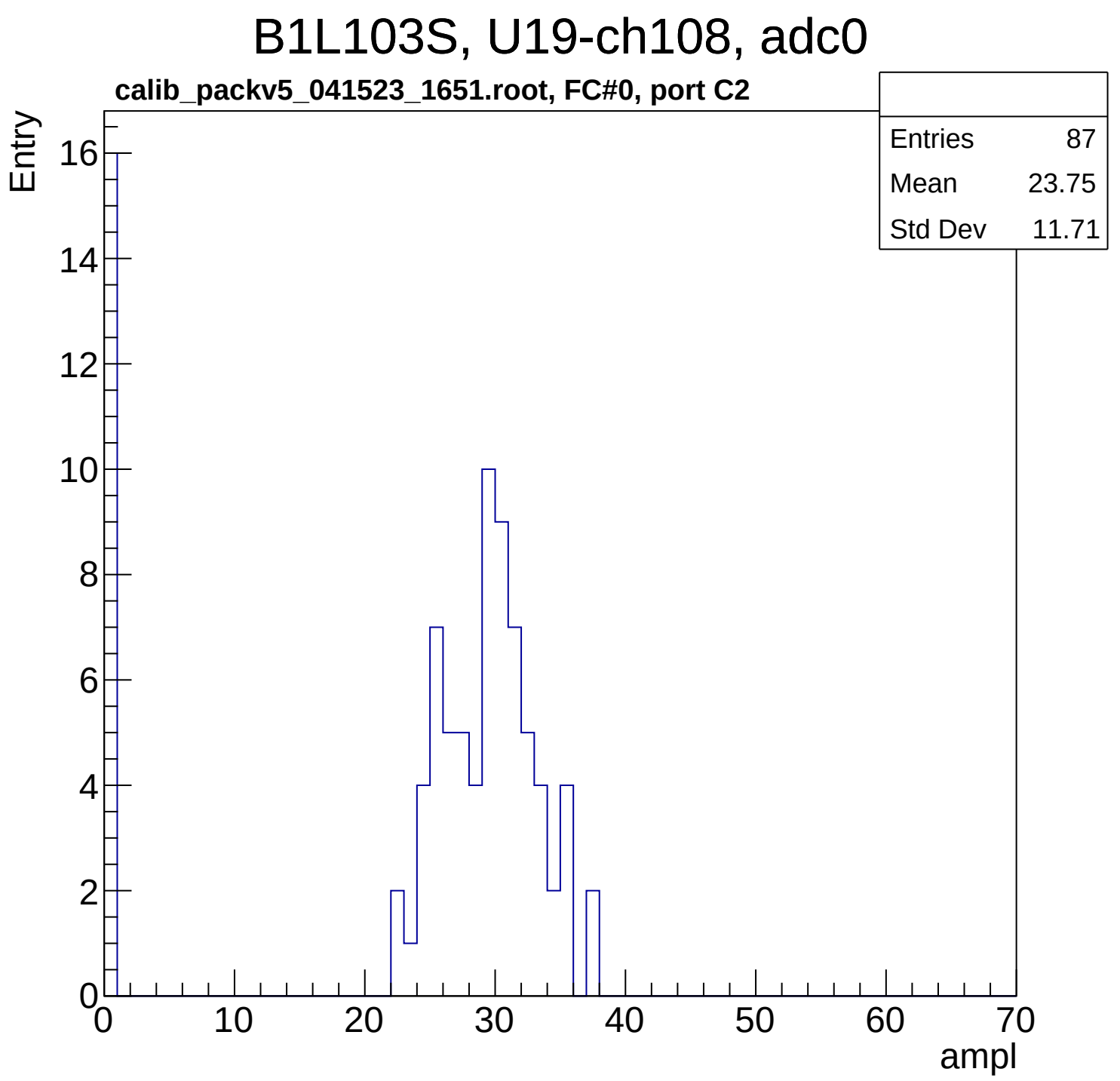
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch108, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 23.75
Std Dev 11.71
Entry
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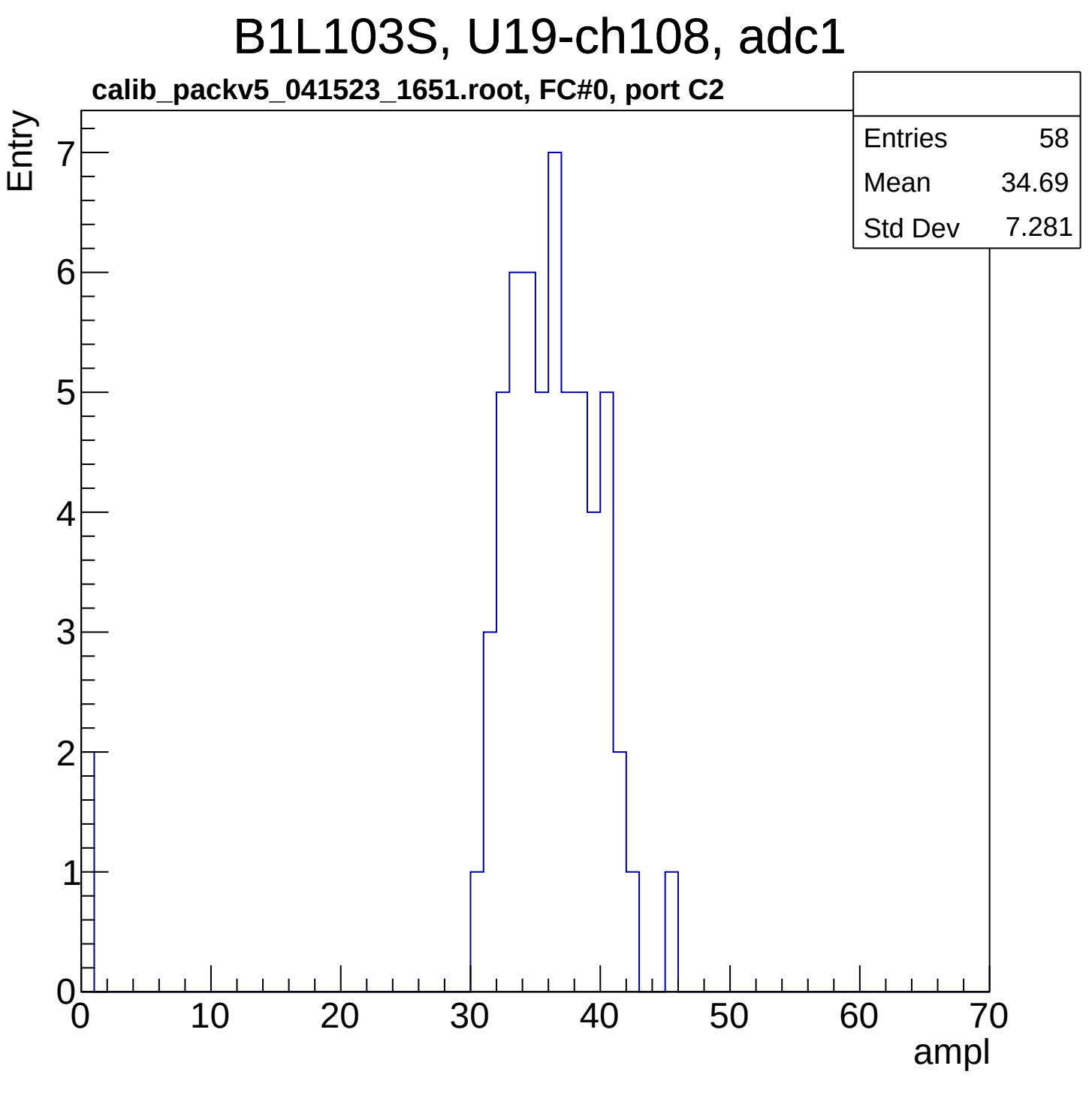
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch108, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 34.69
Std Dev 7.281
Entry
ampl
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2
3
4
5
6
7
0
10
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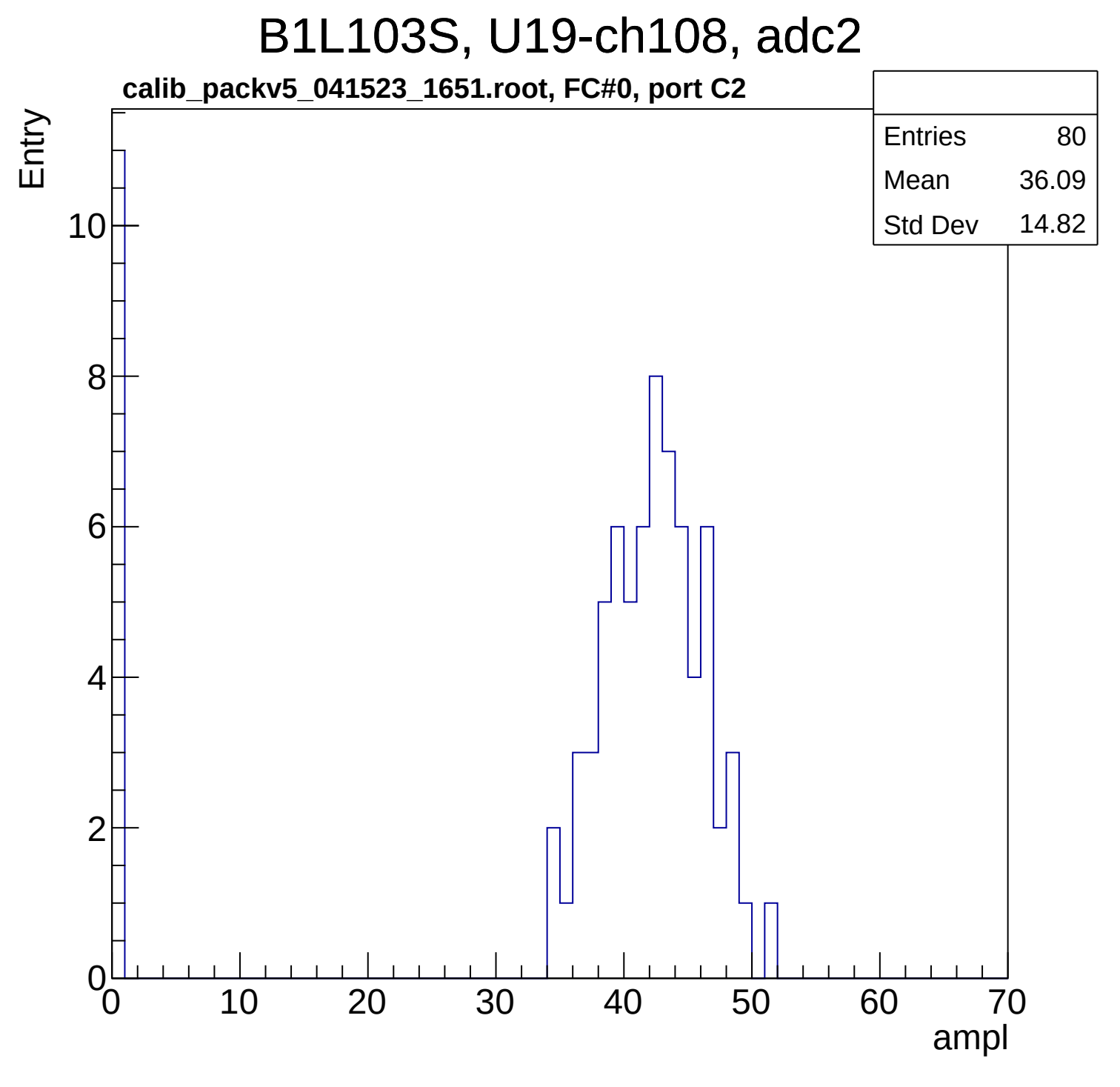
30
40
50
60
70


B1L103S, U19-ch108, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 36.09
Std Dev 14.82
Entry
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2
4
6
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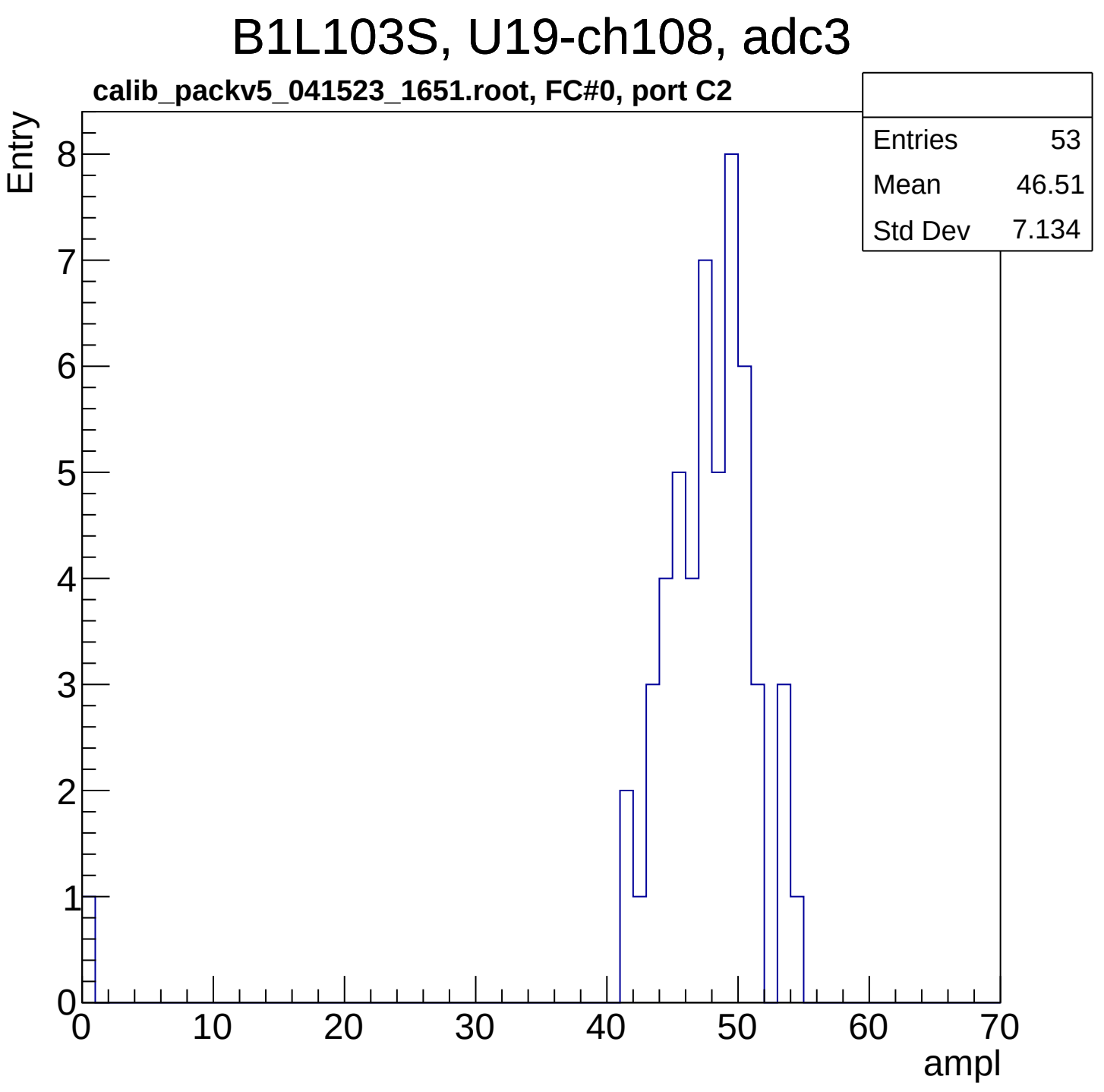
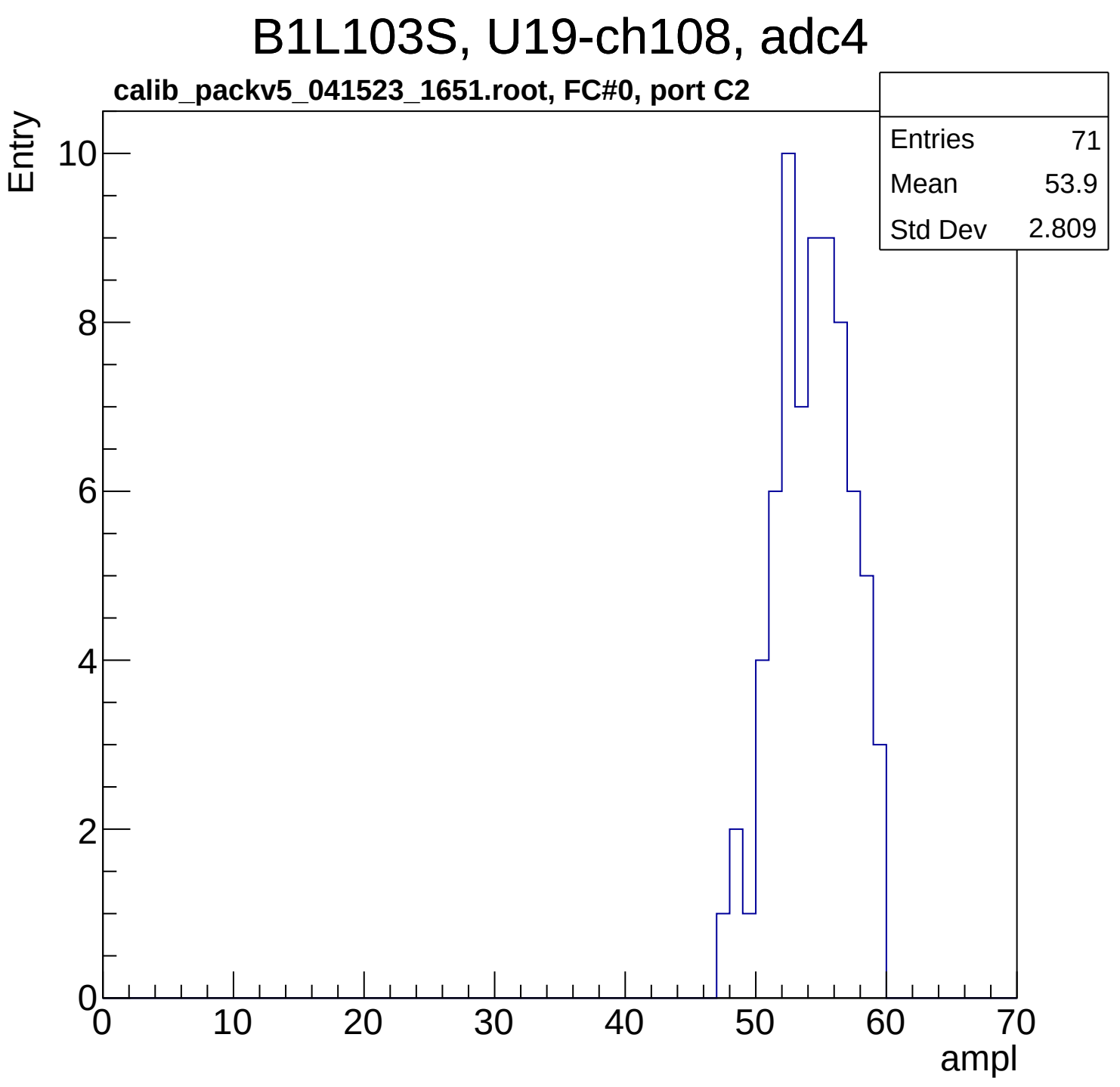
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch108, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 46.51
Std Dev 7.134
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch108, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 53.9
Std Dev 2.809
Entry
0
2
4
6
8
10
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10
20
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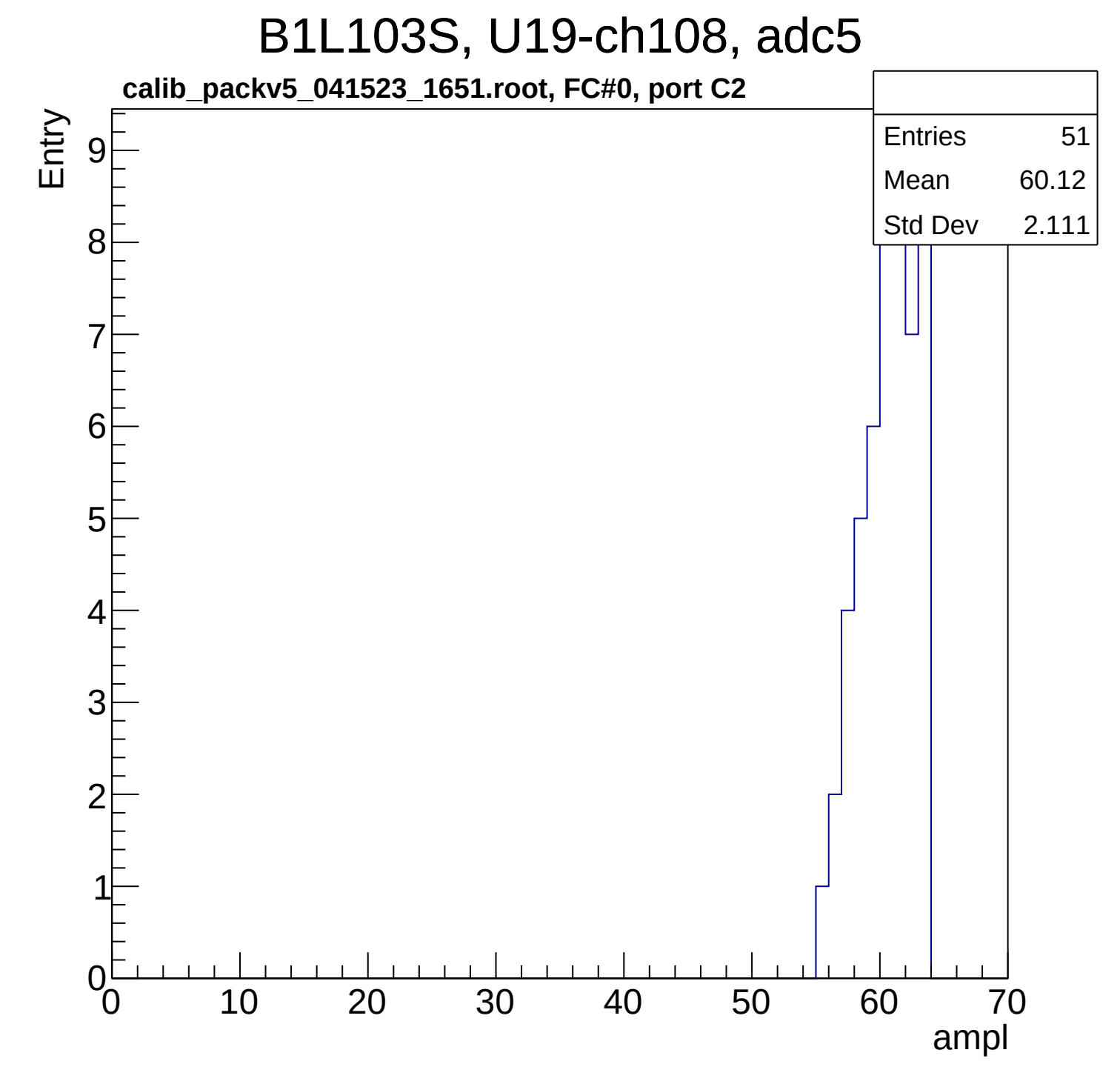
70
ampl


B1L103S, U19-ch108, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 60.12
Std Dev 2.111
Entry
ampl
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0
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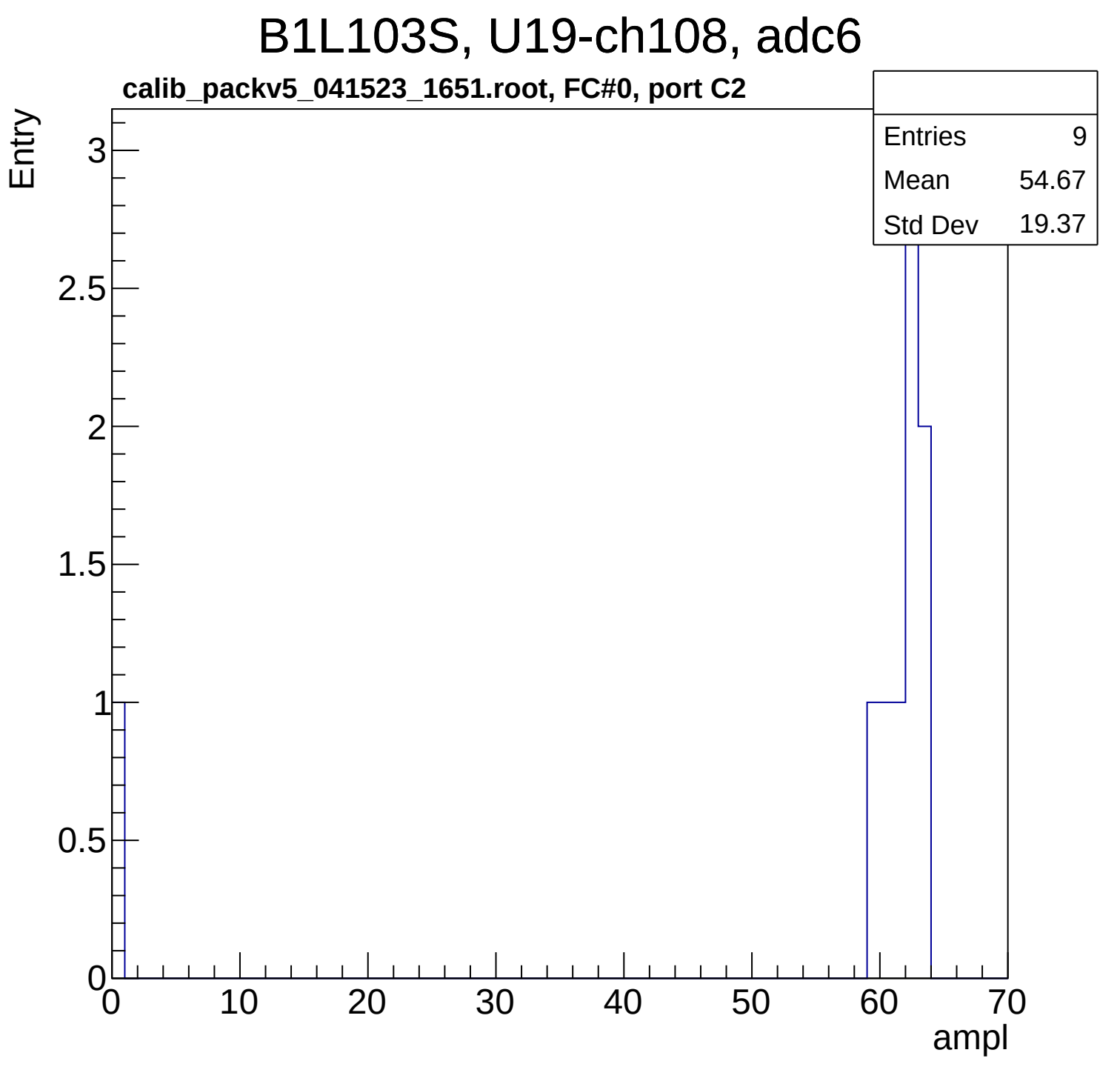
B1L103S, U19-ch108, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 54.67
Std Dev 19.37
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
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40
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60
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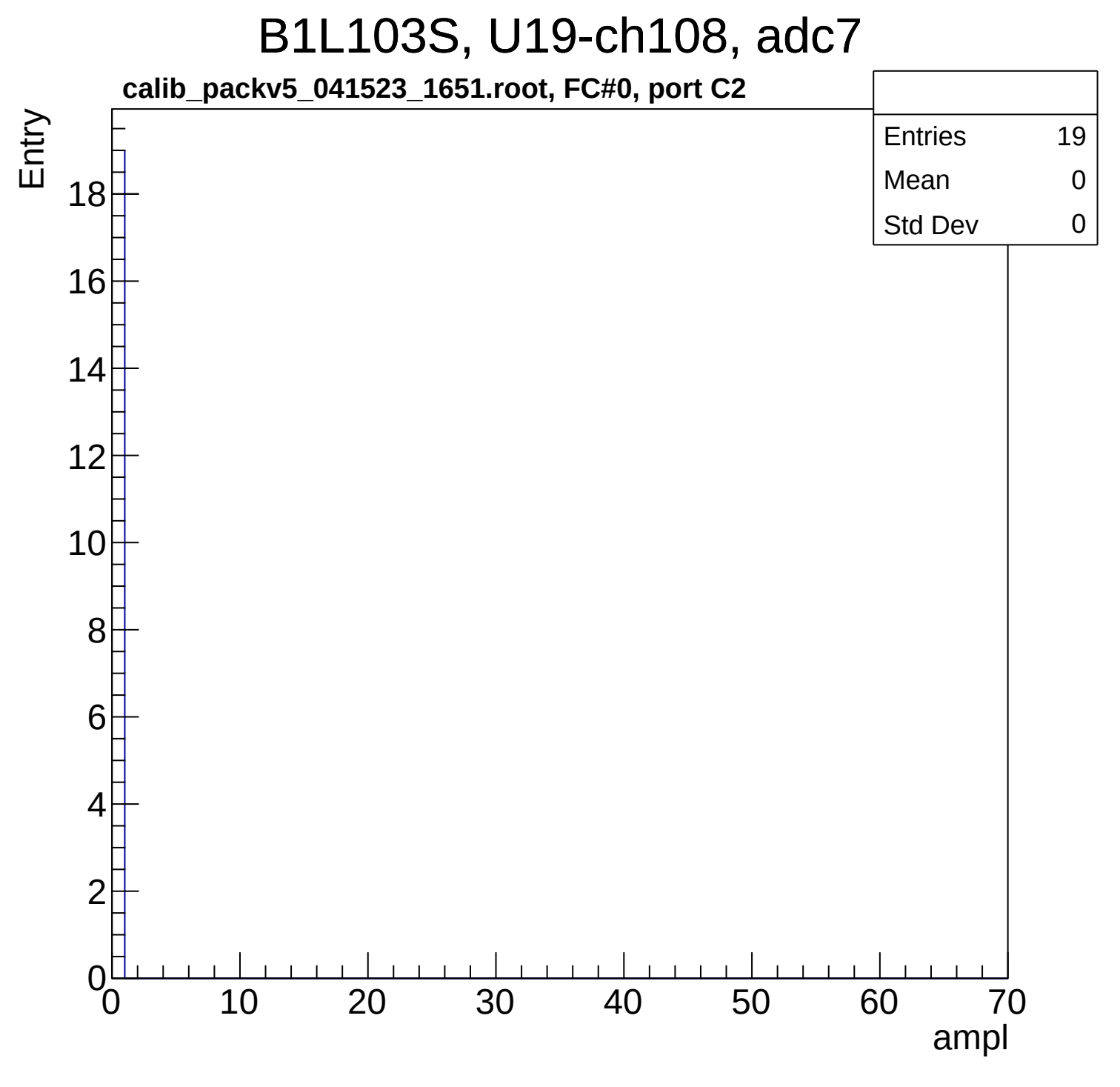
B1L103S, U19-ch108, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
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10
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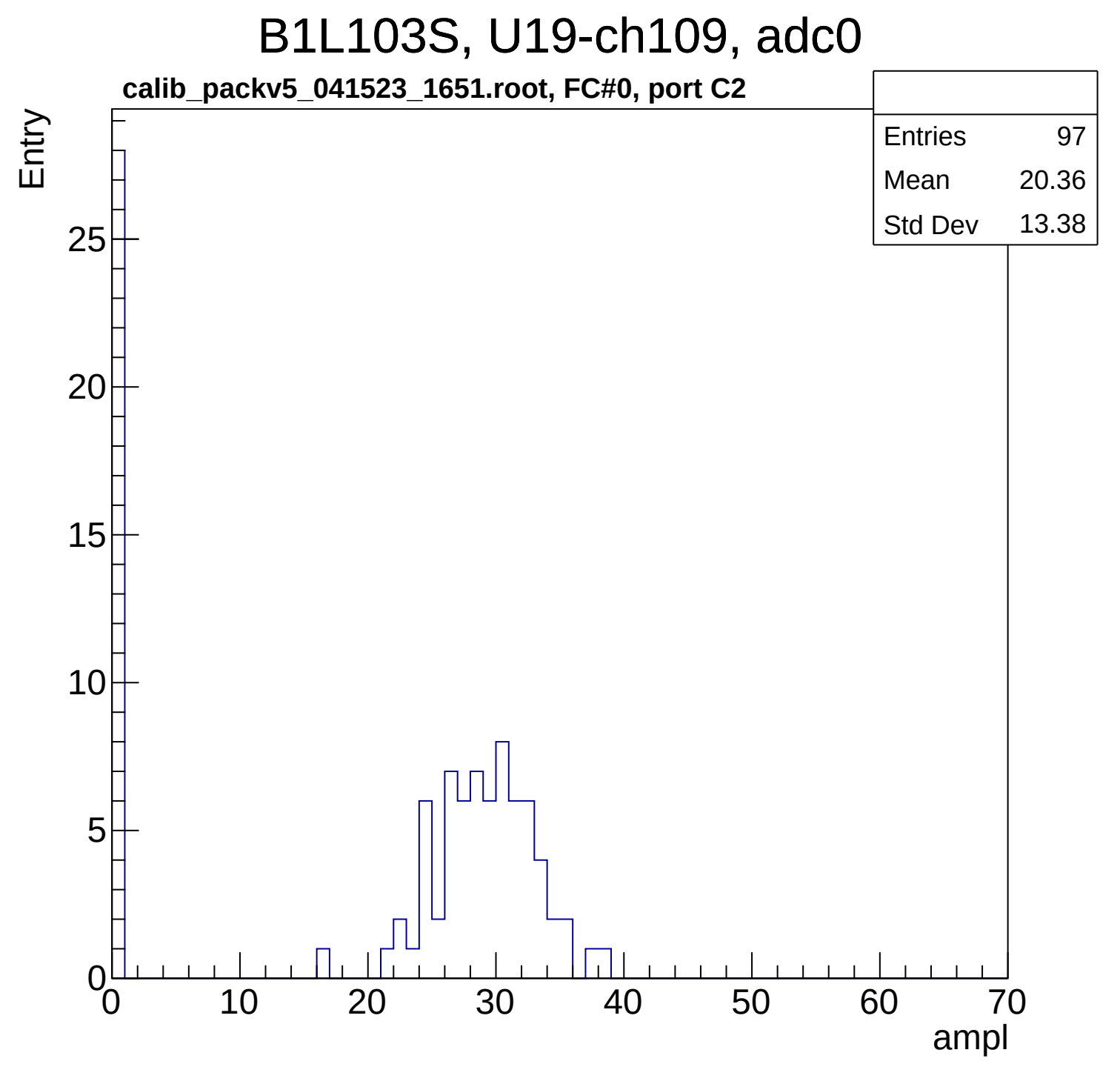
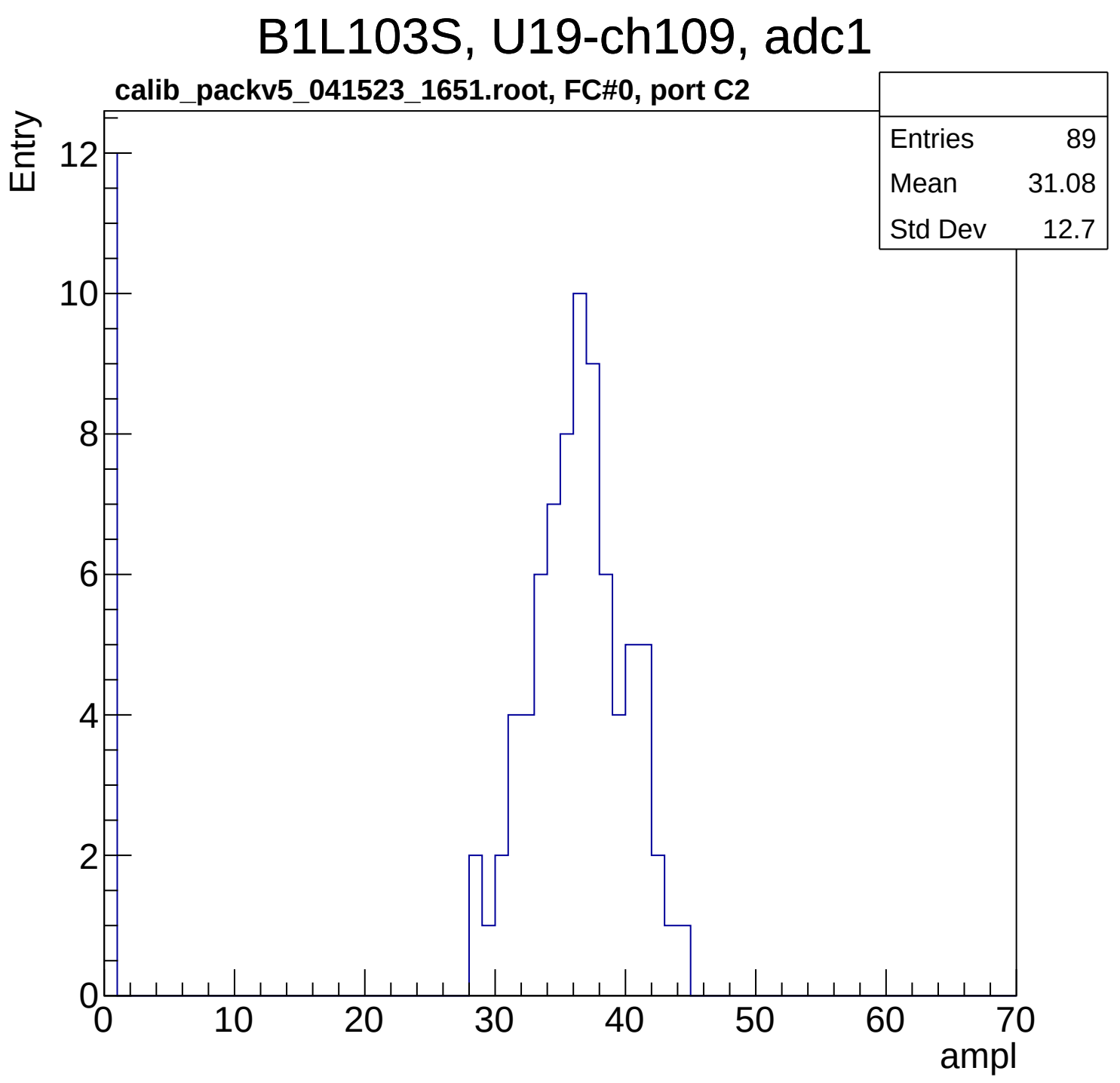
50
60
70
ampl


B1L103S, U19-ch109, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 20.36
Std Dev 13.38
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch109, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 31.08
Std Dev 12.7
Entry
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8
10
12
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10
20
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50
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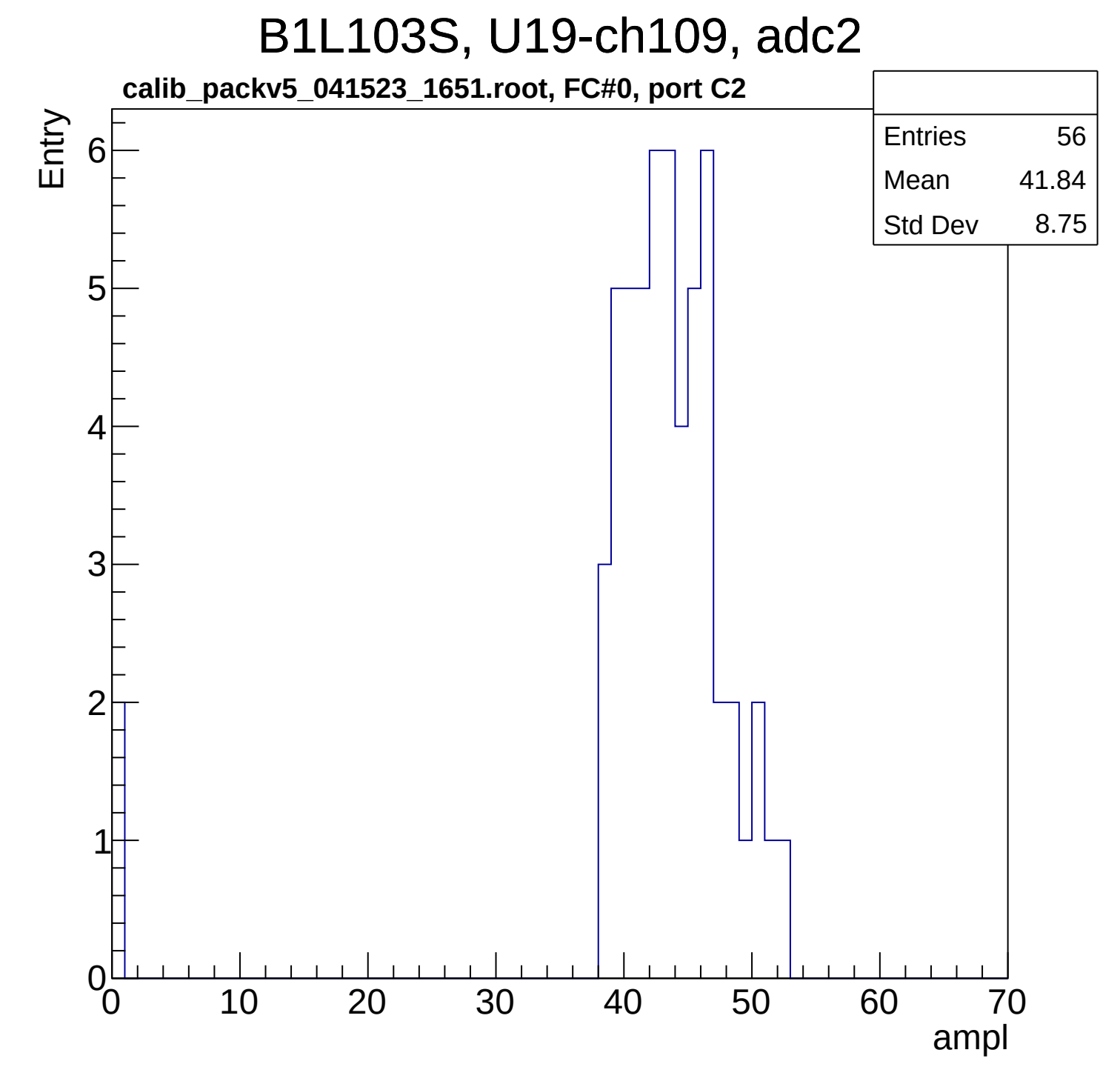
70
ampl


B1L103S, U19-ch109, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 41.84
Std Dev 8.75
Entry
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2
3
4
5
6
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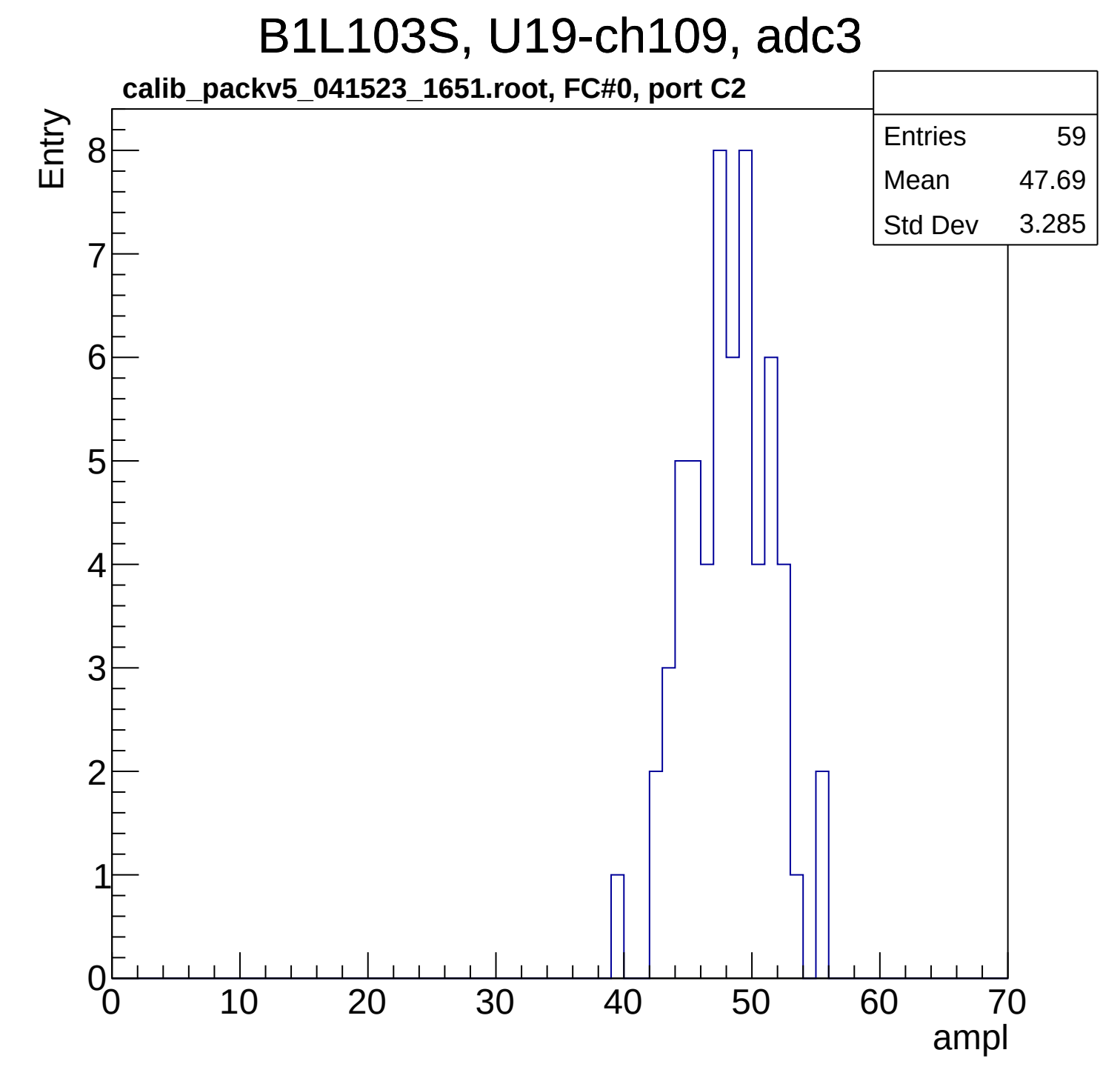
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch109, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 47.69
Std Dev 3.285
Entry
ampl
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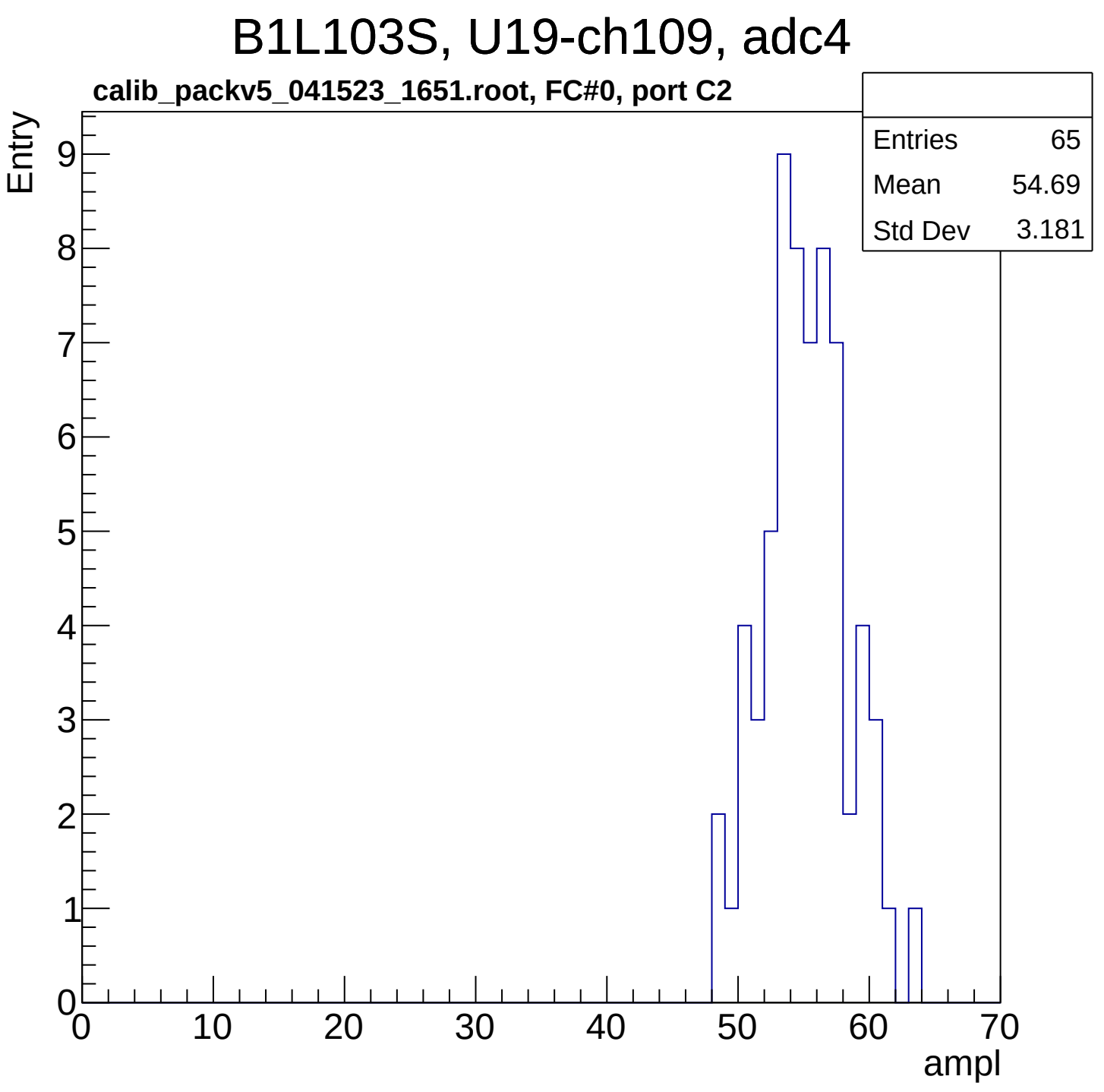
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch109, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 54.69
Std Dev 3.181
Entry
ampl
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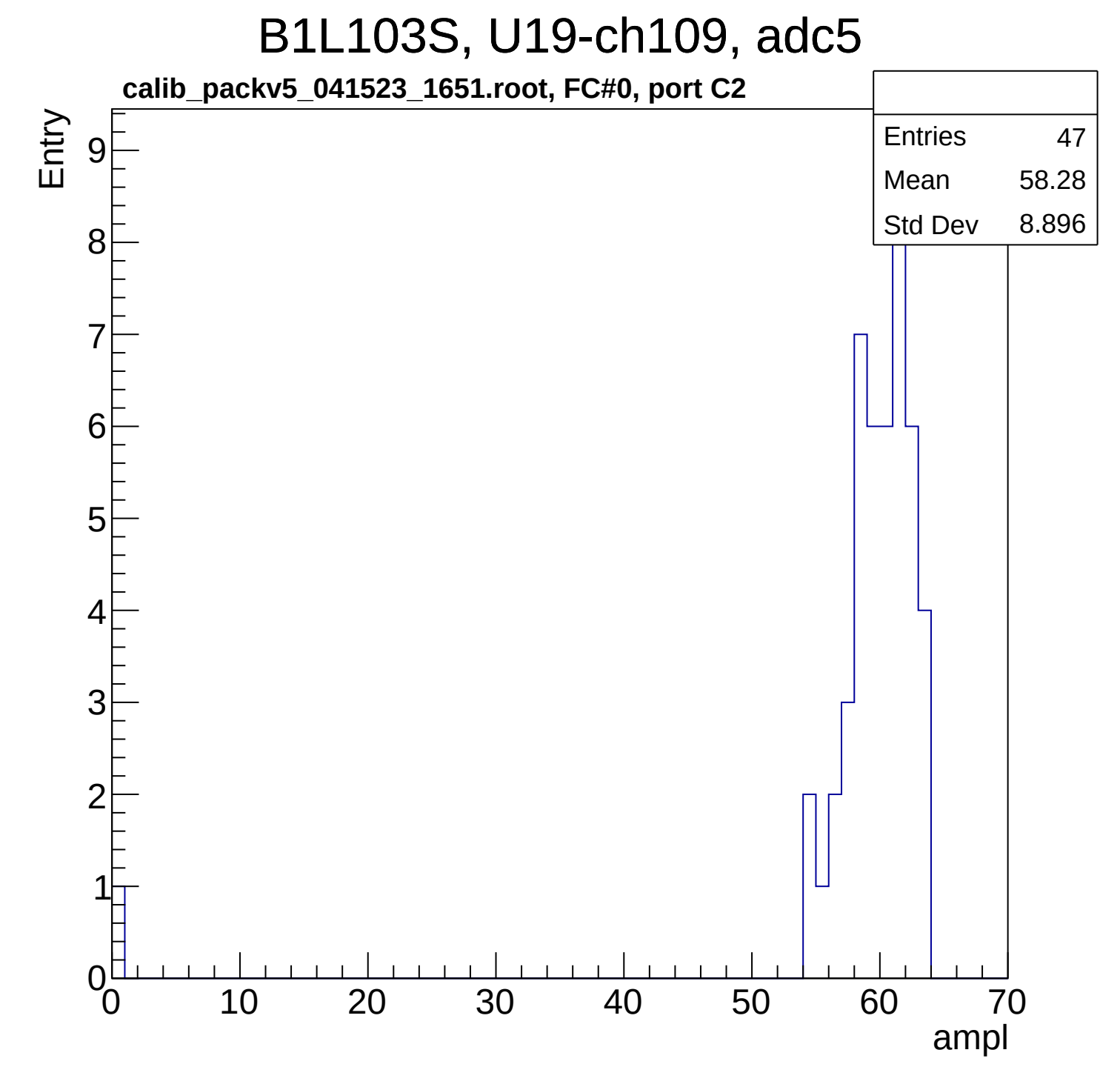
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch109, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 58.28
Std Dev 8.896
Entry
ampl
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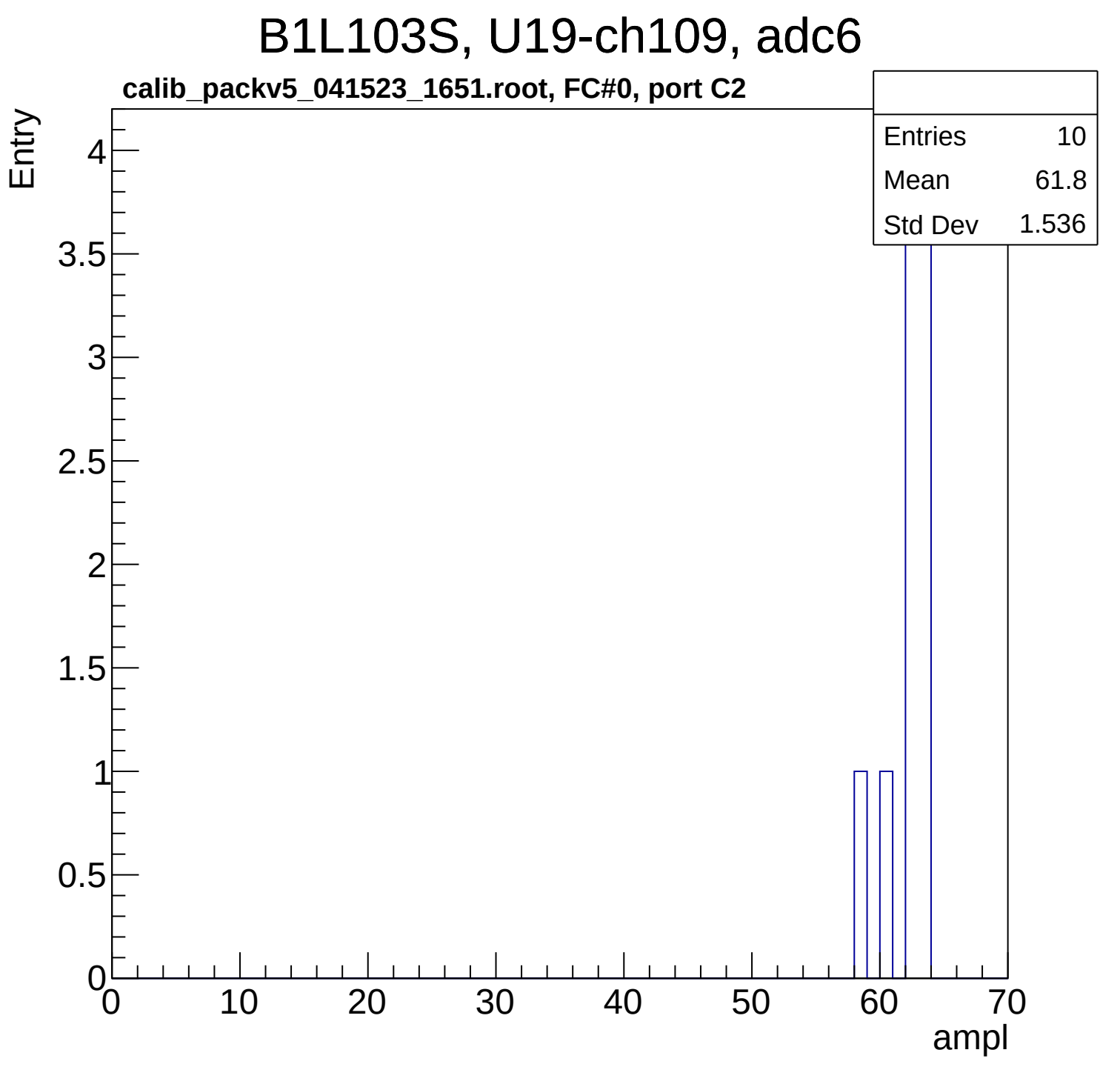
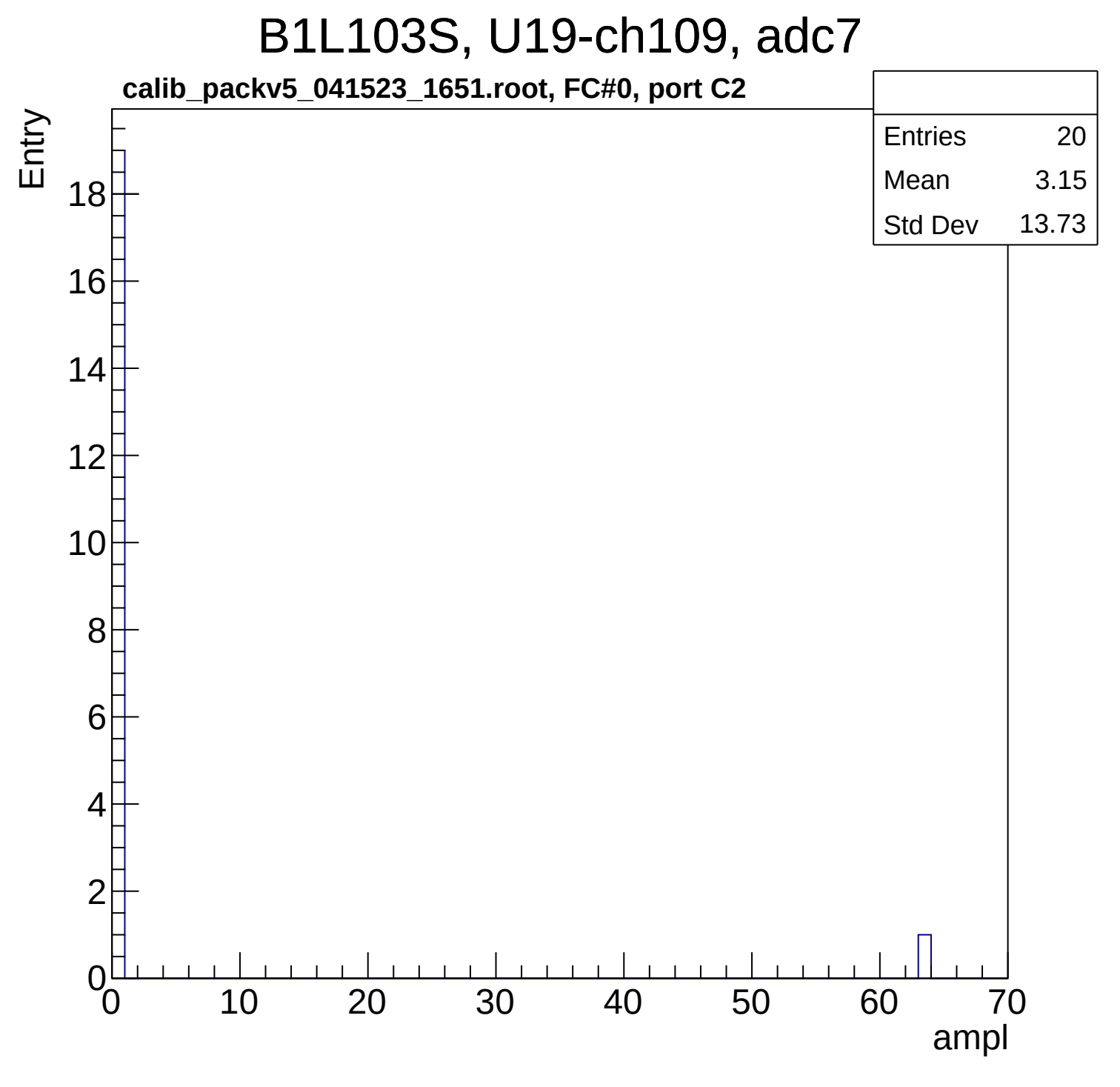
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch109, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61.8
Std Dev 1.536
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U19-ch109, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
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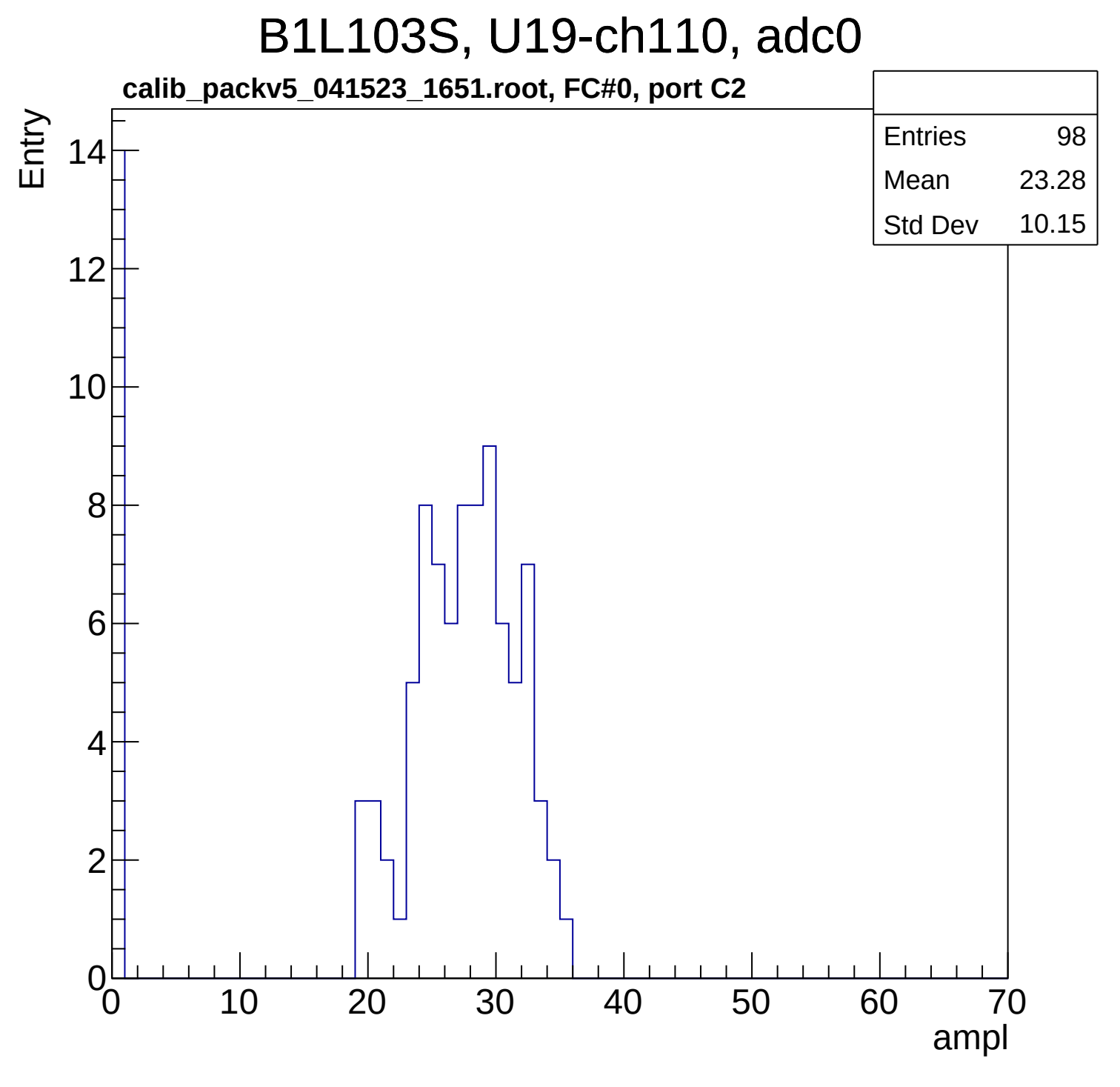
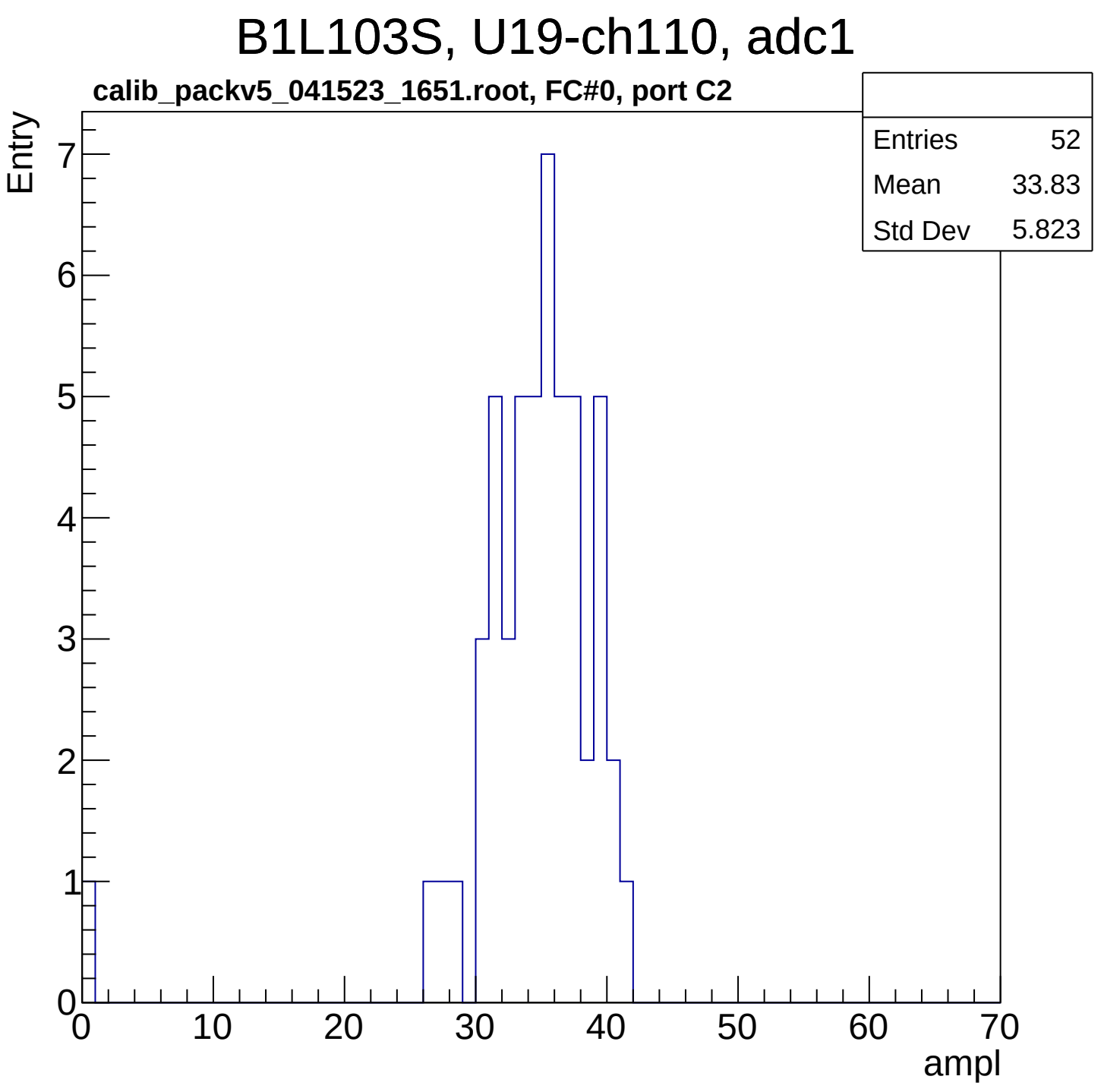
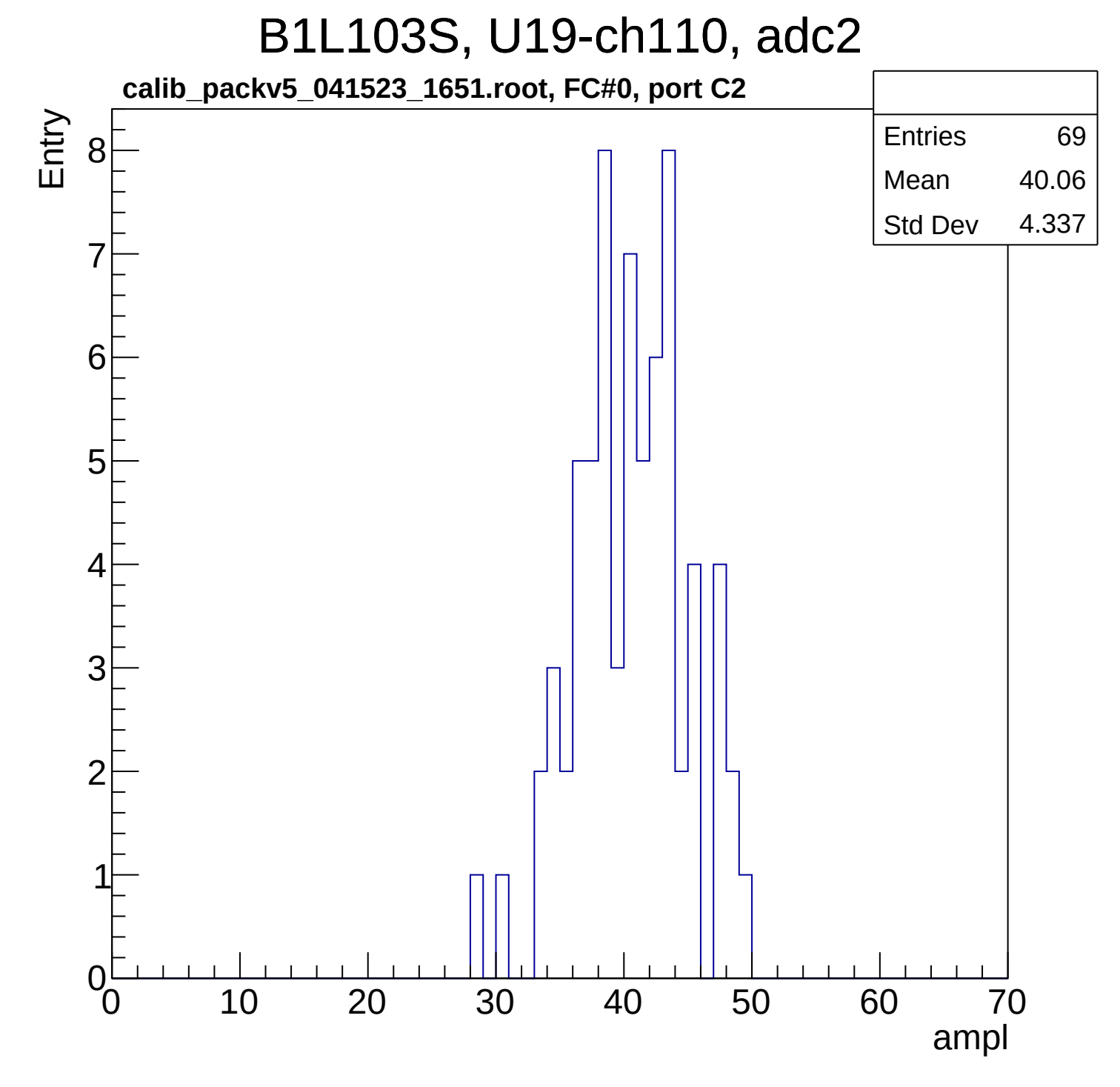
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch110, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 98
Mean 23.28
Std Dev 10.15
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U19-ch110, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 33.83
Std Dev 5.823
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch110, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 40.06
Std Dev 4.337
Entry
ampl
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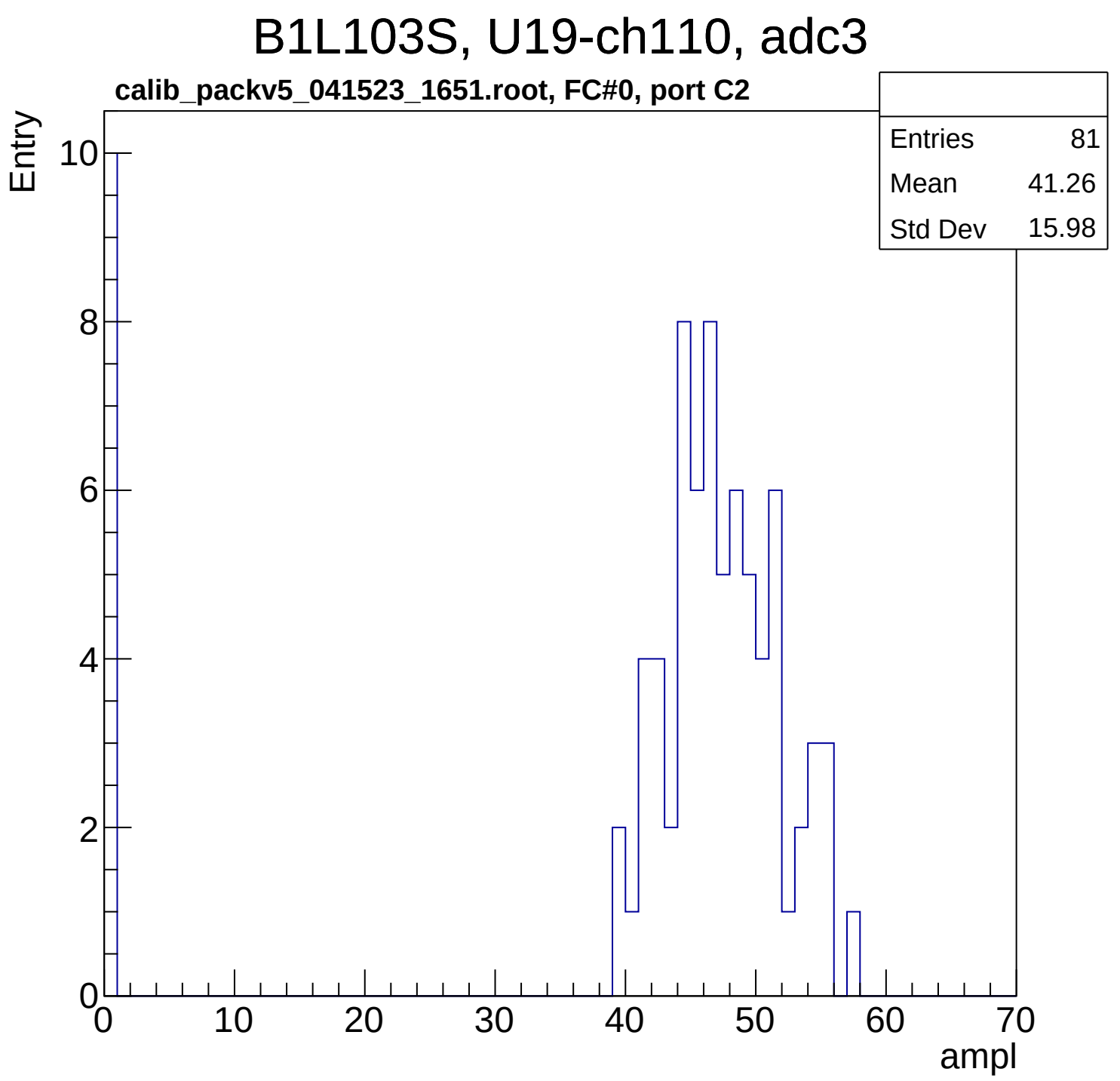
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch110, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 41.26
Std Dev 15.98
Entry
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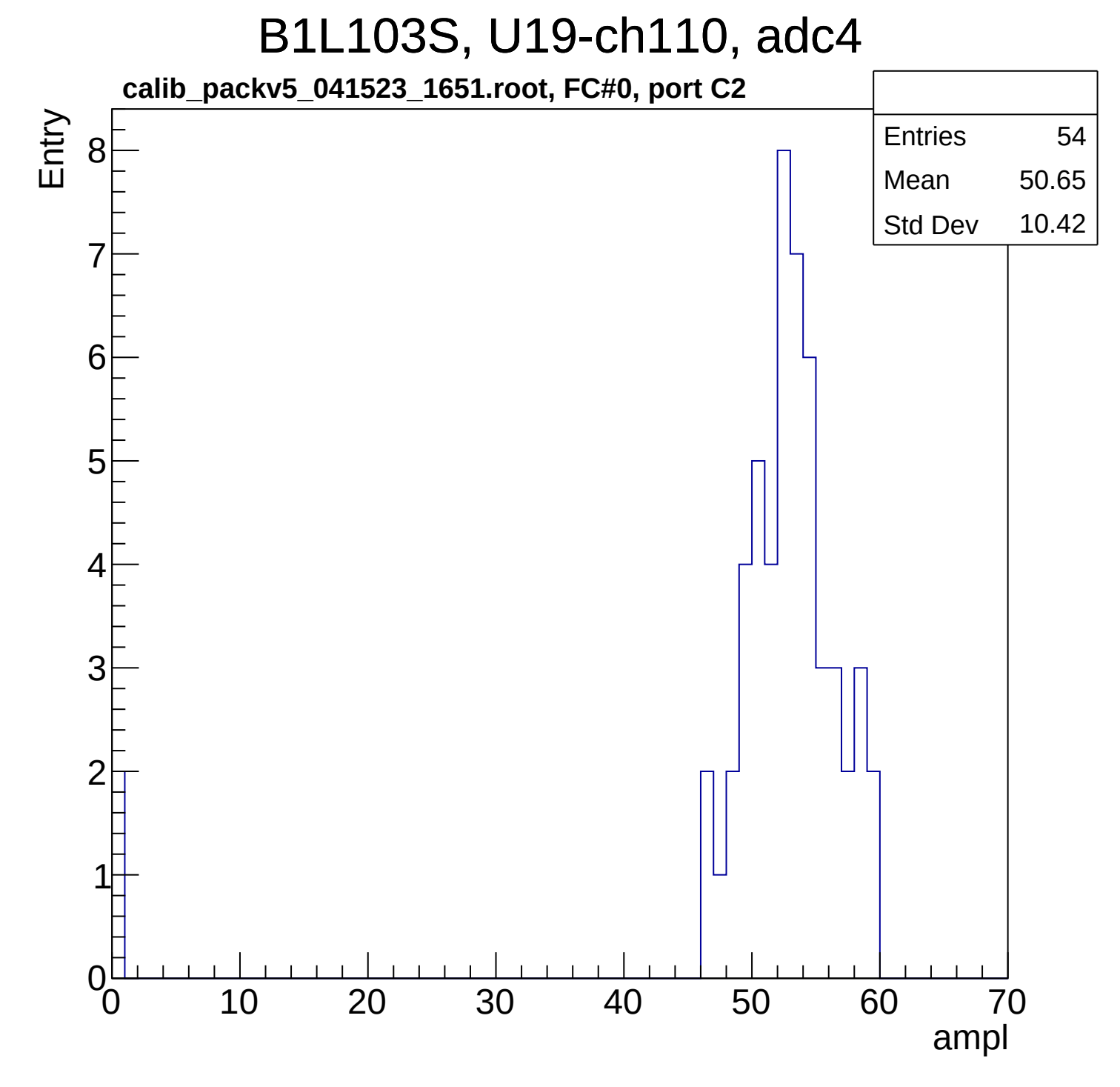
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch110, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 50.65
Std Dev 10.42
Entry
ampl
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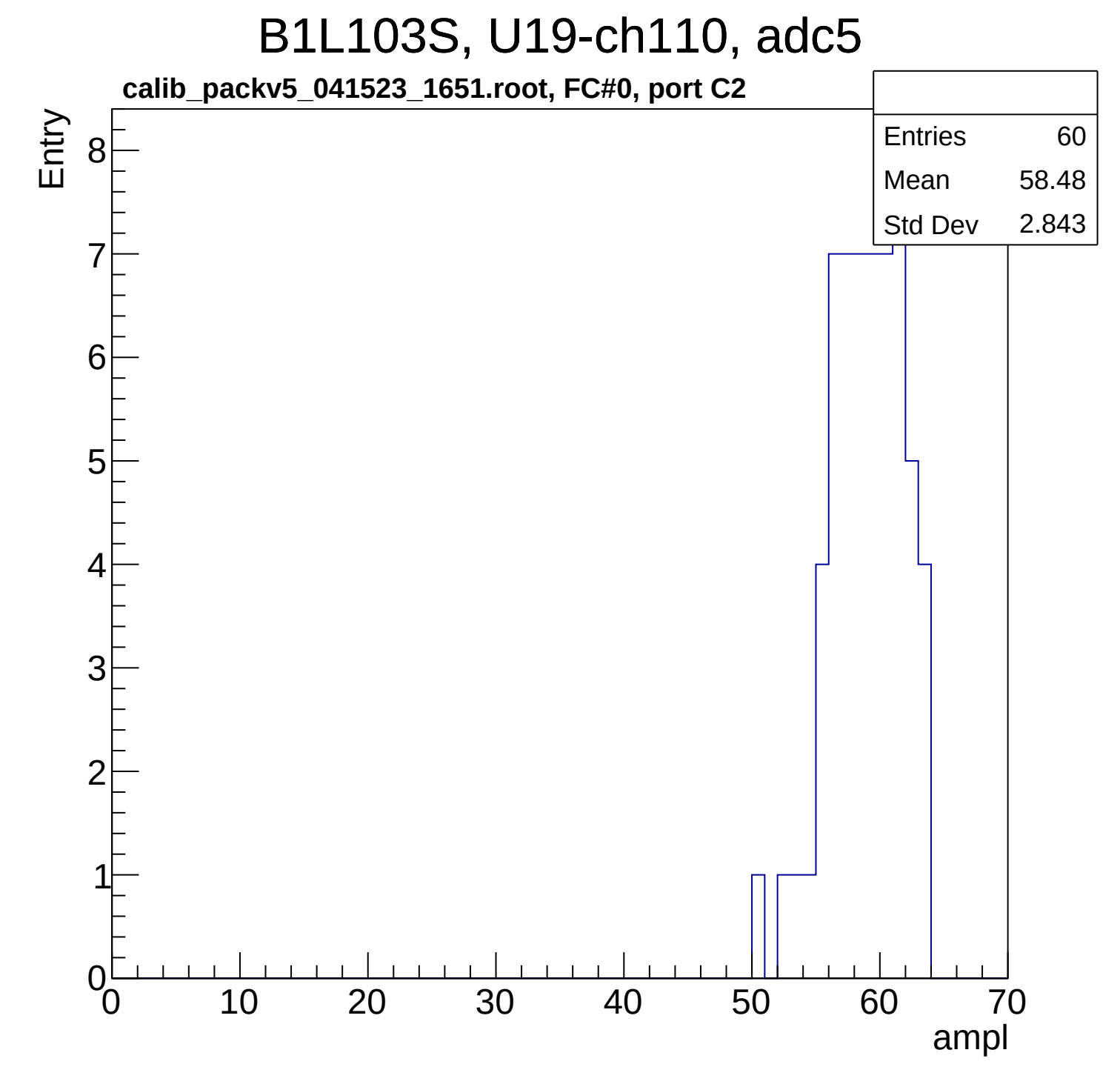
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch110, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 58.48
Std Dev 2.843
Entry
ampl
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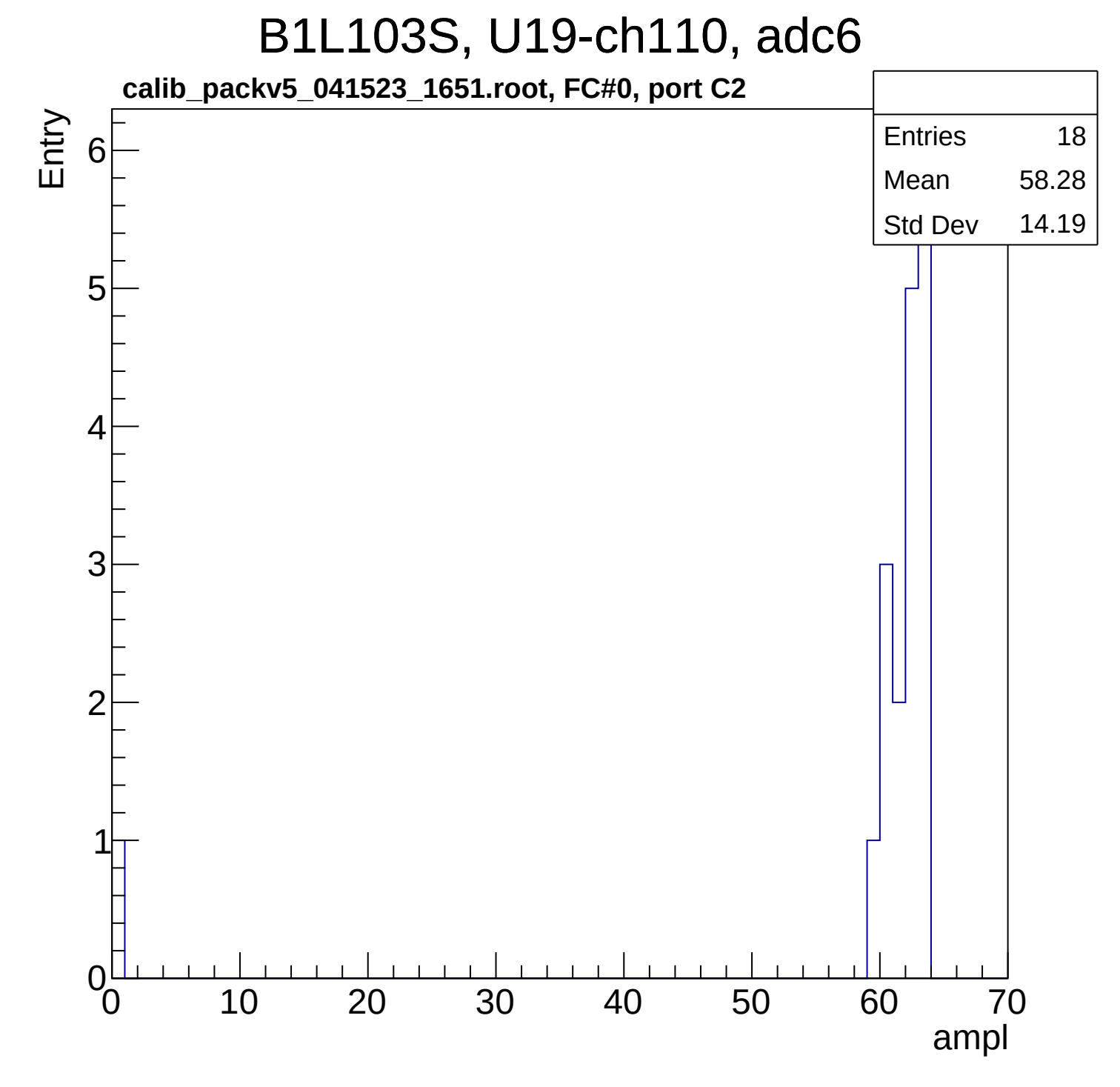
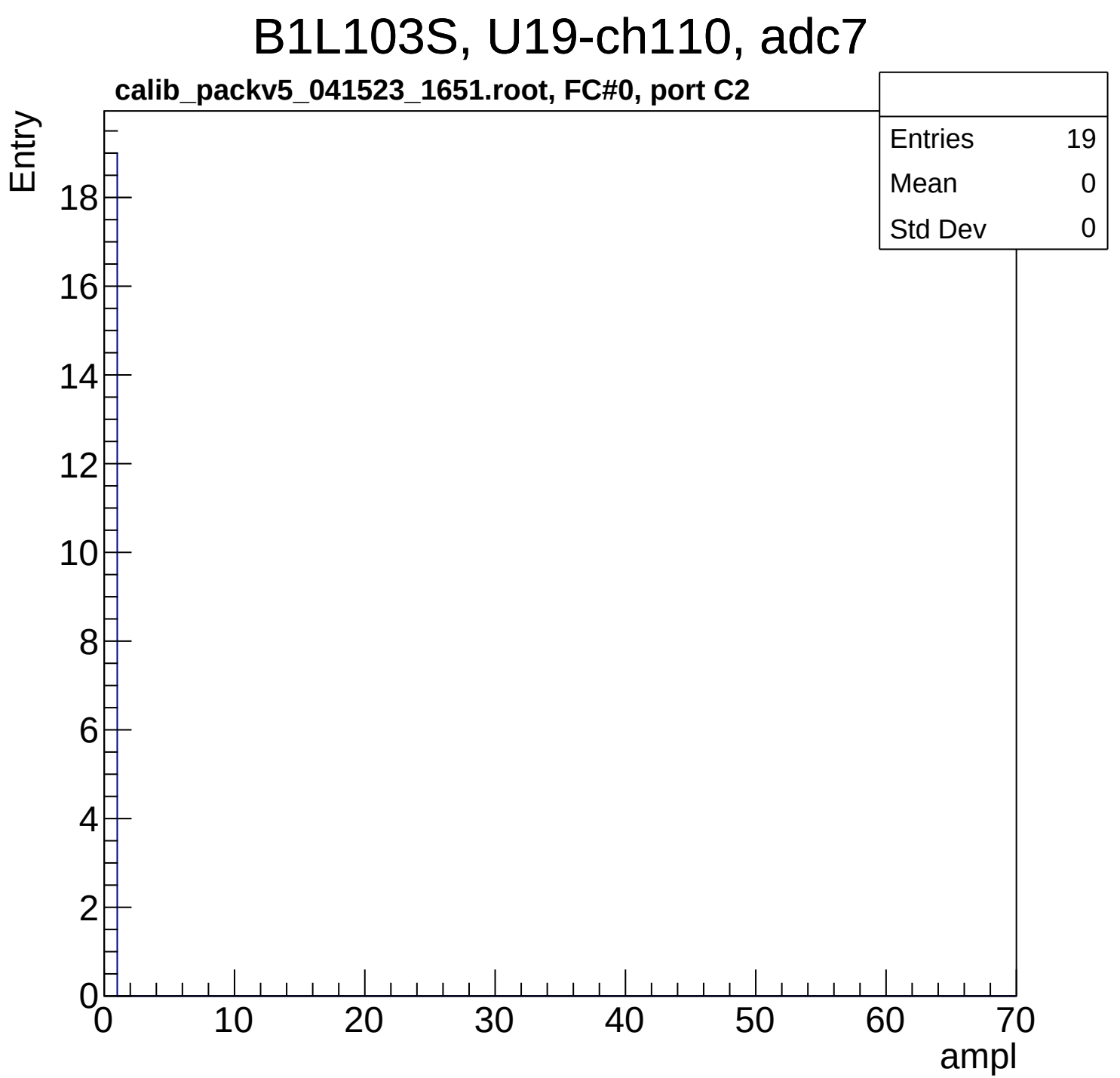
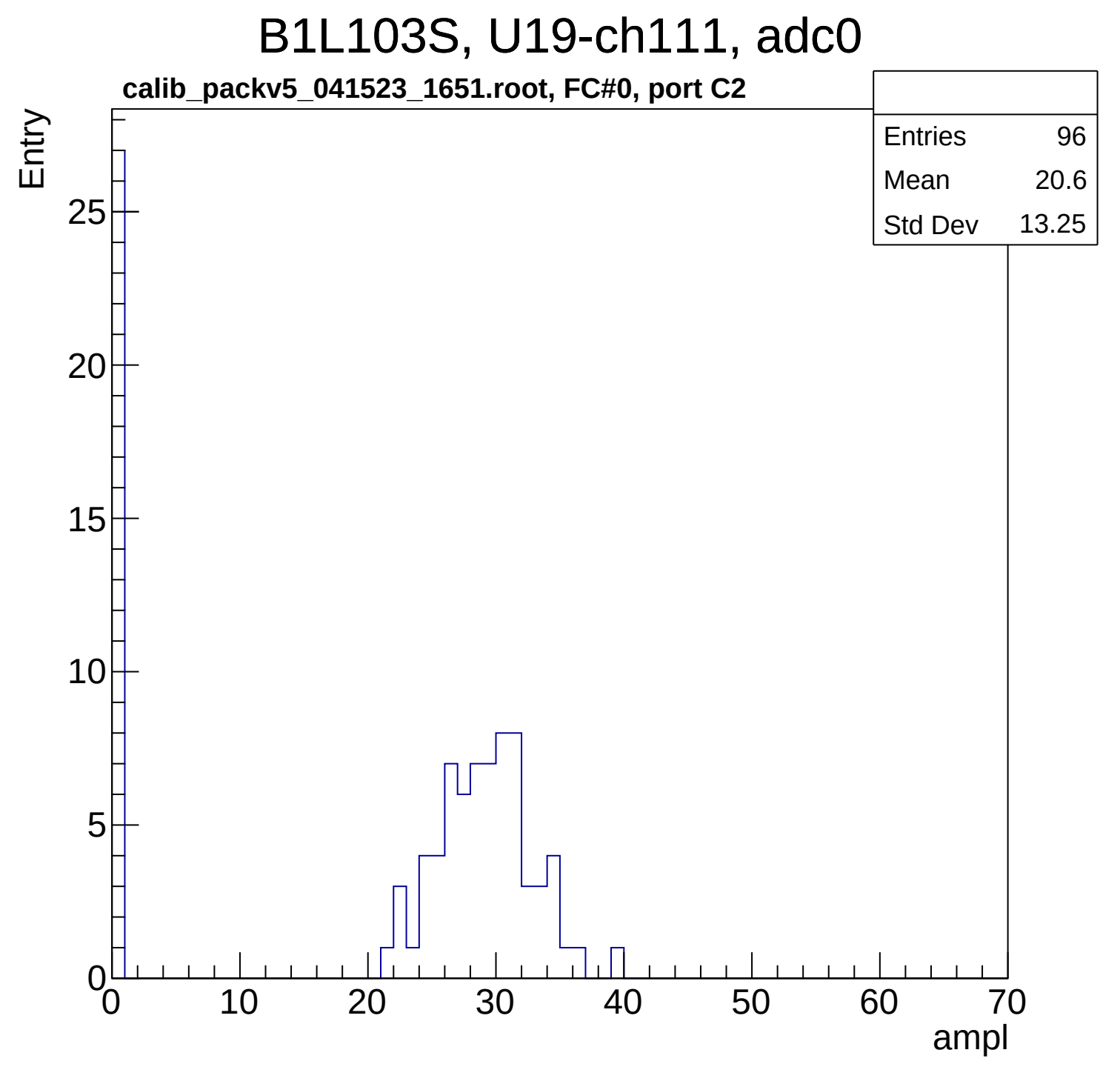
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch110, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 58.28
Std Dev 14.19
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch110, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch111, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 96
Mean 20.6
Std Dev 13.25
Entry
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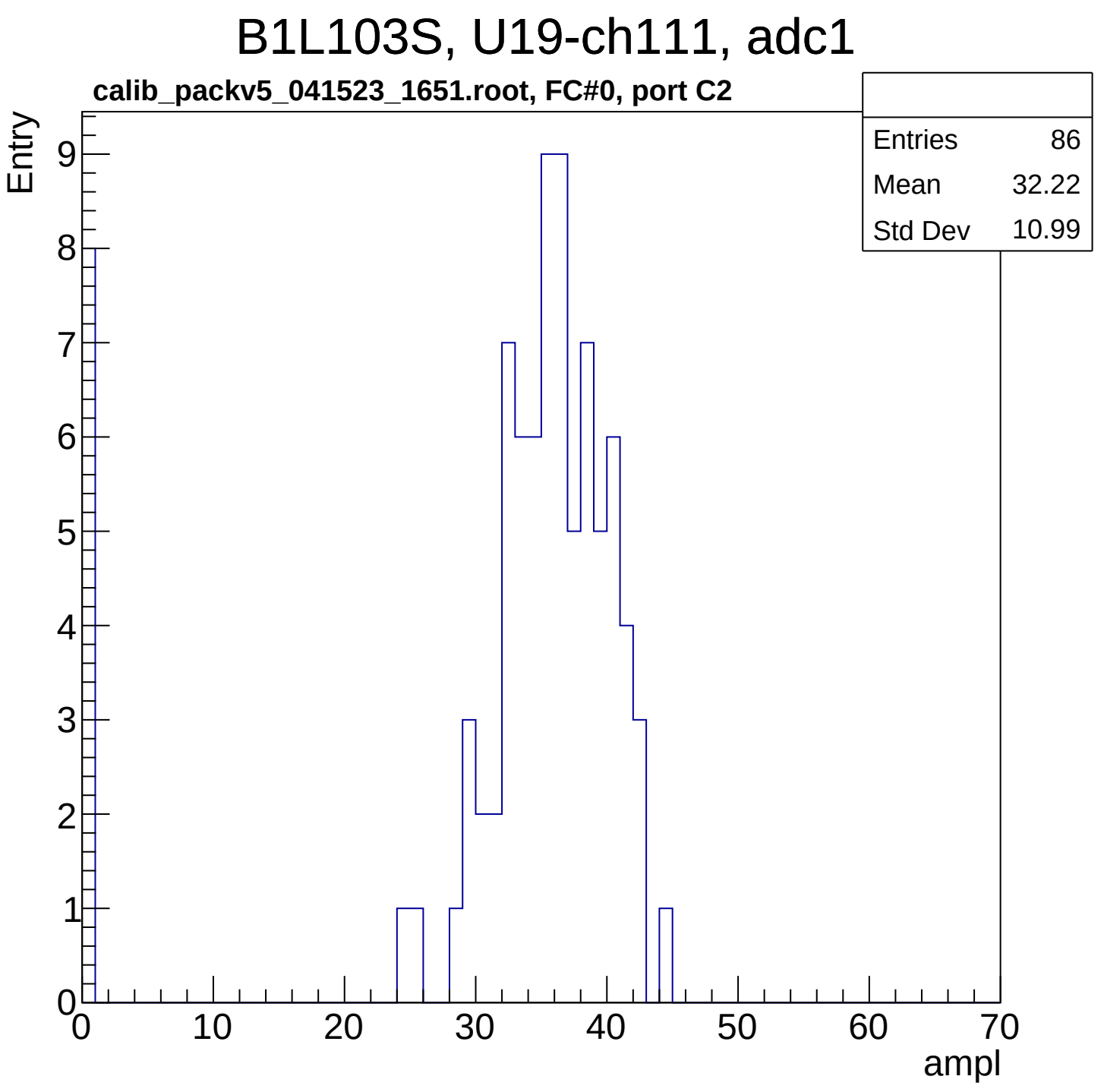
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch111, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 32.22
Std Dev 10.99
Entry
ampl
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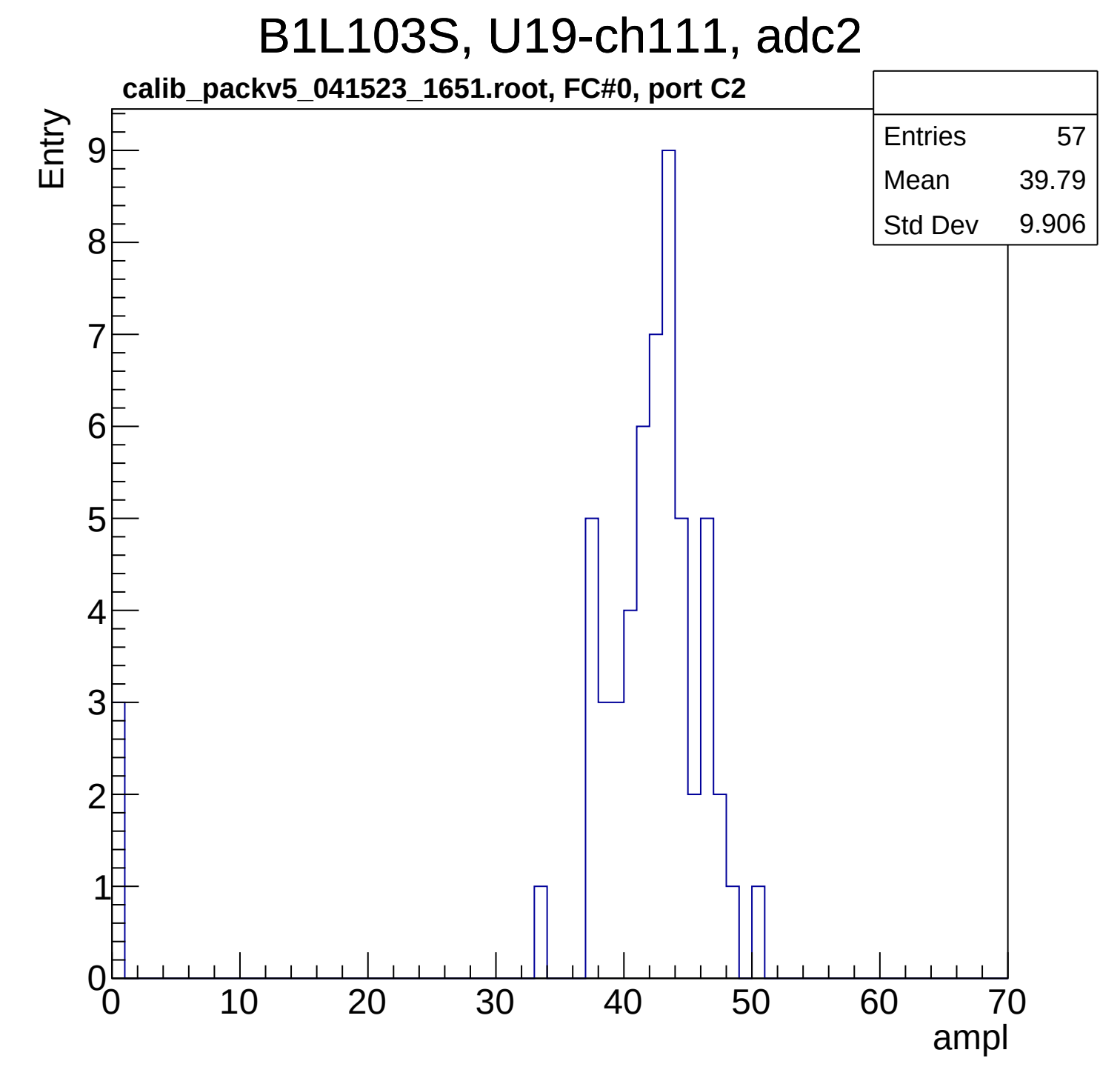
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch111, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 39.79
Std Dev 9.906
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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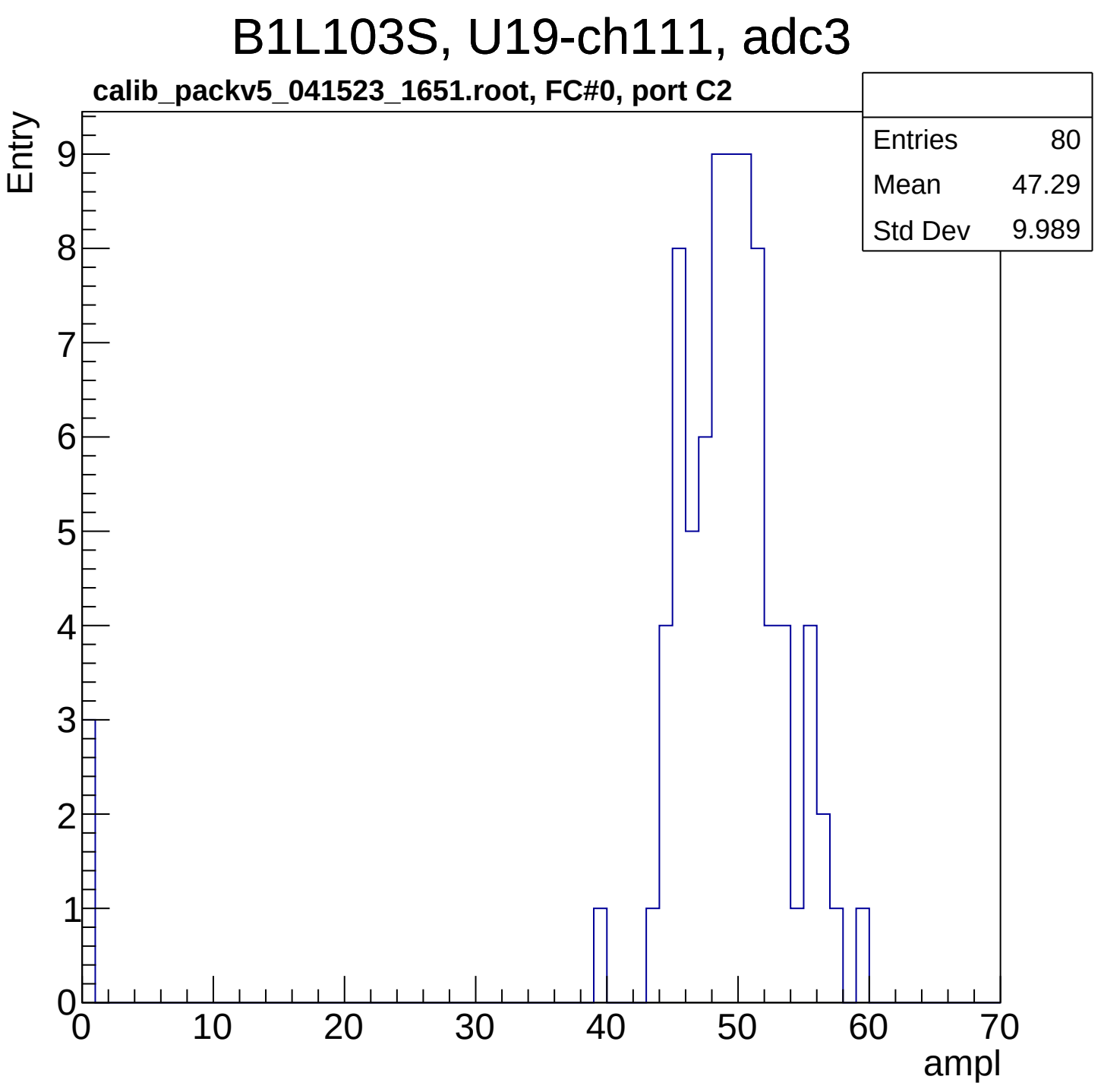
B1L103S, U19-ch111, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 47.29
Std Dev 9.989
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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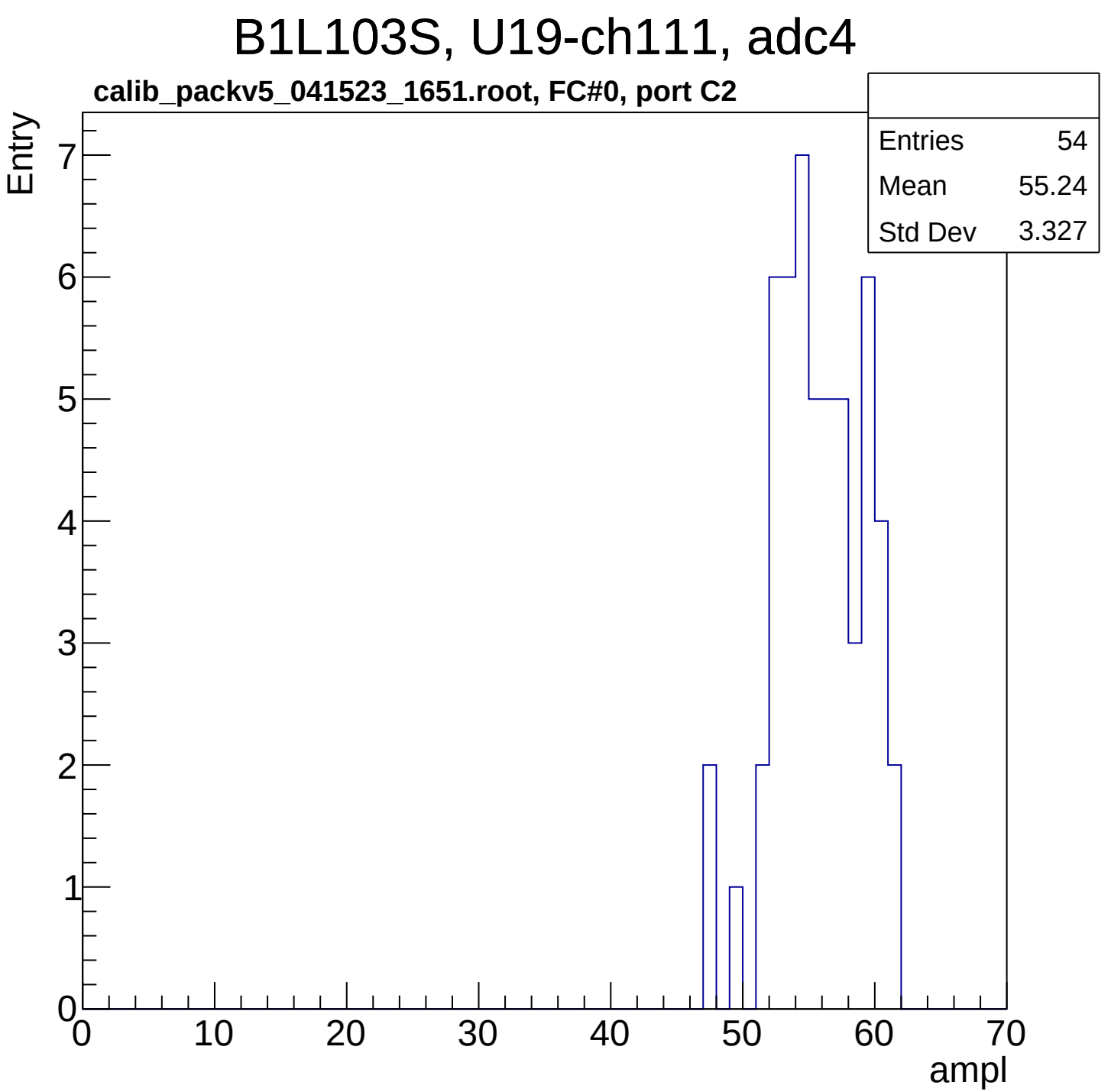
40
50
60
70


B1L103S, U19-ch111, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 55.24
Std Dev 3.327
Entry
ampl
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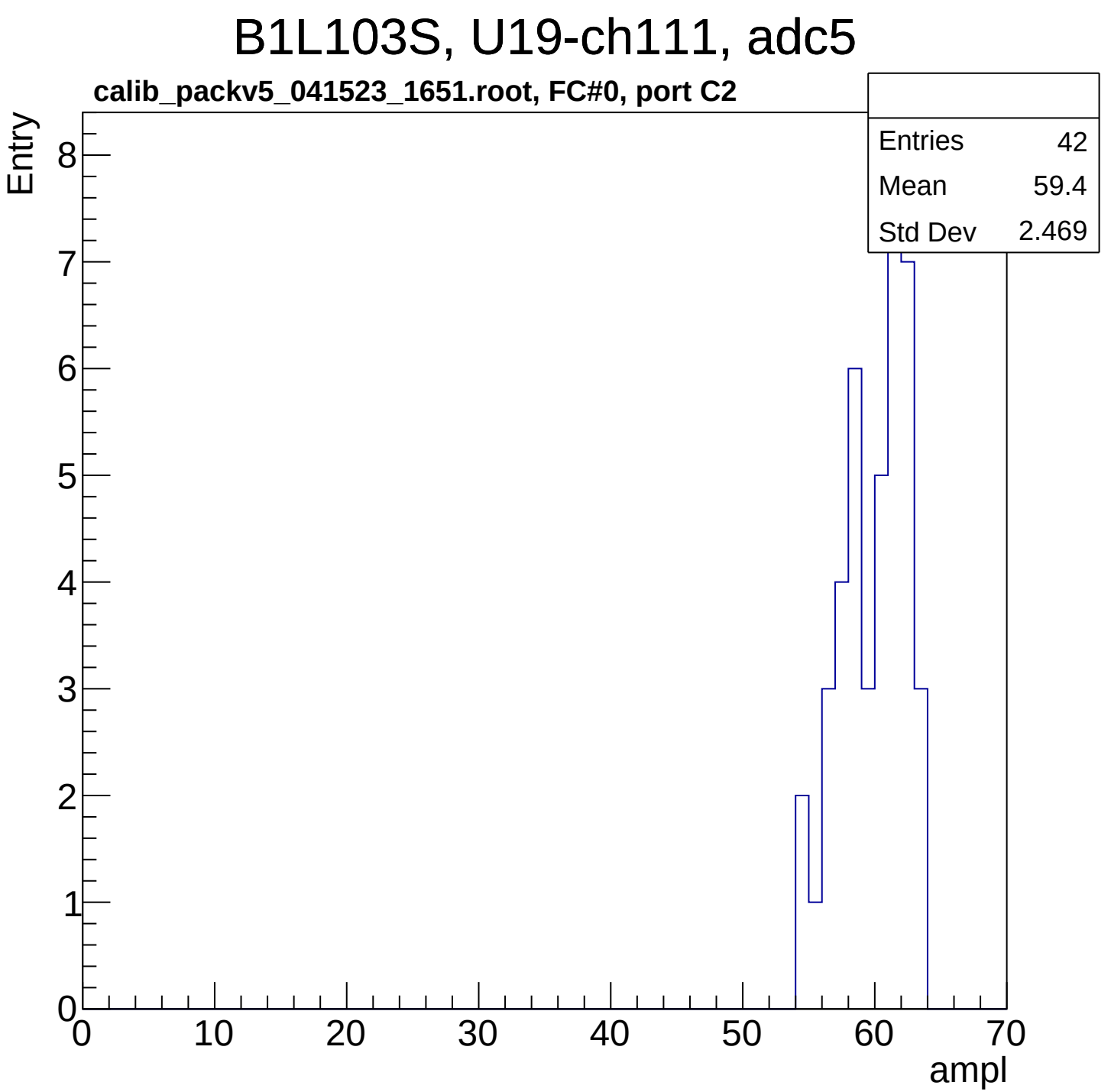
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch111, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 59.4
Std Dev 2.469
Entry
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2
3
4
5
6
7
8
0
10
20
30
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50
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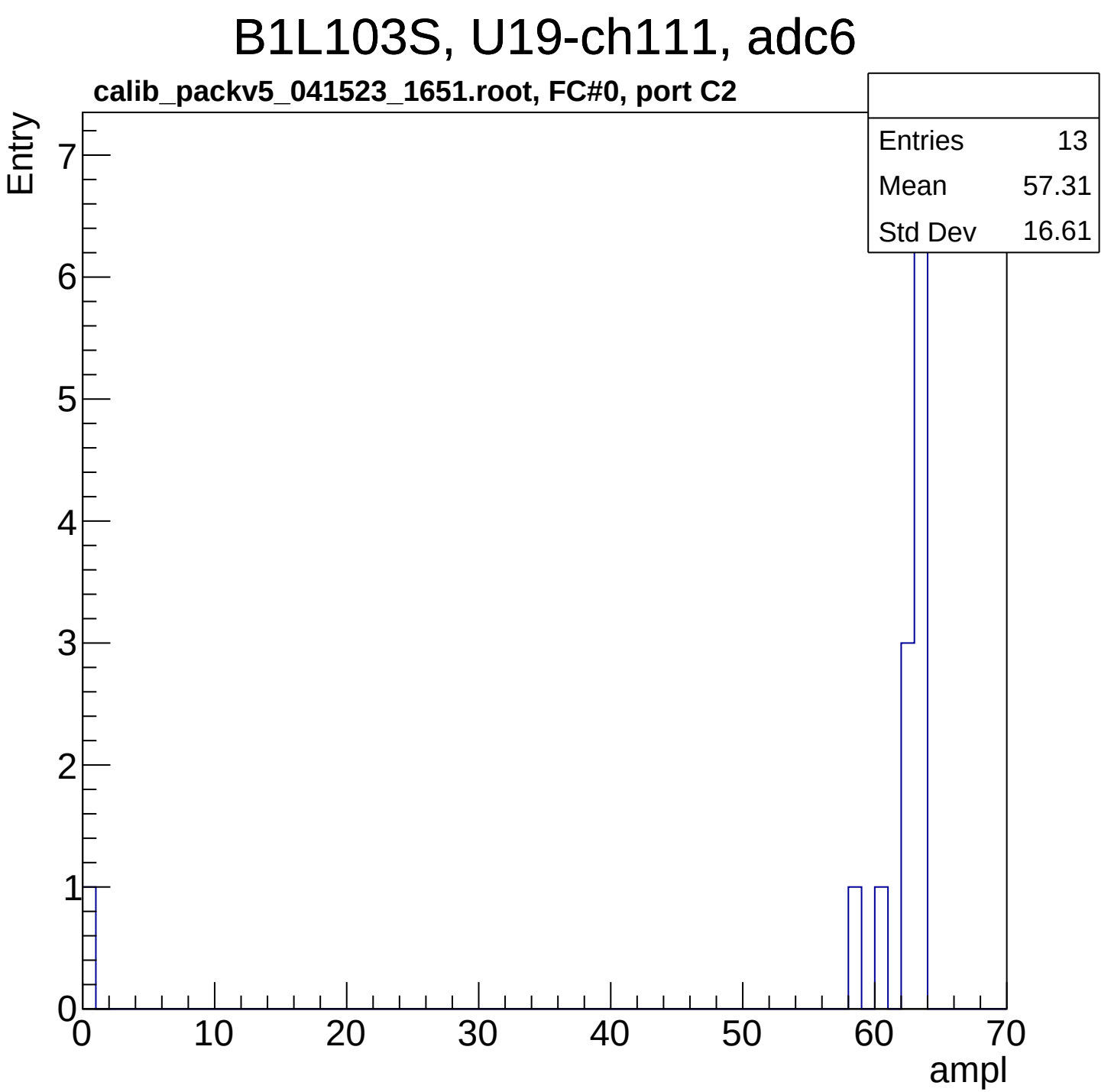
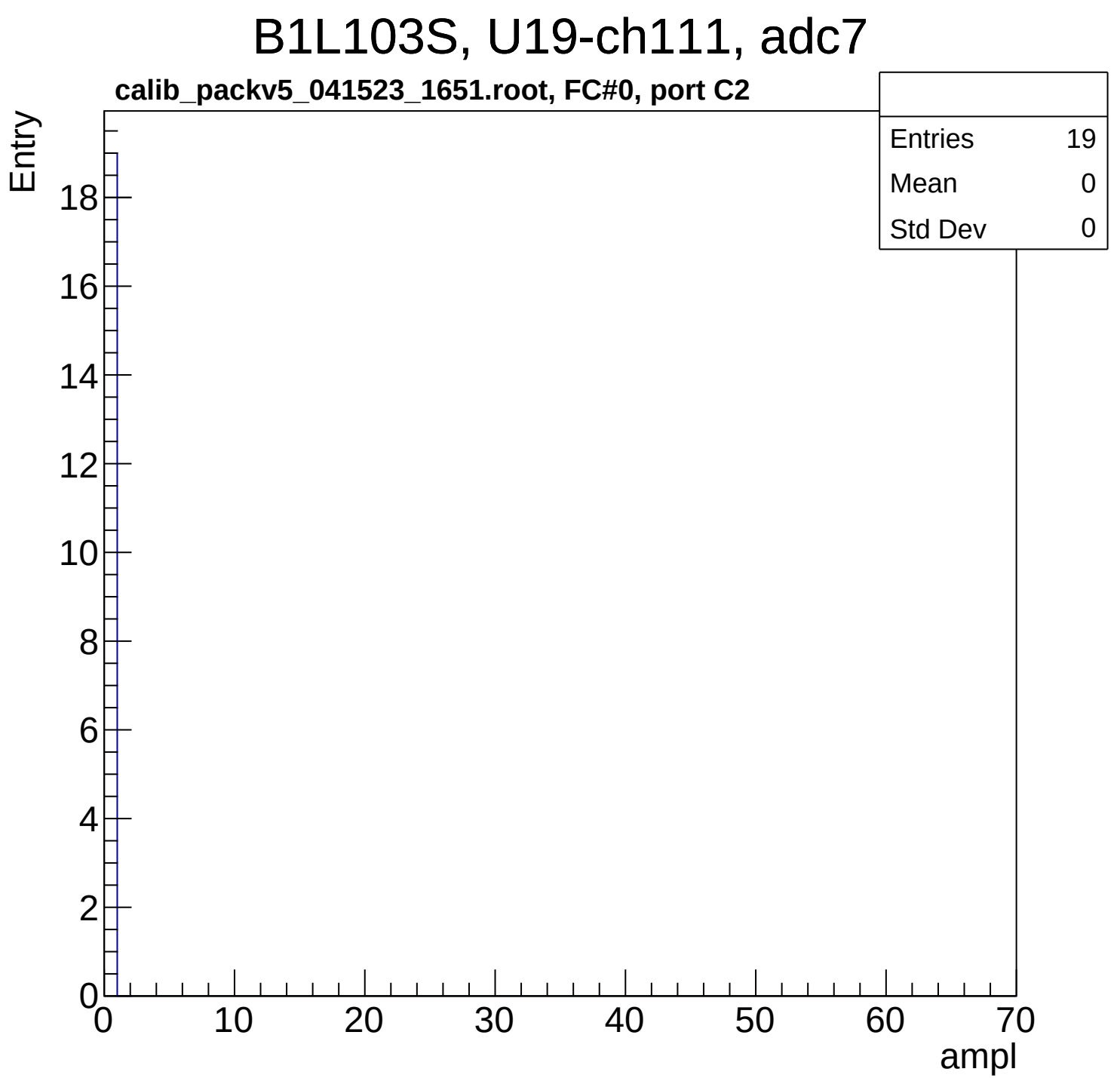
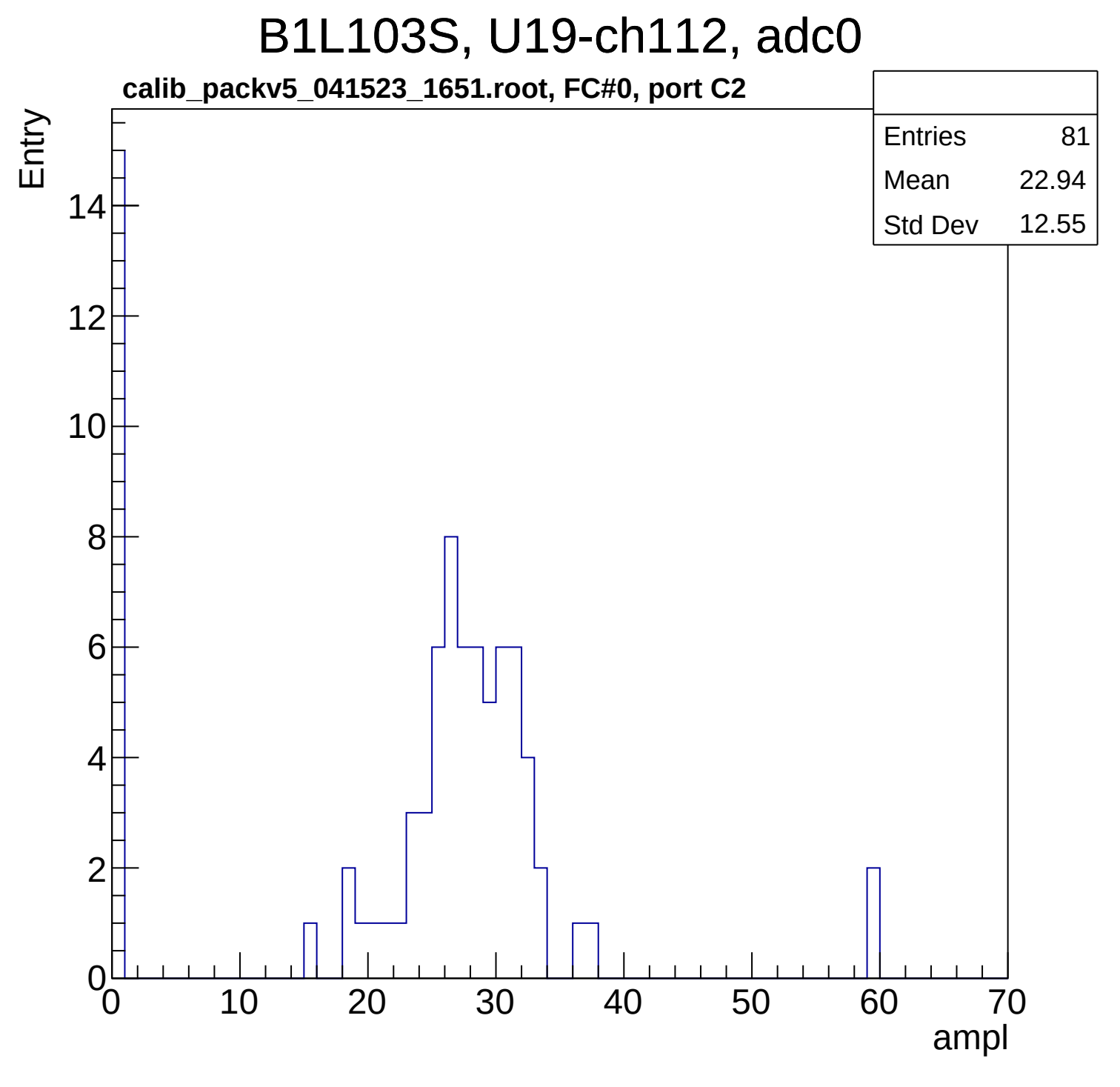
70
ampl


B1L103S, U19-ch111, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 57.31
Std Dev 16.61
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch111, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch112, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 22.94
Std Dev 12.55
Entry
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2
4
6
8
10
12
14
0
10
20
30
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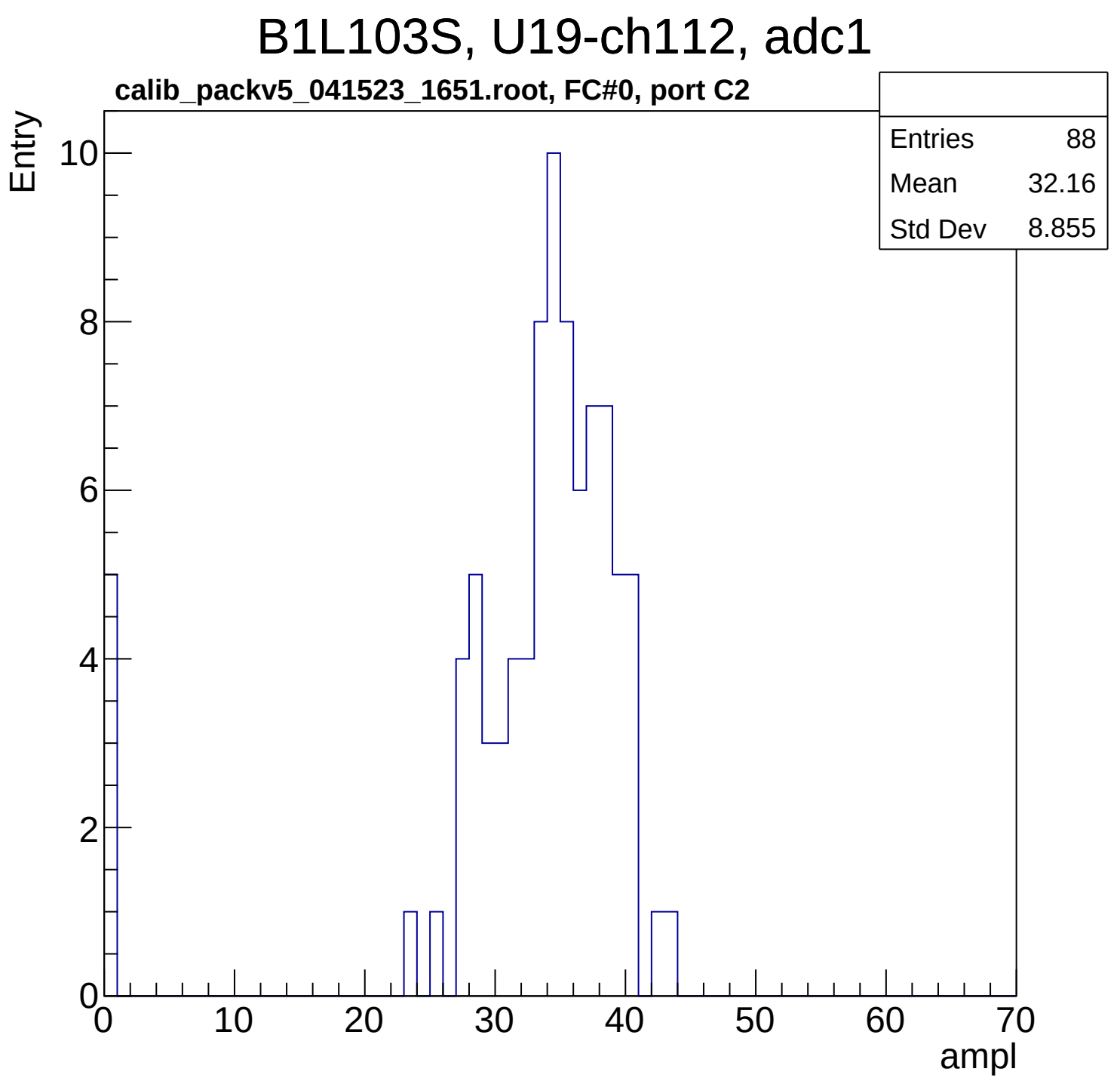
50
60
70
ampl


B1L103S, U19-ch112, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 32.16
Std Dev 8.855
Entry
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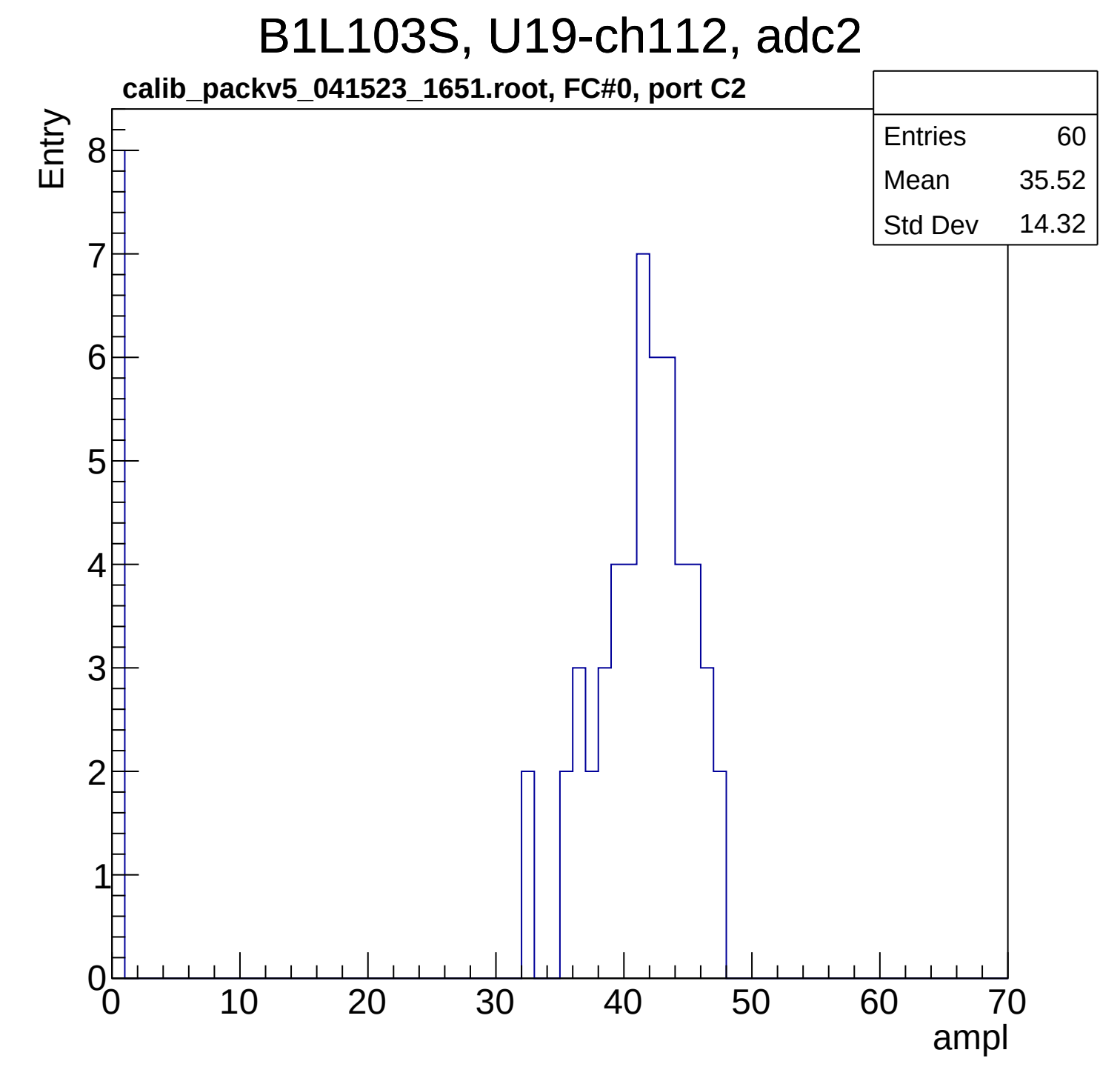
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch112, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 35.52
Std Dev 14.32
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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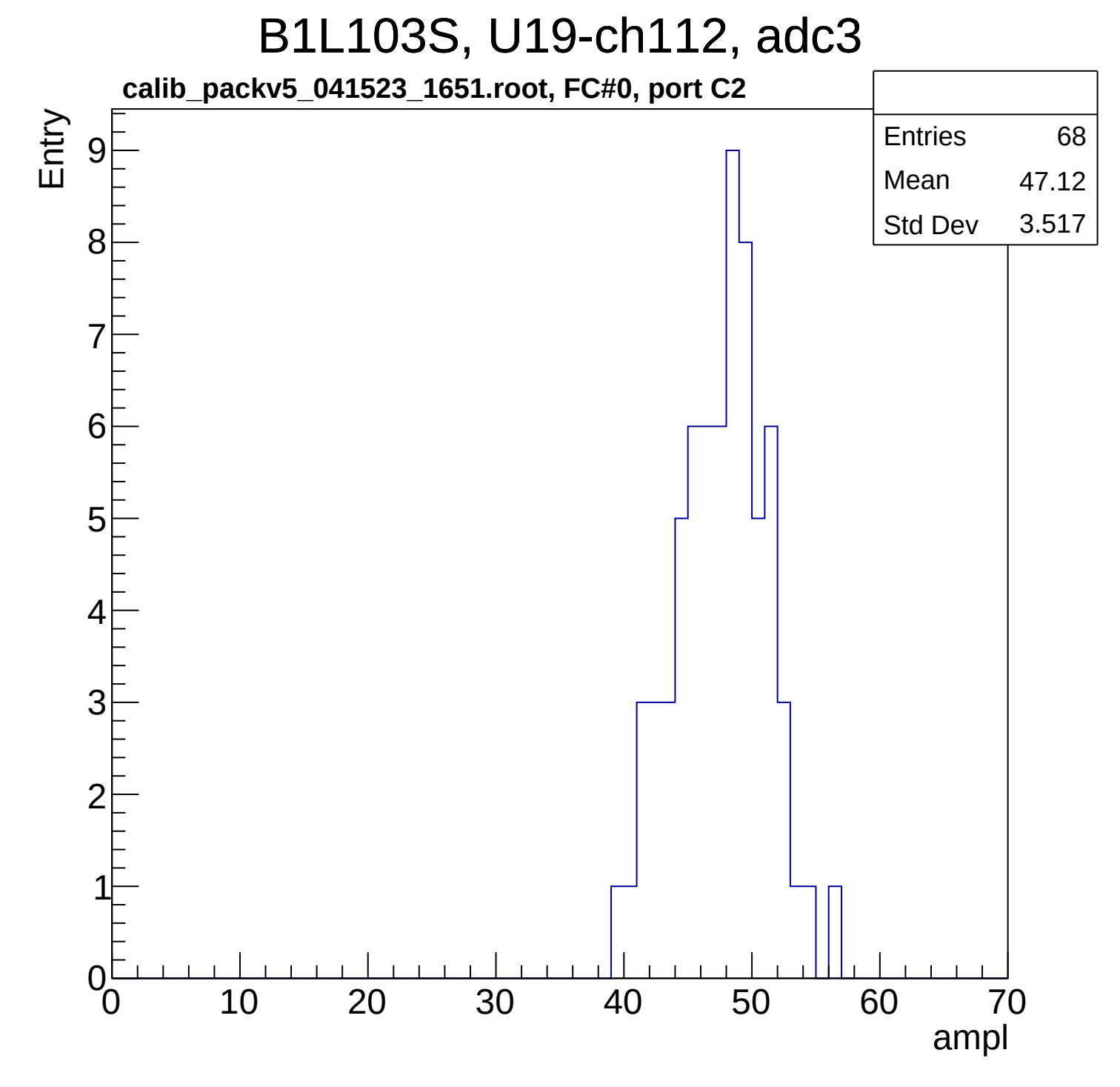
B1L103S, U19-ch112, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 47.12
Std Dev 3.517
Entry
ampl
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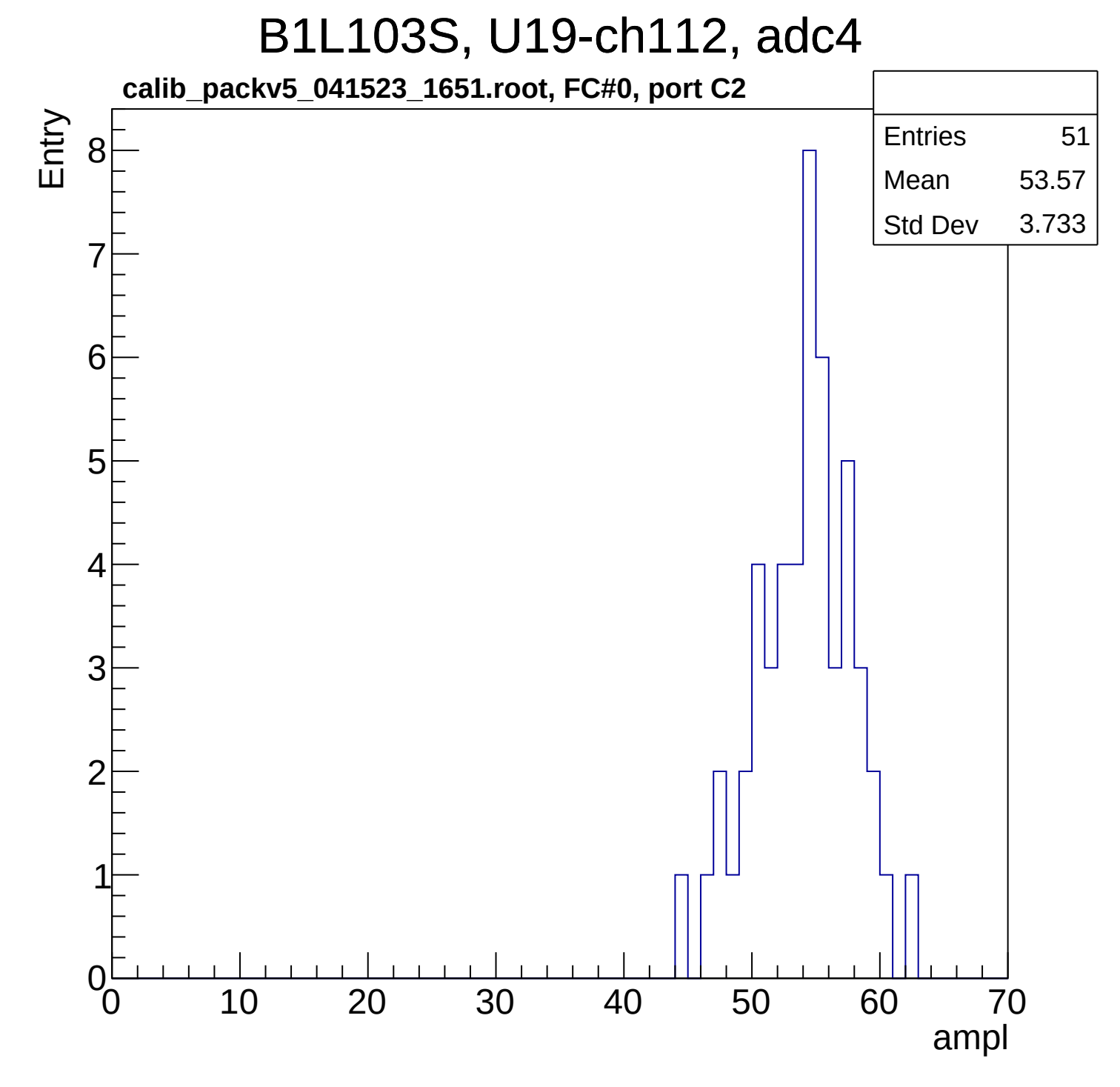
B1L103S, U19-ch112, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 53.57
Std Dev 3.733
Entry
ampl
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7
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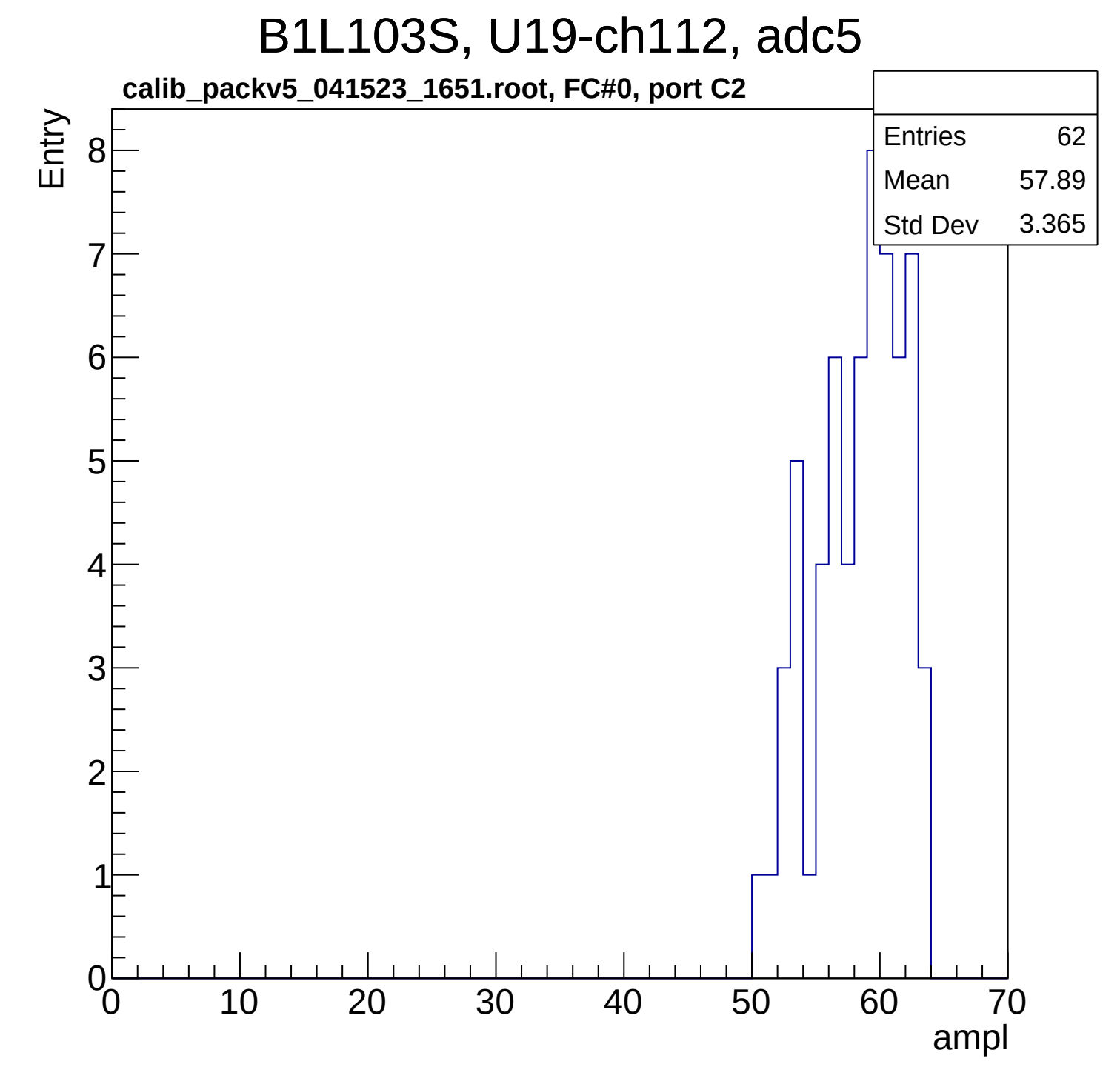
B1L103S, U19-ch112, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 57.89
Std Dev 3.365
Entry
ampl
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7
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60
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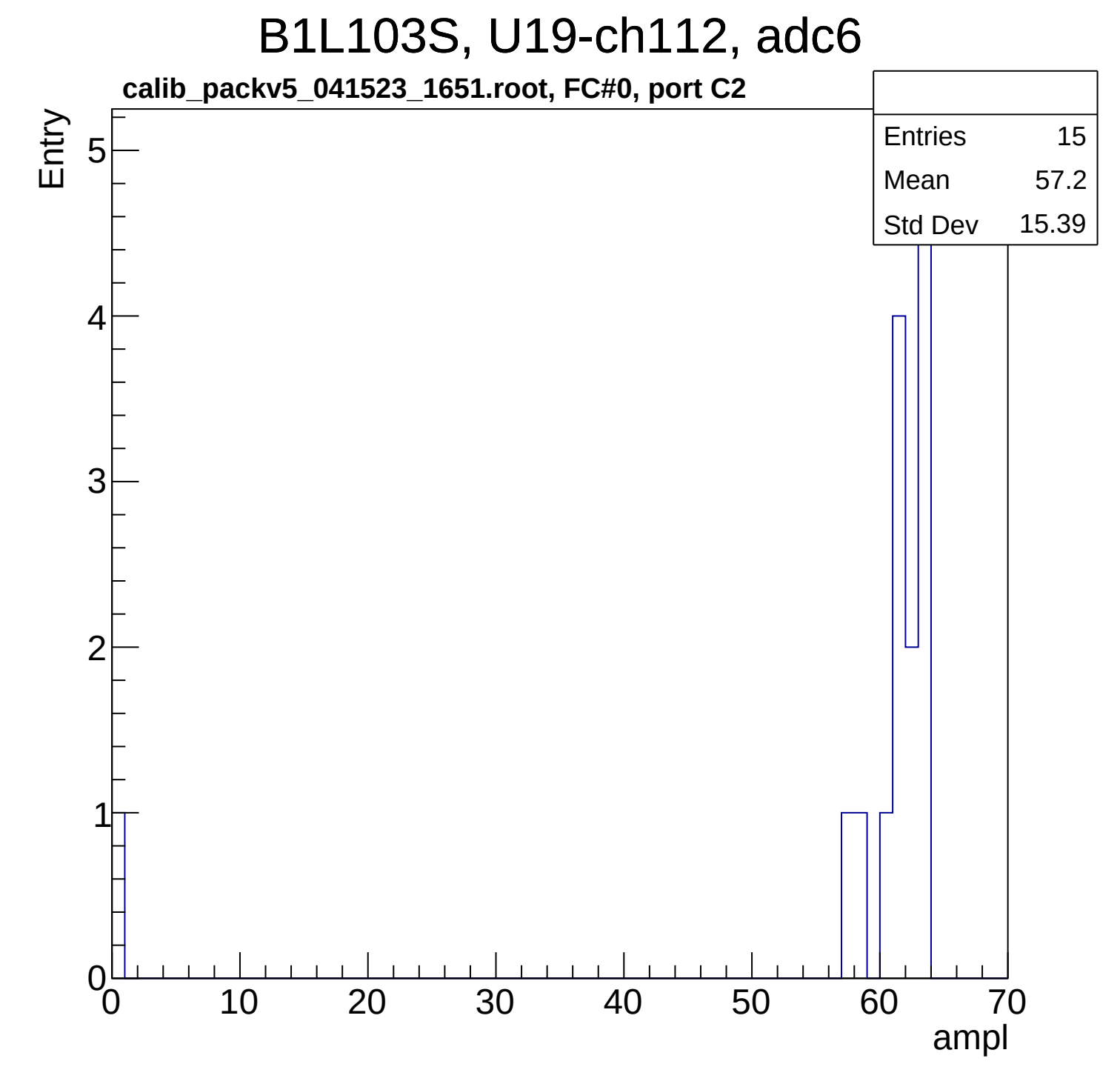
B1L103S, U19-ch112, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 57.2
Std Dev 15.39
Entry
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4
5
0
10
20
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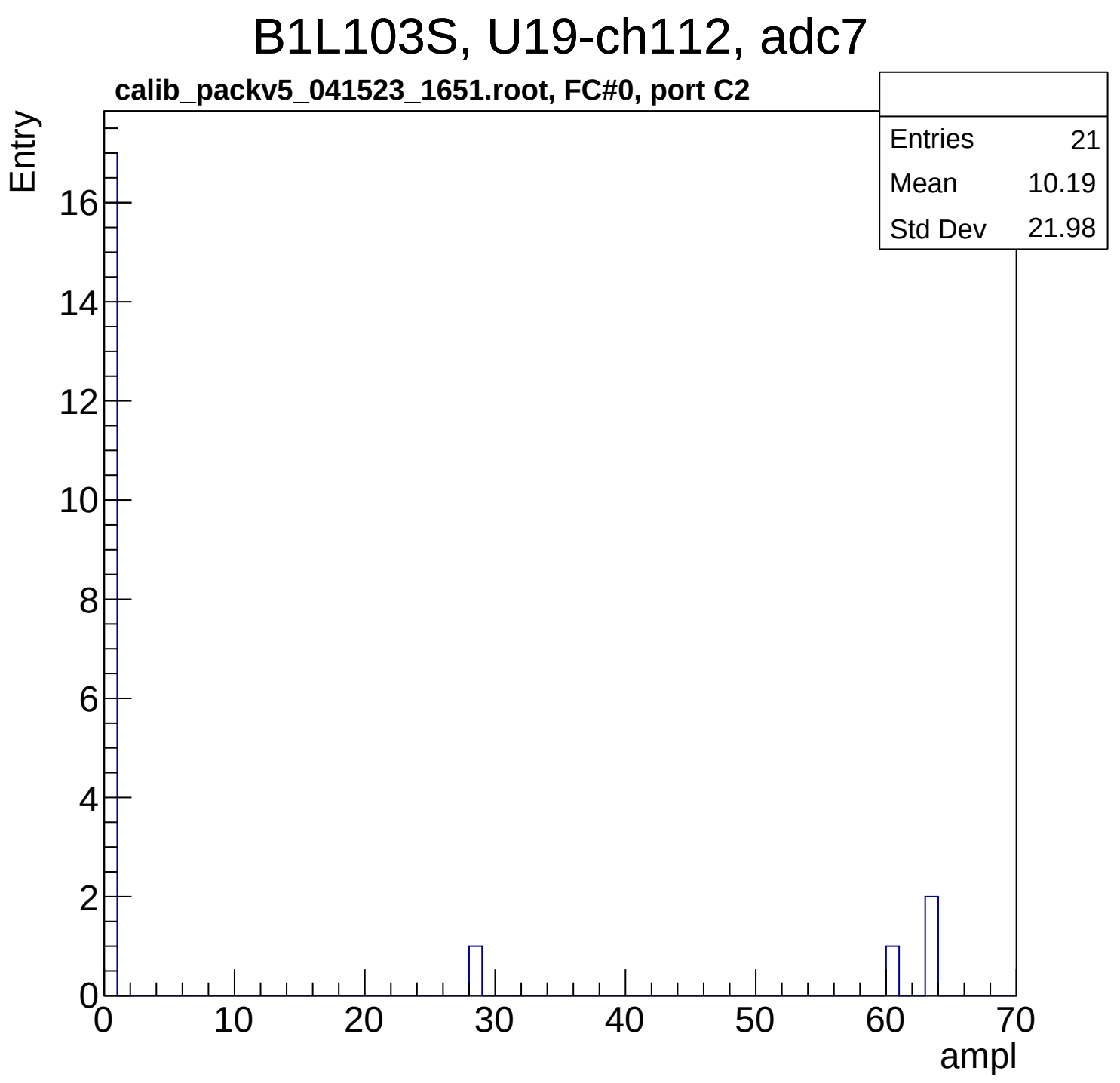
40
50
60
70
ampl


B1L103S, U19-ch112, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 10.19
Std Dev 21.98
Entry
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4
6
8
10
12
14
16
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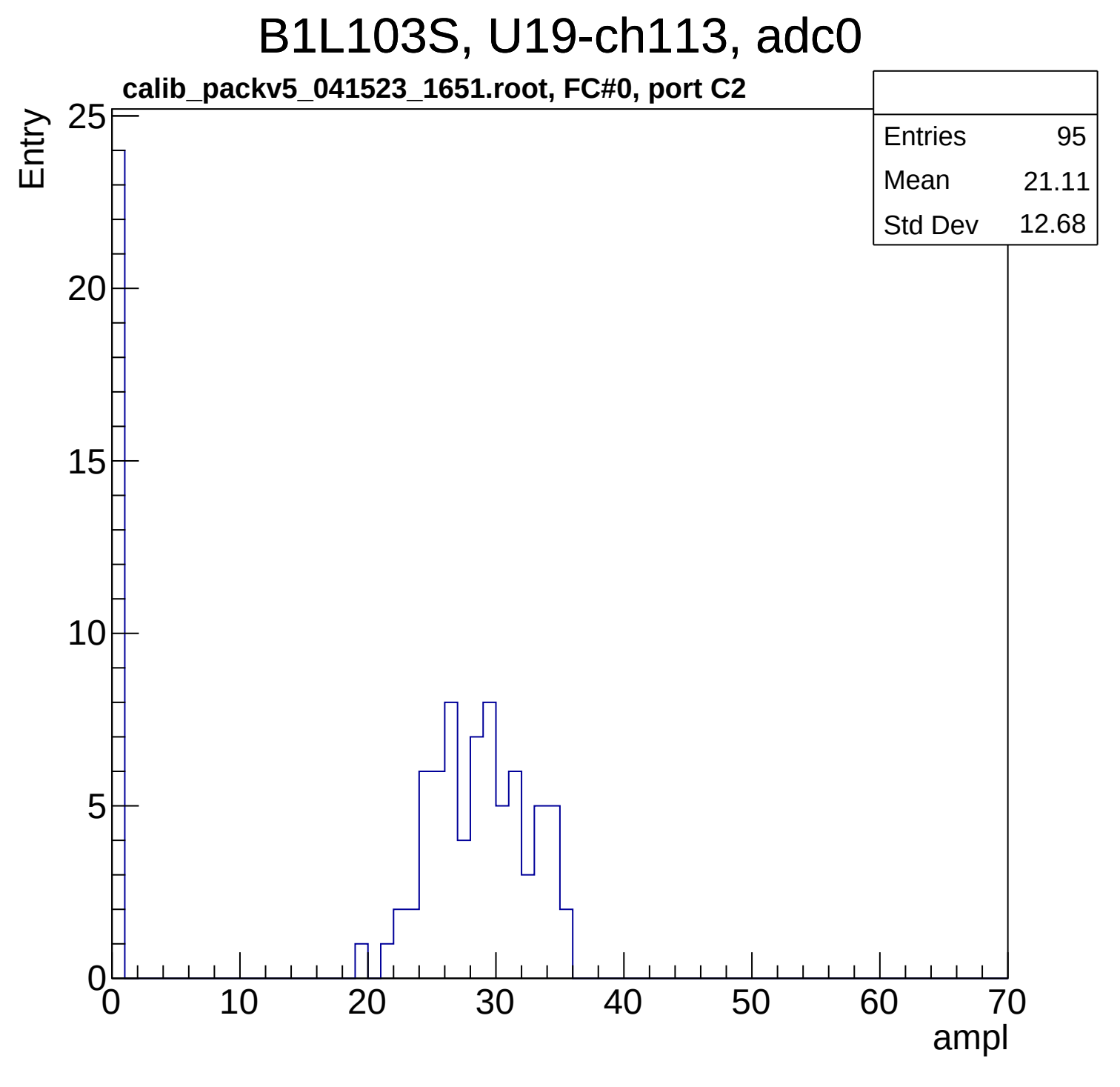
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch113, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 21.11
Std Dev 12.68
Entry
ampl
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10
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0
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40
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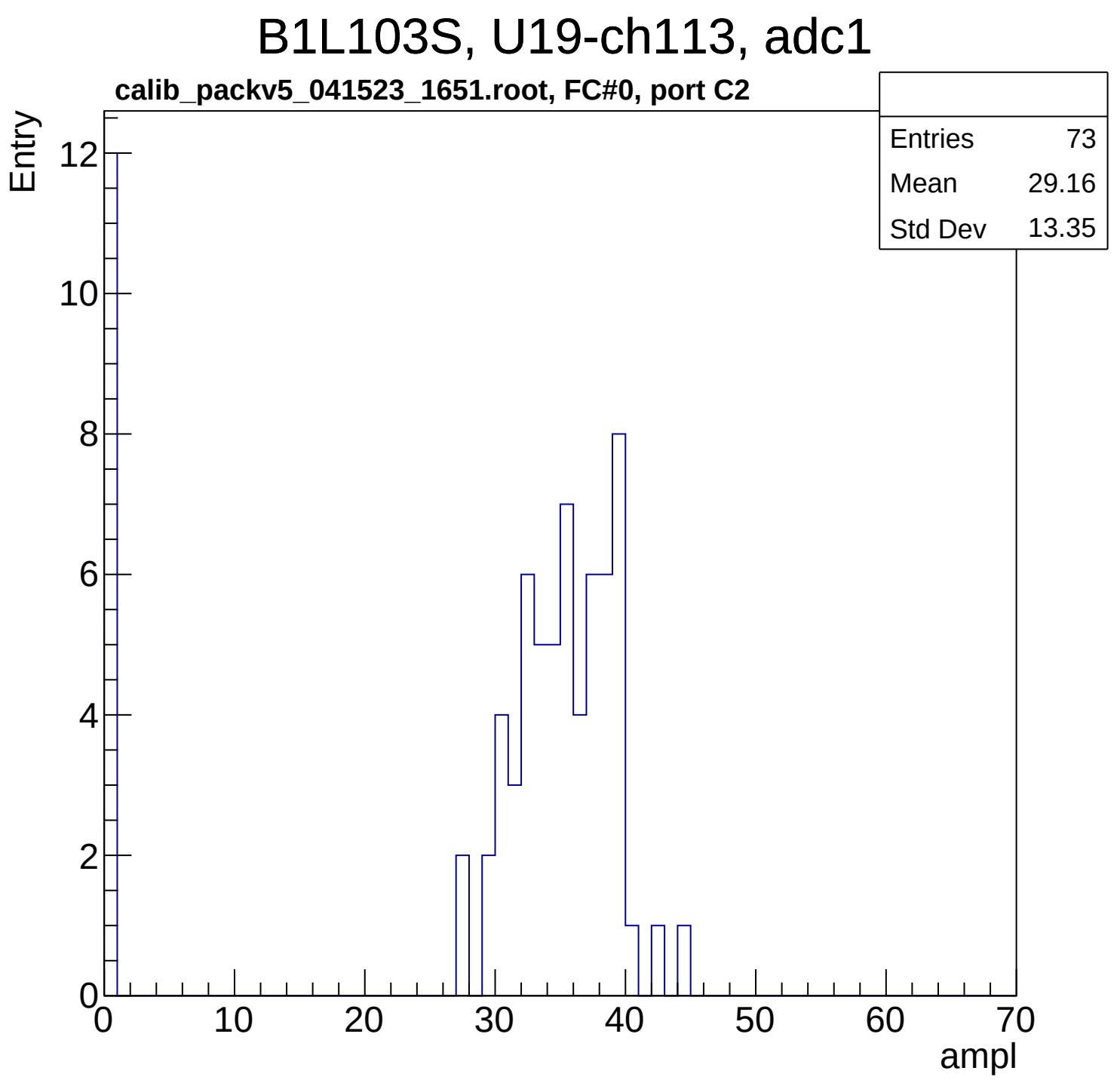
B1L103S, U19-ch113, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 29.16
Std Dev 13.35
Entry
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4
6
8
10
12
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10
20
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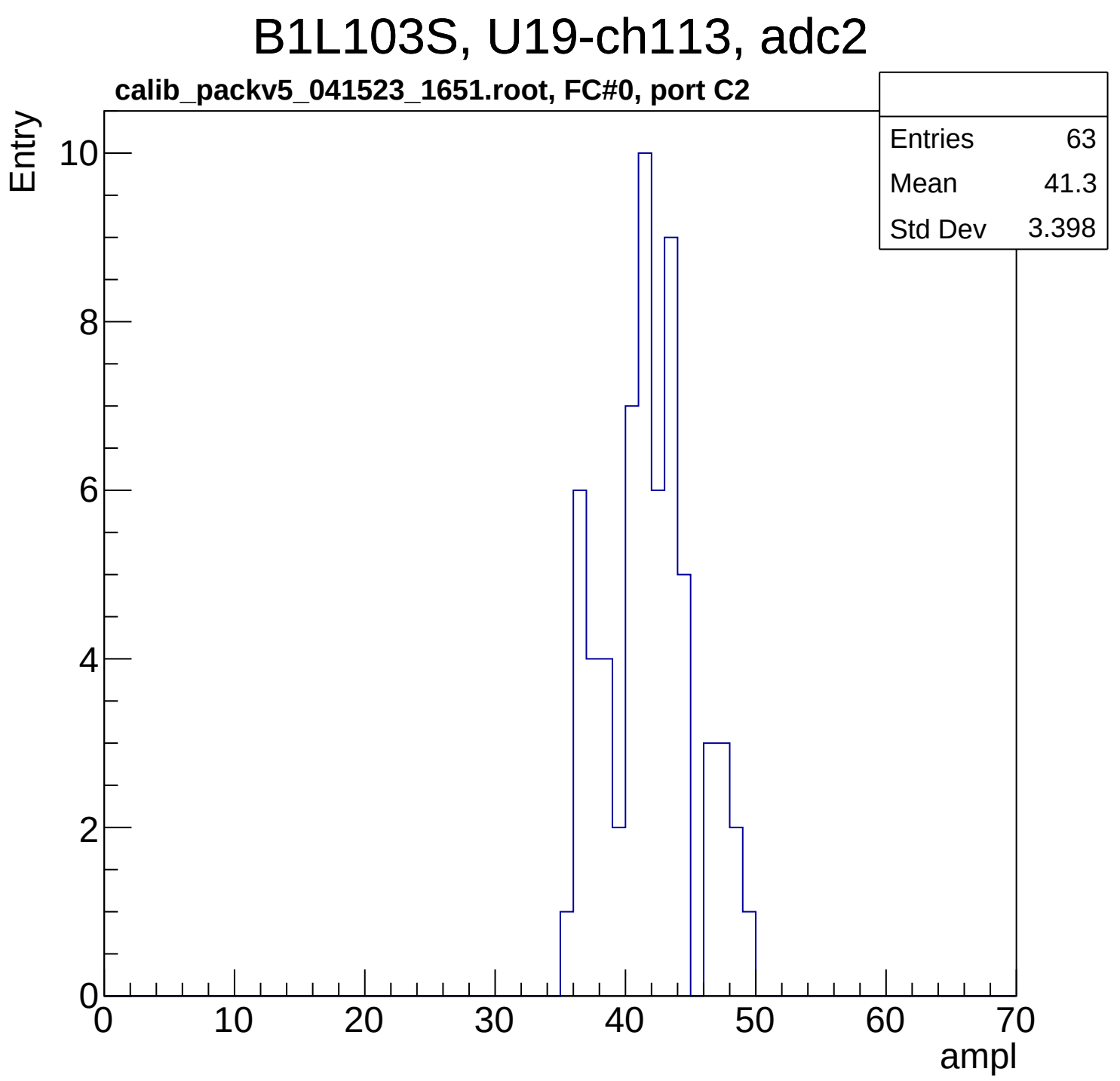
50
60
70
ampl


B1L103S, U19-ch113, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 41.3
Std Dev 3.398
Entry
ampl
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0
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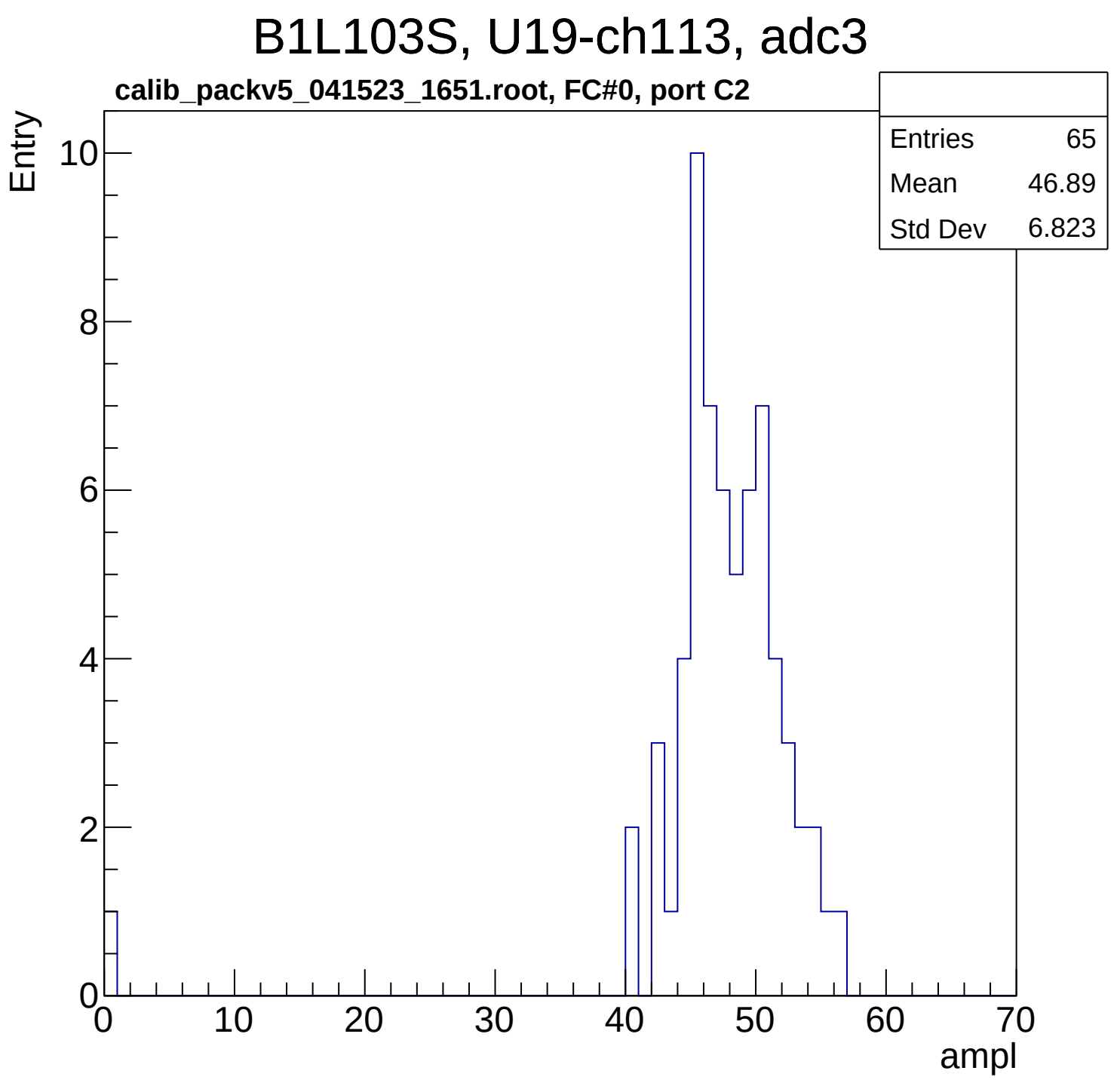
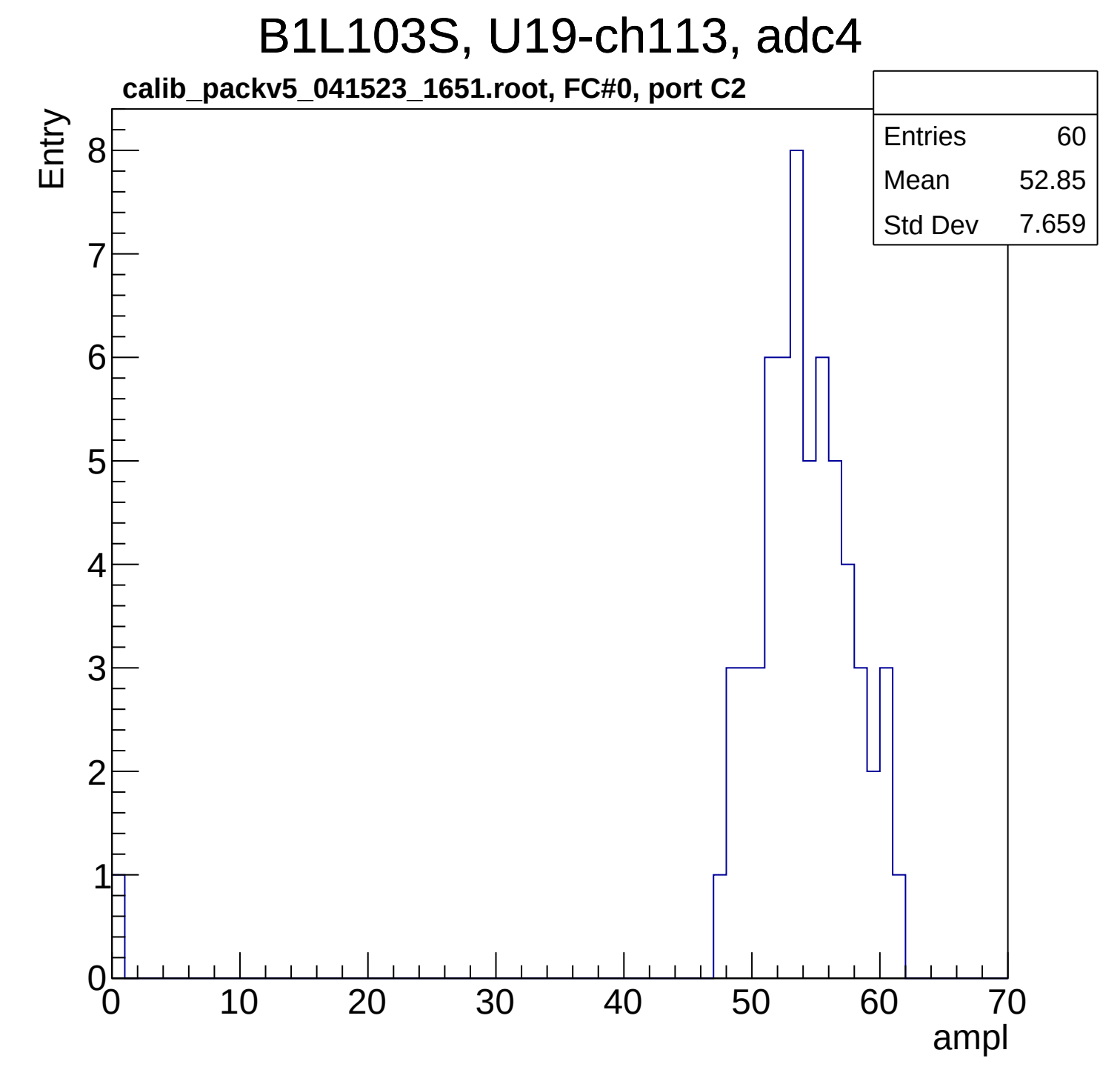

B1L103S, U19-ch113, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 46.89
Std Dev 6.823
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U19-ch113, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 52.85
Std Dev 7.659
Entry
ampl
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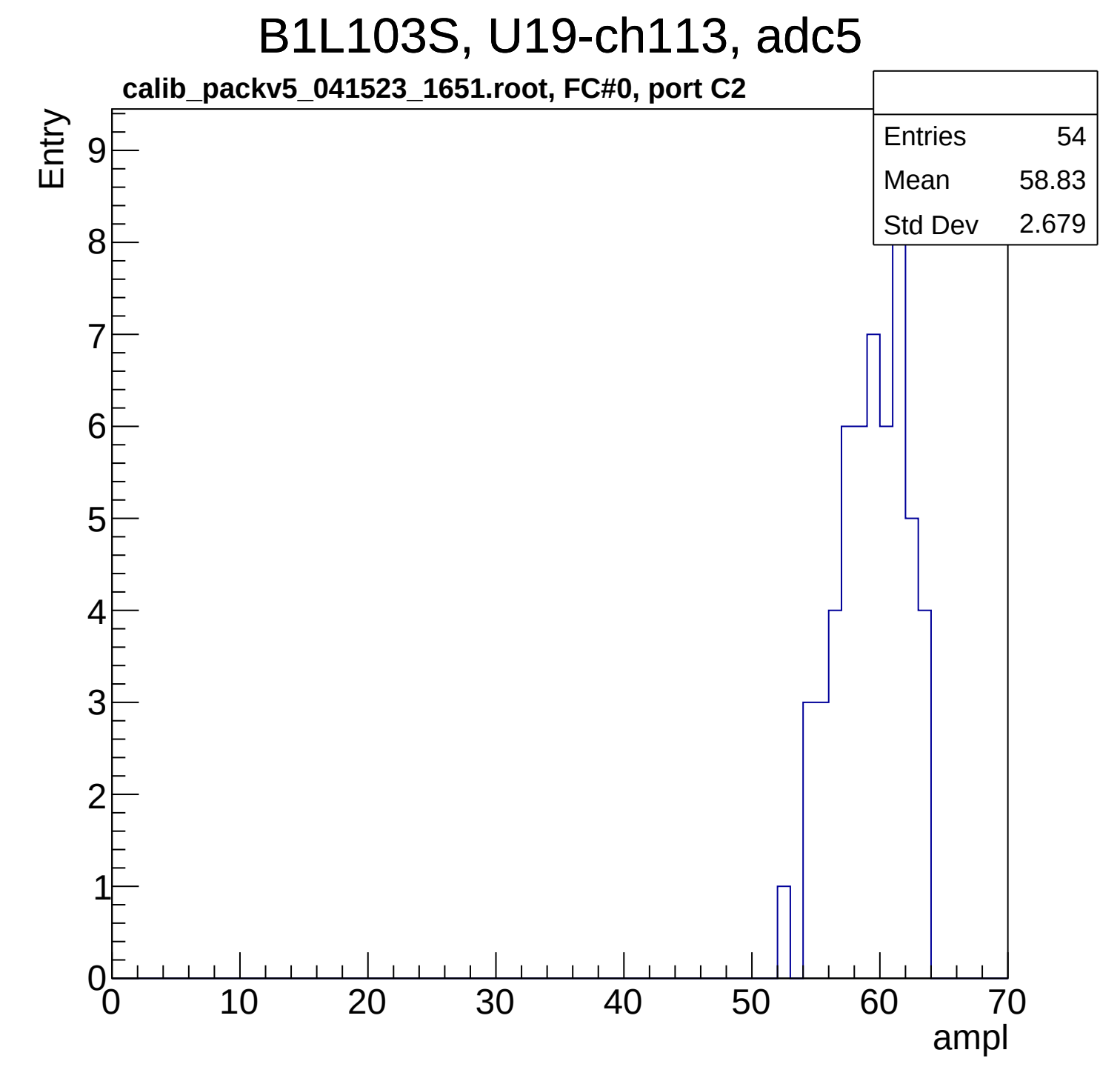
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch113, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 58.83
Std Dev 2.679
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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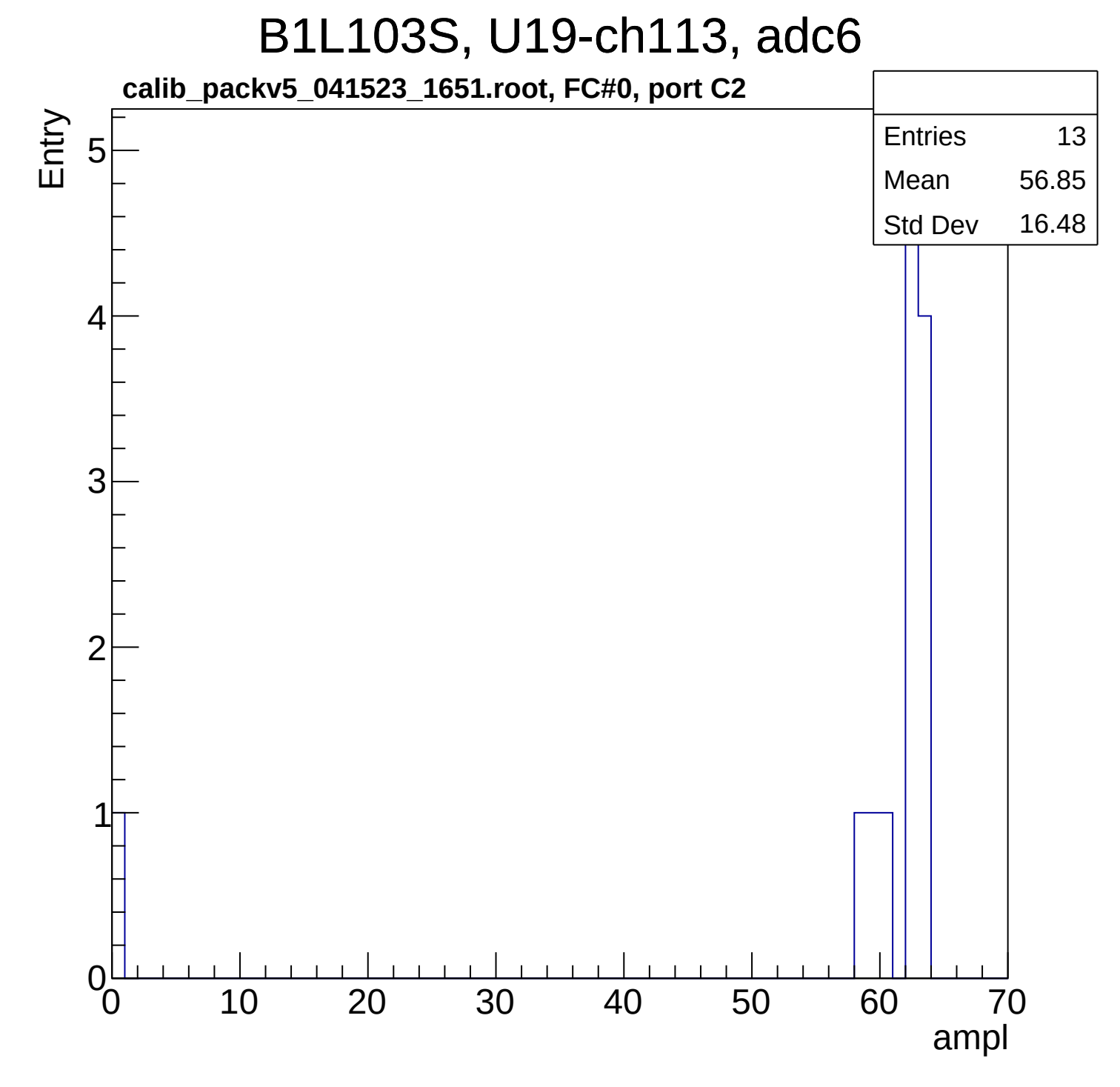
B1L103S, U19-ch113, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 56.85
Std Dev 16.48
Entry
ampl
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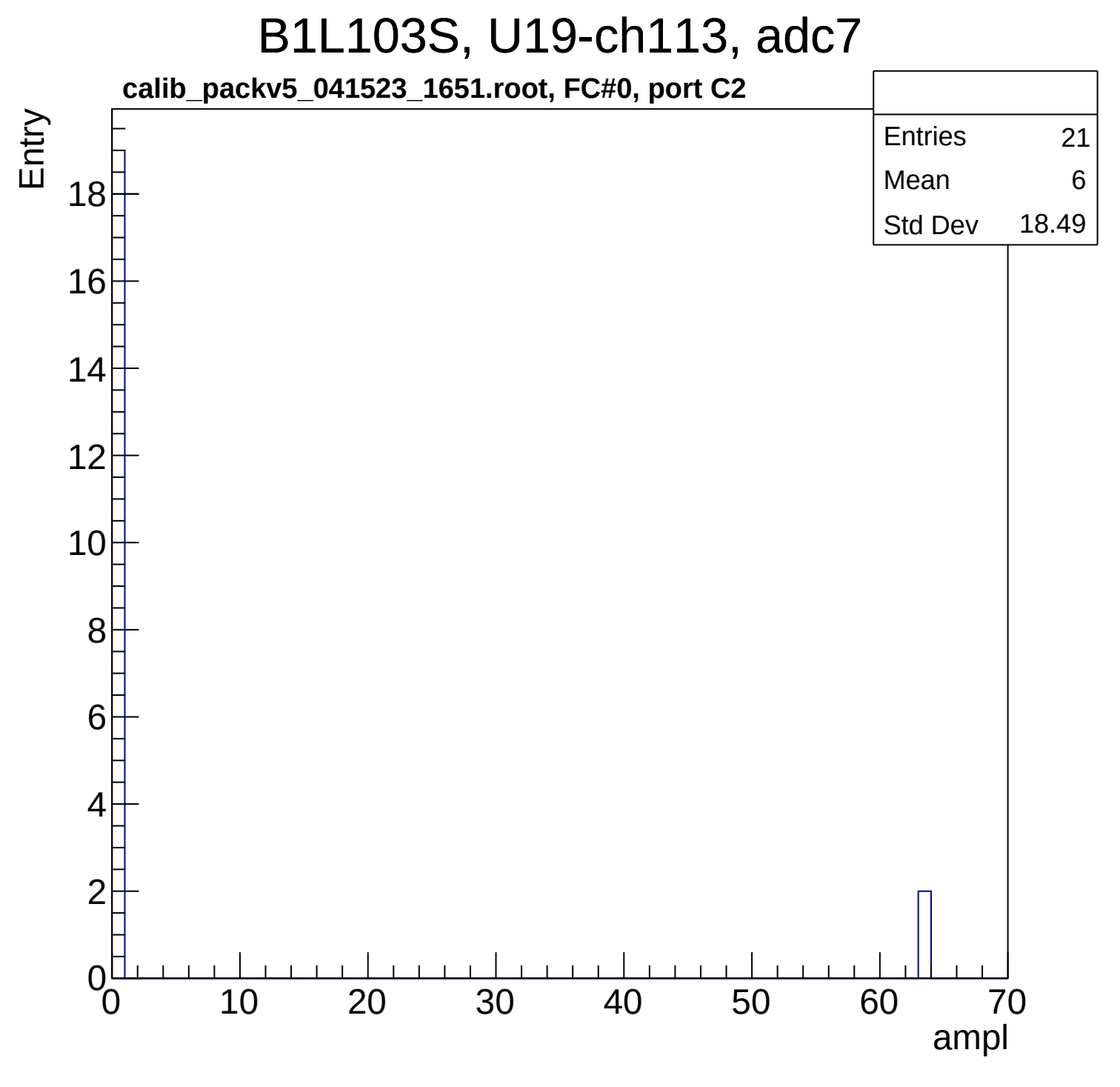
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U19-ch113, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 6
Std Dev 18.49
Entry
0
2
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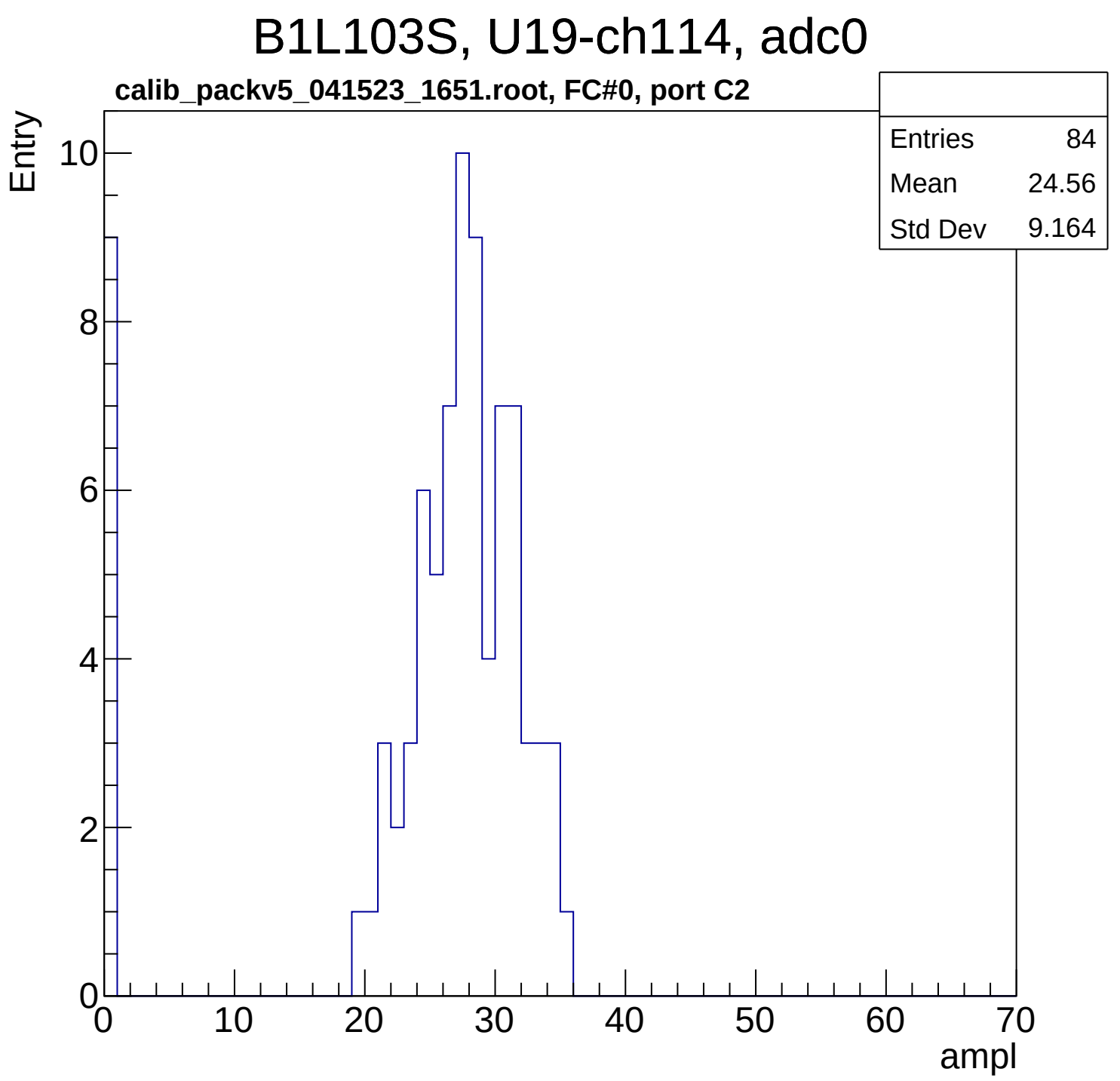
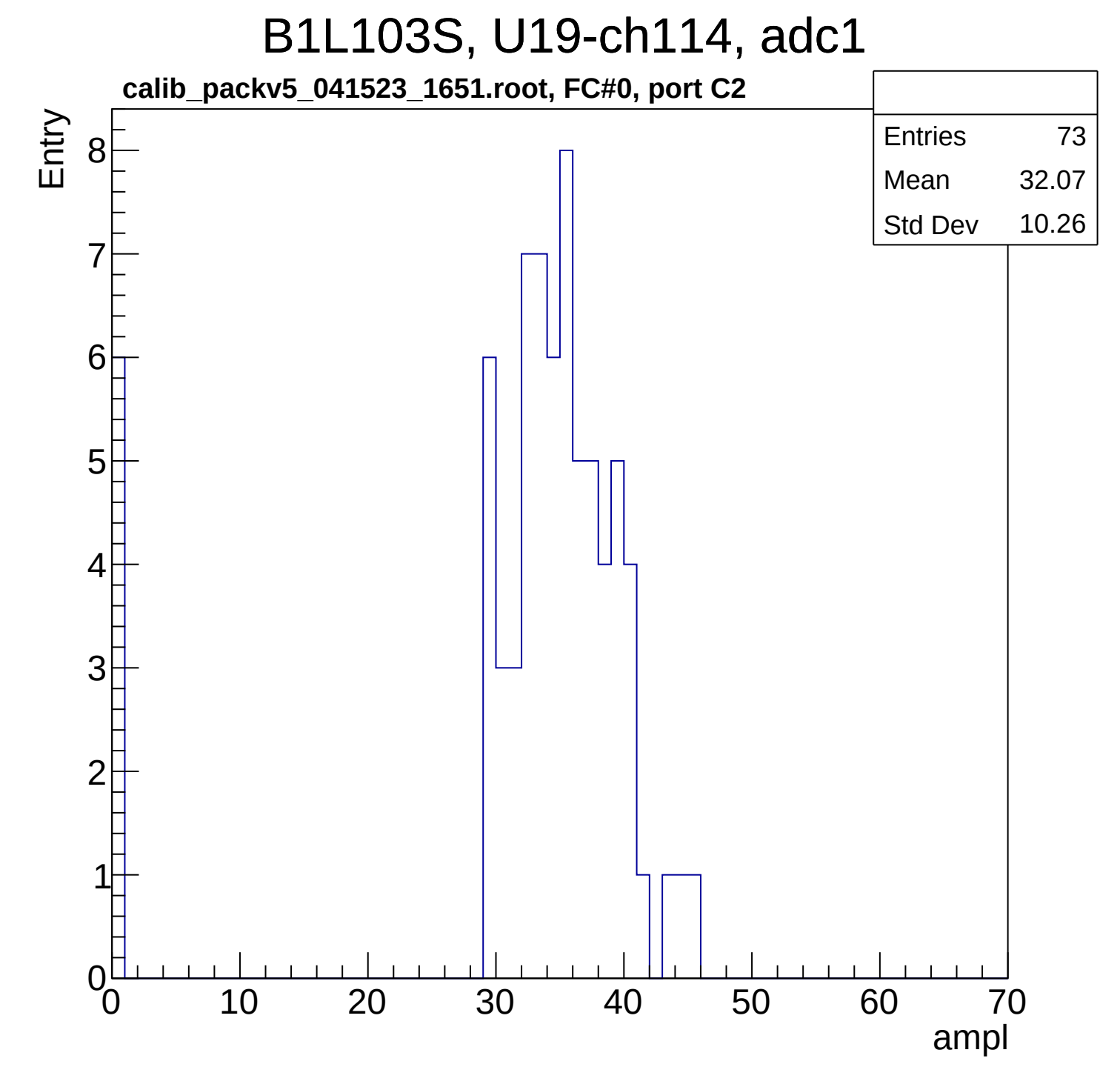
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch114, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 24.56
Std Dev 9.164
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch114, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 32.07
Std Dev 10.26
Entry
ampl
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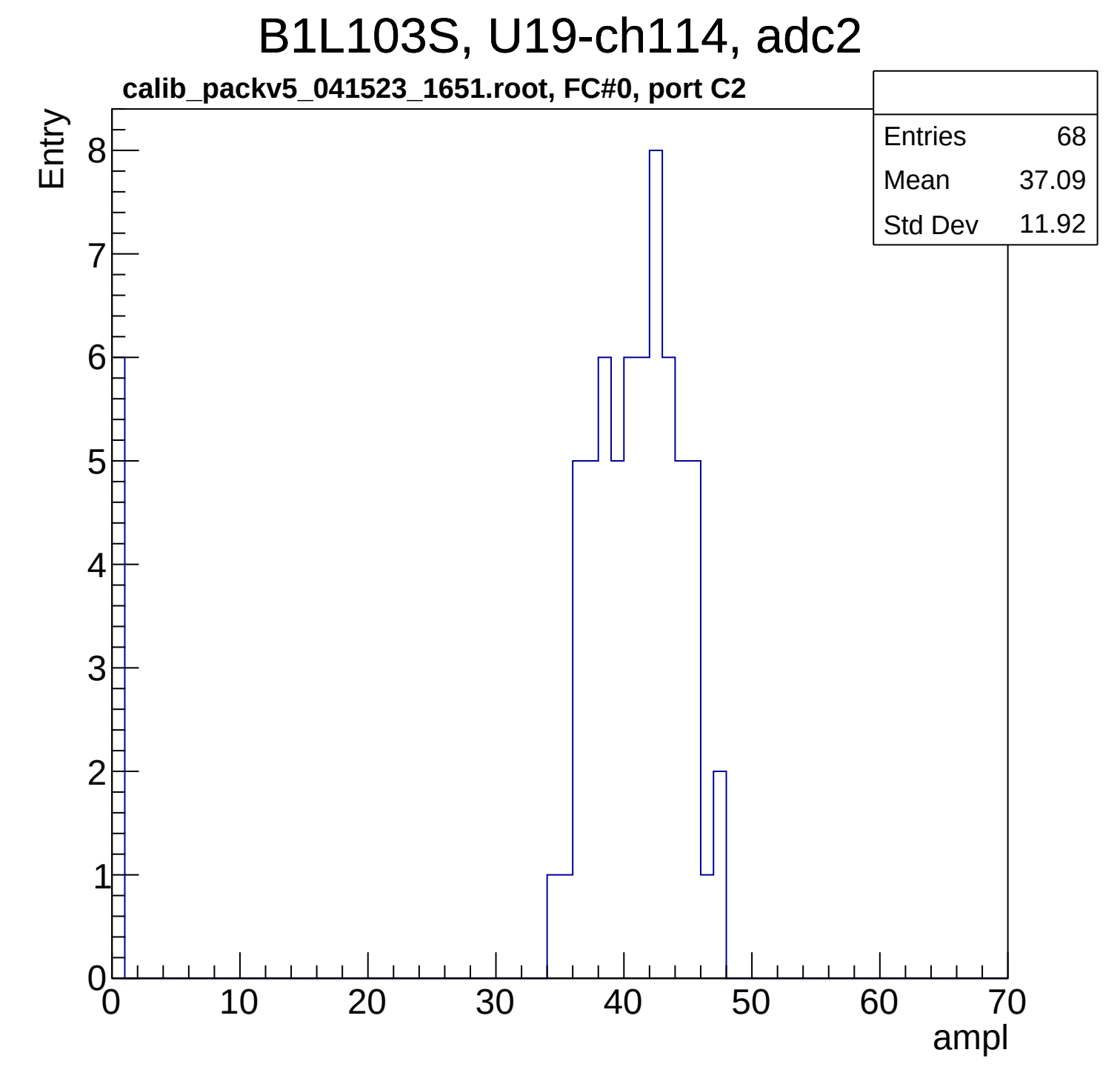
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch114, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 37.09
Std Dev 11.92
Entry
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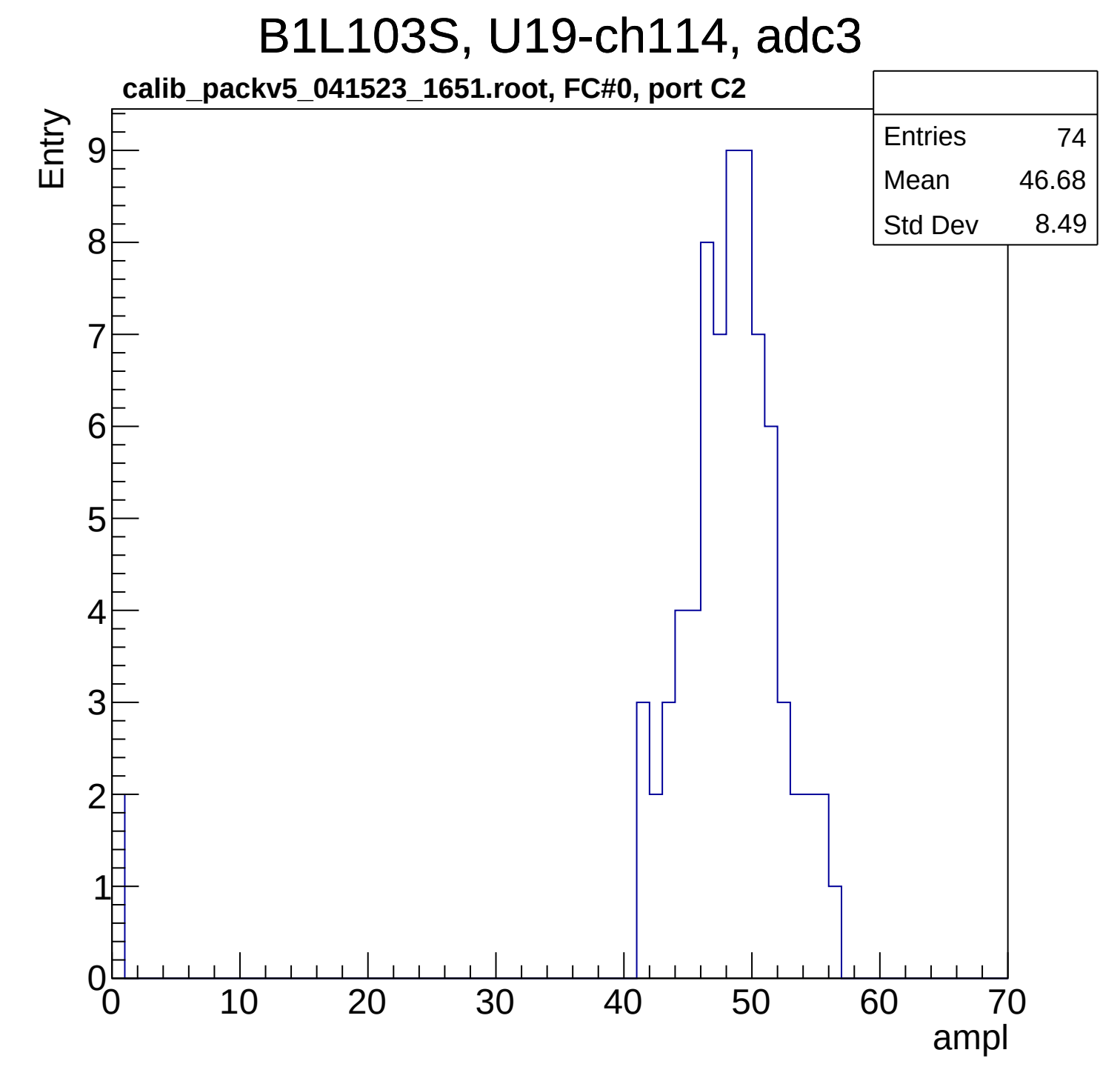
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch114, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 46.68
Std Dev 8.49
Entry
ampl
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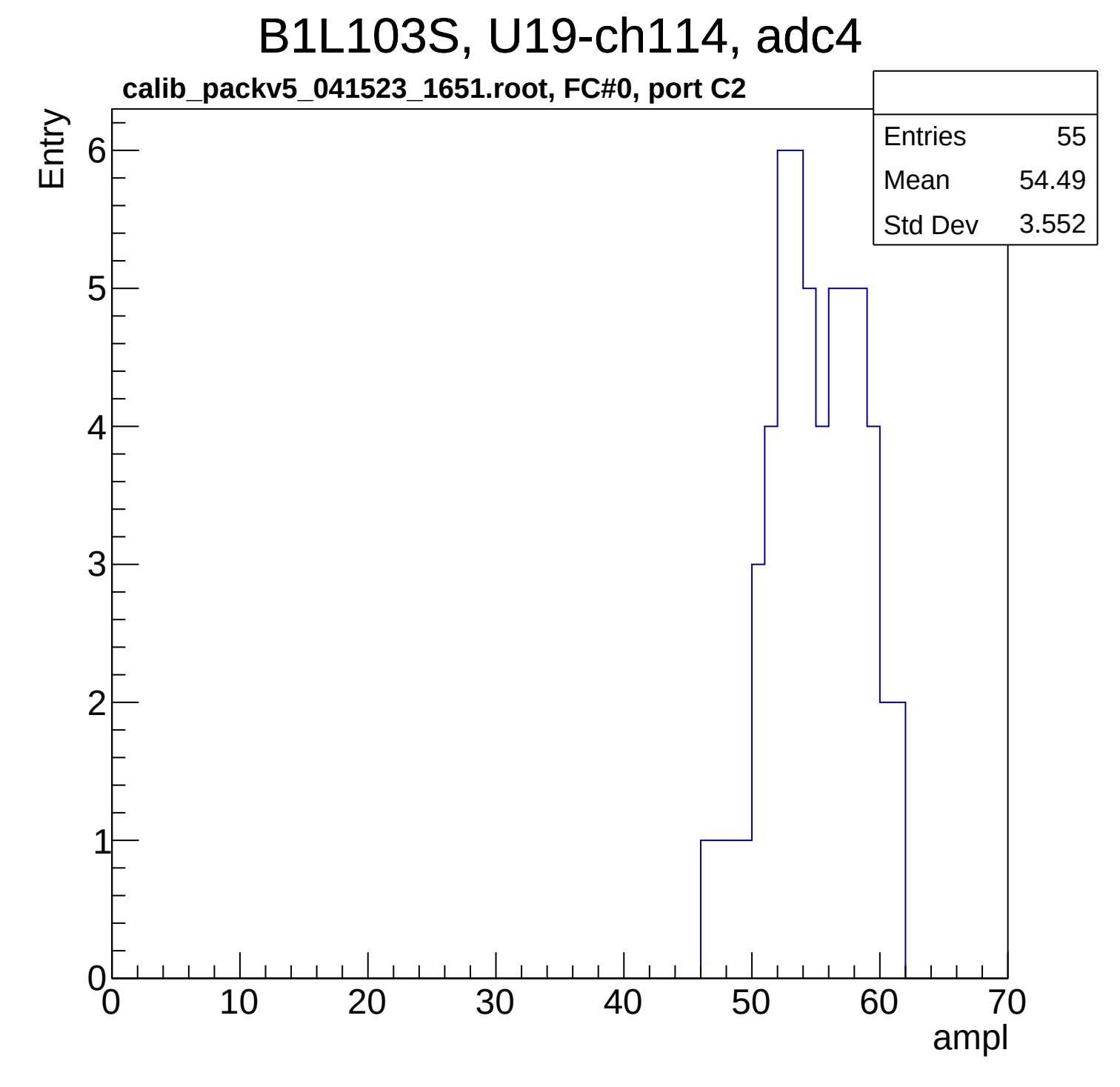
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L103S, U19-ch114, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 54.49
Std Dev 3.552
Entry
ampl
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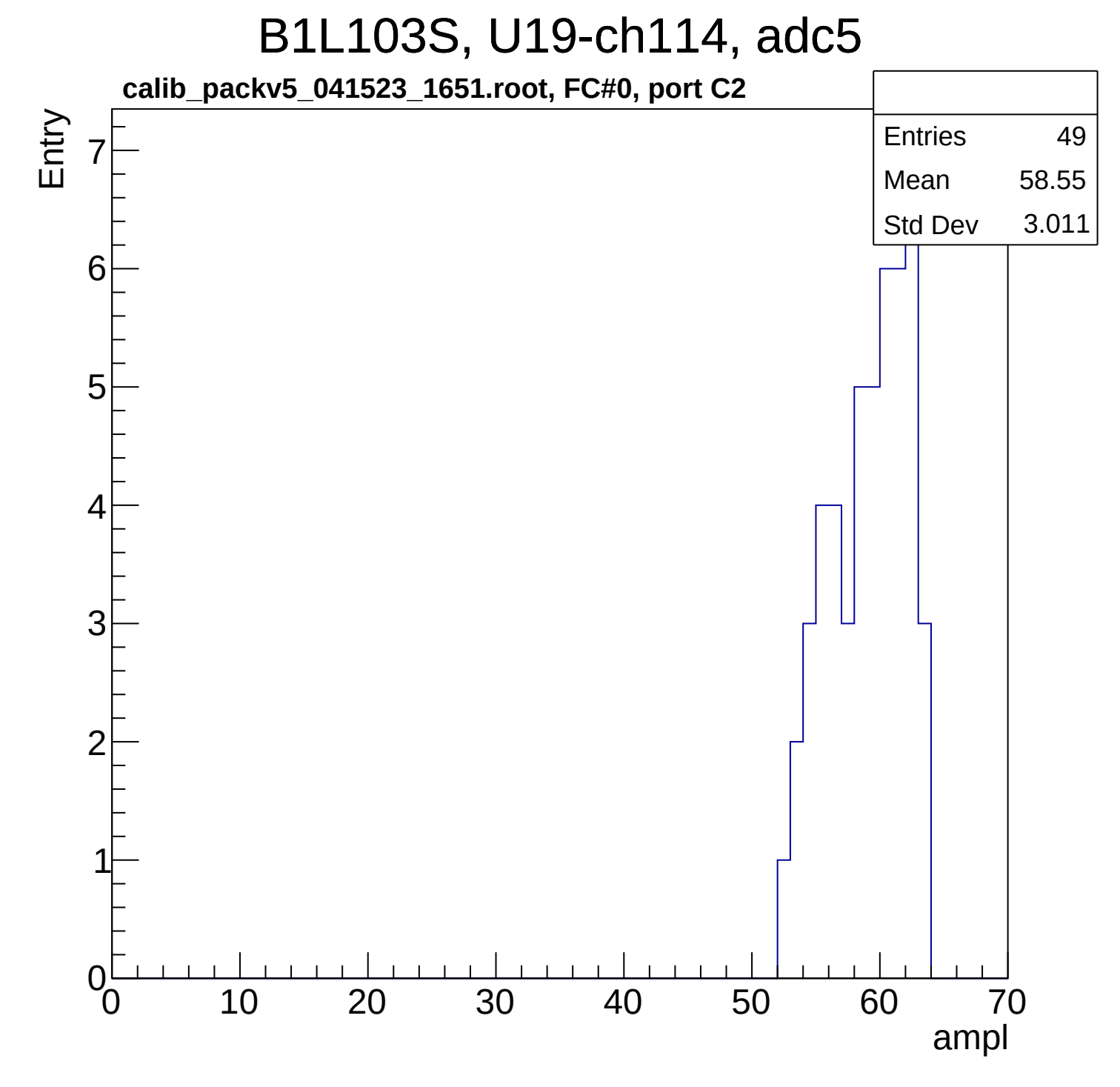
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U19-ch114, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 58.55
Std Dev 3.011
Entry
ampl
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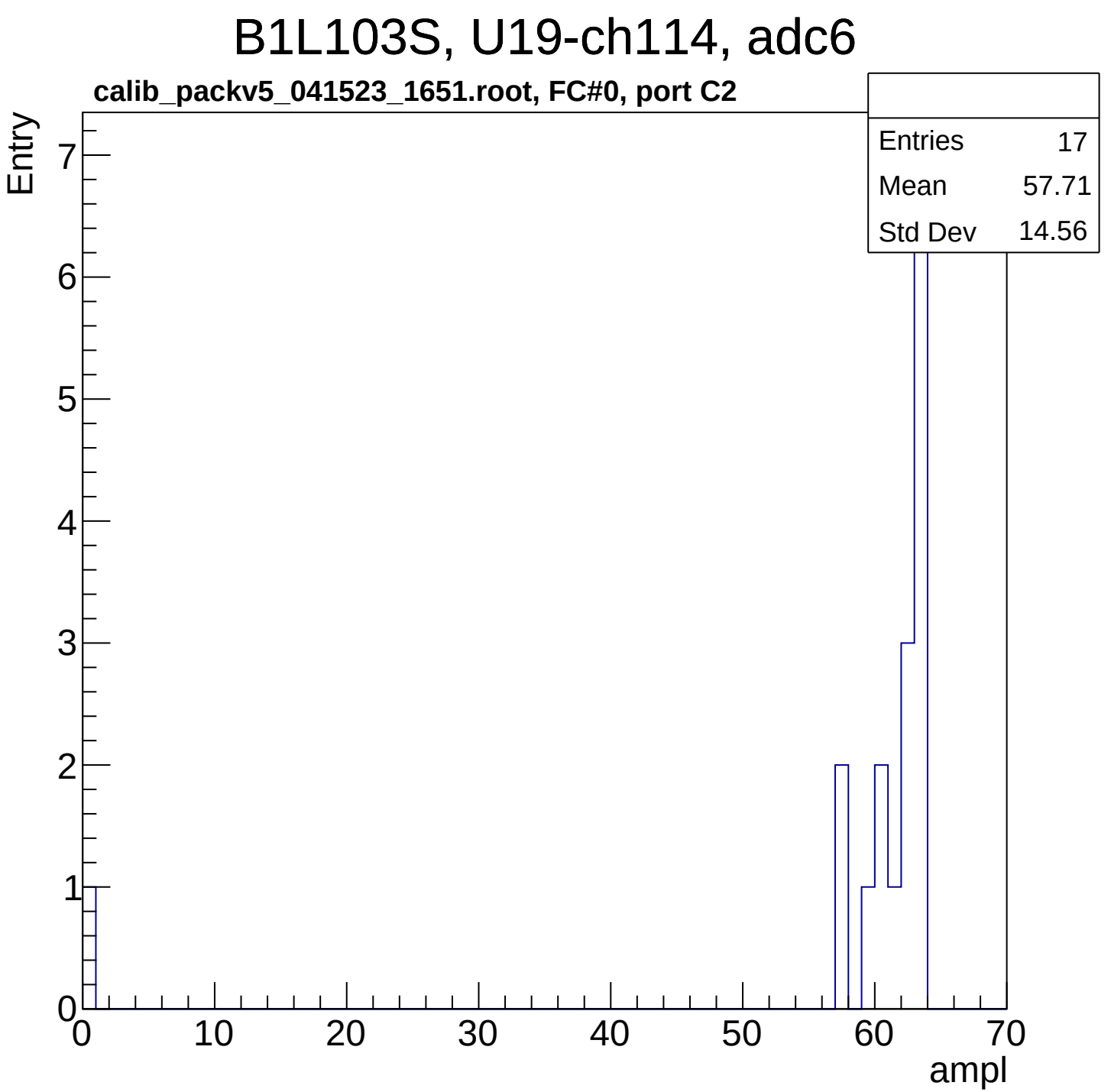
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch114, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 57.71
Std Dev 14.56
Entry
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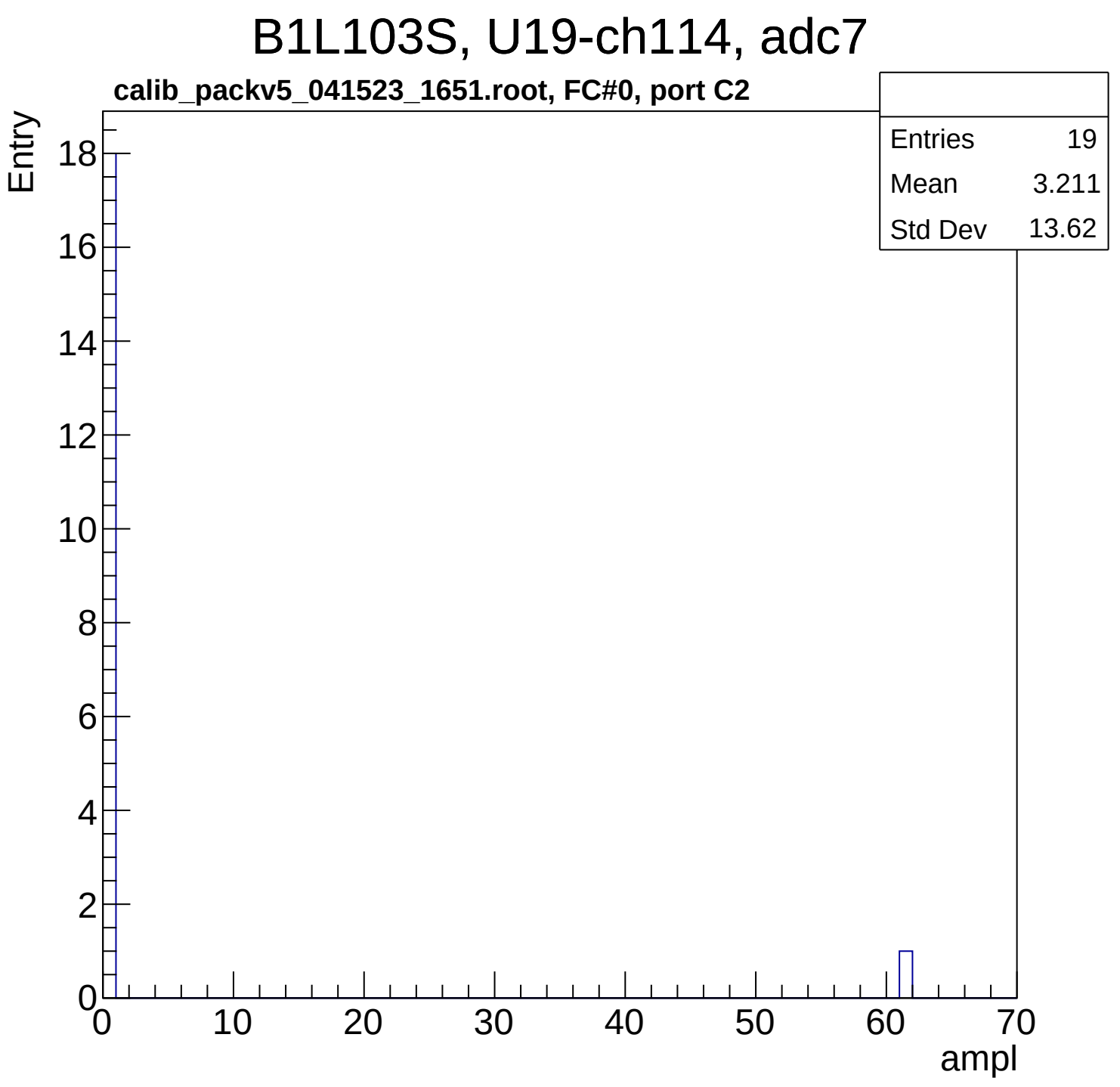
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch114, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.211
Std Dev 13.62
Entry
ampl
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4
6
8
10
12
14
16
18
0
10
20
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40
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60
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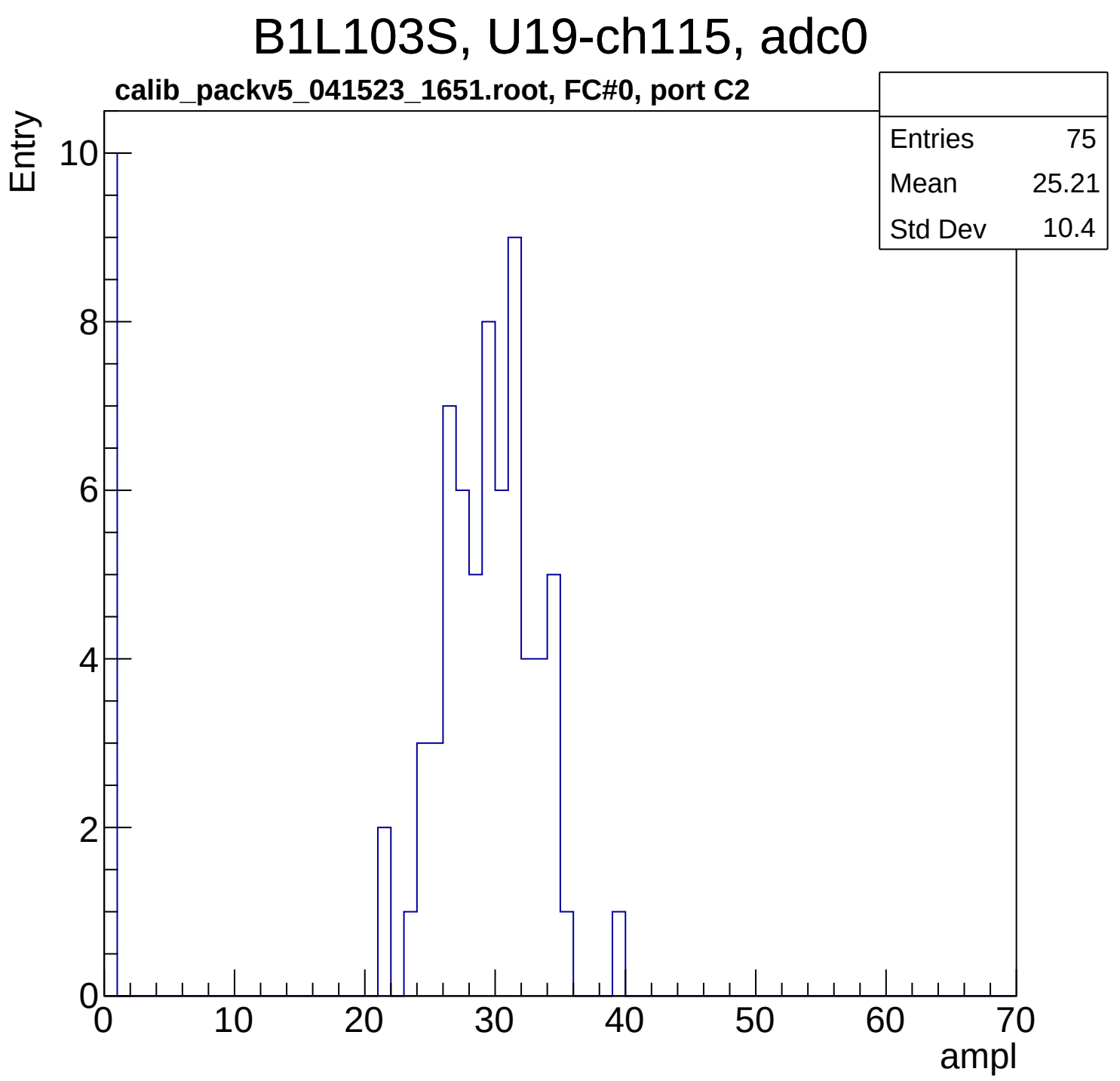
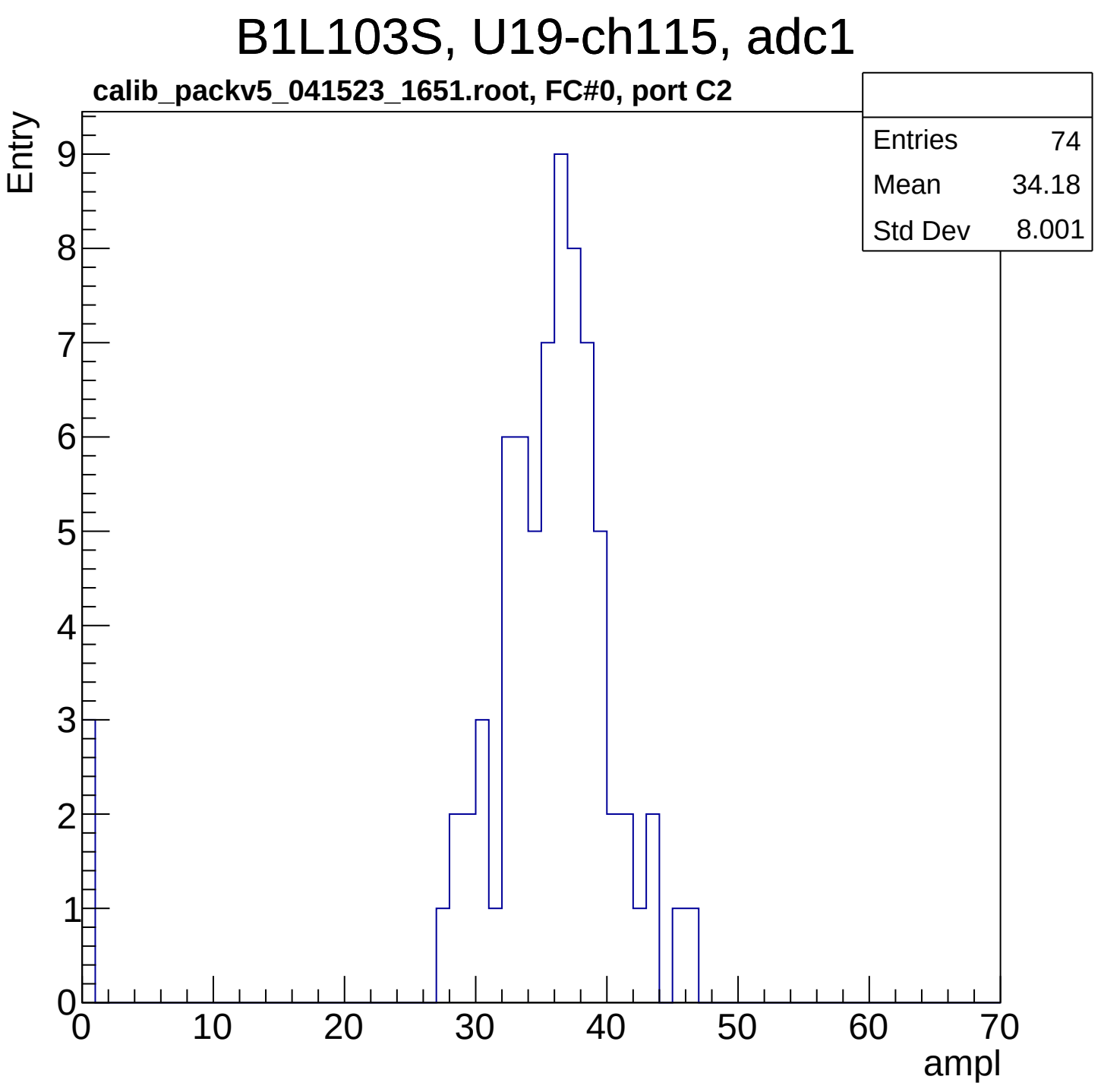

B1L103S, U19-ch115, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 25.21
Std Dev 10.4
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch115, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 34.18
Std Dev 8.001
Entry
ampl
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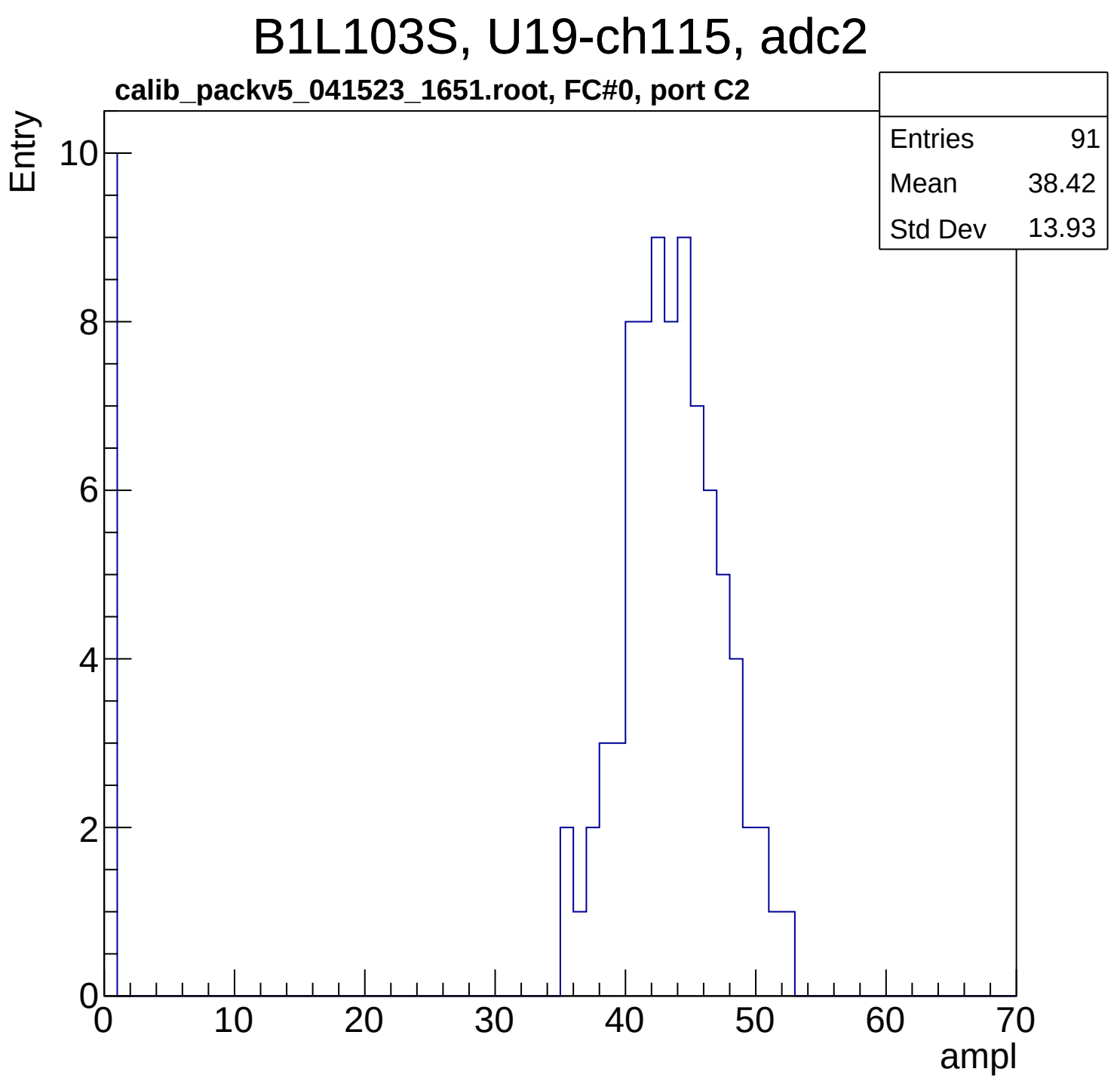
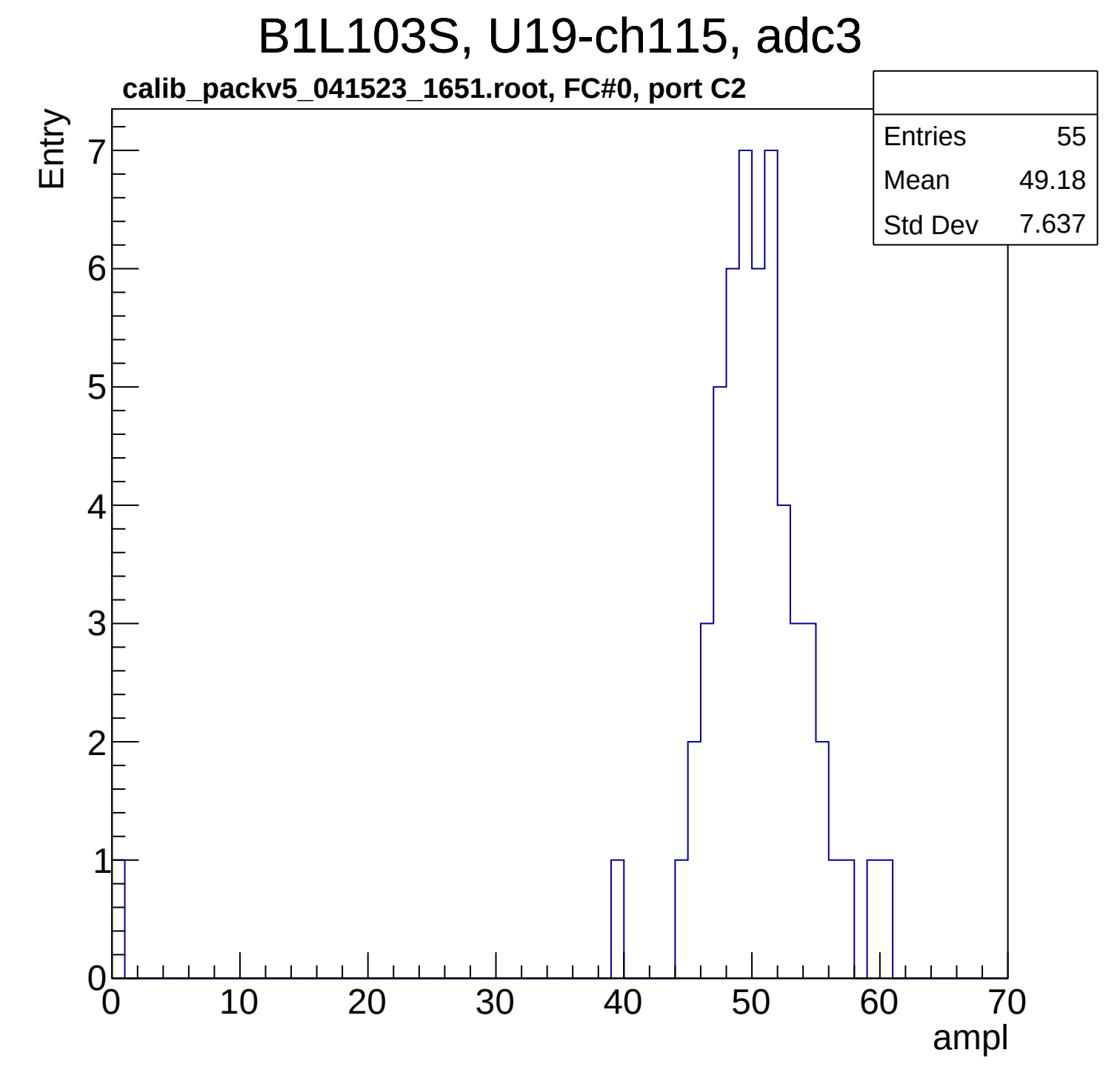
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch115, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 38.42
Std Dev 13.93
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch115, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 49.18
Std Dev 7.637
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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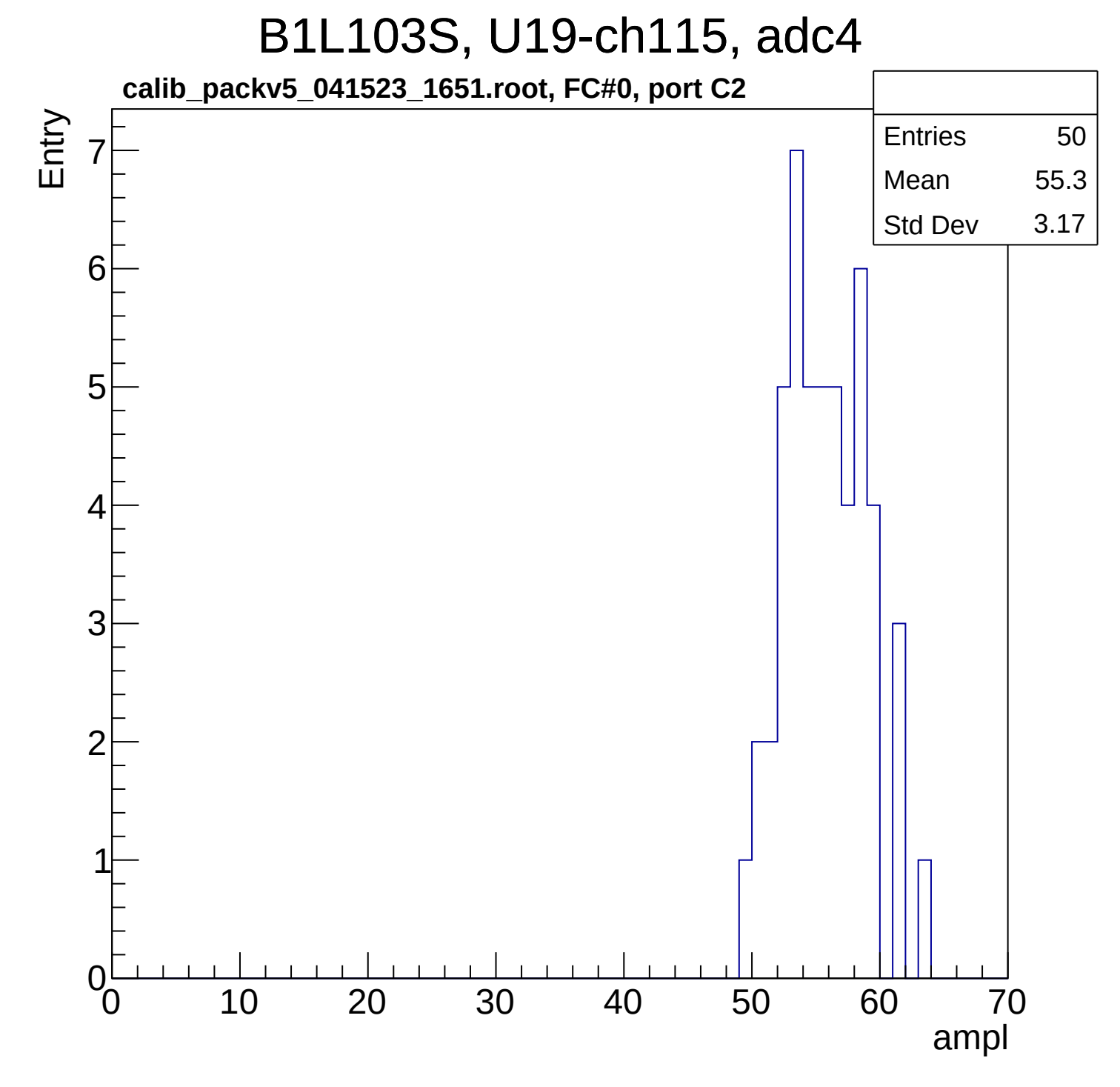
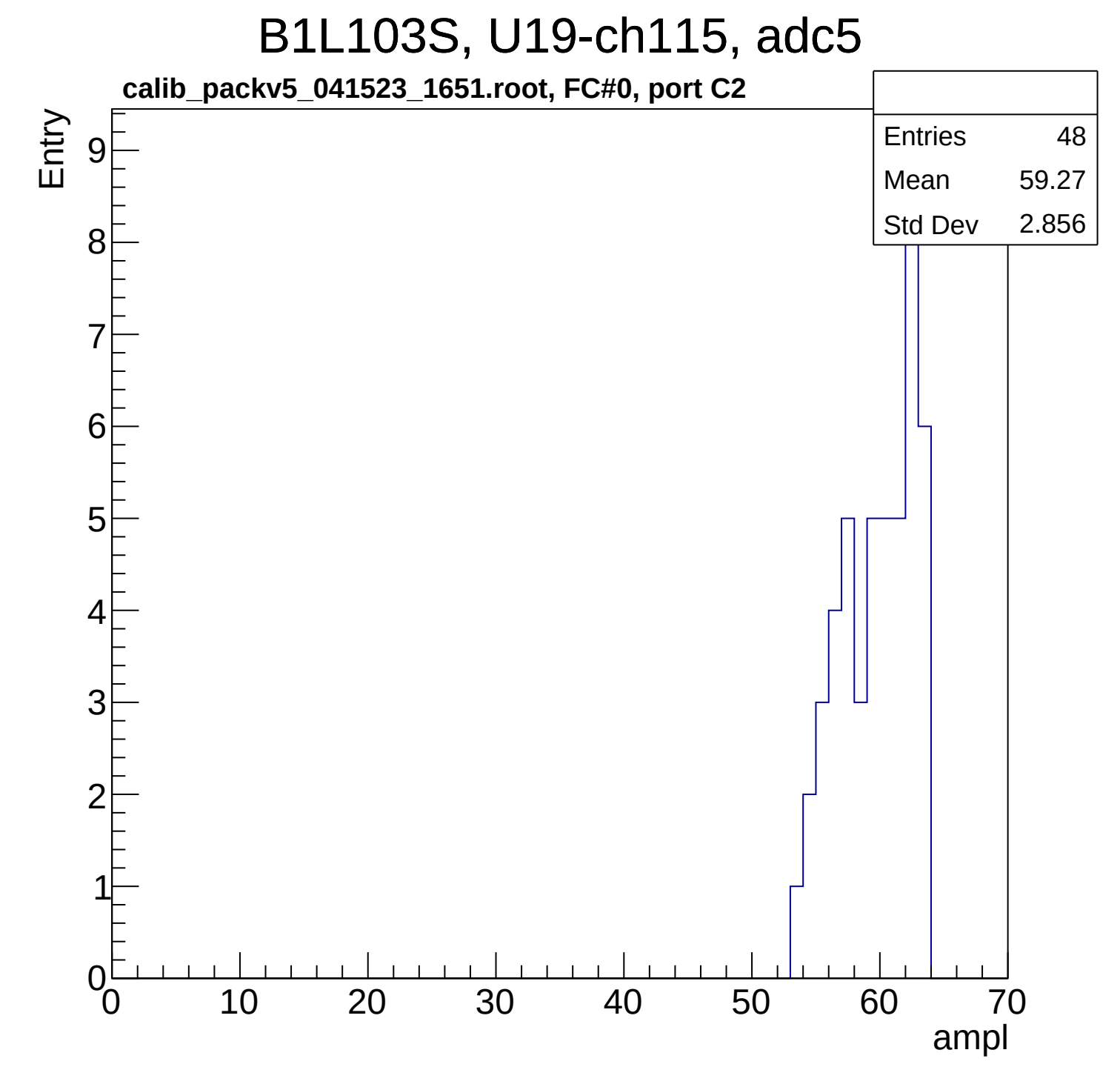

B1L103S, U19-ch115, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 55.3
Std Dev 3.17
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch115, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 59.27
Std Dev 2.856
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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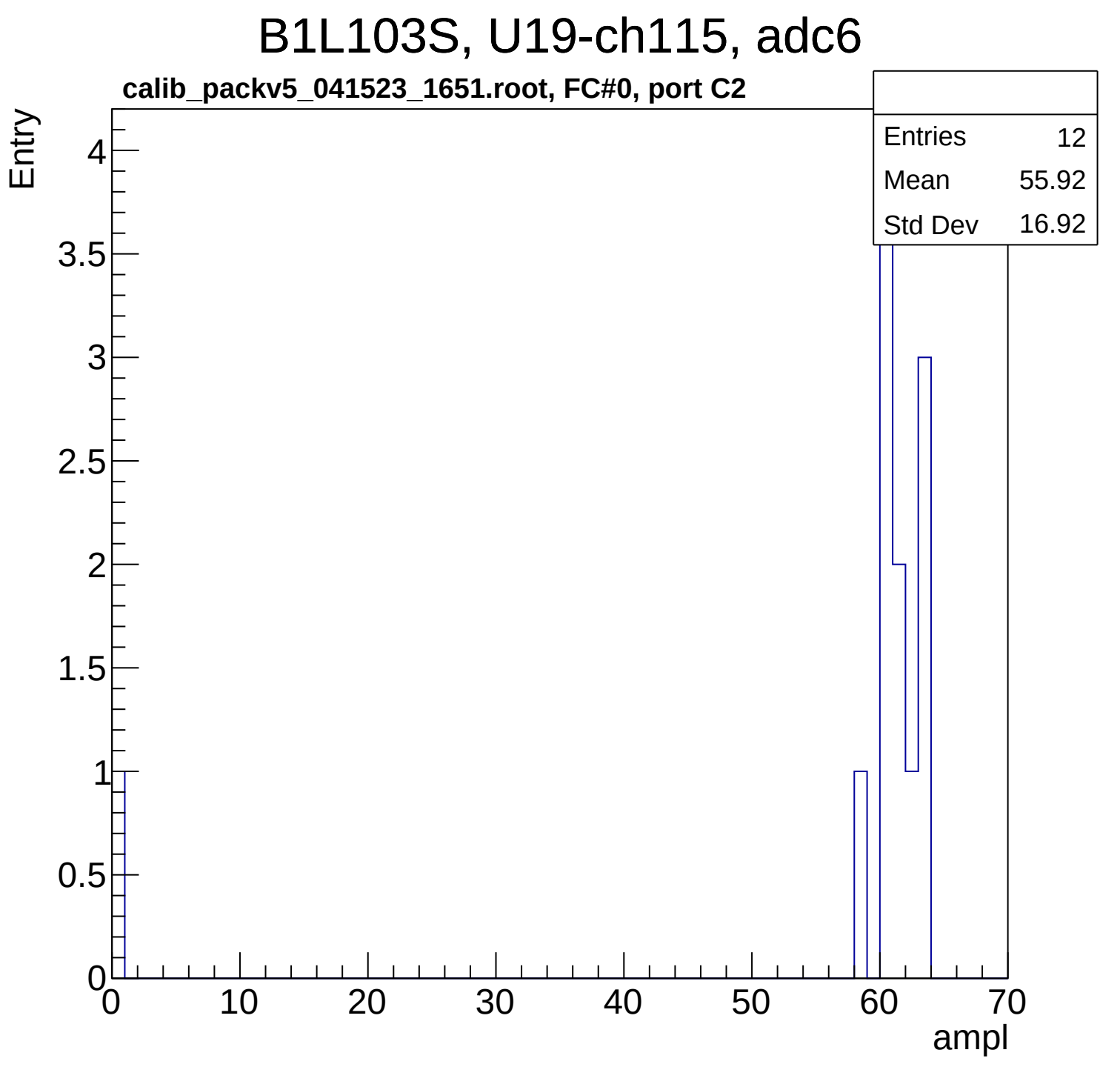
40
50
60
70


B1L103S, U19-ch115, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 55.92
Std Dev 16.92
Entry
ampl
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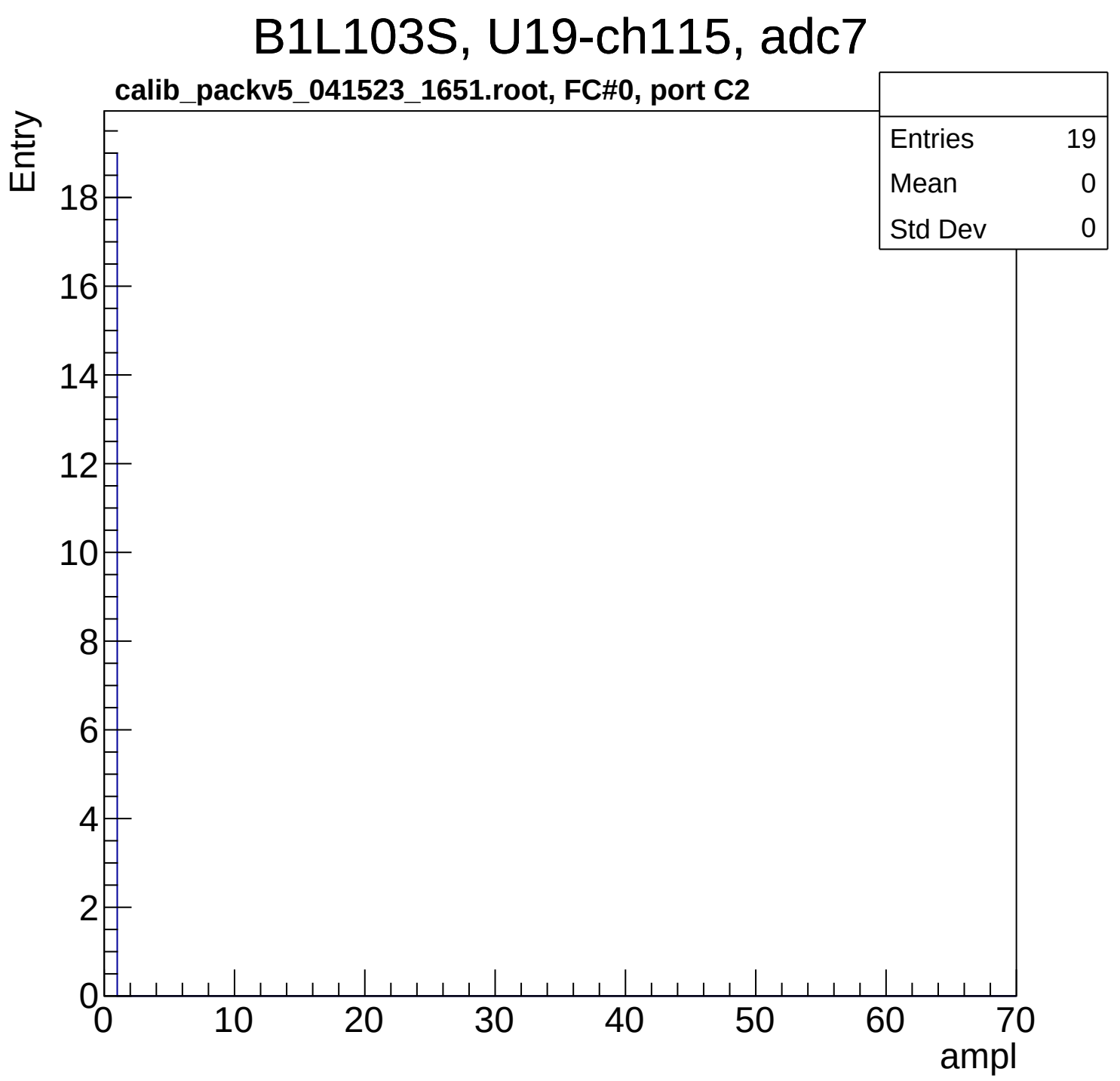
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U19-ch115, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
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6
8
10
12
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16
18
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10
20
30
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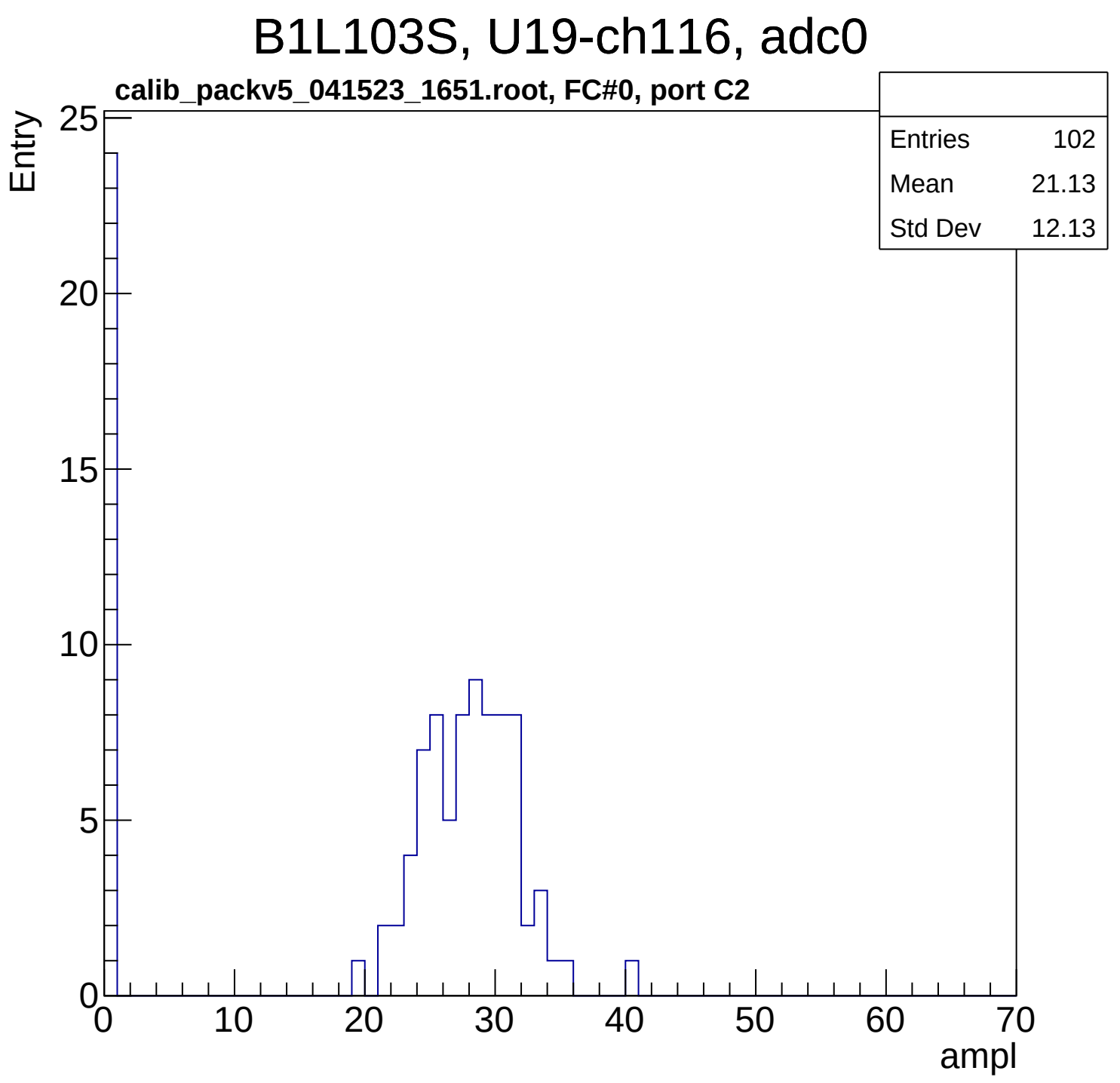
70
ampl


B1L103S, U19-ch116, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 102
Mean 21.13
Std Dev 12.13
Entry
ampl
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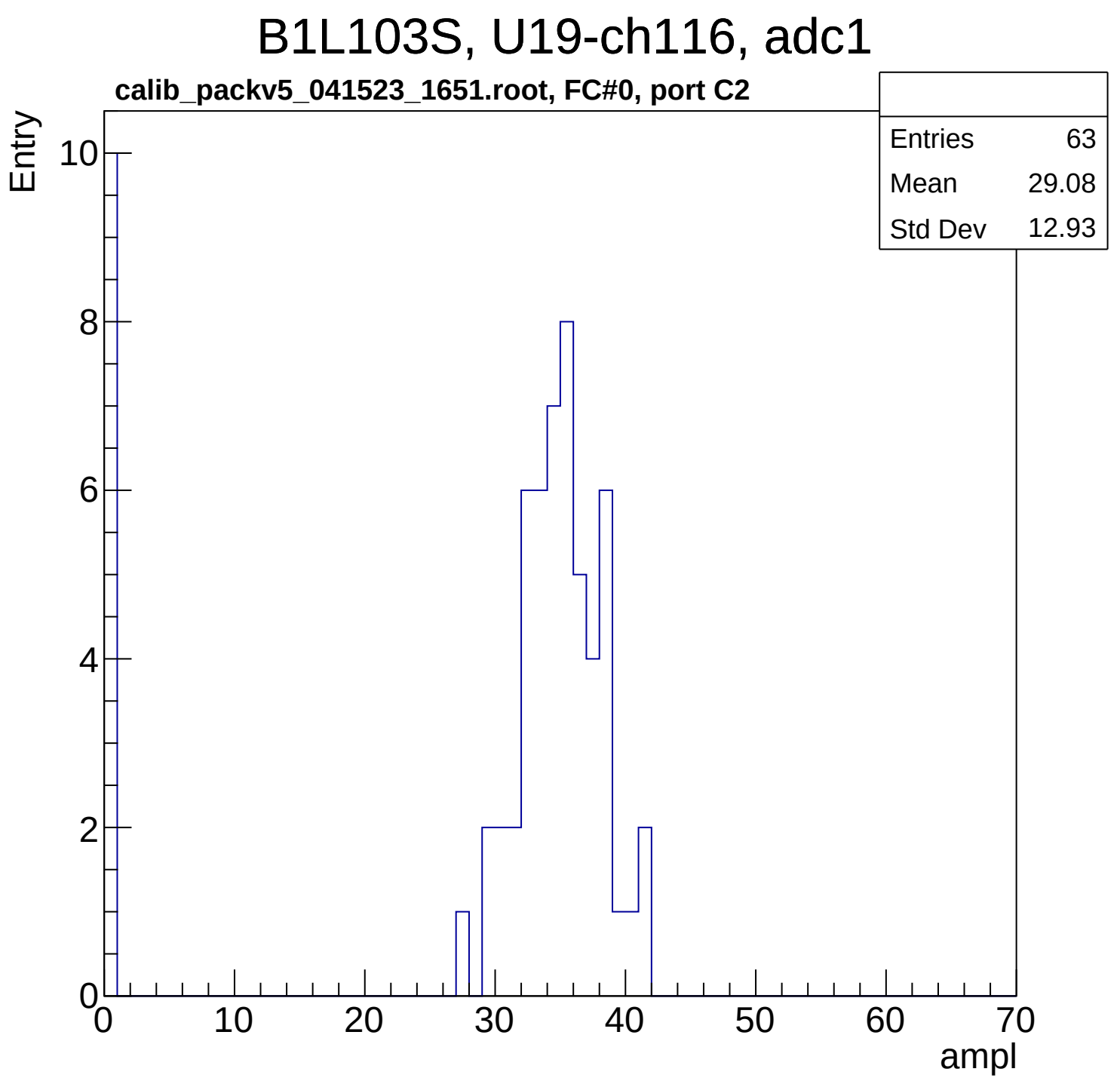
5
10
15
20
25
0
10
20
30
40
50
60
70


B1L103S, U19-ch116, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 29.08
Std Dev 12.93
Entry
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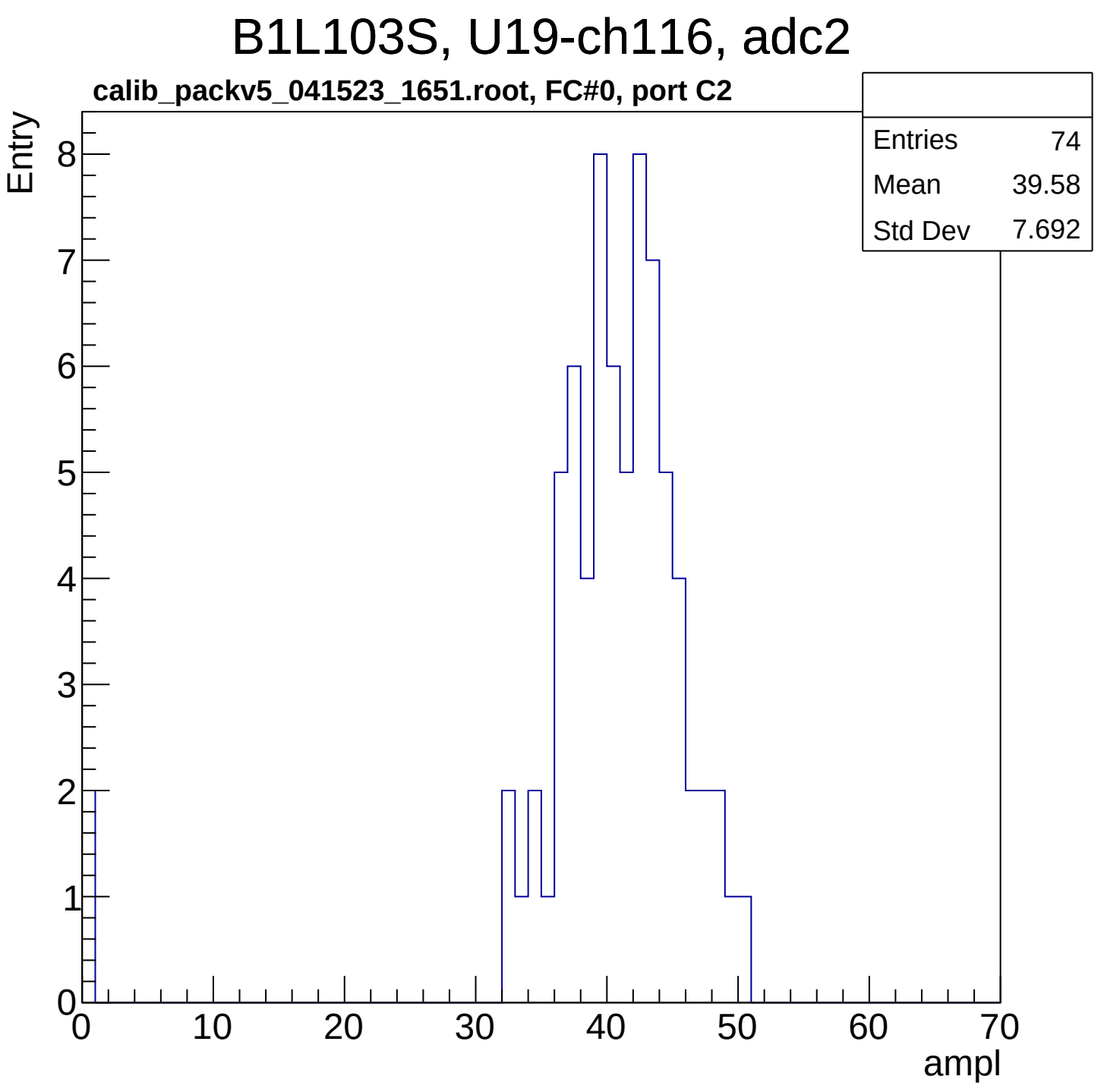
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch116, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 39.58
Std Dev 7.692
Entry
ampl
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2
3
4
5
6
7
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0
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40
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60
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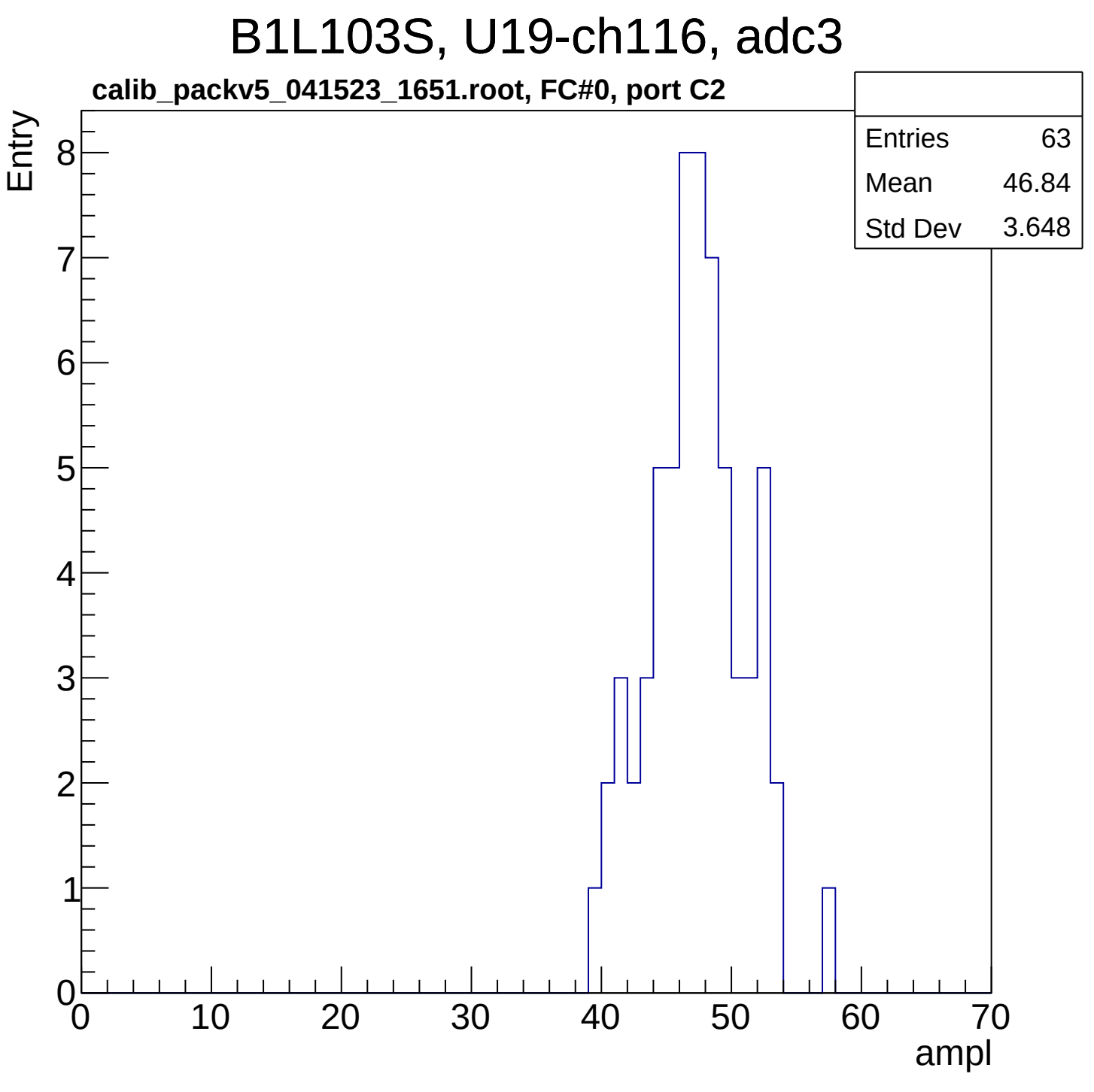
B1L103S, U19-ch116, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 46.84
Std Dev 3.648
Entry
ampl
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2
3
4
5
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7
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0
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60
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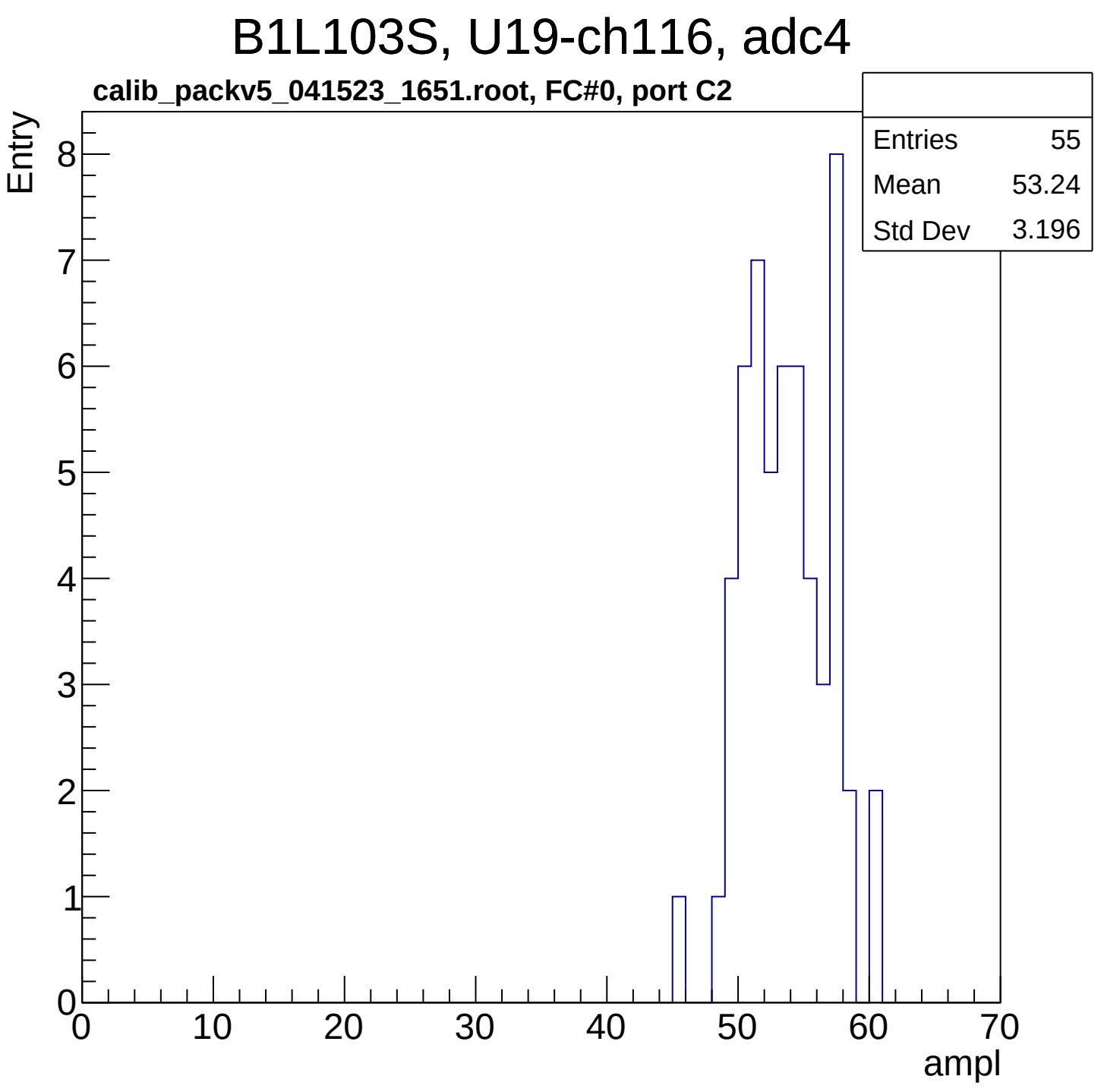
B1L103S, U19-ch116, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 53.24
Std Dev 3.196
Entry
ampl
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2
3
4
5
6
7
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0
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40
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60
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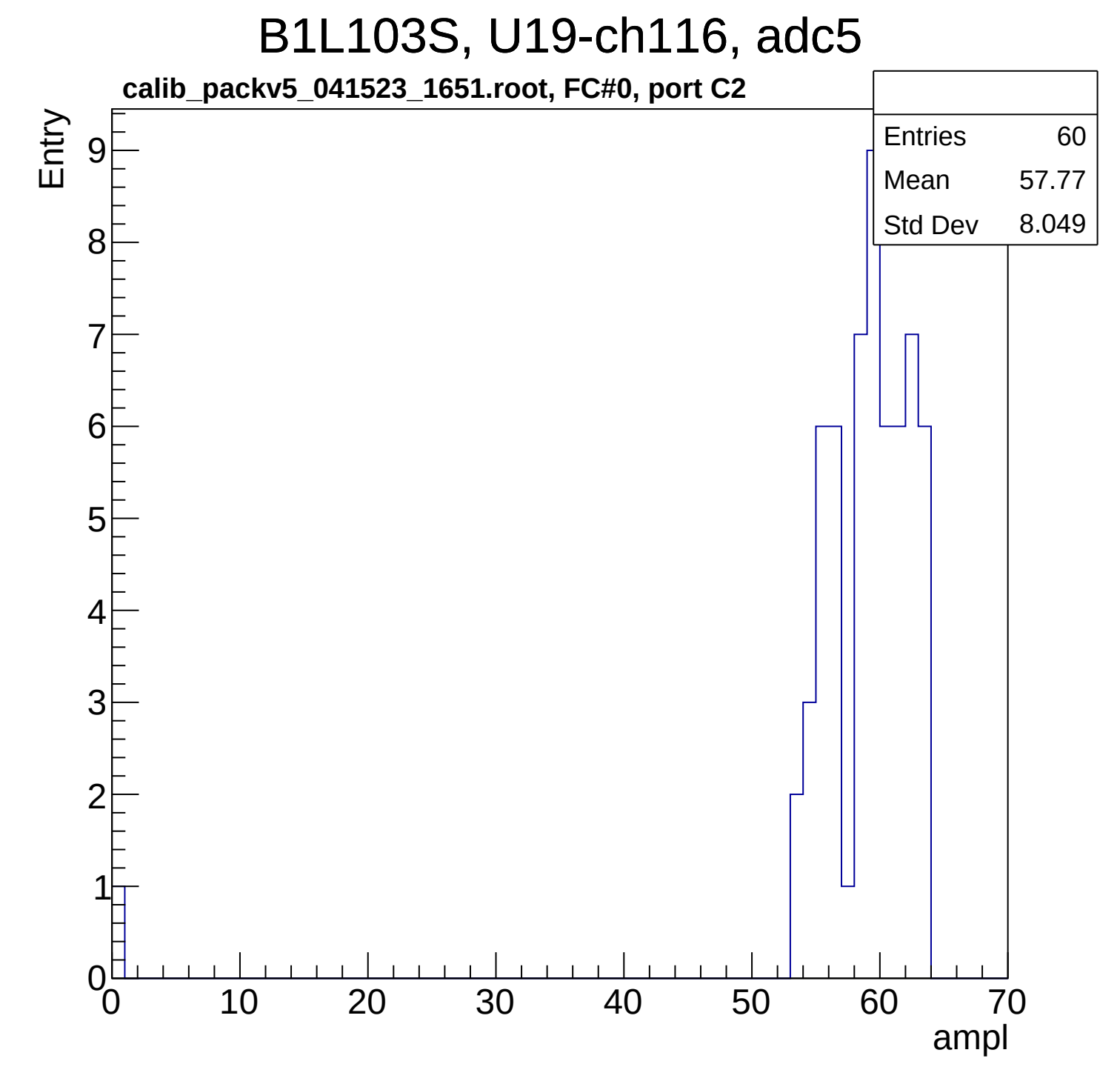
B1L103S, U19-ch116, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 57.77
Std Dev 8.049
Entry
ampl
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2
3
4
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6
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60
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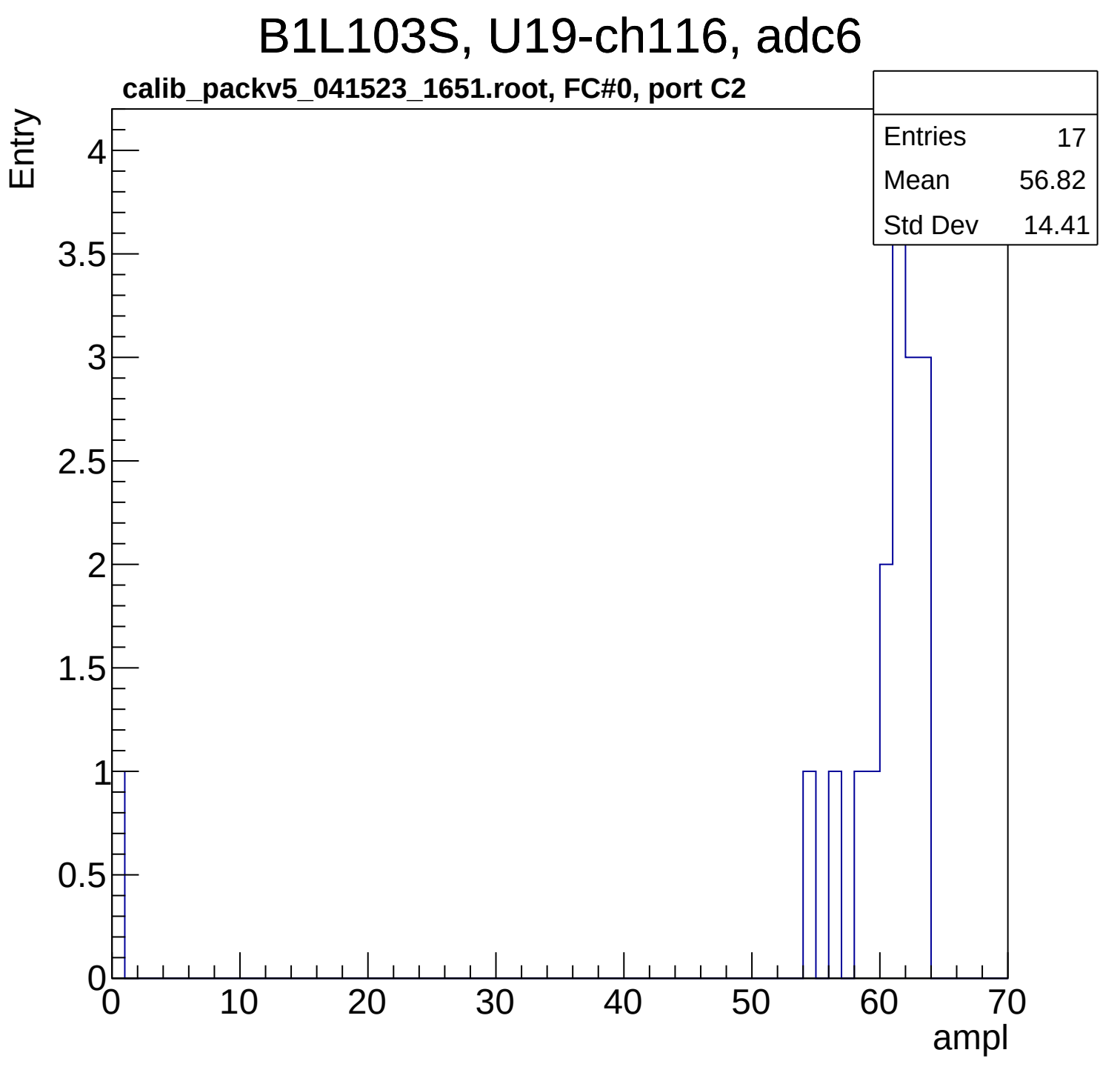
B1L103S, U19-ch116, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 56.82
Std Dev 14.41
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
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20
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40
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60
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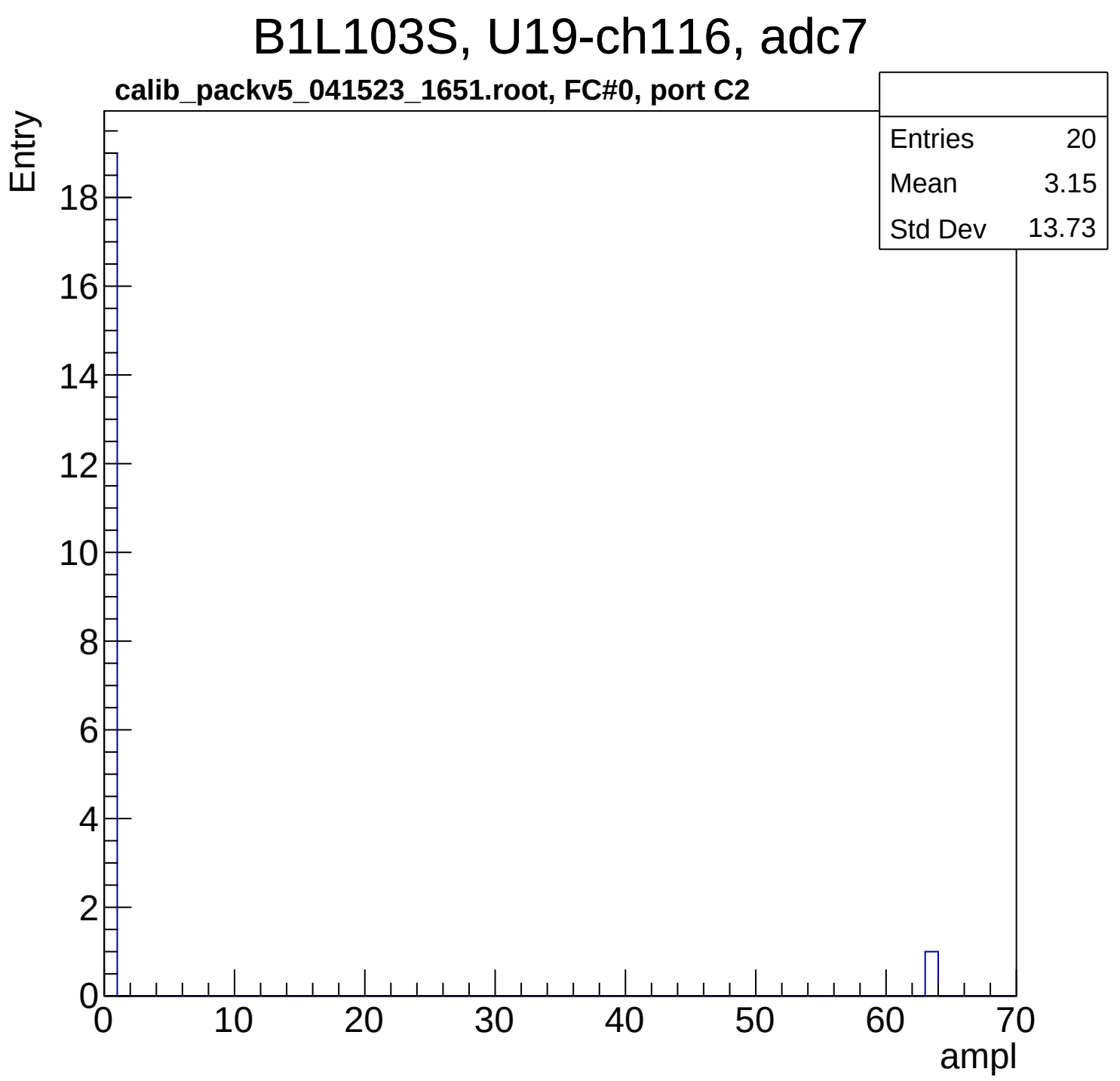
B1L103S, U19-ch116, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
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6
8
10
12
14
16
18
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10
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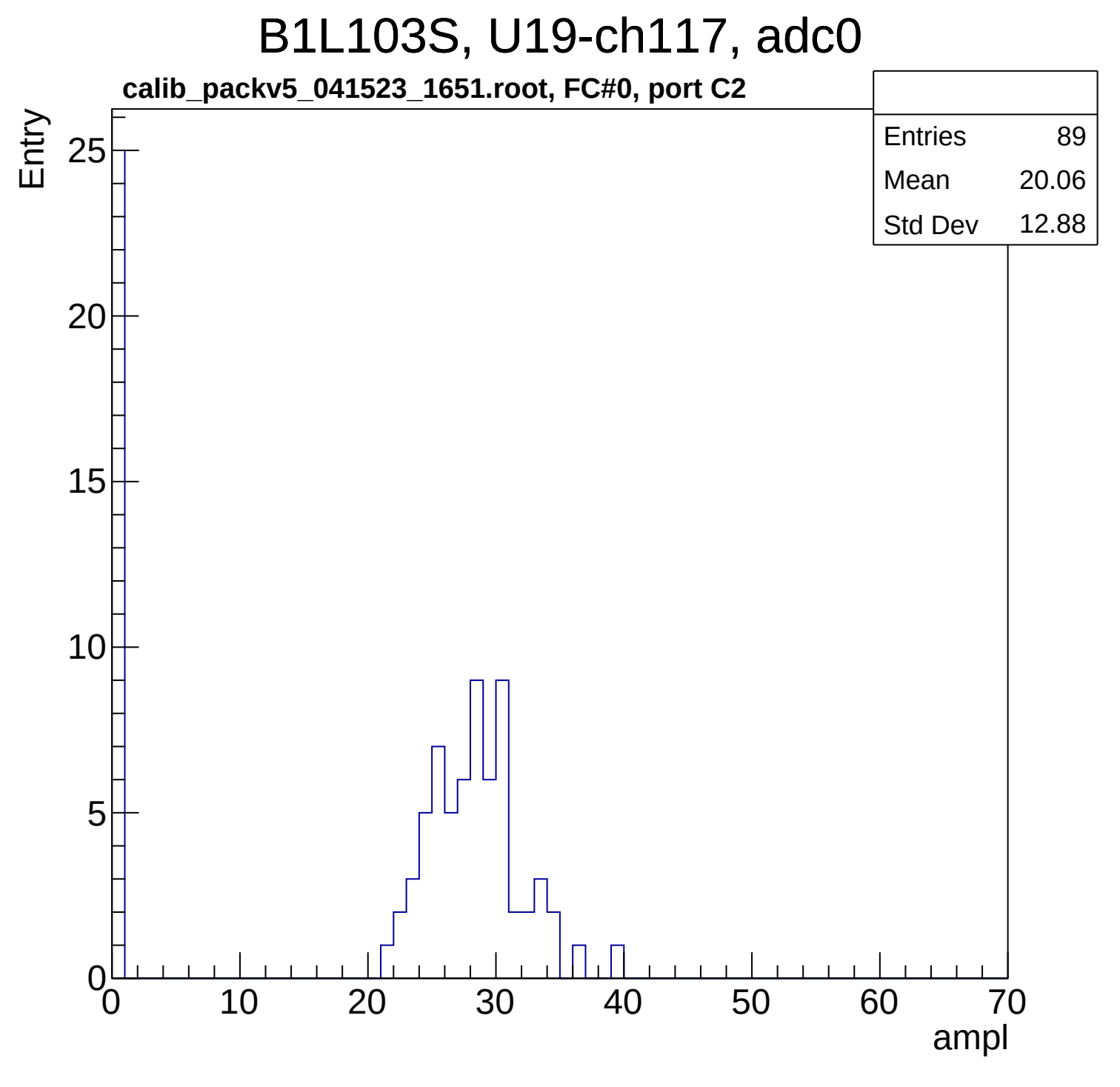
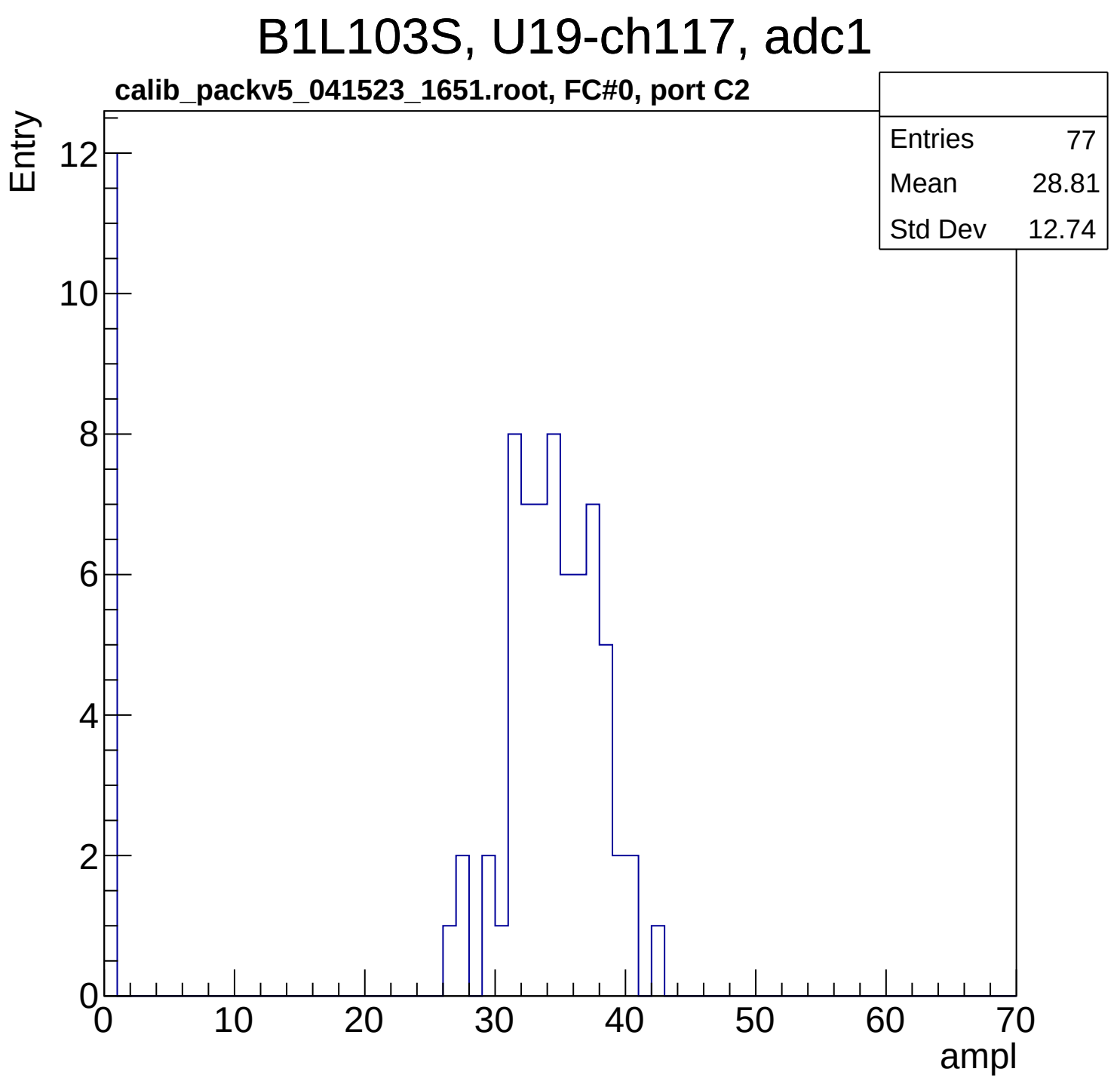
40
50
60
70
ampl


B1L103S, U19-ch117, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 20.06
Std Dev 12.88
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch117, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 28.81
Std Dev 12.74
Entry
0
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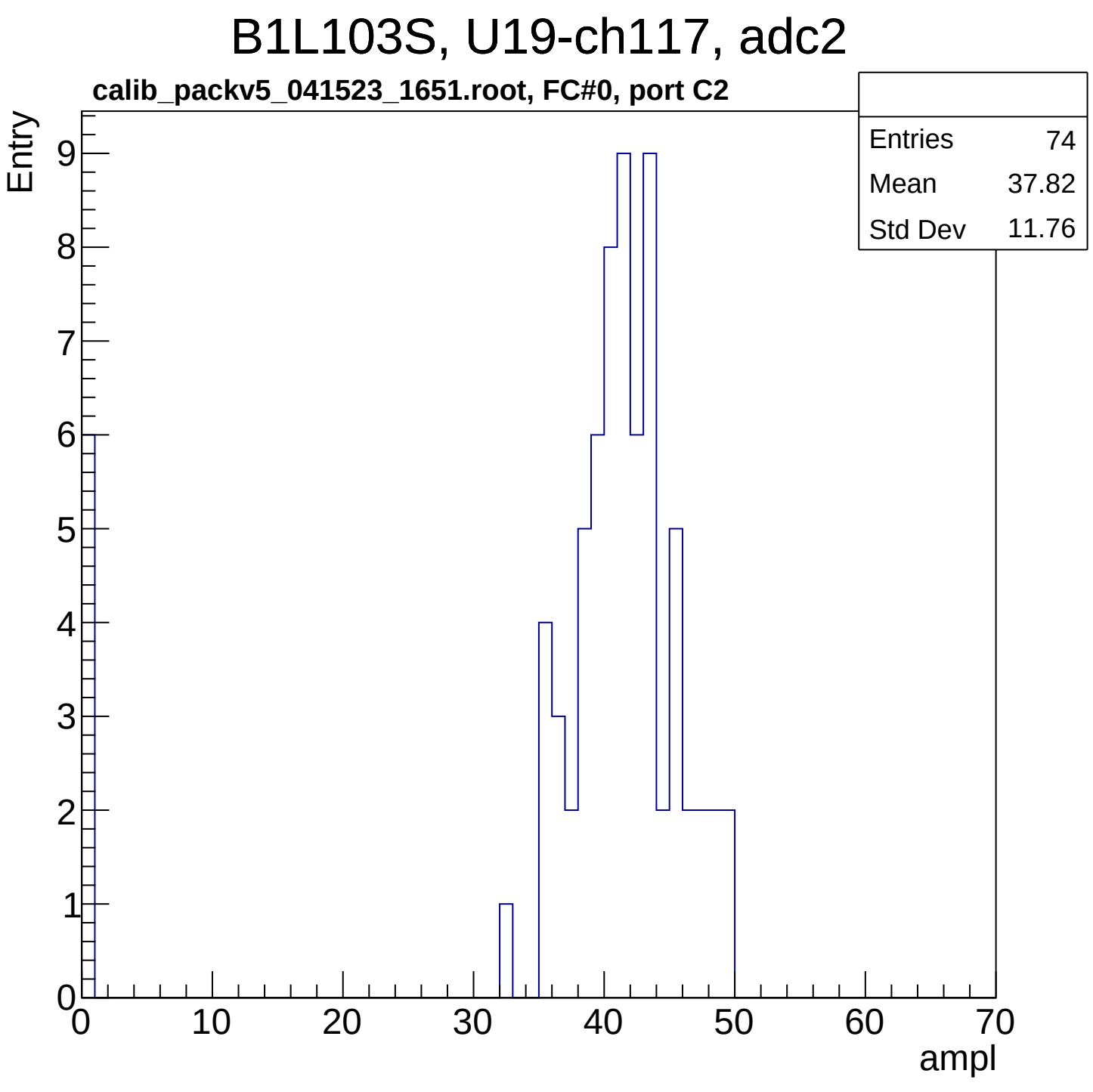
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch117, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 37.82
Std Dev 11.76
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
50
60
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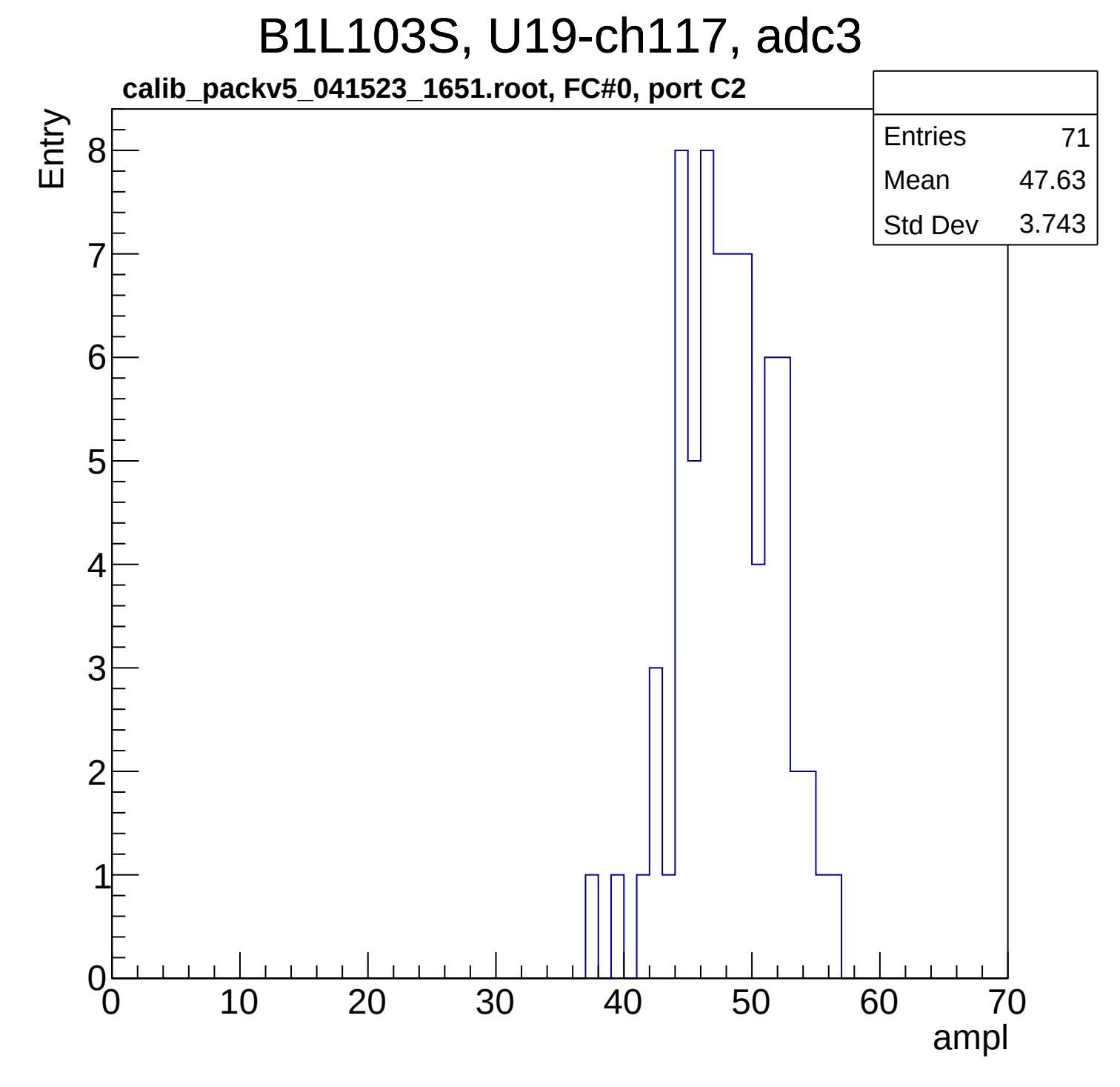
B1L103S, U19-ch117, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 47.63
Std Dev 3.743
Entry
ampl
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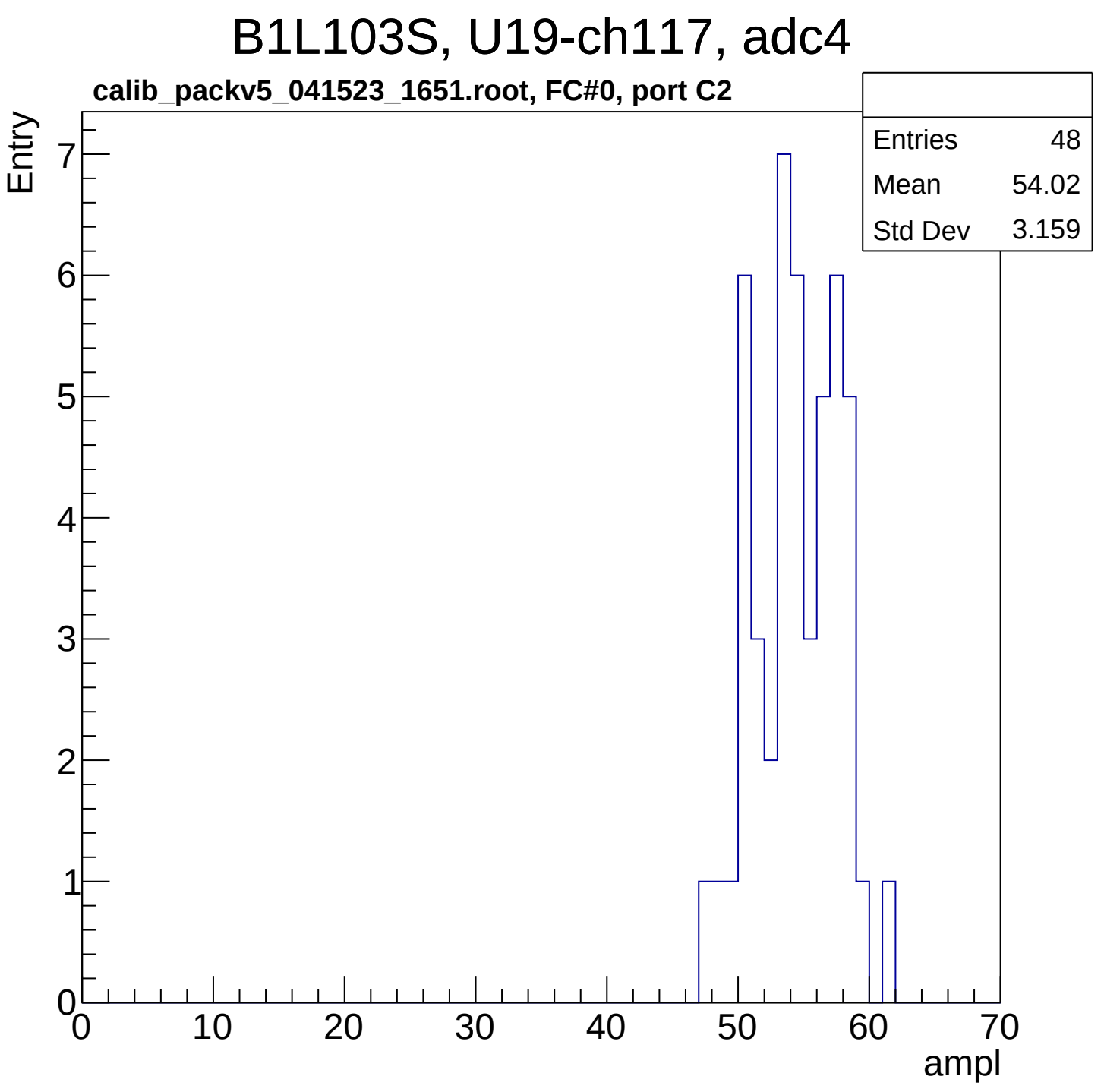
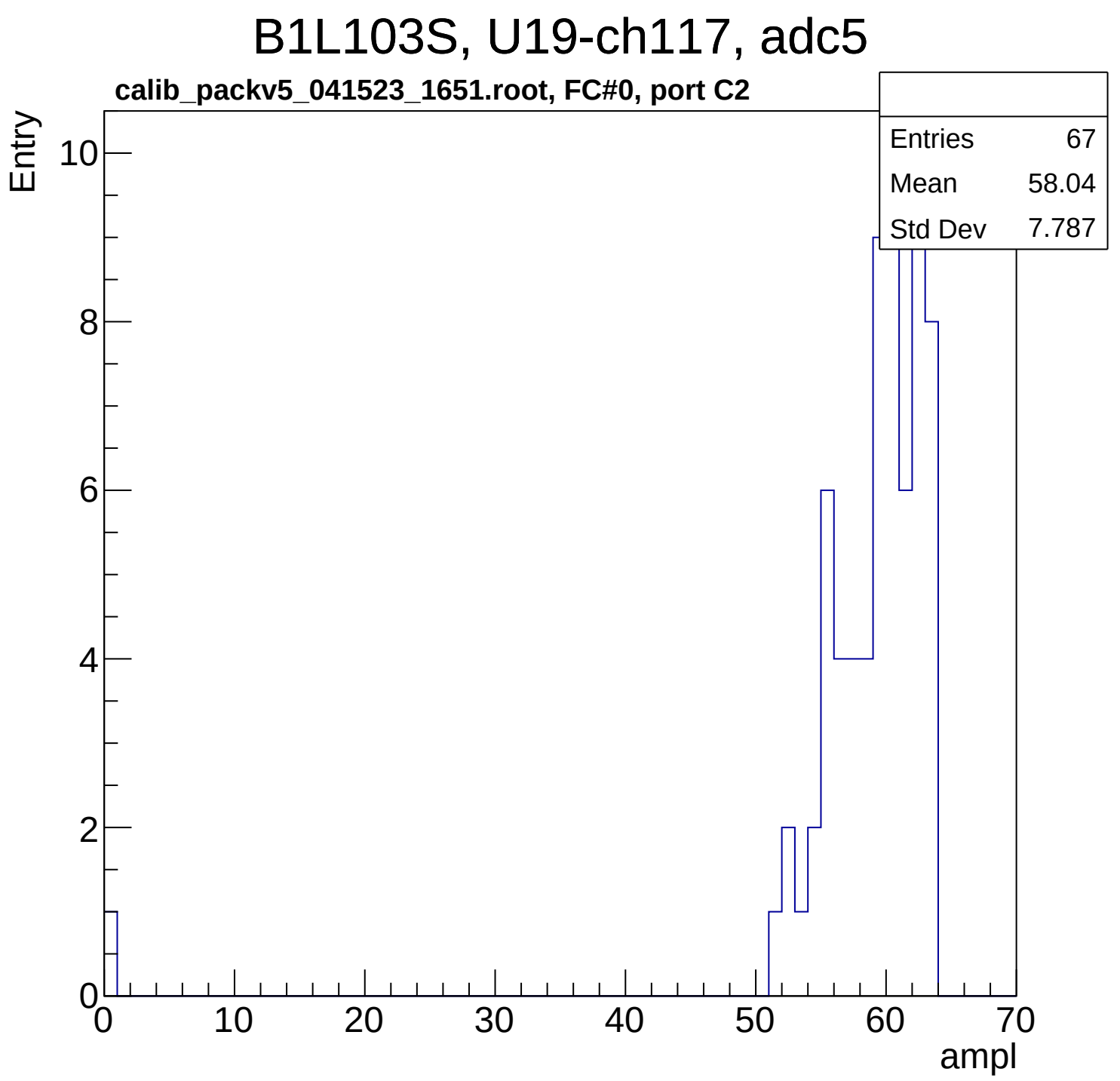
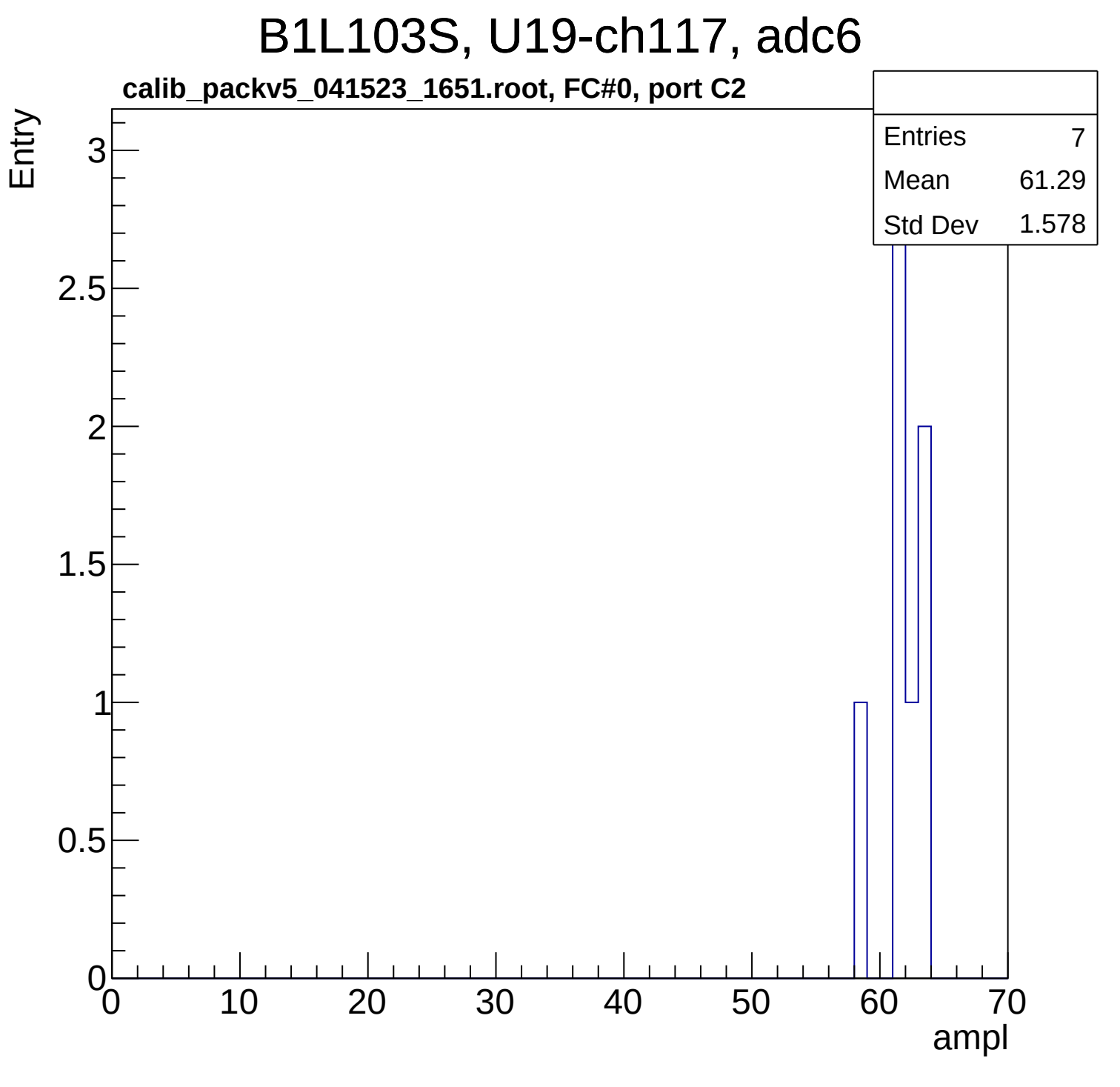
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch117, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 54.02
Std Dev 3.159
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch117, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 58.04
Std Dev 7.787
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch117, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 61.29
Std Dev 1.578
Entry
ampl
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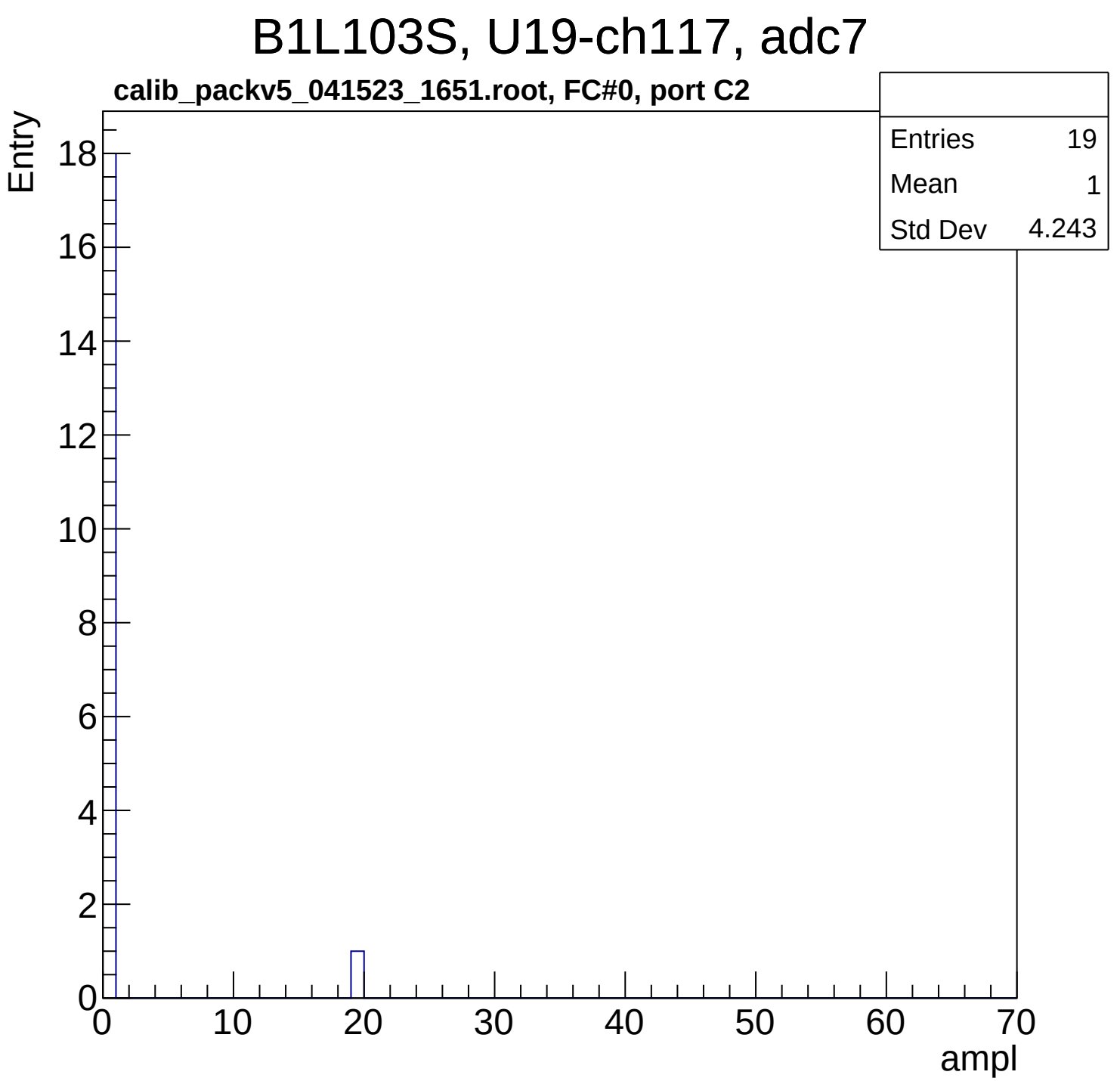
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U19-ch117, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1
Std Dev 4.243
Entry
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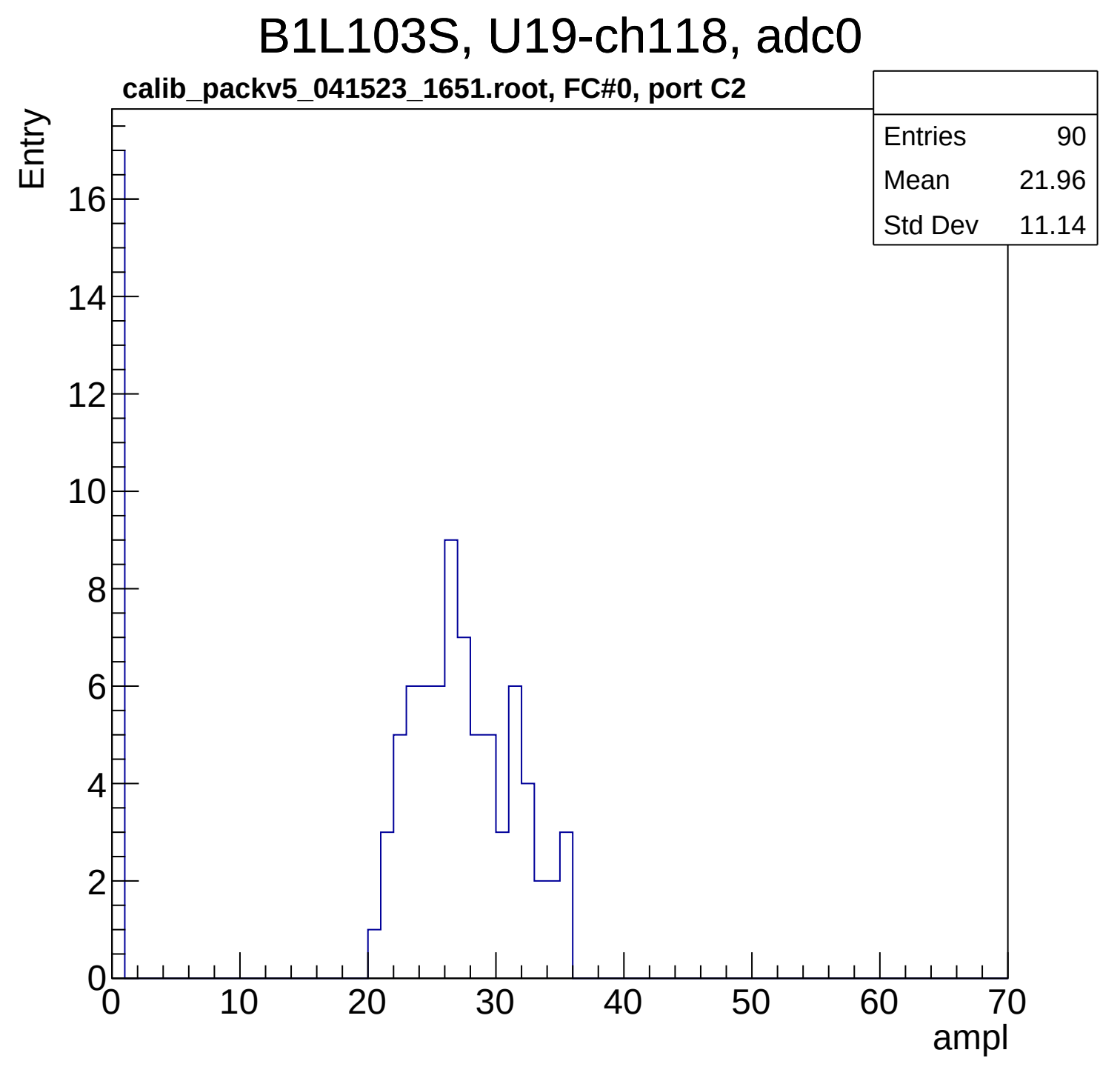
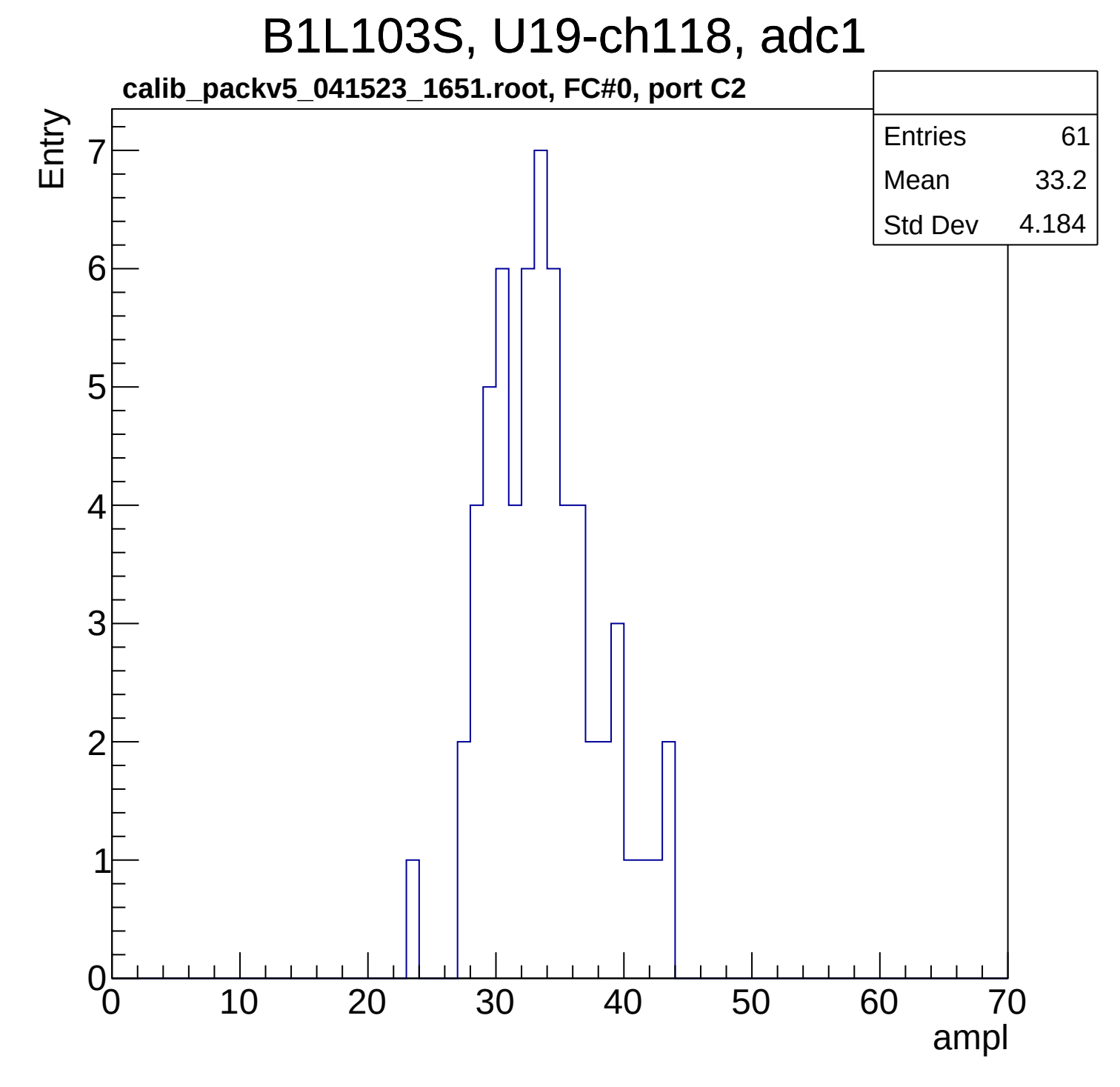
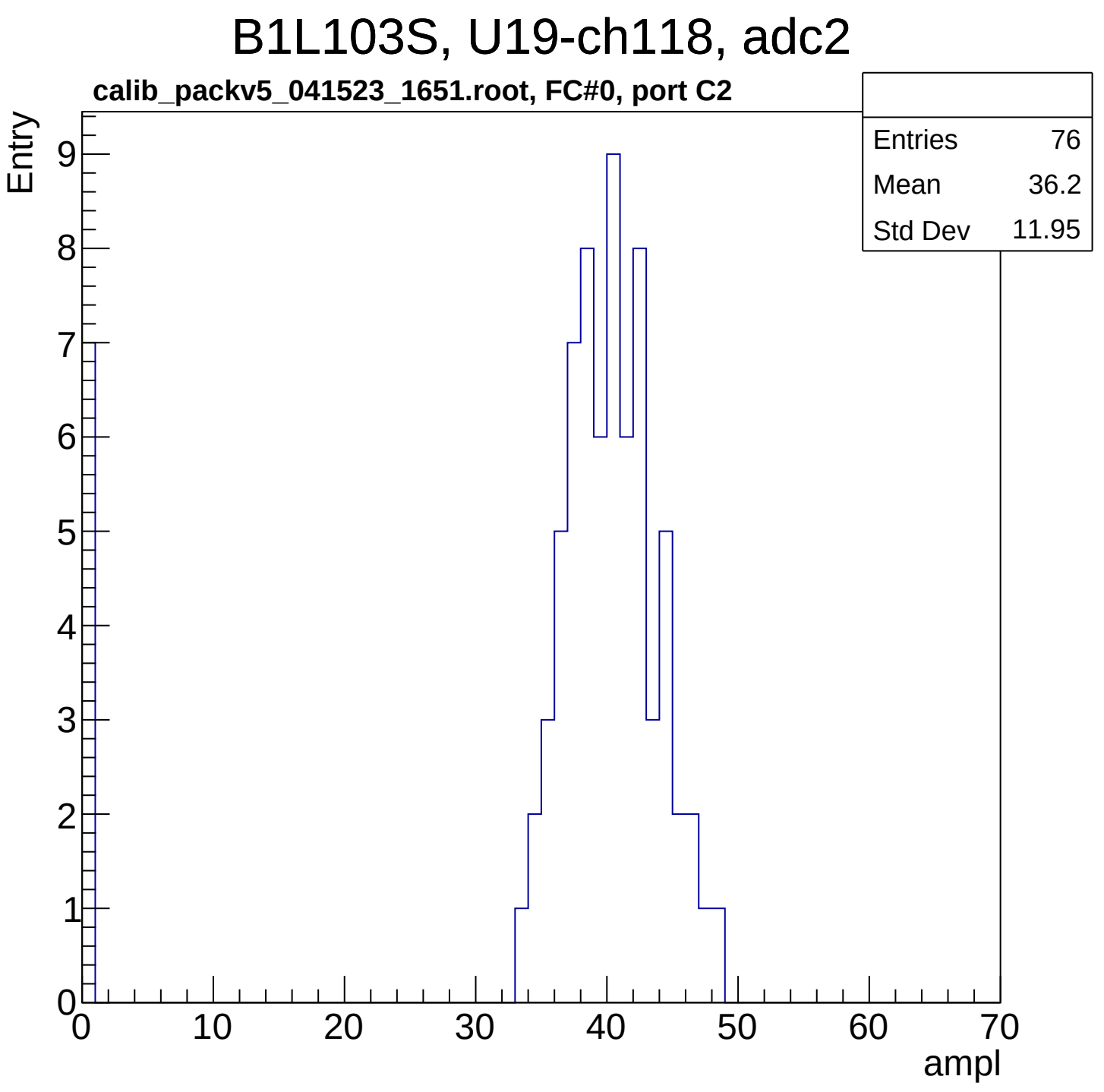
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch118, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 21.96
Std Dev 11.14
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch118, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 33.2
Std Dev 4.184
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch118, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 36.2
Std Dev 11.95
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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30
40
50
60
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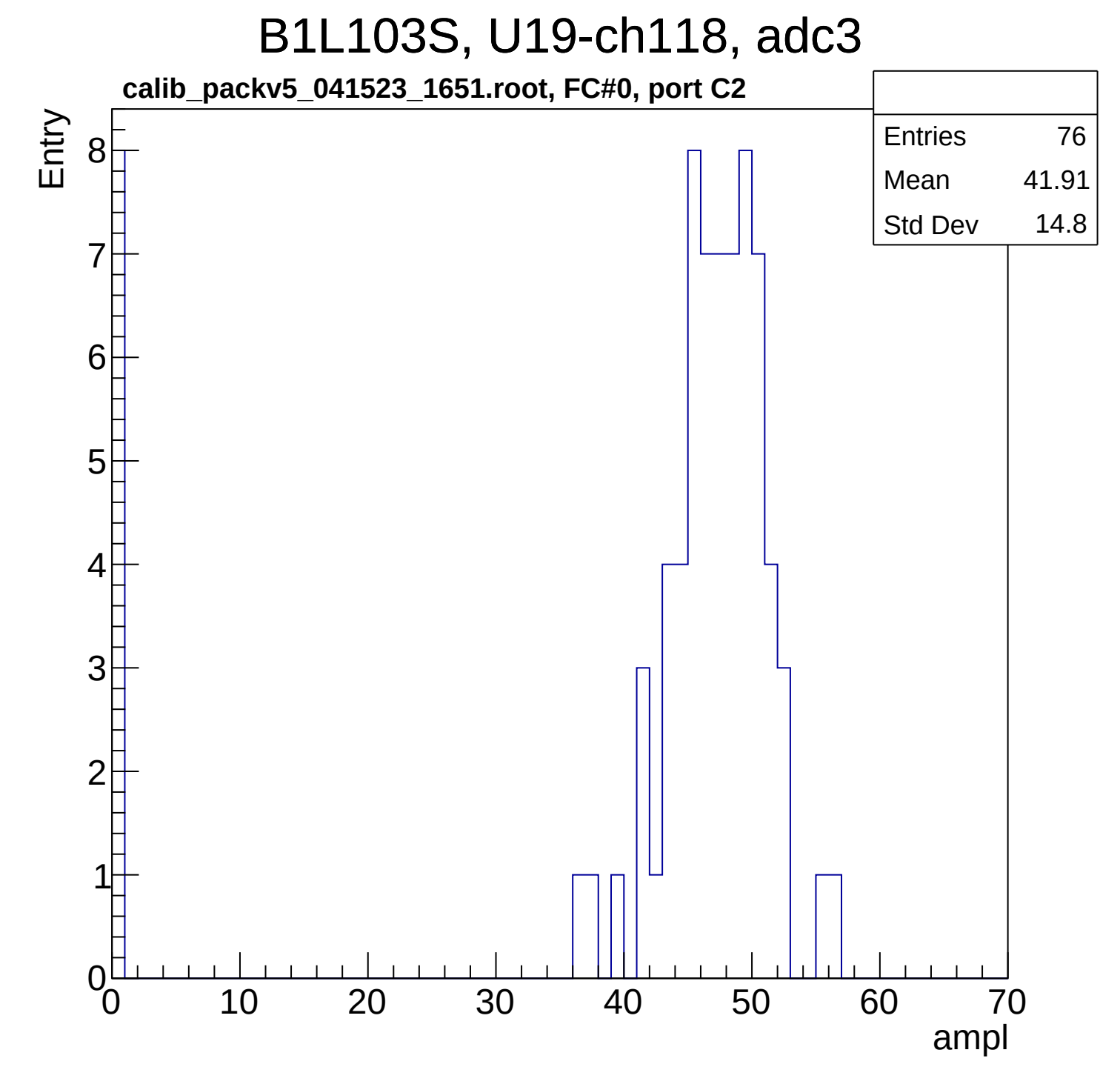
B1L103S, U19-ch118, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 41.91
Std Dev 14.8
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
50
60
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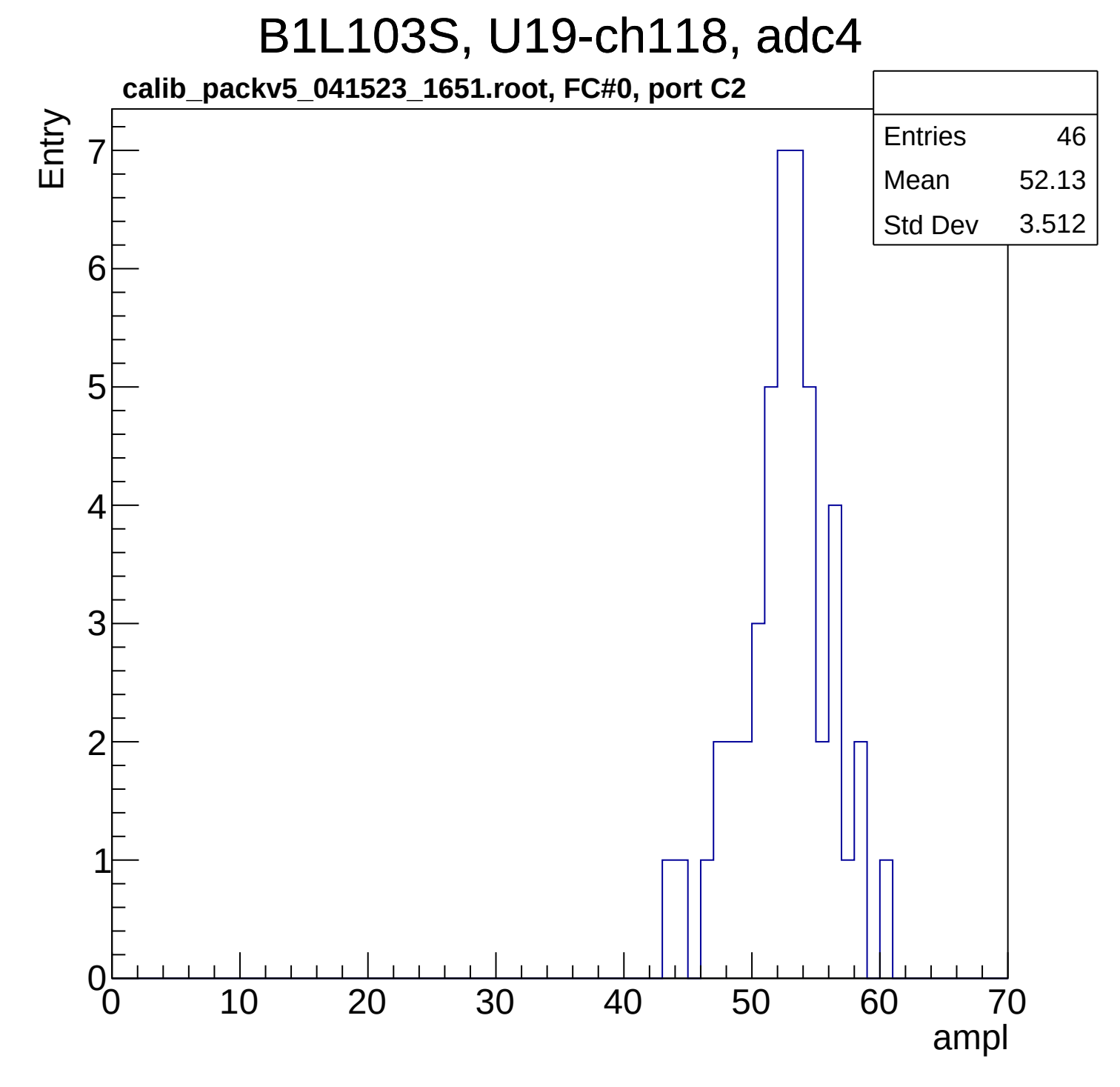
B1L103S, U19-ch118, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 52.13
Std Dev 3.512
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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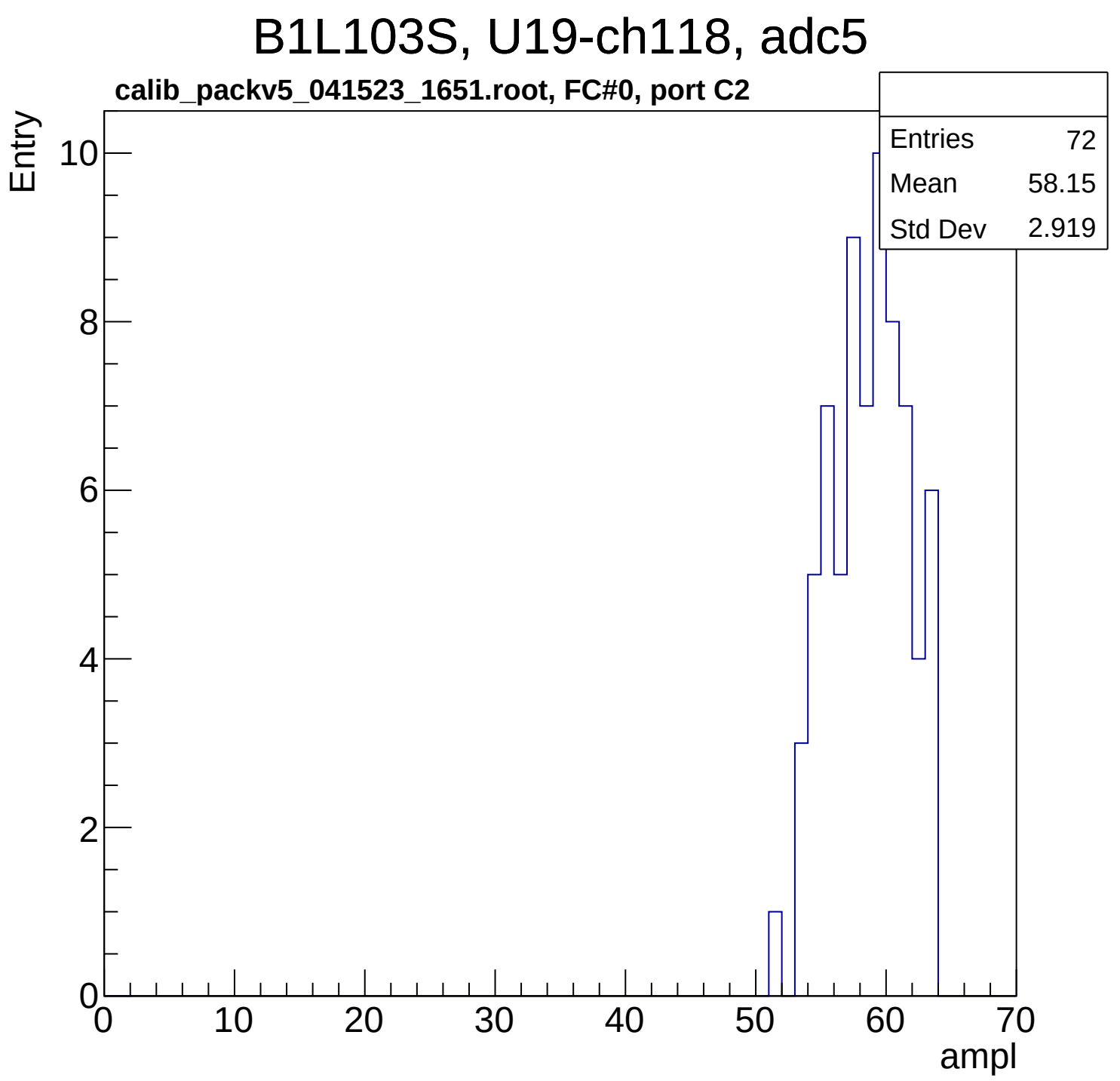
B1L103S, U19-ch118, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 58.15
Std Dev 2.919
Entry
ampl
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2
4
6
8
10
0
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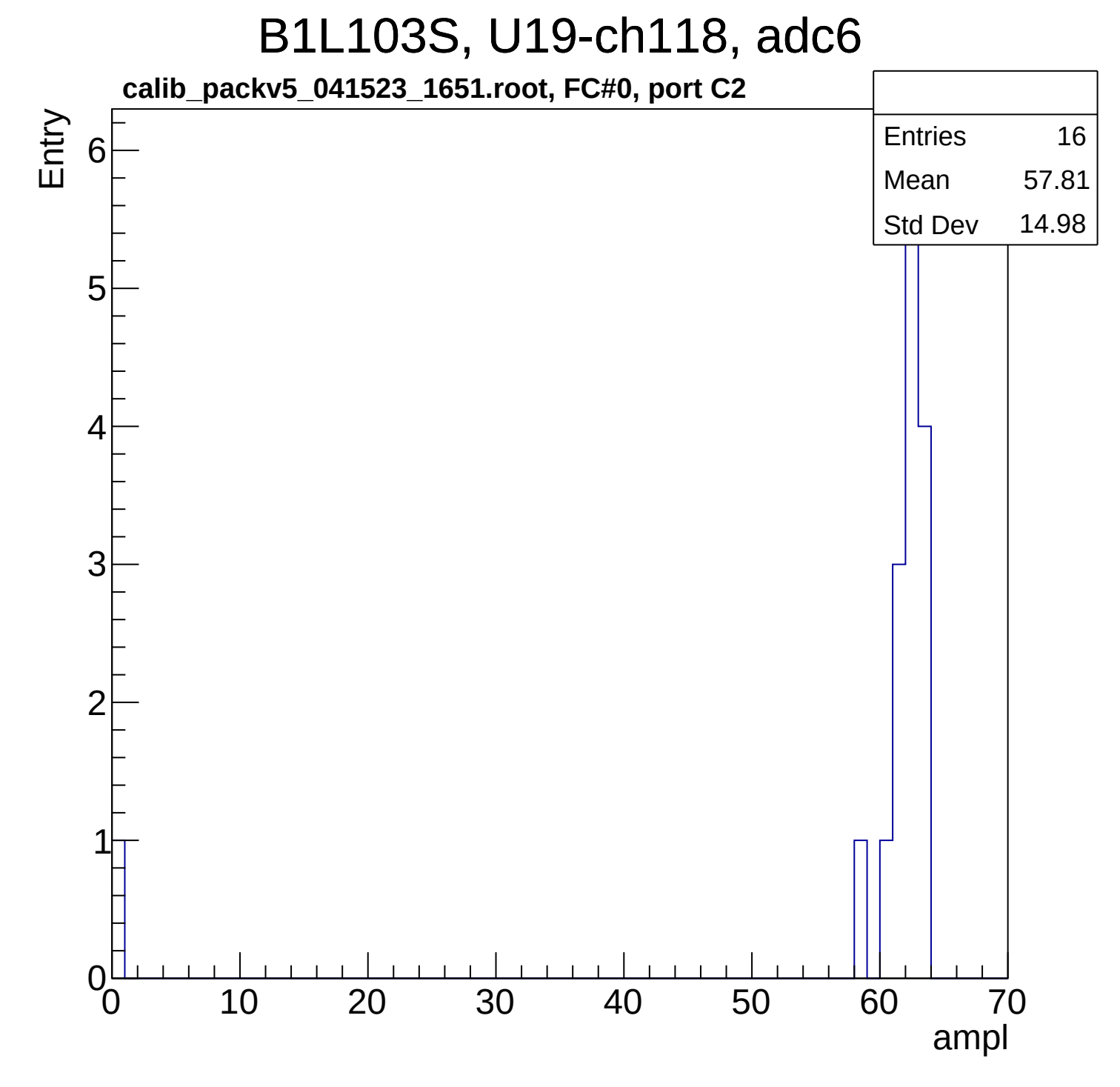
B1L103S, U19-ch118, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 57.81
Std Dev 14.98
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
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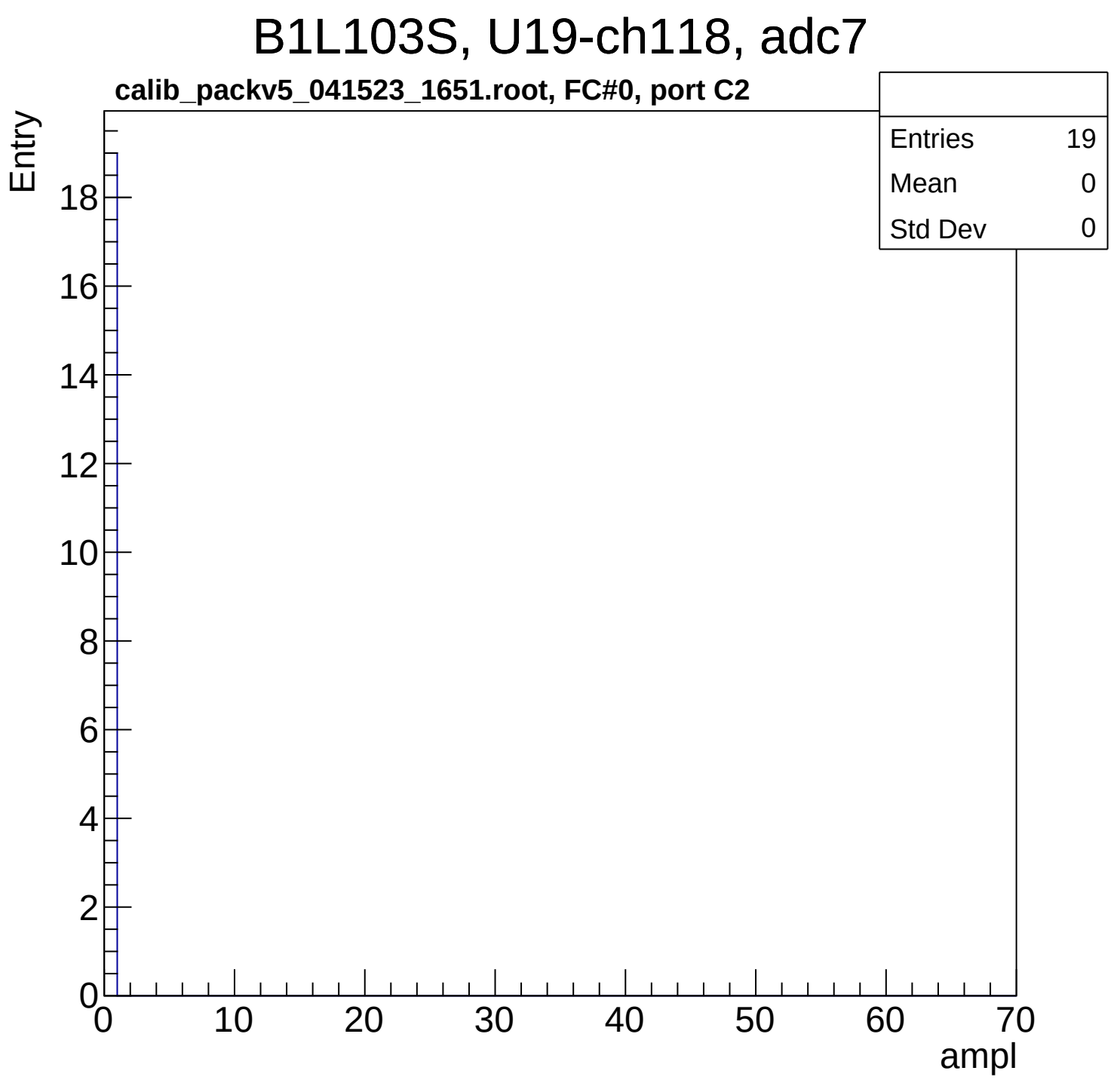
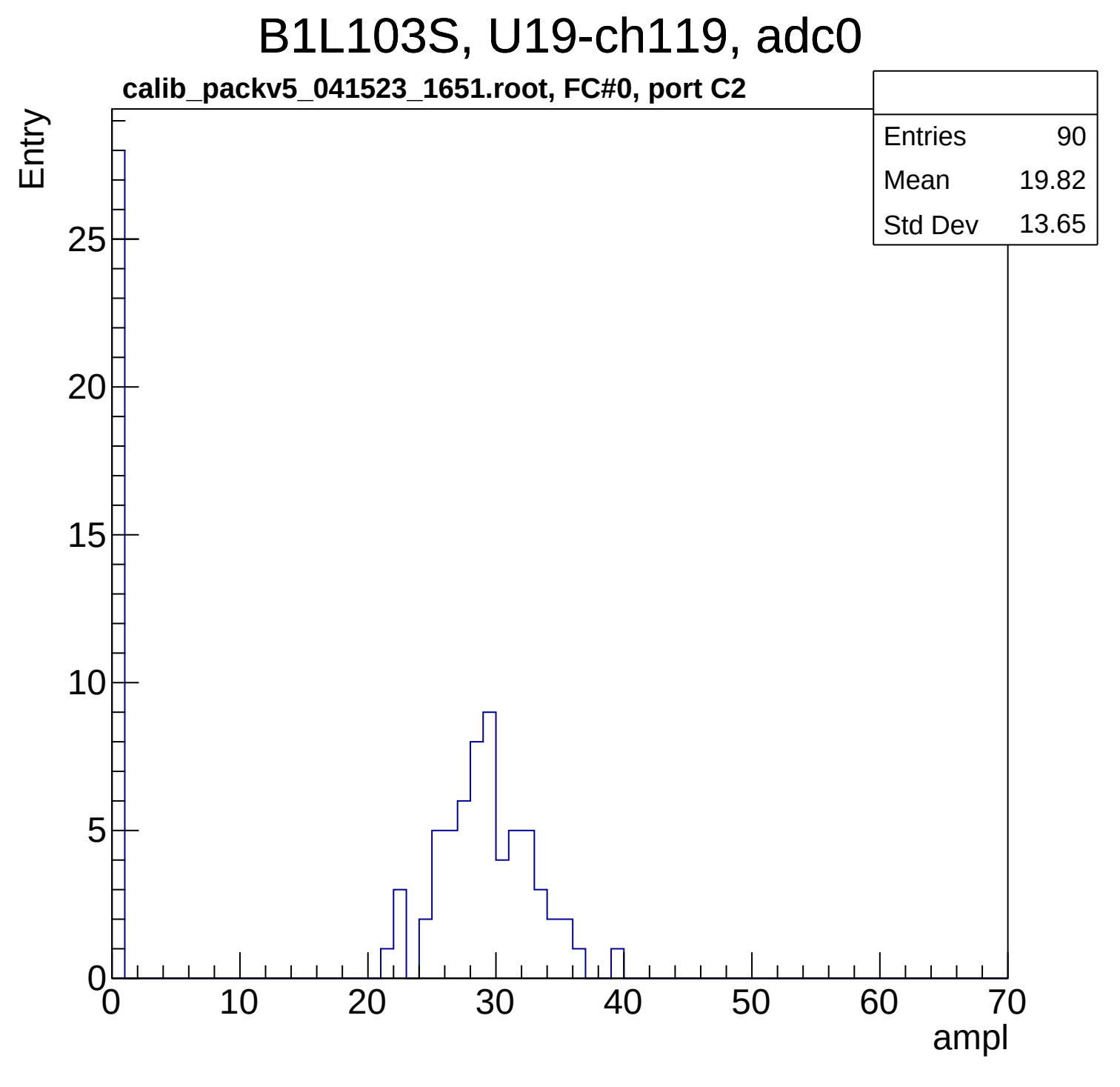
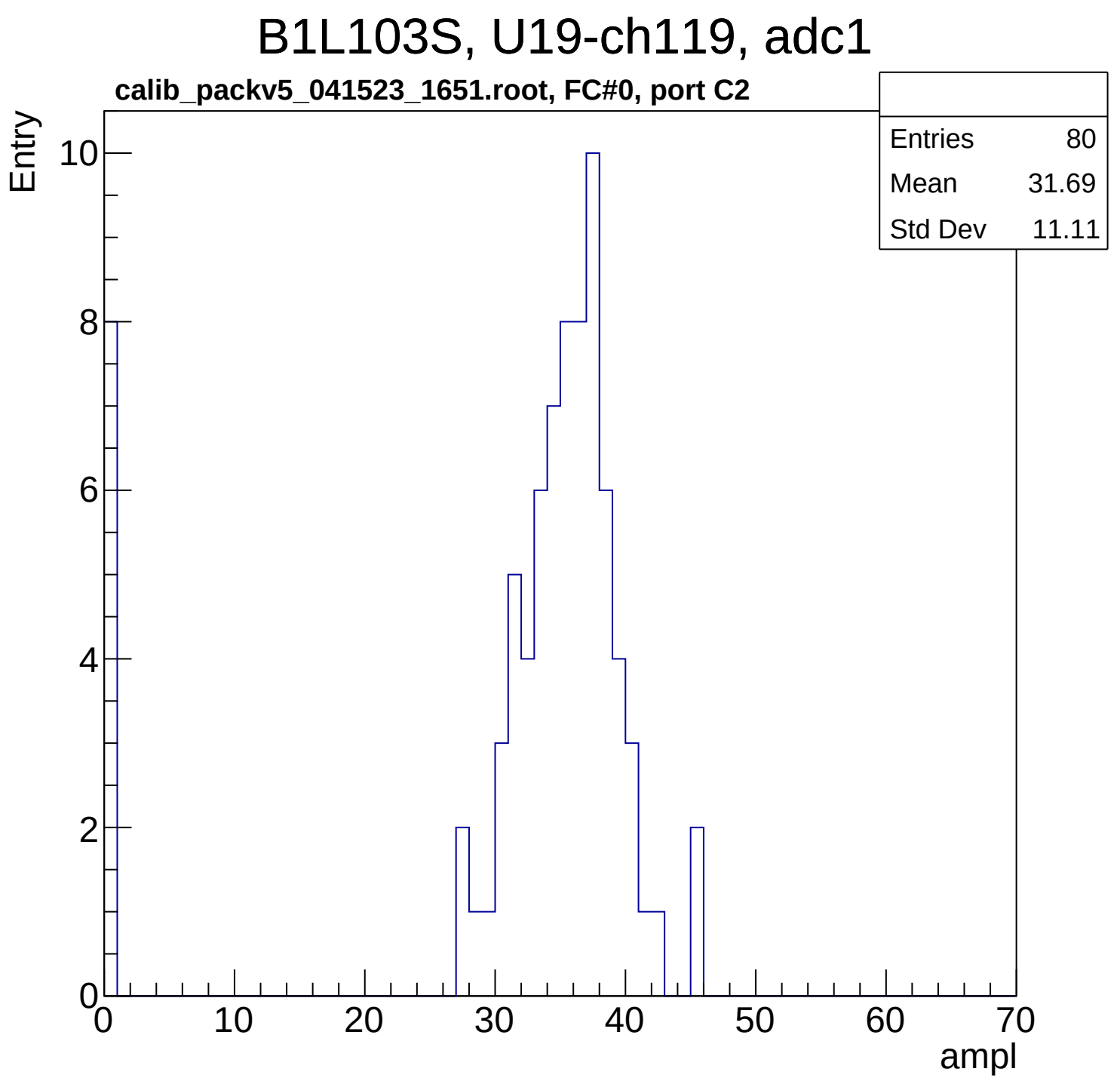

B1L103S, U19-ch118, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch119, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 19.82
Std Dev 13.65
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch119, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 31.69
Std Dev 11.11
Entry
ampl
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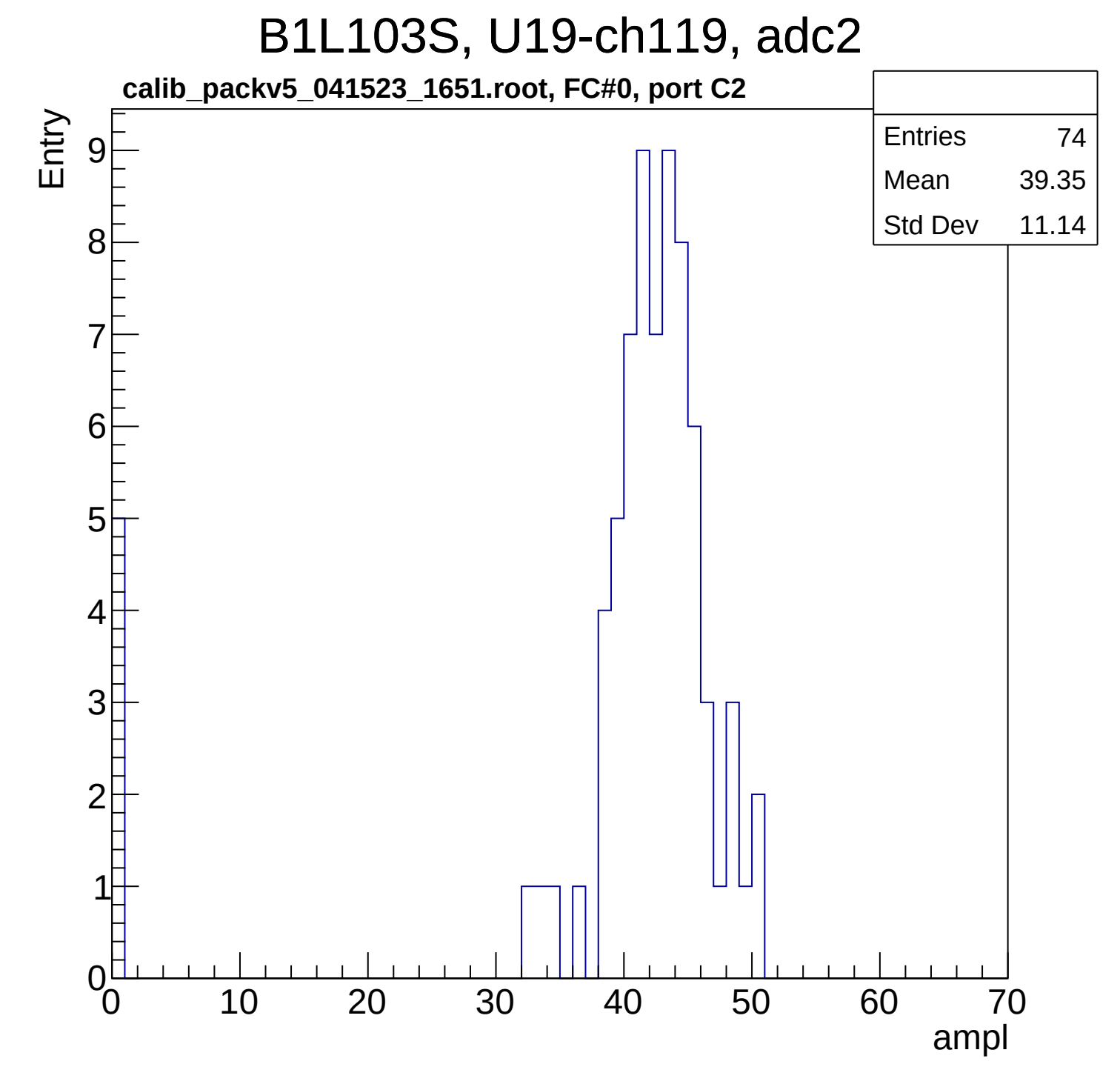
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U19-ch119, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 39.35
Std Dev 11.14
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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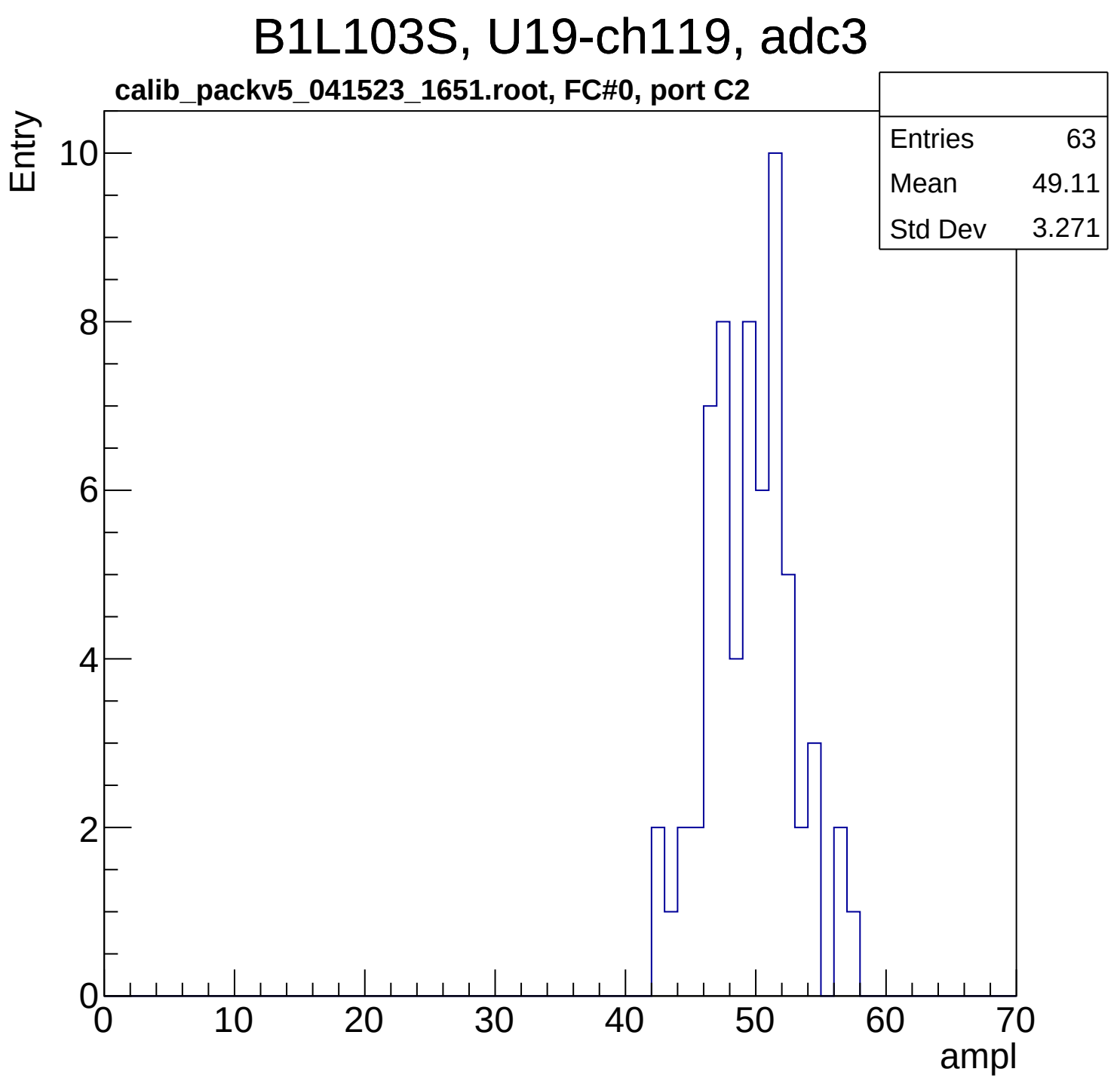
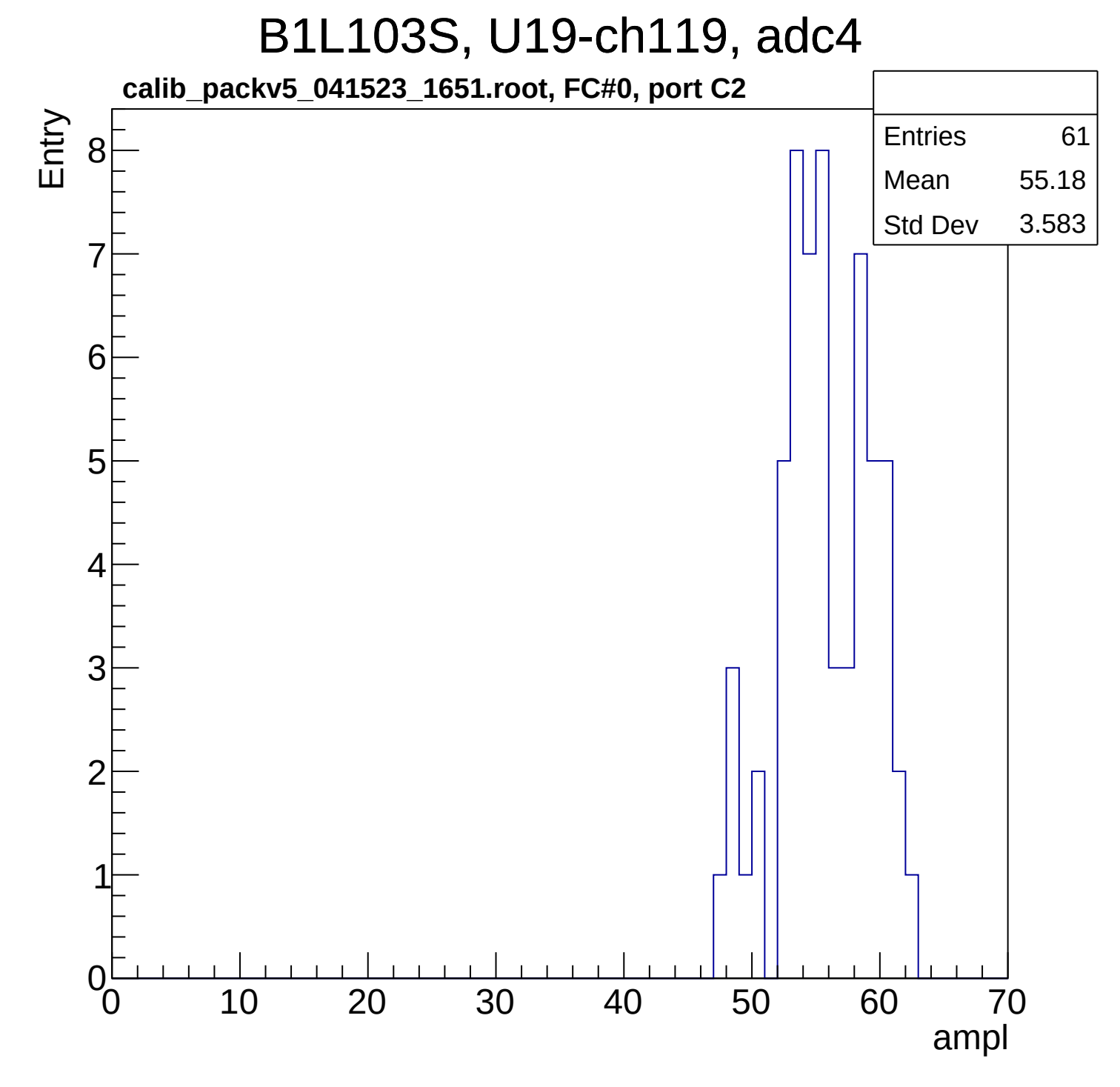

B1L103S, U19-ch119, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 49.11
Std Dev 3.271
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch119, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 55.18
Std Dev 3.583
Entry
ampl
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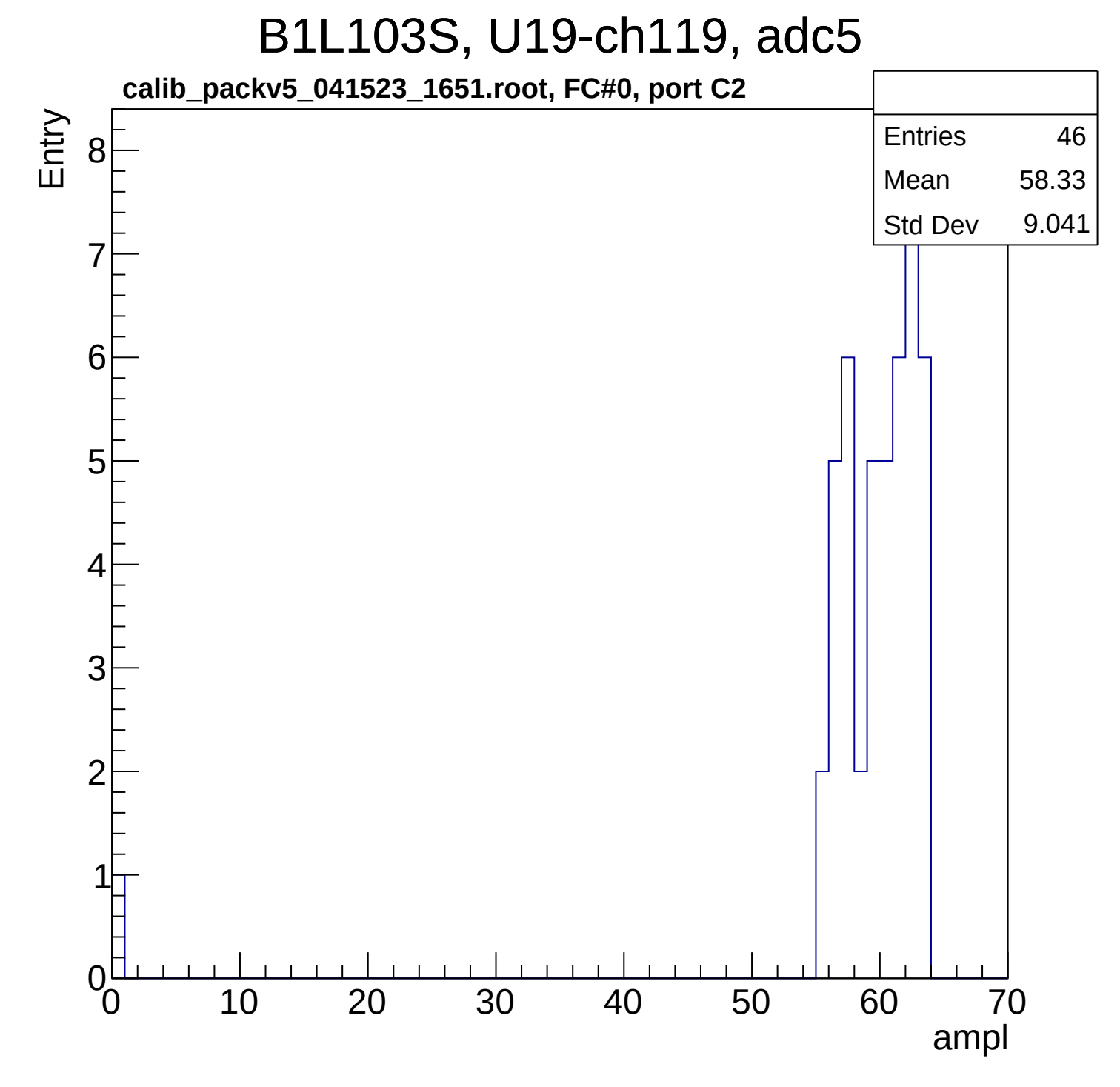
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch119, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 58.33
Std Dev 9.041
Entry
ampl
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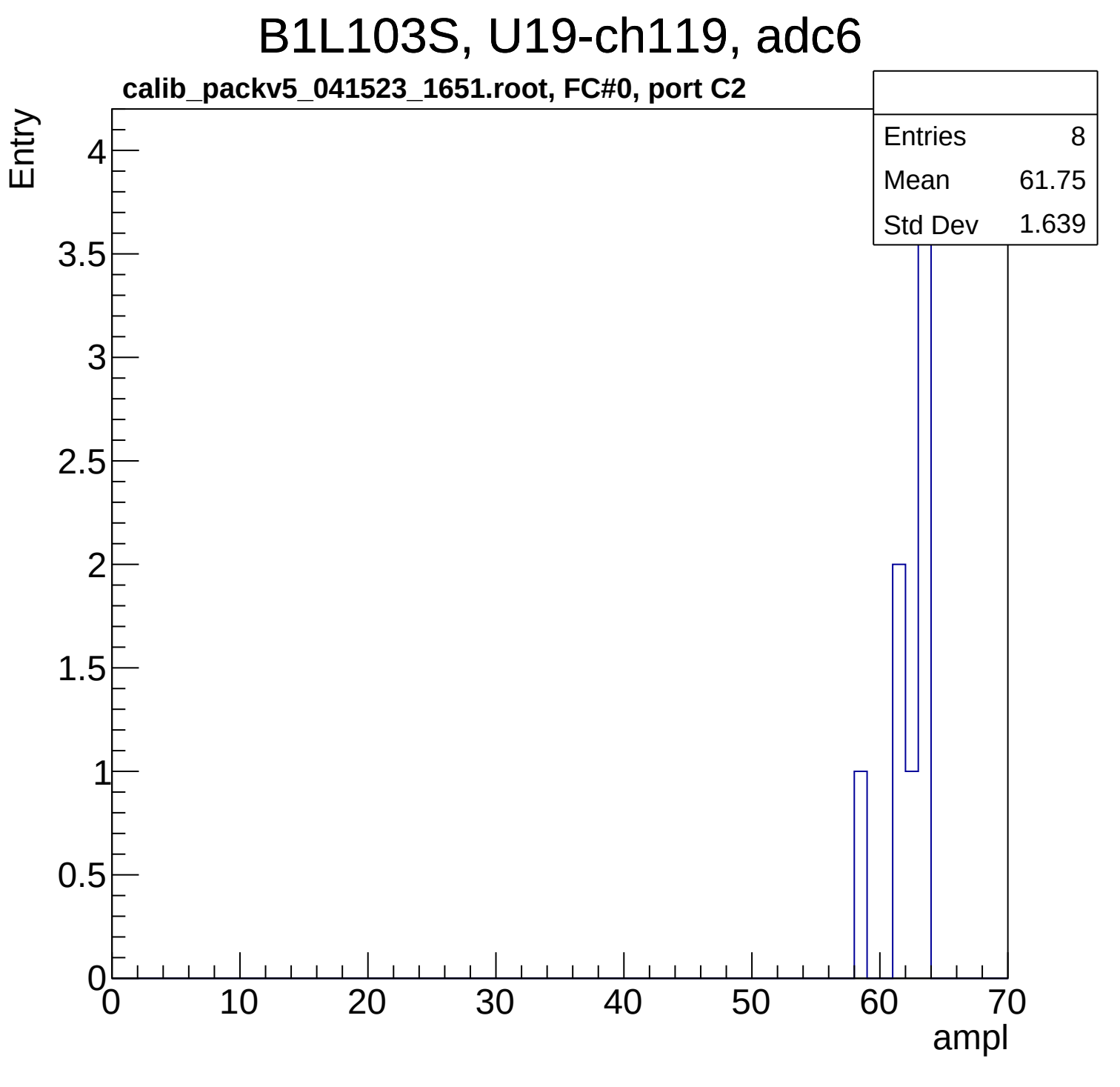
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch119, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 61.75
Std Dev 1.639
Entry
ampl
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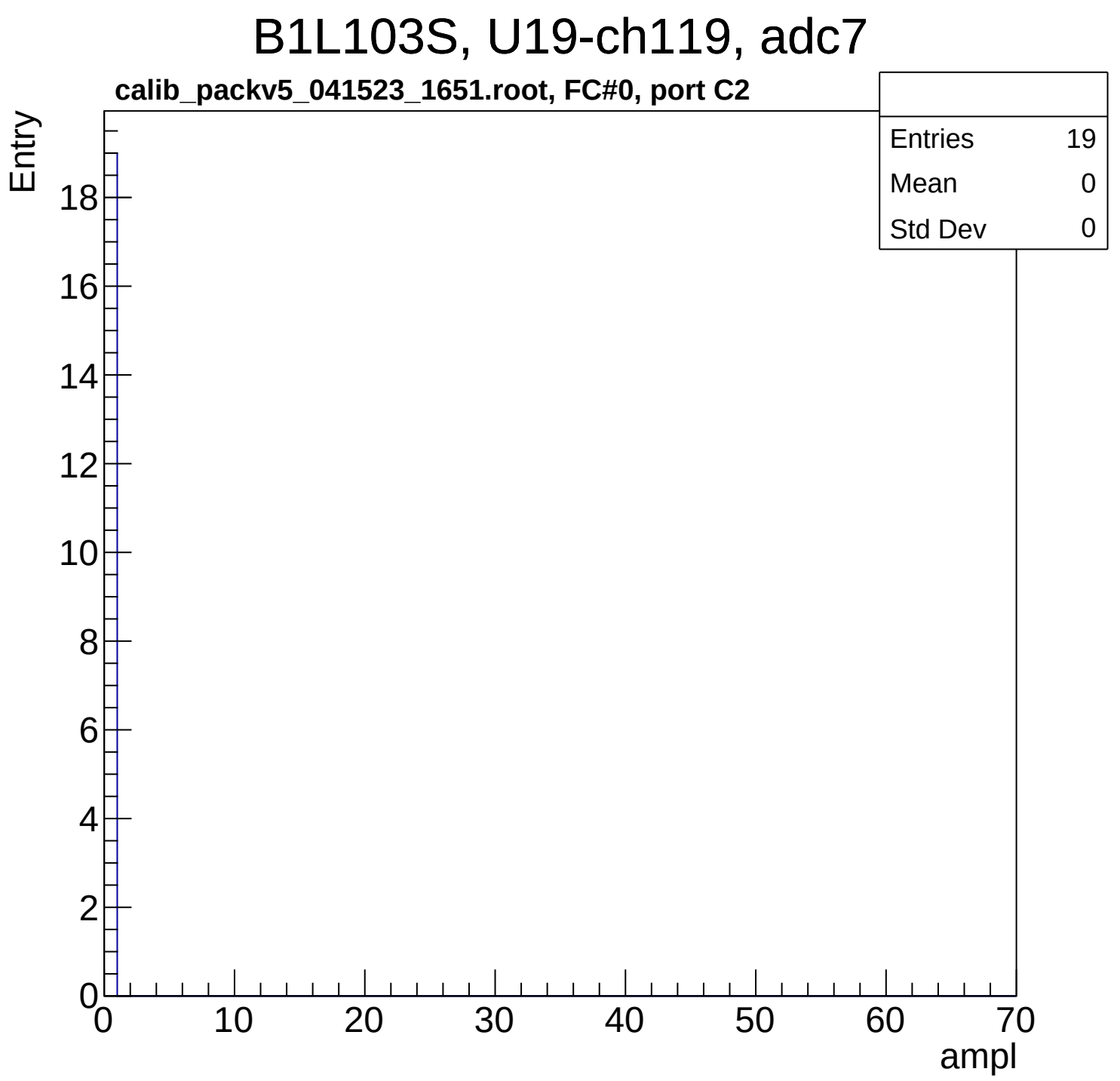
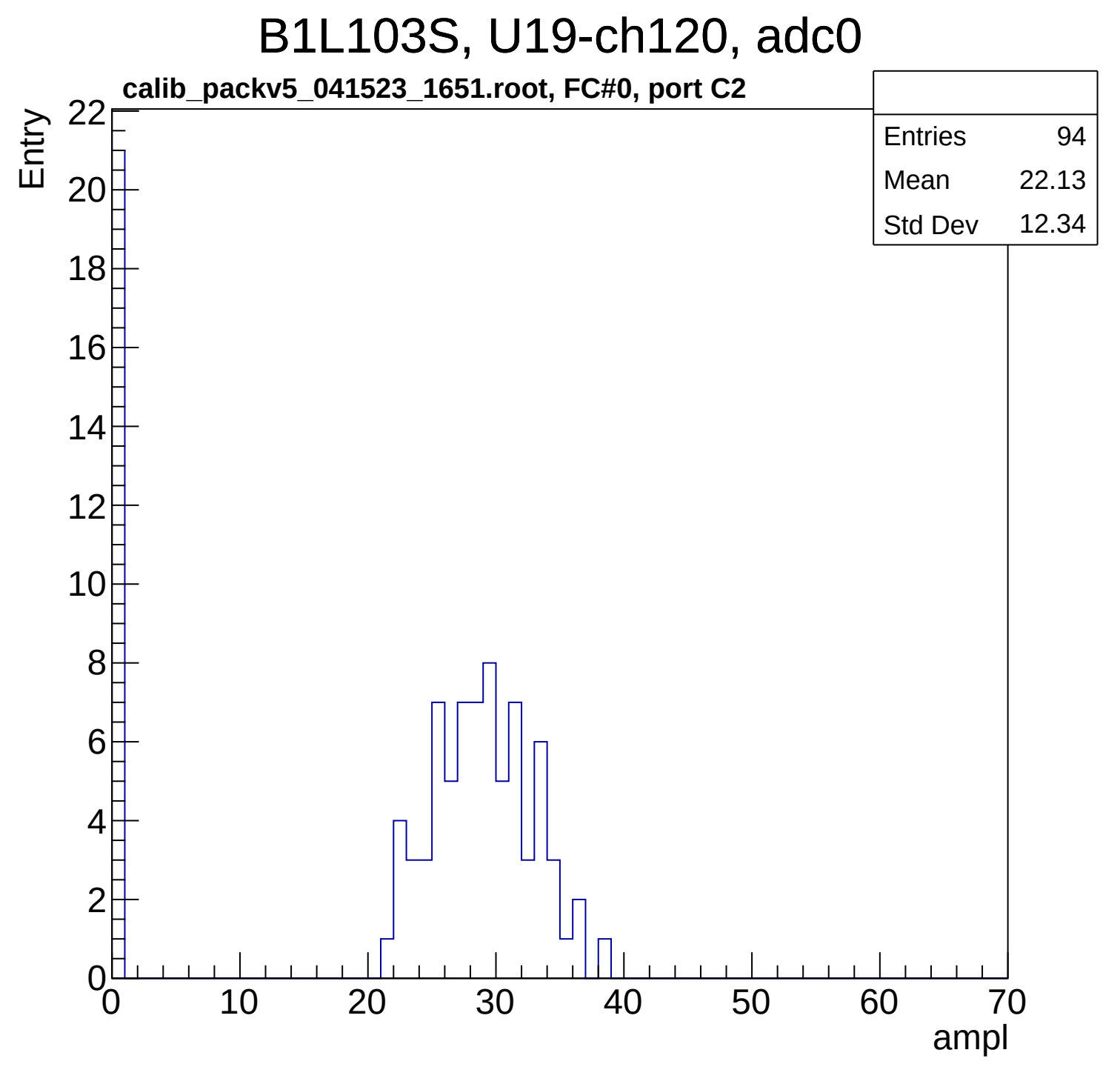
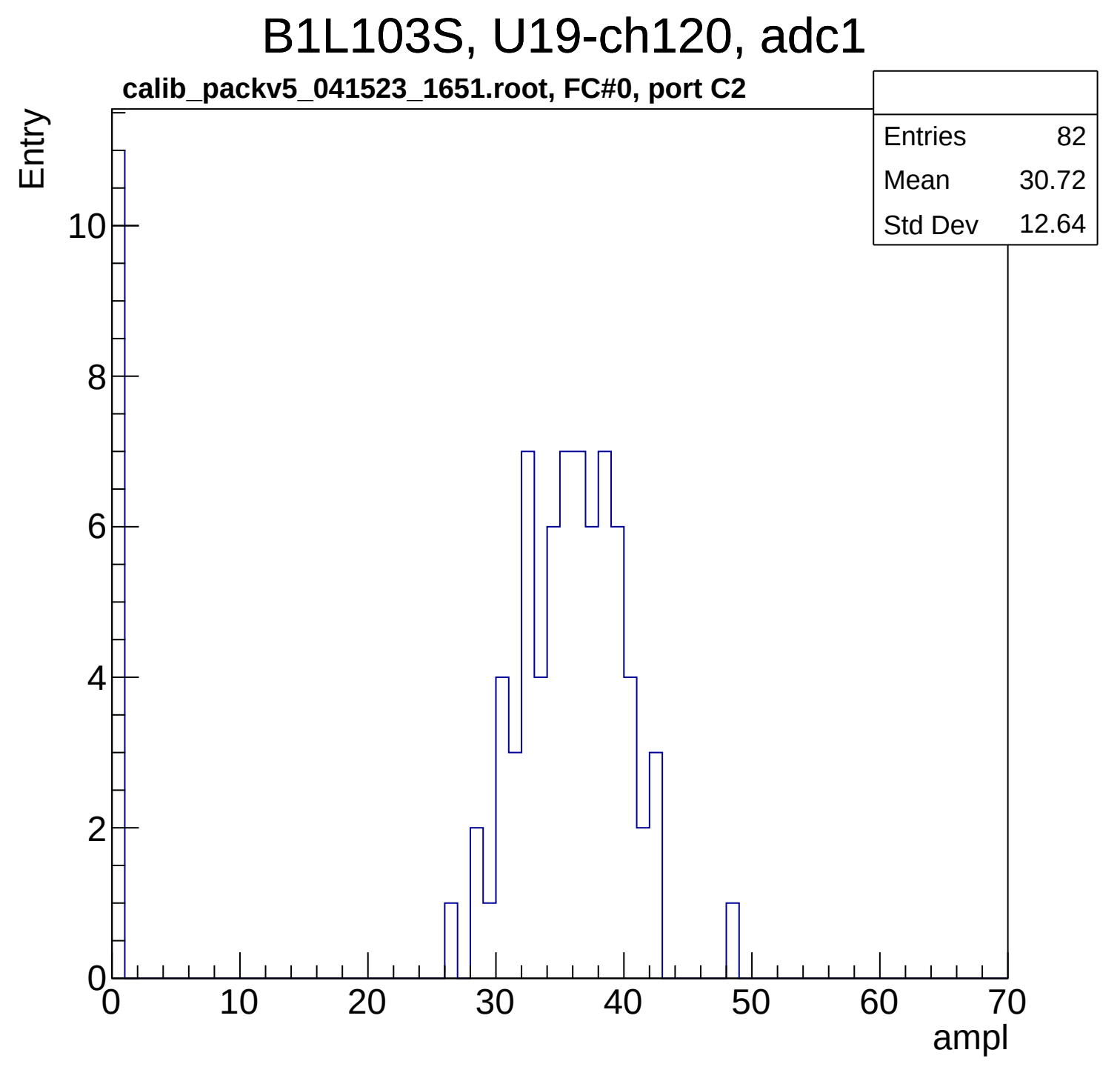
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U19-ch119, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch120, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 22.13
Std Dev 12.34
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70


B1L103S, U19-ch120, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 30.72
Std Dev 12.64
Entry
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6
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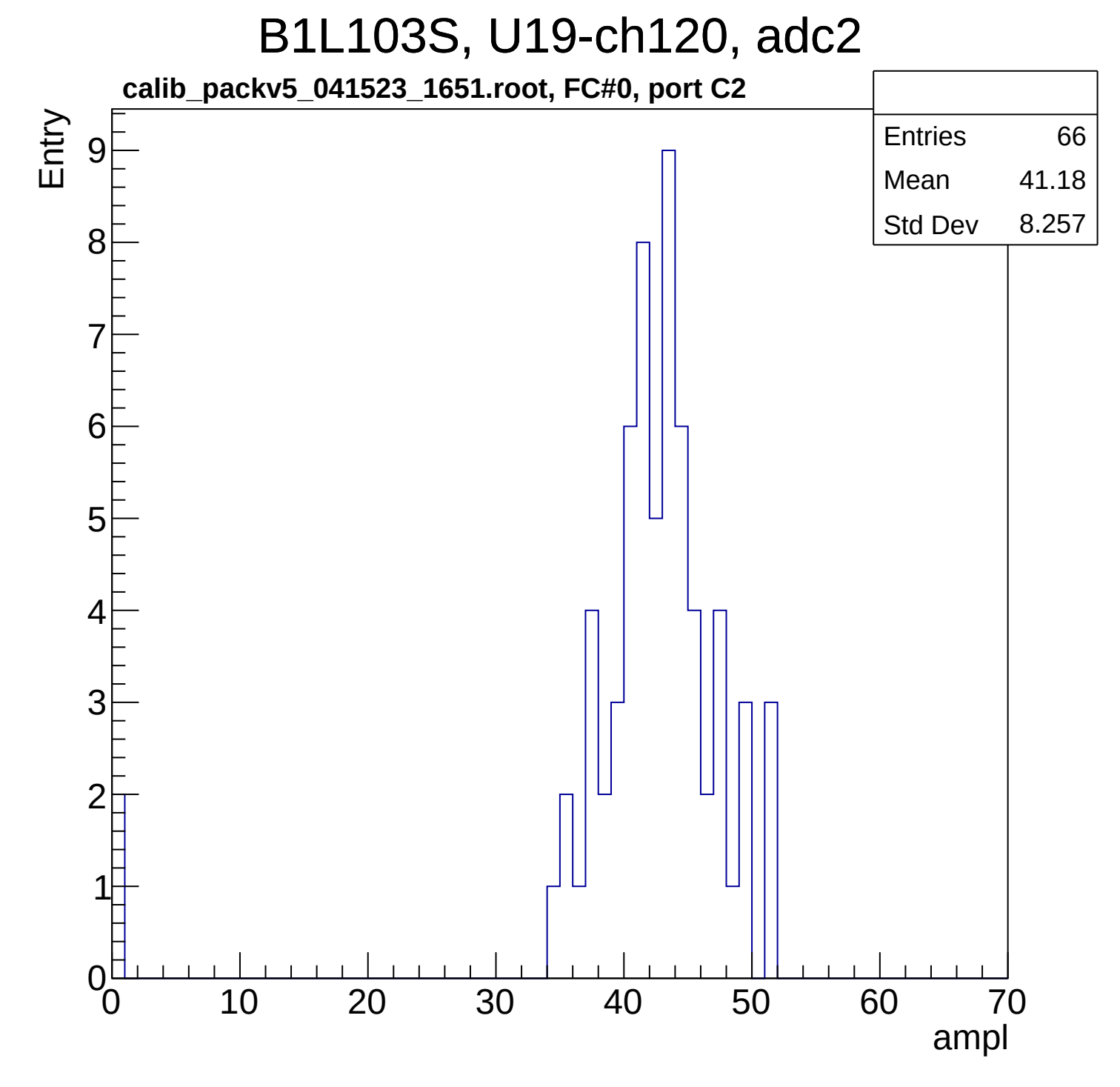
ampl


B1L103S, U19-ch120, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 41.18
Std Dev 8.257
Entry
ampl
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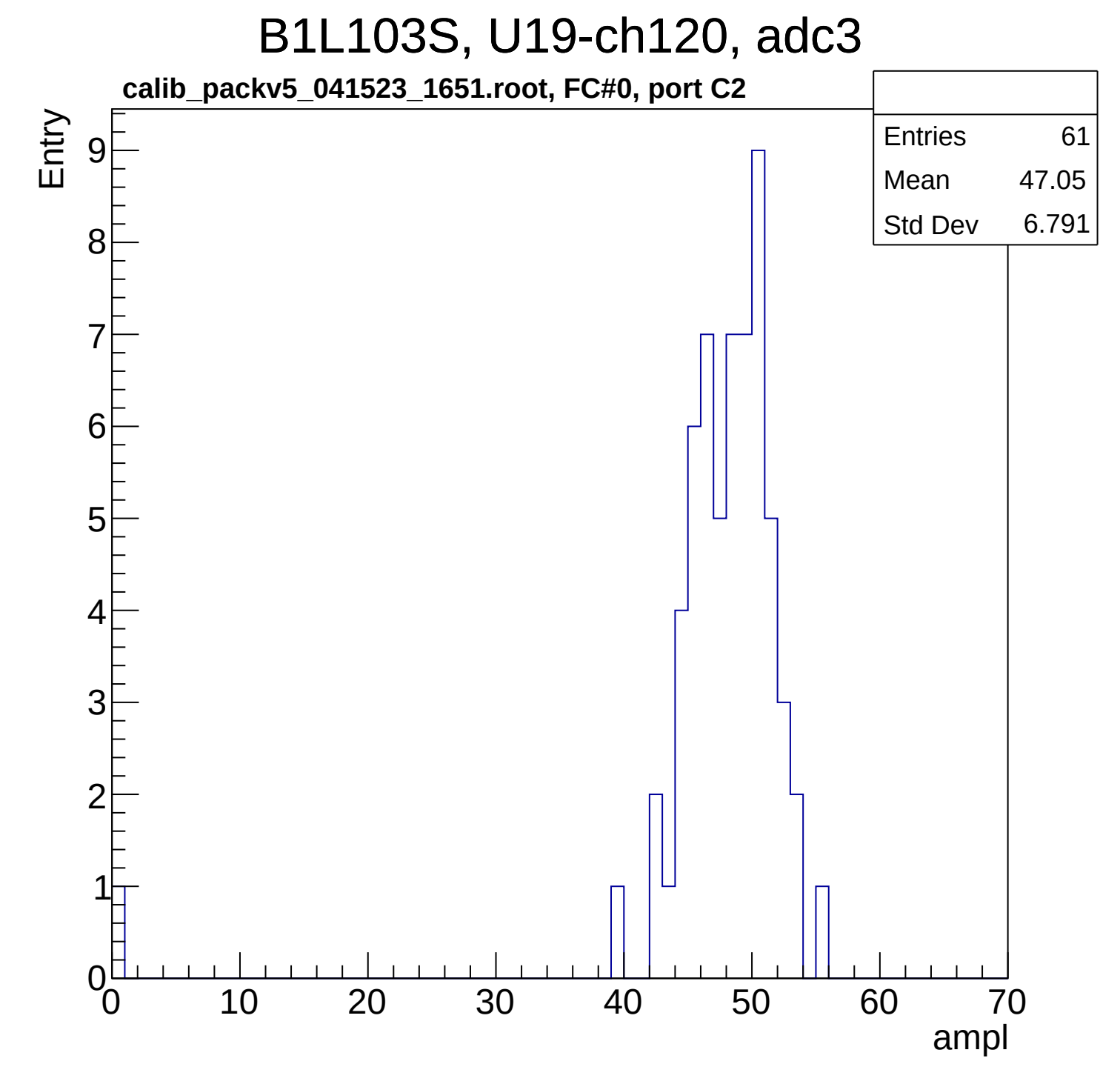
B1L103S, U19-ch120, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 47.05
Std Dev 6.791
Entry
ampl
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4
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8
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0
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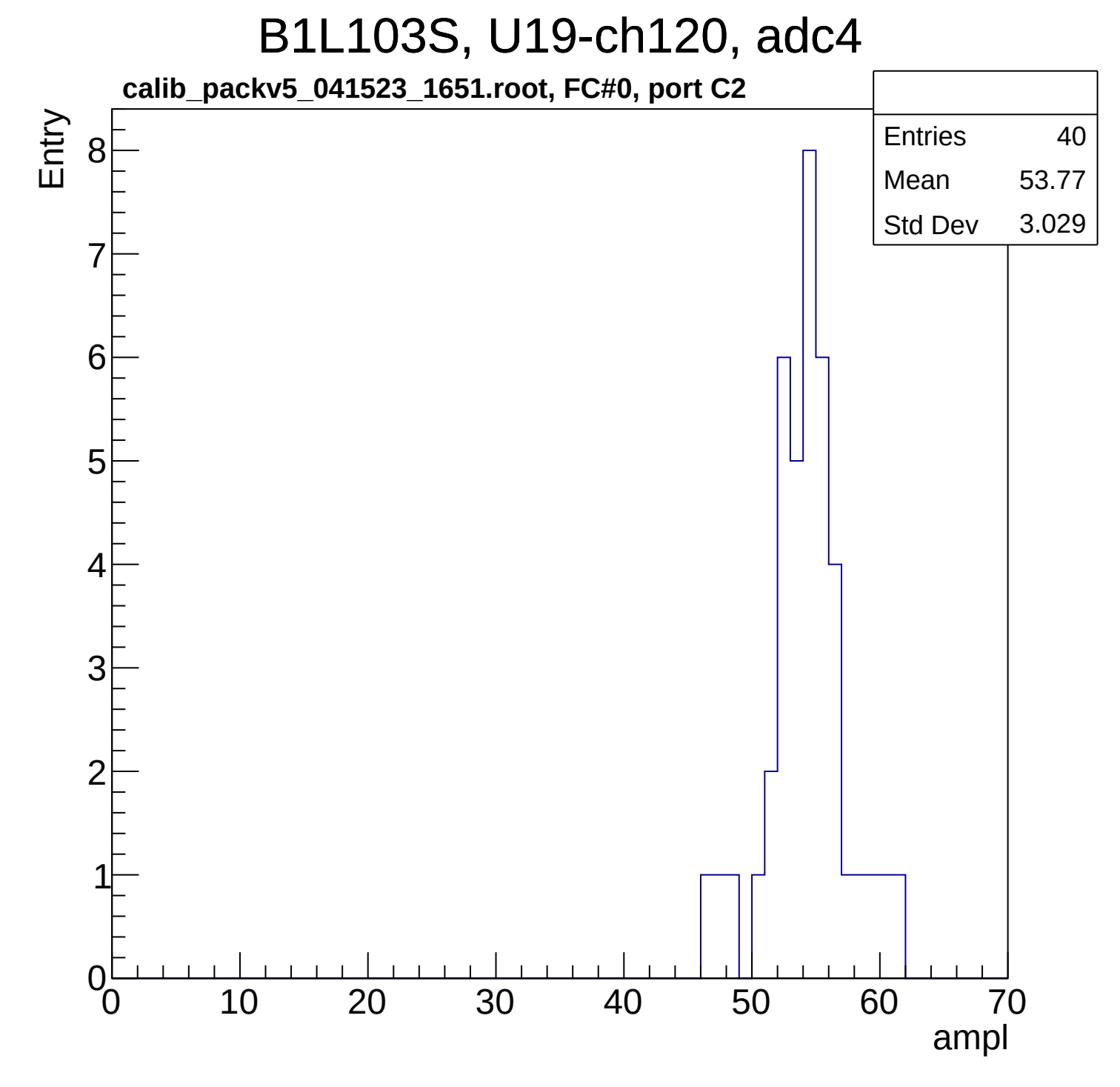
B1L103S, U19-ch120, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 53.77
Std Dev 3.029
Entry
ampl
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0
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60
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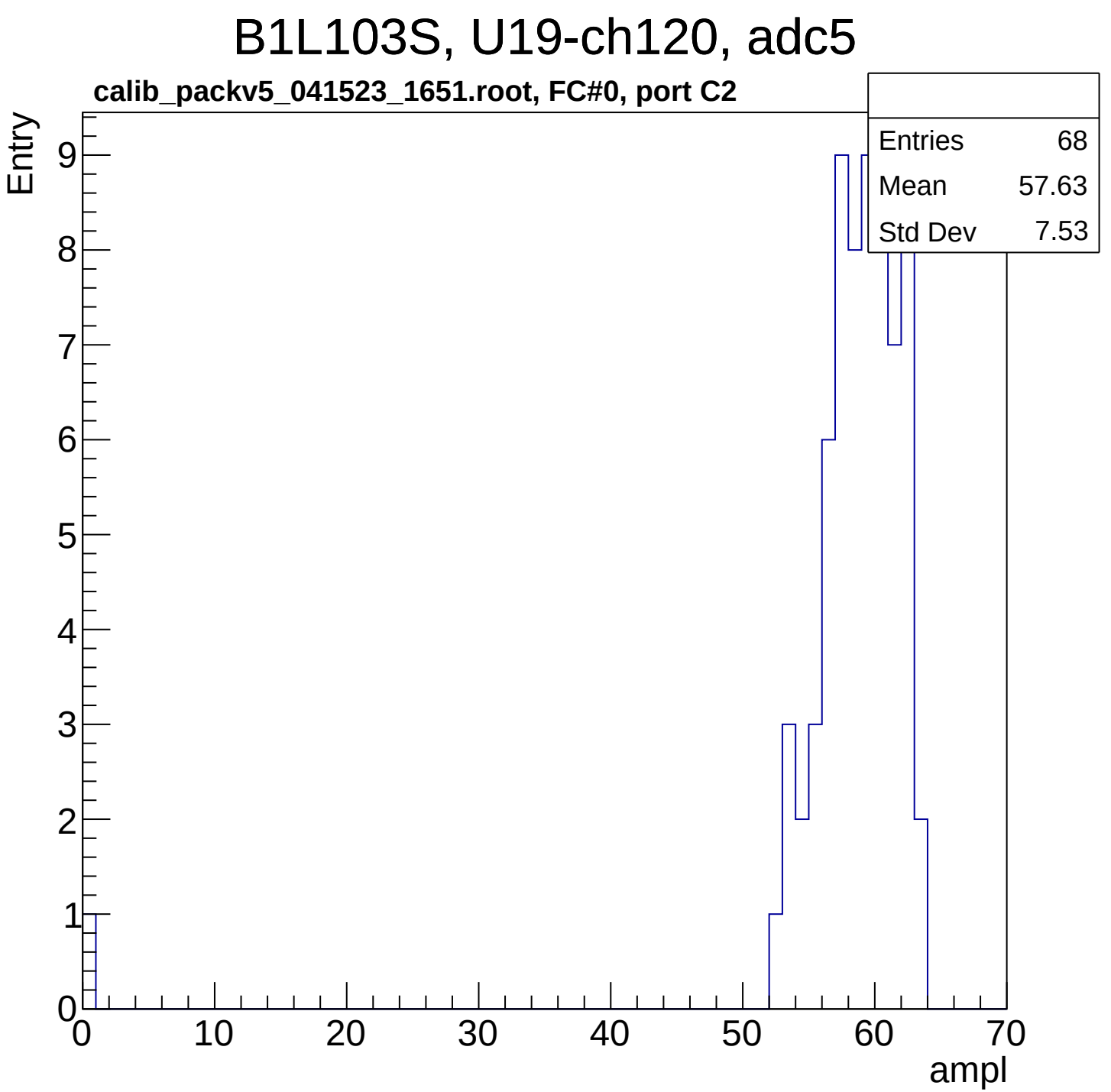
B1L103S, U19-ch120, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 57.63
Std Dev 7.53
Entry
ampl
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2
3
4
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6
7
8
9
0
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40
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60
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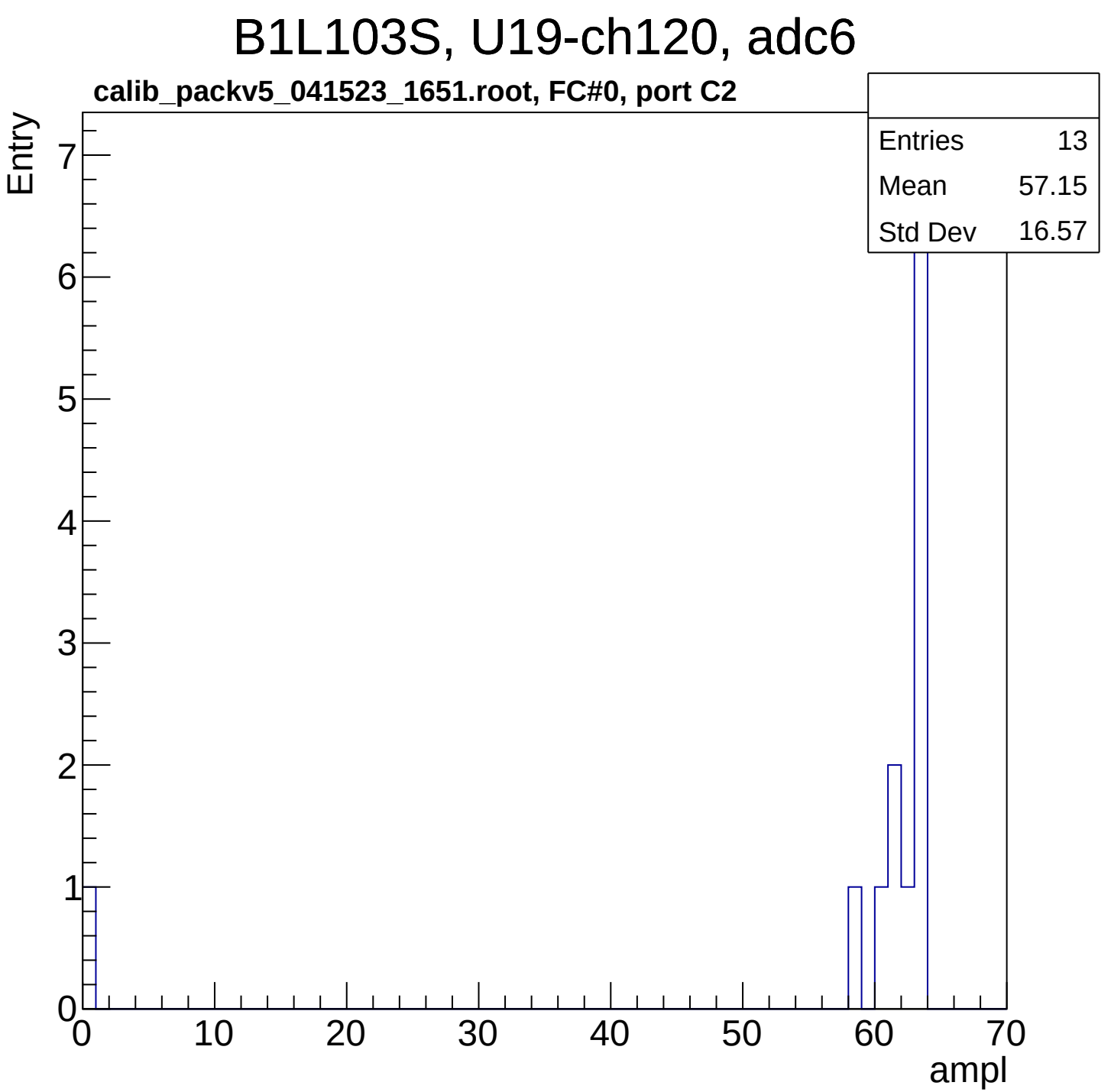
B1L103S, U19-ch120, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 57.15
Std Dev 16.57
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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40
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60
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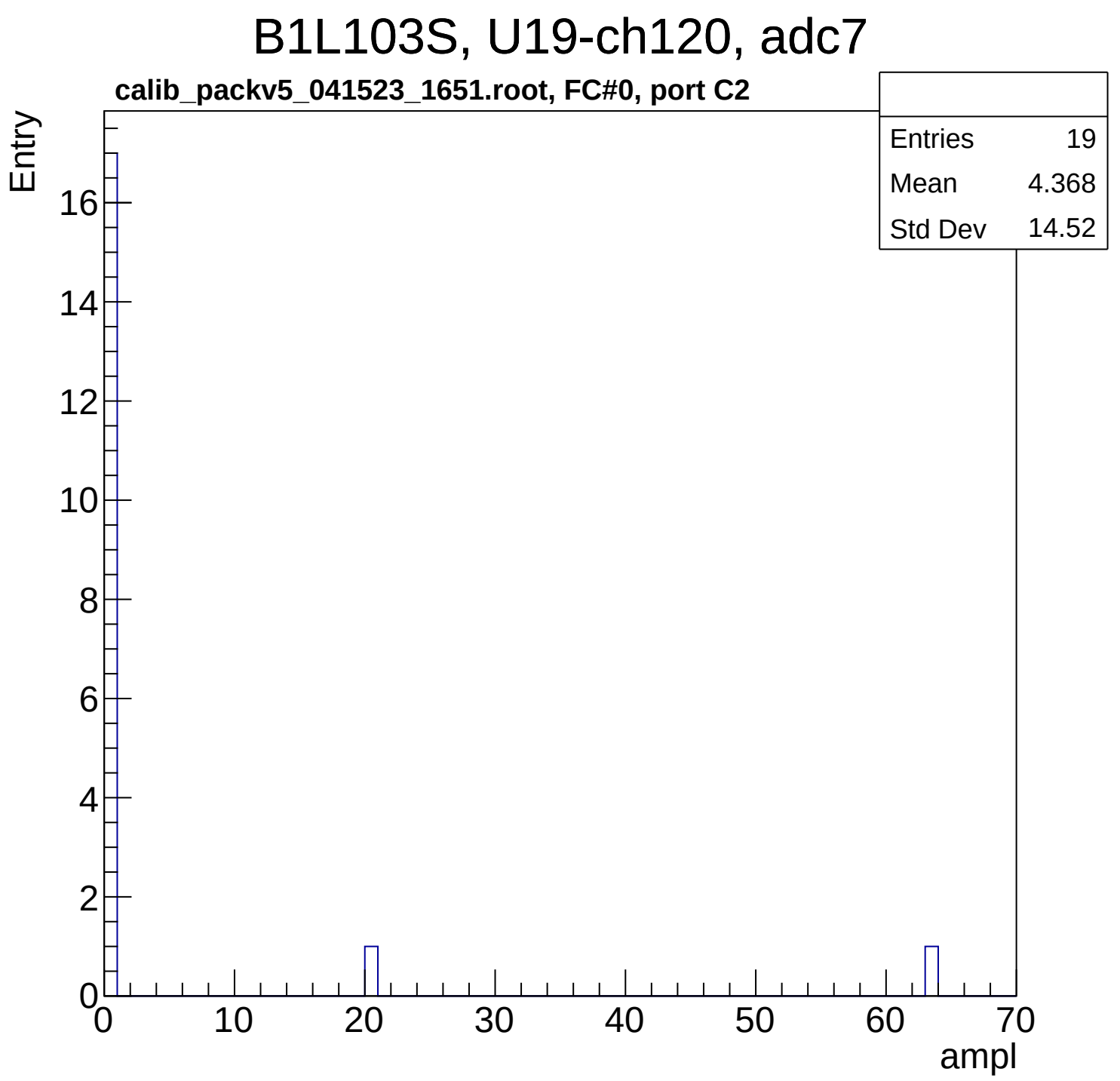
B1L103S, U19-ch120, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 4.368
Std Dev 14.52
Entry
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4
6
8
10
12
14
16
0
10
20
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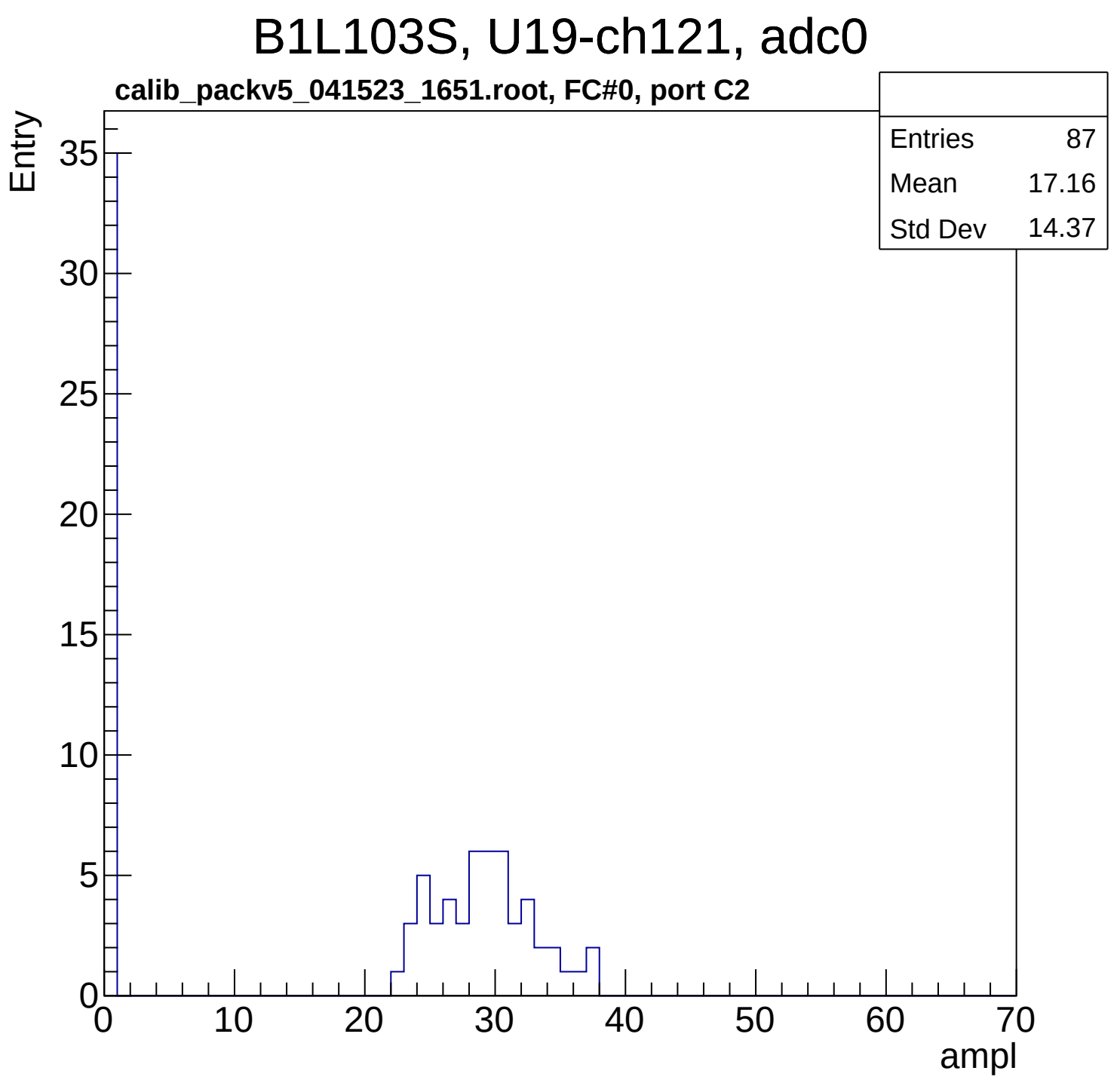
50
60
70
ampl


B1L103S, U19-ch121, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 17.16
Std Dev 14.37
Entry
ampl
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5
10
15
20
25
30
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0
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40
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60
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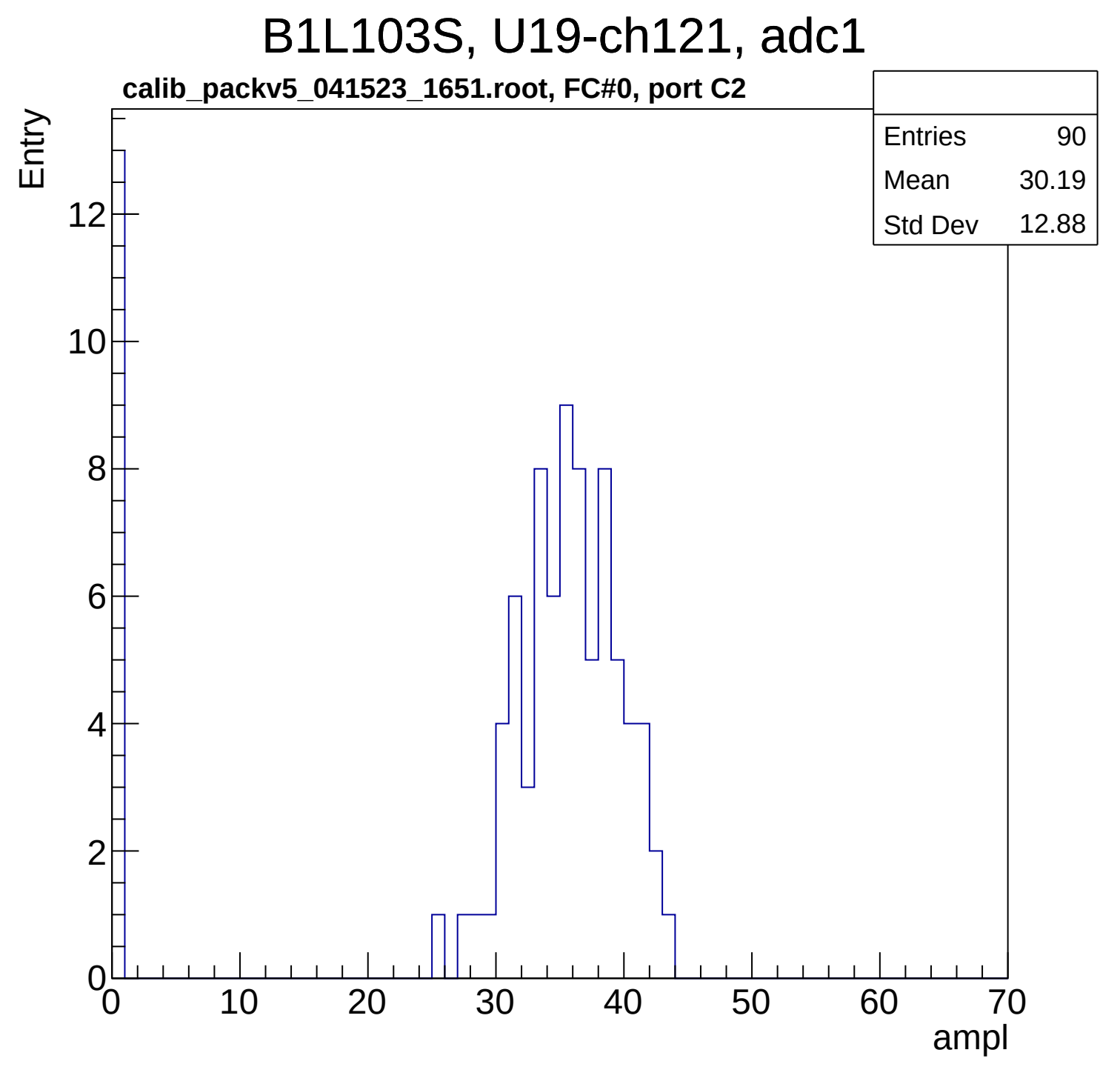
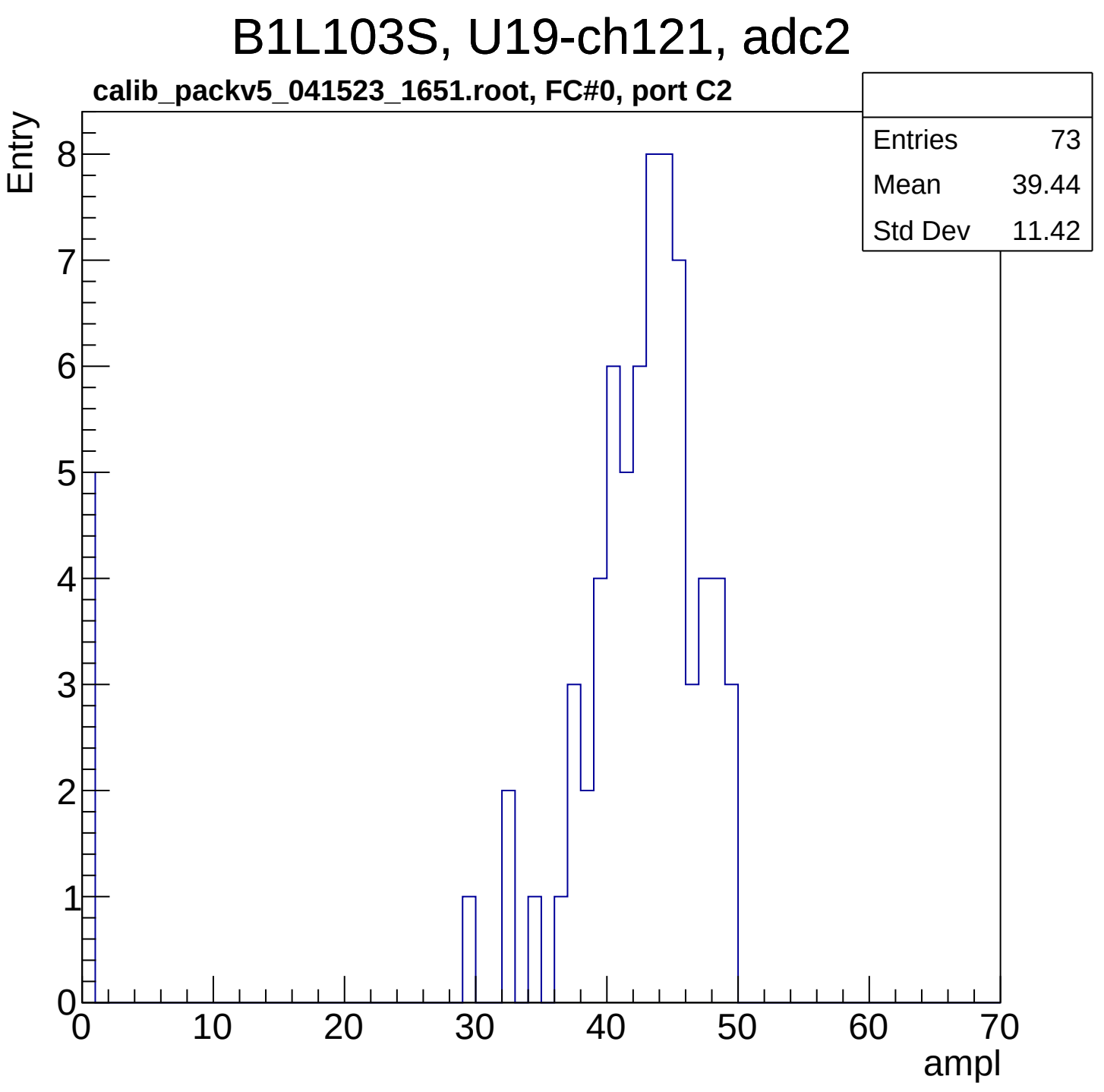
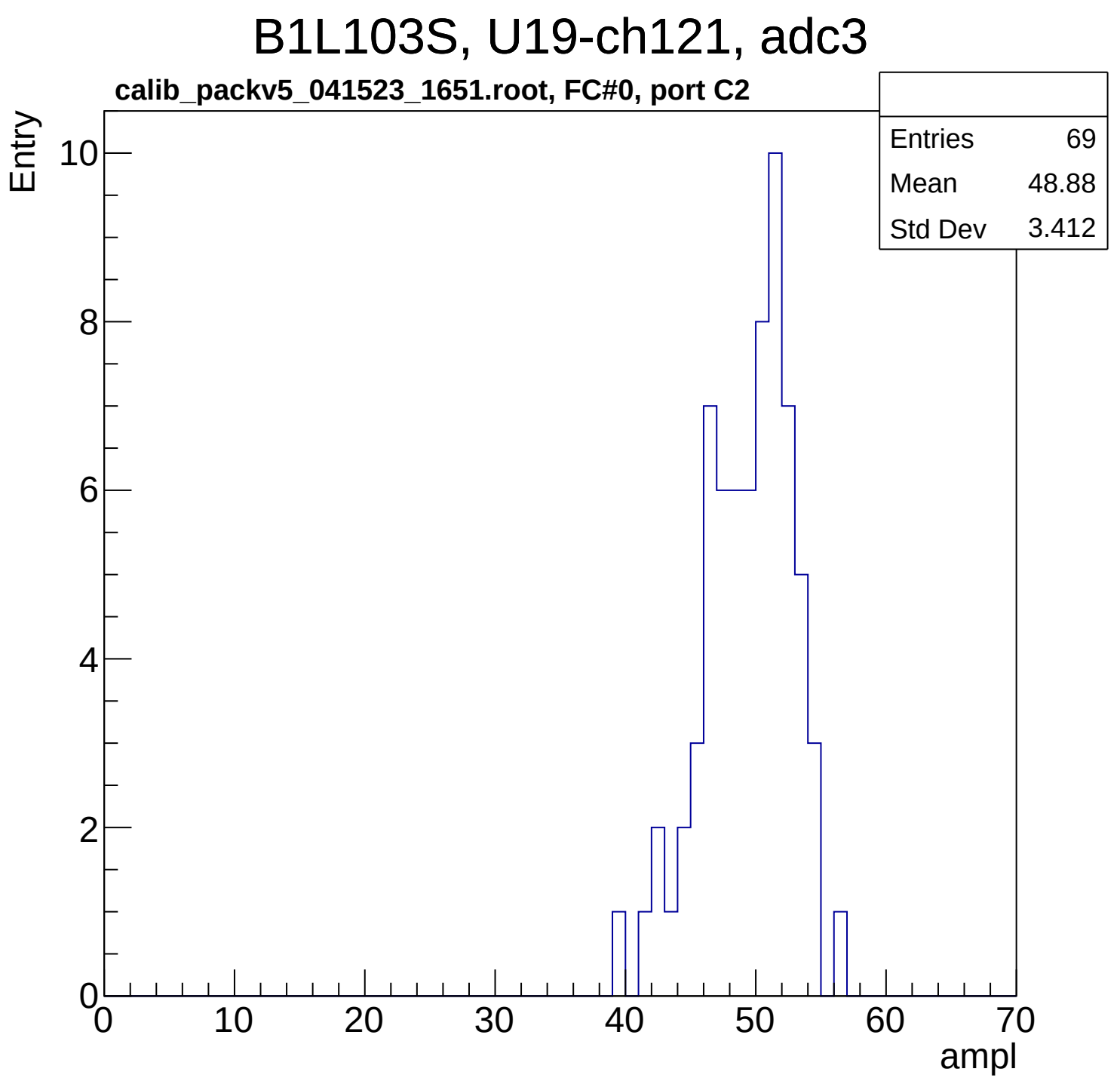
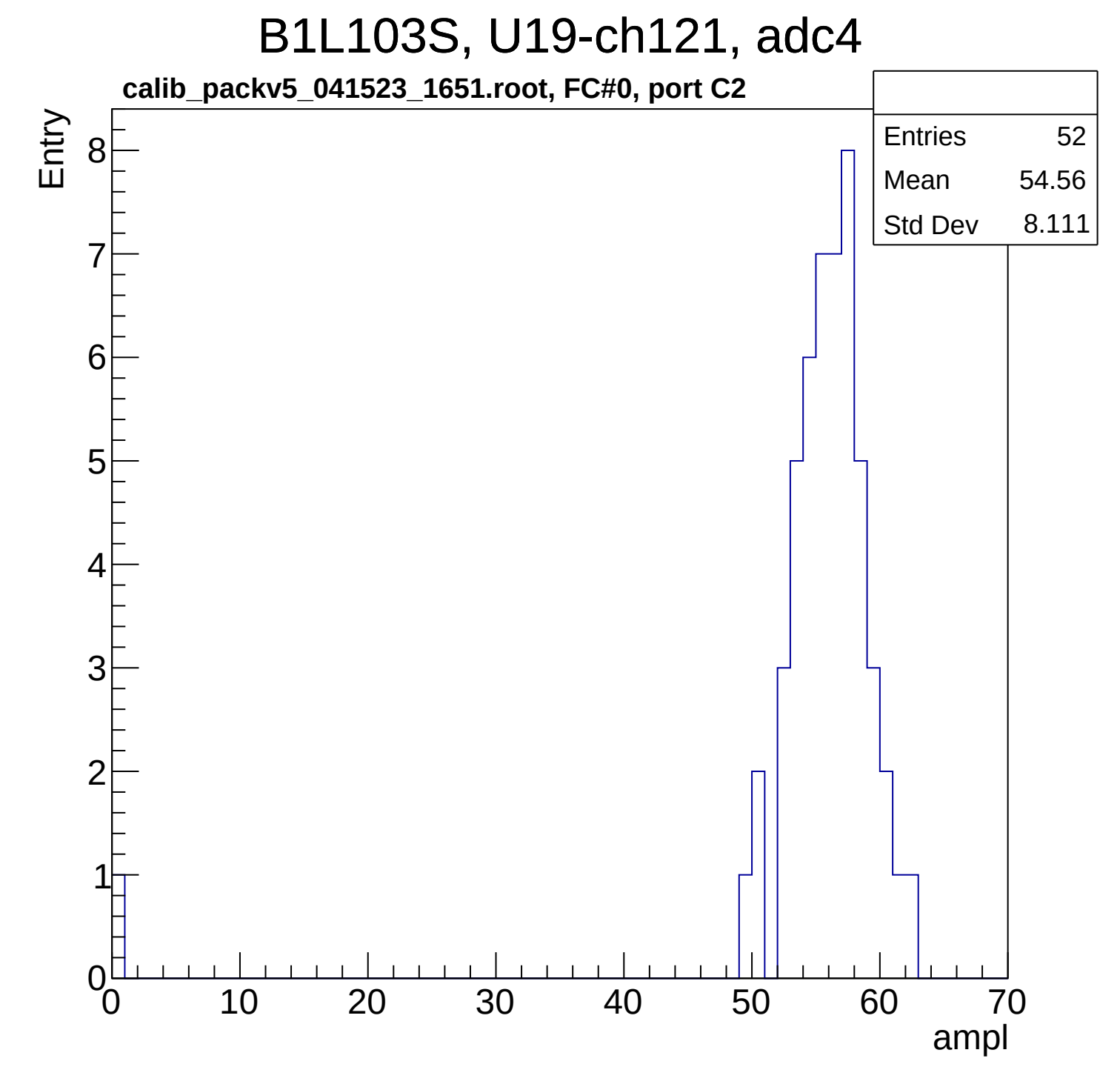

B1L103S, U19-ch121, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 30.19
Std Dev 12.88
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch121, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 39.44
Std Dev 11.42
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch121, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 48.88
Std Dev 3.412
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U19-ch121, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 54.56
Std Dev 8.111
Entry
ampl
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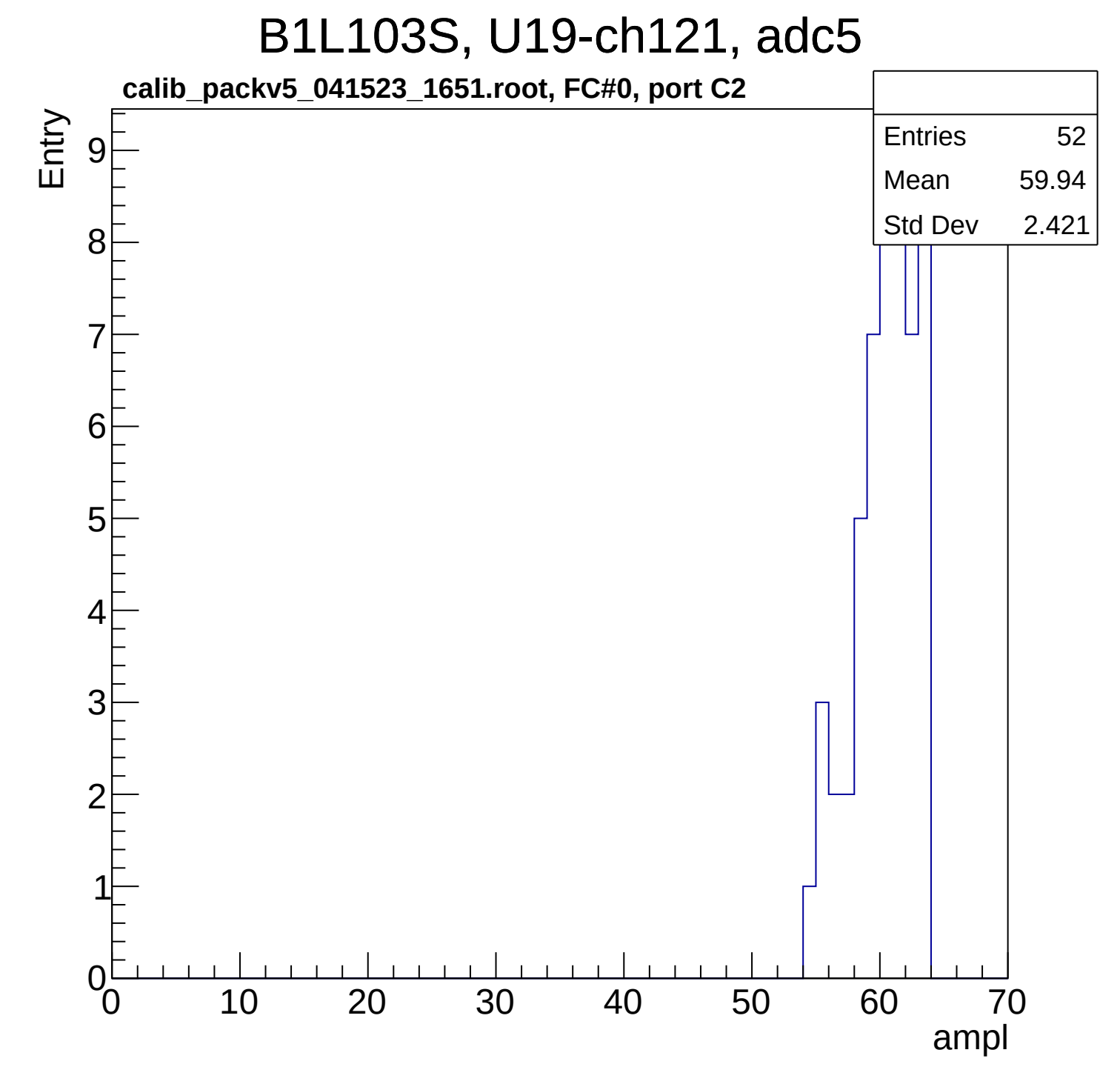
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch121, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 59.94
Std Dev 2.421
Entry
ampl
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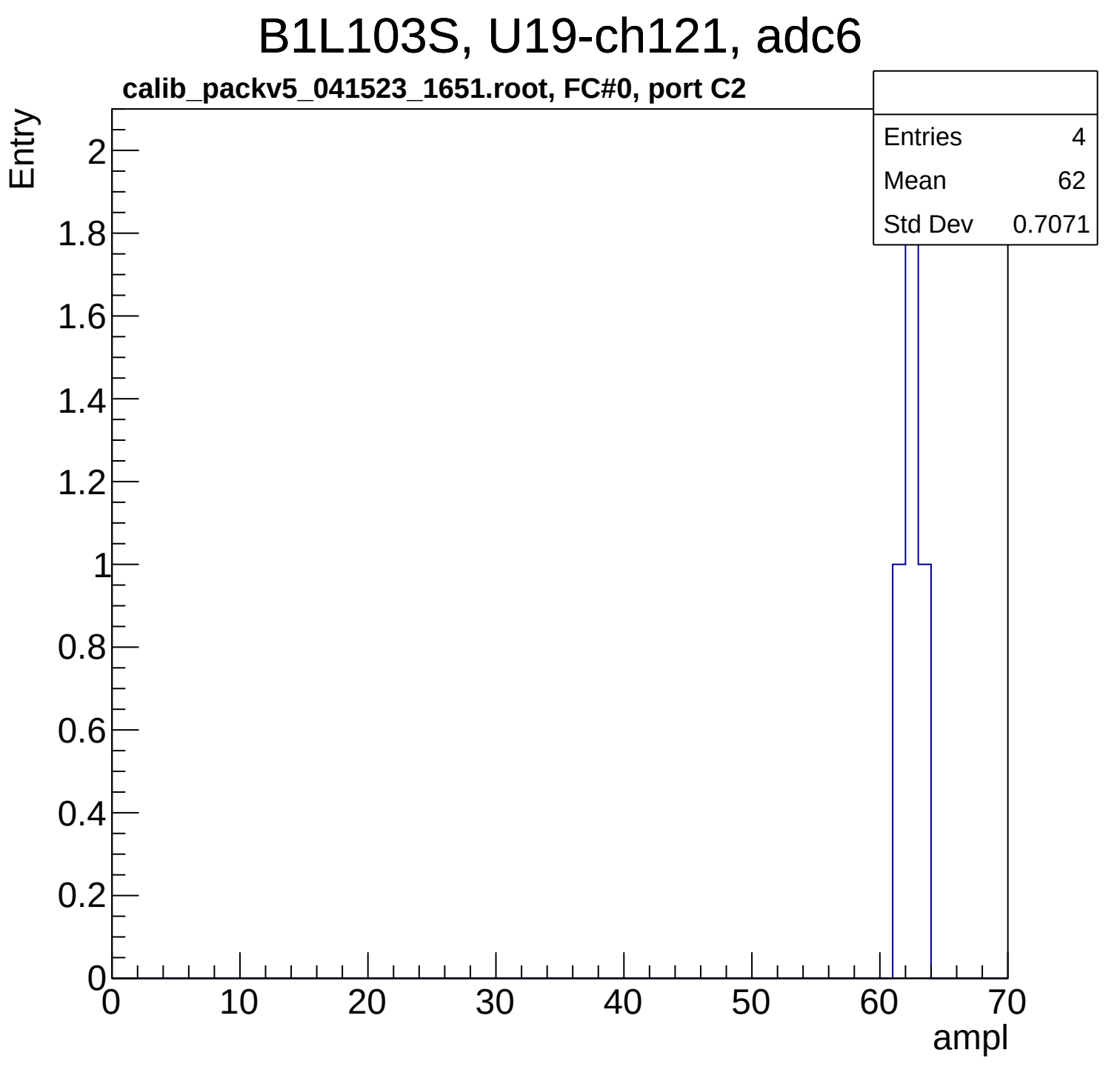
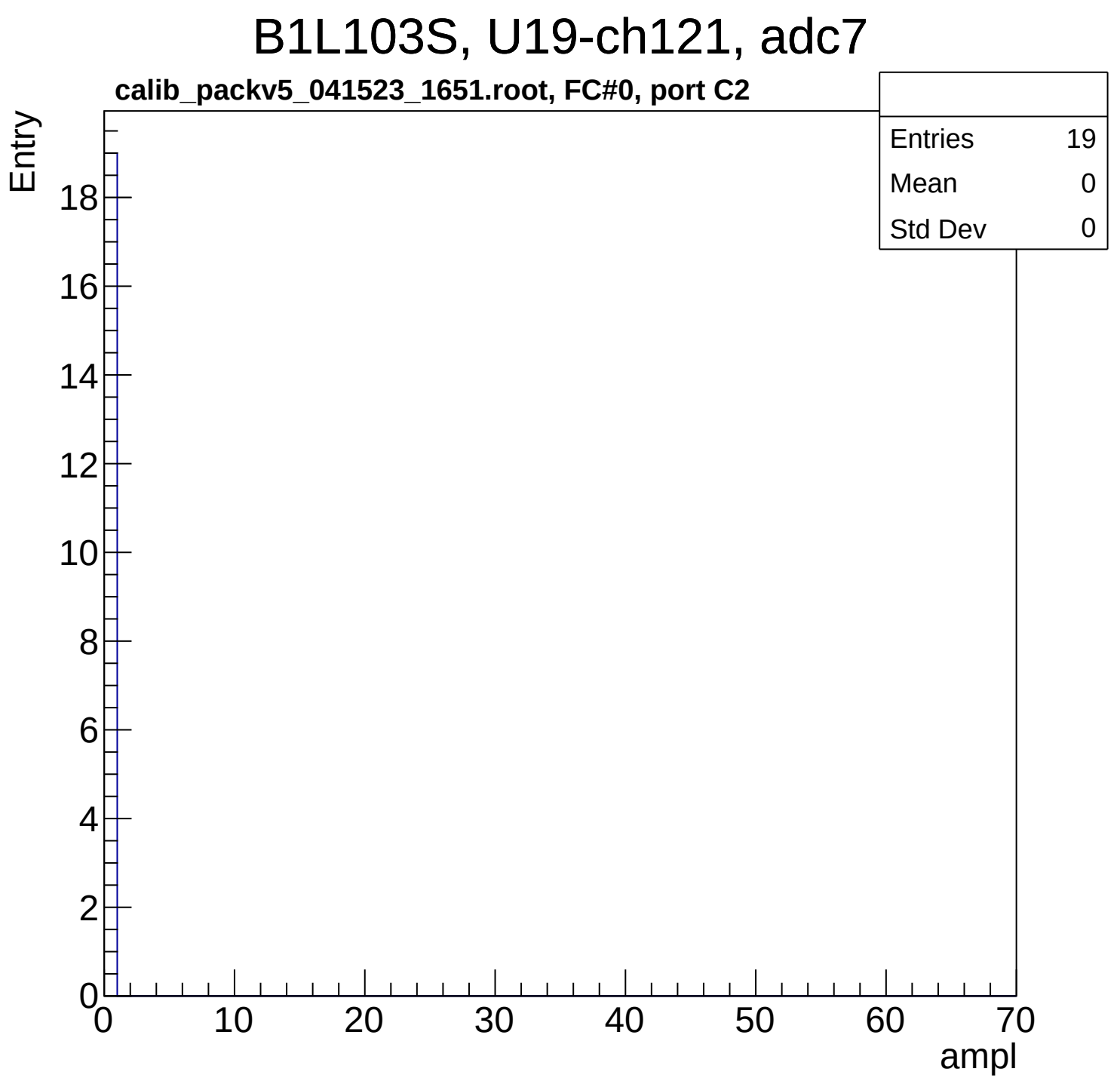
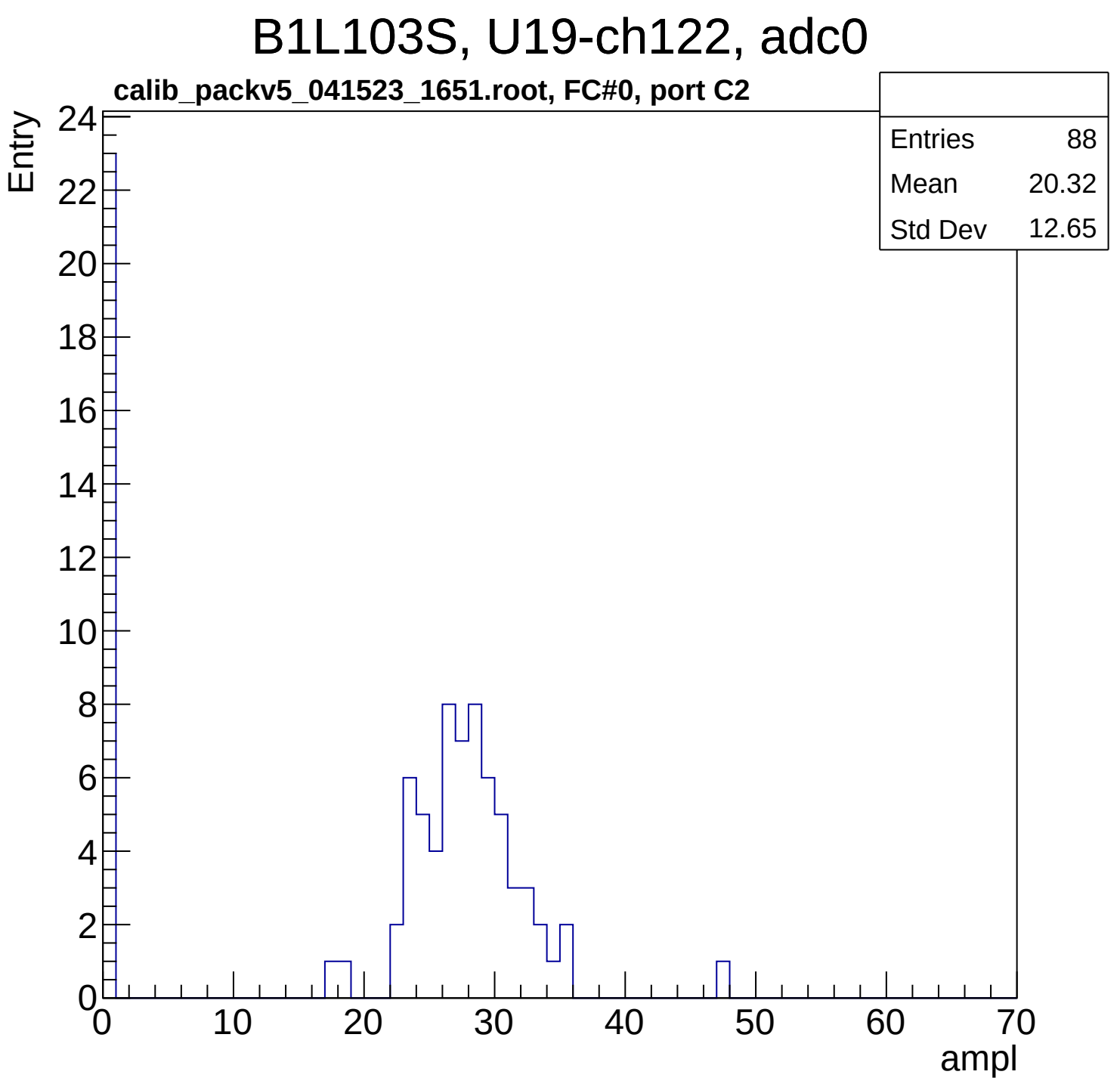
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch121, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 62
Std Dev 0.7071
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U19-ch121, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch122, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 20.32
Std Dev 12.65
Entry
ampl
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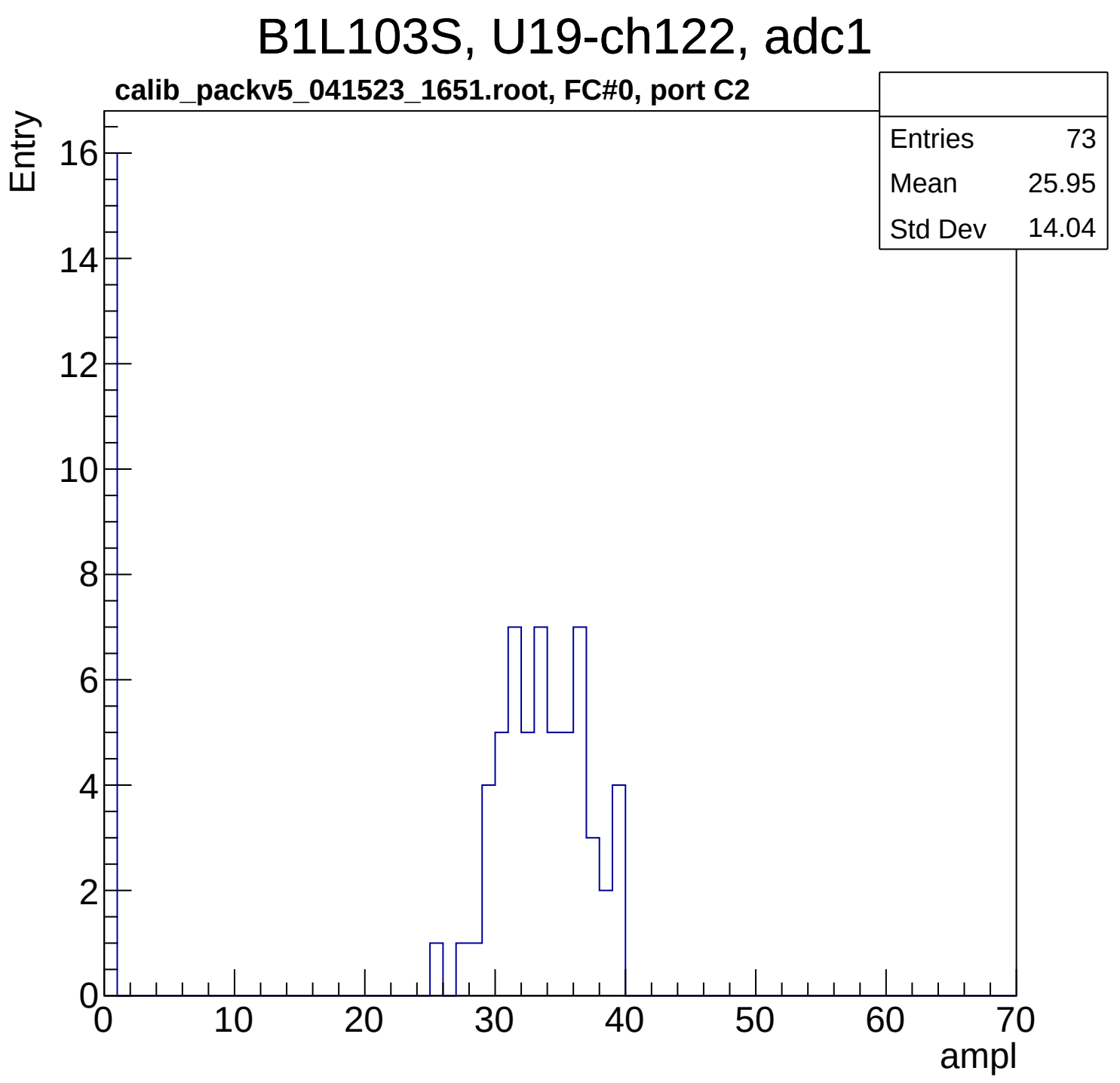
2
4
6
8
10
12
14
16
18
20
22
24
0
10
20
30
40
50
60
70


B1L103S, U19-ch122, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 25.95
Std Dev 14.04
Entry
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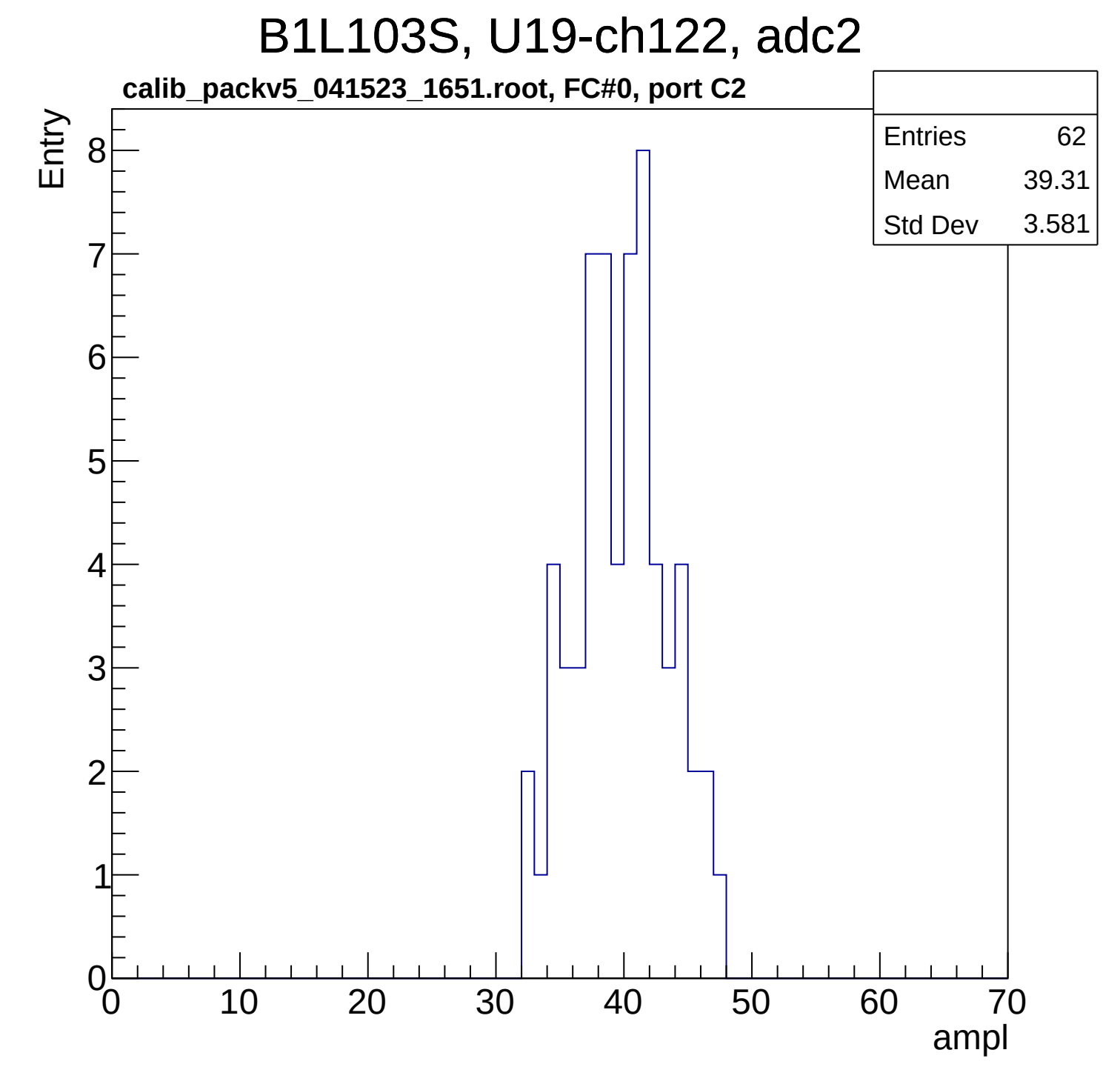
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch122, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 39.31
Std Dev 3.581
Entry
ampl
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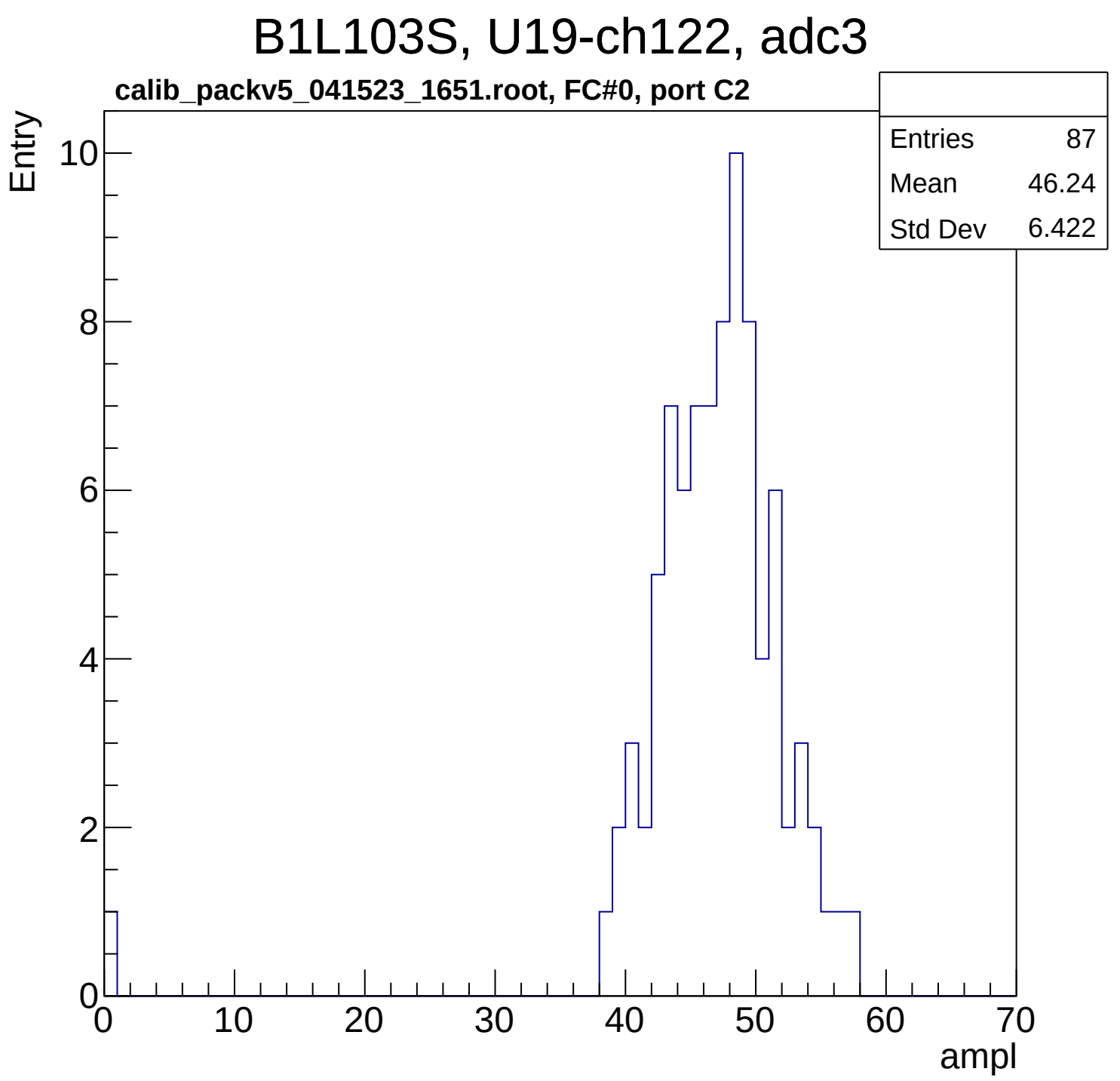
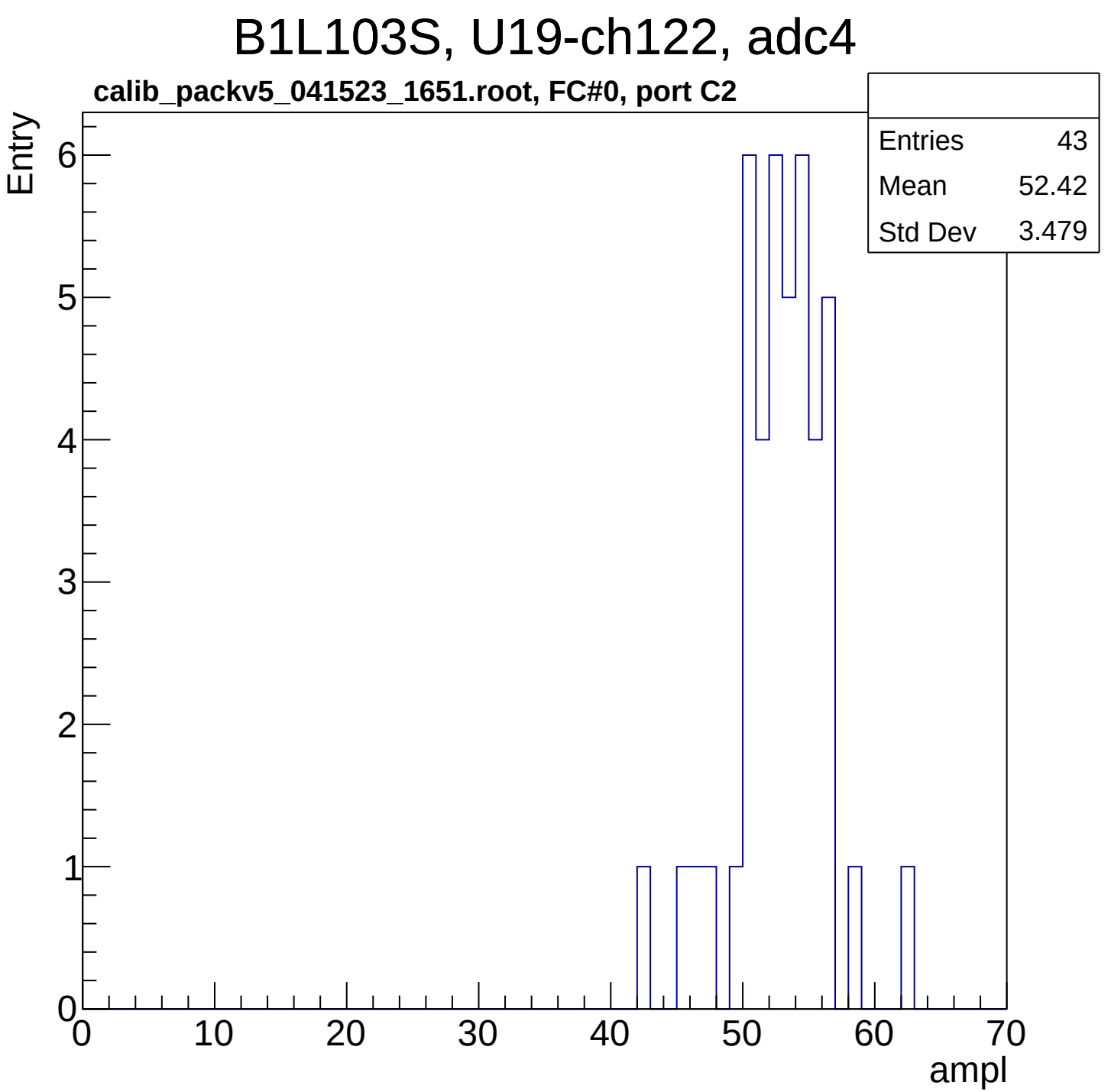
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch122, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 46.24
Std Dev 6.422
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U19-ch122, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 52.42
Std Dev 3.479
Entry
ampl
0
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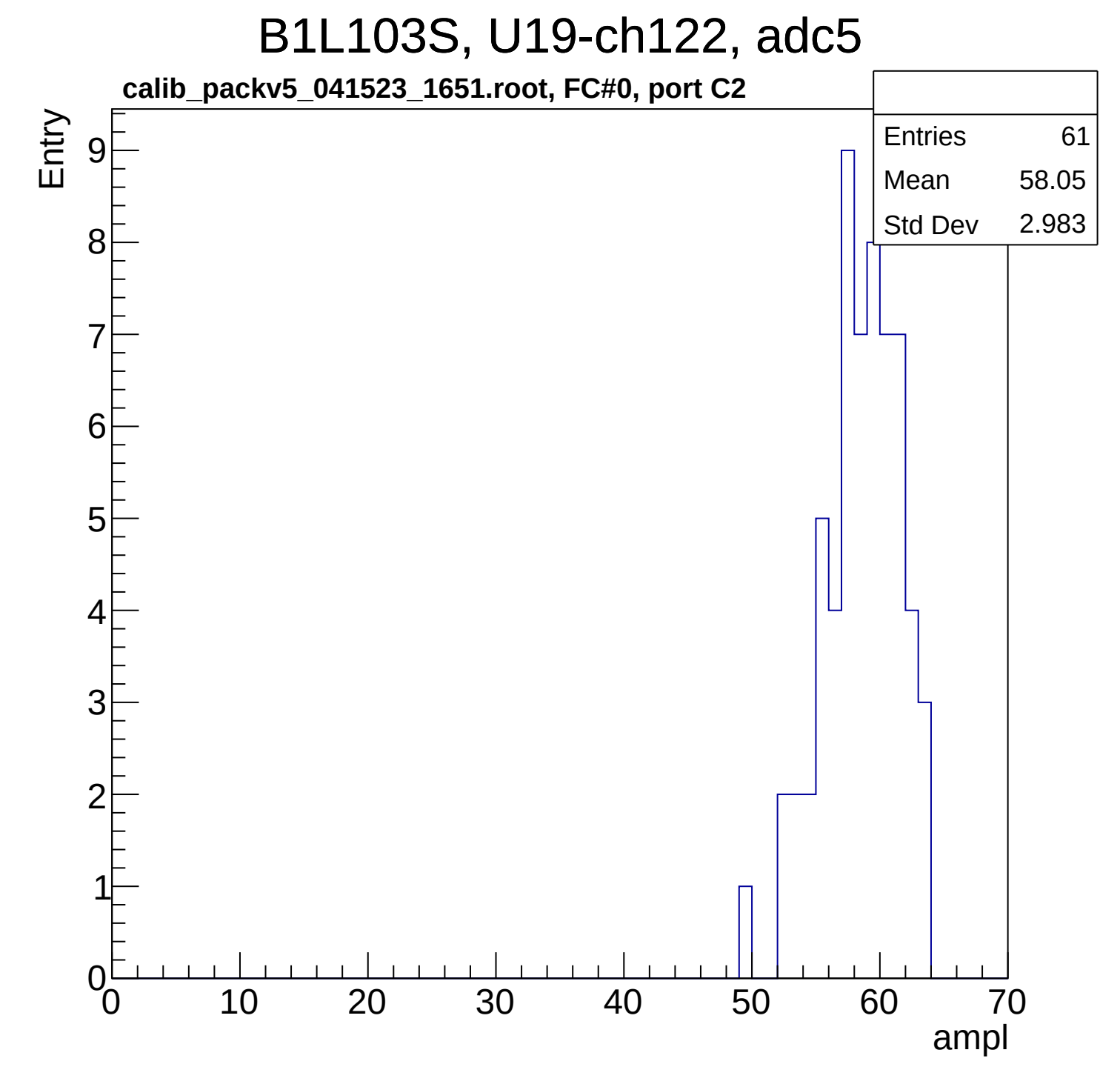
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U19-ch122, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 58.05
Std Dev 2.983
Entry
ampl
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3
4
5
6
7
8
9
0
10
20
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50
60
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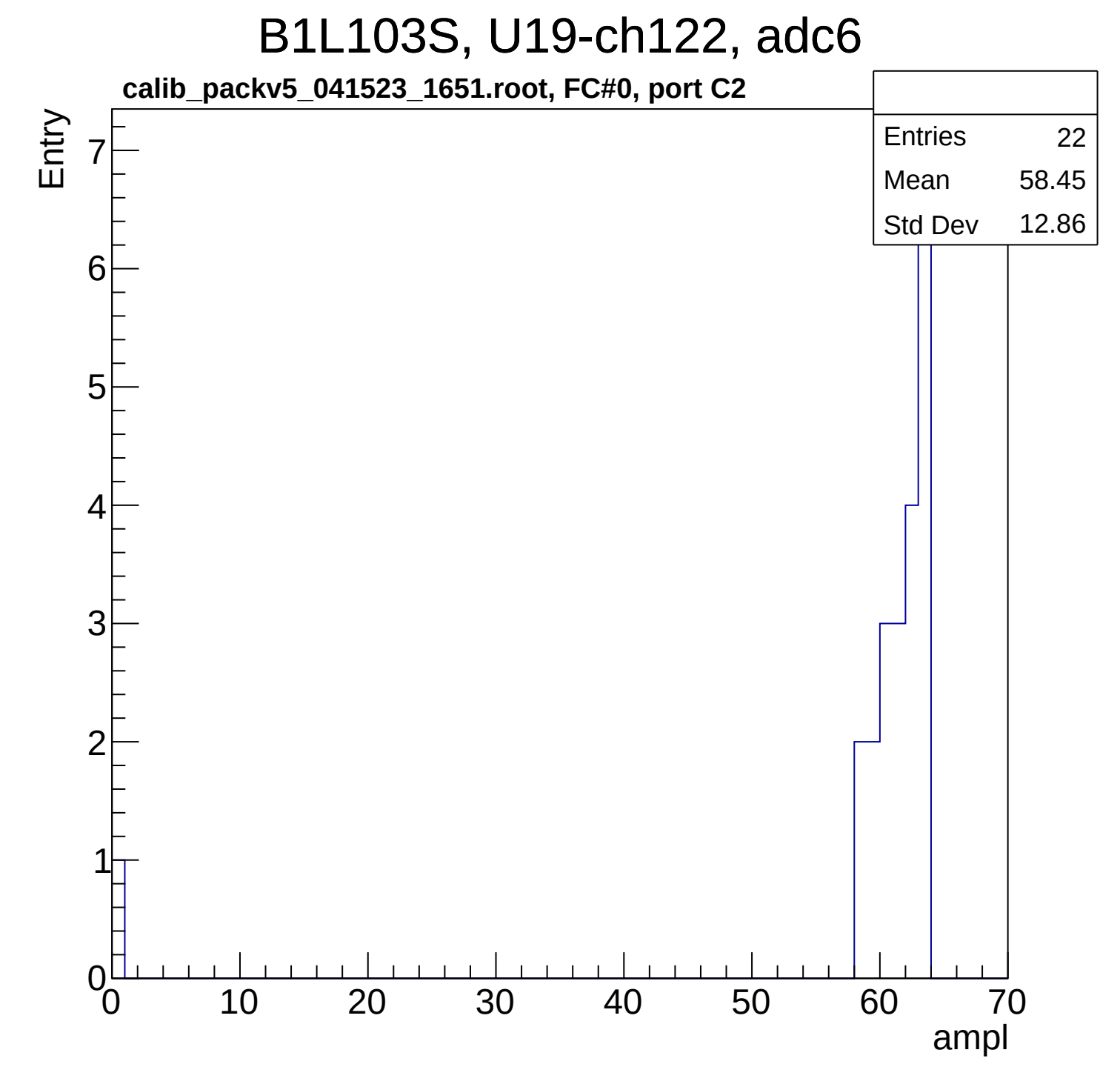
B1L103S, U19-ch122, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 58.45
Std Dev 12.86
Entry
ampl
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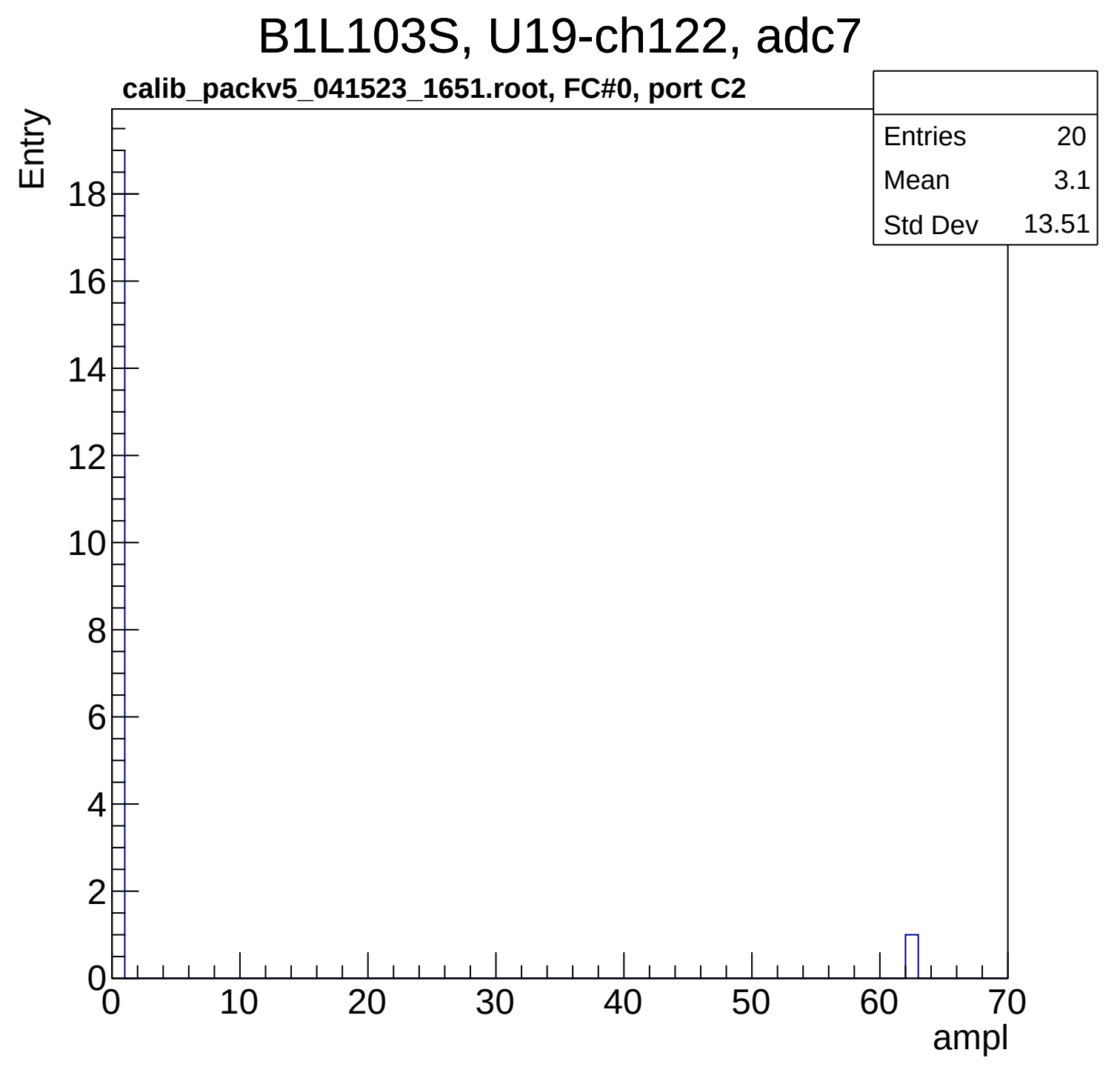
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U19-ch122, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
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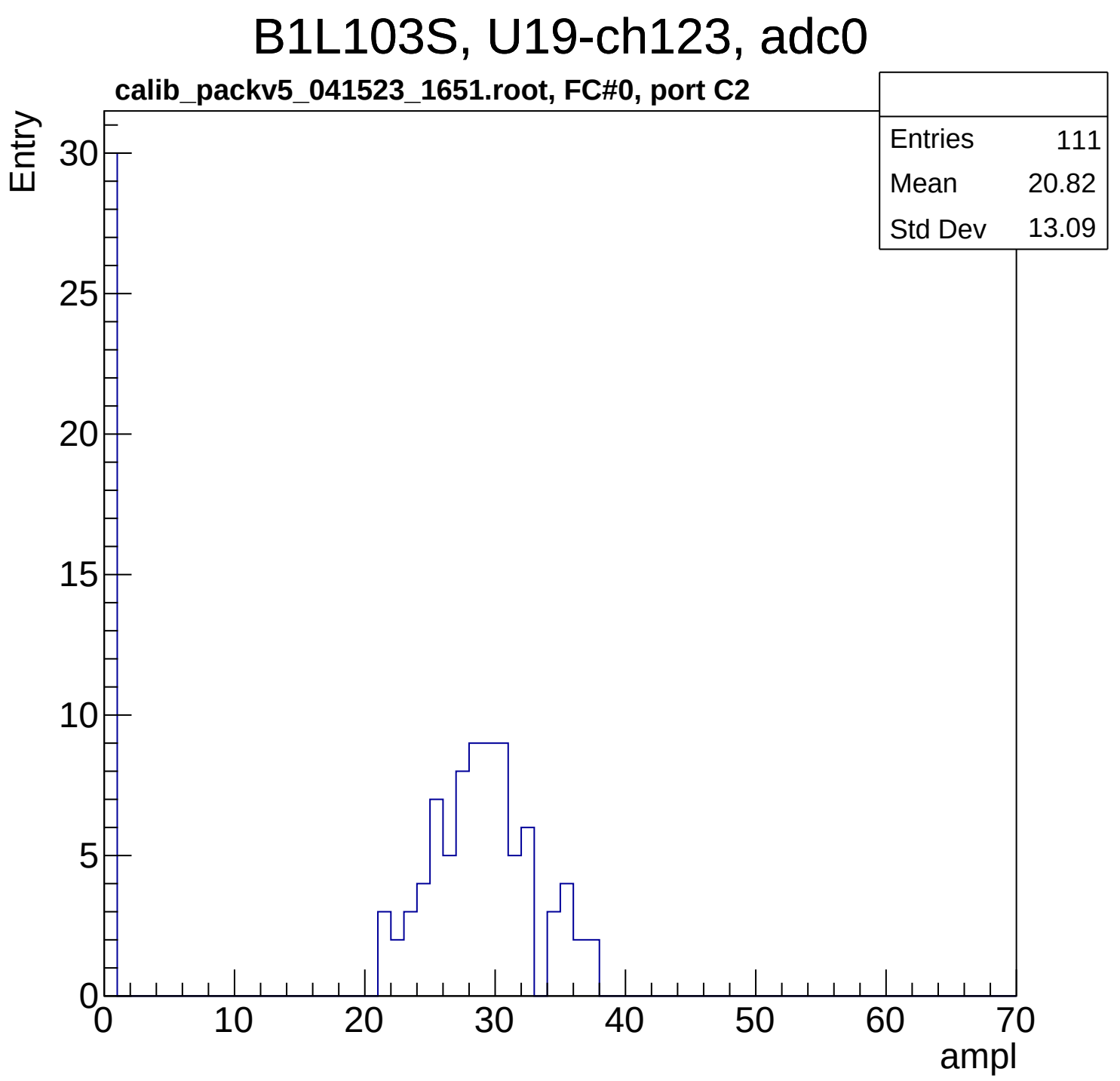
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch123, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 111
Mean 20.82
Std Dev 13.09
Entry
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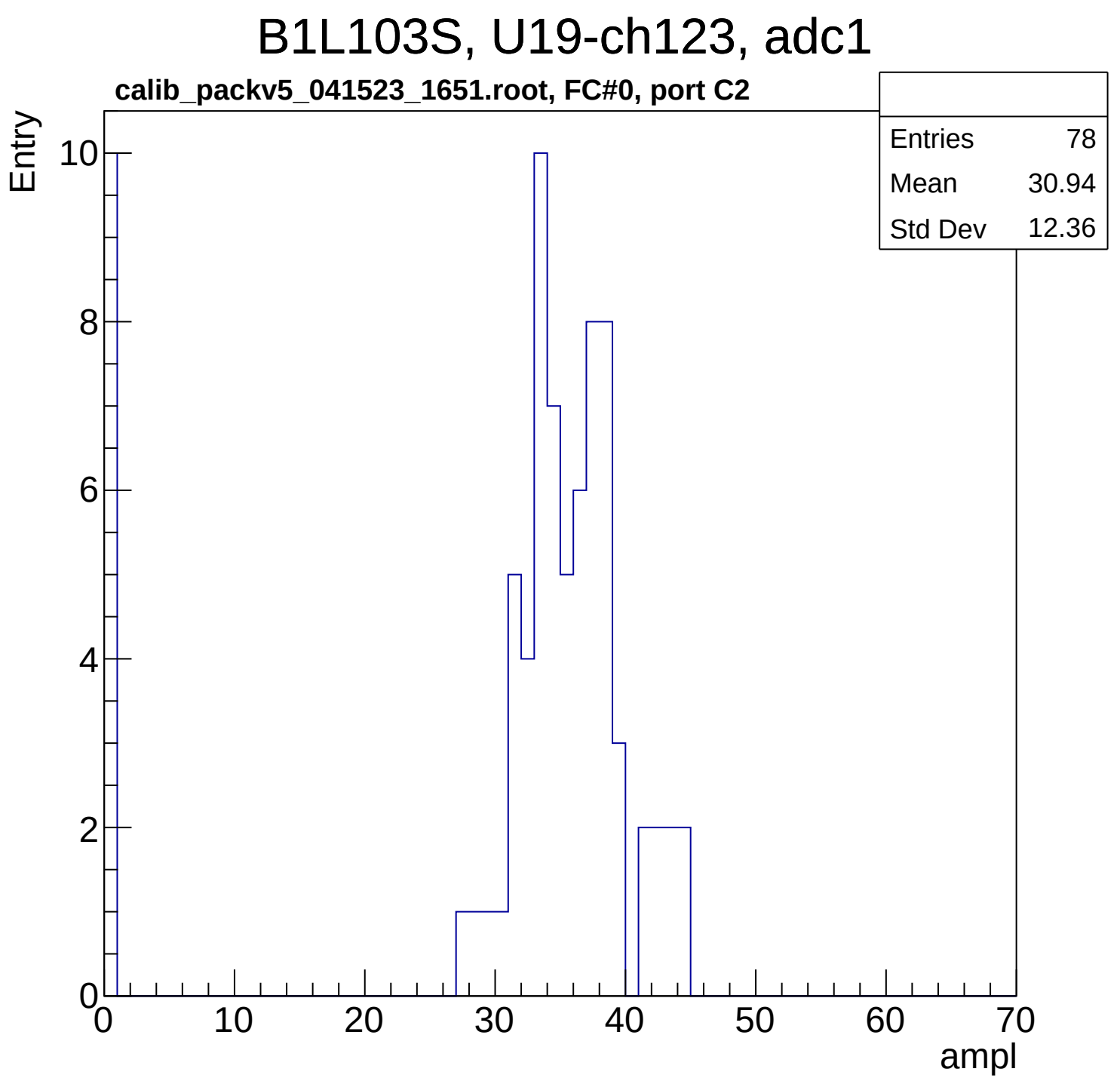
5
10
15
20
25
30
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch123, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 30.94
Std Dev 12.36
Entry
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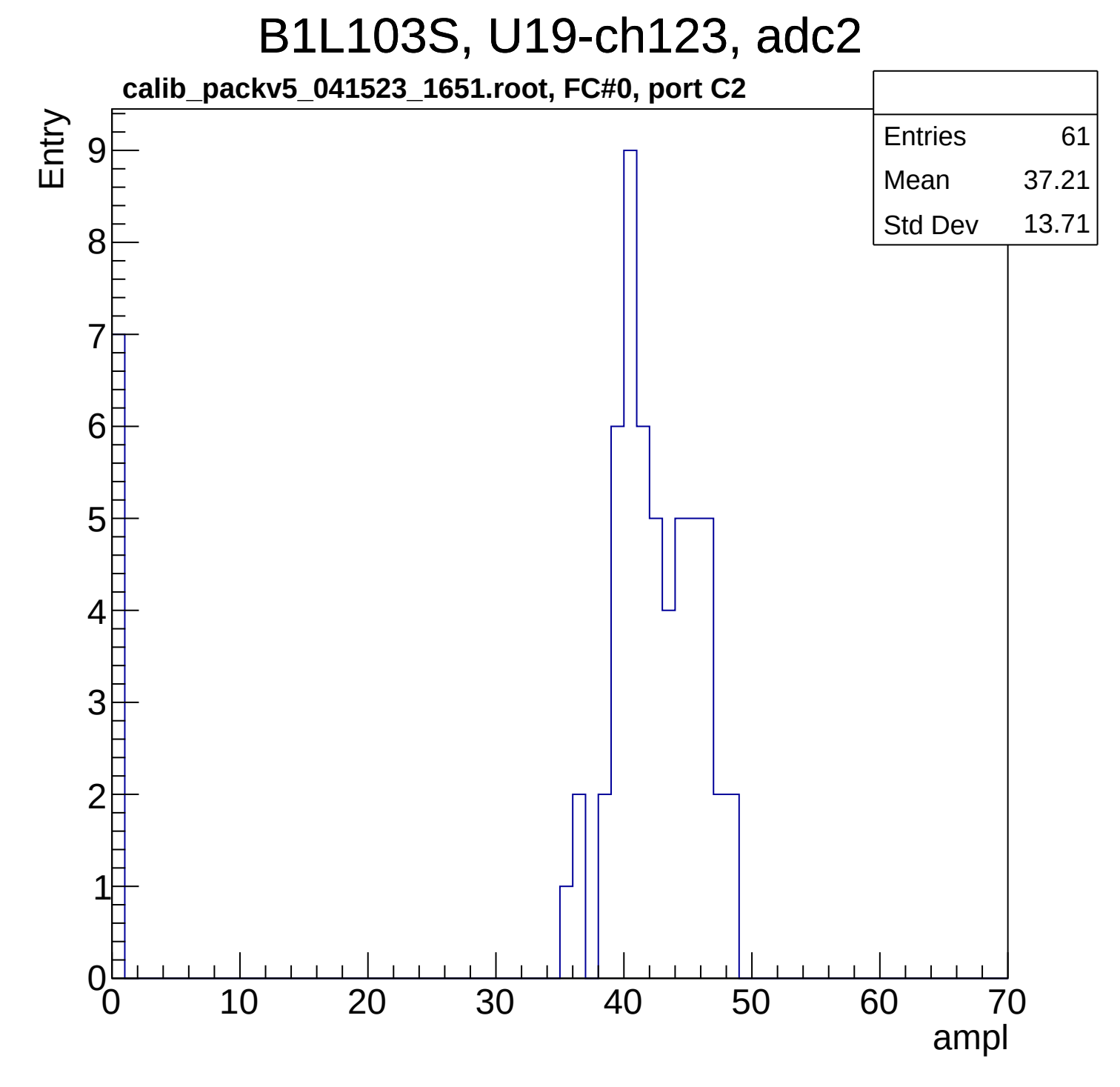
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch123, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 37.21
Std Dev 13.71
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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30
40
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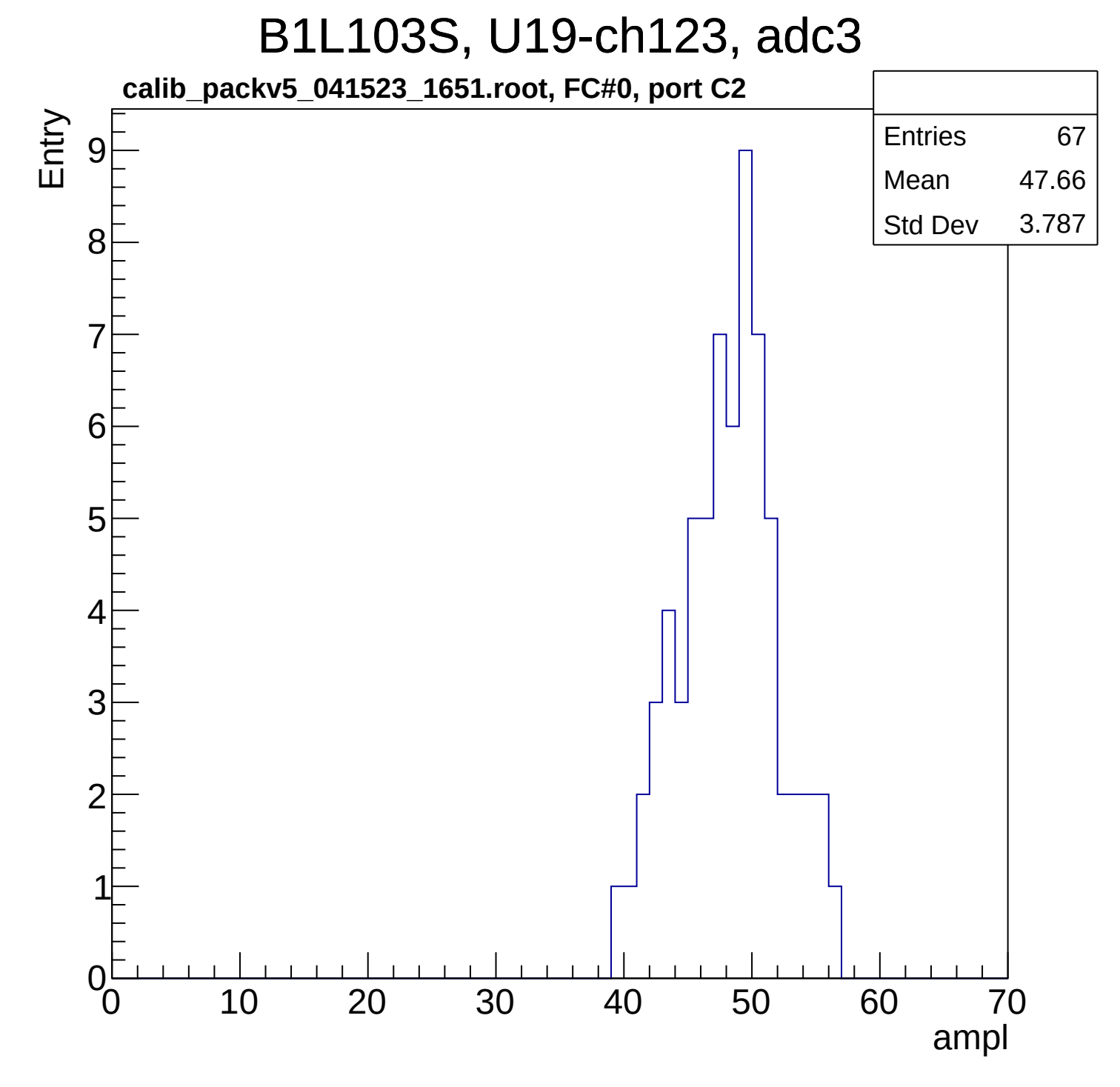
60
70


B1L103S, U19-ch123, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 47.66
Std Dev 3.787
Entry
ampl
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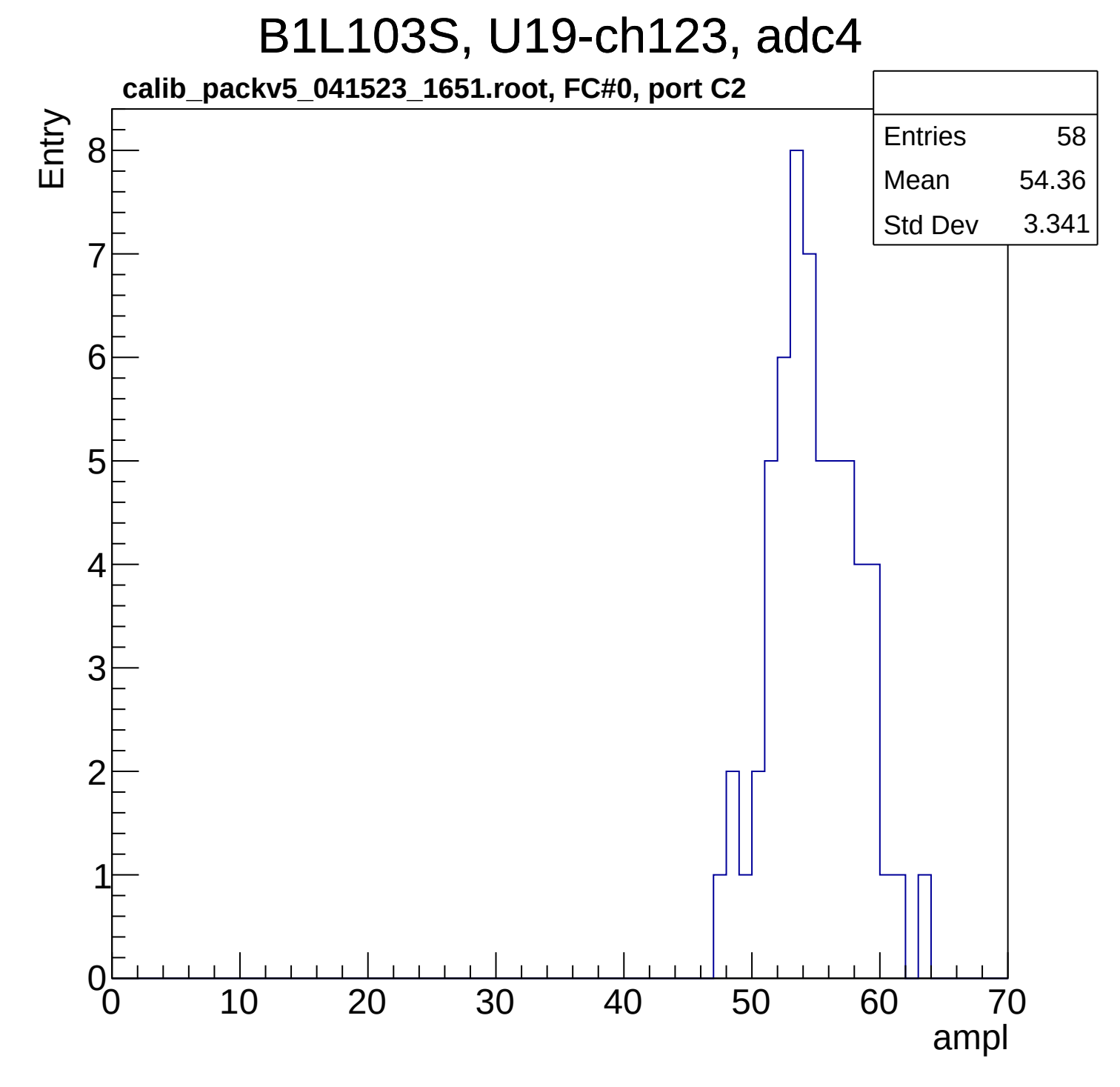
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U19-ch123, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 54.36
Std Dev 3.341
Entry
ampl
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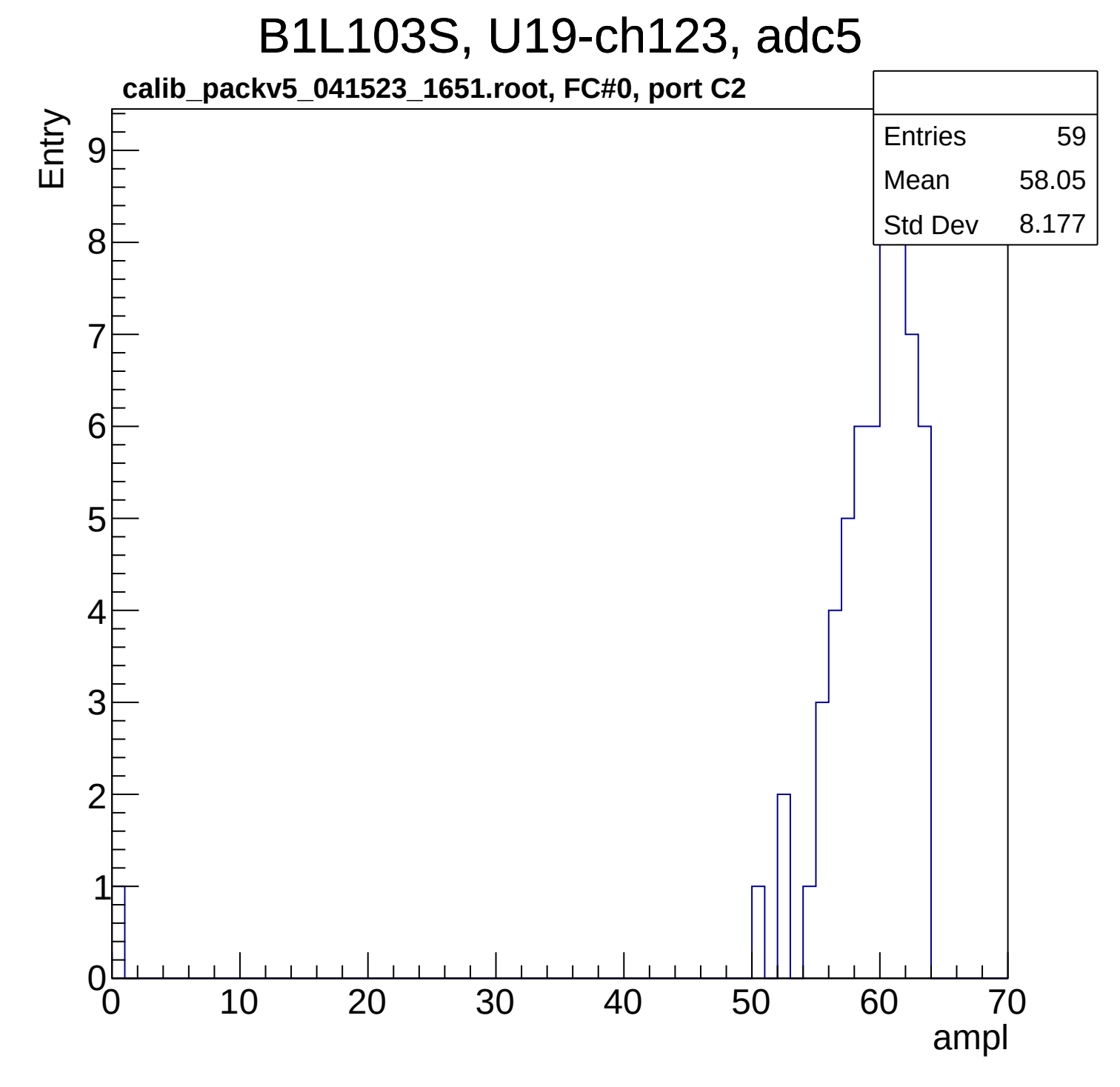
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch123, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 58.05
Std Dev 8.177
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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60
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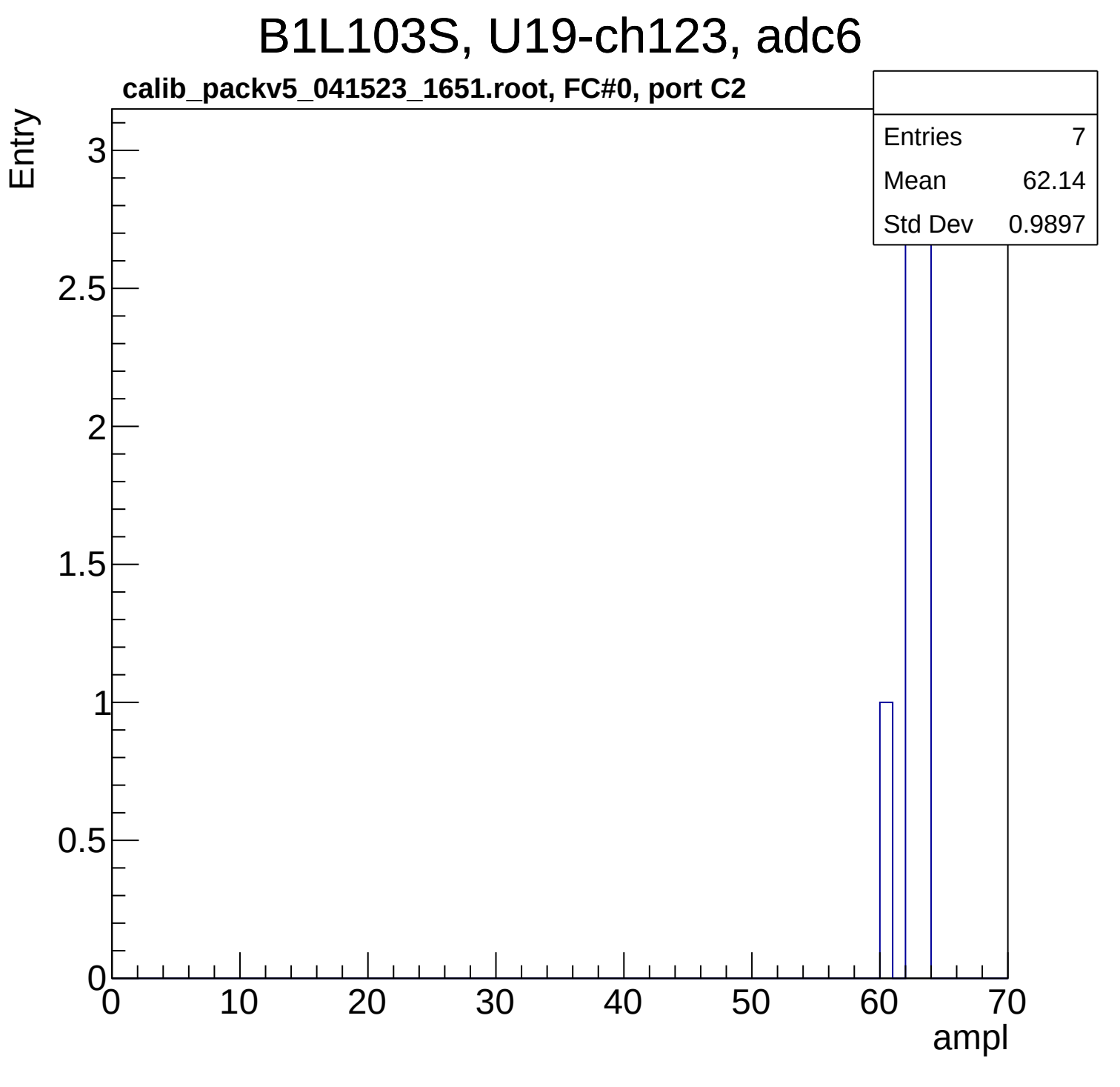
B1L103S, U19-ch123, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 62.14
Std Dev 0.9897
Entry
ampl
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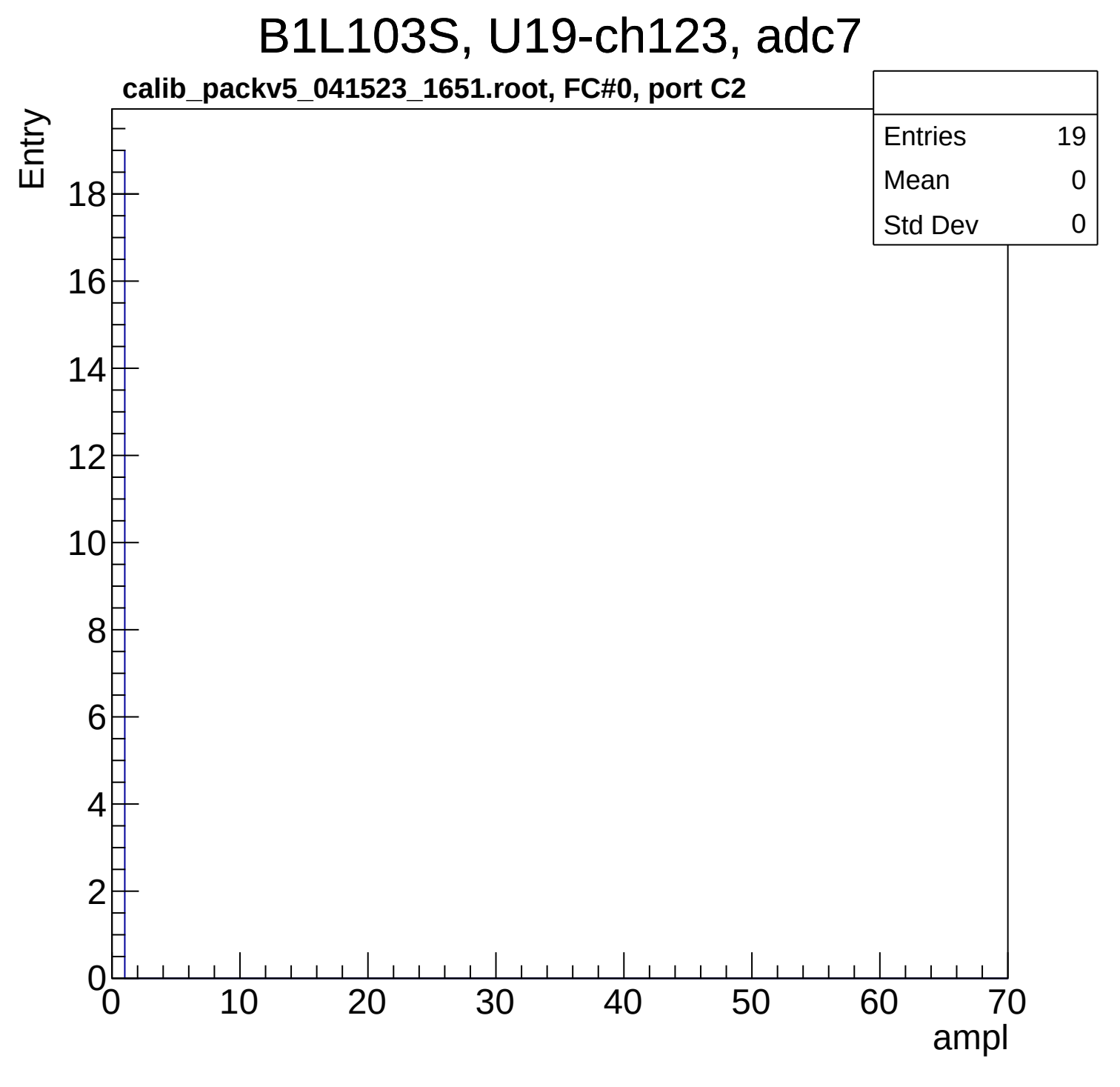
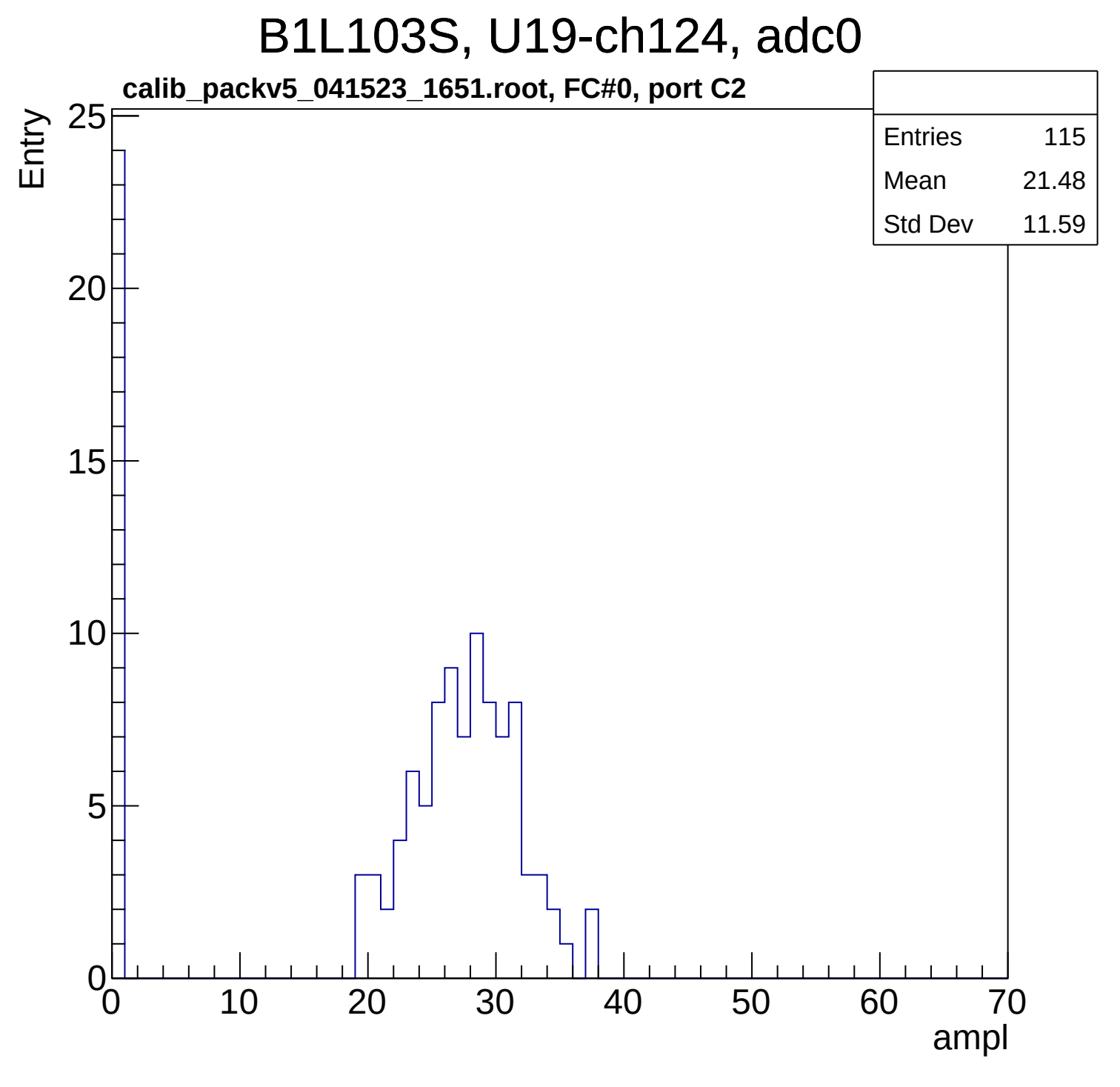
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U19-ch123, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch124, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 115
Mean 21.48
Std Dev 11.59
Entry
ampl
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10
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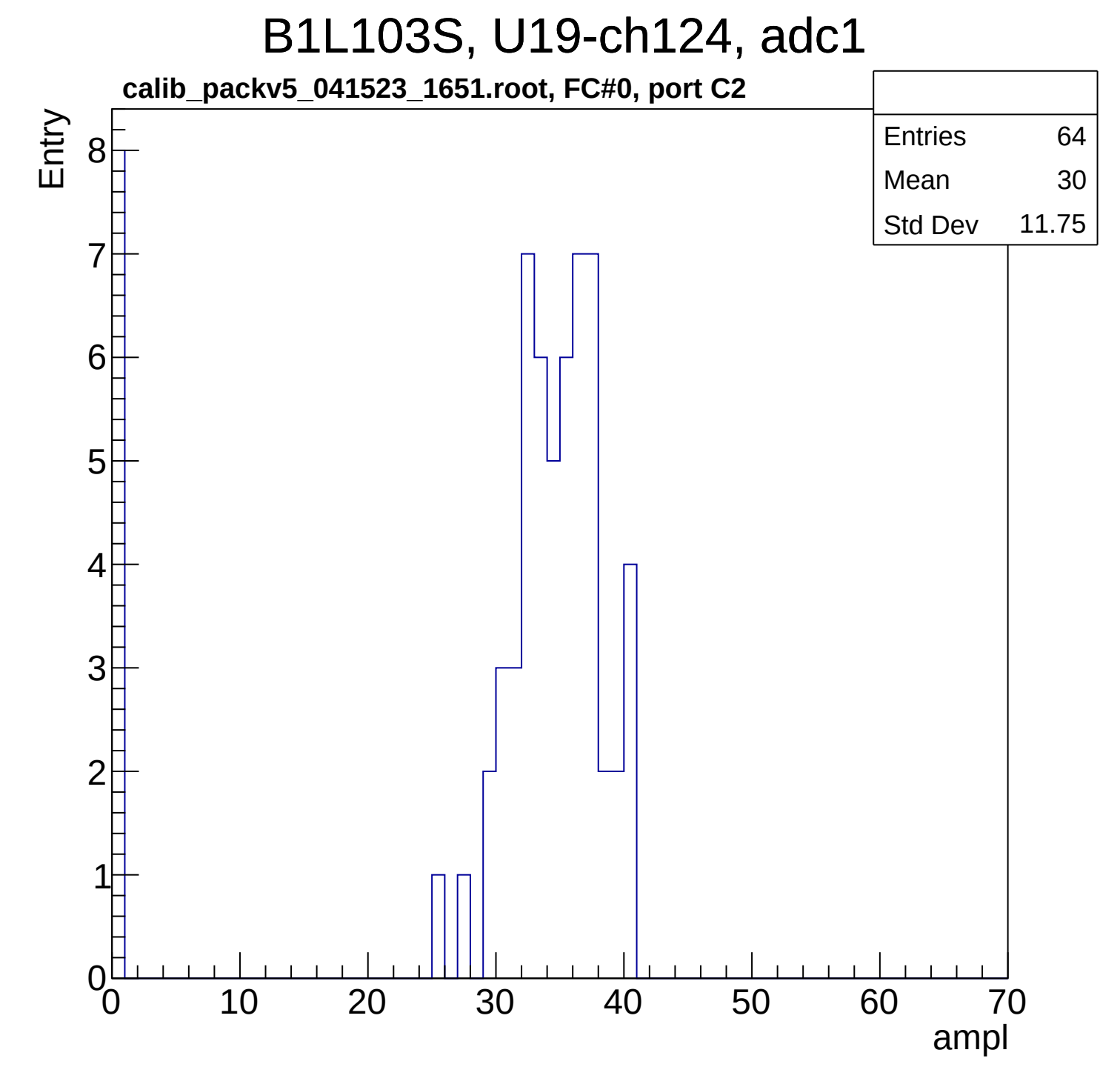
B1L103S, U19-ch124, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 30
Std Dev 11.75
Entry
ampl
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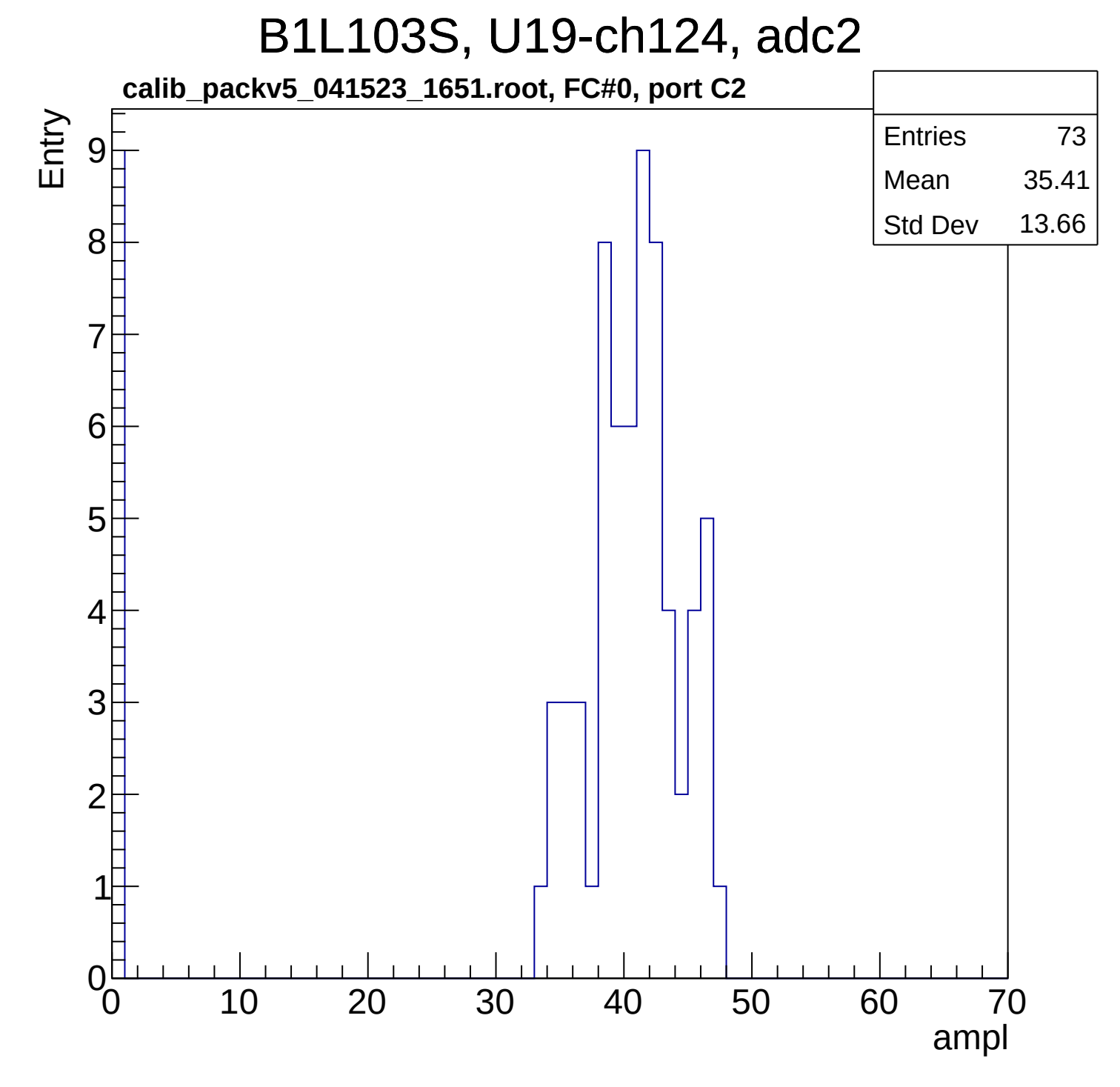
B1L103S, U19-ch124, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 35.41
Std Dev 13.66
Entry
ampl
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3
4
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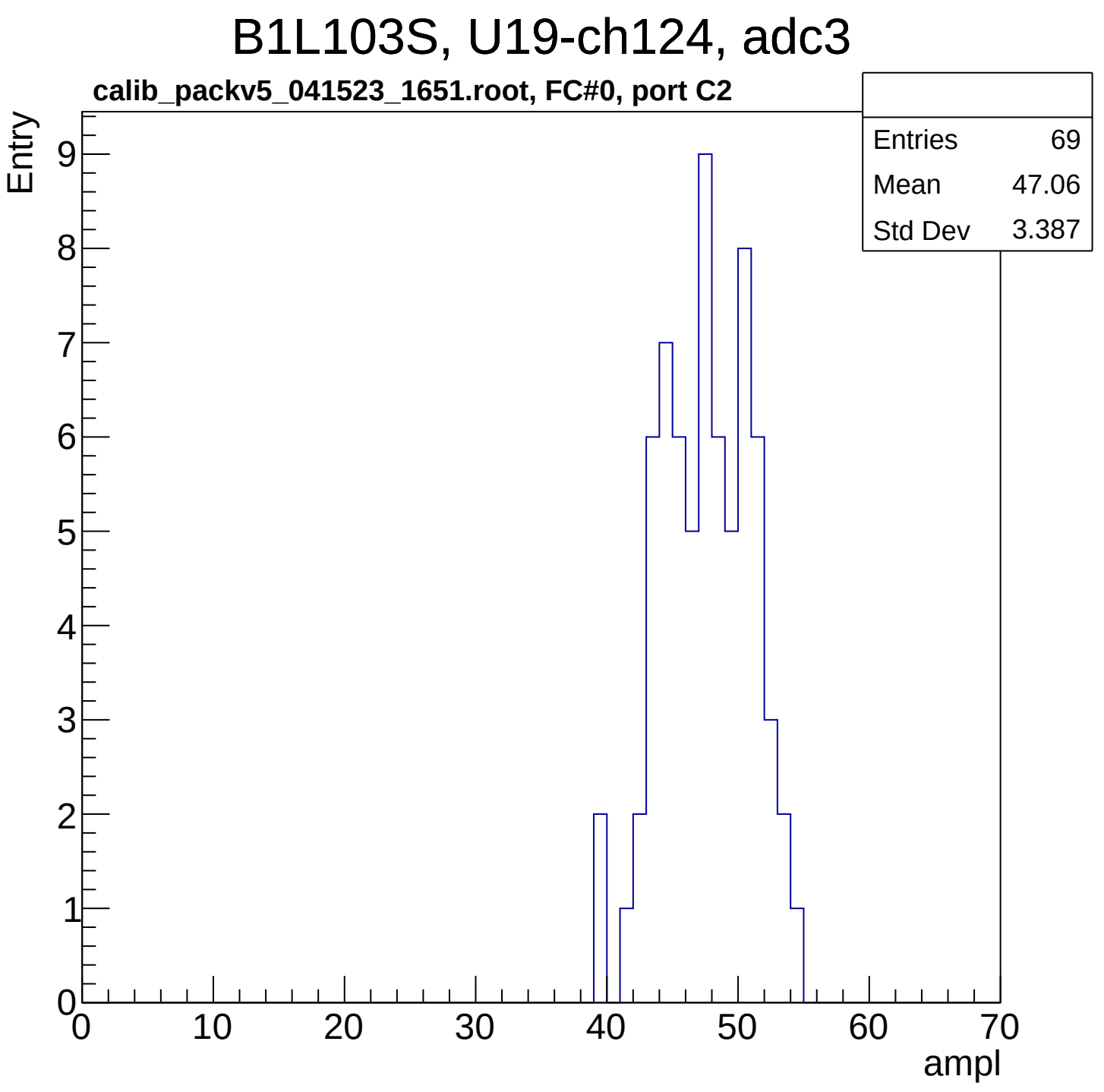
B1L103S, U19-ch124, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 47.06
Std Dev 3.387
Entry
ampl
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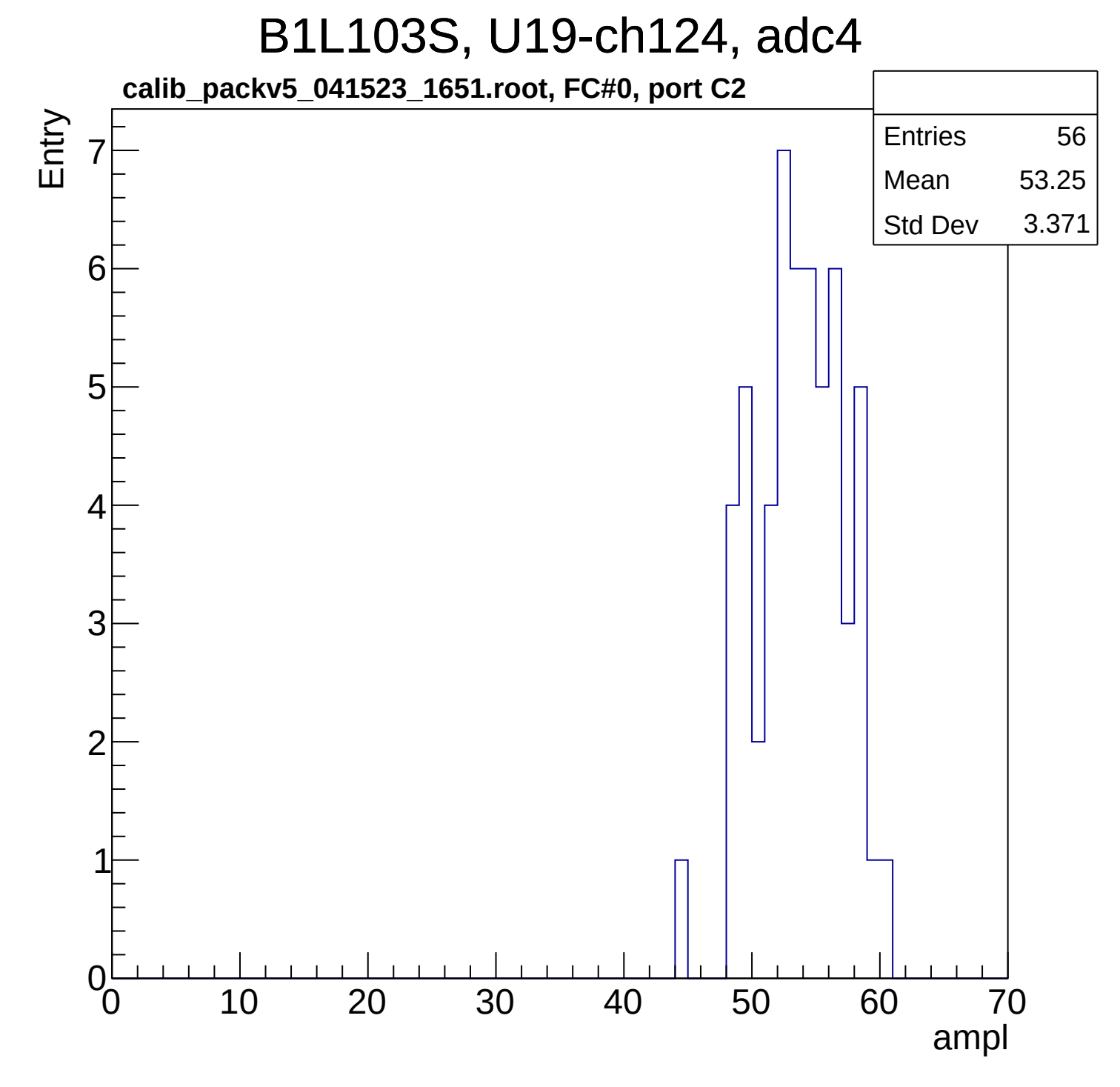
B1L103S, U19-ch124, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 53.25
Std Dev 3.371
Entry
ampl
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0
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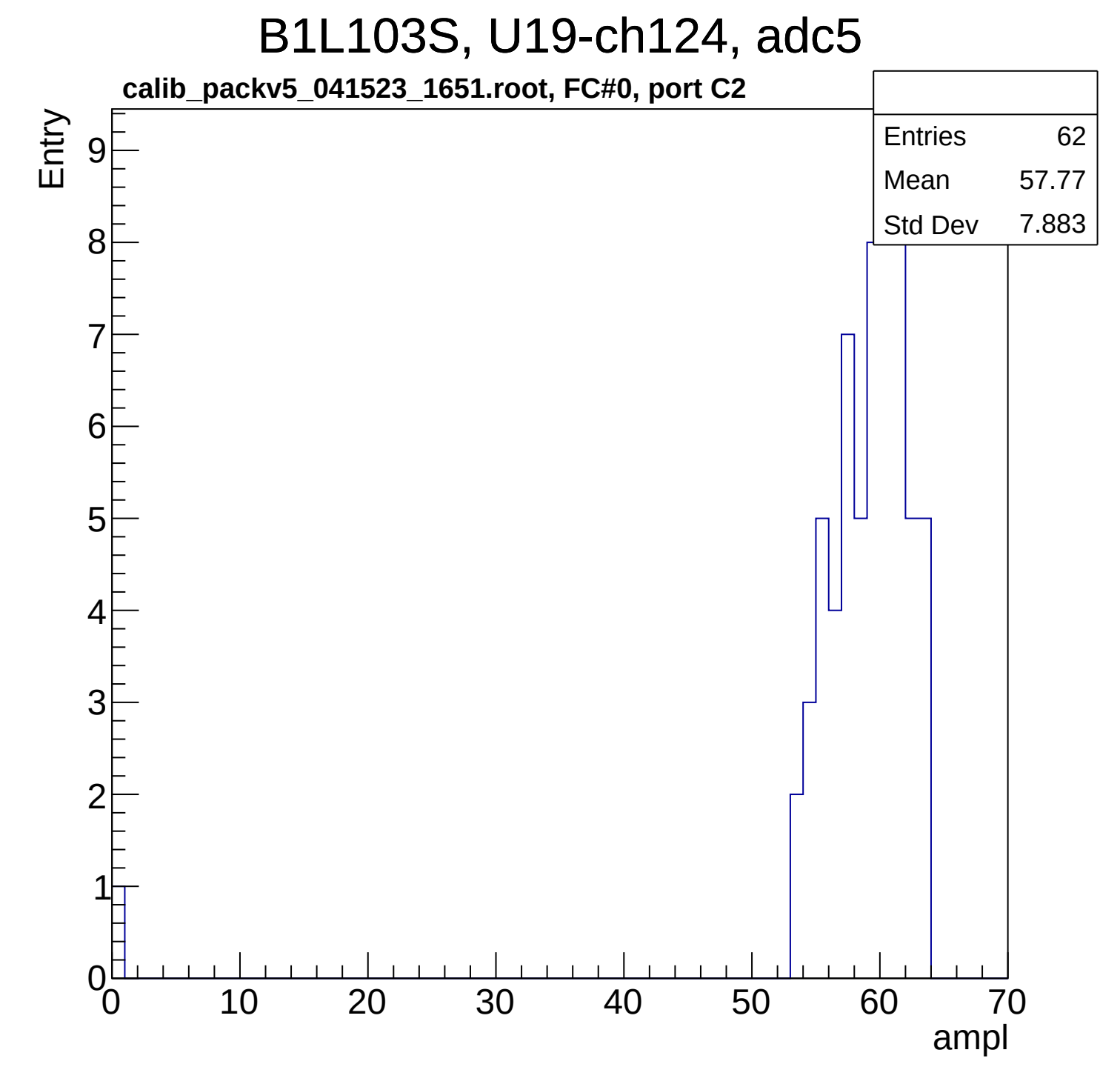
B1L103S, U19-ch124, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 57.77
Std Dev 7.883
Entry
ampl
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7
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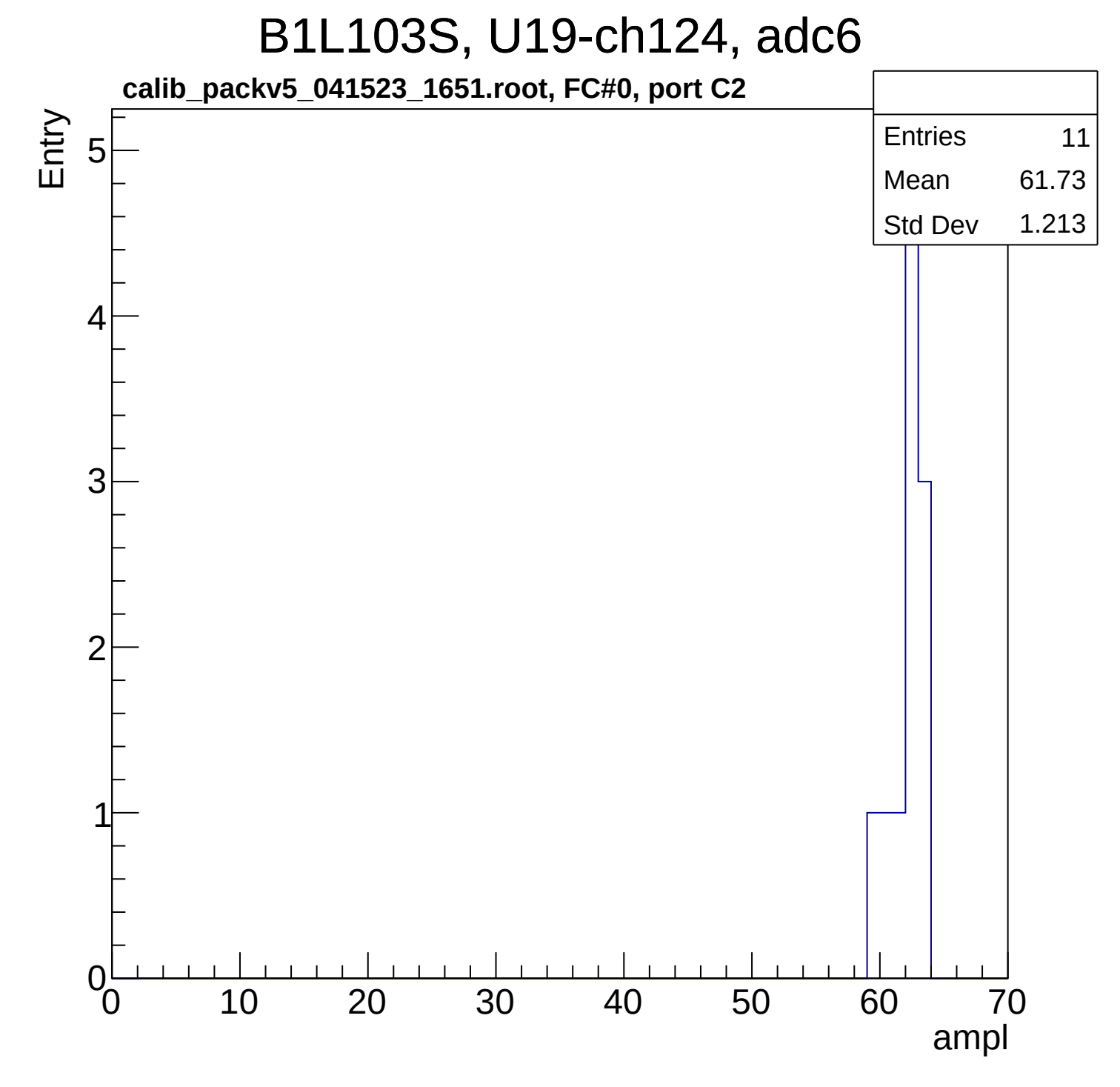
B1L103S, U19-ch124, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 61.73
Std Dev 1.213
Entry
ampl
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2
3
4
5
0
10
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30
40
50
60
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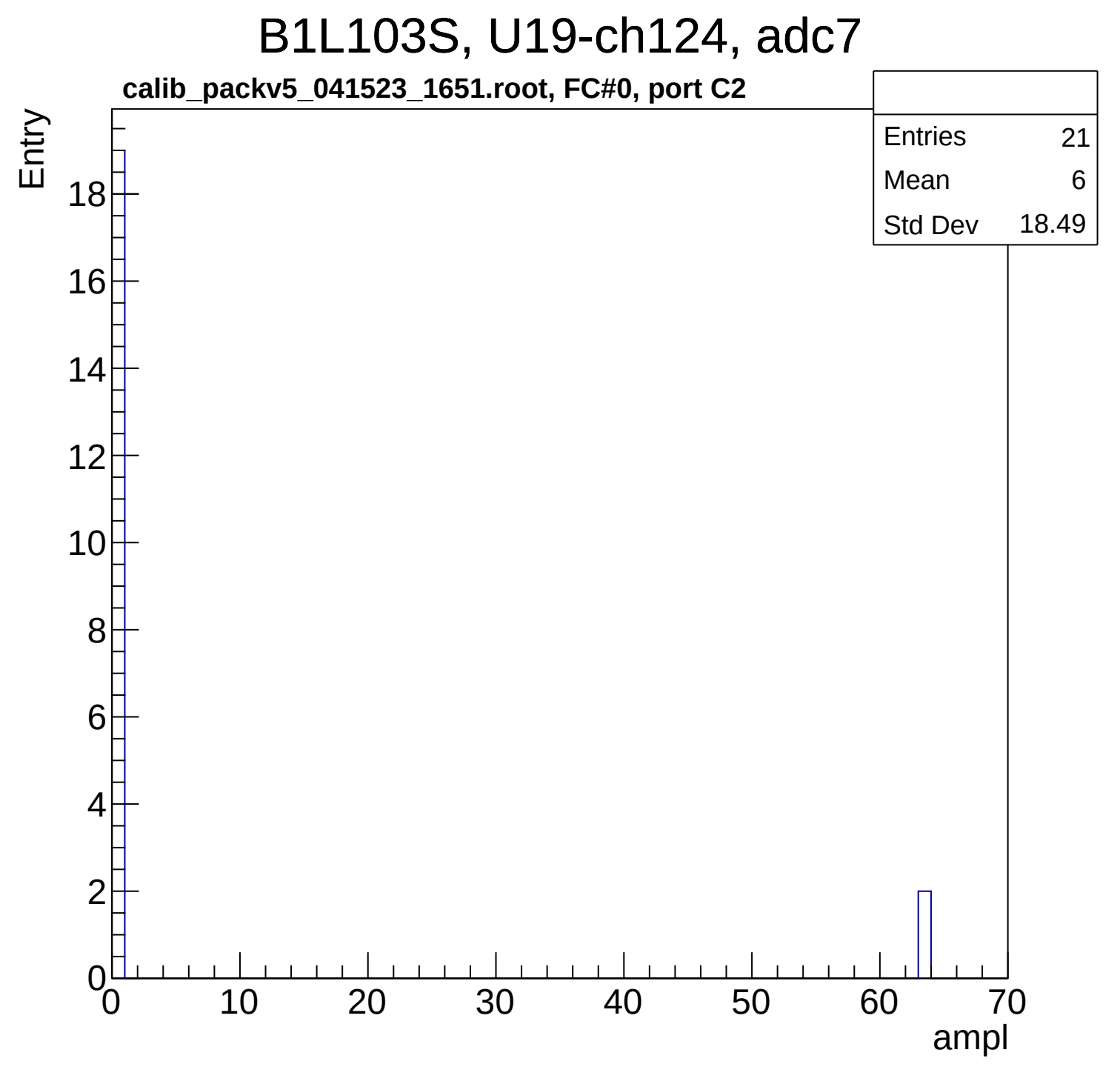
B1L103S, U19-ch124, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 6
Std Dev 18.49
Entry
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8
10
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14
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50
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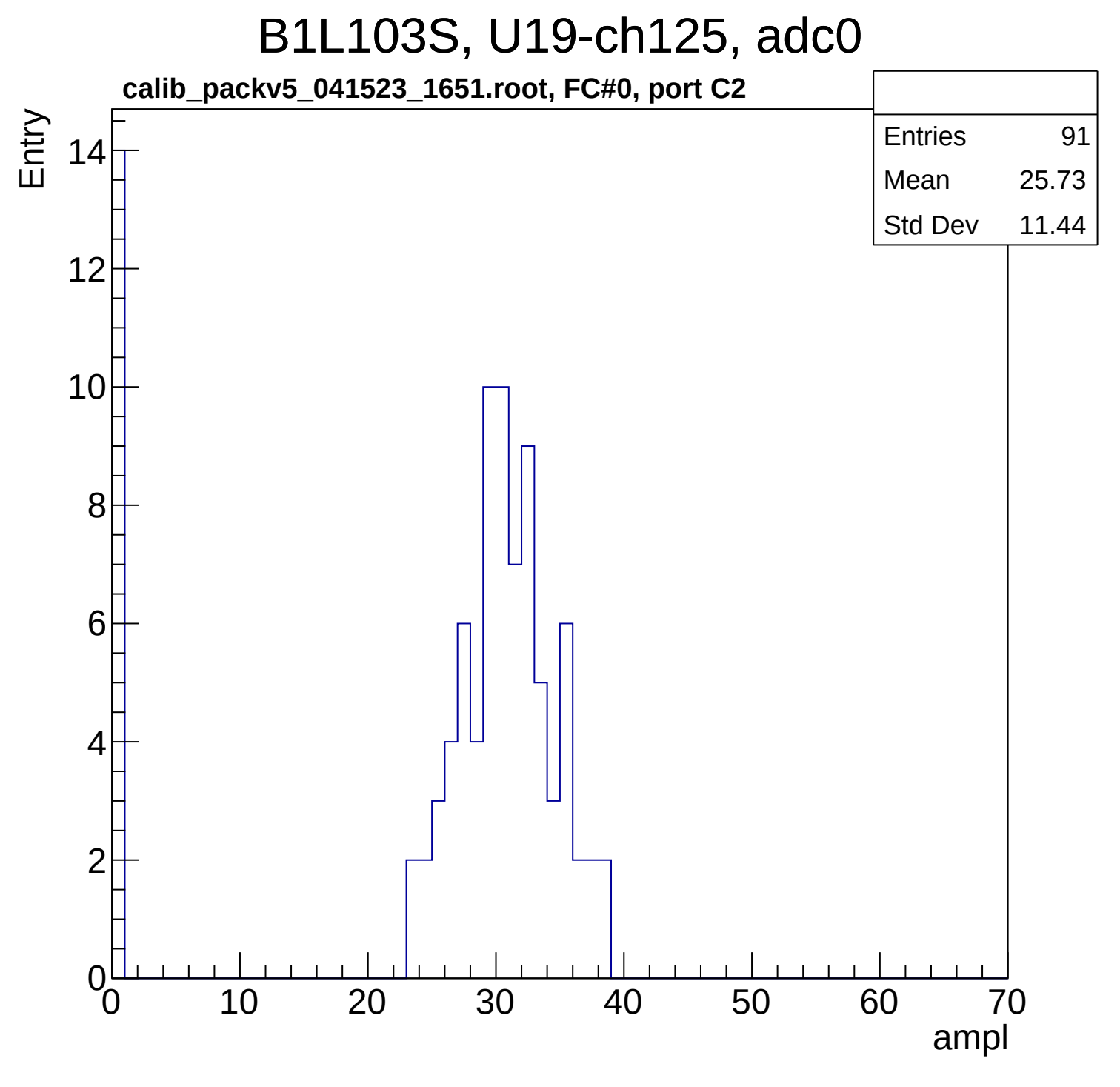
ampl


B1L103S, U19-ch125, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 25.73
Std Dev 11.44
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
30
40
50
60
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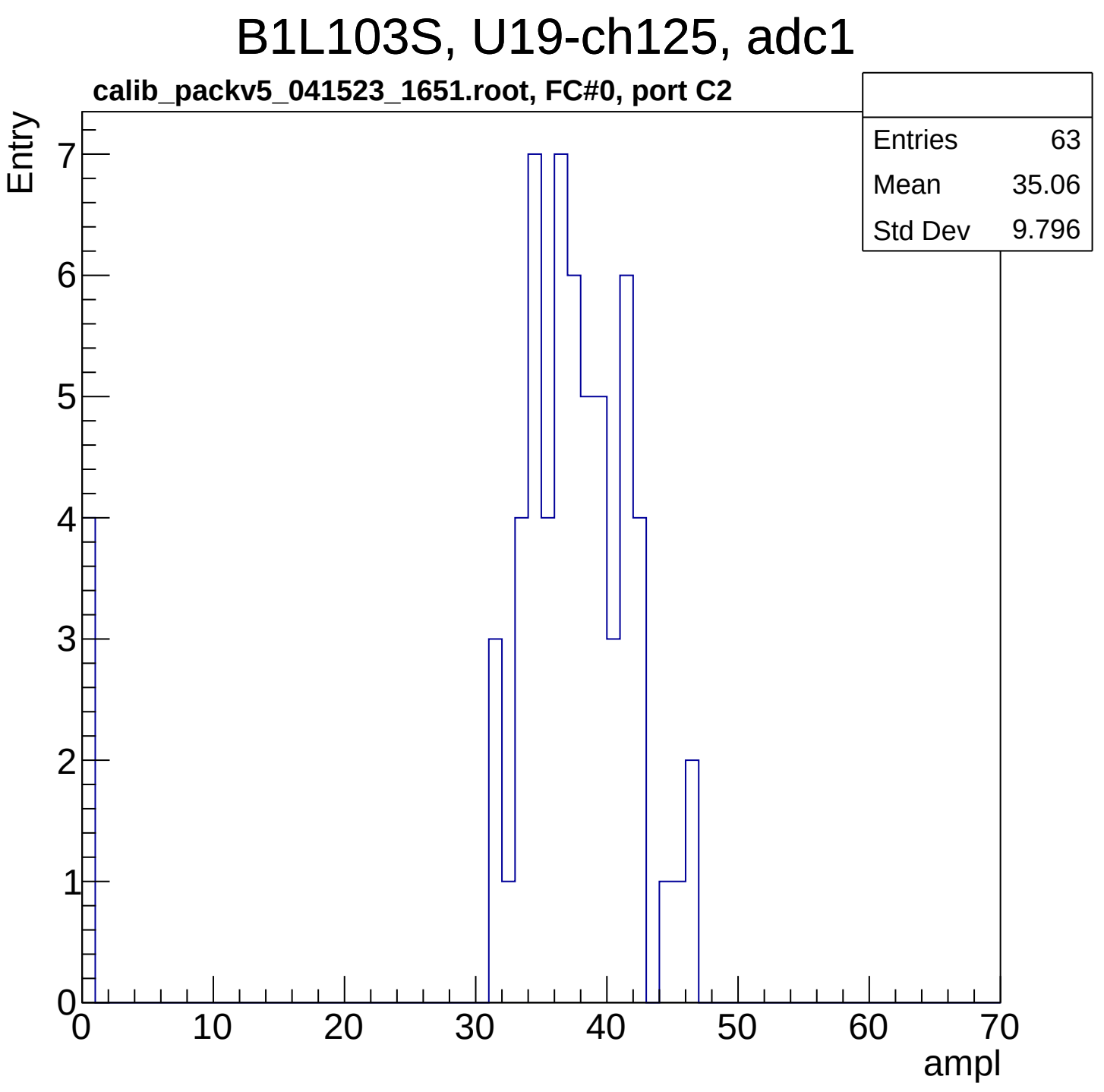
B1L103S, U19-ch125, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 35.06
Std Dev 9.796
Entry
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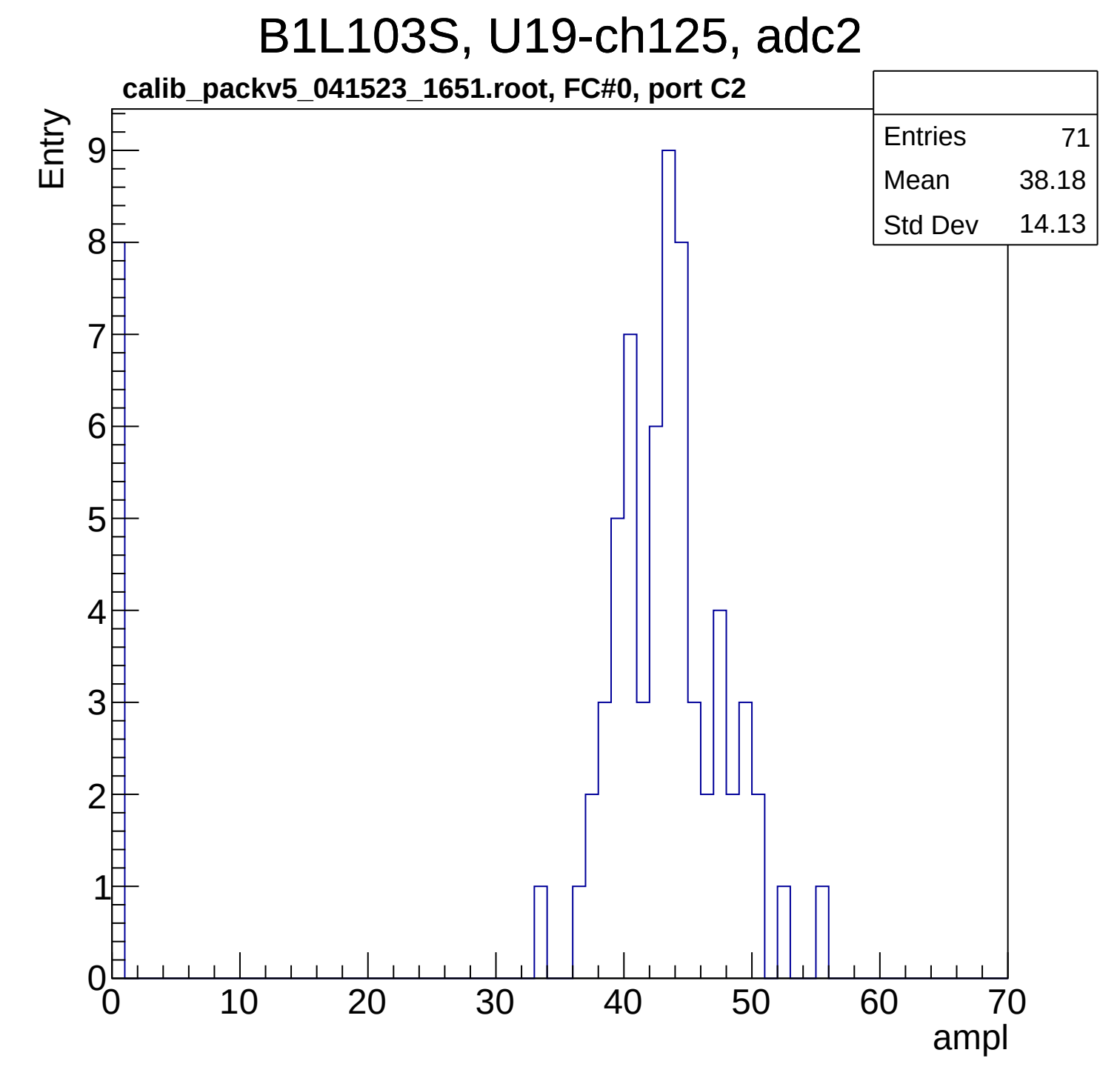
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch125, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 38.18
Std Dev 14.13
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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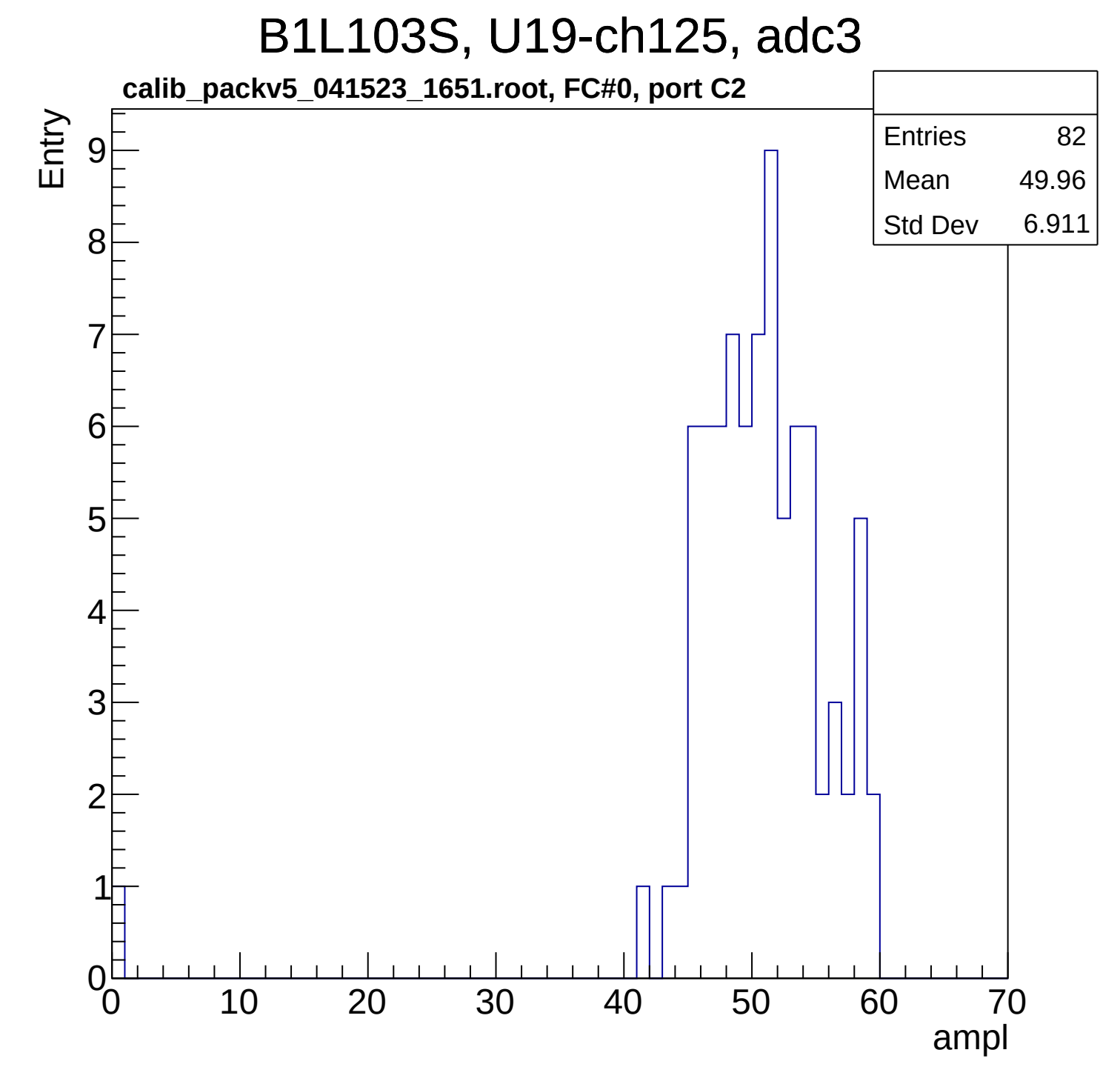
B1L103S, U19-ch125, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 49.96
Std Dev 6.911
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
50
60
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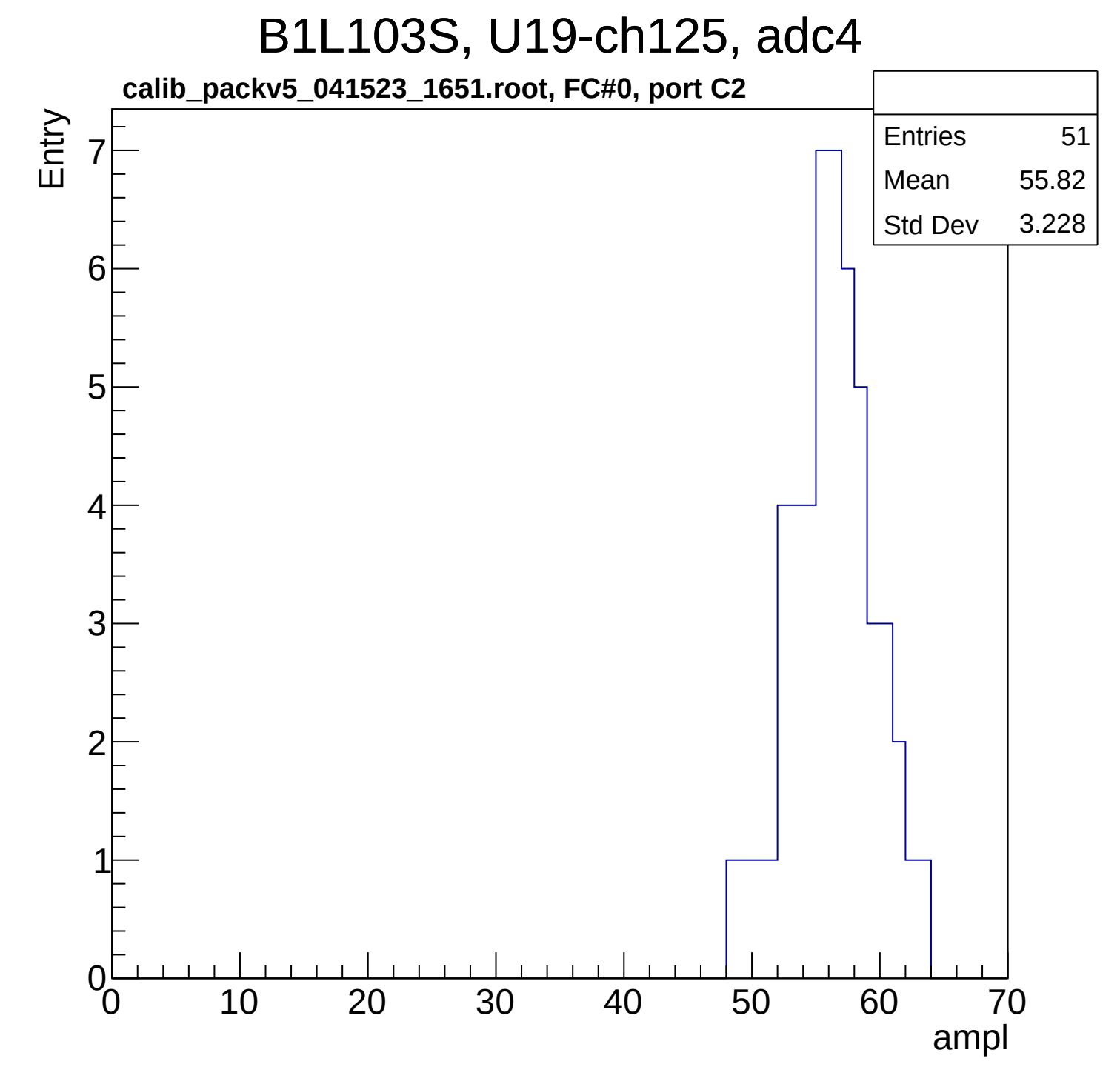
B1L103S, U19-ch125, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 55.82
Std Dev 3.228
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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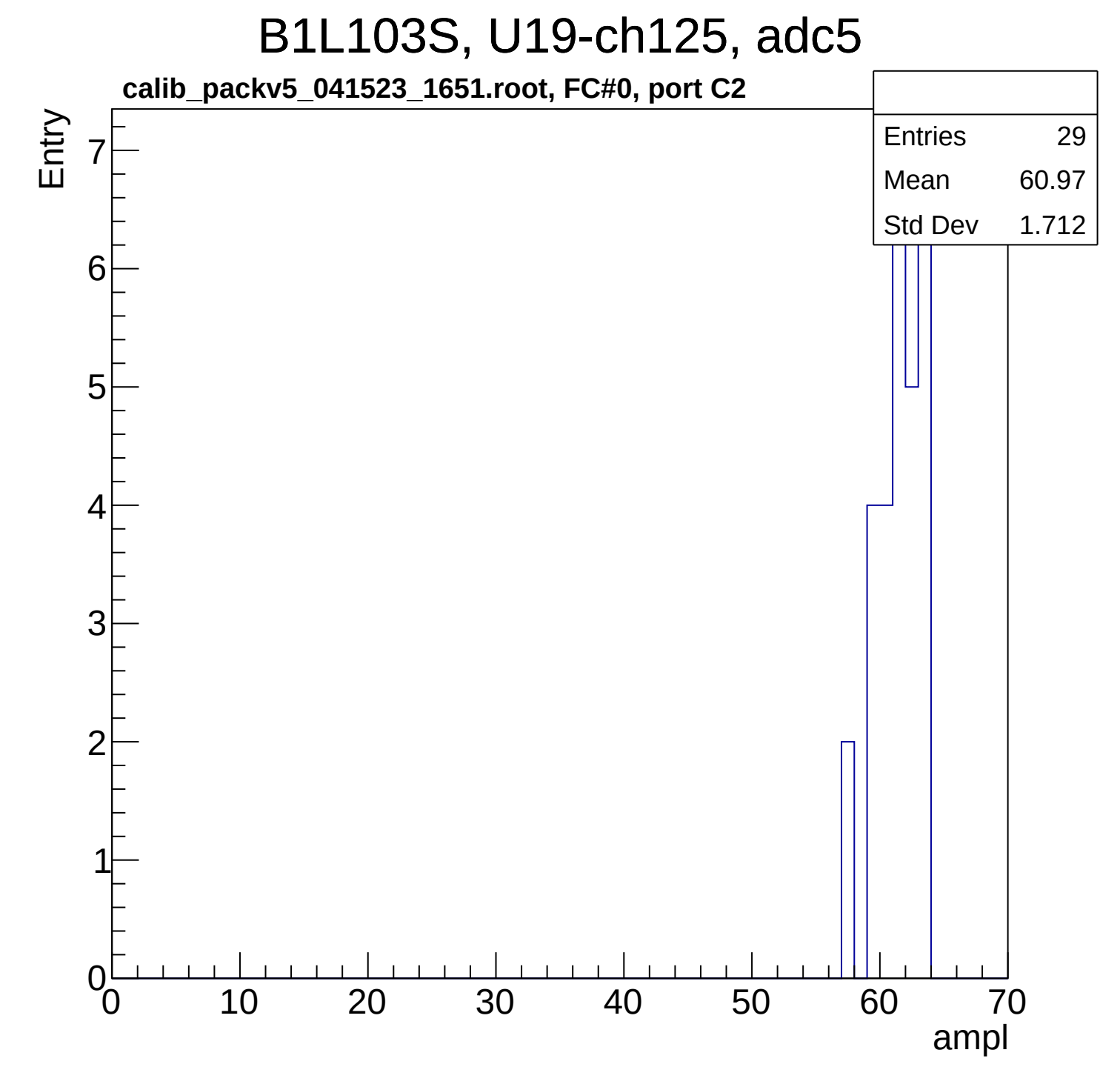
B1L103S, U19-ch125, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 60.97
Std Dev 1.712
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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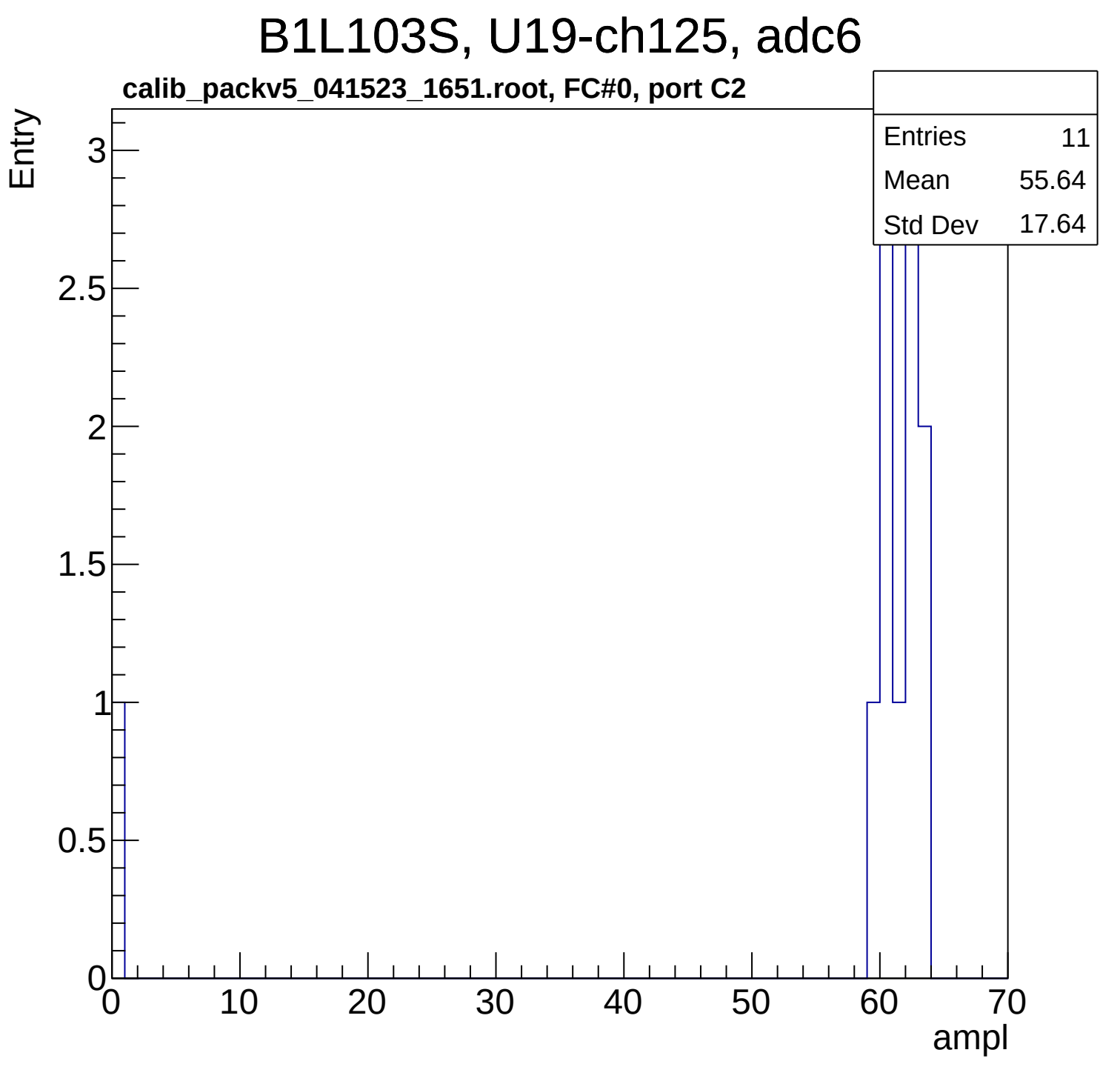
B1L103S, U19-ch125, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 55.64
Std Dev 17.64
Entry
ampl
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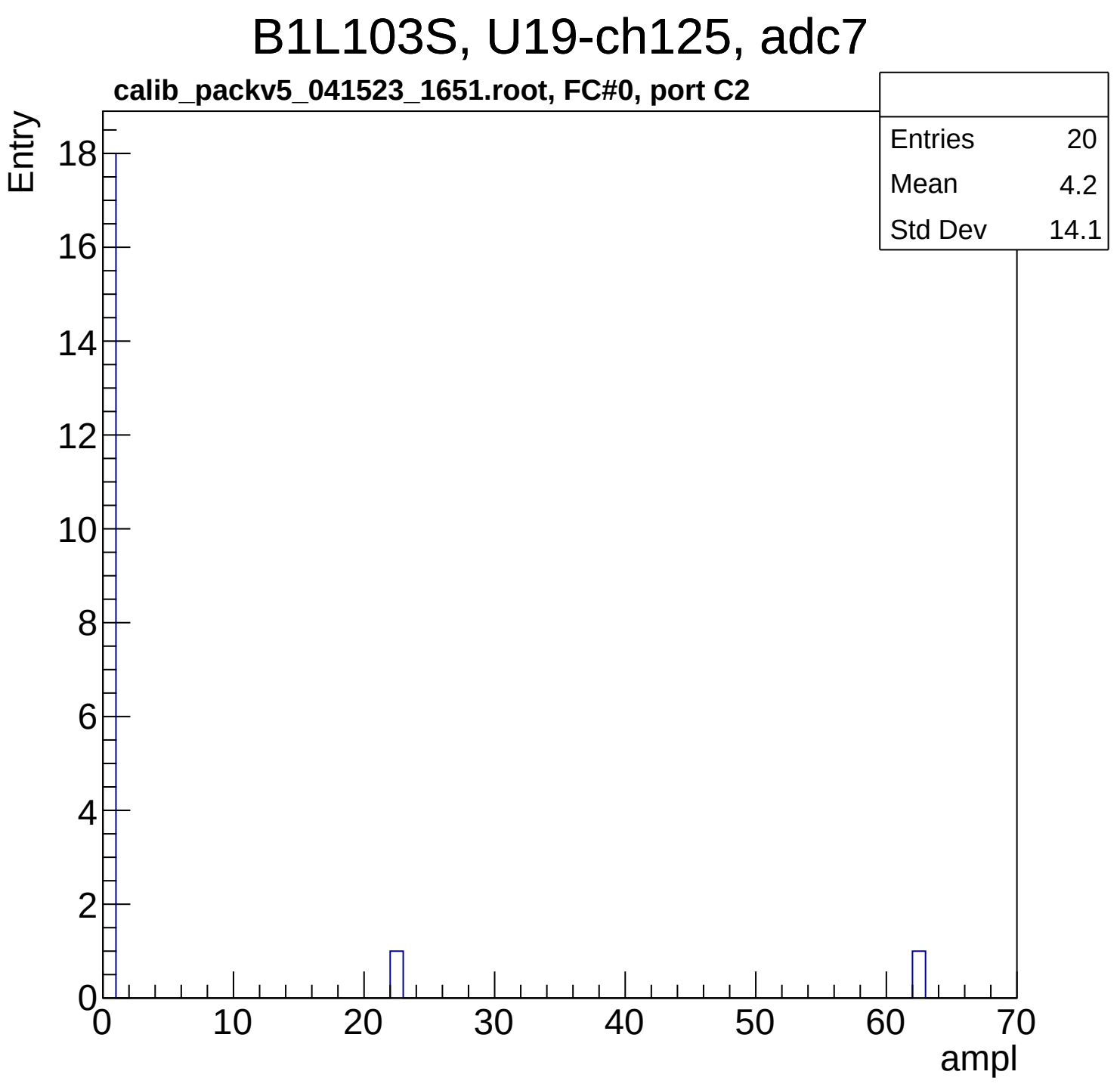
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U19-ch125, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4.2
Std Dev 14.1
Entry
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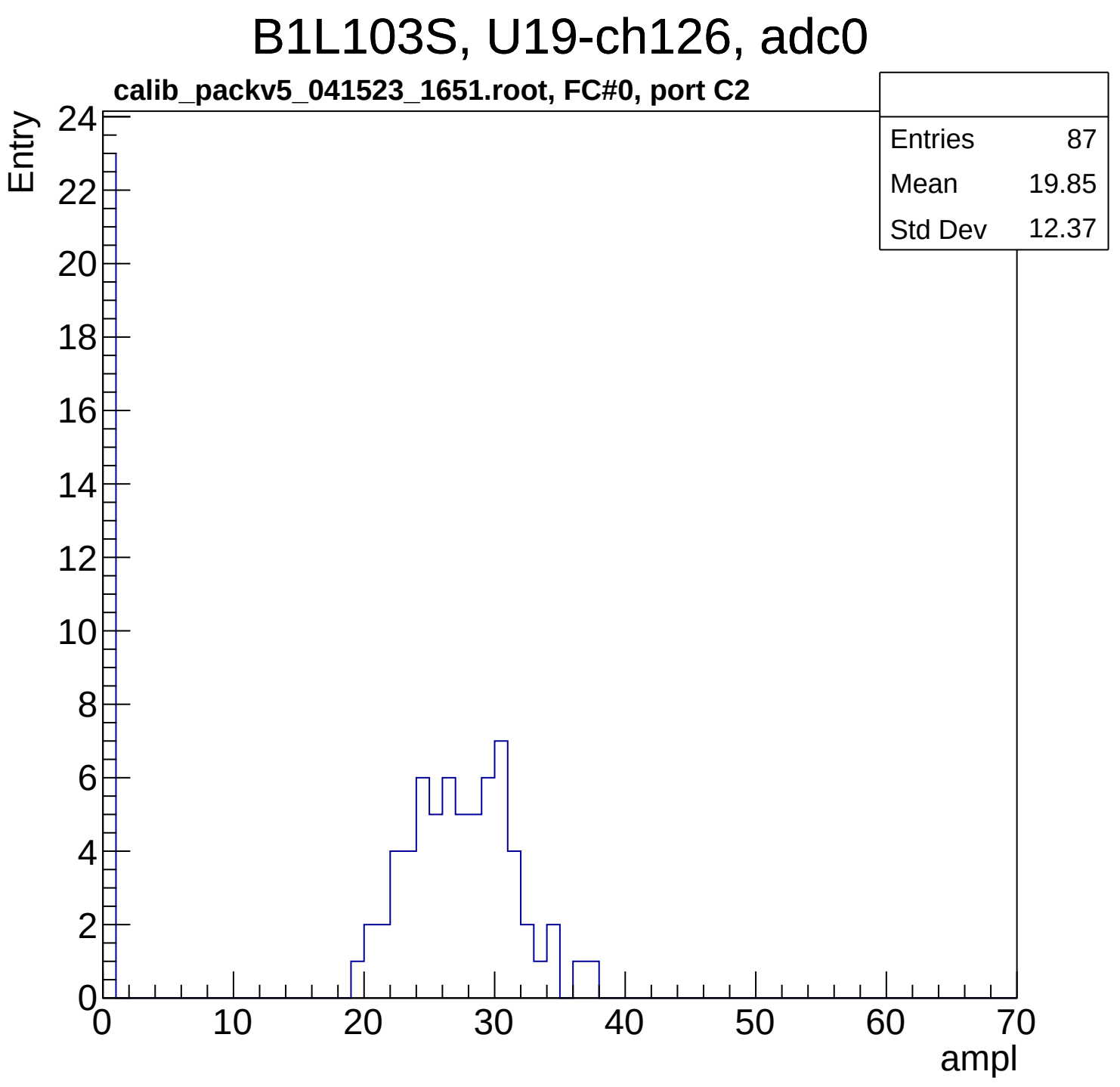
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch126, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 19.85
Std Dev 12.37
Entry
ampl
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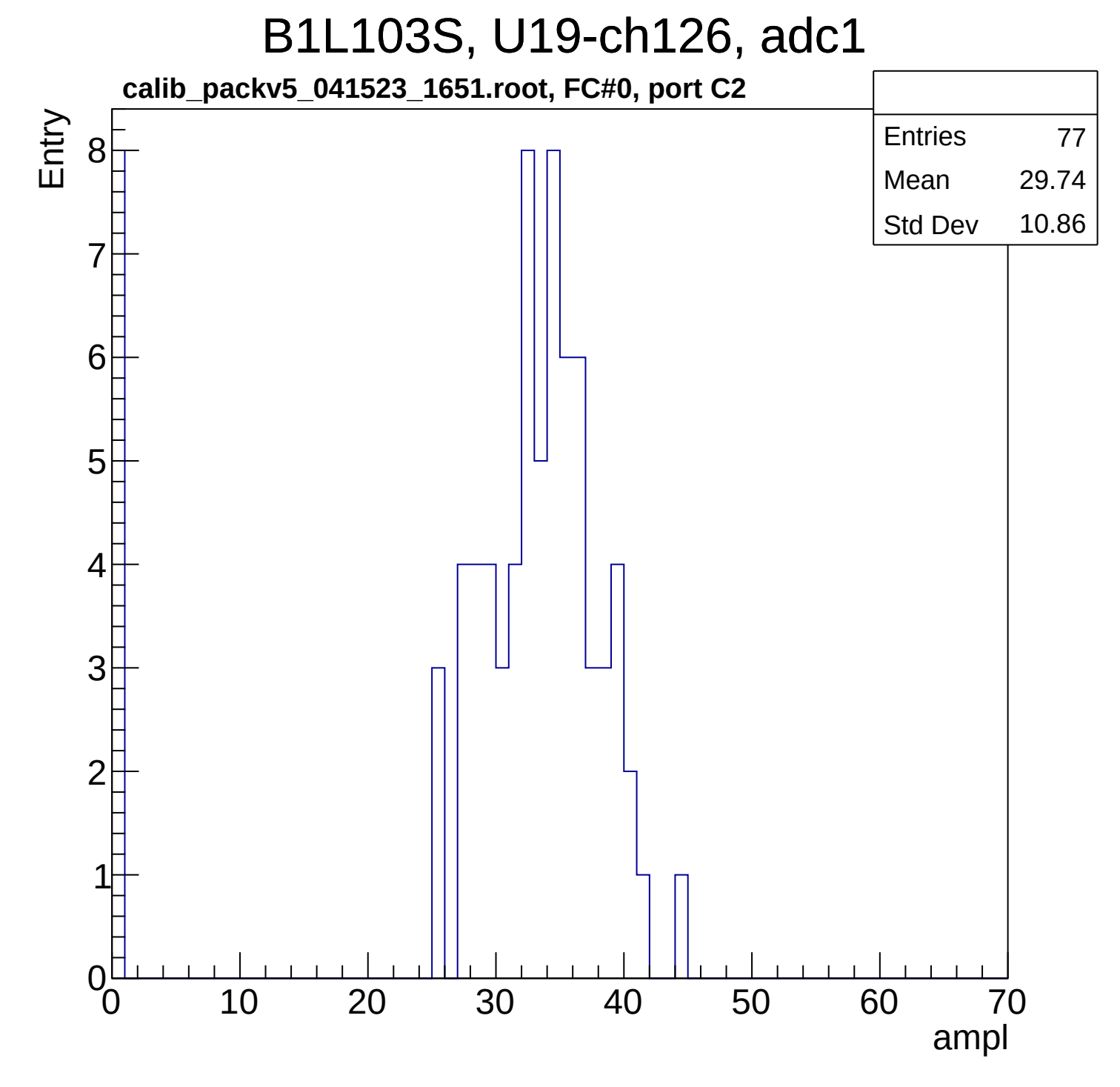
4
6
8
10
12
14
16
18
20
22
24
0
10
20
30
40
50
60
70


B1L103S, U19-ch126, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 29.74
Std Dev 10.86
Entry
ampl
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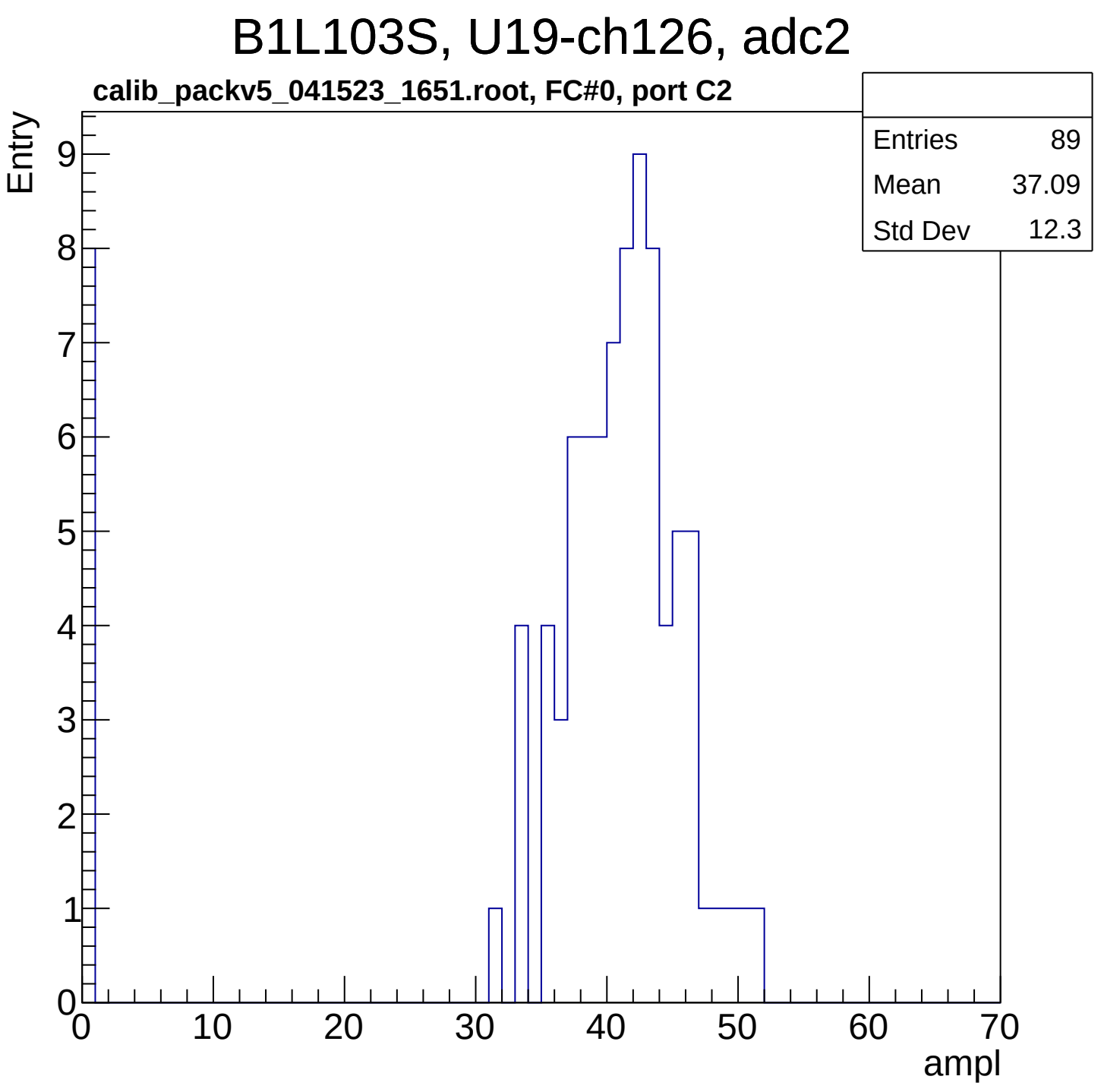
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch126, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 37.09
Std Dev 12.3
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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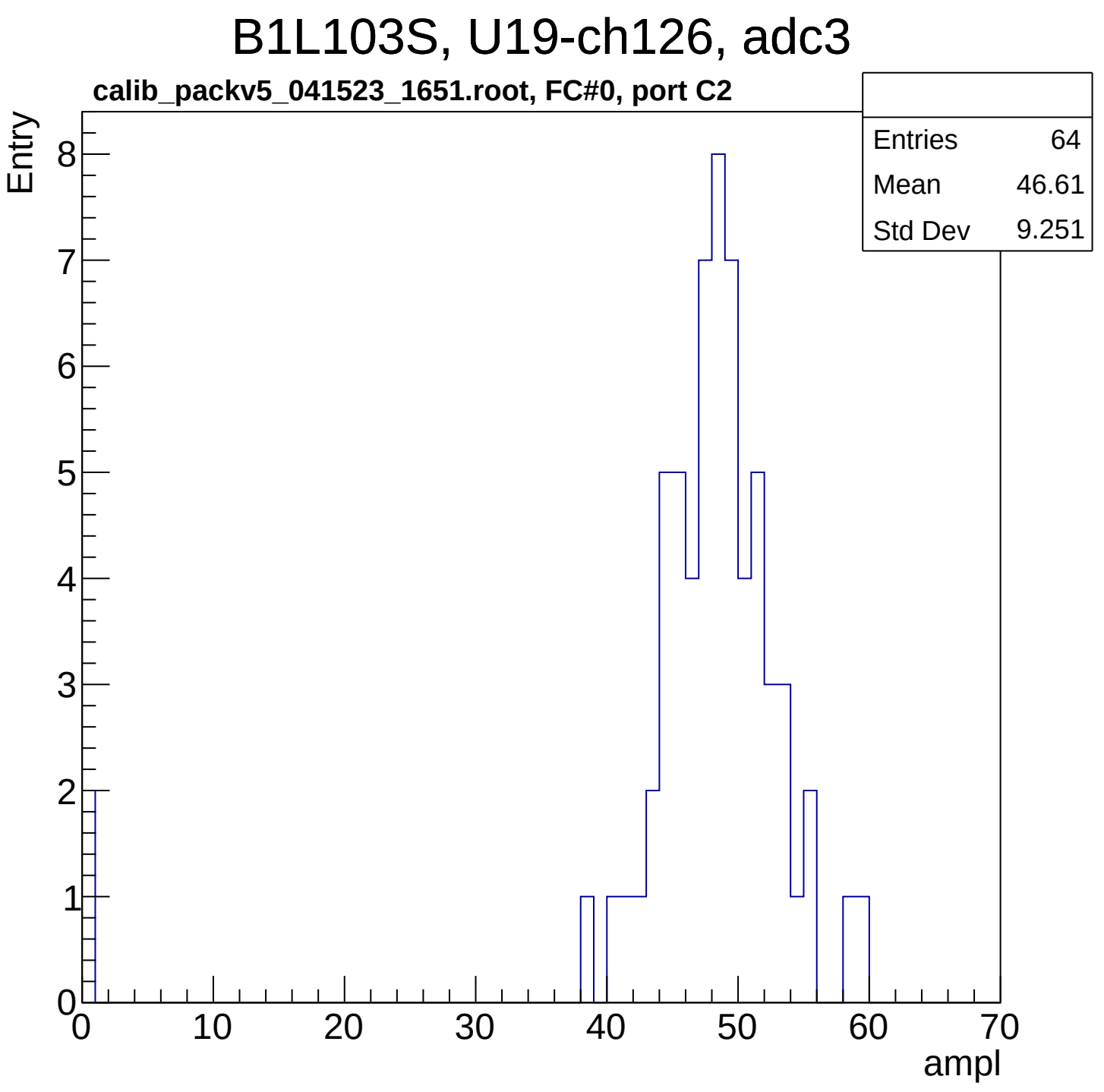
B1L103S, U19-ch126, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 46.61
Std Dev 9.251
Entry
ampl
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2
3
4
5
6
7
8
0
10
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40
50
60
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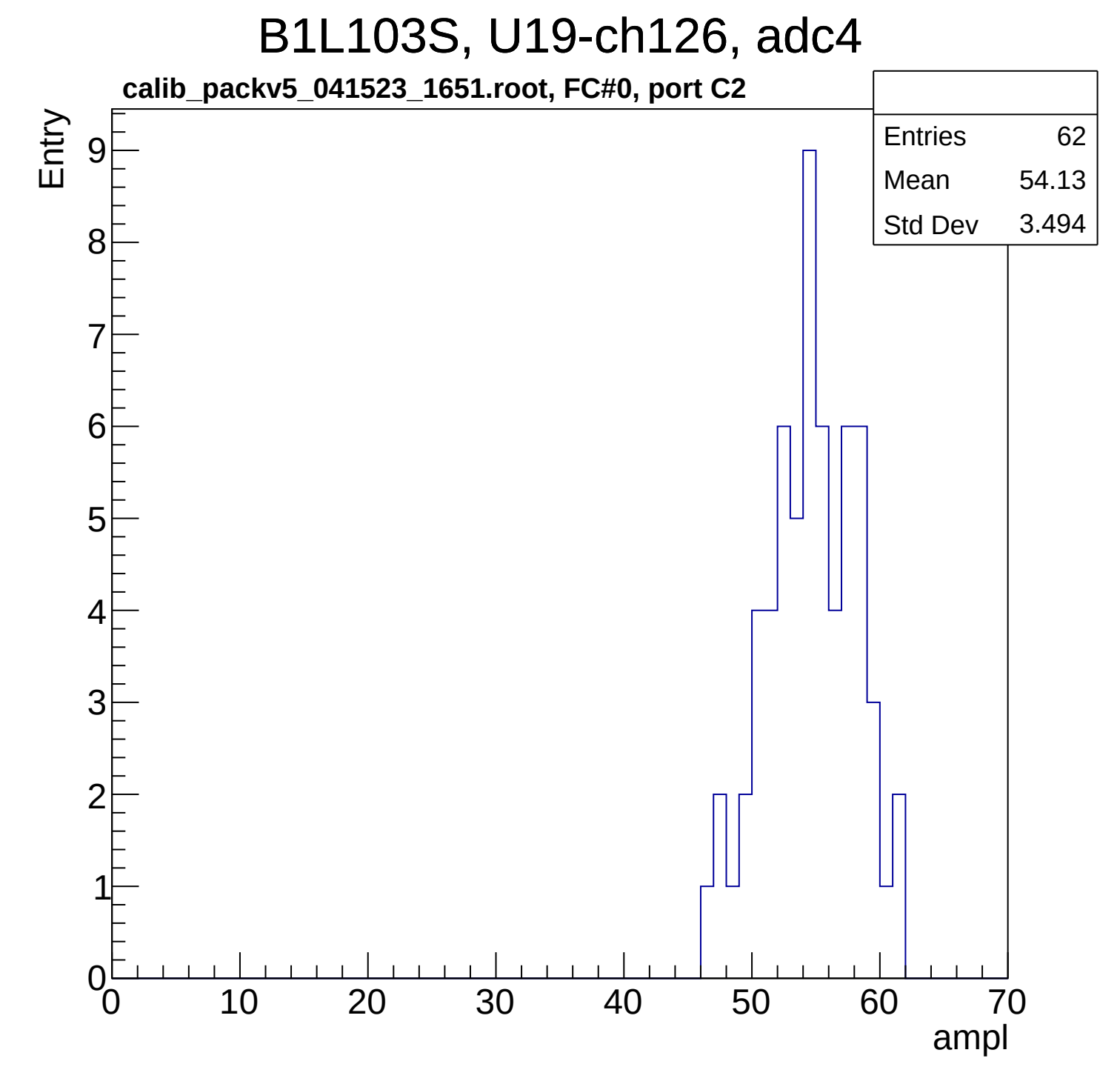
B1L103S, U19-ch126, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 54.13
Std Dev 3.494
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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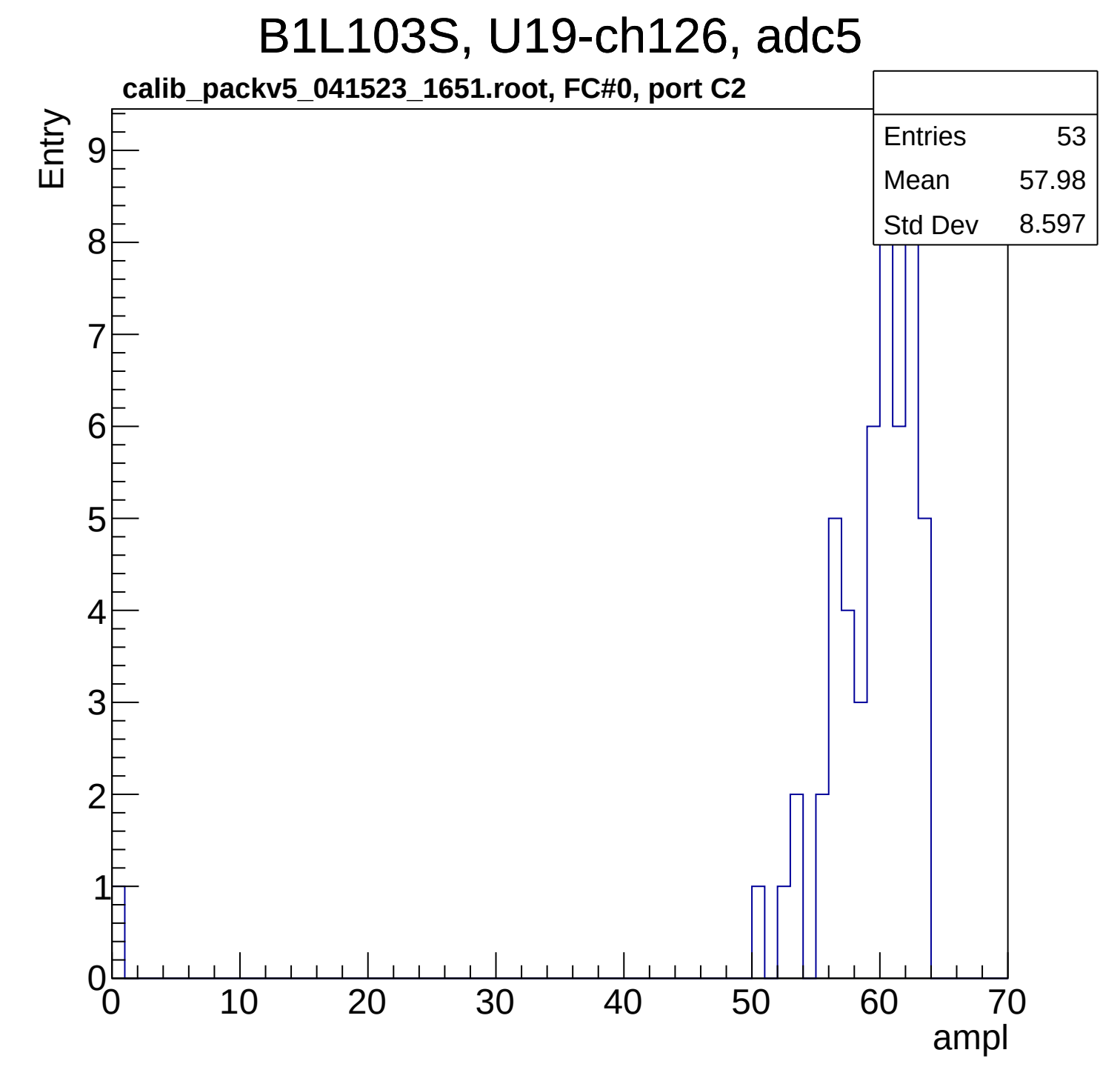
B1L103S, U19-ch126, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 57.98
Std Dev 8.597
Entry
ampl
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3
4
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6
7
8
9
0
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20
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40
50
60
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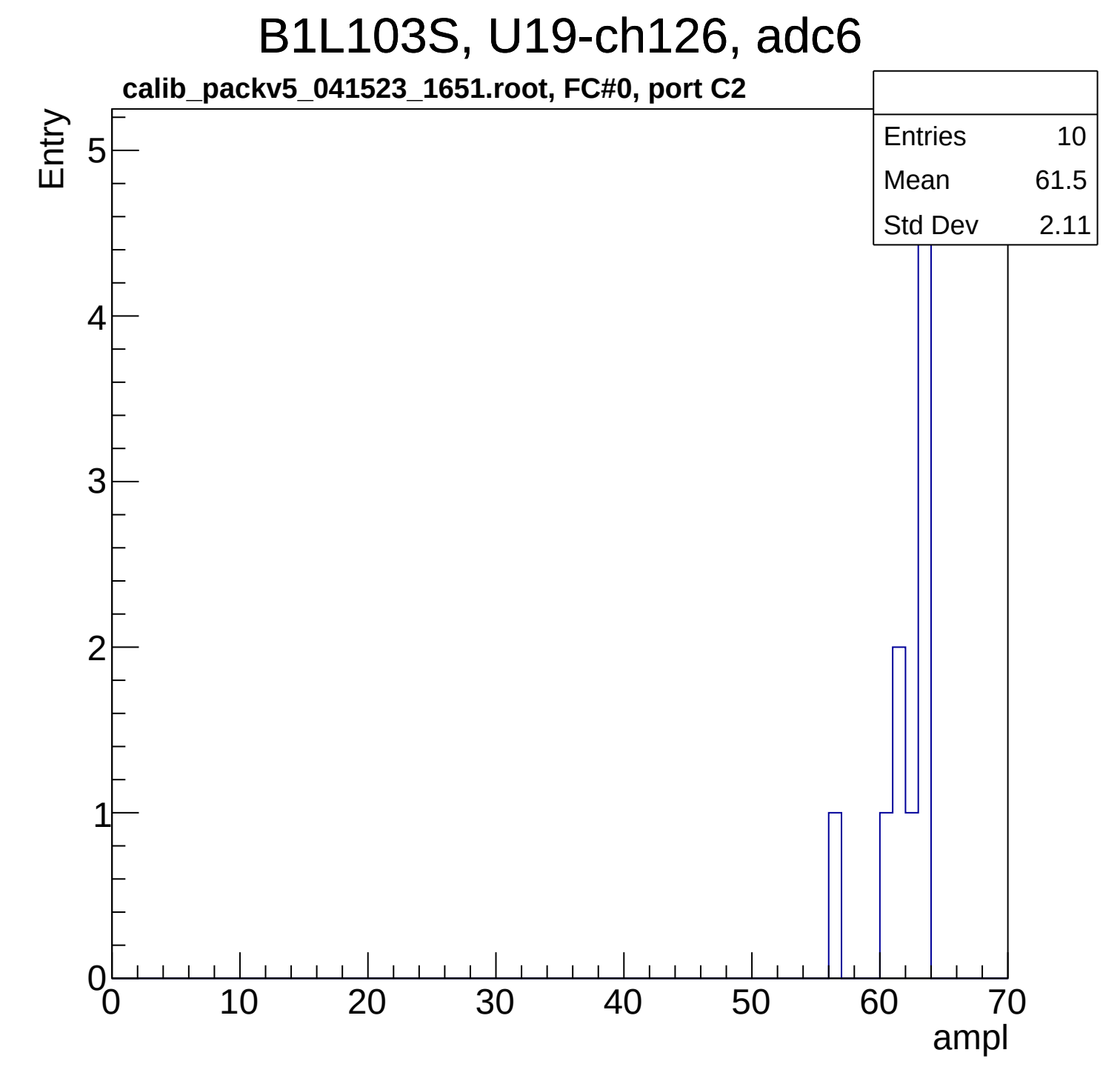
B1L103S, U19-ch126, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61.5
Std Dev 2.11
Entry
ampl
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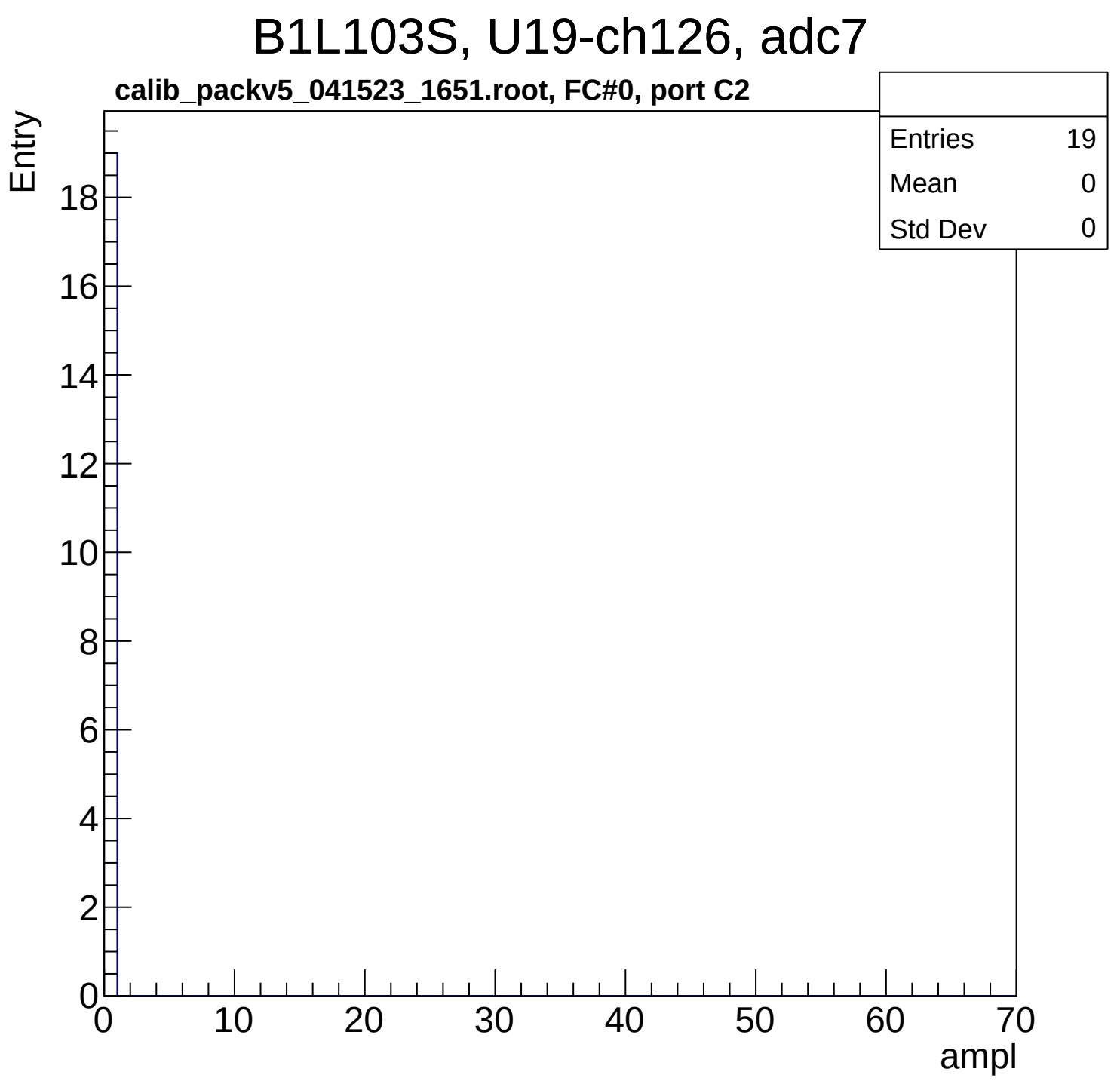
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U19-ch126, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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6
8
10
12
14
16
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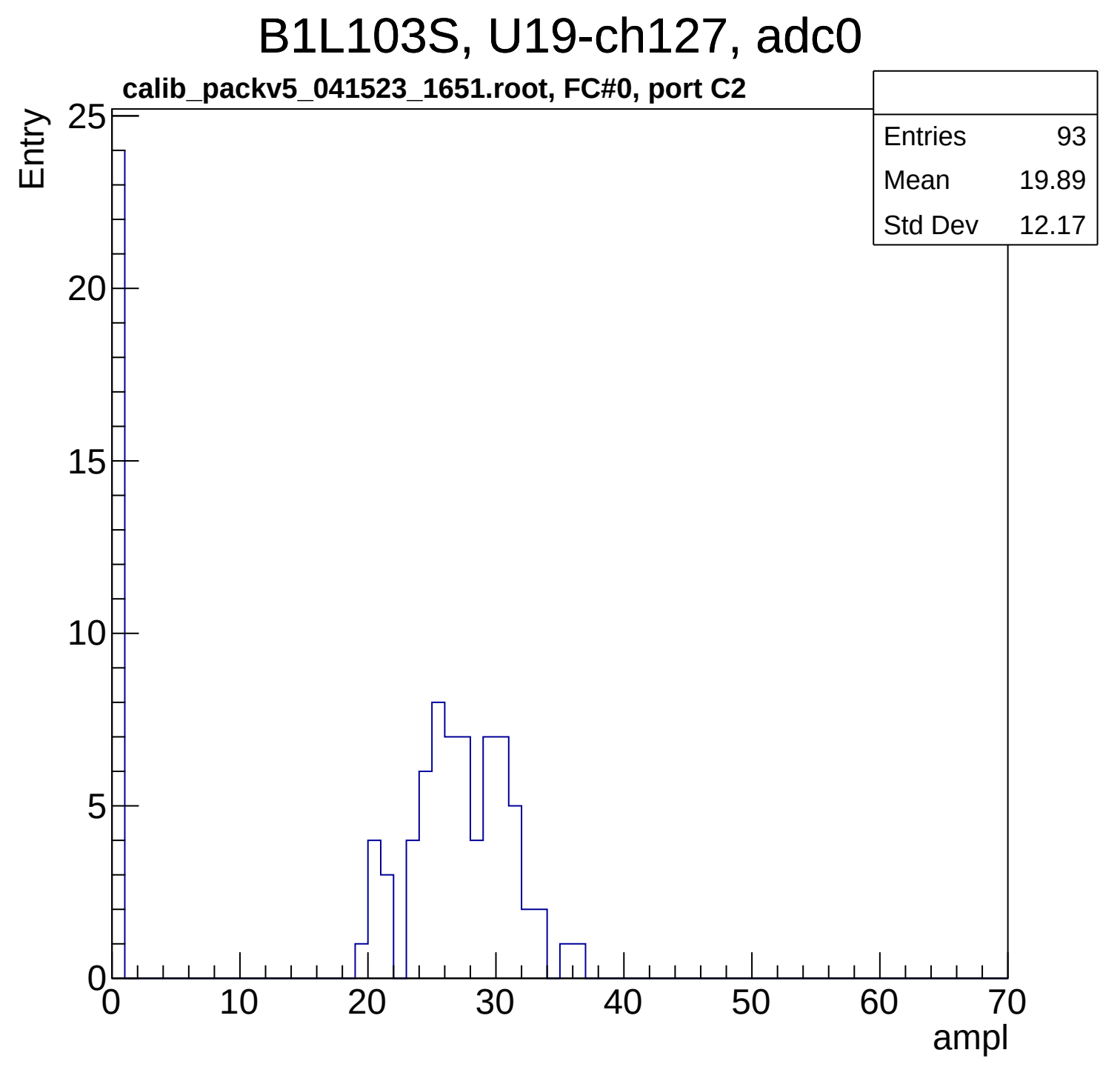
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch127, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 19.89
Std Dev 12.17
Entry
ampl
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10
15
20
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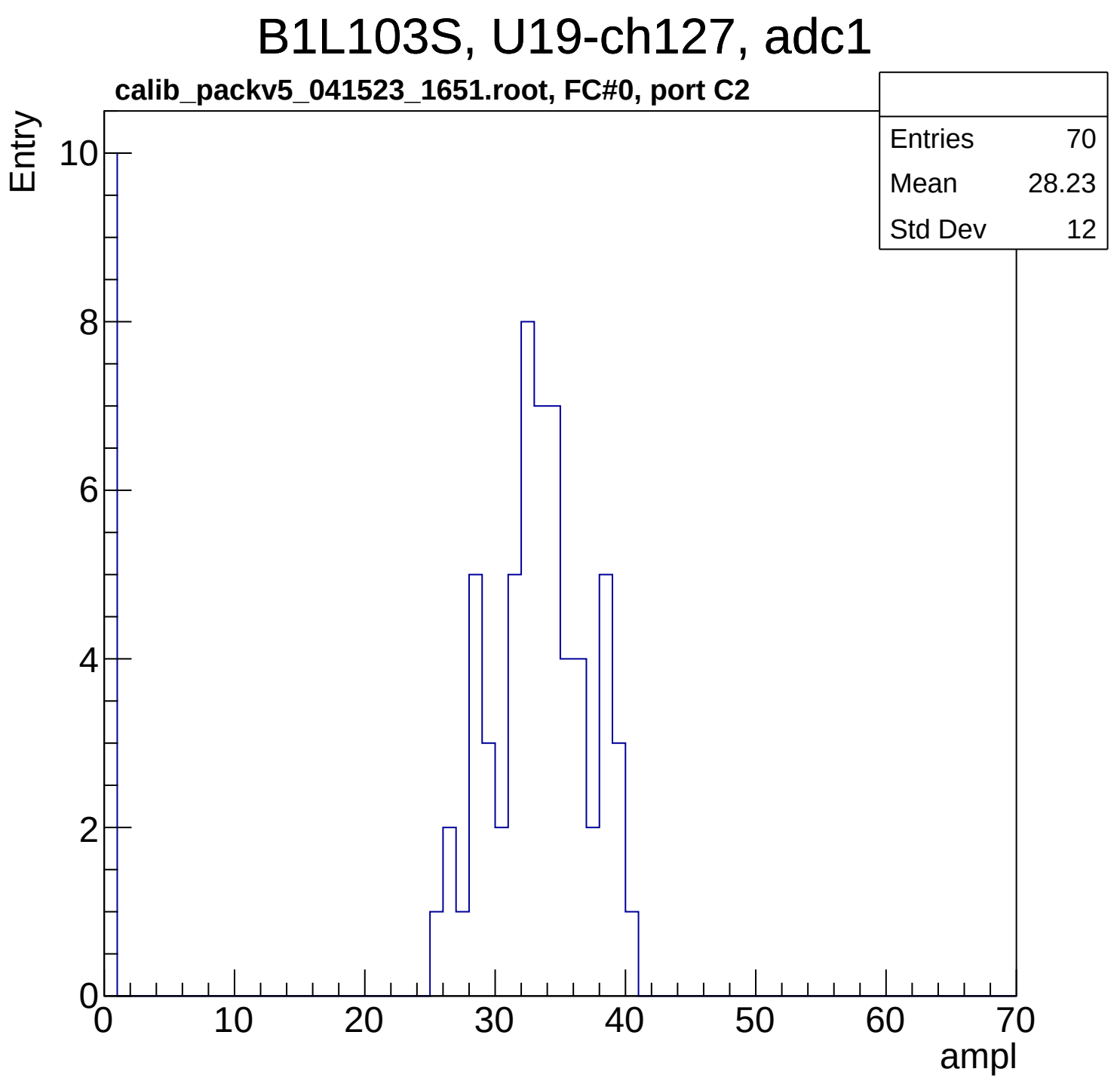
40
50
60
70


B1L103S, U19-ch127, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 28.23
Std Dev 12
Entry
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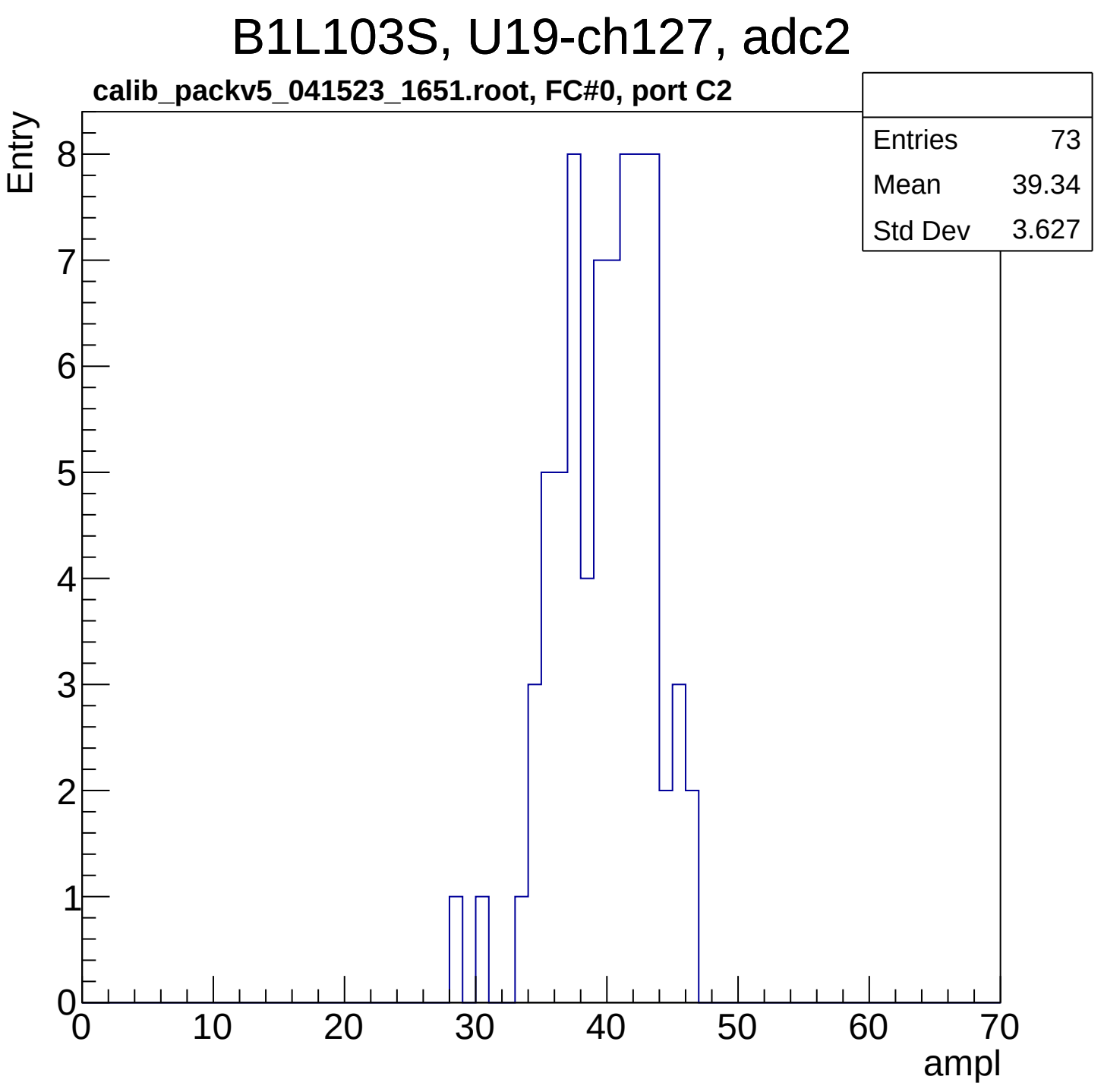
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U19-ch127, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 39.34
Std Dev 3.627
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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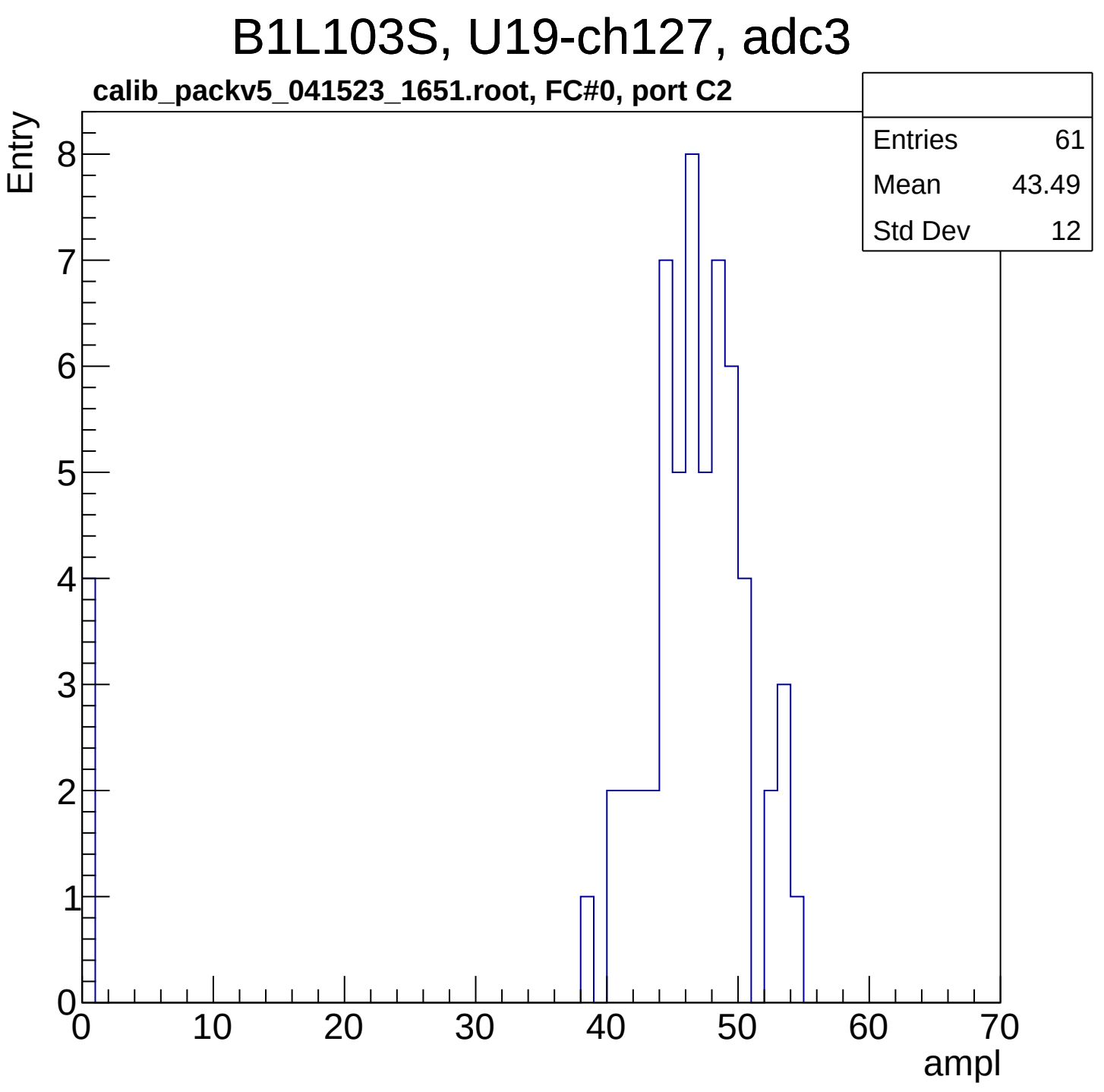
60
70


B1L103S, U19-ch127, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 43.49
Std Dev 12
Entry
ampl
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1
2
3
4
5
6
7
8
0
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60
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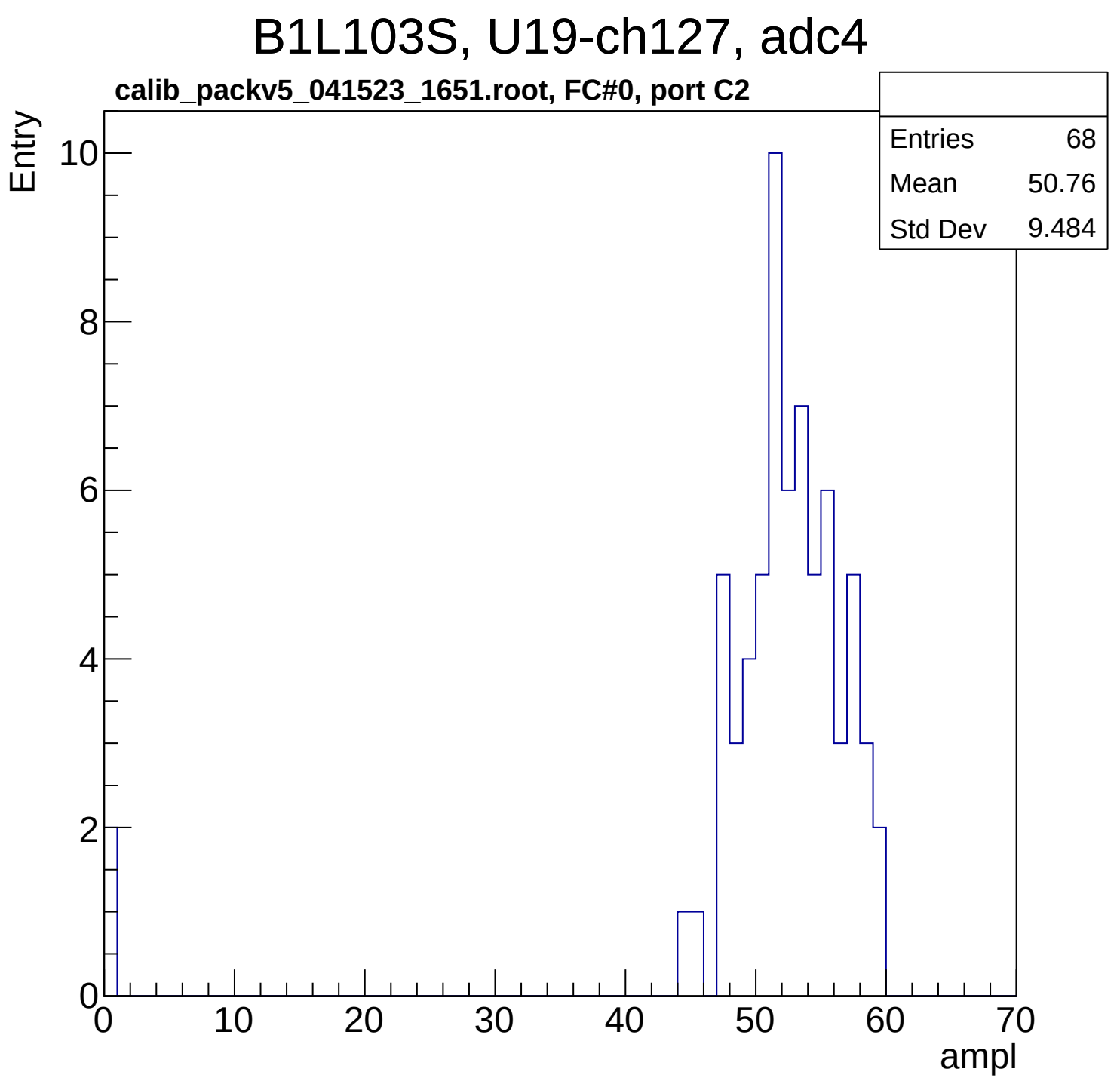
B1L103S, U19-ch127, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 50.76
Std Dev 9.484
Entry
ampl
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10
0
10
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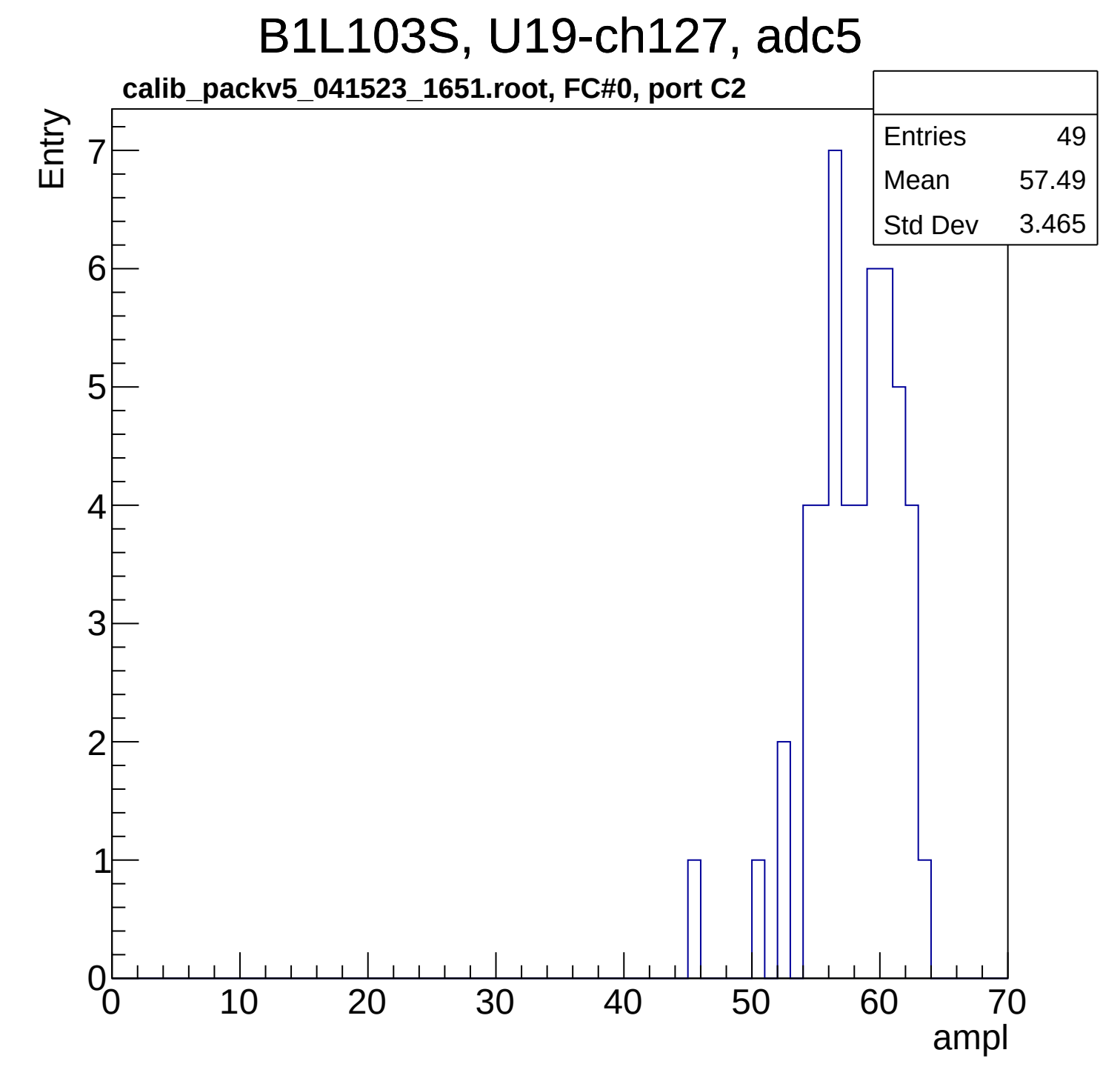
B1L103S, U19-ch127, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 57.49
Std Dev 3.465
Entry
ampl
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7
0
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50
60
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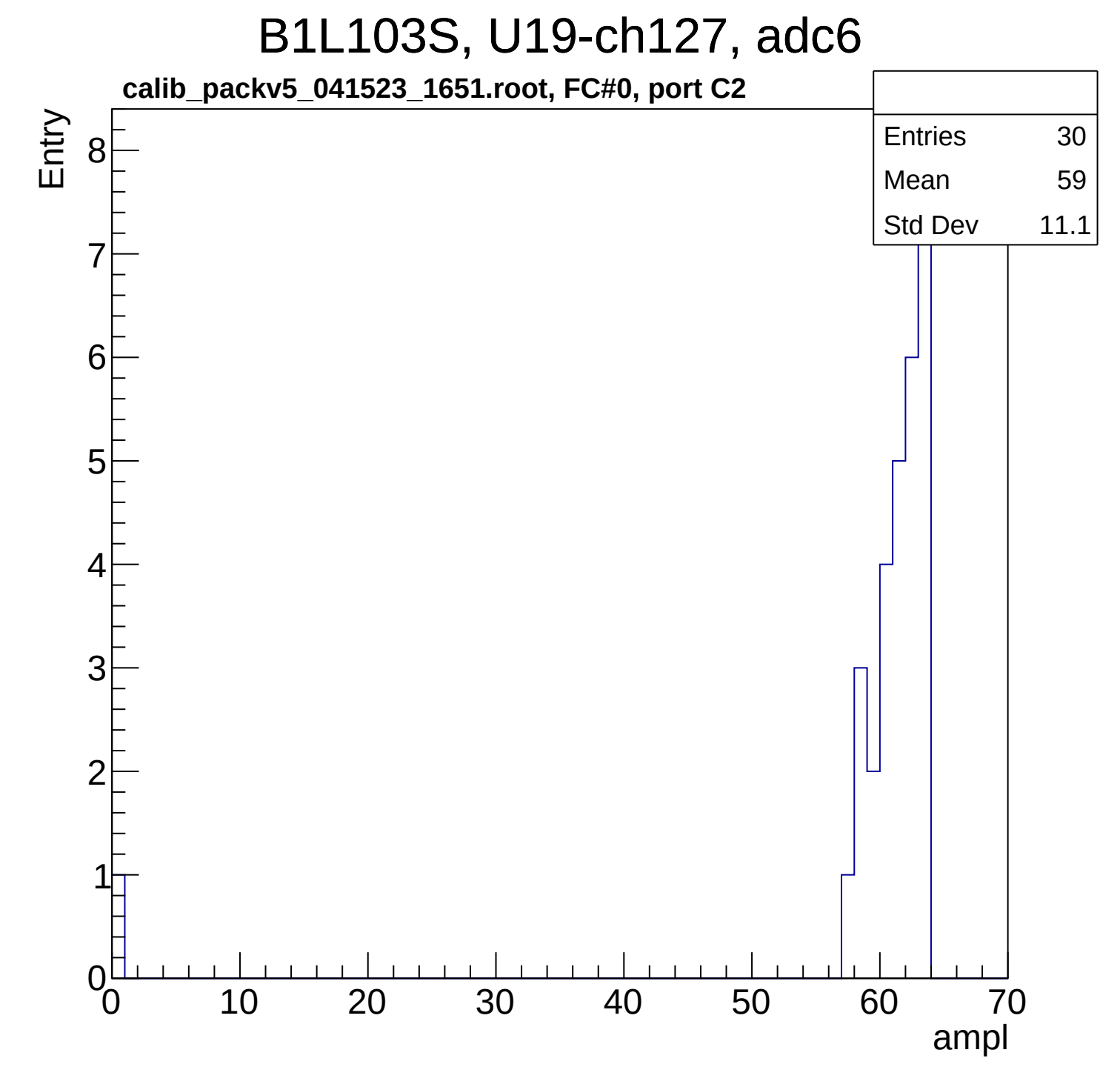
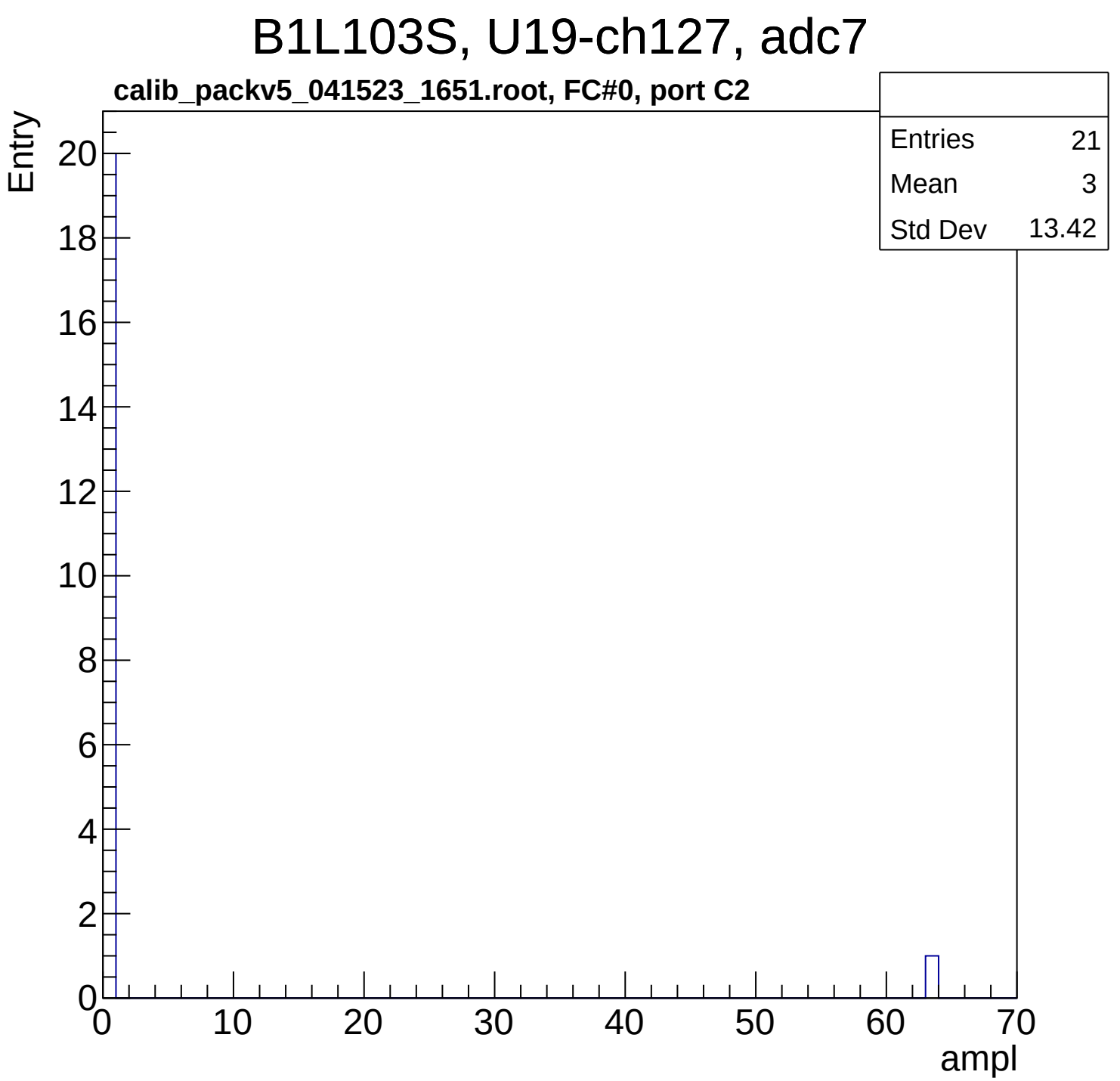

B1L103S, U19-ch127, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 59
Std Dev 11.1
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U19-ch127, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 3
Std Dev 13.42
Entry
0
2
4
6
8
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12
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16
18
20
0
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30
40
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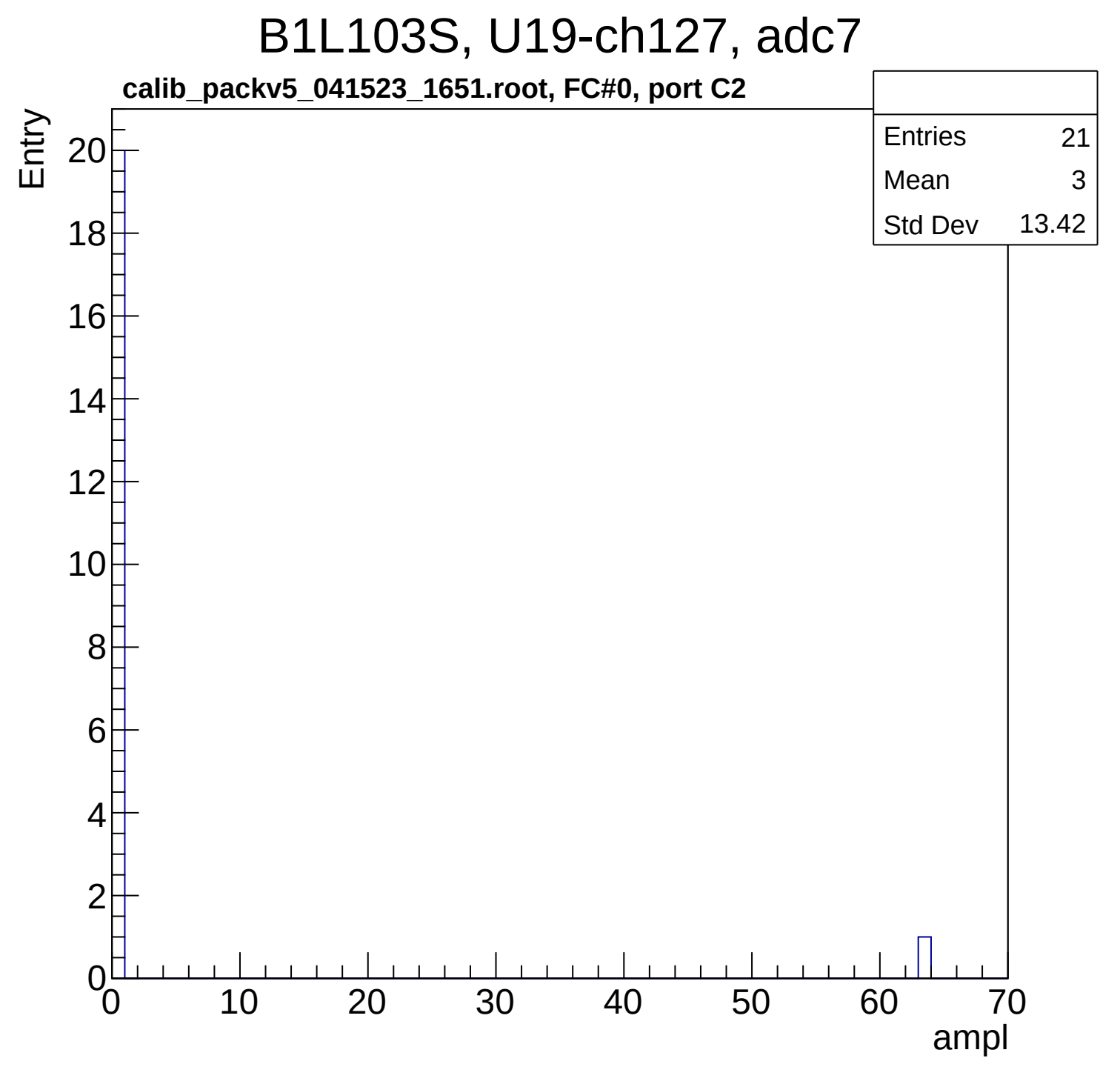
ampl


B1L103S, U19-ch127, adc7
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