



# B0L000S, U4-ch0

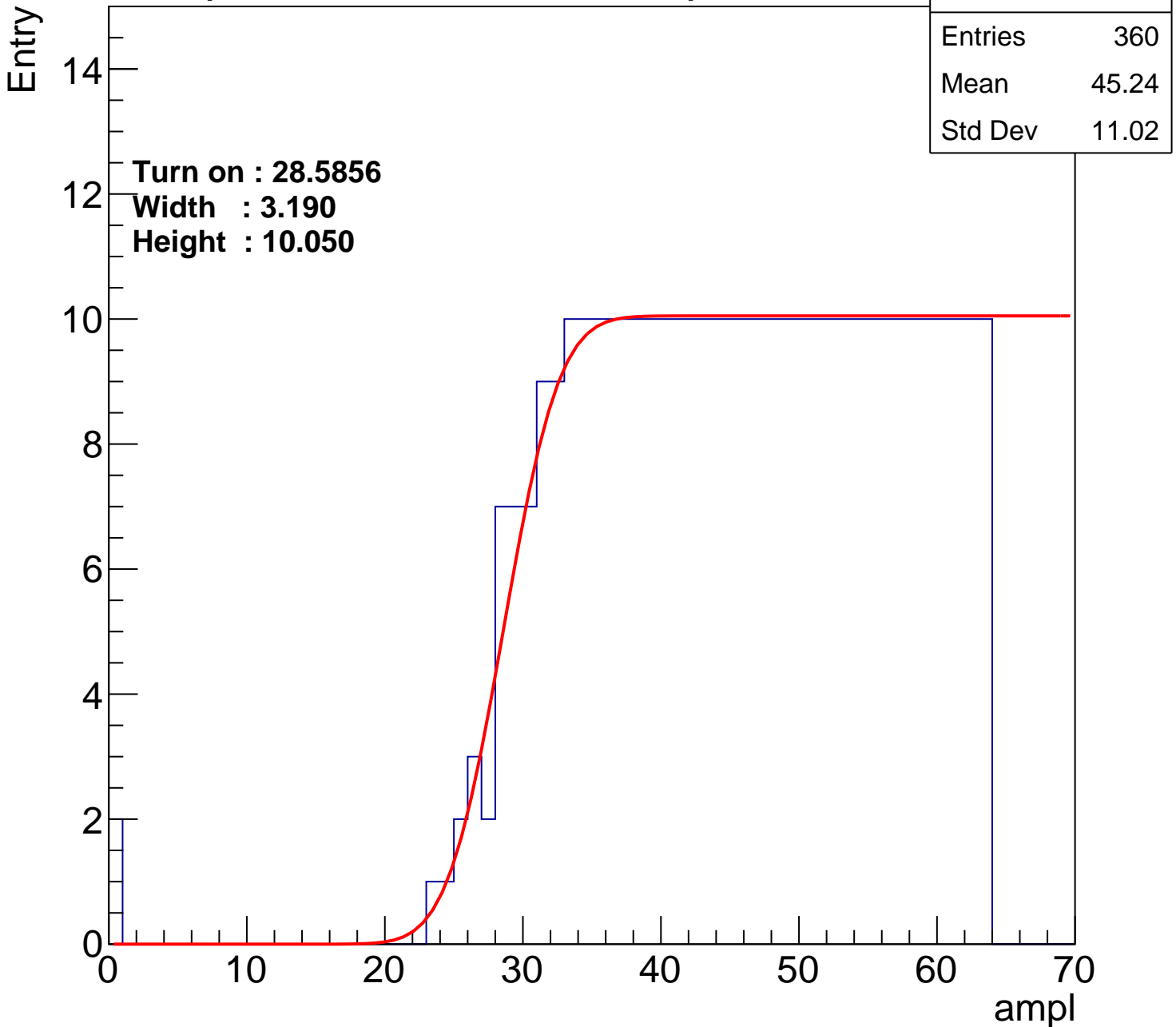
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	360
Mean	45.24
Std Dev	11.02

Turn on : 28.5856

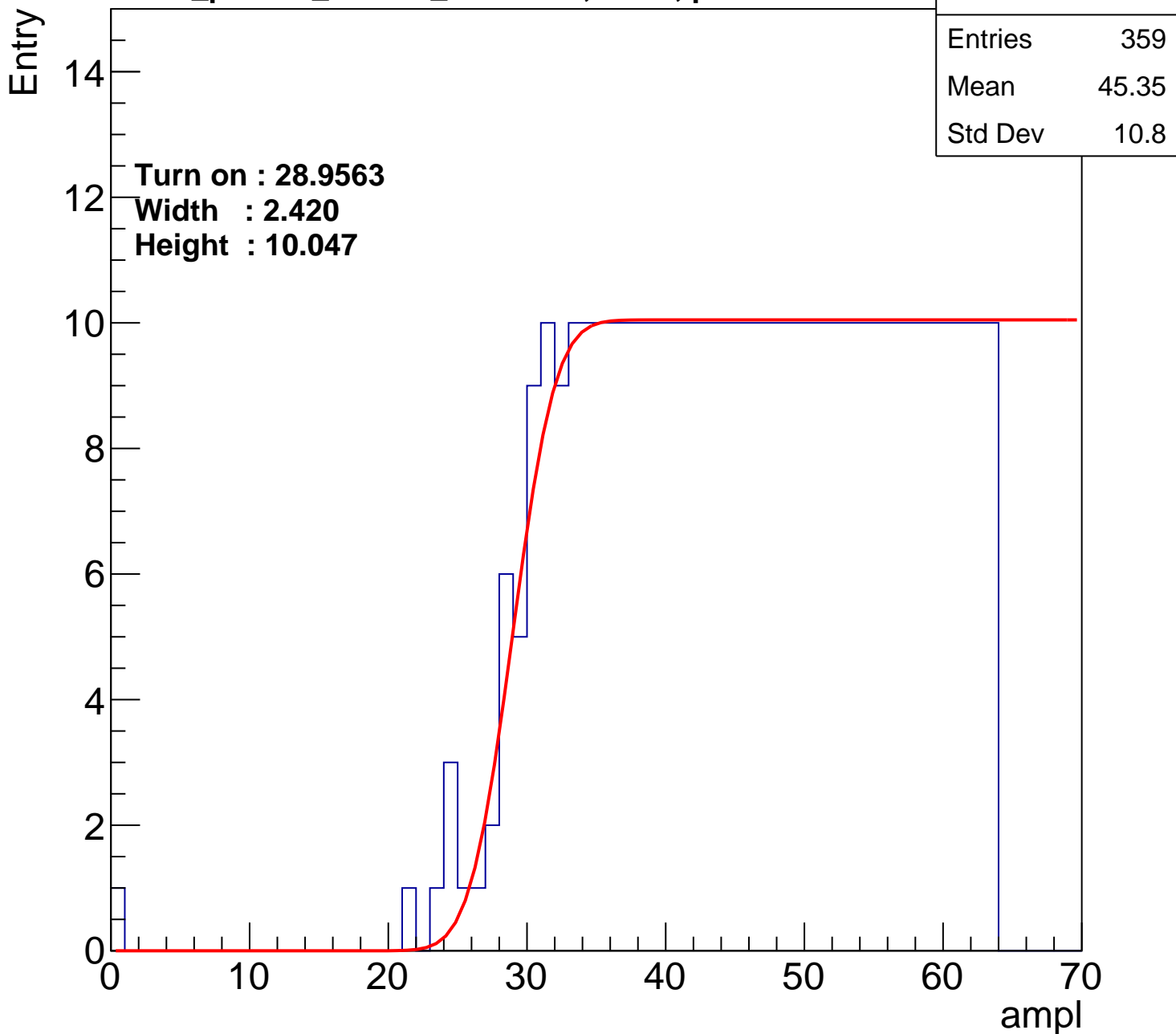
Width : 3.190

Height : 10.050



**calib\_packv5\_042523\_0143.root, FC#5, port B1**

Turn on : 28.9563  
Width : 2.420  
Height : 10.047



# B0L000S, U4-ch2

calib\_packv5\_042523\_0143.root, FC#5, port B1

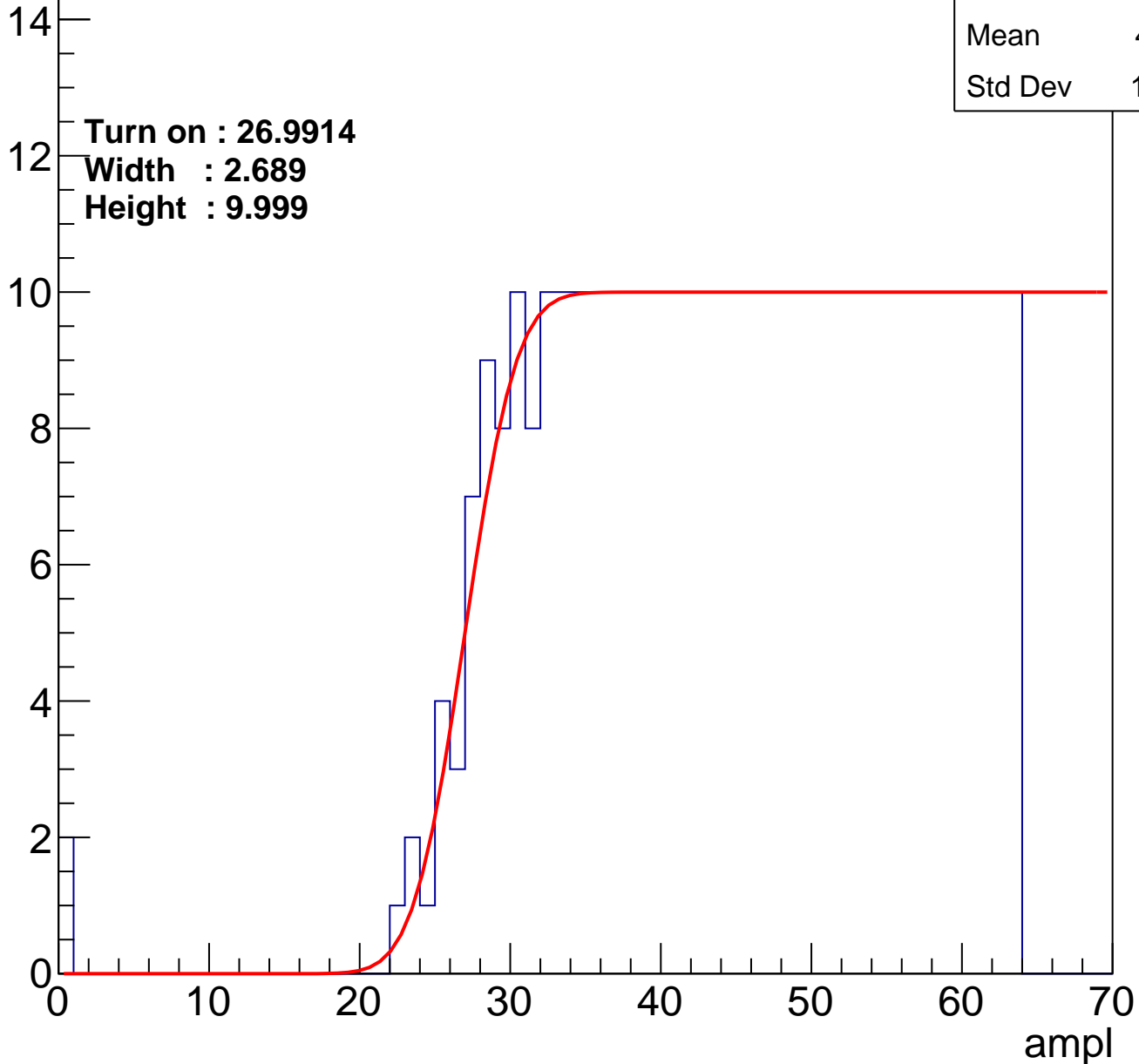
Entries	375
Mean	44.51
Std Dev	11.38

Turn on : 26.9914

Width : 2.689

Height : 9.999

Entry



# B0L000S, U4-ch3

calib\_packv5\_042523\_0143.root, FC#5, port B1

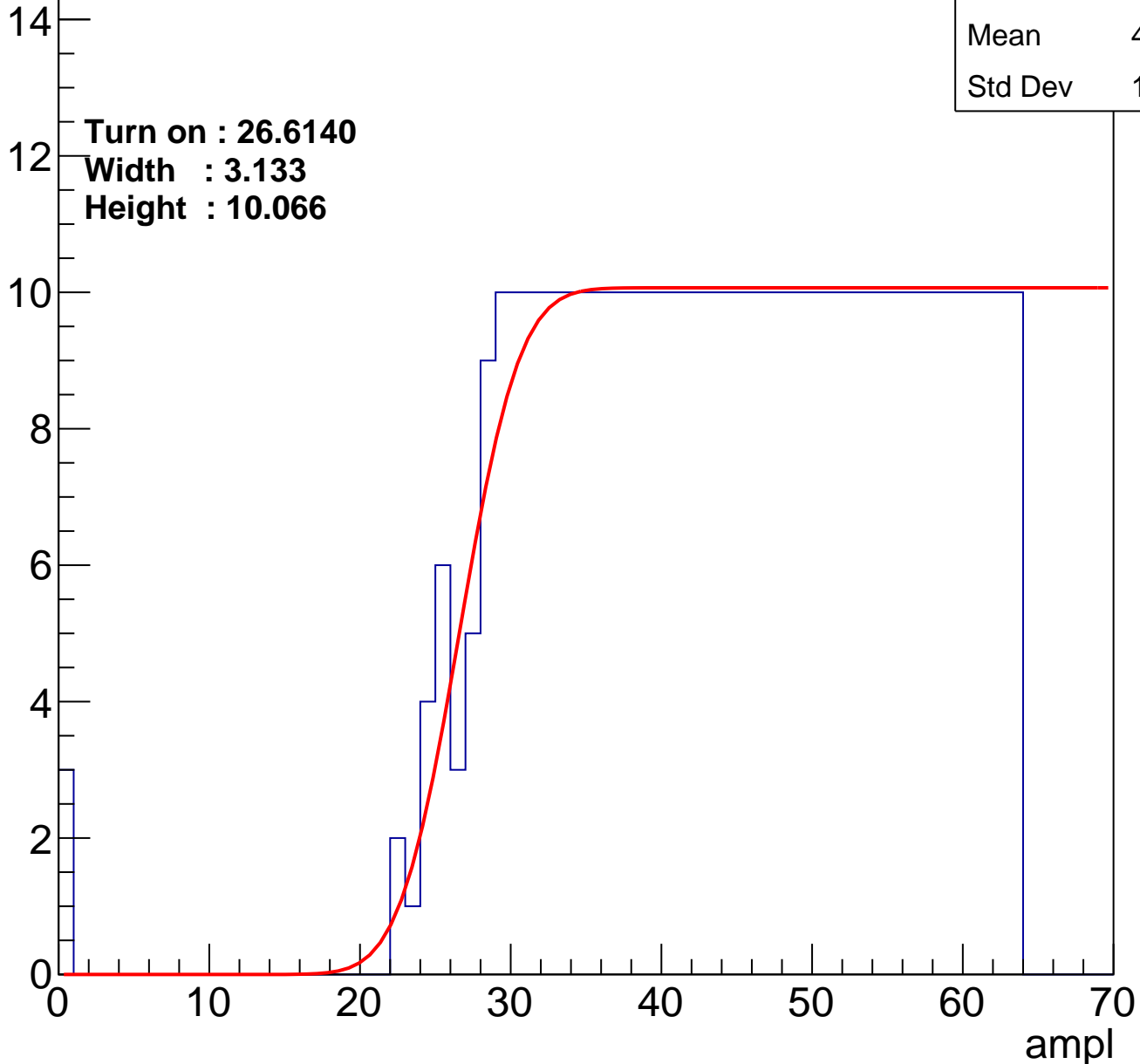
Entries	383
Mean	44.07
Std Dev	11.74

**Turn on : 26.6140**

**Width : 3.133**

**Height : 10.066**

Entry



# B0L000S, U4-ch4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	385
Mean	43.89
Std Dev	11.98

Turn on : 26.5117

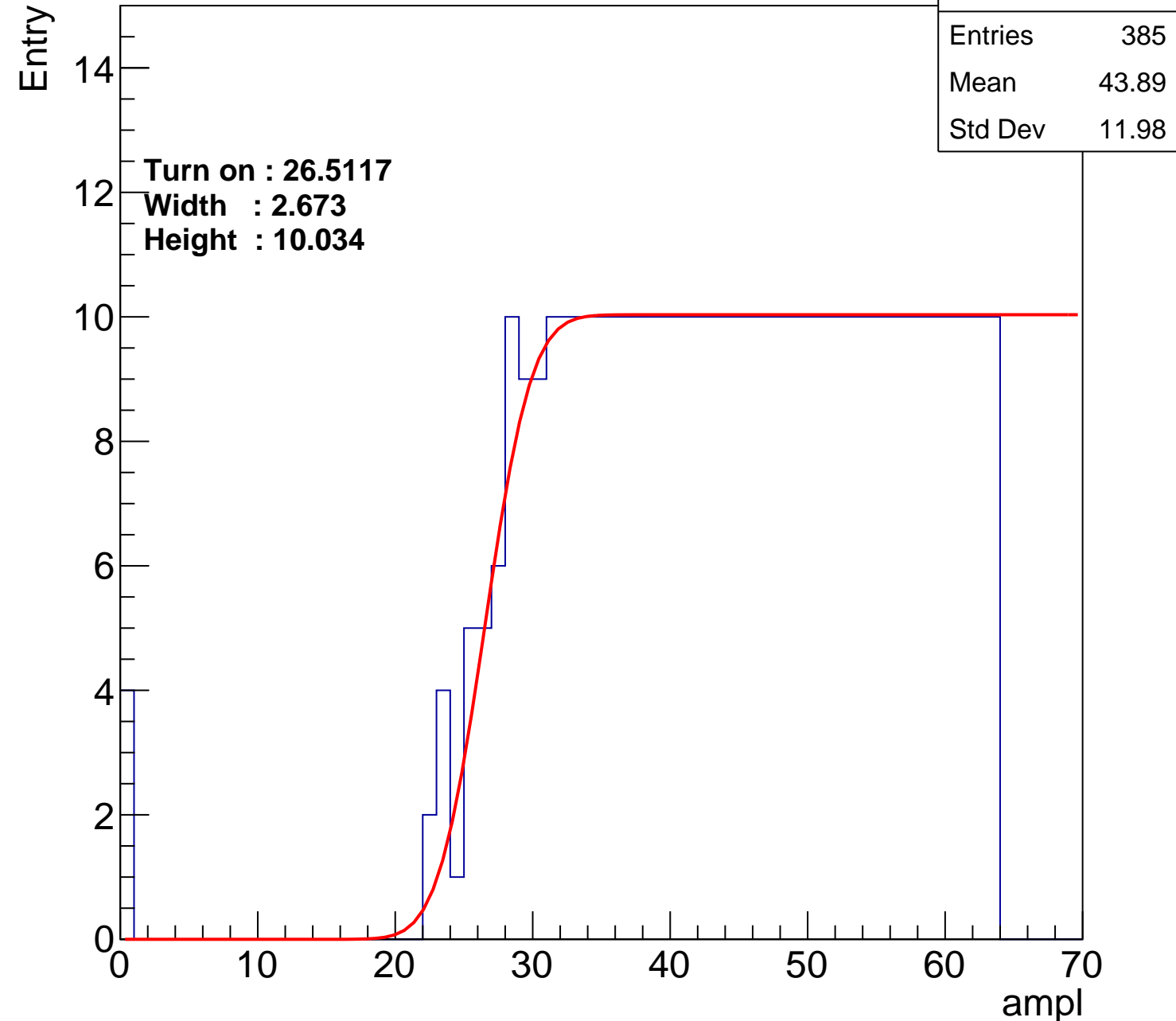
Width : 2.673

Height : 10.034

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch5

calib\_packv5\_042523\_0143.root, FC#5, port B1

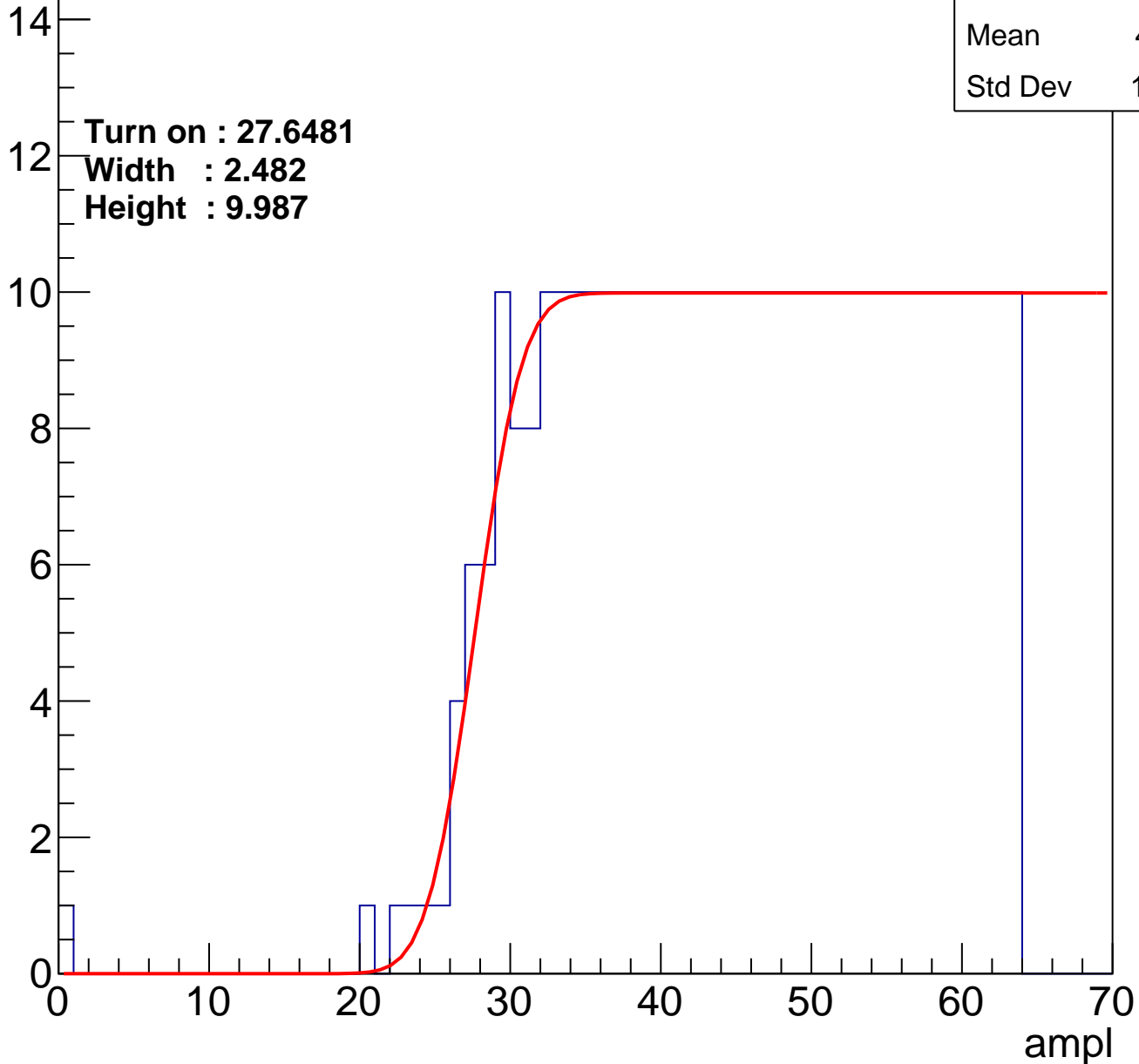
Entries	368
Mean	44.91
Std Dev	11.04

Turn on : 27.6481

Width : 2.482

Height : 9.987

Entry



# B0L000S, U4-ch6

calib\_packv5\_042523\_0143.root, FC#5, port B1

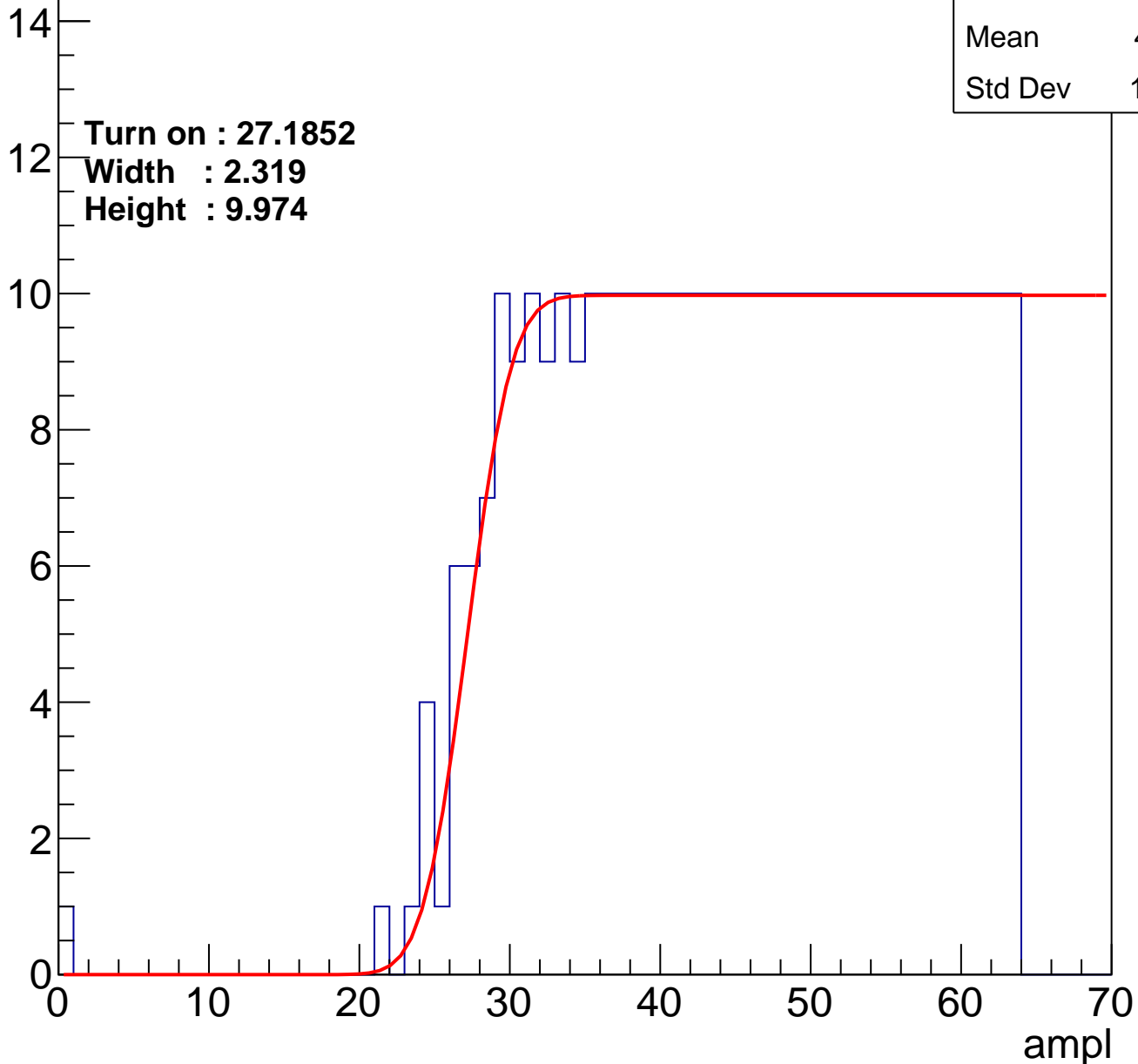
Entries	374
Mean	44.61
Std Dev	11.19

Turn on : 27.1852

Width : 2.319

Height : 9.974

Entry





# B0L000S, U4-ch7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	384
Mean	44.09
Std Dev	11.57

Turn on : 25.4252

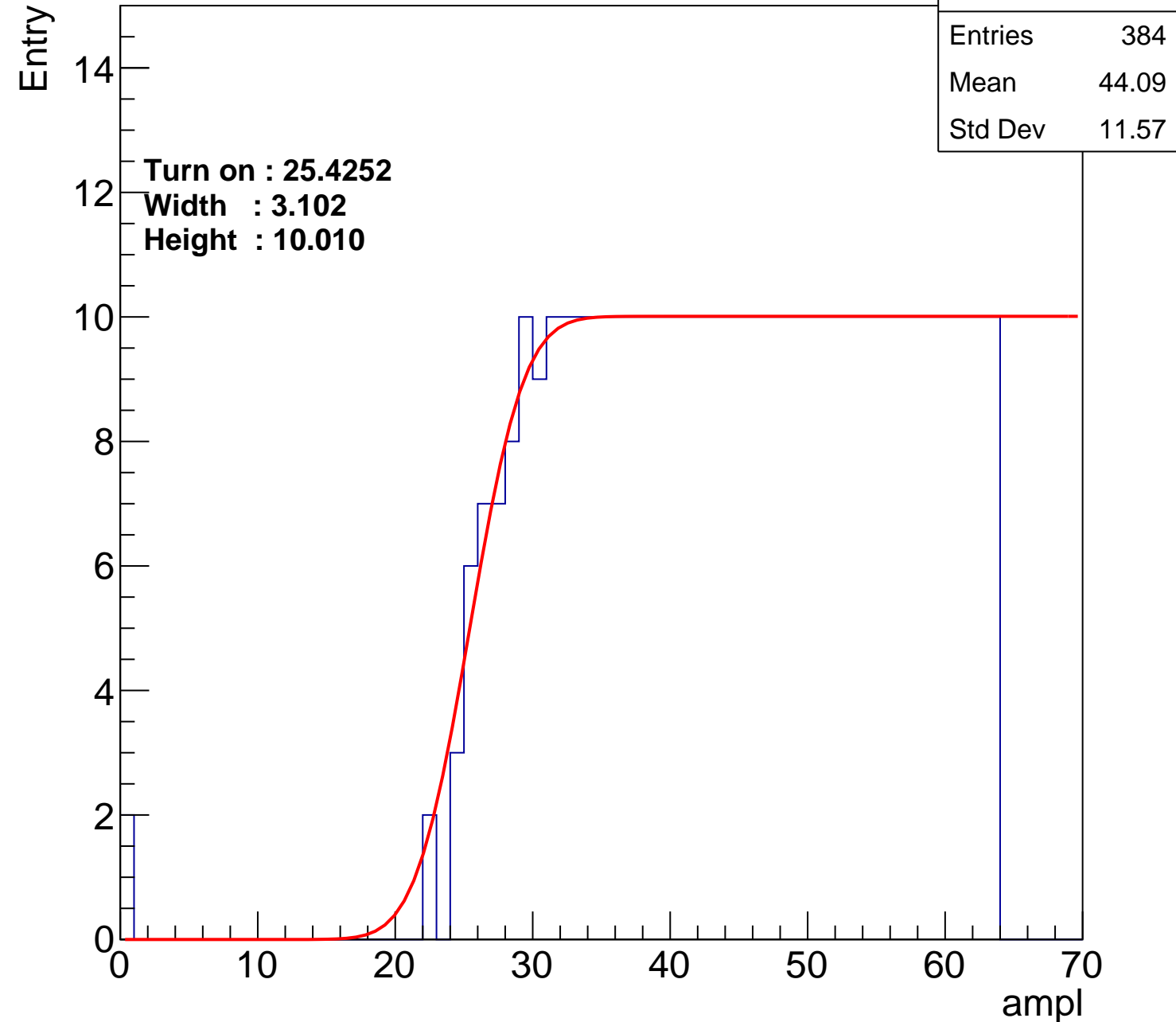
Width : 3.102

Height : 10.010

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch8

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	364
Mean	45.15
Std Dev	10.86

Turn on : 28.2065

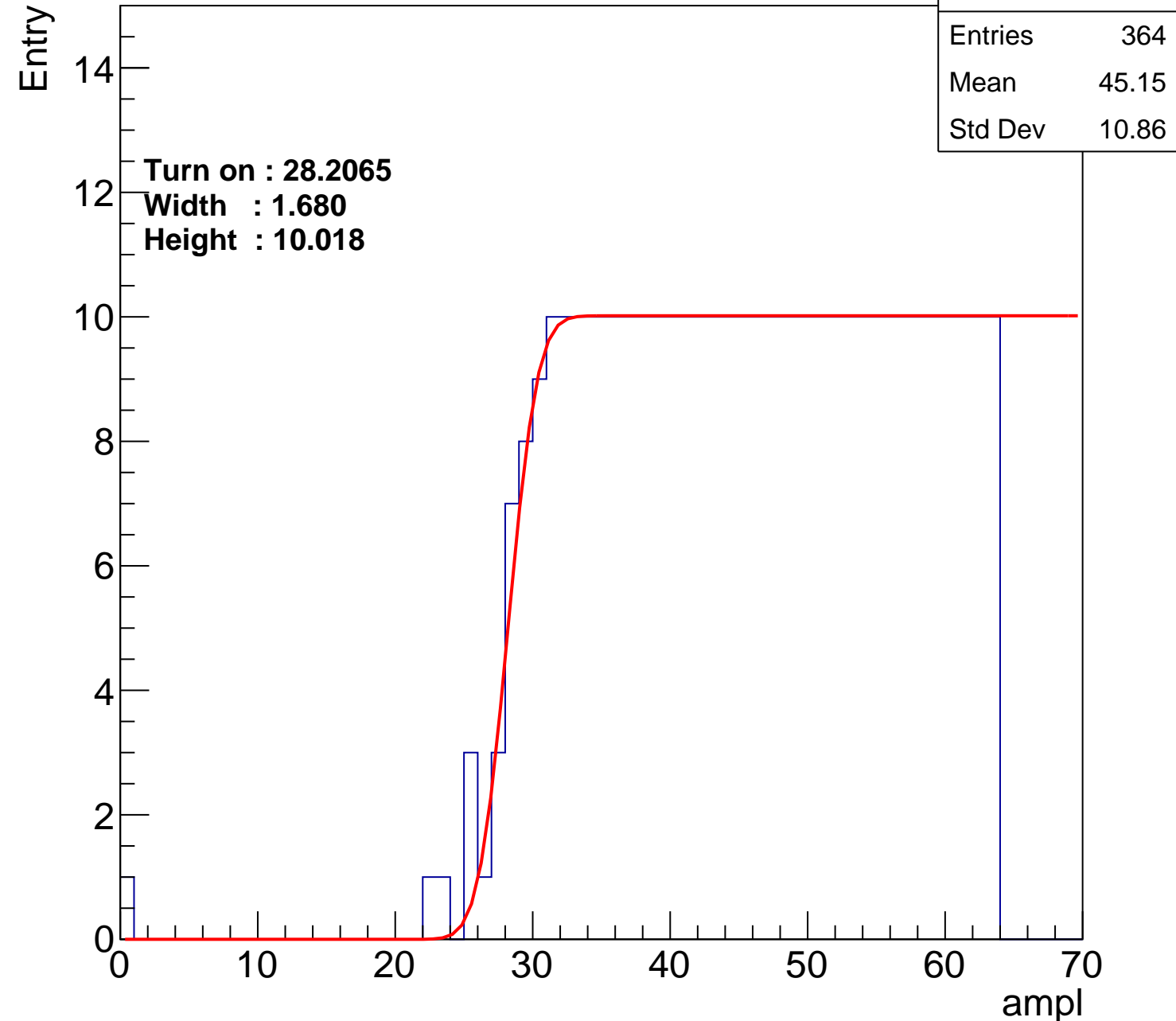
Width : 1.680

Height : 10.018

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch9

calib\_packv5\_042523\_0143.root, FC#5, port B1

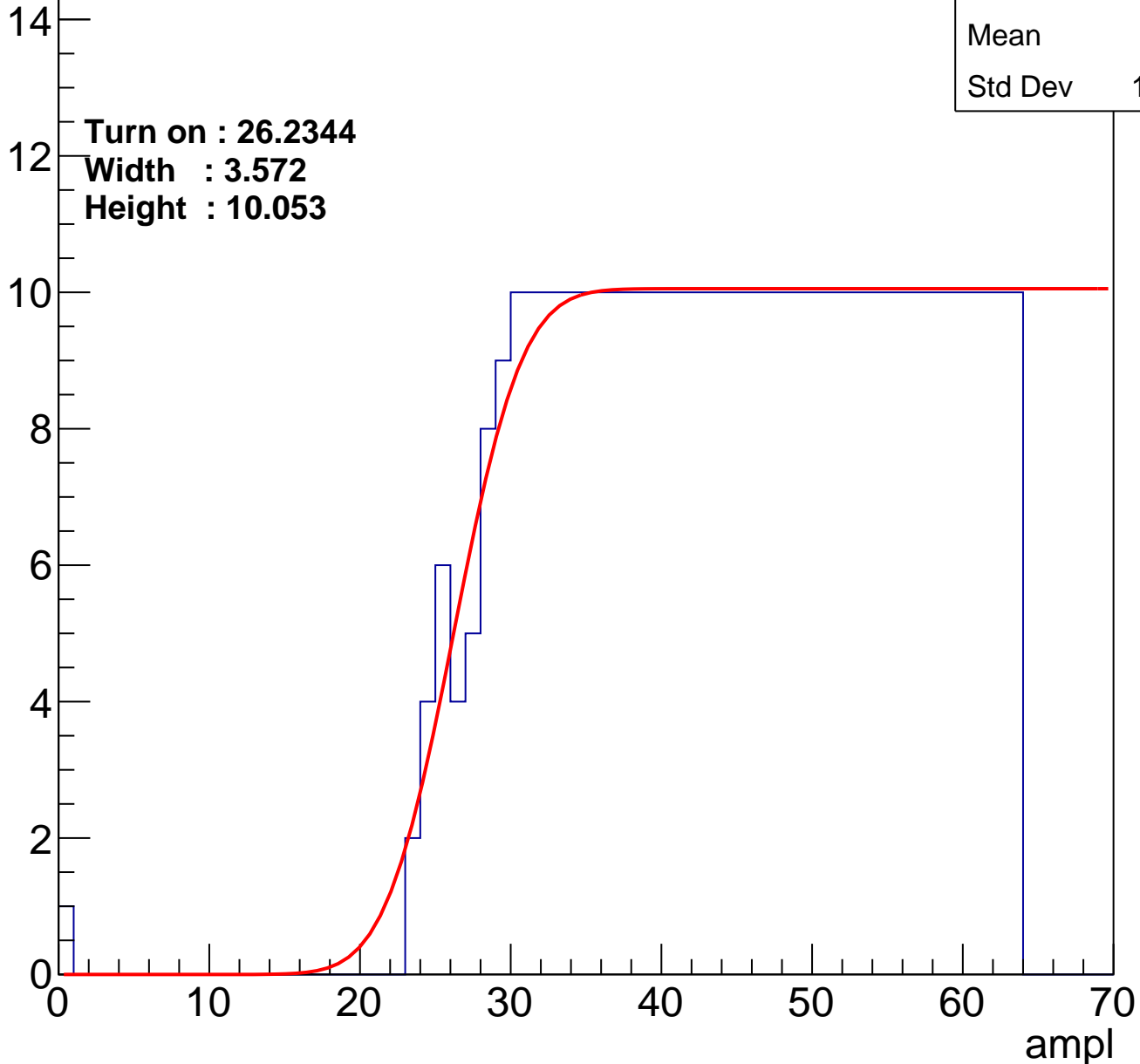
Entries	379
Mean	44.4
Std Dev	11.28

Turn on : 26.2344

Width : 3.572

Height : 10.053

Entry



# B0L000S, U4-ch10

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	380
Mean	44.25
Std Dev	11.54

Turn on : 26.2525

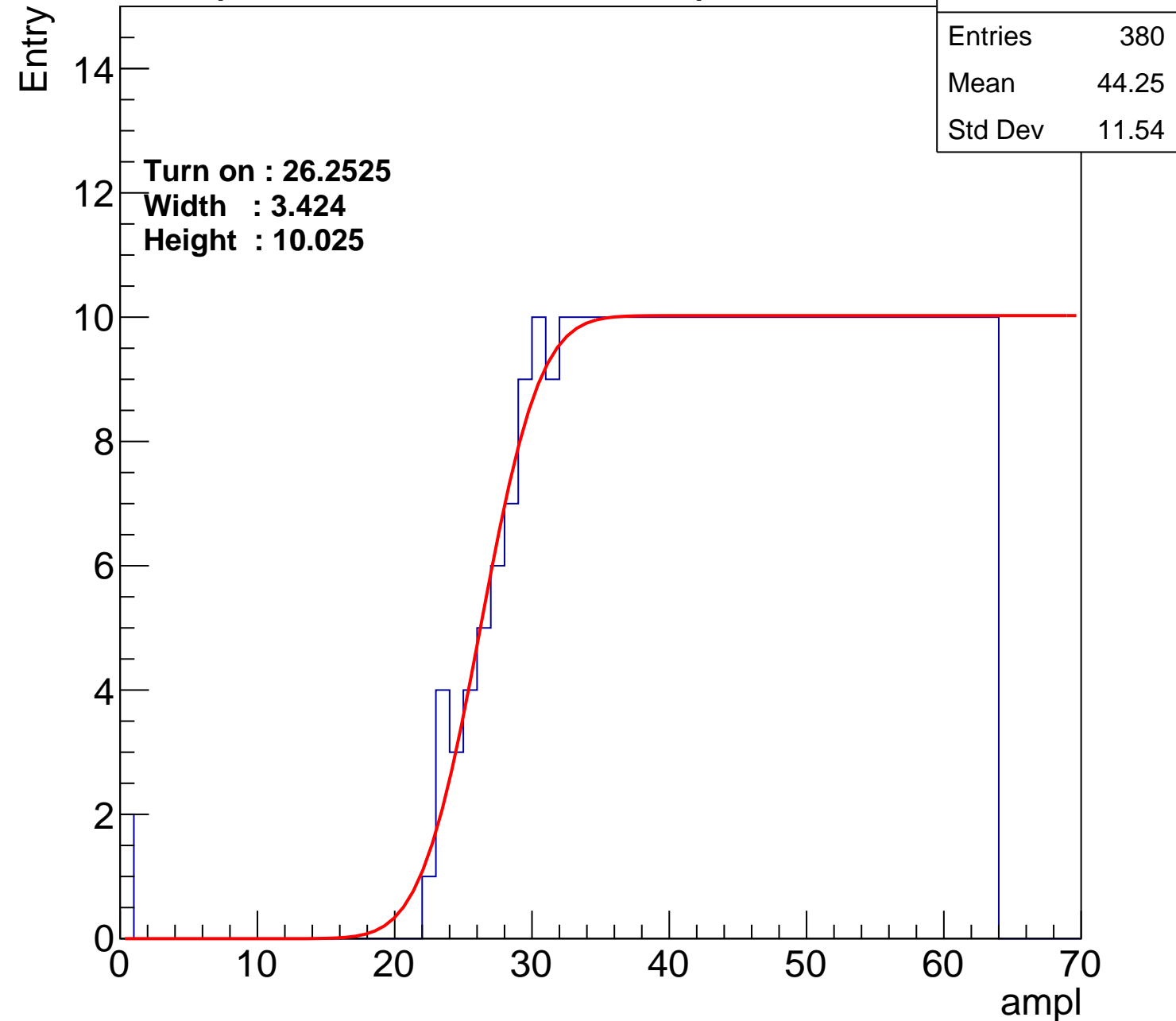
Width : 3.424

Height : 10.025

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch11

calib\_packv5\_042523\_0143.root, FC#5, port B1

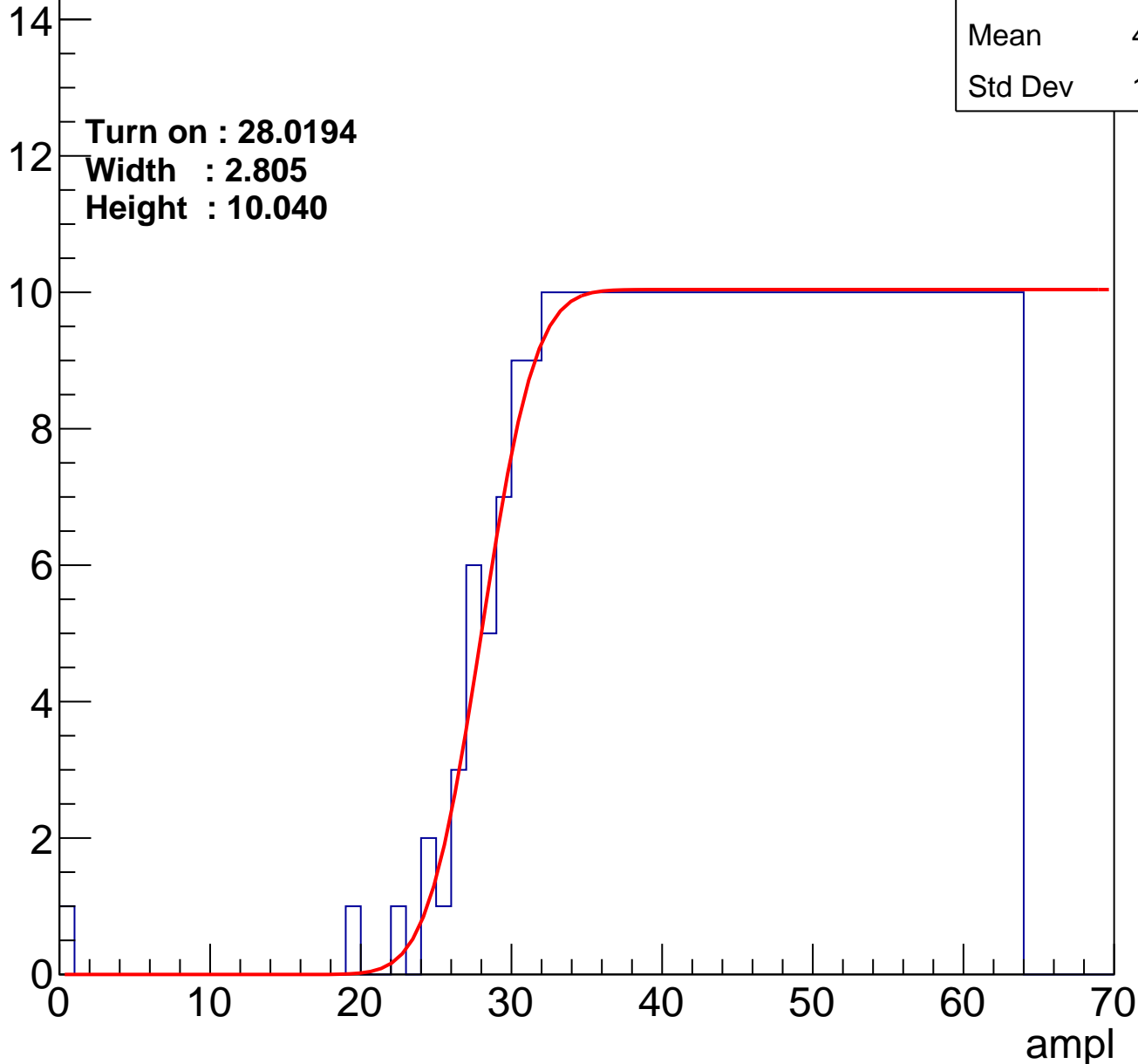
Entries	365
Mean	45.06
Std Dev	10.96

Turn on : 28.0194

Width : 2.805

Height : 10.040

Entry



# B0L000S, U4-ch12

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	380
Mean	44.16
Std Dev	11.83

**Turn on : 26.3863**

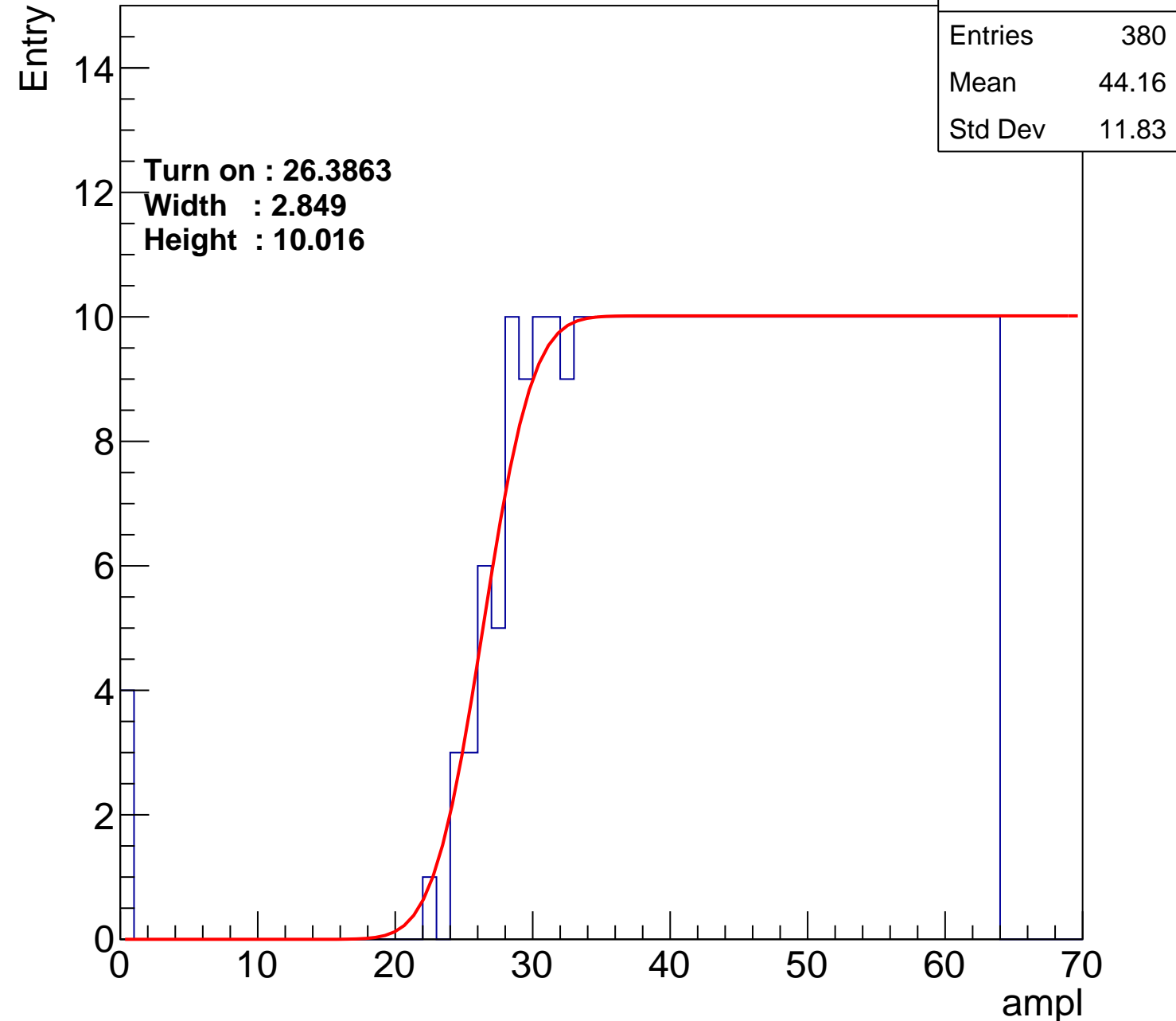
**Width : 2.849**

**Height : 10.016**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch13

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	375
Mean	44.55
Std Dev	11.25

Turn on : 27.2256

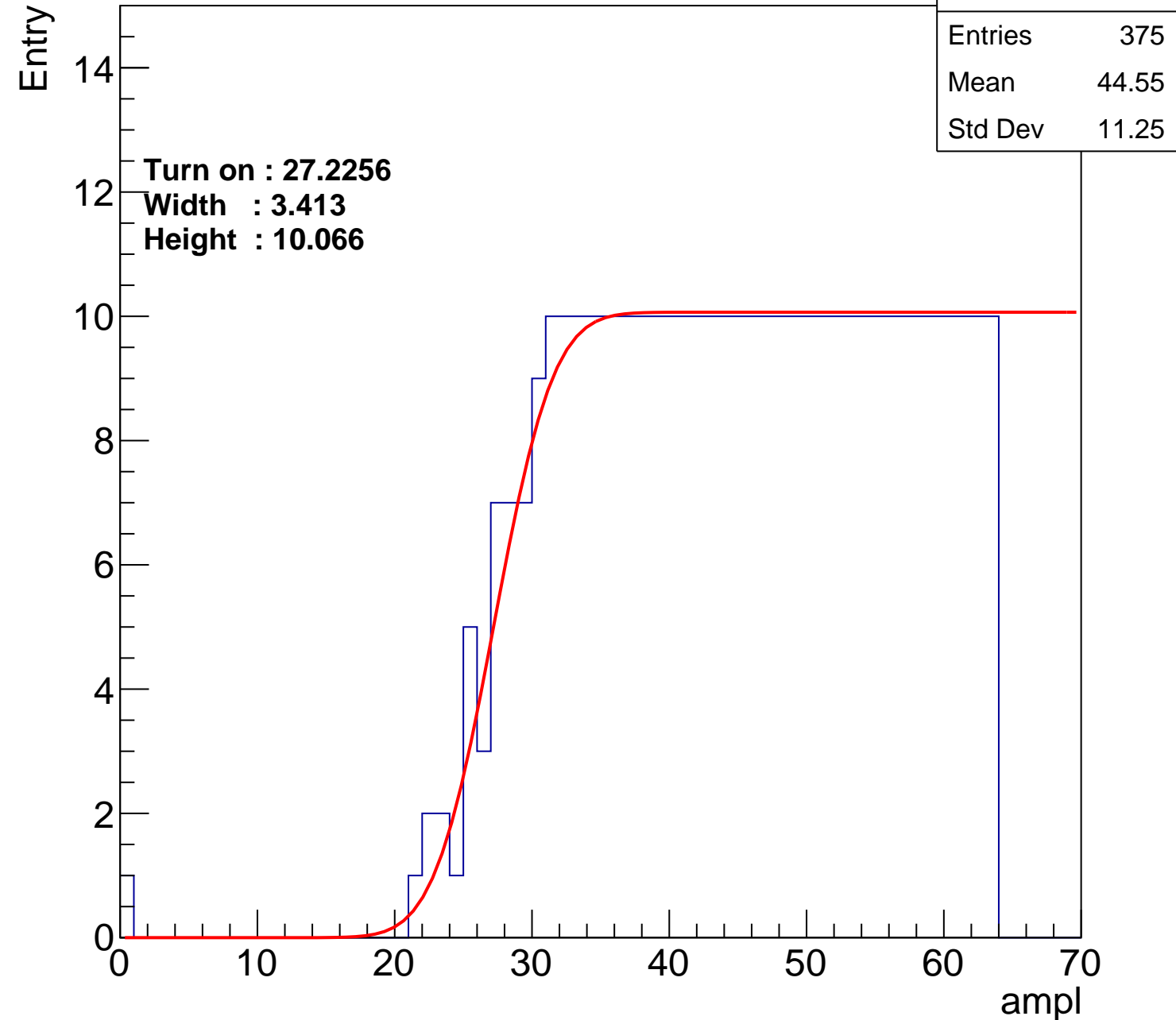
Width : 3.413

Height : 10.066

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch14

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	379
Mean	44.39
Std Dev	11.29

Turn on : 26.7148

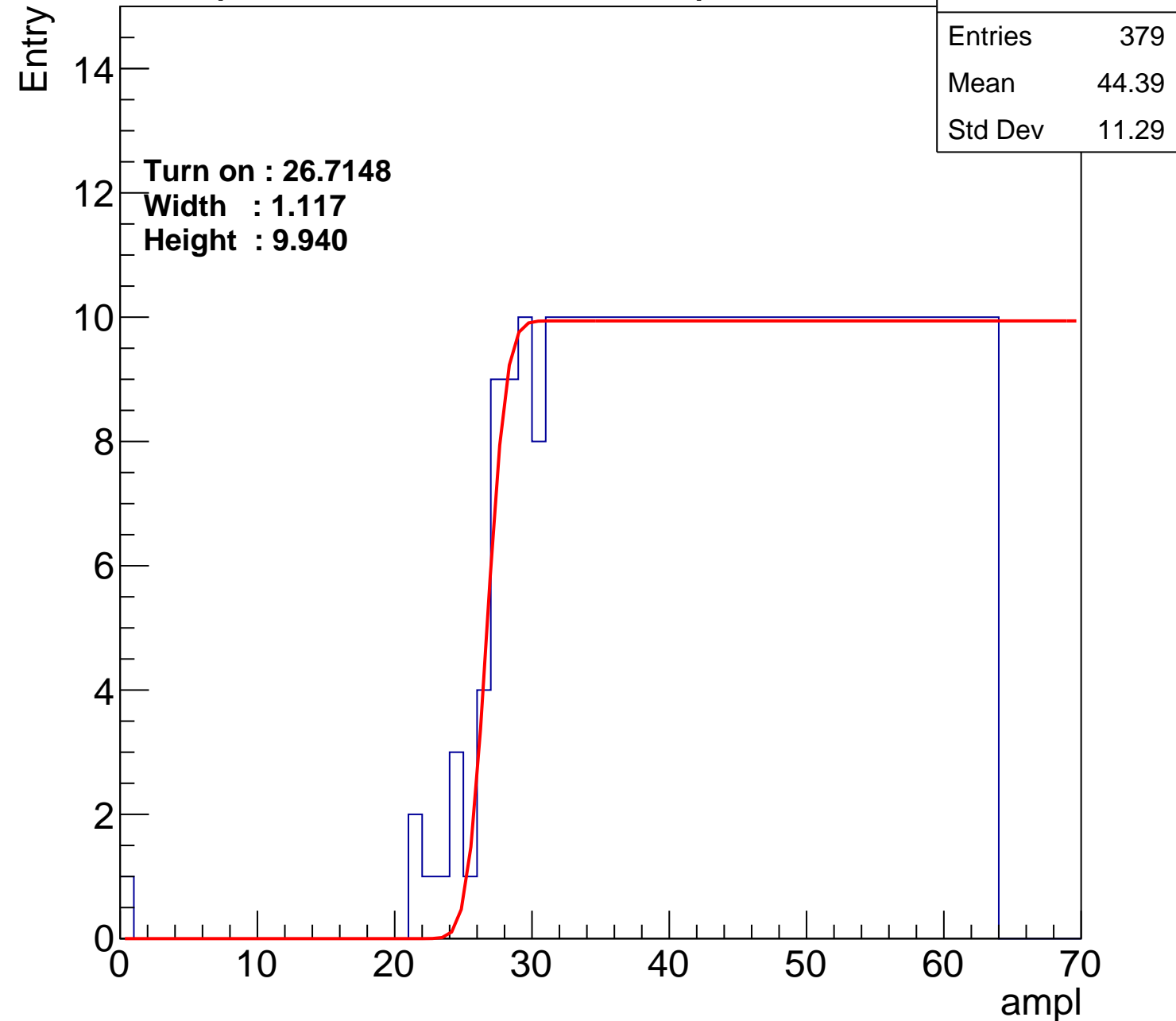
Width : 1.117

Height : 9.940

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L000S, U4-ch15

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	365
Mean	44.91
Std Dev	11.36

Turn on : 27.8194

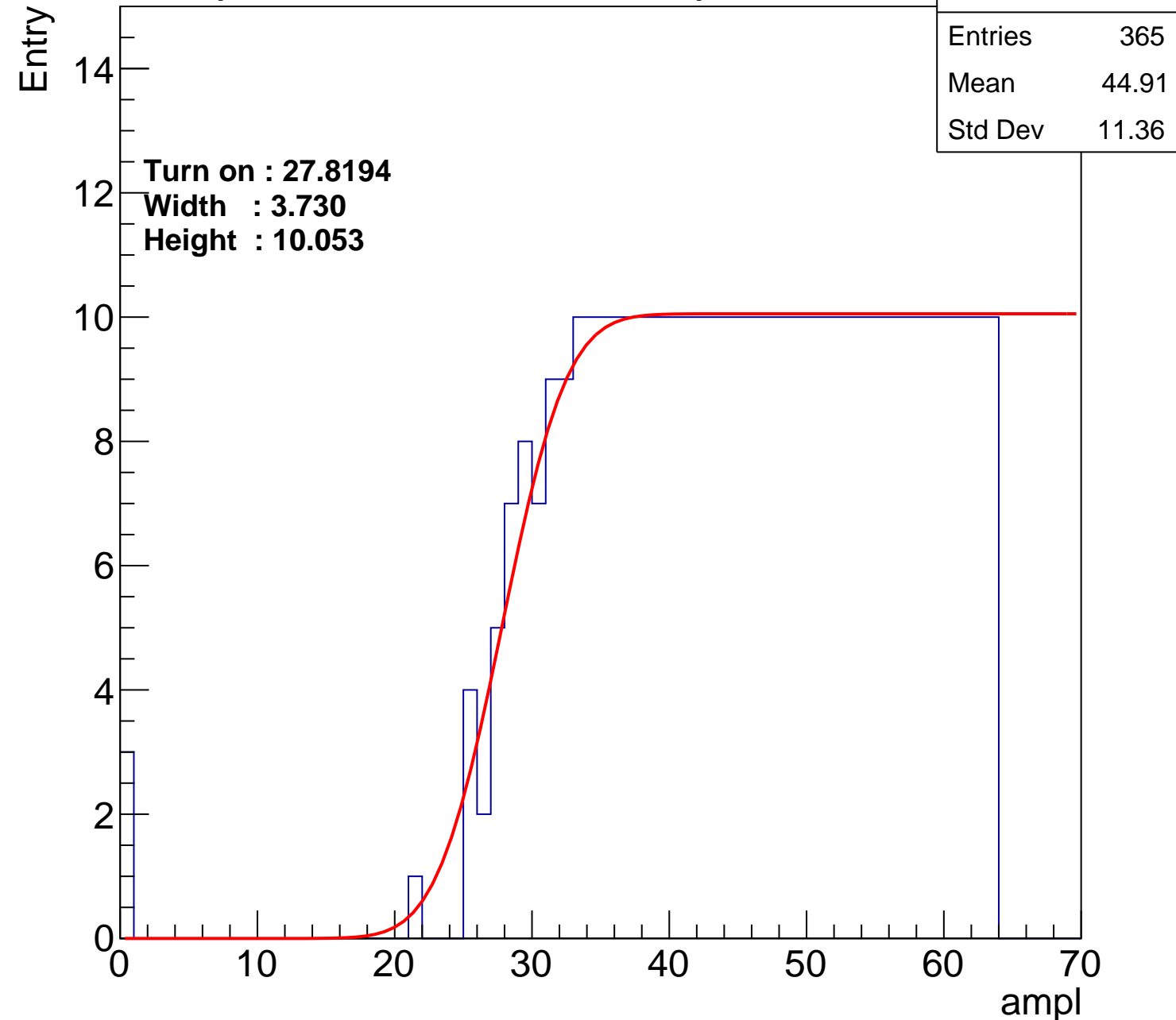
Width : 3.730

Height : 10.053

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch16

calib\_packv5\_042523\_0143.root, FC#5, port B1

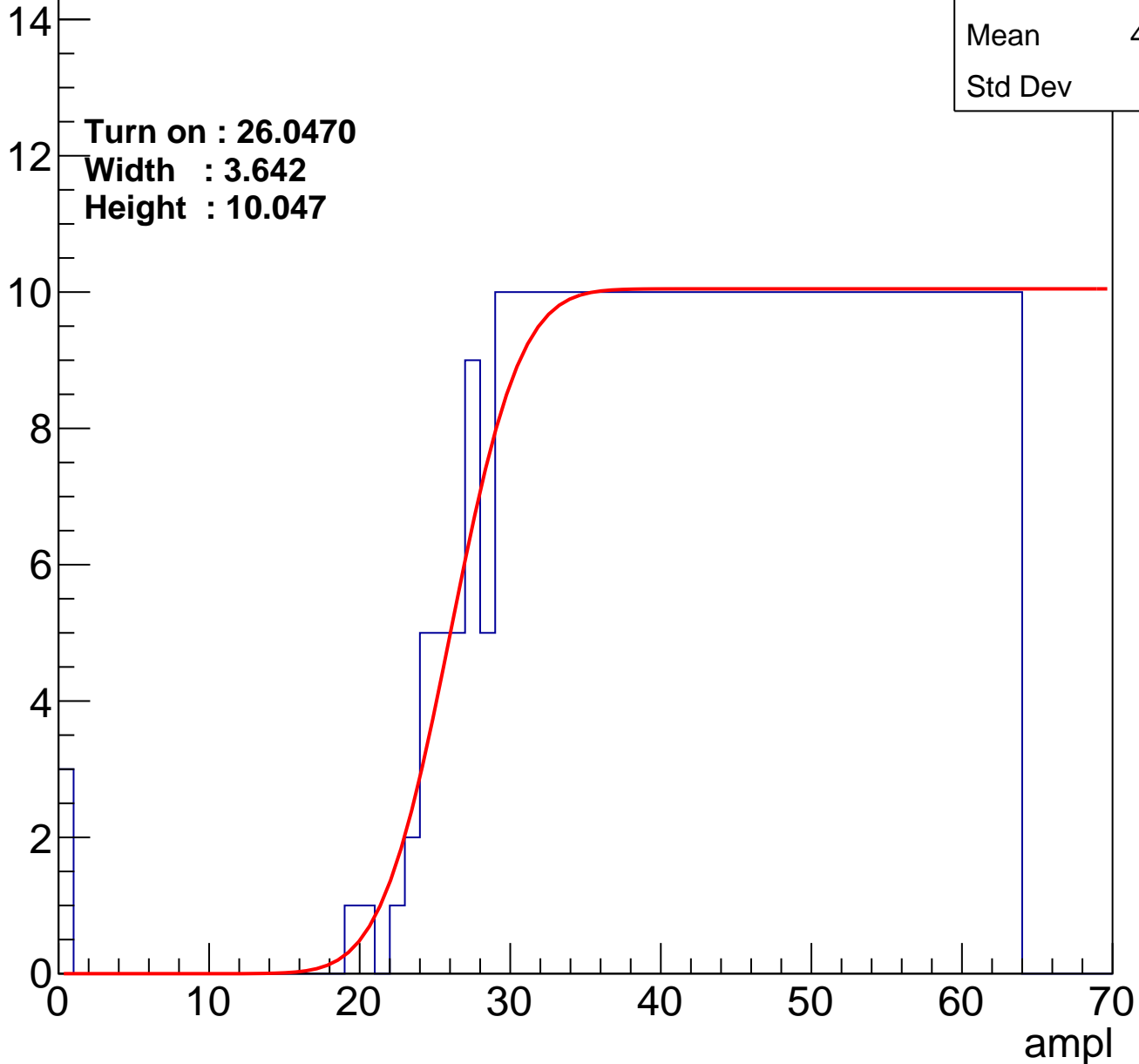
Entries	387
Mean	43.84
Std Dev	11.9

**Turn on : 26.0470**

**Width : 3.642**

**Height : 10.047**

Entry



# B0L000S, U4-ch17

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	367
Mean	44.67
Std Dev	11.79

Turn on : 28.0128

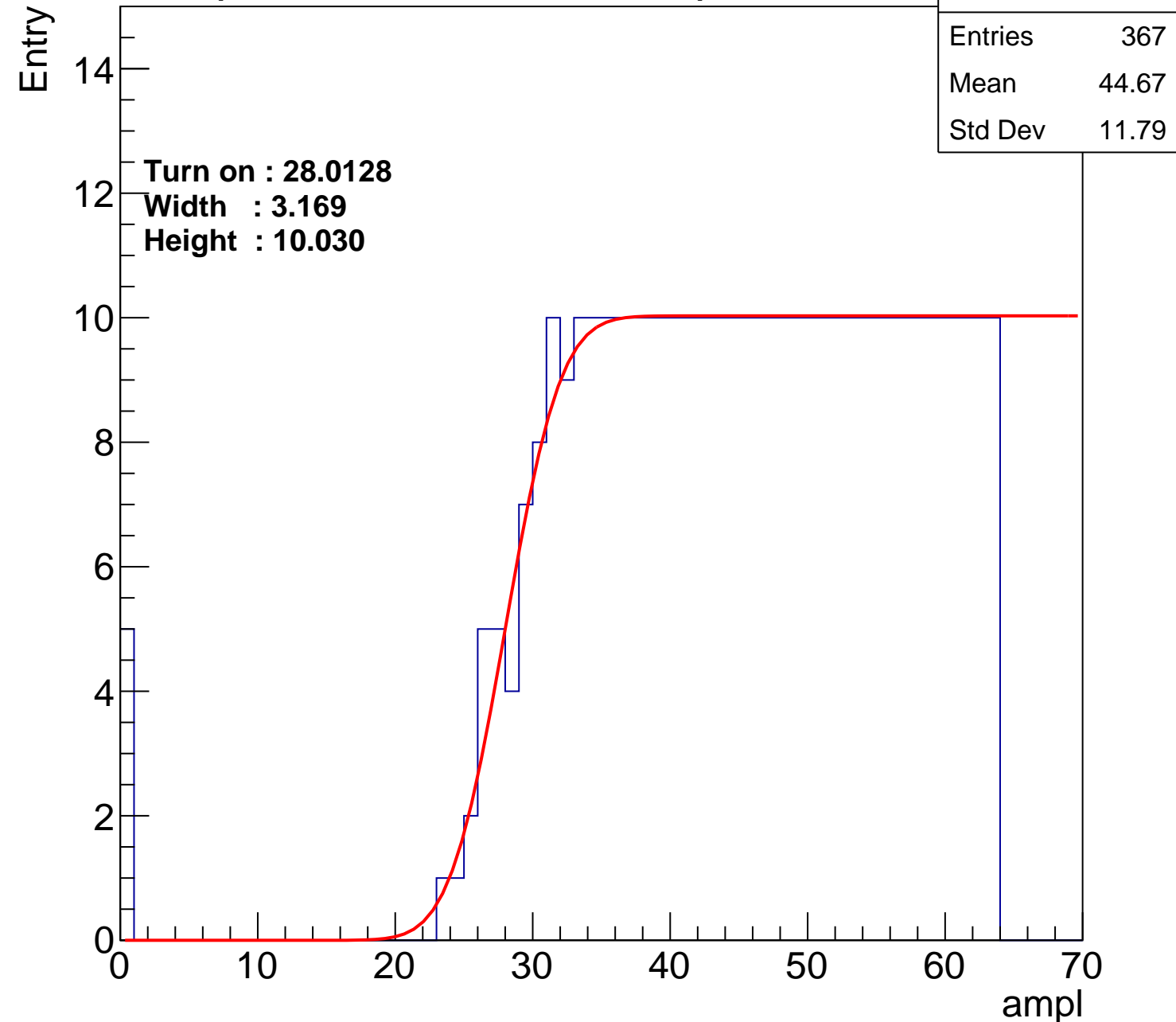
Width : 3.169

Height : 10.030

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch18

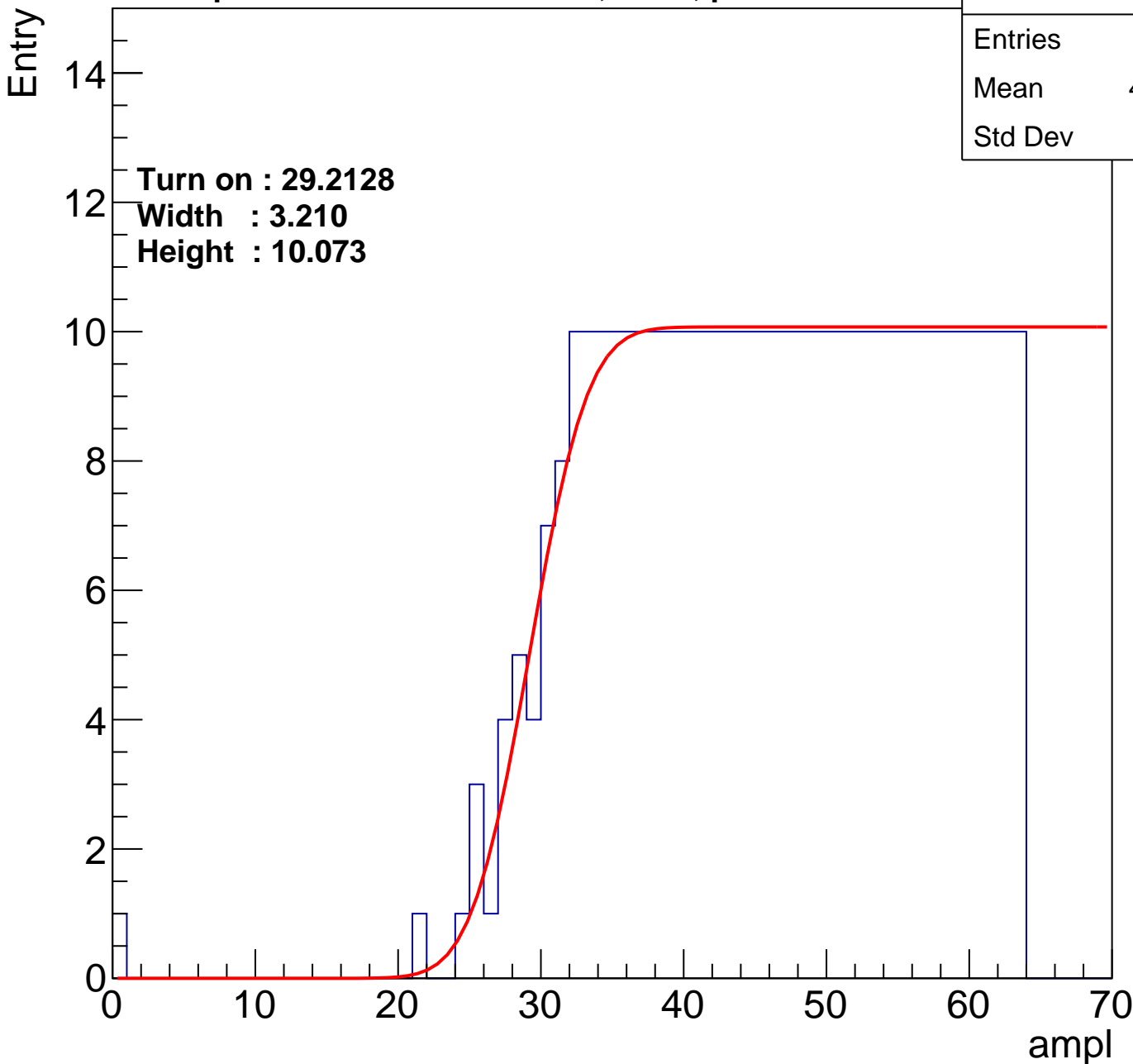
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	355
Mean	45.54
Std Dev	10.71

Turn on : 29.2128

Width : 3.210

Height : 10.073



# B0L000S, U4-ch19

calib\_packv5\_042523\_0143.root, FC#5, port B1

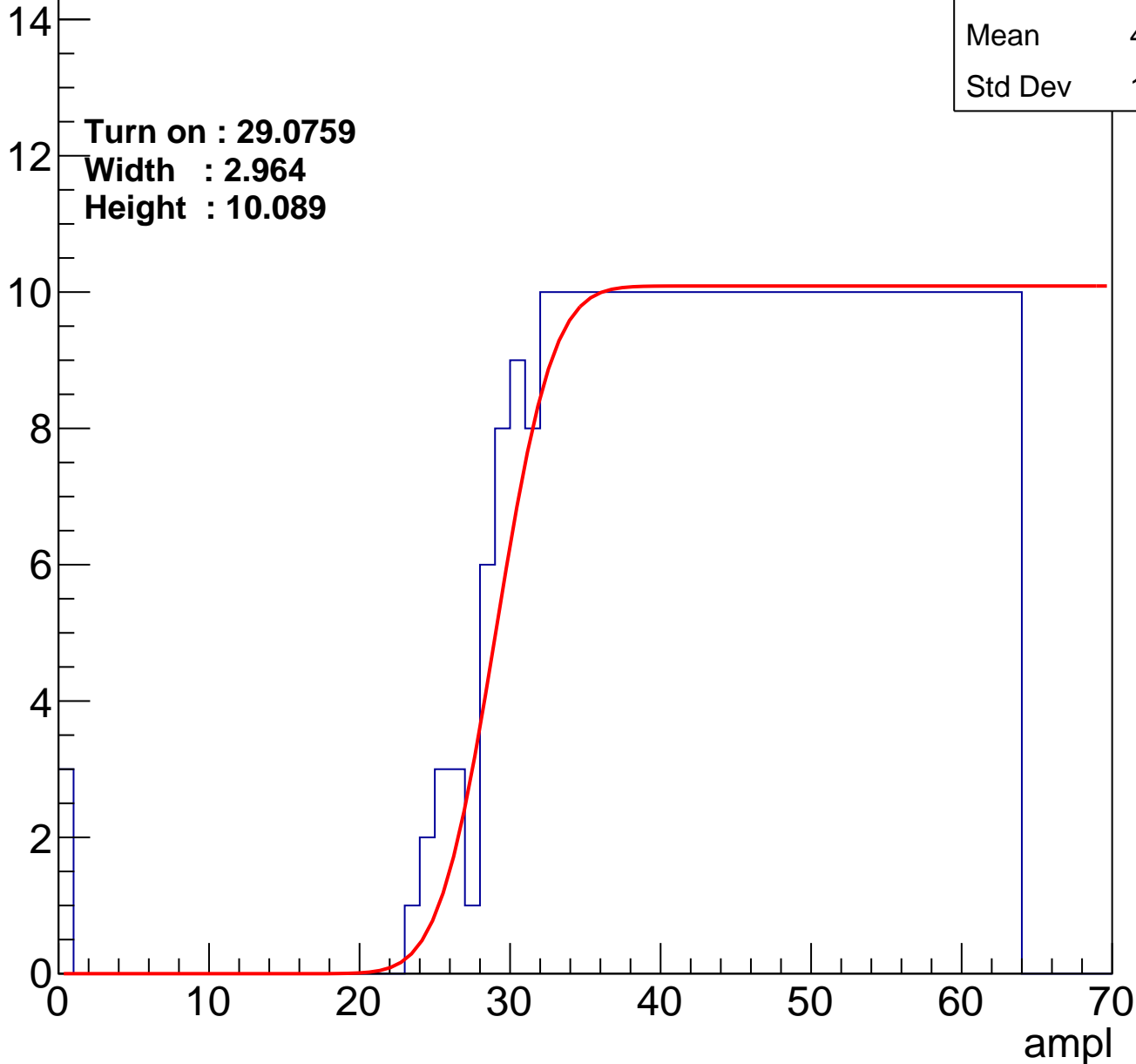
Entry

Entries	364
Mean	44.97
Std Dev	11.33

Turn on : 29.0759

Width : 2.964

Height : 10.089



# B0L000S, U4-ch20

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	369
Mean	44.79
Std Dev	11.24

**Turn on : 27.5737**

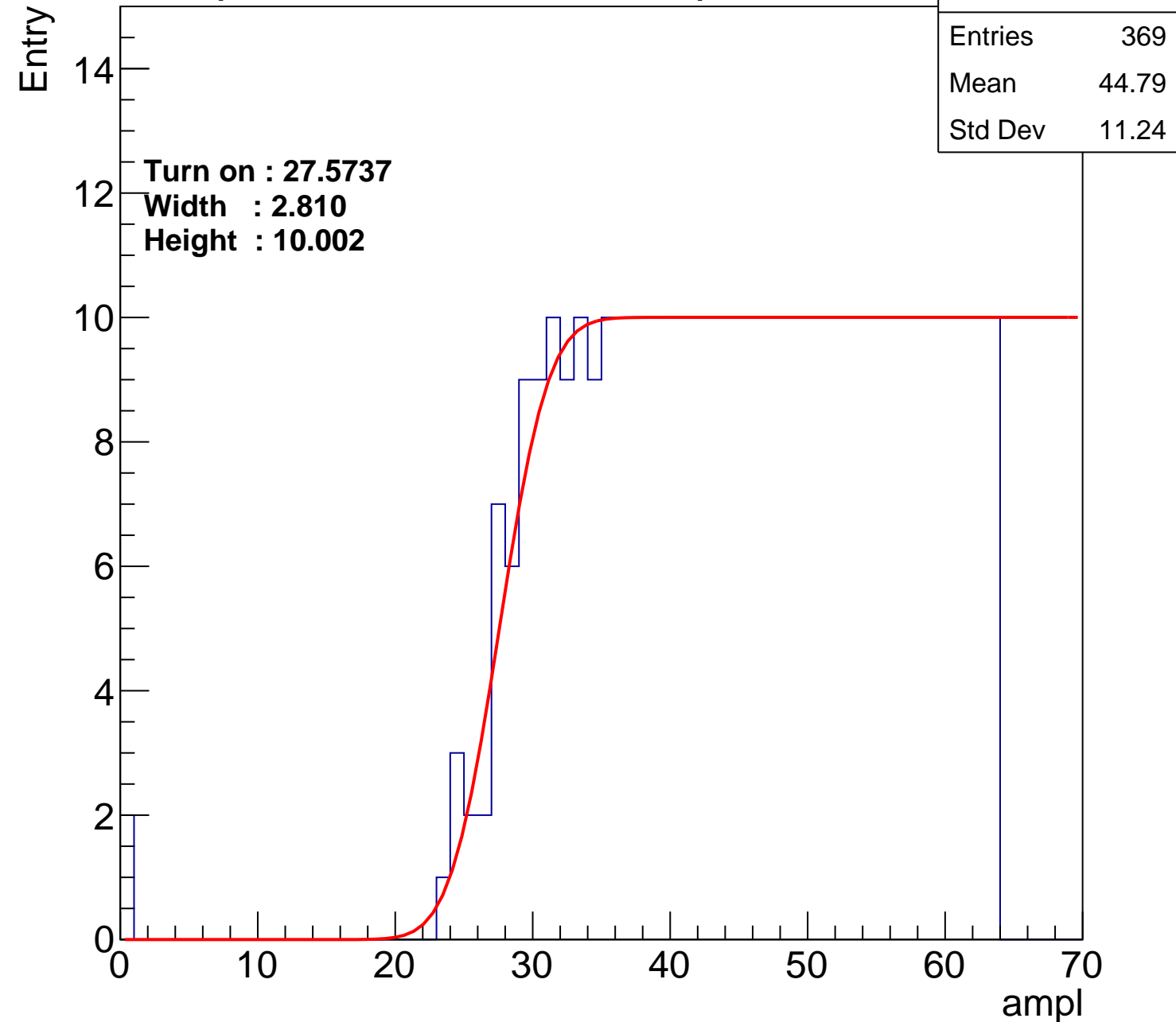
**Width : 2.810**

**Height : 10.002**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch21

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	377
Mean	44.31
Std Dev	11.68

**Turn on : 26.6897**

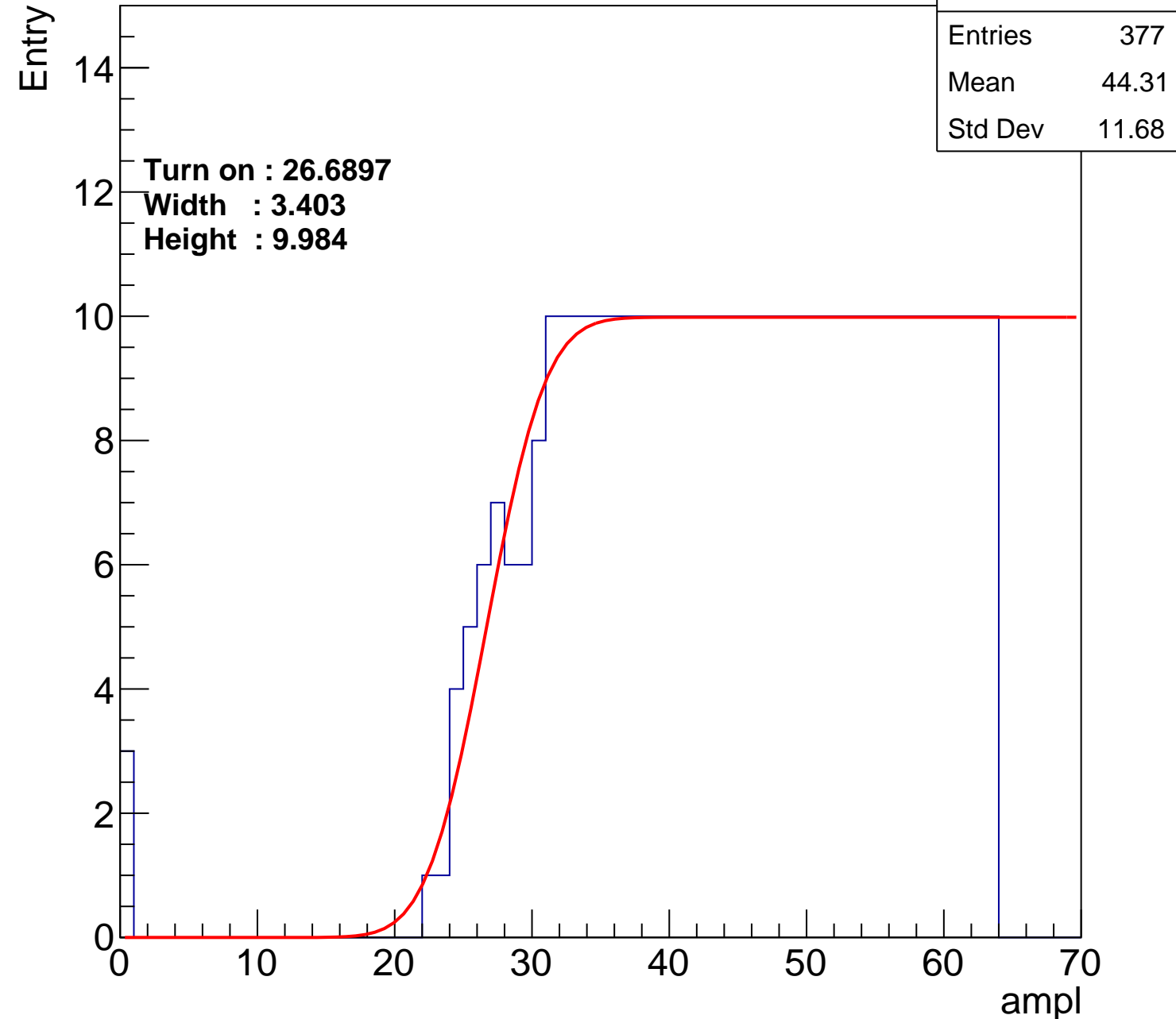
**Width : 3.403**

**Height : 9.984**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch22

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	367
Mean	44.87
Std Dev	11.24

Turn on : 27.5646

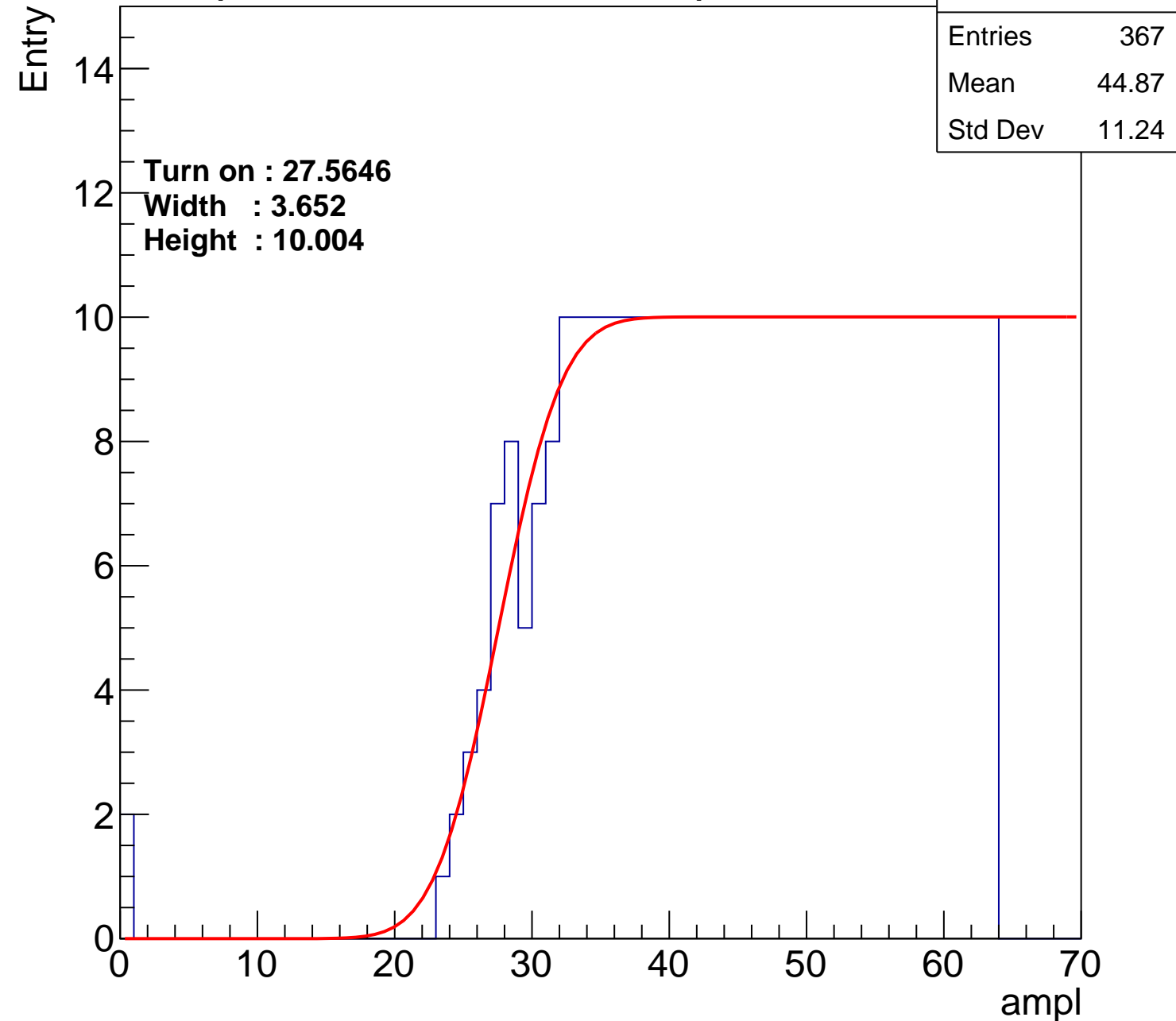
Width : 3.652

Height : 10.004

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L000S, U4-ch23

calib\_packv5\_042523\_0143.root, FC#5, port B1

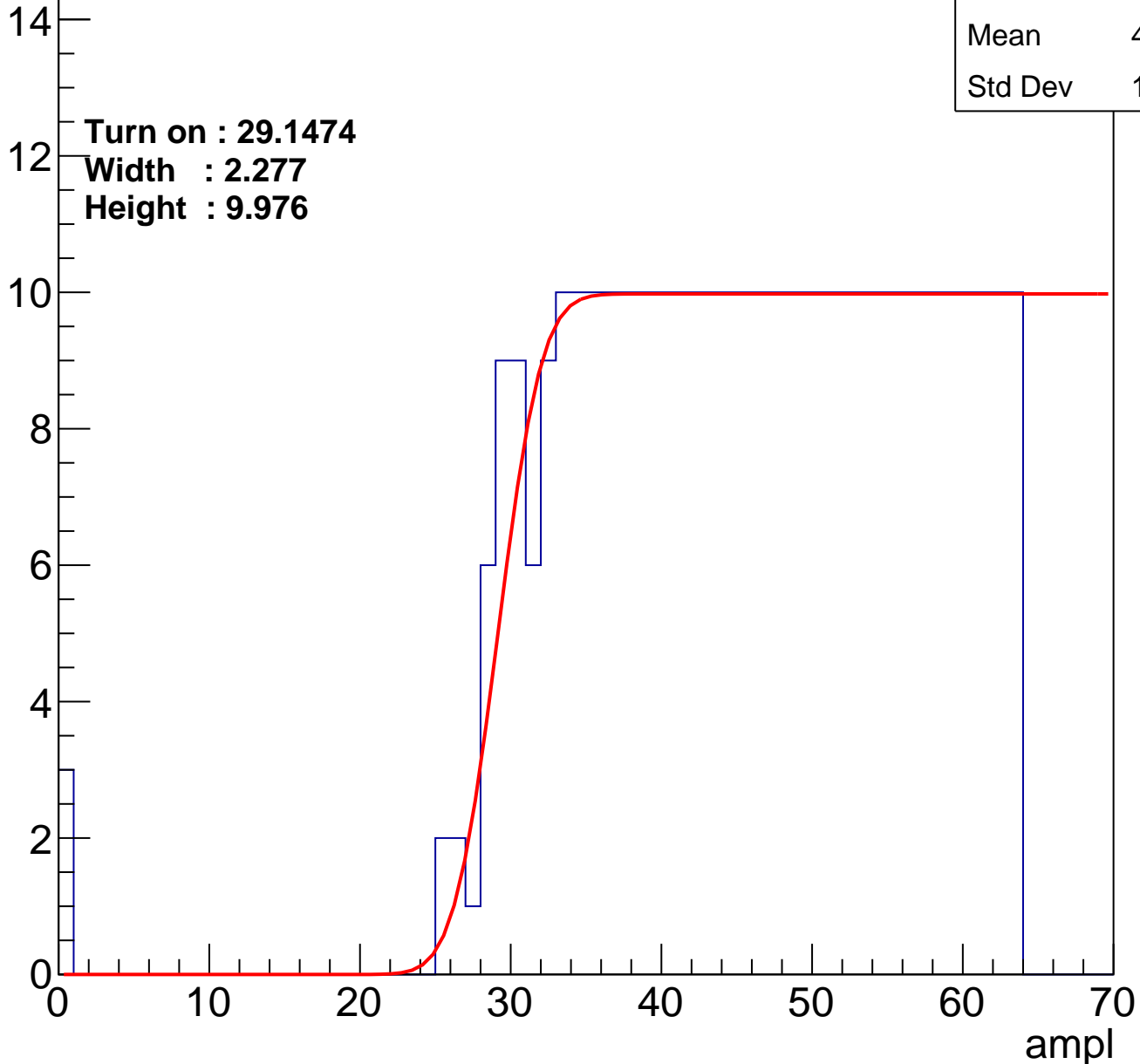
Entries	357
Mean	45.33
Std Dev	11.13

Turn on : 29.1474

Width : 2.277

Height : 9.976

Entry



# B0L000S, U4-ch24

calib\_packv5\_042523\_0143.root, FC#5, port B1

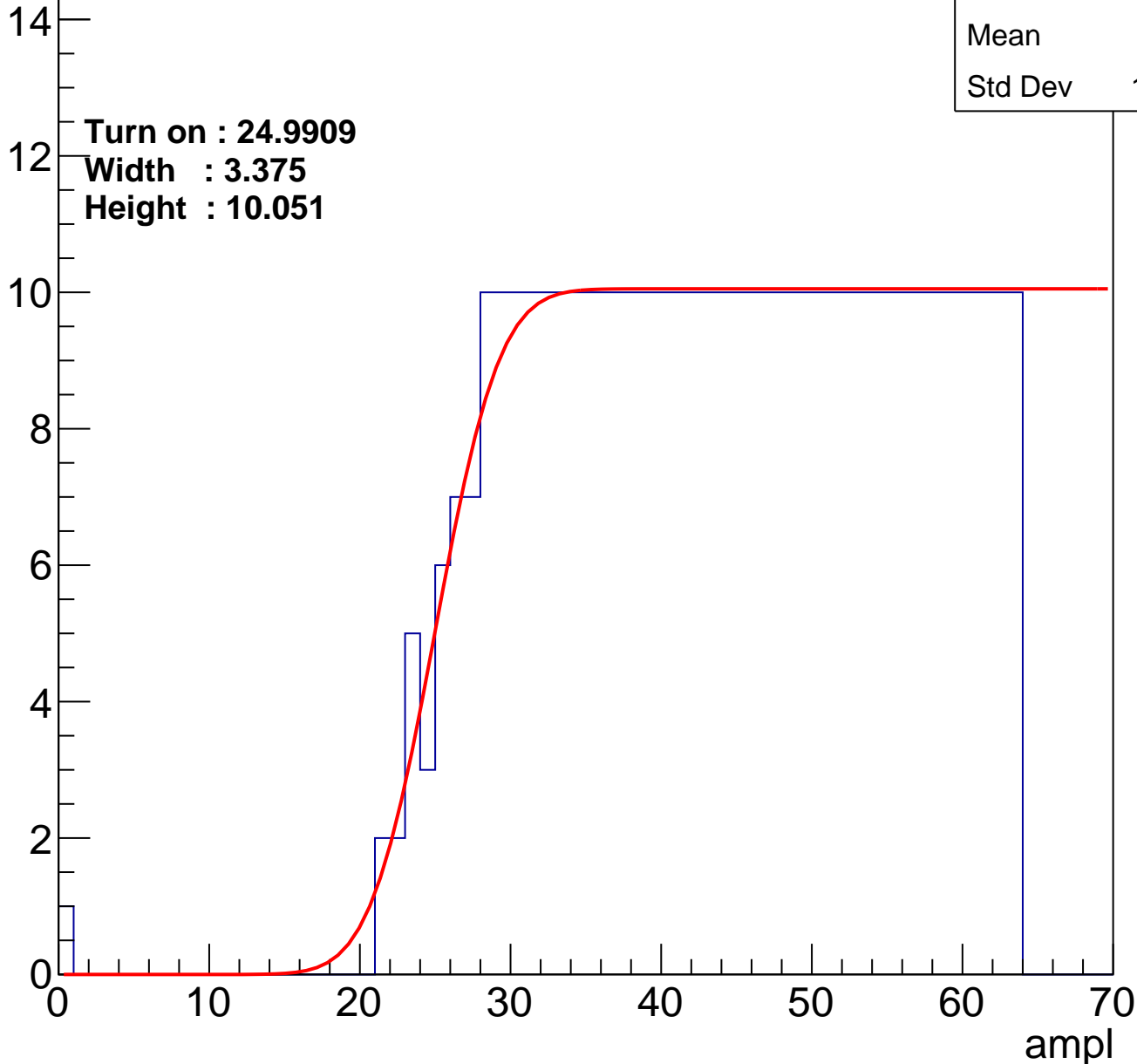
Entries	393
Mean	43.7
Std Dev	11.66

Turn on : 24.9909

Width : 3.375

Height : 10.051

Entry



# B0L000S, U4-ch25

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	364
Mean	44.96
Std Dev	11.33

**Turn on : 28.5350**

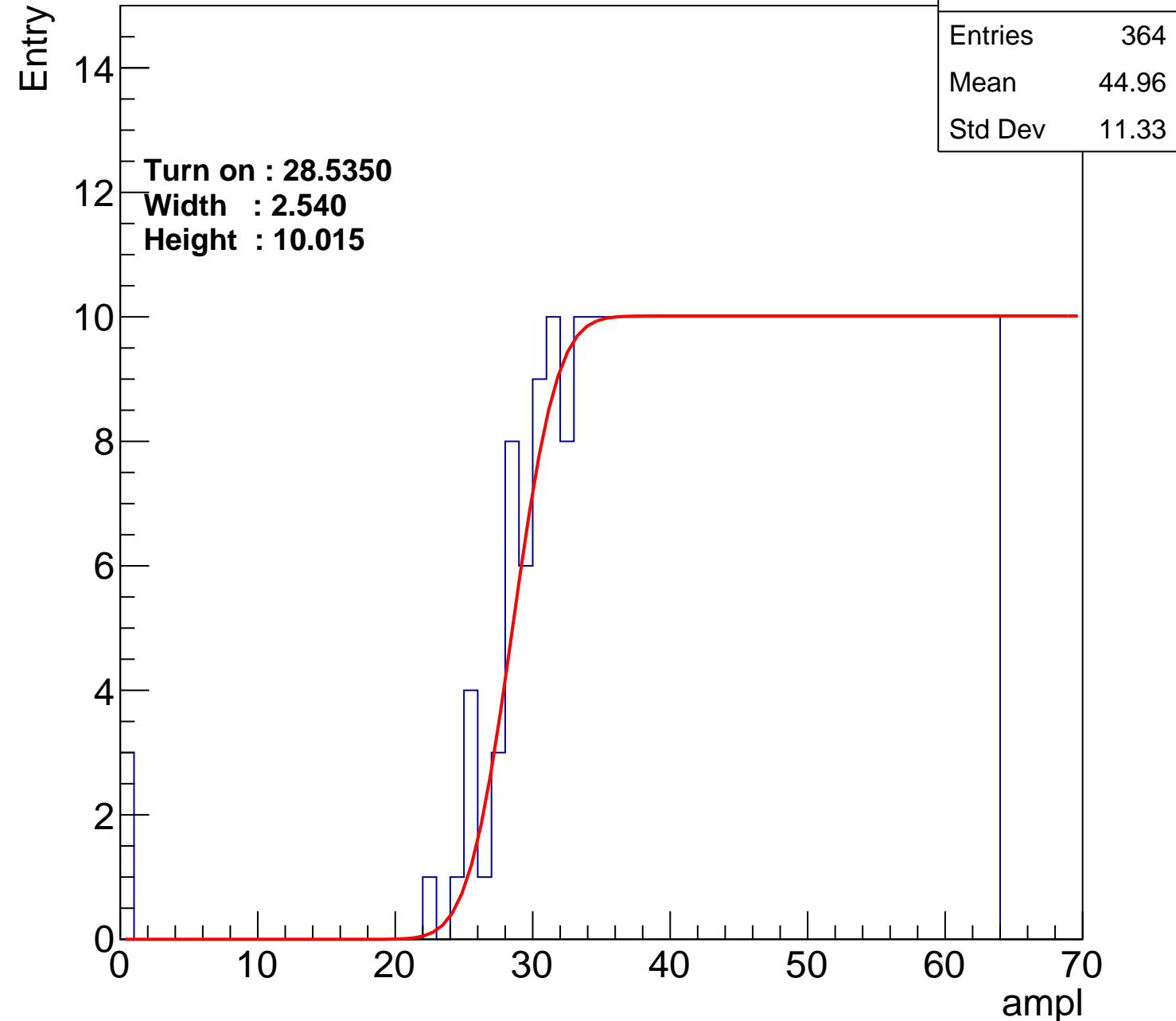
**Width : 2.540**

**Height : 10.015**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch26

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	363
Mean	45.06
Std Dev	11.15

Turn on : 28.1894

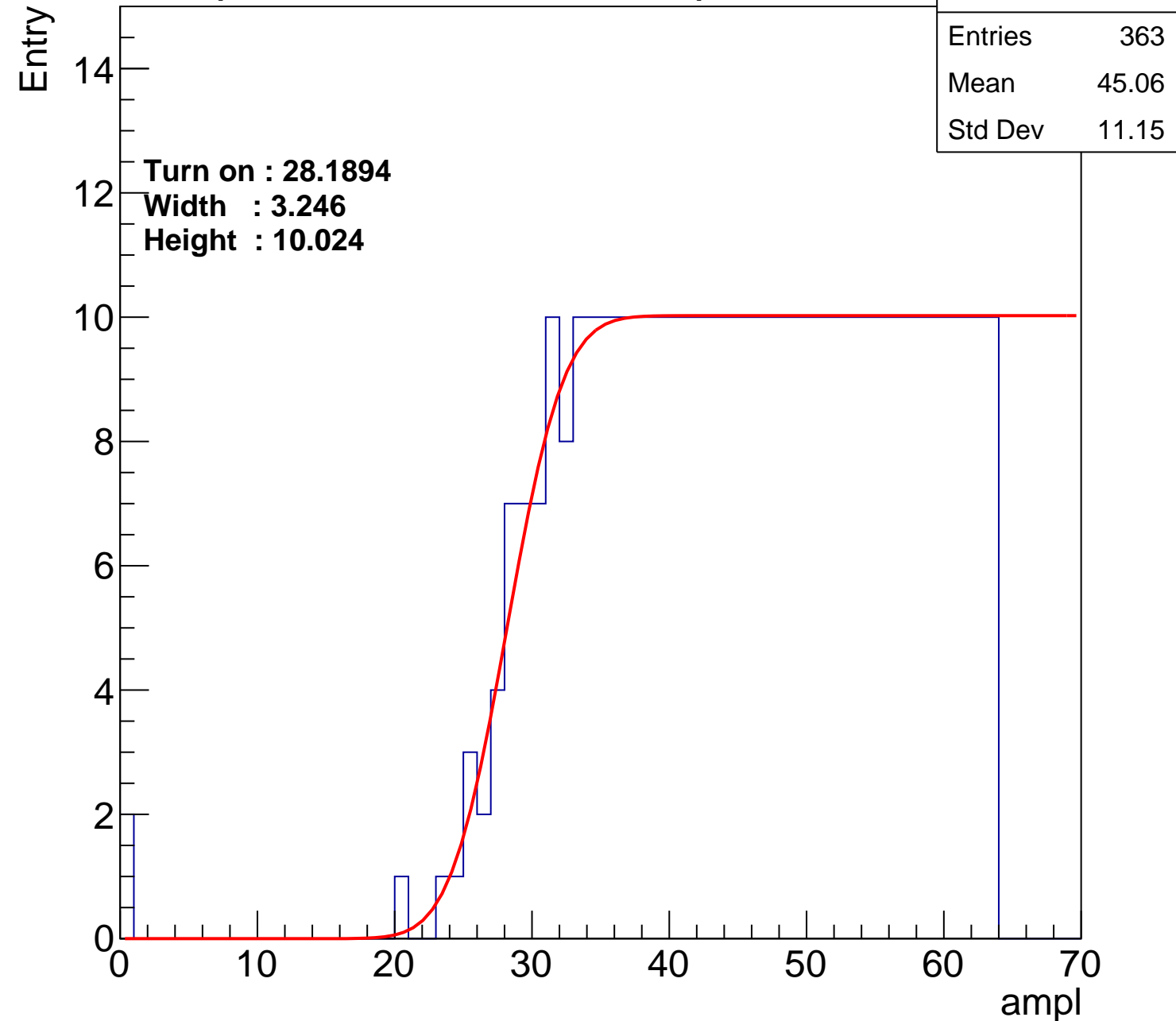
Width : 3.246

Height : 10.024

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch27

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	371
Mean	44.77
Std Dev	11.09

Turn on : 26.9515

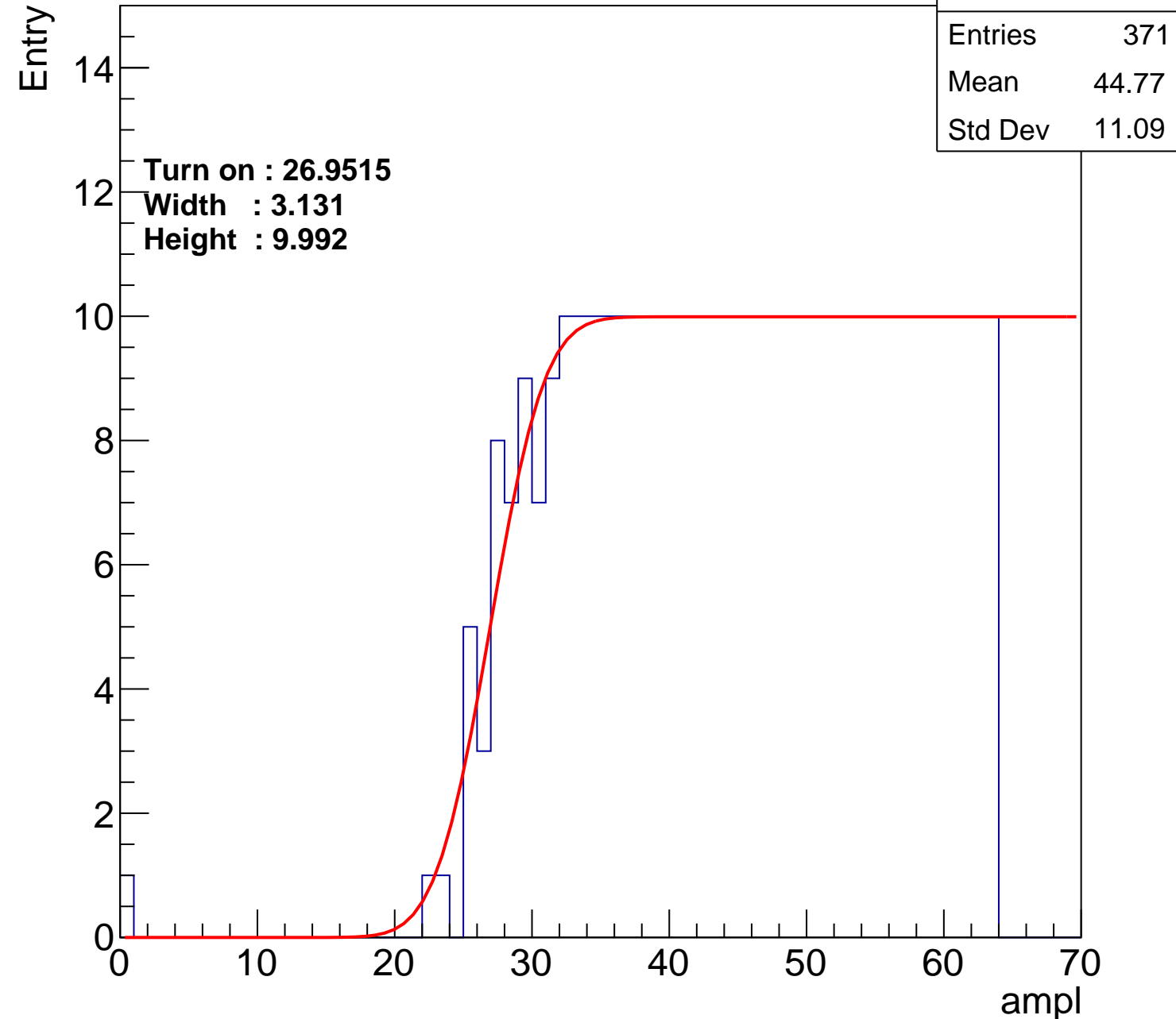
Width : 3.131

Height : 9.992

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch28

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	369
Mean	44.45
Std Dev	12.11

**Turn on : 28.5157**

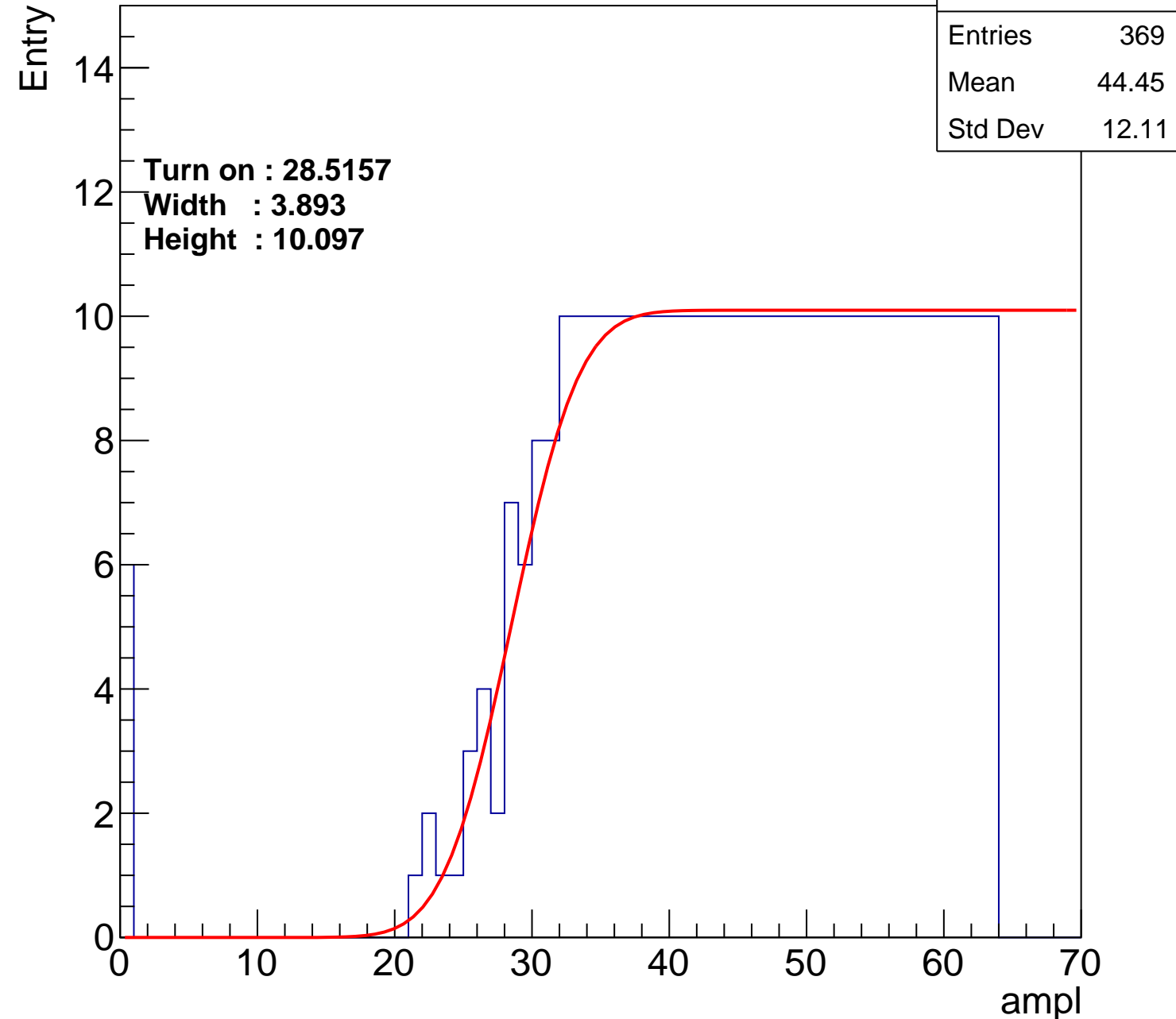
**Width : 3.893**

**Height : 10.097**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch29

calib\_packv5\_042523\_0143.root, FC#5, port B1

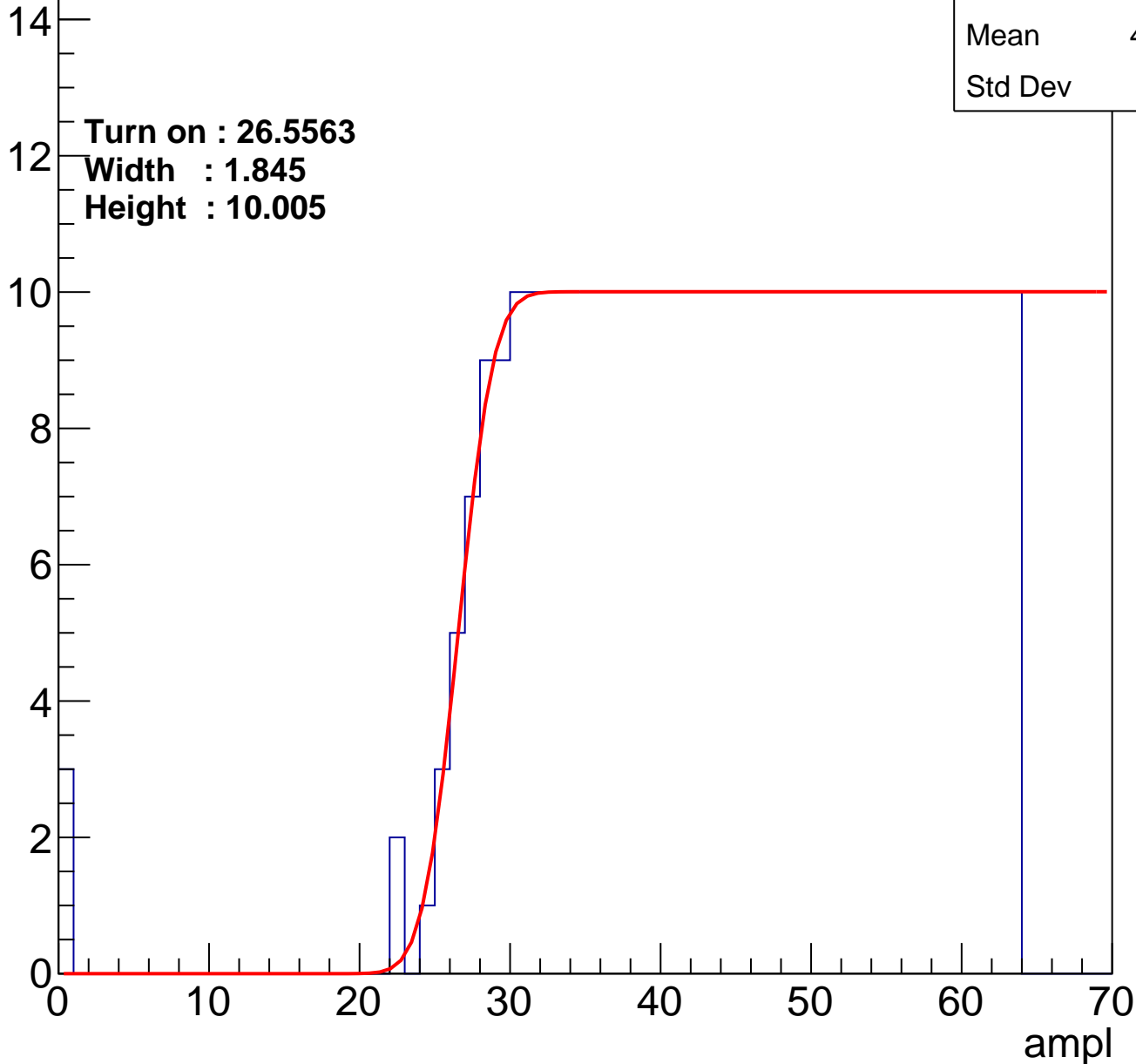
Entry

Entries	379
Mean	44.29
Std Dev	11.61

Turn on : 26.5563

Width : 1.845

Height : 10.005



# B0L000S, U4-ch30

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	358
Mean	45.21
Std Dev	11.36

**Turn on : 28.8760**

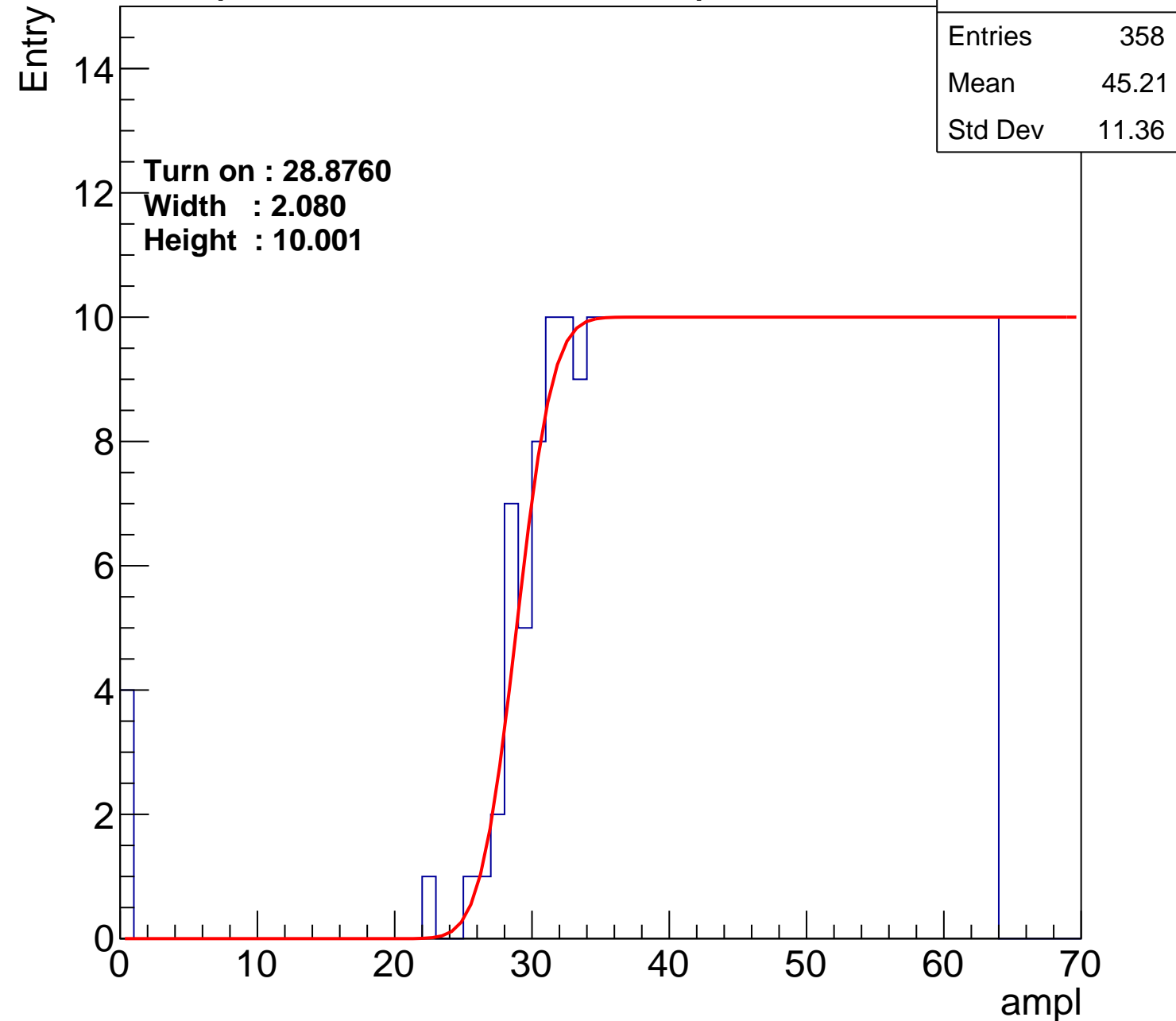
**Width : 2.080**

**Height : 10.001**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L000S, U4-ch31

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	370
Mean	44.76
Std Dev	11.25

**Turn on : 27.3113**

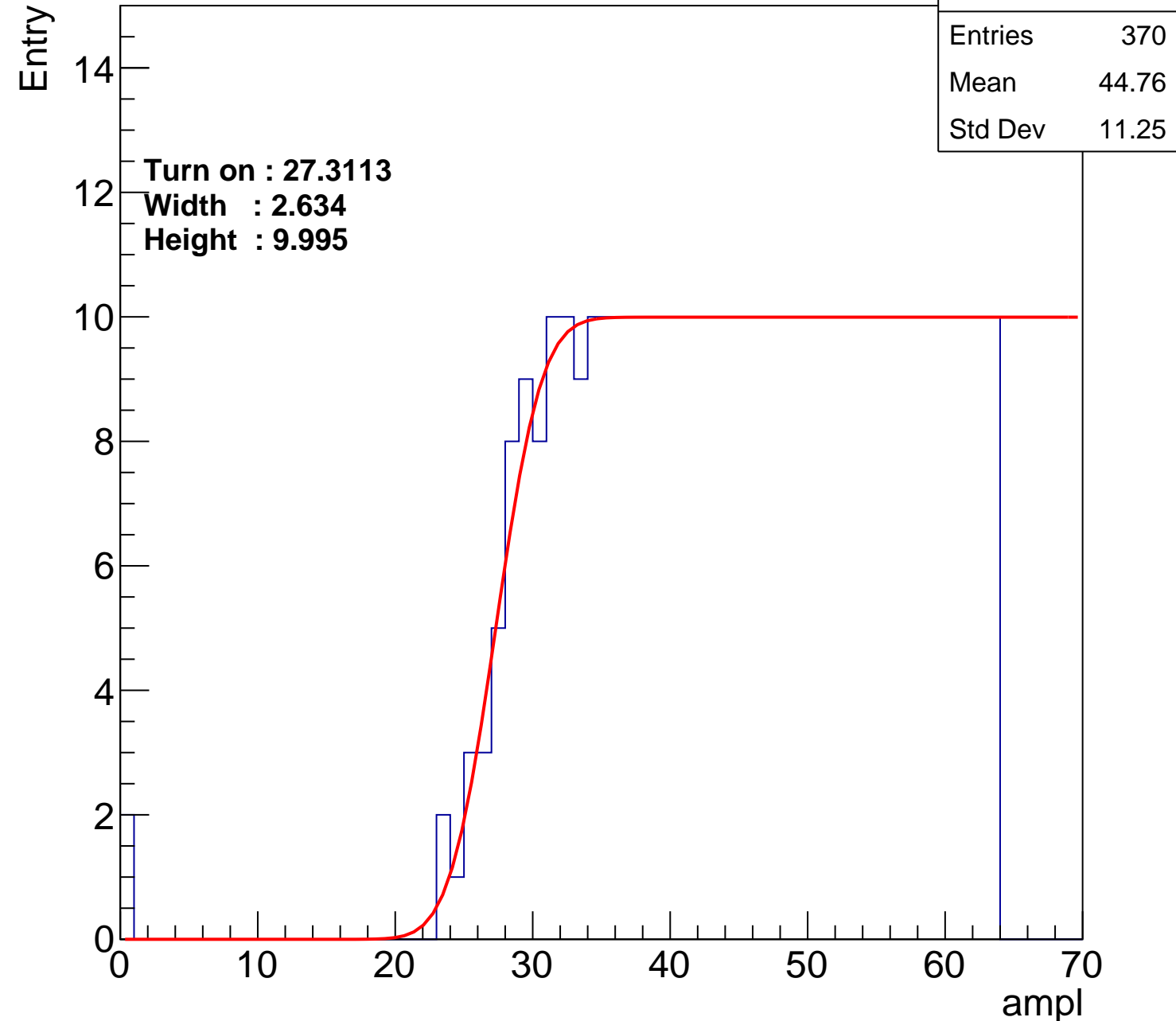
**Width : 2.634**

**Height : 9.995**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch32

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	377
Mean	44.29
Std Dev	11.69

Turn on : 26.6624

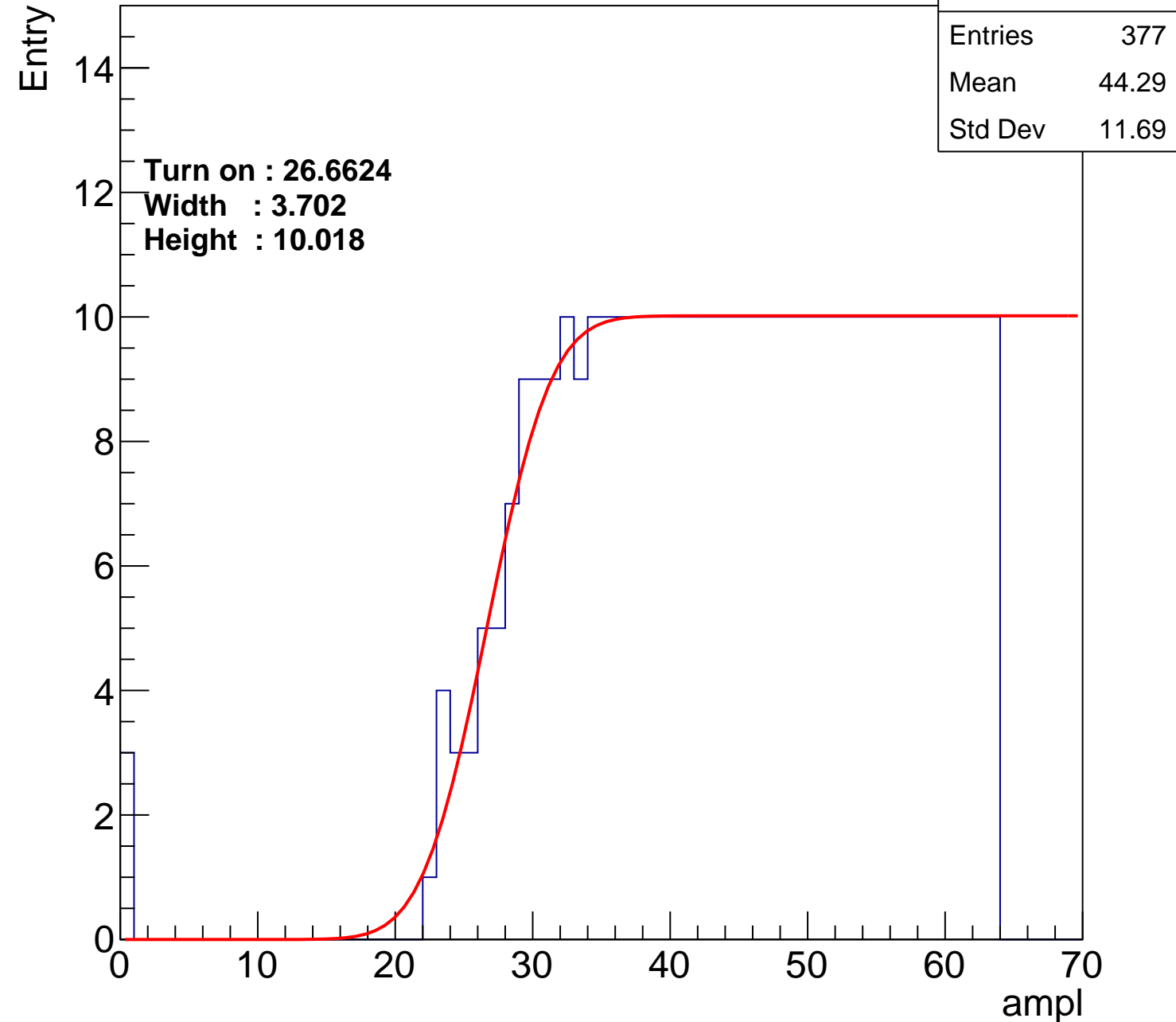
Width : 3.702

Height : 10.018

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch33

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	379
Mean	44.28
Std Dev	11.55

Turn on : 26.6617

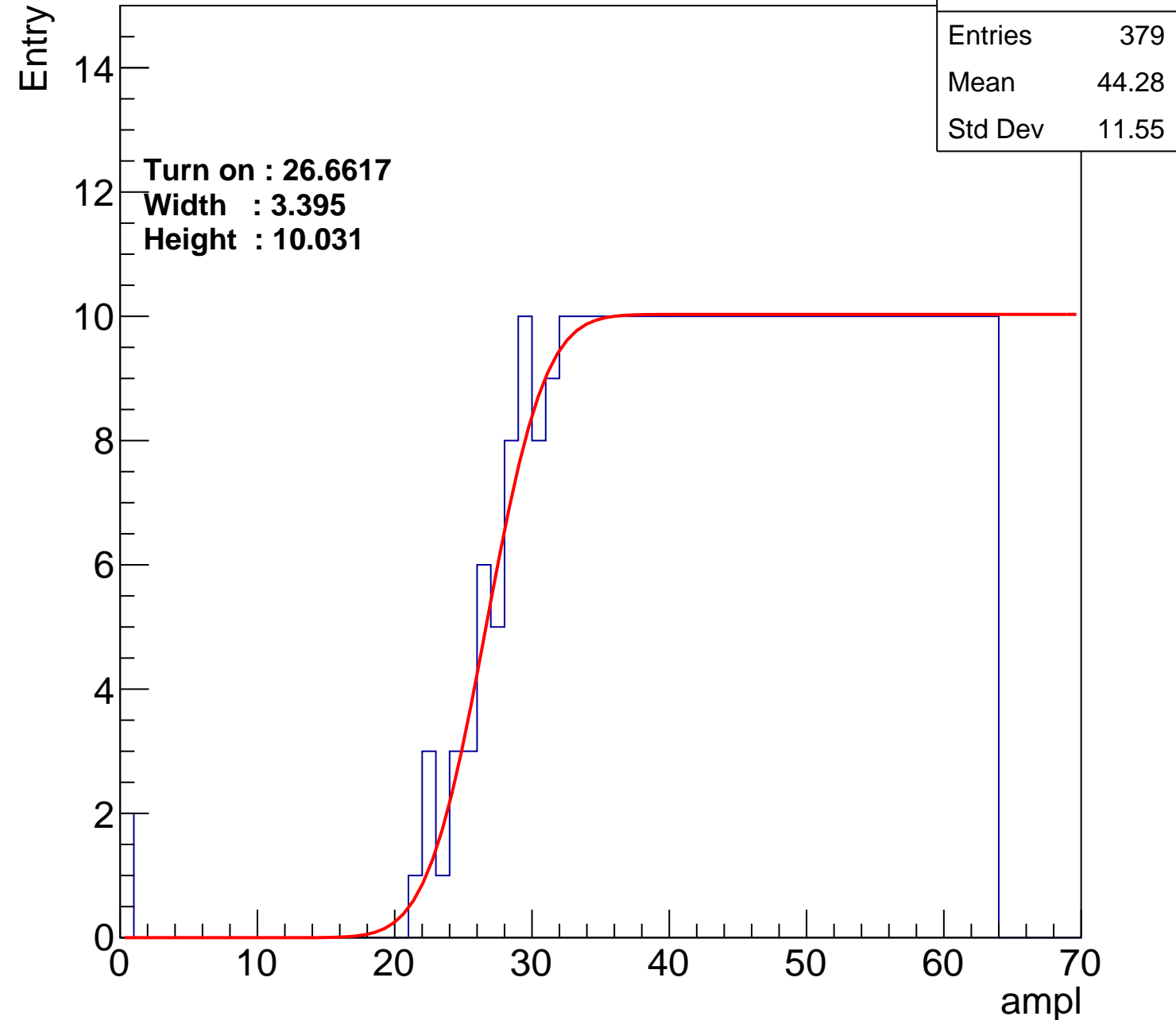
Width : 3.395

Height : 10.031

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch34

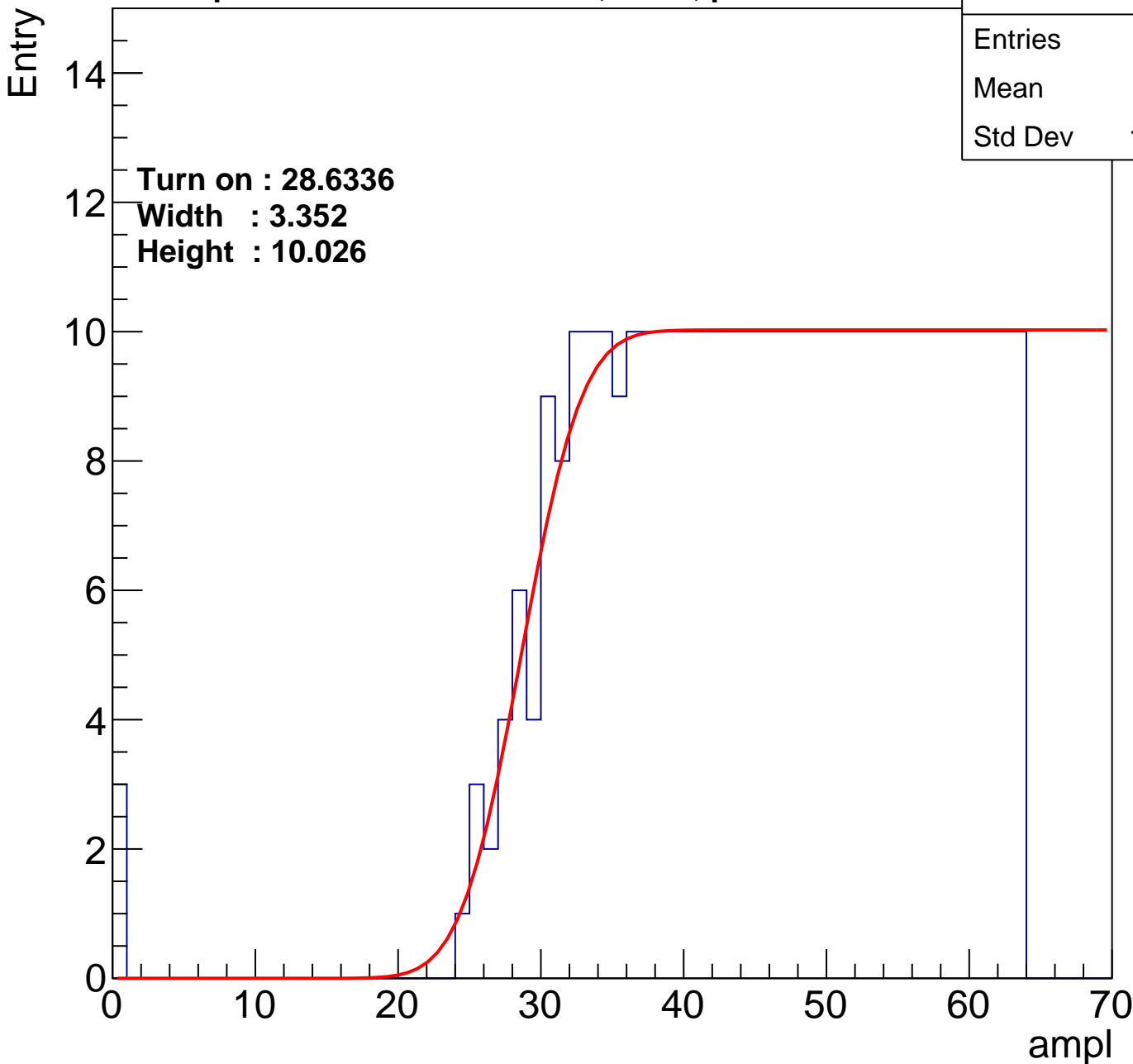
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	359
Mean	45.2
Std Dev	11.23

Turn on : 28.6336

Width : 3.352

Height : 10.026



# B0L000S, U4-ch35

**calib\_packv5\_042523\_0143.root, FC#5, port B1**

Entries	367
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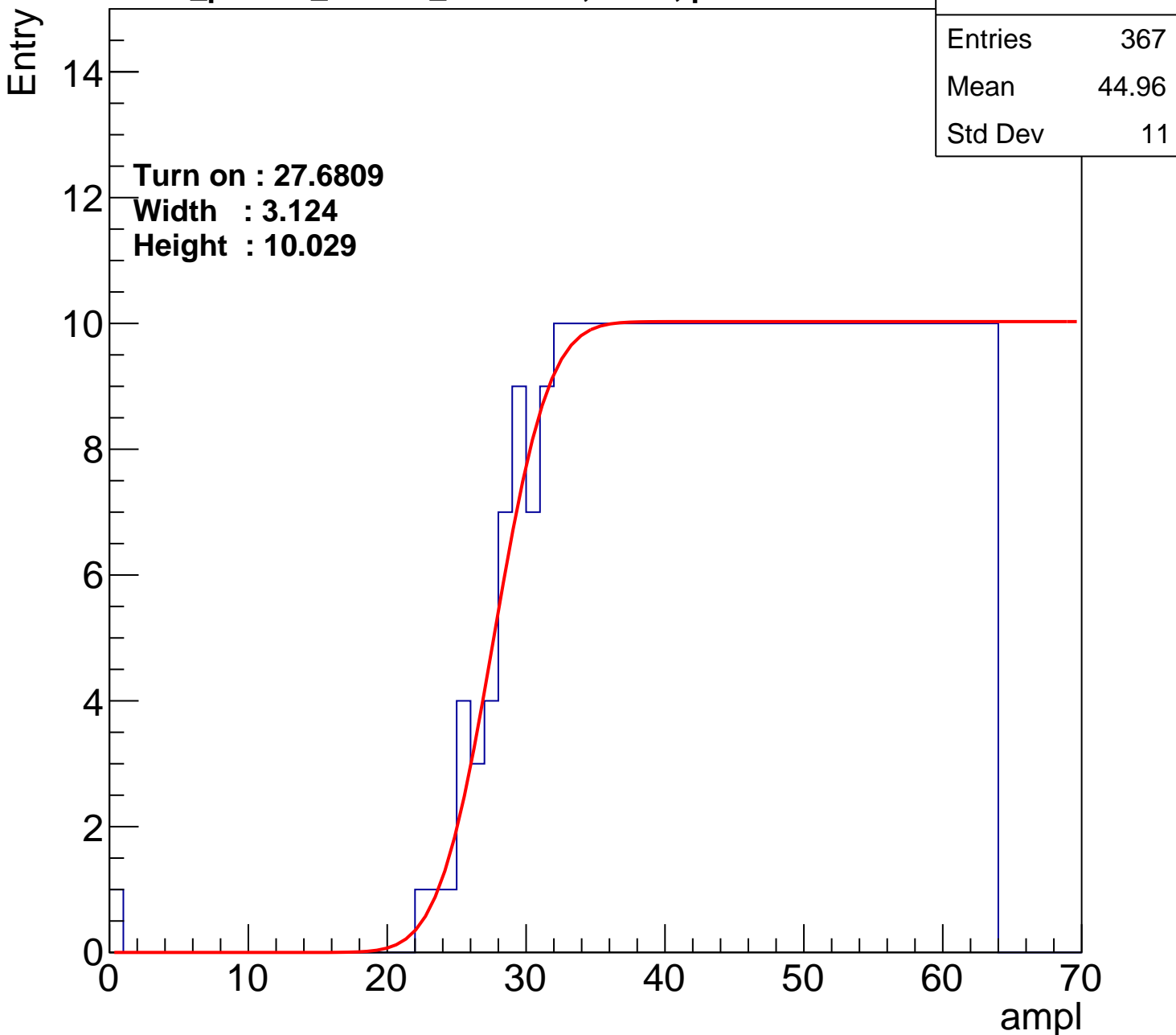
Mean	44.96
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Std Dev	11
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**Turn on : 27.6809**

**Width : 3.124**

**Height : 10.029**



# B0L000S, U4-ch36

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	368
Mean	44.84
Std Dev	11.23

Turn on : 27.7519

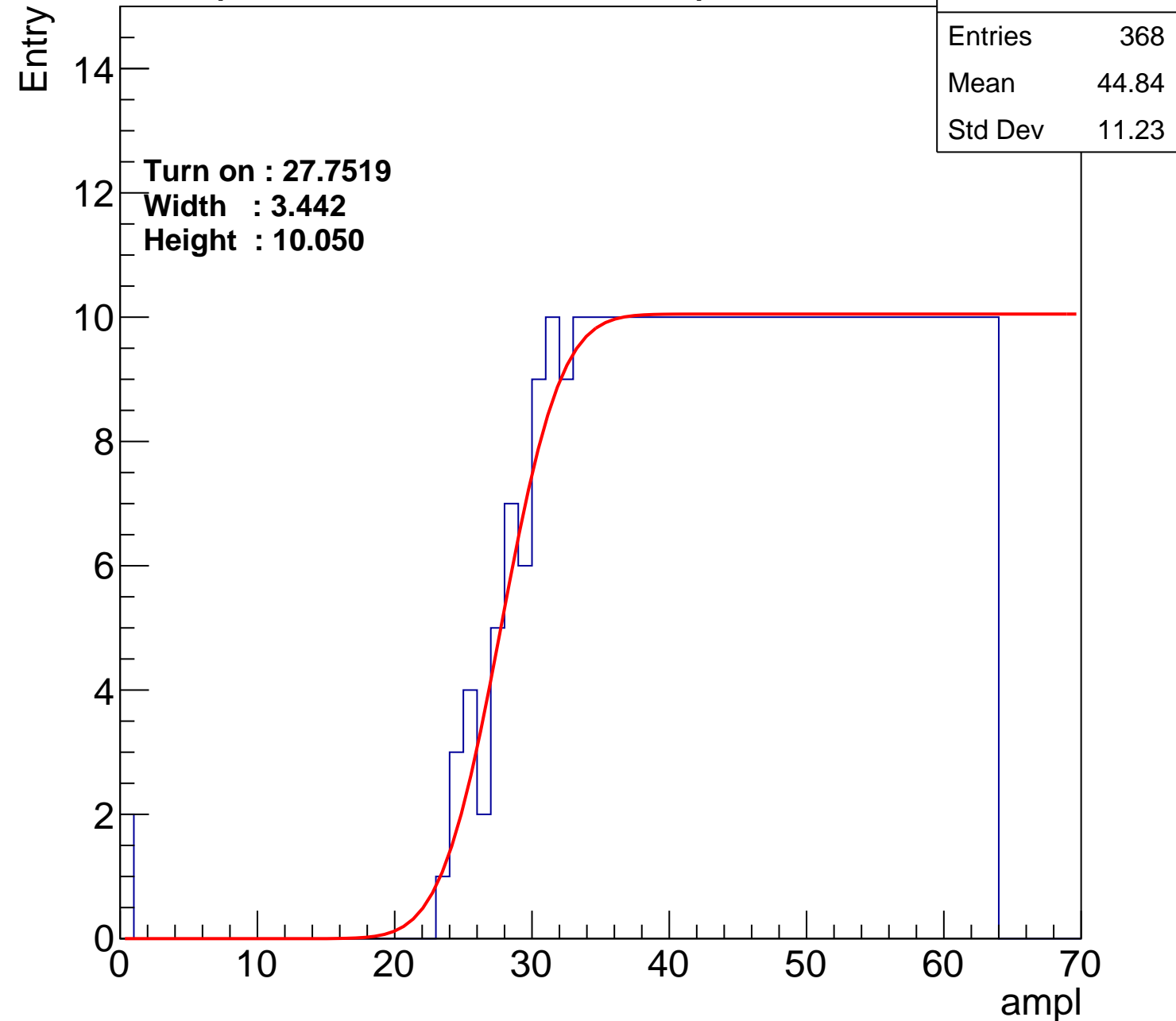
Width : 3.442

Height : 10.050

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch37

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	371
Mean	44.66
Std Dev	11.44

**Turn on : 27.5100**

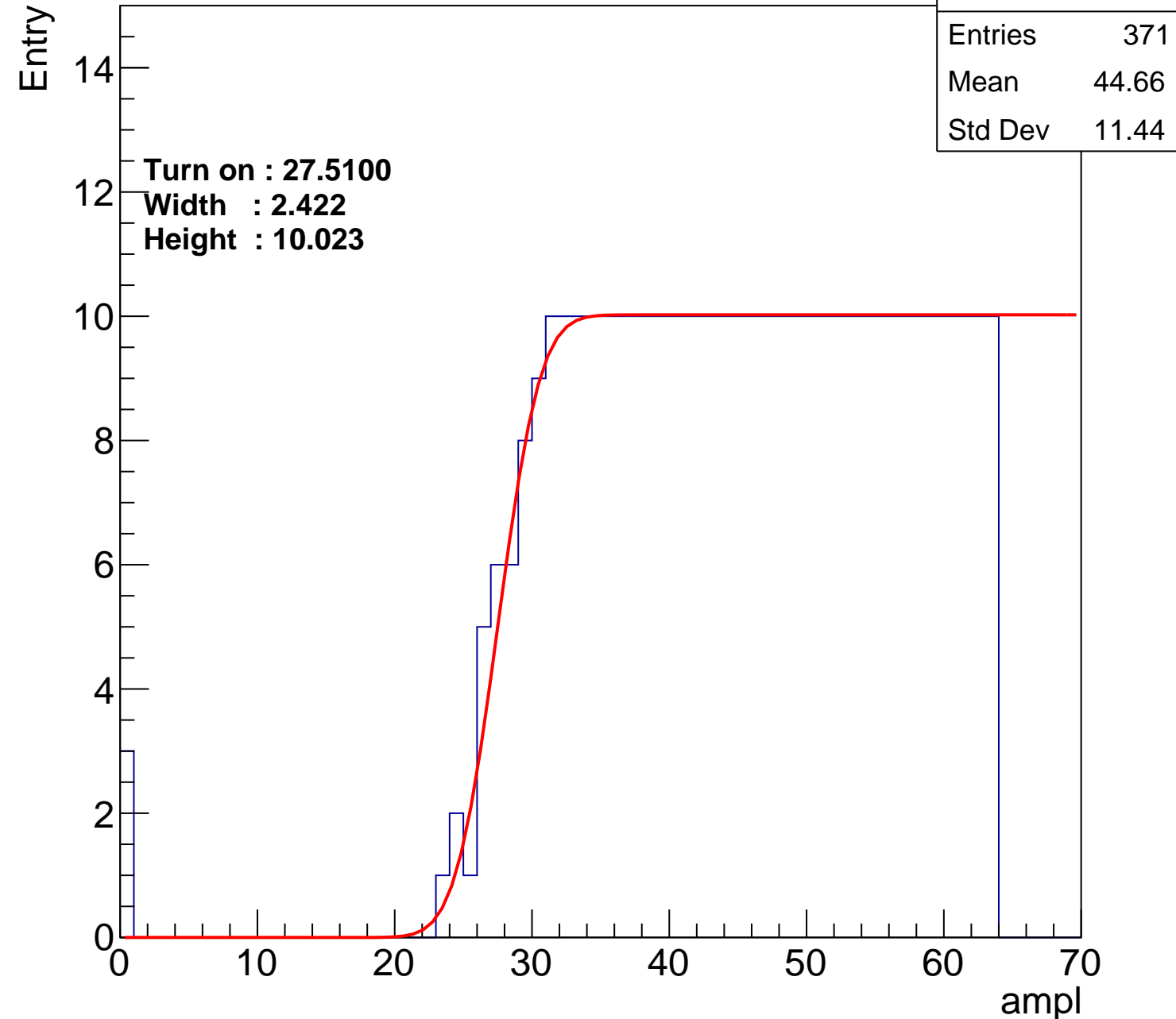
**Width : 2.422**

**Height : 10.023**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch38

calib\_packv5\_042523\_0143.root, FC#5, port B1

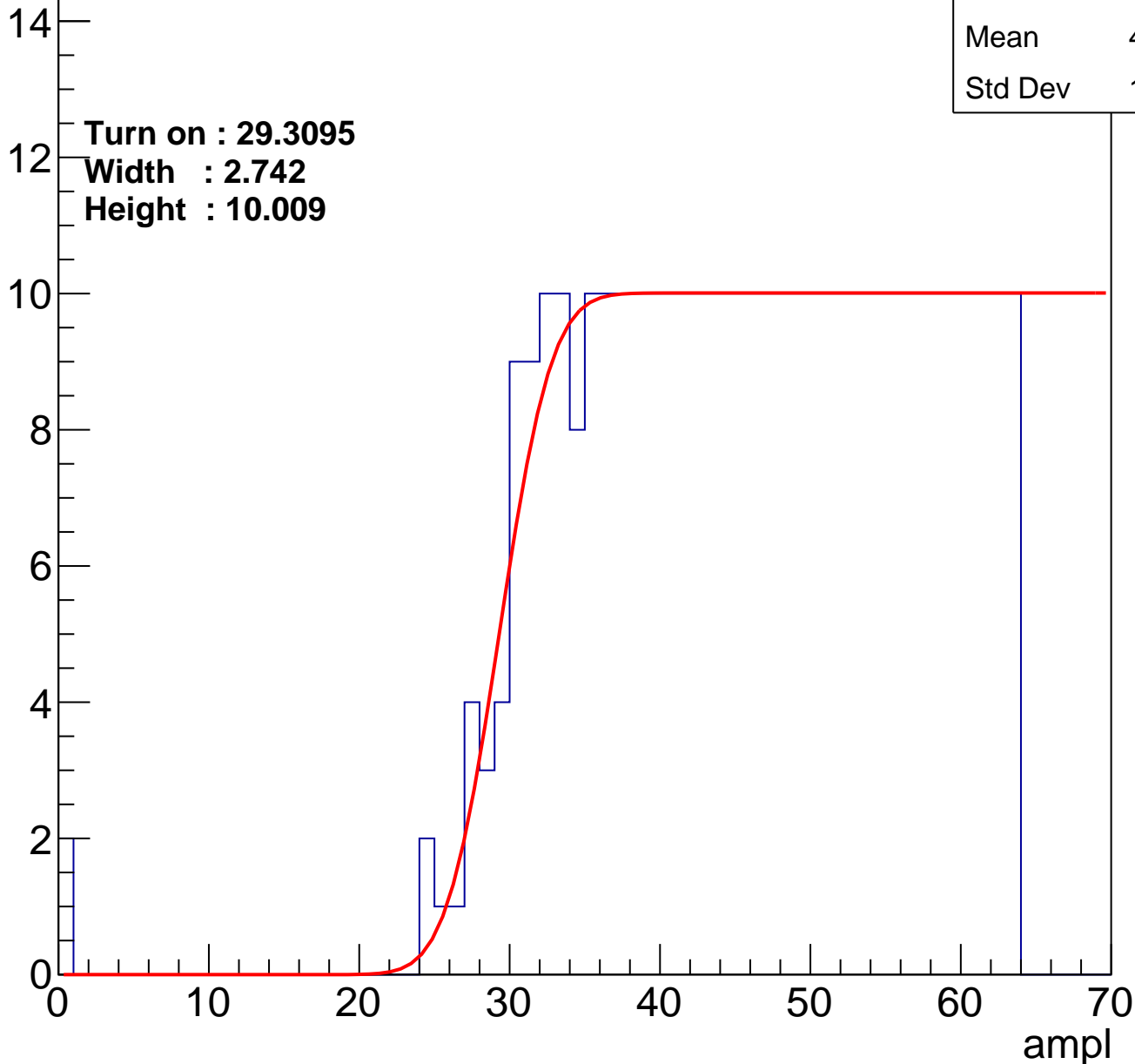
Entry

Entries	353
Mean	45.58
Std Dev	10.85

Turn on : 29.3095

Width : 2.742

Height : 10.009





# B0L000S, U4-ch39

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	365
Mean	45.07
Std Dev	10.93

Turn on : 27.9251

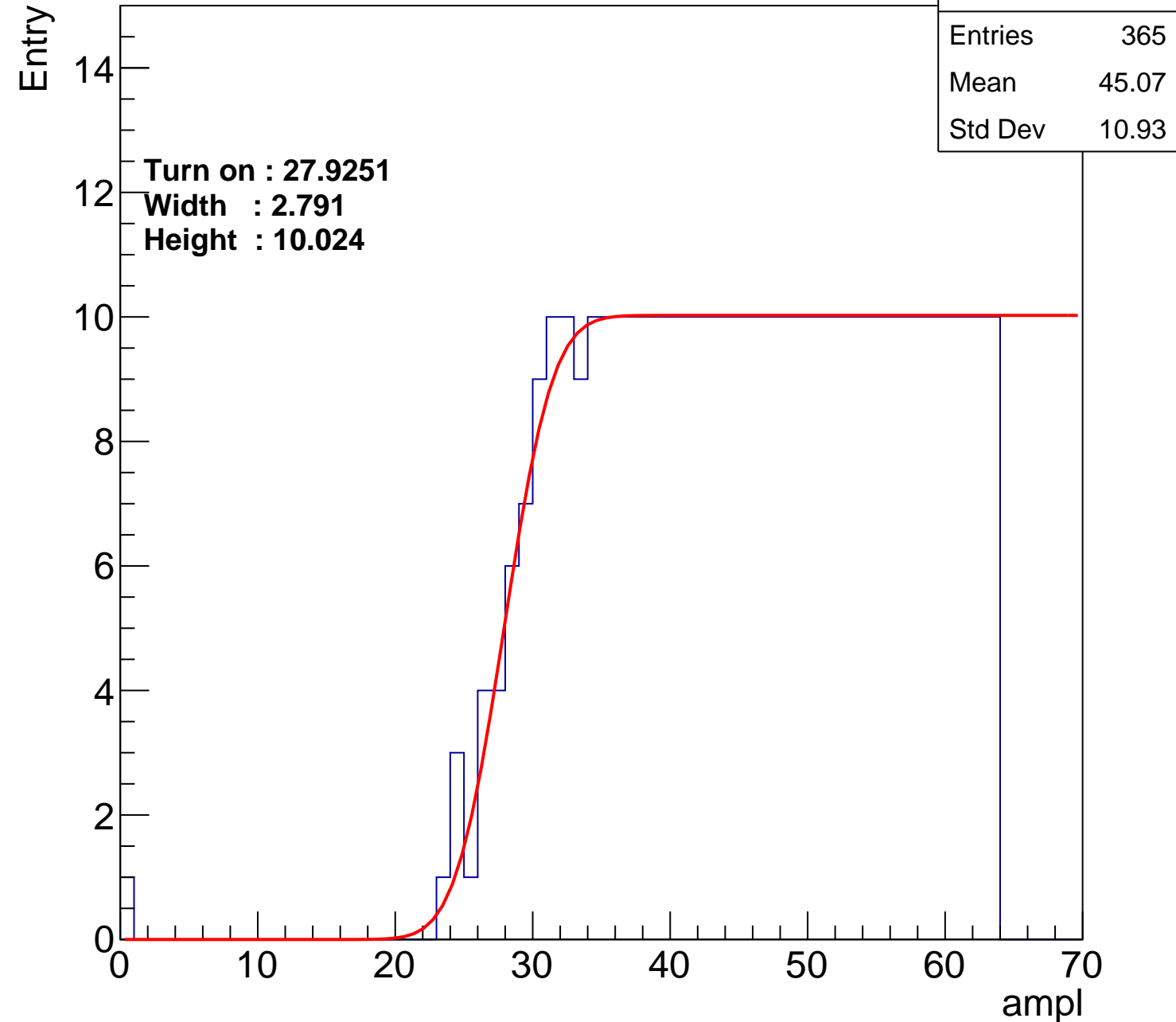
Width : 2.791

Height : 10.024

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch40

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	391
Mean	43.82
Std Dev	11.58

**Turn on : 24.9689**

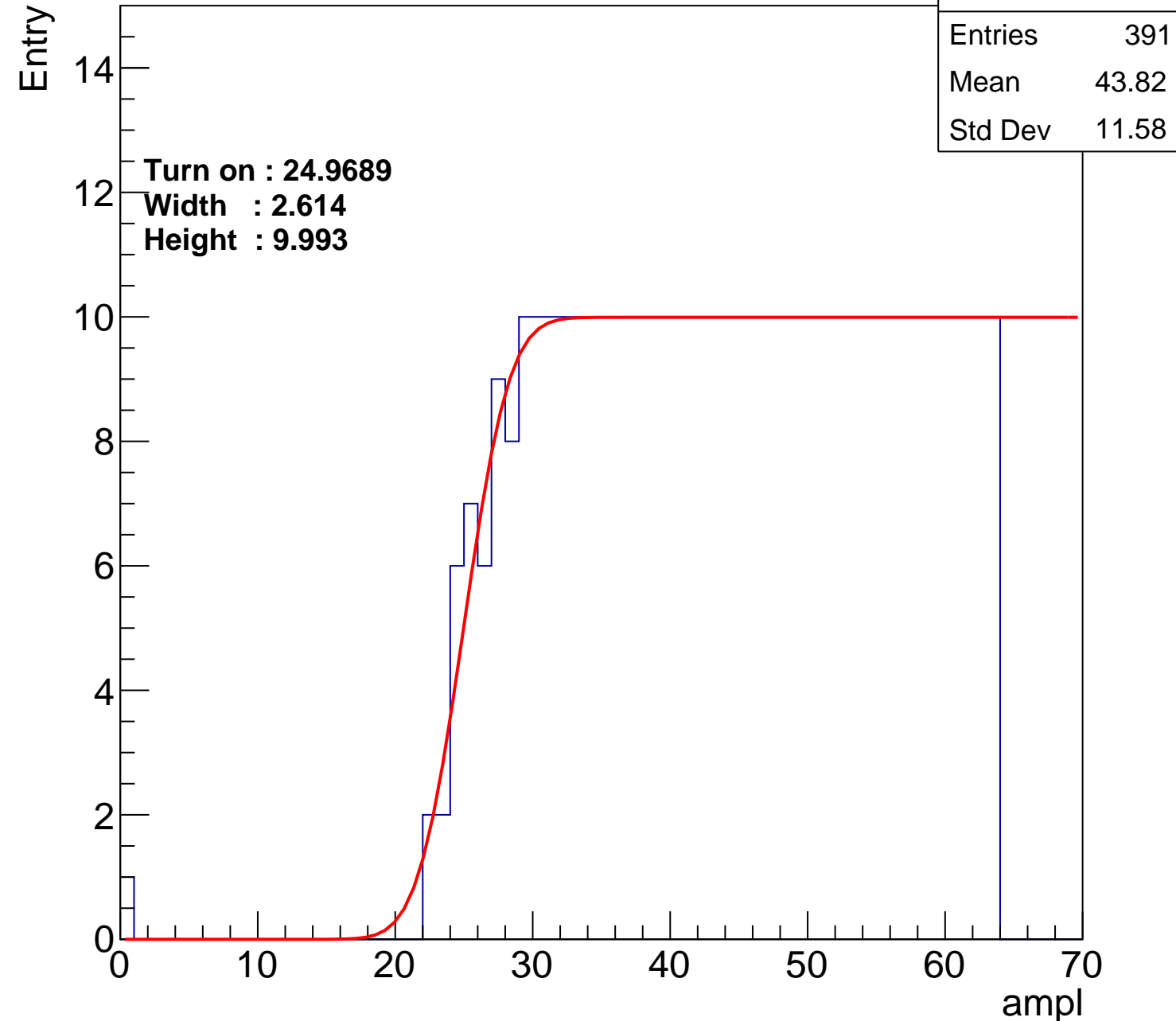
**Width : 2.614**

**Height : 9.993**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch41

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	373
Mean	44.67
Std Dev	11.14

Turn on : 27.1718

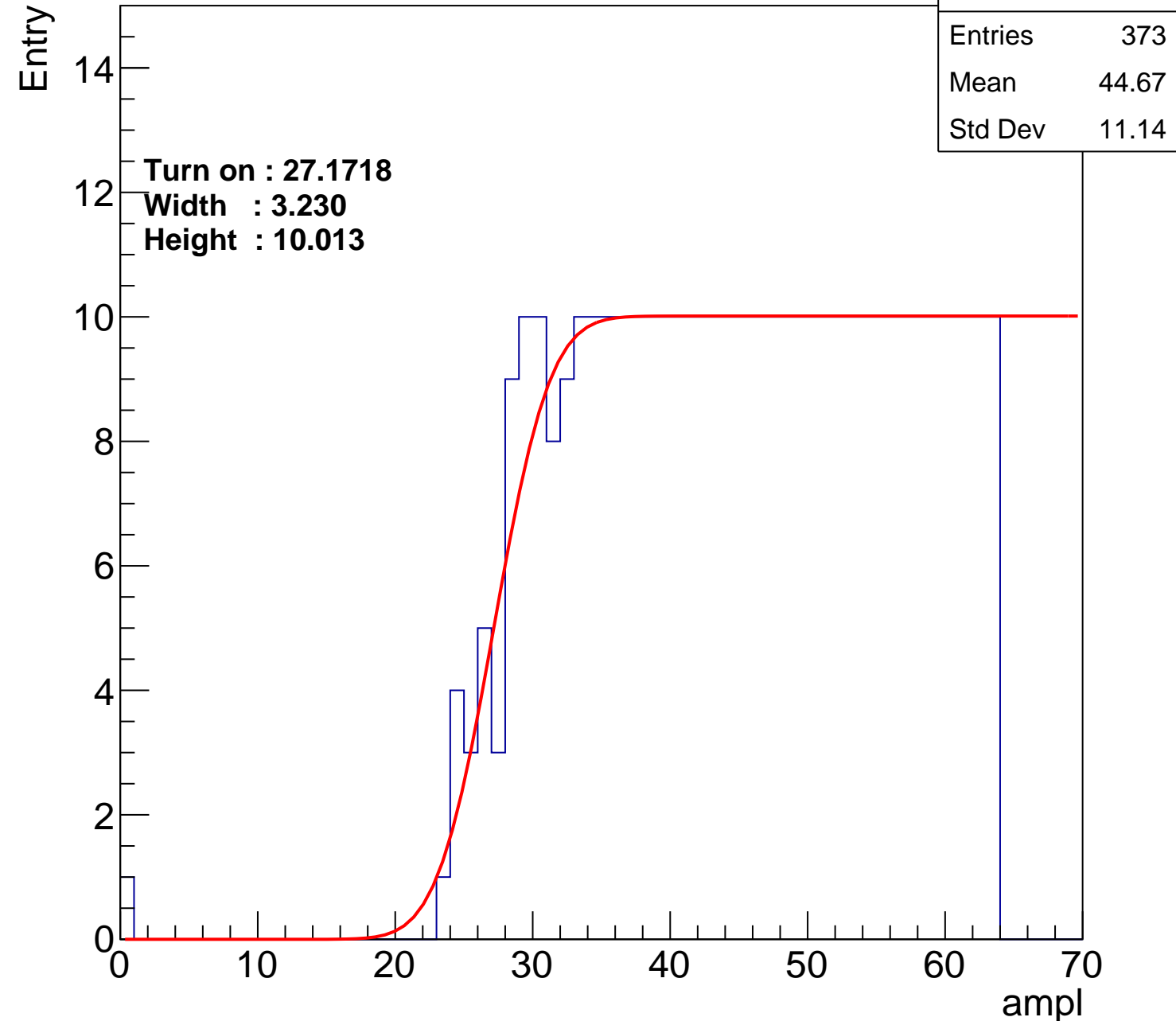
Width : 3.230

Height : 10.013

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch42

calib\_packv5\_042523\_0143.root, FC#5, port B1

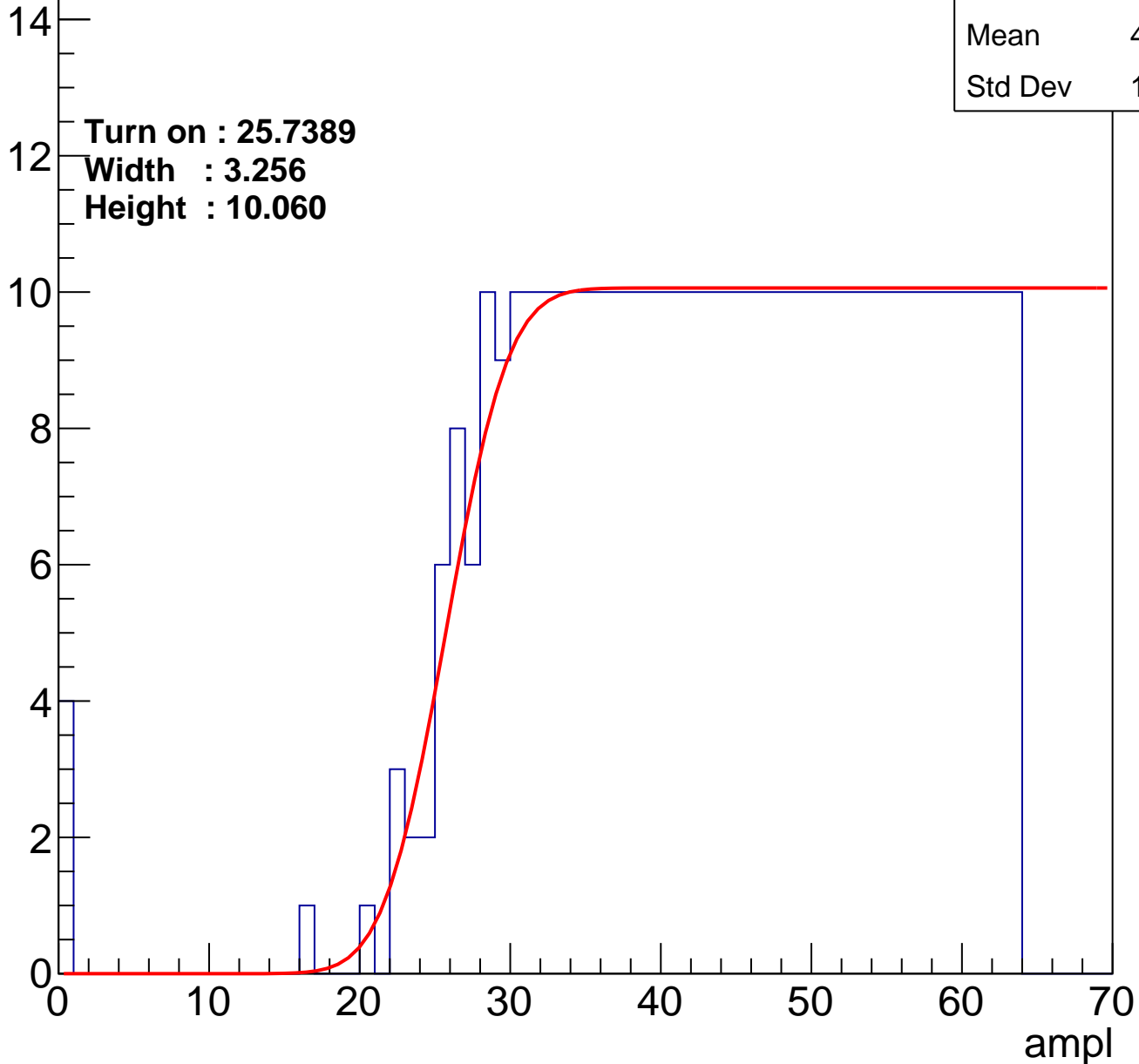
Entries	392
Mean	43.54
Std Dev	12.17

**Turn on : 25.7389**

**Width : 3.256**

**Height : 10.060**

Entry



# B0L000S, U4-ch43

calib\_packv5\_042523\_0143.root, FC#5, port B1

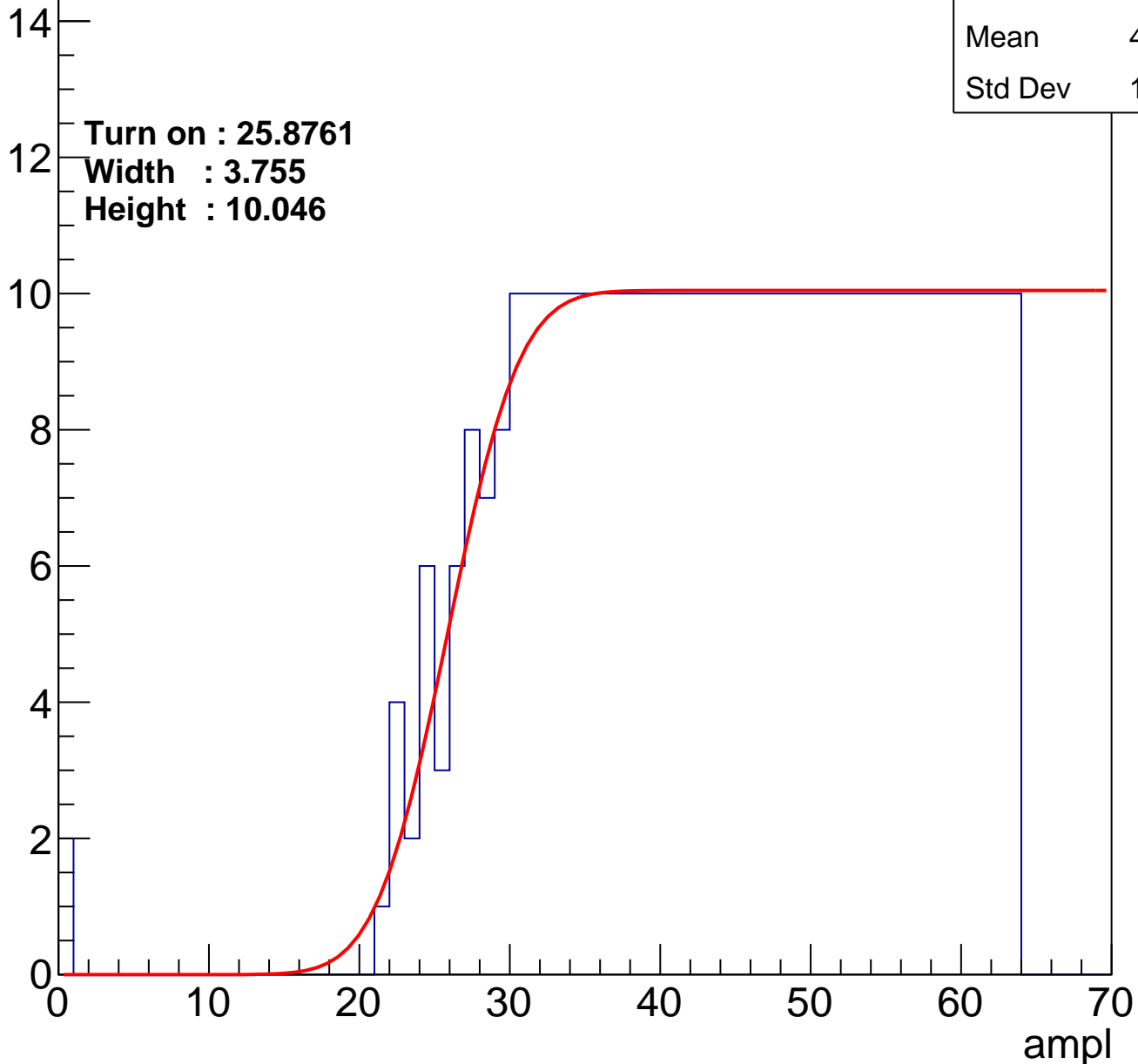
Entry

Entries	387
Mean	43.89
Std Dev	11.75

Turn on : 25.8761

Width : 3.755

Height : 10.046



# B0L000S, U4-ch44

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	400
Mean	43.12
Std Dev	12.41

Turn on : 25.0034

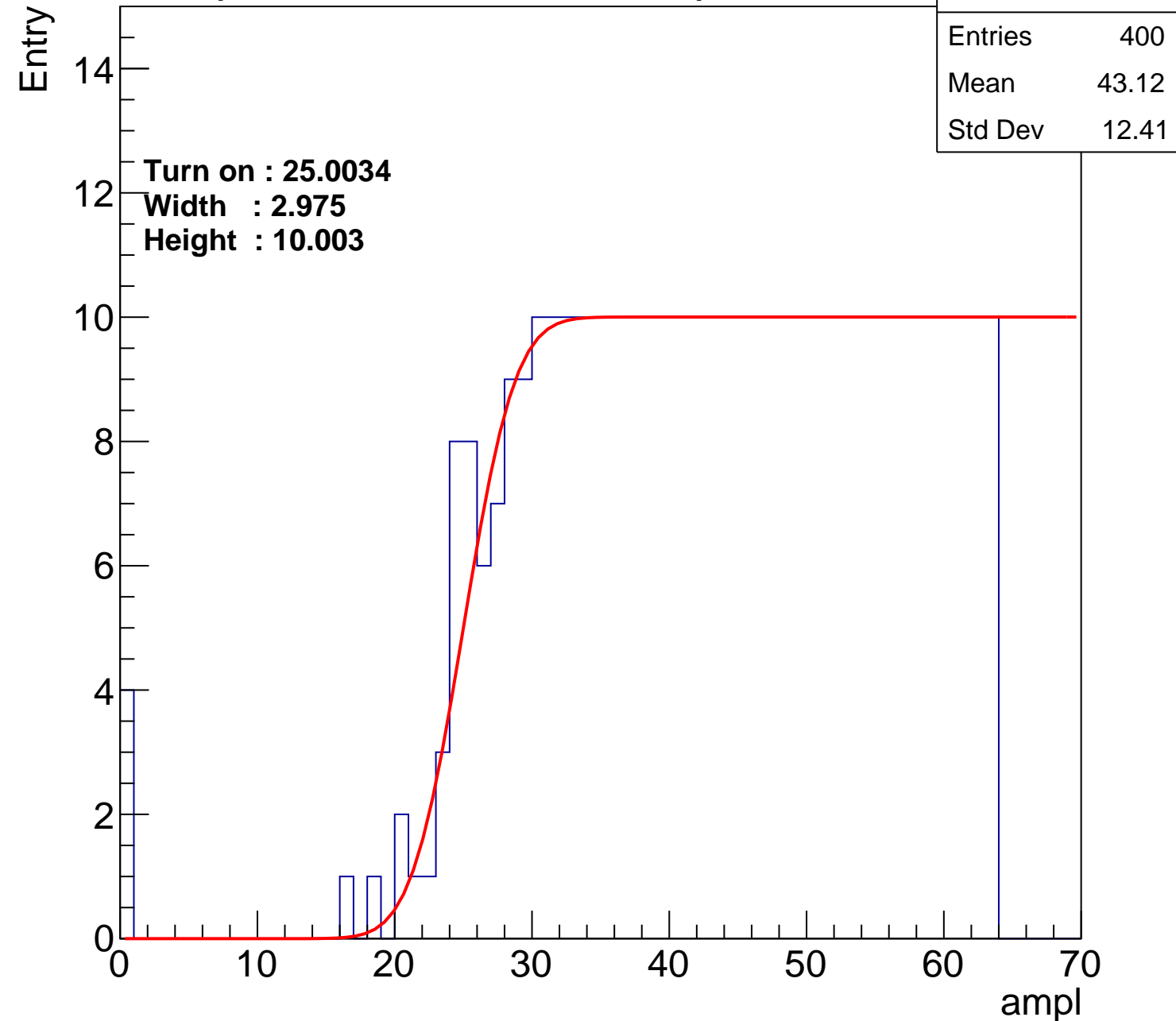
Width : 2.975

Height : 10.003

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch45

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	378
Mean	44.17
Std Dev	11.99

Turn on : 26.8718

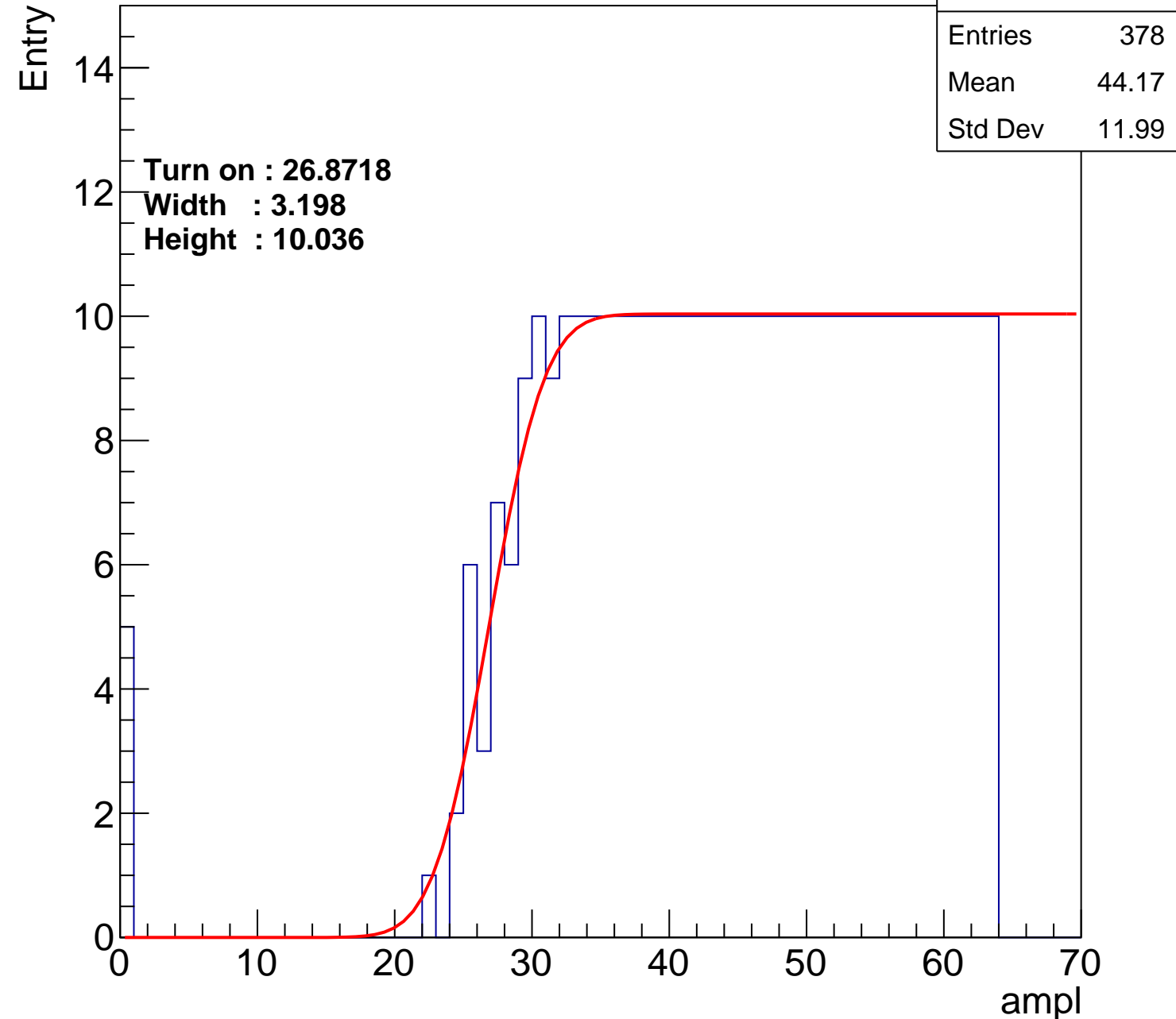
Width : 3.198

Height : 10.036

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch46

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	363
Mean	45.13
Std Dev	11.04

**Turn on : 27.8679**

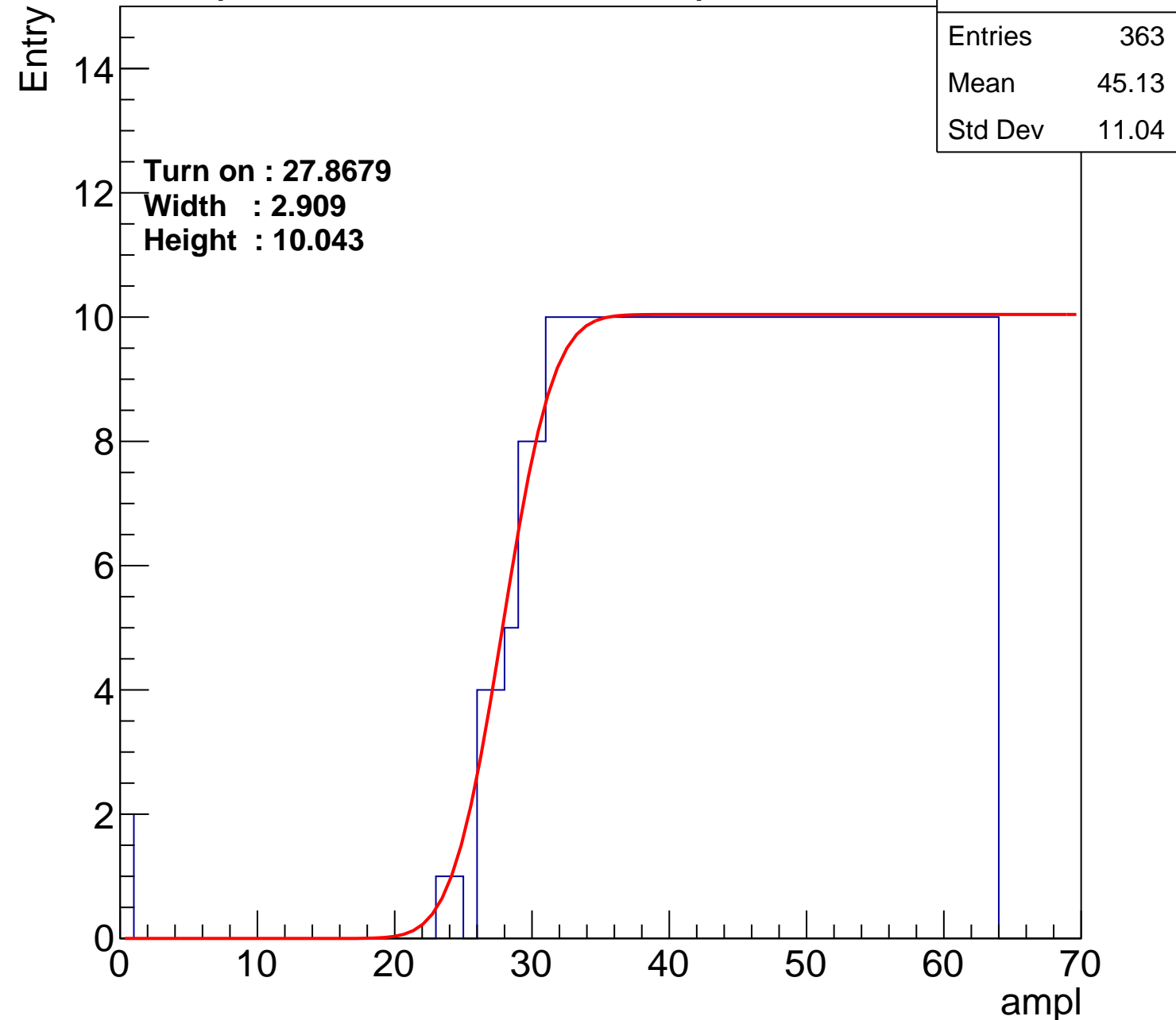
**Width : 2.909**

**Height : 10.043**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L000S, U4-ch47

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	392
Mean	43.72
Std Dev	11.68

**Turn on : 24.9702**

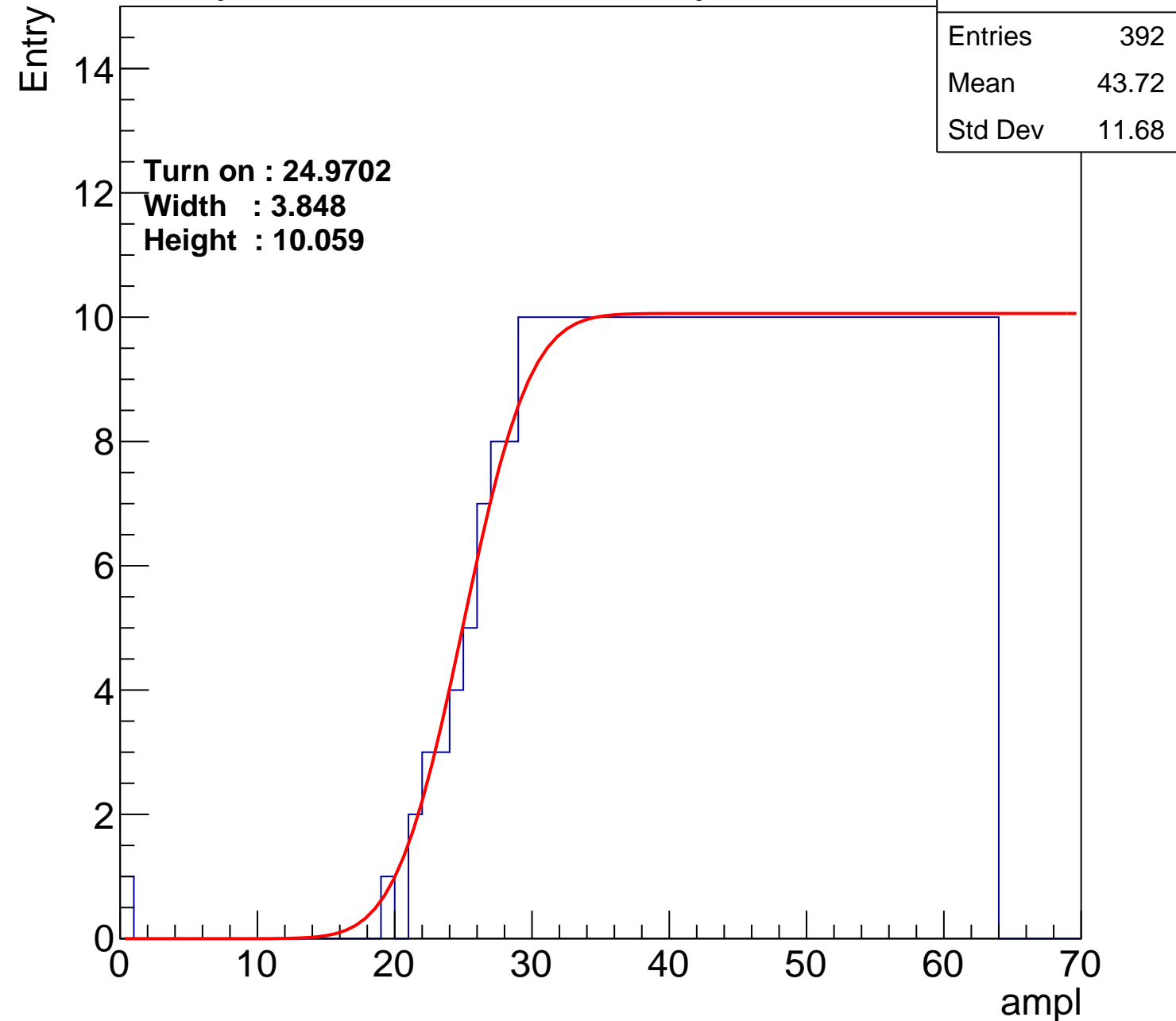
**Width : 3.848**

**Height : 10.059**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch48

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	367
Mean	44.77
Std Dev	11.48

Turn on : 28.1514

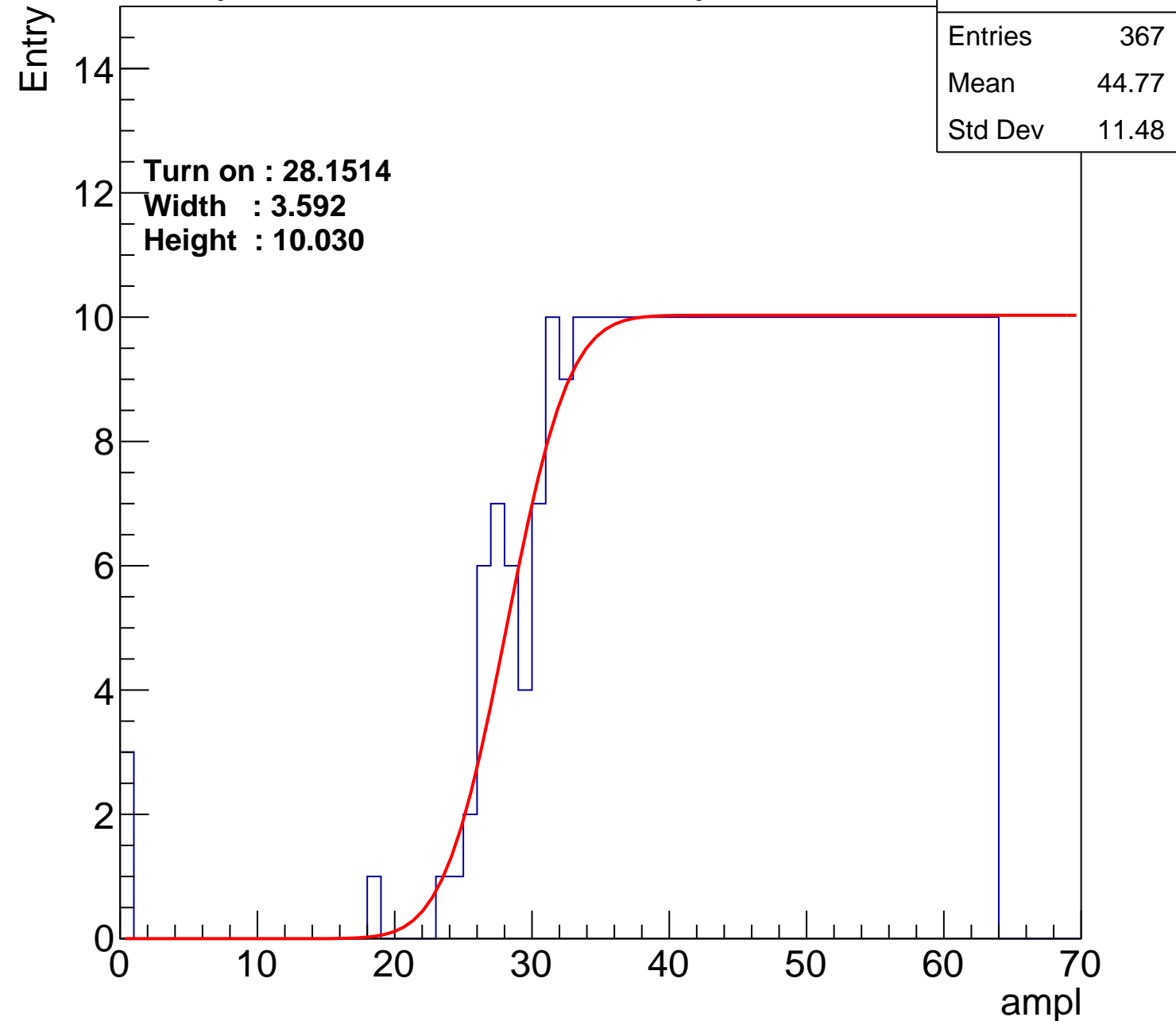
Width : 3.592

Height : 10.030

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch49

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	381
Mean	44.32
Std Dev	11.29

Turn on : 26.2418

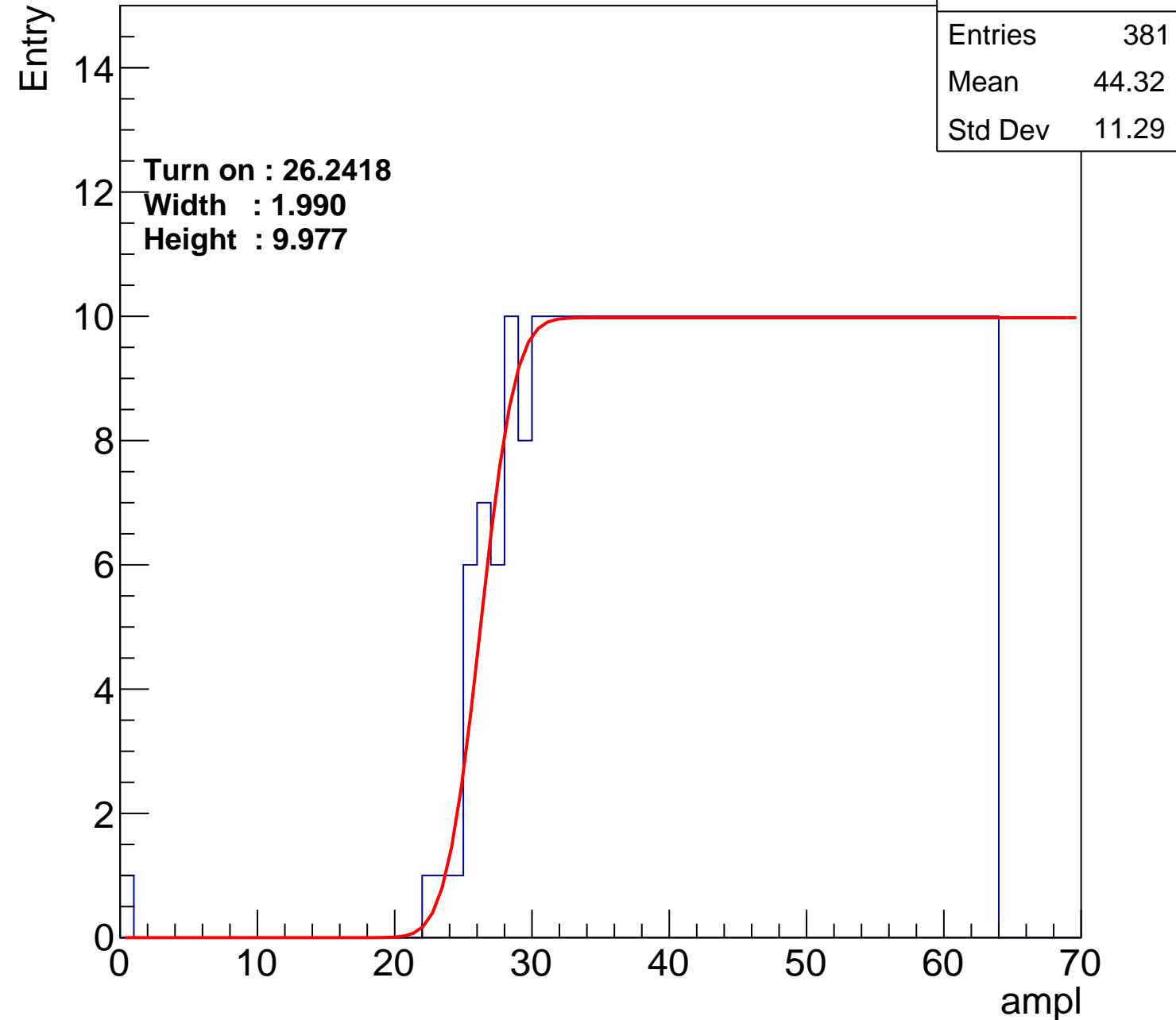
Width : 1.990

Height : 9.977

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch50

calib\_packv5\_042523\_0143.root, FC#5, port B1

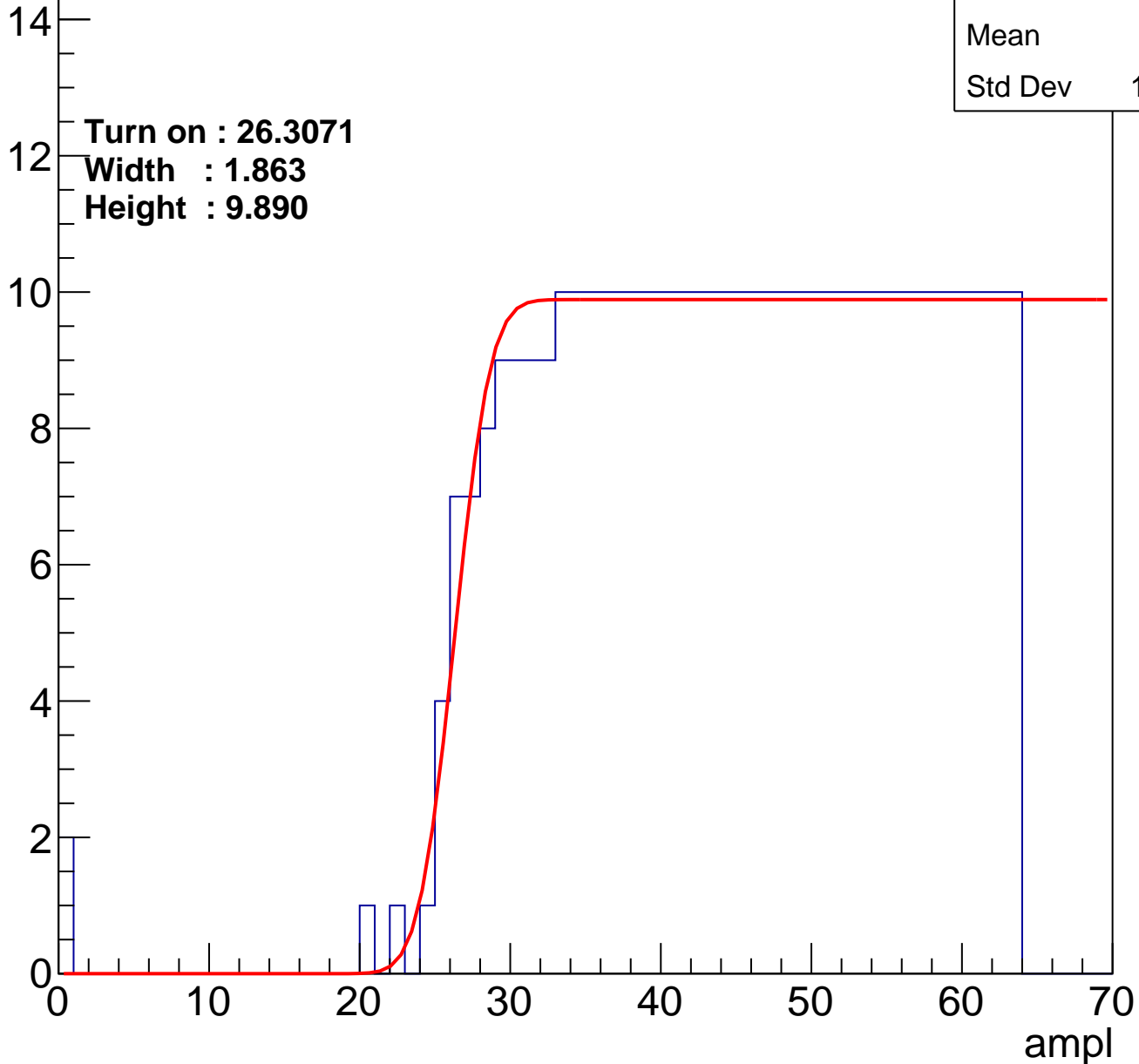
Entries	377
Mean	44.4
Std Dev	11.45

**Turn on : 26.3071**

**Width : 1.863**

**Height : 9.890**

Entry



# B0L000S, U4-ch51

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	357
Mean	45.32
Std Dev	11.04

Turn on : 28.7894

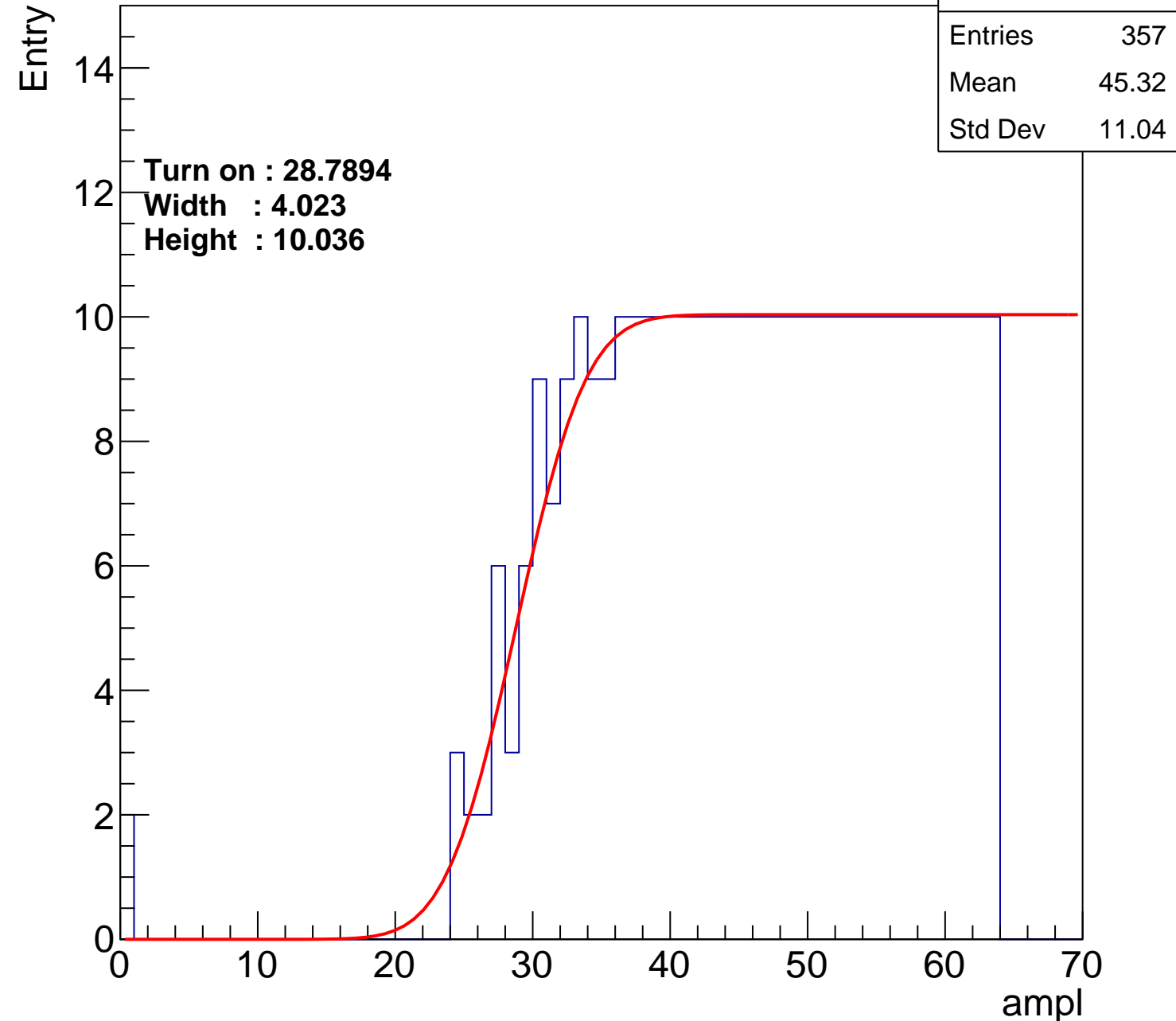
Width : 4.023

Height : 10.036

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch52

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	368
Mean	44.71
Std Dev	11.52

Turn on : 27.7718

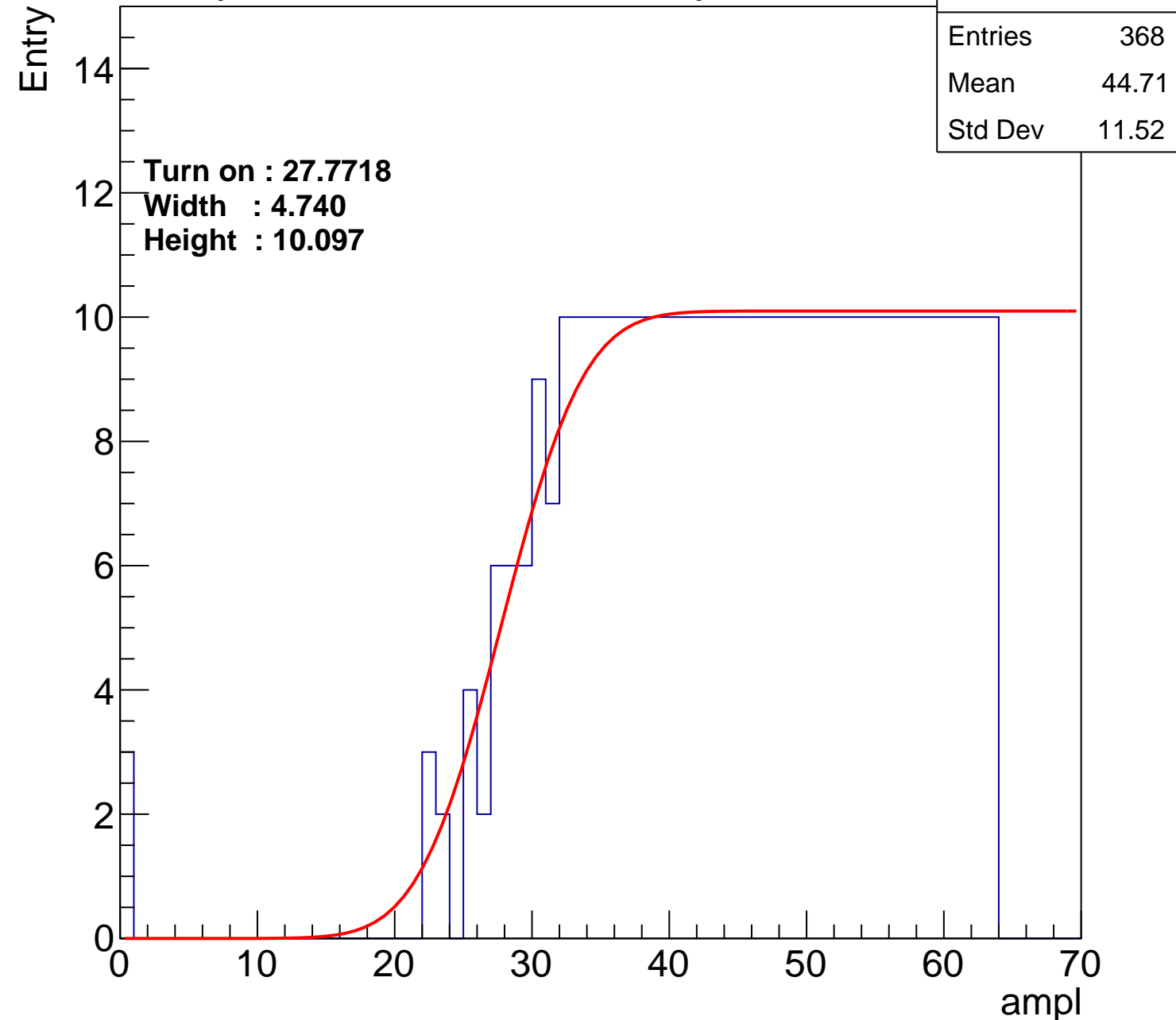
Width : 4.740

Height : 10.097

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch53

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	373
Mean	44.52
Std Dev	11.55

**Turn on : 27.7778**

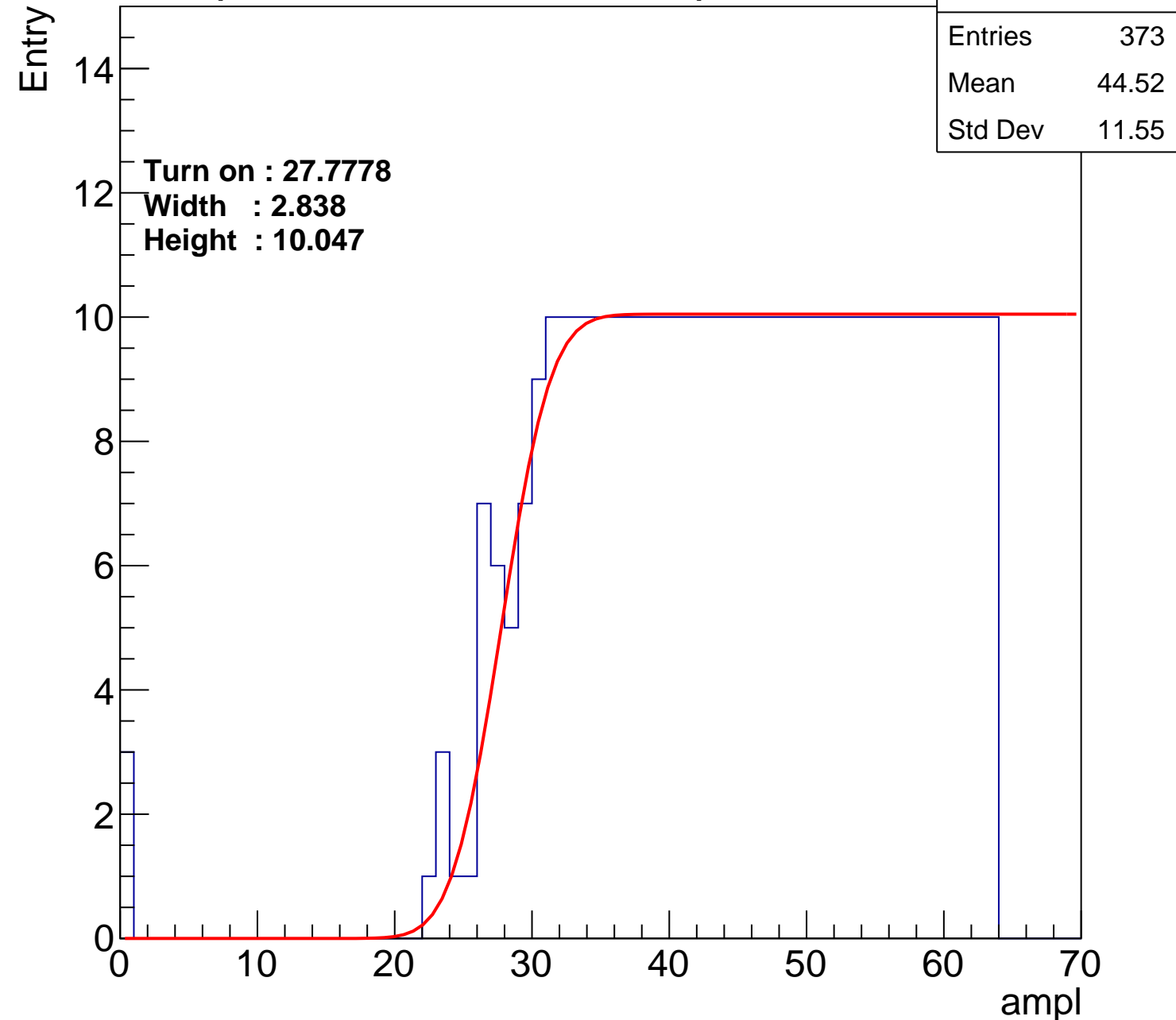
**Width : 2.838**

**Height : 10.047**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch54

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	370
Mean	44.49
Std Dev	12

Turn on : 27.7605

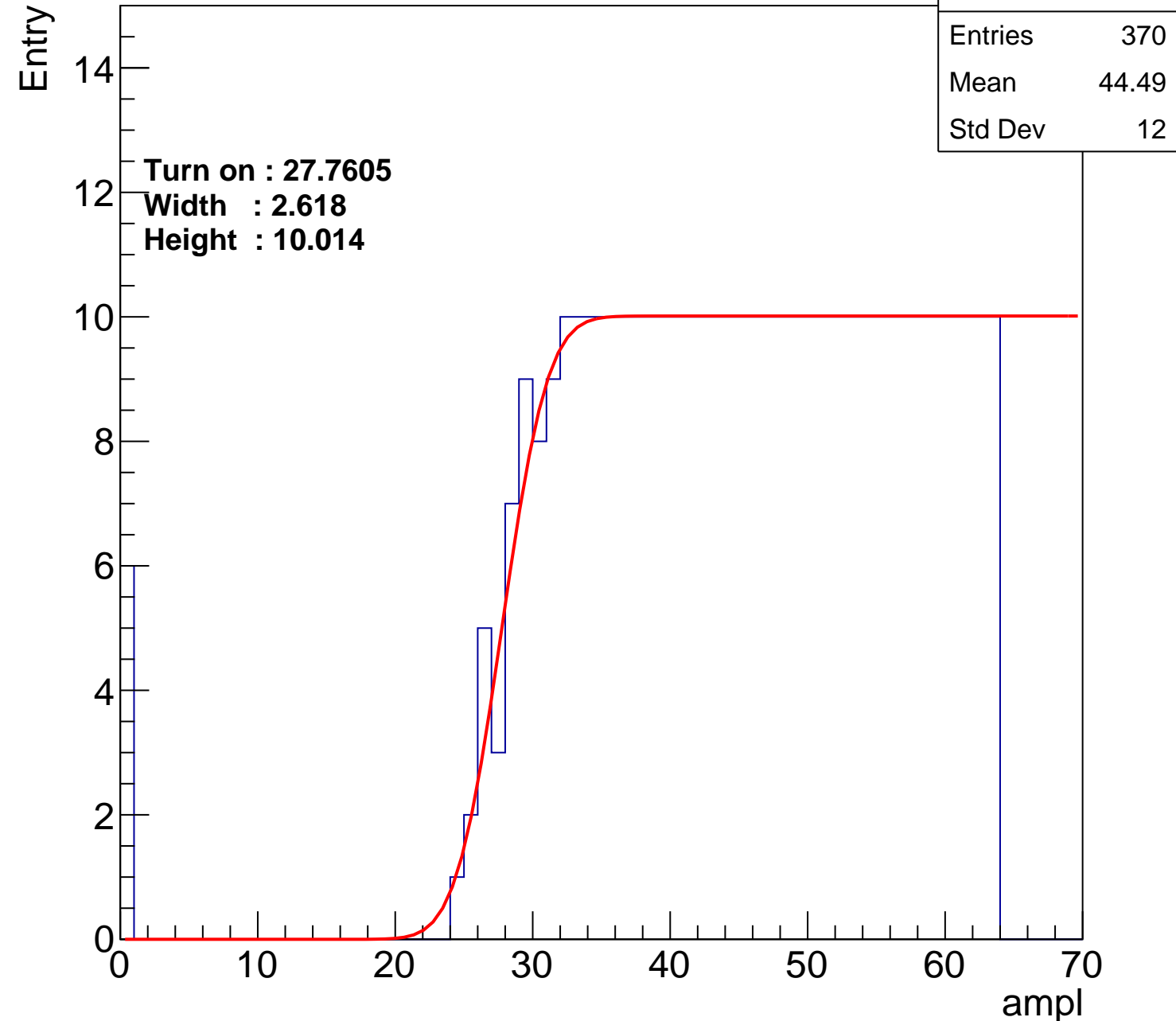
Width : 2.618

Height : 10.014

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L000S, U4-ch55

calib\_packv5\_042523\_0143.root, FC#5, port B1

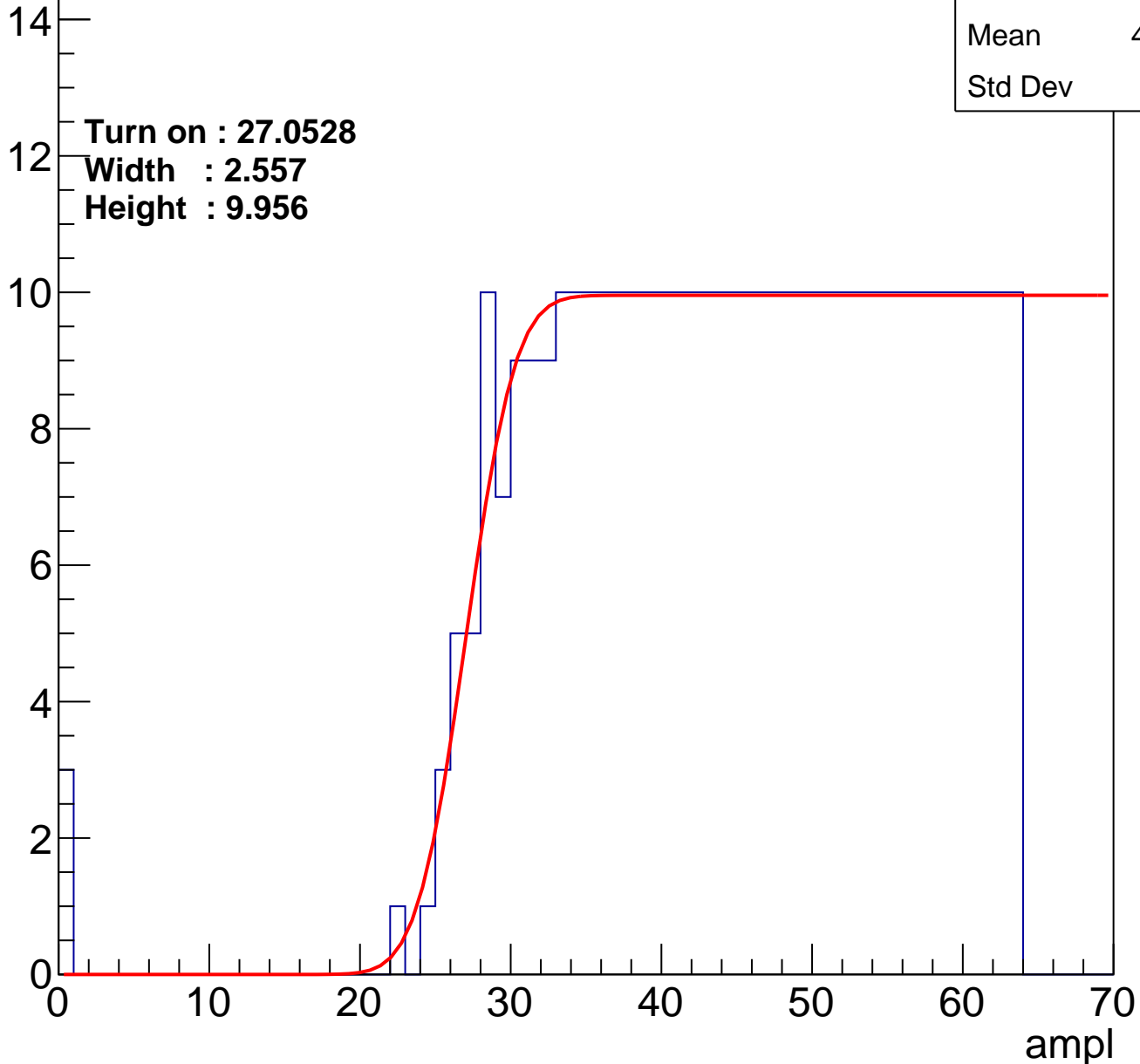
Entries	372
Mean	44.59
Std Dev	11.5

Turn on : 27.0528

Width : 2.557

Height : 9.956

Entry



# B0L000S, U4-ch56

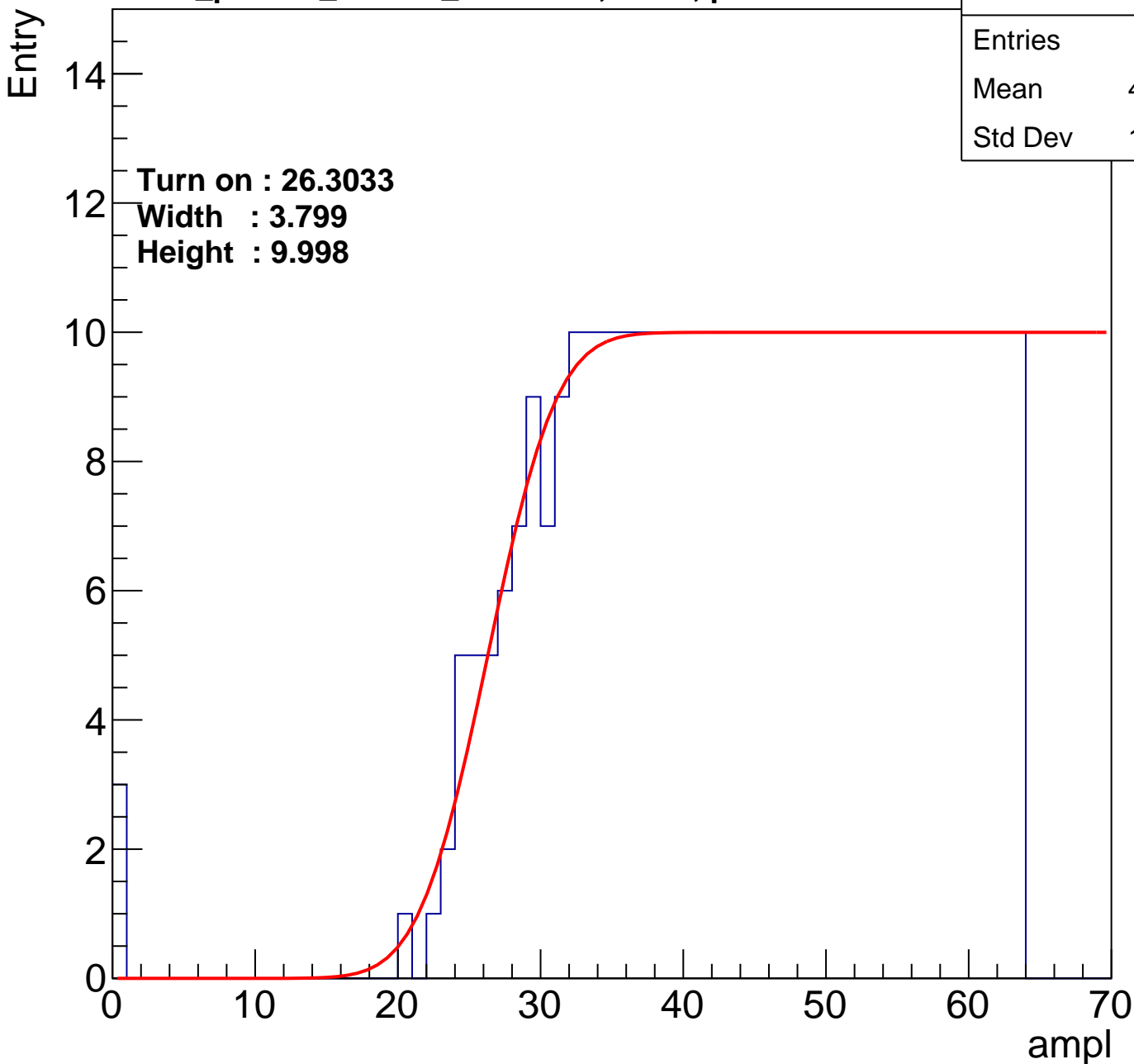
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	380
Mean	44.13
Std Dev	11.79

Turn on : 26.3033

Width : 3.799

Height : 9.998



# B0L000S, U4-ch57

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	376
Mean	44.48
Std Dev	11.29

**Turn on : 26.0903**

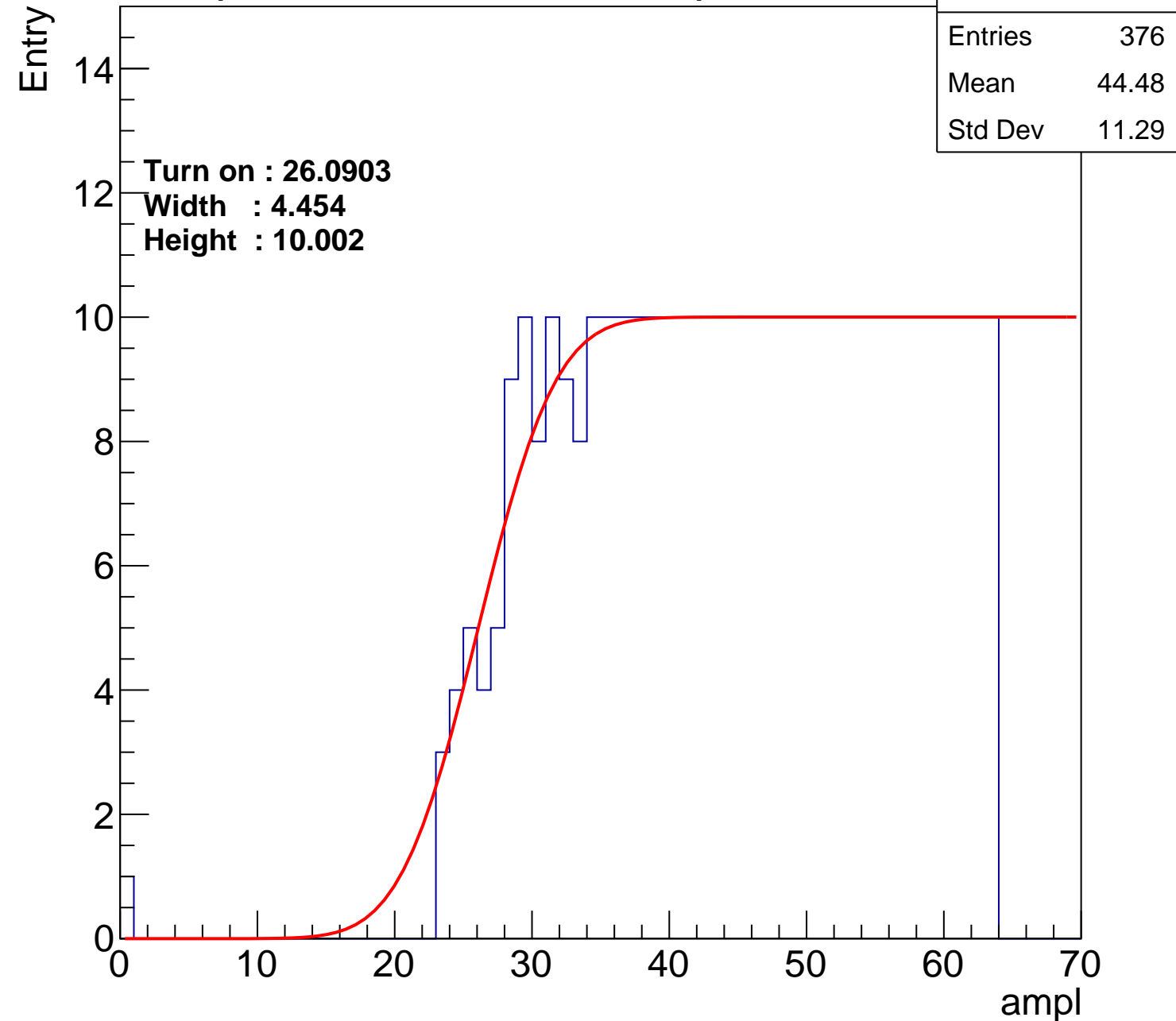
**Width : 4.454**

**Height : 10.002**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch58

calib\_packv5\_042523\_0143.root, FC#5, port B1

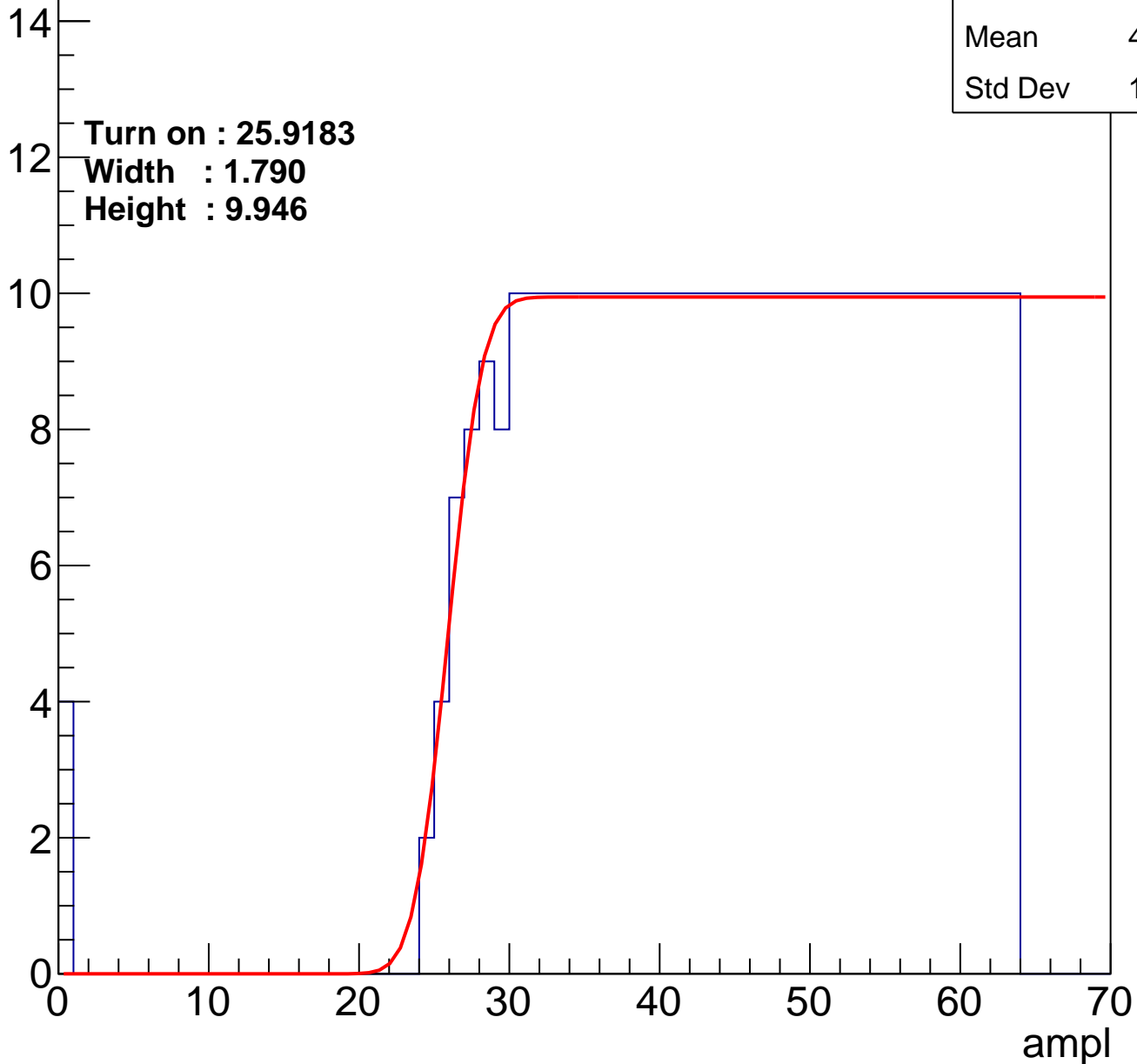
Entry

Entries	382
Mean	44.08
Std Dev	11.84

Turn on : 25.9183

Width : 1.790

Height : 9.946



# B0L000S, U4-ch59

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	360
Mean	45.27
Std Dev	10.88

Turn on : 29.4118

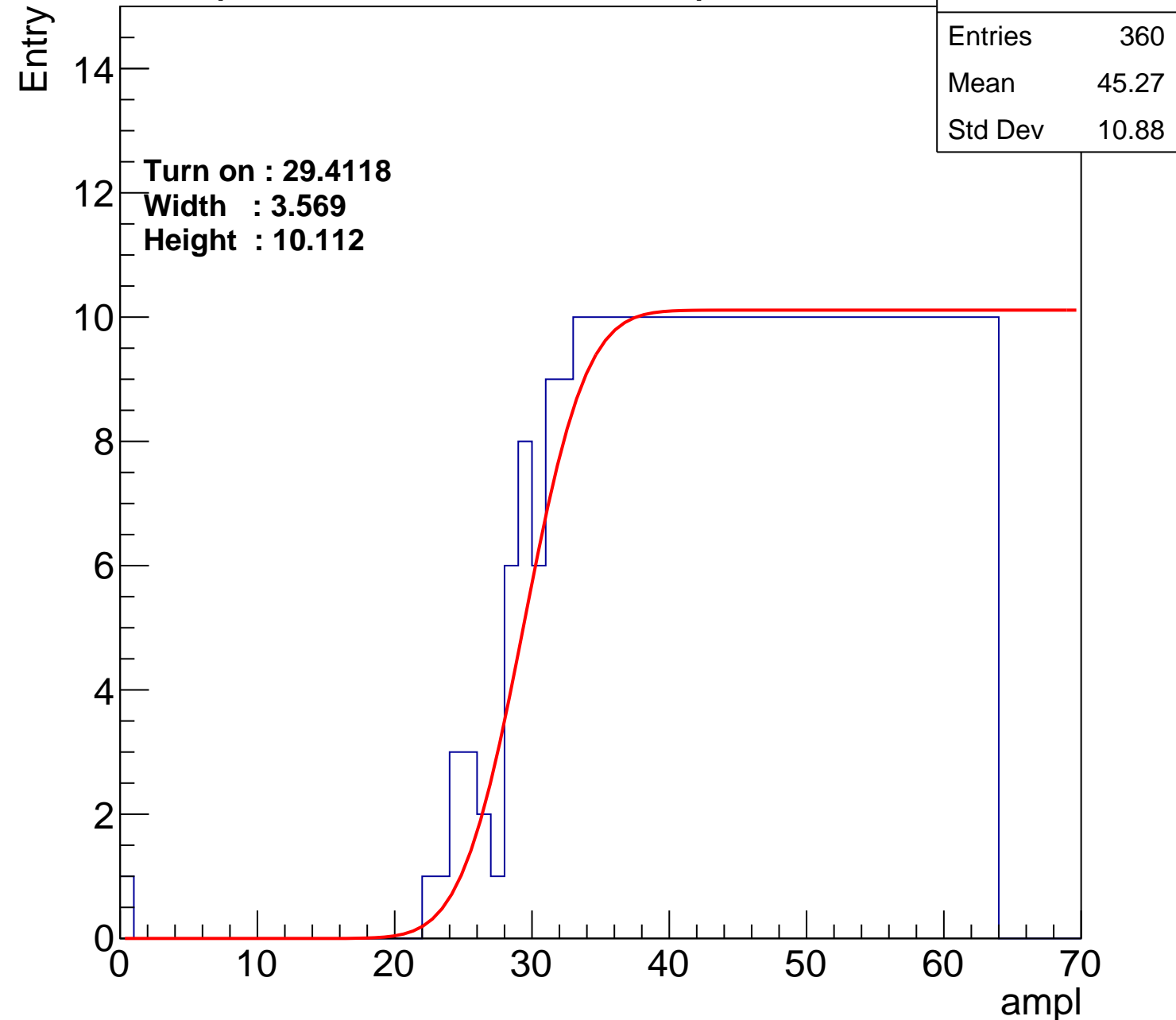
Width : 3.569

Height : 10.112

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch60

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	375
Mean	44.35
Std Dev	11.78

Turn on : 27.1851

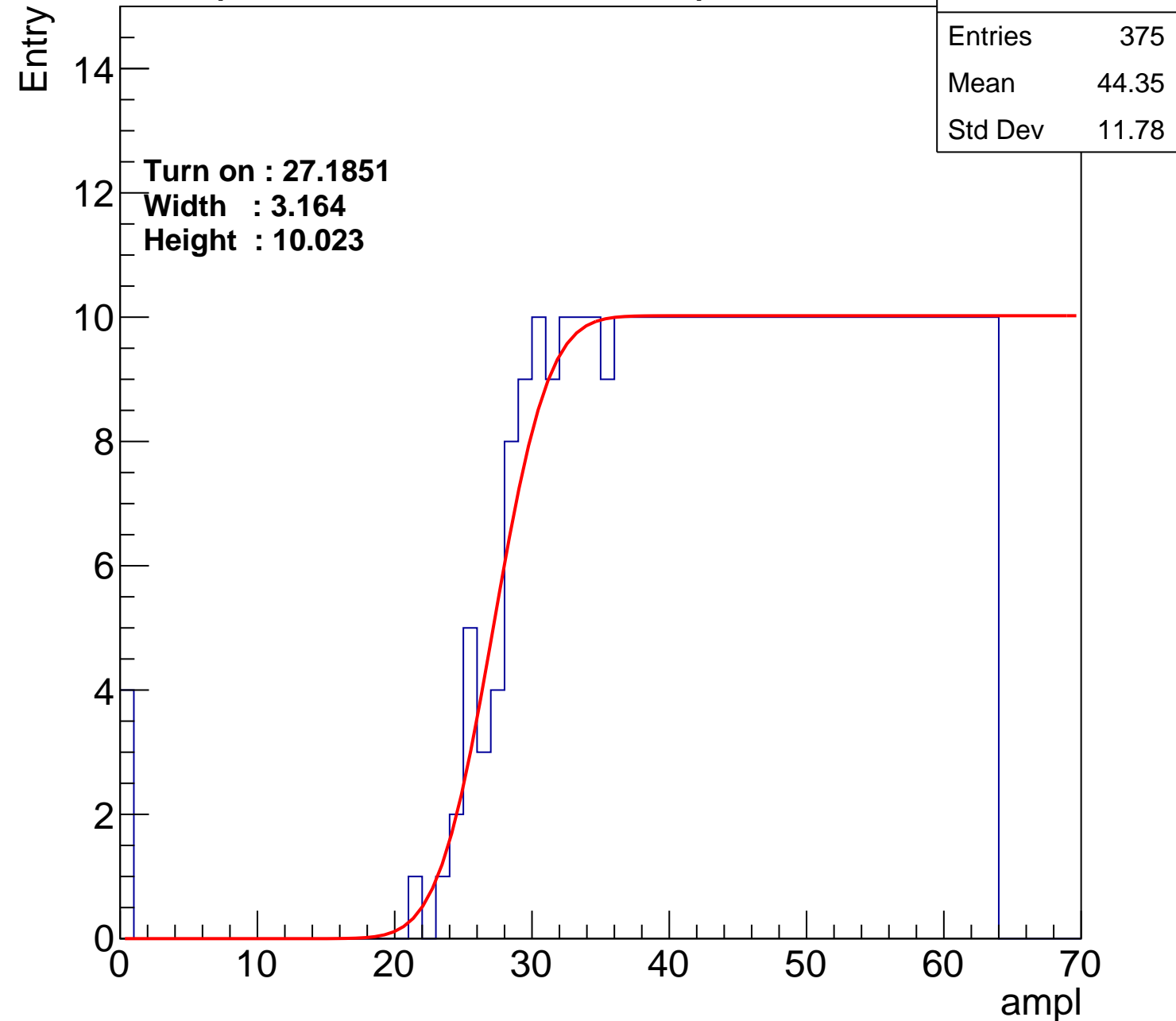
Width : 3.164

Height : 10.023

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch61

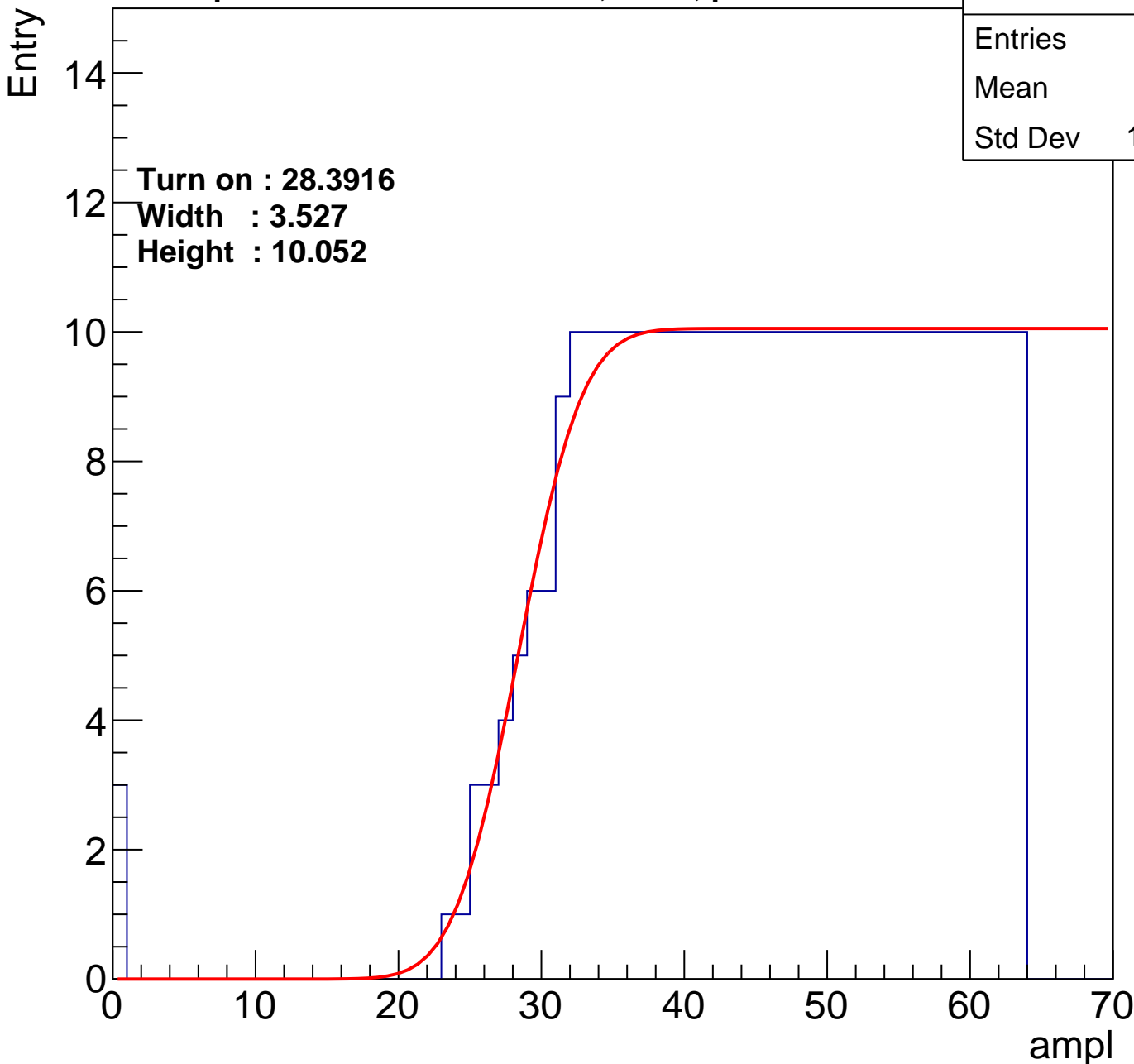
**calib\_packv5\_042523\_0143.root, FC#5, port B1**

Entries	361
Mean	45.1
Std Dev	11.28

**Turn on : 28.3916**

**Width : 3.527**

**Height : 10.052**



# B0L000S, U4-ch62

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	374
Mean	44.55
Std Dev	11.38

Turn on : 26.9207

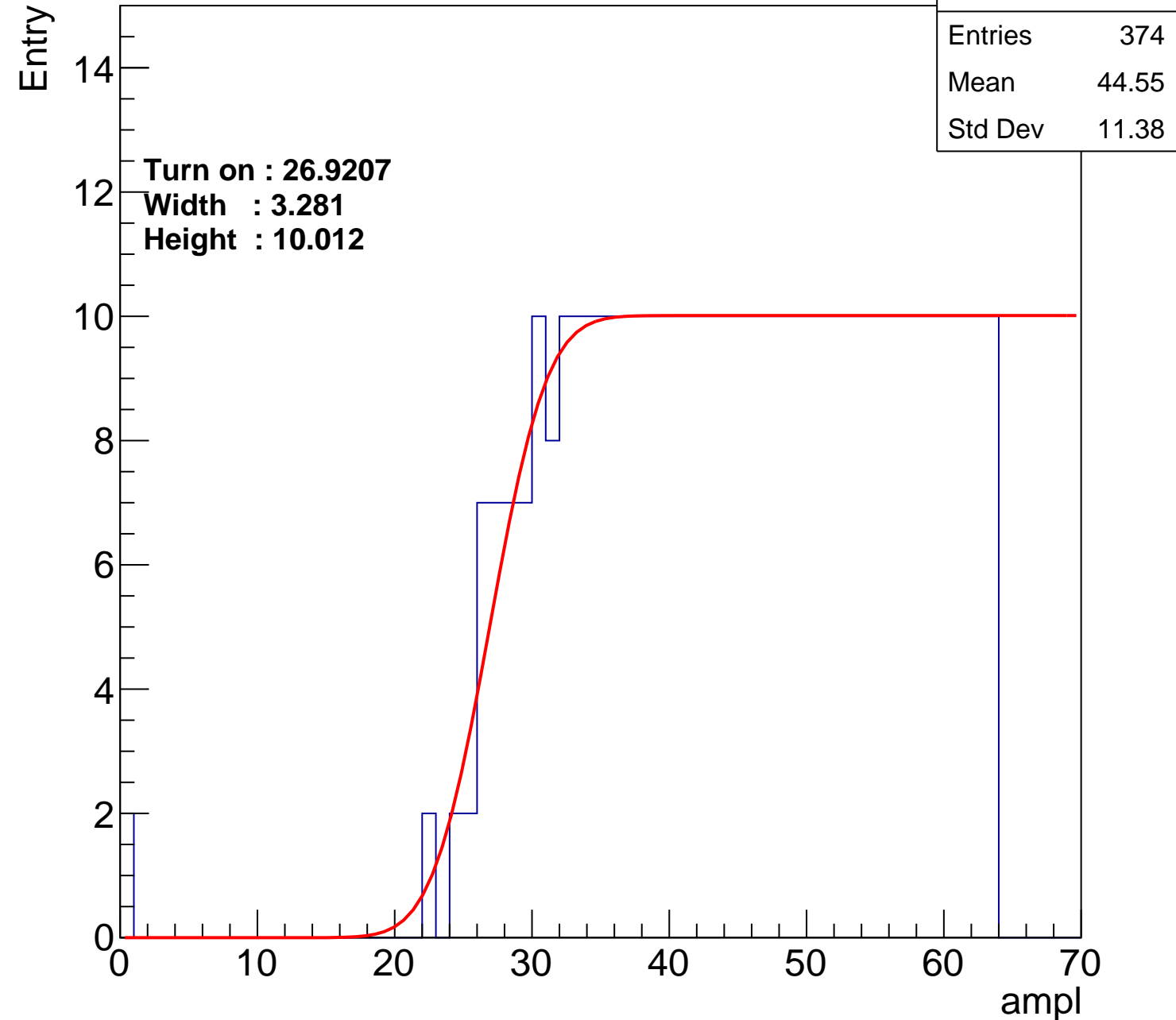
Width : 3.281

Height : 10.012

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L000S, U4-ch63

calib\_packv5\_042523\_0143.root, FC#5, port B1

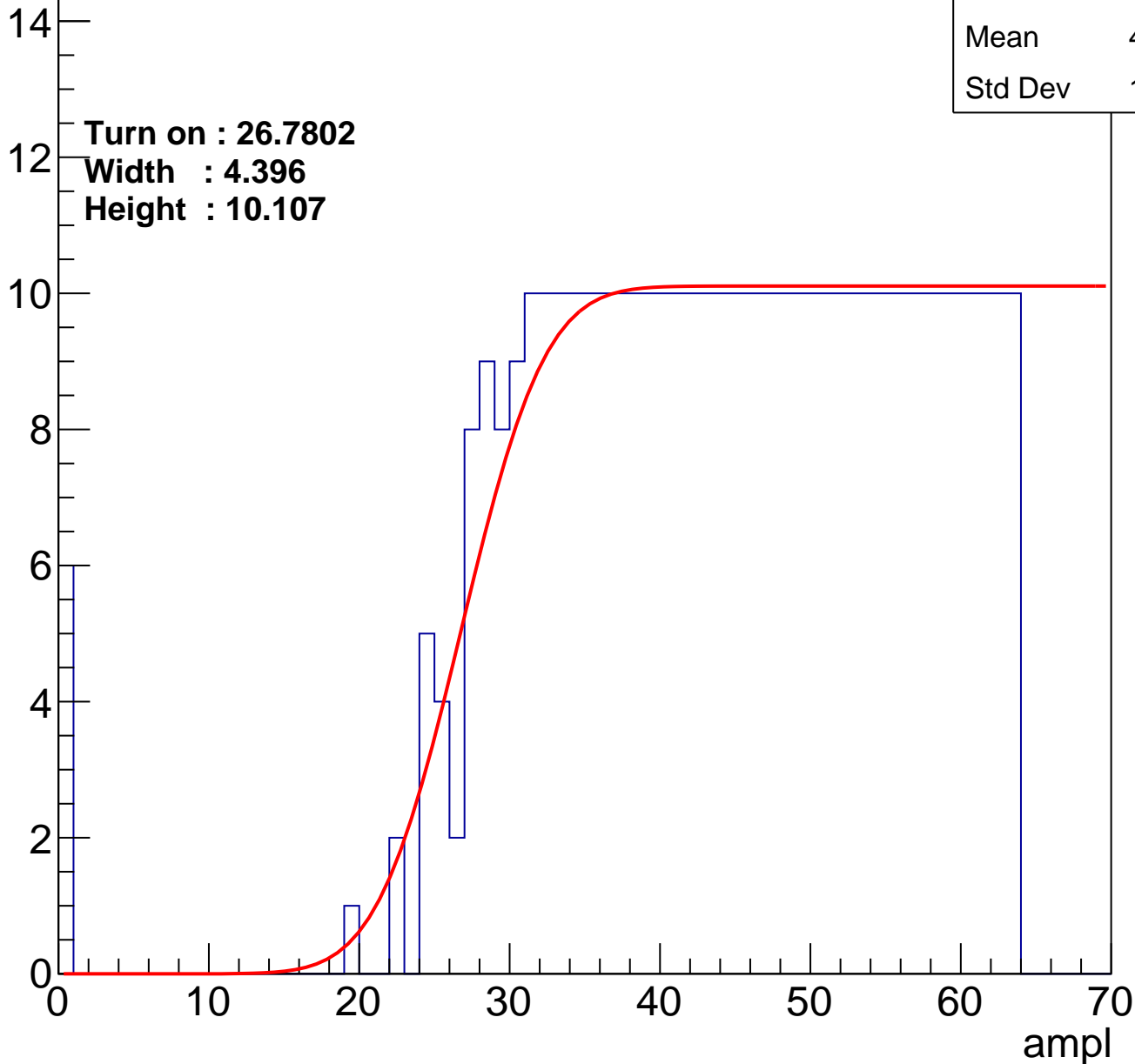
Entry

Entries	384
Mean	43.79
Std Dev	12.33

**Turn on : 26.7802**

**Width : 4.396**

**Height : 10.107**



# B0L000S, U4-ch64

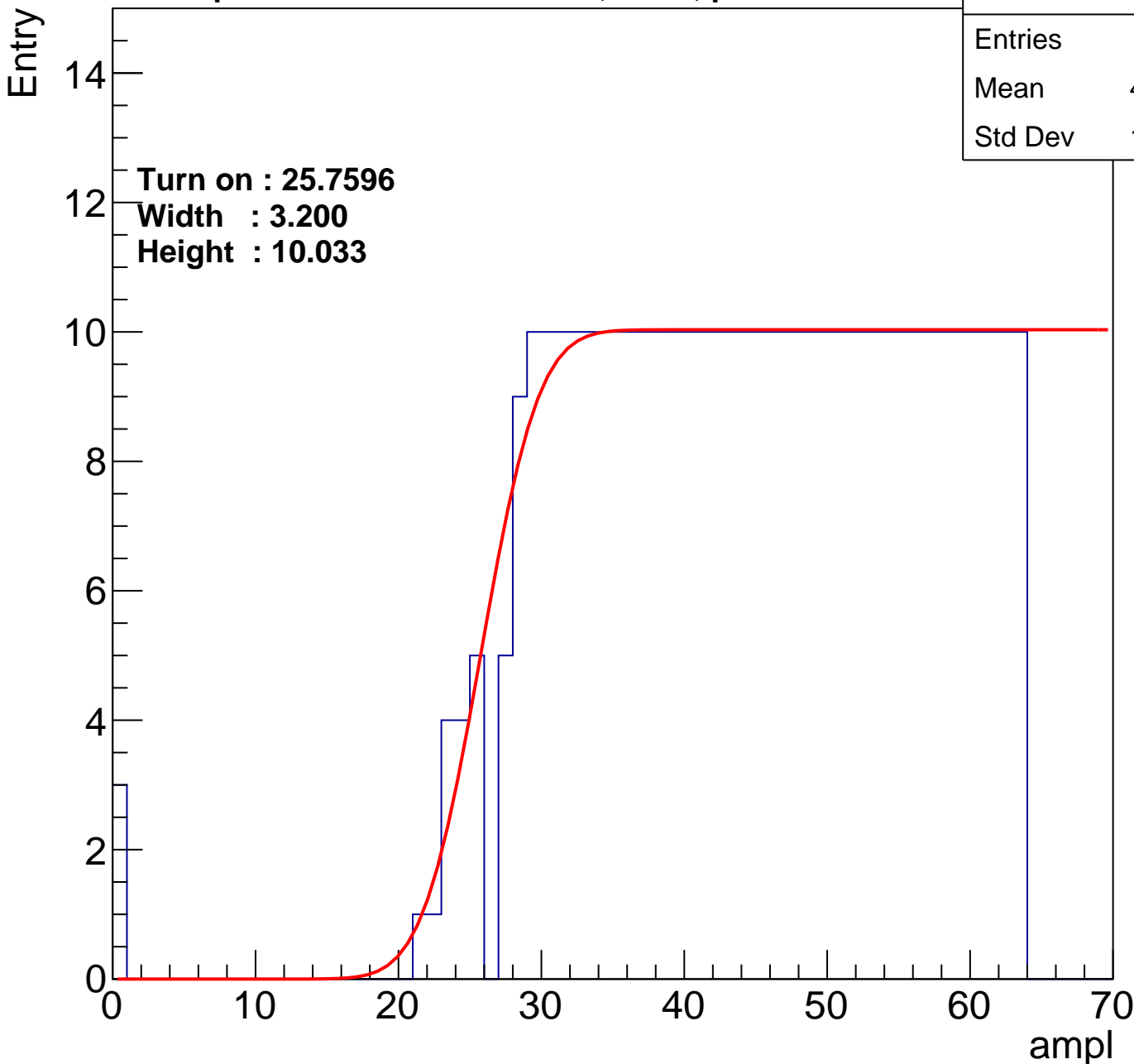
**calib\_packv5\_042523\_0143.root, FC#5, port B1**

Entries	382
Mean	44.09
Std Dev	11.76

**Turn on : 25.7596**

**Width : 3.200**

**Height : 10.033**



# B0L000S, U4-ch65

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	370
Mean	44.72
Std Dev	11.32

Turn on : 27.8553

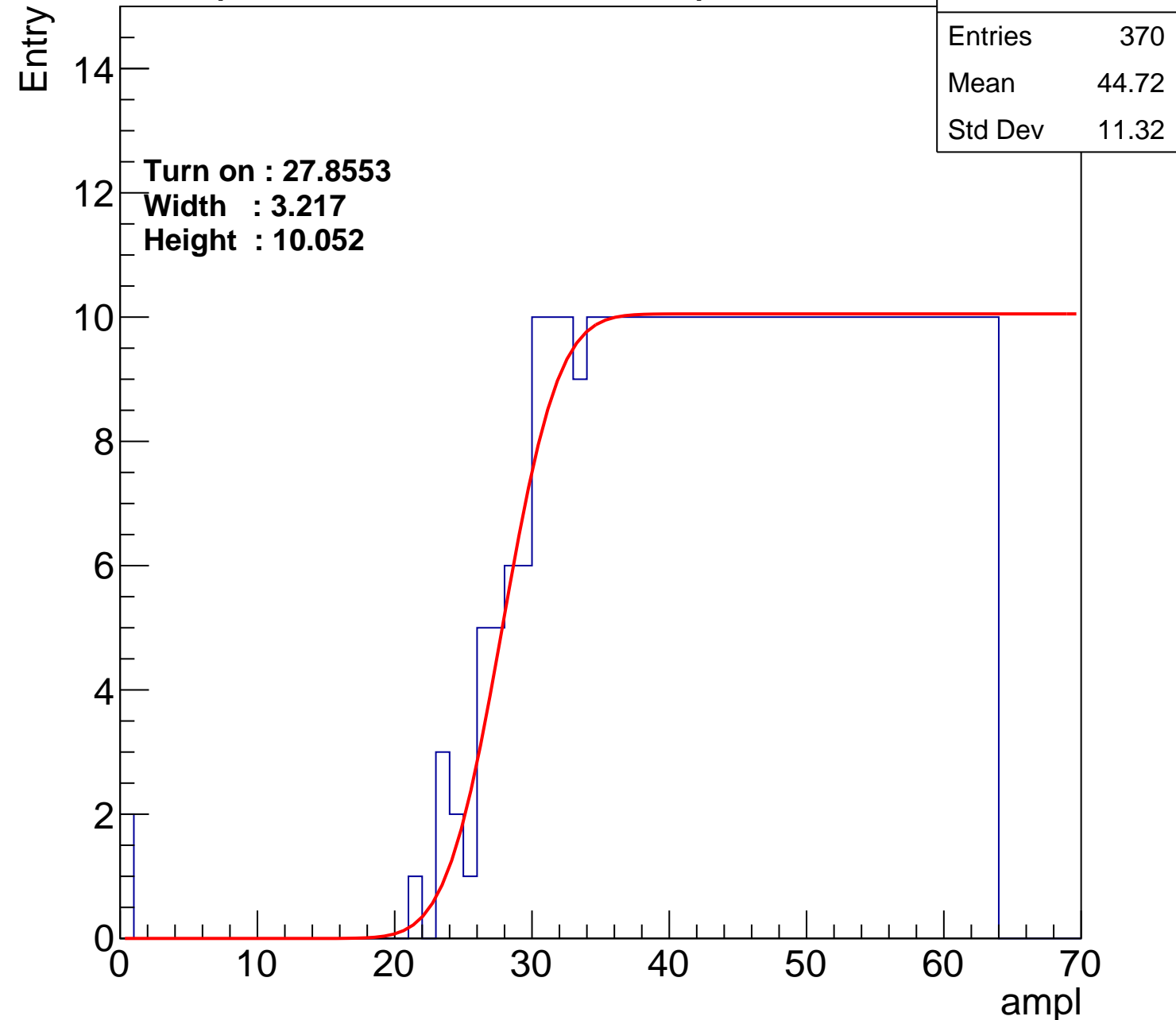
Width : 3.217

Height : 10.052

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch66

calib\_packv5\_042523\_0143.root, FC#5, port B1

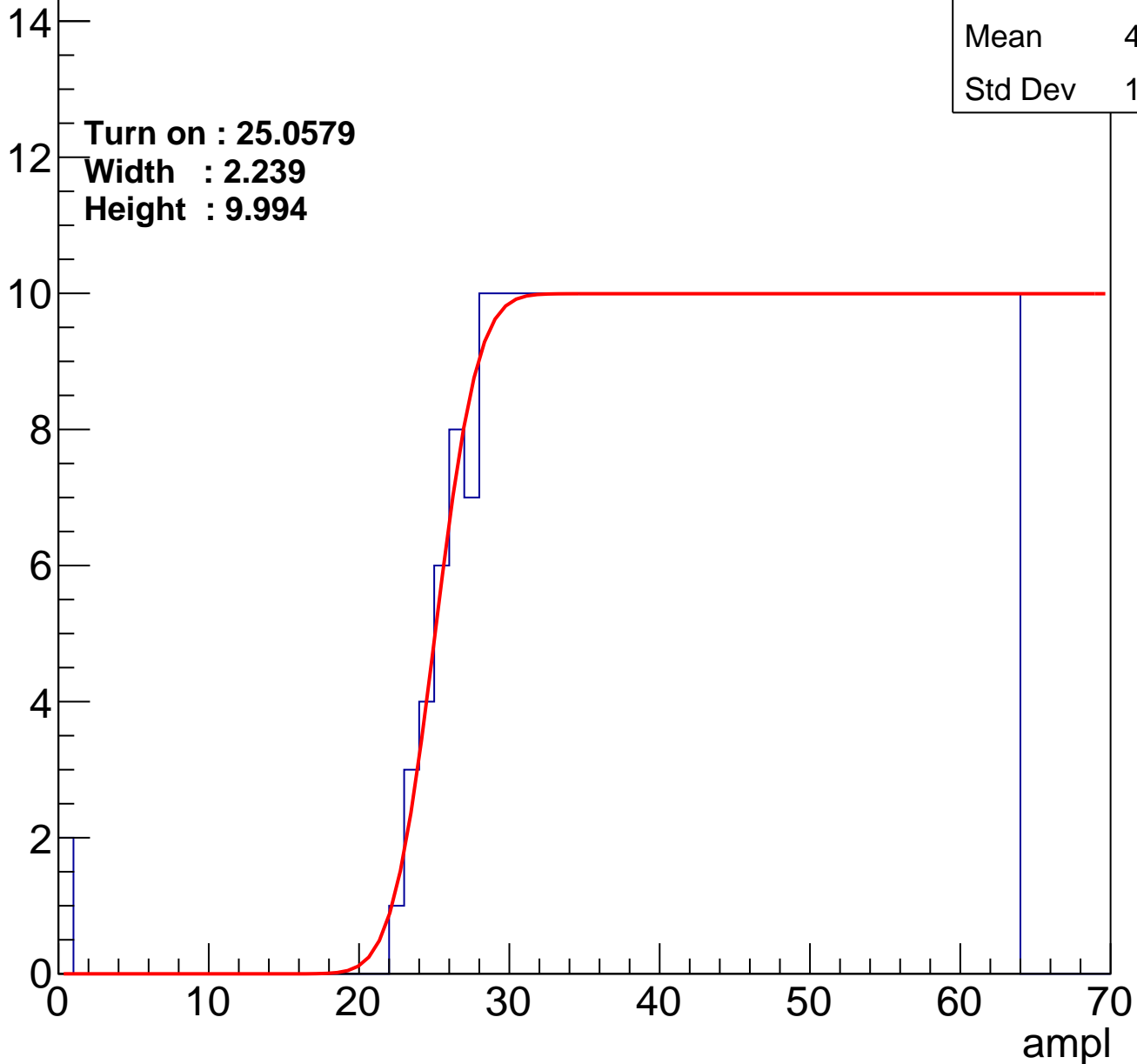
Entries	391
Mean	43.77
Std Dev	11.72

Turn on : 25.0579

Width : 2.239

Height : 9.994

Entry



# B0L000S, U4-ch67

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	350
Mean	45.74
Std Dev	10.76

Turn on : 29.2342

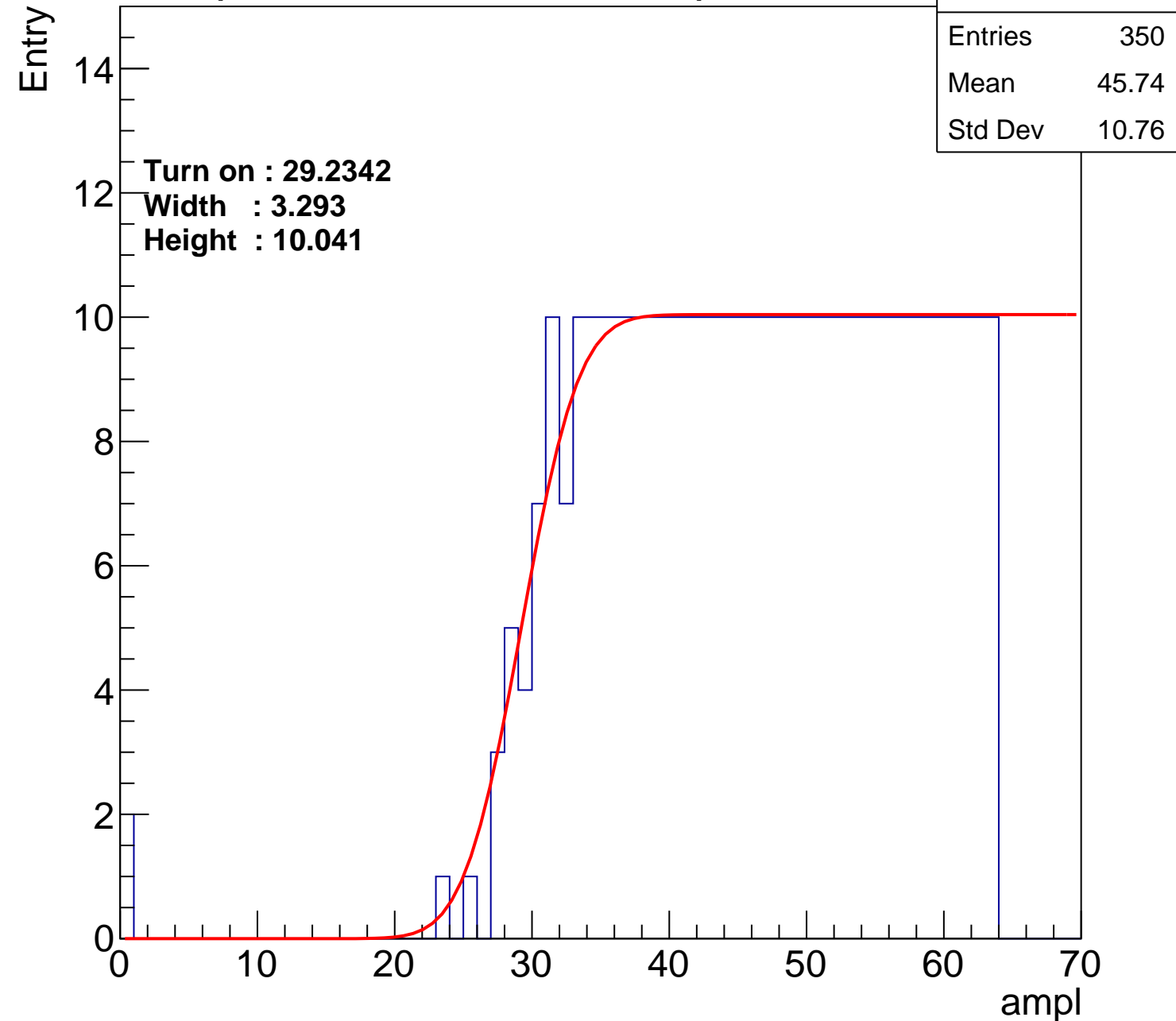
Width : 3.293

Height : 10.041

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch68

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	358
Mean	45.3
Std Dev	11.03

**Turn on : 28.4508**

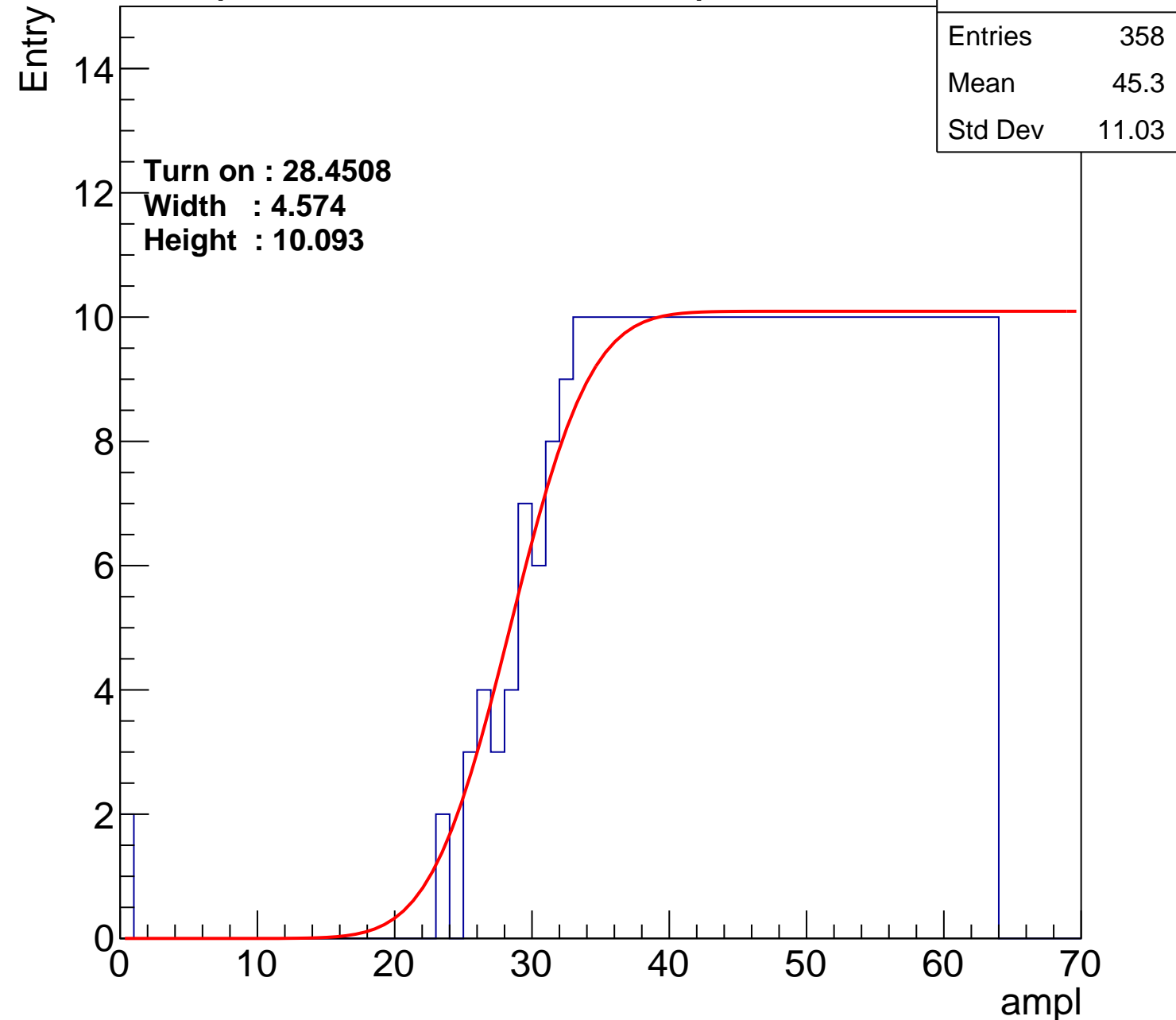
**Width : 4.574**

**Height : 10.093**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch69

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	365
Mean	45.01
Std Dev	11.13

**Turn on : 27.9400**

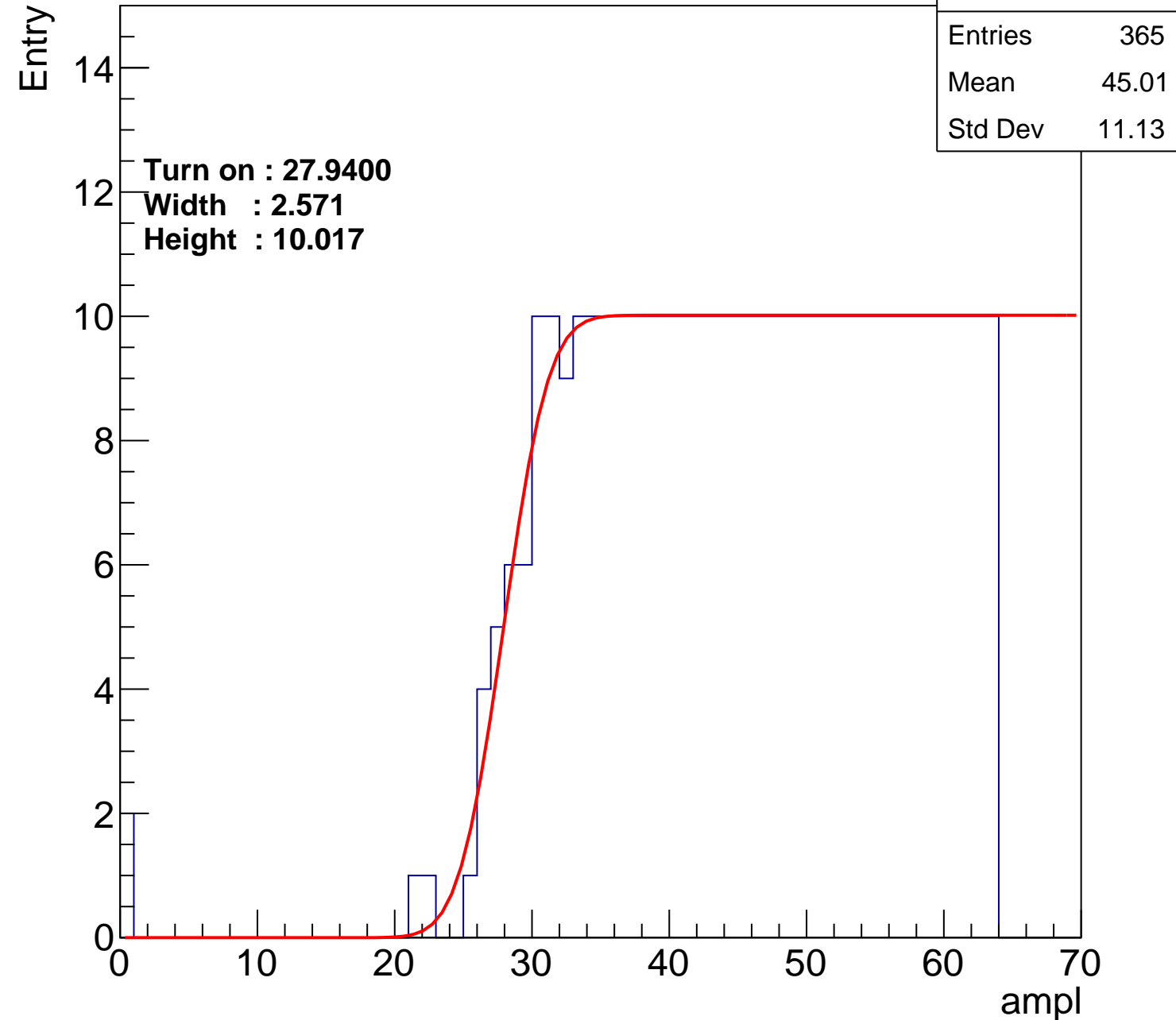
**Width : 2.571**

**Height : 10.017**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch70

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	389
Mean	43.69
Std Dev	12.09

**Turn on : 25.8294**

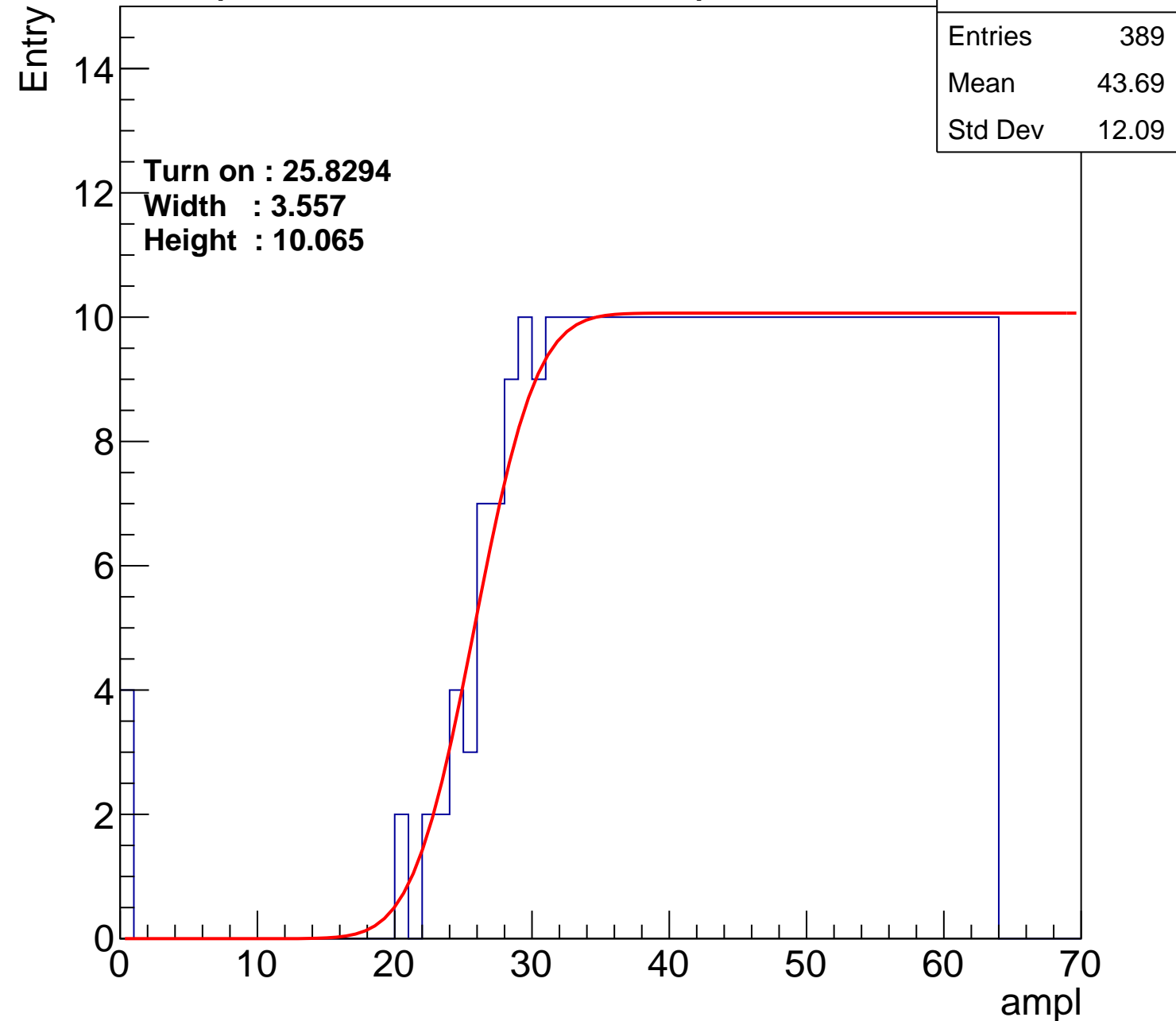
**Width : 3.557**

**Height : 10.065**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L000S, U4-ch71

calib\_packv5\_042523\_0143.root, FC#5, port B1

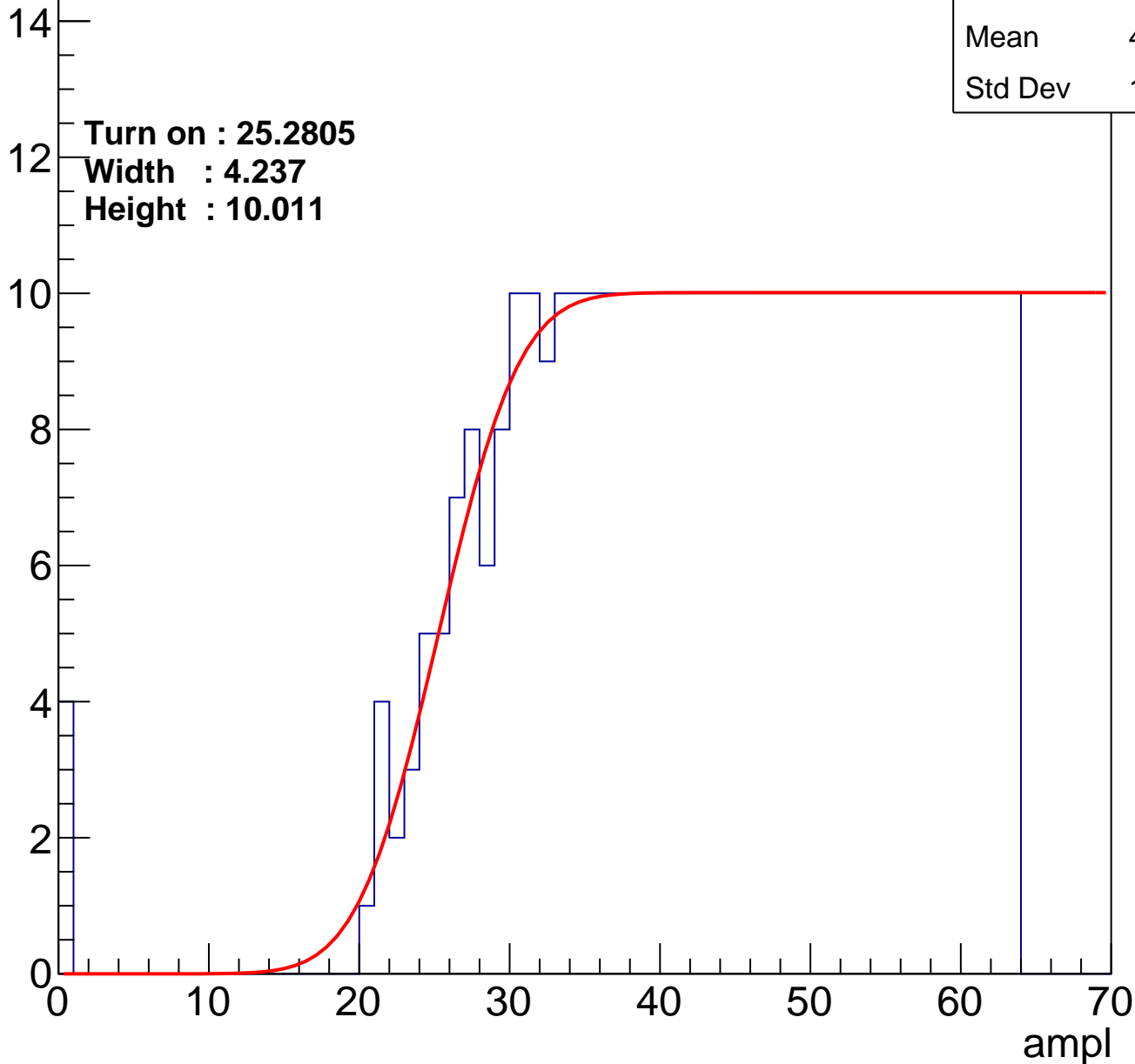
Entries	392
Mean	43.46
Std Dev	12.27

Turn on : 25.2805

Width : 4.237

Height : 10.011

Entry



# B0L000S, U4-ch72

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	374
Mean	44.55
Std Dev	11.38

Turn on : 27.0191

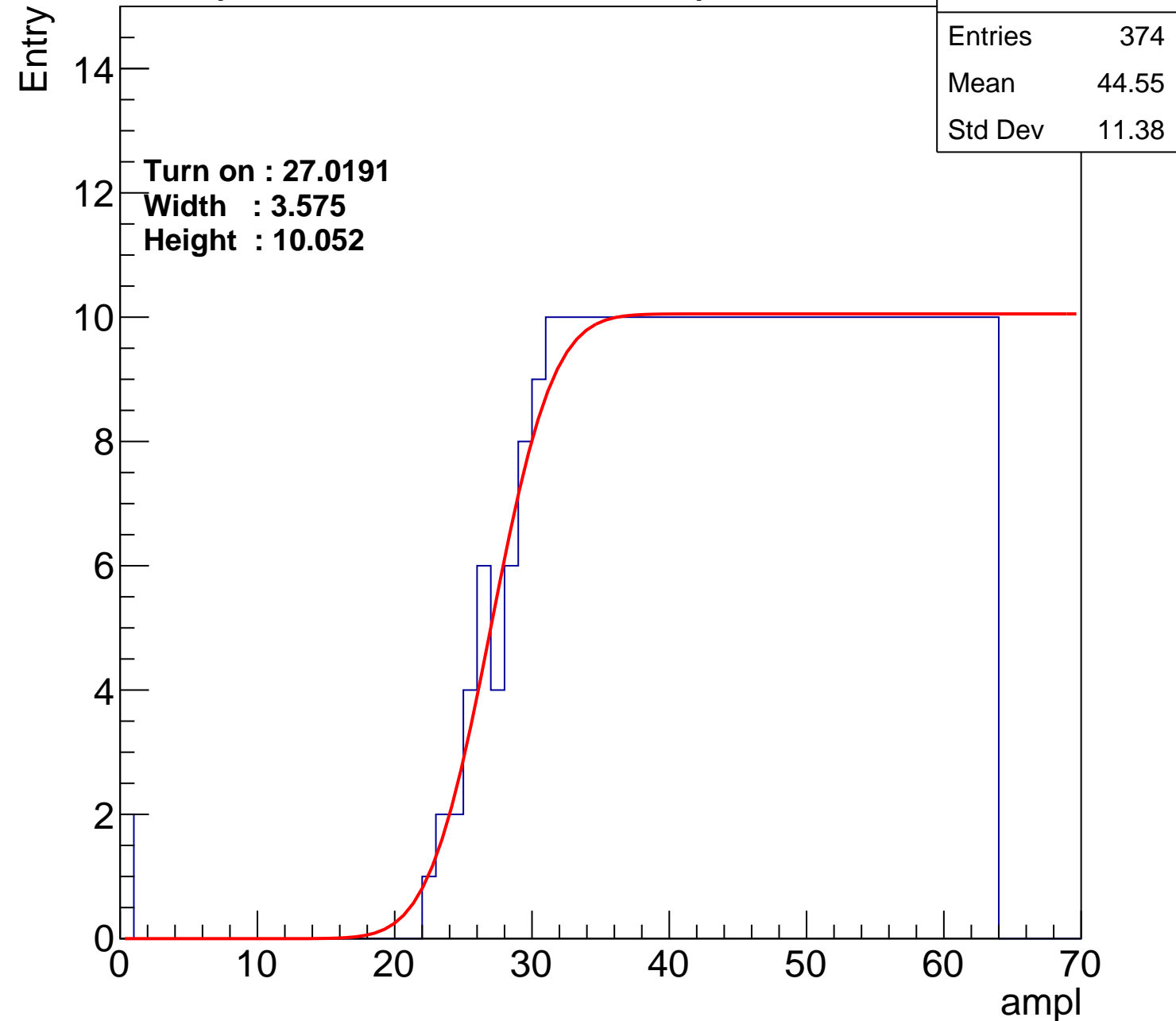
Width : 3.575

Height : 10.052

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch73

calib\_packv5\_042523\_0143.root, FC#5, port B1

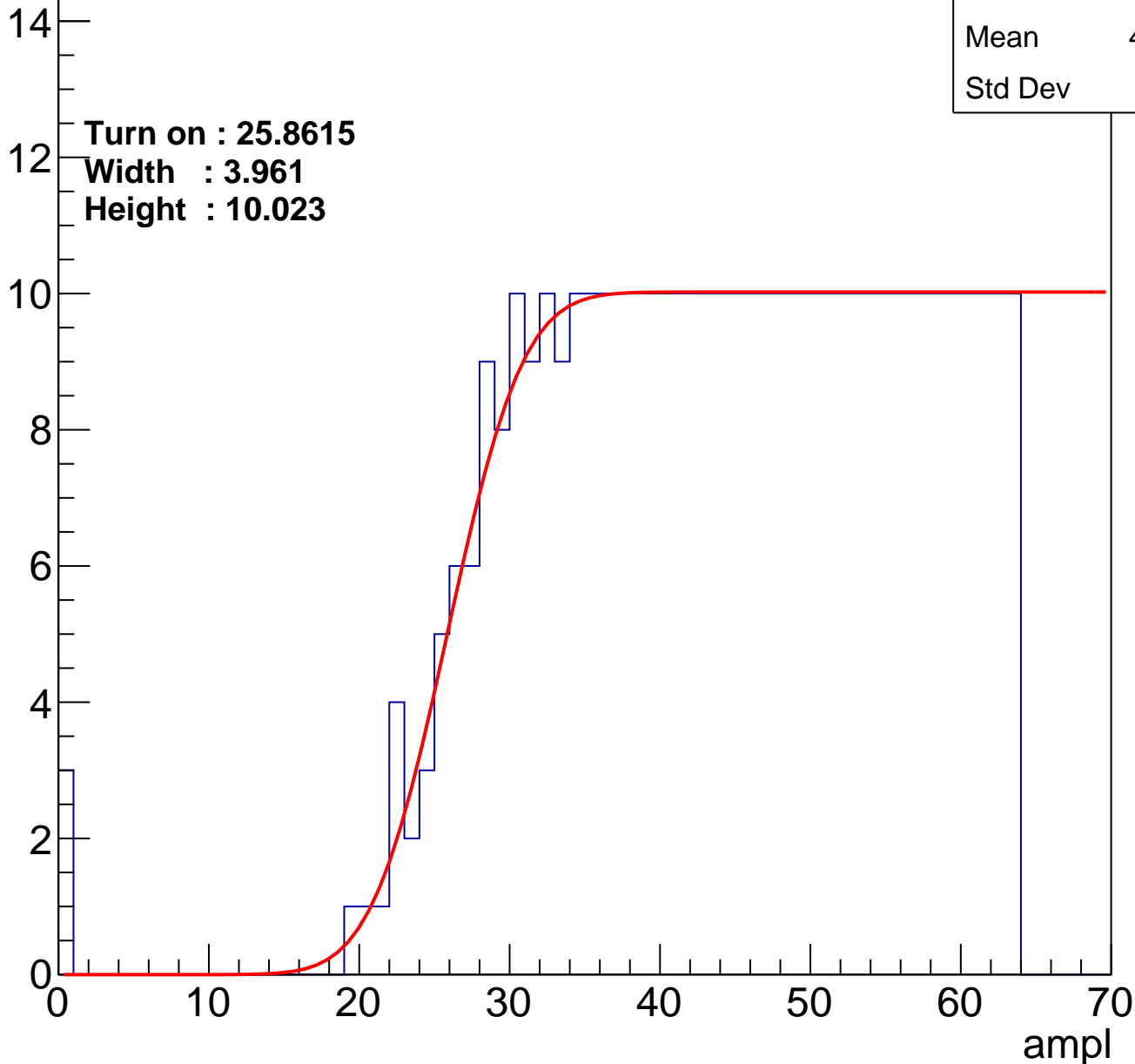
Entry

Entries	387
Mean	43.77
Std Dev	12

Turn on : 25.8615

Width : 3.961

Height : 10.023



# B0L000S, U4-ch74

calib\_packv5\_042523\_0143.root, FC#5, port B1

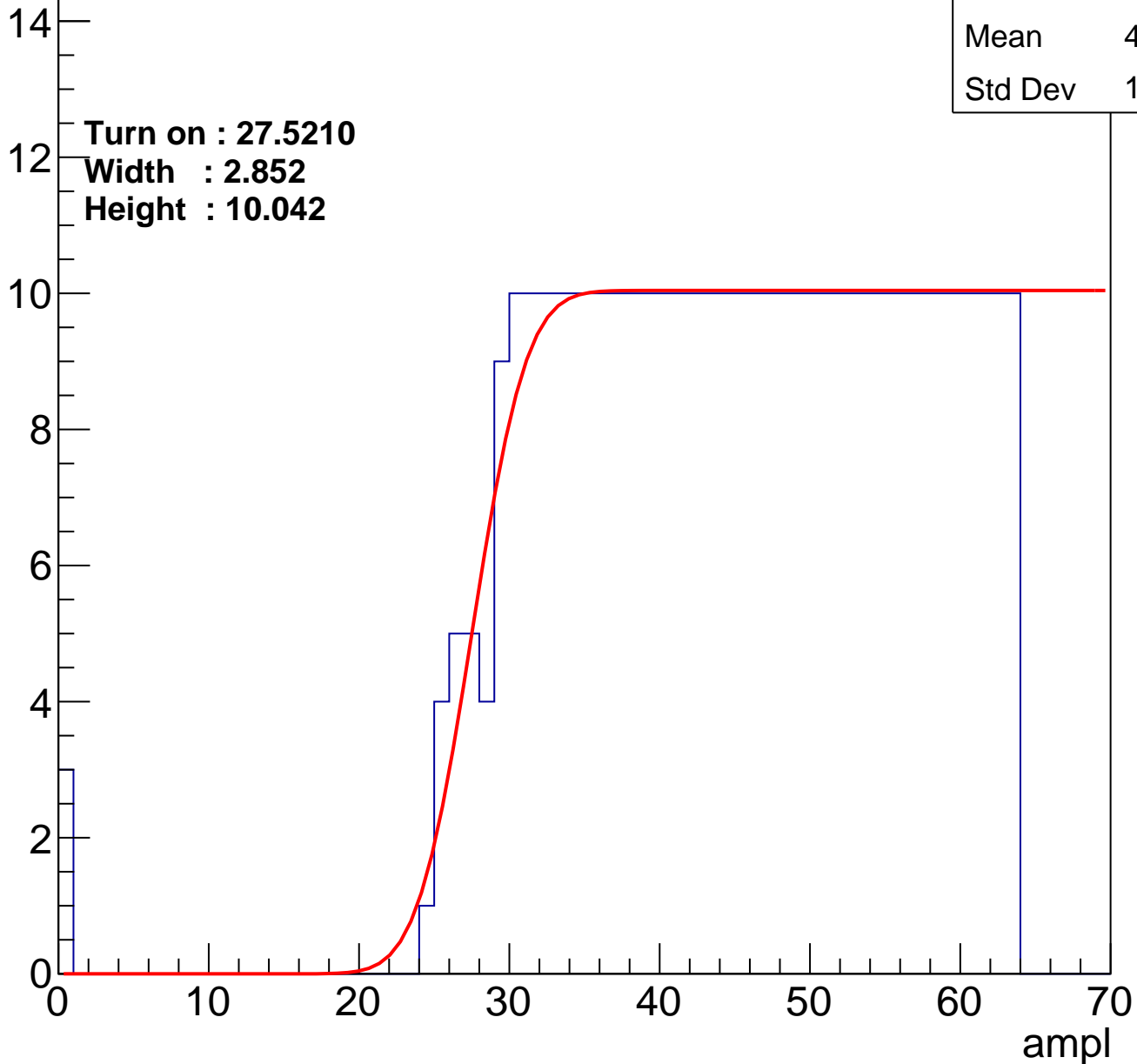
Entries	371
Mean	44.67
Std Dev	11.43

Turn on : 27.5210

Width : 2.852

Height : 10.042

Entry



# B0L000S, U4-ch75

calib\_packv5\_042523\_0143.root, FC#5, port B1

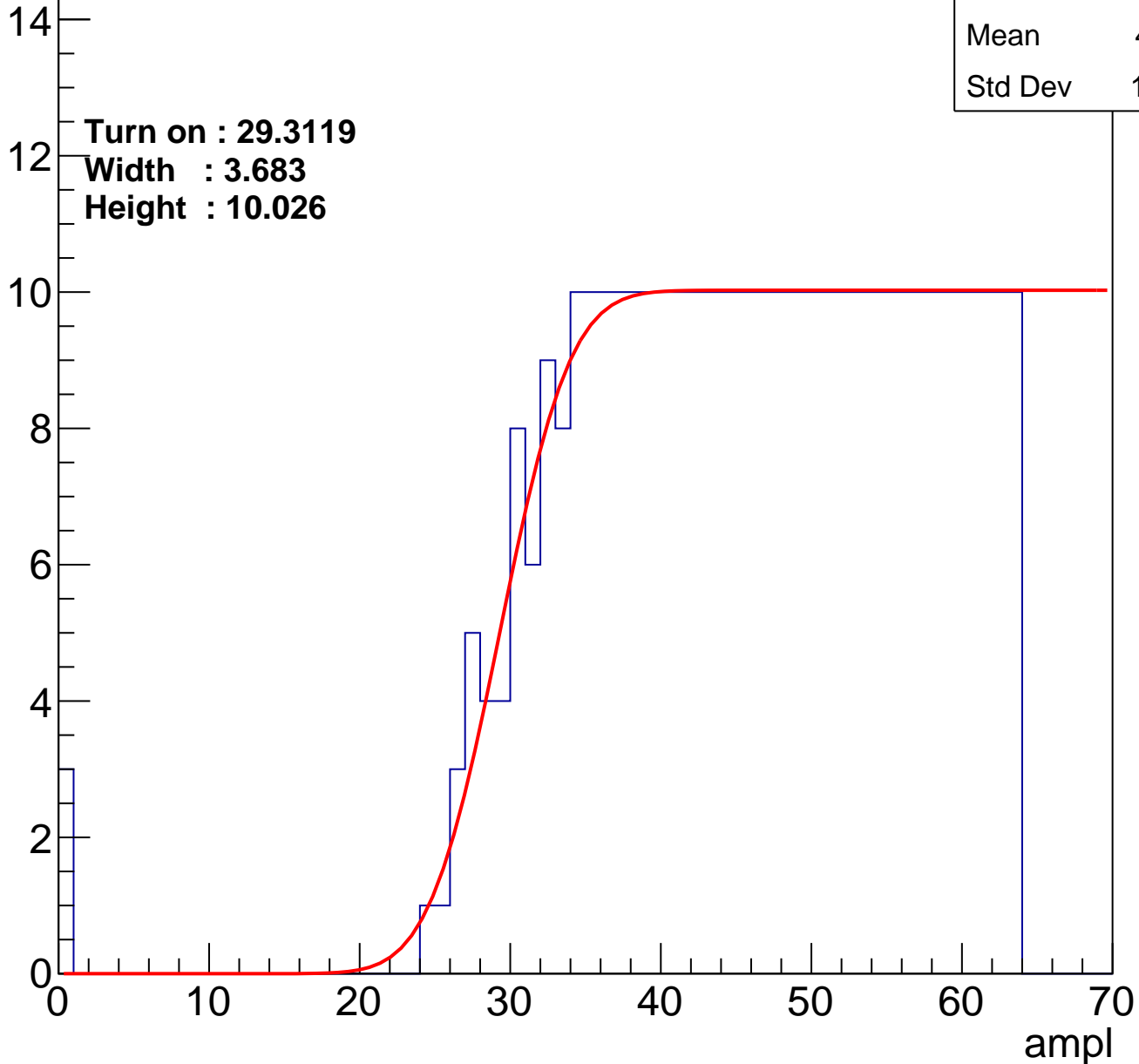
Entries	352
Mean	45.51
Std Dev	11.12

Turn on : 29.3119

Width : 3.683

Height : 10.026

Entry



# B0L000S, U4-ch76

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	383
Mean	44.11
Std Dev	11.6

**Turn on : 26.2495**

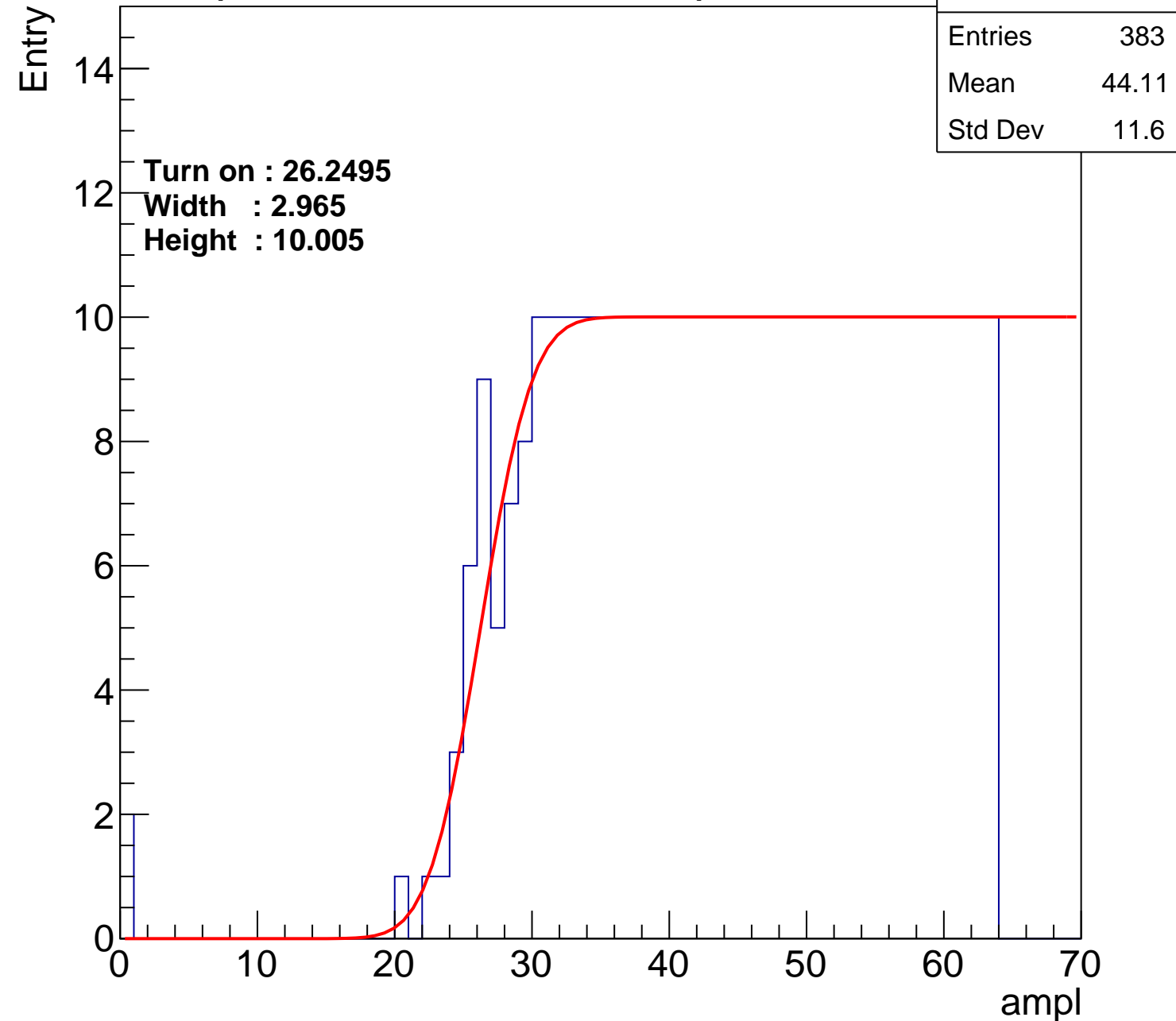
**Width : 2.965**

**Height : 10.005**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch77

calib\_packv5\_042523\_0143.root, FC#5, port B1

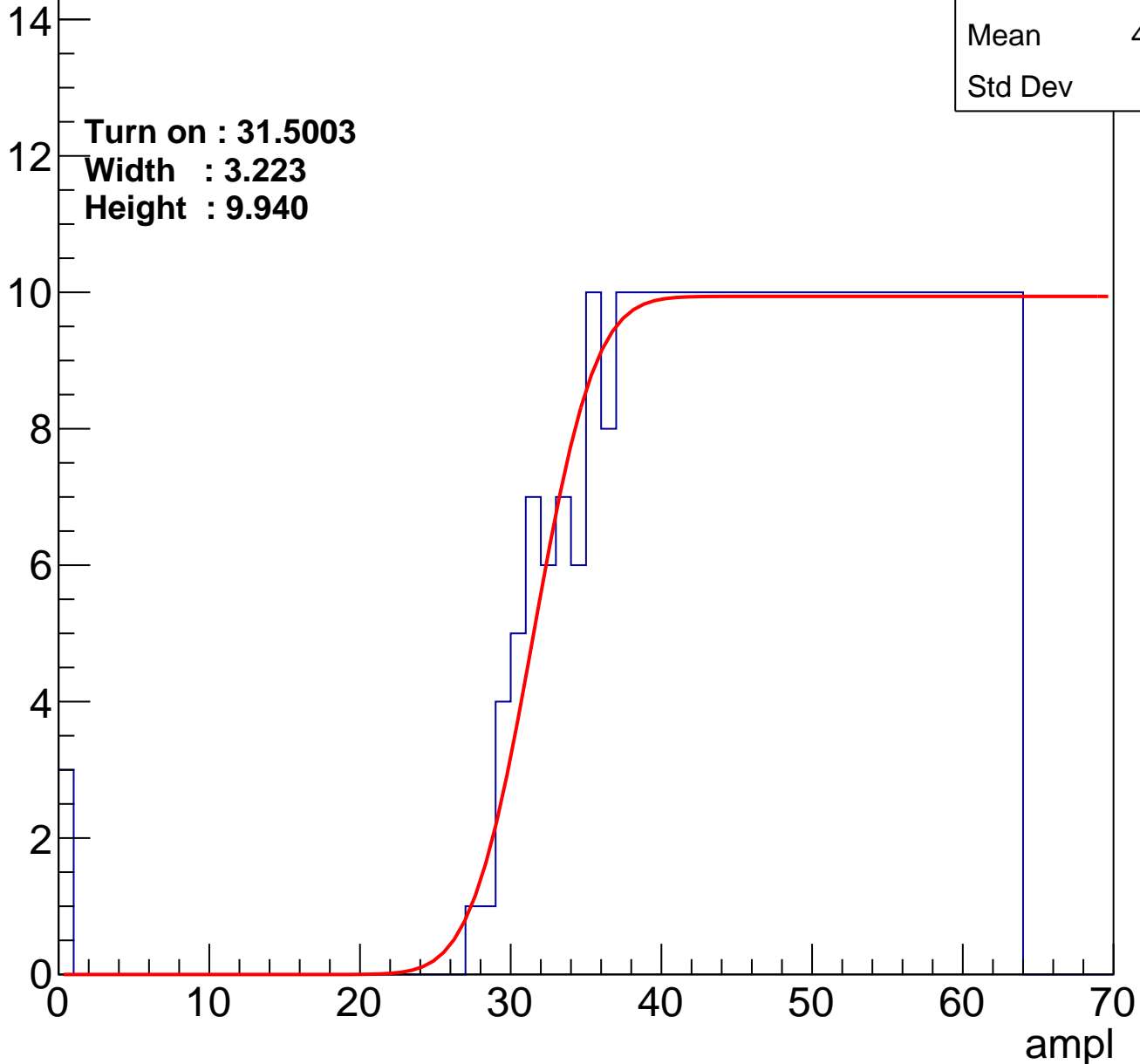
Entries	328
Mean	46.66
Std Dev	10.6

Turn on : 31.5003

Width : 3.223

Height : 9.940

Entry



# B0L000S, U4-ch78

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	376
Mean	44.45
Std Dev	11.43

Turn on : 26.8241

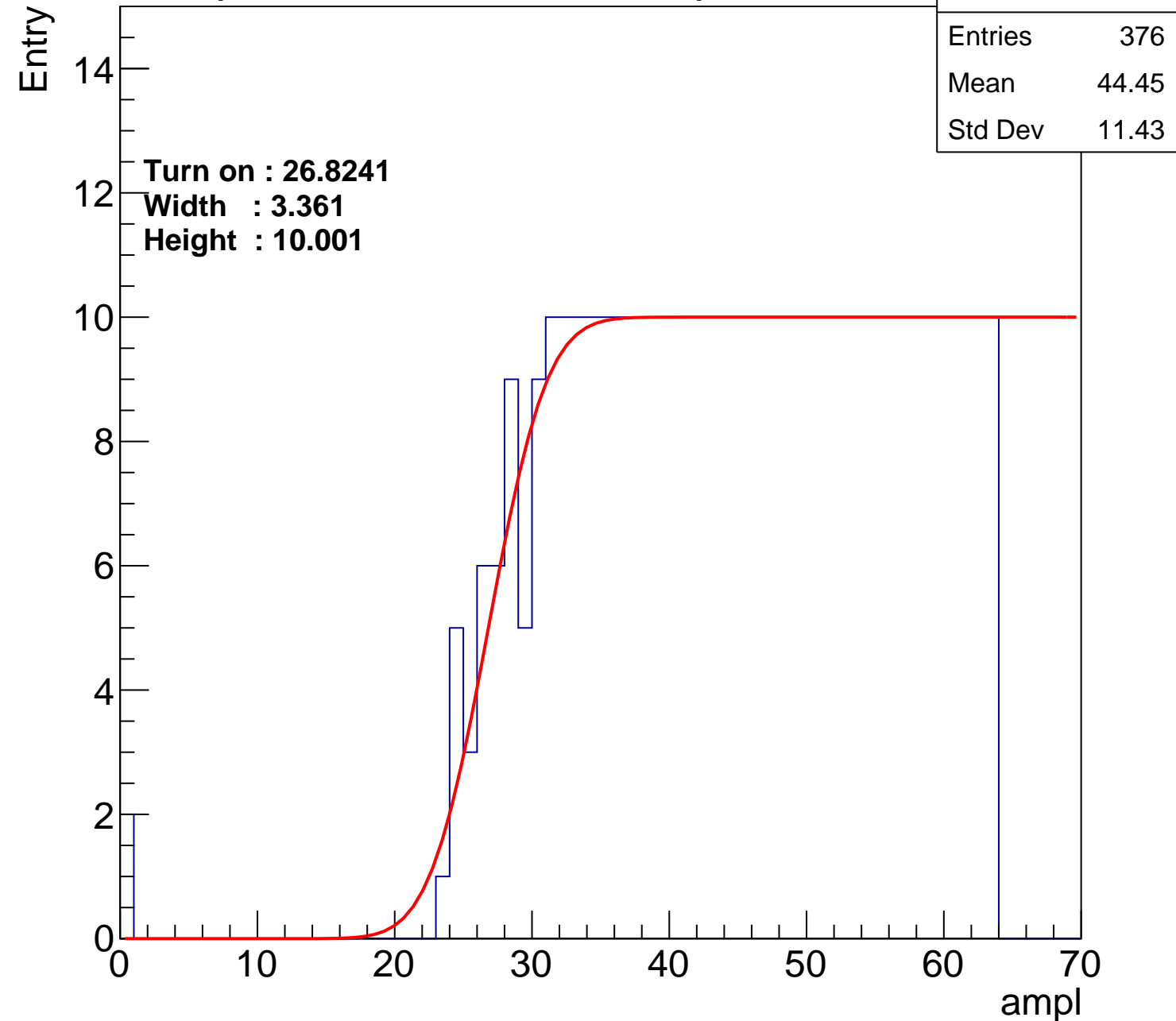
Width : 3.361

Height : 10.001

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L000S, U4-ch79

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	350
Mean	45.69
Std Dev	10.83

Turn on : 29.1291

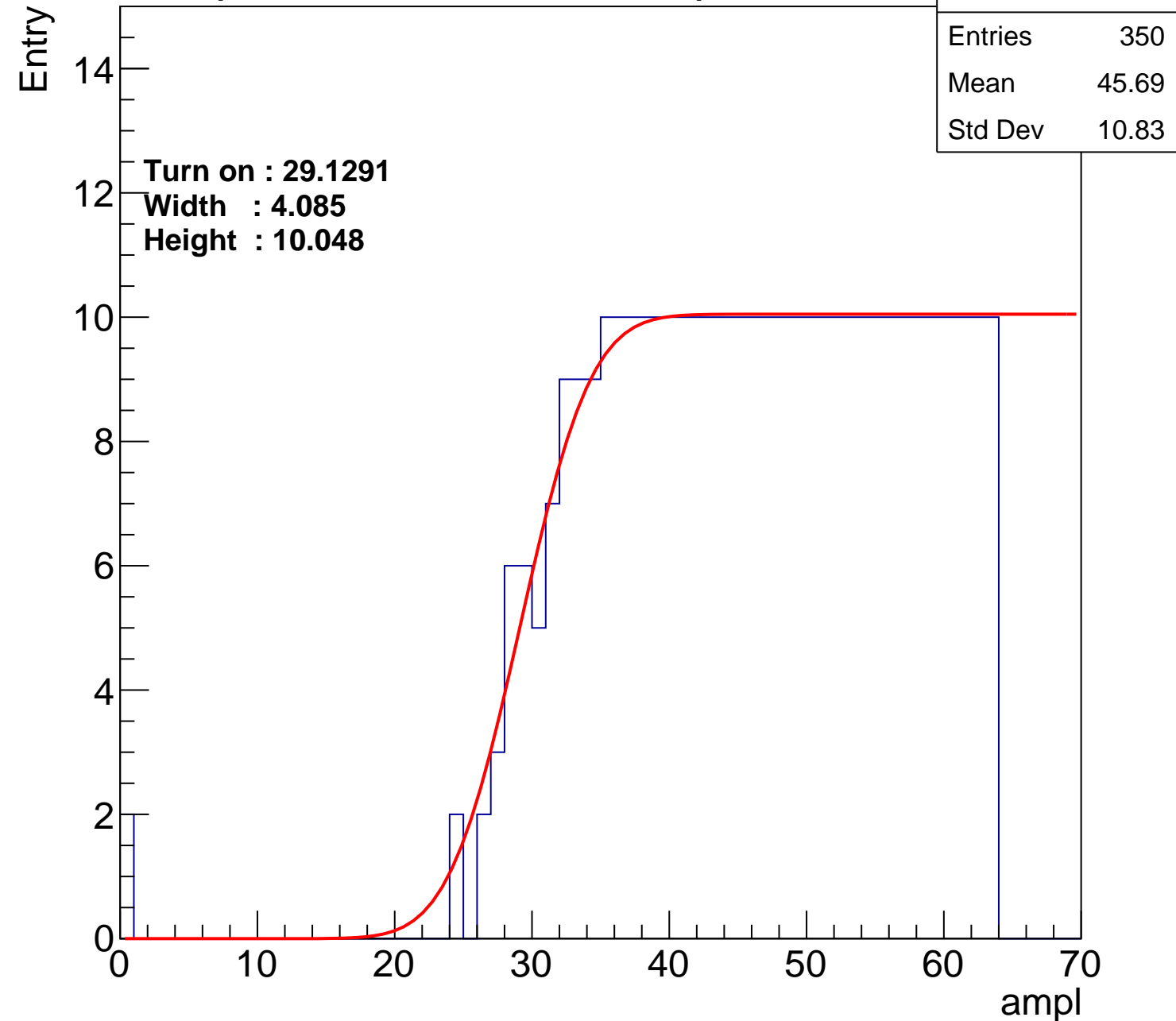
Width : 4.085

Height : 10.048

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch80

calib\_packv5\_042523\_0143.root, FC#5, port B1

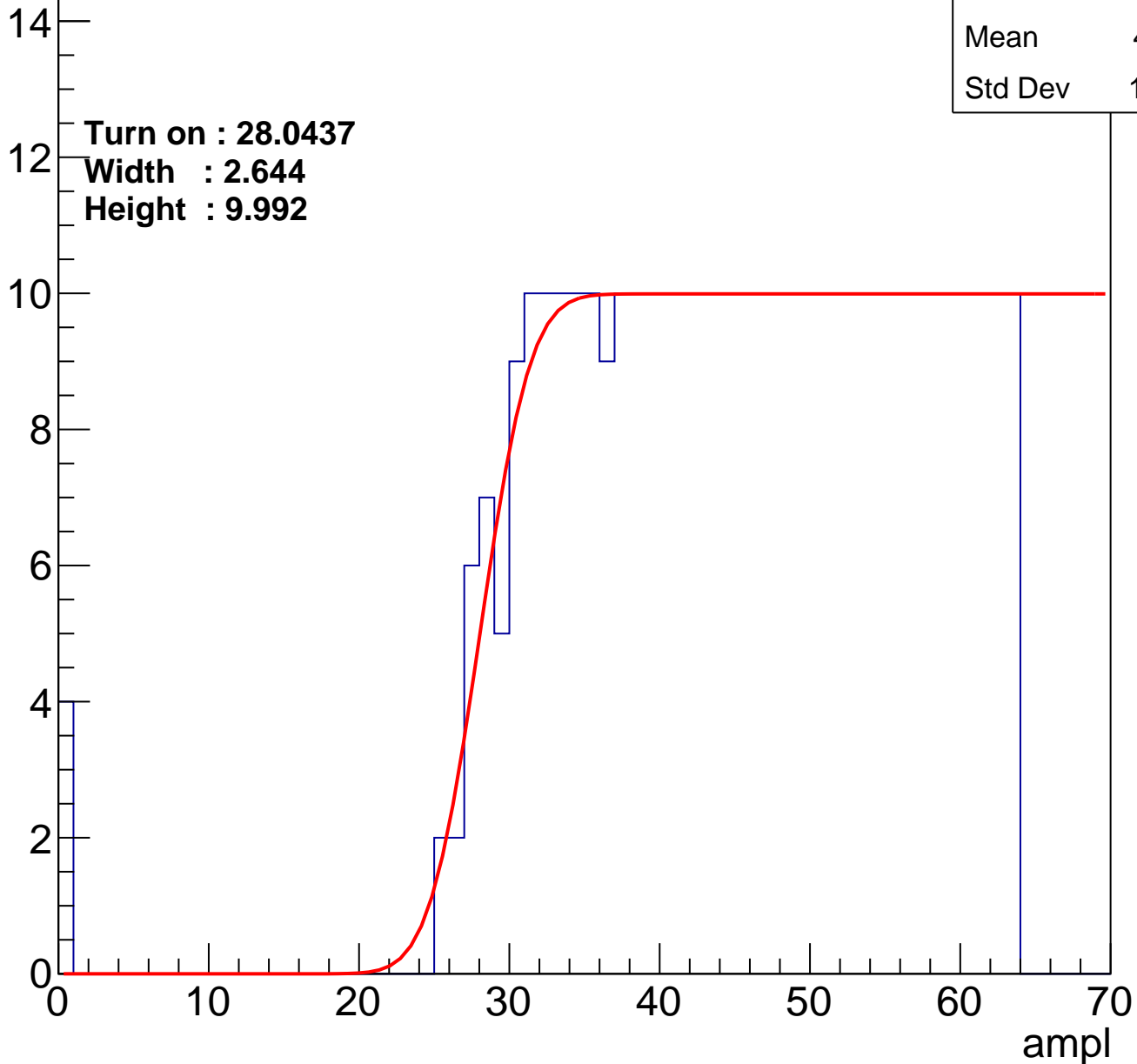
Entry

Entries	364
Mean	44.91
Std Dev	11.49

**Turn on : 28.0437**

**Width : 2.644**

**Height : 9.992**



# B0L000S, U4-ch81

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	374
Mean	44.48
Std Dev	11.57

Turn on : 27.0861

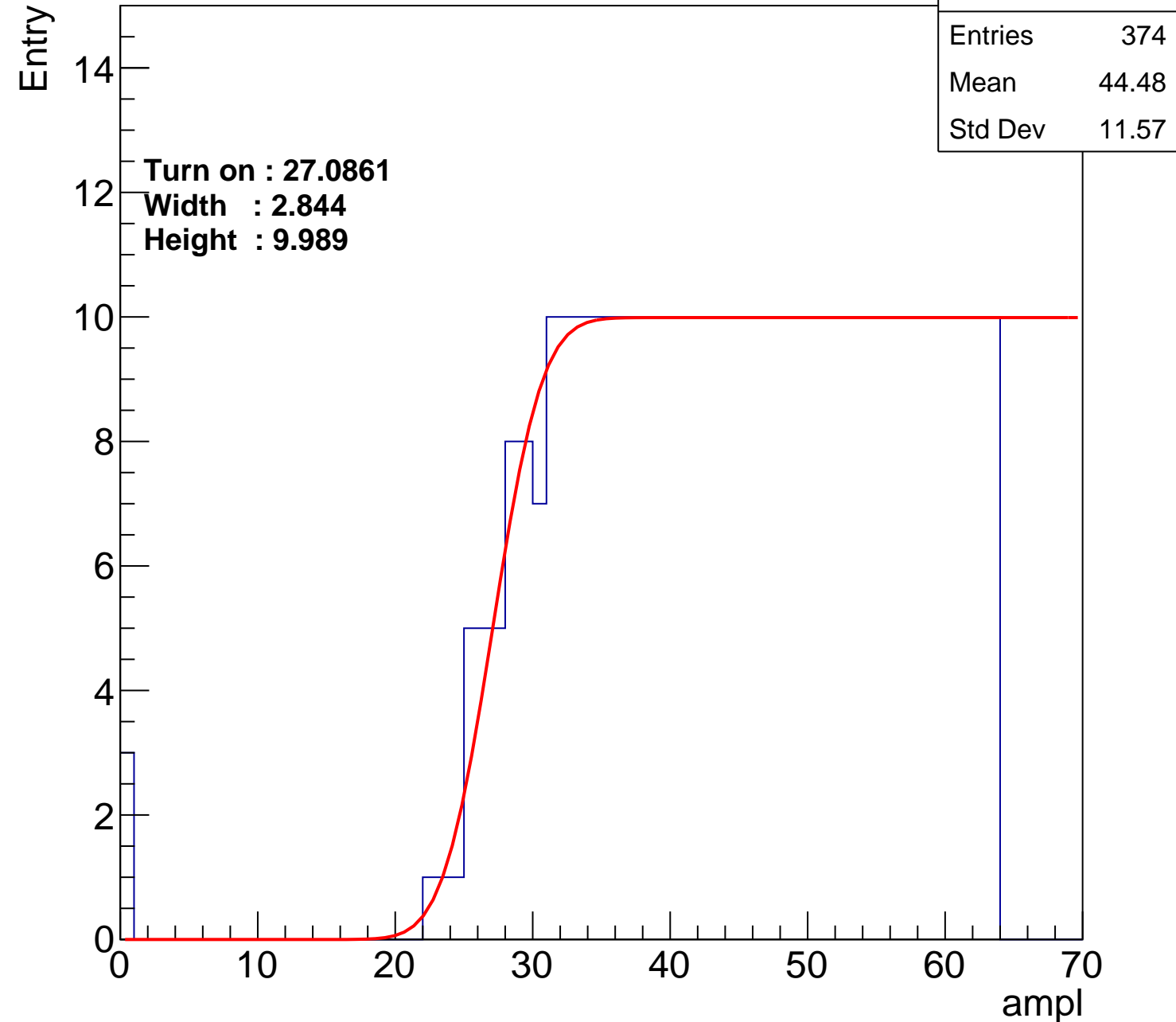
Width : 2.844

Height : 9.989

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch82

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	361
Mean	45.04
Std Dev	11.46

**Turn on : 28.2749**

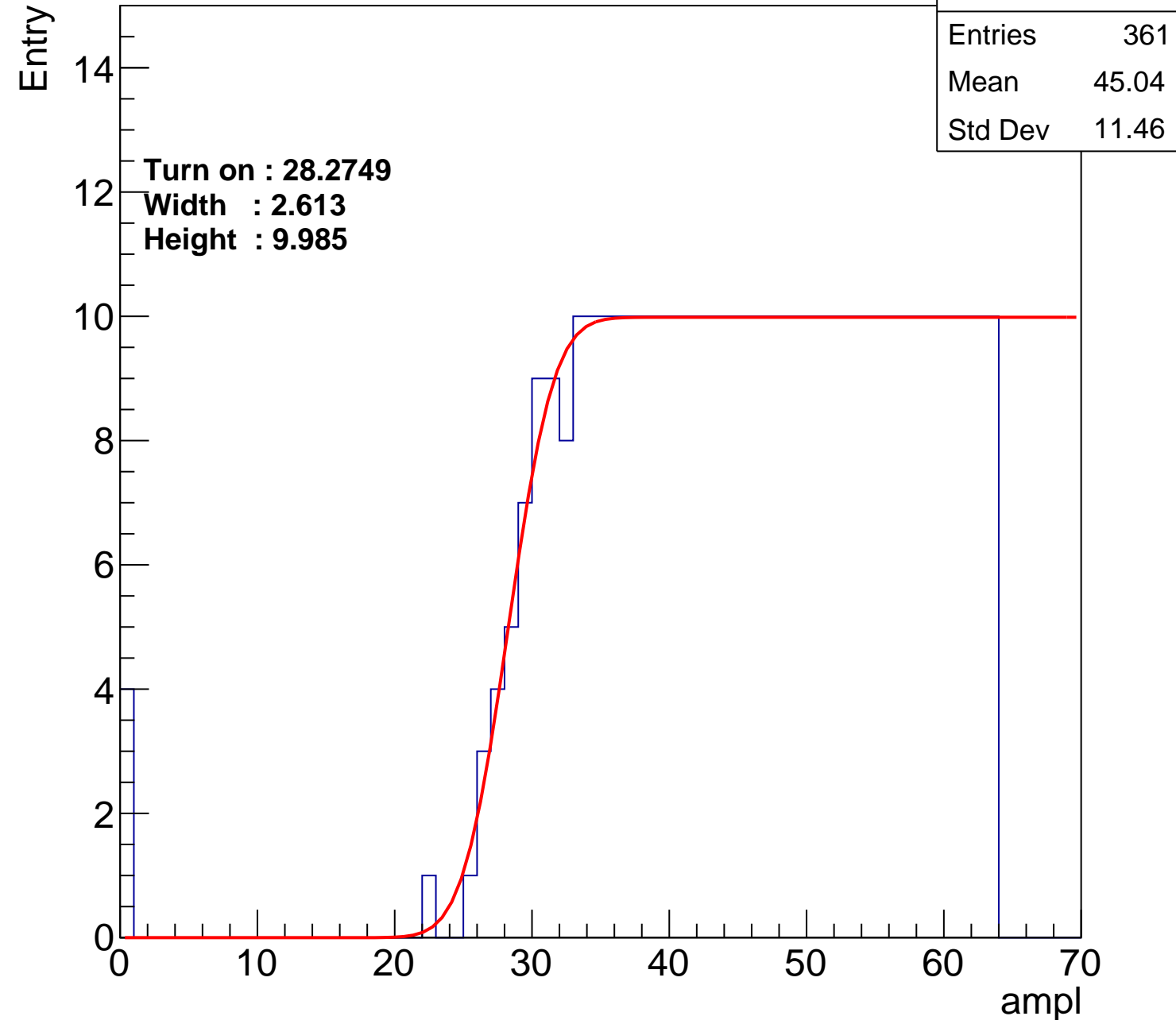
**Width : 2.613**

**Height : 9.985**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch83

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	381
Mean	44.26
Std Dev	11.39

**Turn on : 26.3495**

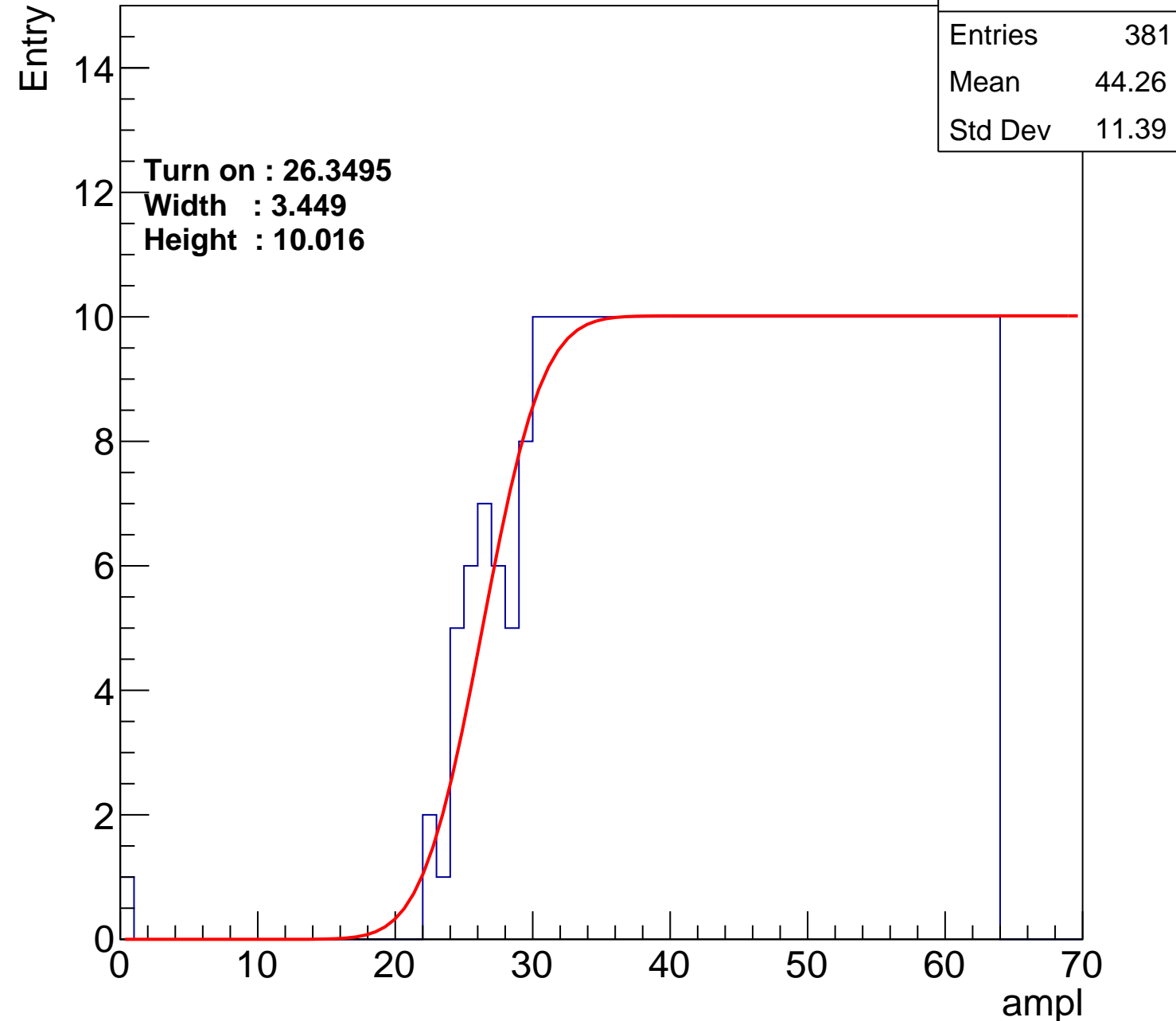
**Width : 3.449**

**Height : 10.016**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch84

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	384
Mean	43.97
Std Dev	11.84

**Turn on : 26.0708**

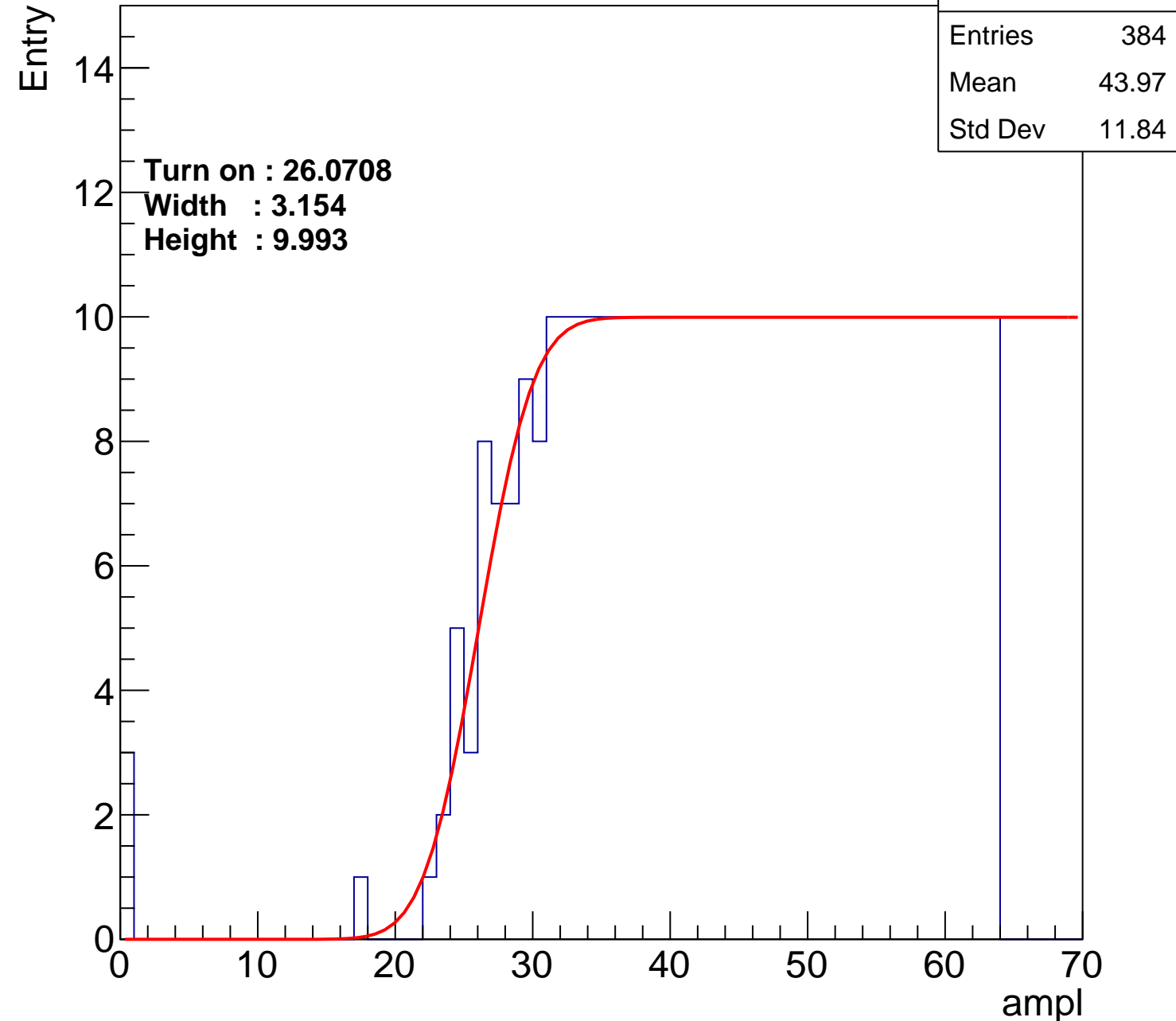
**Width : 3.154**

**Height : 9.993**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch85

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	364
Mean	44.98
Std Dev	11.32

Turn on : 28.0718

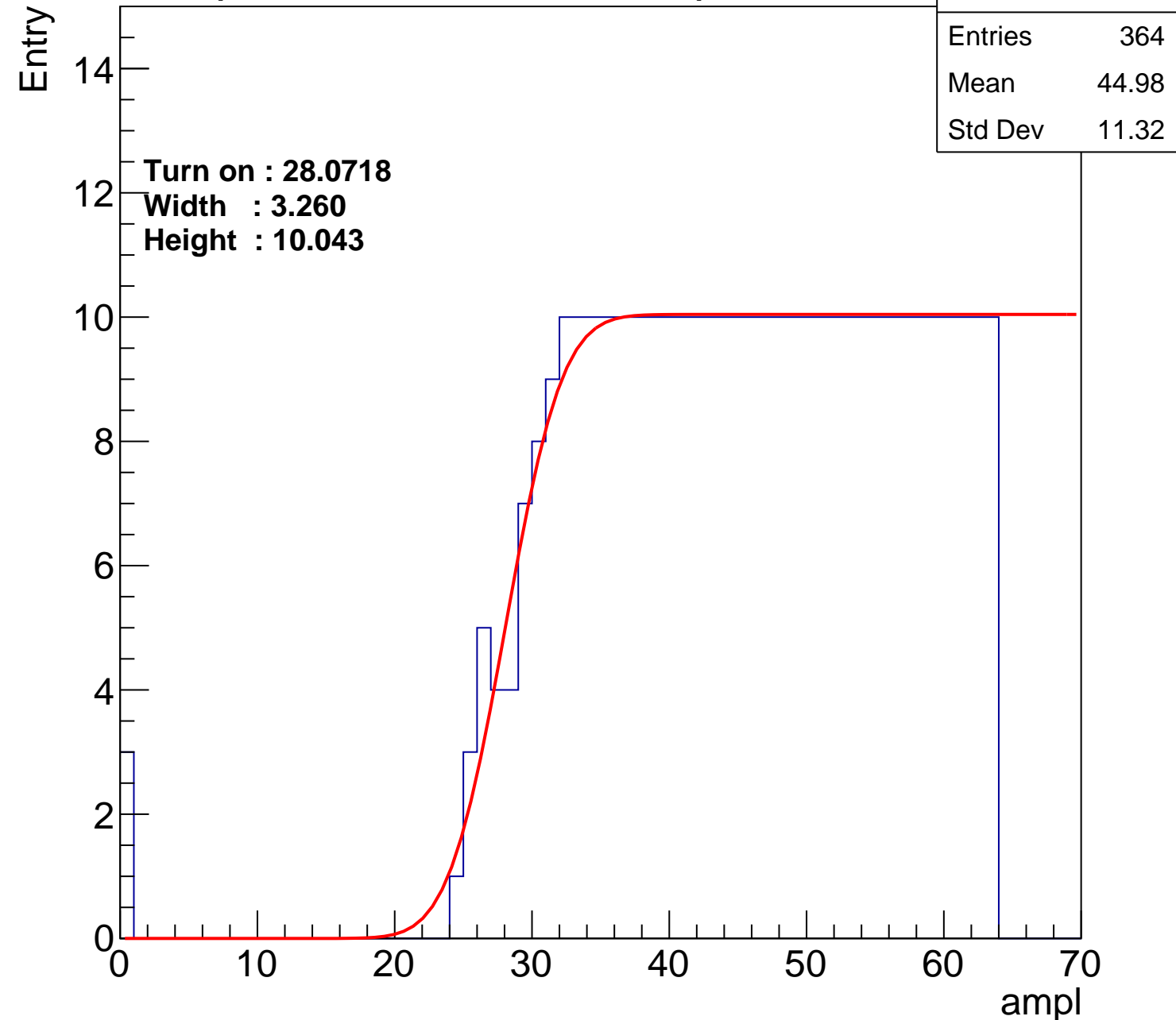
Width : 3.260

Height : 10.043

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch86

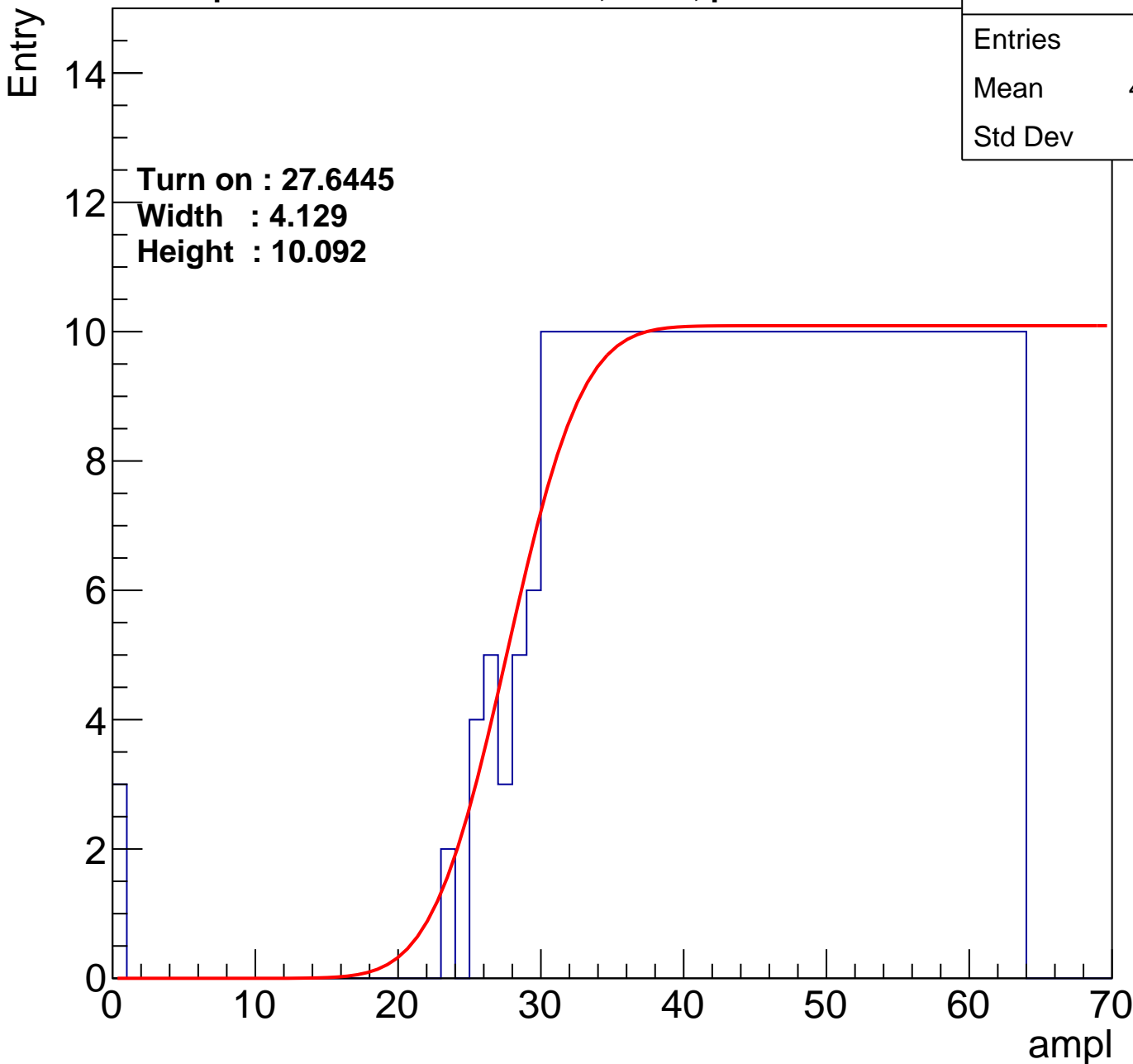
**calib\_packv5\_042523\_0143.root, FC#5, port B1**

Entries	368
Mean	44.79
Std Dev	11.41

**Turn on : 27.6445**

**Width : 4.129**

**Height : 10.092**





# B0L000S, U4-ch87

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	372
Mean	44.67
Std Dev	11.21

Turn on : 27.3728

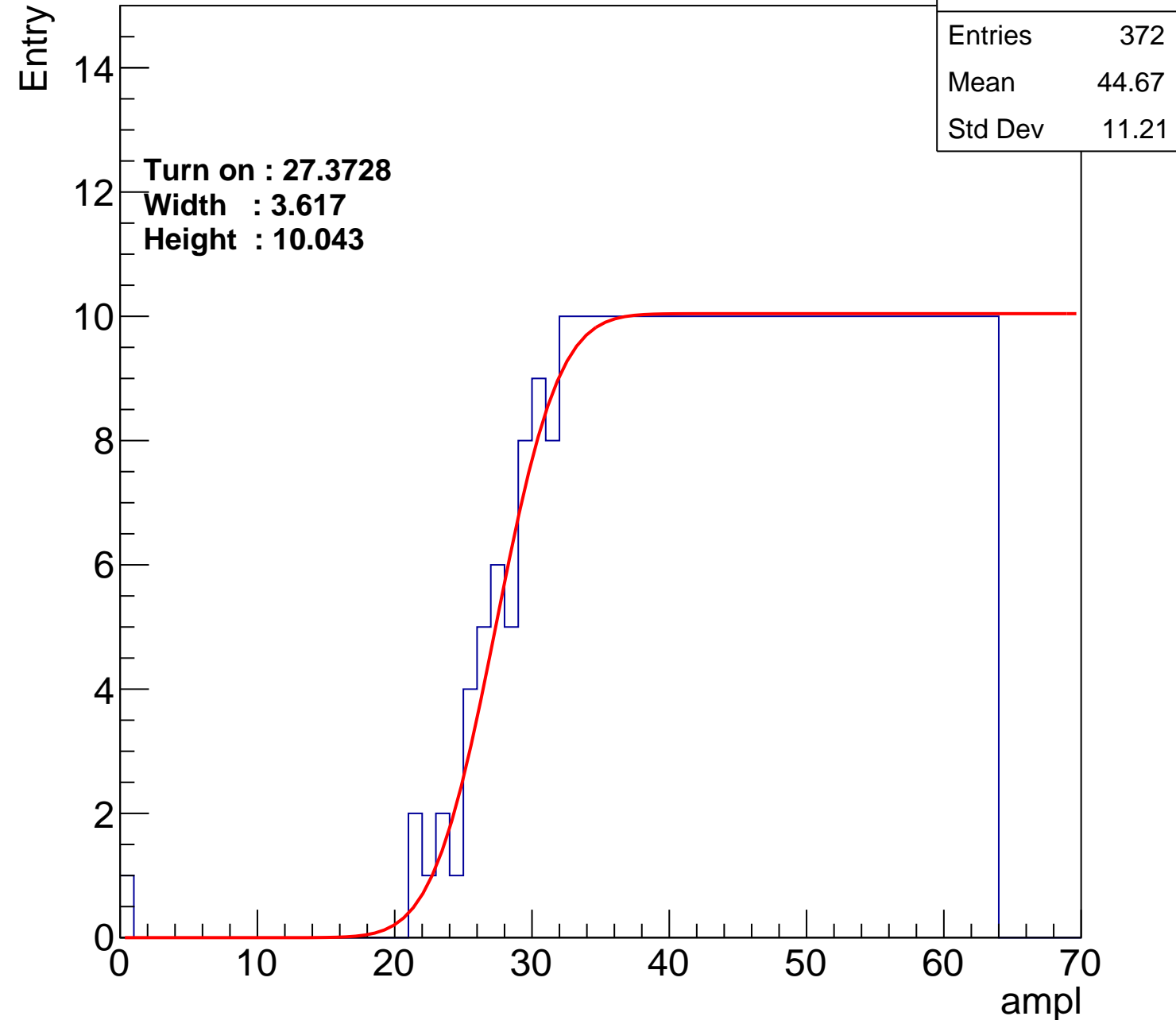
Width : 3.617

Height : 10.043

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch88

calib\_packv5\_042523\_0143.root, FC#5, port B1

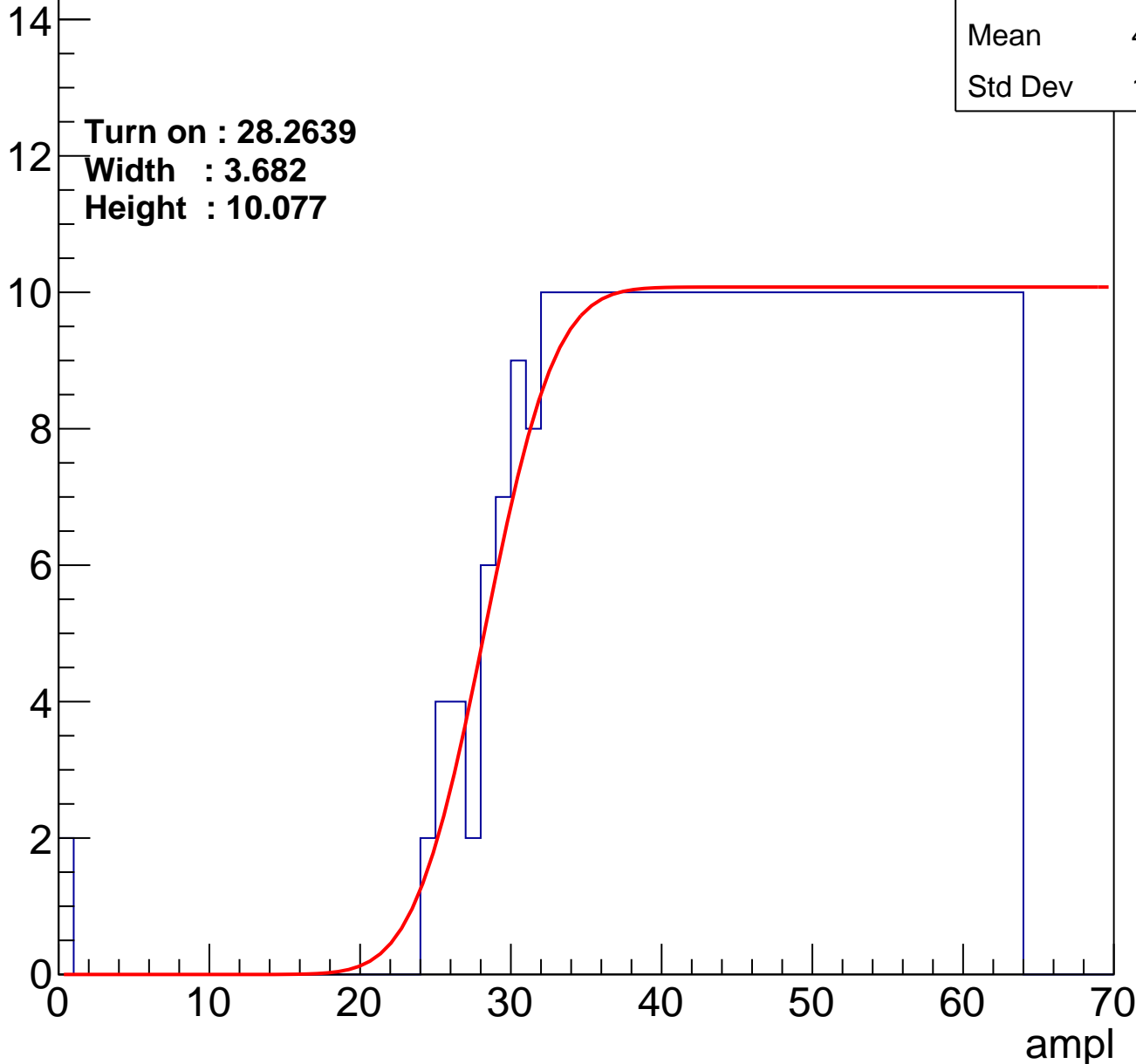
Entries	364
Mean	45.04
Std Dev	11.12

Turn on : 28.2639

Width : 3.682

Height : 10.077

Entry



# B0L000S, U4-ch89

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	374
Mean	44.24
Std Dev	12.16

Turn on : 27.4749

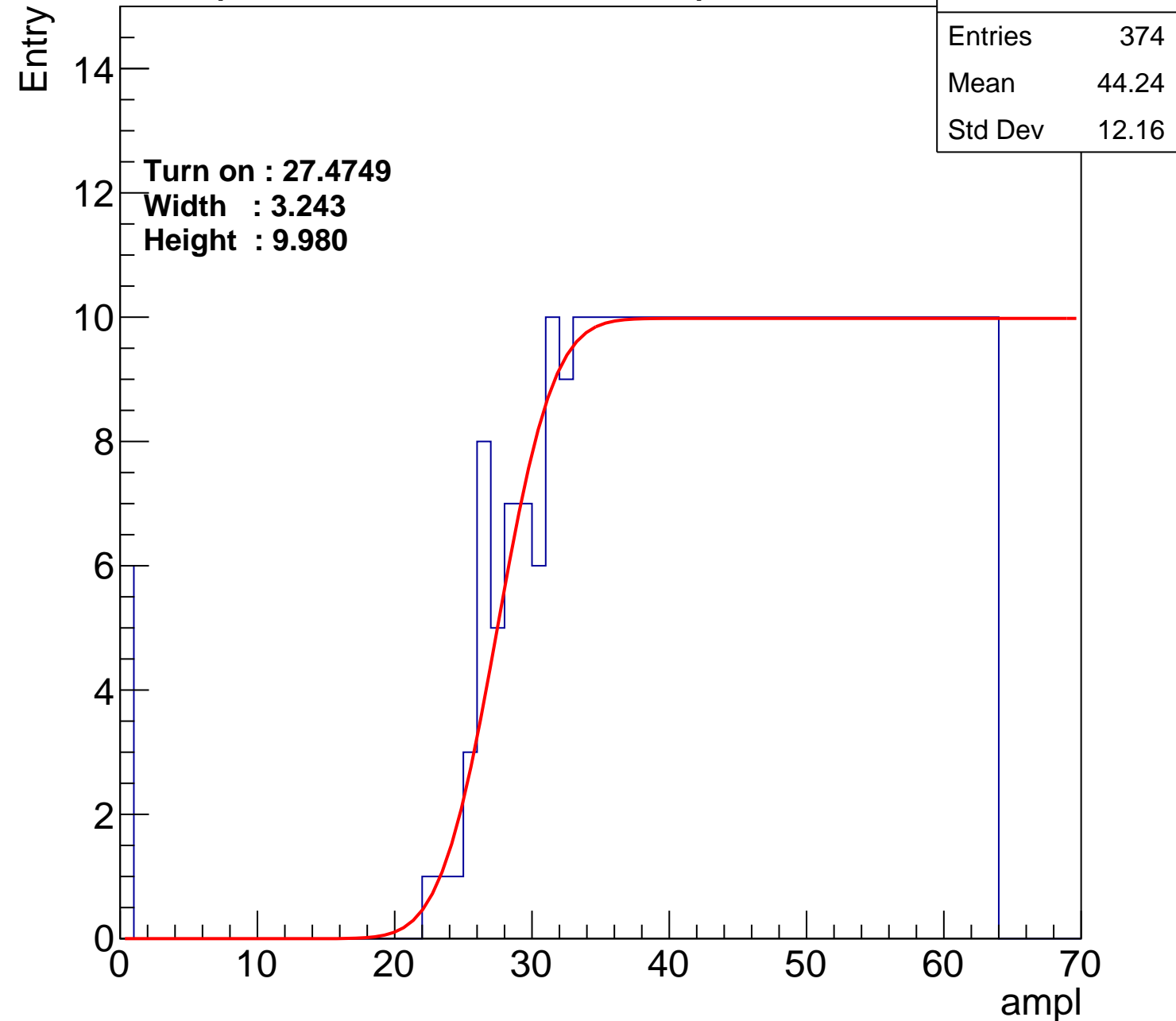
Width : 3.243

Height : 9.980

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch90

calib\_packv5\_042523\_0143.root, FC#5, port B1

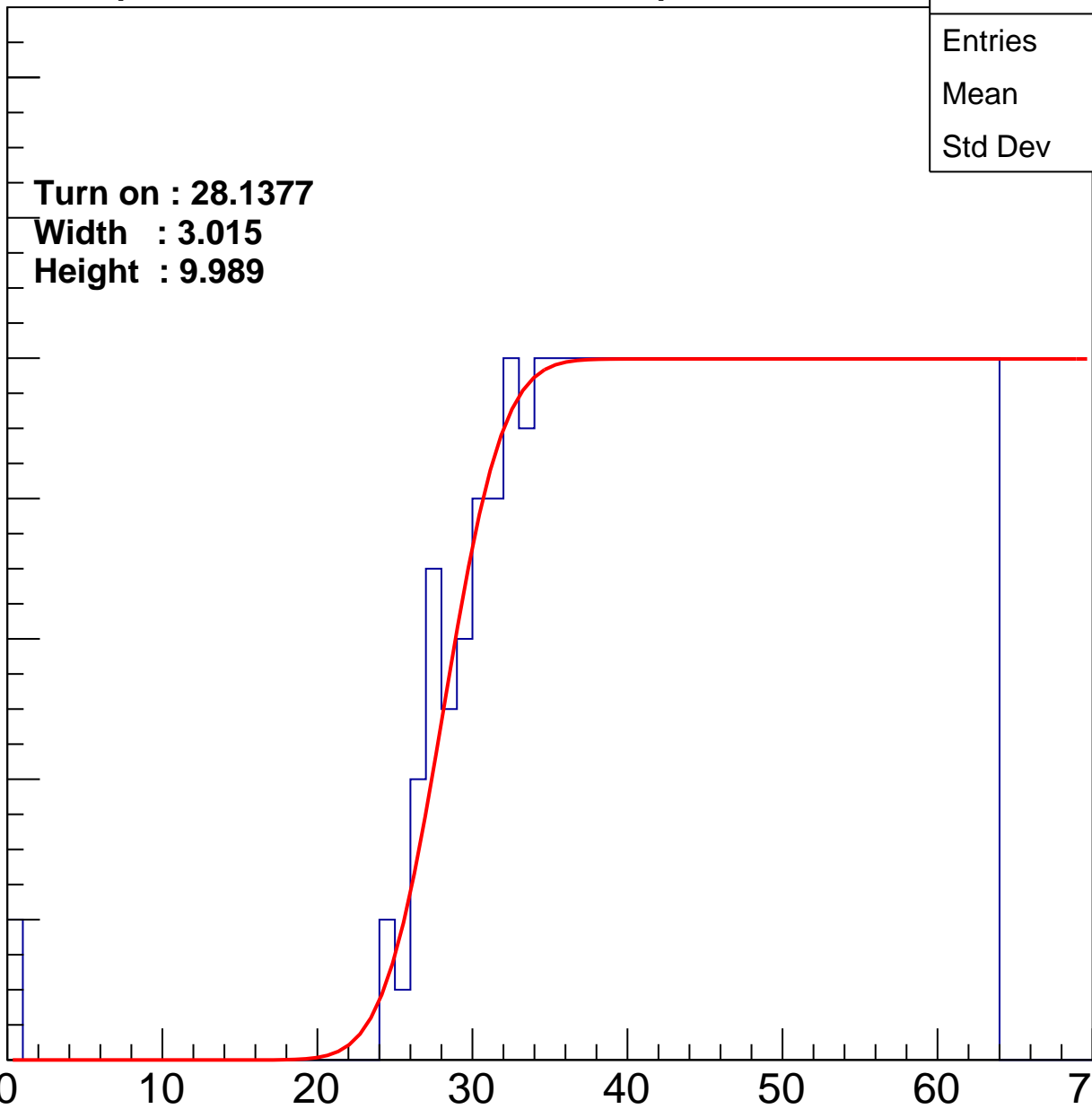
Entry

14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 28.1377**  
**Width : 3.015**  
**Height : 9.989**

Entries	362
Mean	45.12
Std Dev	11.09

ampl



# B0L000S, U4-ch91

calib\_packv5\_042523\_0143.root, FC#5, port B1

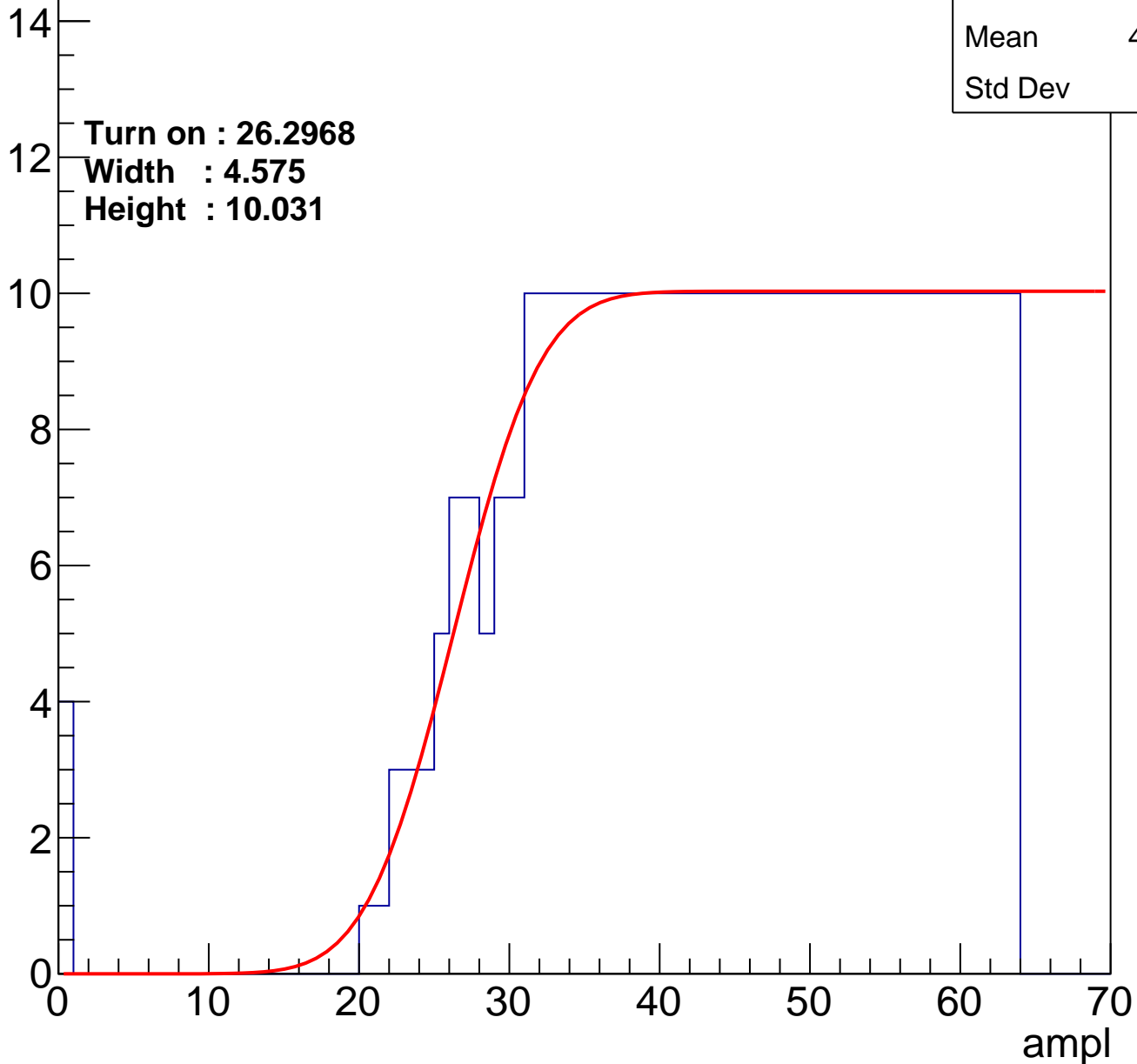
Entries	383
Mean	43.88
Std Dev	12.1

Turn on : 26.2968

Width : 4.575

Height : 10.031

Entry



# B0L000S, U4-ch92

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	371
Mean	44.68
Std Dev	11.33

Turn on : 27.7228

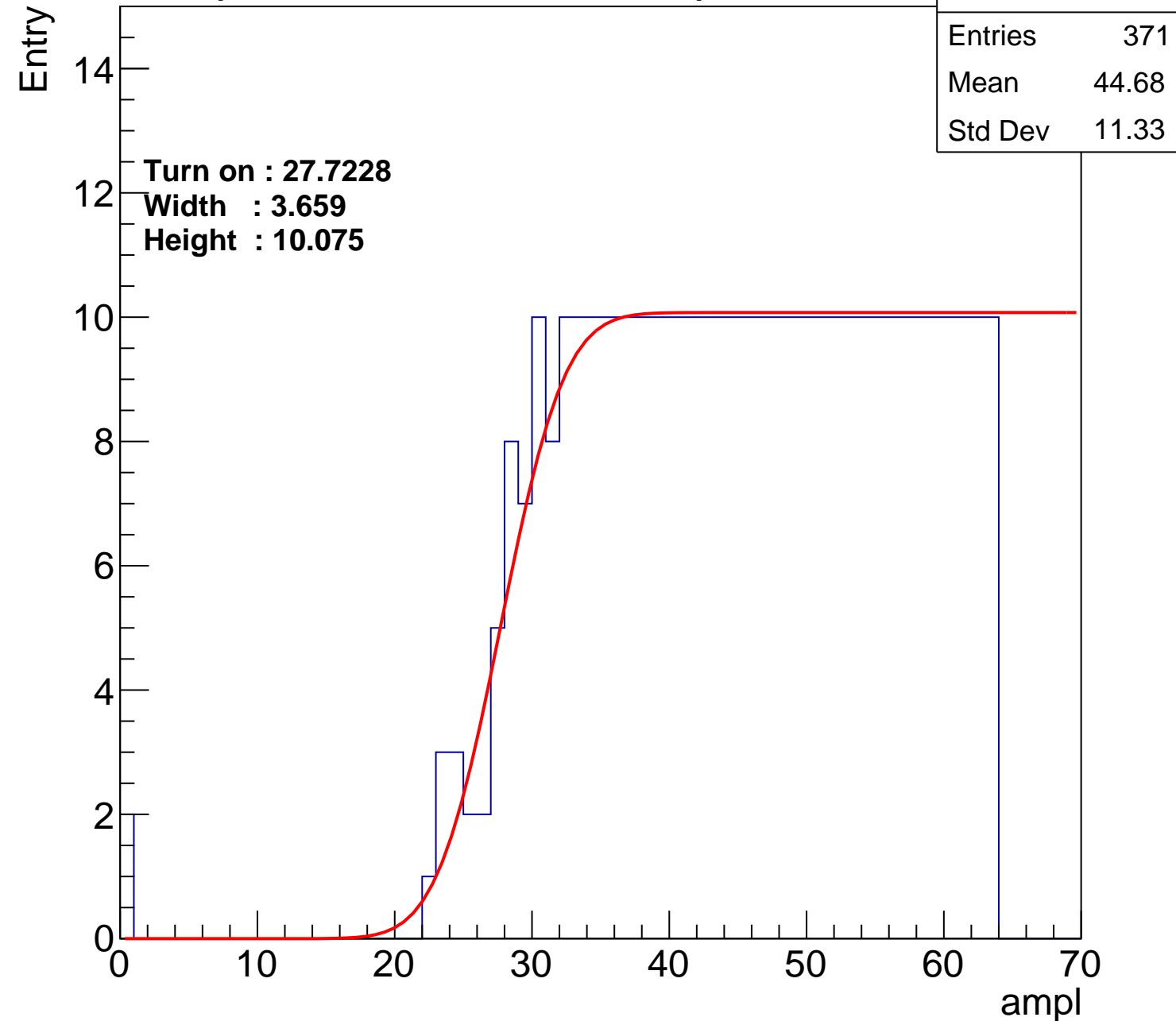
Width : 3.659

Height : 10.075

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch93

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	375
Mean	44.39
Std Dev	11.74

**Turn on : 26.9487**

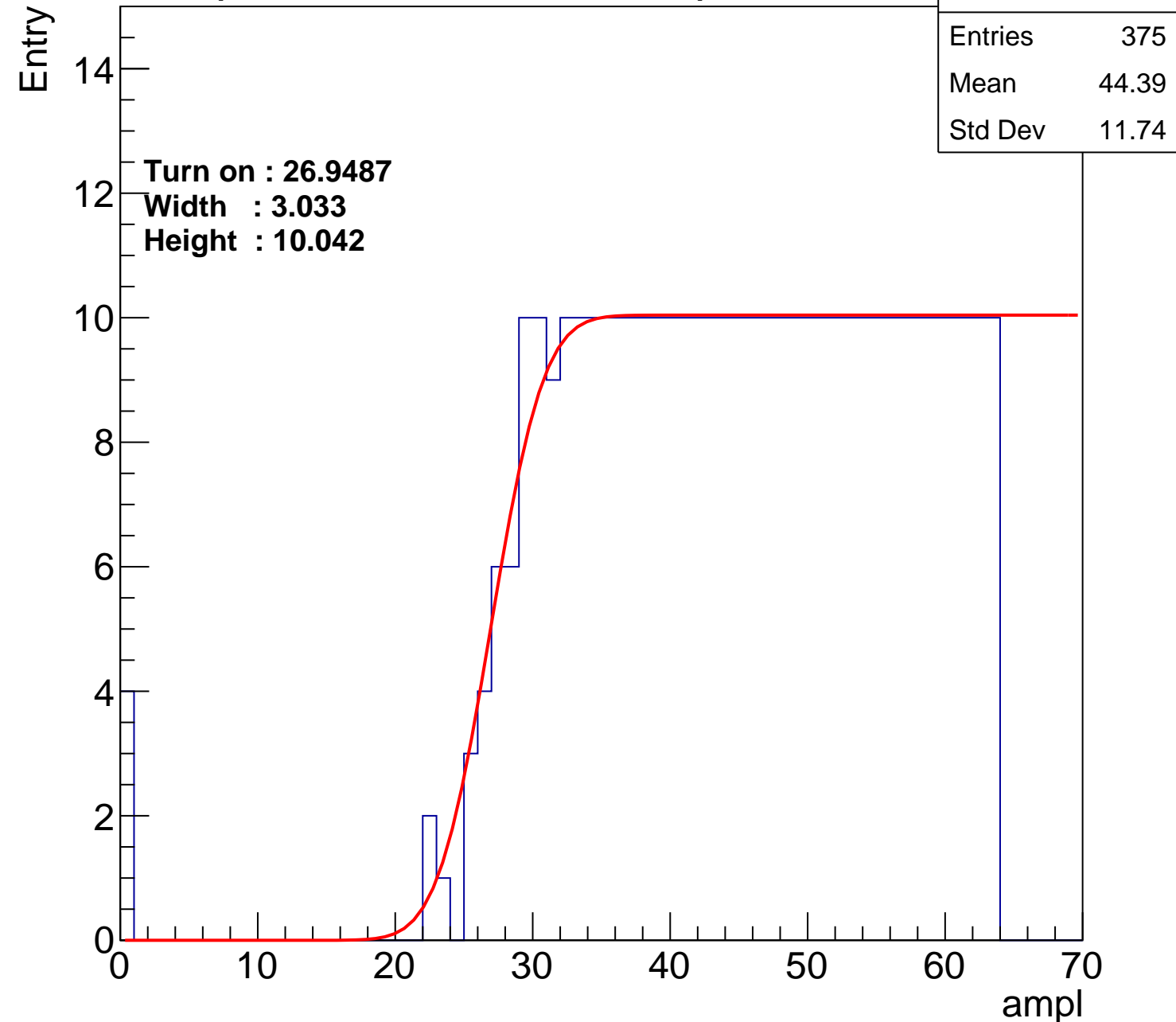
**Width : 3.033**

**Height : 10.042**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch94

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	389
Mean	43.77
Std Dev	11.9

Turn on : 25.7418

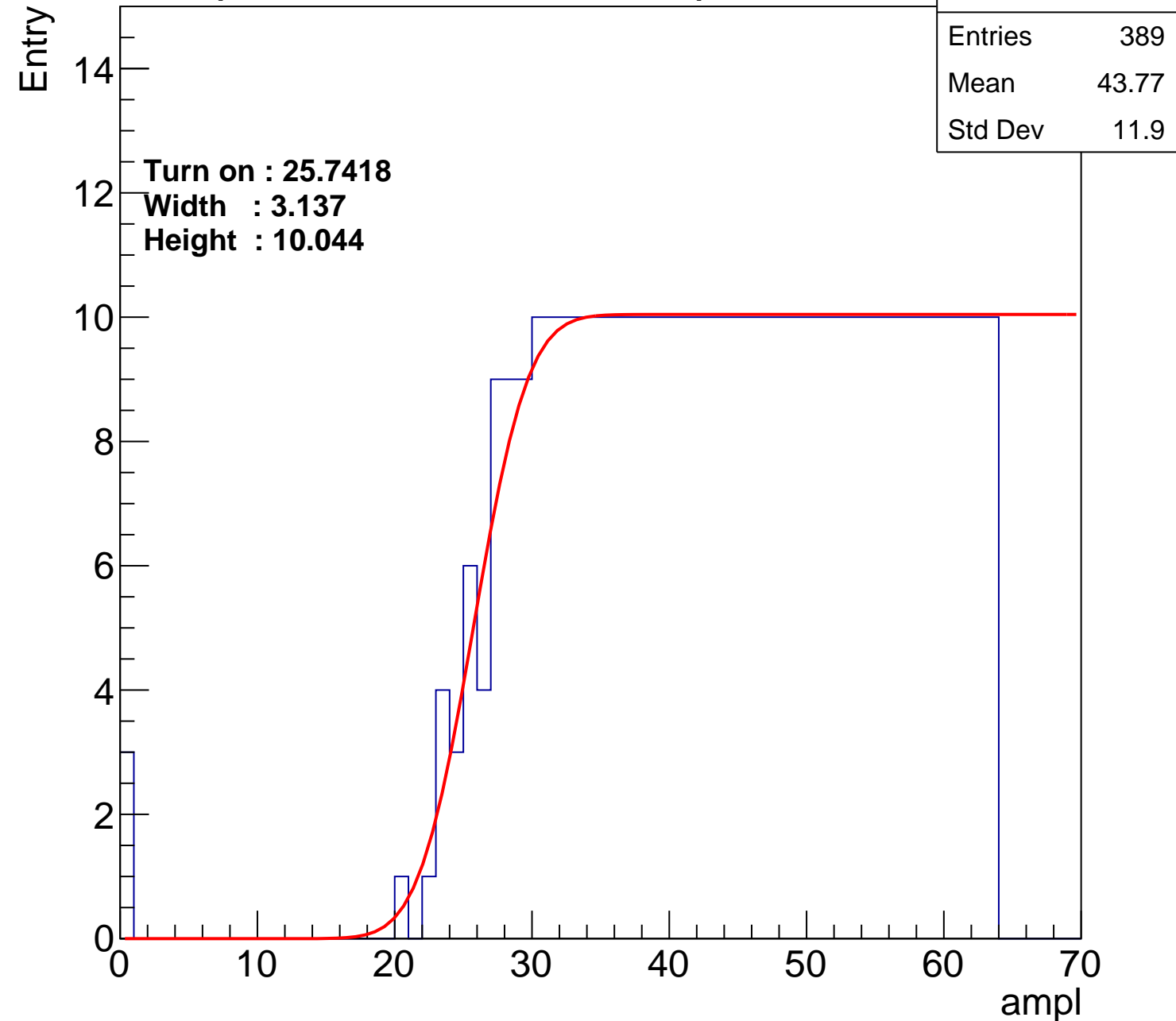
Width : 3.137

Height : 10.044

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L000S, U4-ch95

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	386
Mean	43.7
Std Dev	12.29

**Turn on : 26.2710**

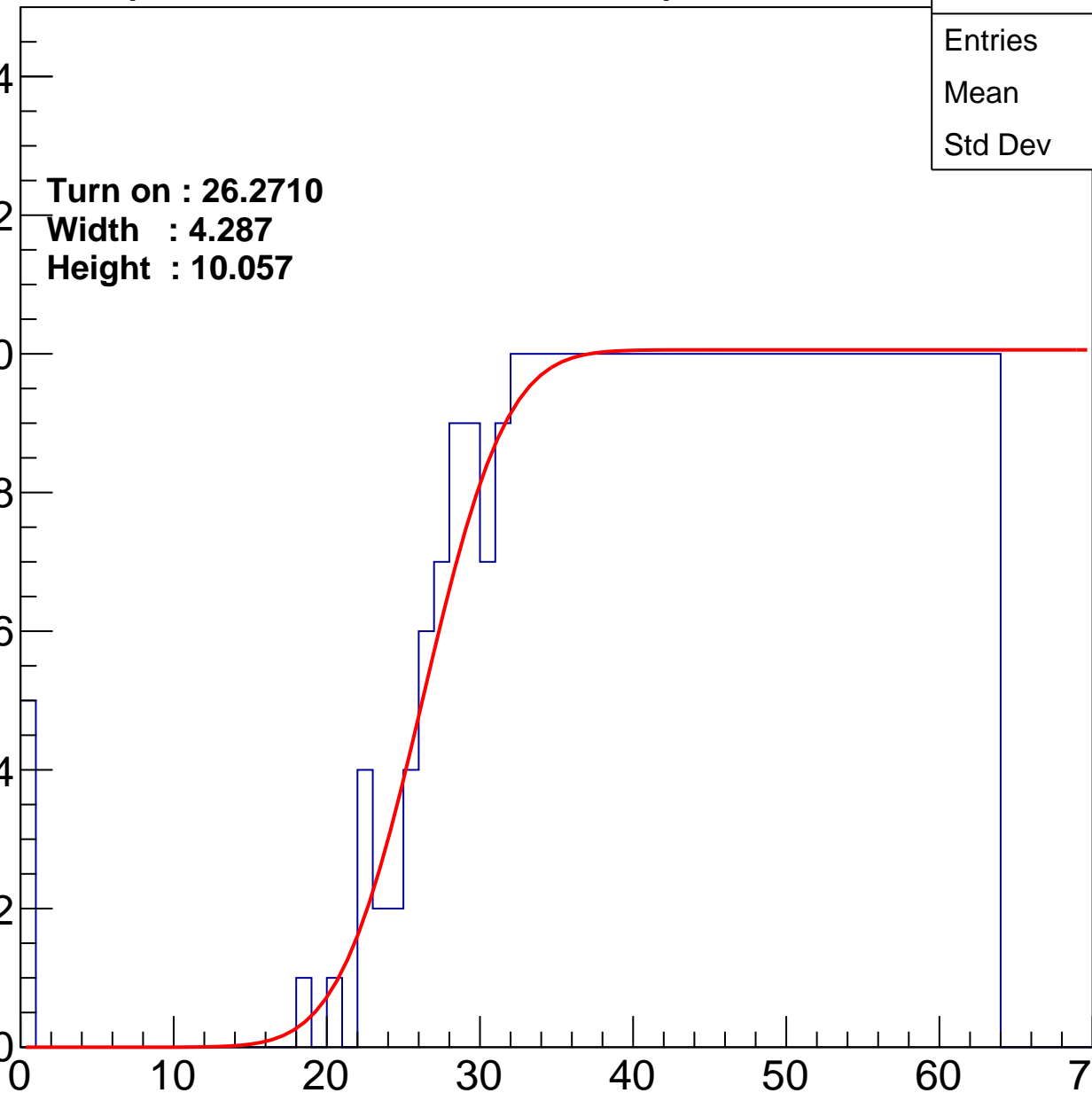
**Width : 4.287**

**Height : 10.057**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch96

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	372
Mean	44.49
Std Dev	11.73

Turn on : 27.2070

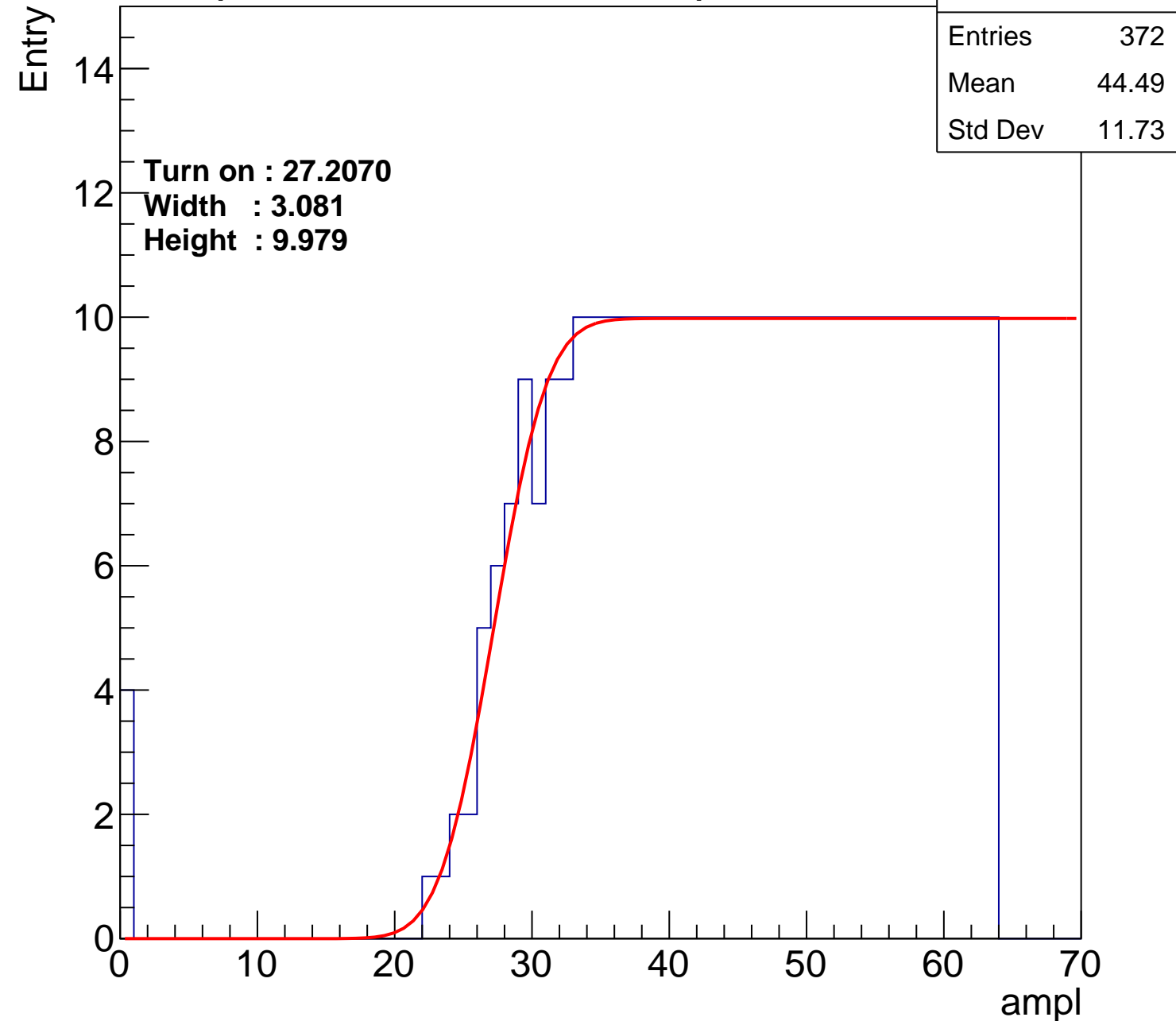
Width : 3.081

Height : 9.979

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch97

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	370
Mean	44.76
Std Dev	11.26

Turn on : 27.3910

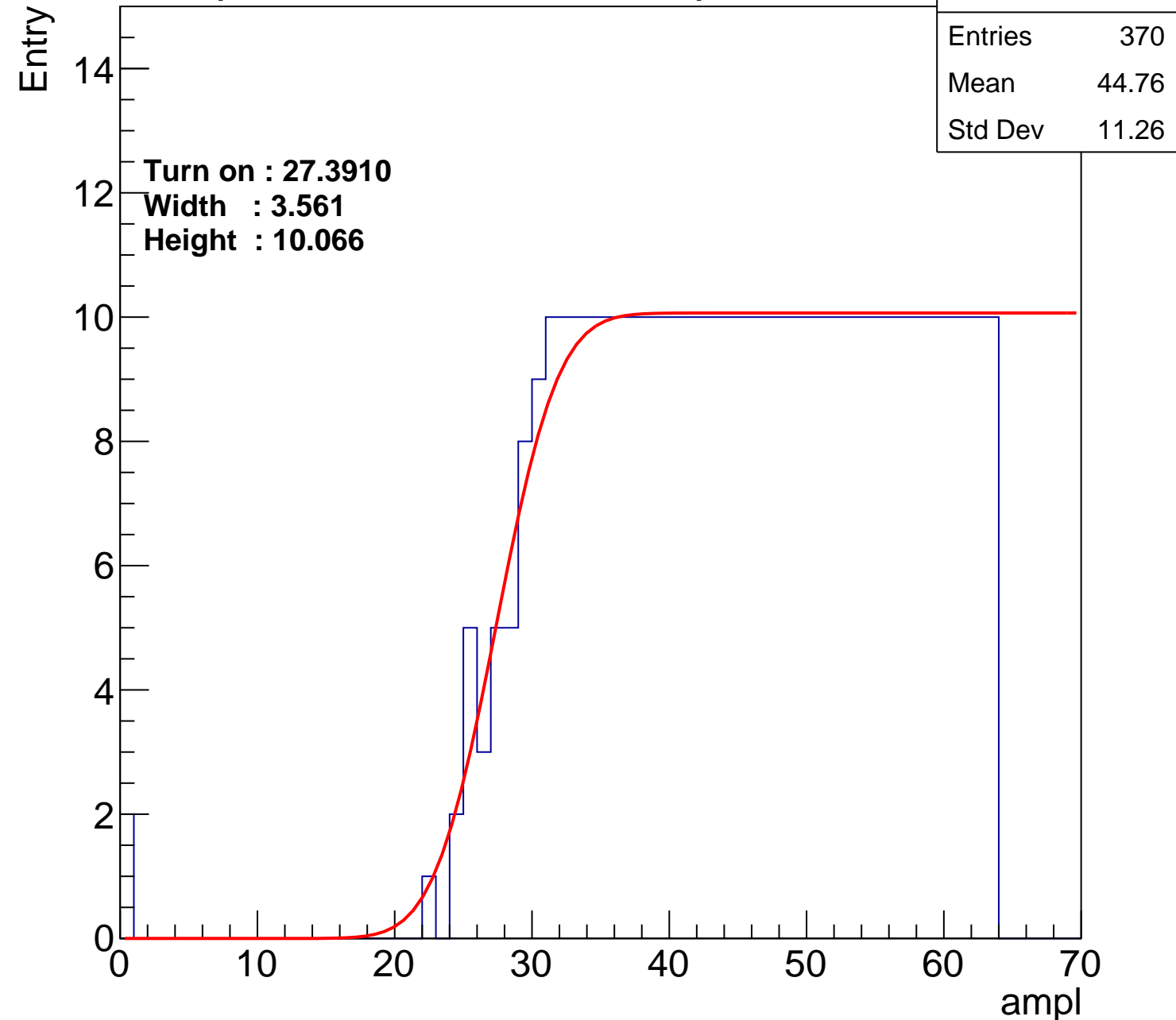
Width : 3.561

Height : 10.066

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch98

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	376
Mean	44.3
Std Dev	11.82

Turn on : 27.0910

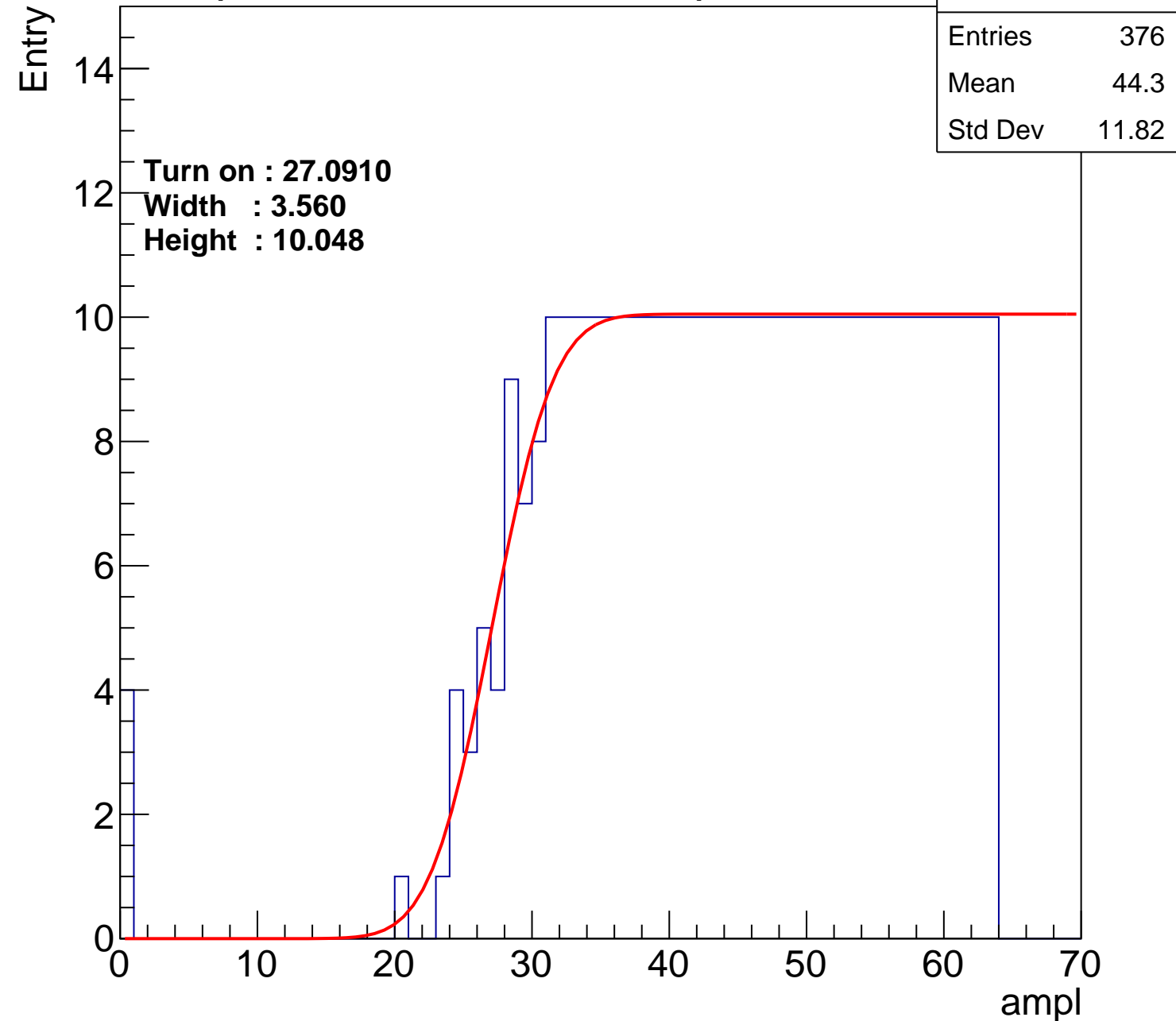
Width : 3.560

Height : 10.048

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch99

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	371
Mean	44.53
Std Dev	11.74

**Turn on : 28.0109**

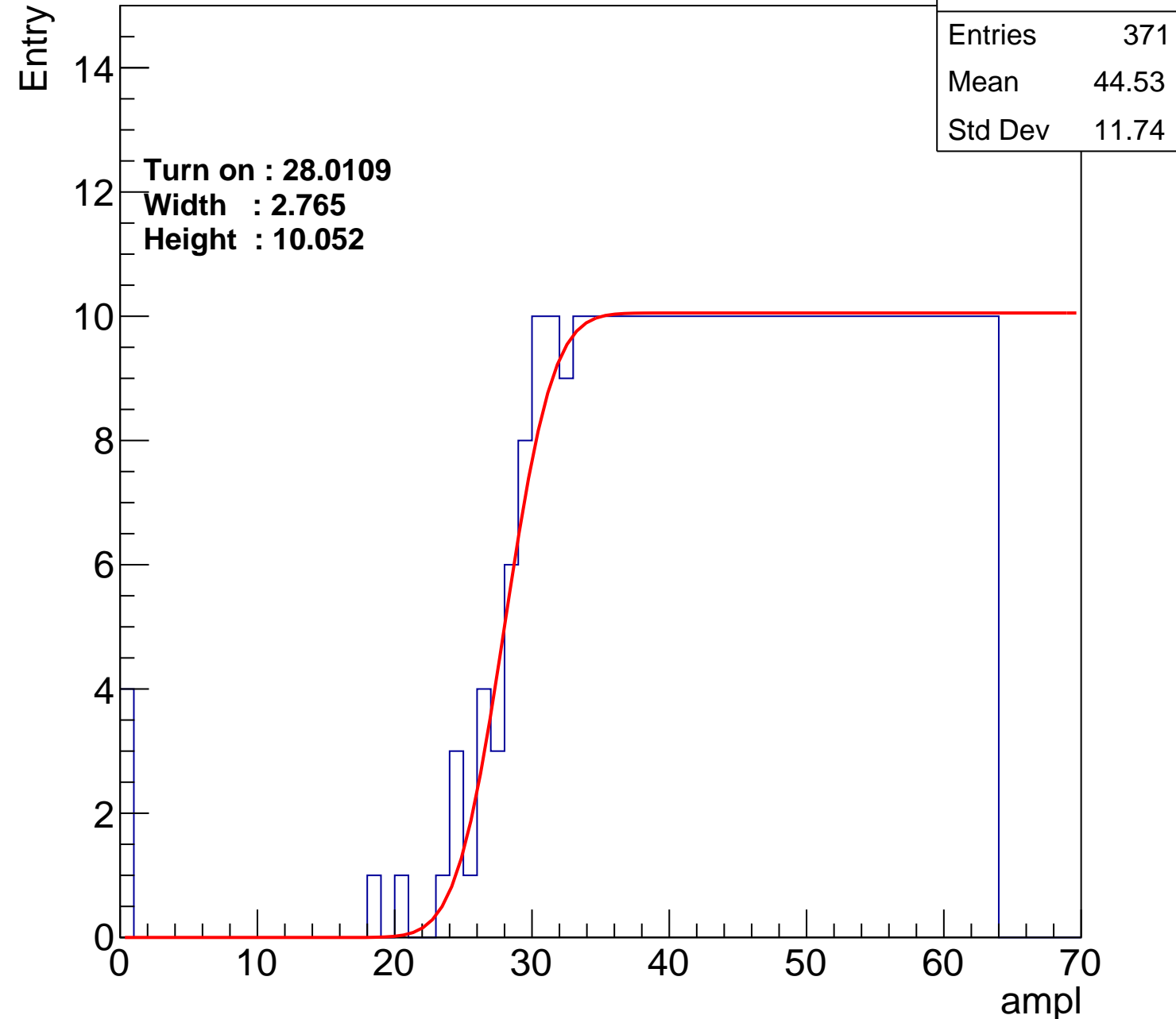
**Width : 2.765**

**Height : 10.052**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch100

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	379
Mean	44.31
Std Dev	11.49

Turn on : 26.3858

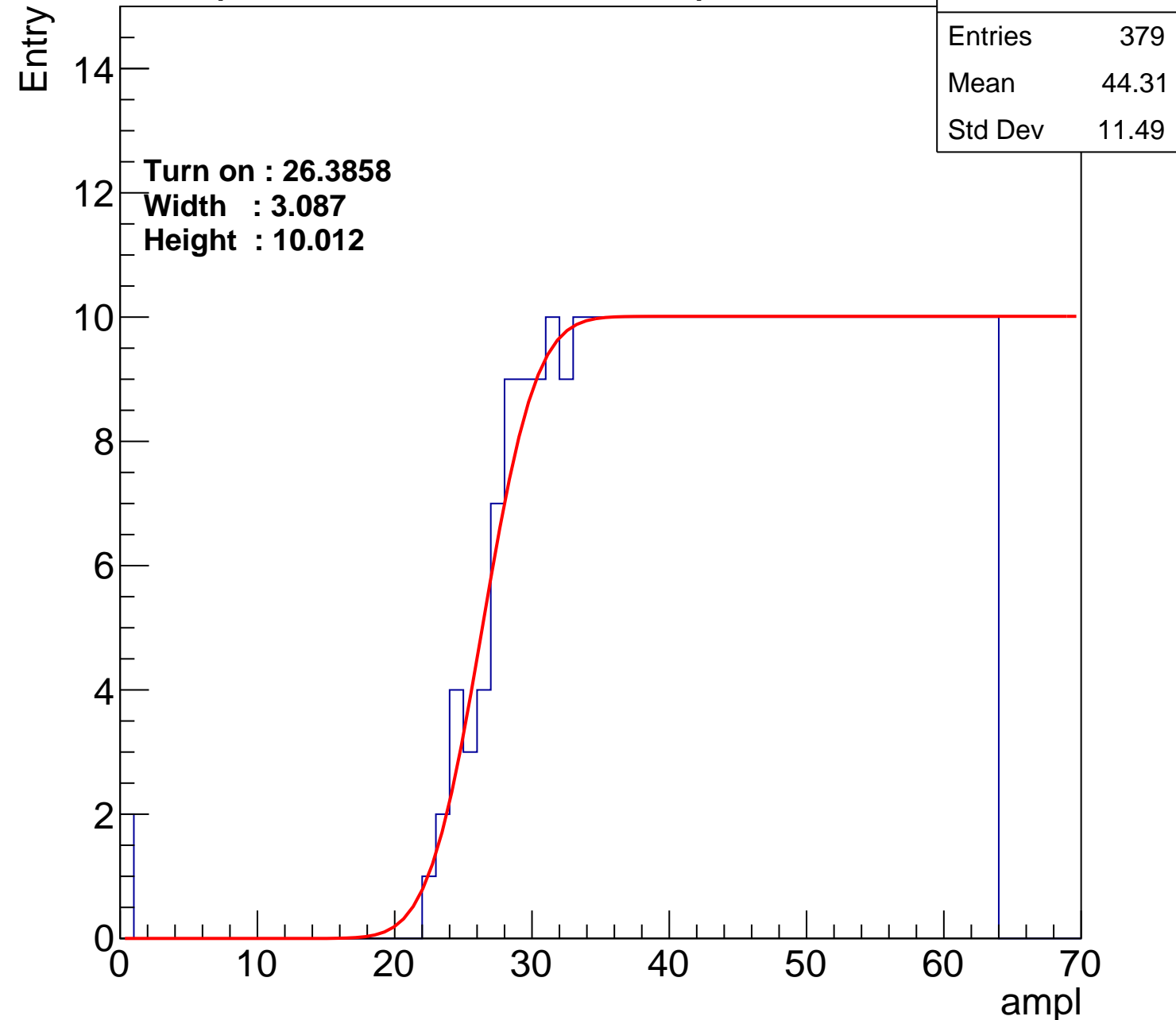
Width : 3.087

Height : 10.012

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch101

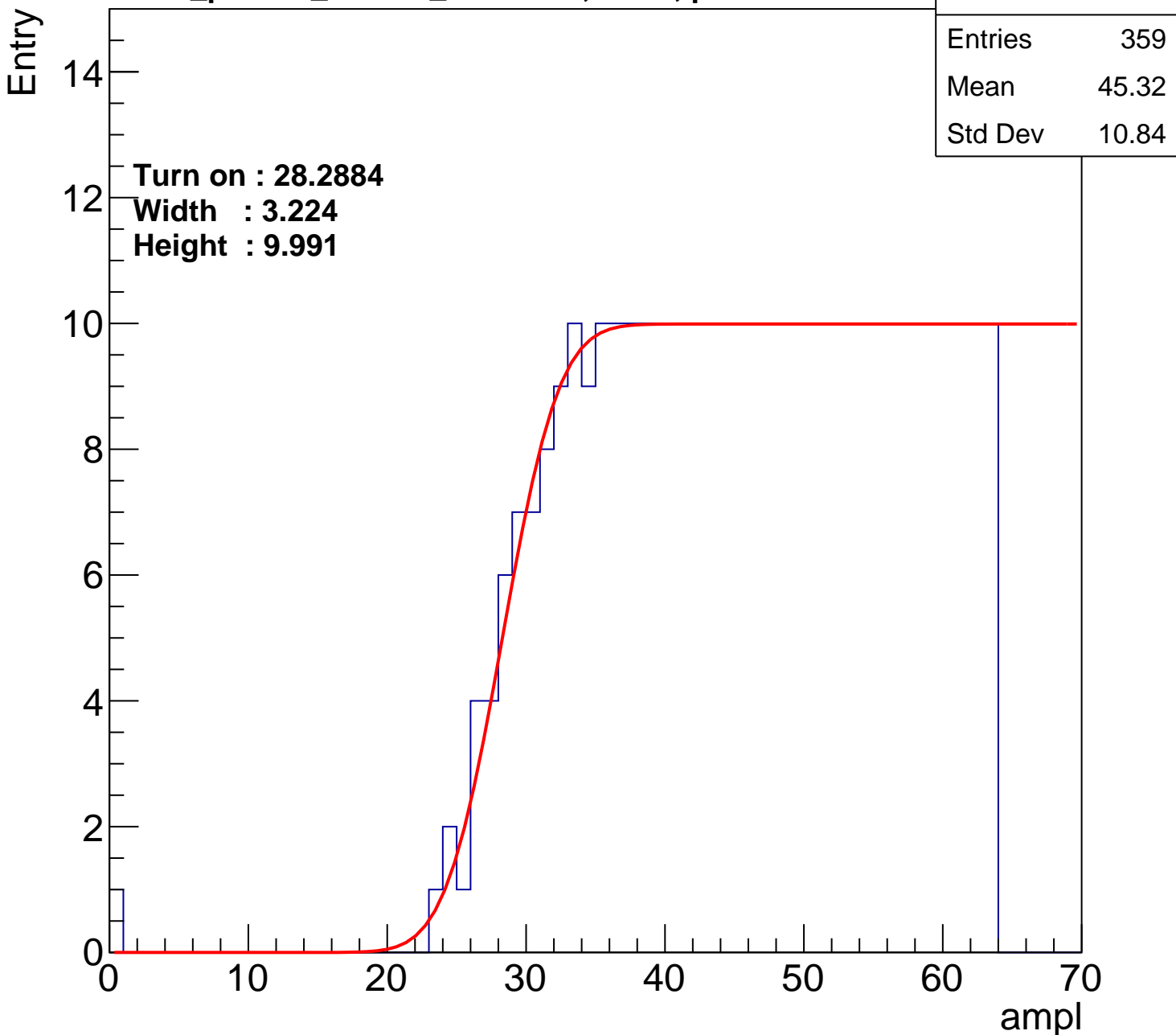
**calib\_packv5\_042523\_0143.root, FC#5, port B1**

**Turn on : 28.2884**

**Width : 3.224**

**Height : 9.991**

Entries	359
Mean	45.32
Std Dev	10.84



# B0L000S, U4-ch102

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	397
Mean	43.49
Std Dev	11.78

Turn on : 24.2795

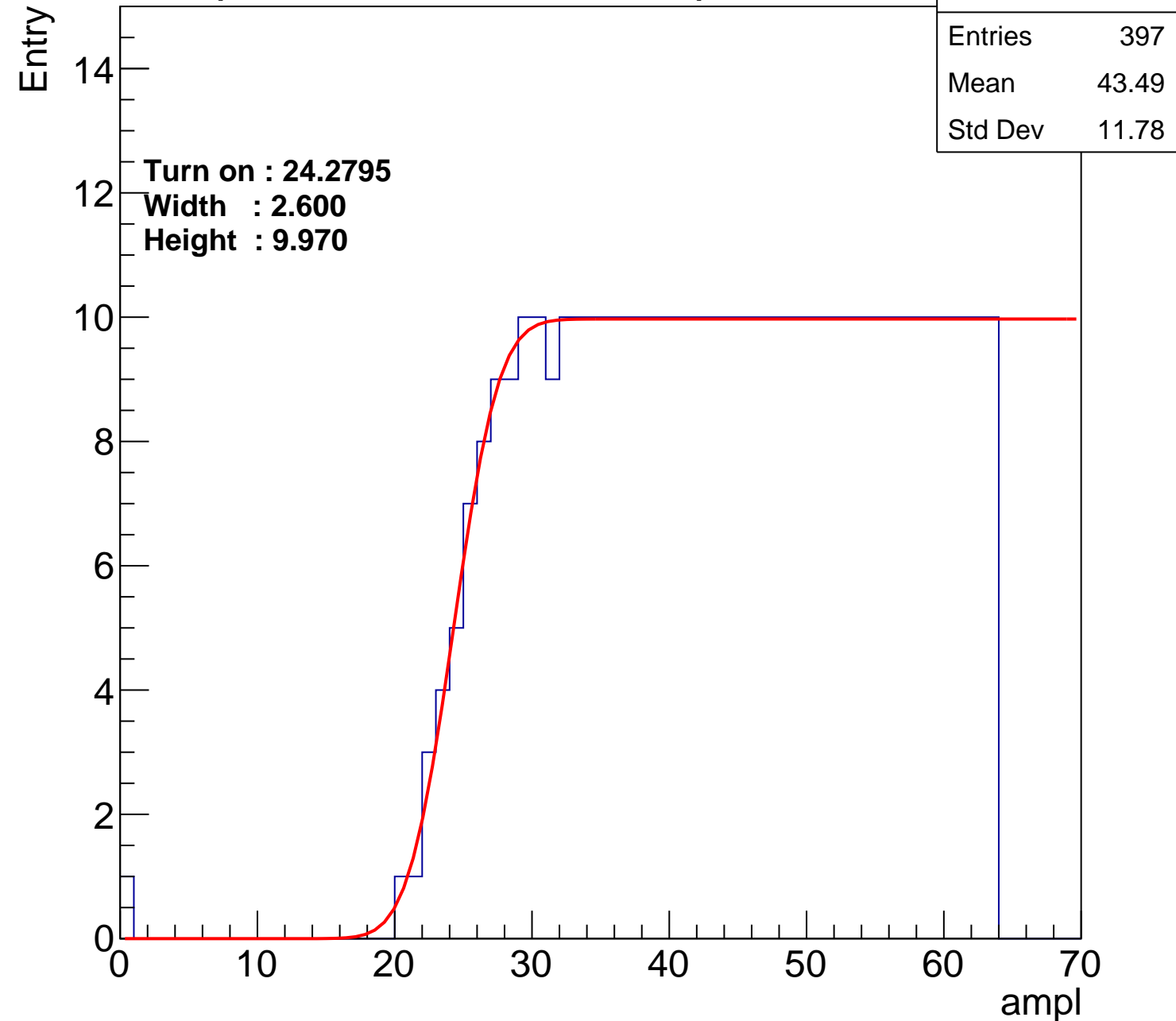
Width : 2.600

Height : 9.970

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L000S, U4-ch103

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	356
Mean	45.33
Std Dev	11.19

**Turn on : 29.4067**

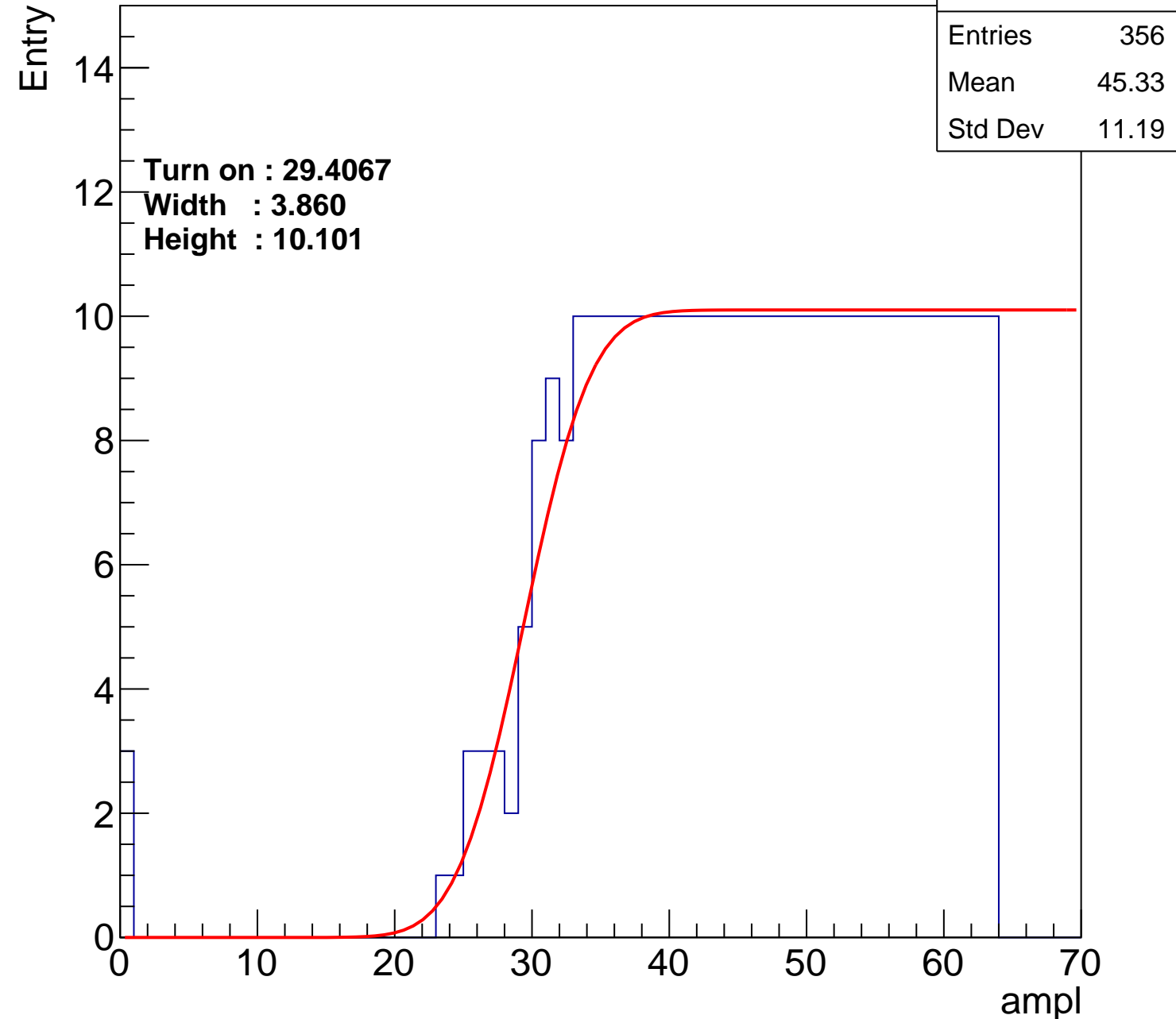
**Width : 3.860**

**Height : 10.101**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch104

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	358
Mean	45.09
Std Dev	11.64

Turn on : 28.8834

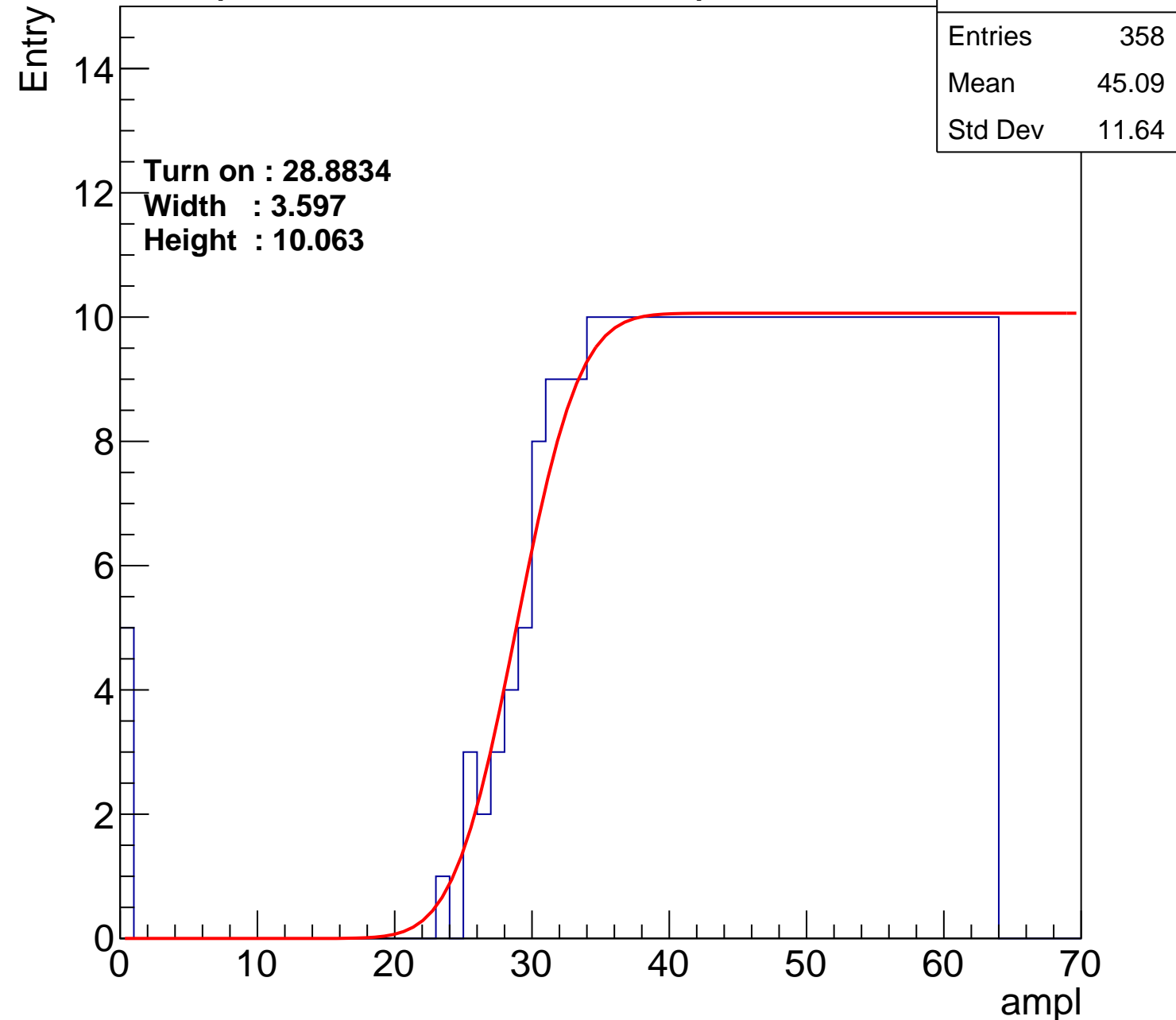
Width : 3.597

Height : 10.063

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch105

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	376
Mean	44.44
Std Dev	11.44

**Turn on : 26.5778**

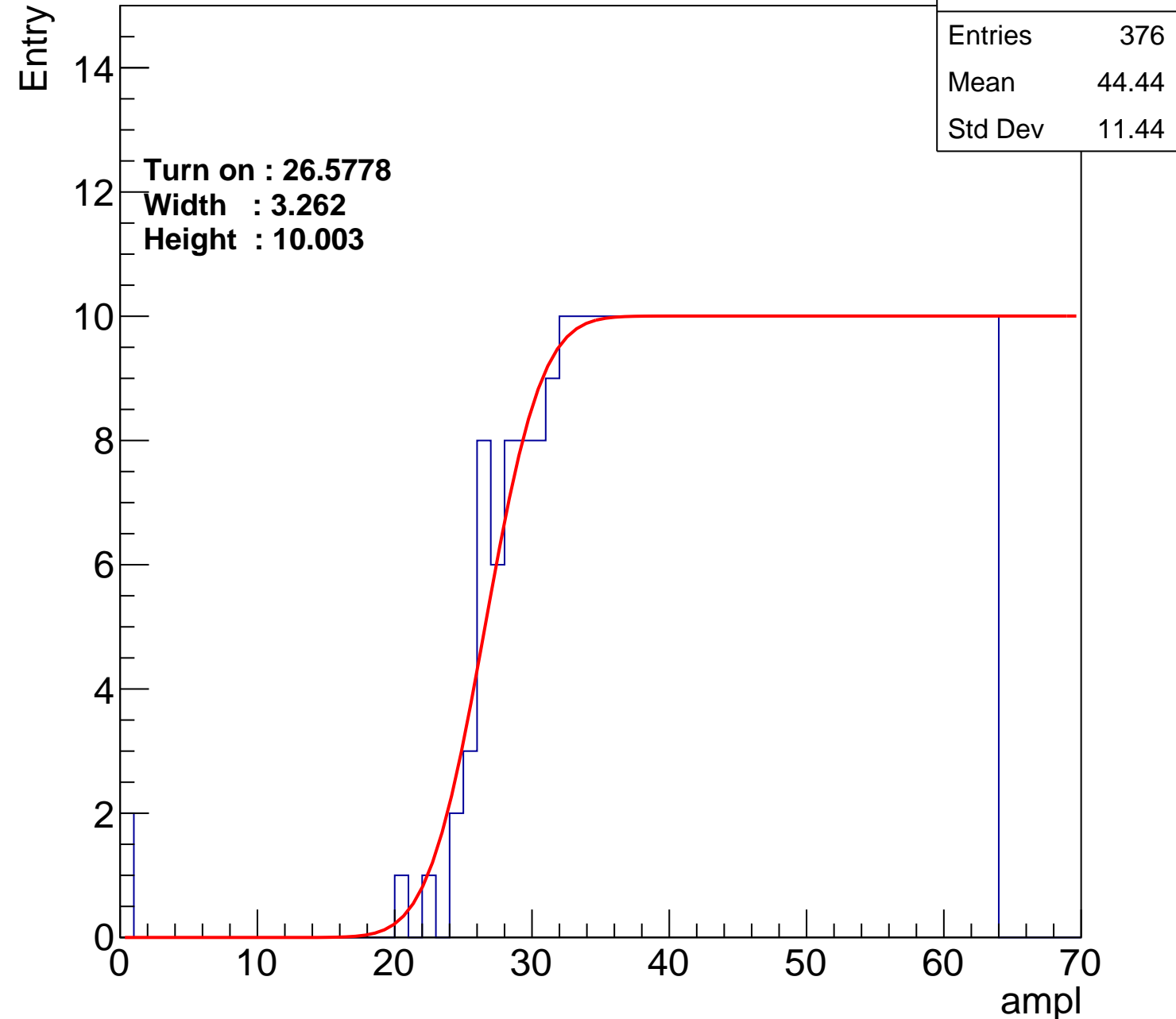
**Width : 3.262**

**Height : 10.003**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch106

calib\_packv5\_042523\_0143.root, FC#5, port B1

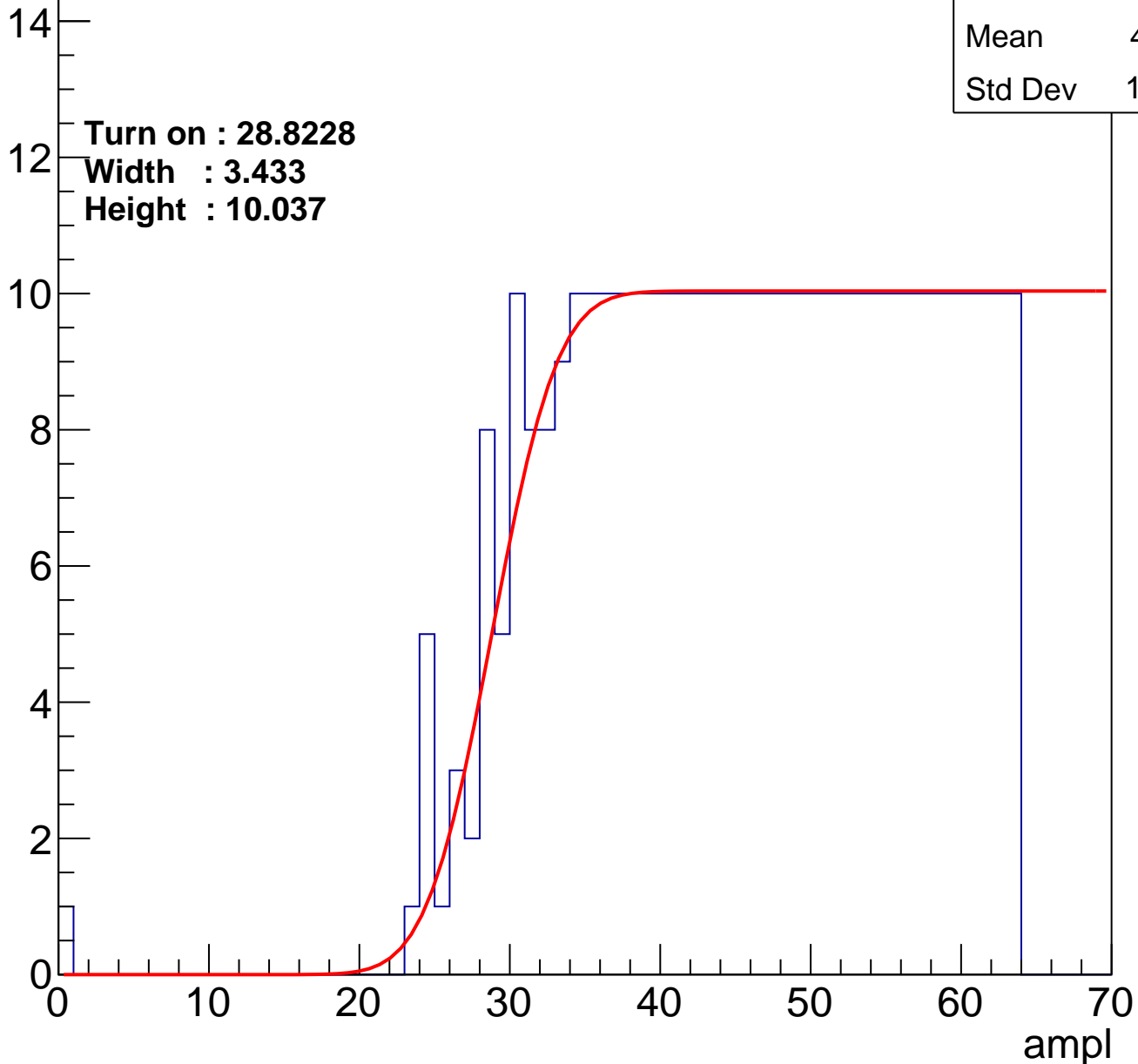
Entries	361
Mean	45.21
Std Dev	10.92

Turn on : 28.8228

Width : 3.433

Height : 10.037

Entry



# B0L000S, U4-ch107

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	365
Mean	44.94
Std Dev	11.31

Turn on : 27.8836

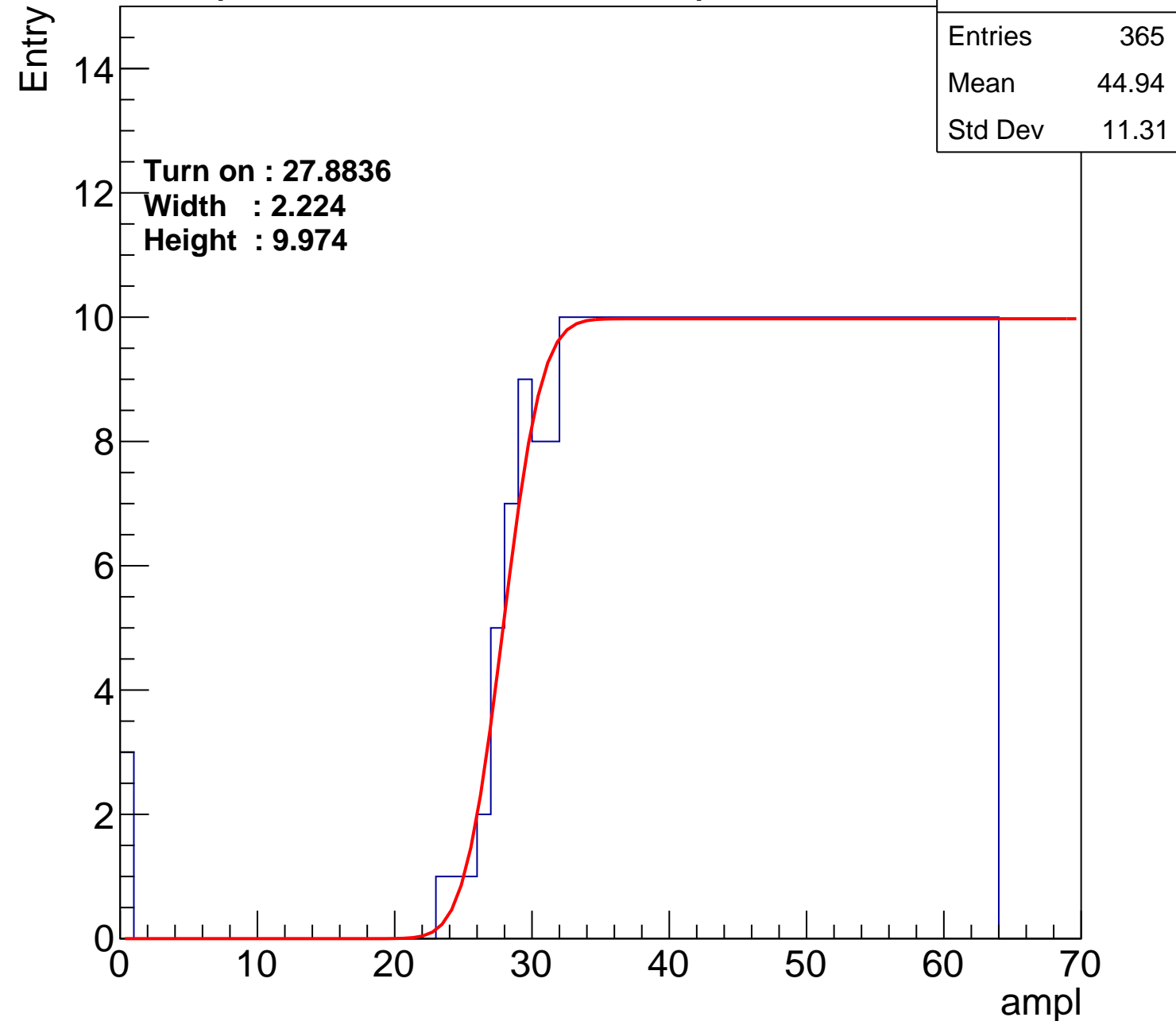
Width : 2.224

Height : 9.974

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch108

calib\_packv5\_042523\_0143.root, FC#5, port B1

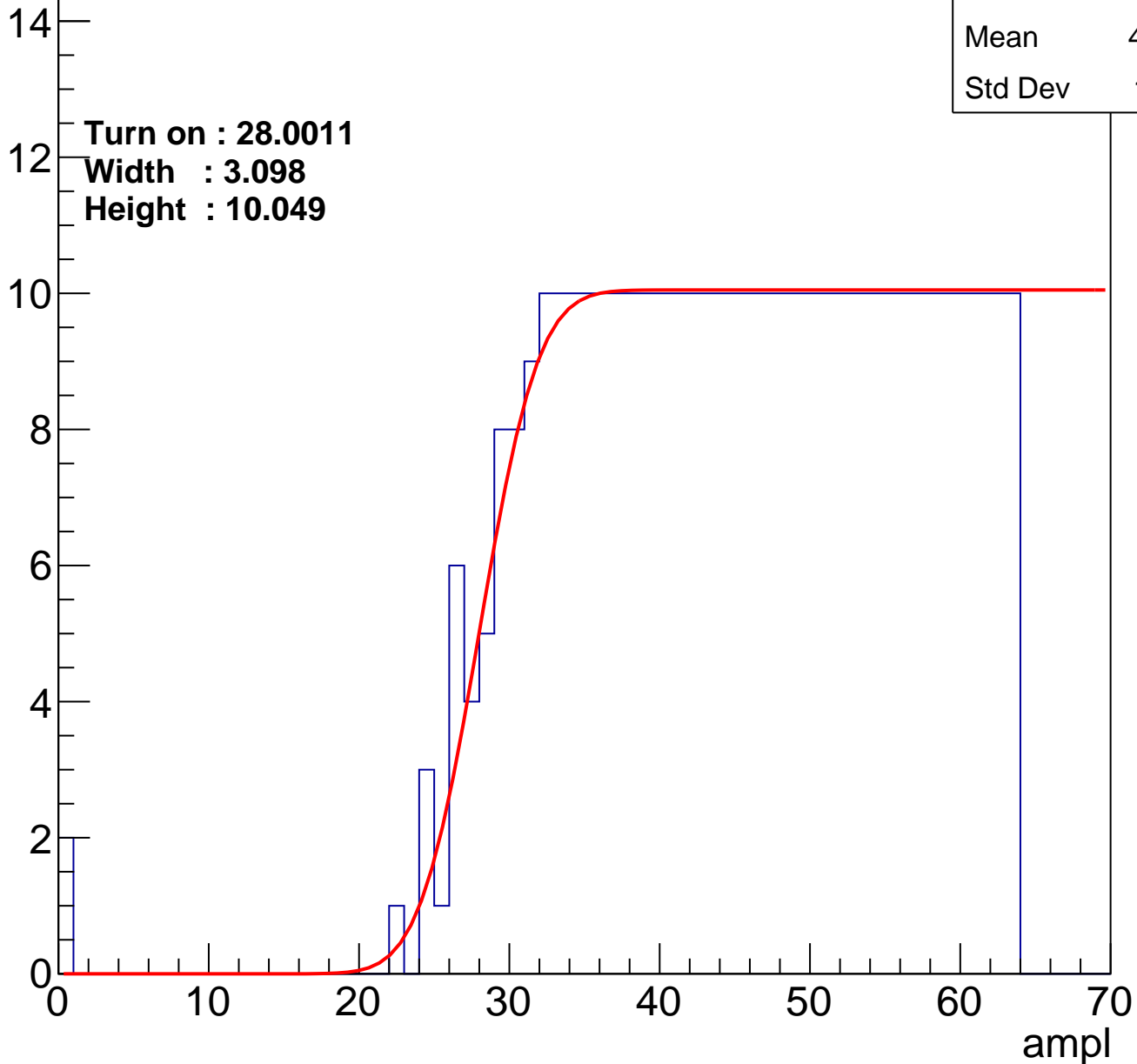
Entries	367
Mean	44.89
Std Dev	11.21

Turn on : 28.0011

Width : 3.098

Height : 10.049

Entry



# B0L000S, U4-ch109

calib\_packv5\_042523\_0143.root, FC#5, port B1

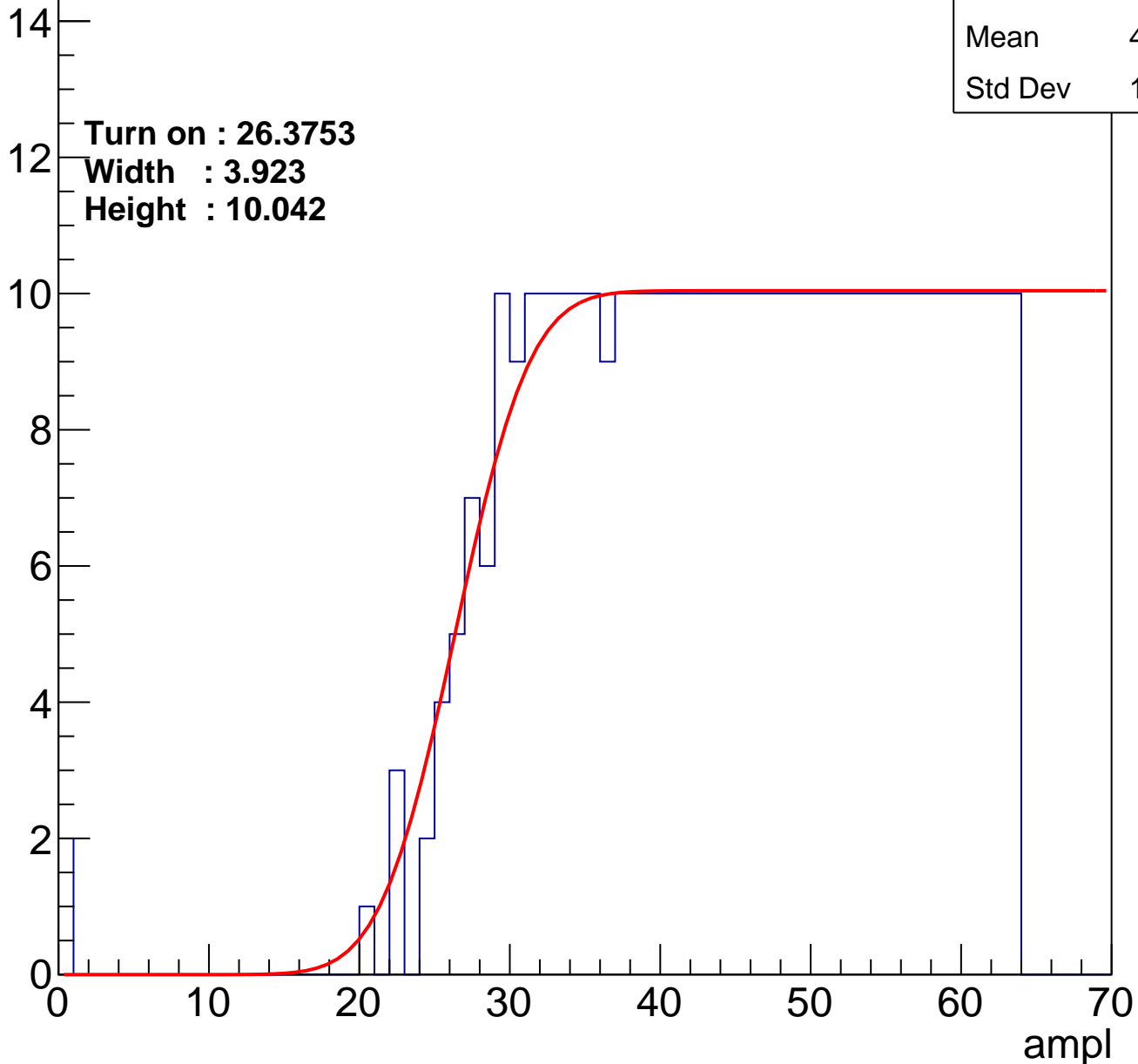
Entries	378
Mean	44.33
Std Dev	11.52

**Turn on : 26.3753**

**Width : 3.923**

**Height : 10.042**

Entry



# B0L000S, U4-ch110

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	381
Mean	44.06
Std Dev	11.93

Turn on : 26.6519

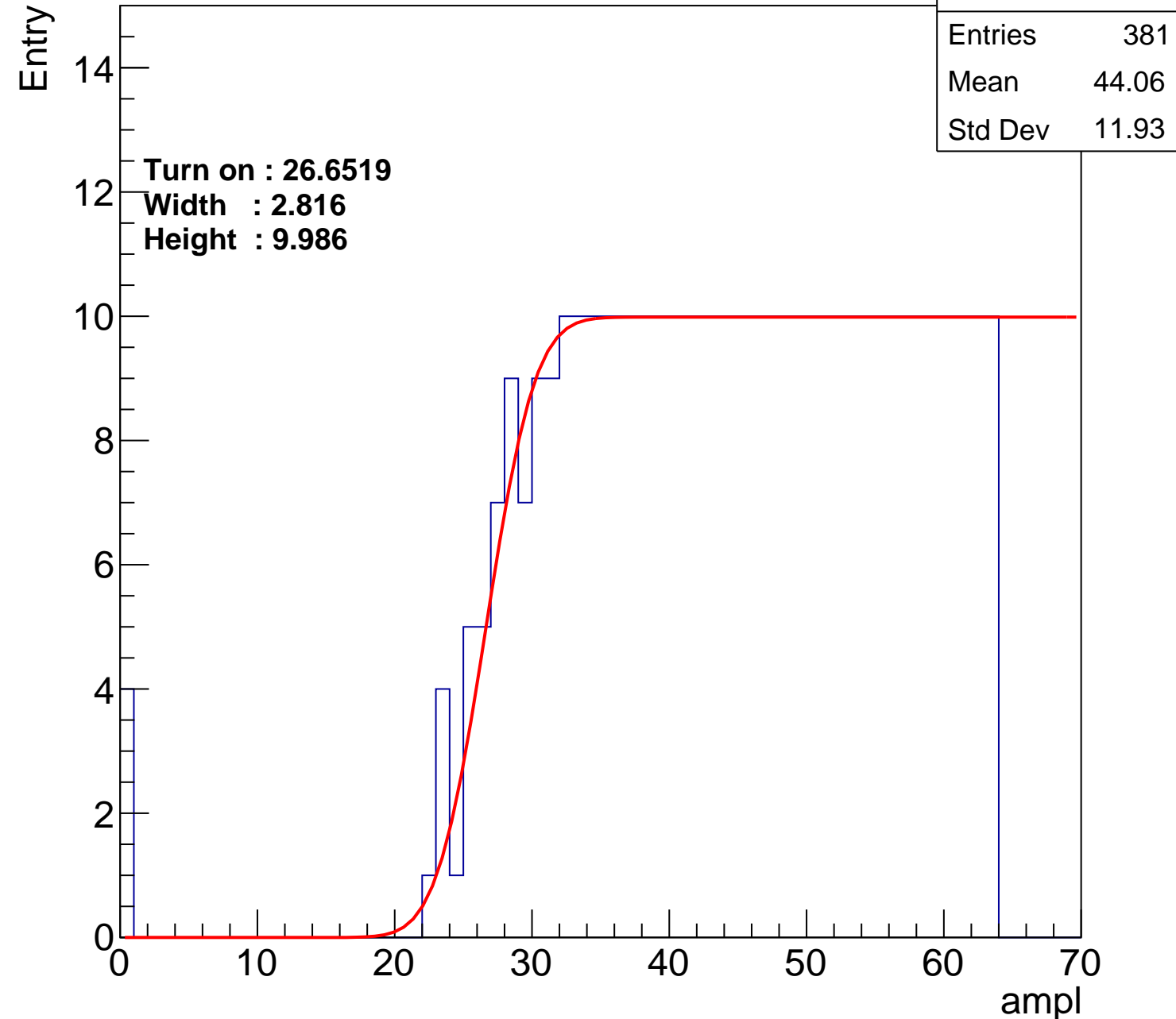
Width : 2.816

Height : 9.986

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L000S, U4-ch111

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	371
Mean	44.61
Std Dev	11.51

**Turn on : 27.2194**

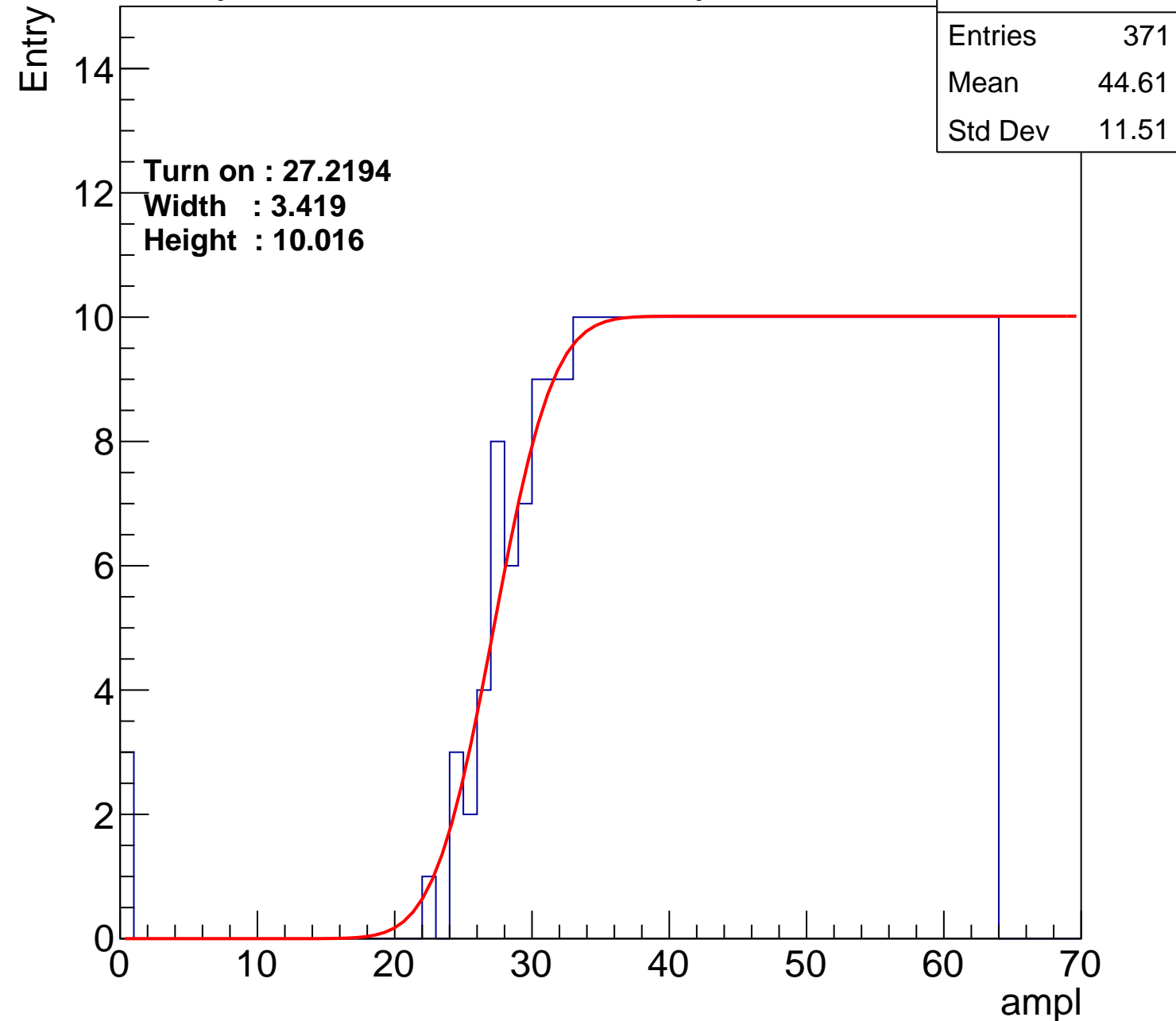
**Width : 3.419**

**Height : 10.016**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch112

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	369
Mean	44.4
Std Dev	12.25

Turn on : 27.6936

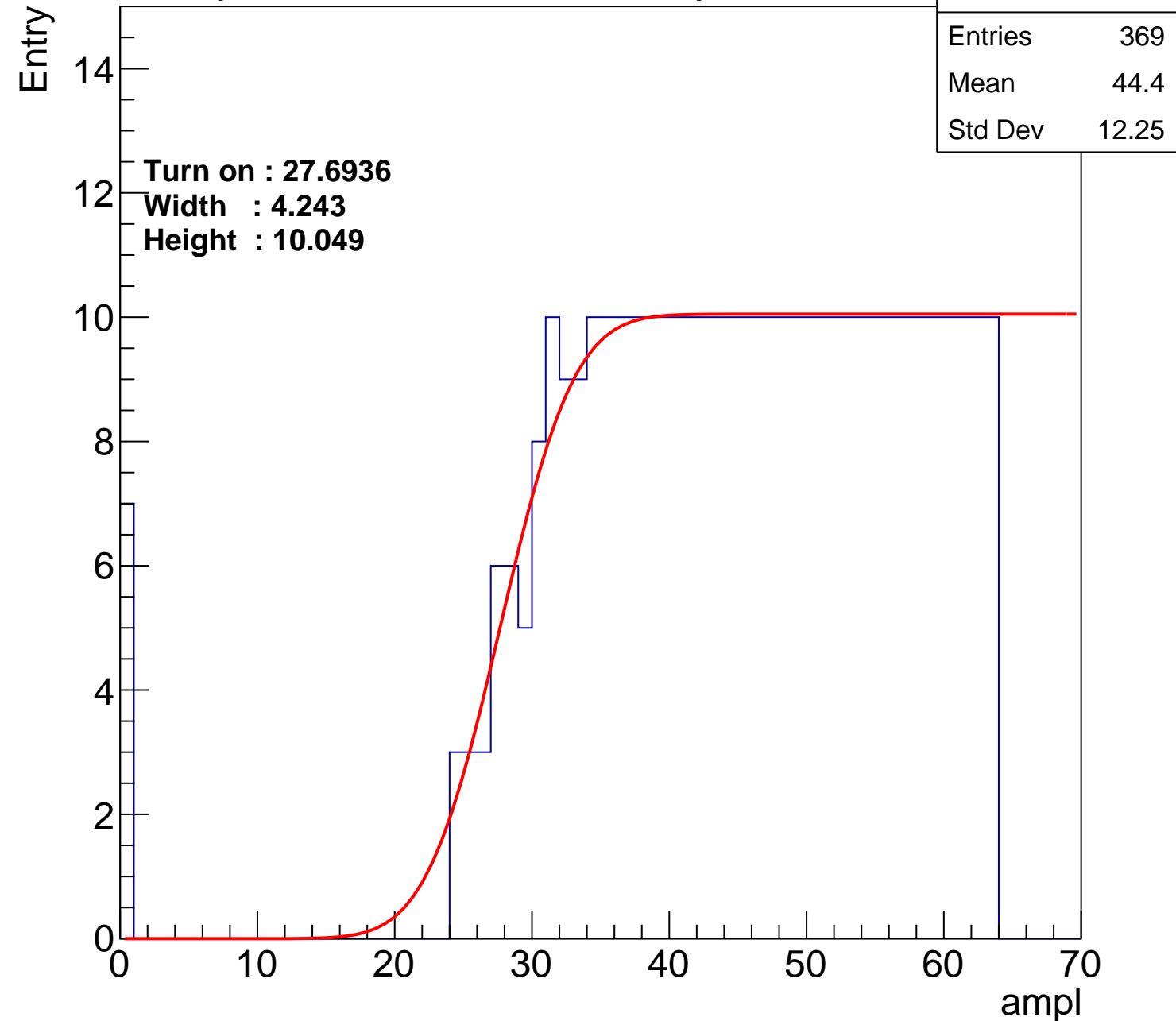
Width : 4.243

Height : 10.049

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch113

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	372
Mean	44.57
Std Dev	11.52

**Turn on : 27.1307**

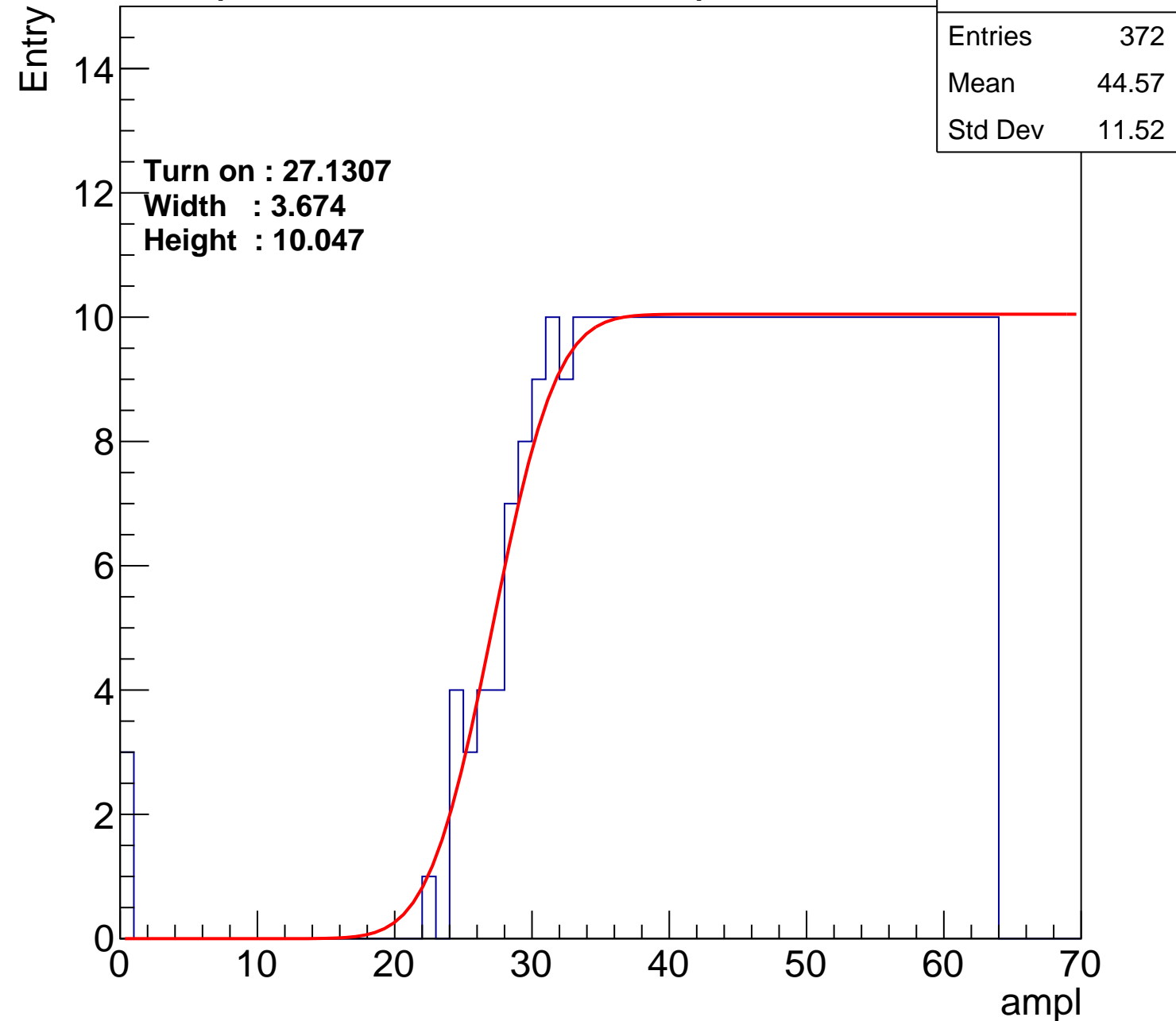
**Width : 3.674**

**Height : 10.047**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch114

calib\_packv5\_042523\_0143.root, FC#5, port B1

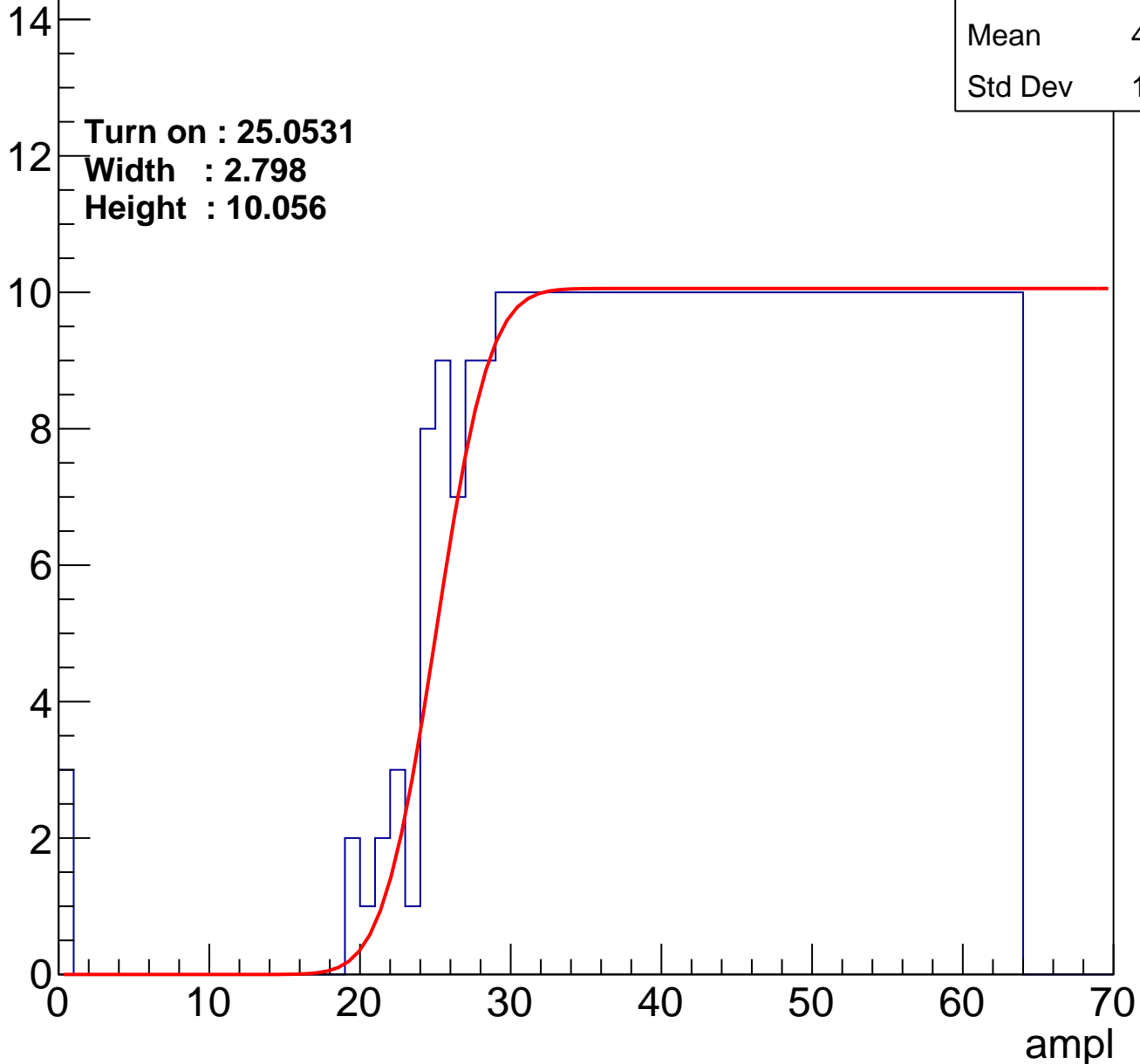
Entries	404
Mean	43.03
Std Dev	12.28

Turn on : 25.0531

Width : 2.798

Height : 10.056

Entry



# B0L000S, U4-ch115

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	355
Mean	45.37
Std Dev	11.17

**Turn on : 29.0278**

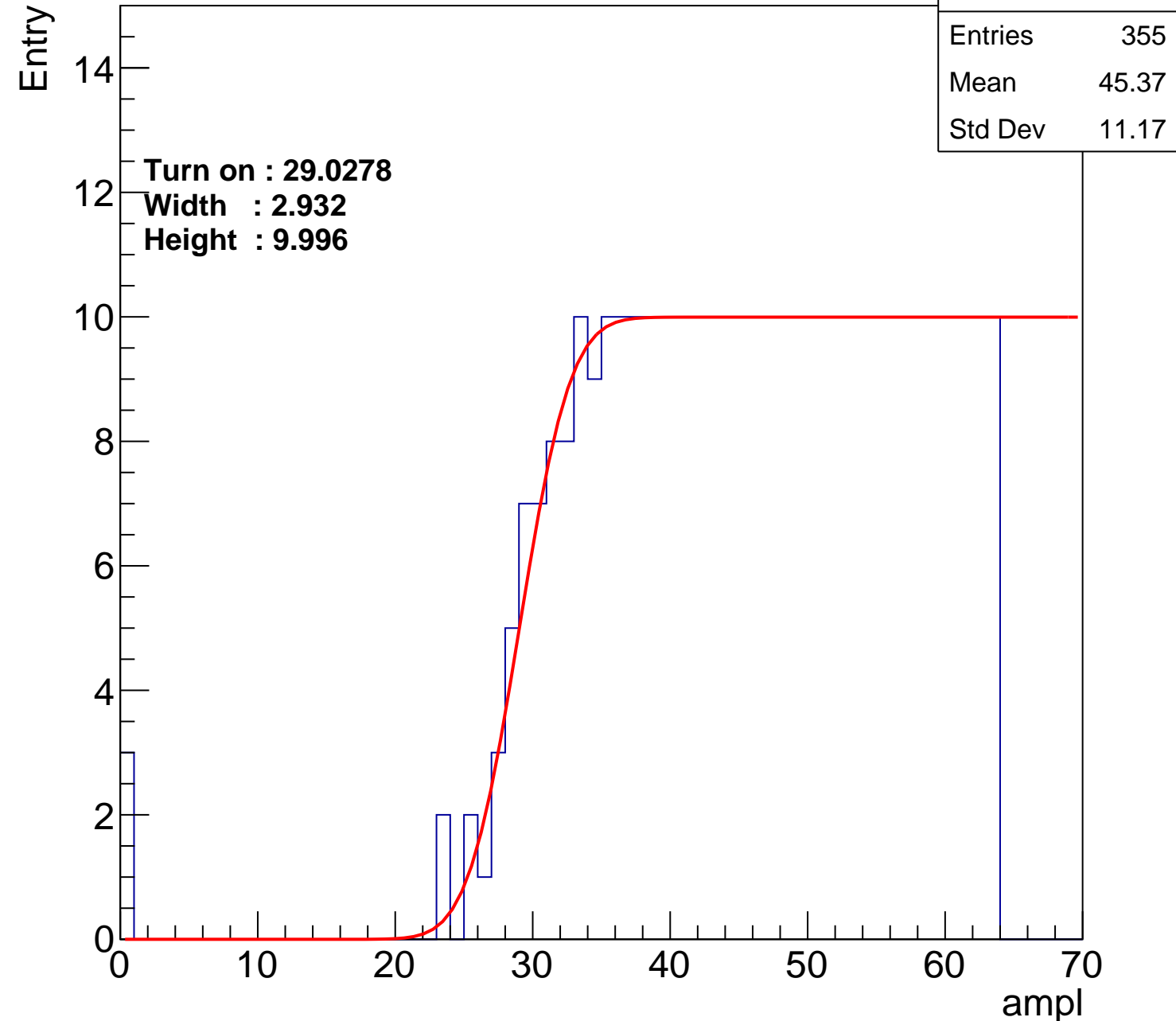
**Width : 2.932**

**Height : 9.996**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch116

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	383
Mean	44.07
Std Dev	11.74

Turn on : 26.5322

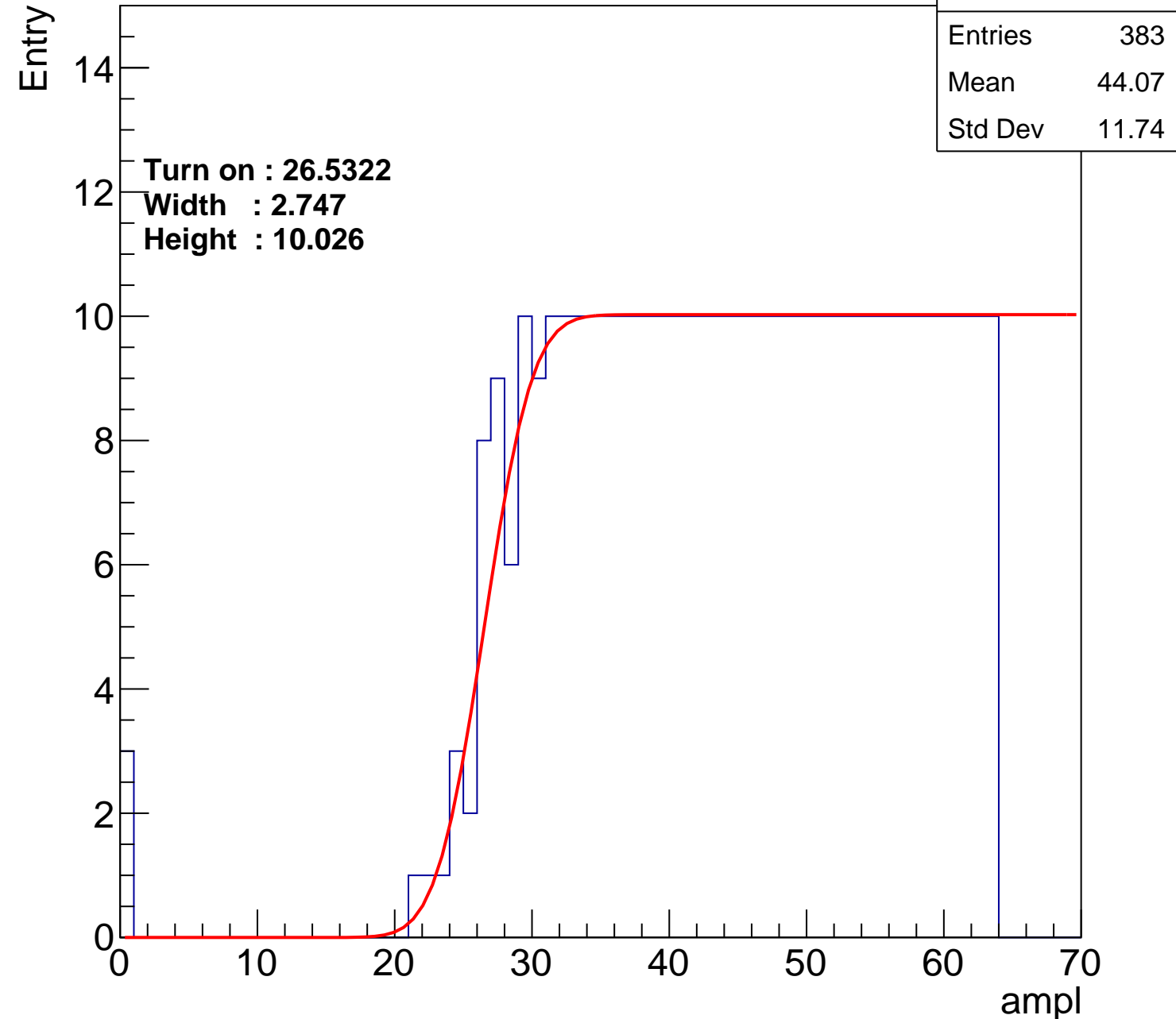
Width : 2.747

Height : 10.026

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch117

calib\_packv5\_042523\_0143.root, FC#5, port B1

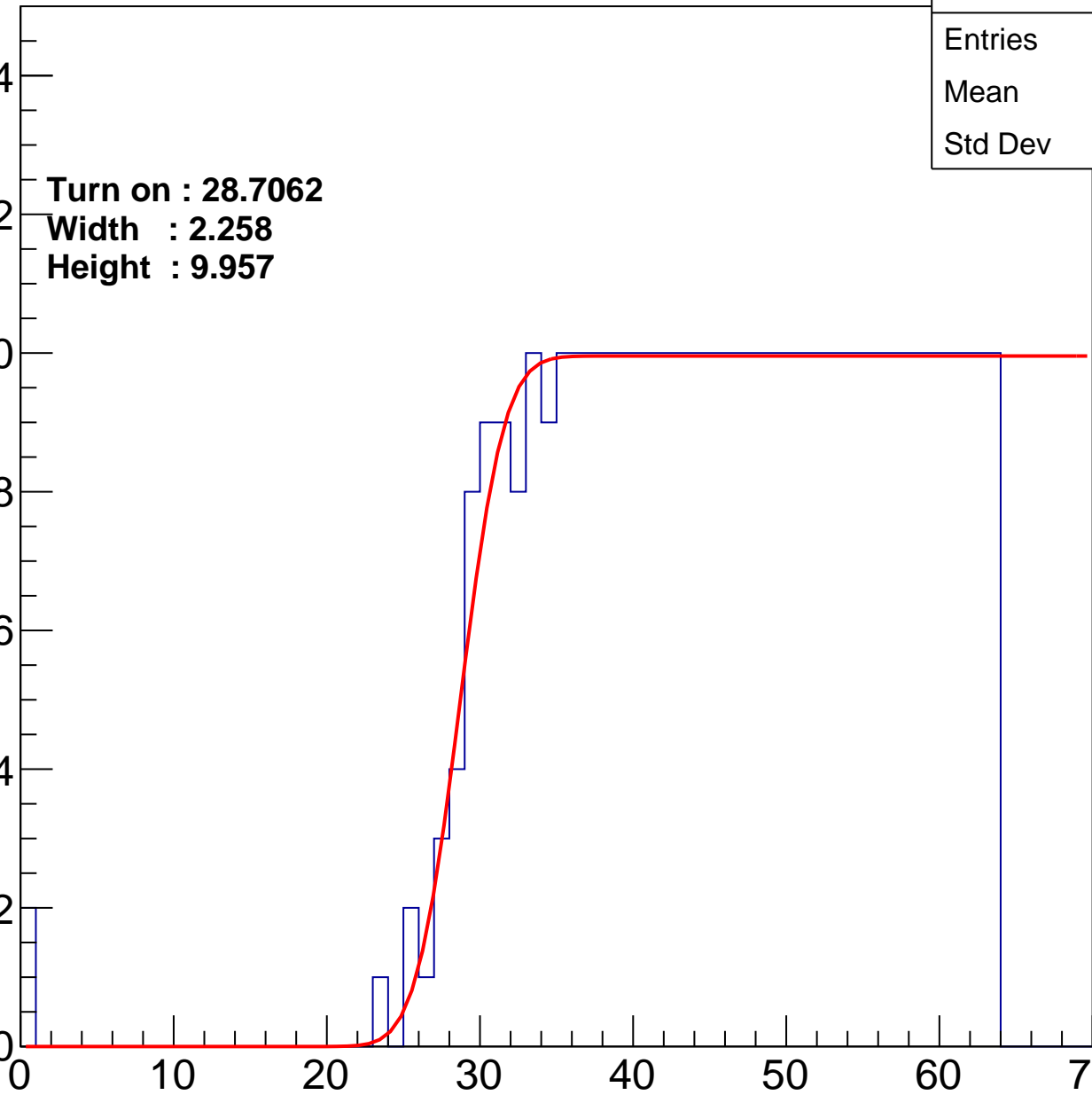
Entry

14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 28.7062**  
**Width : 2.258**  
**Height : 9.957**

Entries	356
Mean	45.44
Std Dev	10.92

ampl



# B0L000S, U4-ch118

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	357
Mean	45.38
Std Dev	10.97

**Turn on : 28.4749**

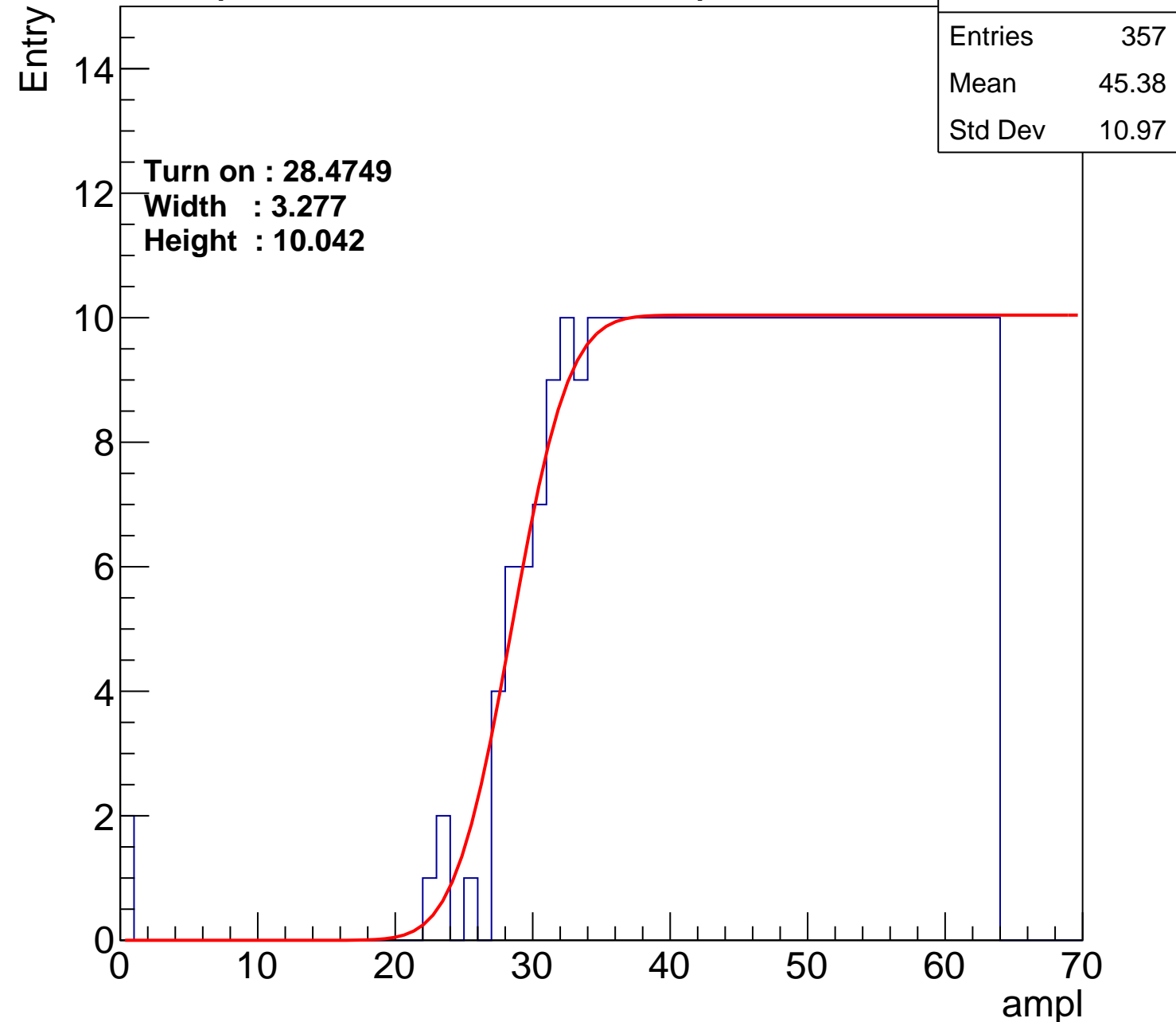
**Width : 3.277**

**Height : 10.042**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





**calib\_packv5\_042523\_0143.root, FC#5, port B1**

**calib\_packv5\_042523\_0143.root, FC#5, port B1**

Turn on : 26.6296  
Width : 4.211  
Height : 10.059



# B0L000S, U4-ch120

calib\_packv5\_042523\_0143.root, FC#5, port B1

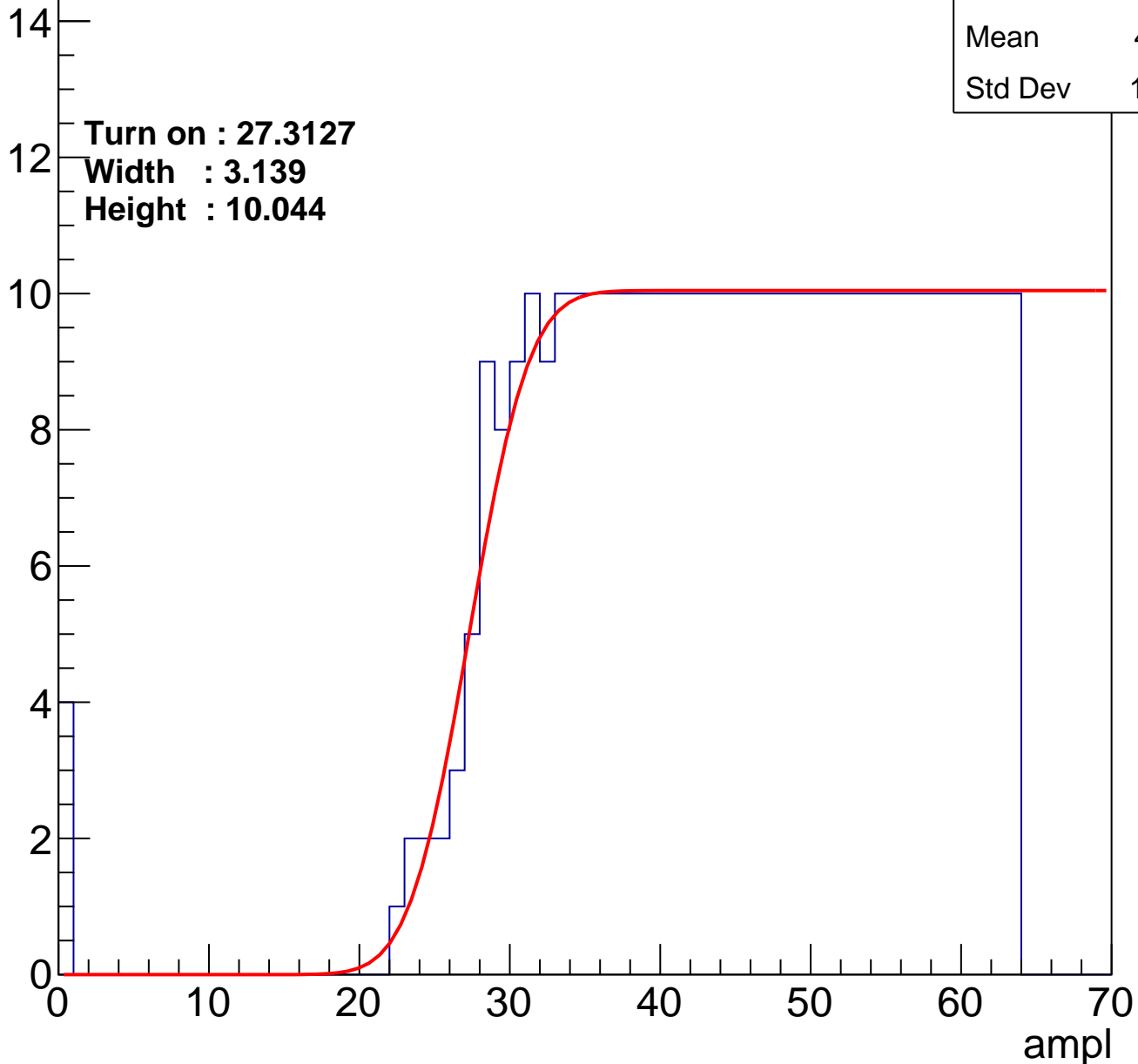
Entries	374
Mean	44.41
Std Dev	11.75

Turn on : 27.3127

Width : 3.139

Height : 10.044

Entry



# B0L000S, U4-ch121

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	357
Mean	45.3
Std Dev	11.18

Turn on : 28.9623

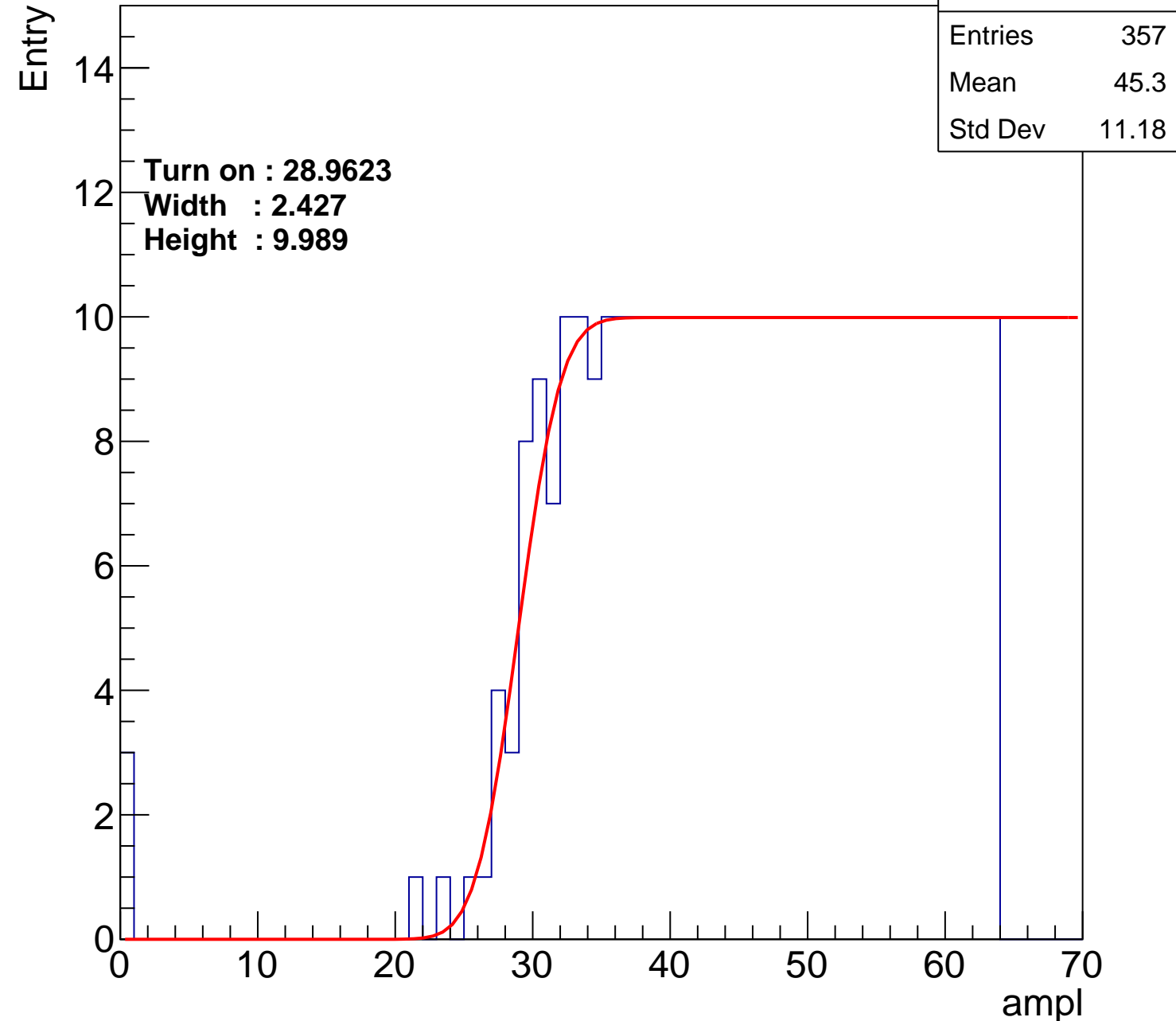
Width : 2.427

Height : 9.989

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch122

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	382
Mean	44.03
Std Dev	11.92

Turn on : 26.1012

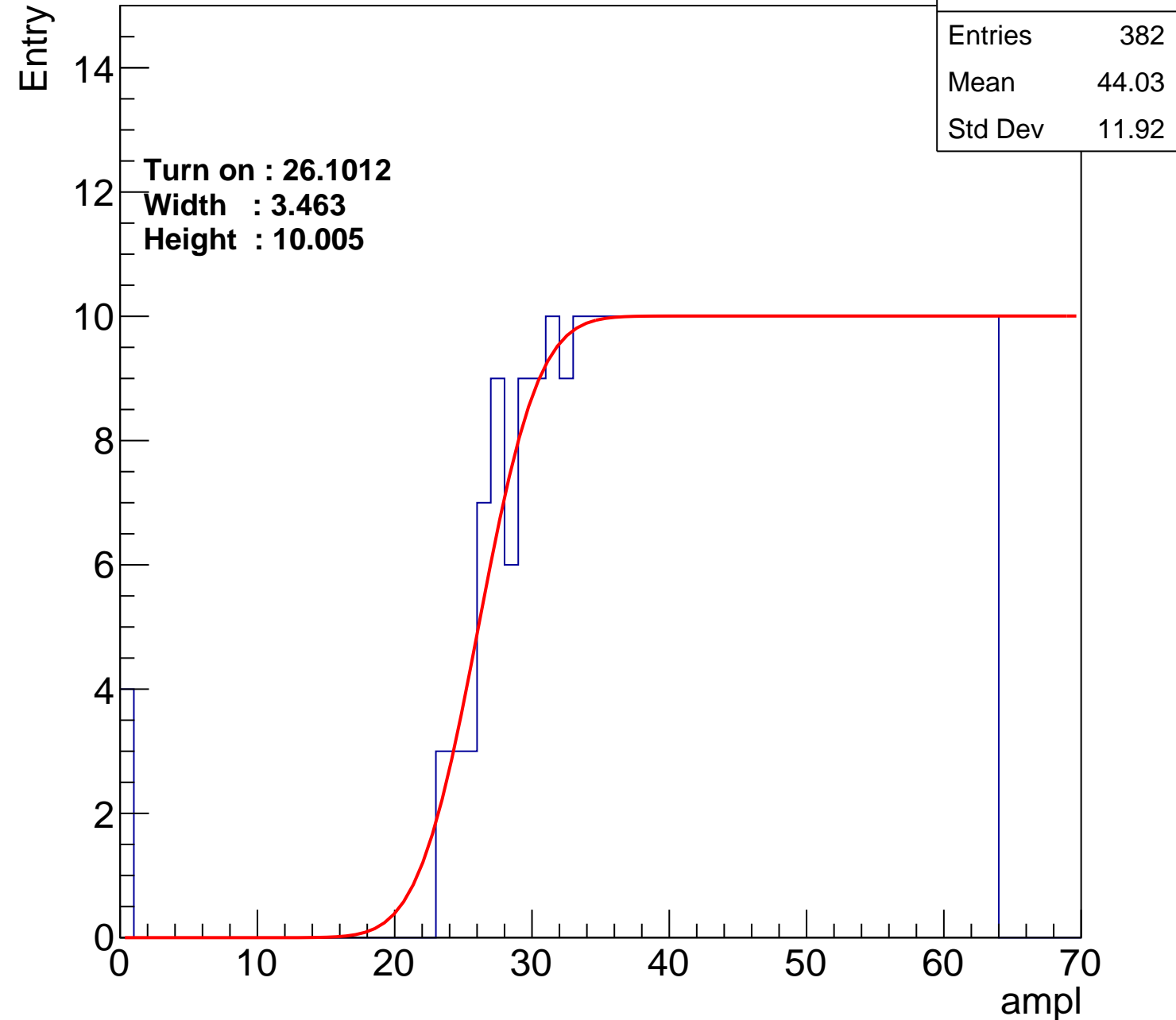
Width : 3.463

Height : 10.005

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U4-ch123

calib\_packv5\_042523\_0143.root, FC#5, port B1

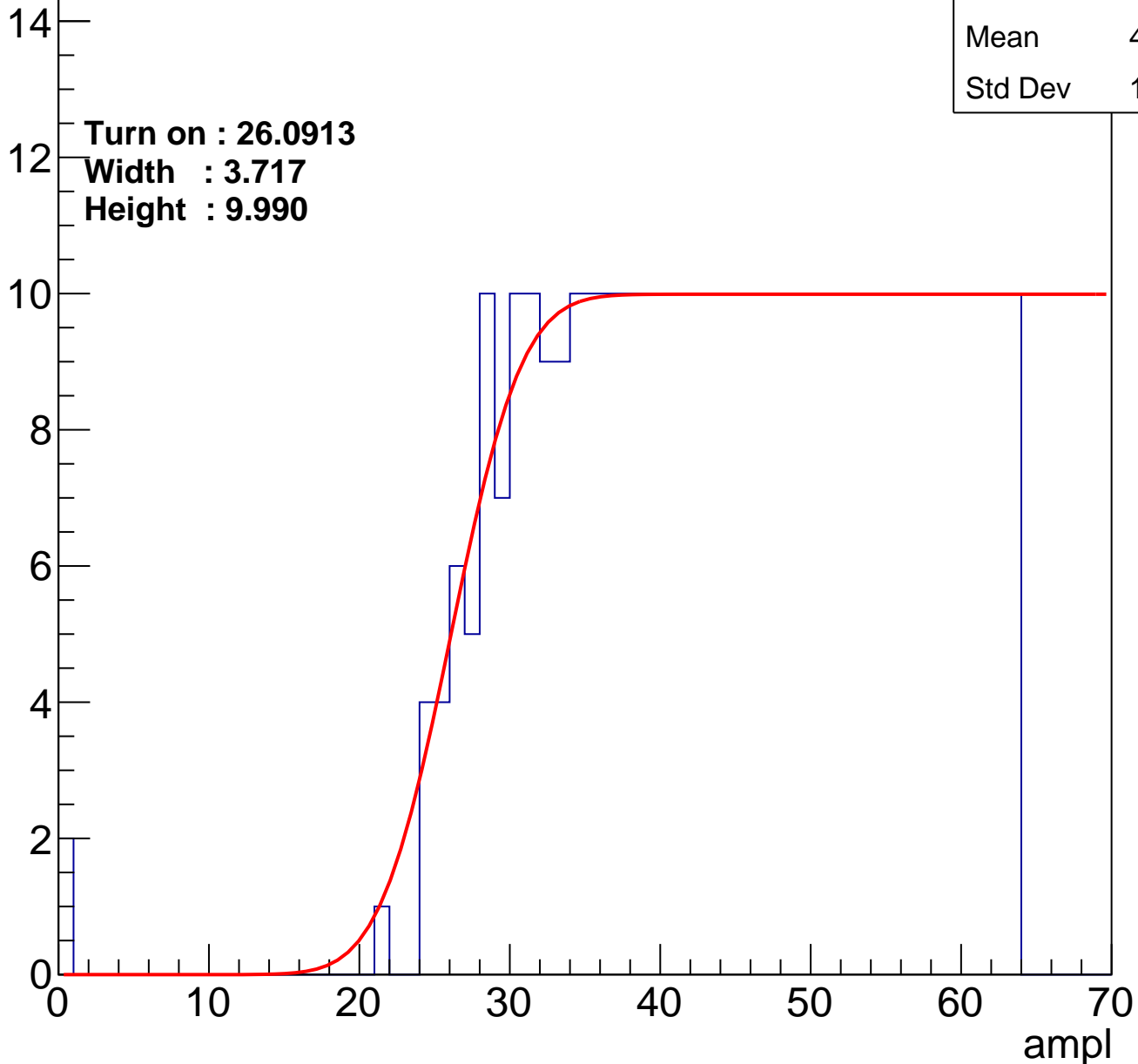
Entries	377
Mean	44.39
Std Dev	11.46

Turn on : 26.0913

Width : 3.717

Height : 9.990

Entry



# B0L000S, U4-ch124

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	370
Mean	44.75
Std Dev	11.26

Turn on : 27.2723

Width : 3.578

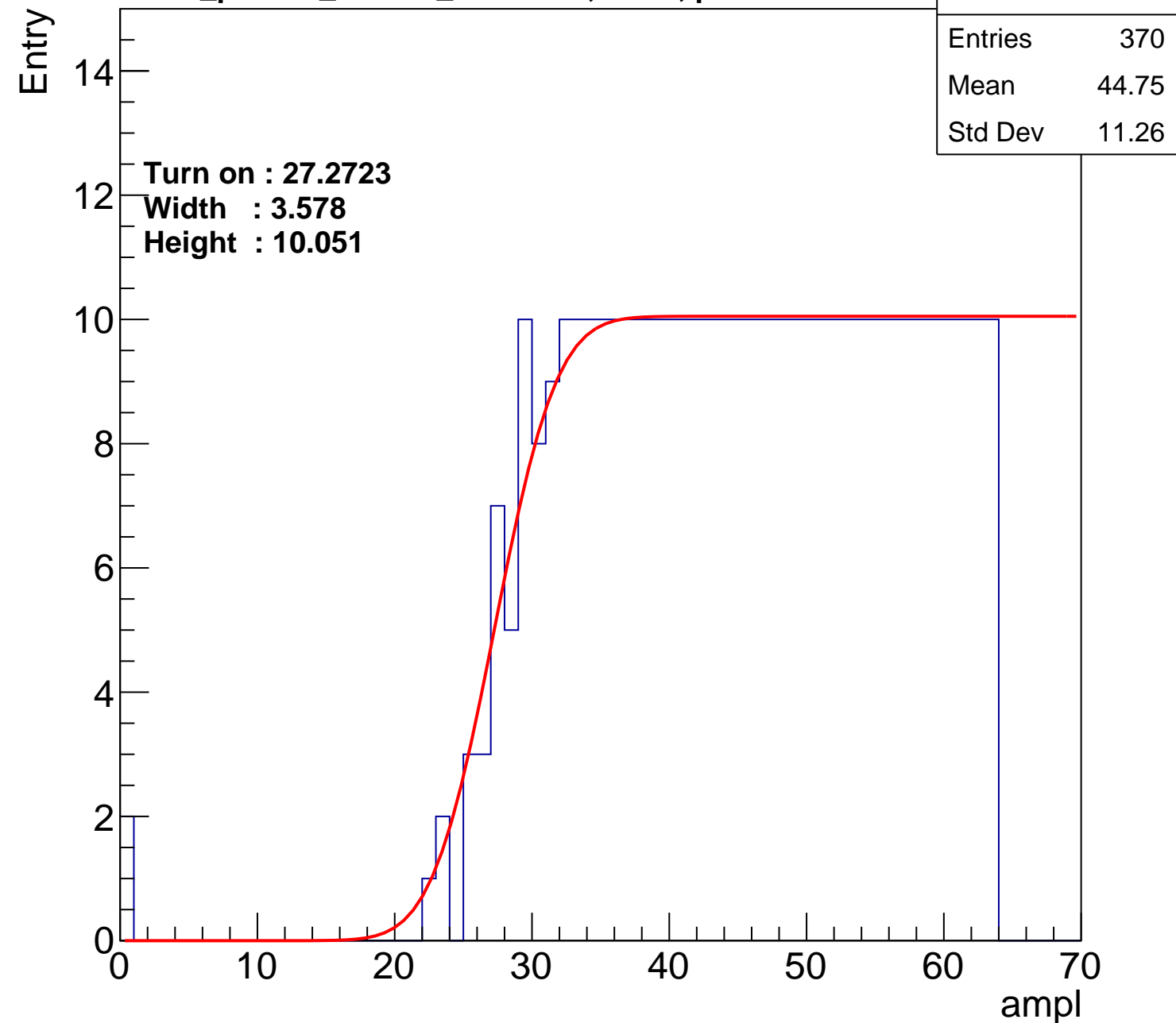
Height : 10.051

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L000S, U4-ch125

calib\_packv5\_042523\_0143.root, FC#5, port B1

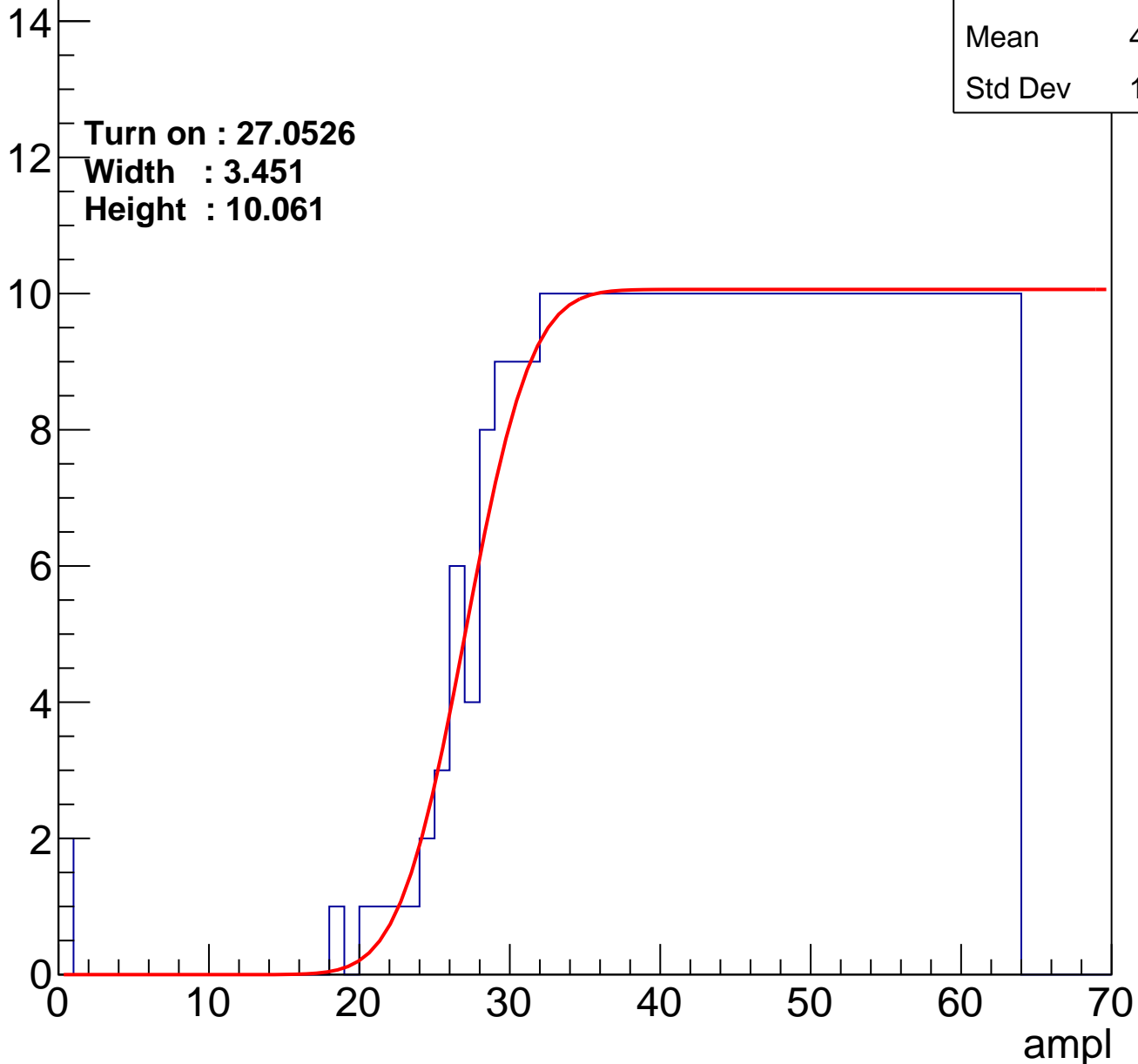
Entries	377
Mean	44.36
Std Dev	11.52

Turn on : 27.0526

Width : 3.451

Height : 10.061

Entry



# B0L000S, U4-ch126

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	376
Mean	44.52
Std Dev	11.23

Turn on : 26.9251

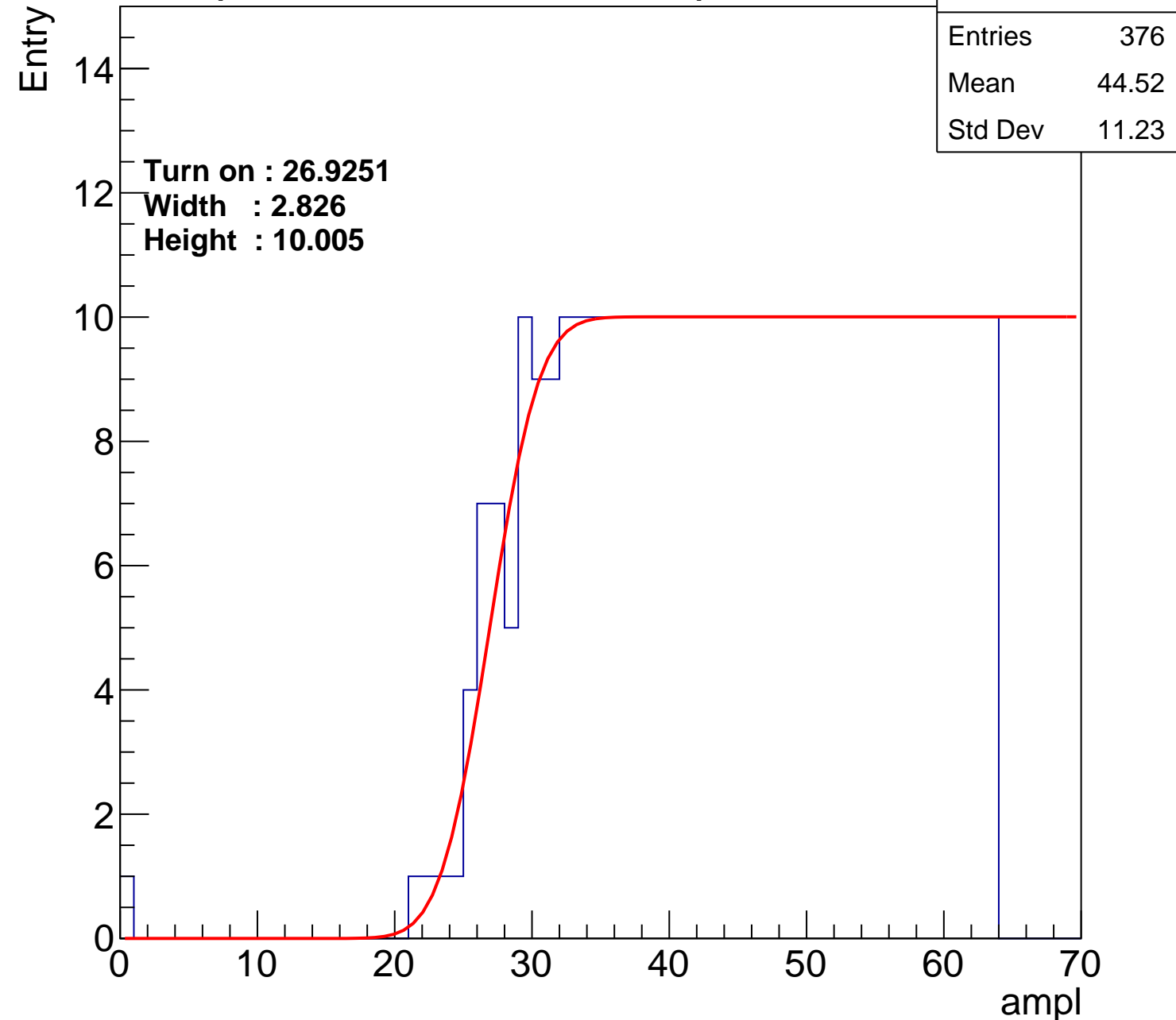
Width : 2.826

Height : 10.005

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L000S, U4-ch127

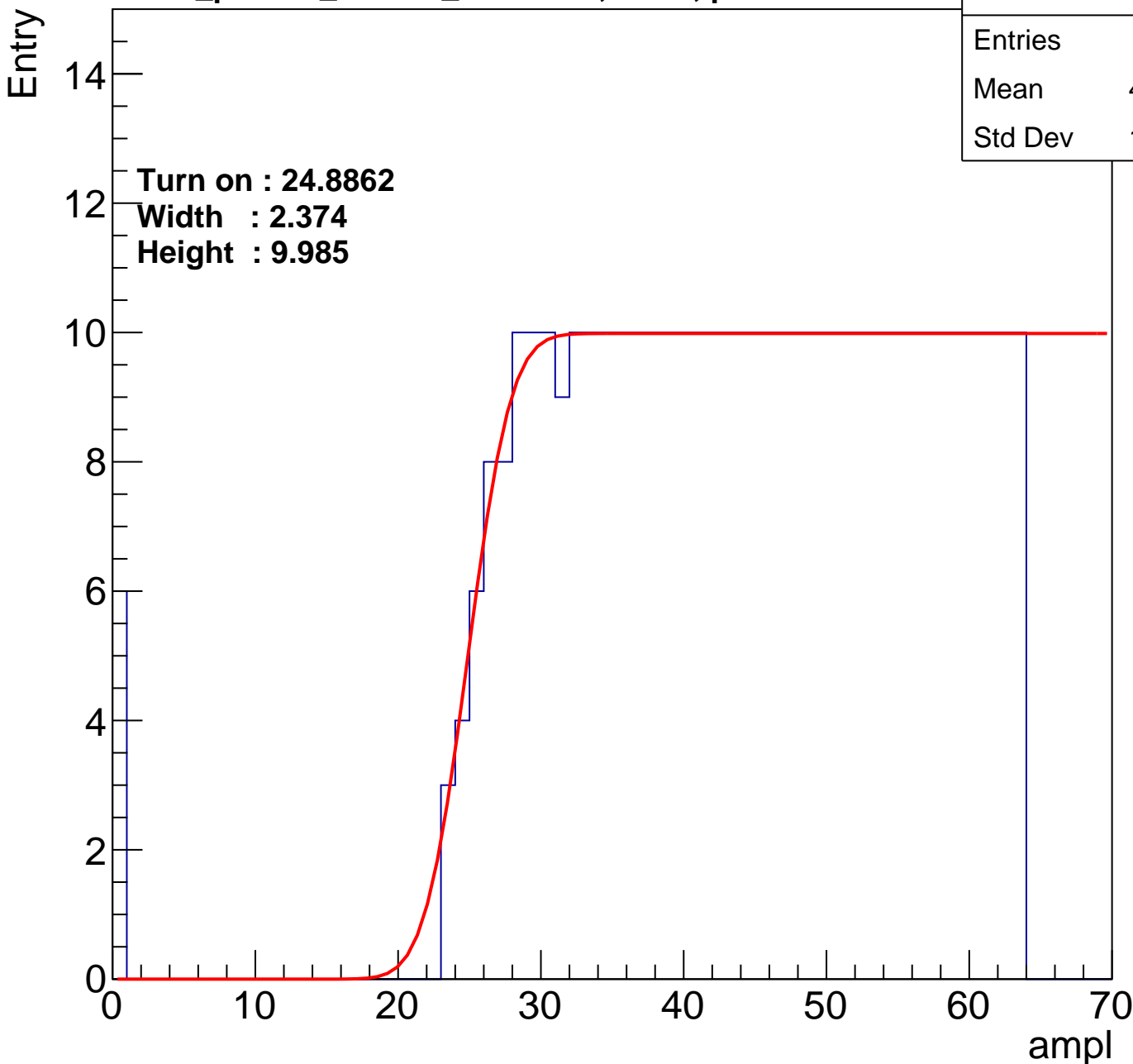
**calib\_packv5\_042523\_0143.root, FC#5, port B1**

Entries	394
Mean	43.37
Std Dev	12.44

**Turn on : 24.8862**

**Width : 2.374**

**Height : 9.985**



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