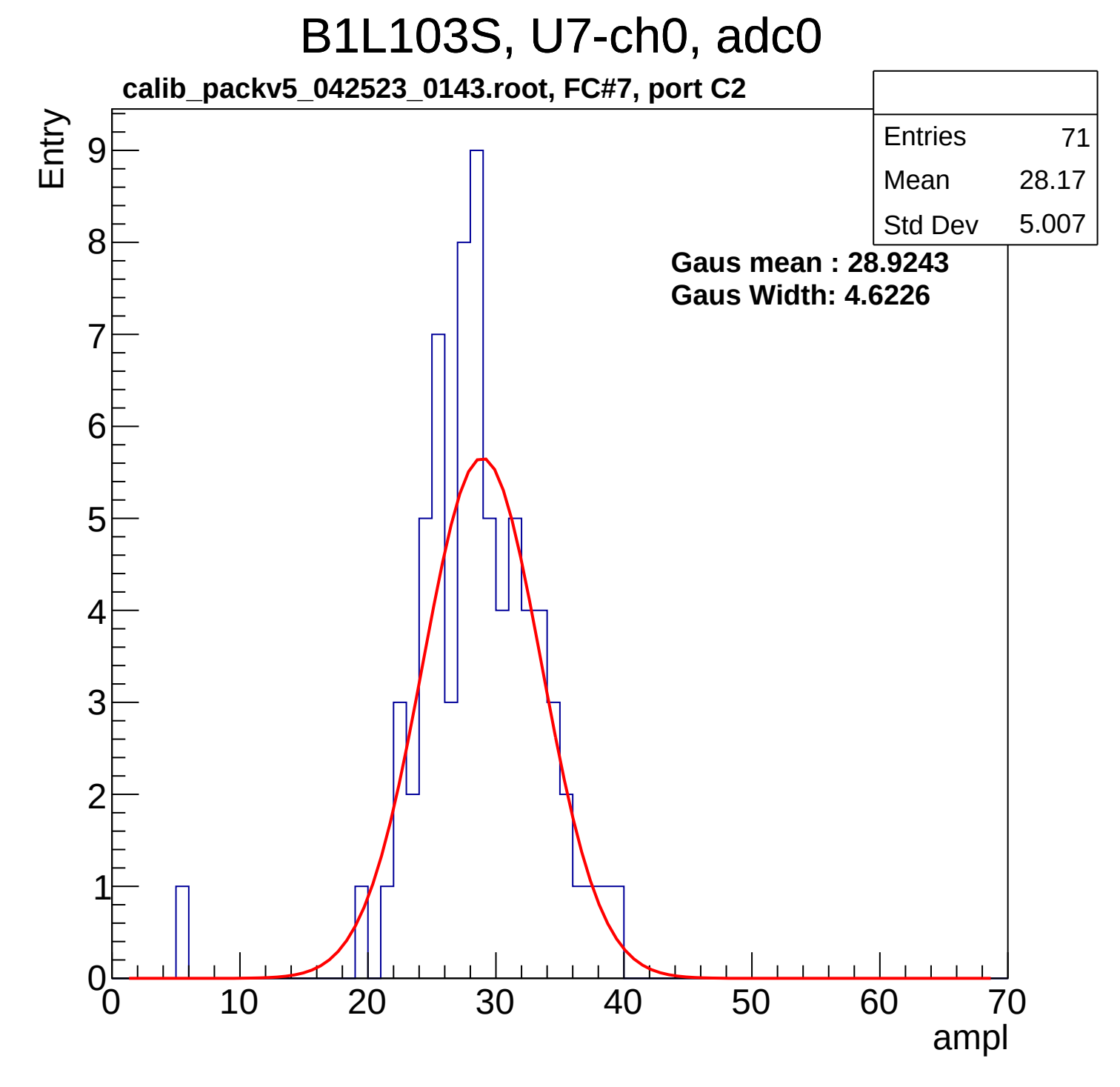
B1L103S, U7-ch0, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 71
Mean 28.17
Std Dev 5.007
Gaus mean : 28.9243
Gaus Width: 4.6226
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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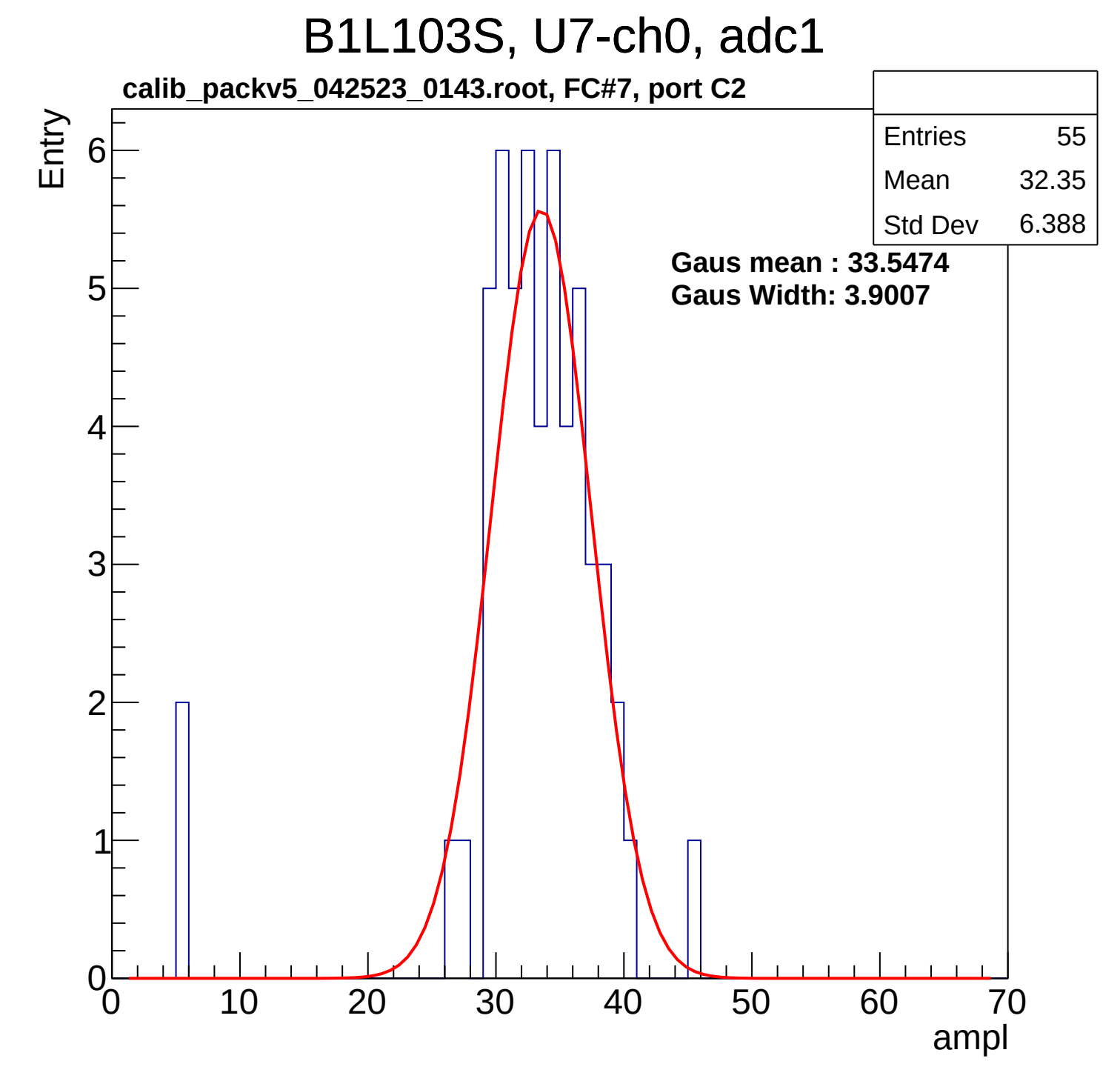
B1L103S, U7-ch0, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 32.35
Std Dev 6.388
Gaus mean : 33.5474
Gaus Width: 3.9007
Entry
ampl
0
1
2
3
4
5
6
0
10
20
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40
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60
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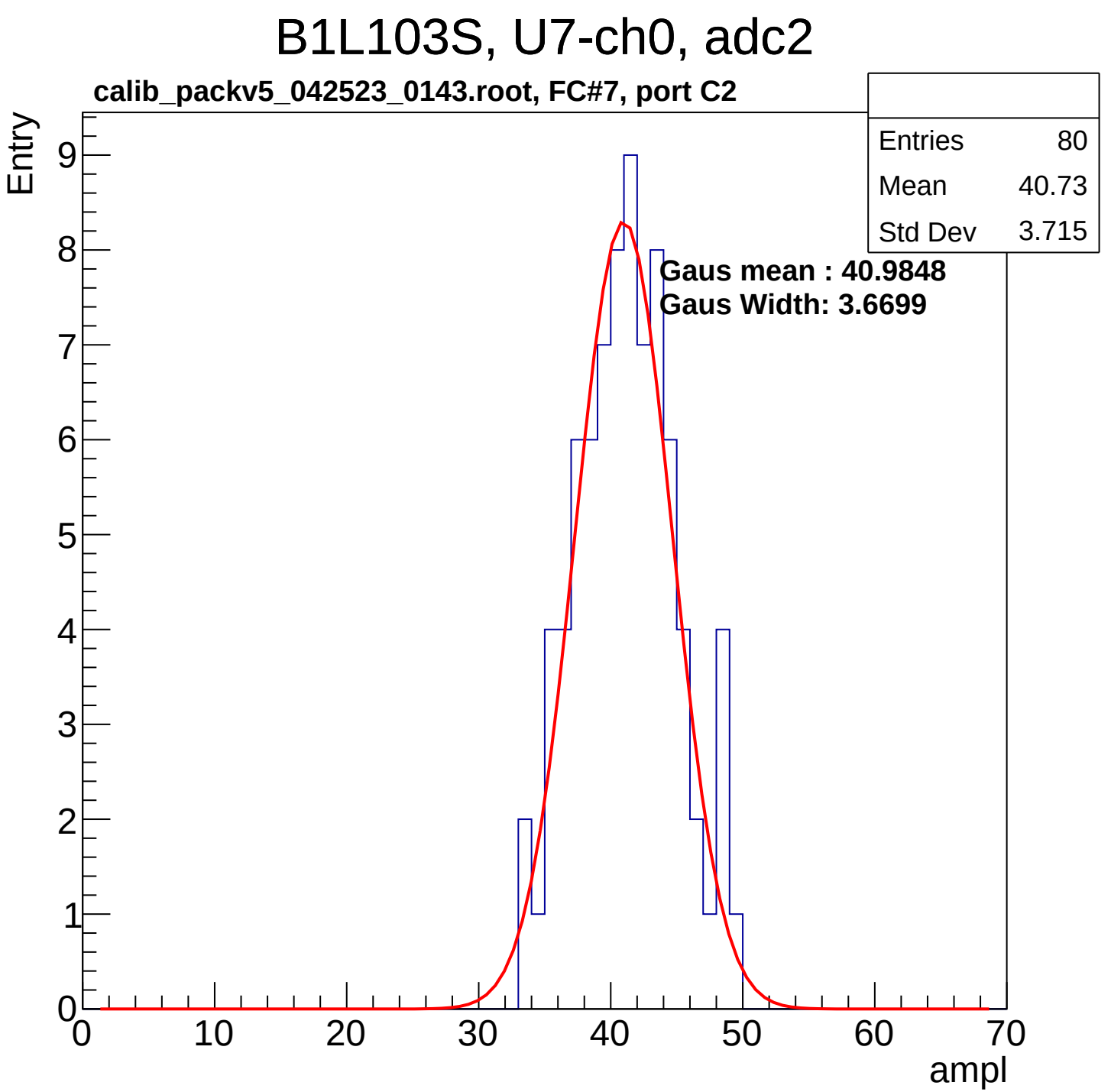
B1L103S, U7-ch0, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 80
Mean 40.73
Std Dev 3.715
Gaus mean : 40.9848
Gaus Width: 3.6699
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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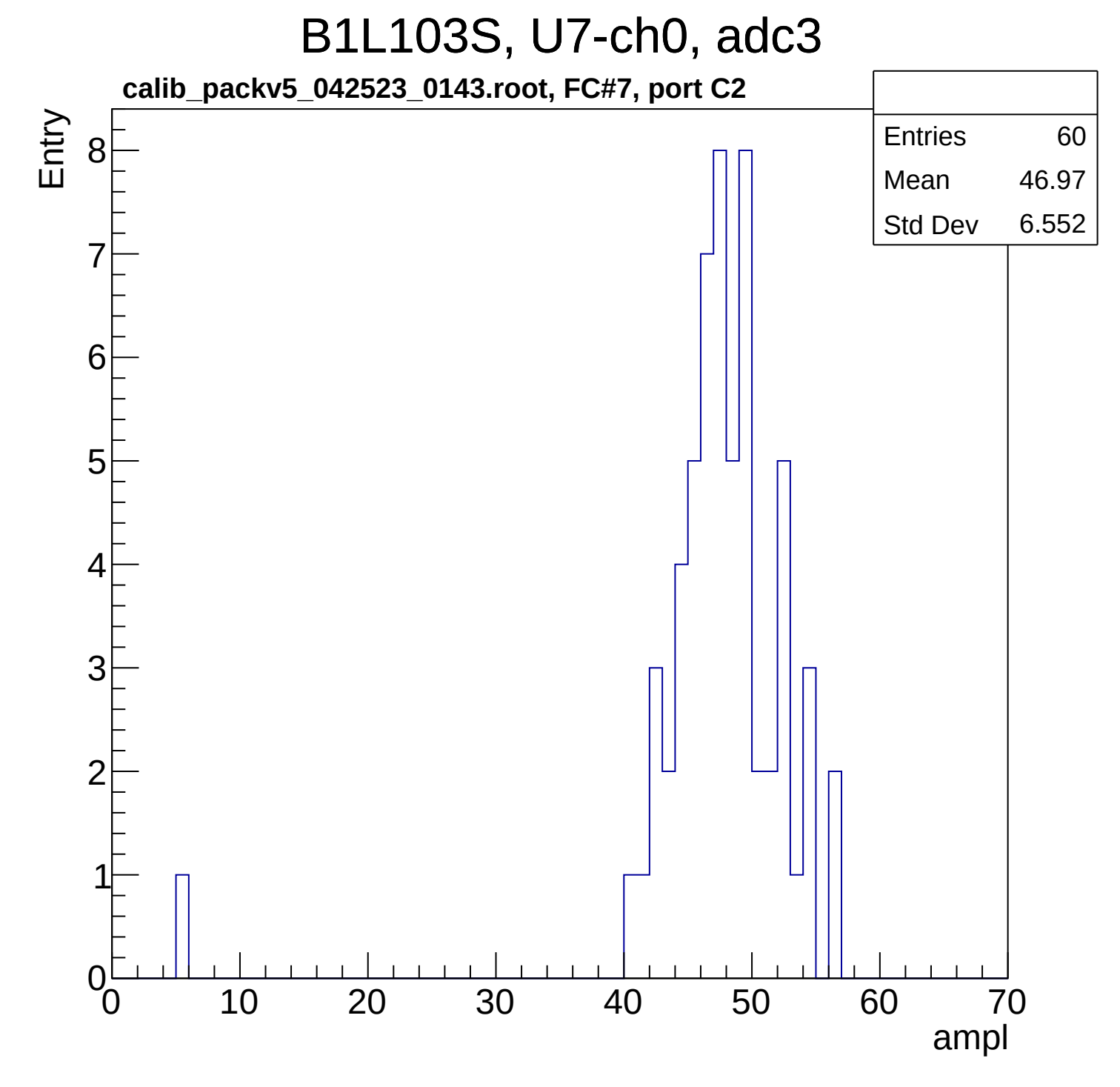
B1L103S, U7-ch0, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 60
Mean 46.97
Std Dev 6.552
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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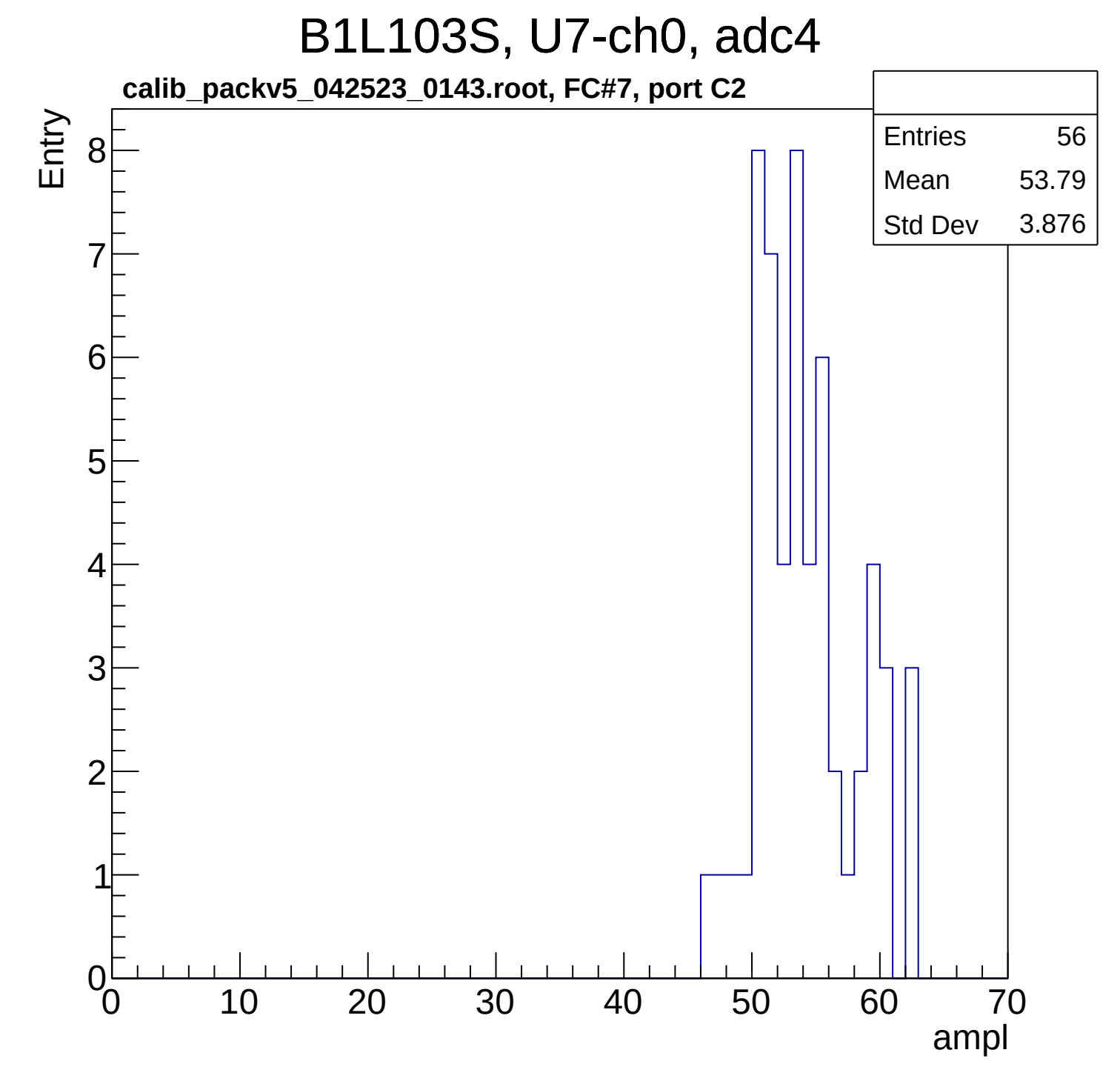
B1L103S, U7-ch0, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 53.79
Std Dev 3.876
Entry
ampl
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1
2
3
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5
6
7
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0
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40
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60
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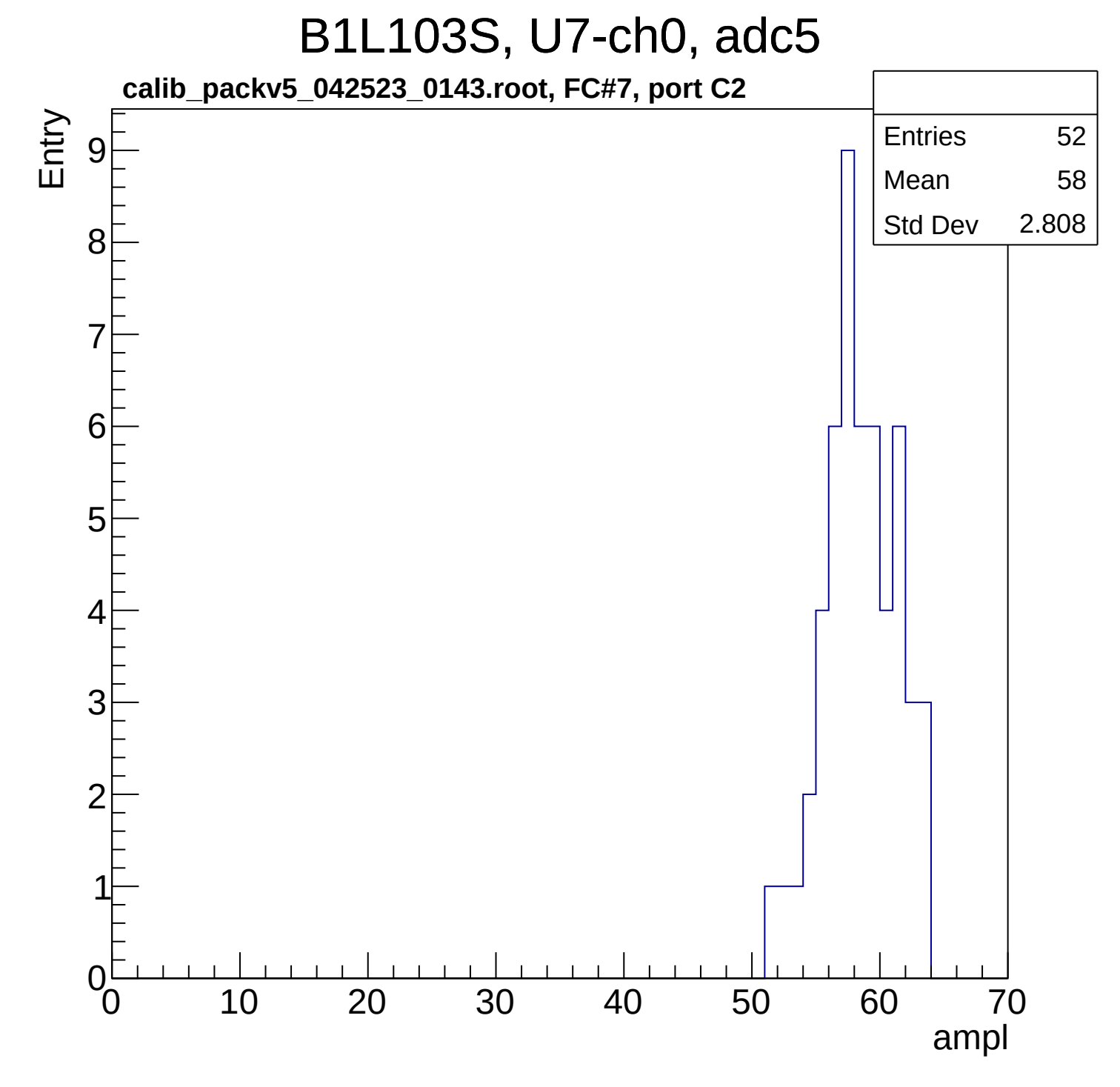
B1L103S, U7-ch0, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 52
Mean 58
Std Dev 2.808
Entry
ampl
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0
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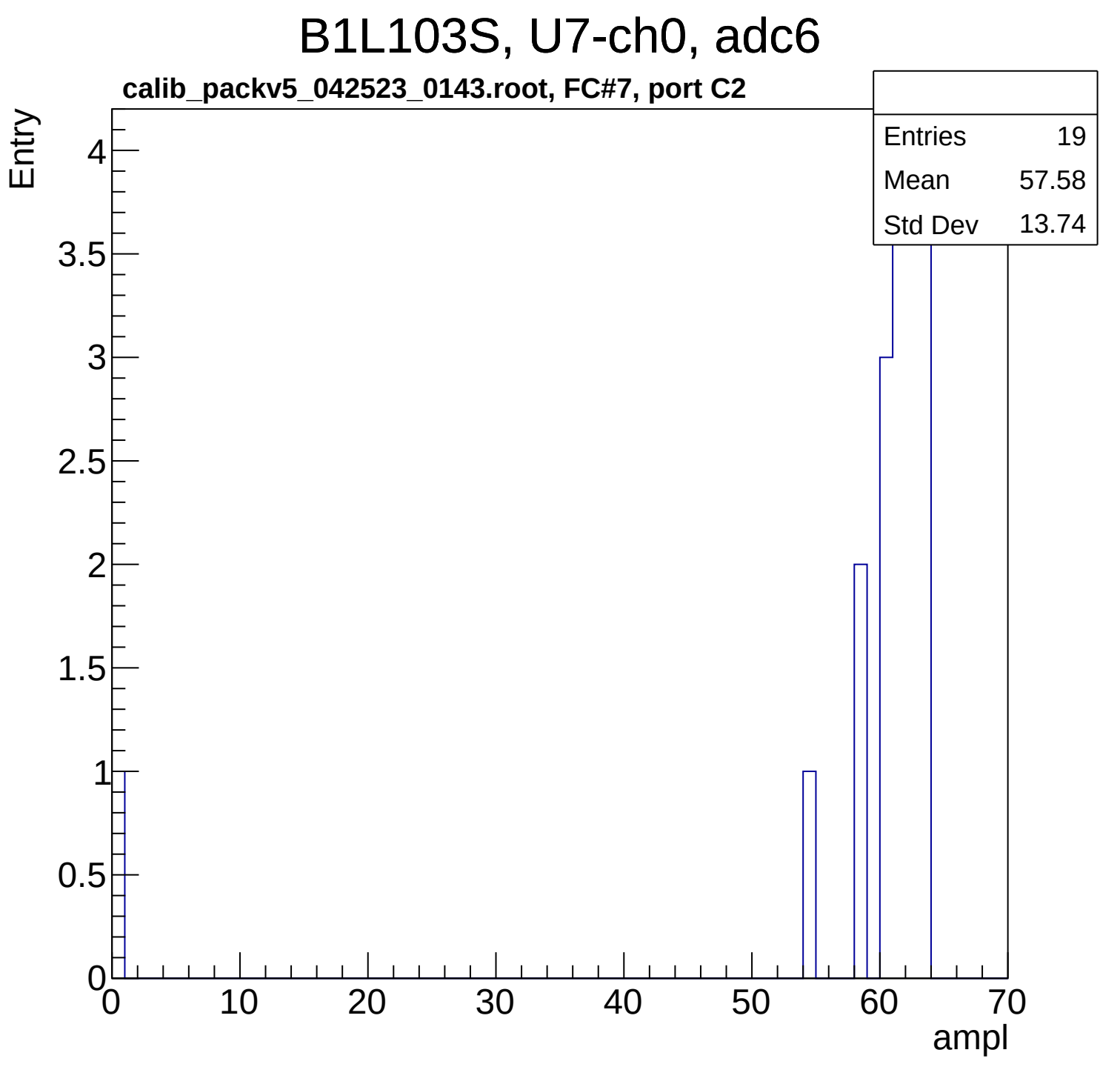
B1L103S, U7-ch0, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 19
Mean 57.58
Std Dev 13.74
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
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60
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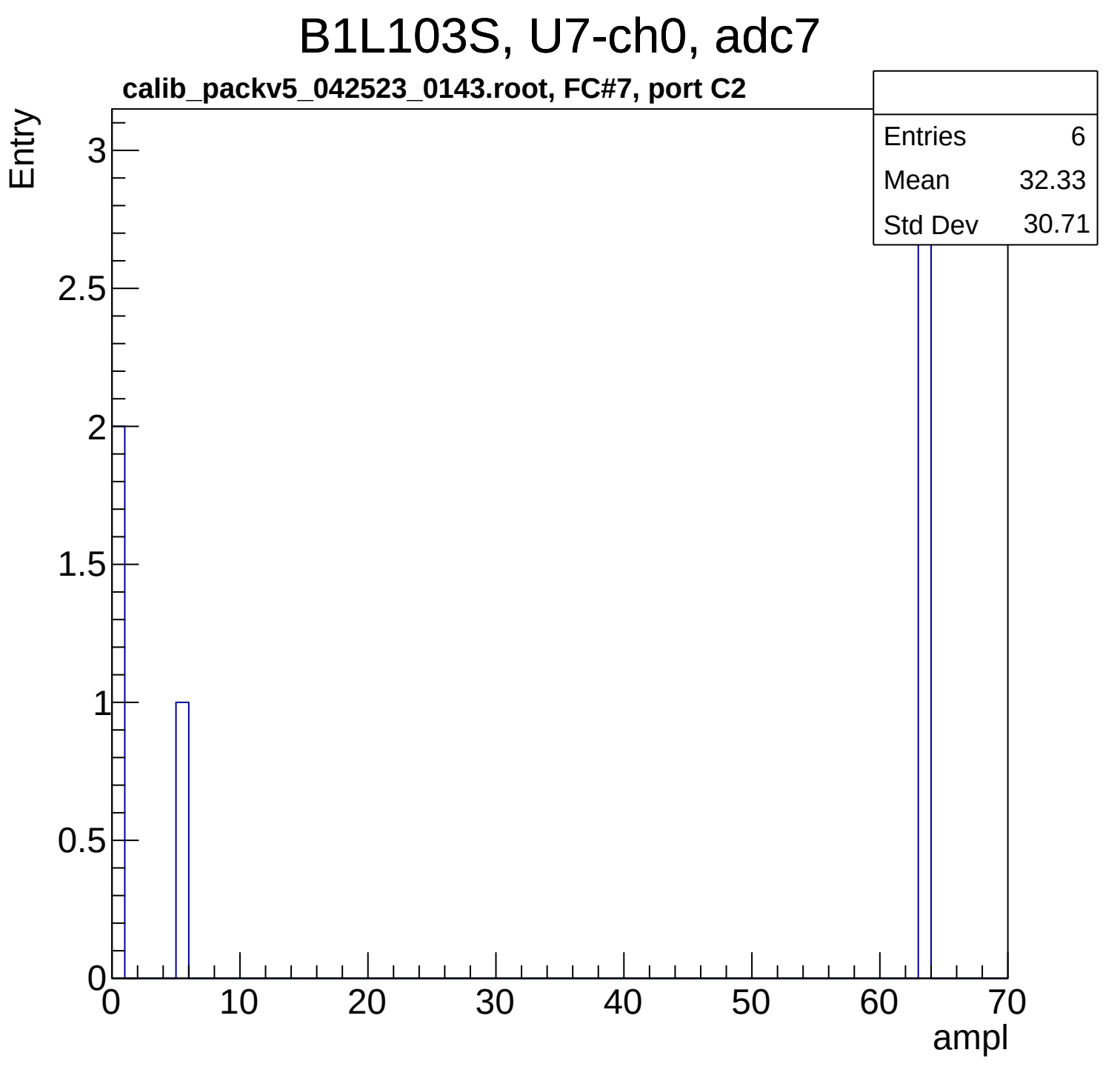
B1L103S, U7-ch0, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 6
Mean 32.33
Std Dev 30.71
Entry
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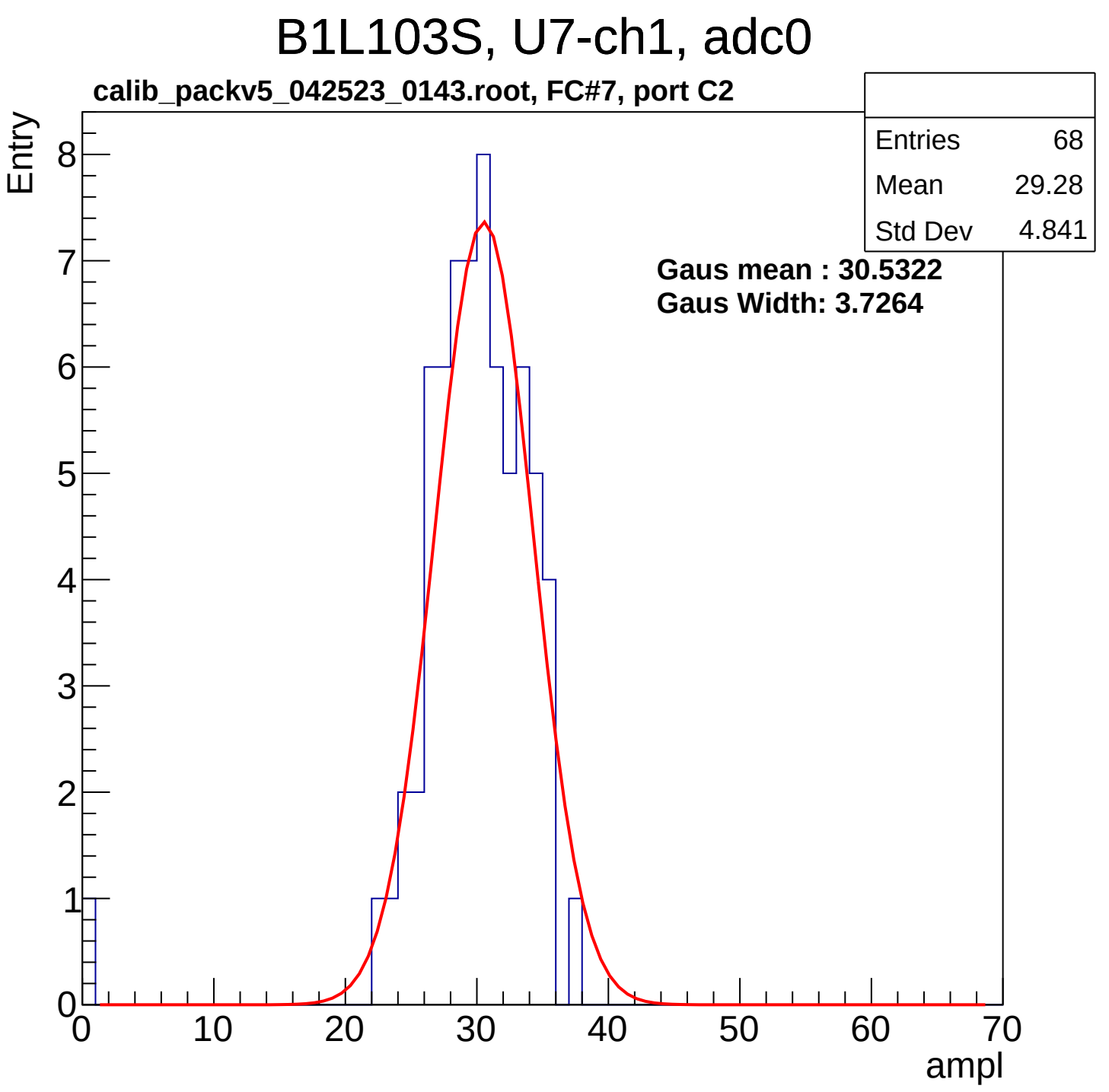
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch1, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 29.28
Std Dev 4.841
Gaus mean : 30.5322
Gaus Width: 3.7264
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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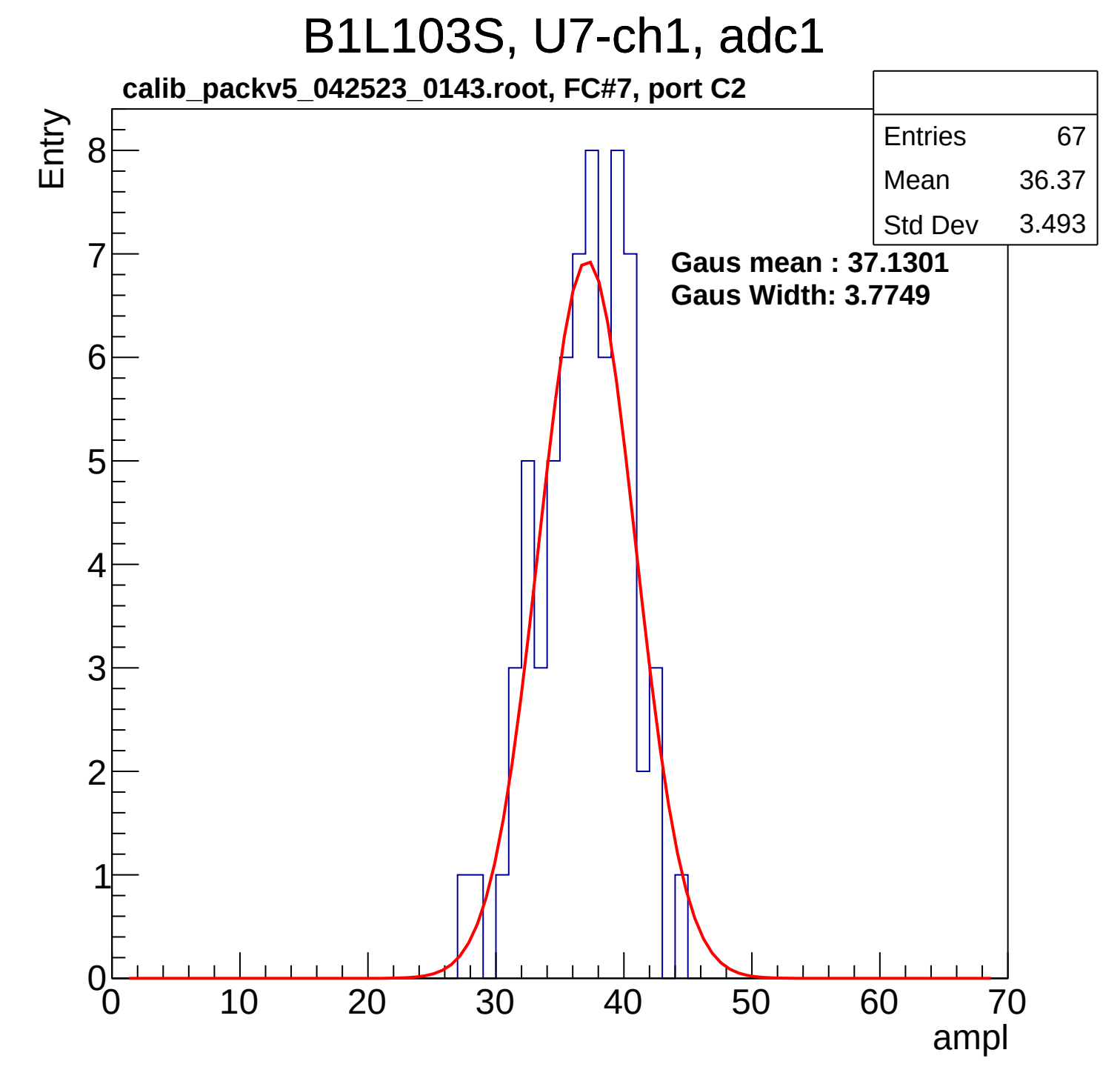
B1L103S, U7-ch1, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 36.37
Std Dev 3.493
Gaus mean : 37.1301
Gaus Width: 3.7749
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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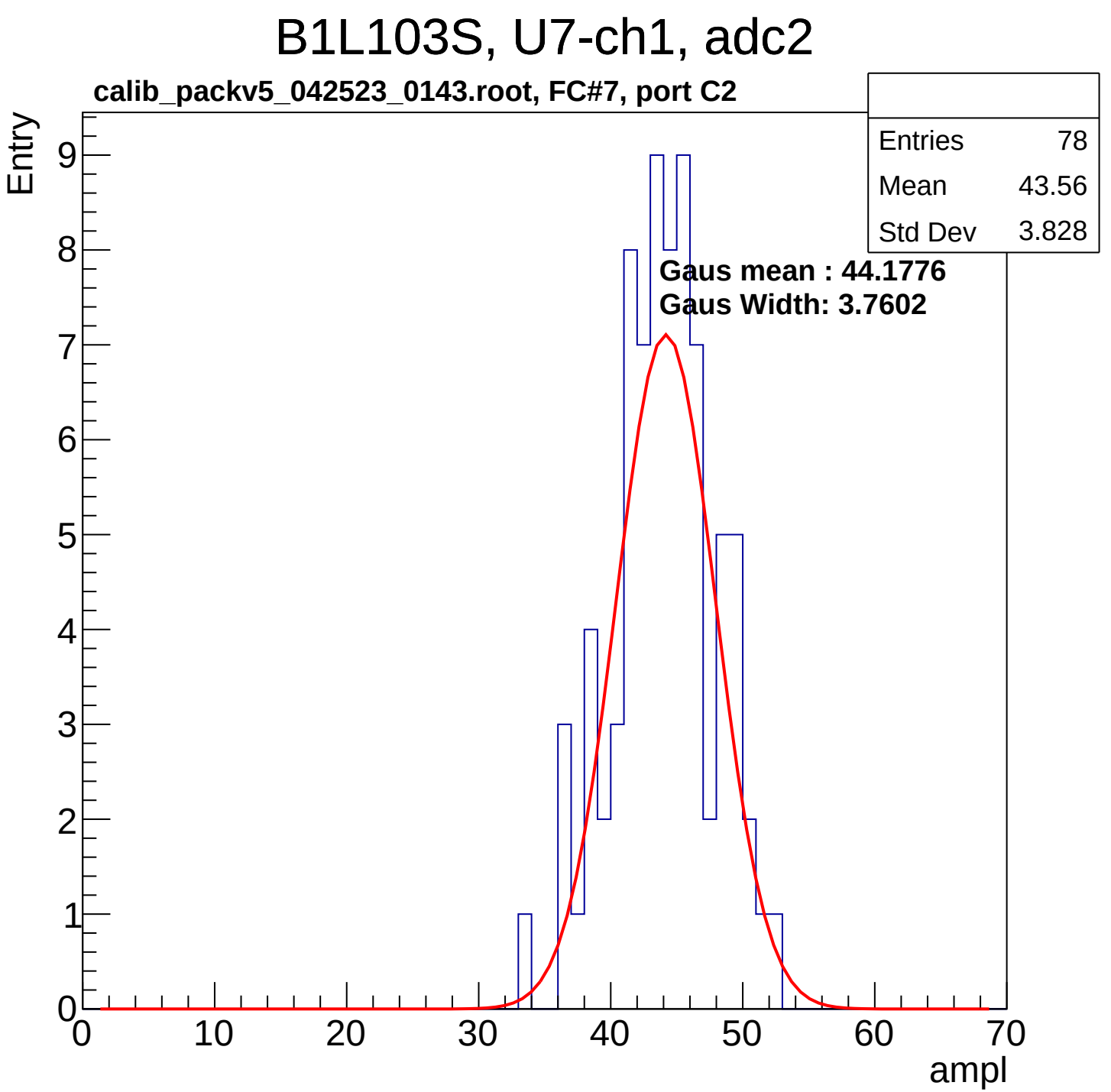
B1L103S, U7-ch1, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 78
Mean 43.56
Std Dev 3.828
Gaus mean : 44.1776
Gaus Width: 3.7602
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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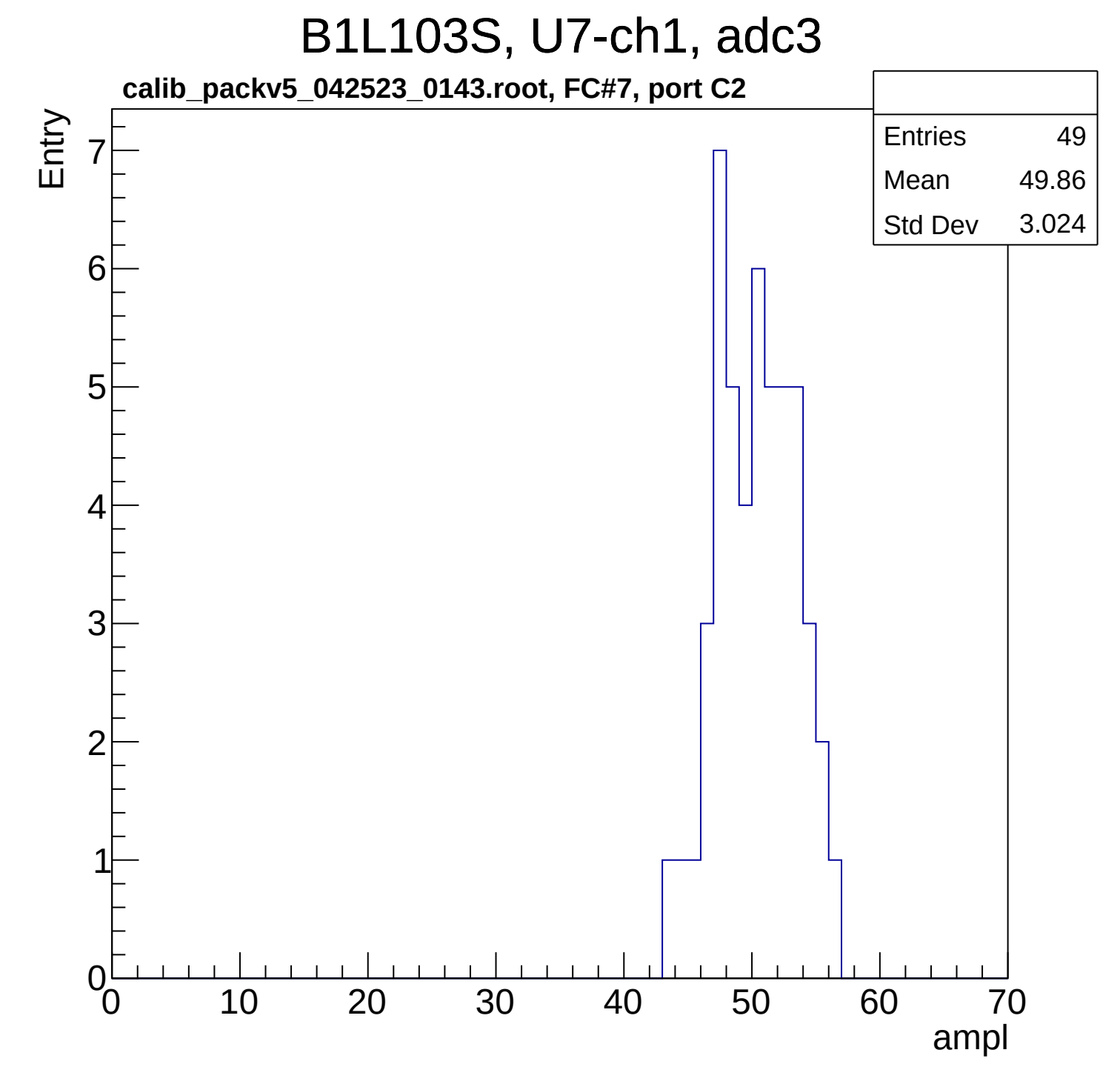
B1L103S, U7-ch1, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 49
Mean 49.86
Std Dev 3.024
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
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60
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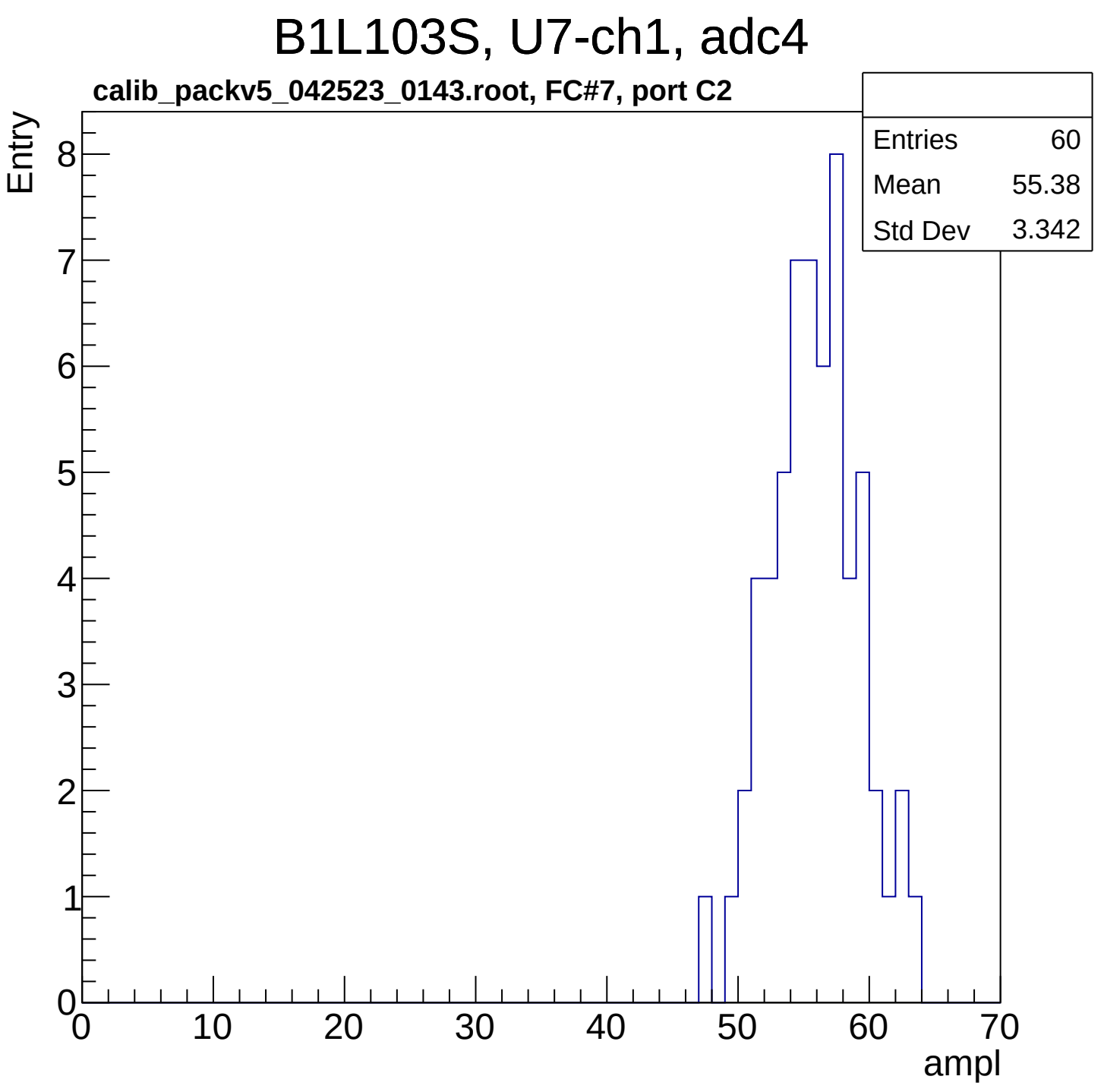
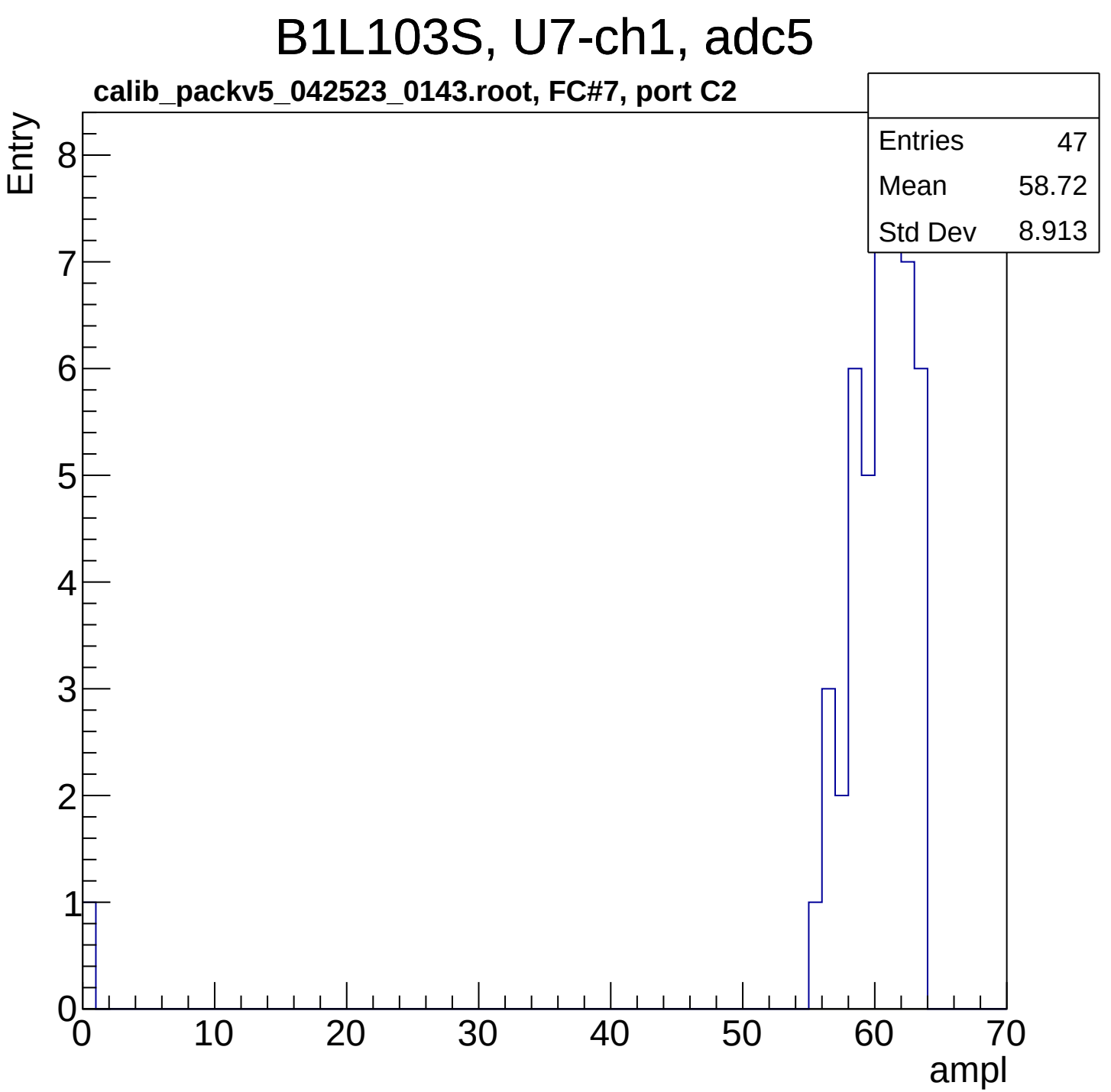

B1L103S, U7-ch1, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 60
Mean 55.38
Std Dev 3.342
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch1, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 47
Mean 58.72
Std Dev 8.913
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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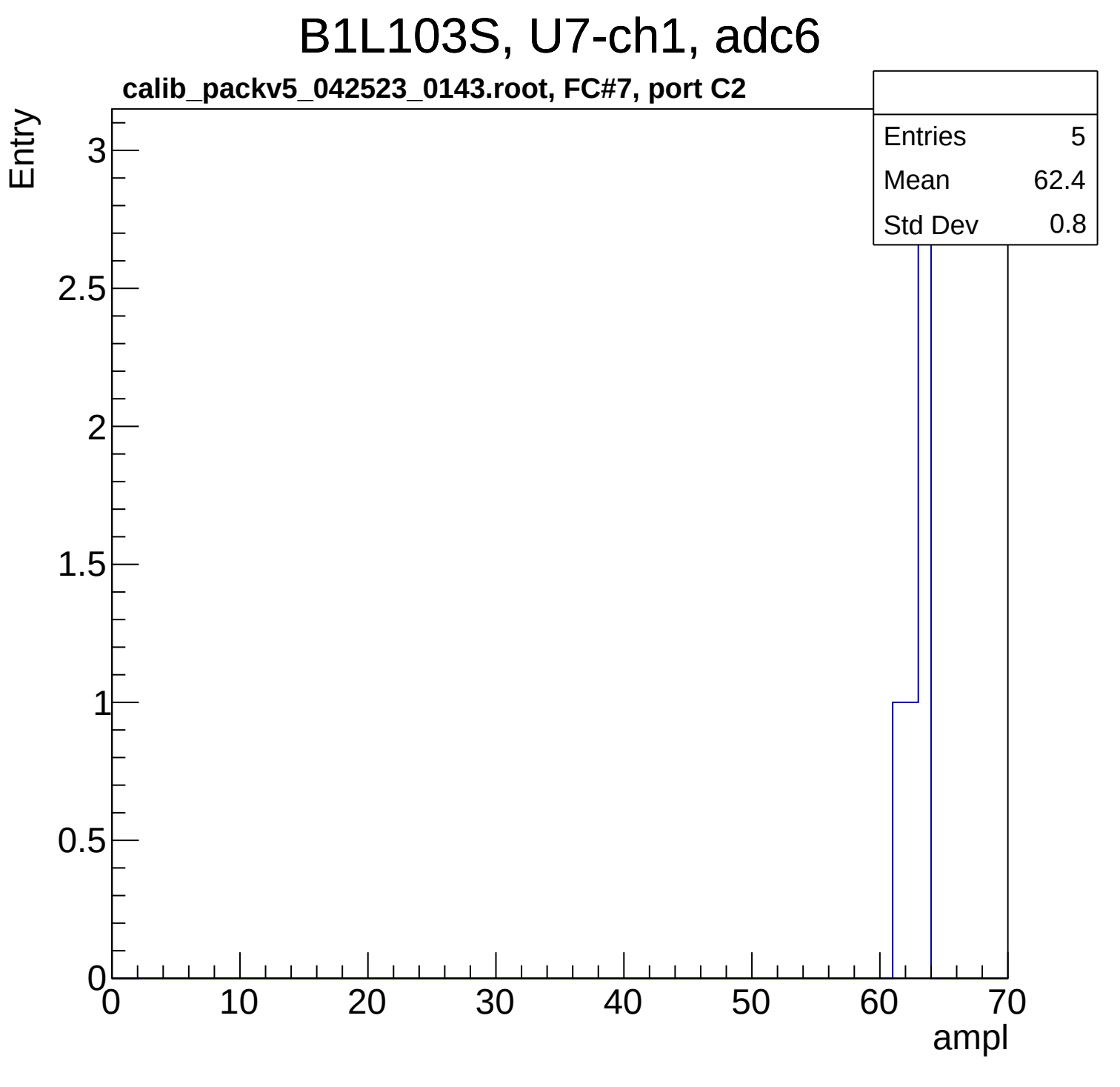
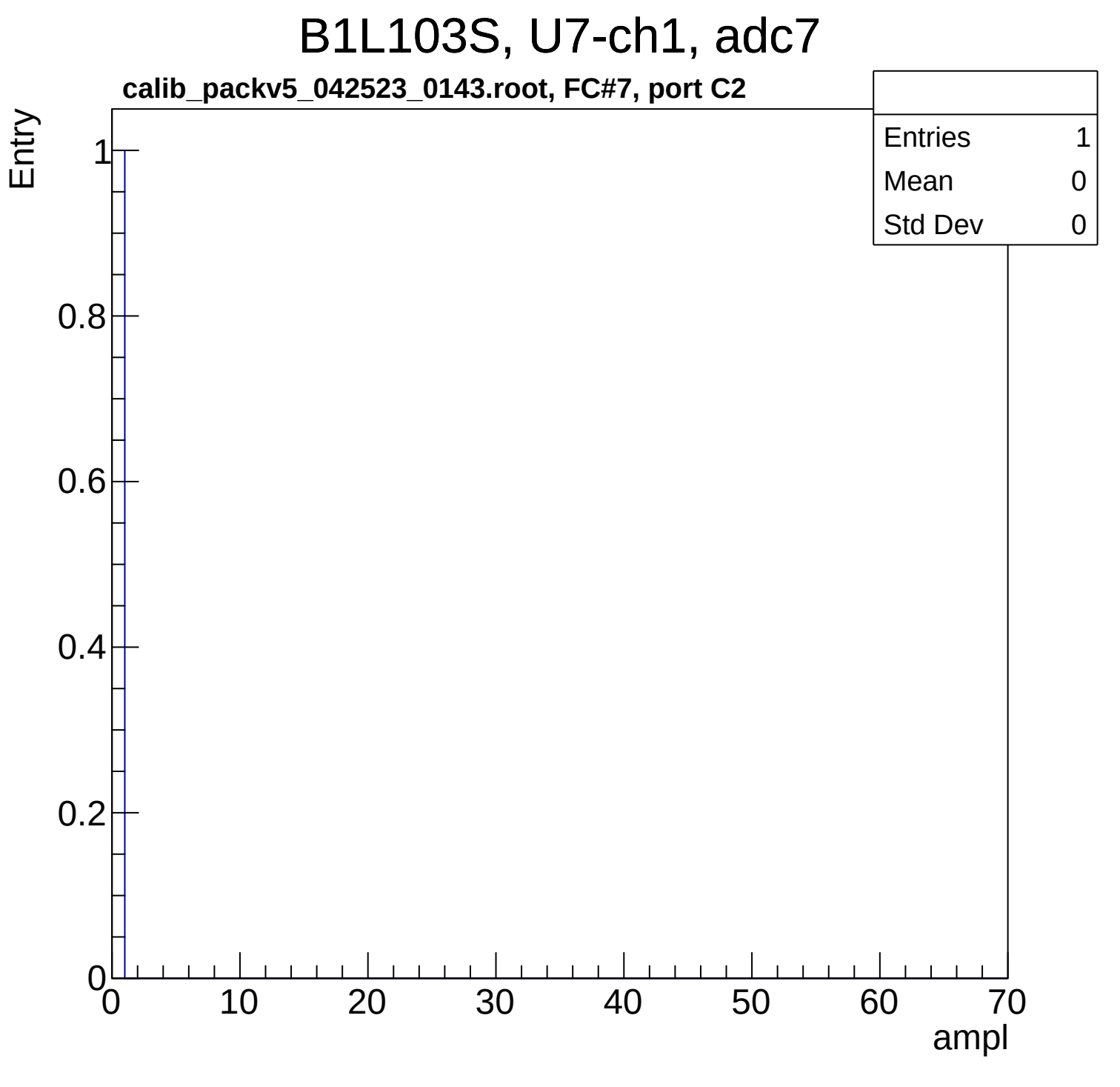
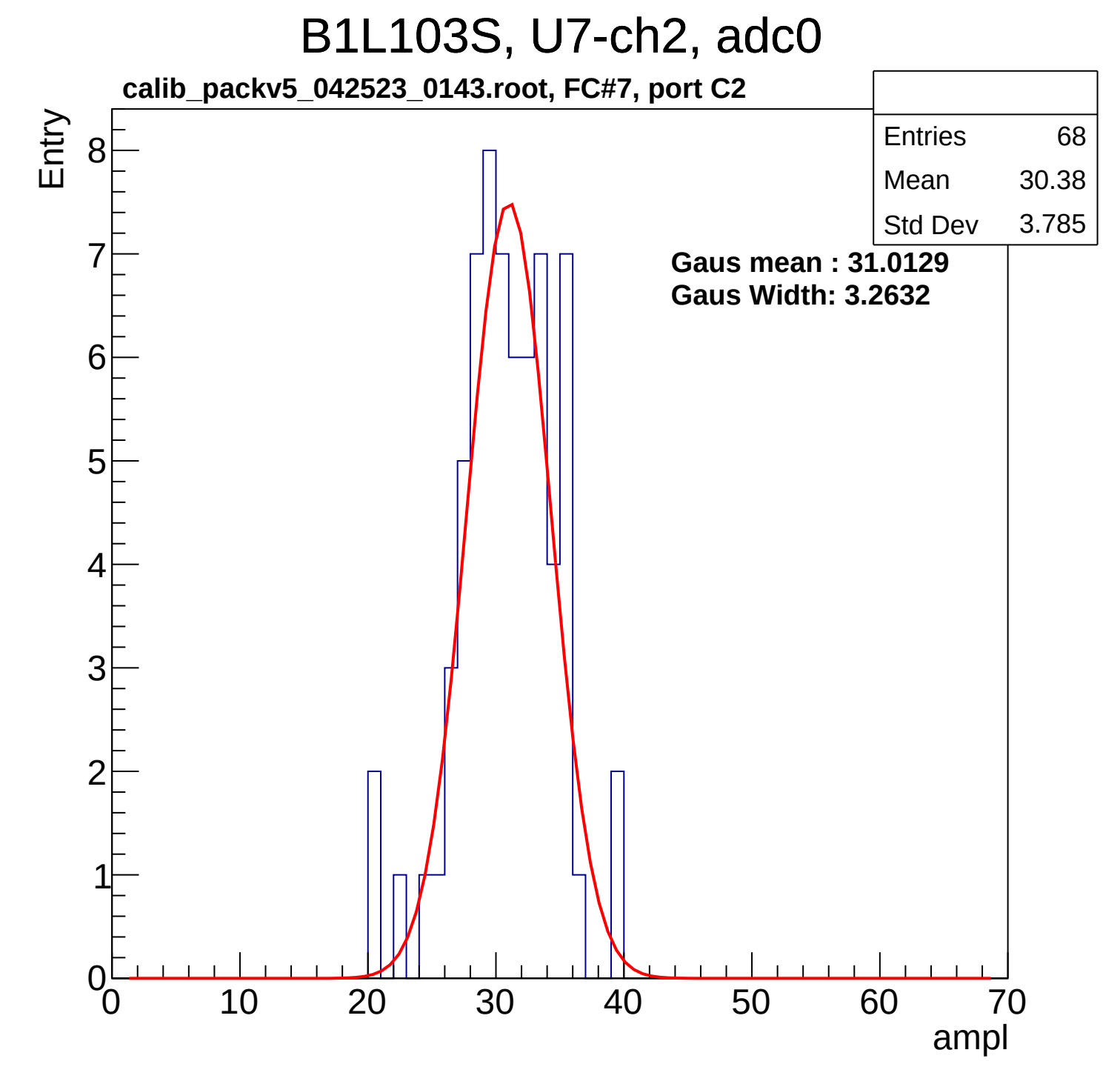

B1L103S, U7-ch1, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 5
Mean 62.4
Std Dev 0.8
Entry
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch1, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch2, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 30.38
Std Dev 3.785
Gaus mean : 31.0129
Gaus Width: 3.2632
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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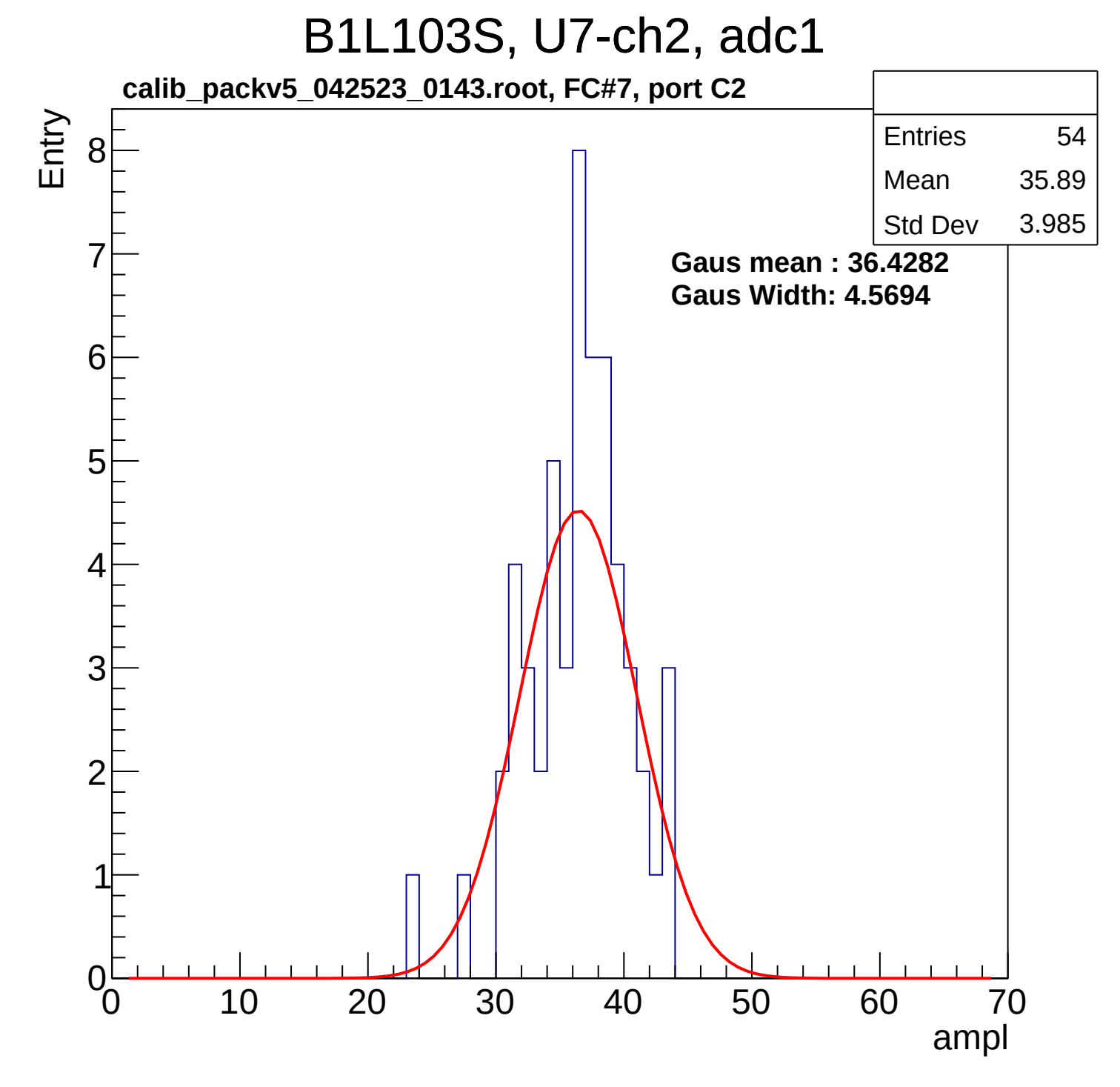
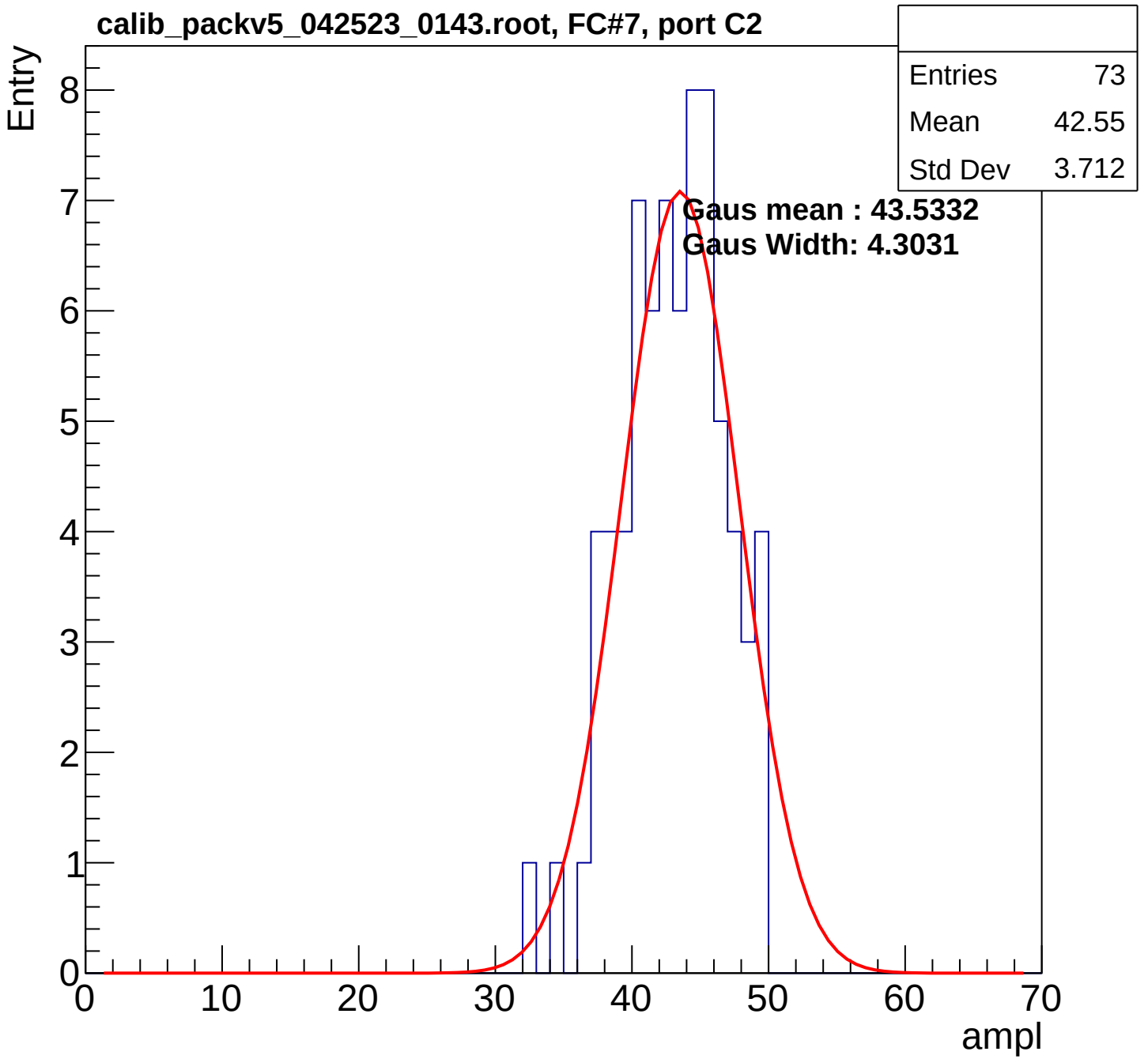
40
50
60
70


B1L103S, U7-ch2, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 54
Mean 35.89
Std Dev 3.985
Gaus mean : 36.4282
Gaus Width: 4.5694
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch2, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 73
Mean 42.55
Std Dev 3.712
Gaus mean : 43.5332
Gaus Width: 4.3031
Entry
ampl
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1
2
3
4
5
6
7
8
0
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40
50
60
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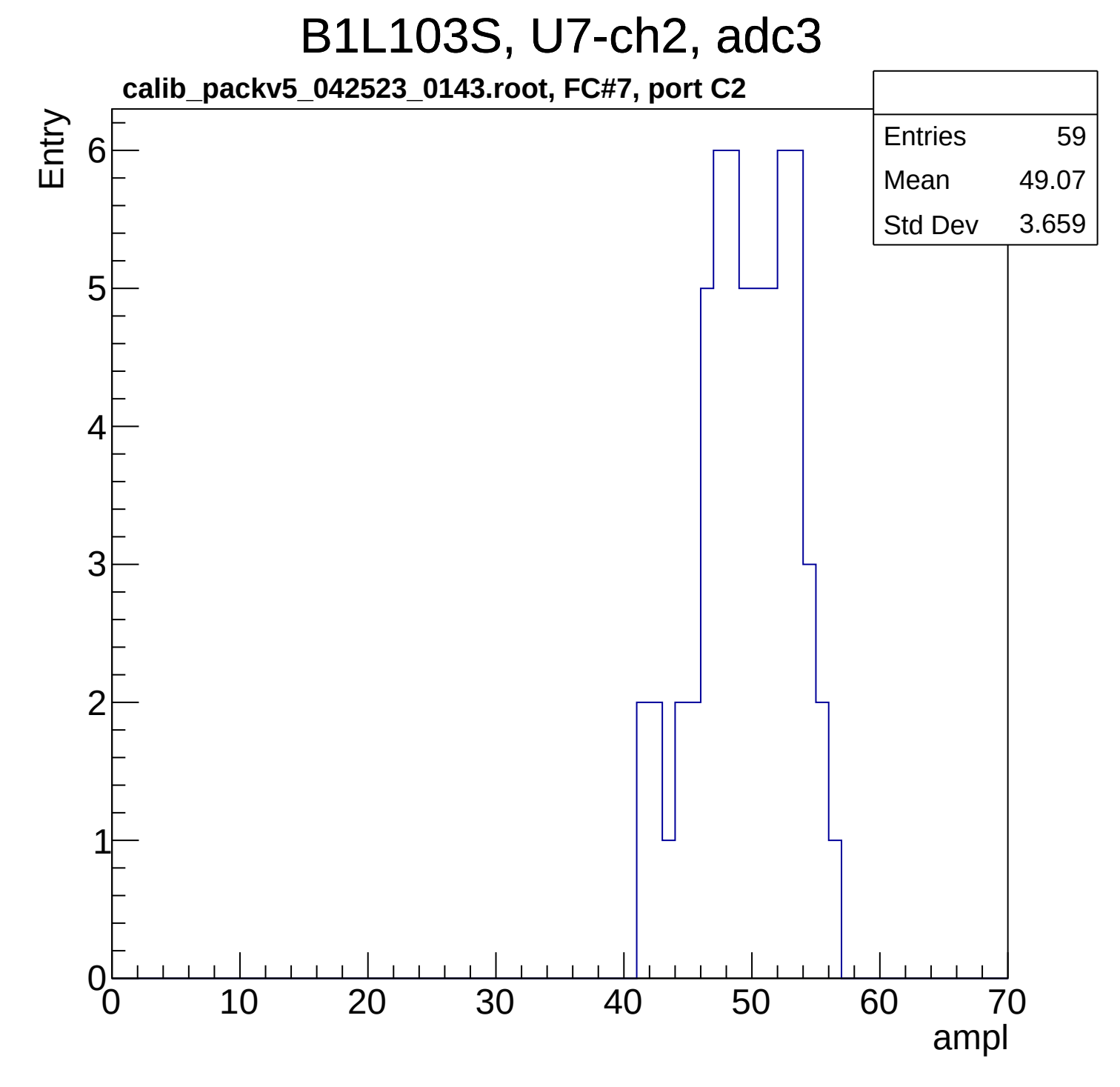
B1L103S, U7-ch2, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 49.07
Std Dev 3.659
Entry
ampl
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1
2
3
4
5
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0
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20
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40
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60
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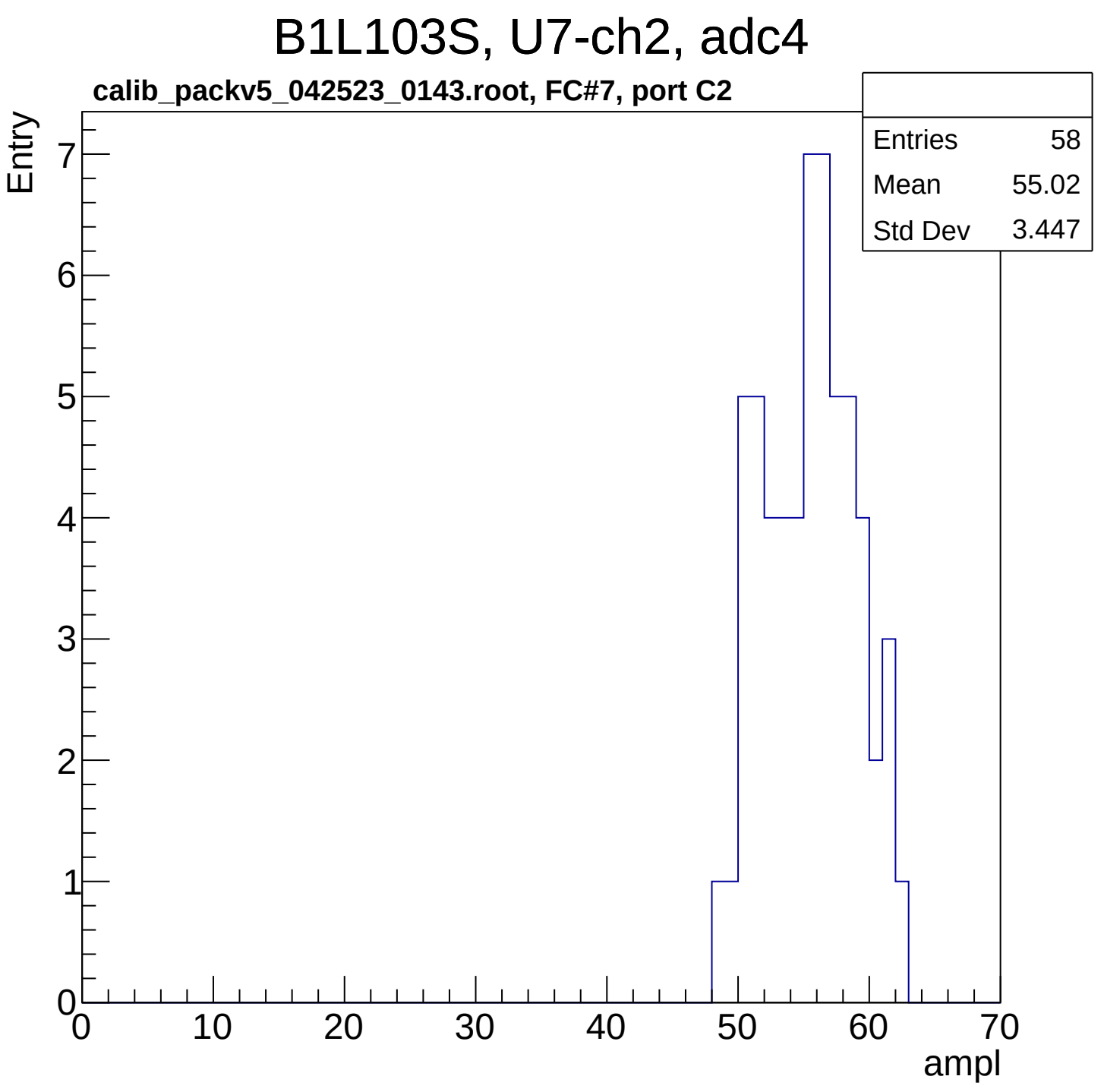
B1L103S, U7-ch2, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 58
Mean 55.02
Std Dev 3.447
Entry
ampl
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1
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3
4
5
6
7
0
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20
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40
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60
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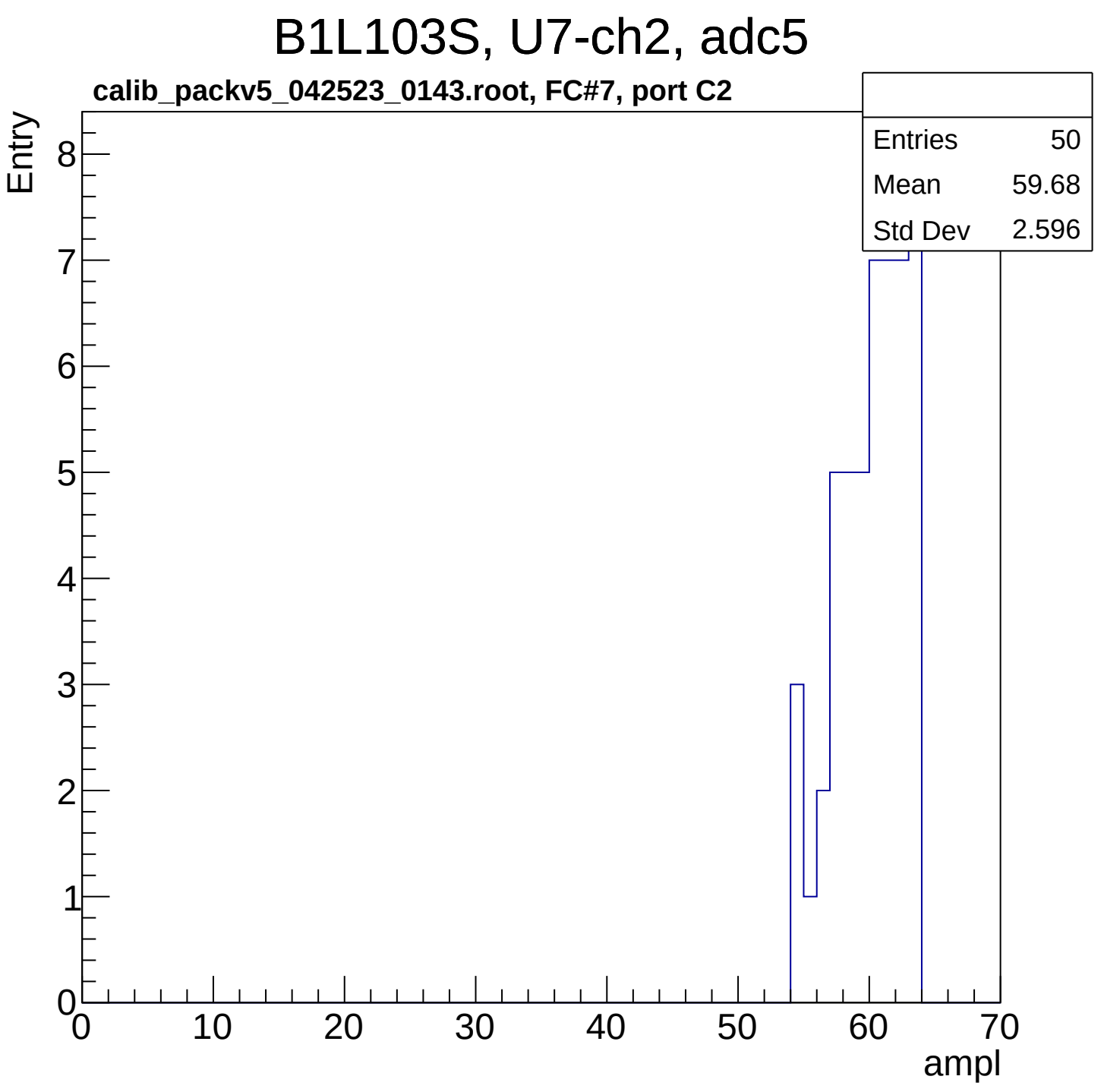
B1L103S, U7-ch2, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 50
Mean 59.68
Std Dev 2.596
Entry
ampl
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2
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4
5
6
7
8
0
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20
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40
50
60
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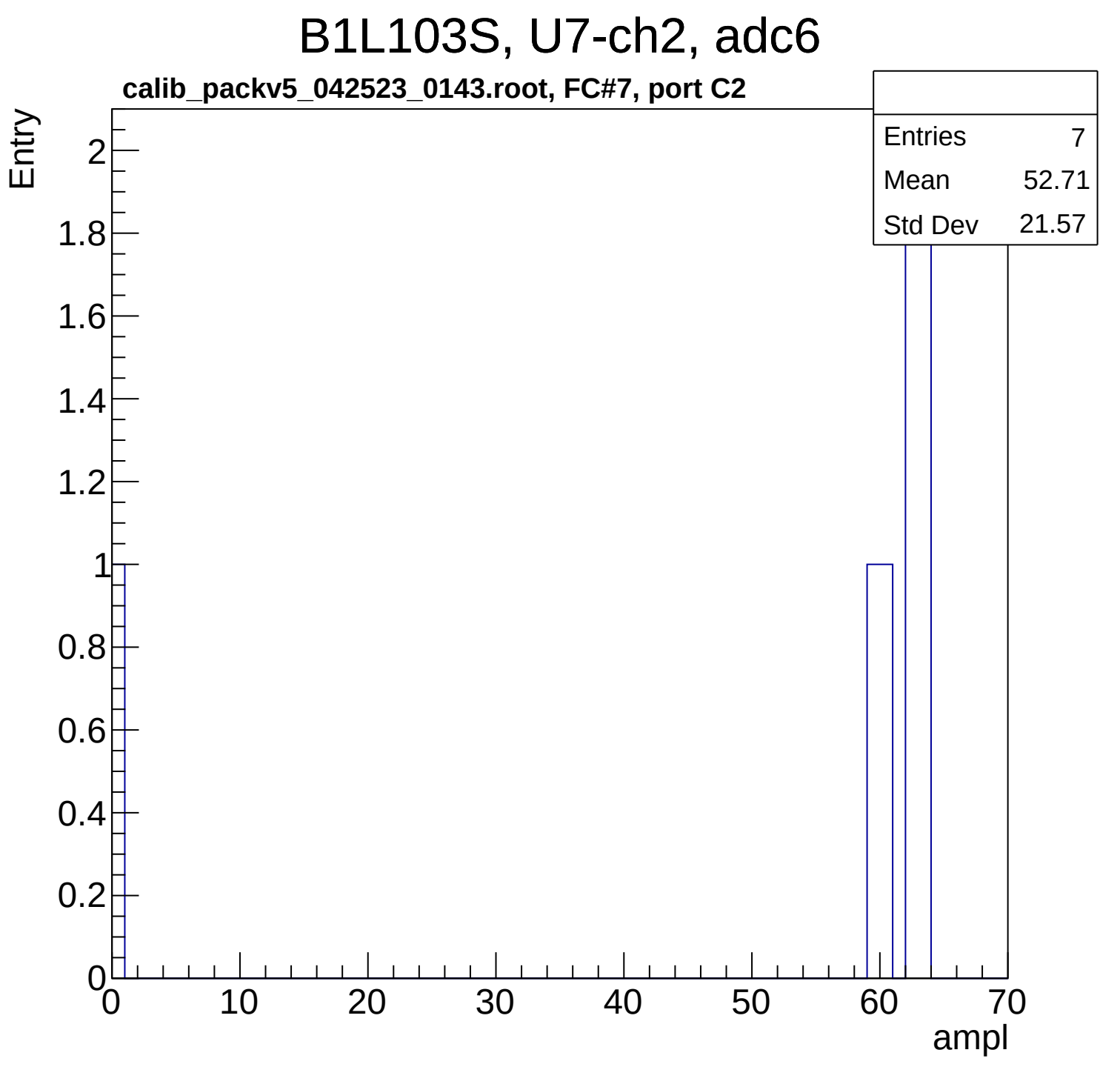
B1L103S, U7-ch2, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 7
Mean 52.71
Std Dev 21.57
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
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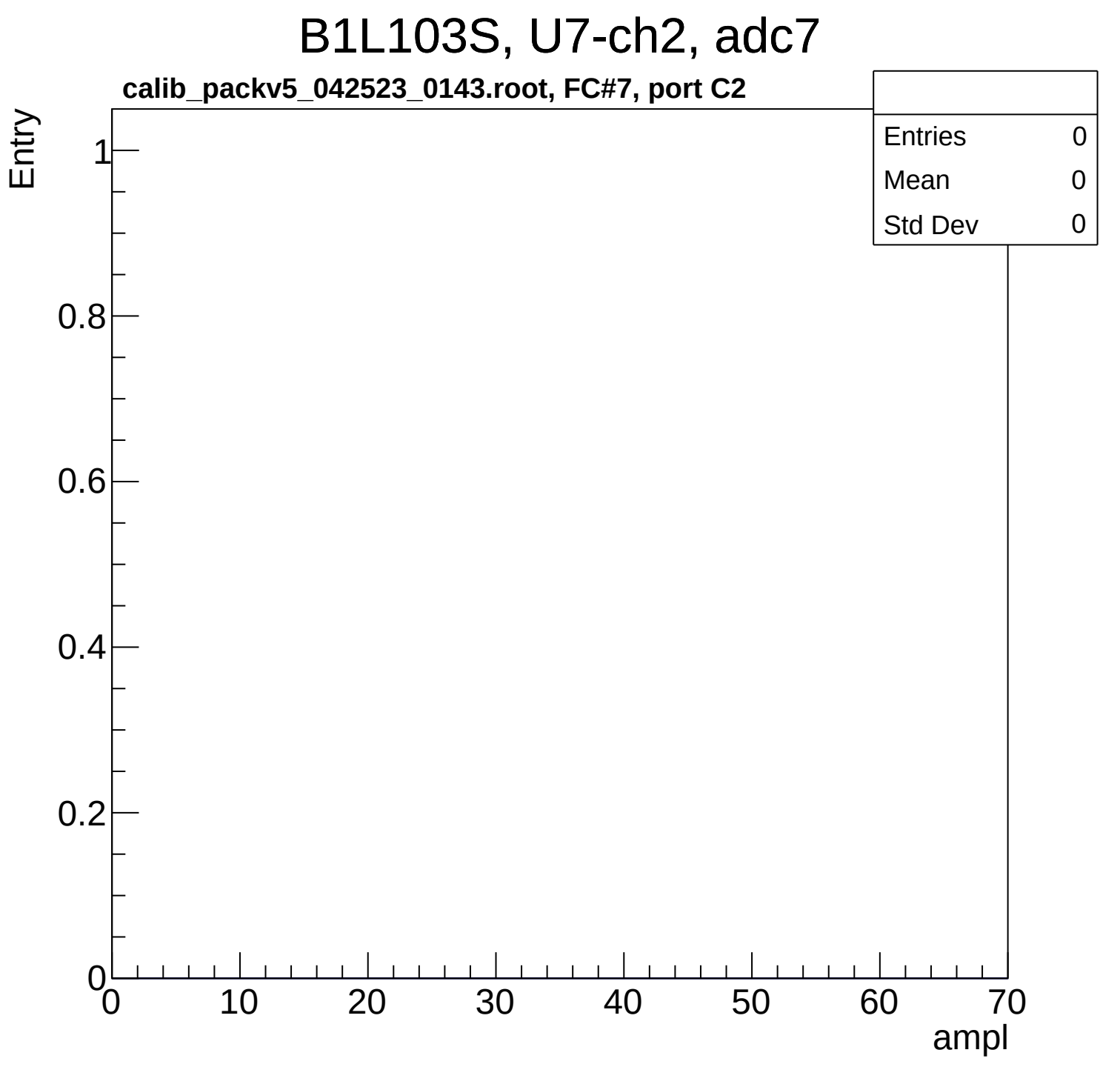
40
50
60
70


B1L103S, U7-ch2, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
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0.6
0.4
0.2
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10
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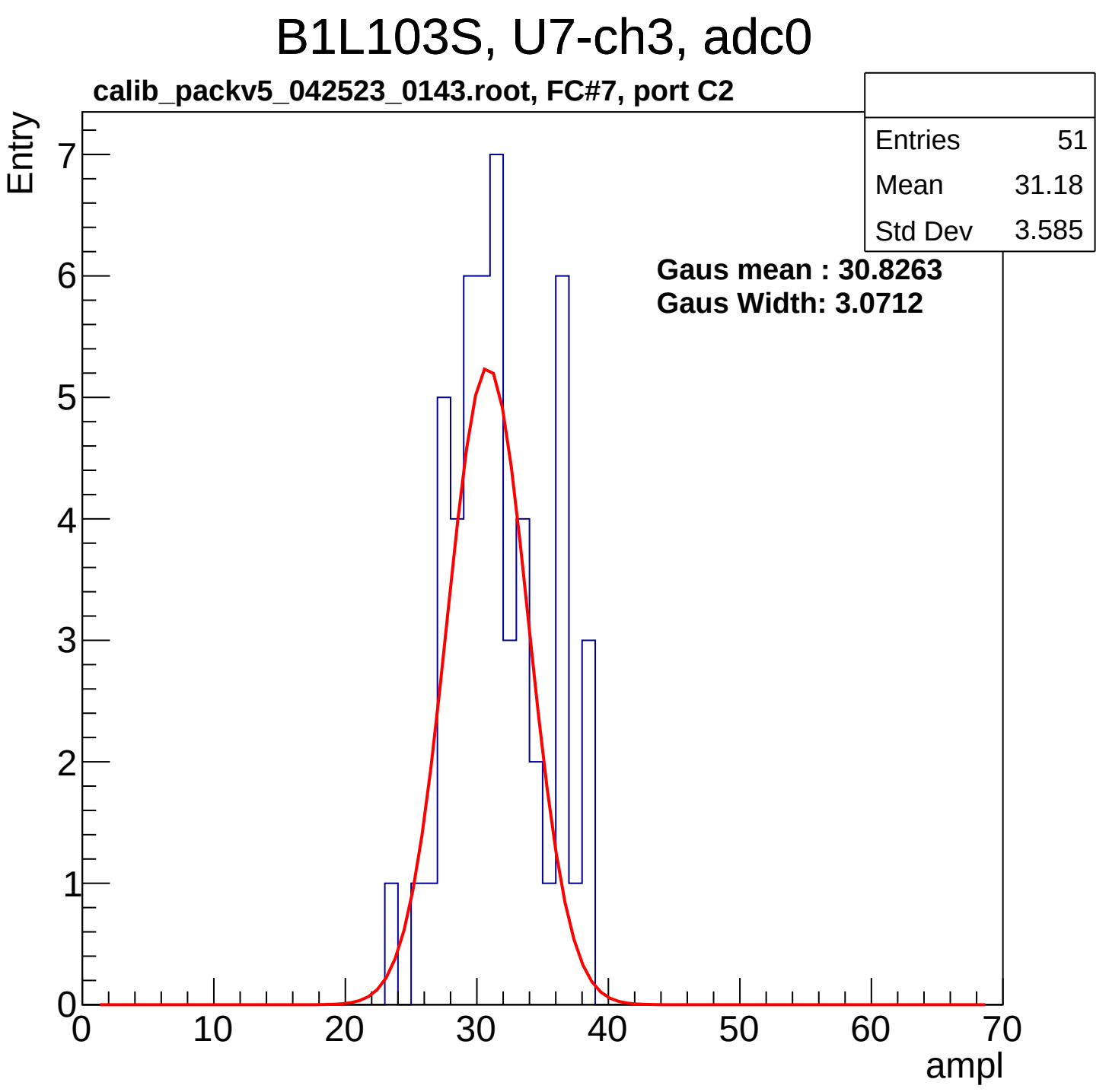
50
60
70
ampl


B1L103S, U7-ch3, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 51
Mean 31.18
Std Dev 3.585
Gaus mean : 30.8263
Gaus Width: 3.0712
Entry
ampl
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2
3
4
5
6
7
0
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20
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40
50
60
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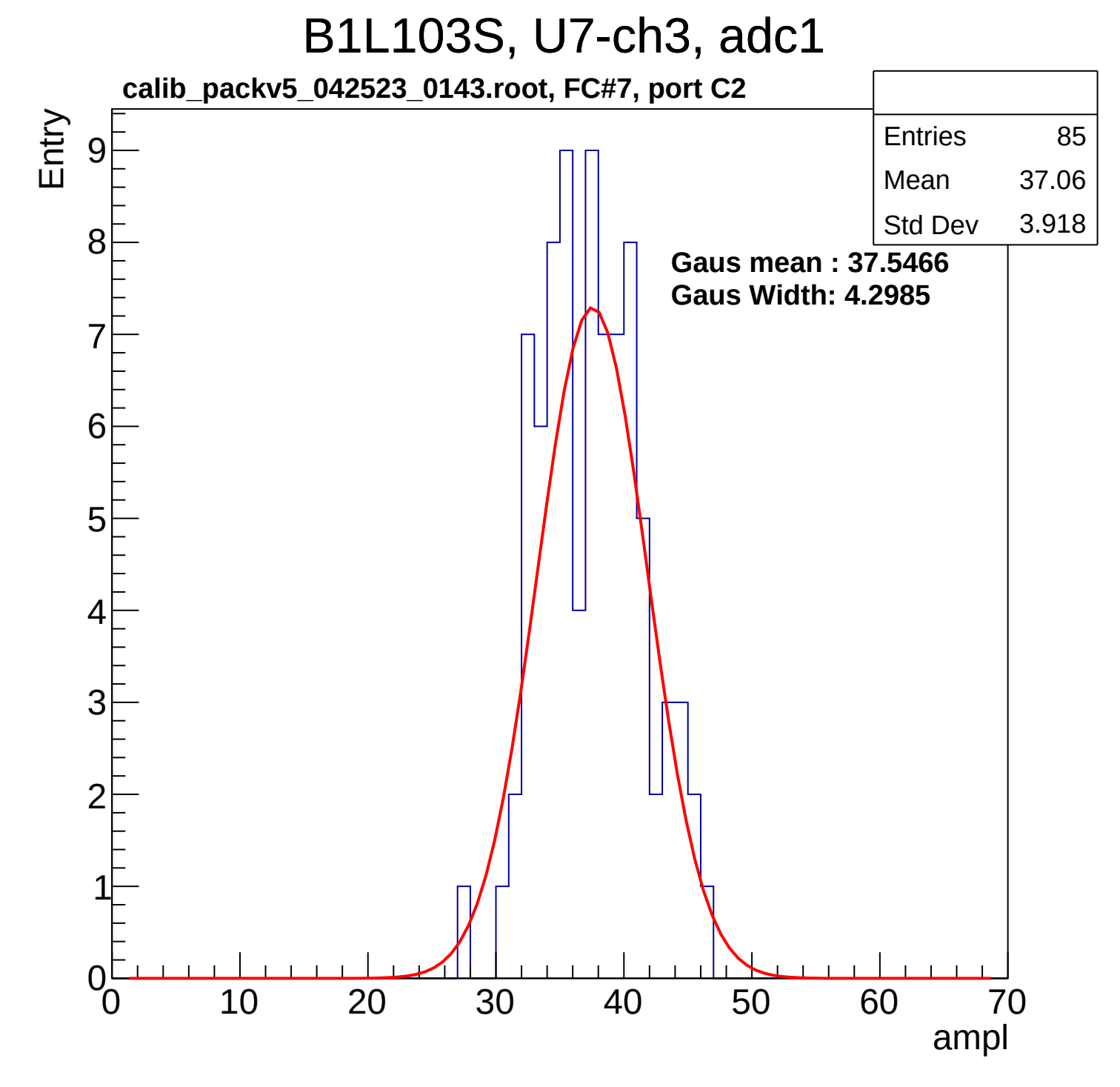
B1L103S, U7-ch3, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 85
Mean 37.06
Std Dev 3.918
Gaus mean : 37.5466
Gaus Width: 4.2985
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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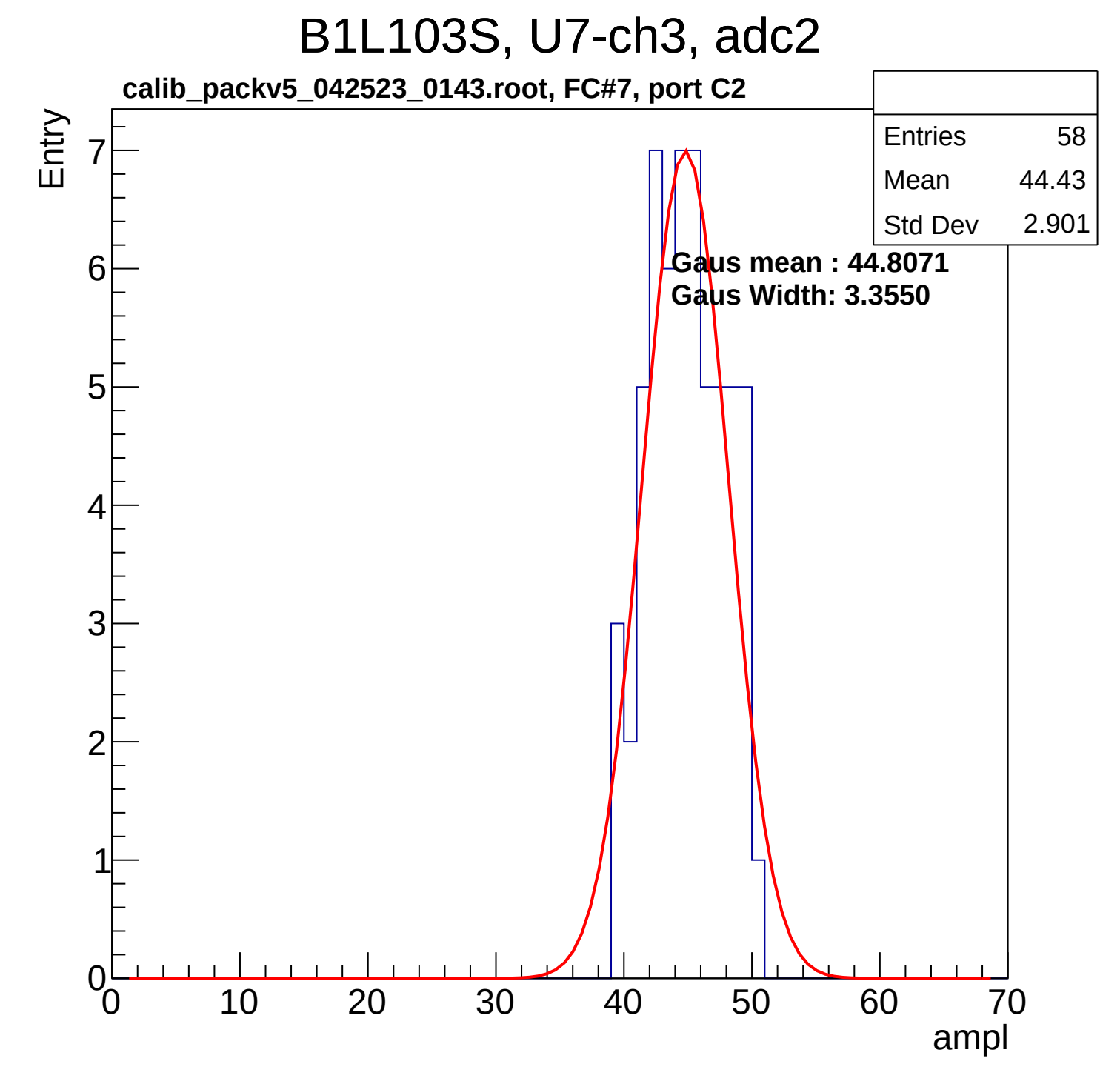
B1L103S, U7-ch3, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 58
Mean 44.43
Std Dev 2.901
Gaus mean : 44.8071
Gaus Width: 3.3550
Entry
ampl
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2
3
4
5
6
7
0
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40
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60
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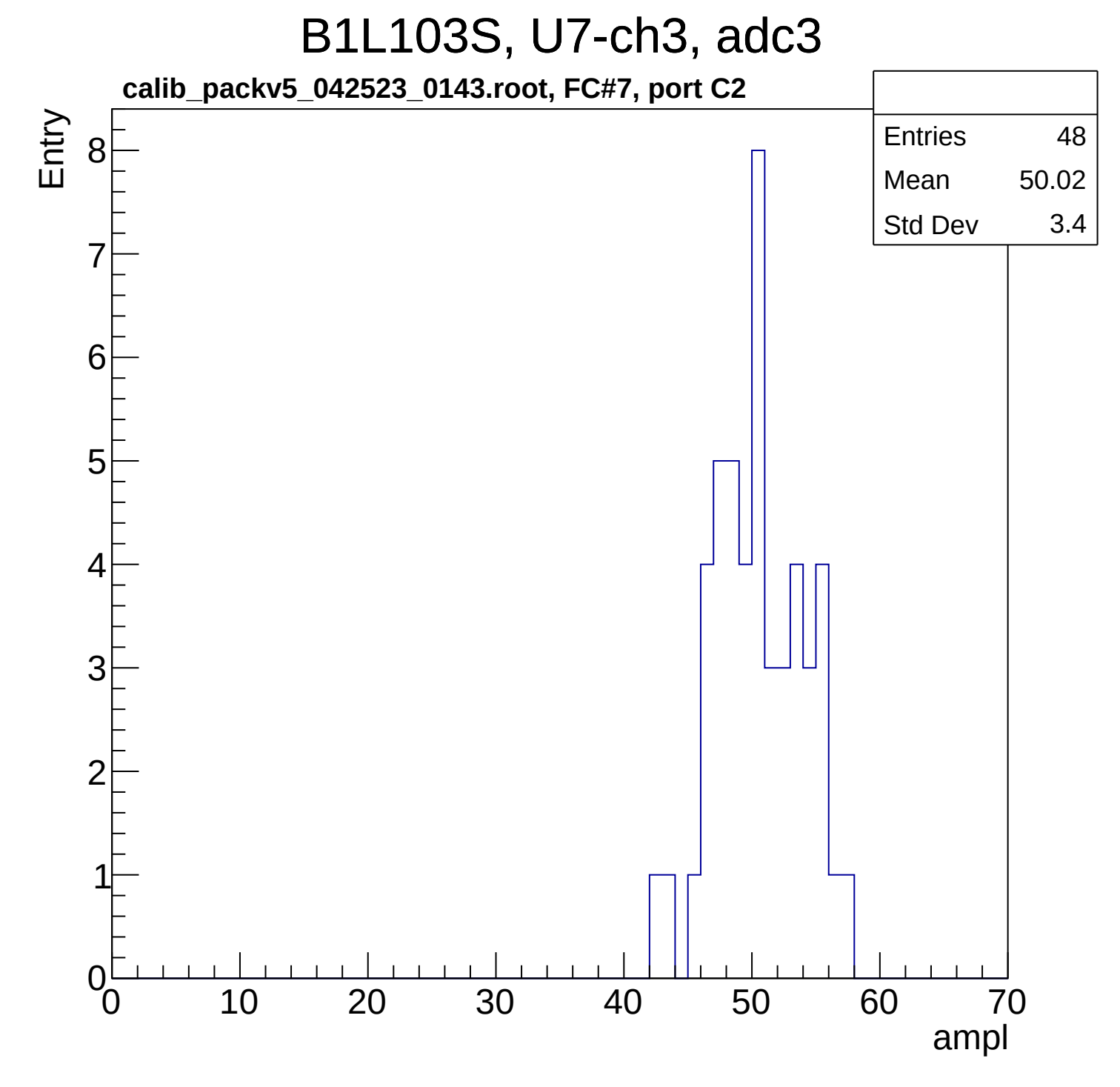
B1L103S, U7-ch3, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 48
Mean 50.02
Std Dev 3.4
Entry
ampl
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4
5
6
7
8
0
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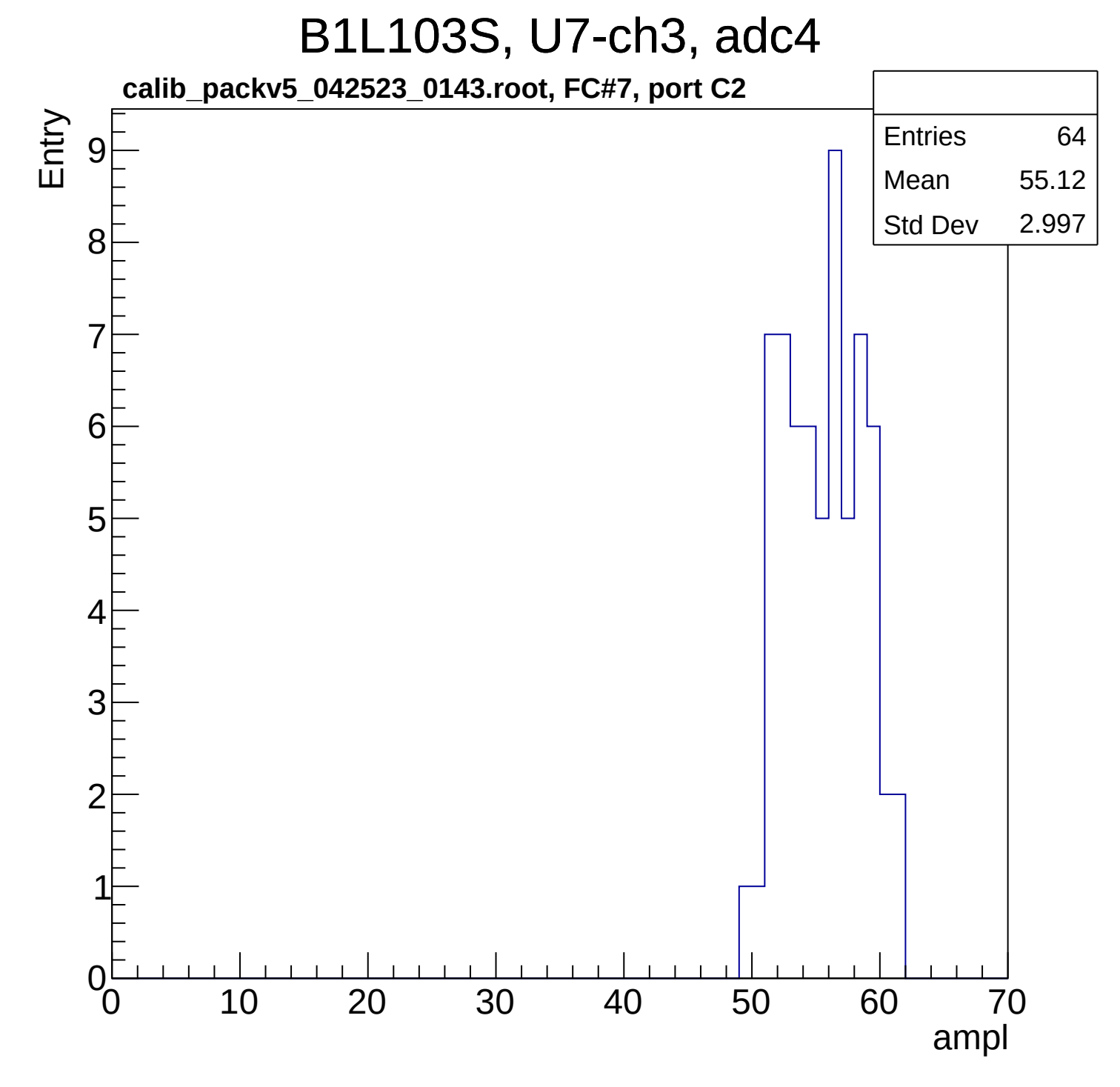
B1L103S, U7-ch3, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 55.12
Std Dev 2.997
Entry
ampl
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3
4
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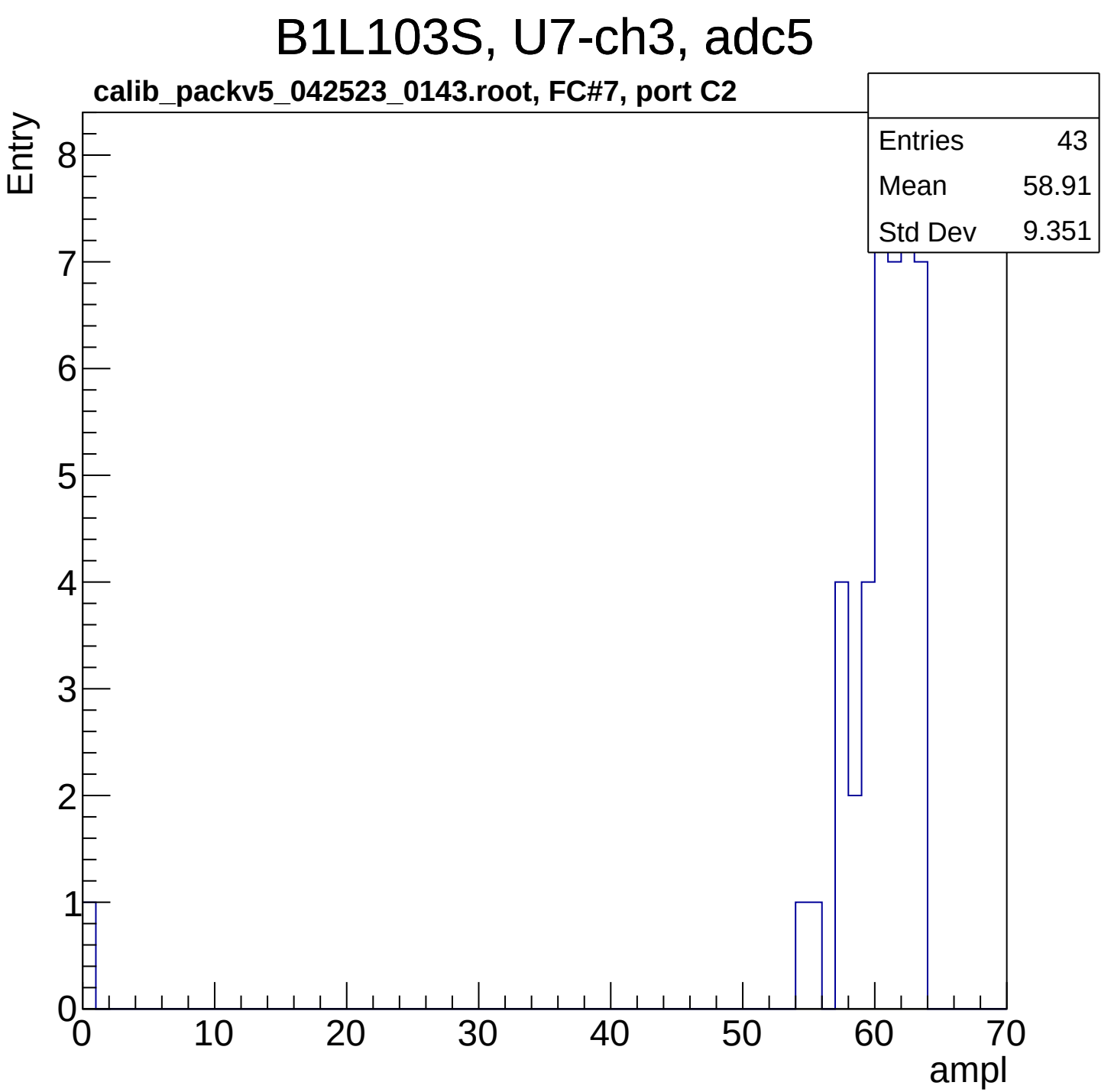
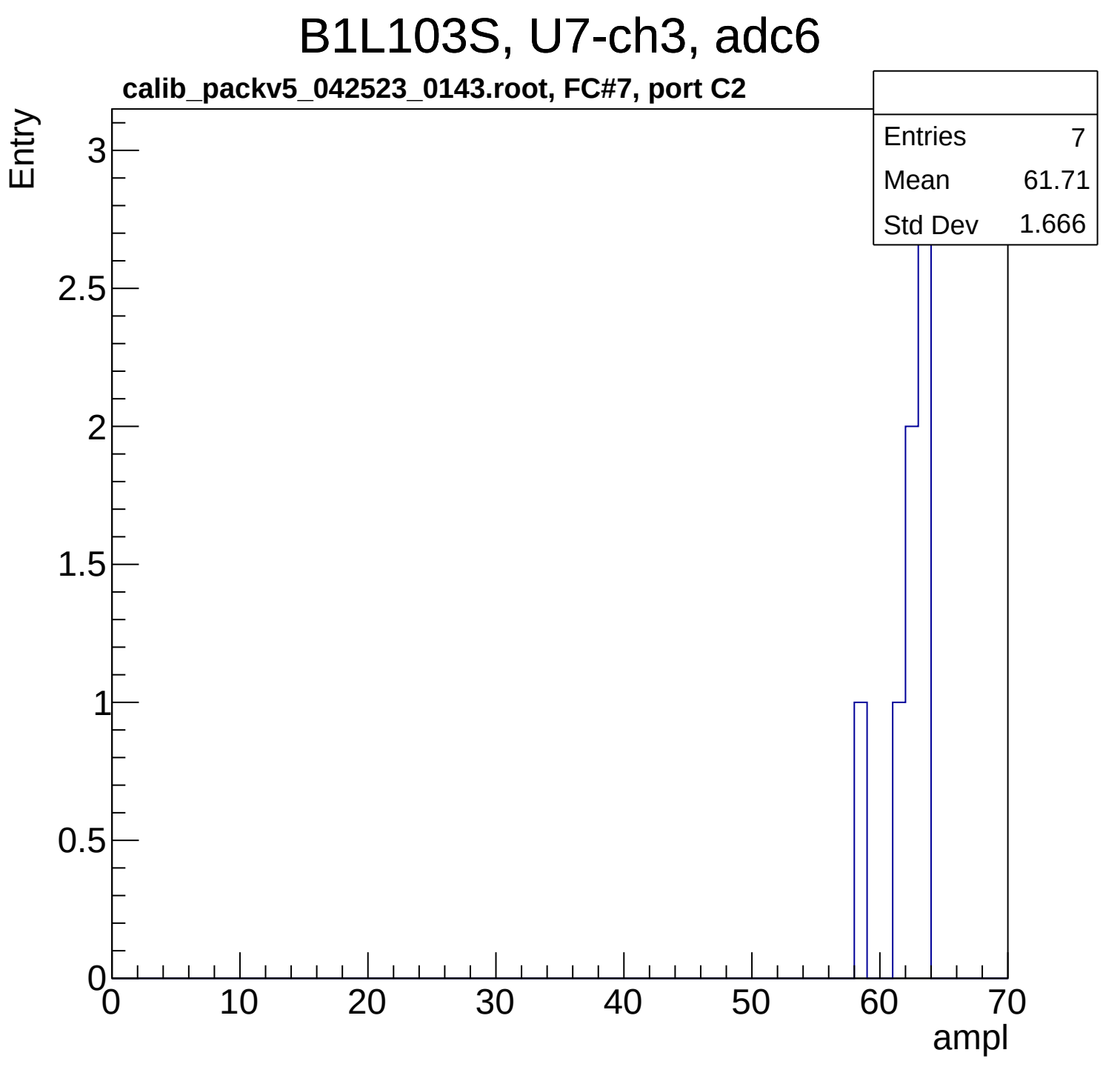

B1L103S, U7-ch3, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 43
Mean 58.91
Std Dev 9.351
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch3, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 7
Mean 61.71
Std Dev 1.666
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
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40
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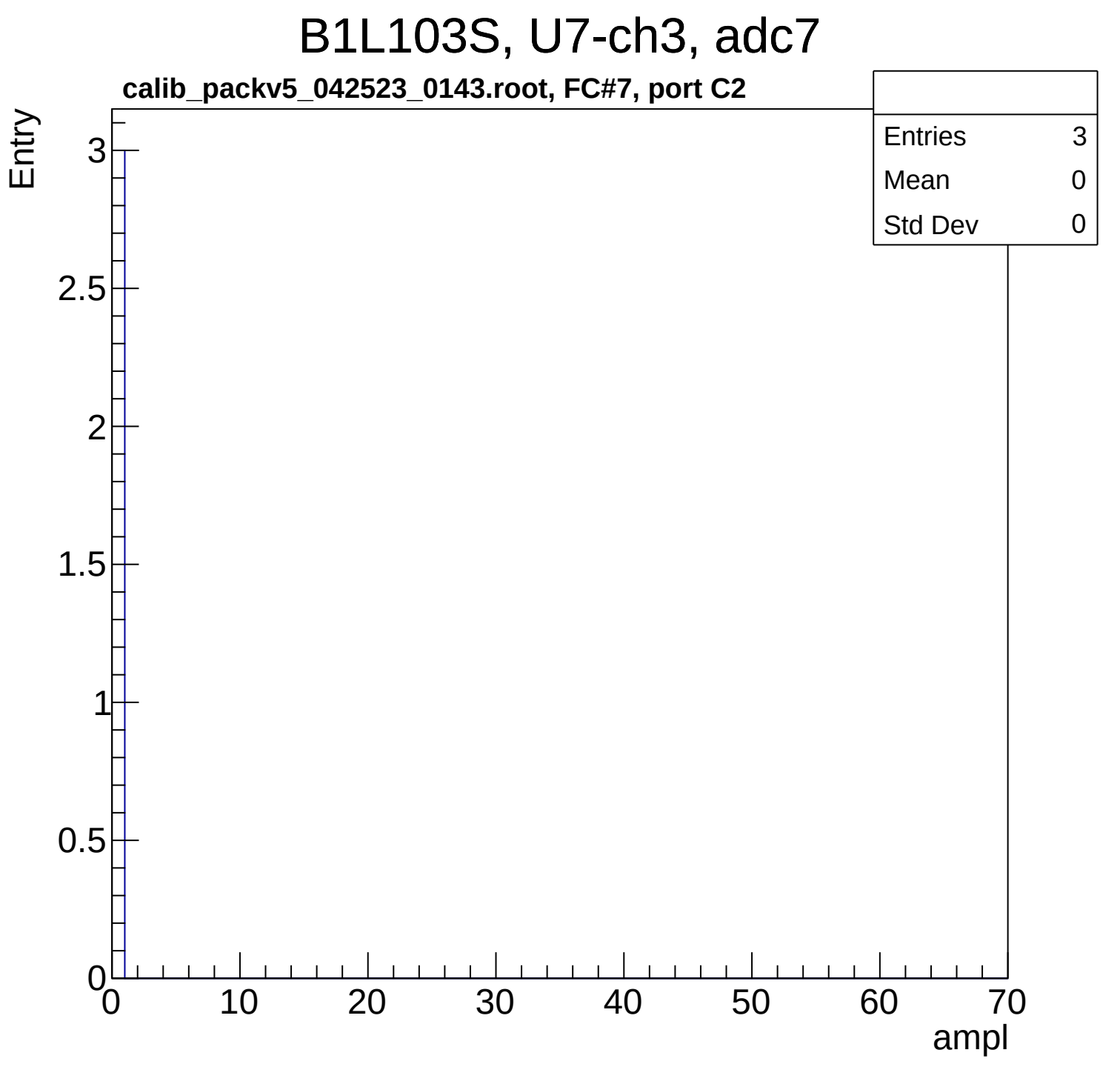
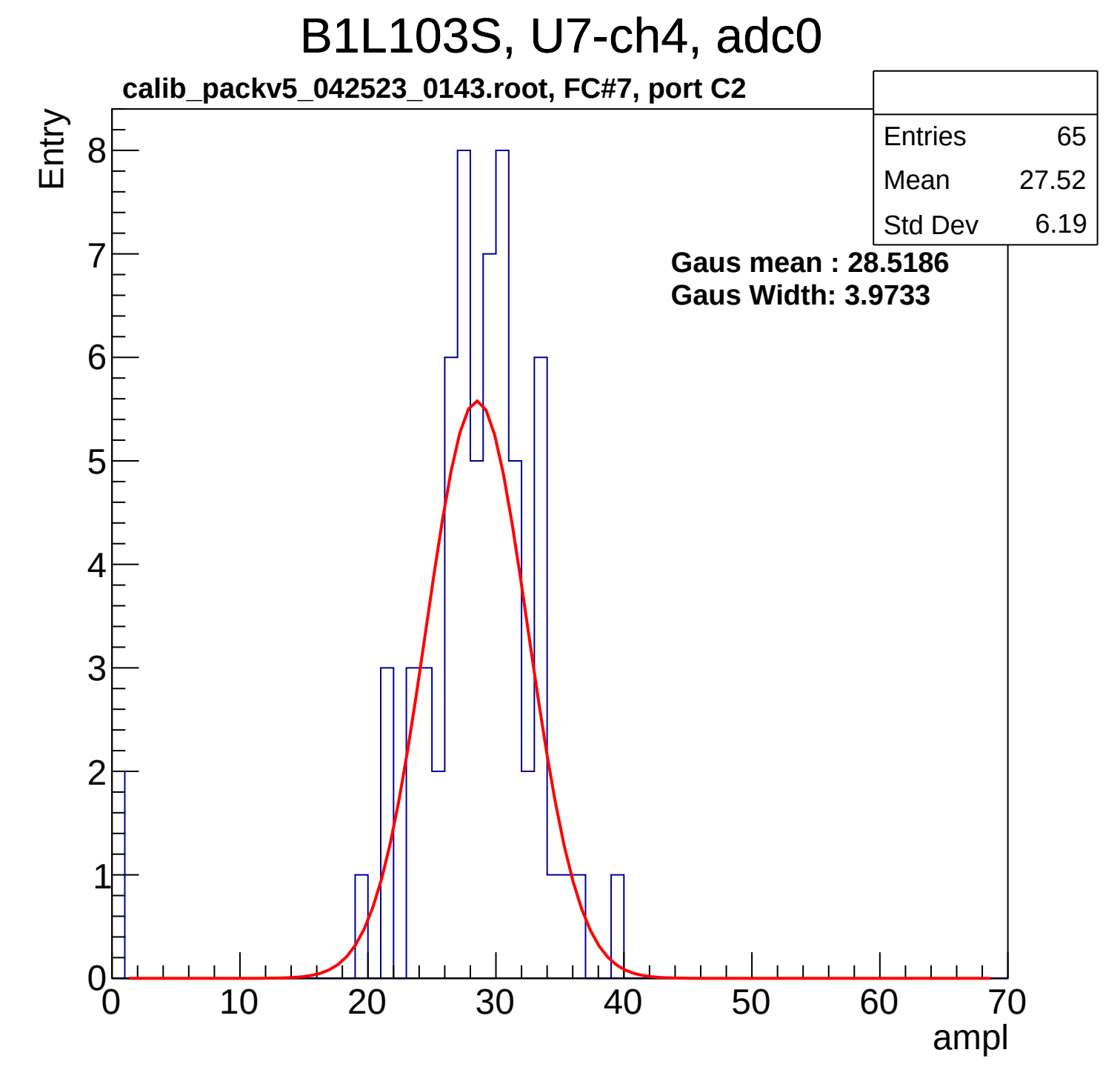
60
70


B1L103S, U7-ch3, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 0
Std Dev 0
Entry
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch4, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 27.52
Std Dev 6.19
Gaus mean : 28.5186
Gaus Width: 3.9733
Entry
ampl
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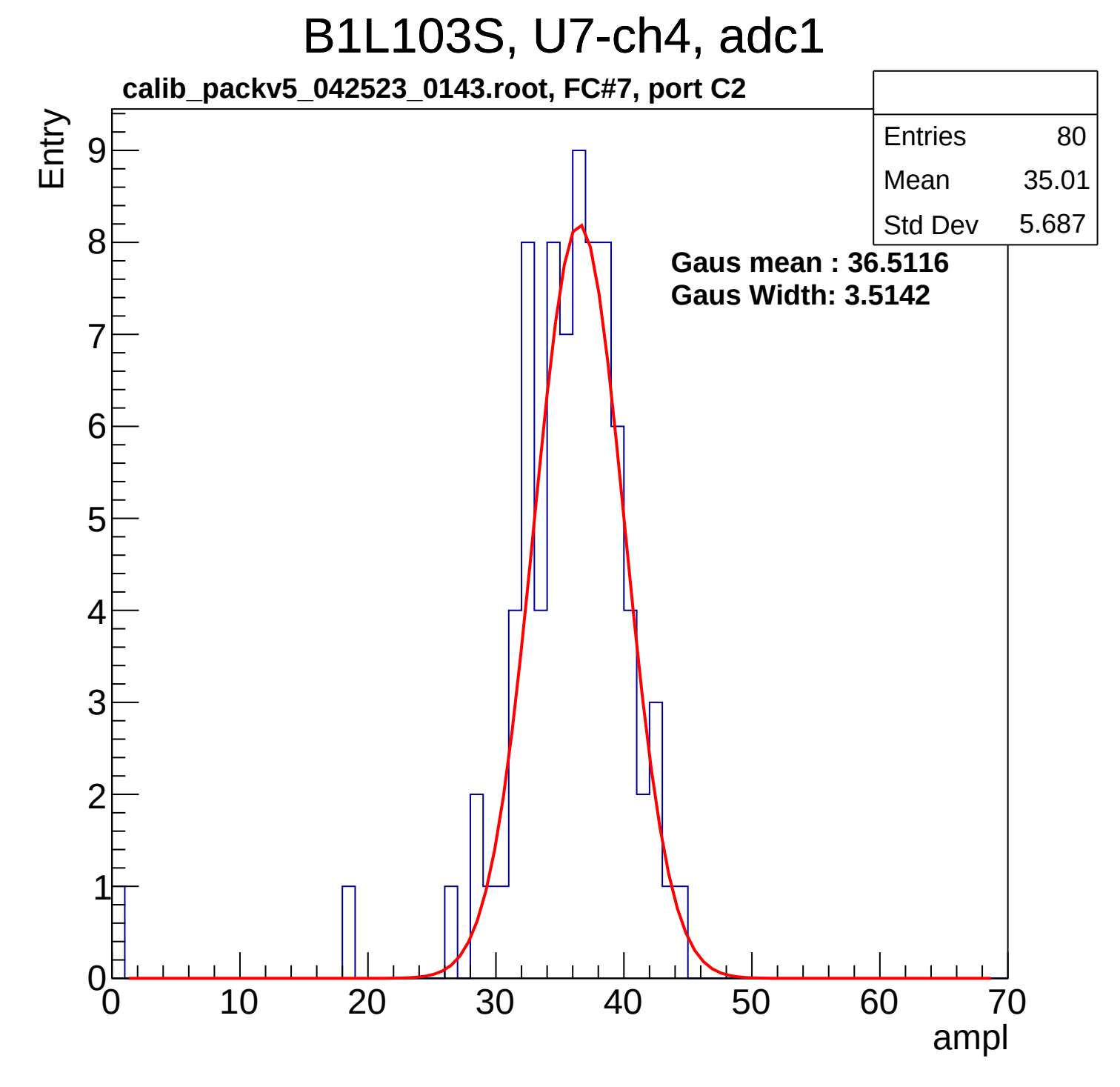
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch4, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 80
Mean 35.01
Std Dev 5.687
Gaus mean : 36.5116
Gaus Width: 3.5142
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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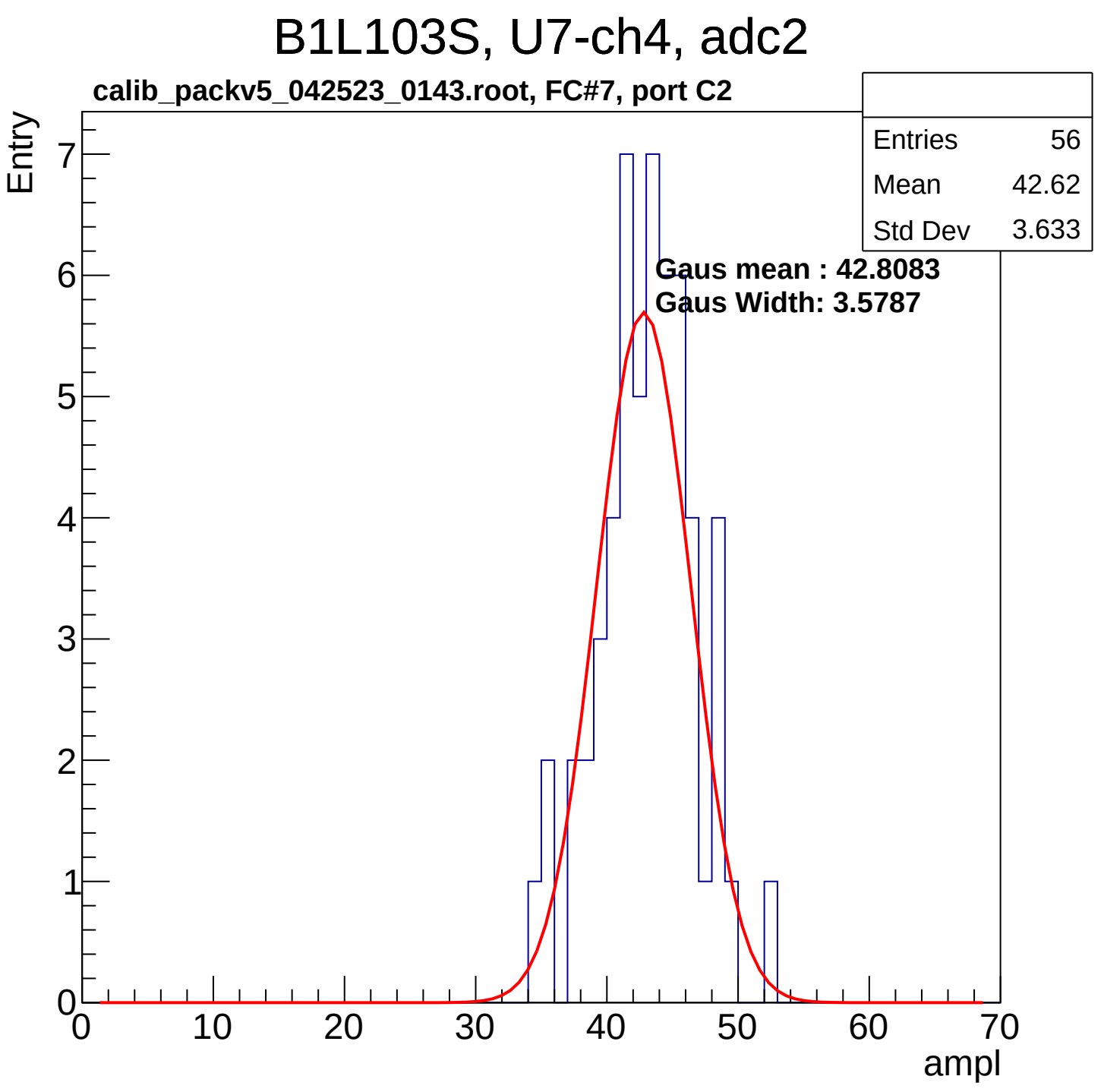
B1L103S, U7-ch4, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 42.62
Std Dev 3.633
Gaus mean : 42.8083
Gaus Width: 3.5787
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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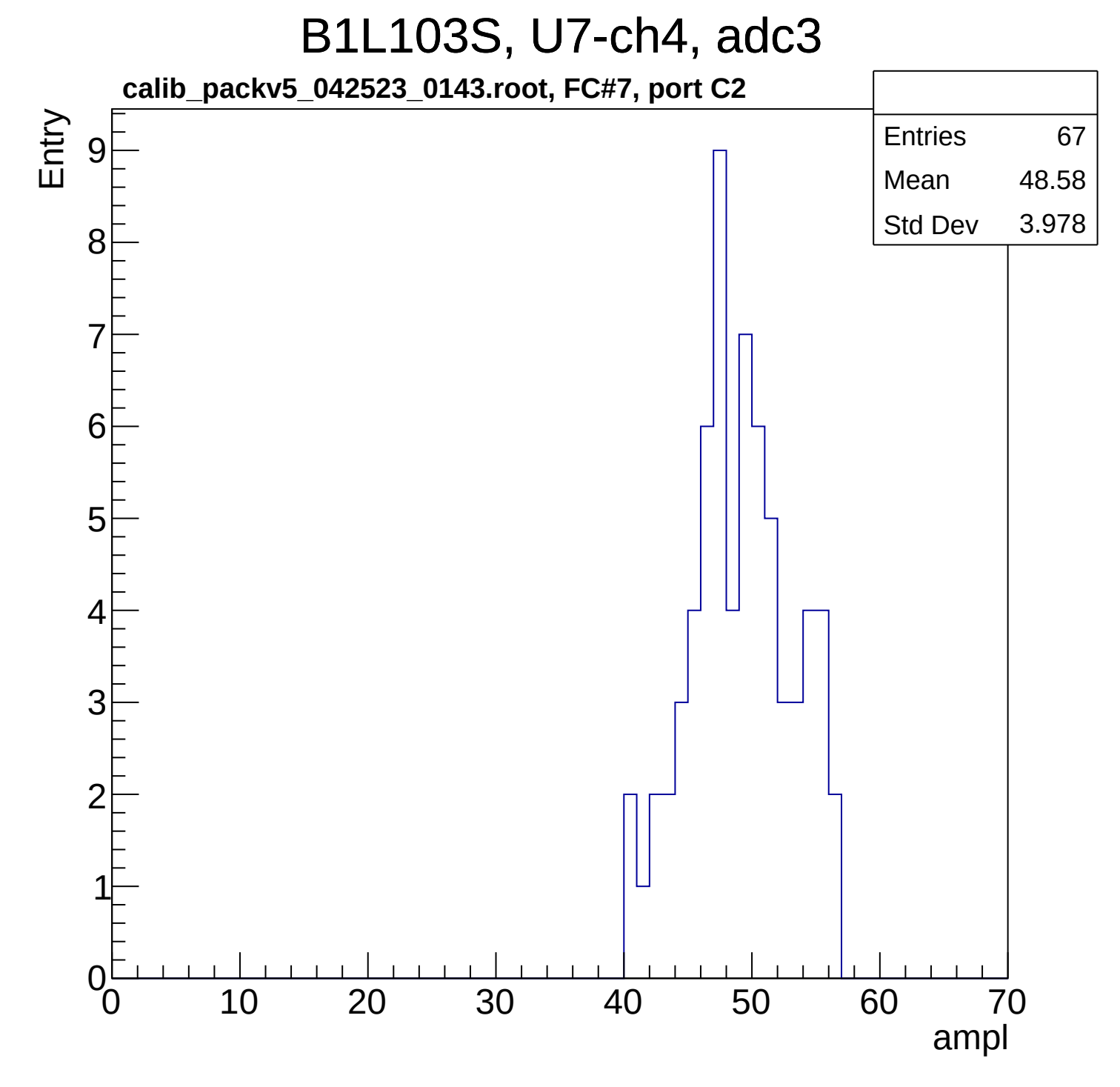
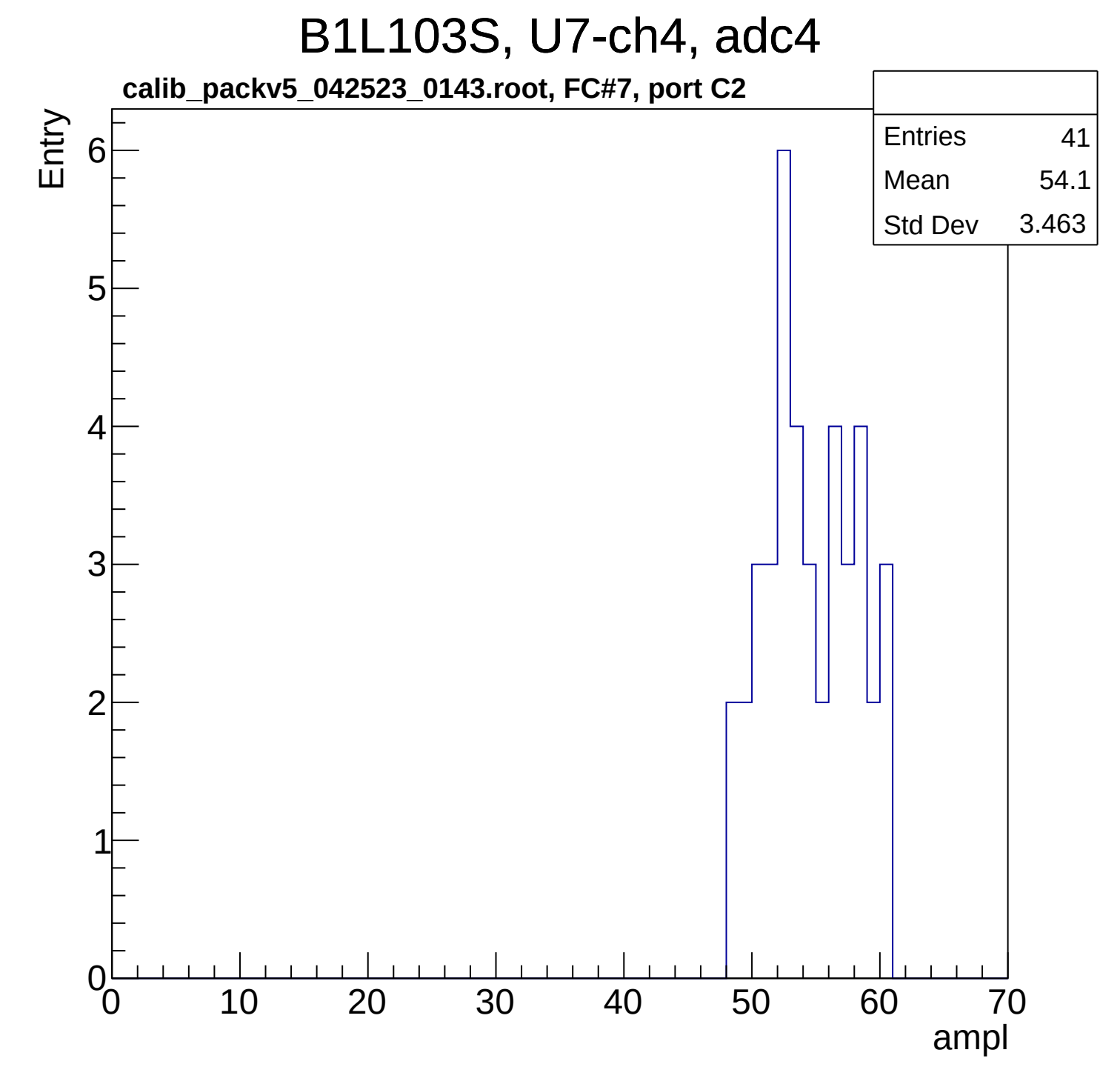
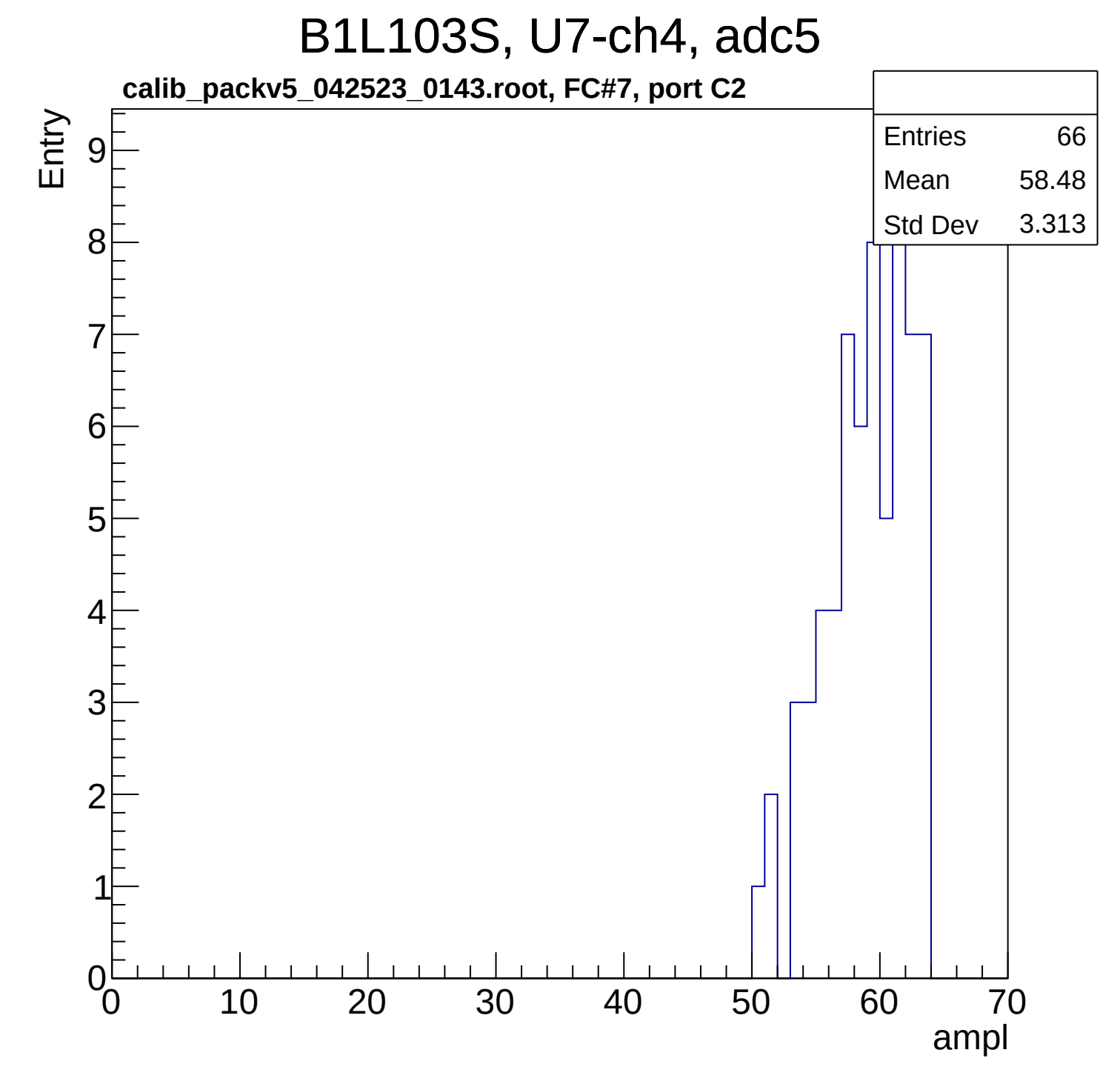

B1L103S, U7-ch4, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 48.58
Std Dev 3.978
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch4, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 41
Mean 54.1
Std Dev 3.463
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch4, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 58.48
Std Dev 3.313
Entry
ampl
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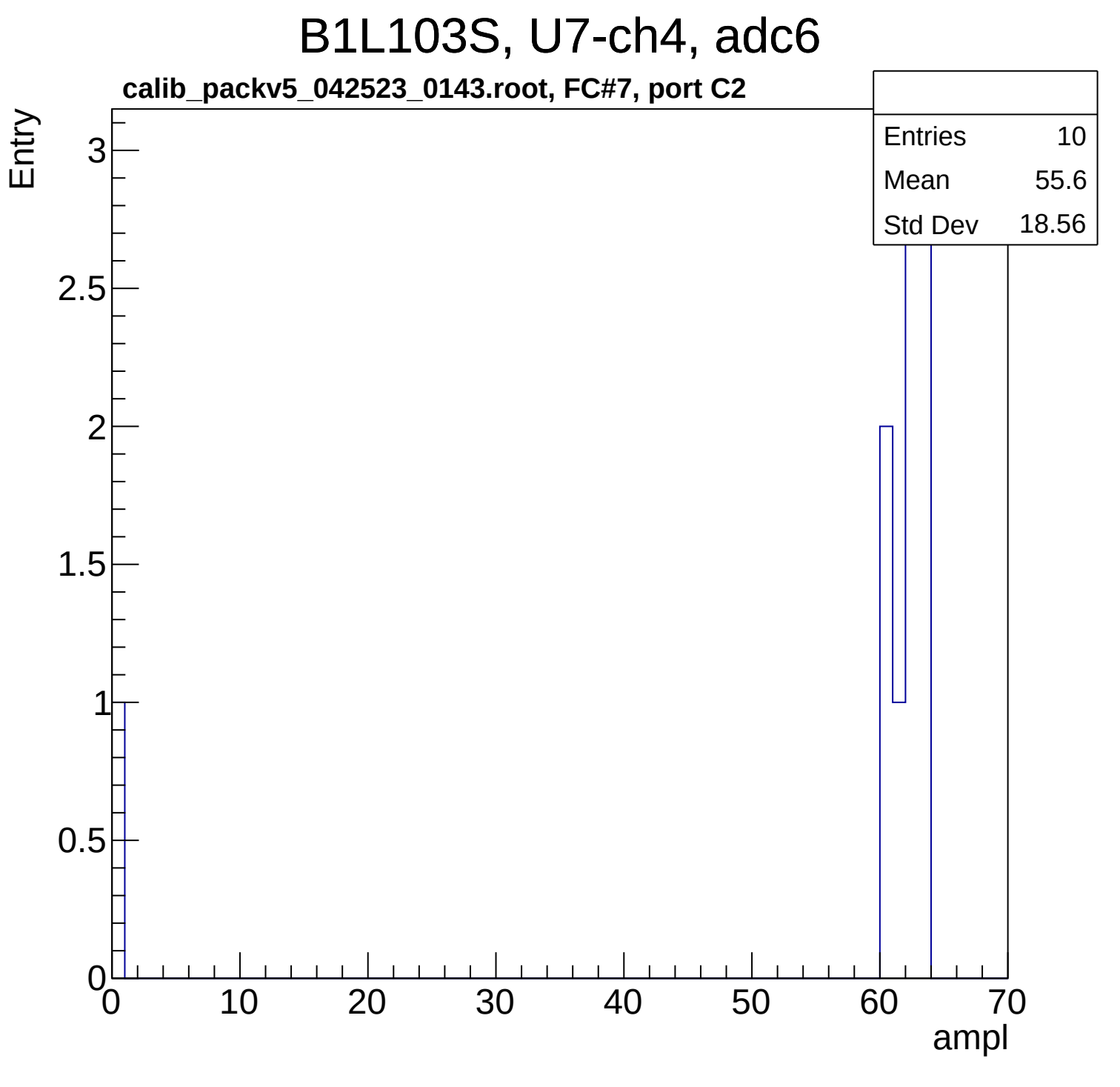
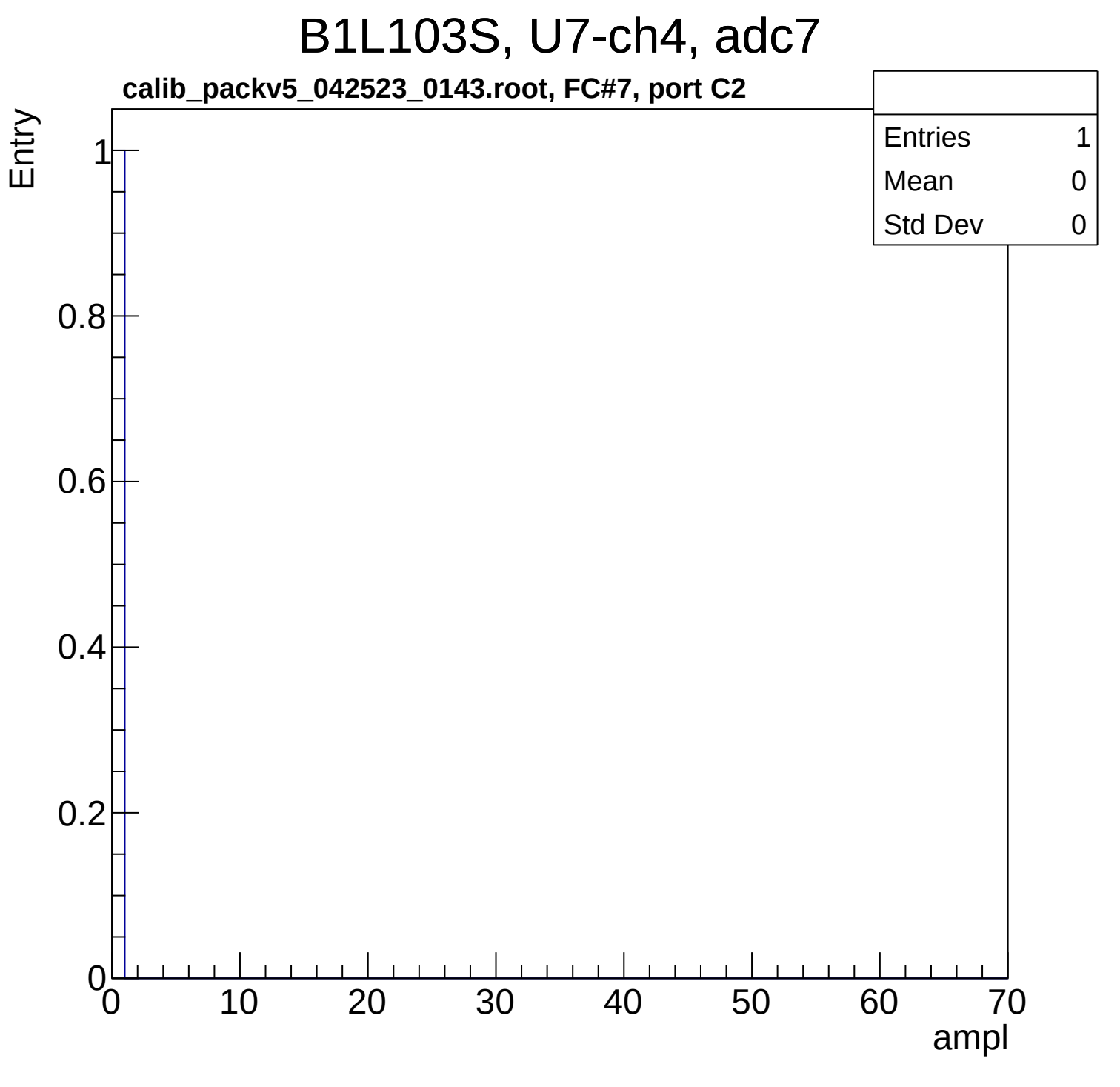
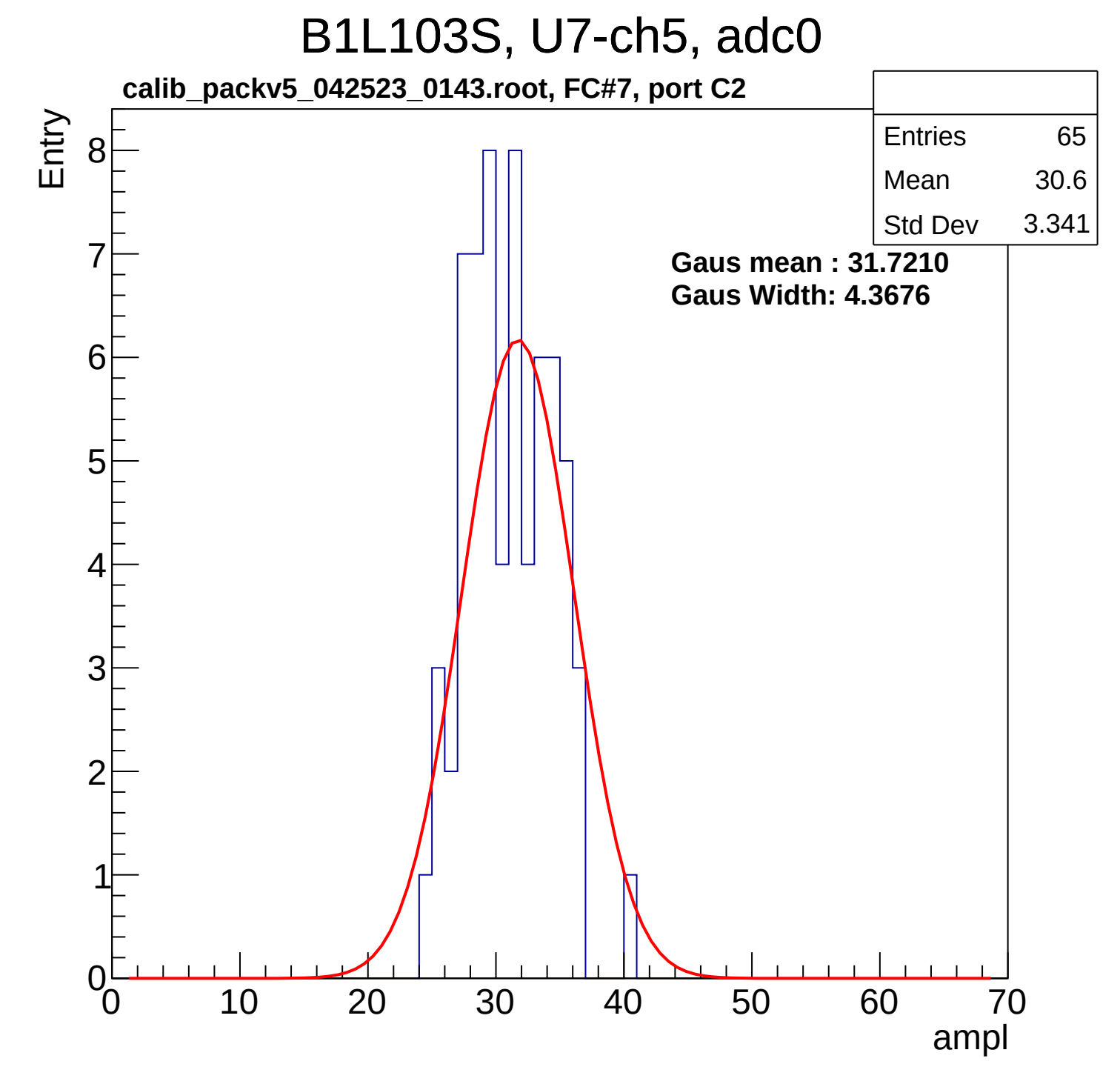
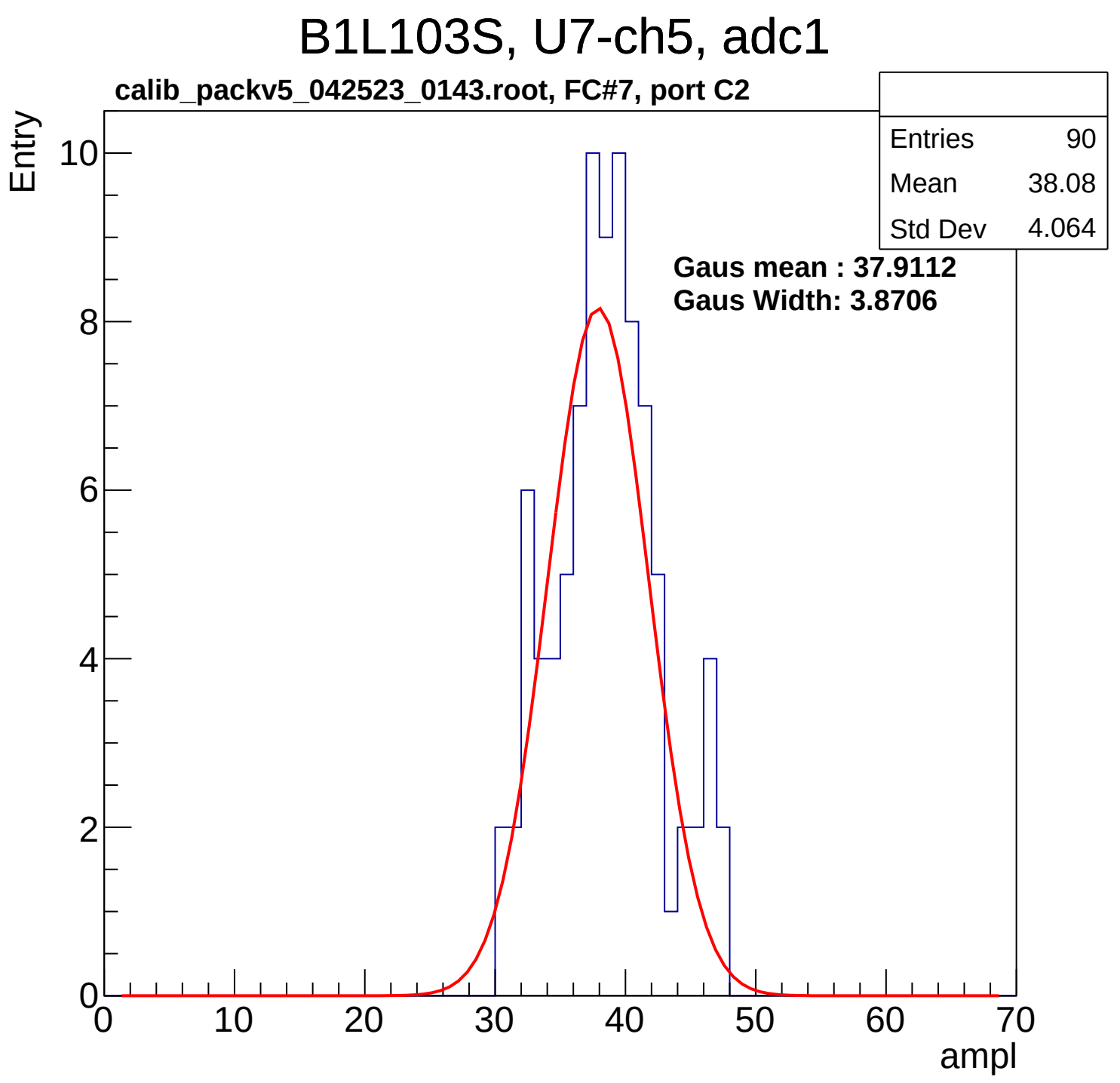
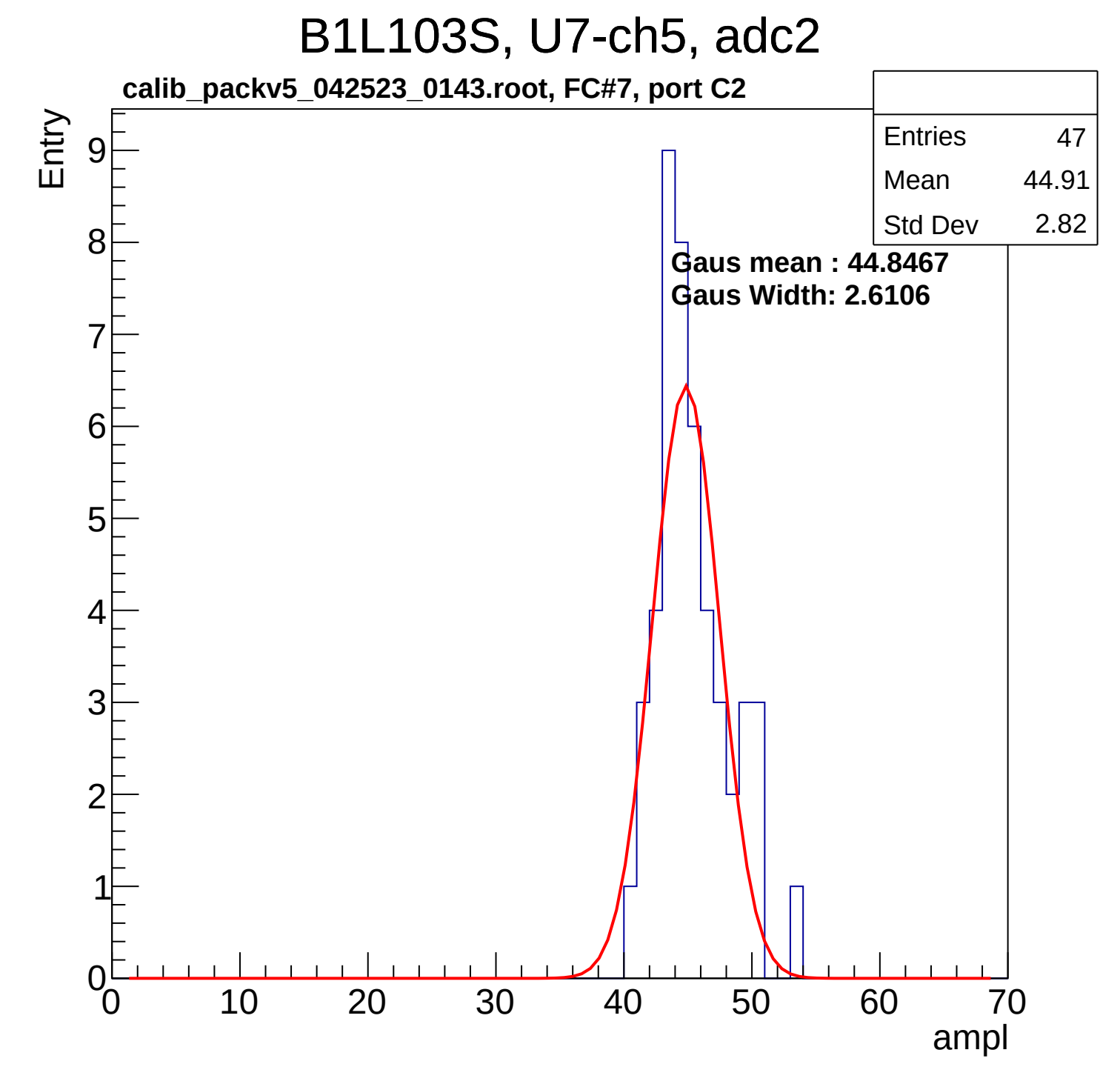
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

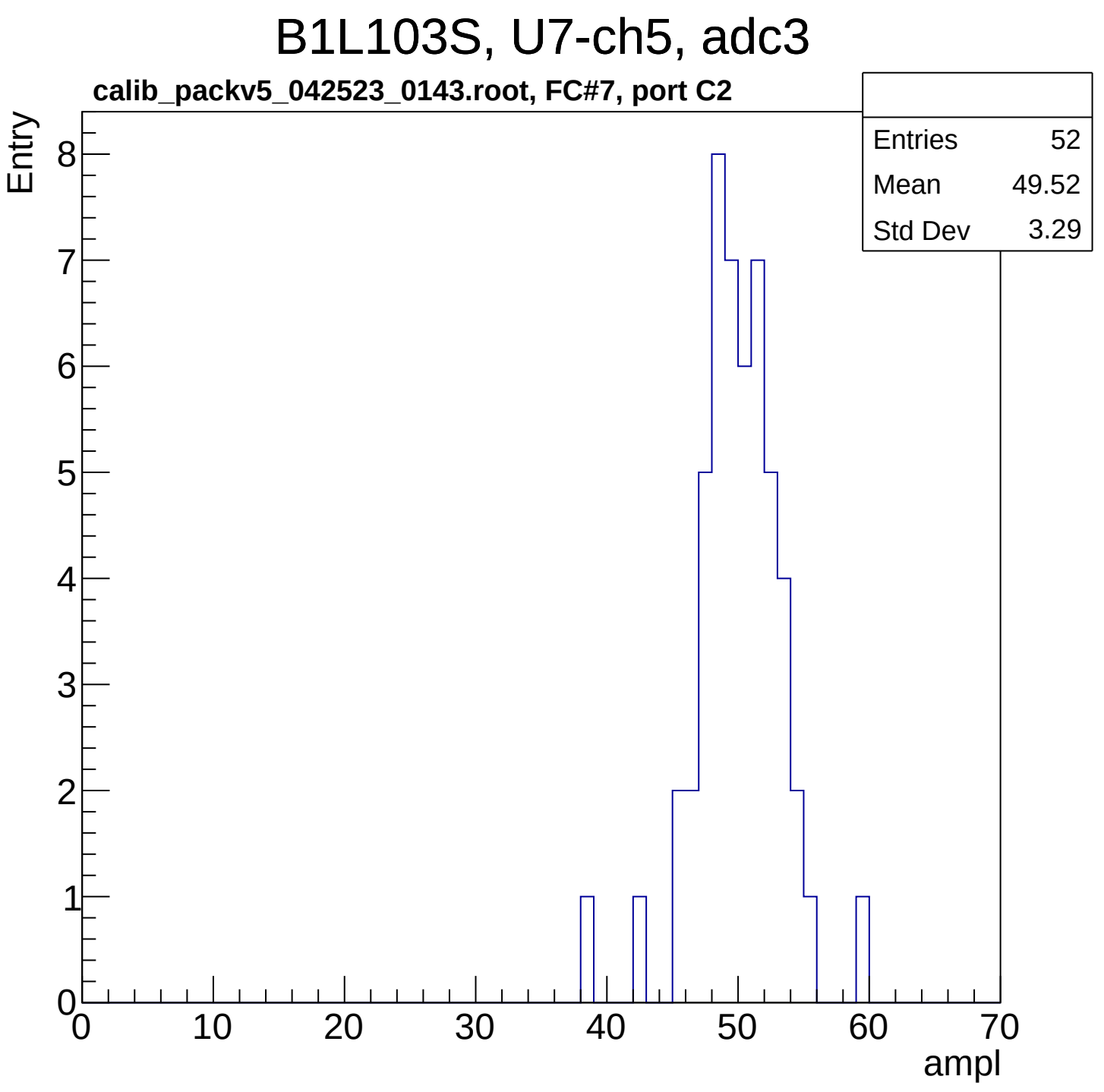

B1L103S, U7-ch4, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 10
Mean 55.6
Std Dev 18.56
Entry
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl

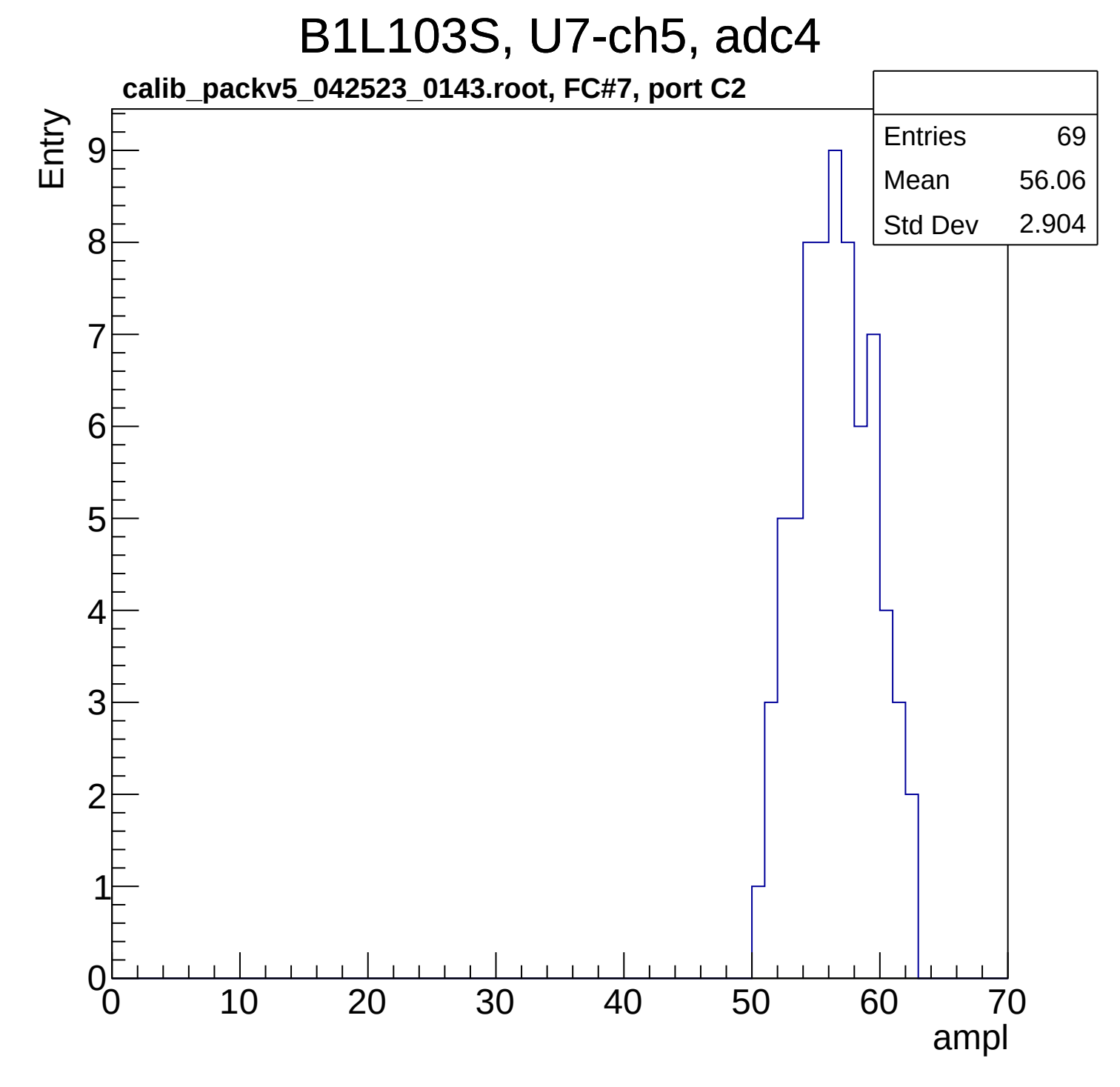

B1L103S, U7-ch4, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch5, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 30.6
Std Dev 3.341
Gaus mean : 31.7210
Gaus Width: 4.3676
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch5, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 90
Mean 38.08
Std Dev 4.064
Gaus mean : 37.9112
Gaus Width: 3.8706
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch5, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 47
Mean 44.91
Std Dev 2.82
Gaus mean : 44.8467
Gaus Width: 2.6106
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch5, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 52
Mean 49.52
Std Dev 3.29
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch5, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 56.06
Std Dev 2.904
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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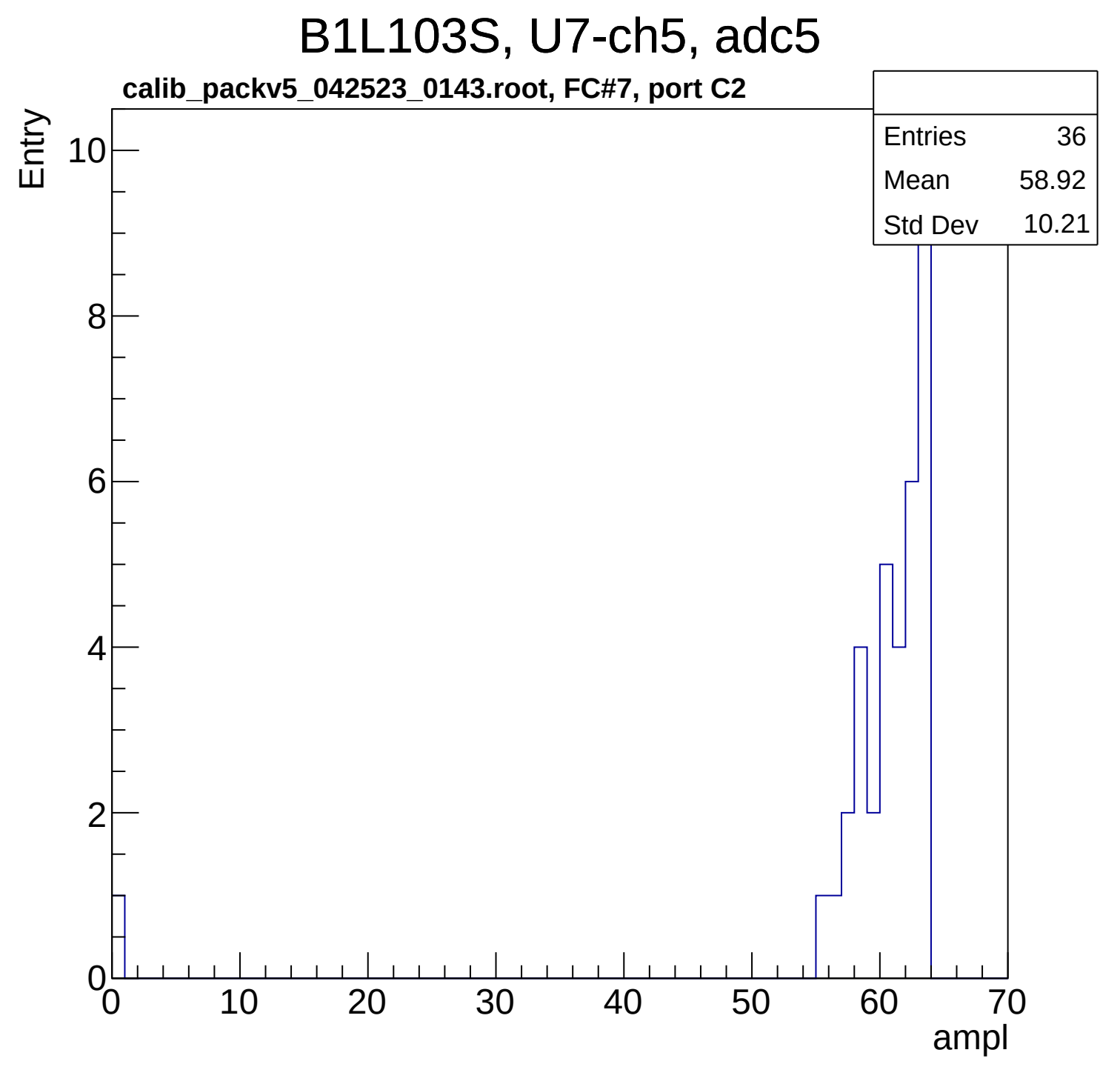
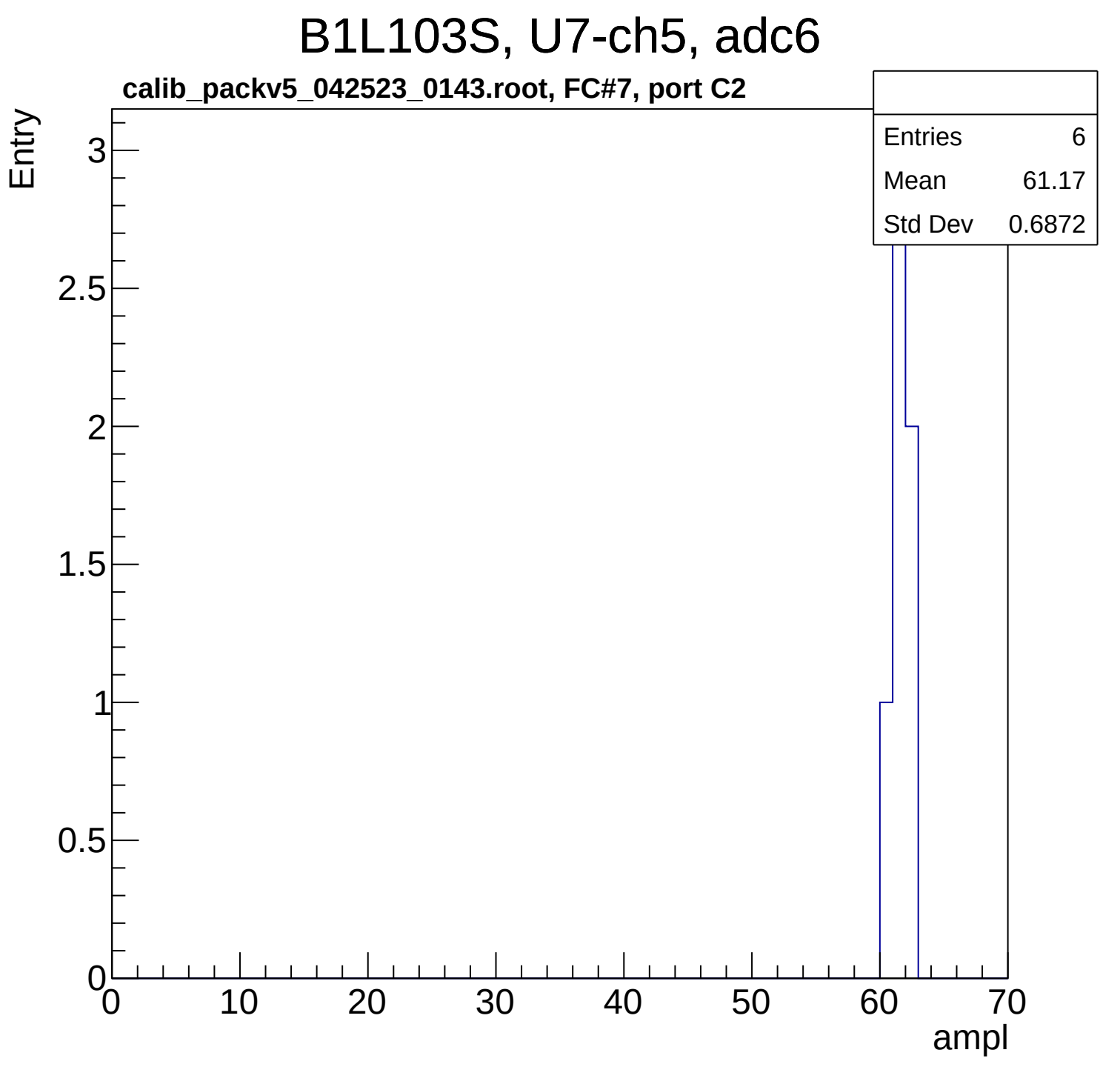
40
50
60
70


B1L103S, U7-ch5, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 36
Mean 58.92
Std Dev 10.21
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch5, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 6
Mean 61.17
Std Dev 0.6872
Entry
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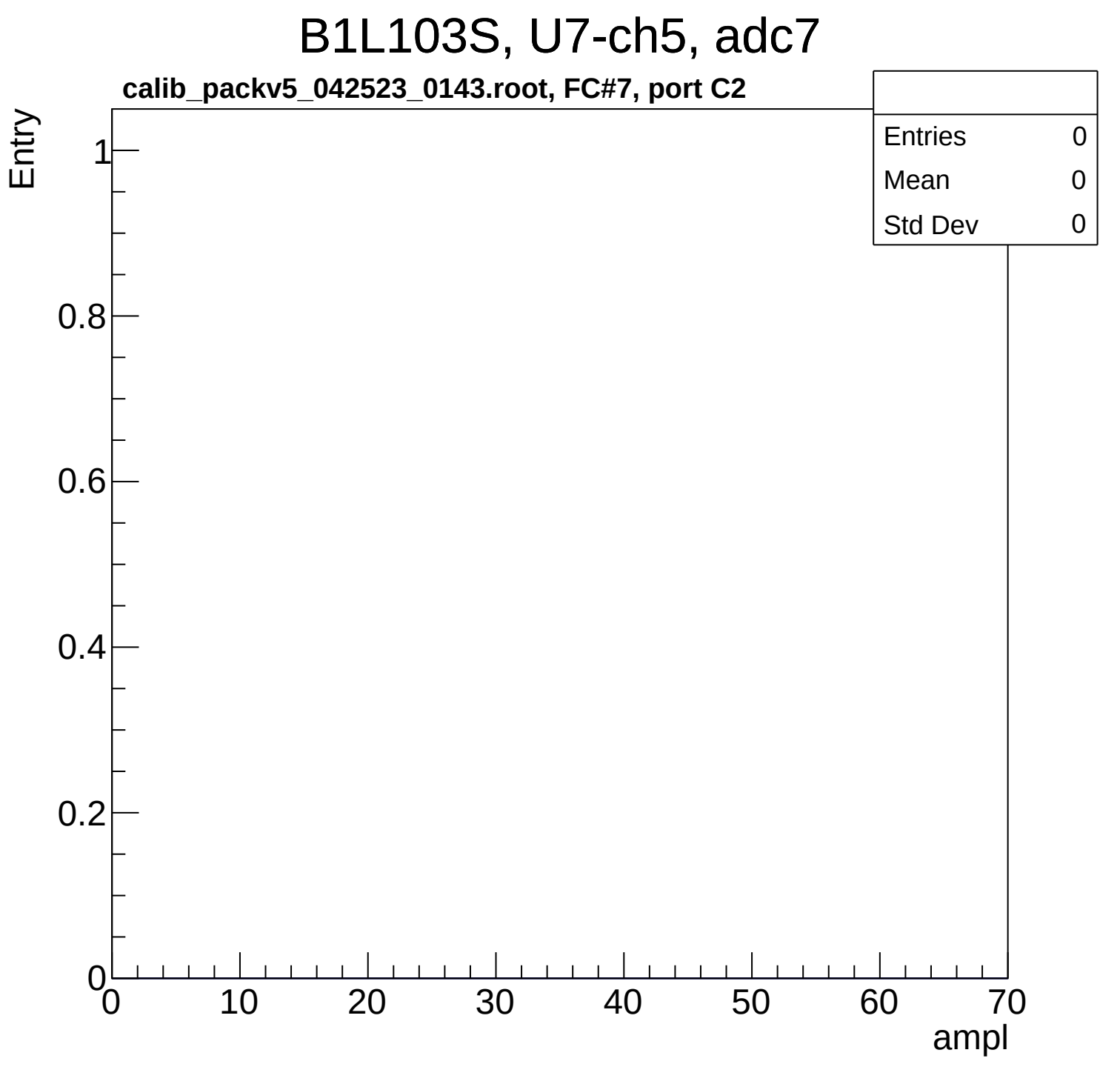
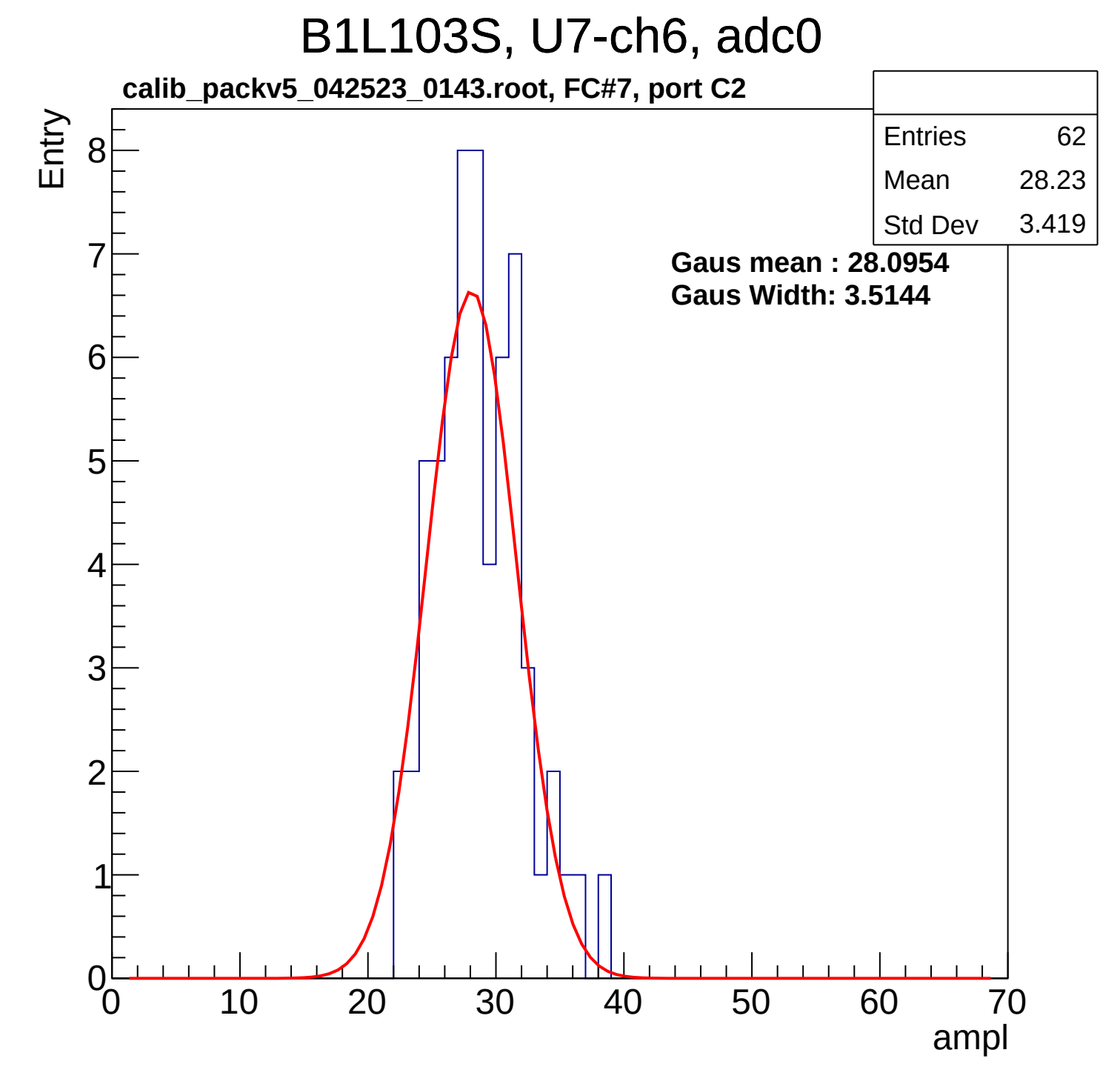
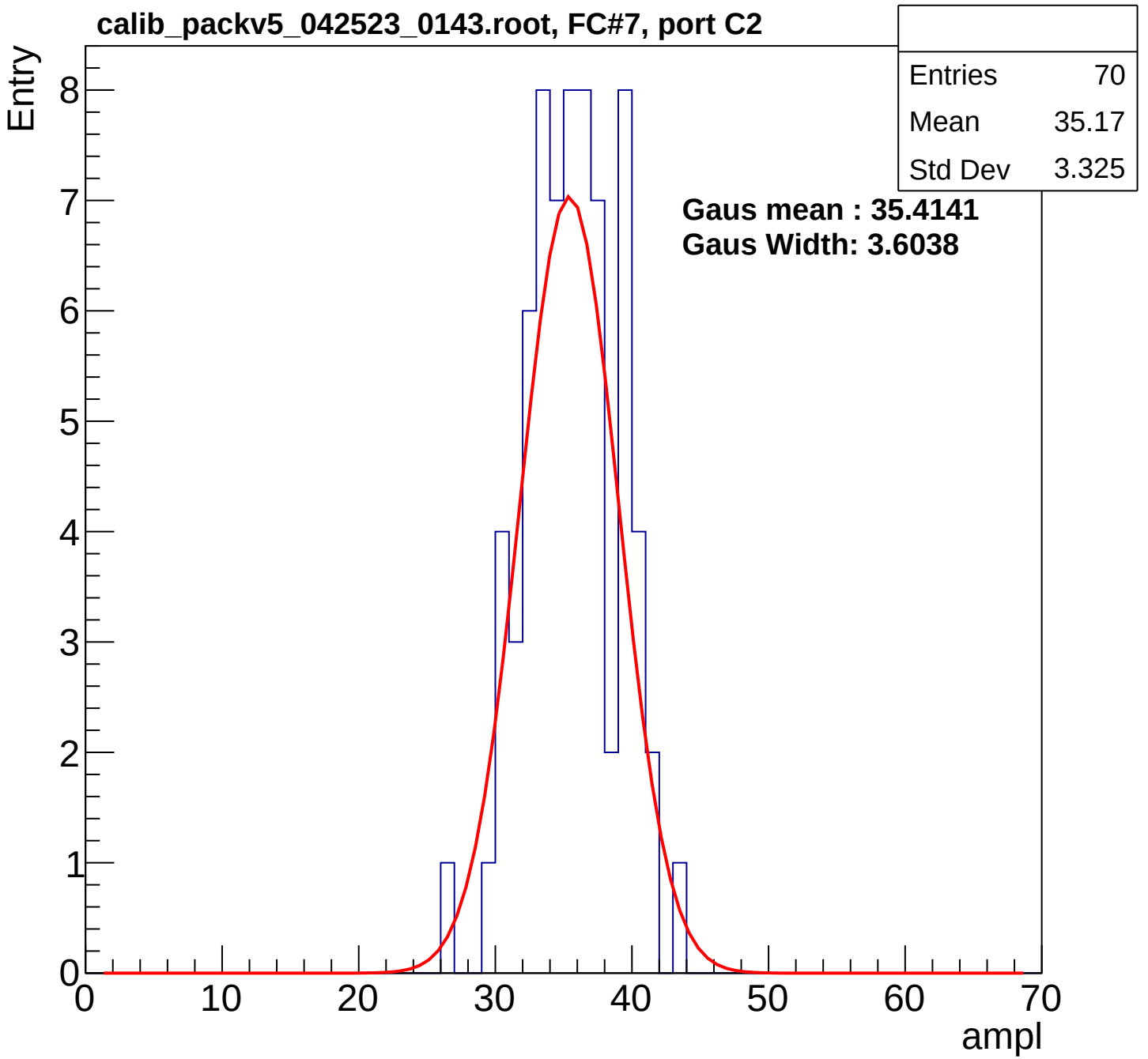
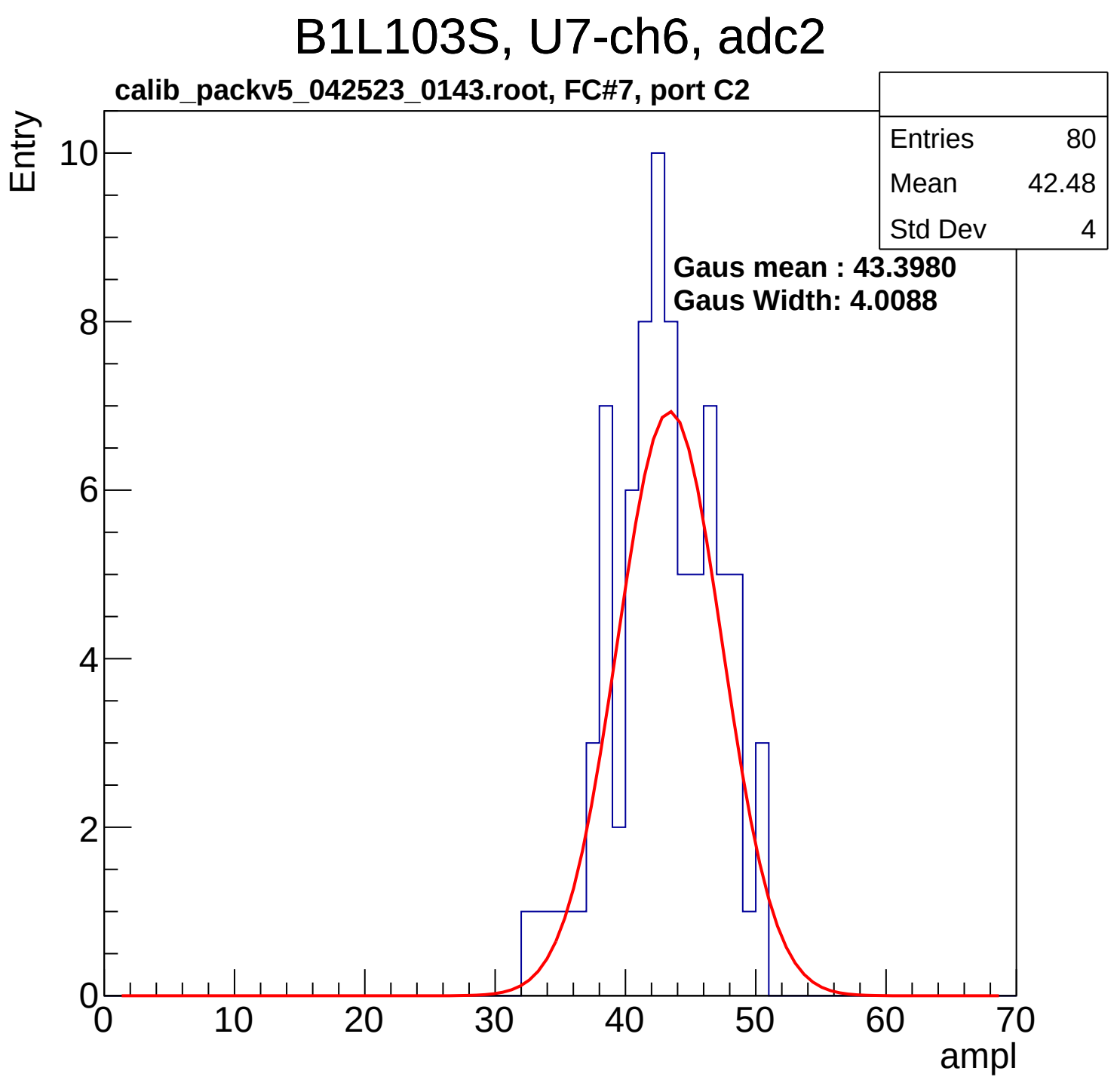
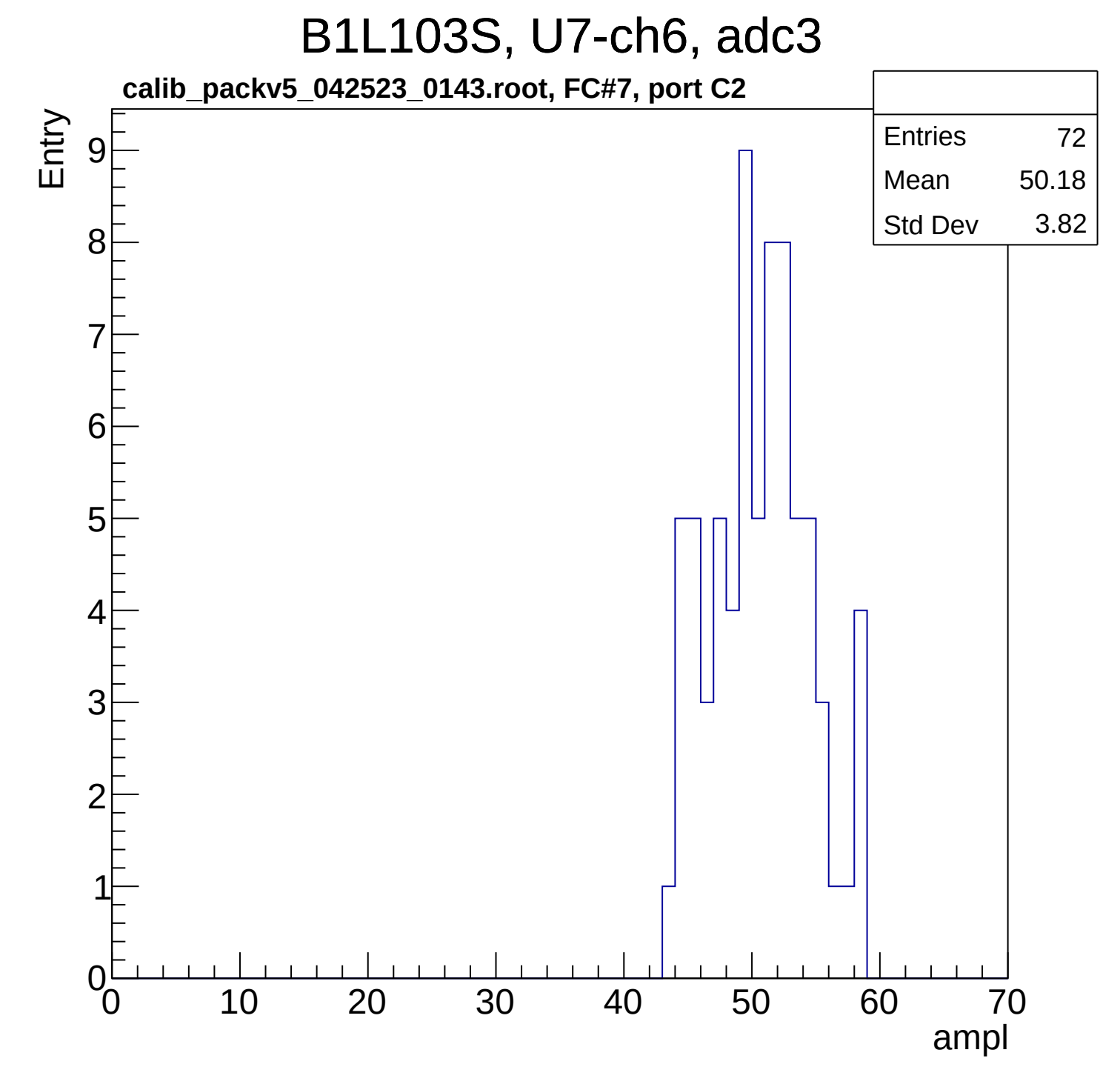
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch5, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch6, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 62
Mean 28.23
Std Dev 3.419
Gaus mean : 28.0954
Gaus Width: 3.5144
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch6, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 35.17
Std Dev 3.325
Gaus mean : 35.4141
Gaus Width: 3.6038
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch6, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 80
Mean 42.48
Std Dev 4
Gaus mean : 43.3980
Gaus Width: 4.0088
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch6, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 72
Mean 50.18
Std Dev 3.82
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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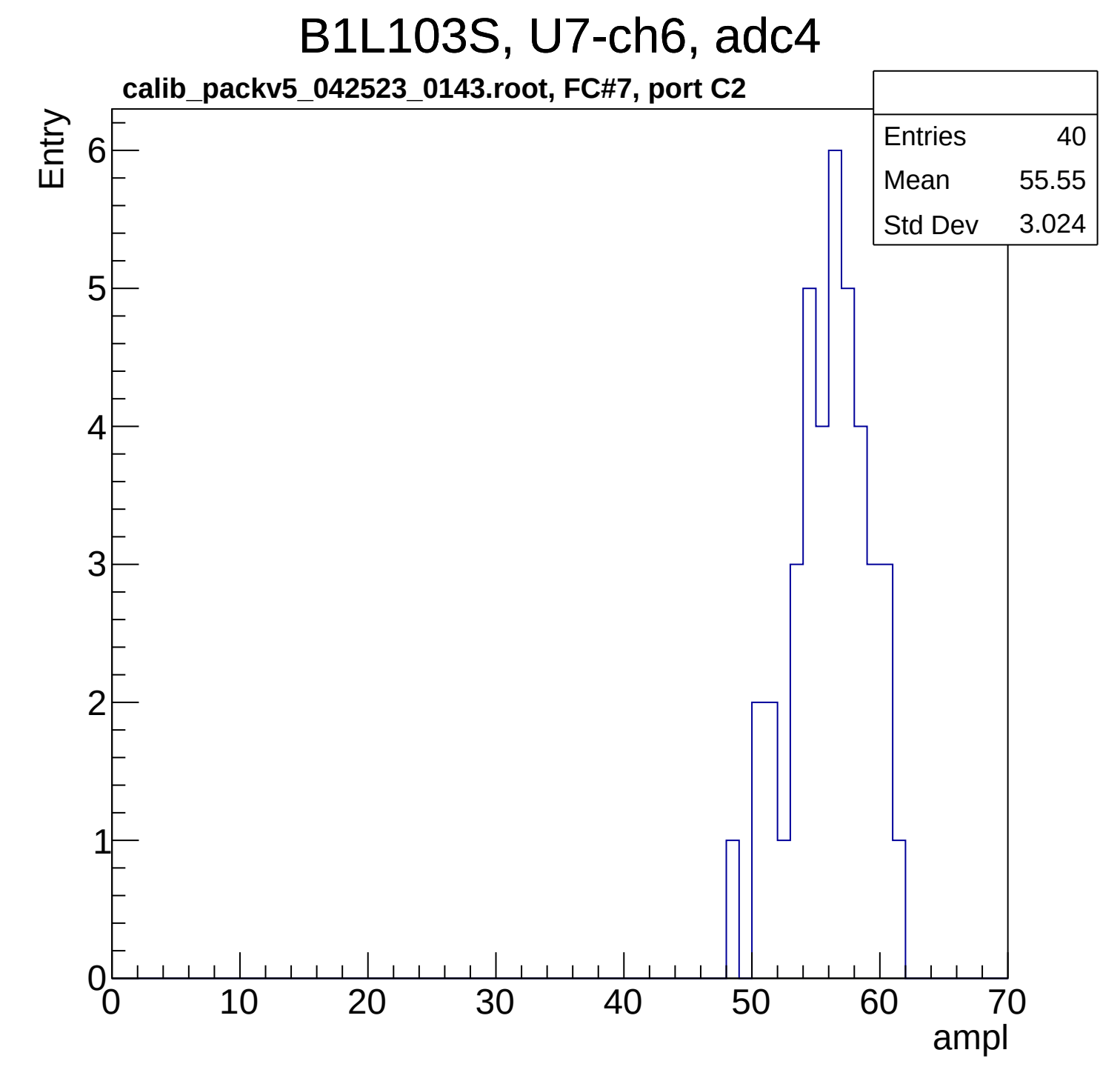
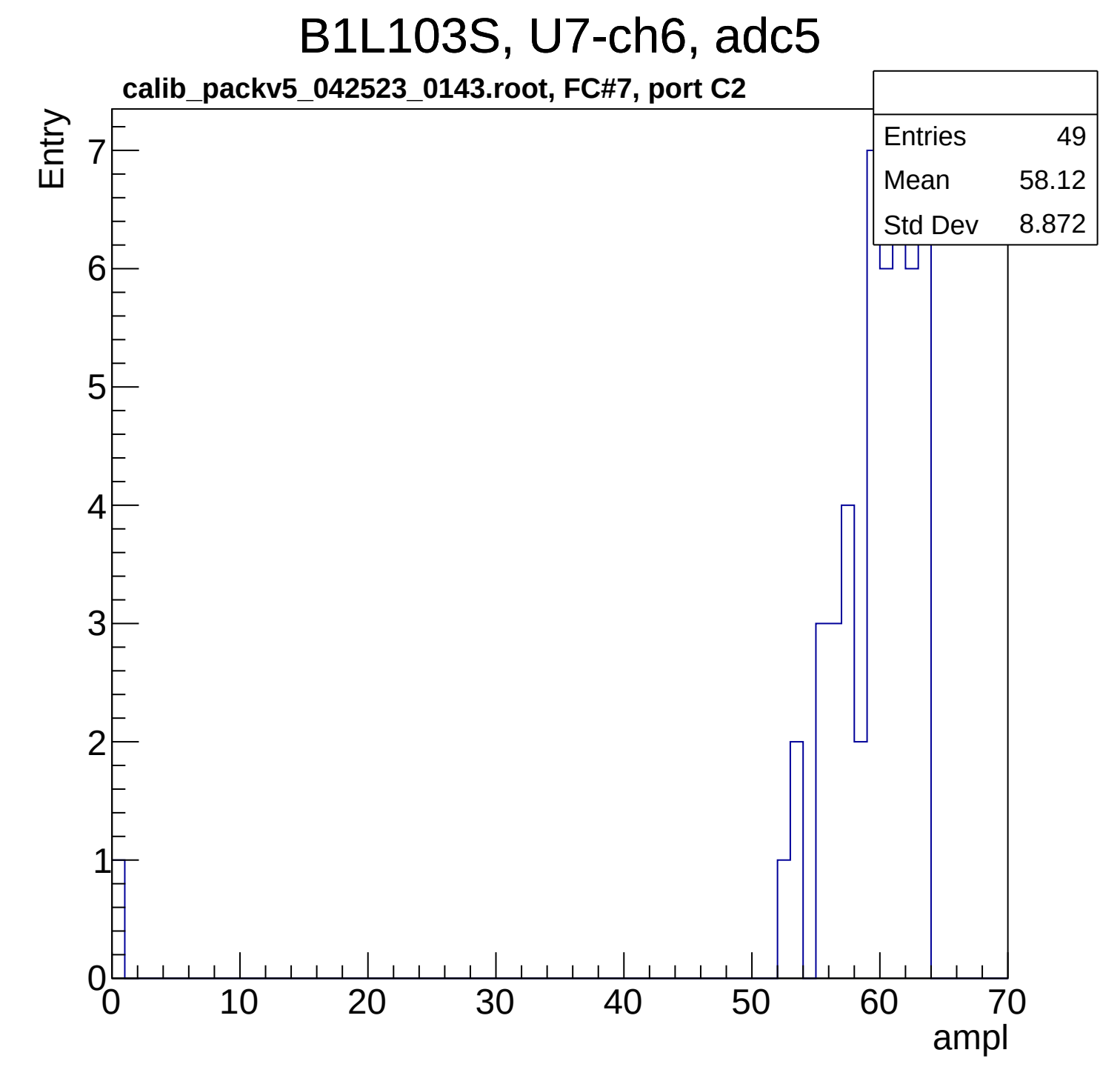

B1L103S, U7-ch6, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 40
Mean 55.55
Std Dev 3.024
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch6, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 49
Mean 58.12
Std Dev 8.872
Entry
ampl
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1
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3
4
5
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0
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20
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40
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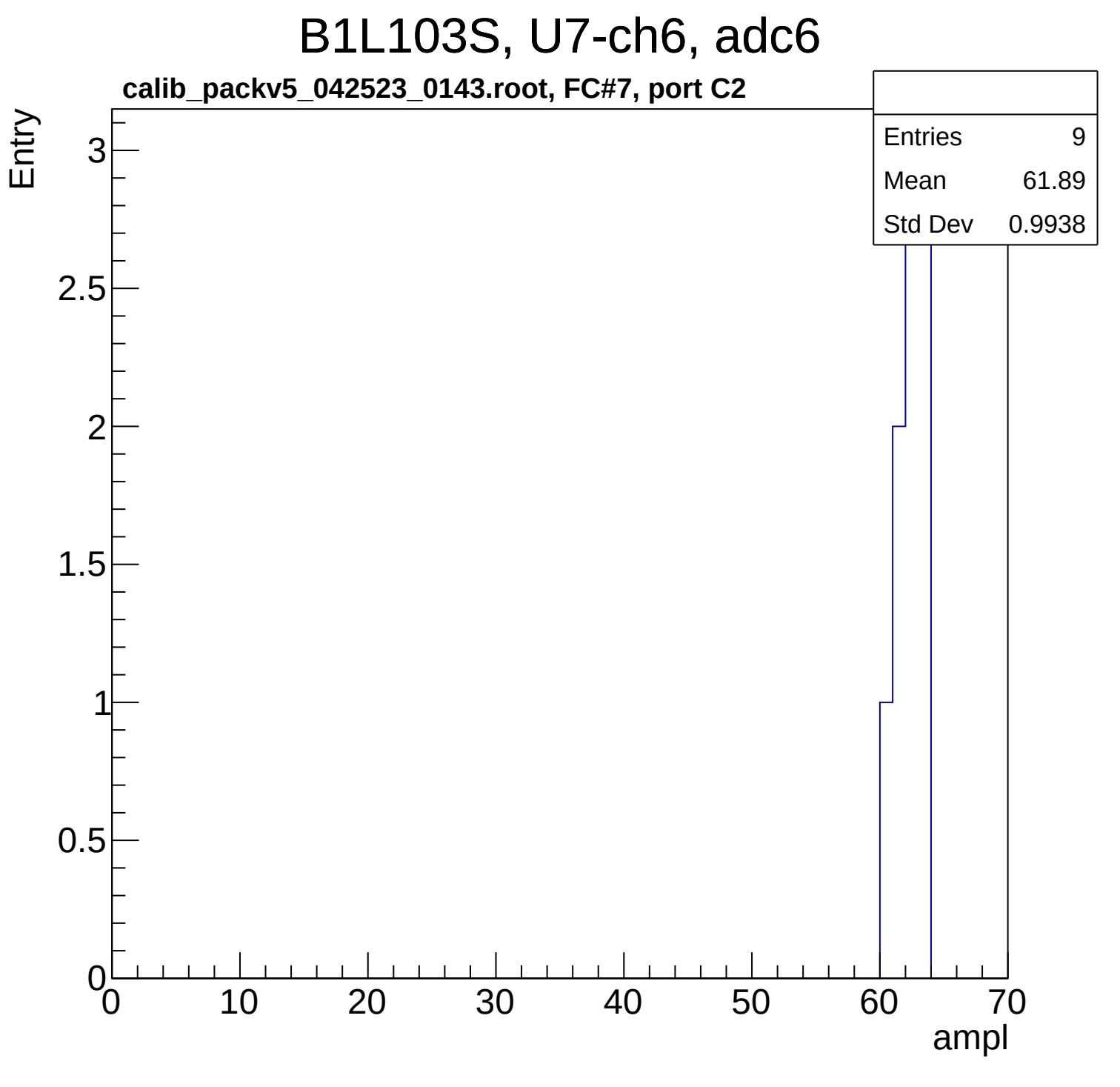
60
70


B1L103S, U7-ch6, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 9
Mean 61.89
Std Dev 0.9938
Entry
ampl
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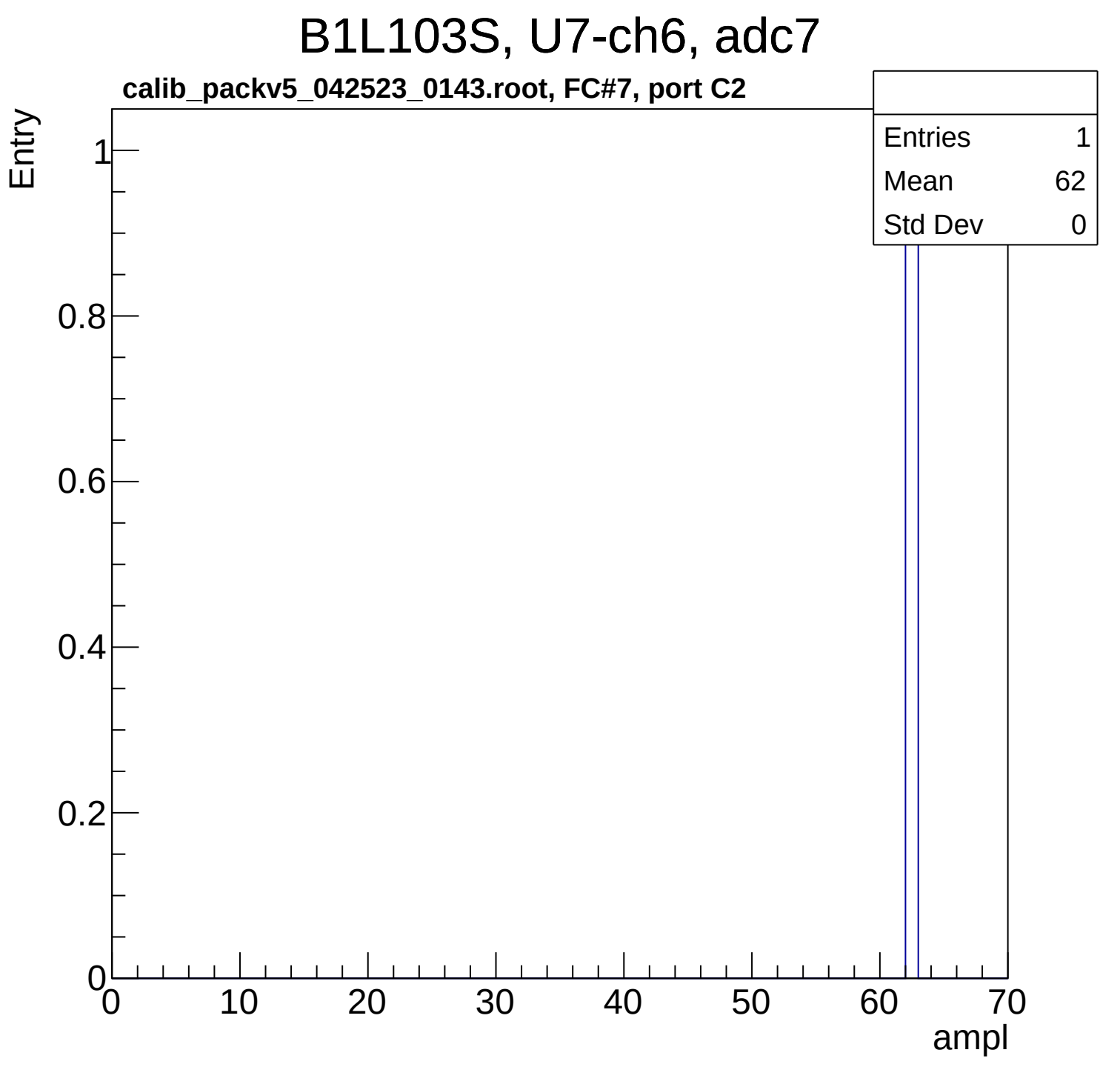
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U7-ch6, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 62
Std Dev 0
Entry
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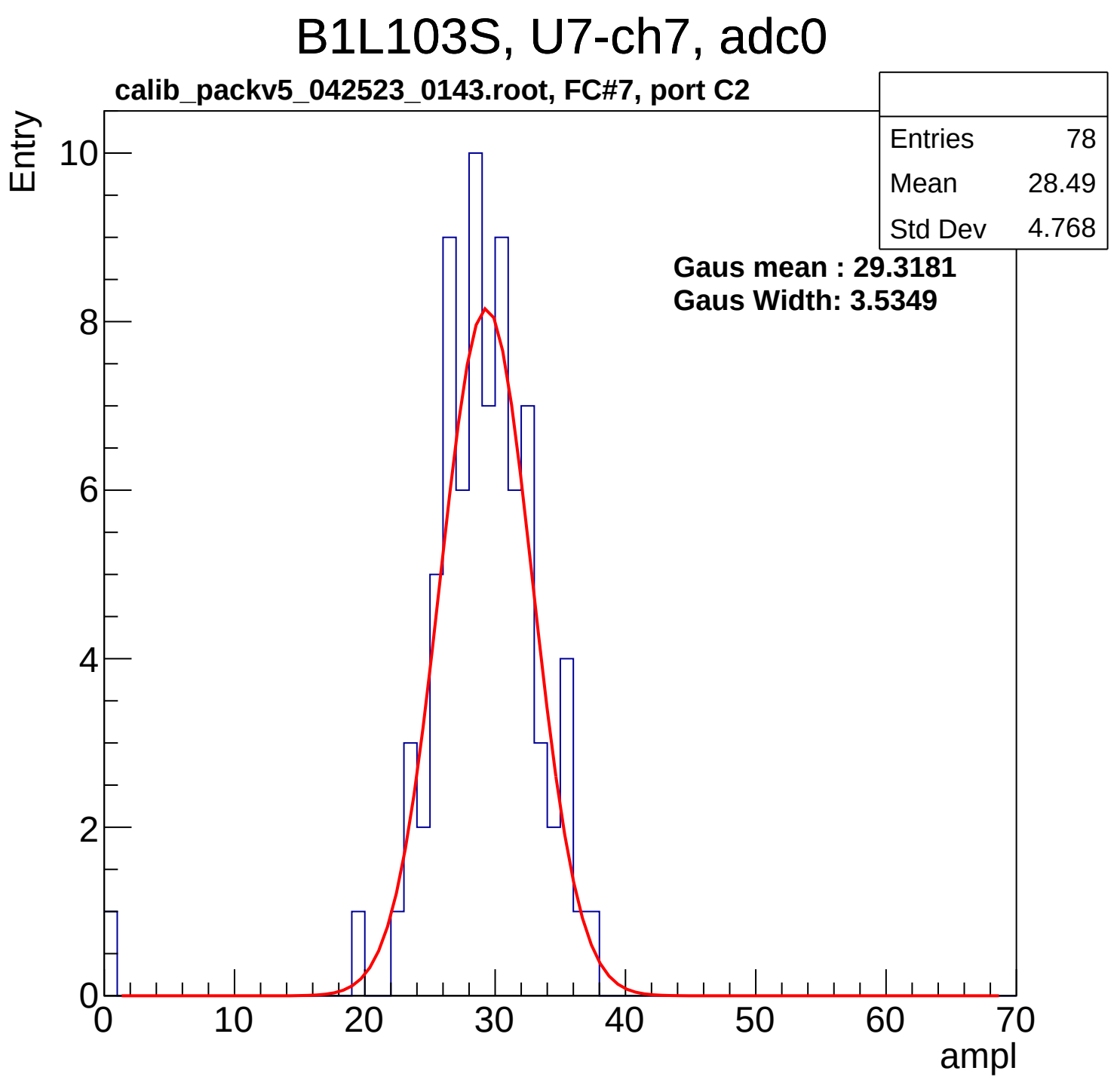
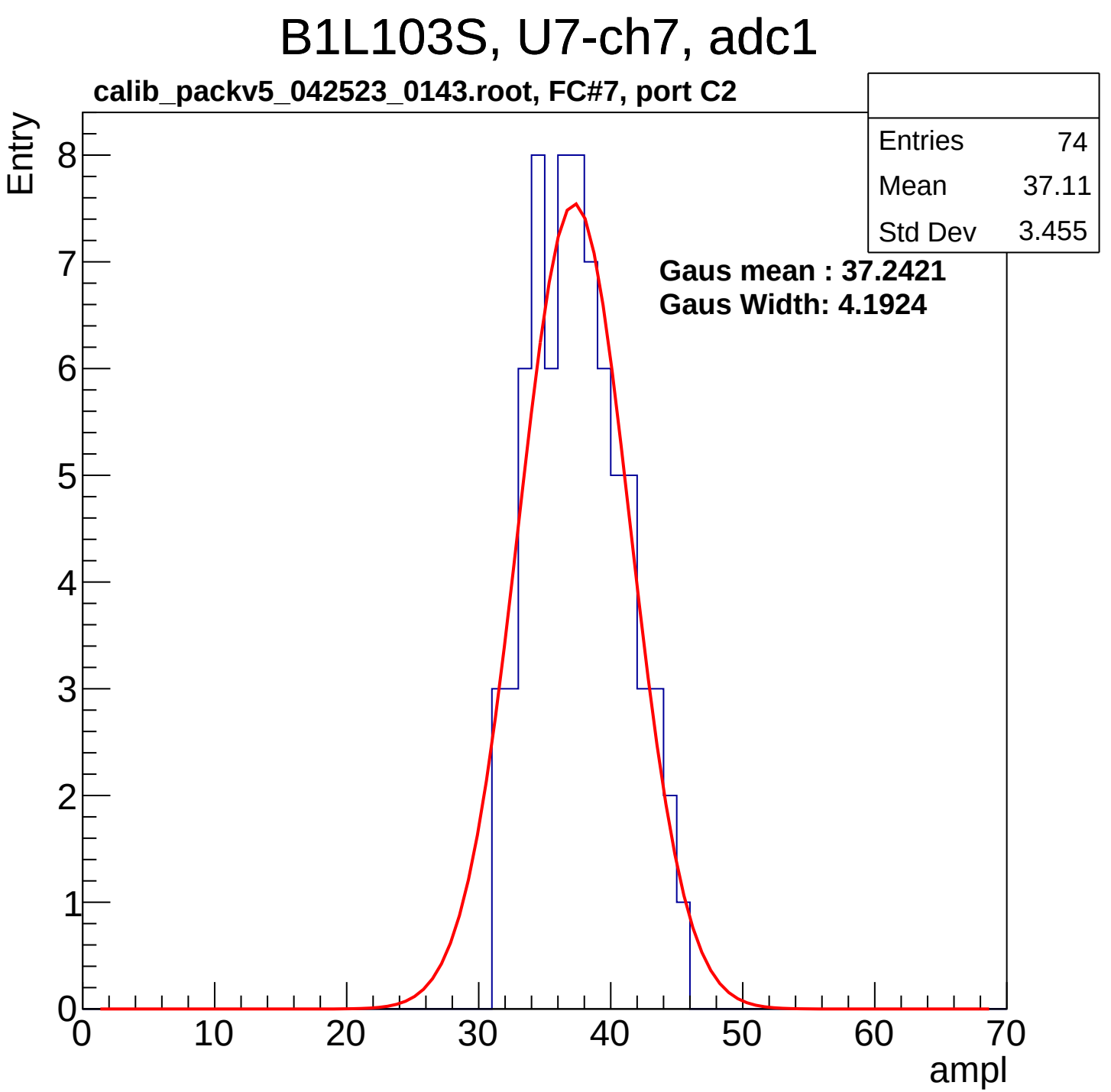
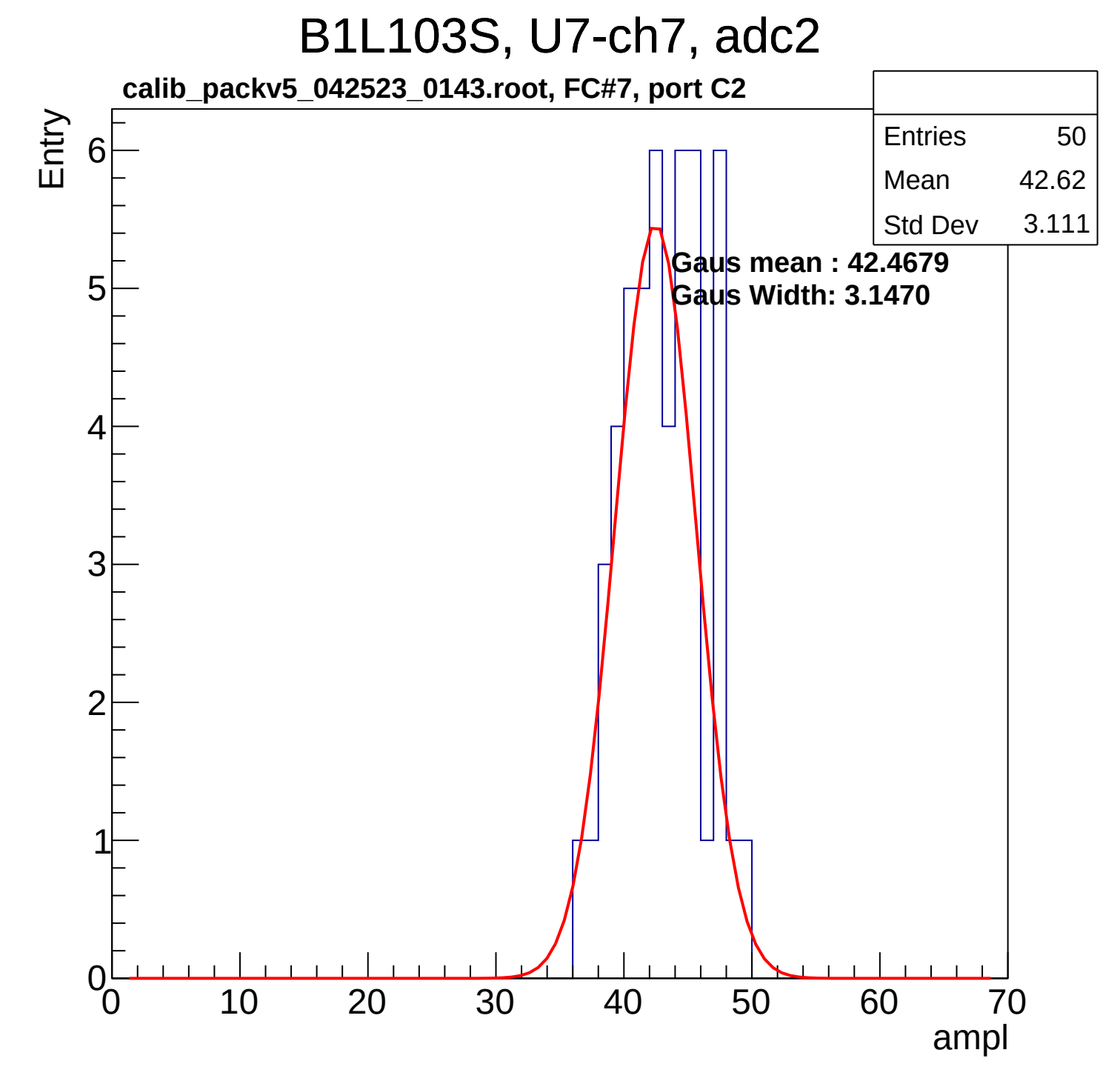
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch7, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 78
Mean 28.49
Std Dev 4.768
Gaus mean : 29.3181
Gaus Width: 3.5349
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch7, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 74
Mean 37.11
Std Dev 3.455
Gaus mean : 37.2421
Gaus Width: 4.1924
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch7, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 50
Mean 42.62
Std Dev 3.111
Gaus mean : 42.4679
Gaus Width: 3.1470
Entry
ampl
0
1
2
3
4
5
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0
10
20
30
40
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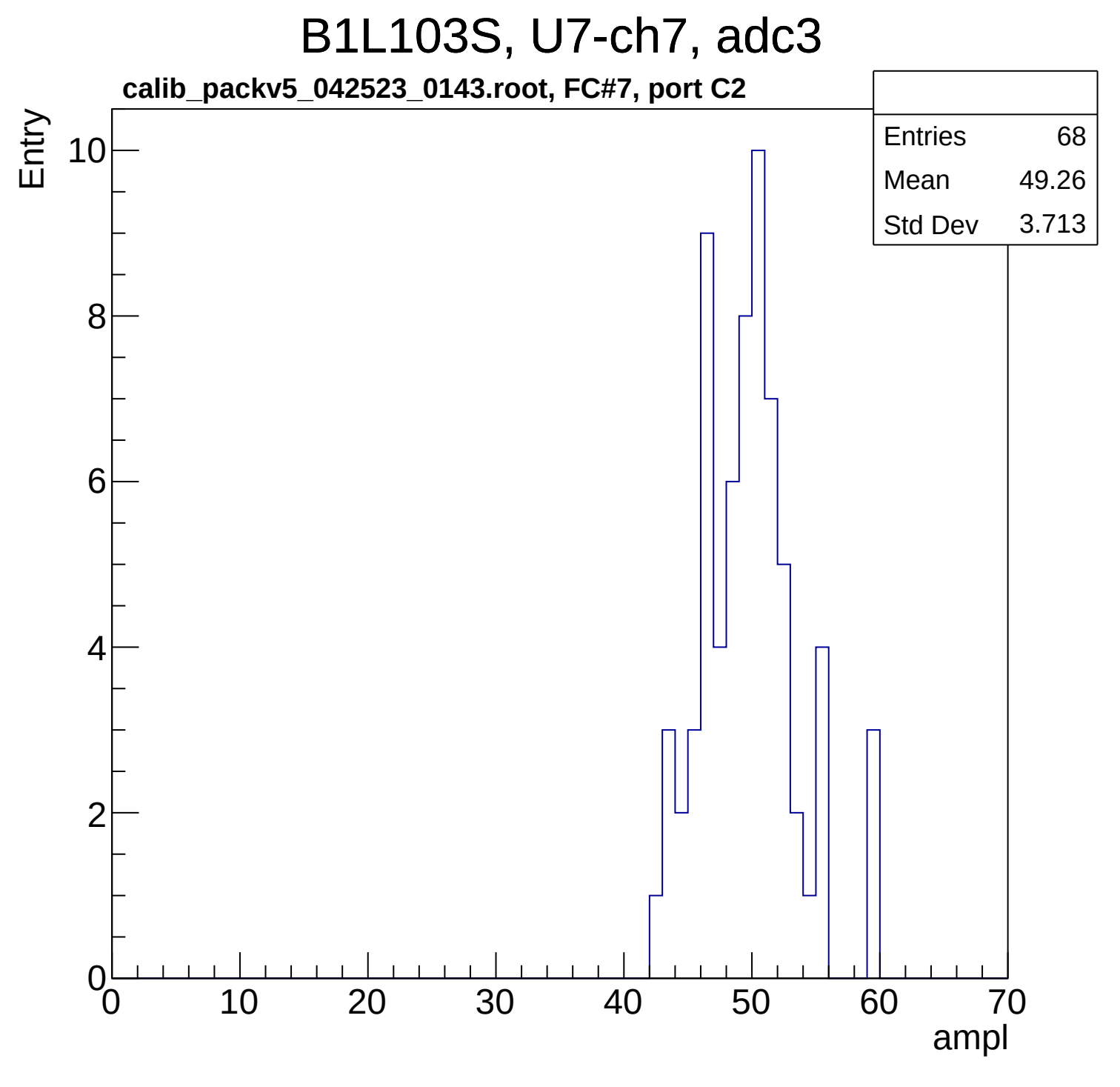
60
70


B1L103S, U7-ch7, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 49.26
Std Dev 3.713
Entry
ampl
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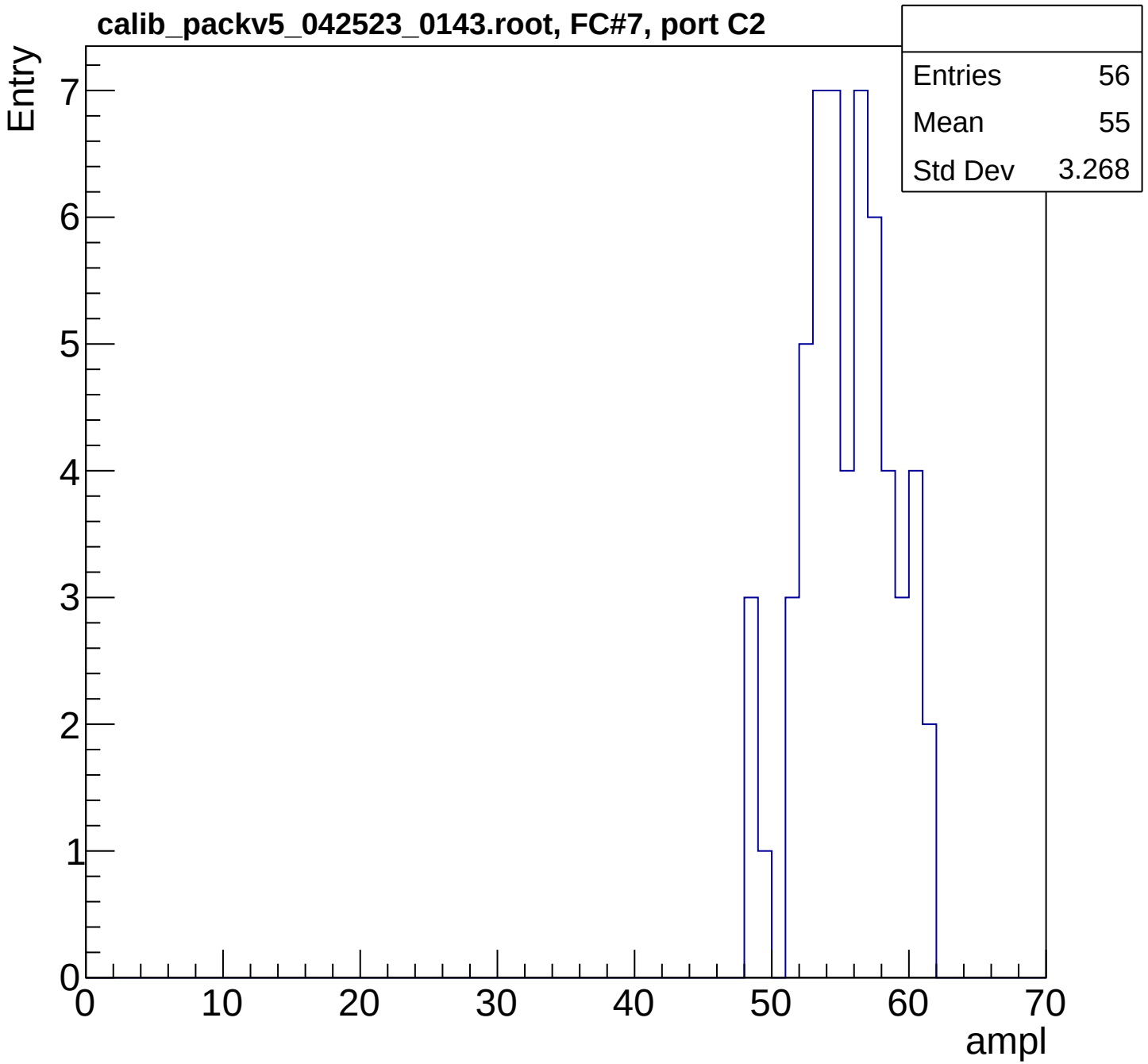
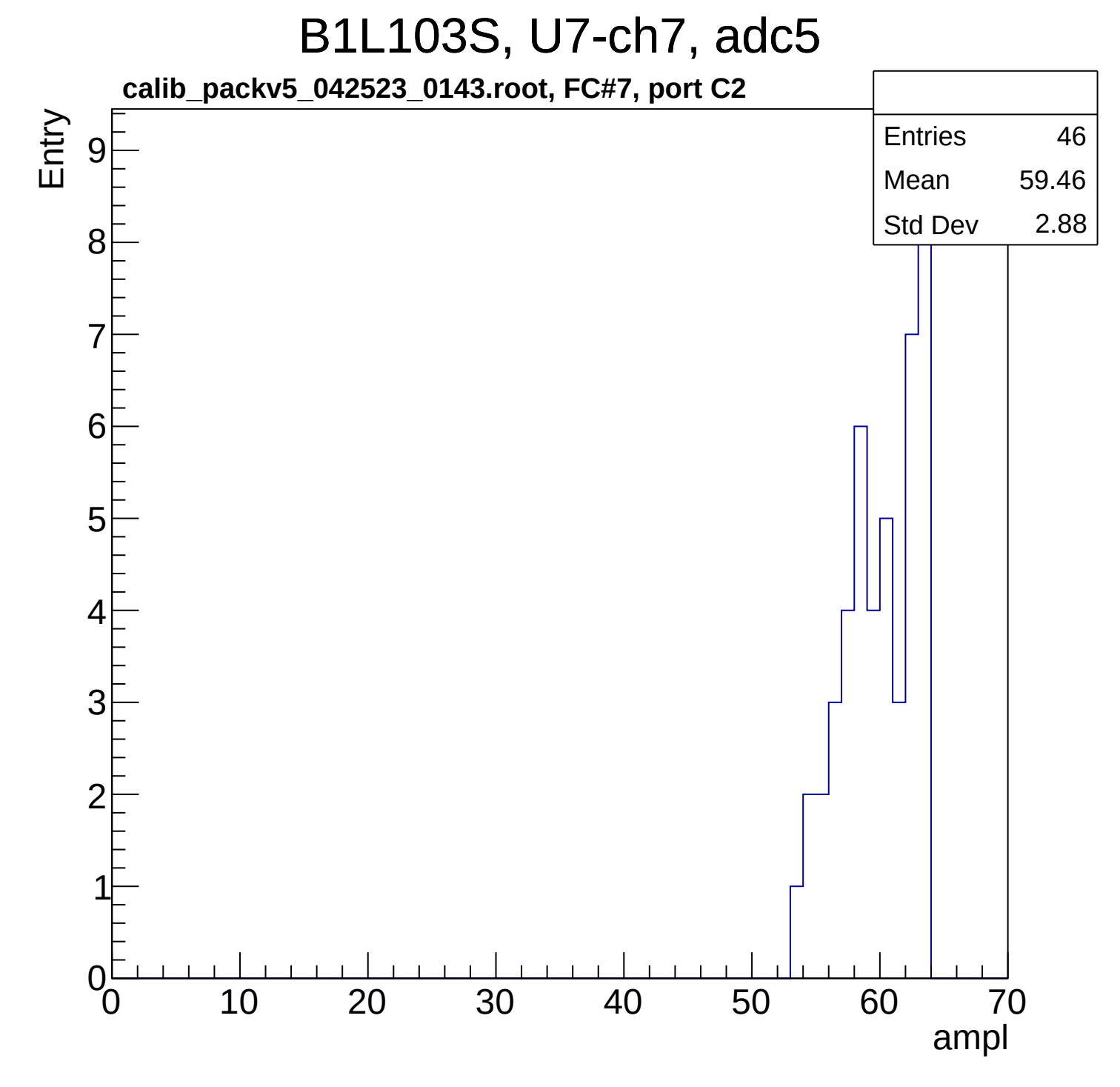
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch7, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 55
Std Dev 3.268
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch7, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 46
Mean 59.46
Std Dev 2.88
Entry
ampl
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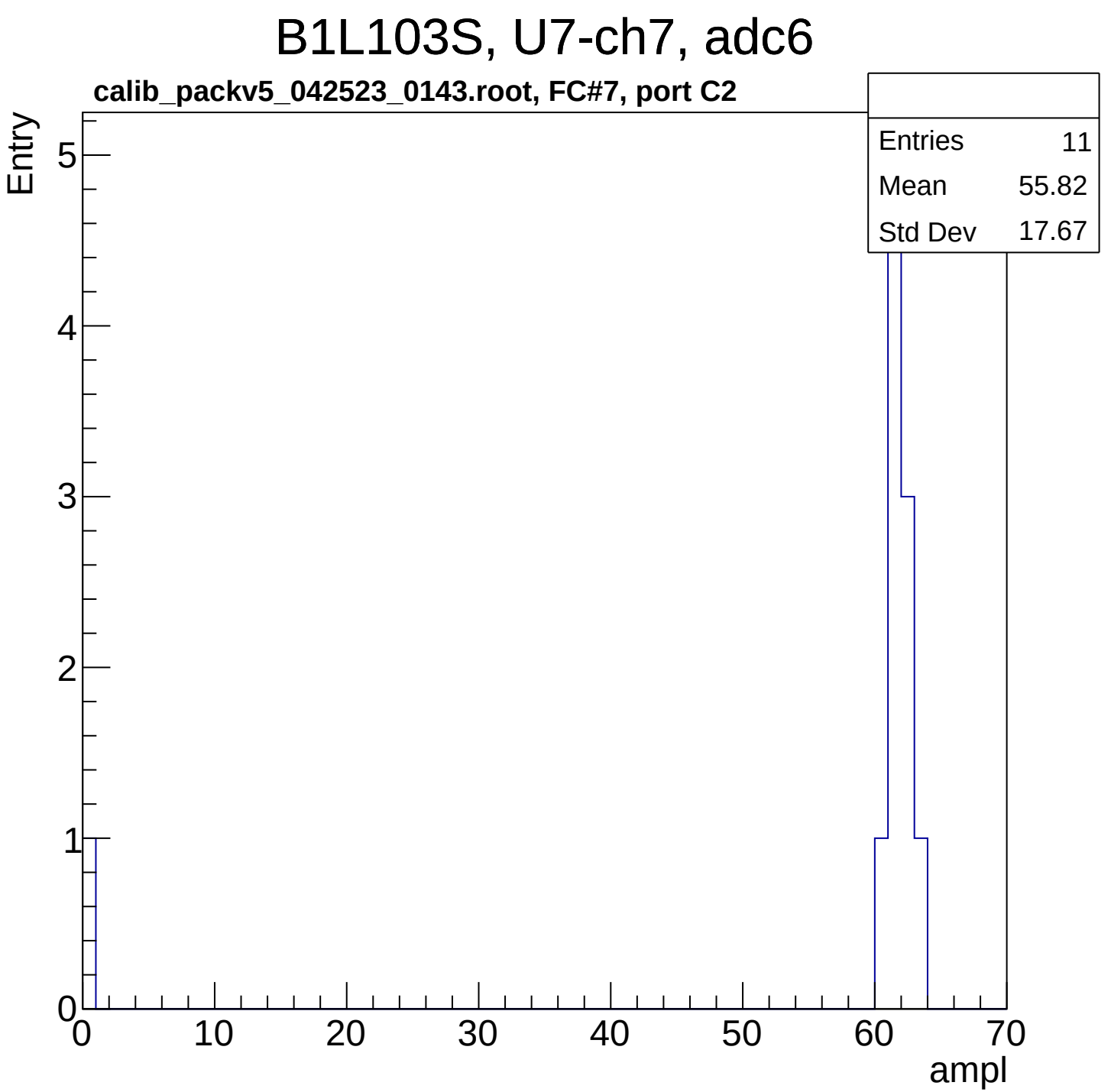
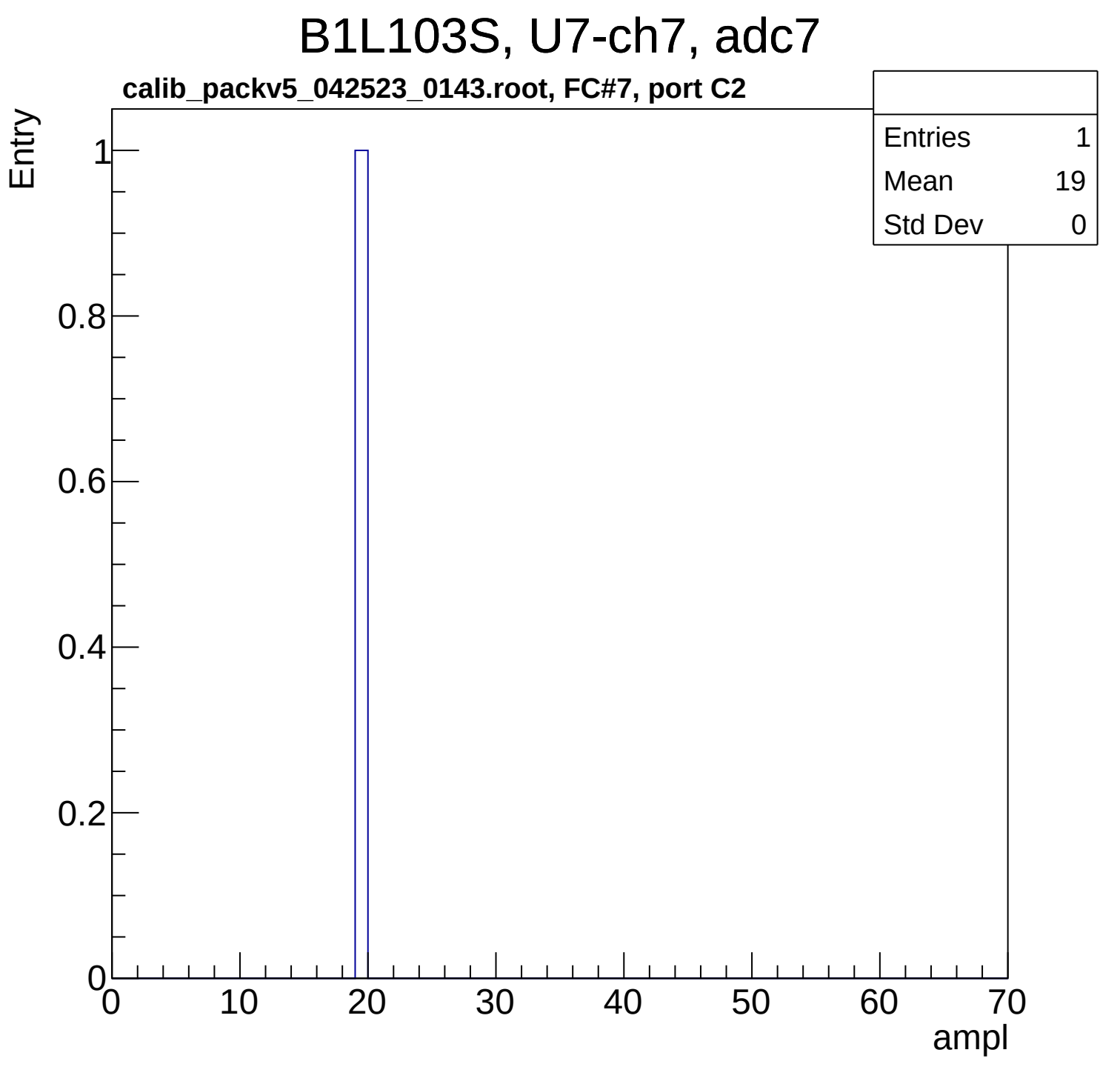
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch7, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 11
Mean 55.82
Std Dev 17.67
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch7, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 19
Std Dev 0
Entry
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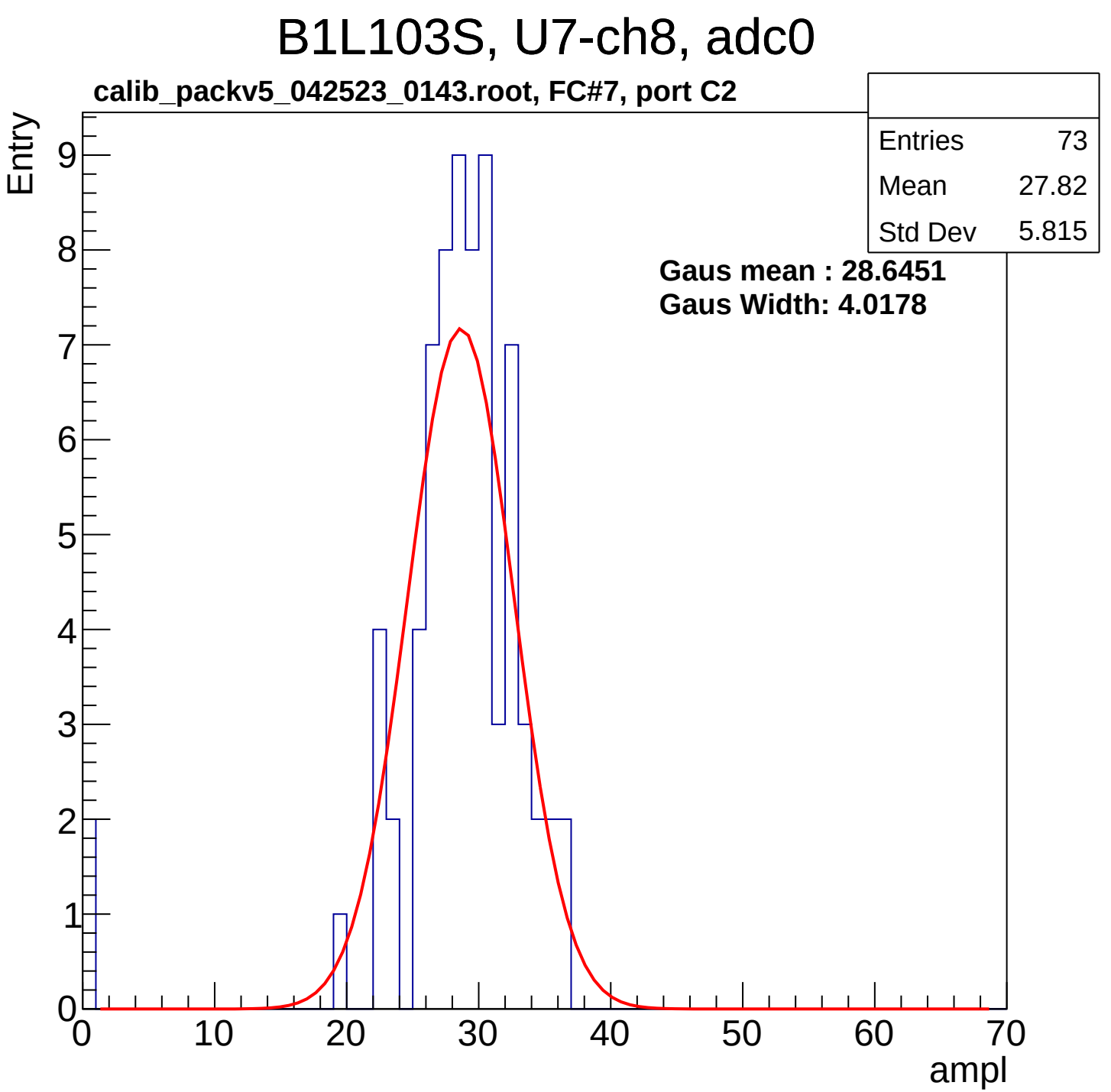
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch8, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 73
Mean 27.82
Std Dev 5.815
Gaus mean : 28.6451
Gaus Width: 4.0178
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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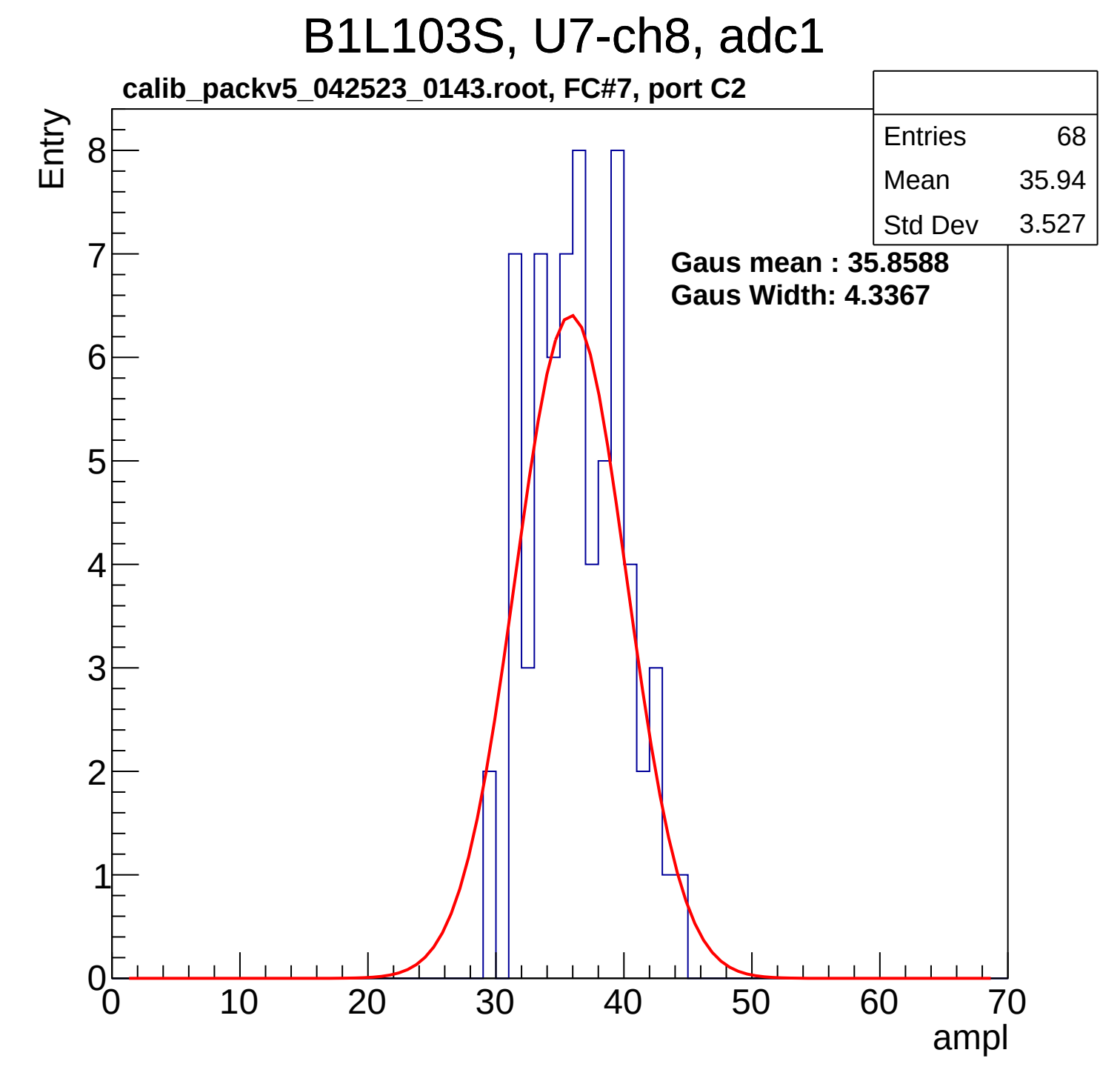
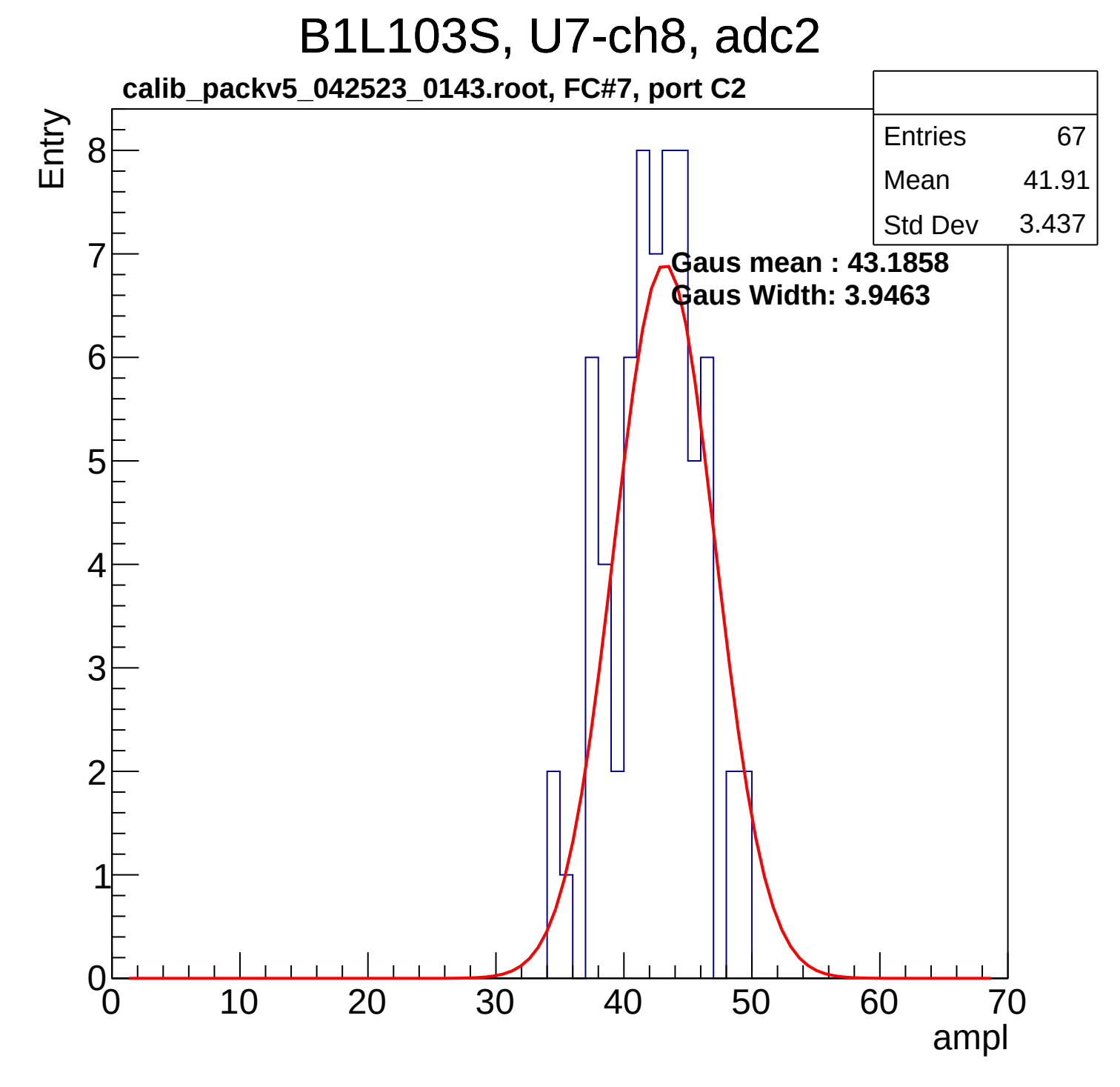
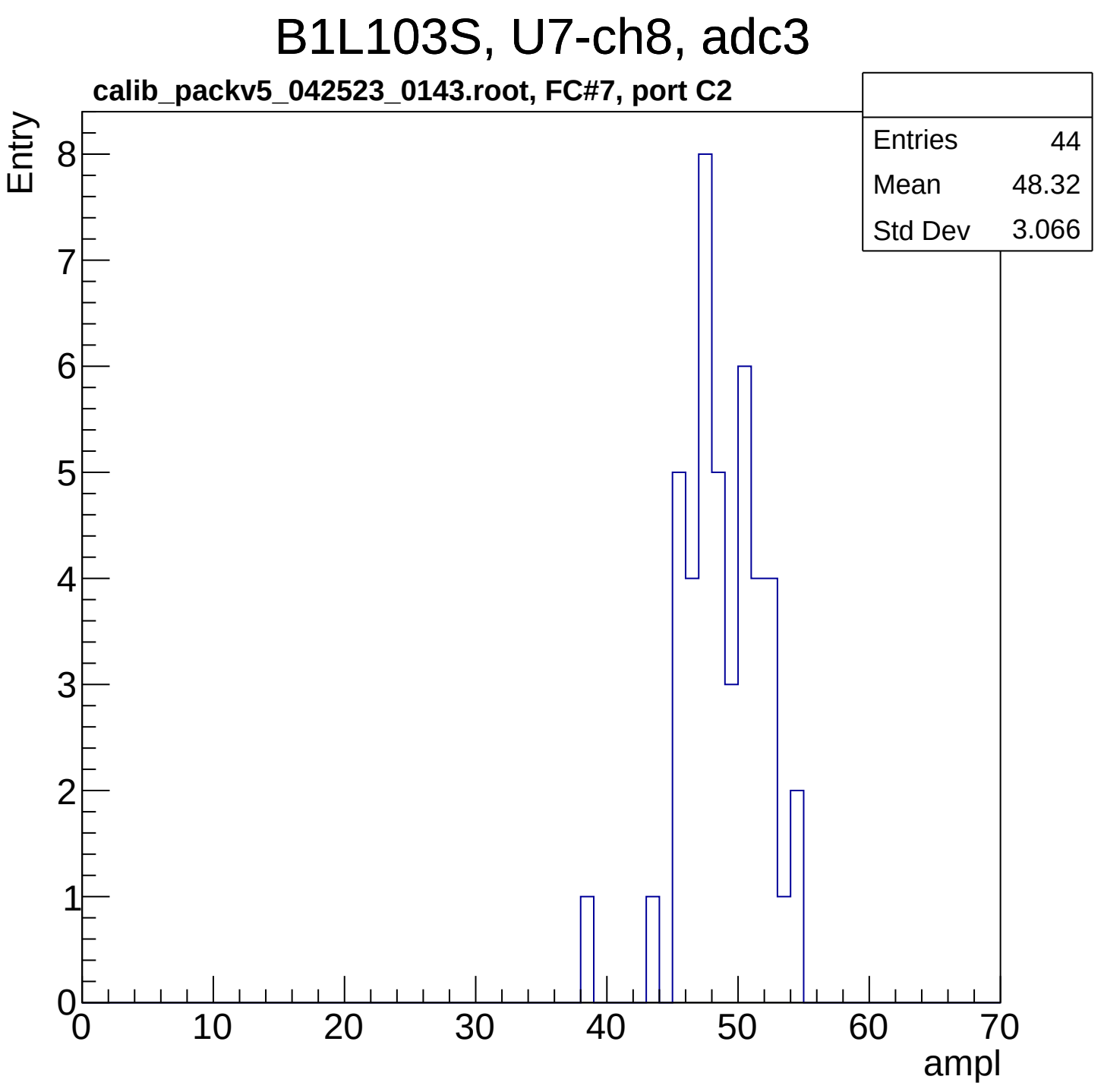
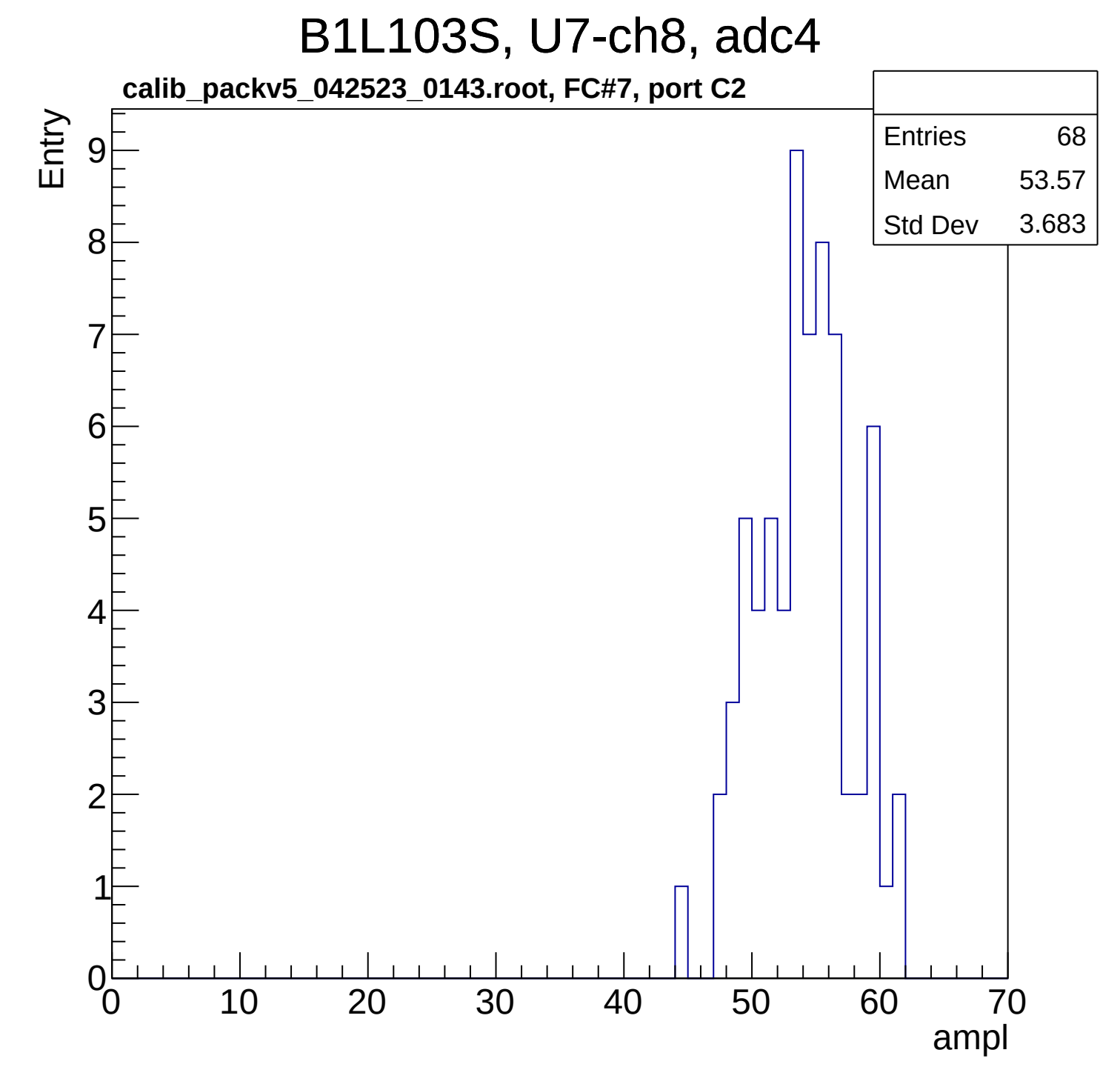
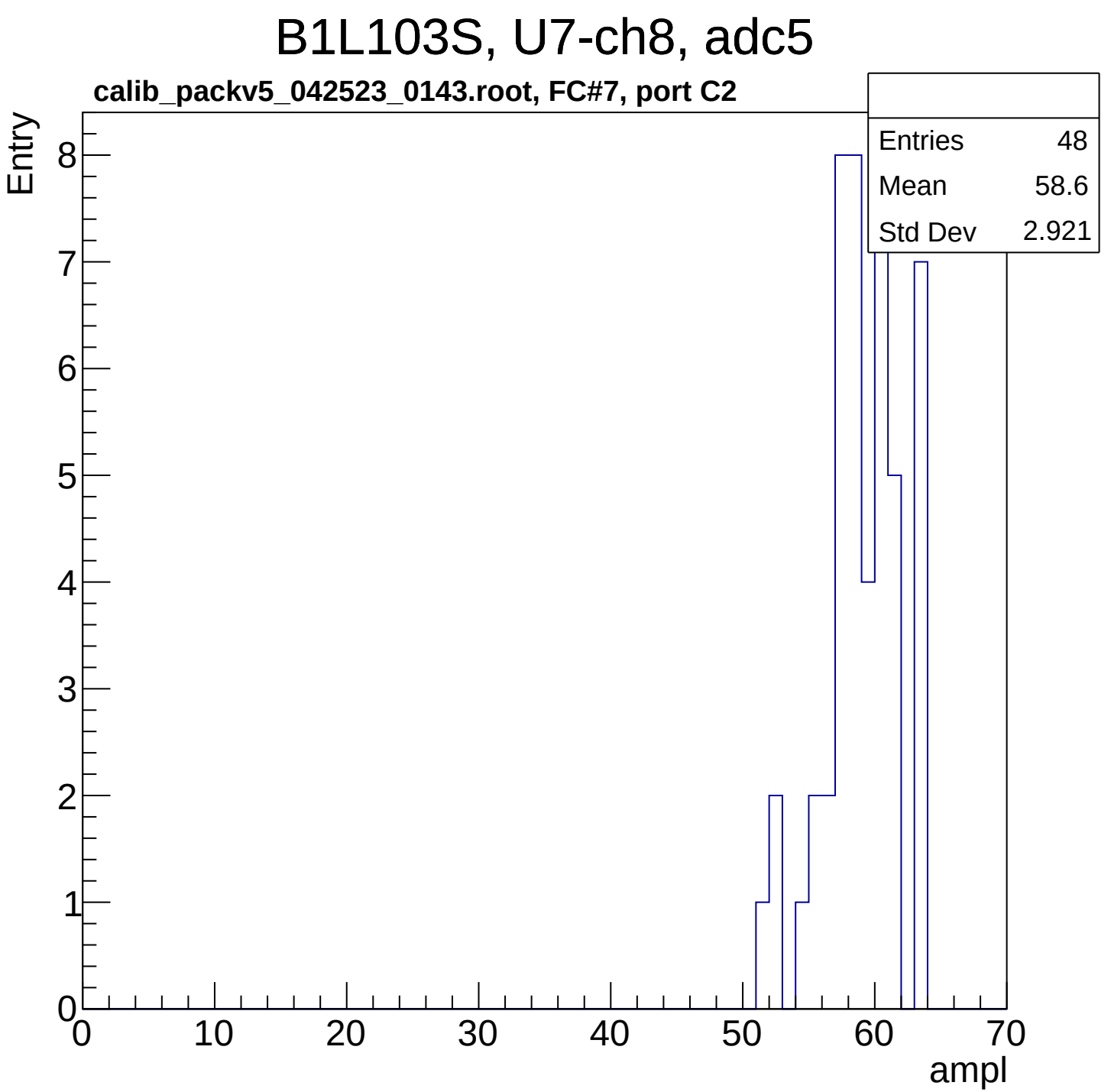
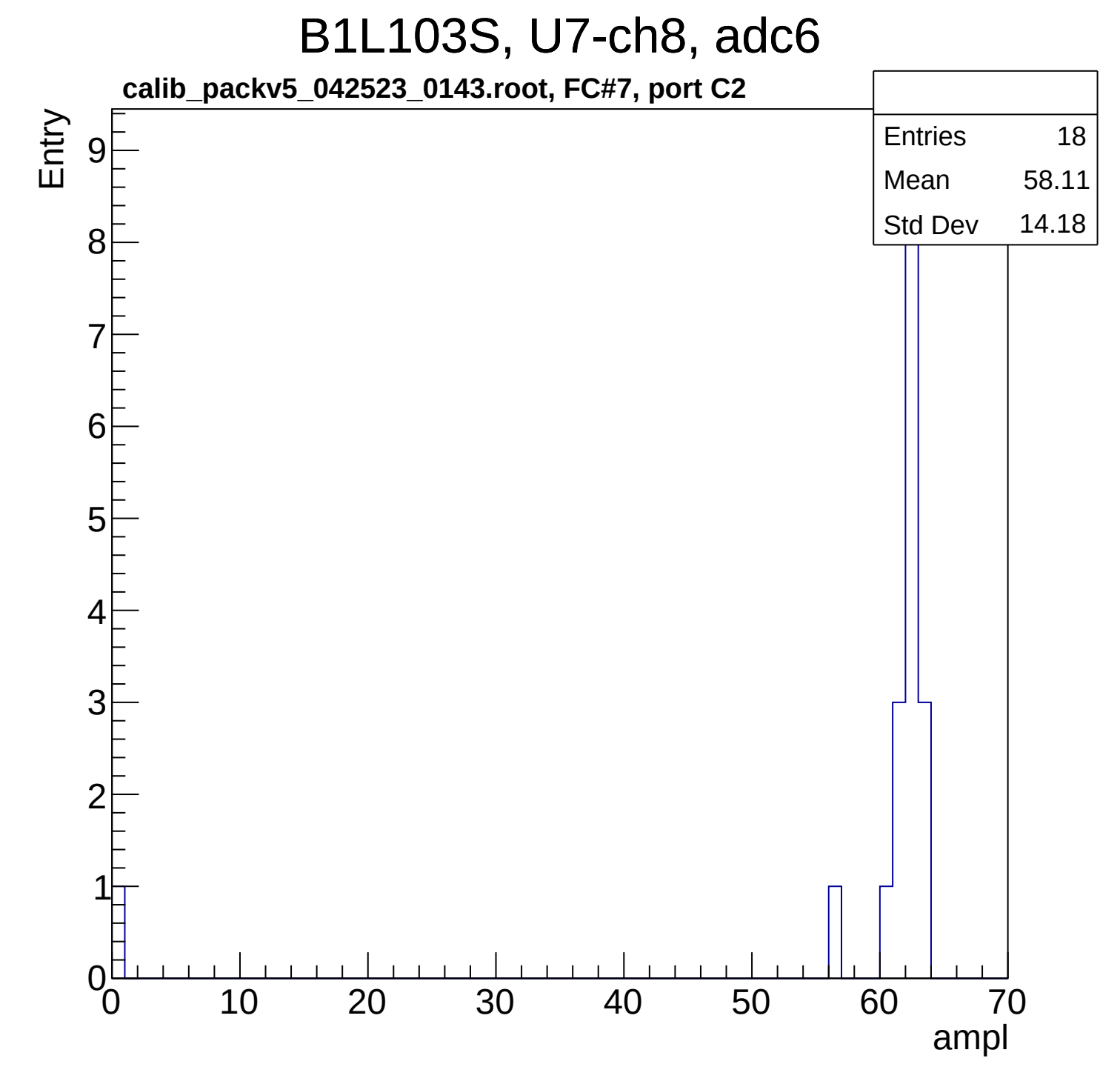

B1L103S, U7-ch8, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 35.94
Std Dev 3.527
Gaus mean : 35.8588
Gaus Width: 4.3367
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch8, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 41.91
Std Dev 3.437
Gaus mean : 43.1858
Gaus Width: 3.9463
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch8, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 44
Mean 48.32
Std Dev 3.066
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch8, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 53.57
Std Dev 3.683
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch8, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 48
Mean 58.6
Std Dev 2.921
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch8, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 18
Mean 58.11
Std Dev 14.18
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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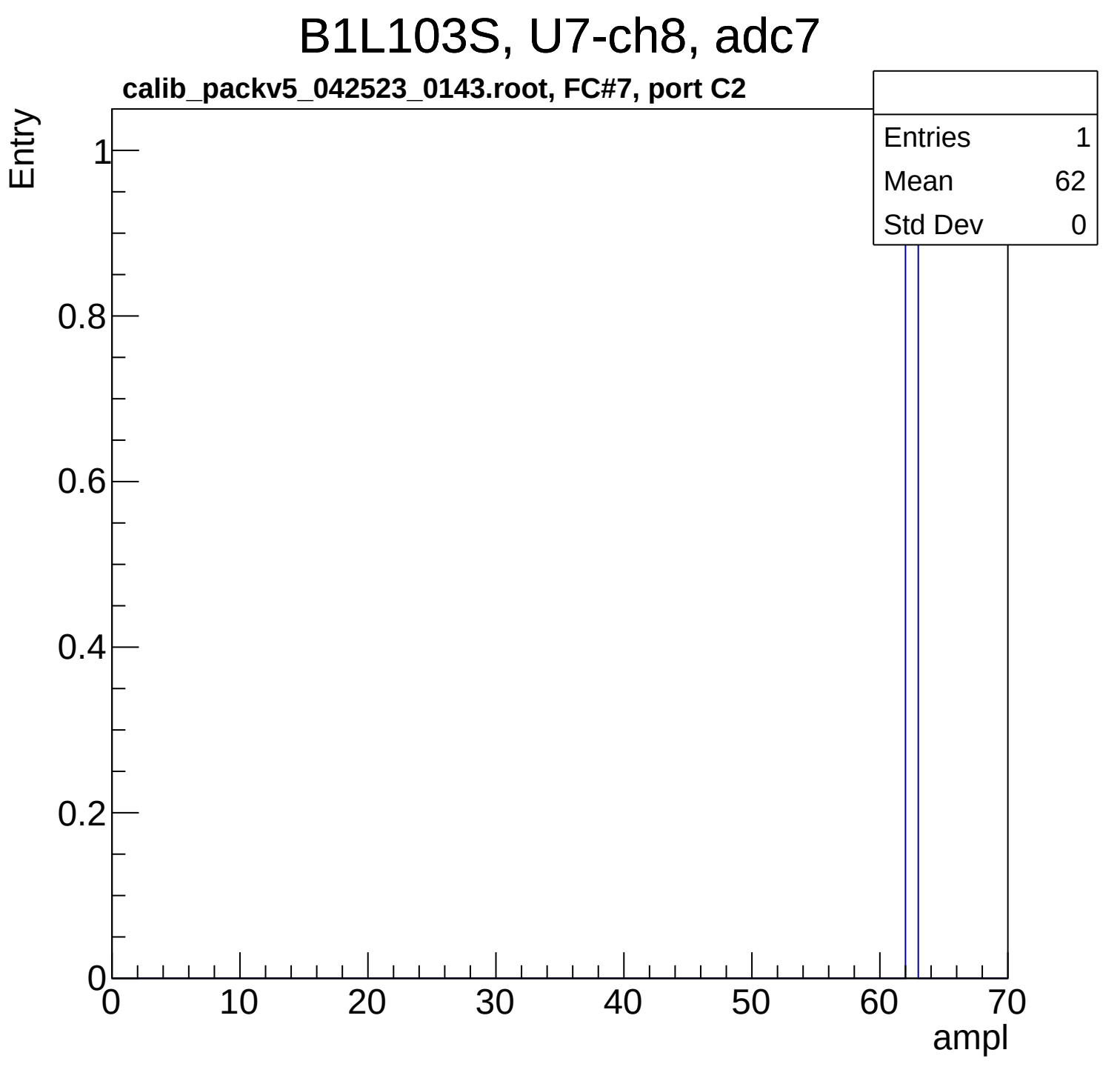
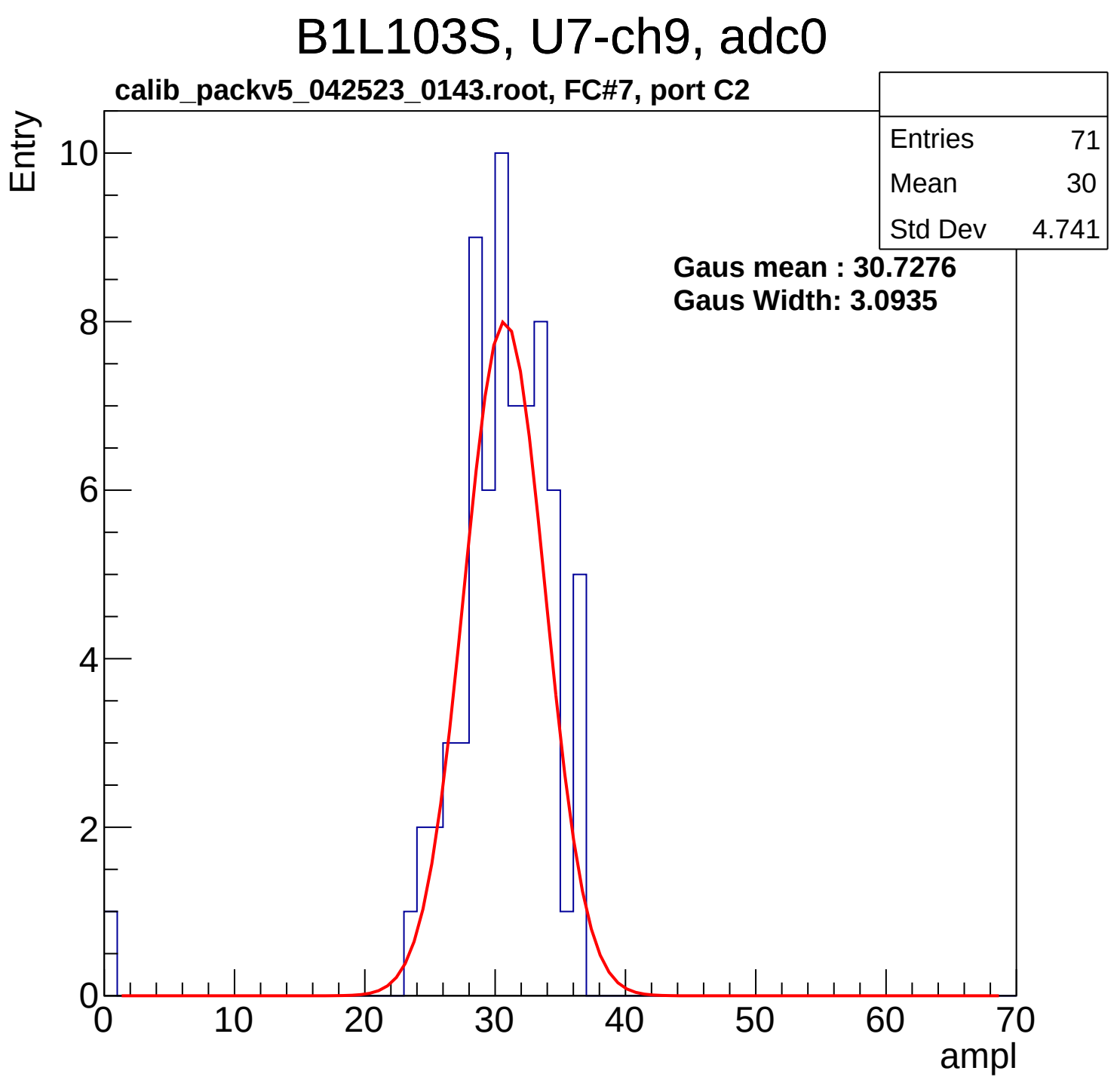
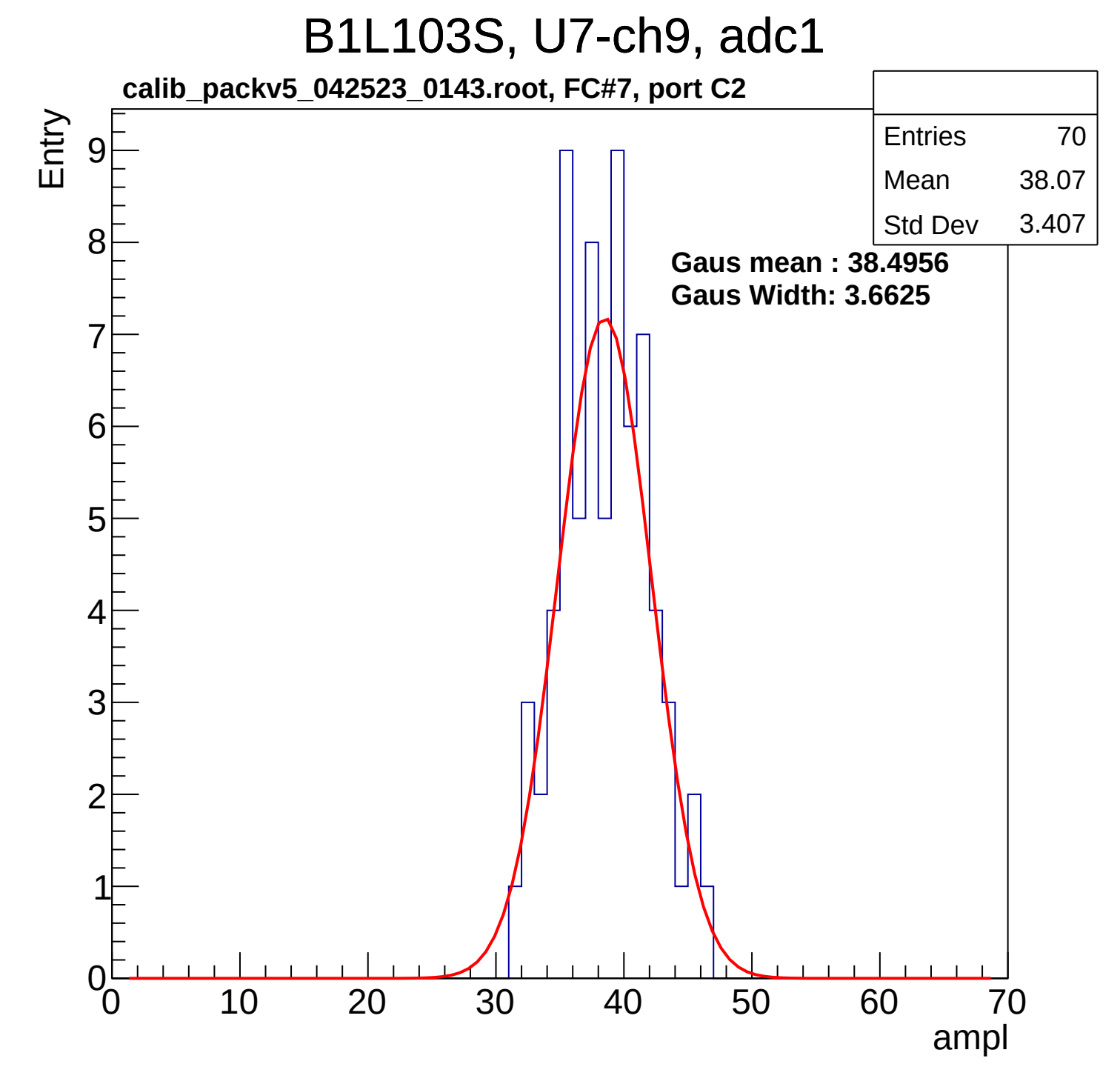
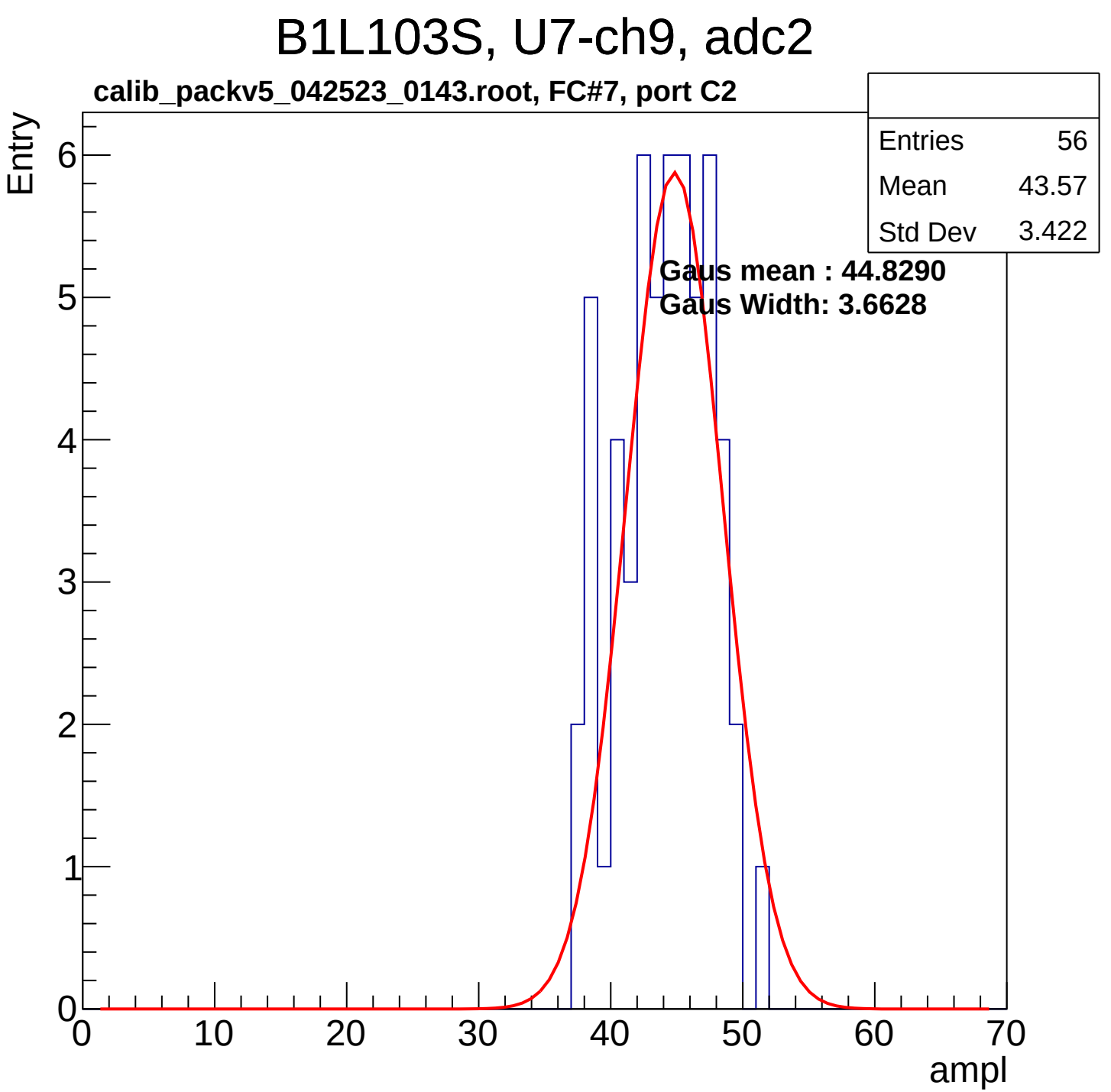
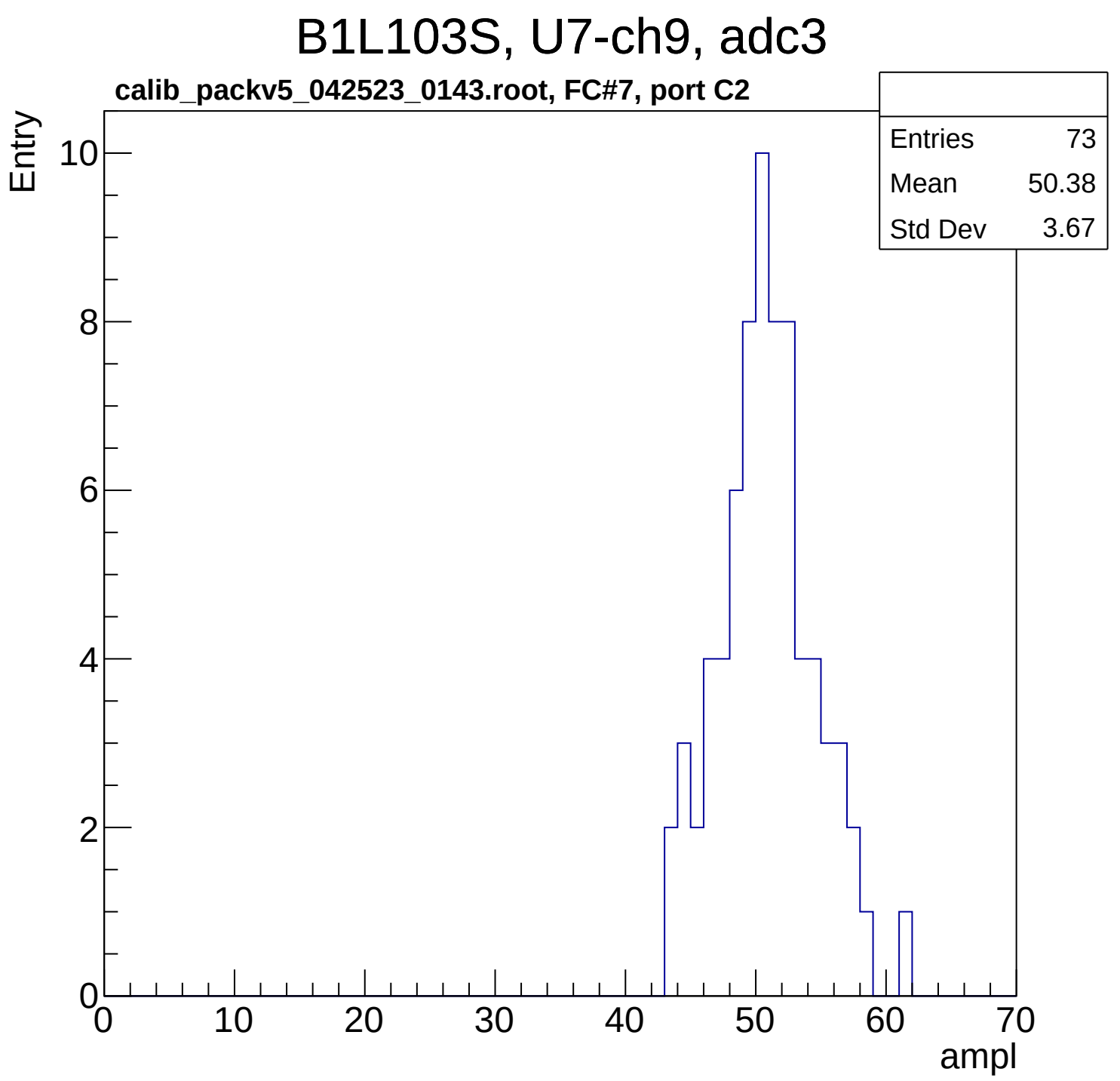
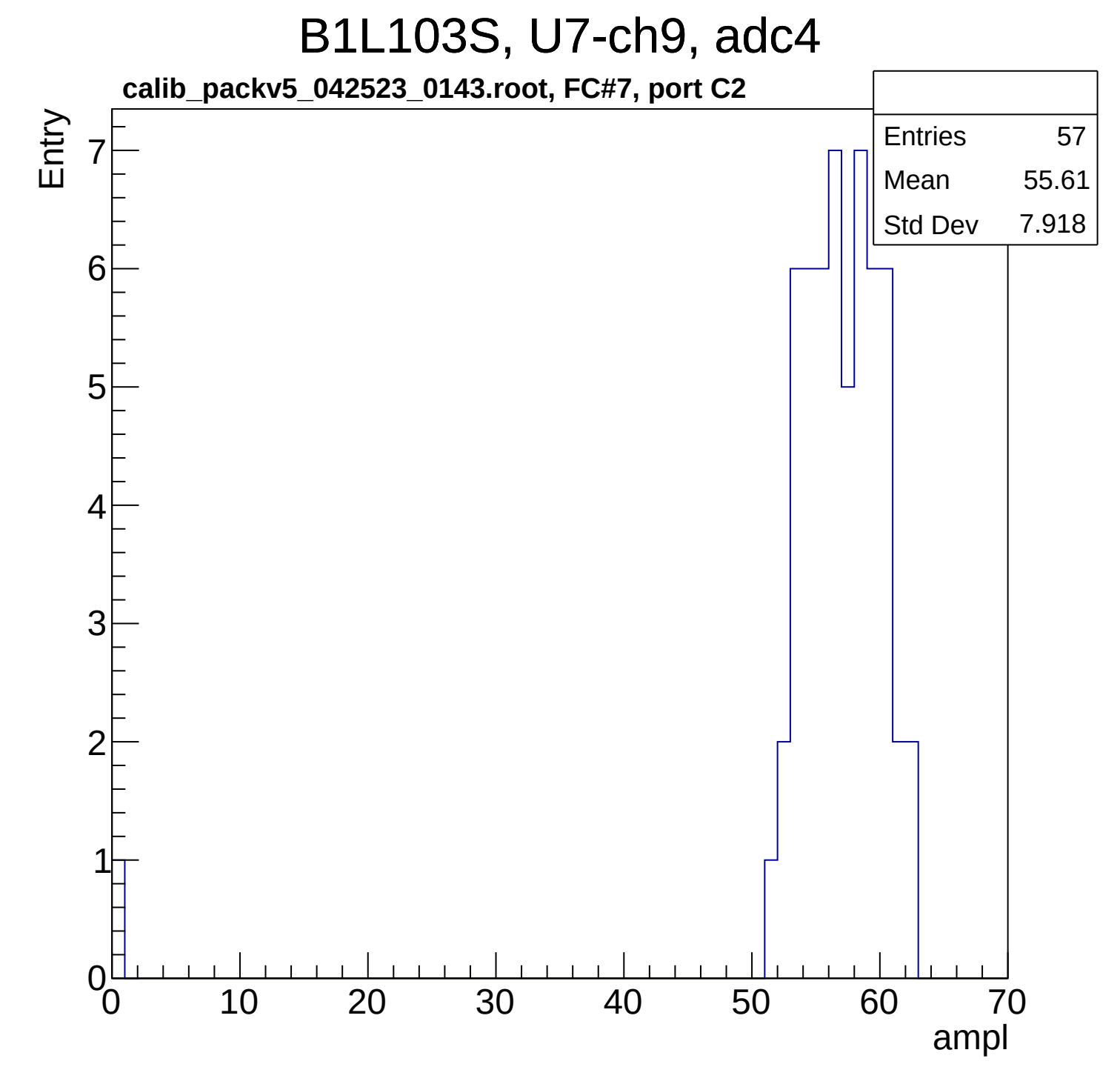

B1L103S, U7-ch8, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 62
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

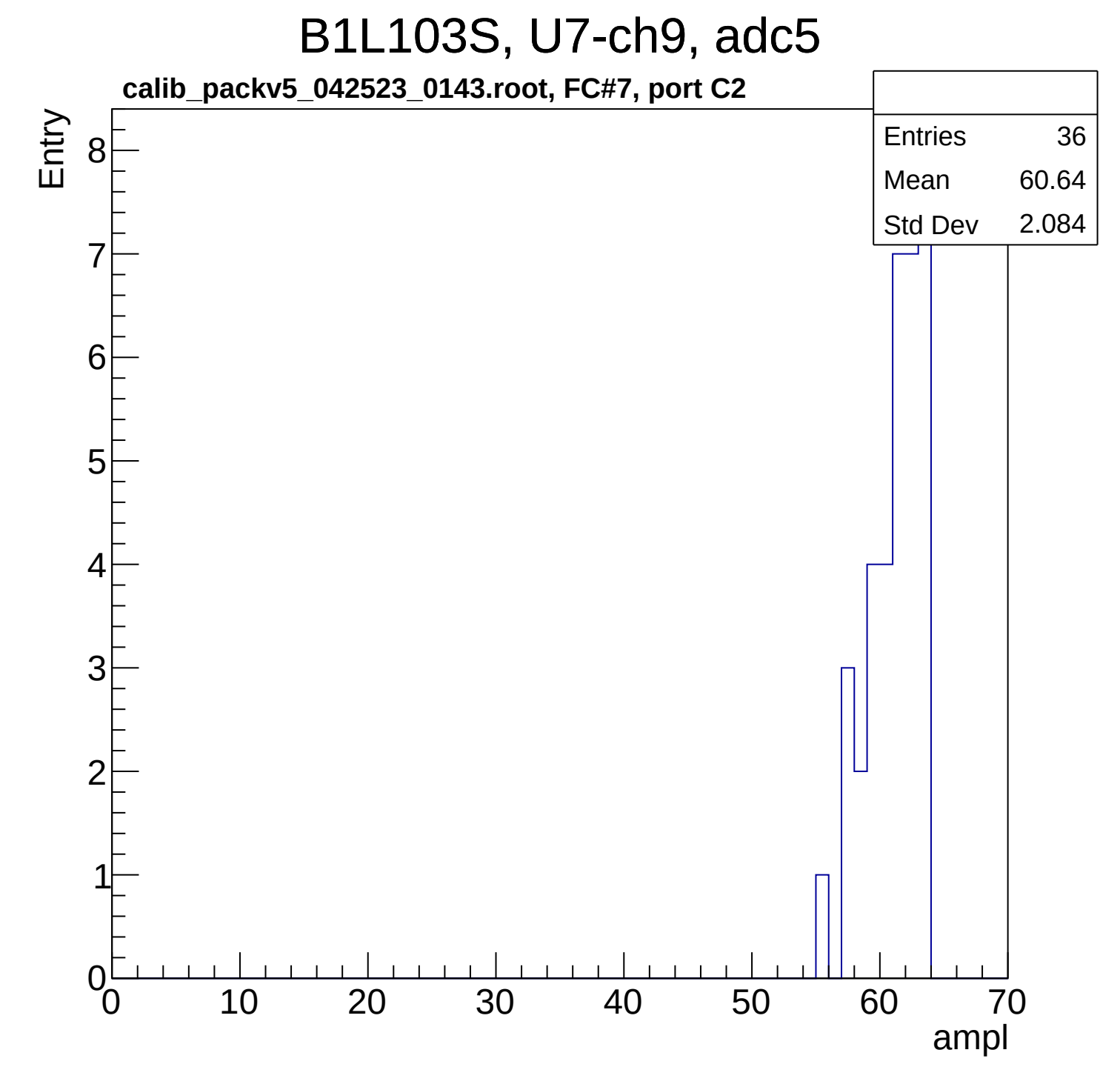

B1L103S, U7-ch9, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 71
Mean 30
Std Dev 4.741
Gaus mean : 30.7276
Gaus Width: 3.0935
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

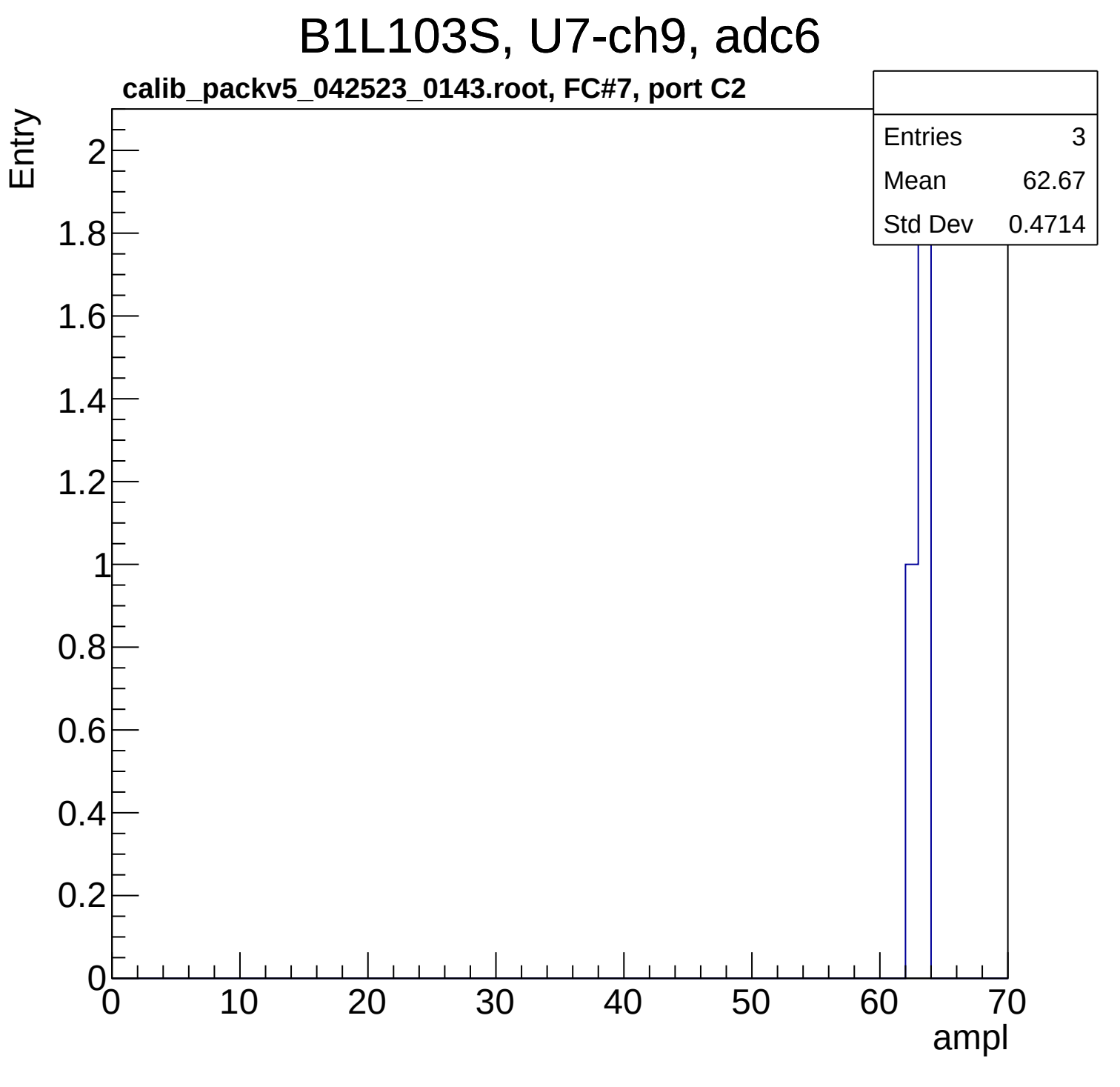

B1L103S, U7-ch9, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 38.07
Std Dev 3.407
Gaus mean : 38.4956
Gaus Width: 3.6625
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

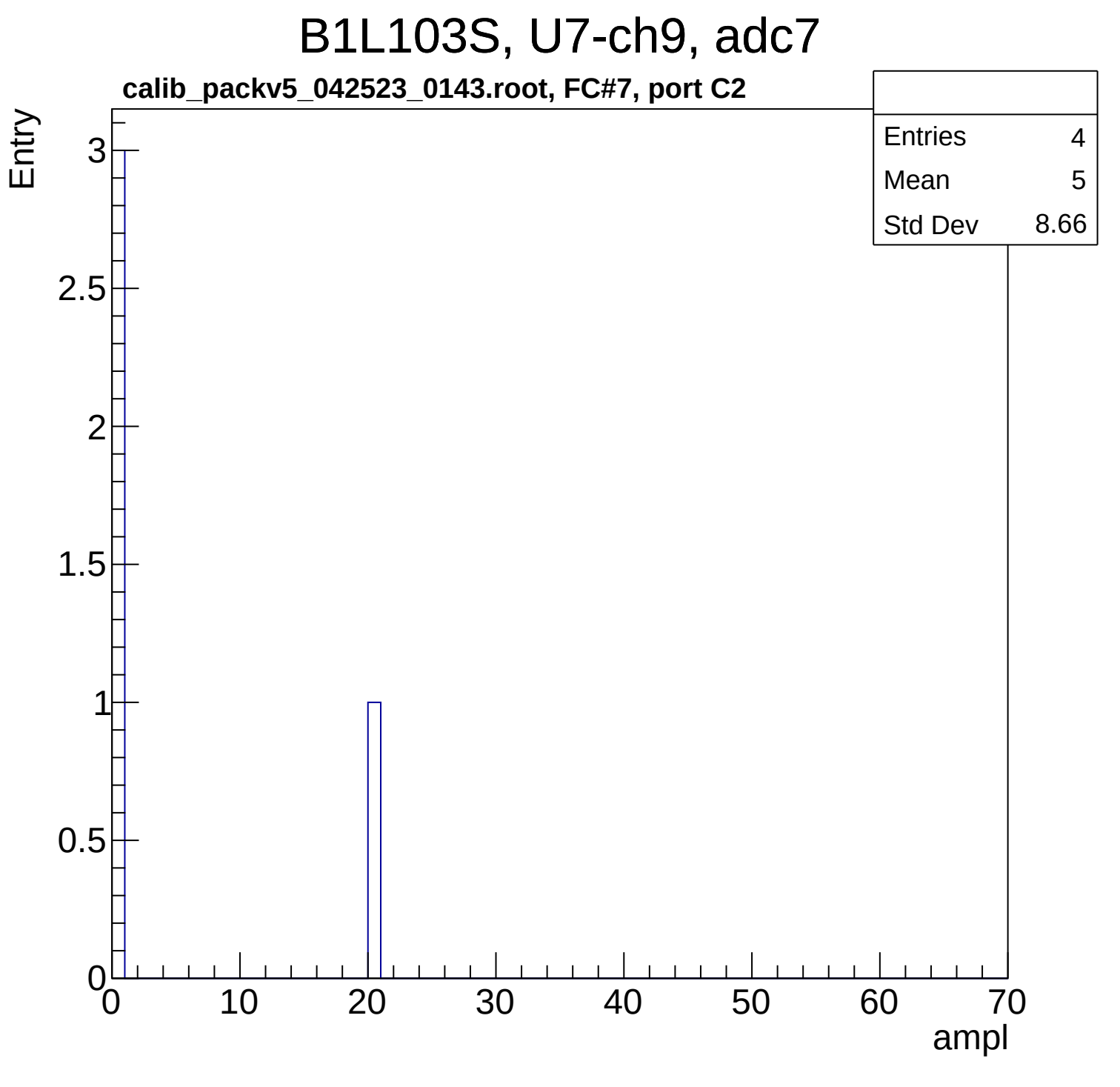

B1L103S, U7-ch9, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 43.57
Std Dev 3.422
Gaus mean : 44.8290
Gaus Width: 3.6628
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U7-ch9, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 73
Mean 50.38
Std Dev 3.67
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch9, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 55.61
Std Dev 7.918
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch9, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 36
Mean 60.64
Std Dev 2.084
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch9, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 62.67
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U7-ch9, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 4
Mean 5
Std Dev 8.66
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
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40
50
60
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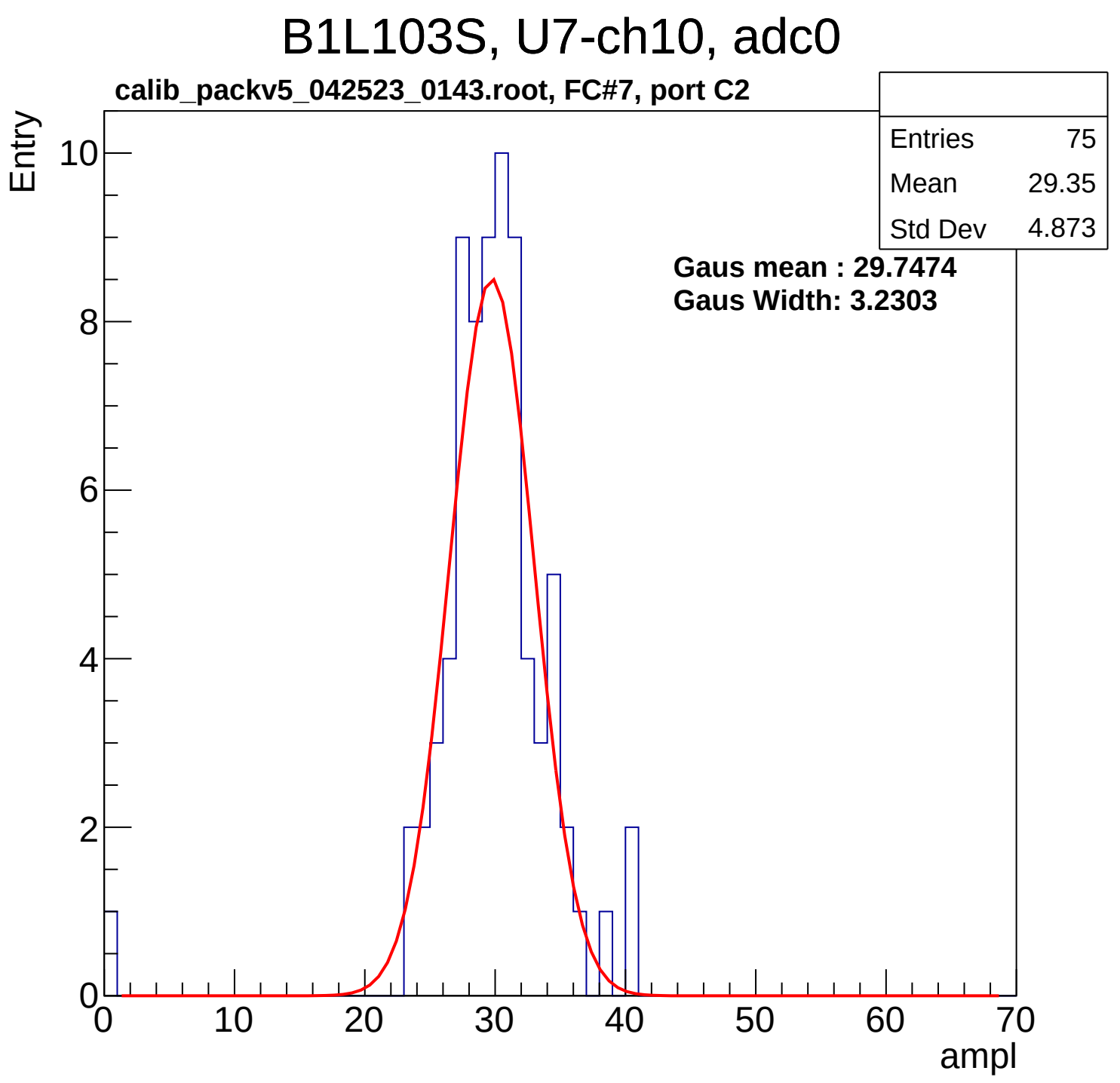
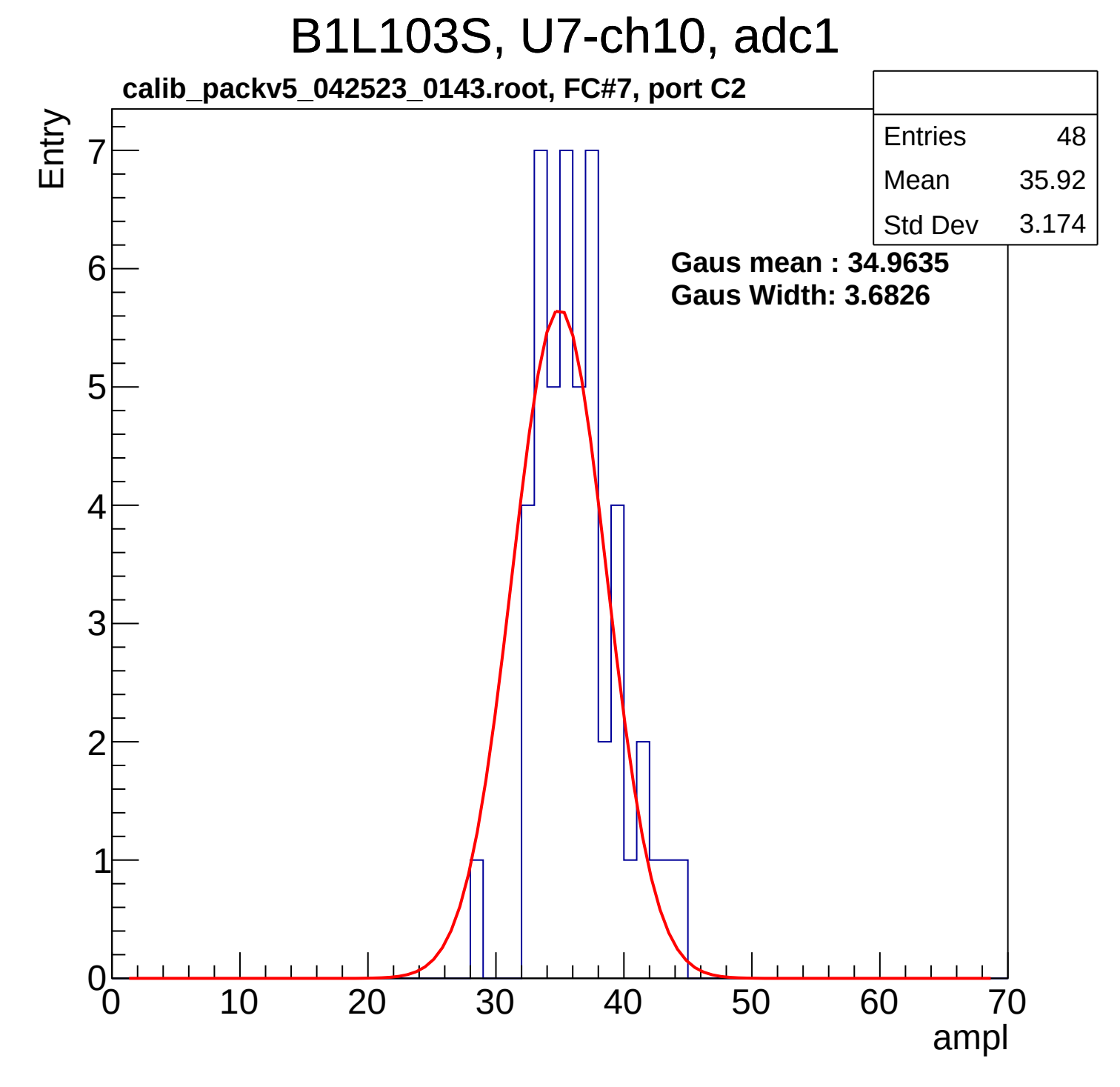
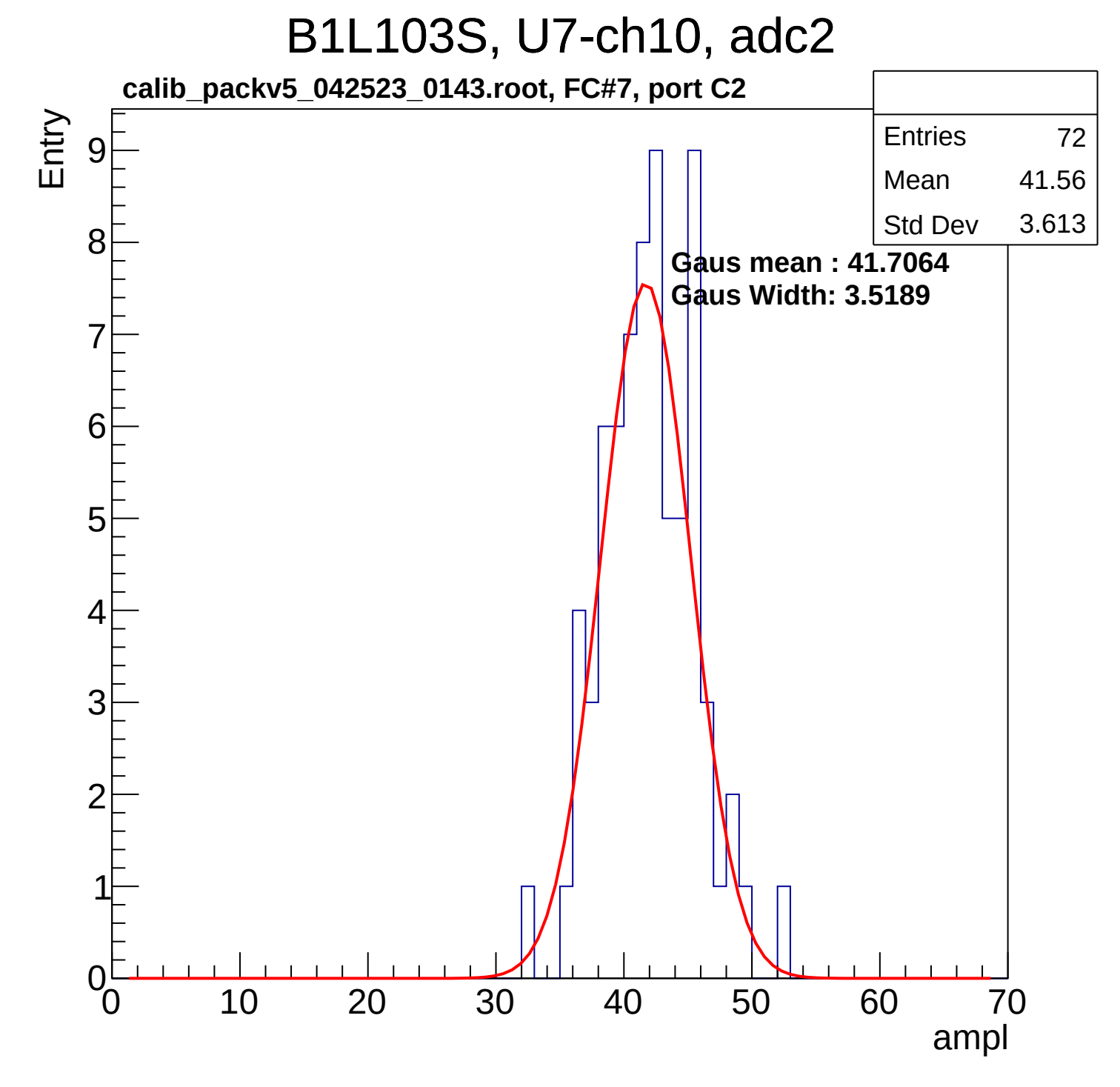

B1L103S, U7-ch10, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 75
Mean 29.35
Std Dev 4.873
Gaus mean : 29.7474
Gaus Width: 3.2303
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch10, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 48
Mean 35.92
Std Dev 3.174
Gaus mean : 34.9635
Gaus Width: 3.6826
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch10, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 72
Mean 41.56
Std Dev 3.613
Gaus mean : 41.7064
Gaus Width: 3.5189
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
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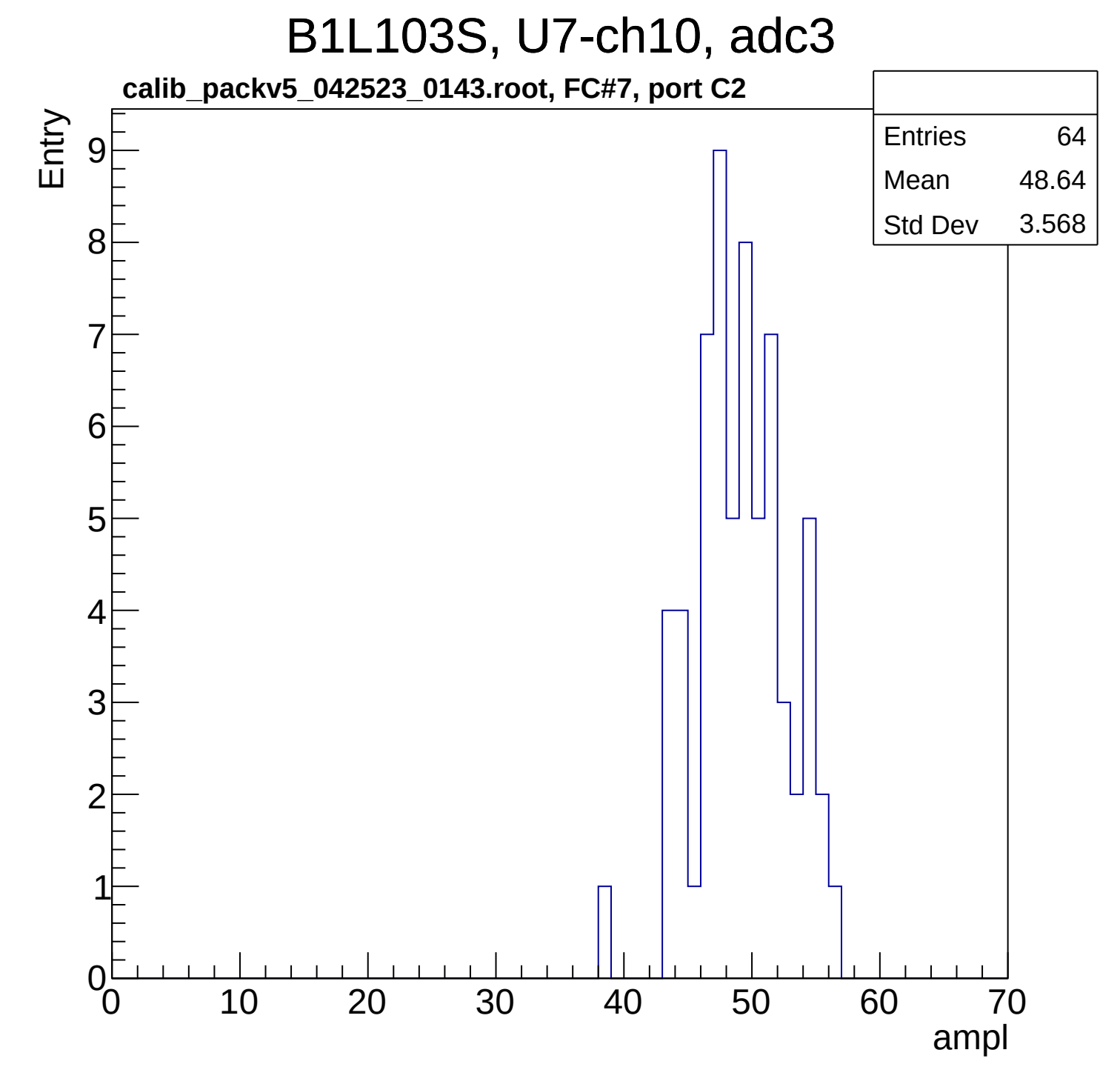
60
70


B1L103S, U7-ch10, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 48.64
Std Dev 3.568
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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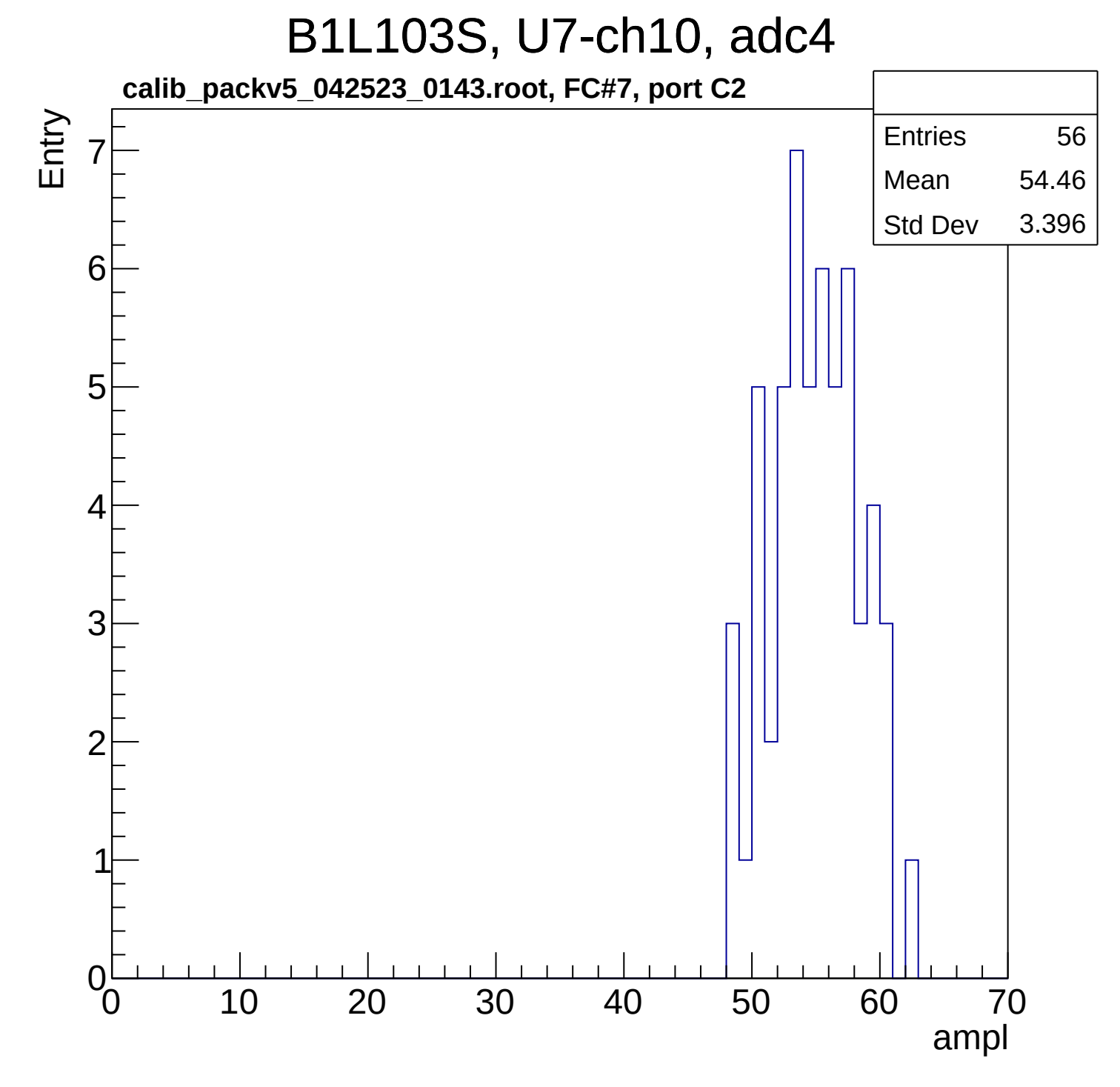
B1L103S, U7-ch10, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 54.46
Std Dev 3.396
Entry
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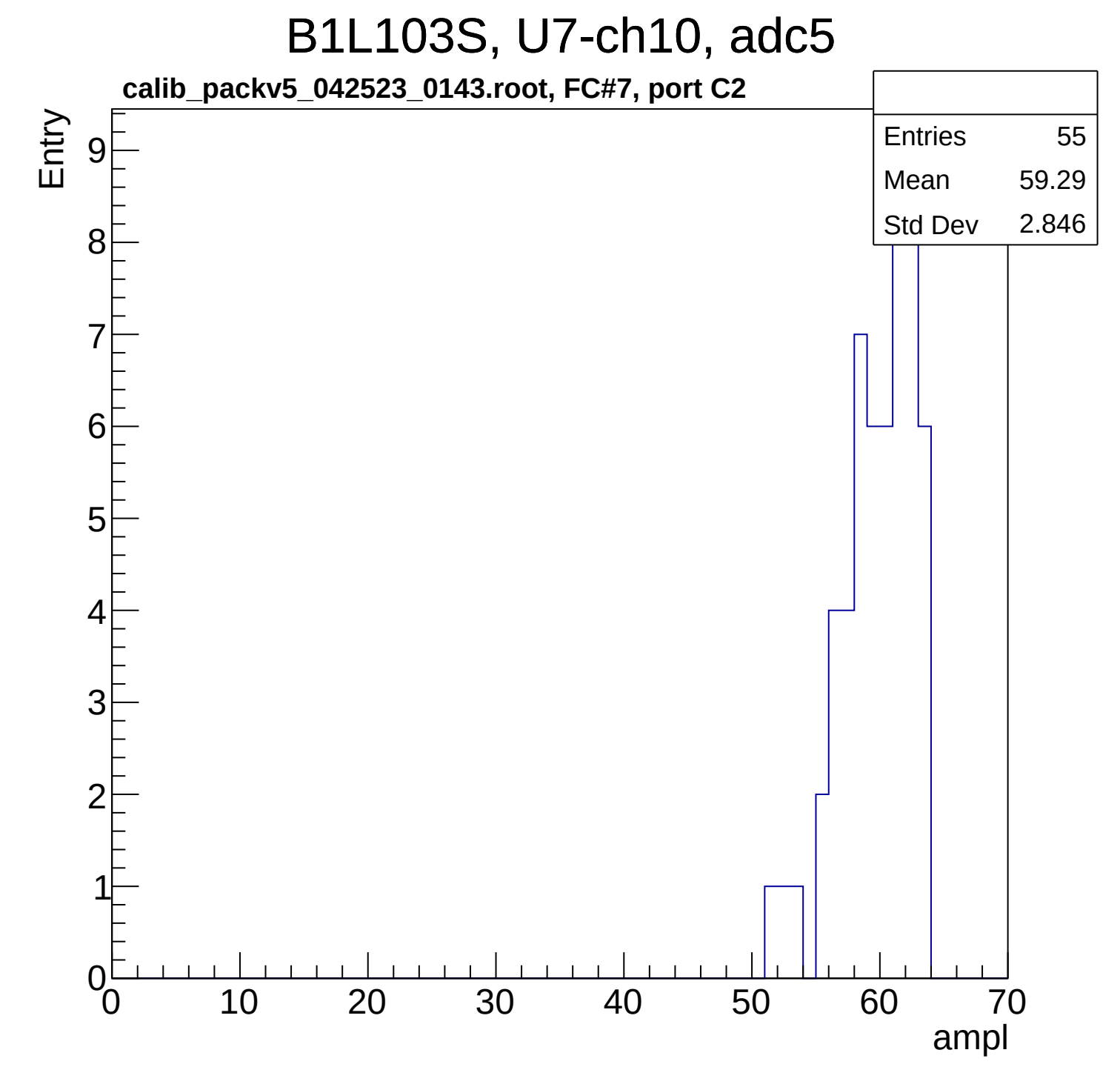
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch10, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 59.29
Std Dev 2.846
Entry
ampl
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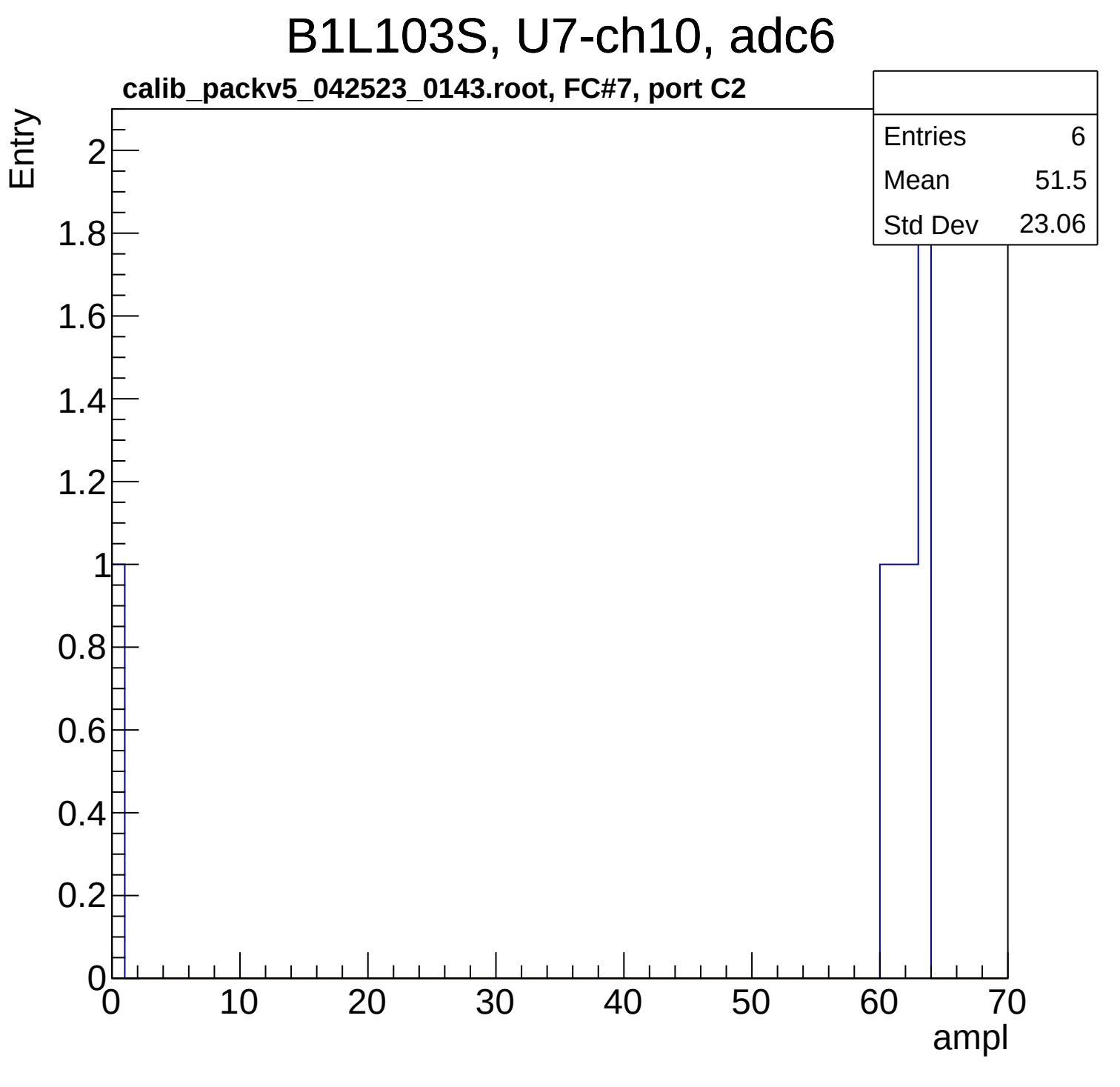
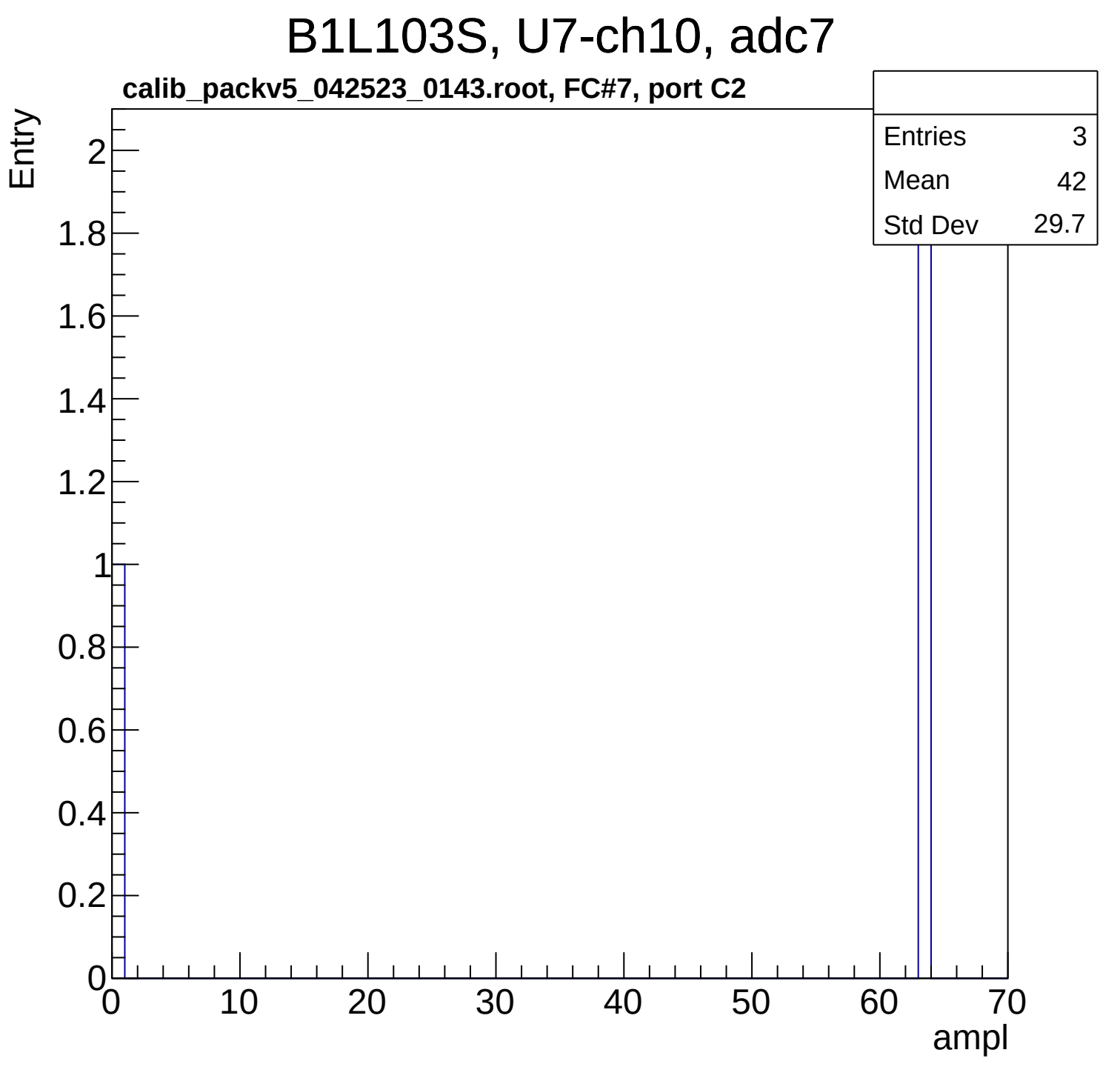
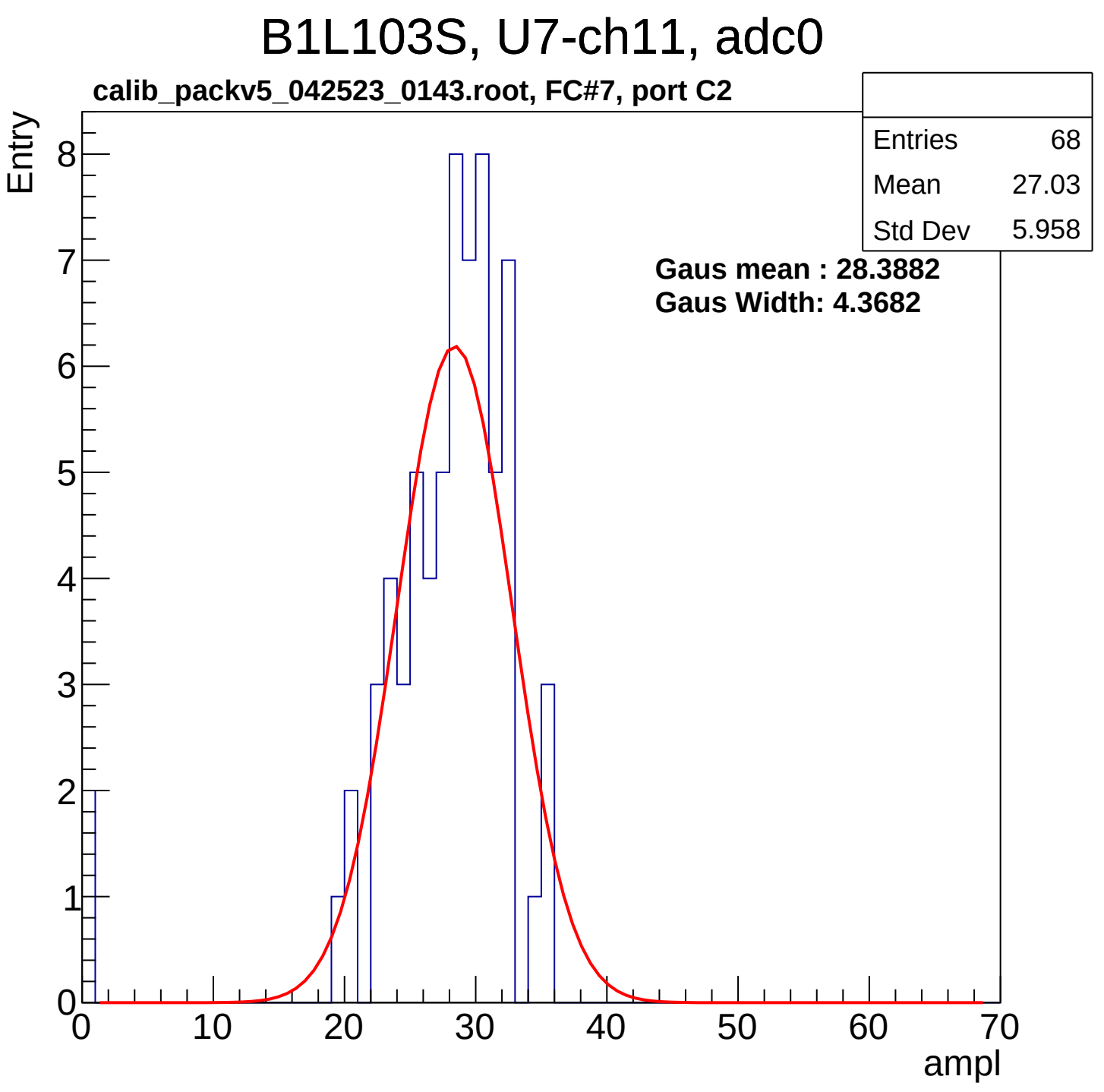
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch10, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 6
Mean 51.5
Std Dev 23.06
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U7-ch10, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 42
Std Dev 29.7
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U7-ch11, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 27.03
Std Dev 5.958
Gaus mean : 28.3882
Gaus Width: 4.3682
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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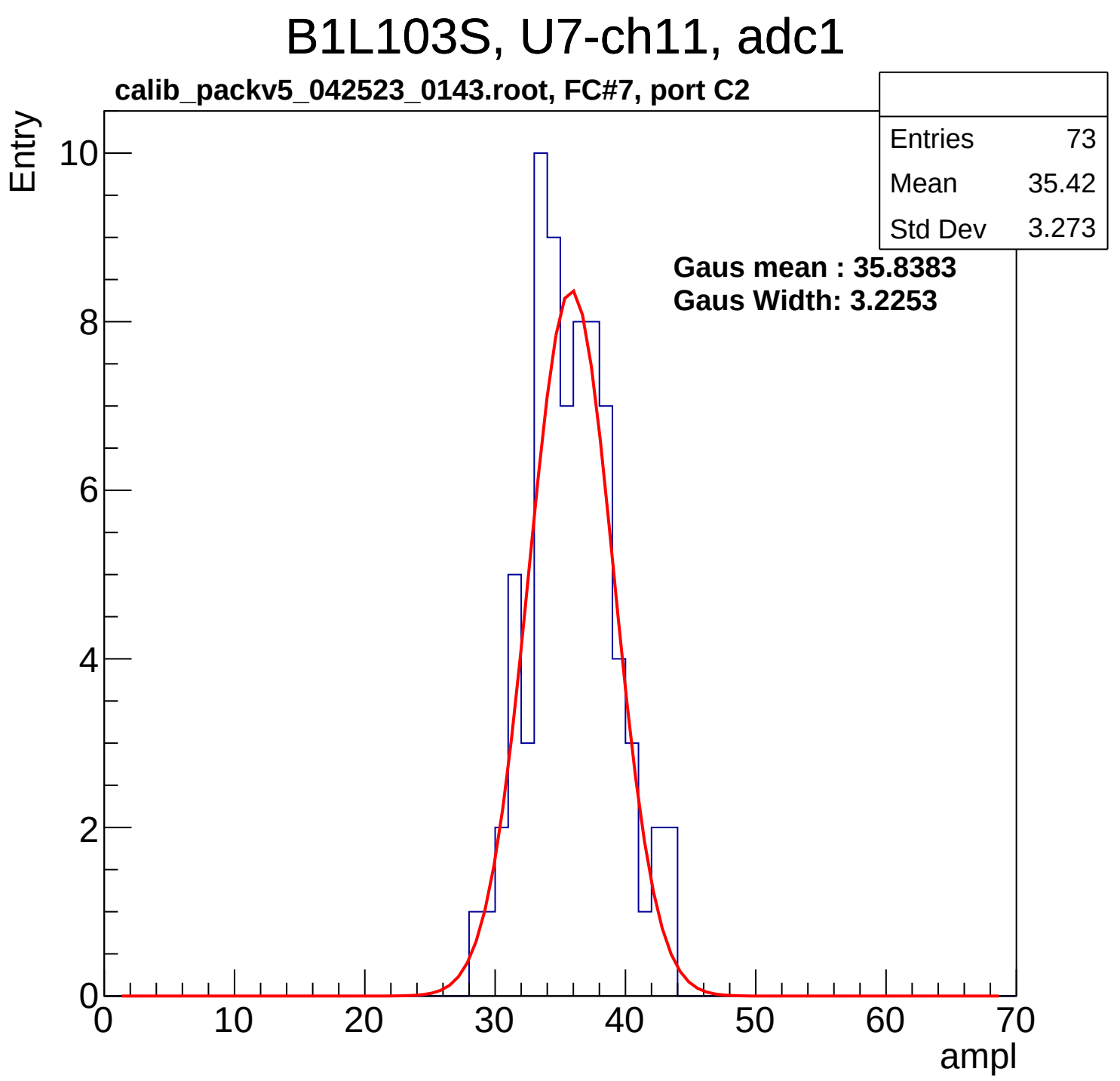
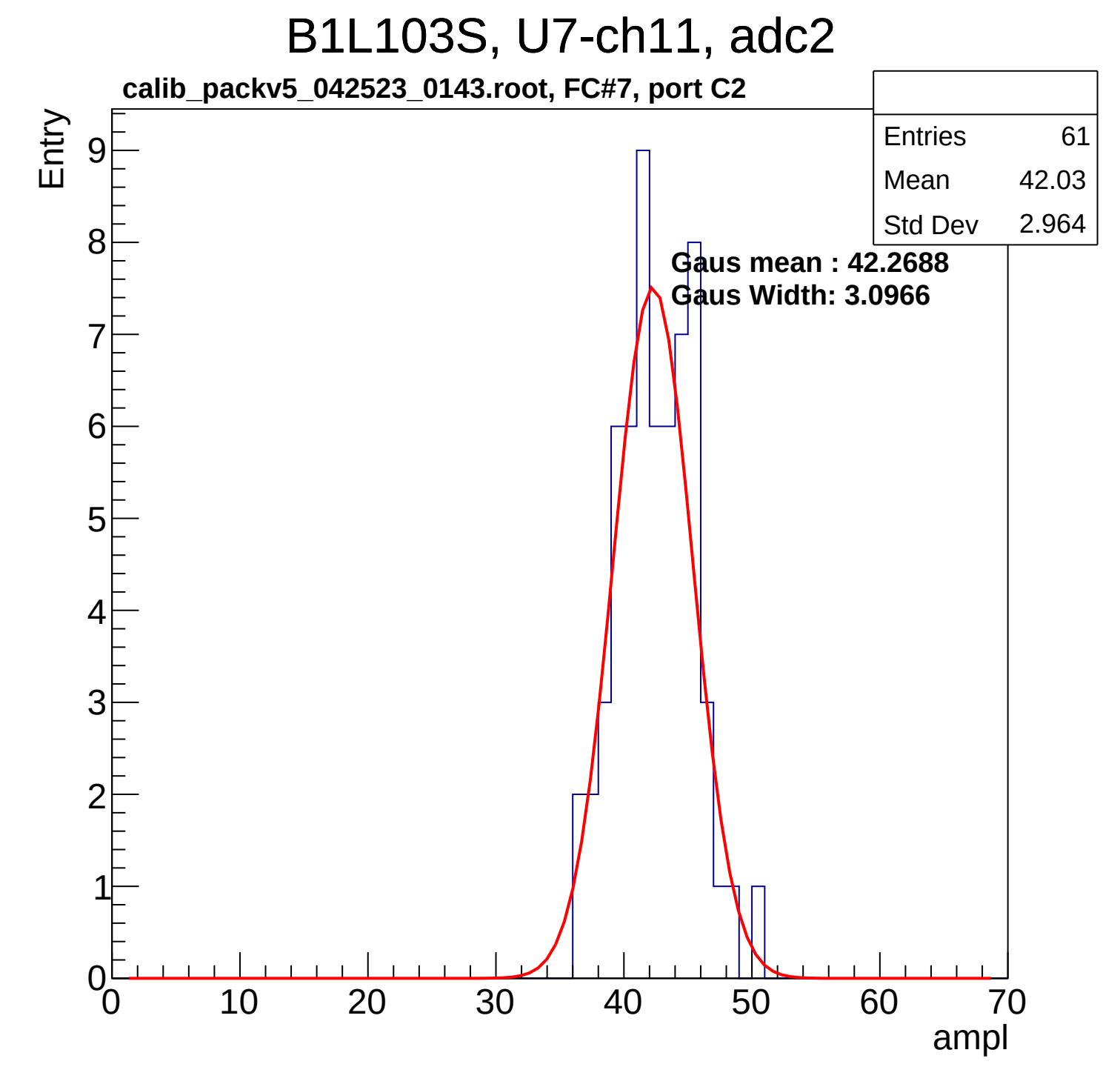
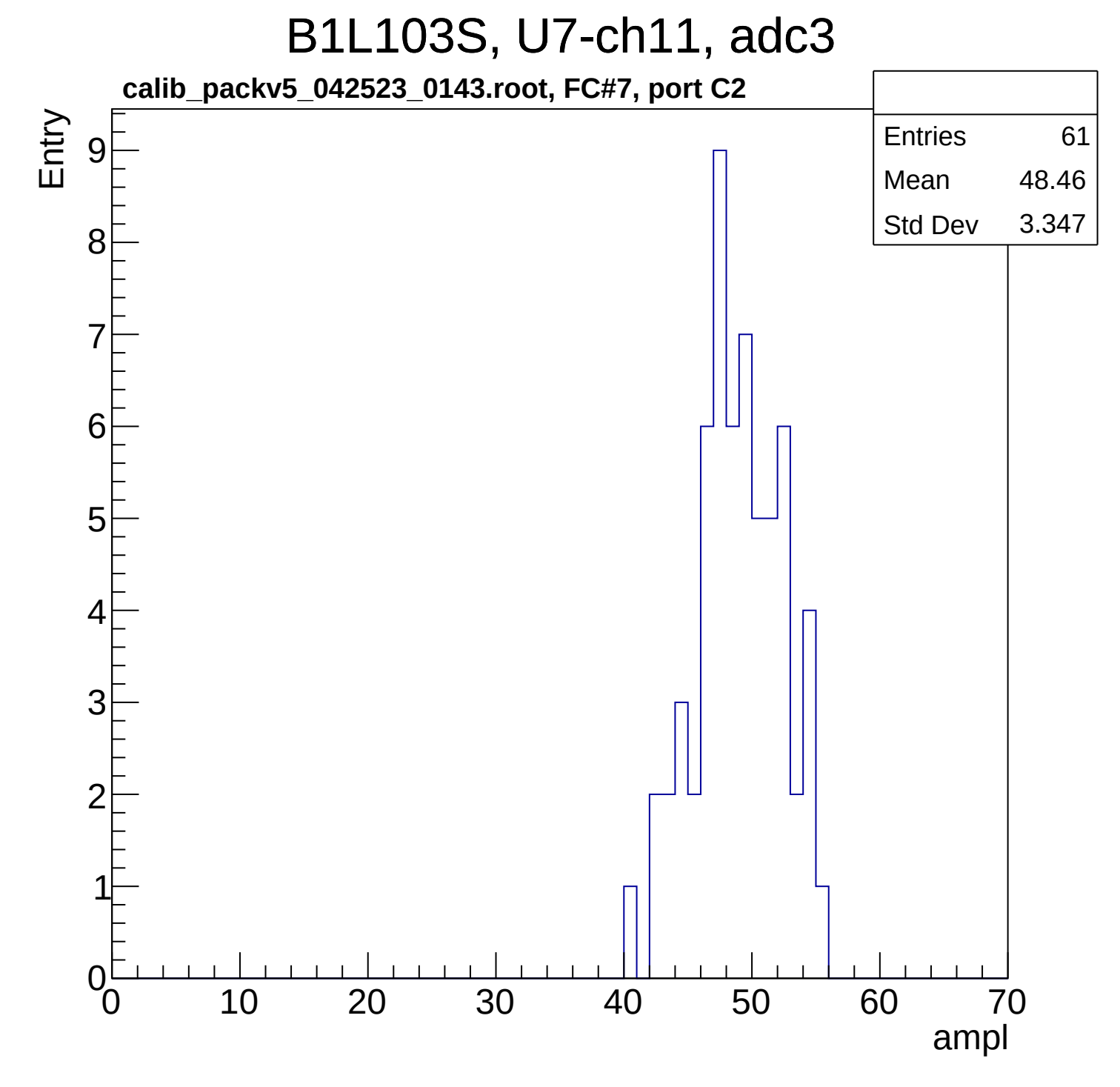
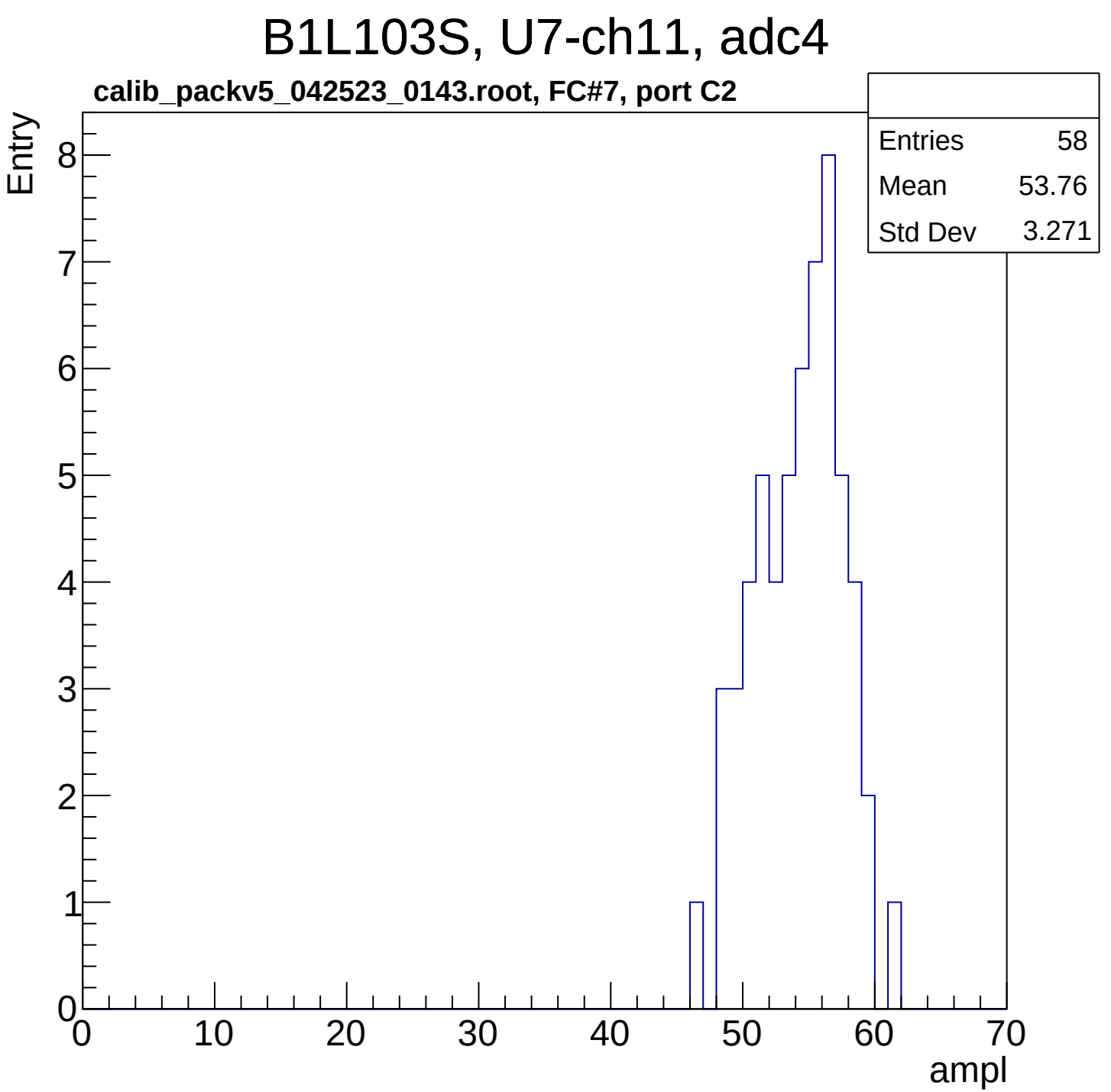
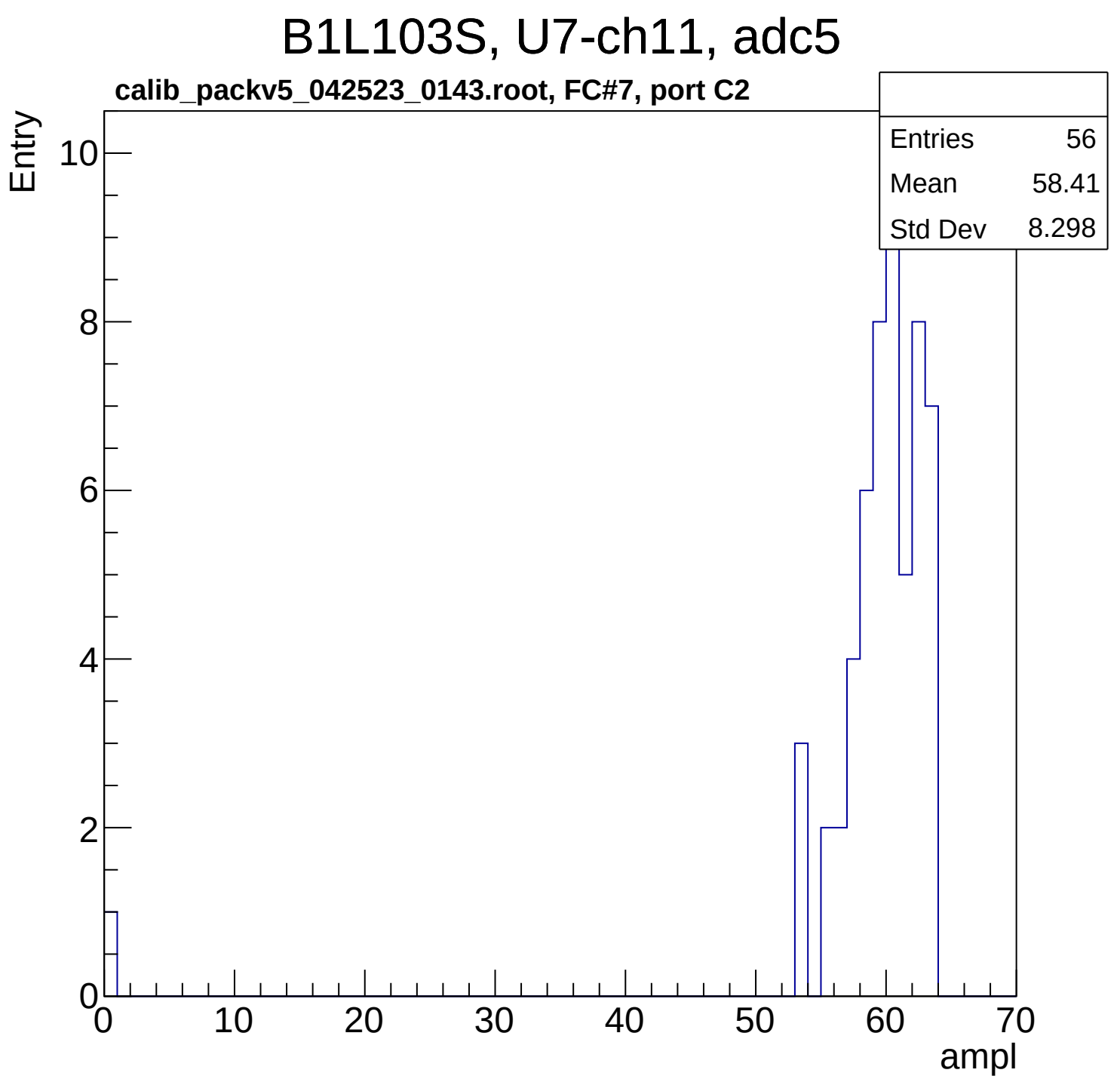
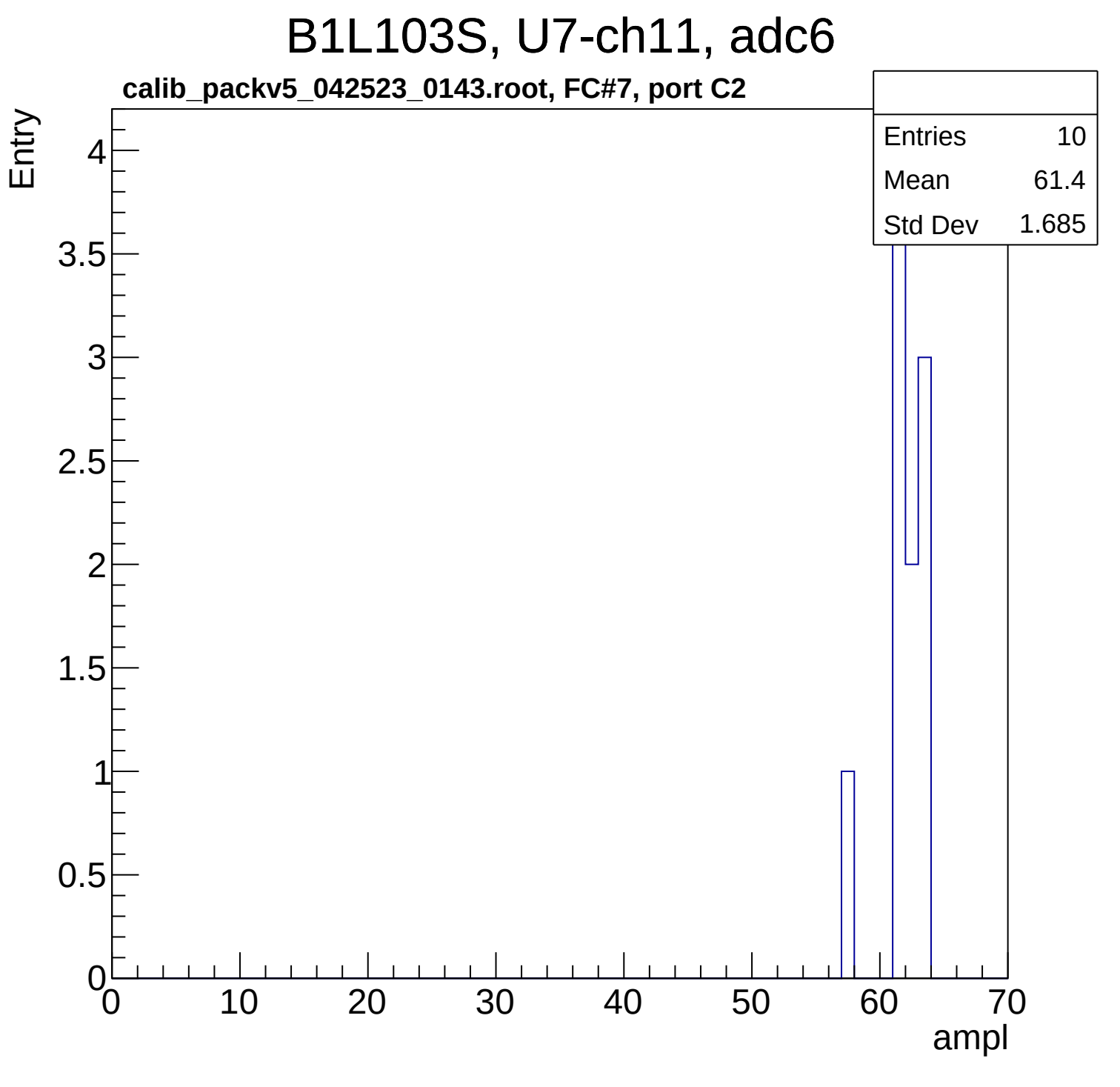

B1L103S, U7-ch11, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 73
Mean 35.42
Std Dev 3.273
Gaus mean : 35.8383
Gaus Width: 3.2253
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

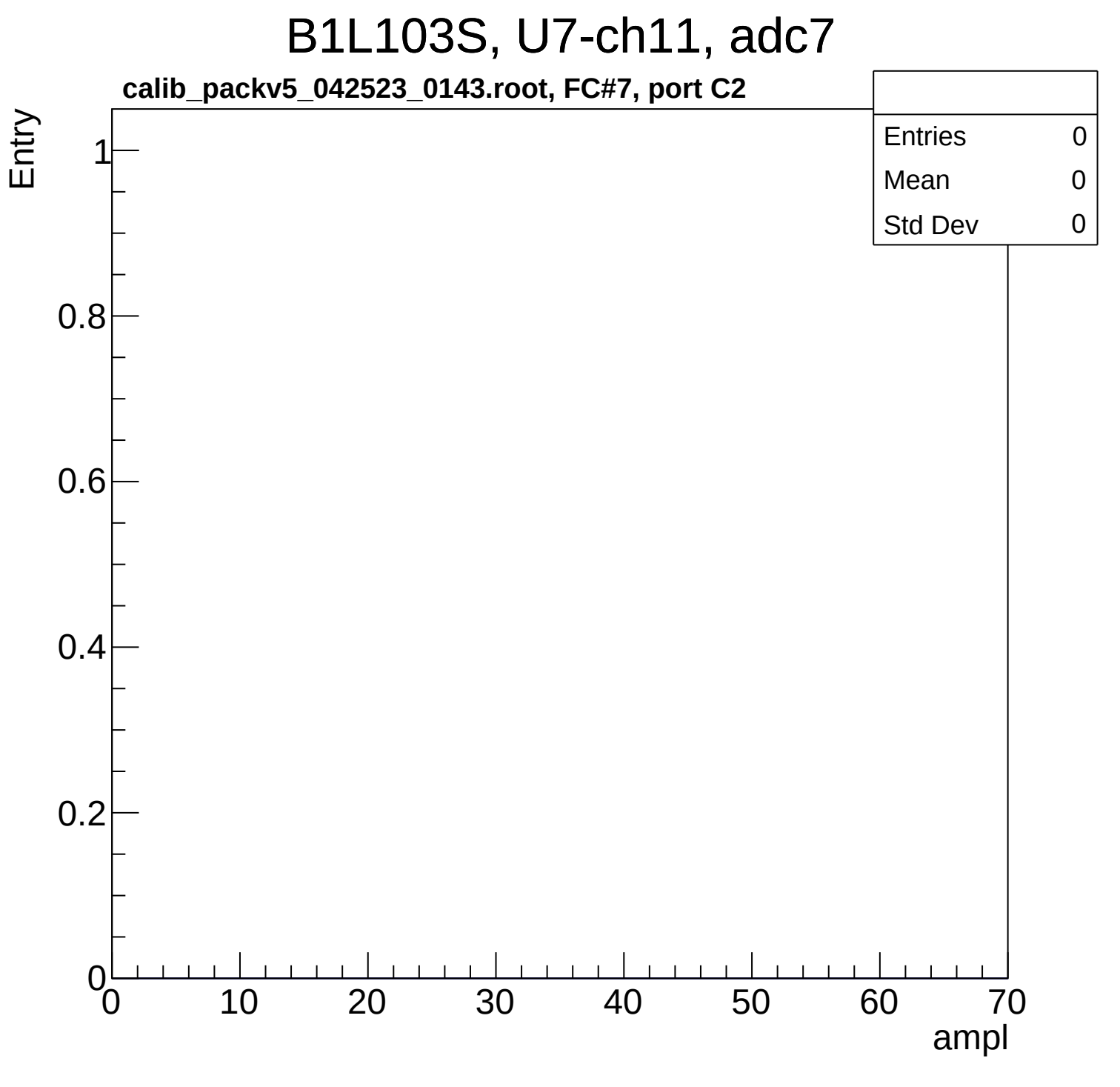

B1L103S, U7-ch11, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 61
Mean 42.03
Std Dev 2.964
Gaus mean : 42.2688
Gaus Width: 3.0966
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

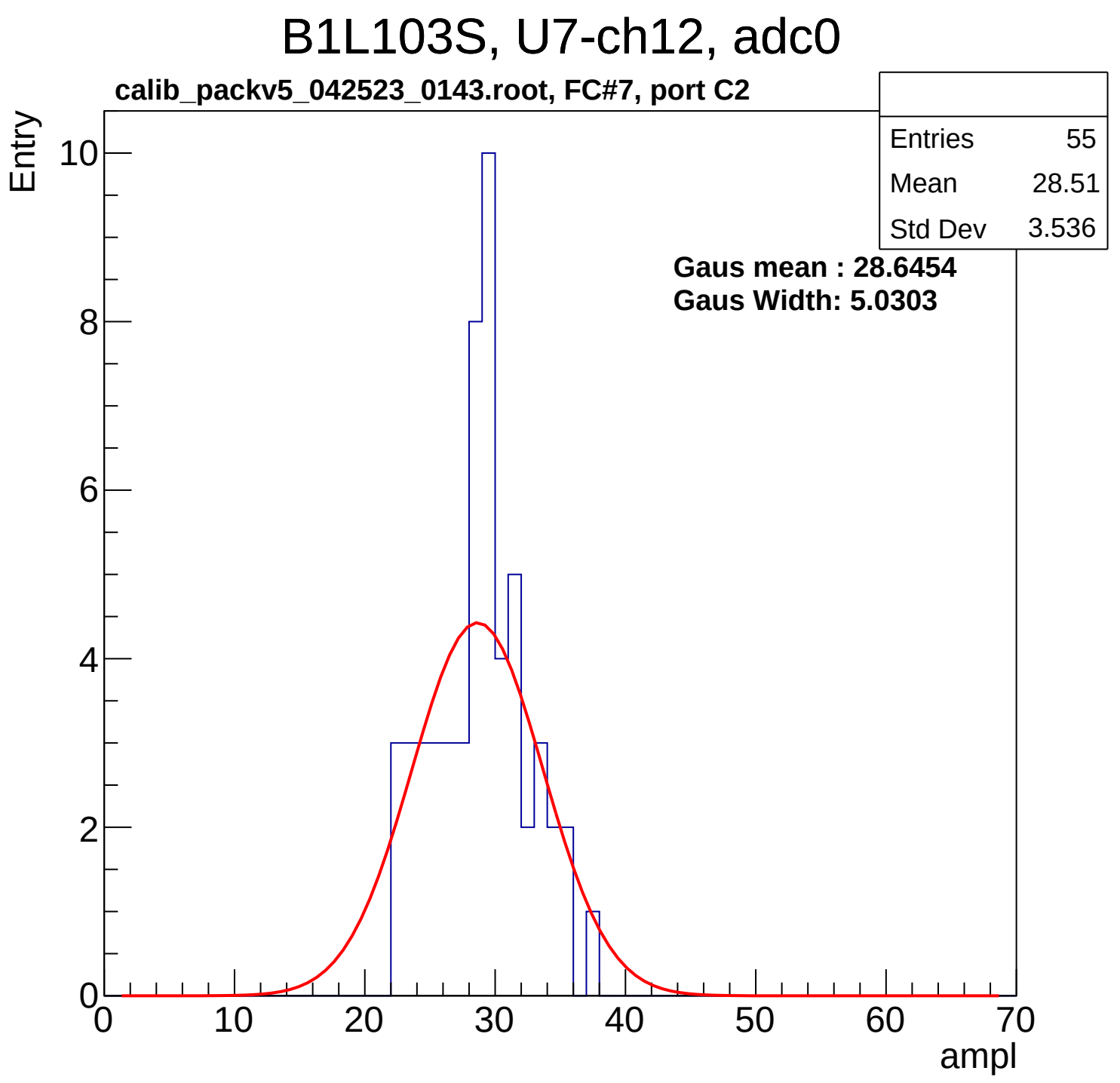

B1L103S, U7-ch11, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 61
Mean 48.46
Std Dev 3.347
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

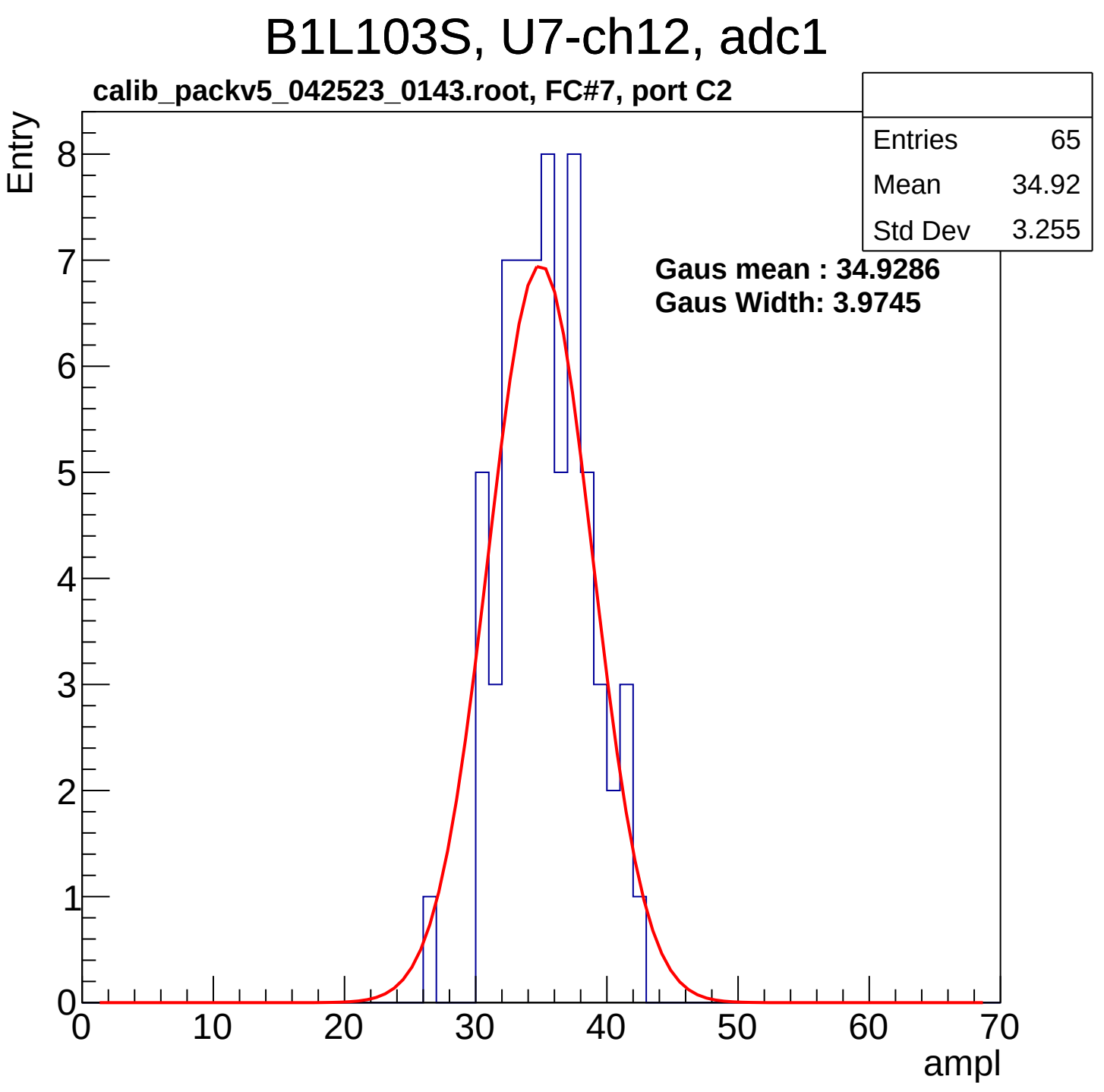

B1L103S, U7-ch11, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 58
Mean 53.76
Std Dev 3.271
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

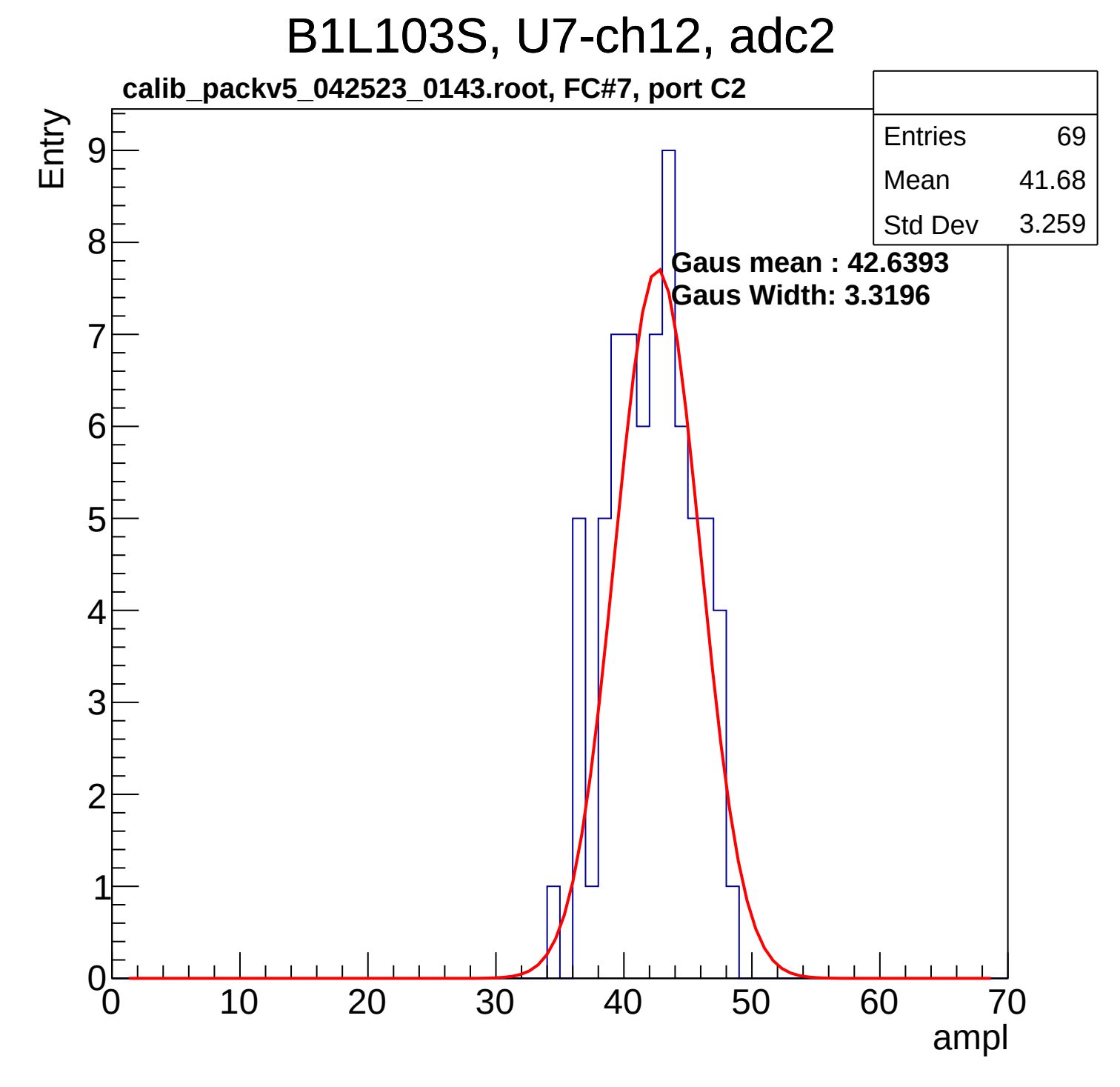

B1L103S, U7-ch11, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 58.41
Std Dev 8.298
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

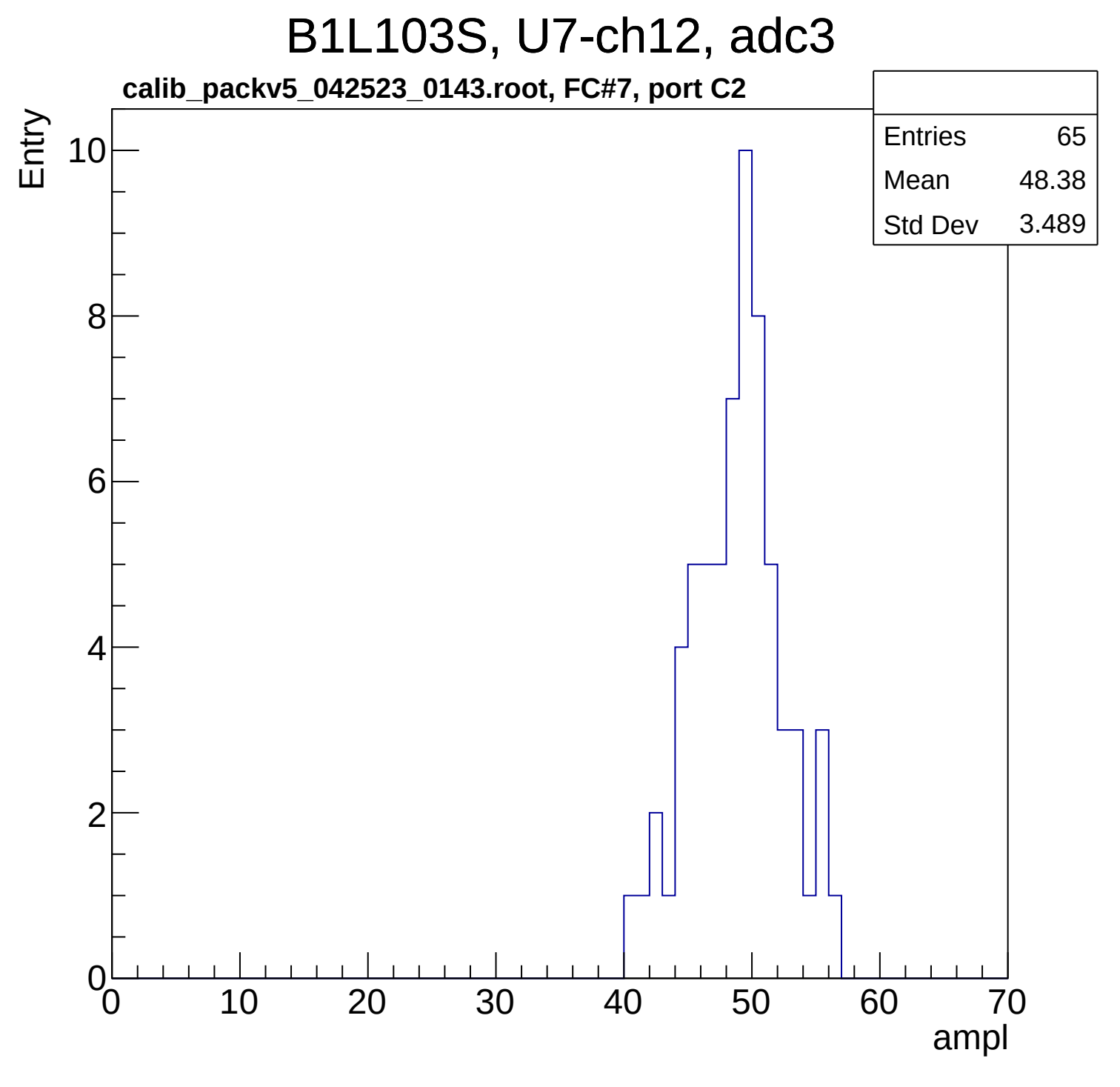

B1L103S, U7-ch11, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 10
Mean 61.4
Std Dev 1.685
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

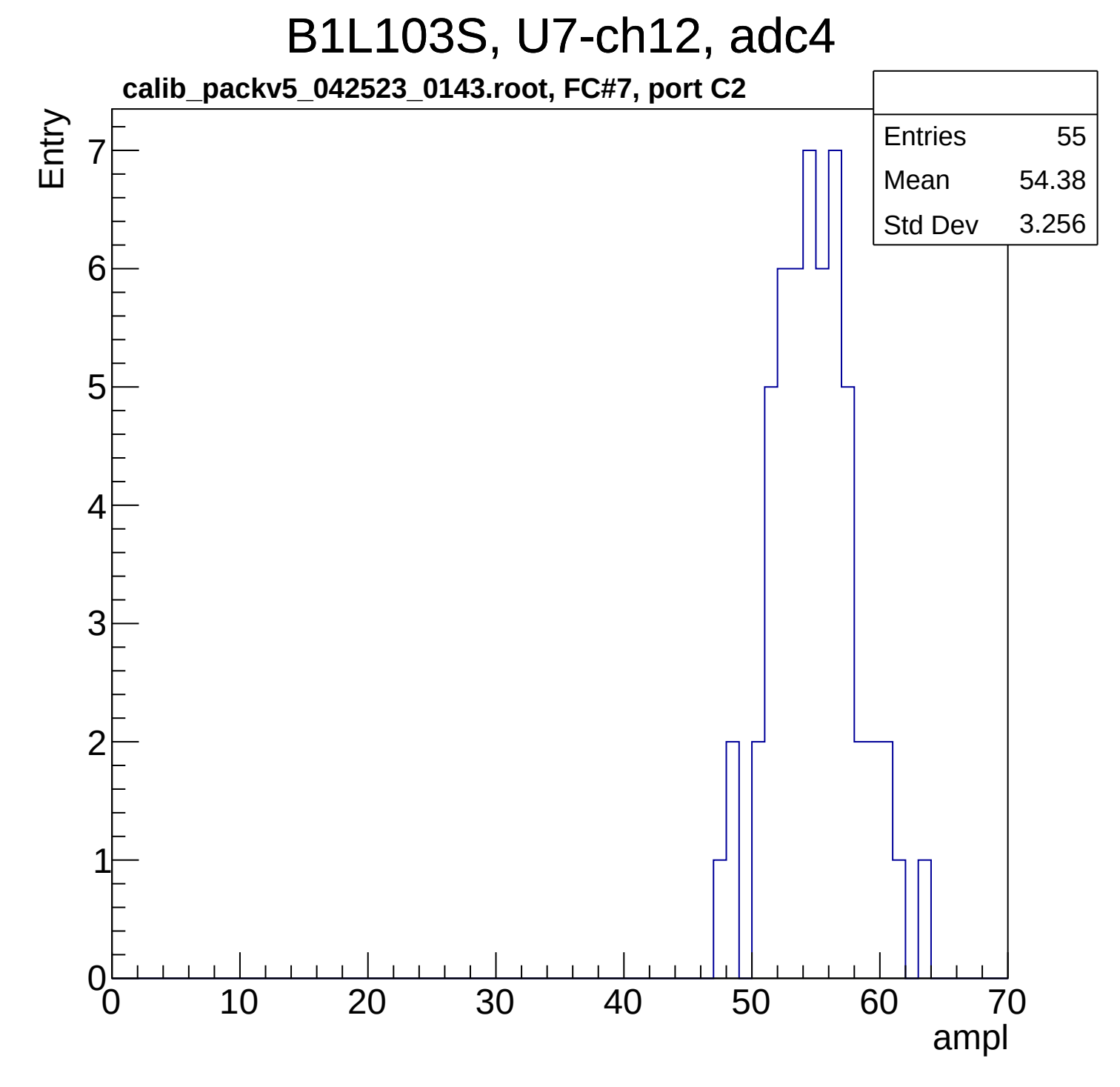

B1L103S, U7-ch11, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

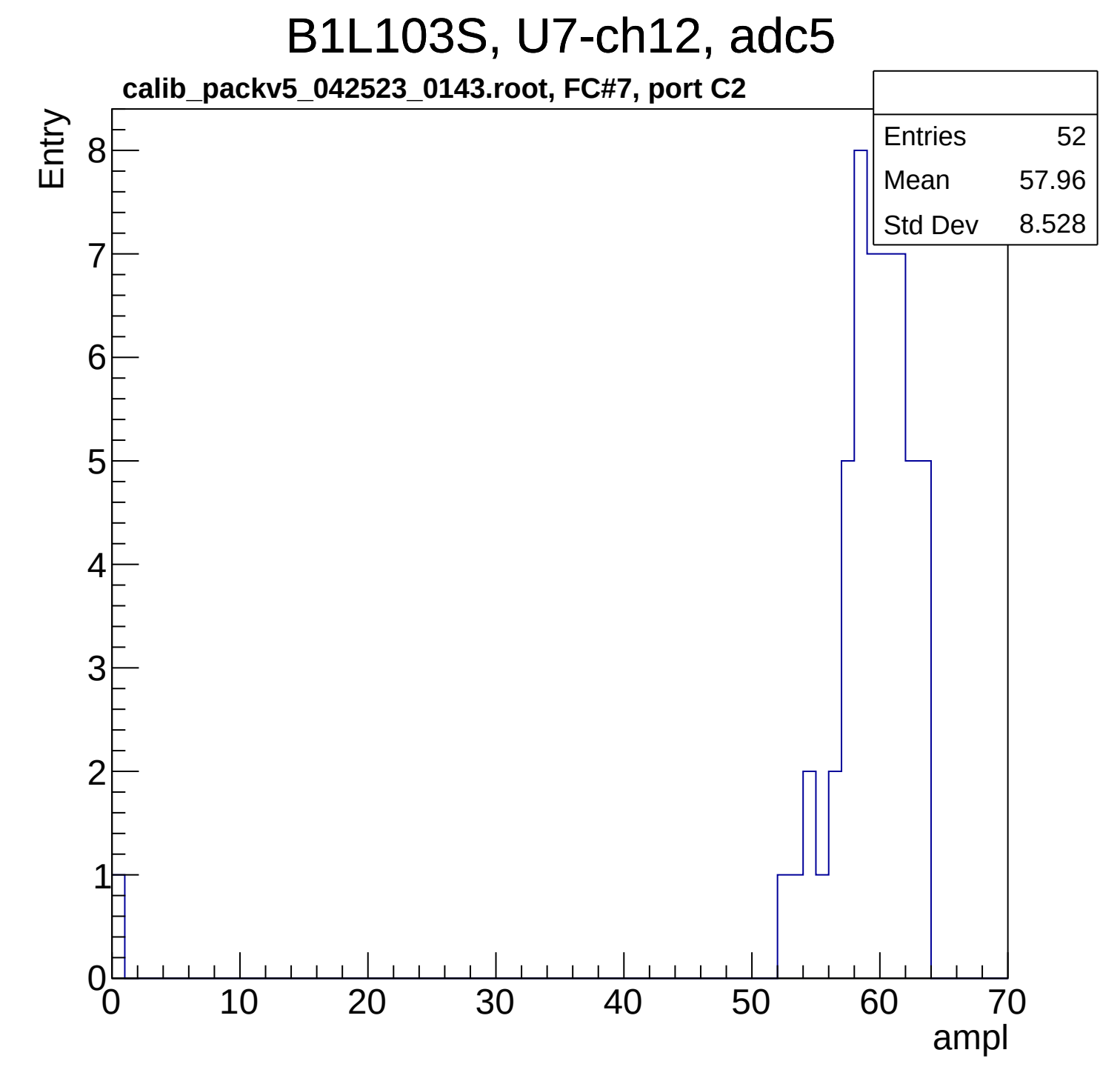

B1L103S, U7-ch12, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 28.51
Std Dev 3.536
Gaus mean : 28.6454
Gaus Width: 5.0303
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

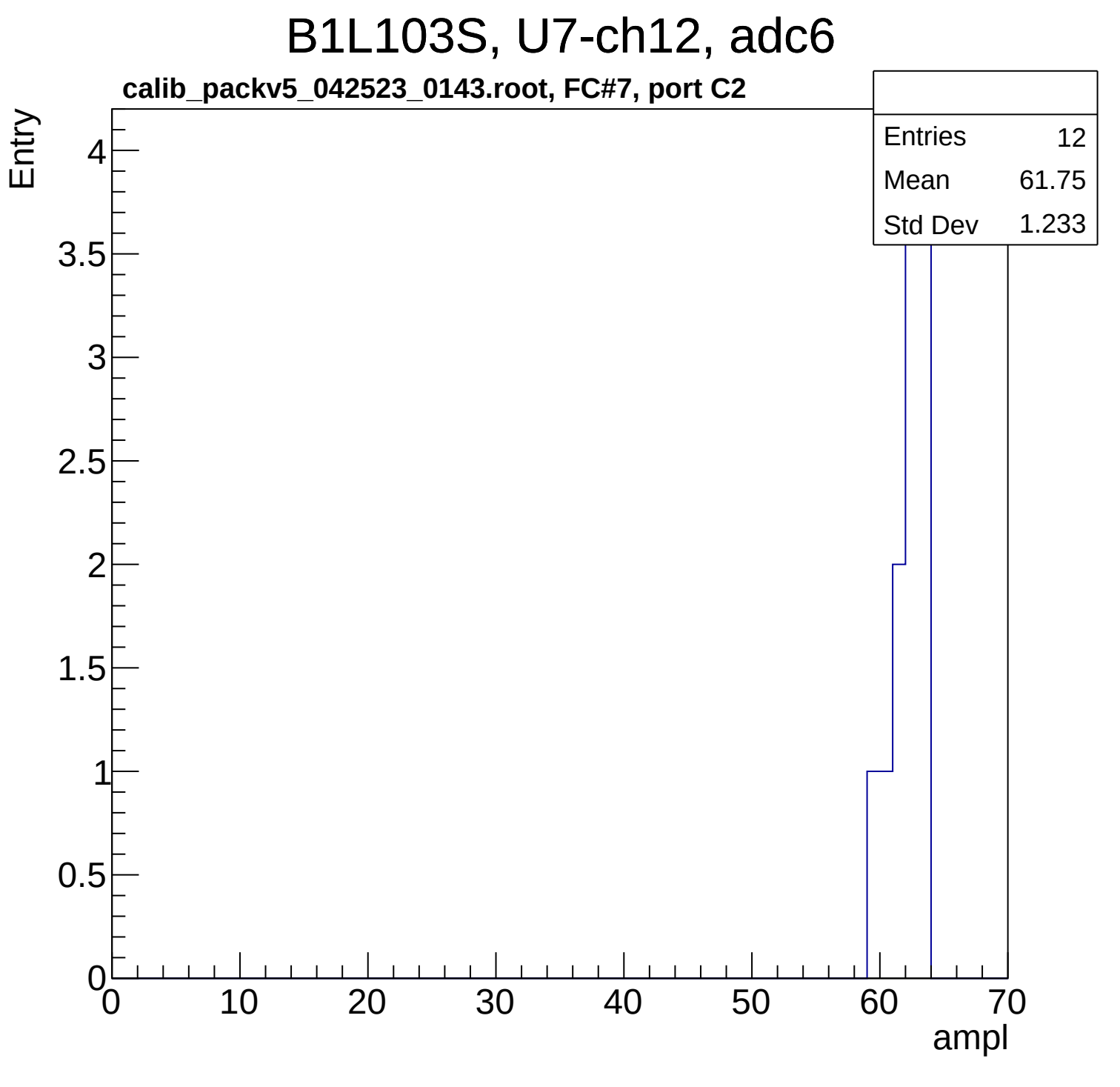

B1L103S, U7-ch12, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 34.92
Std Dev 3.255
Gaus mean : 34.9286
Gaus Width: 3.9745
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

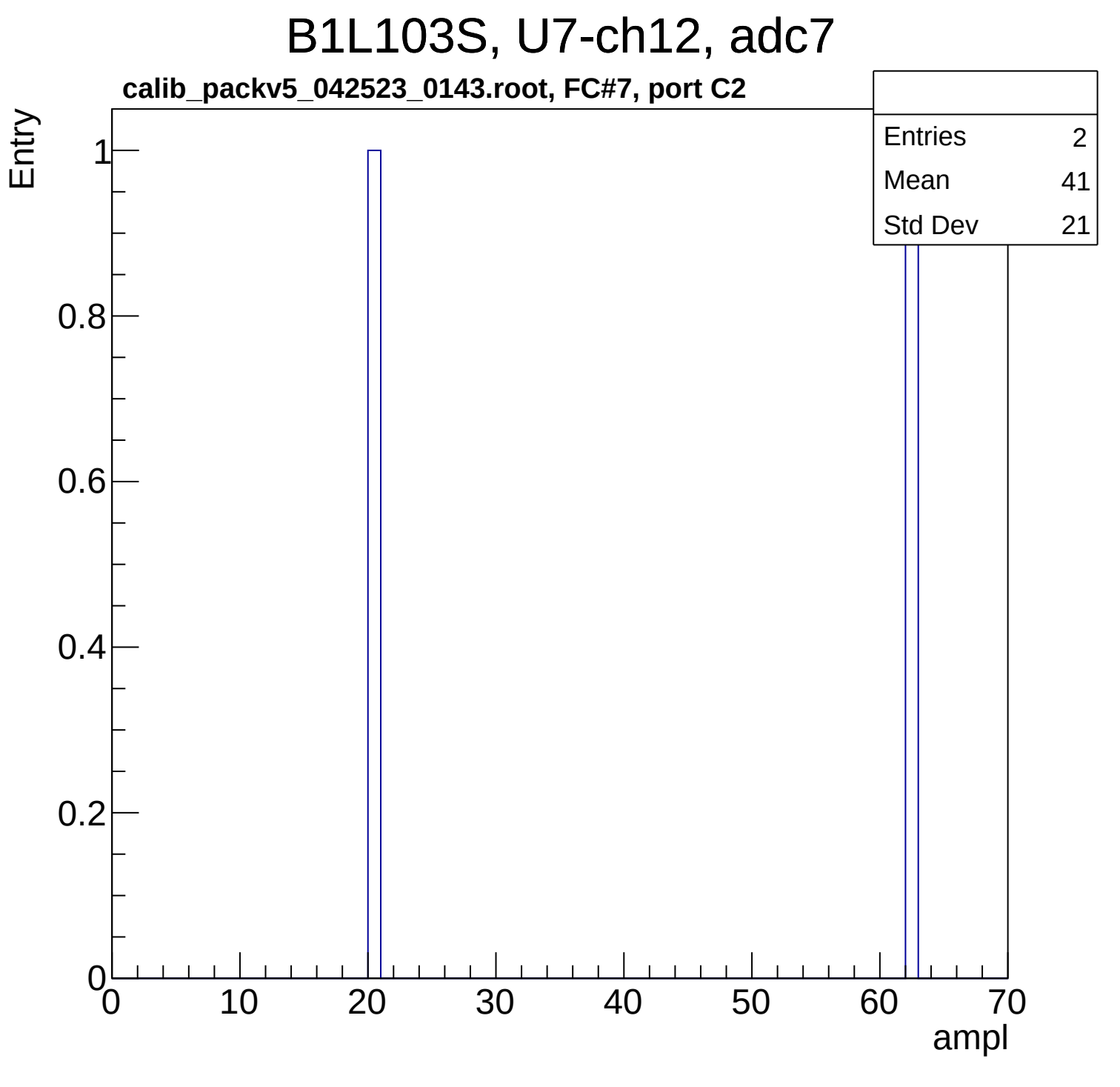

B1L103S, U7-ch12, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 41.68
Std Dev 3.259
Gaus mean : 42.6393
Gaus Width: 3.3196
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

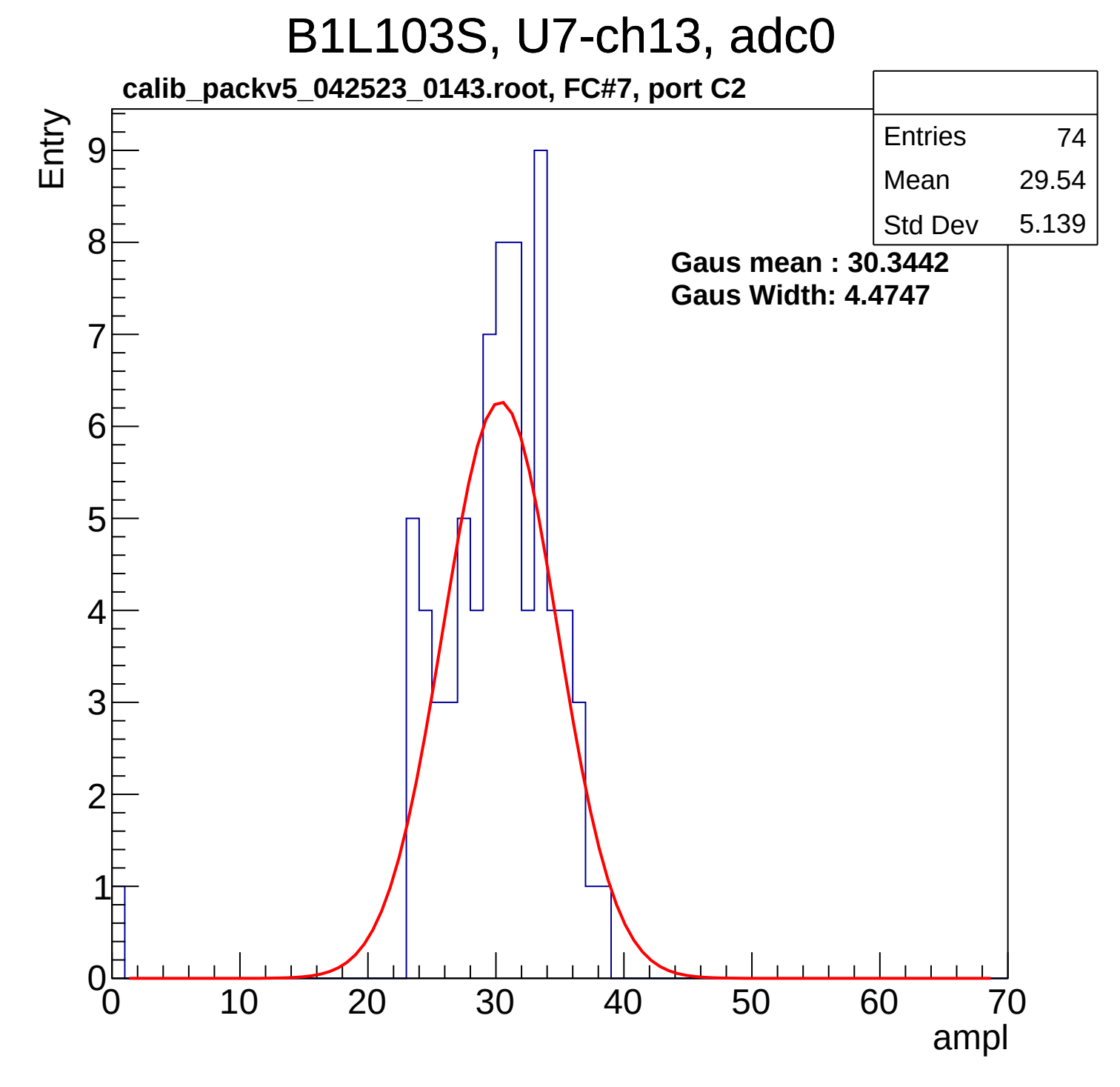

B1L103S, U7-ch12, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 48.38
Std Dev 3.489
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

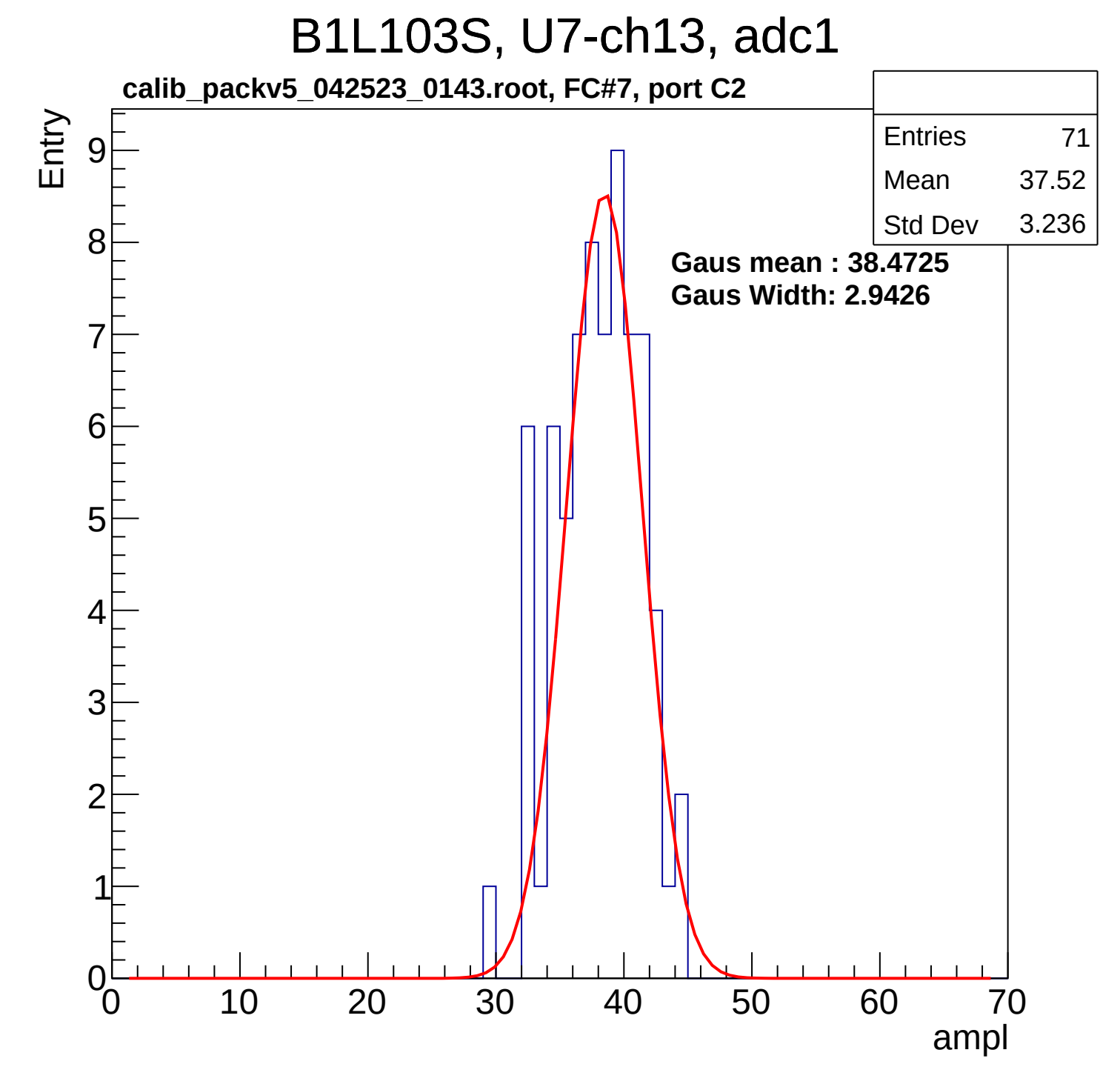

B1L103S, U7-ch12, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 54.38
Std Dev 3.256
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

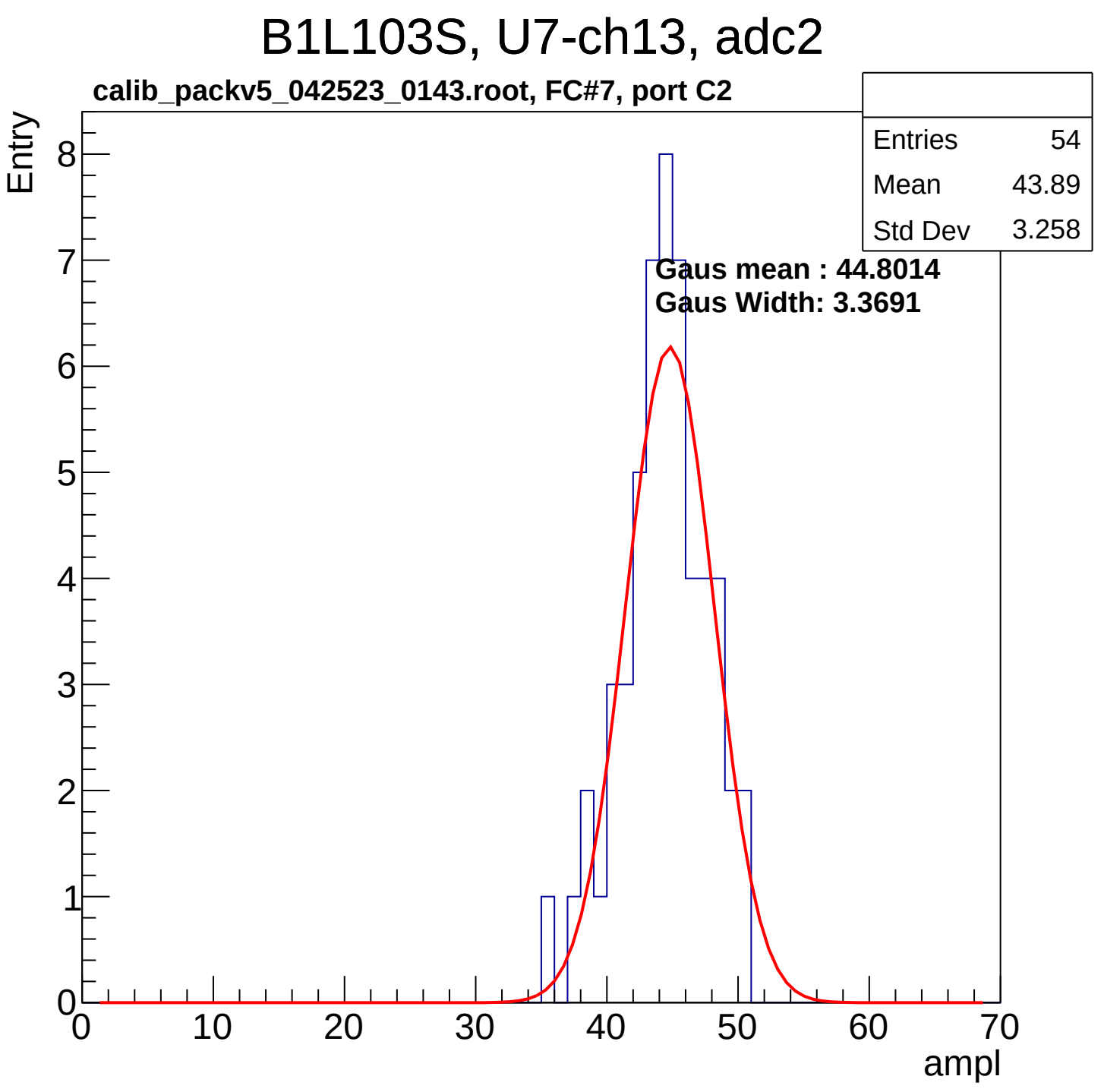

B1L103S, U7-ch12, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 52
Mean 57.96
Std Dev 8.528
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

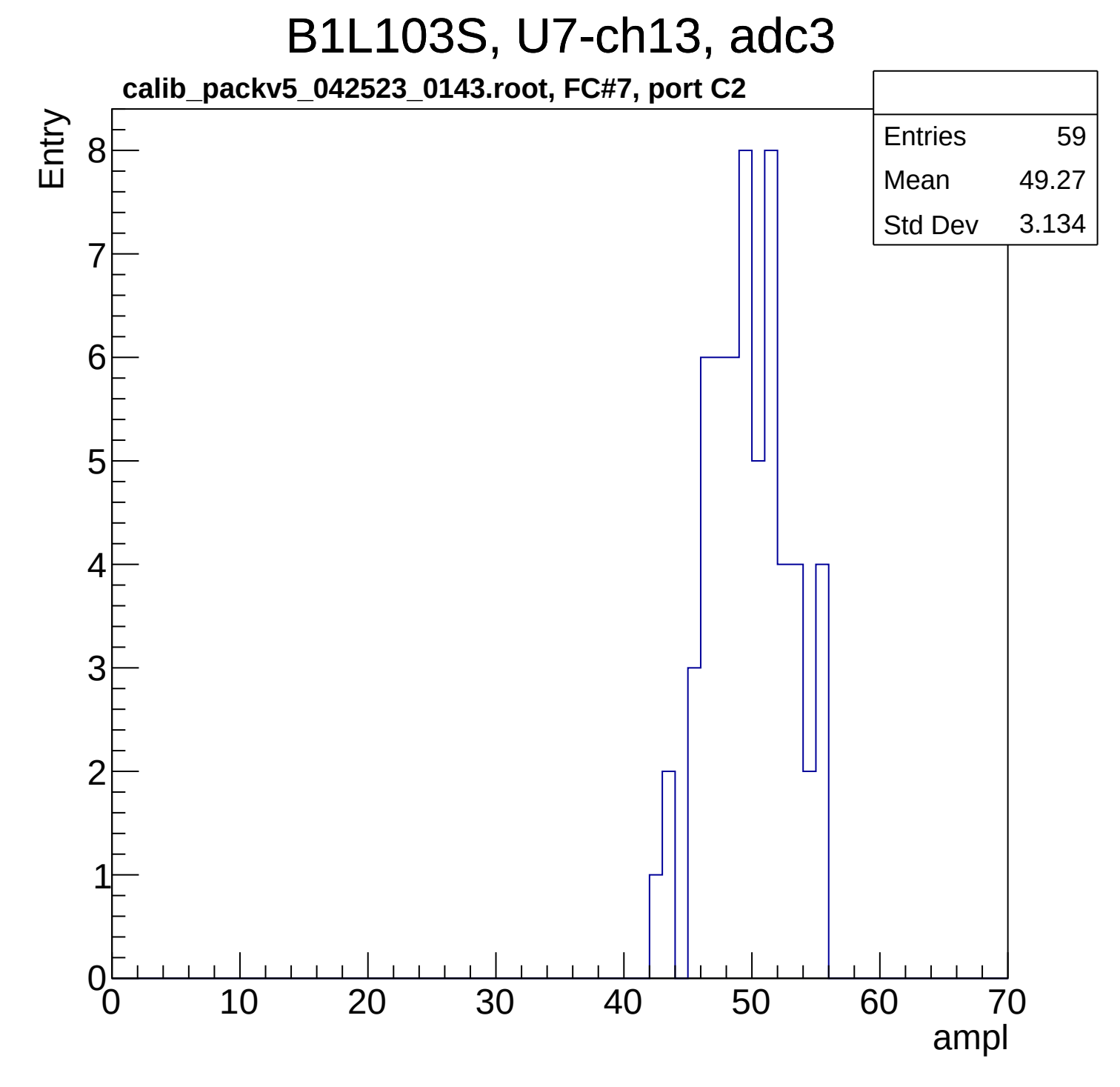

B1L103S, U7-ch12, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 12
Mean 61.75
Std Dev 1.233
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

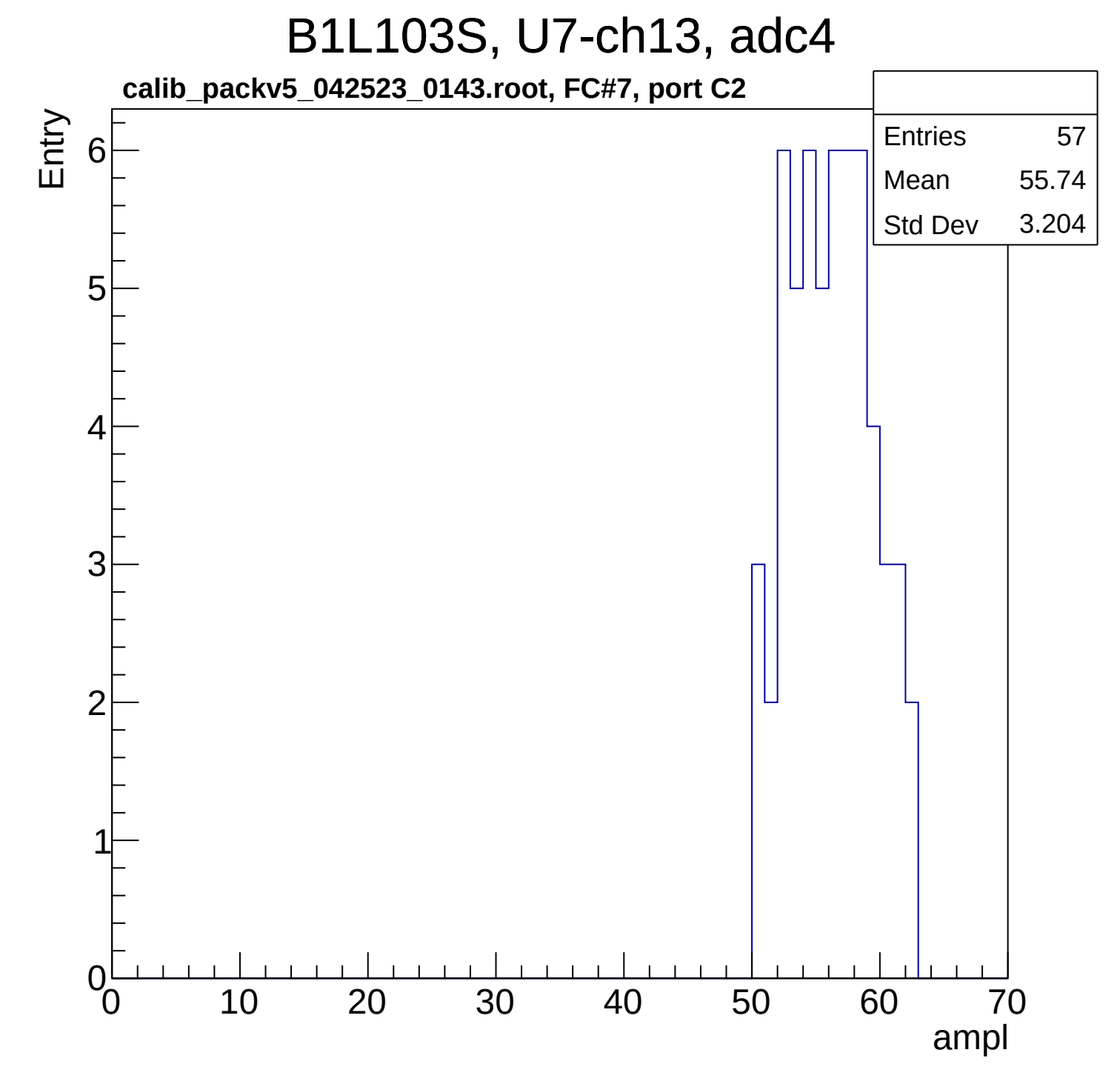

B1L103S, U7-ch12, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 41
Std Dev 21
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

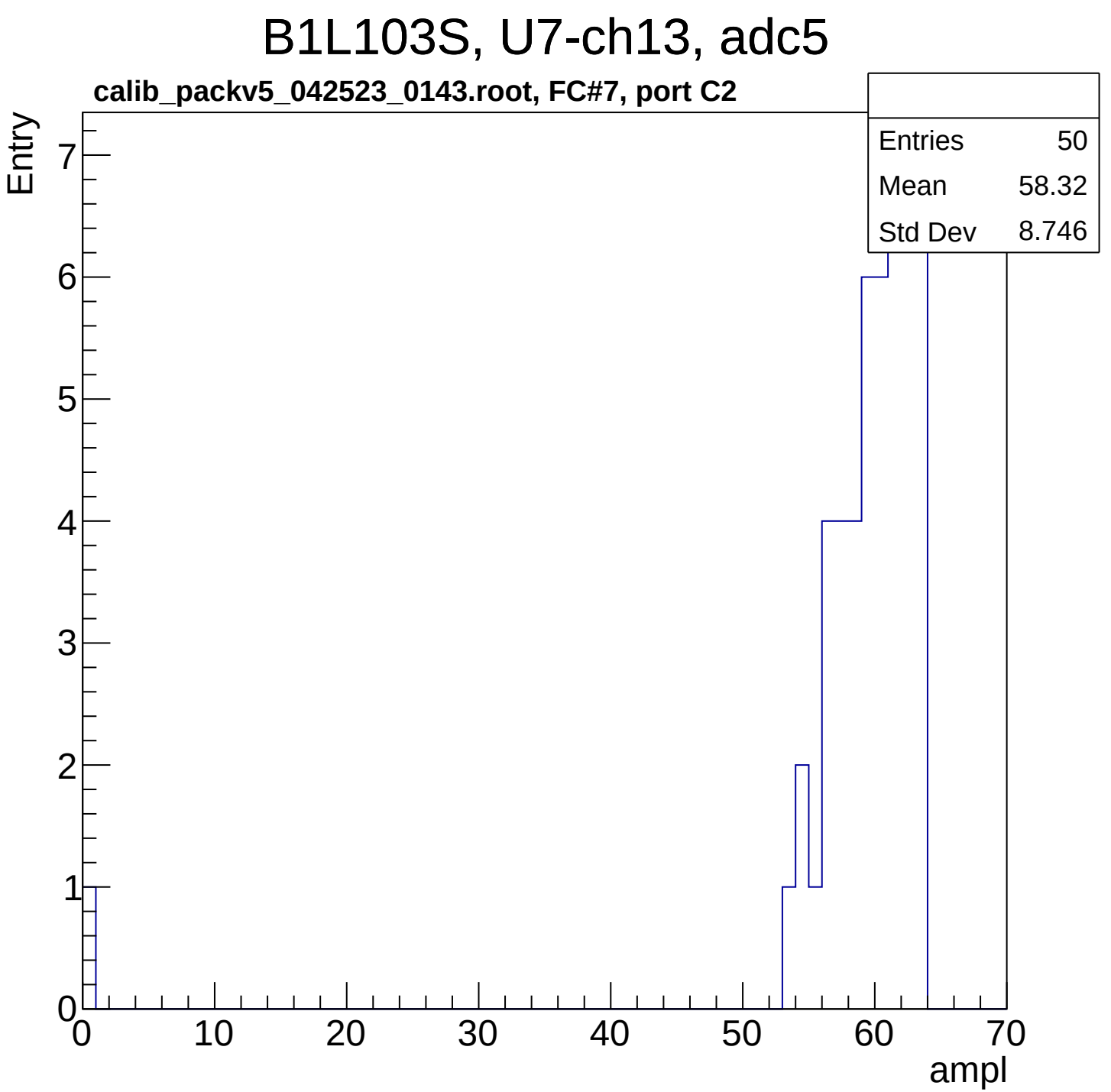

B1L103S, U7-ch13, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 74
Mean 29.54
Std Dev 5.139
Gaus mean : 30.3442
Gaus Width: 4.4747
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch13, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 71
Mean 37.52
Std Dev 3.236
Gaus mean : 38.4725
Gaus Width: 2.9426
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch13, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 54
Mean 43.89
Std Dev 3.258
Gaus mean : 44.8014
Gaus Width: 3.3691
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch13, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 49.27
Std Dev 3.134
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch13, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 55.74
Std Dev 3.204
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U7-ch13, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 50
Mean 58.32
Std Dev 8.746
Entry
ampl
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1
2
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4
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0
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20
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40
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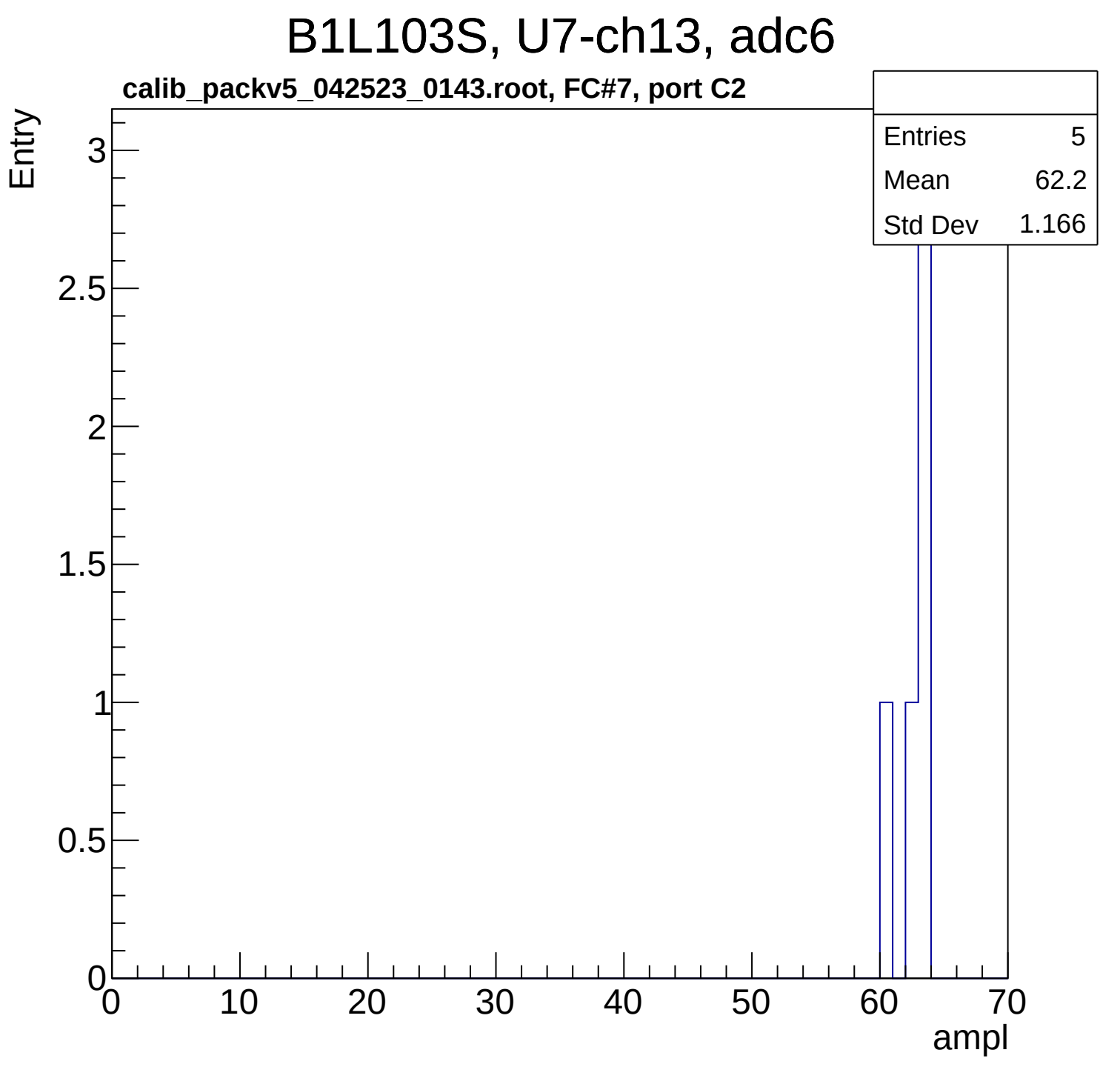
60
70


B1L103S, U7-ch13, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 5
Mean 62.2
Std Dev 1.166
Entry
ampl
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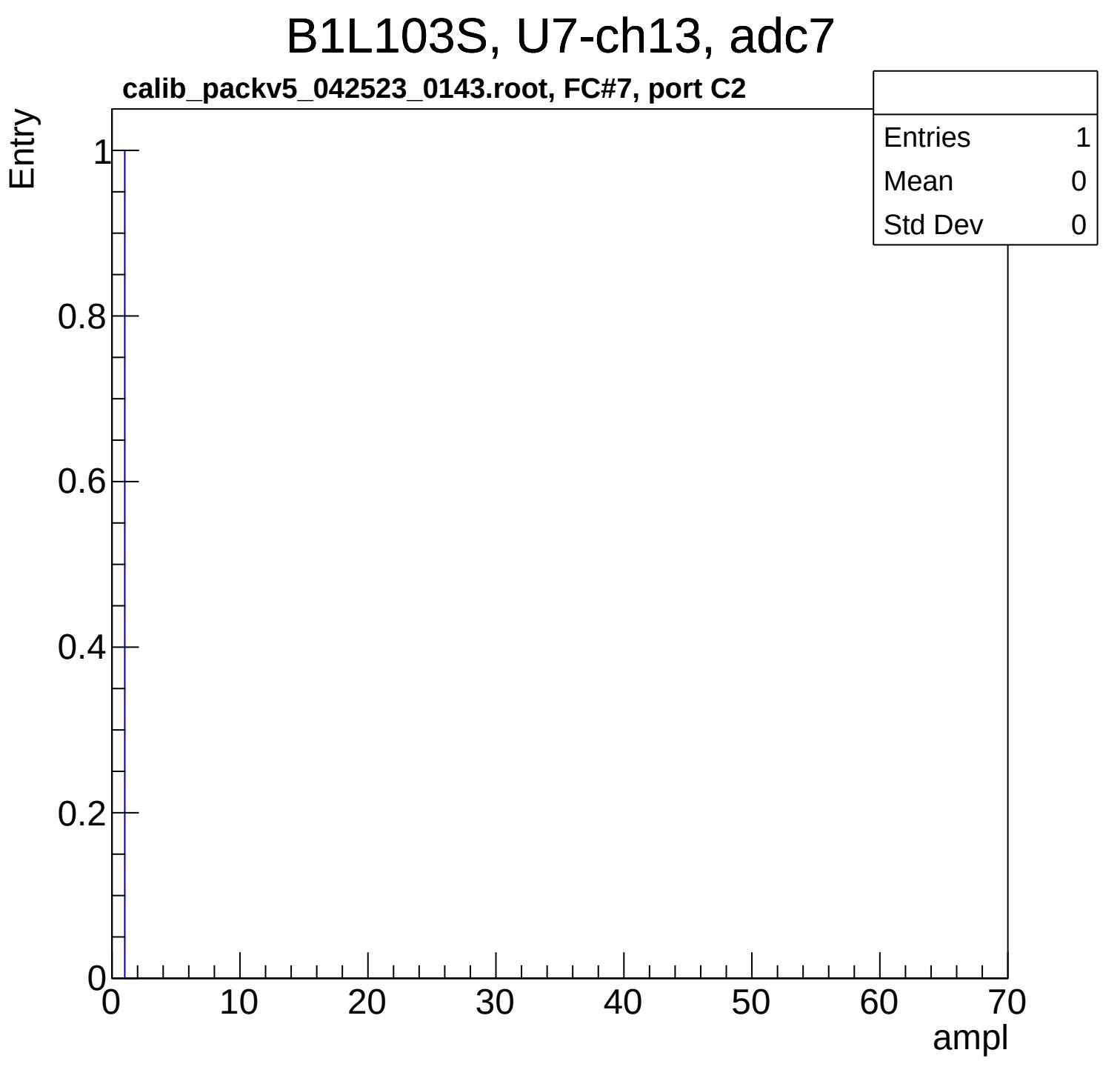
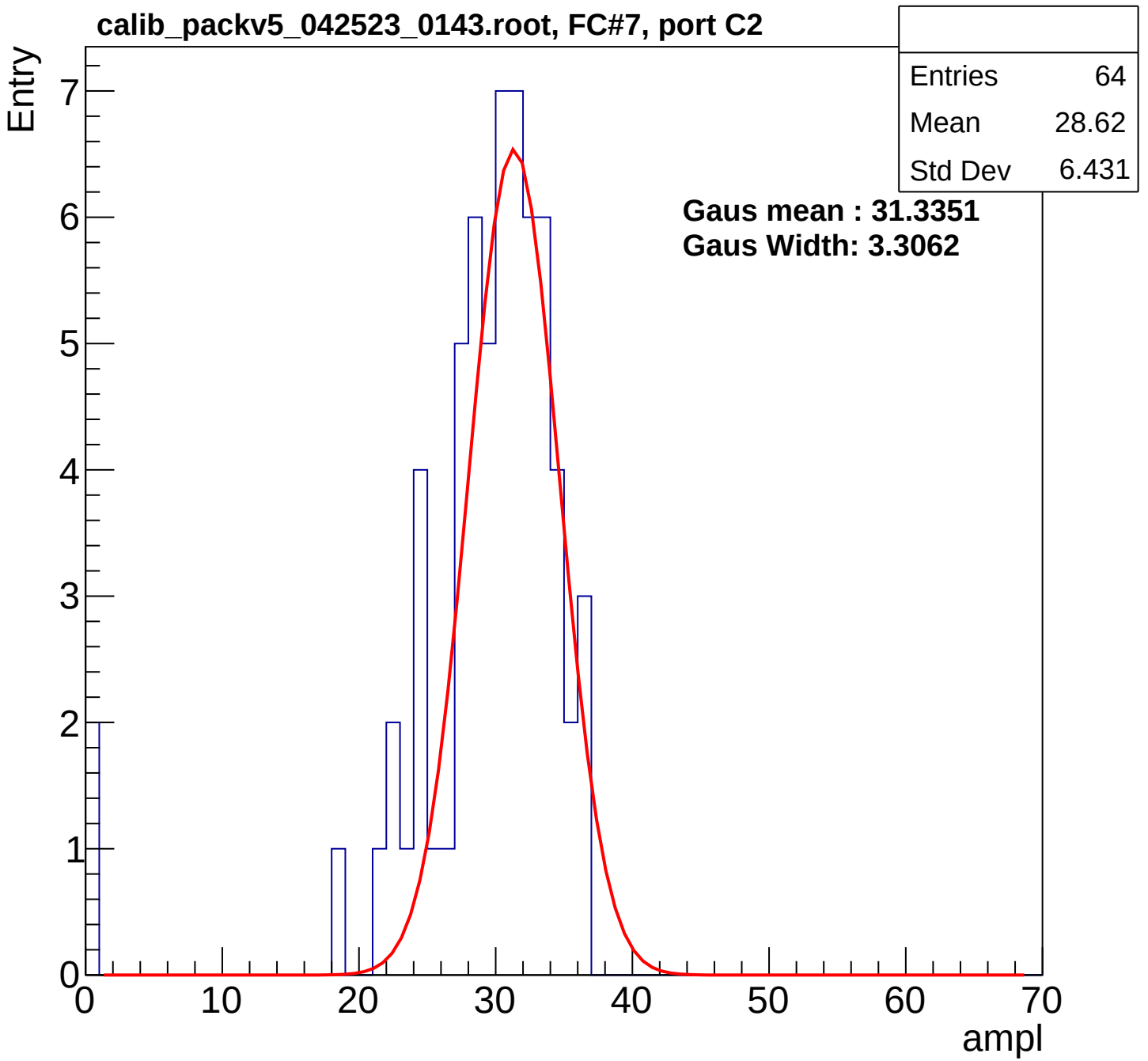
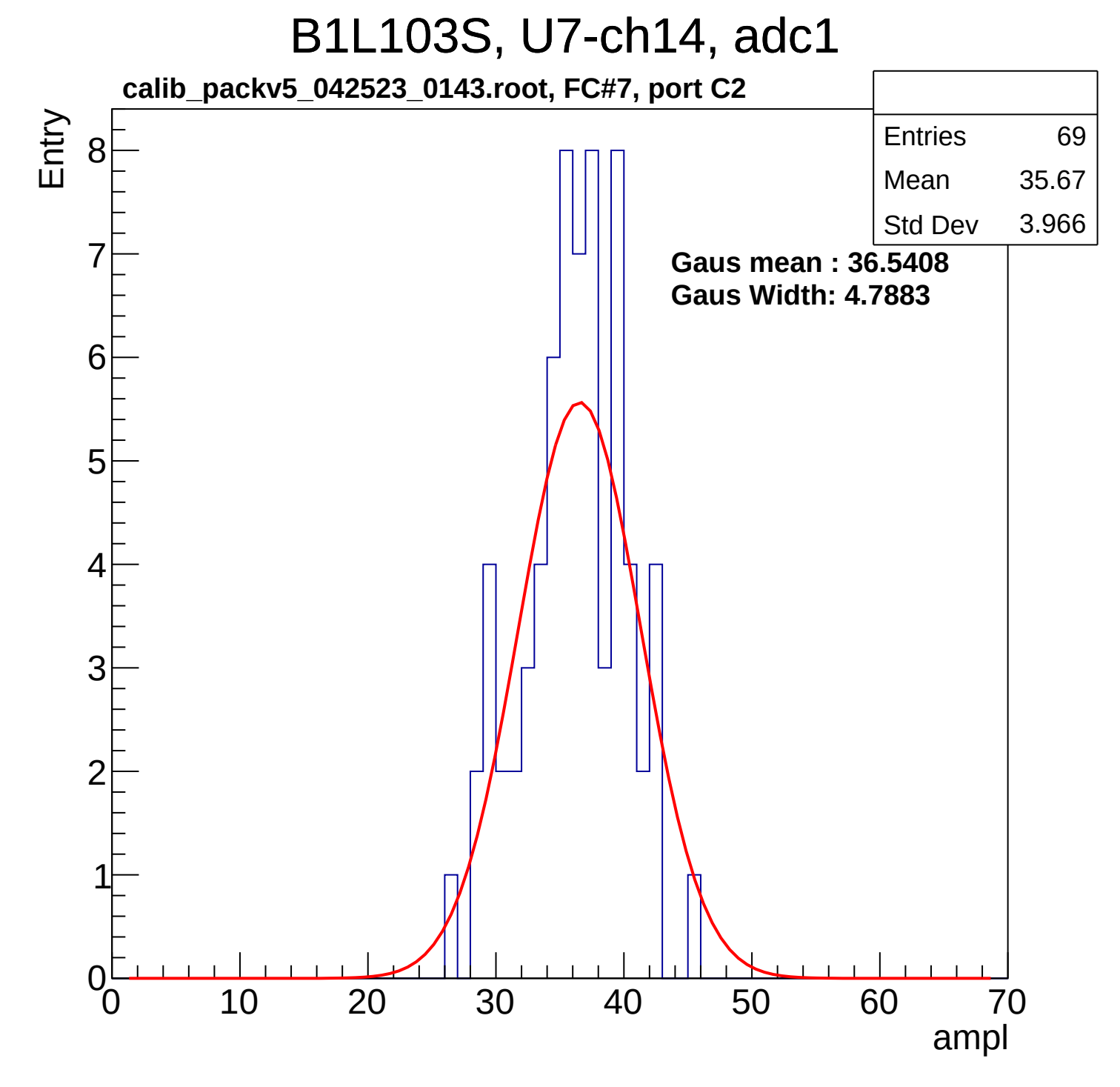
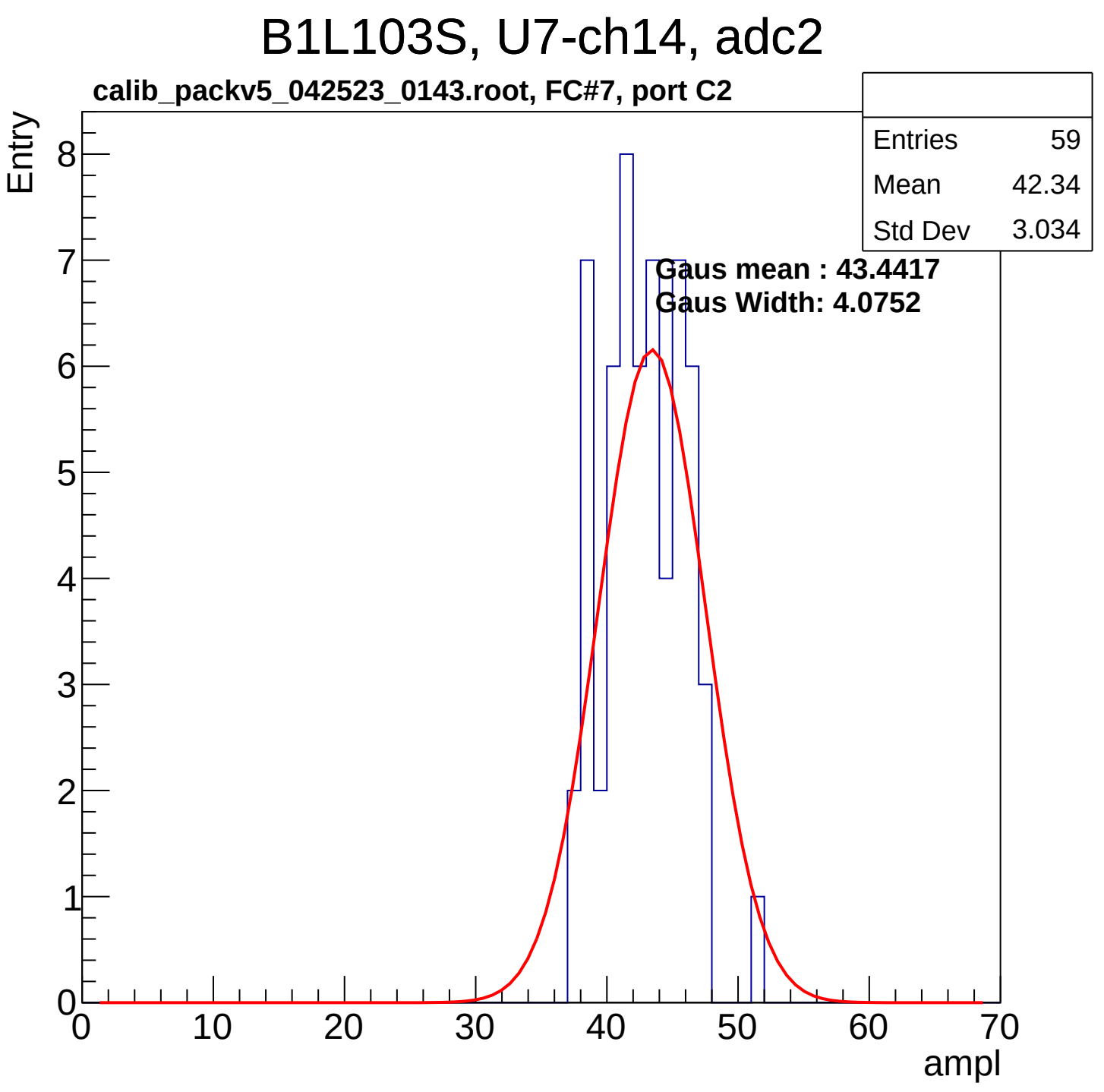
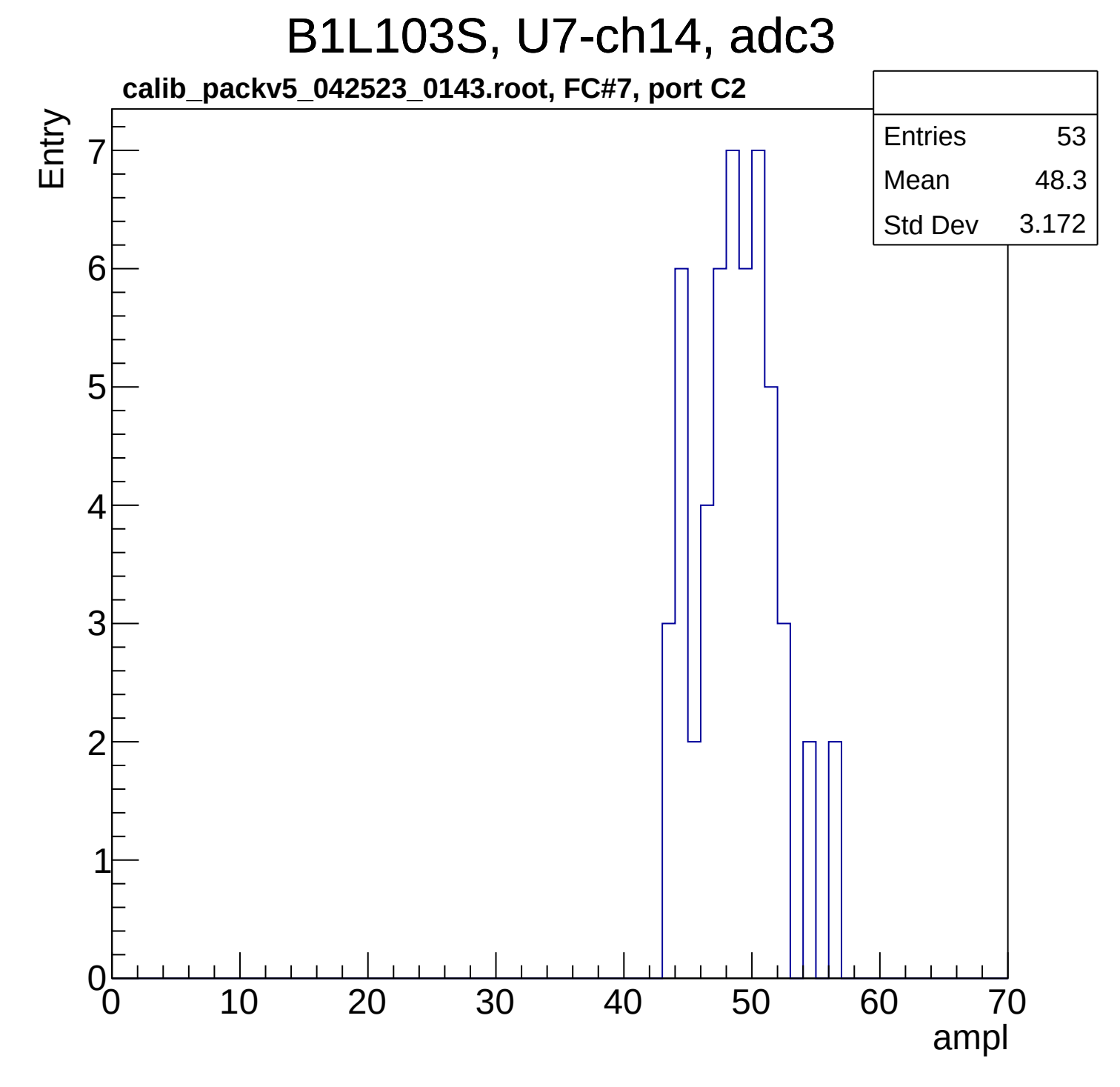
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

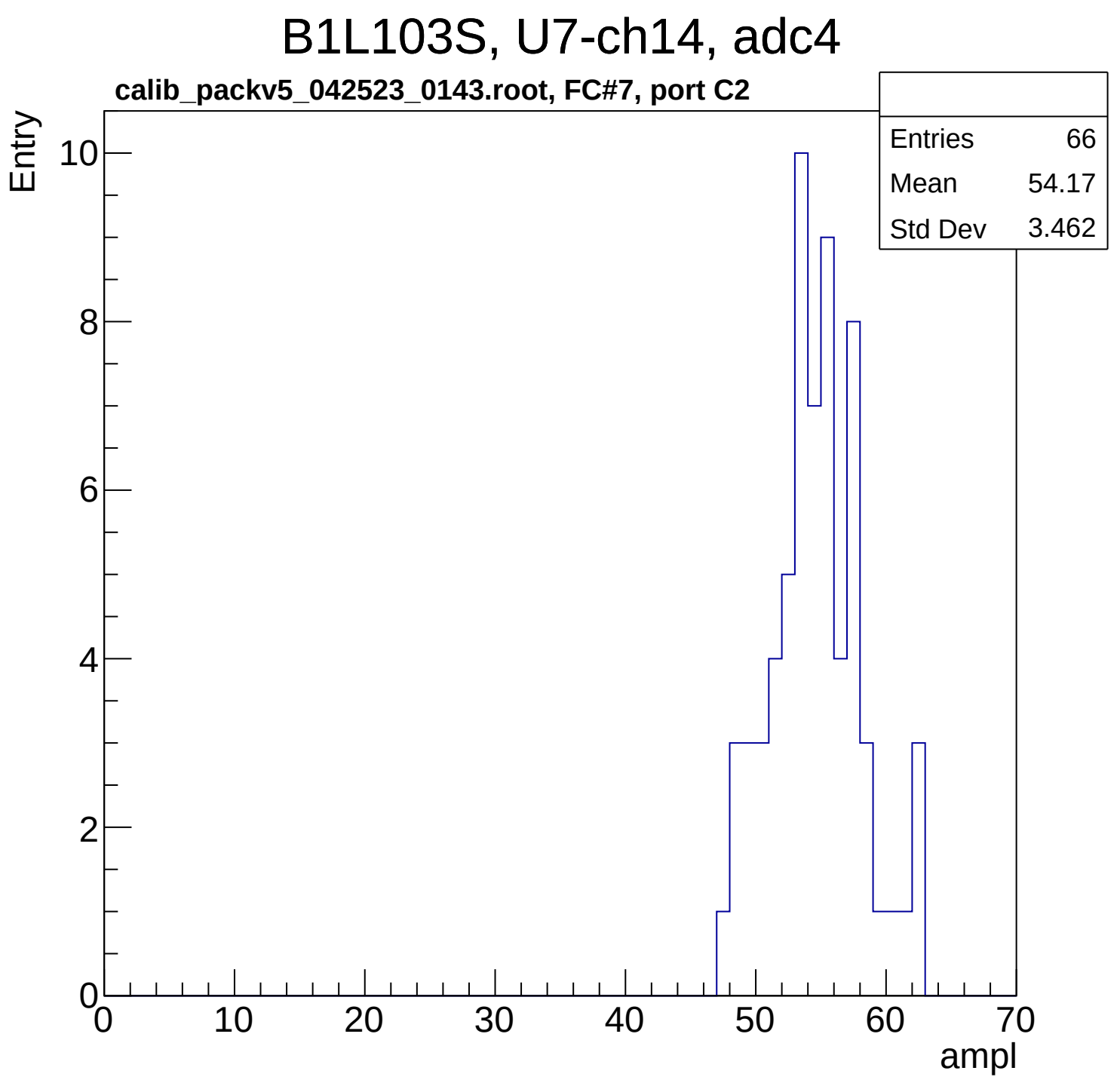

B1L103S, U7-ch13, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

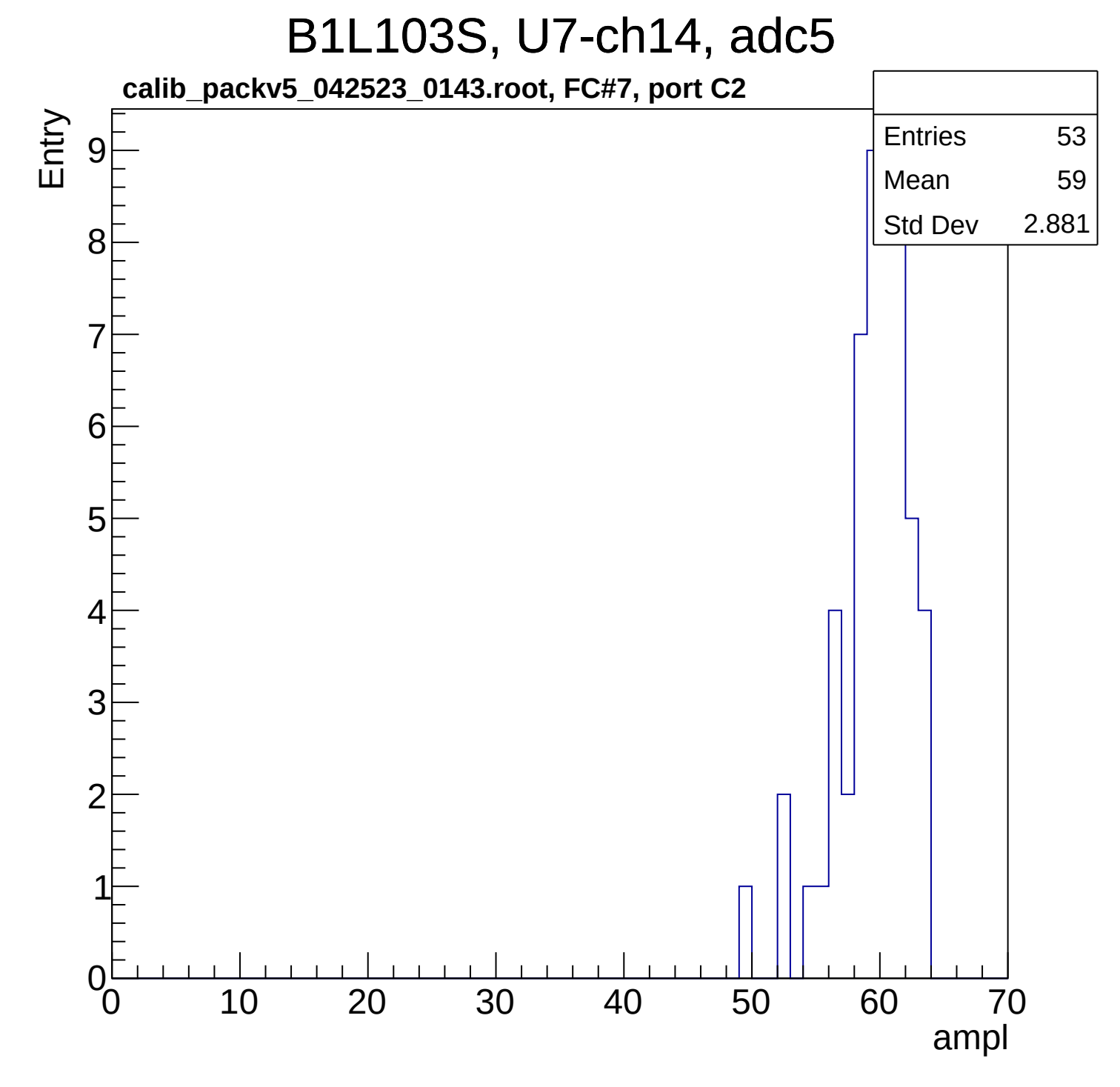

B1L103S, U7-ch14, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 28.62
Std Dev 6.431
Gaus mean : 31.3351
Gaus Width: 3.3062
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch14, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 35.67
Std Dev 3.966
Gaus mean : 36.5408
Gaus Width: 4.7883
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch14, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 42.34
Std Dev 3.034
Gaus mean : 43.4417
Gaus Width: 4.0752
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch14, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 48.3
Std Dev 3.172
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch14, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 54.17
Std Dev 3.462
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch14, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 59
Std Dev 2.881
Entry
ampl
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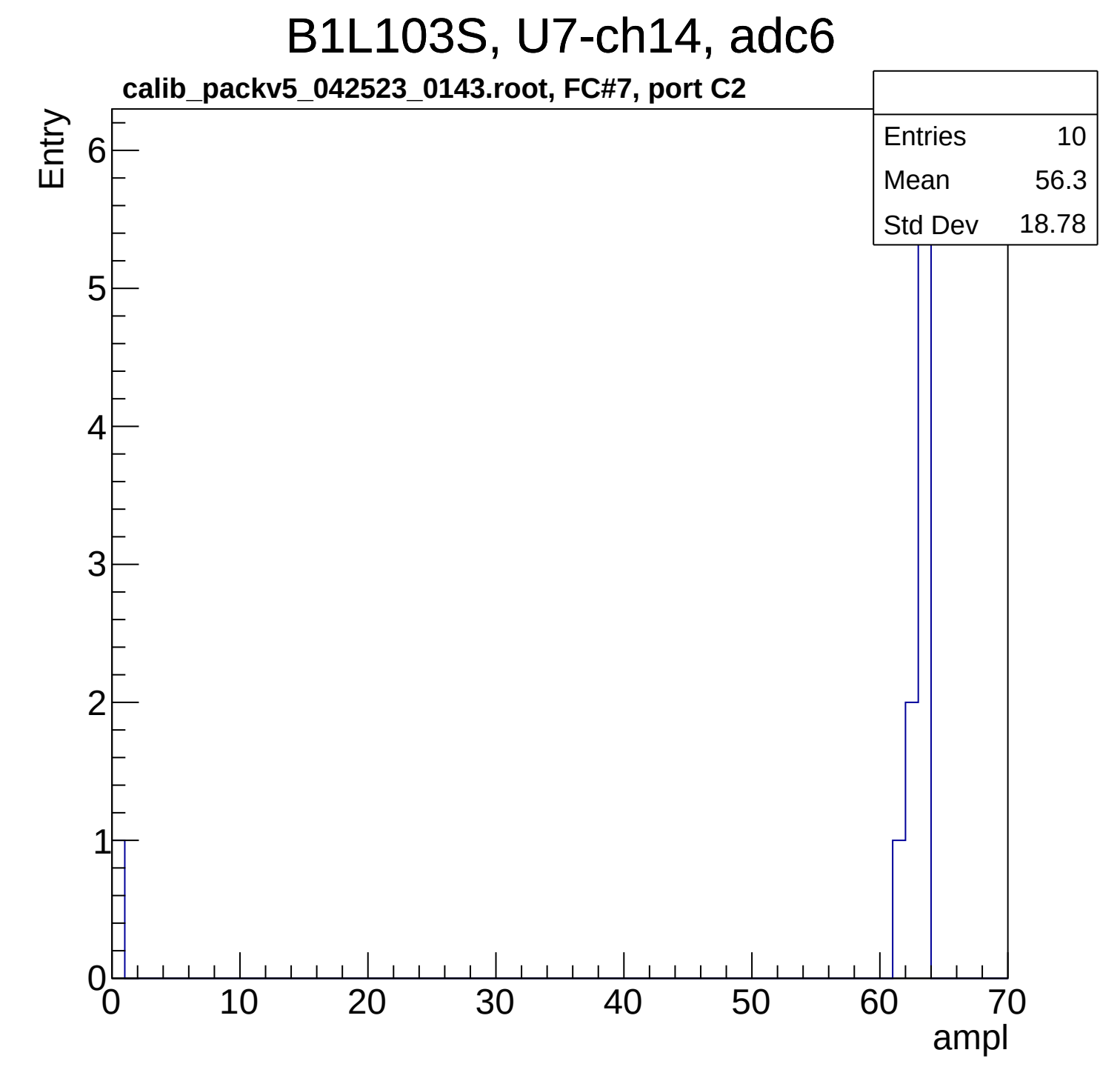
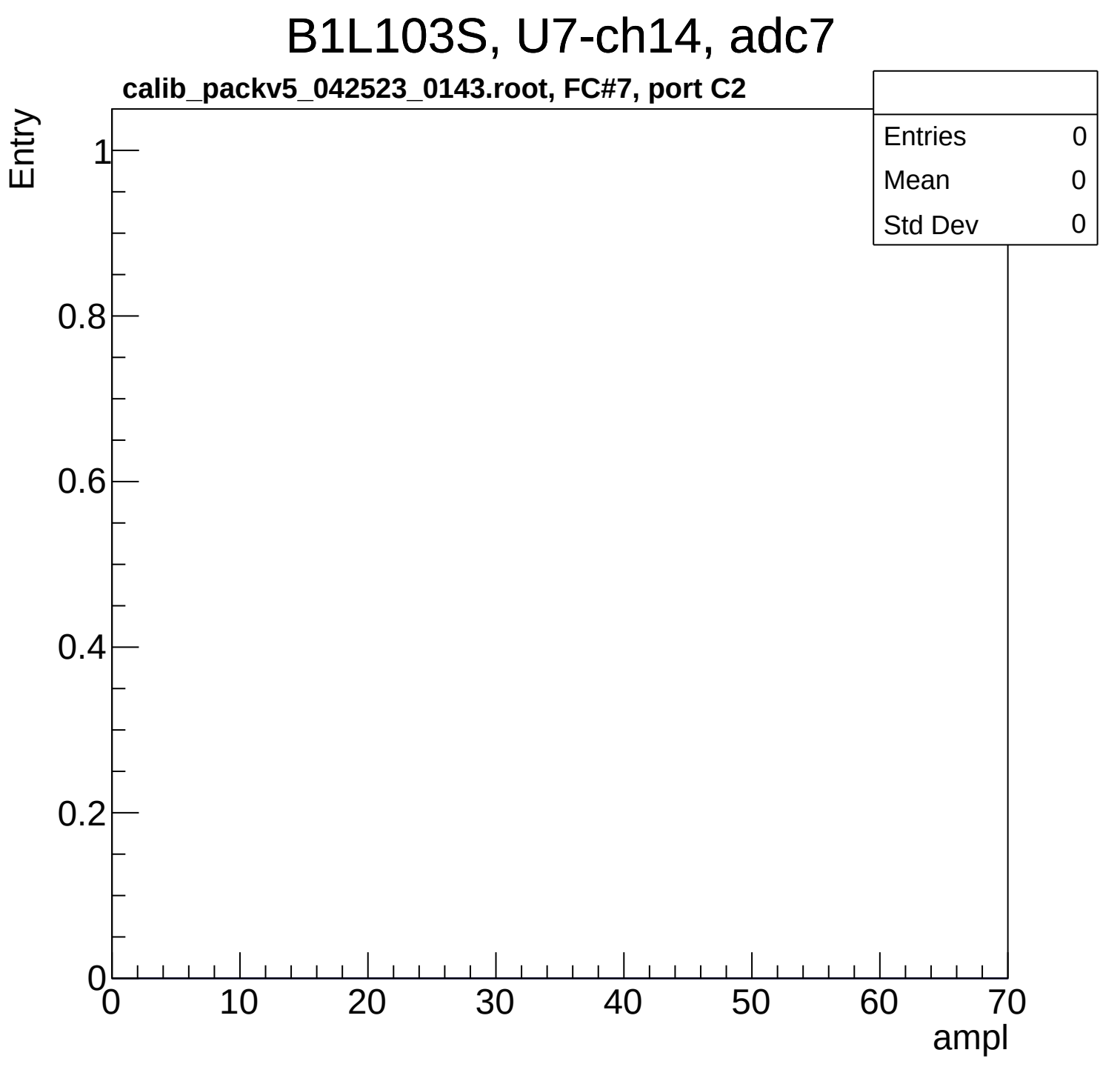
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch14, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 10
Mean 56.3
Std Dev 18.78
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch14, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
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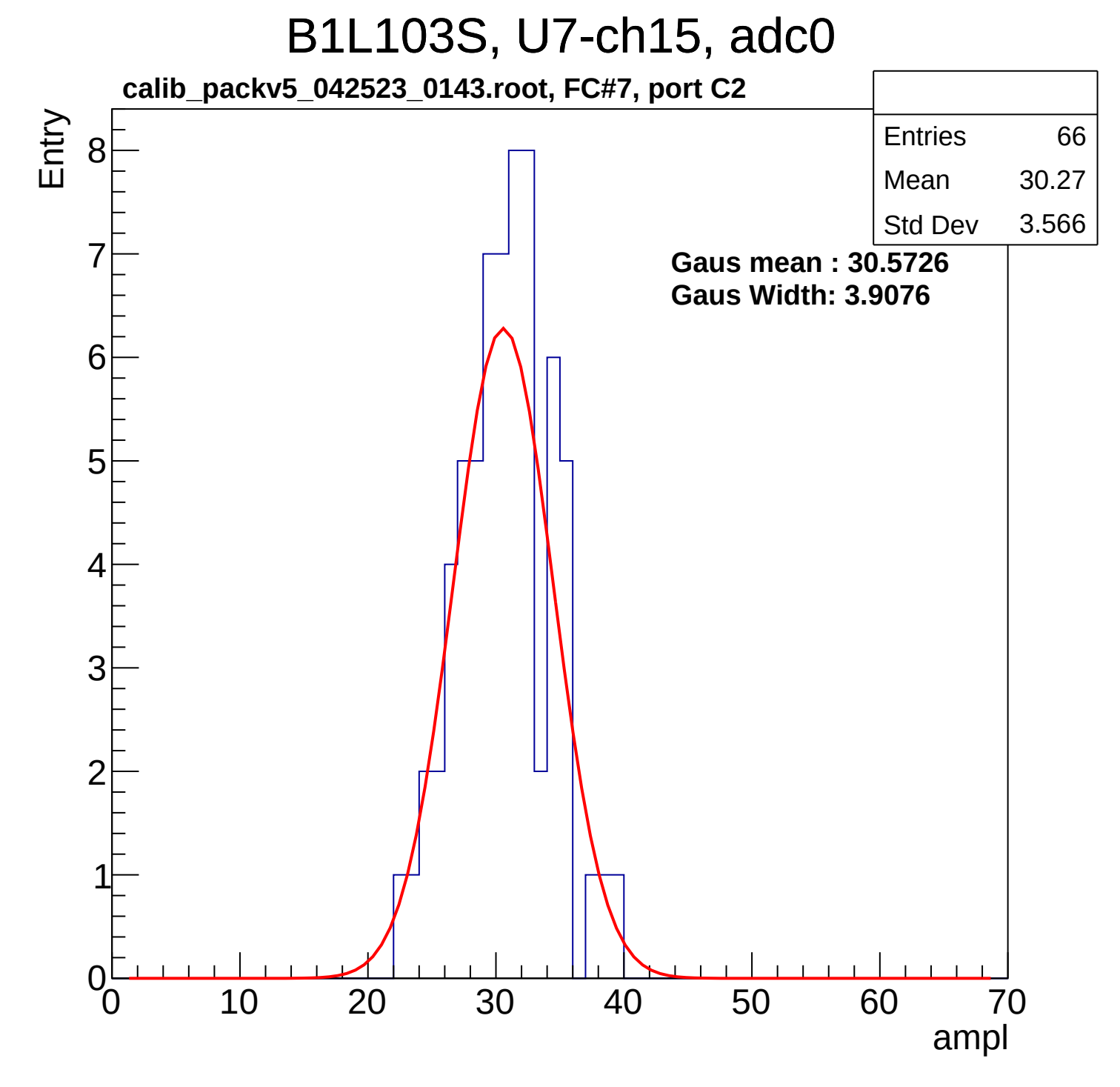
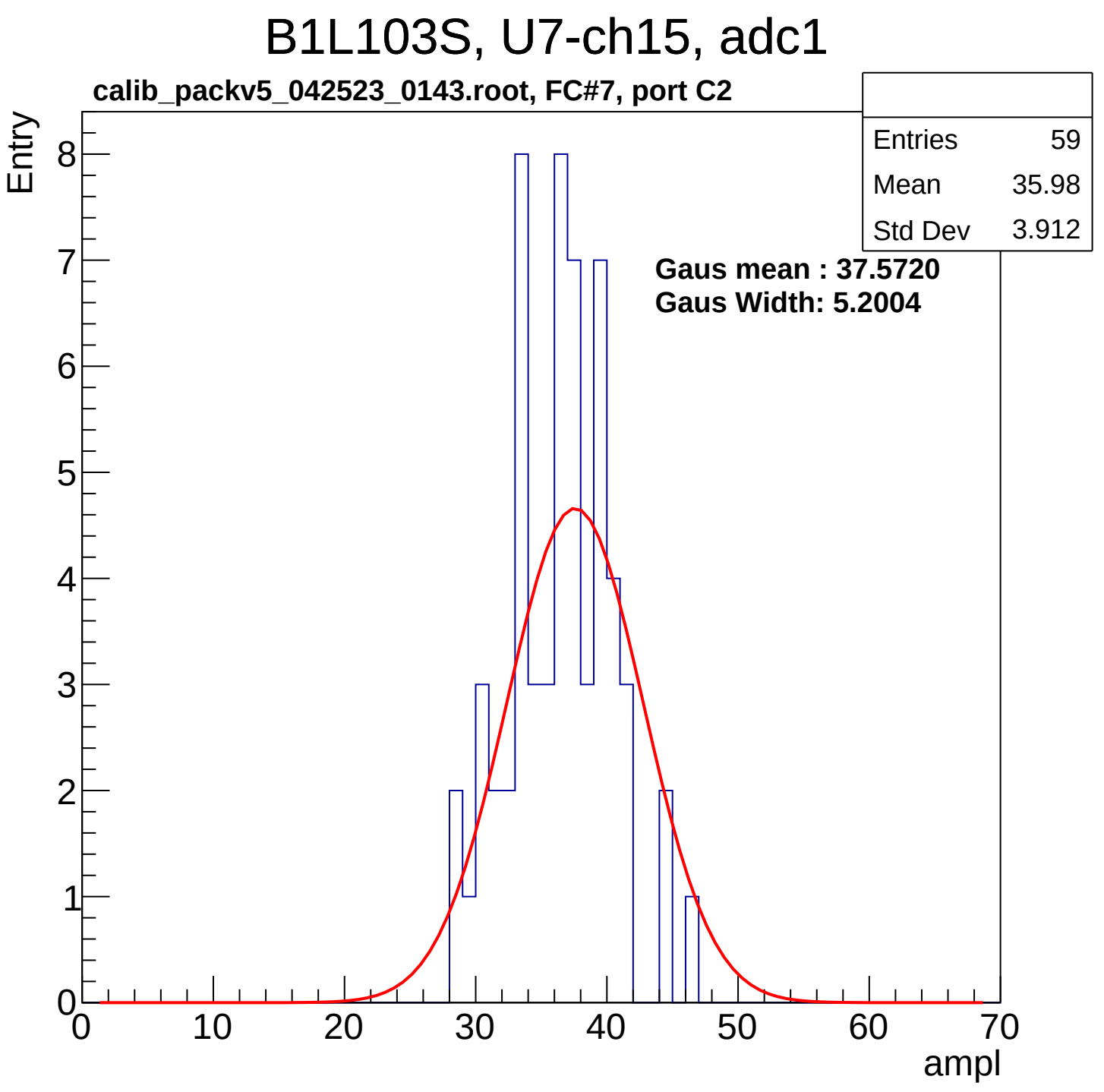
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch15, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 30.27
Std Dev 3.566
Gaus mean : 30.5726
Gaus Width: 3.9076
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch15, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 35.98
Std Dev 3.912
Gaus mean : 37.5720
Gaus Width: 5.2004
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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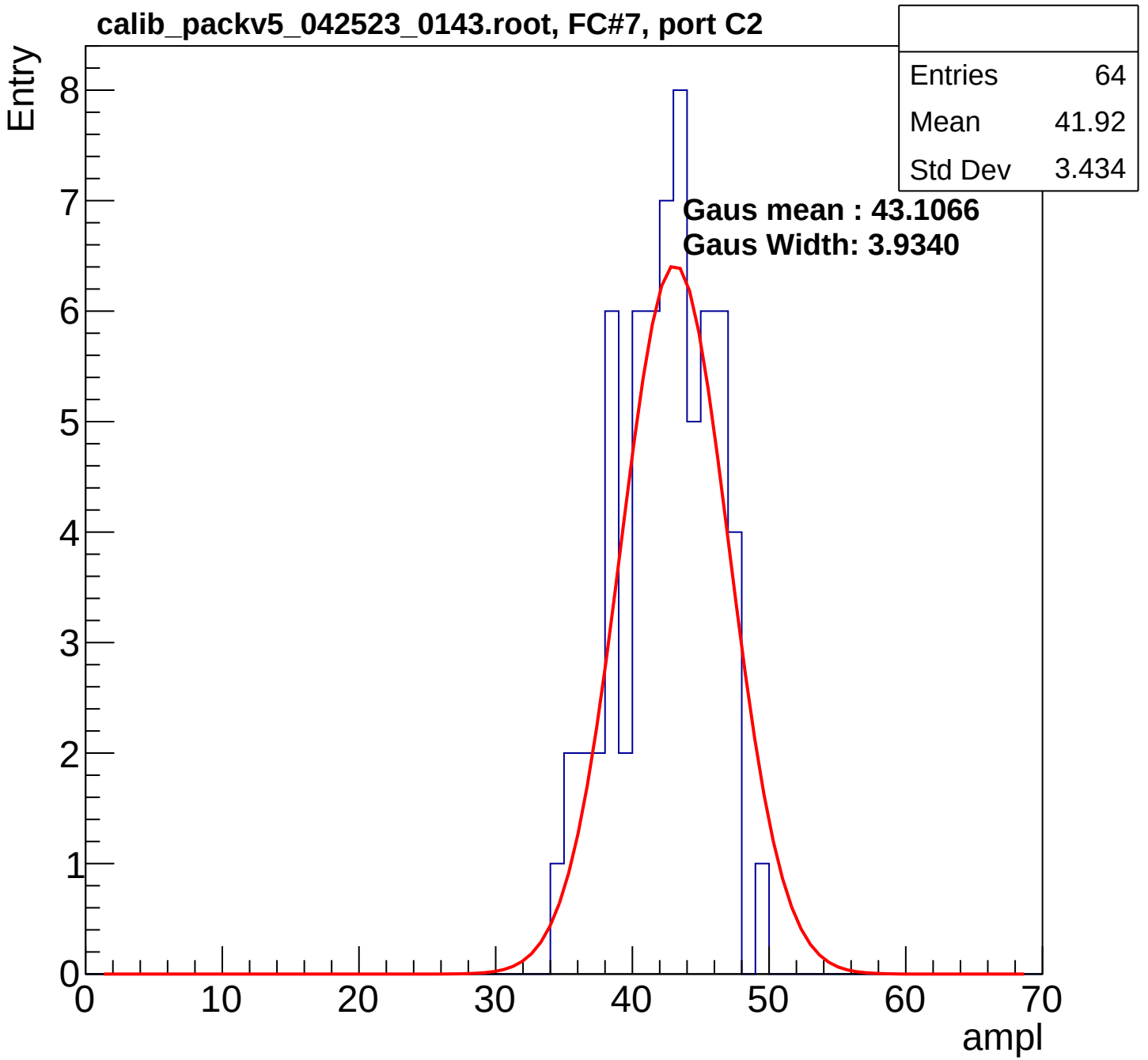
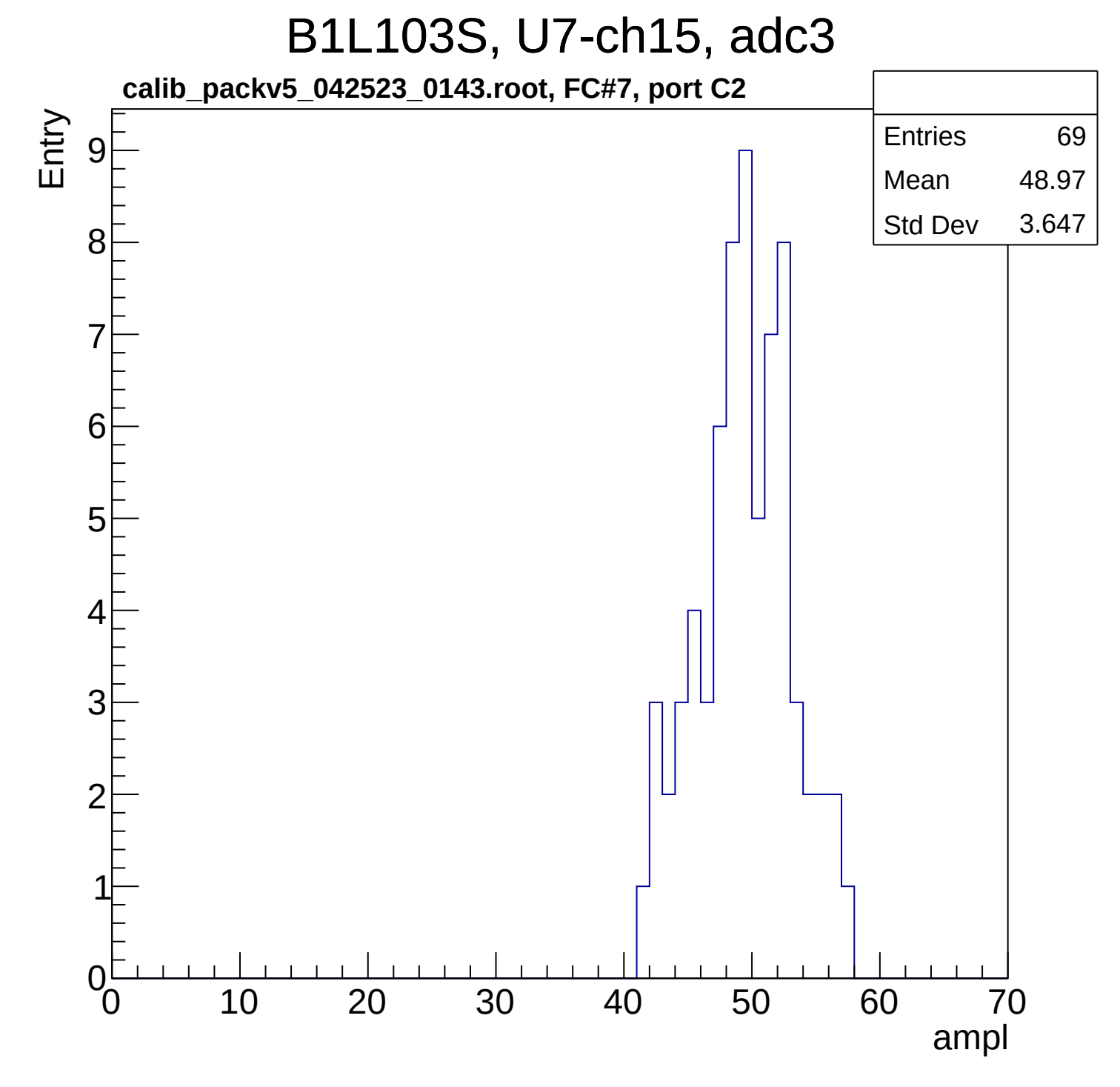

B1L103S, U7-ch15, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 41.92
Std Dev 3.434
Gaus mean : 43.1066
Gaus Width: 3.9340
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch15, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 48.97
Std Dev 3.647
Entry
ampl
0
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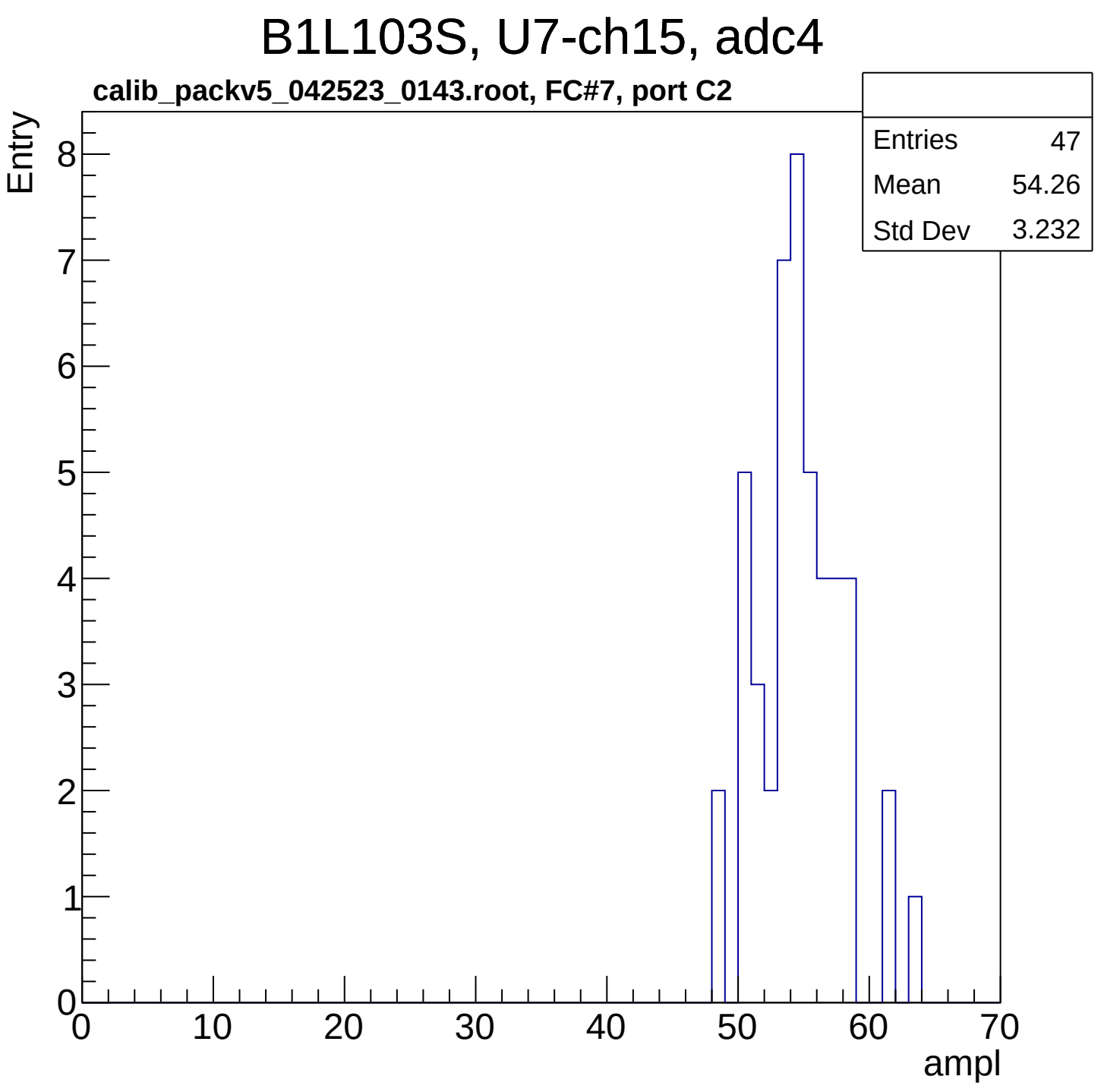
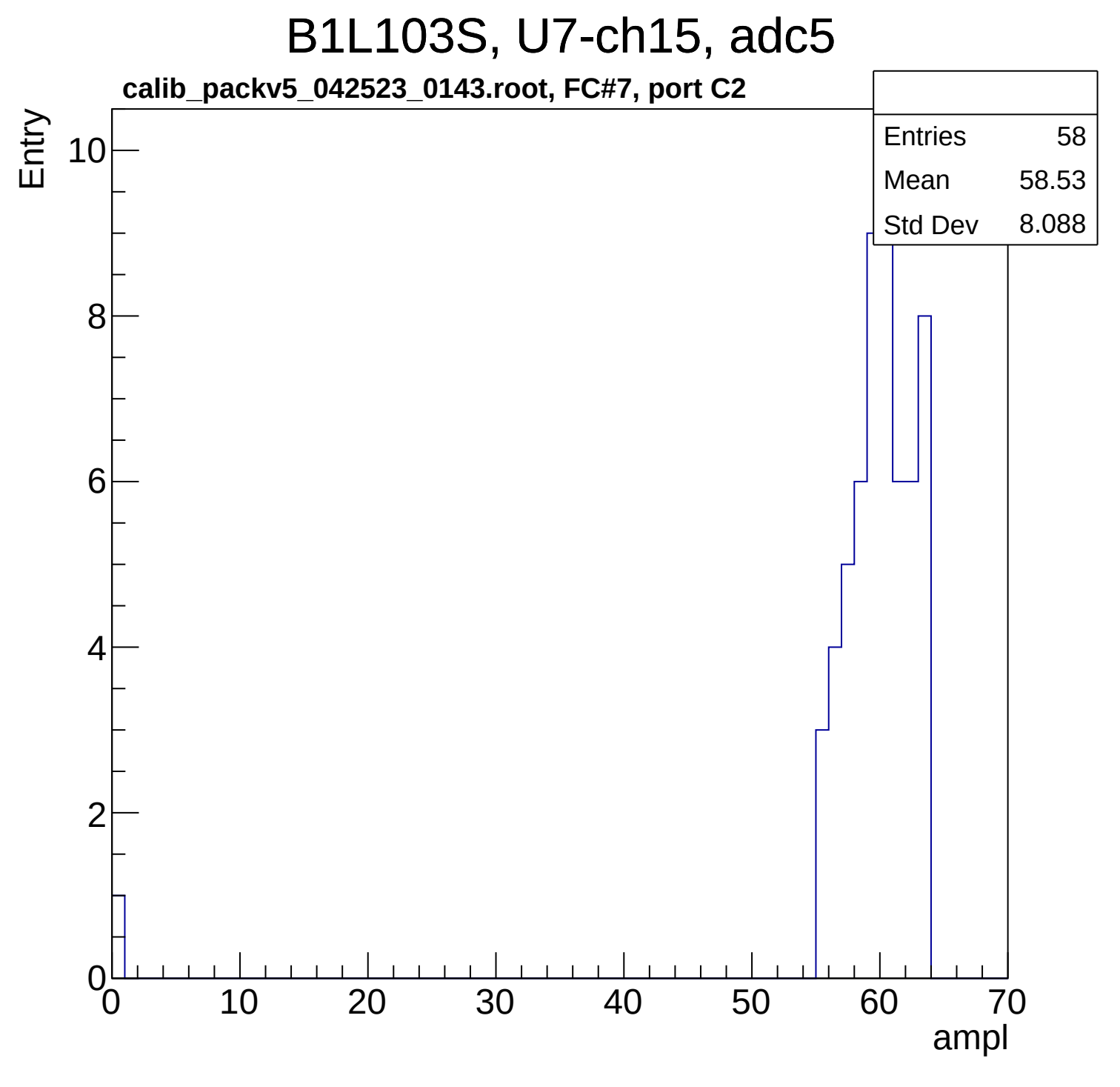
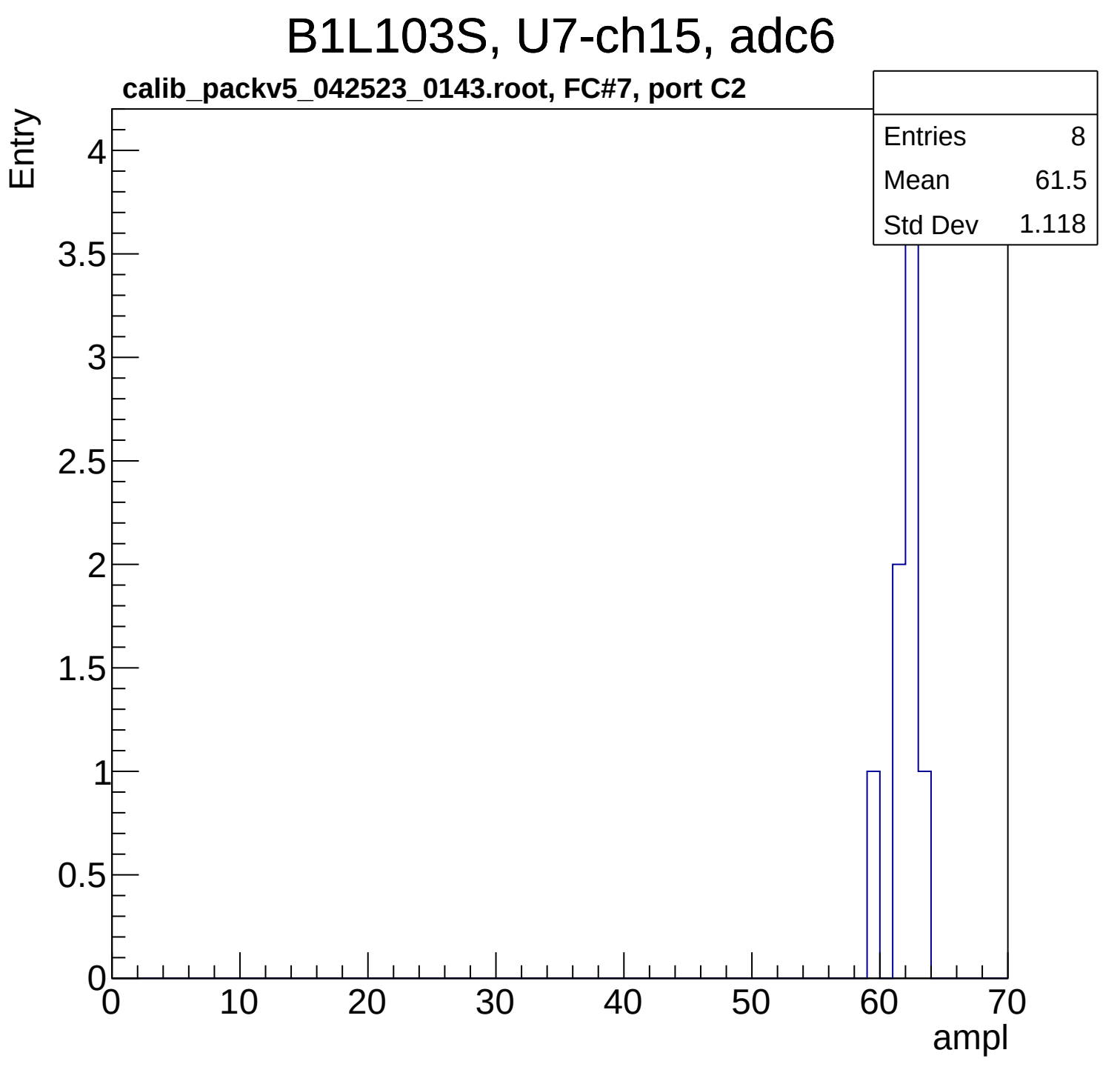
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch15, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 47
Mean 54.26
Std Dev 3.232
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch15, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 58
Mean 58.53
Std Dev 8.088
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch15, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 8
Mean 61.5
Std Dev 1.118
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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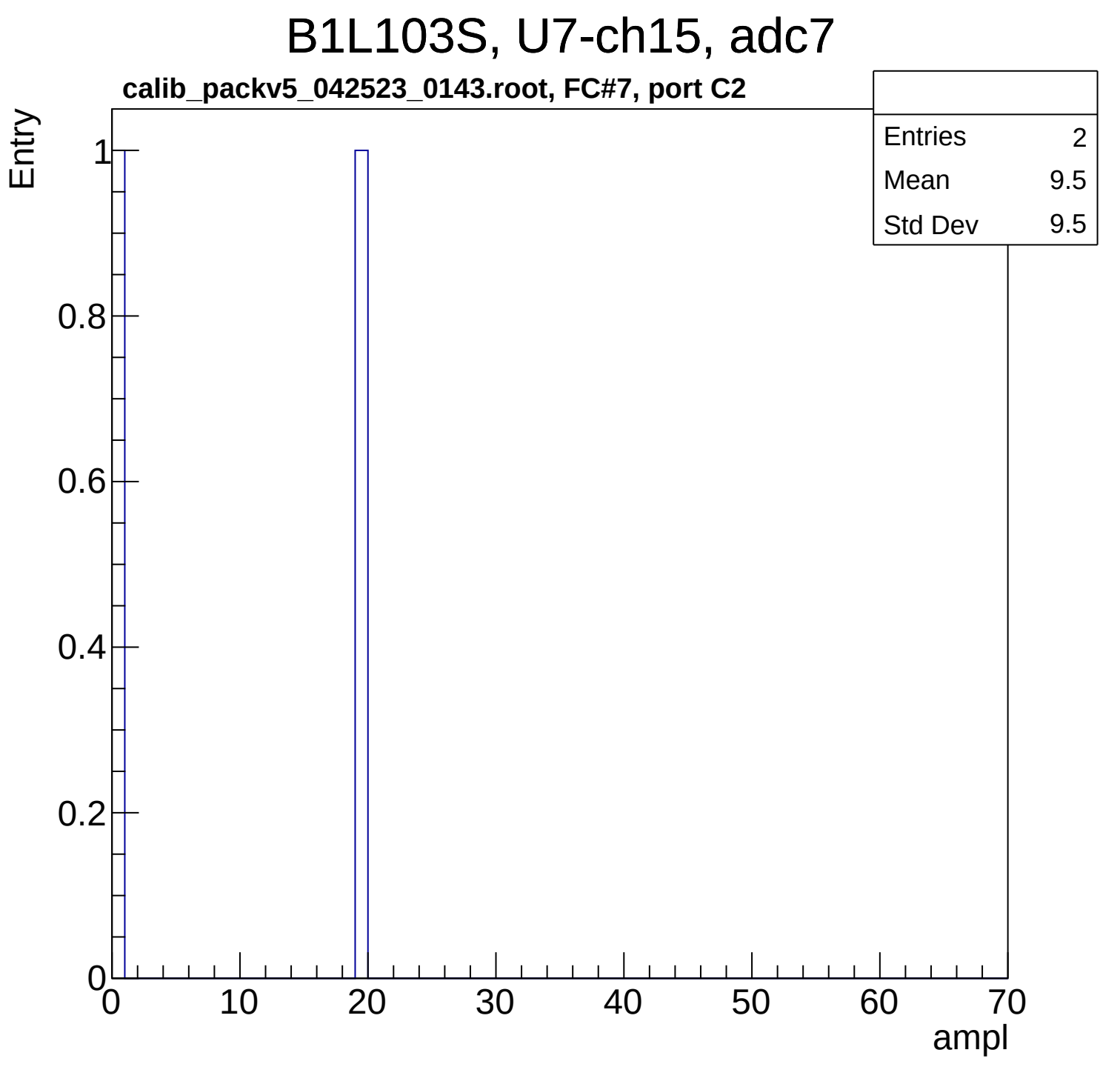
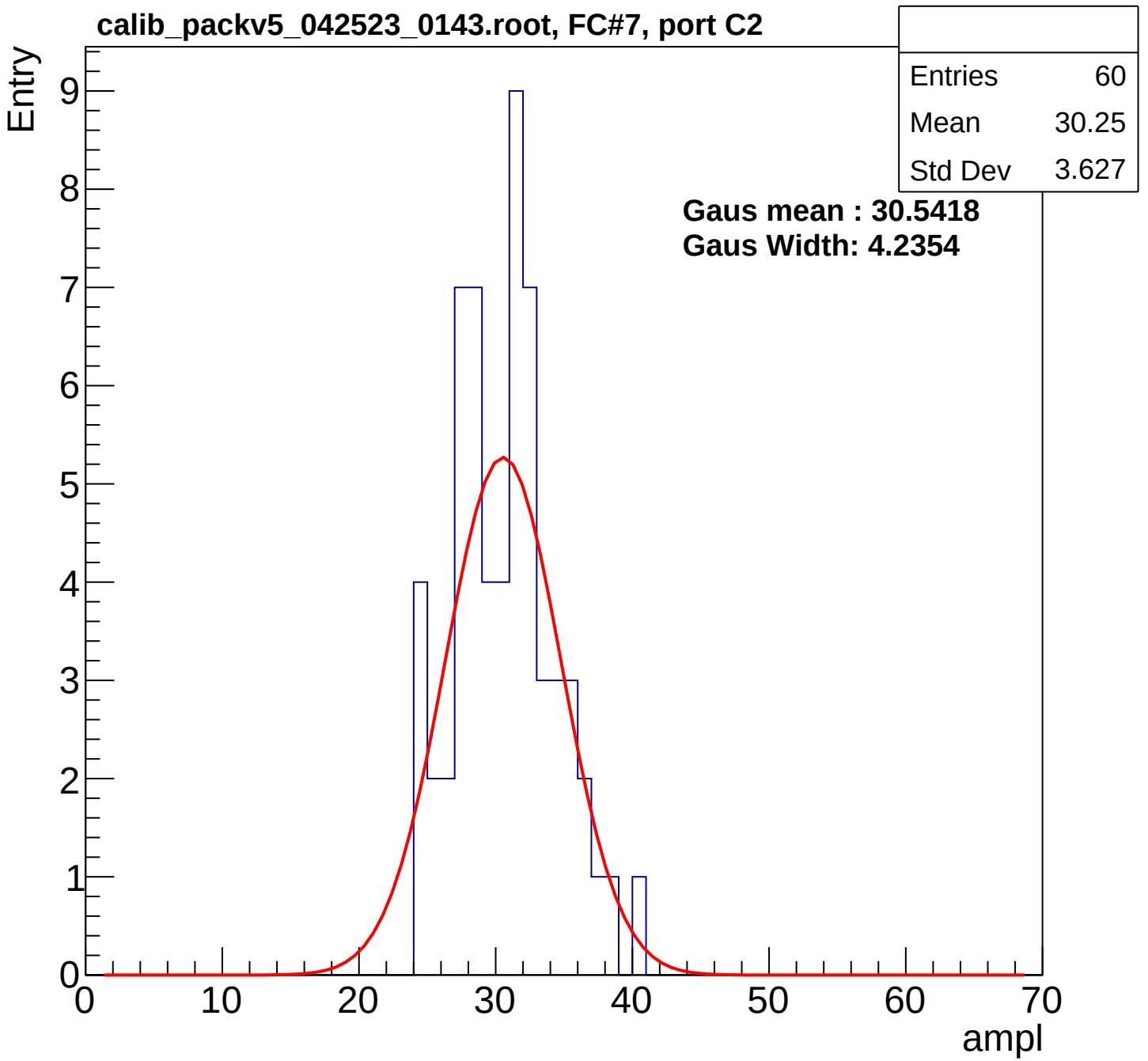
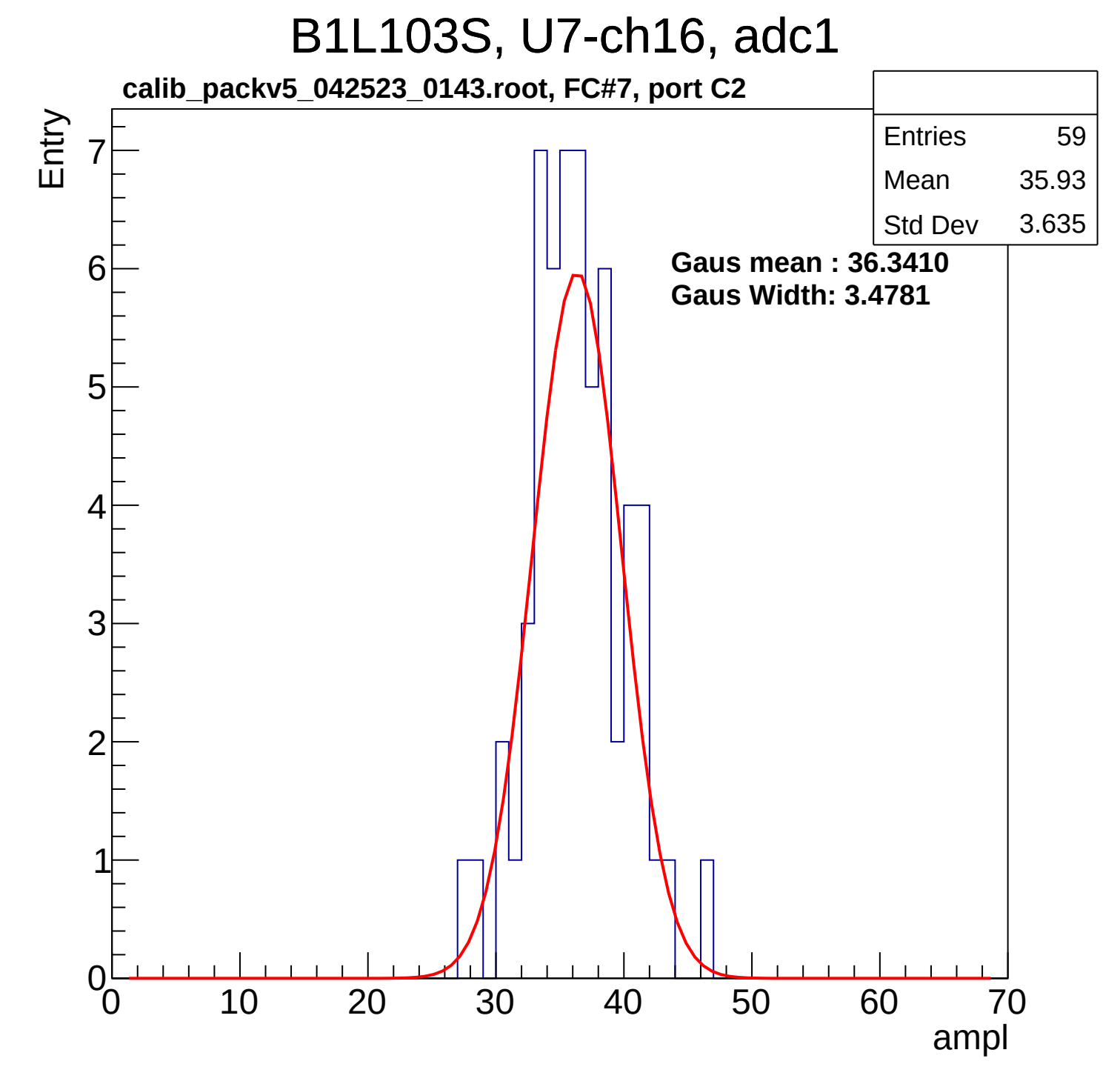
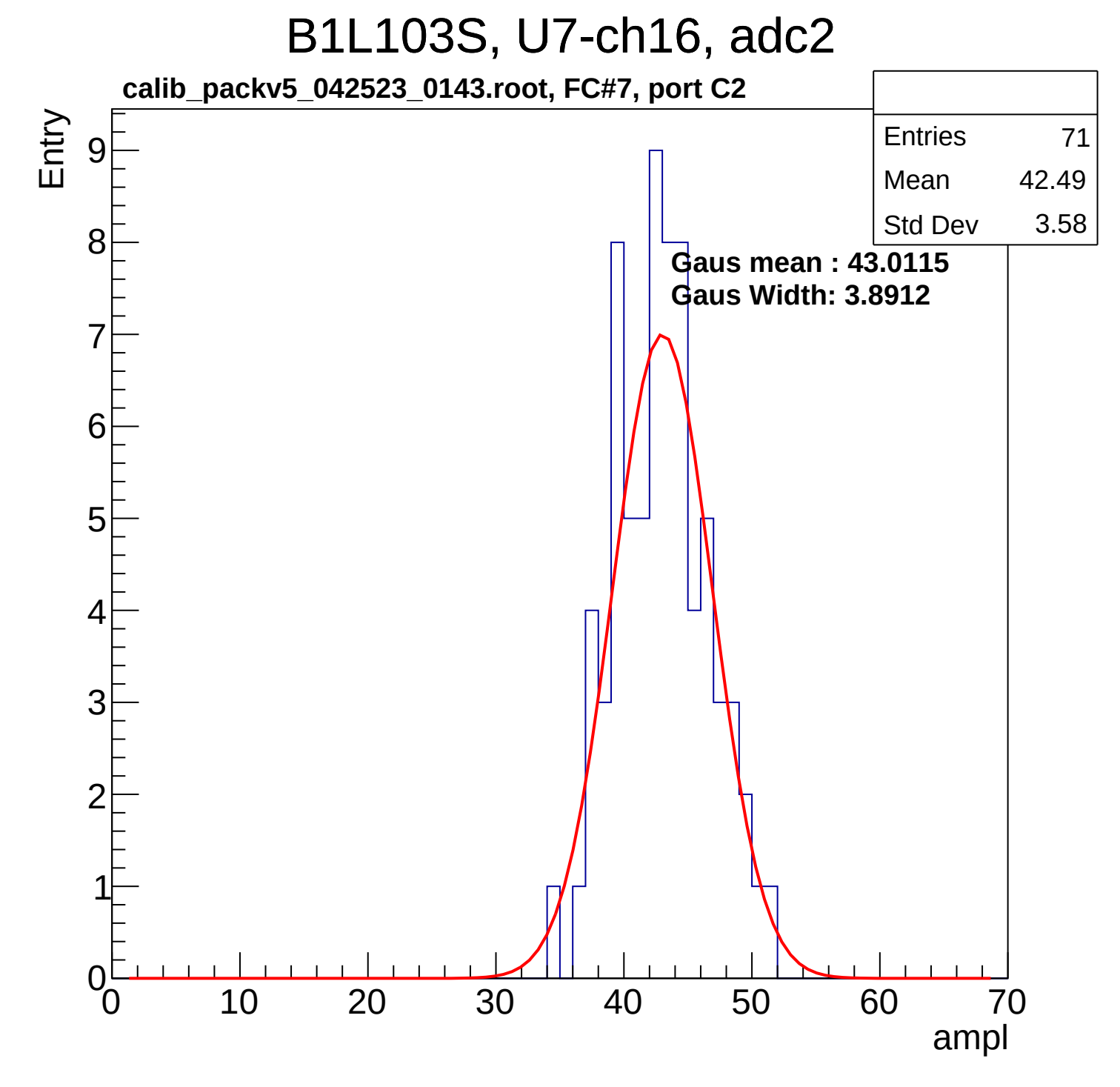
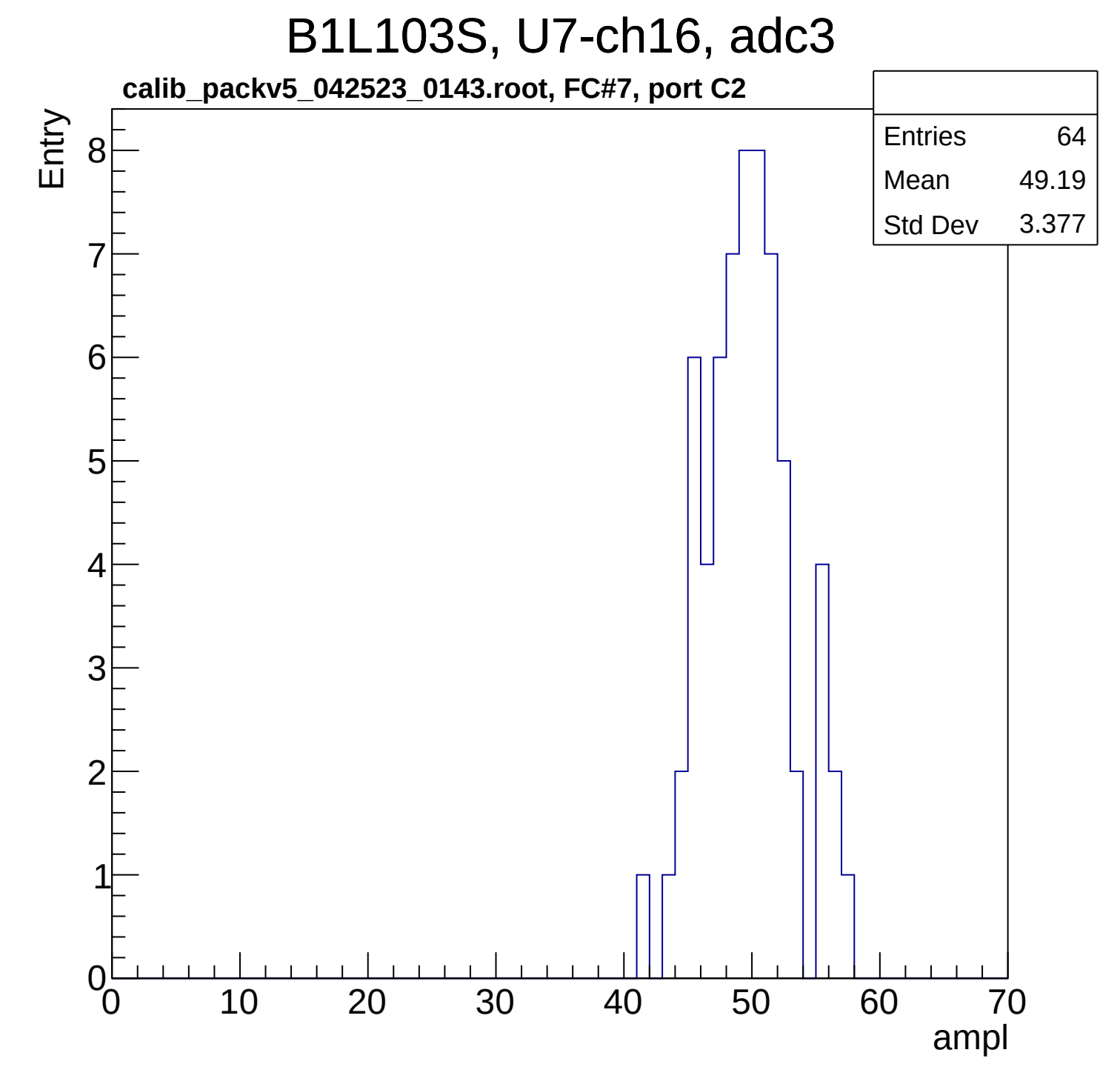
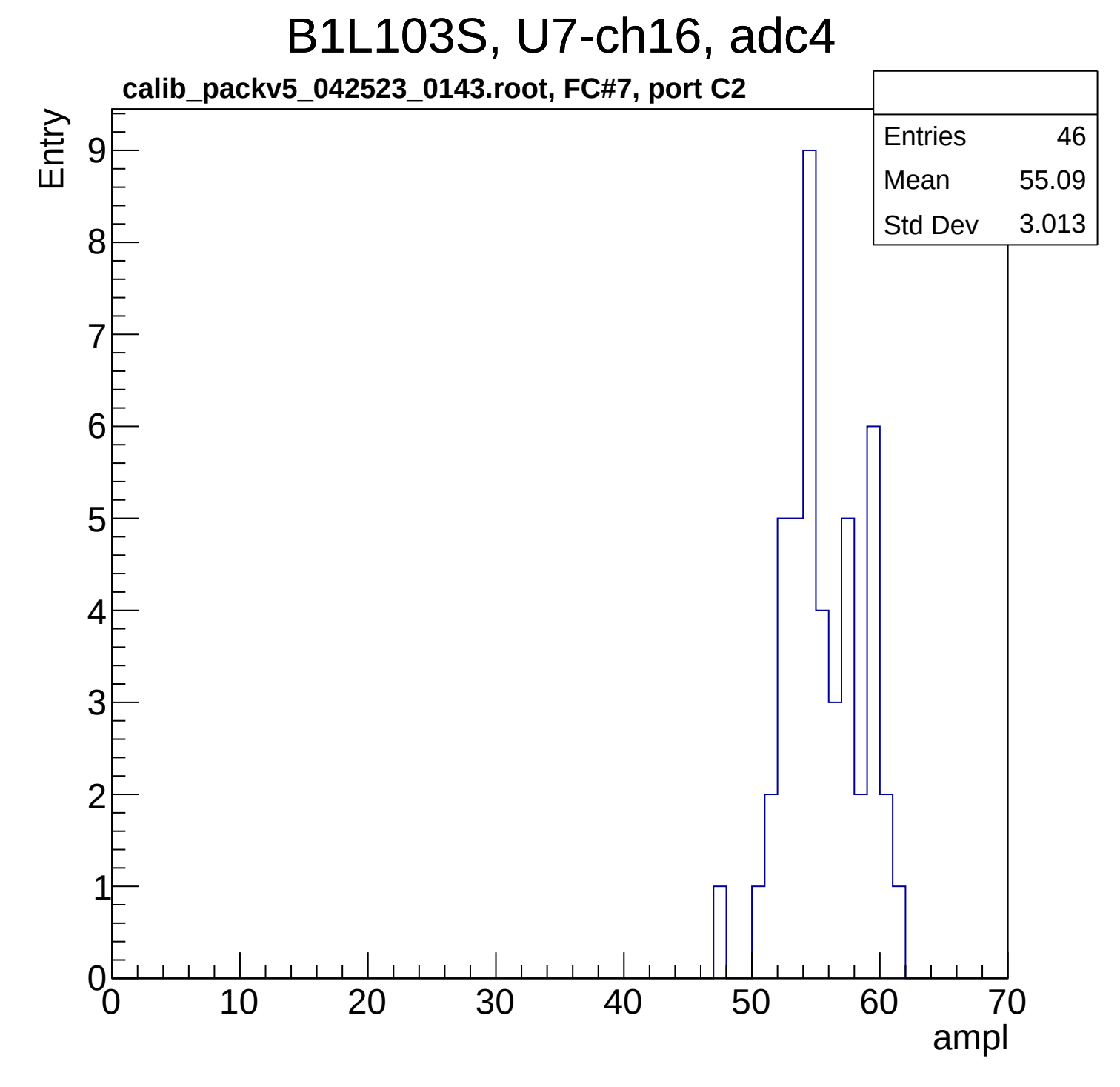

B1L103S, U7-ch15, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 9.5
Std Dev 9.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch16, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 60
Mean 30.25
Std Dev 3.627
Gaus mean : 30.5418
Gaus Width: 4.2354
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch16, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 35.93
Std Dev 3.635
Gaus mean : 36.3410
Gaus Width: 3.4781
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch16, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 71
Mean 42.49
Std Dev 3.58
Gaus mean : 43.0115
Gaus Width: 3.8912
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch16, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 49.19
Std Dev 3.377
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch16, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 46
Mean 55.09
Std Dev 3.013
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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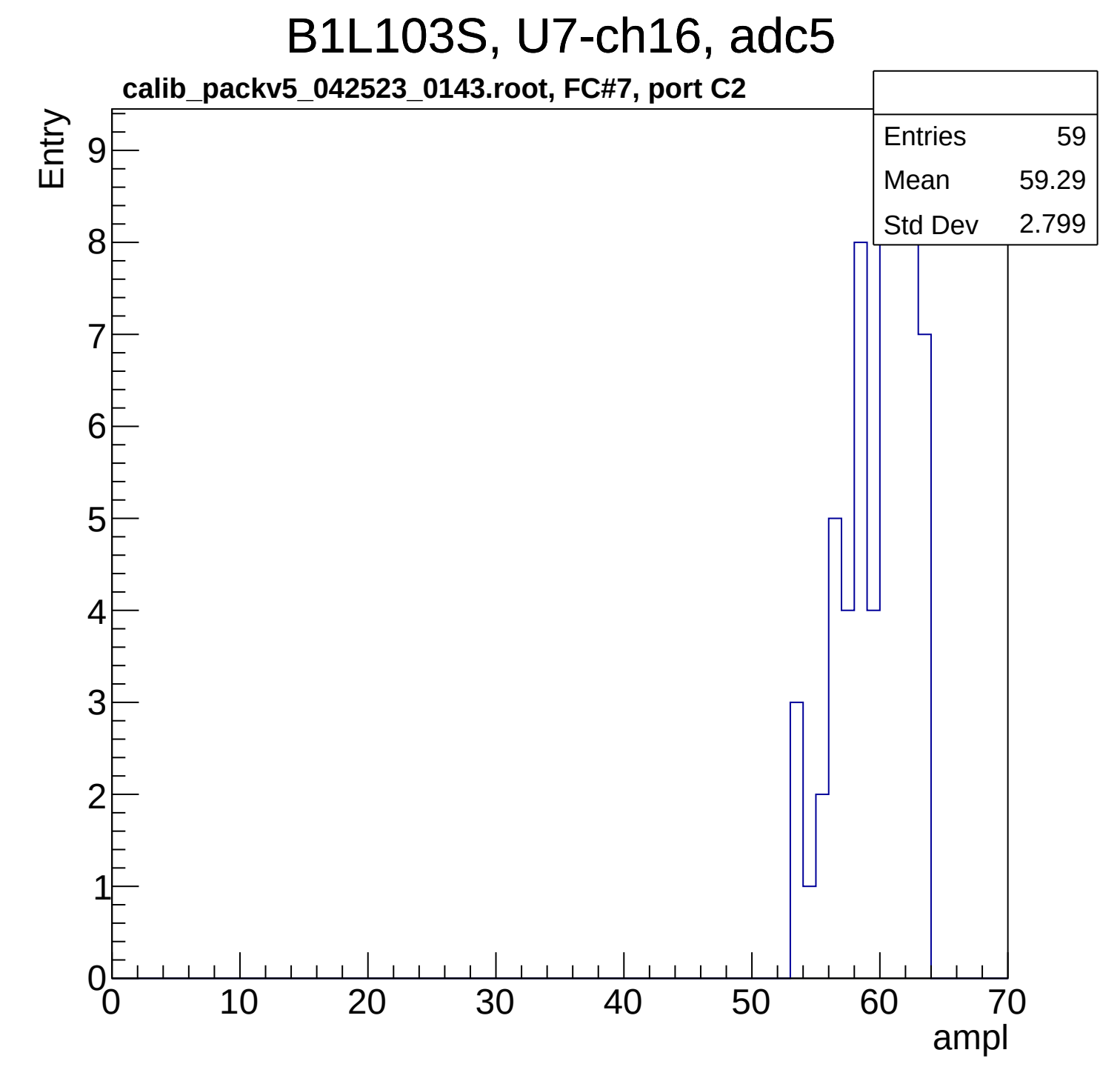
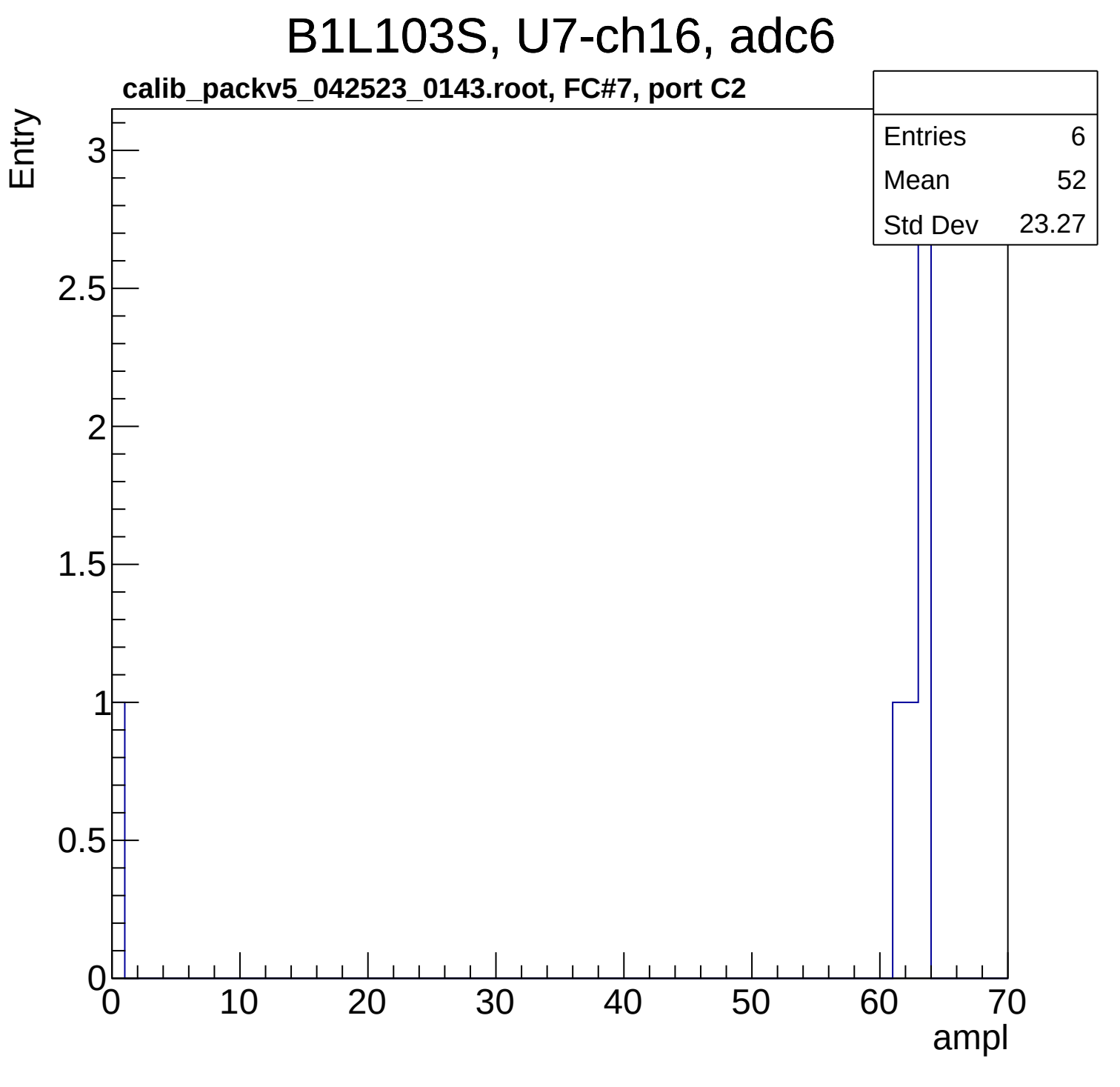
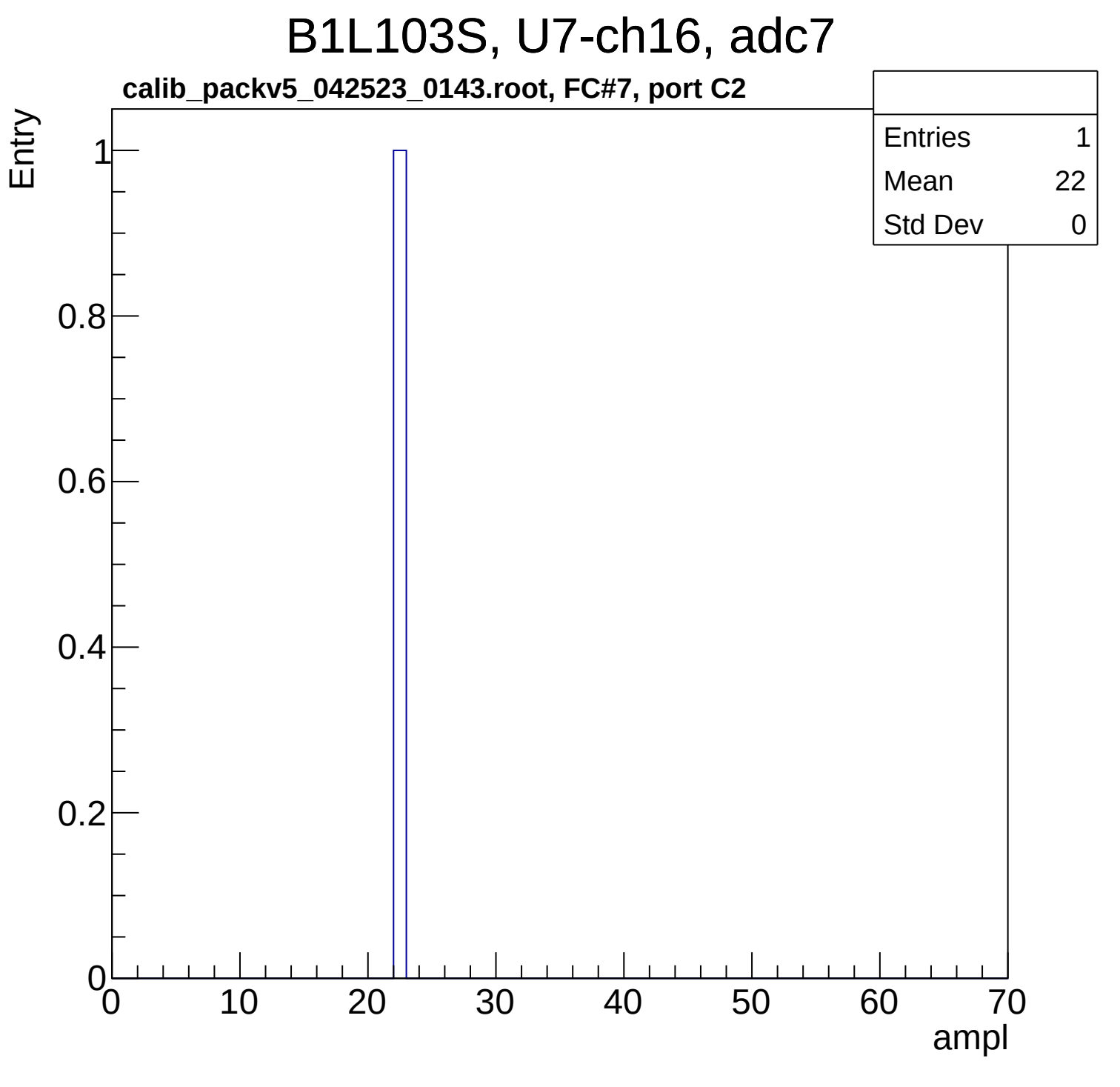
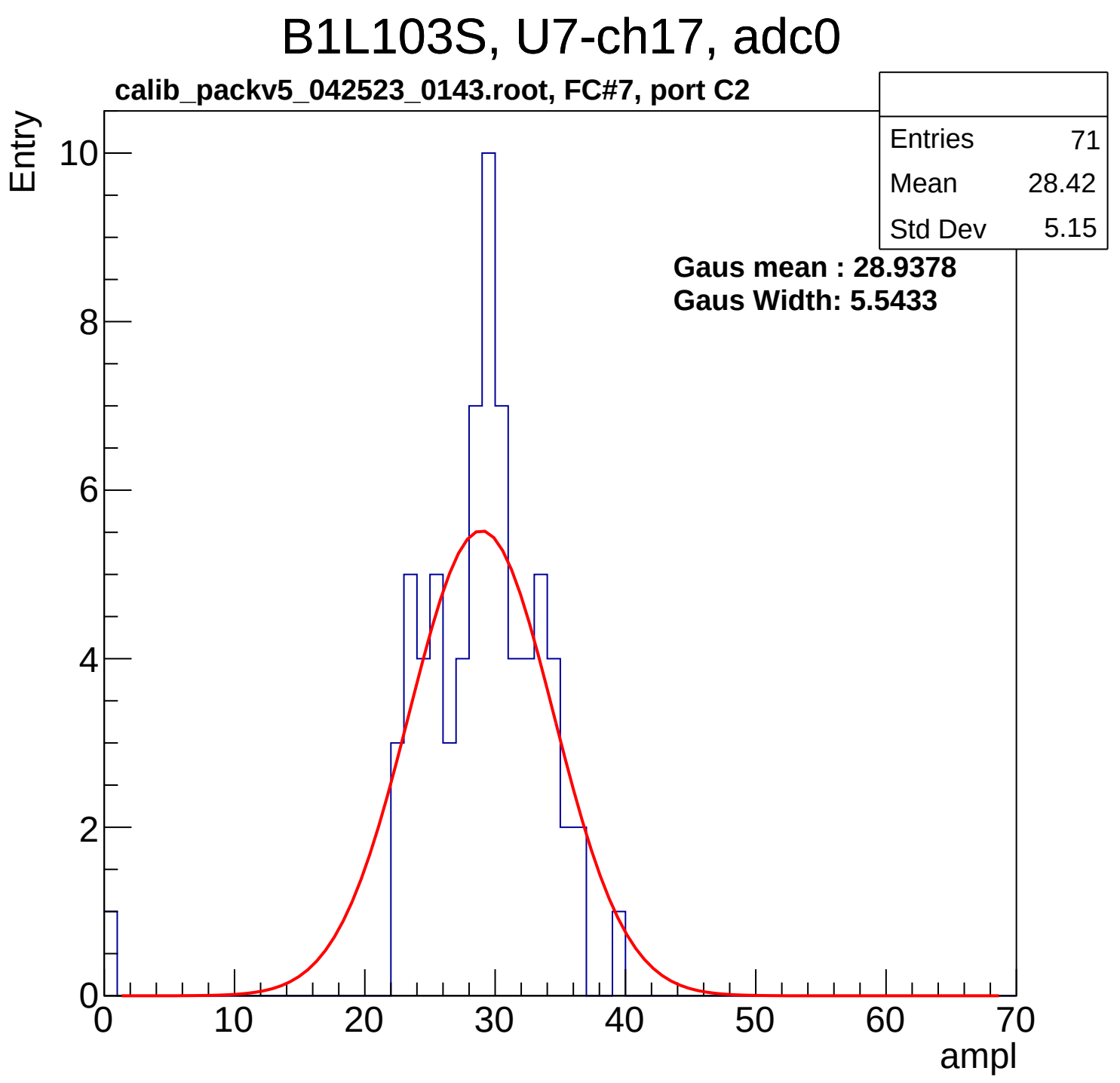
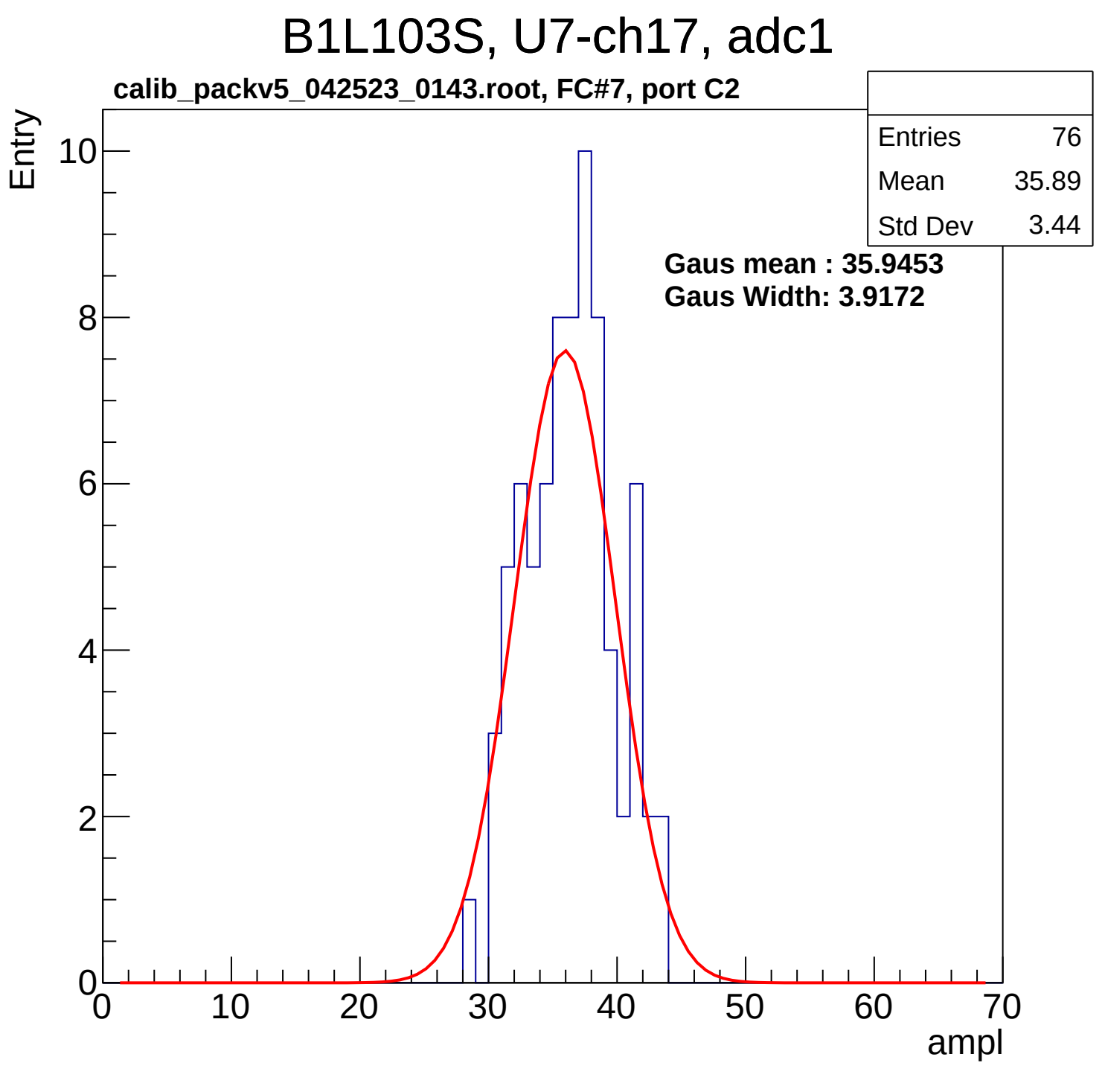
40
50
60
70

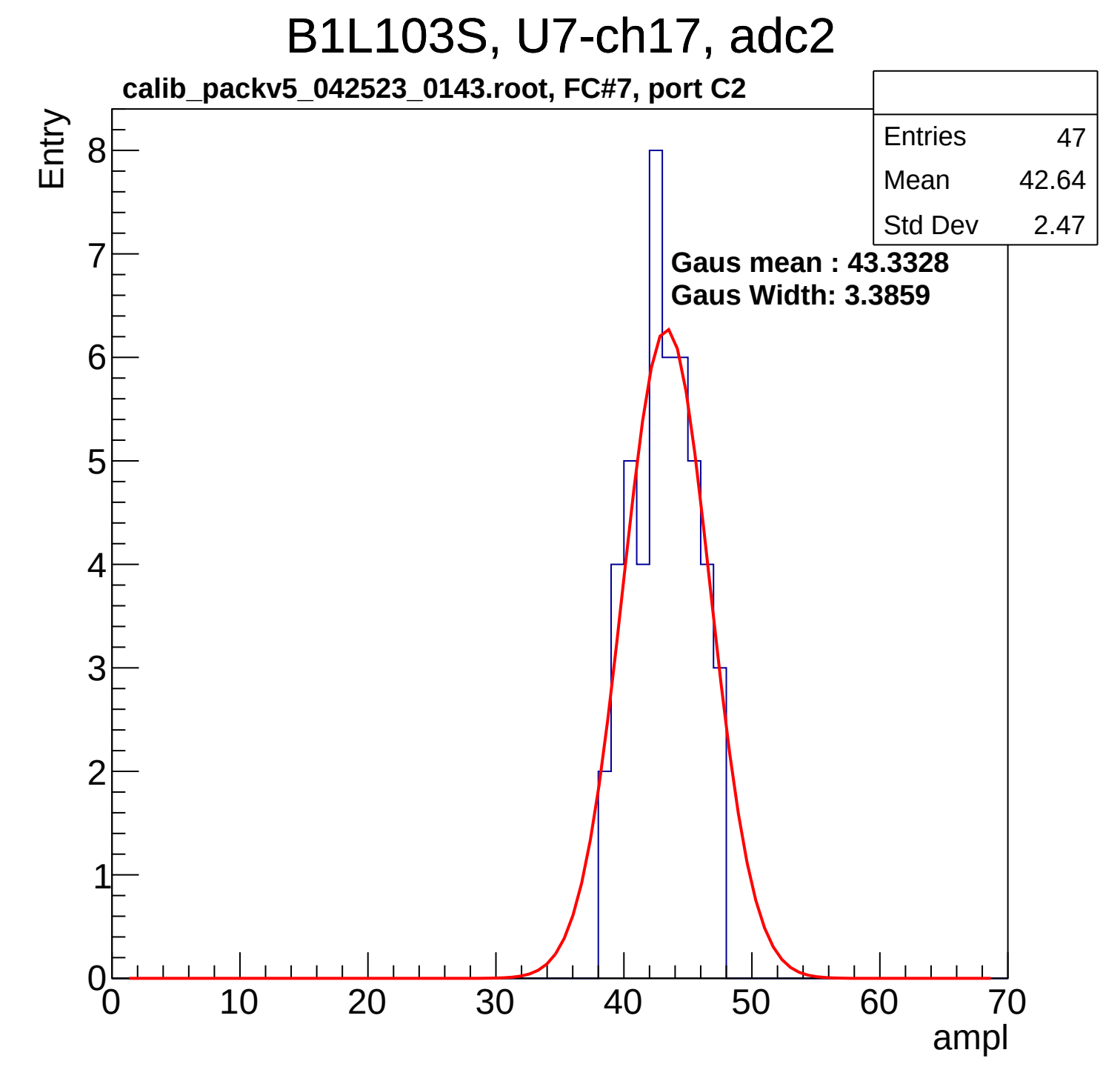

B1L103S, U7-ch16, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 59.29
Std Dev 2.799
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

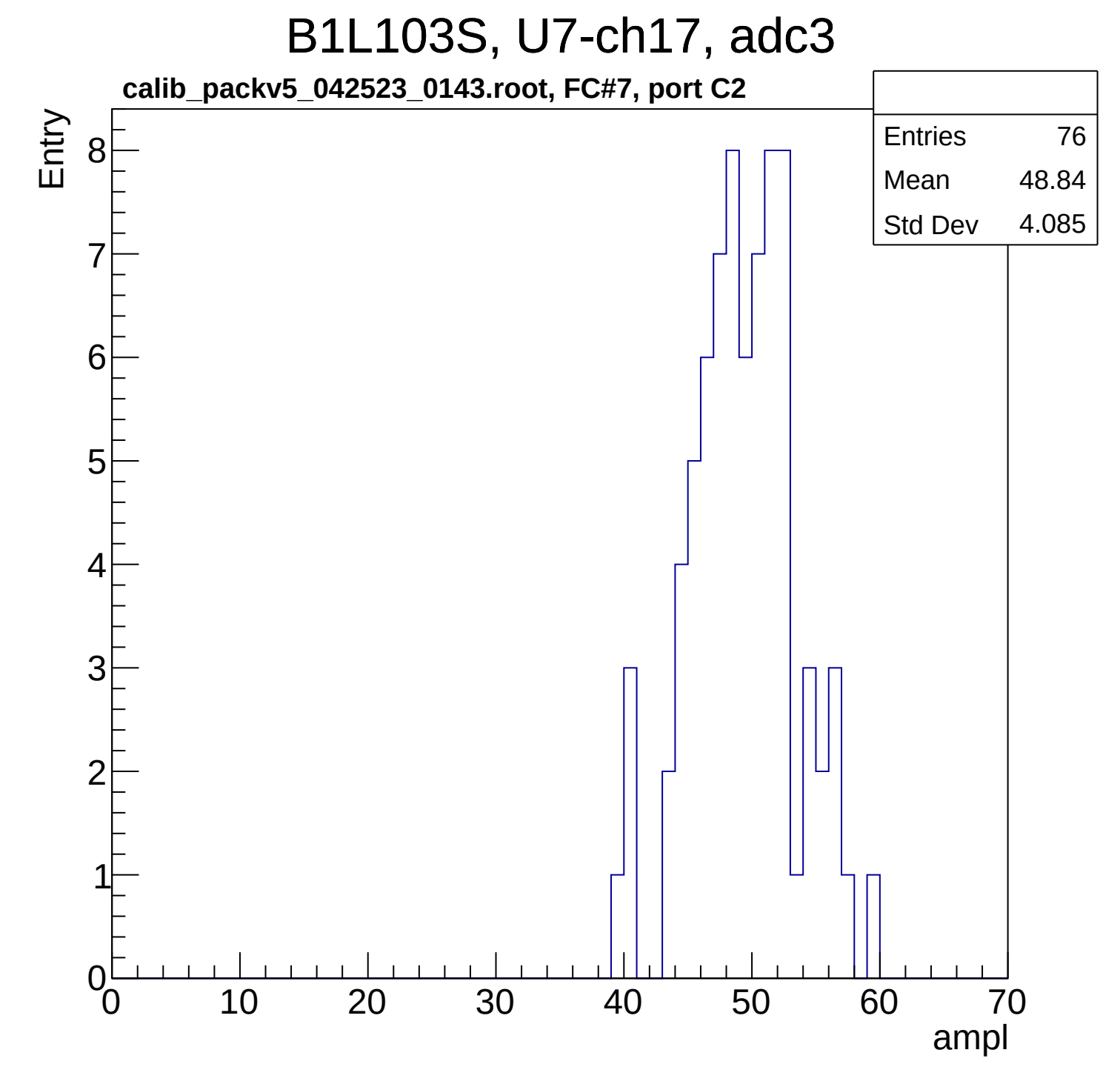

B1L103S, U7-ch16, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 6
Mean 52
Std Dev 23.27
Entry
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch16, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 22
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch17, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 71
Mean 28.42
Std Dev 5.15
Gaus mean : 28.9378
Gaus Width: 5.5433
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch17, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 76
Mean 35.89
Std Dev 3.44
Gaus mean : 35.9453
Gaus Width: 3.9172
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch17, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 47
Mean 42.64
Std Dev 2.47
Gaus mean : 43.3328
Gaus Width: 3.3859
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch17, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 76
Mean 48.84
Std Dev 4.085
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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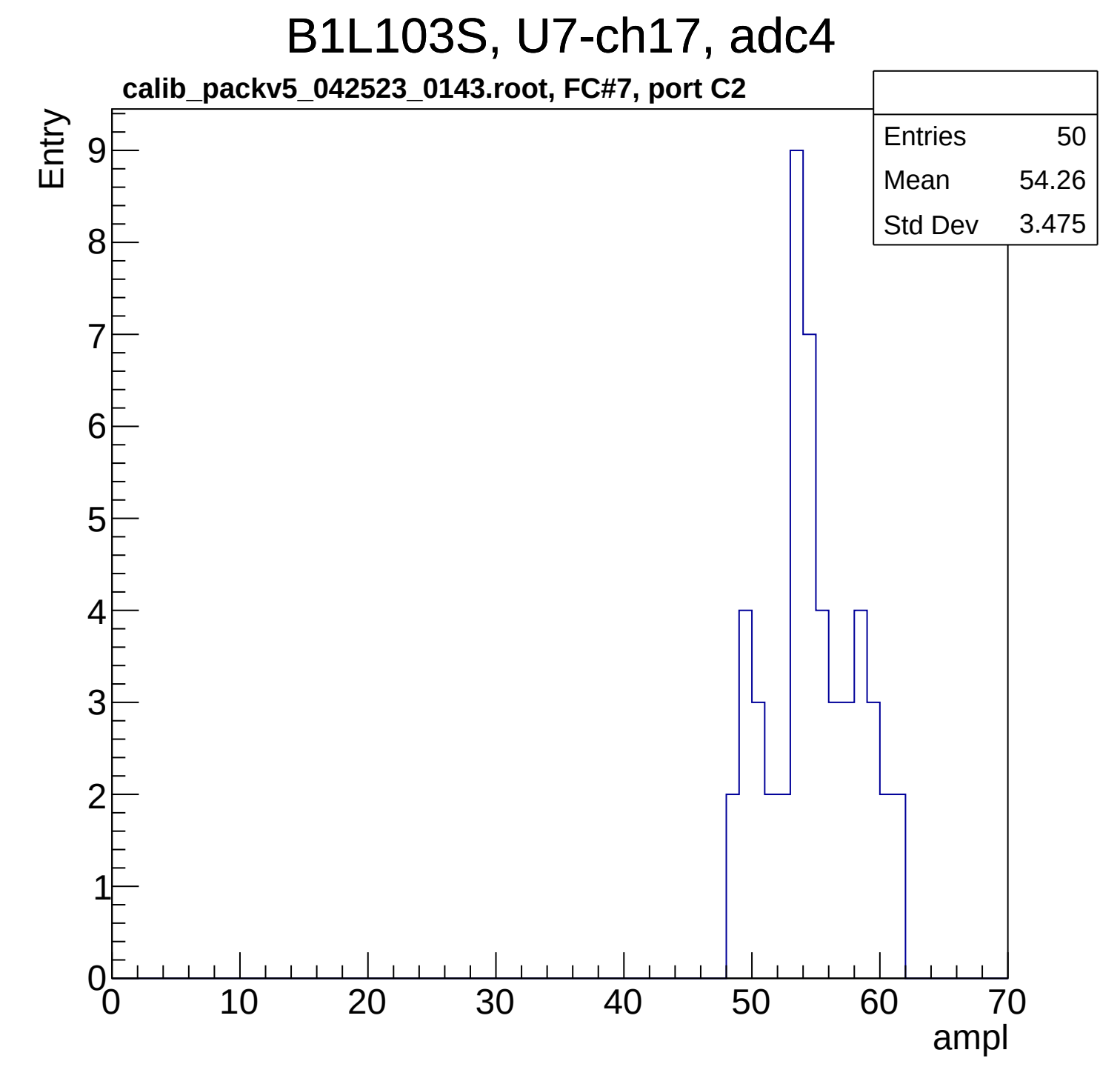
40
50
60
70


B1L103S, U7-ch17, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 50
Mean 54.26
Std Dev 3.475
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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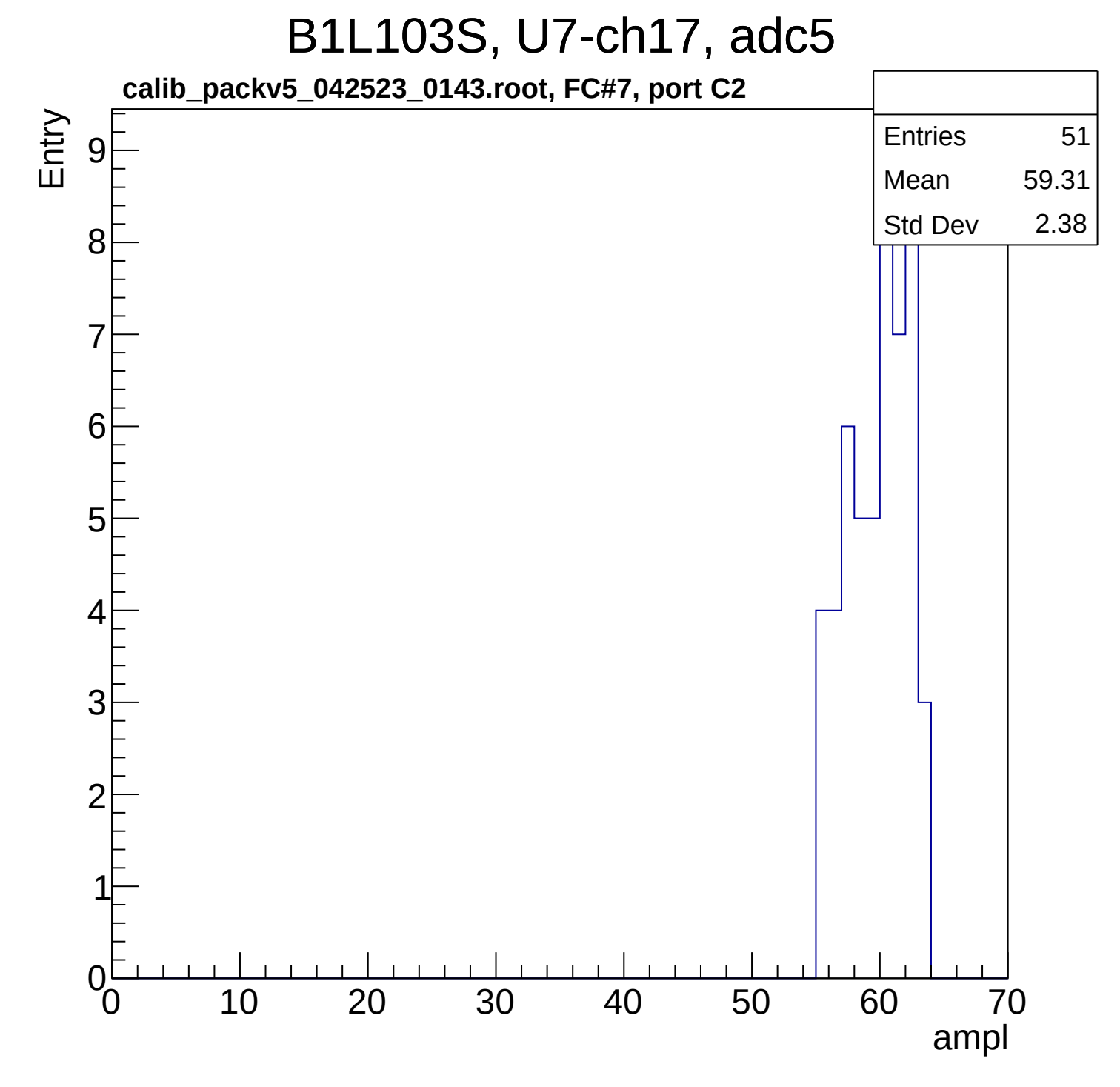
40
50
60
70


B1L103S, U7-ch17, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 51
Mean 59.31
Std Dev 2.38
Entry
ampl
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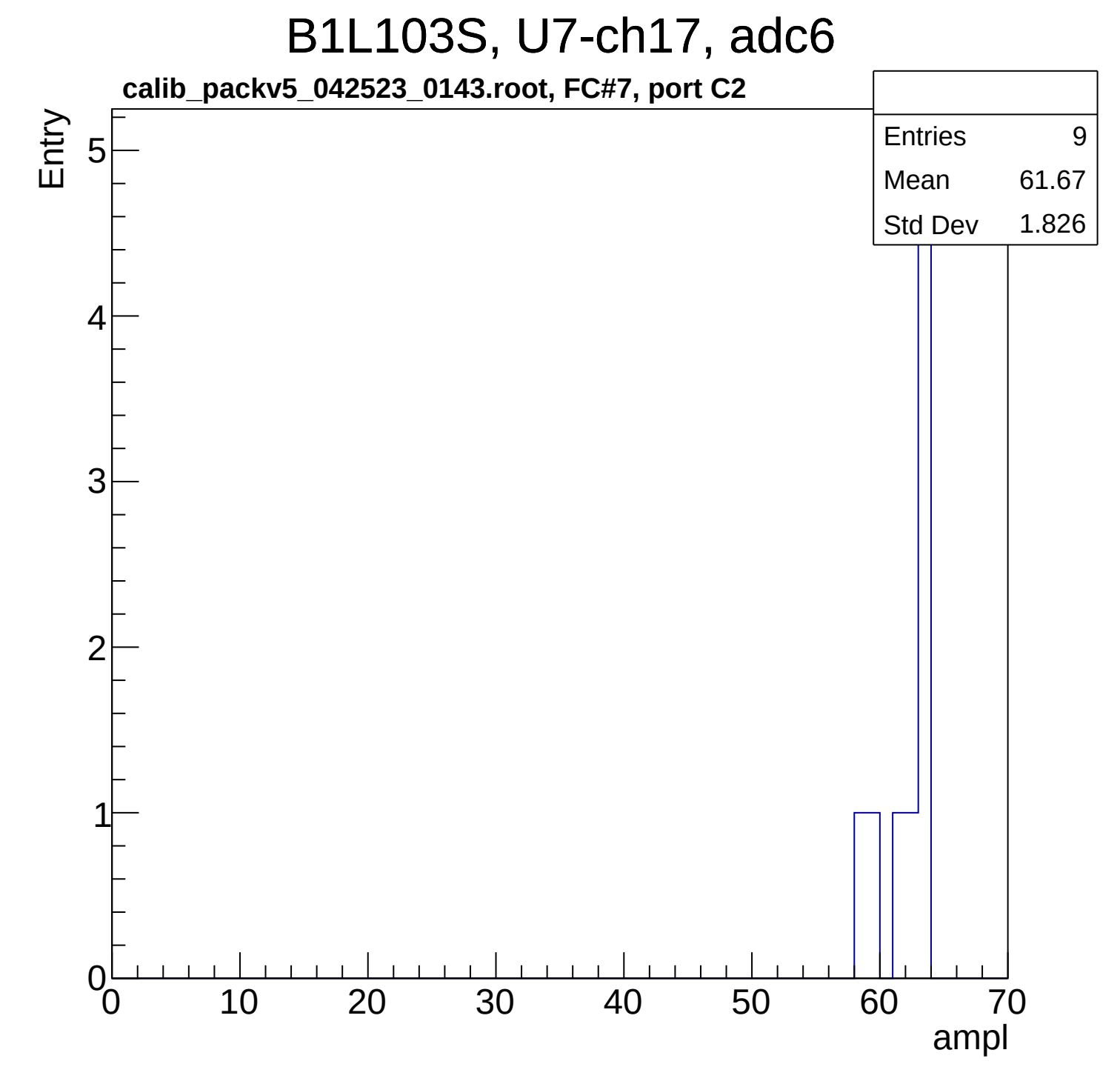
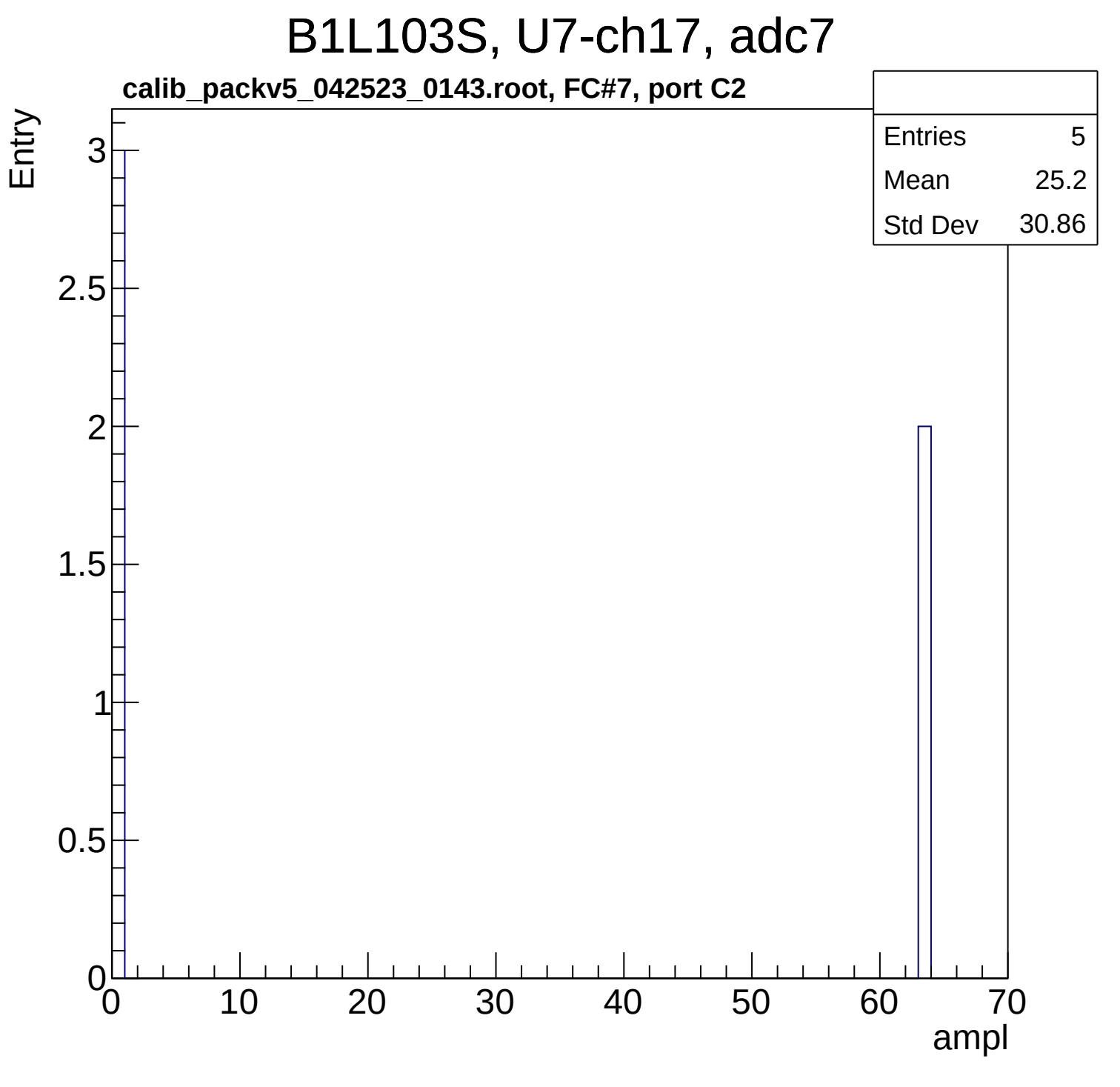
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch17, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 9
Mean 61.67
Std Dev 1.826
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U7-ch17, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 5
Mean 25.2
Std Dev 30.86
Entry
ampl
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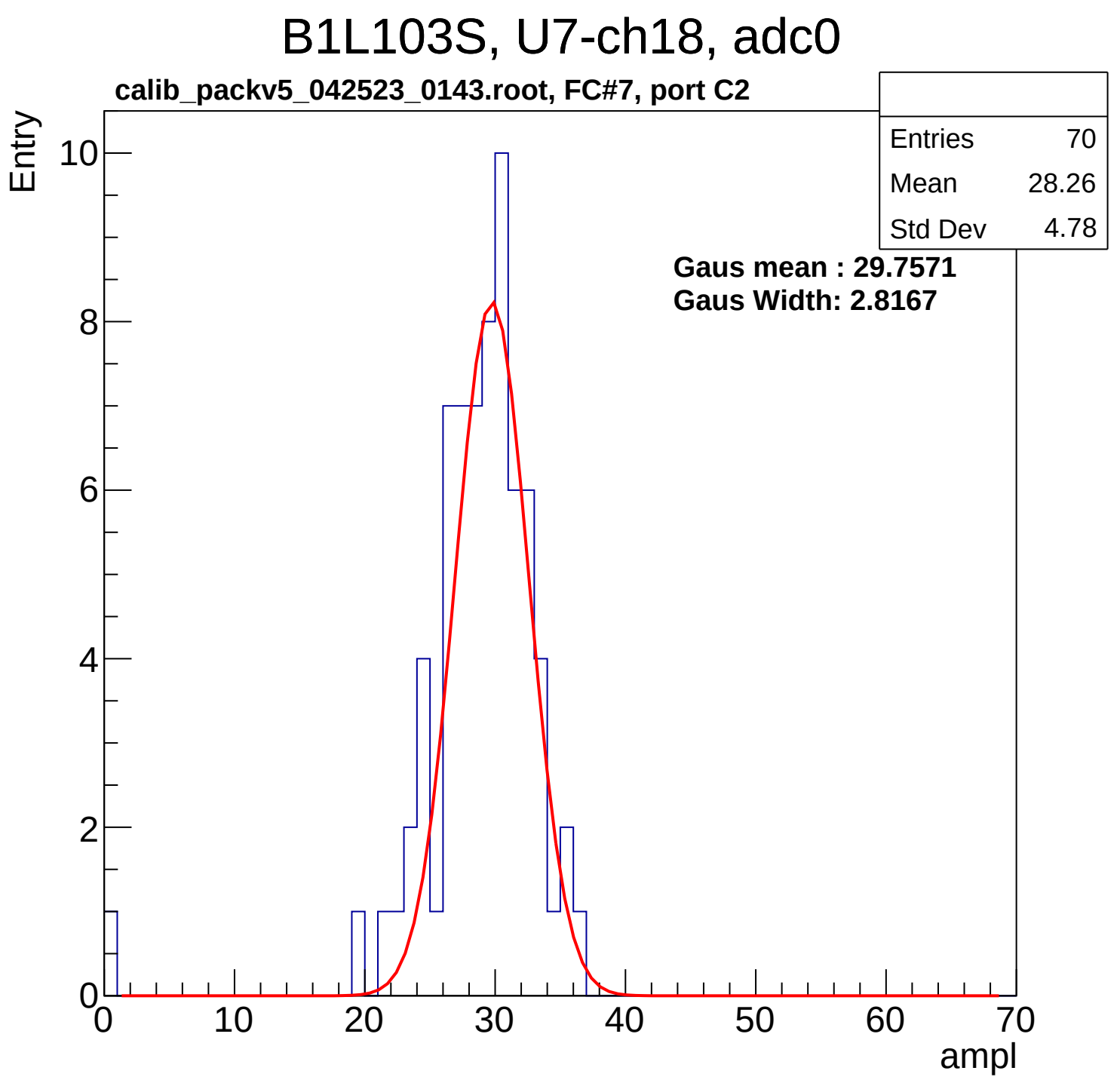
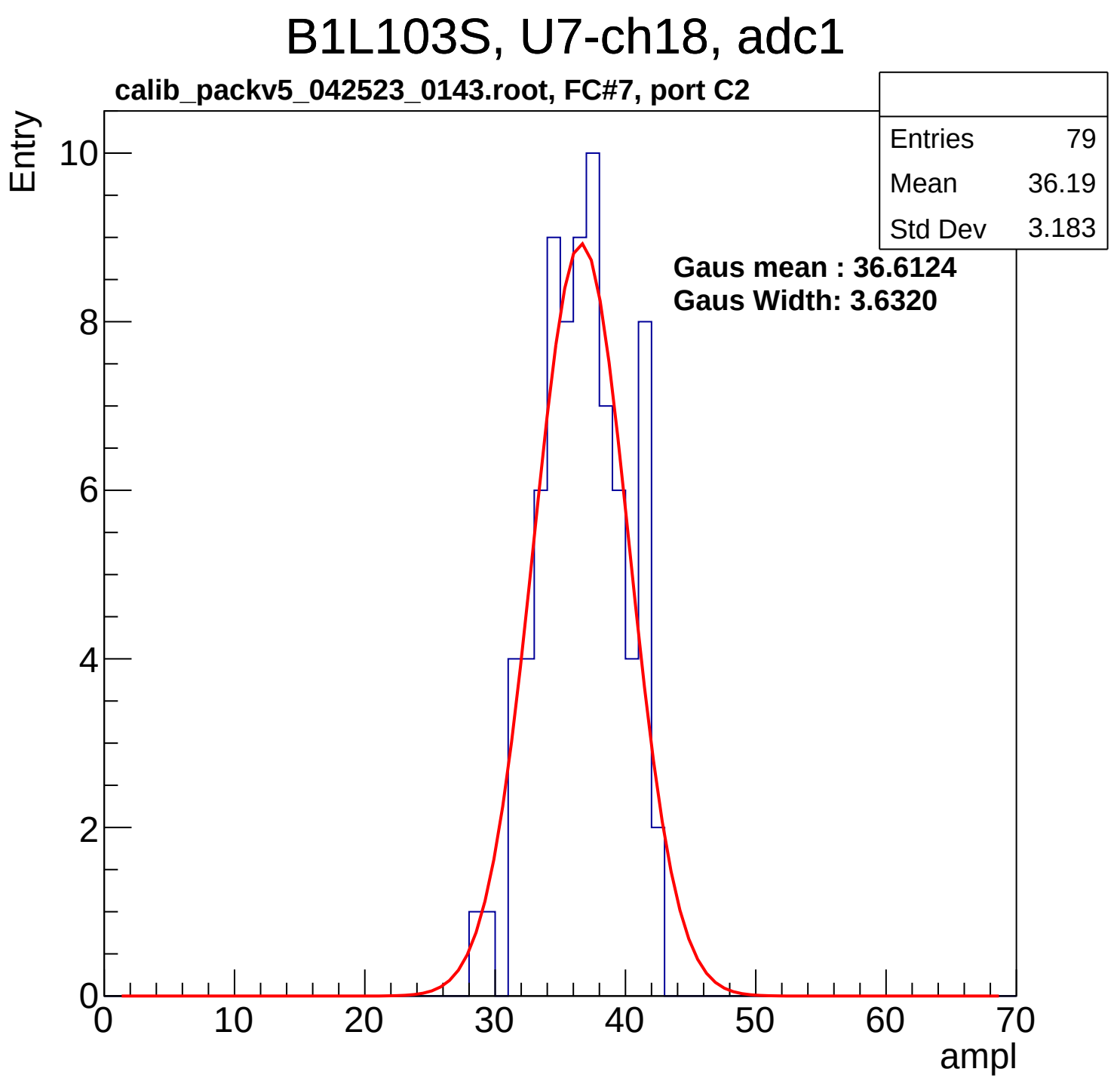
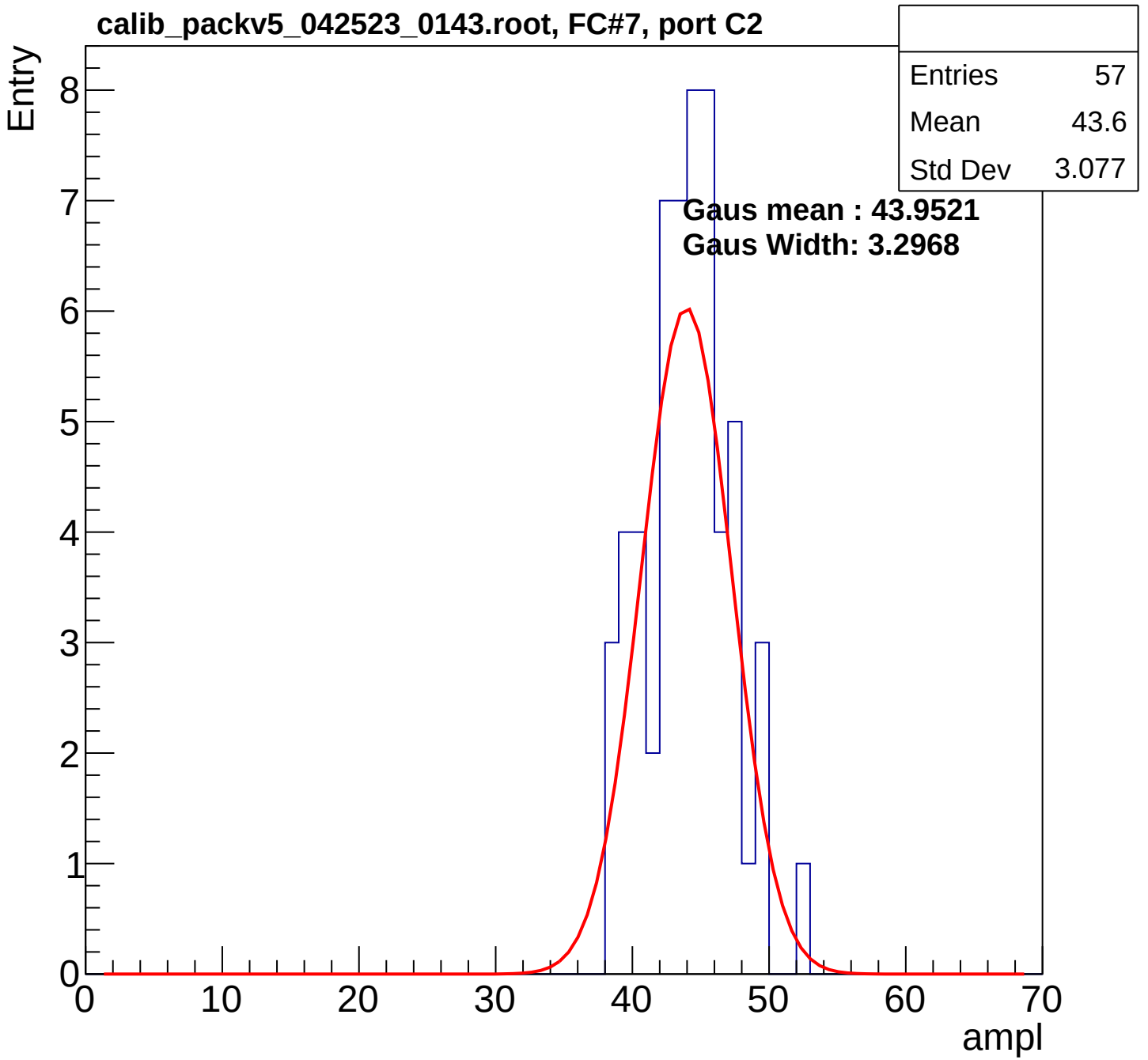
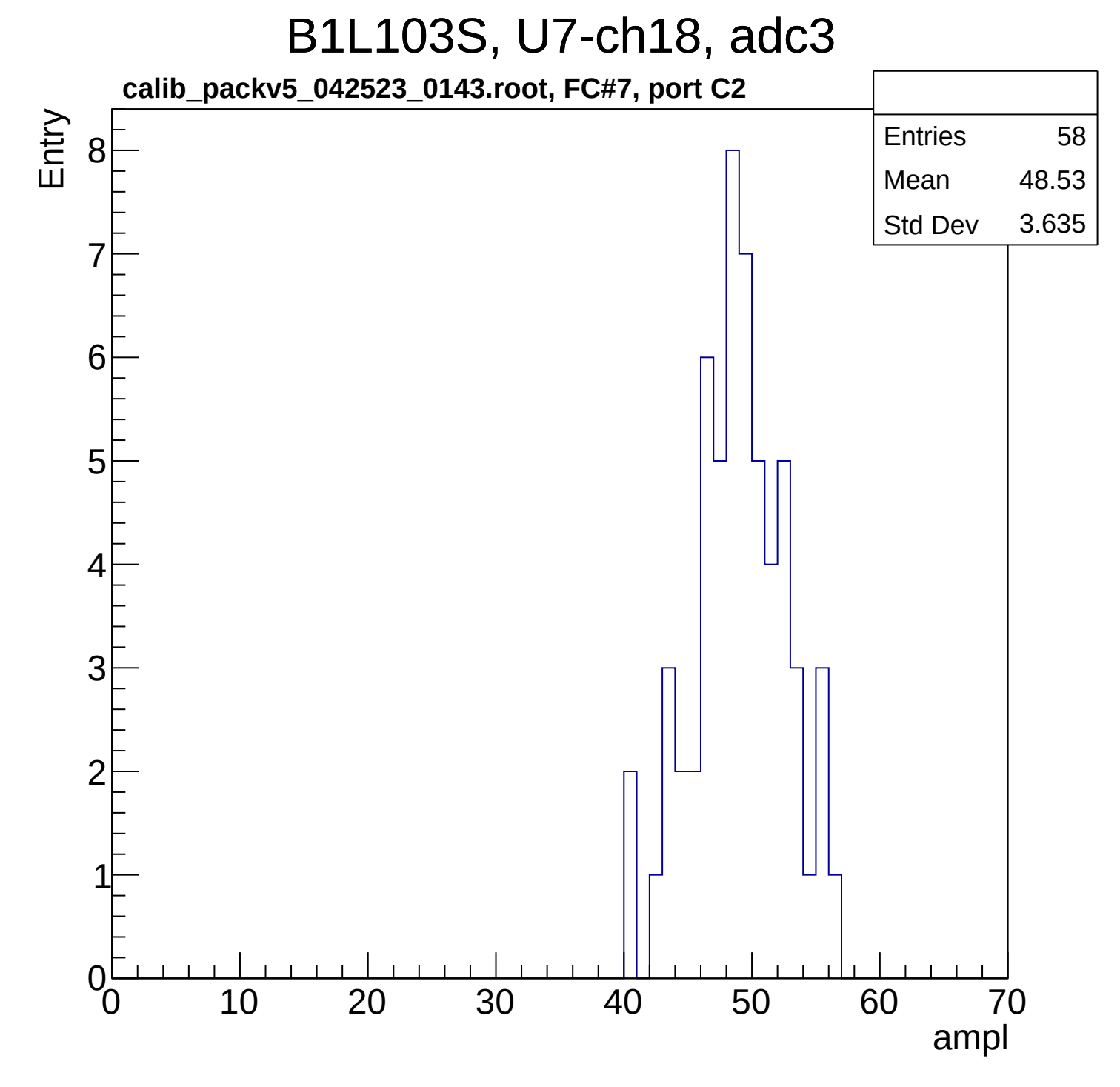
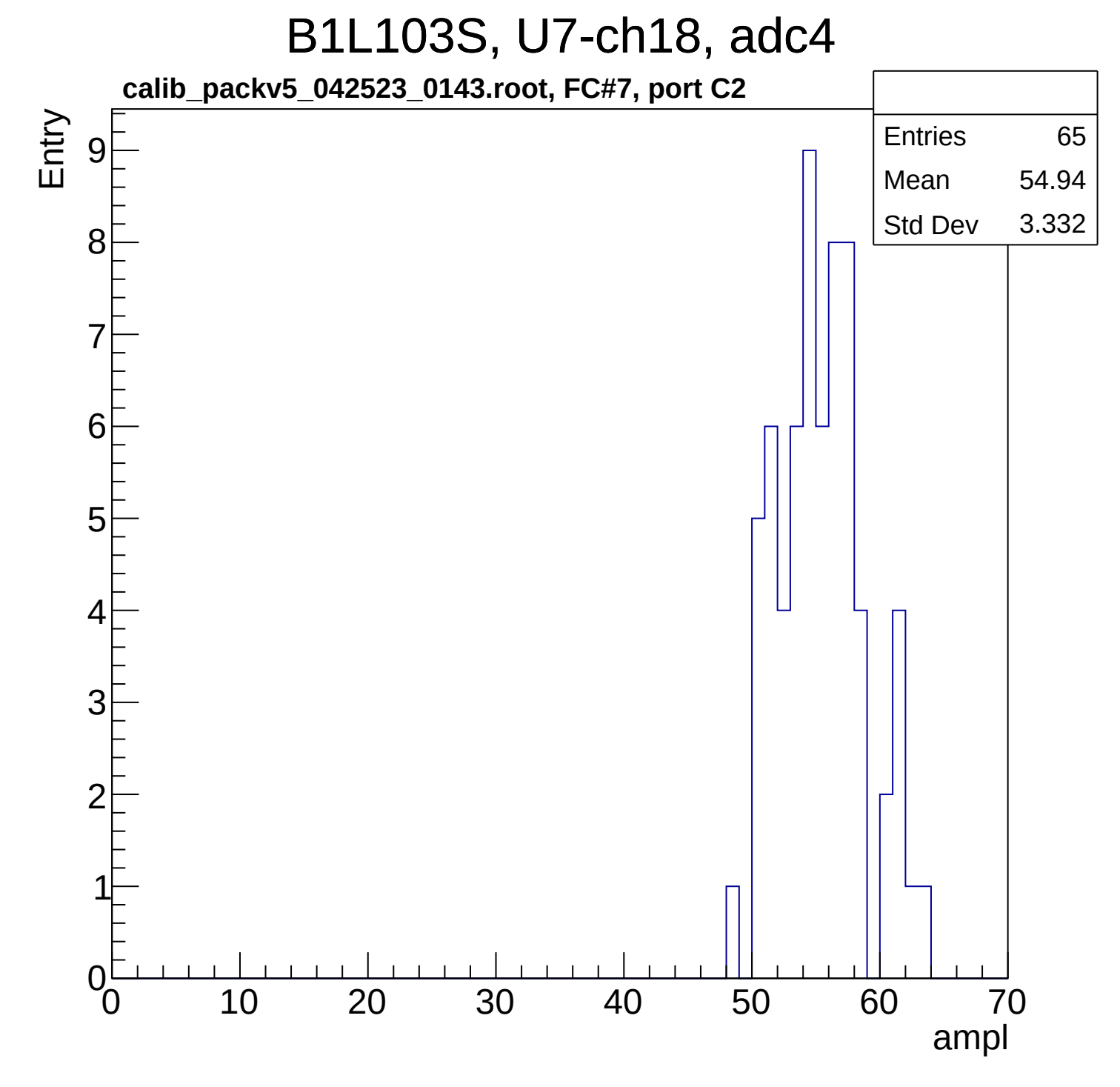
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U7-ch18, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 28.26
Std Dev 4.78
Gaus mean : 29.7571
Gaus Width: 2.8167
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch18, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 79
Mean 36.19
Std Dev 3.183
Gaus mean : 36.6124
Gaus Width: 3.6320
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch18, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 43.6
Std Dev 3.077
Gaus mean : 43.9521
Gaus Width: 3.2968
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch18, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 58
Mean 48.53
Std Dev 3.635
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch18, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 54.94
Std Dev 3.332
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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40
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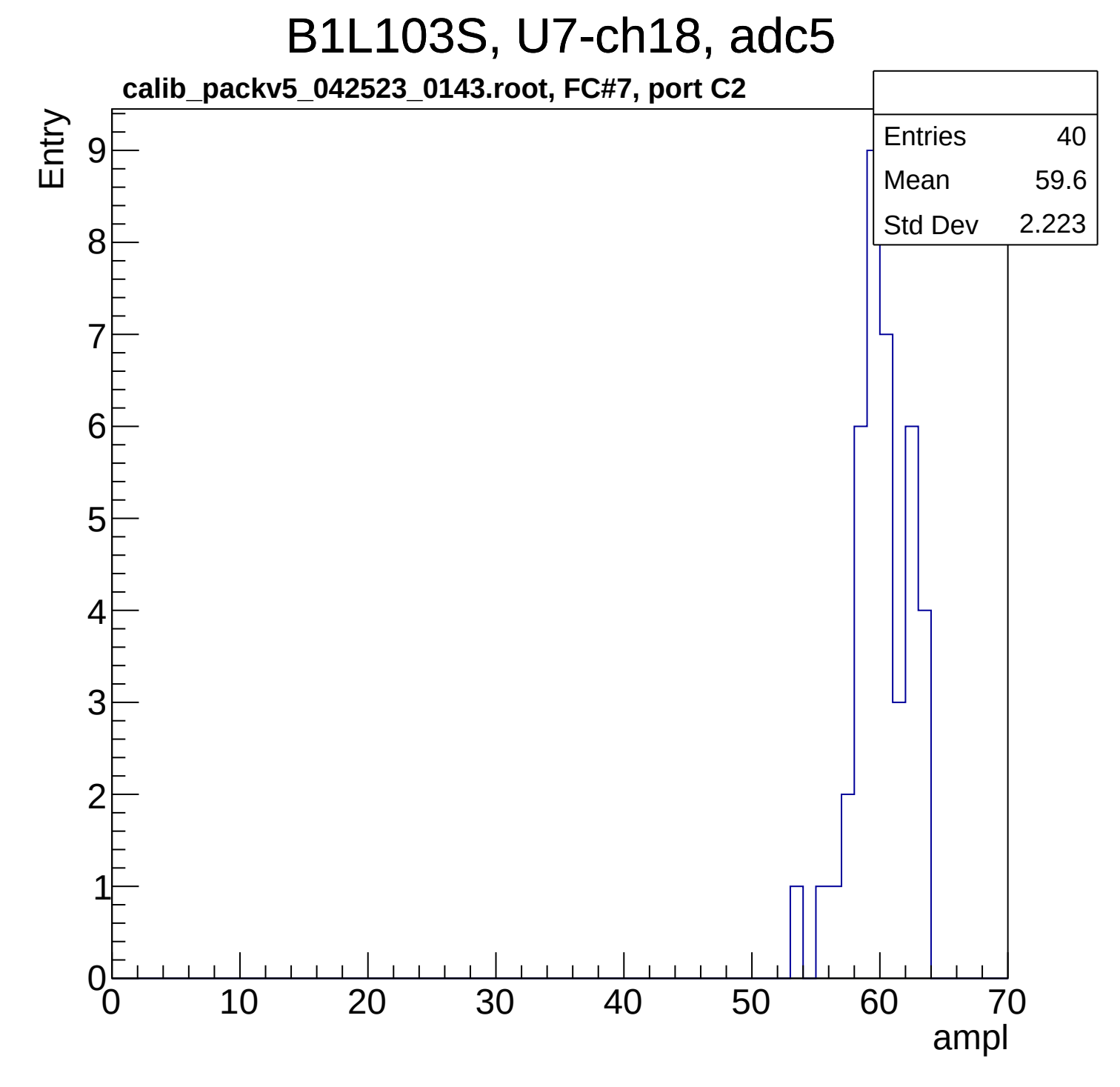
60
70


B1L103S, U7-ch18, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 40
Mean 59.6
Std Dev 2.223
Entry
ampl
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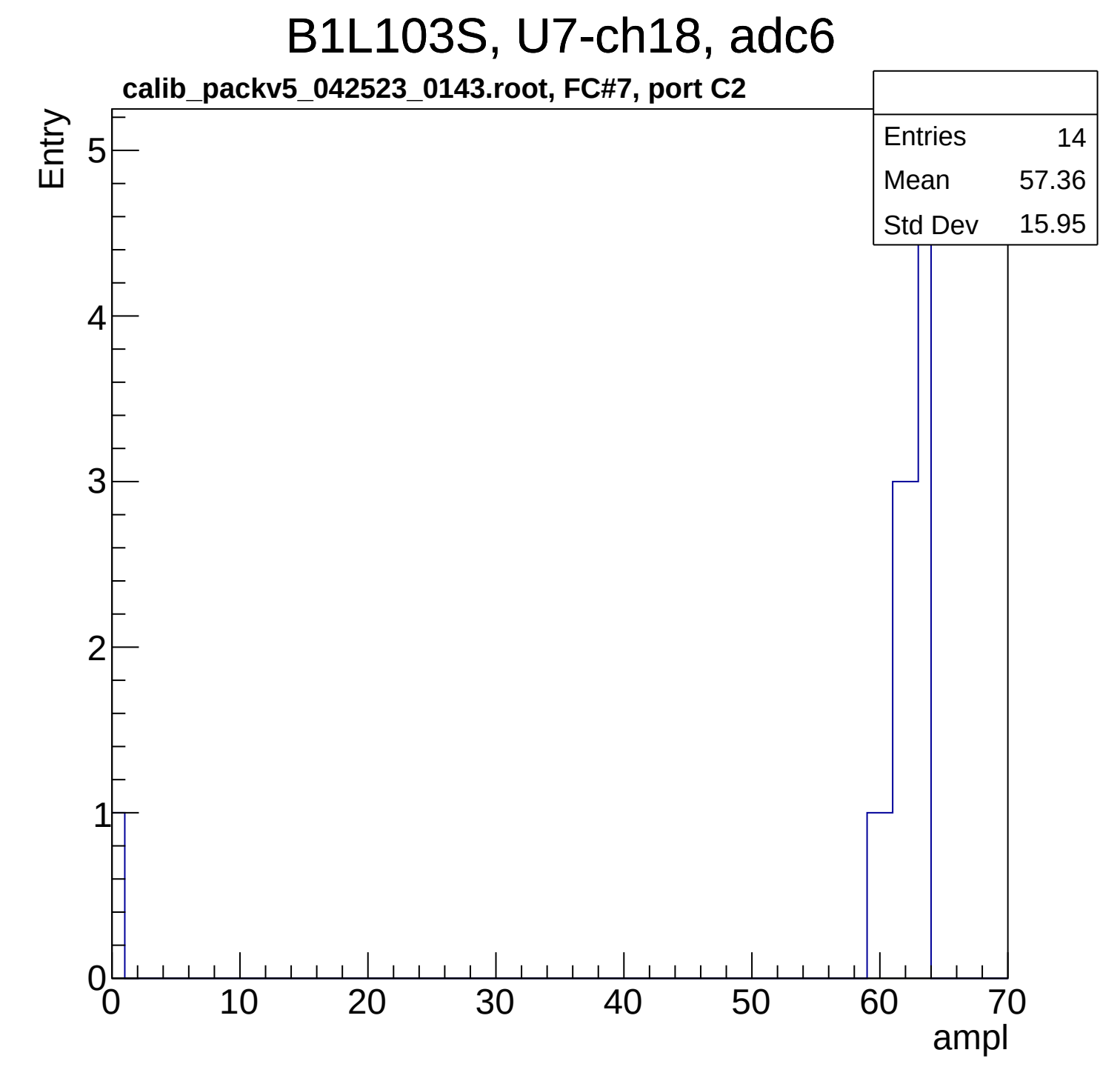
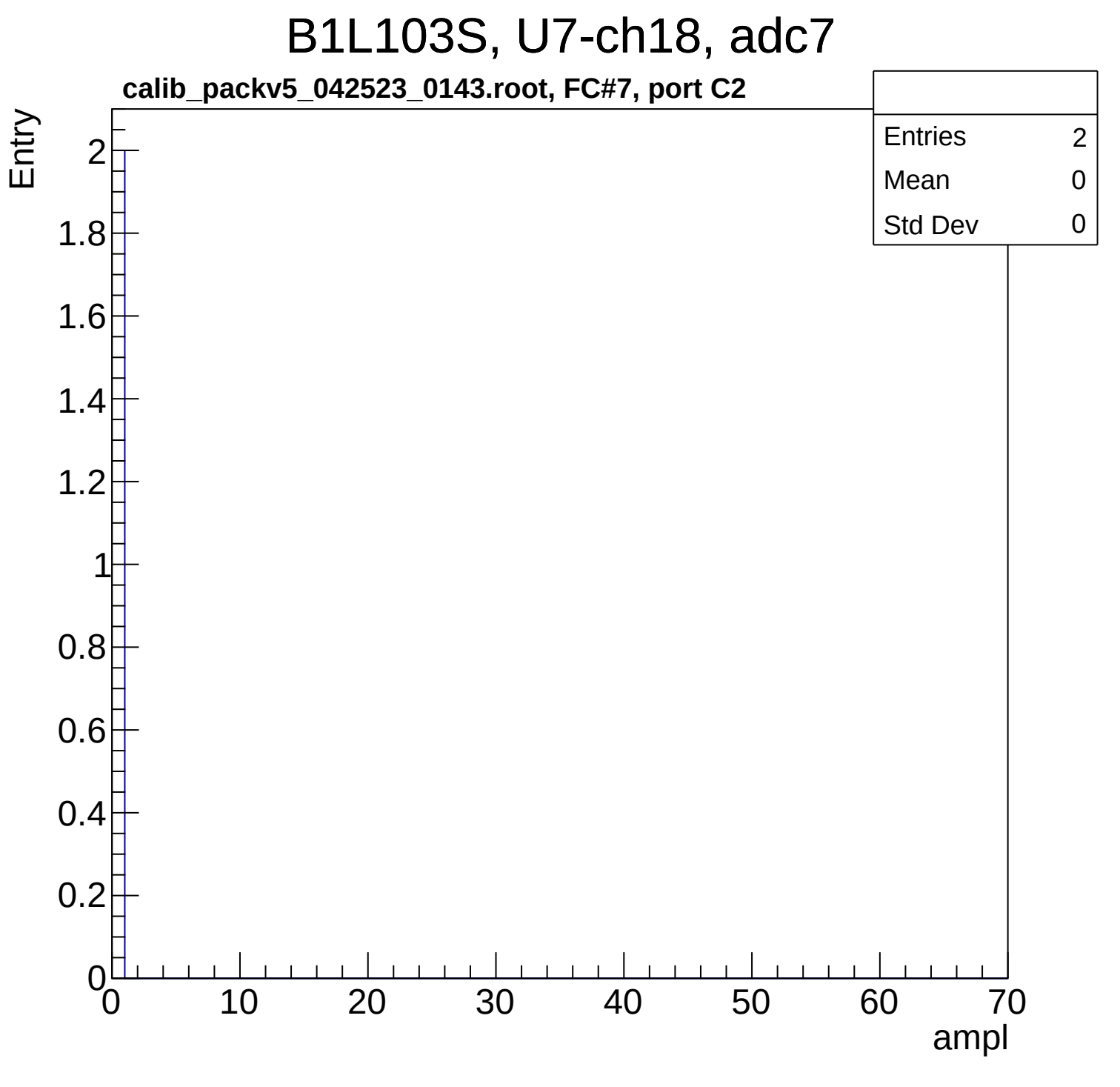
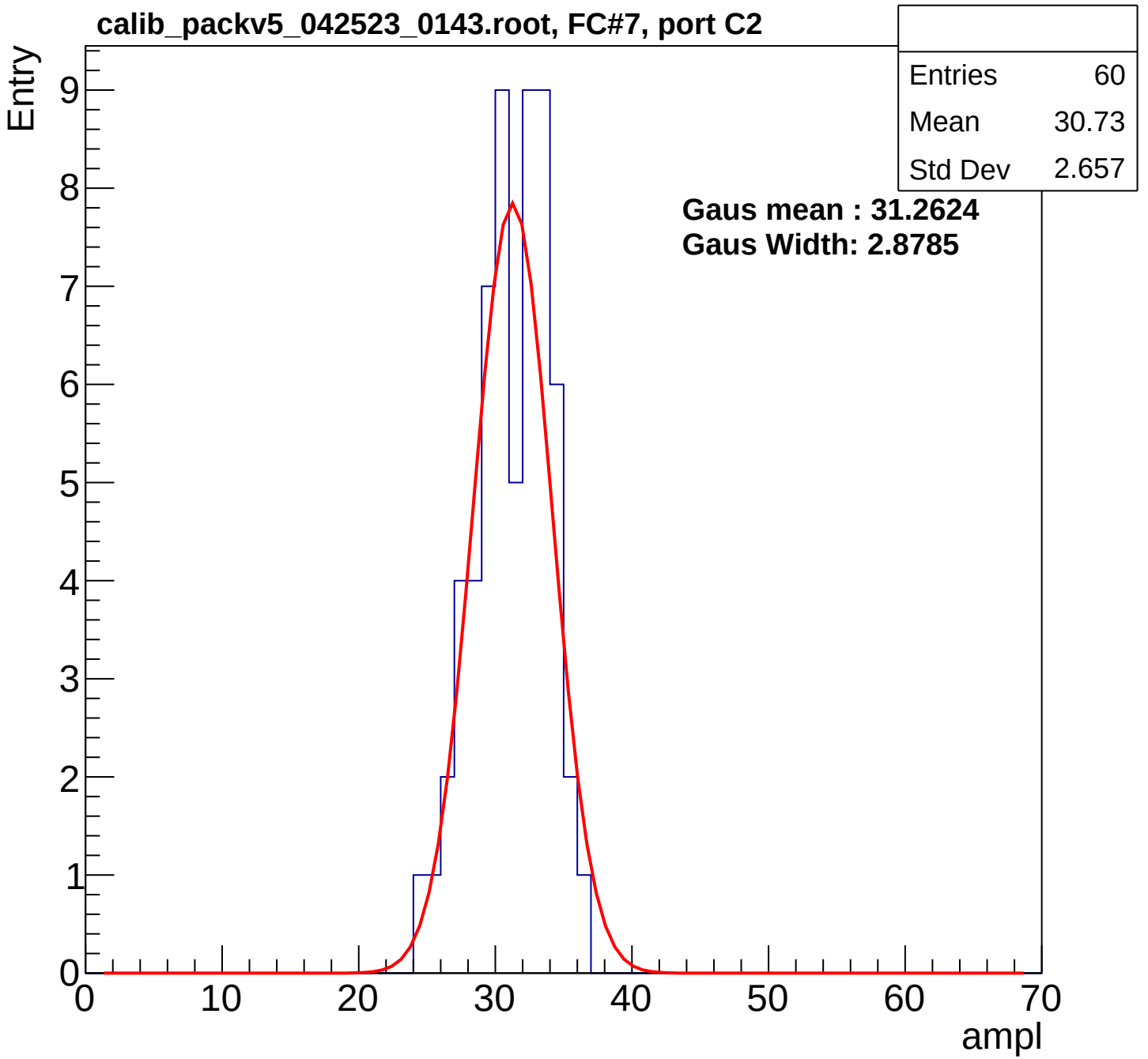
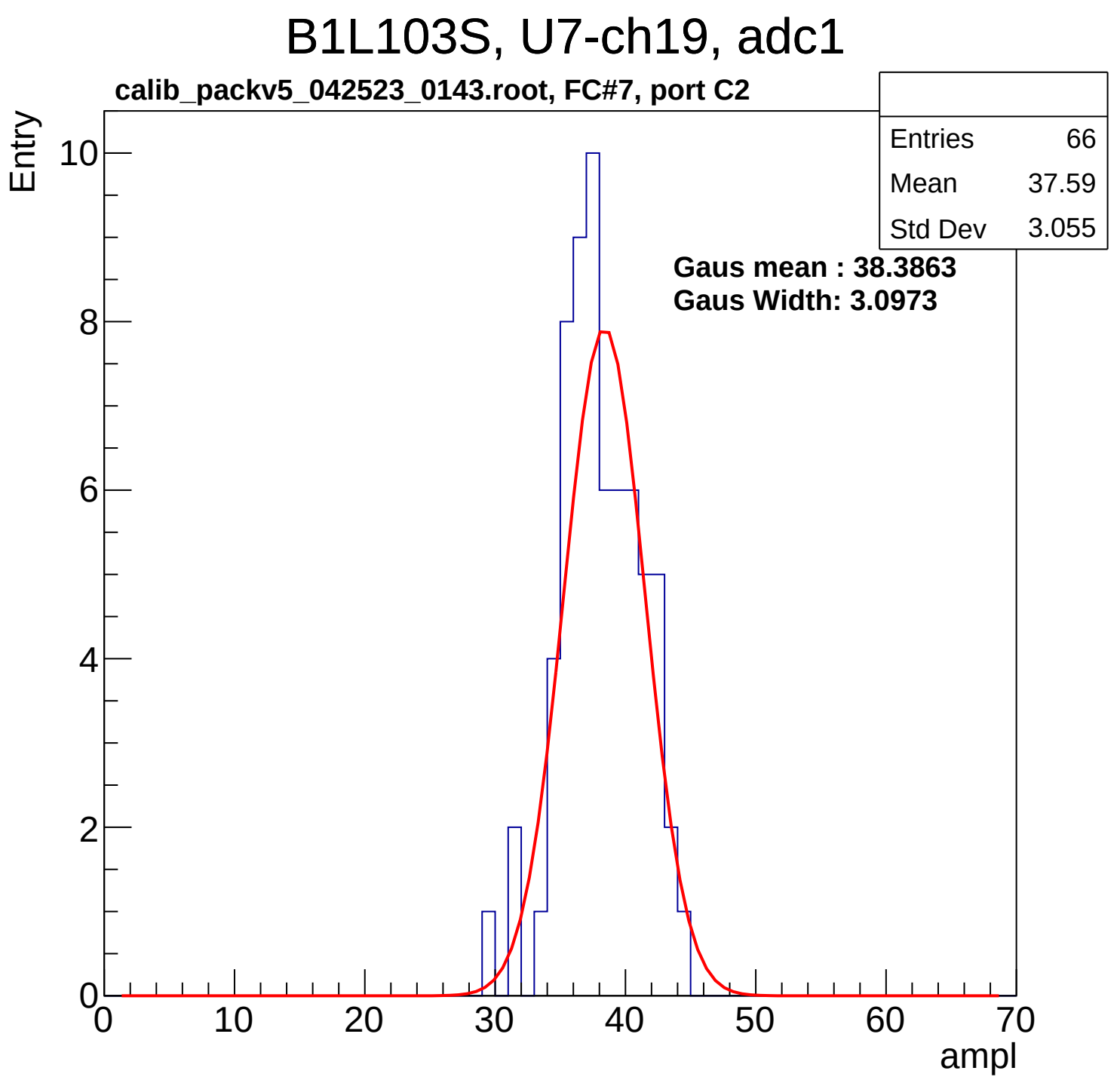
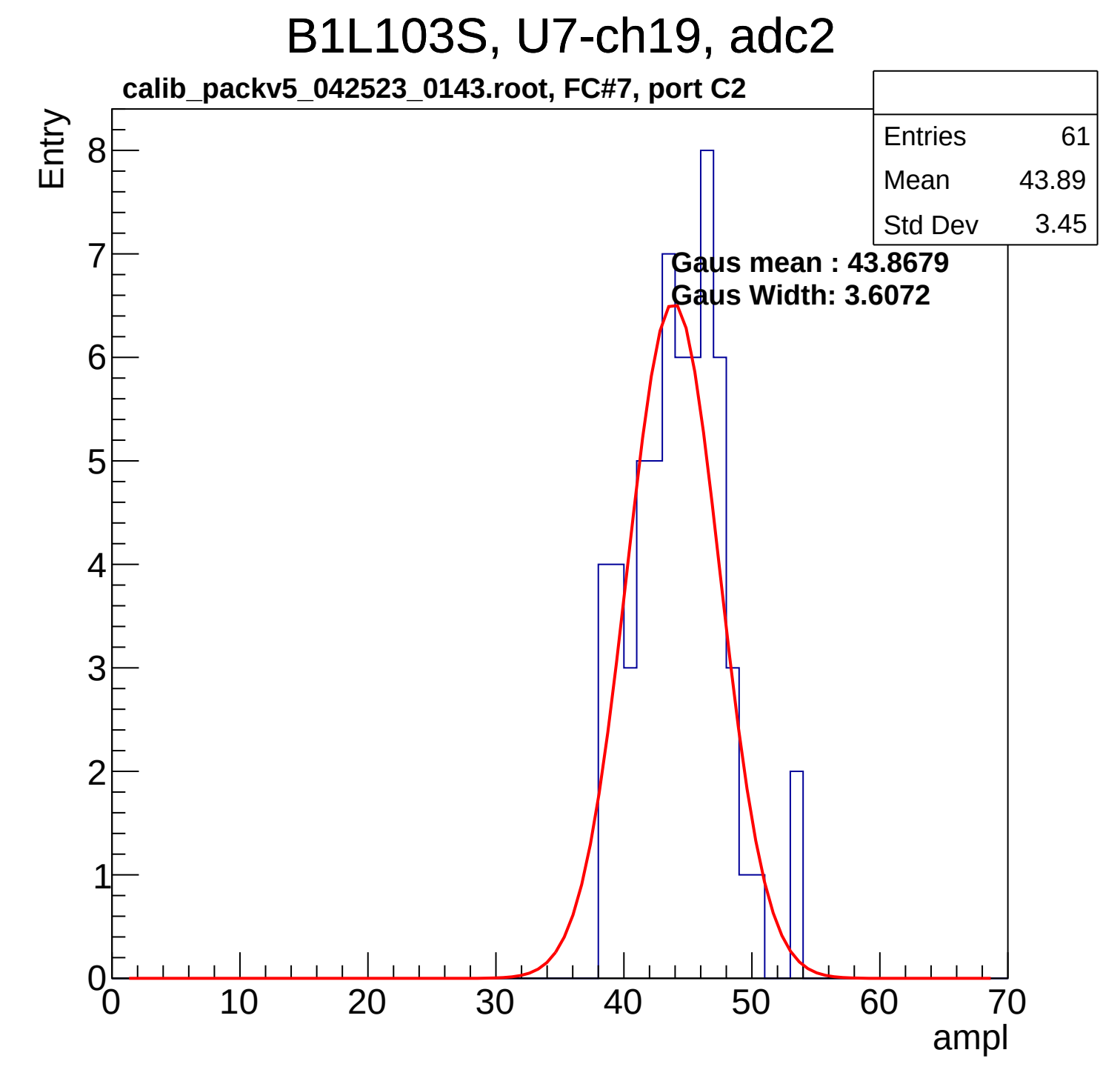
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

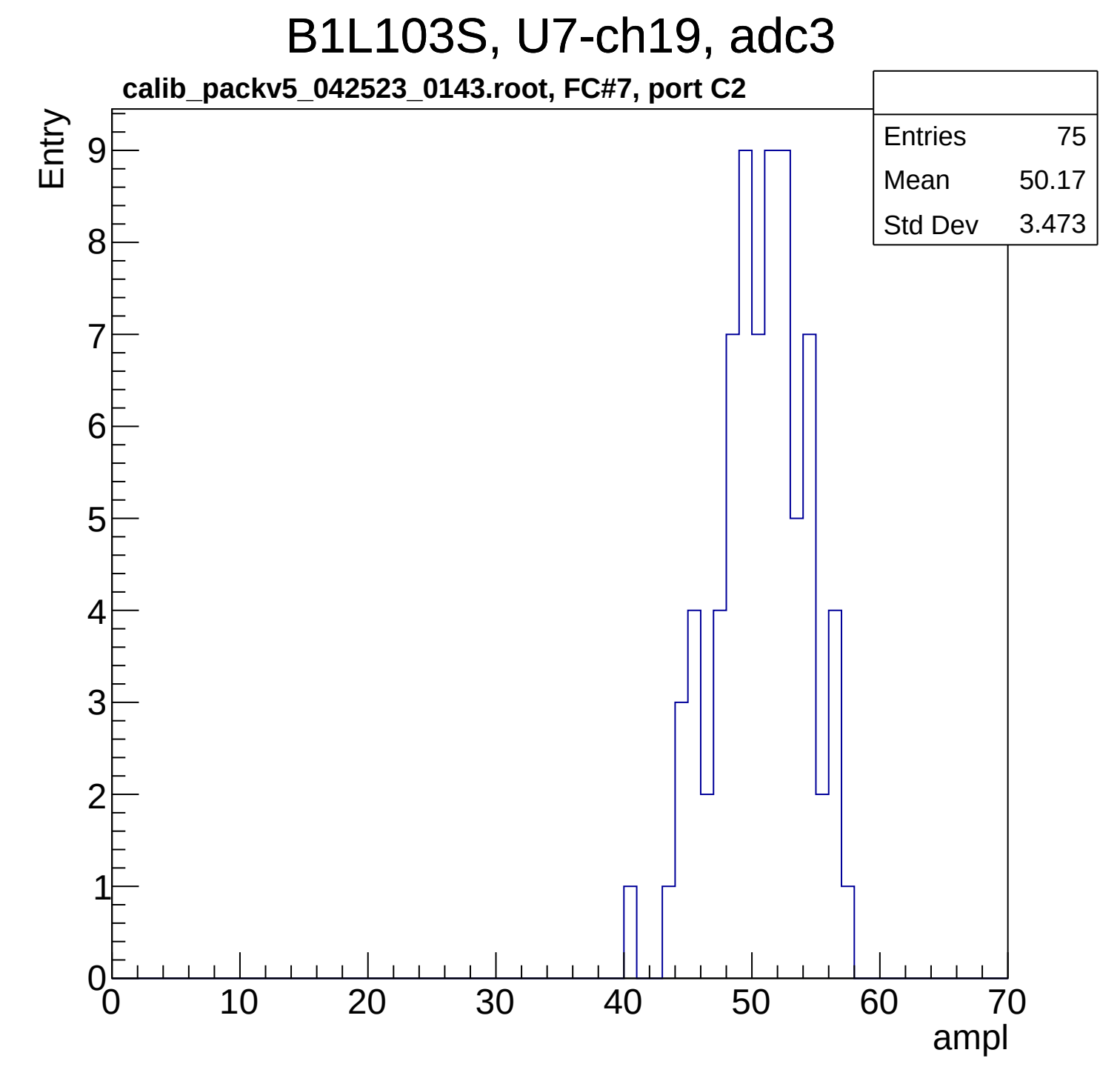

B1L103S, U7-ch18, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 14
Mean 57.36
Std Dev 15.95
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch18, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch19, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 60
Mean 30.73
Std Dev 2.657
Gaus mean : 31.2624
Gaus Width: 2.8785
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch19, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 37.59
Std Dev 3.055
Gaus mean : 38.3863
Gaus Width: 3.0973
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch19, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 61
Mean 43.89
Std Dev 3.45
Gaus mean : 43.8679
Gaus Width: 3.6072
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch19, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 75
Mean 50.17
Std Dev 3.473
Entry
ampl
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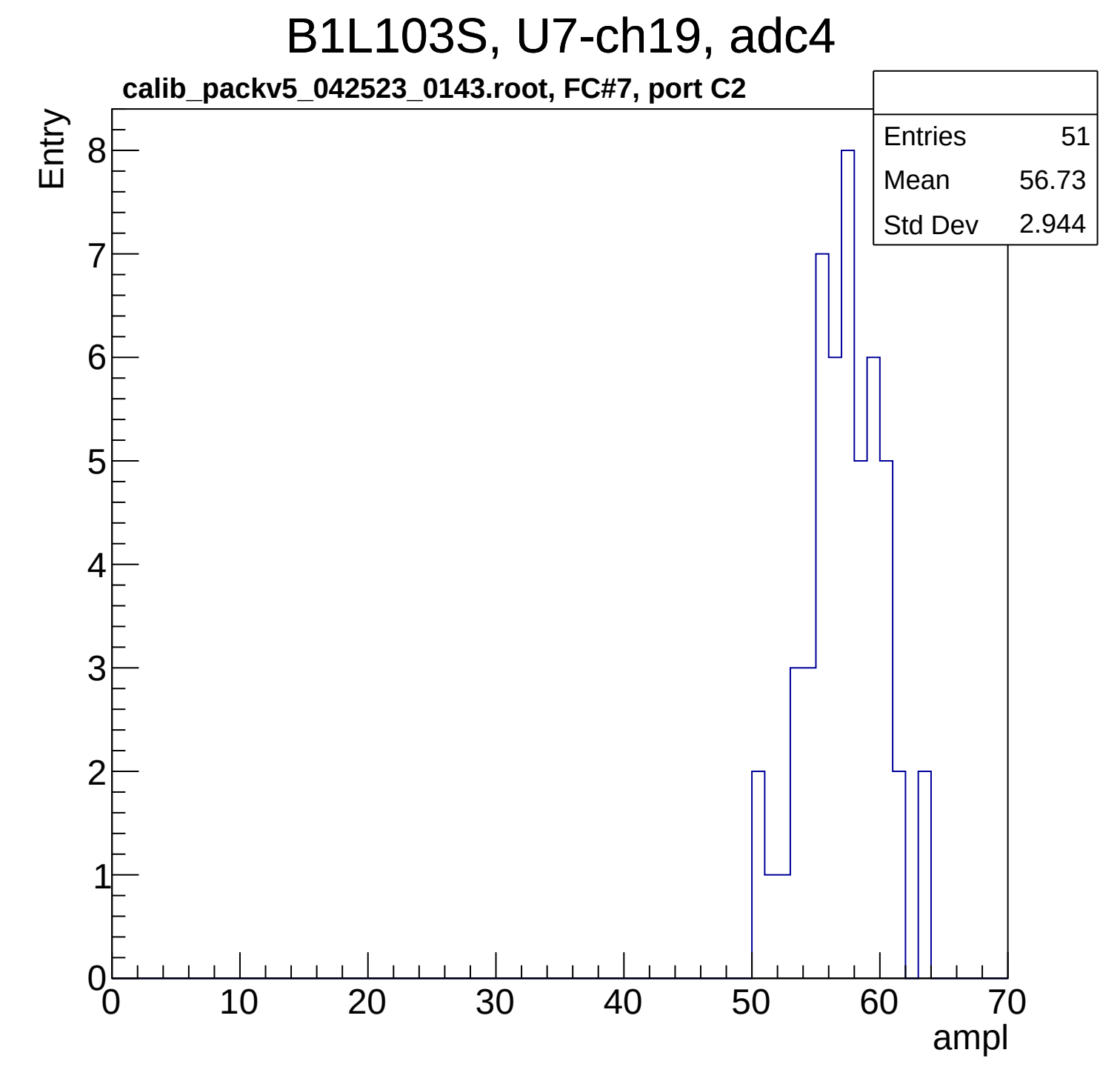
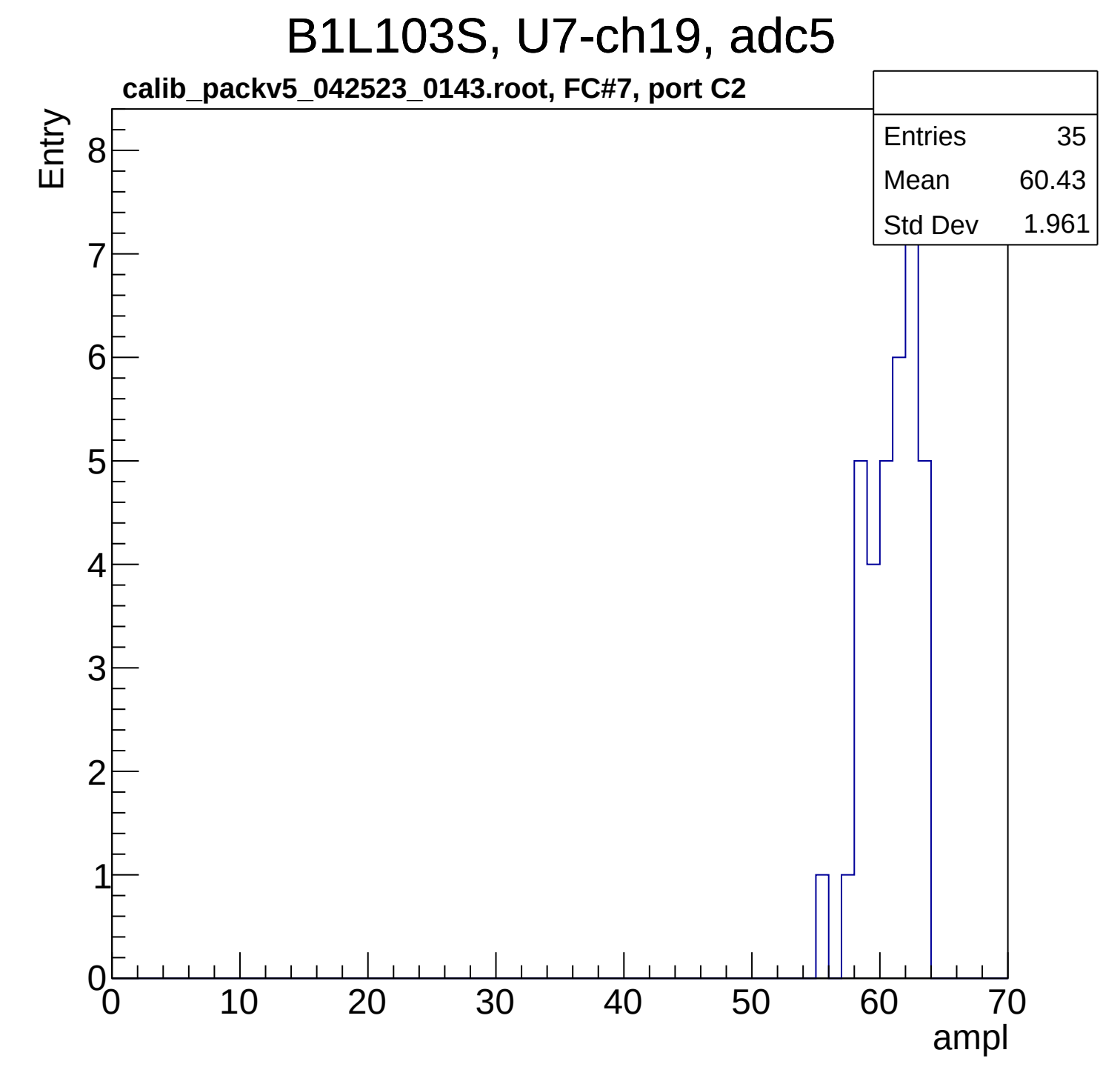
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch19, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 51
Mean 56.73
Std Dev 2.944
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch19, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 35
Mean 60.43
Std Dev 1.961
Entry
ampl
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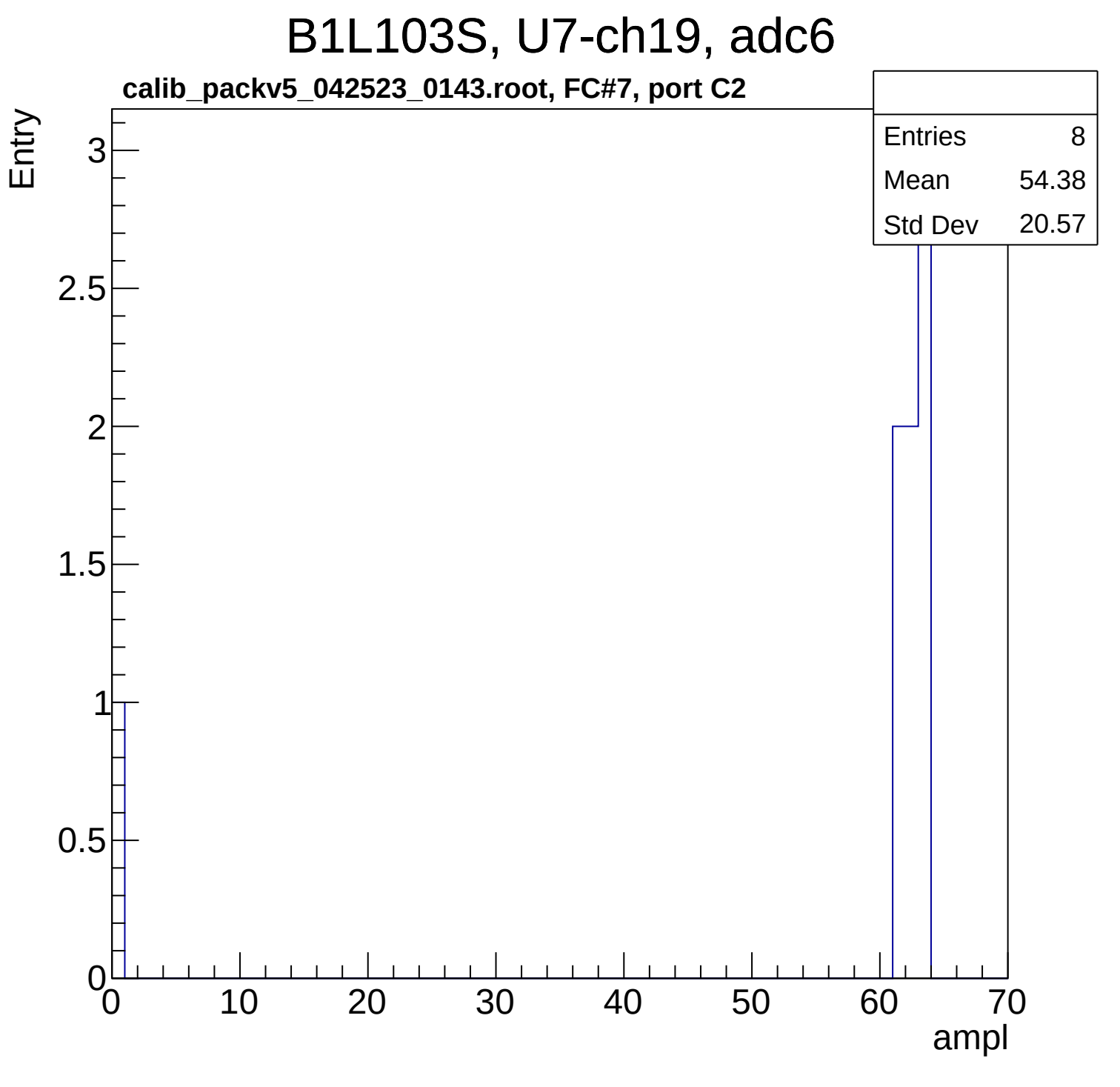
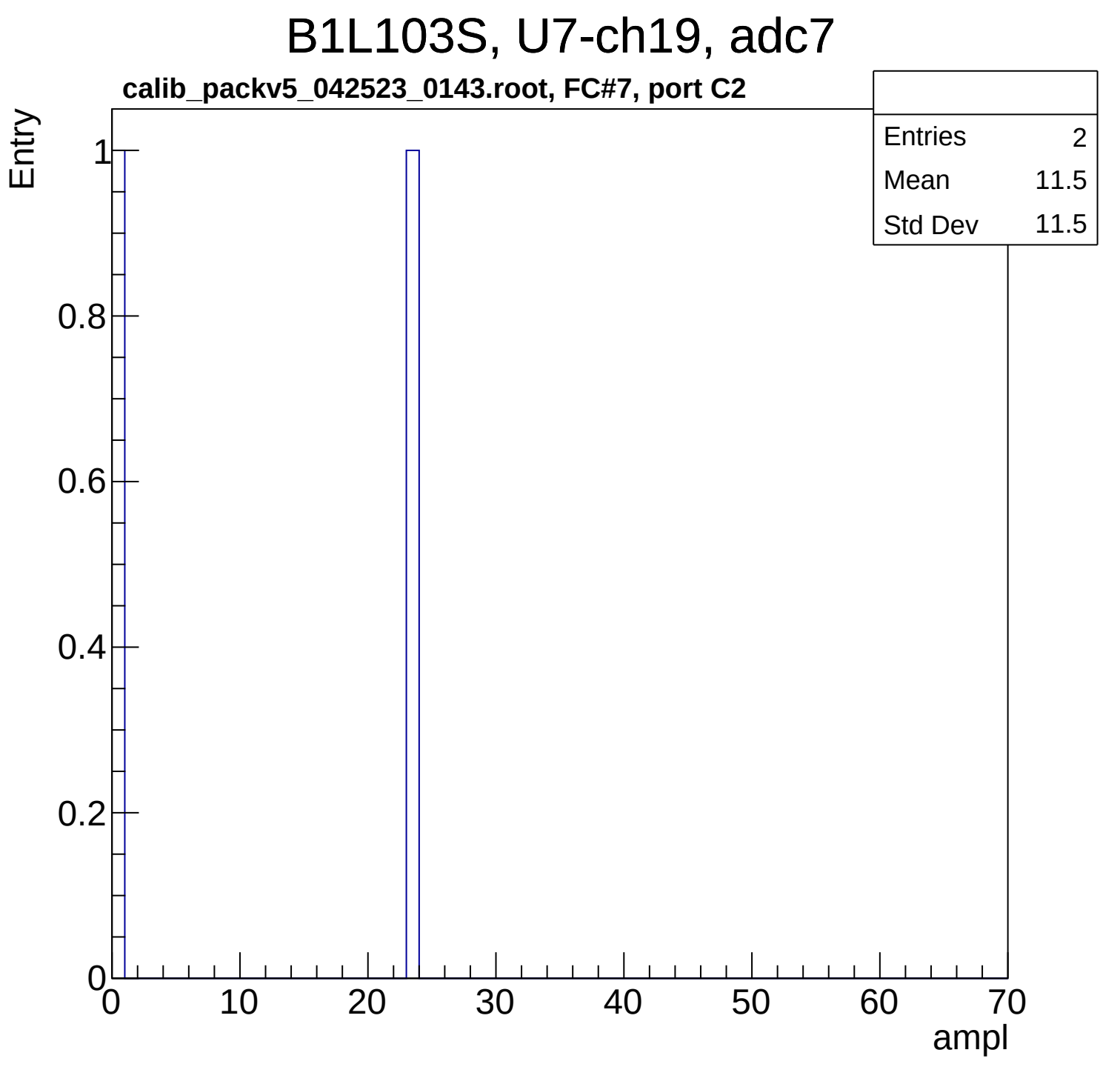
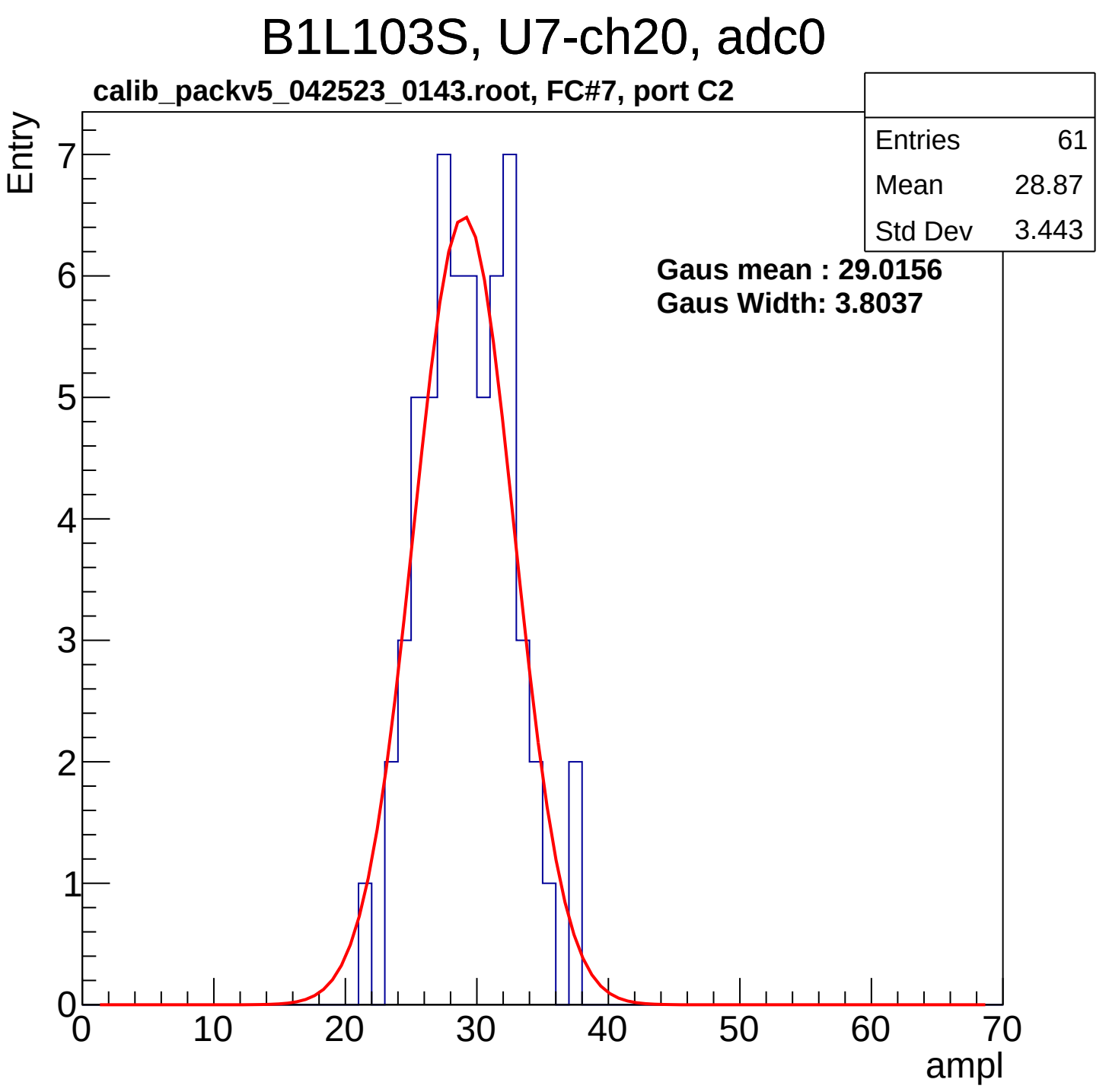
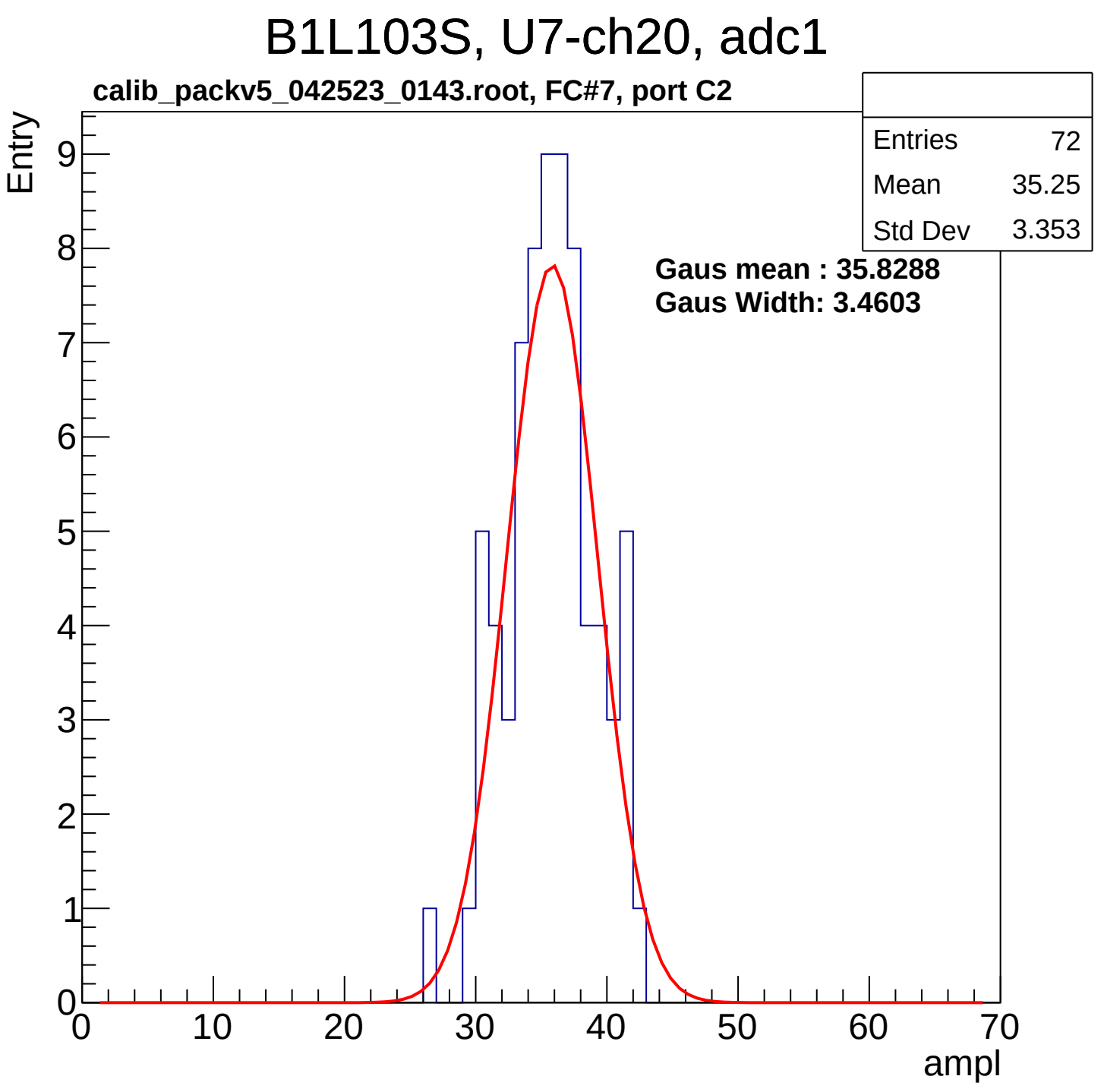
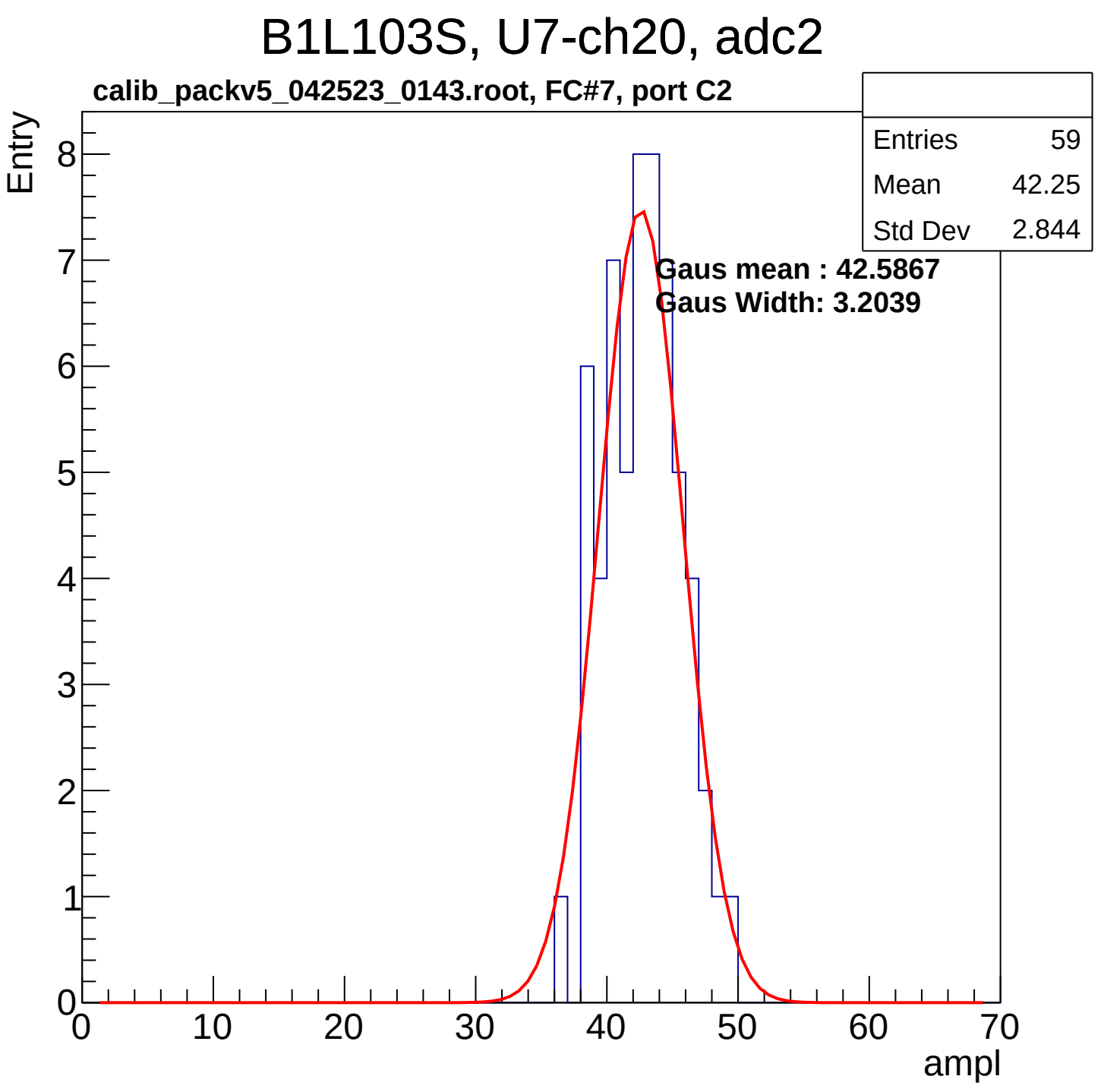
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

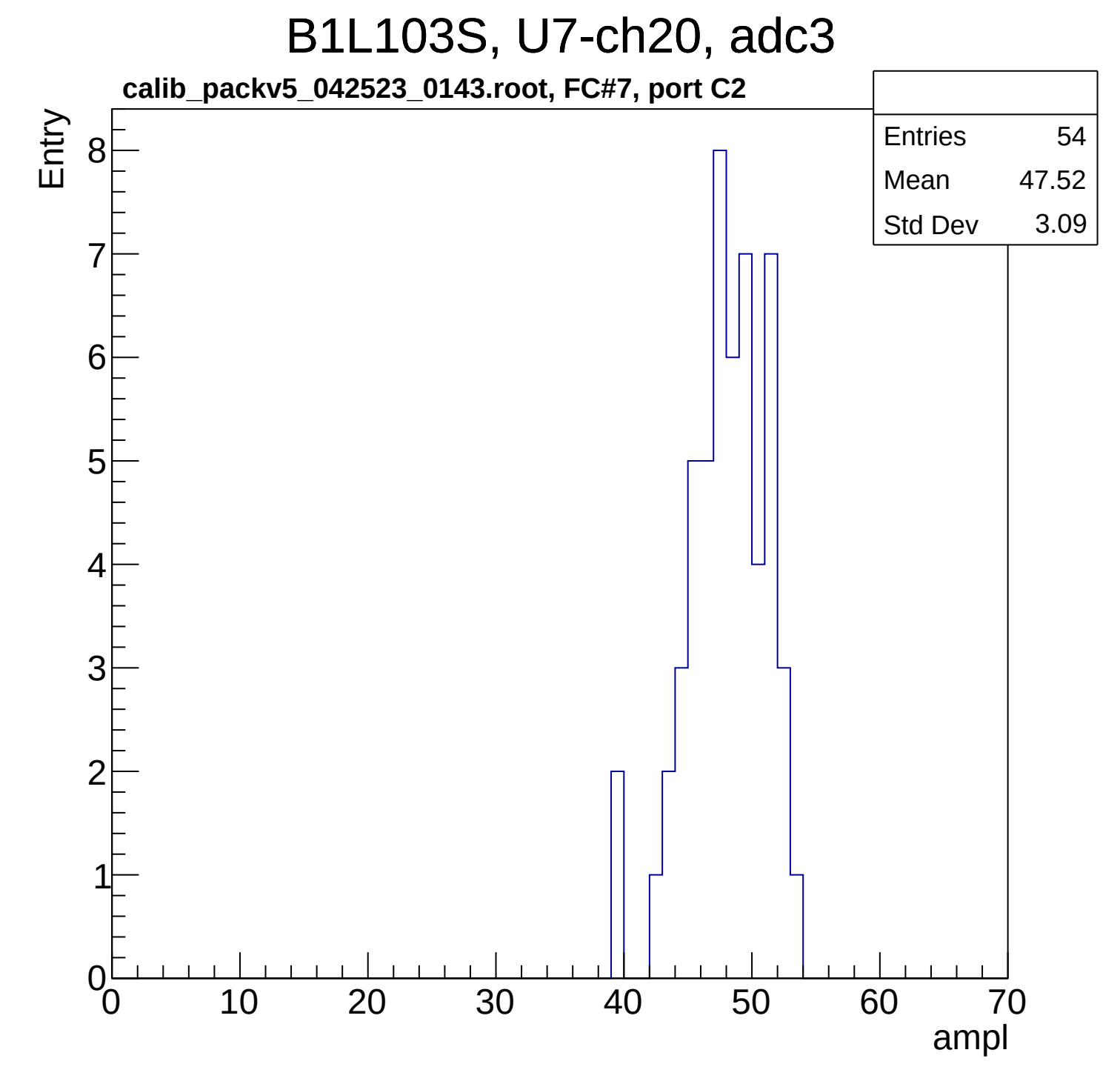

B1L103S, U7-ch19, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 8
Mean 54.38
Std Dev 20.57
Entry
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl

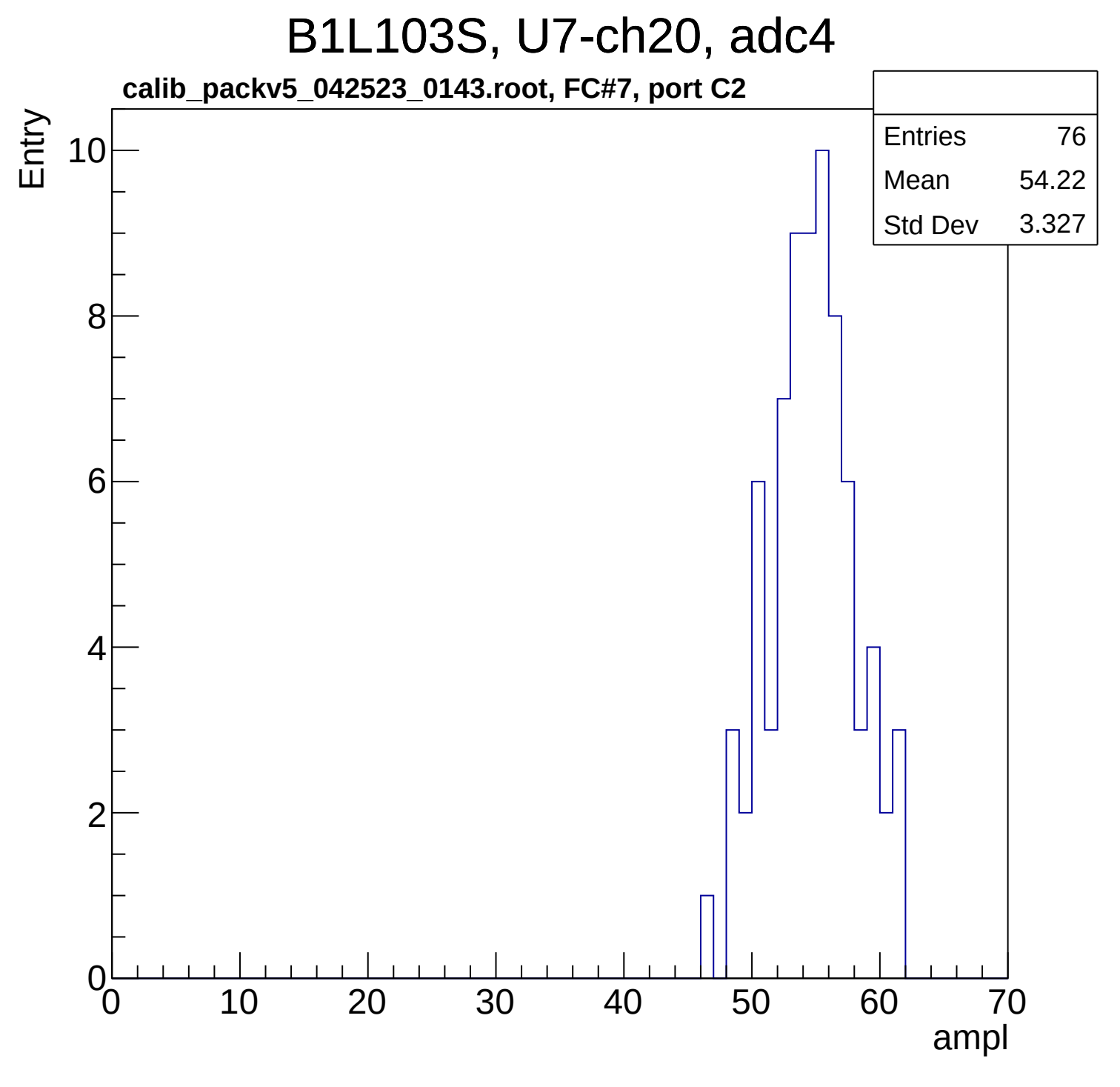

B1L103S, U7-ch19, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 11.5
Std Dev 11.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

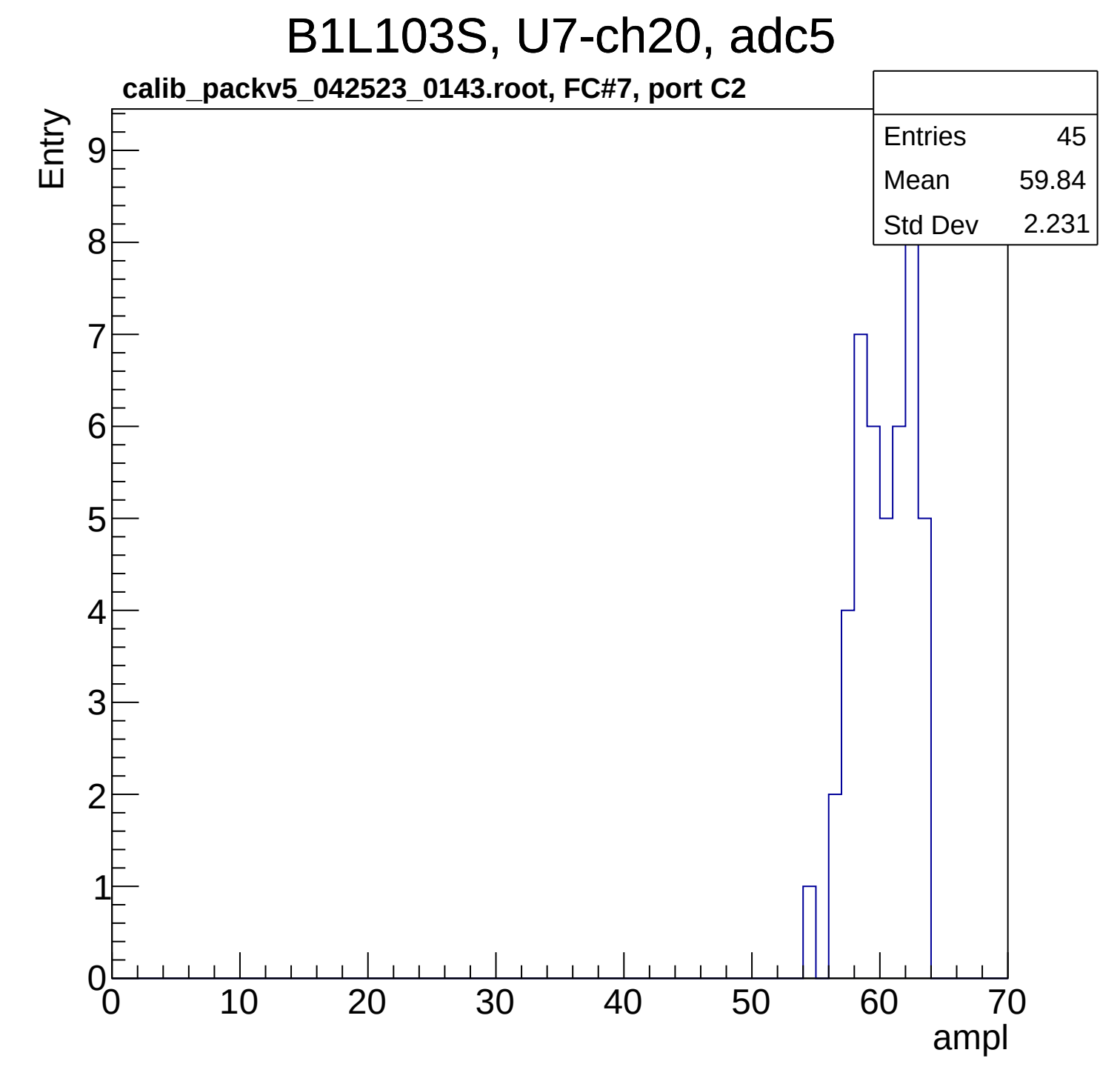

B1L103S, U7-ch20, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 61
Mean 28.87
Std Dev 3.443
Gaus mean : 29.0156
Gaus Width: 3.8037
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch20, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 72
Mean 35.25
Std Dev 3.353
Gaus mean : 35.8288
Gaus Width: 3.4603
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch20, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 42.25
Std Dev 2.844
Gaus mean : 42.5867
Gaus Width: 3.2039
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch20, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 54
Mean 47.52
Std Dev 3.09
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch20, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 76
Mean 54.22
Std Dev 3.327
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch20, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 45
Mean 59.84
Std Dev 2.231
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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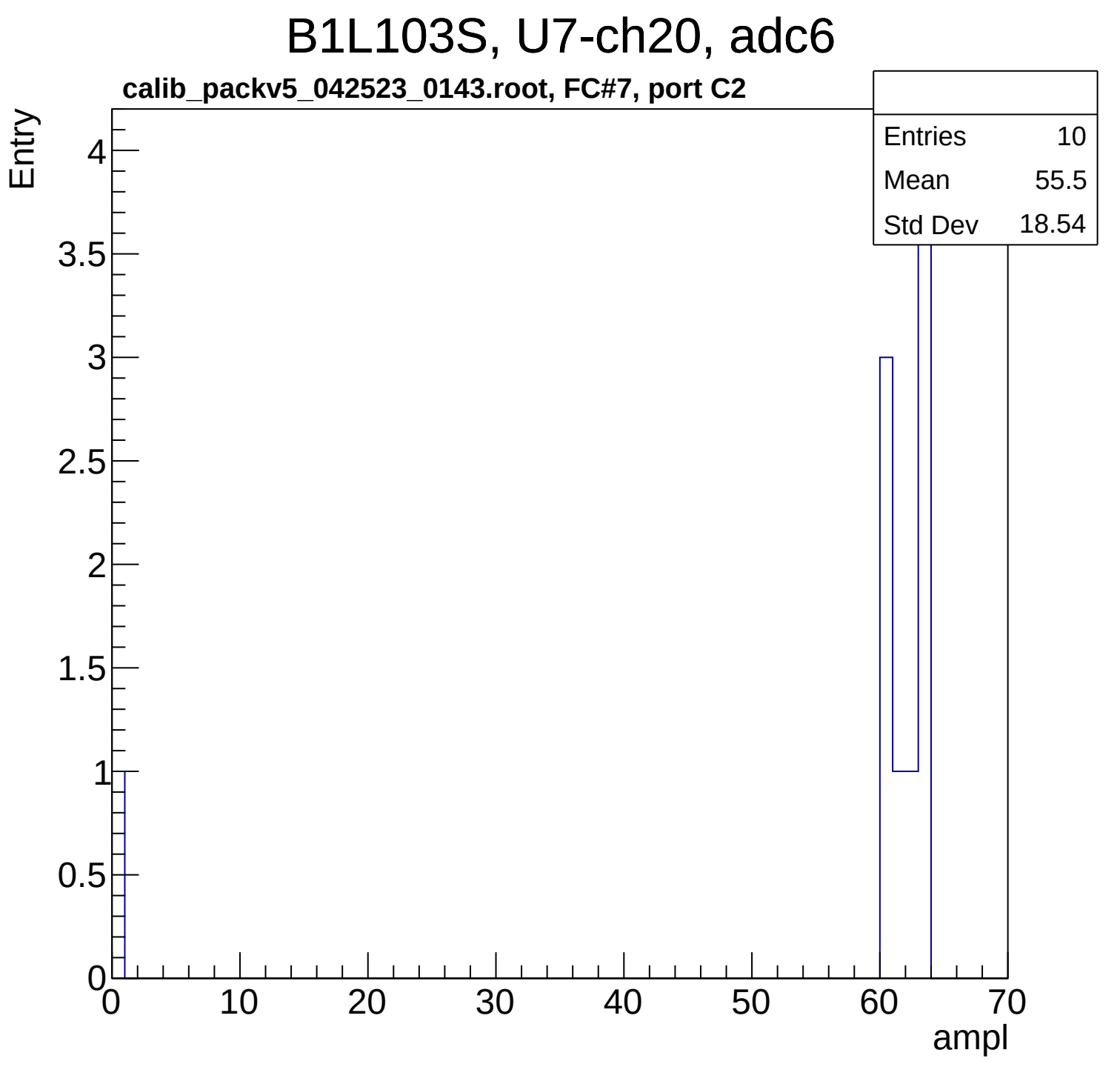
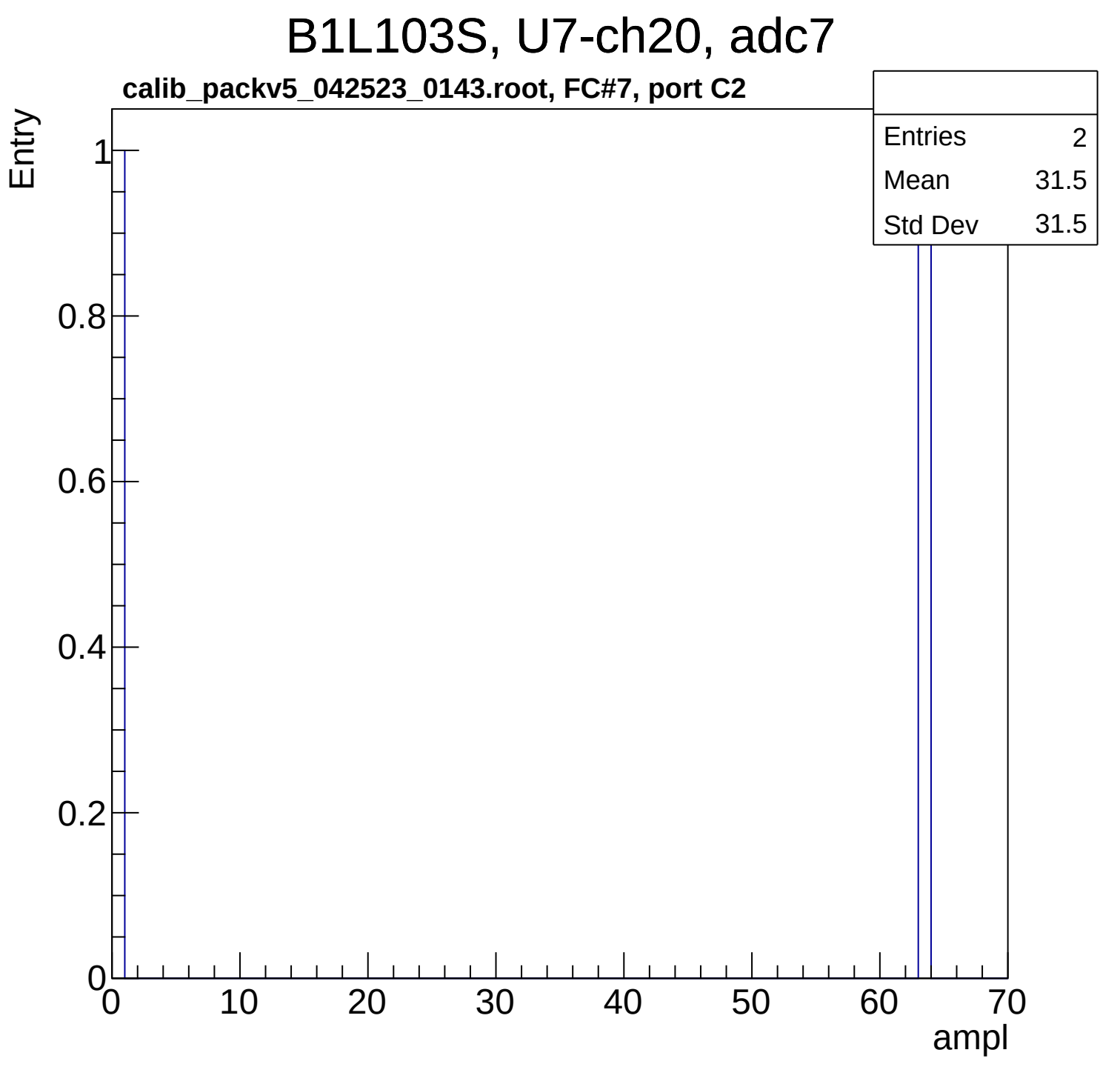
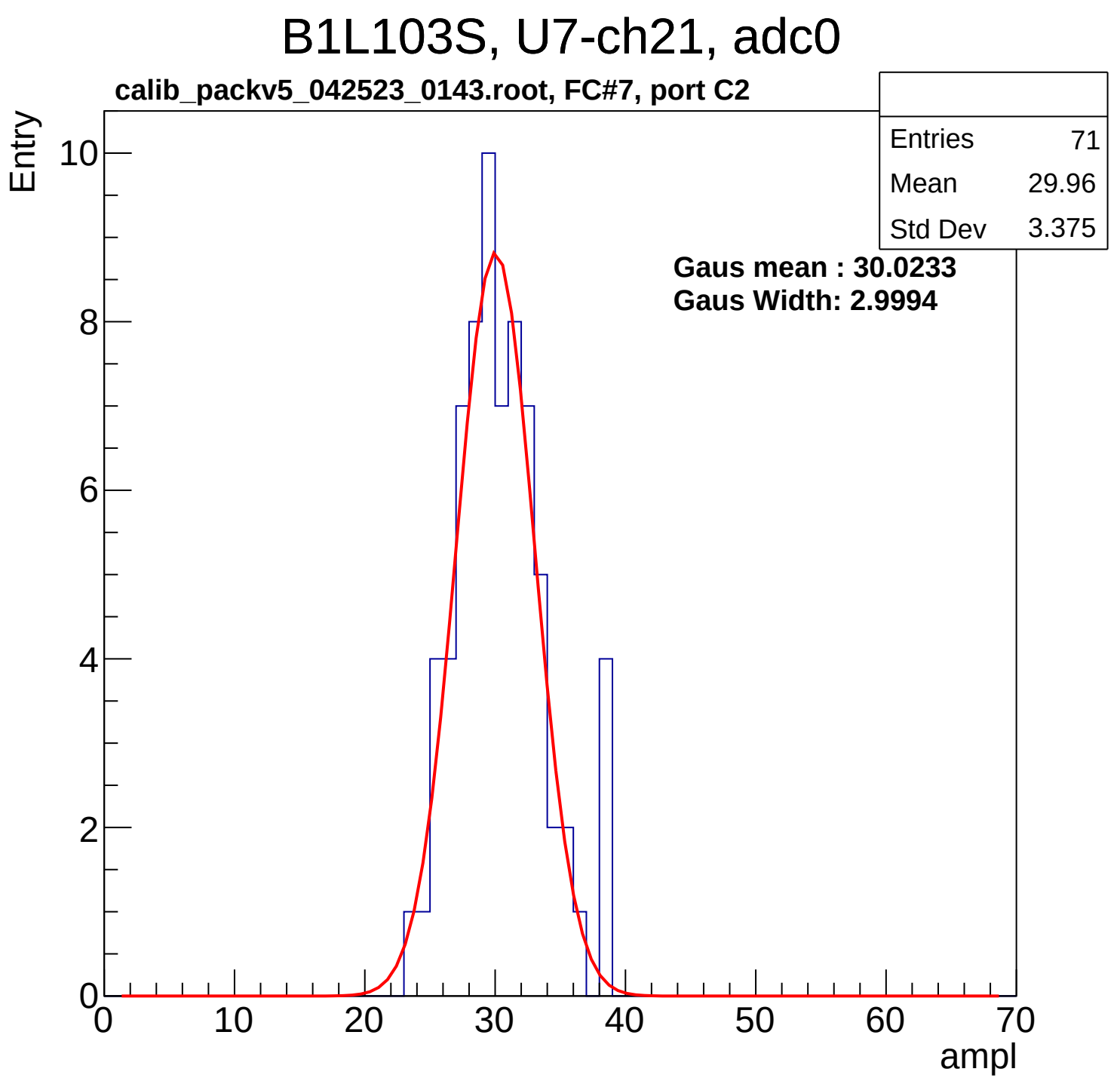
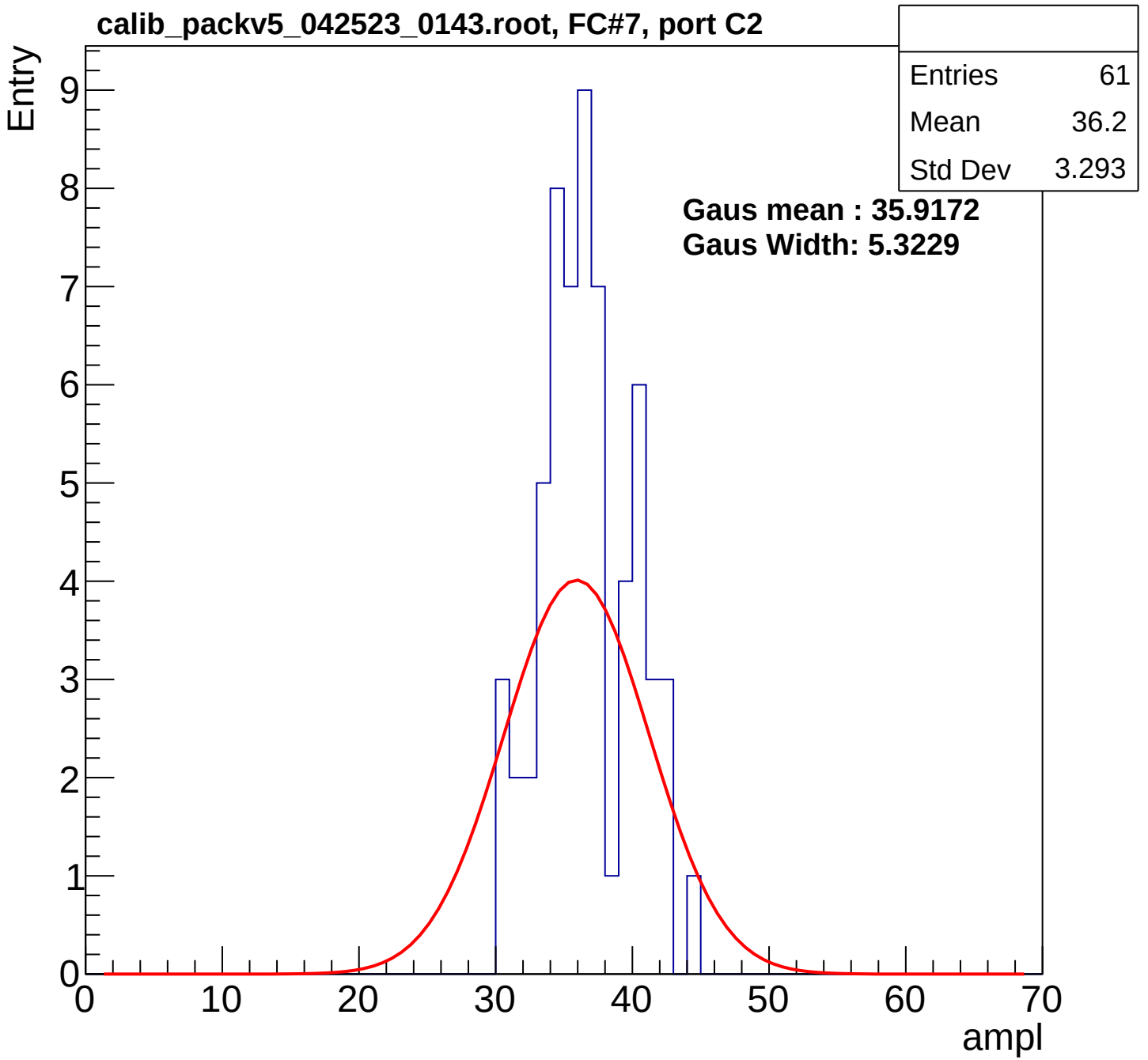
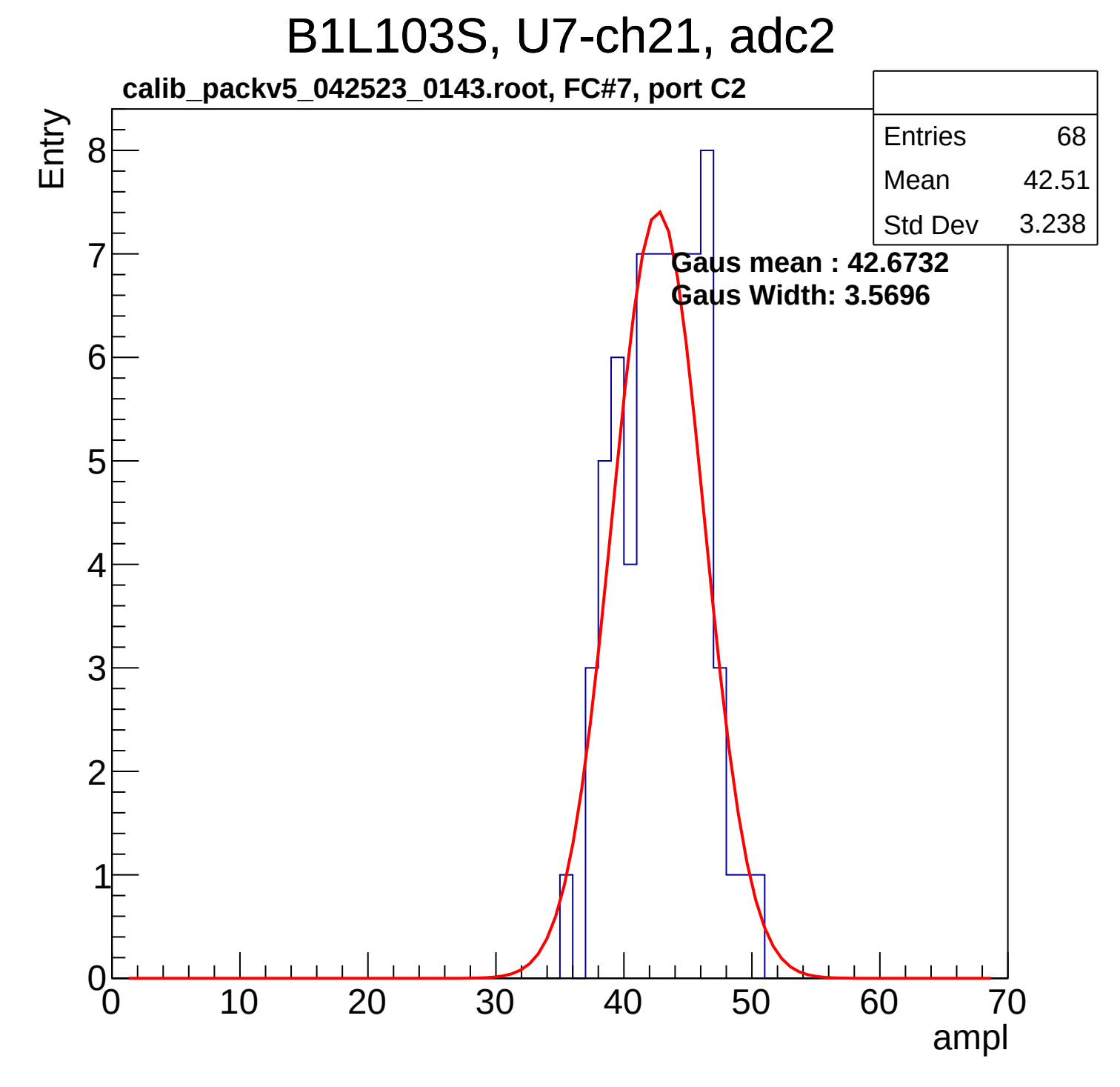

B1L103S, U7-ch20, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 10
Mean 55.5
Std Dev 18.54
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U7-ch20, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 31.5
Std Dev 31.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch21, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 71
Mean 29.96
Std Dev 3.375
Gaus mean : 30.0233
Gaus Width: 2.9994
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch21, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 61
Mean 36.2
Std Dev 3.293
Gaus mean : 35.9172
Gaus Width: 5.3229
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch21, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 42.51
Std Dev 3.238
Gaus mean : 42.6732
Gaus Width: 3.5696
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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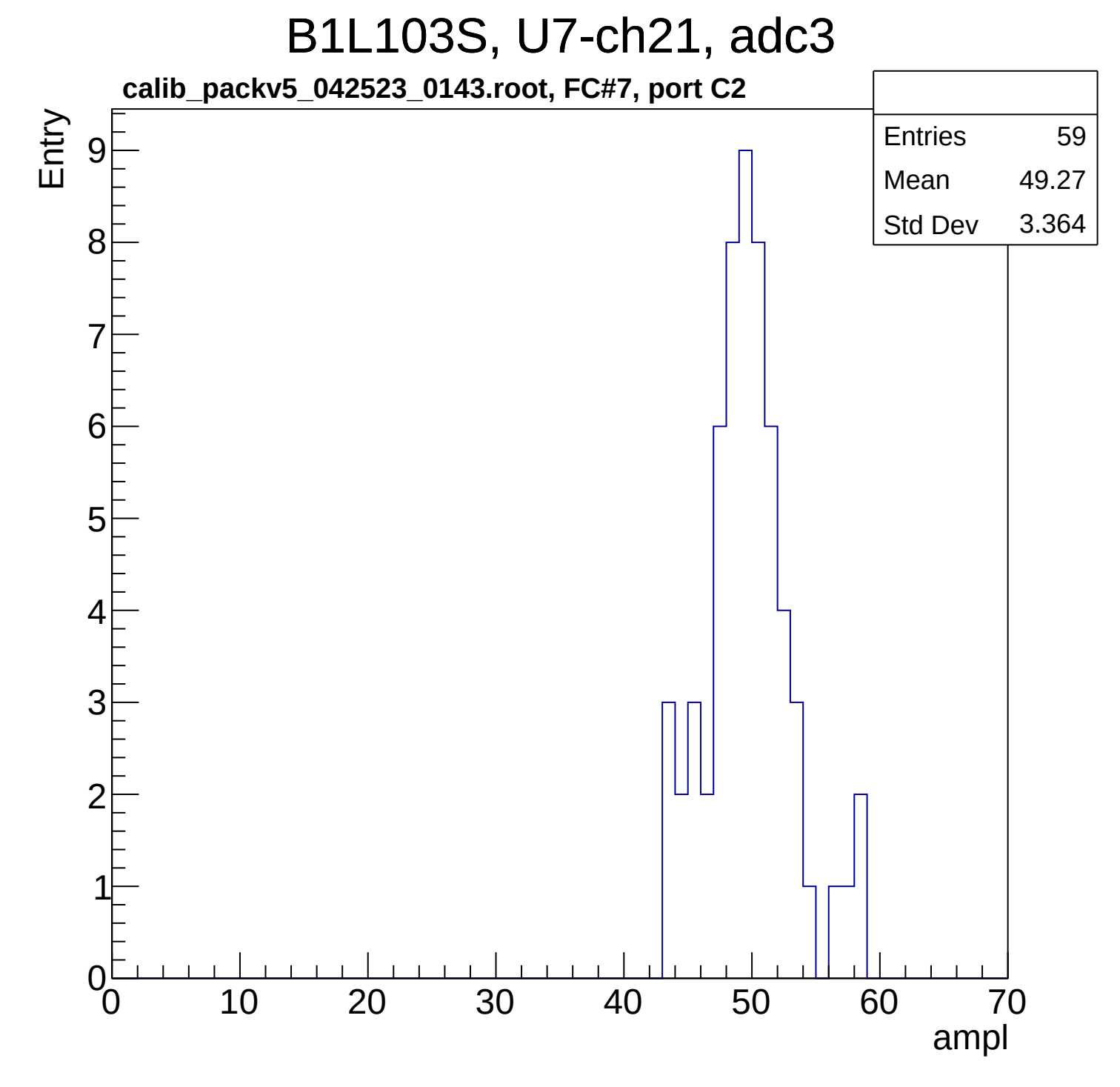
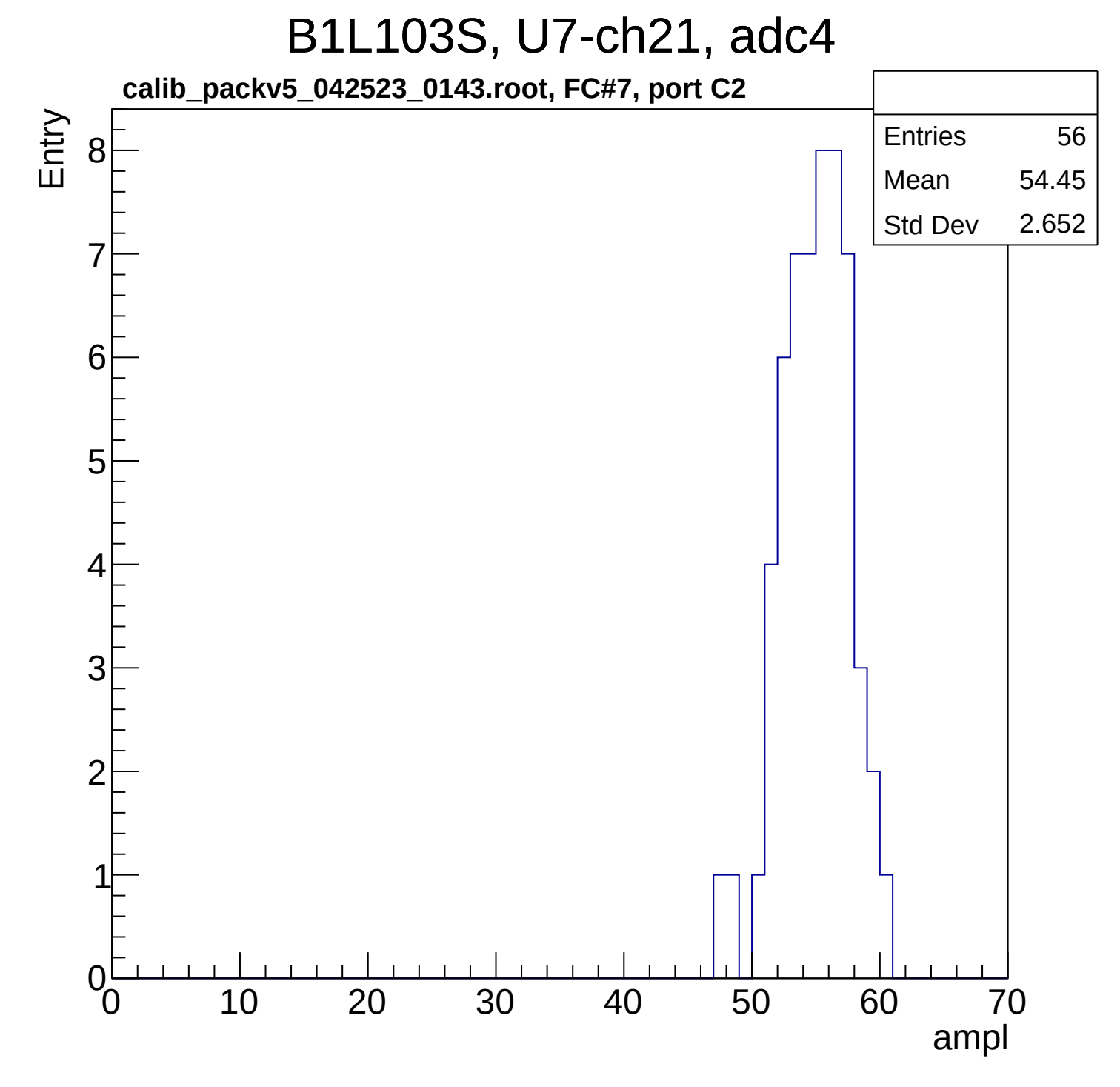

B1L103S, U7-ch21, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 49.27
Std Dev 3.364
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch21, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 54.45
Std Dev 2.652
Entry
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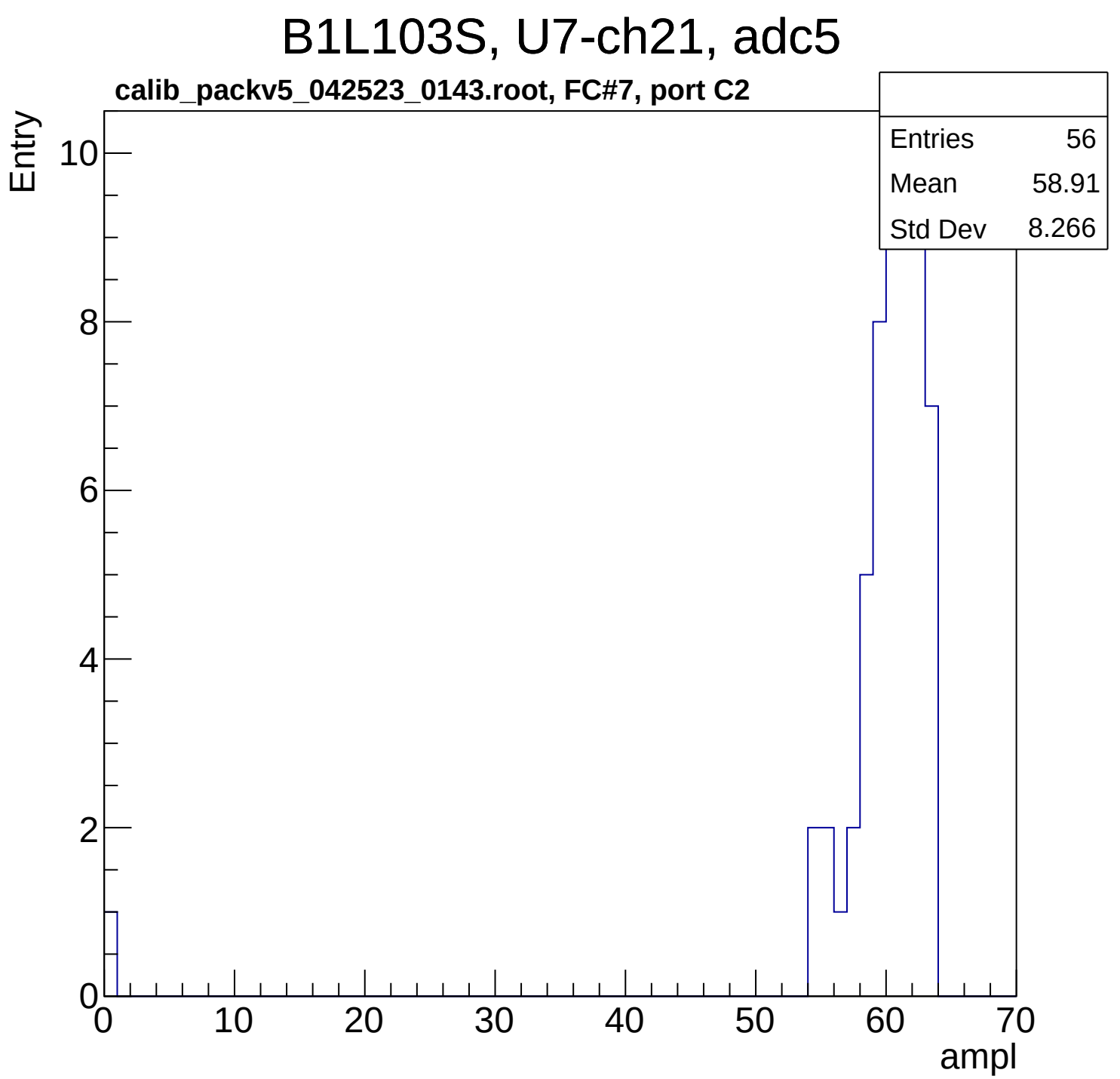
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch21, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 58.91
Std Dev 8.266
Entry
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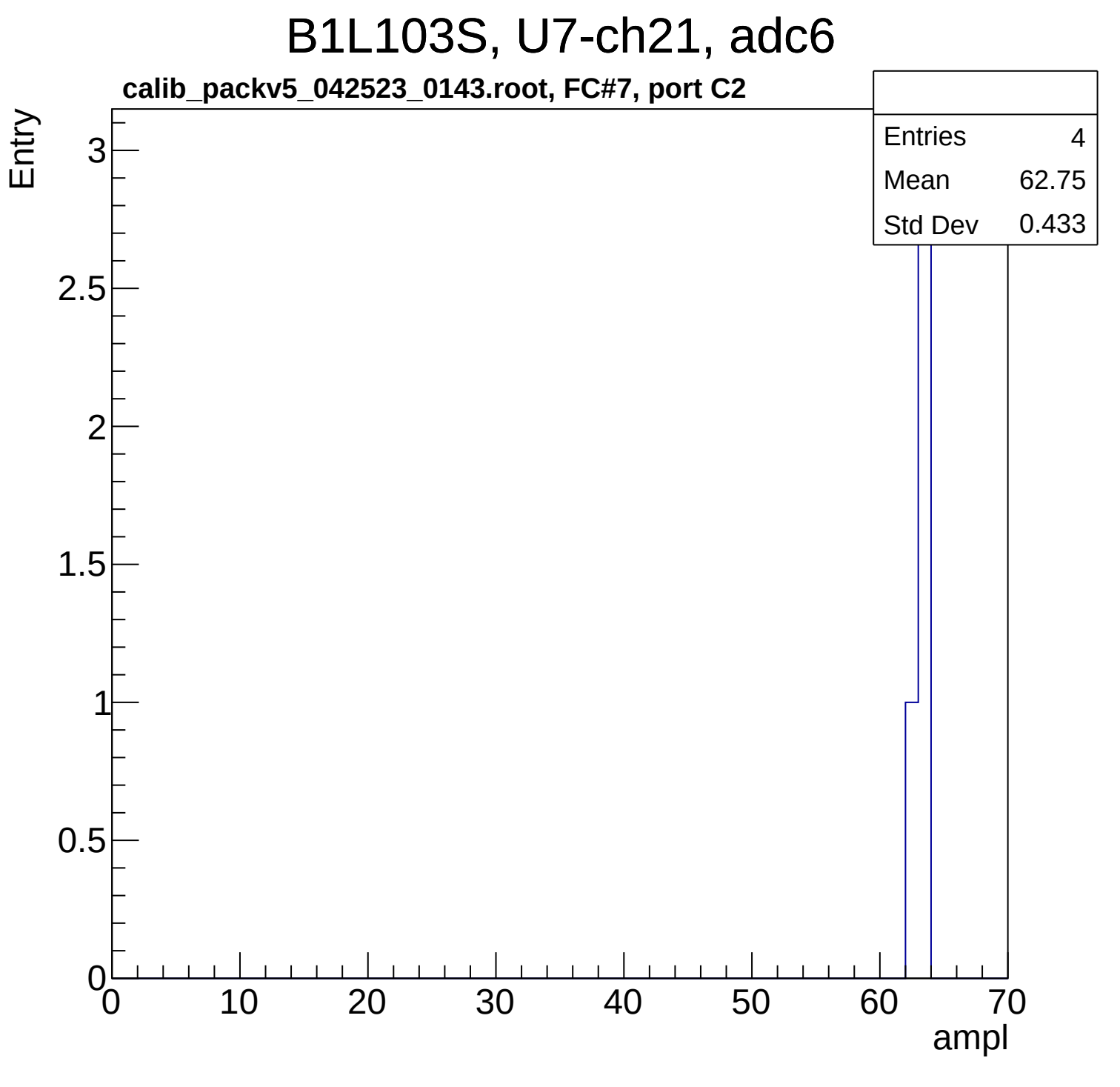
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch21, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 4
Mean 62.75
Std Dev 0.433
Entry
ampl
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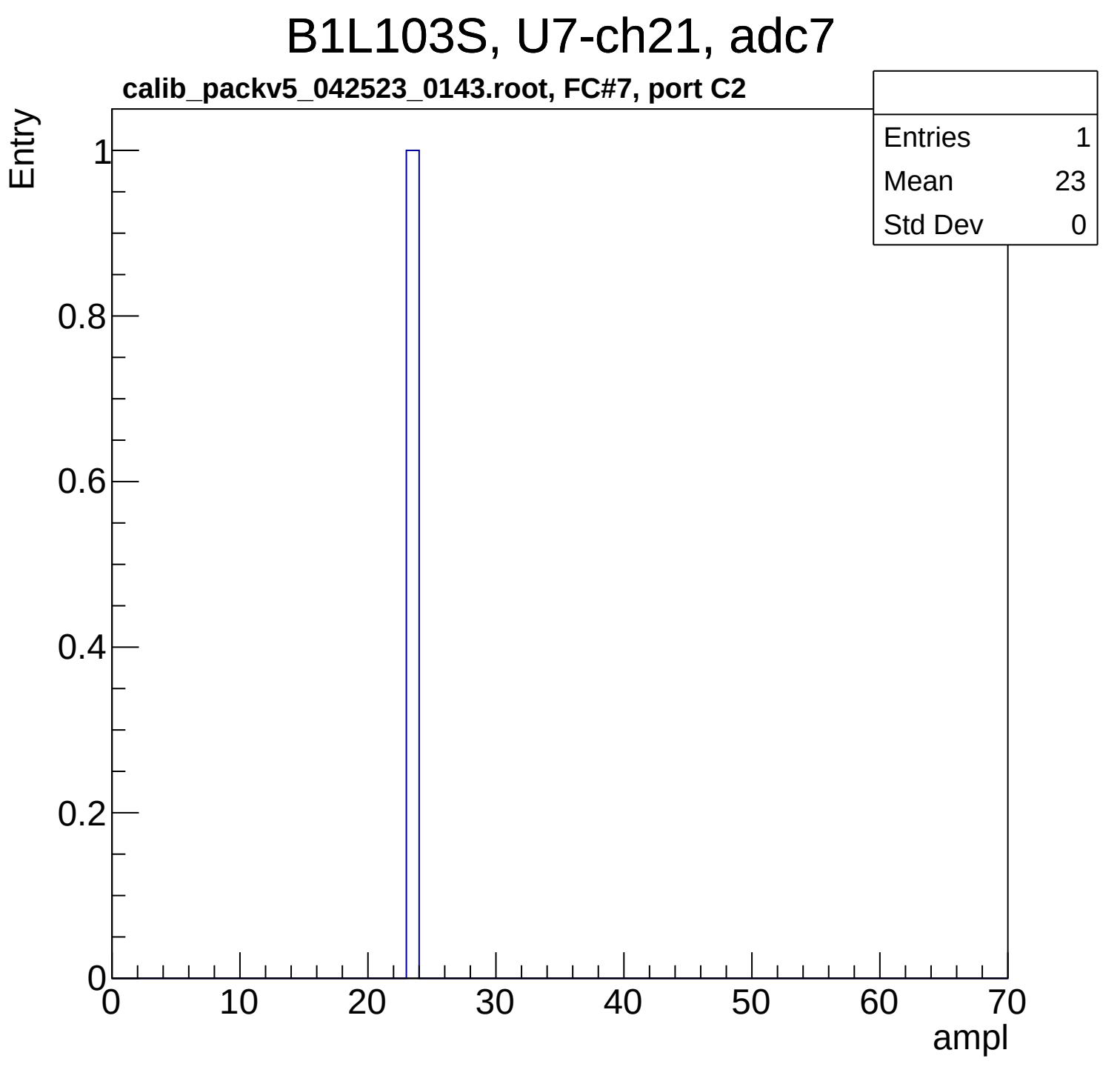
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U7-ch21, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 23
Std Dev 0
Entry
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0.6
0.4
0.2
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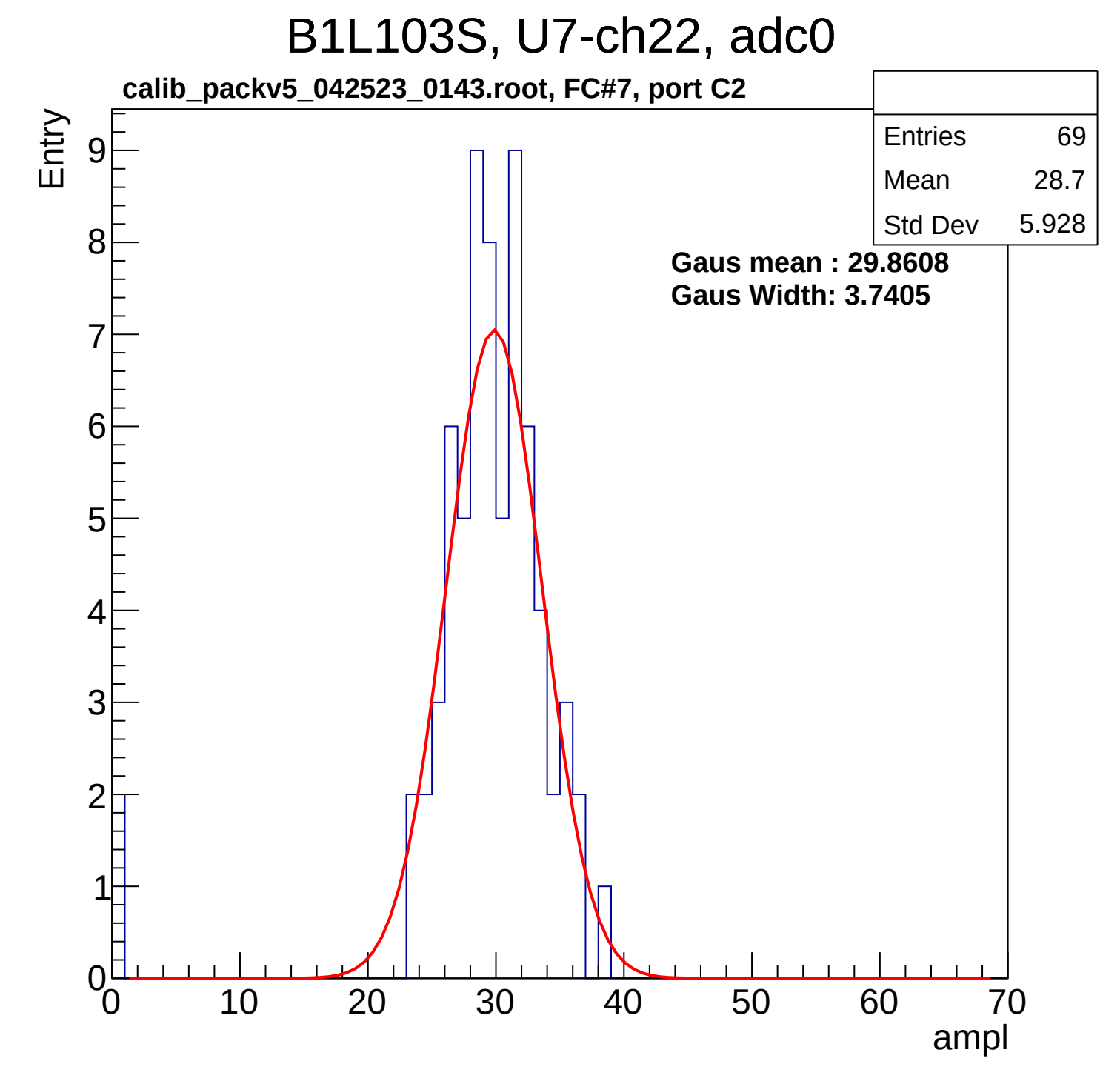
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch22, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 28.7
Std Dev 5.928
Gaus mean : 29.8608
Gaus Width: 3.7405
Entry
ampl
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2
3
4
5
6
7
8
9
0
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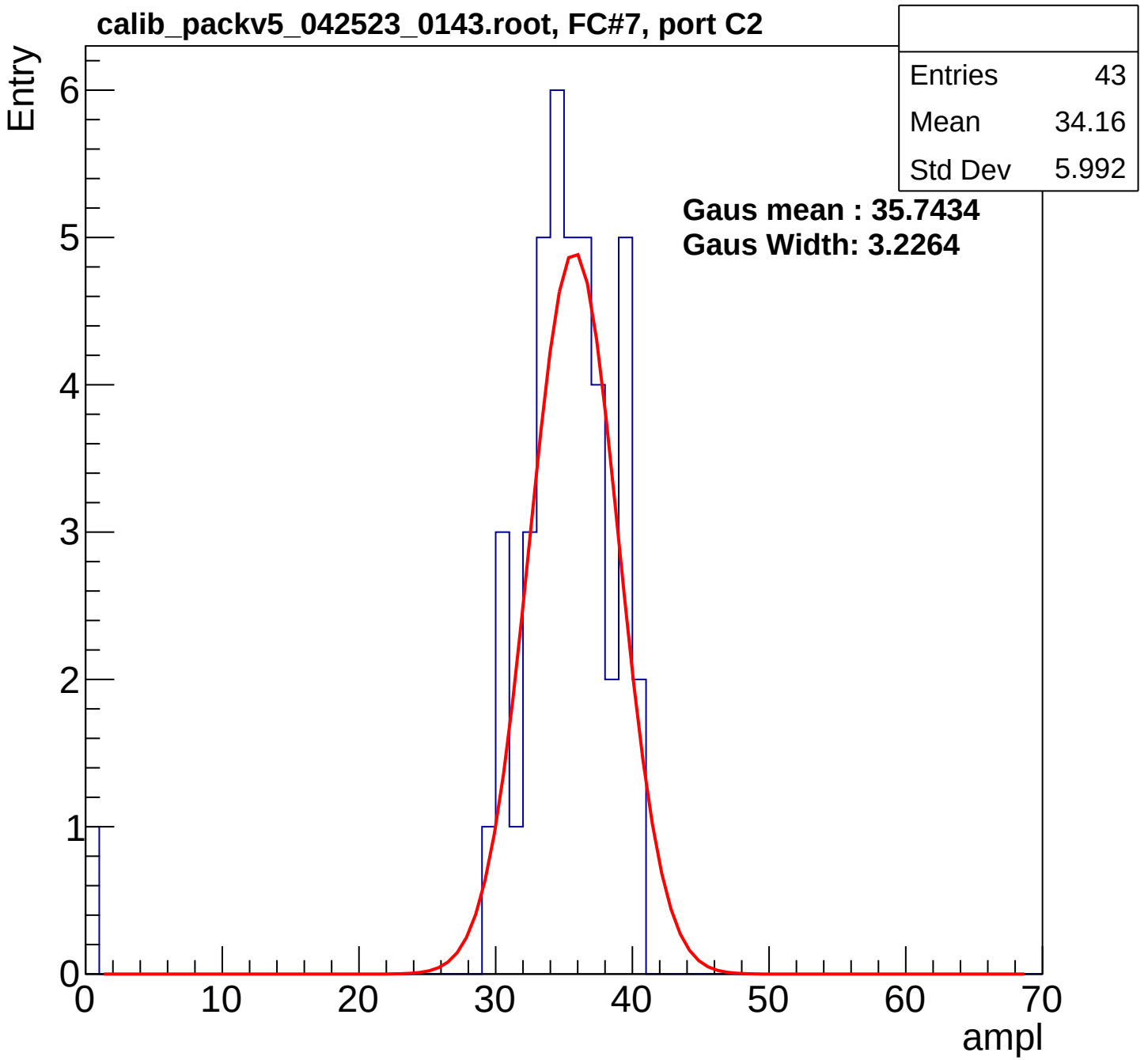
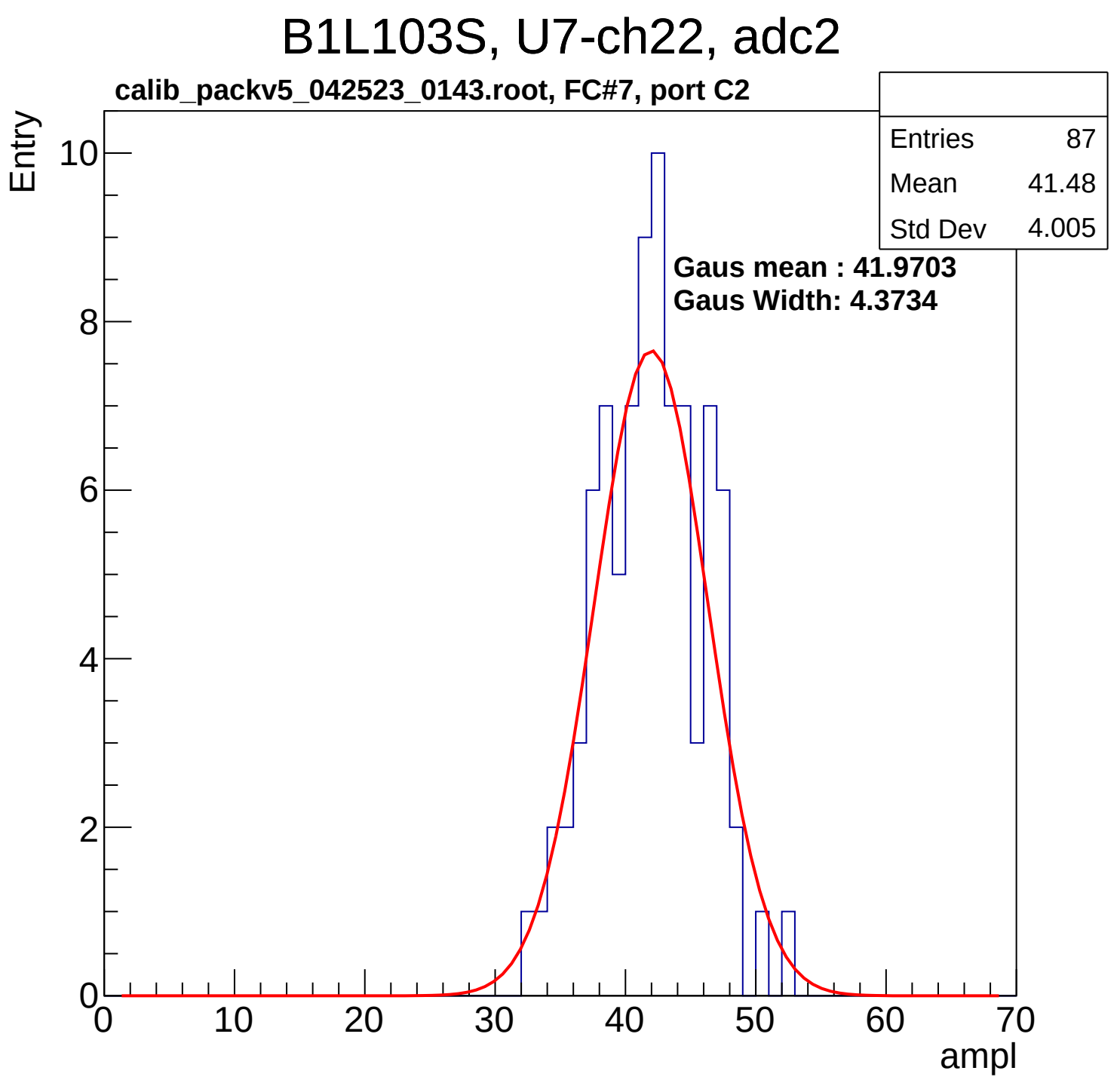
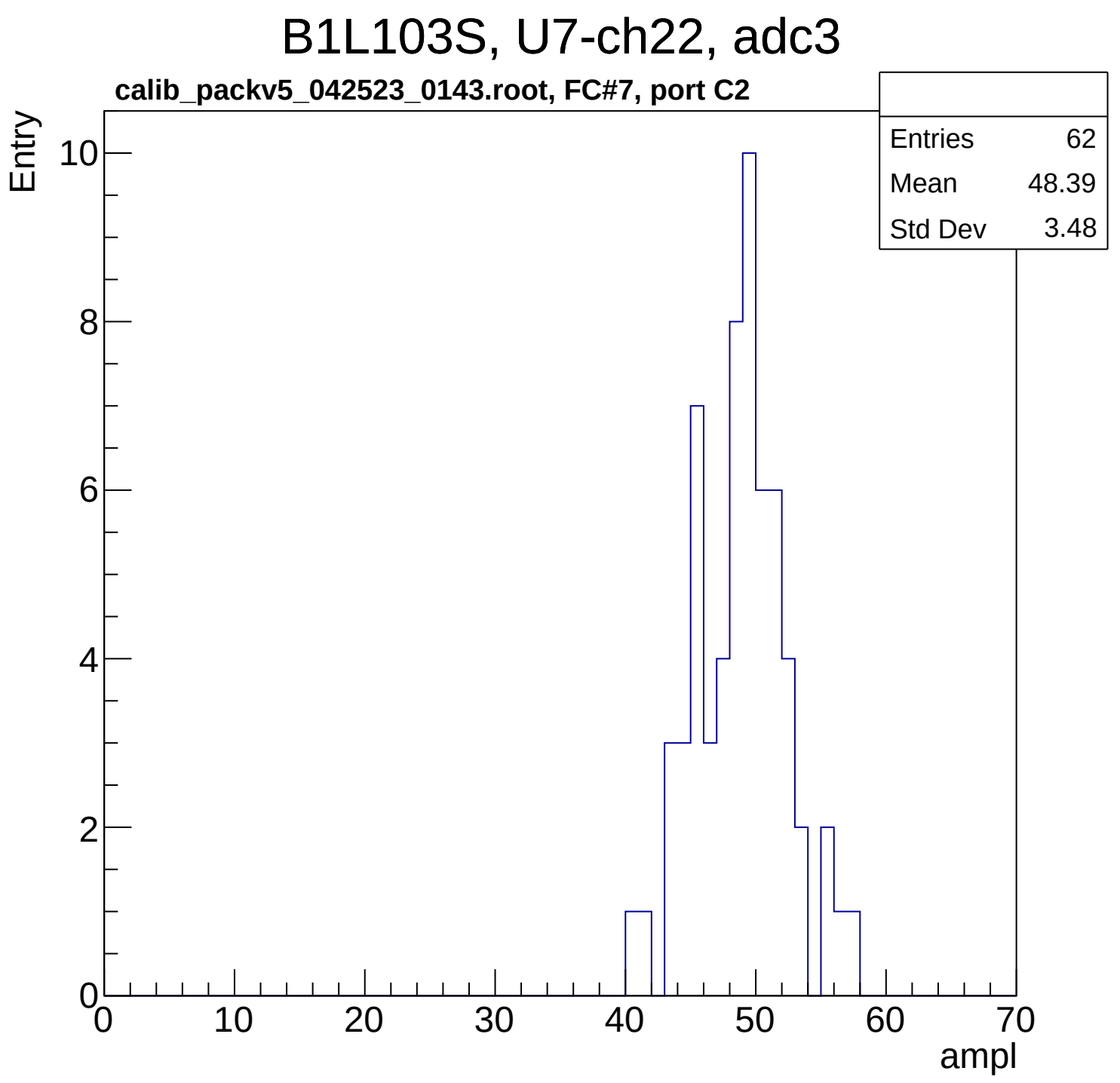
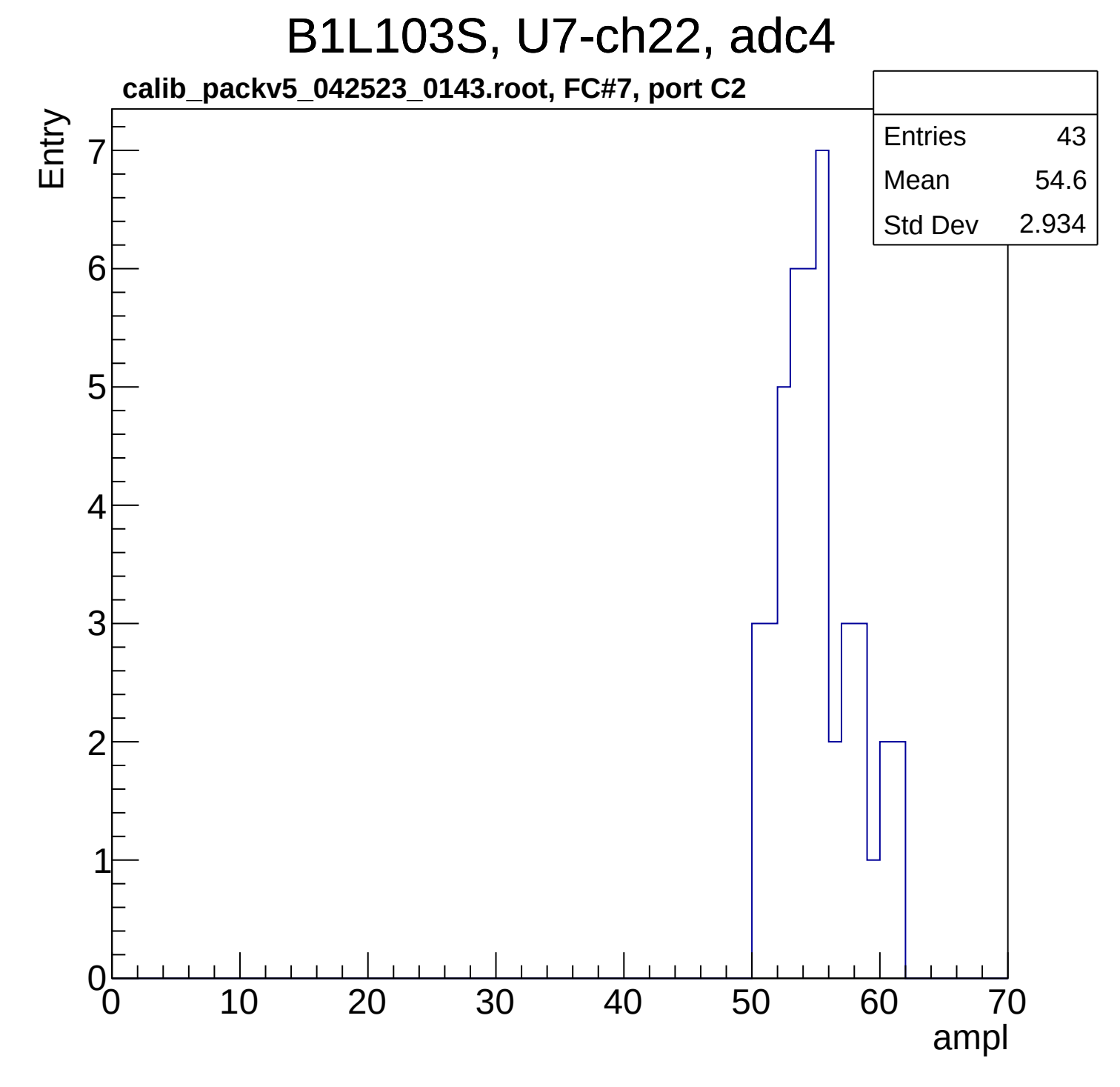
60
70


B1L103S, U7-ch22, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 43
Mean 34.16
Std Dev 5.992
Gaus mean : 35.7434
Gaus Width: 3.2264
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U7-ch22, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 87
Mean 41.48
Std Dev 4.005
Gaus mean : 41.9703
Gaus Width: 4.3734
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch22, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 62
Mean 48.39
Std Dev 3.48
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch22, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 43
Mean 54.6
Std Dev 2.934
Entry
ampl
0
1
2
3
4
5
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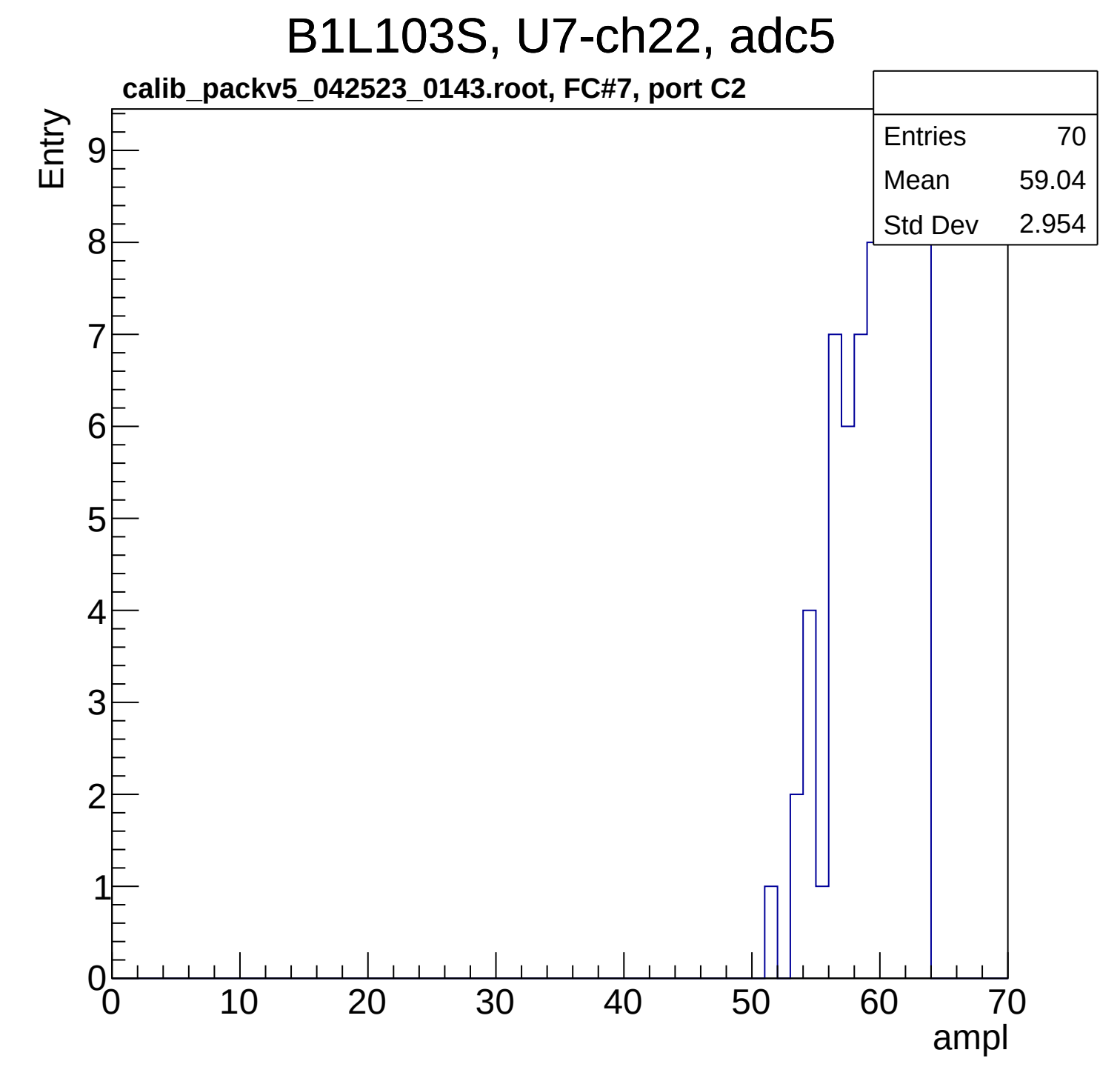
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch22, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 59.04
Std Dev 2.954
Entry
ampl
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3
4
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6
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0
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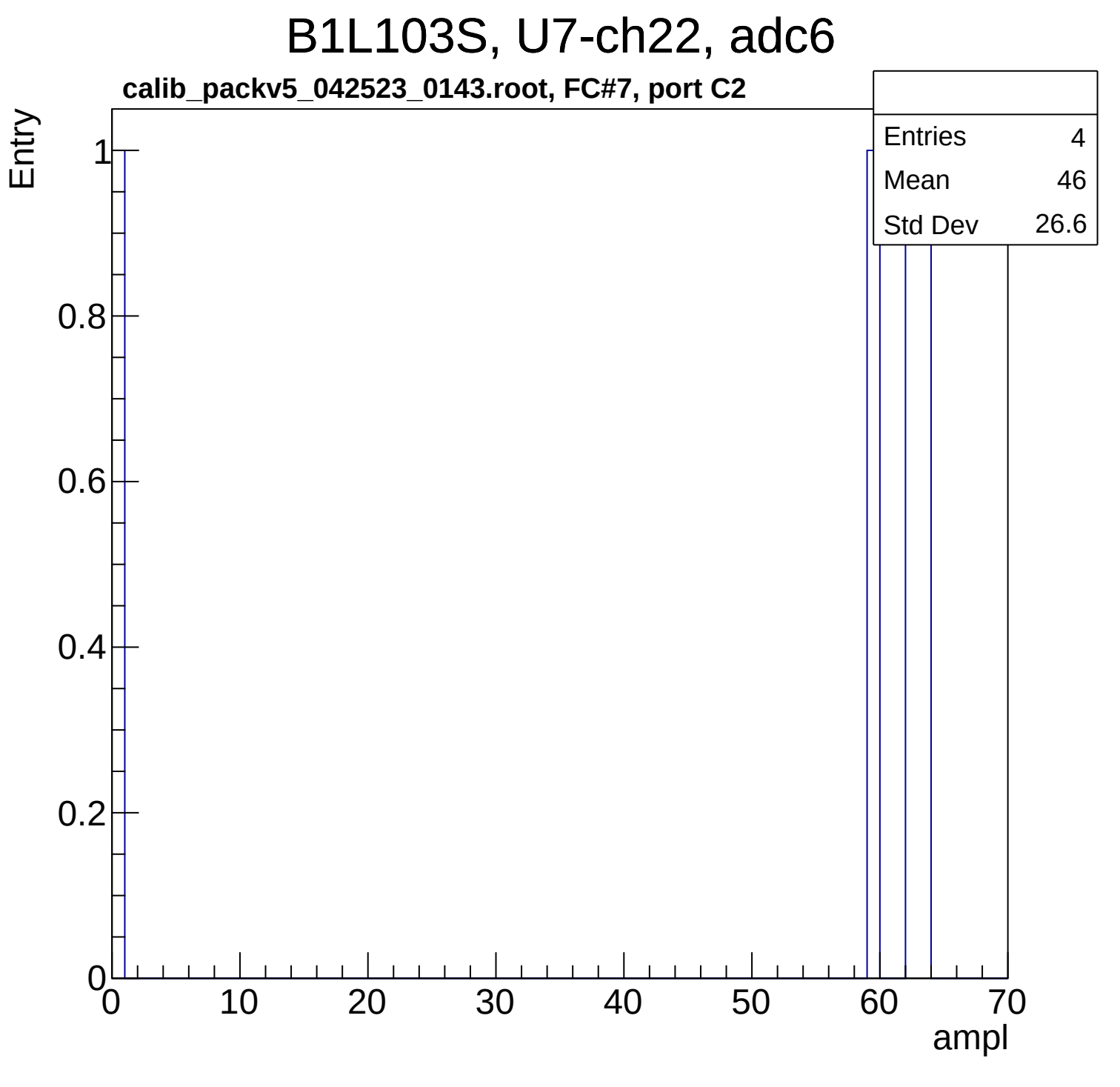
B1L103S, U7-ch22, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 4
Mean 46
Std Dev 26.6
Entry
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10
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40
50
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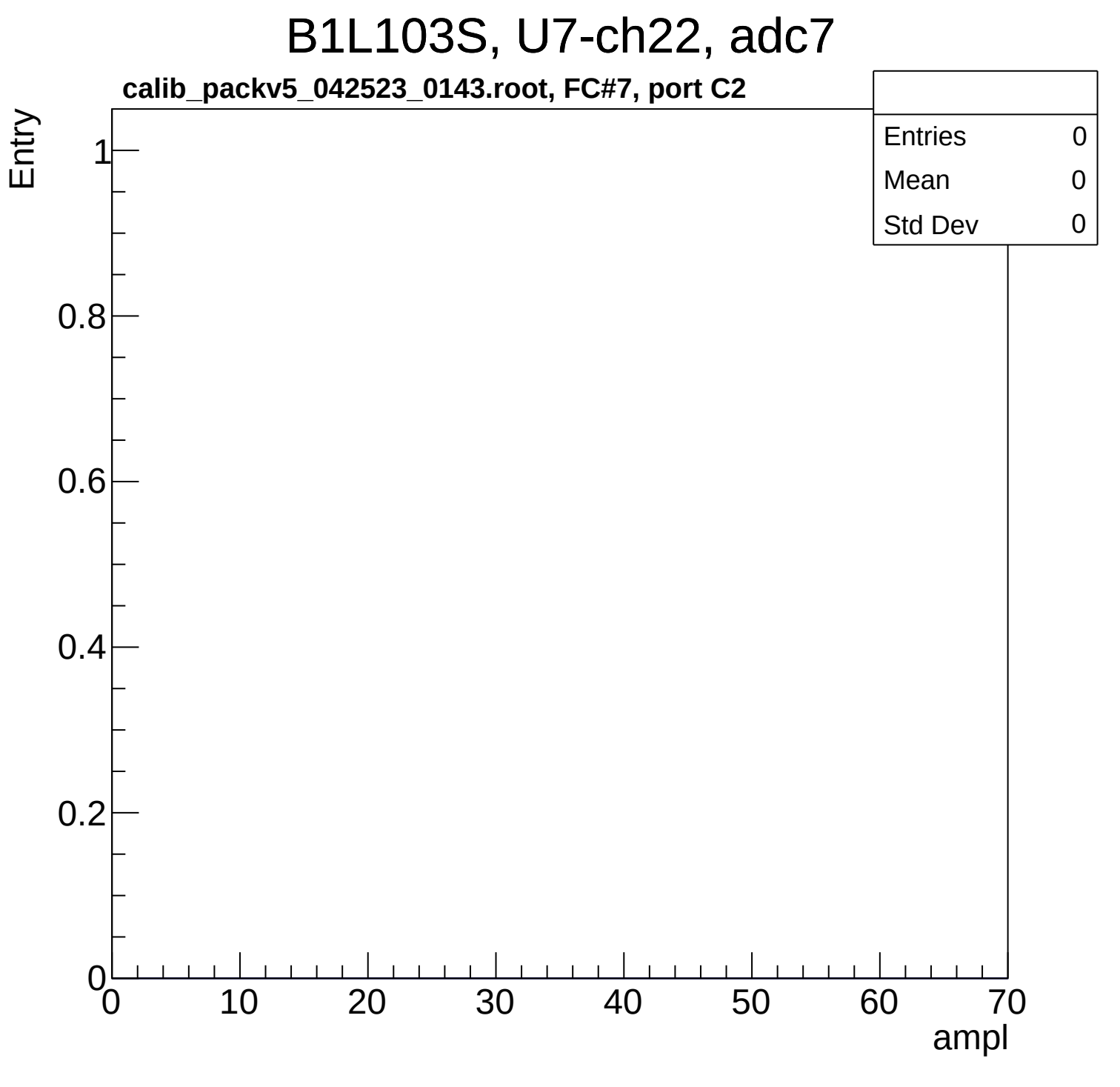
70
ampl


B1L103S, U7-ch22, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
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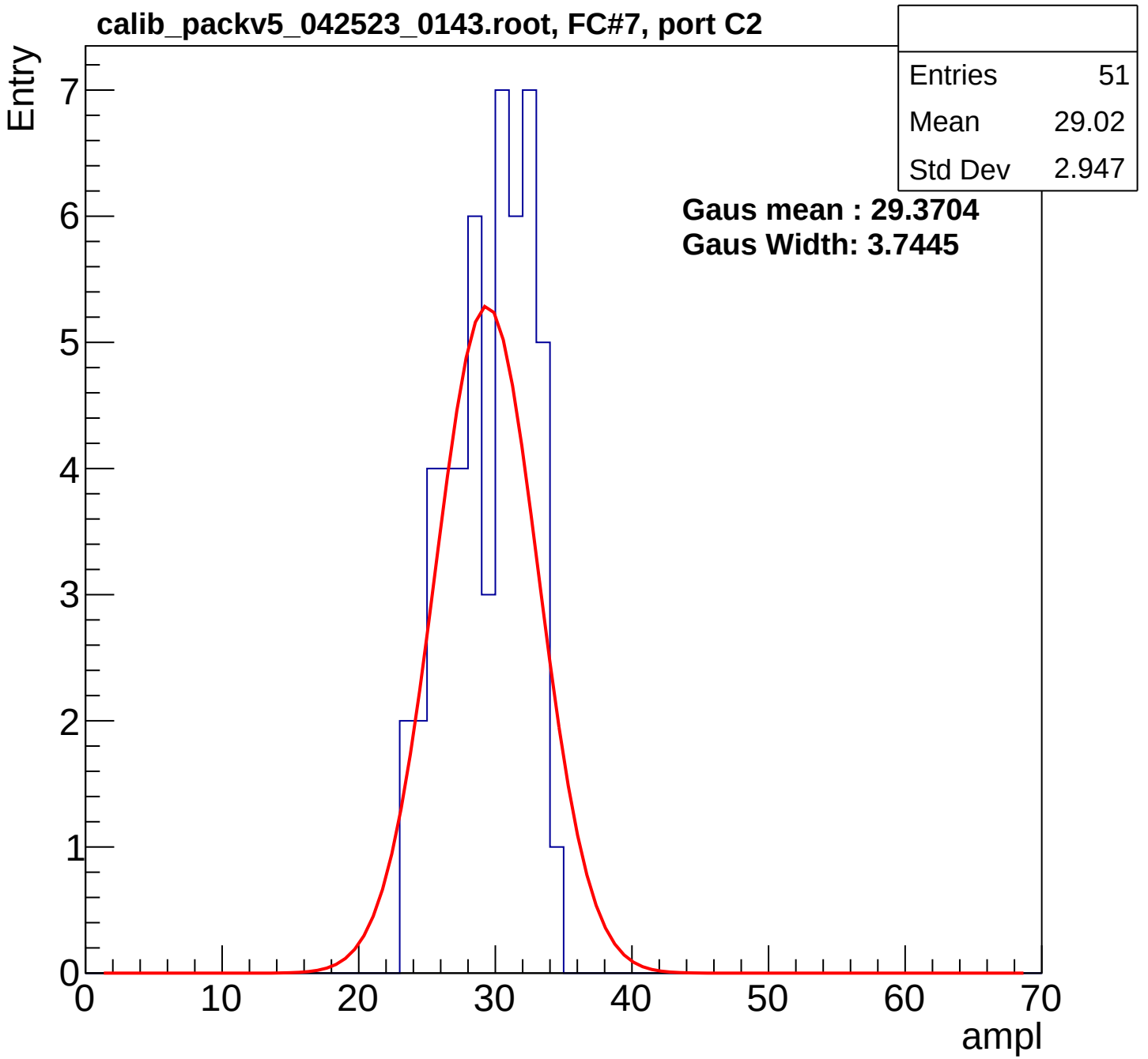
50
60
70
ampl


B1L103S, U7-ch23, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 51
Mean 29.02
Std Dev 2.947
Gaus mean : 29.3704
Gaus Width: 3.7445
Entry
ampl
0
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2
3
4
5
6
7
0
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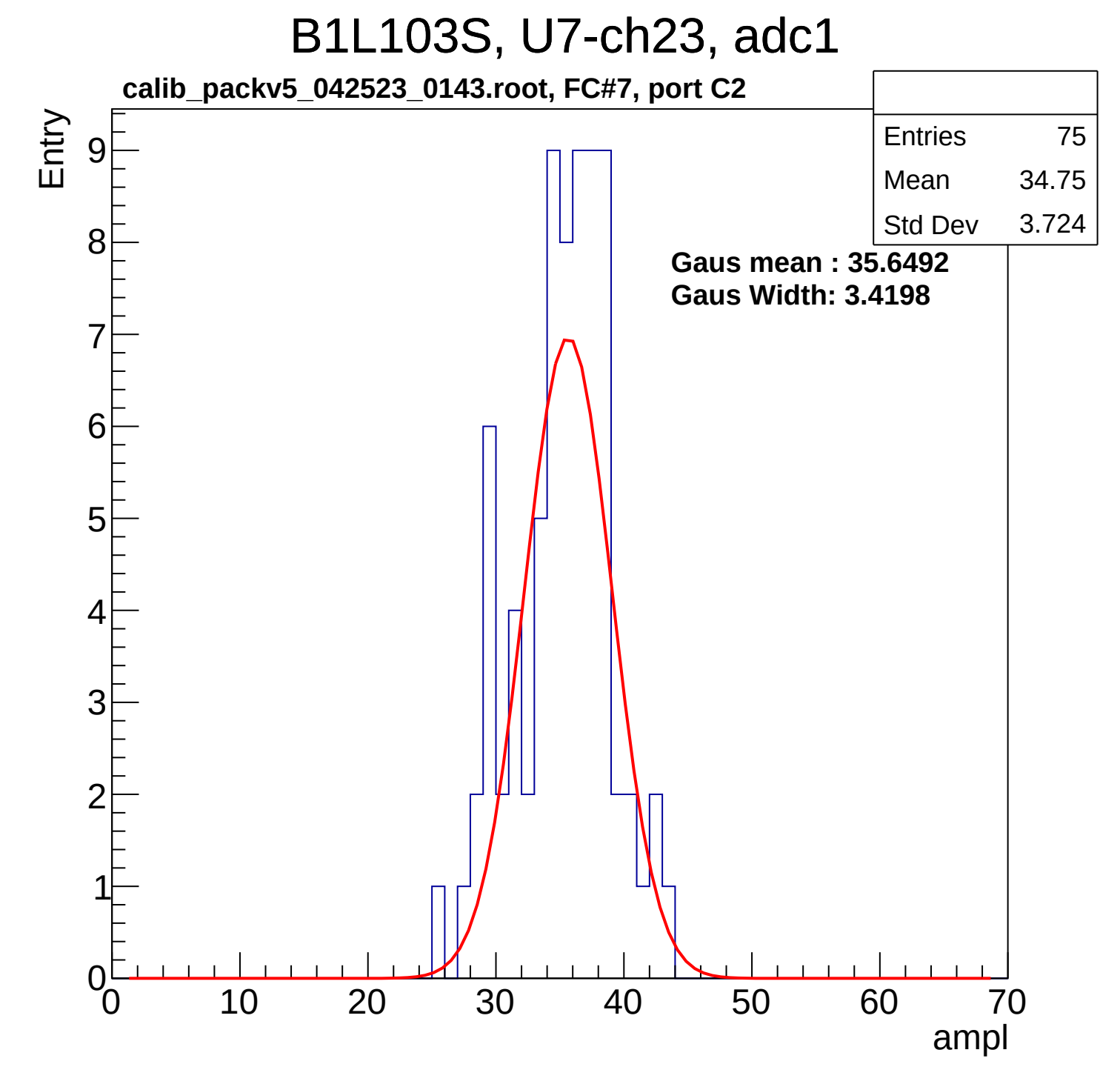
30
40
50
60
70


B1L103S, U7-ch23, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 75
Mean 34.75
Std Dev 3.724
Gaus mean : 35.6492
Gaus Width: 3.4198
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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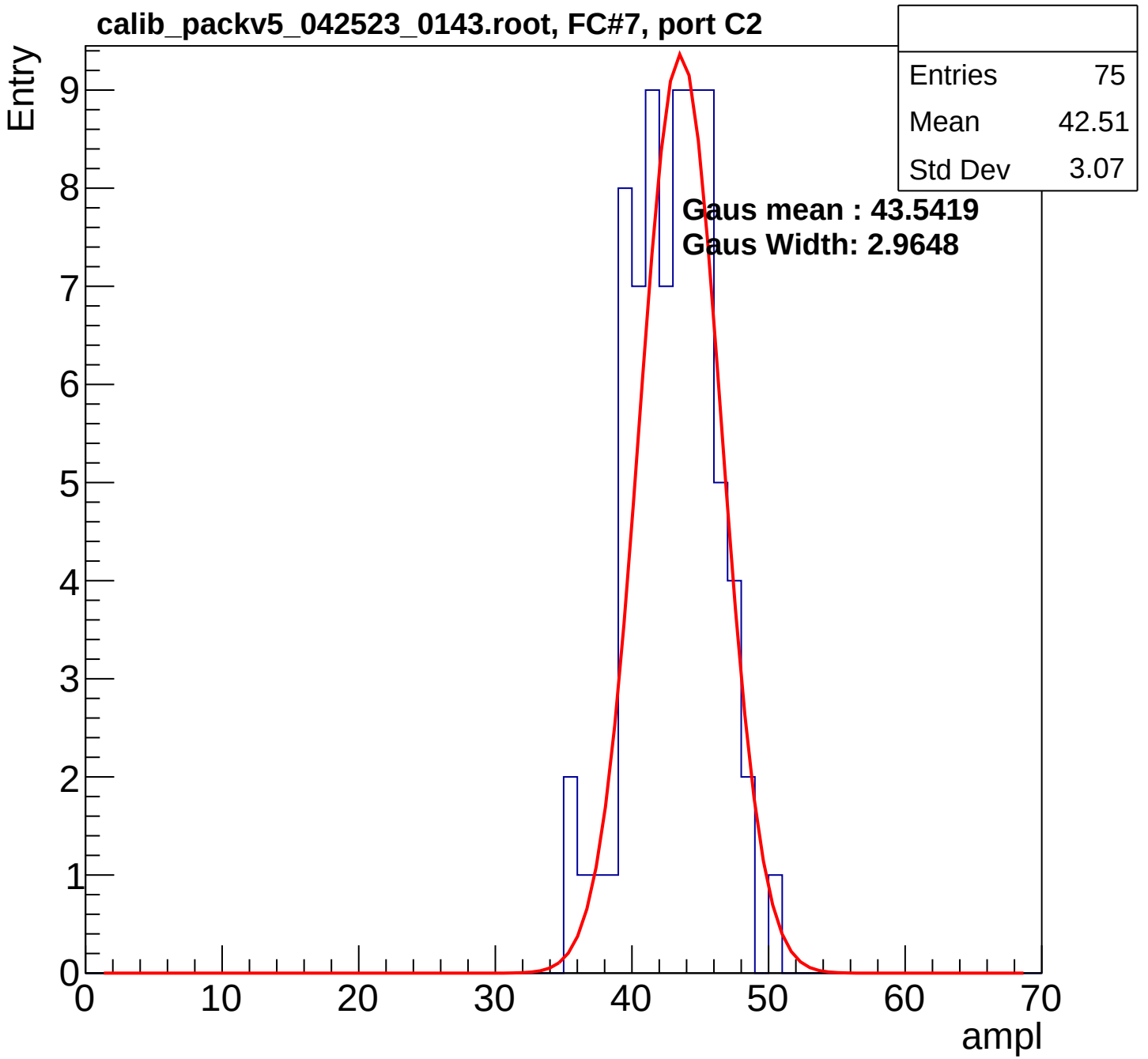
B1L103S, U7-ch23, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 75
Mean 42.51
Std Dev 3.07
Gaus mean : 43.5419
Gaus Width: 2.9648
Entry
ampl
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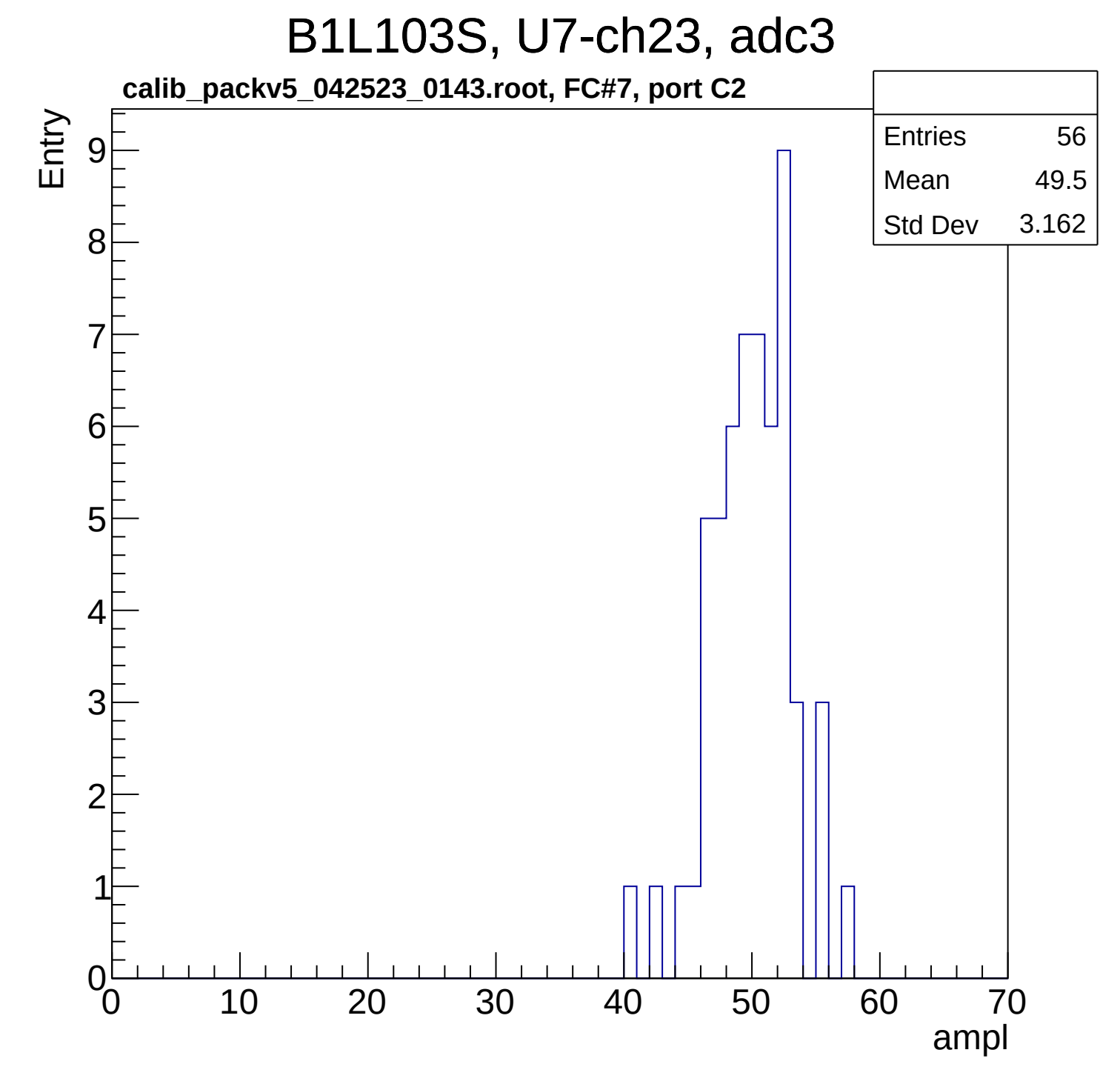
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch23, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 49.5
Std Dev 3.162
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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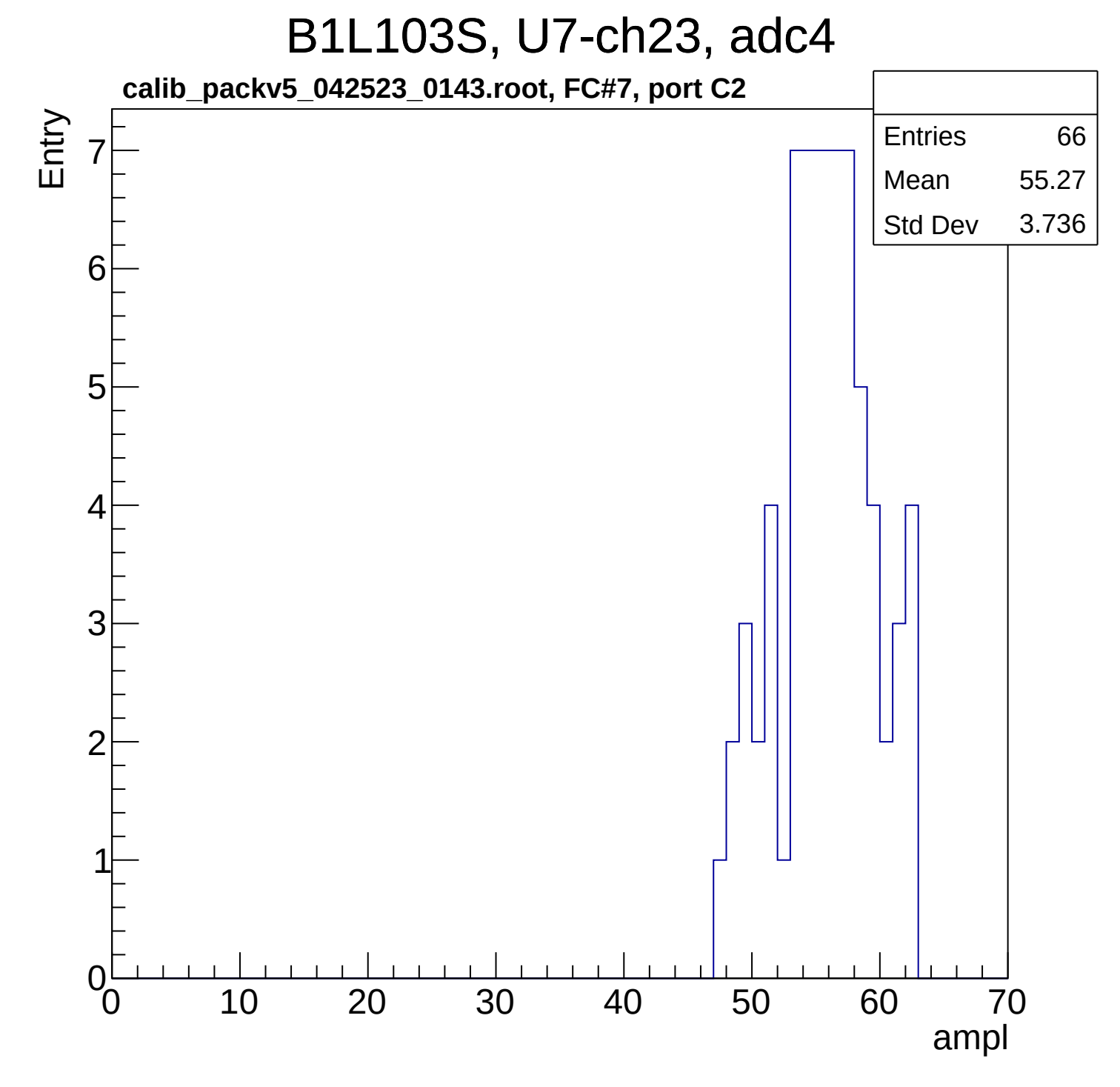
40
50
60
70


B1L103S, U7-ch23, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 55.27
Std Dev 3.736
Entry
ampl
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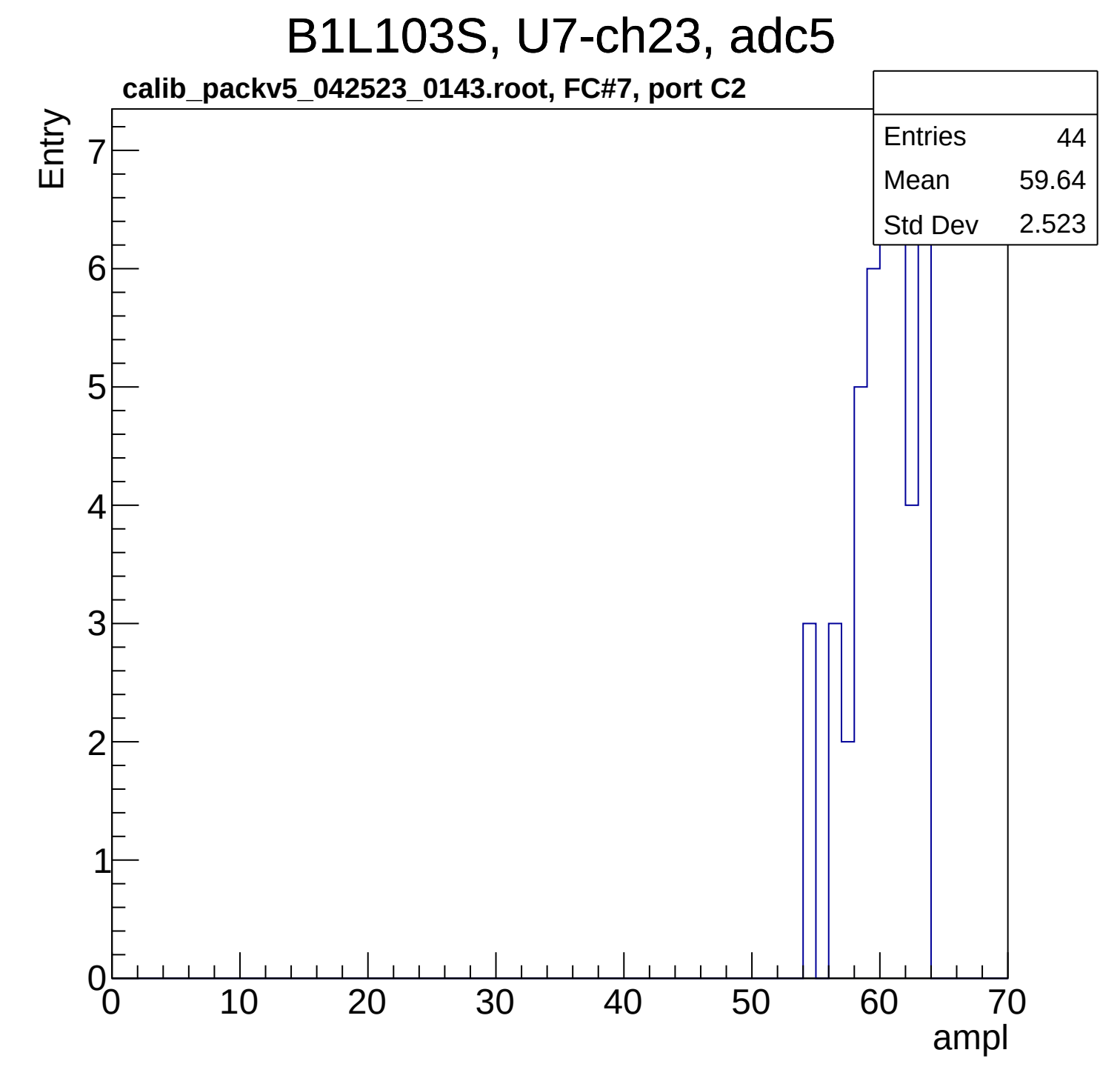
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch23, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 44
Mean 59.64
Std Dev 2.523
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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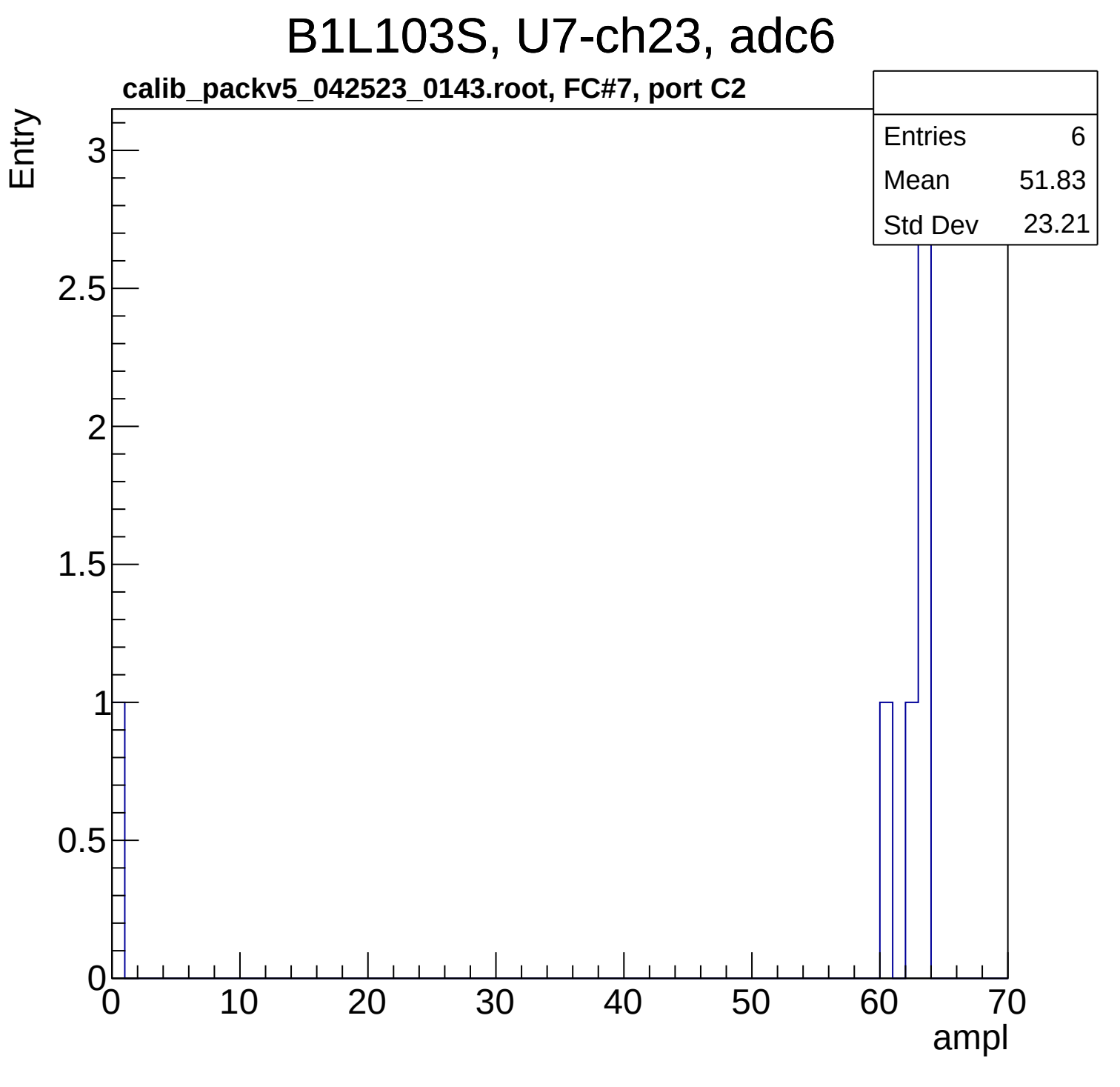
B1L103S, U7-ch23, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 6
Mean 51.83
Std Dev 23.21
Entry
ampl
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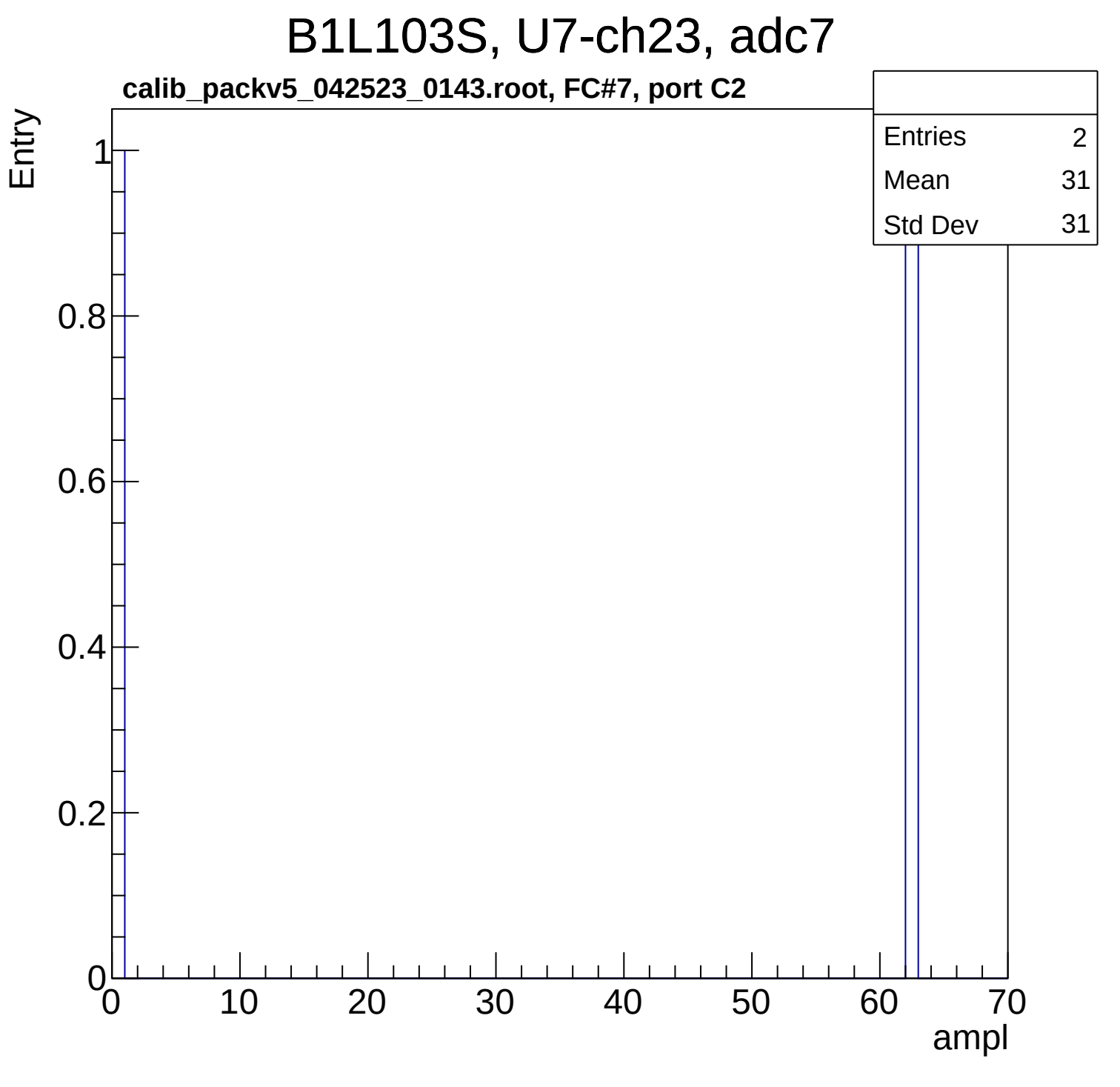
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U7-ch23, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 31
Std Dev 31
Entry
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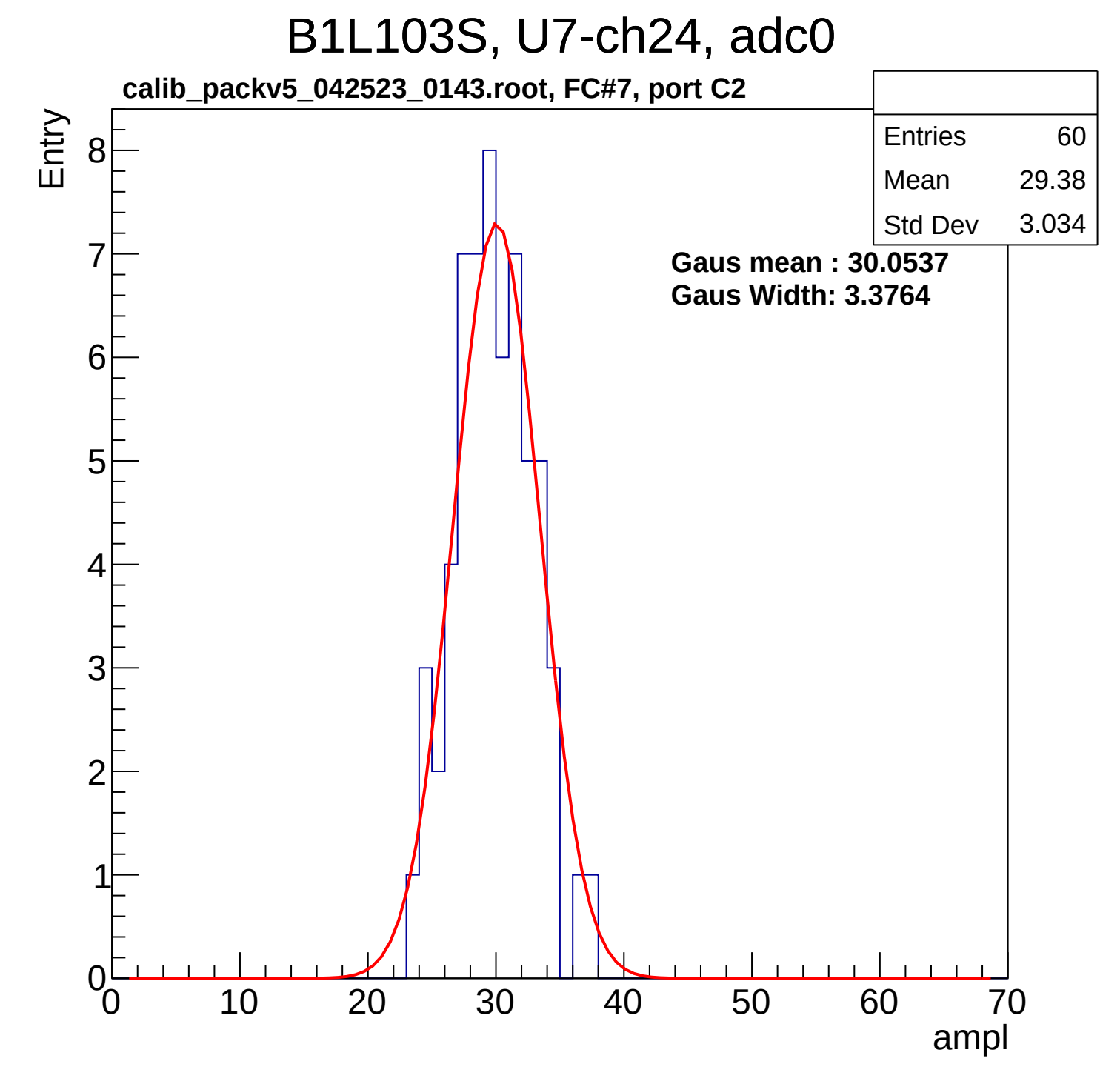
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch24, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 60
Mean 29.38
Std Dev 3.034
Gaus mean : 30.0537
Gaus Width: 3.3764
Entry
ampl
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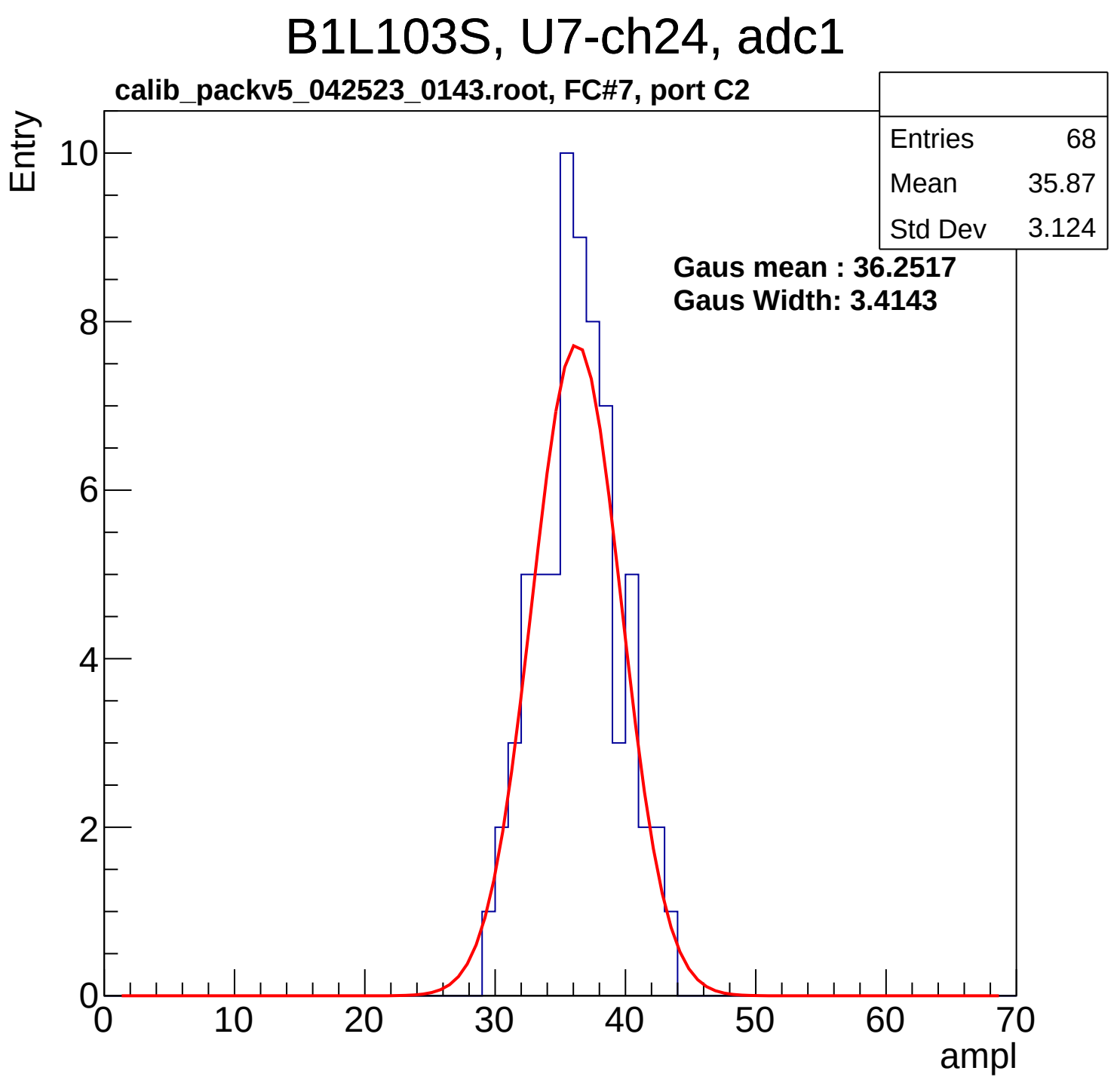
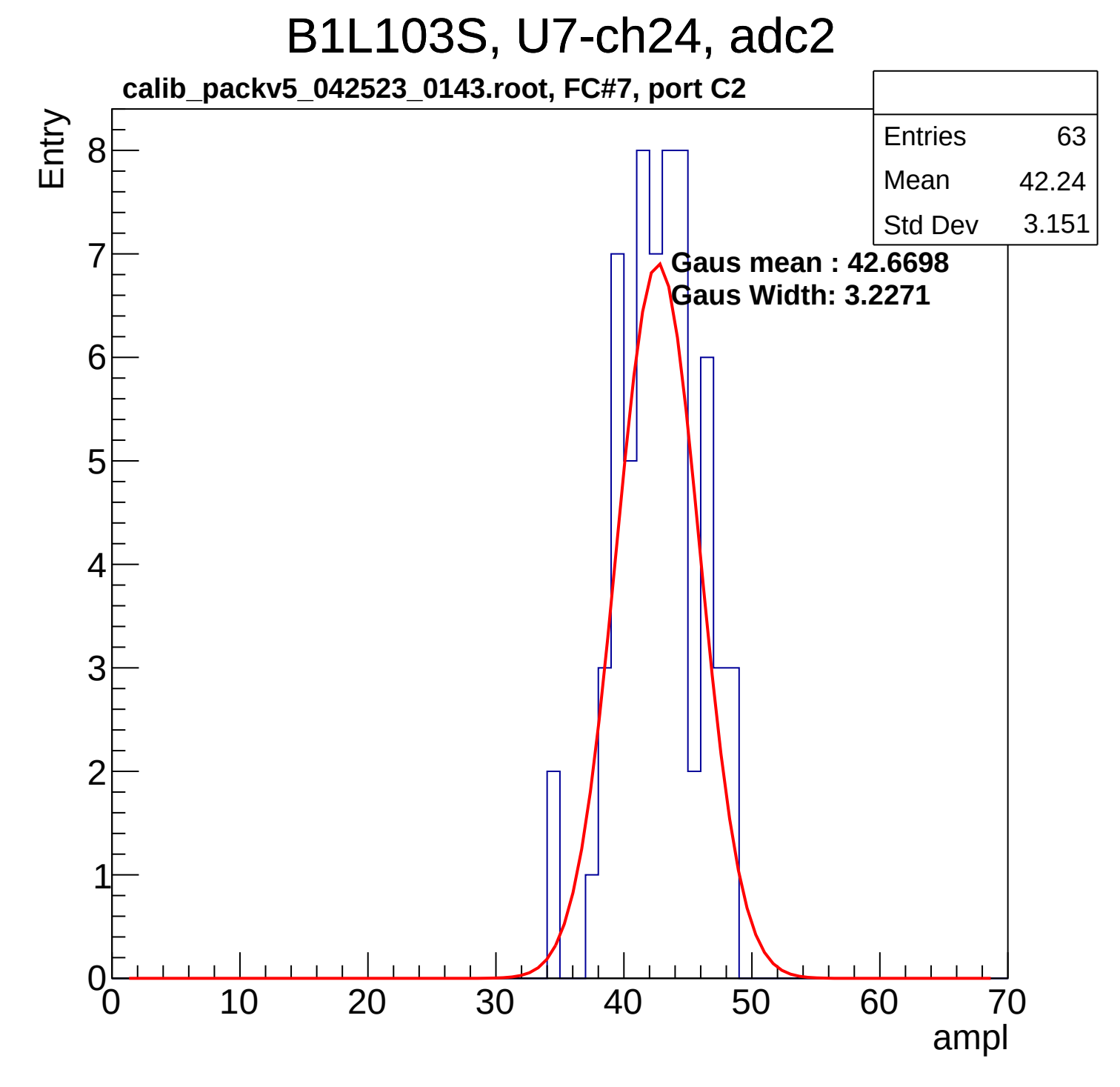
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch24, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 35.87
Std Dev 3.124
Gaus mean : 36.2517
Gaus Width: 3.4143
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch24, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 42.24
Std Dev 3.151
Gaus mean : 42.6698
Gaus Width: 3.2271
Entry
ampl
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1
2
3
4
5
6
7
8
0
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40
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60
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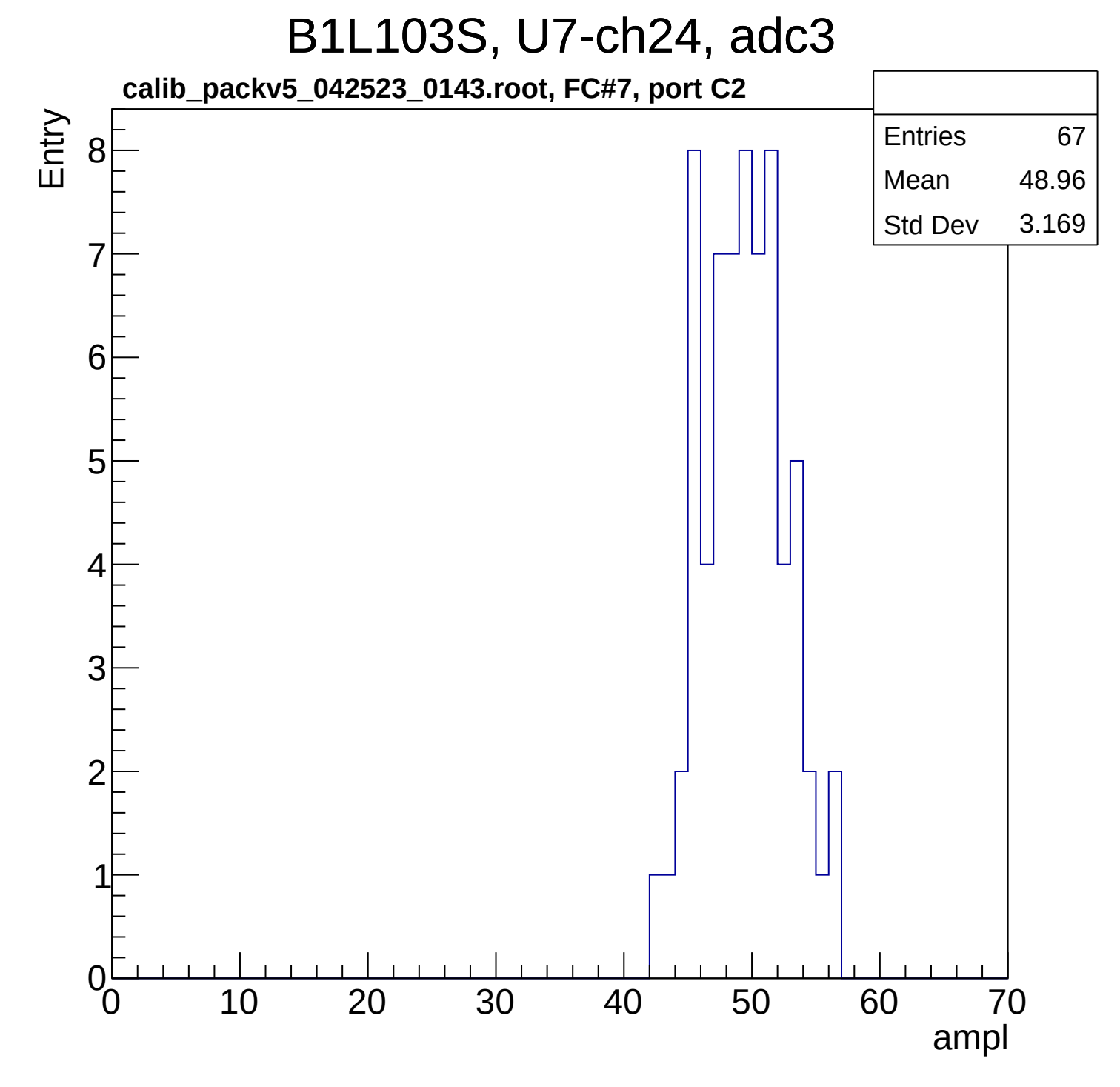
B1L103S, U7-ch24, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 48.96
Std Dev 3.169
Entry
ampl
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1
2
3
4
5
6
7
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0
10
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30
40
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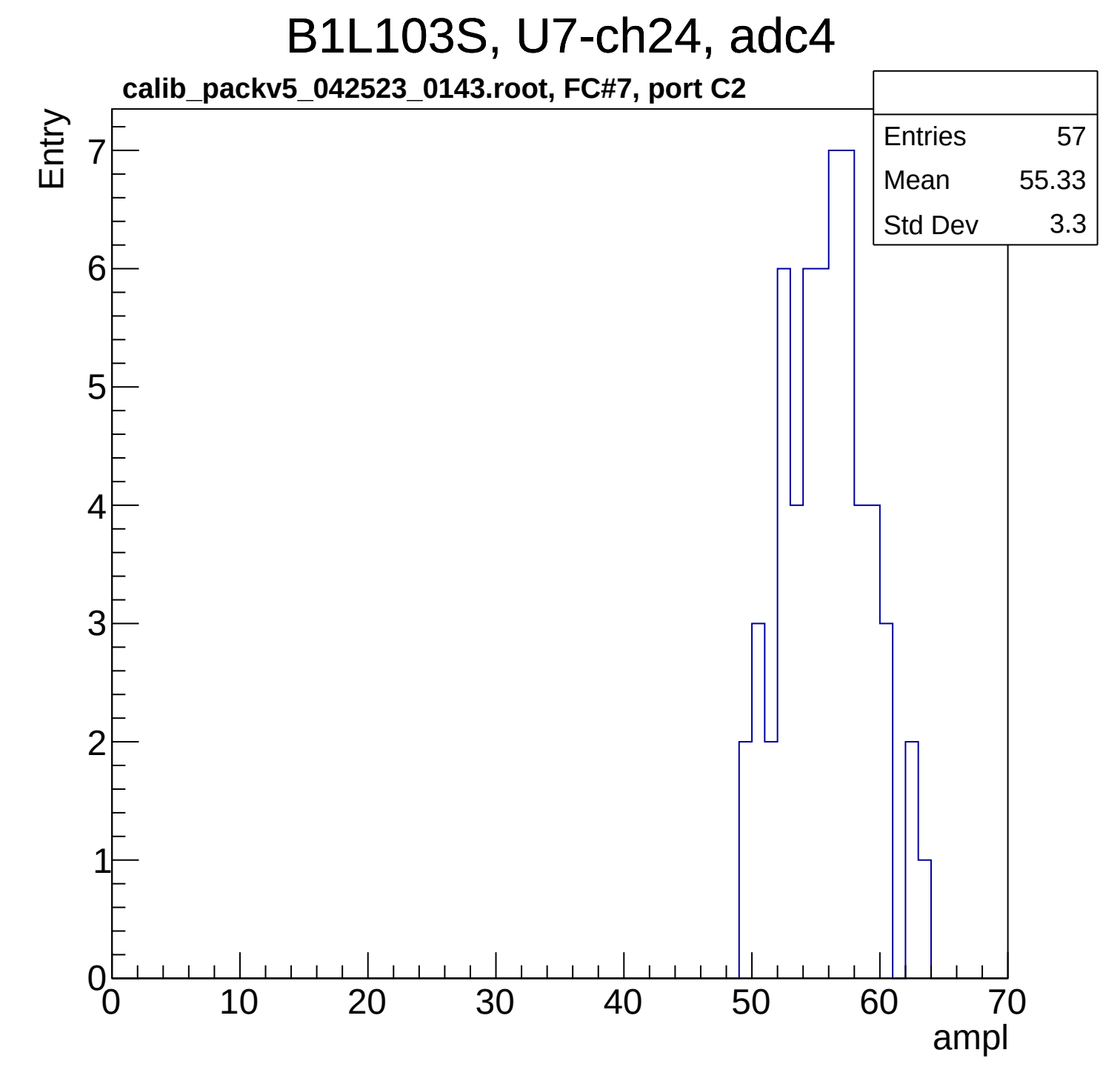
60
70


B1L103S, U7-ch24, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 55.33
Std Dev 3.3
Entry
ampl
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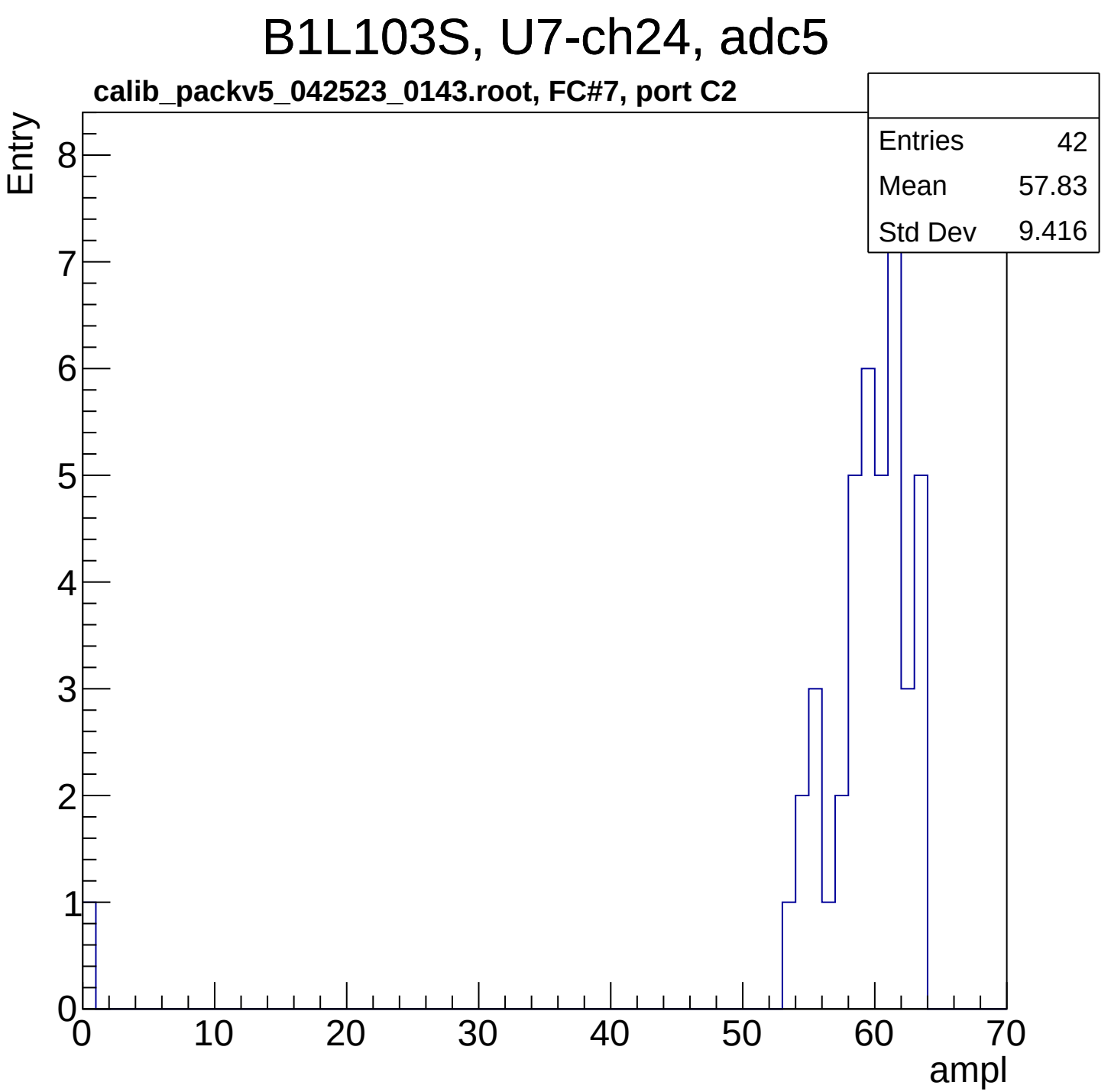
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch24, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 42
Mean 57.83
Std Dev 9.416
Entry
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2
3
4
5
6
7
8
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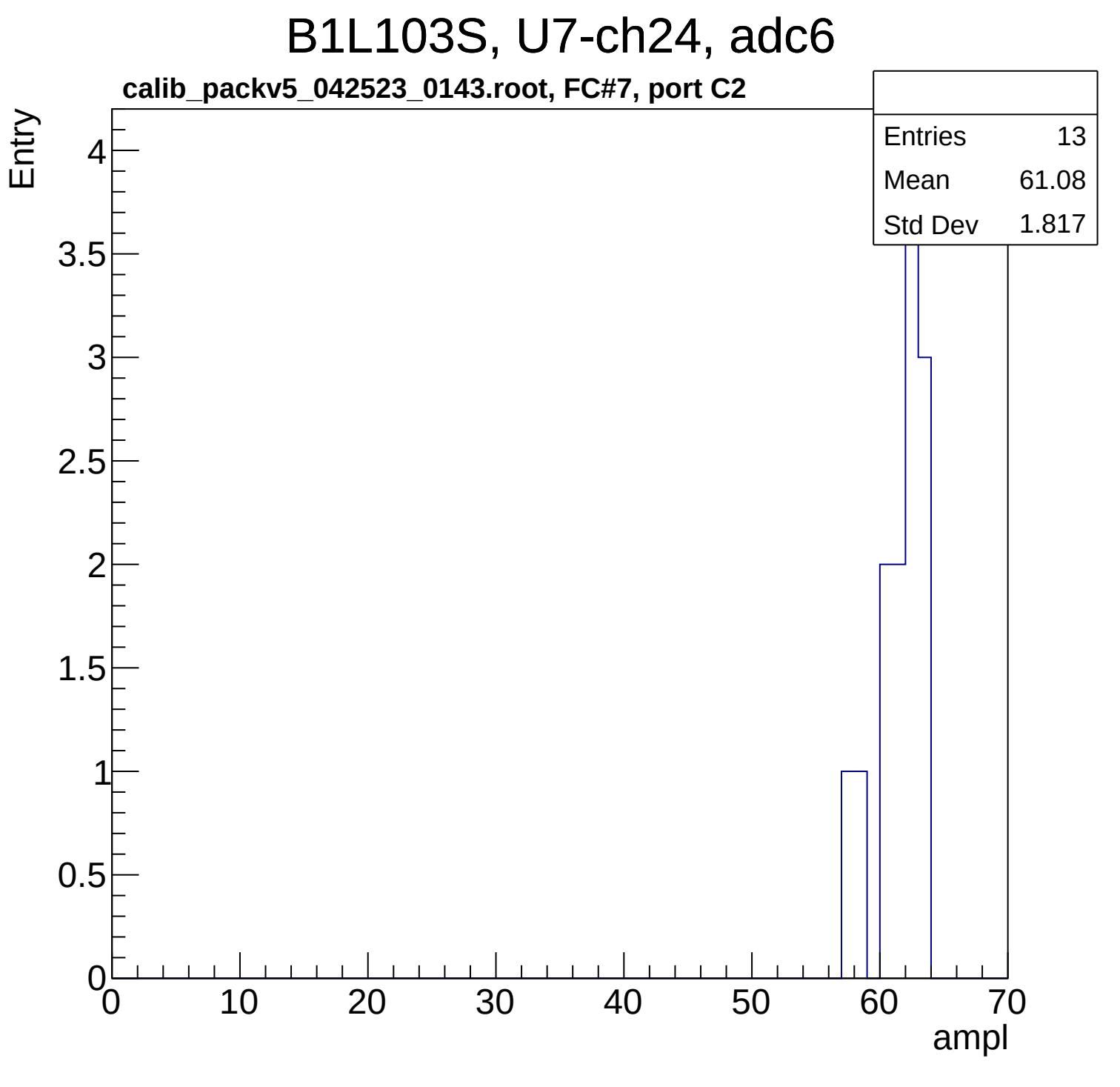
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch24, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 13
Mean 61.08
Std Dev 1.817
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
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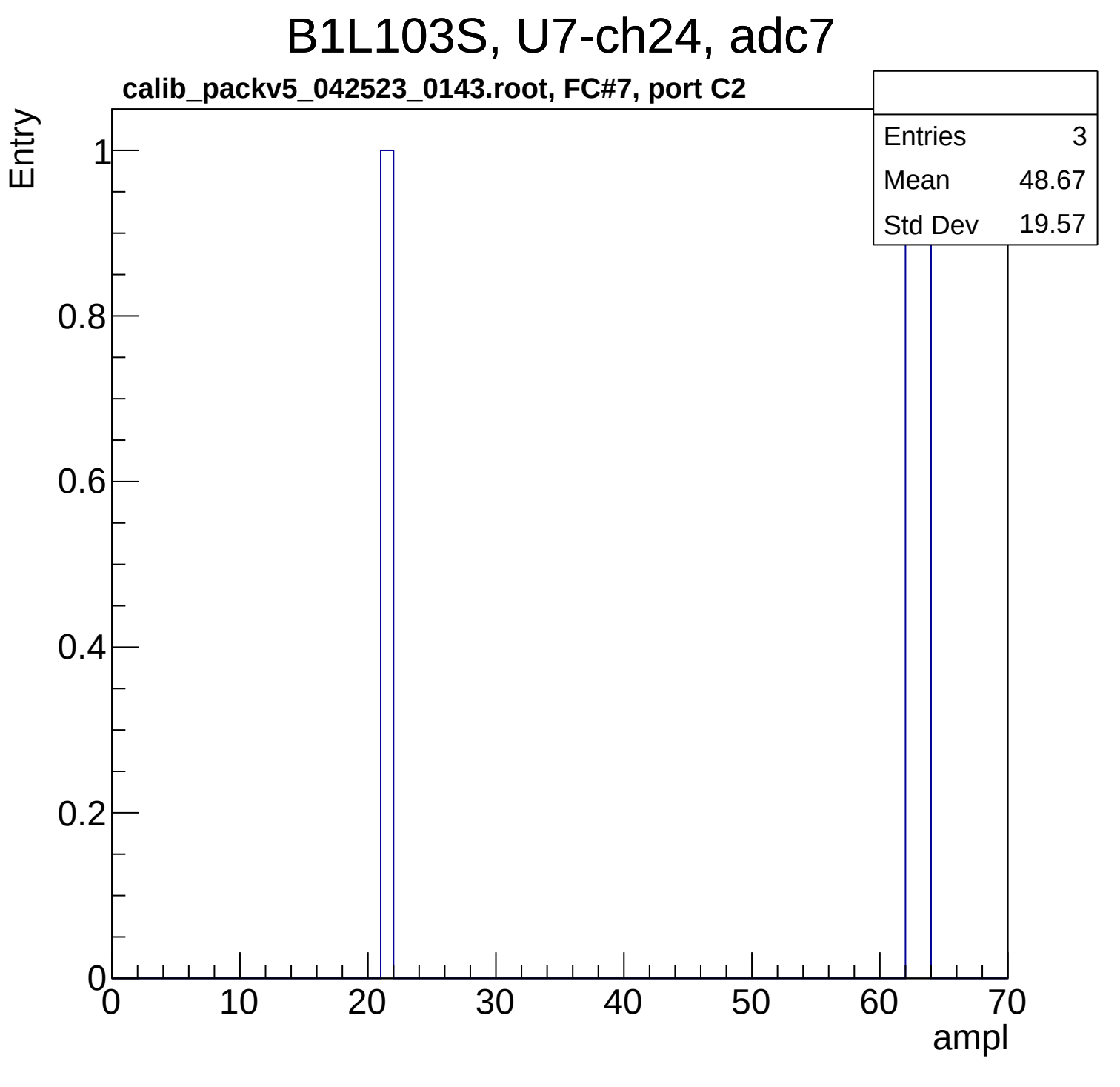
60
70


B1L103S, U7-ch24, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 48.67
Std Dev 19.57
Entry
ampl
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0.2
0.4
0.6
0.8
1
0
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40
50
60
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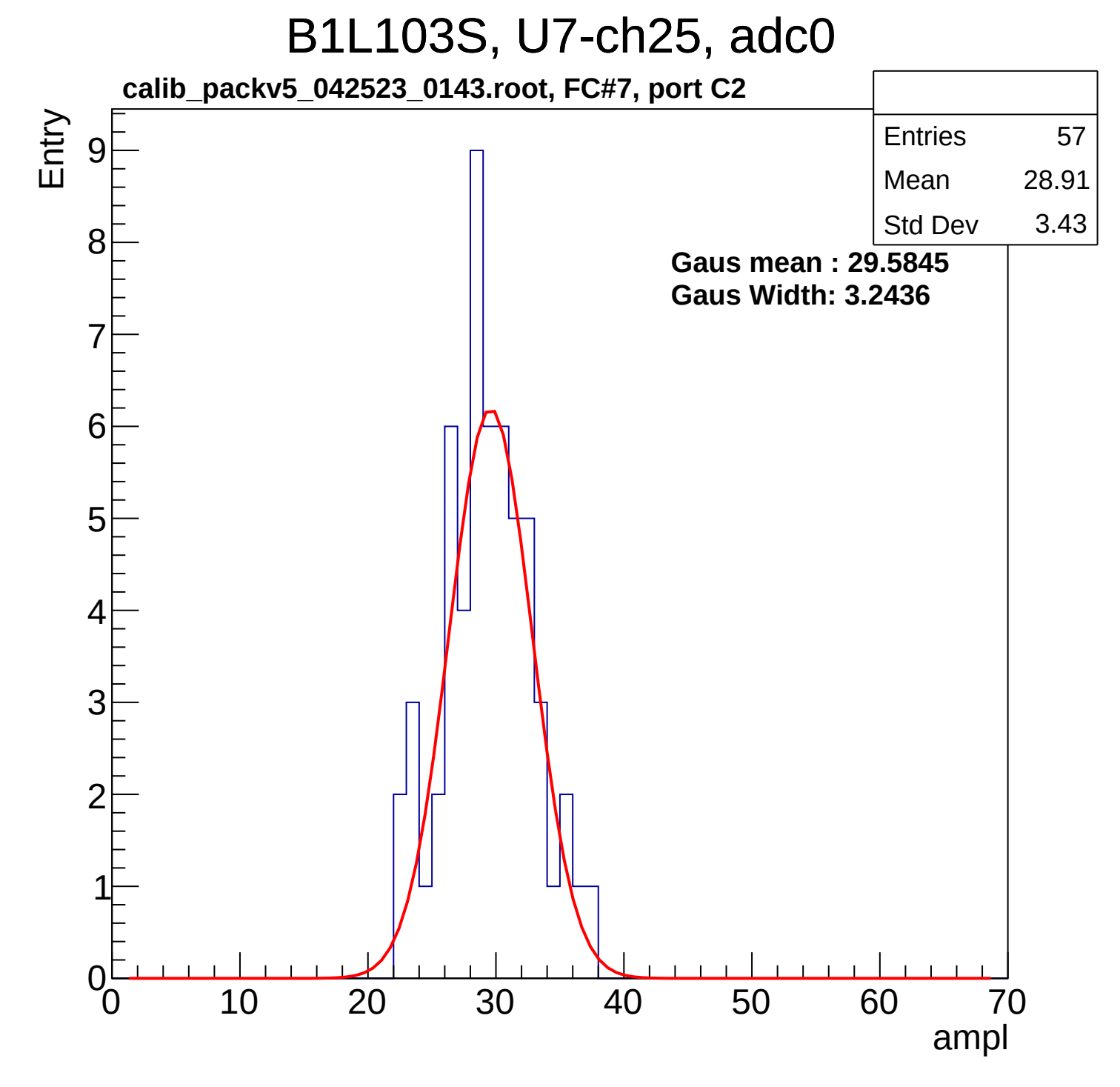
B1L103S, U7-ch25, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 28.91
Std Dev 3.43
Gaus mean : 29.5845
Gaus Width: 3.2436
Entry
ampl
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3
4
5
6
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0
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60
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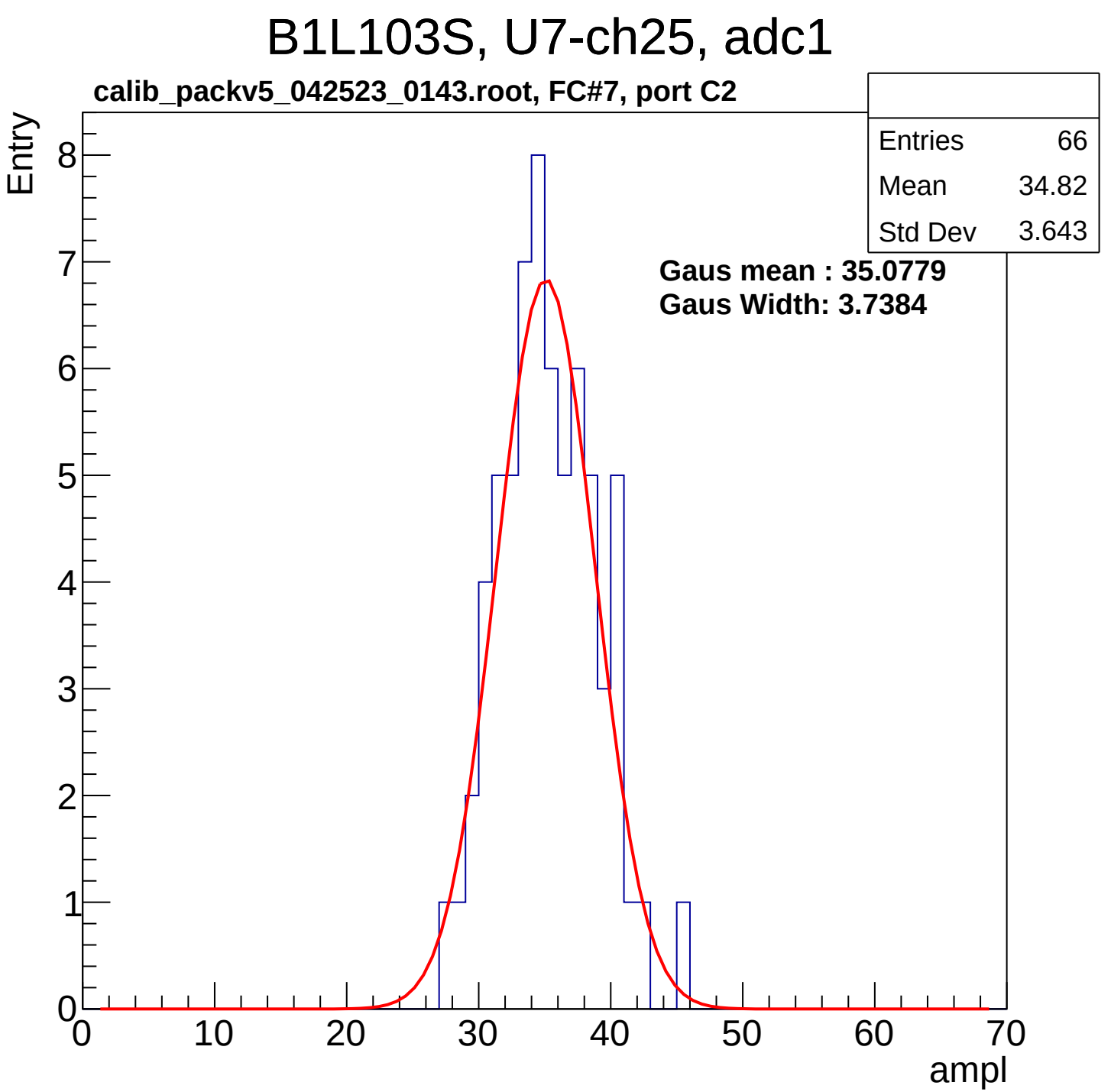
B1L103S, U7-ch25, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 34.82
Std Dev 3.643
Gaus mean : 35.0779
Gaus Width: 3.7384
Entry
ampl
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1
2
3
4
5
6
7
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0
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40
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60
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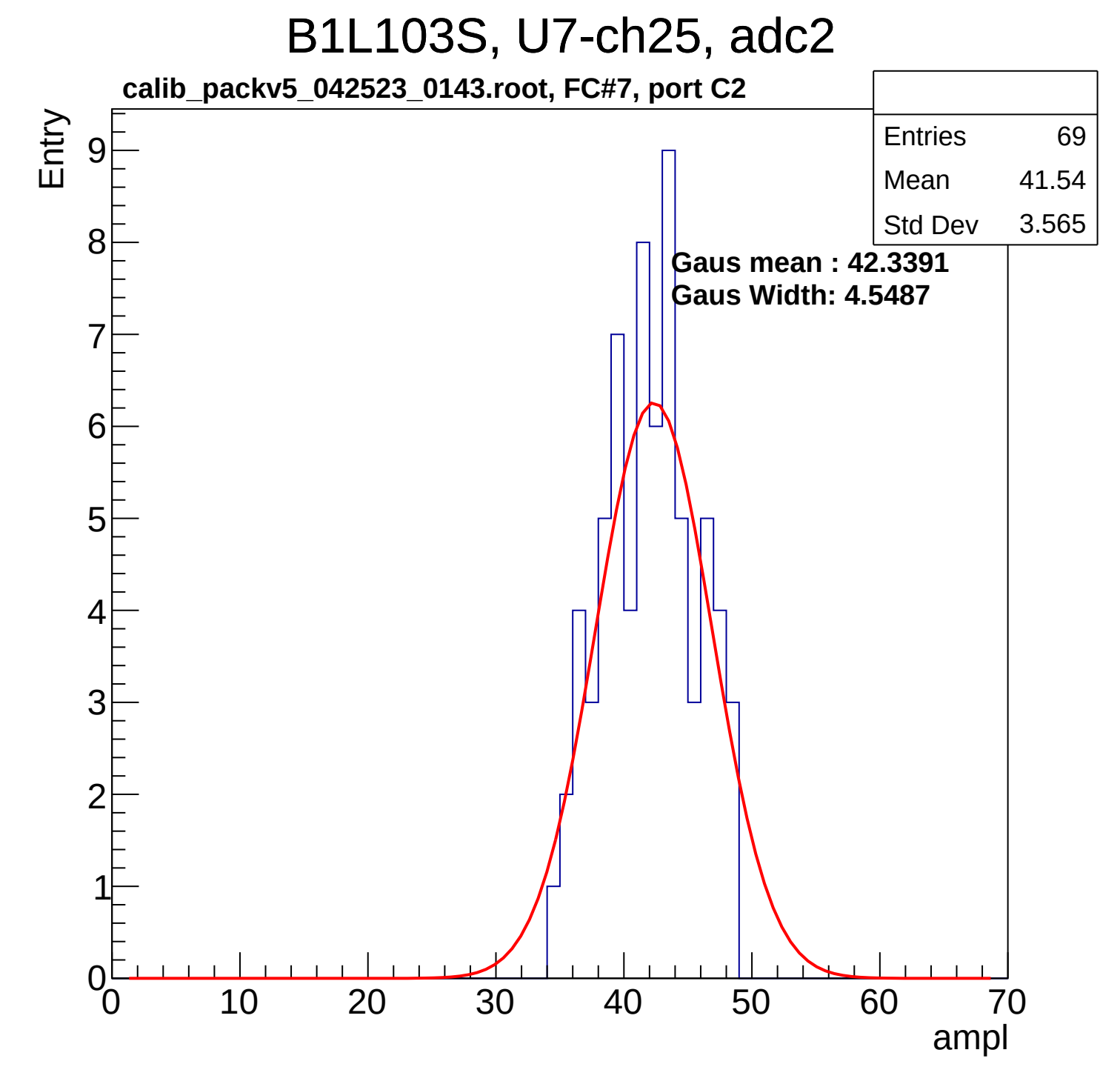
B1L103S, U7-ch25, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 41.54
Std Dev 3.565
Gaus mean : 42.3391
Gaus Width: 4.5487
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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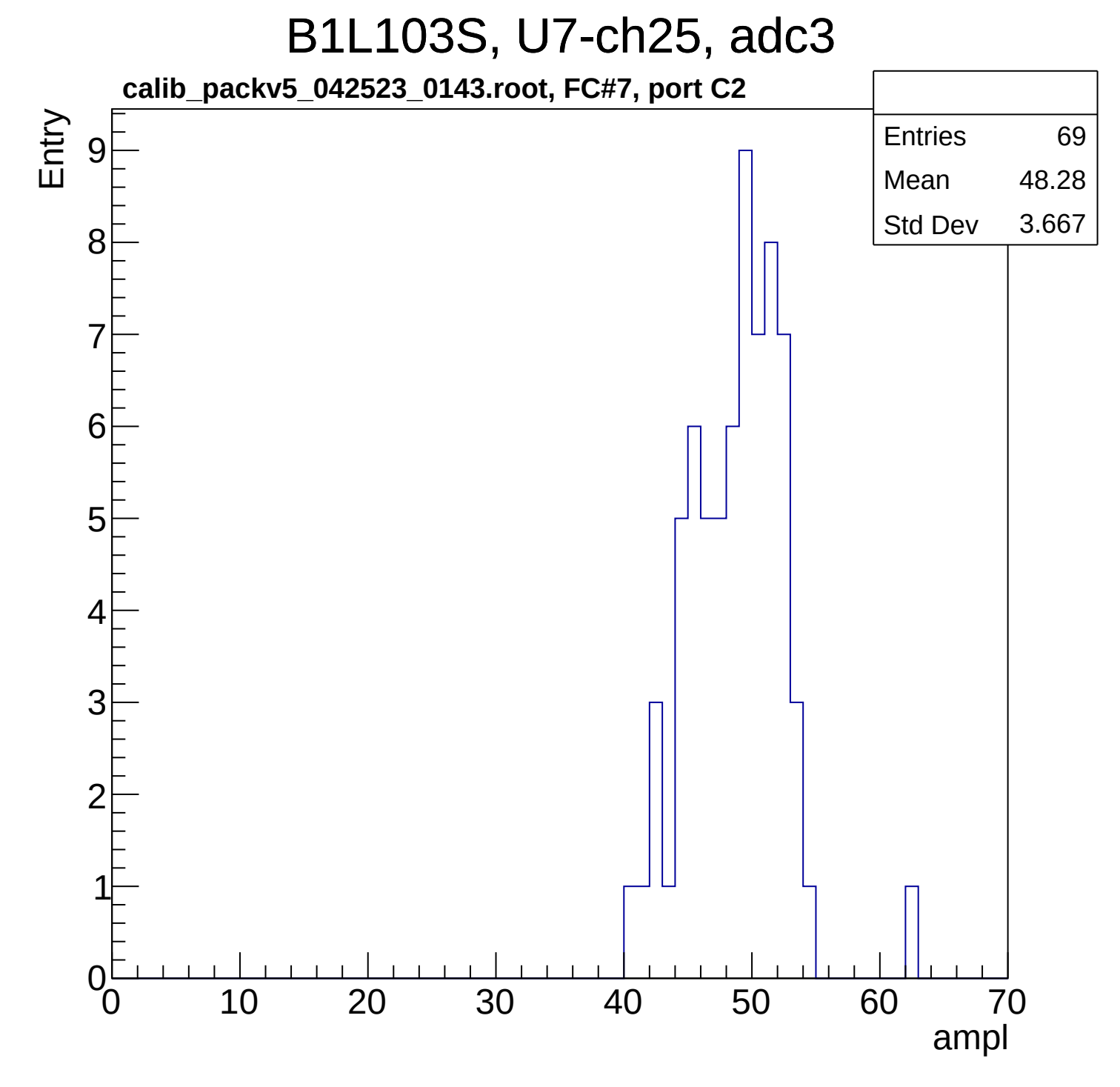
B1L103S, U7-ch25, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 48.28
Std Dev 3.667
Entry
ampl
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2
3
4
5
6
7
8
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0
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60
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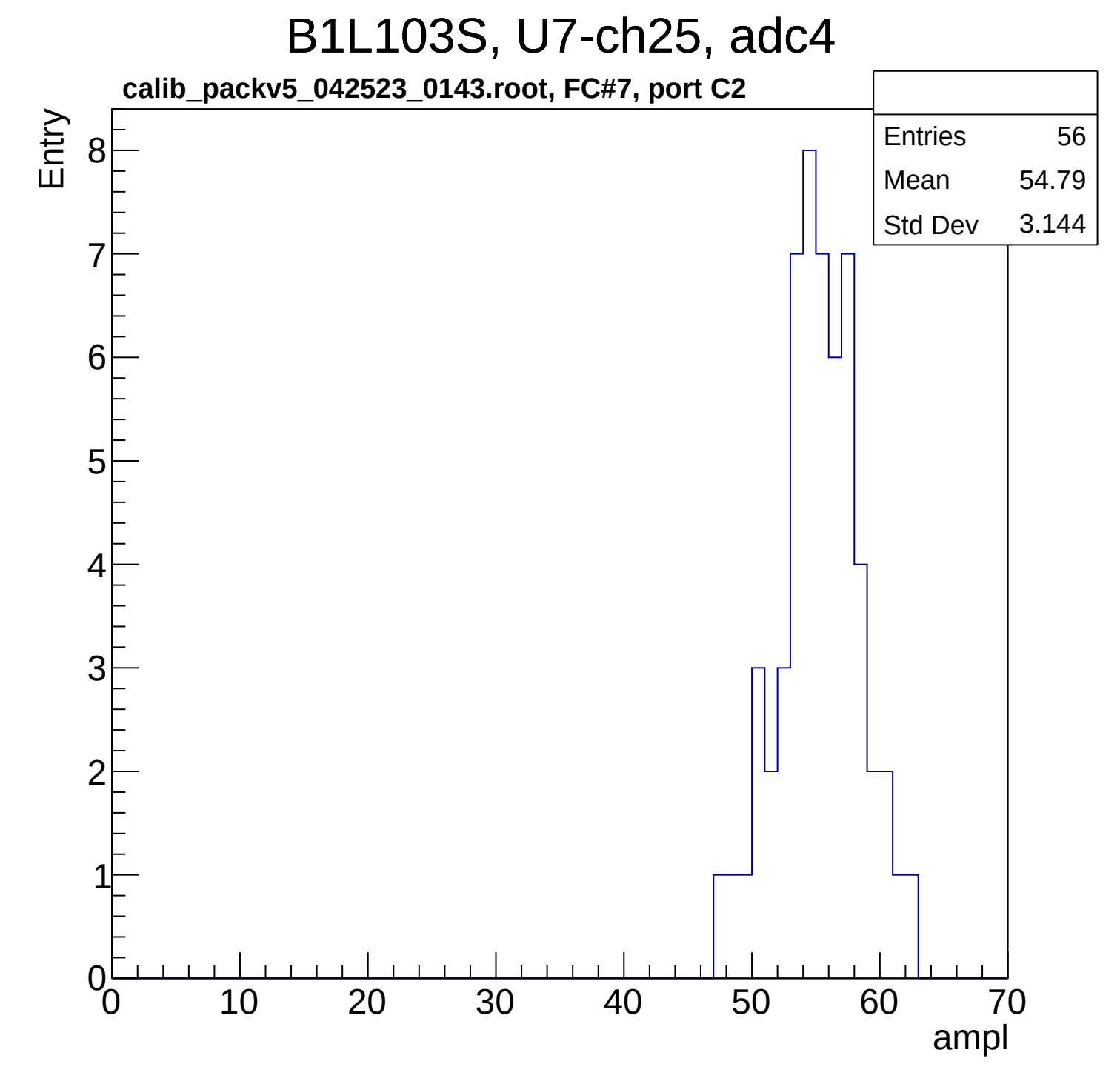
B1L103S, U7-ch25, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 54.79
Std Dev 3.144
Entry
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10
20
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50
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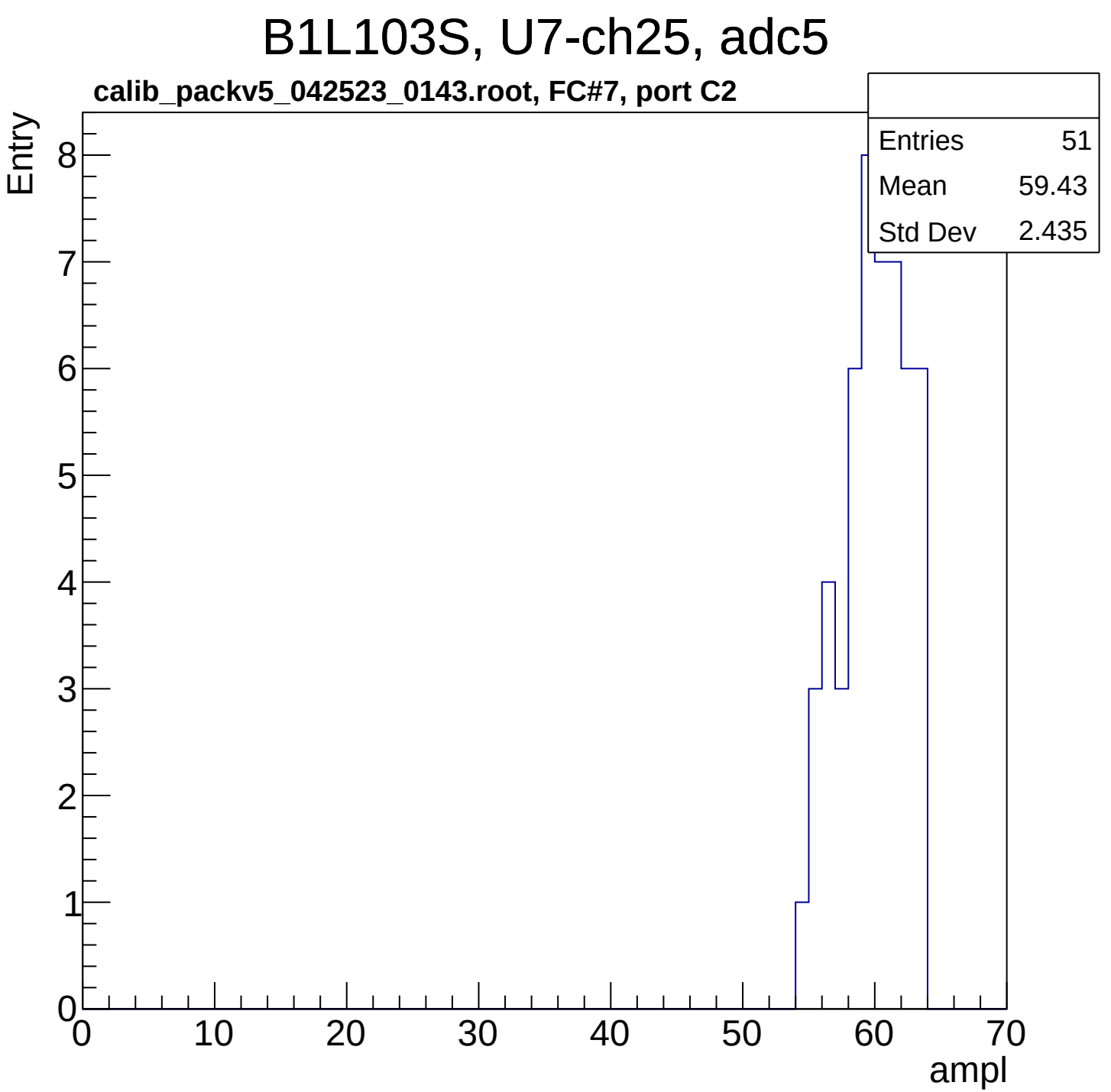
70
ampl


B1L103S, U7-ch25, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 51
Mean 59.43
Std Dev 2.435
Entry
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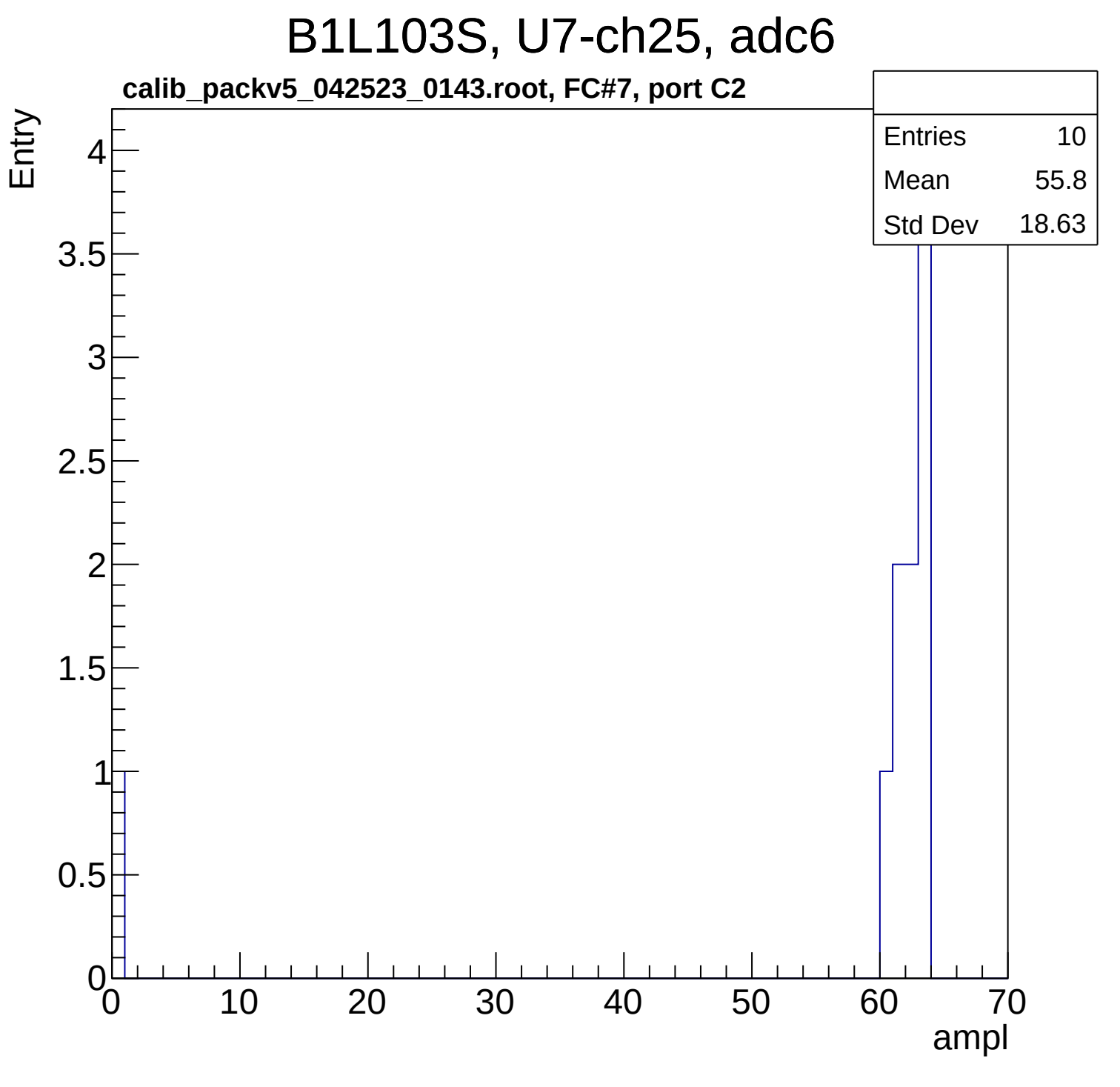
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch25, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 10
Mean 55.8
Std Dev 18.63
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
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30
40
50
60
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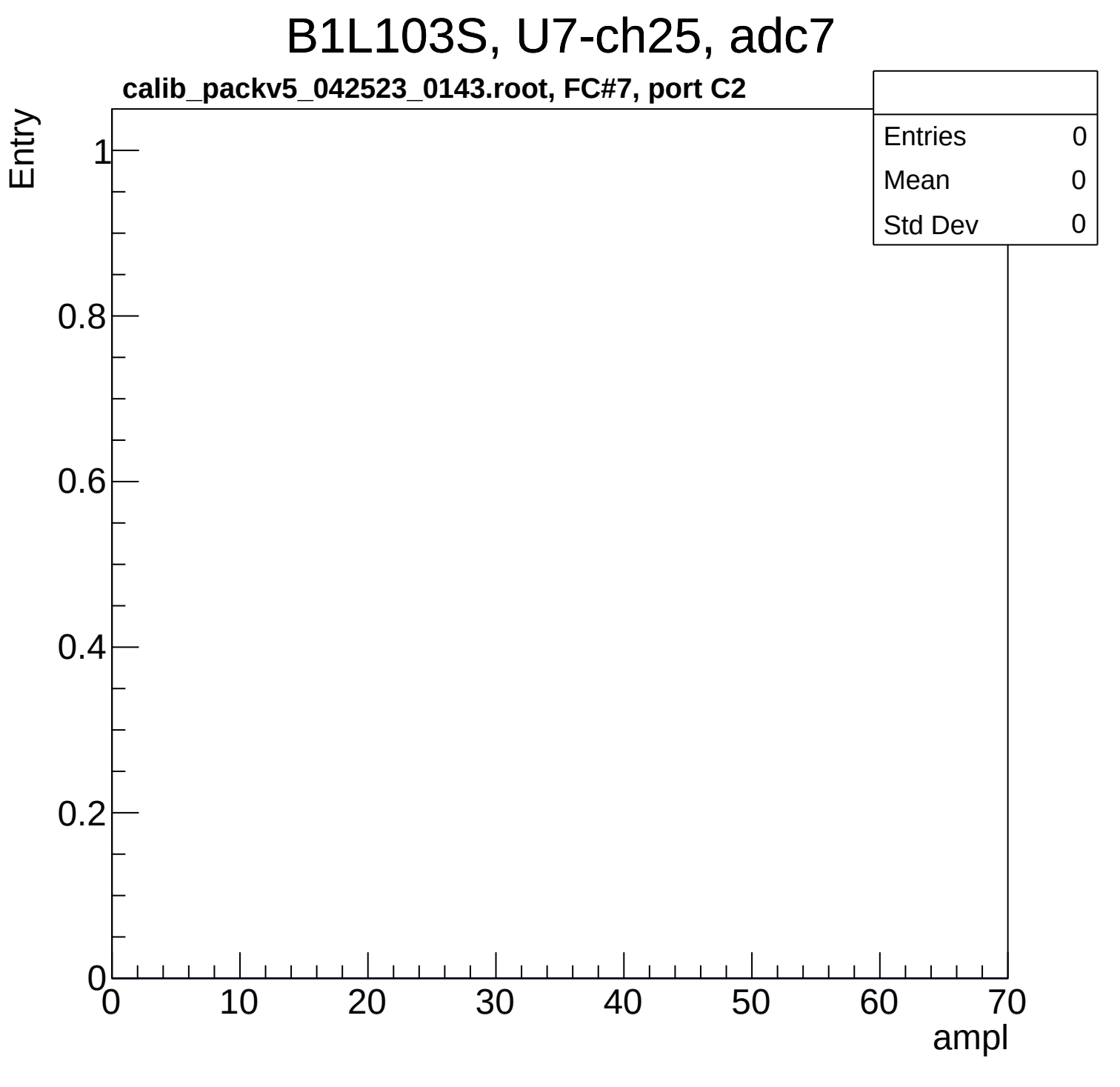
B1L103S, U7-ch25, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
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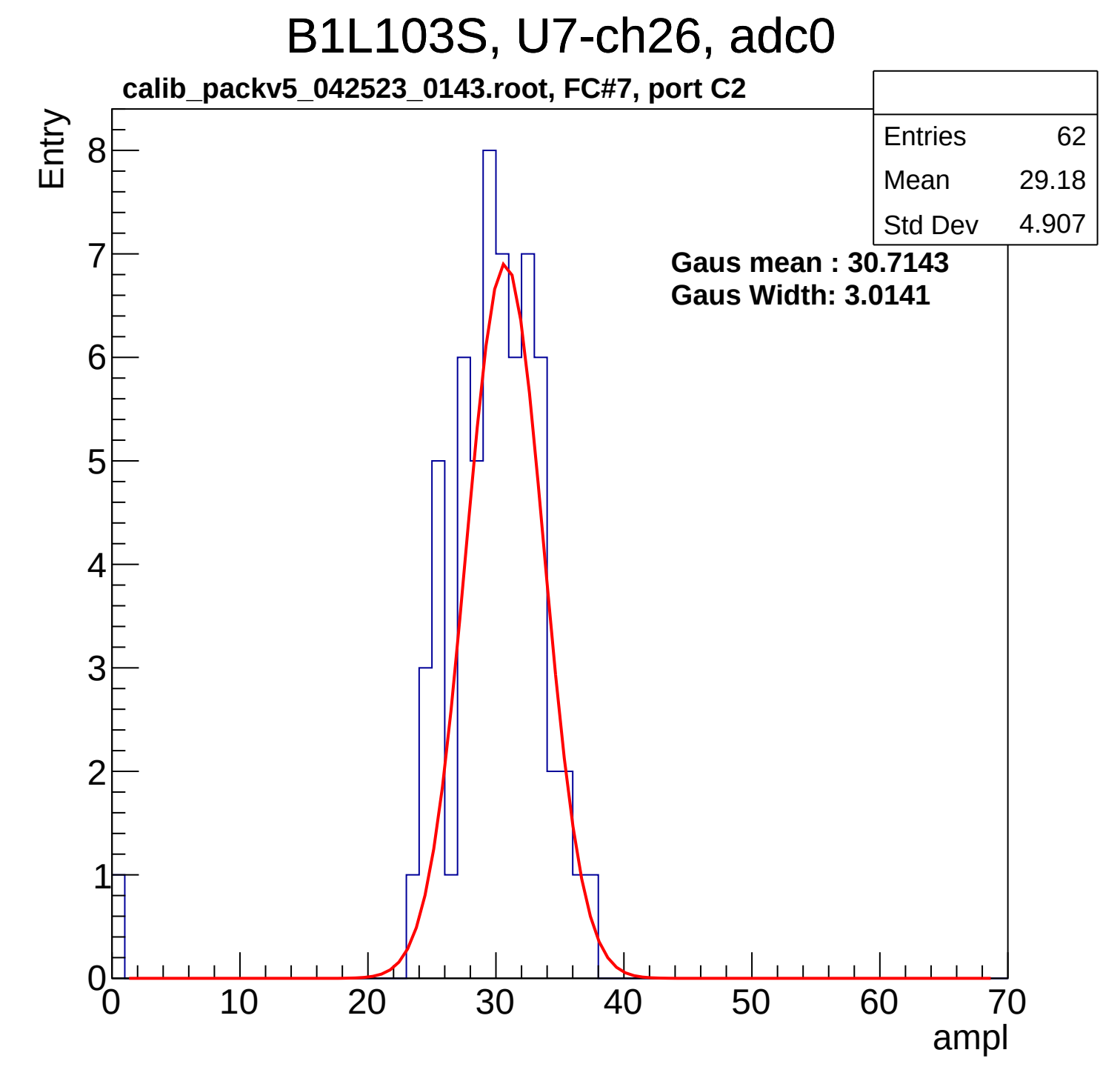
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch26, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 62
Mean 29.18
Std Dev 4.907
Gaus mean : 30.7143
Gaus Width: 3.0141
Entry
ampl
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1
2
3
4
5
6
7
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0
10
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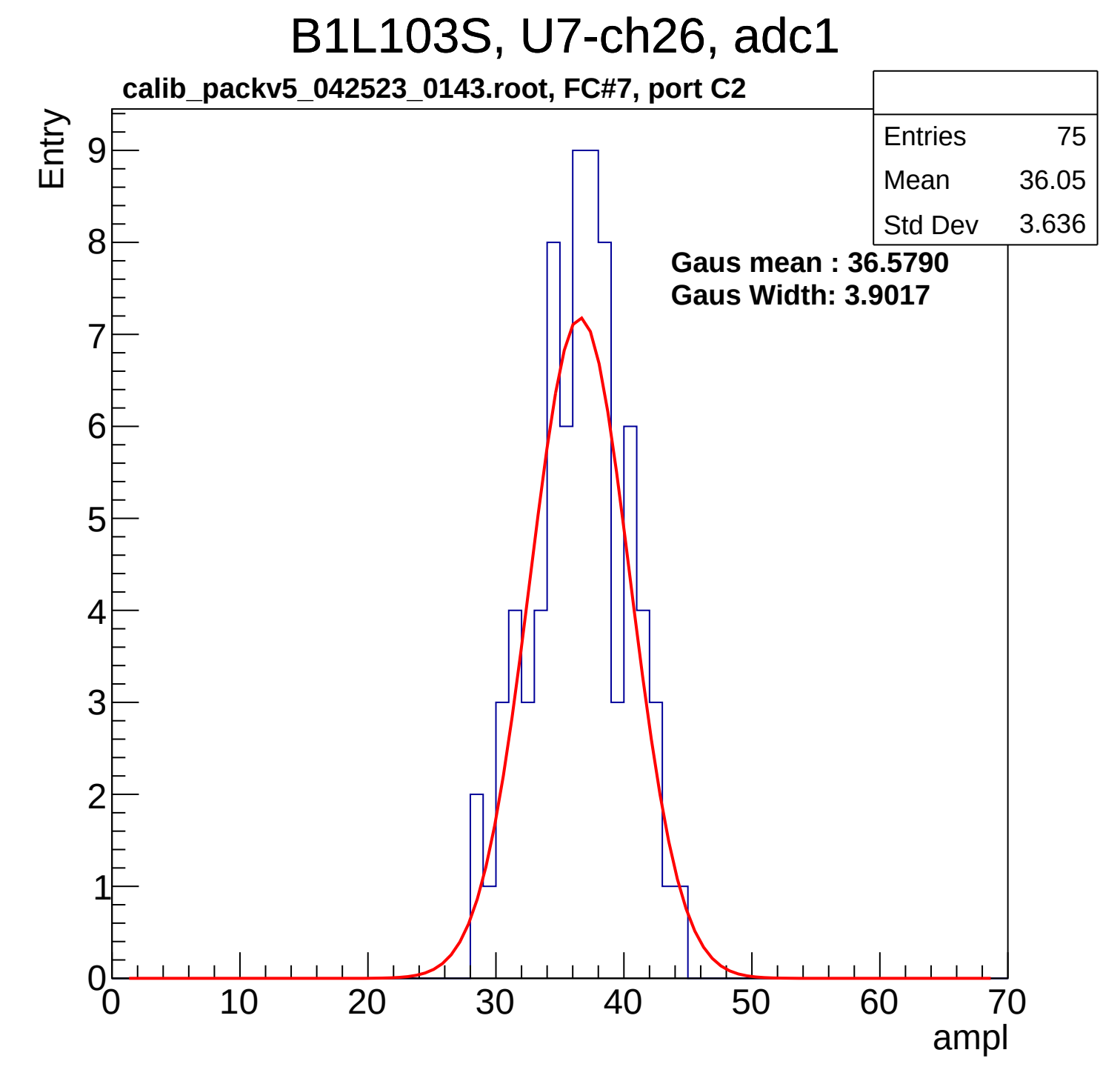
B1L103S, U7-ch26, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 75
Mean 36.05
Std Dev 3.636
Gaus mean : 36.5790
Gaus Width: 3.9017
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
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60
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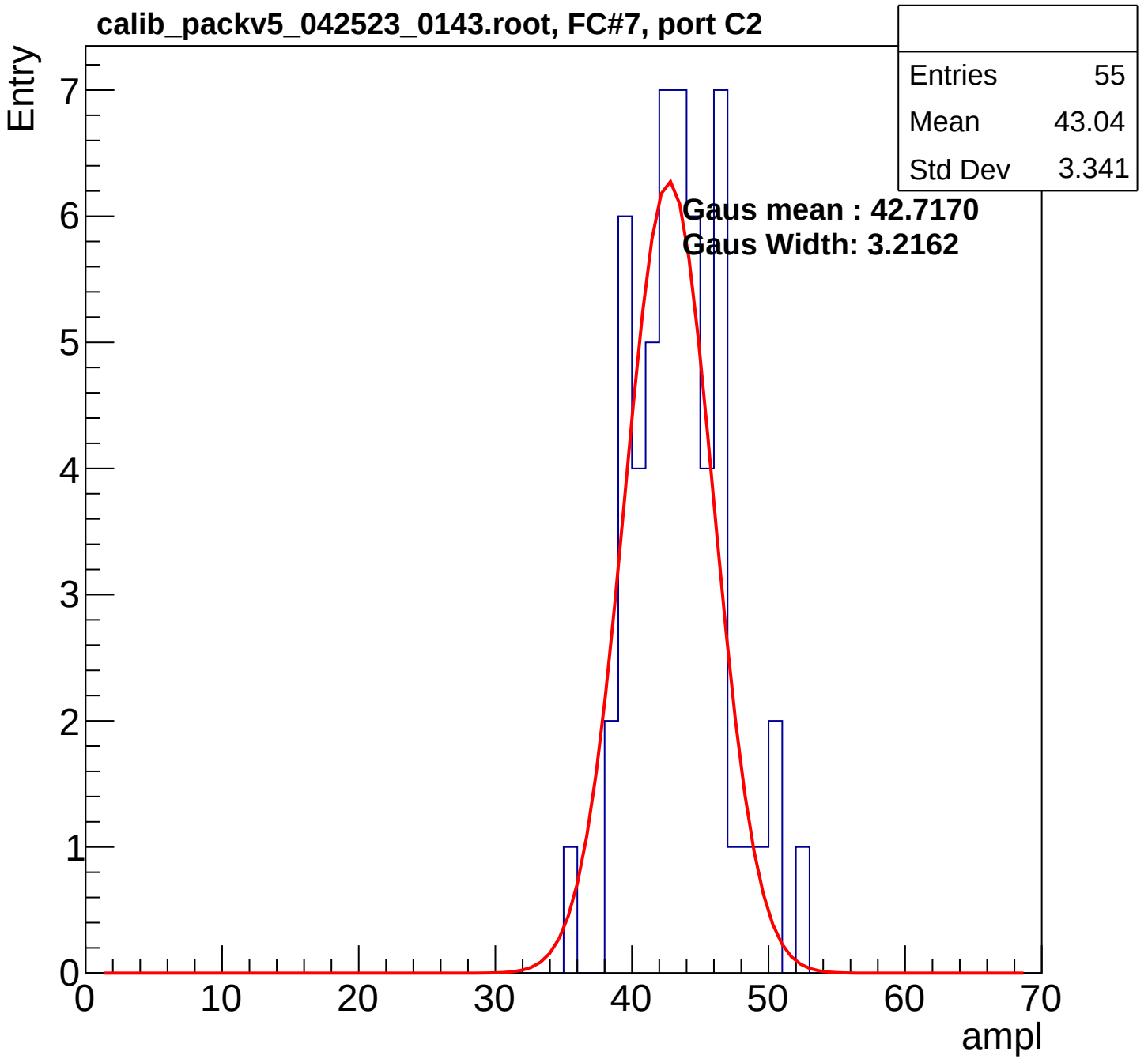
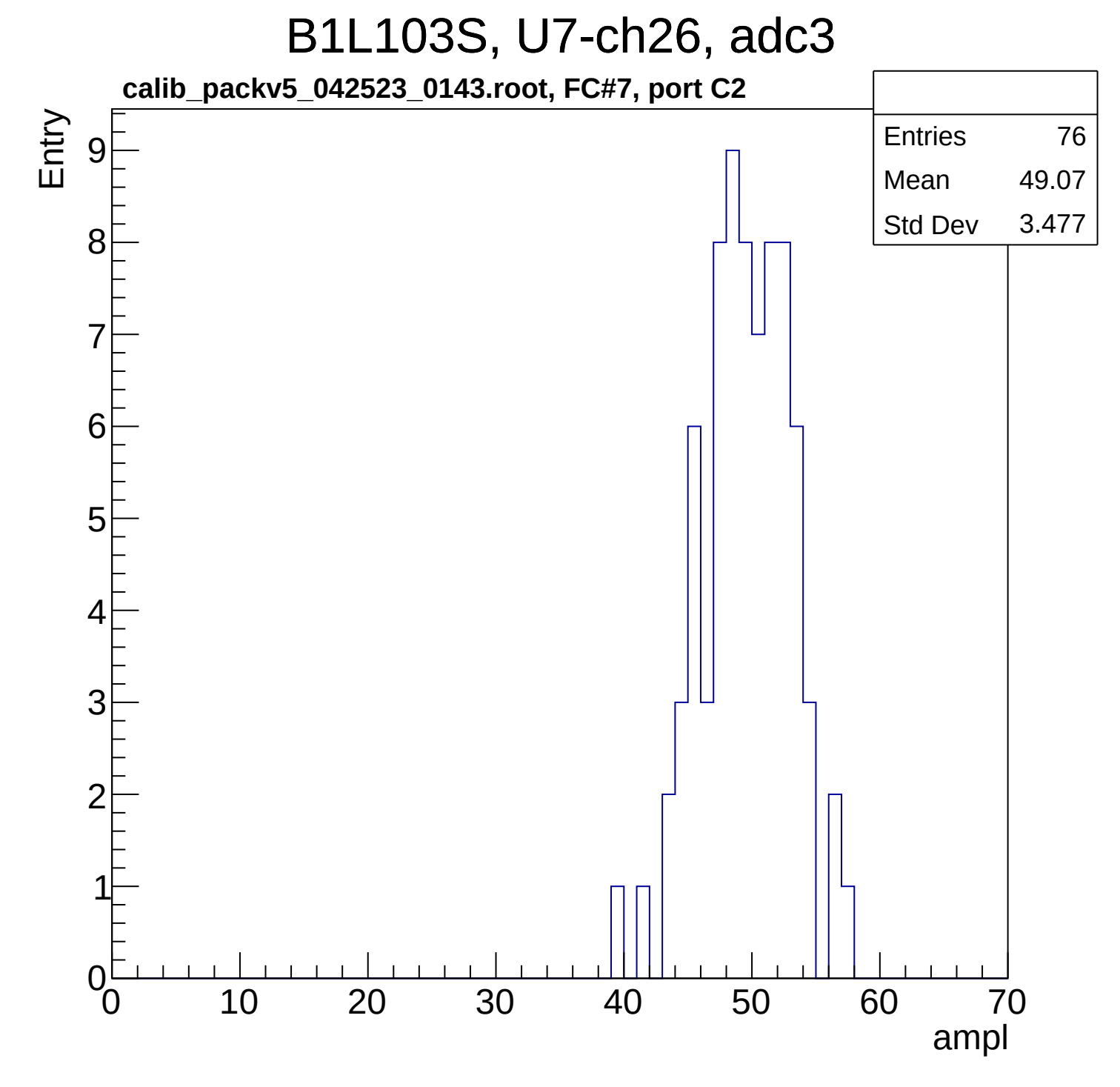

B1L103S, U7-ch26, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 43.04
Std Dev 3.341
Gaus mean : 42.7170
Gaus Width: 3.2162
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch26, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 76
Mean 49.07
Std Dev 3.477
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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40
50
60
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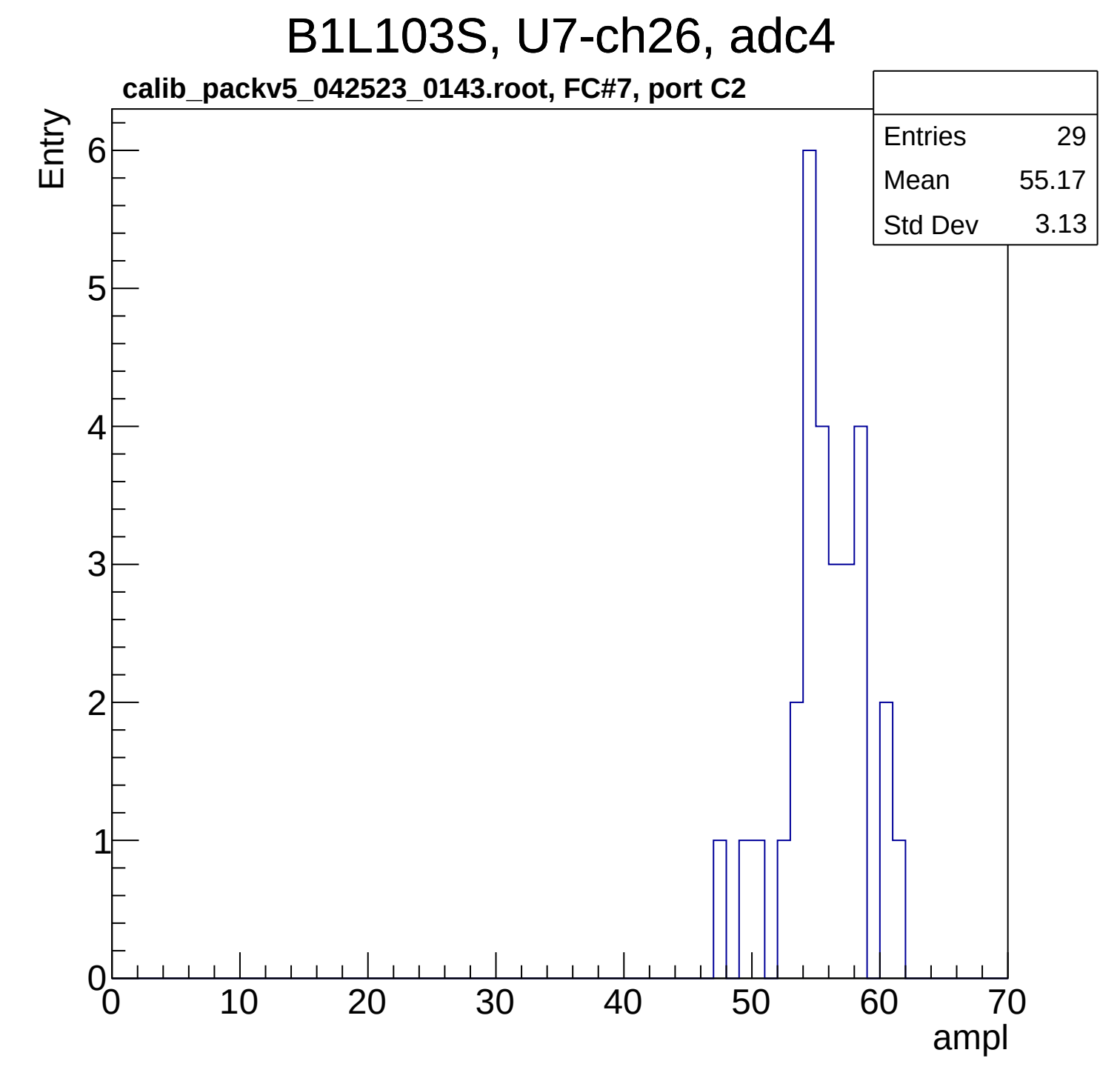
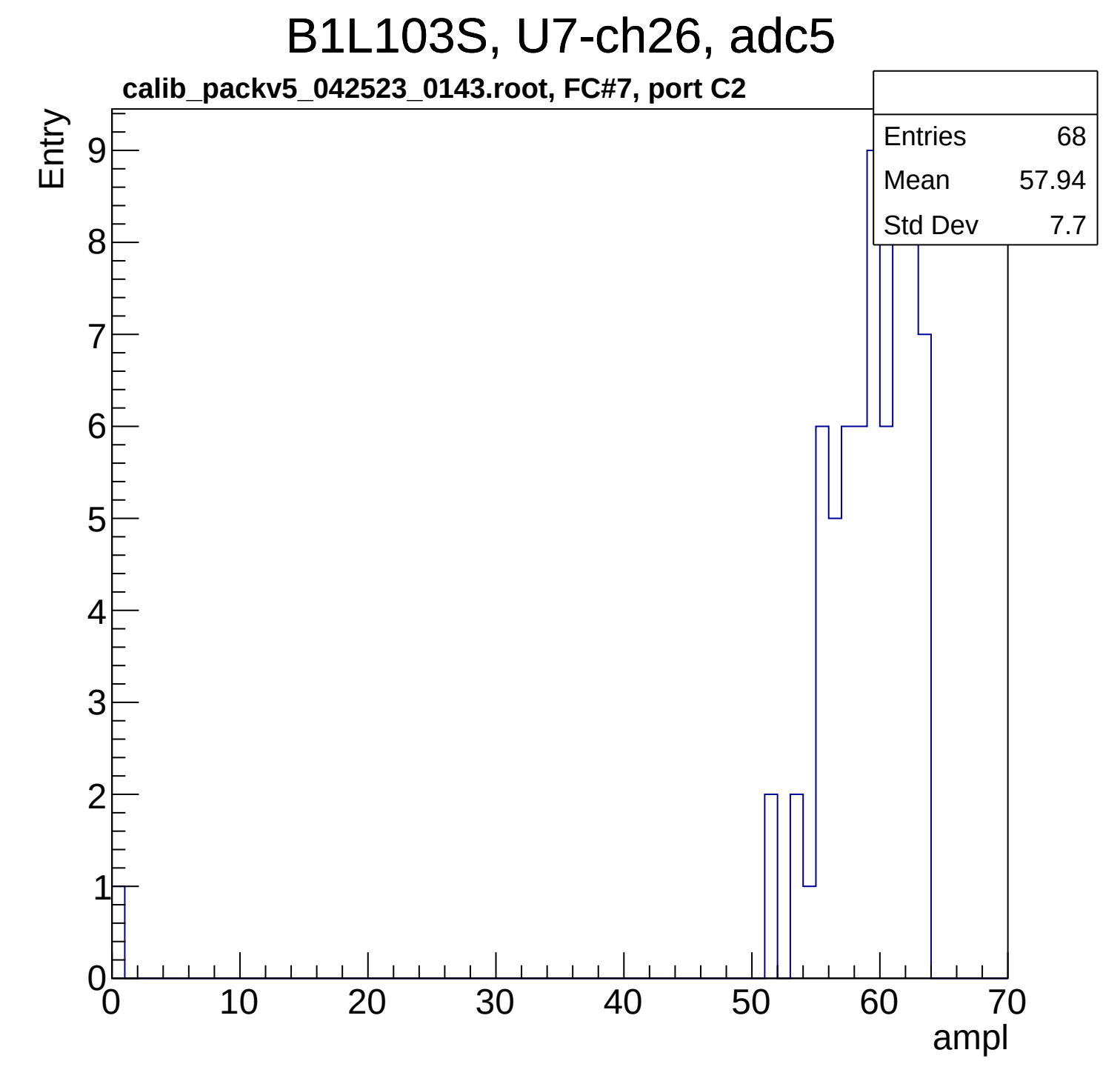

B1L103S, U7-ch26, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 29
Mean 55.17
Std Dev 3.13
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch26, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 57.94
Std Dev 7.7
Entry
ampl
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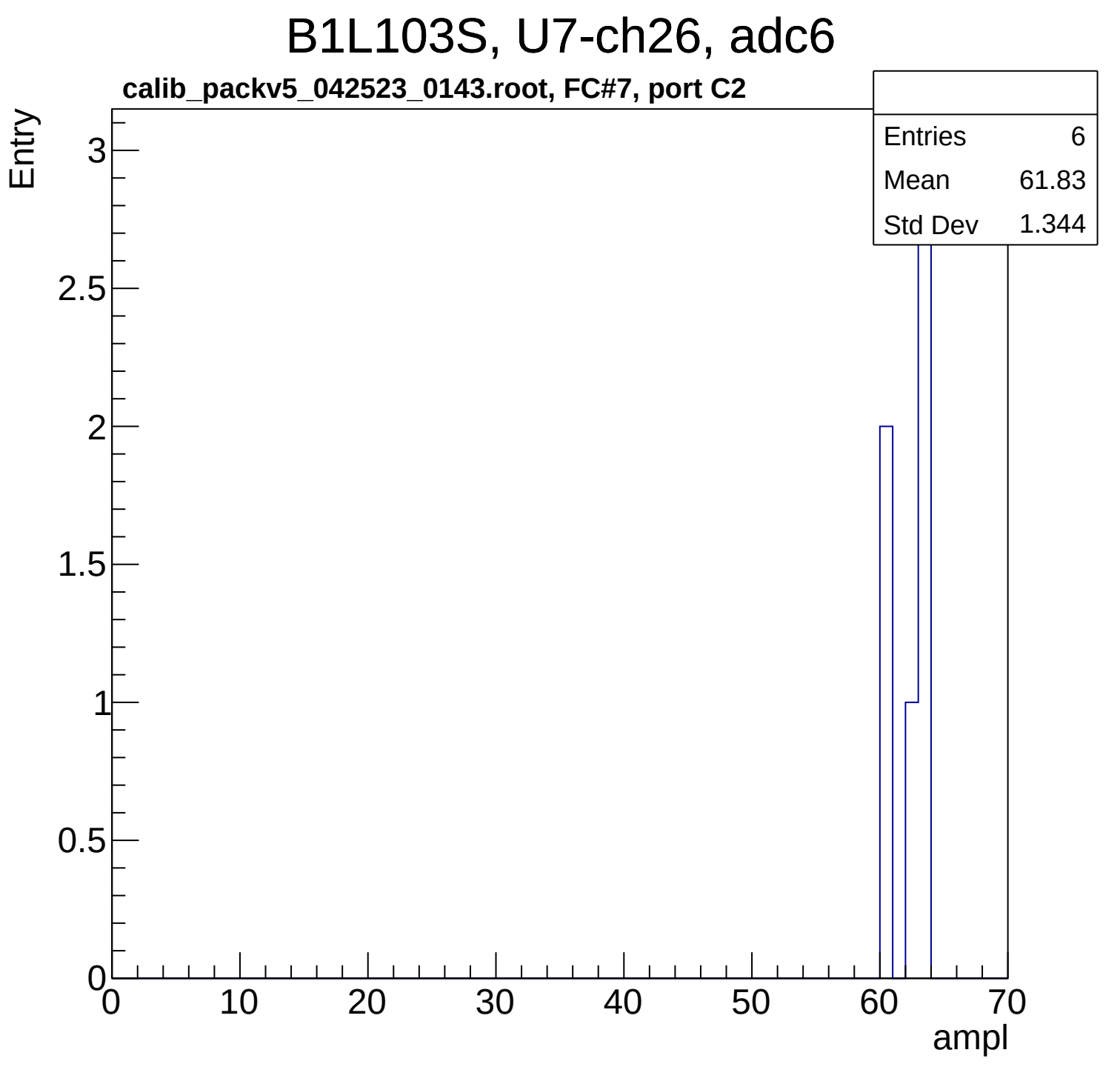
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch26, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 6
Mean 61.83
Std Dev 1.344
Entry
ampl
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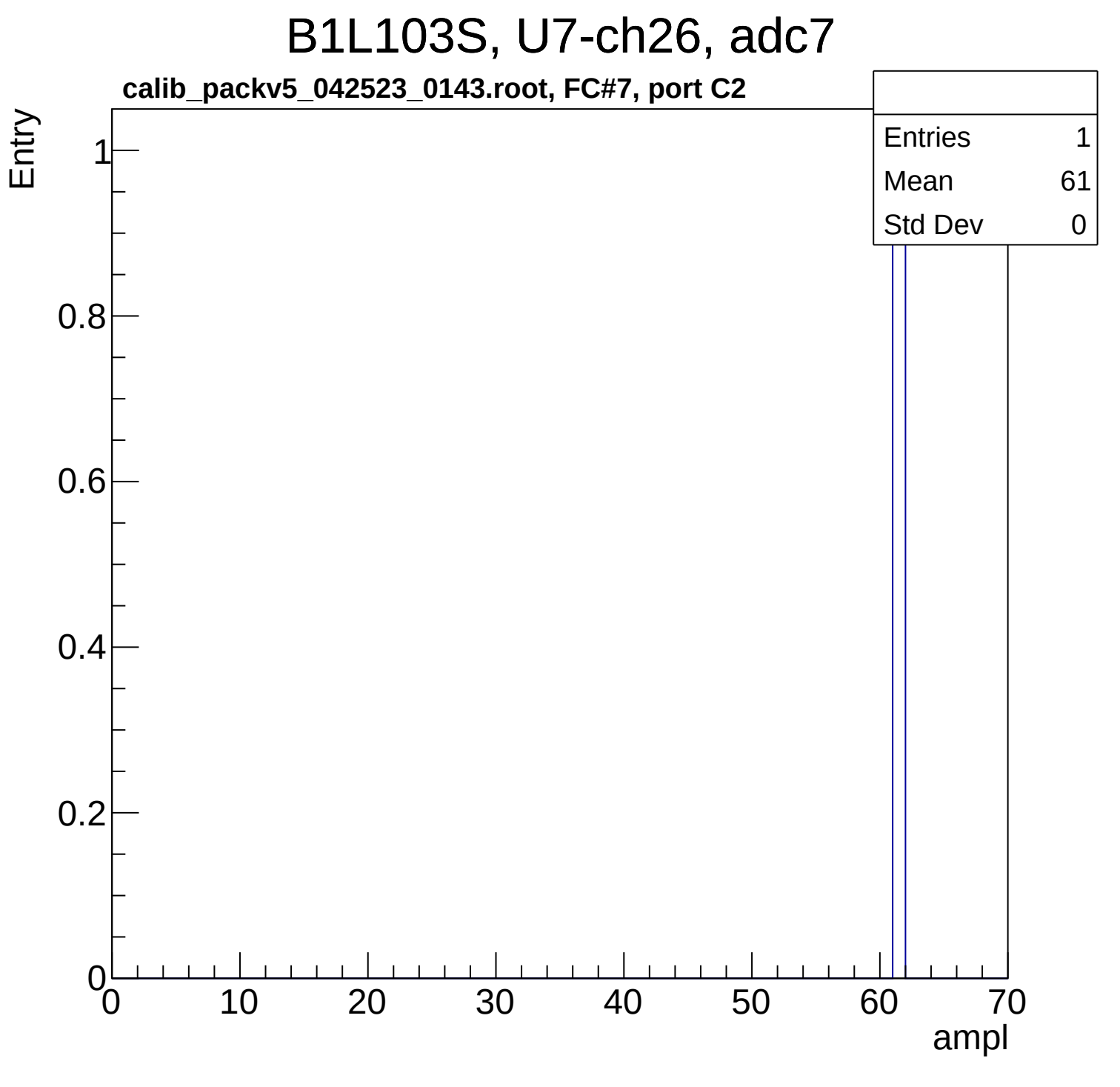
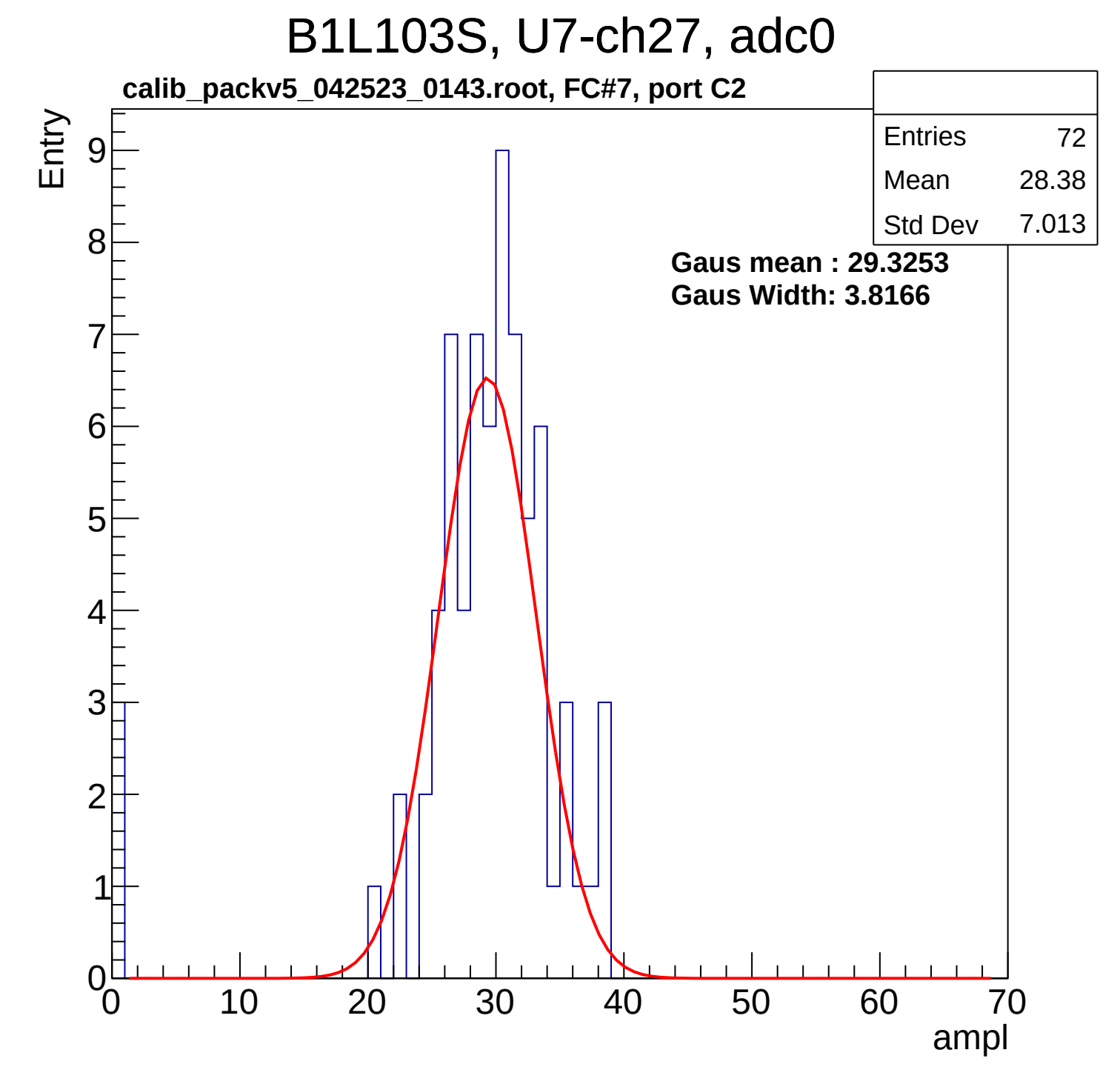
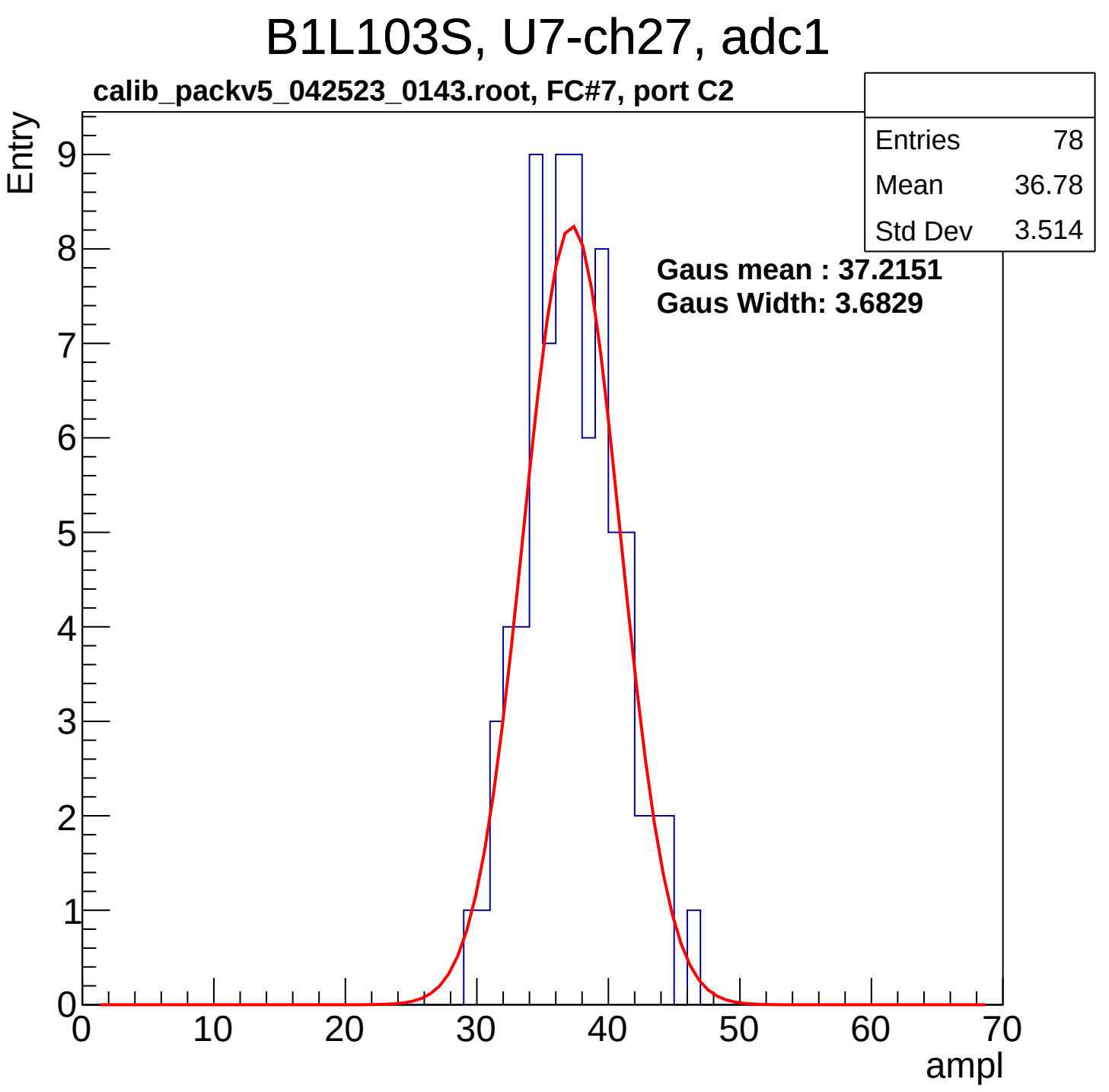
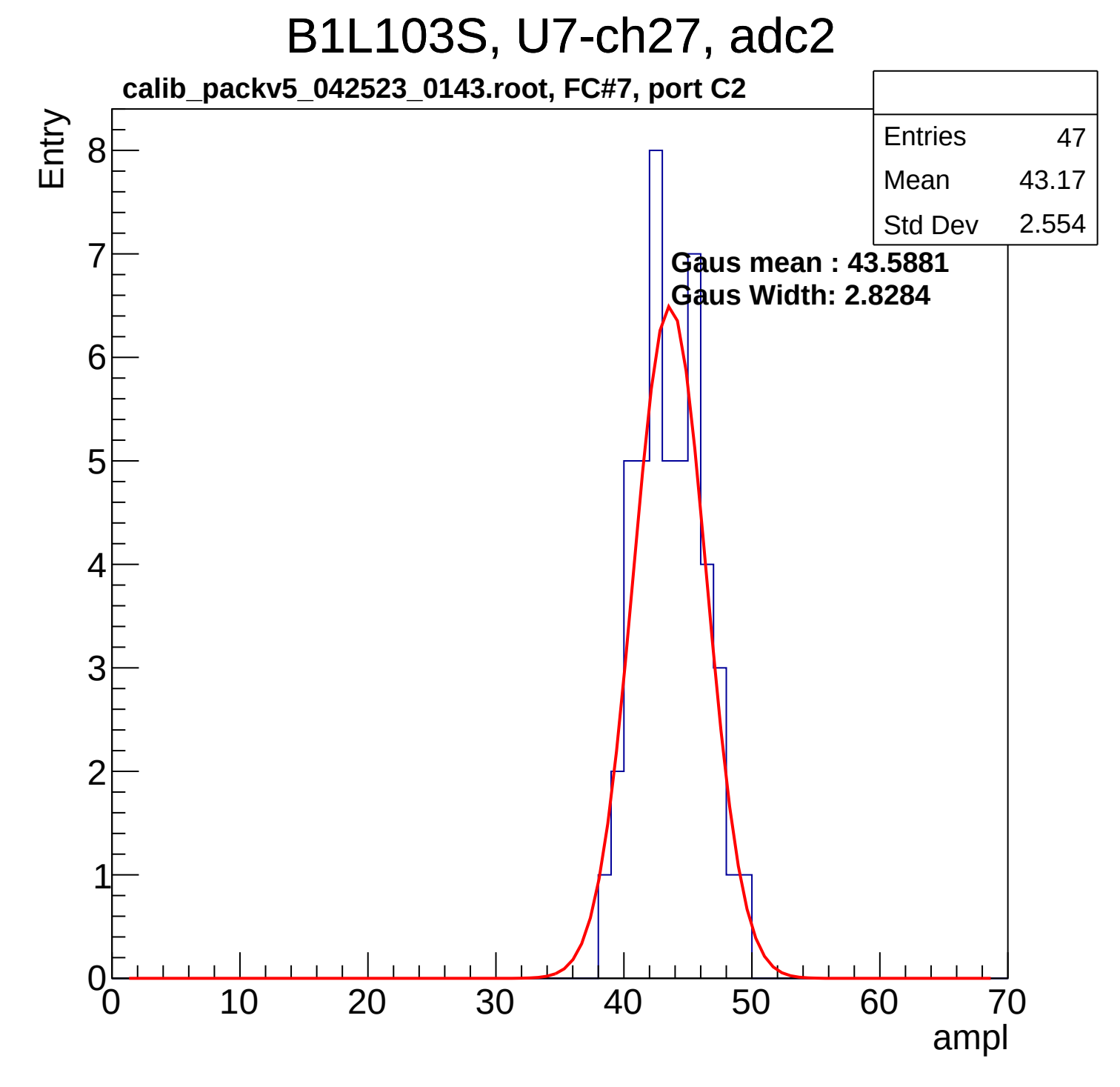
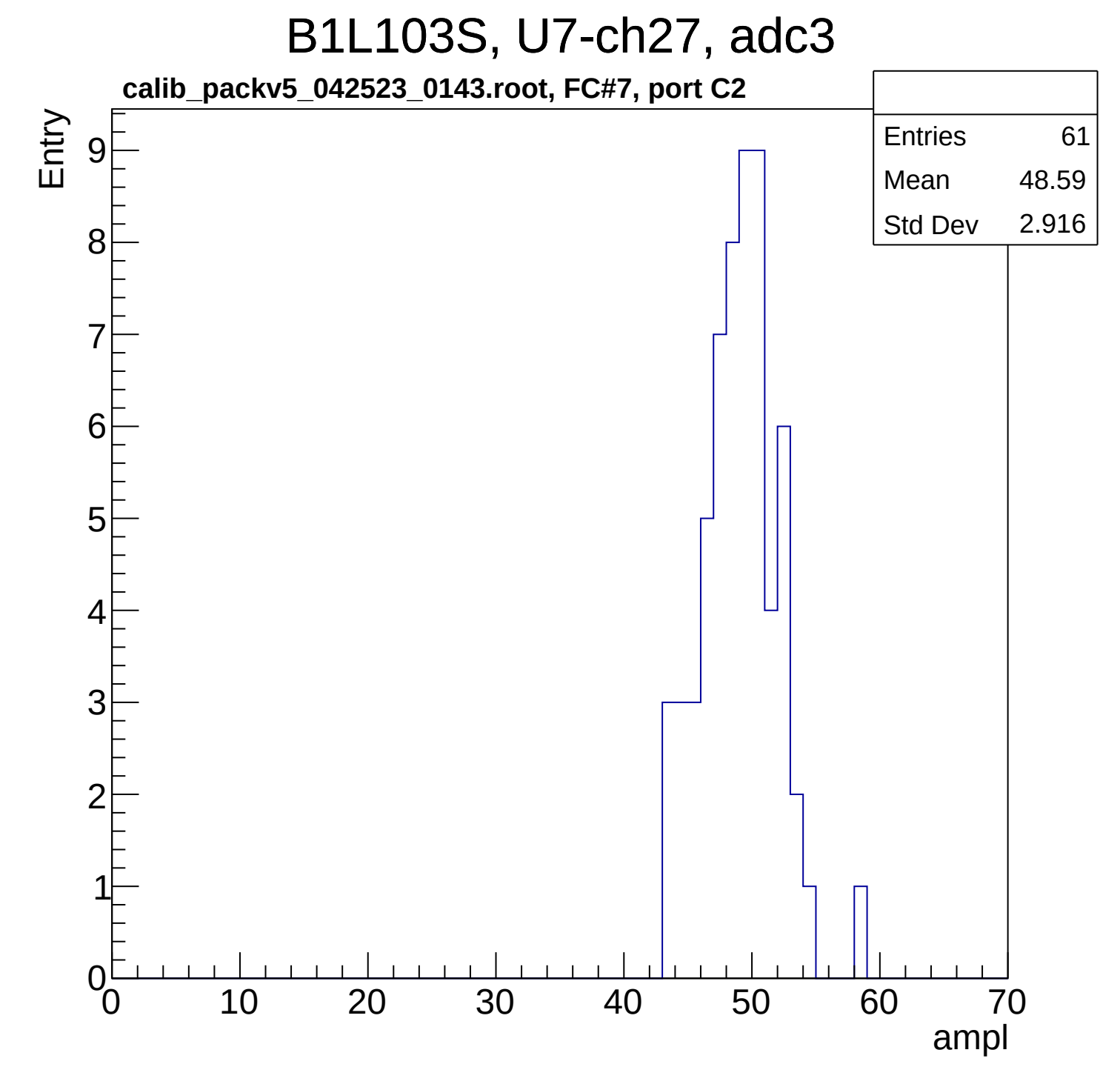
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

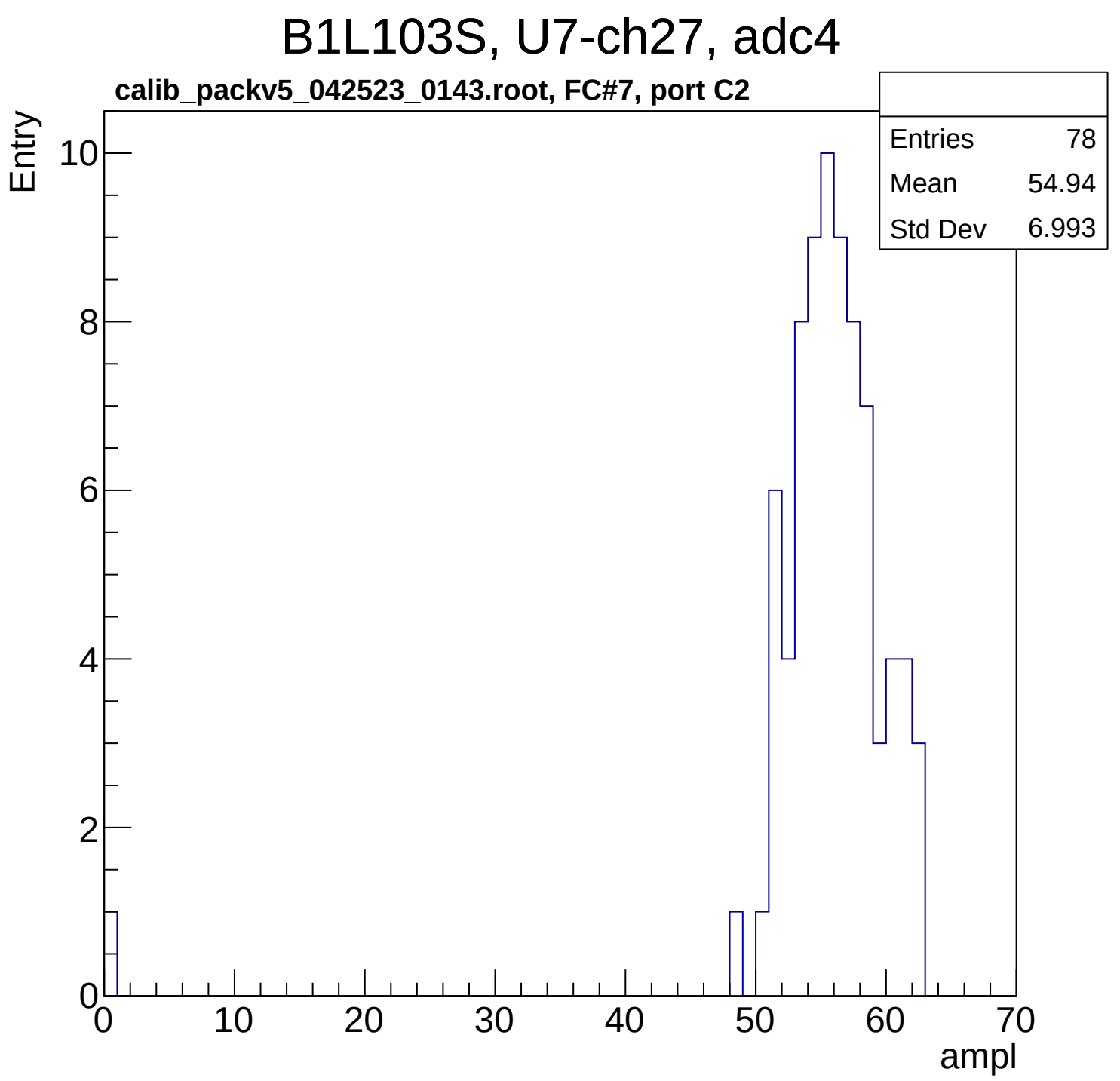

B1L103S, U7-ch26, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 61
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

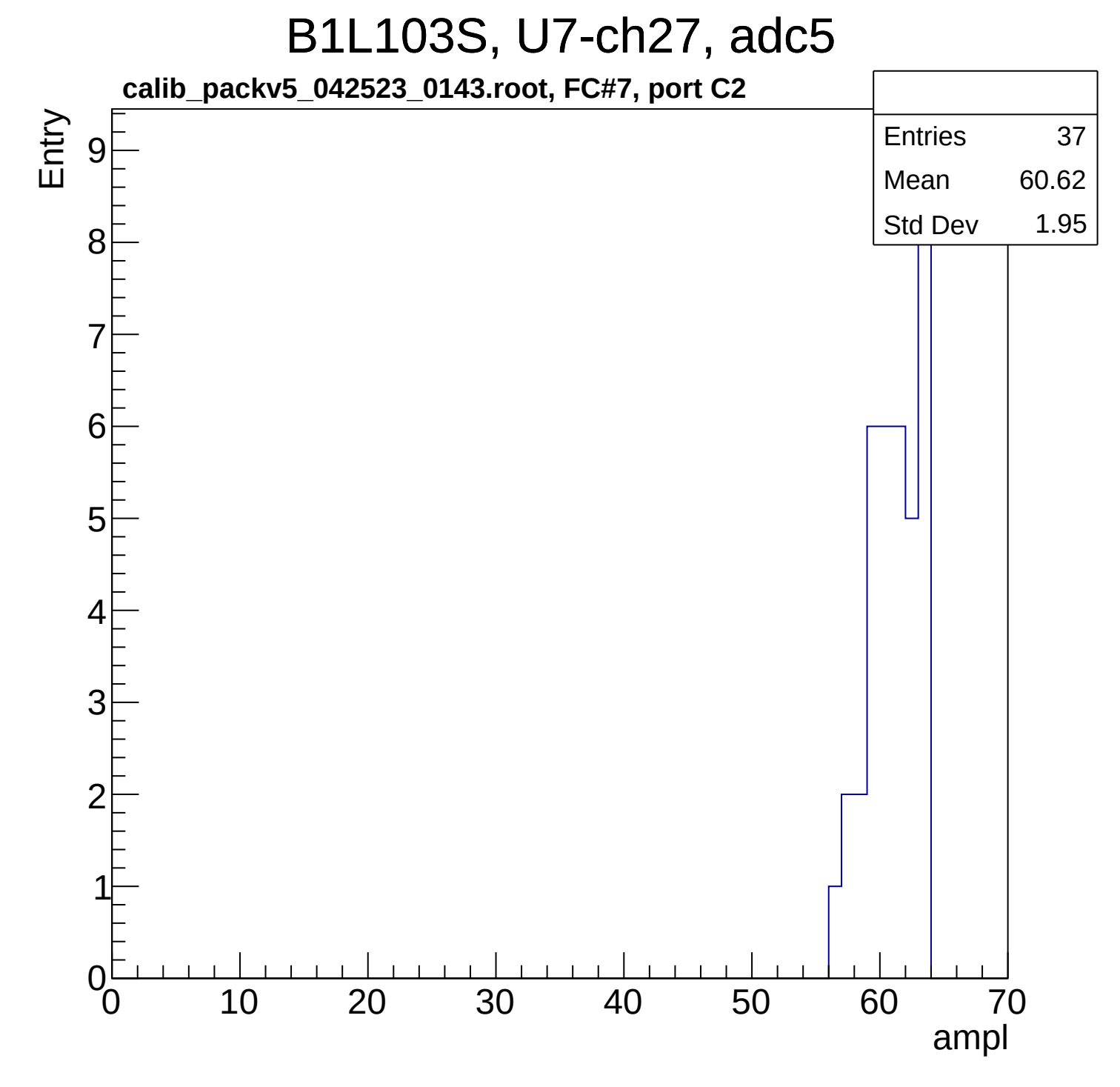

B1L103S, U7-ch27, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 72
Mean 28.38
Std Dev 7.013
Gaus mean : 29.3253
Gaus Width: 3.8166
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

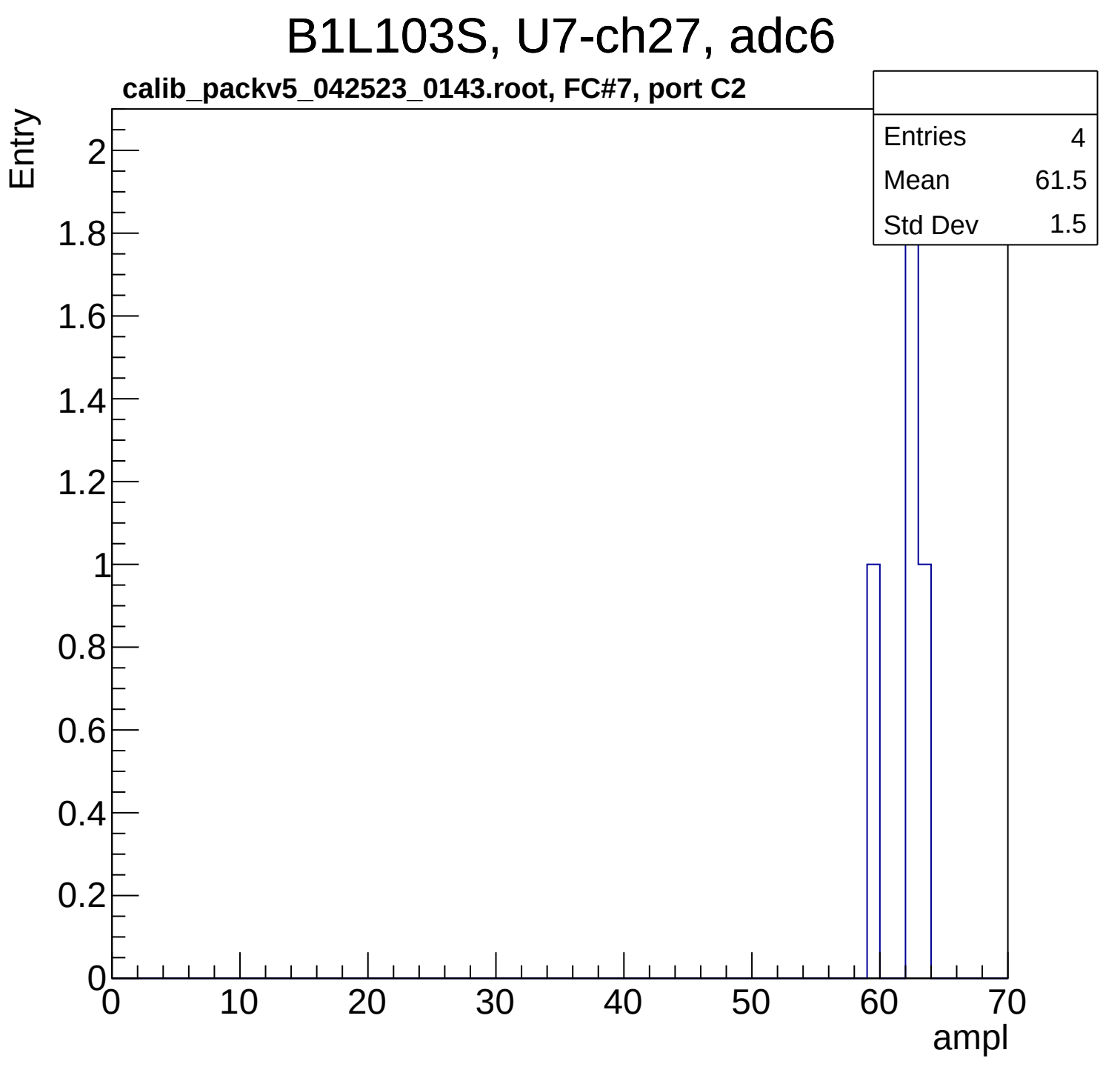

B1L103S, U7-ch27, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 78
Mean 36.78
Std Dev 3.514
Gaus mean : 37.2151
Gaus Width: 3.6829
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

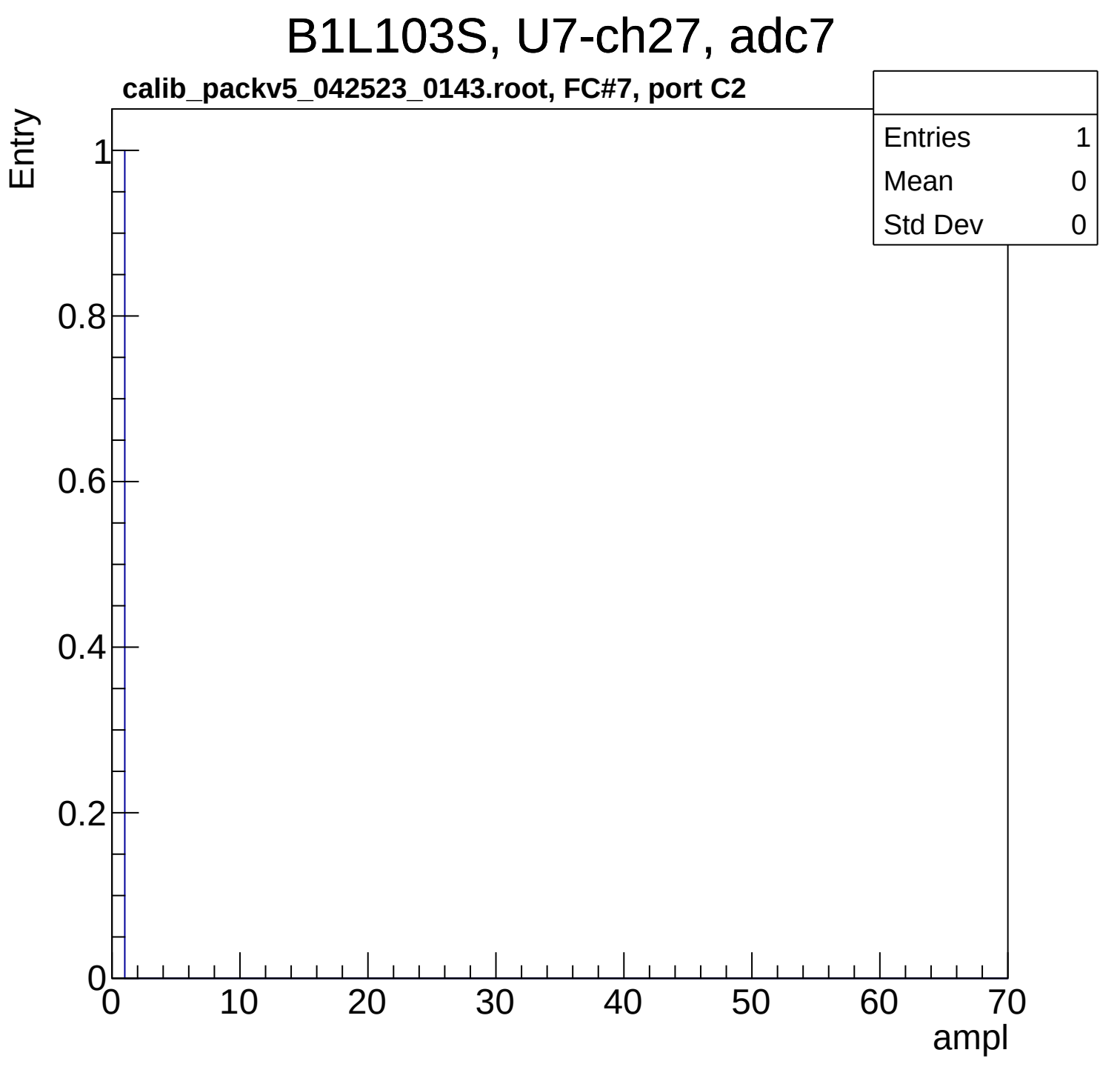

B1L103S, U7-ch27, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 47
Mean 43.17
Std Dev 2.554
Gaus mean : 43.5881
Gaus Width: 2.8284
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

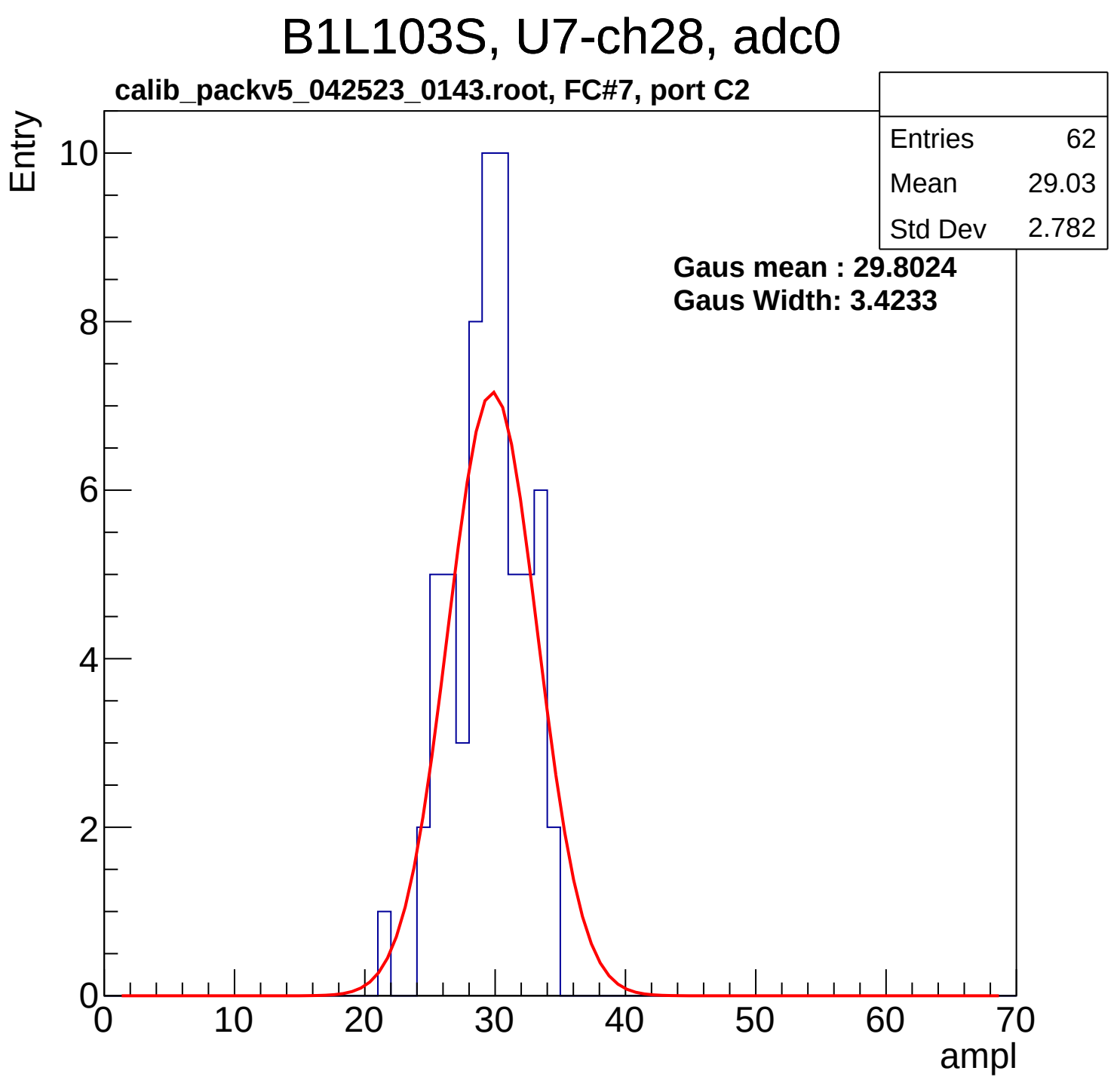

B1L103S, U7-ch27, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 61
Mean 48.59
Std Dev 2.916
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

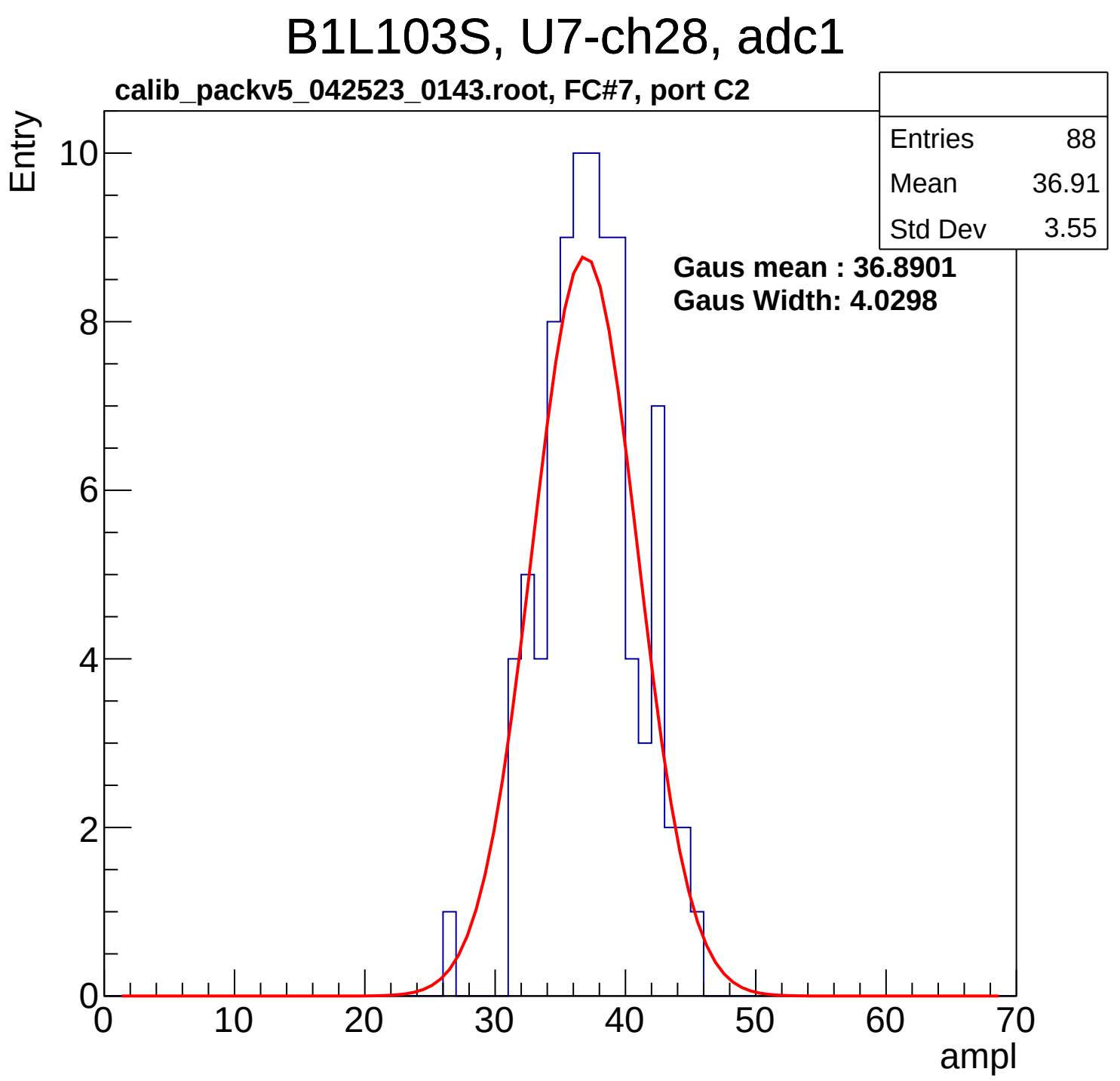

B1L103S, U7-ch27, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 78
Mean 54.94
Std Dev 6.993
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

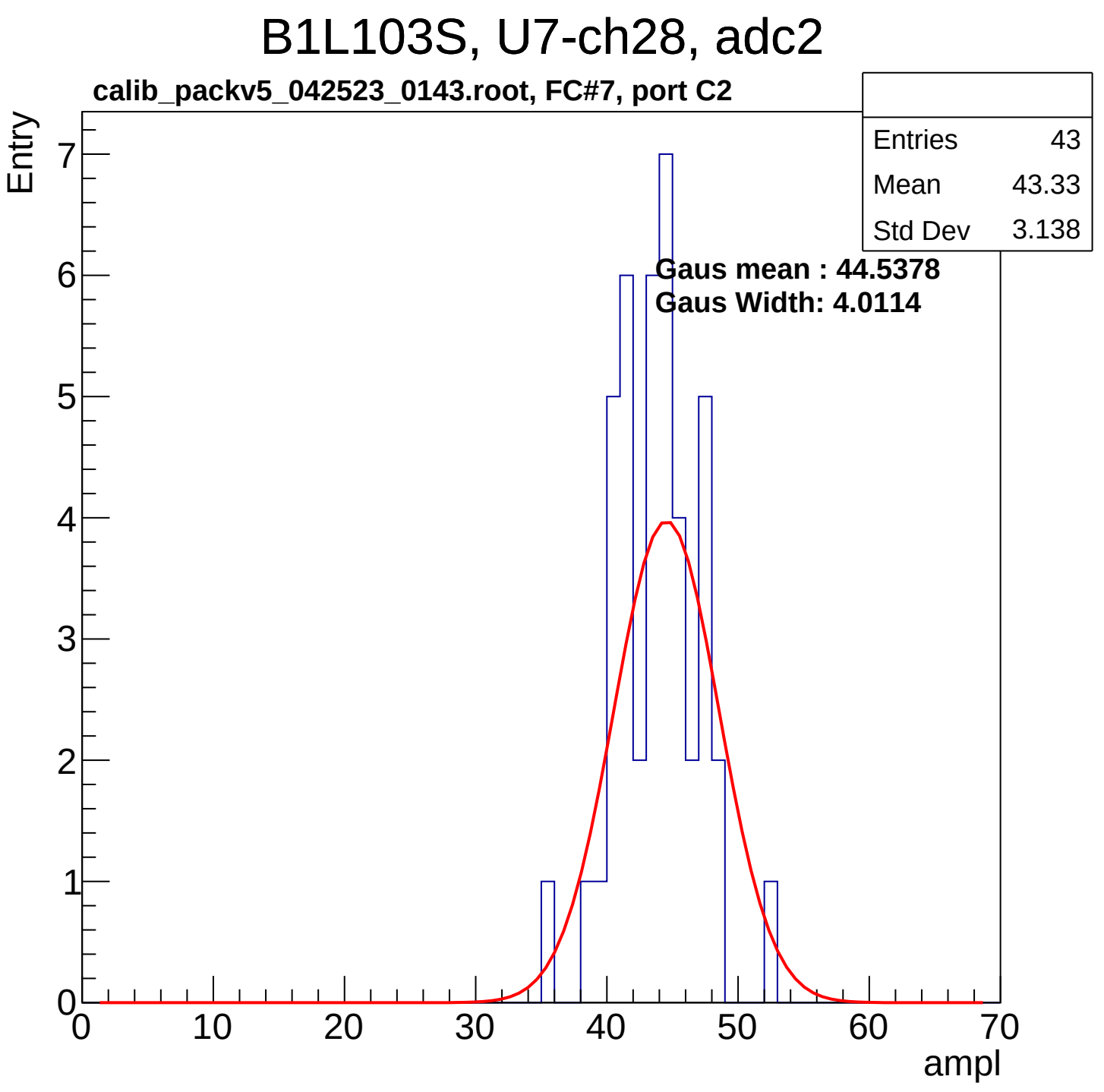

B1L103S, U7-ch27, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 37
Mean 60.62
Std Dev 1.95
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

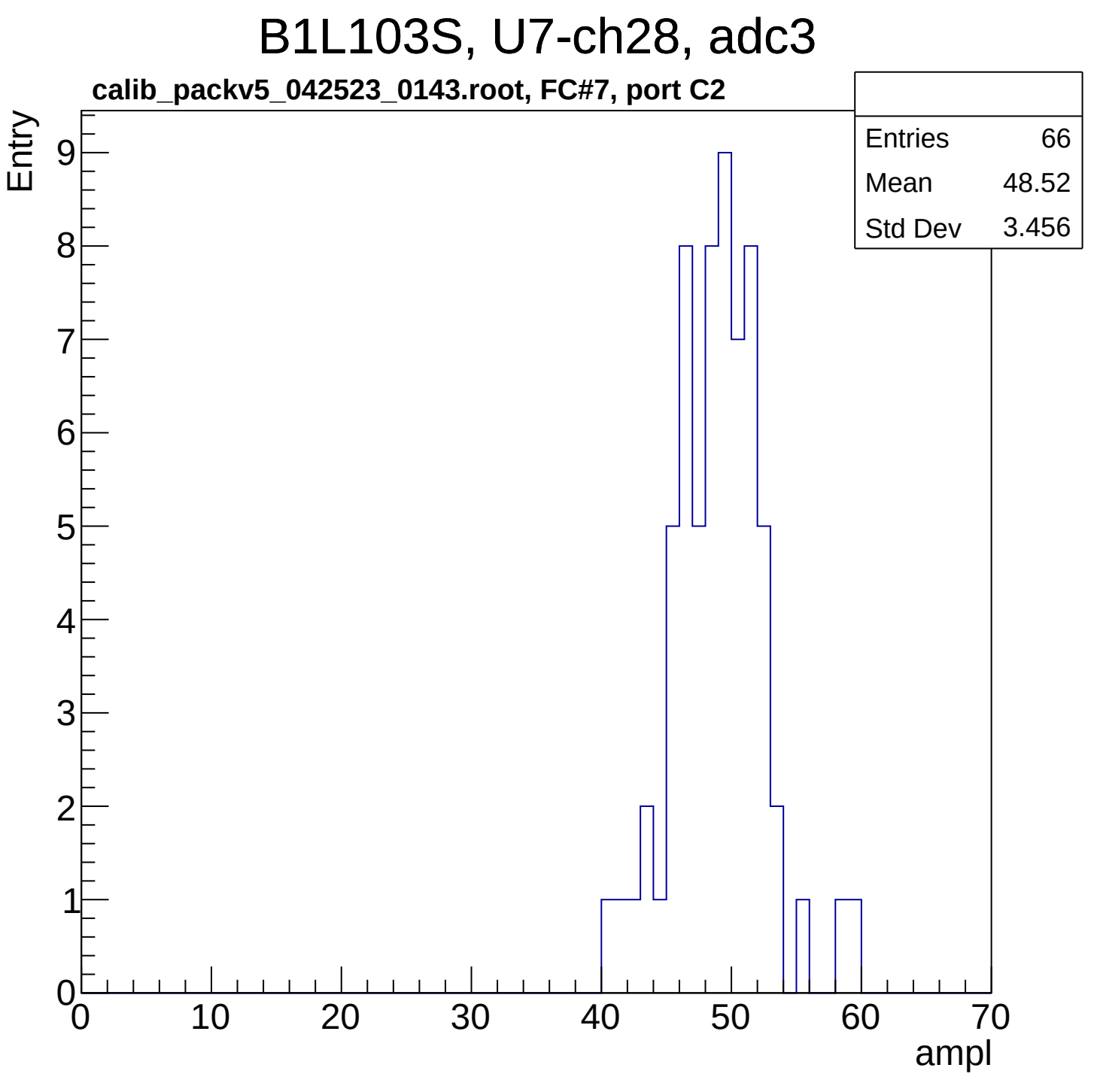

B1L103S, U7-ch27, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 4
Mean 61.5
Std Dev 1.5
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

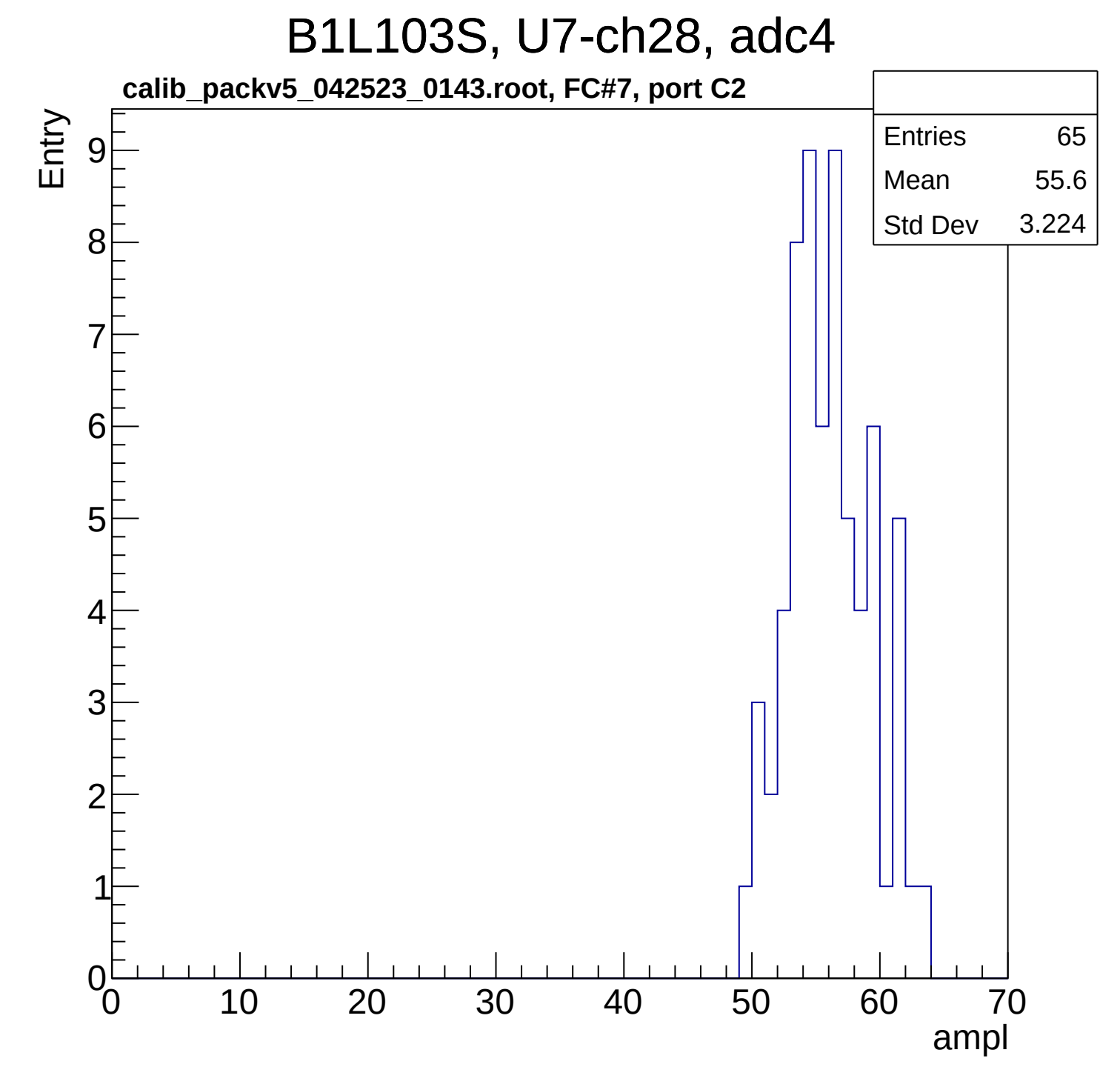

B1L103S, U7-ch27, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

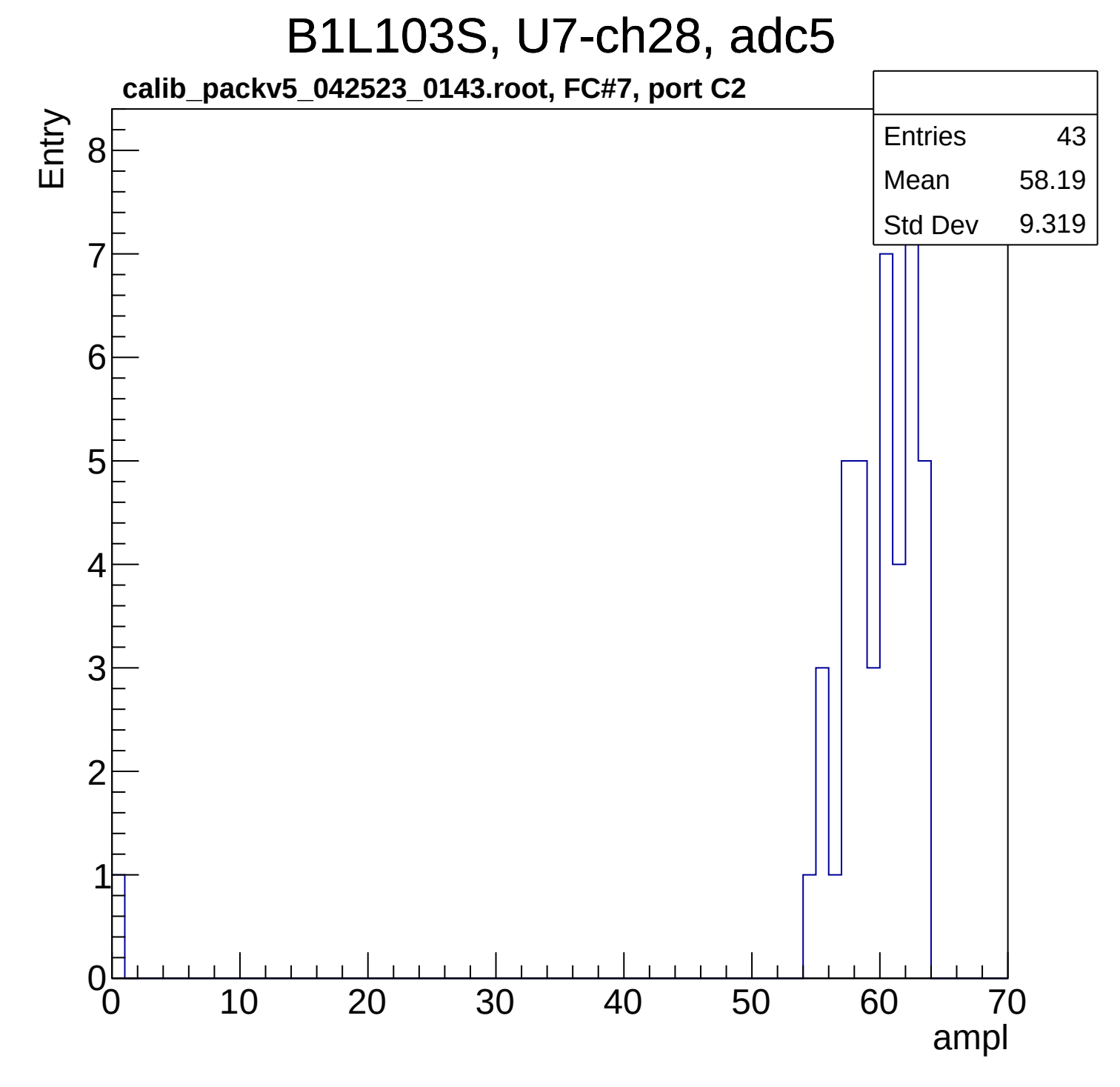

B1L103S, U7-ch28, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 62
Mean 29.03
Std Dev 2.782
Gaus mean : 29.8024
Gaus Width: 3.4233
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch28, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 88
Mean 36.91
Std Dev 3.55
Gaus mean : 36.8901
Gaus Width: 4.0298
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch28, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 43
Mean 43.33
Std Dev 3.138
Gaus mean : 44.5378
Gaus Width: 4.0114
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch28, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 48.52
Std Dev 3.456
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch28, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 55.6
Std Dev 3.224
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch28, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 43
Mean 58.19
Std Dev 9.319
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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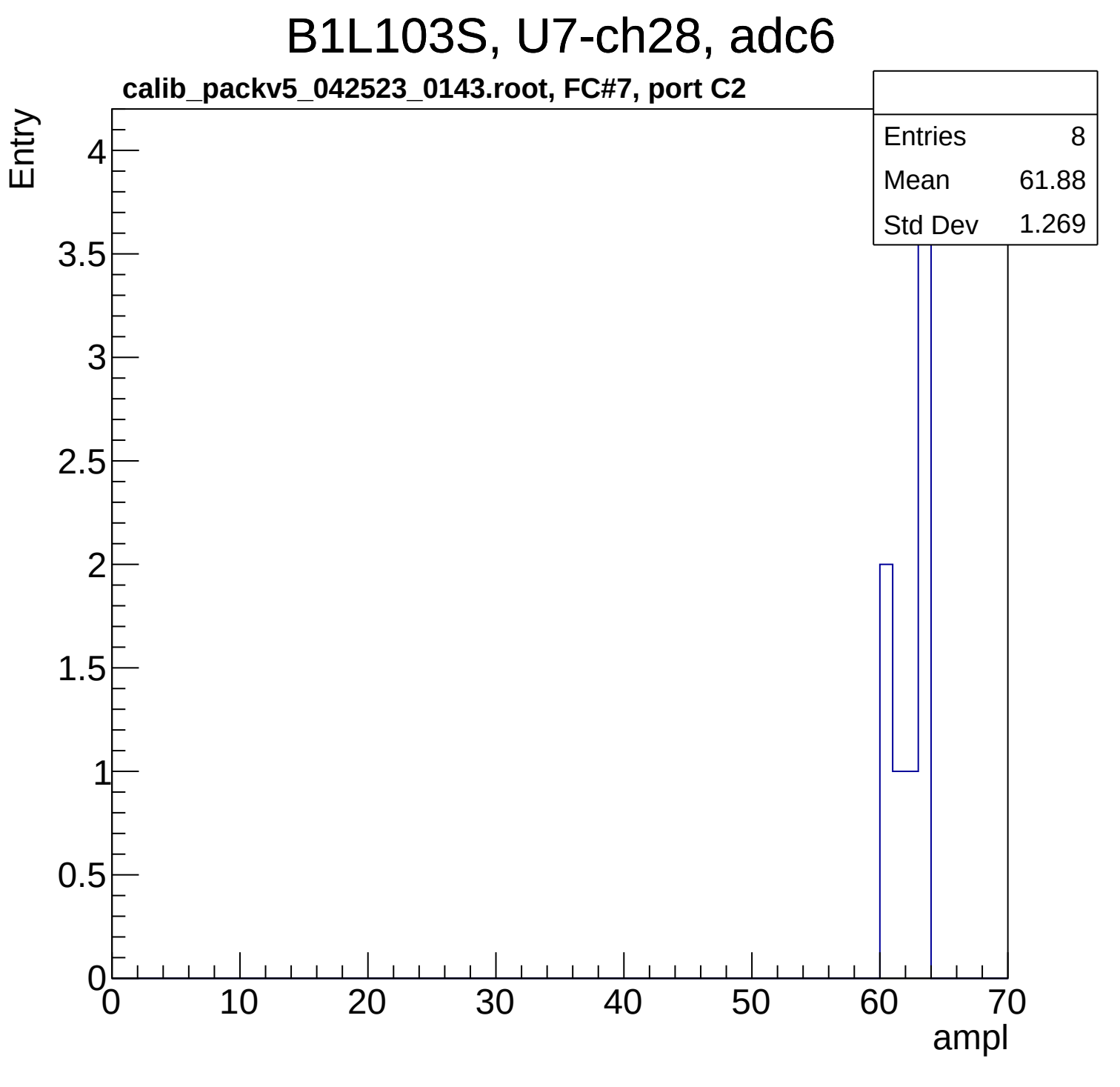
40
50
60
70


B1L103S, U7-ch28, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 8
Mean 61.88
Std Dev 1.269
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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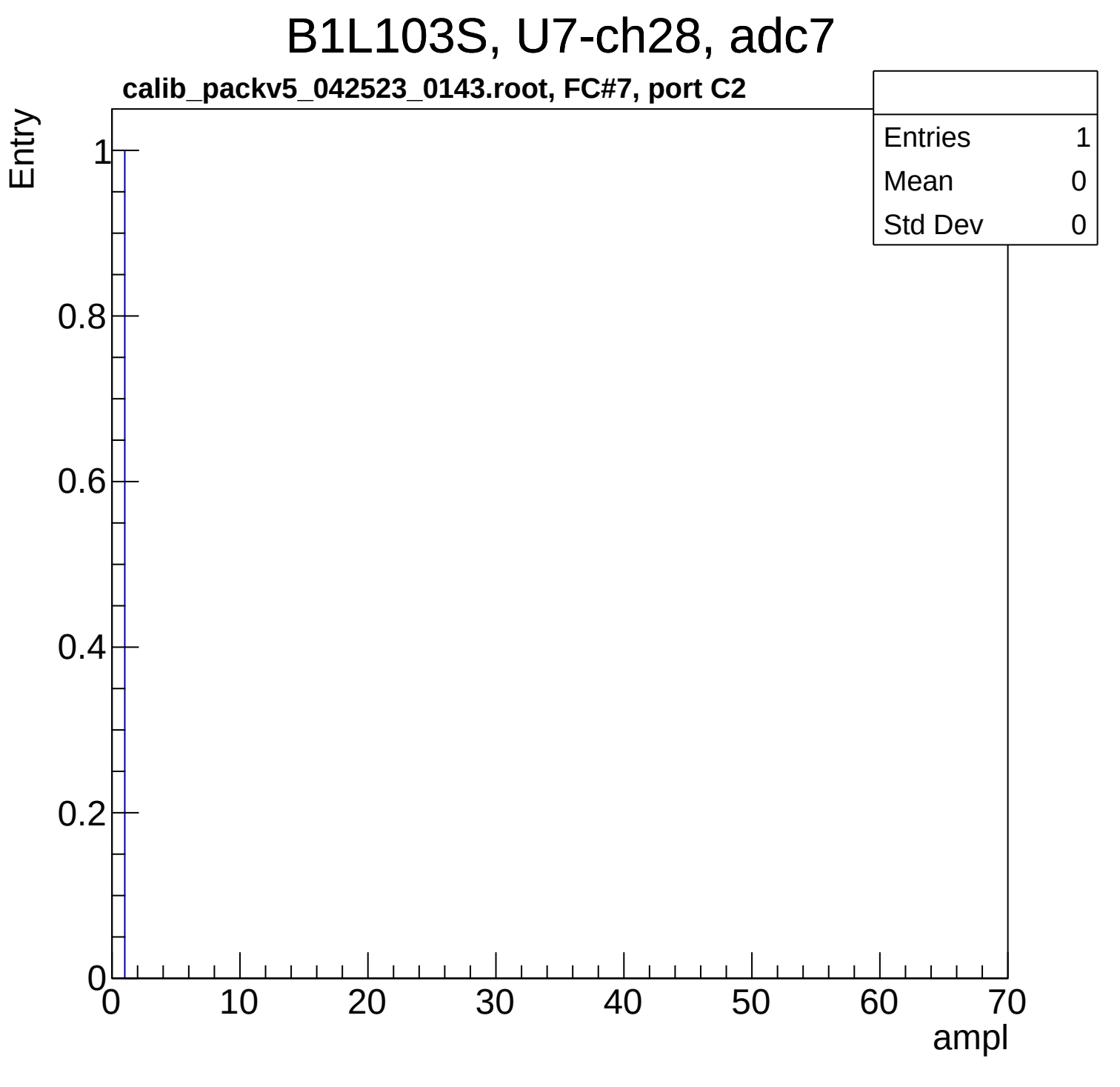
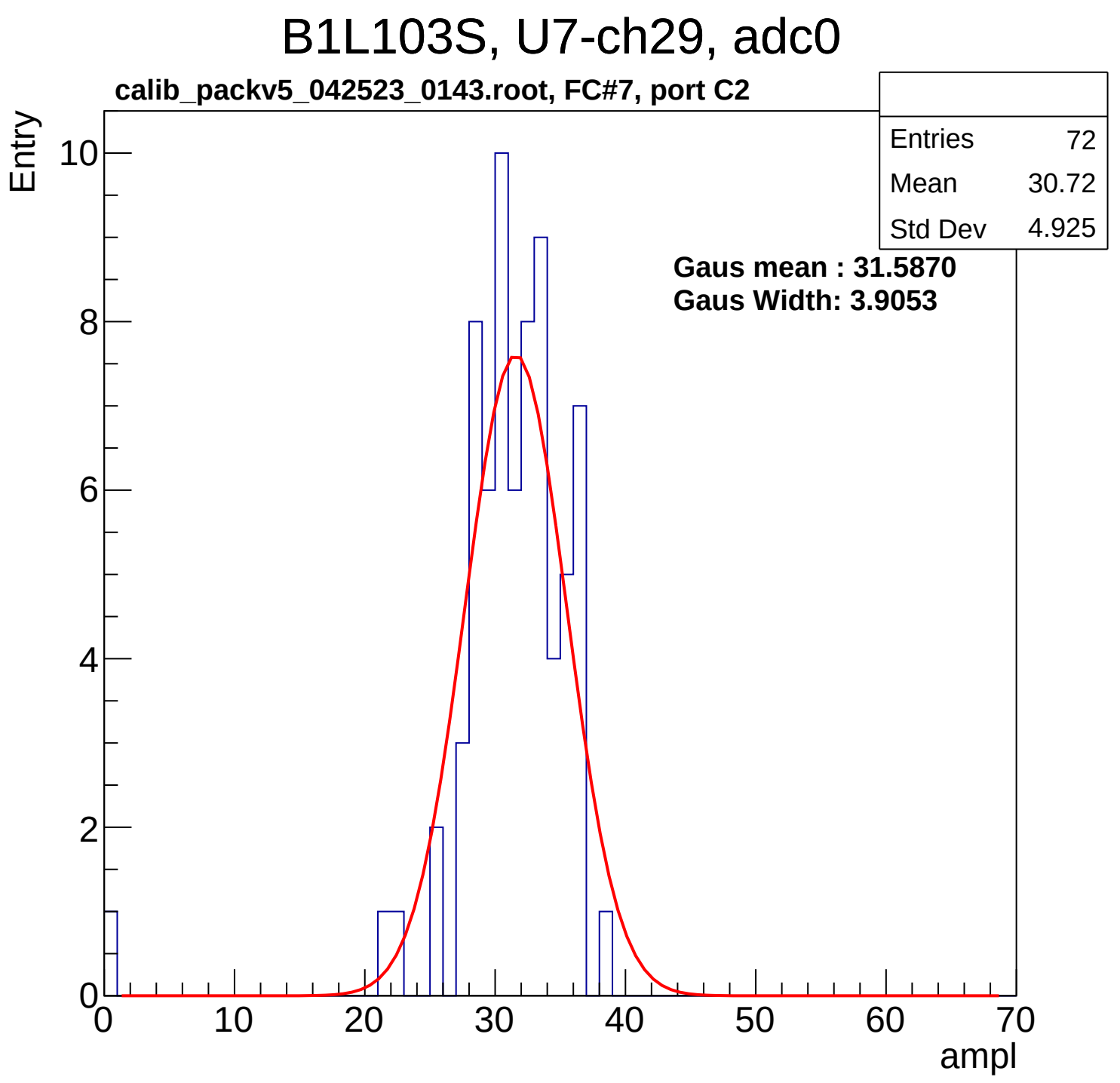
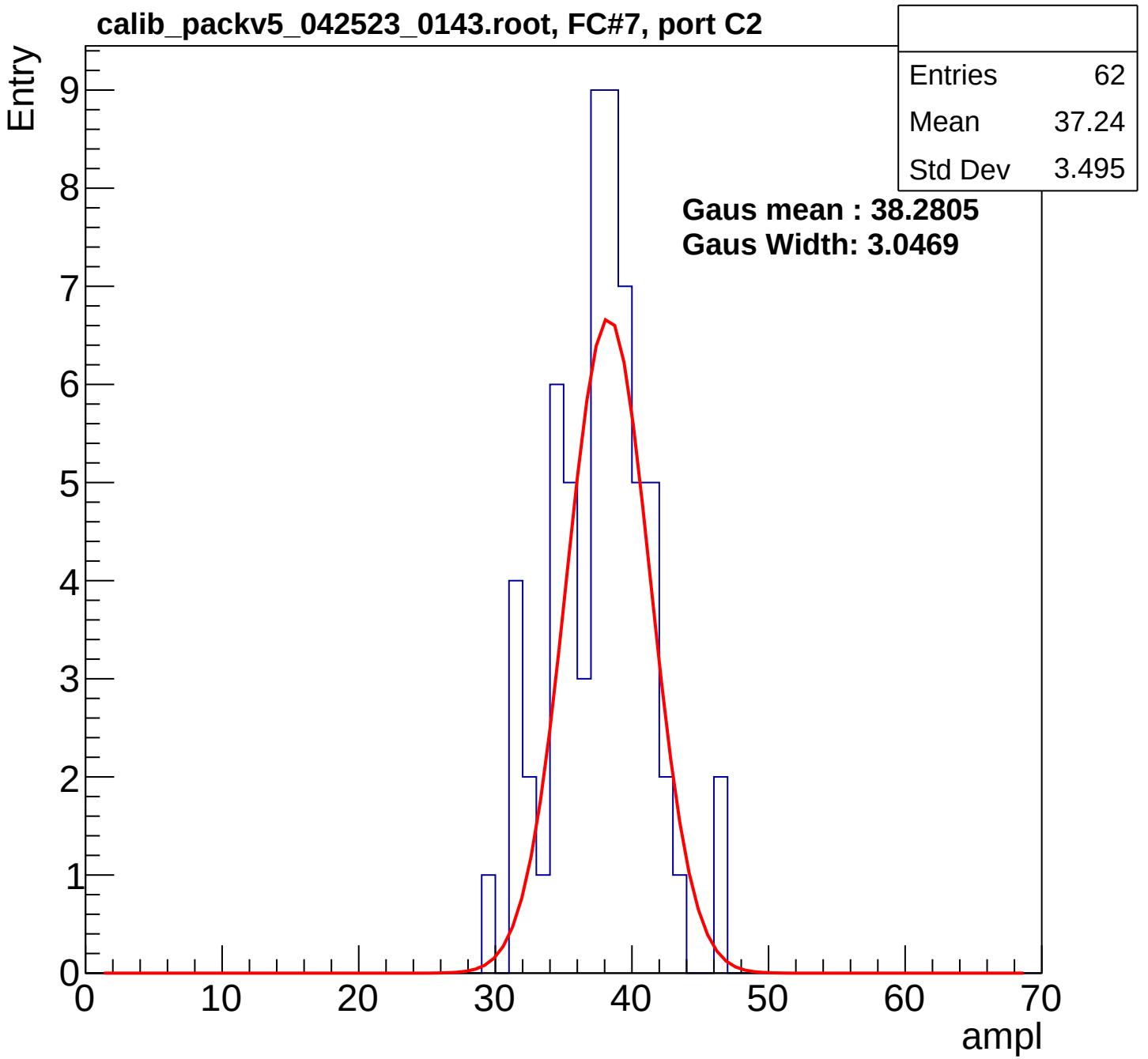
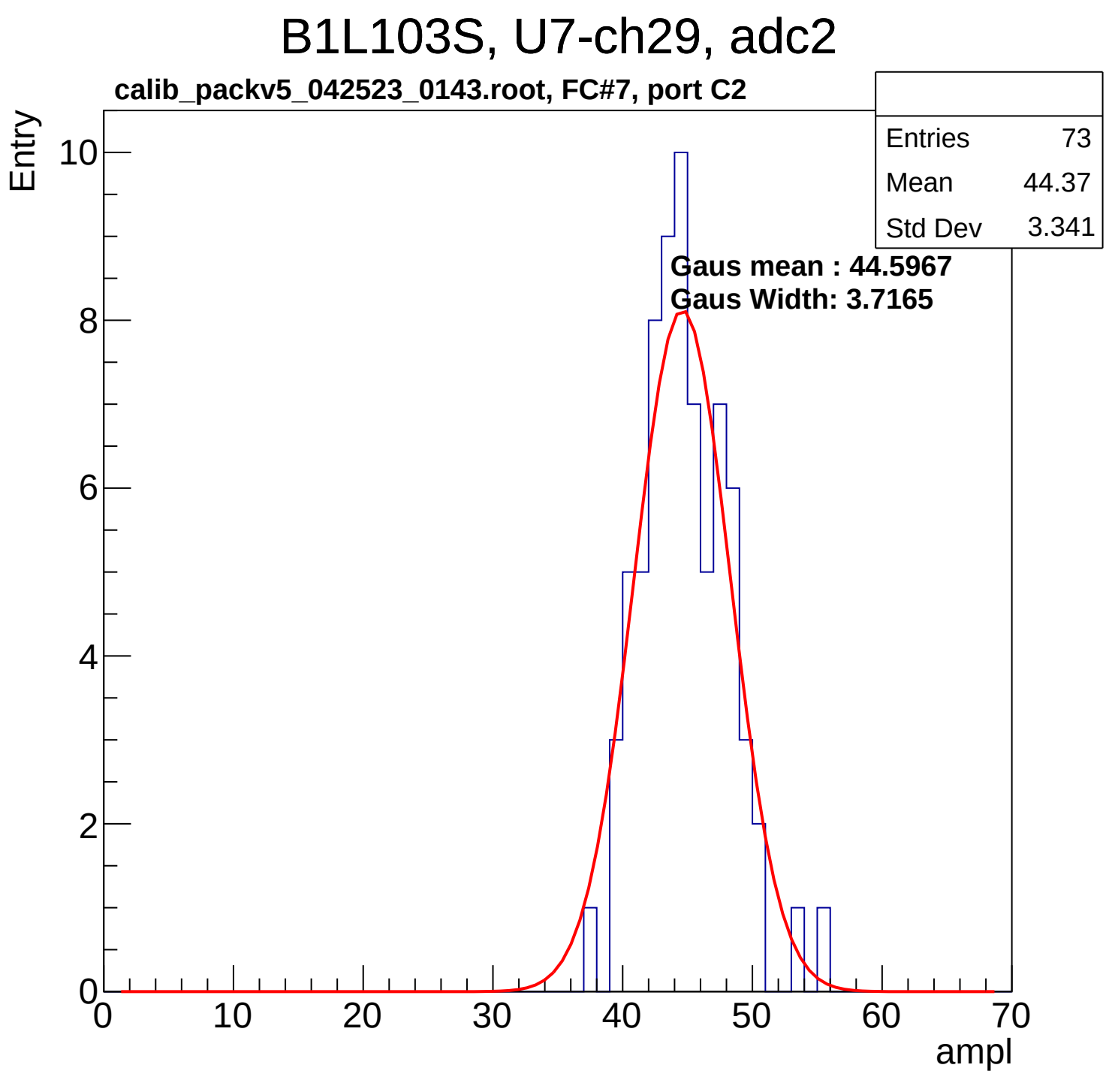
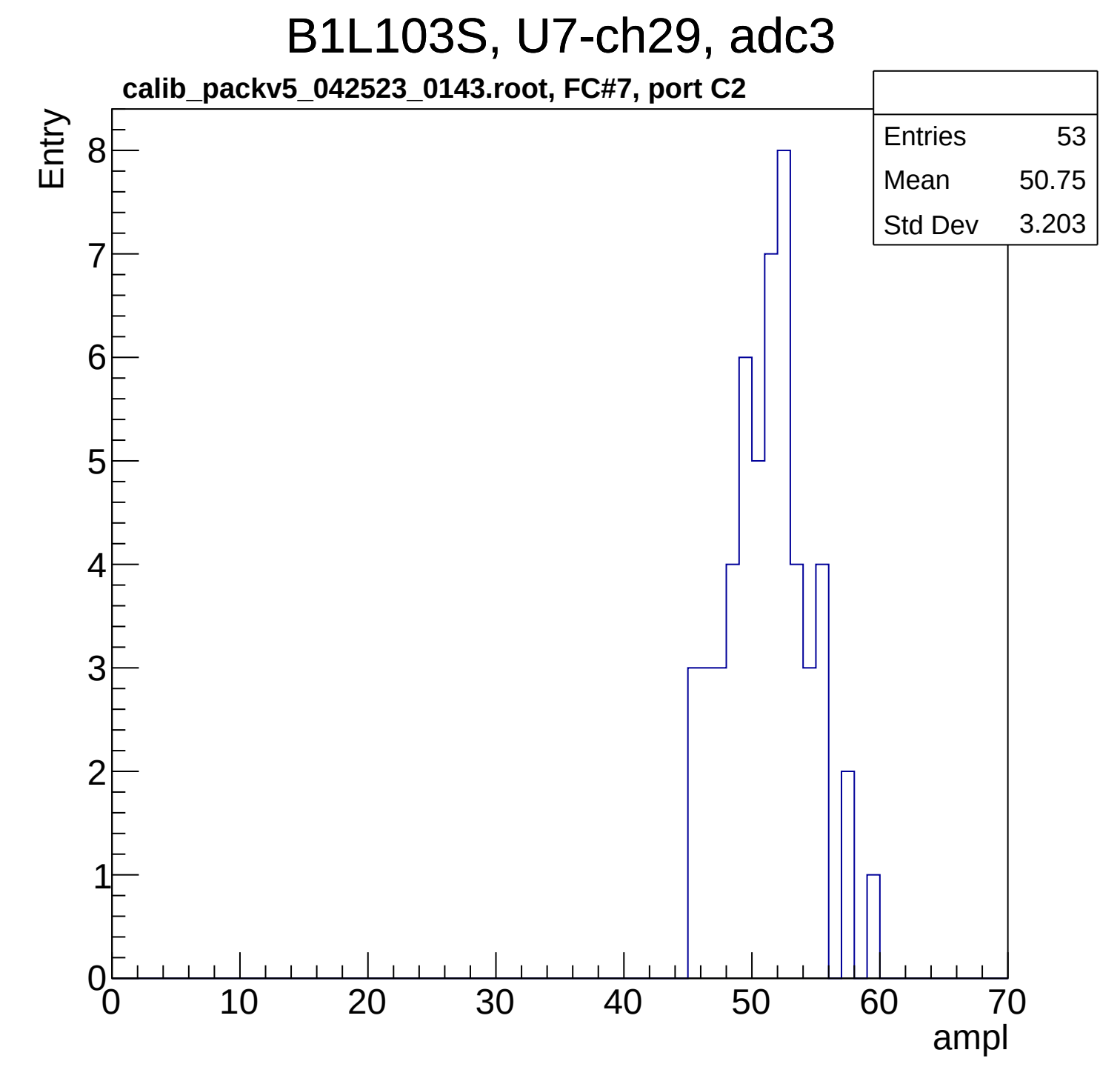
40
50
60
70


B1L103S, U7-ch28, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch29, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 72
Mean 30.72
Std Dev 4.925
Gaus mean : 31.5870
Gaus Width: 3.9053
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch29, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 62
Mean 37.24
Std Dev 3.495
Gaus mean : 38.2805
Gaus Width: 3.0469
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch29, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 73
Mean 44.37
Std Dev 3.341
Gaus mean : 44.5967
Gaus Width: 3.7165
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch29, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 50.75
Std Dev 3.203
Entry
ampl
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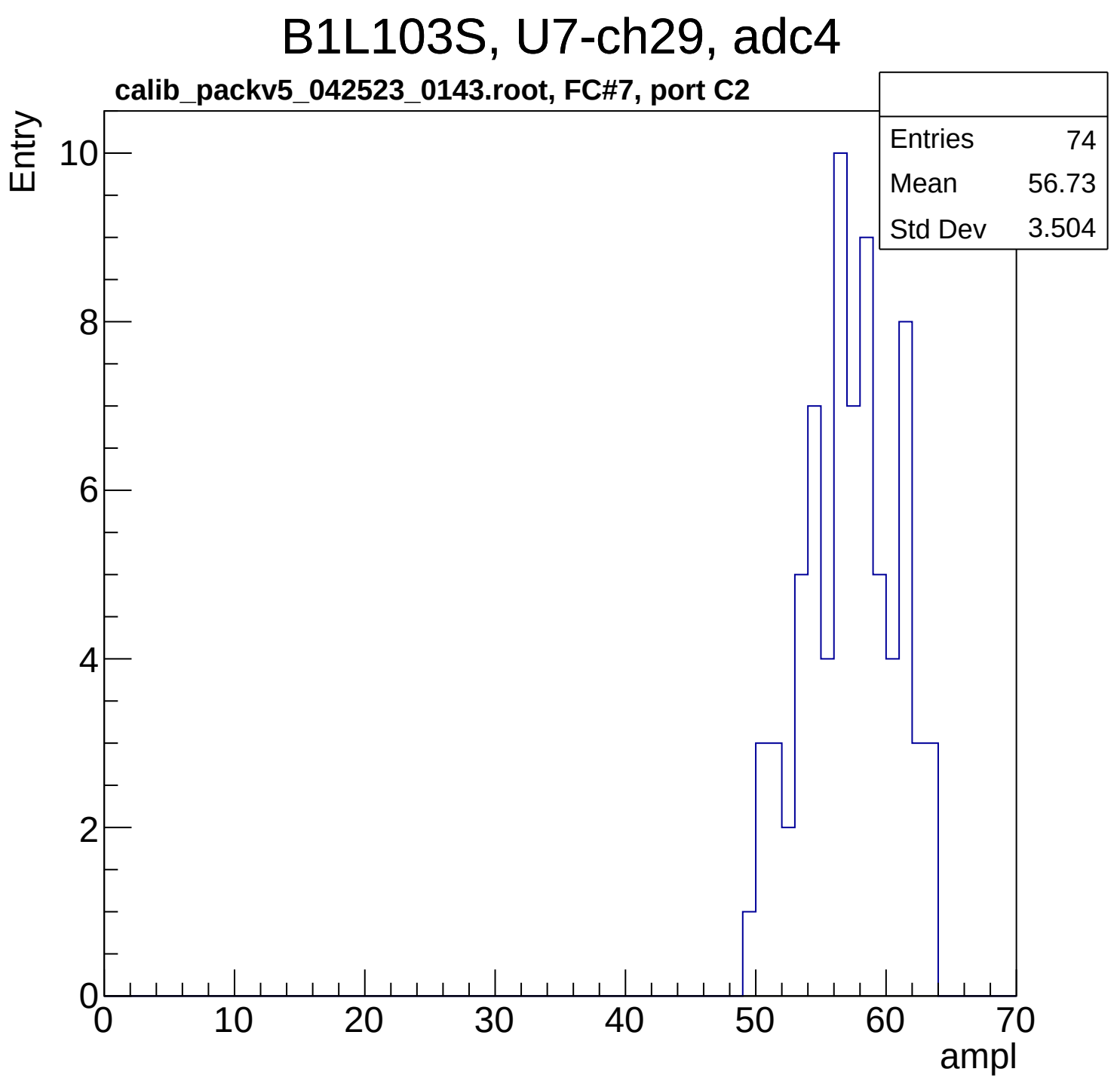
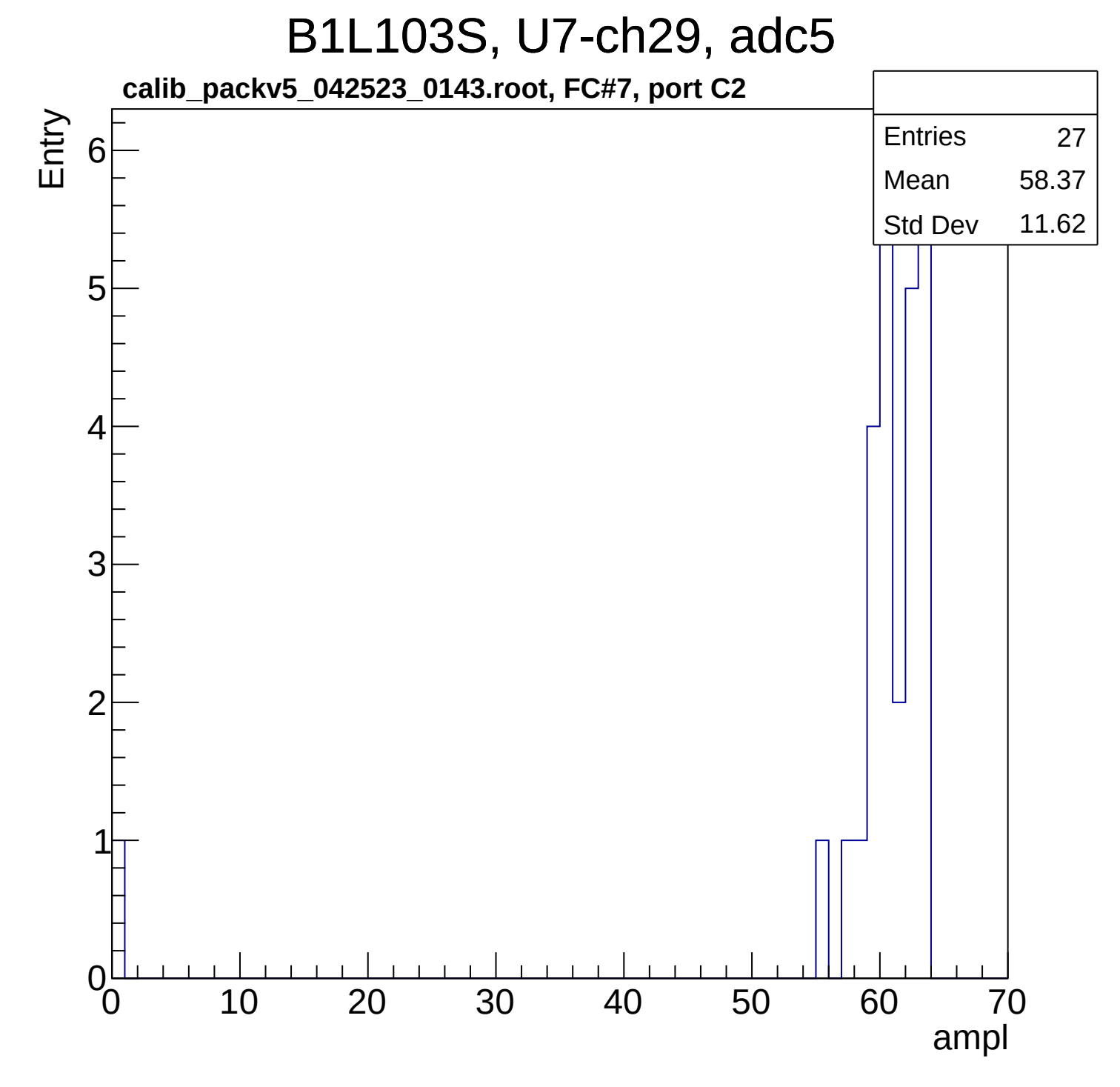
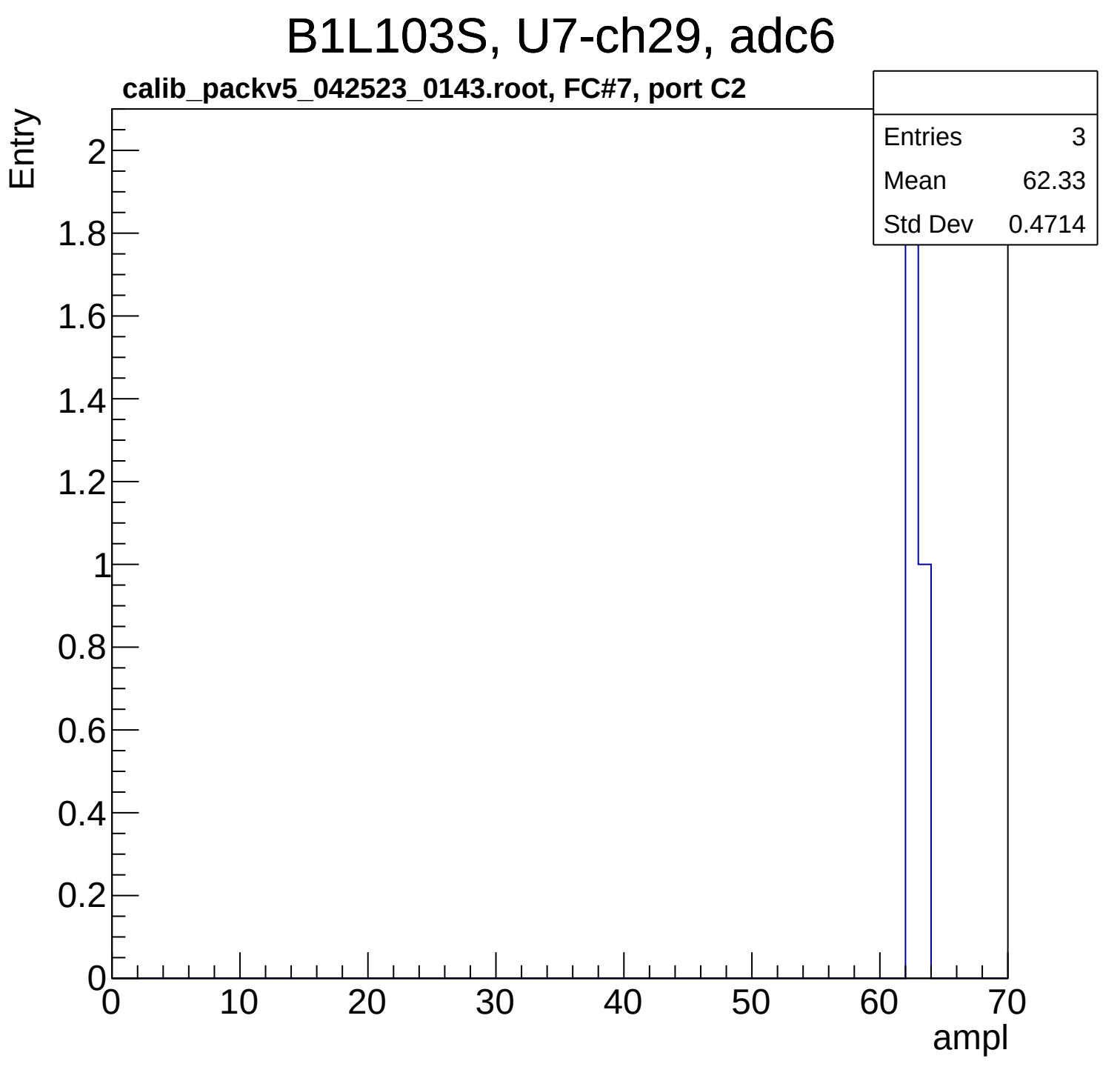
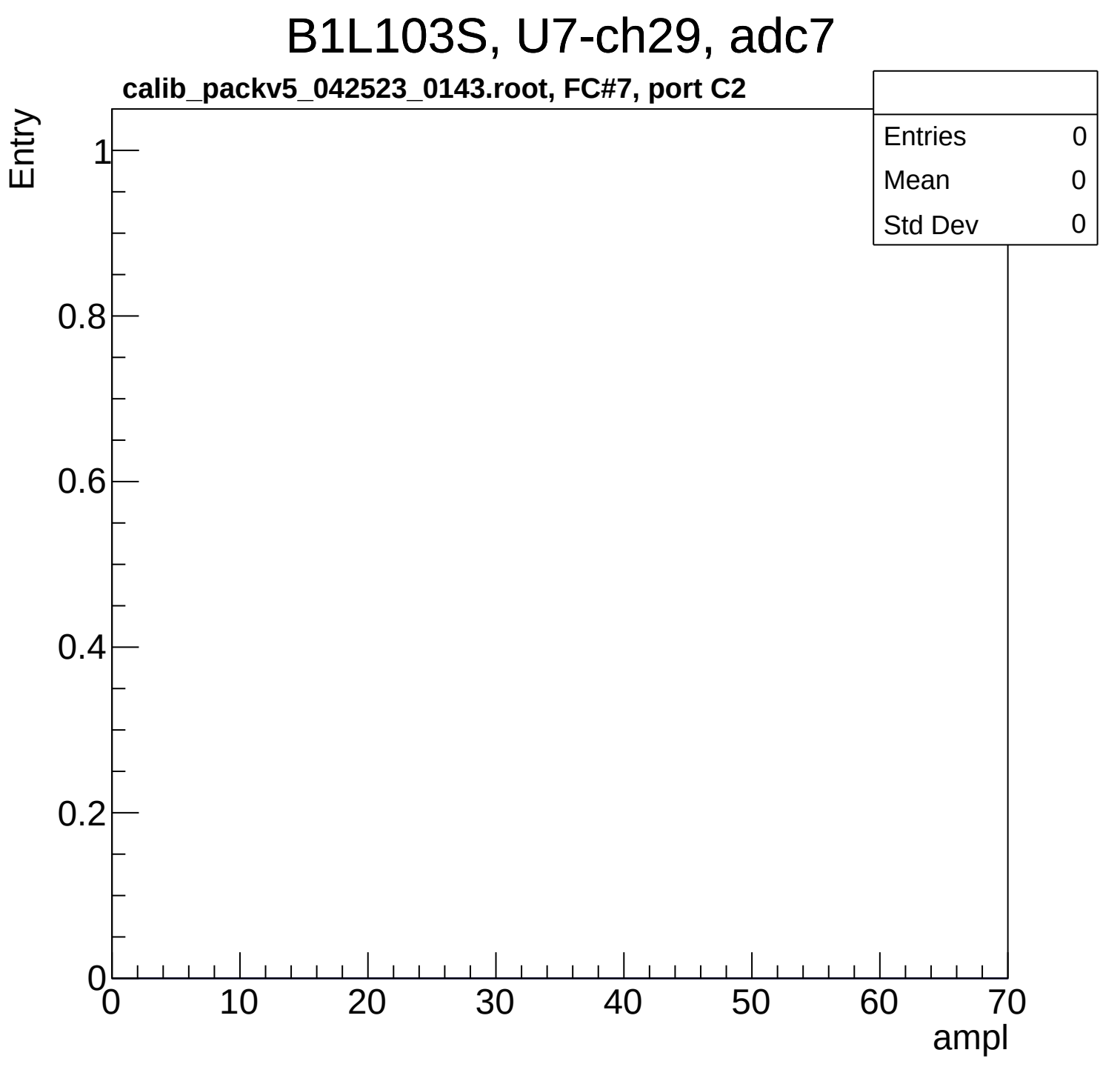
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch29, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 74
Mean 56.73
Std Dev 3.504
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch29, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 27
Mean 58.37
Std Dev 11.62
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U7-ch29, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 62.33
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U7-ch29, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
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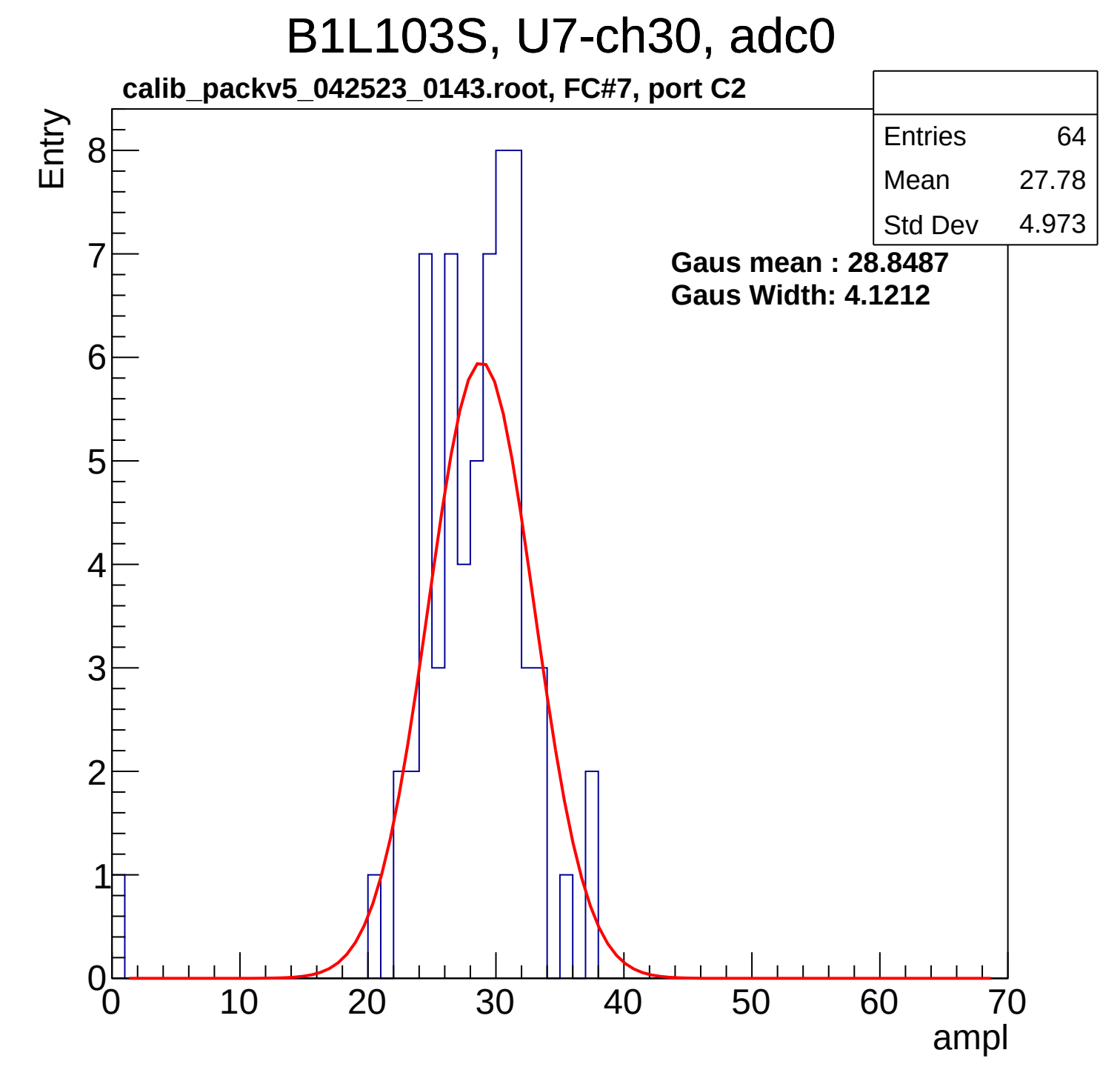
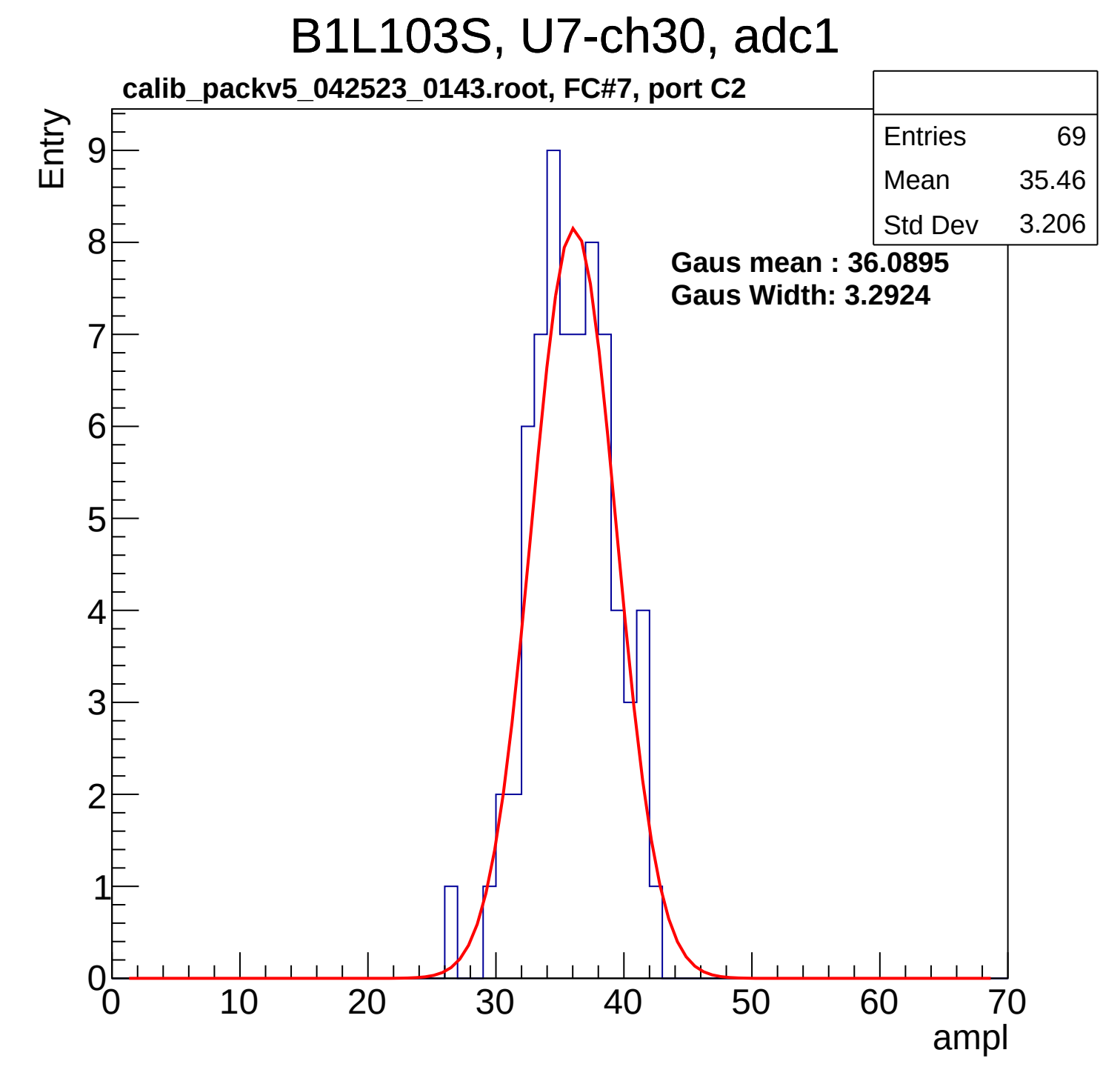
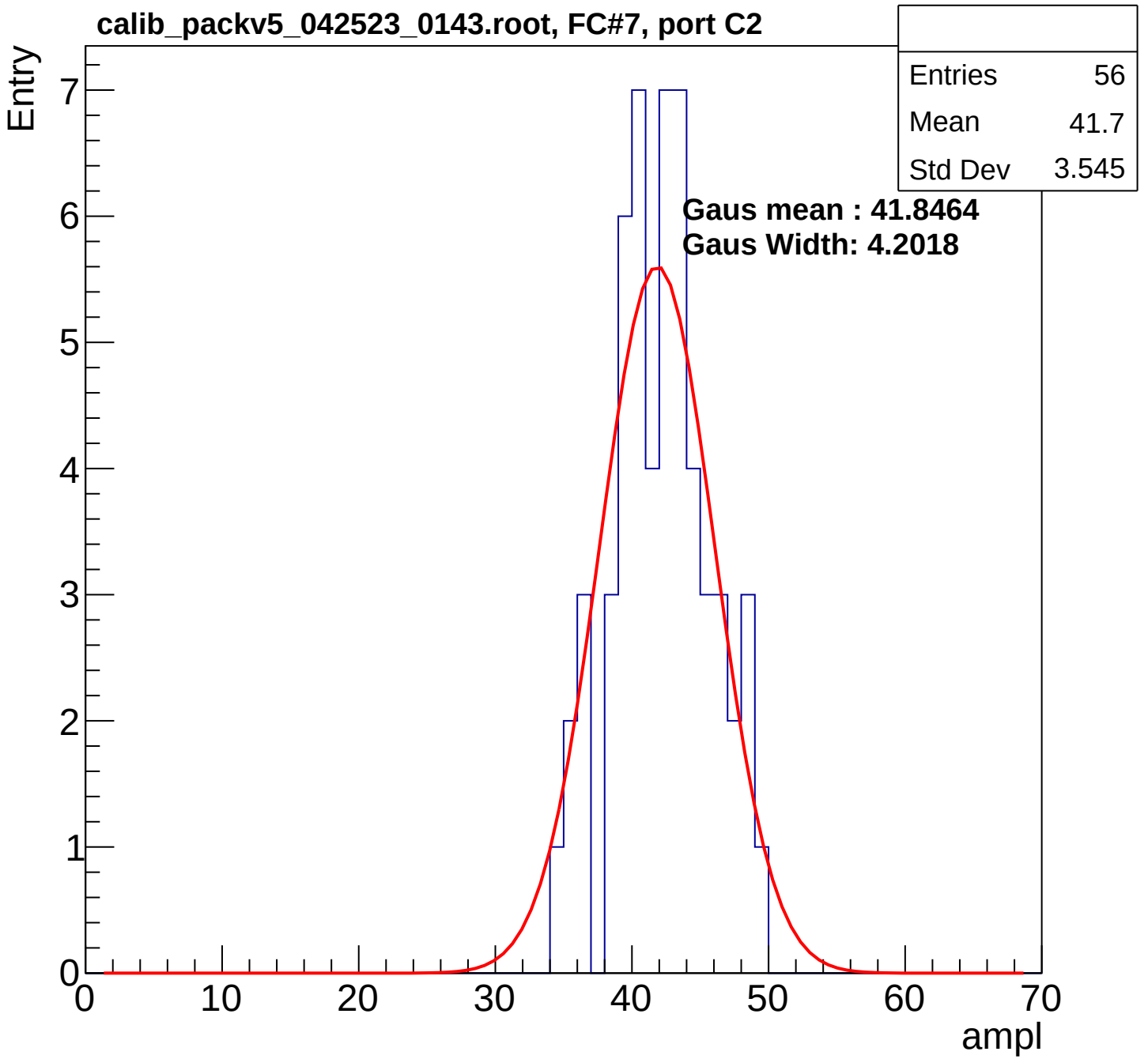
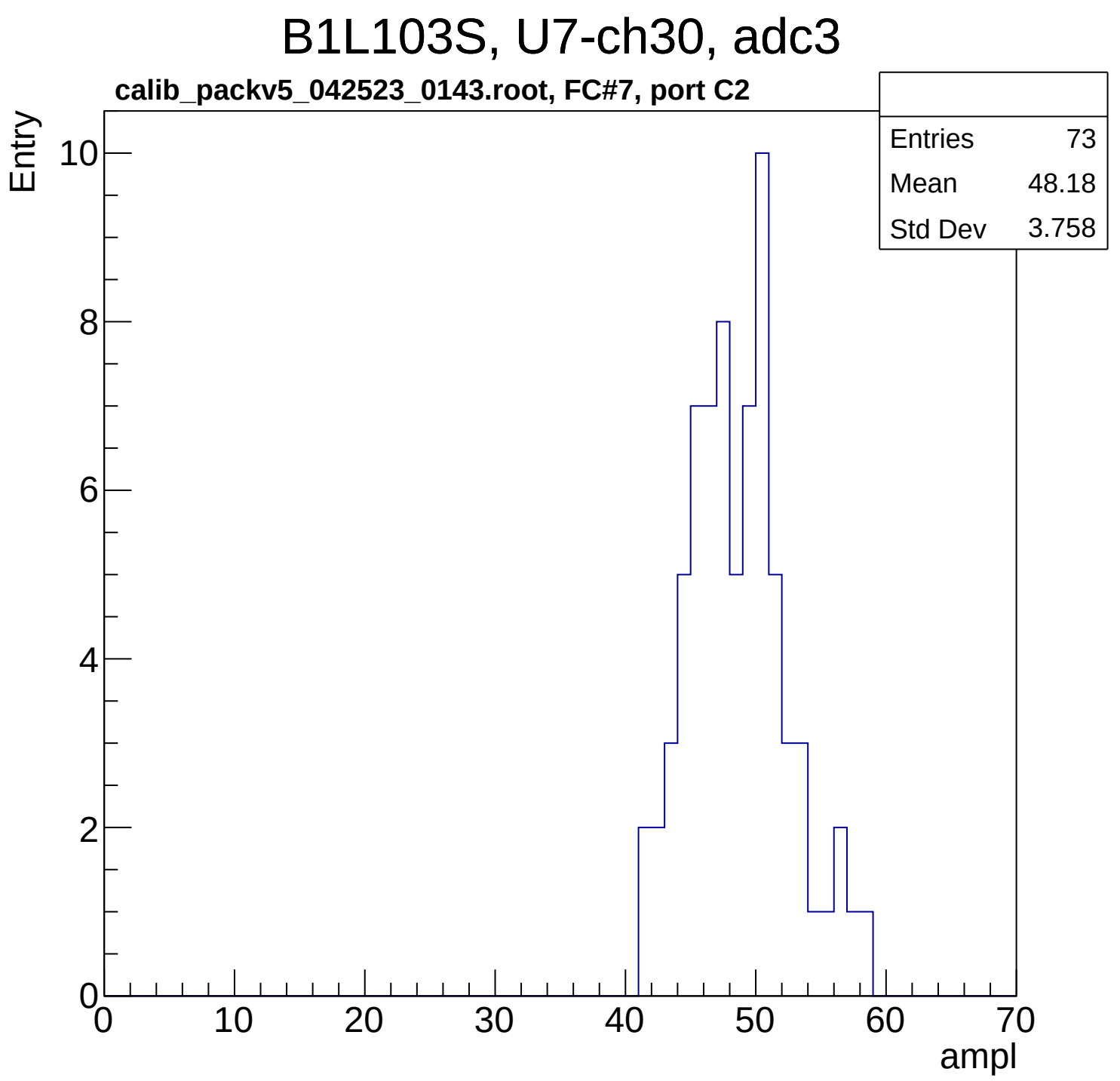
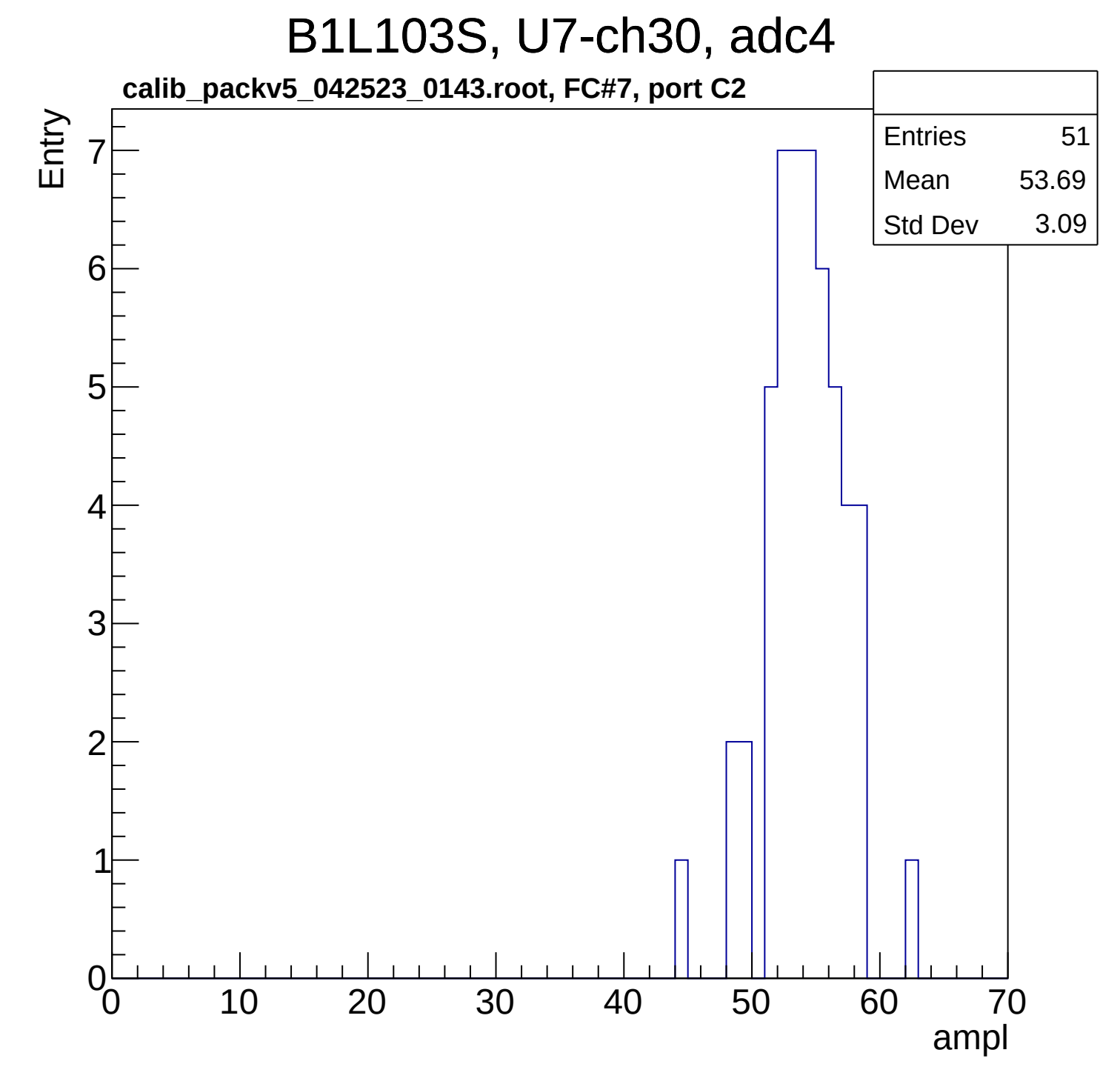
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

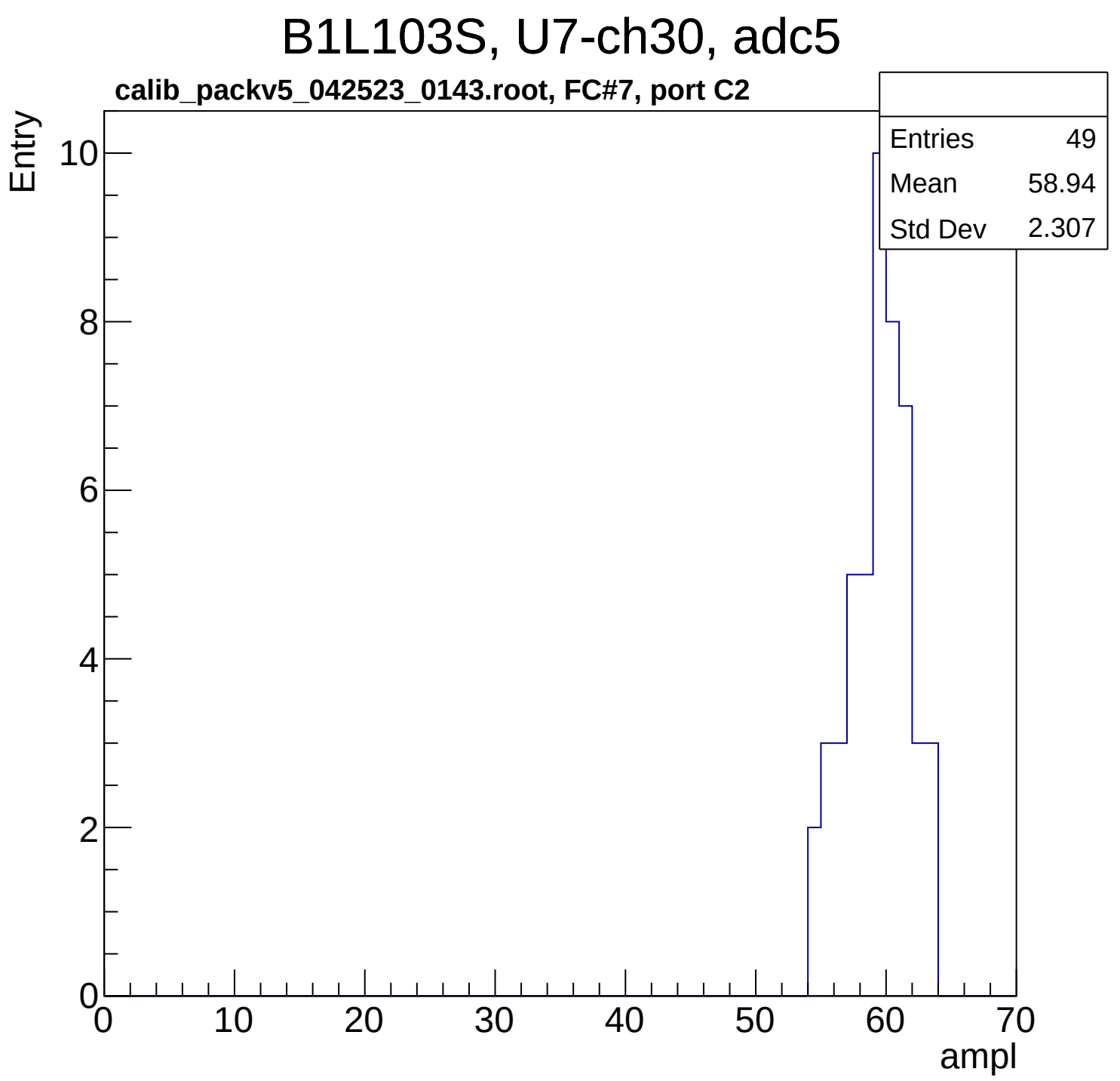

B1L103S, U7-ch30, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 27.78
Std Dev 4.973
Gaus mean : 28.8487
Gaus Width: 4.1212
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

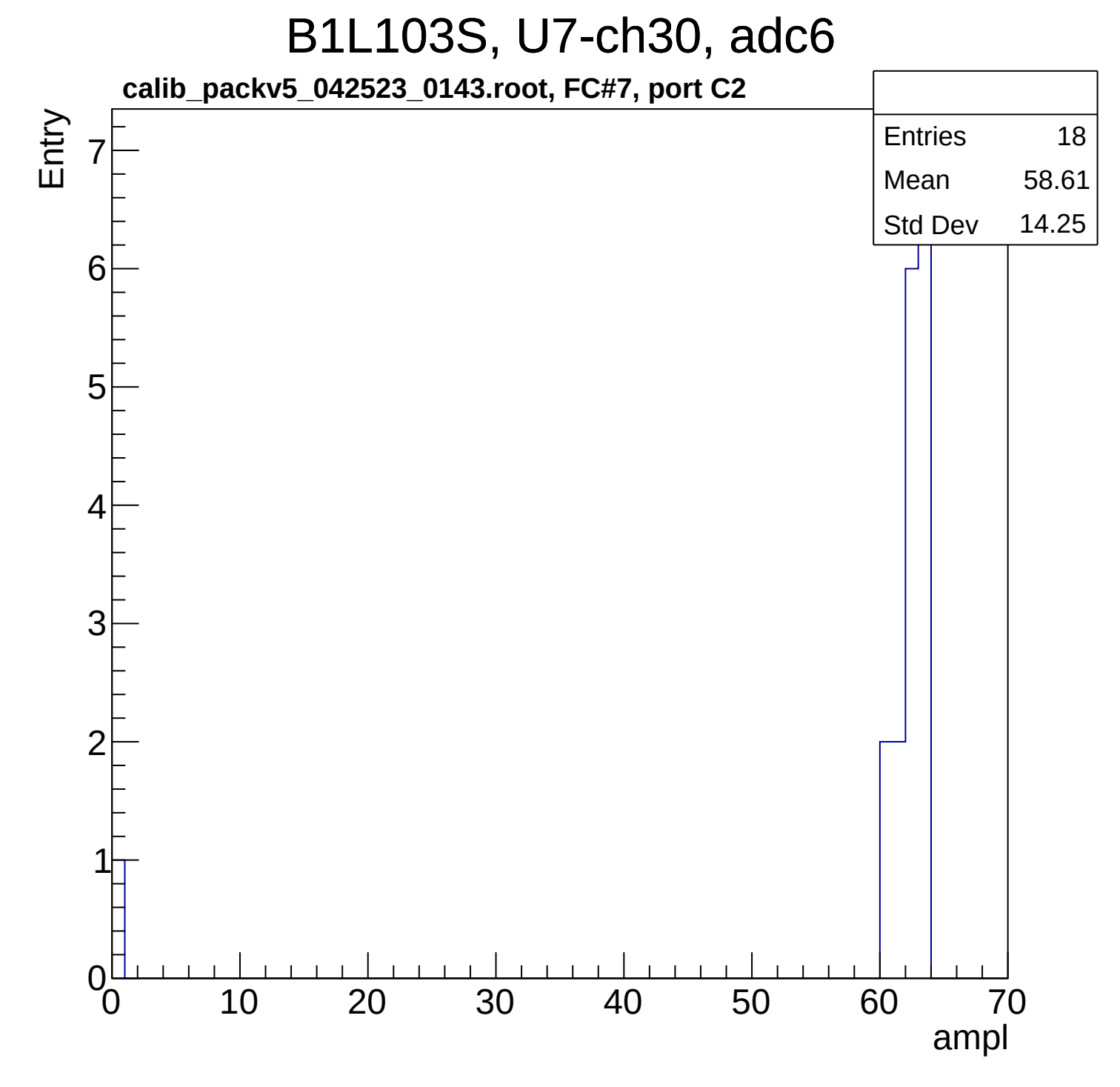

B1L103S, U7-ch30, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 35.46
Std Dev 3.206
Gaus mean : 36.0895
Gaus Width: 3.2924
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

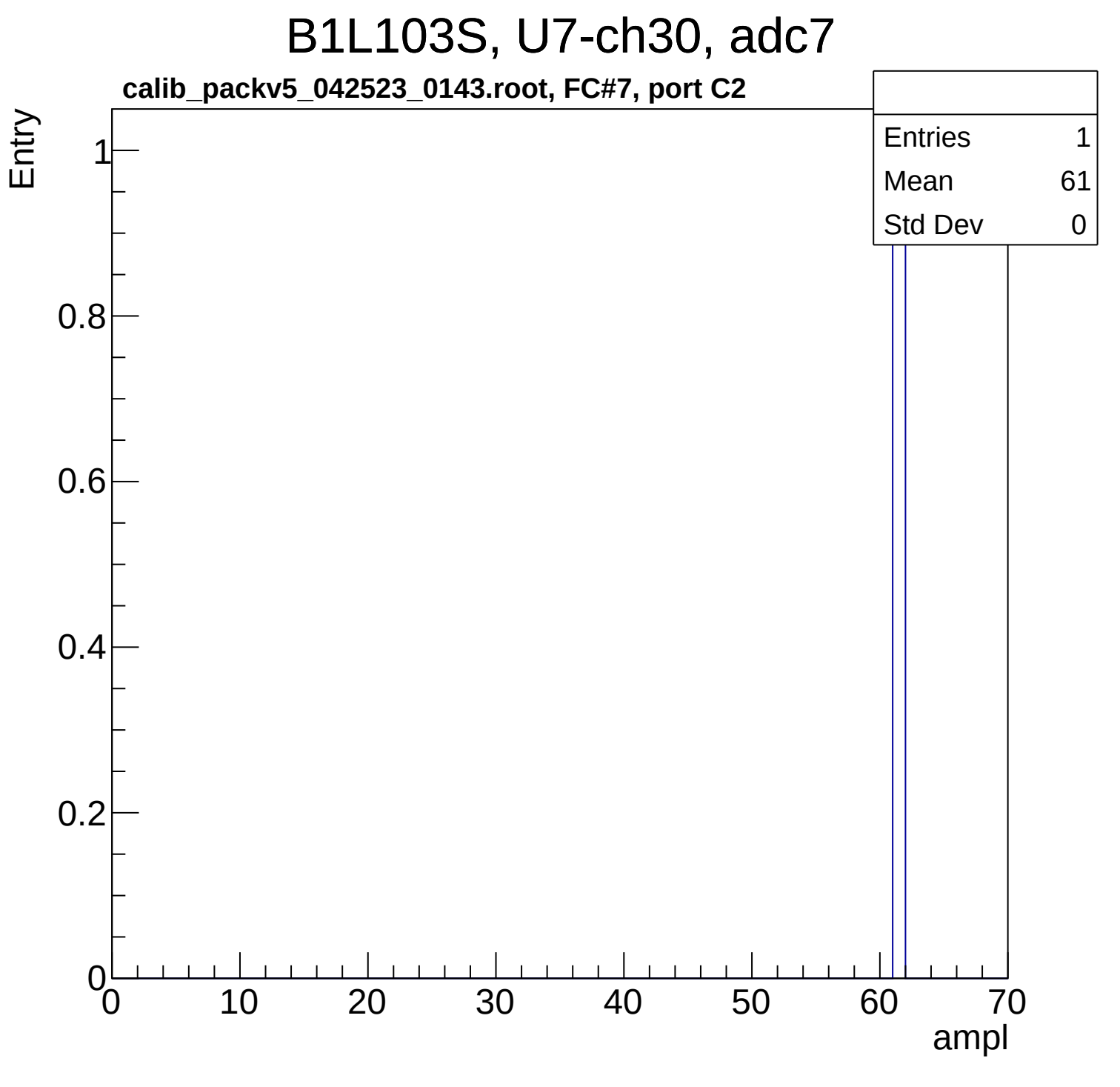

B1L103S, U7-ch30, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 41.7
Std Dev 3.545
Gaus mean : 41.8464
Gaus Width: 4.2018
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

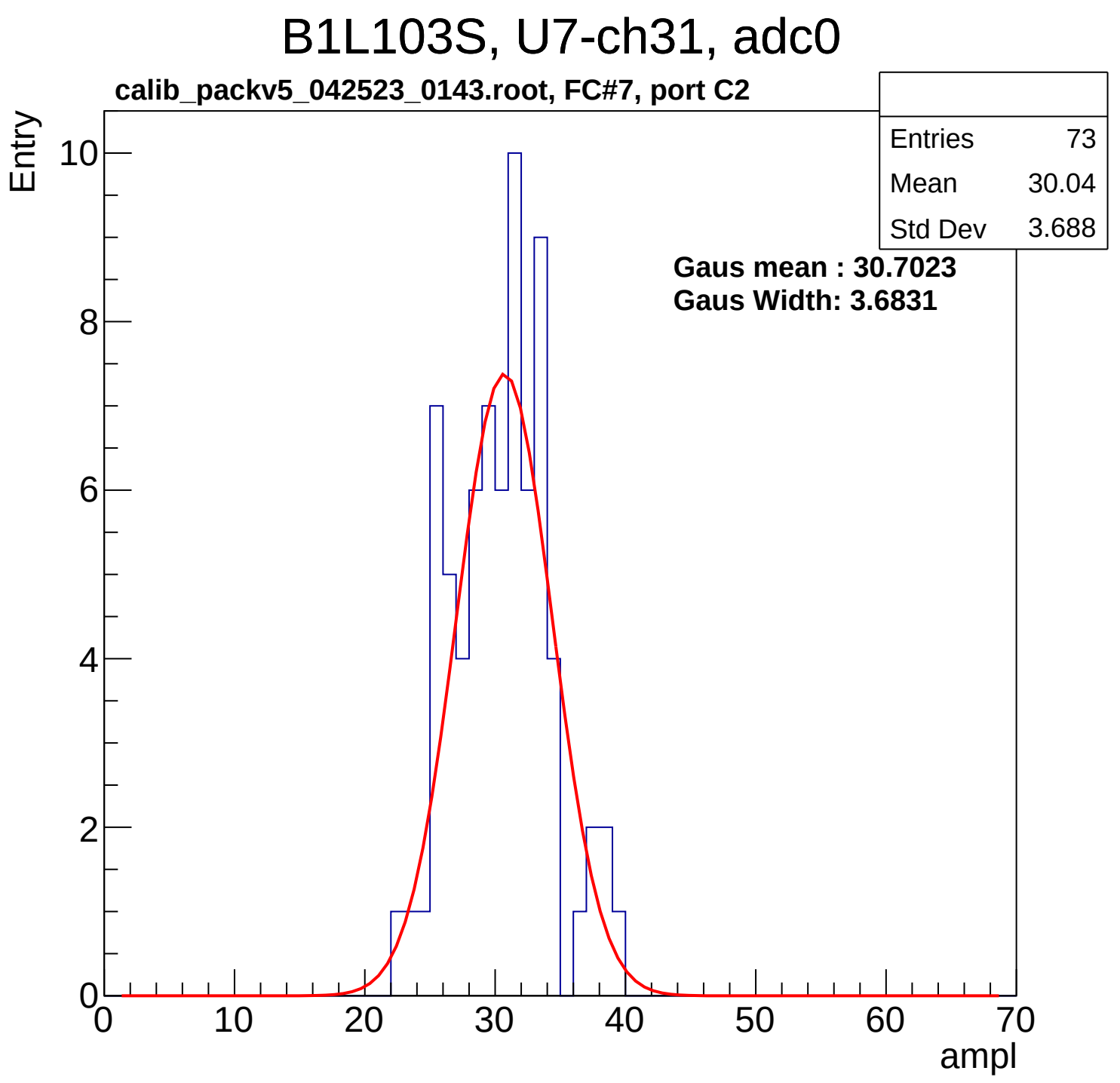

B1L103S, U7-ch30, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 73
Mean 48.18
Std Dev 3.758
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

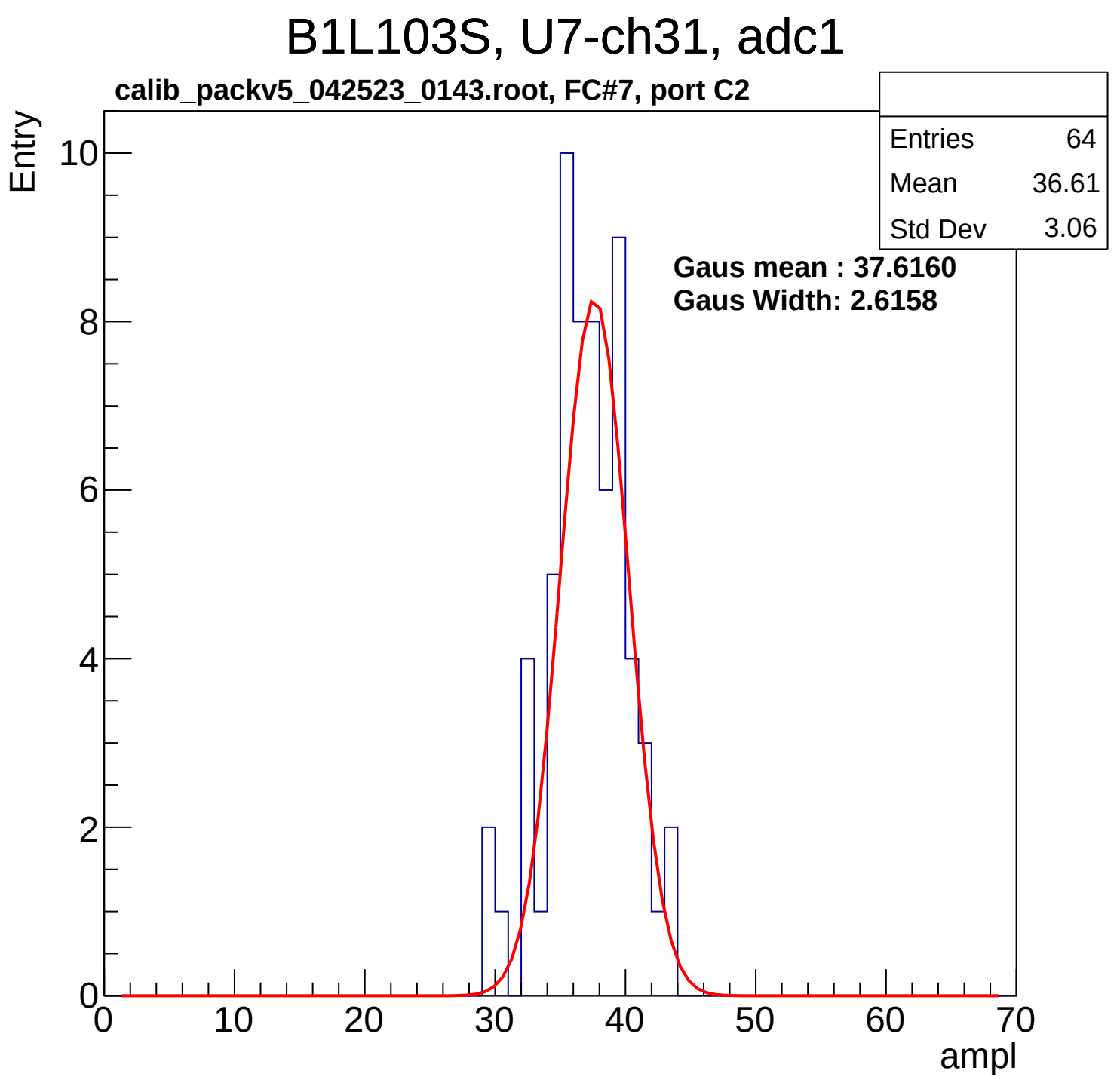

B1L103S, U7-ch30, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 51
Mean 53.69
Std Dev 3.09
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

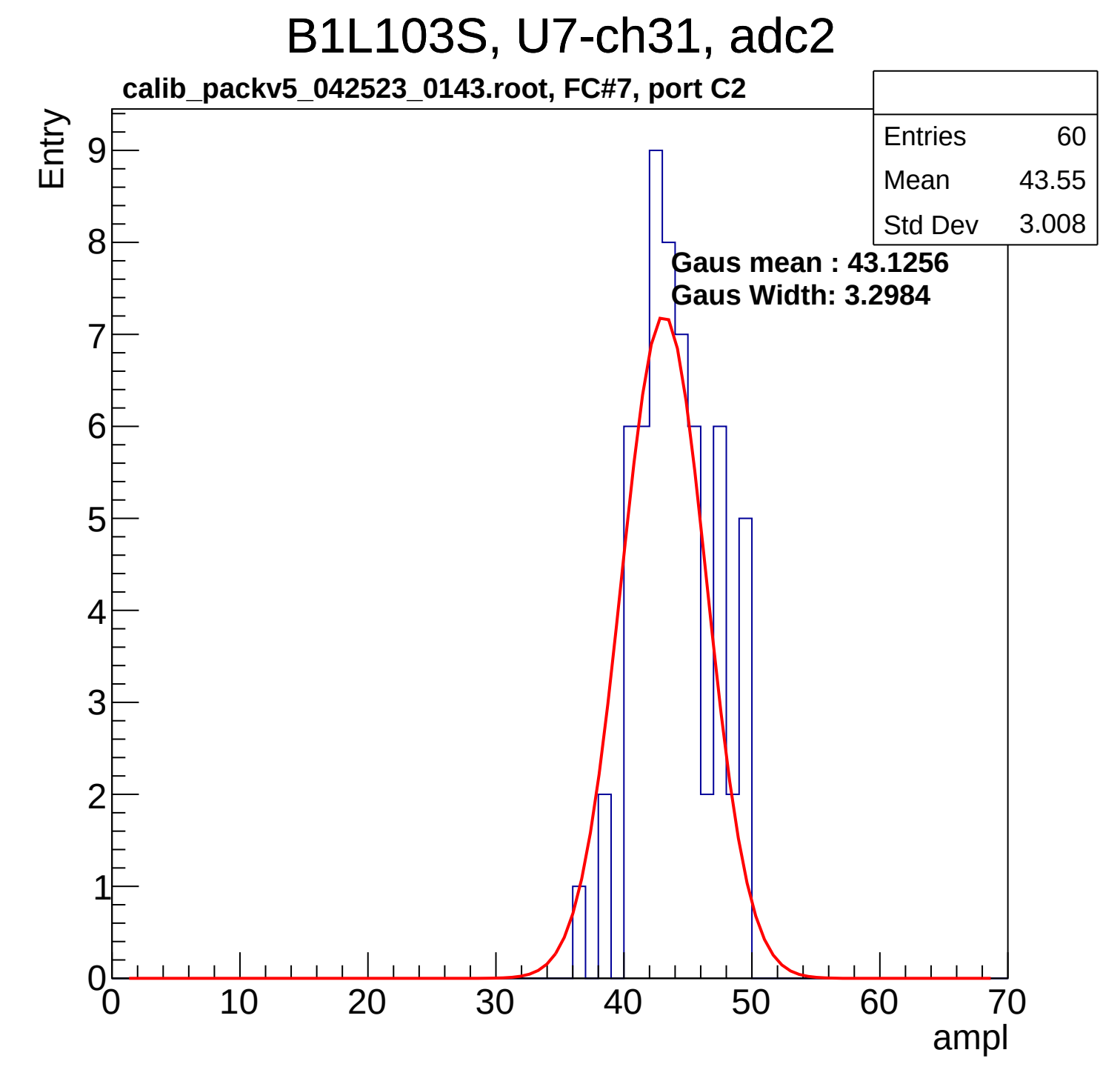

B1L103S, U7-ch30, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 49
Mean 58.94
Std Dev 2.307
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

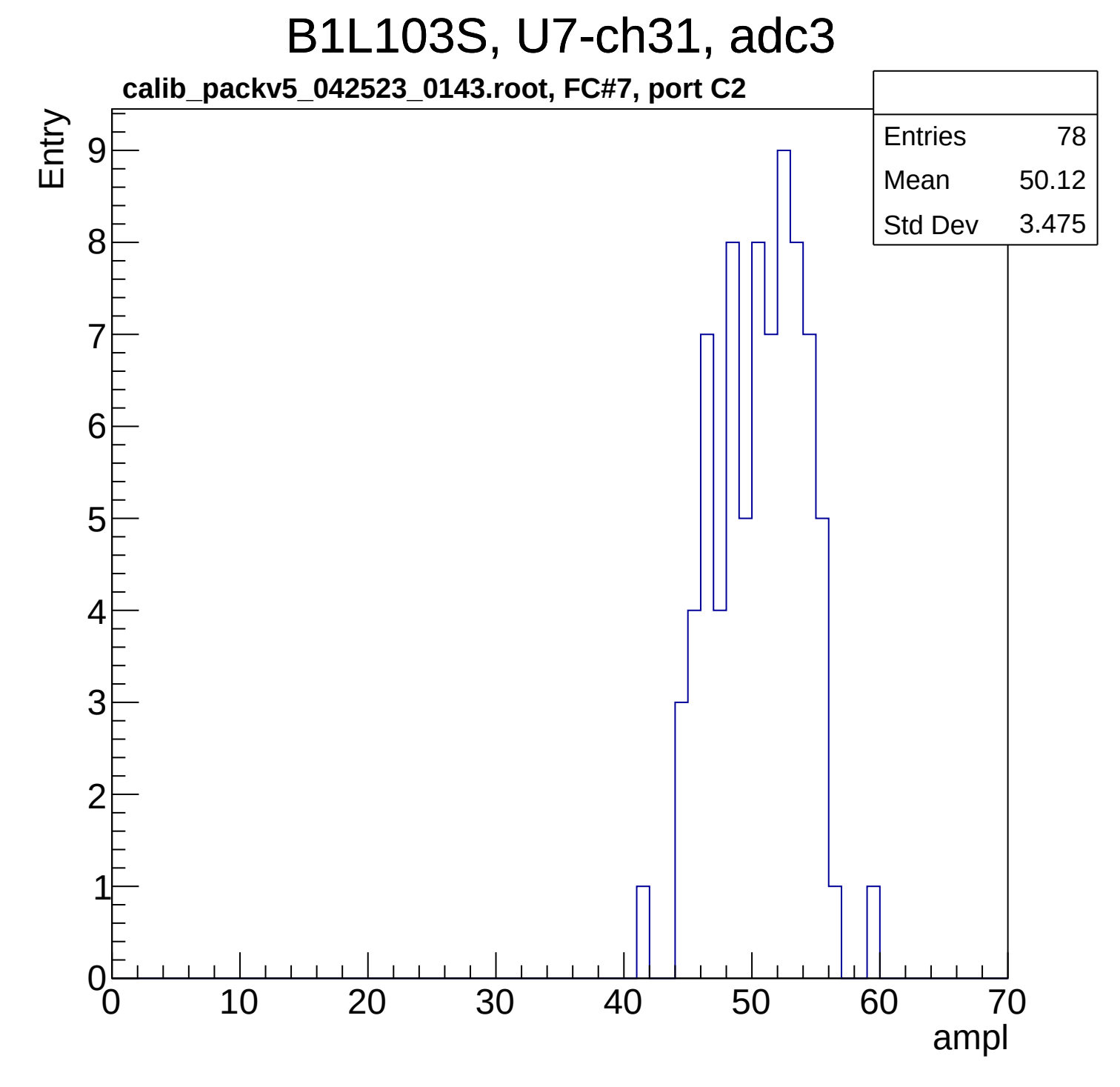

B1L103S, U7-ch30, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 18
Mean 58.61
Std Dev 14.25
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

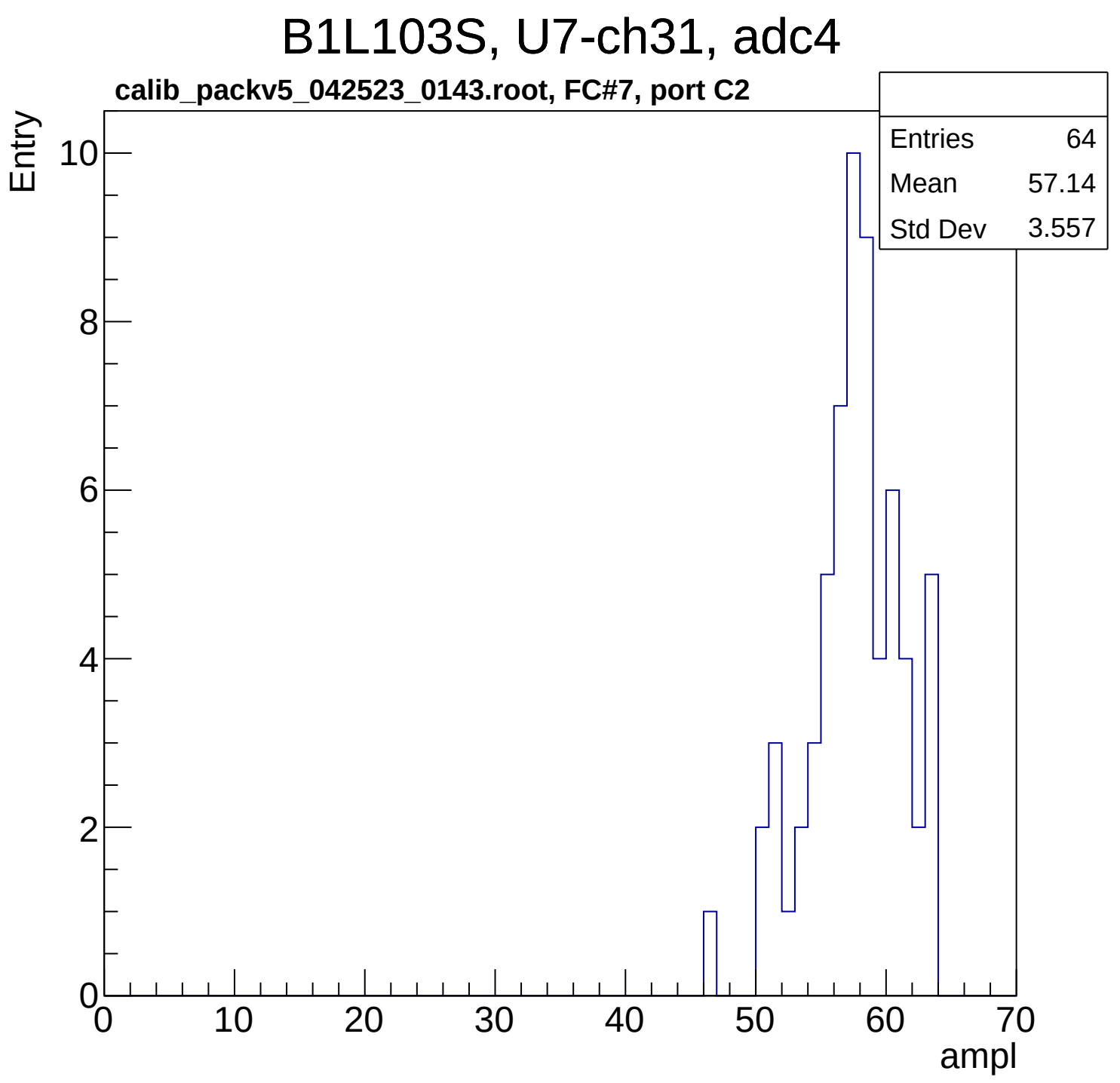

B1L103S, U7-ch30, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 61
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

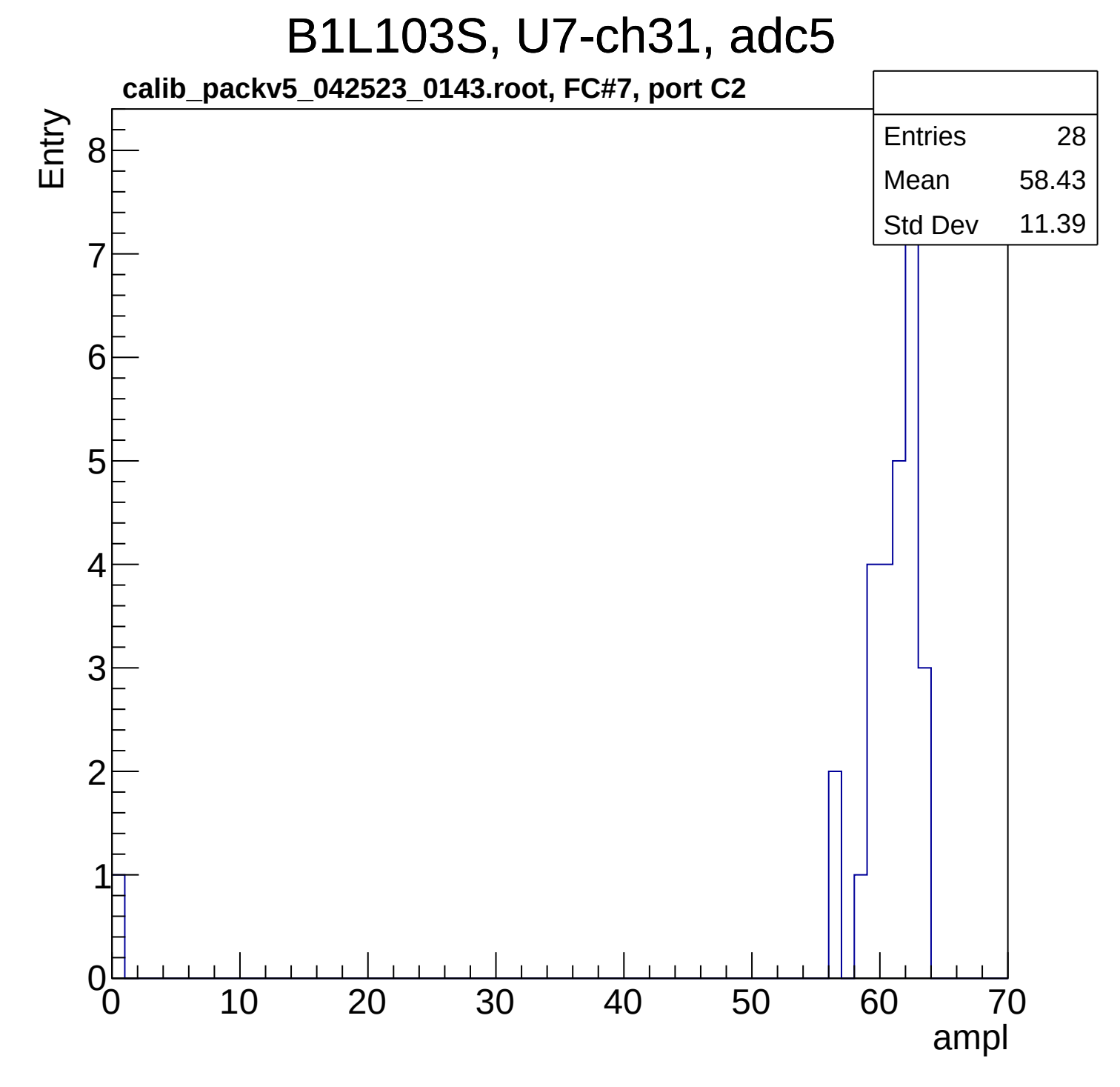

B1L103S, U7-ch31, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 73
Mean 30.04
Std Dev 3.688
Gaus mean : 30.7023
Gaus Width: 3.6831
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

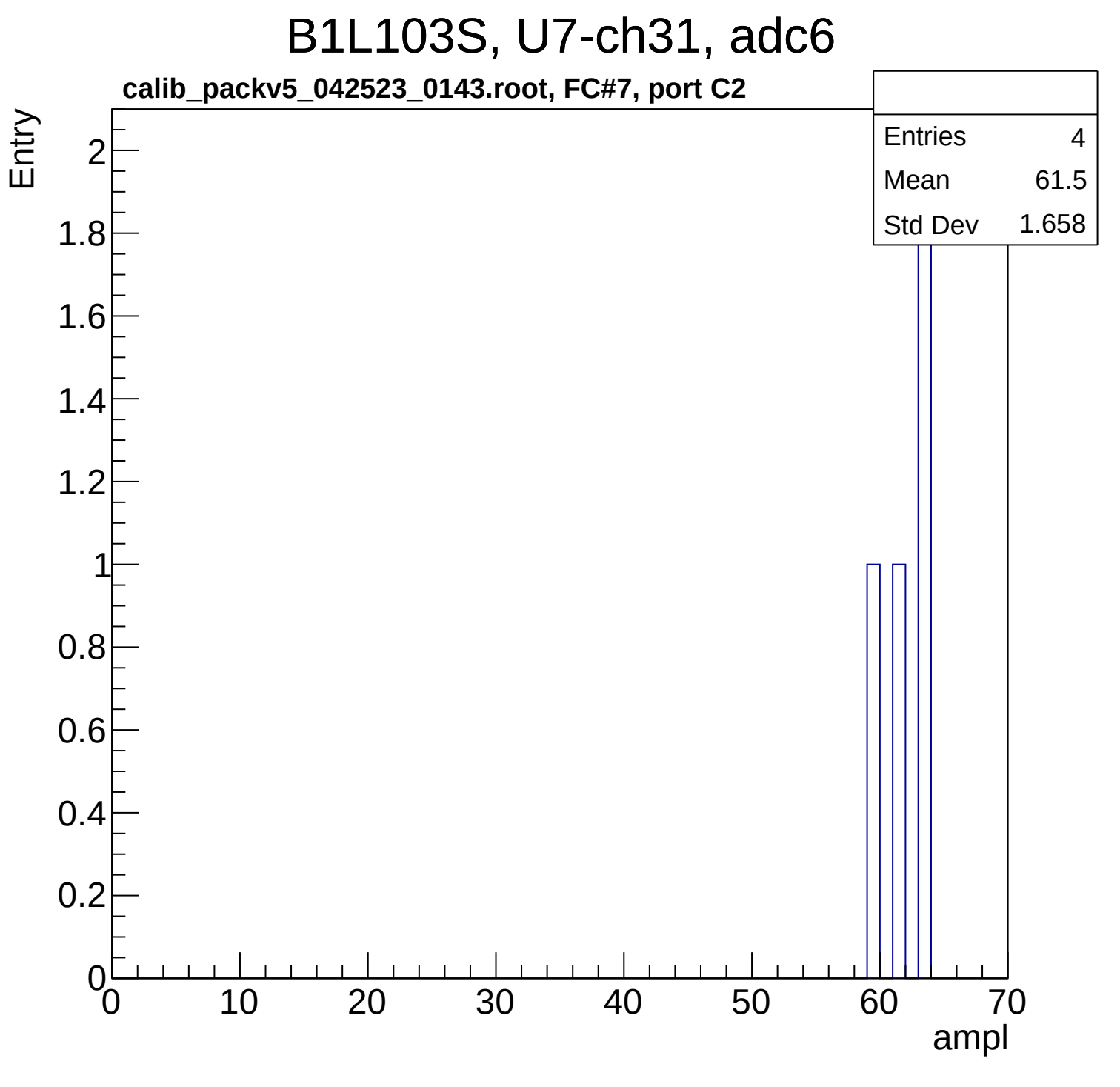

B1L103S, U7-ch31, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 36.61
Std Dev 3.06
Gaus mean : 37.6160
Gaus Width: 2.6158
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

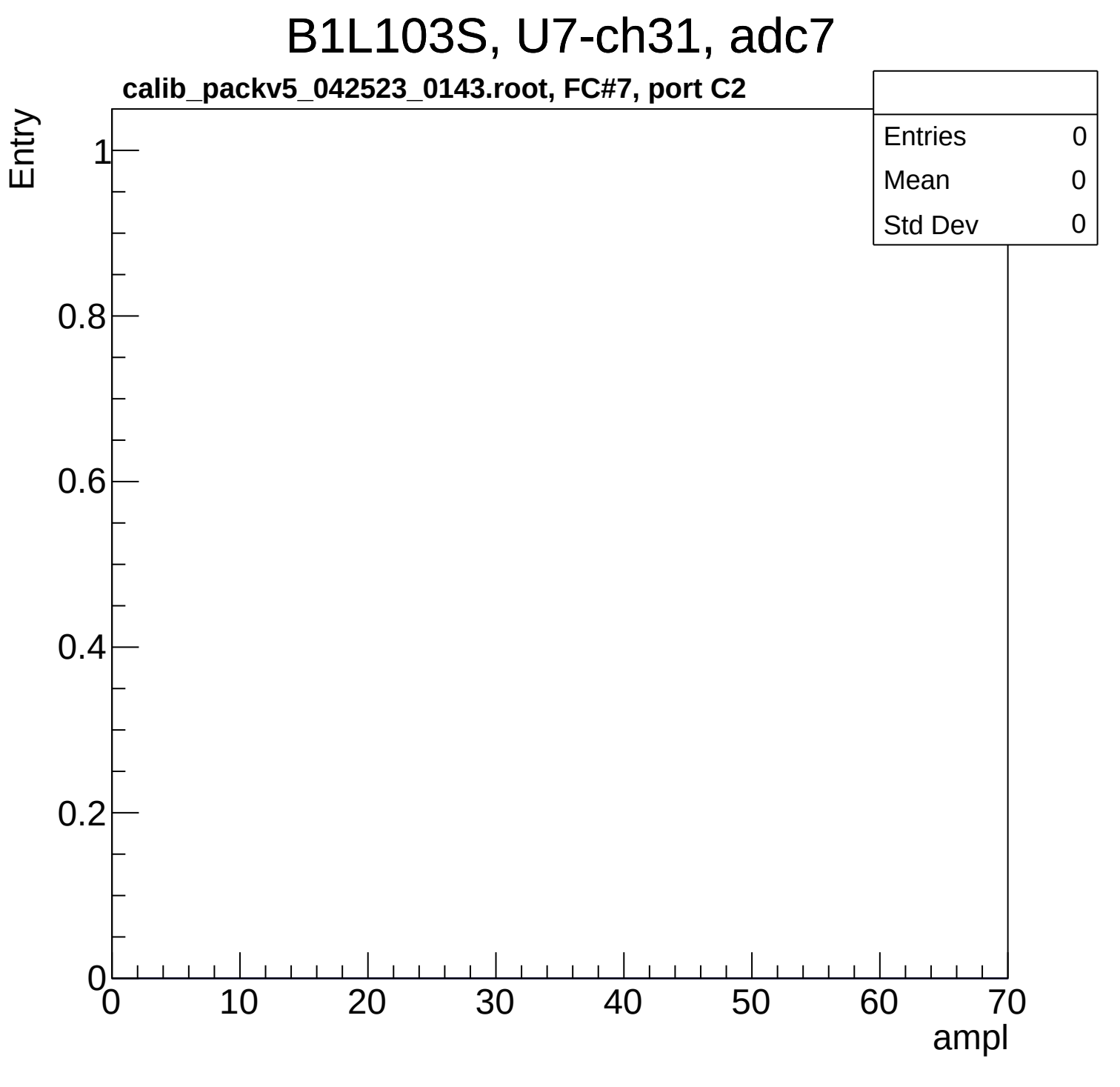

B1L103S, U7-ch31, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 60
Mean 43.55
Std Dev 3.008
Gaus mean : 43.1256
Gaus Width: 3.2984
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

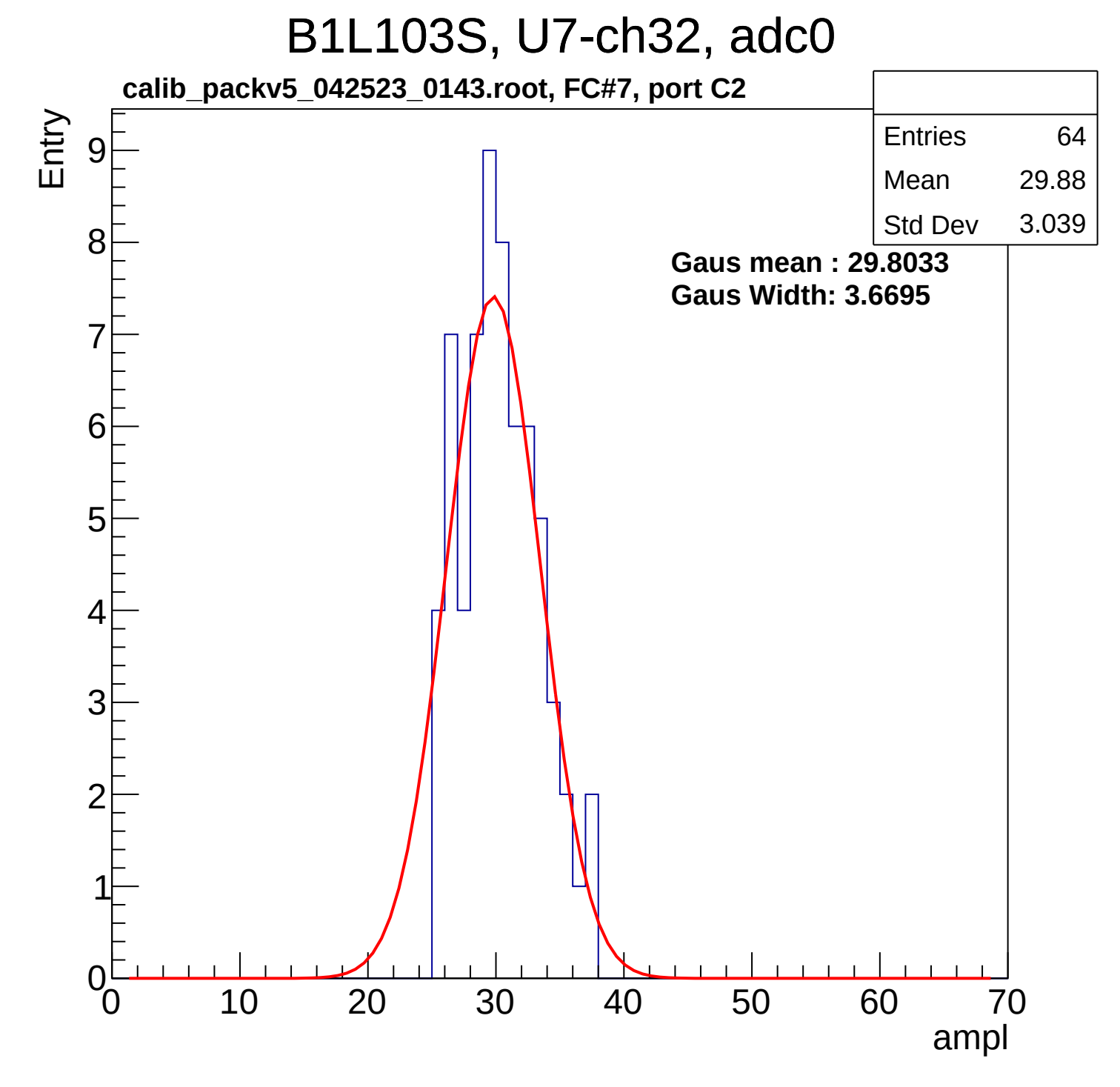

B1L103S, U7-ch31, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 78
Mean 50.12
Std Dev 3.475
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

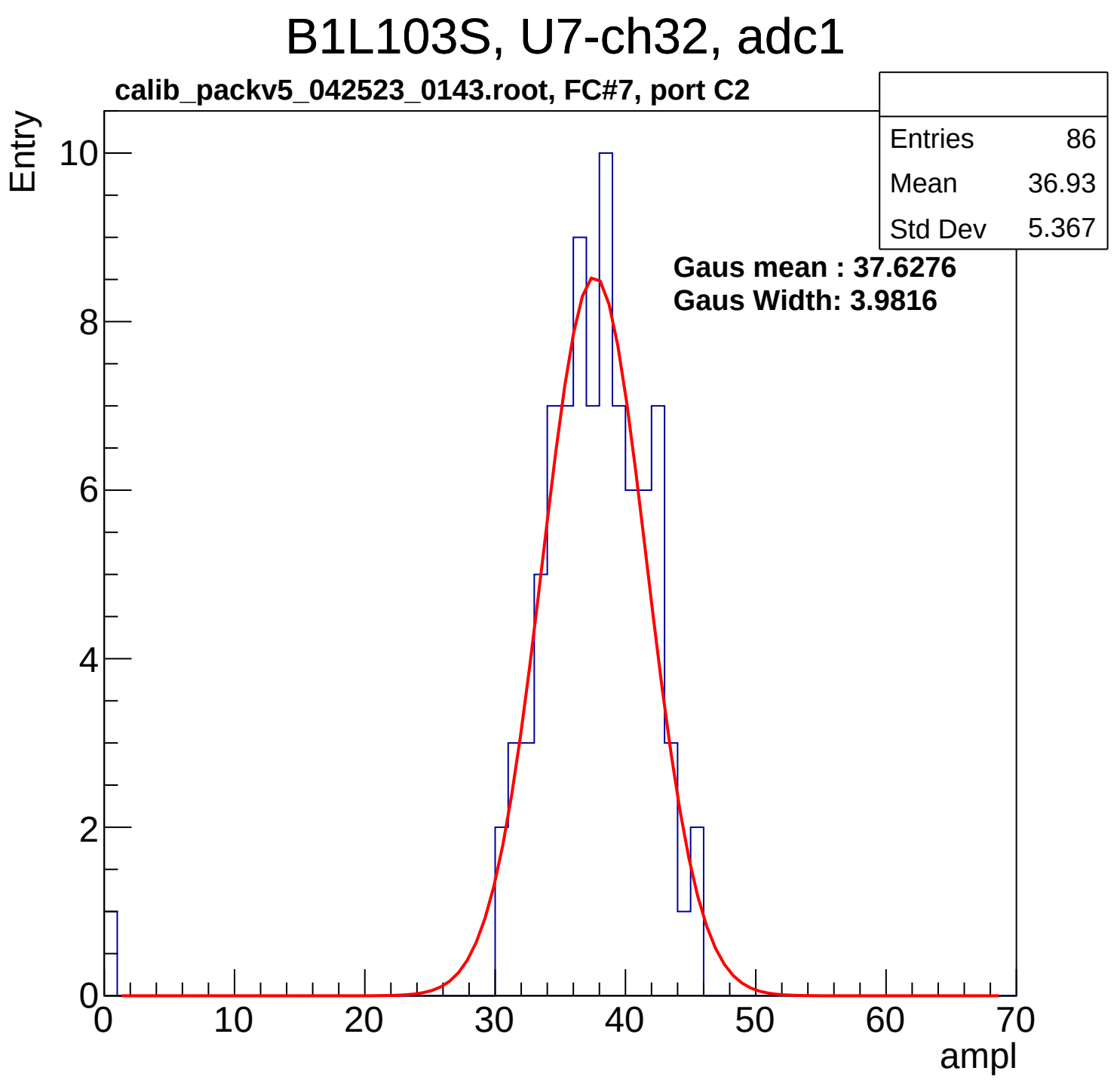

B1L103S, U7-ch31, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 57.14
Std Dev 3.557
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

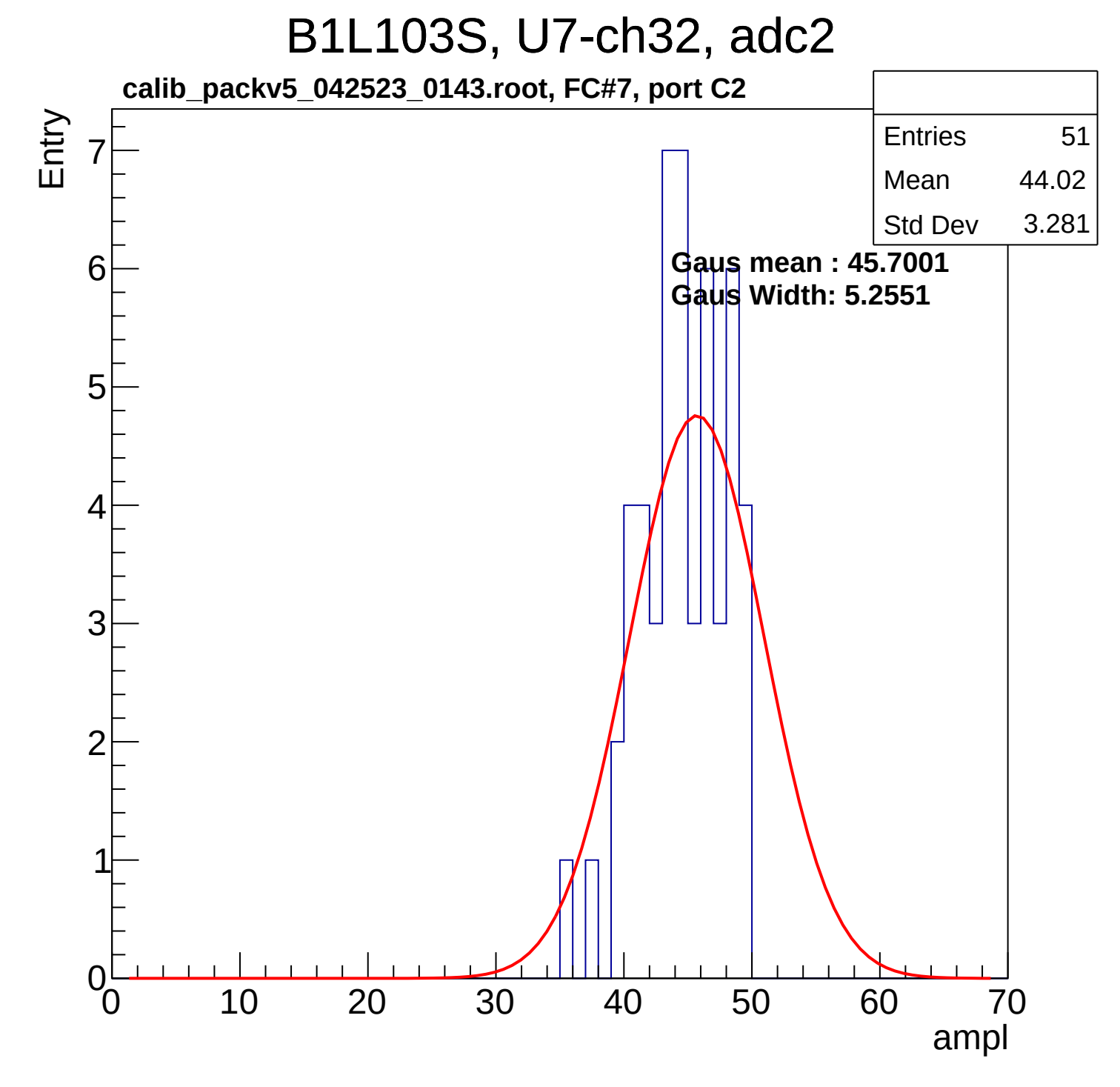

B1L103S, U7-ch31, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 28
Mean 58.43
Std Dev 11.39
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

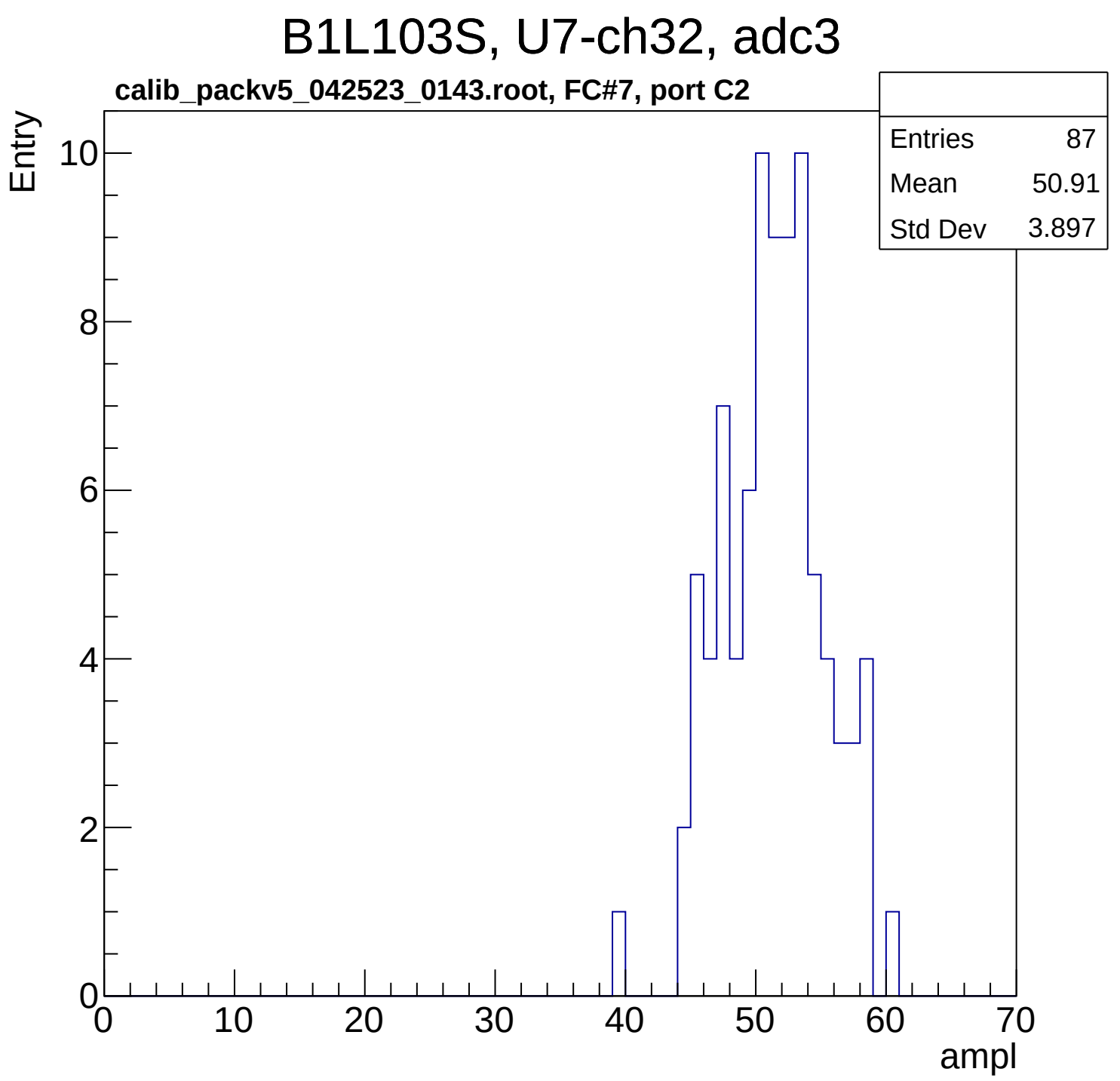

B1L103S, U7-ch31, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 4
Mean 61.5
Std Dev 1.658
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

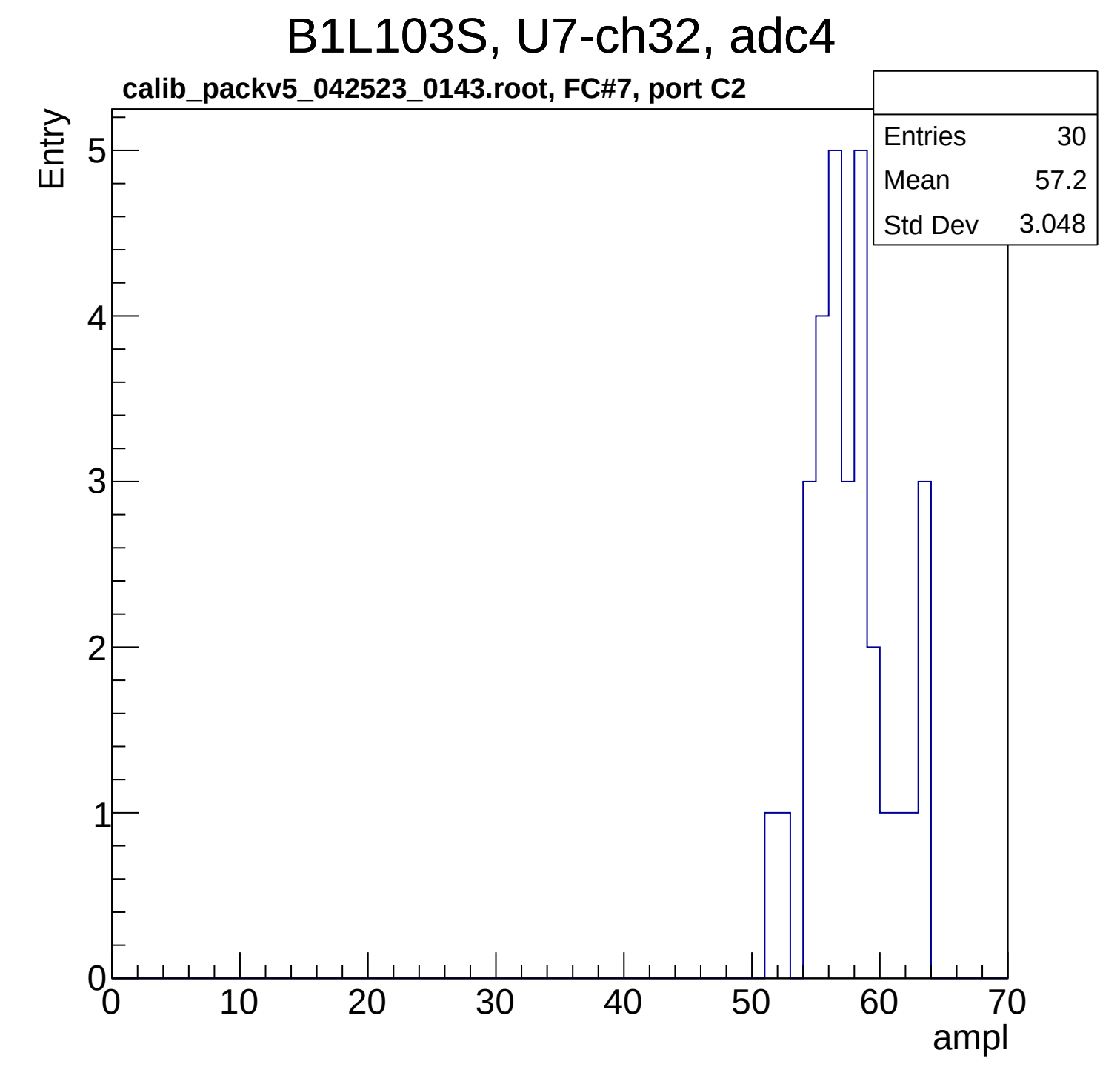

B1L103S, U7-ch31, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

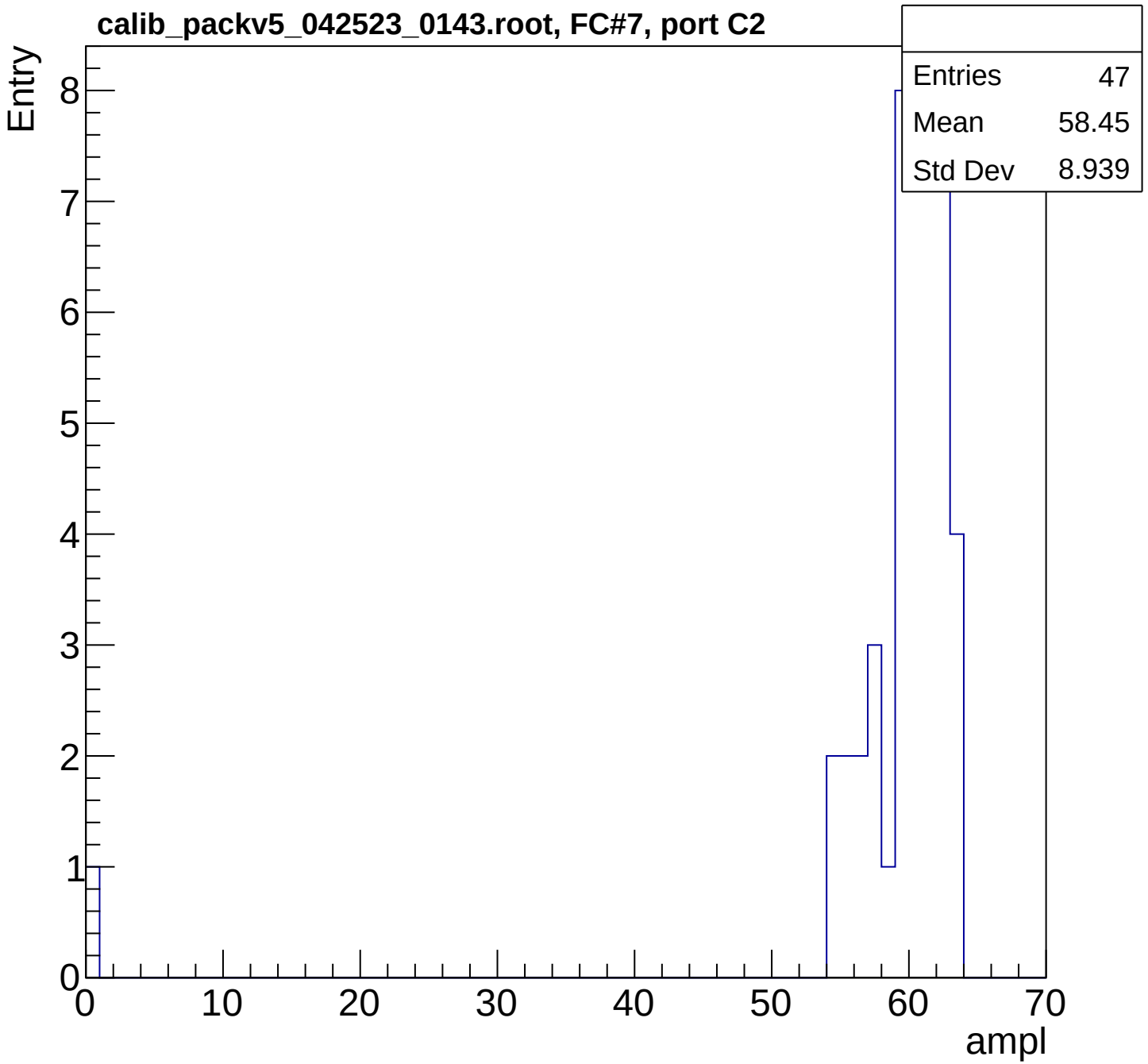

B1L103S, U7-ch32, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 29.88
Std Dev 3.039
Gaus mean : 29.8033
Gaus Width: 3.6695
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch32, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 86
Mean 36.93
Std Dev 5.367
Gaus mean : 37.6276
Gaus Width: 3.9816
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch32, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 51
Mean 44.02
Std Dev 3.281
Gaus mean : 45.7001
Gaus Width: 5.2551
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch32, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 87
Mean 50.91
Std Dev 3.897
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch32, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 30
Mean 57.2
Std Dev 3.048
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch32, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 47
Mean 58.45
Std Dev 8.939
Entry
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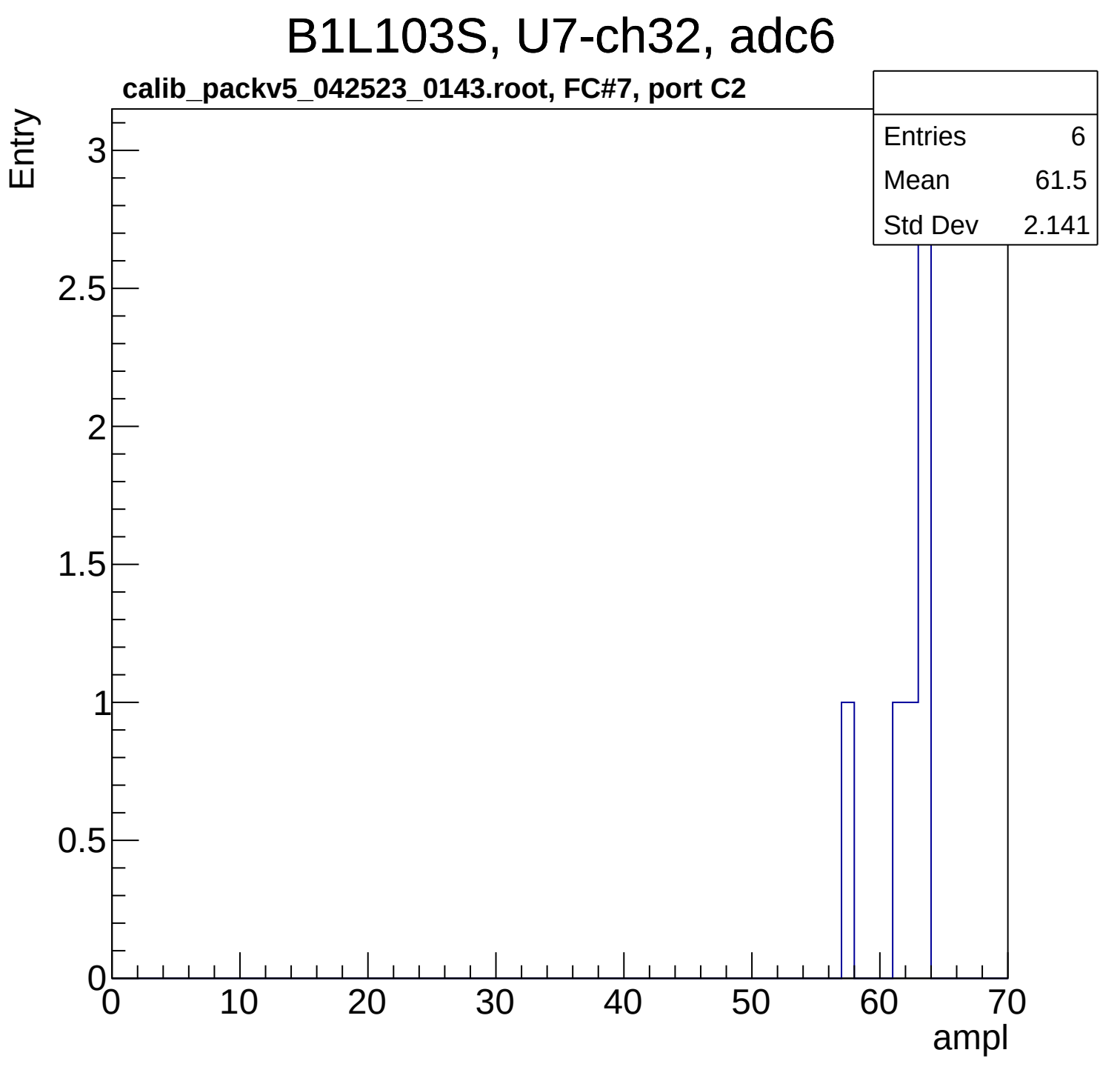
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch32, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 6
Mean 61.5
Std Dev 2.141
Entry
ampl
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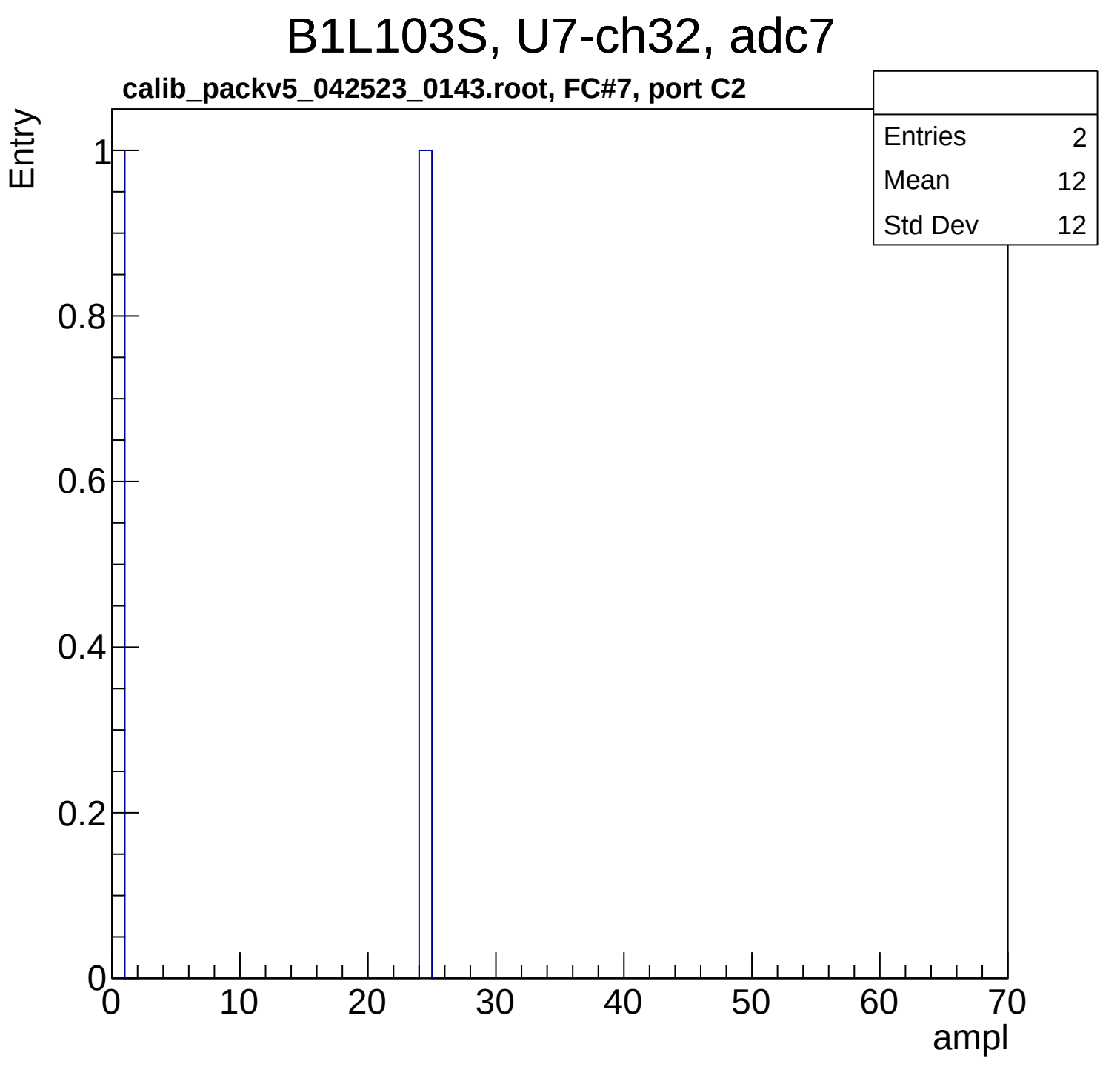
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U7-ch32, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 12
Std Dev 12
Entry
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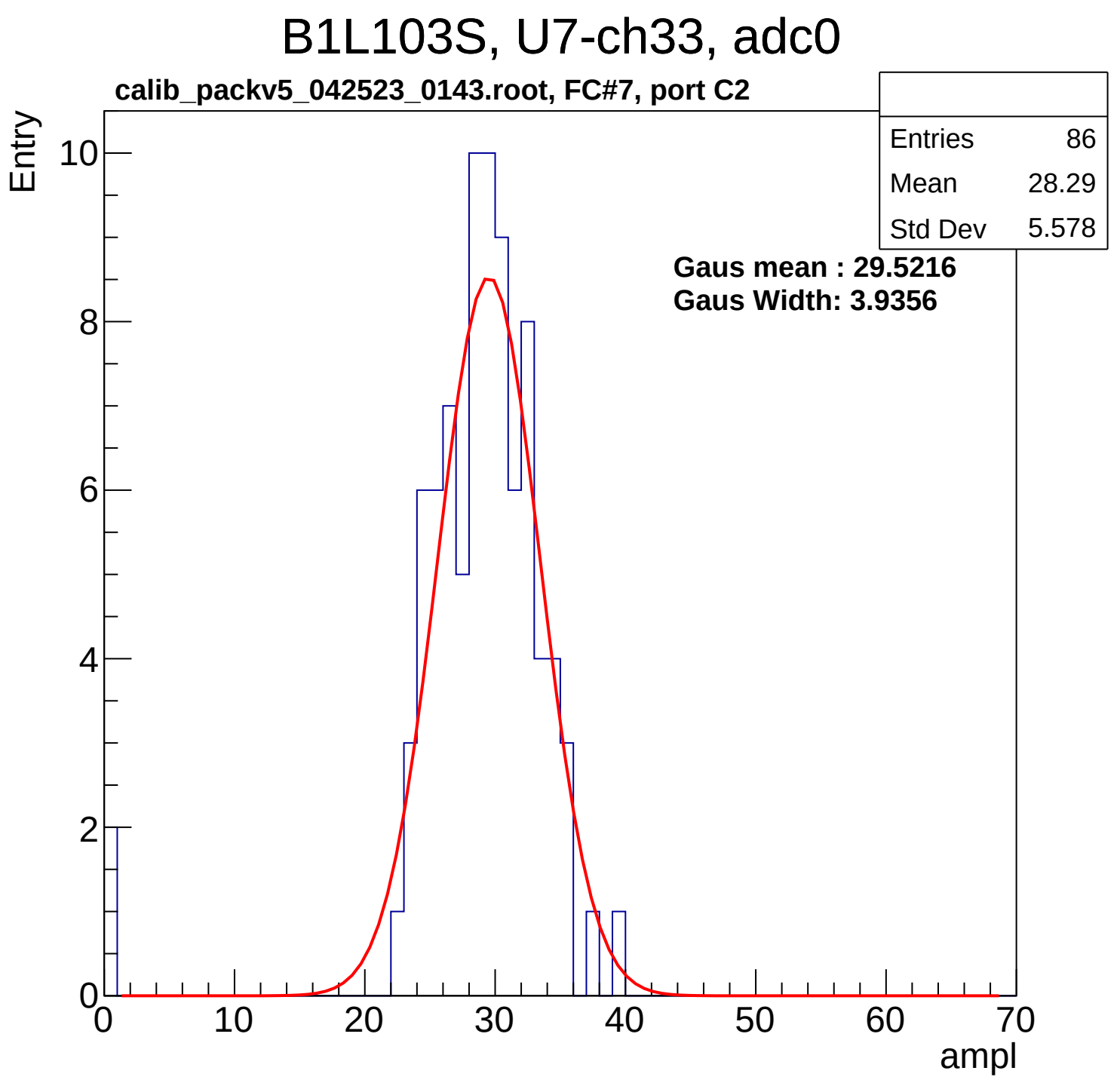
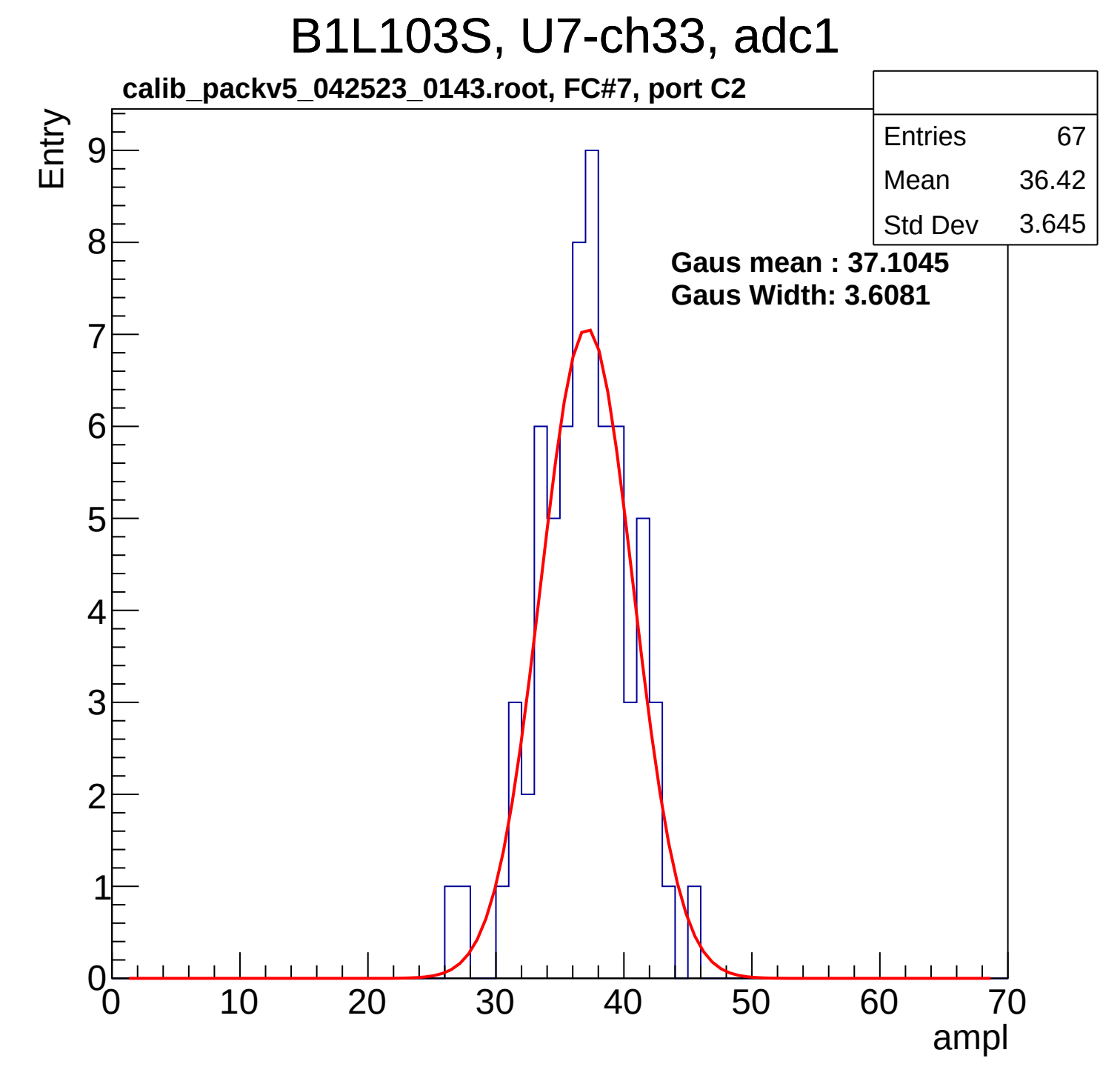
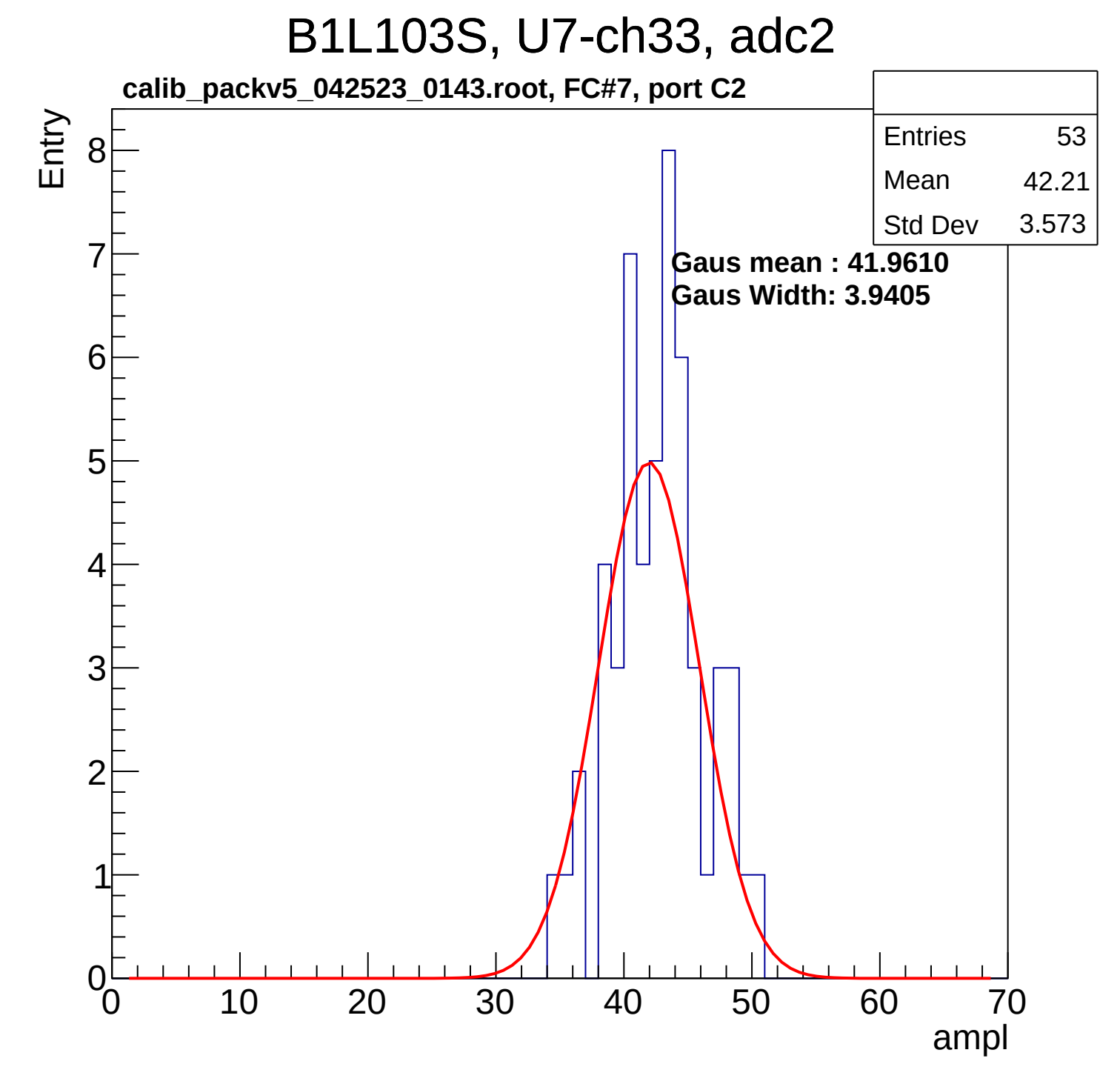
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch33, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 86
Mean 28.29
Std Dev 5.578
Gaus mean : 29.5216
Gaus Width: 3.9356
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch33, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 36.42
Std Dev 3.645
Gaus mean : 37.1045
Gaus Width: 3.6081
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch33, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 42.21
Std Dev 3.573
Gaus mean : 41.9610
Gaus Width: 3.9405
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
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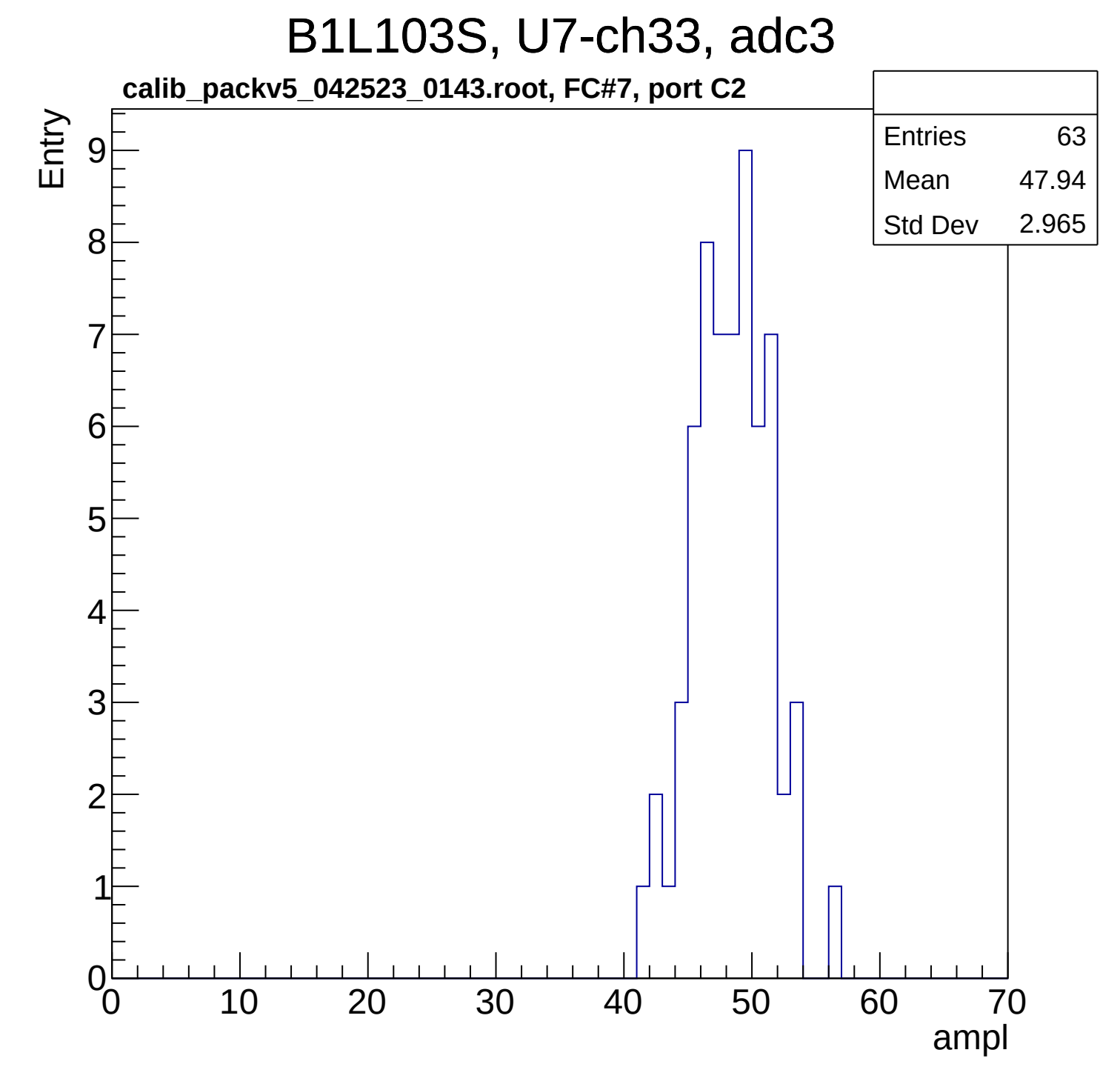
60
70


B1L103S, U7-ch33, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 47.94
Std Dev 2.965
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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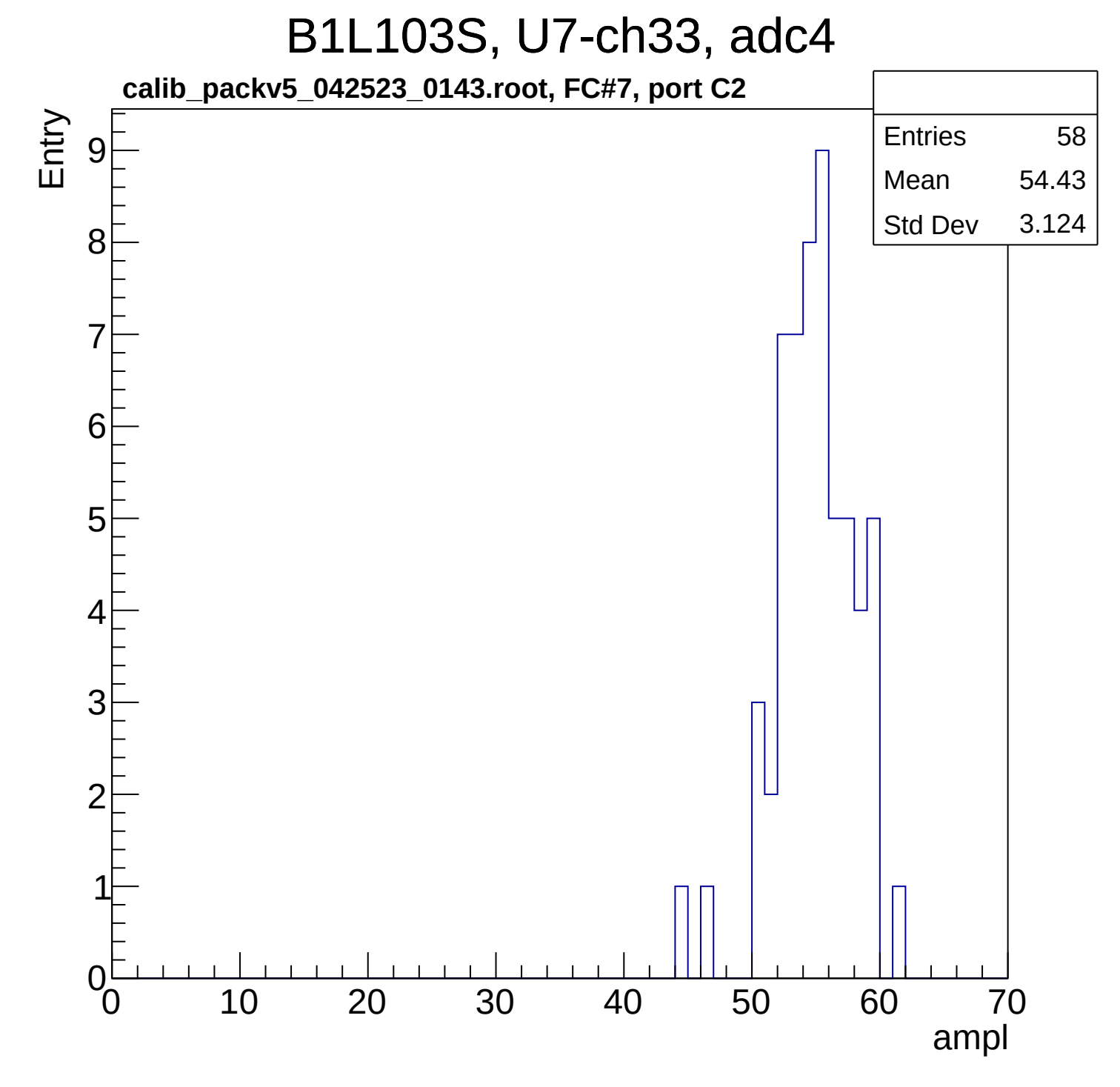
40
50
60
70


B1L103S, U7-ch33, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 58
Mean 54.43
Std Dev 3.124
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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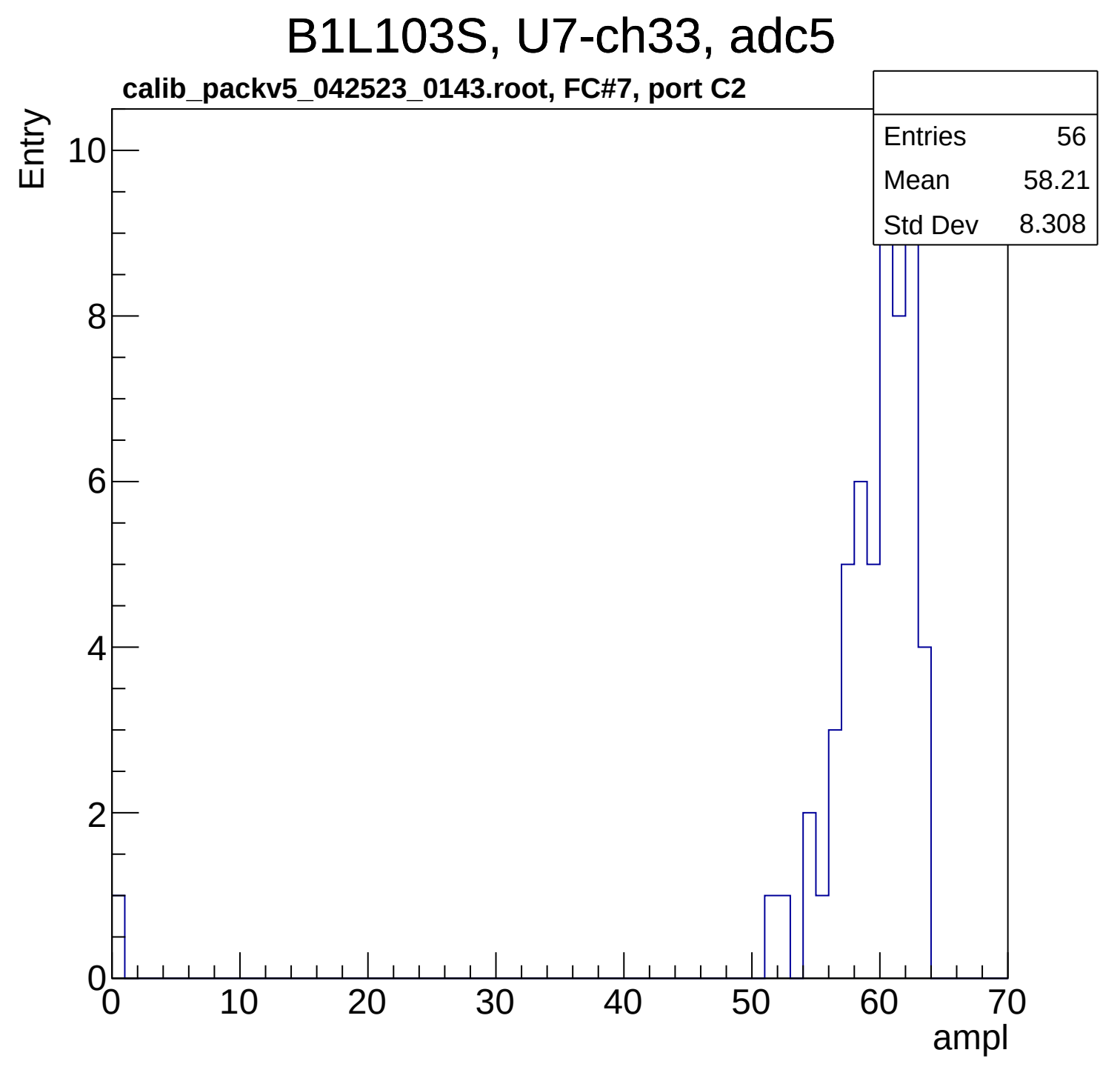
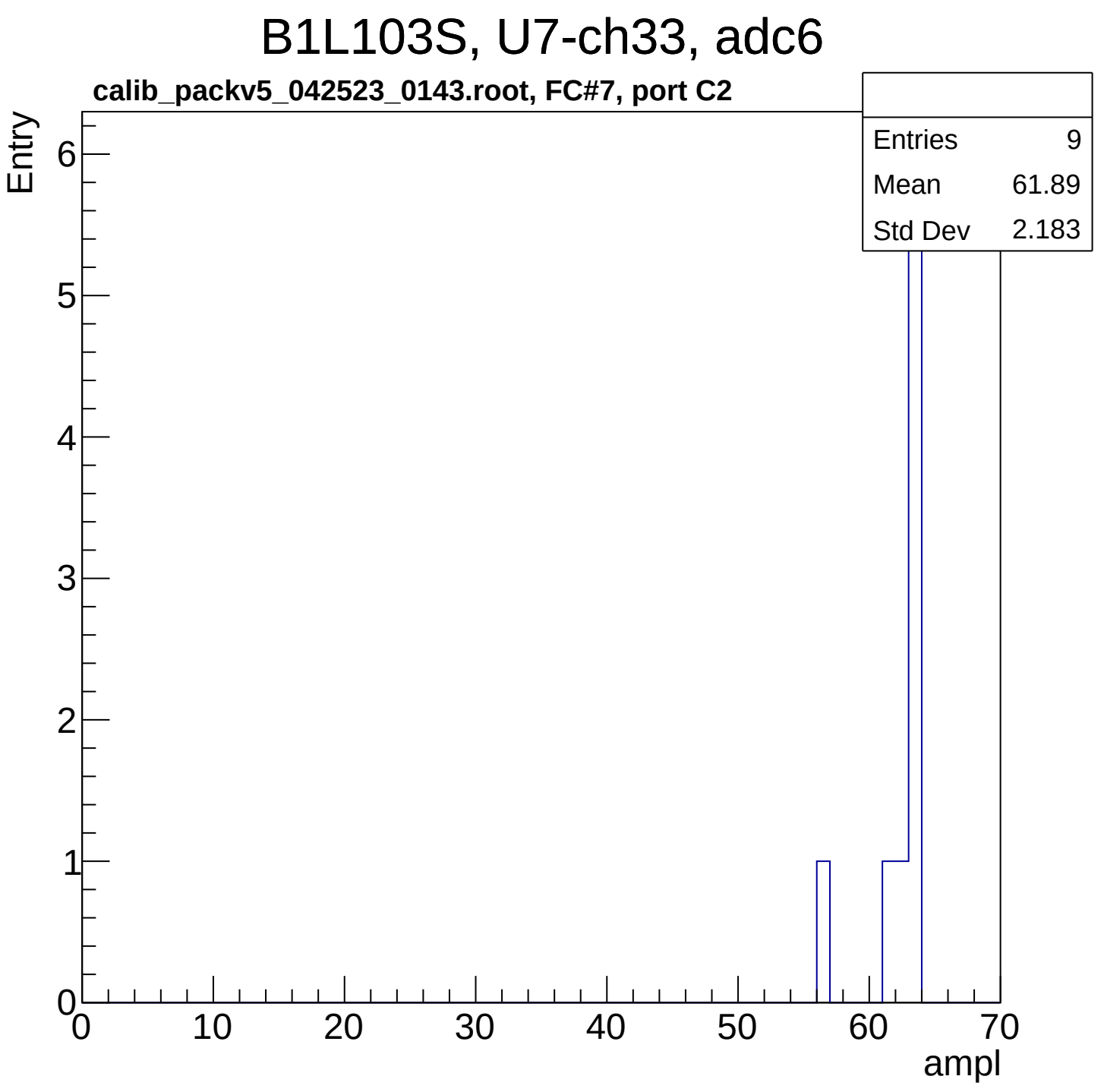
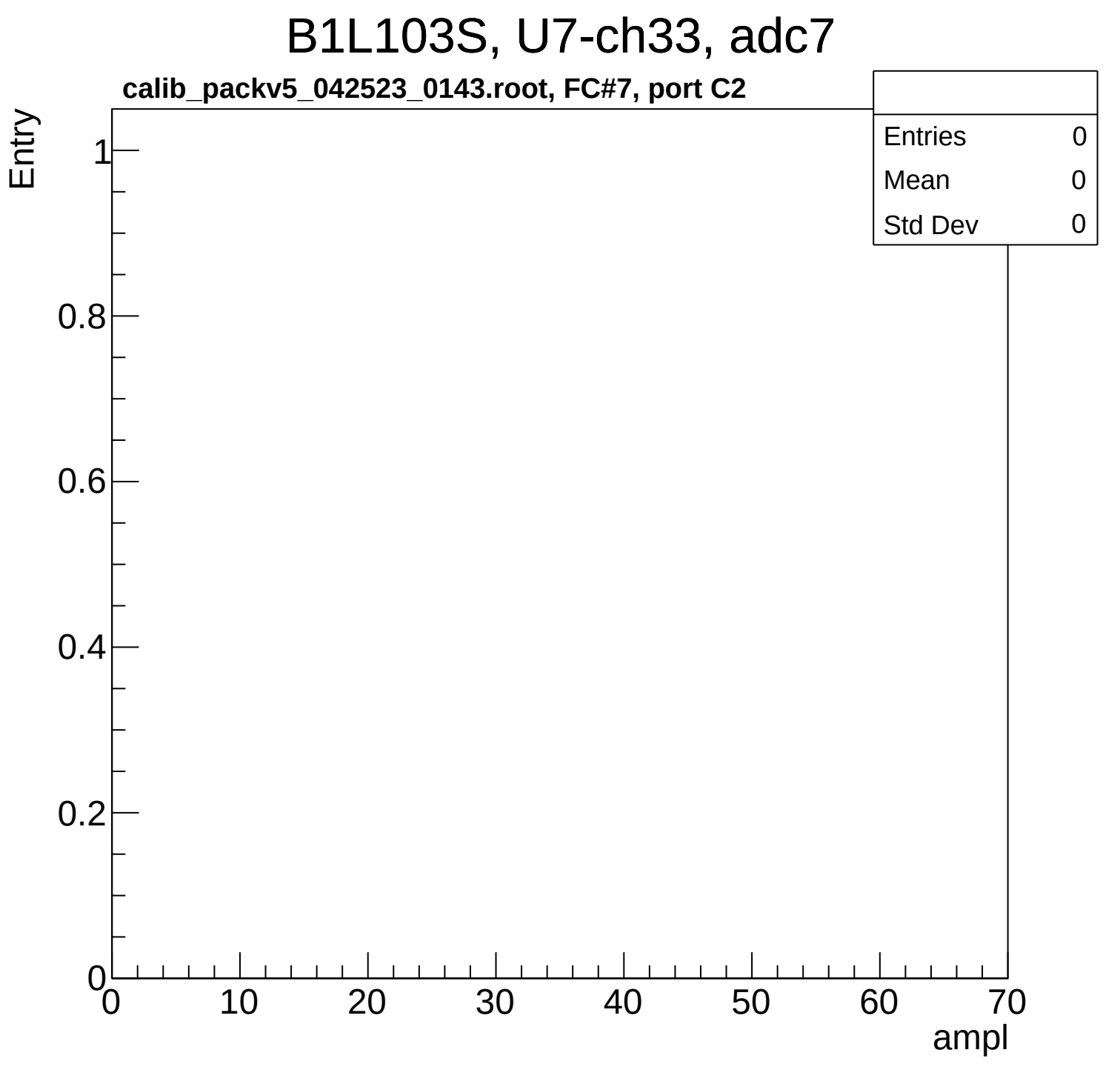

B1L103S, U7-ch33, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 58.21
Std Dev 8.308
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch33, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 9
Mean 61.89
Std Dev 2.183
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U7-ch33, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
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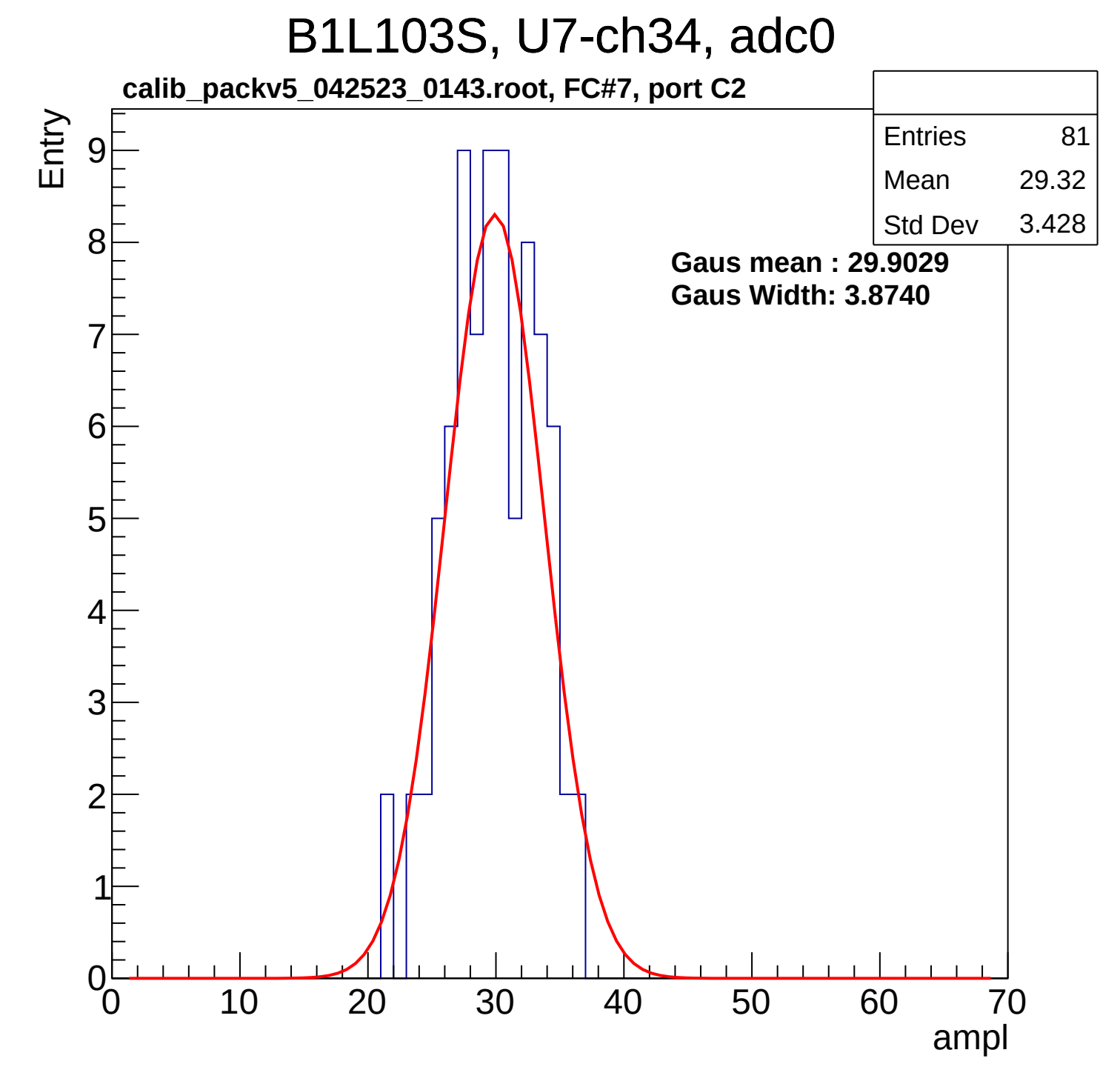
30
40
50
60
70
ampl


B1L103S, U7-ch34, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 81
Mean 29.32
Std Dev 3.428
Gaus mean : 29.9029
Gaus Width: 3.8740
Entry
ampl
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2
3
4
5
6
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8
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0
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40
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60
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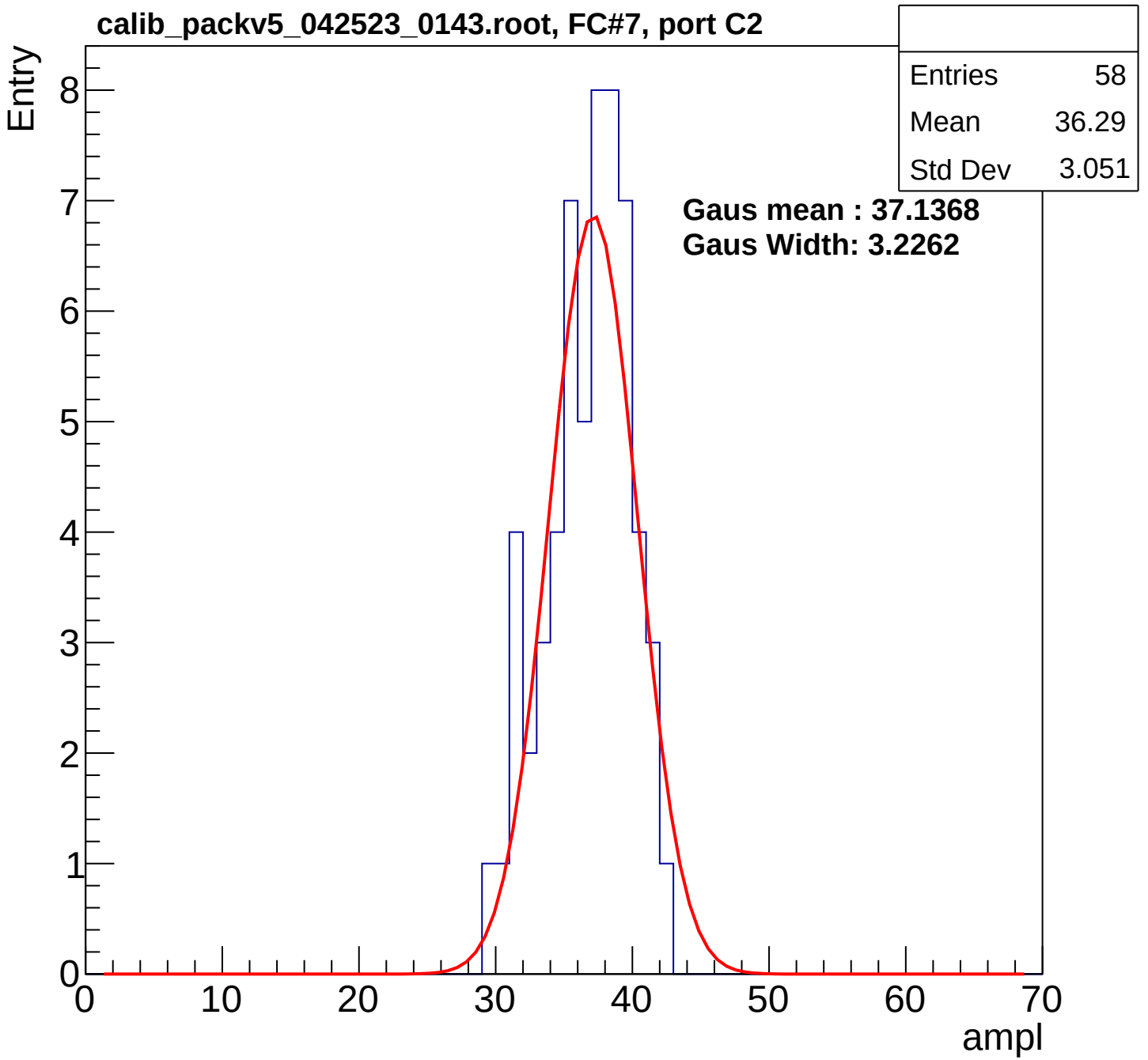
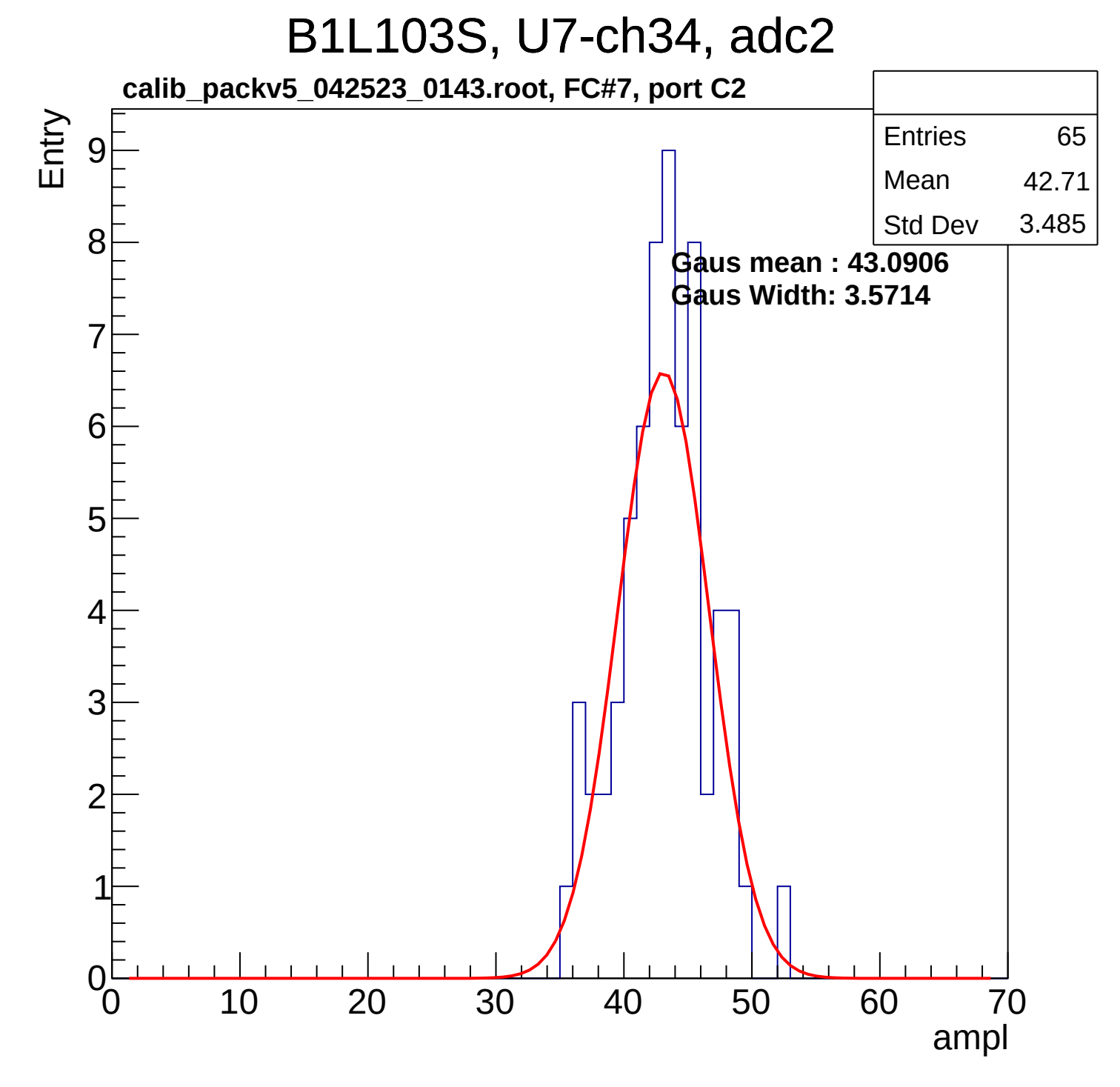

B1L103S, U7-ch34, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 58
Mean 36.29
Std Dev 3.051
Gaus mean : 37.1368
Gaus Width: 3.2262
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch34, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 42.71
Std Dev 3.485
Gaus mean : 43.0906
Gaus Width: 3.5714
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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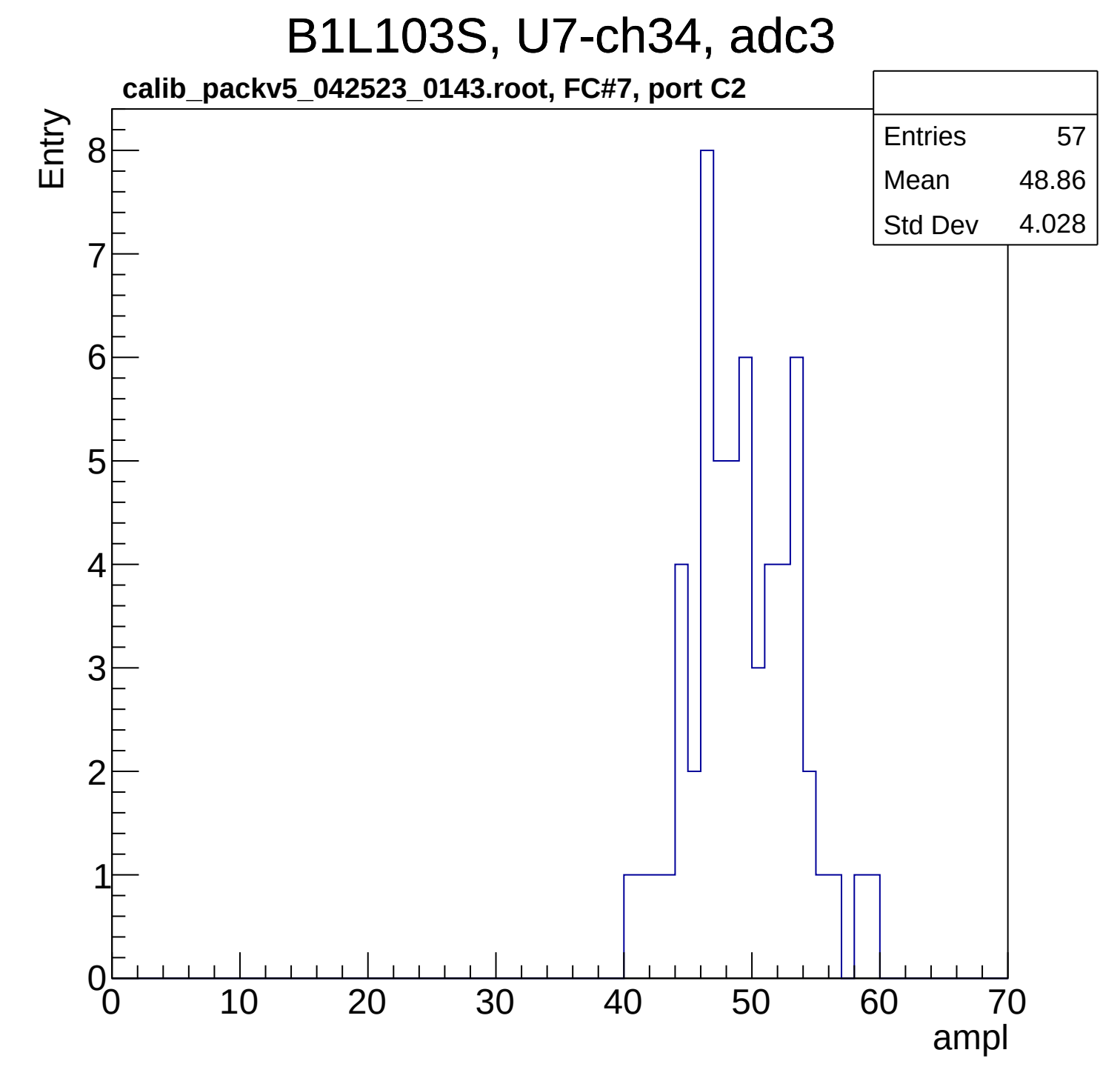
60
70


B1L103S, U7-ch34, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 48.86
Std Dev 4.028
Entry
ampl
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2
3
4
5
6
7
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0
10
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40
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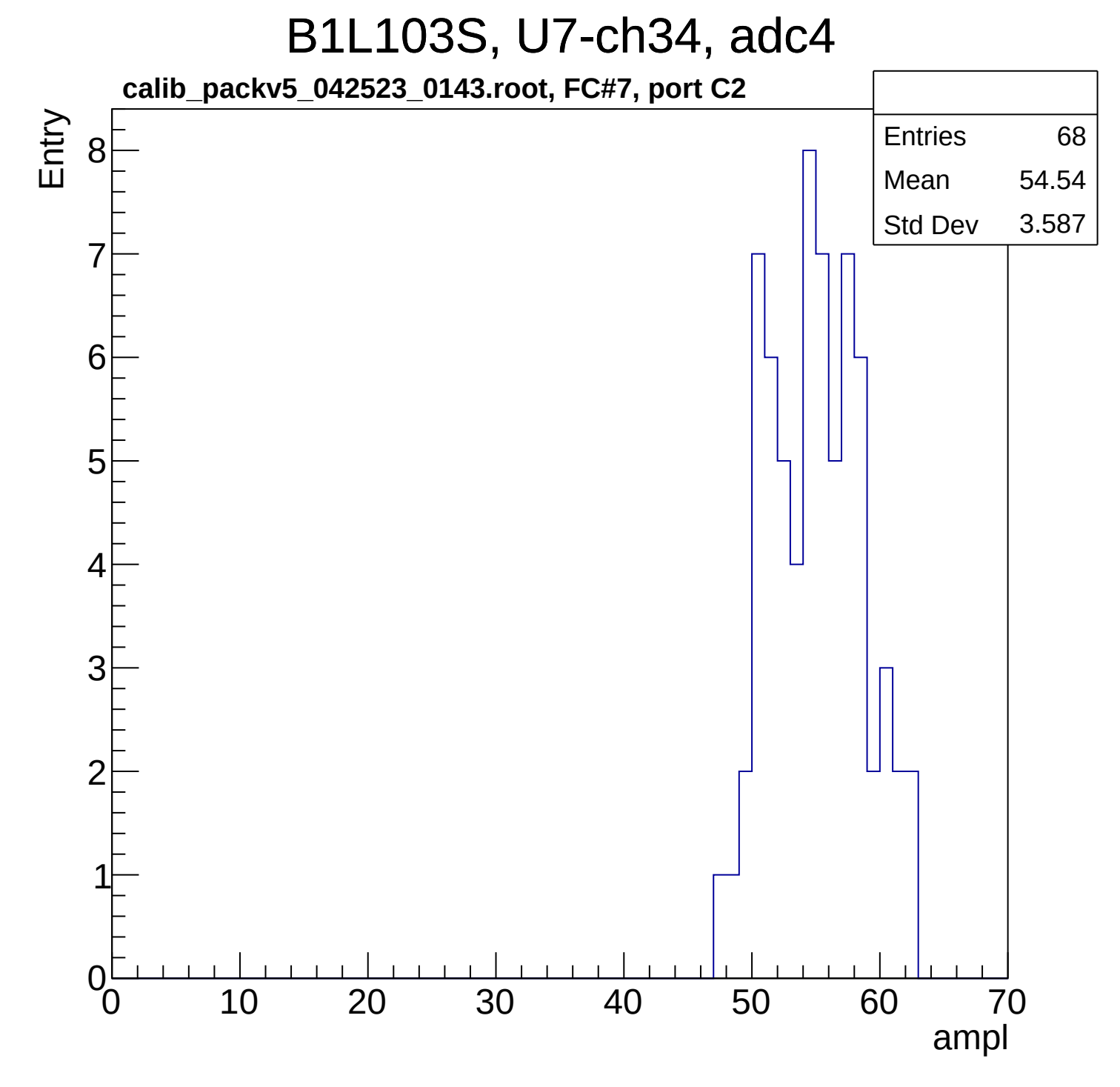
60
70


B1L103S, U7-ch34, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 54.54
Std Dev 3.587
Entry
0
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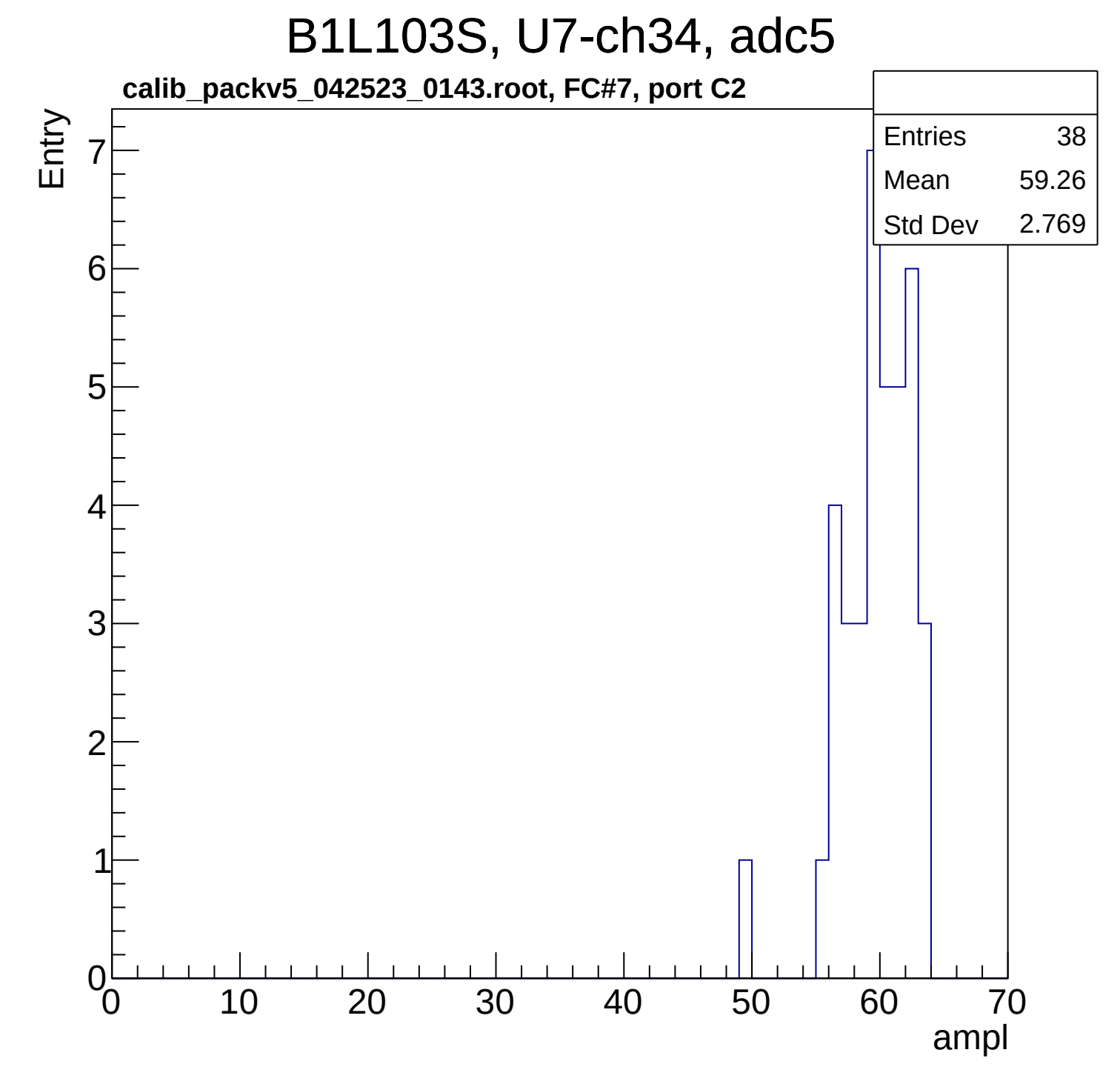
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch34, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 38
Mean 59.26
Std Dev 2.769
Entry
ampl
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6
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0
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20
30
40
50
60
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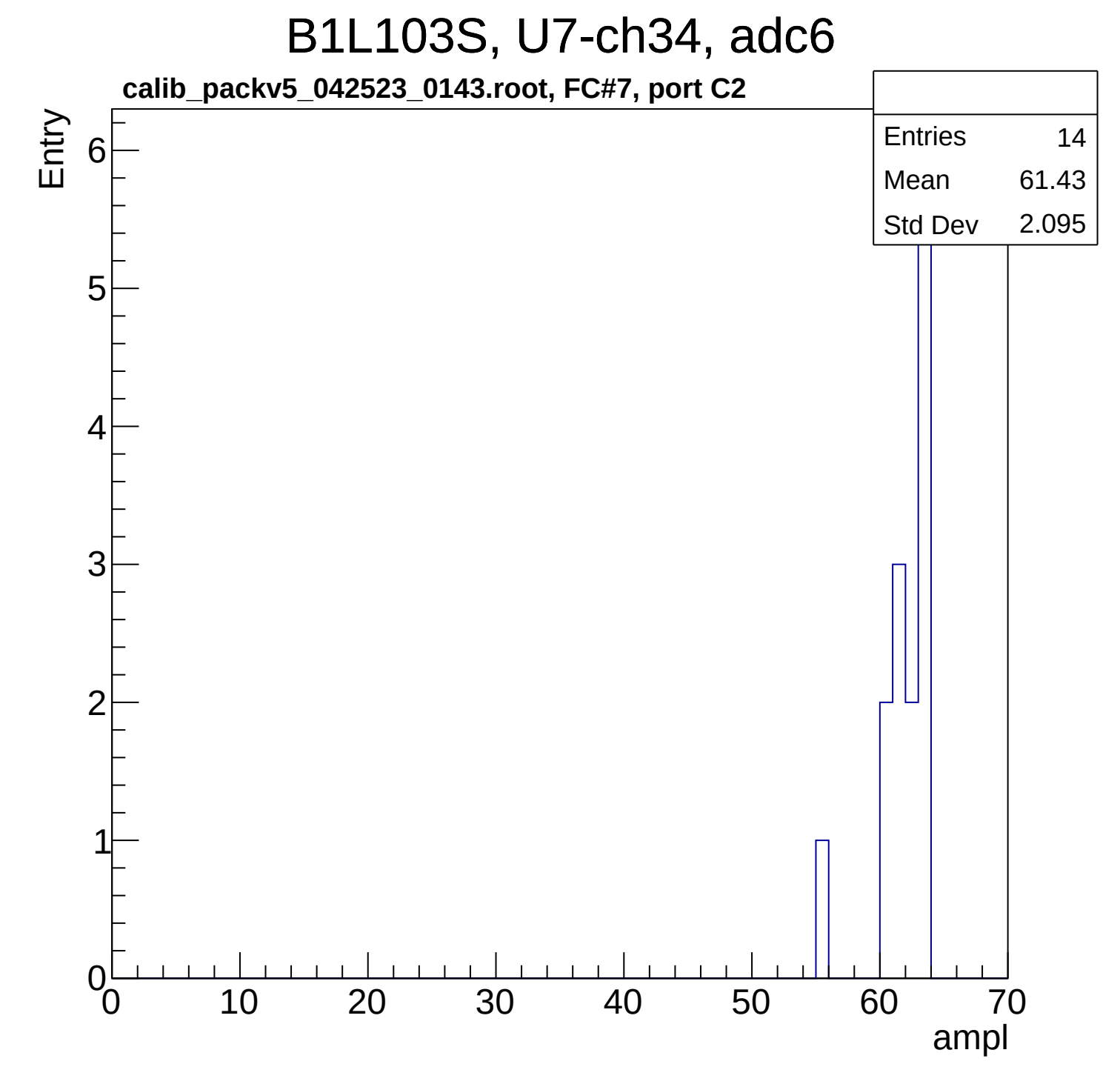
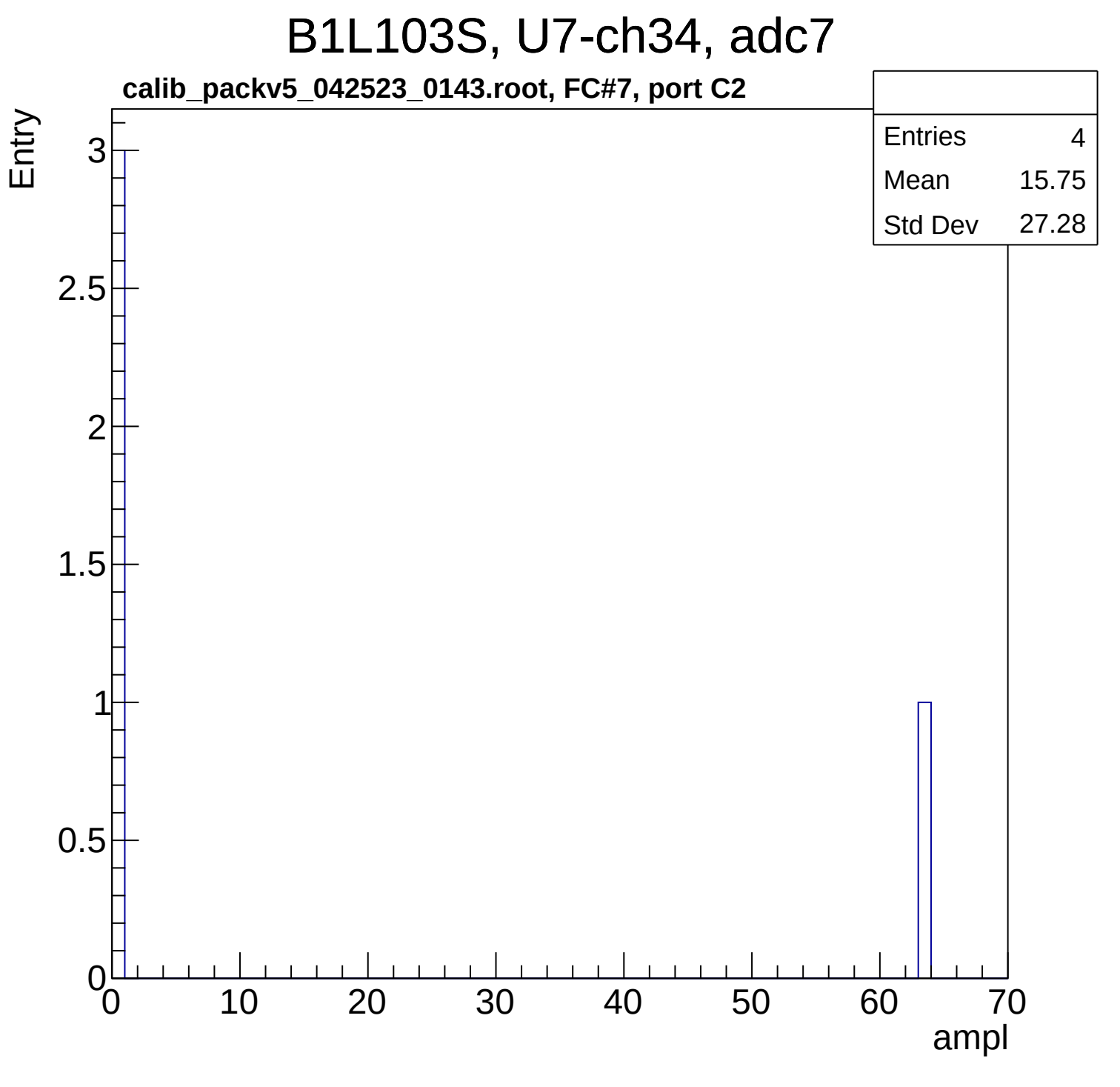
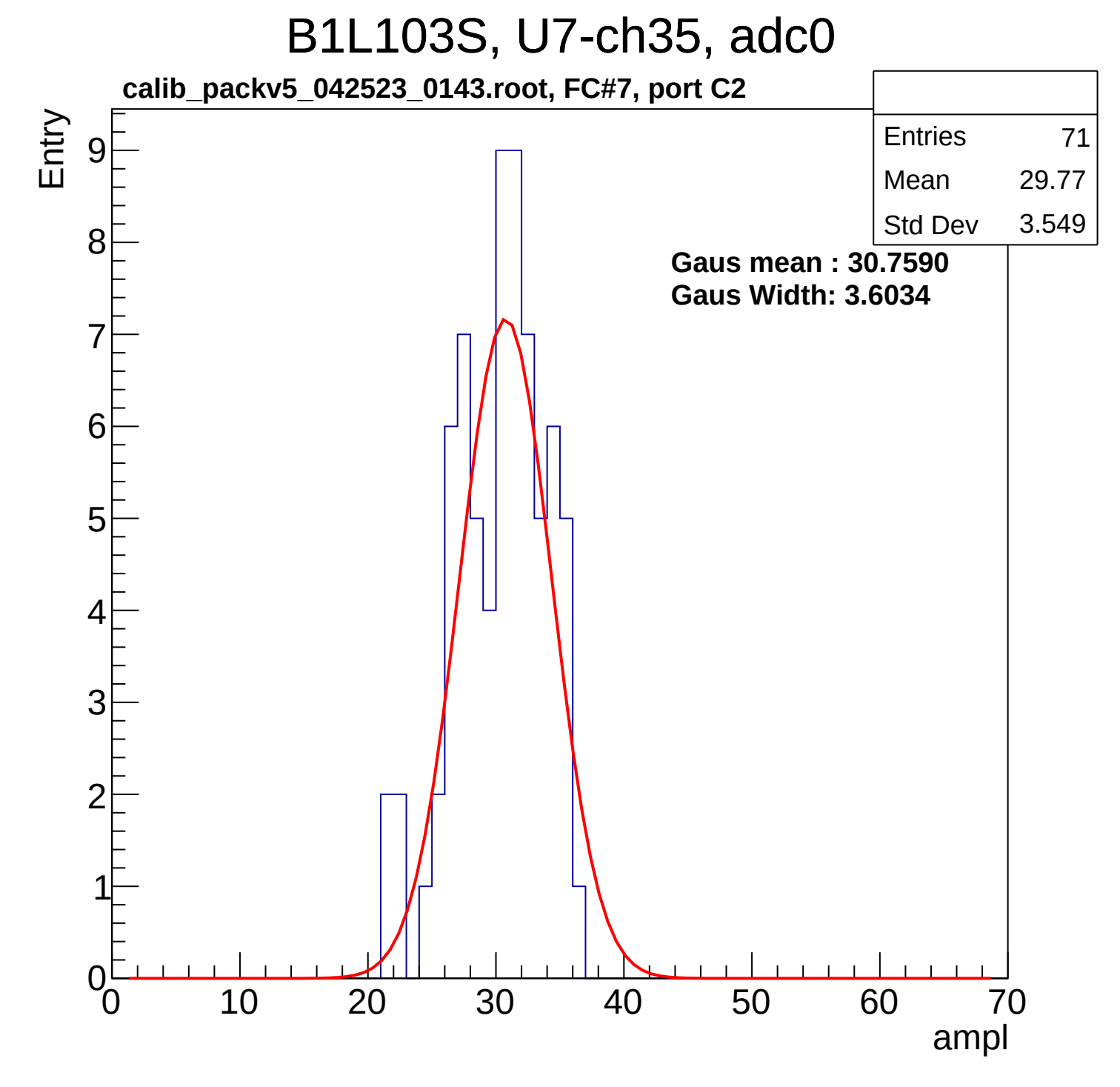
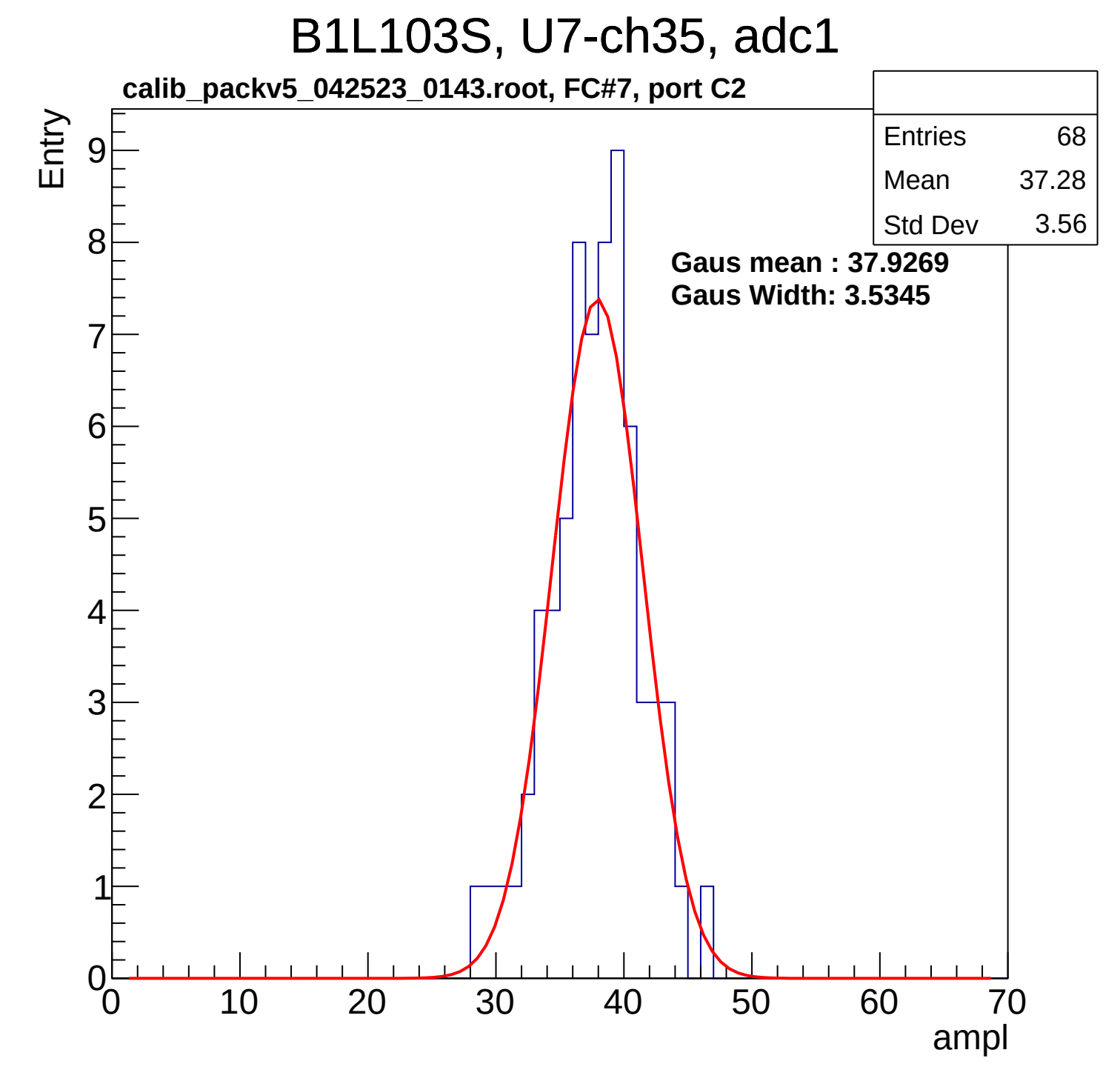
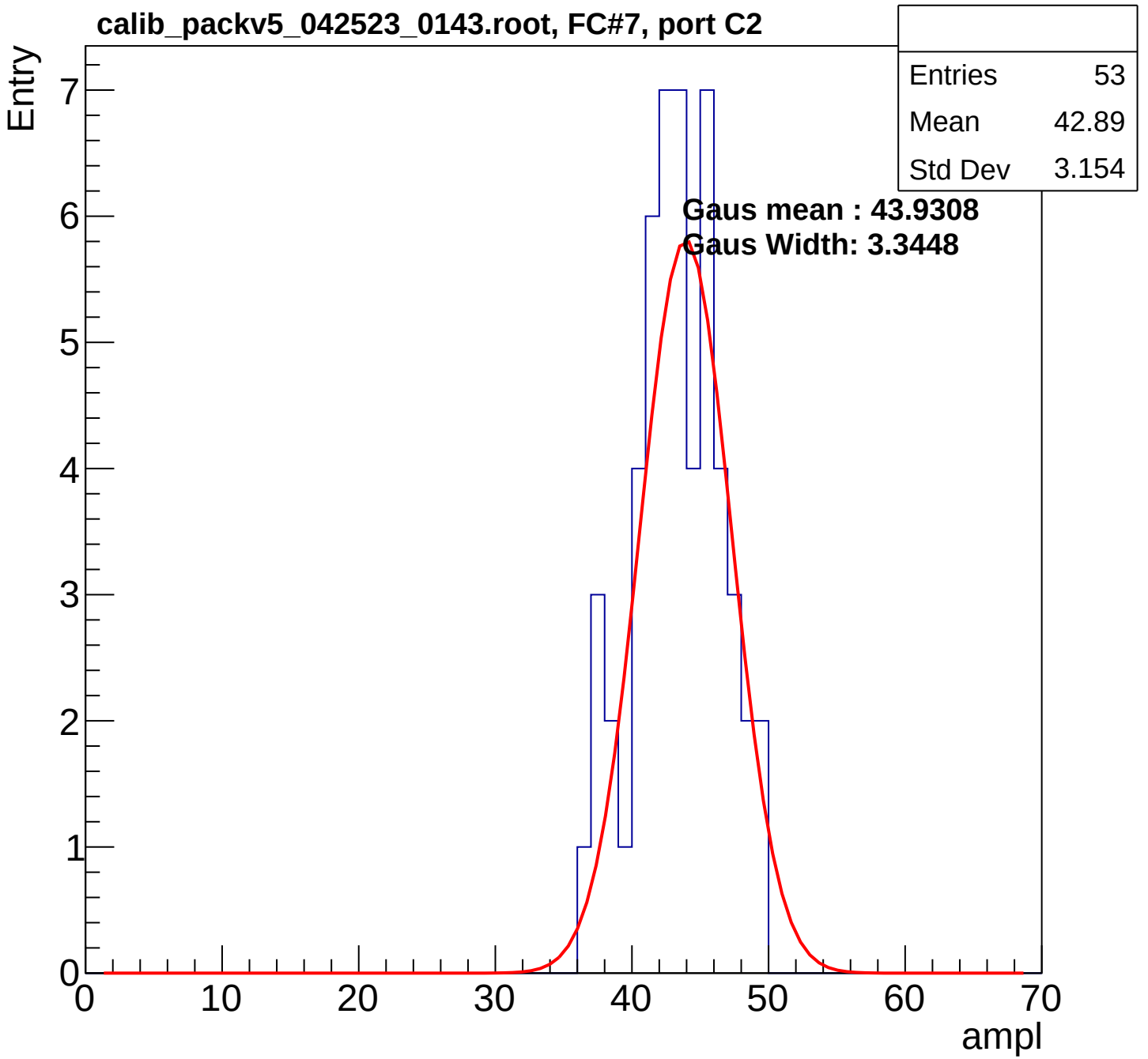

B1L103S, U7-ch34, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 14
Mean 61.43
Std Dev 2.095
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch34, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 4
Mean 15.75
Std Dev 27.28
Entry
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch35, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 71
Mean 29.77
Std Dev 3.549
Gaus mean : 30.7590
Gaus Width: 3.6034
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch35, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 37.28
Std Dev 3.56
Gaus mean : 37.9269
Gaus Width: 3.5345
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch35, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 42.89
Std Dev 3.154
Gaus mean : 43.9308
Gaus Width: 3.3448
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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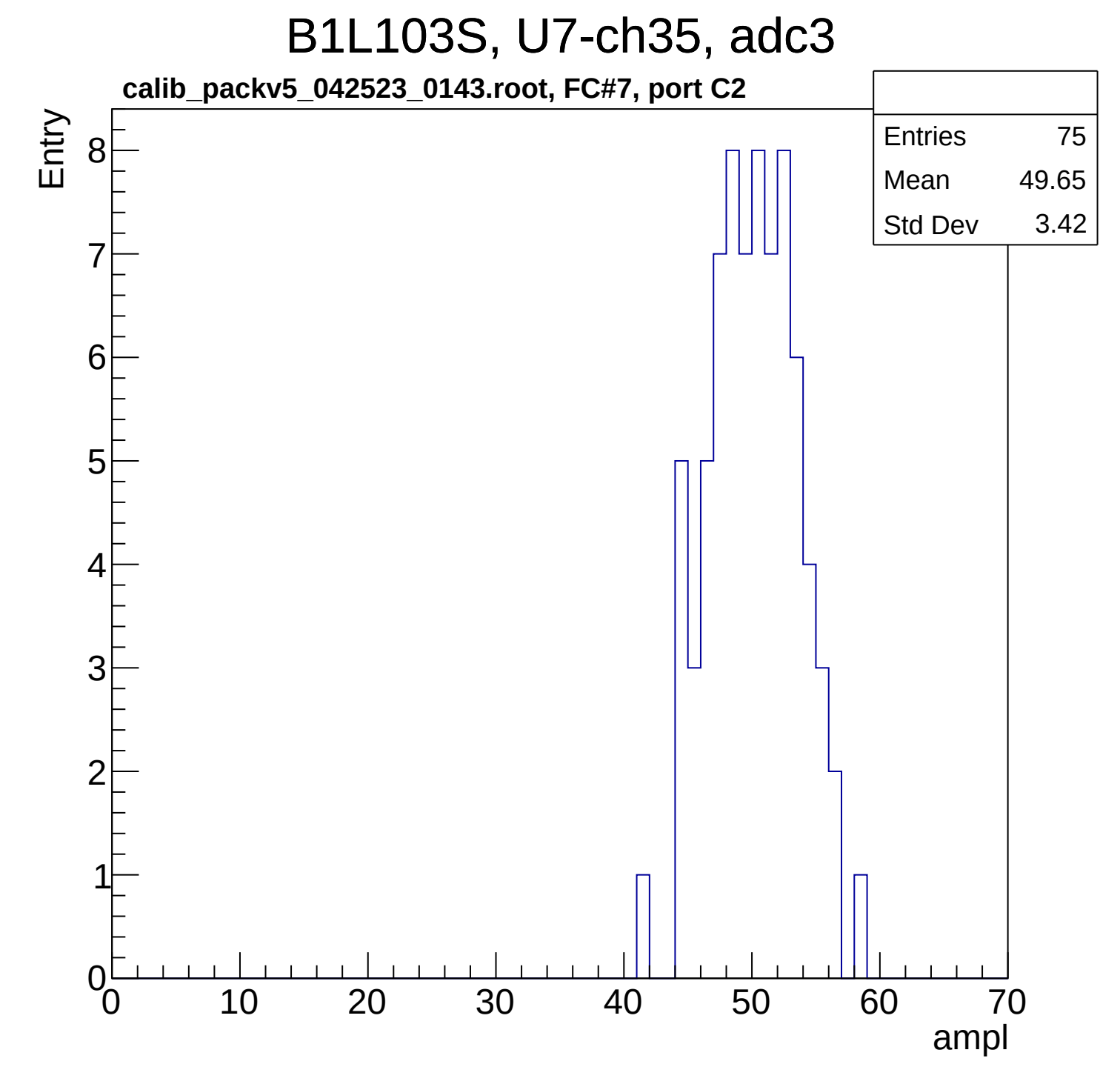
B1L103S, U7-ch35, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 75
Mean 49.65
Std Dev 3.42
Entry
ampl
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1
2
3
4
5
6
7
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0
10
20
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40
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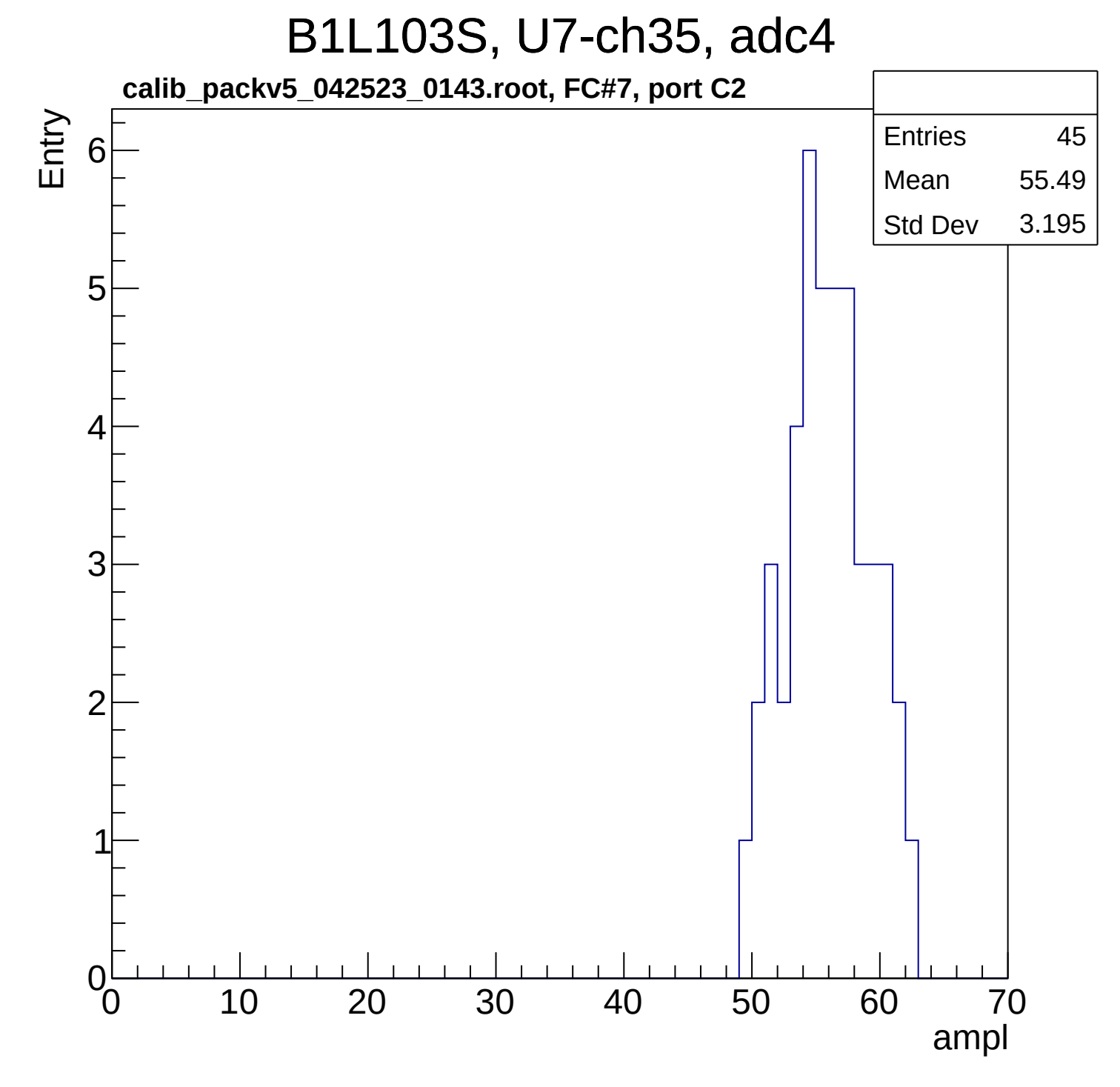
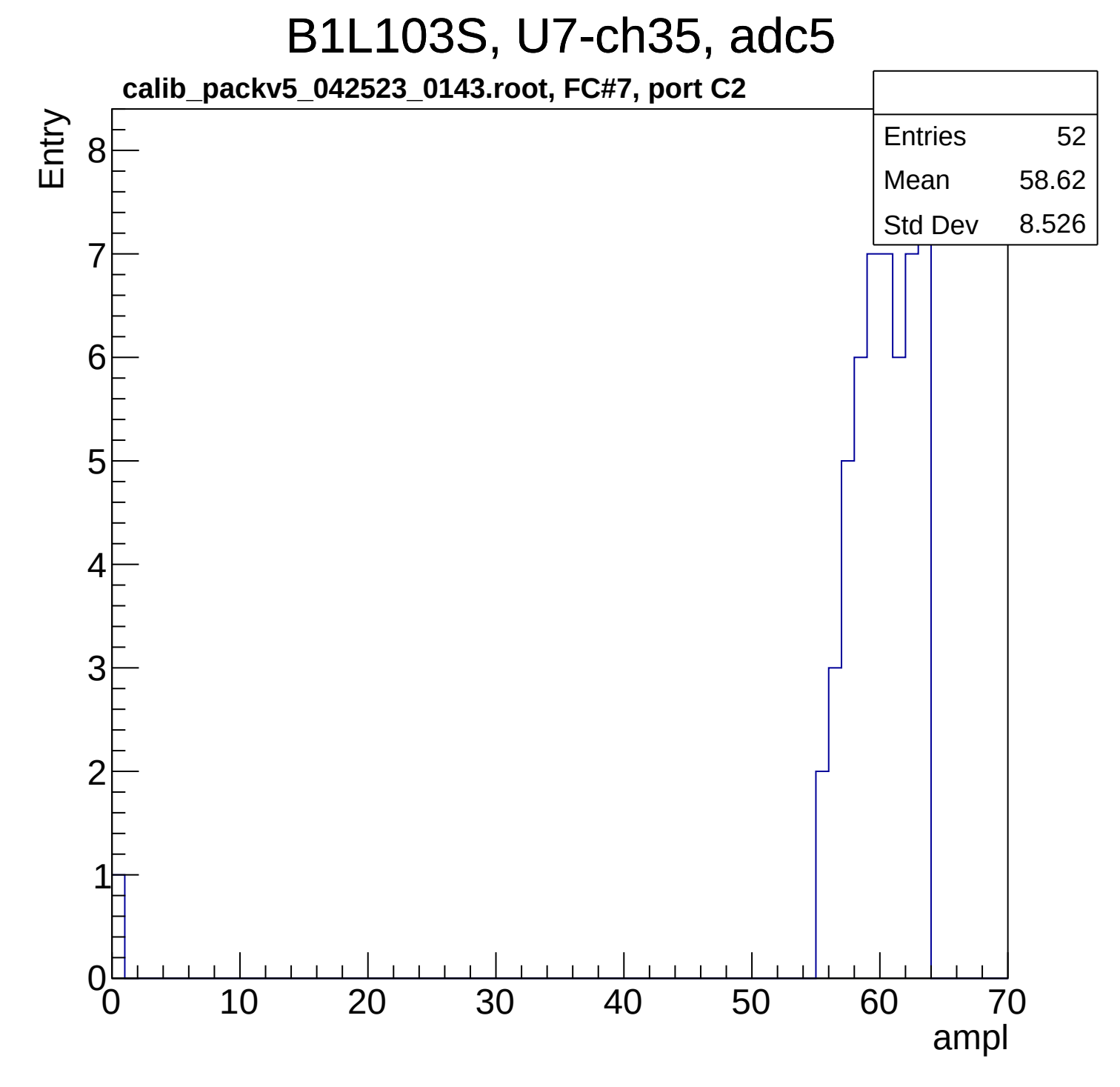
60
70


B1L103S, U7-ch35, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 45
Mean 55.49
Std Dev 3.195
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch35, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 52
Mean 58.62
Std Dev 8.526
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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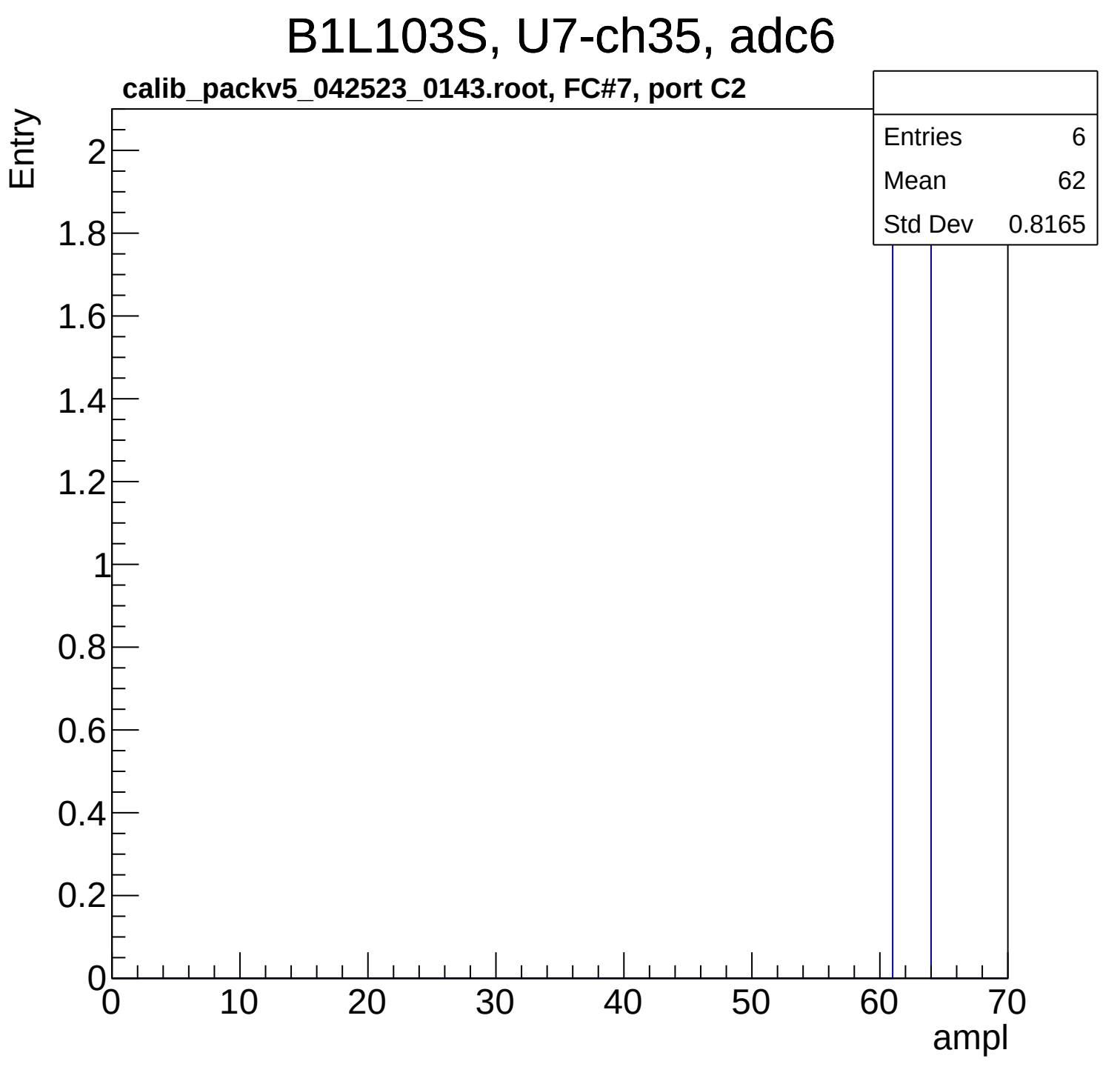
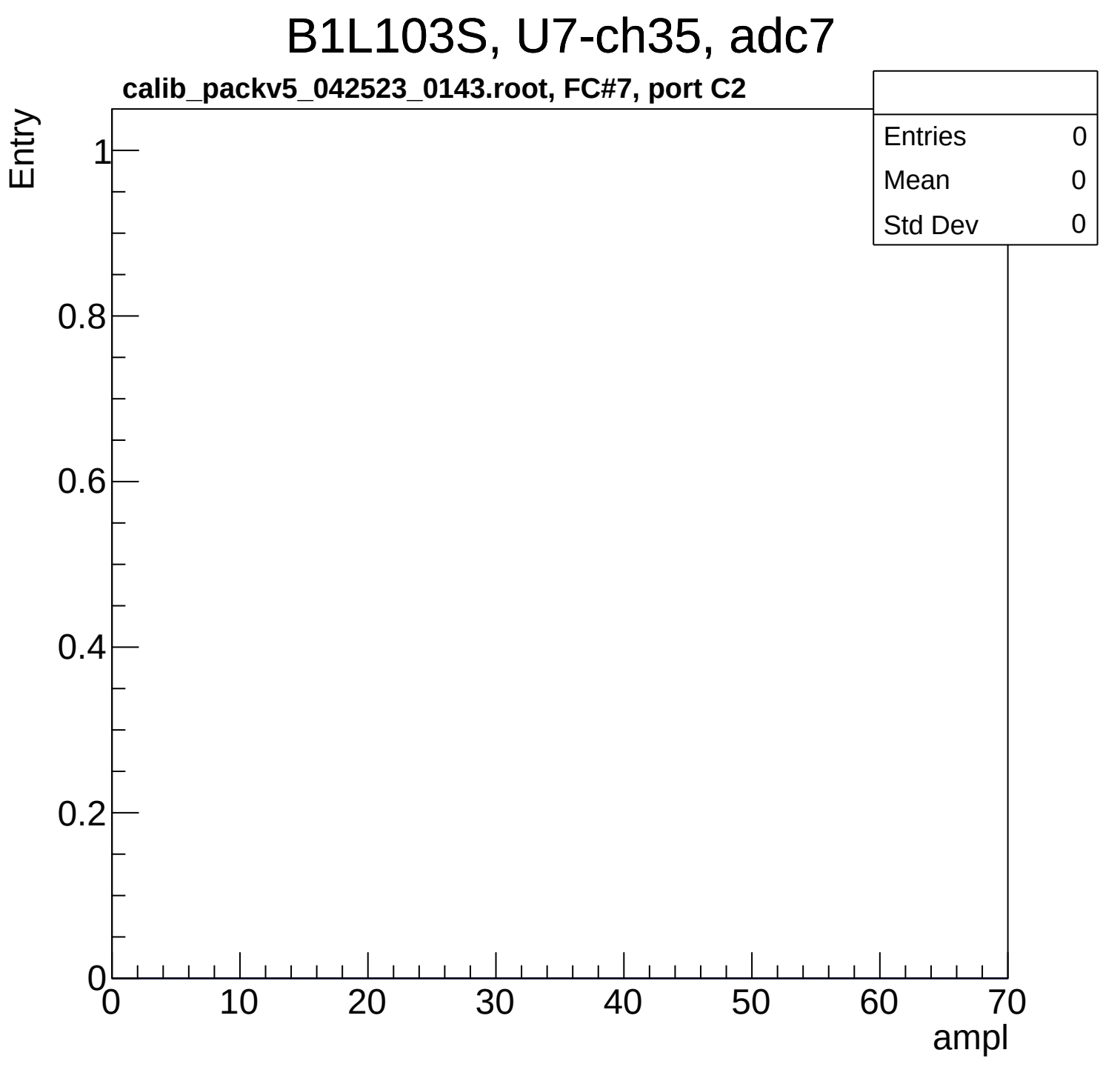
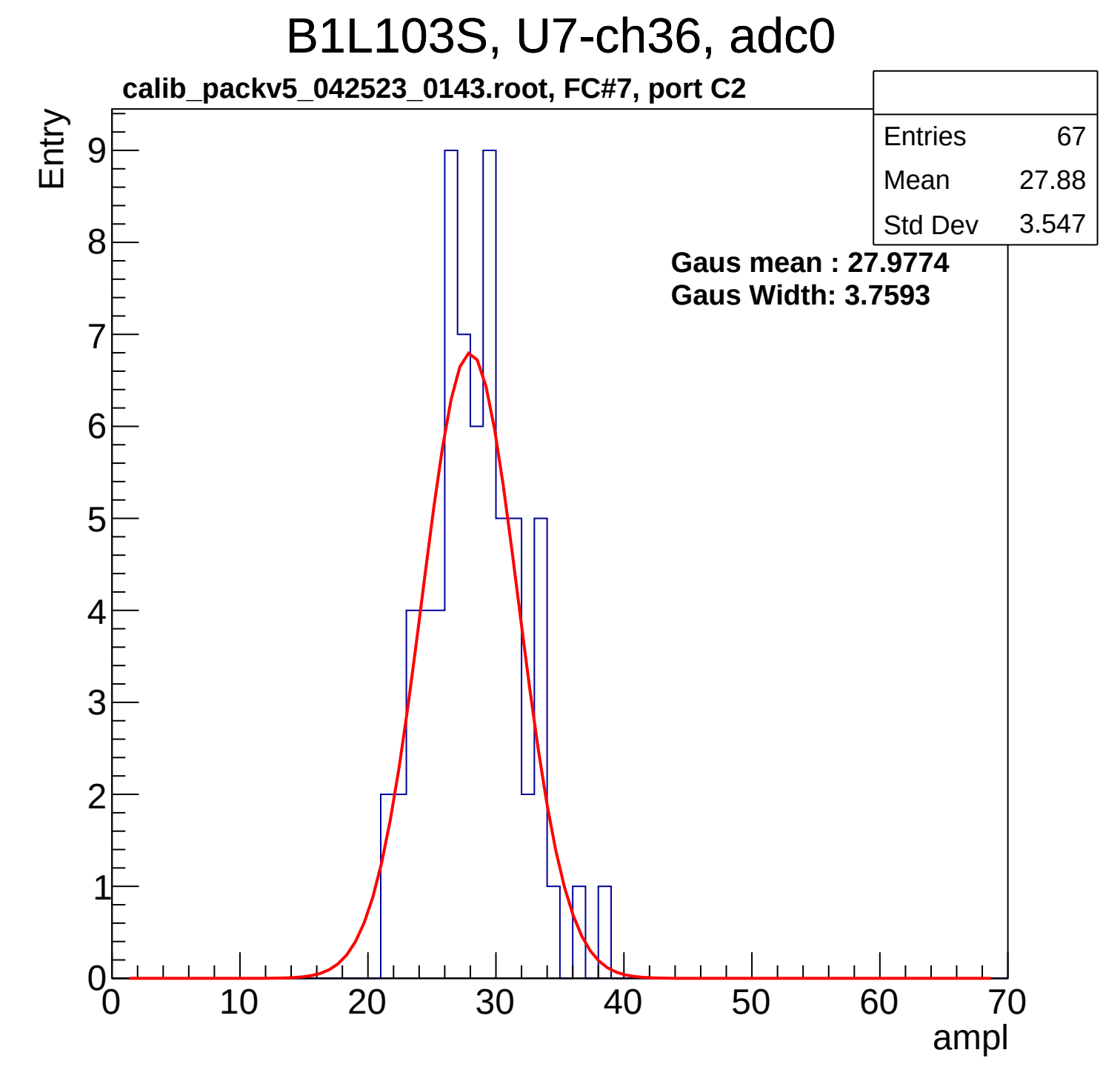

B1L103S, U7-ch35, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 6
Mean 62
Std Dev 0.8165
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U7-ch35, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch36, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 27.88
Std Dev 3.547
Gaus mean : 27.9774
Gaus Width: 3.7593
Entry
ampl
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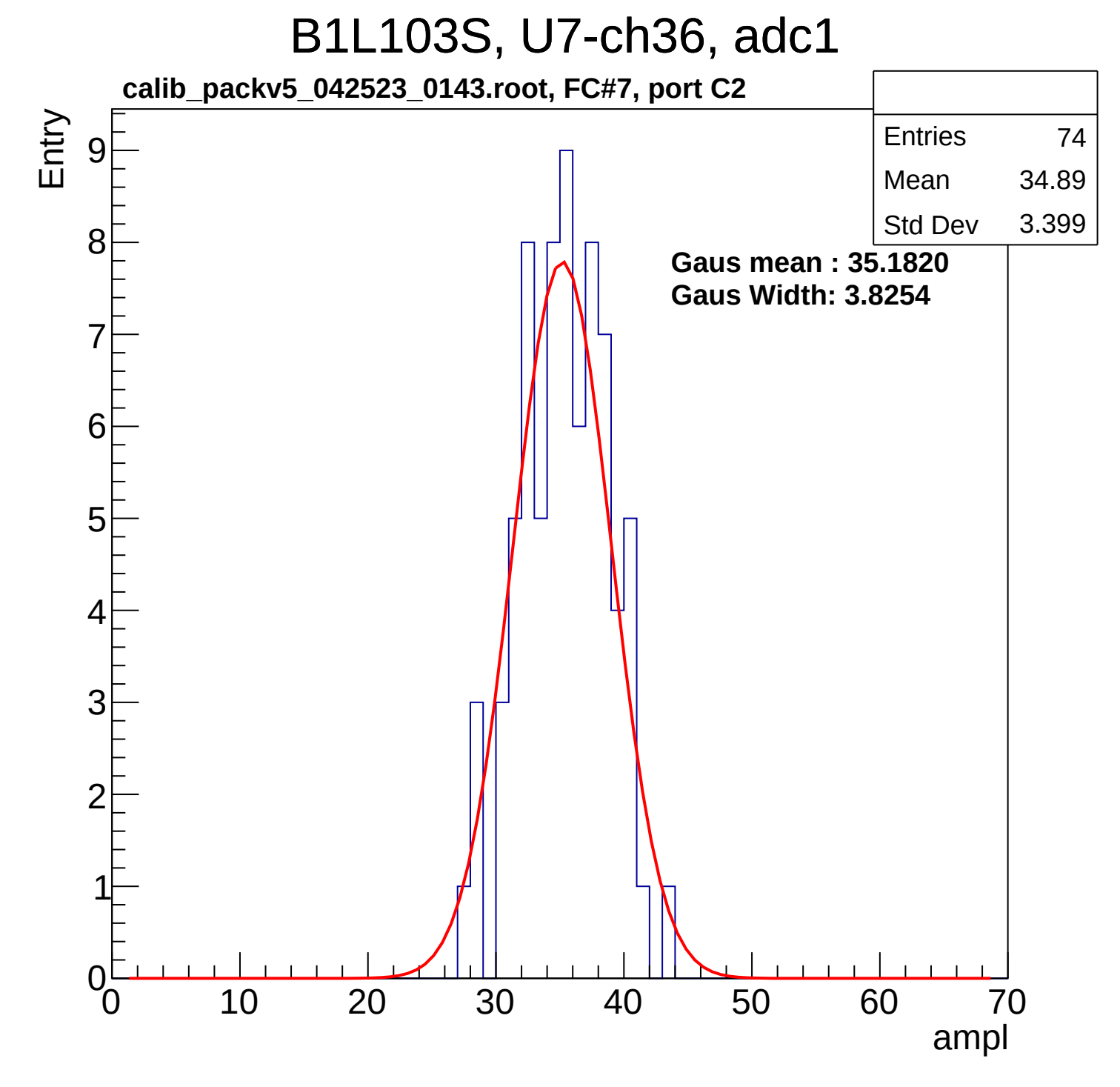
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch36, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 74
Mean 34.89
Std Dev 3.399
Gaus mean : 35.1820
Gaus Width: 3.8254
Entry
ampl
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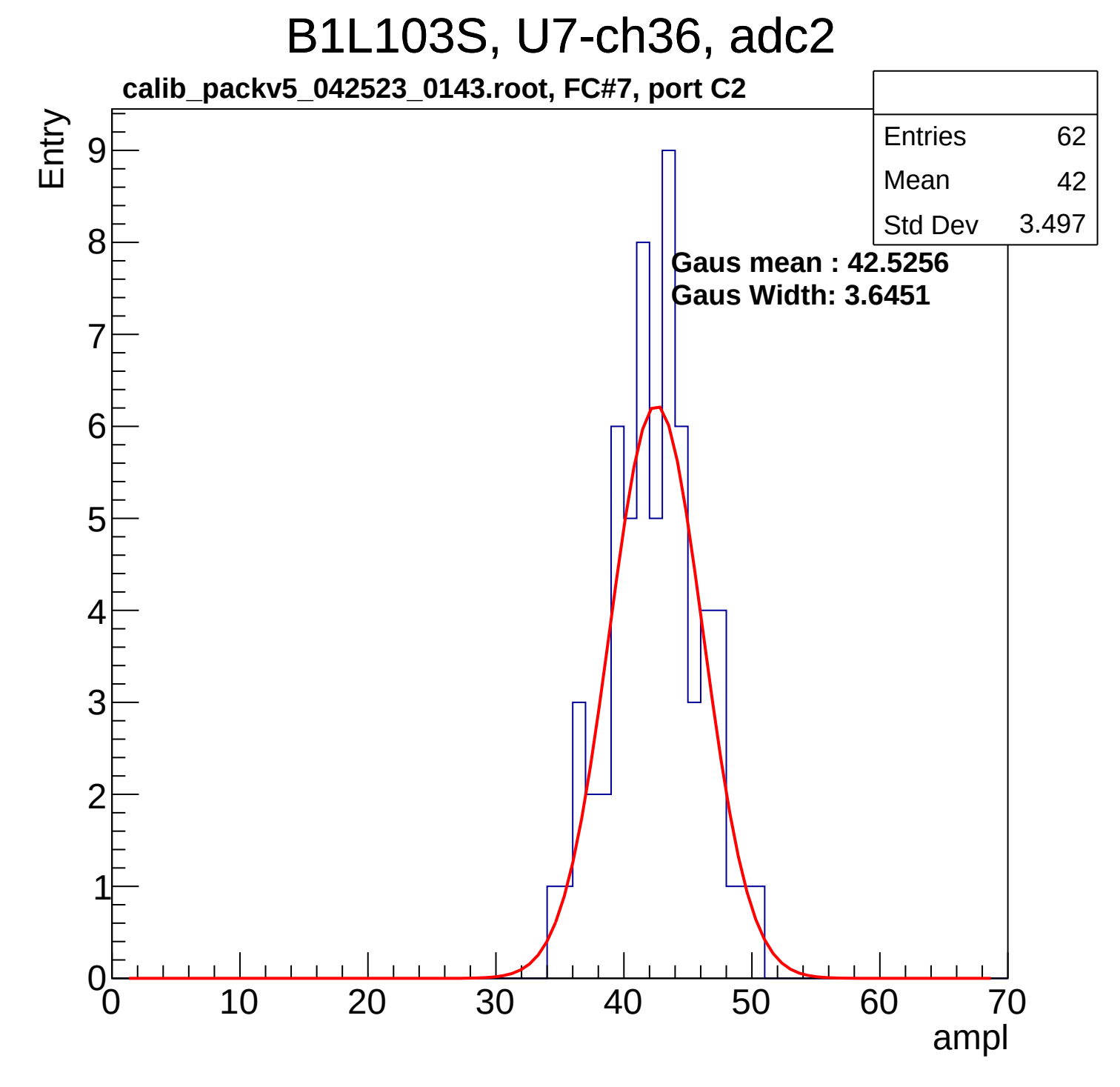
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch36, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 62
Mean 42
Std Dev 3.497
Gaus mean : 42.5256
Gaus Width: 3.6451
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
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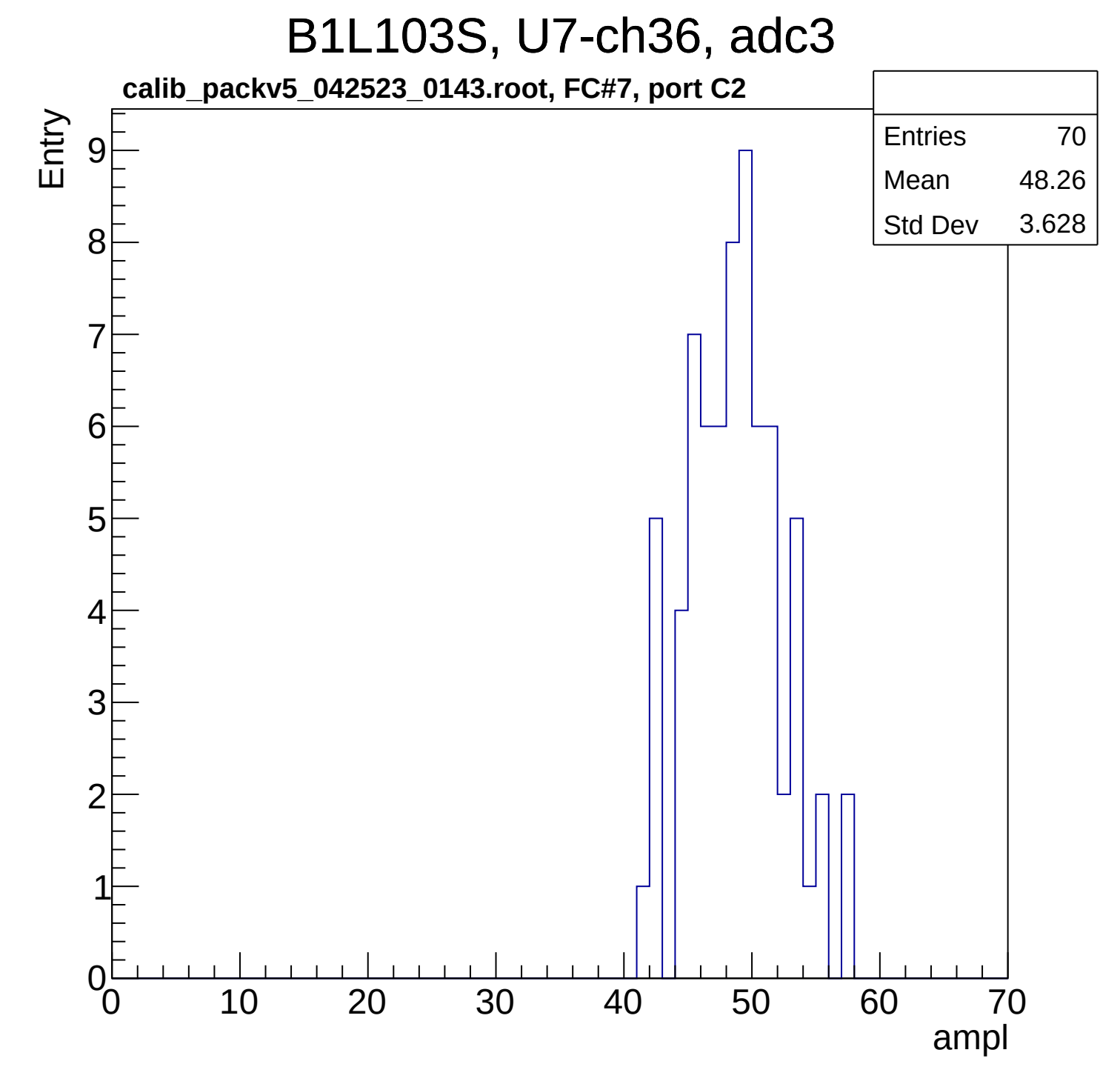
B1L103S, U7-ch36, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 48.26
Std Dev 3.628
Entry
ampl
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2
3
4
5
6
7
8
9
0
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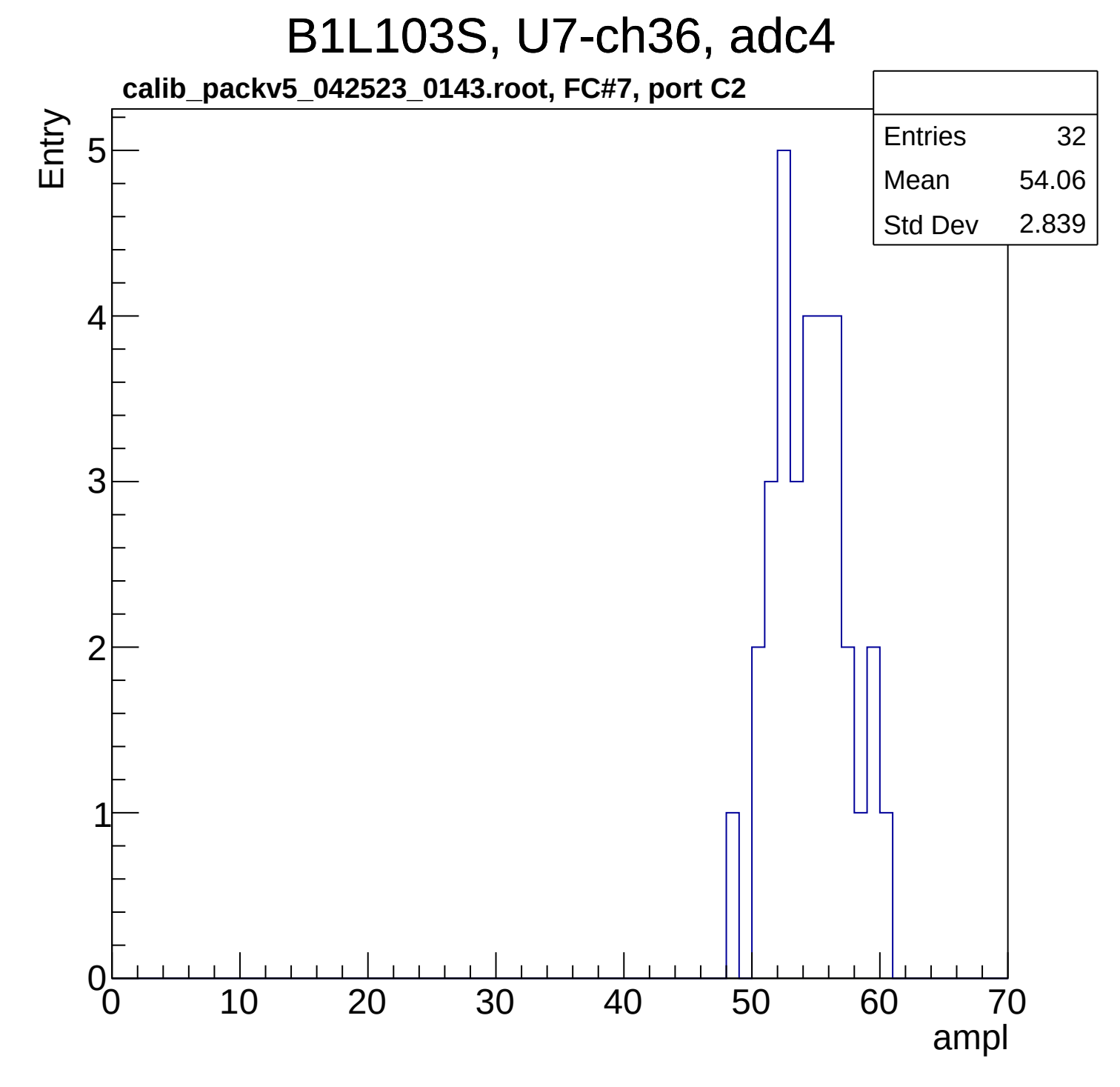
60
70


B1L103S, U7-ch36, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 32
Mean 54.06
Std Dev 2.839
Entry
0
1
2
3
4
5
0
10
20
30
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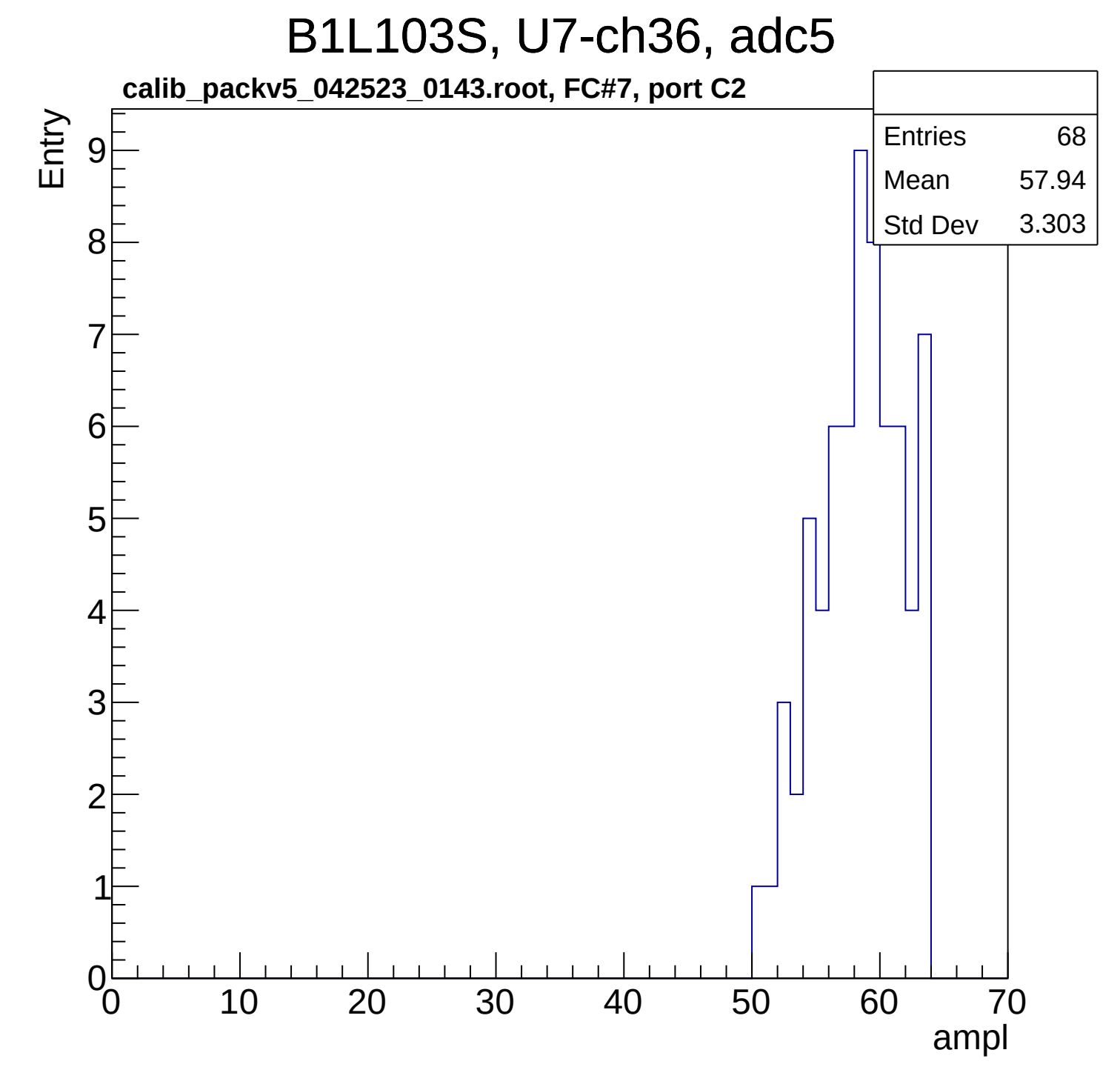
50
60
70
ampl


B1L103S, U7-ch36, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 57.94
Std Dev 3.303
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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40
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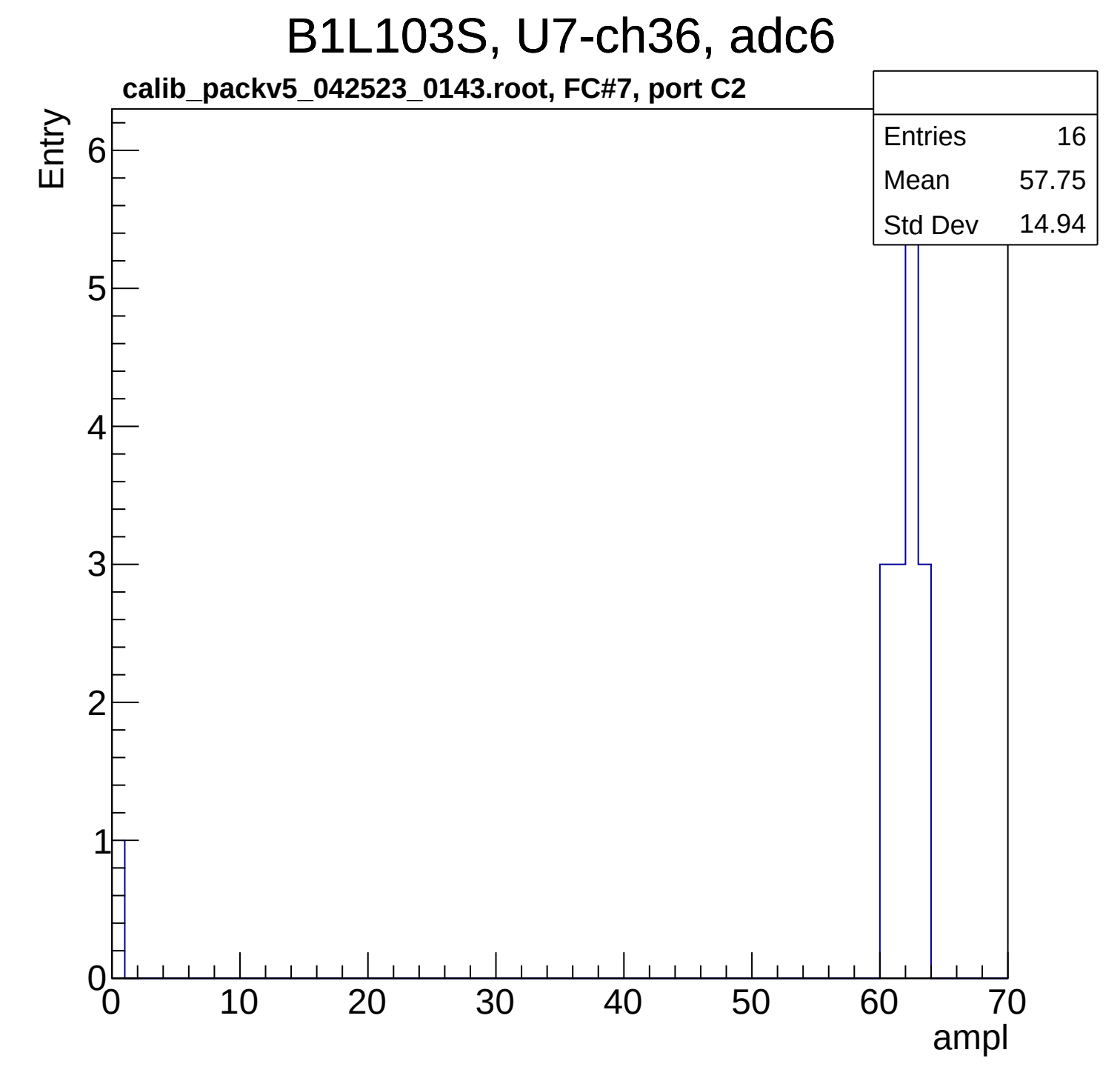
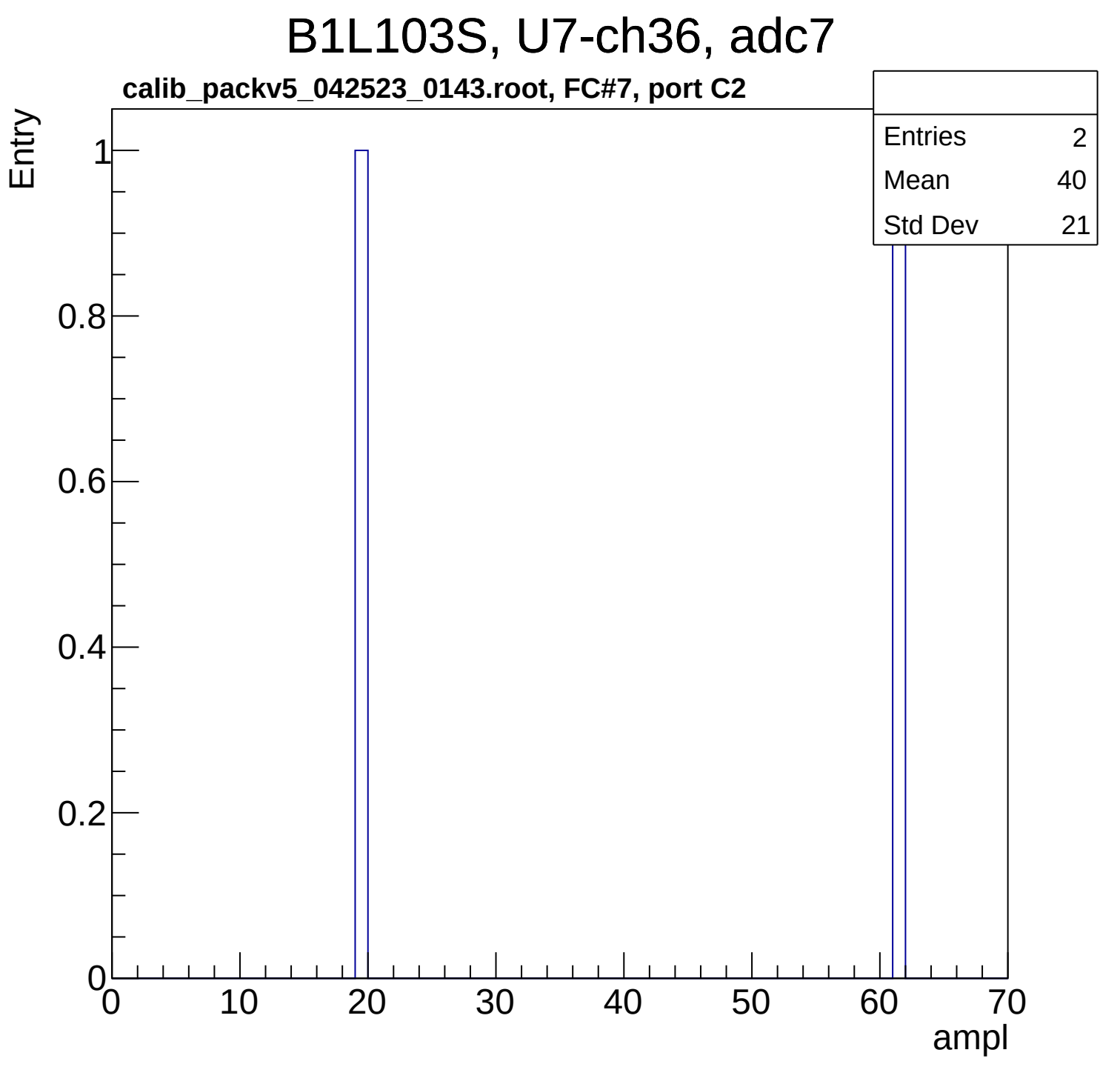
60
70


B1L103S, U7-ch36, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 16
Mean 57.75
Std Dev 14.94
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch36, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 40
Std Dev 21
Entry
ampl
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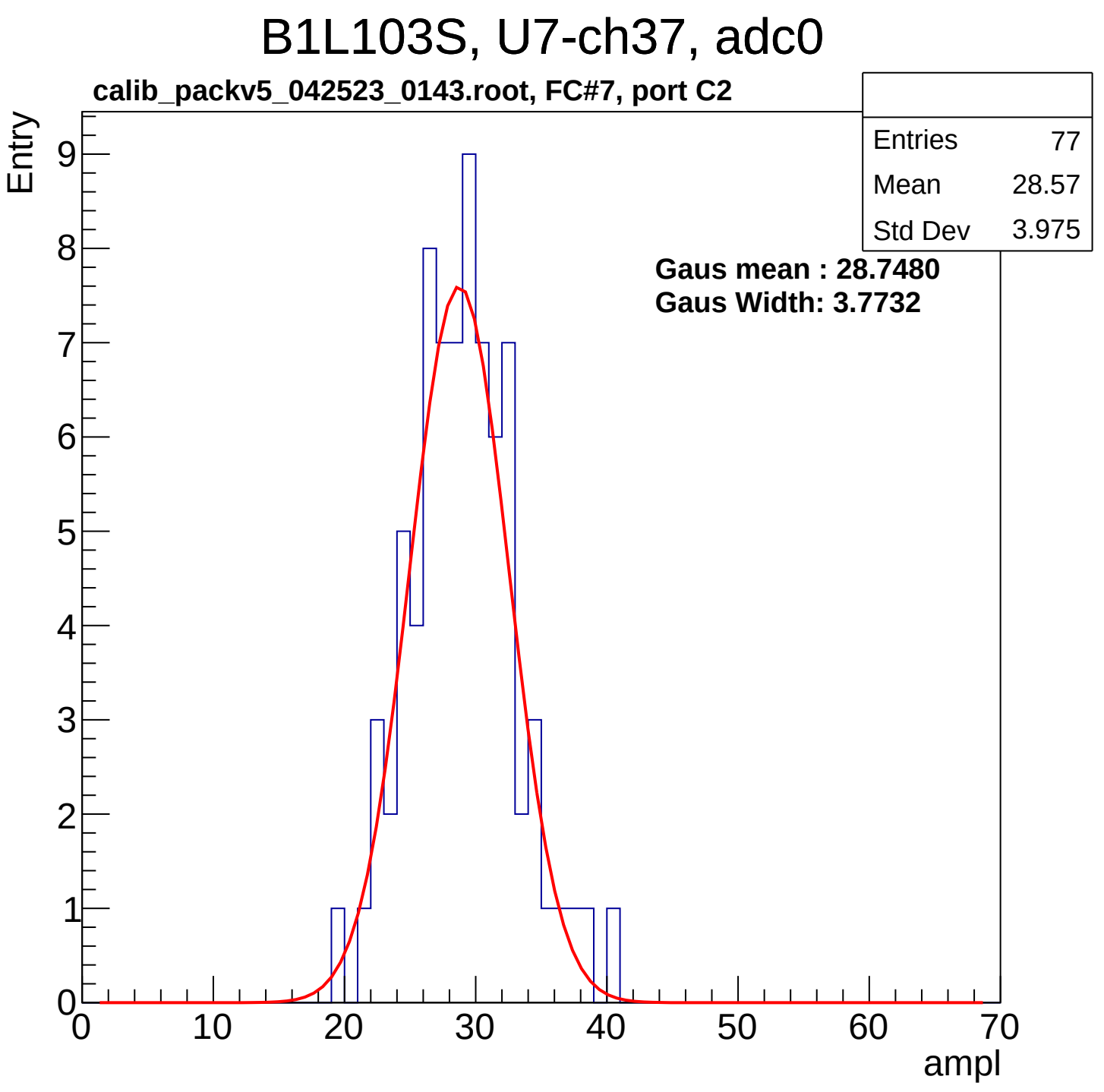
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B1L103S, U7-ch37, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 77
Mean 28.57
Std Dev 3.975
Gaus mean : 28.7480
Gaus Width: 3.7732
Entry
ampl
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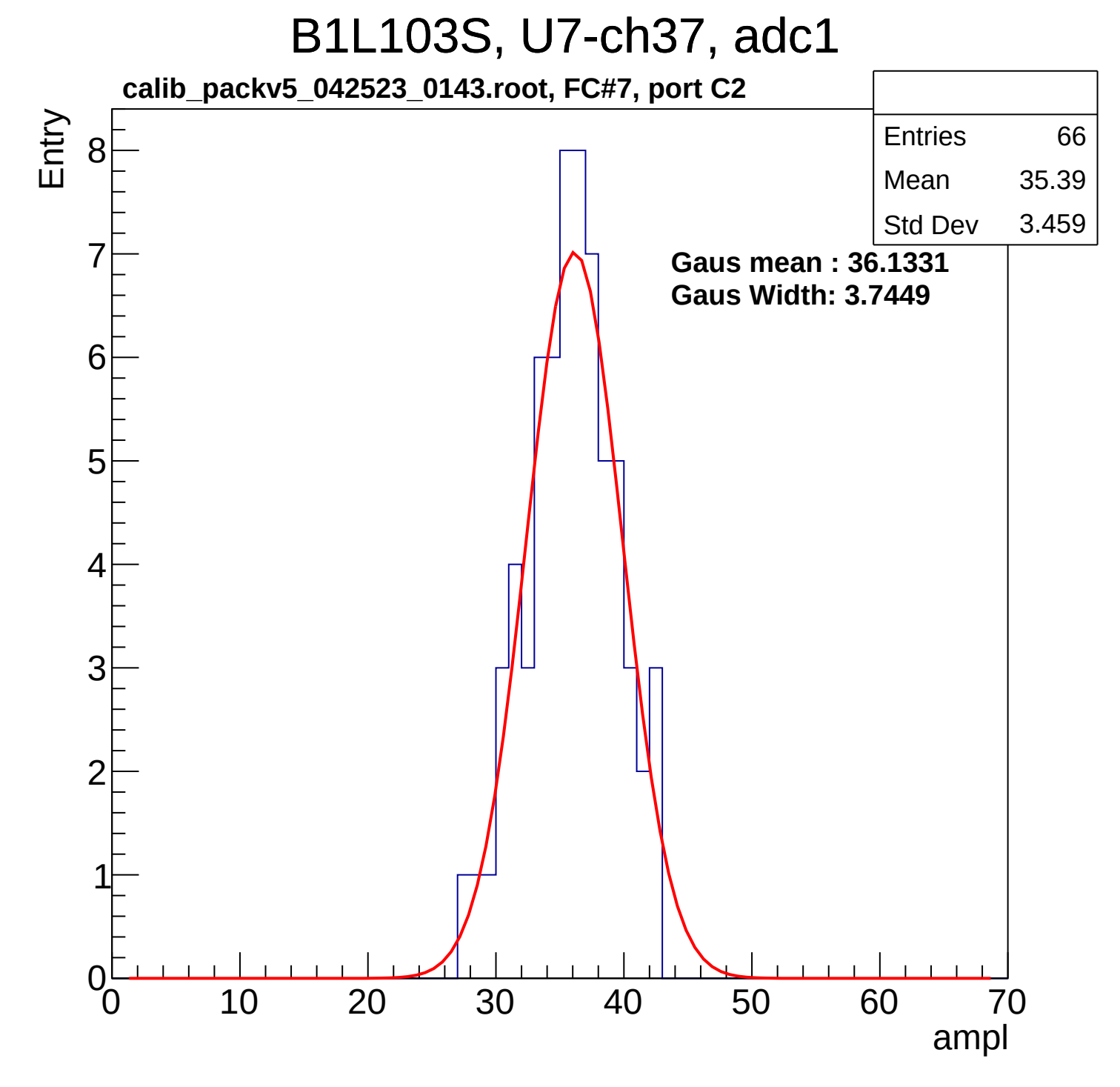
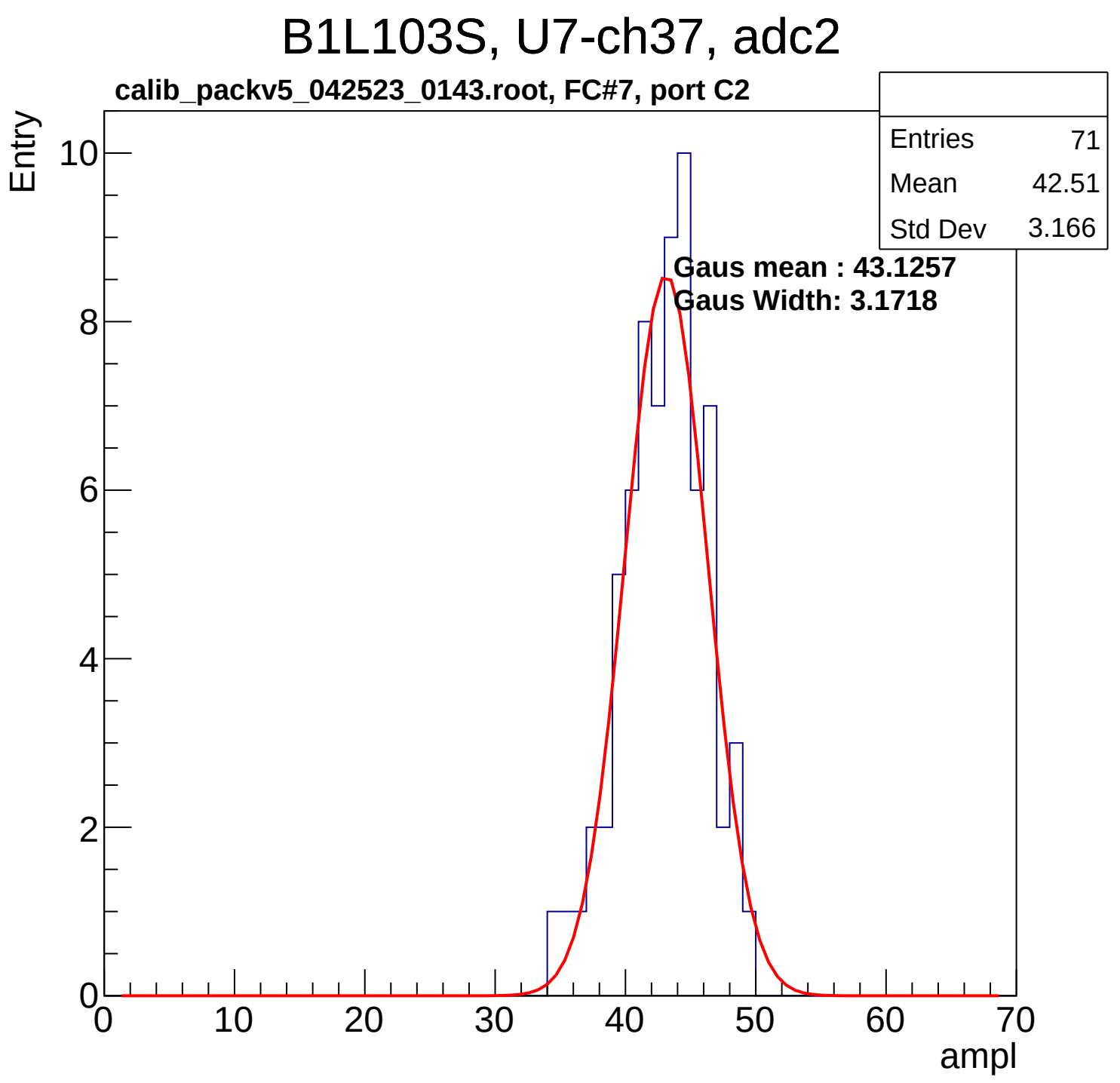
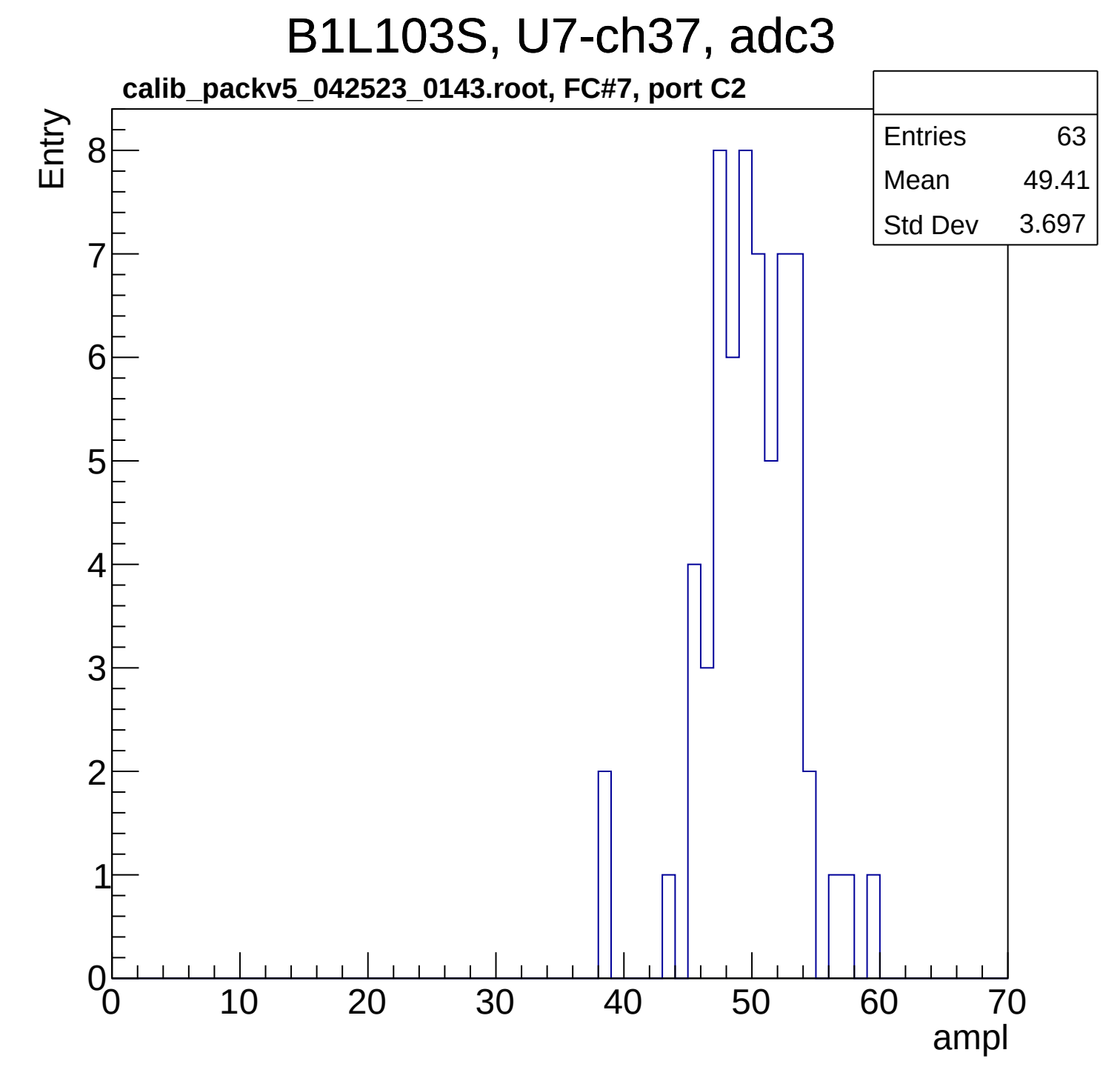
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch37, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 35.39
Std Dev 3.459
Gaus mean : 36.1331
Gaus Width: 3.7449
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch37, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 71
Mean 42.51
Std Dev 3.166
Gaus mean : 43.1257
Gaus Width: 3.1718
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch37, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 49.41
Std Dev 3.697
Entry
ampl
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1
2
3
4
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7
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10
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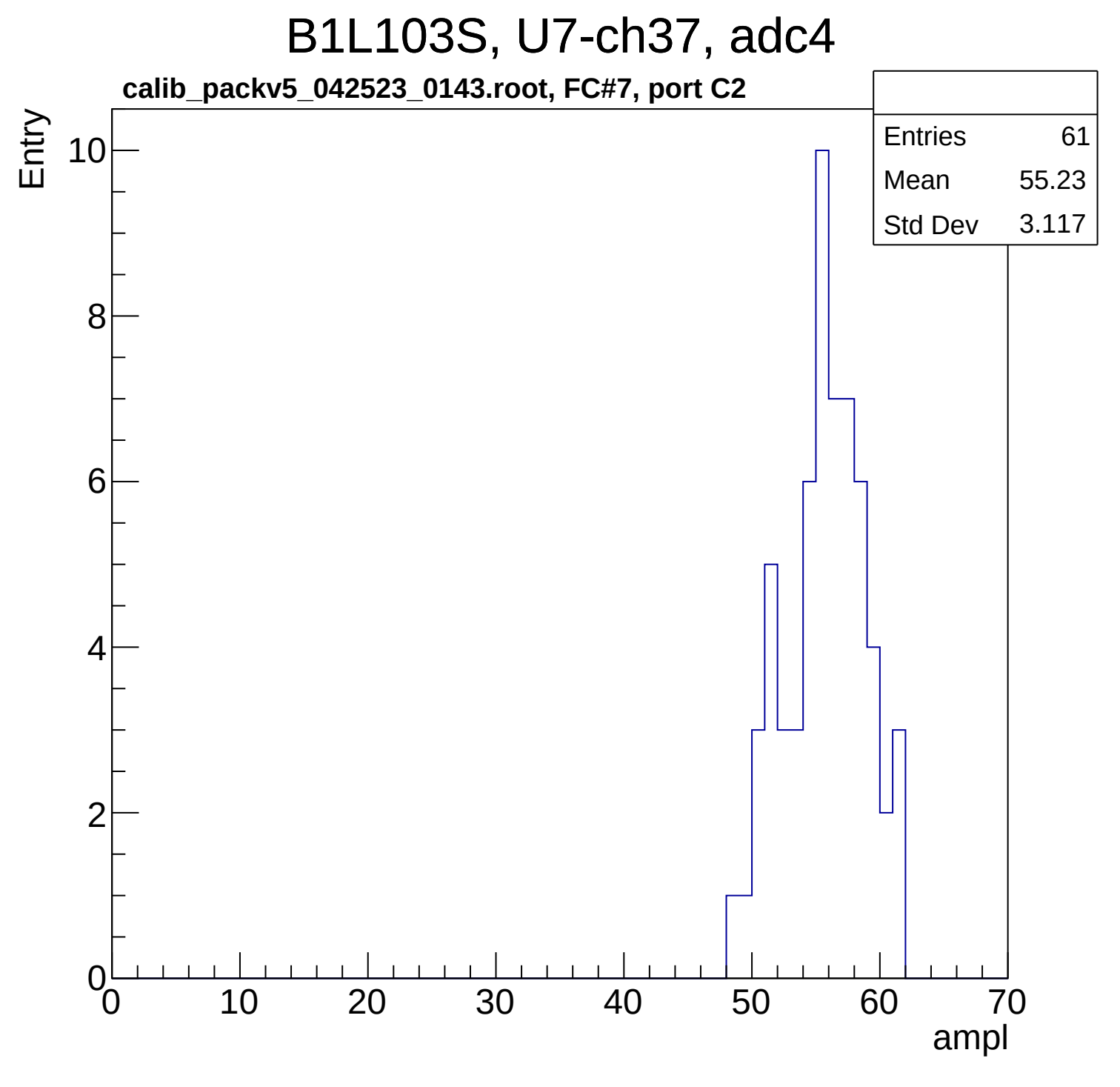
B1L103S, U7-ch37, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 61
Mean 55.23
Std Dev 3.117
Entry
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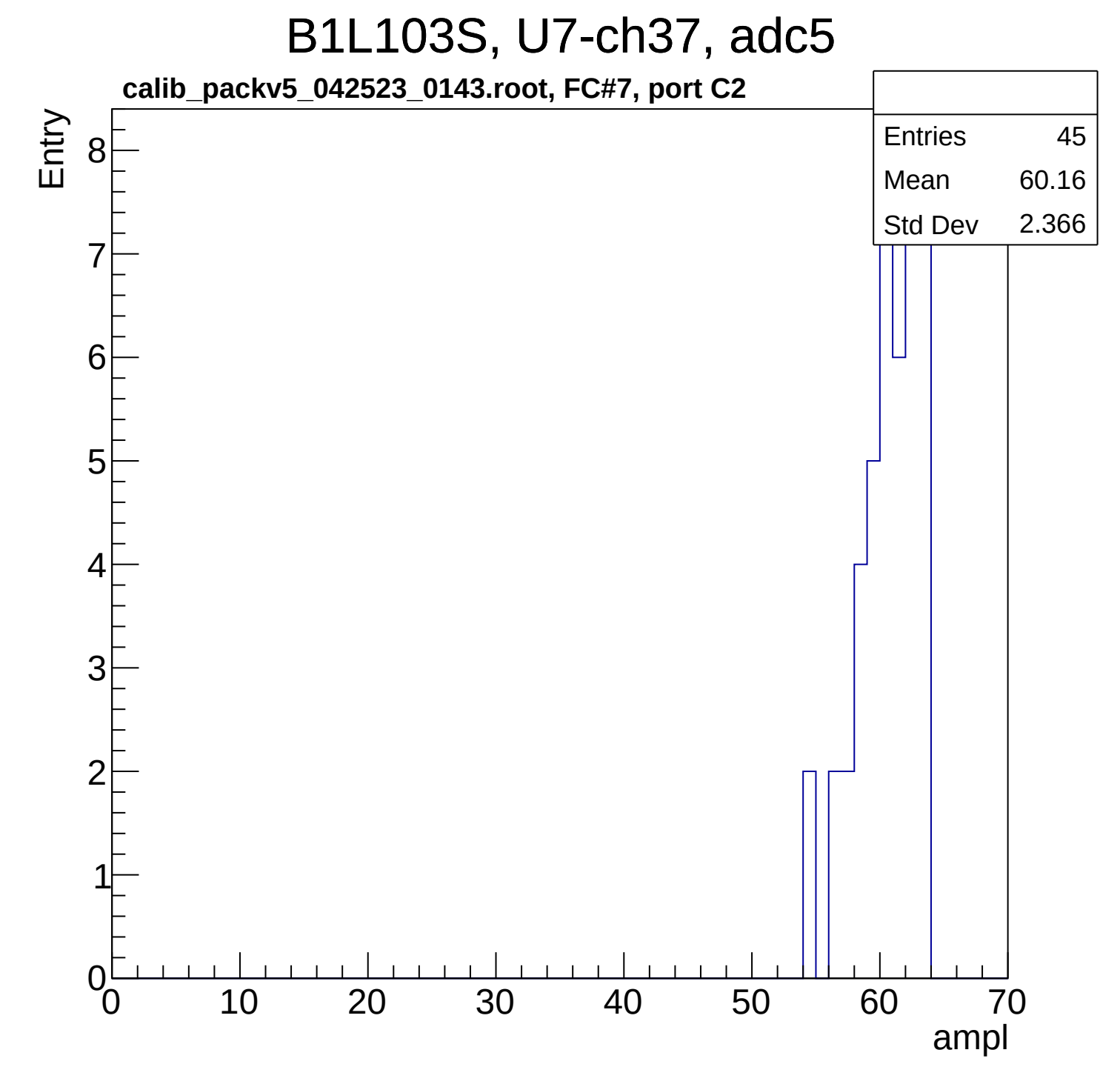
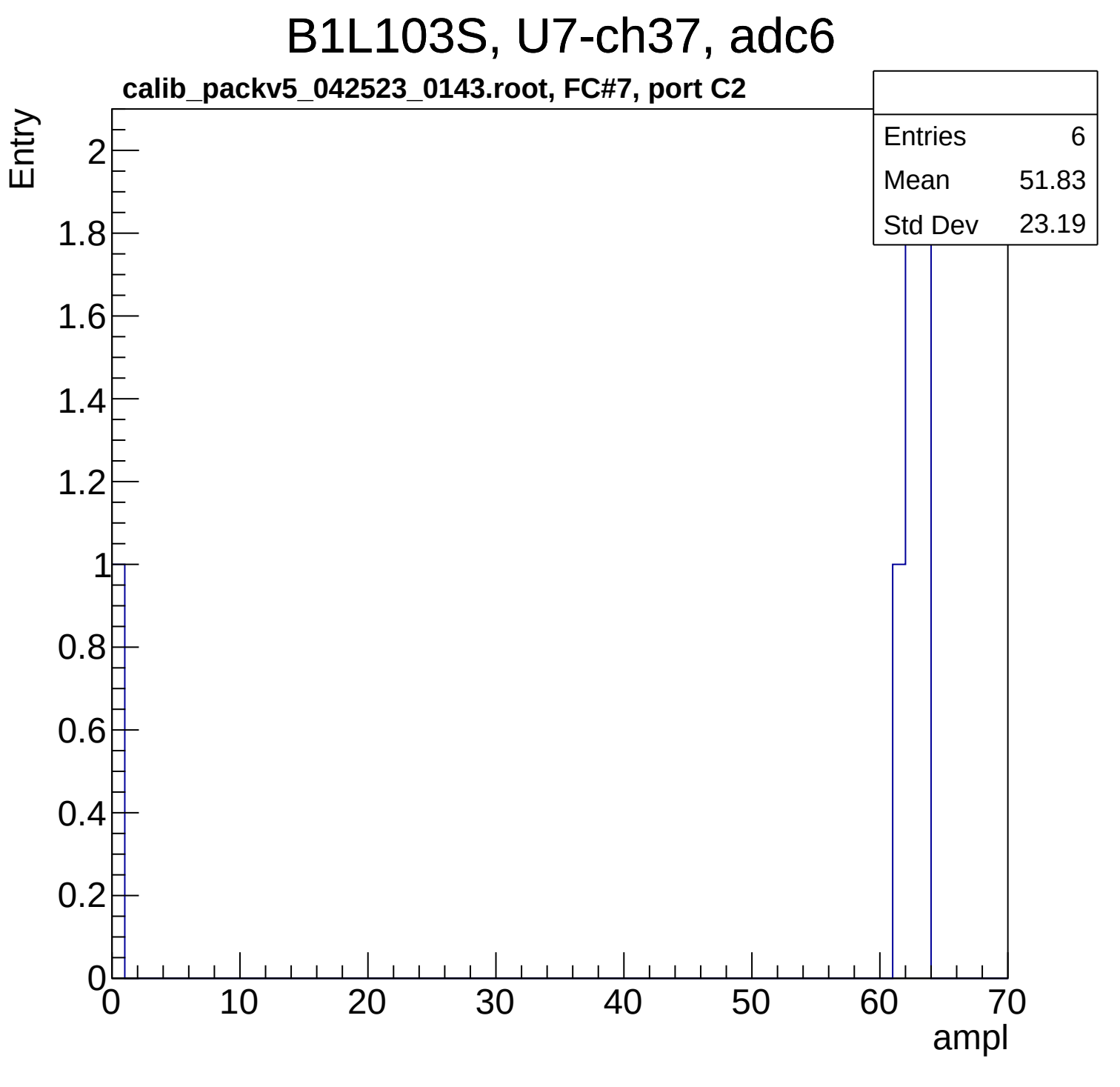
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch37, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 45
Mean 60.16
Std Dev 2.366
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch37, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 6
Mean 51.83
Std Dev 23.19
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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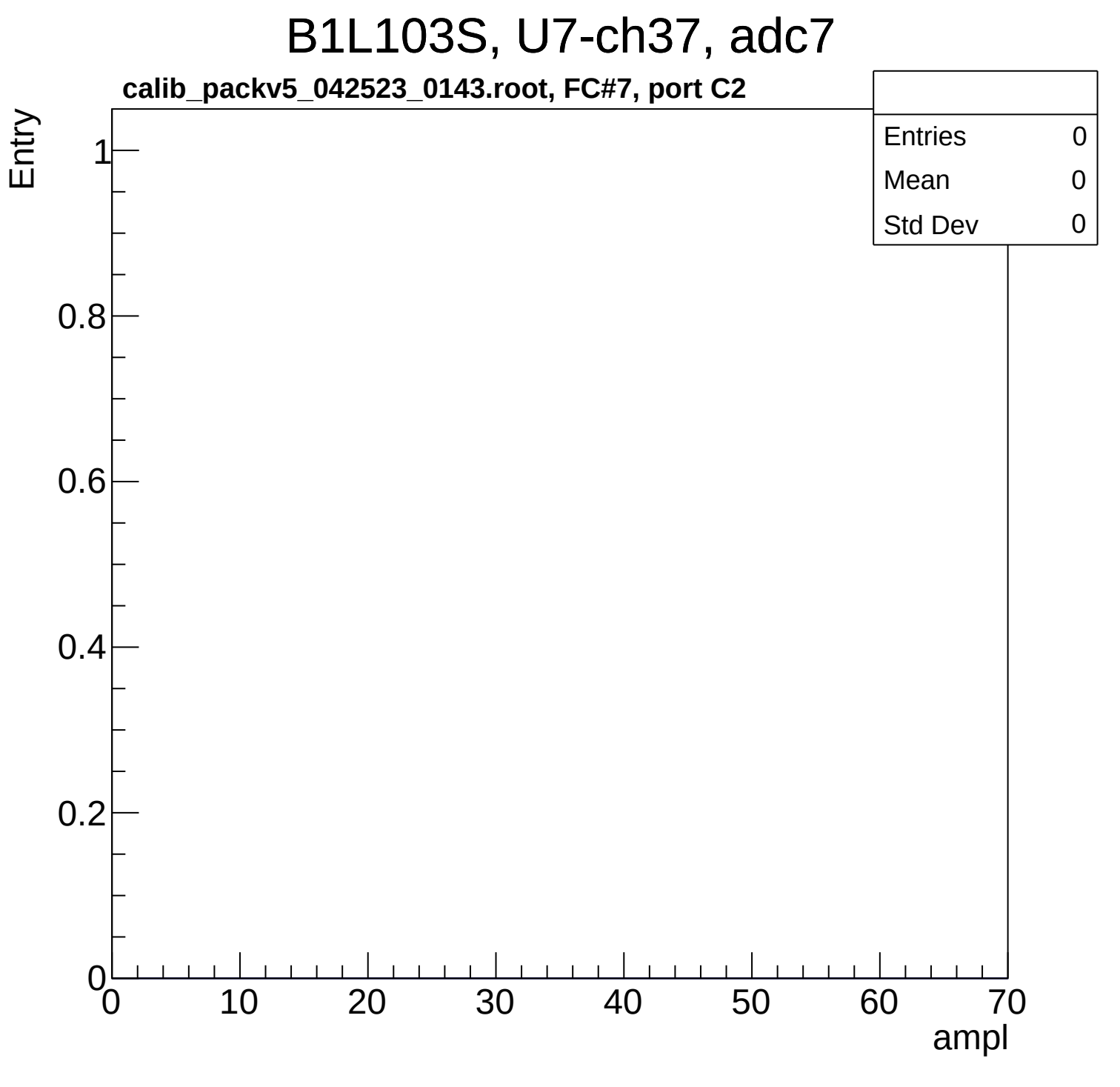
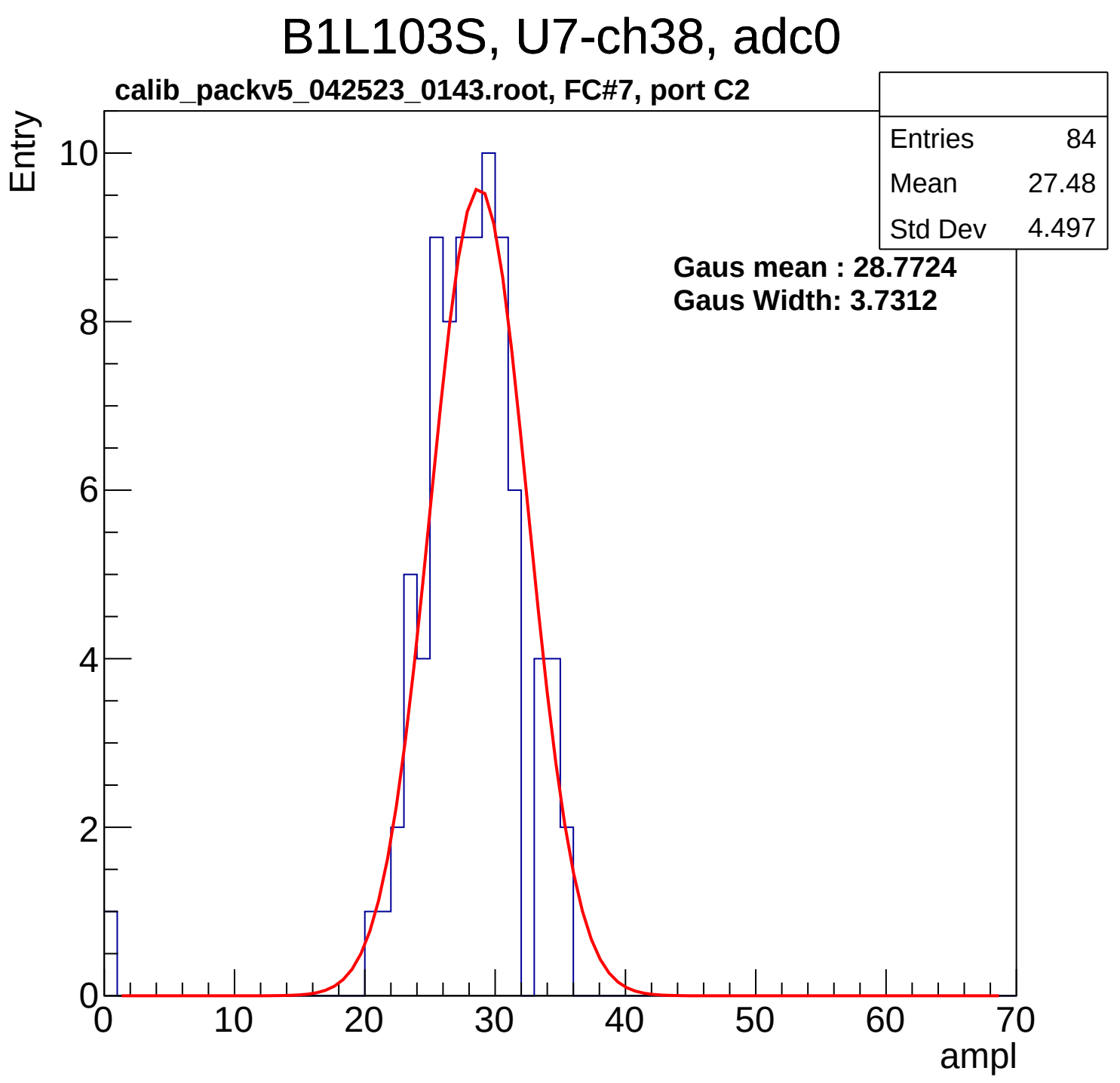
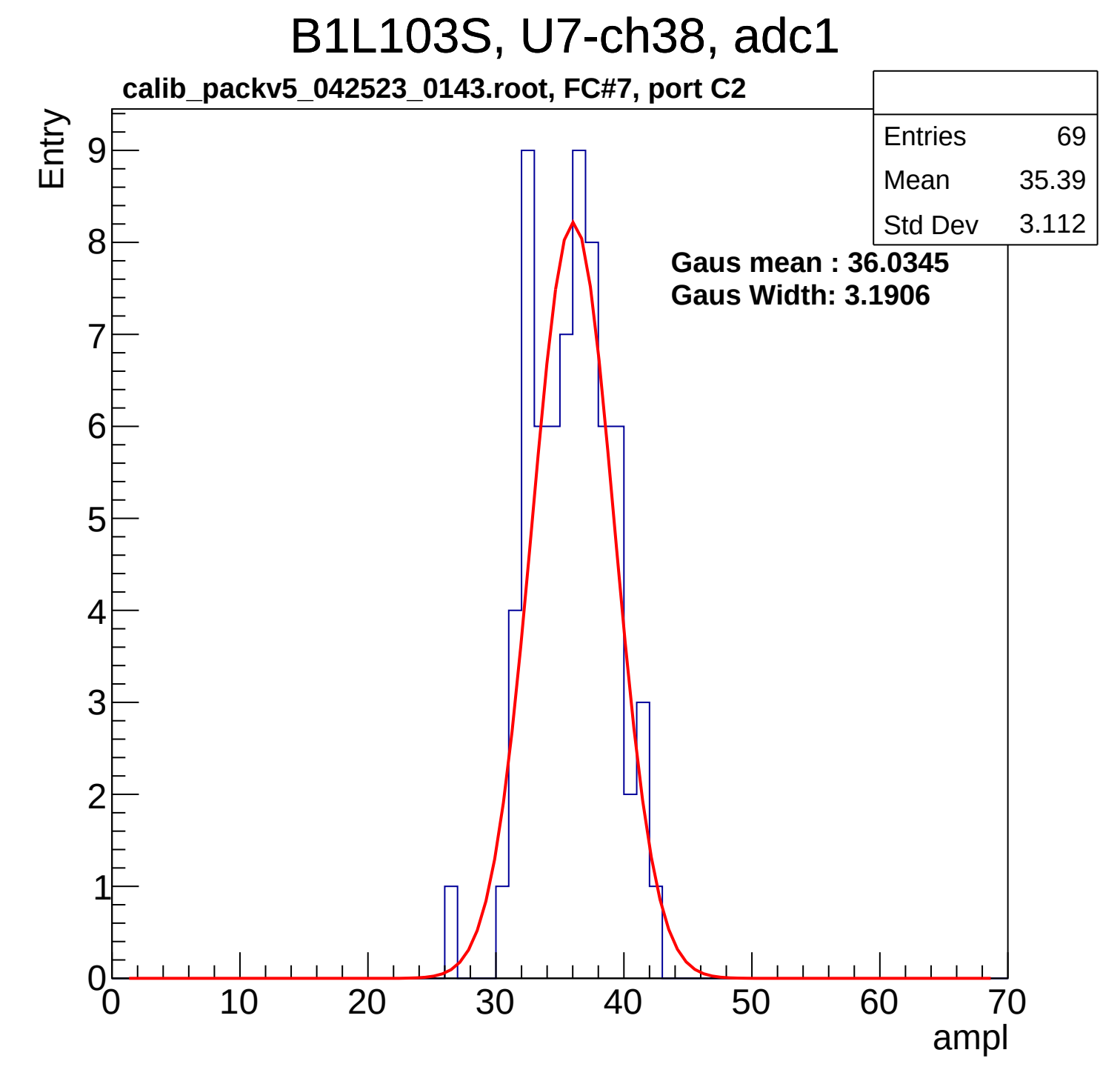
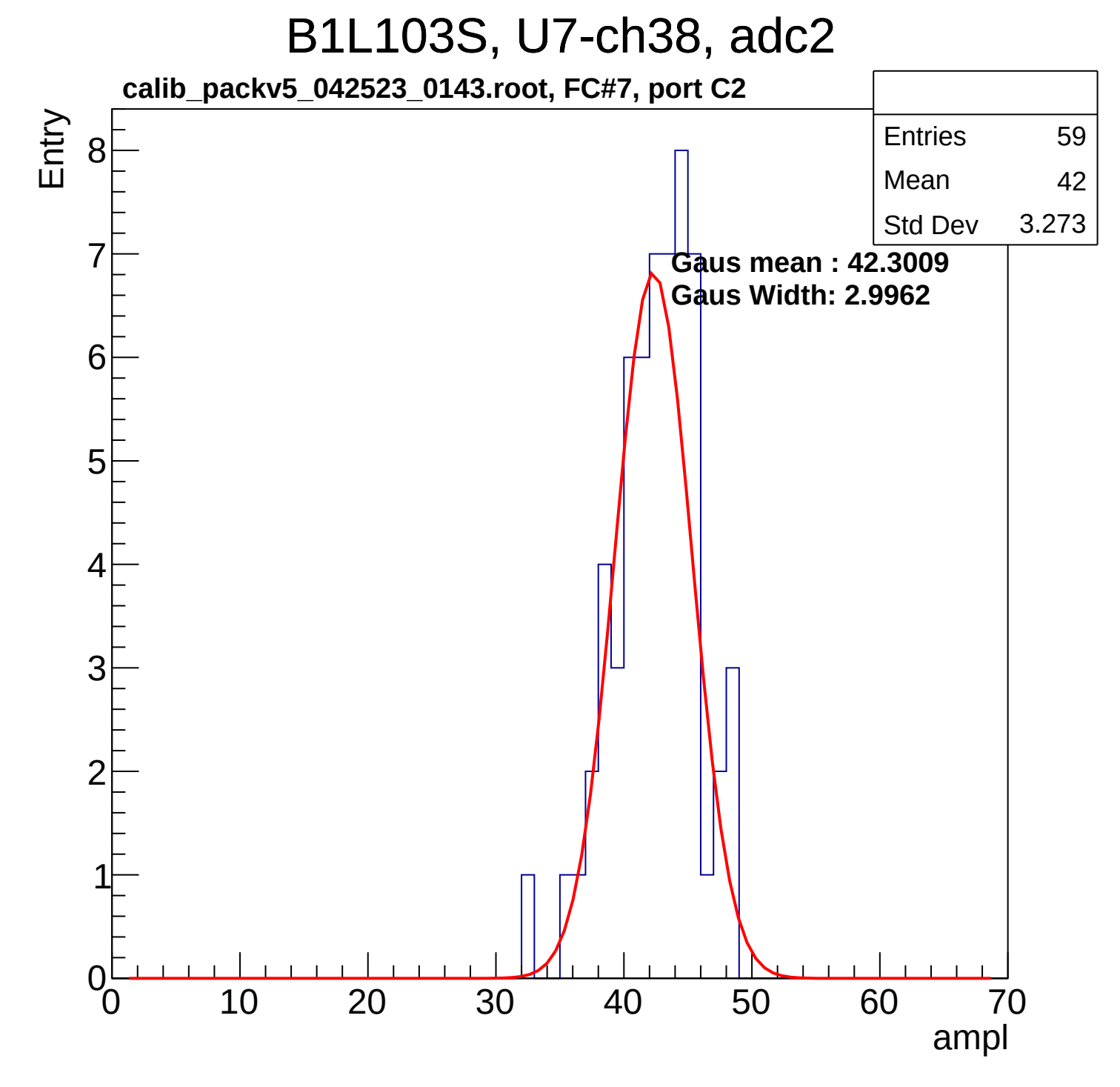
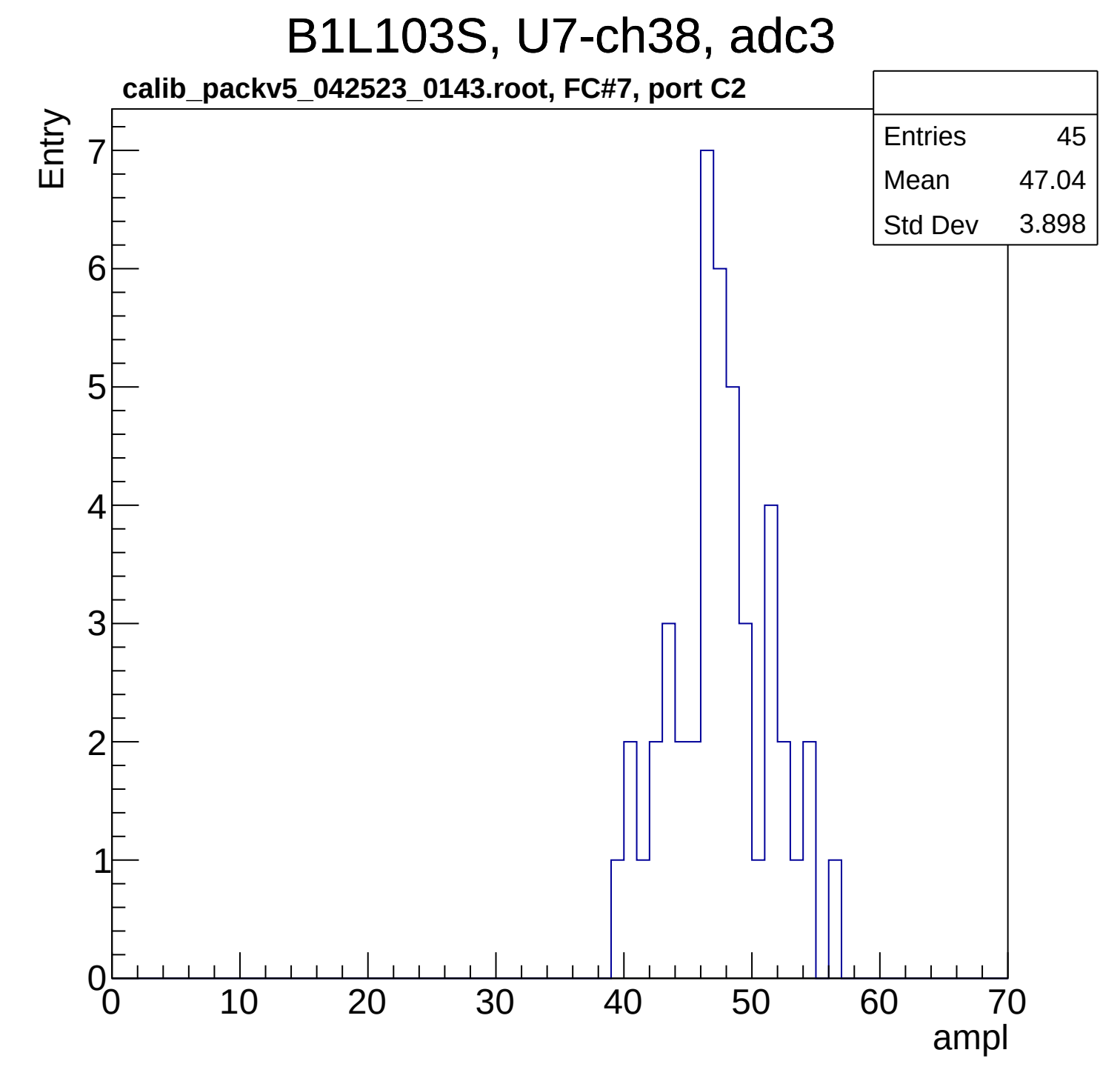
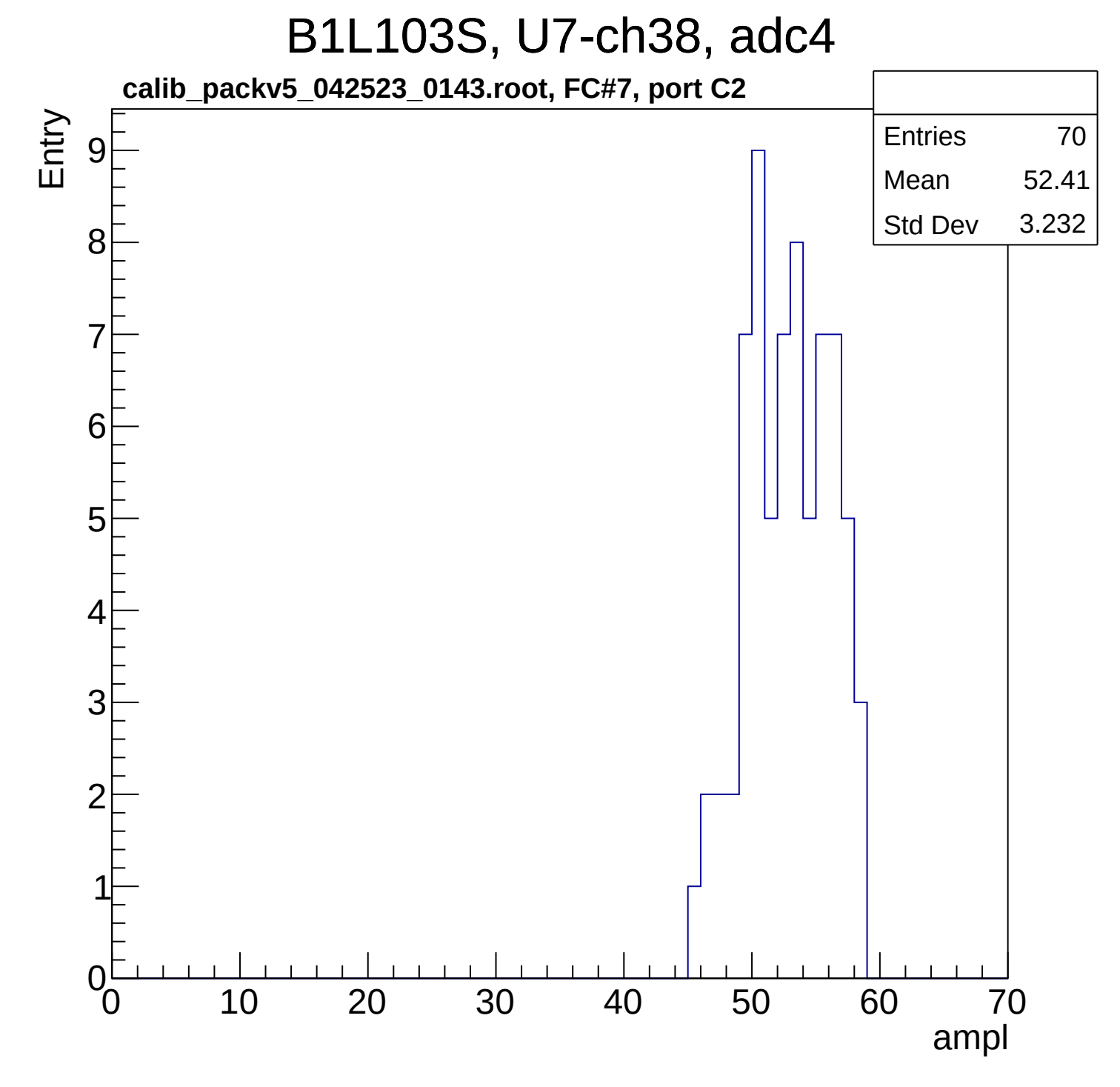

B1L103S, U7-ch37, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

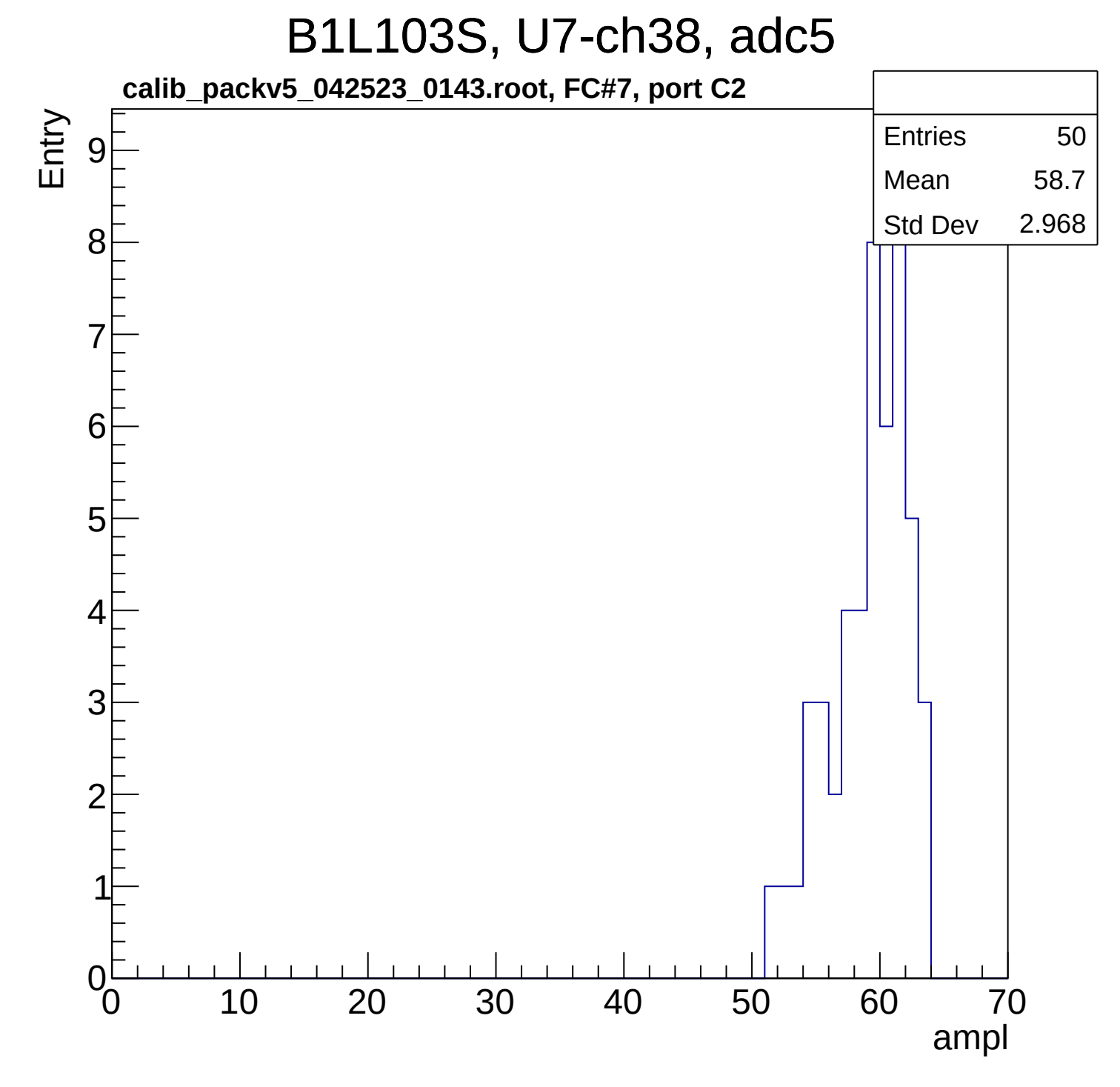

B1L103S, U7-ch38, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 84
Mean 27.48
Std Dev 4.497
Gaus mean : 28.7724
Gaus Width: 3.7312
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

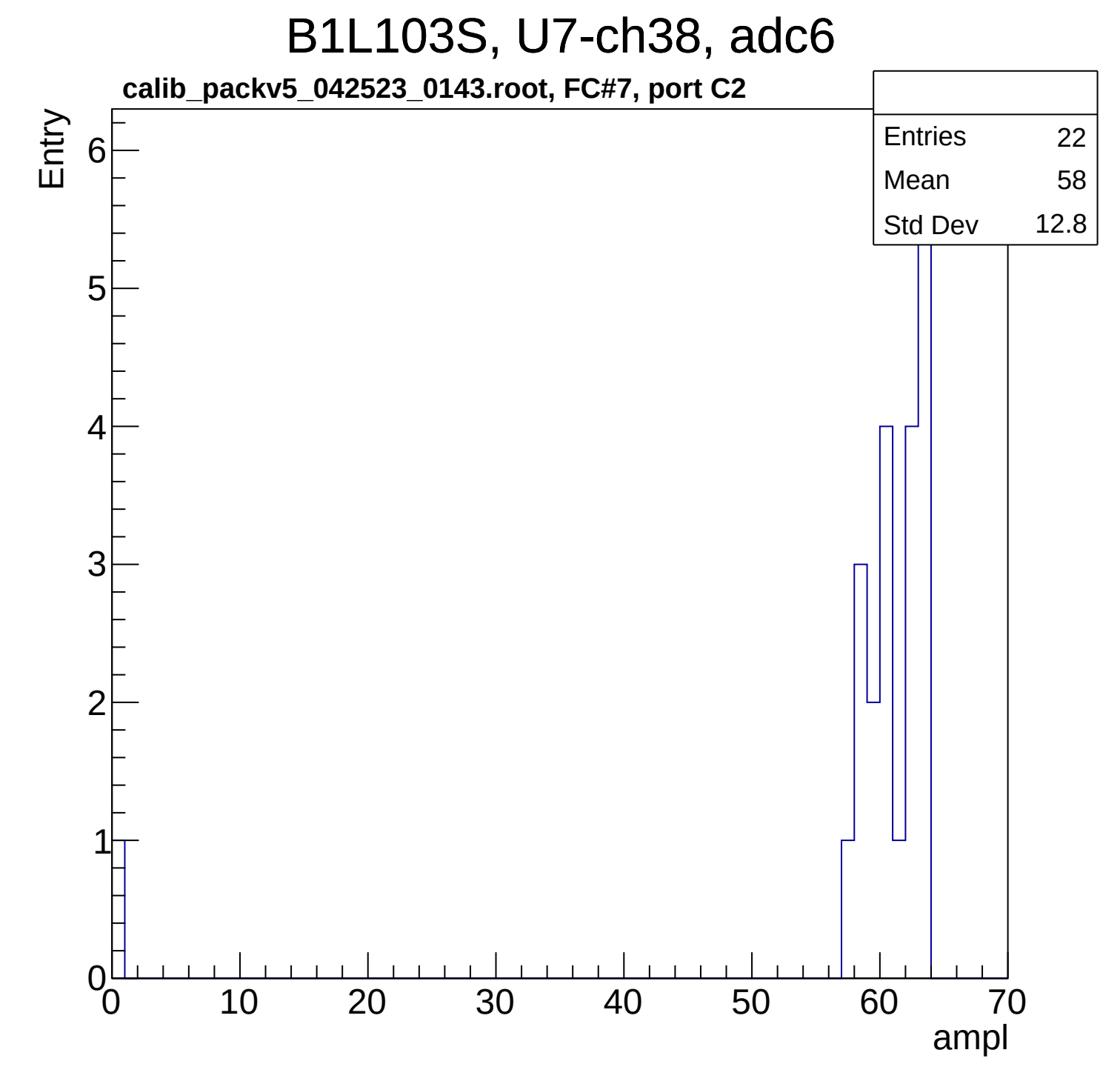

B1L103S, U7-ch38, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 35.39
Std Dev 3.112
Gaus mean : 36.0345
Gaus Width: 3.1906
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

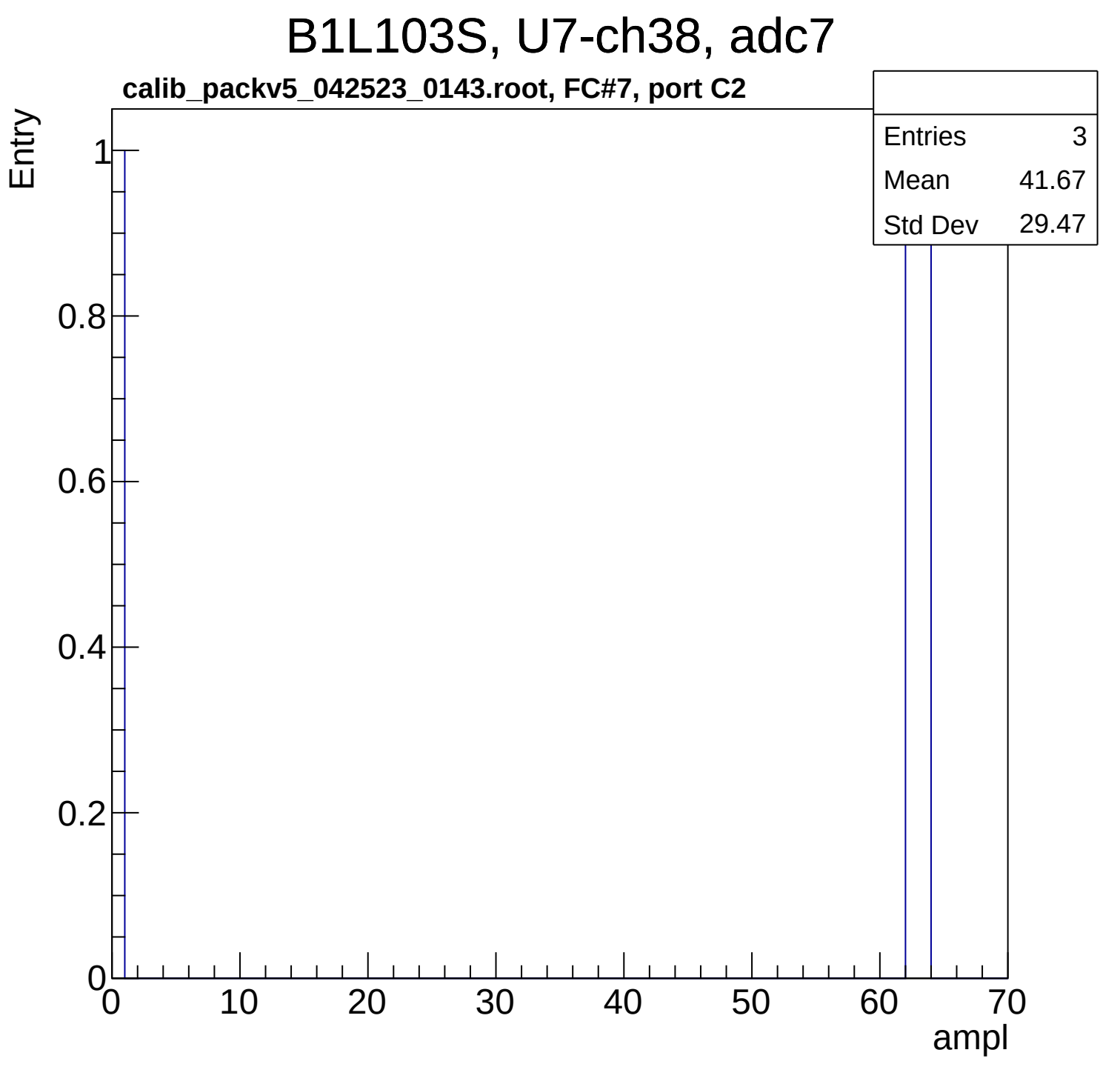

B1L103S, U7-ch38, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 42
Std Dev 3.273
Gaus mean : 42.3009
Gaus Width: 2.9962
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

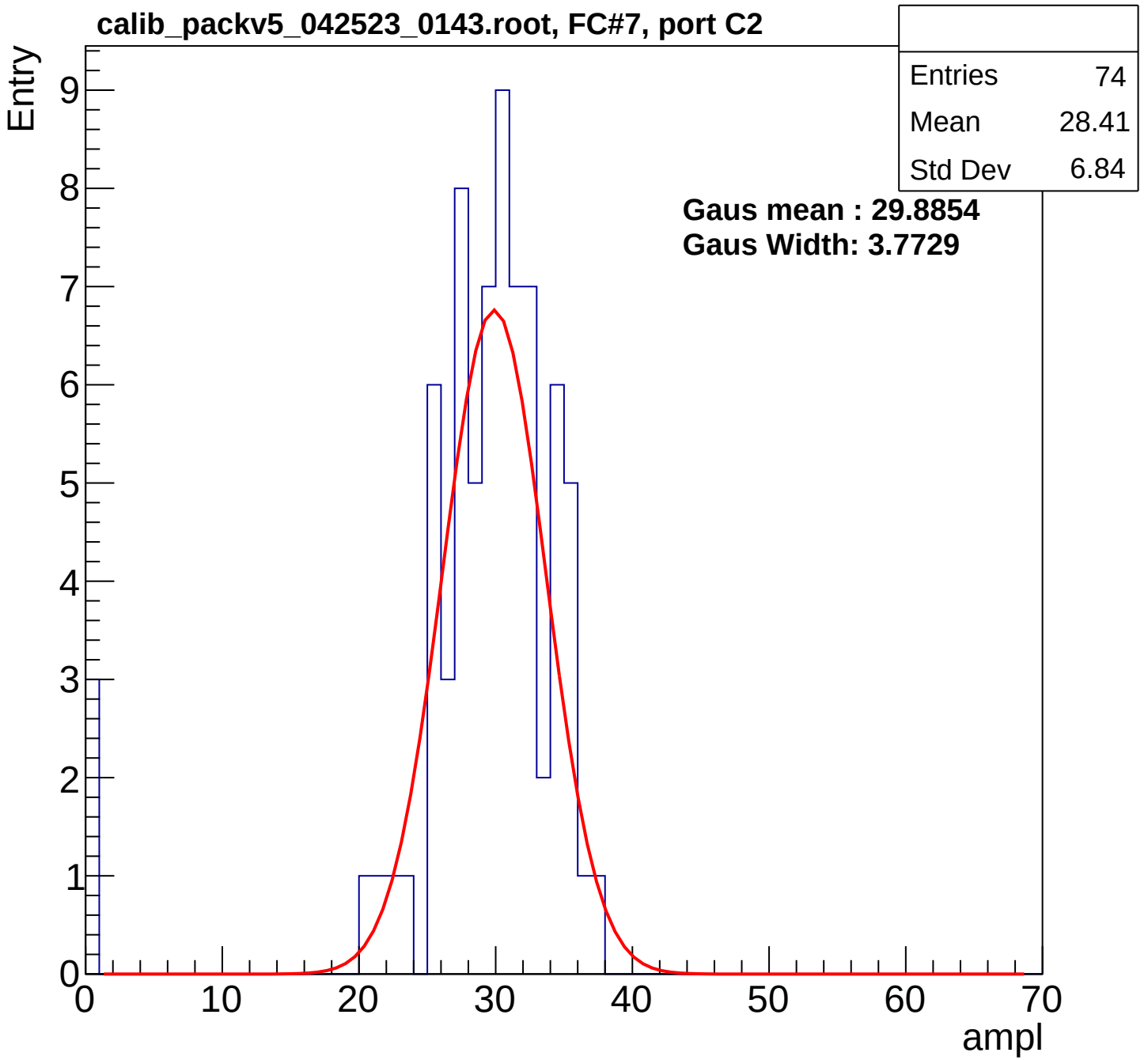

B1L103S, U7-ch38, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 45
Mean 47.04
Std Dev 3.898
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

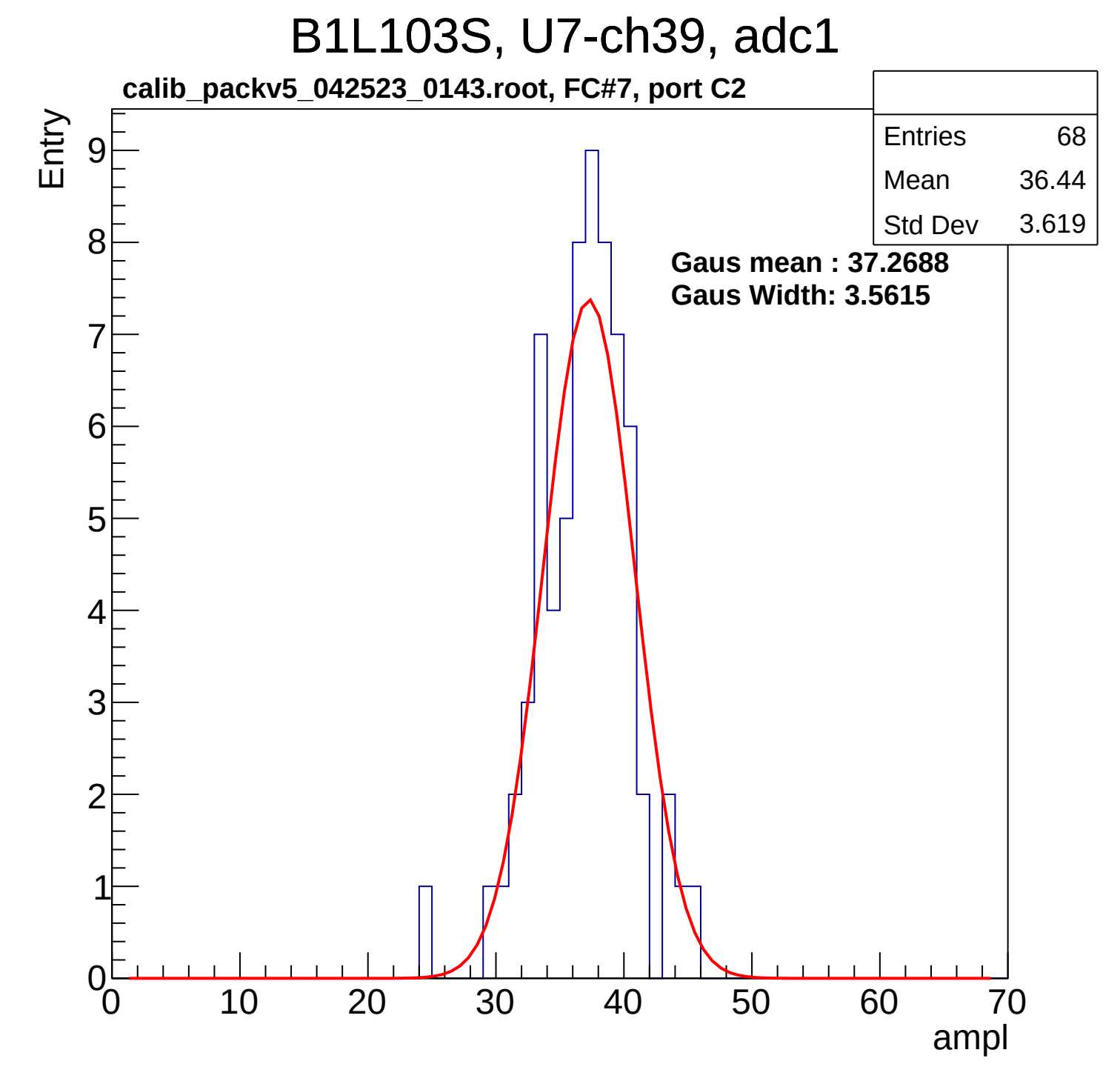

B1L103S, U7-ch38, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 52.41
Std Dev 3.232
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

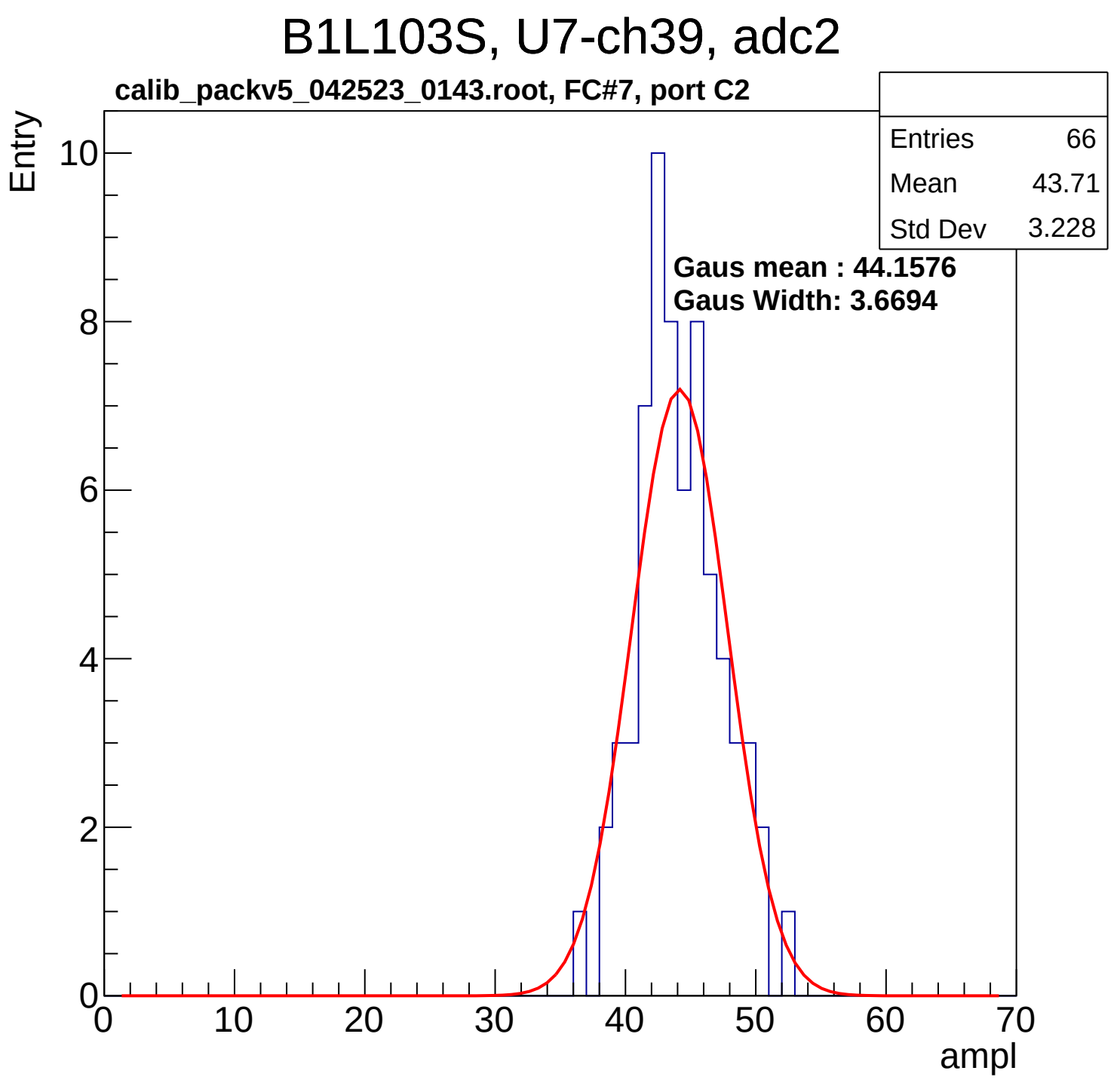

B1L103S, U7-ch38, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 50
Mean 58.7
Std Dev 2.968
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

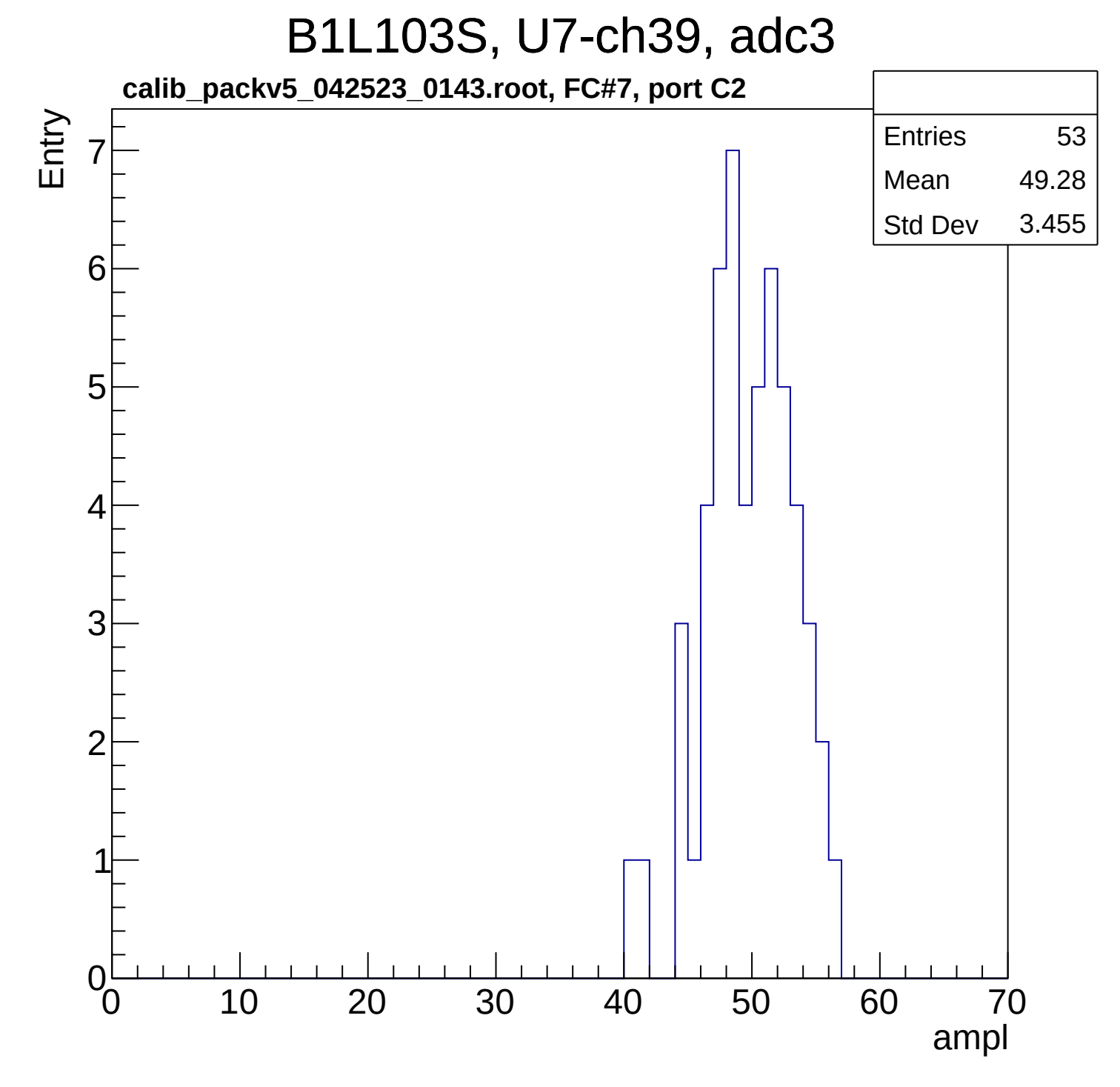

B1L103S, U7-ch38, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 22
Mean 58
Std Dev 12.8
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch38, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 41.67
Std Dev 29.47
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch39, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 74
Mean 28.41
Std Dev 6.84
Gaus mean : 29.8854
Gaus Width: 3.7729
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch39, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 36.44
Std Dev 3.619
Gaus mean : 37.2688
Gaus Width: 3.5615
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch39, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 43.71
Std Dev 3.228
Gaus mean : 44.1576
Gaus Width: 3.6694
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch39, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 49.28
Std Dev 3.455
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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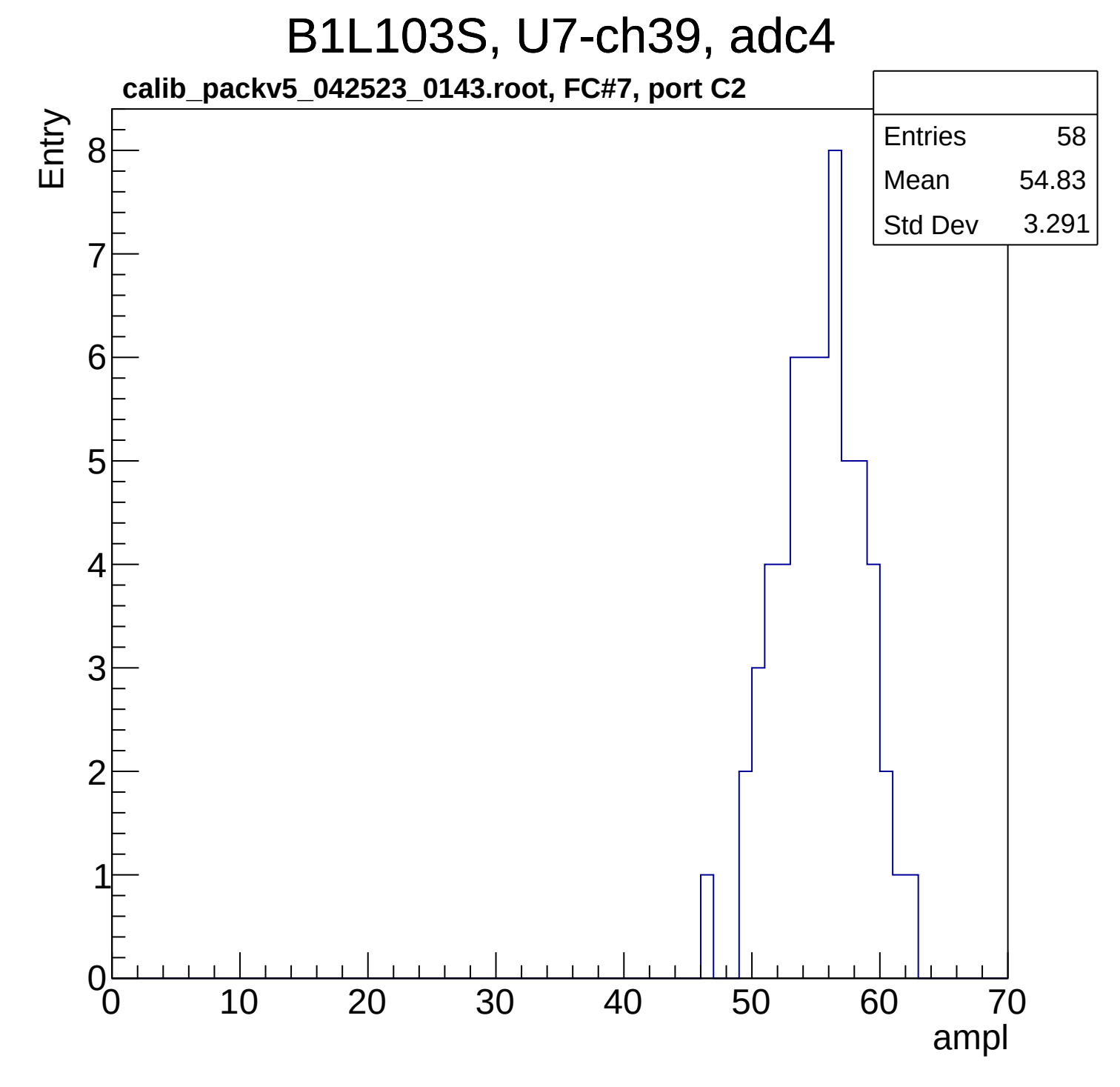
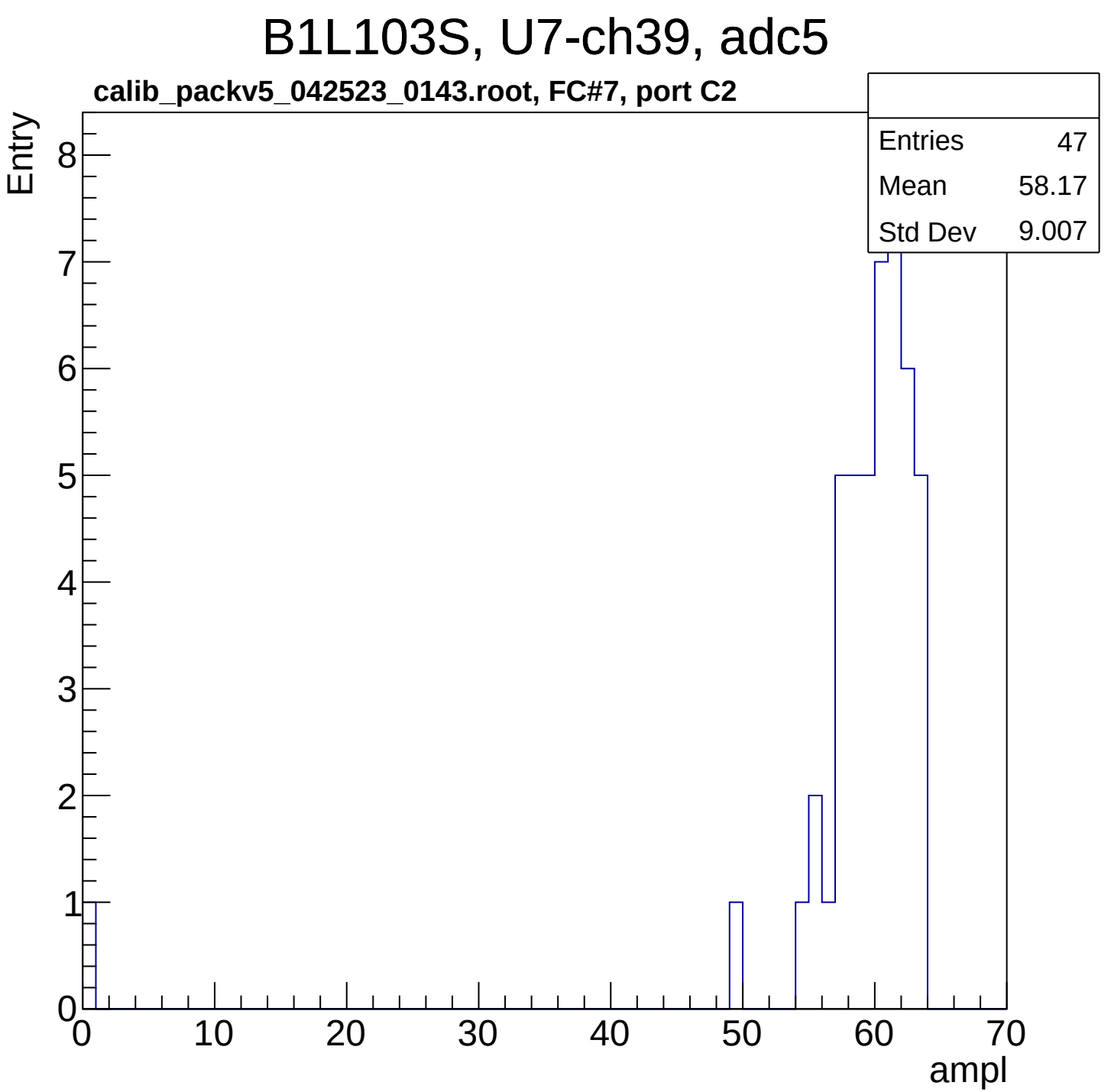
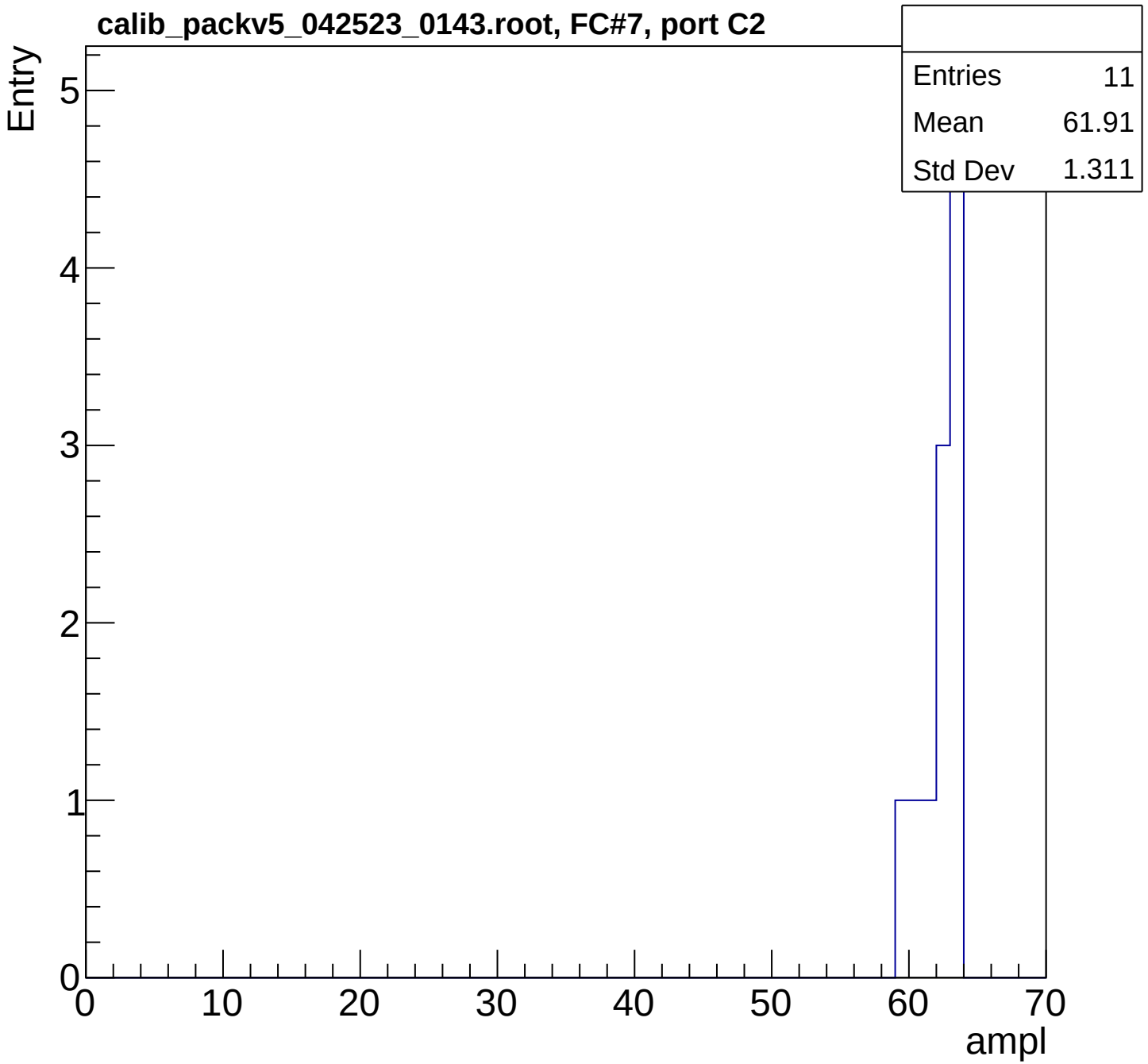
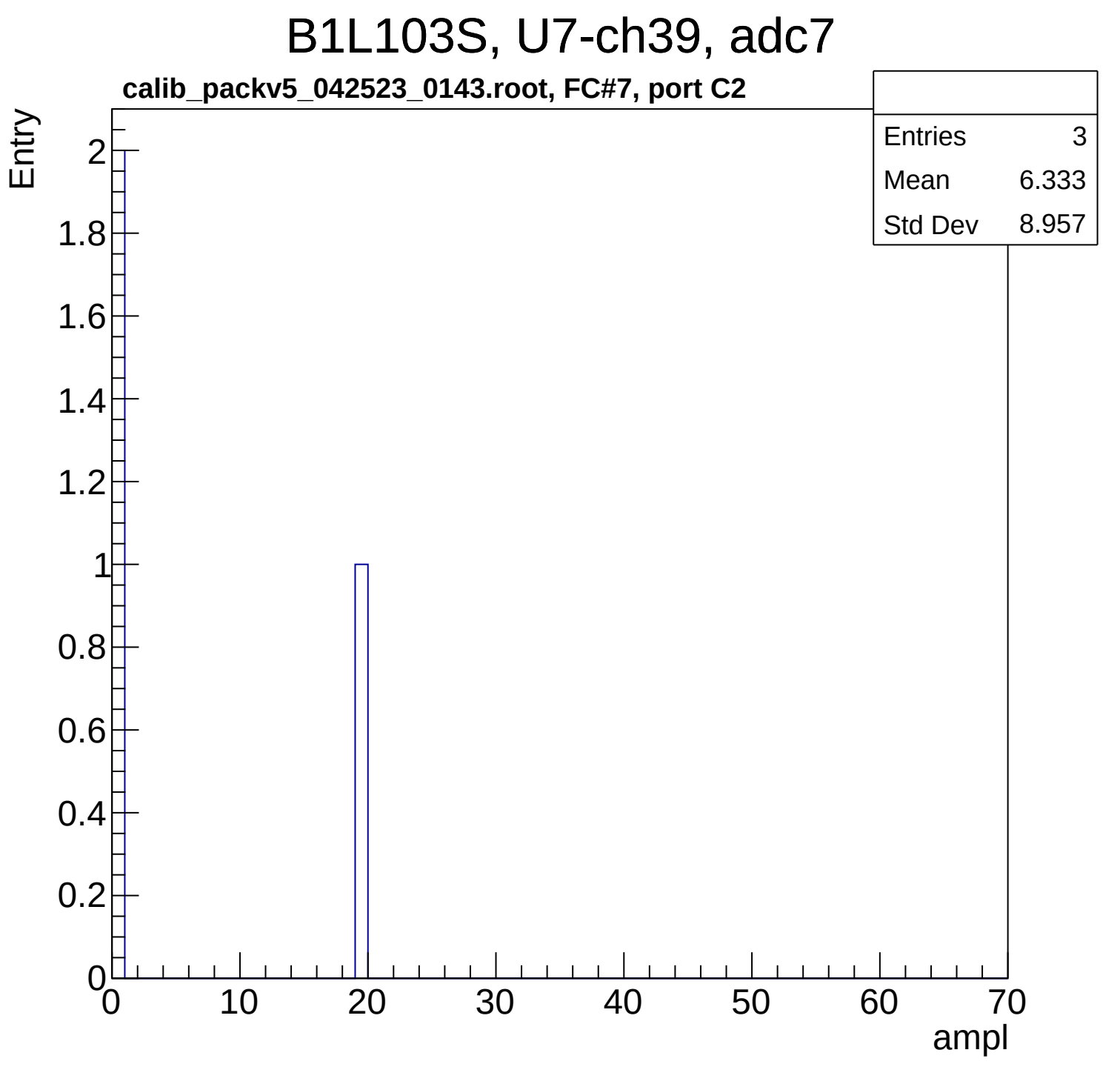
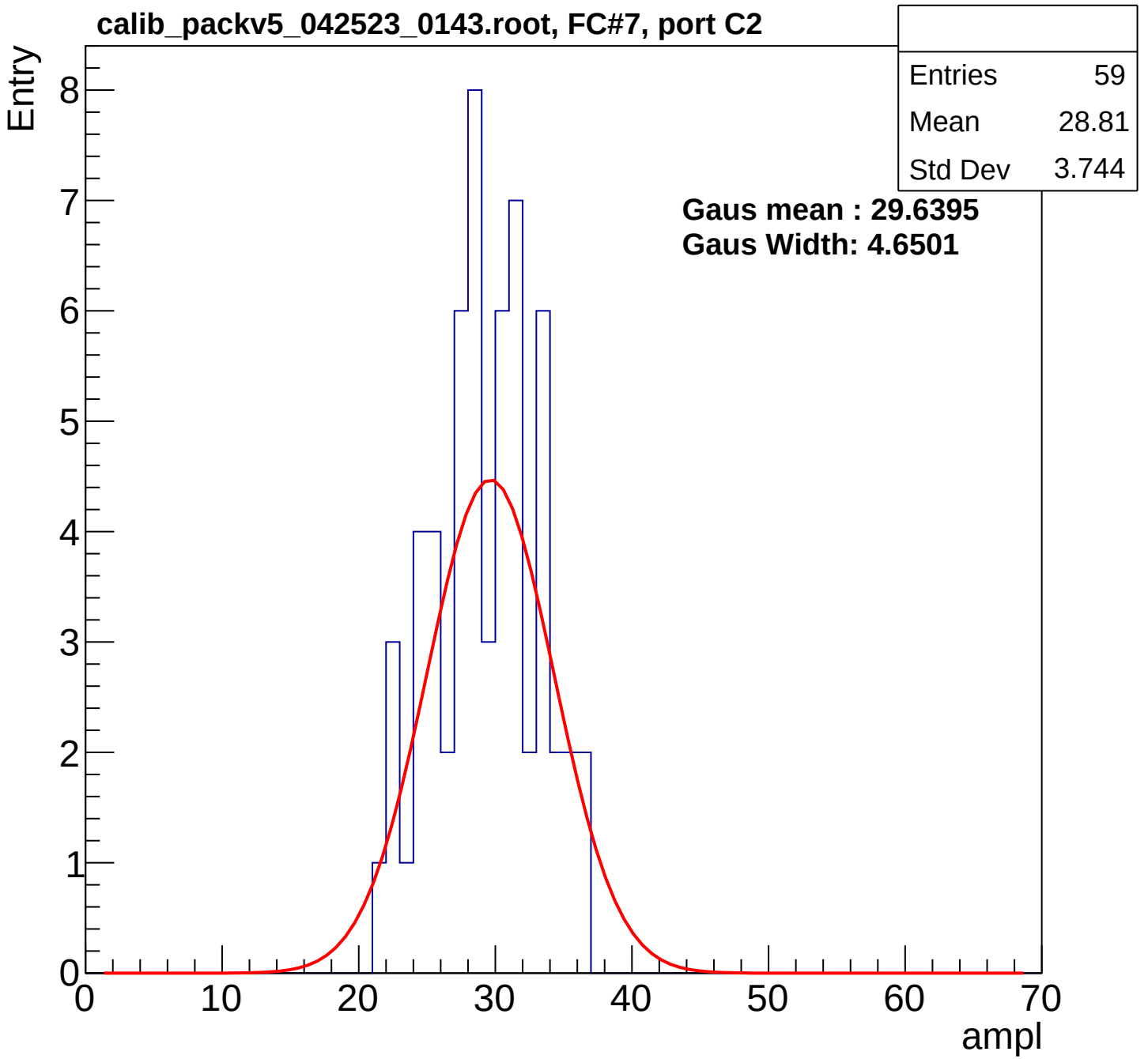

B1L103S, U7-ch39, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 58
Mean 54.83
Std Dev 3.291
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch39, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 47
Mean 58.17
Std Dev 9.007
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch39, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 11
Mean 61.91
Std Dev 1.311
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch39, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 6.333
Std Dev 8.957
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U7-ch40, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 28.81
Std Dev 3.744
Gaus mean : 29.6395
Gaus Width: 4.6501
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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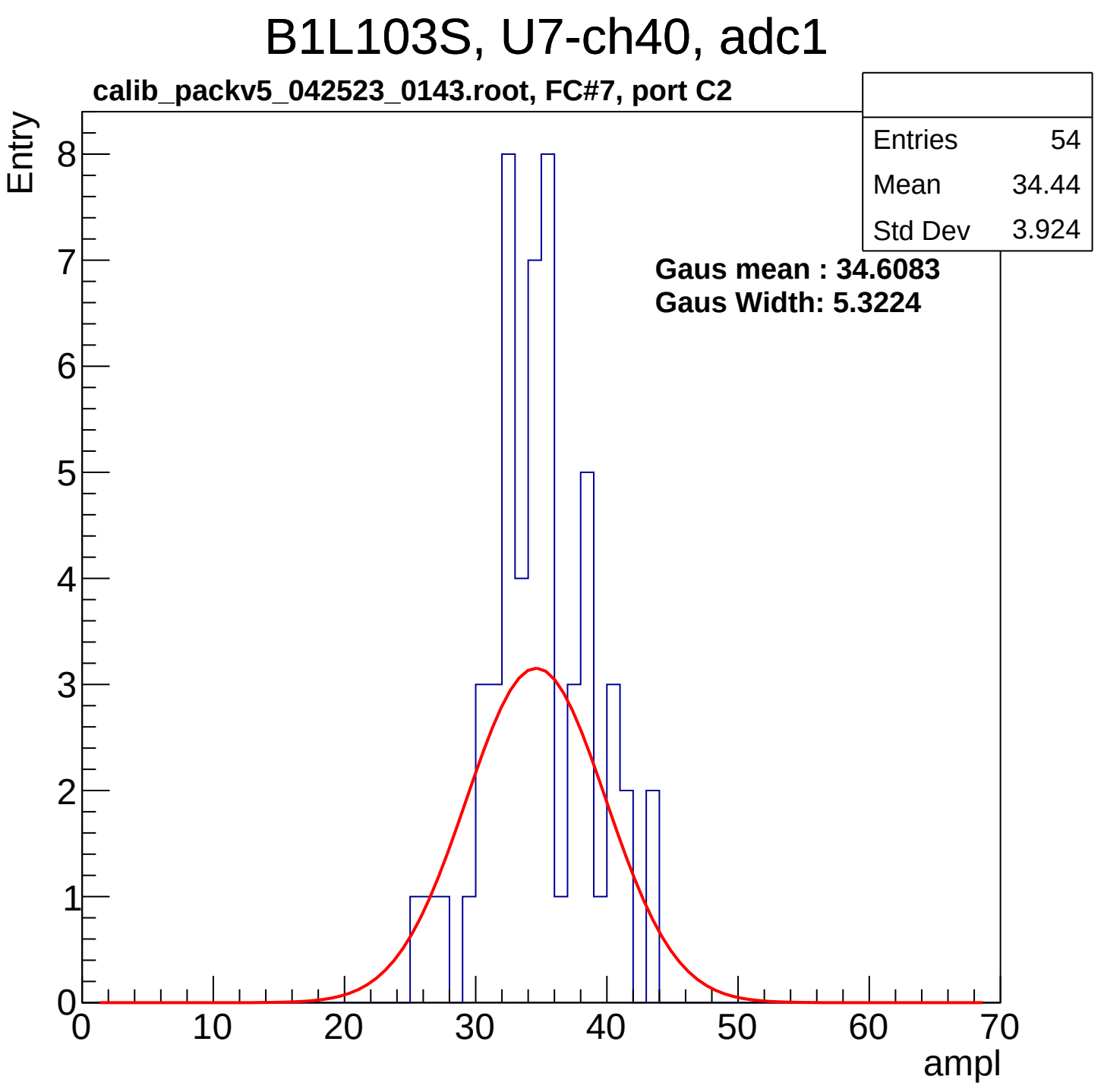
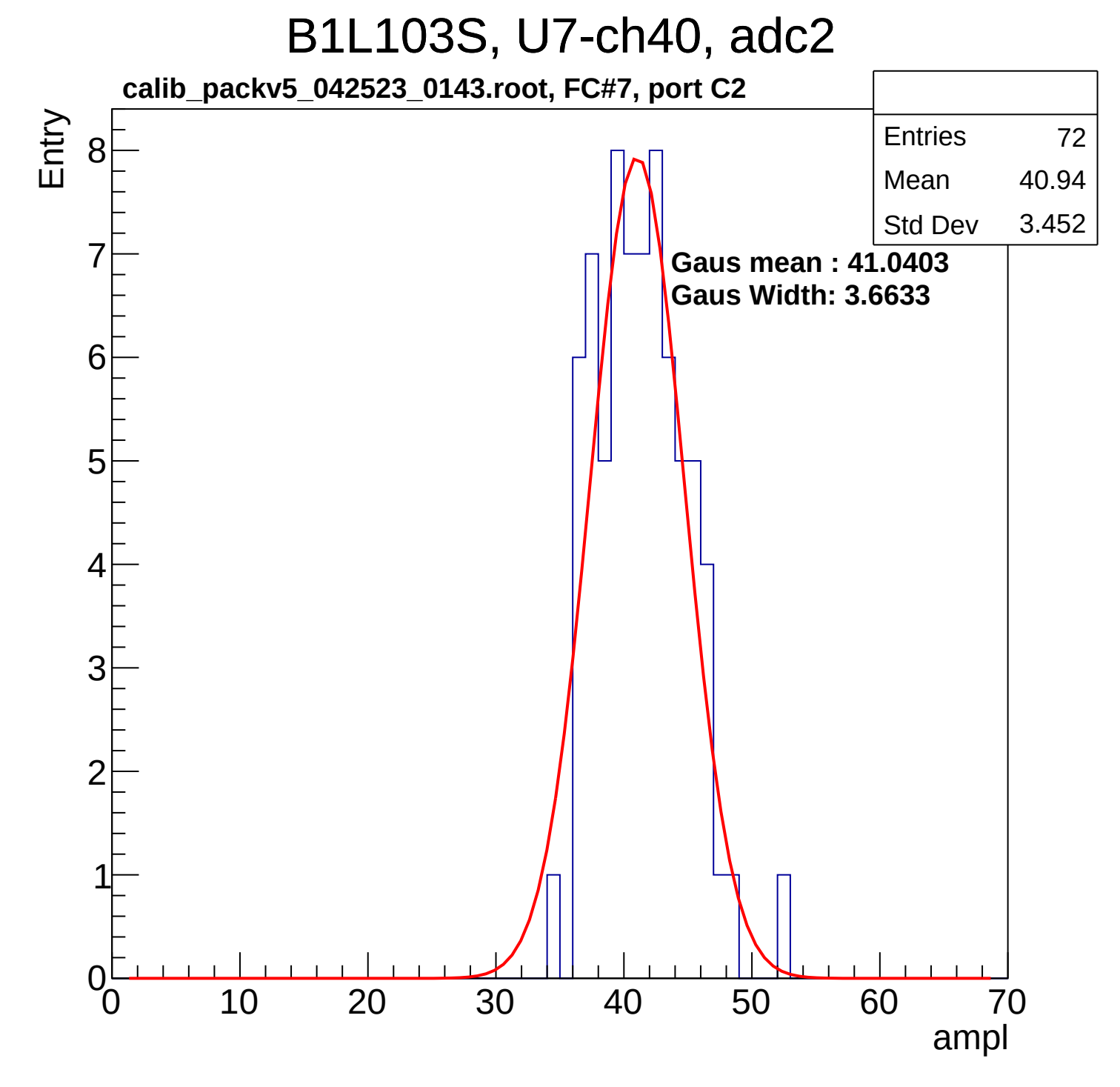
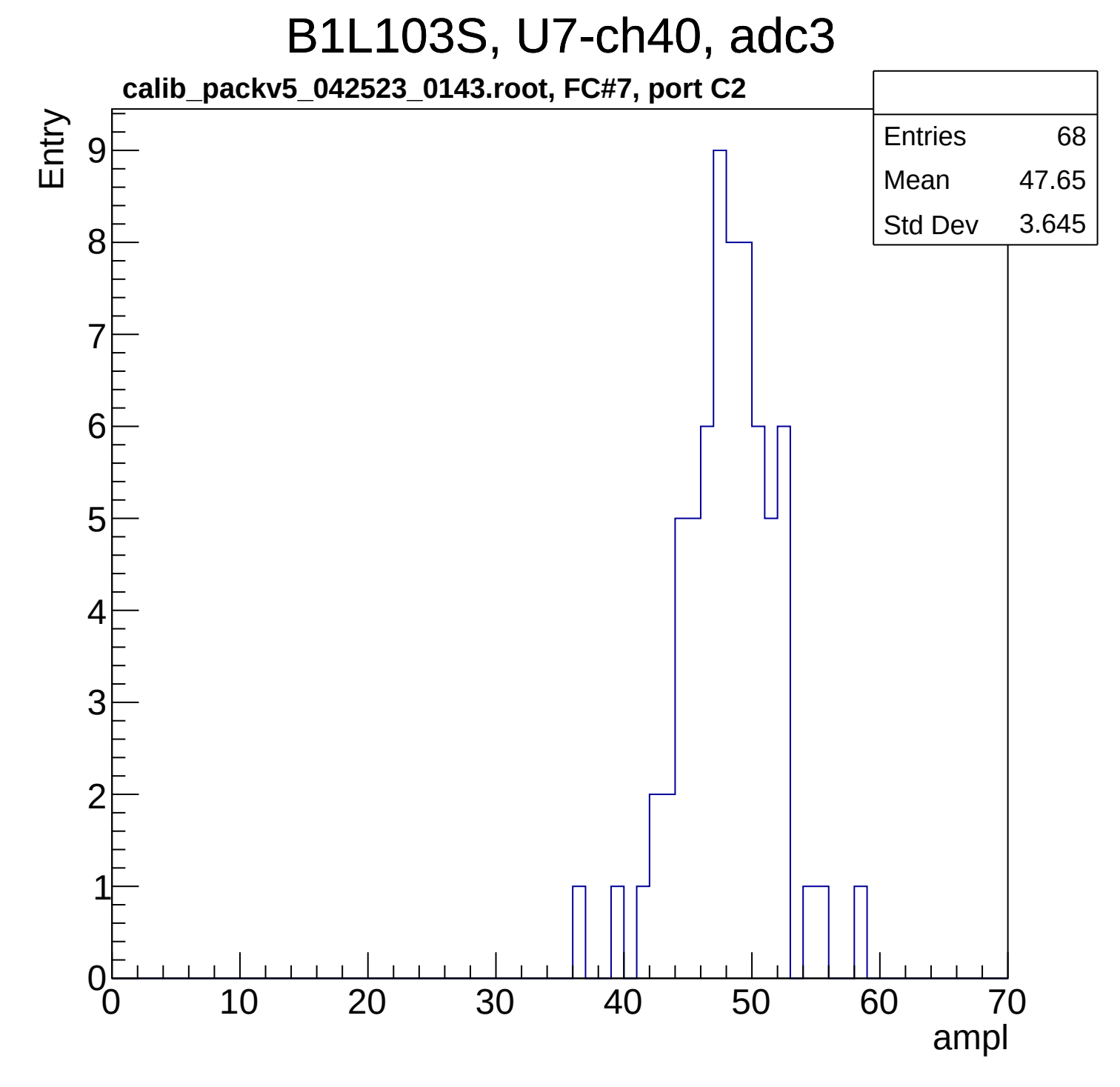
20
30
40
50
60
70


B1L103S, U7-ch40, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 54
Mean 34.44
Std Dev 3.924
Gaus mean : 34.6083
Gaus Width: 5.3224
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch40, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 72
Mean 40.94
Std Dev 3.452
Gaus mean : 41.0403
Gaus Width: 3.6633
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch40, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 47.65
Std Dev 3.645
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
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40
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60
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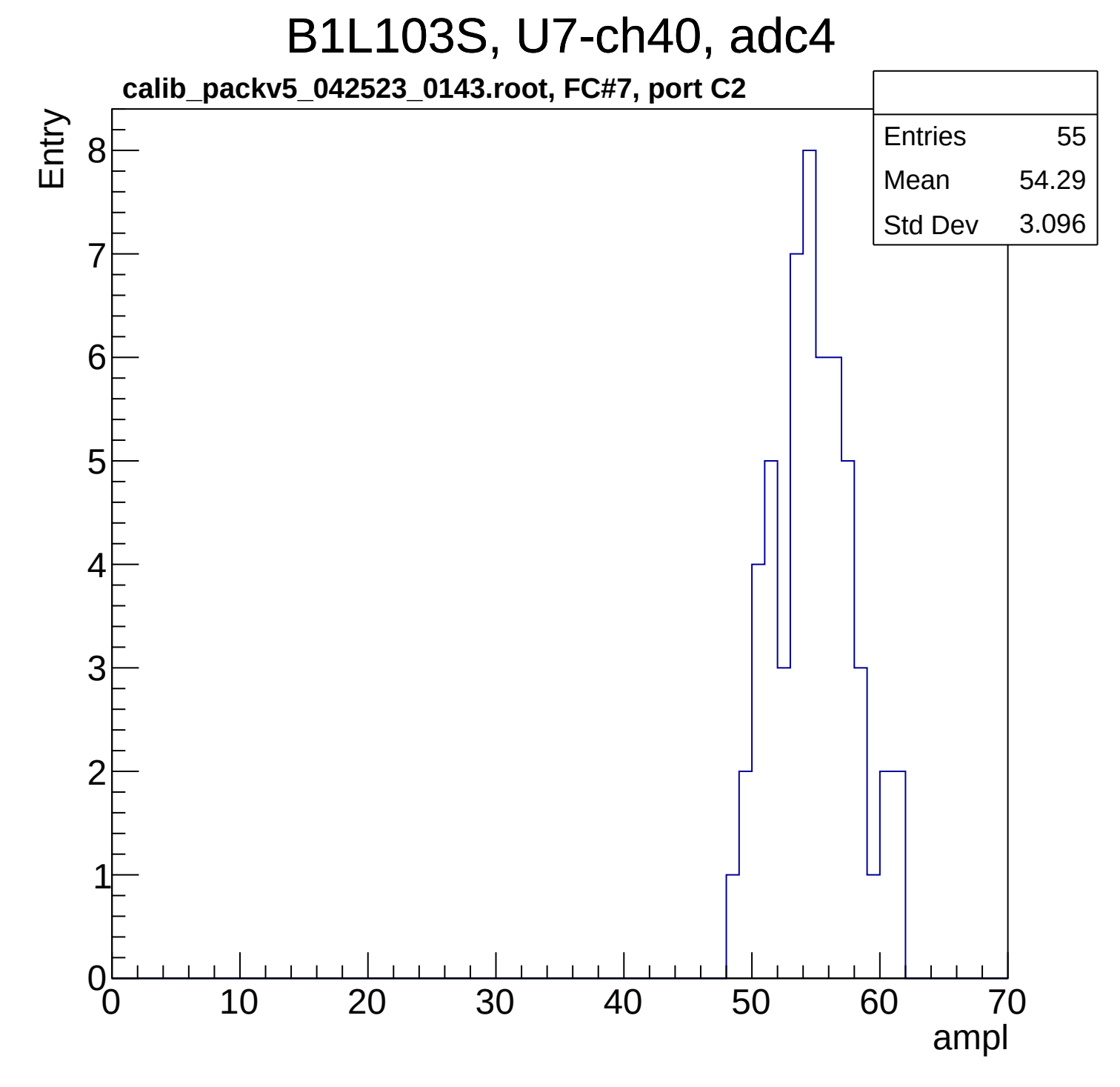
B1L103S, U7-ch40, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 54.29
Std Dev 3.096
Entry
ampl
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1
2
3
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5
6
7
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0
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60
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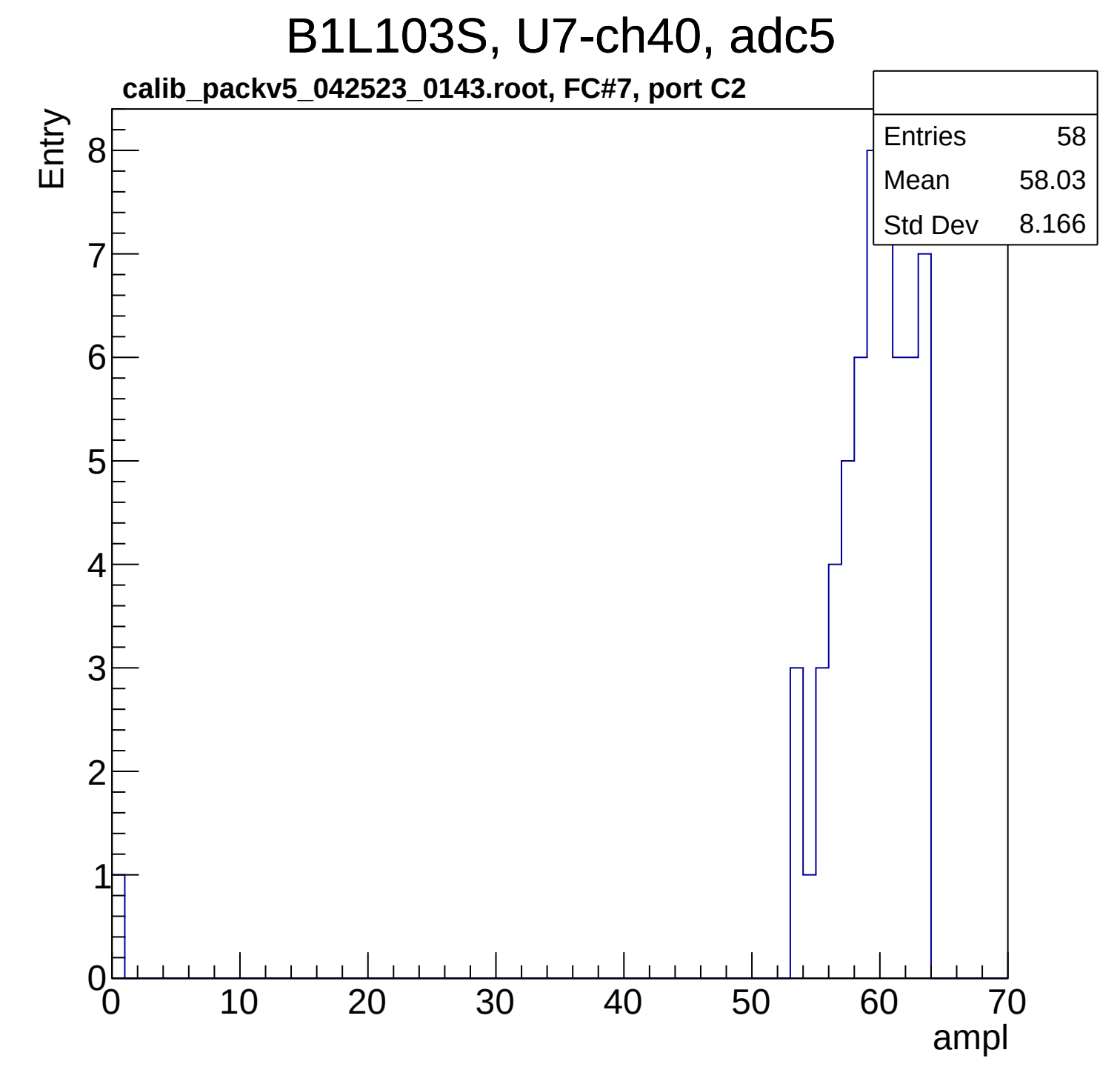
B1L103S, U7-ch40, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 58
Mean 58.03
Std Dev 8.166
Entry
ampl
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2
3
4
5
6
7
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0
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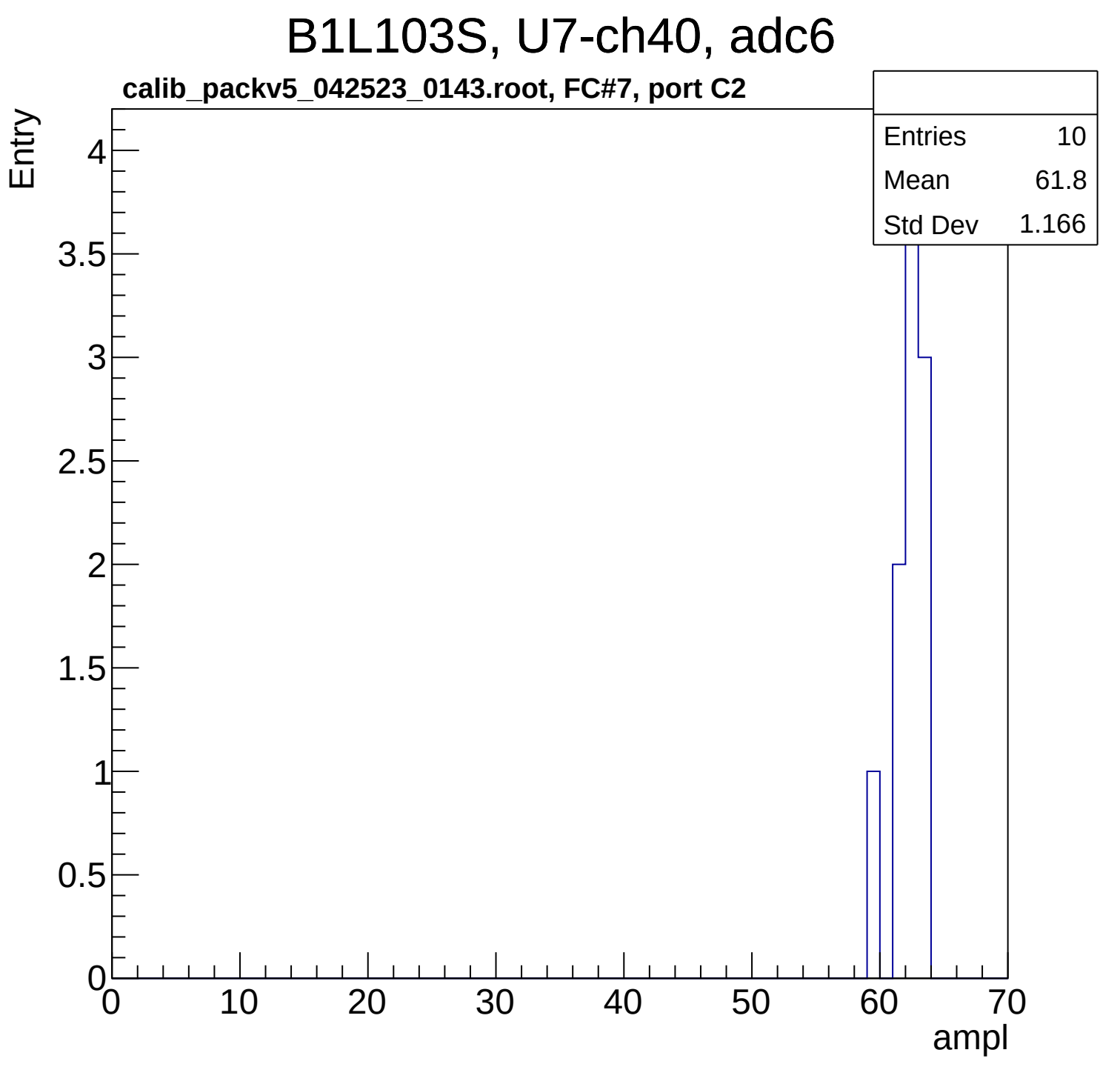
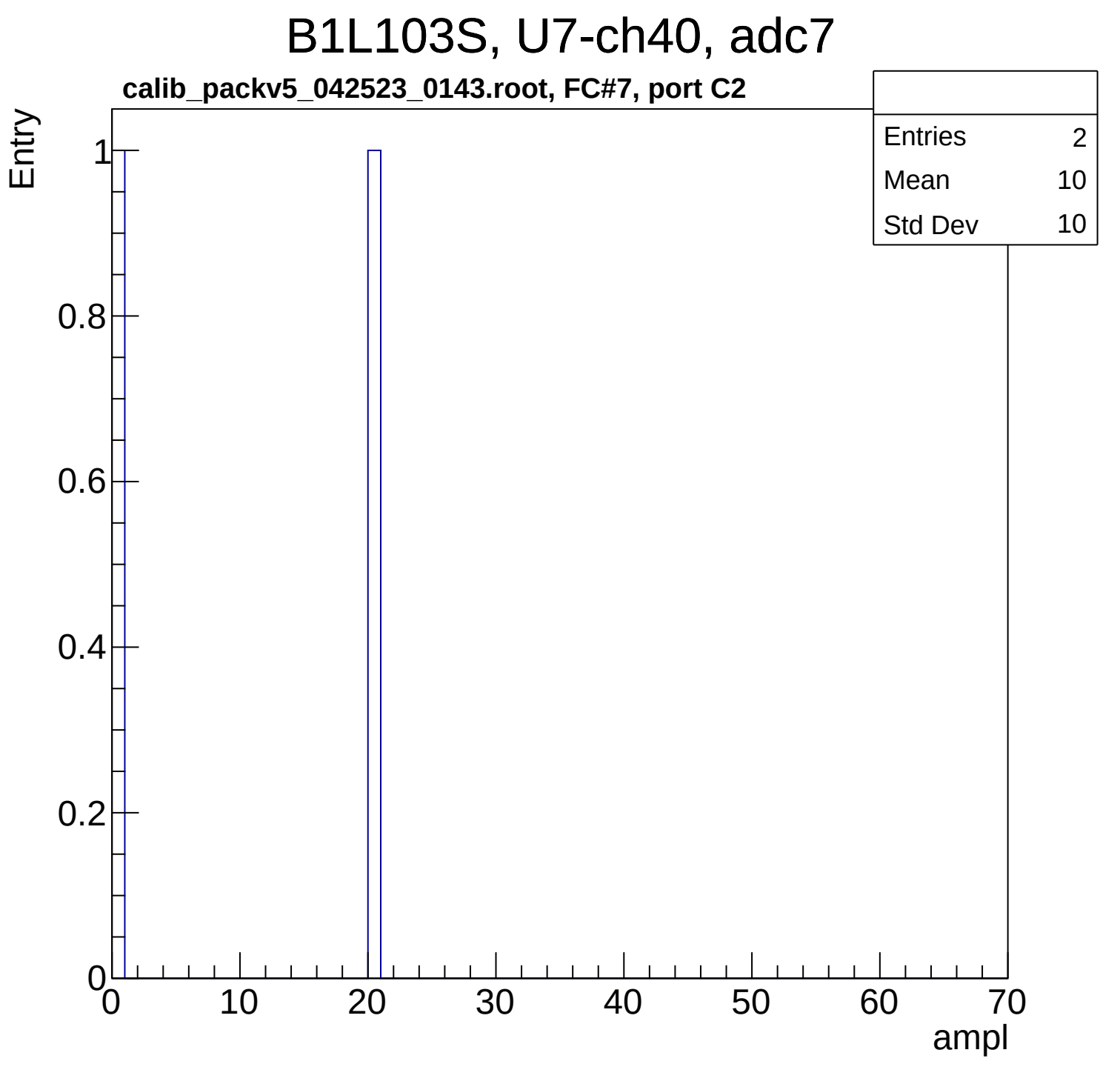

B1L103S, U7-ch40, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 10
Mean 61.8
Std Dev 1.166
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U7-ch40, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 10
Std Dev 10
Entry
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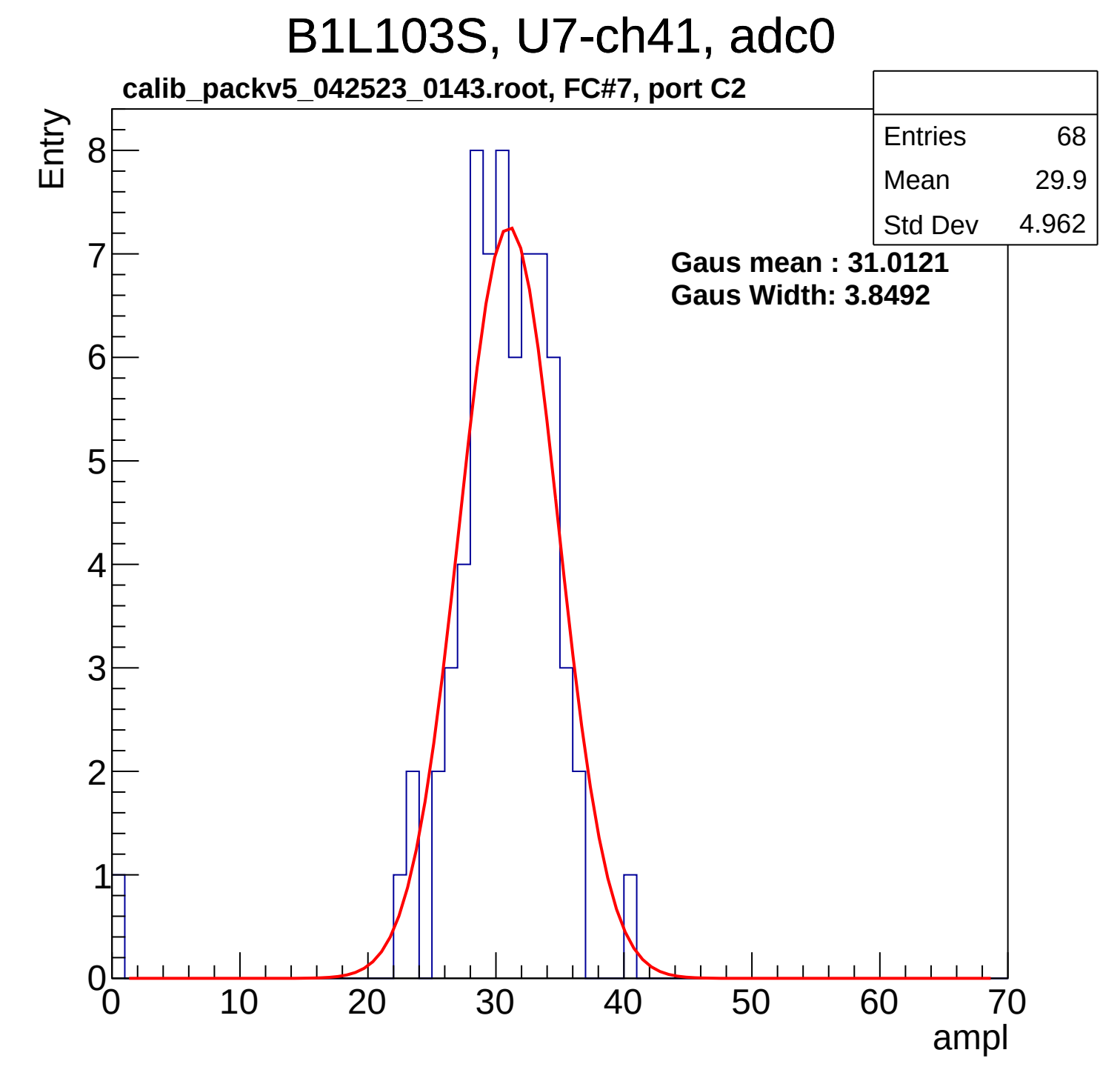
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch41, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 29.9
Std Dev 4.962
Gaus mean : 31.0121
Gaus Width: 3.8492
Entry
ampl
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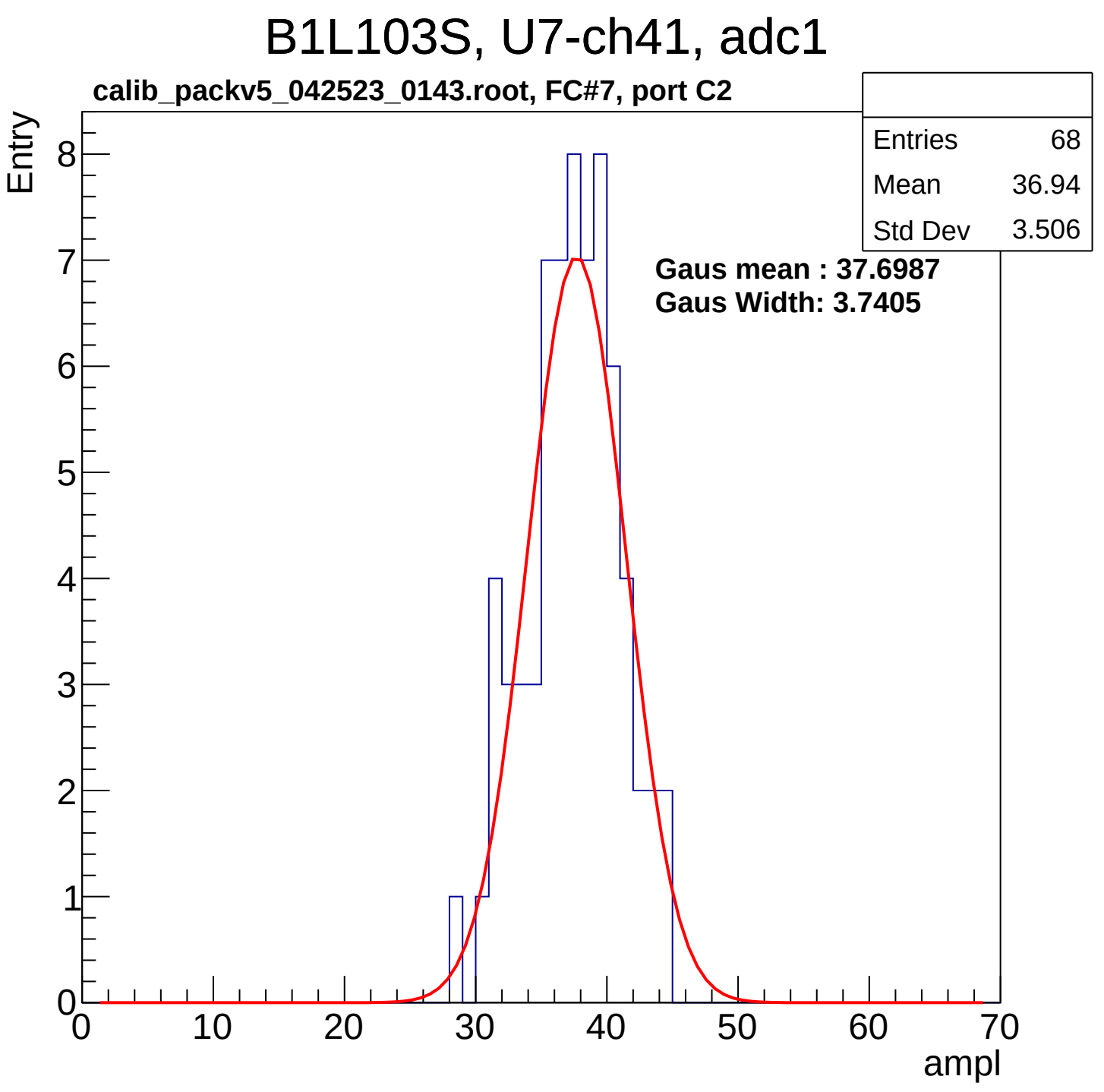
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch41, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 36.94
Std Dev 3.506
Gaus mean : 37.6987
Gaus Width: 3.7405
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
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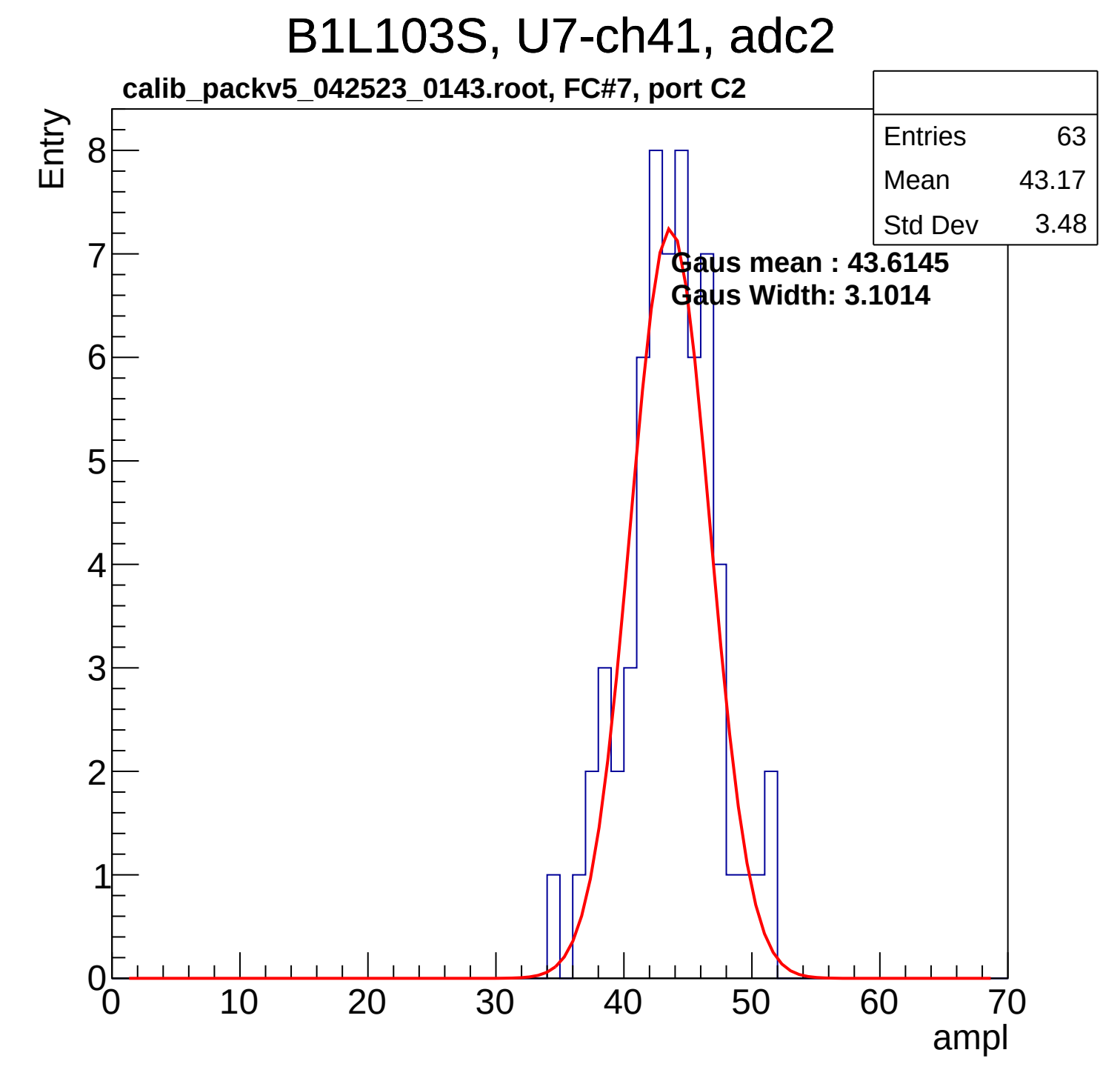
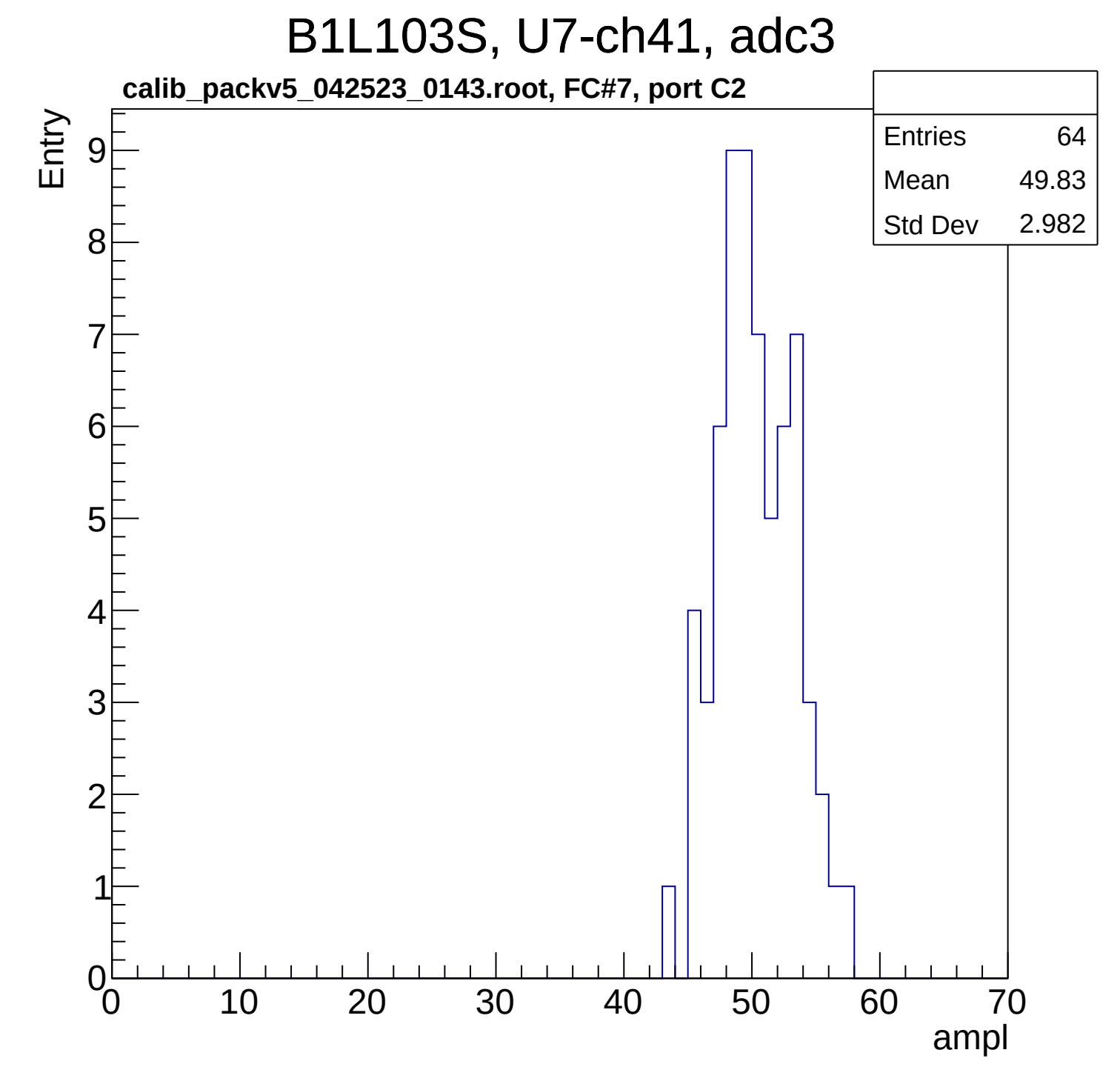
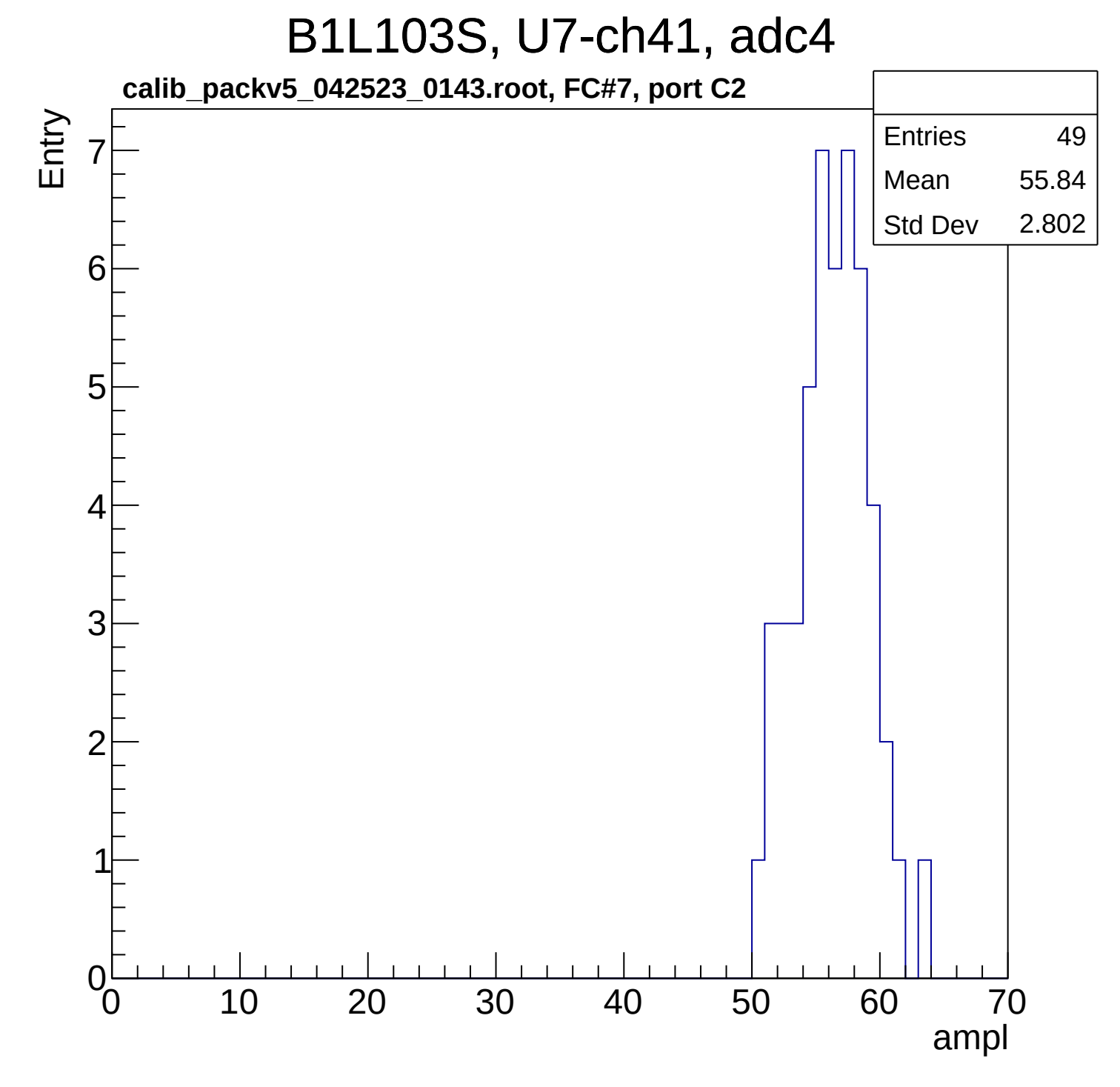

B1L103S, U7-ch41, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 43.17
Std Dev 3.48
Gaus mean : 43.6145
Gaus Width: 3.1014
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch41, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 49.83
Std Dev 2.982
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch41, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 49
Mean 55.84
Std Dev 2.802
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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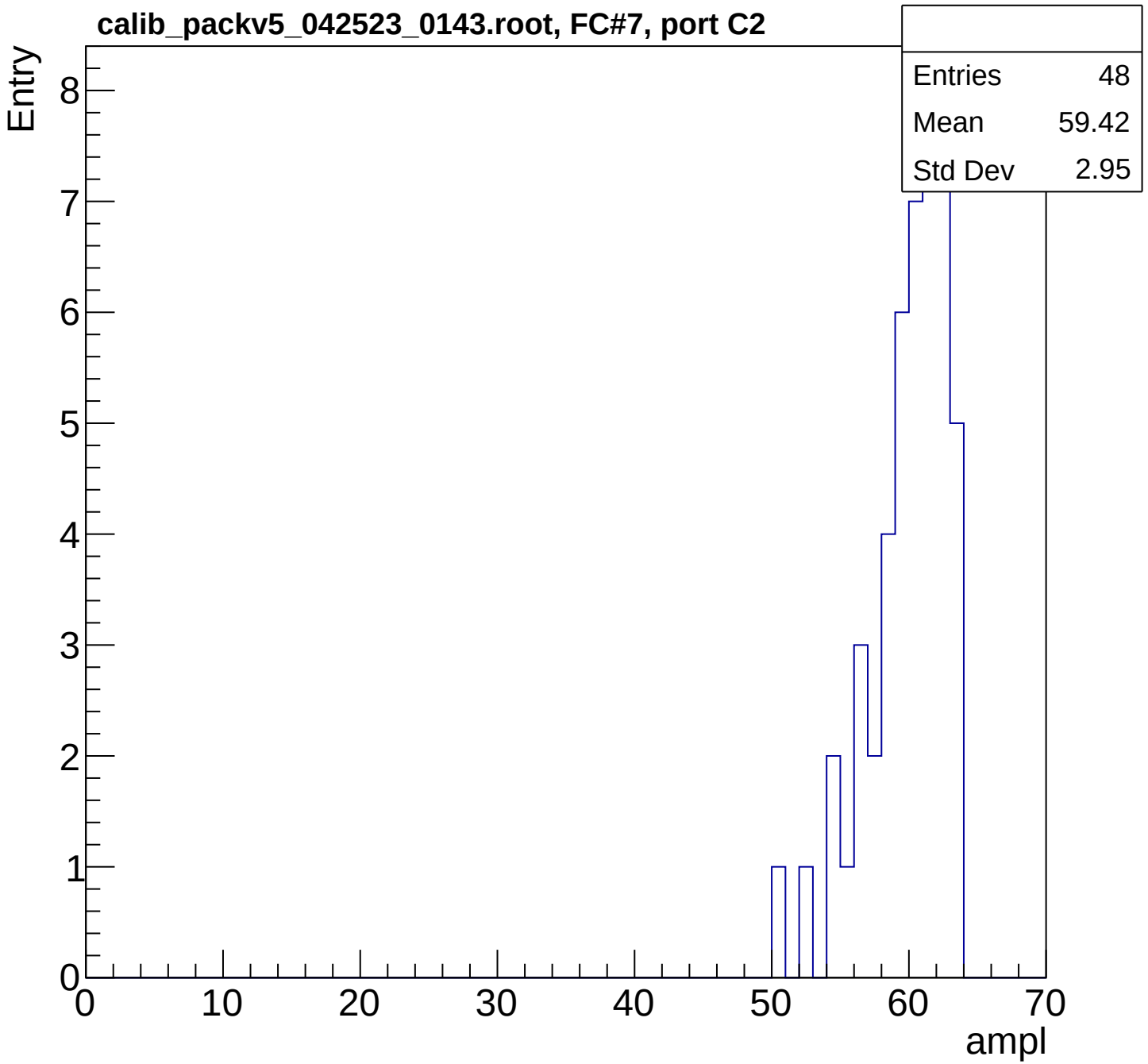
B1L103S, U7-ch41, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 48
Mean 59.42
Std Dev 2.95
Entry
ampl
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1
2
3
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5
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7
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0
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40
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60
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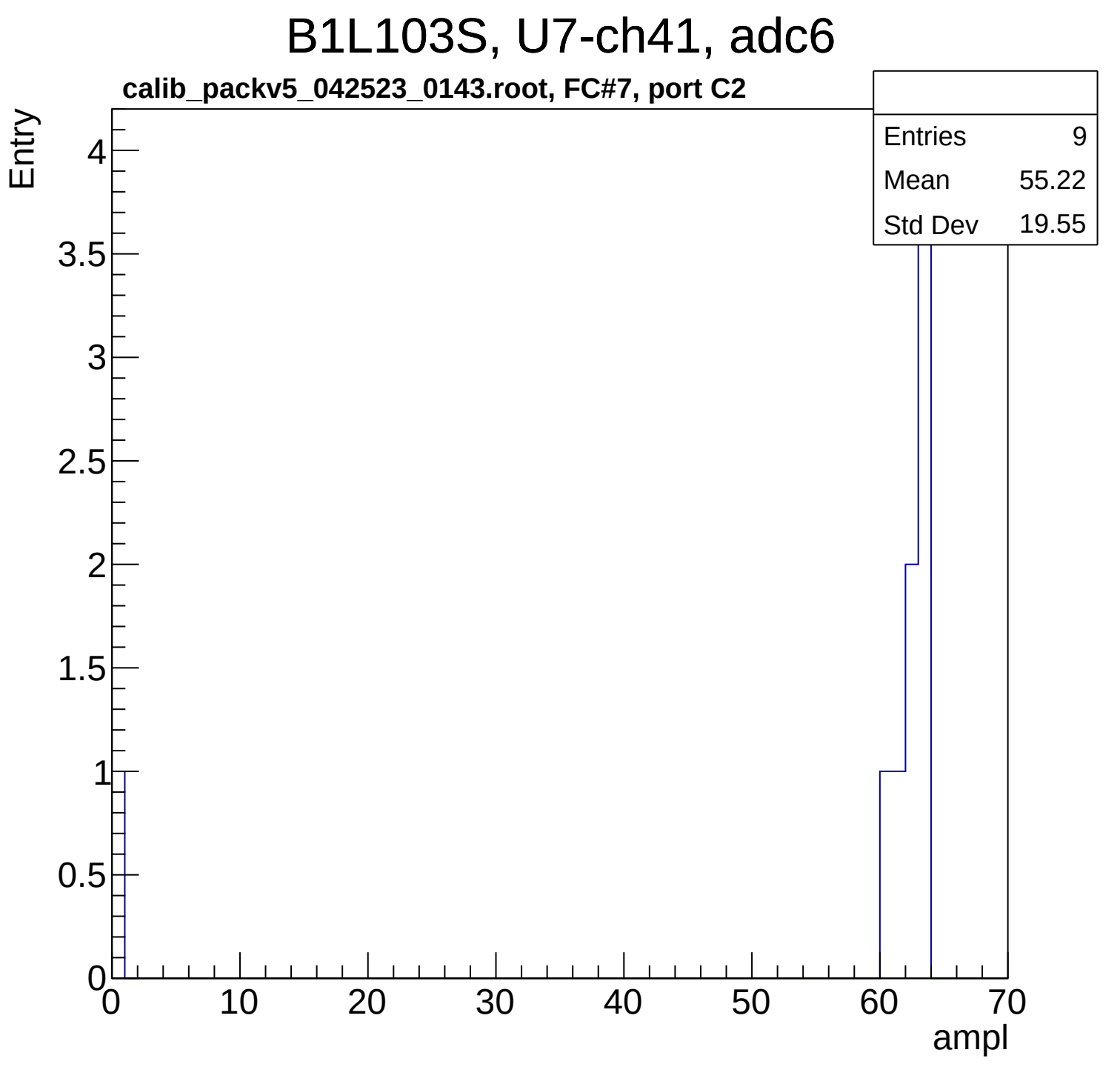
B1L103S, U7-ch41, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 9
Mean 55.22
Std Dev 19.55
Entry
ampl
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0.5
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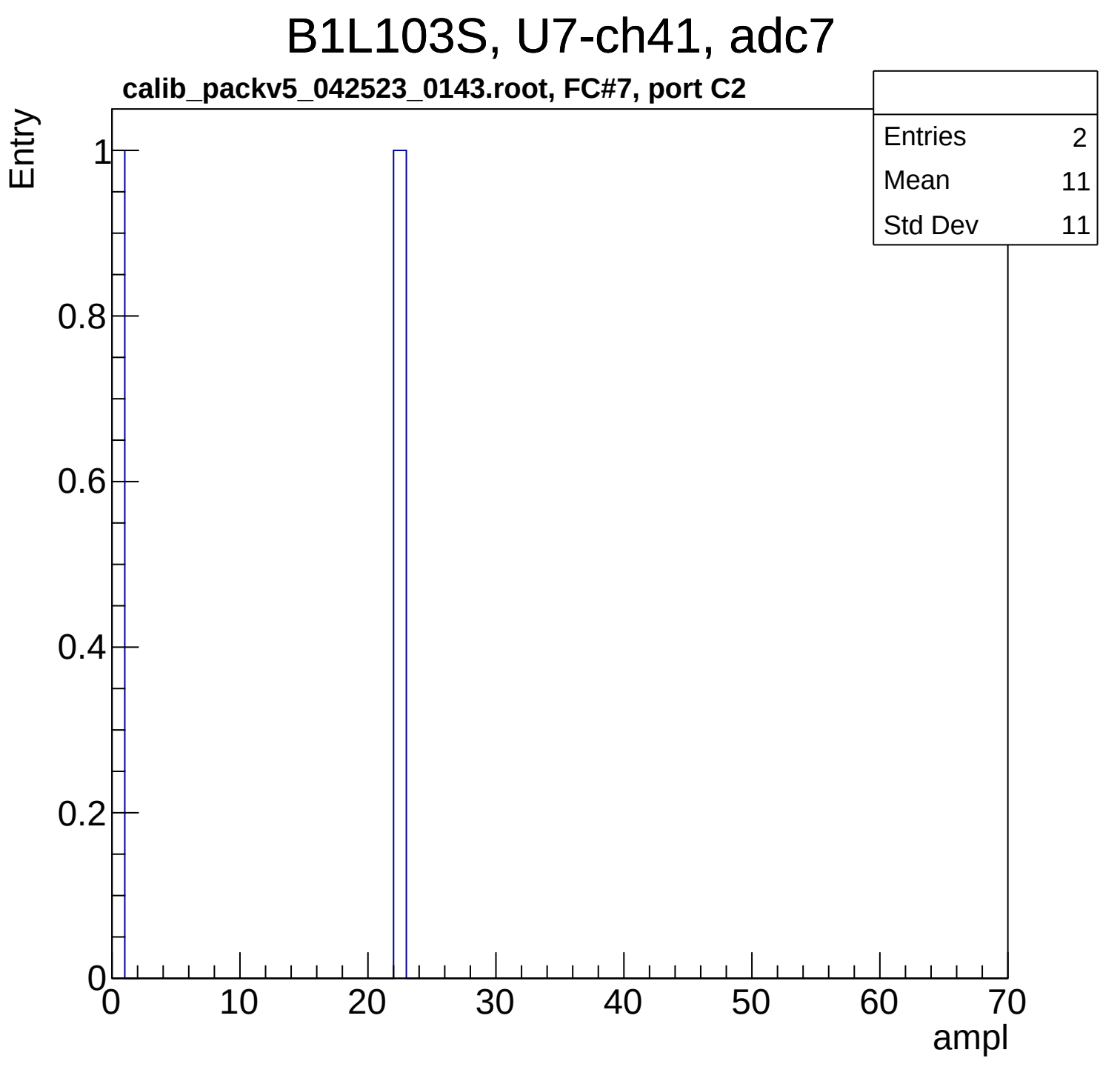
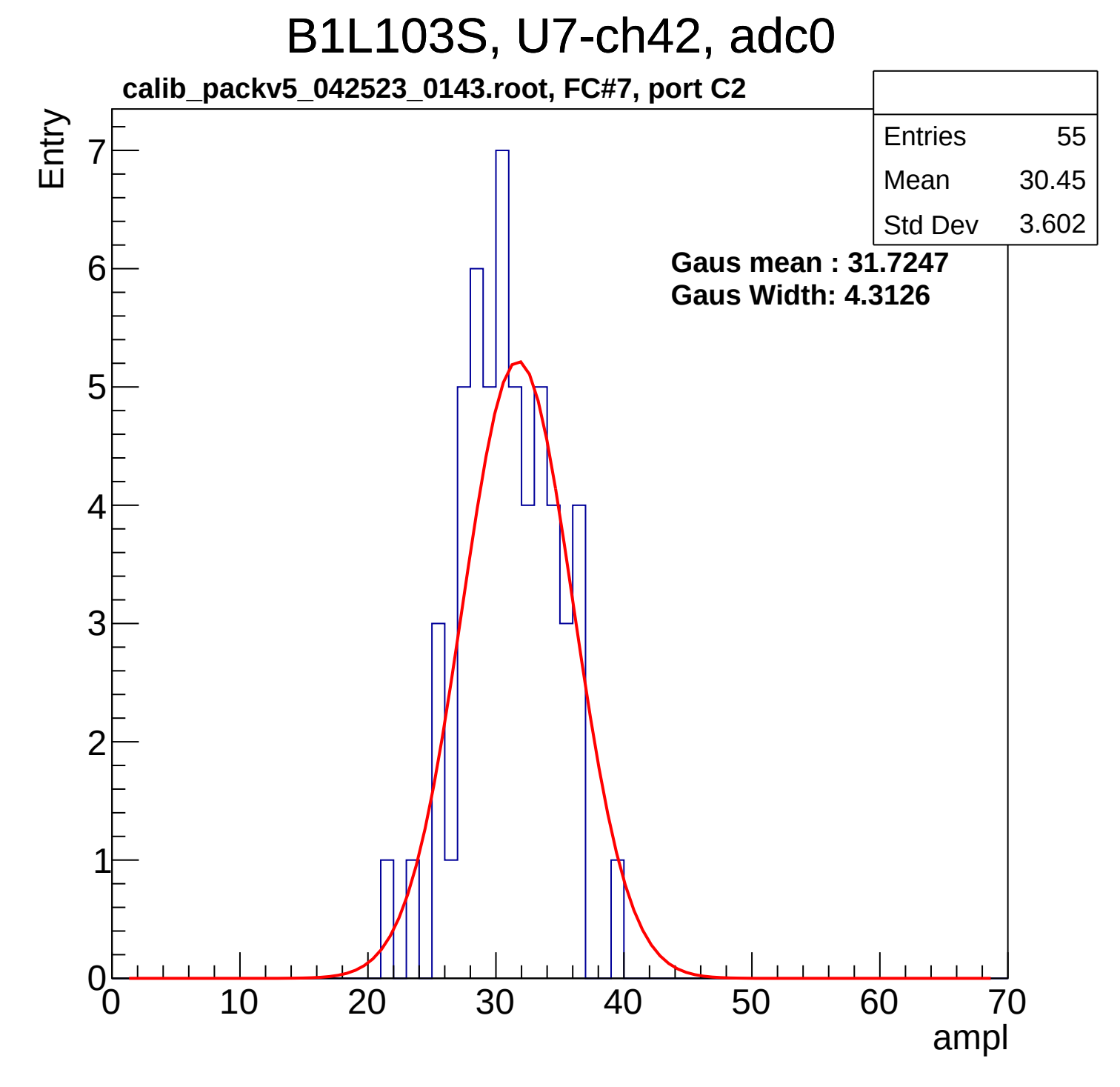
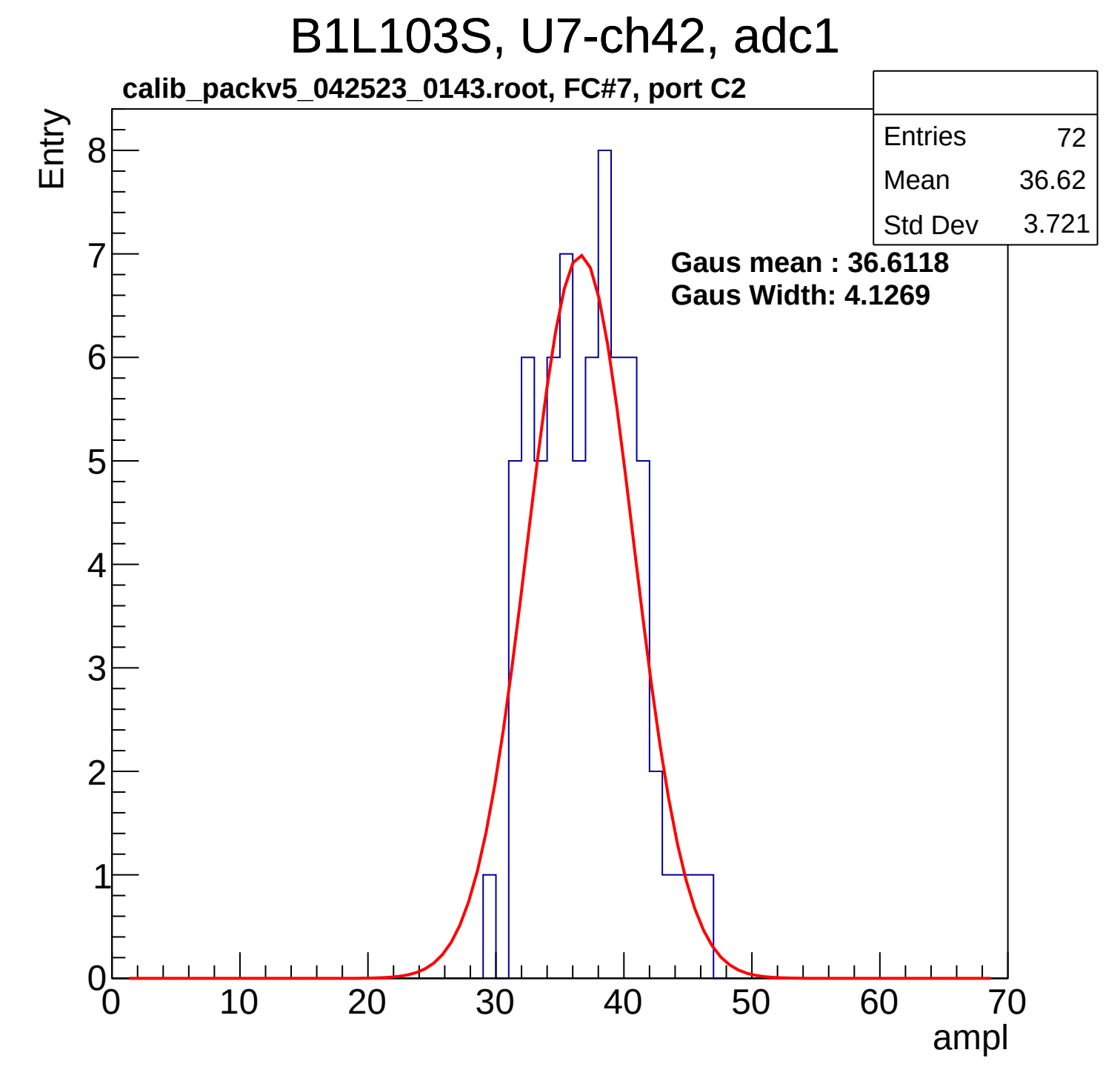
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U7-ch41, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 11
Std Dev 11
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch42, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 30.45
Std Dev 3.602
Gaus mean : 31.7247
Gaus Width: 4.3126
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch42, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 72
Mean 36.62
Std Dev 3.721
Gaus mean : 36.6118
Gaus Width: 4.1269
Entry
ampl
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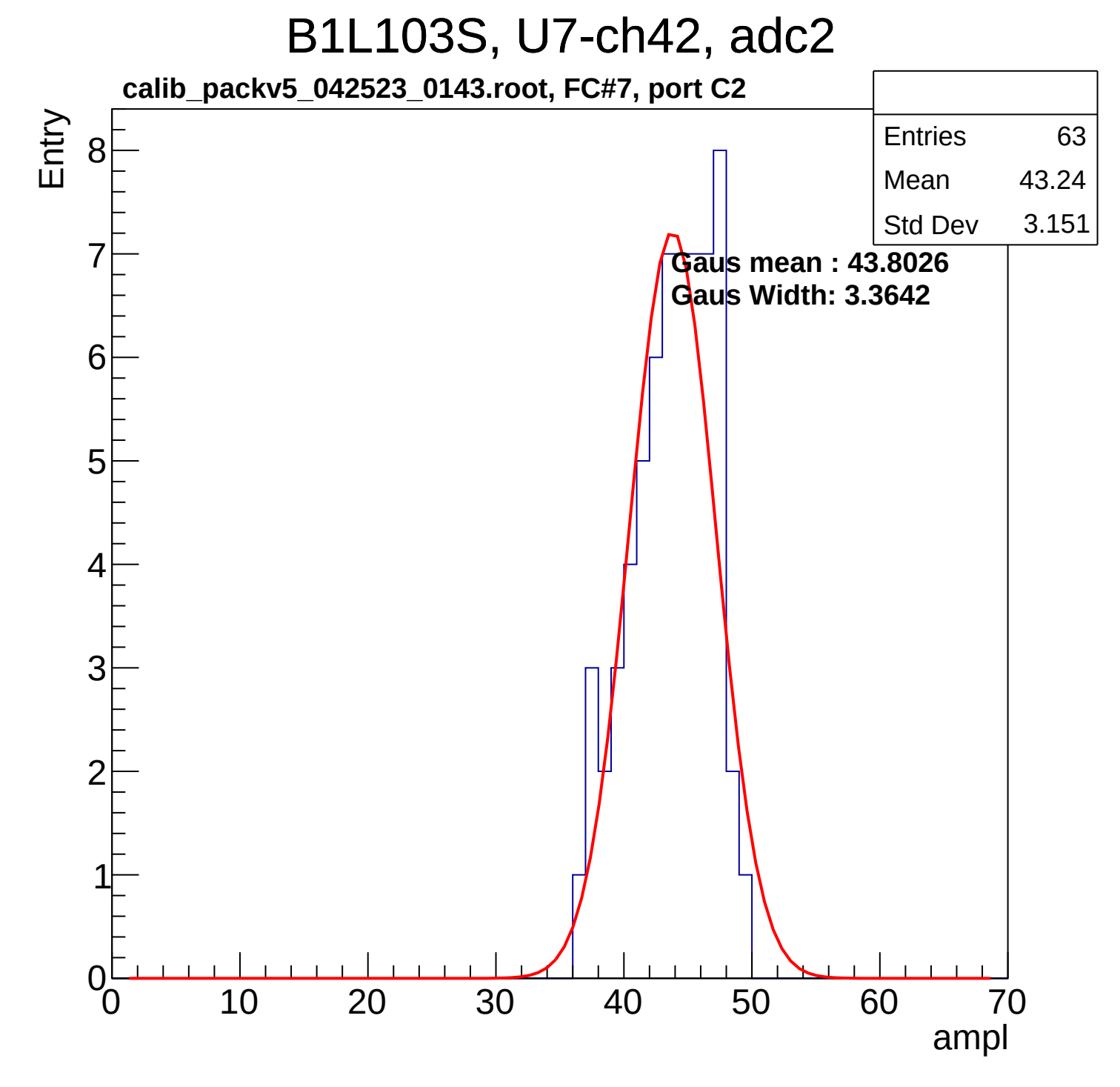
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch42, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 43.24
Std Dev 3.151
Gaus mean : 43.8026
Gaus Width: 3.3642
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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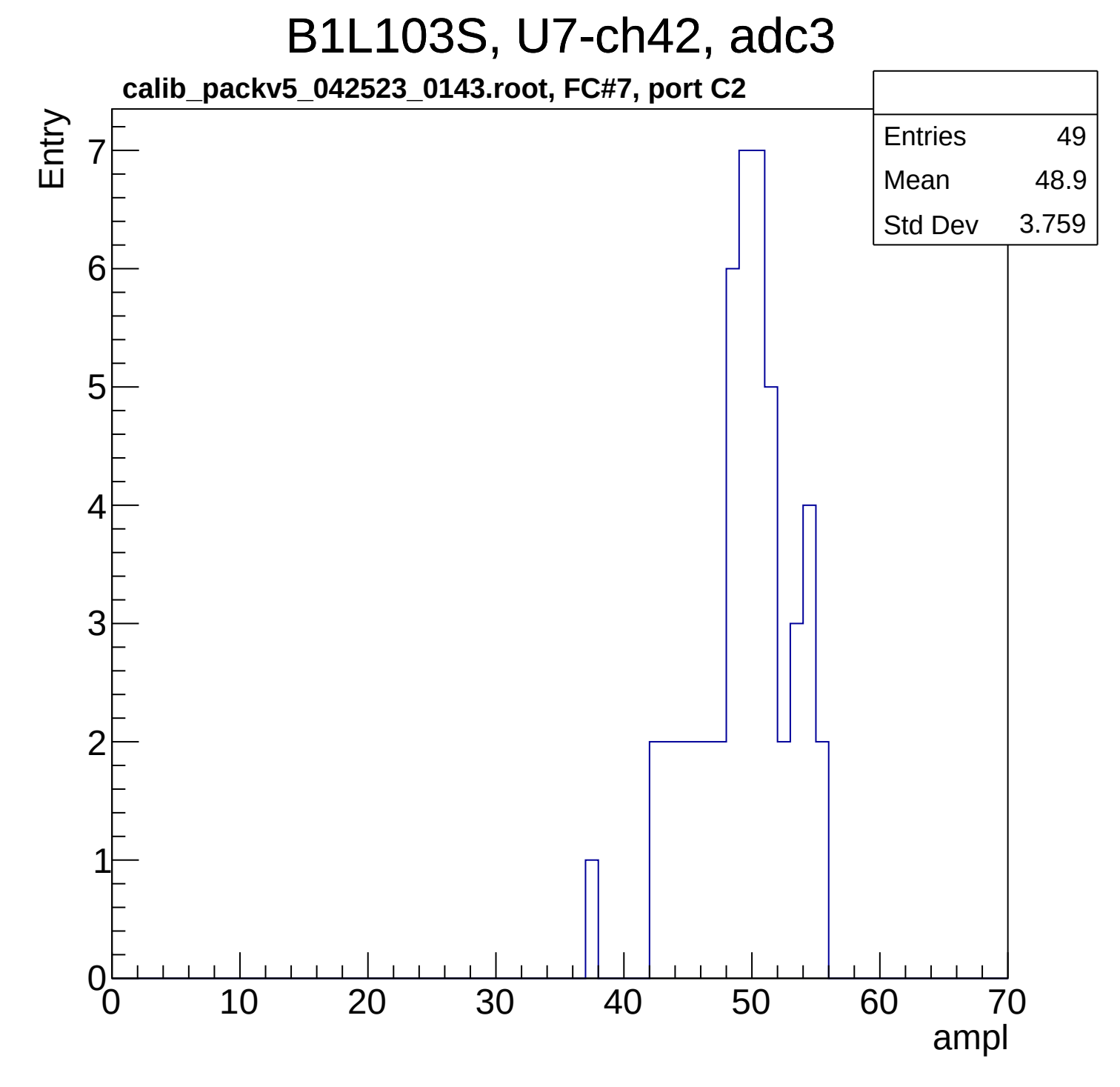
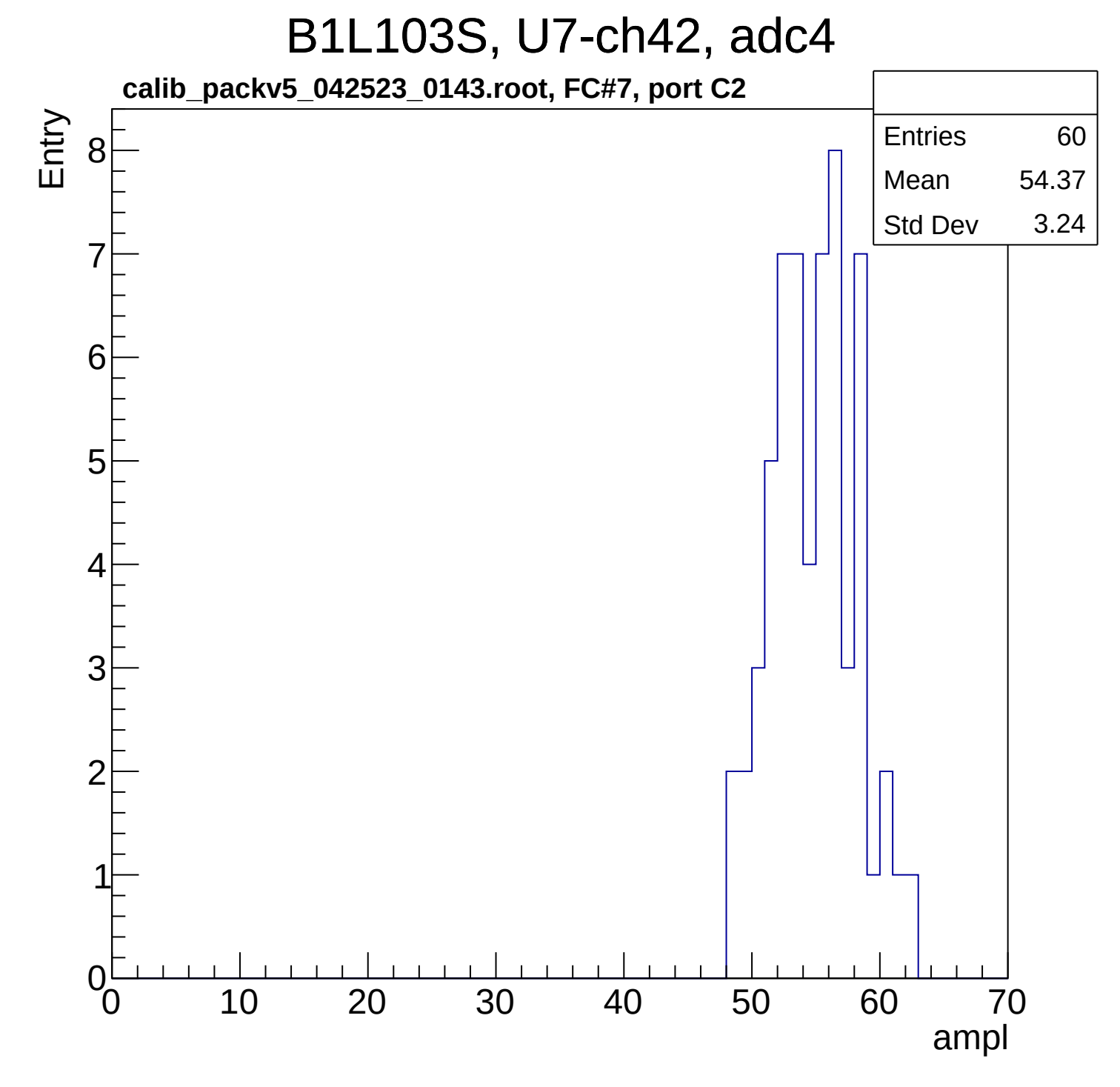

B1L103S, U7-ch42, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 49
Mean 48.9
Std Dev 3.759
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch42, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 60
Mean 54.37
Std Dev 3.24
Entry
ampl
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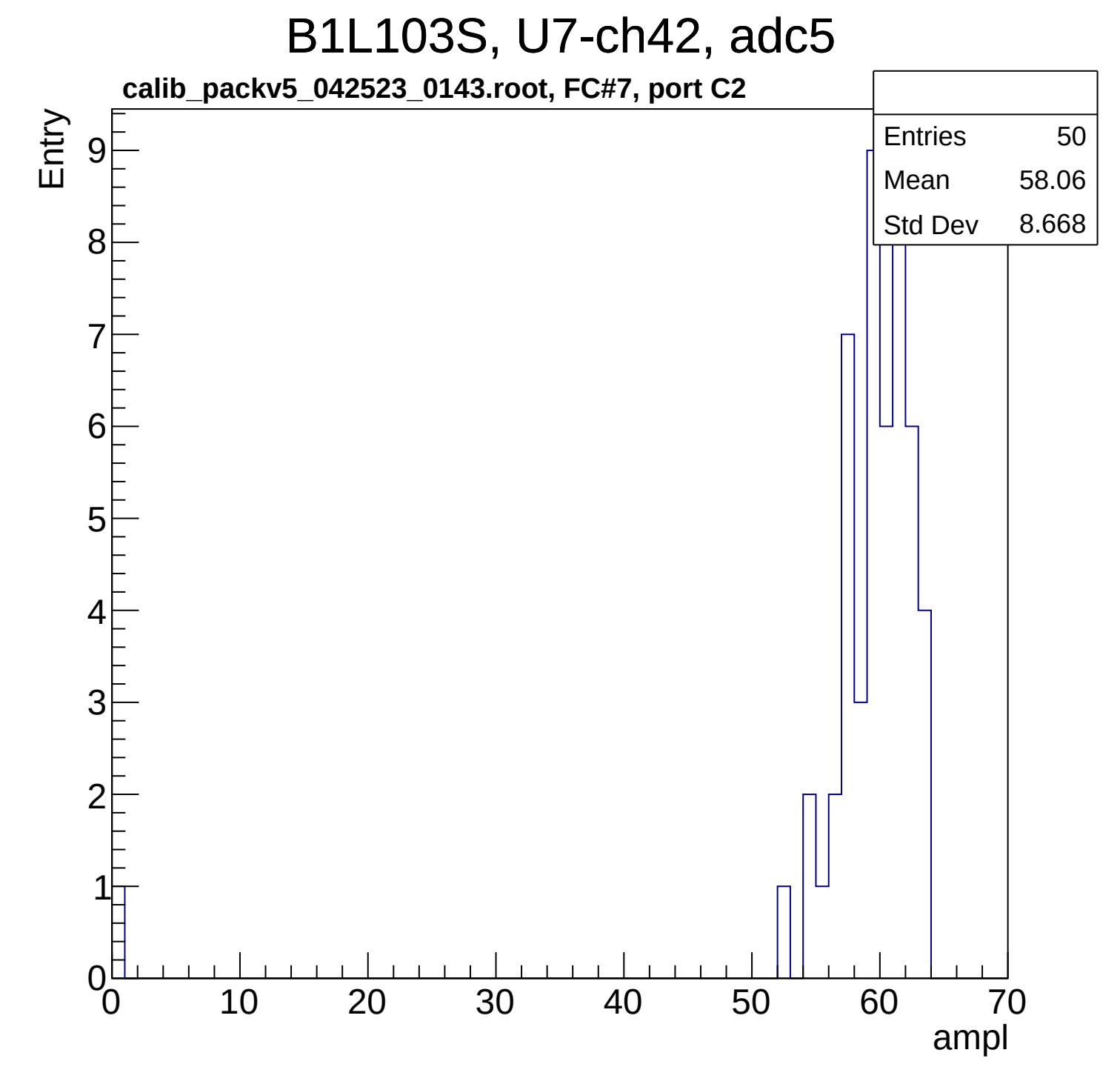
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch42, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 50
Mean 58.06
Std Dev 8.668
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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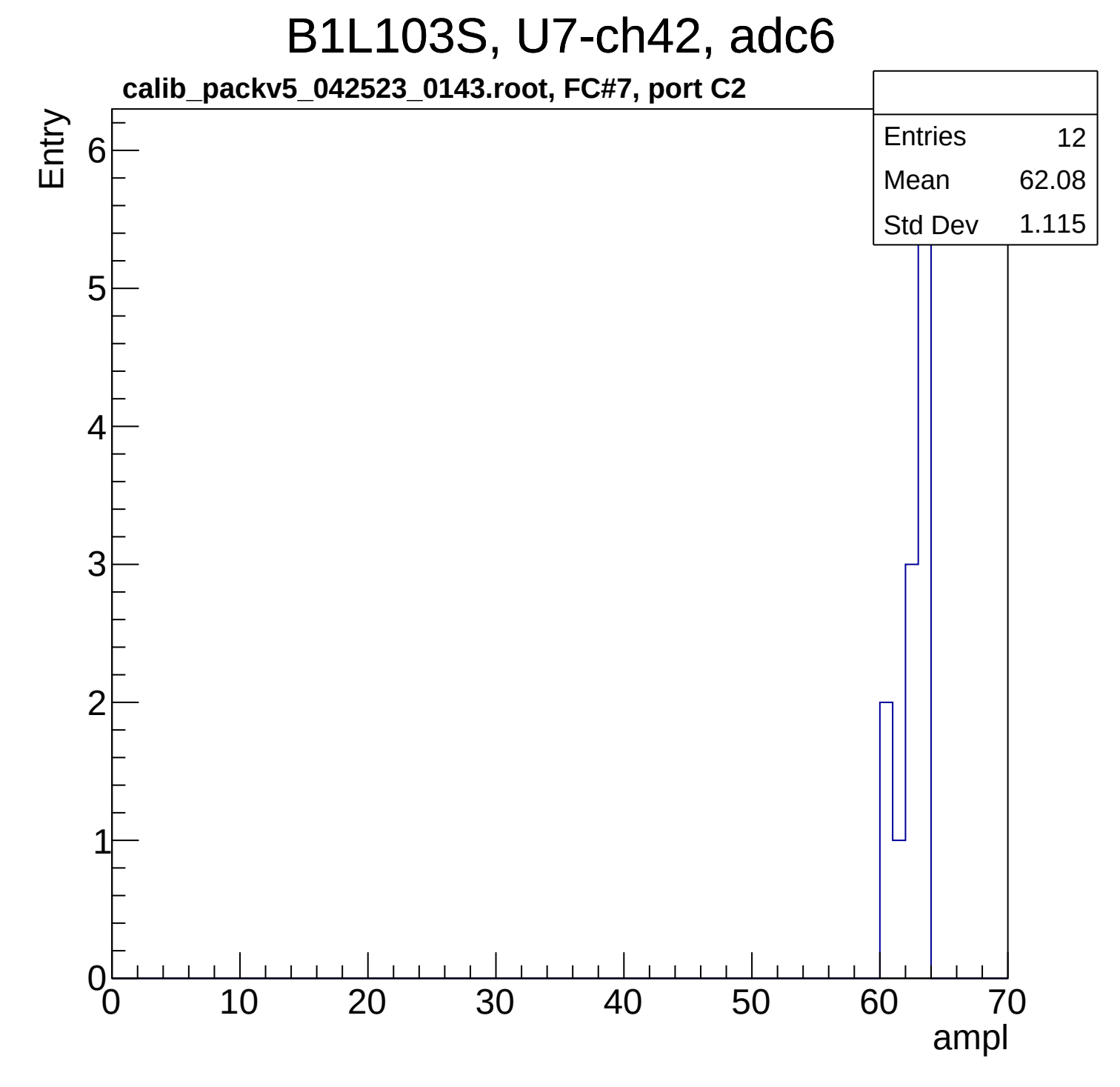
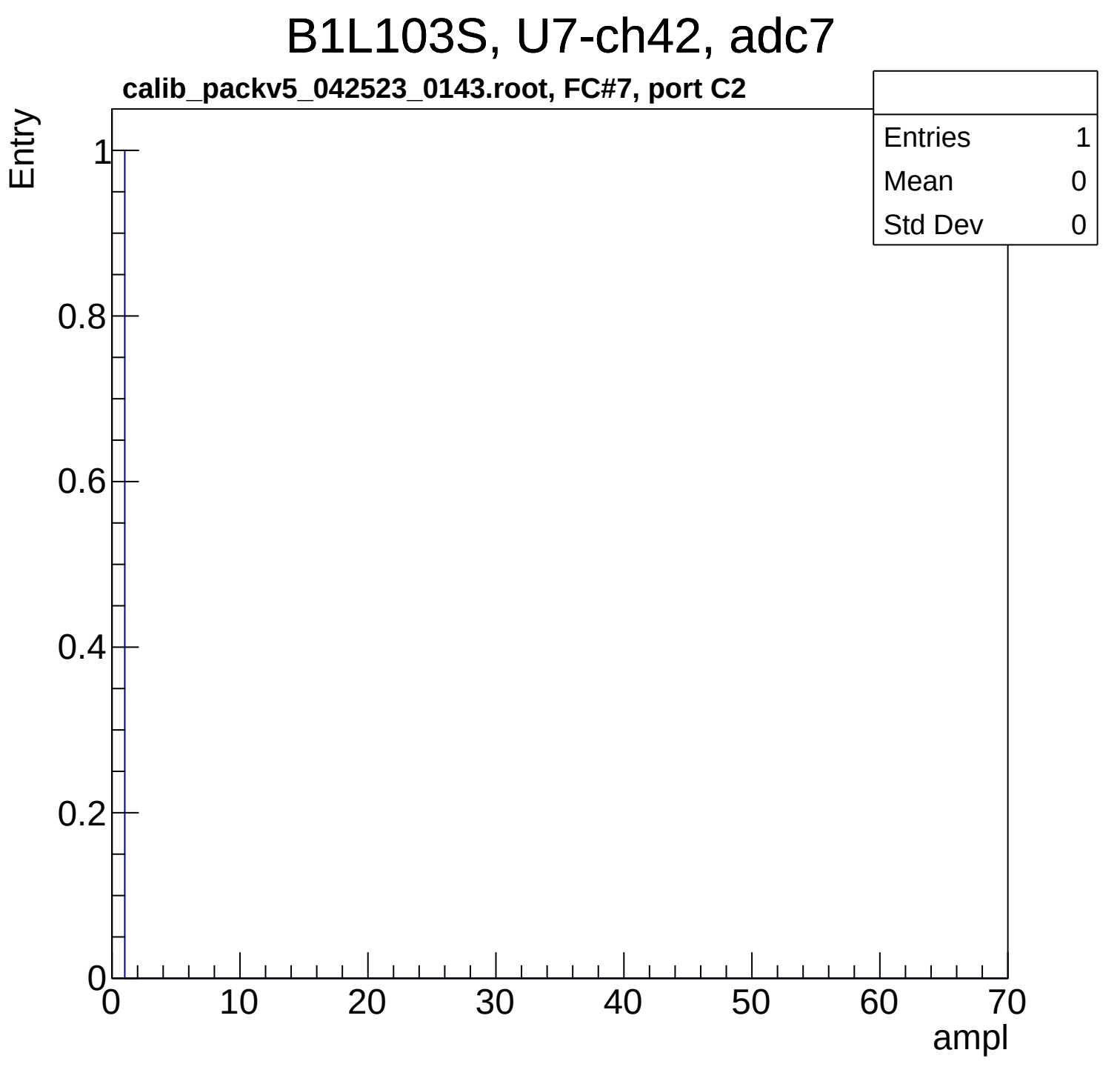

B1L103S, U7-ch42, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 12
Mean 62.08
Std Dev 1.115
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U7-ch42, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
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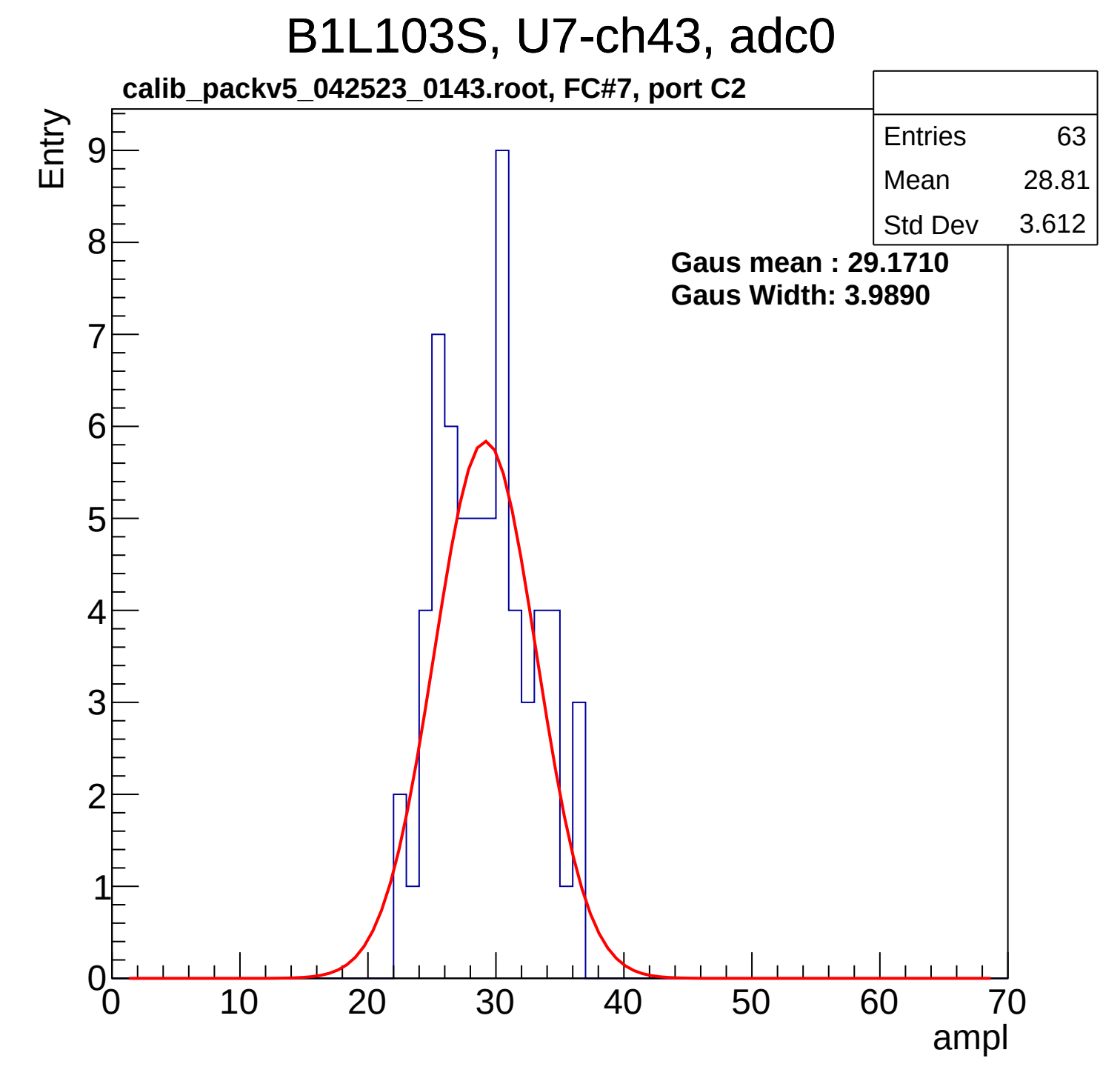
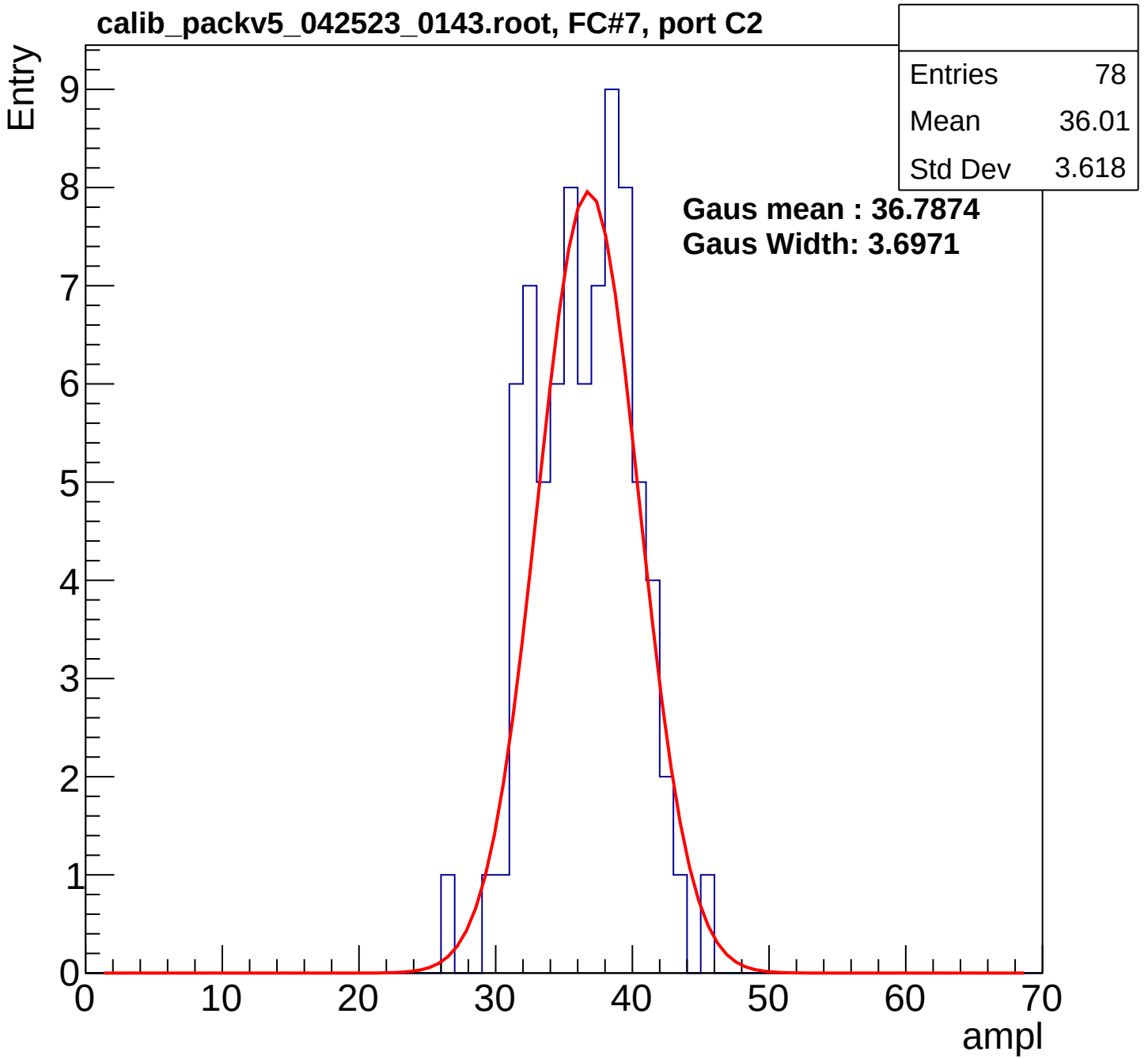
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch43, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 28.81
Std Dev 3.612
Gaus mean : 29.1710
Gaus Width: 3.9890
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L103S, U7-ch43, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 78
Mean 36.01
Std Dev 3.618
Gaus mean : 36.7874
Gaus Width: 3.6971
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
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40
50
60
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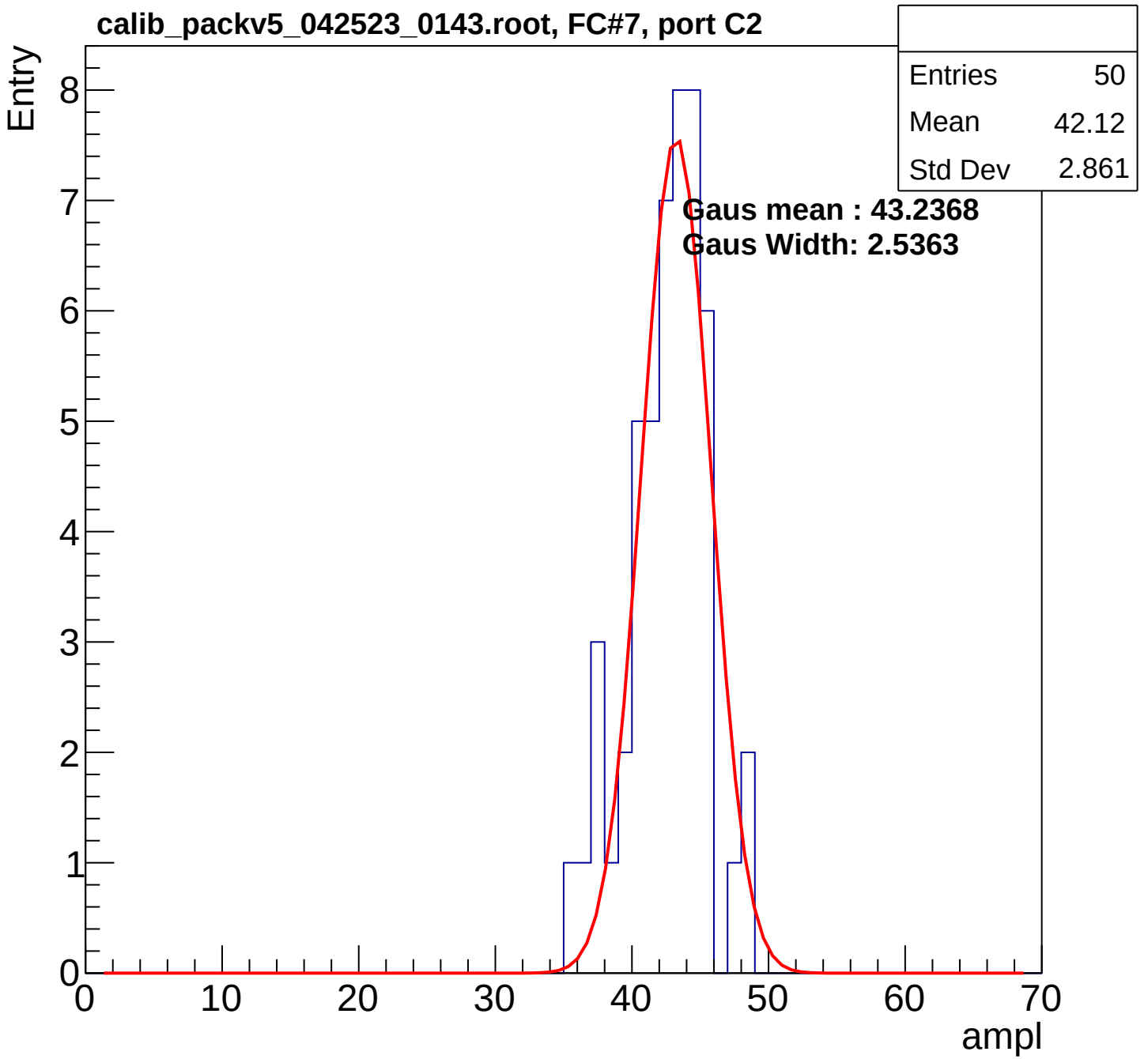
B1L103S, U7-ch43, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 50
Mean 42.12
Std Dev 2.861
Gaus mean : 43.2368
Gaus Width: 2.5363
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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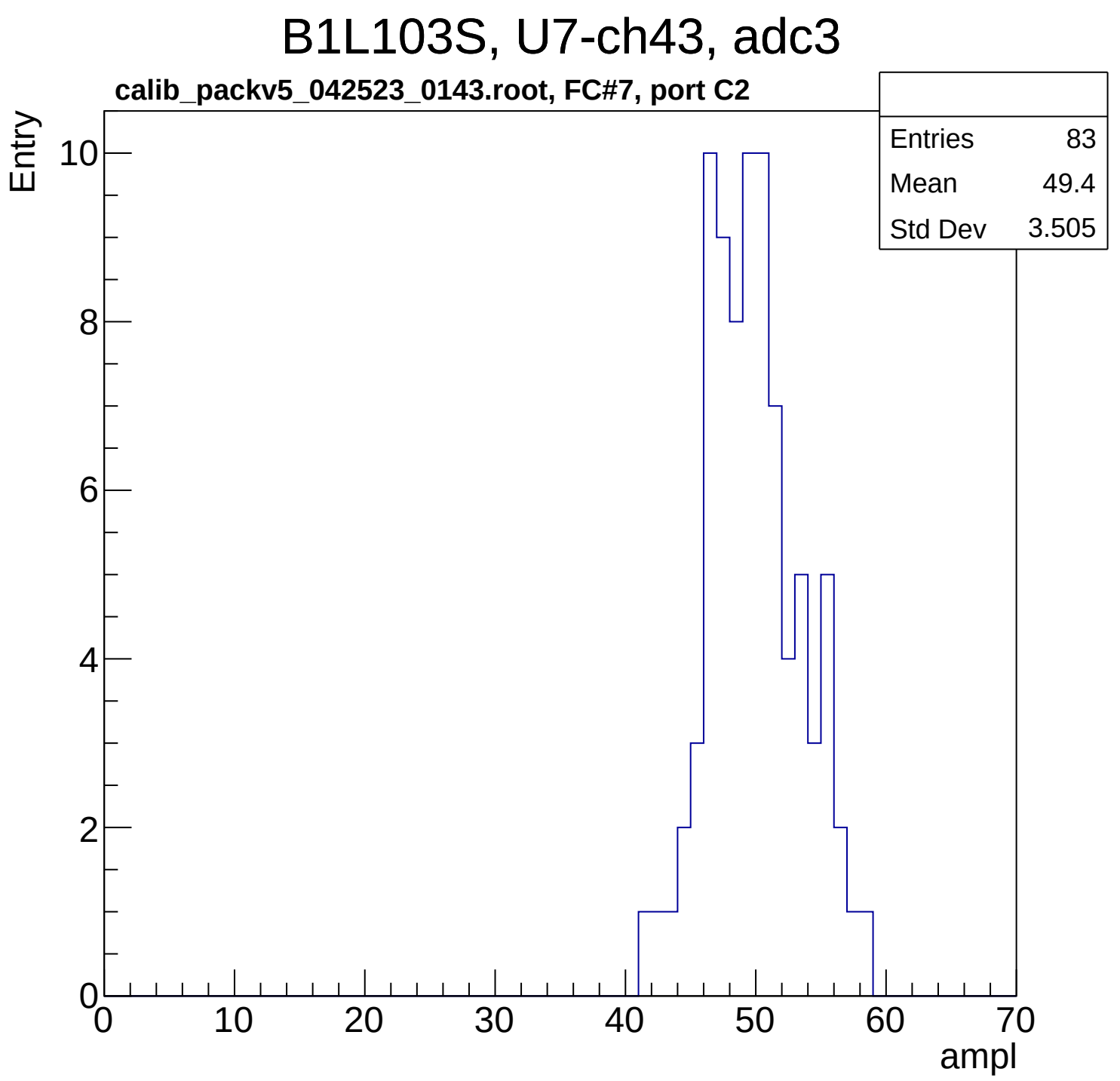
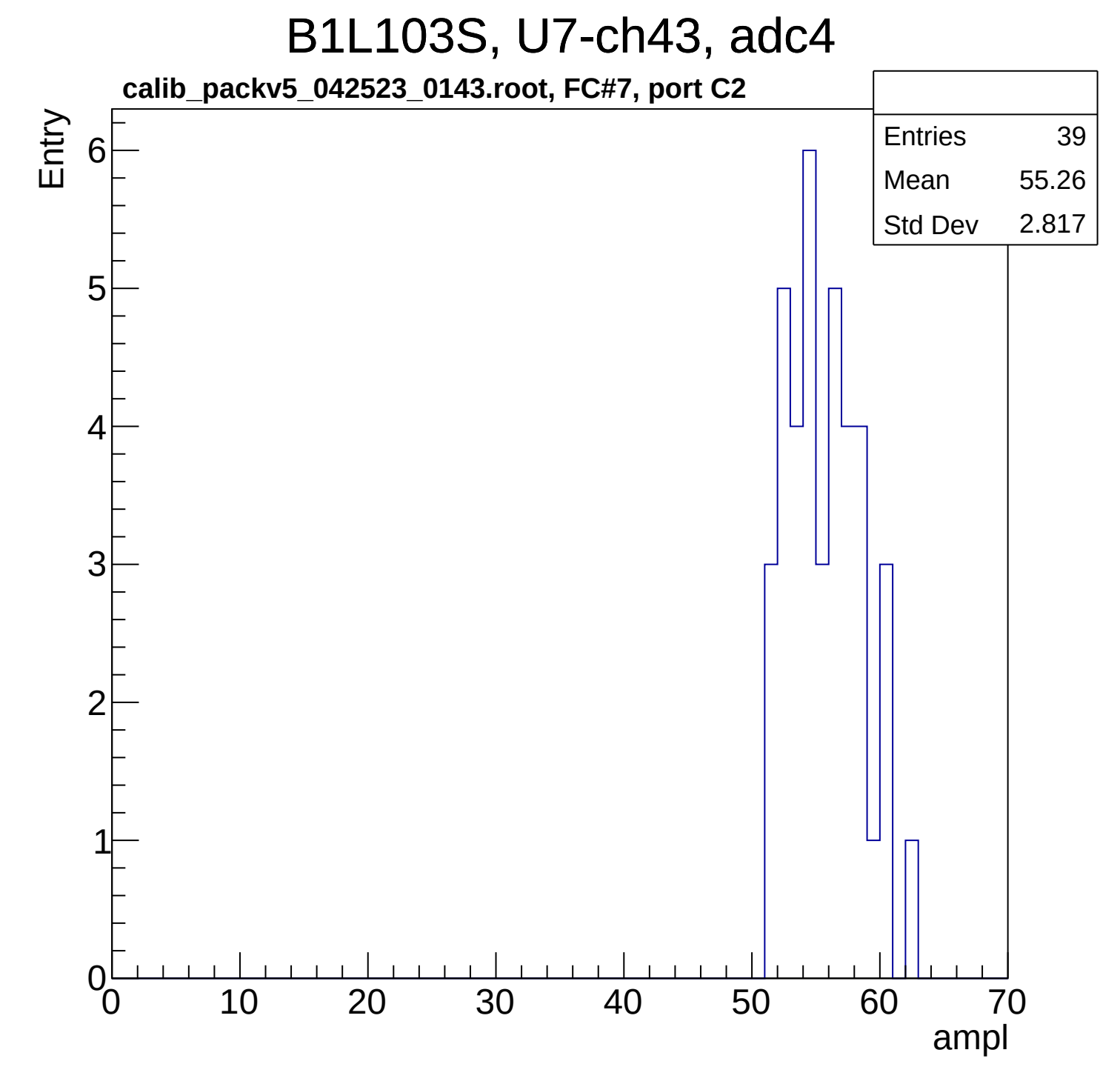

B1L103S, U7-ch43, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 83
Mean 49.4
Std Dev 3.505
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch43, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 39
Mean 55.26
Std Dev 2.817
Entry
ampl
0
1
2
3
4
5
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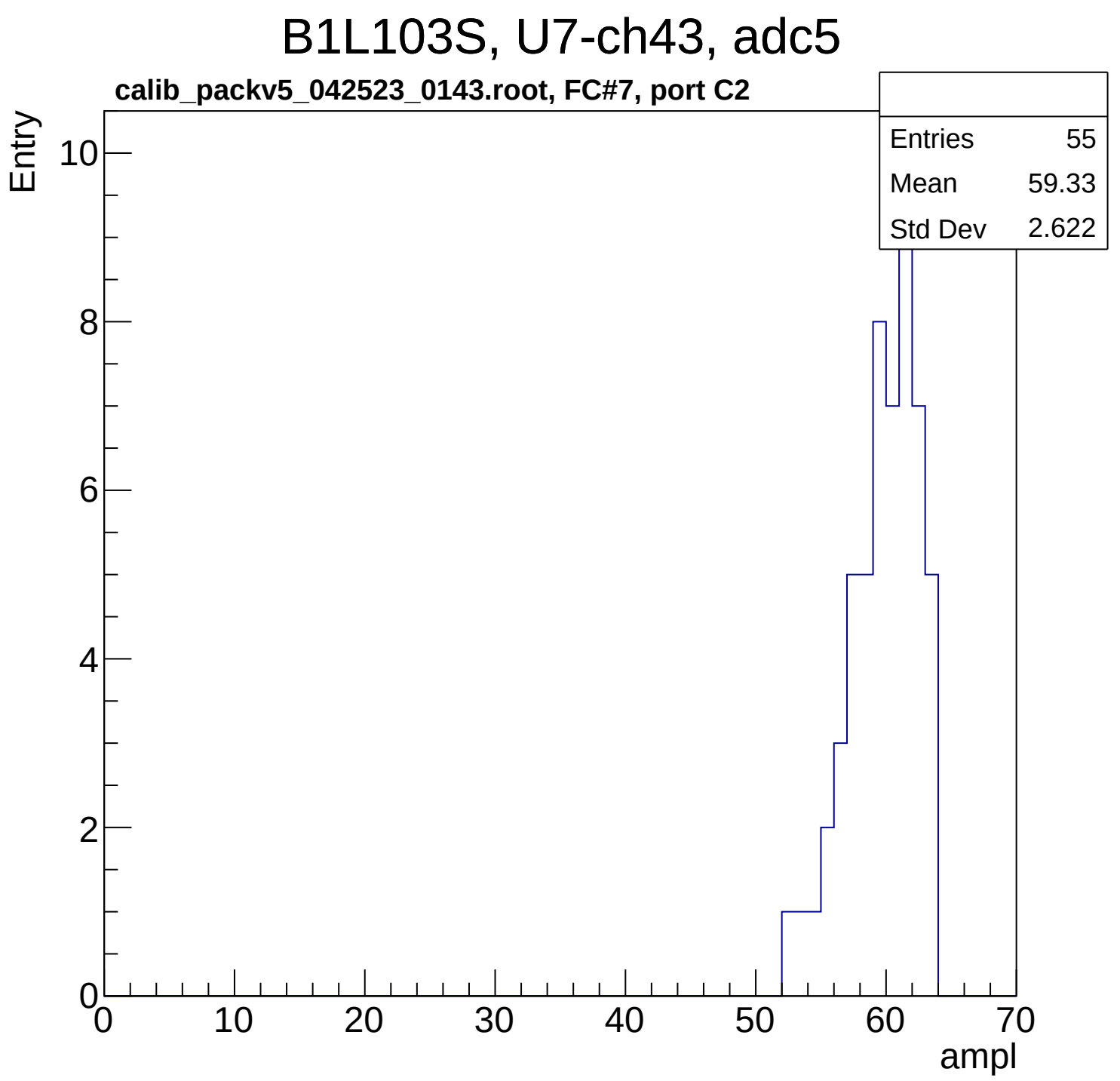
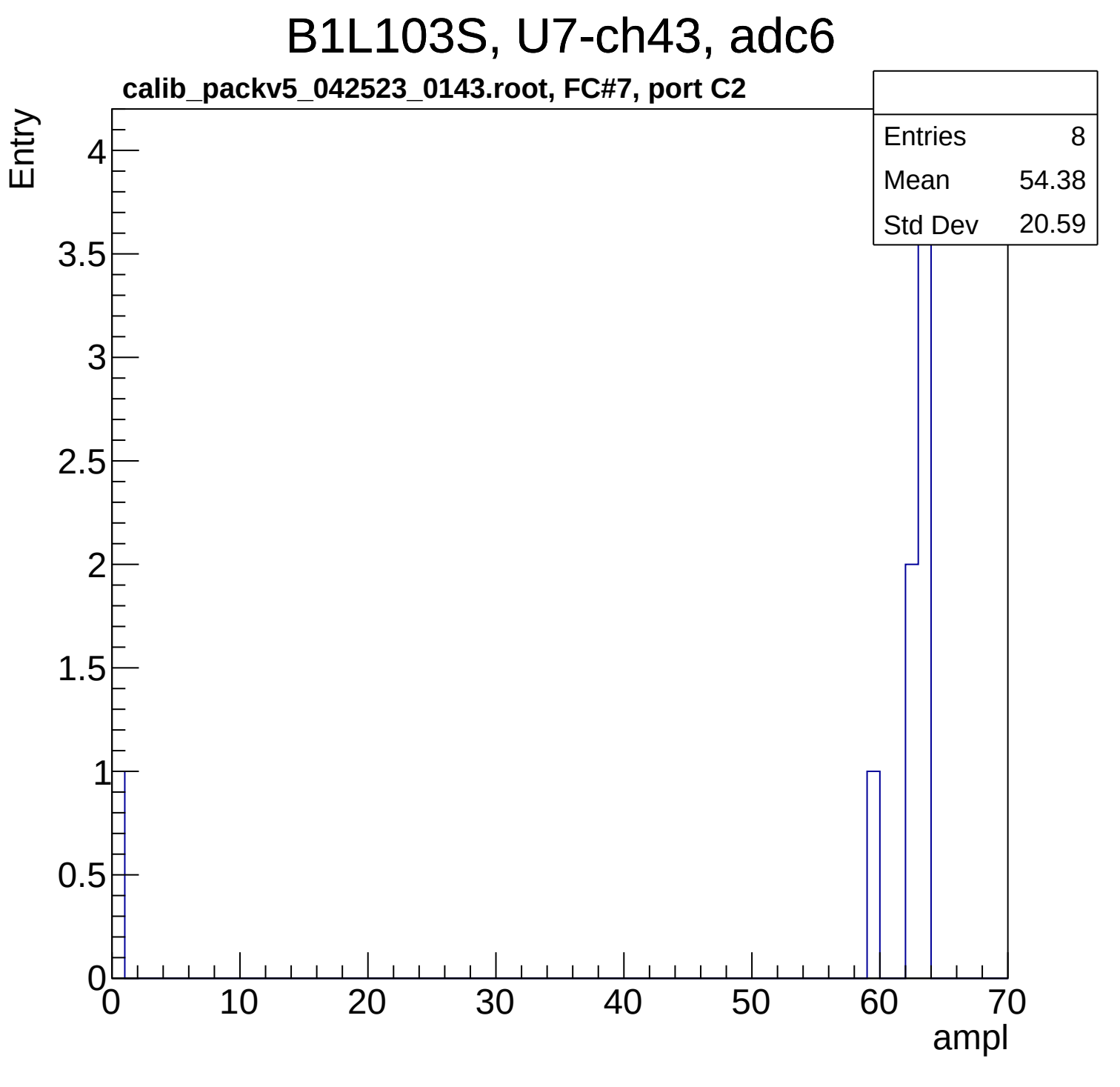
0
10
20
30
40
50
60
70


B1L103S, U7-ch43, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 59.33
Std Dev 2.622
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch43, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 8
Mean 54.38
Std Dev 20.59
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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40
50
60
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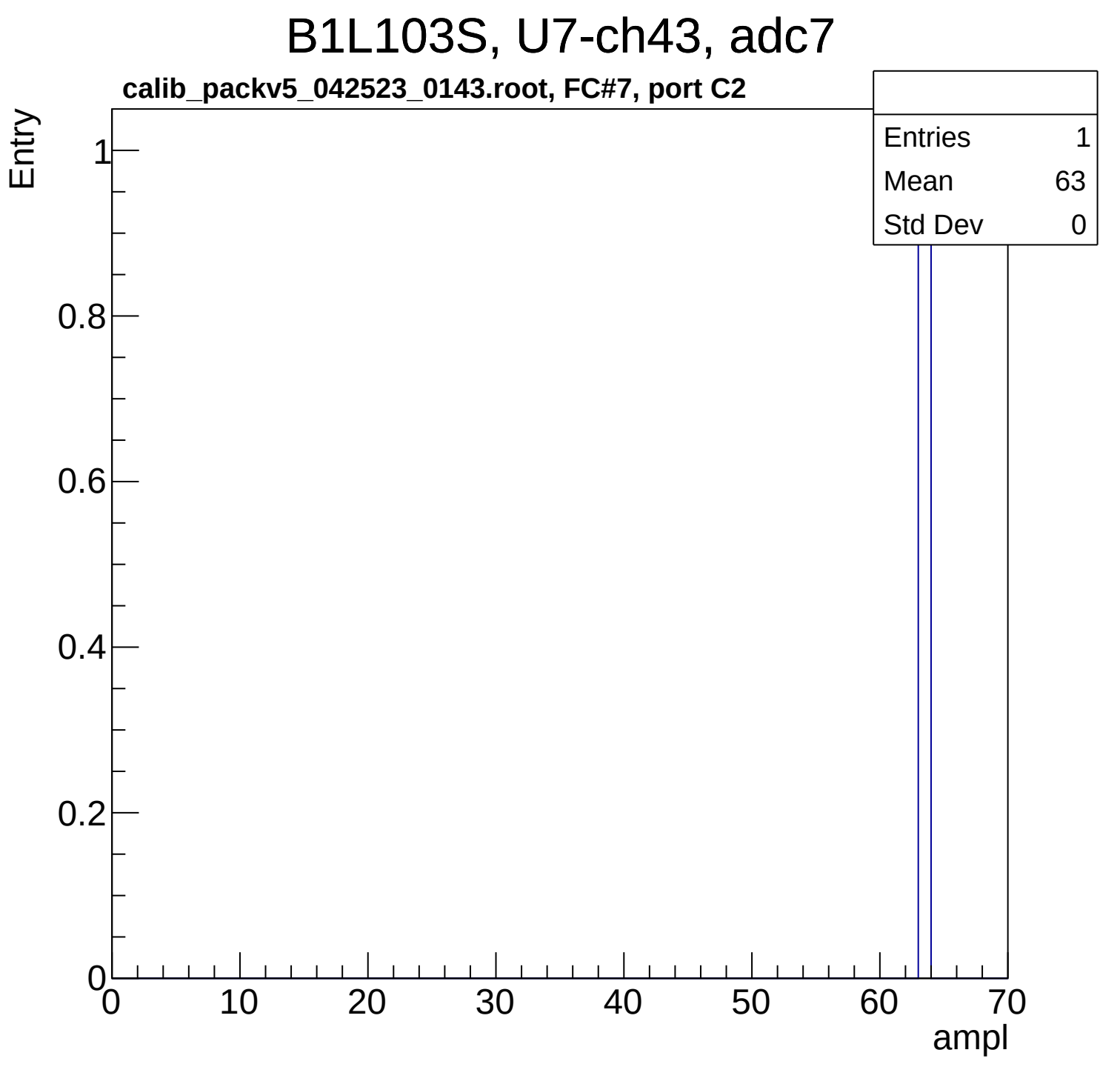
B1L103S, U7-ch43, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 63
Std Dev 0
Entry
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0.6
0.4
0.2
0
0
10
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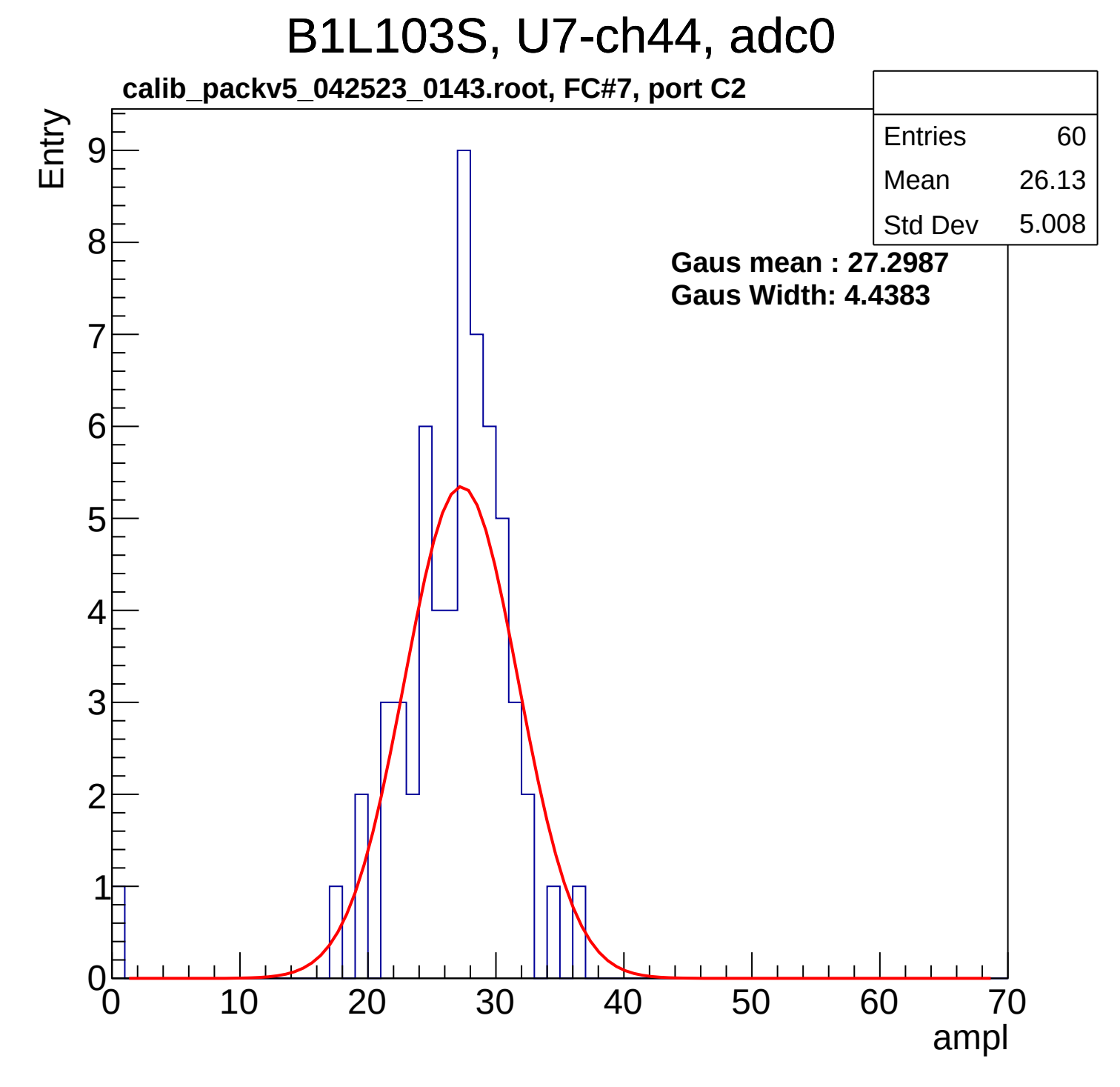
30
40
50
60
70
ampl


B1L103S, U7-ch44, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 60
Mean 26.13
Std Dev 5.008
Gaus mean : 27.2987
Gaus Width: 4.4383
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
30
40
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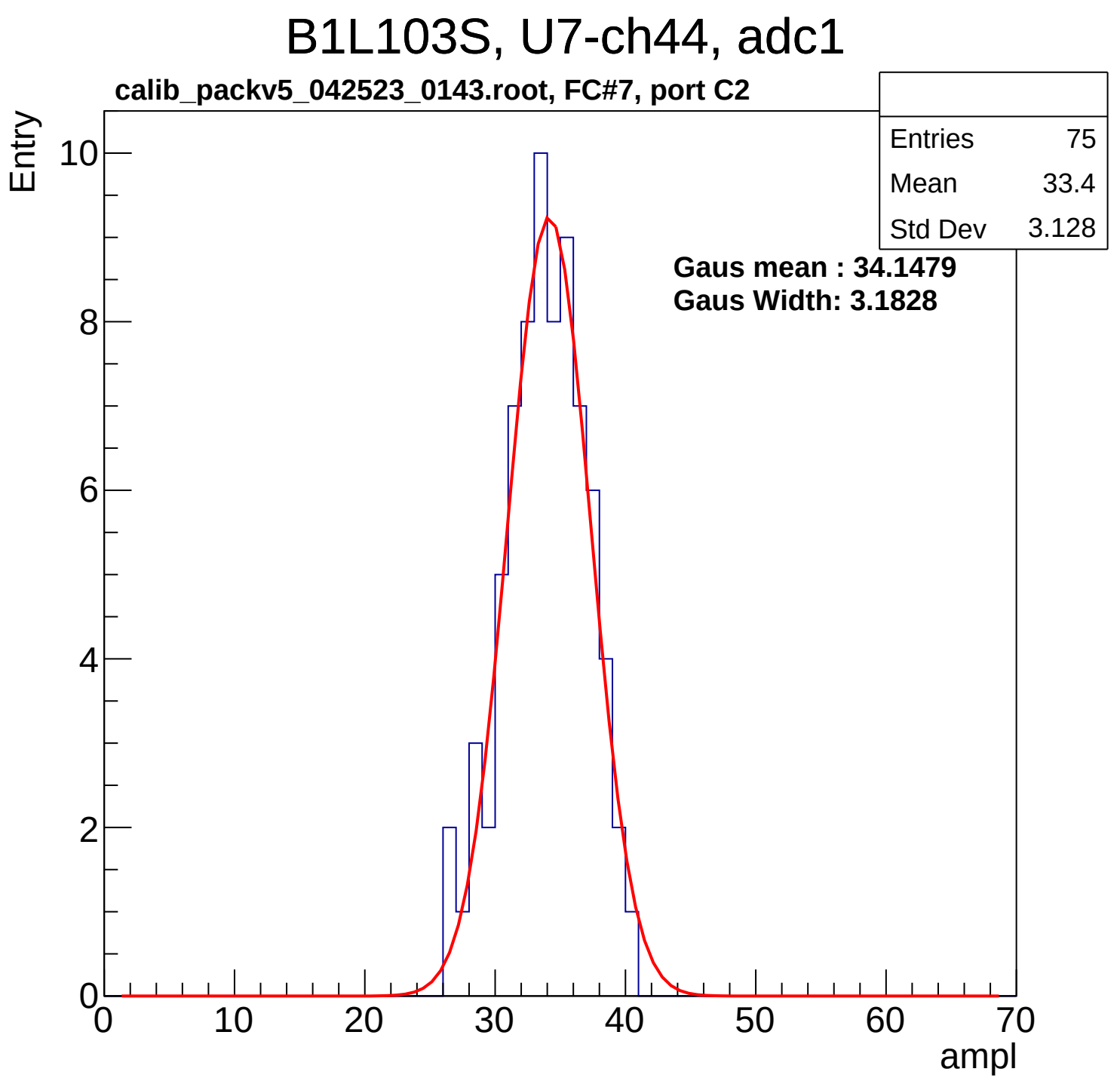
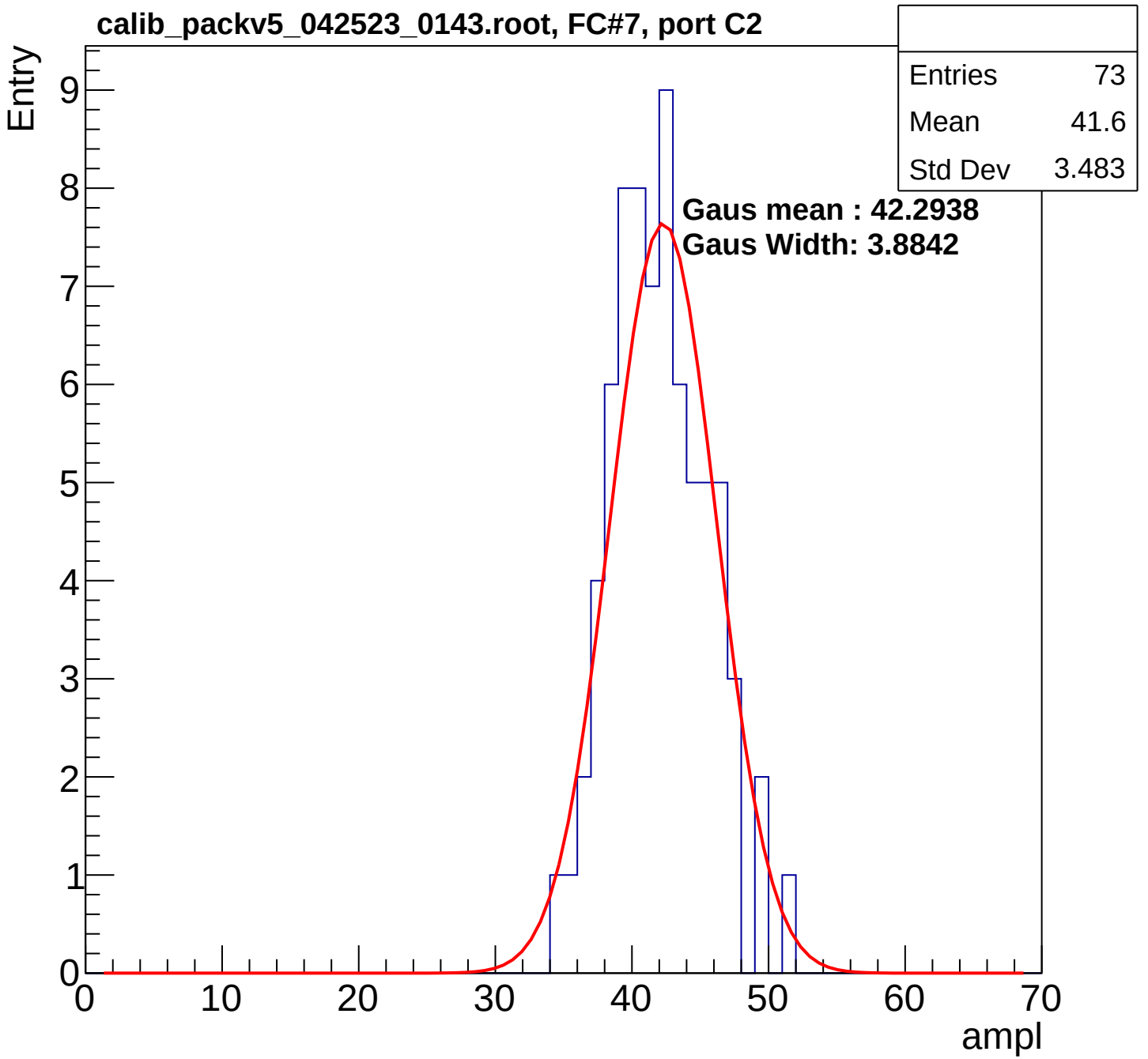
60
70


B1L103S, U7-ch44, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 75
Mean 33.4
Std Dev 3.128
Gaus mean : 34.1479
Gaus Width: 3.1828
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch44, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 73
Mean 41.6
Std Dev 3.483
Gaus mean : 42.2938
Gaus Width: 3.8842
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
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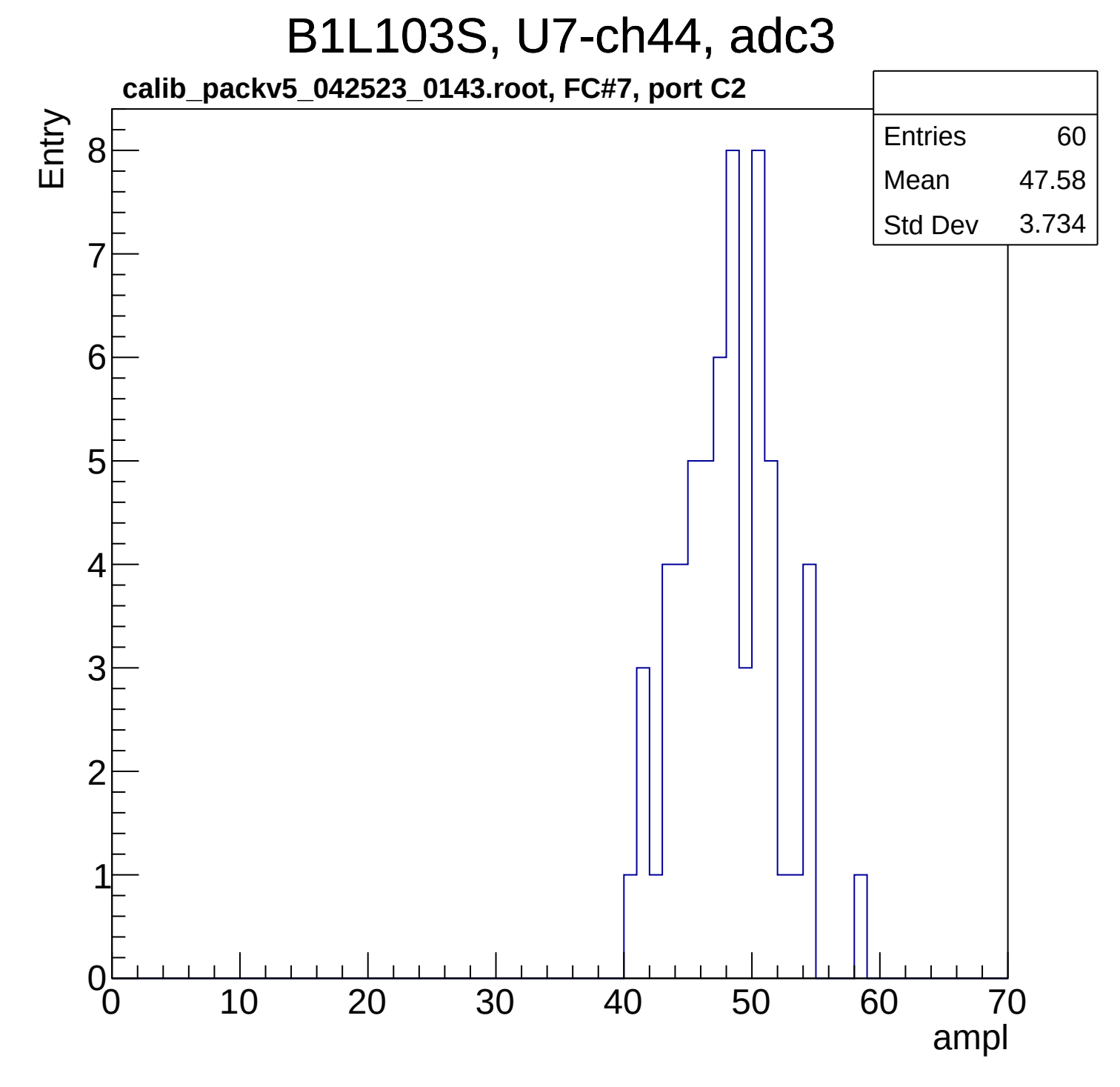
60
70


B1L103S, U7-ch44, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 60
Mean 47.58
Std Dev 3.734
Entry
ampl
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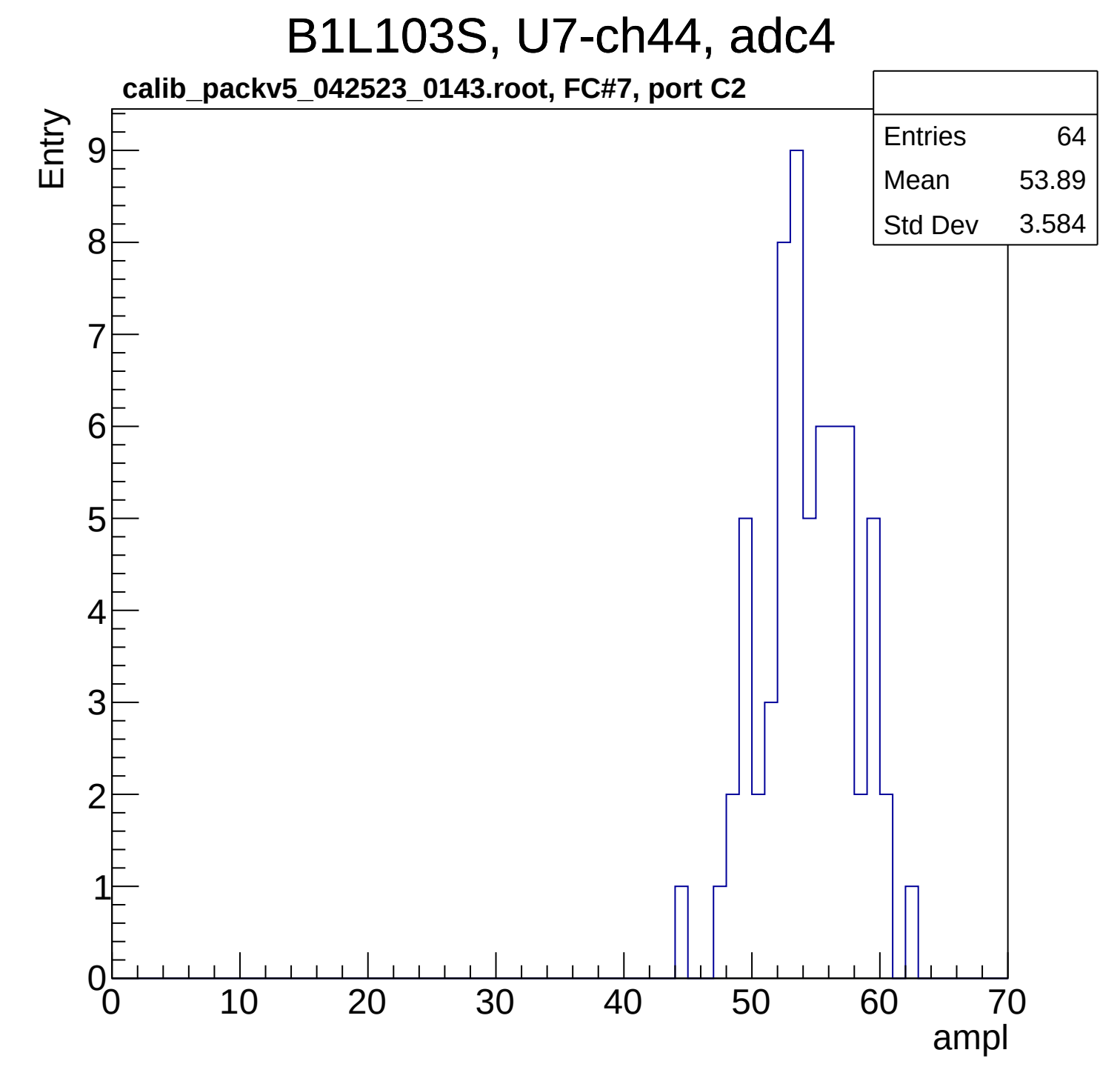
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch44, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 53.89
Std Dev 3.584
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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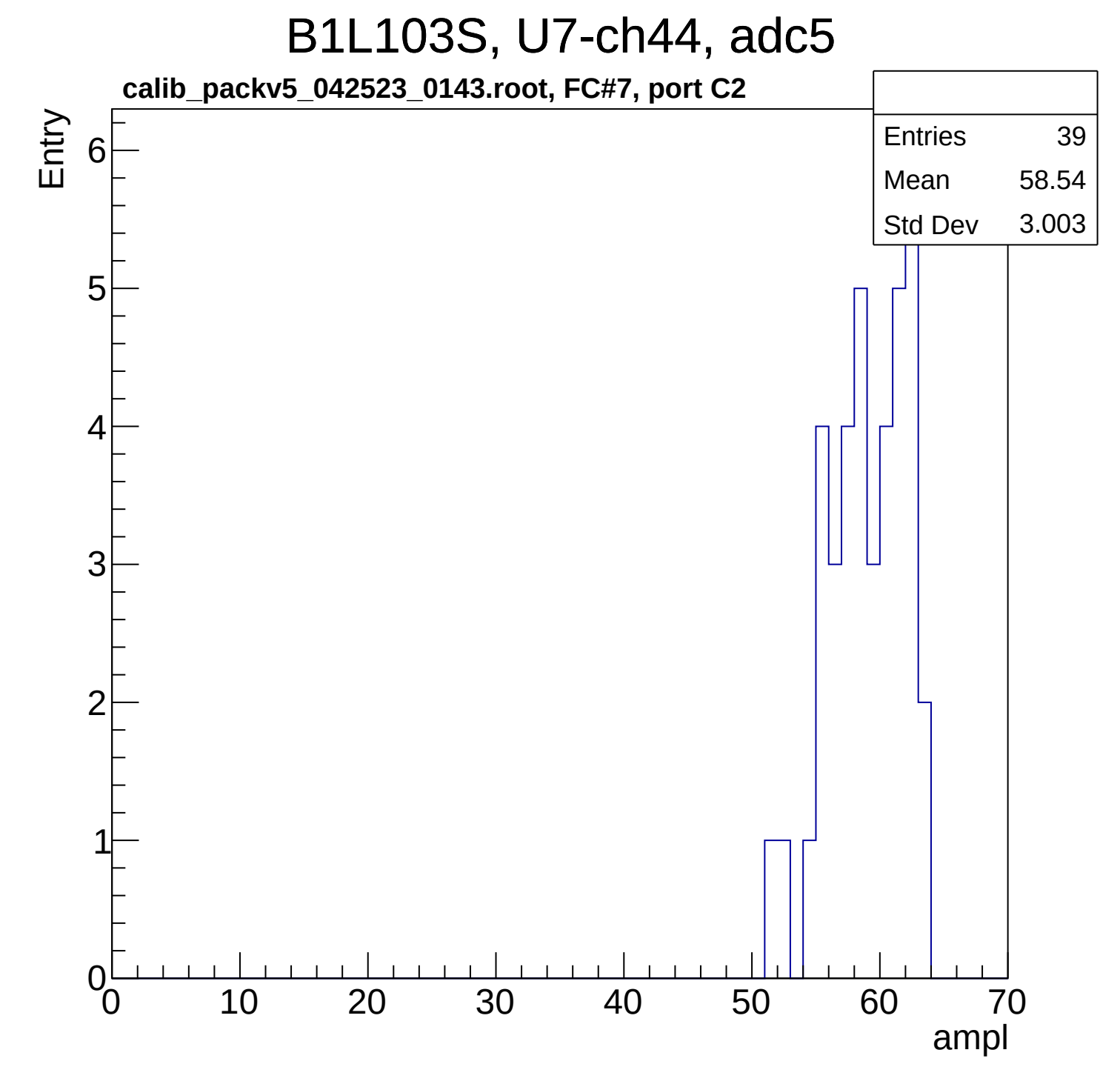
B1L103S, U7-ch44, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 39
Mean 58.54
Std Dev 3.003
Entry
ampl
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2
3
4
5
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0
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20
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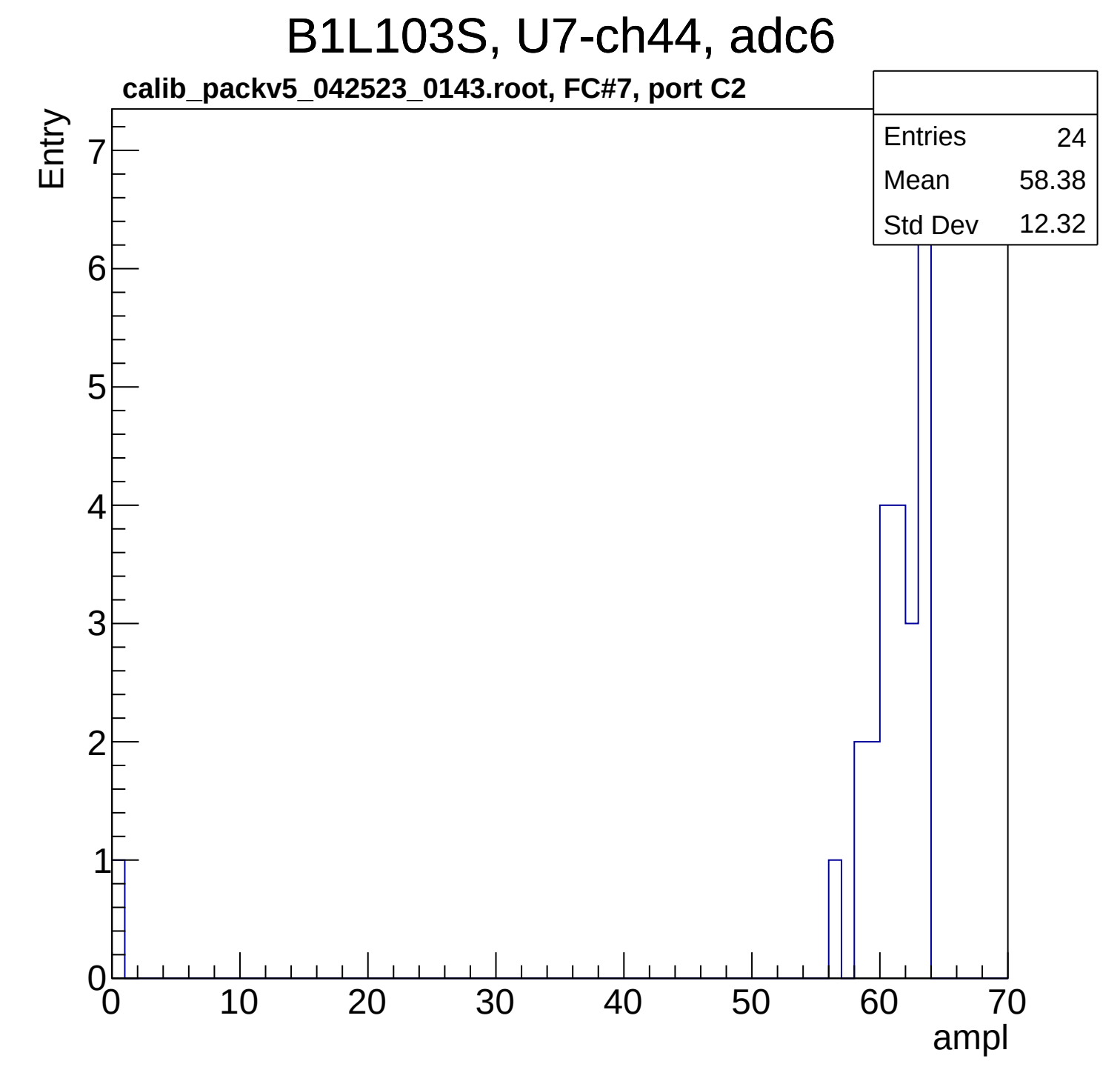
40
50
60
70


B1L103S, U7-ch44, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 24
Mean 58.38
Std Dev 12.32
Entry
ampl
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4
5
6
7
0
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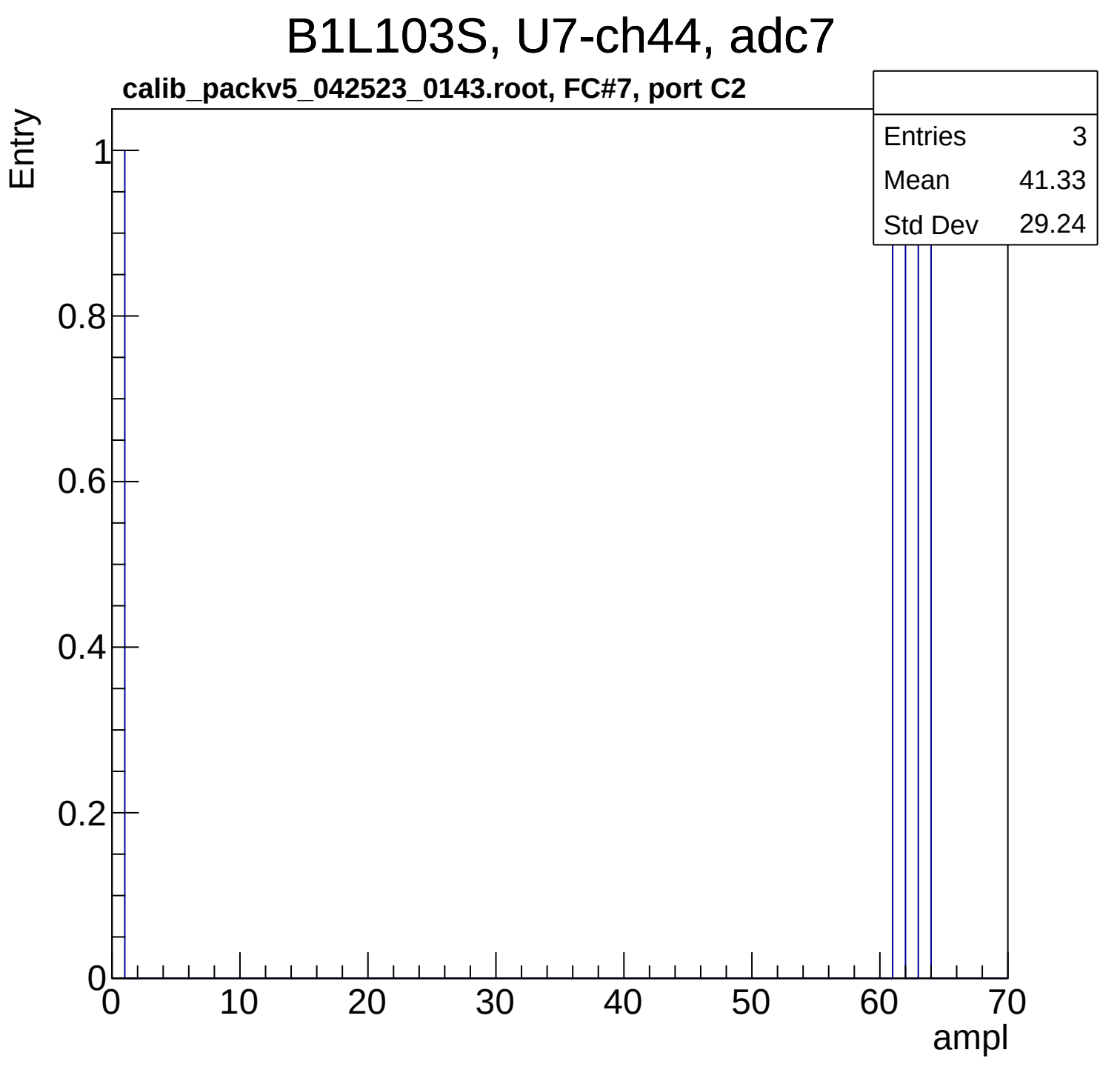
20
30
40
50
60
70


B1L103S, U7-ch44, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 41.33
Std Dev 29.24
Entry
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0.6
0.4
0.2
0
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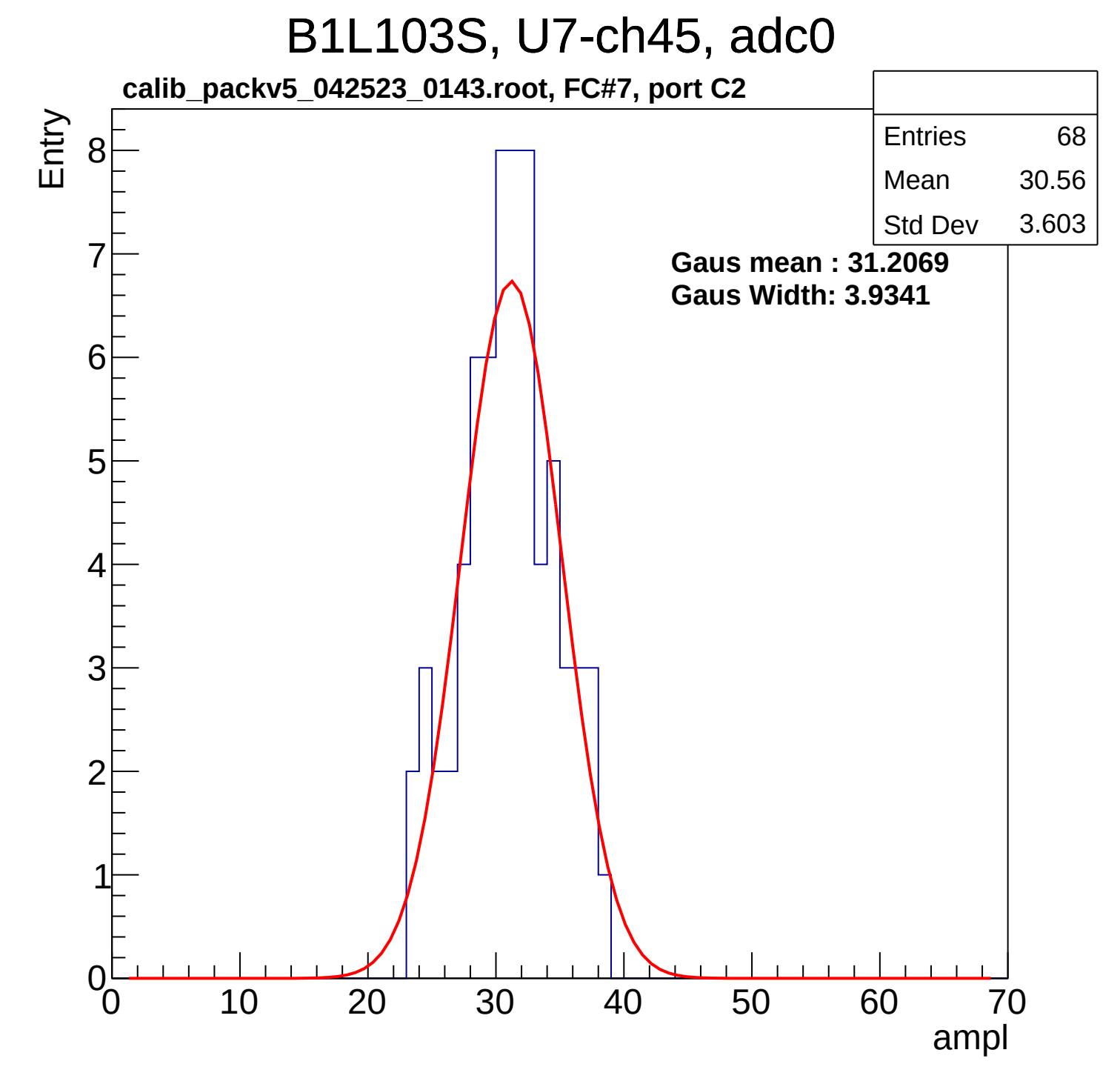
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch45, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 30.56
Std Dev 3.603
Gaus mean : 31.2069
Gaus Width: 3.9341
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
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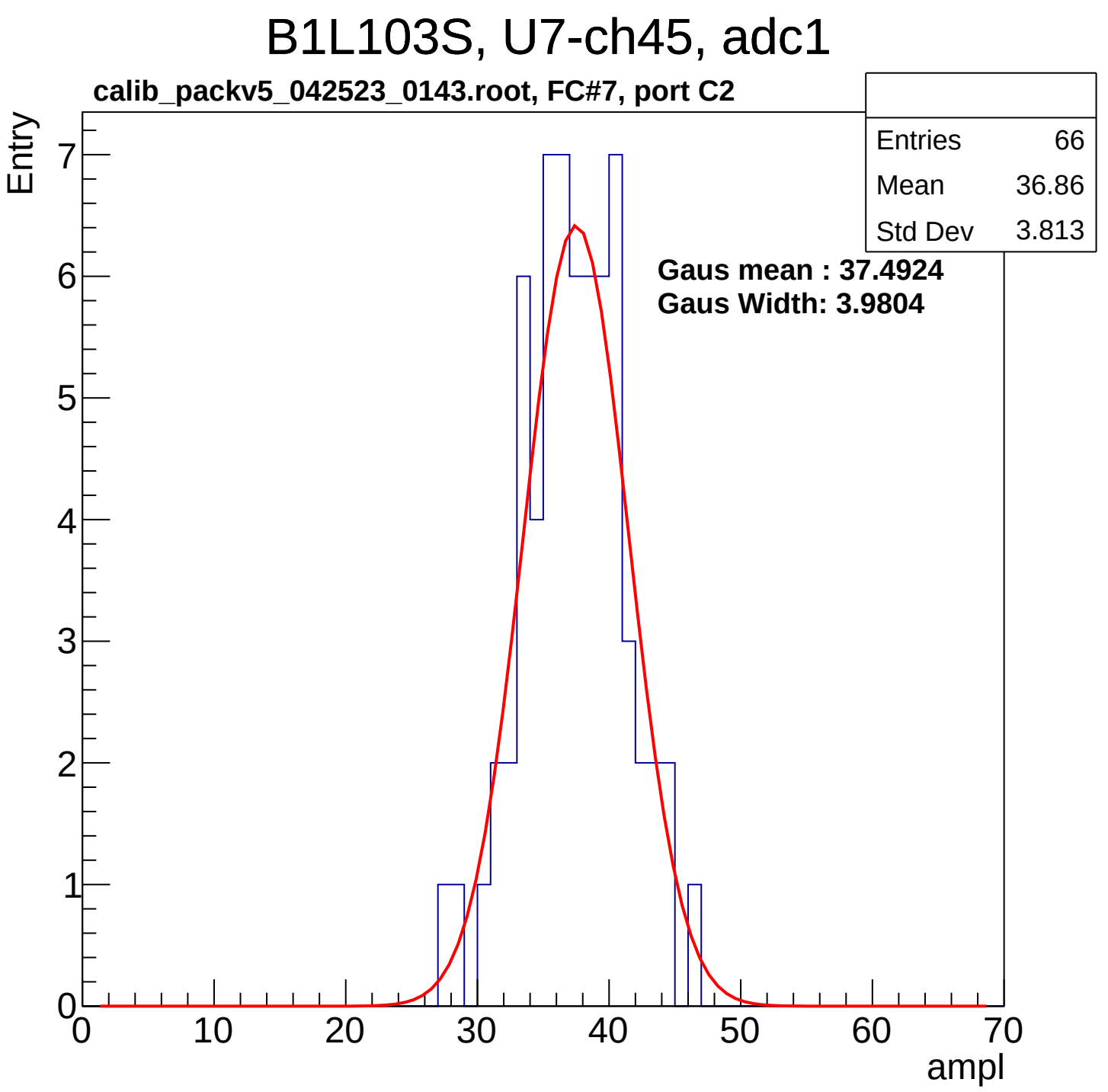
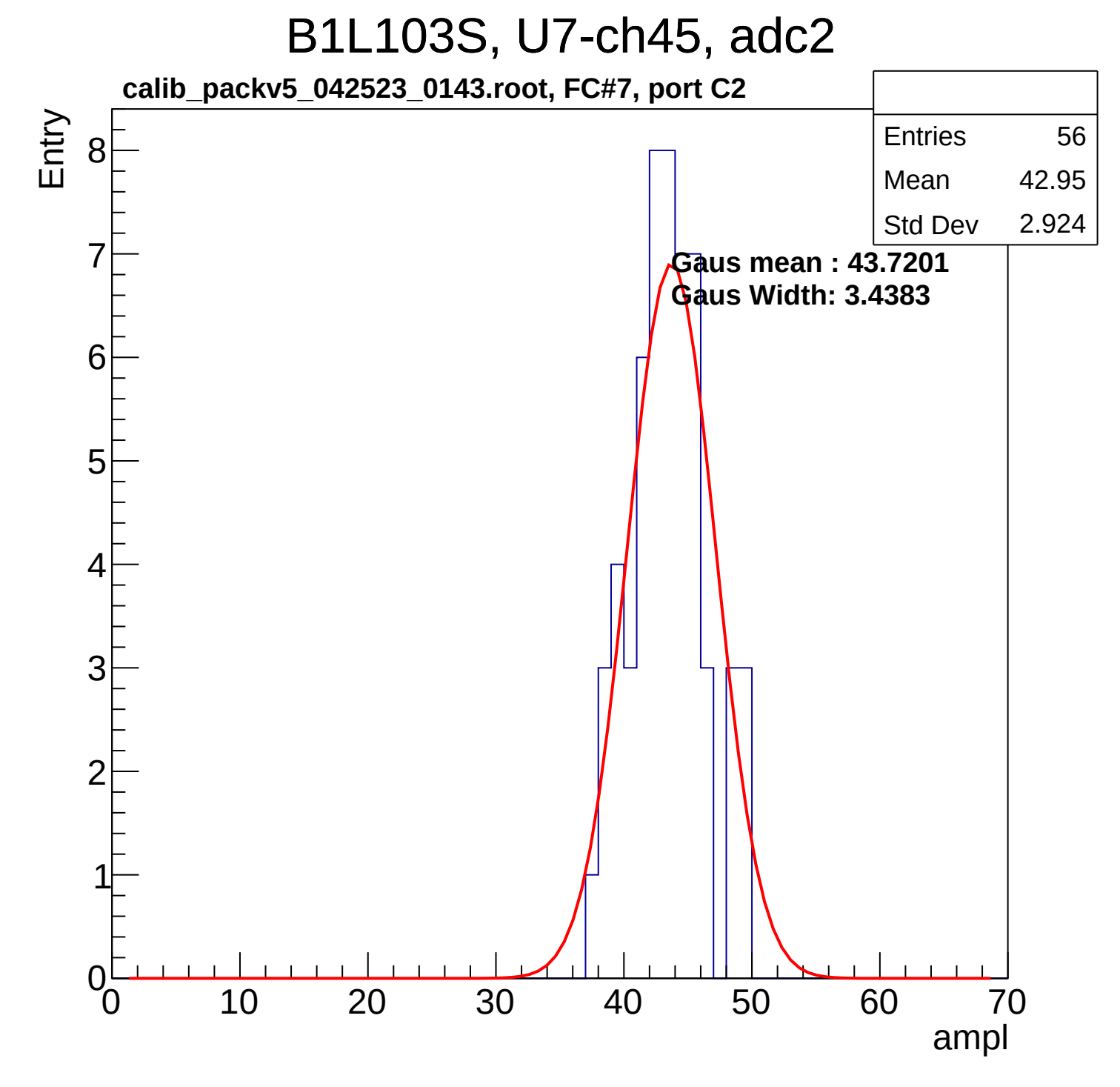
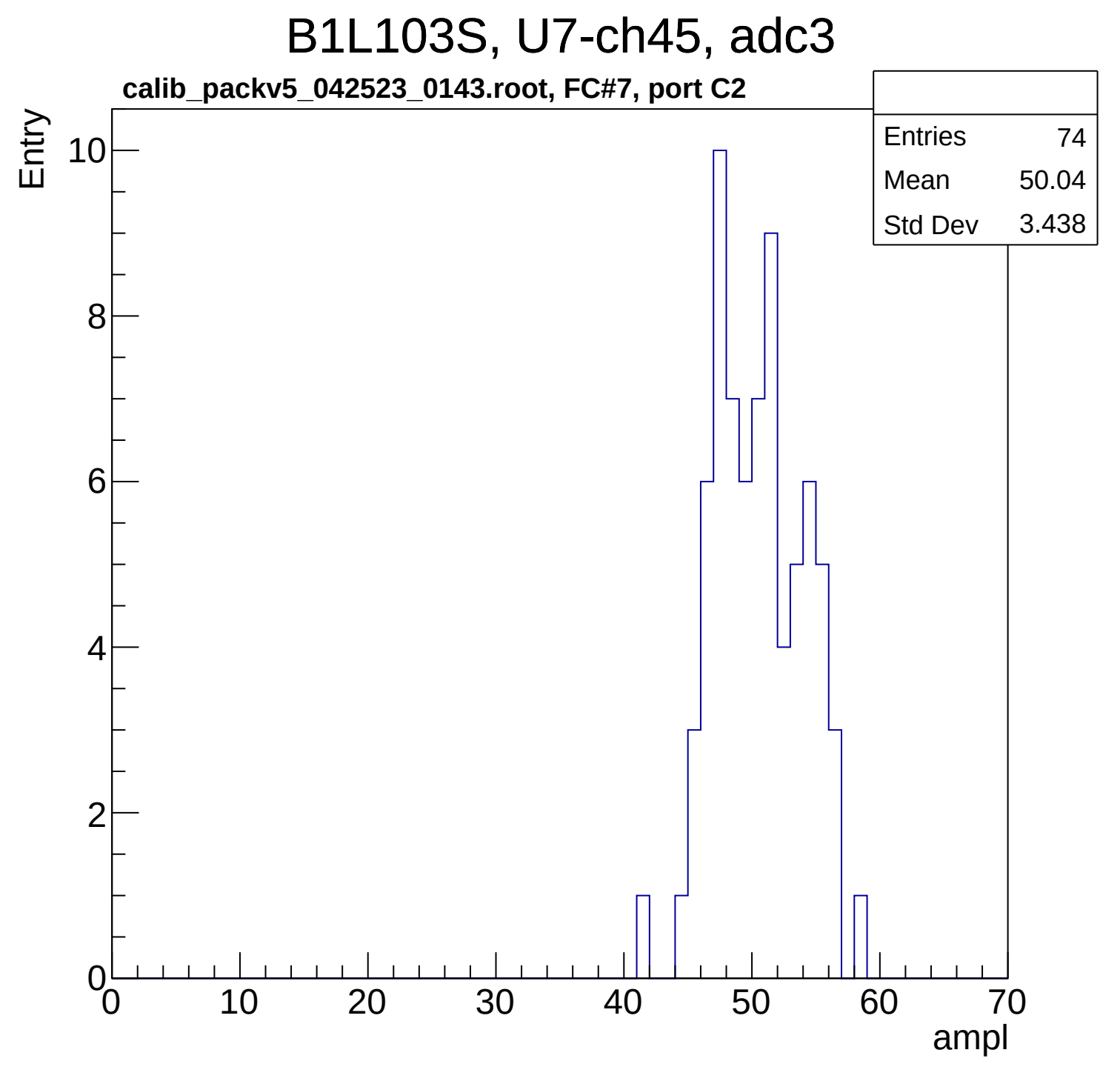
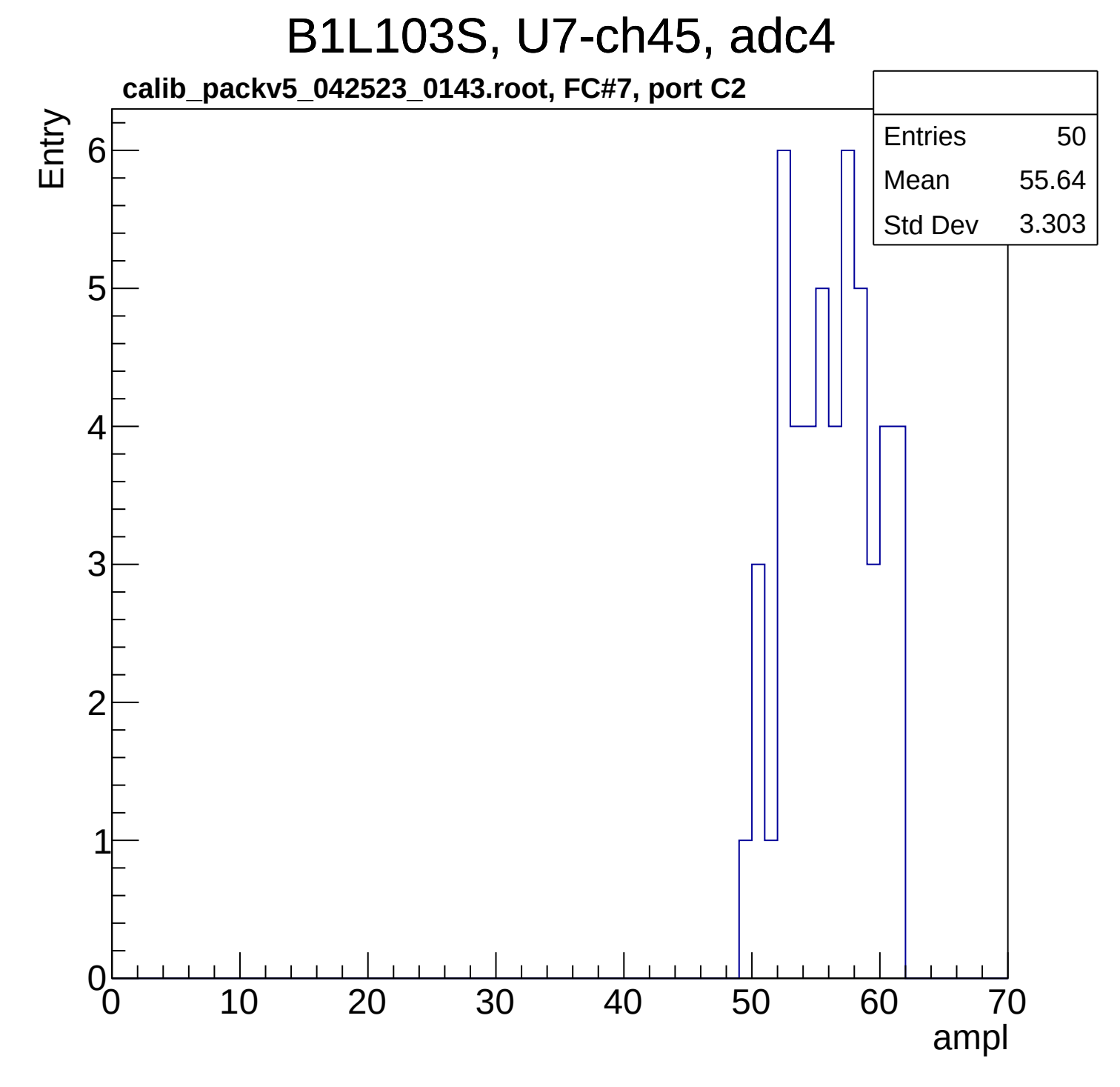
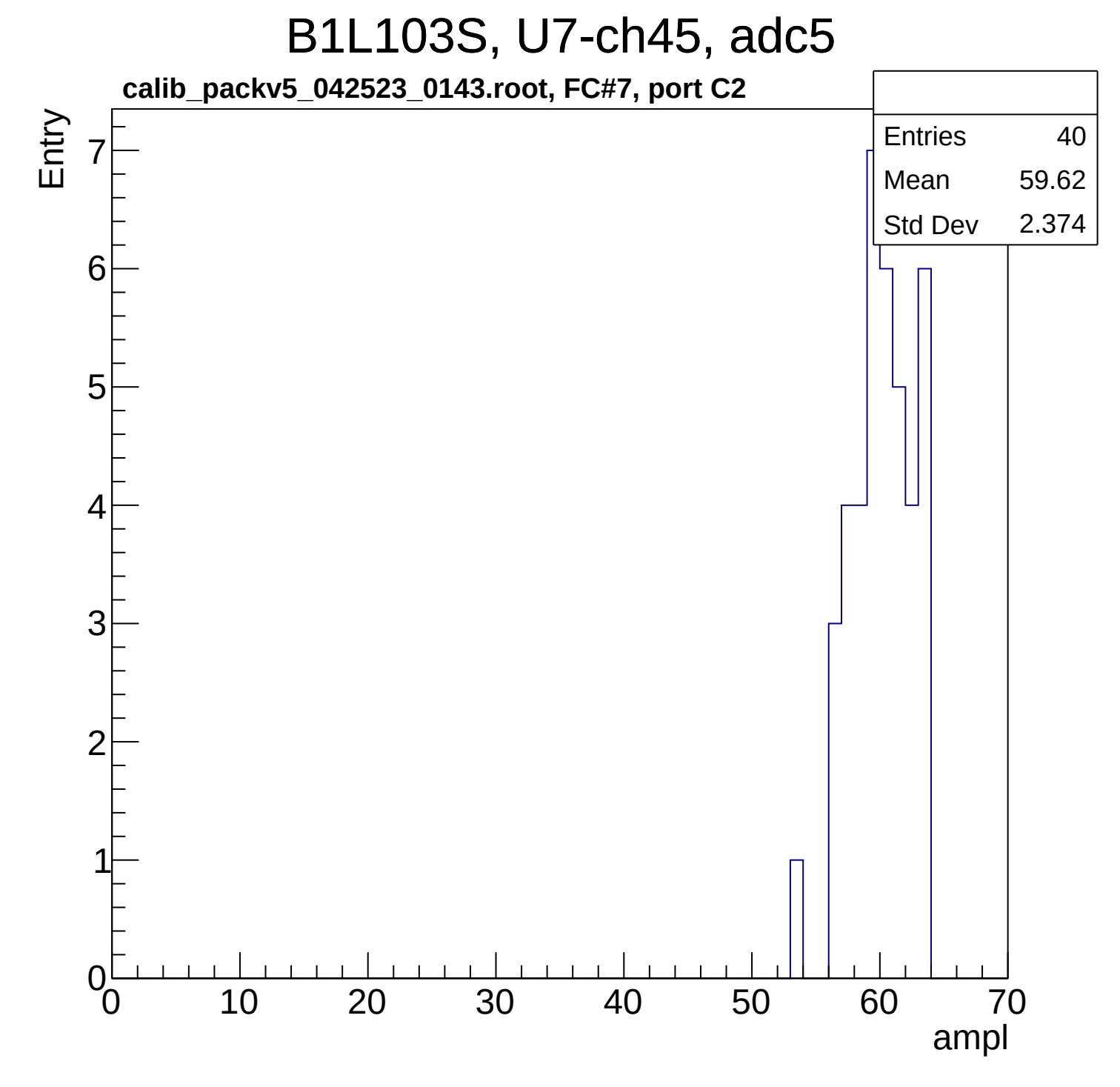

B1L103S, U7-ch45, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 36.86
Std Dev 3.813
Gaus mean : 37.4924
Gaus Width: 3.9804
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch45, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 42.95
Std Dev 2.924
Gaus mean : 43.7201
Gaus Width: 3.4383
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch45, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 74
Mean 50.04
Std Dev 3.438
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch45, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 50
Mean 55.64
Std Dev 3.303
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U7-ch45, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 40
Mean 59.62
Std Dev 2.374
Entry
ampl
0
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2
3
4
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0
10
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40
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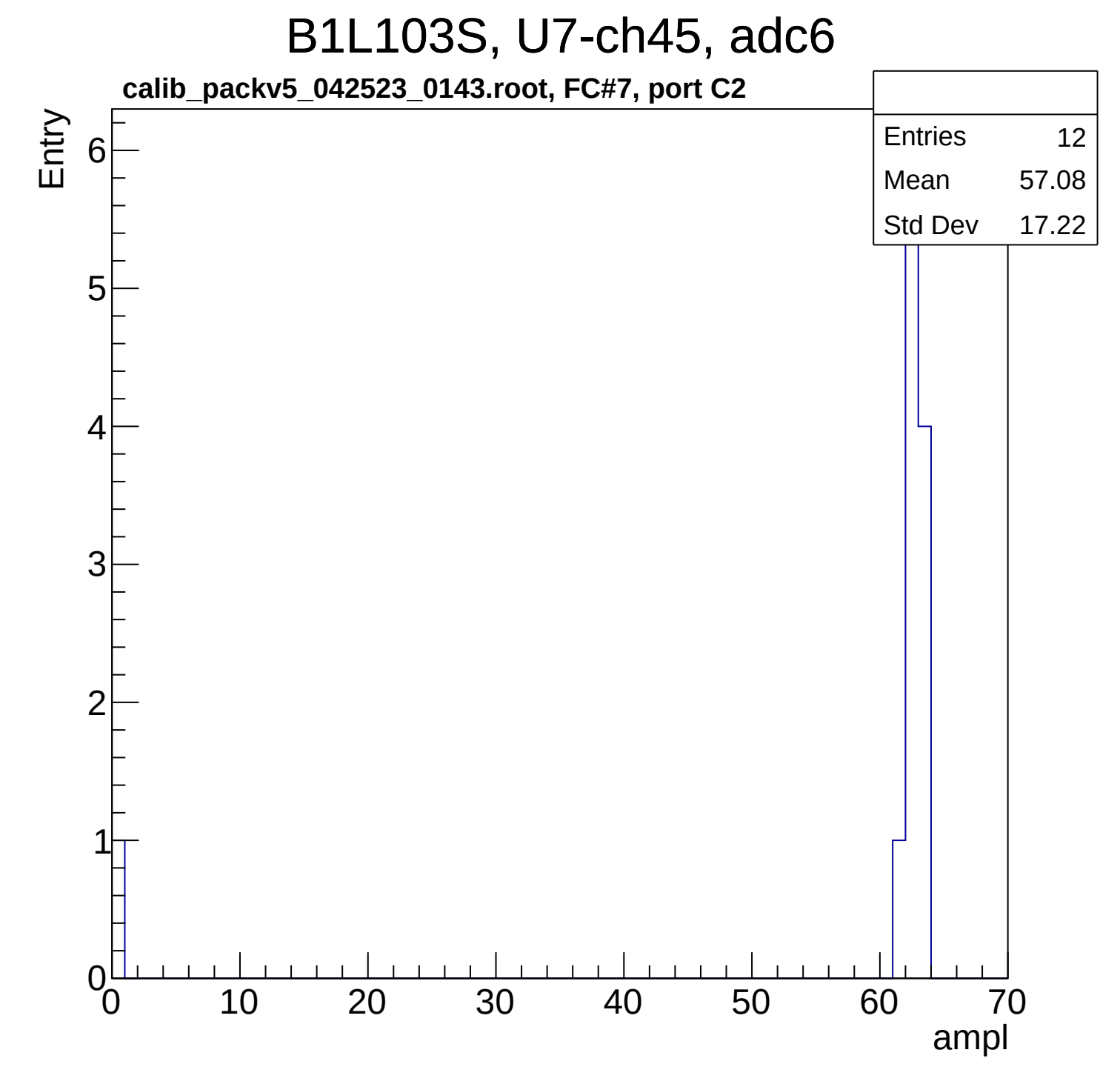
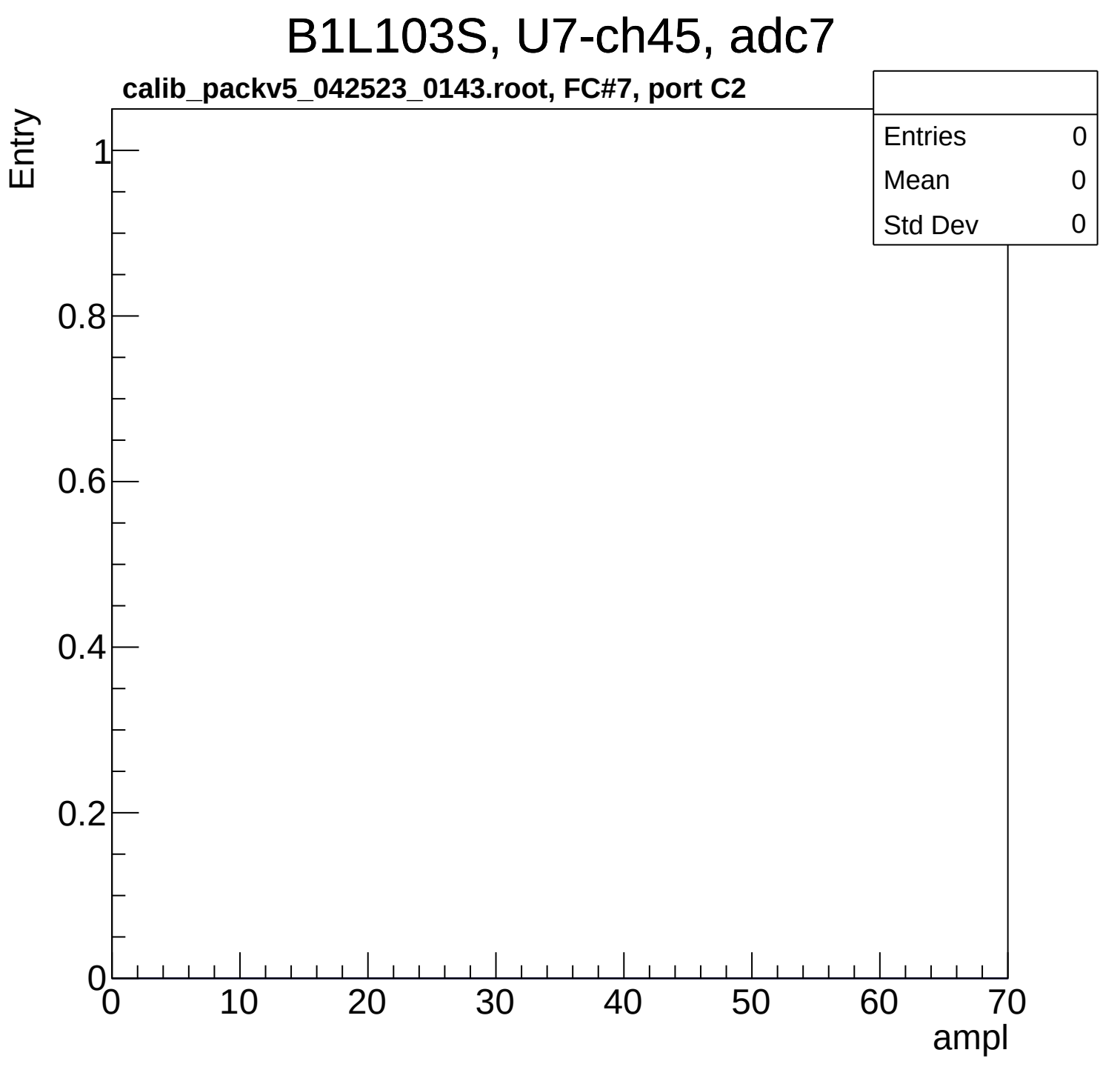
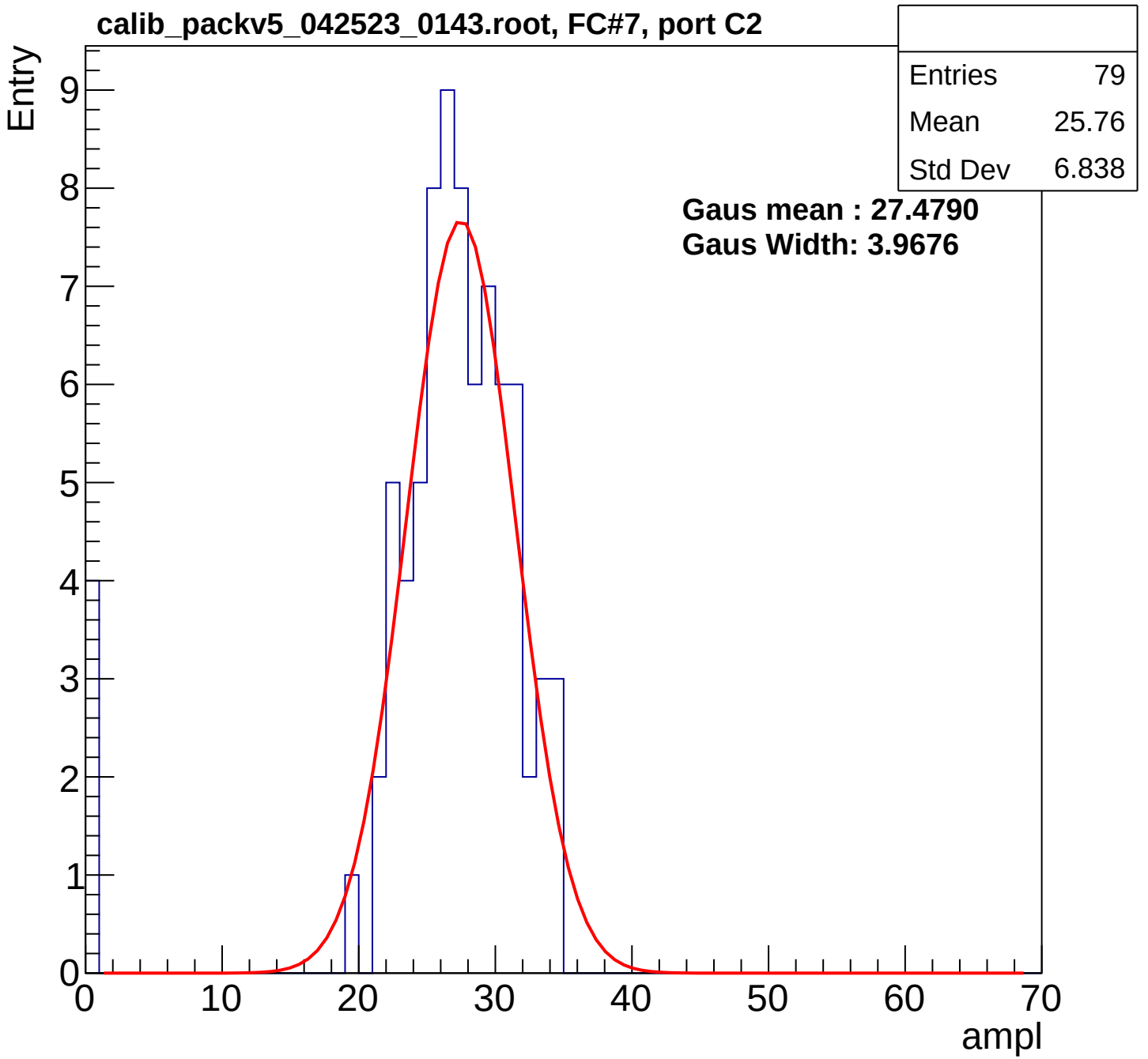
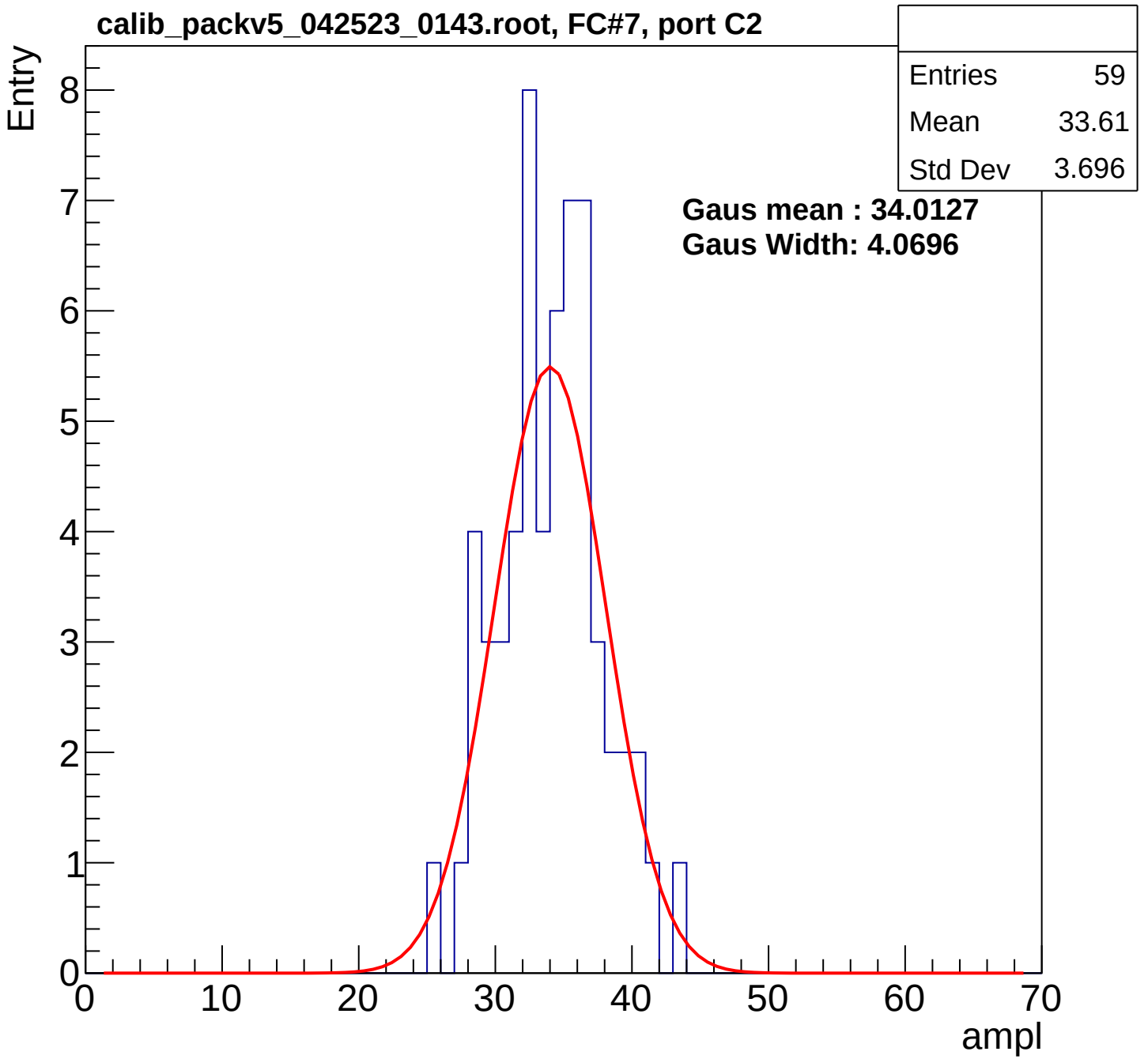
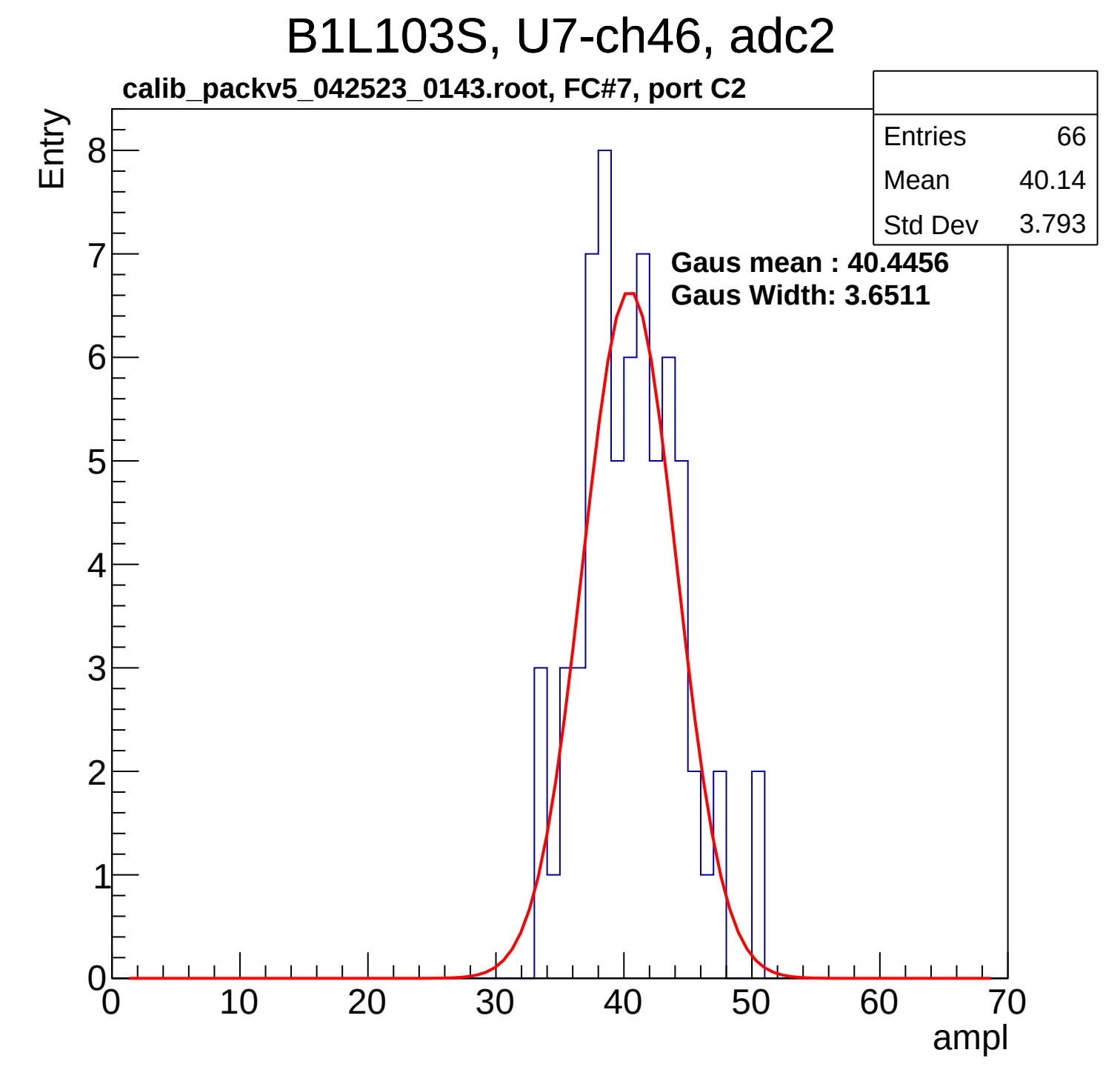
60
70

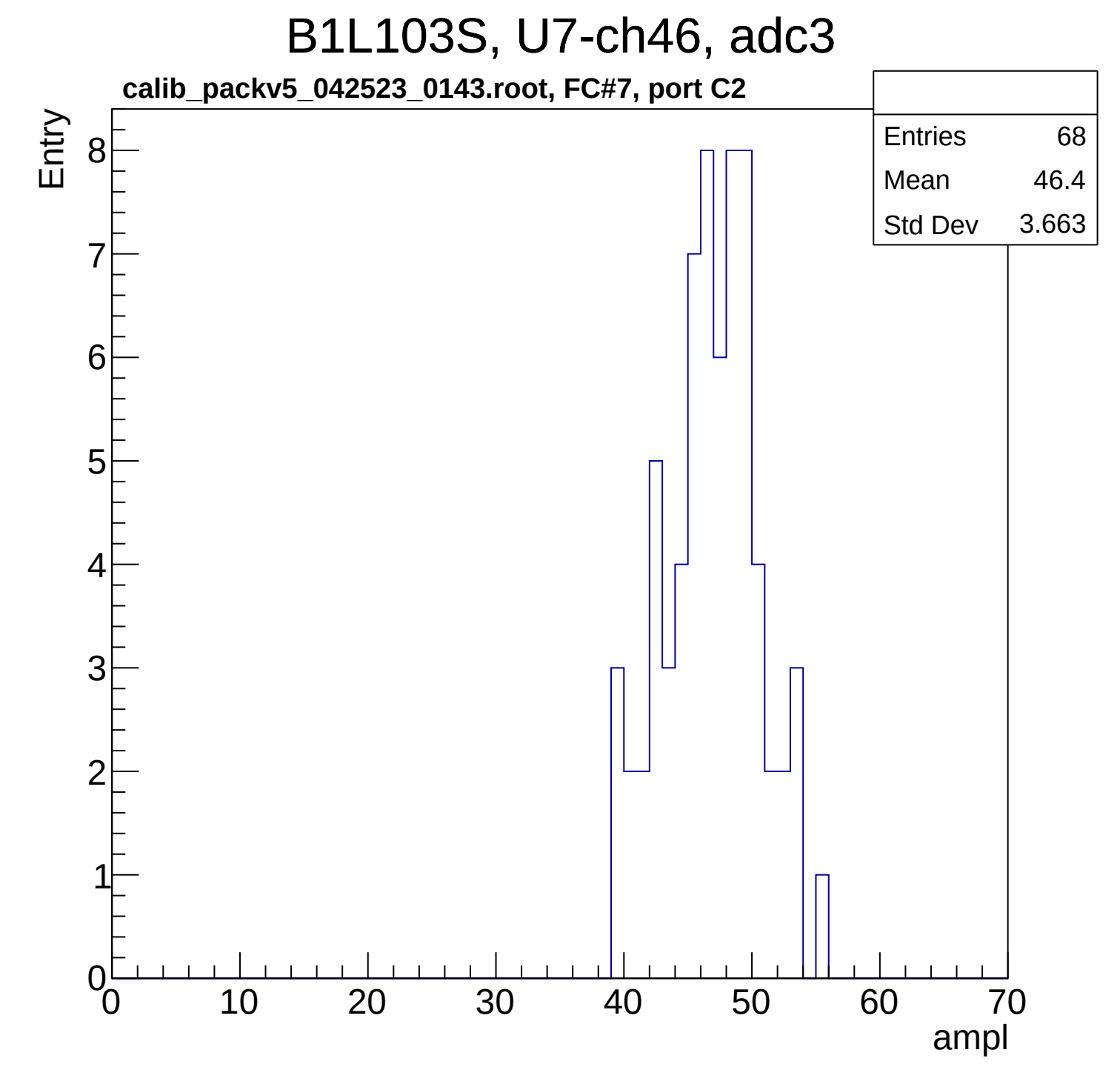

B1L103S, U7-ch45, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 12
Mean 57.08
Std Dev 17.22
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U7-ch45, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch46, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 79
Mean 25.76
Std Dev 6.838
Gaus mean : 27.4790
Gaus Width: 3.9676
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch46, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 33.61
Std Dev 3.696
Gaus mean : 34.0127
Gaus Width: 4.0696
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch46, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 40.14
Std Dev 3.793
Gaus mean : 40.4456
Gaus Width: 3.6511
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch46, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 46.4
Std Dev 3.663
Entry
ampl
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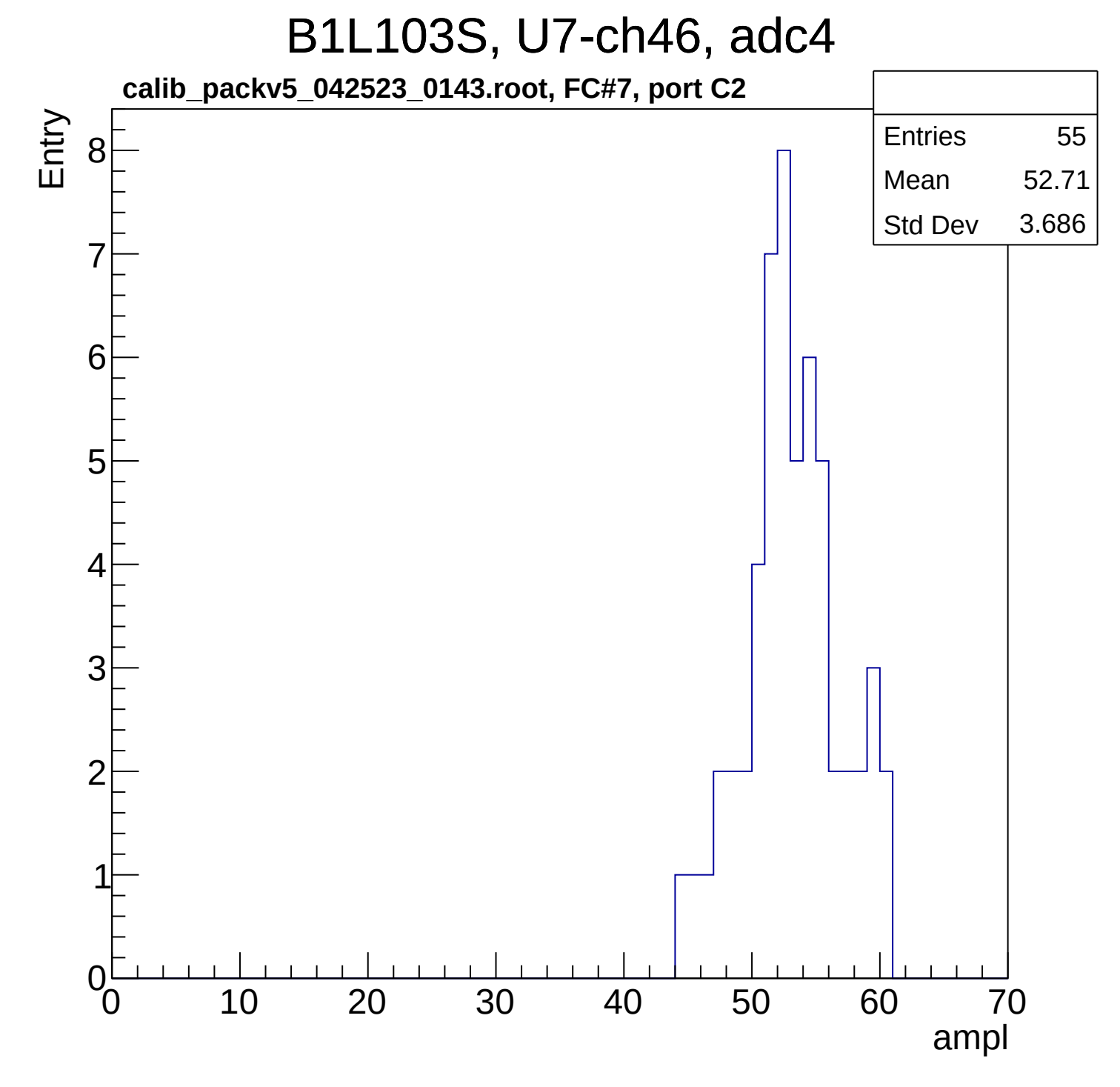
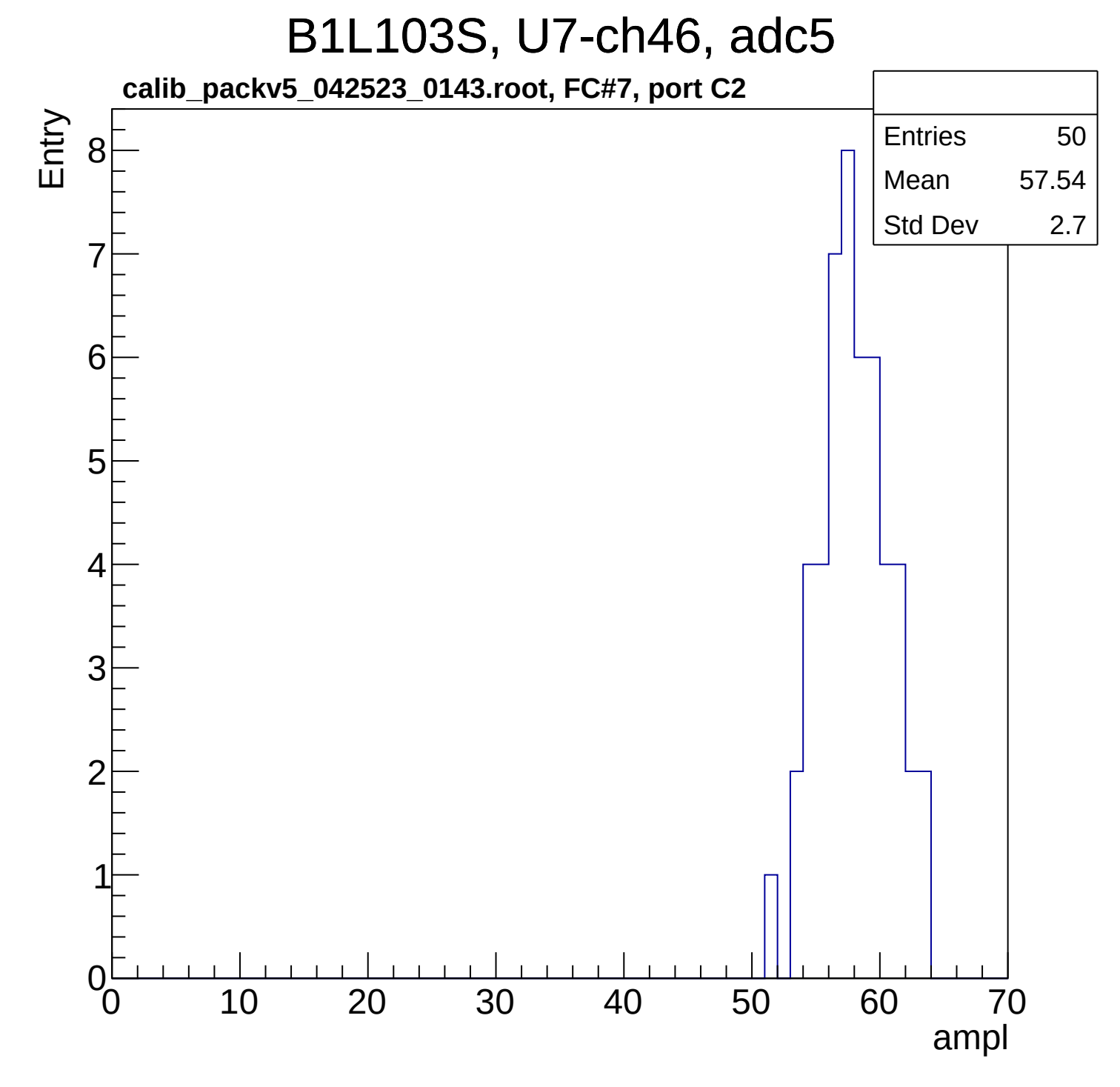
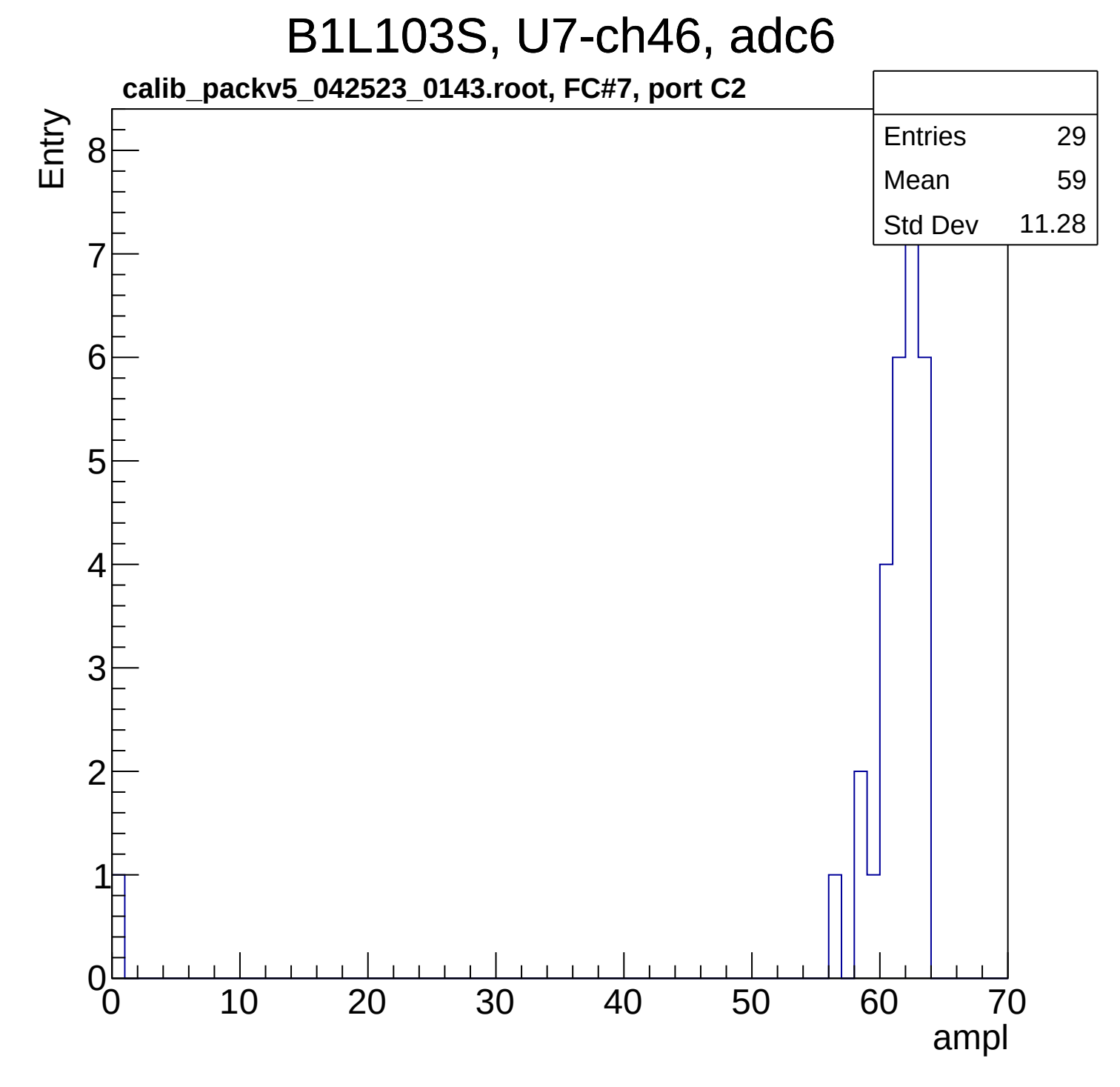
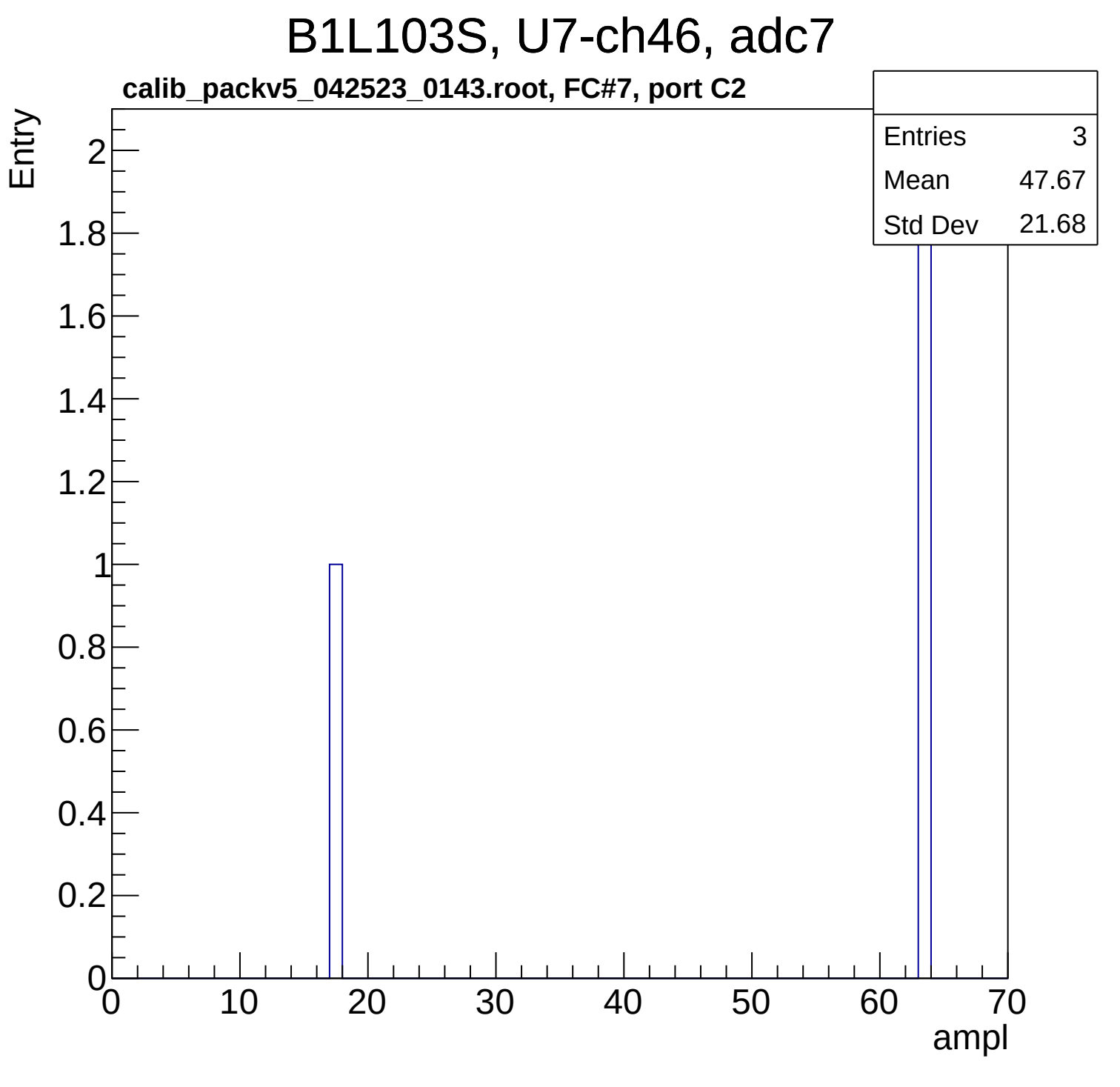
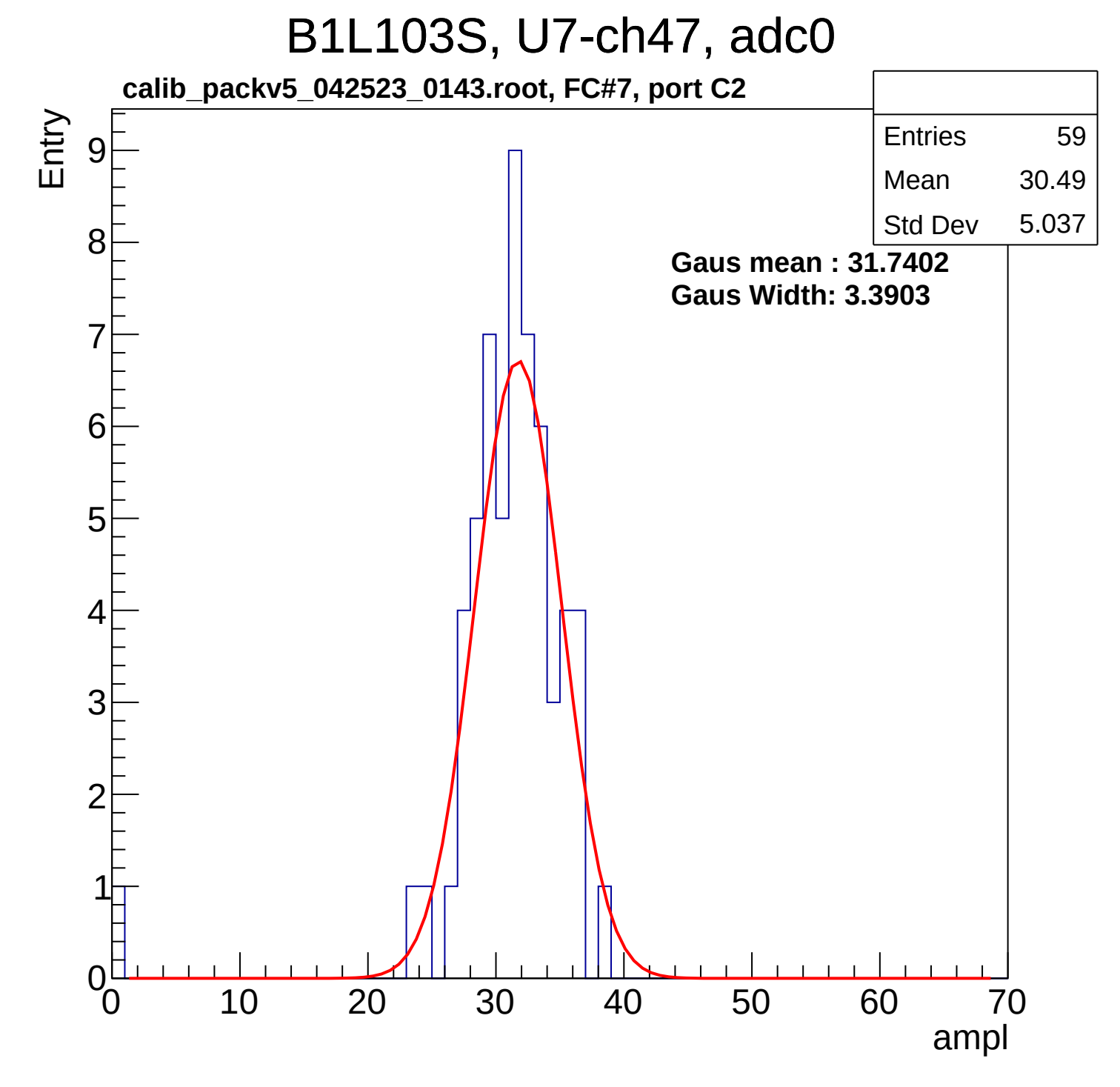
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

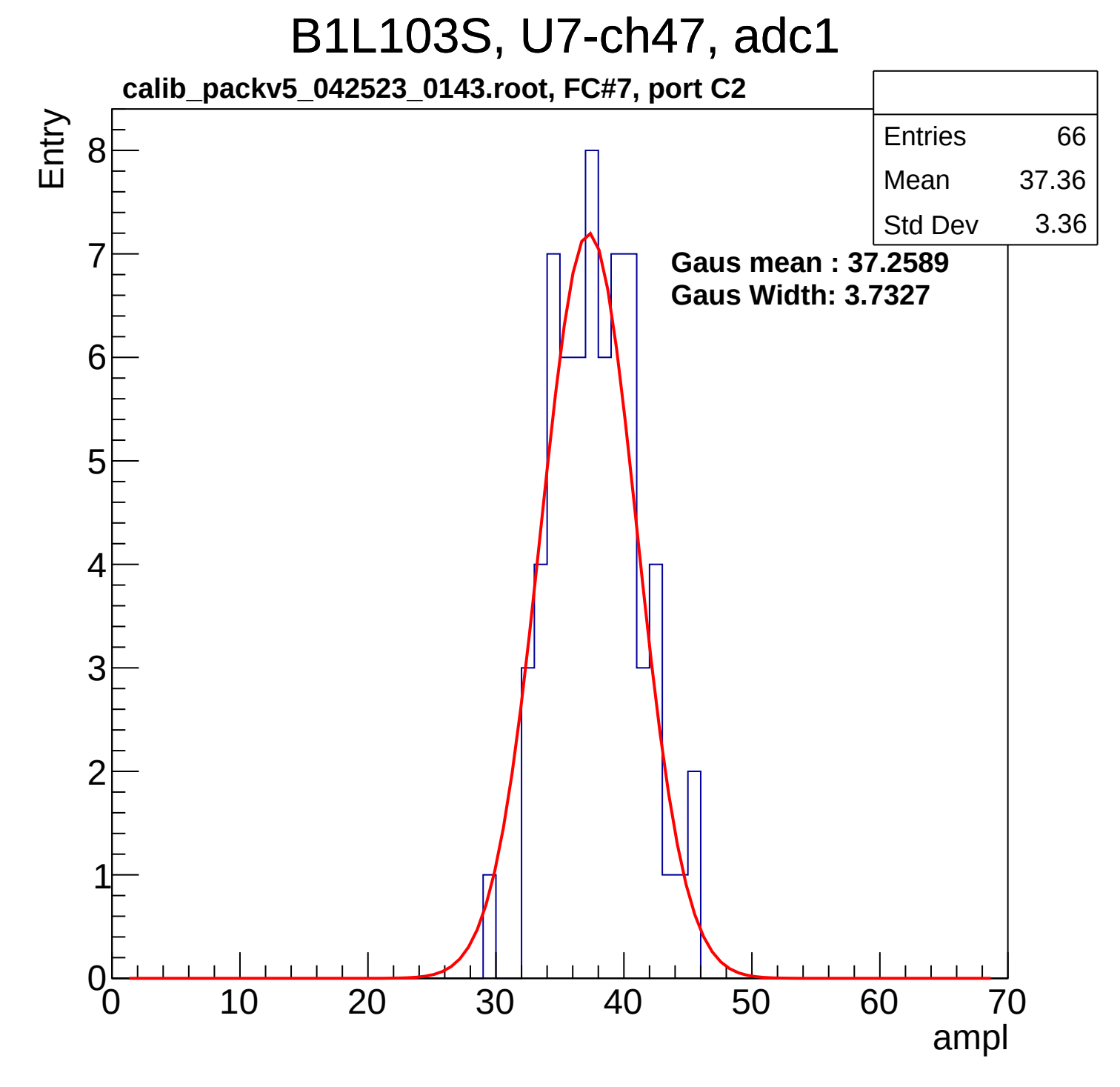

B1L103S, U7-ch46, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 52.71
Std Dev 3.686
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

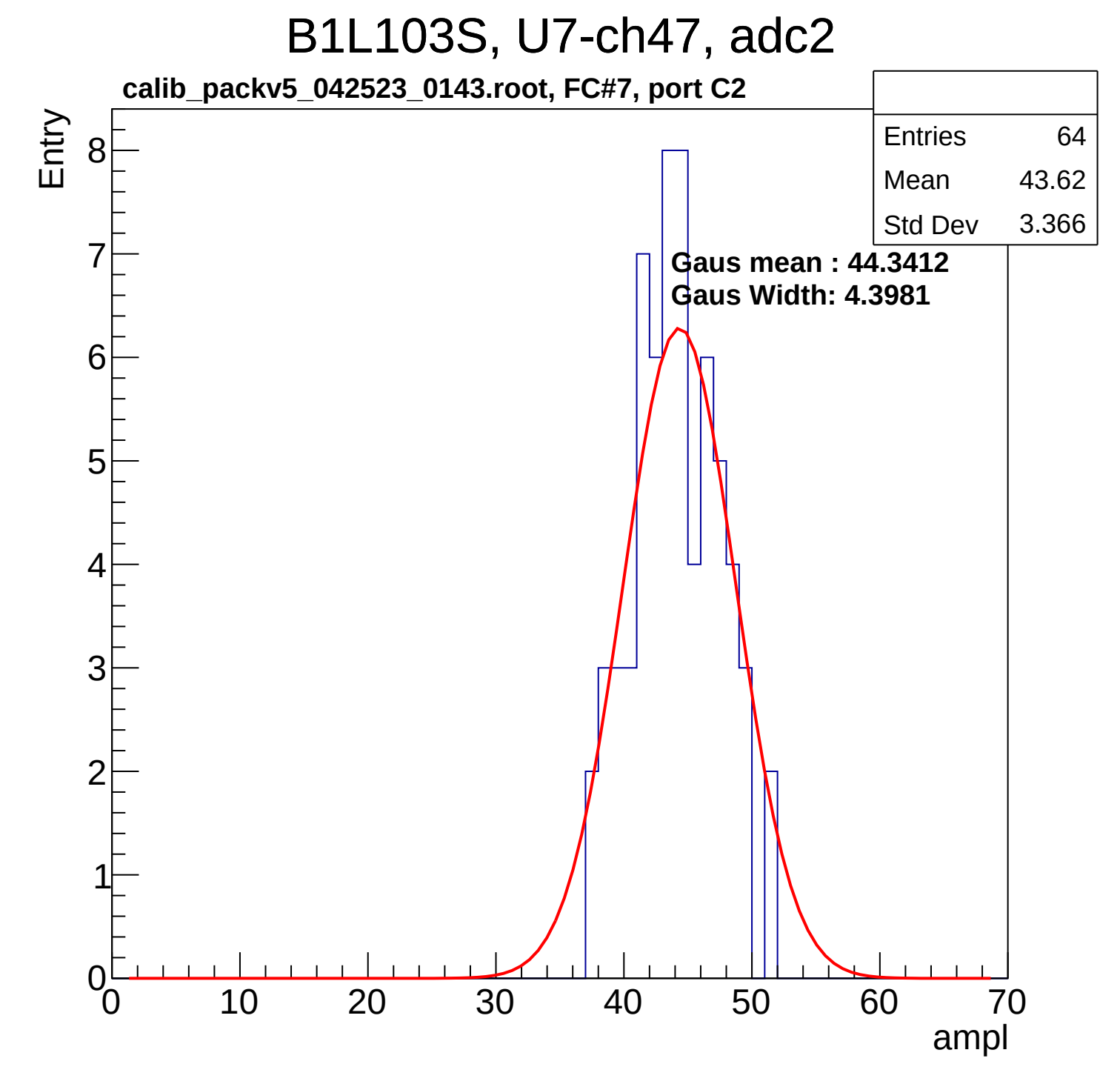

B1L103S, U7-ch46, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 50
Mean 57.54
Std Dev 2.7
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

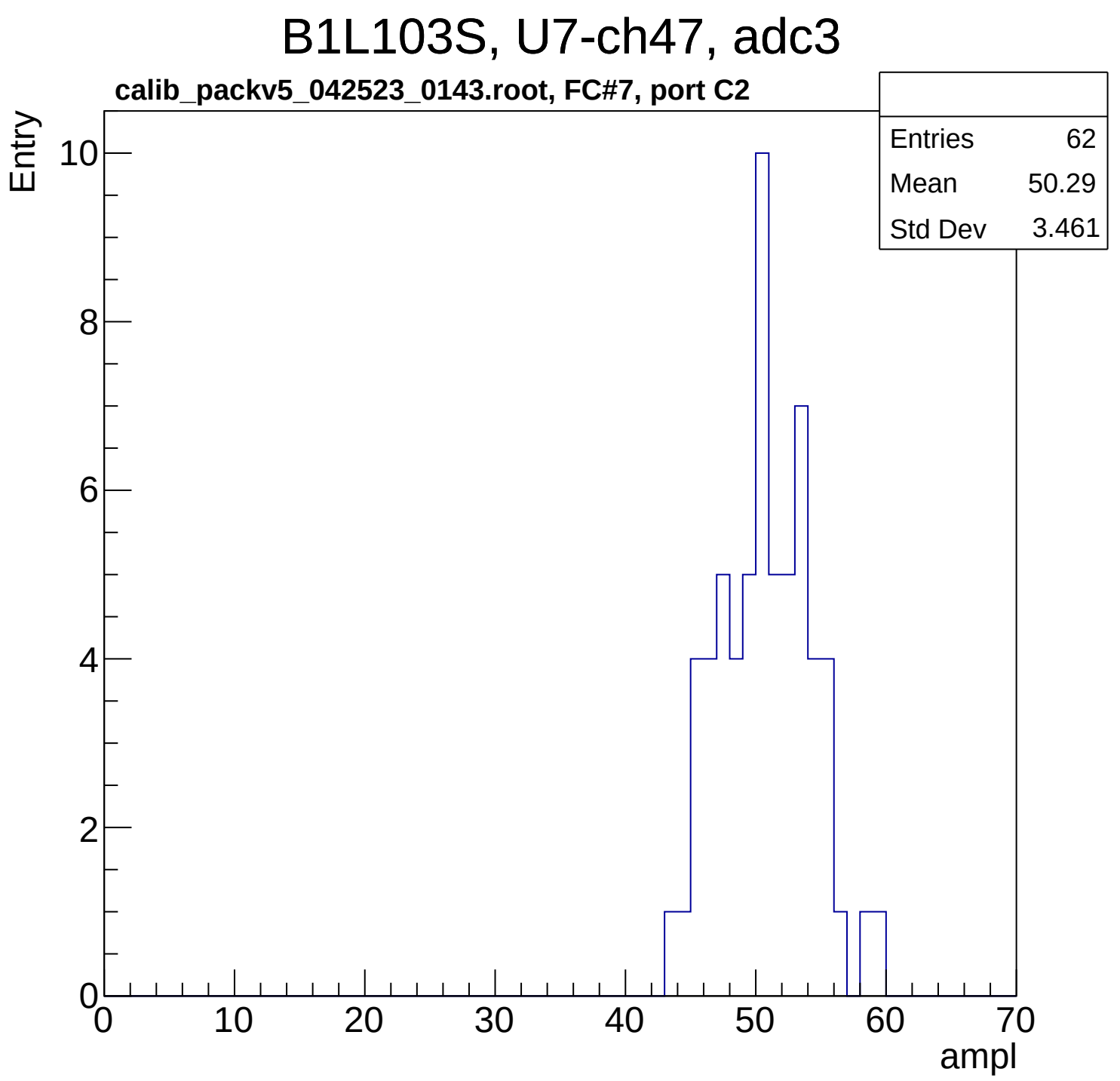

B1L103S, U7-ch46, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 29
Mean 59
Std Dev 11.28
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

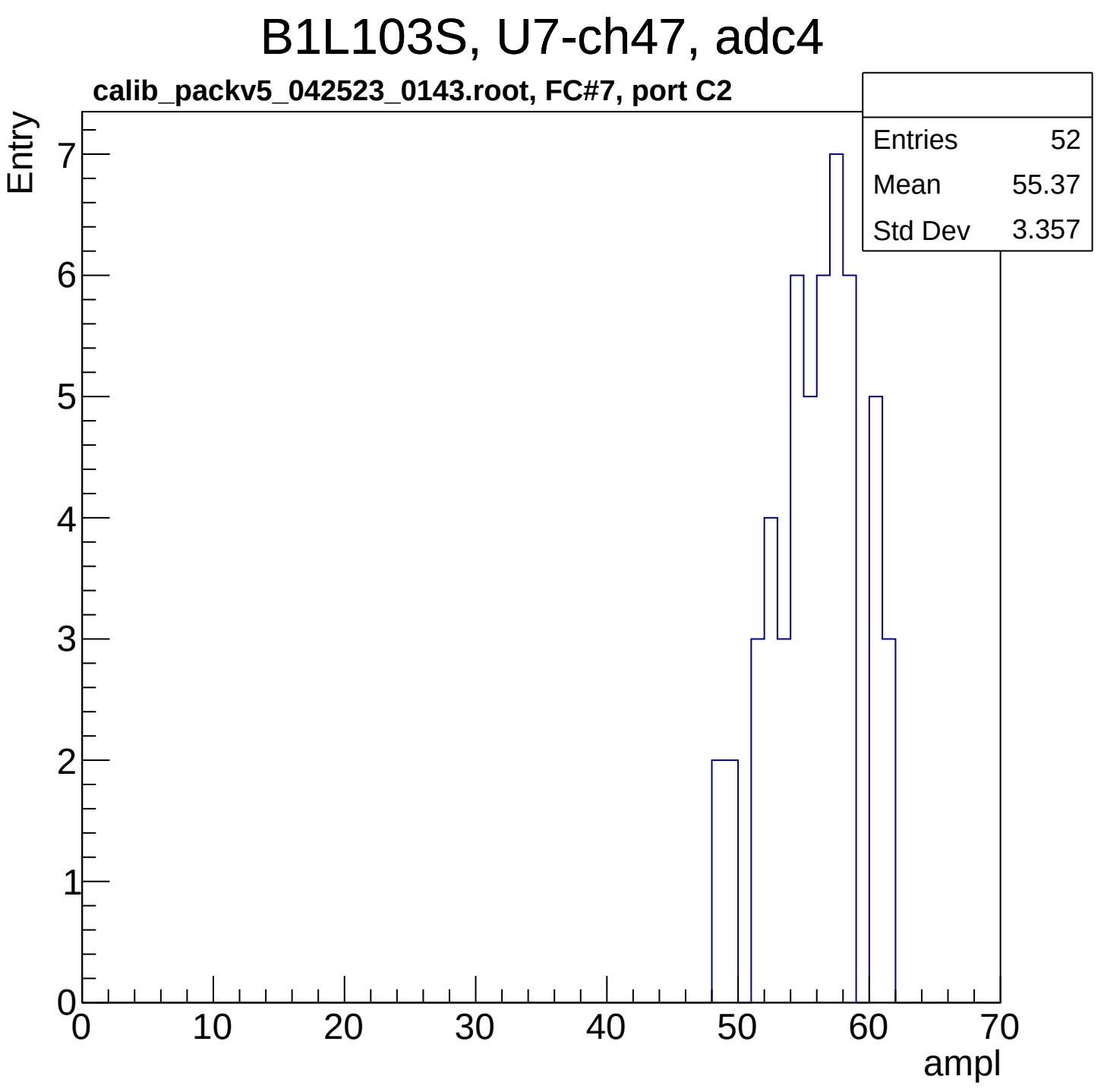

B1L103S, U7-ch46, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 47.67
Std Dev 21.68
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

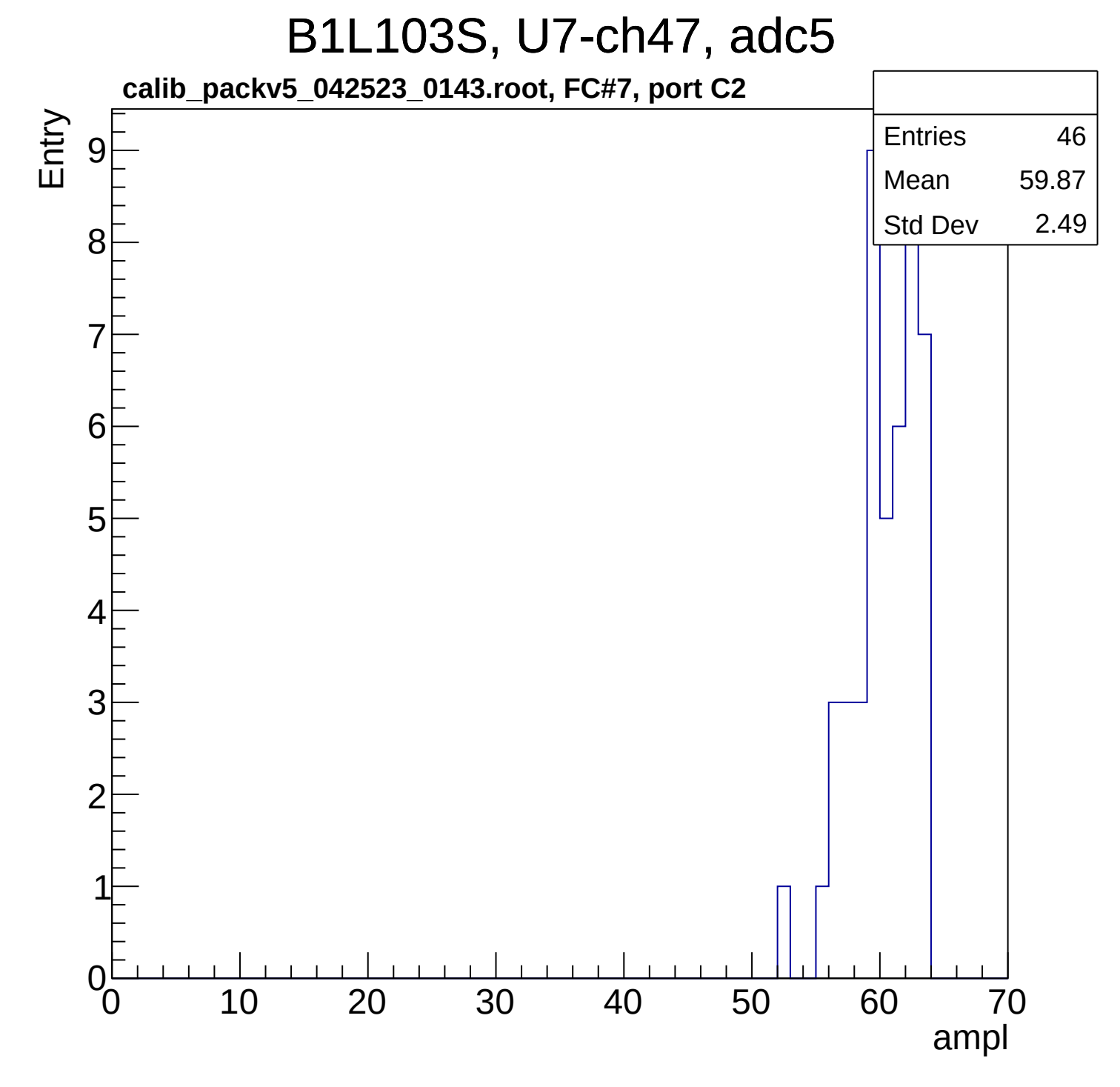

B1L103S, U7-ch47, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 30.49
Std Dev 5.037
Gaus mean : 31.7402
Gaus Width: 3.3903
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch47, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 37.36
Std Dev 3.36
Gaus mean : 37.2589
Gaus Width: 3.7327
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch47, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 43.62
Std Dev 3.366
Gaus mean : 44.3412
Gaus Width: 4.3981
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch47, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 62
Mean 50.29
Std Dev 3.461
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch47, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 52
Mean 55.37
Std Dev 3.357
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch47, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 46
Mean 59.87
Std Dev 2.49
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
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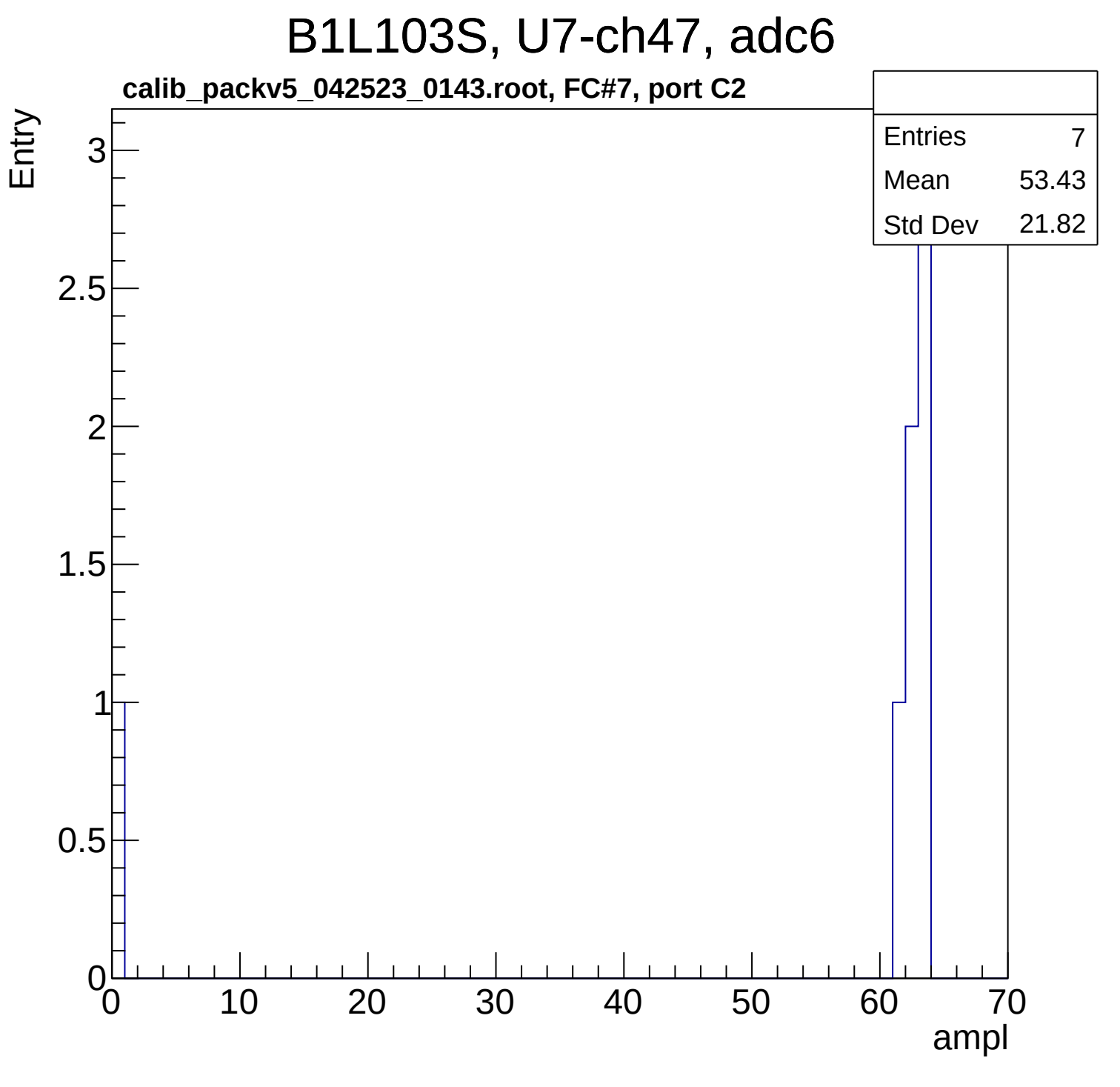
60
70


B1L103S, U7-ch47, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 7
Mean 53.43
Std Dev 21.82
Entry
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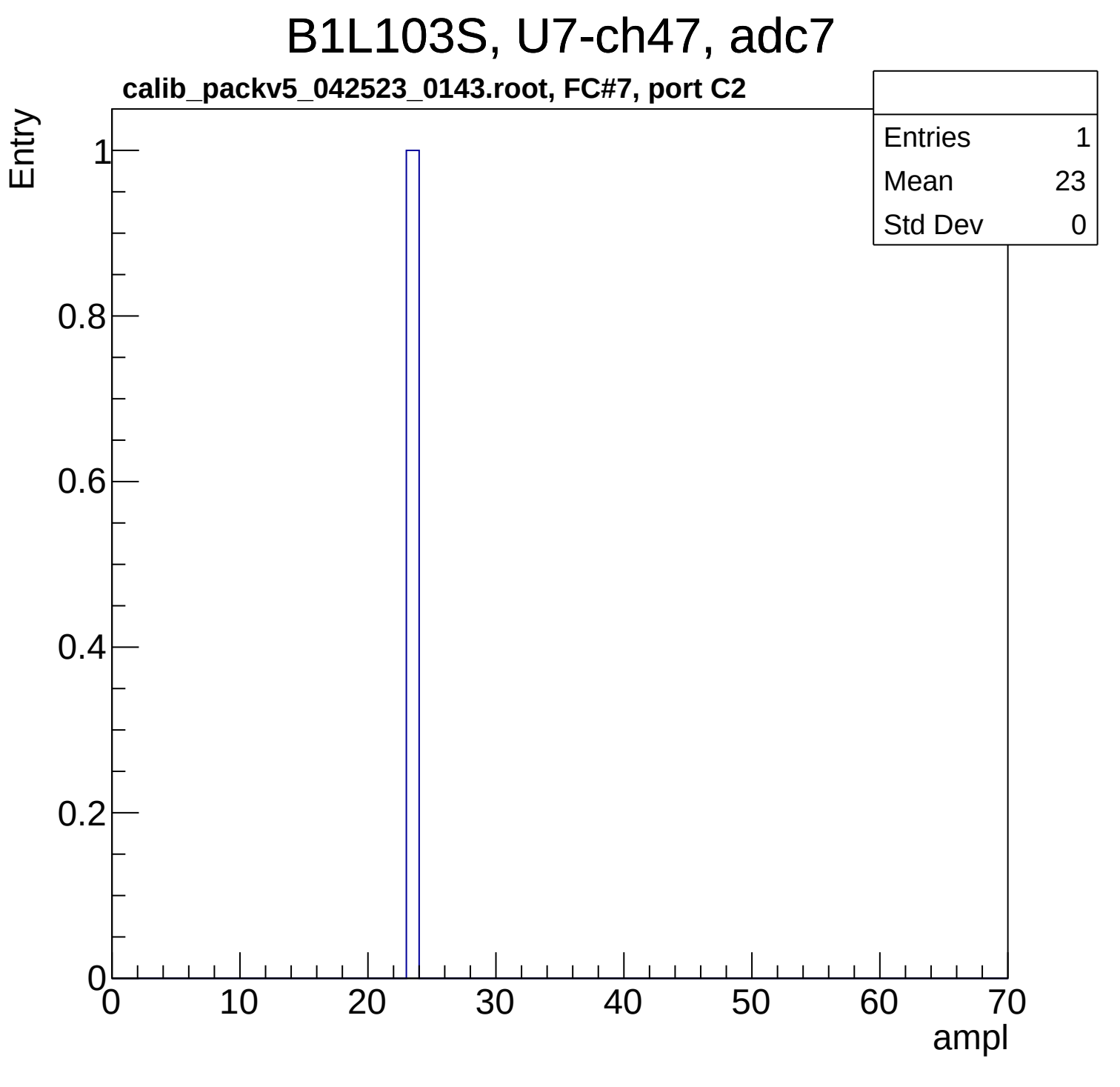
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch47, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 23
Std Dev 0
Entry
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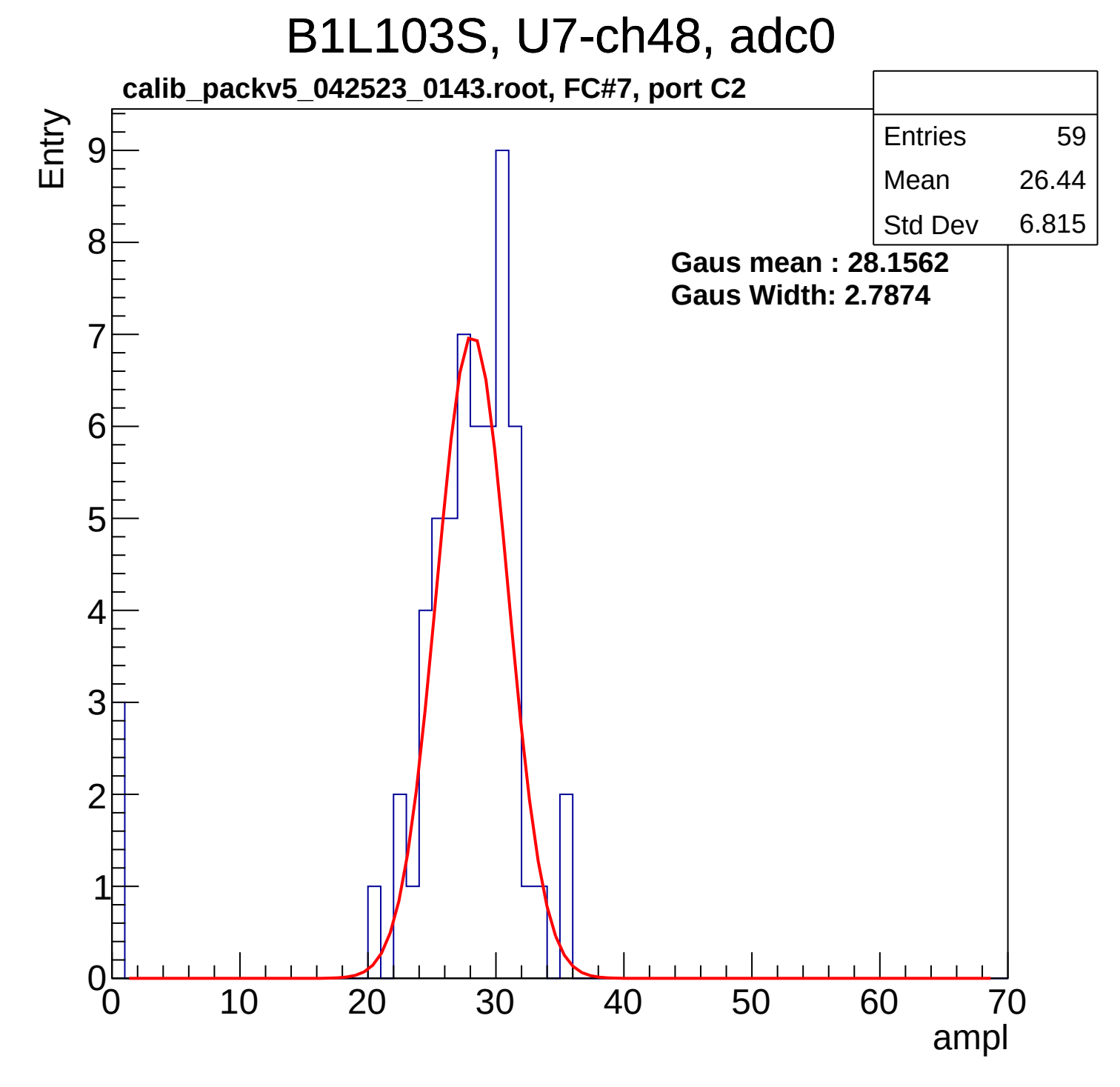
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch48, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 26.44
Std Dev 6.815
Gaus mean : 28.1562
Gaus Width: 2.7874
Entry
ampl
0
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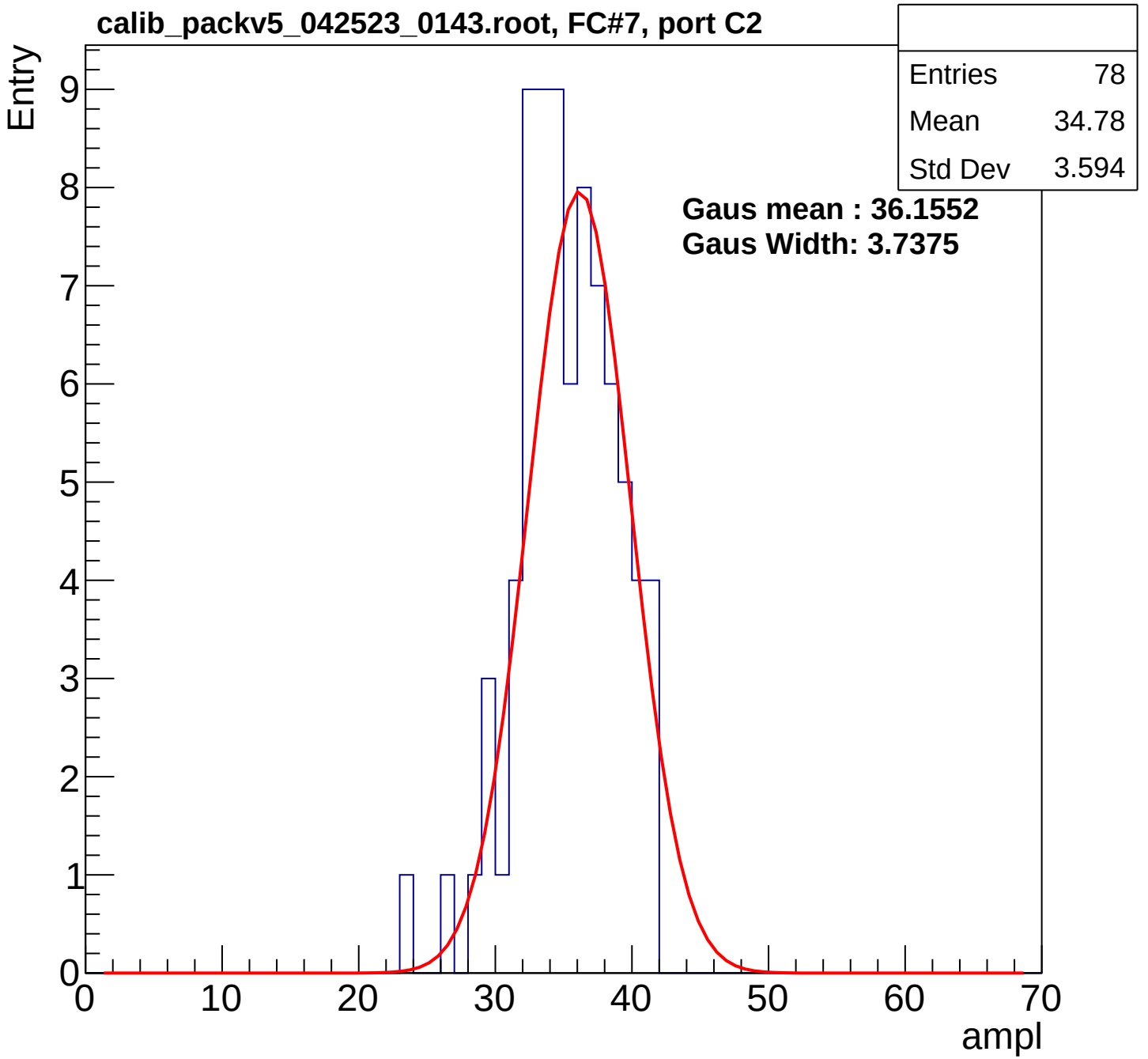
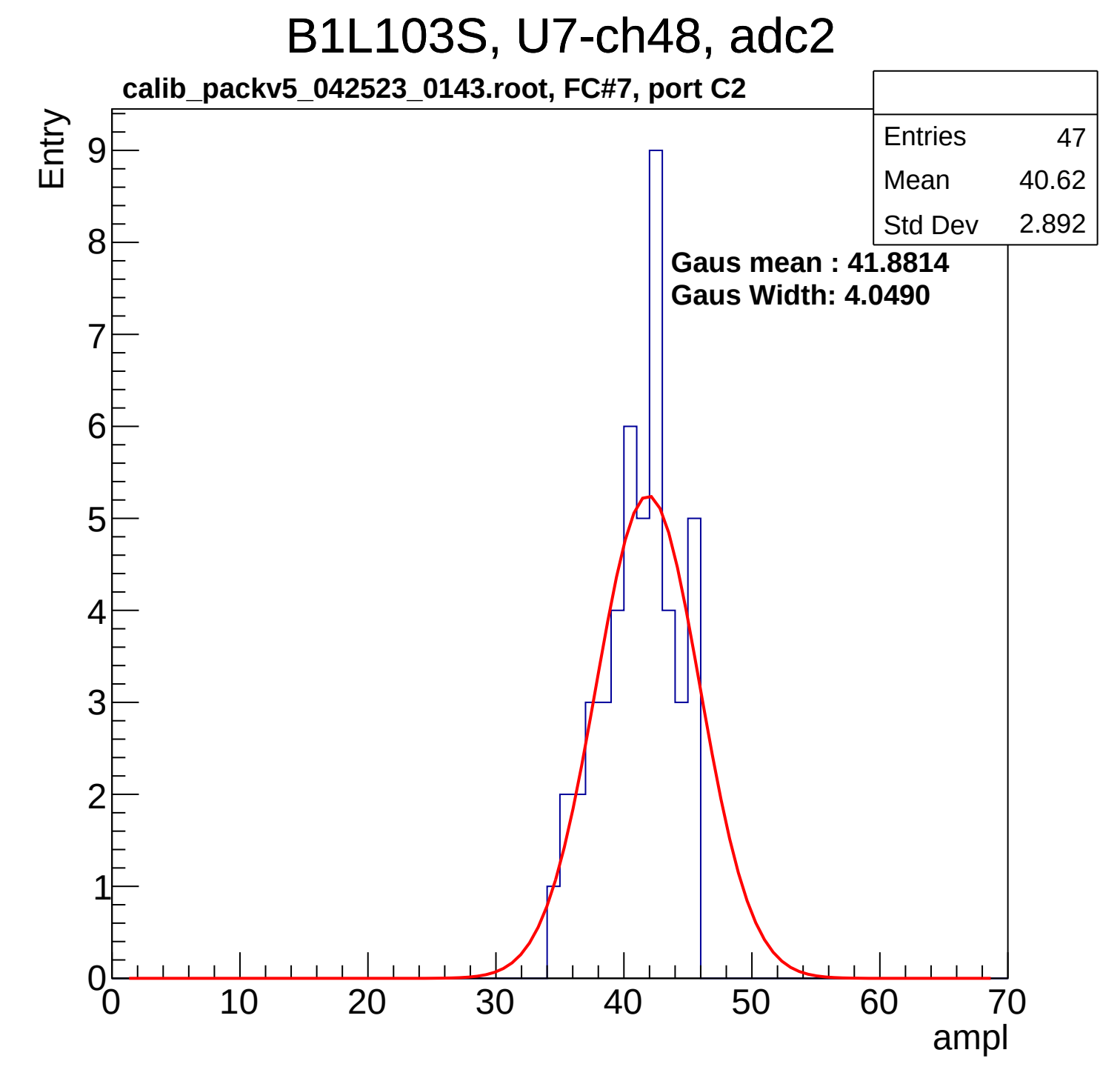
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch48, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 78
Mean 34.78
Std Dev 3.594
Gaus mean : 36.1552
Gaus Width: 3.7375
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch48, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 47
Mean 40.62
Std Dev 2.892
Gaus mean : 41.8814
Gaus Width: 4.0490
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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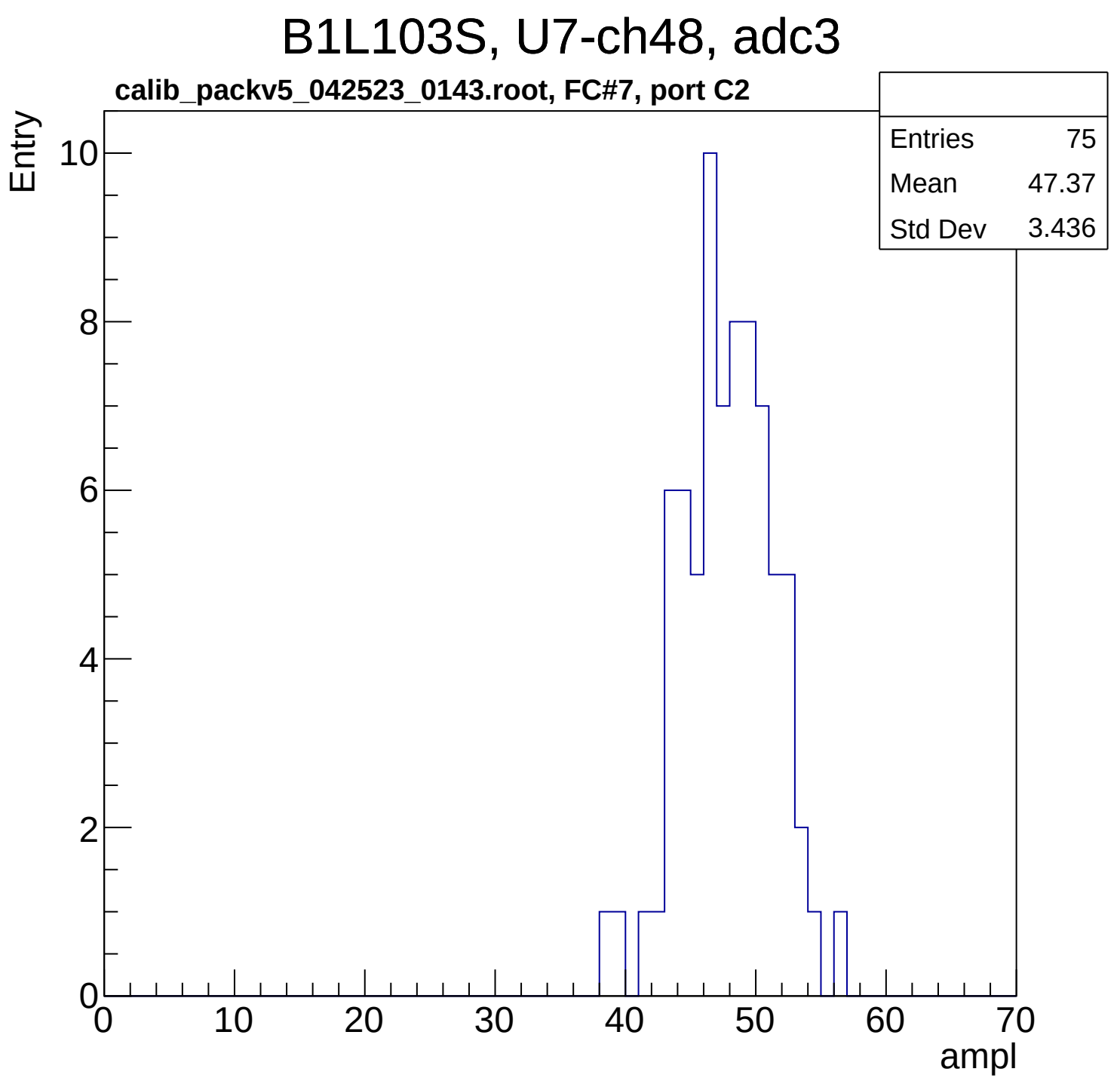
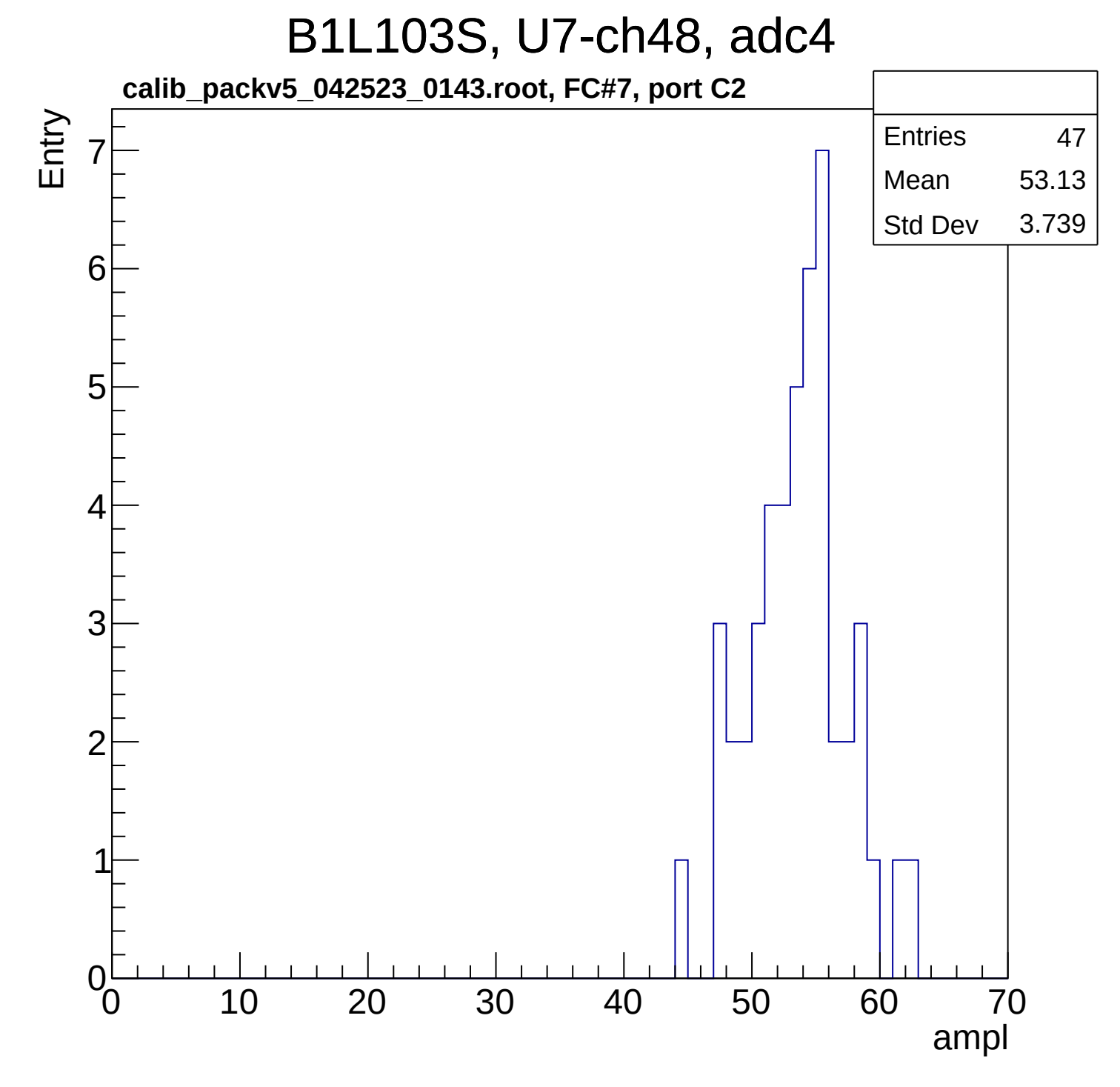
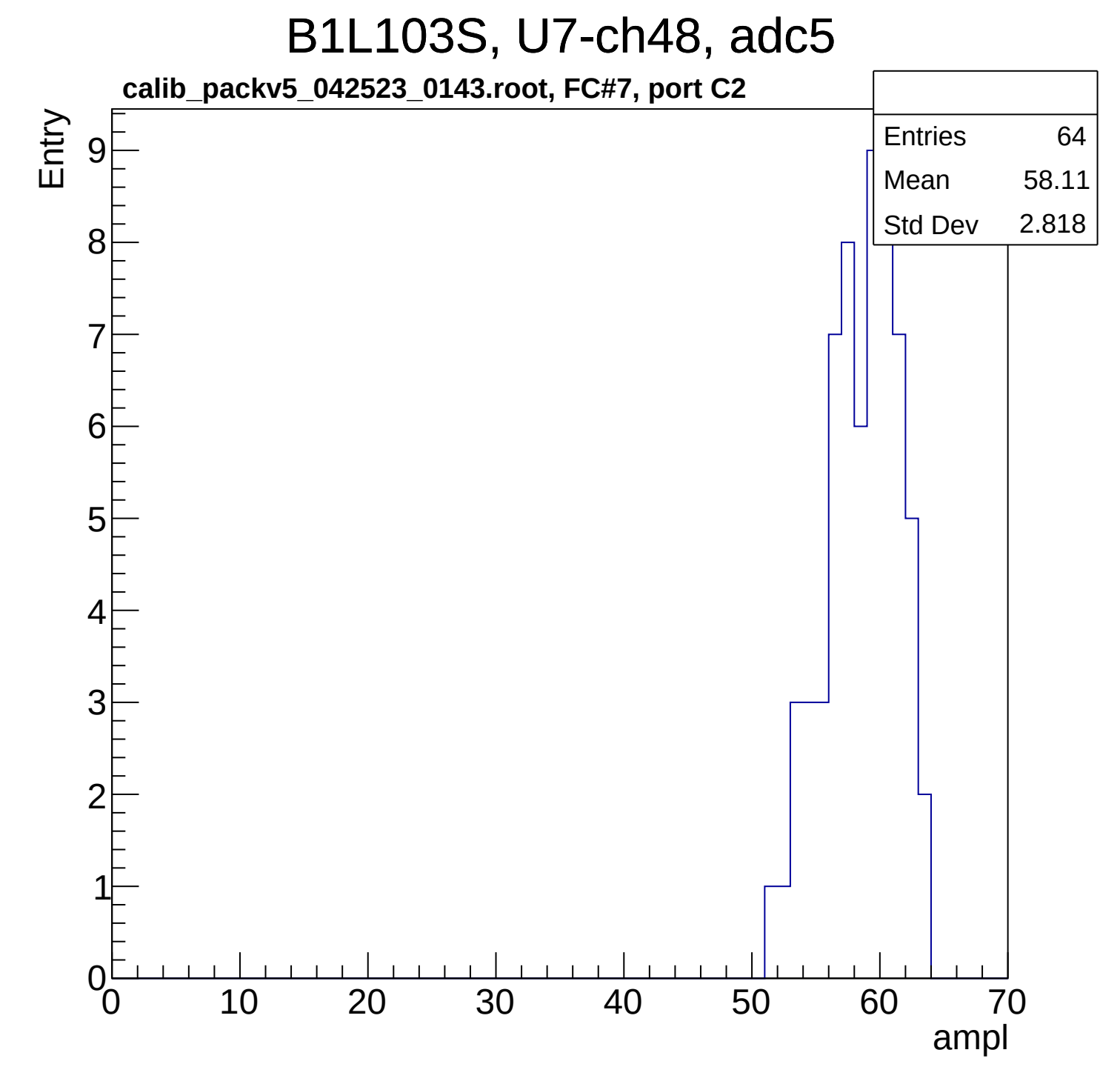

B1L103S, U7-ch48, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 75
Mean 47.37
Std Dev 3.436
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch48, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 47
Mean 53.13
Std Dev 3.739
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch48, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 58.11
Std Dev 2.818
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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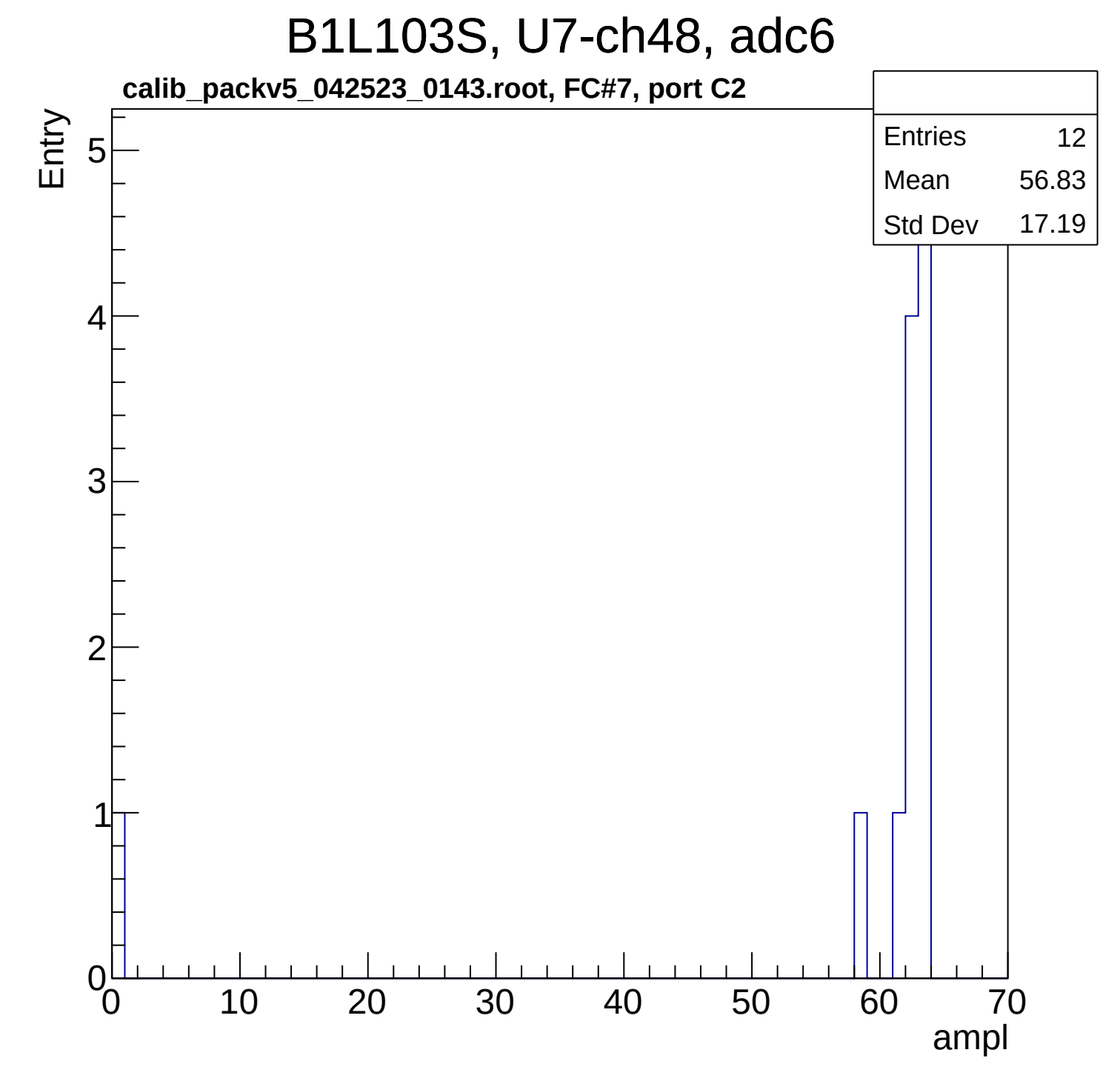
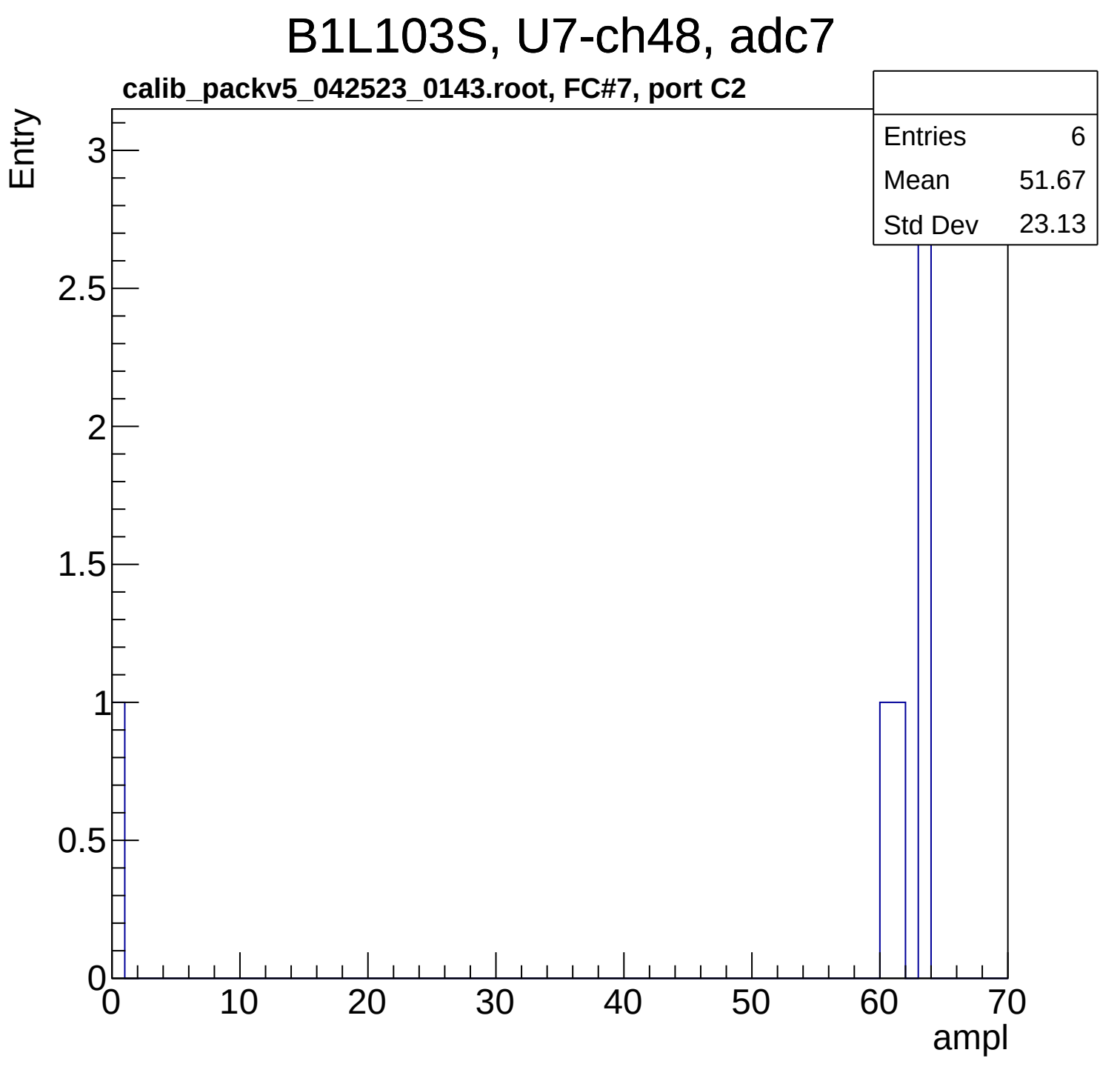

B1L103S, U7-ch48, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 12
Mean 56.83
Std Dev 17.19
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch48, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 6
Mean 51.67
Std Dev 23.13
Entry
ampl
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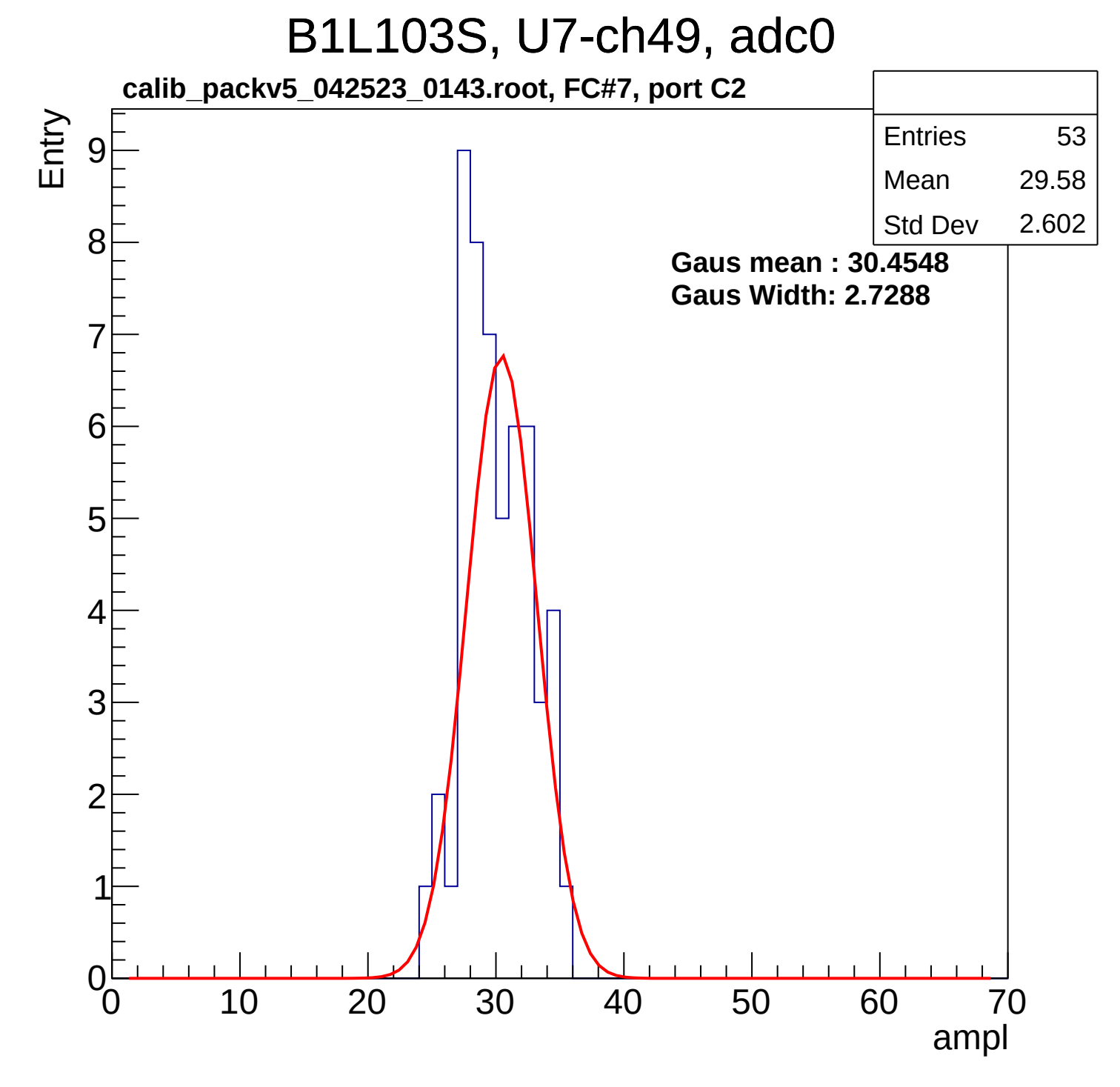
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U7-ch49, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 29.58
Std Dev 2.602
Gaus mean : 30.4548
Gaus Width: 2.7288
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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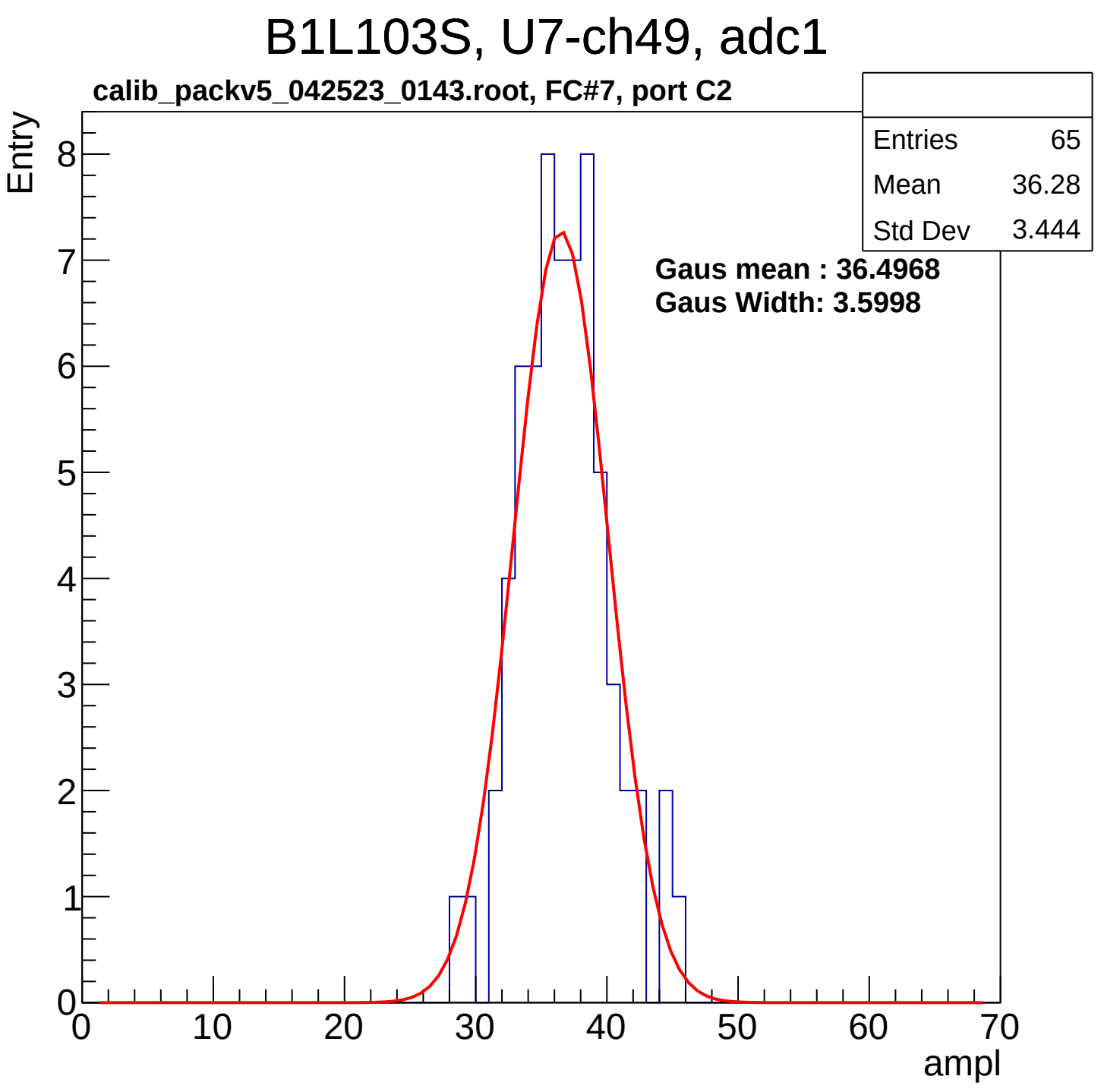
B1L103S, U7-ch49, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 36.28
Std Dev 3.444
Gaus mean : 36.4968
Gaus Width: 3.5998
Entry
ampl
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1
2
3
4
5
6
7
8
0
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60
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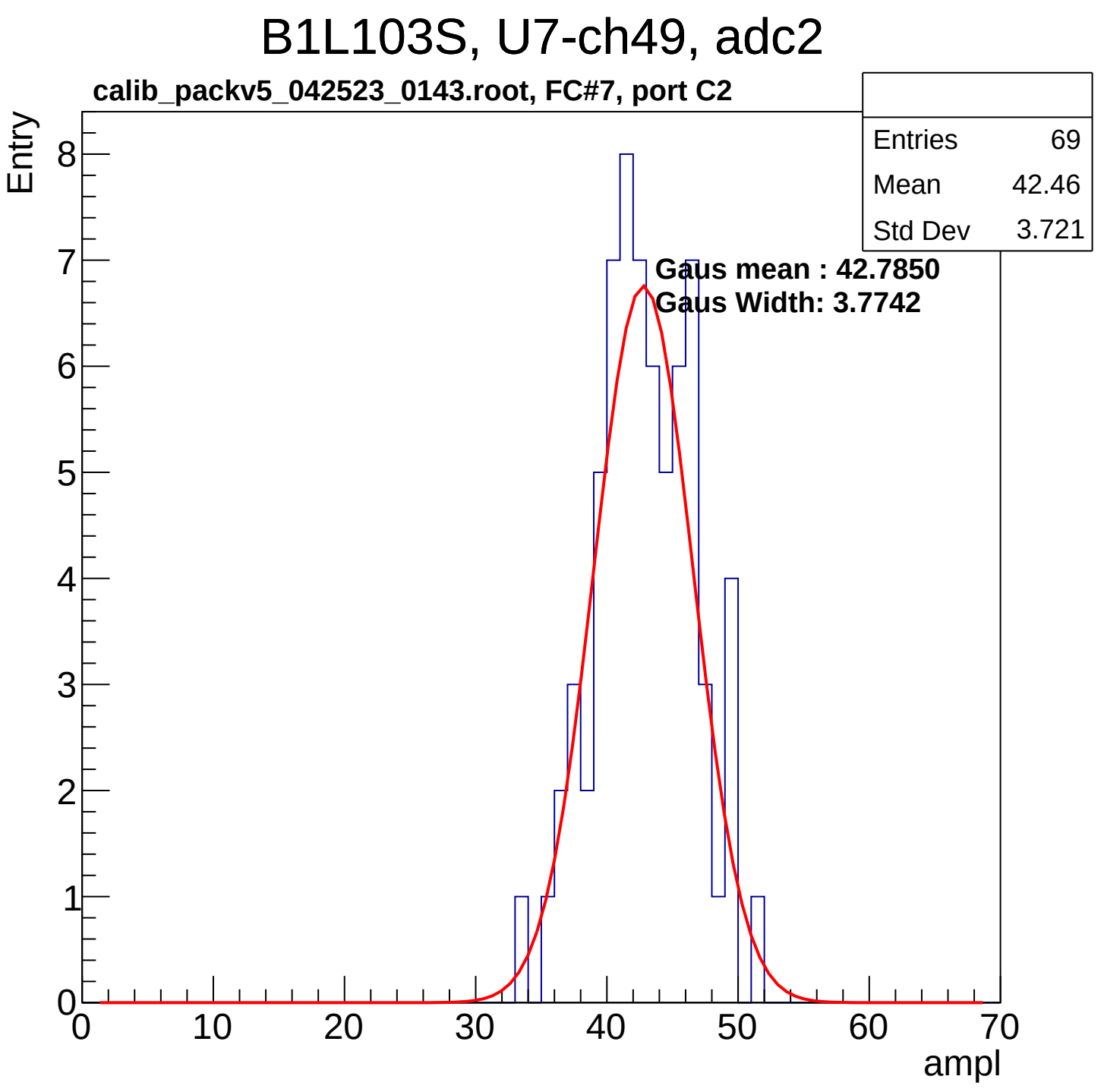
B1L103S, U7-ch49, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 42.46
Std Dev 3.721
Gaus mean : 42.7850
Gaus Width: 3.7742
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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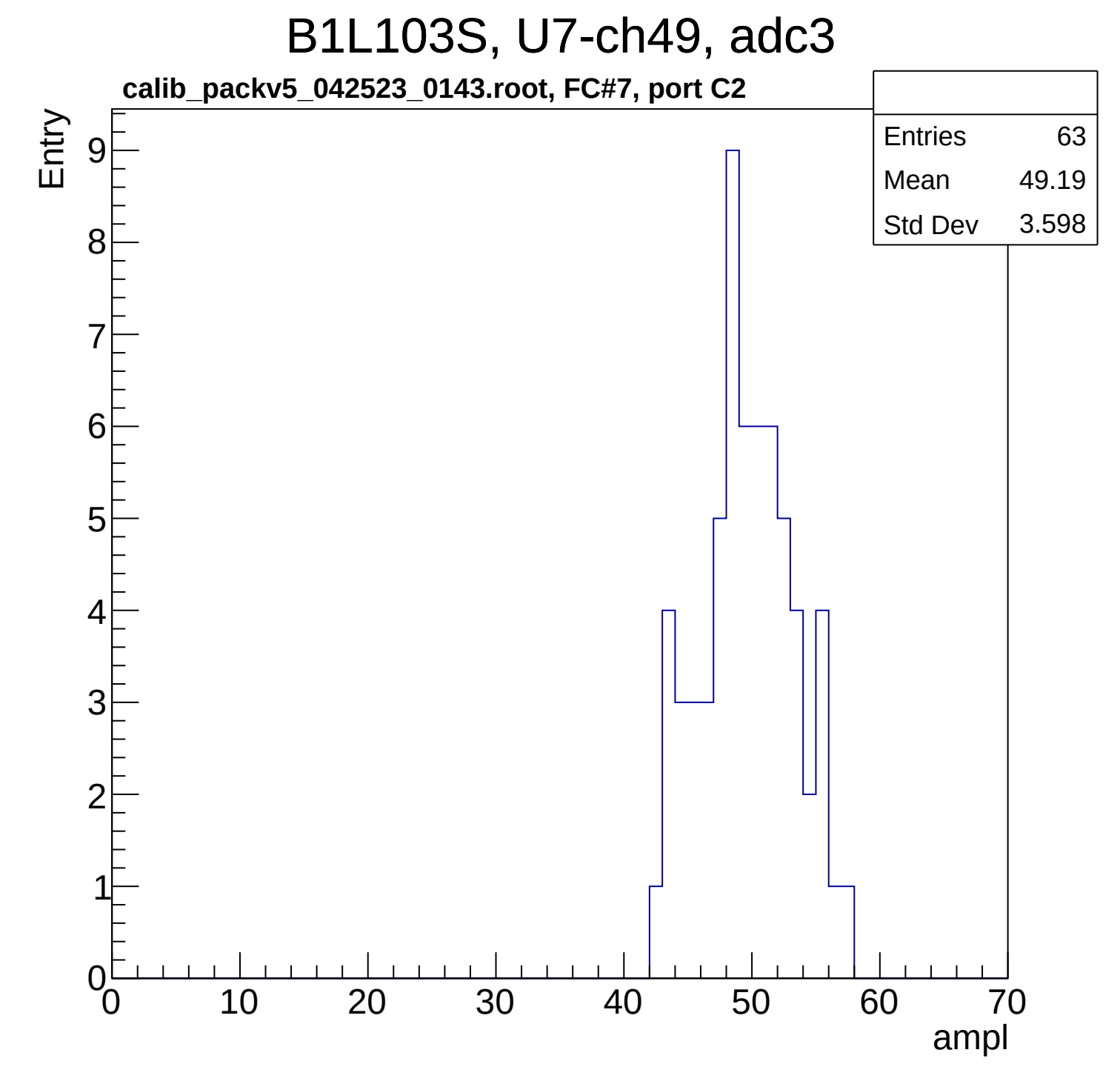
B1L103S, U7-ch49, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 49.19
Std Dev 3.598
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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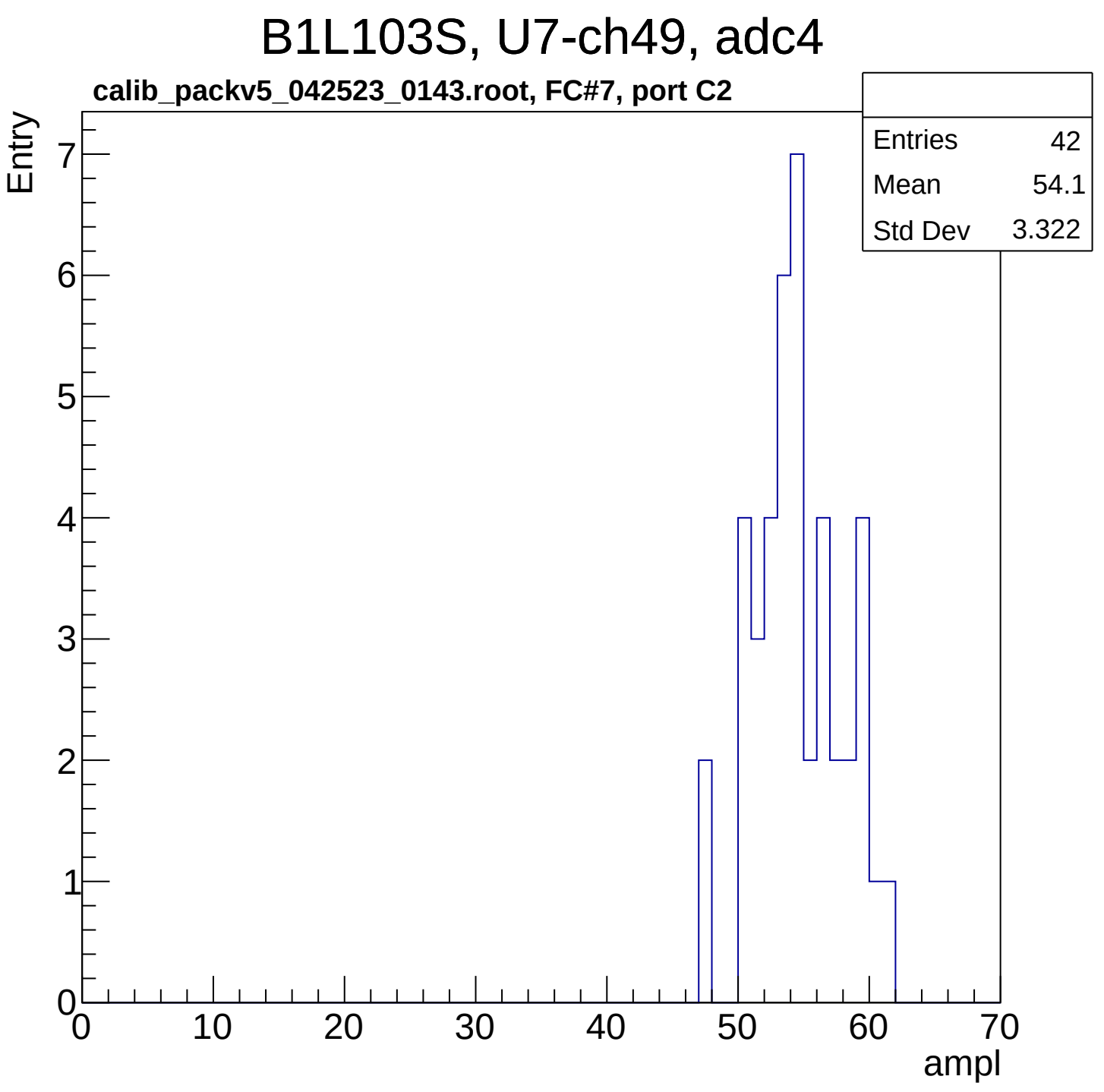
B1L103S, U7-ch49, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 42
Mean 54.1
Std Dev 3.322
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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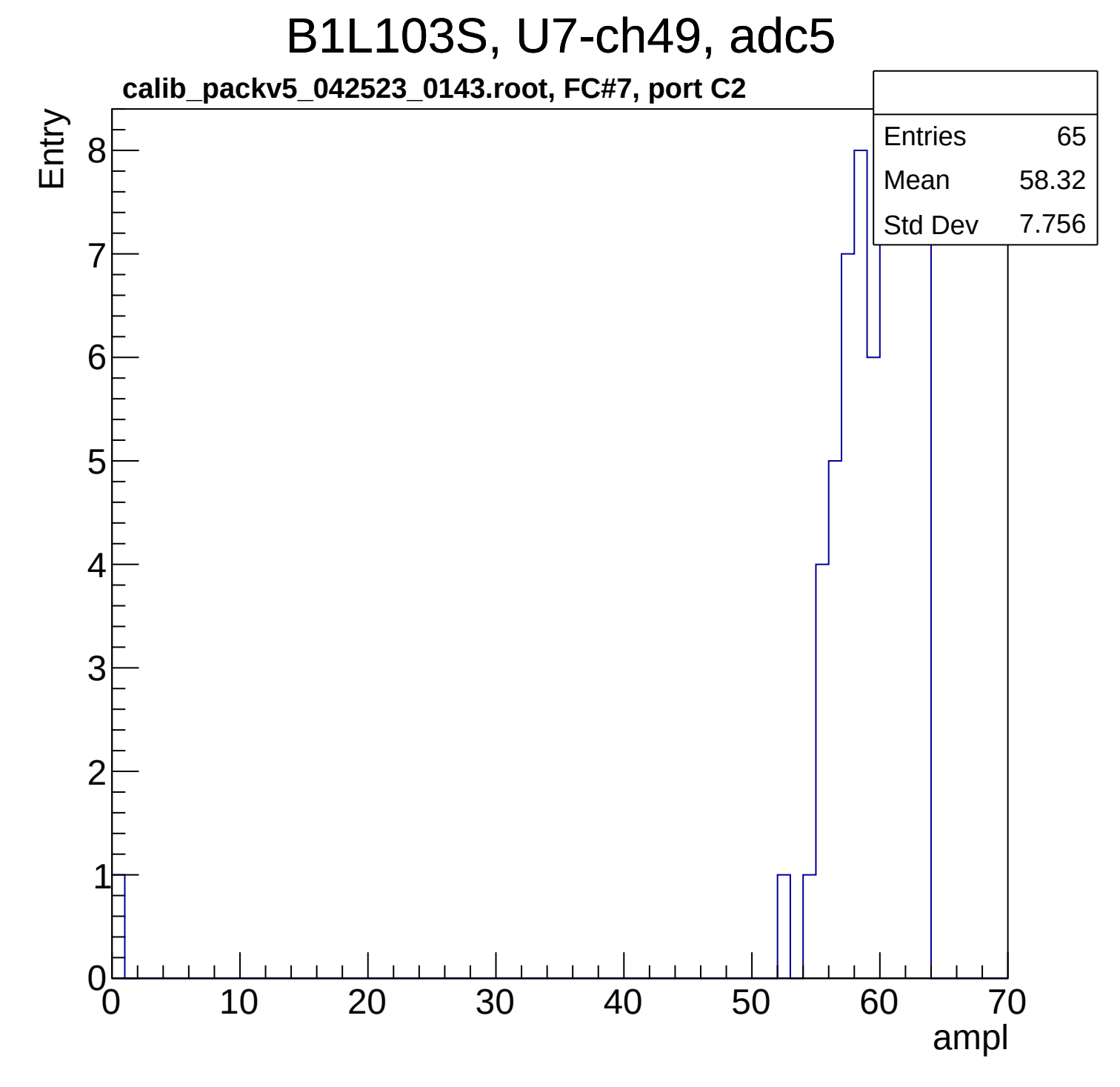
B1L103S, U7-ch49, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 58.32
Std Dev 7.756
Entry
ampl
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5
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7
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0
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40
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60
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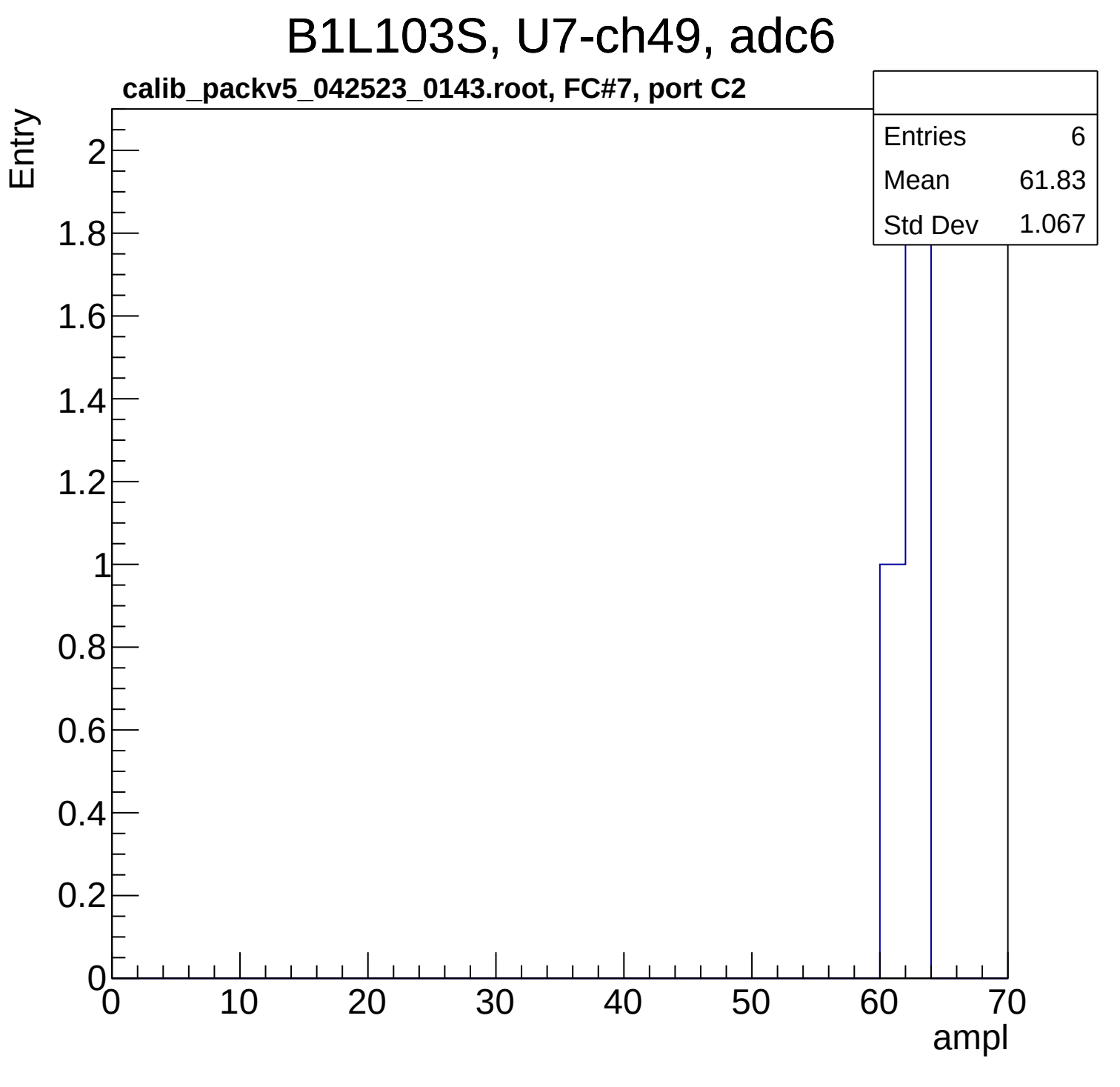
B1L103S, U7-ch49, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 6
Mean 61.83
Std Dev 1.067
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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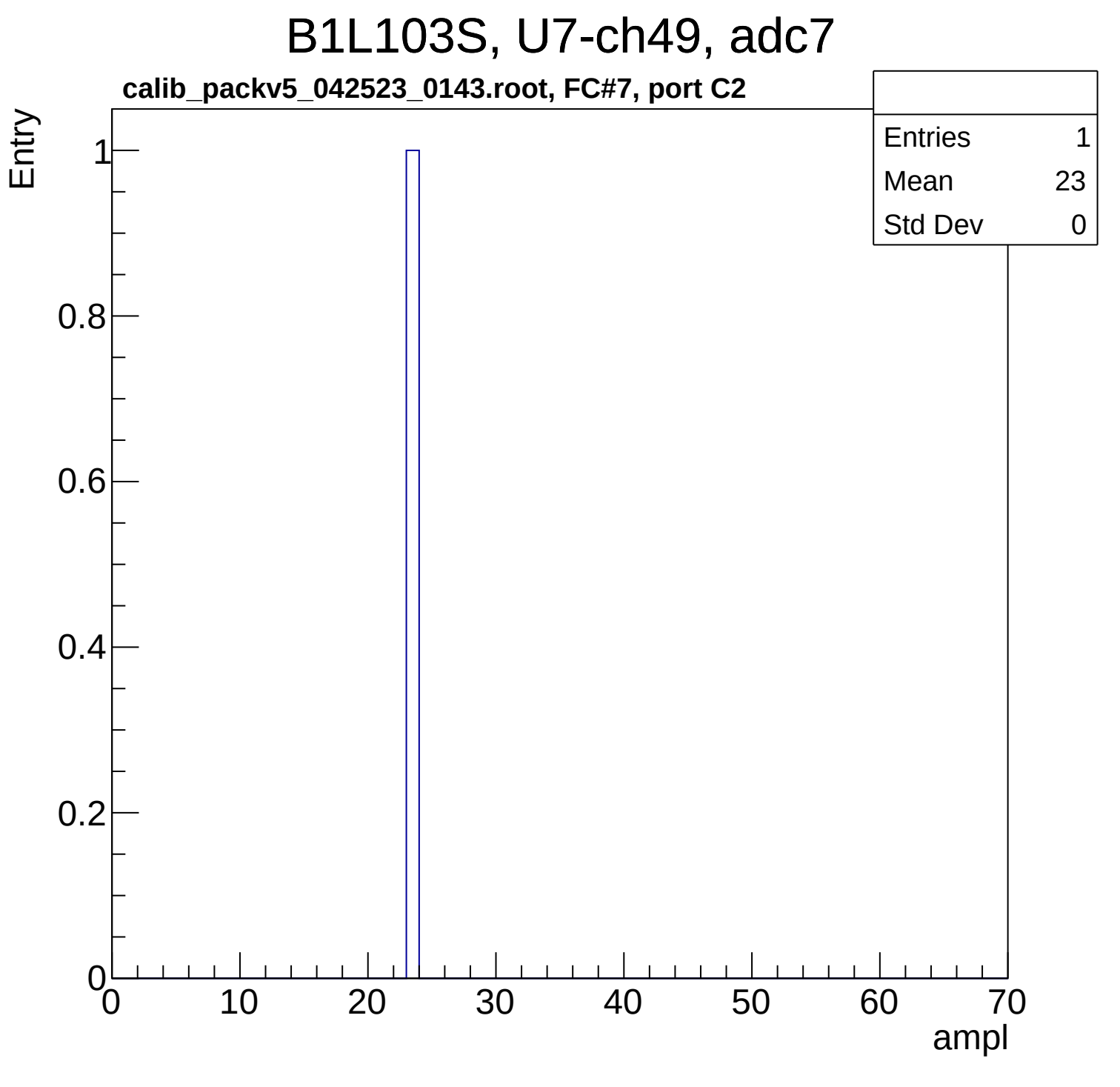
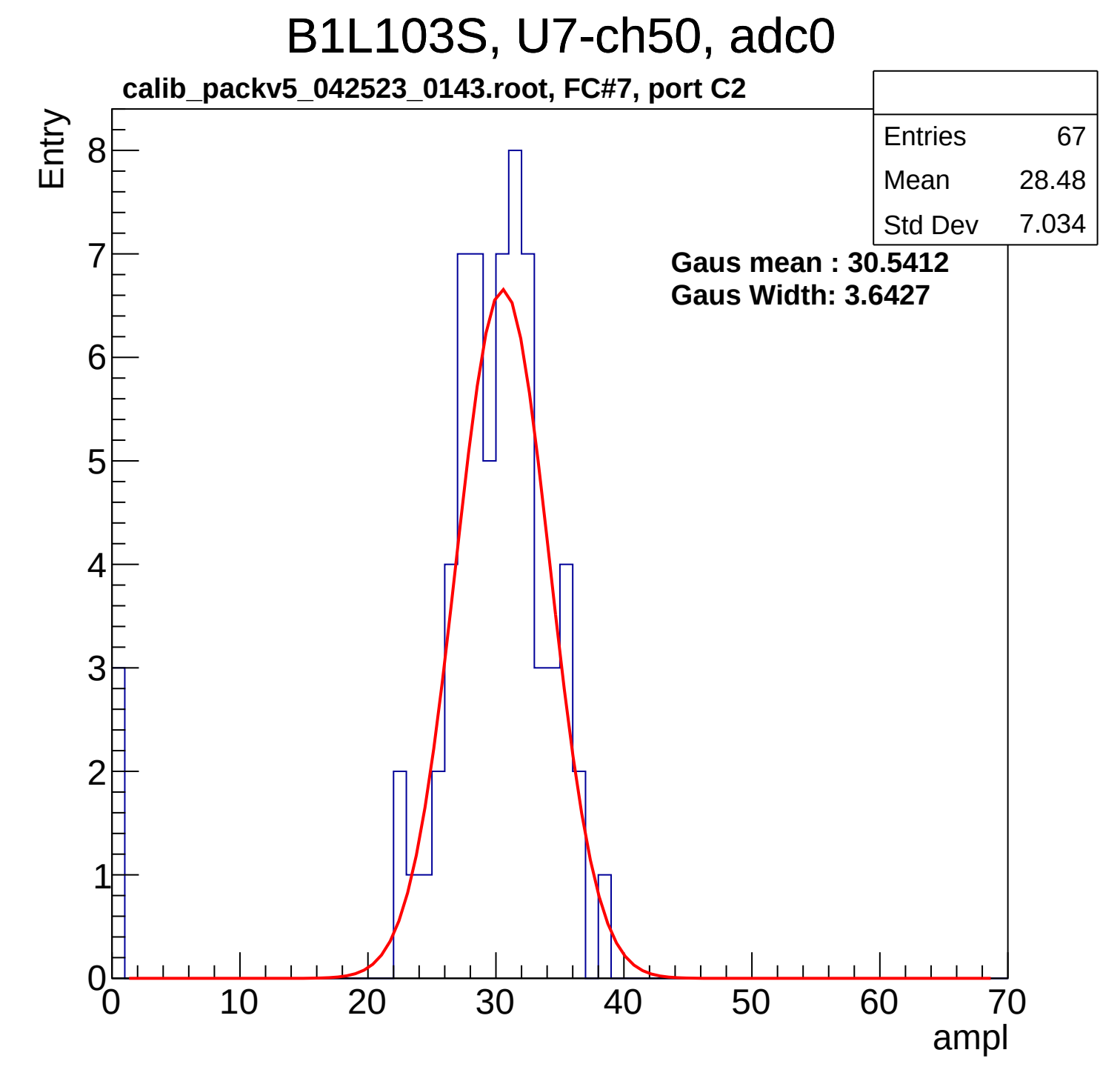

B1L103S, U7-ch49, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 23
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch50, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 28.48
Std Dev 7.034
Gaus mean : 30.5412
Gaus Width: 3.6427
Entry
ampl
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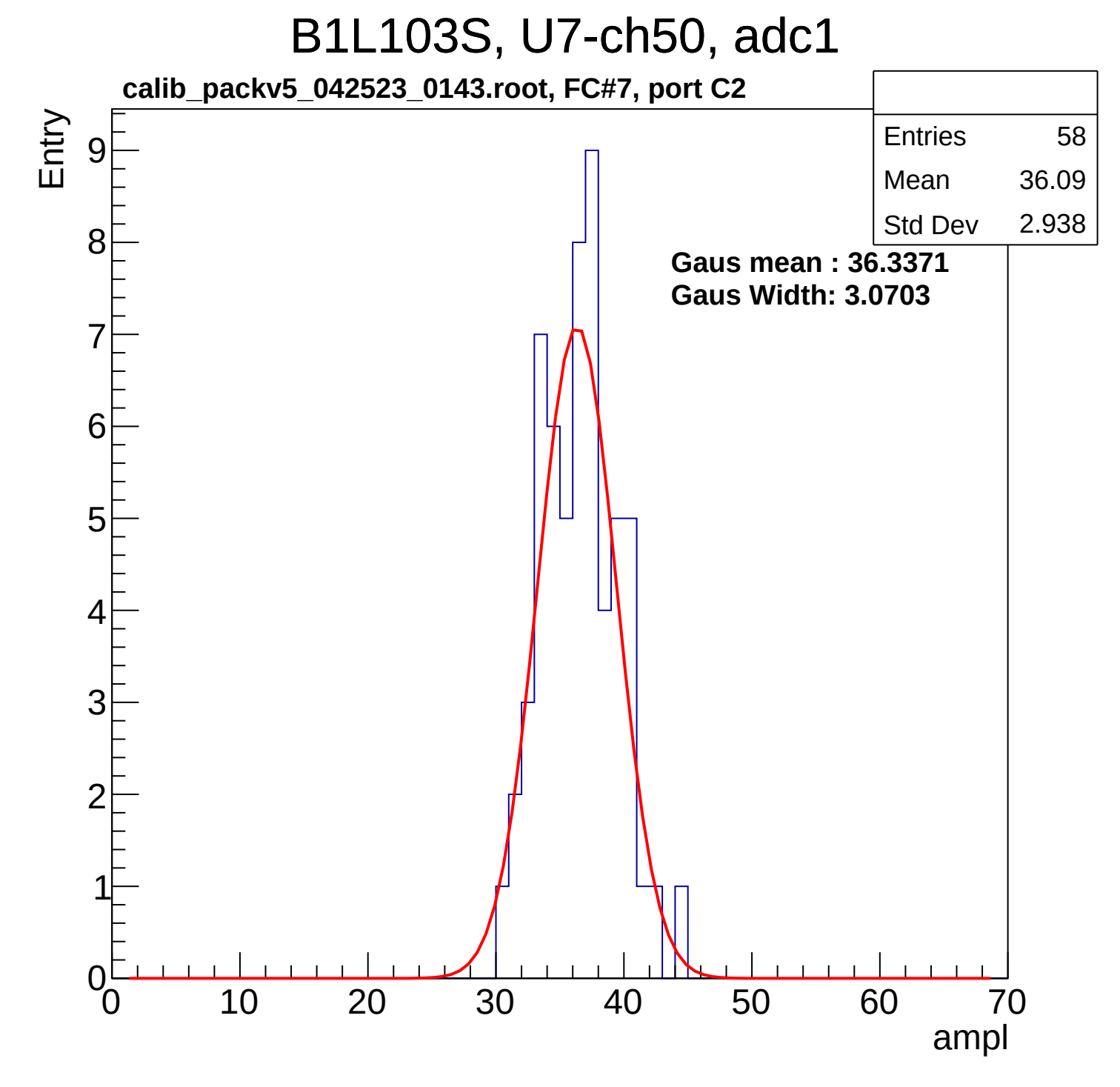
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch50, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 58
Mean 36.09
Std Dev 2.938
Gaus mean : 36.3371
Gaus Width: 3.0703
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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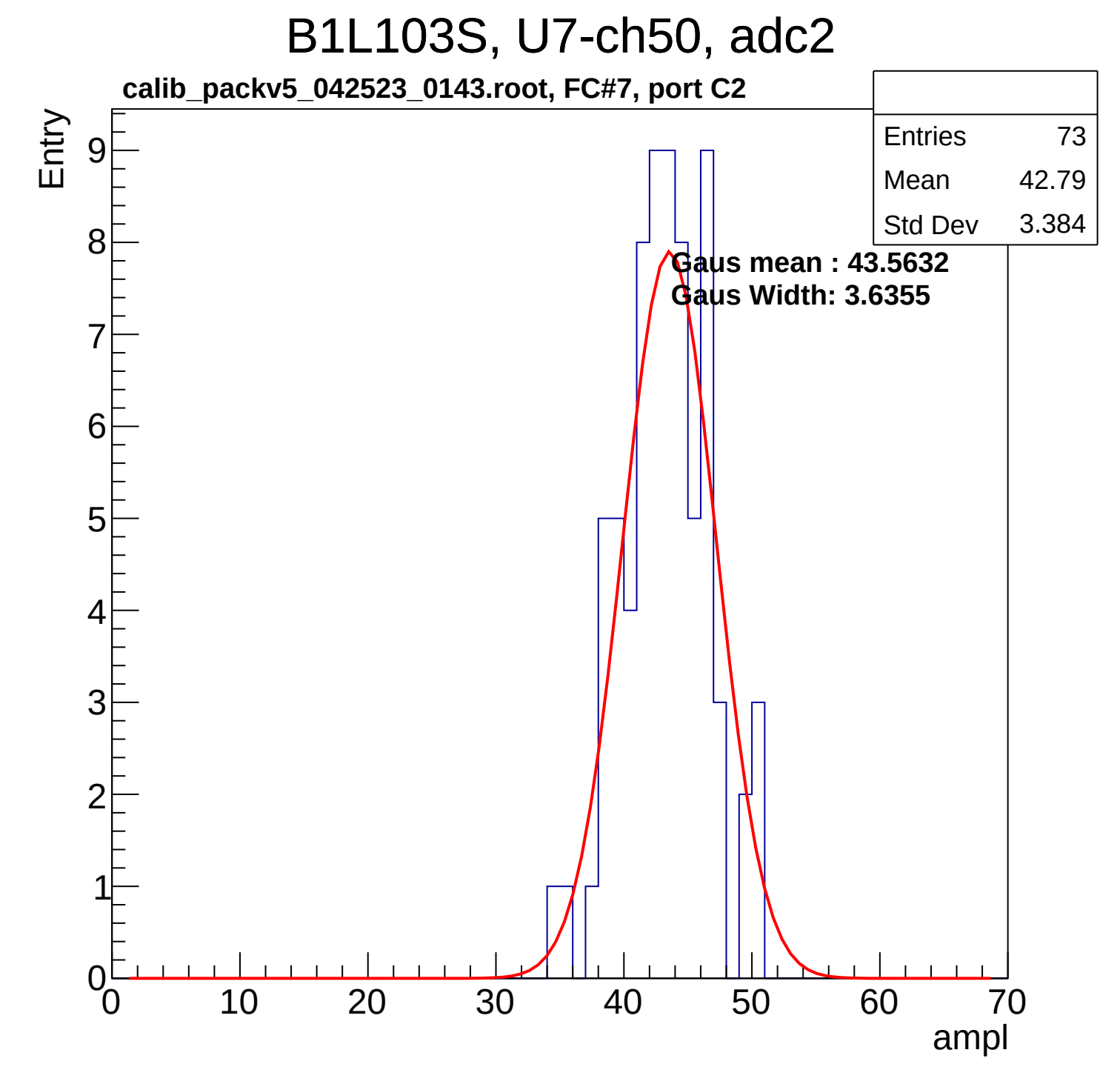
B1L103S, U7-ch50, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 73
Mean 42.79
Std Dev 3.384
Gaus mean : 43.5632
Gaus Width: 3.6355
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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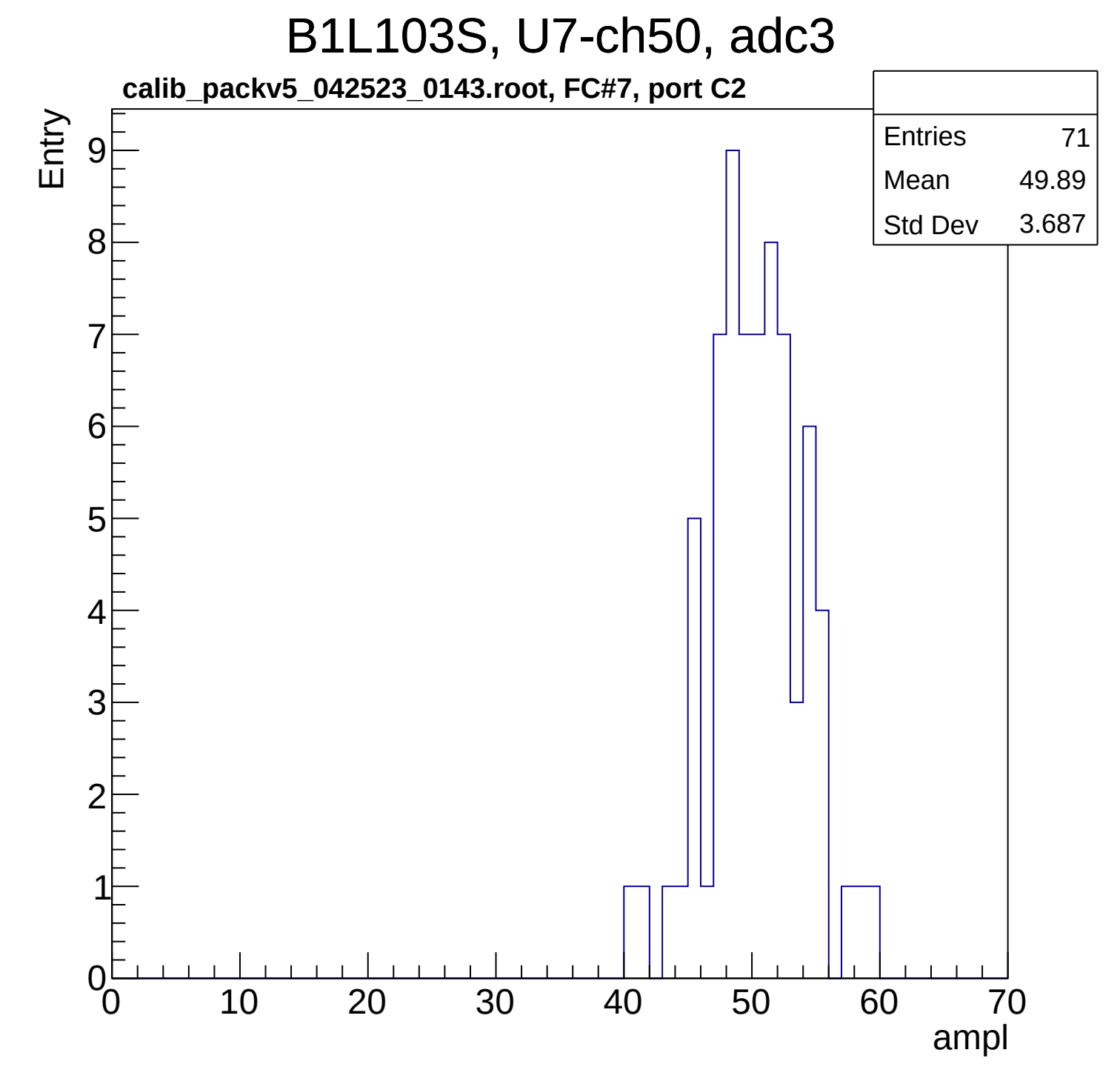
B1L103S, U7-ch50, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 71
Mean 49.89
Std Dev 3.687
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
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60
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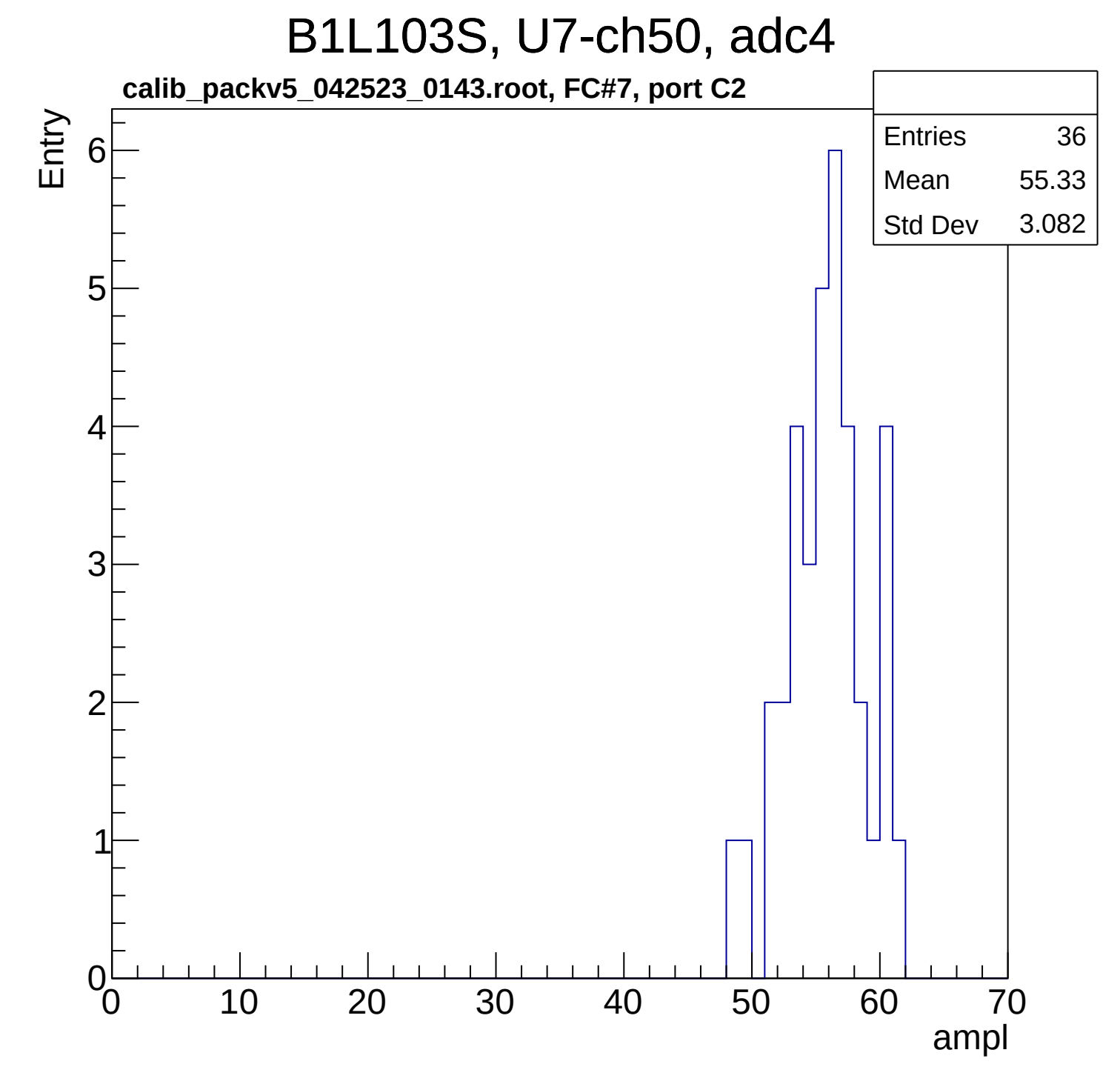
B1L103S, U7-ch50, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 36
Mean 55.33
Std Dev 3.082
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
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60
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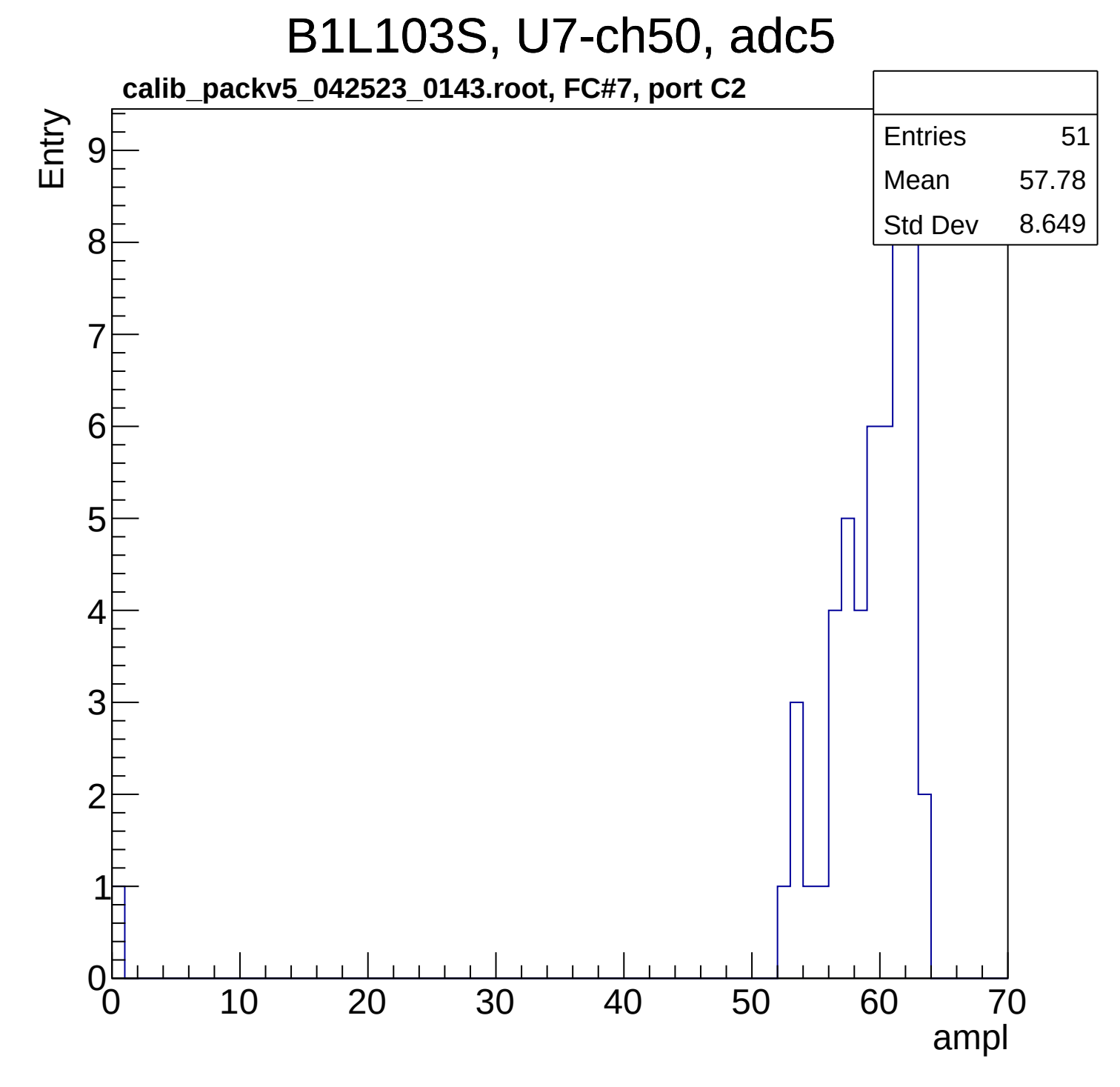
B1L103S, U7-ch50, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 51
Mean 57.78
Std Dev 8.649
Entry
ampl
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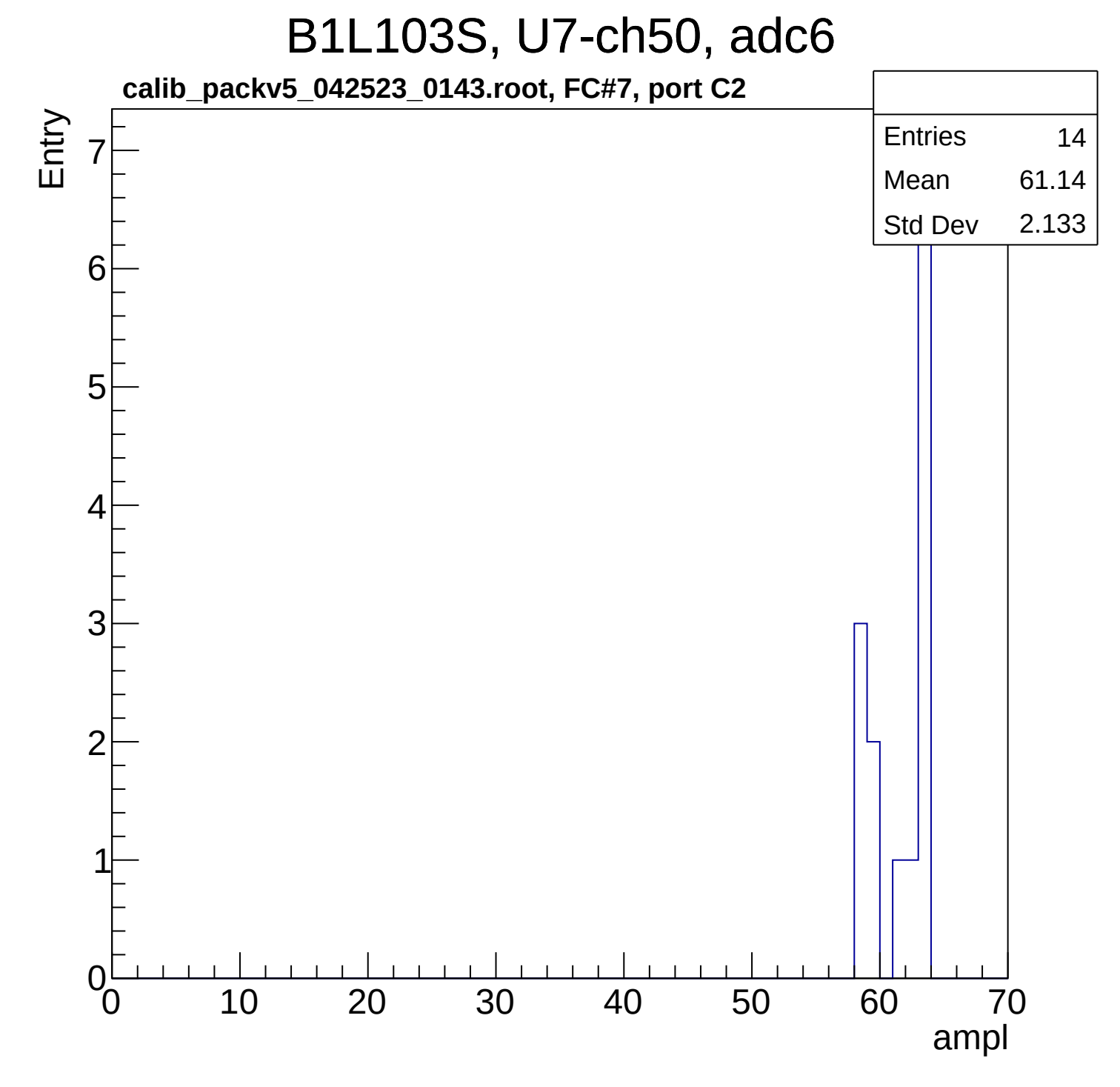
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch50, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 14
Mean 61.14
Std Dev 2.133
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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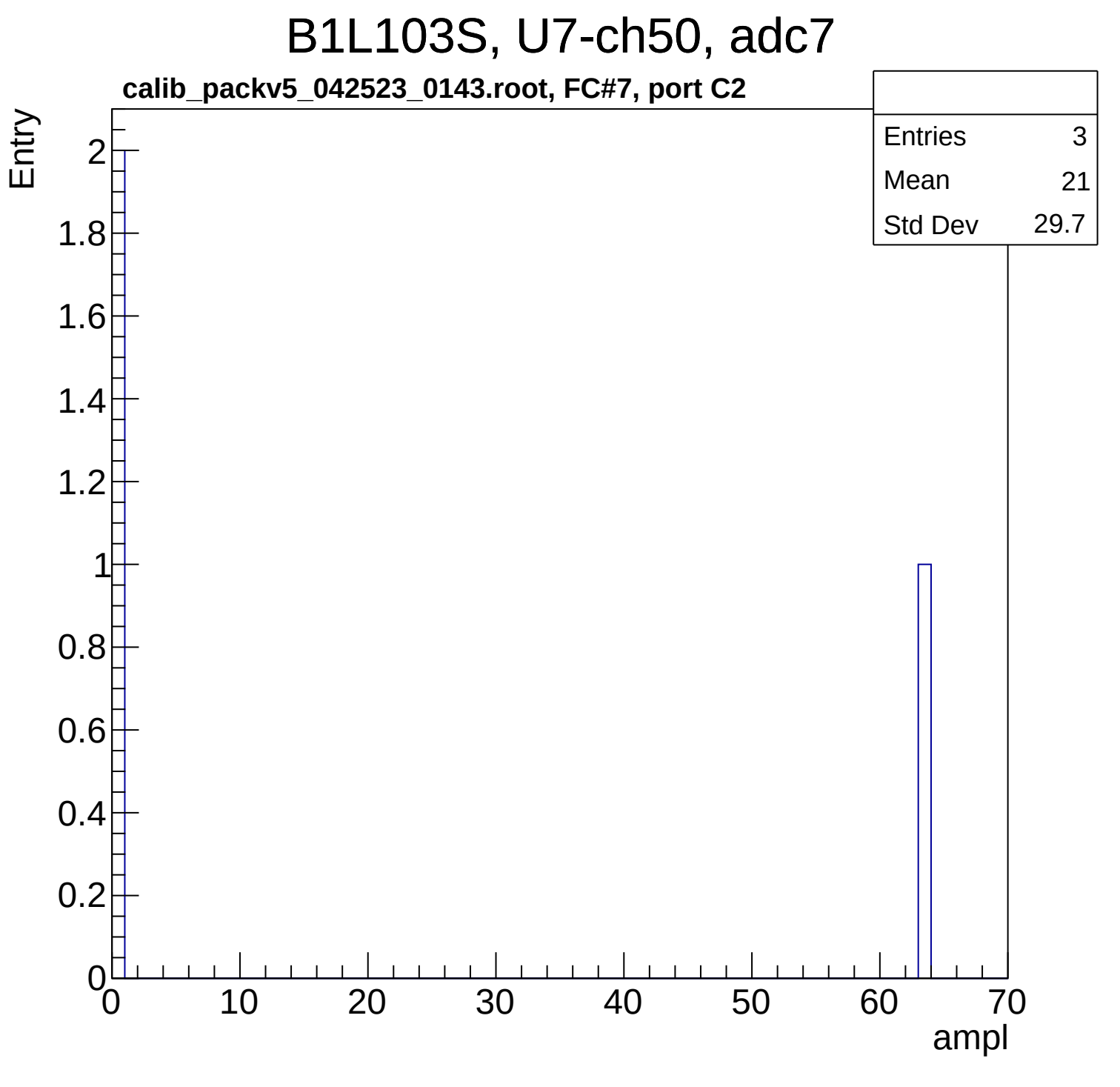
B1L103S, U7-ch50, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 21
Std Dev 29.7
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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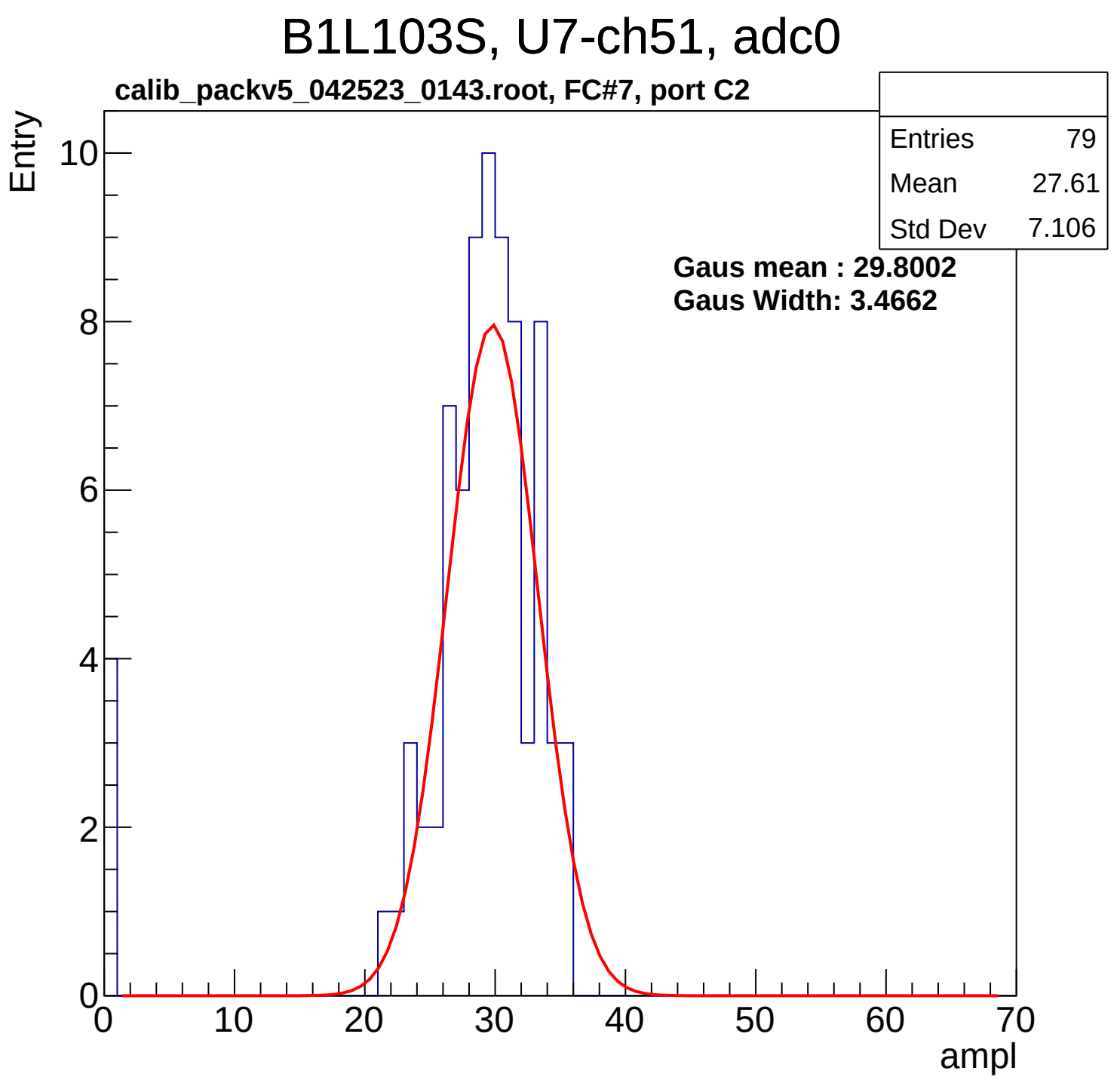
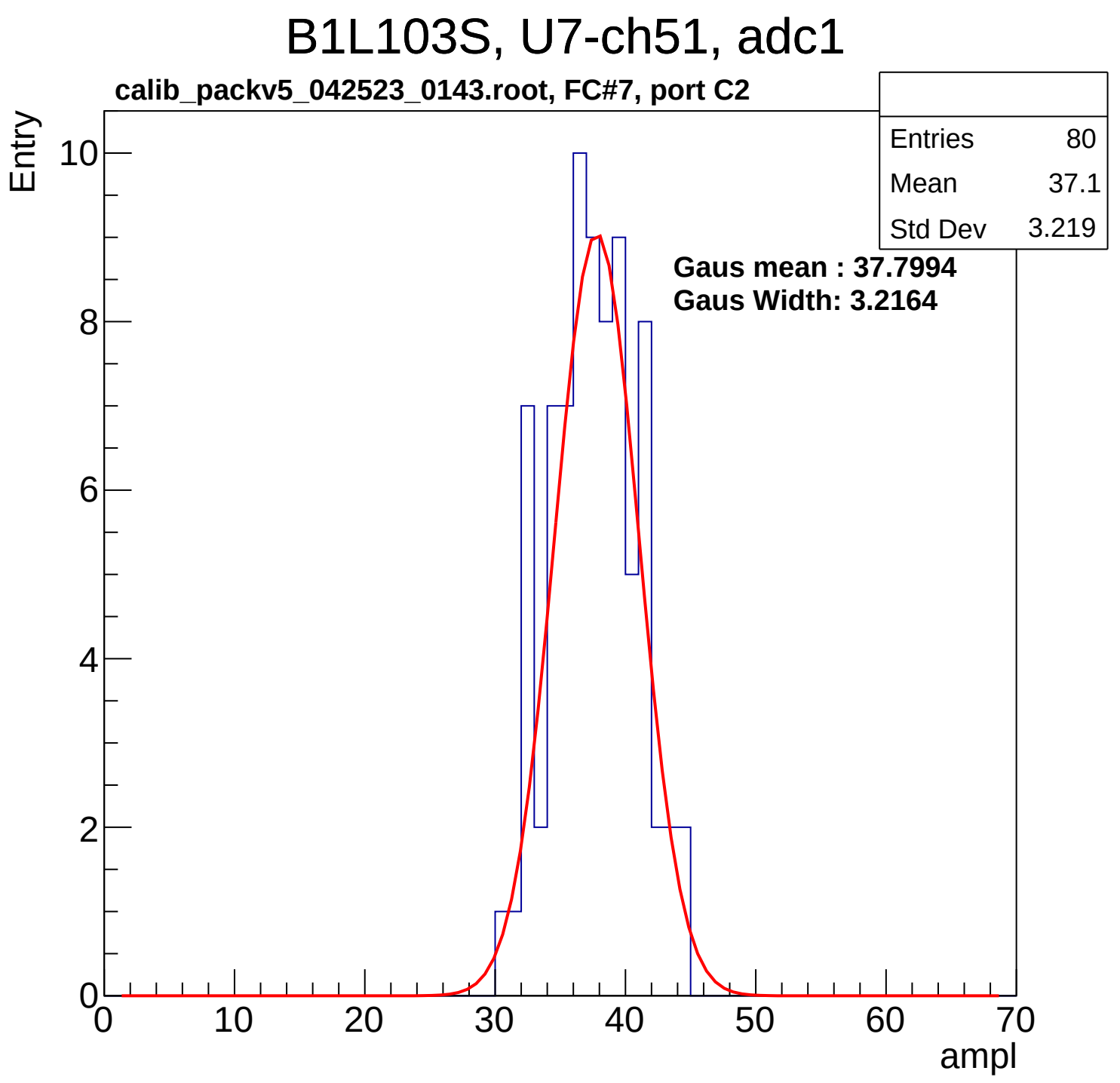
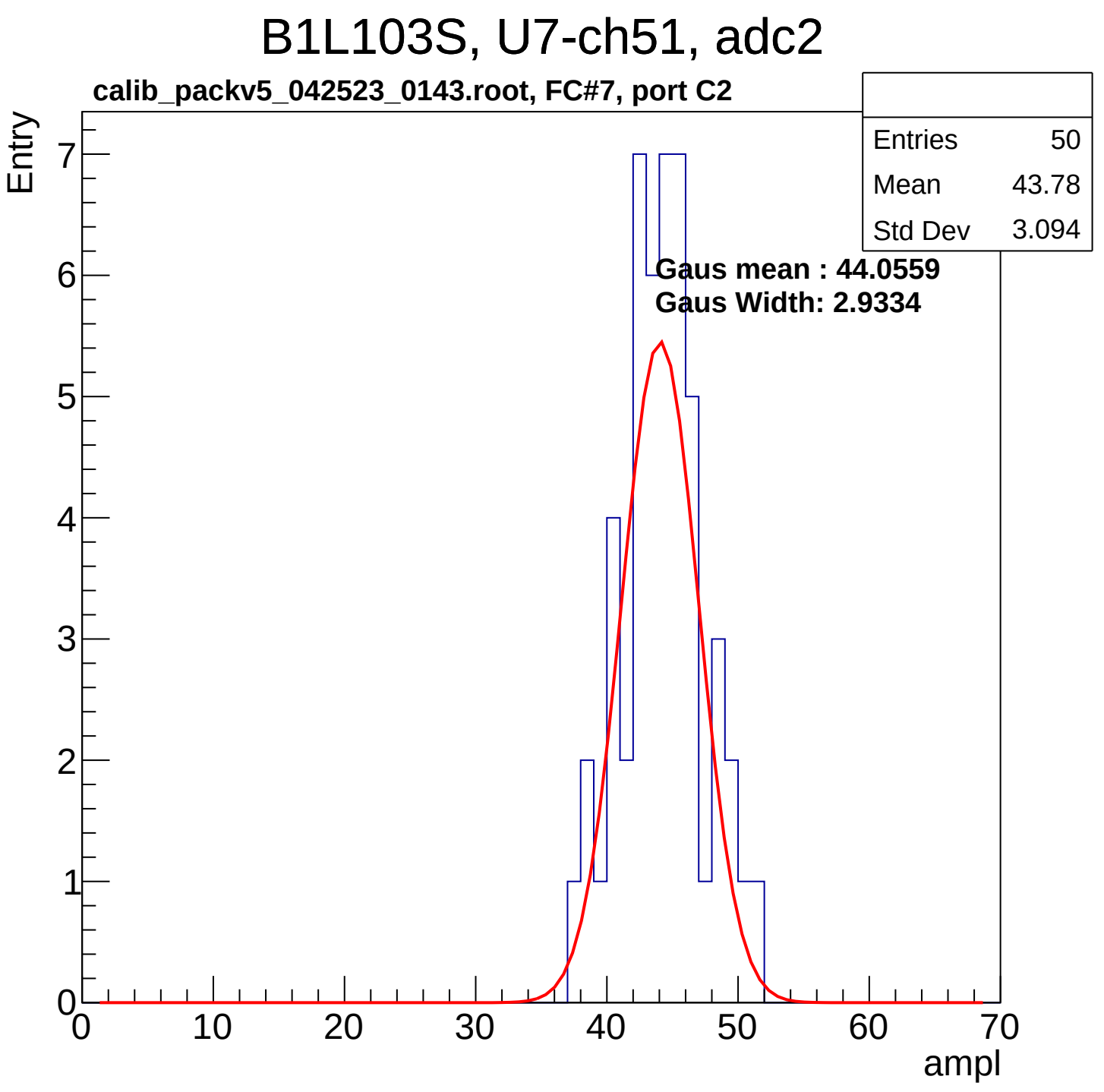

B1L103S, U7-ch51, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 79
Mean 27.61
Std Dev 7.106
Gaus mean : 29.8002
Gaus Width: 3.4662
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch51, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 80
Mean 37.1
Std Dev 3.219
Gaus mean : 37.7994
Gaus Width: 3.2164
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch51, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 50
Mean 43.78
Std Dev 3.094
Gaus mean : 44.0559
Gaus Width: 2.9334
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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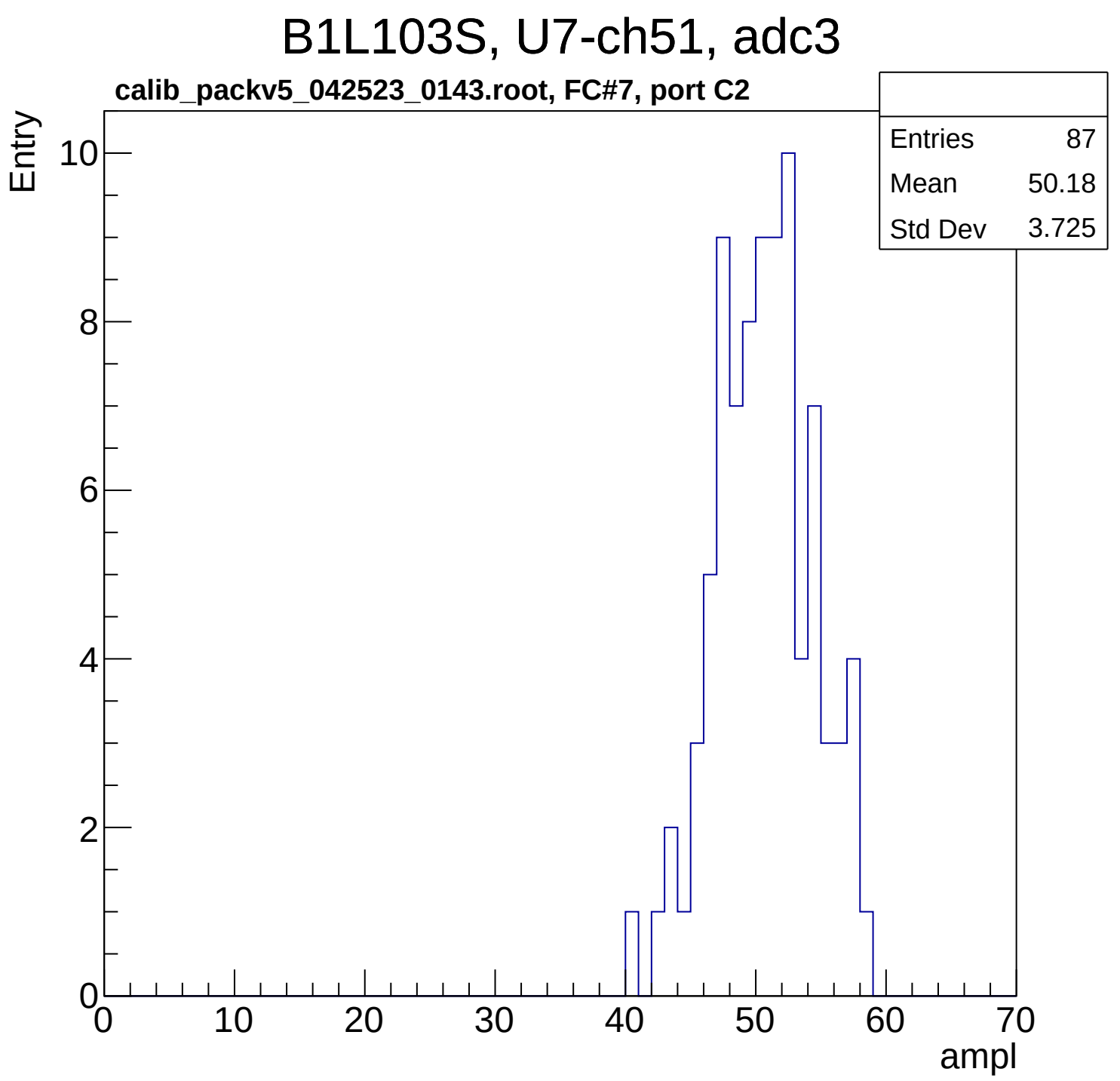
B1L103S, U7-ch51, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 87
Mean 50.18
Std Dev 3.725
Entry
ampl
0
2
4
6
8
10
0
10
20
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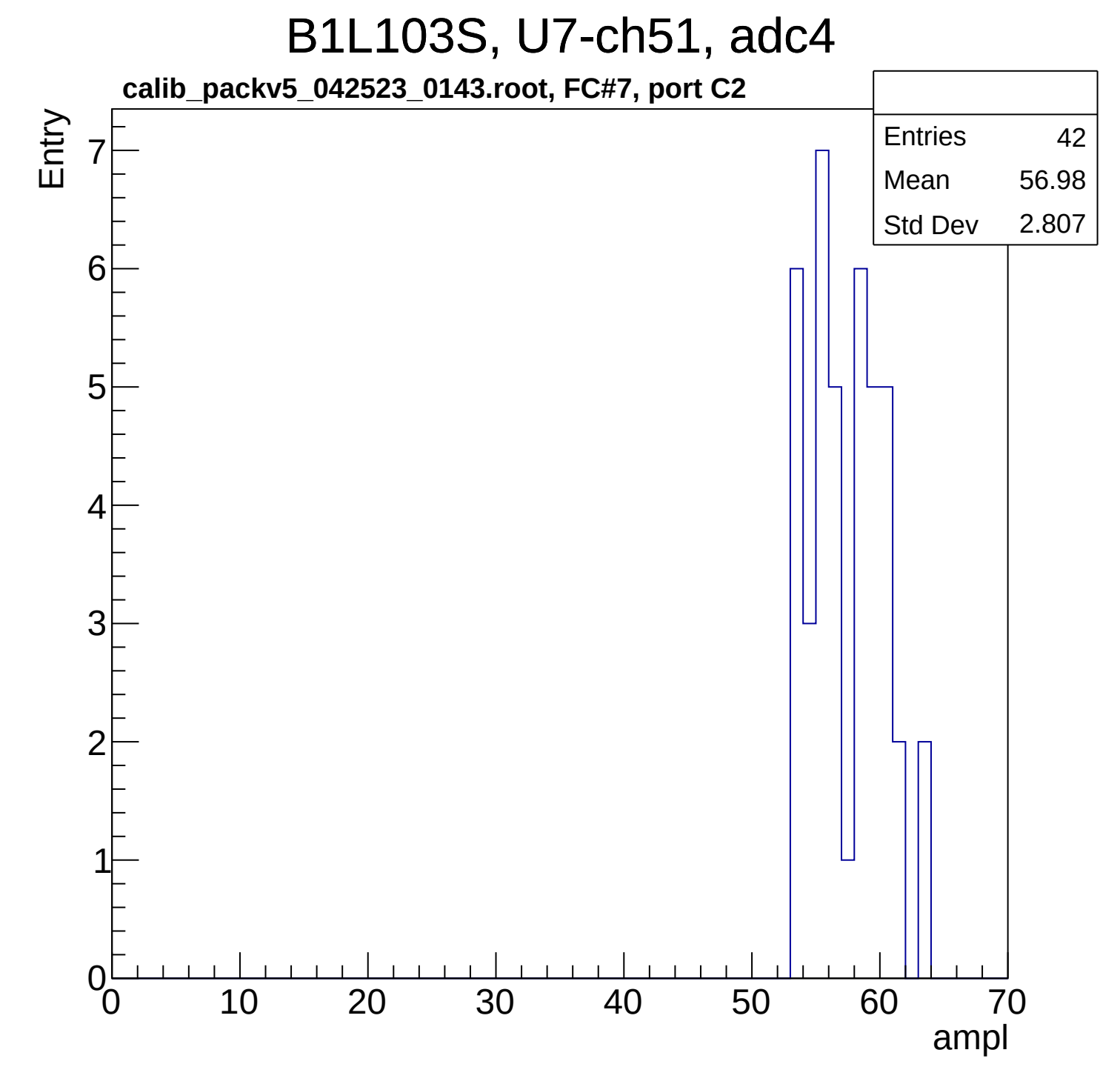
60
70


B1L103S, U7-ch51, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 42
Mean 56.98
Std Dev 2.807
Entry
ampl
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1
2
3
4
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6
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0
10
20
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40
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60
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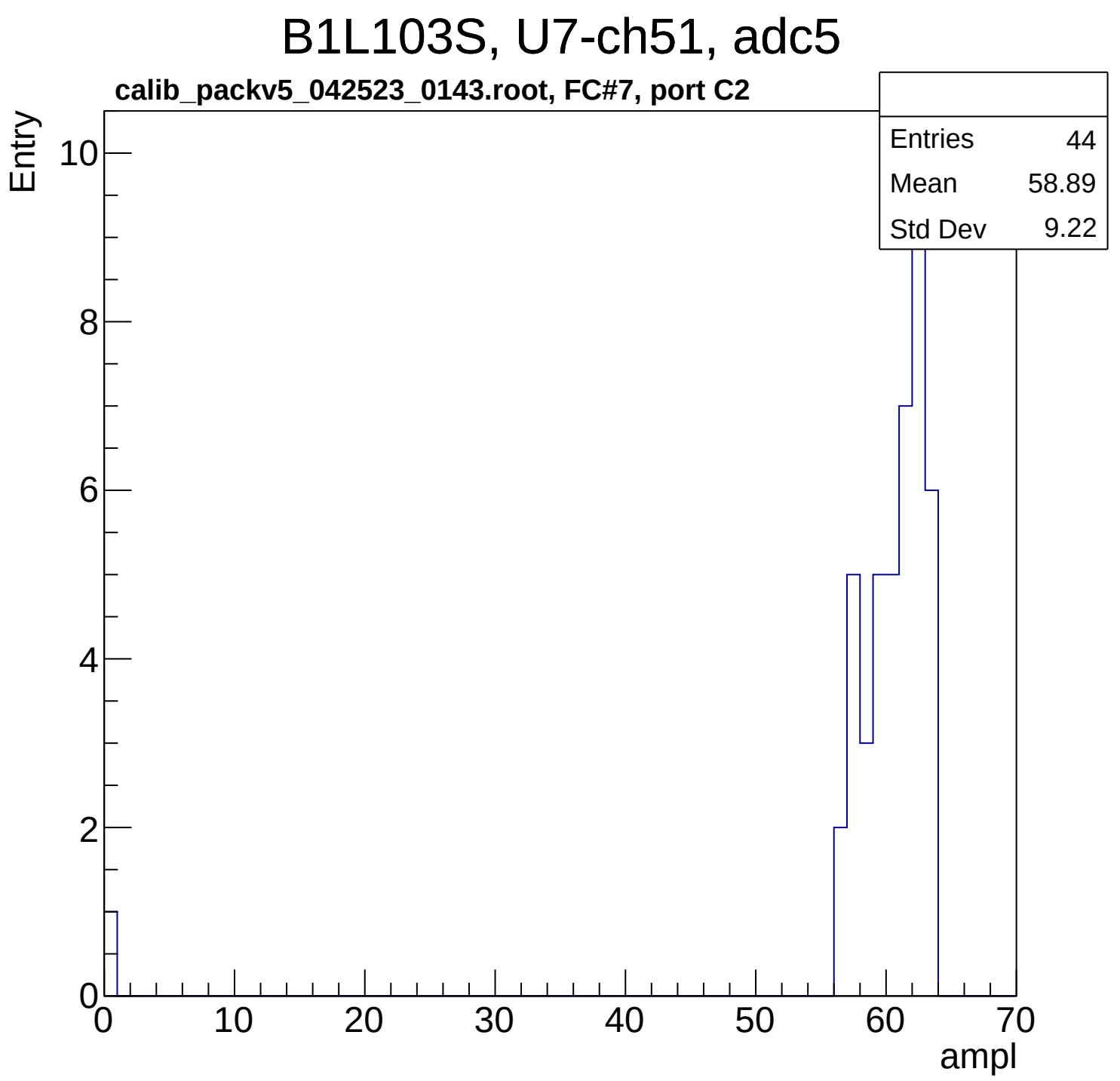
B1L103S, U7-ch51, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 44
Mean 58.89
Std Dev 9.22
Entry
0
2
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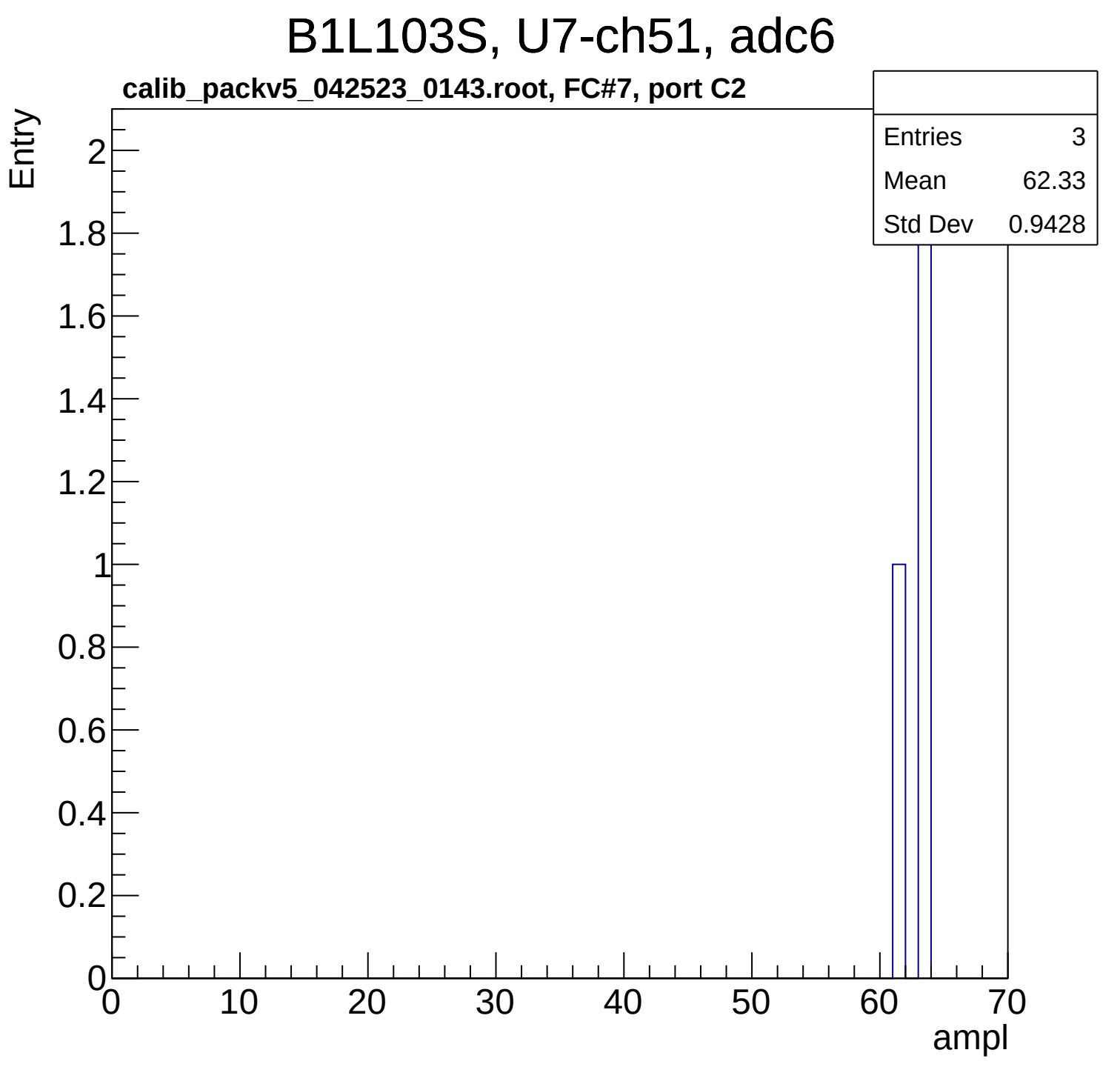
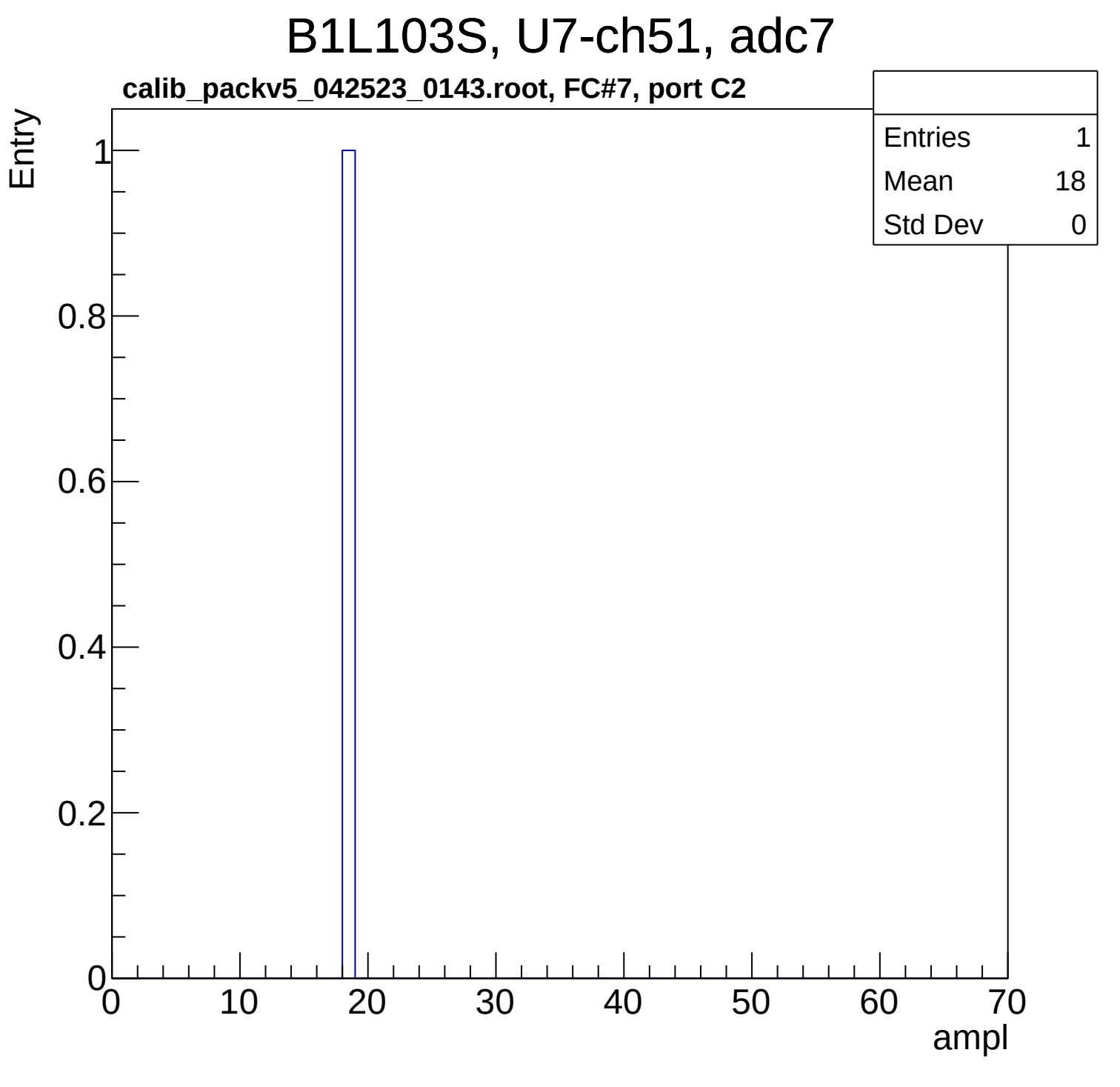
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch51, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 62.33
Std Dev 0.9428
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U7-ch51, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 18
Std Dev 0
Entry
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0.8
0.6
0.4
0.2
0
0
10
20
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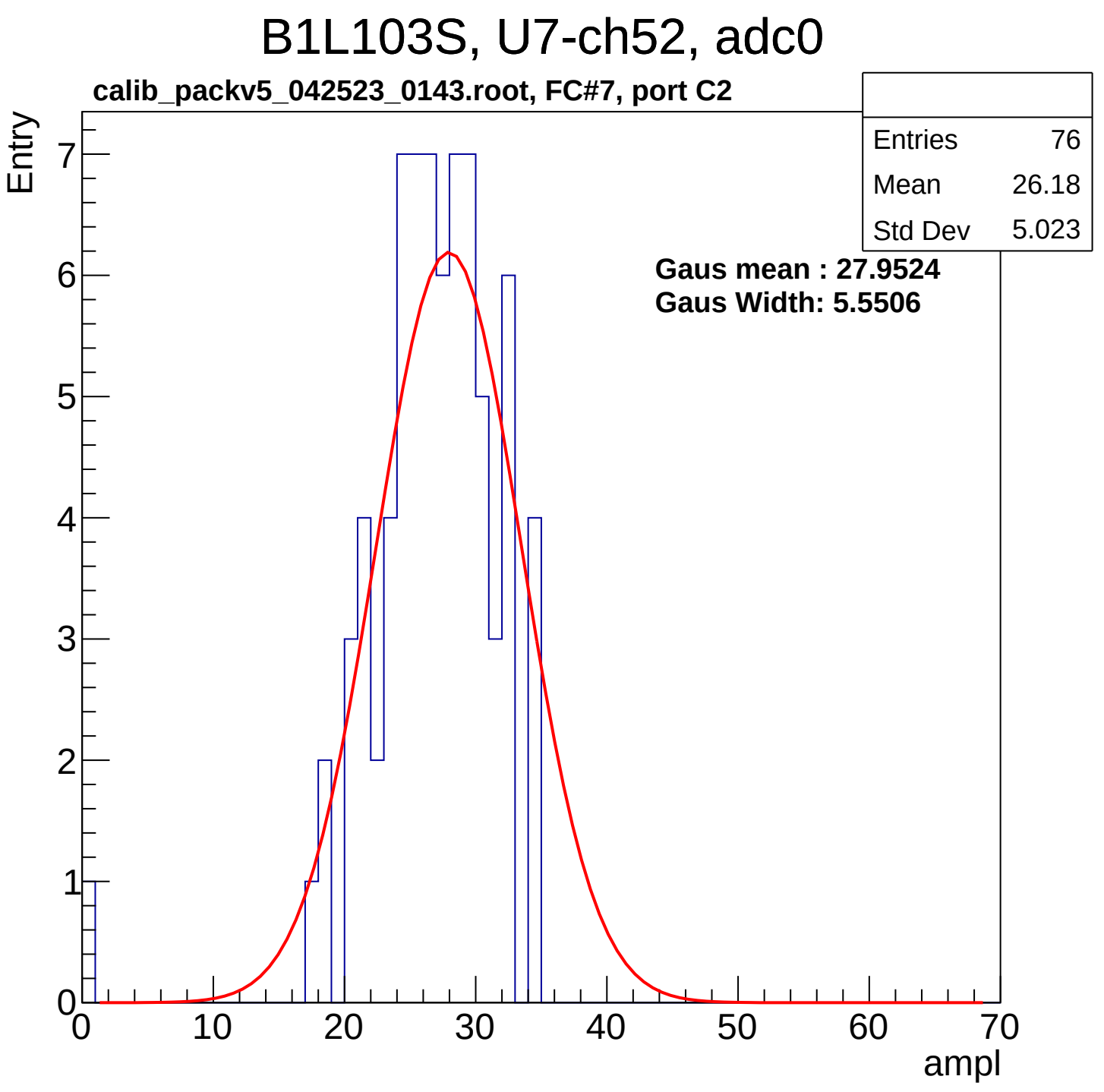
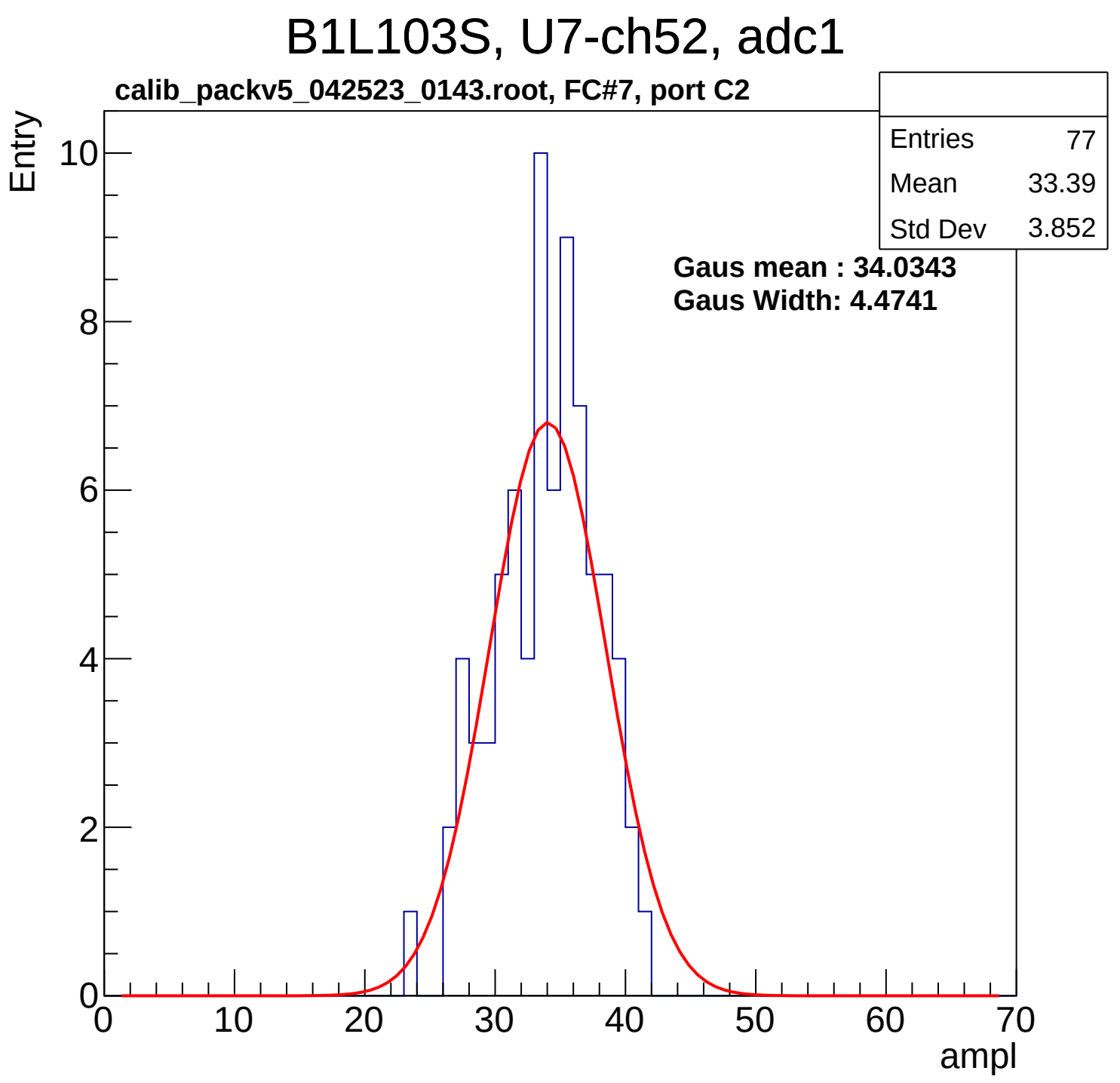
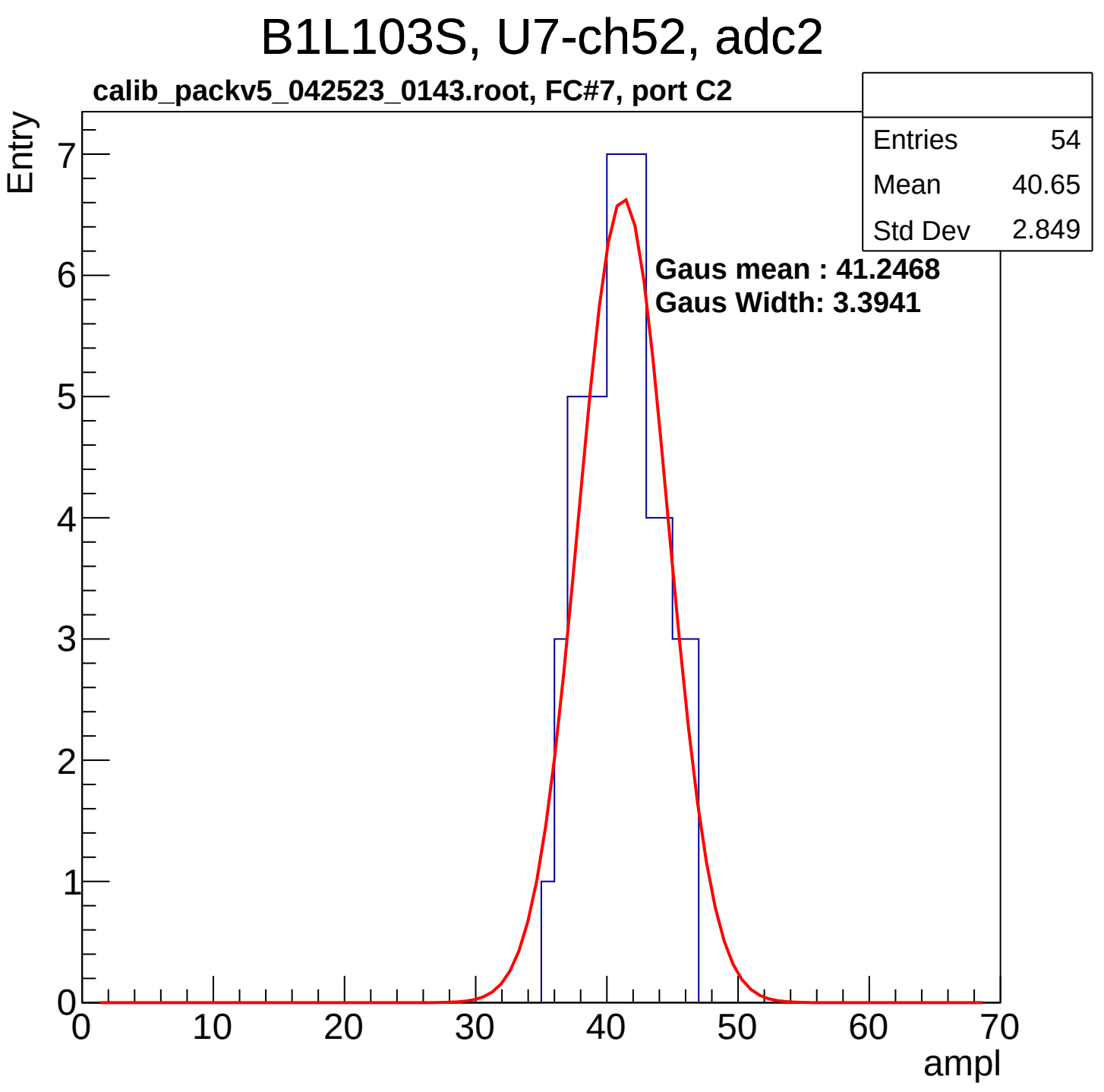
40
50
60
70
ampl


B1L103S, U7-ch52, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 76
Mean 26.18
Std Dev 5.023
Gaus mean : 27.9524
Gaus Width: 5.5506
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch52, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 77
Mean 33.39
Std Dev 3.852
Gaus mean : 34.0343
Gaus Width: 4.4741
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch52, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 54
Mean 40.65
Std Dev 2.849
Gaus mean : 41.2468
Gaus Width: 3.3941
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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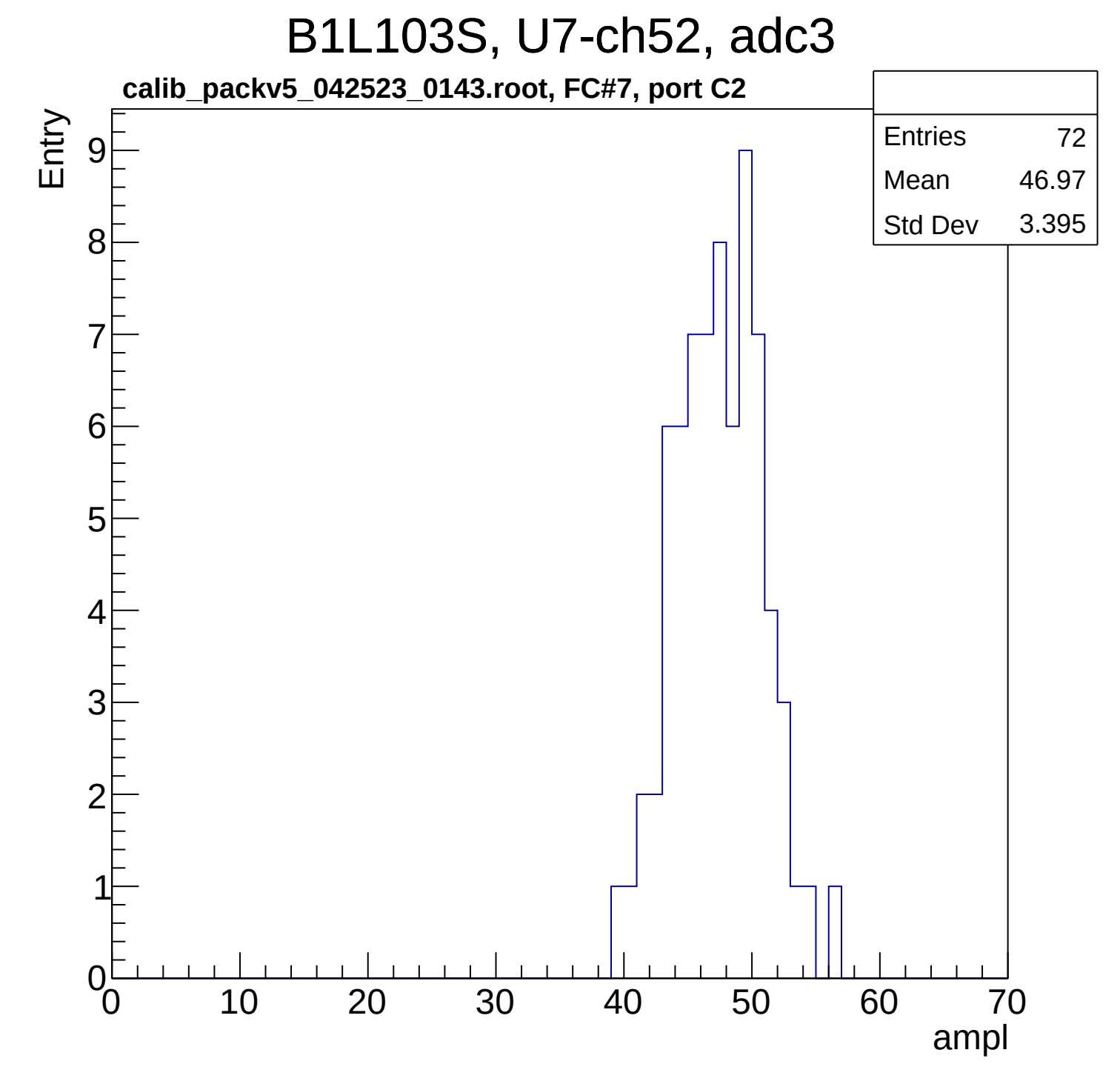
B1L103S, U7-ch52, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 72
Mean 46.97
Std Dev 3.395
Entry
ampl
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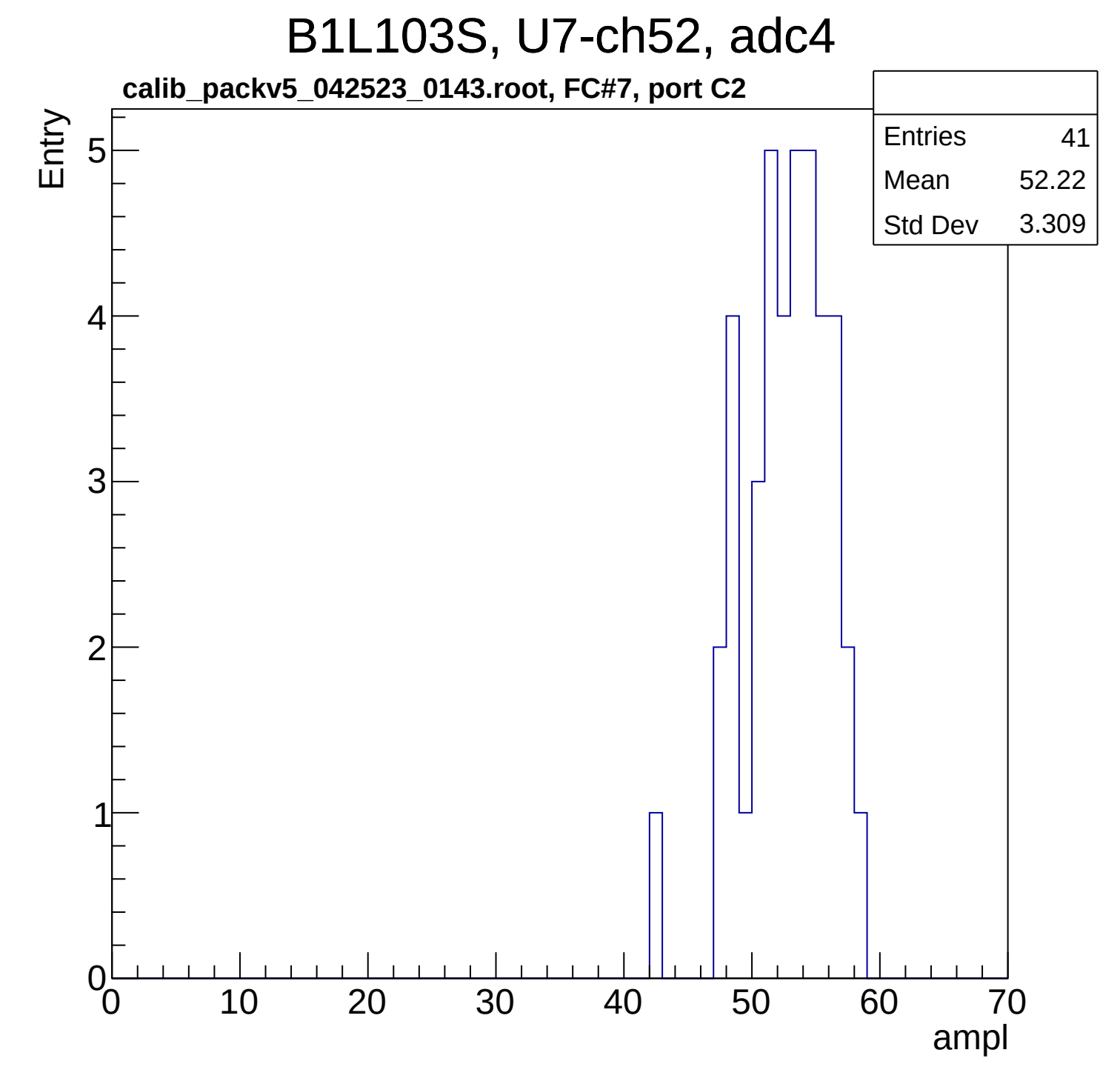
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch52, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 41
Mean 52.22
Std Dev 3.309
Entry
ampl
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2
3
4
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50
60
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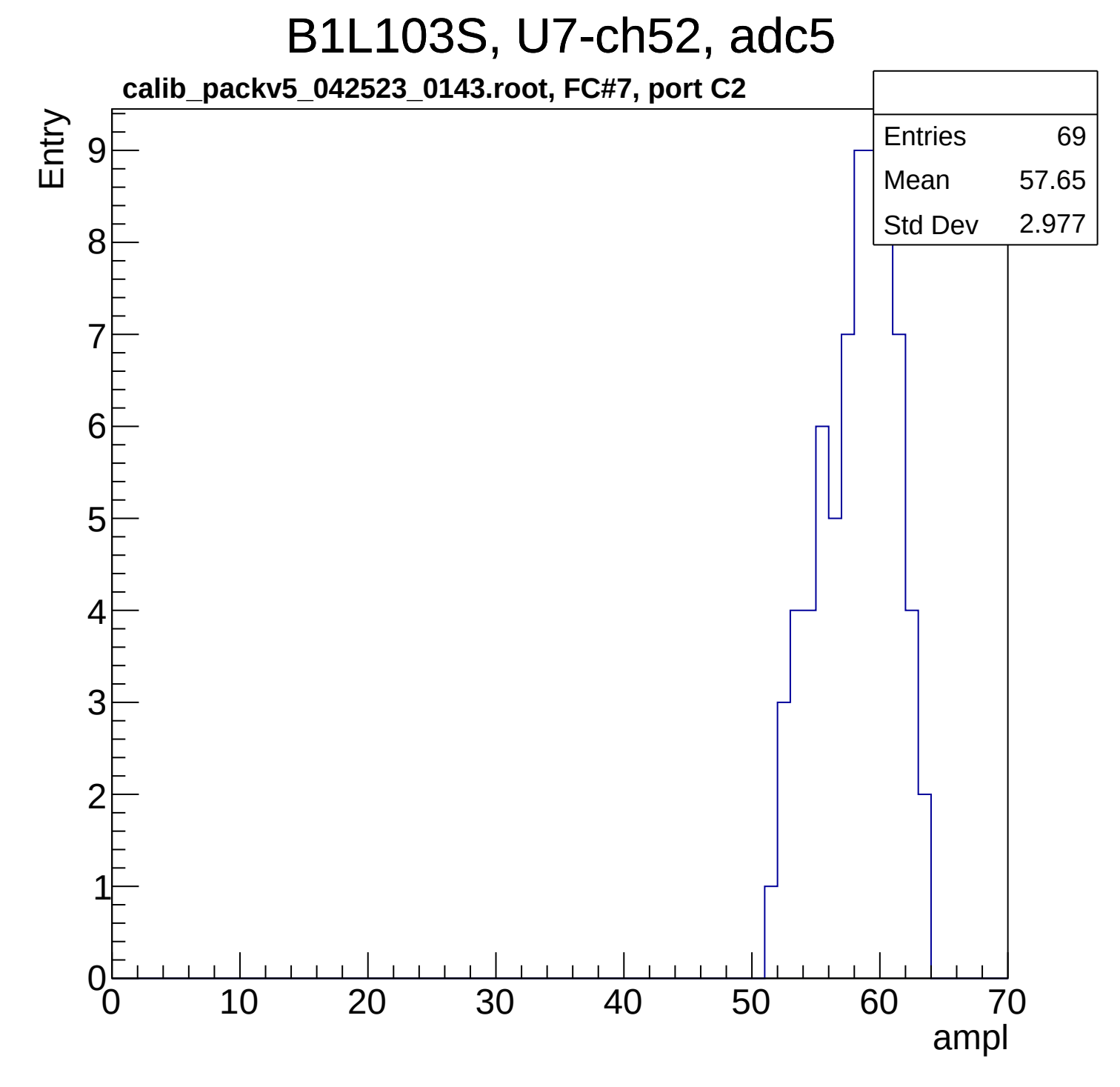
B1L103S, U7-ch52, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 57.65
Std Dev 2.977
Entry
ampl
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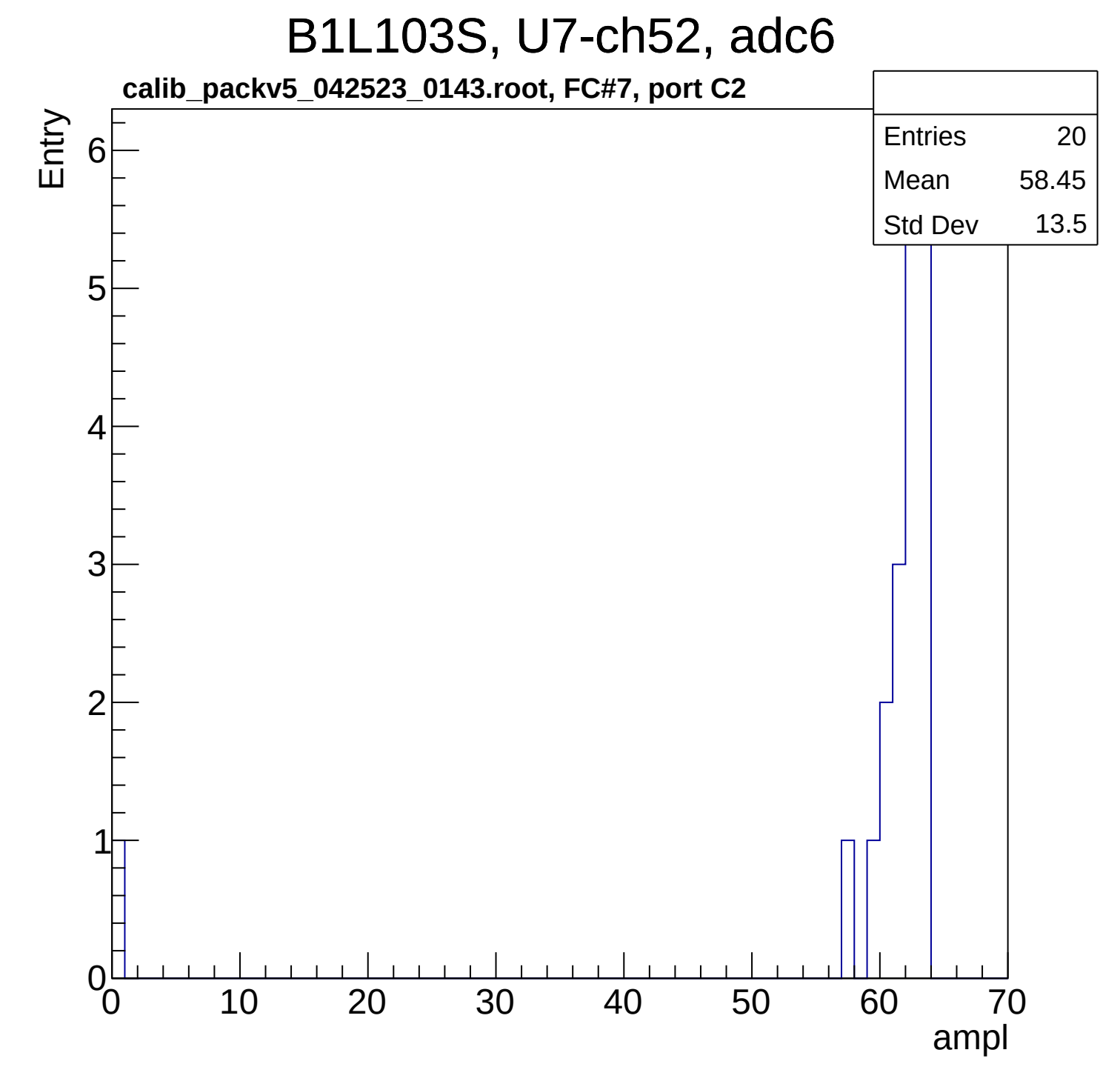
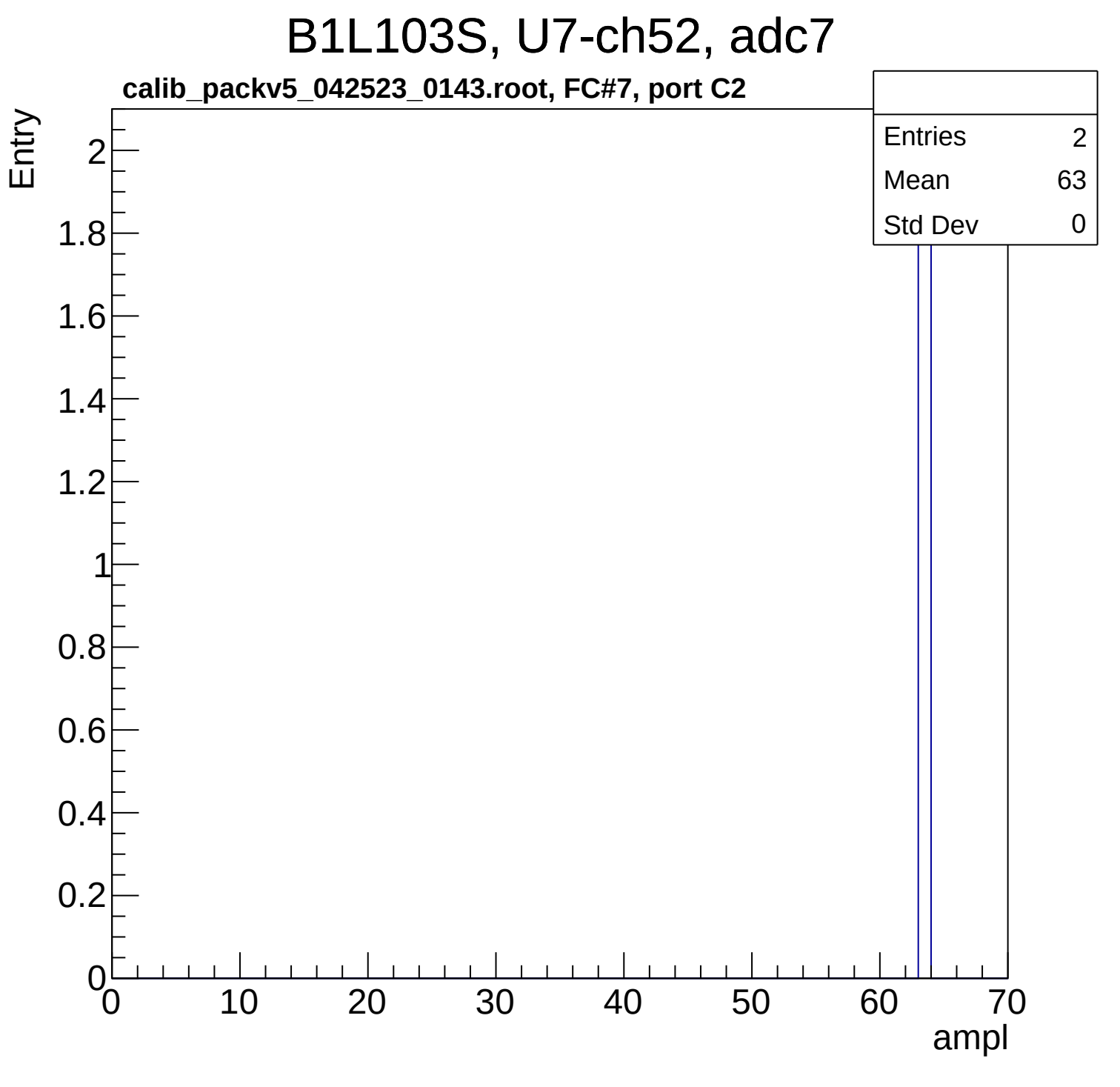
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch52, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 20
Mean 58.45
Std Dev 13.5
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch52, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 63
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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40
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60
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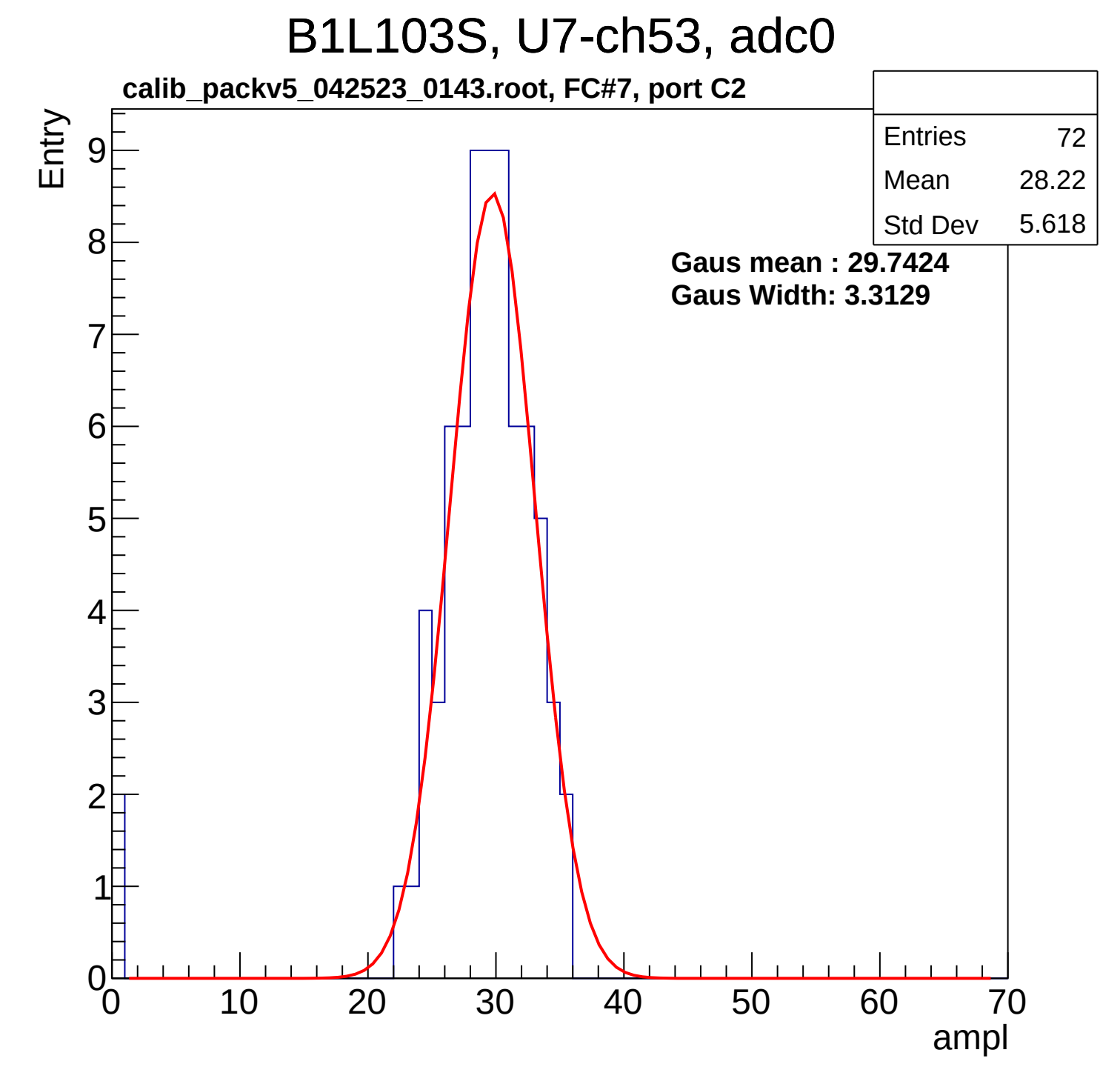
B1L103S, U7-ch53, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 72
Mean 28.22
Std Dev 5.618
Gaus mean : 29.7424
Gaus Width: 3.3129
Entry
ampl
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2
3
4
5
6
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0
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60
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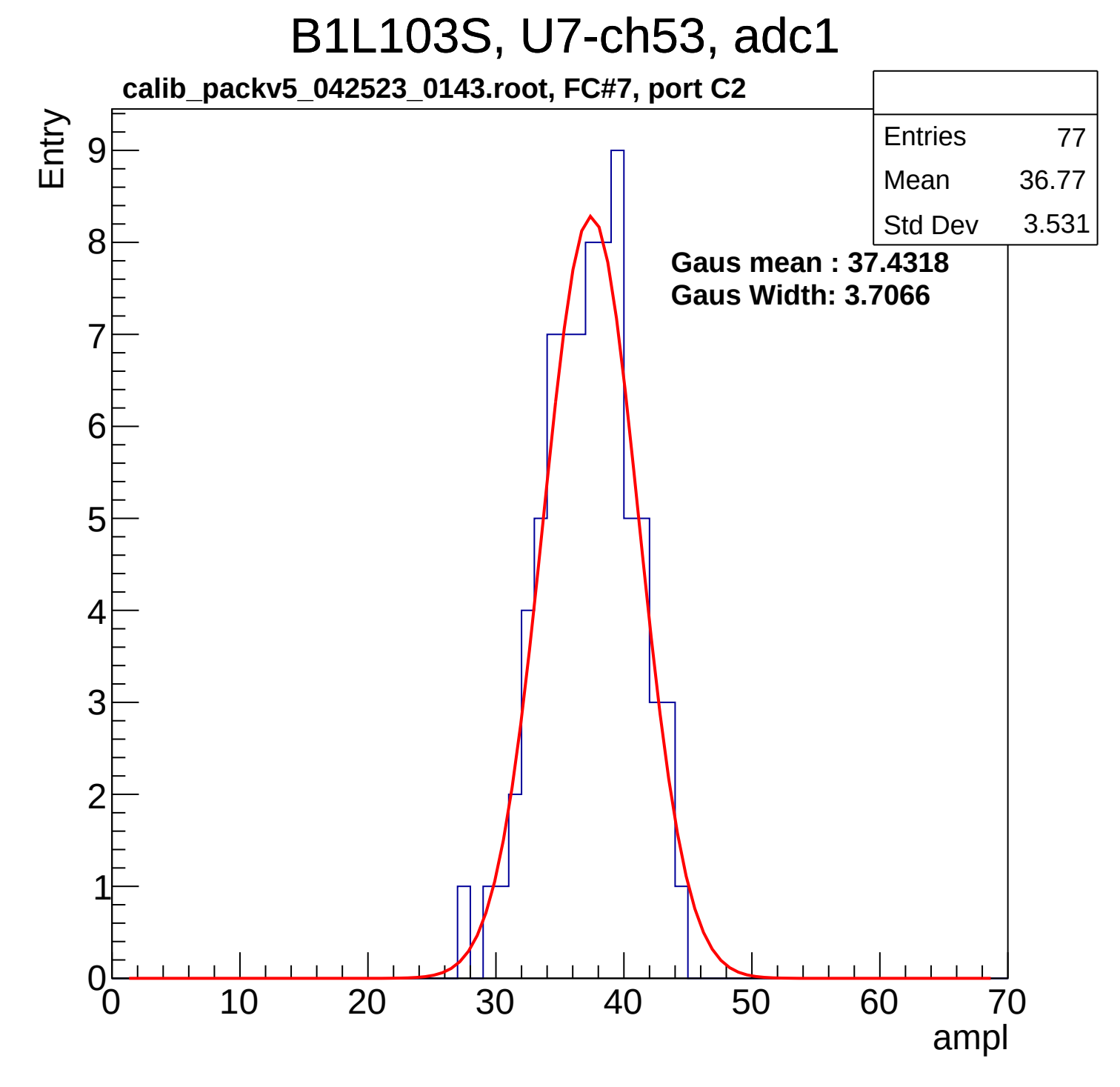
B1L103S, U7-ch53, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 77
Mean 36.77
Std Dev 3.531
Gaus mean : 37.4318
Gaus Width: 3.7066
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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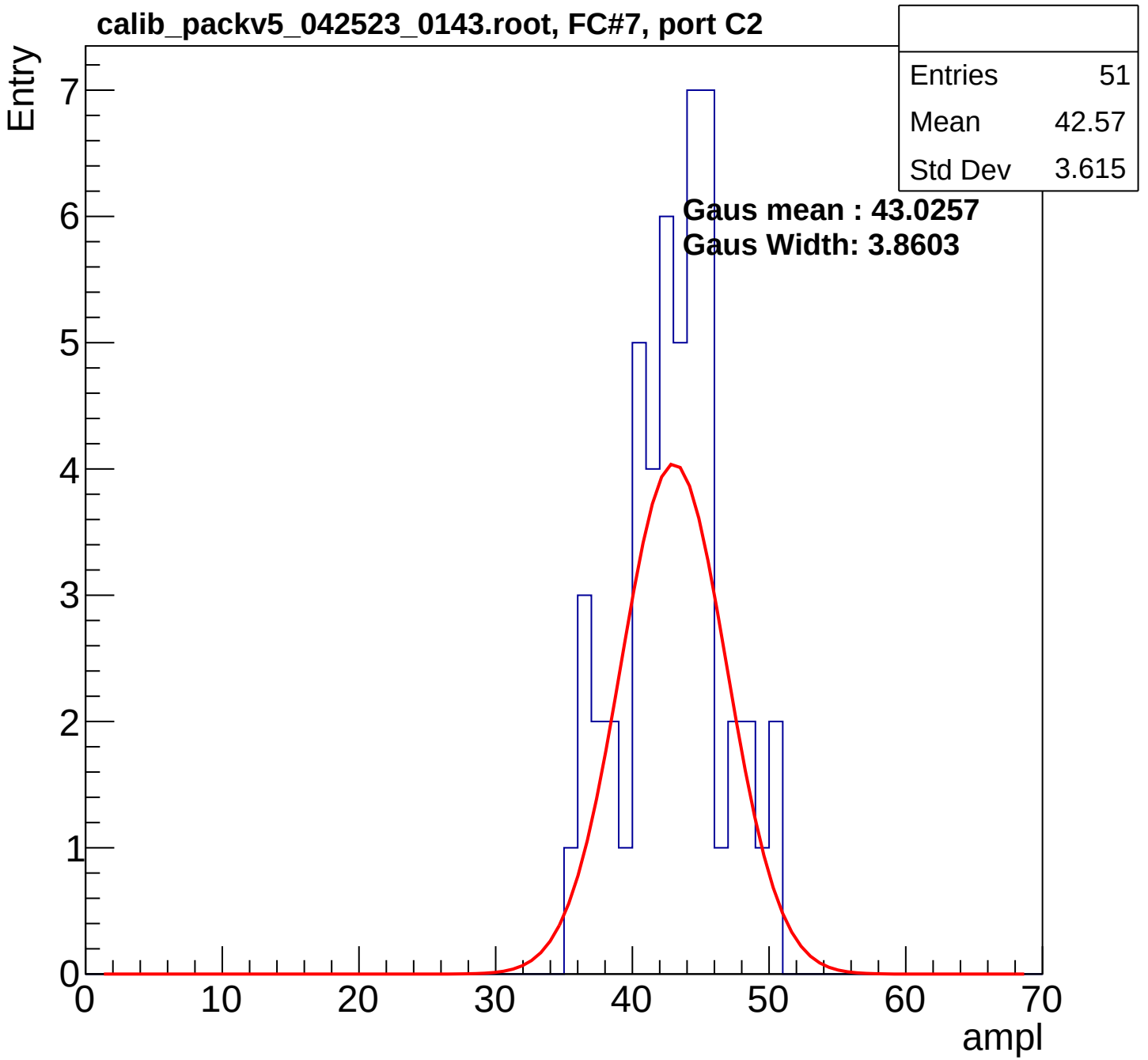
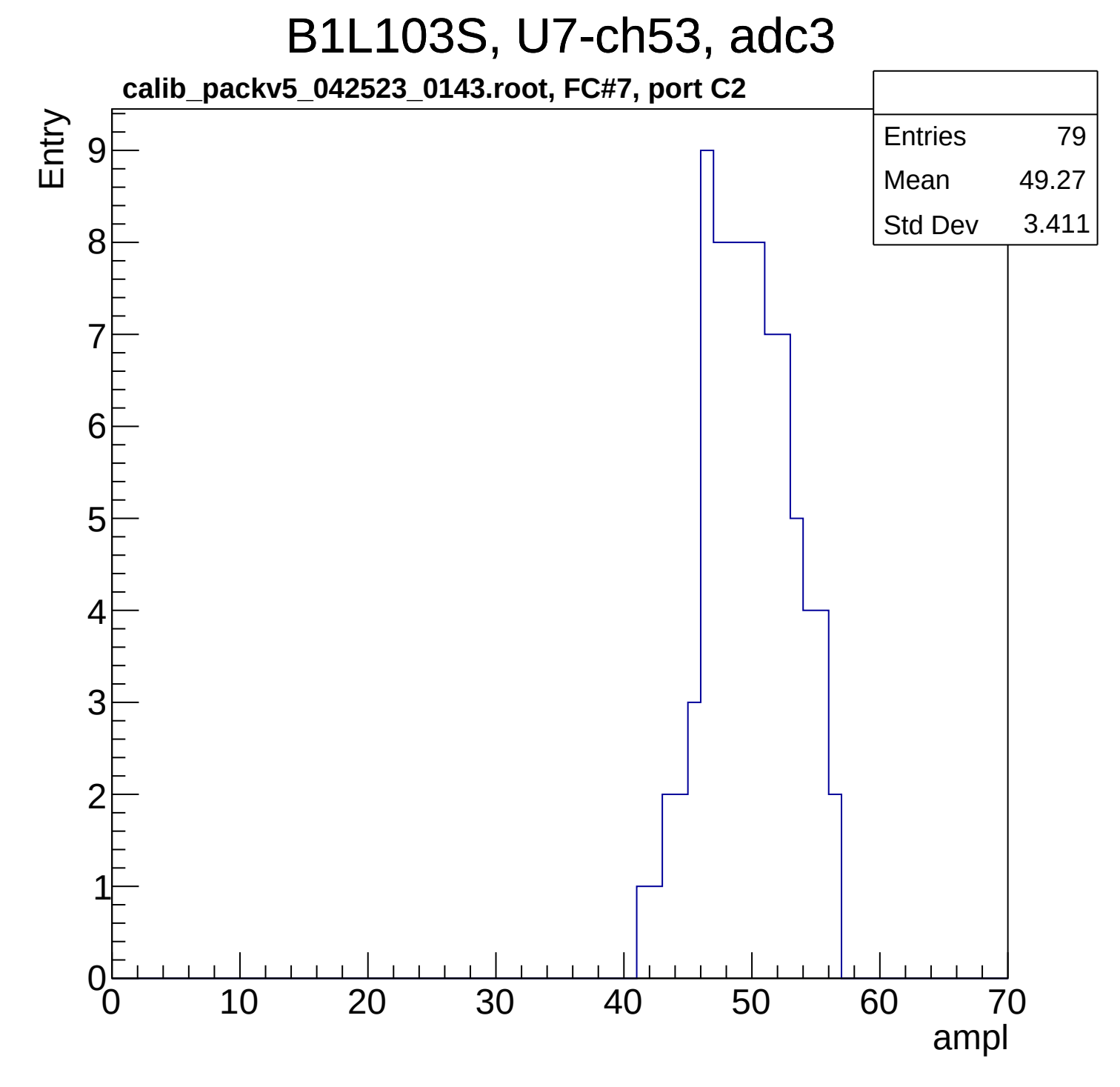

B1L103S, U7-ch53, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 51
Mean 42.57
Std Dev 3.615
Gaus mean : 43.0257
Gaus Width: 3.8603
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch53, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 79
Mean 49.27
Std Dev 3.411
Entry
ampl
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2
3
4
5
6
7
8
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0
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60
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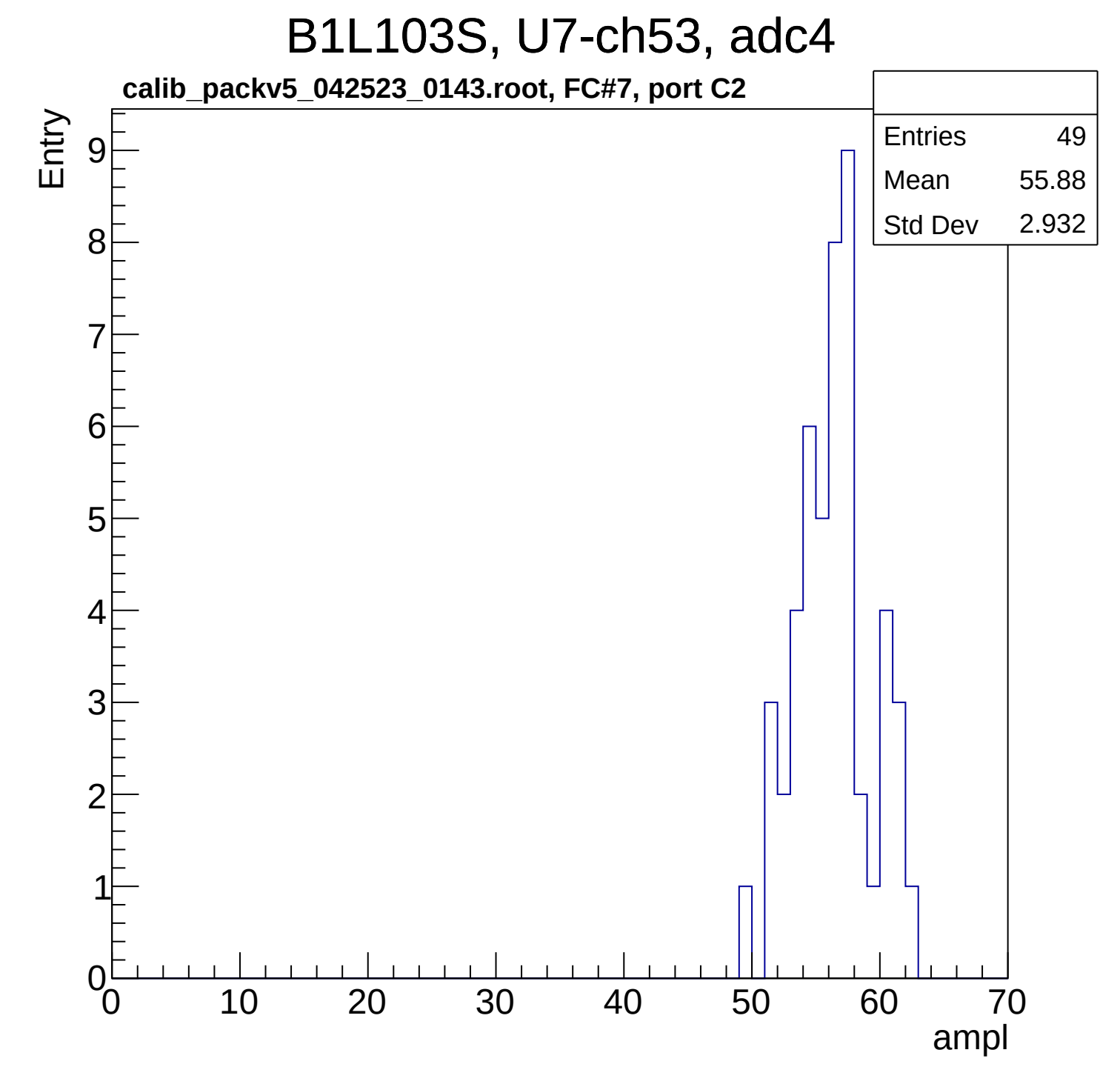
B1L103S, U7-ch53, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 49
Mean 55.88
Std Dev 2.932
Entry
ampl
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1
2
3
4
5
6
7
8
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0
10
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30
40
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60
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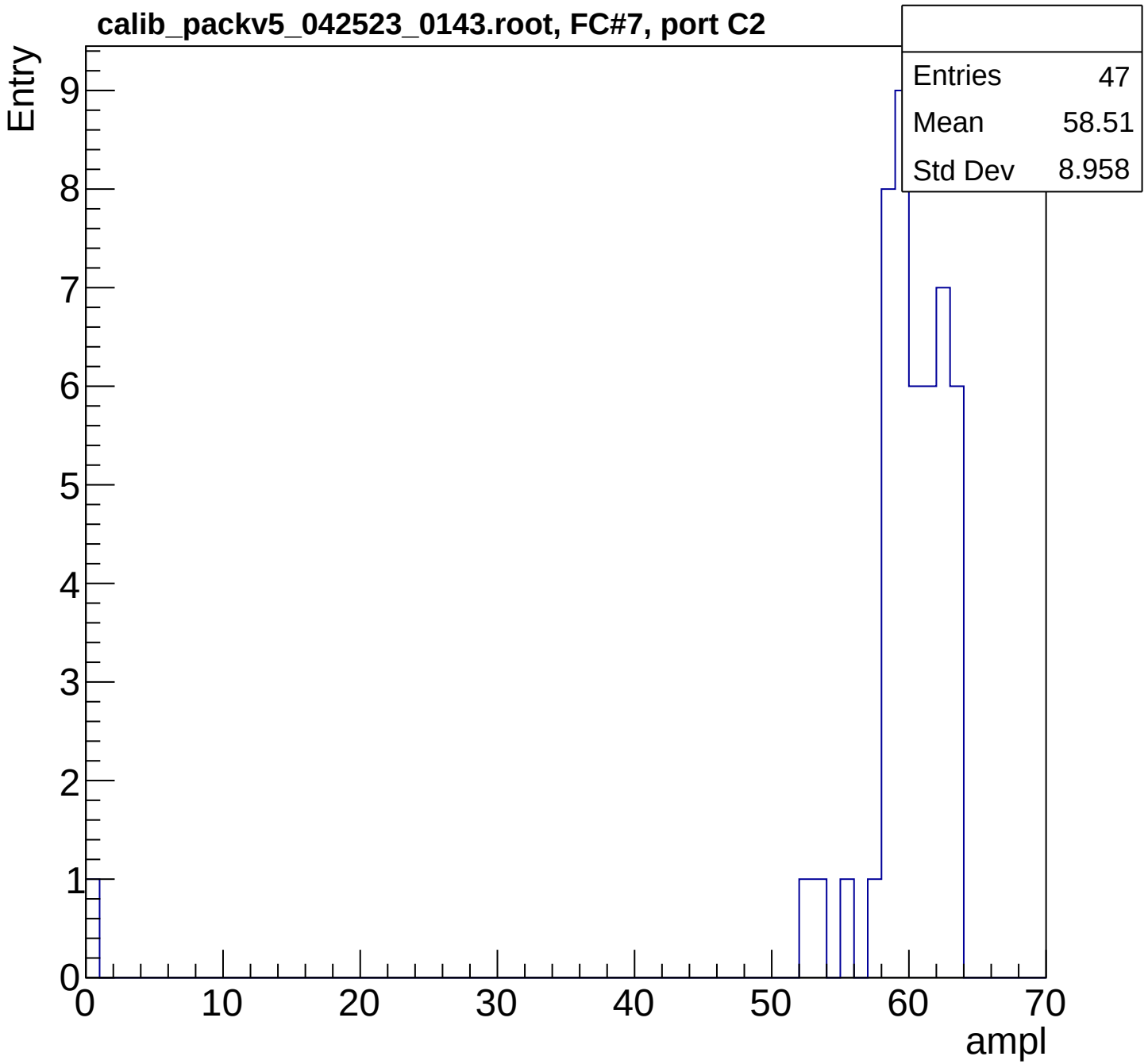
B1L103S, U7-ch53, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 47
Mean 58.51
Std Dev 8.958
Entry
ampl
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2
3
4
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6
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0
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60
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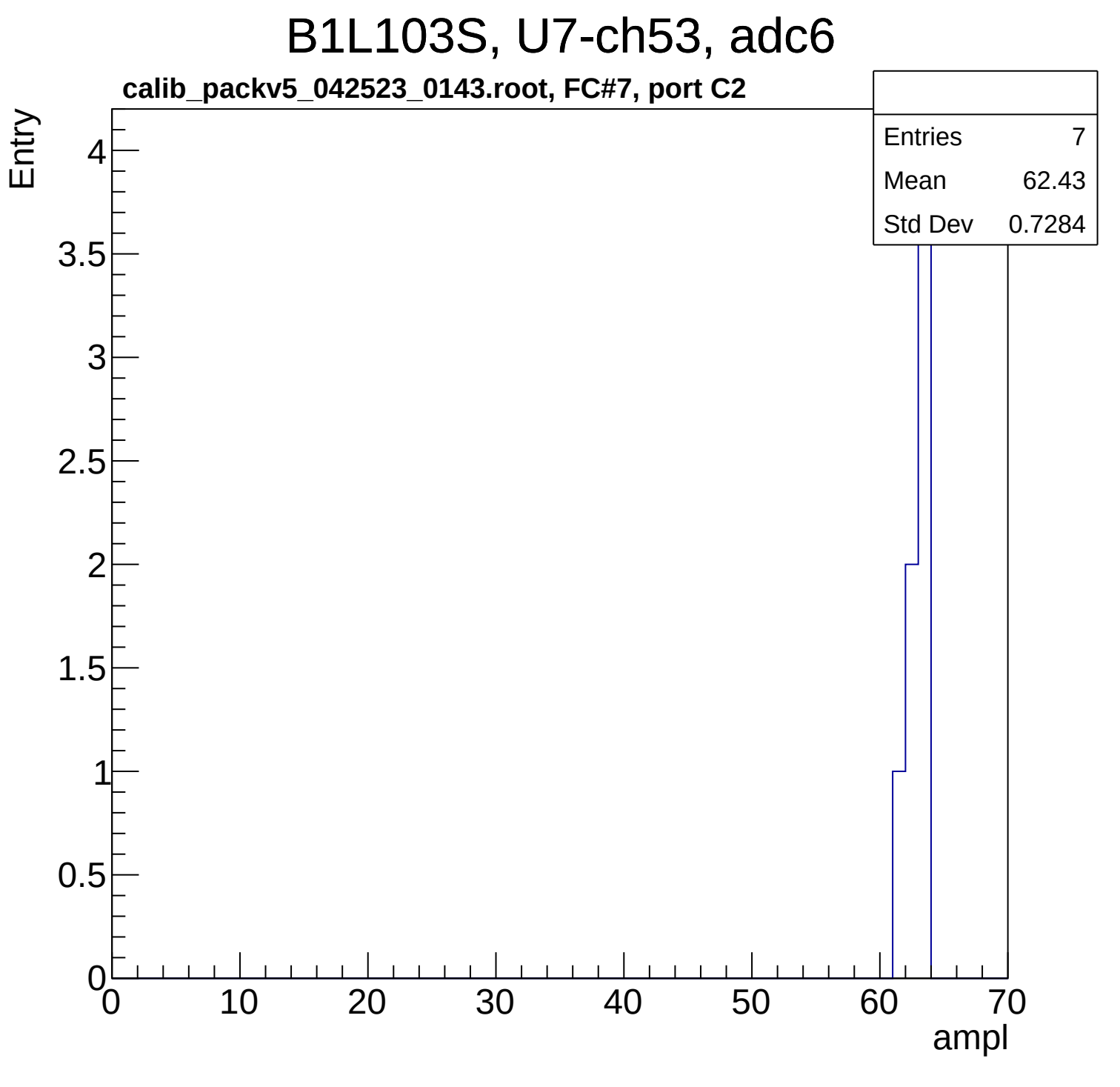
B1L103S, U7-ch53, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 7
Mean 62.43
Std Dev 0.7284
Entry
ampl
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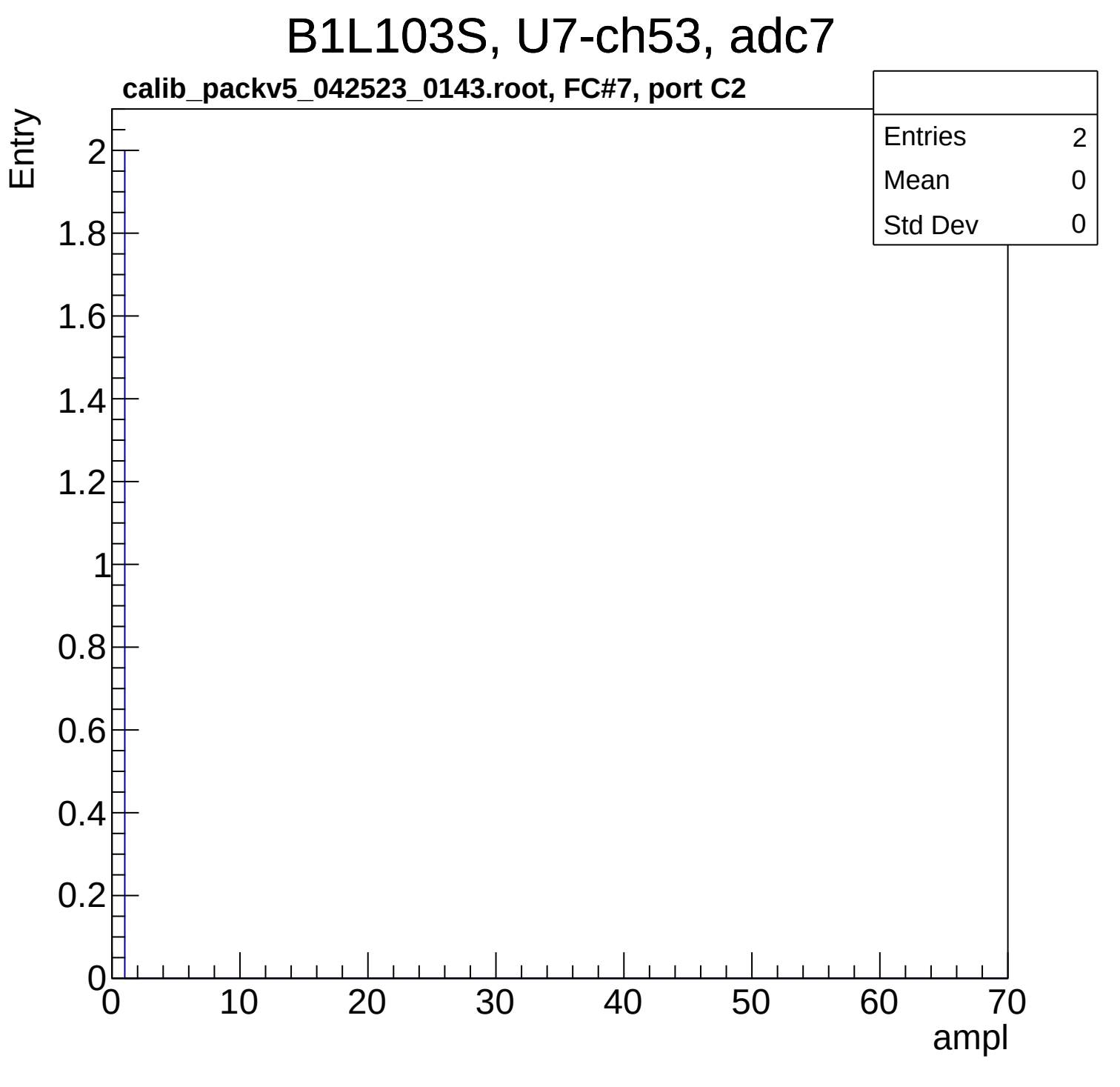
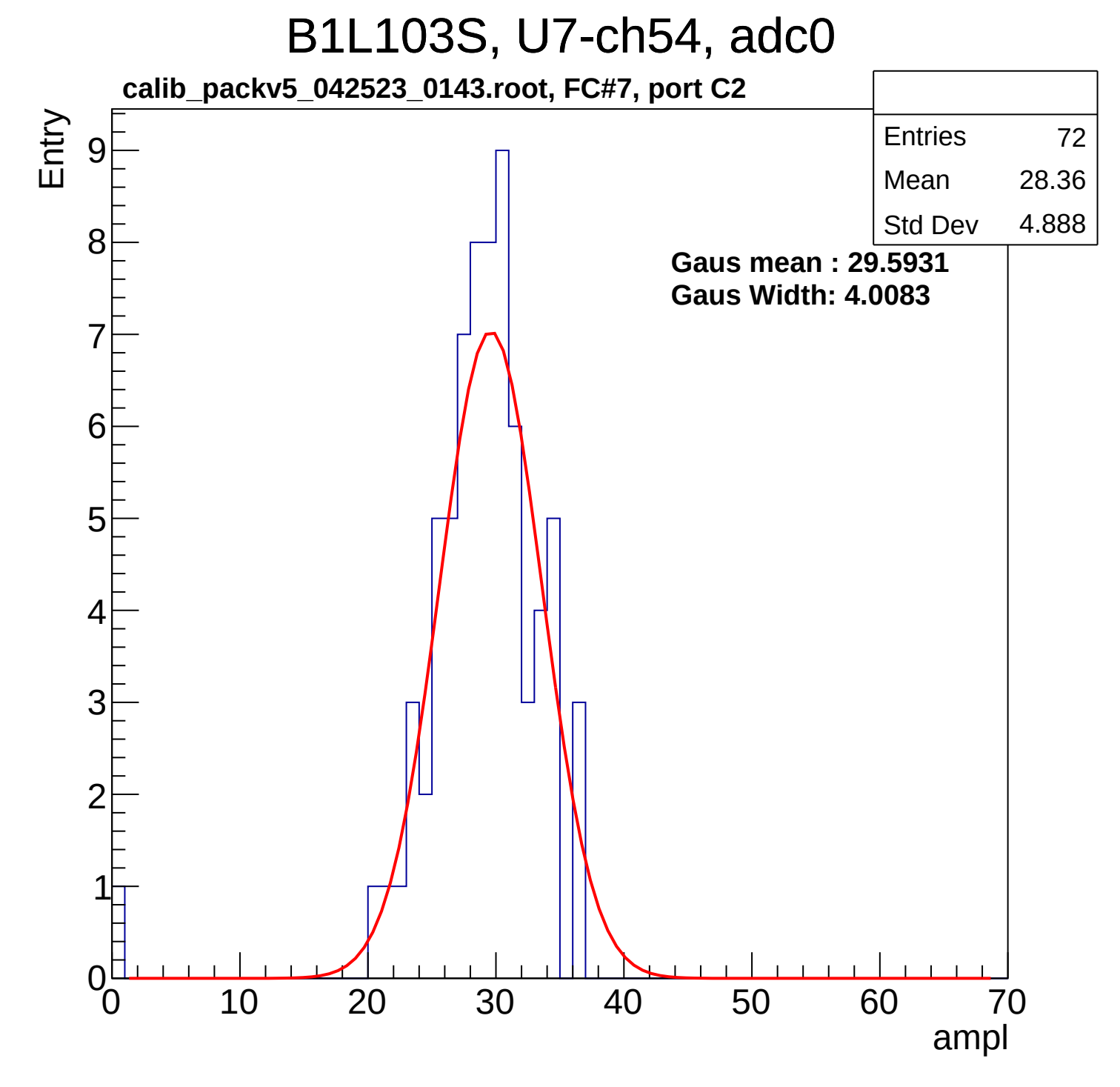
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U7-ch53, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch54, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 72
Mean 28.36
Std Dev 4.888
Gaus mean : 29.5931
Gaus Width: 4.0083
Entry
ampl
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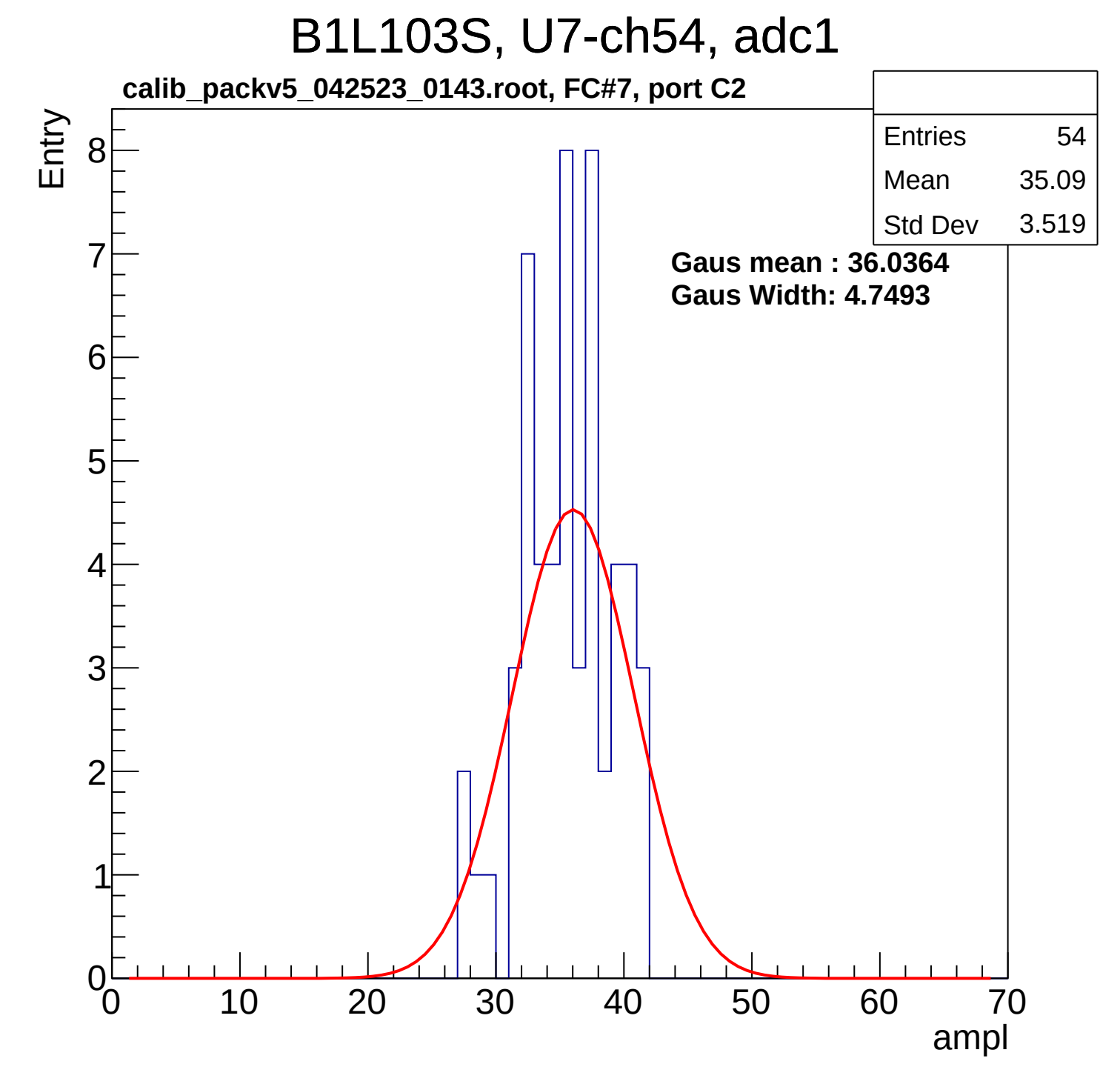
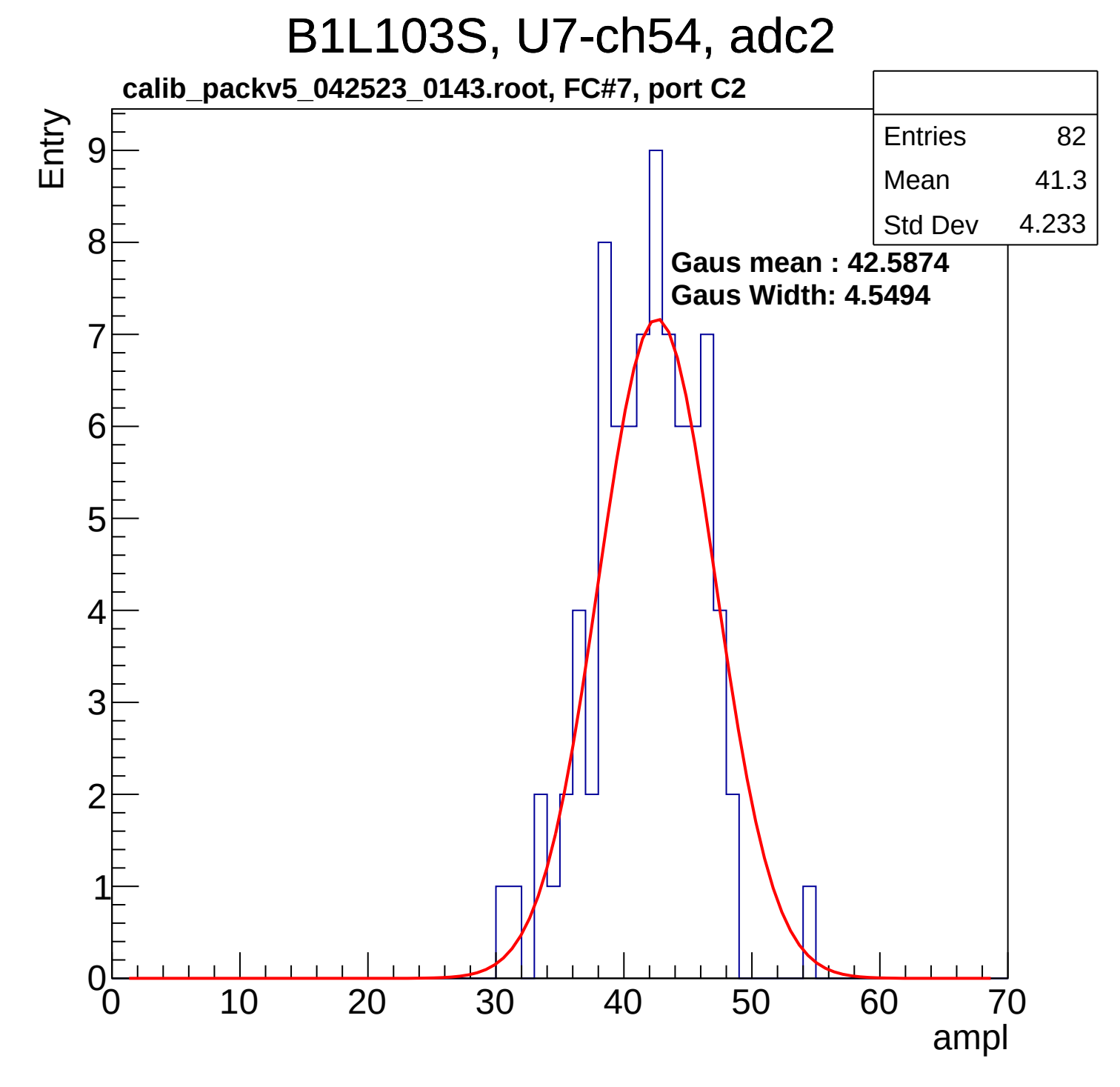
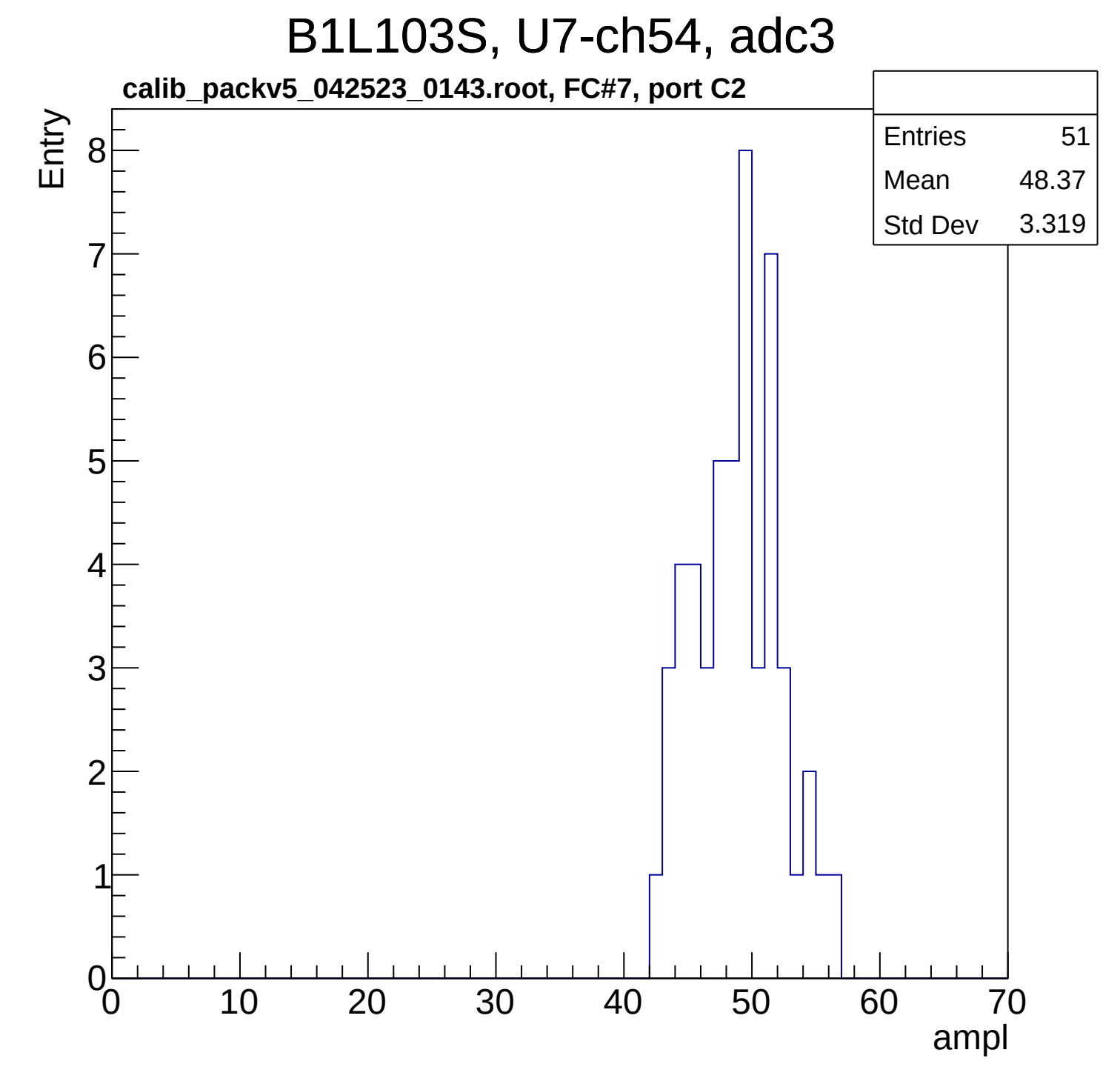
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch54, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 54
Mean 35.09
Std Dev 3.519
Gaus mean : 36.0364
Gaus Width: 4.7493
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch54, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 82
Mean 41.3
Std Dev 4.233
Gaus mean : 42.5874
Gaus Width: 4.5494
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch54, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 51
Mean 48.37
Std Dev 3.319
Entry
ampl
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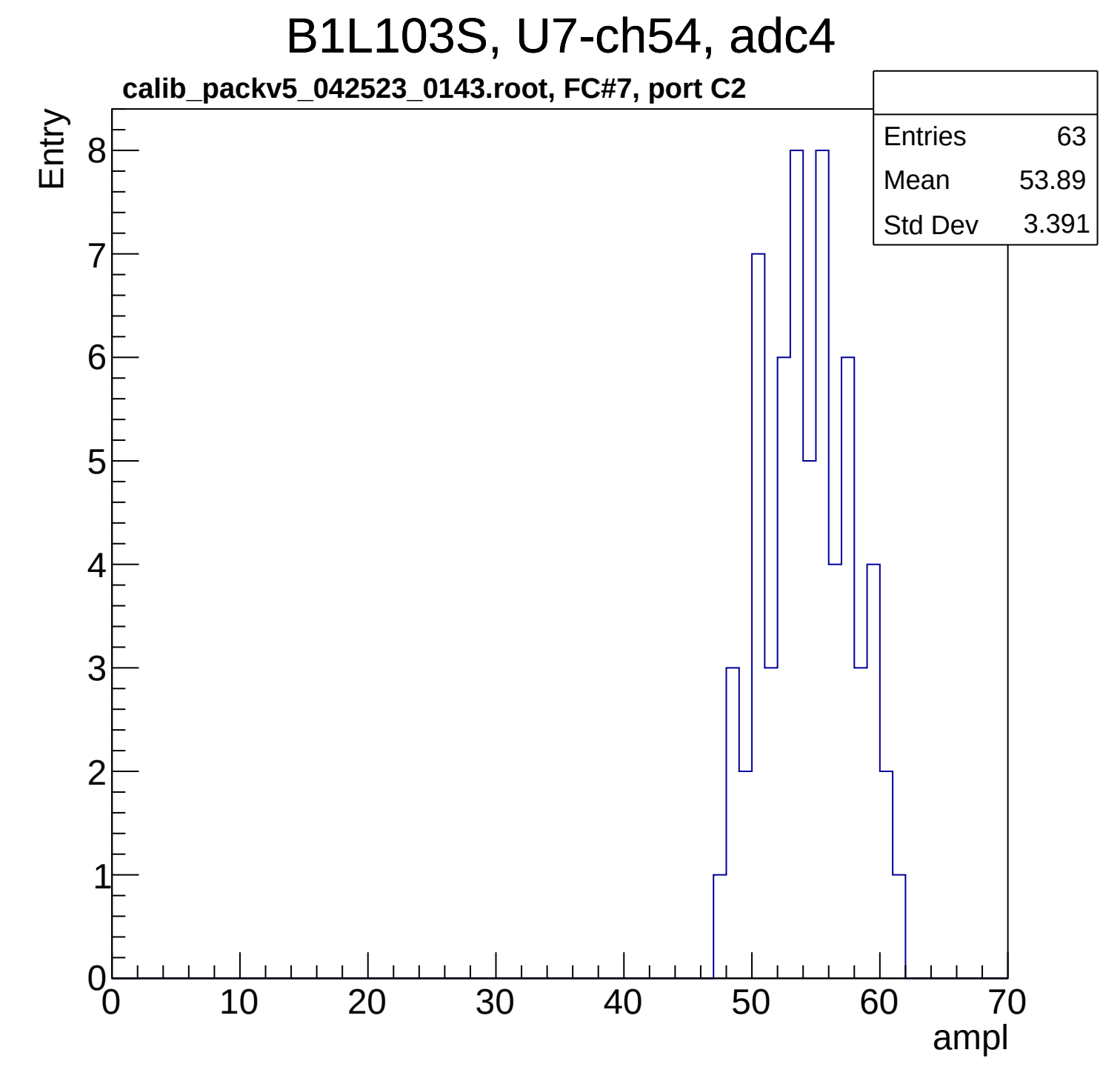
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch54, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 53.89
Std Dev 3.391
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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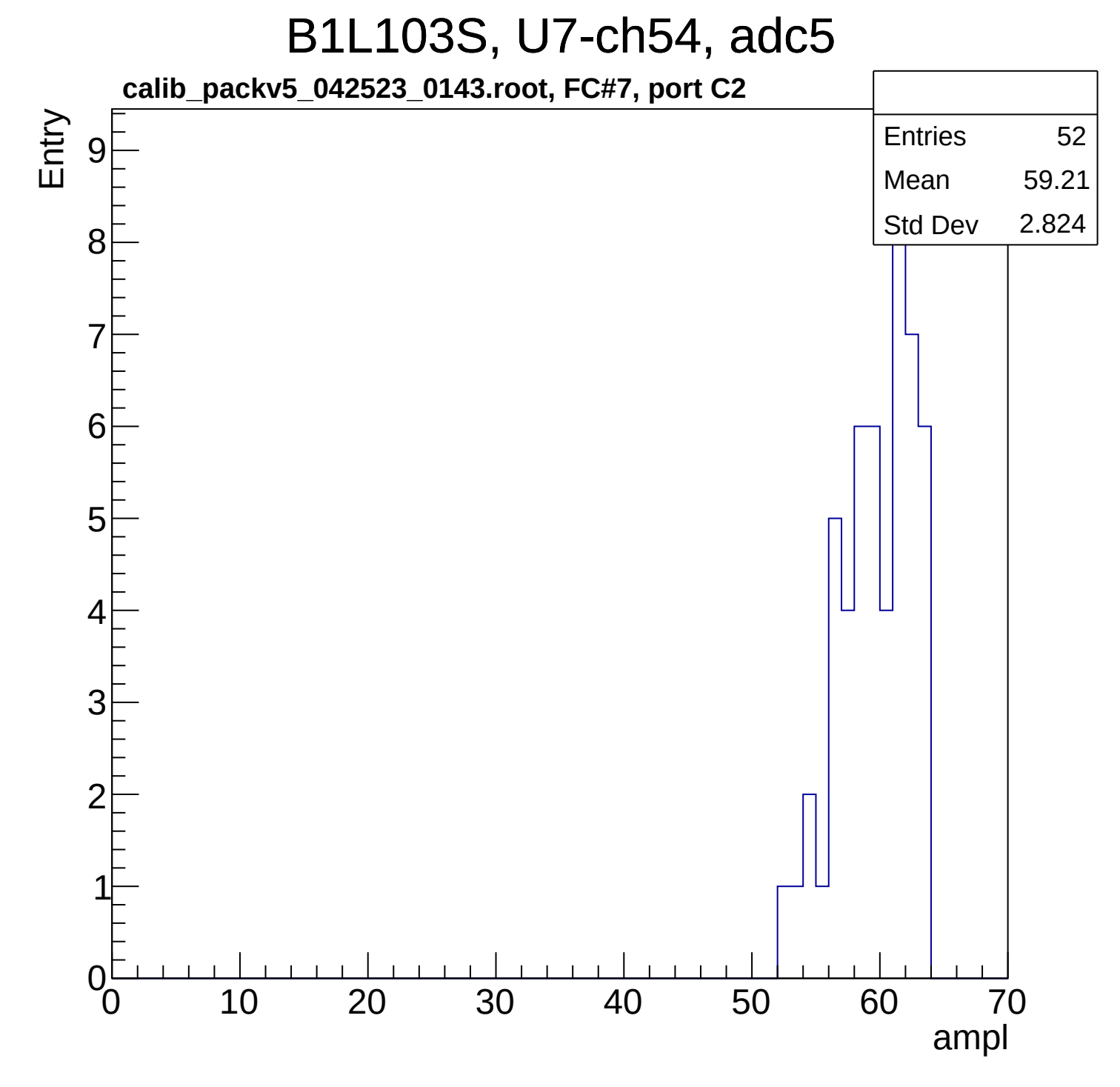
B1L103S, U7-ch54, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 52
Mean 59.21
Std Dev 2.824
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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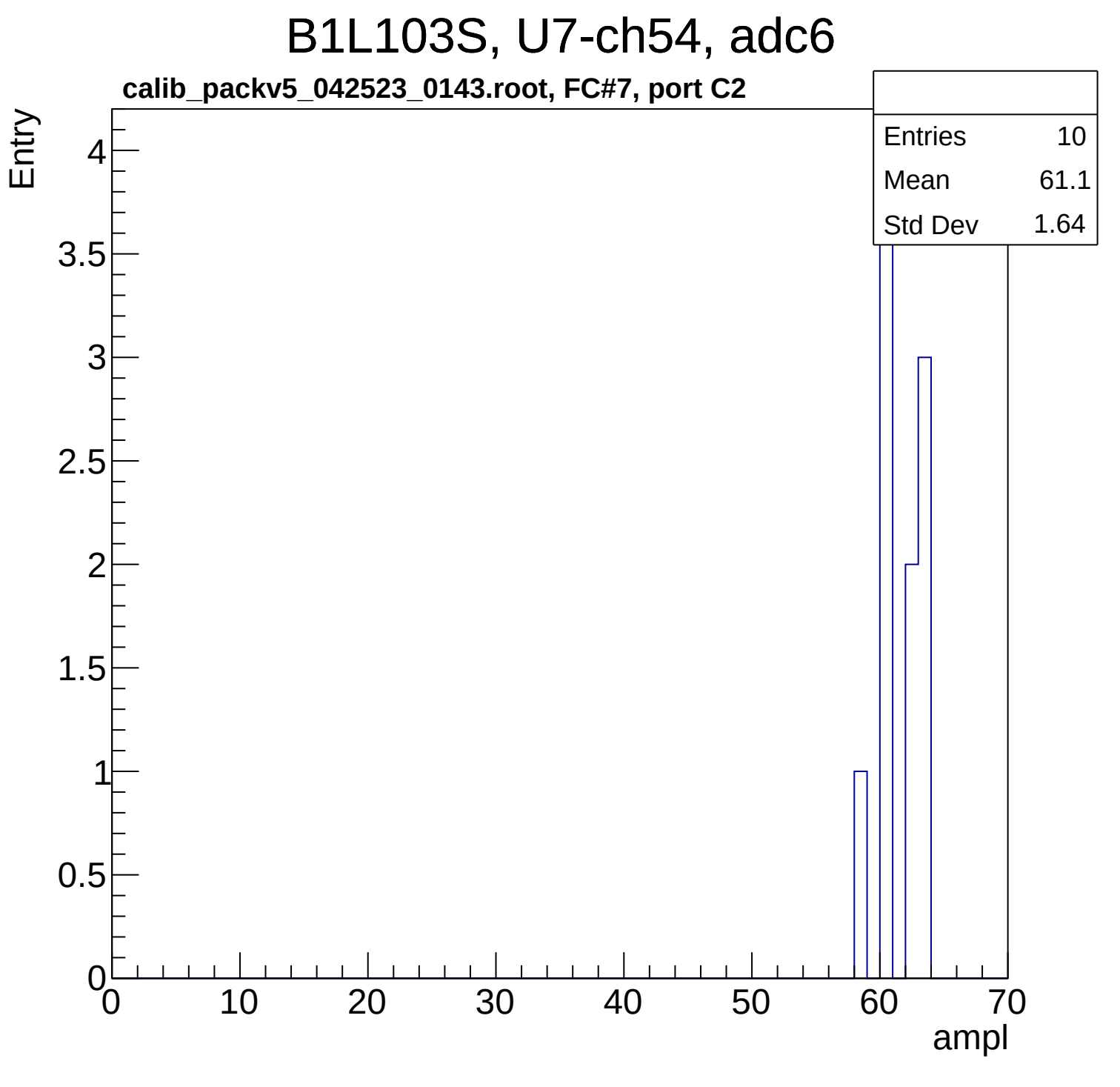
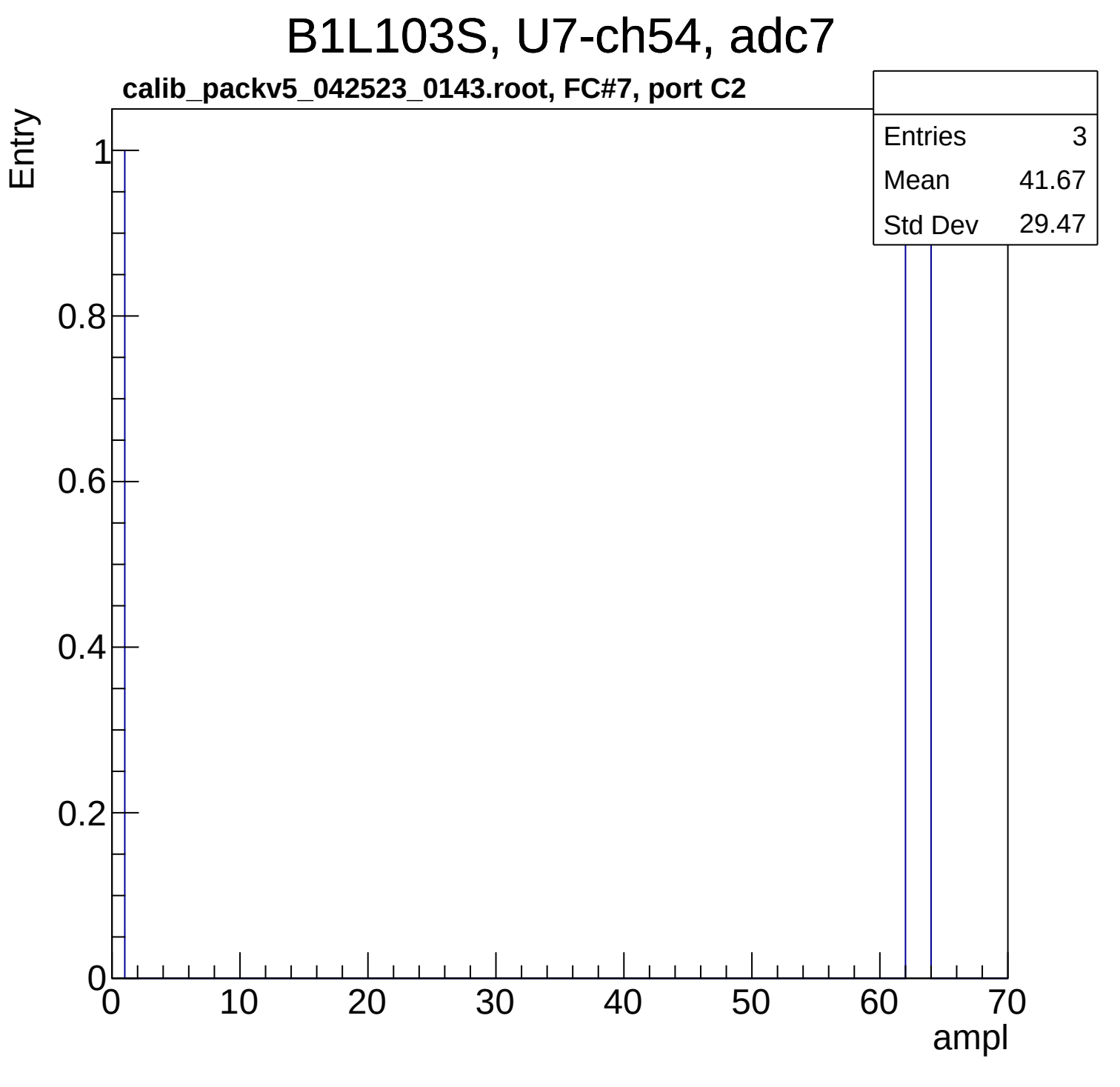
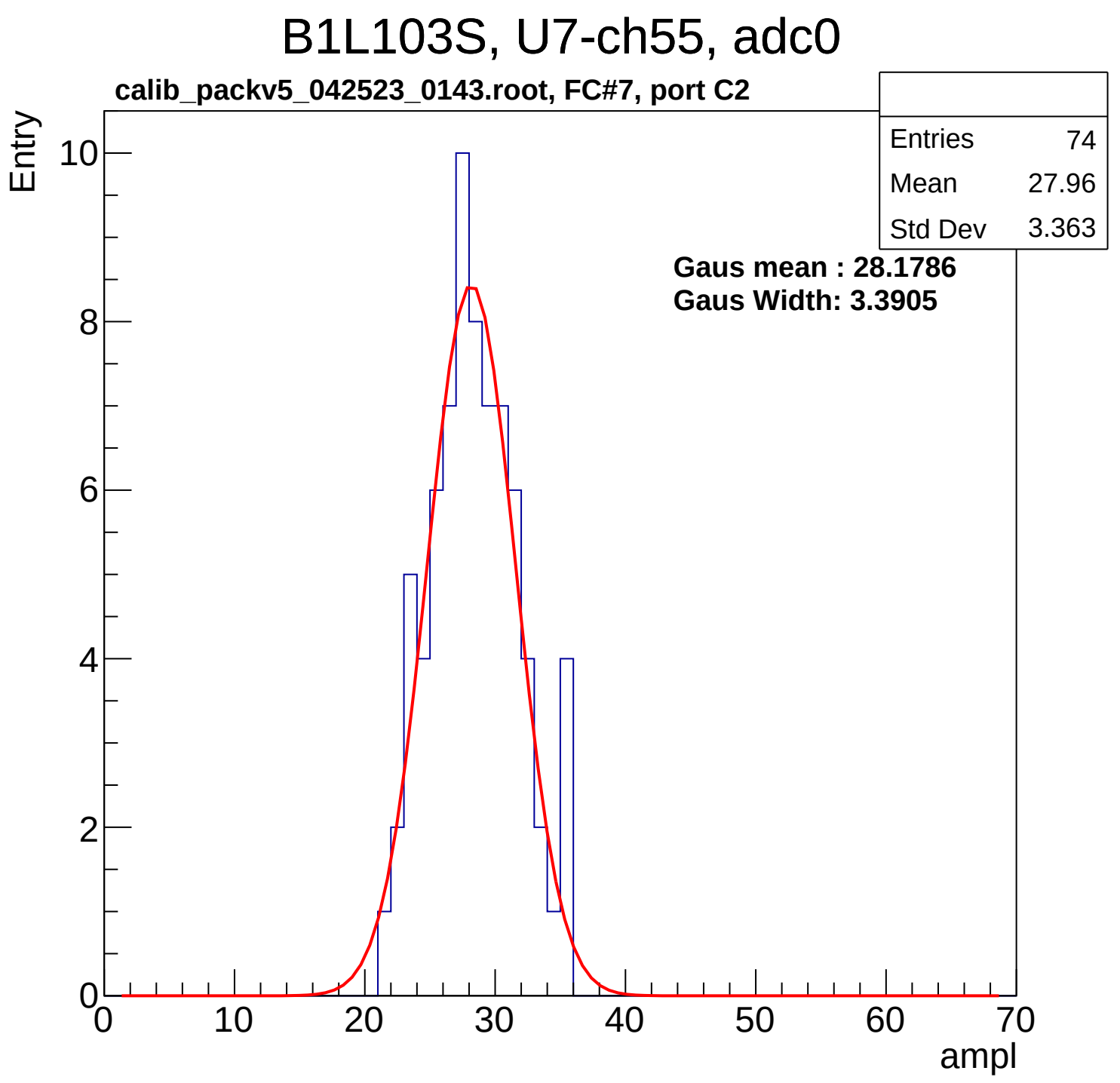
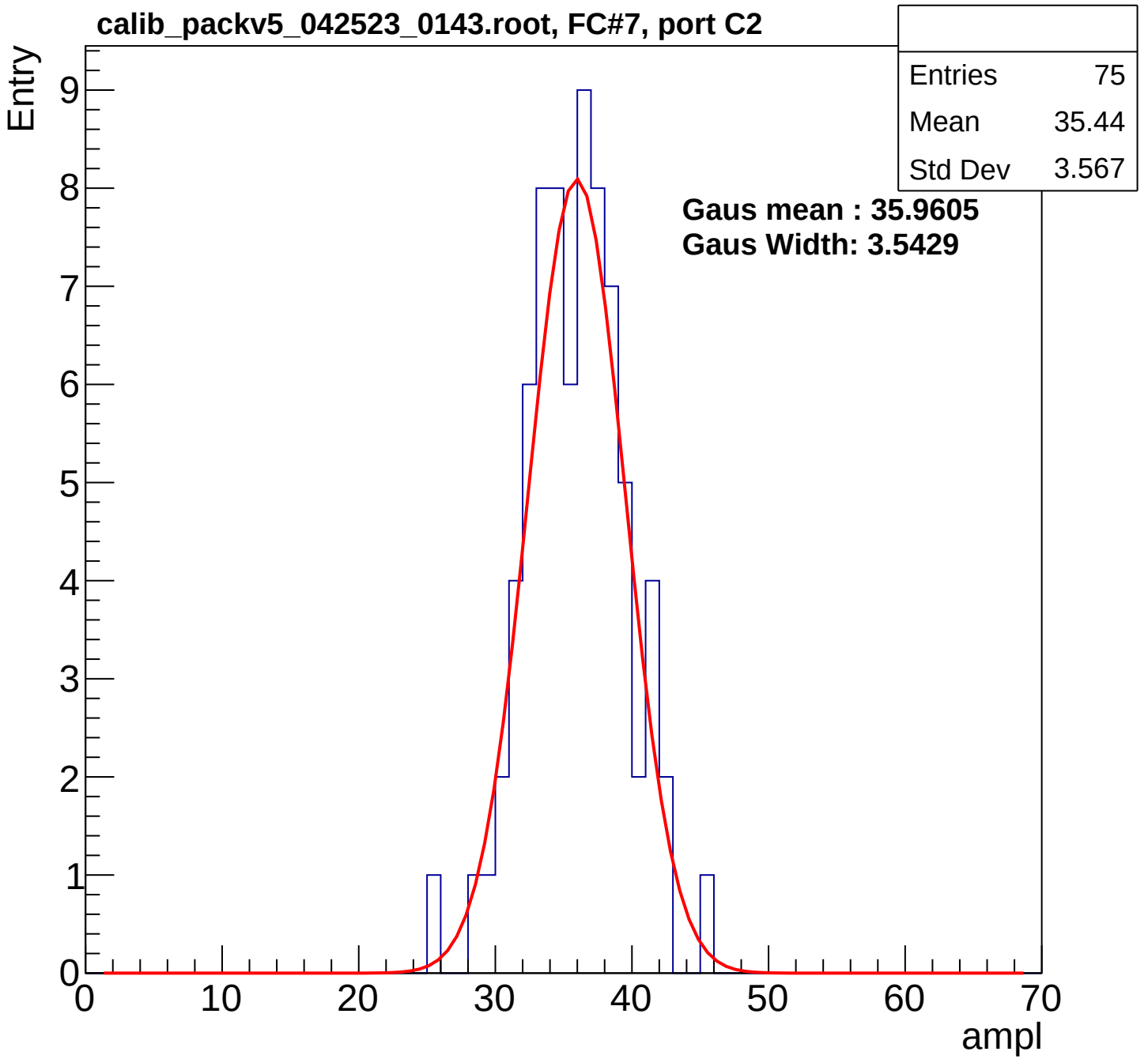
40
50
60
70


B1L103S, U7-ch54, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 10
Mean 61.1
Std Dev 1.64
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U7-ch54, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 41.67
Std Dev 29.47
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch55, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 74
Mean 27.96
Std Dev 3.363
Gaus mean : 28.1786
Gaus Width: 3.3905
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch55, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 75
Mean 35.44
Std Dev 3.567
Gaus mean : 35.9605
Gaus Width: 3.5429
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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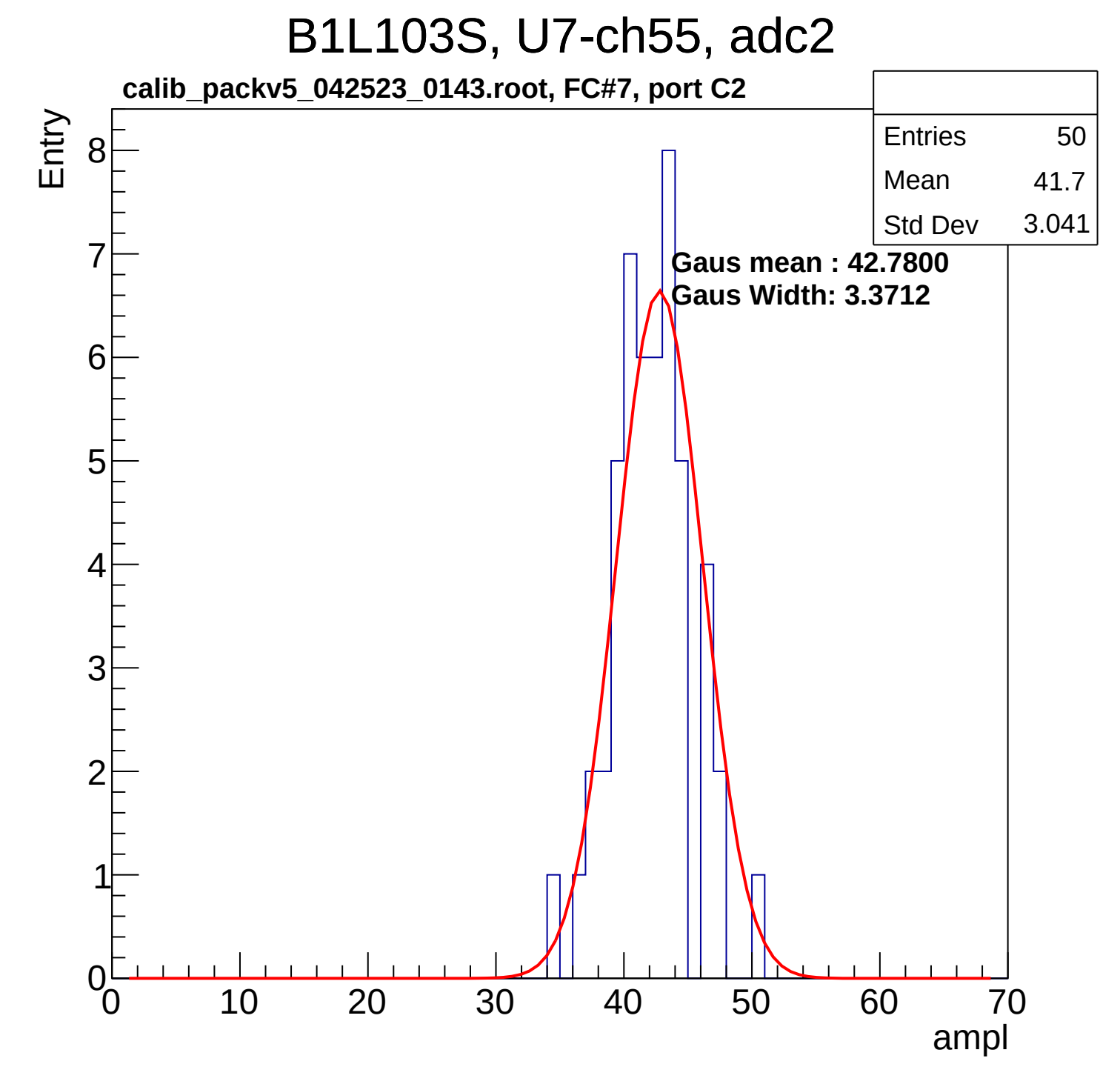
B1L103S, U7-ch55, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 50
Mean 41.7
Std Dev 3.041
Gaus mean : 42.7800
Gaus Width: 3.3712
Entry
ampl
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1
2
3
4
5
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7
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0
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20
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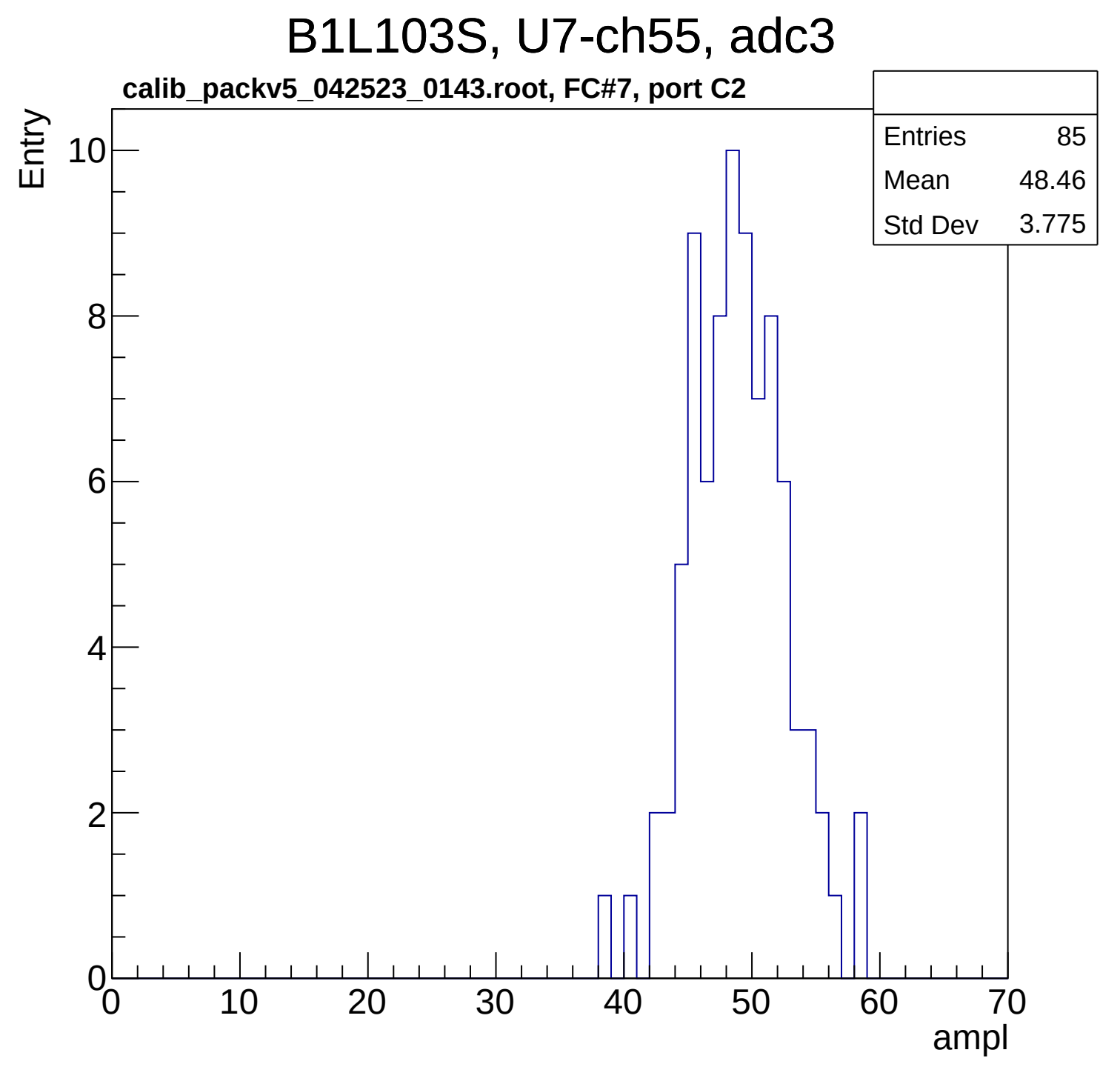
B1L103S, U7-ch55, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 85
Mean 48.46
Std Dev 3.775
Entry
ampl
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2
4
6
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0
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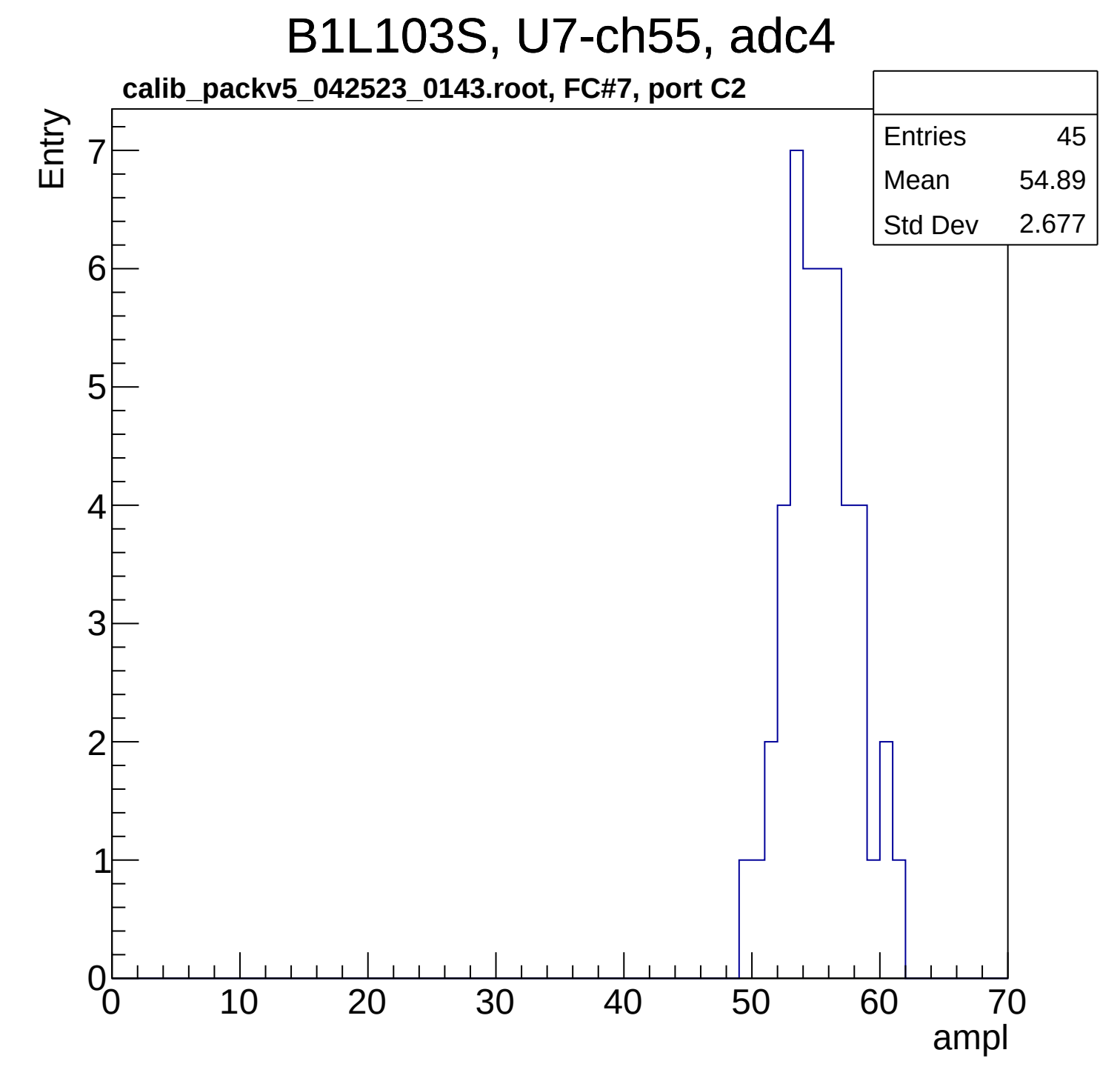
B1L103S, U7-ch55, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 45
Mean 54.89
Std Dev 2.677
Entry
ampl
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1
2
3
4
5
6
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0
10
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60
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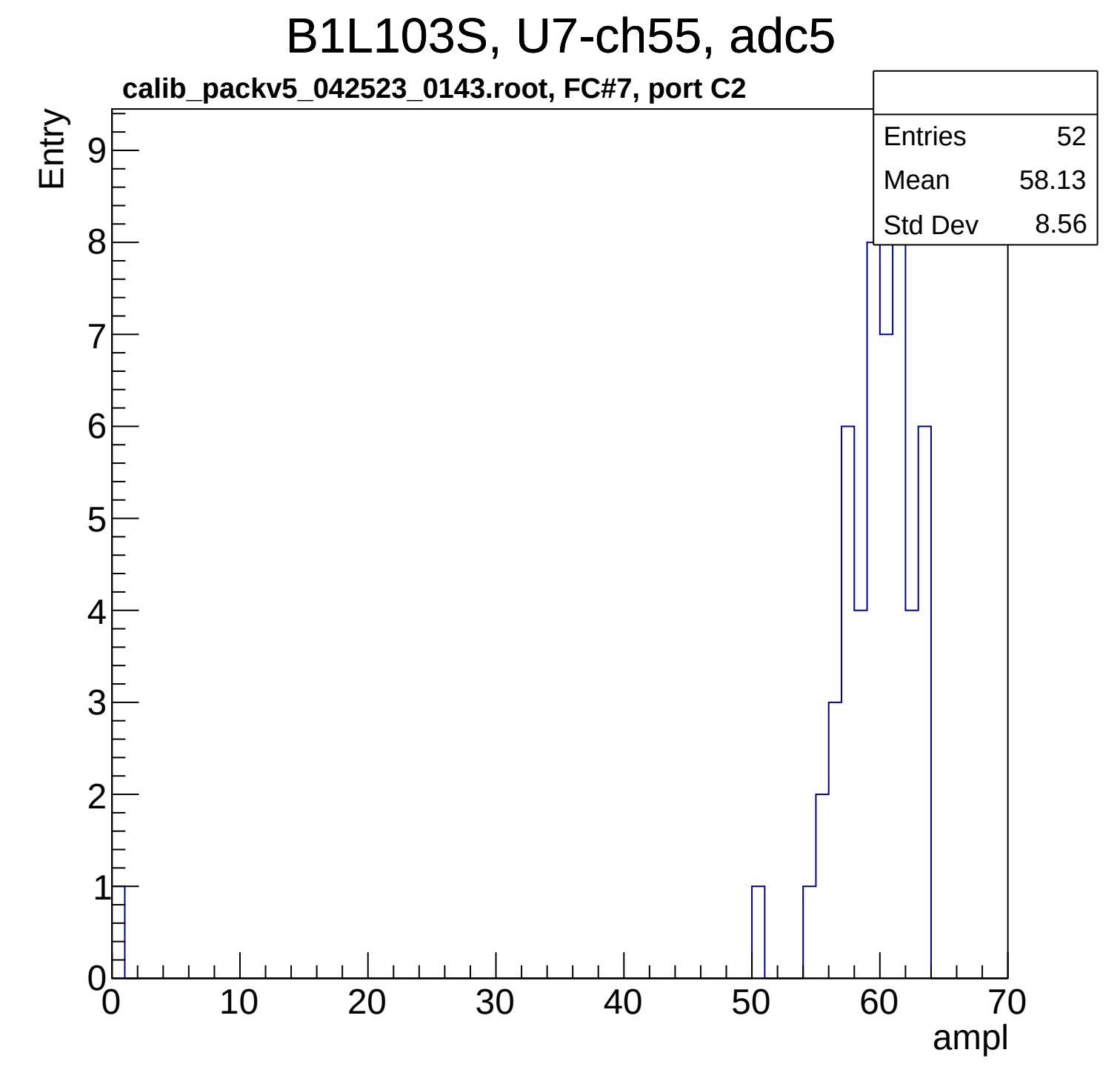
B1L103S, U7-ch55, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 52
Mean 58.13
Std Dev 8.56
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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60
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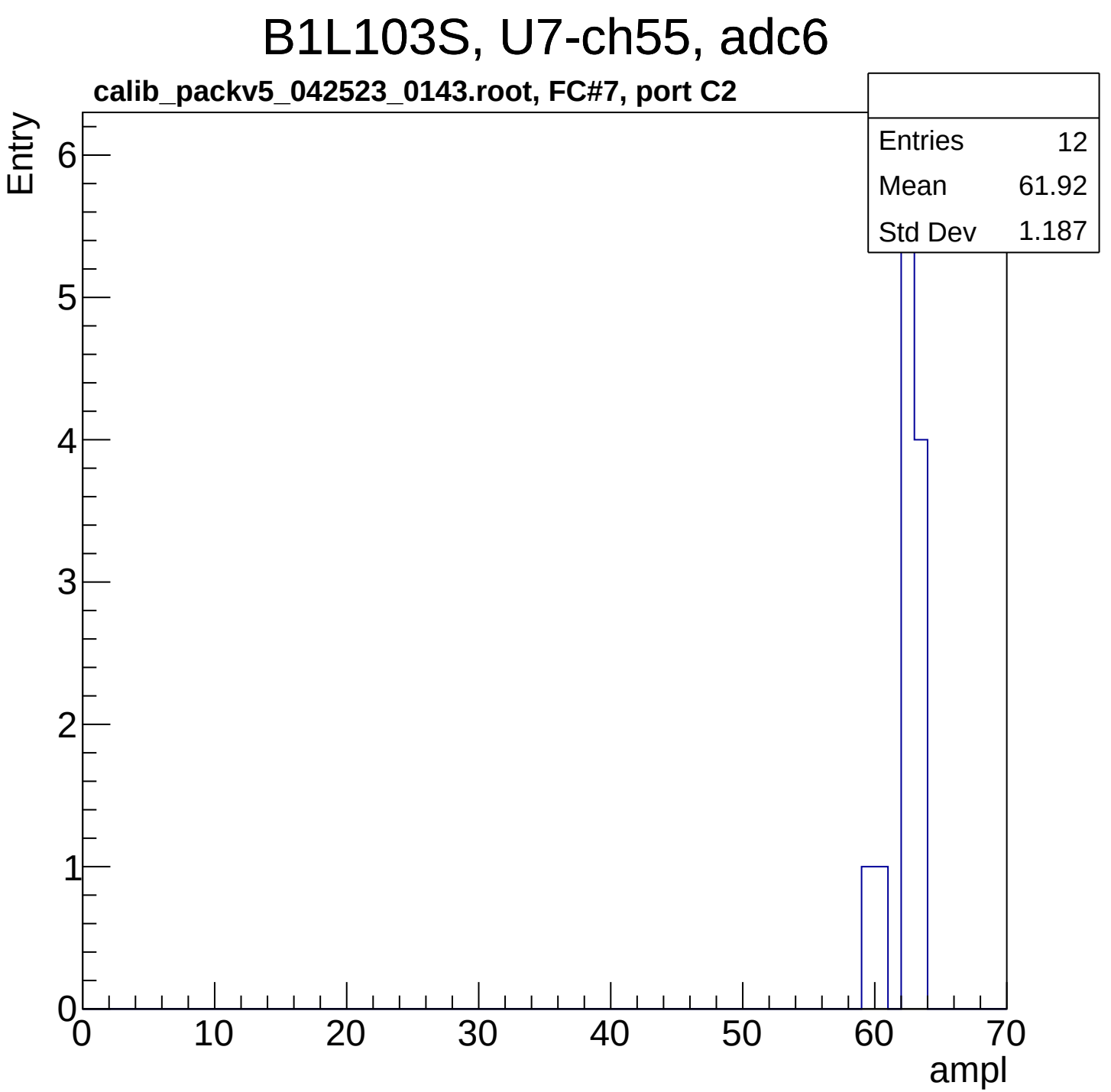
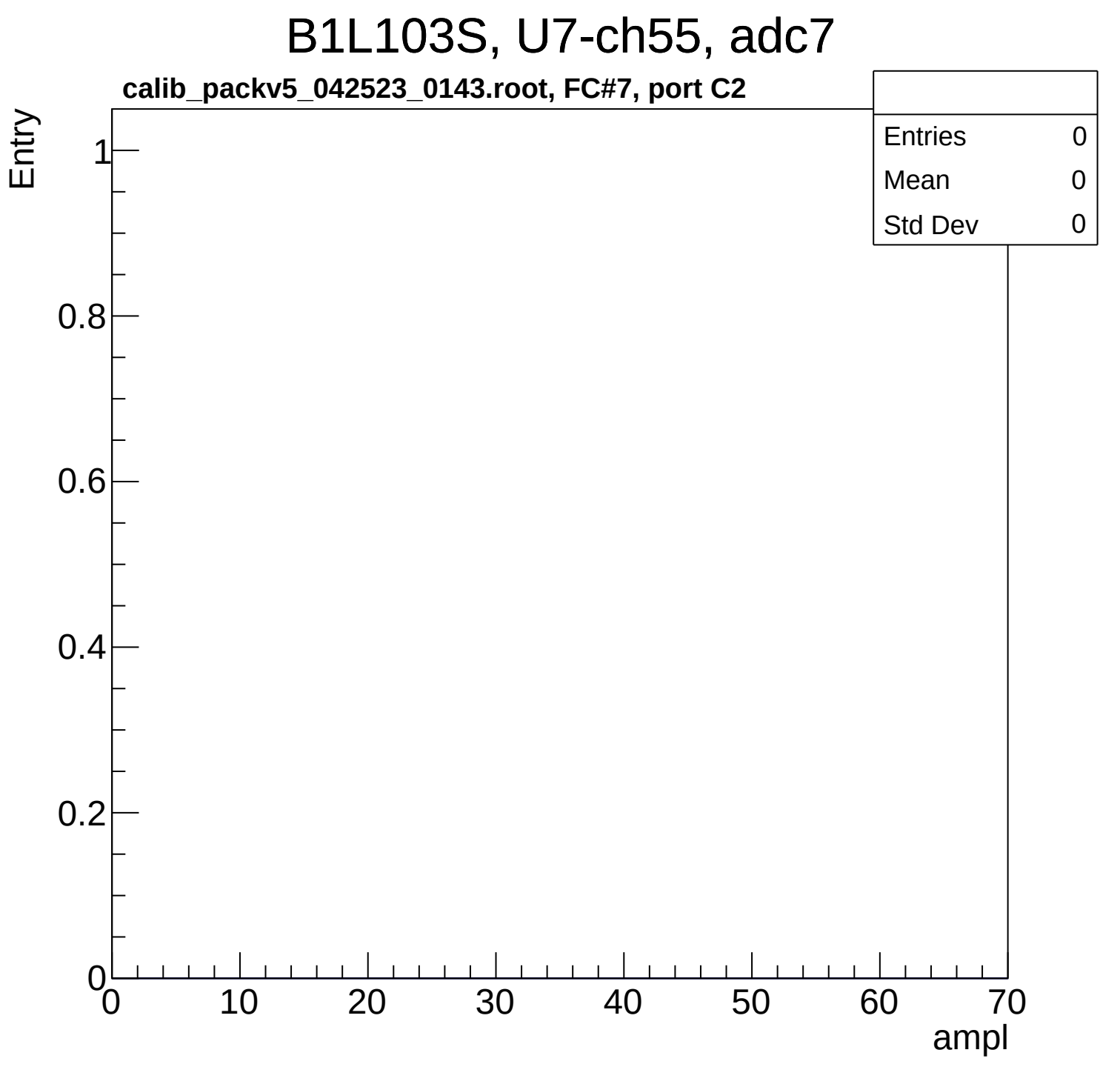

B1L103S, U7-ch55, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 12
Mean 61.92
Std Dev 1.187
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch55, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
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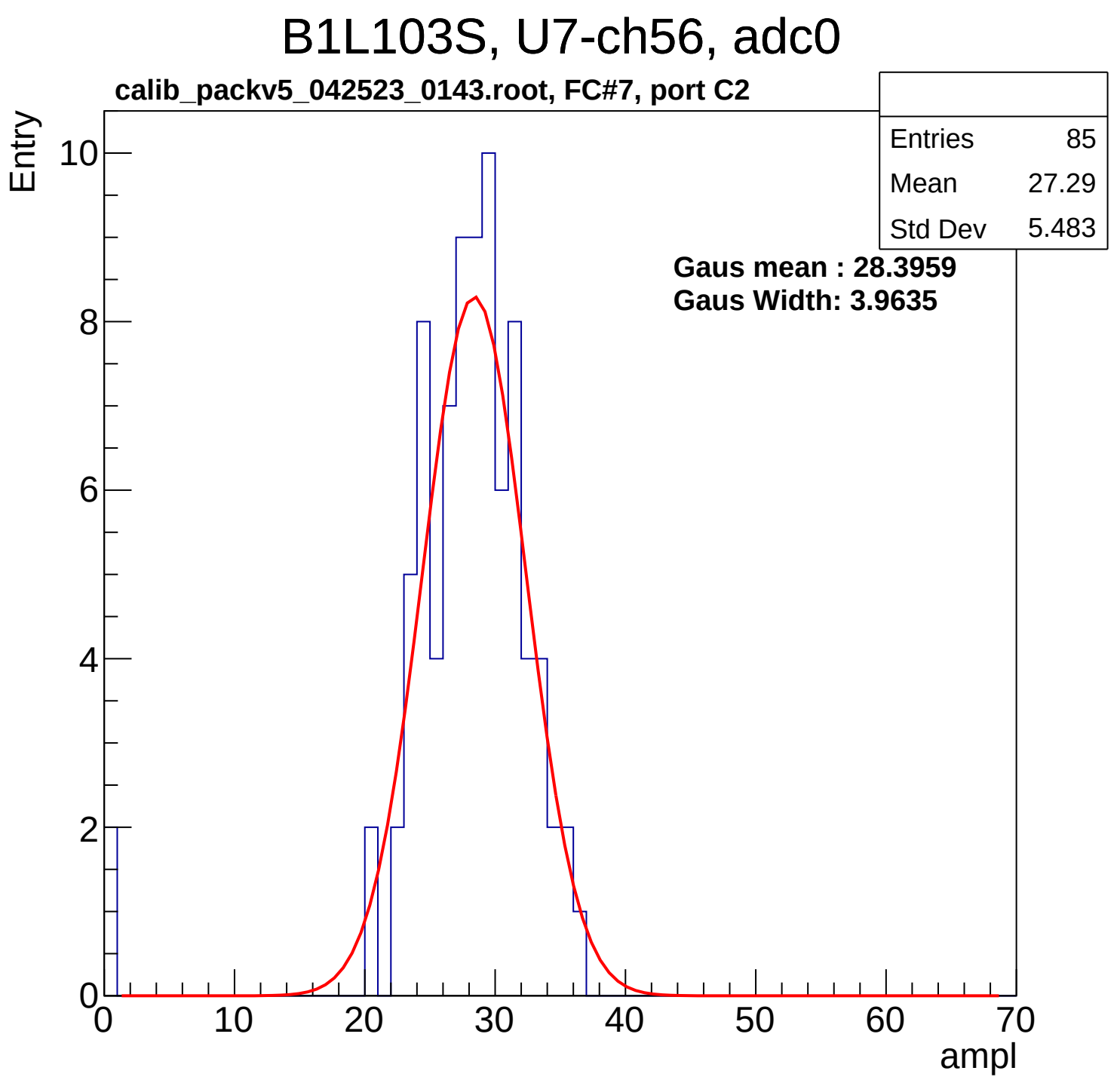
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch56, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 85
Mean 27.29
Std Dev 5.483
Gaus mean : 28.3959
Gaus Width: 3.9635
Entry
ampl
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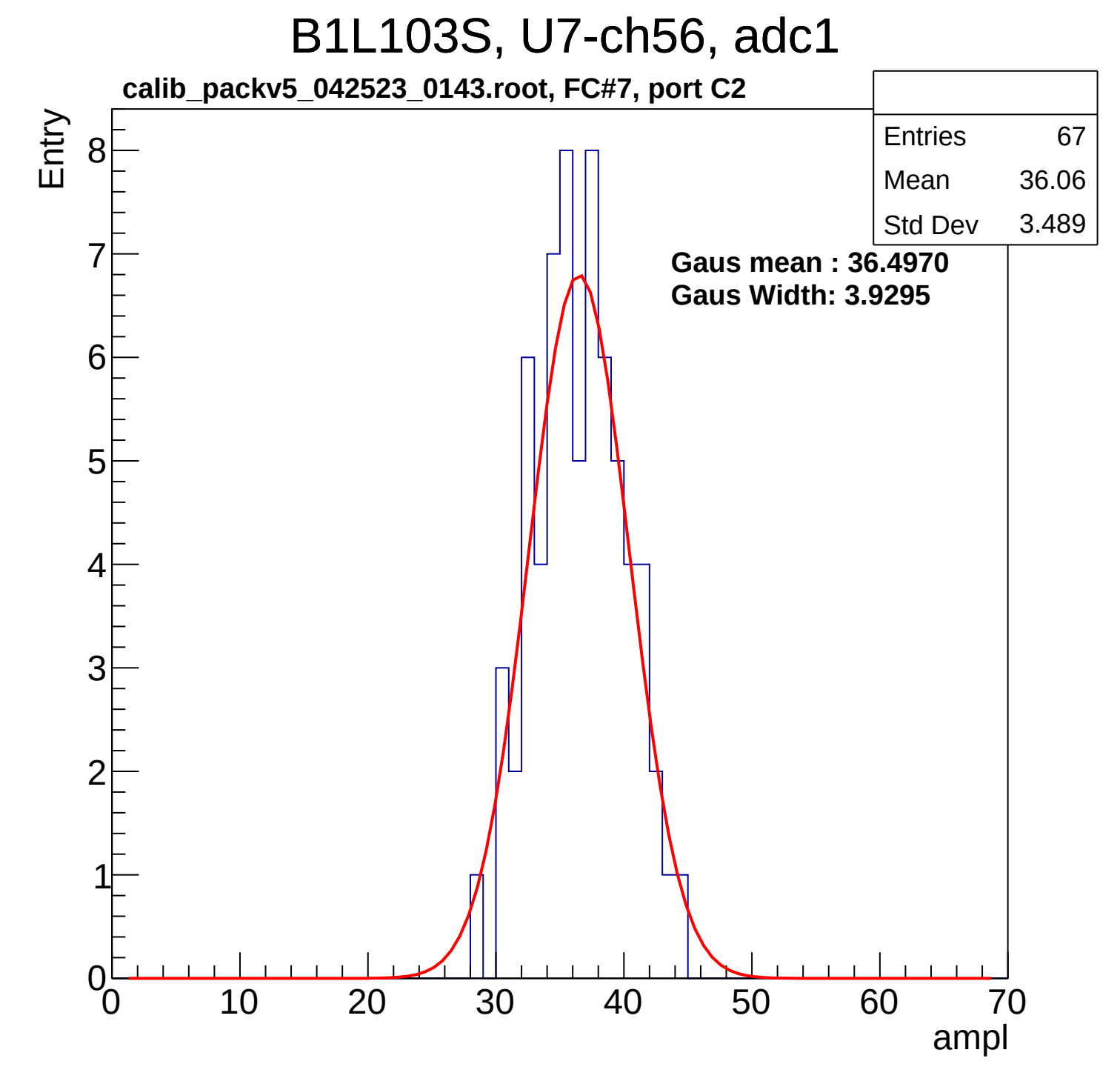
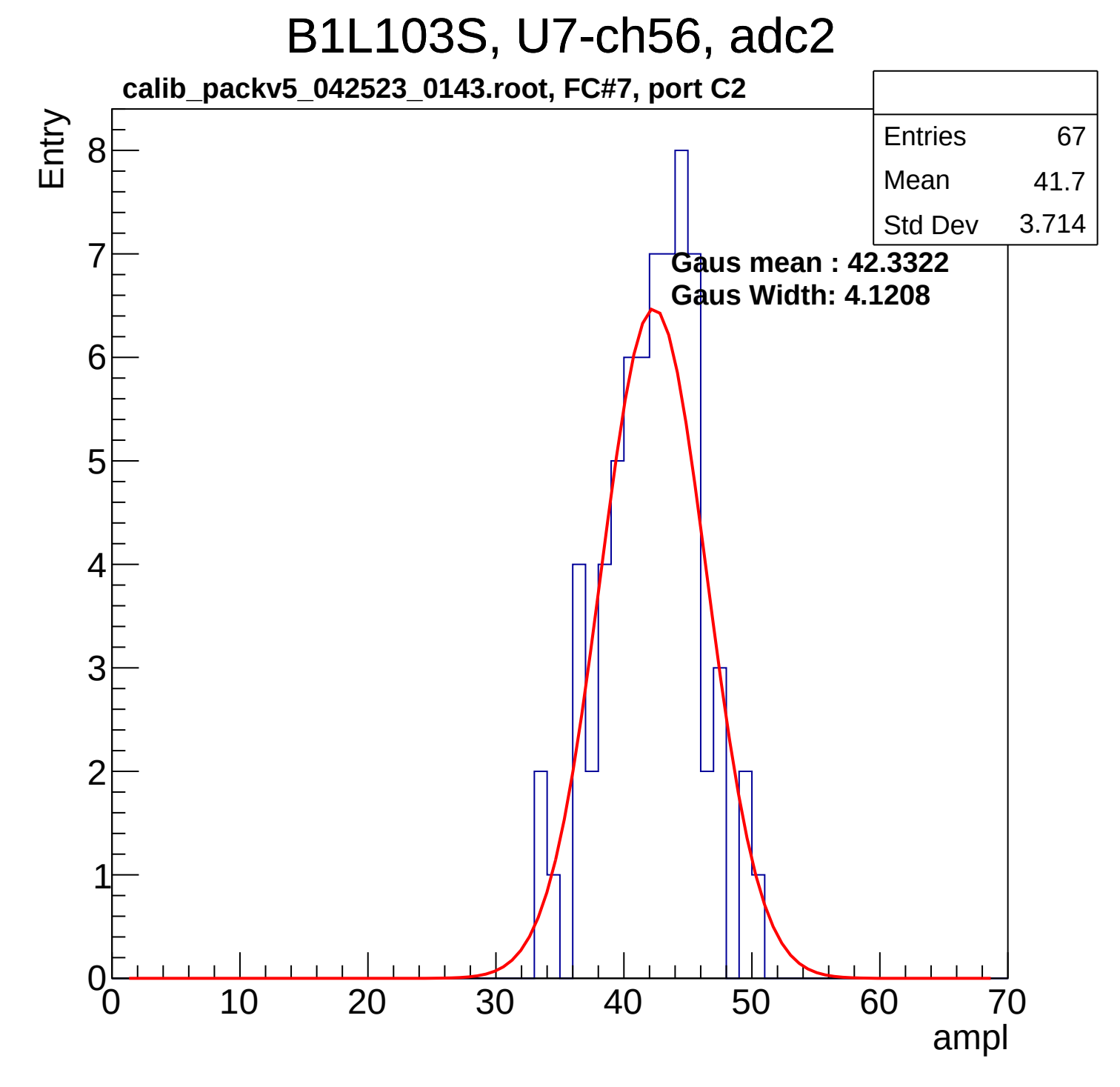
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch56, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 36.06
Std Dev 3.489
Gaus mean : 36.4970
Gaus Width: 3.9295
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch56, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 41.7
Std Dev 3.714
Gaus mean : 42.3322
Gaus Width: 4.1208
Entry
ampl
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1
2
3
4
5
6
7
8
0
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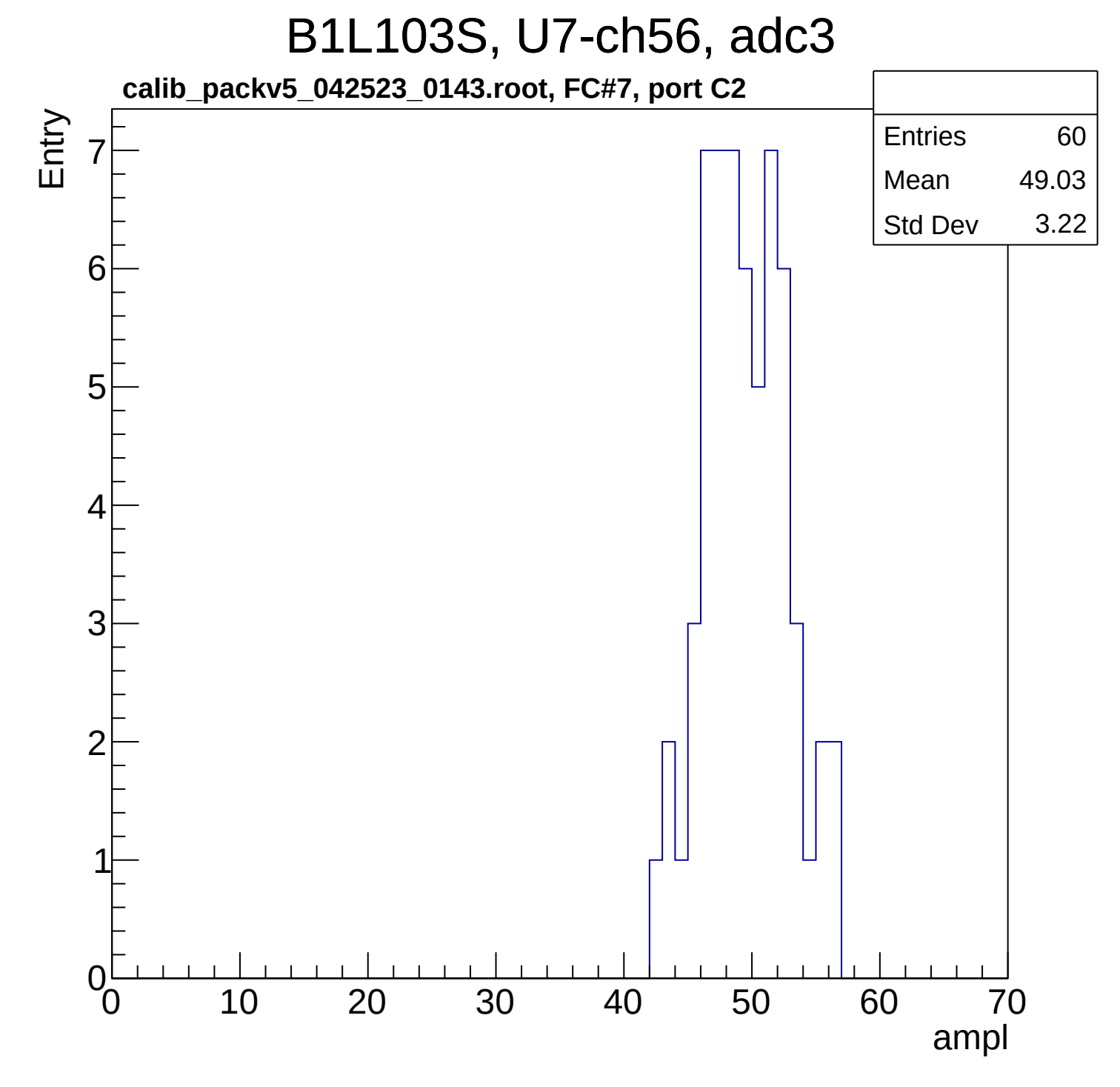
B1L103S, U7-ch56, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 60
Mean 49.03
Std Dev 3.22
Entry
ampl
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1
2
3
4
5
6
7
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10
20
30
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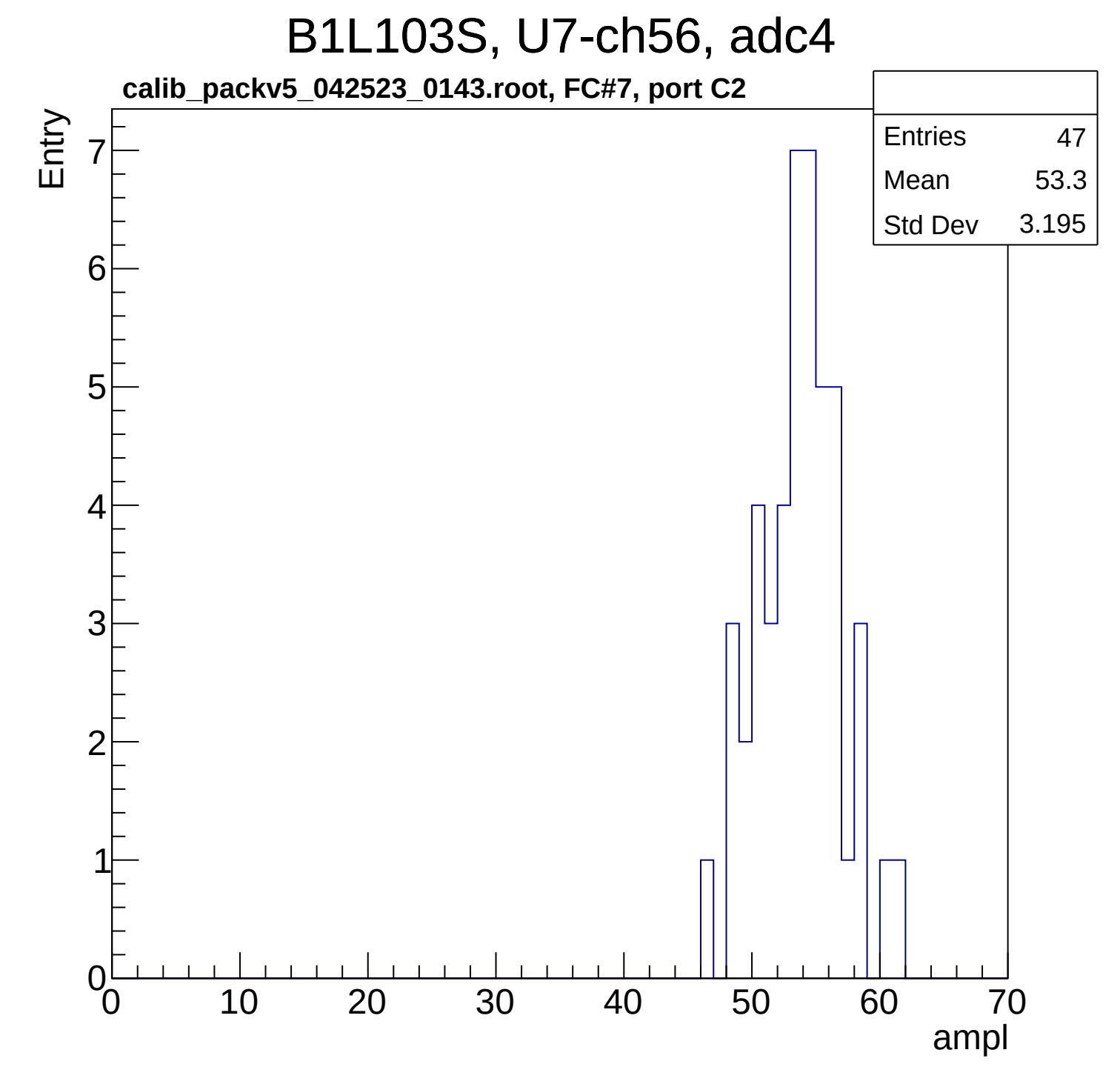
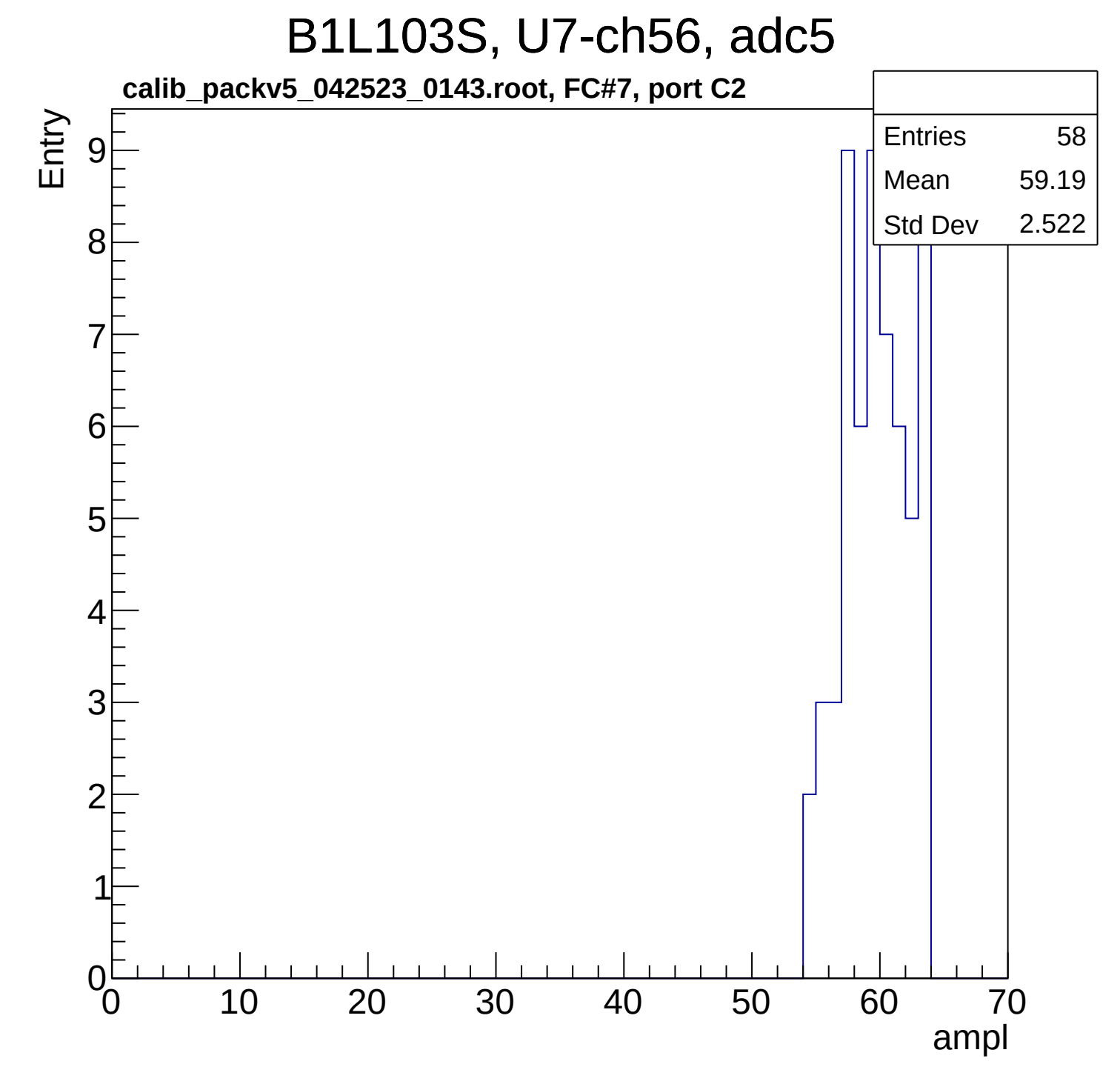

B1L103S, U7-ch56, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 47
Mean 53.3
Std Dev 3.195
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch56, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 58
Mean 59.19
Std Dev 2.522
Entry
ampl
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2
3
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6
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0
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60
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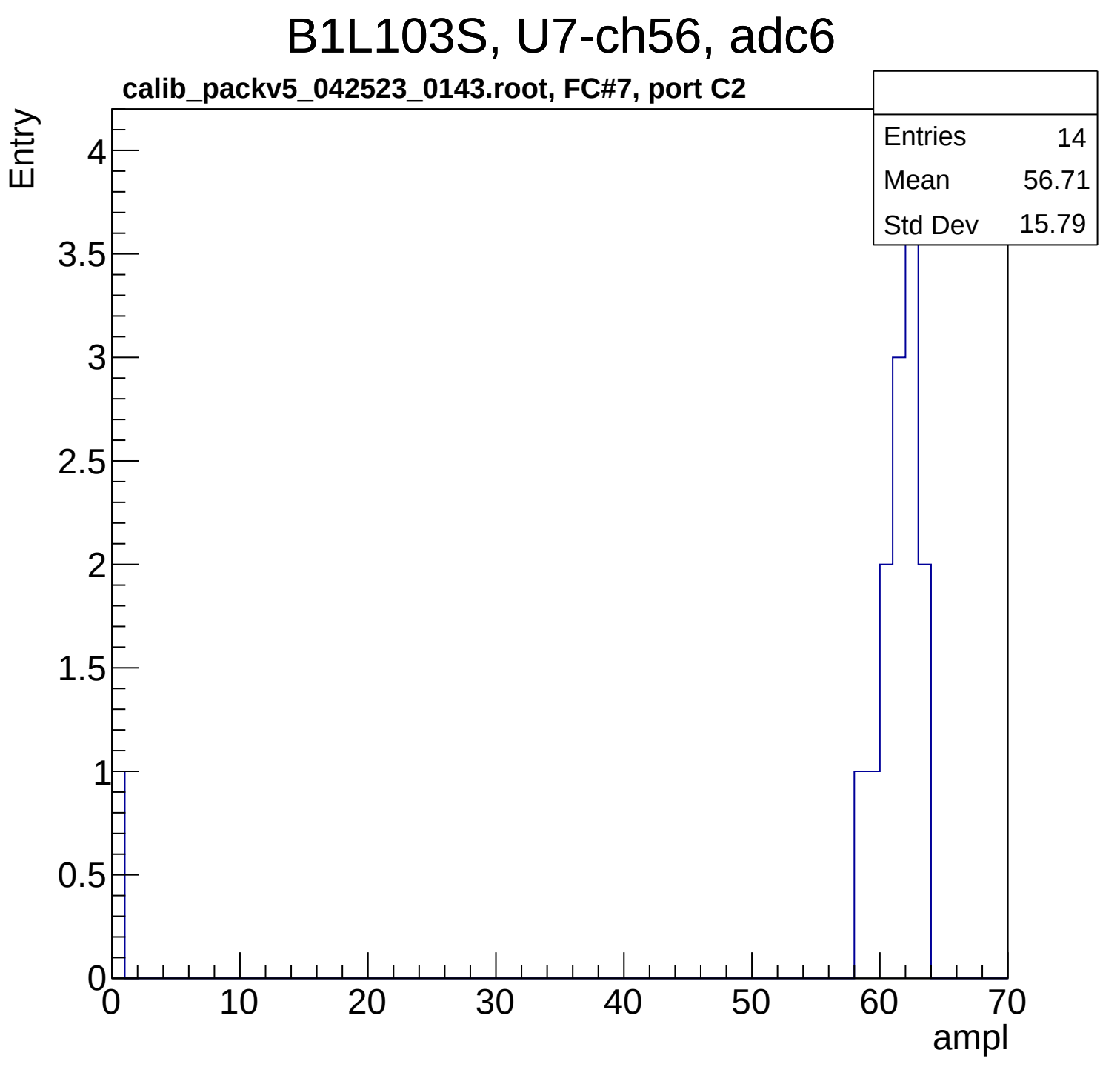
B1L103S, U7-ch56, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 14
Mean 56.71
Std Dev 15.79
Entry
ampl
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0.5
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1.5
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3.5
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0
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40
50
60
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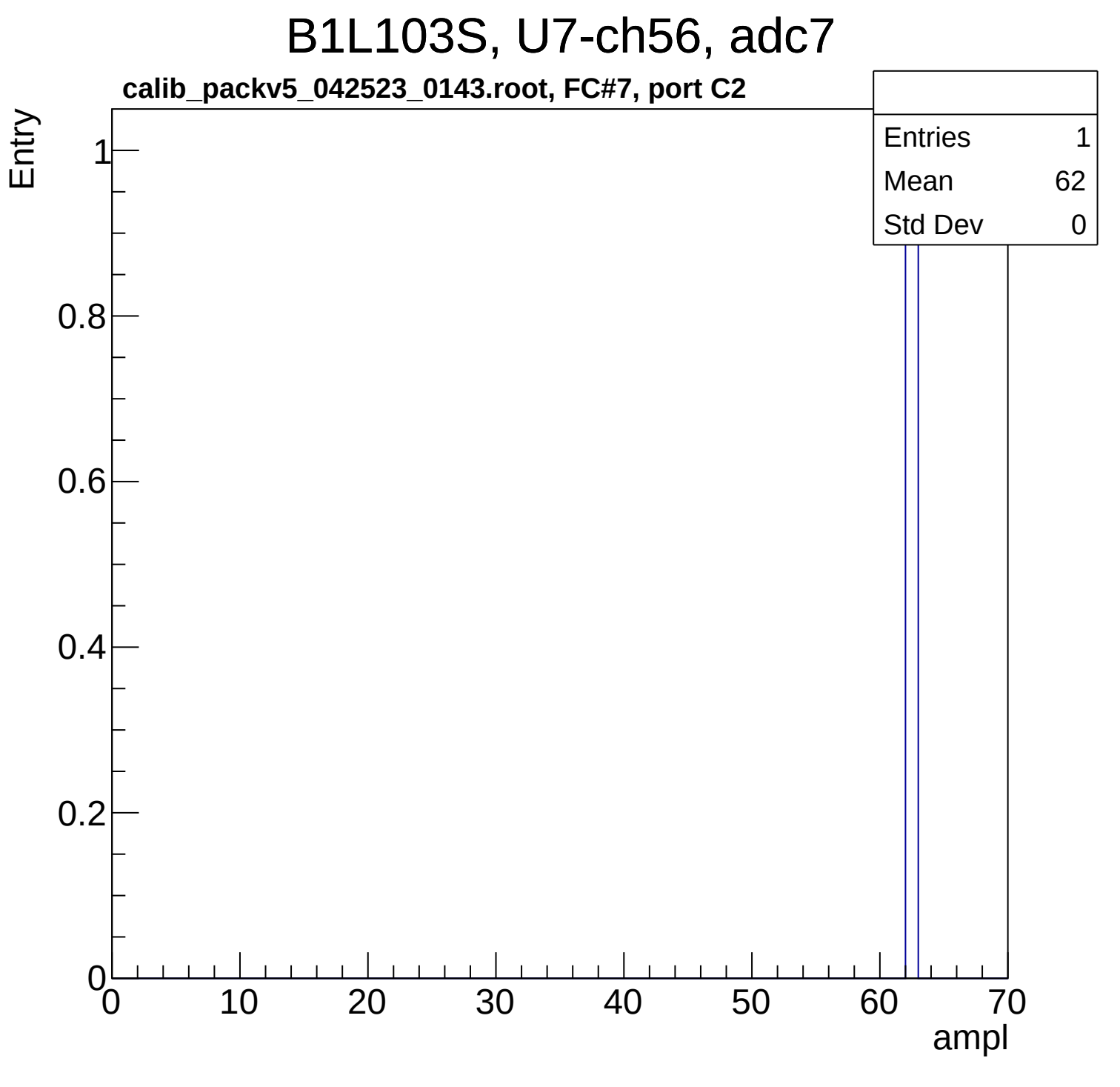
B1L103S, U7-ch56, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 62
Std Dev 0
Entry
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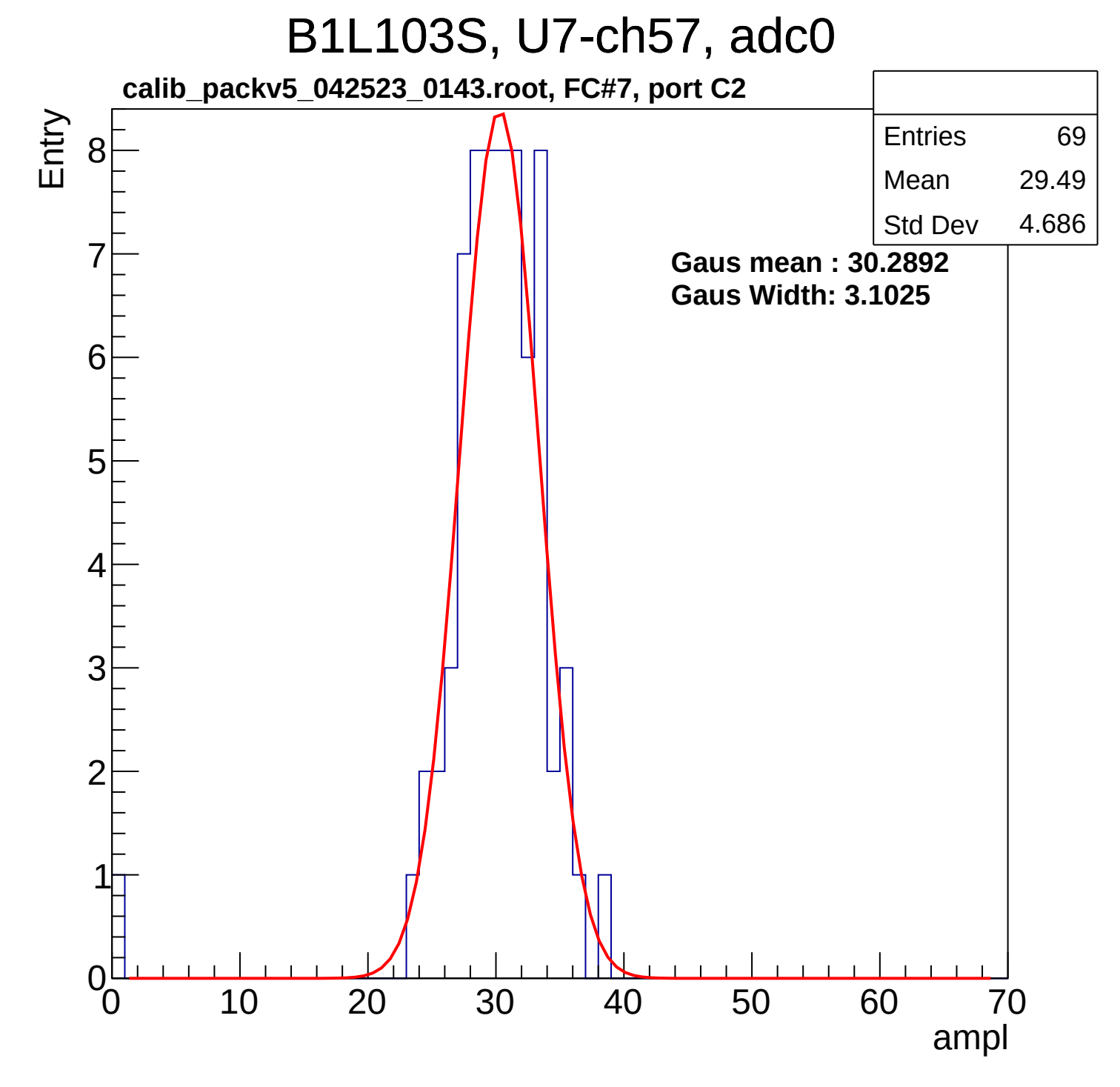
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch57, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 29.49
Std Dev 4.686
Gaus mean : 30.2892
Gaus Width: 3.1025
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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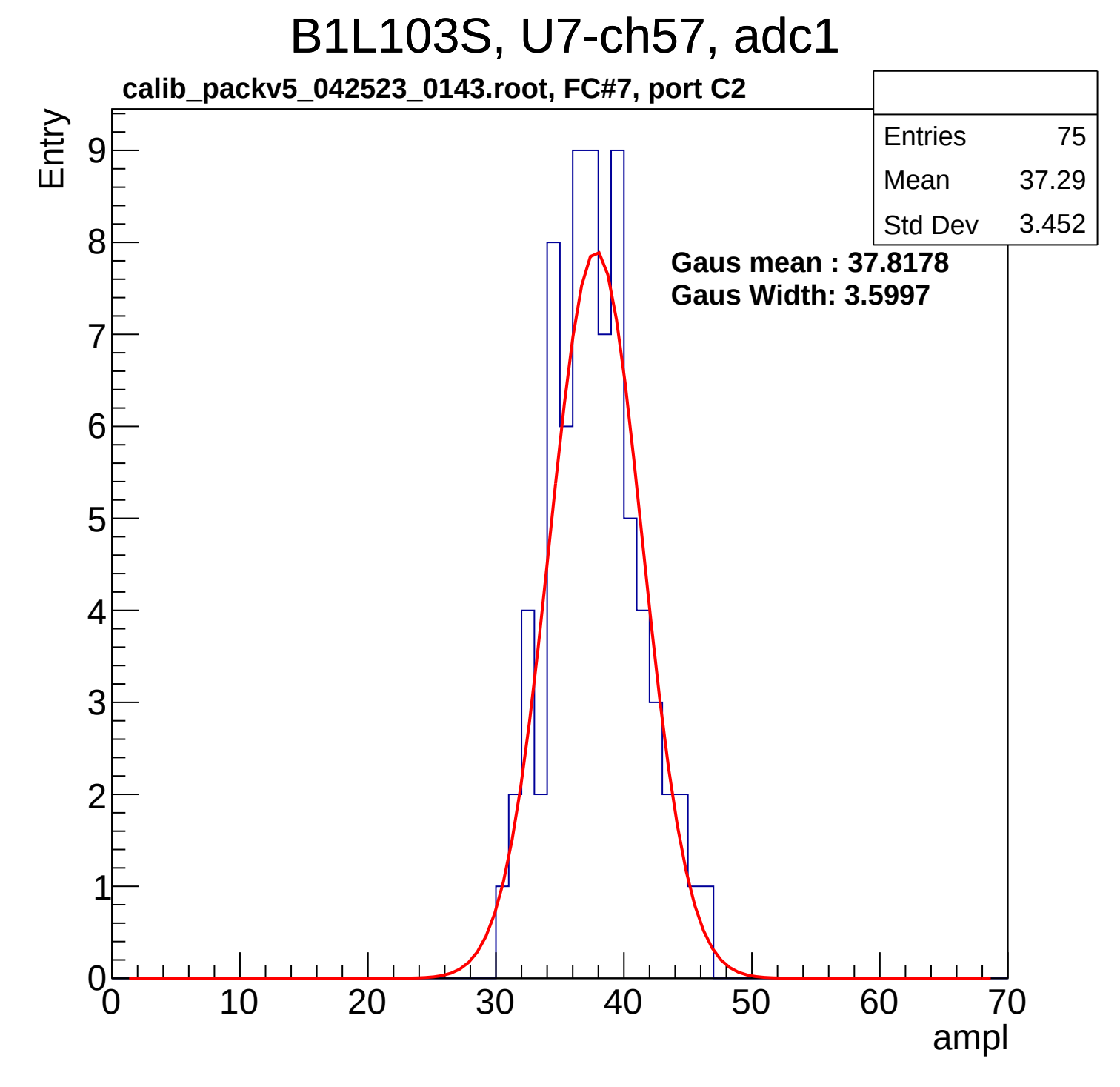
B1L103S, U7-ch57, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 75
Mean 37.29
Std Dev 3.452
Gaus mean : 37.8178
Gaus Width: 3.5997
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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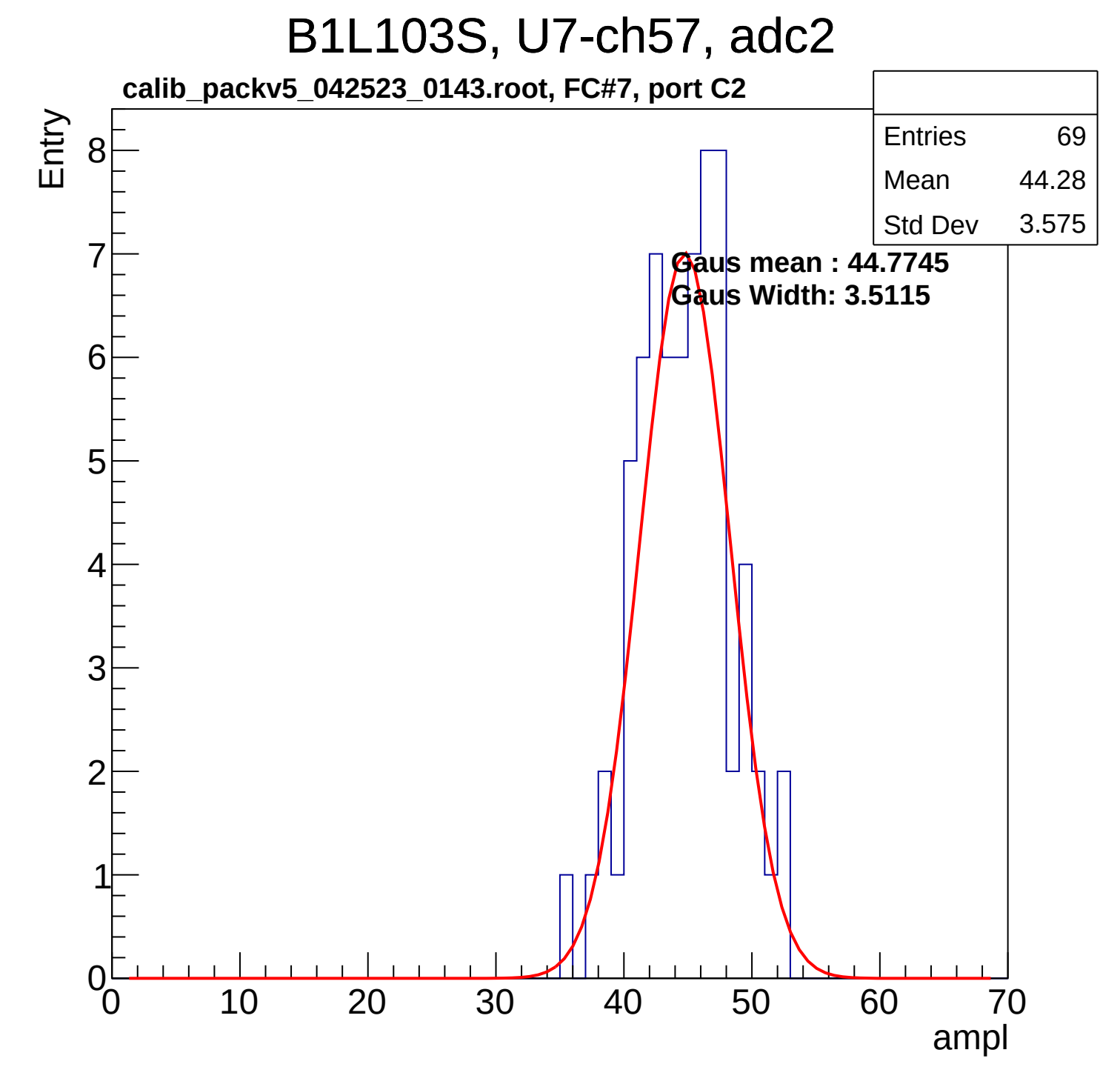
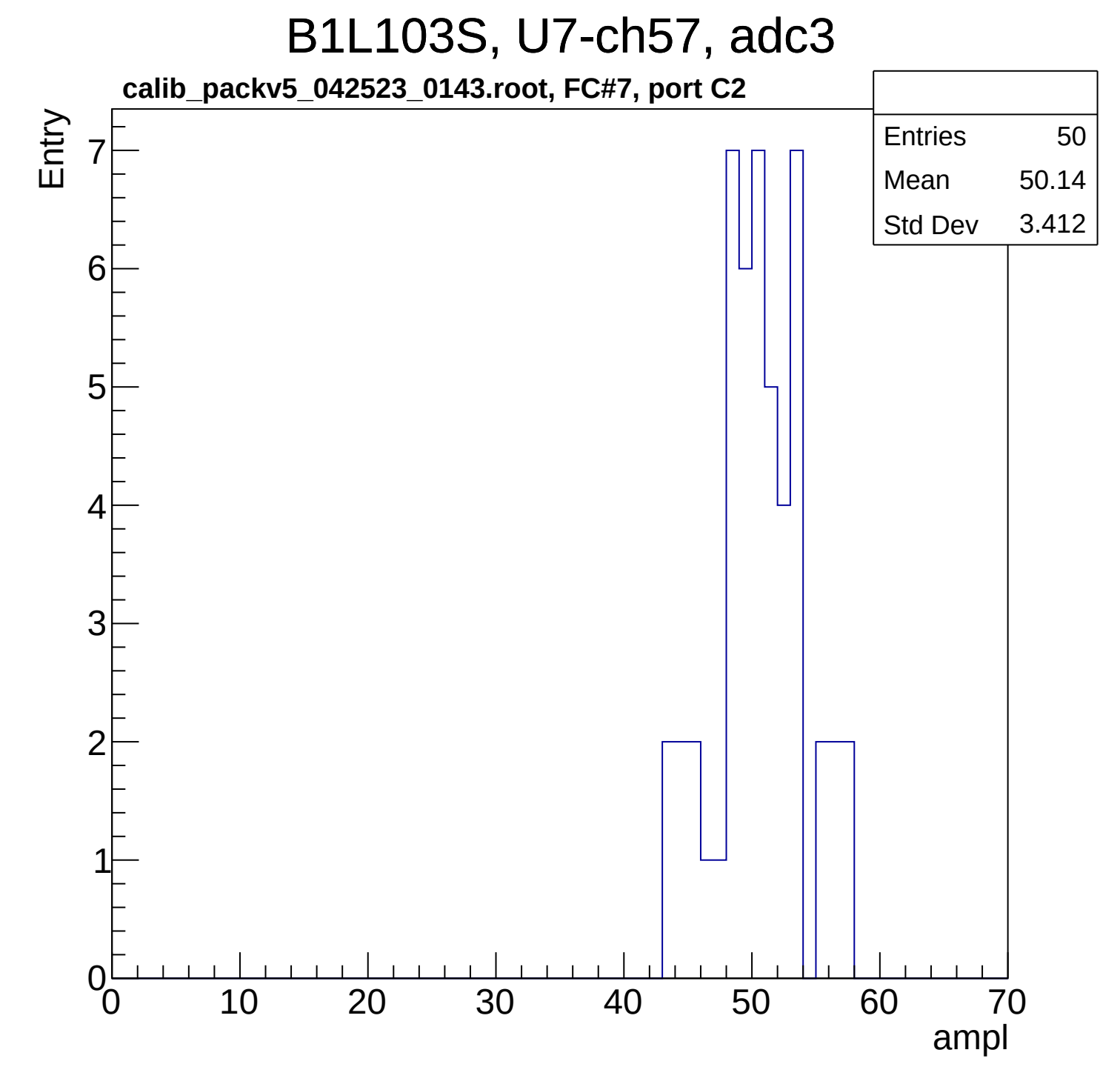
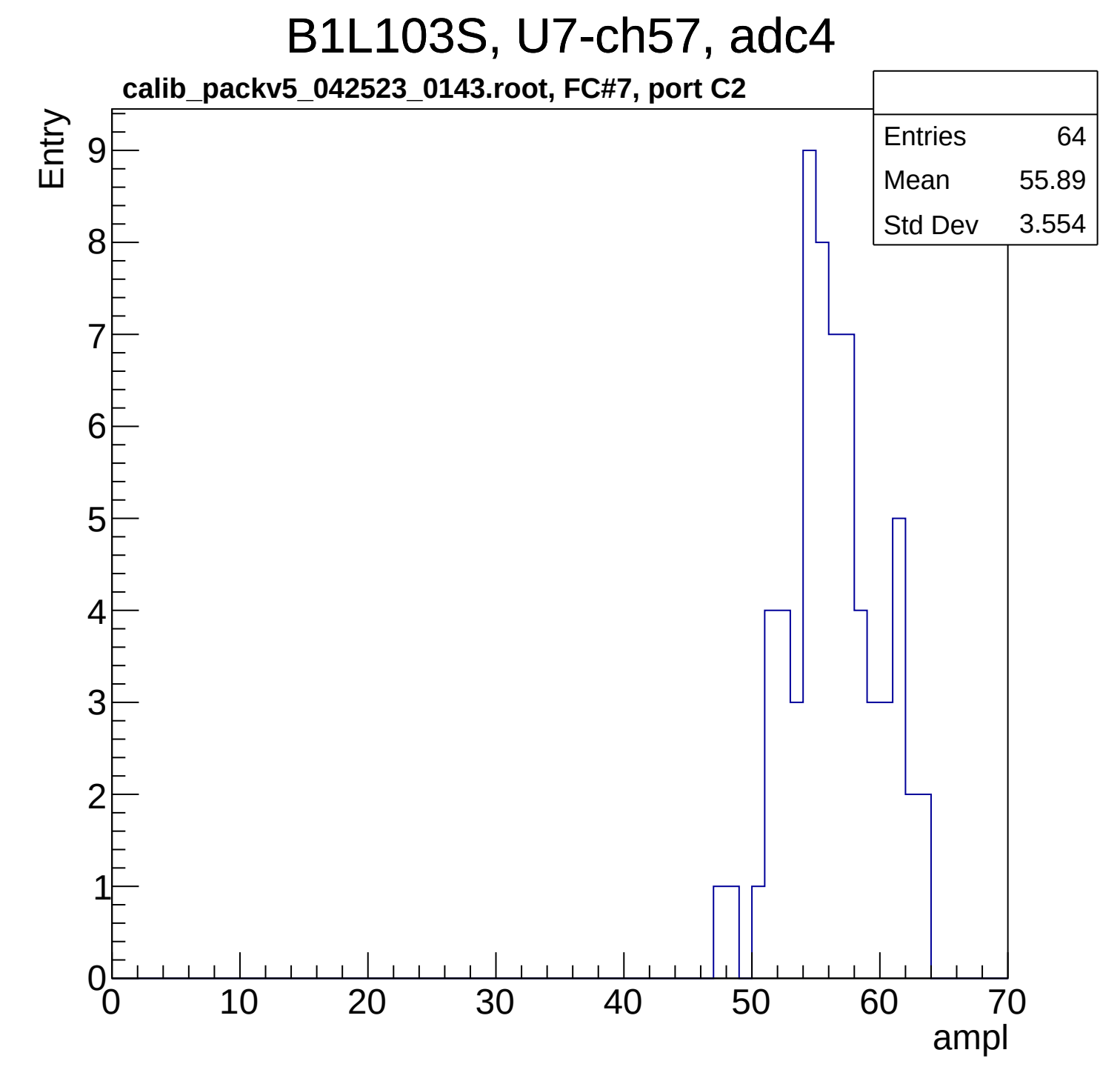

B1L103S, U7-ch57, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 44.28
Std Dev 3.575
Gaus mean : 44.7745
Gaus Width: 3.5115
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch57, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 50
Mean 50.14
Std Dev 3.412
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch57, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 55.89
Std Dev 3.554
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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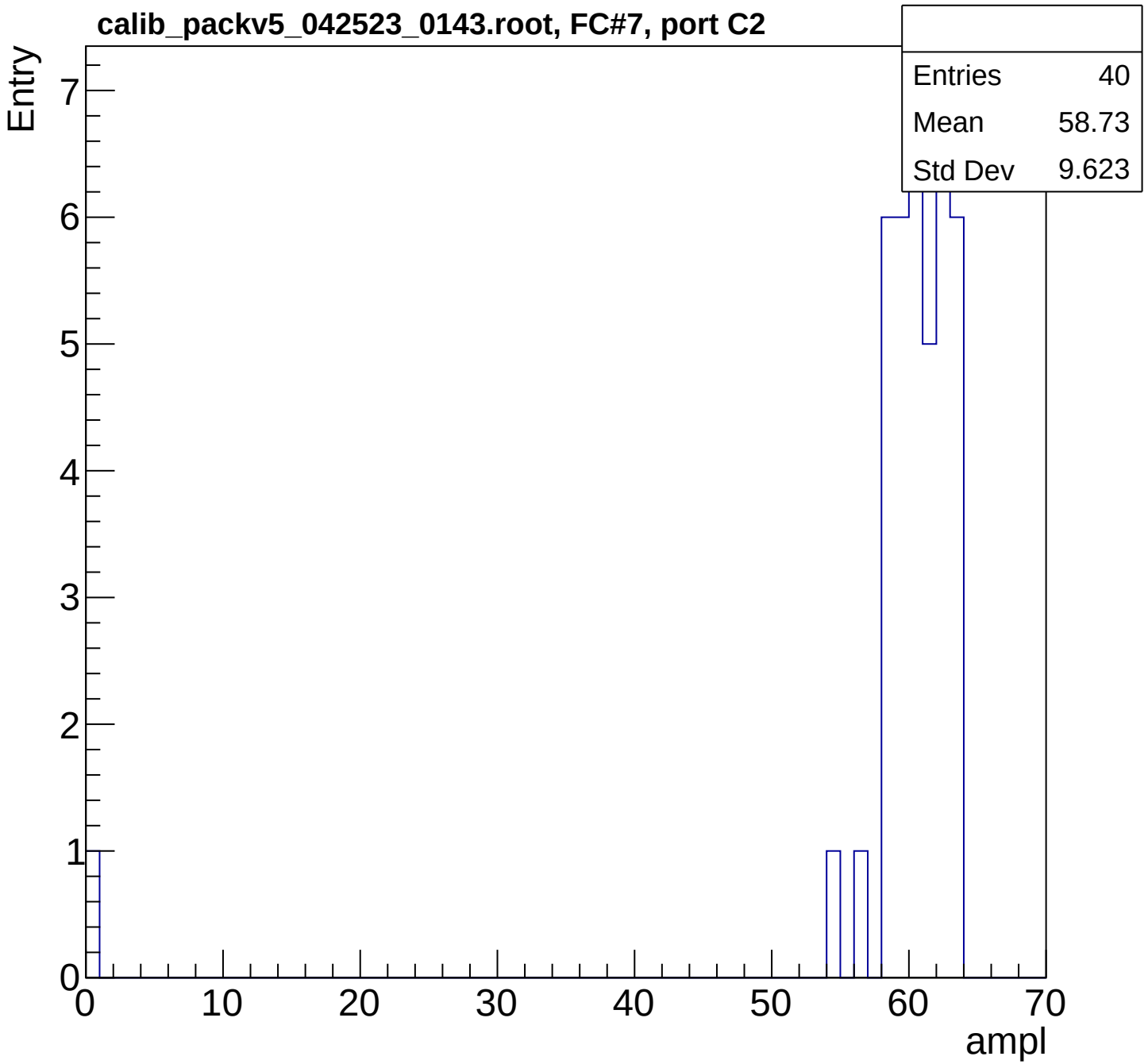
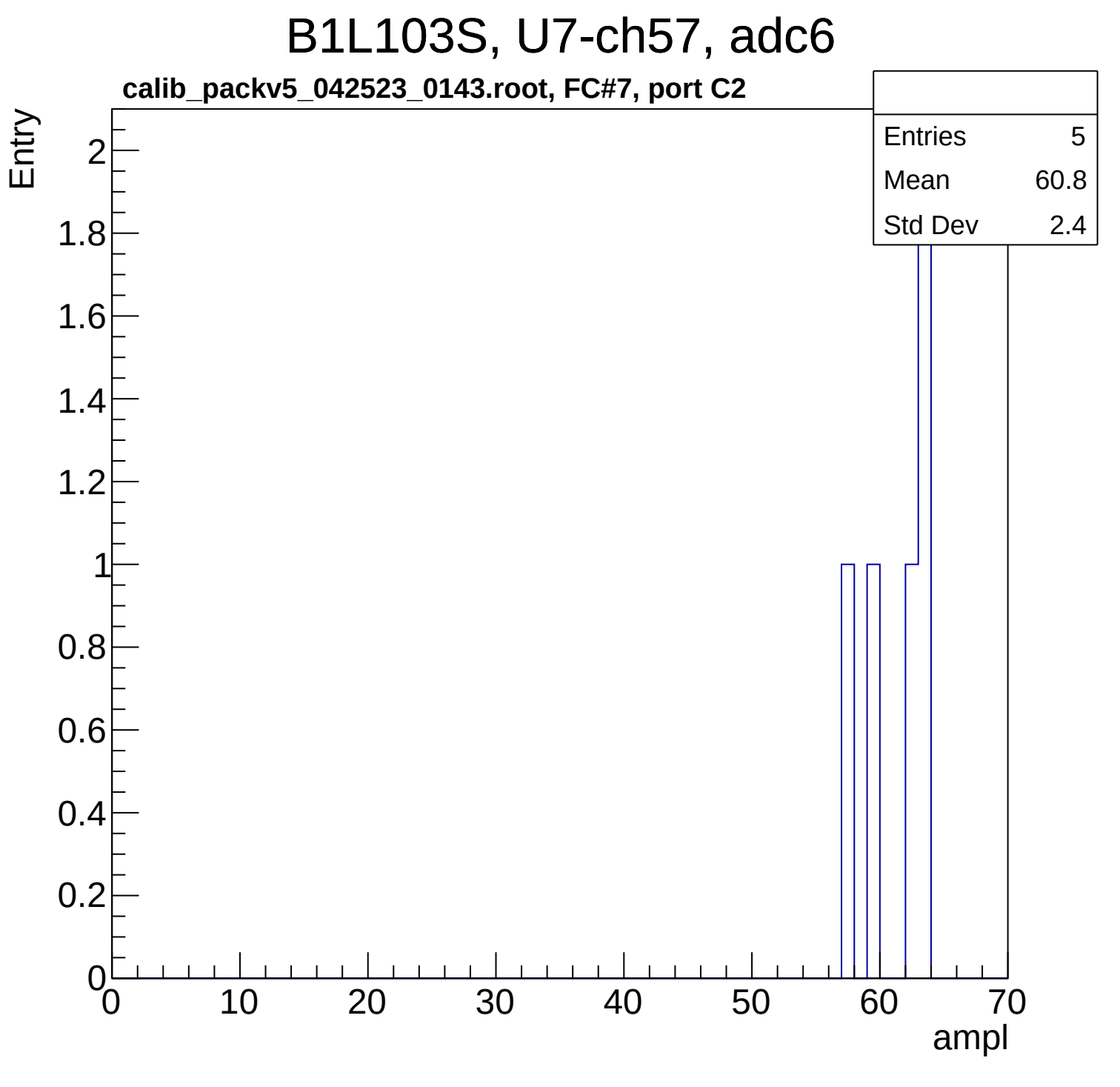
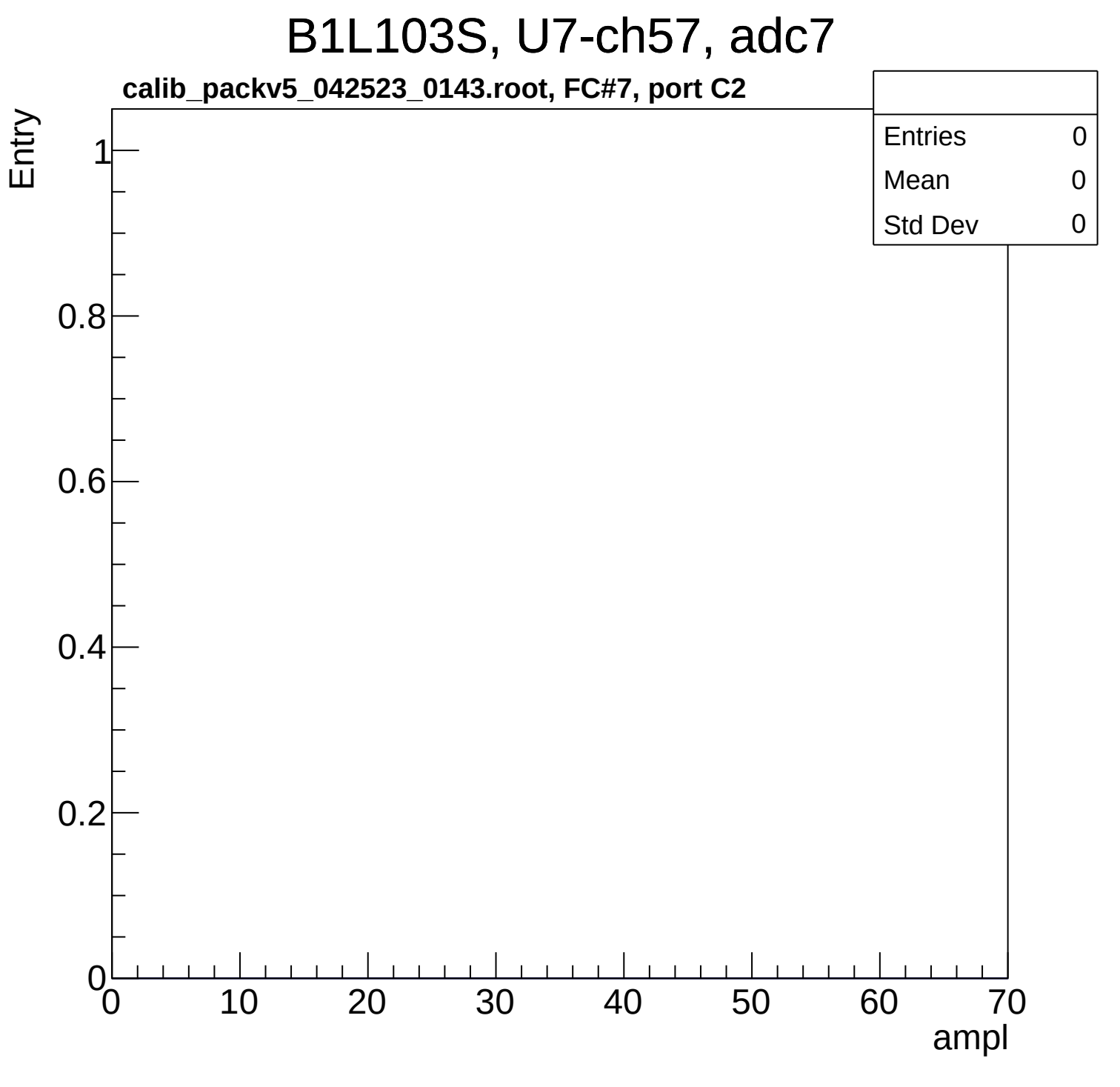
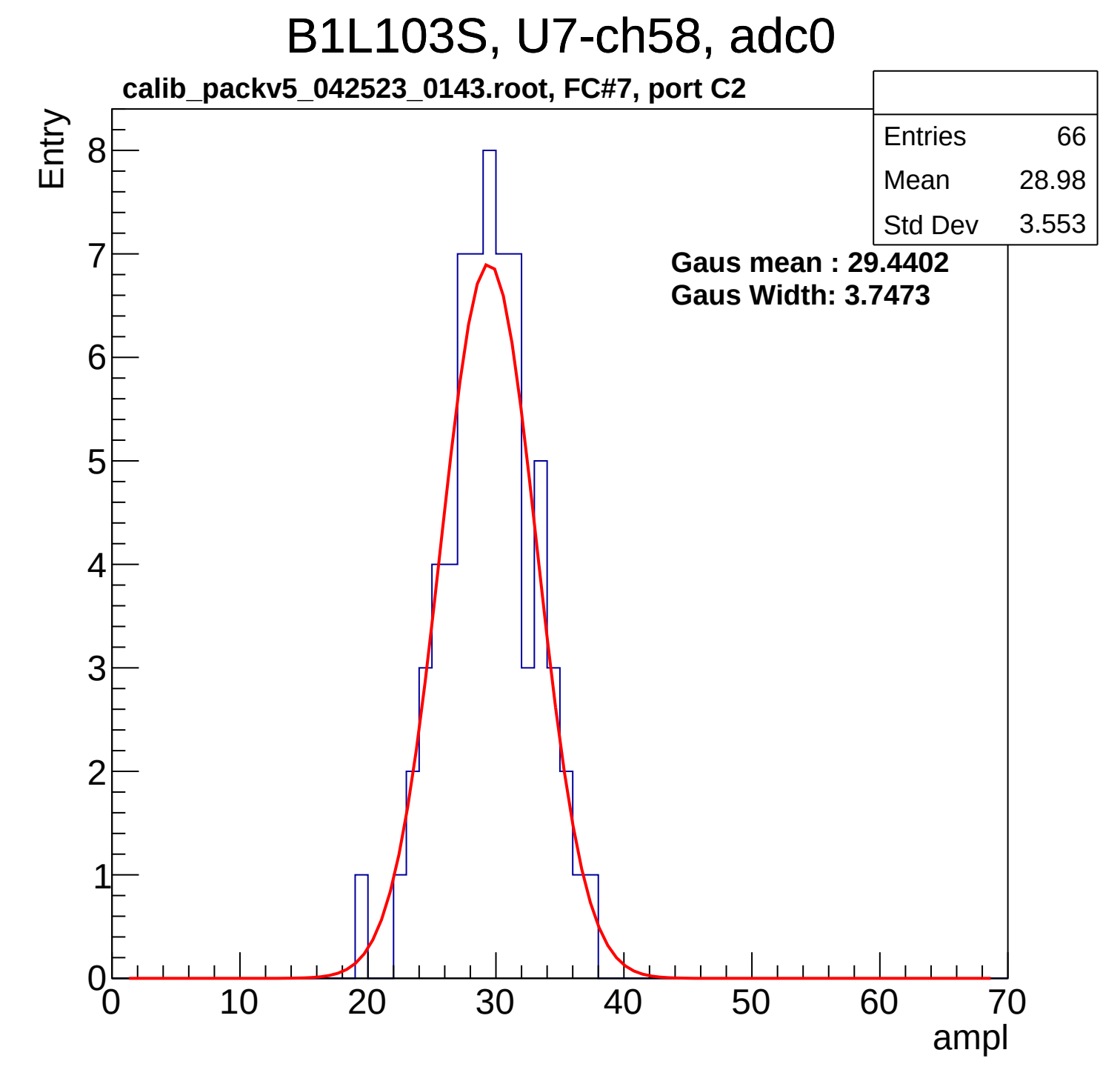
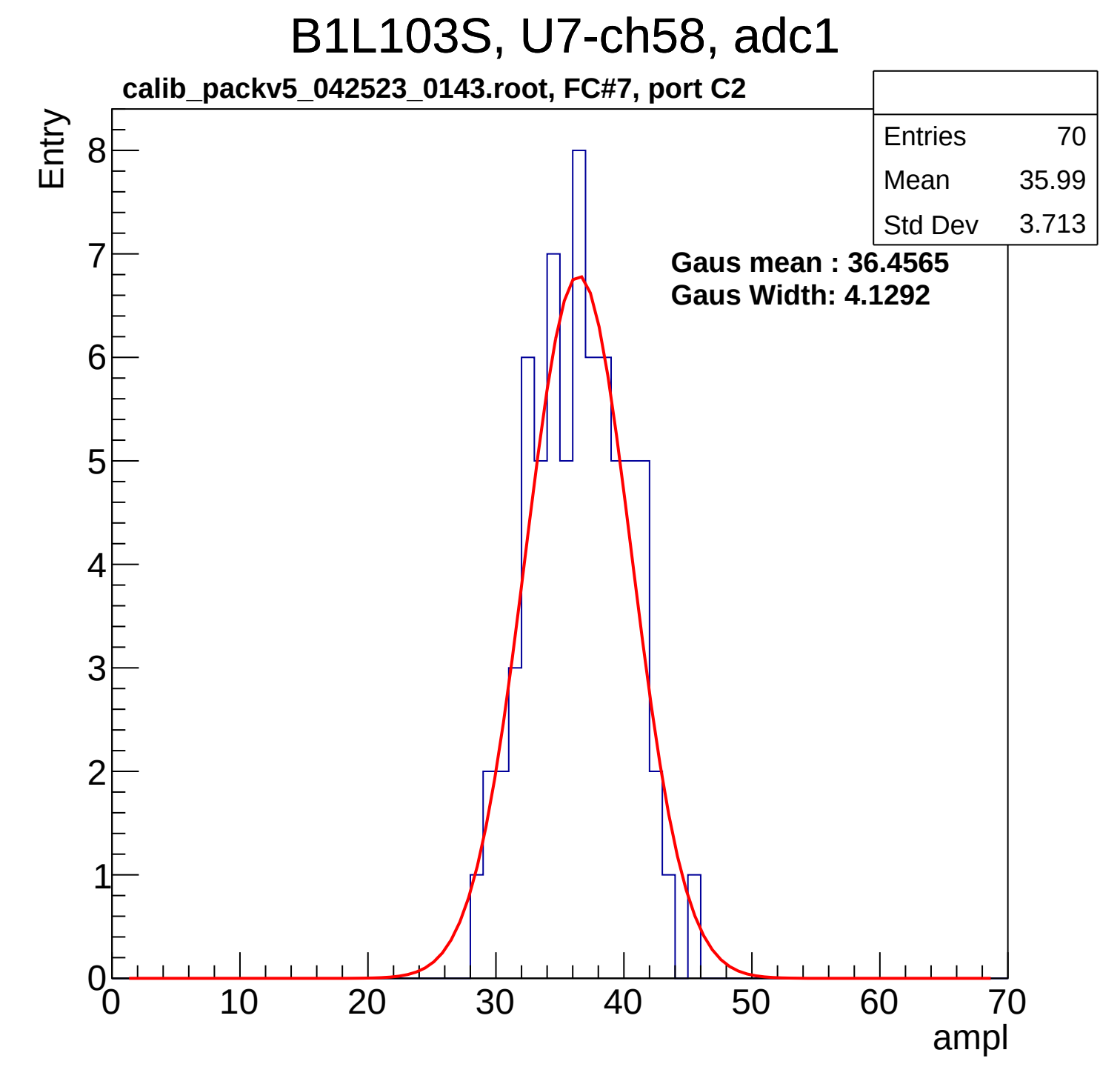
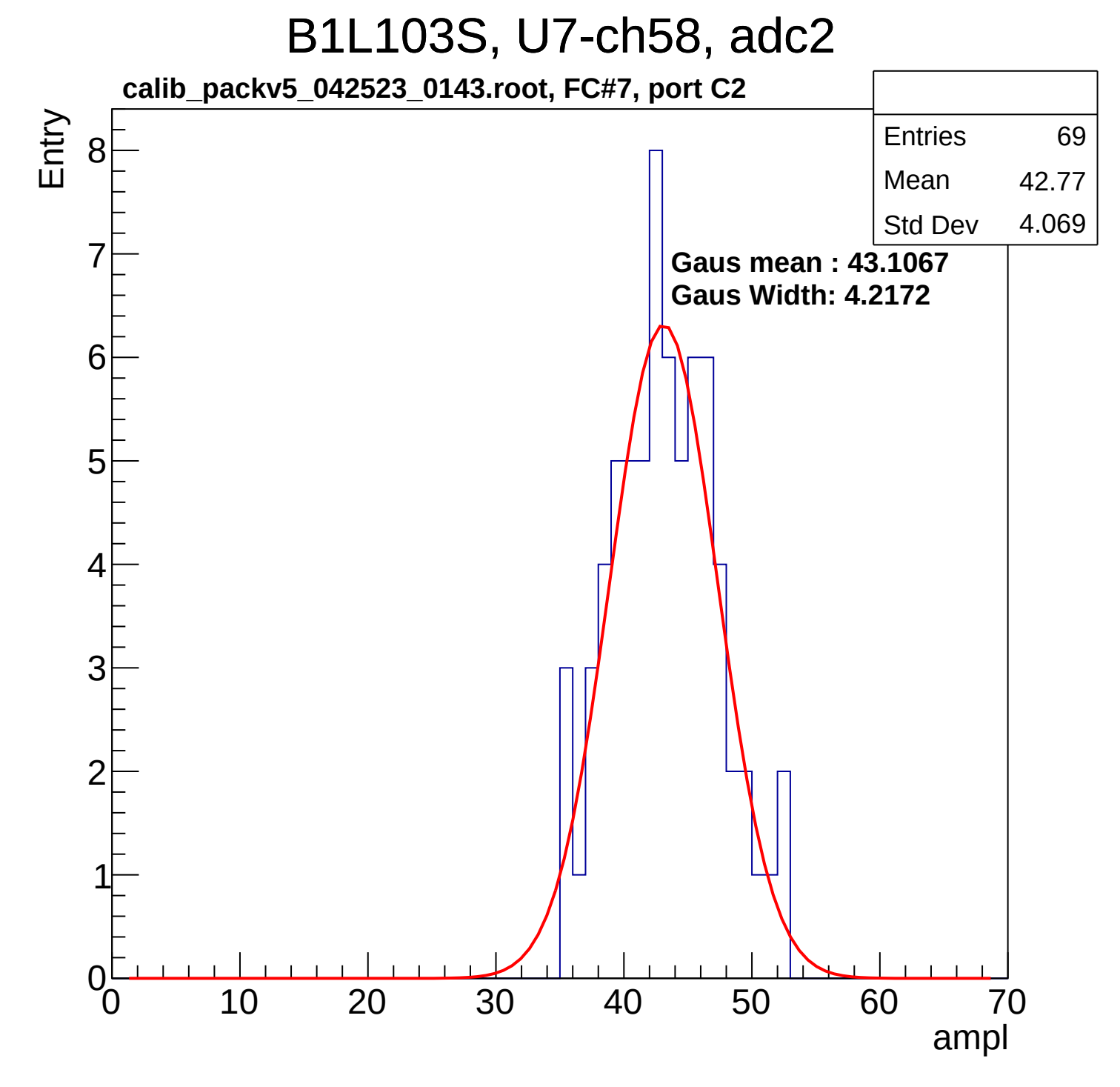

B1L103S, U7-ch57, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 40
Mean 58.73
Std Dev 9.623
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch57, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 5
Mean 60.8
Std Dev 2.4
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U7-ch57, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch58, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 28.98
Std Dev 3.553
Gaus mean : 29.4402
Gaus Width: 3.7473
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch58, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 35.99
Std Dev 3.713
Gaus mean : 36.4565
Gaus Width: 4.1292
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch58, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 42.77
Std Dev 4.069
Gaus mean : 43.1067
Gaus Width: 4.2172
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
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40
50
60
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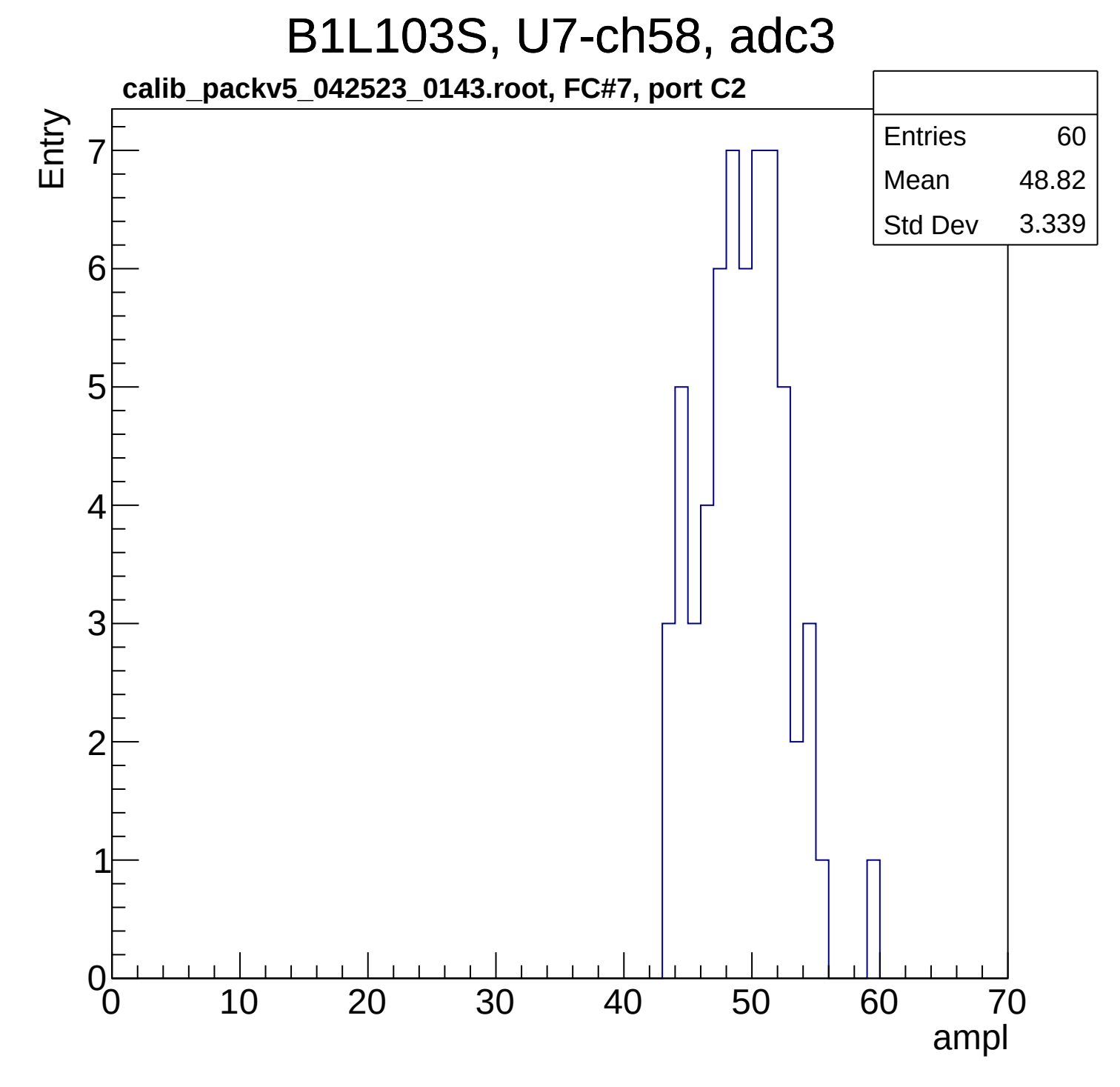
B1L103S, U7-ch58, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 60
Mean 48.82
Std Dev 3.339
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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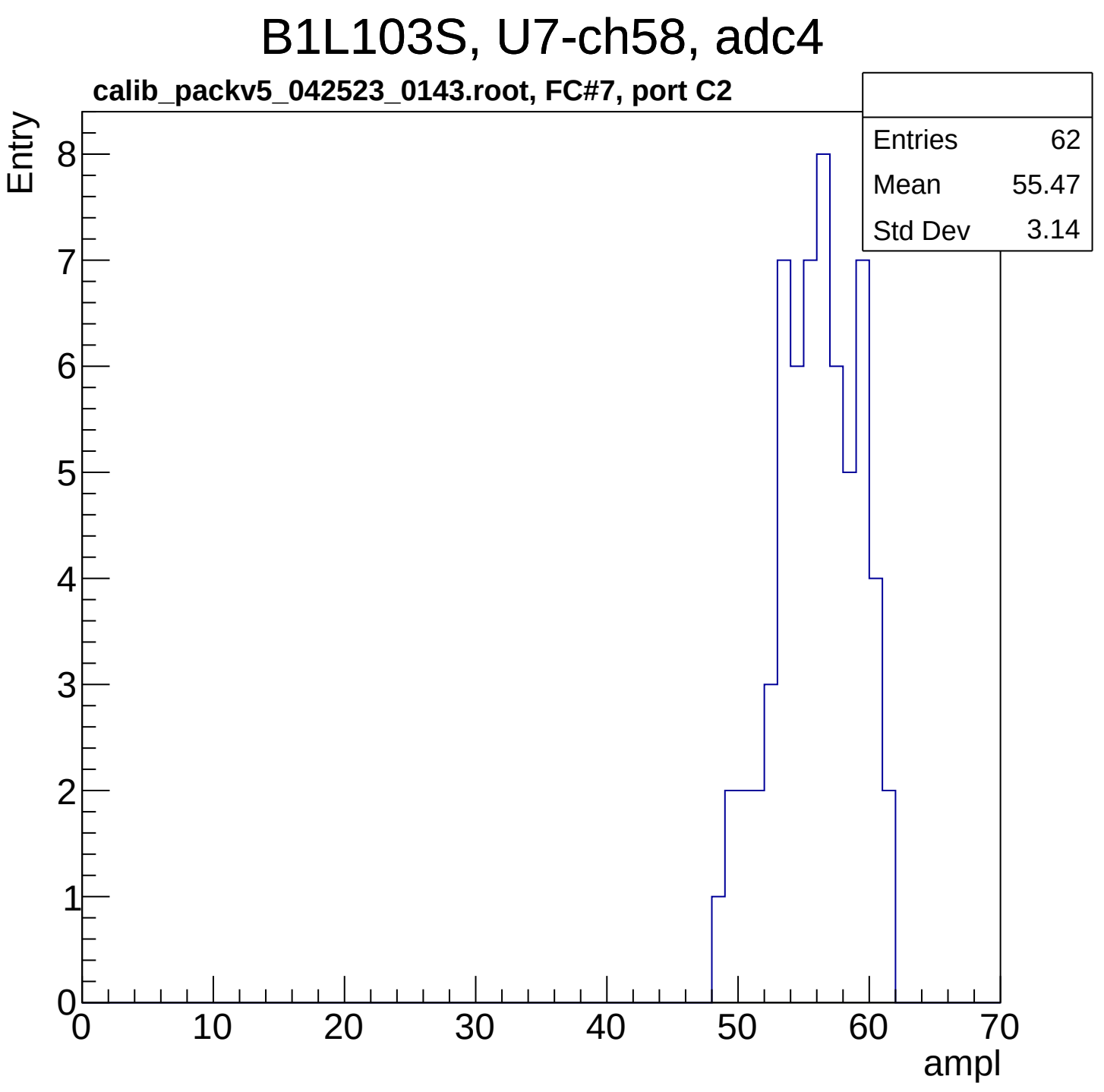
B1L103S, U7-ch58, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 62
Mean 55.47
Std Dev 3.14
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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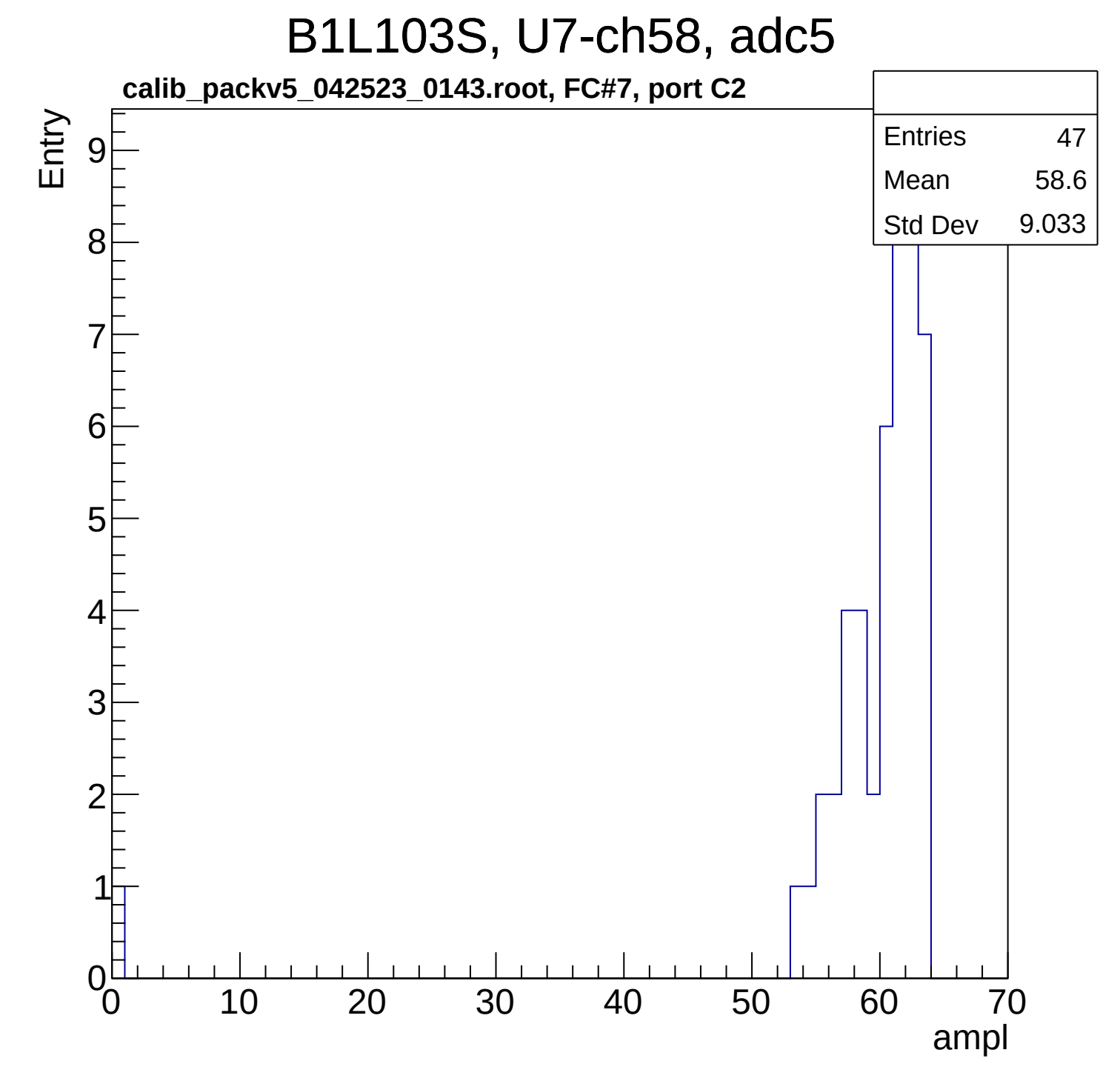
40
50
60
70


B1L103S, U7-ch58, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 47
Mean 58.6
Std Dev 9.033
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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20
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40
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60
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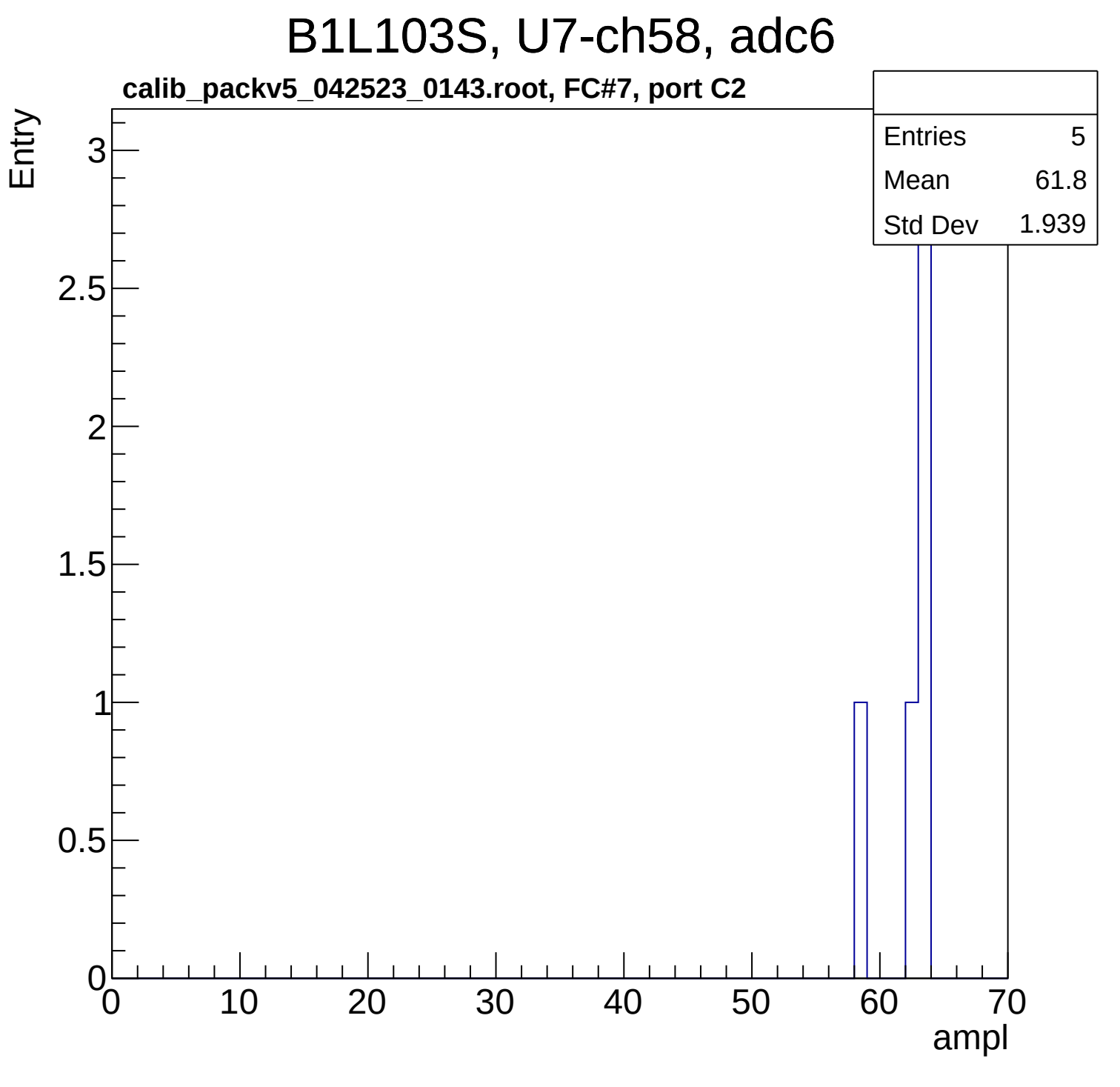
B1L103S, U7-ch58, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 5
Mean 61.8
Std Dev 1.939
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
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20
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40
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60
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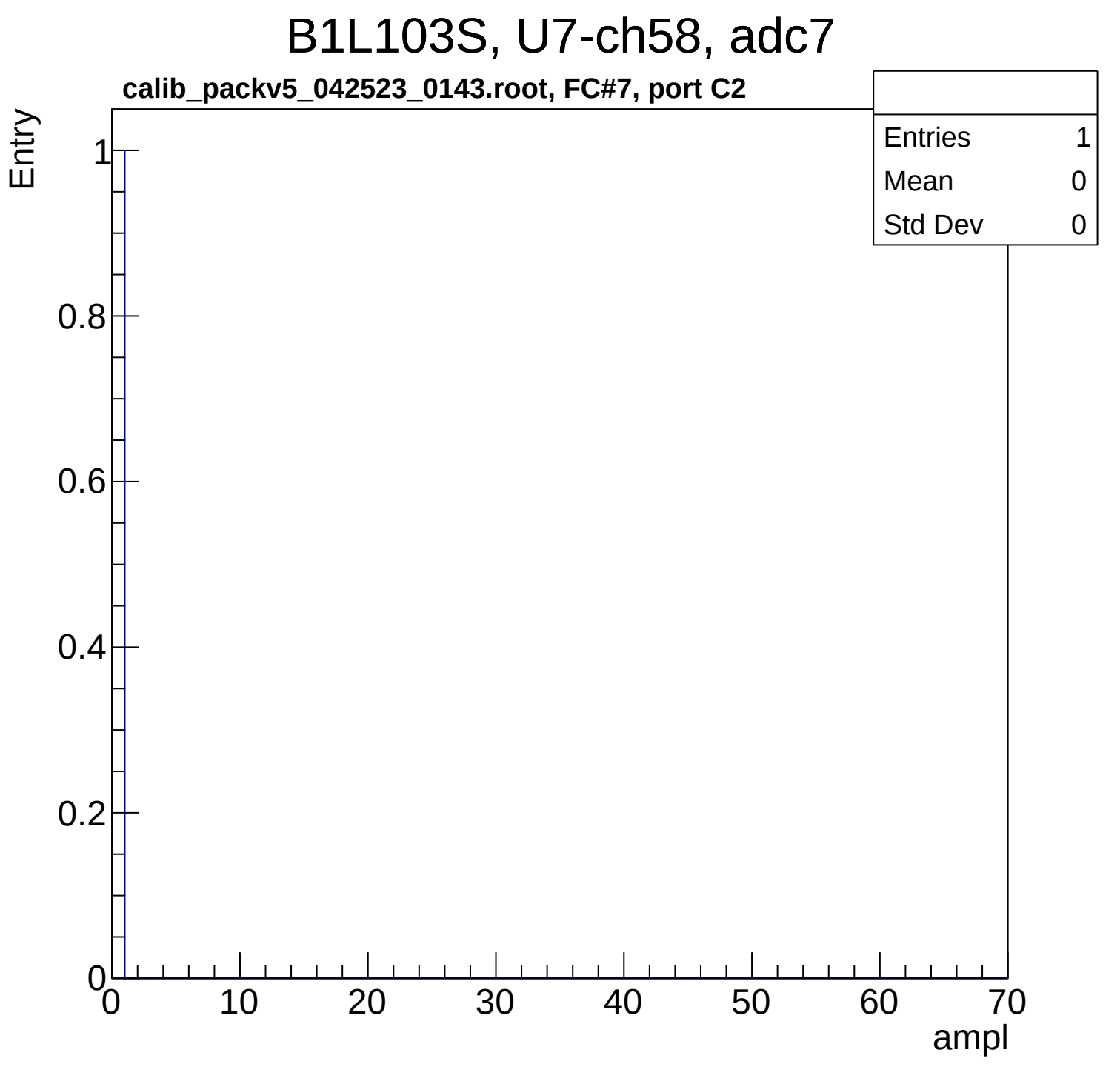
B1L103S, U7-ch58, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
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0.6
0.4
0.2
0
0
10
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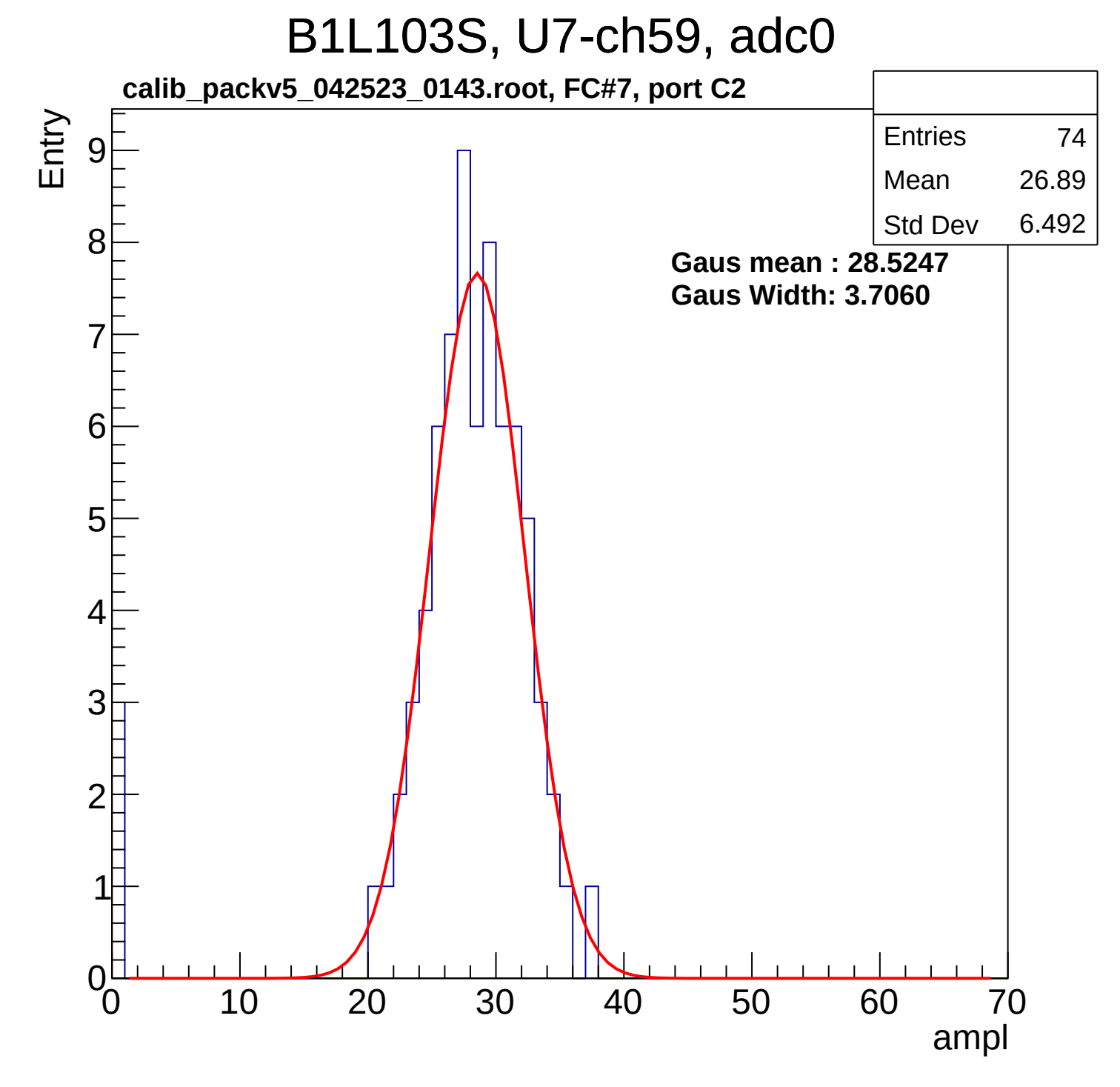
40
50
60
70
ampl


B1L103S, U7-ch59, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 74
Mean 26.89
Std Dev 6.492
Gaus mean : 28.5247
Gaus Width: 3.7060
Entry
ampl
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2
3
4
5
6
7
8
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0
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40
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60
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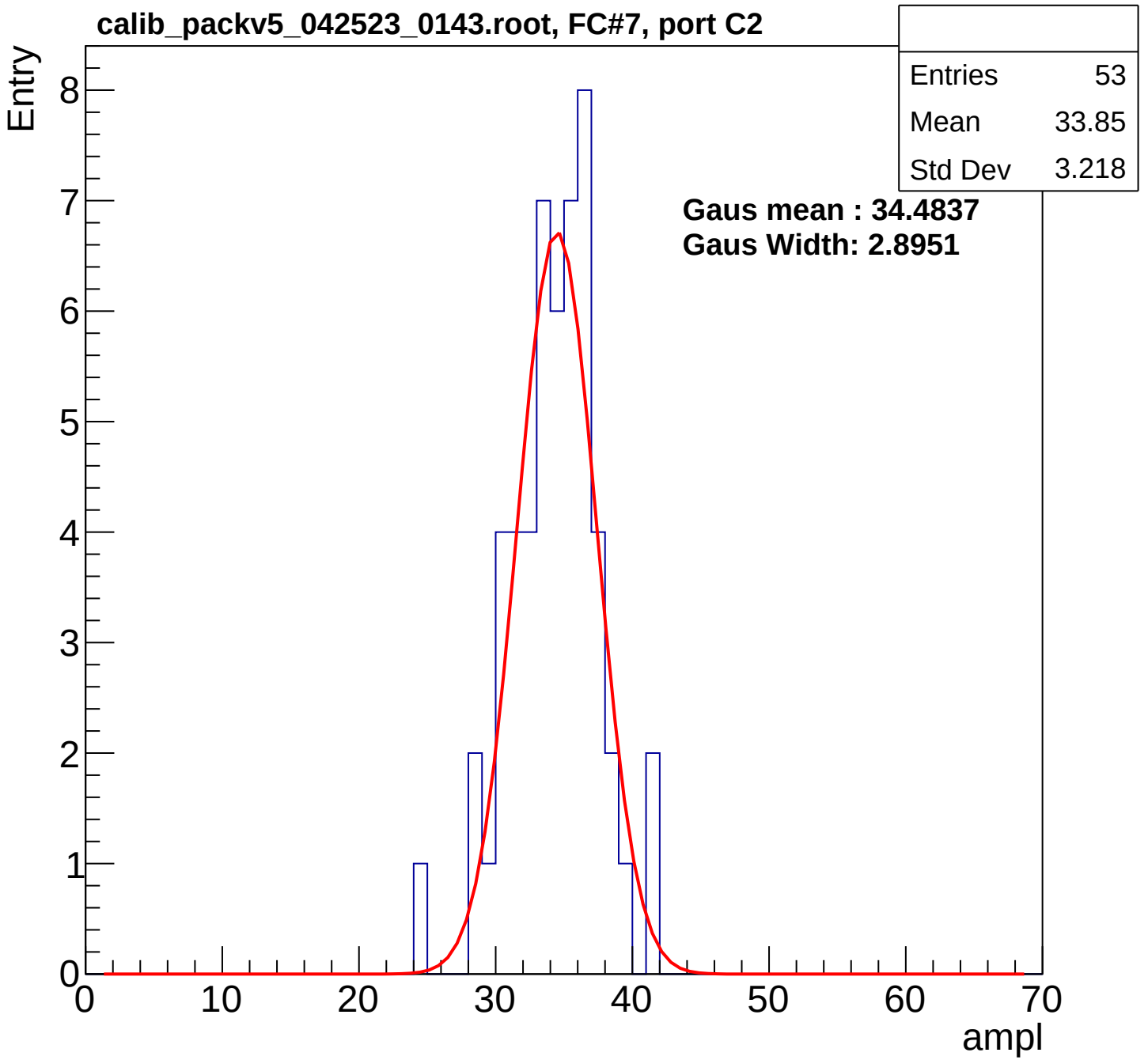
B1L103S, U7-ch59, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 33.85
Std Dev 3.218
Gaus mean : 34.4837
Gaus Width: 2.8951
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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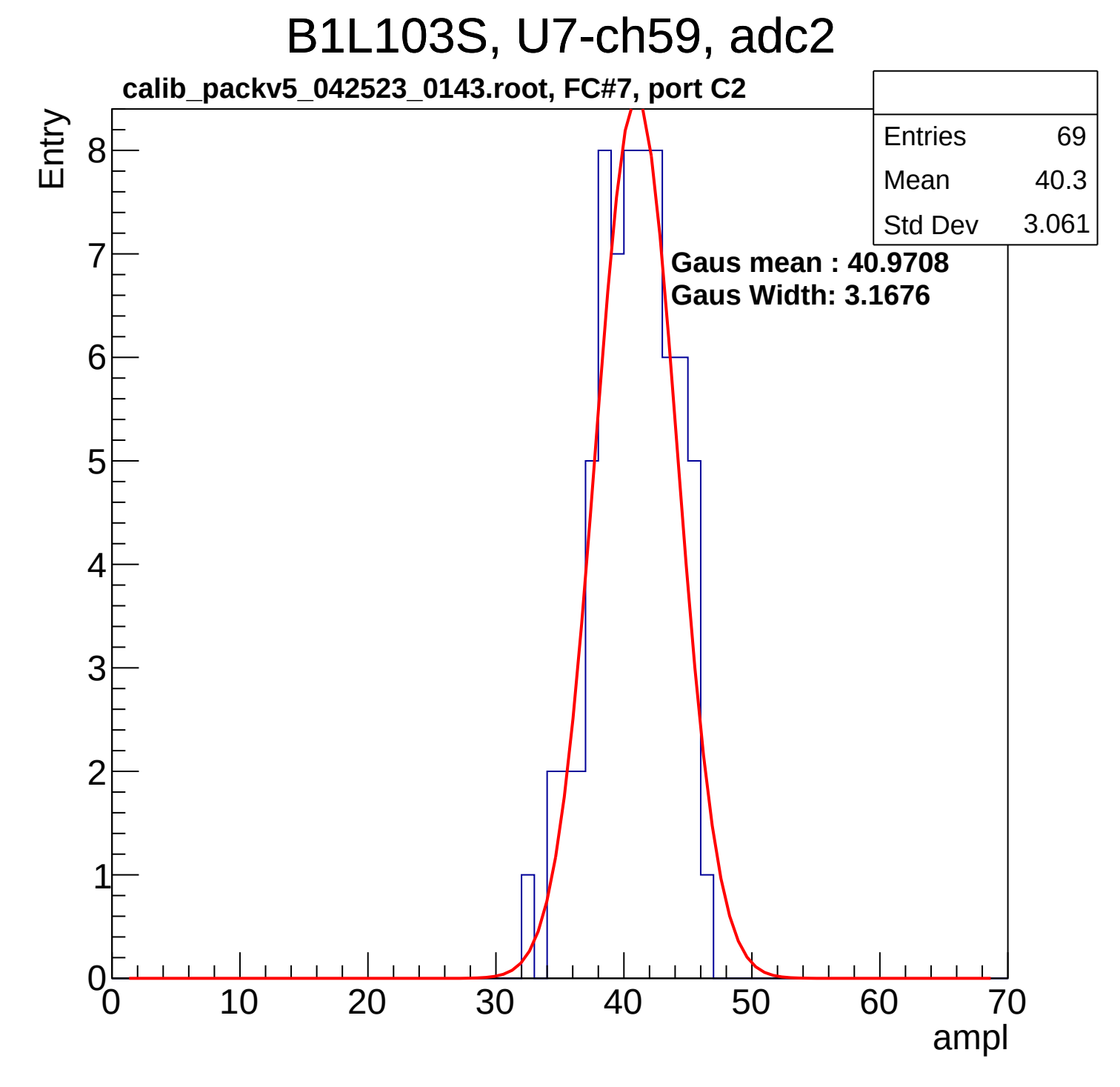
B1L103S, U7-ch59, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 40.3
Std Dev 3.061
Gaus mean : 40.9708
Gaus Width: 3.1676
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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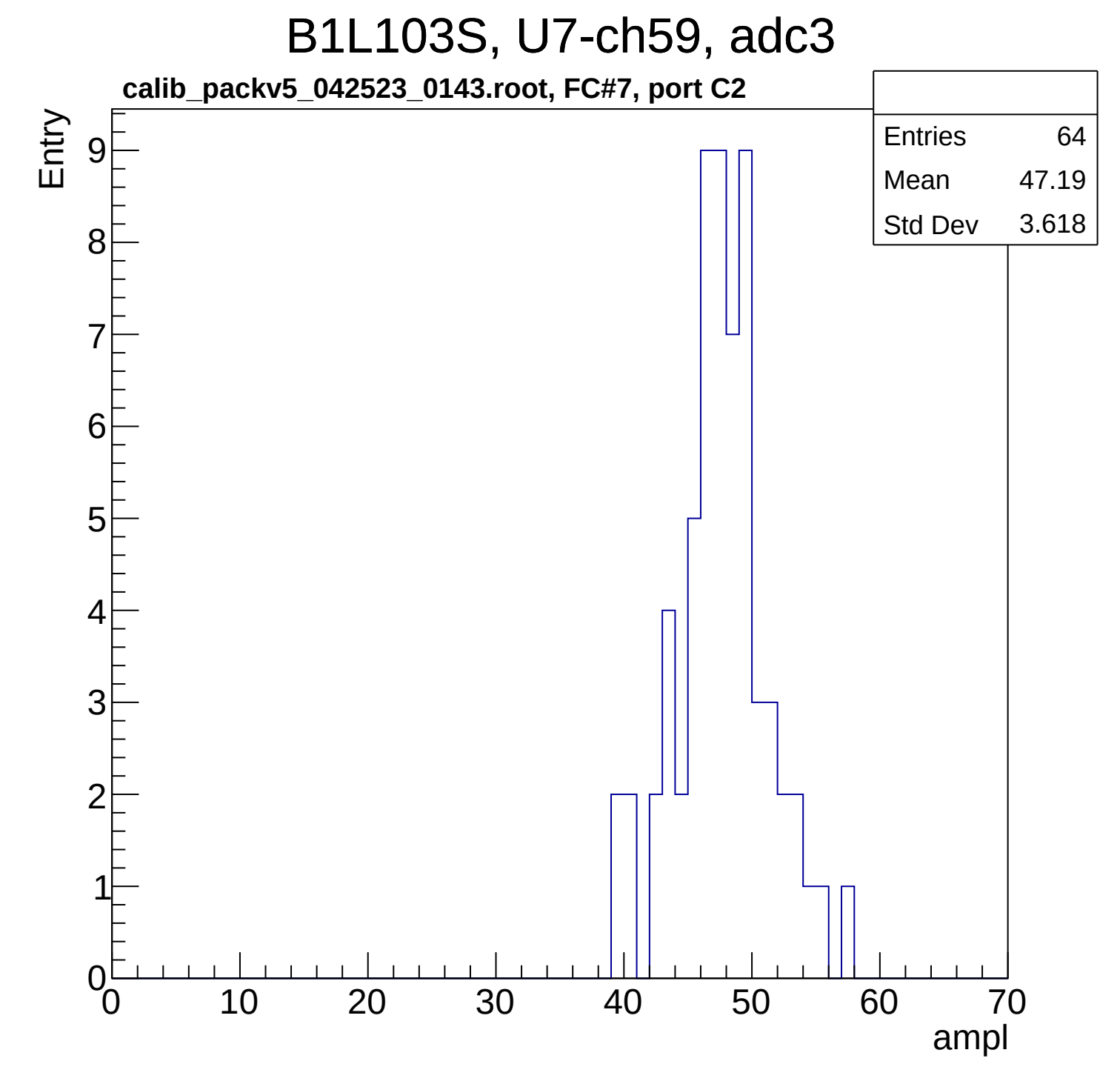
B1L103S, U7-ch59, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 47.19
Std Dev 3.618
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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60
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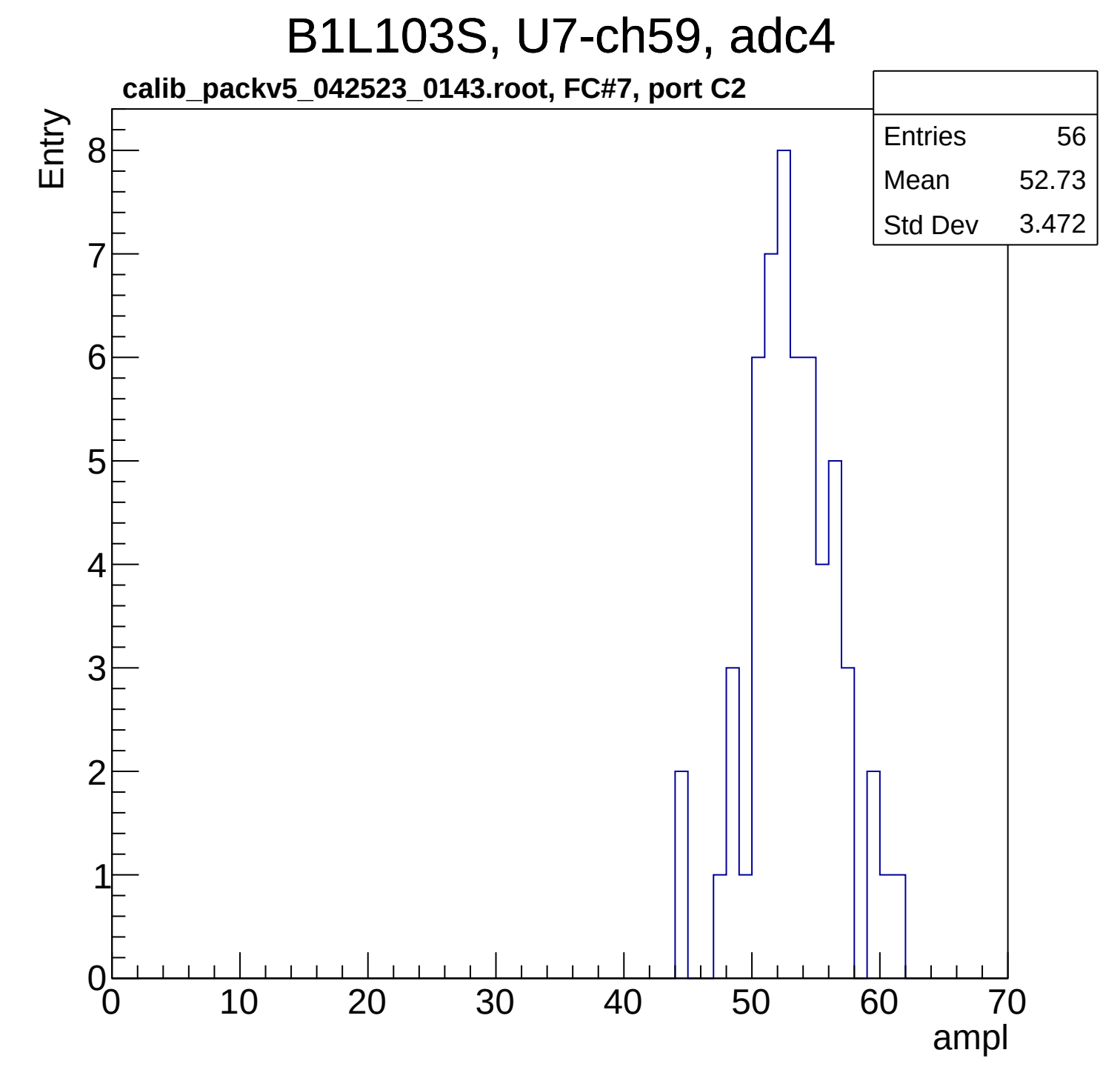
B1L103S, U7-ch59, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 52.73
Std Dev 3.472
Entry
ampl
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1
2
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4
5
6
7
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60
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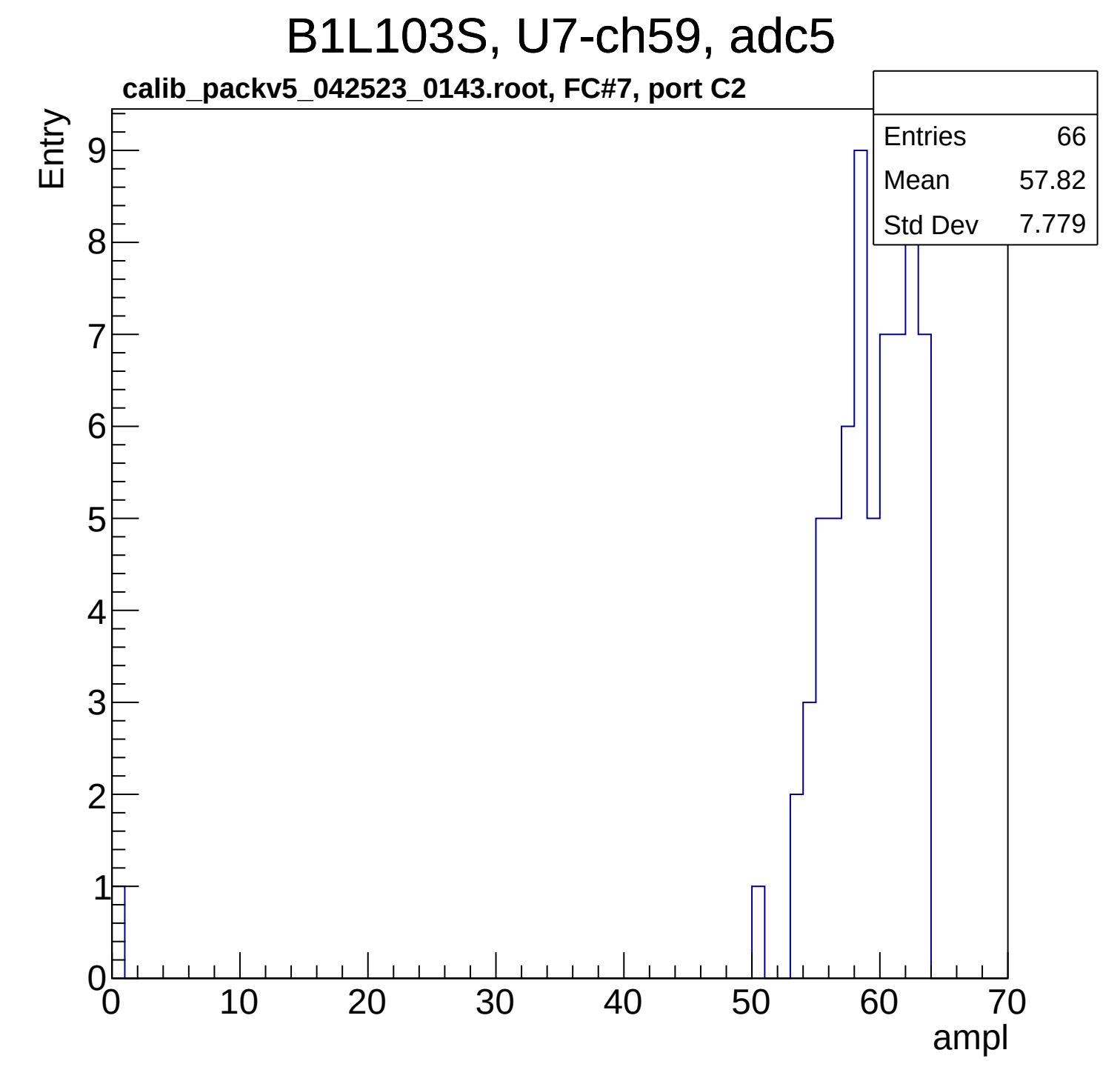
B1L103S, U7-ch59, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 57.82
Std Dev 7.779
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
50
60
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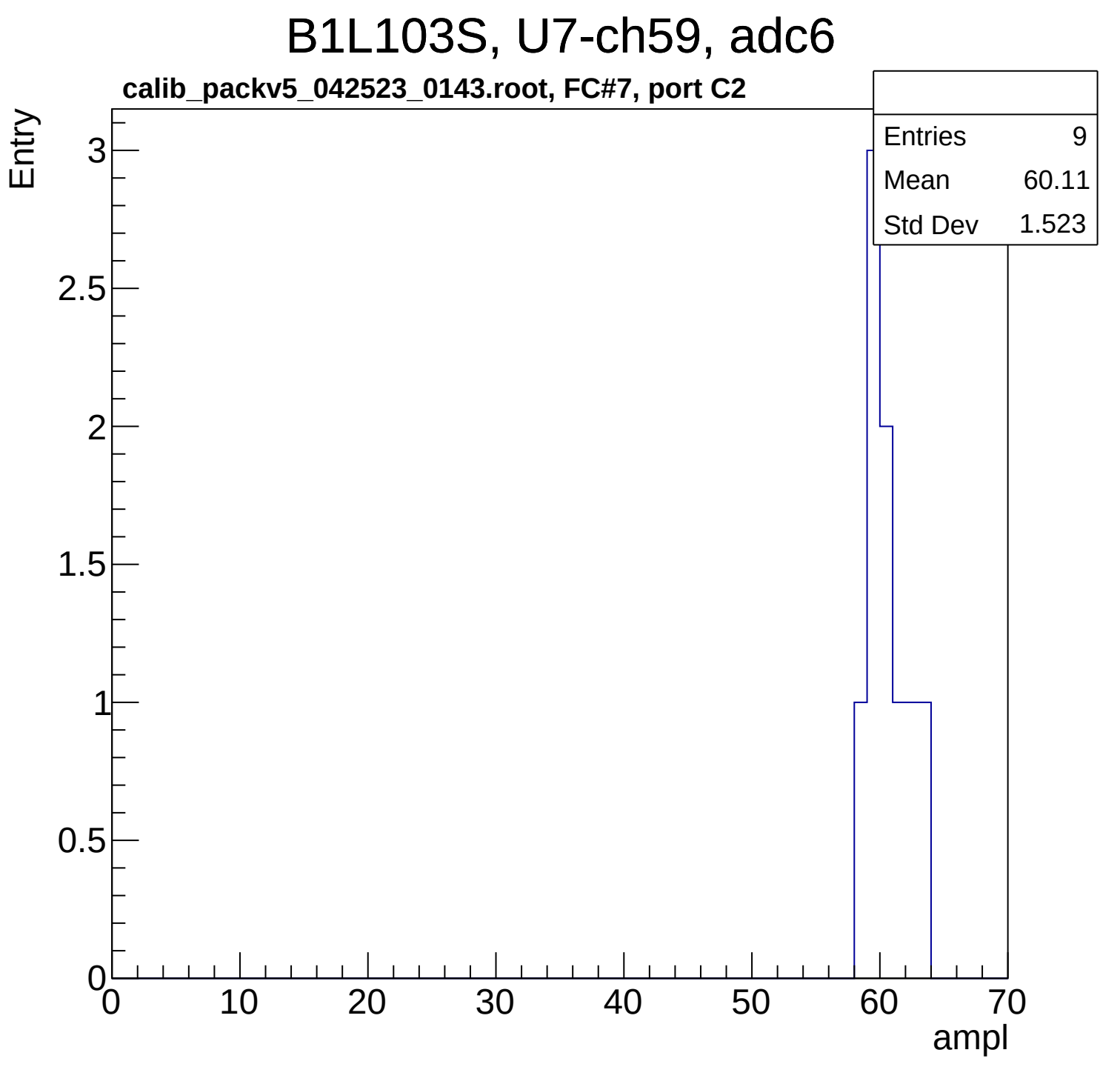
B1L103S, U7-ch59, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 9
Mean 60.11
Std Dev 1.523
Entry
ampl
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0.5
1
1.5
2
2.5
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0
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20
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40
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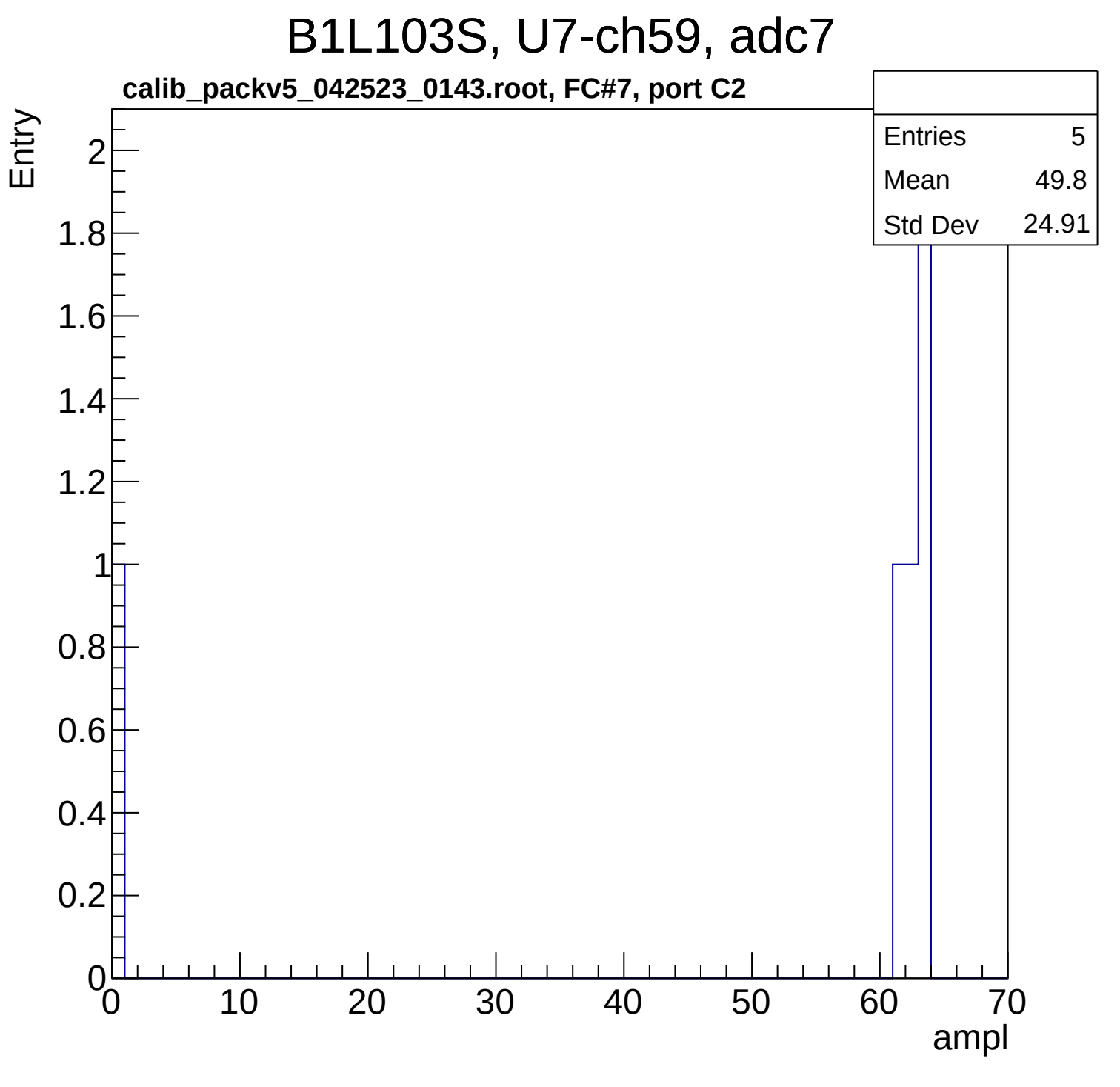
B1L103S, U7-ch59, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 5
Mean 49.8
Std Dev 24.91
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
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10
20
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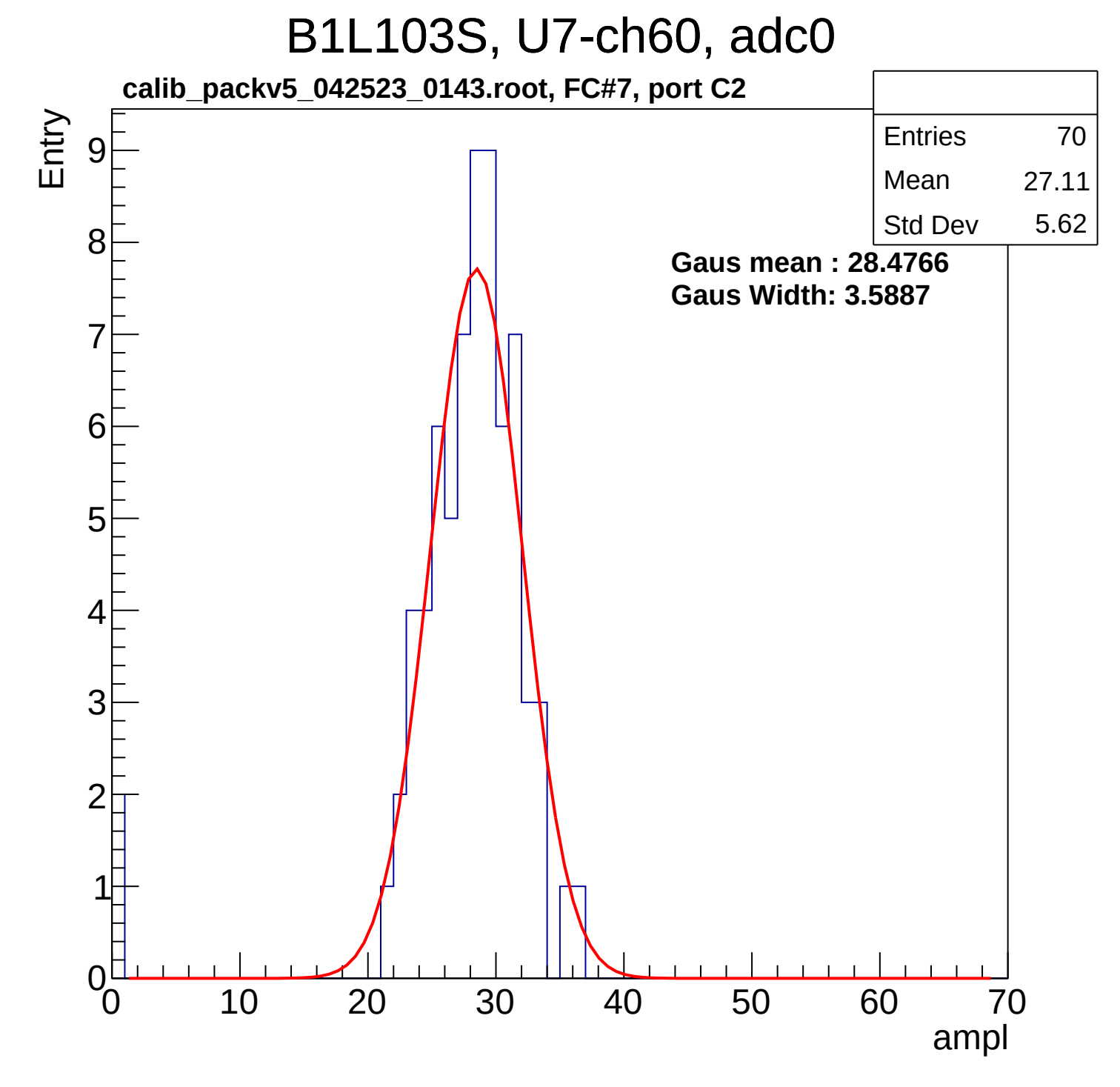
40
50
60
70


B1L103S, U7-ch60, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 27.11
Std Dev 5.62
Gaus mean : 28.4766
Gaus Width: 3.5887
Entry
ampl
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1
2
3
4
5
6
7
8
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0
10
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60
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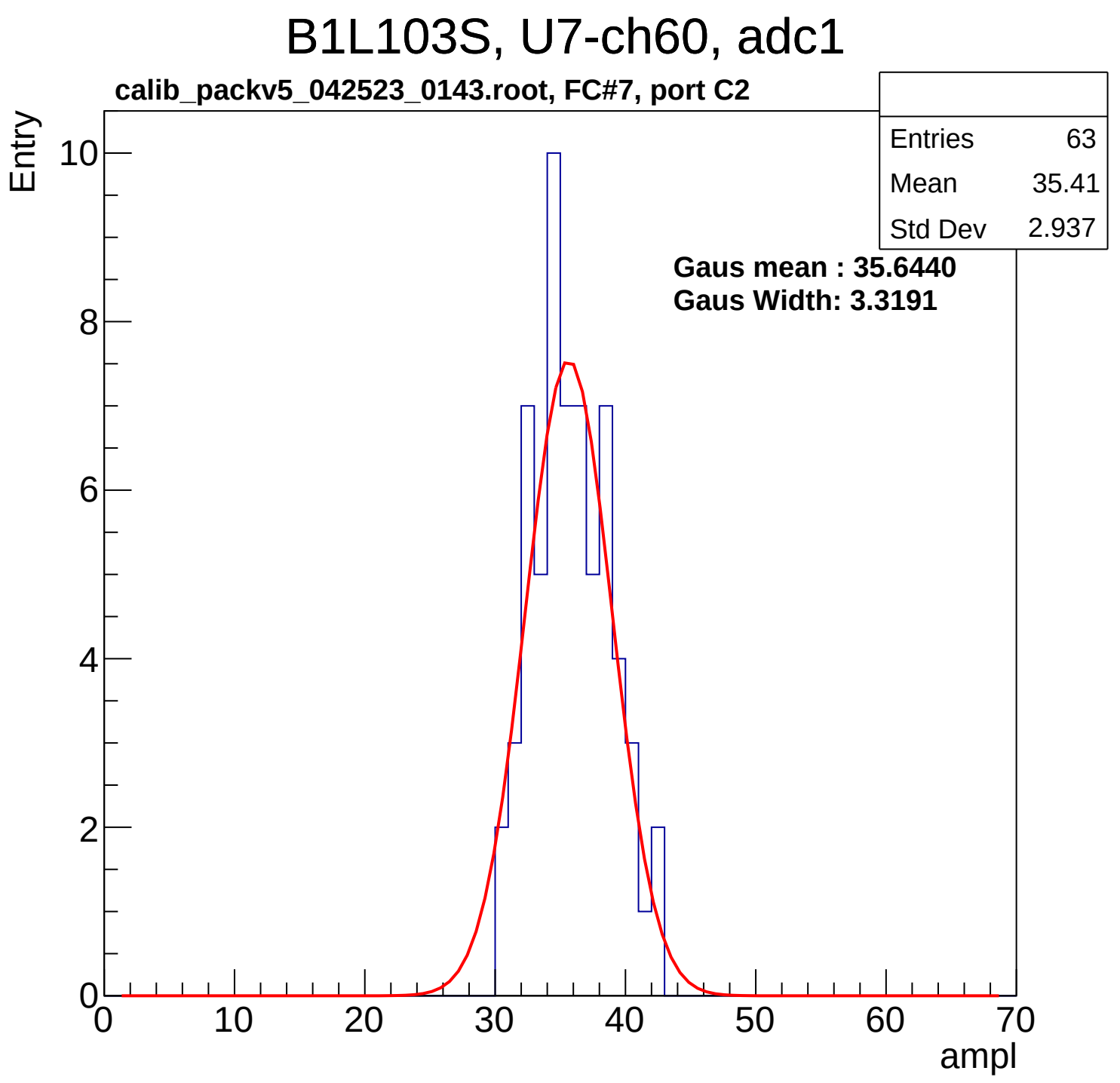
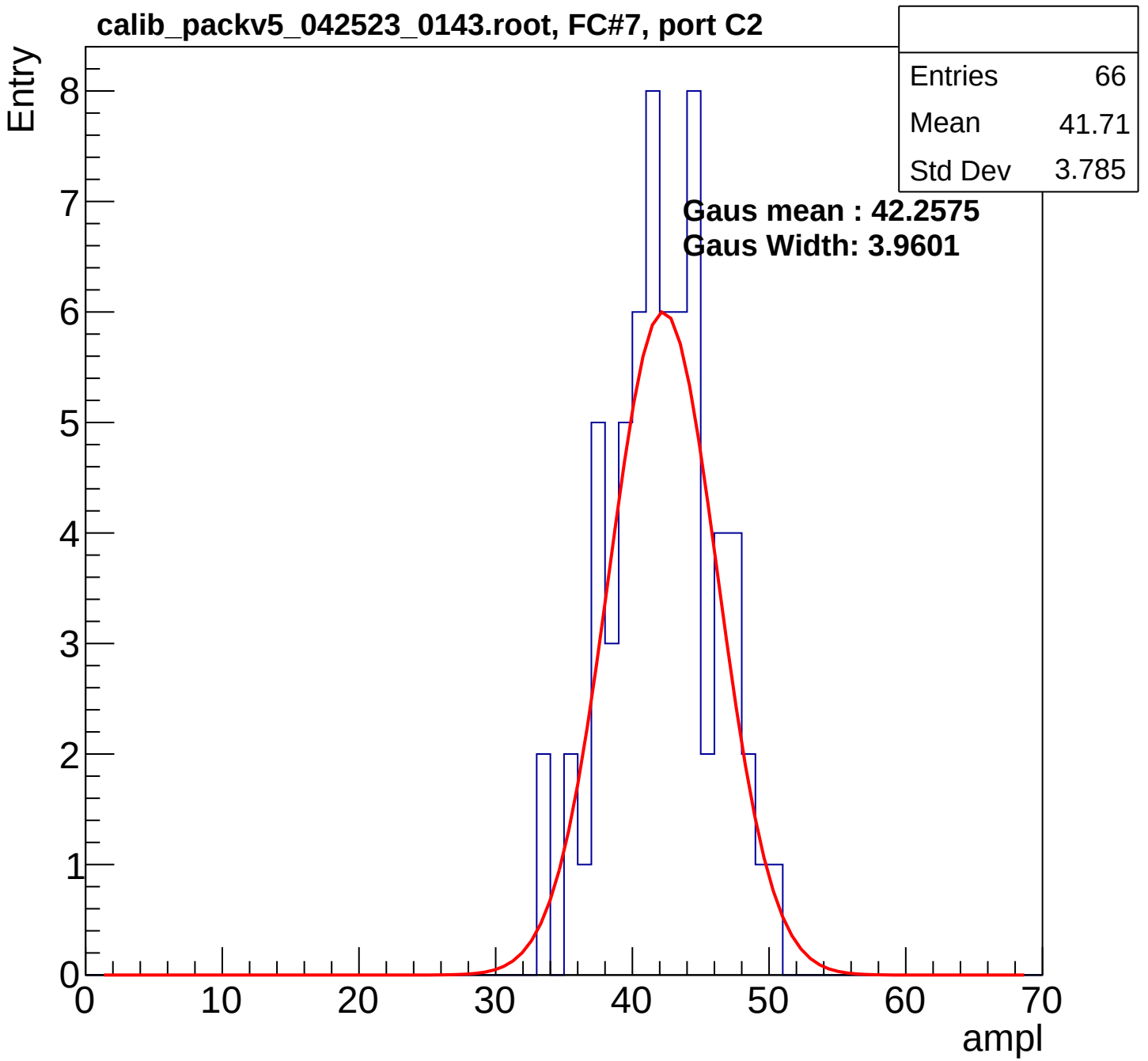
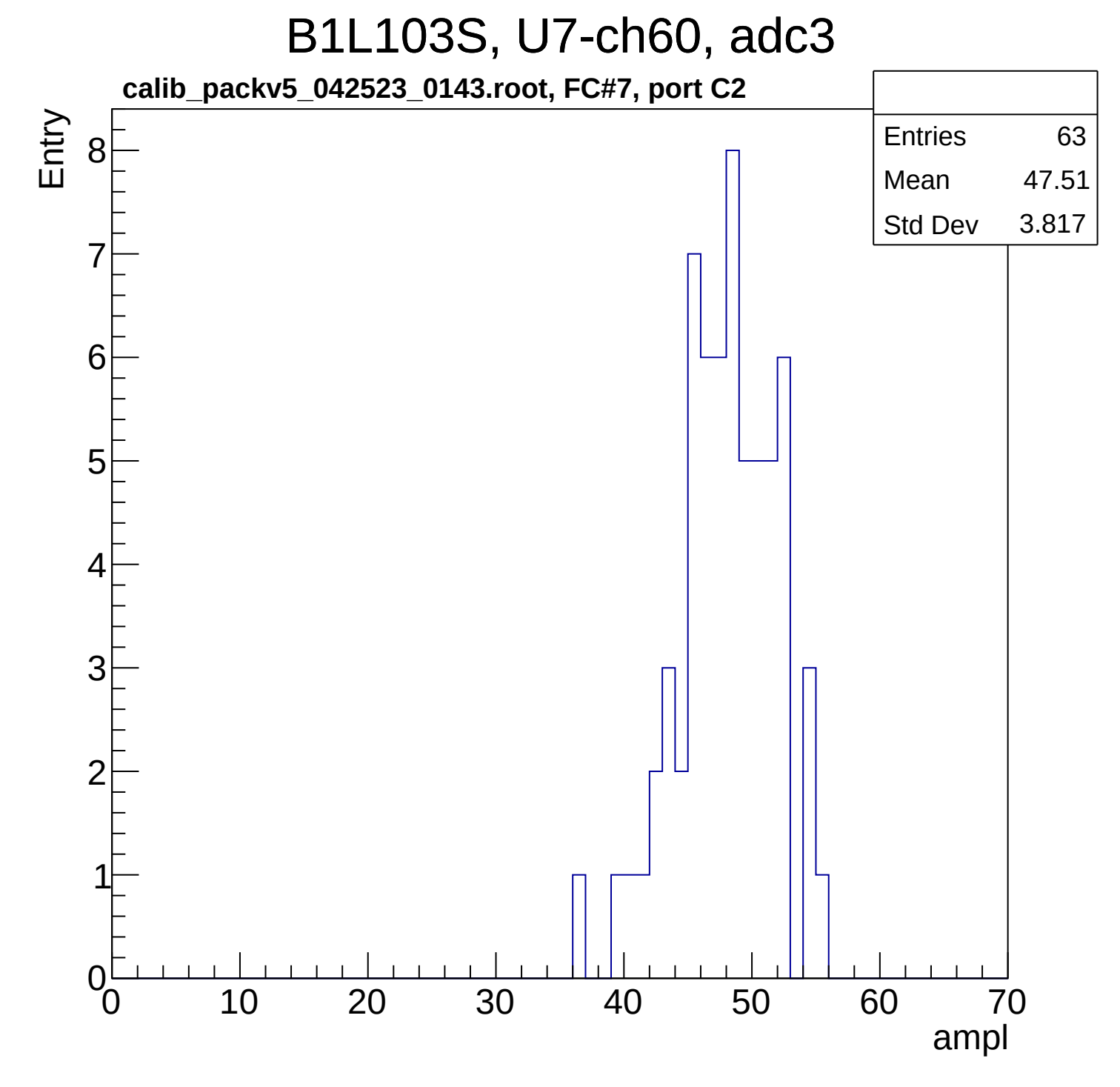

B1L103S, U7-ch60, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 35.41
Std Dev 2.937
Gaus mean : 35.6440
Gaus Width: 3.3191
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch60, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 41.71
Std Dev 3.785
Gaus mean : 42.2575
Gaus Width: 3.9601
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch60, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 47.51
Std Dev 3.817
Entry
ampl
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2
3
4
5
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0
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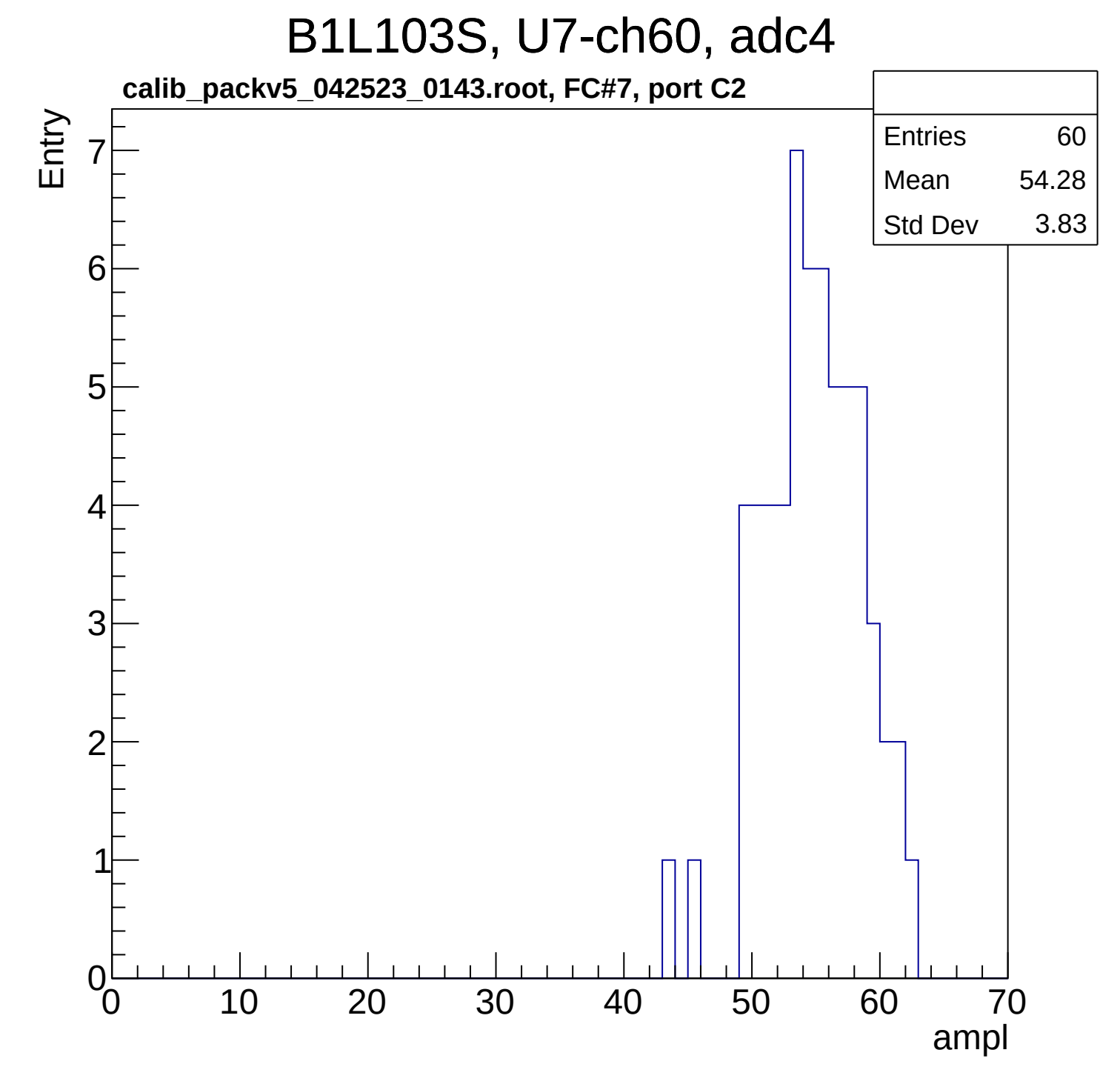
B1L103S, U7-ch60, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 60
Mean 54.28
Std Dev 3.83
Entry
ampl
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1
2
3
4
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6
7
0
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20
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40
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60
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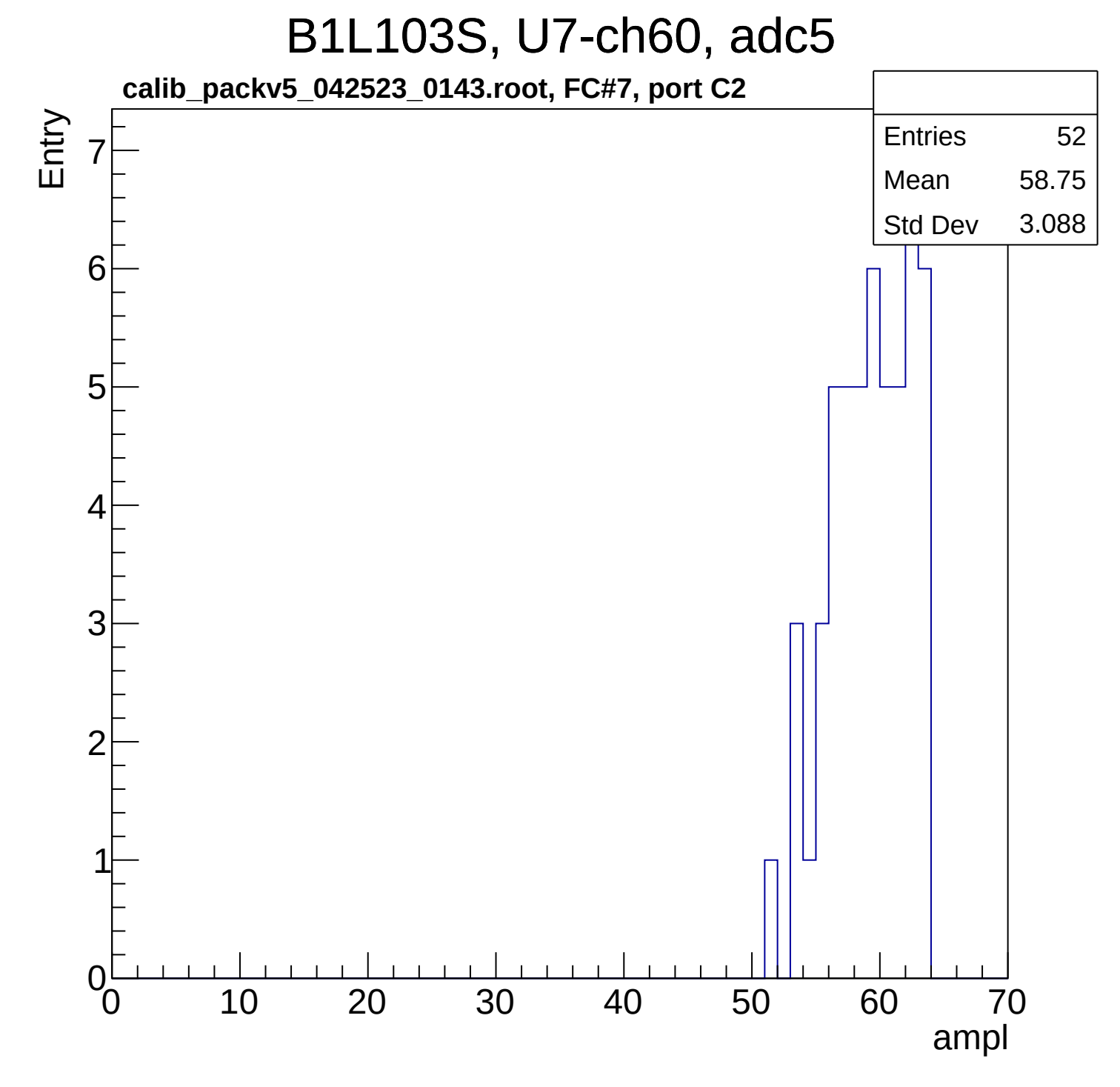
B1L103S, U7-ch60, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 52
Mean 58.75
Std Dev 3.088
Entry
ampl
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0
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40
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60
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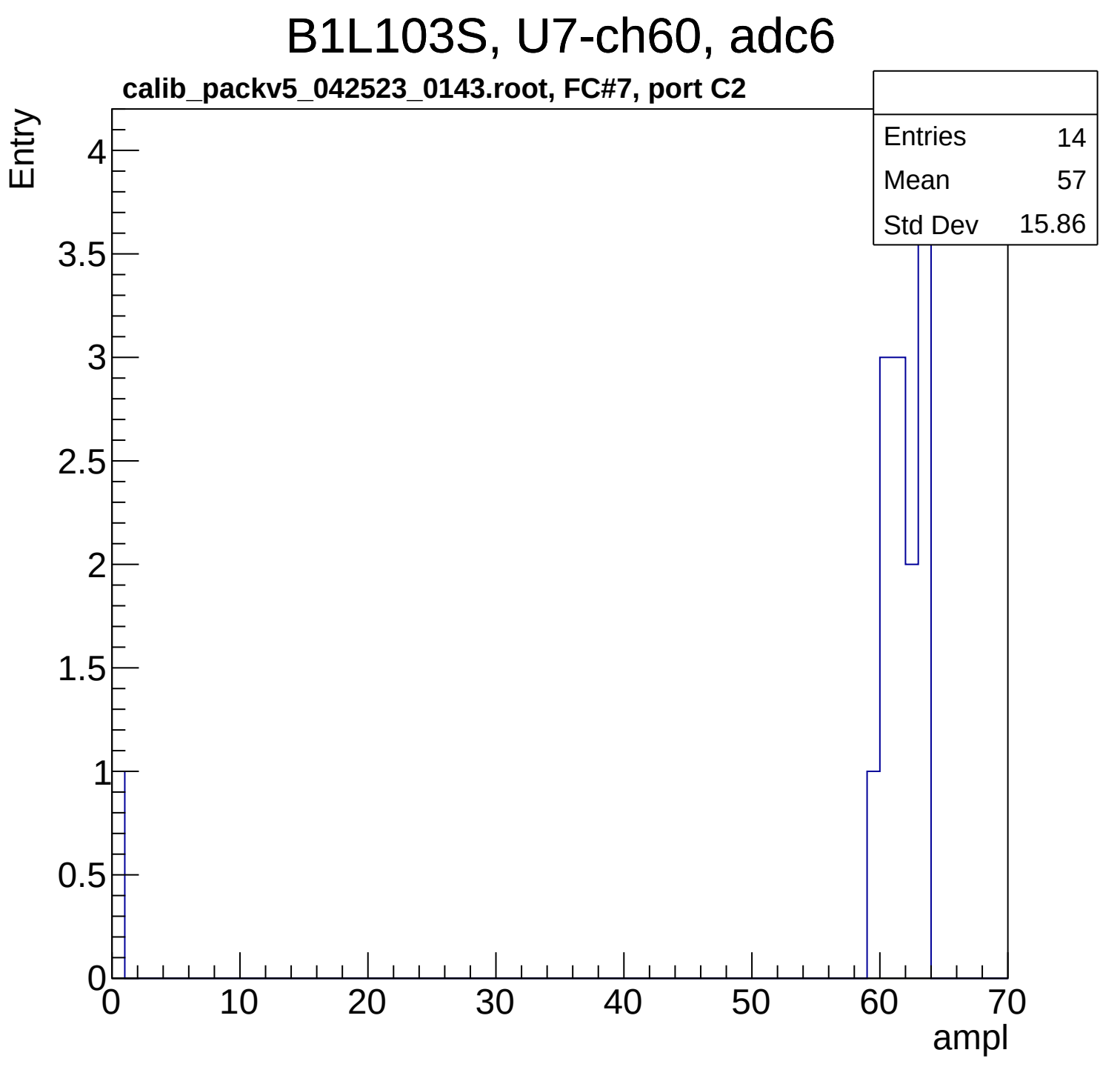
B1L103S, U7-ch60, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 14
Mean 57
Std Dev 15.86
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
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40
50
60
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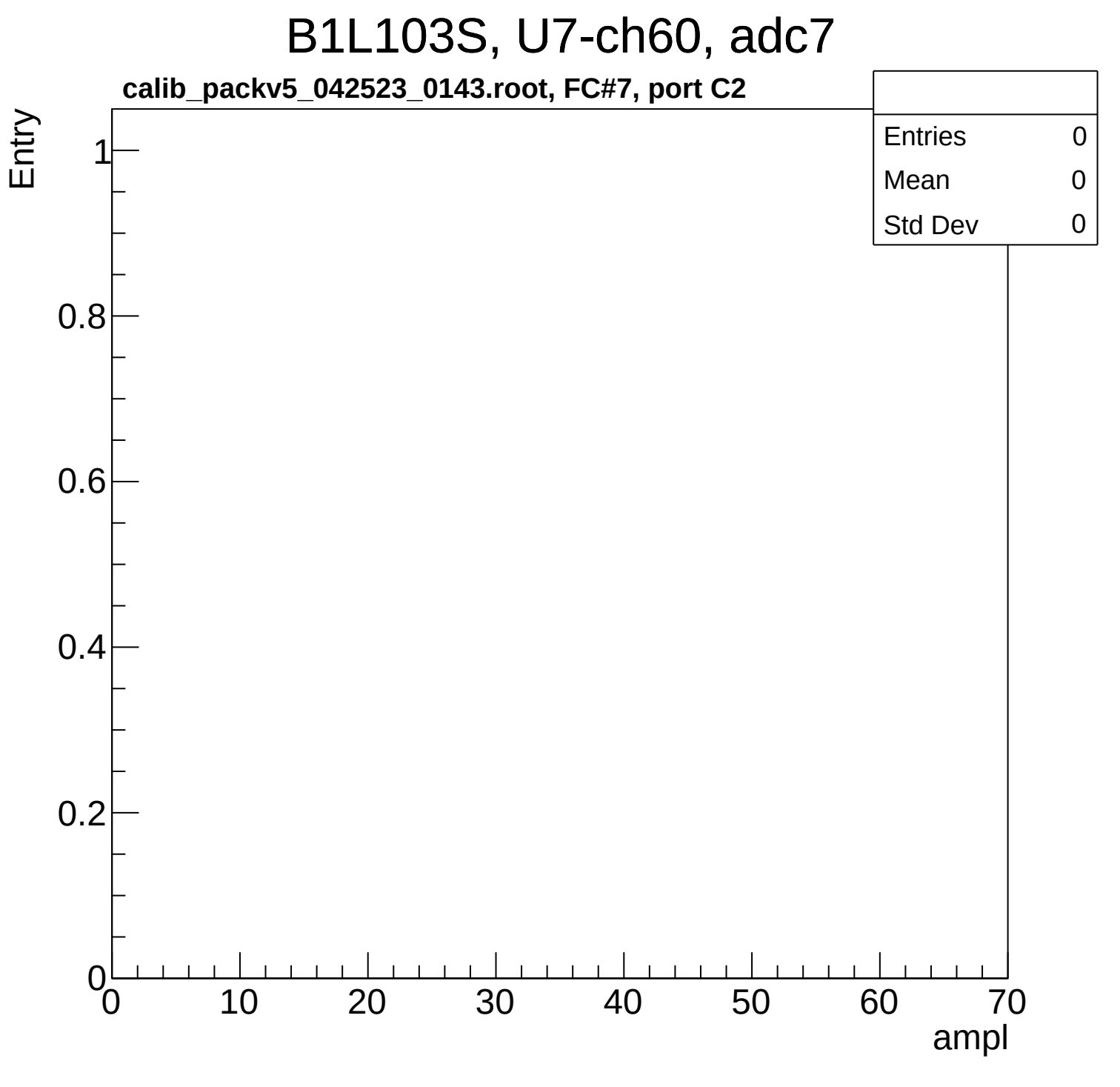
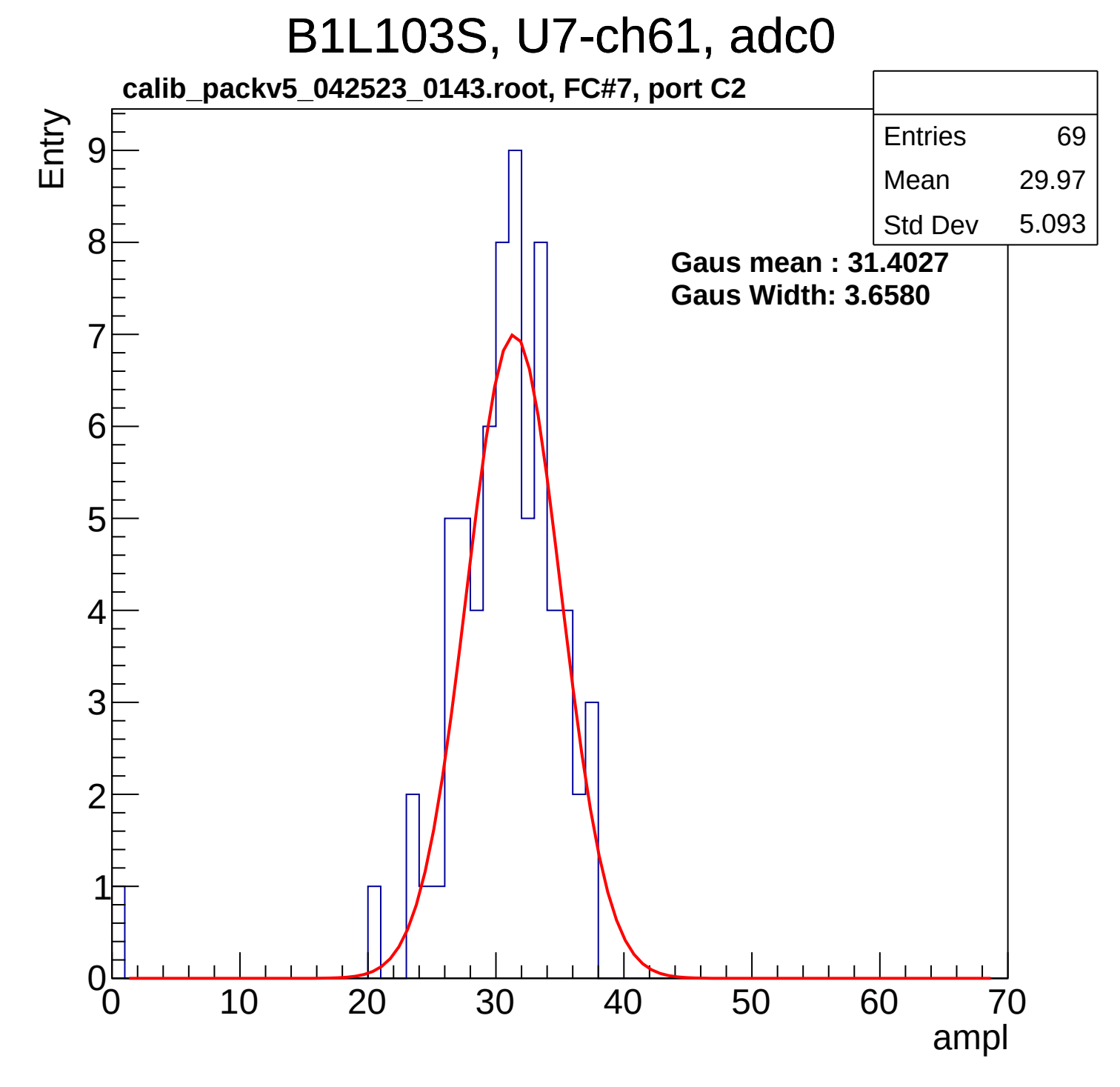
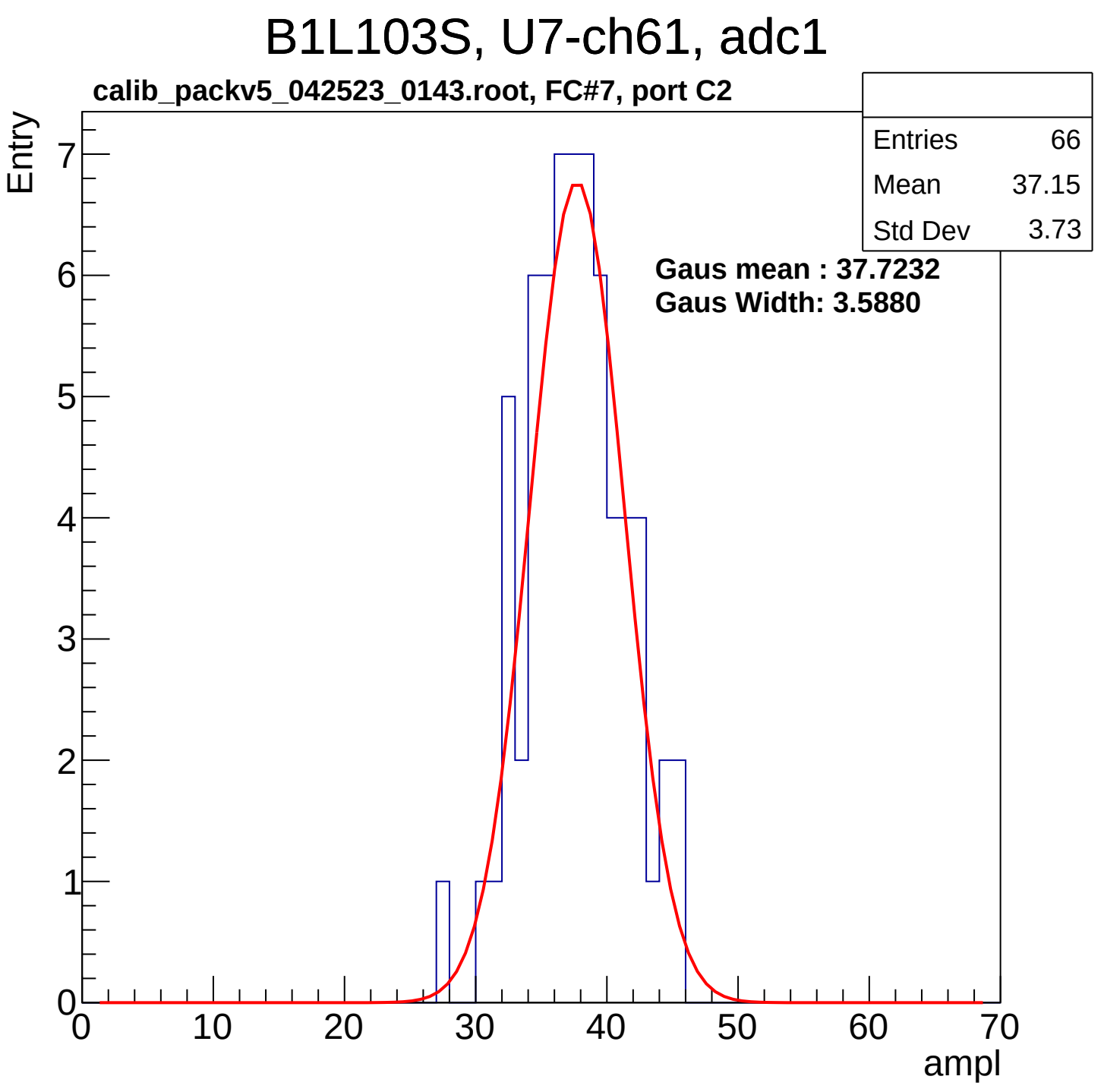
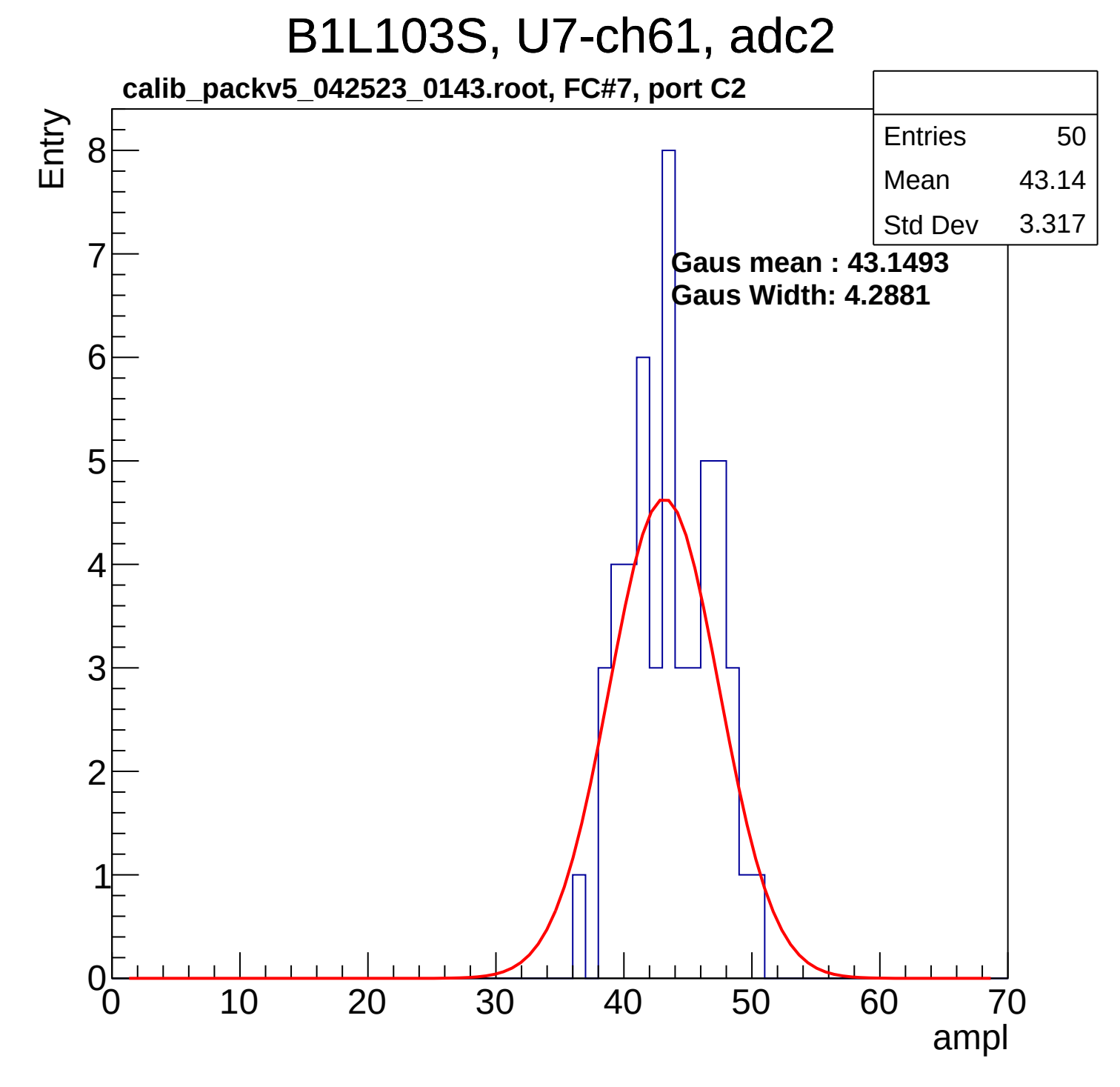
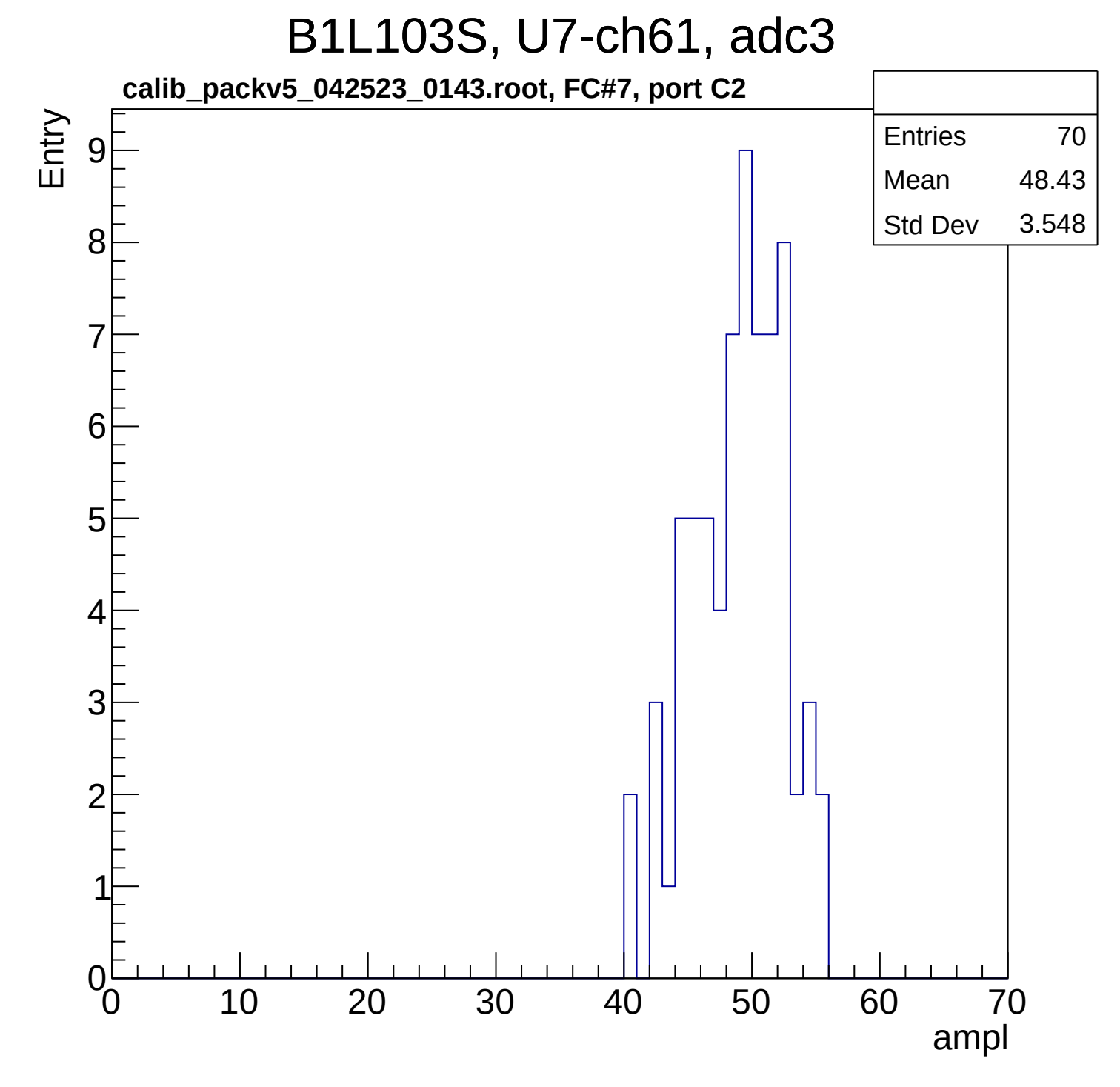

B1L103S, U7-ch60, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch61, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 29.97
Std Dev 5.093
Gaus mean : 31.4027
Gaus Width: 3.6580
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch61, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 37.15
Std Dev 3.73
Gaus mean : 37.7232
Gaus Width: 3.5880
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch61, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 50
Mean 43.14
Std Dev 3.317
Gaus mean : 43.1493
Gaus Width: 4.2881
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch61, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 48.43
Std Dev 3.548
Entry
ampl
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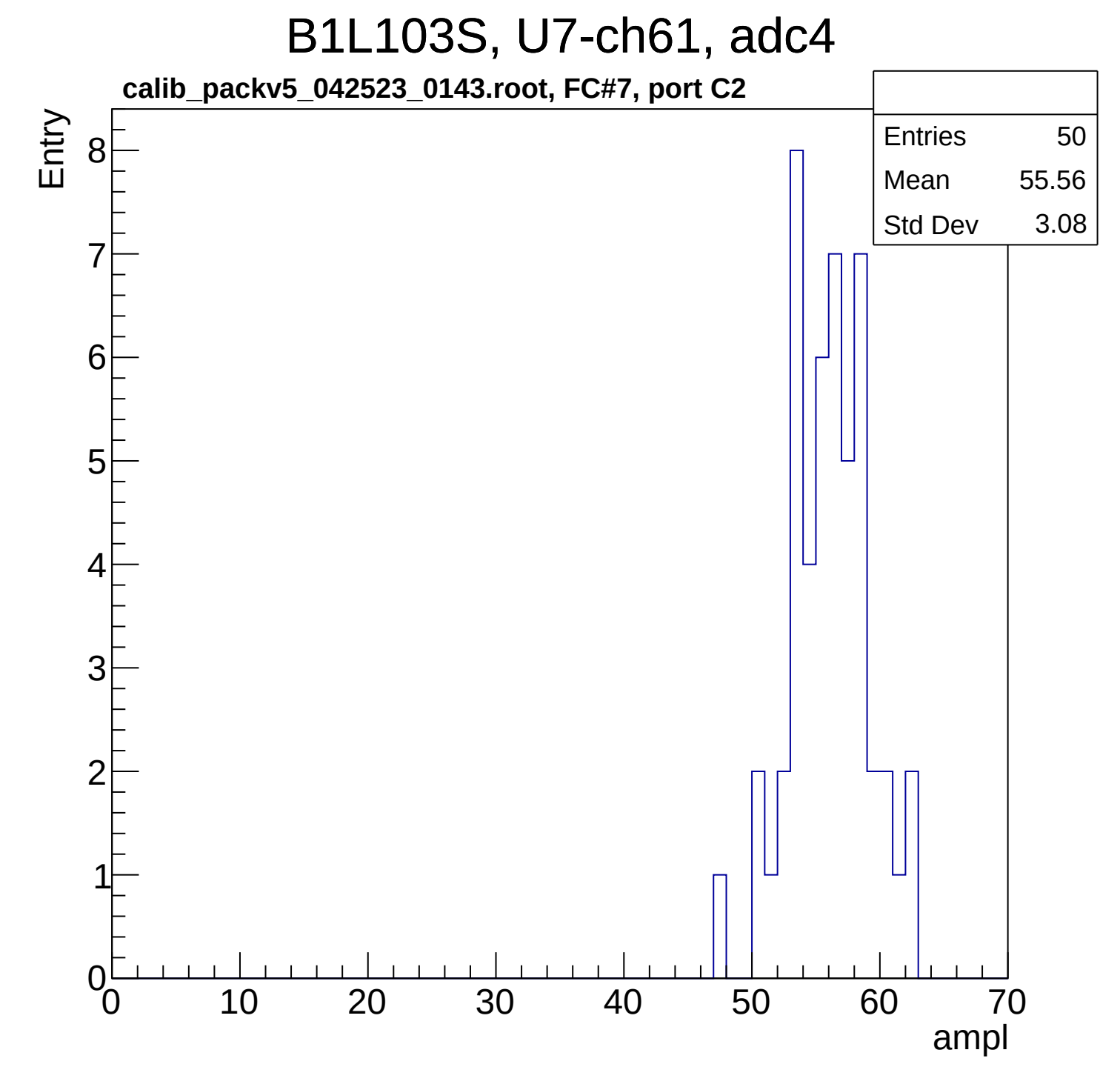
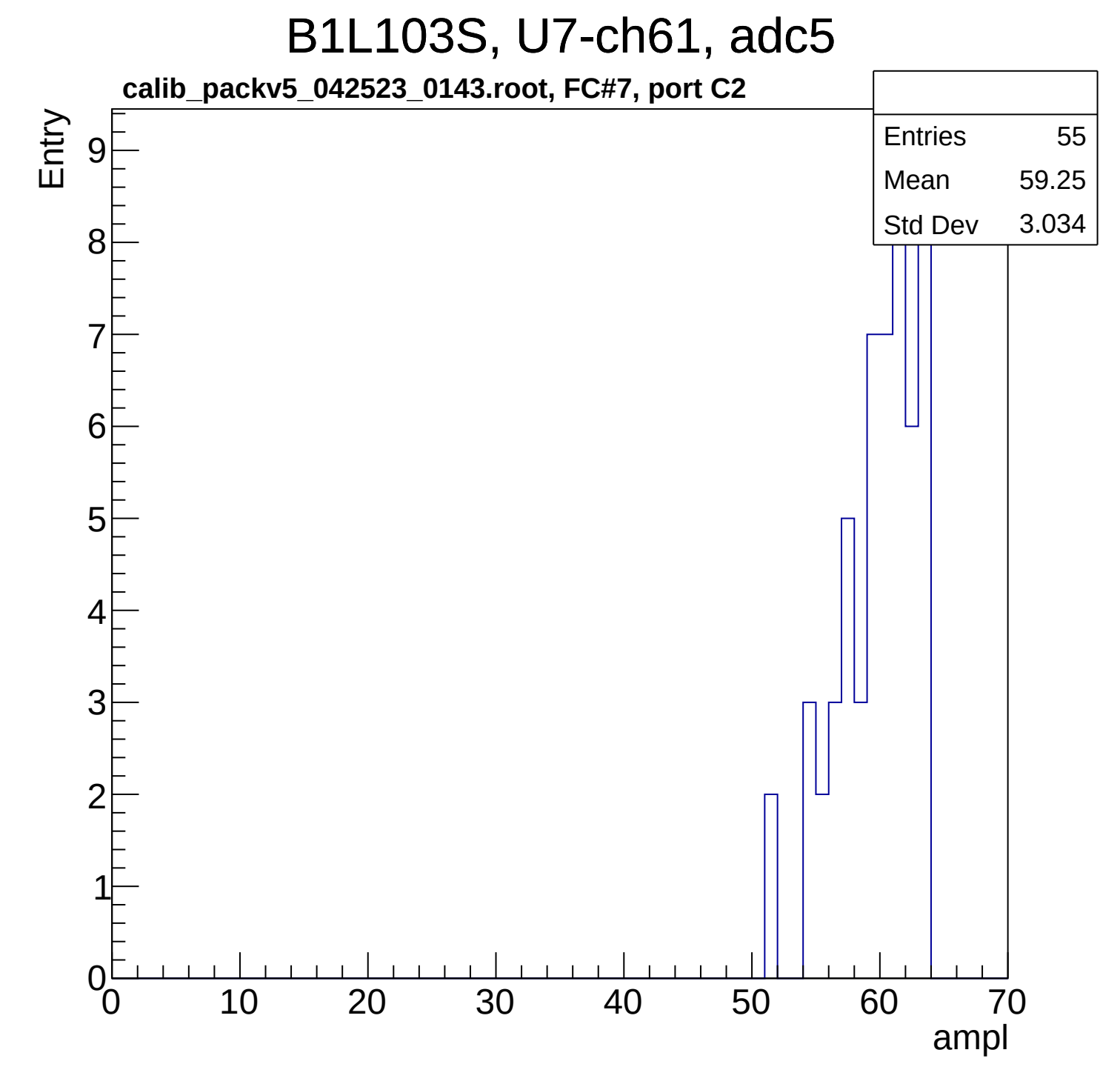
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch61, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 50
Mean 55.56
Std Dev 3.08
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch61, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 59.25
Std Dev 3.034
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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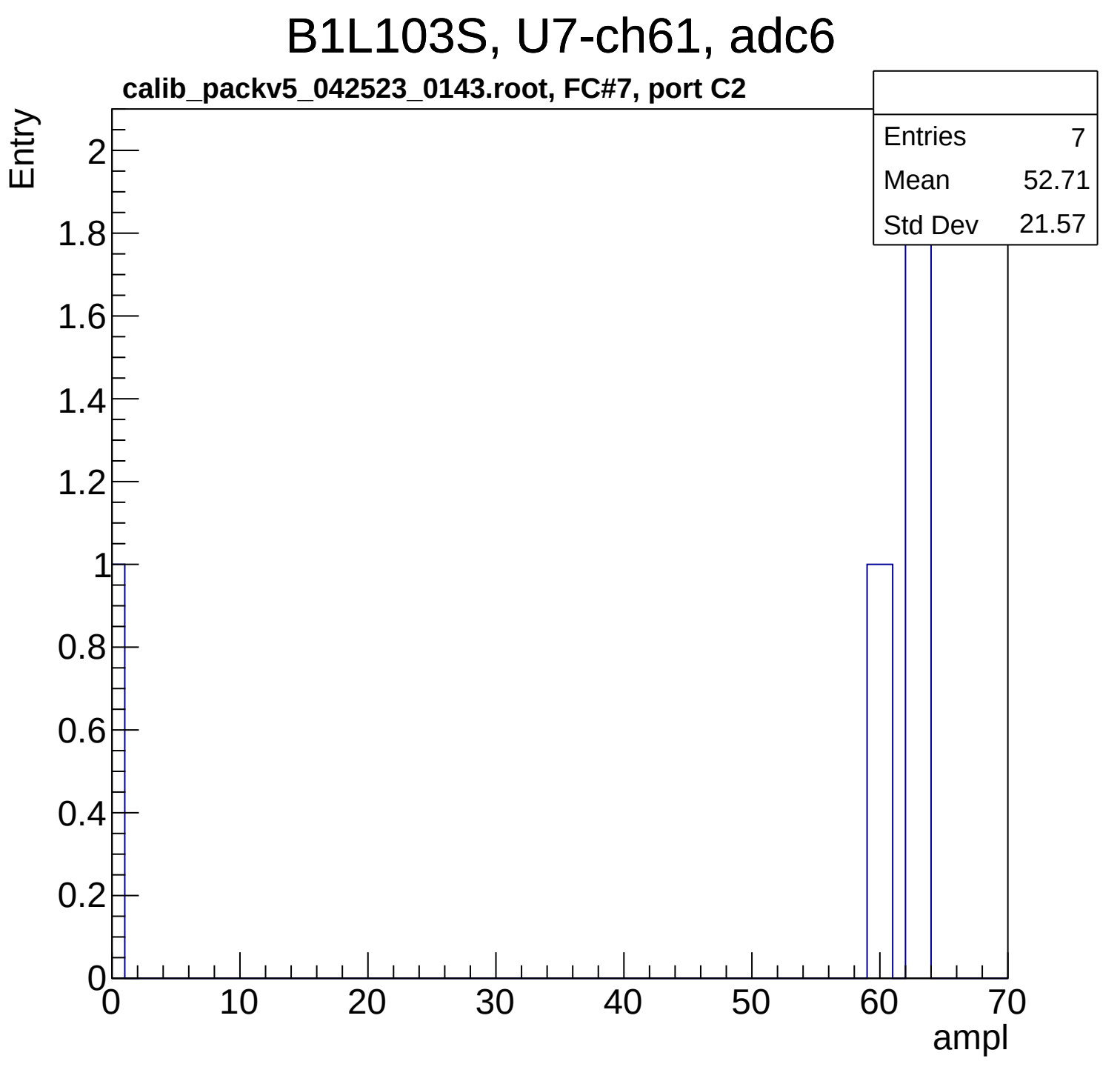
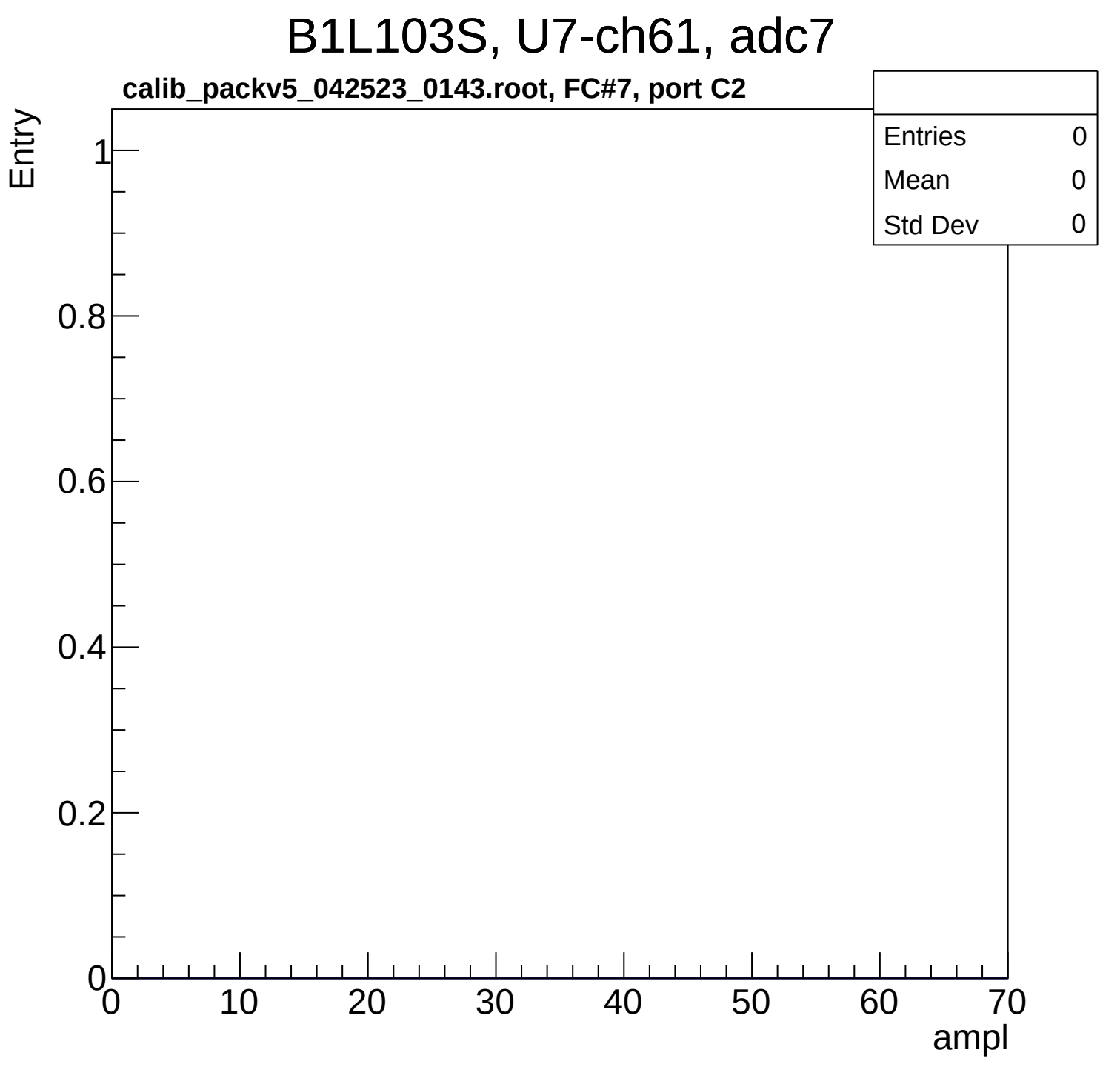
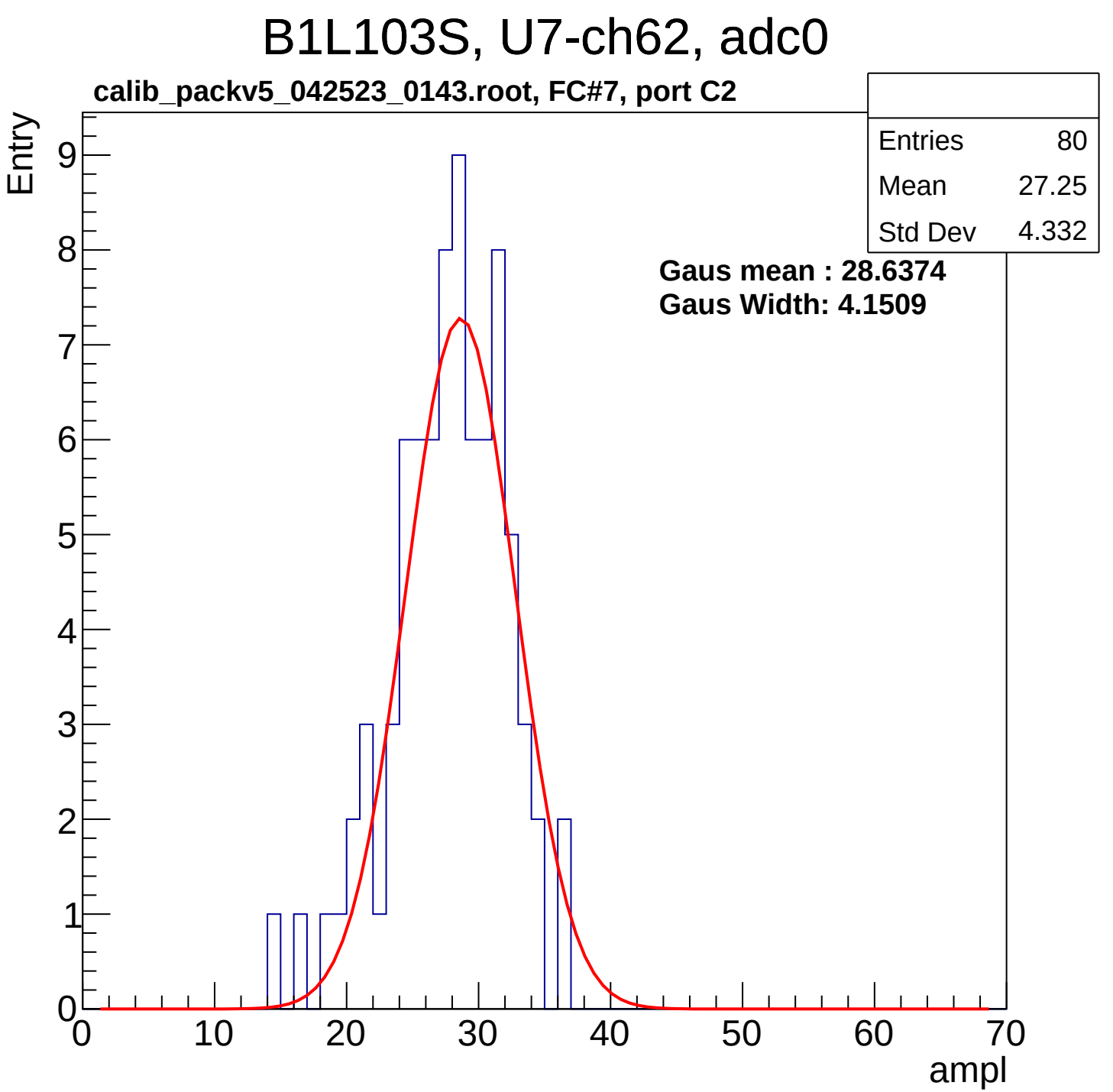
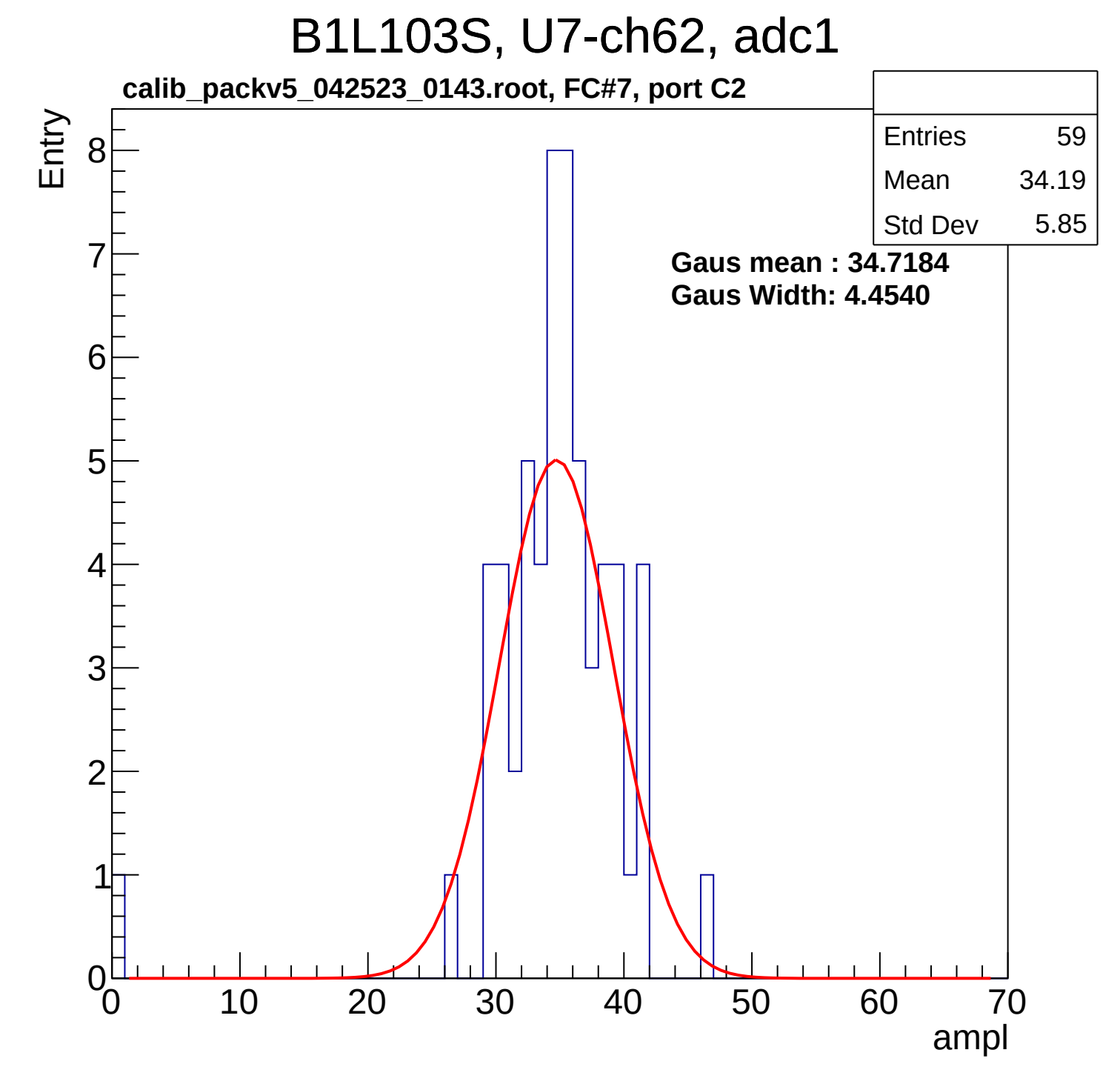
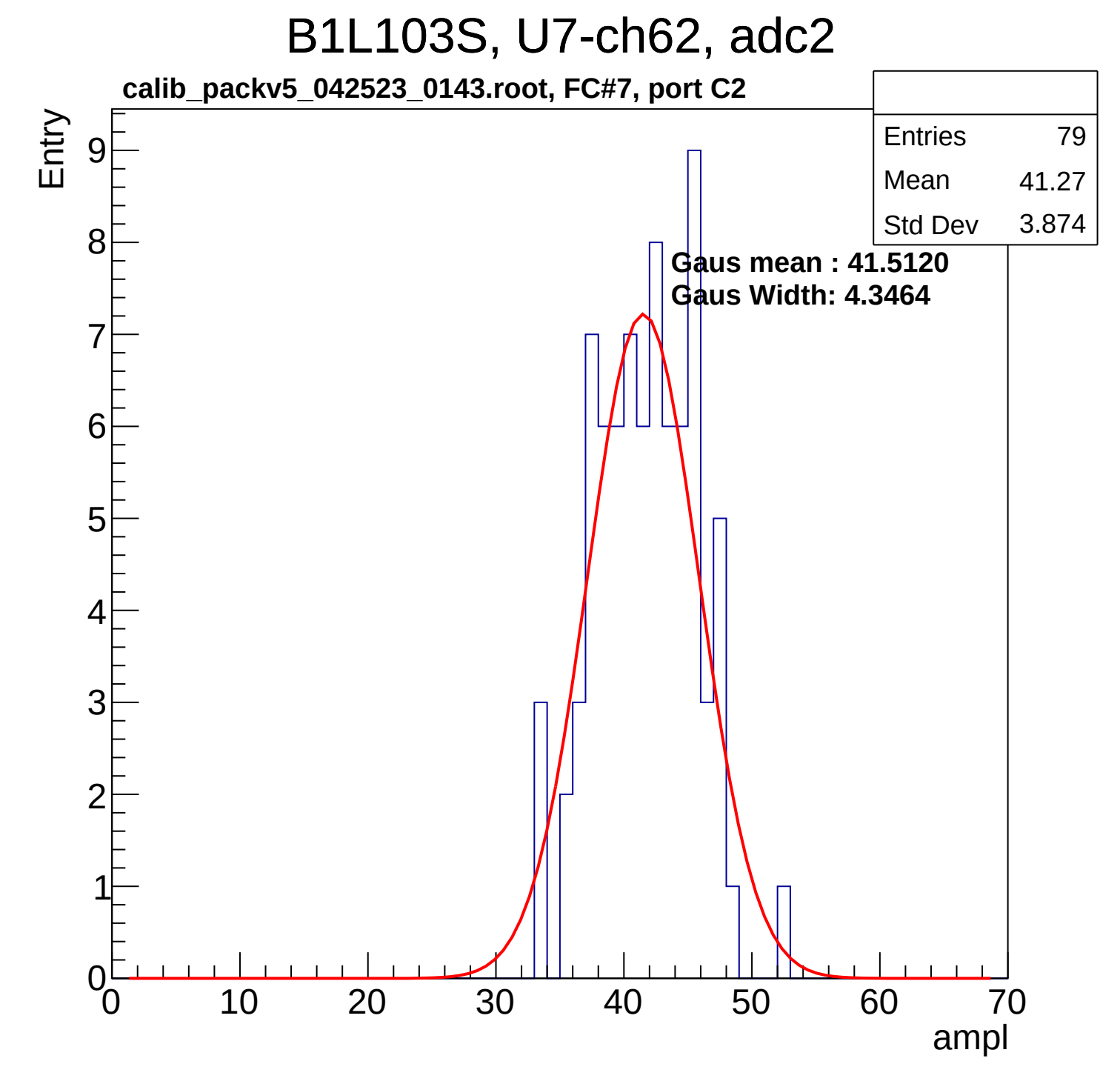

B1L103S, U7-ch61, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 7
Mean 52.71
Std Dev 21.57
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U7-ch61, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch62, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 80
Mean 27.25
Std Dev 4.332
Gaus mean : 28.6374
Gaus Width: 4.1509
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch62, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 34.19
Std Dev 5.85
Gaus mean : 34.7184
Gaus Width: 4.4540
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch62, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 79
Mean 41.27
Std Dev 3.874
Gaus mean : 41.5120
Gaus Width: 4.3464
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
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60
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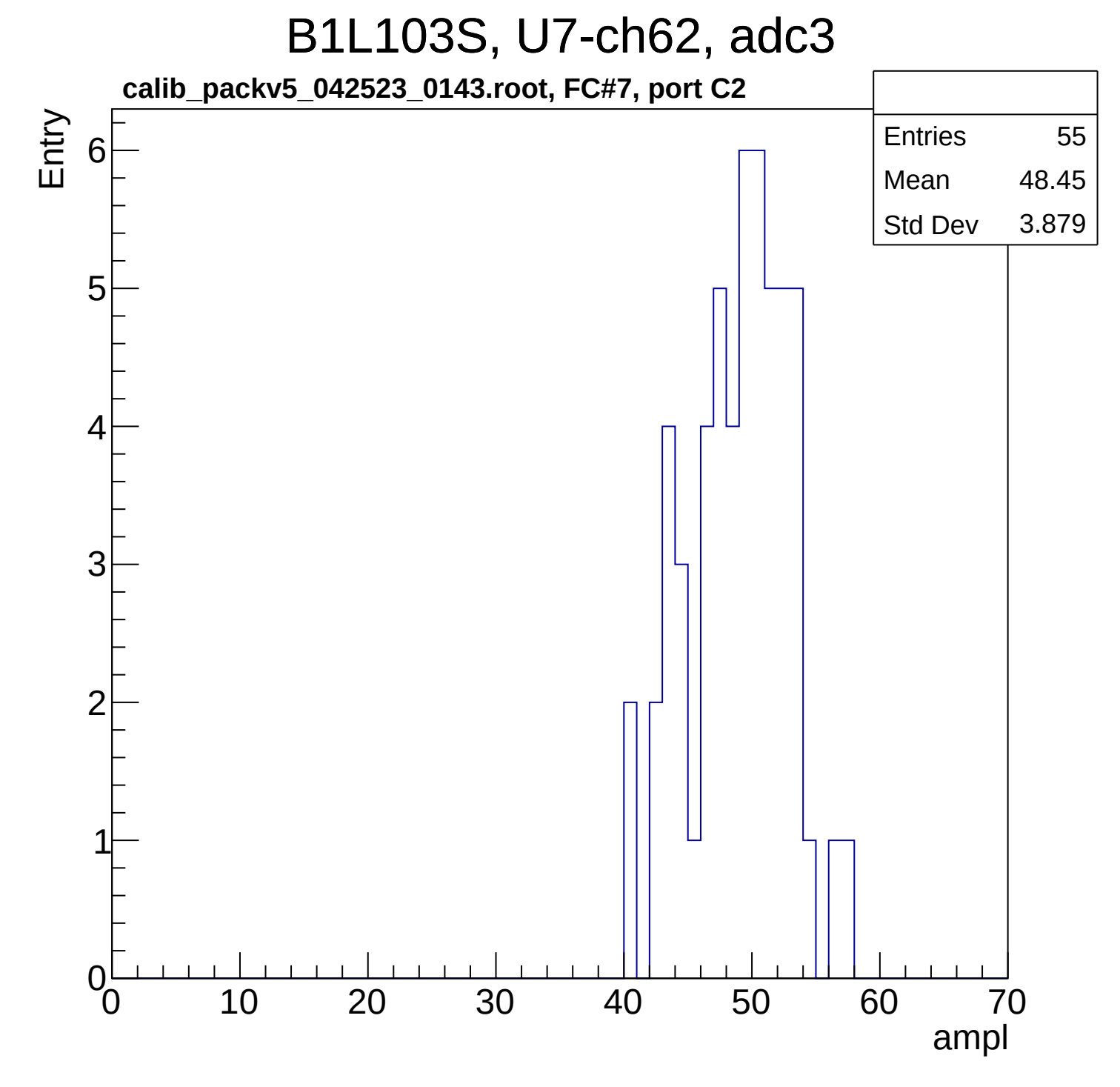
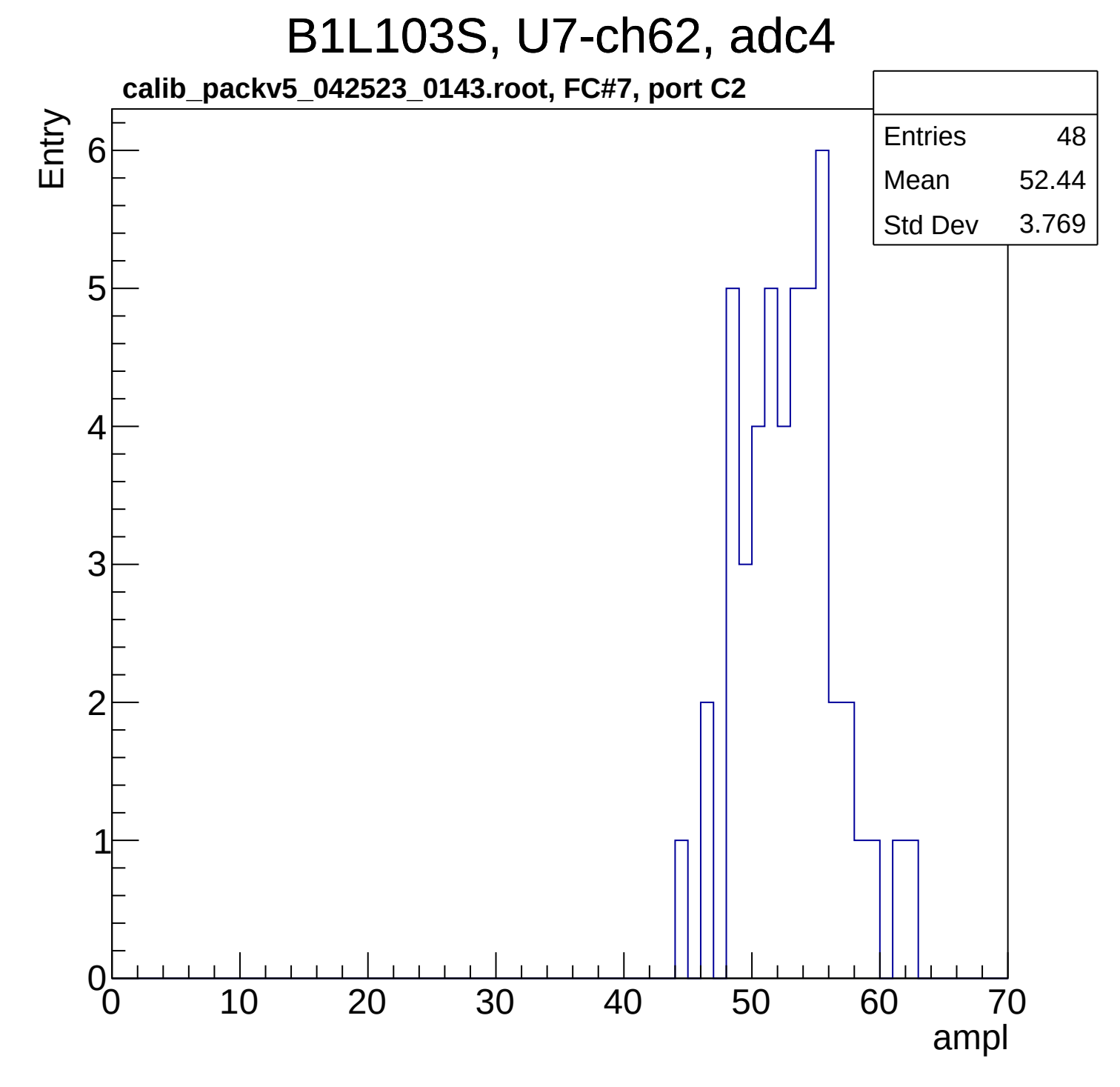
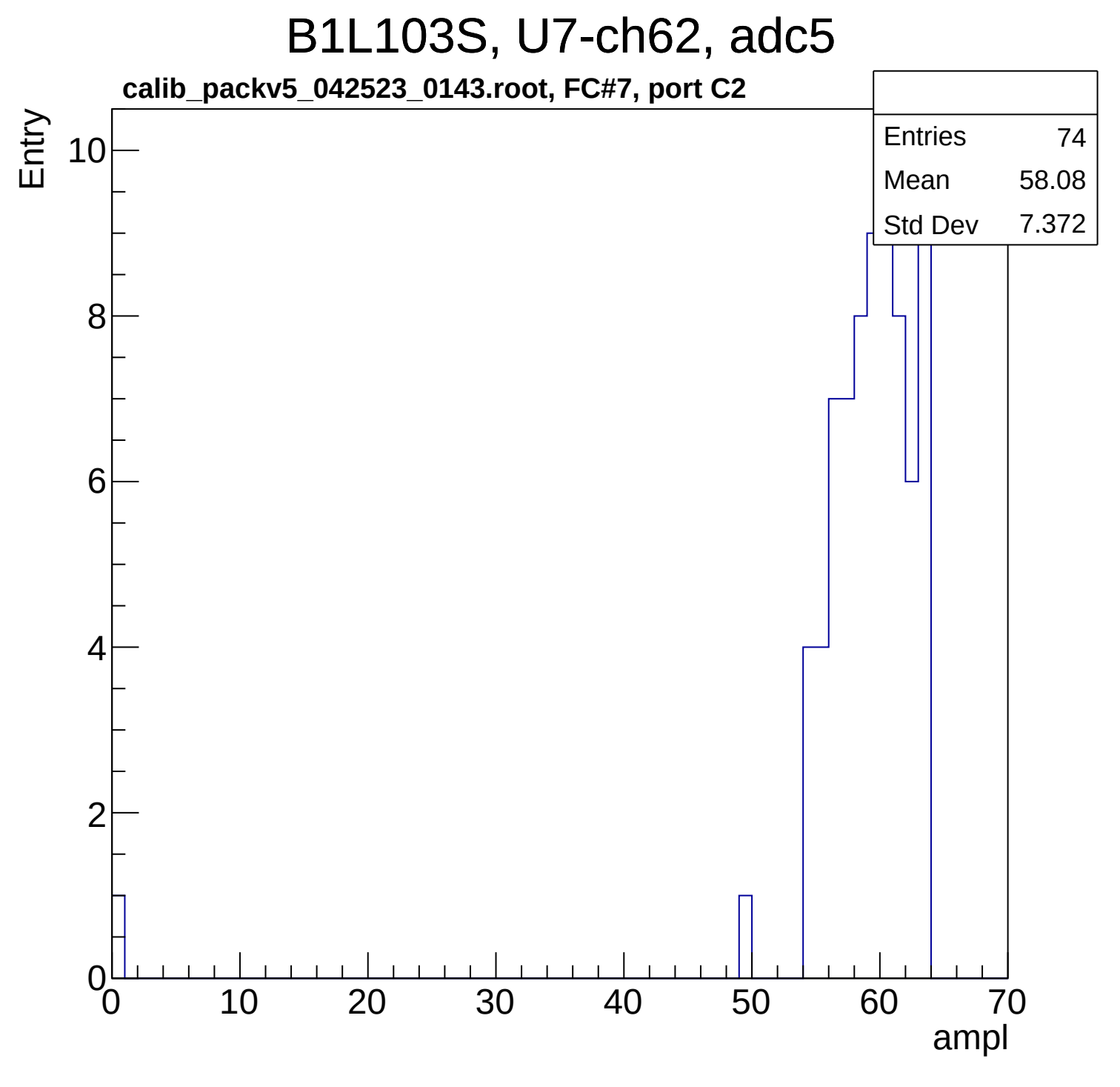
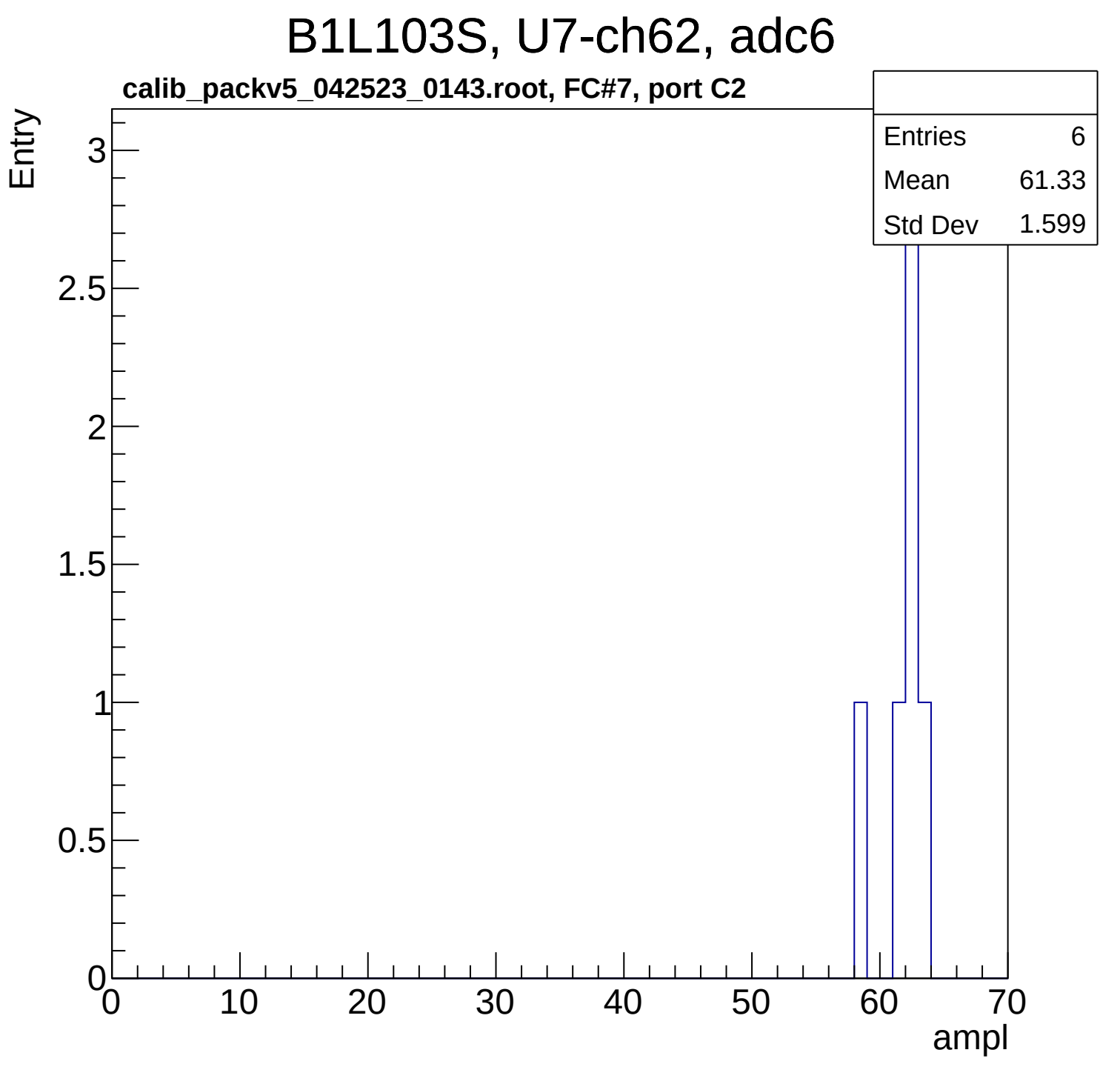

B1L103S, U7-ch62, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 48.45
Std Dev 3.879
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U7-ch62, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 48
Mean 52.44
Std Dev 3.769
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U7-ch62, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 74
Mean 58.08
Std Dev 7.372
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch62, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 6
Mean 61.33
Std Dev 1.599
Entry
ampl
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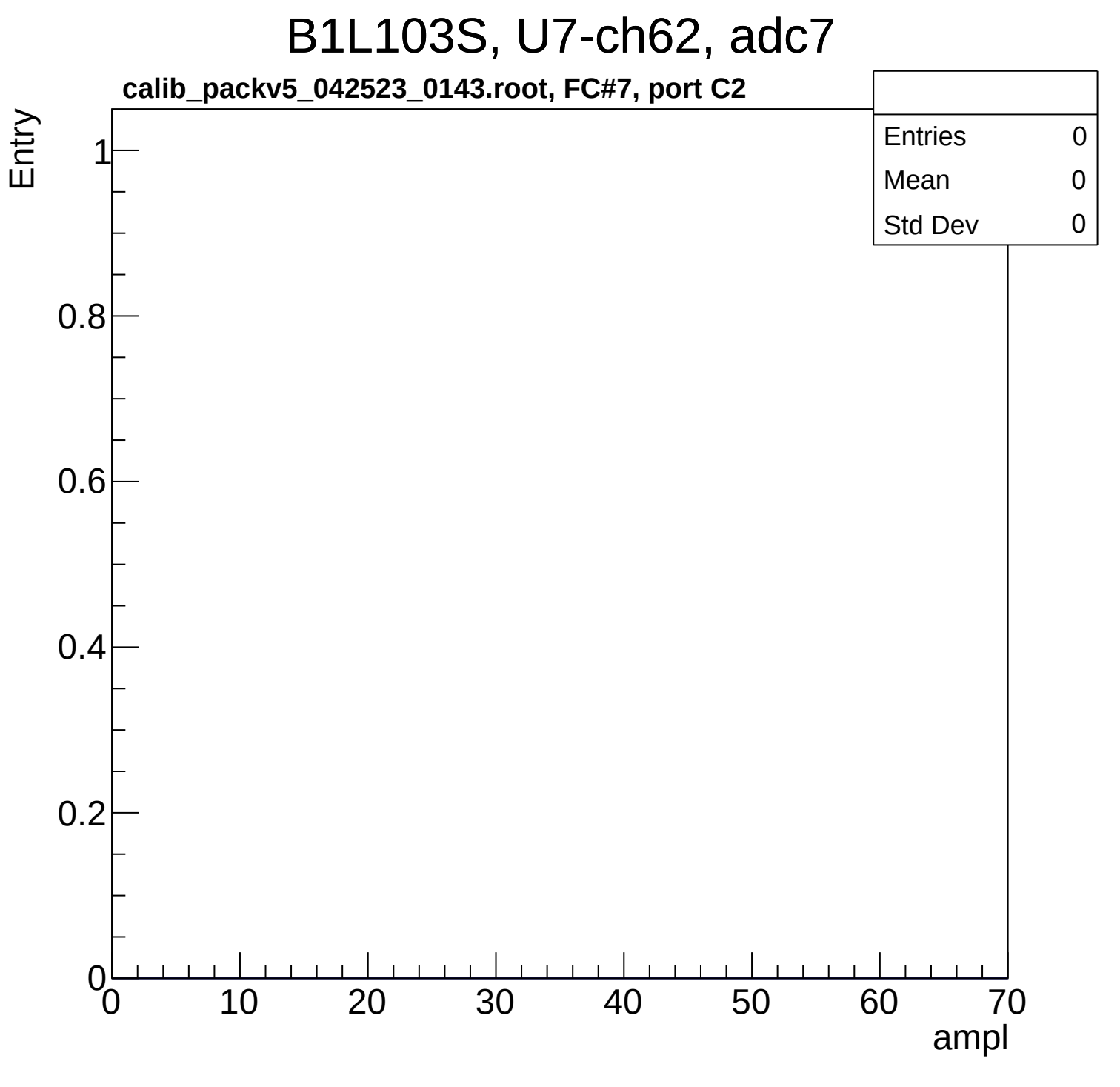
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U7-ch62, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
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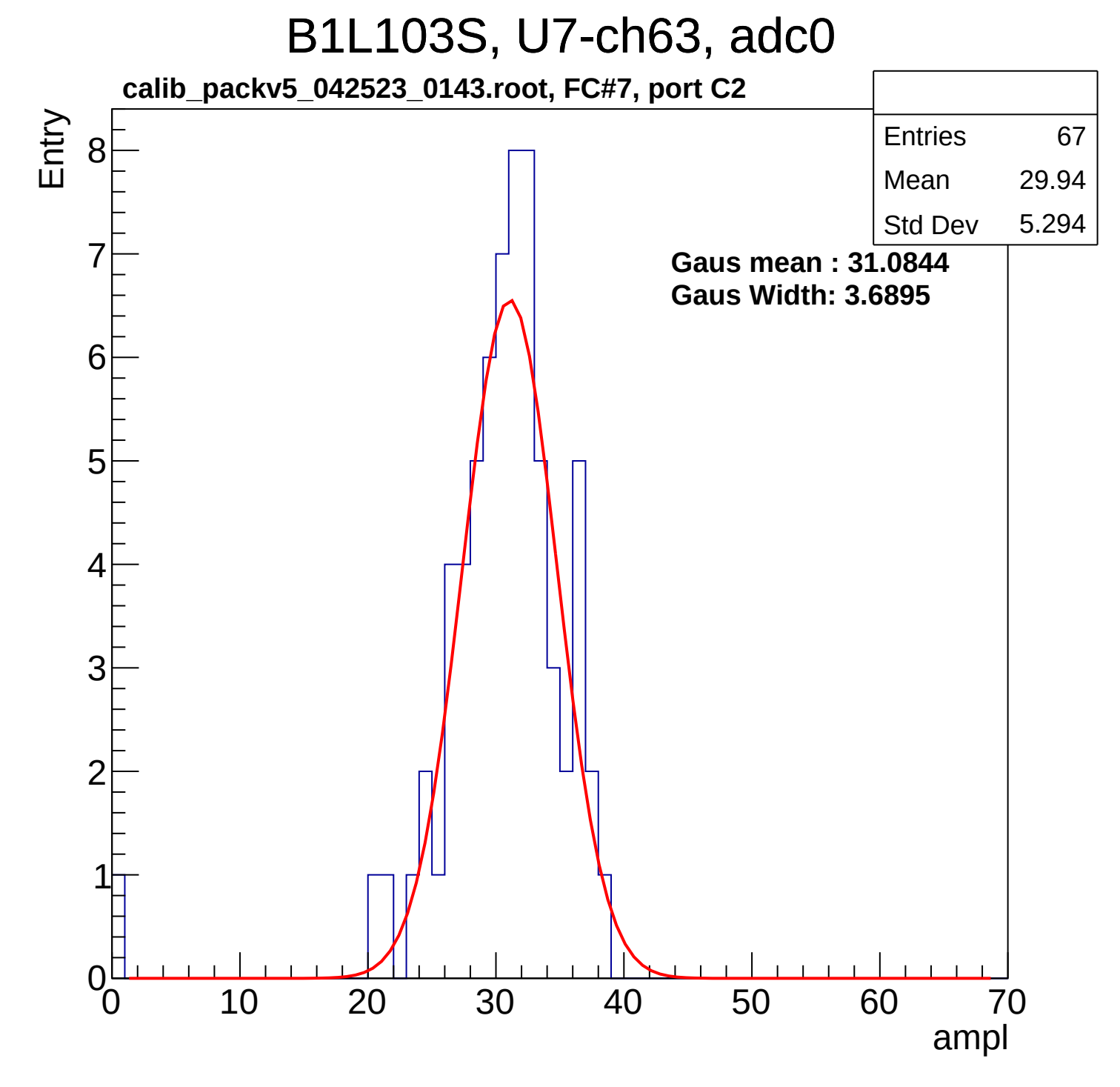
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch63, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 29.94
Std Dev 5.294
Gaus mean : 31.0844
Gaus Width: 3.6895
Entry
ampl
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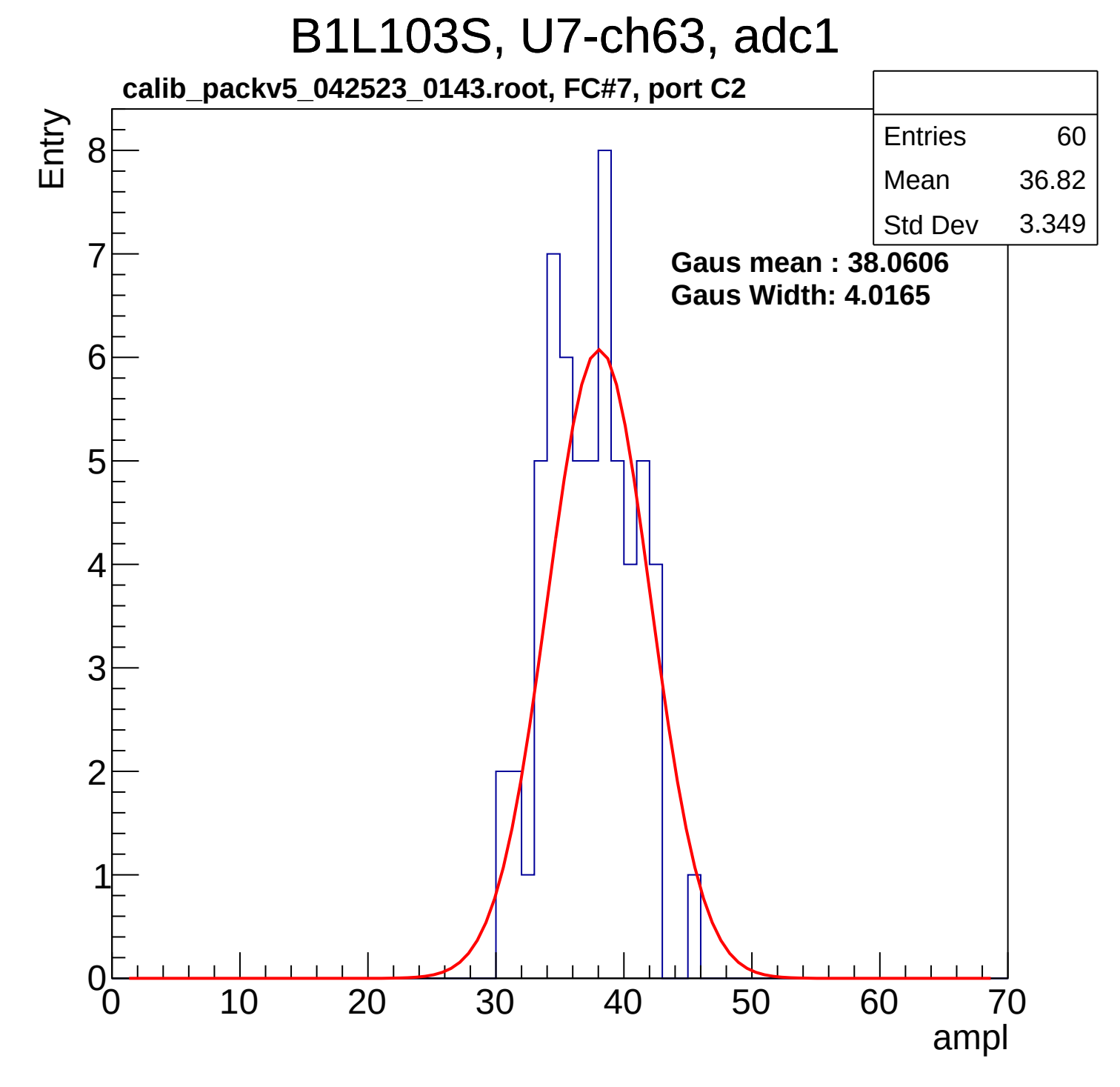
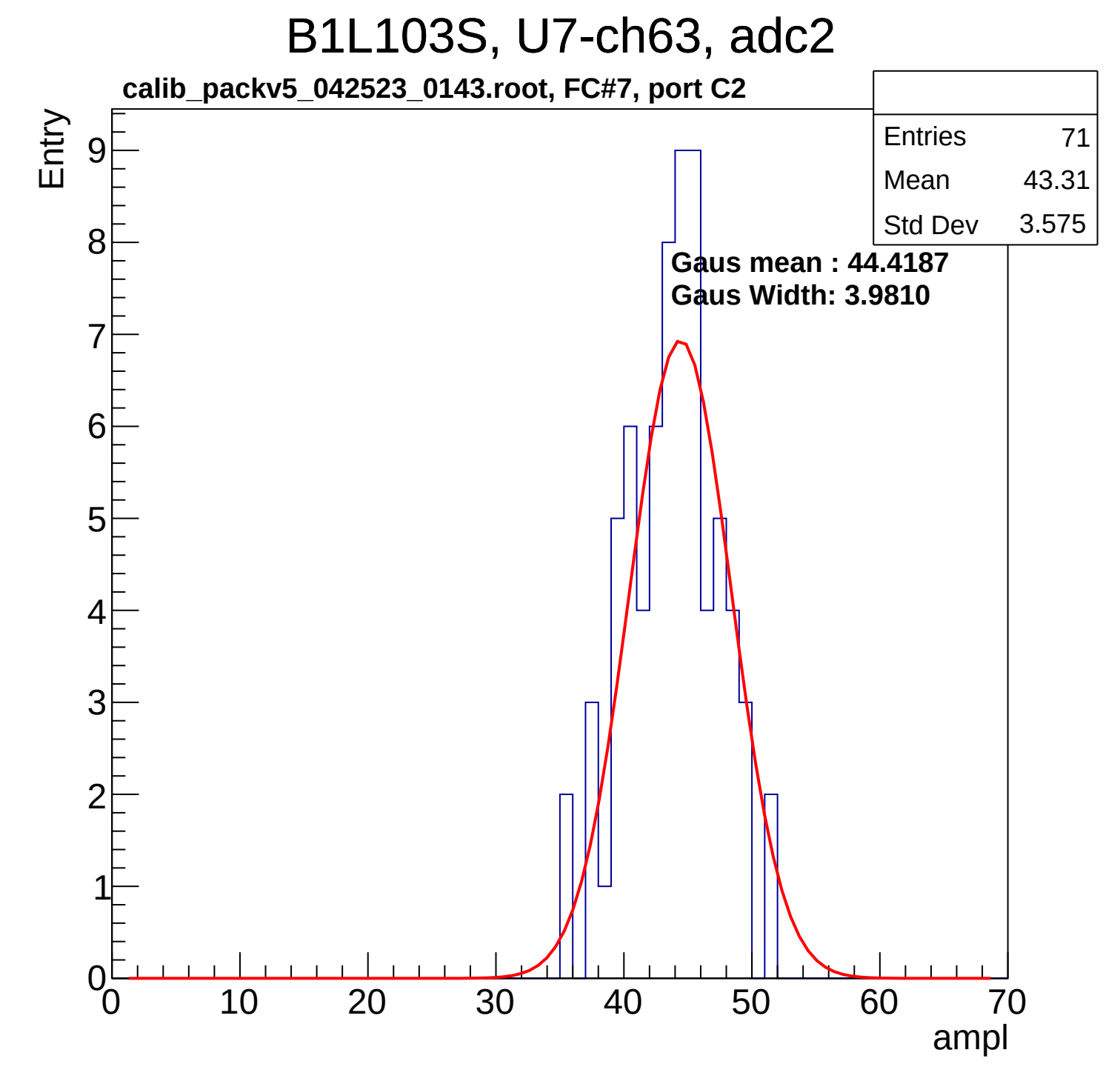
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch63, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 60
Mean 36.82
Std Dev 3.349
Gaus mean : 38.0606
Gaus Width: 4.0165
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch63, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 71
Mean 43.31
Std Dev 3.575
Gaus mean : 44.4187
Gaus Width: 3.9810
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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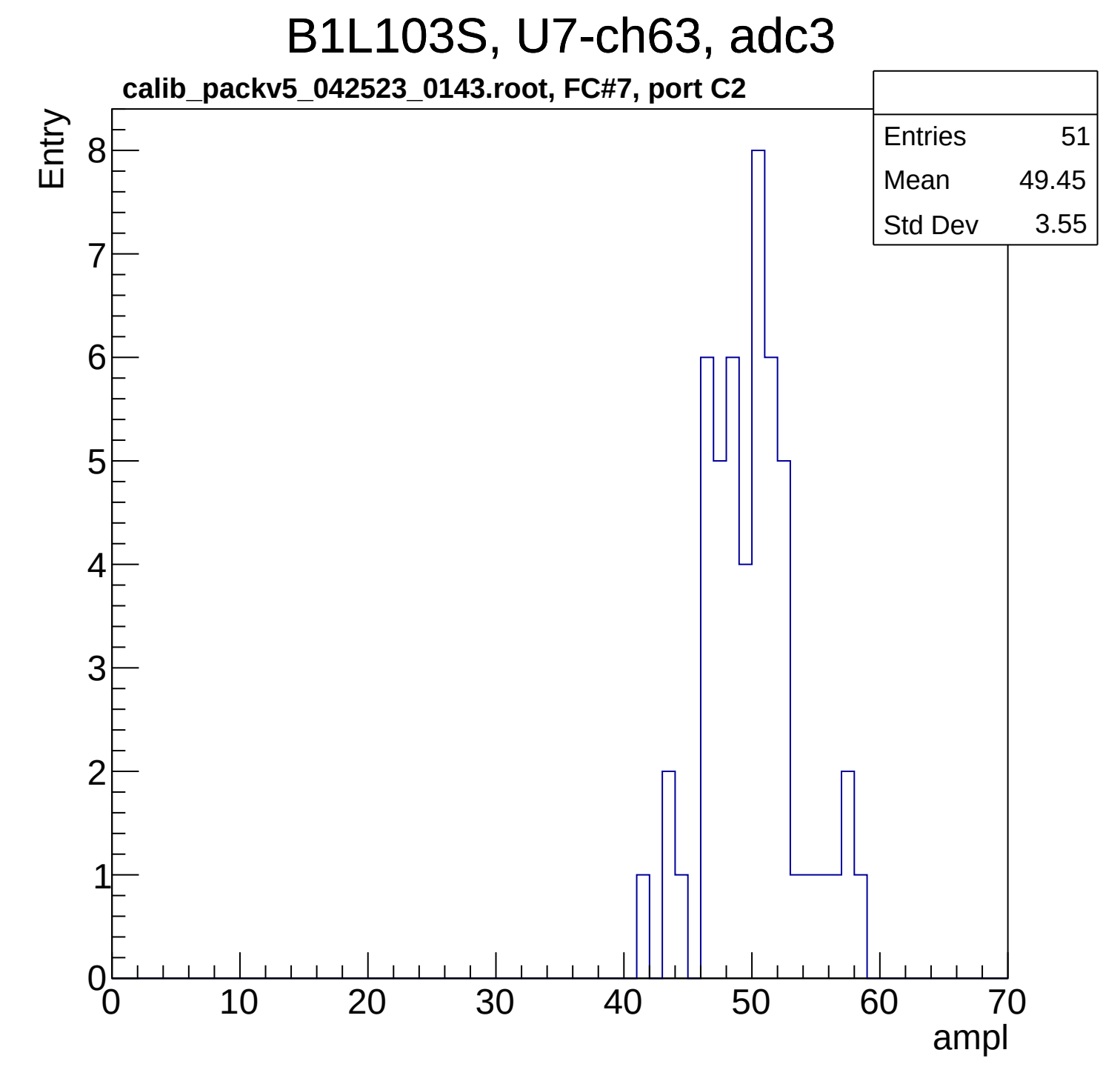
B1L103S, U7-ch63, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 51
Mean 49.45
Std Dev 3.55
Entry
ampl
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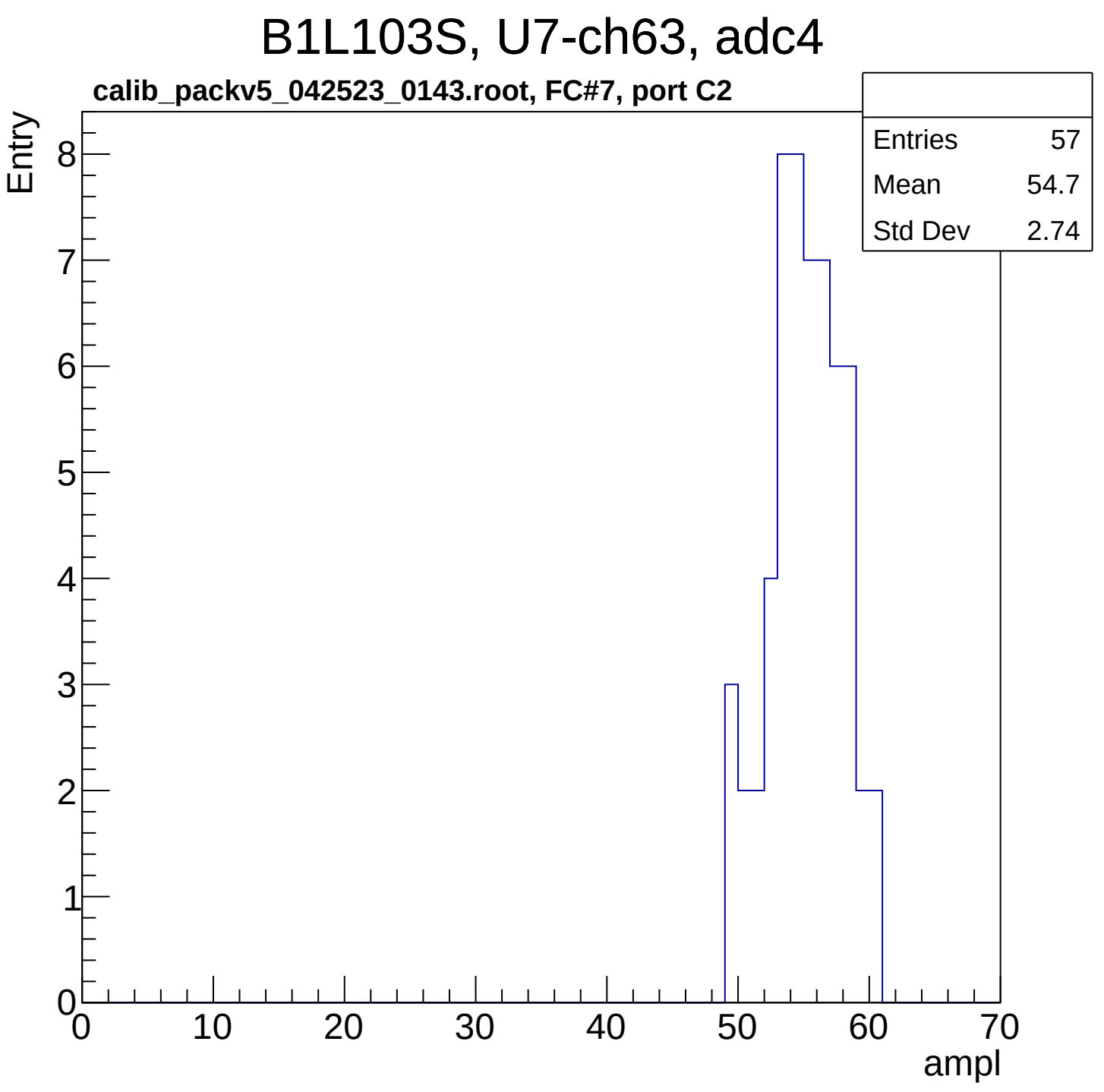
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch63, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 54.7
Std Dev 2.74
Entry
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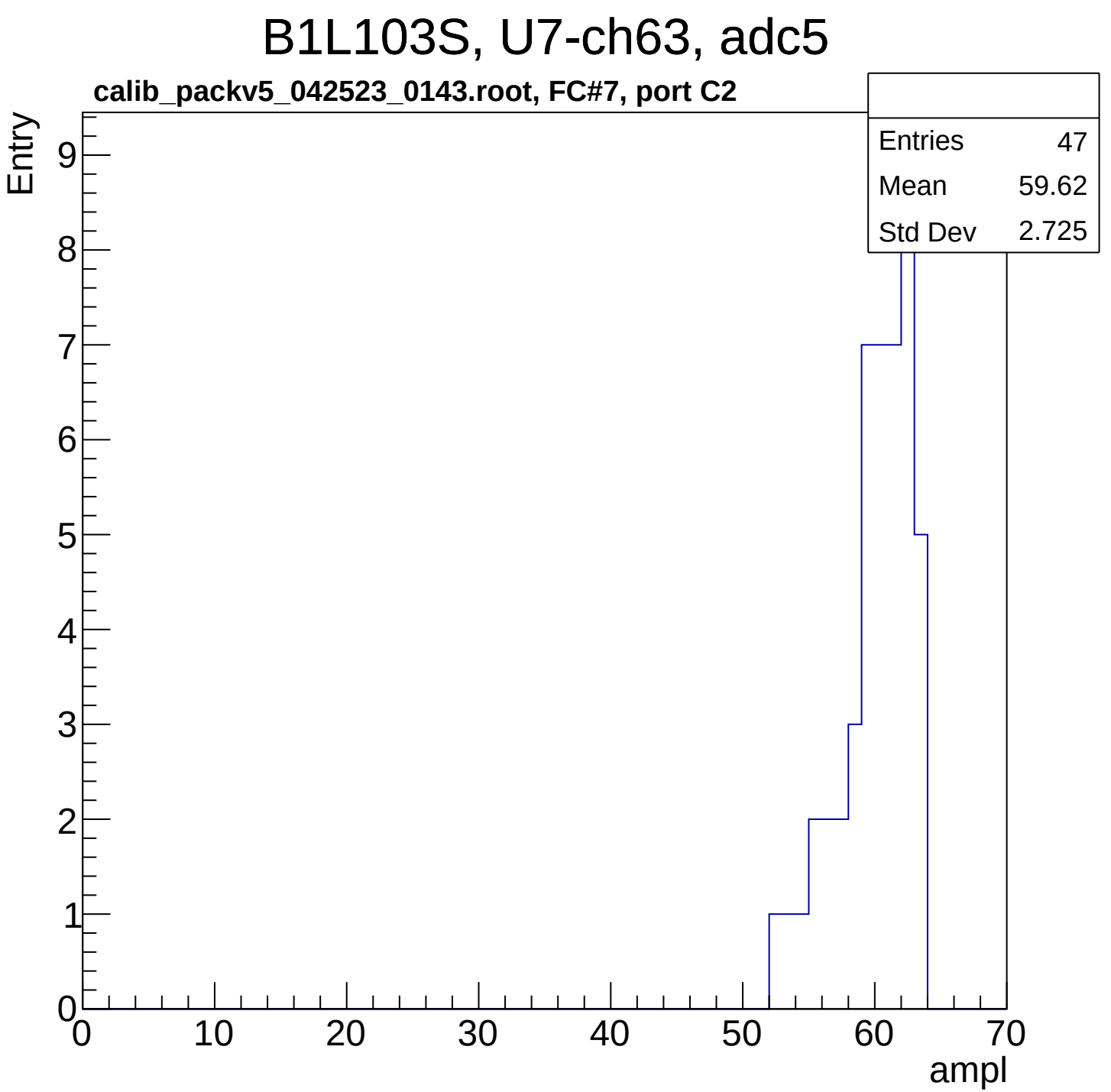
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch63, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 47
Mean 59.62
Std Dev 2.725
Entry
ampl
0
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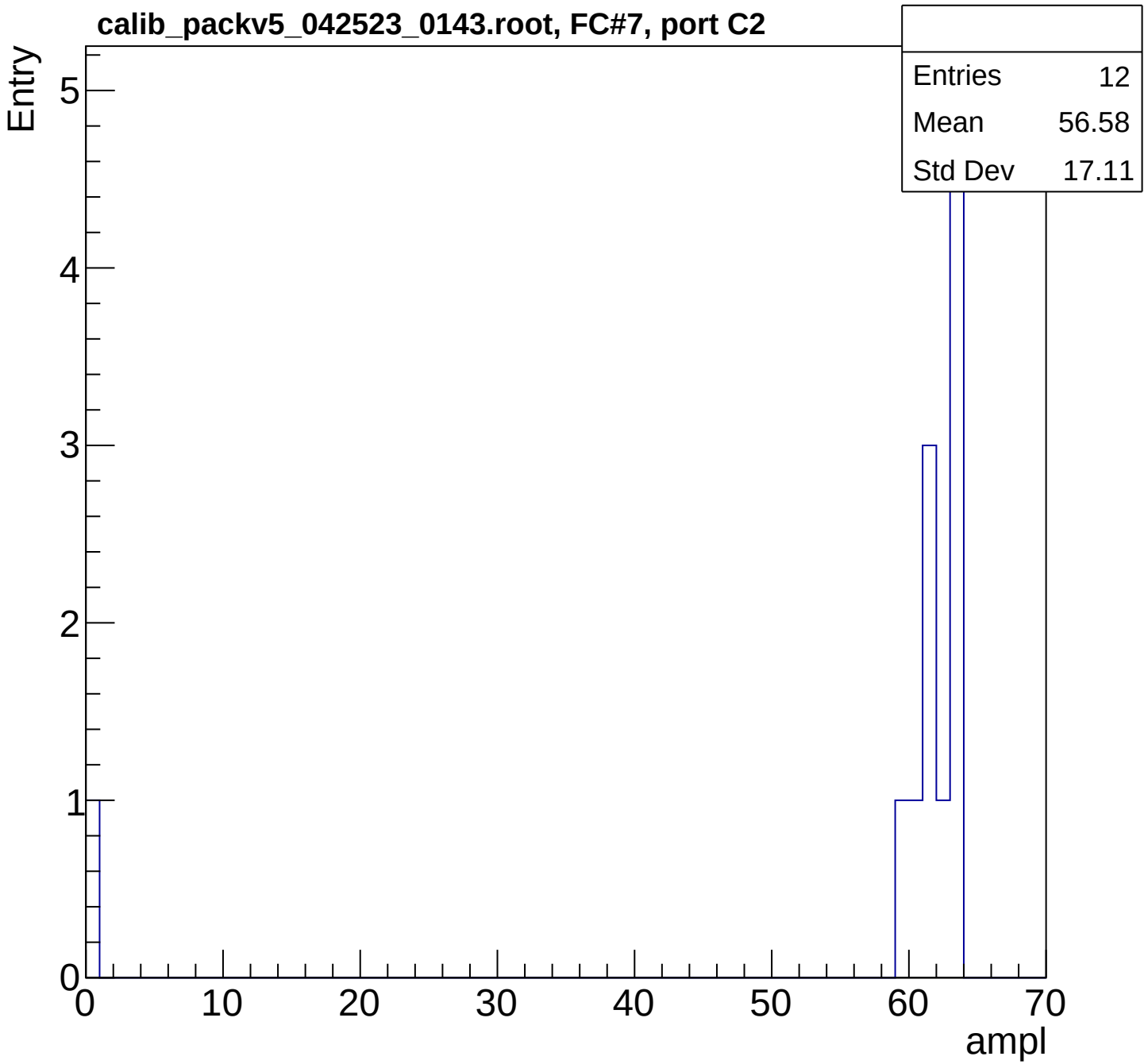
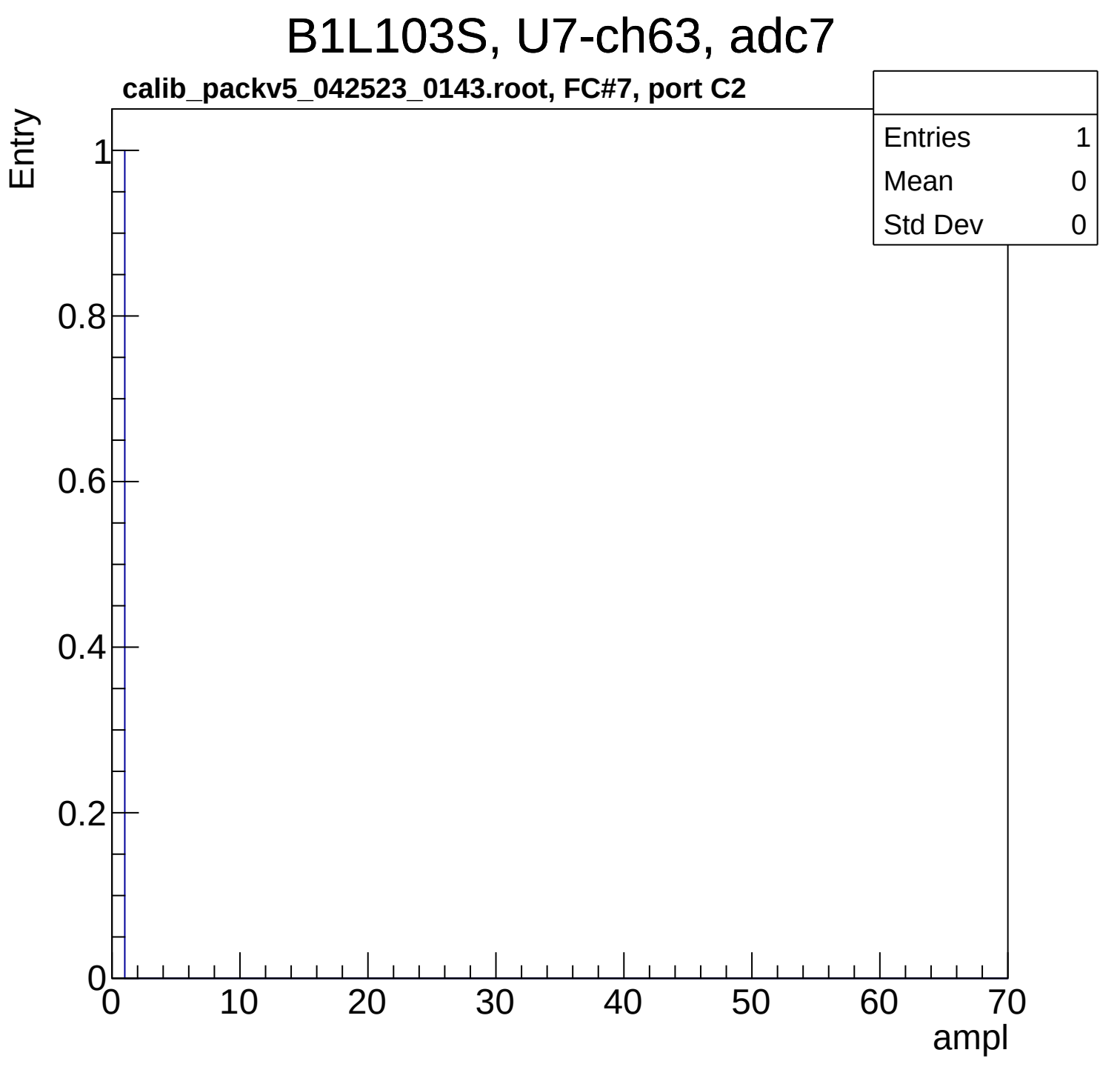
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch63, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 12
Mean 56.58
Std Dev 17.11
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch63, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
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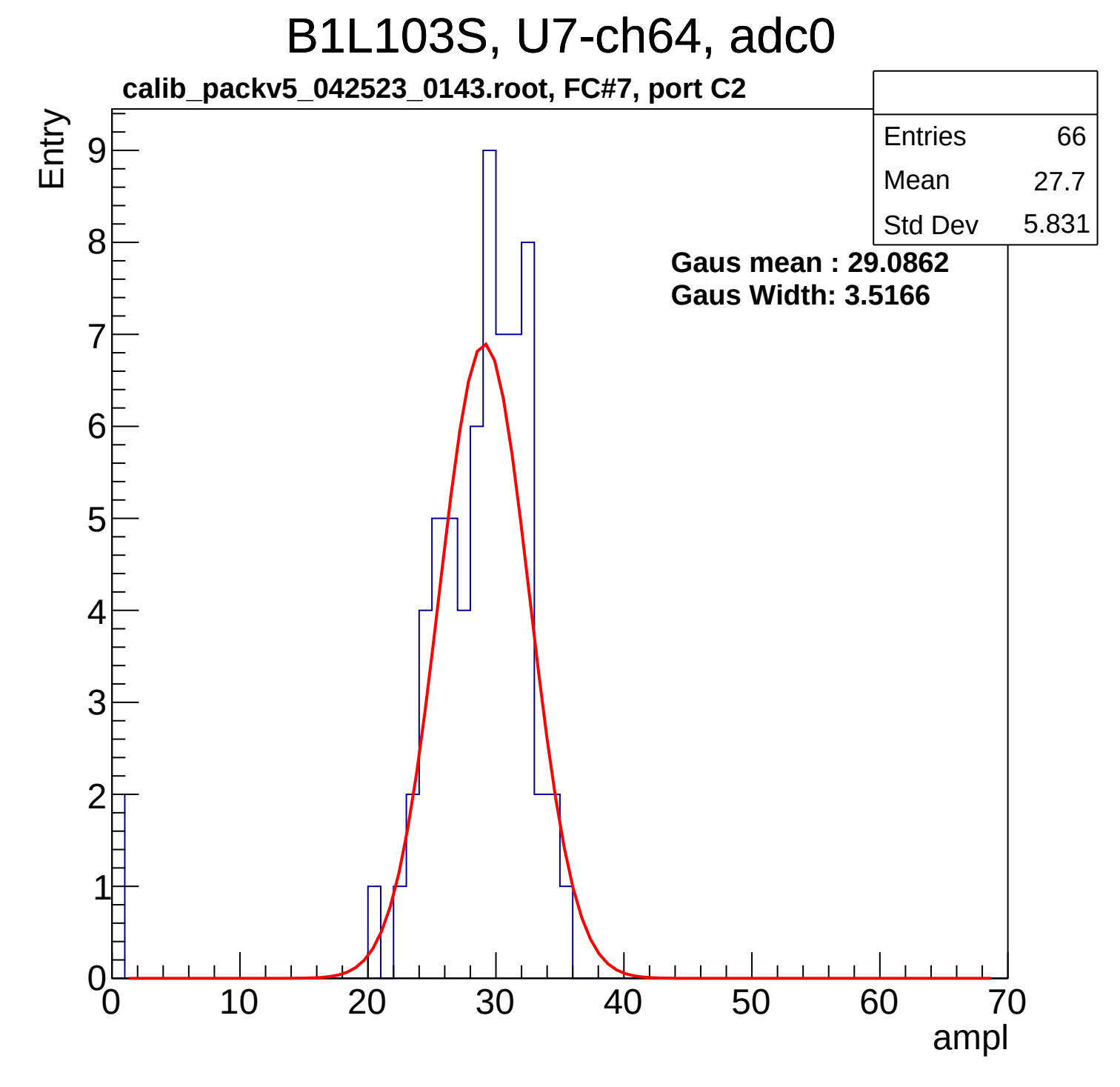
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch64, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 27.7
Std Dev 5.831
Gaus mean : 29.0862
Gaus Width: 3.5166
Entry
ampl
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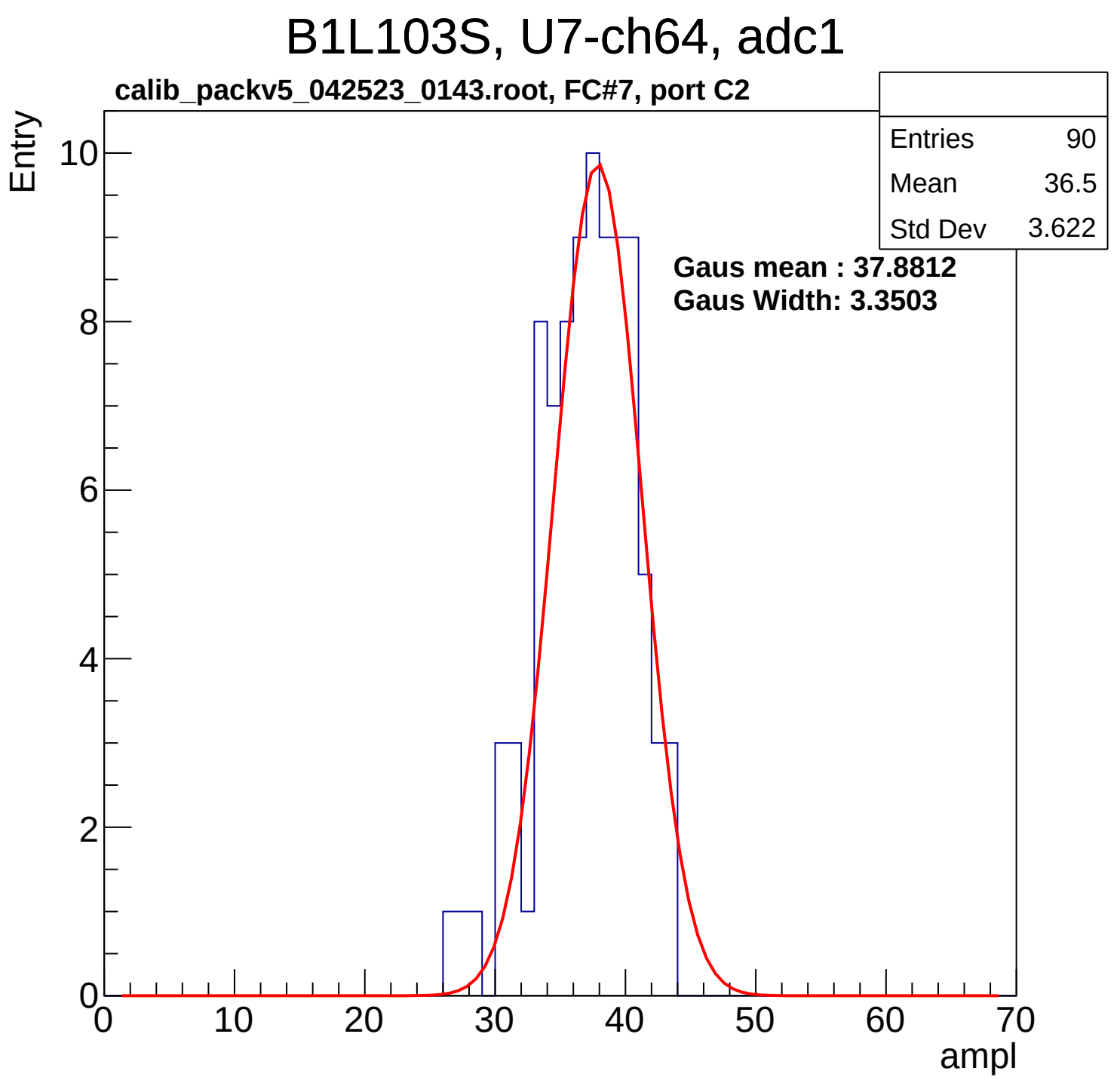
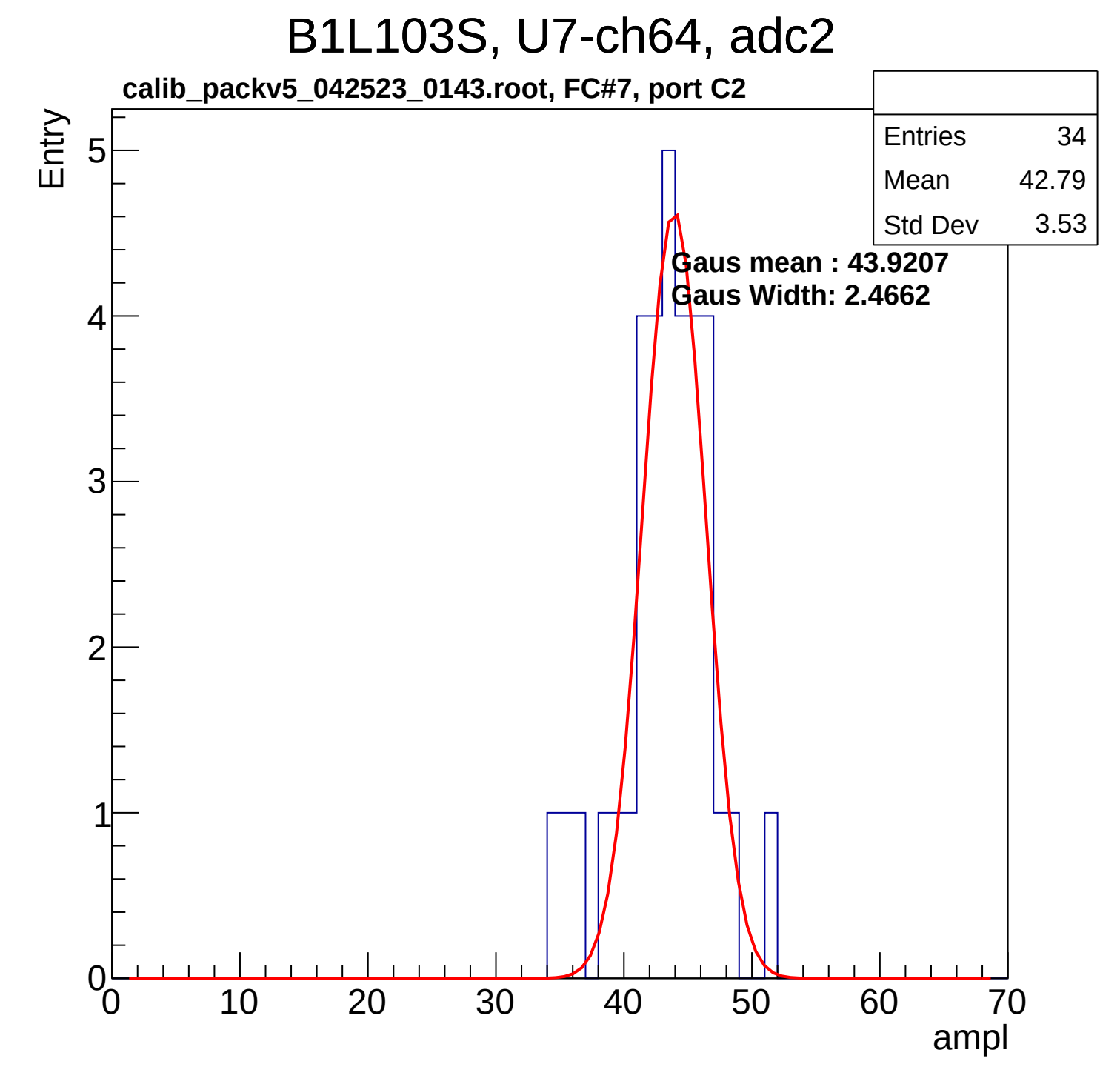
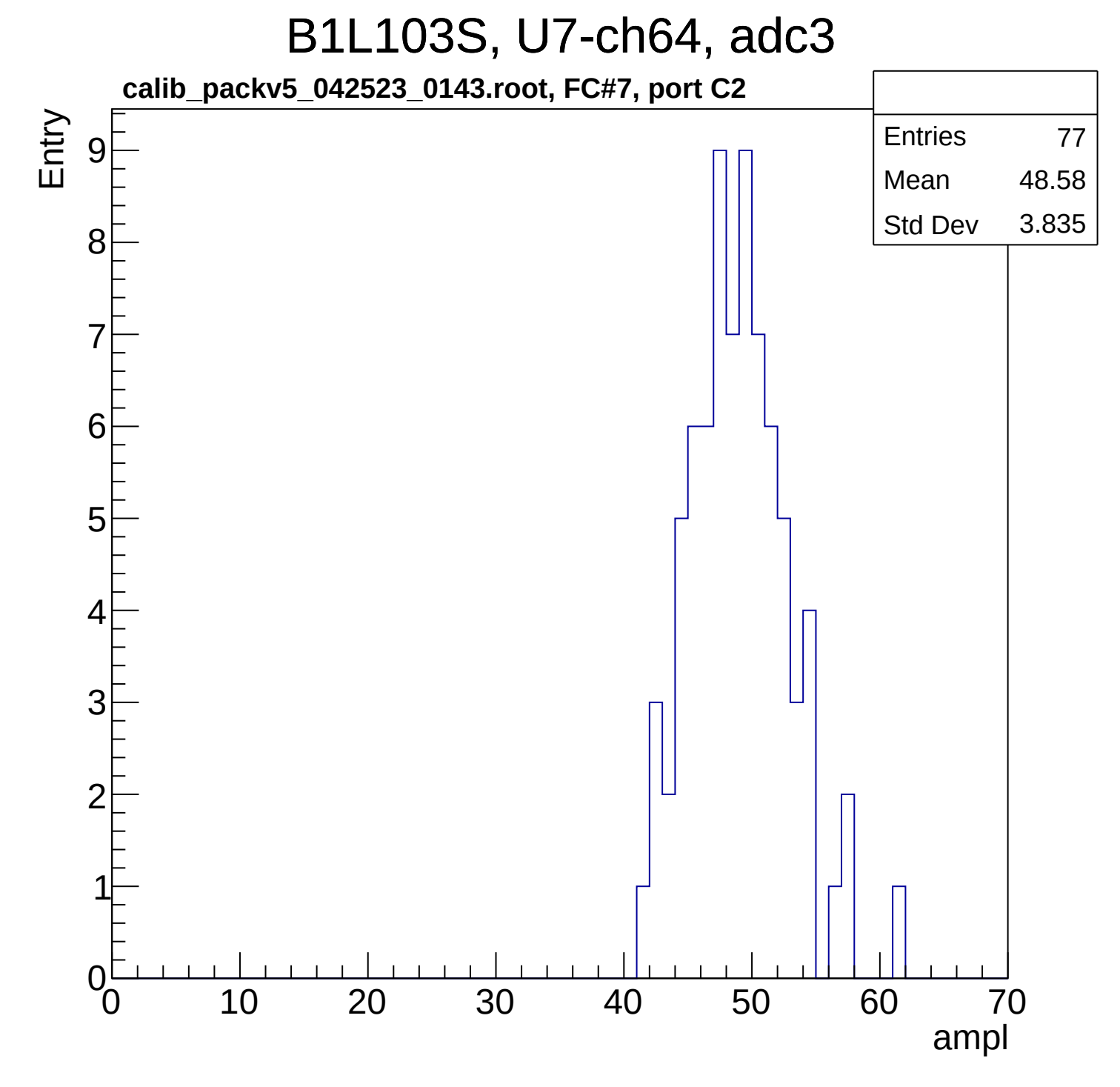
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch64, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 90
Mean 36.5
Std Dev 3.622
Gaus mean : 37.8812
Gaus Width: 3.3503
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch64, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 34
Mean 42.79
Std Dev 3.53
Gaus mean : 43.9207
Gaus Width: 2.4662
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U7-ch64, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 77
Mean 48.58
Std Dev 3.835
Entry
ampl
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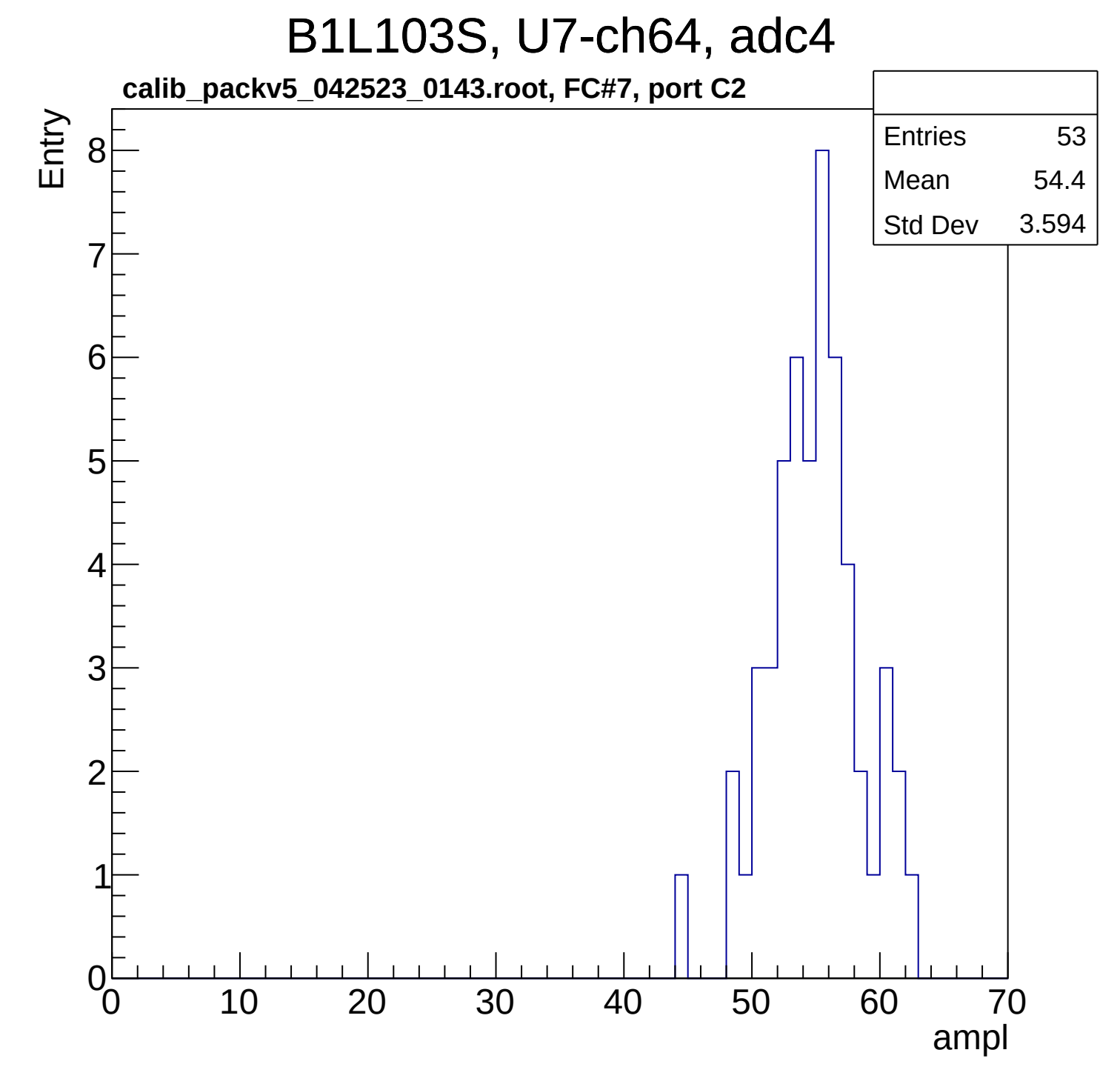
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch64, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 54.4
Std Dev 3.594
Entry
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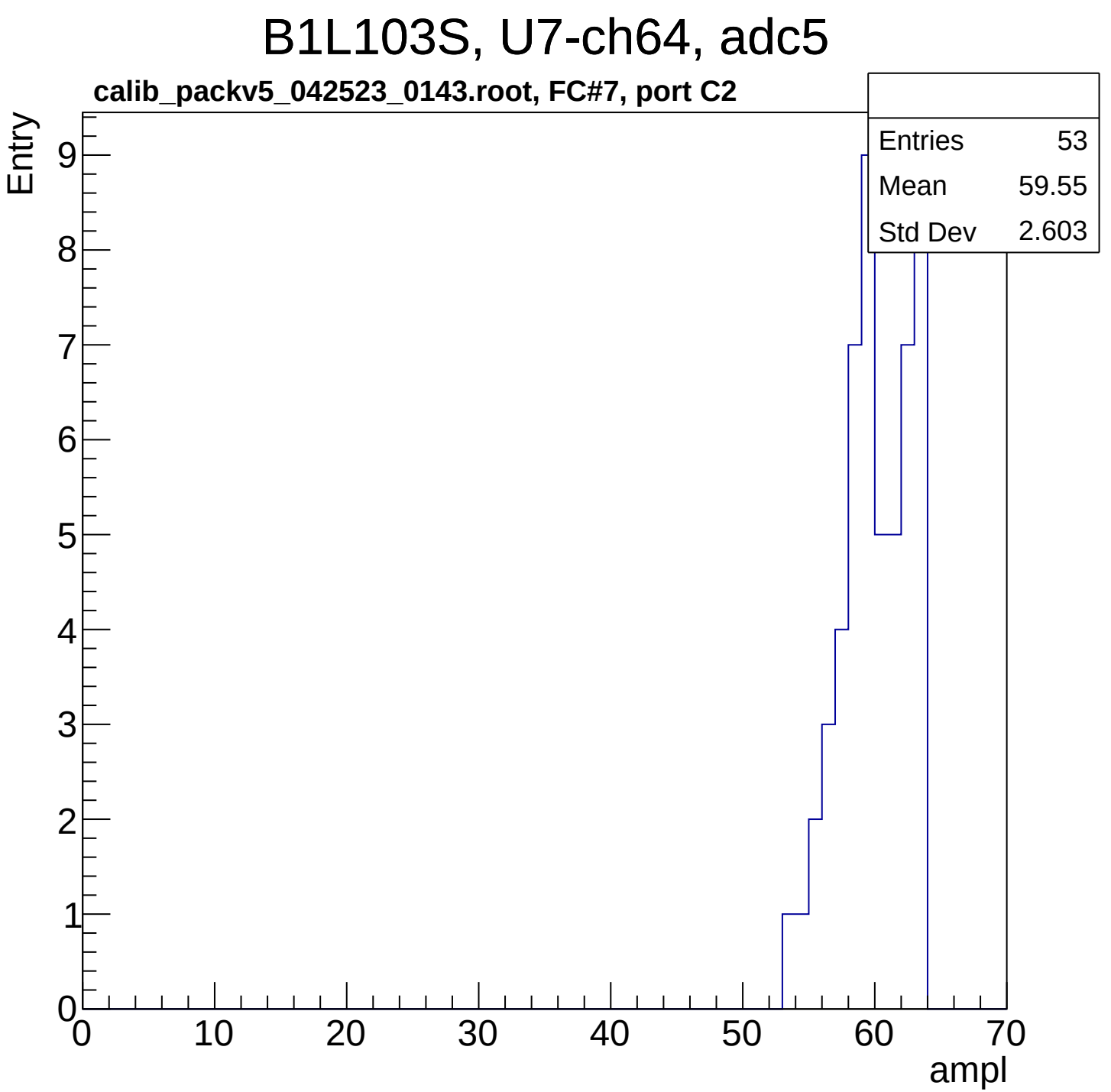
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch64, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 59.55
Std Dev 2.603
Entry
ampl
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2
3
4
5
6
7
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9
0
10
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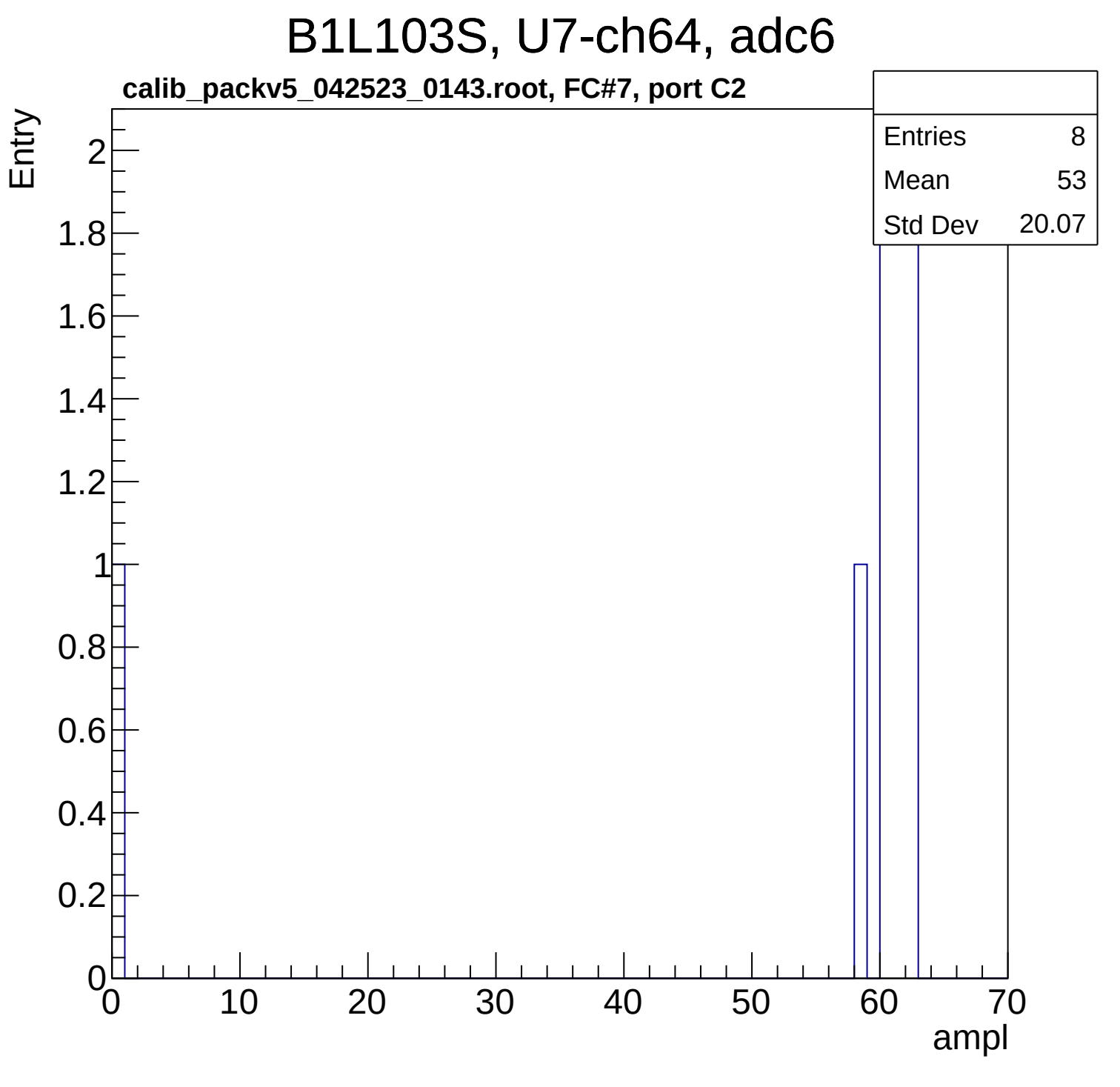
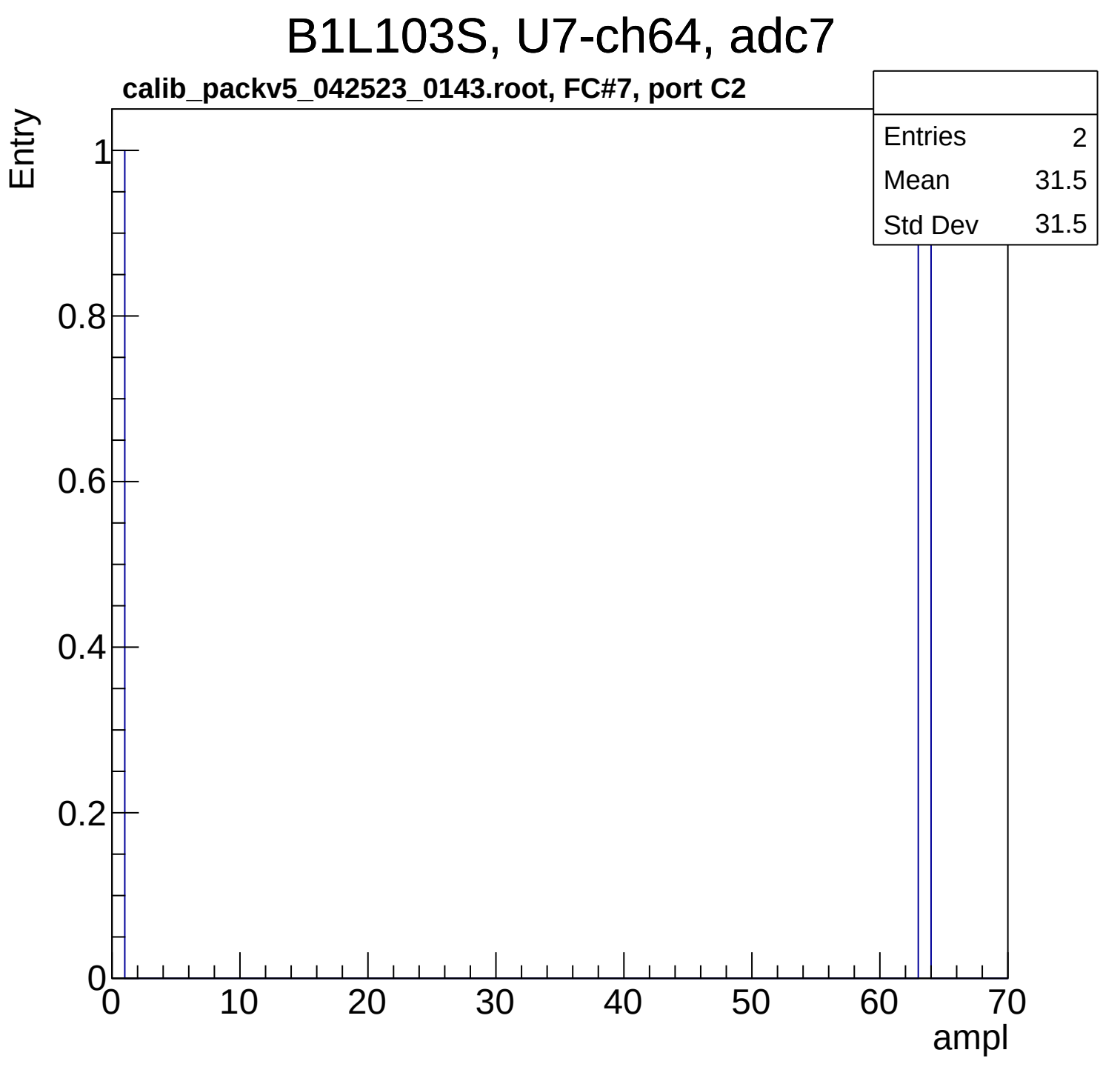
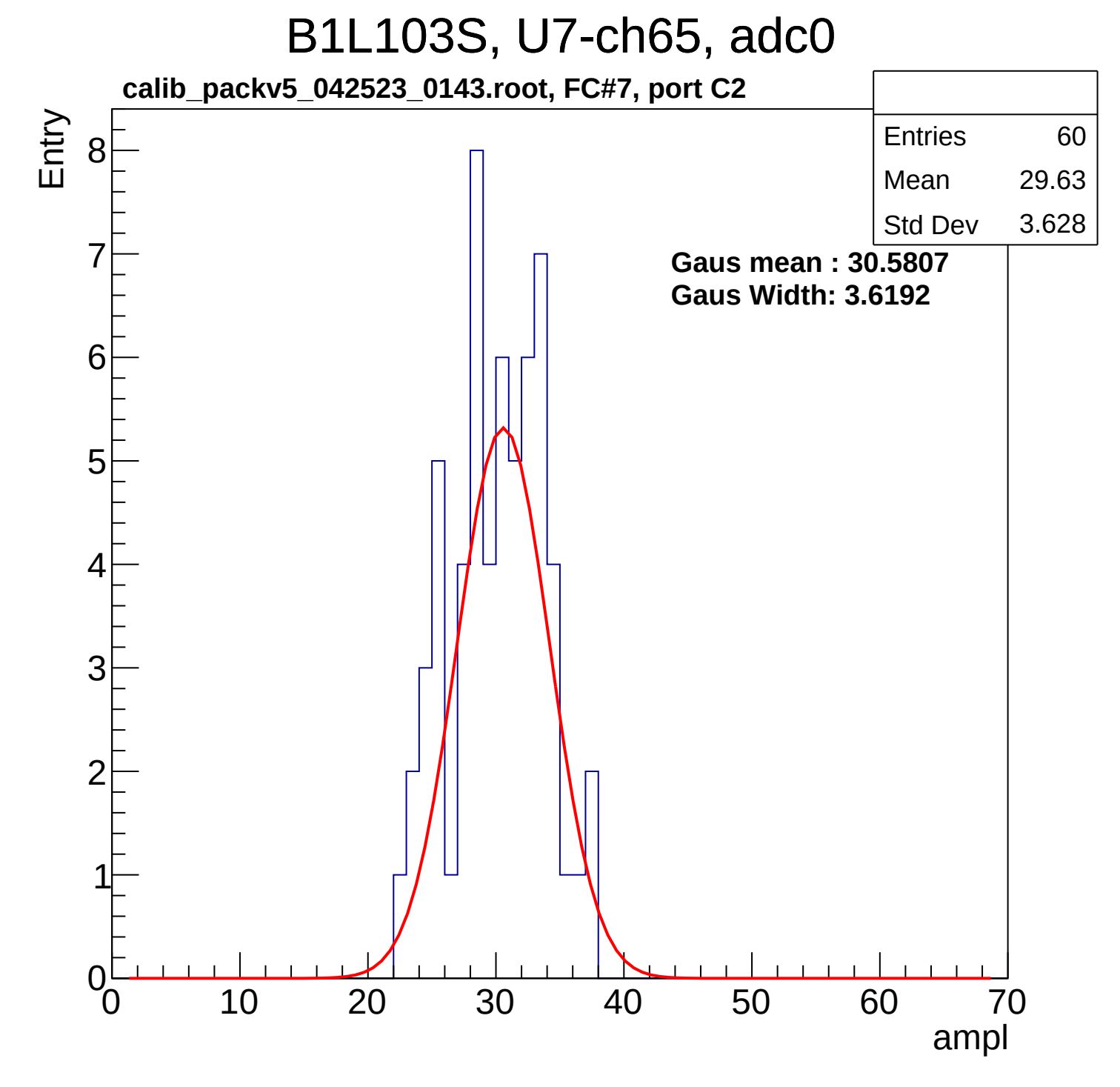
40
50
60
70


B1L103S, U7-ch64, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 8
Mean 53
Std Dev 20.07
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U7-ch64, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 31.5
Std Dev 31.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch65, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 60
Mean 29.63
Std Dev 3.628
Gaus mean : 30.5807
Gaus Width: 3.6192
Entry
ampl
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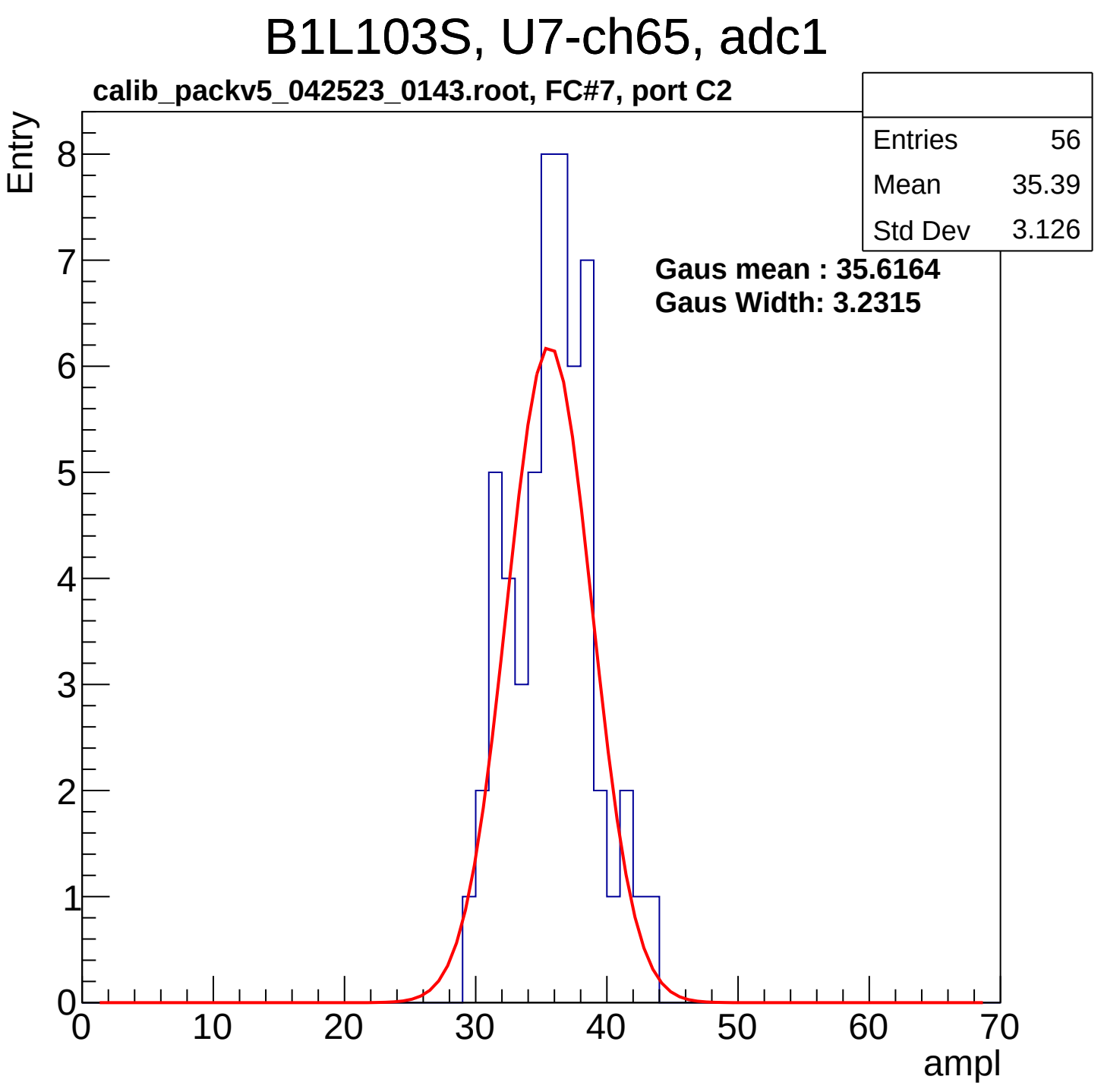
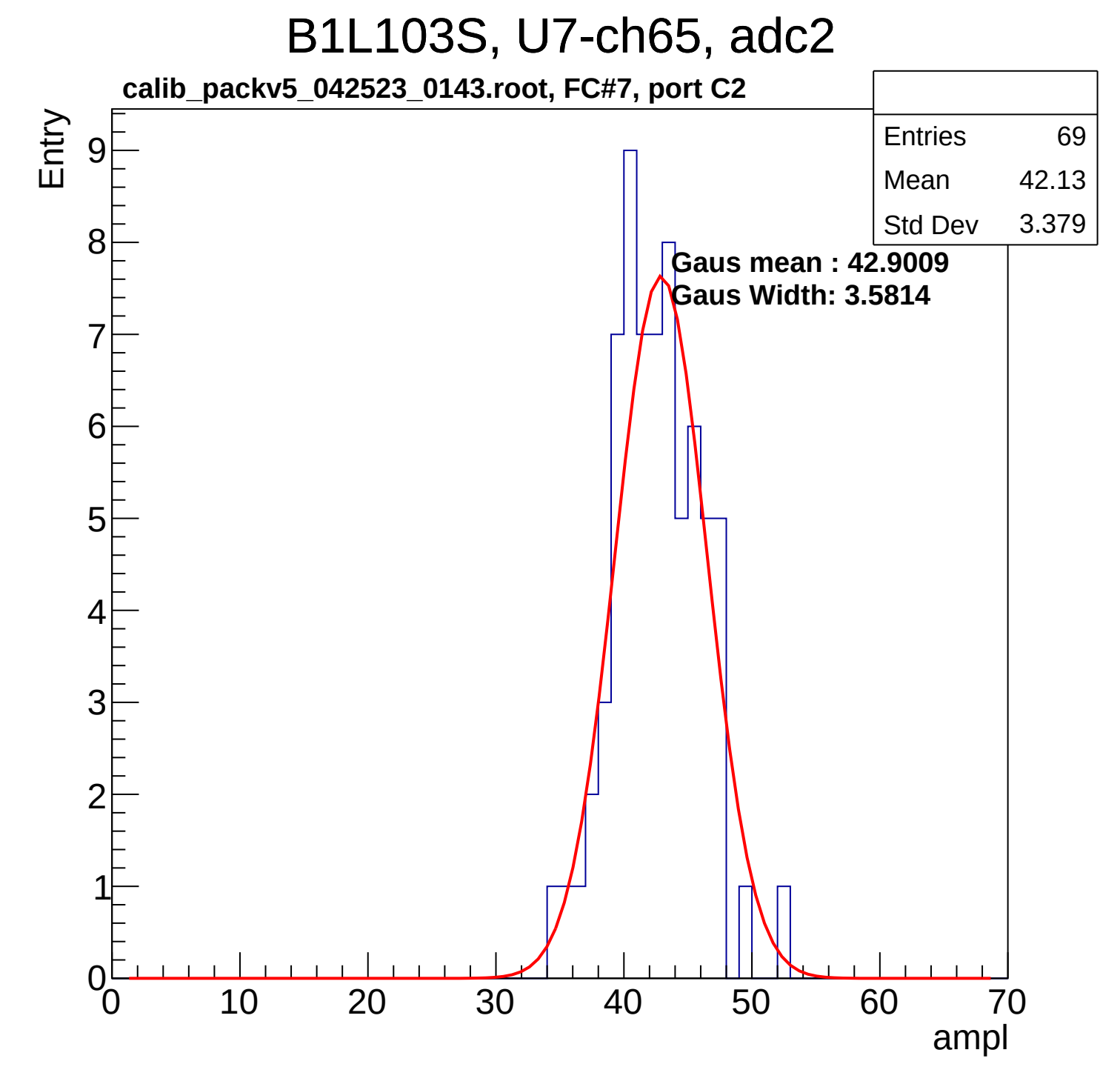
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch65, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 35.39
Std Dev 3.126
Gaus mean : 35.6164
Gaus Width: 3.2315
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch65, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 42.13
Std Dev 3.379
Gaus mean : 42.9009
Gaus Width: 3.5814
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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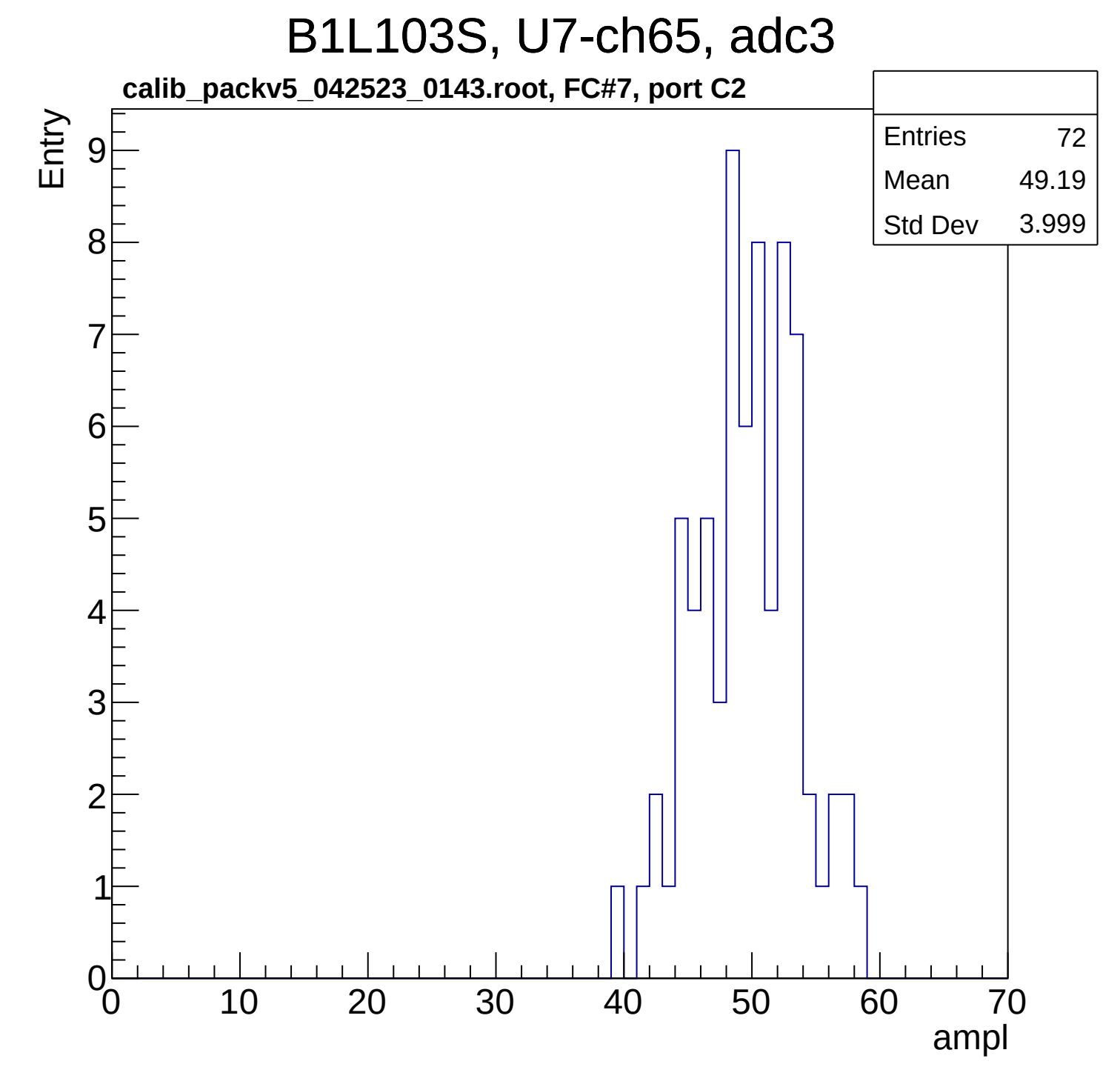
B1L103S, U7-ch65, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 72
Mean 49.19
Std Dev 3.999
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
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60
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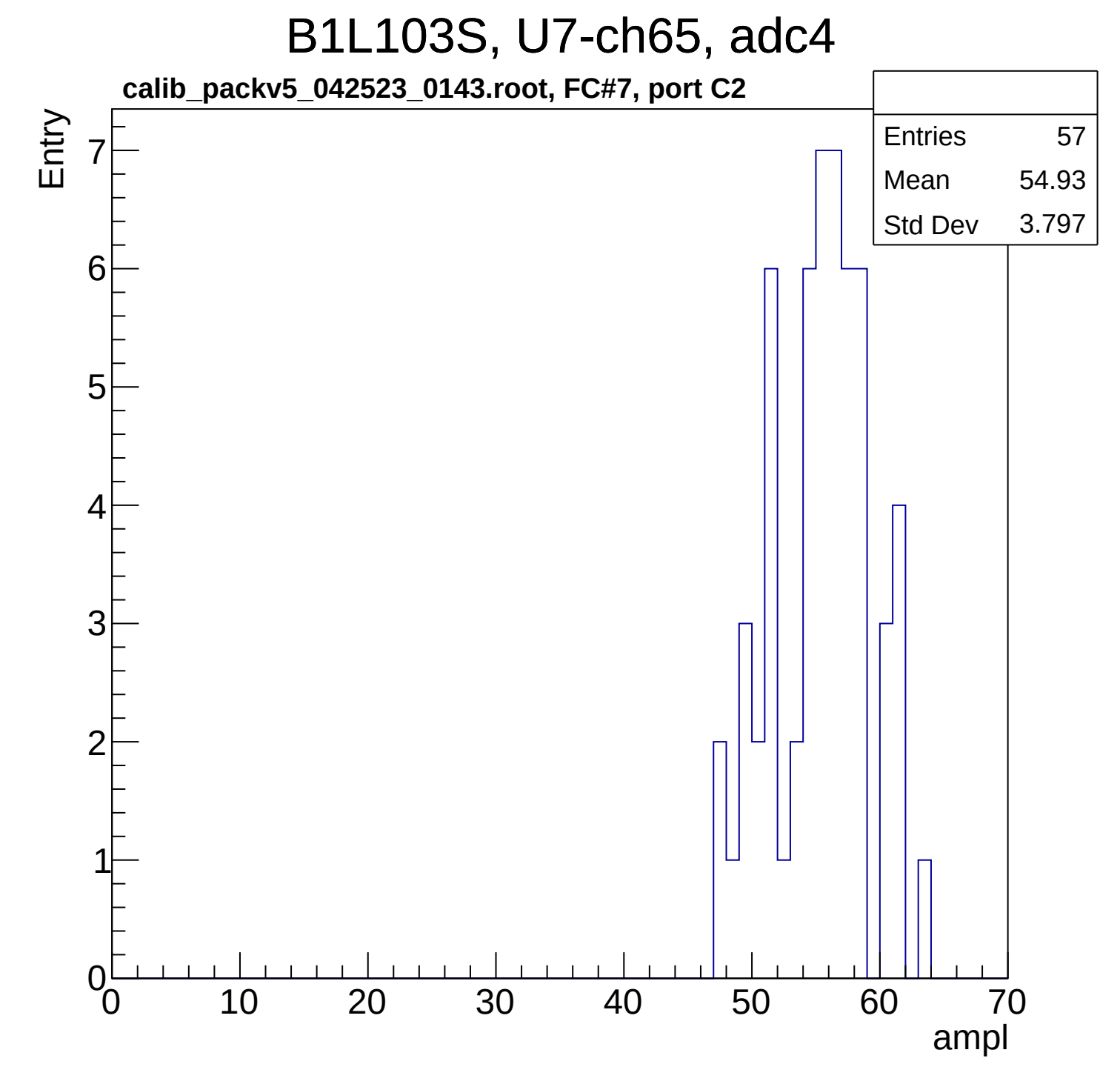
B1L103S, U7-ch65, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 54.93
Std Dev 3.797
Entry
ampl
0
1
2
3
4
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6
7
0
10
20
30
40
50
60
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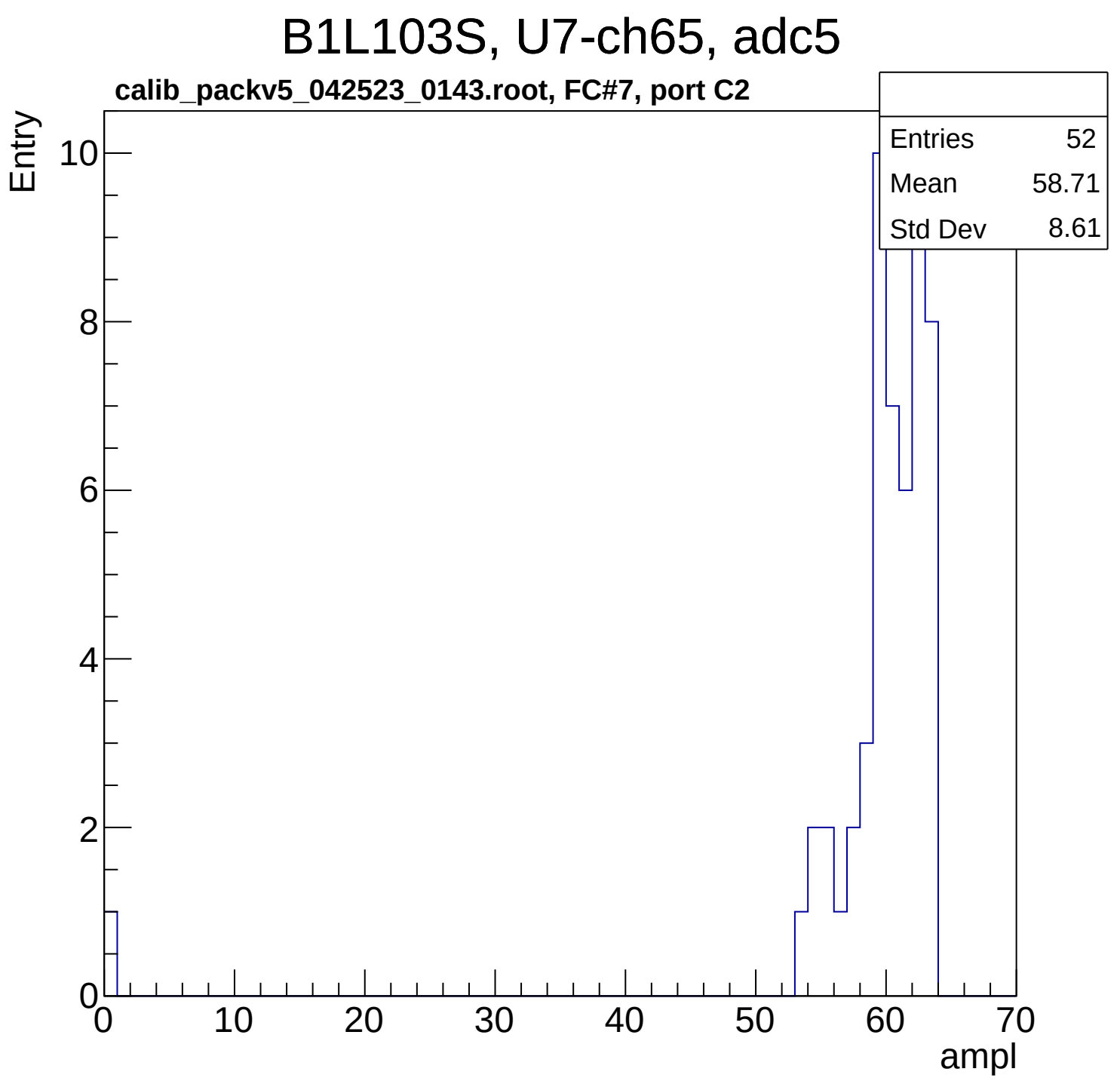
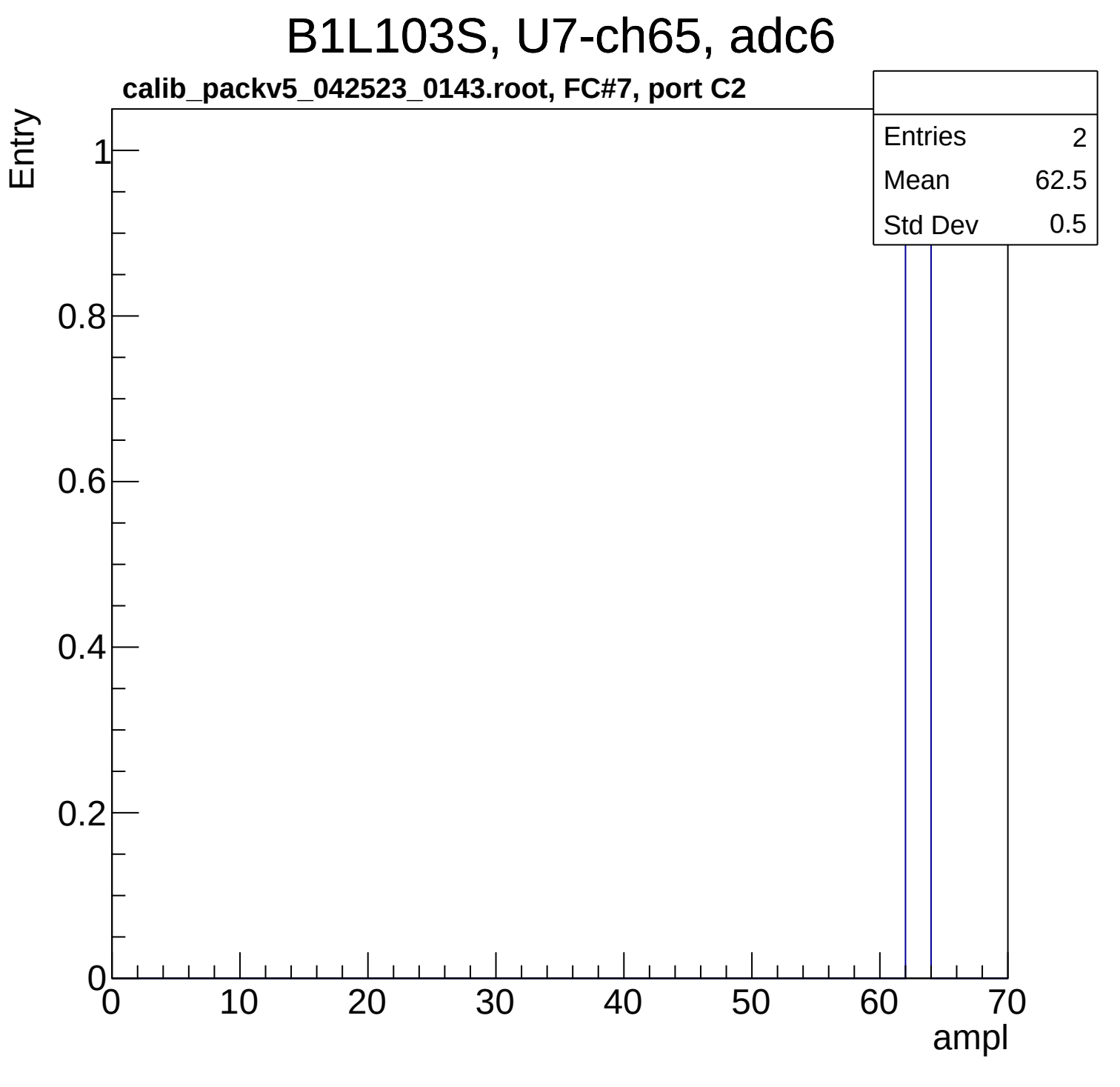
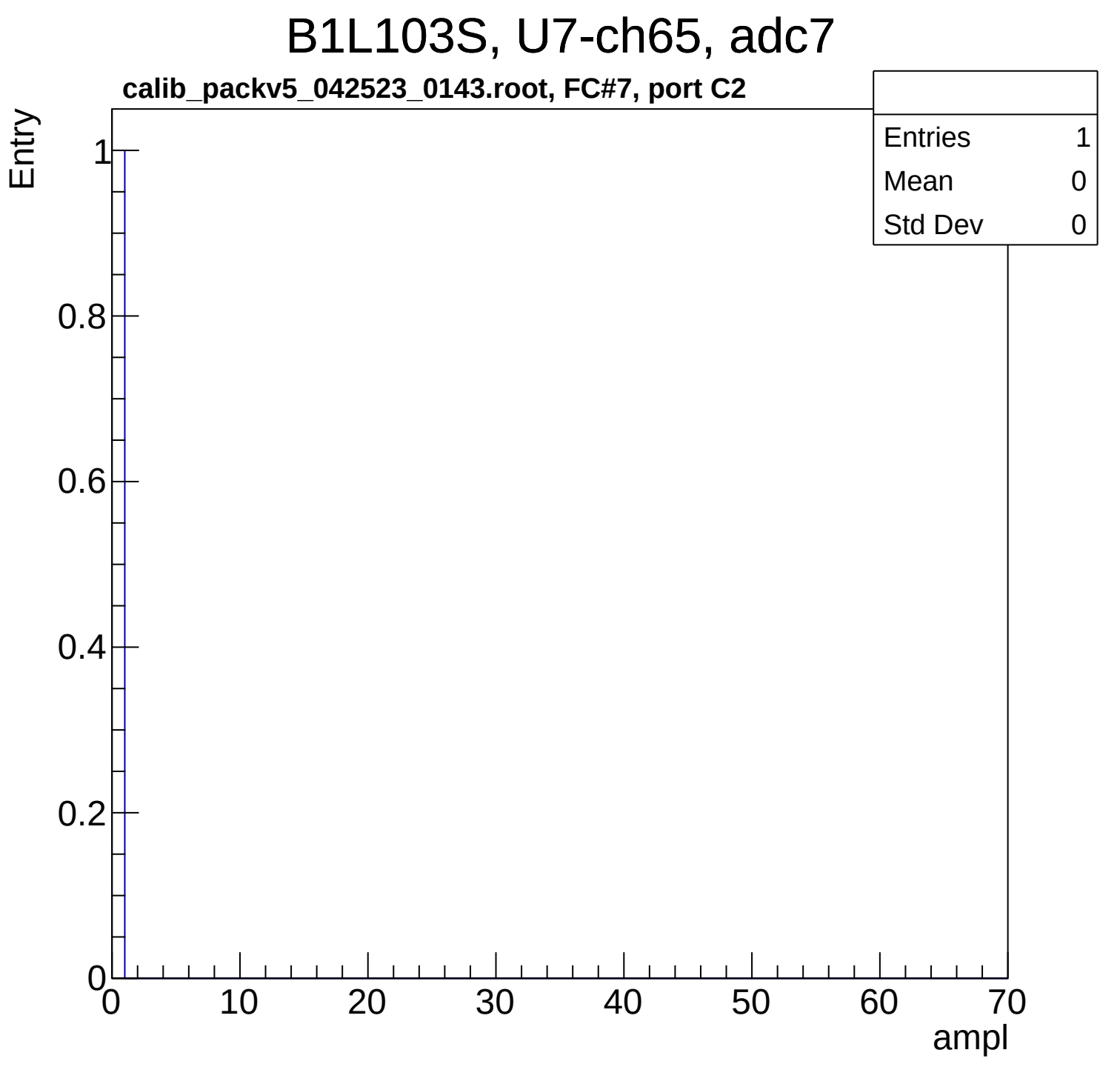

B1L103S, U7-ch65, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 52
Mean 58.71
Std Dev 8.61
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch65, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch65, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
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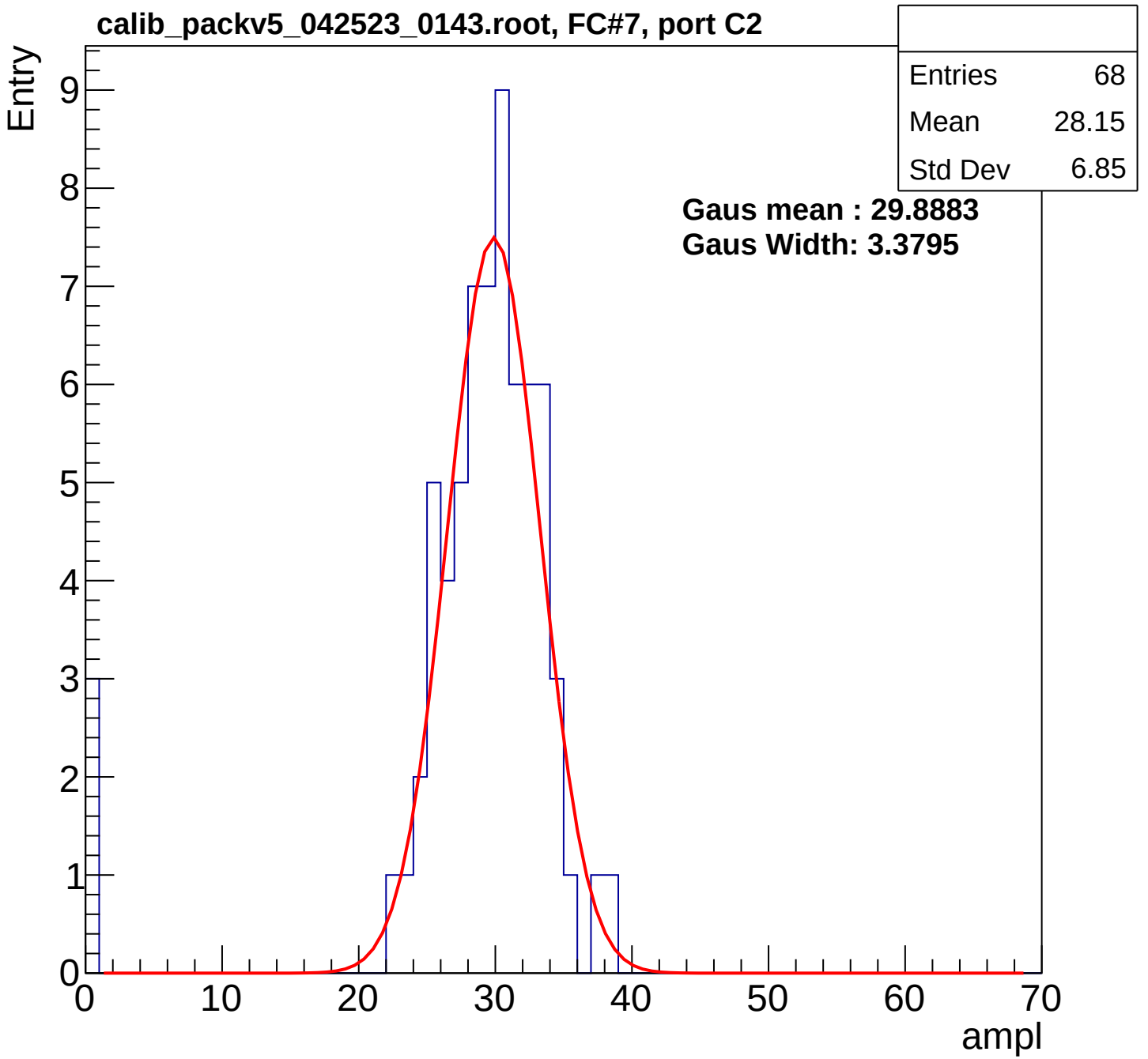
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch66, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 28.15
Std Dev 6.85
Gaus mean : 29.8883
Gaus Width: 3.3795
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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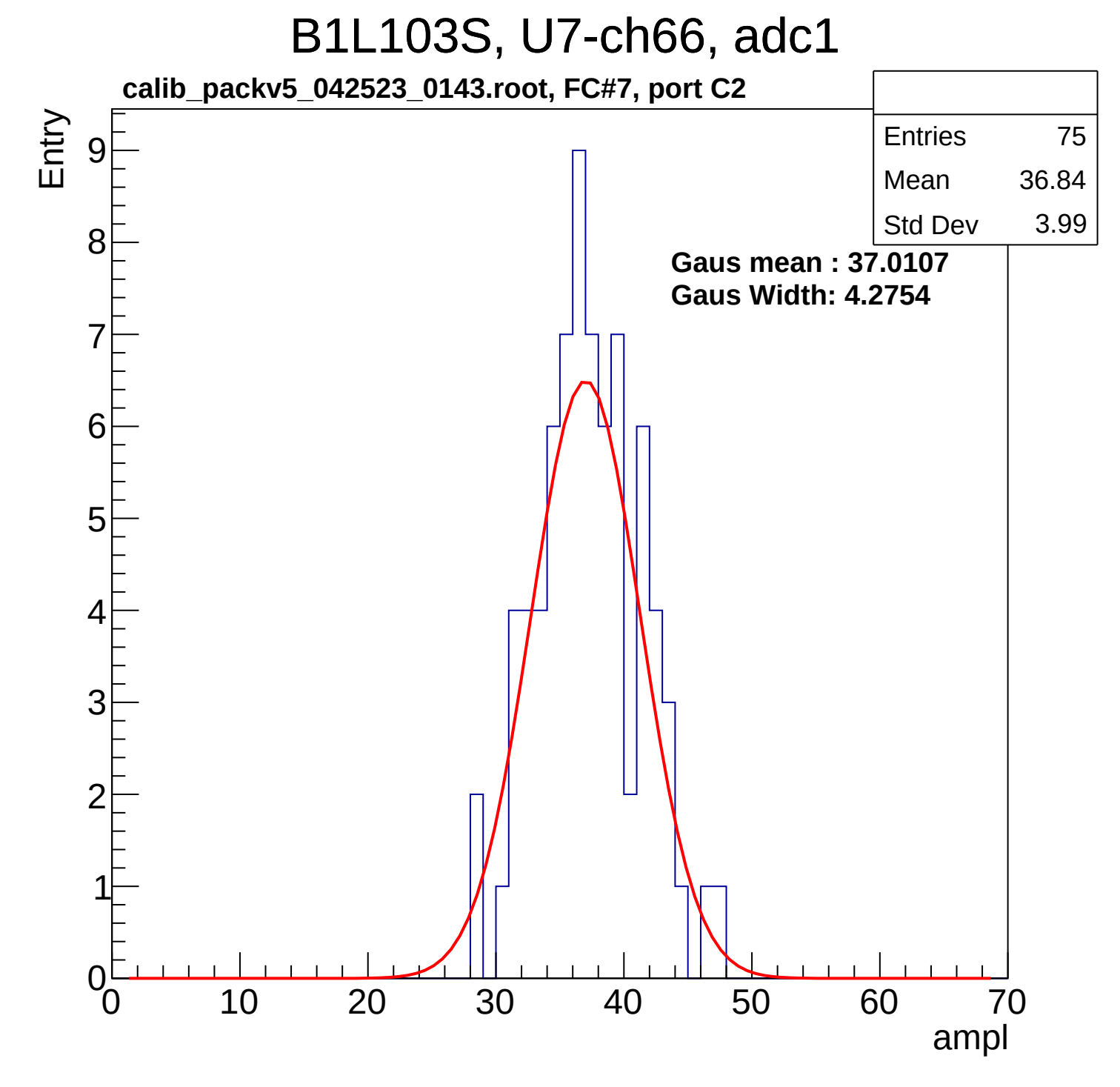
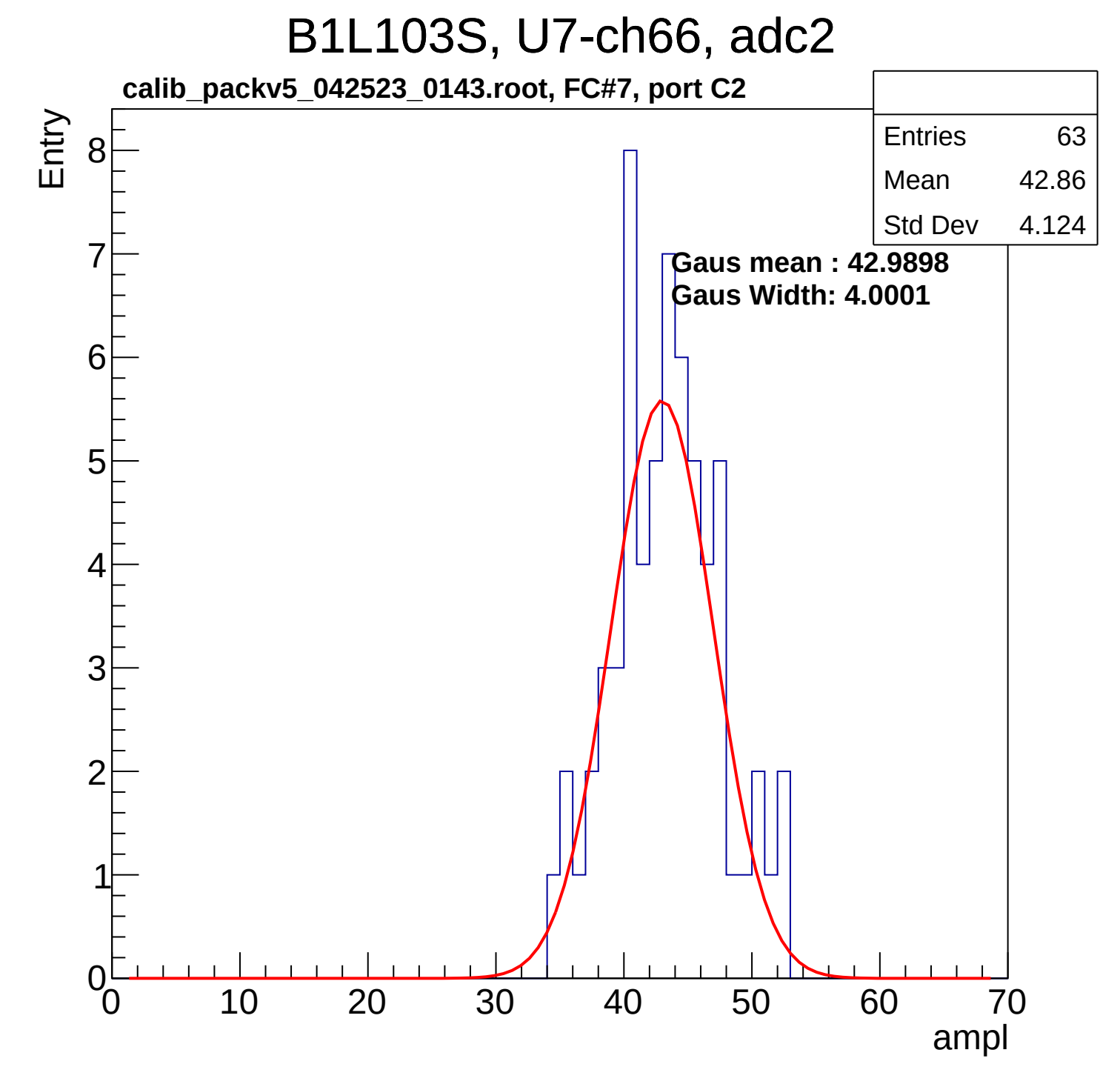
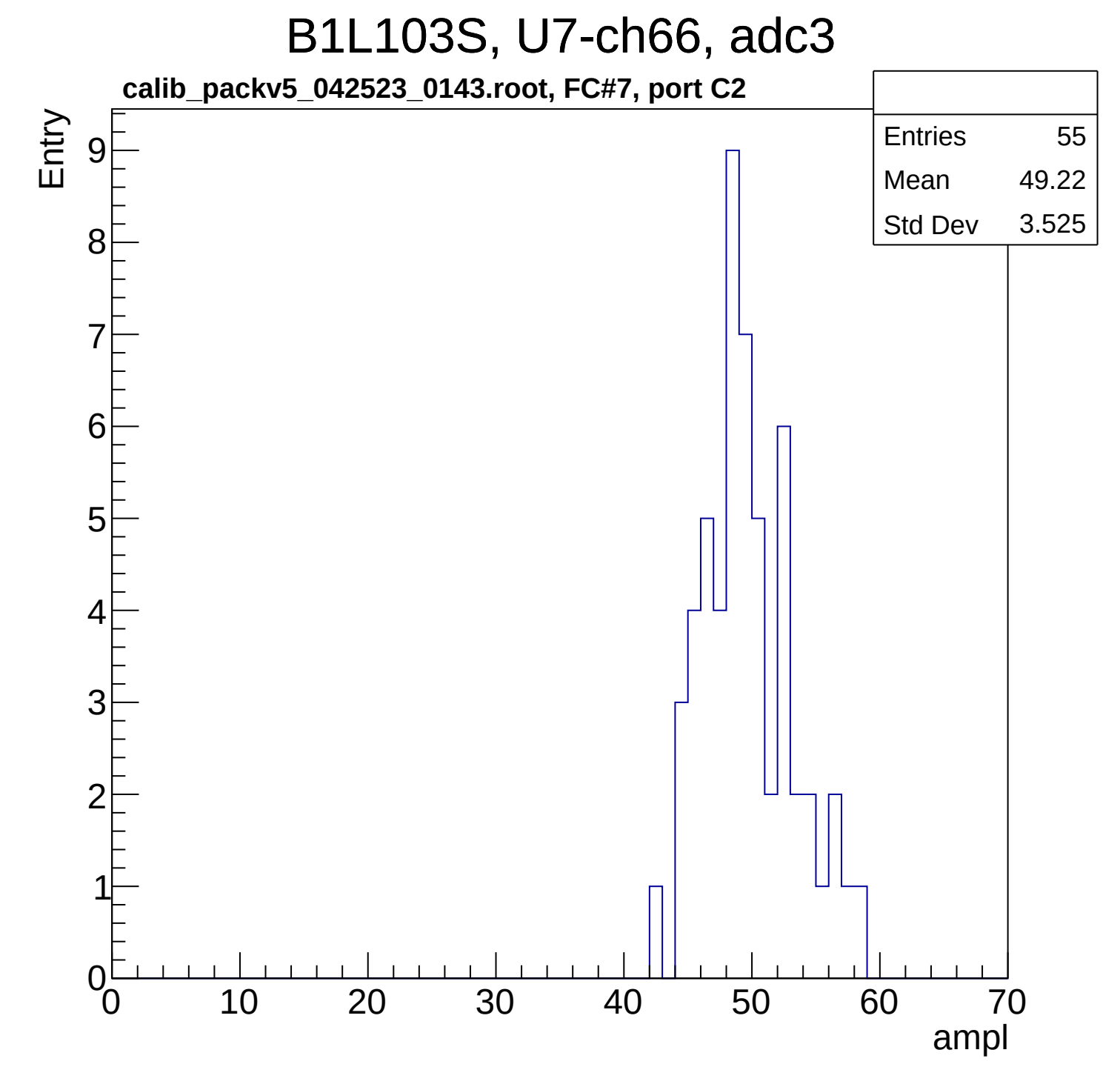

B1L103S, U7-ch66, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 75
Mean 36.84
Std Dev 3.99
Gaus mean : 37.0107
Gaus Width: 4.2754
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch66, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 42.86
Std Dev 4.124
Gaus mean : 42.9898
Gaus Width: 4.0001
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch66, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 49.22
Std Dev 3.525
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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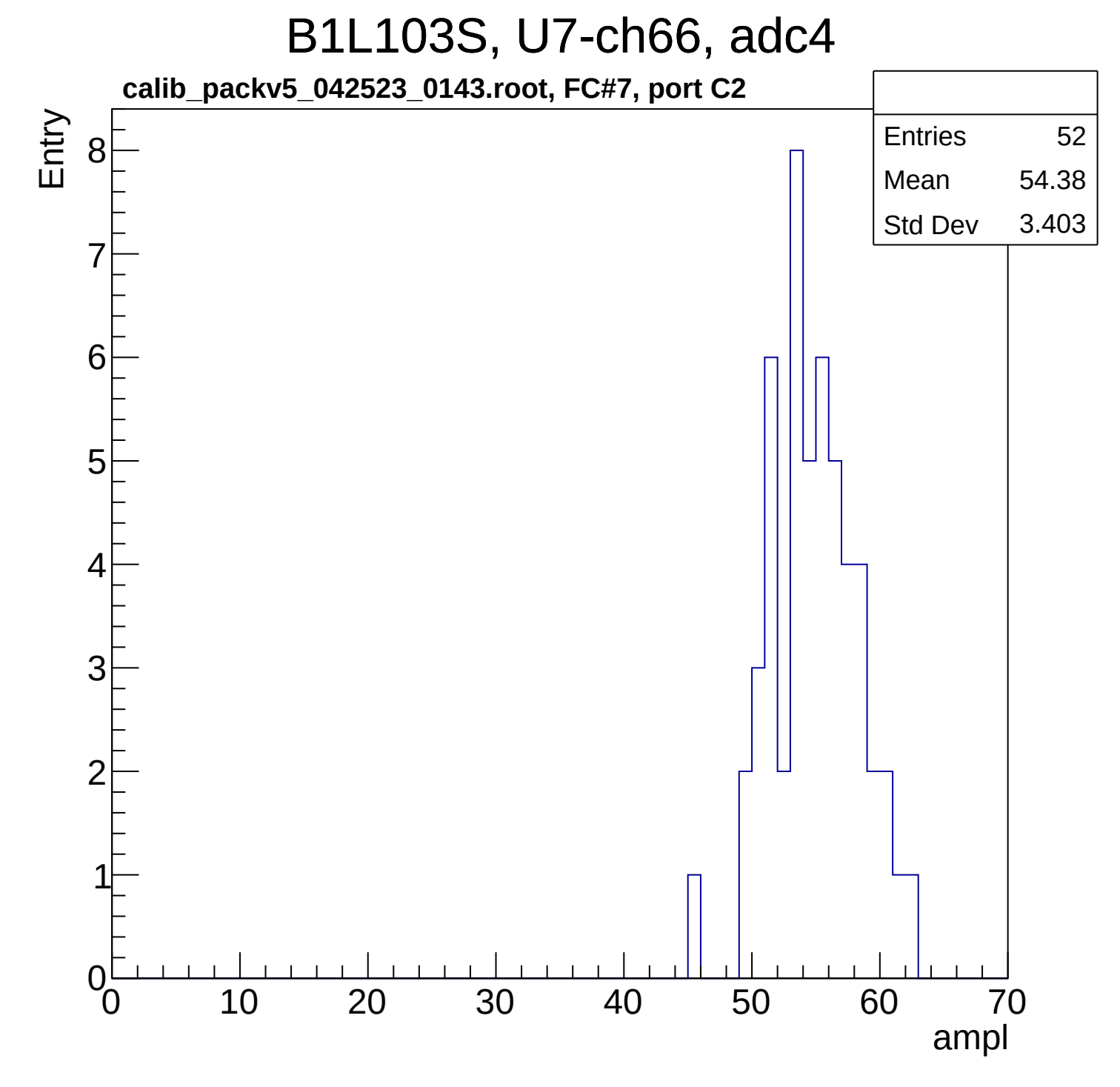
B1L103S, U7-ch66, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 52
Mean 54.38
Std Dev 3.403
Entry
ampl
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0
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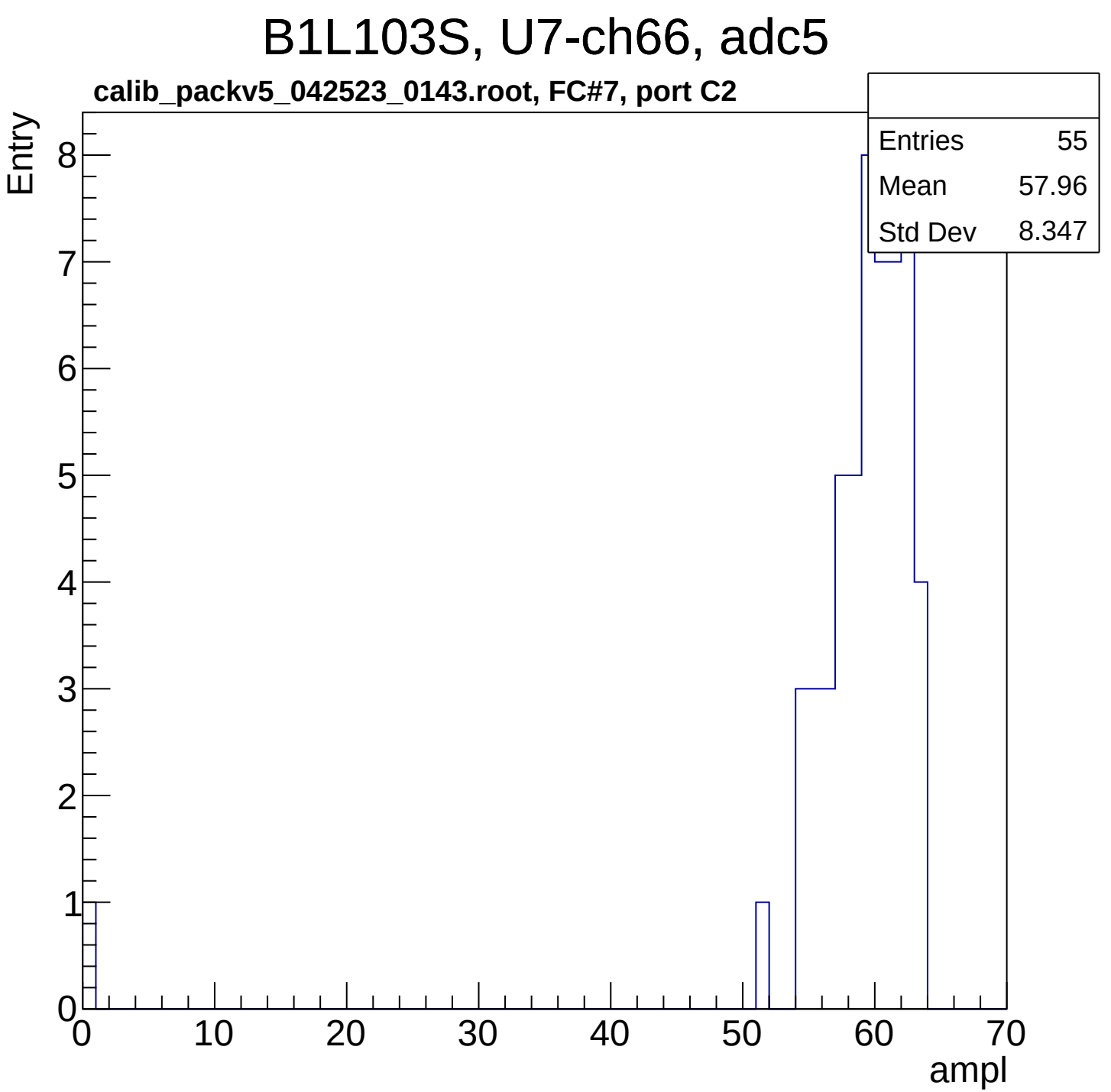
B1L103S, U7-ch66, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 57.96
Std Dev 8.347
Entry
ampl
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5
6
7
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0
10
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40
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60
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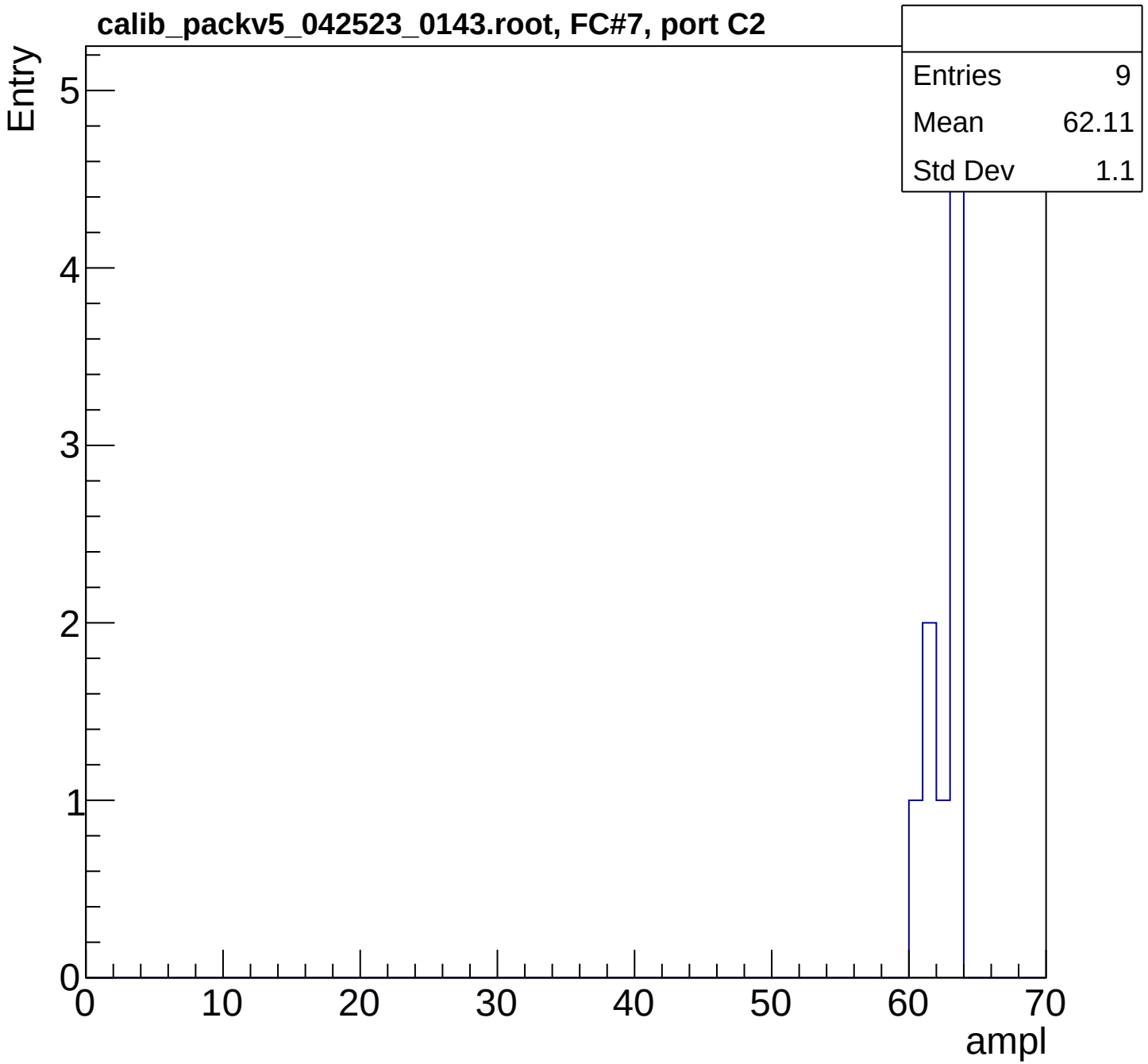
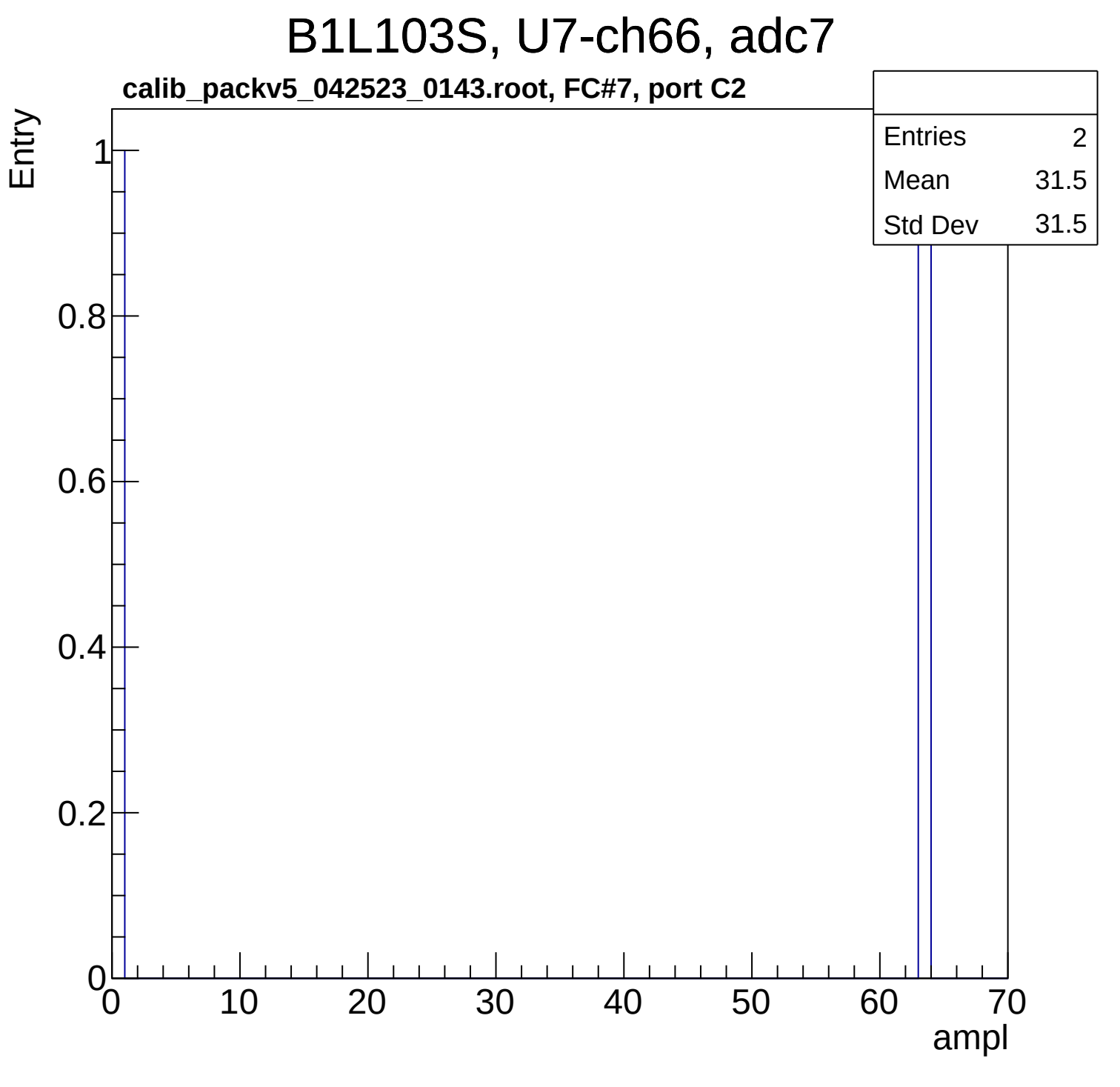

B1L103S, U7-ch66, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 9
Mean 62.11
Std Dev 1.1
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch66, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 31.5
Std Dev 31.5
Entry
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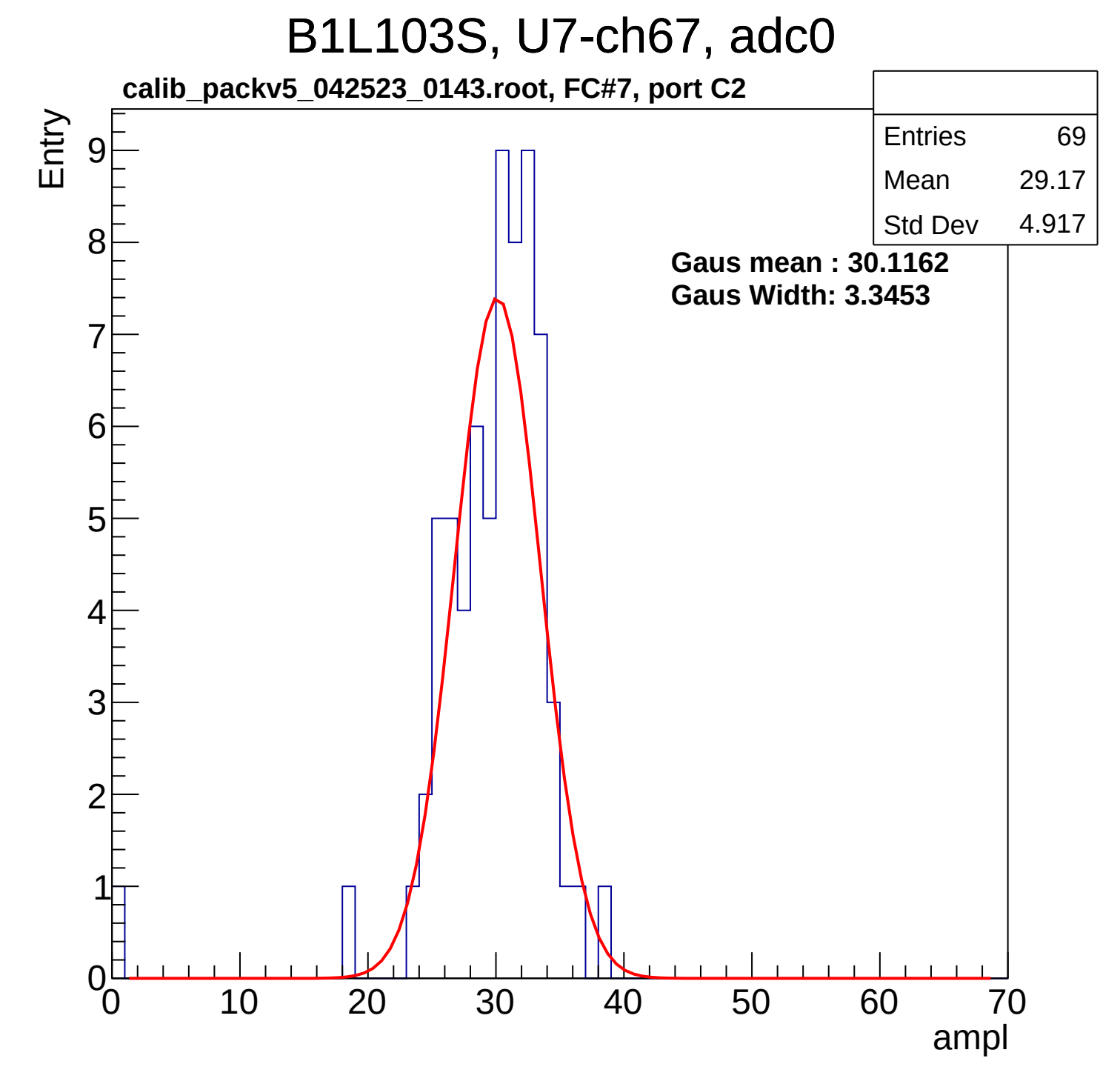
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch67, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 29.17
Std Dev 4.917
Gaus mean : 30.1162
Gaus Width: 3.3453
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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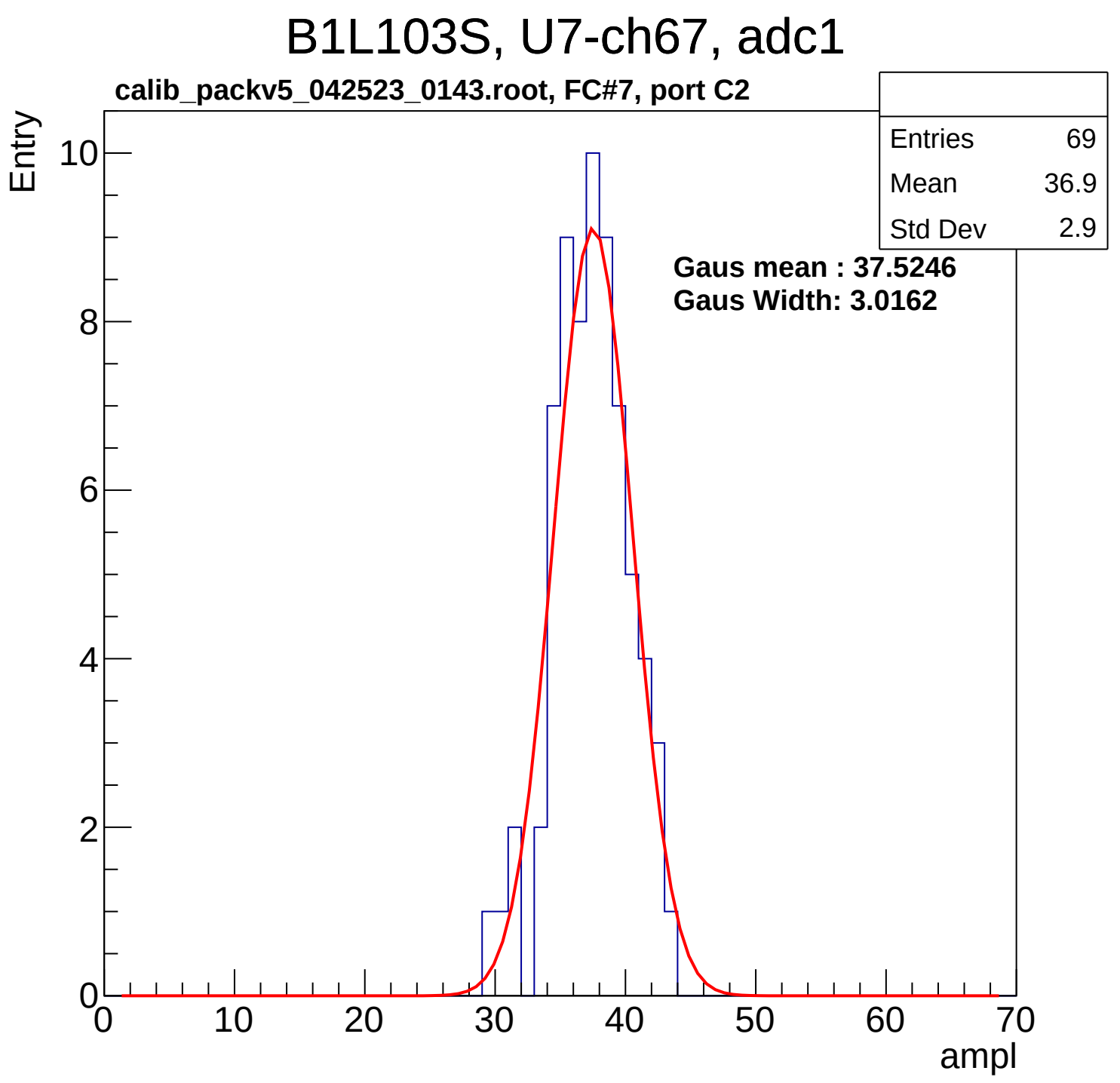
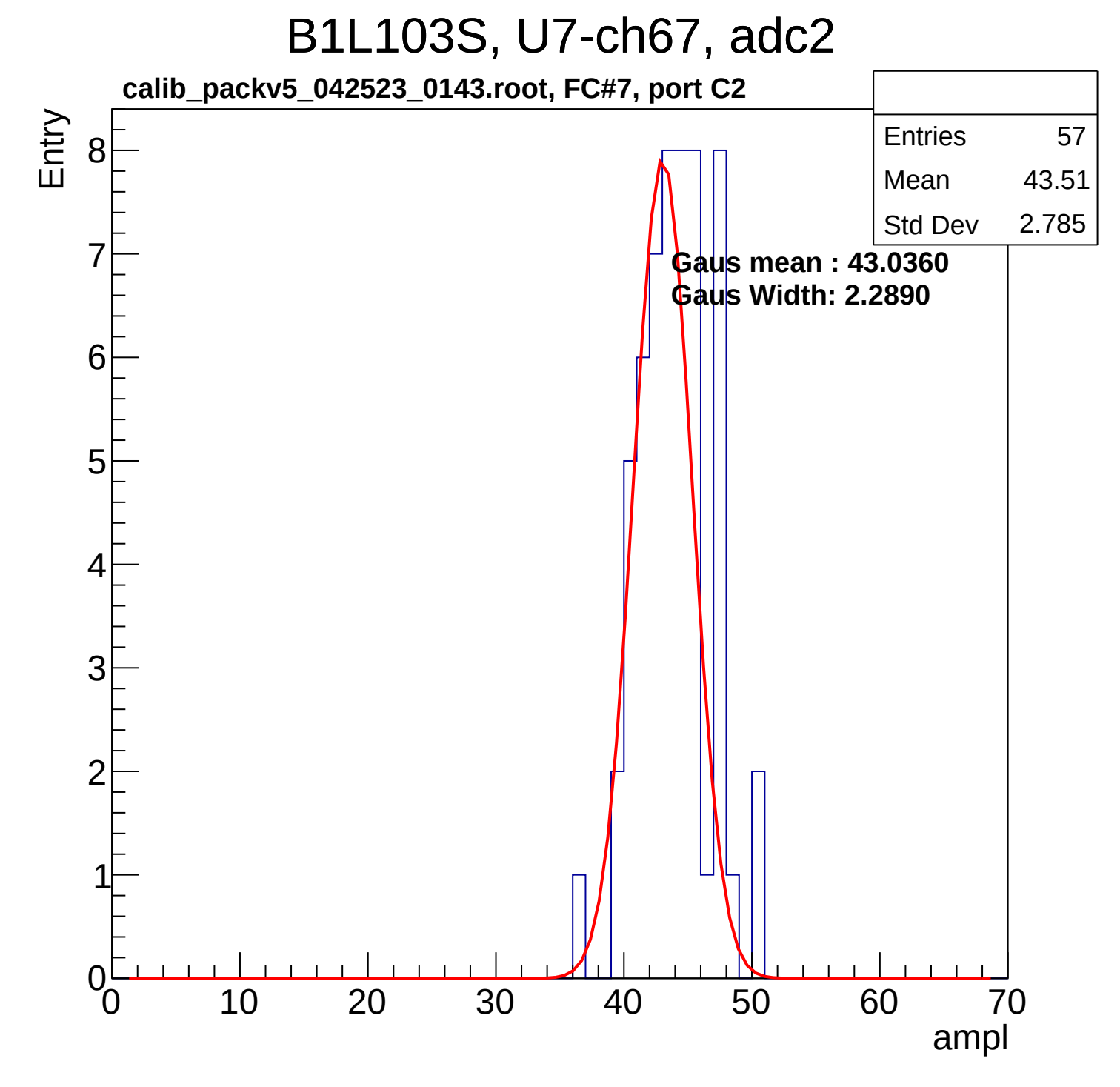

B1L103S, U7-ch67, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 36.9
Std Dev 2.9
Gaus mean : 37.5246
Gaus Width: 3.0162
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch67, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 43.51
Std Dev 2.785
Gaus mean : 43.0360
Gaus Width: 2.2890
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
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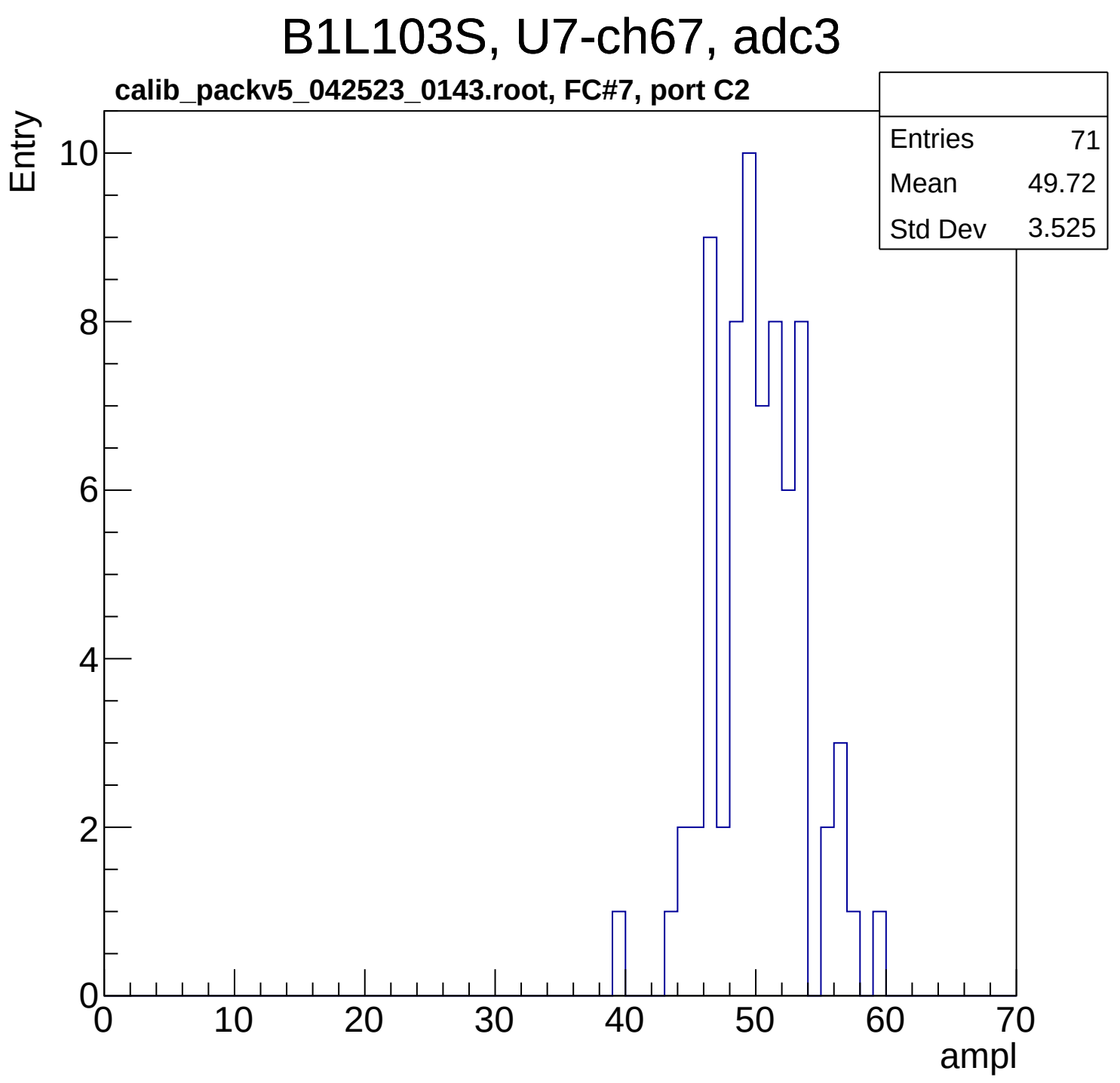
60
70


B1L103S, U7-ch67, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 71
Mean 49.72
Std Dev 3.525
Entry
ampl
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2
4
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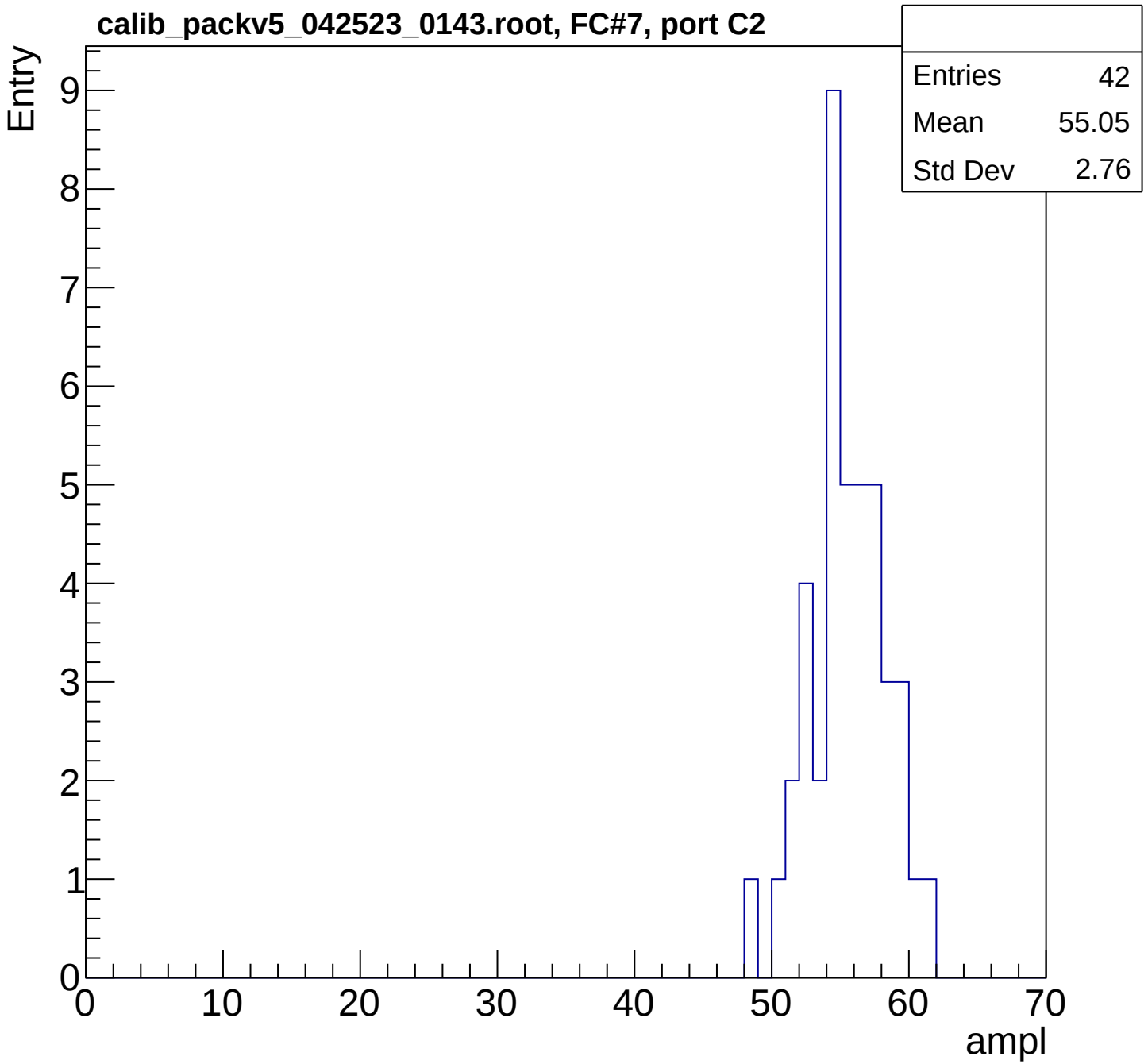
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch67, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 42
Mean 55.05
Std Dev 2.76
Entry
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3
4
5
6
7
8
9
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10
20
30
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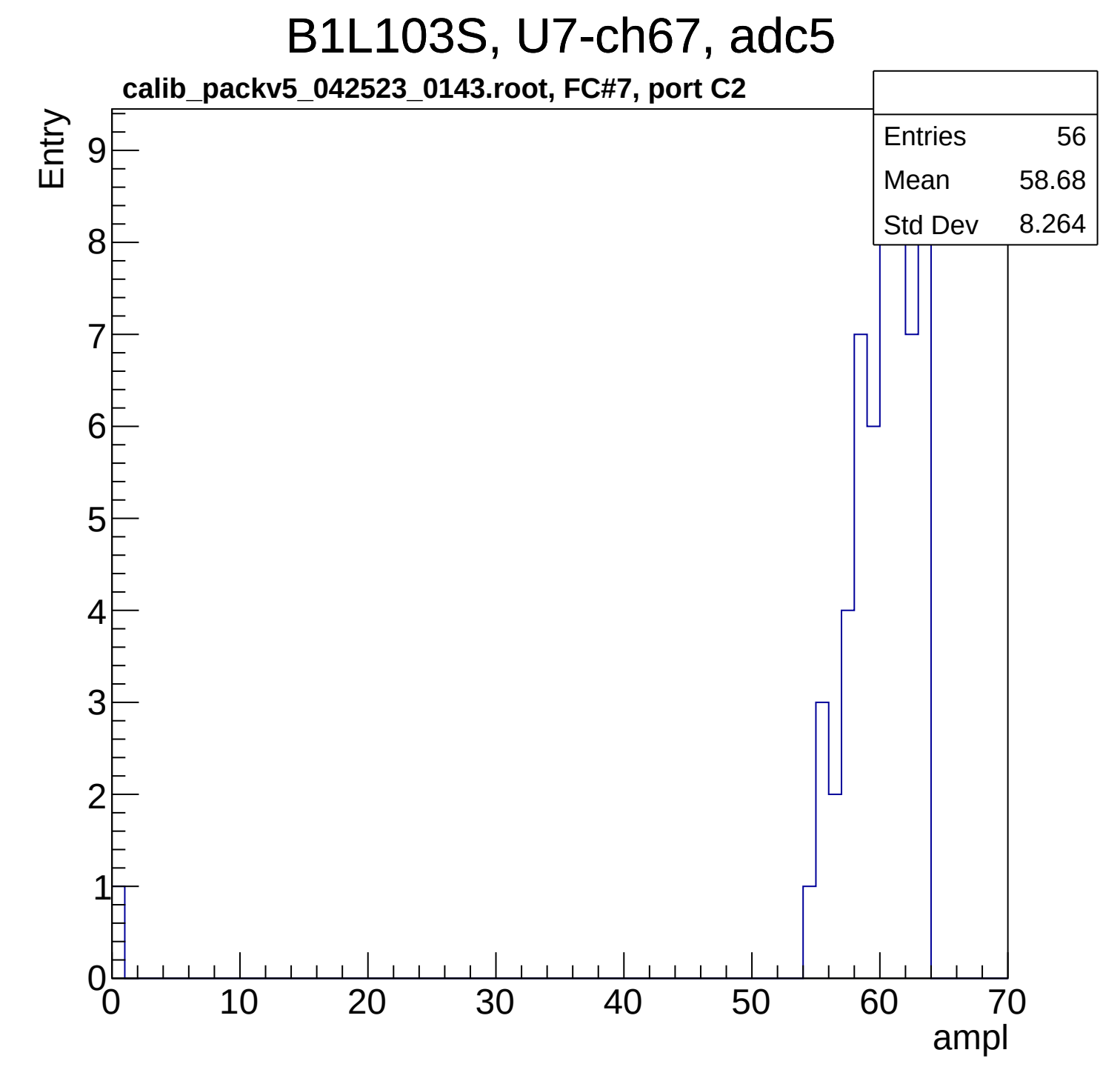
50
60
70
ampl


B1L103S, U7-ch67, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 58.68
Std Dev 8.264
Entry
ampl
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3
4
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6
7
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10
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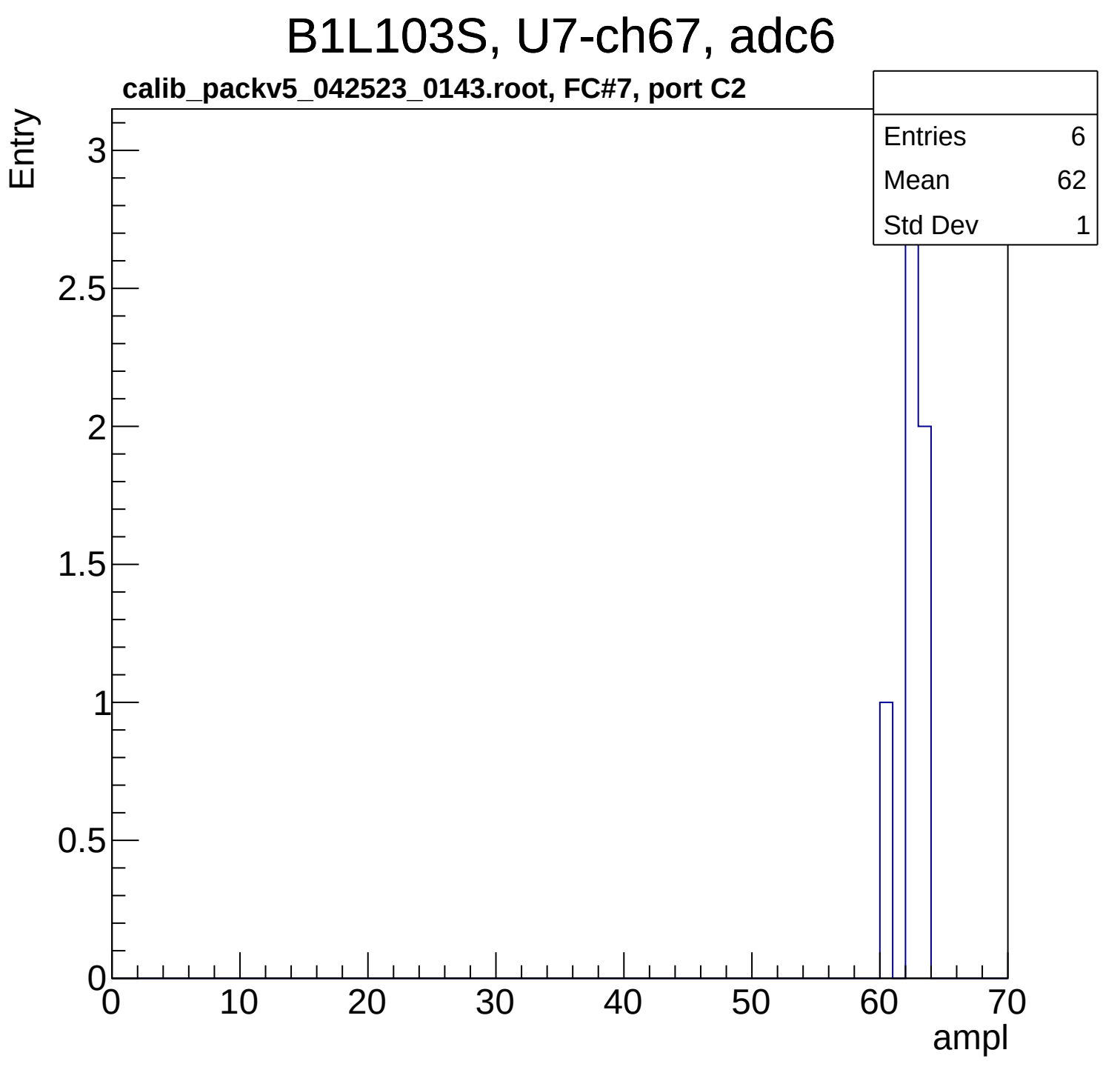
B1L103S, U7-ch67, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 6
Mean 62
Std Dev 1
Entry
ampl
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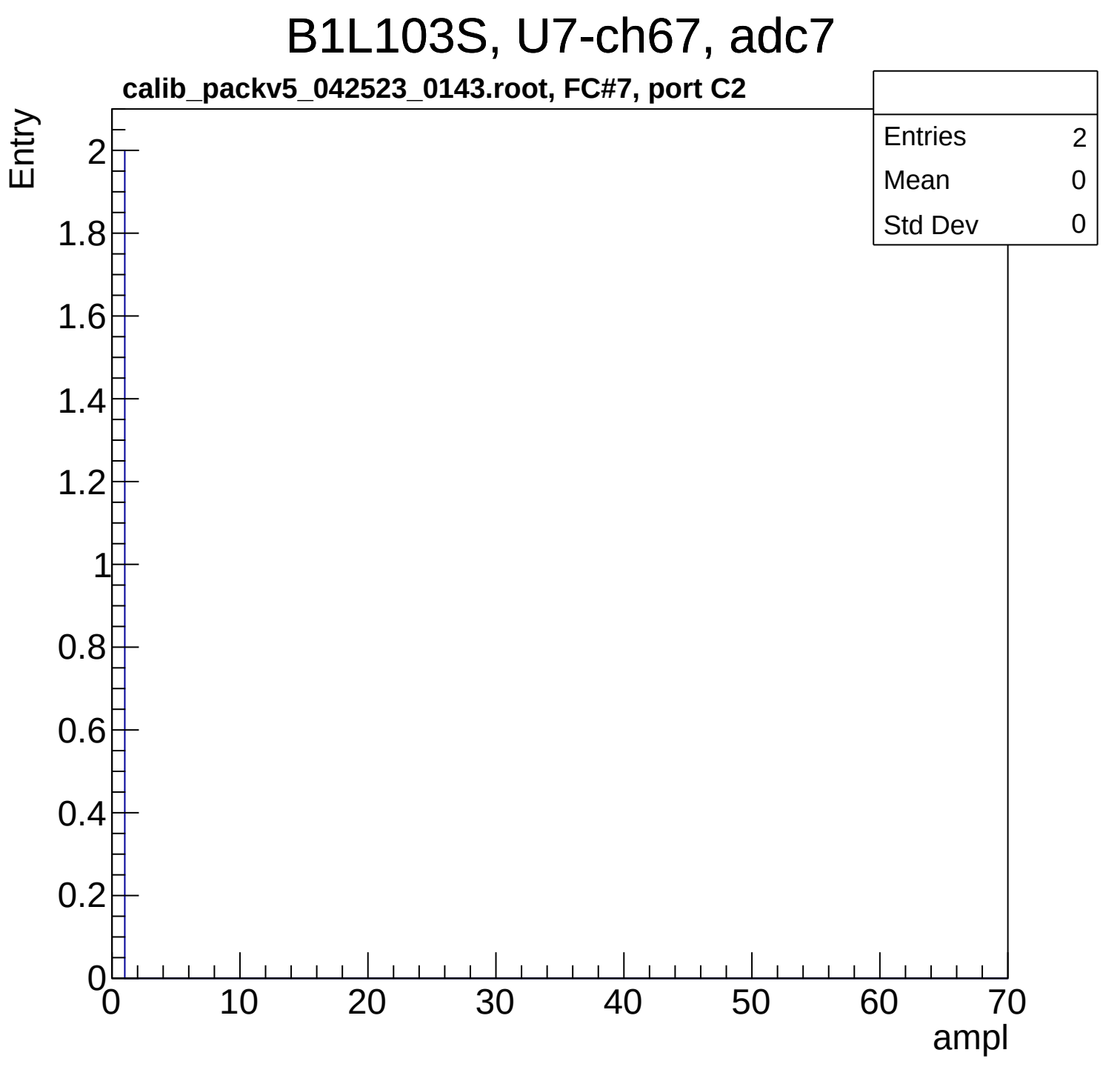
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U7-ch67, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
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0.8
0.6
0.4
0.2
0
0
10
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30
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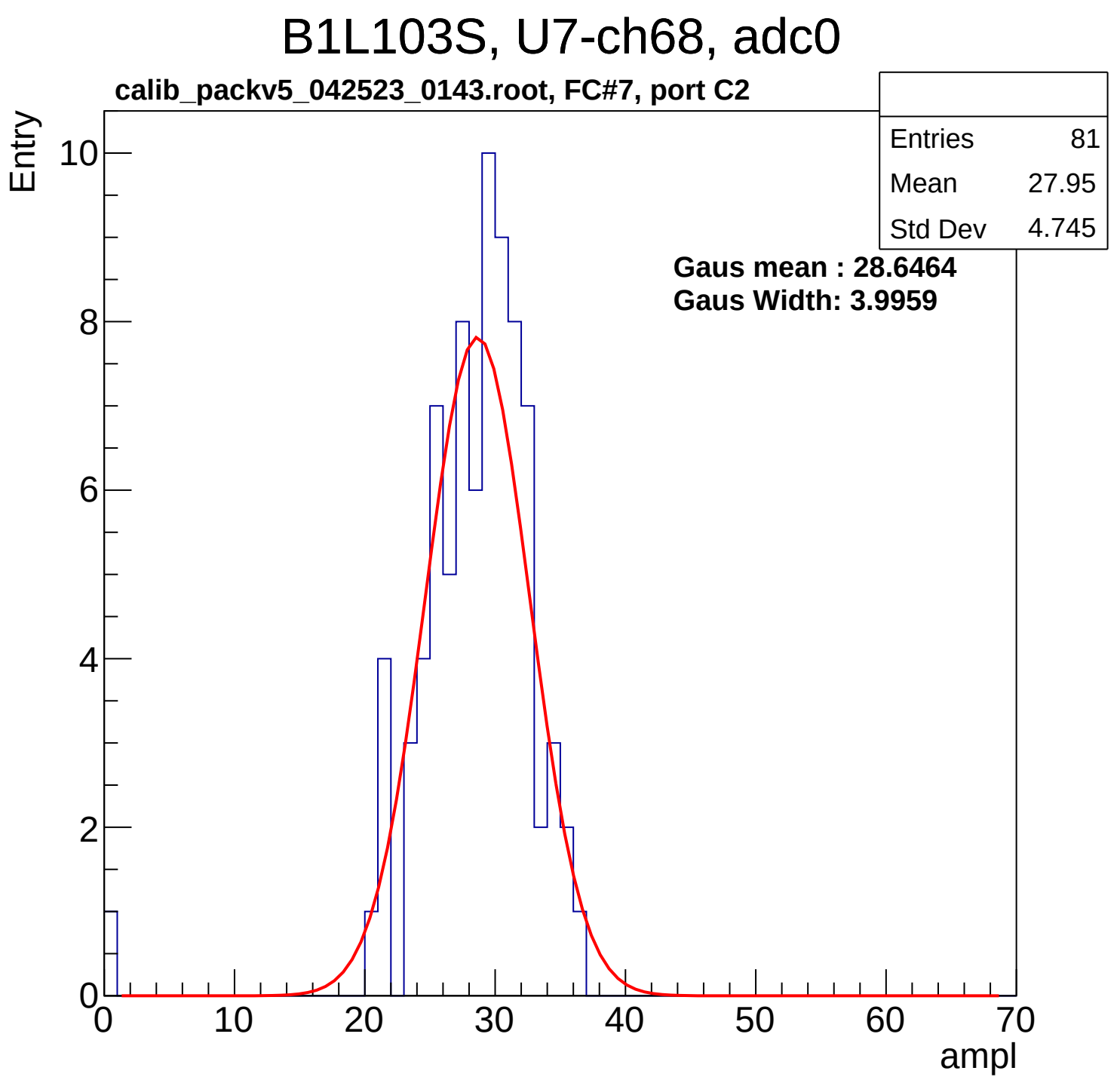
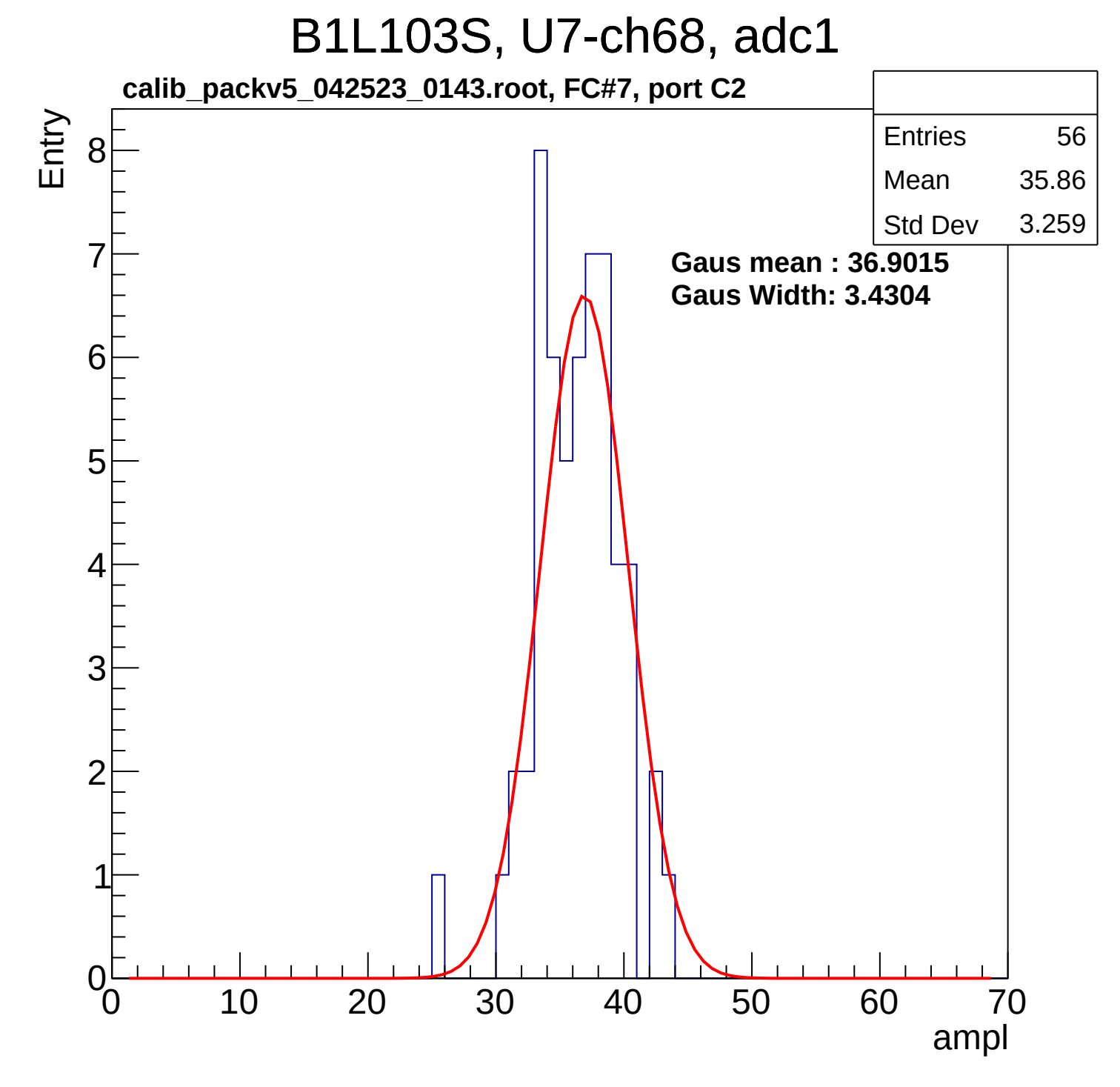
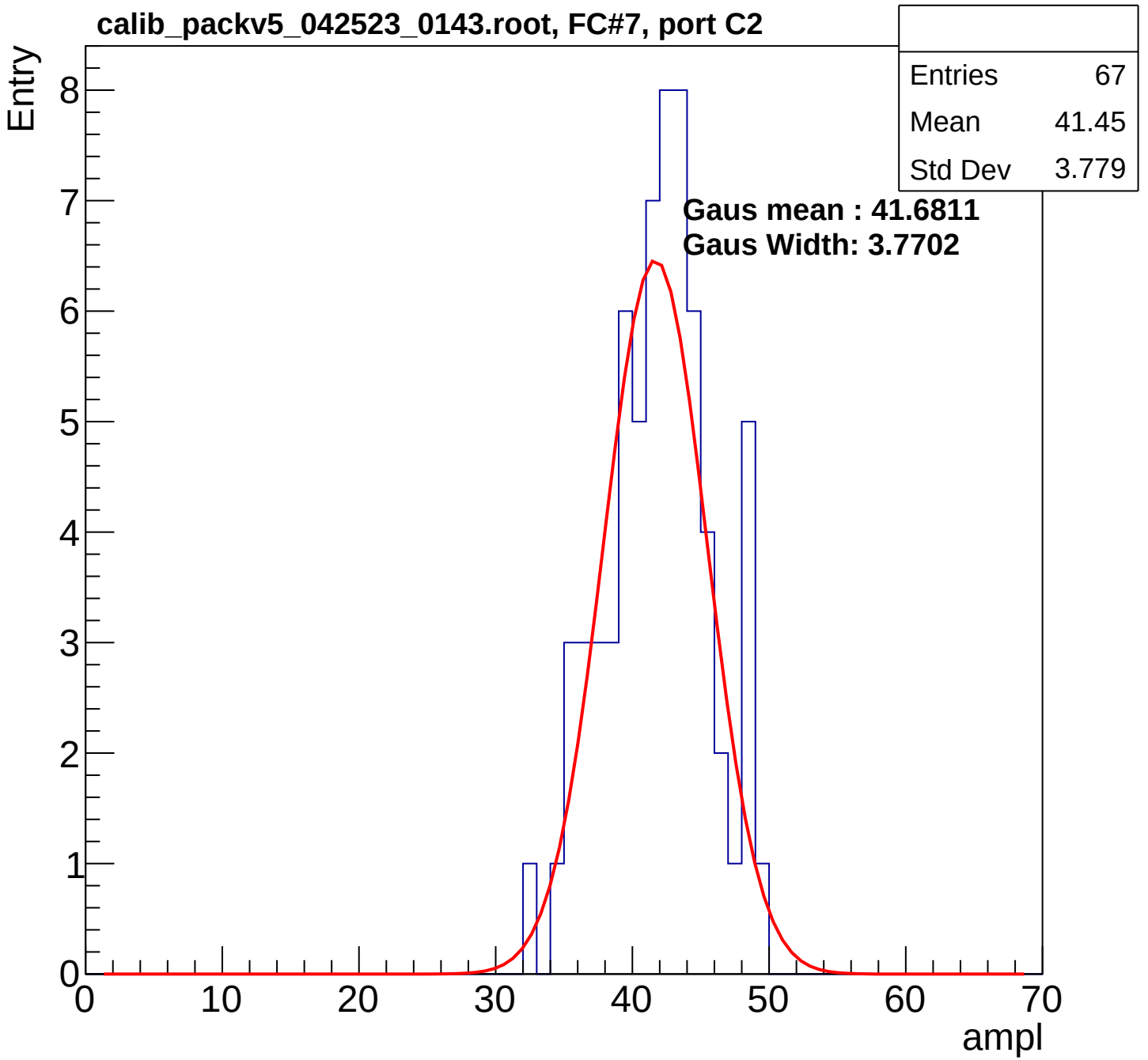
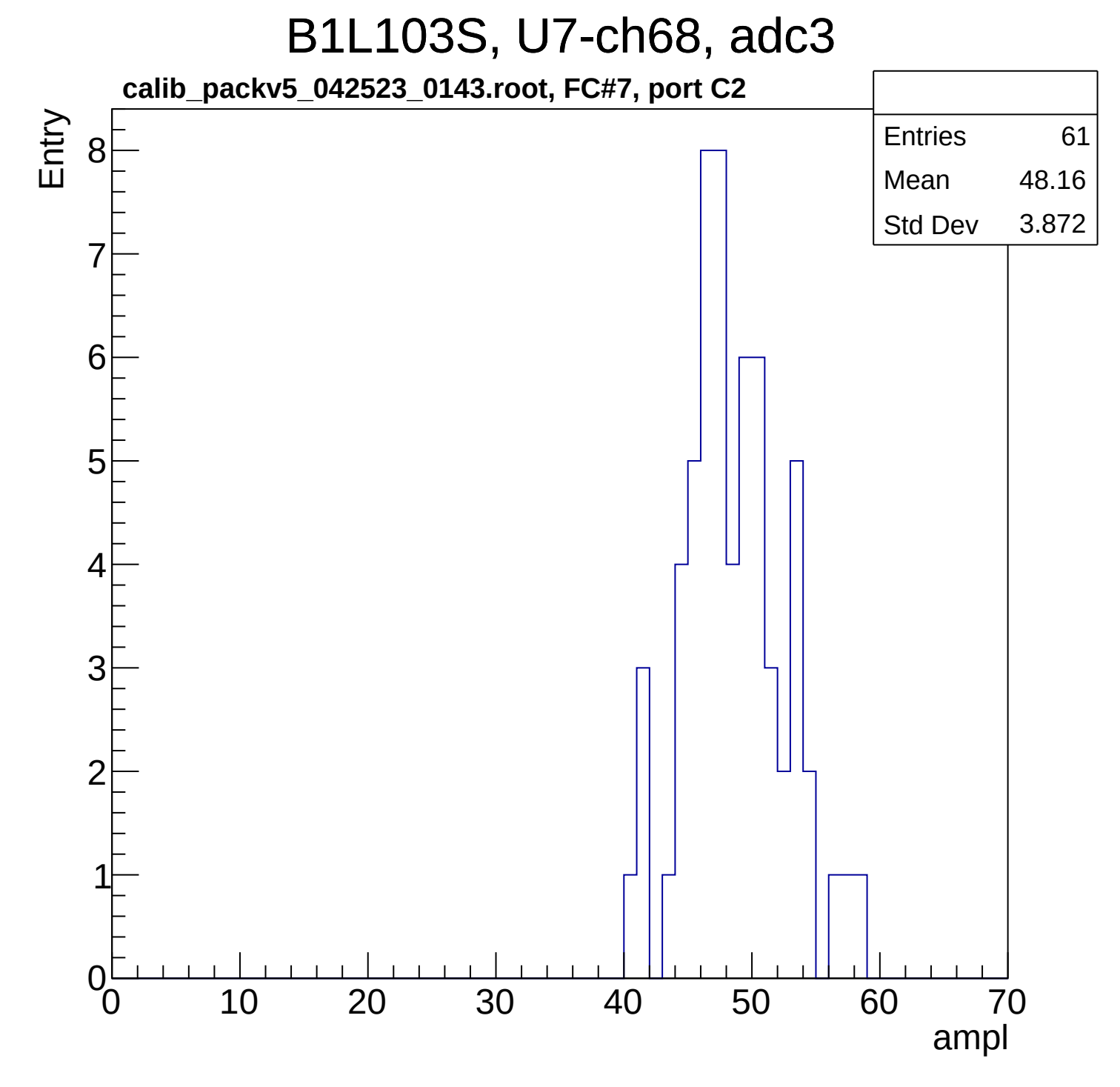
50
60
70
ampl


B1L103S, U7-ch68, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 81
Mean 27.95
Std Dev 4.745
Gaus mean : 28.6464
Gaus Width: 3.9959
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch68, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 35.86
Std Dev 3.259
Gaus mean : 36.9015
Gaus Width: 3.4304
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch68, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 41.45
Std Dev 3.779
Gaus mean : 41.6811
Gaus Width: 3.7702
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch68, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 61
Mean 48.16
Std Dev 3.872
Entry
ampl
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1
2
3
4
5
6
7
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0
10
20
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40
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60
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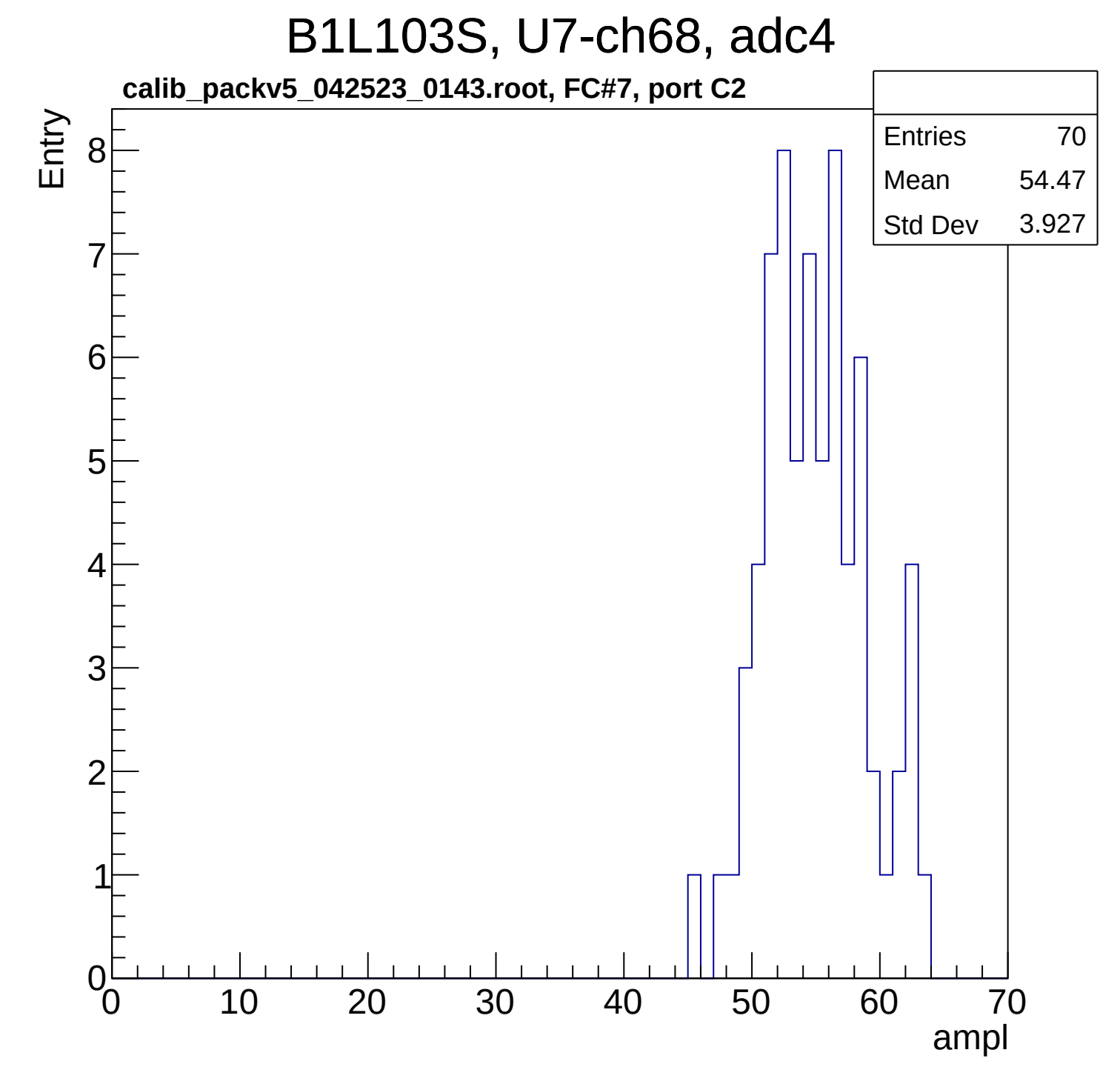
B1L103S, U7-ch68, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 54.47
Std Dev 3.927
Entry
ampl
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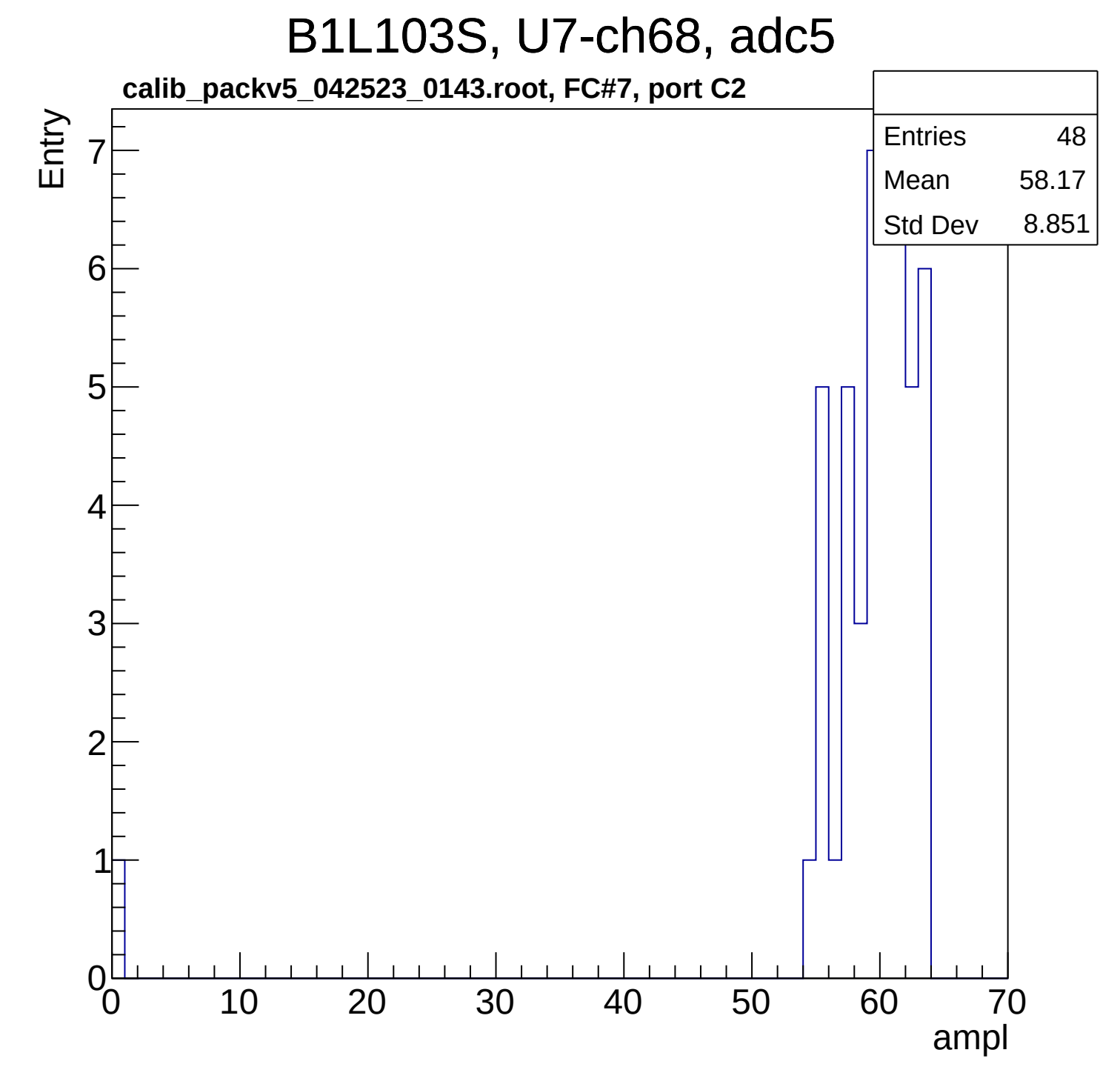
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch68, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 48
Mean 58.17
Std Dev 8.851
Entry
ampl
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1
2
3
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0
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40
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60
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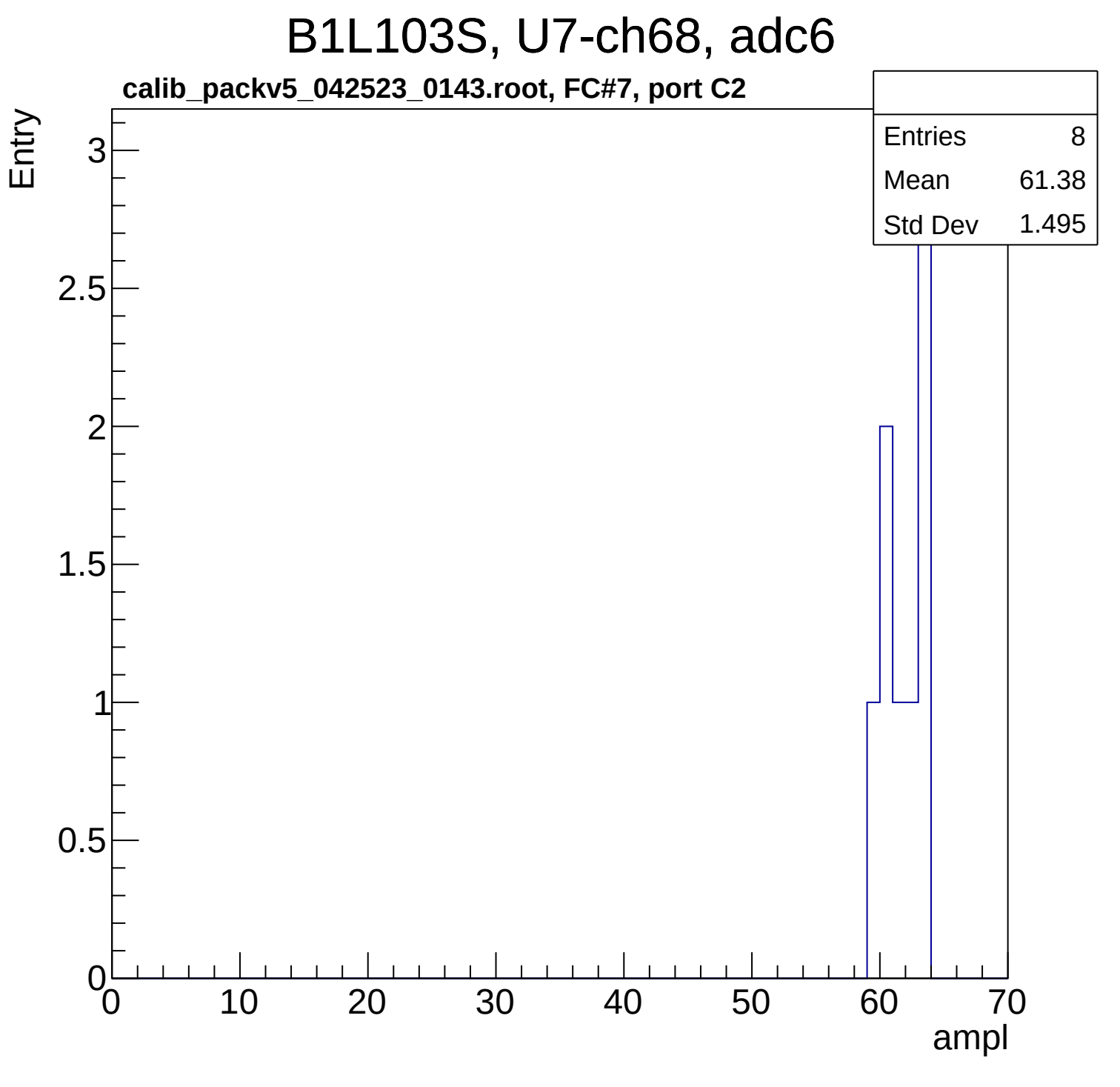
B1L103S, U7-ch68, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 8
Mean 61.38
Std Dev 1.495
Entry
ampl
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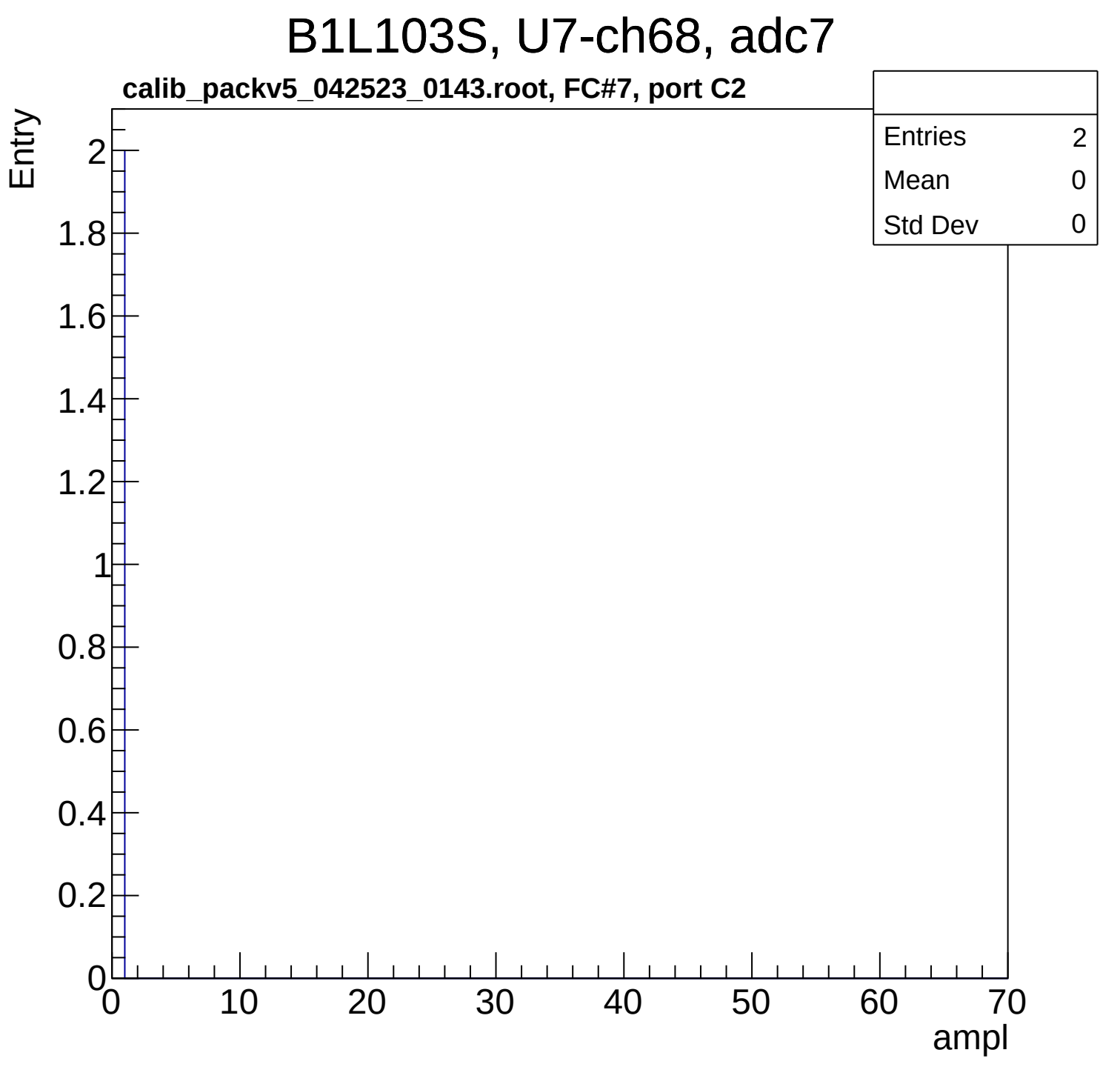
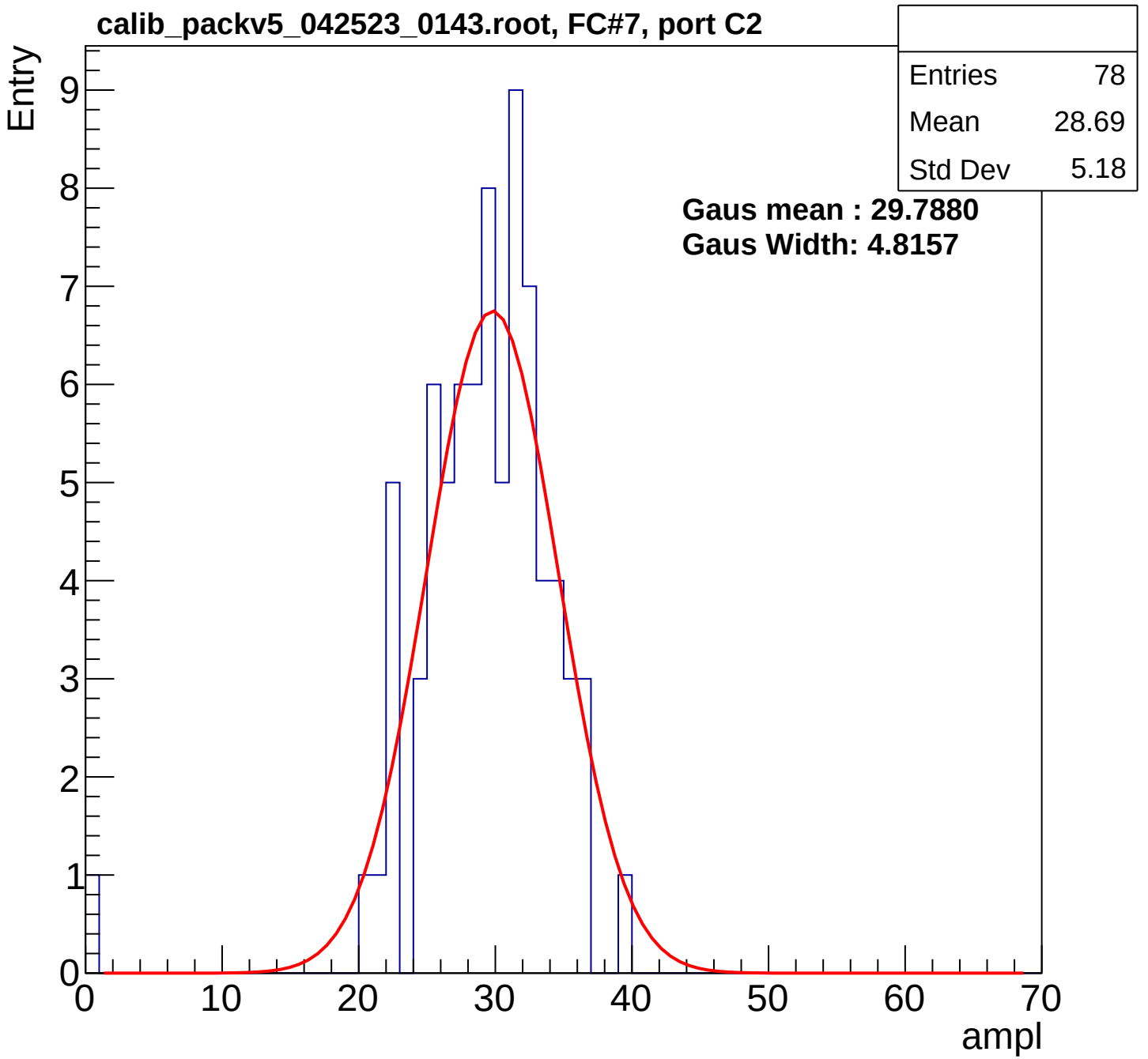
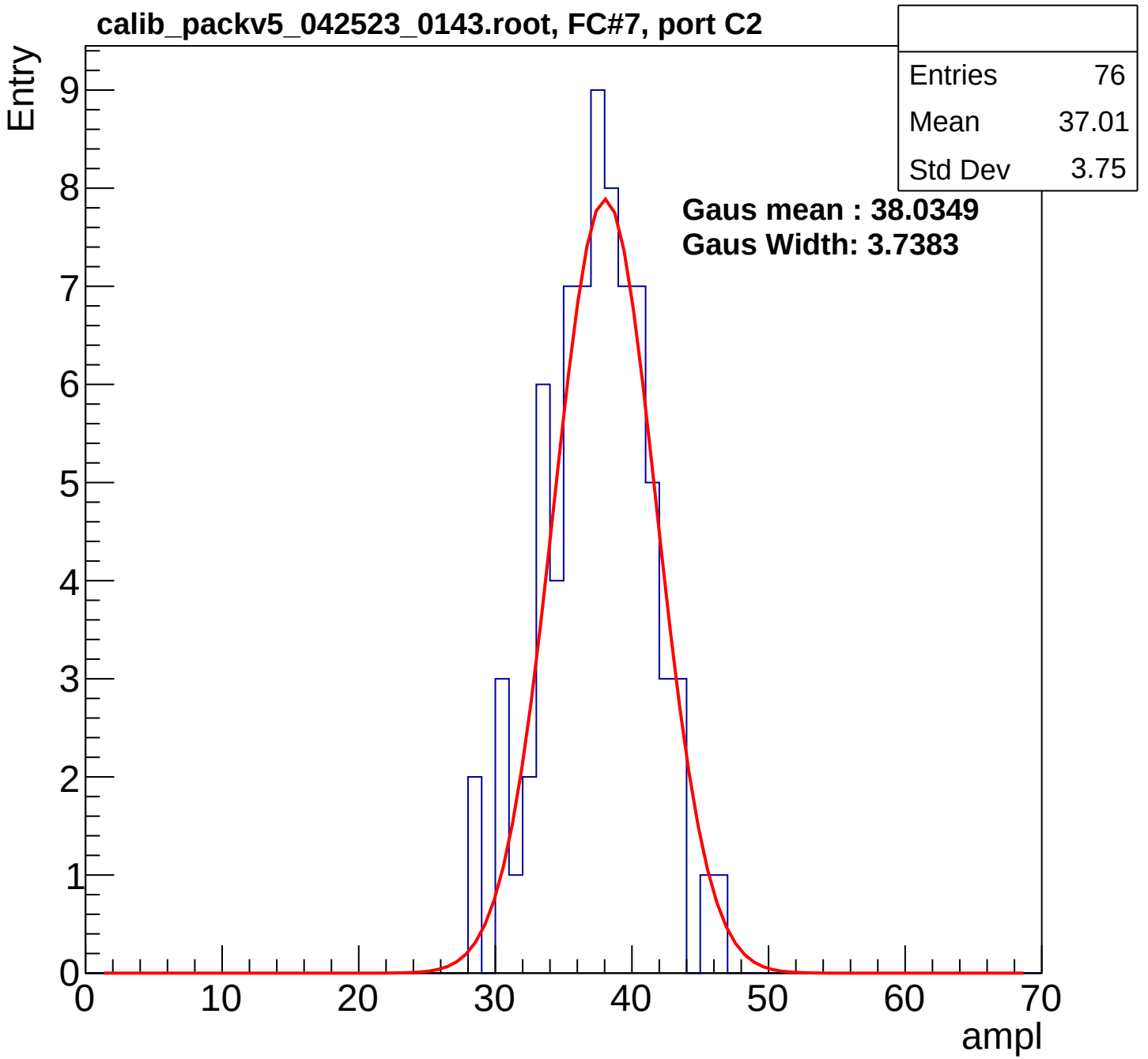
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U7-ch68, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch69, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 78
Mean 28.69
Std Dev 5.18
Gaus mean : 29.7880
Gaus Width: 4.8157
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch69, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 76
Mean 37.01
Std Dev 3.75
Gaus mean : 38.0349
Gaus Width: 3.7383
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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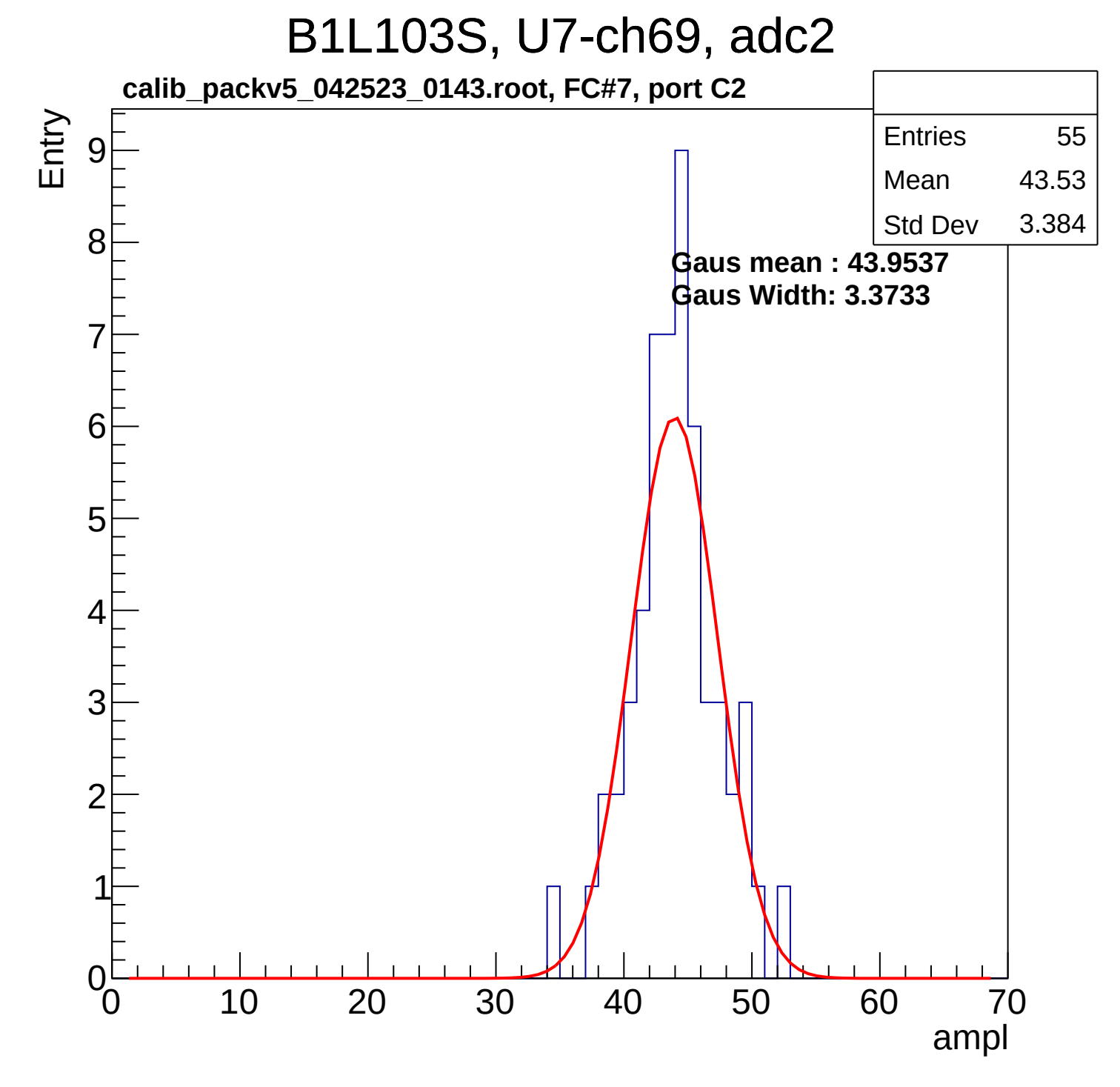
B1L103S, U7-ch69, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 43.53
Std Dev 3.384
Gaus mean : 43.9537
Gaus Width: 3.3733
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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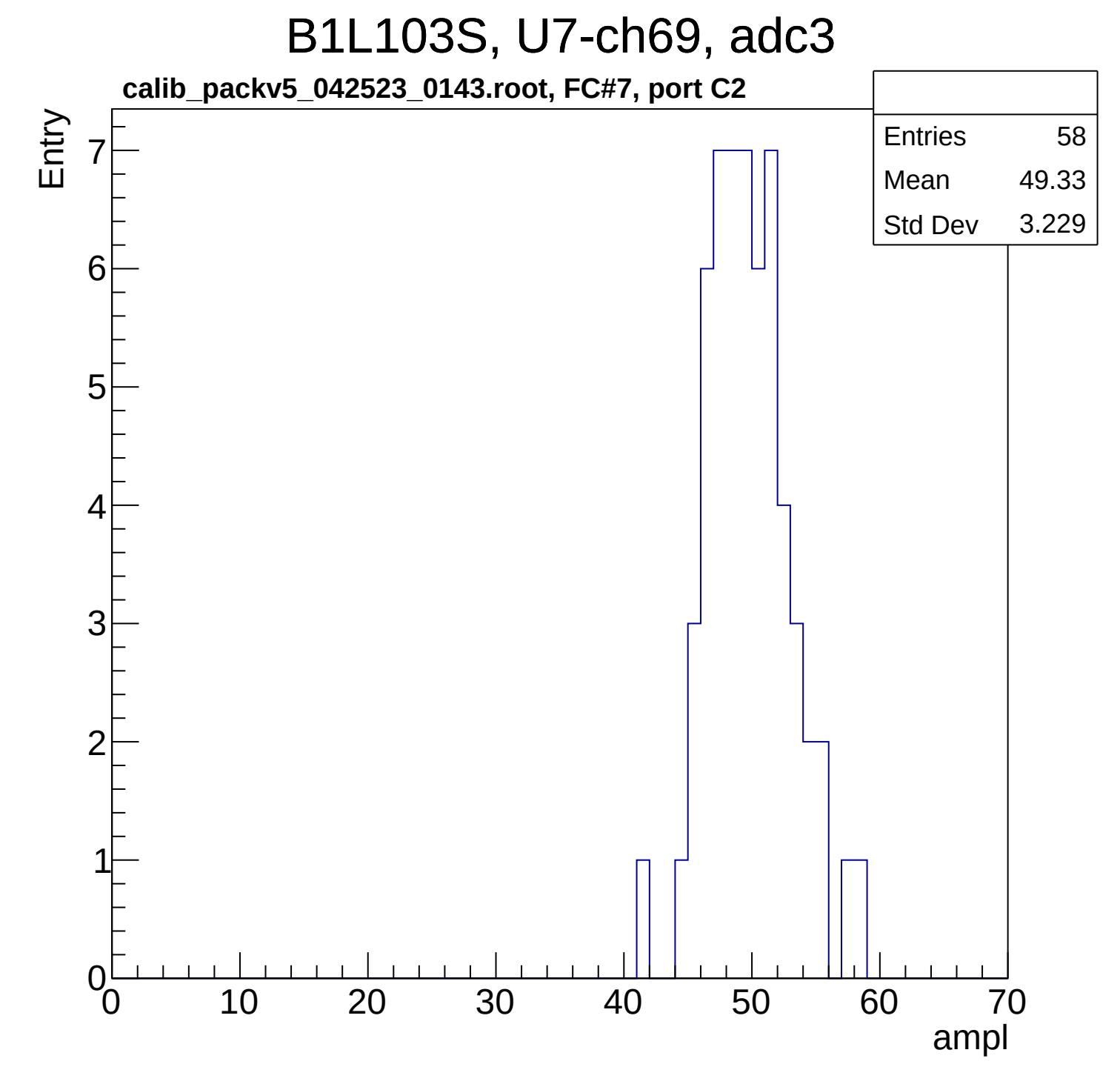
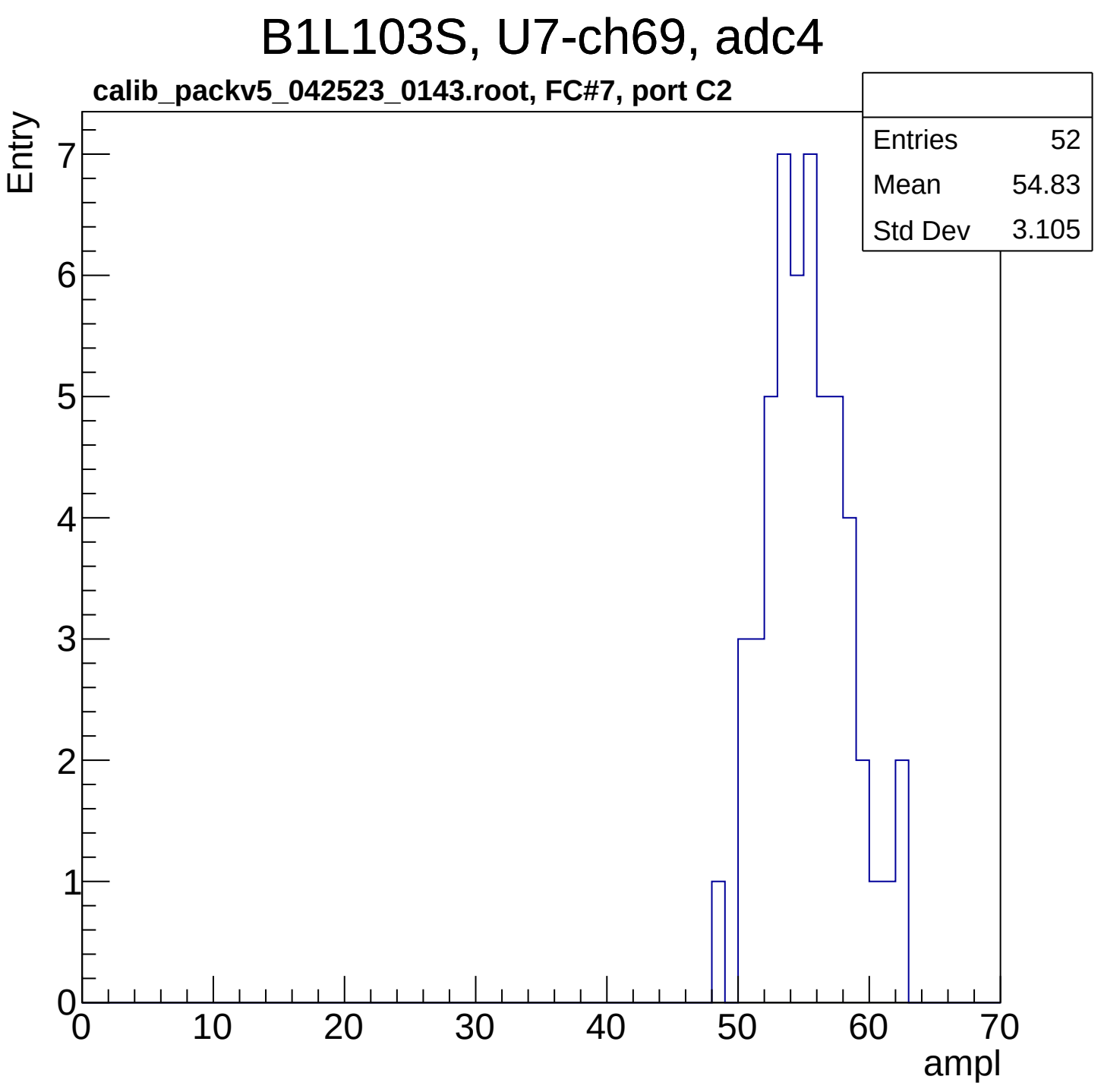

B1L103S, U7-ch69, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 58
Mean 49.33
Std Dev 3.229
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch69, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 52
Mean 54.83
Std Dev 3.105
Entry
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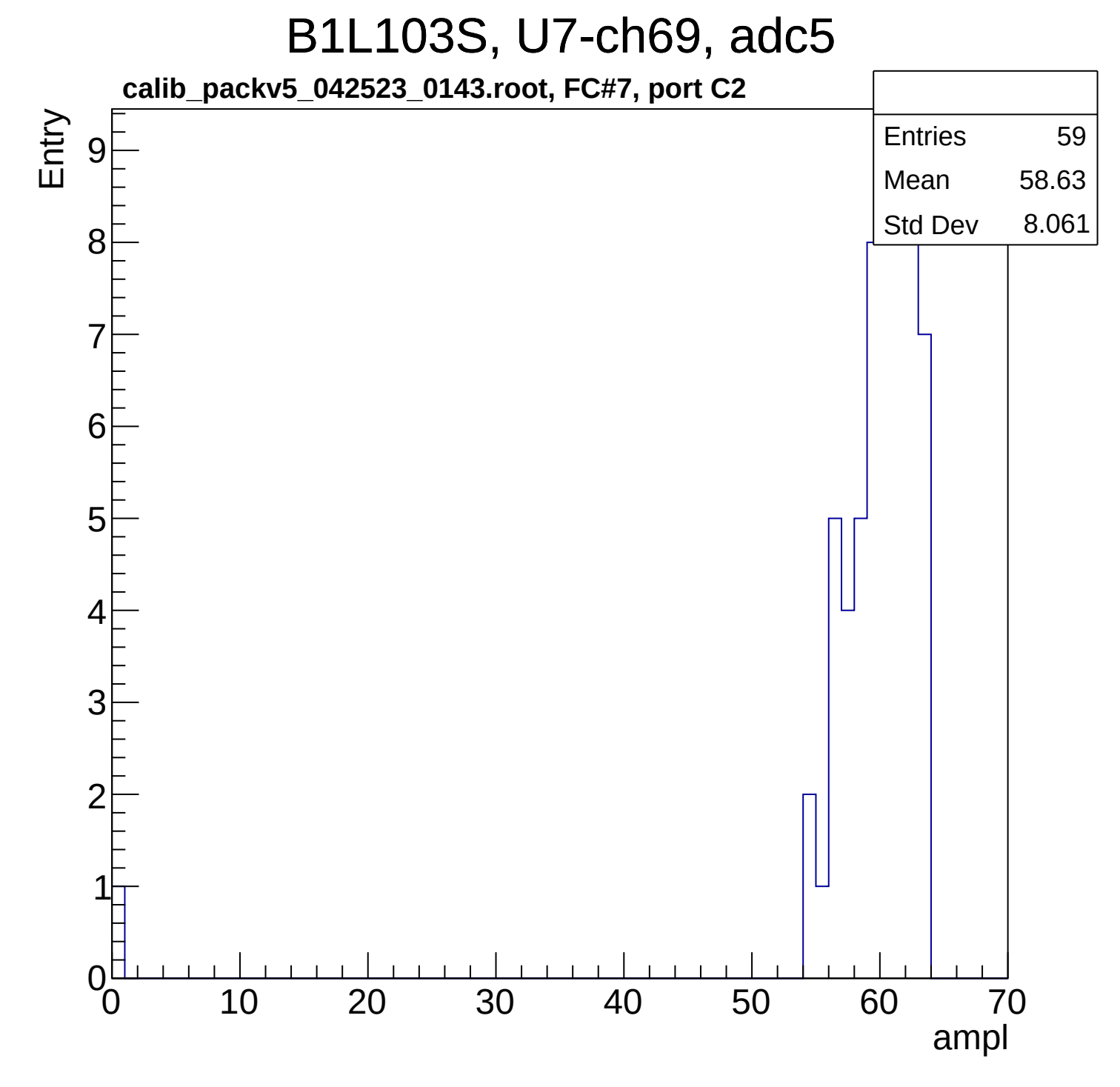
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch69, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 58.63
Std Dev 8.061
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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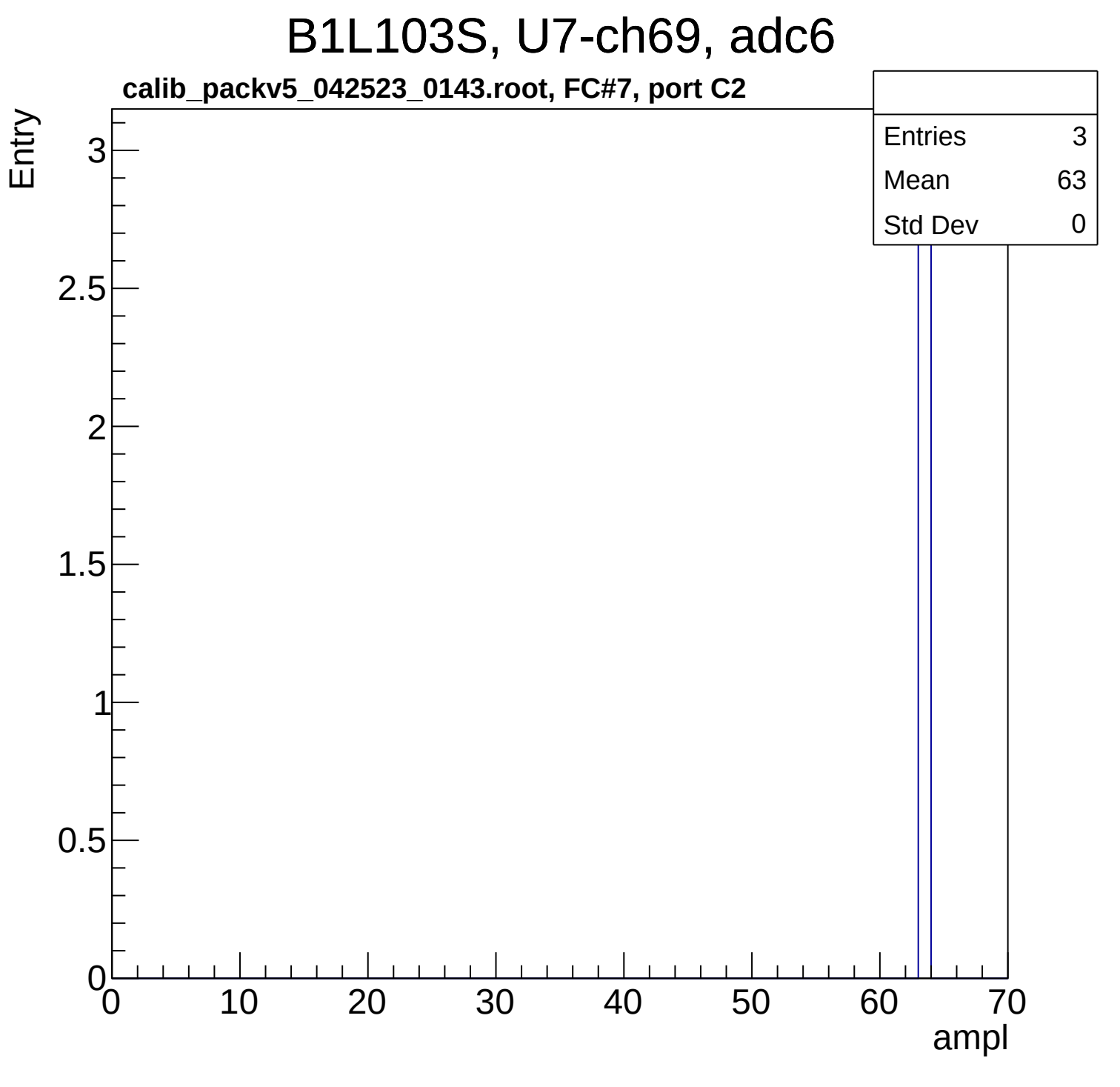
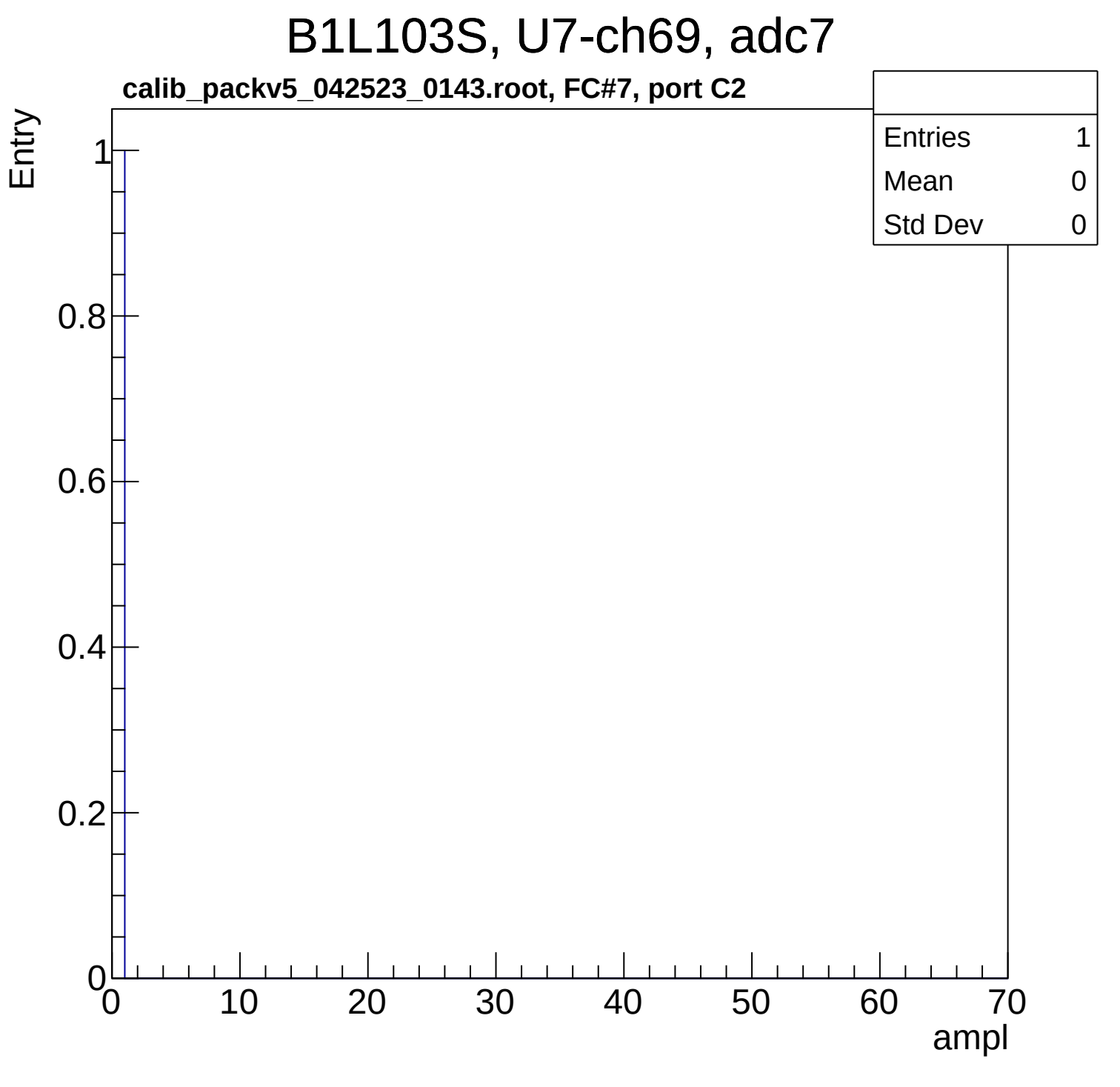
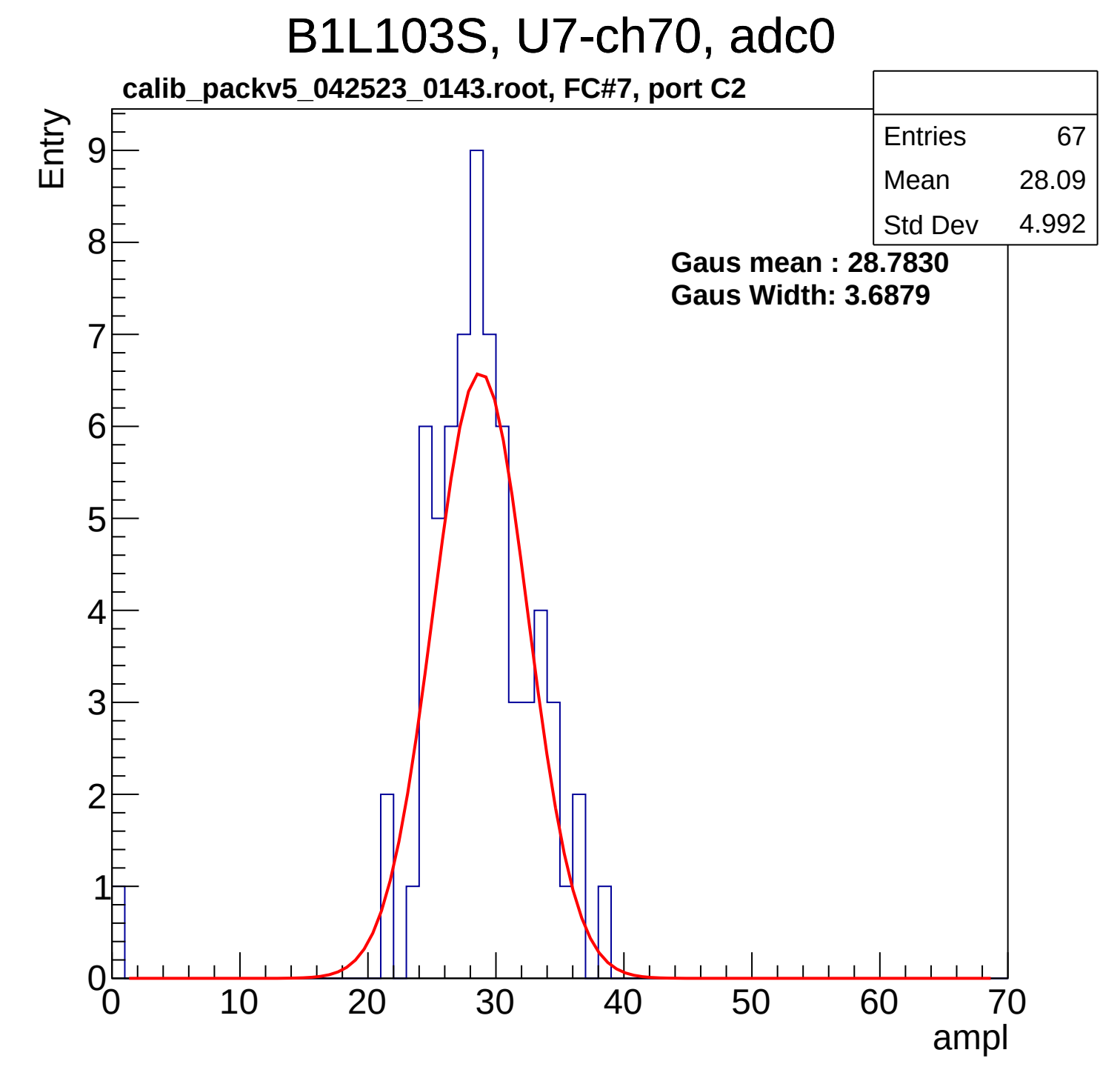

B1L103S, U7-ch69, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 63
Std Dev 0
Entry
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch69, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch70, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 28.09
Std Dev 4.992
Gaus mean : 28.7830
Gaus Width: 3.6879
Entry
ampl
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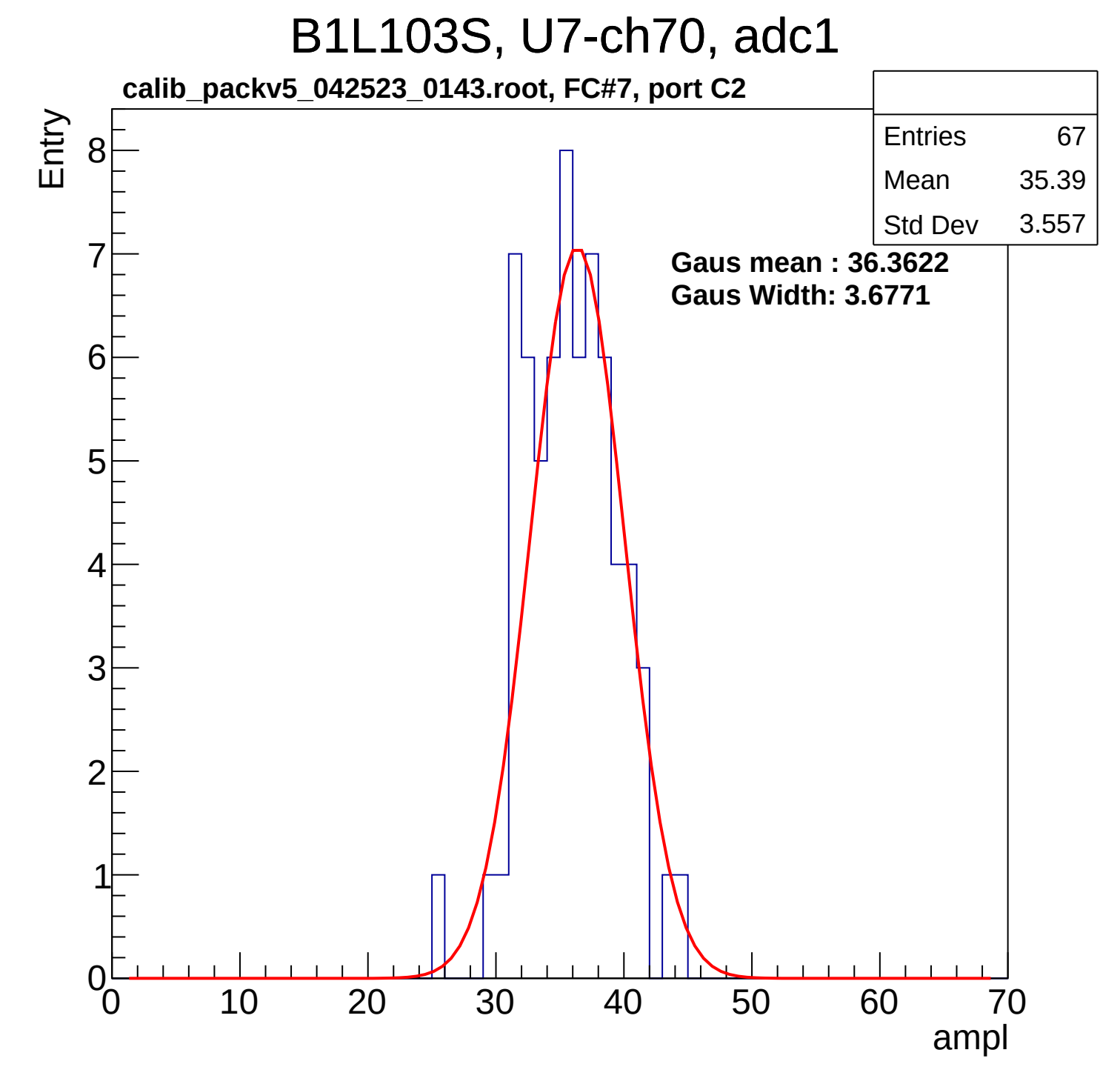
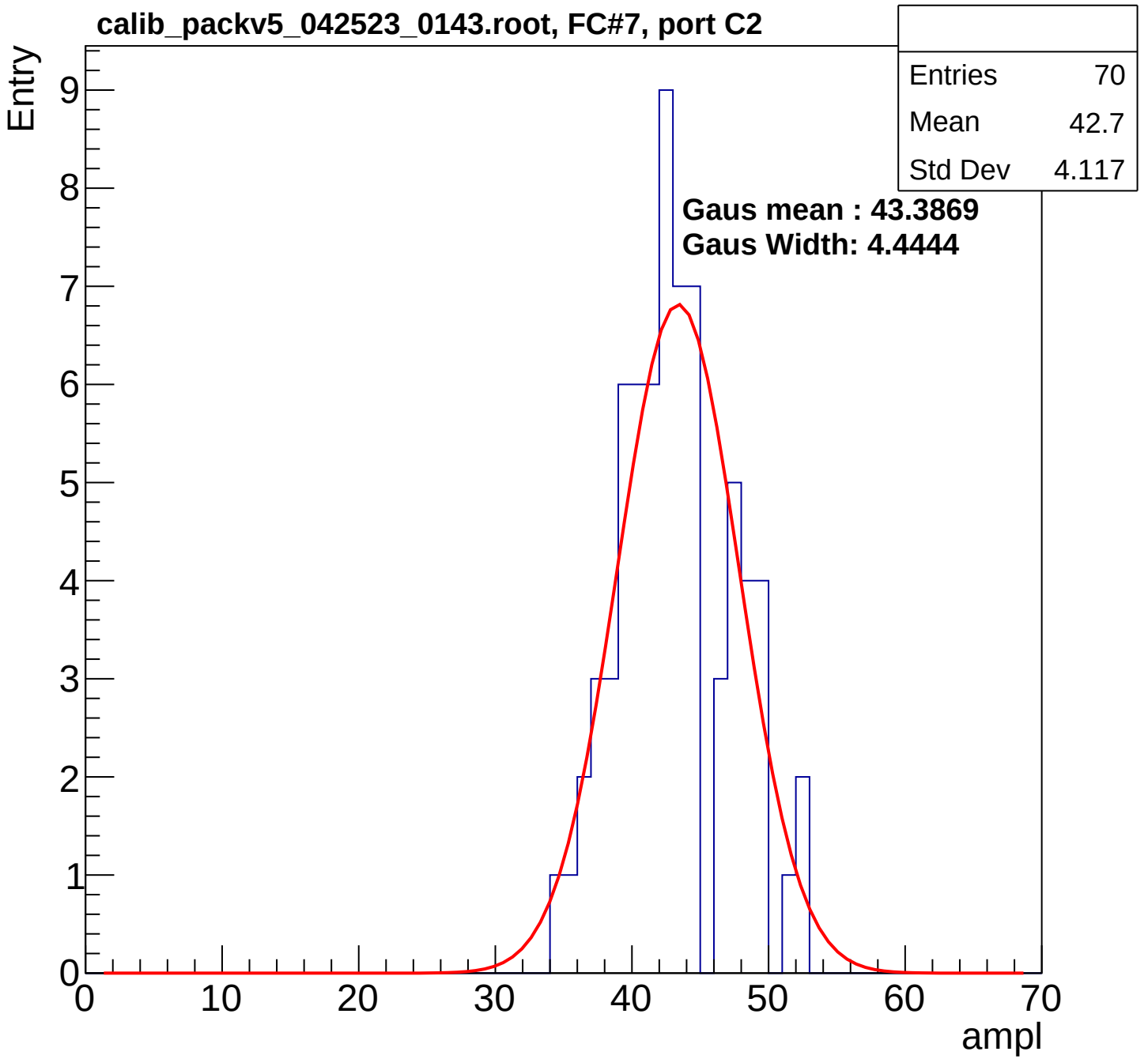
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch70, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 35.39
Std Dev 3.557
Gaus mean : 36.3622
Gaus Width: 3.6771
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch70, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 42.7
Std Dev 4.117
Gaus mean : 43.3869
Gaus Width: 4.4444
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
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60
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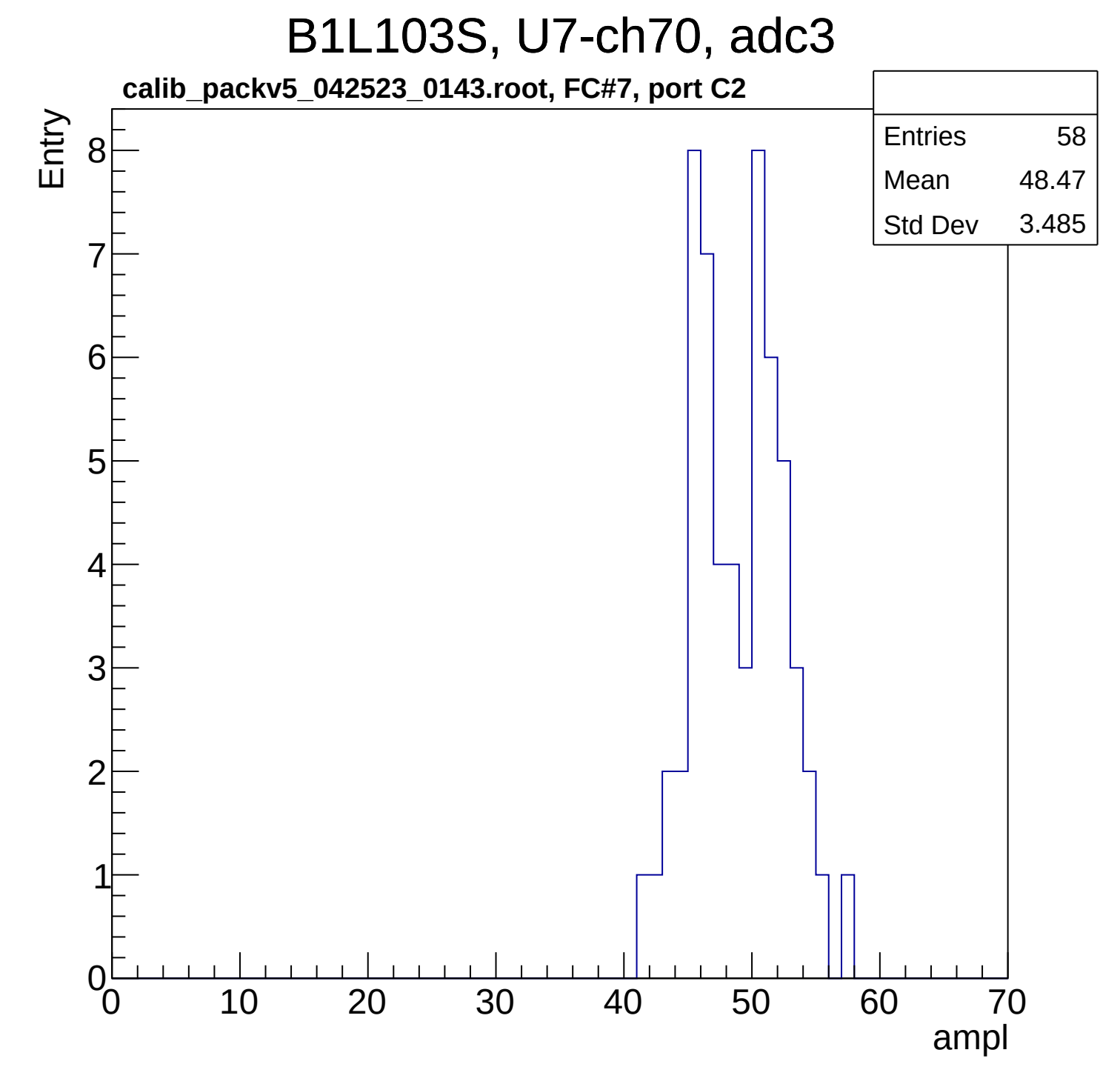
B1L103S, U7-ch70, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 58
Mean 48.47
Std Dev 3.485
Entry
ampl
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1
2
3
4
5
6
7
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0
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40
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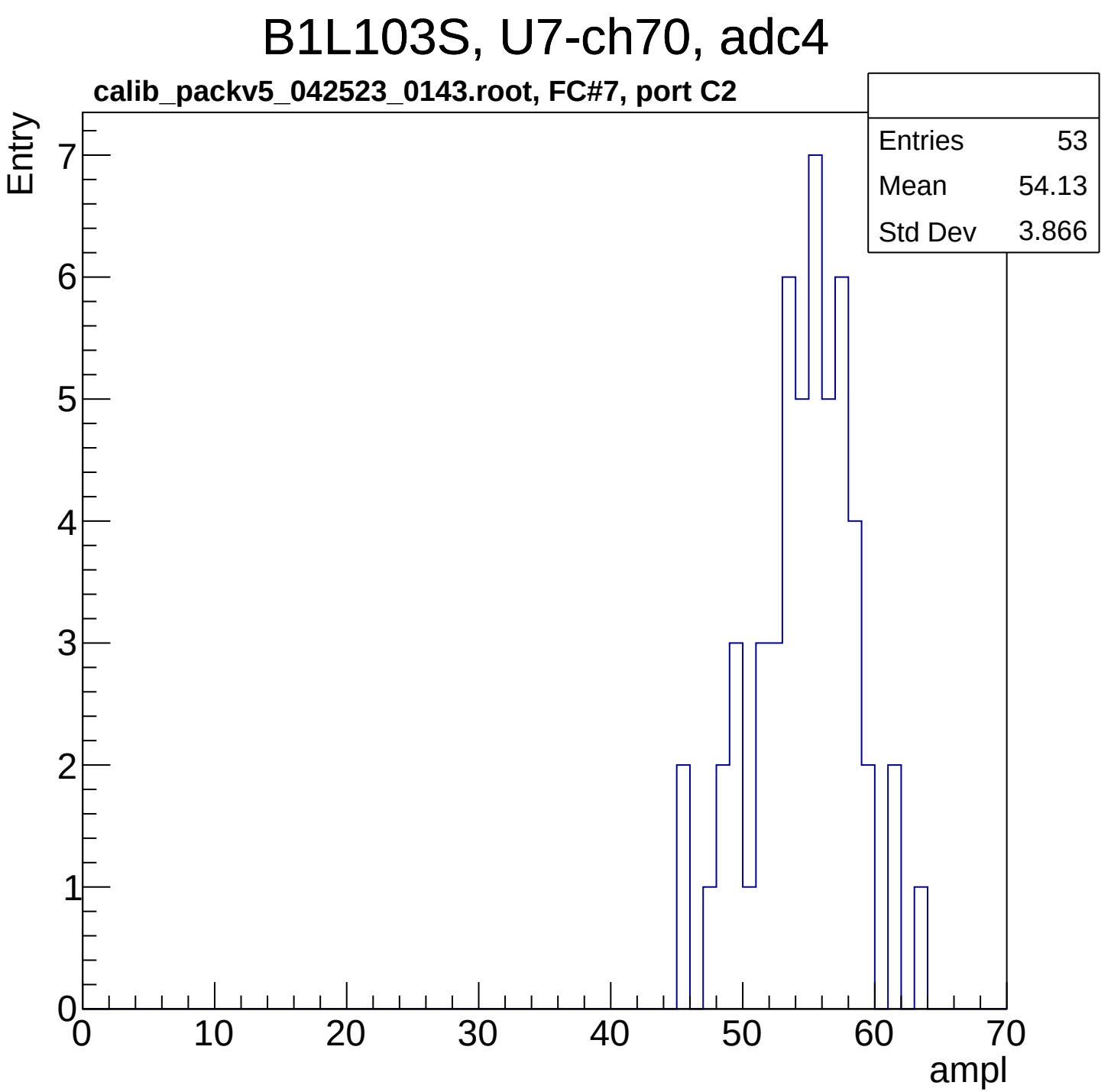
60
70


B1L103S, U7-ch70, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 54.13
Std Dev 3.866
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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50
60
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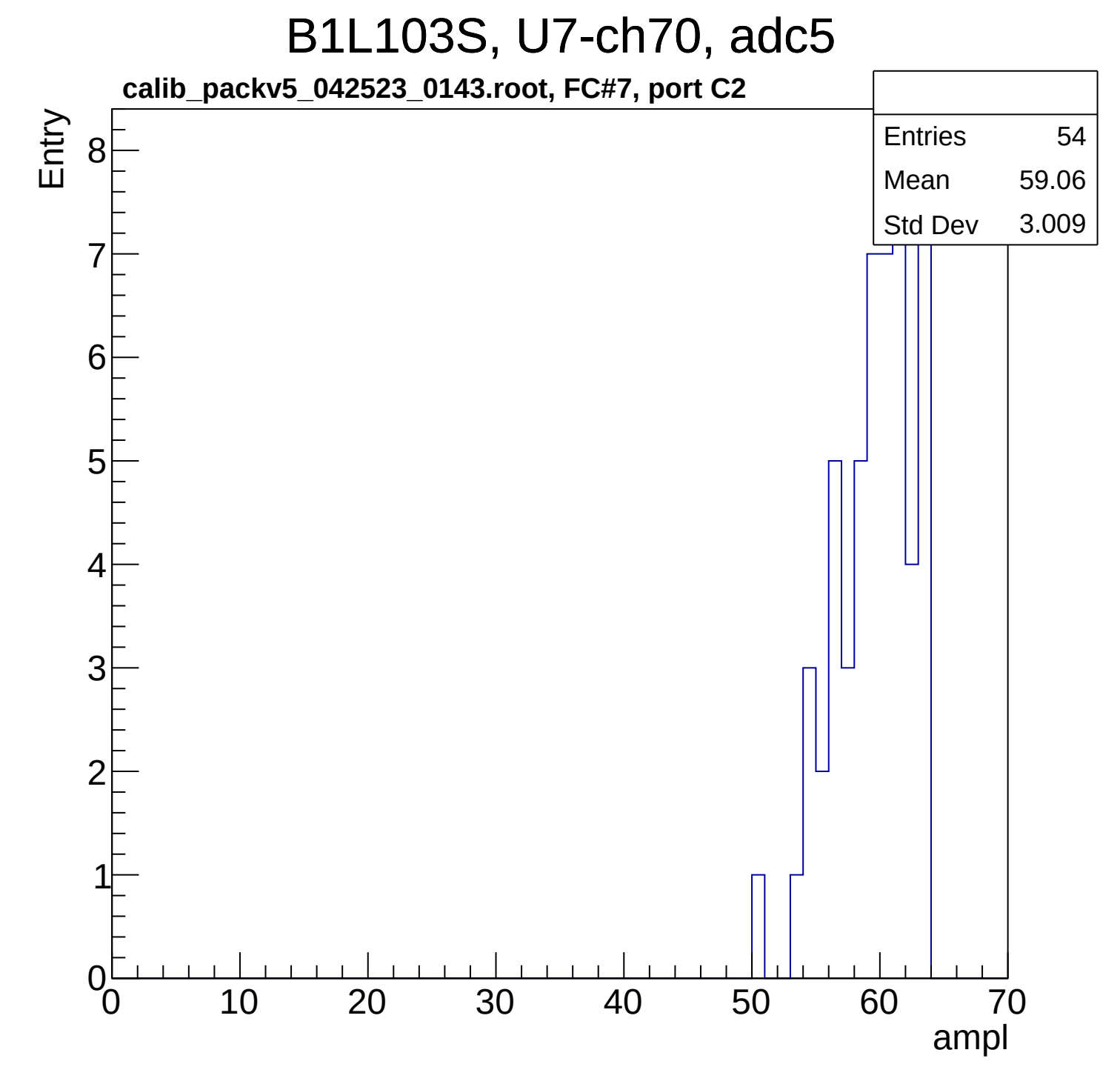
B1L103S, U7-ch70, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 54
Mean 59.06
Std Dev 3.009
Entry
ampl
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1
2
3
4
5
6
7
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0
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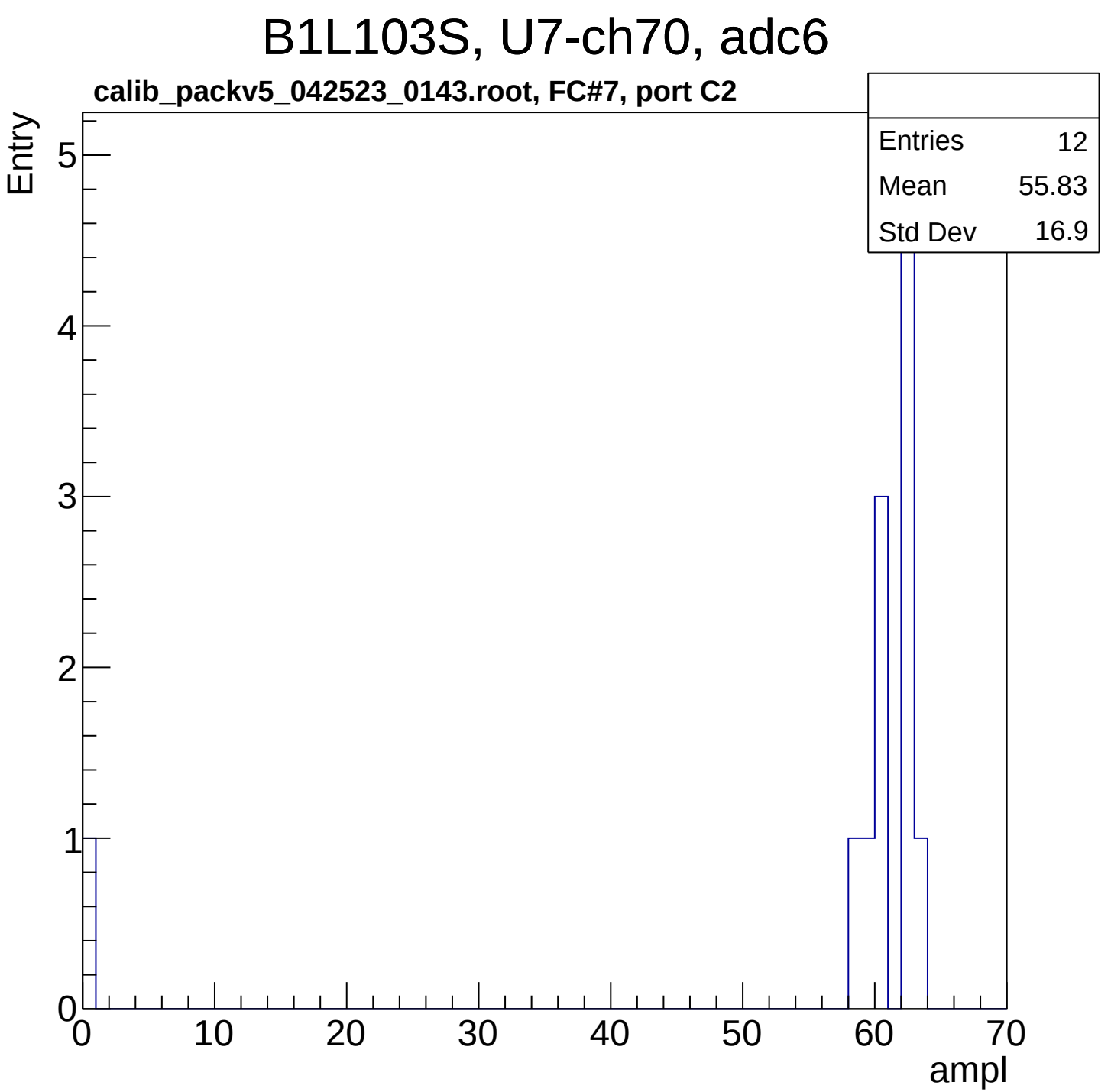
B1L103S, U7-ch70, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 12
Mean 55.83
Std Dev 16.9
Entry
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2
3
4
5
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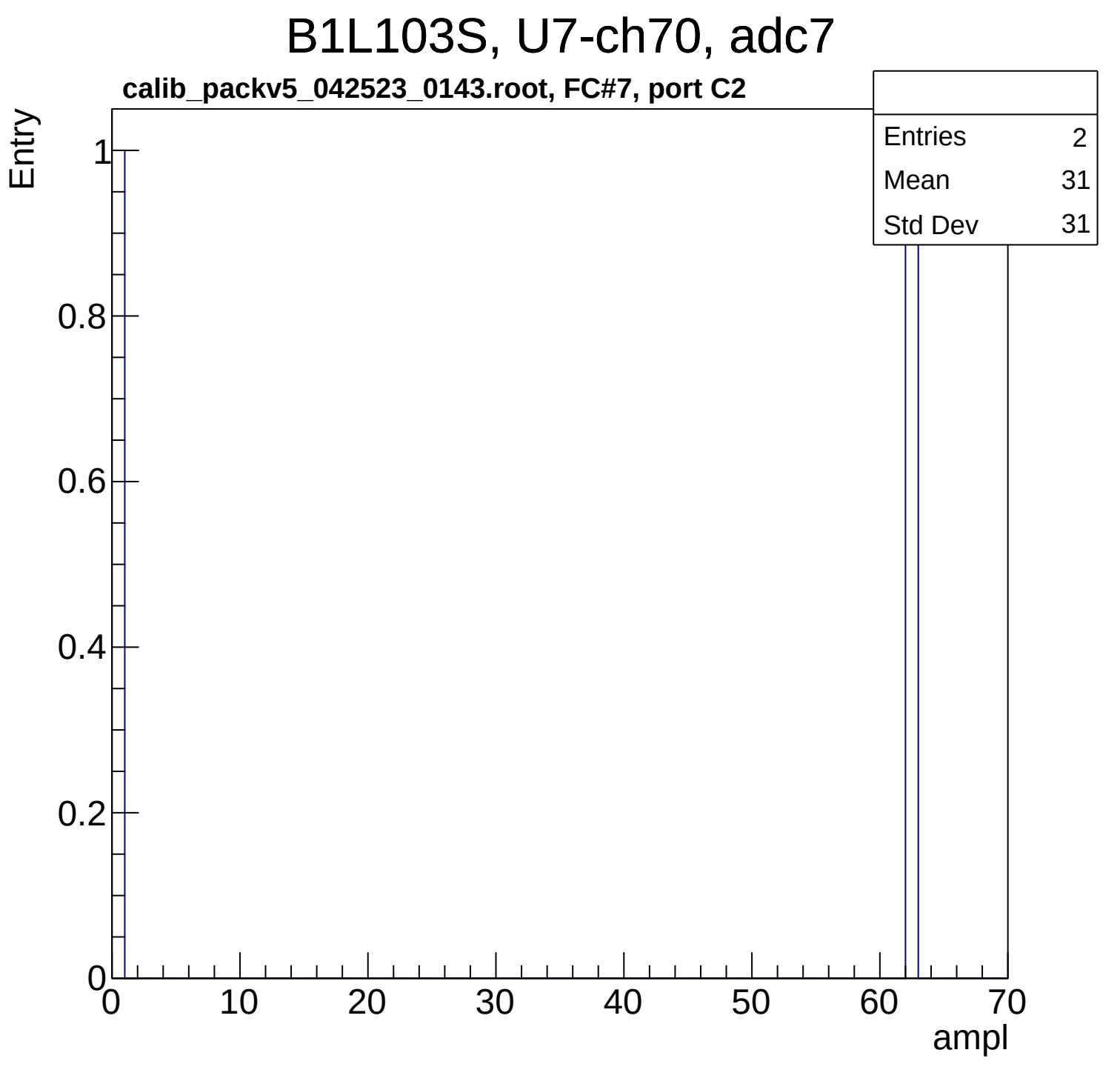
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch70, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 31
Std Dev 31
Entry
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0.6
0.4
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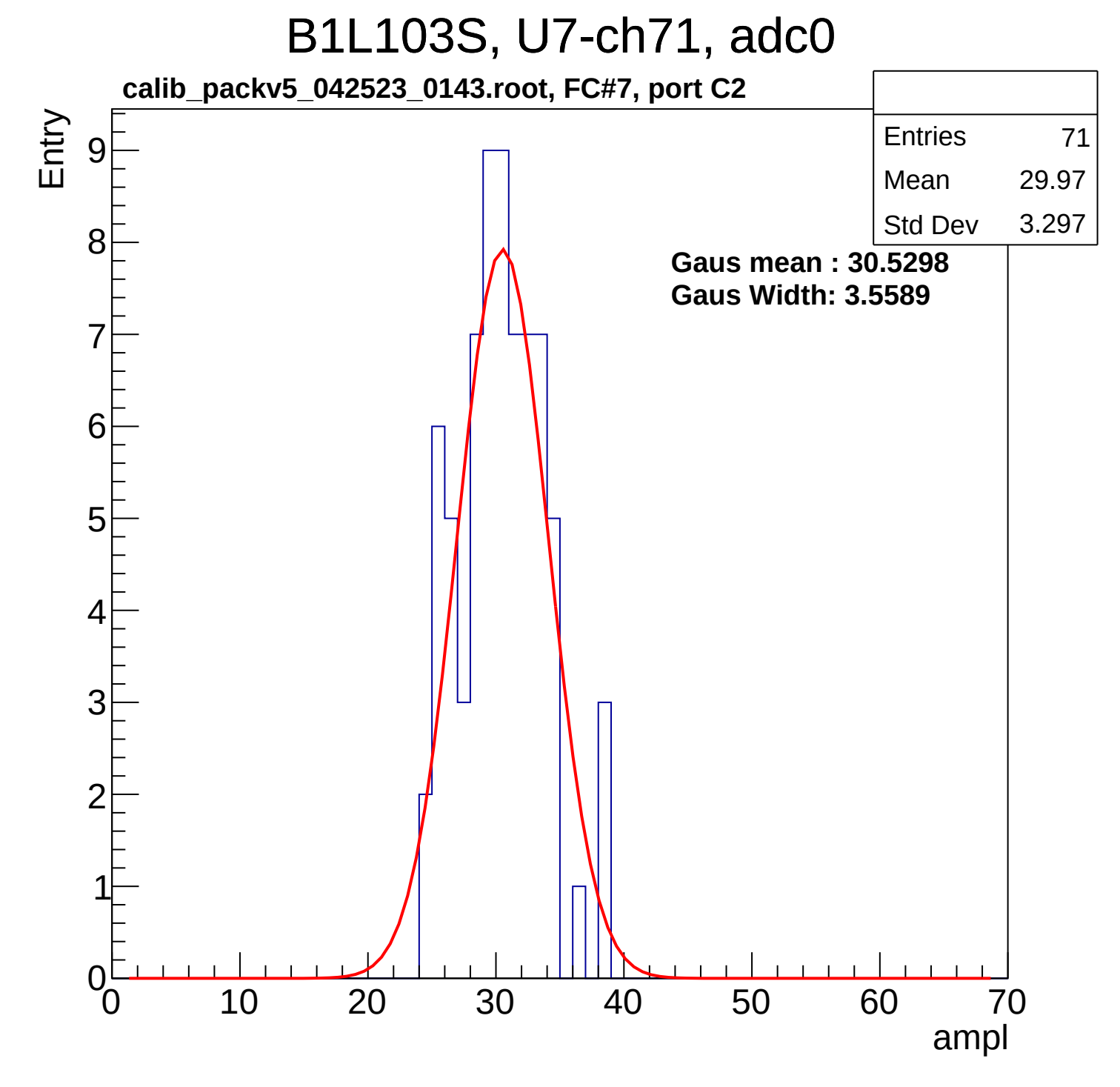
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch71, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 71
Mean 29.97
Std Dev 3.297
Gaus mean : 30.5298
Gaus Width: 3.5589
Entry
ampl
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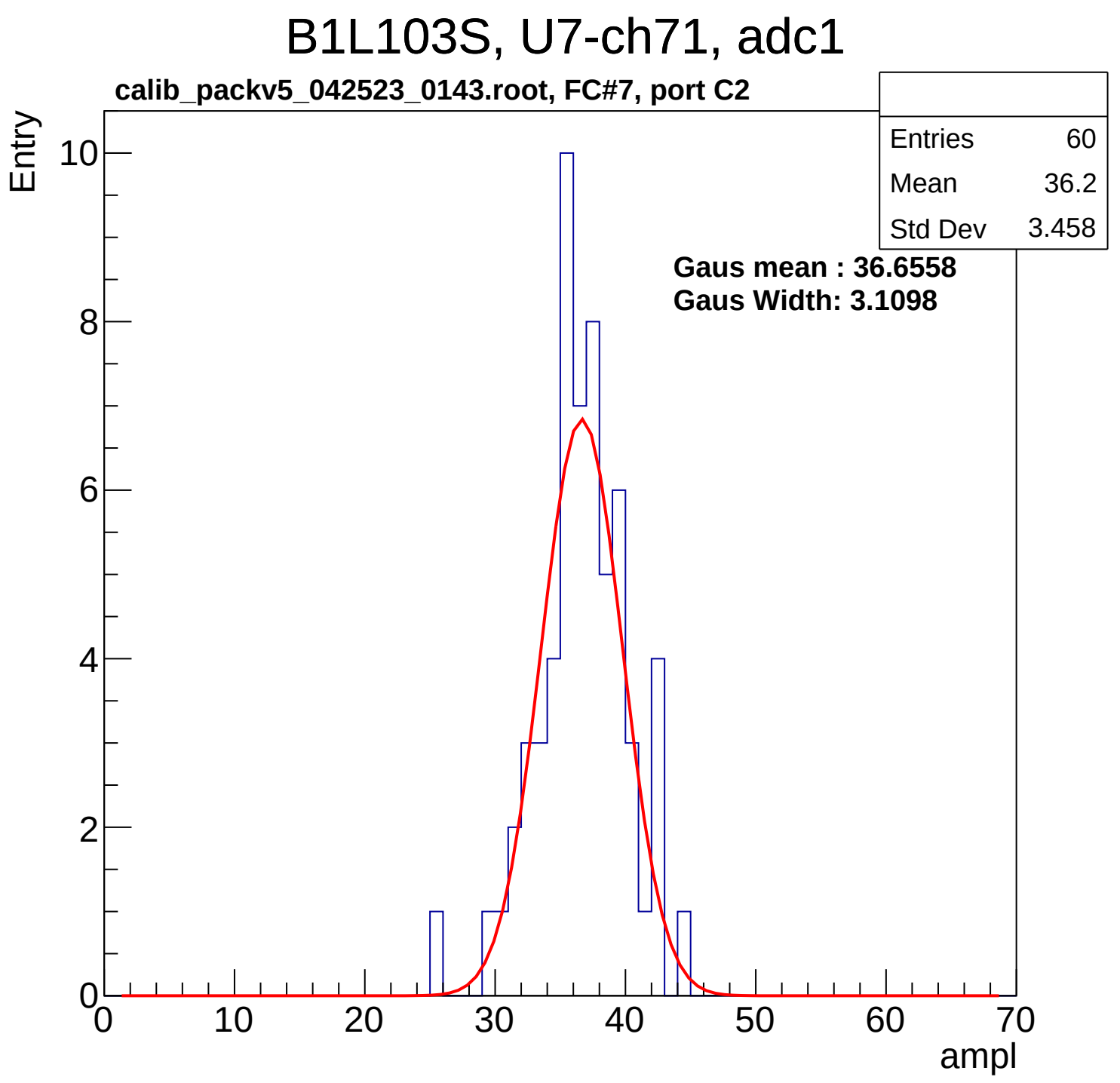
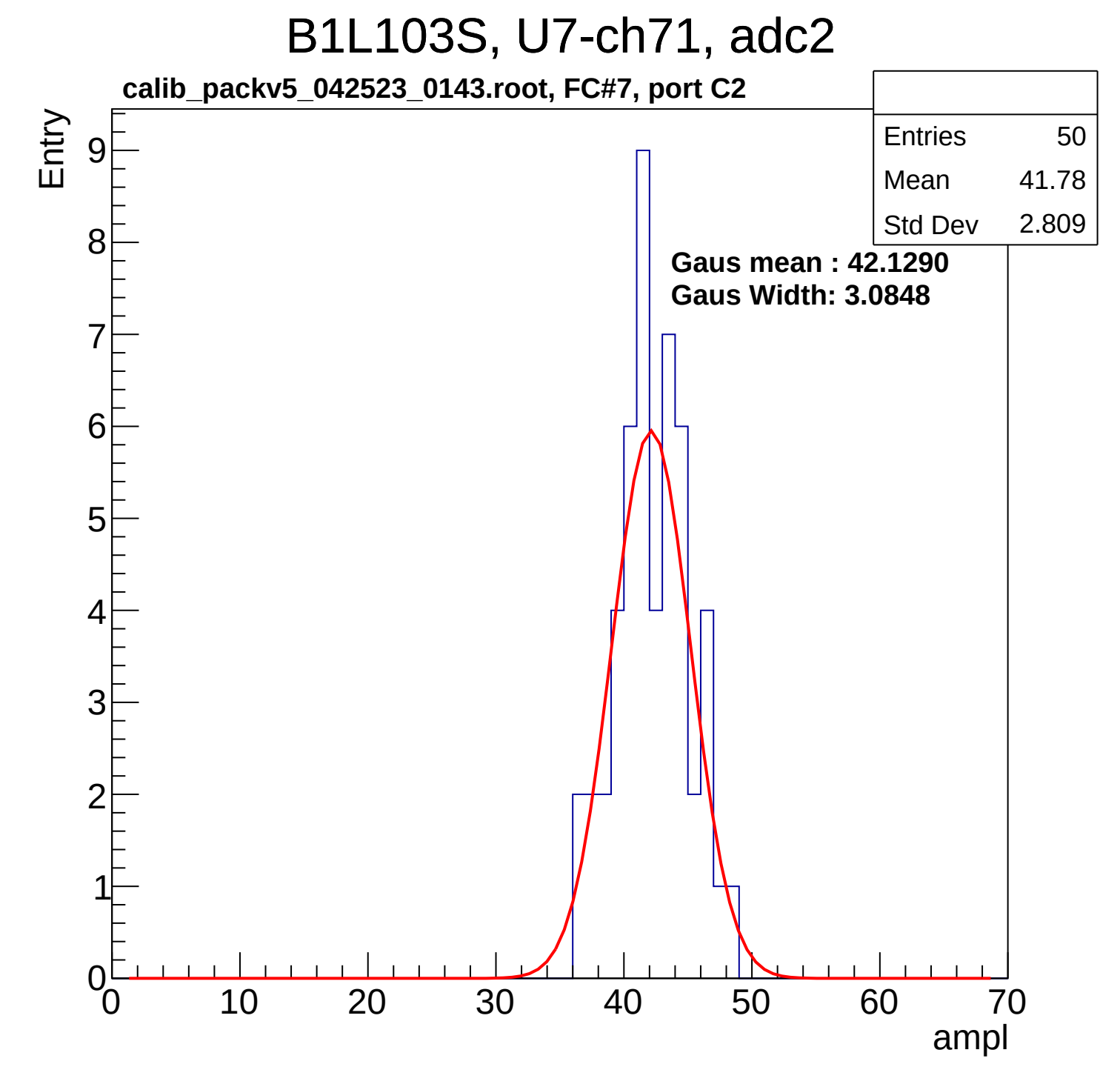
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch71, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 60
Mean 36.2
Std Dev 3.458
Gaus mean : 36.6558
Gaus Width: 3.1098
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch71, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 50
Mean 41.78
Std Dev 2.809
Gaus mean : 42.1290
Gaus Width: 3.0848
Entry
ampl
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1
2
3
4
5
6
7
8
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0
10
20
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40
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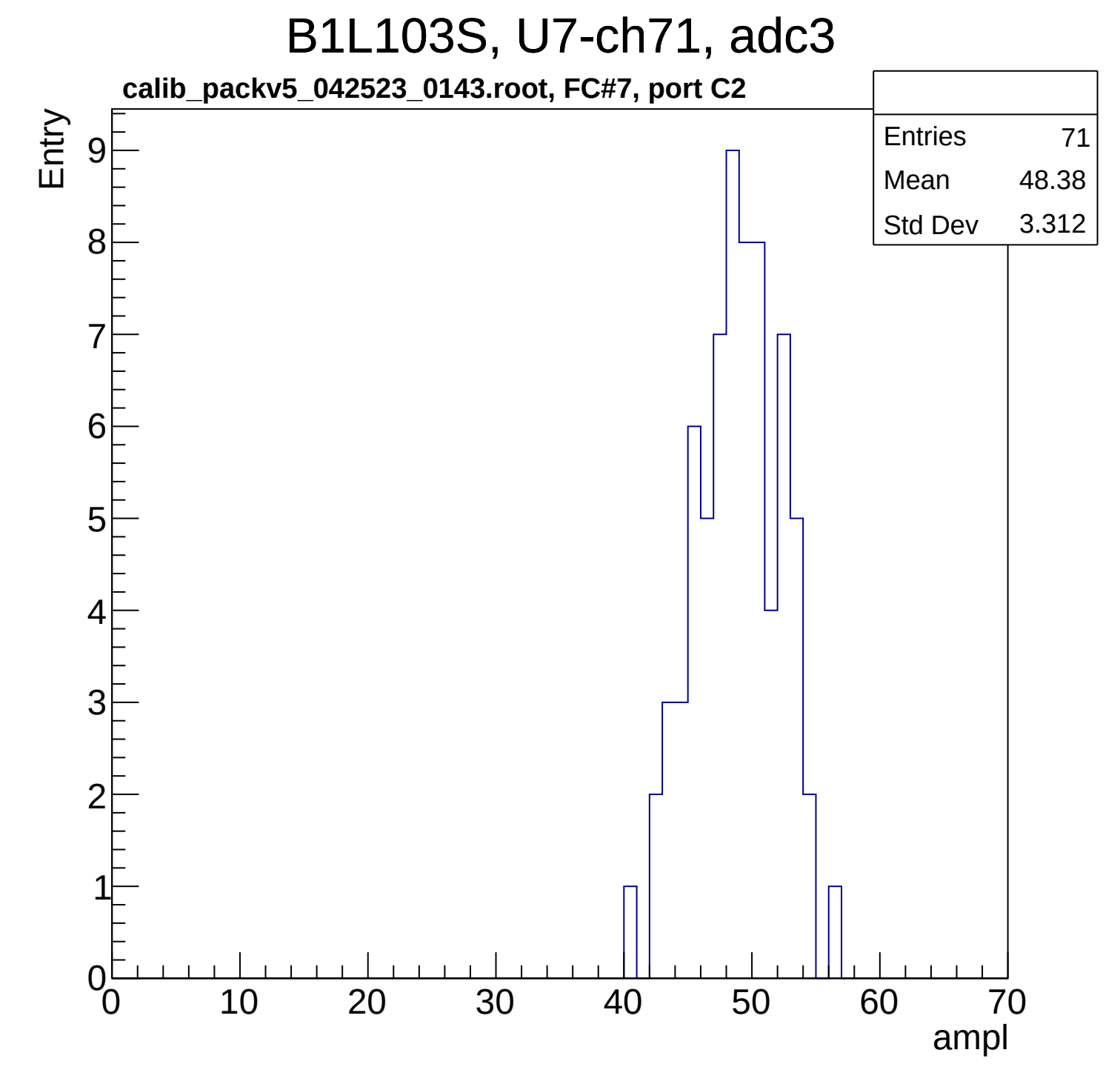
B1L103S, U7-ch71, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 71
Mean 48.38
Std Dev 3.312
Entry
ampl
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3
4
5
6
7
8
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0
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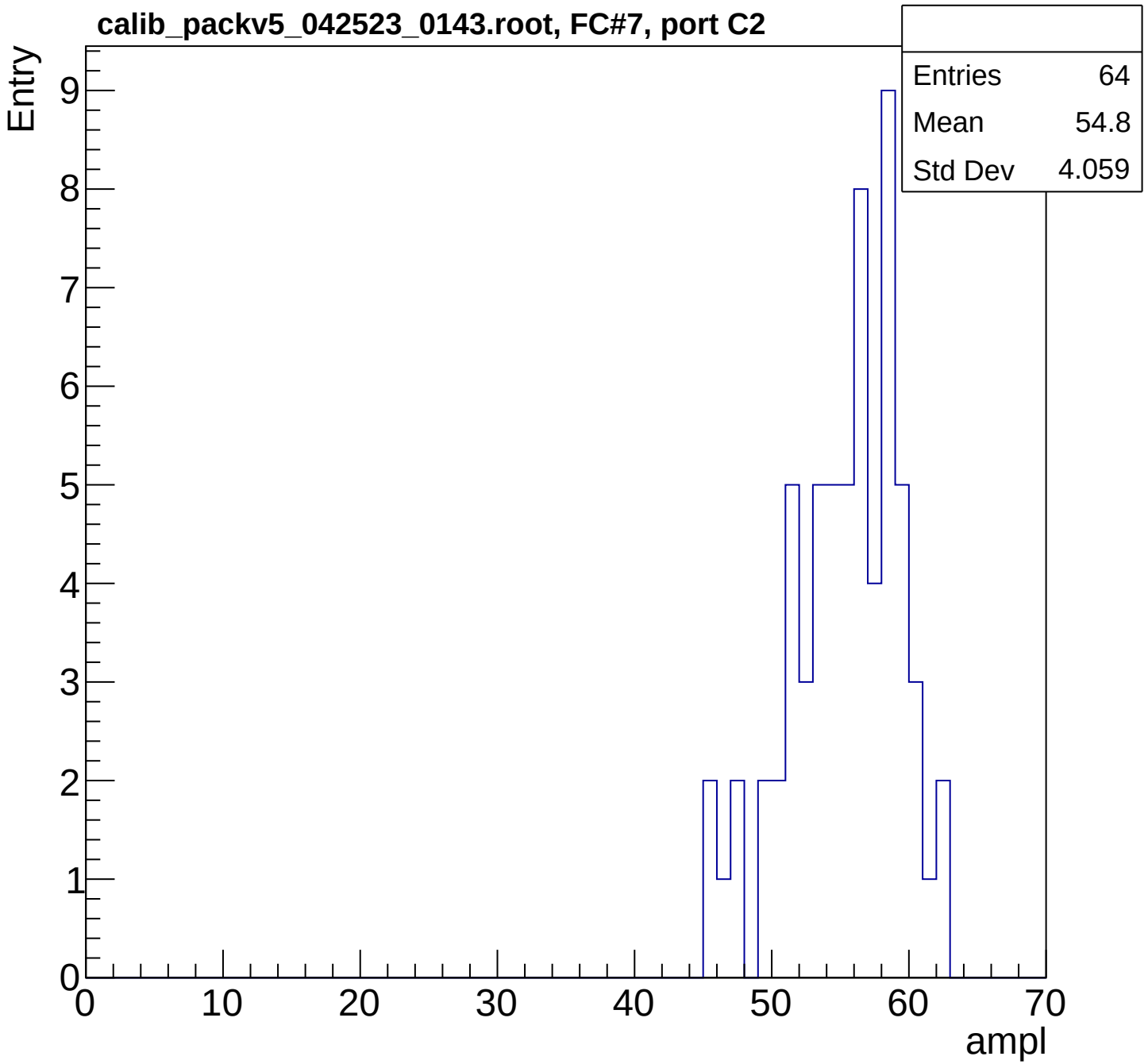
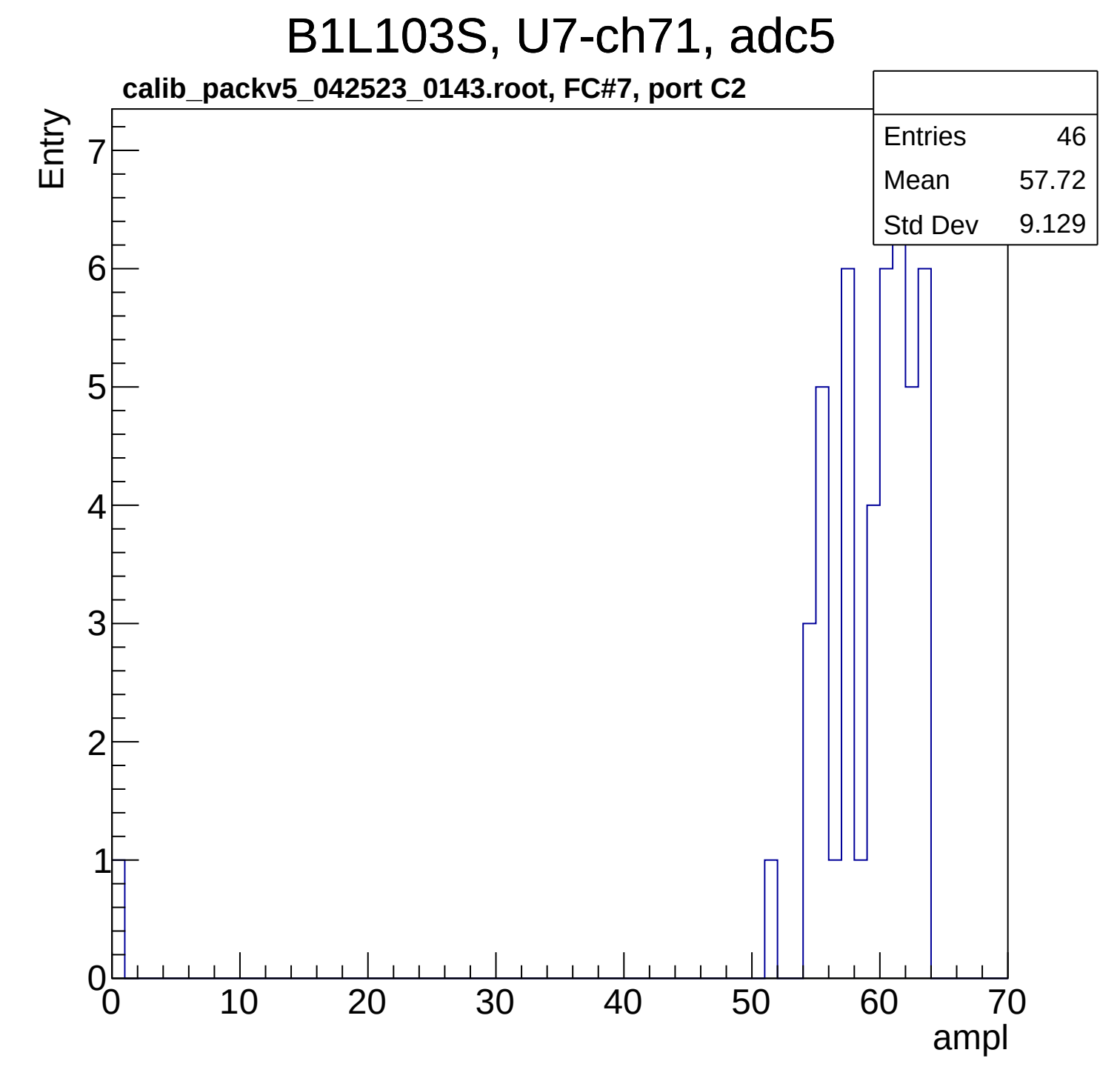

B1L103S, U7-ch71, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 54.8
Std Dev 4.059
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch71, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 46
Mean 57.72
Std Dev 9.129
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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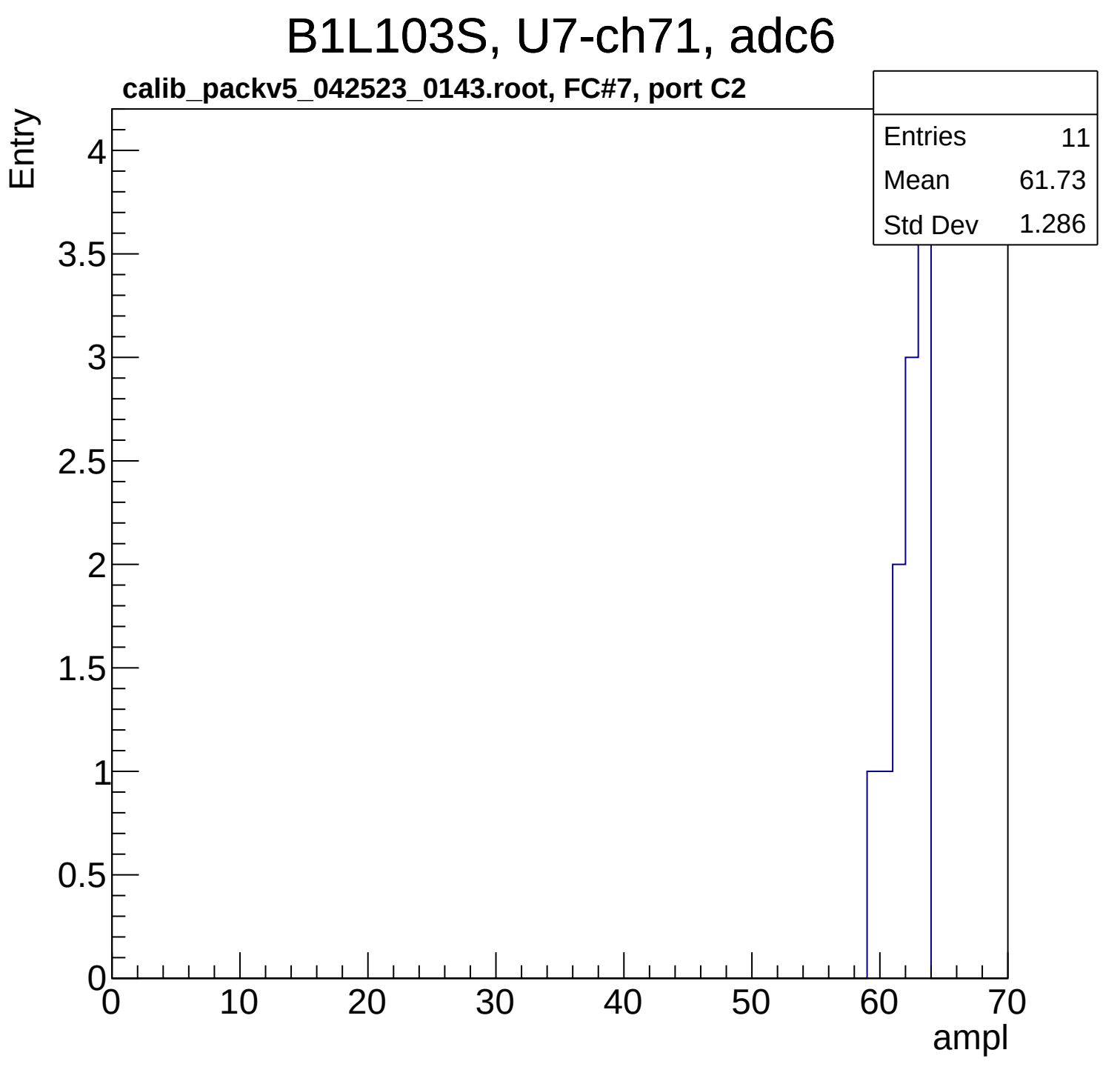
B1L103S, U7-ch71, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 11
Mean 61.73
Std Dev 1.286
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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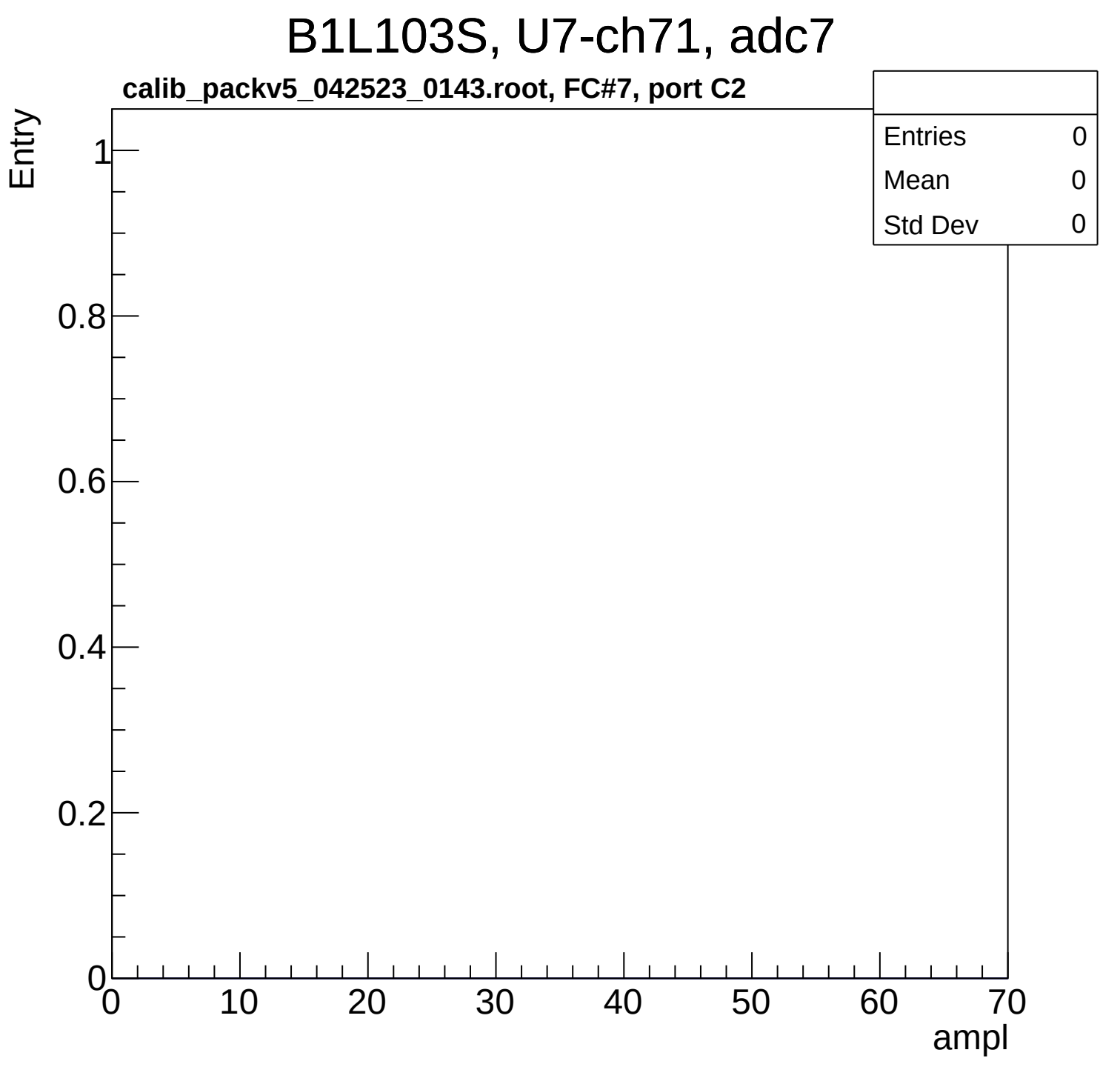
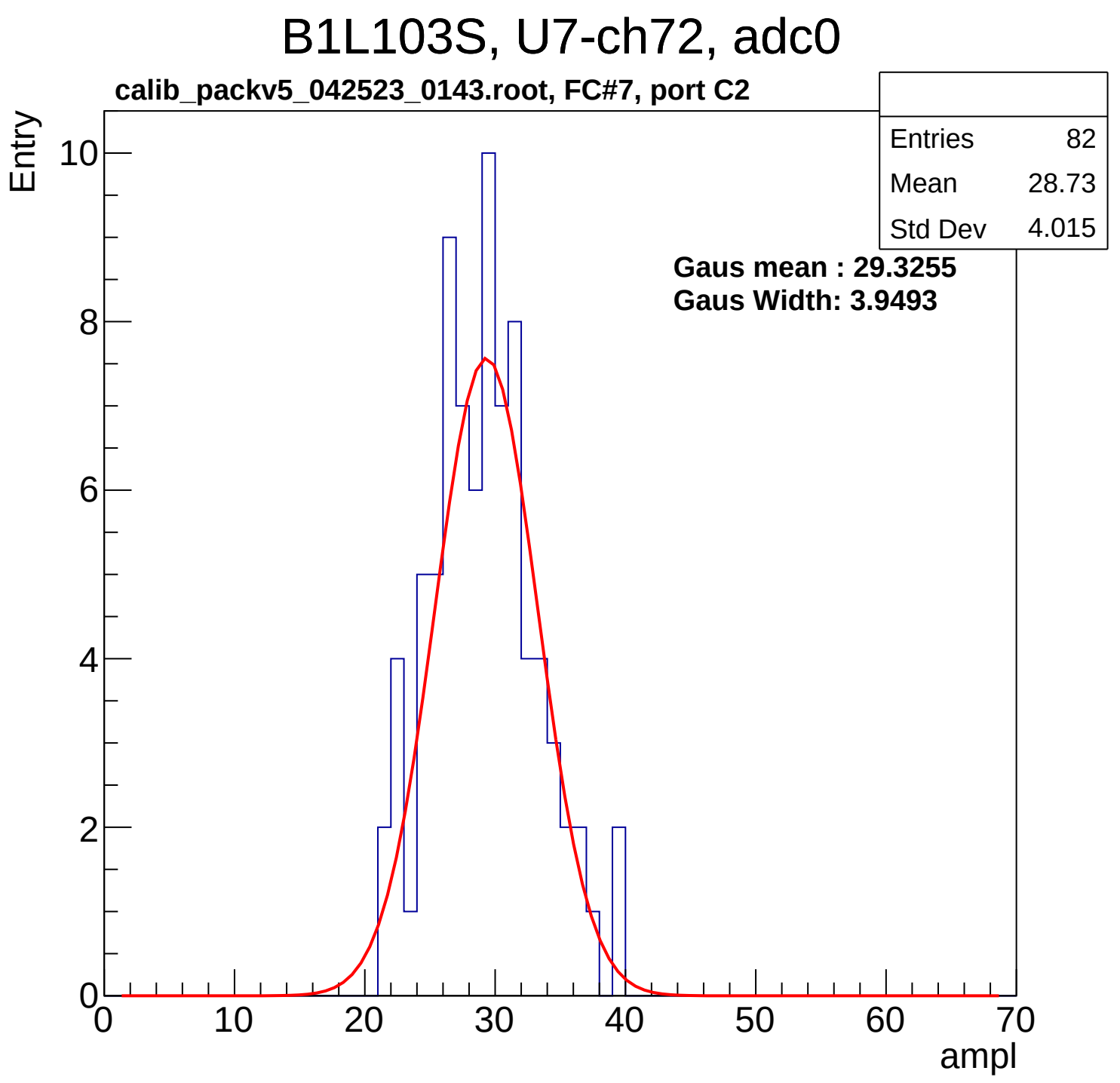
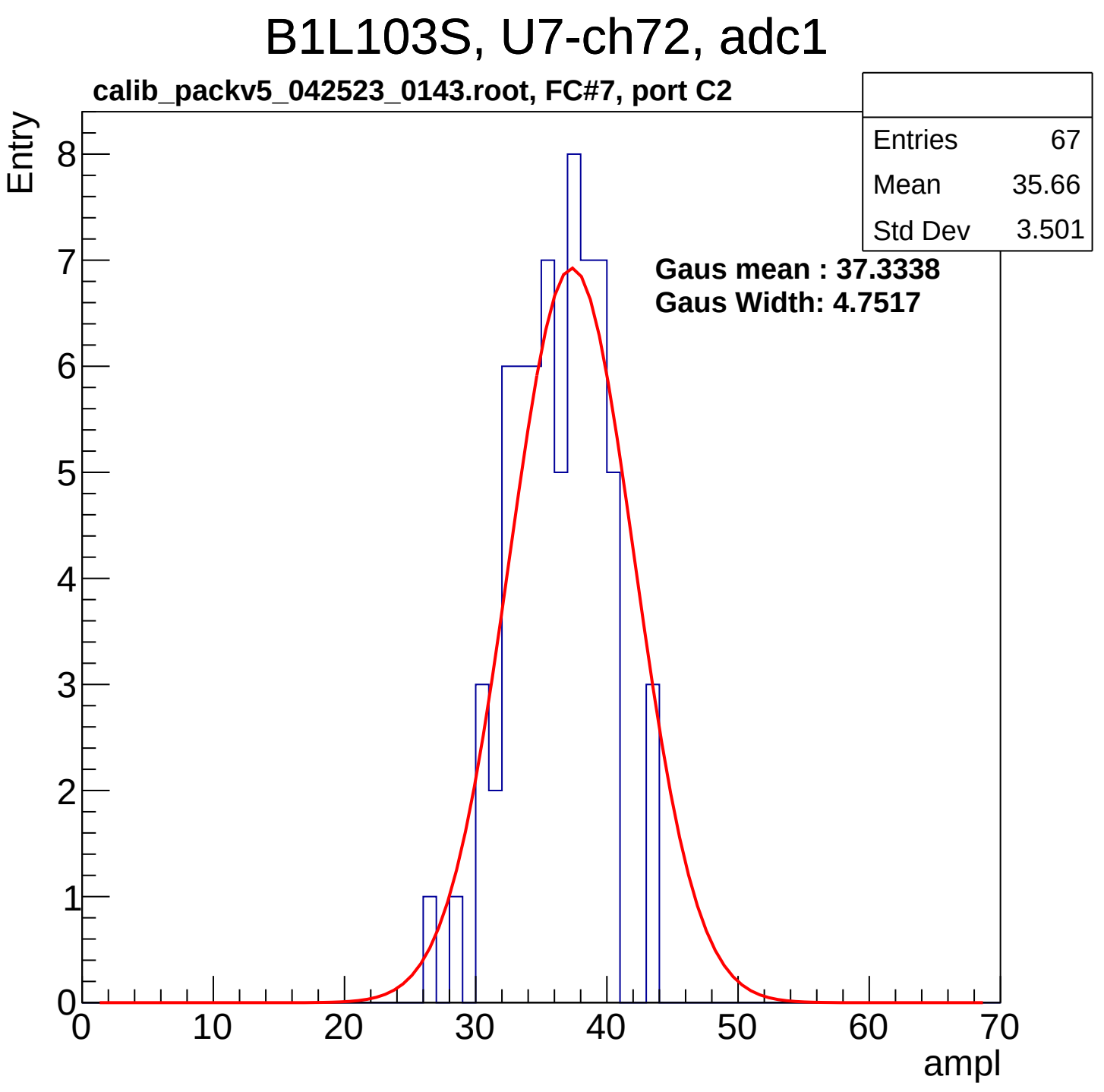
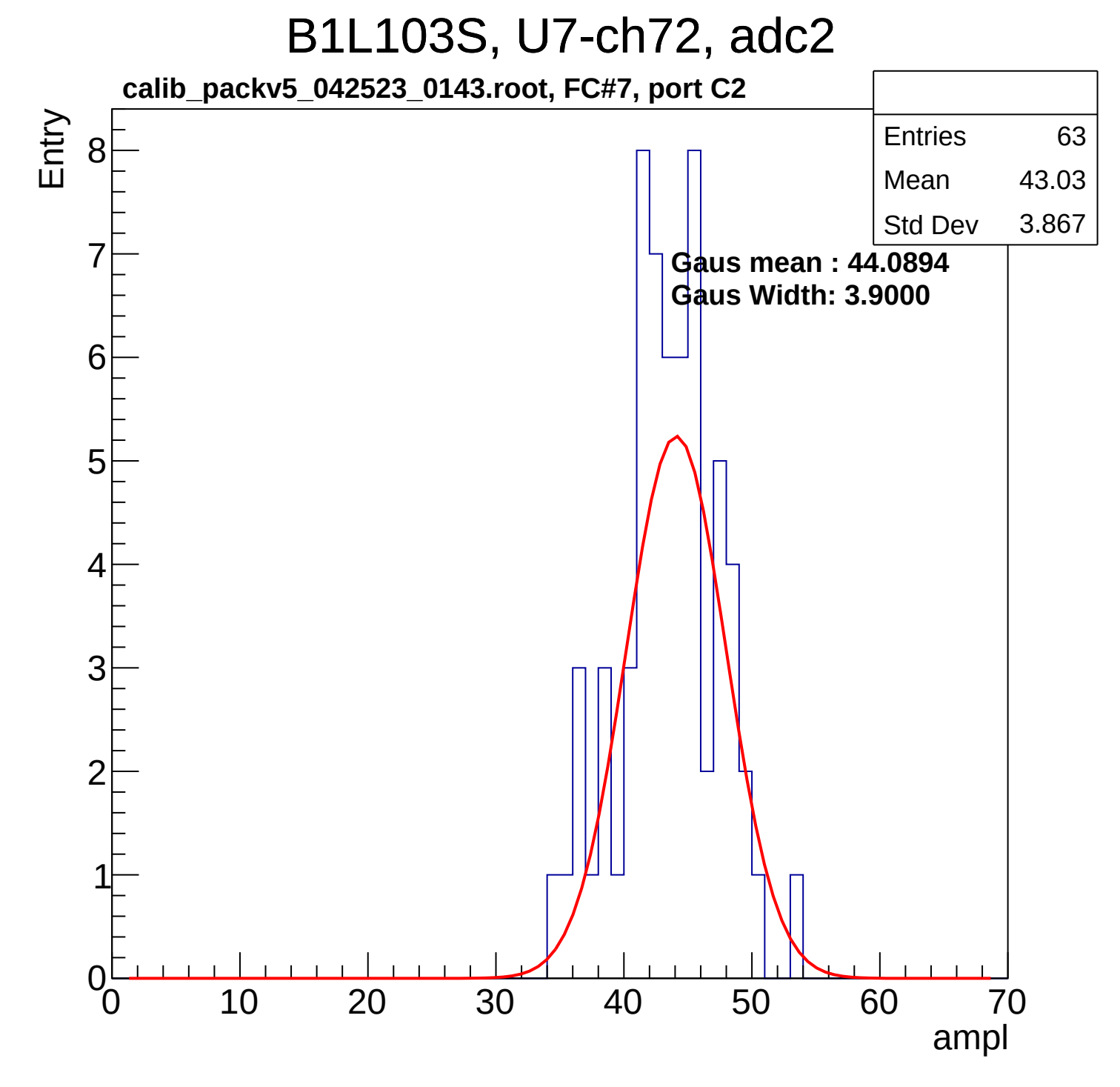
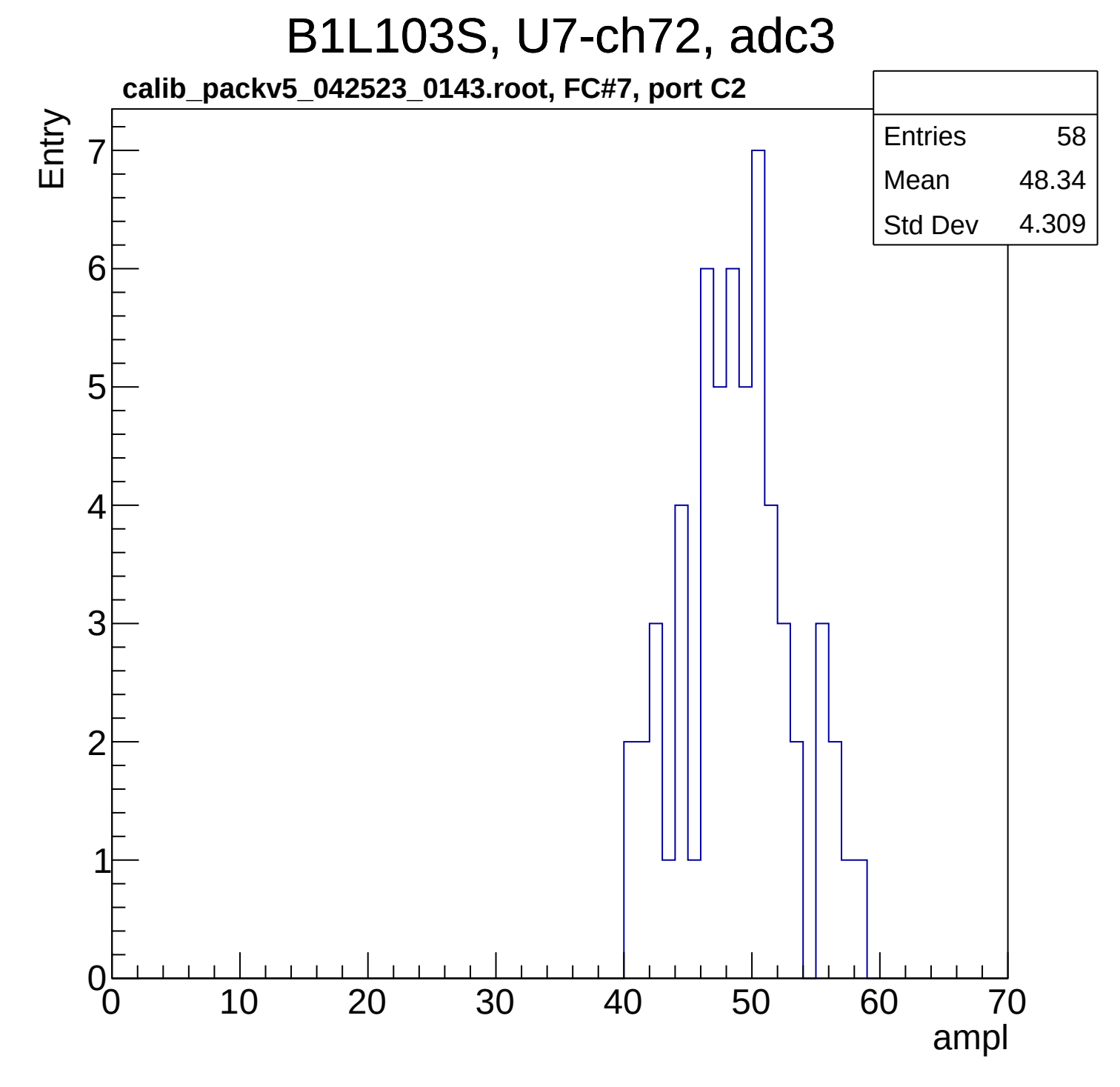
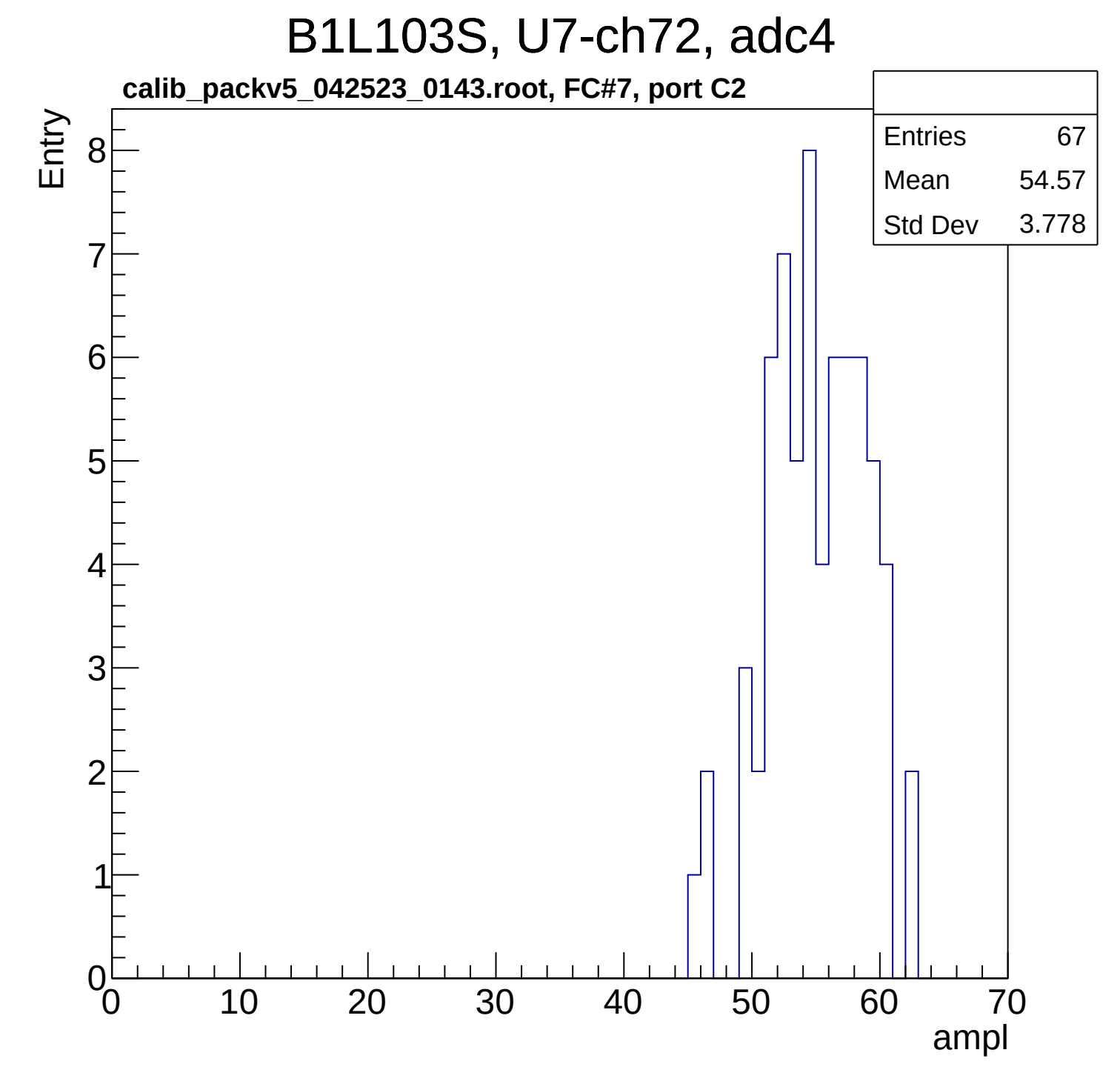

B1L103S, U7-ch71, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch72, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 82
Mean 28.73
Std Dev 4.015
Gaus mean : 29.3255
Gaus Width: 3.9493
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch72, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 35.66
Std Dev 3.501
Gaus mean : 37.3338
Gaus Width: 4.7517
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch72, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 43.03
Std Dev 3.867
Gaus mean : 44.0894
Gaus Width: 3.9000
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch72, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 58
Mean 48.34
Std Dev 4.309
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch72, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 54.57
Std Dev 3.778
Entry
ampl
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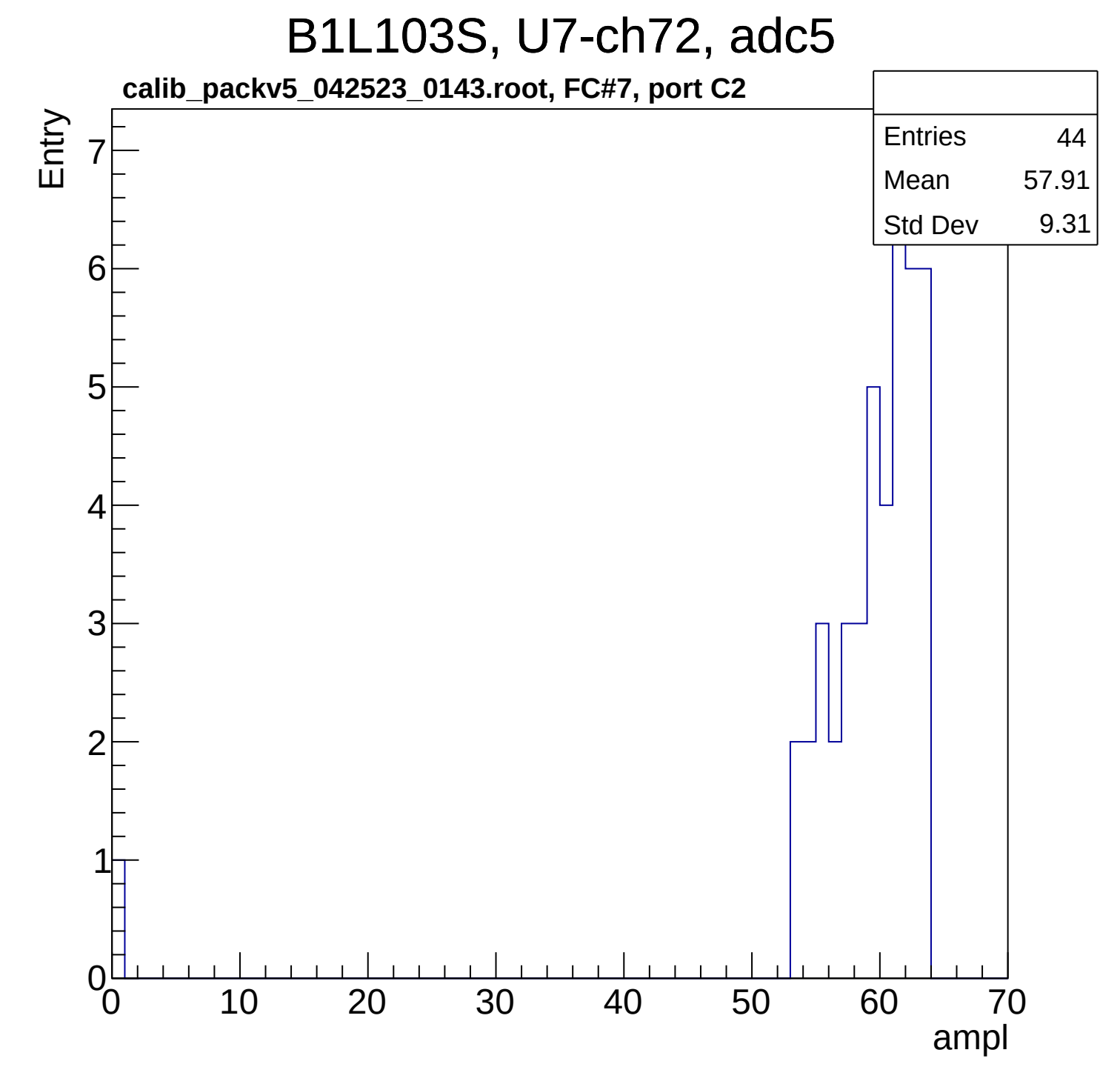
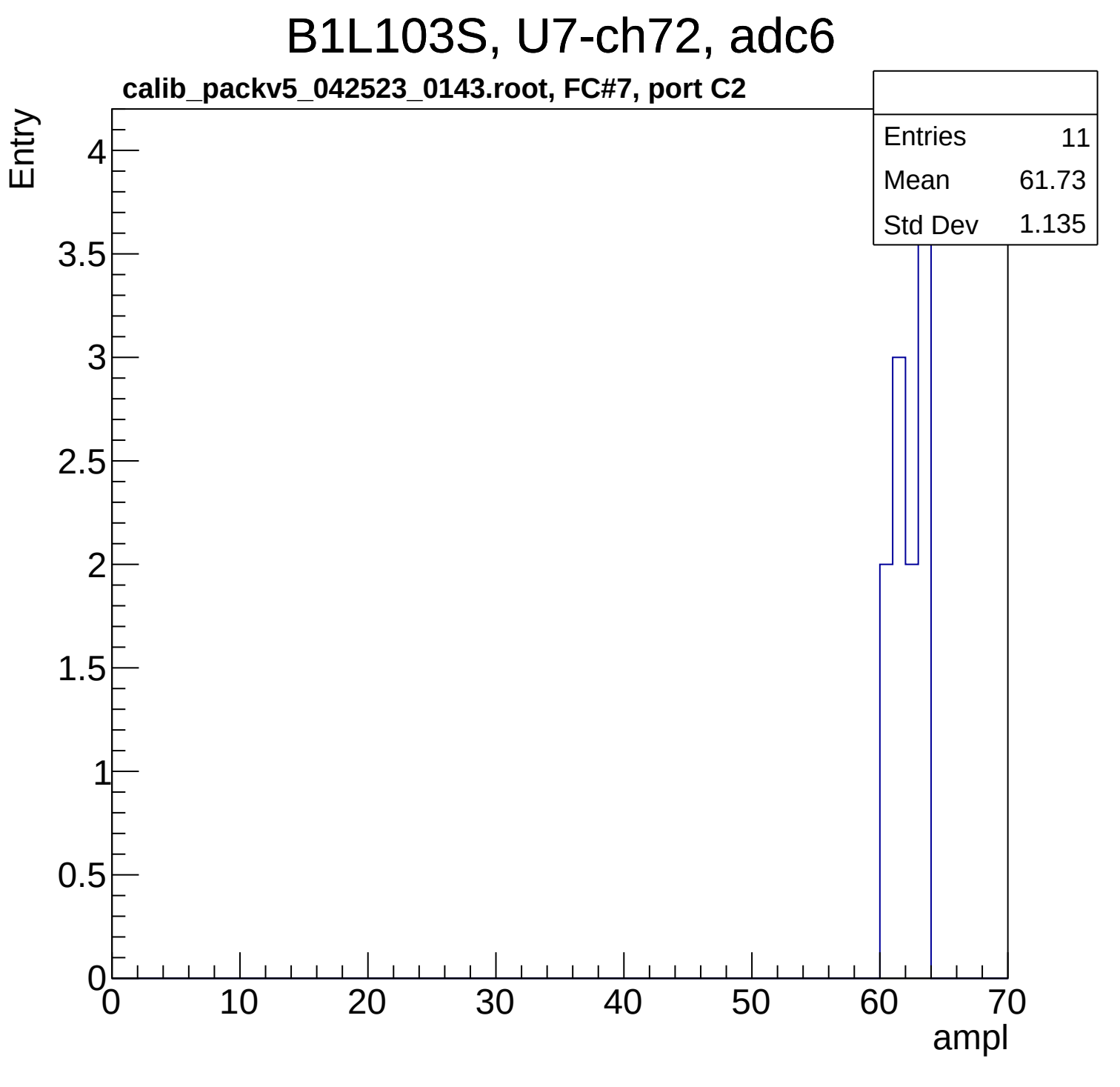
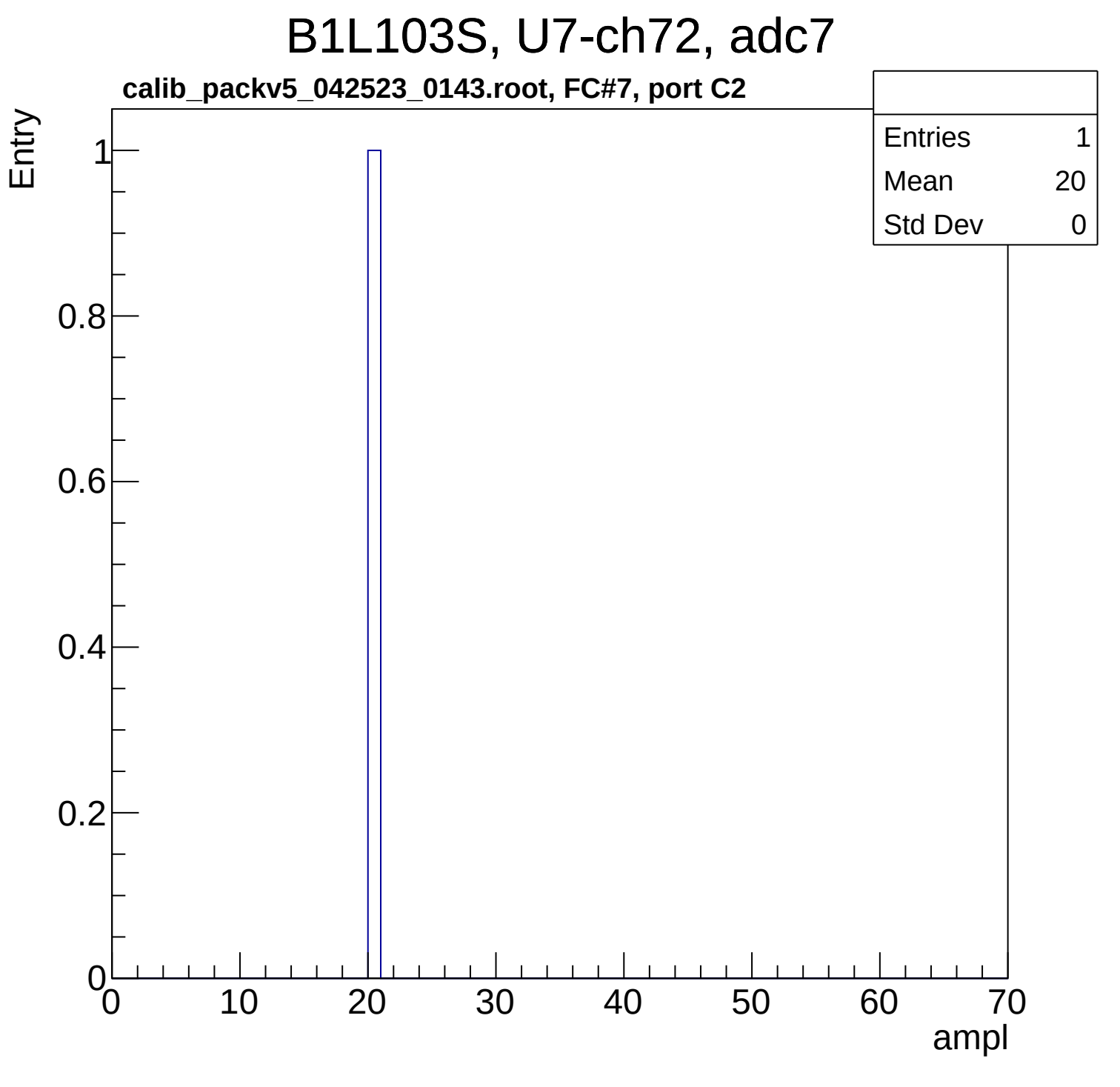
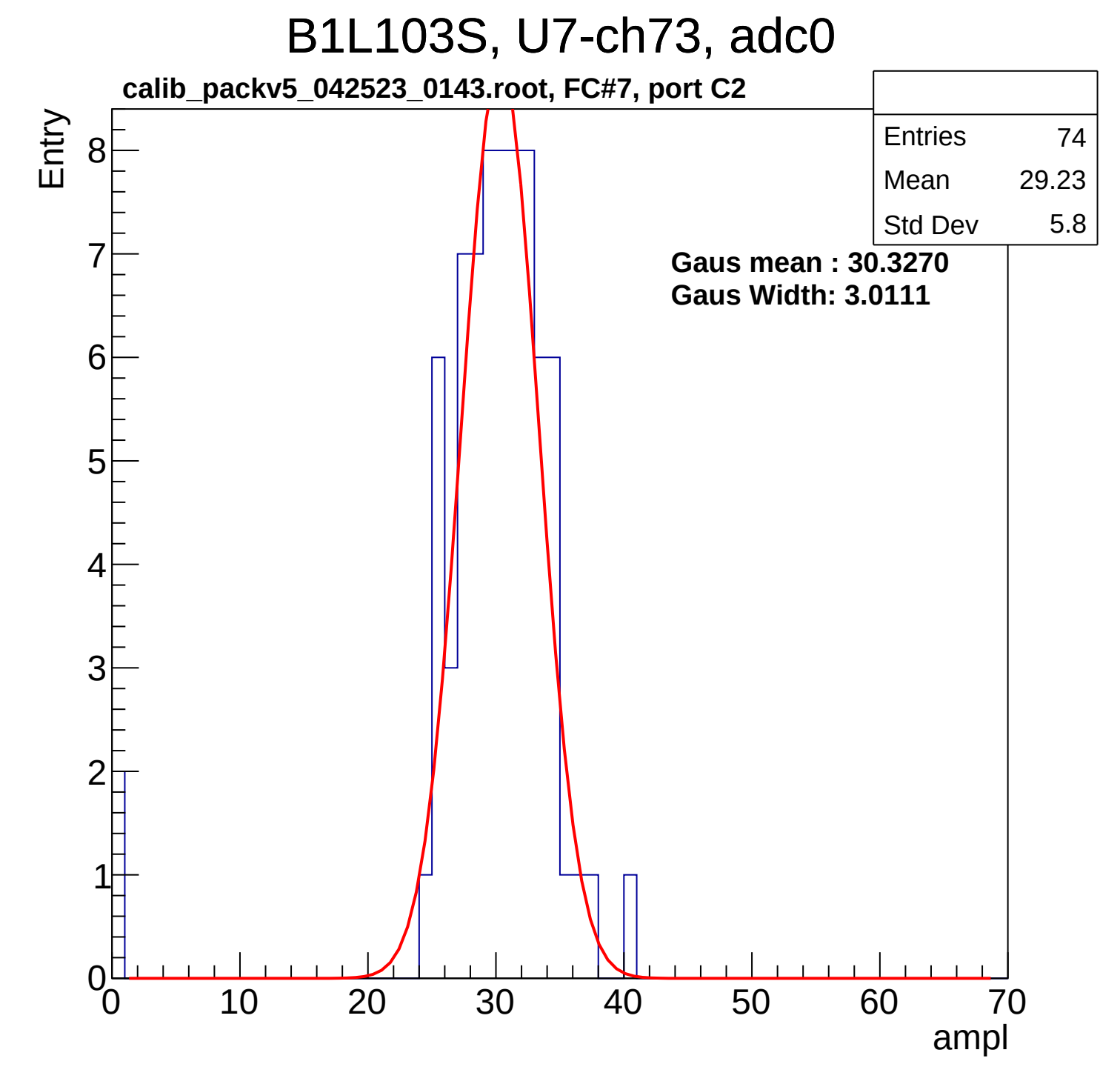
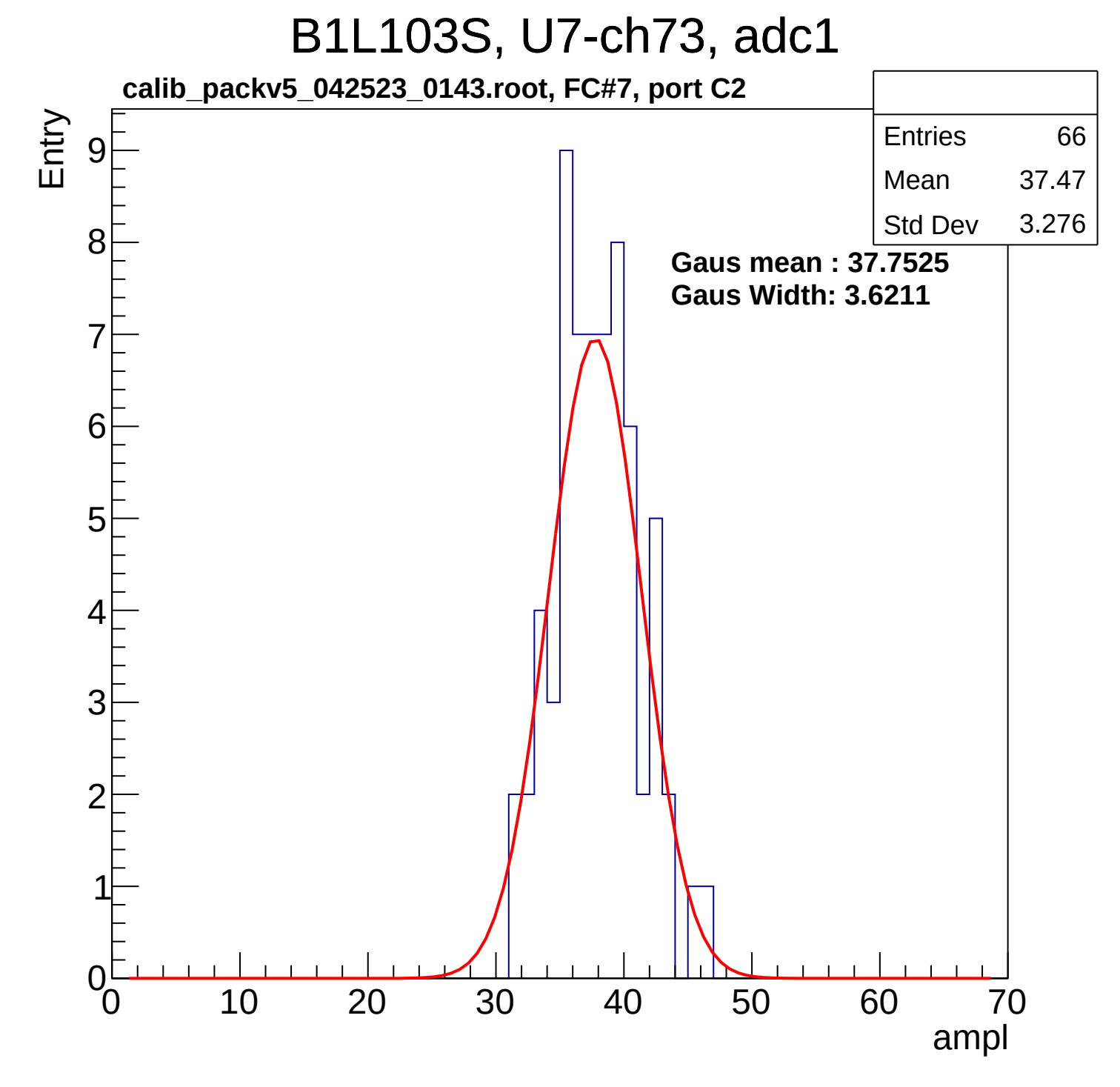
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

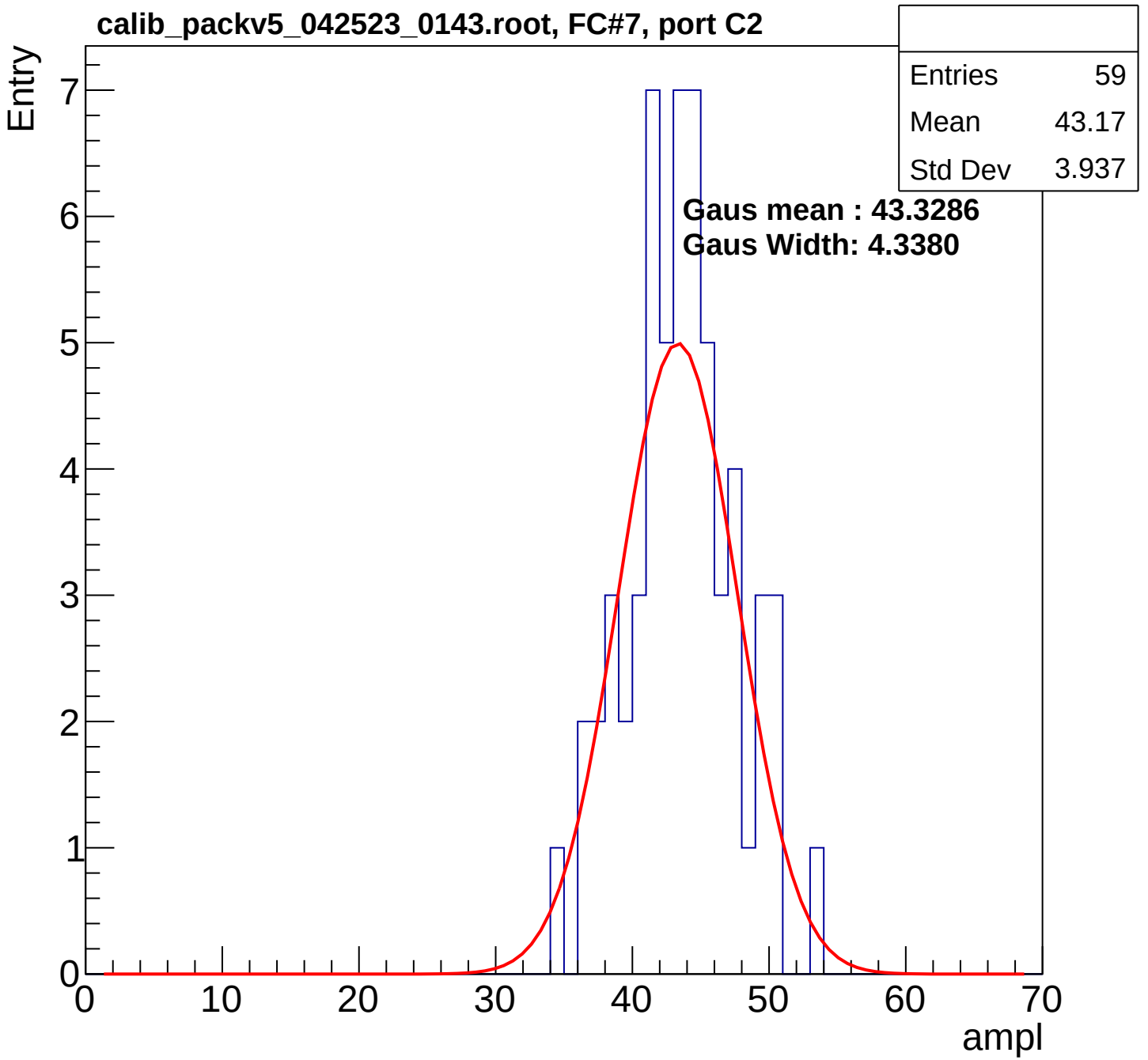

B1L103S, U7-ch72, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 44
Mean 57.91
Std Dev 9.31
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

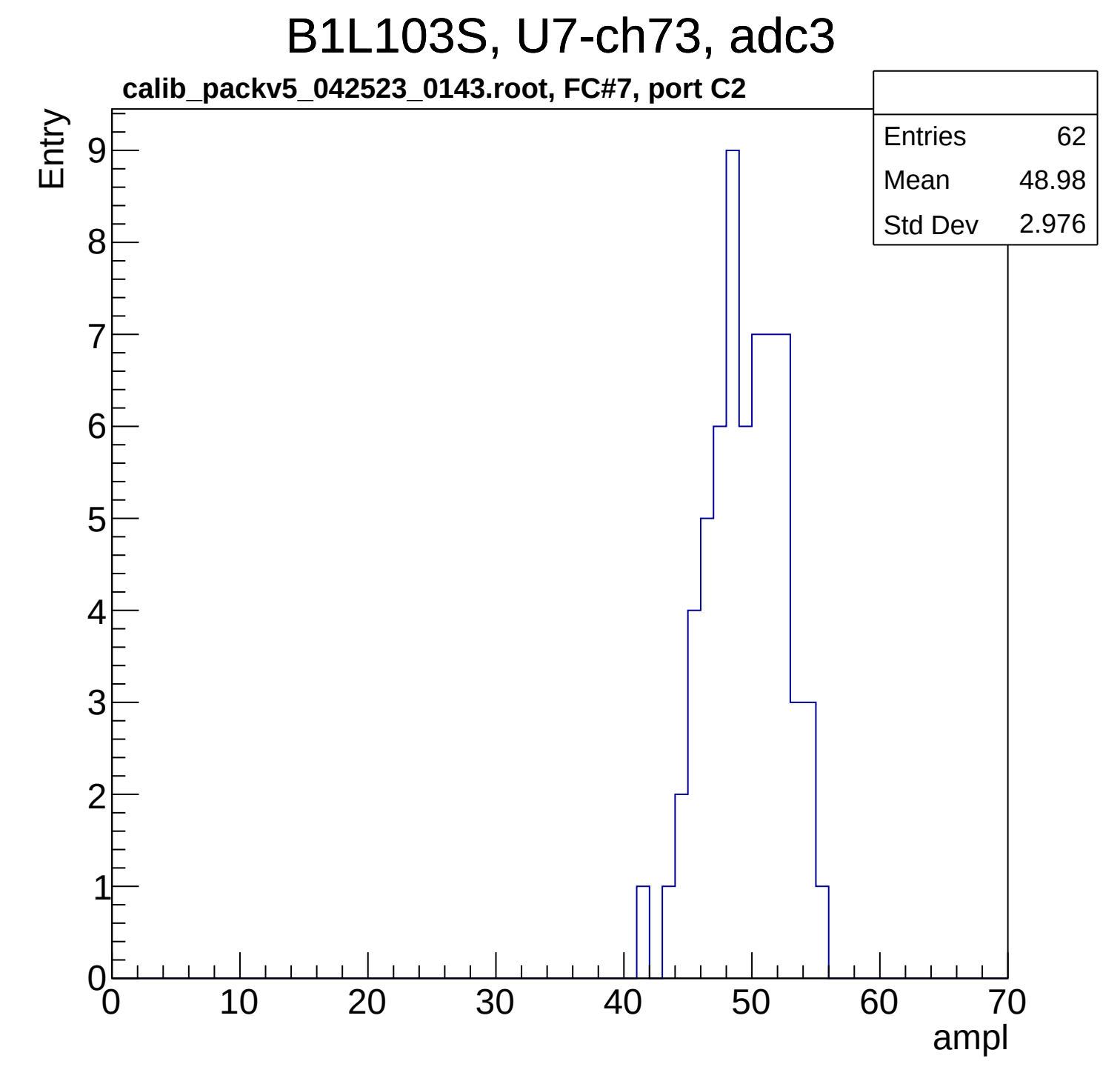

B1L103S, U7-ch72, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 11
Mean 61.73
Std Dev 1.135
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

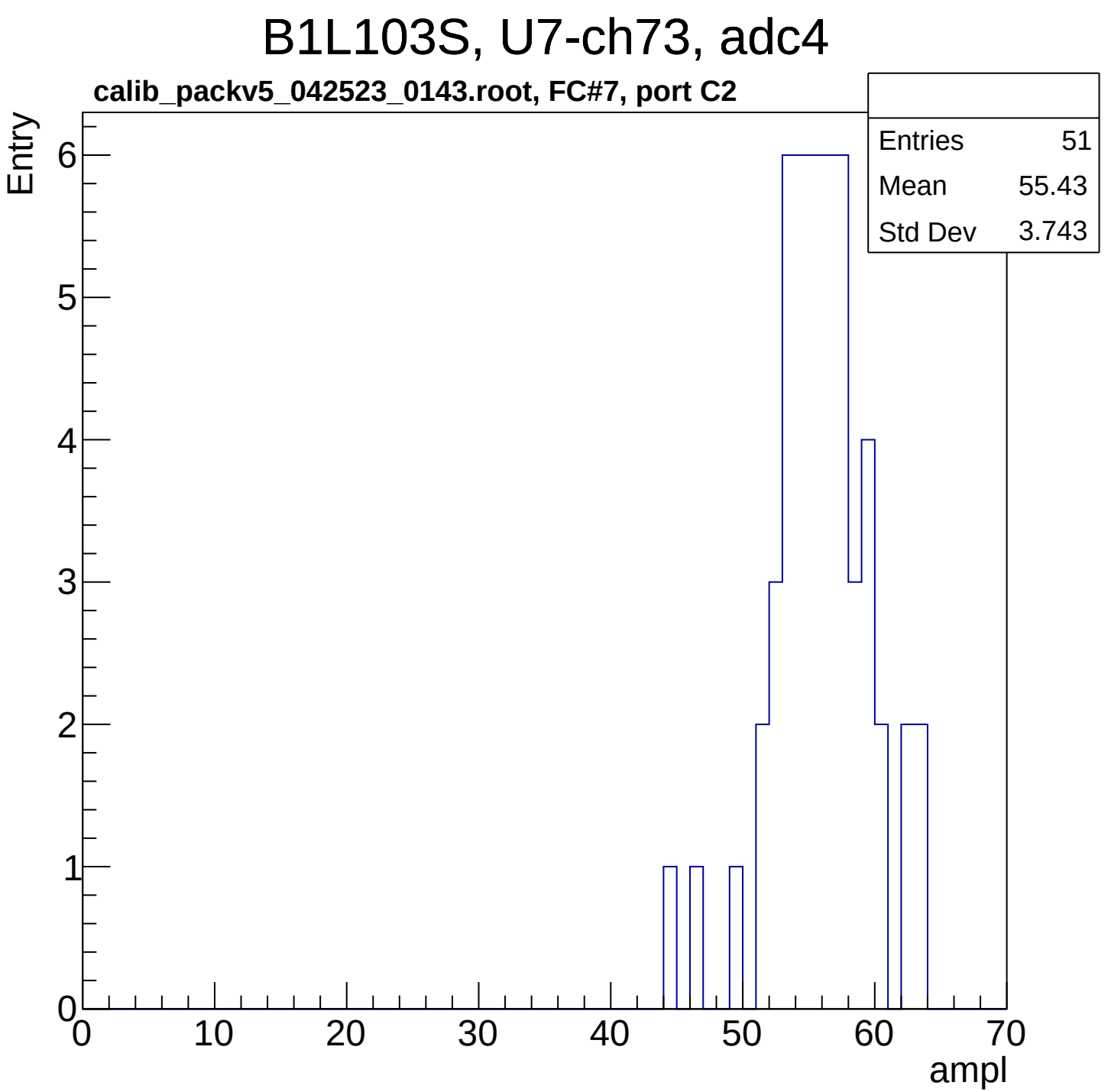

B1L103S, U7-ch72, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 20
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

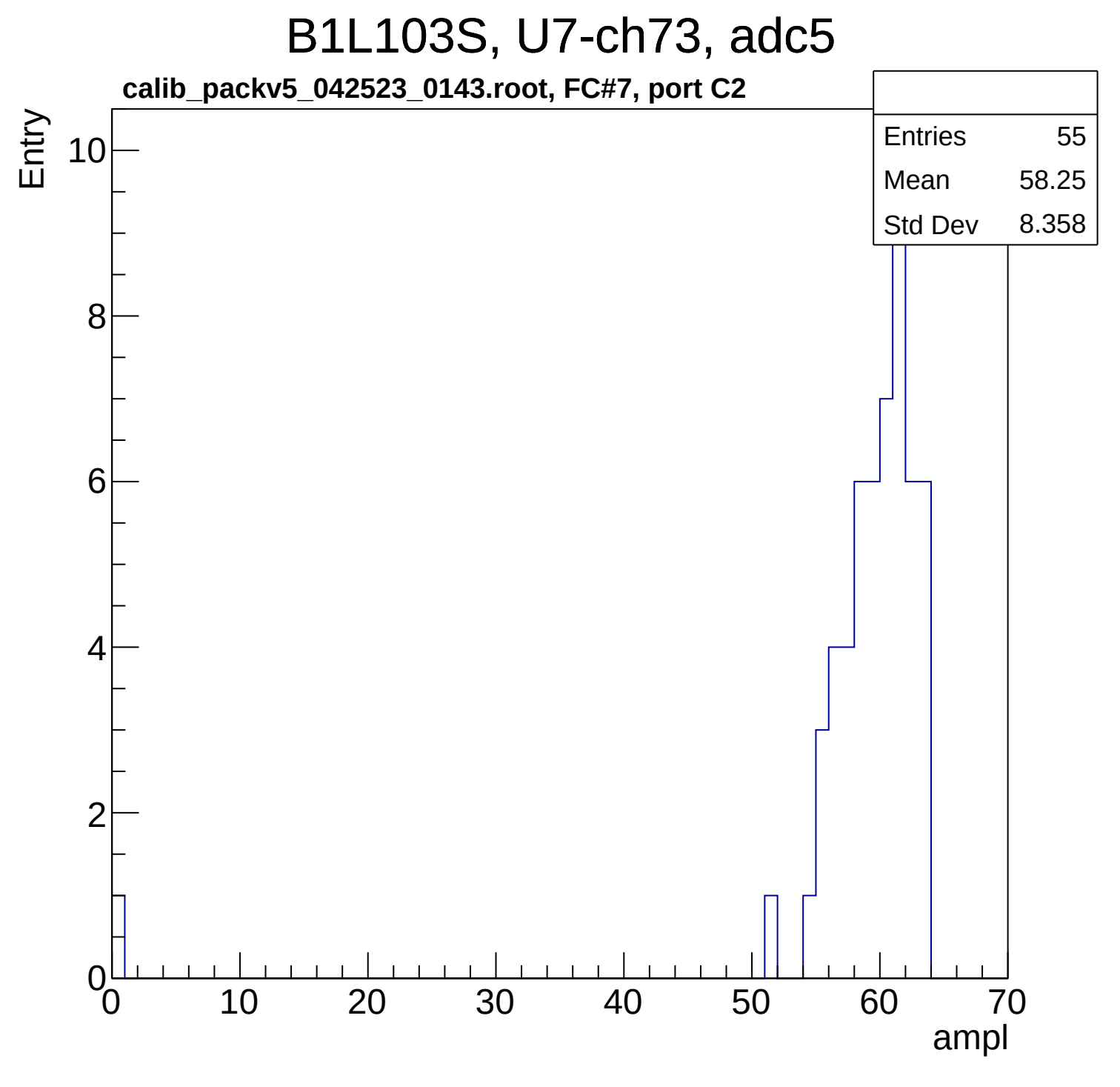

B1L103S, U7-ch73, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 74
Mean 29.23
Std Dev 5.8
Gaus mean : 30.3270
Gaus Width: 3.0111
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

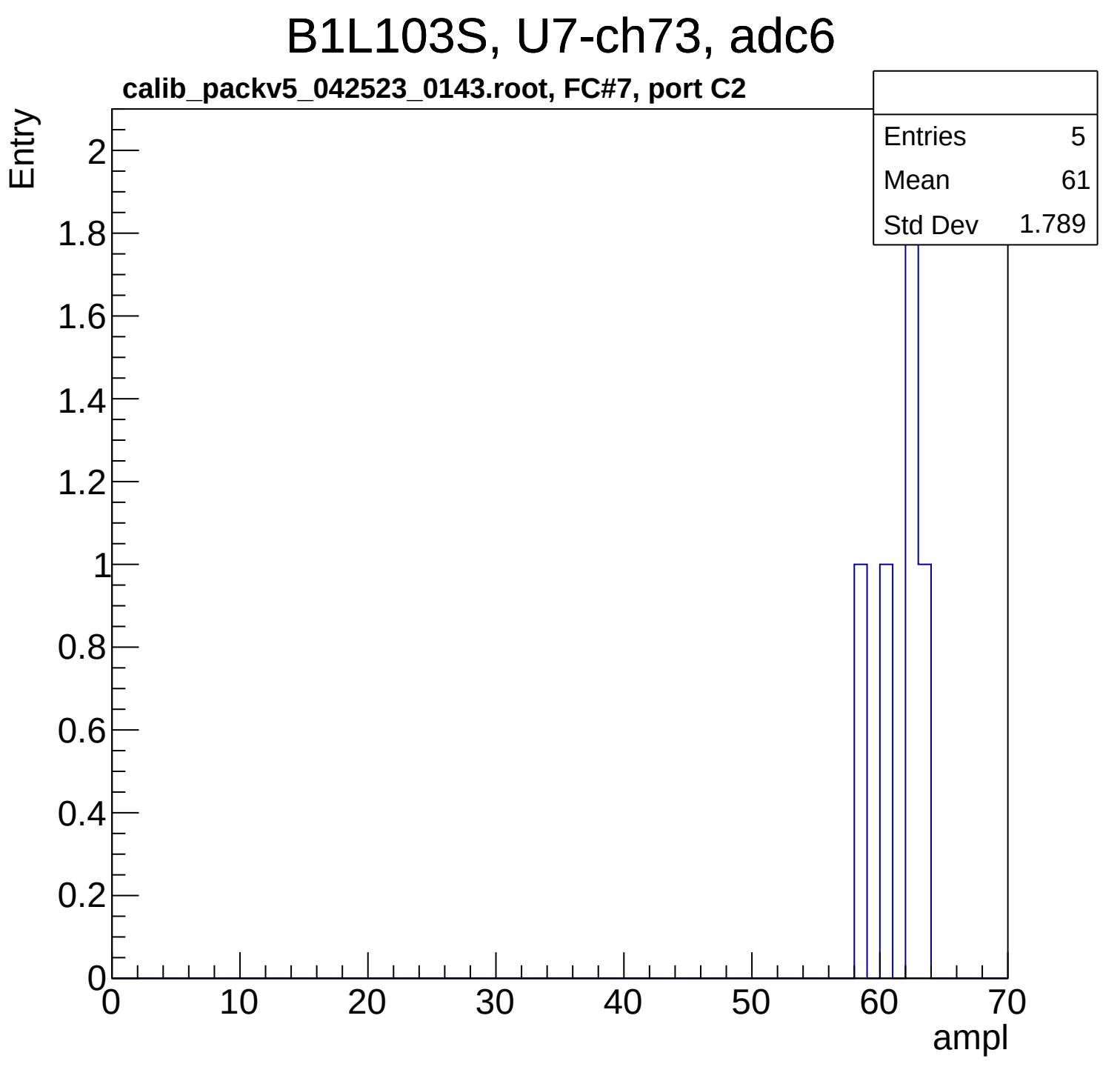

B1L103S, U7-ch73, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 37.47
Std Dev 3.276
Gaus mean : 37.7525
Gaus Width: 3.6211
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

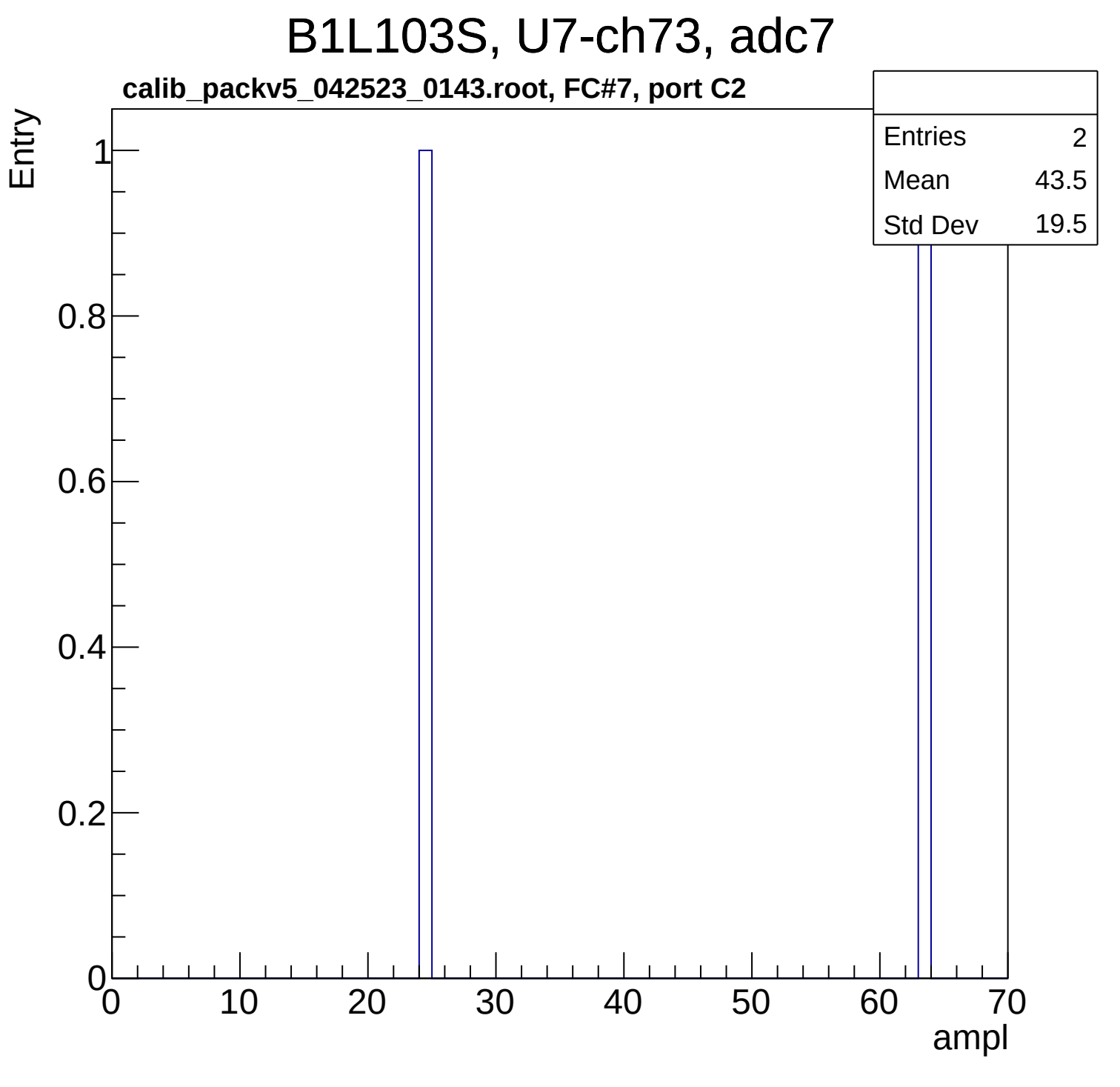

B1L103S, U7-ch73, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 43.17
Std Dev 3.937
Gaus mean : 43.3286
Gaus Width: 4.3380
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

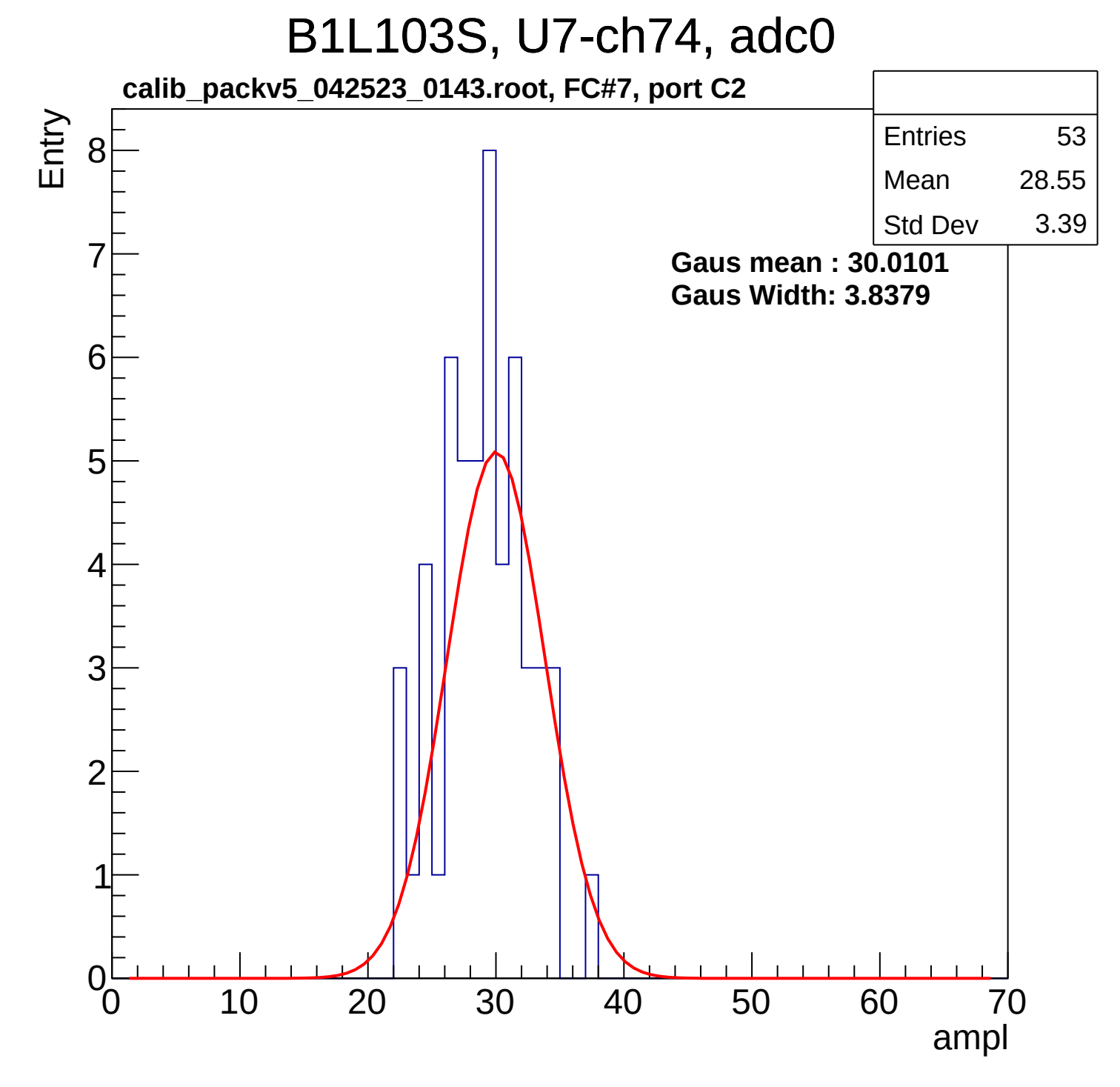

B1L103S, U7-ch73, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 62
Mean 48.98
Std Dev 2.976
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

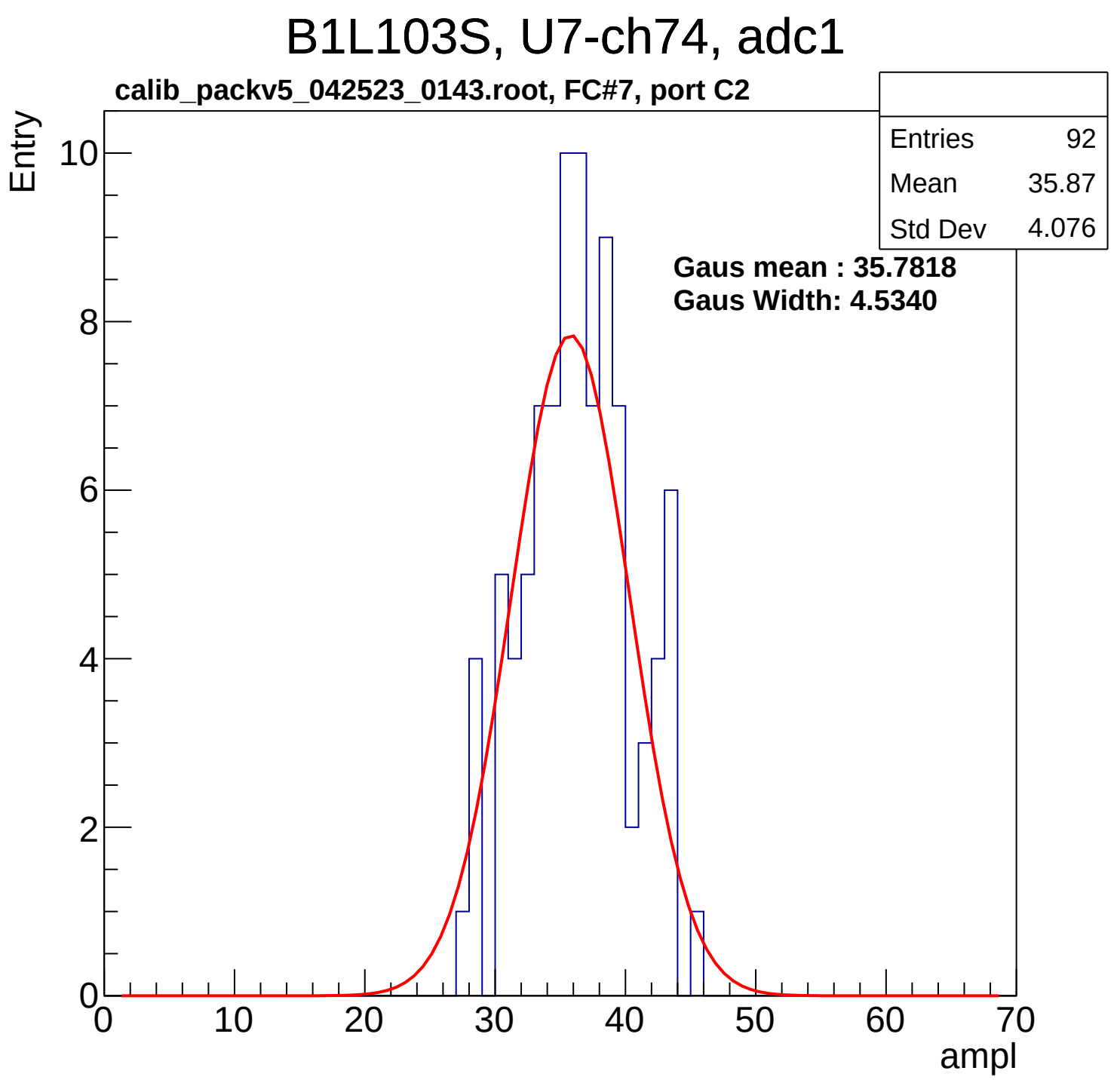

B1L103S, U7-ch73, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 51
Mean 55.43
Std Dev 3.743
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

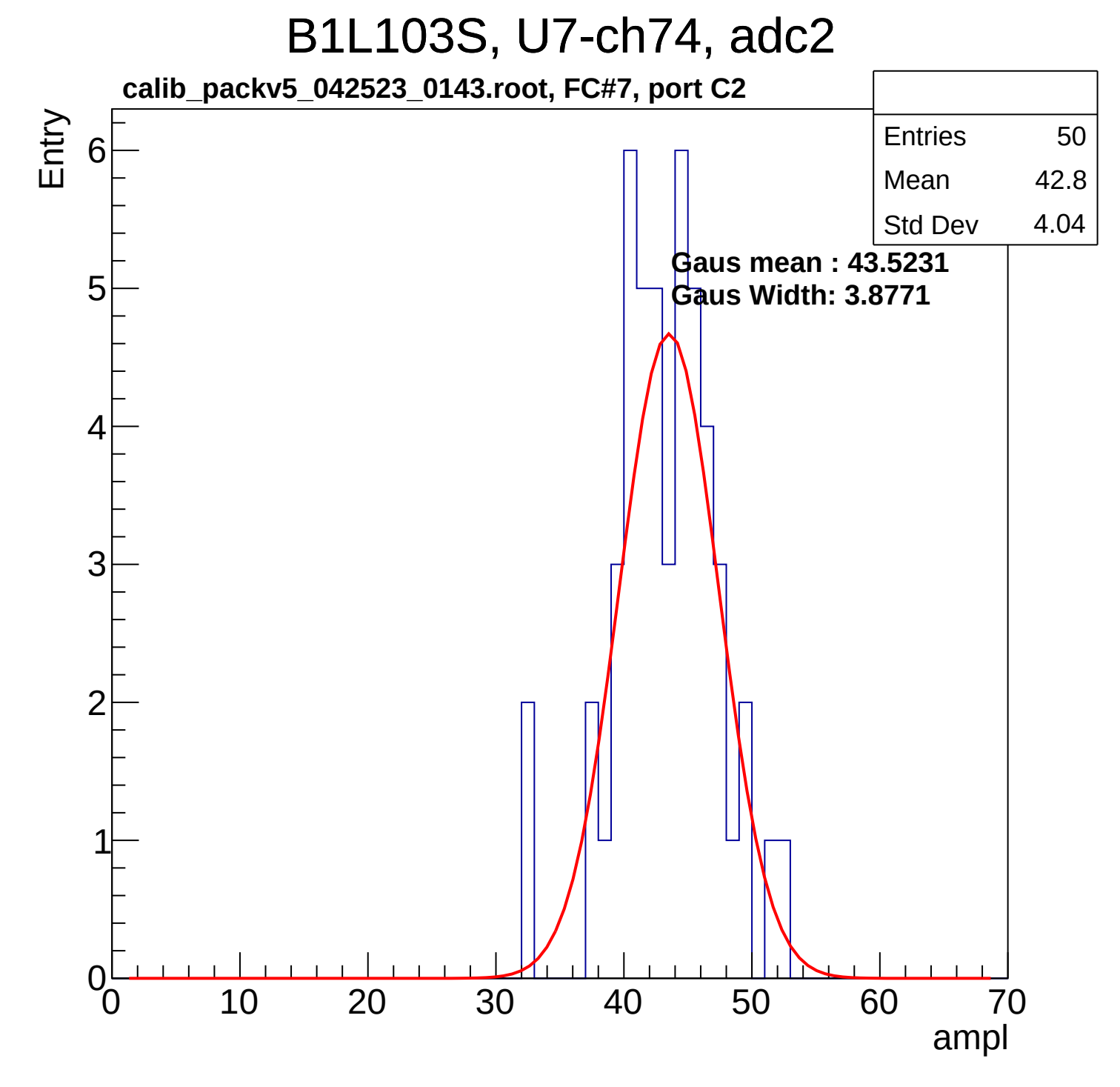

B1L103S, U7-ch73, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 58.25
Std Dev 8.358
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

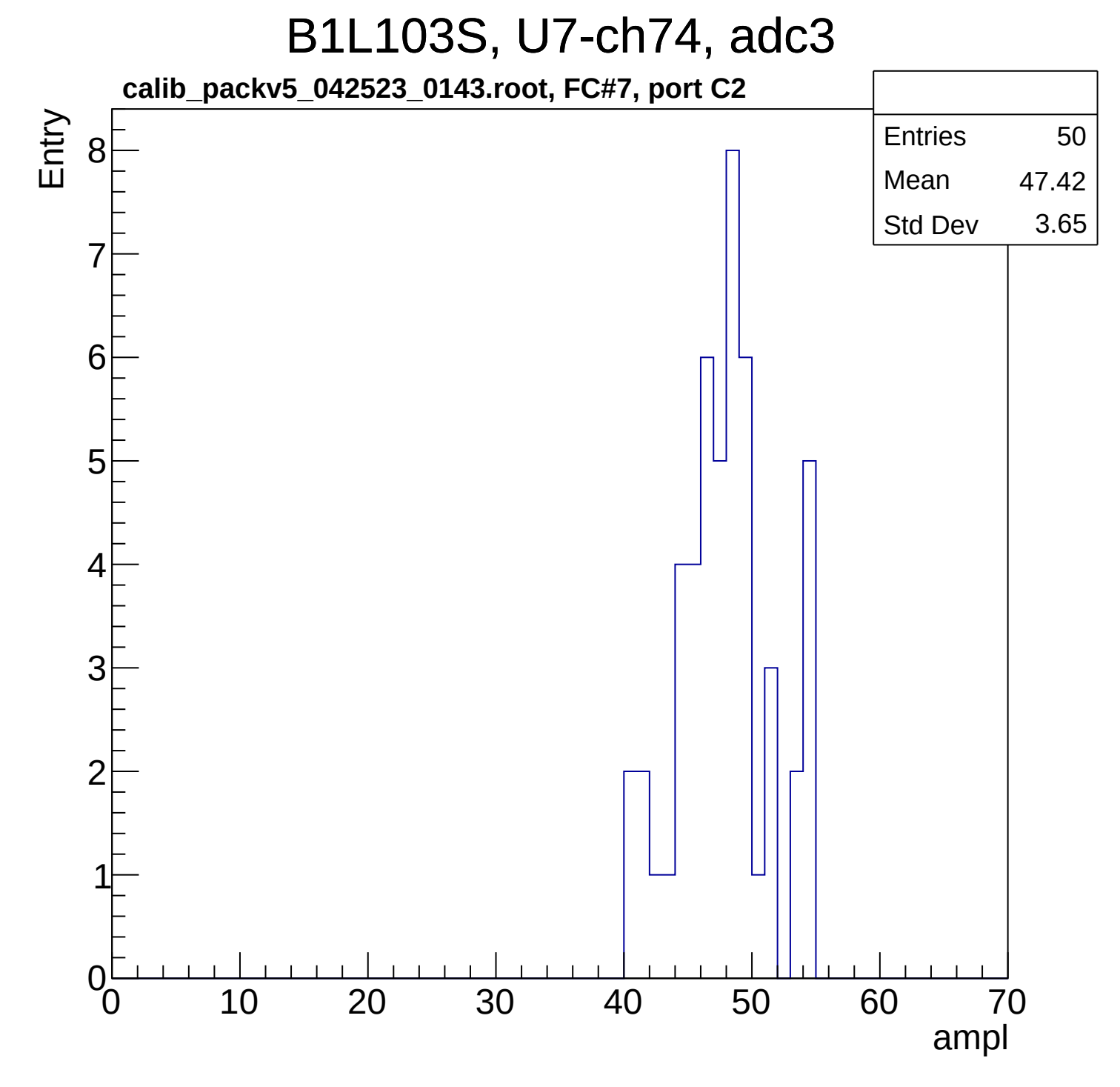

B1L103S, U7-ch73, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 5
Mean 61
Std Dev 1.789
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U7-ch73, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 43.5
Std Dev 19.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch74, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 28.55
Std Dev 3.39
Gaus mean : 30.0101
Gaus Width: 3.8379
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch74, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 92
Mean 35.87
Std Dev 4.076
Gaus mean : 35.7818
Gaus Width: 4.5340
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch74, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 50
Mean 42.8
Std Dev 4.04
Gaus mean : 43.5231
Gaus Width: 3.8771
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U7-ch74, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 50
Mean 47.42
Std Dev 3.65
Entry
ampl
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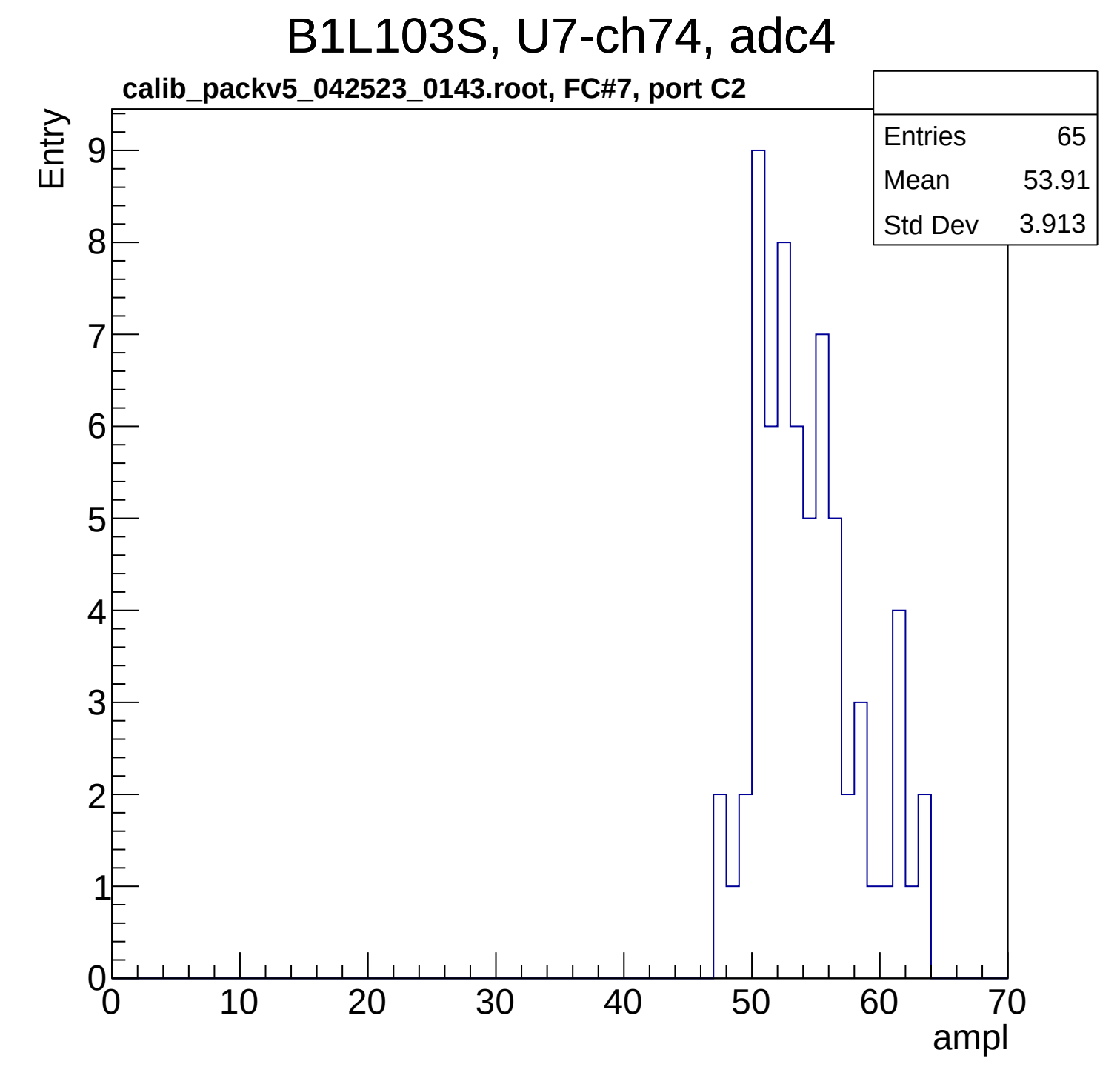
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch74, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 53.91
Std Dev 3.913
Entry
ampl
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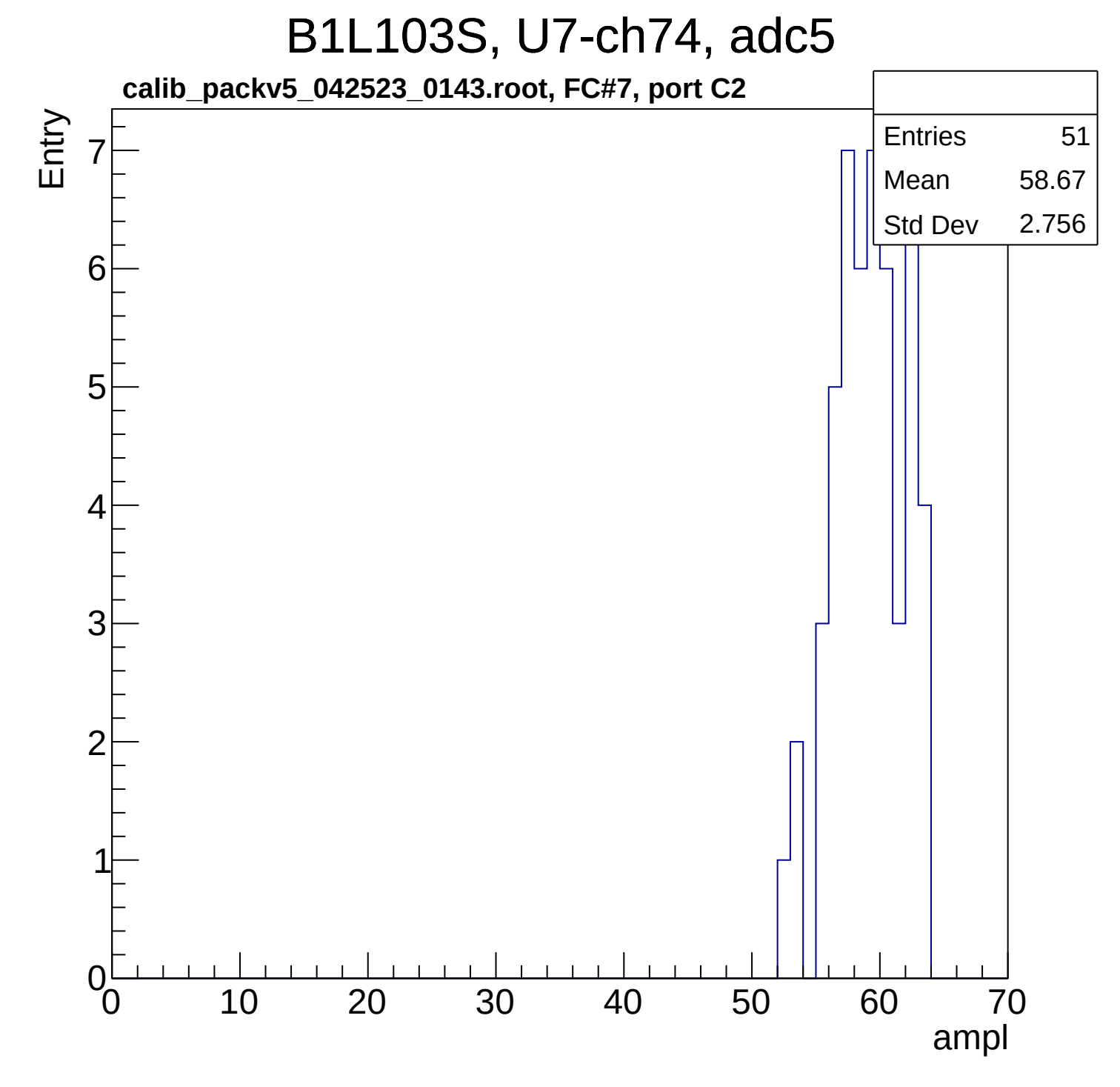
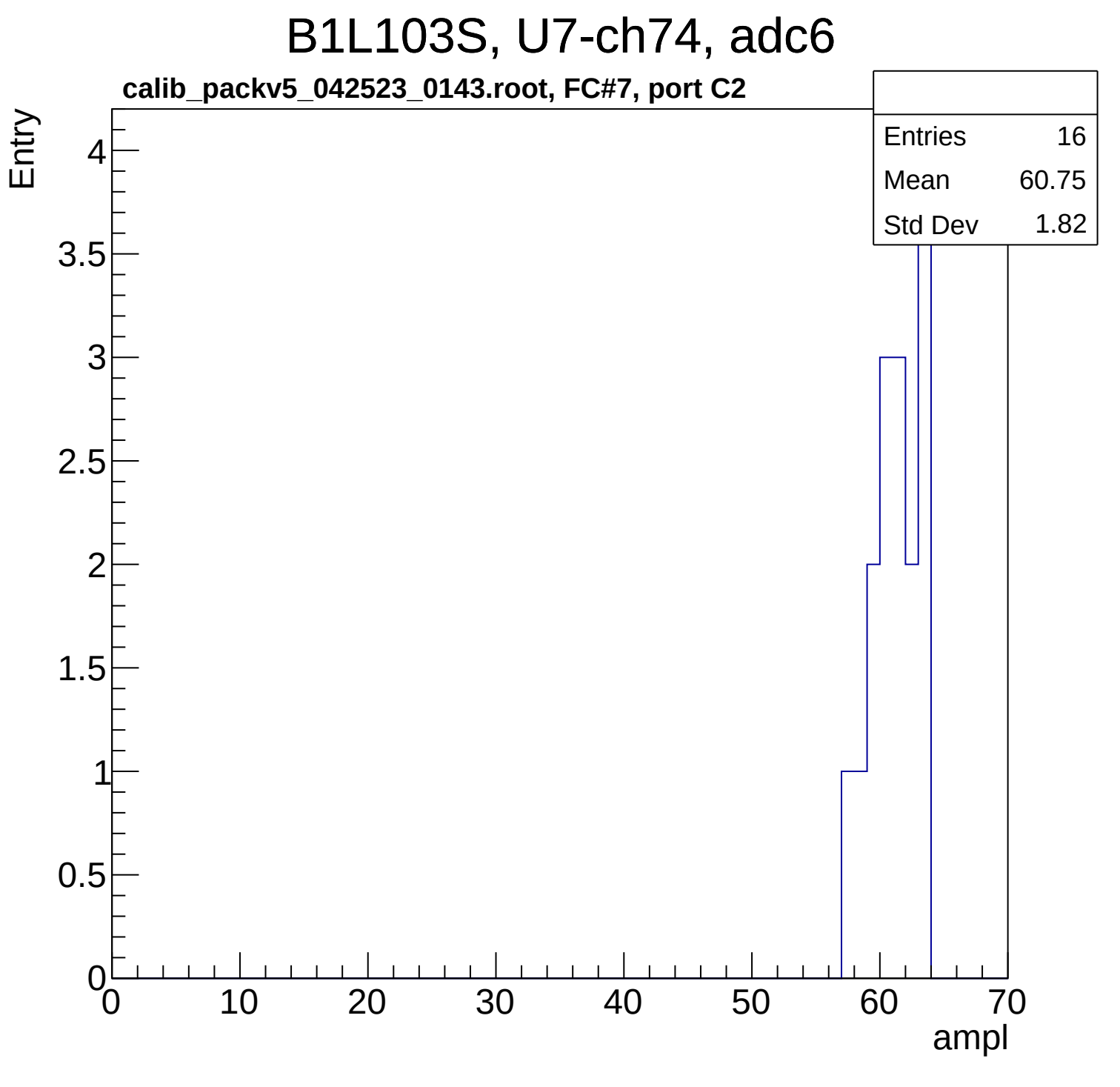
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch74, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 51
Mean 58.67
Std Dev 2.756
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch74, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 16
Mean 60.75
Std Dev 1.82
Entry
ampl
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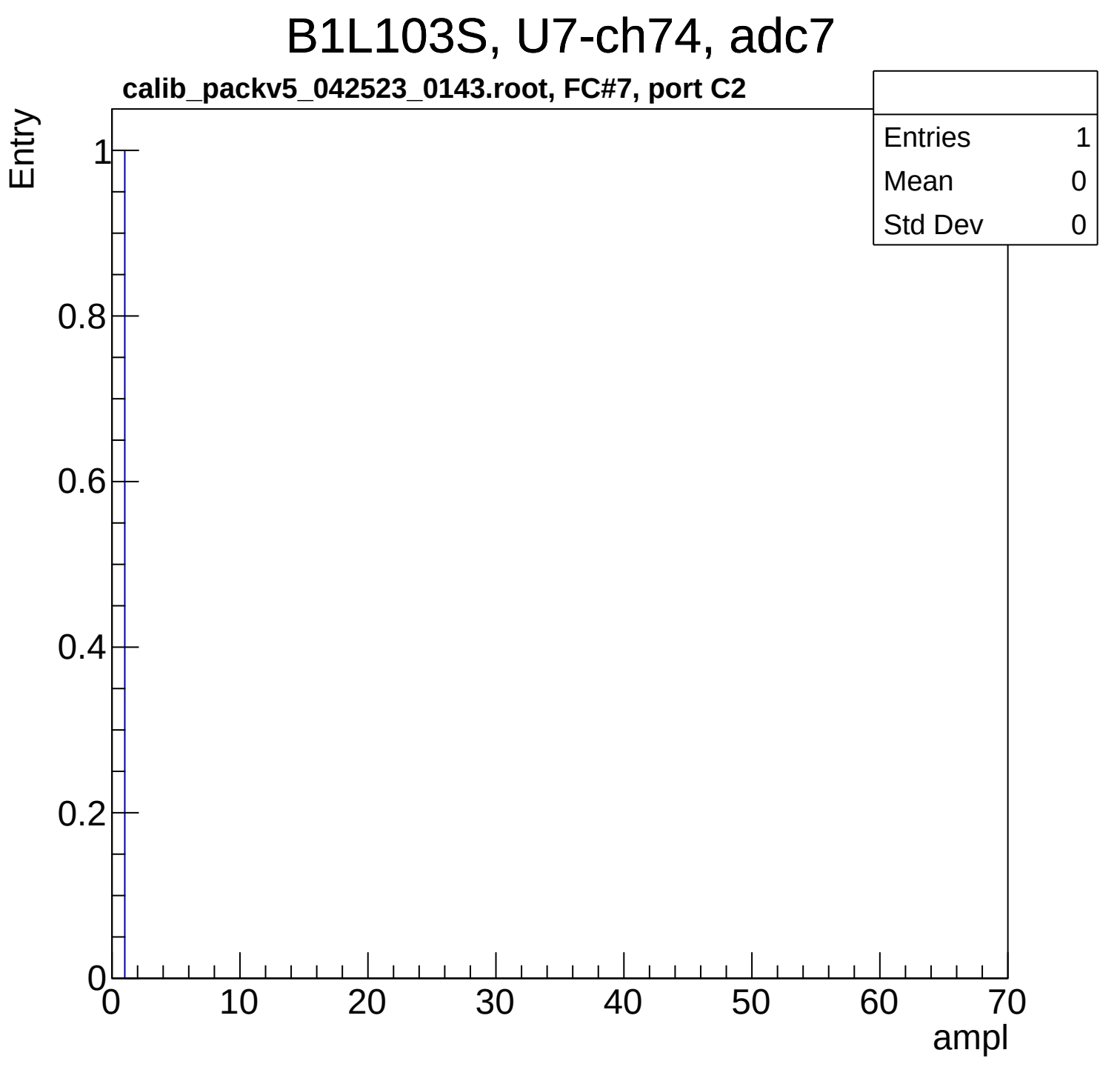
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U7-ch74, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
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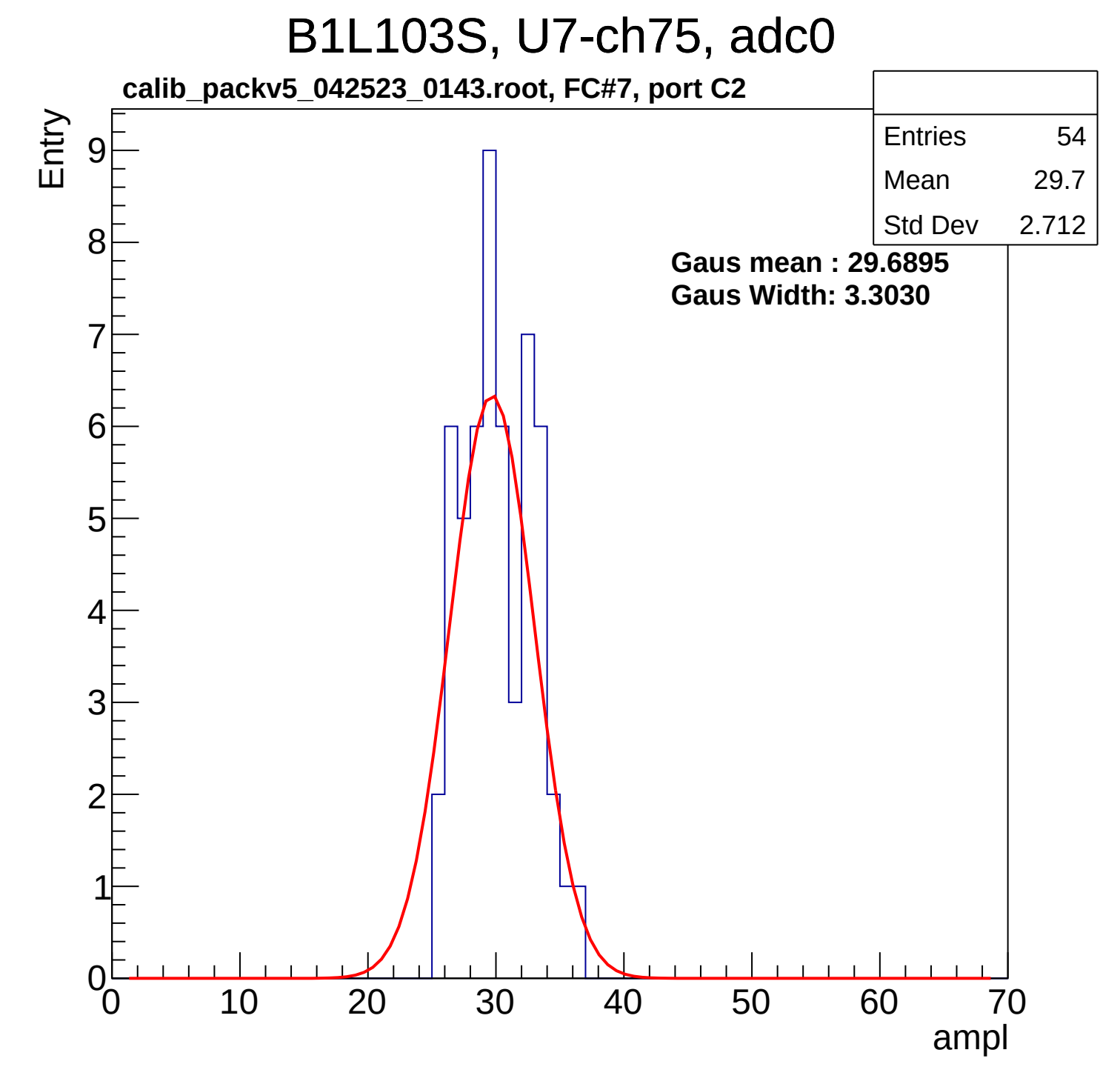
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch75, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 54
Mean 29.7
Std Dev 2.712
Gaus mean : 29.6895
Gaus Width: 3.3030
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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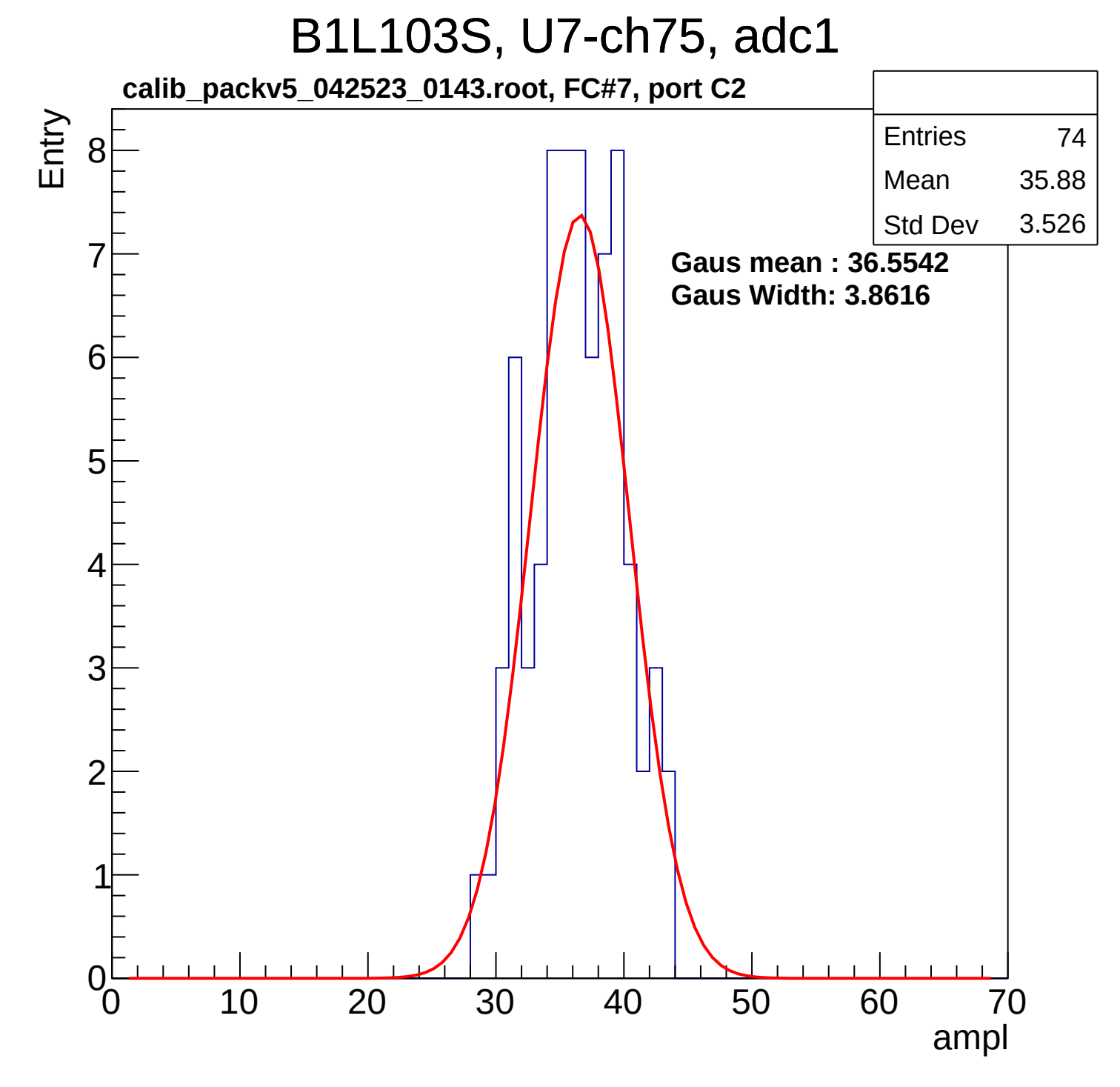
B1L103S, U7-ch75, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 74
Mean 35.88
Std Dev 3.526
Gaus mean : 36.5542
Gaus Width: 3.8616
Entry
ampl
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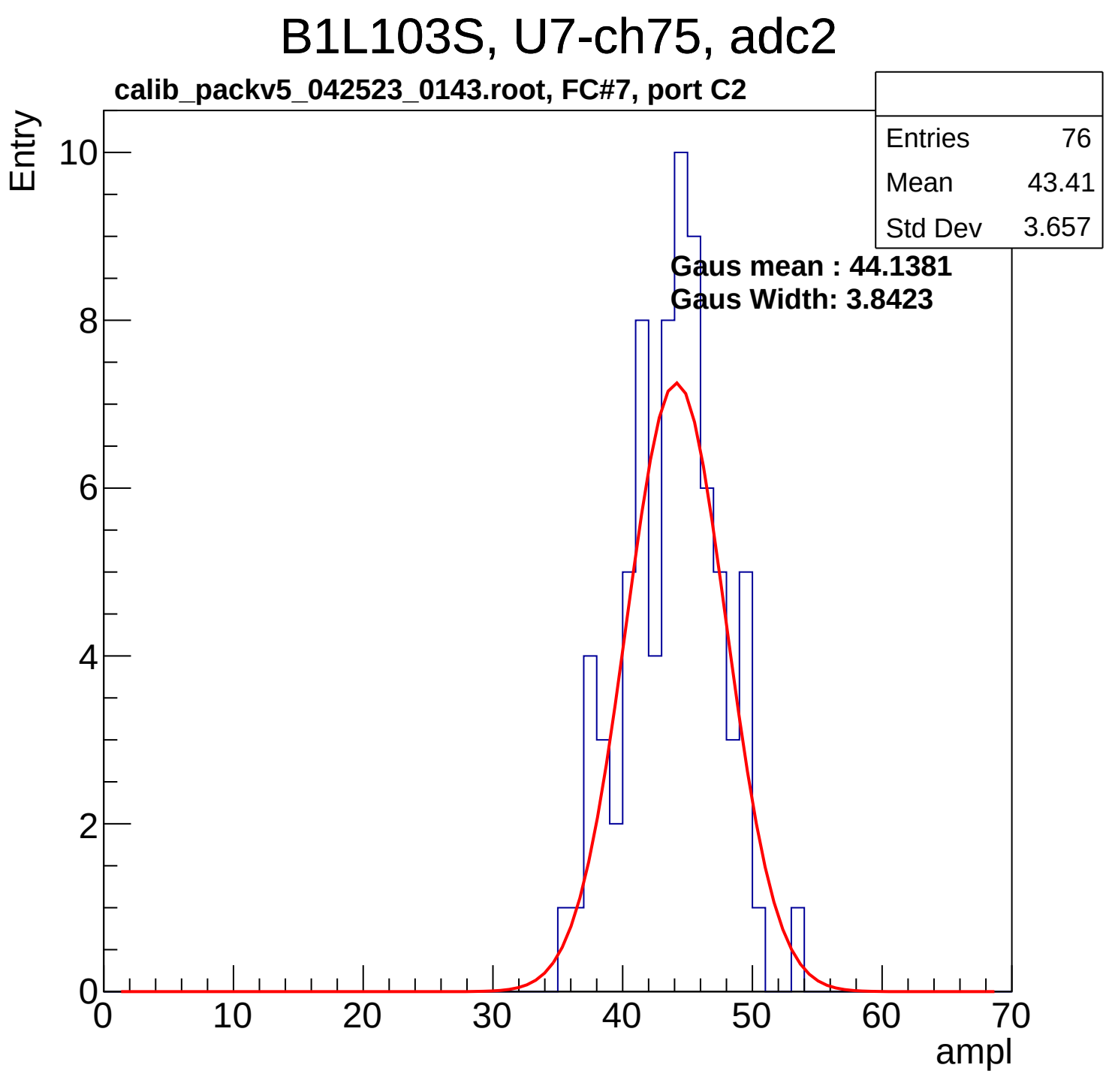
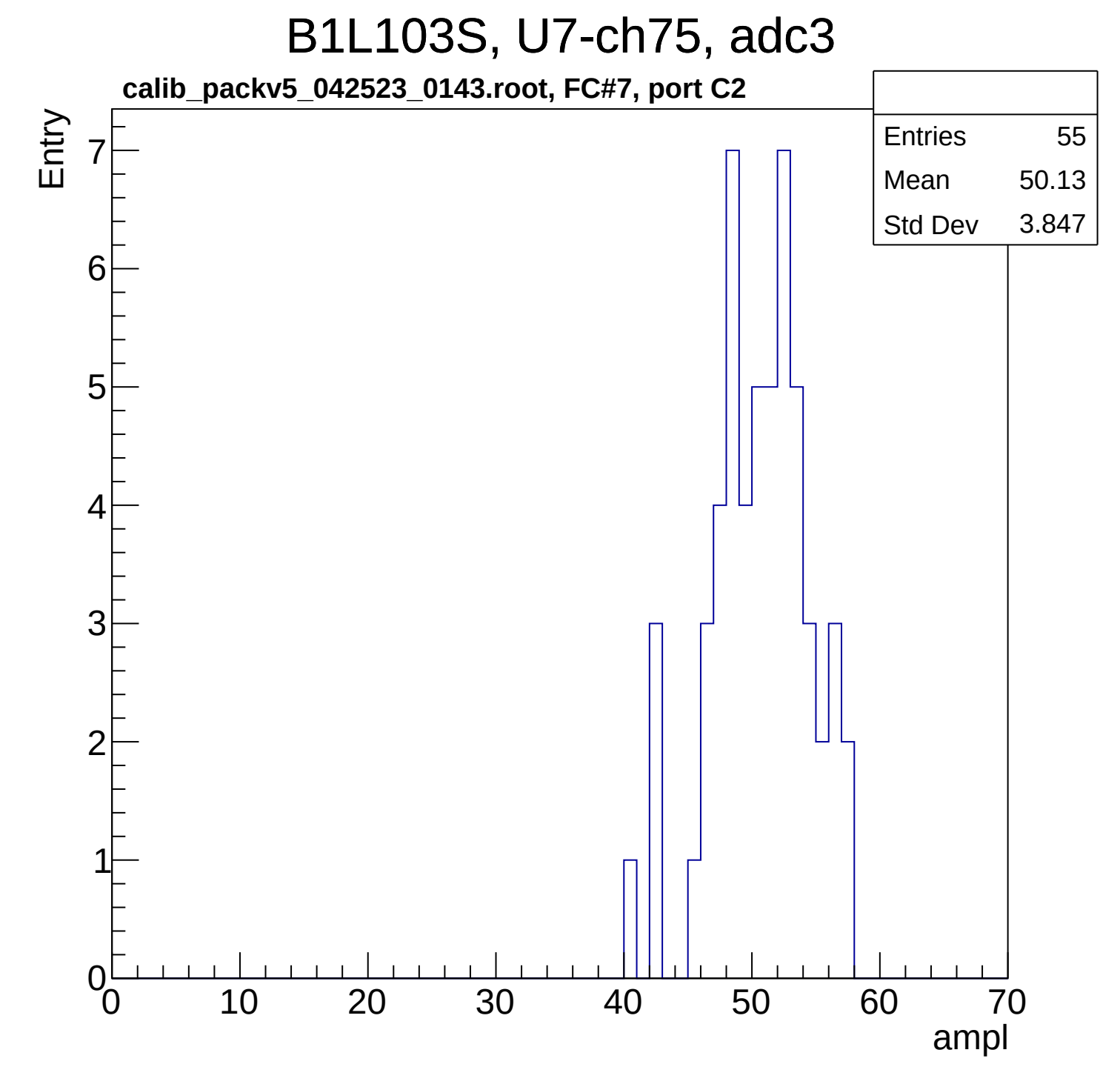
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch75, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 76
Mean 43.41
Std Dev 3.657
Gaus mean : 44.1381
Gaus Width: 3.8423
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch75, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 50.13
Std Dev 3.847
Entry
ampl
0
1
2
3
4
5
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0
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60
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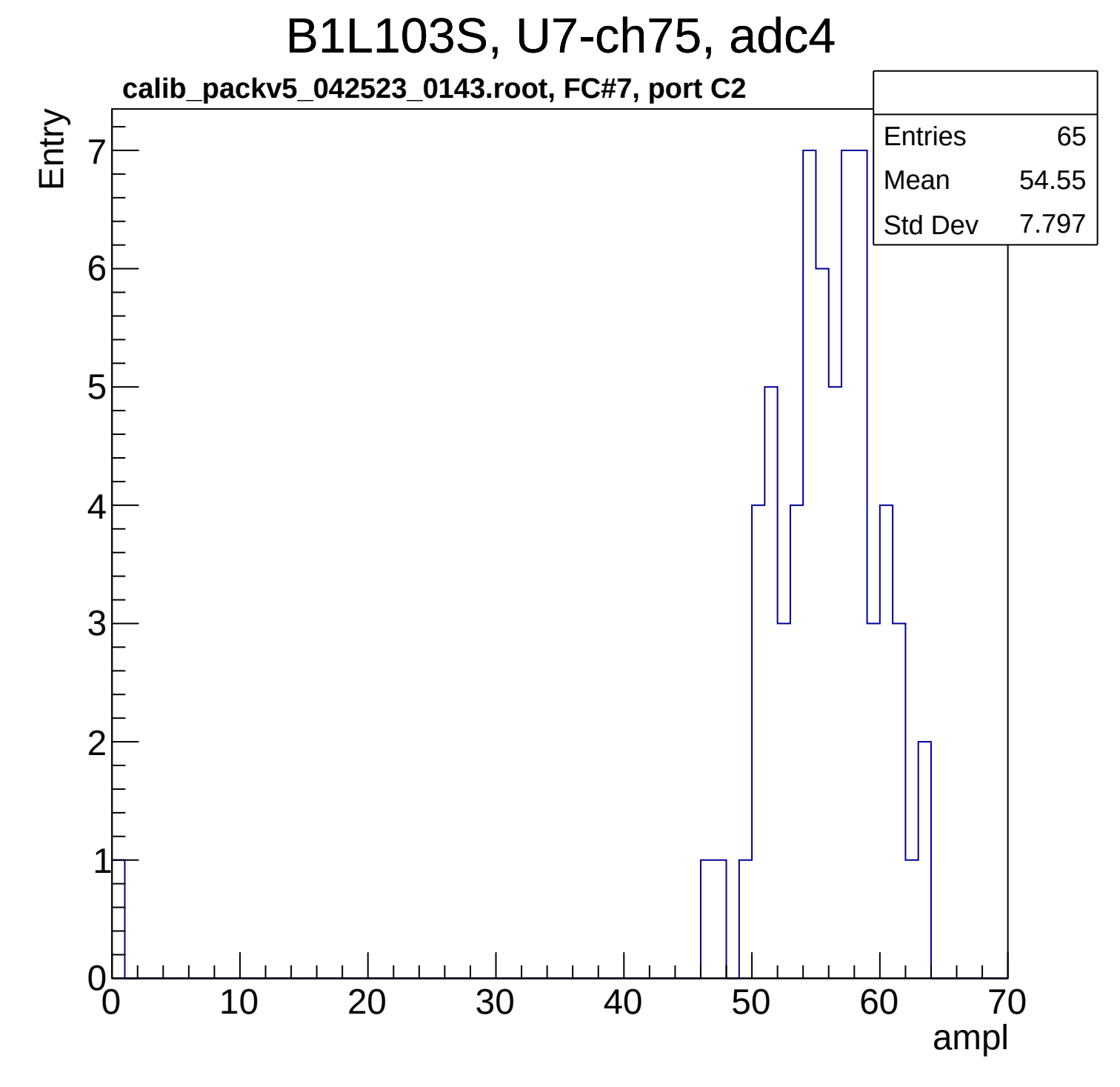
B1L103S, U7-ch75, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 54.55
Std Dev 7.797
Entry
ampl
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2
3
4
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60
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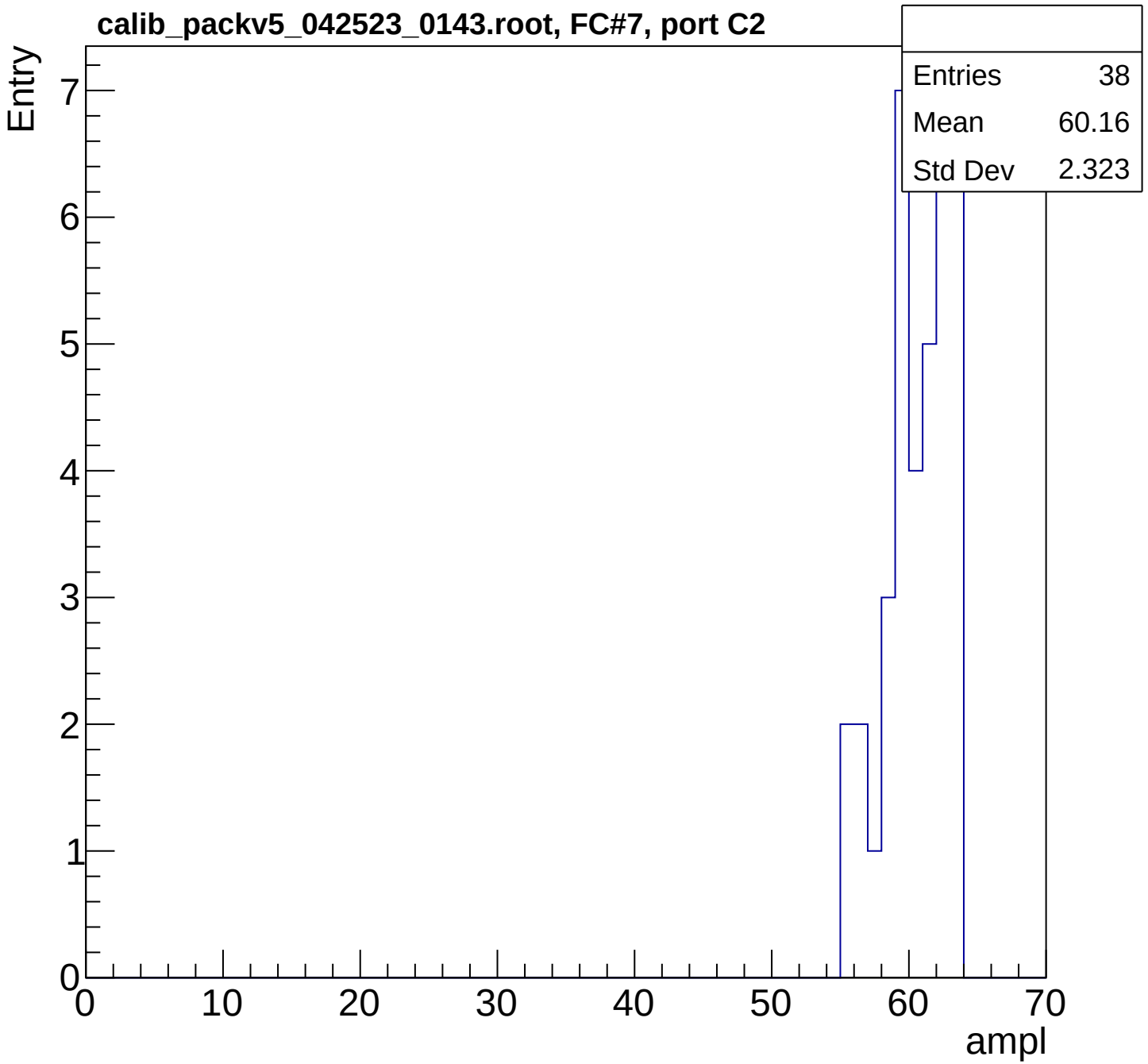
B1L103S, U7-ch75, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 38
Mean 60.16
Std Dev 2.323
Entry
ampl
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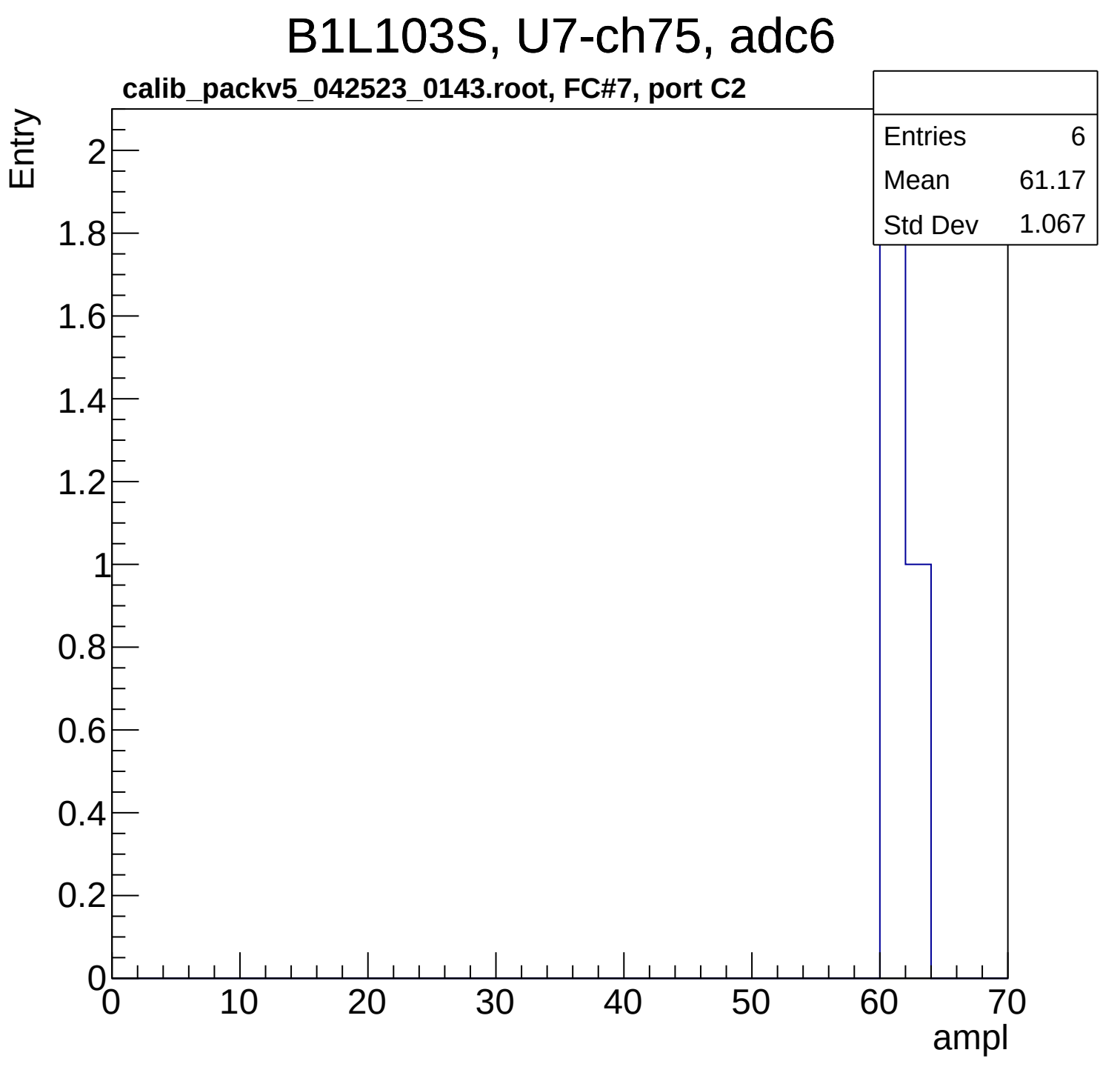
B1L103S, U7-ch75, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 6
Mean 61.17
Std Dev 1.067
Entry
ampl
0
0.2
0.4
0.6
0.8
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1.2
1.4
1.6
1.8
2
0
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60
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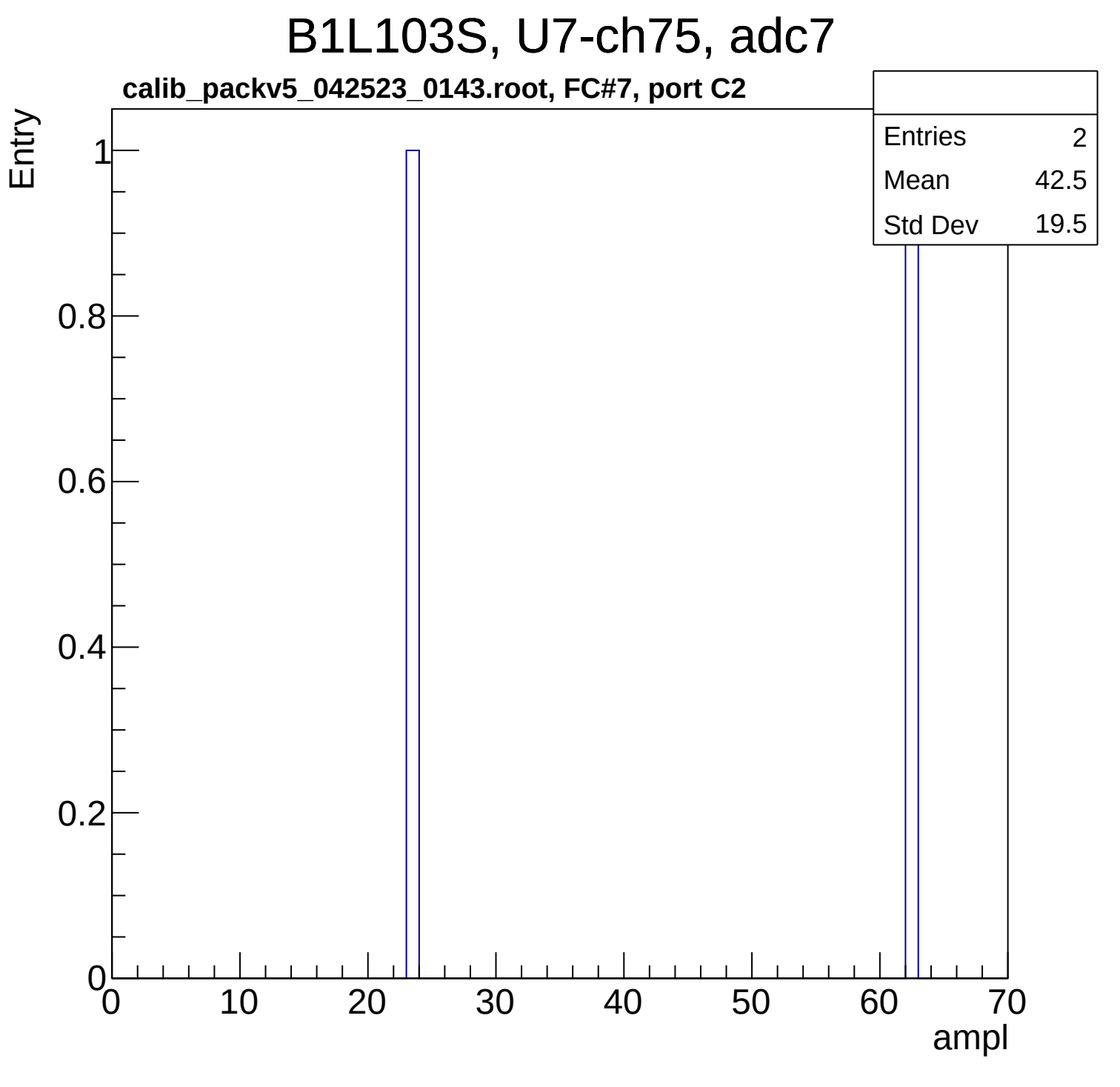
B1L103S, U7-ch75, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 42.5
Std Dev 19.5
Entry
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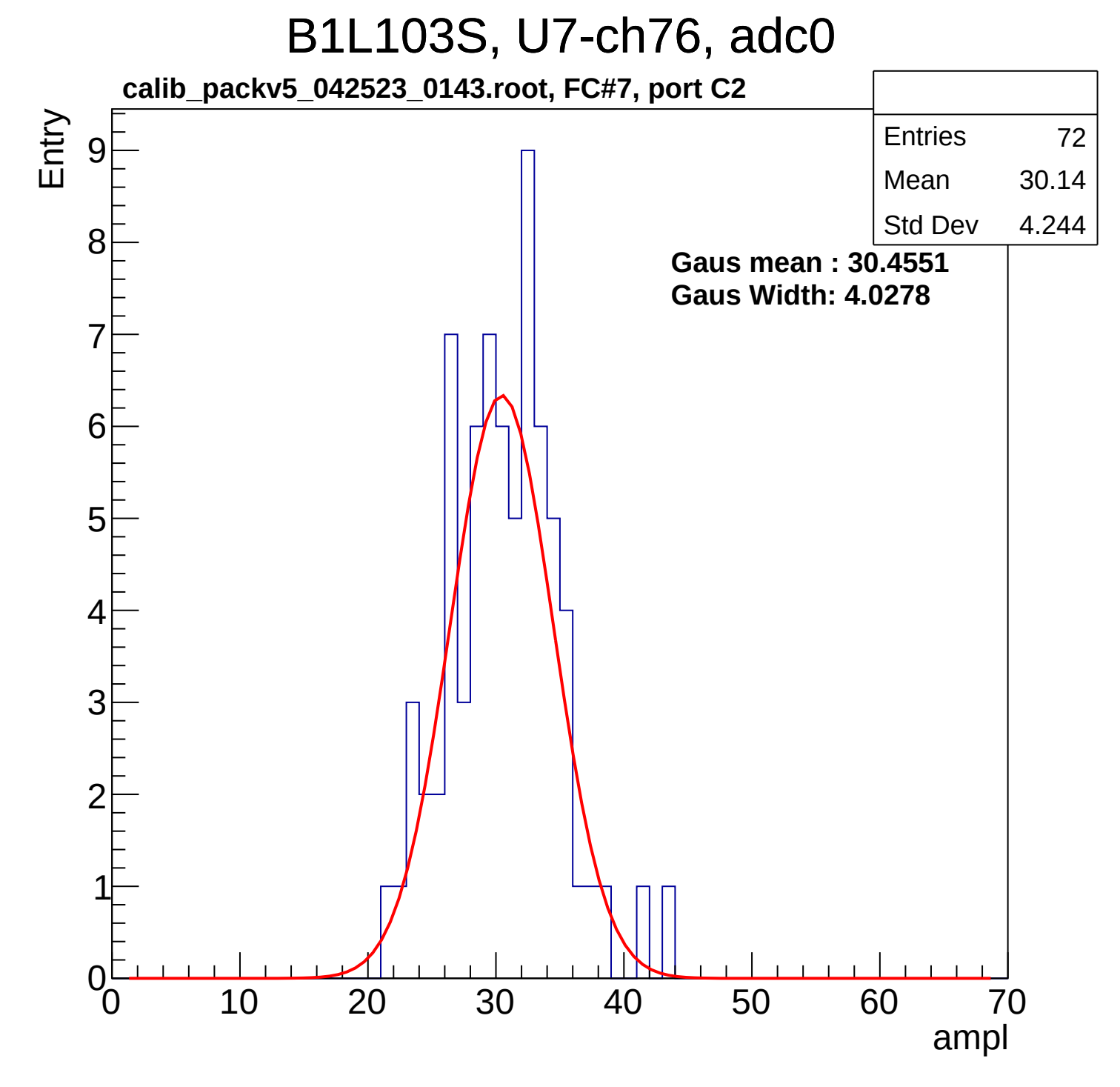
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch76, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 72
Mean 30.14
Std Dev 4.244
Gaus mean : 30.4551
Gaus Width: 4.0278
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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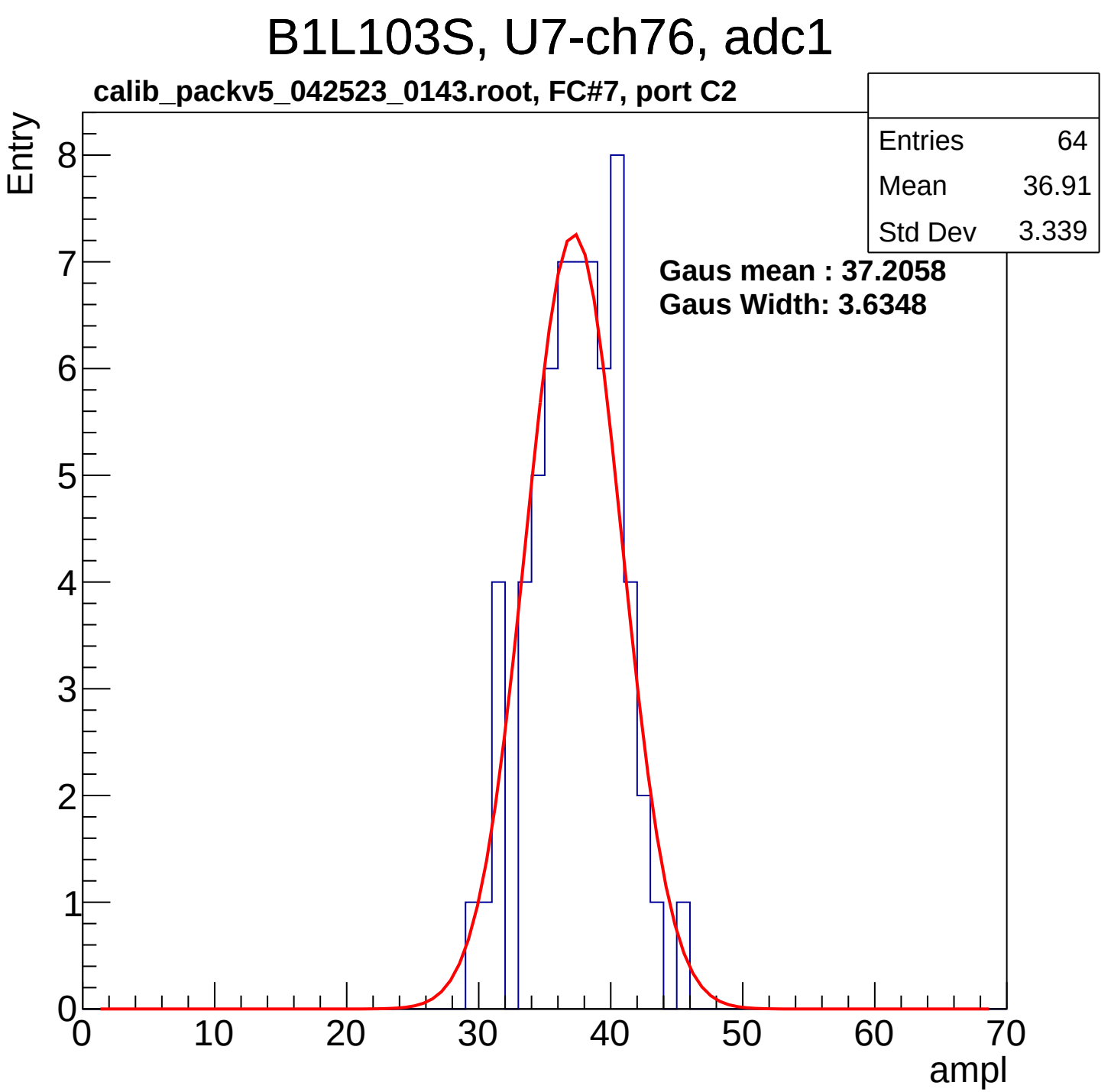
B1L103S, U7-ch76, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 36.91
Std Dev 3.339
Gaus mean : 37.2058
Gaus Width: 3.6348
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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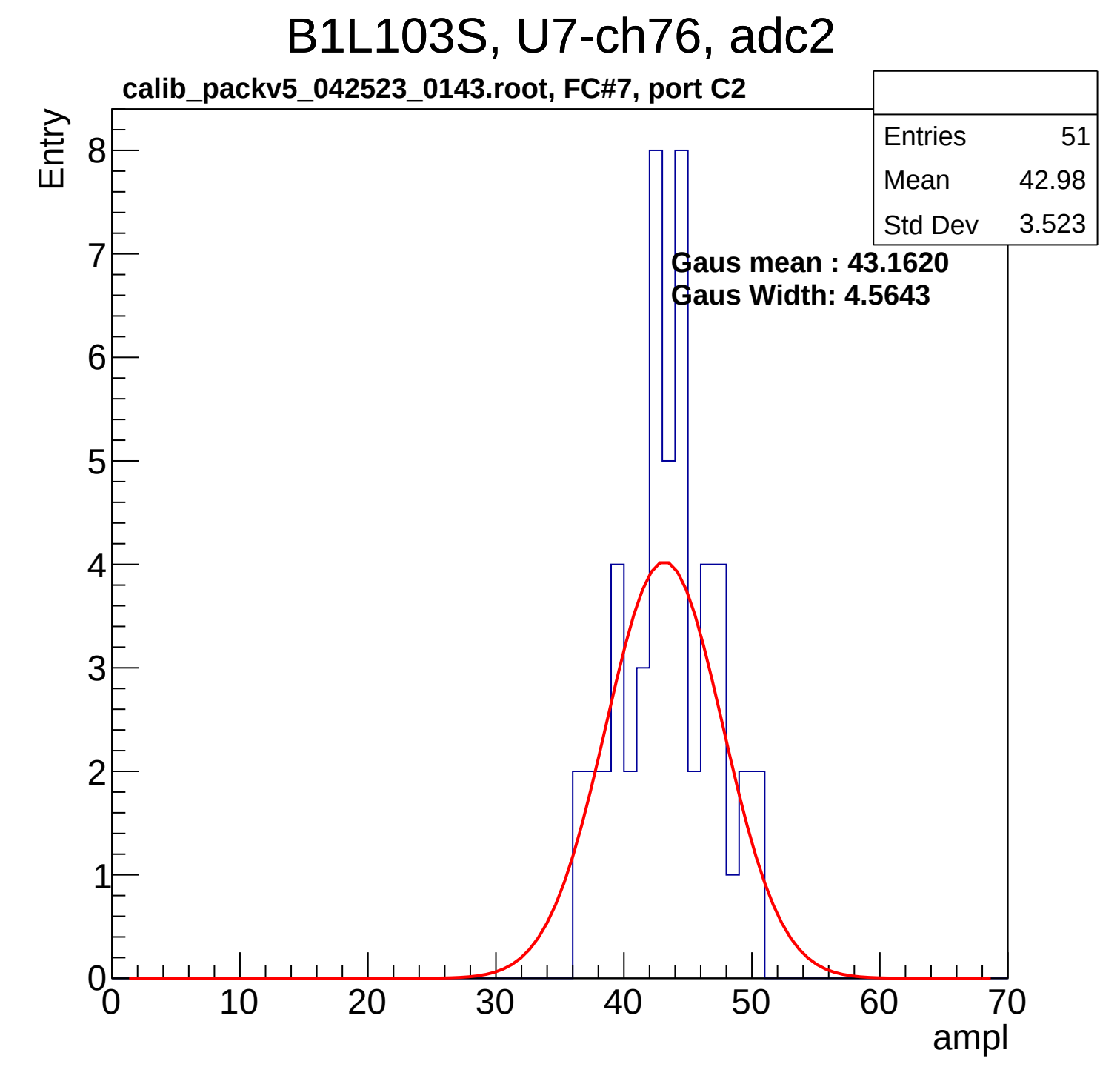
B1L103S, U7-ch76, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 51
Mean 42.98
Std Dev 3.523
Gaus mean : 43.1620
Gaus Width: 4.5643
Entry
ampl
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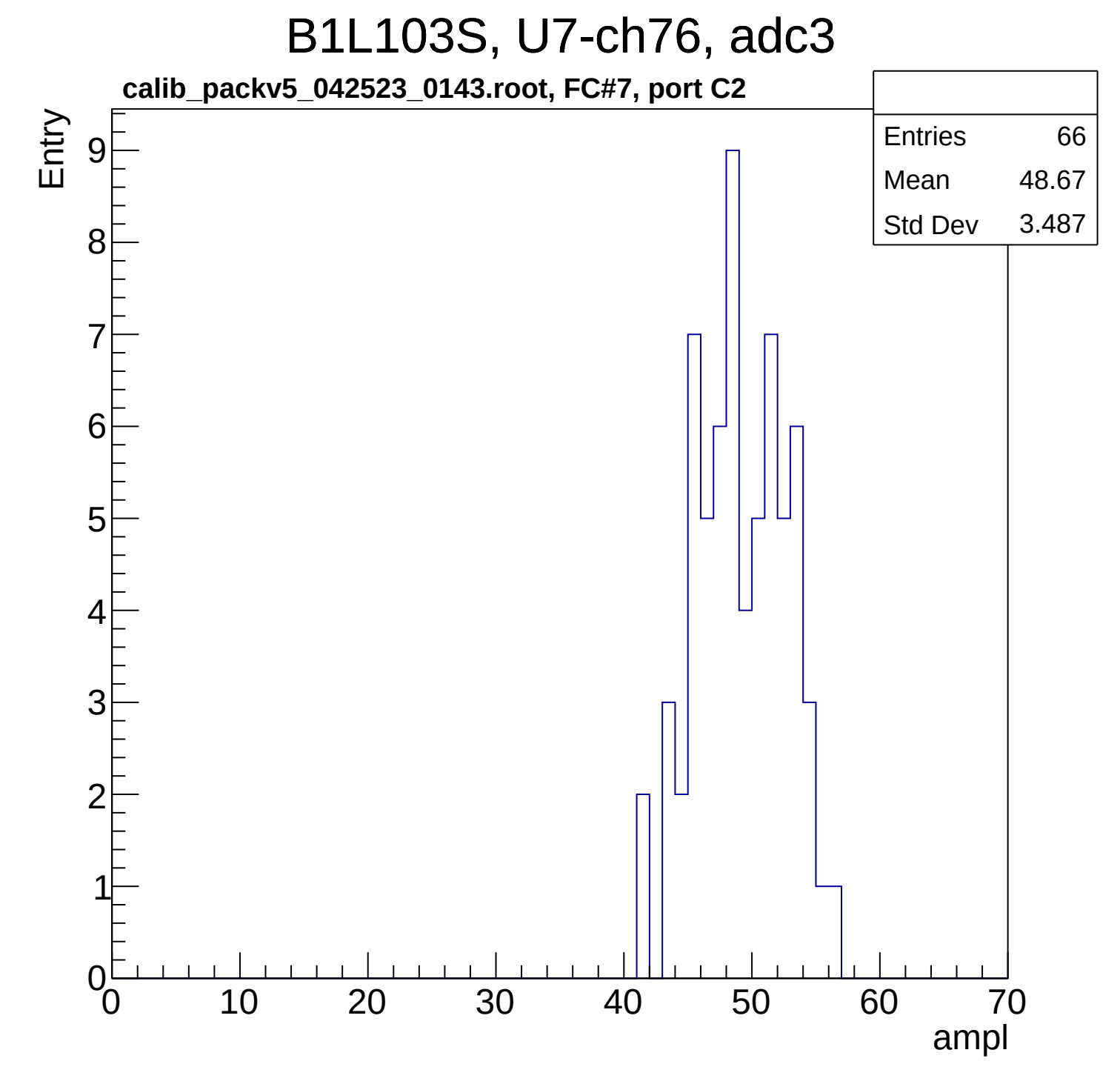
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch76, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 48.67
Std Dev 3.487
Entry
ampl
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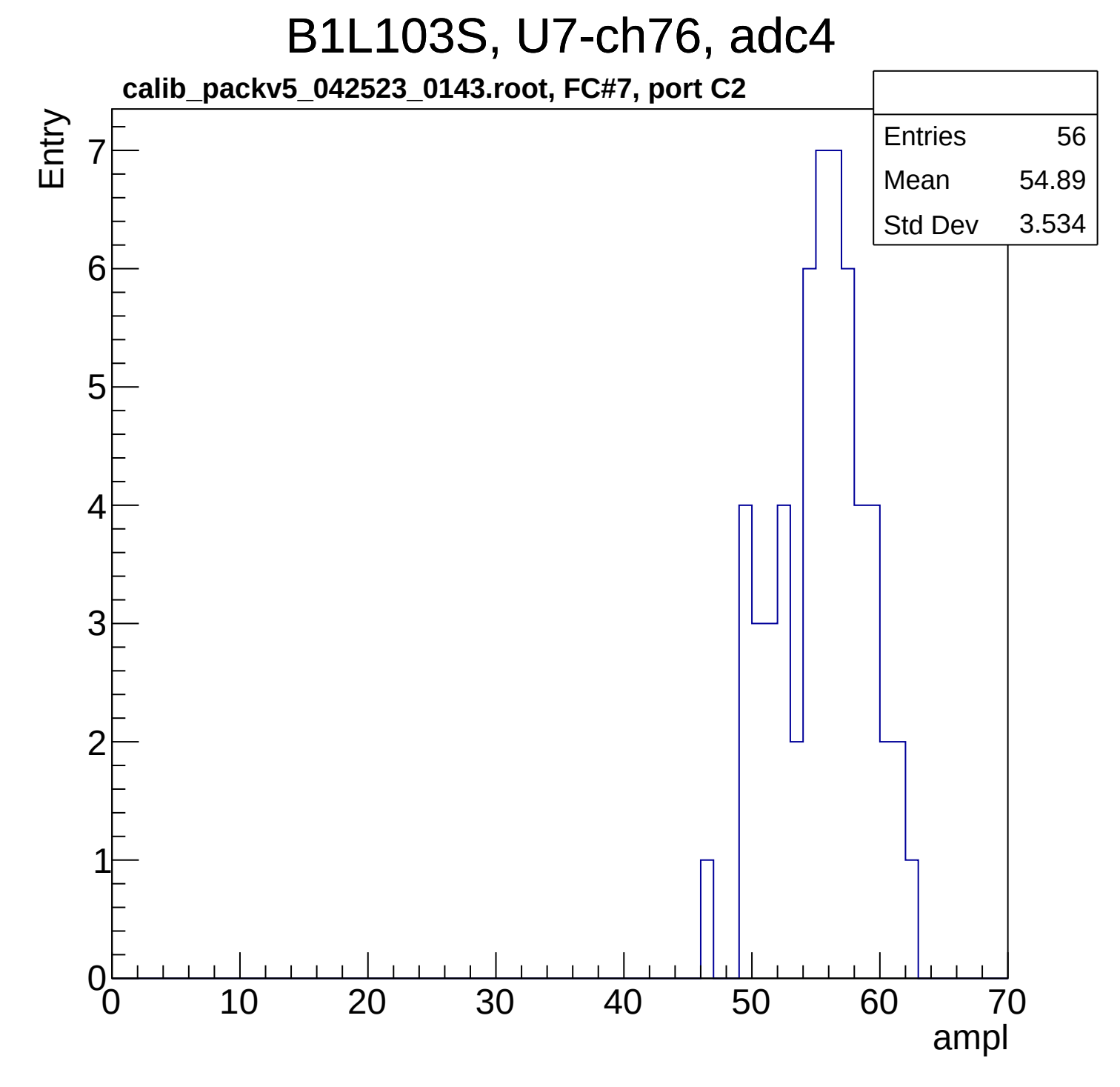
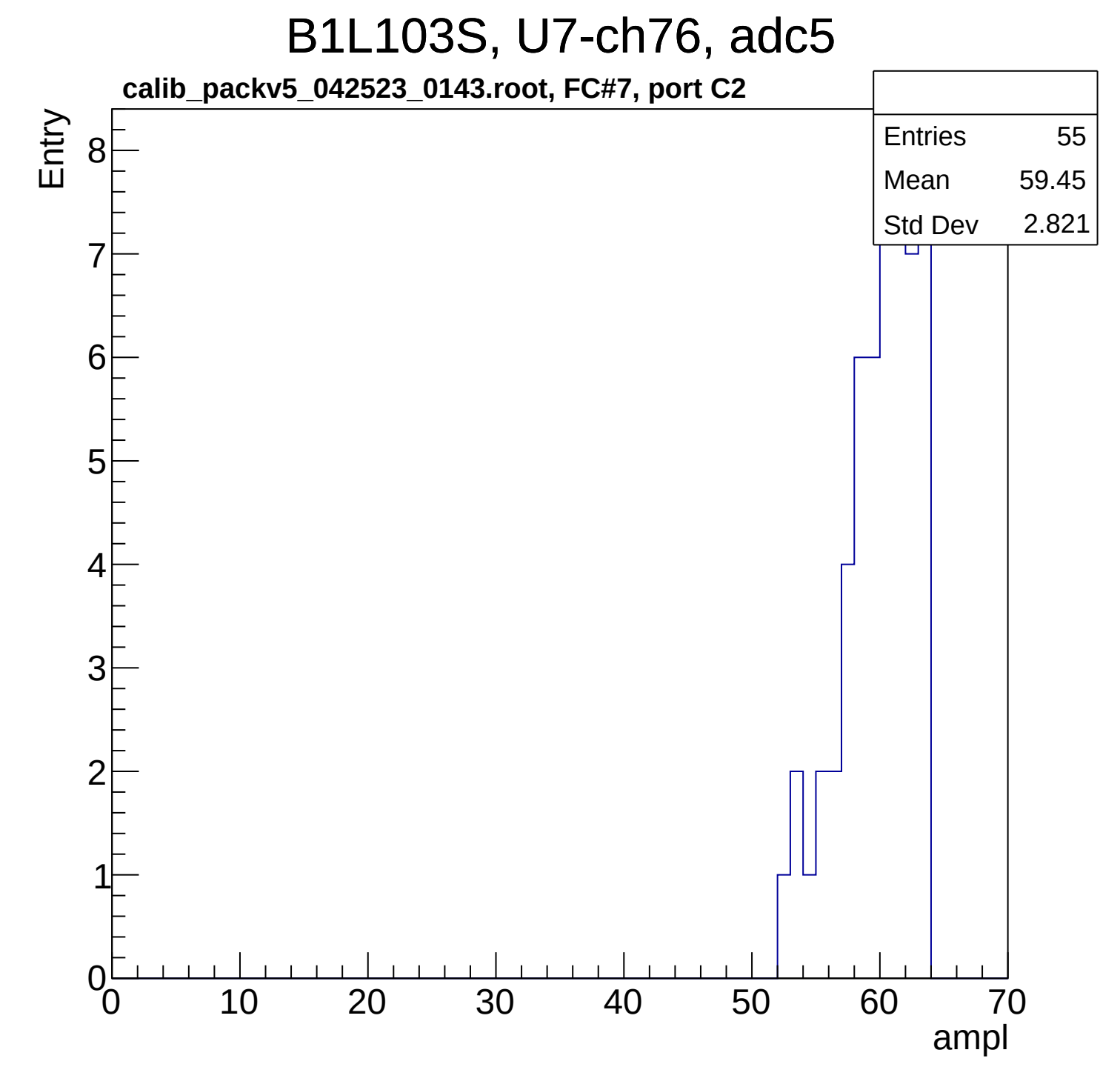
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch76, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 54.89
Std Dev 3.534
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch76, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 59.45
Std Dev 2.821
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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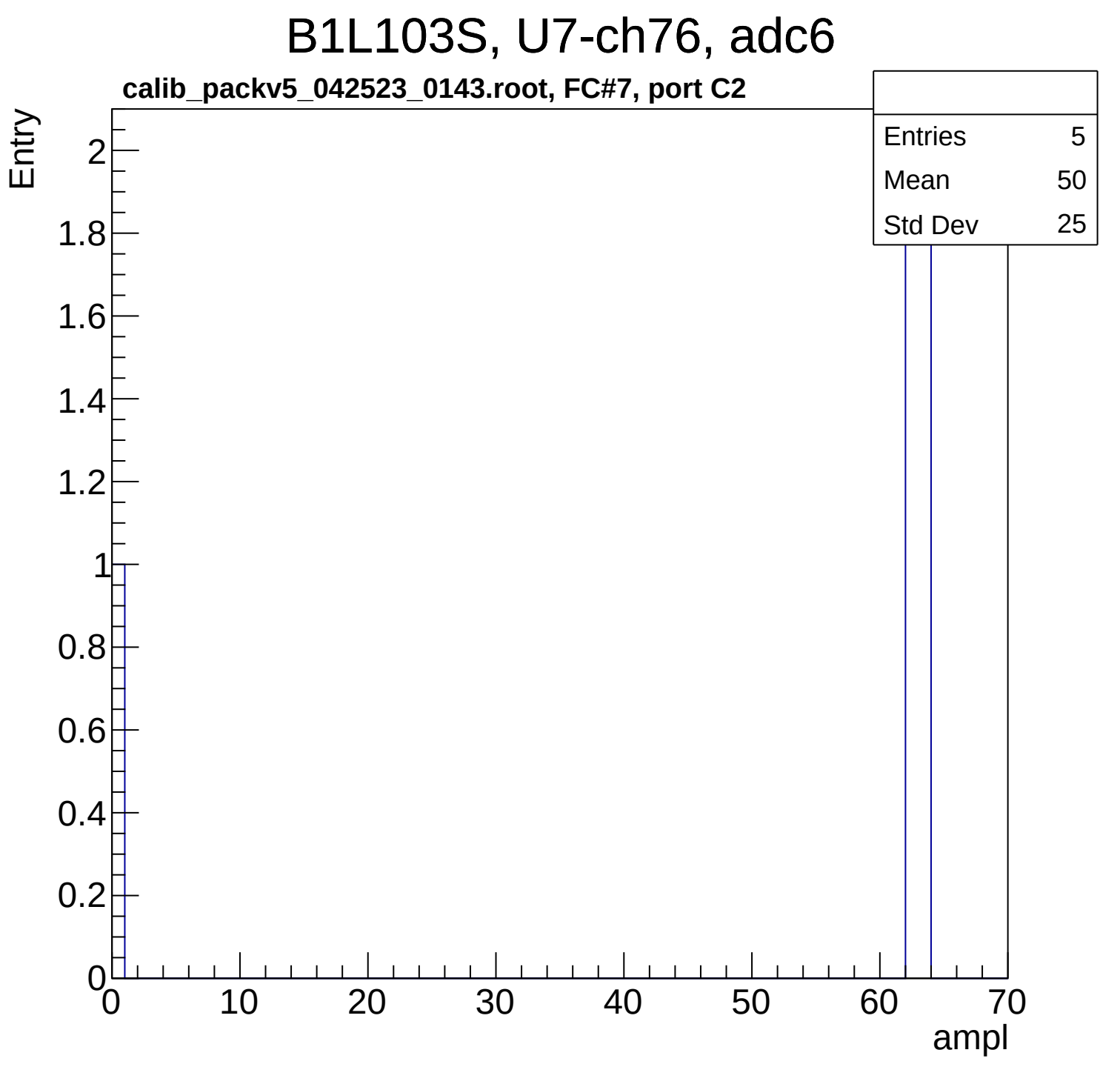
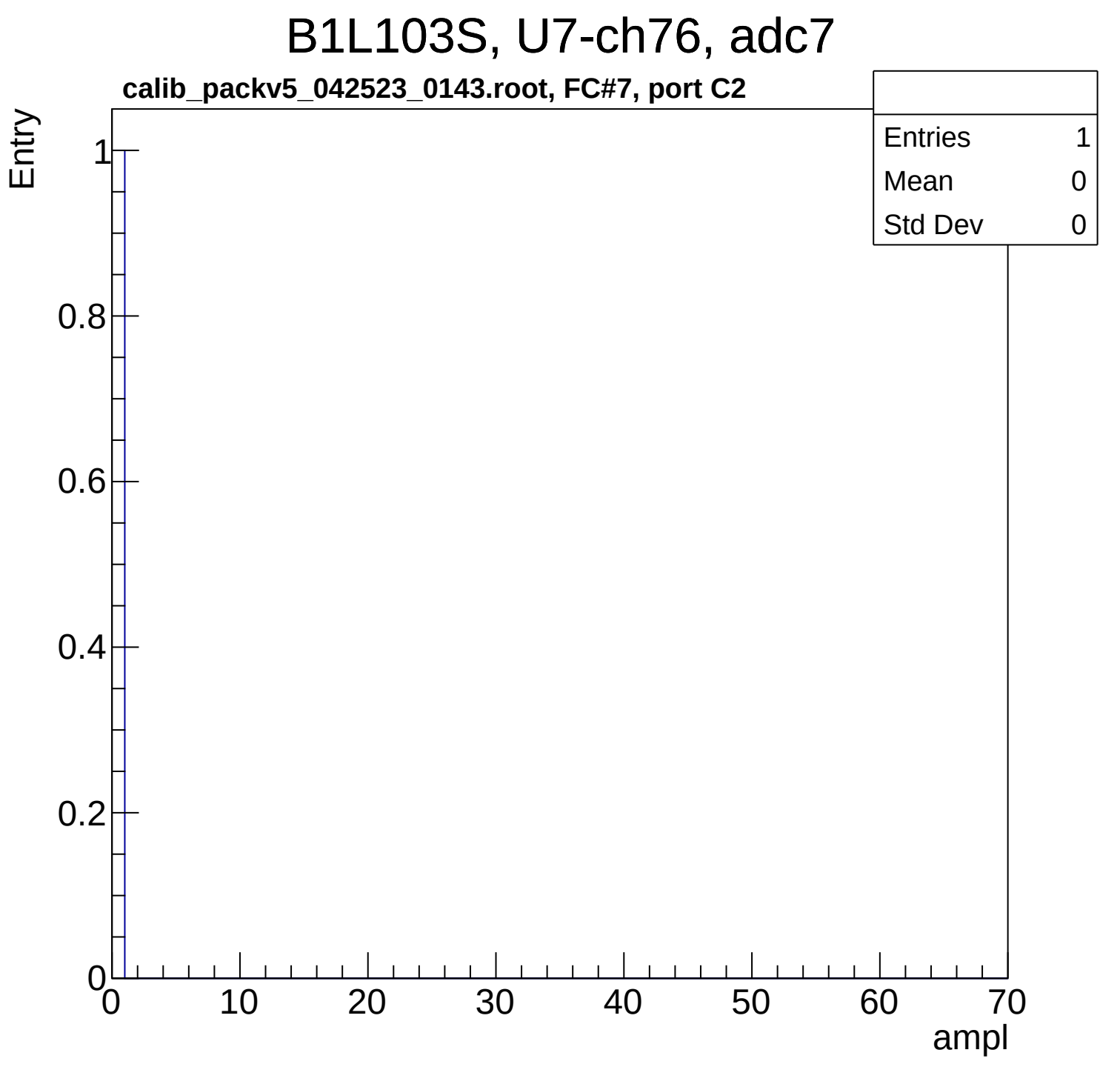
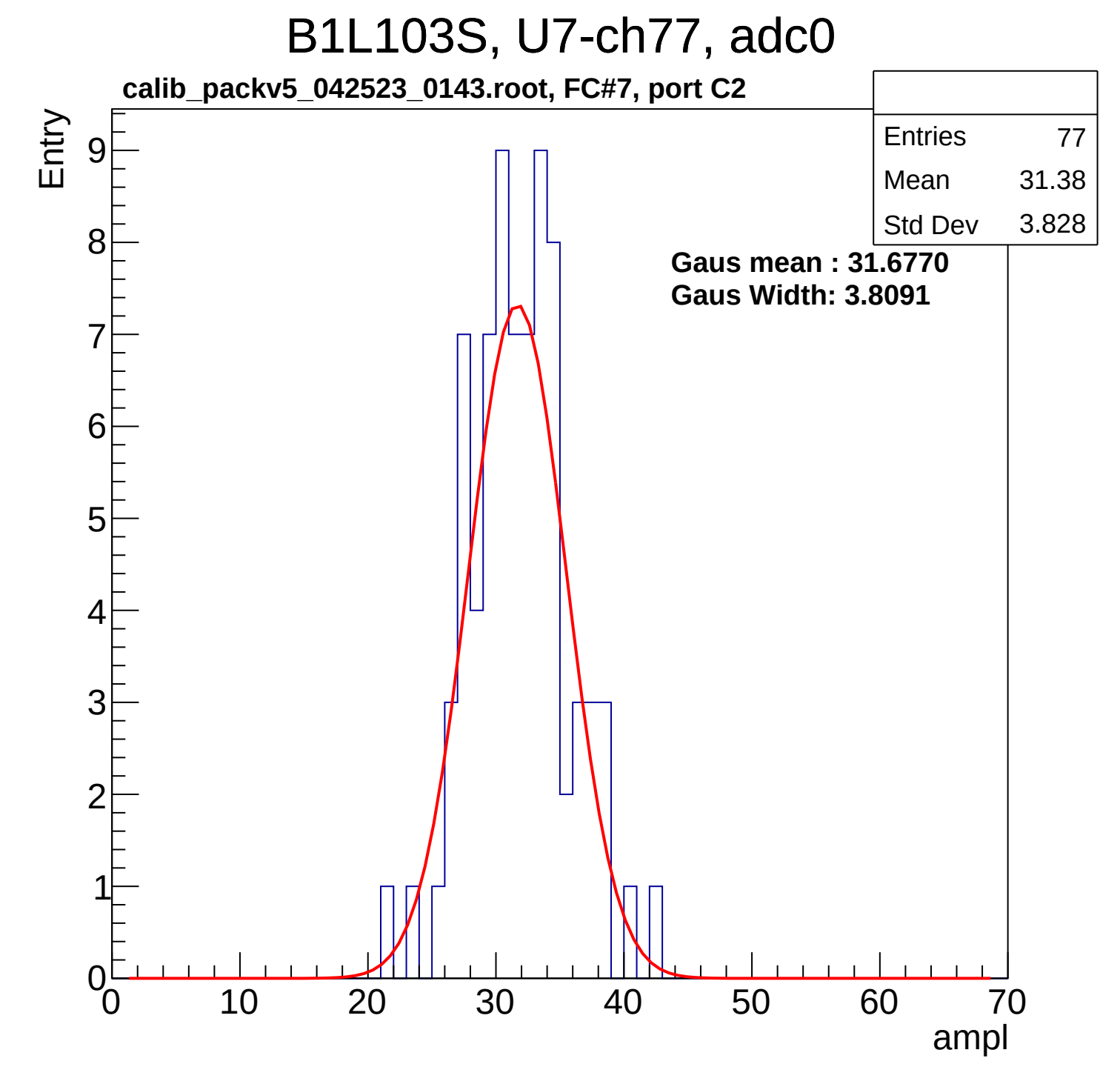

B1L103S, U7-ch76, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 5
Mean 50
Std Dev 25
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U7-ch76, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch77, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 77
Mean 31.38
Std Dev 3.828
Gaus mean : 31.6770
Gaus Width: 3.8091
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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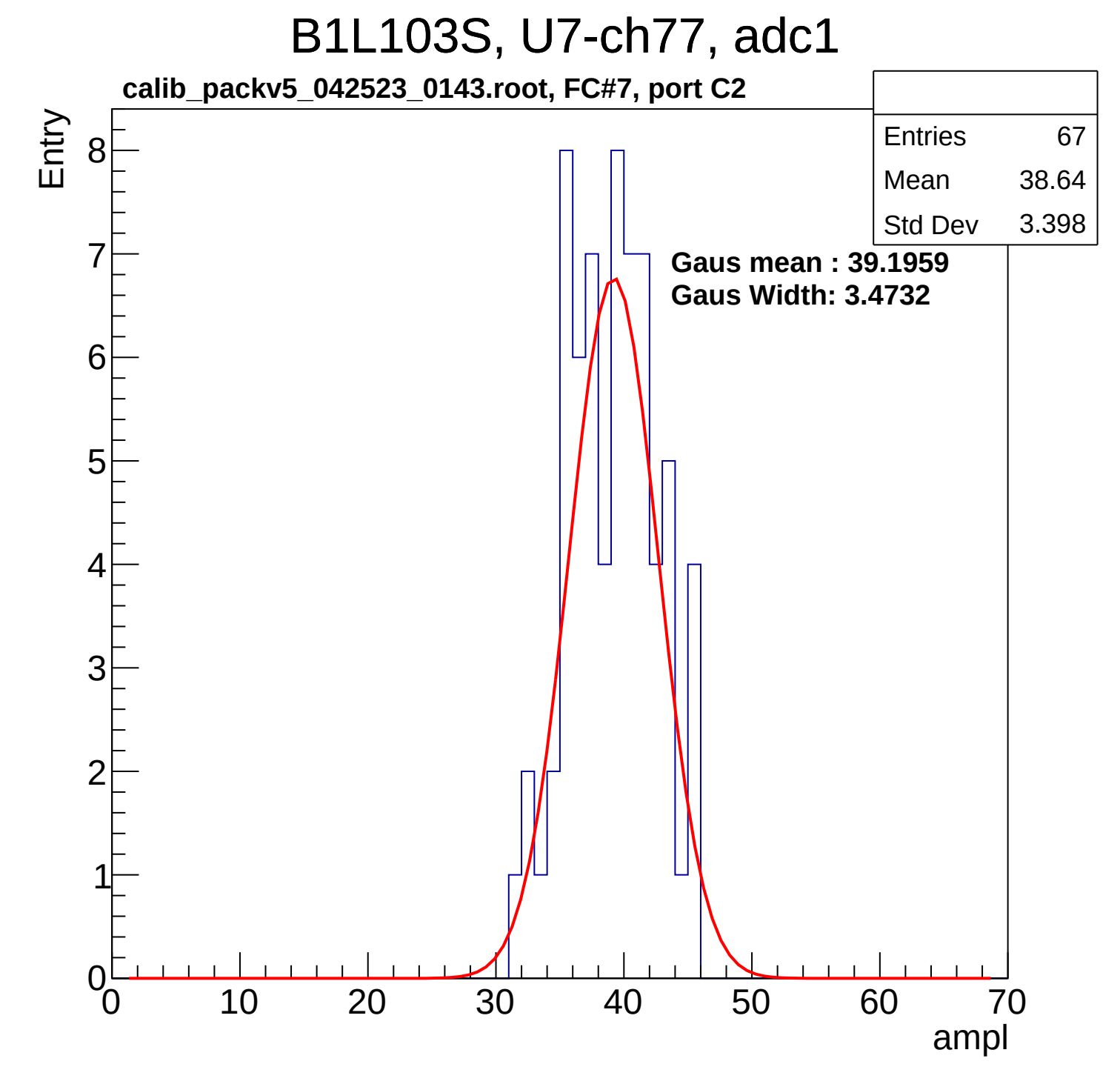
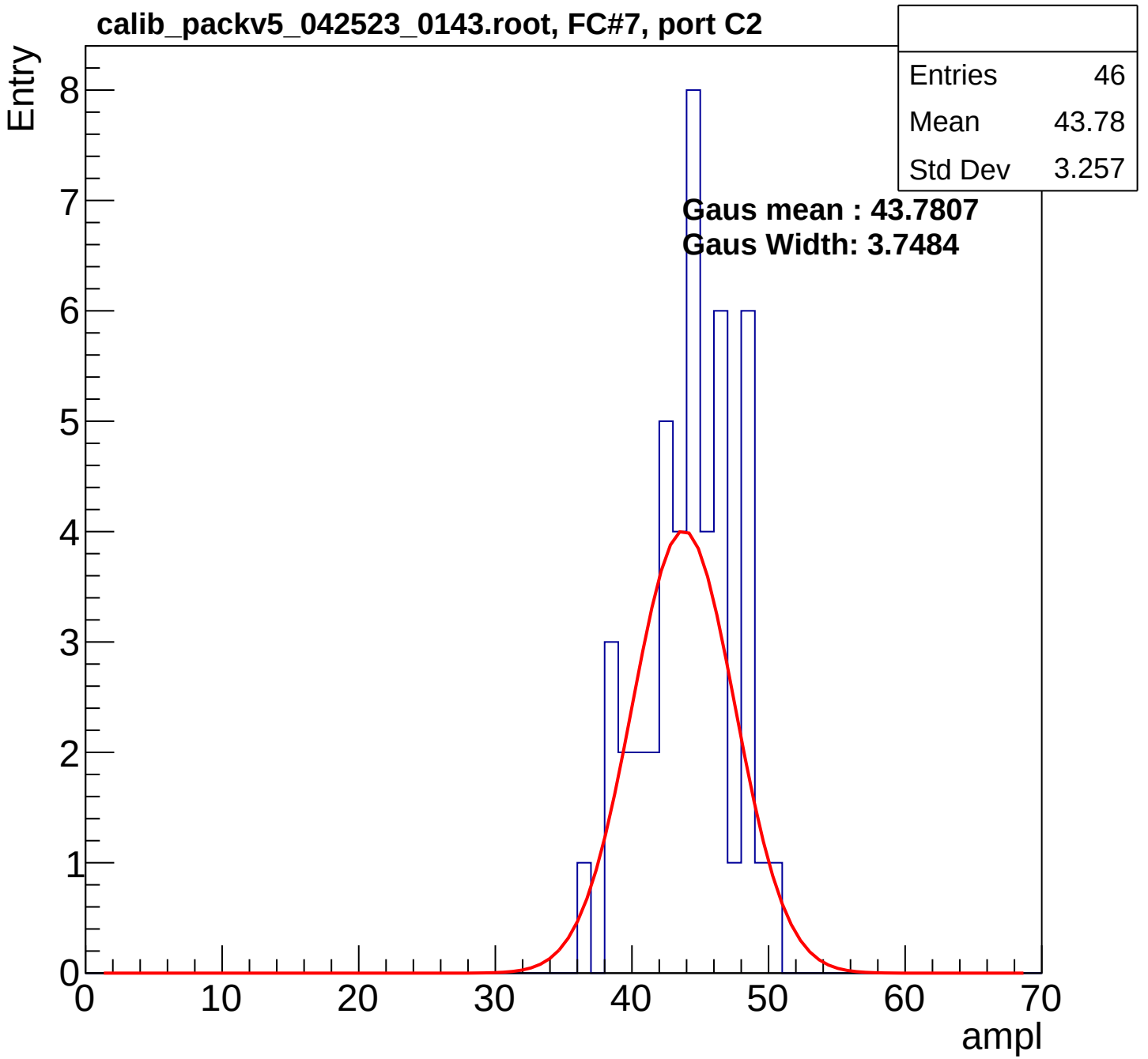

B1L103S, U7-ch77, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 38.64
Std Dev 3.398
Gaus mean : 39.1959
Gaus Width: 3.4732
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch77, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 46
Mean 43.78
Std Dev 3.257
Gaus mean : 43.7807
Gaus Width: 3.7484
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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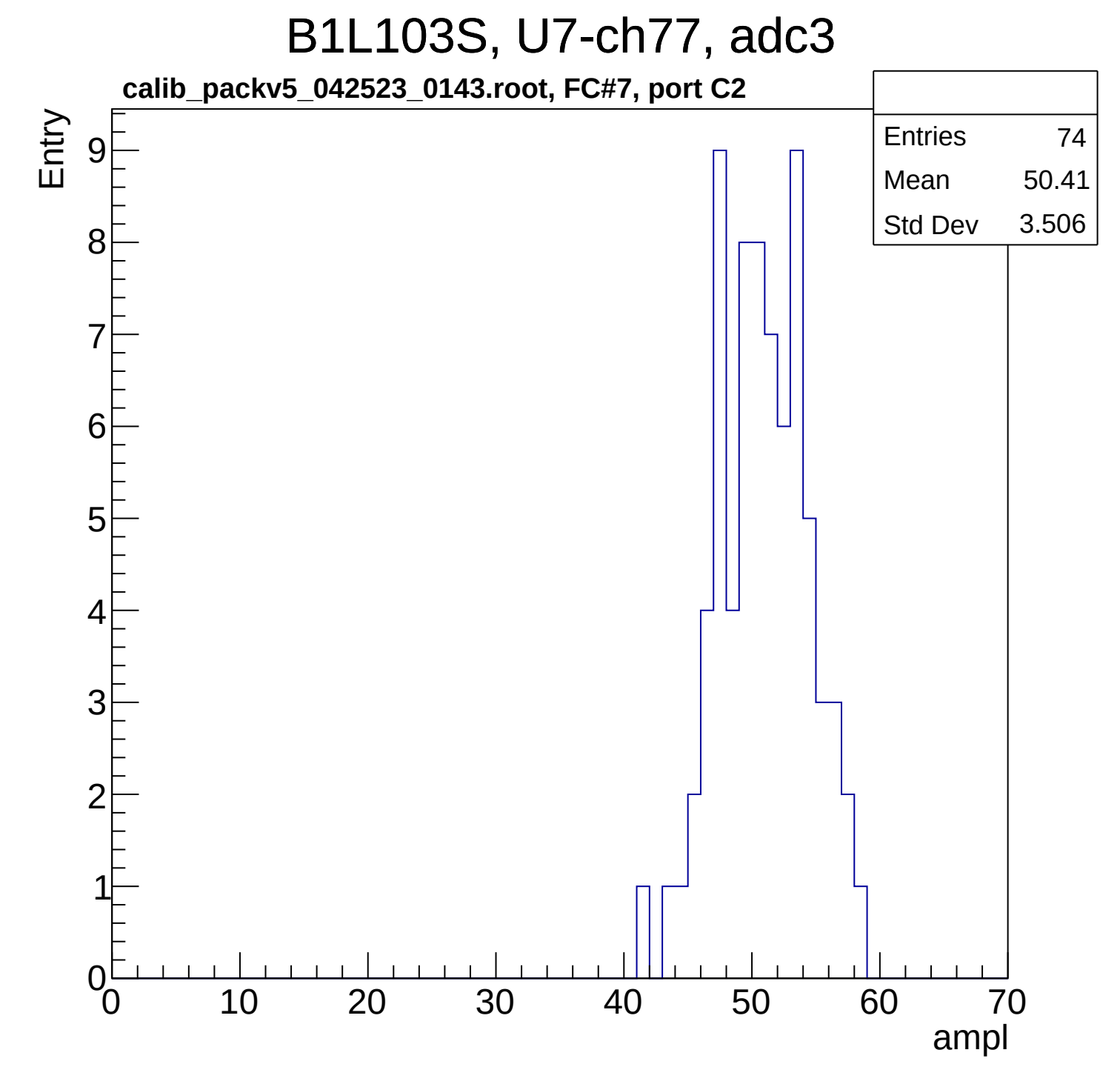
B1L103S, U7-ch77, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 74
Mean 50.41
Std Dev 3.506
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
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60
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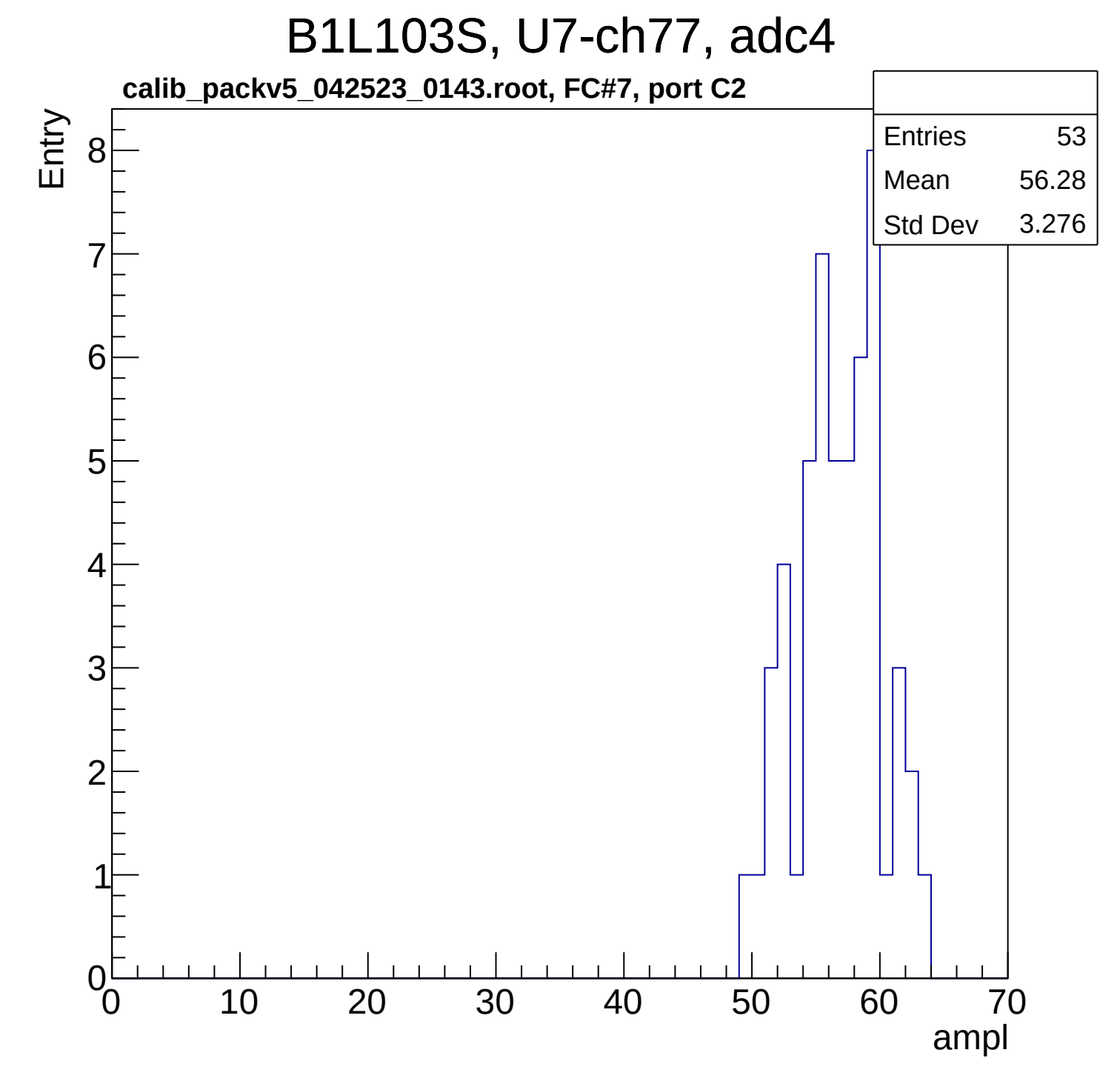
B1L103S, U7-ch77, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 56.28
Std Dev 3.276
Entry
ampl
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1
2
3
4
5
6
7
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0
10
20
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40
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60
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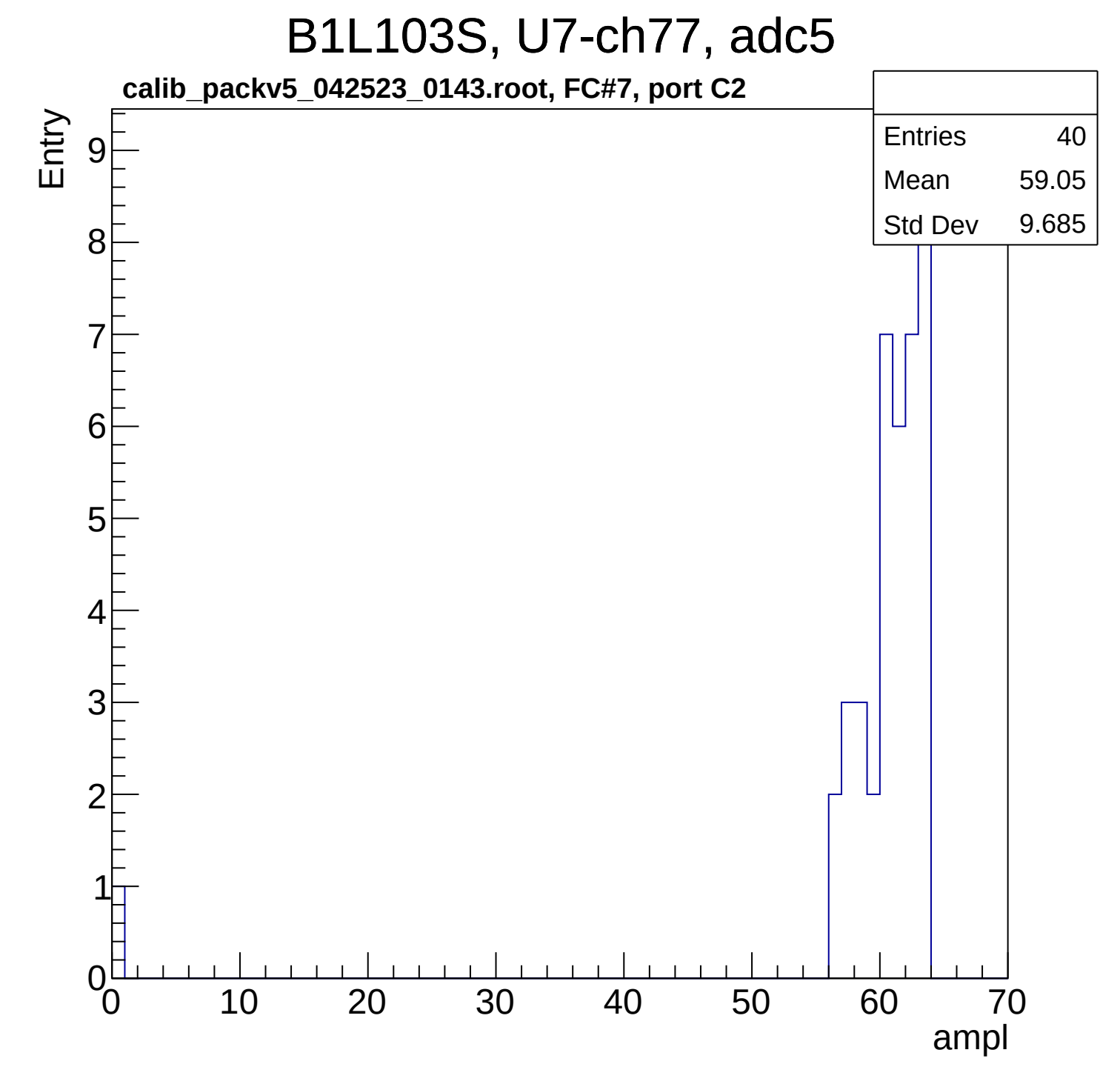
B1L103S, U7-ch77, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 40
Mean 59.05
Std Dev 9.685
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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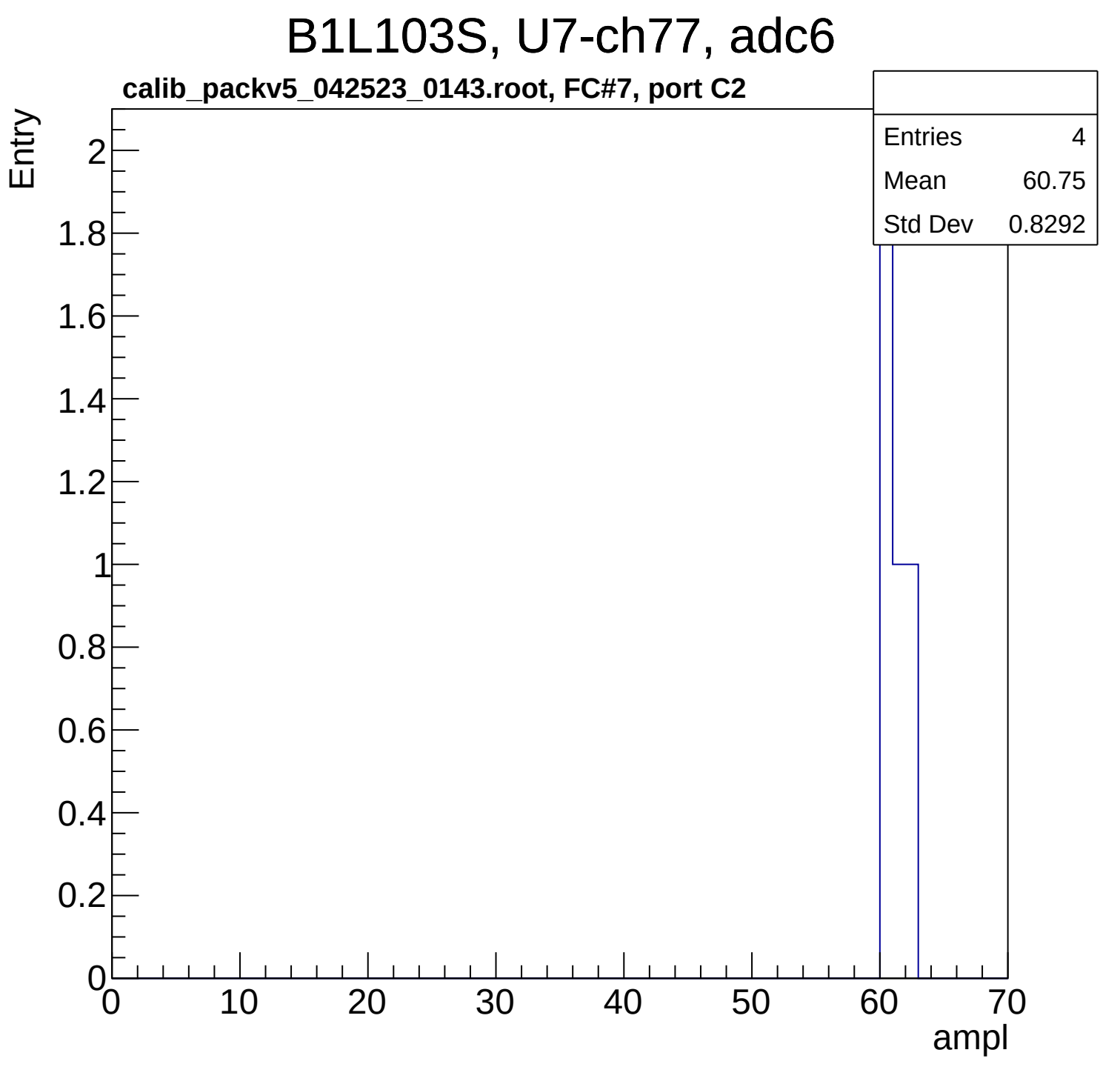
B1L103S, U7-ch77, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 4
Mean 60.75
Std Dev 0.8292
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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20
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40
50
60
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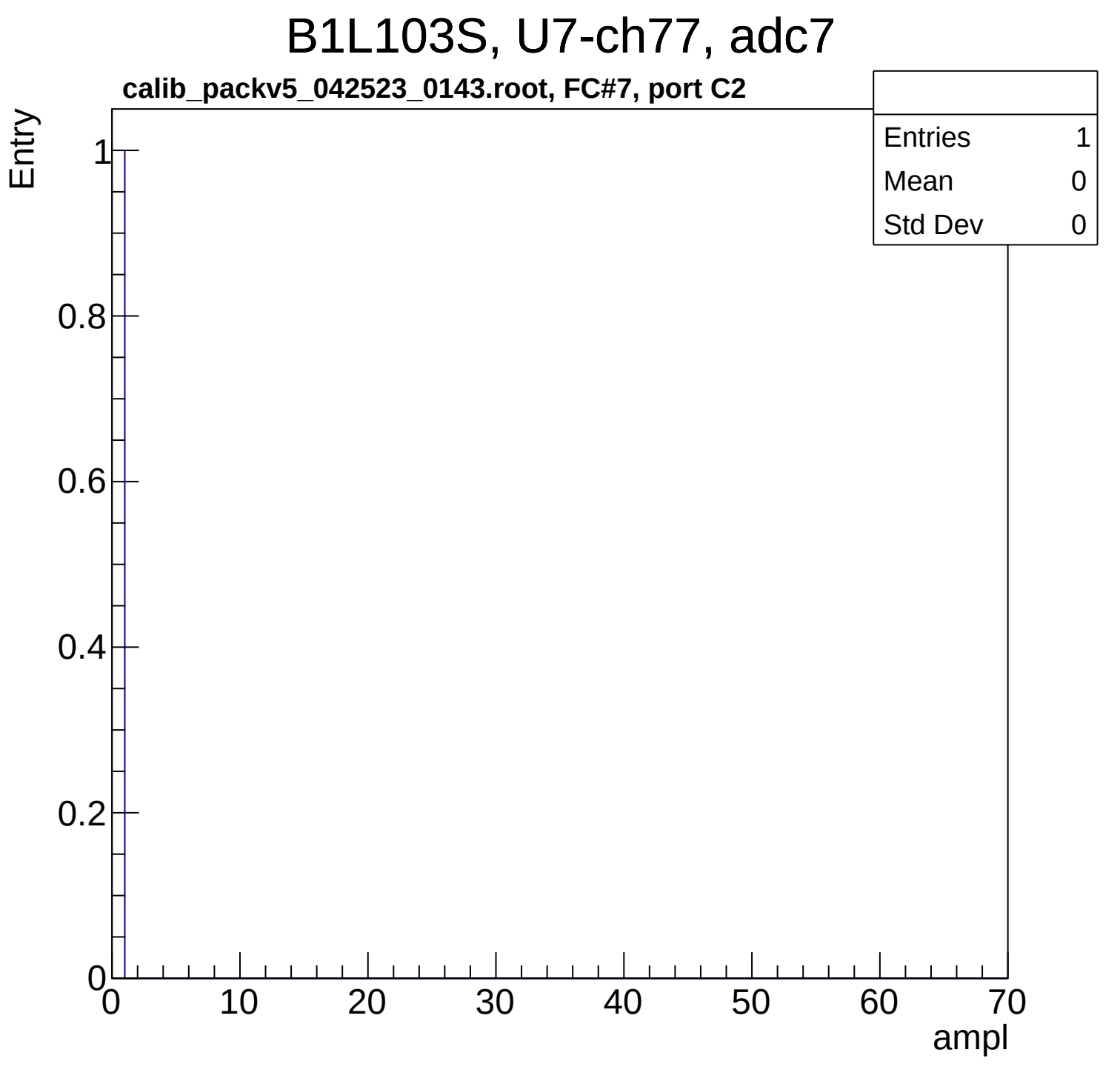
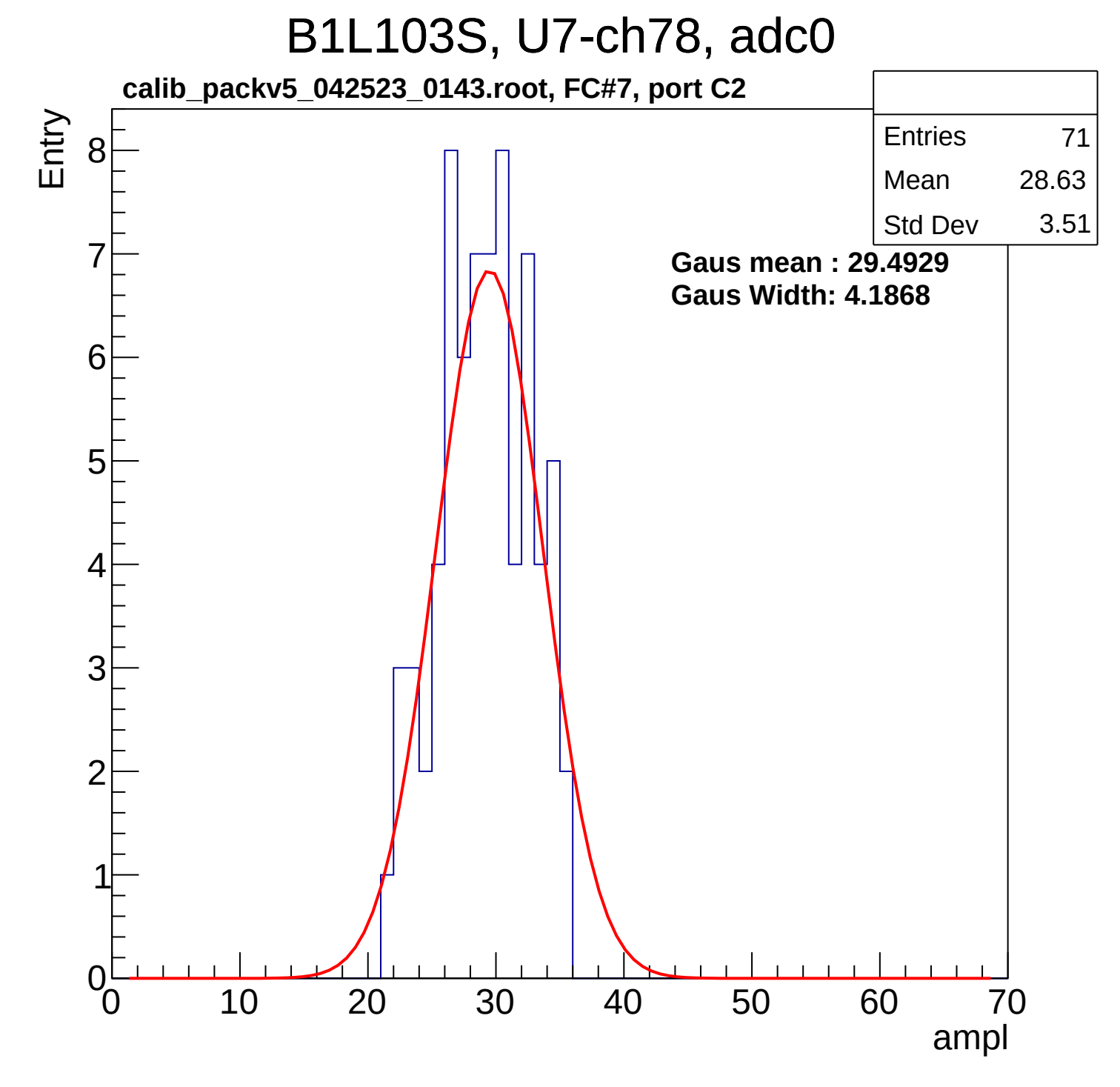
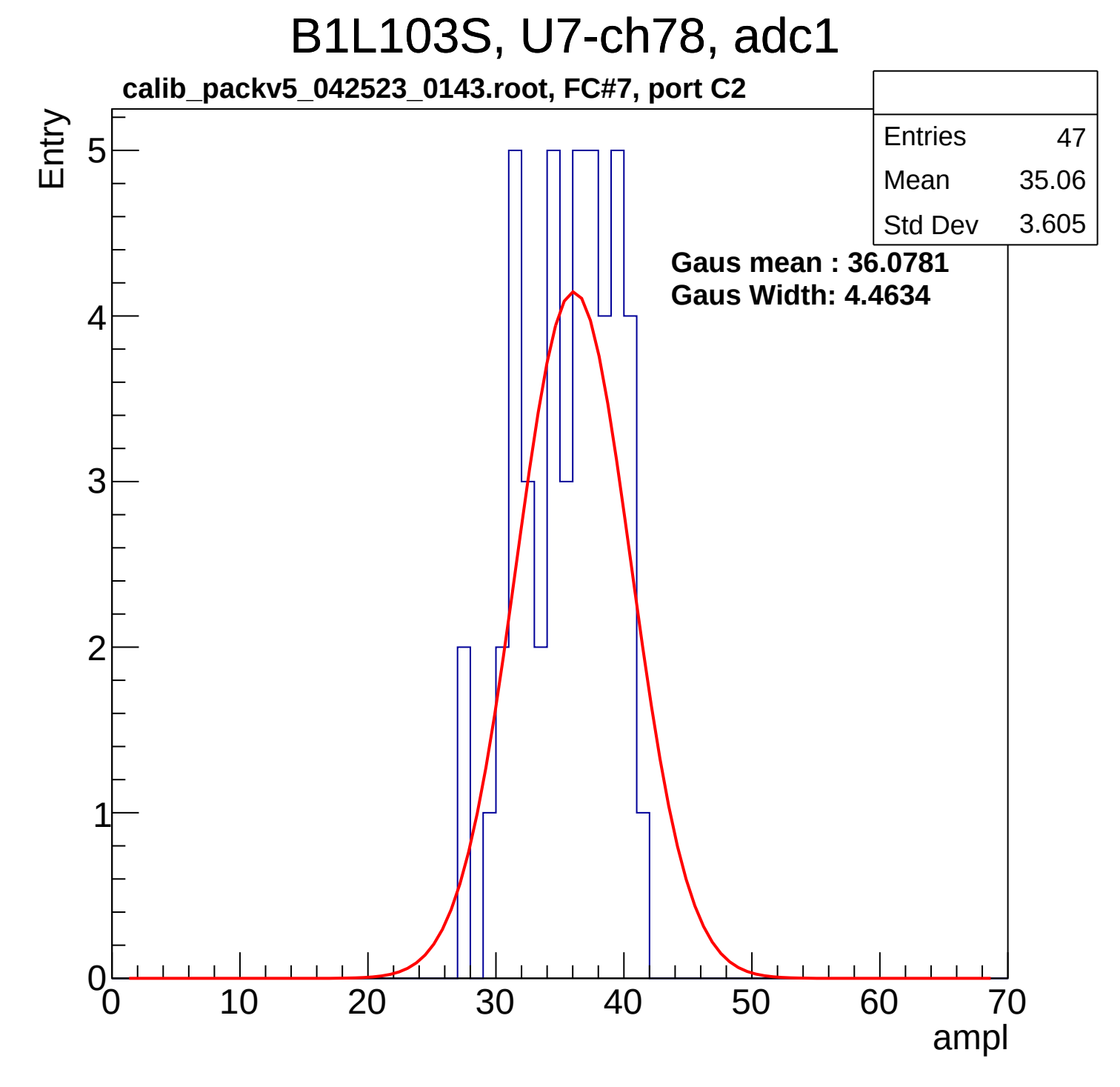
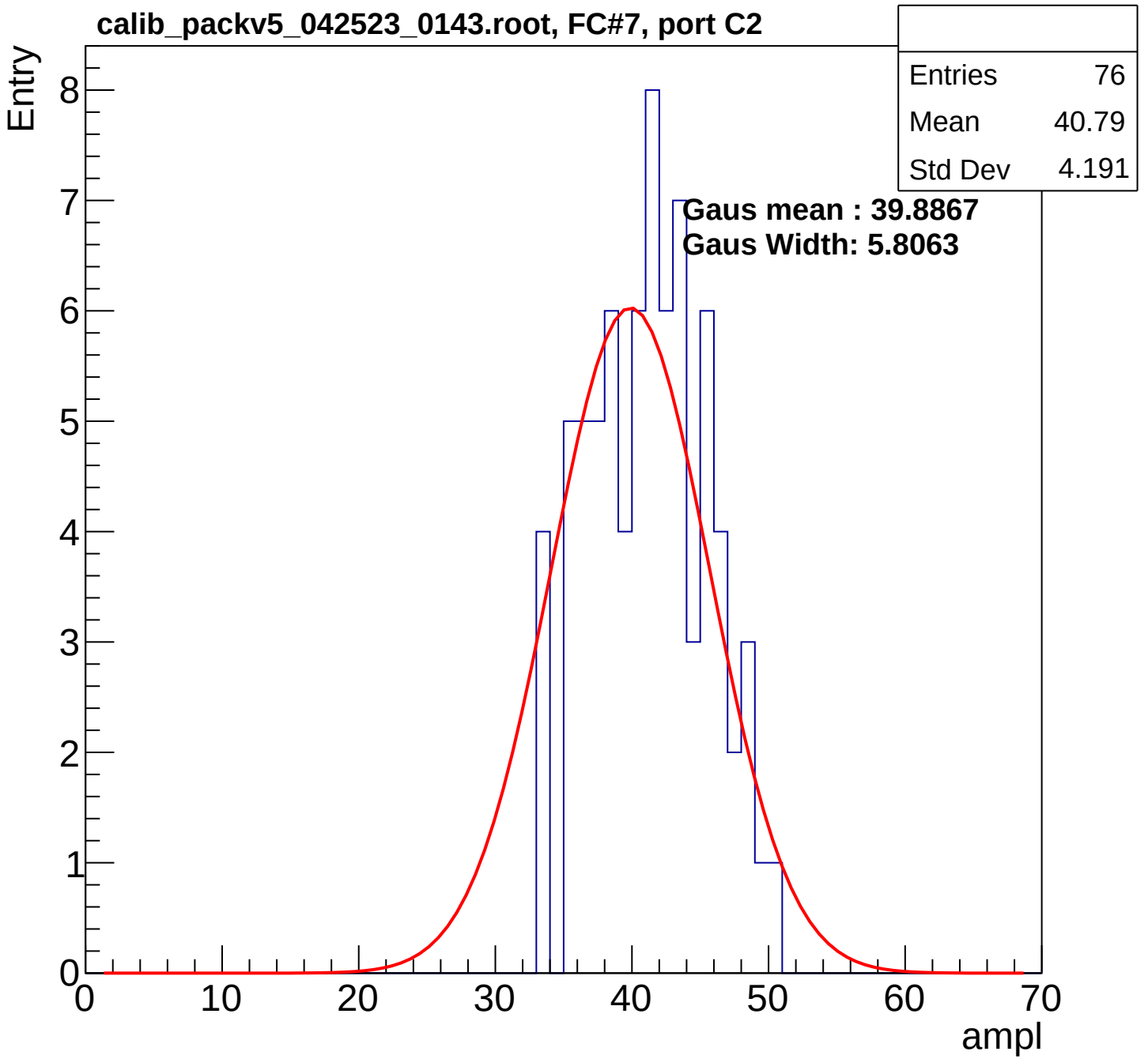

B1L103S, U7-ch77, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch78, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 71
Mean 28.63
Std Dev 3.51
Gaus mean : 29.4929
Gaus Width: 4.1868
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch78, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 47
Mean 35.06
Std Dev 3.605
Gaus mean : 36.0781
Gaus Width: 4.4634
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U7-ch78, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 76
Mean 40.79
Std Dev 4.191
Gaus mean : 39.8867
Gaus Width: 5.8063
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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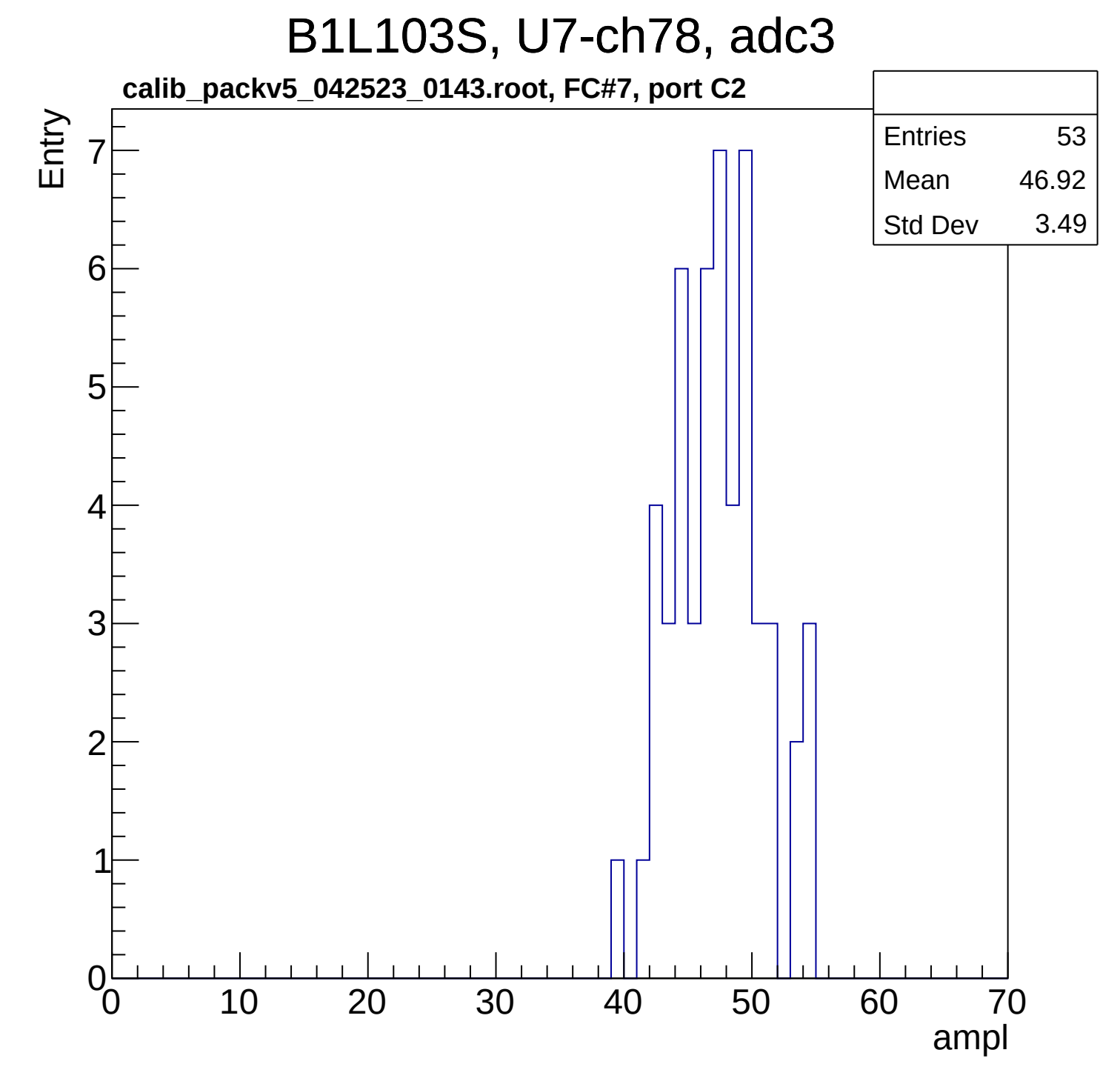
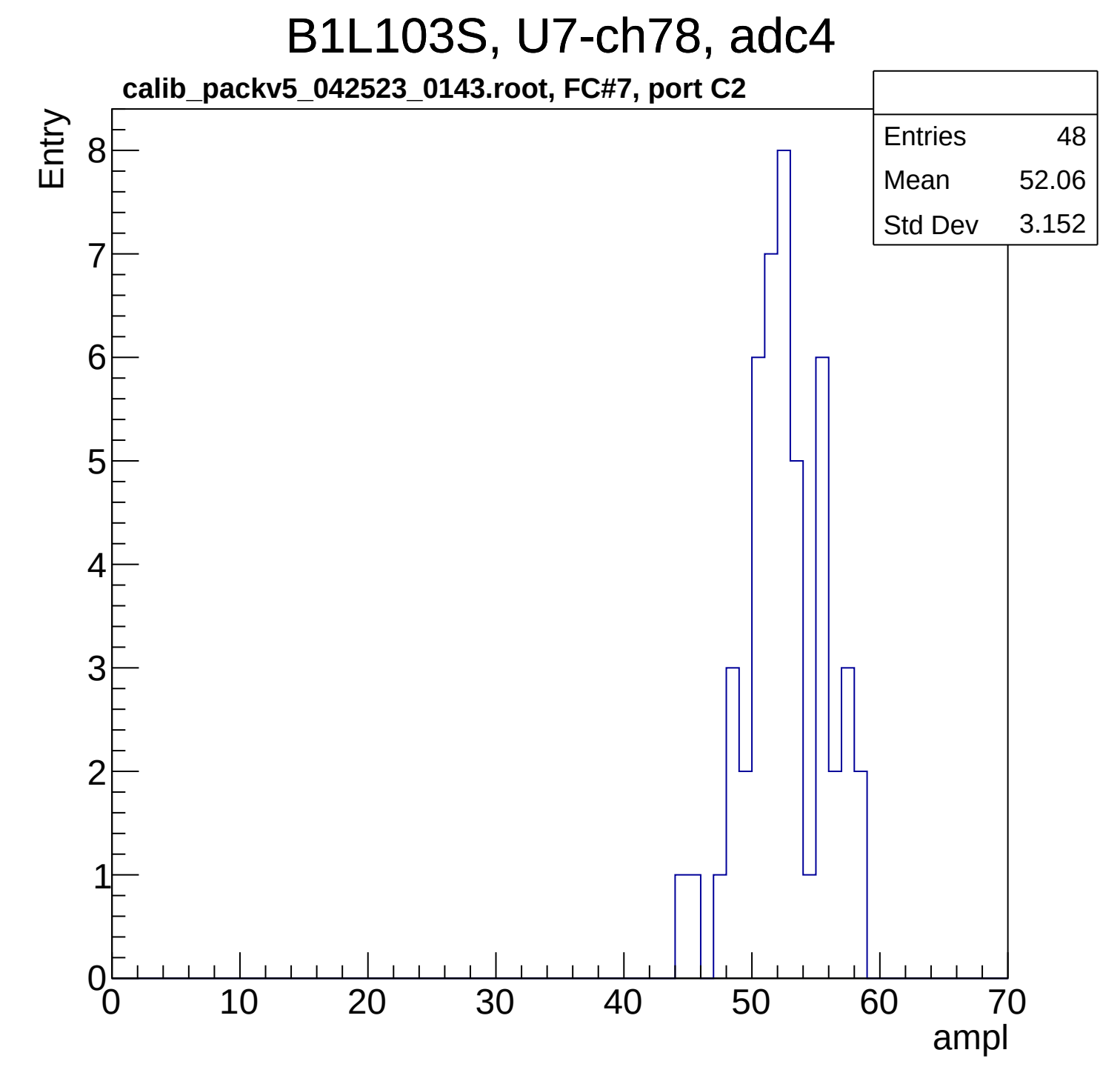

B1L103S, U7-ch78, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 46.92
Std Dev 3.49
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch78, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 48
Mean 52.06
Std Dev 3.152
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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40
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60
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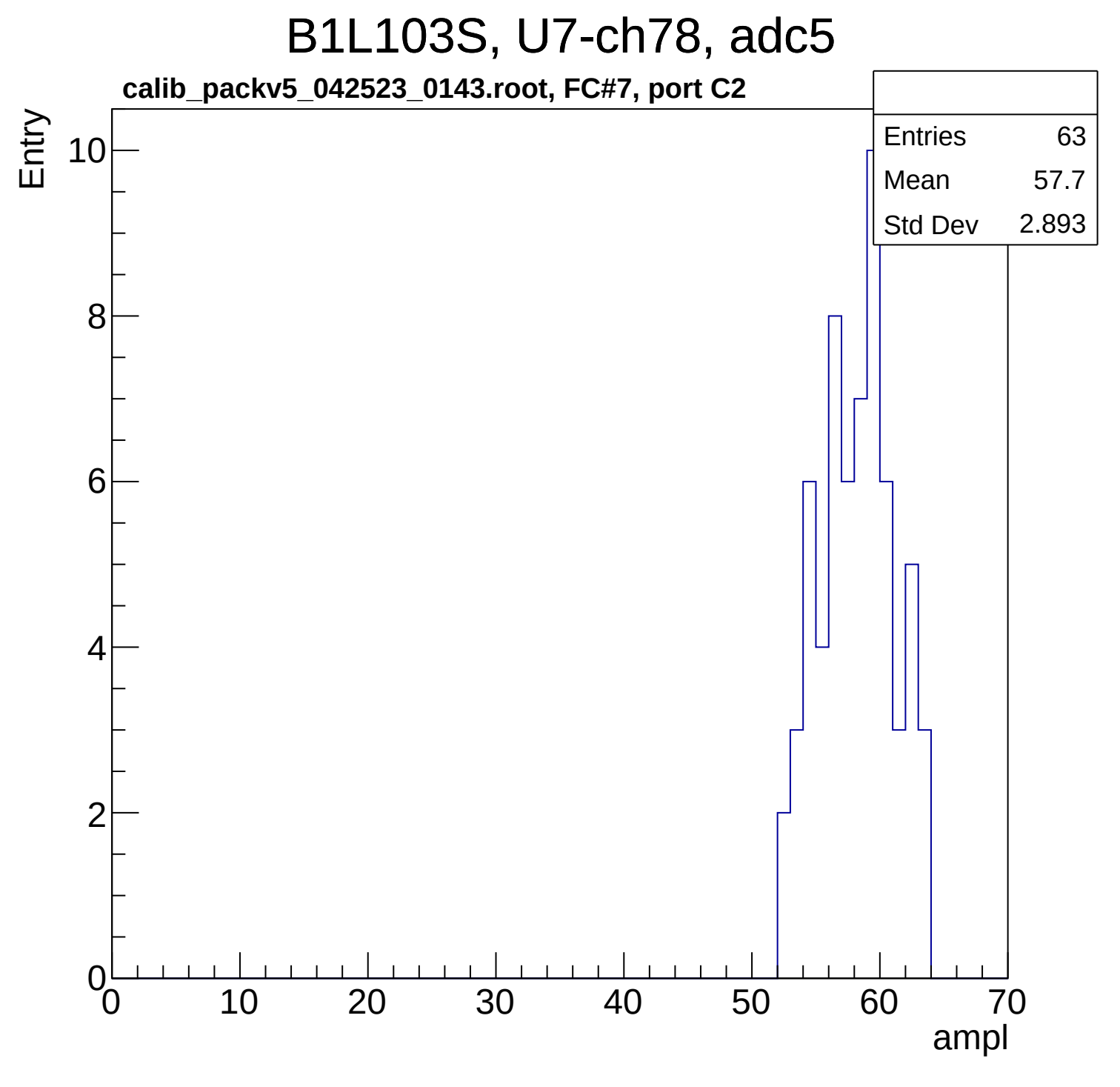
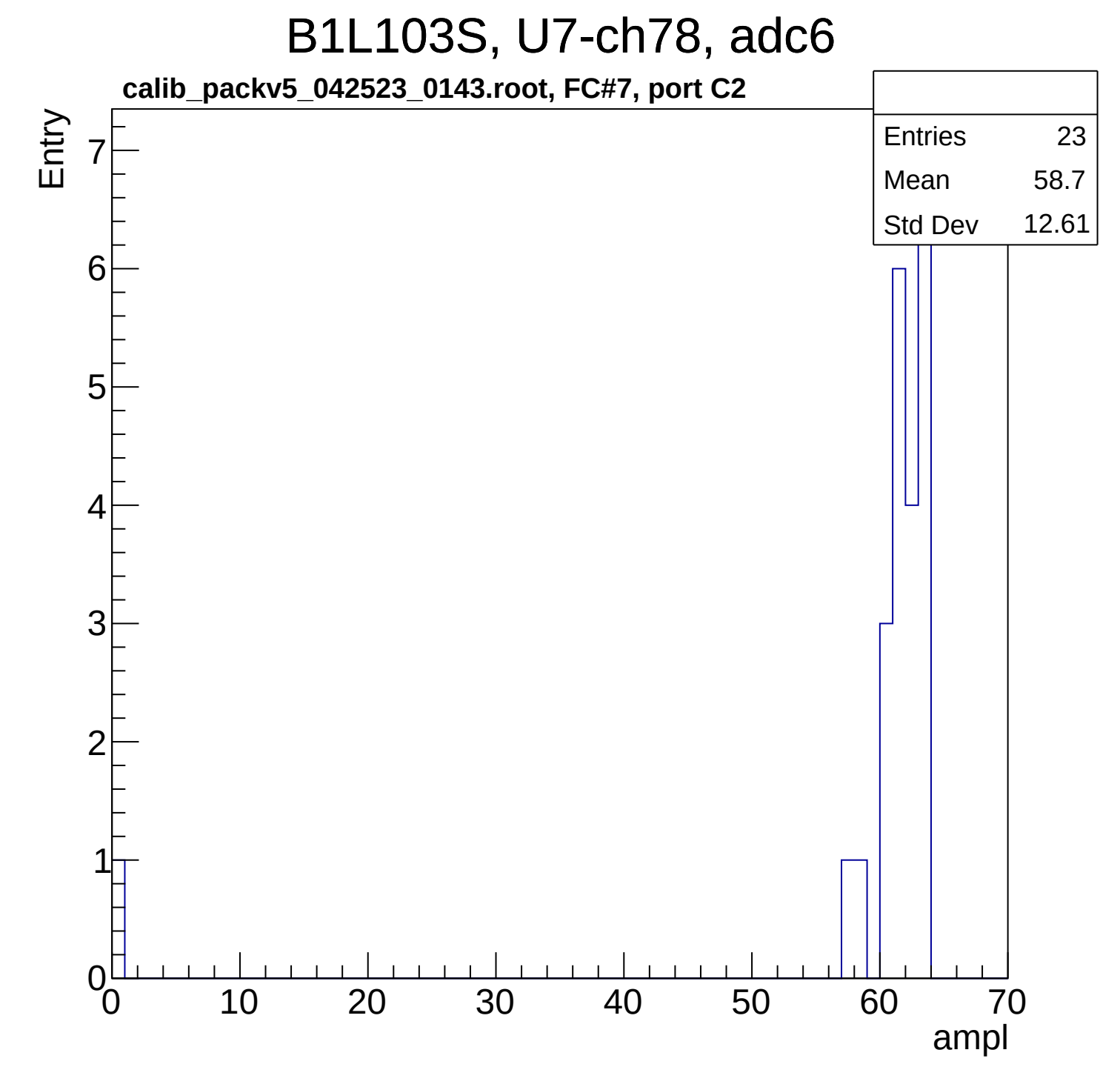

B1L103S, U7-ch78, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 57.7
Std Dev 2.893
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch78, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 23
Mean 58.7
Std Dev 12.61
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
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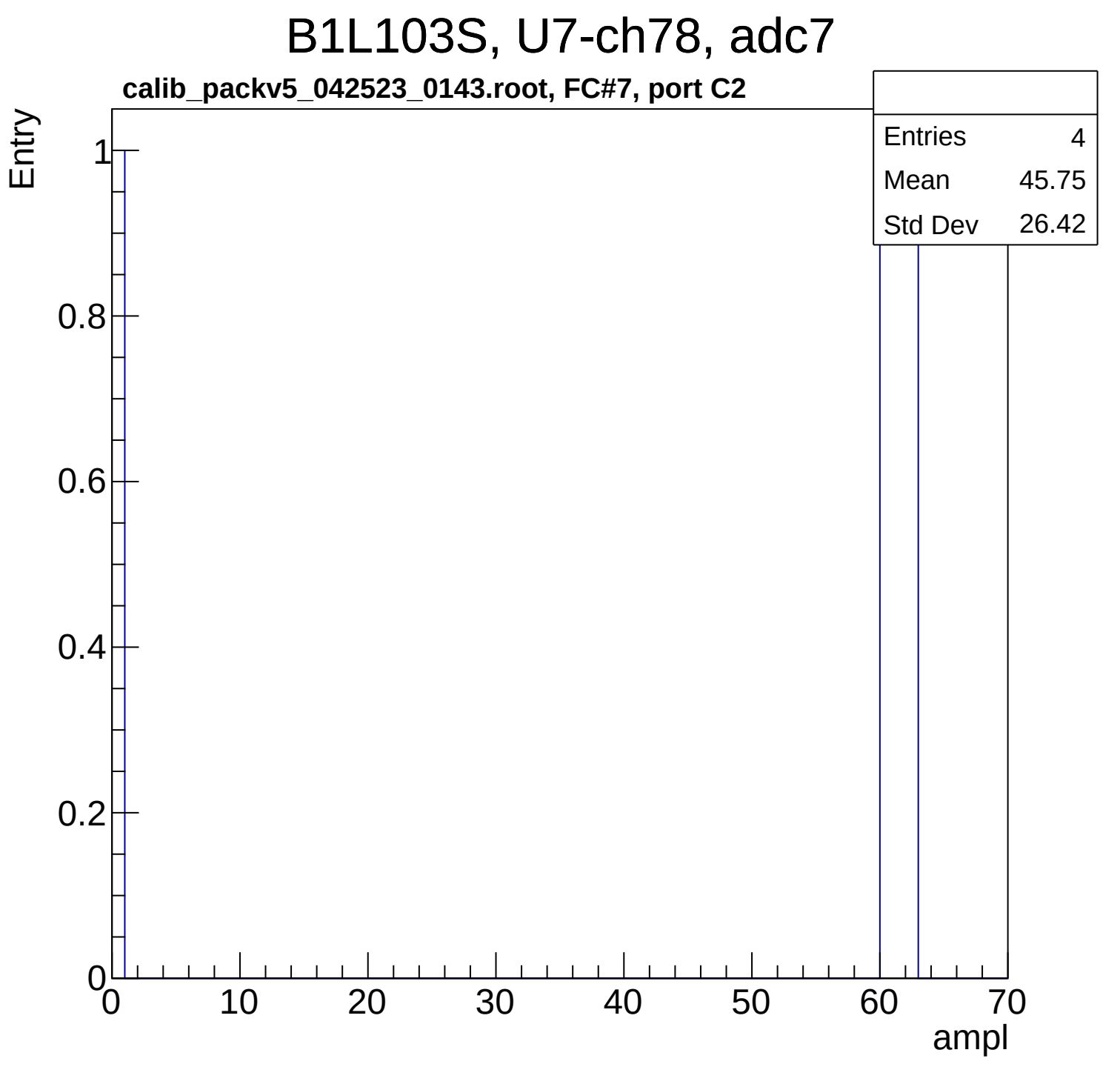
B1L103S, U7-ch78, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 4
Mean 45.75
Std Dev 26.42
Entry
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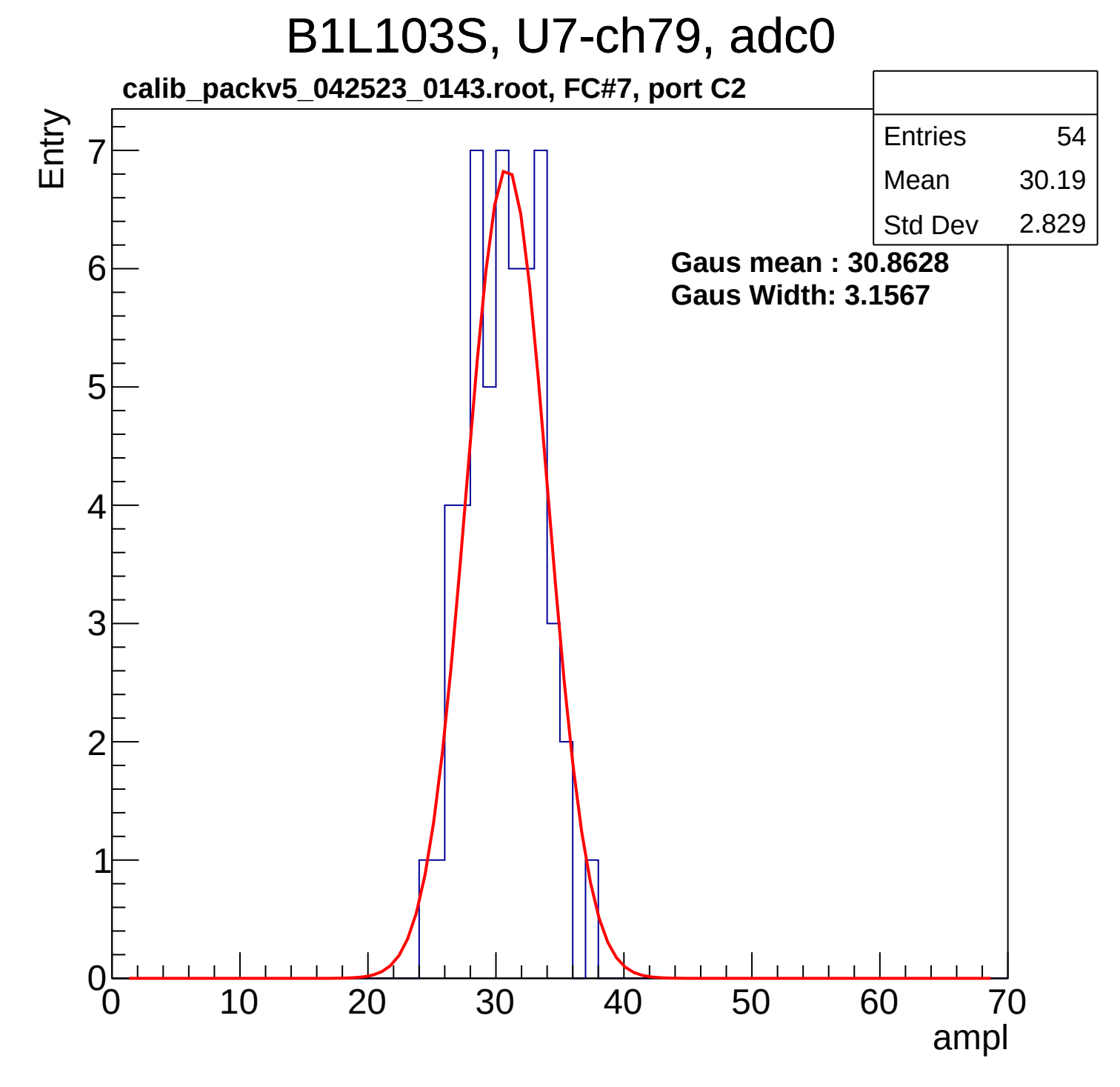
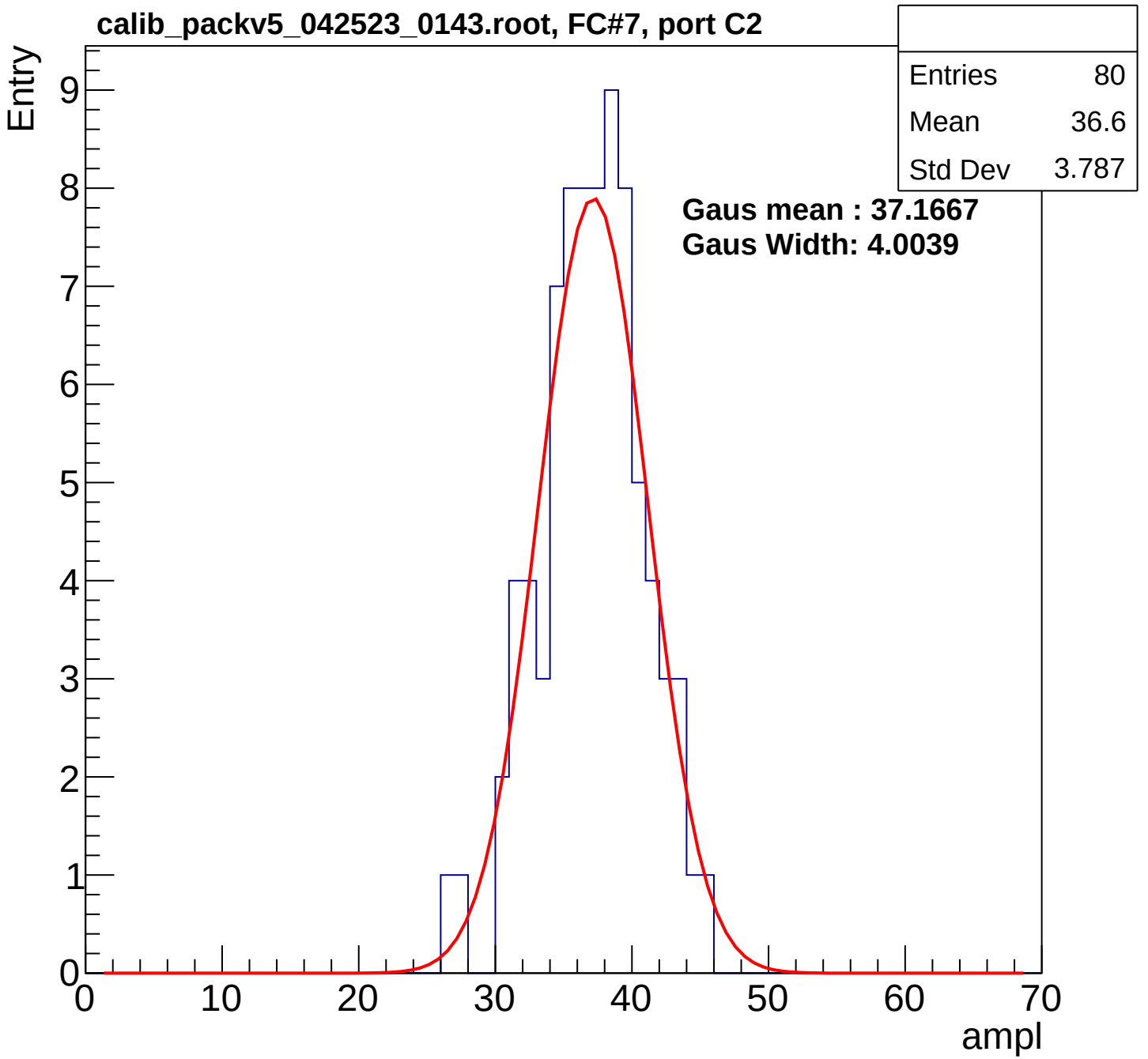
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch79, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 54
Mean 30.19
Std Dev 2.829
Gaus mean : 30.8628
Gaus Width: 3.1567
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch79, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 80
Mean 36.6
Std Dev 3.787
Gaus mean : 37.1667
Gaus Width: 4.0039
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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60
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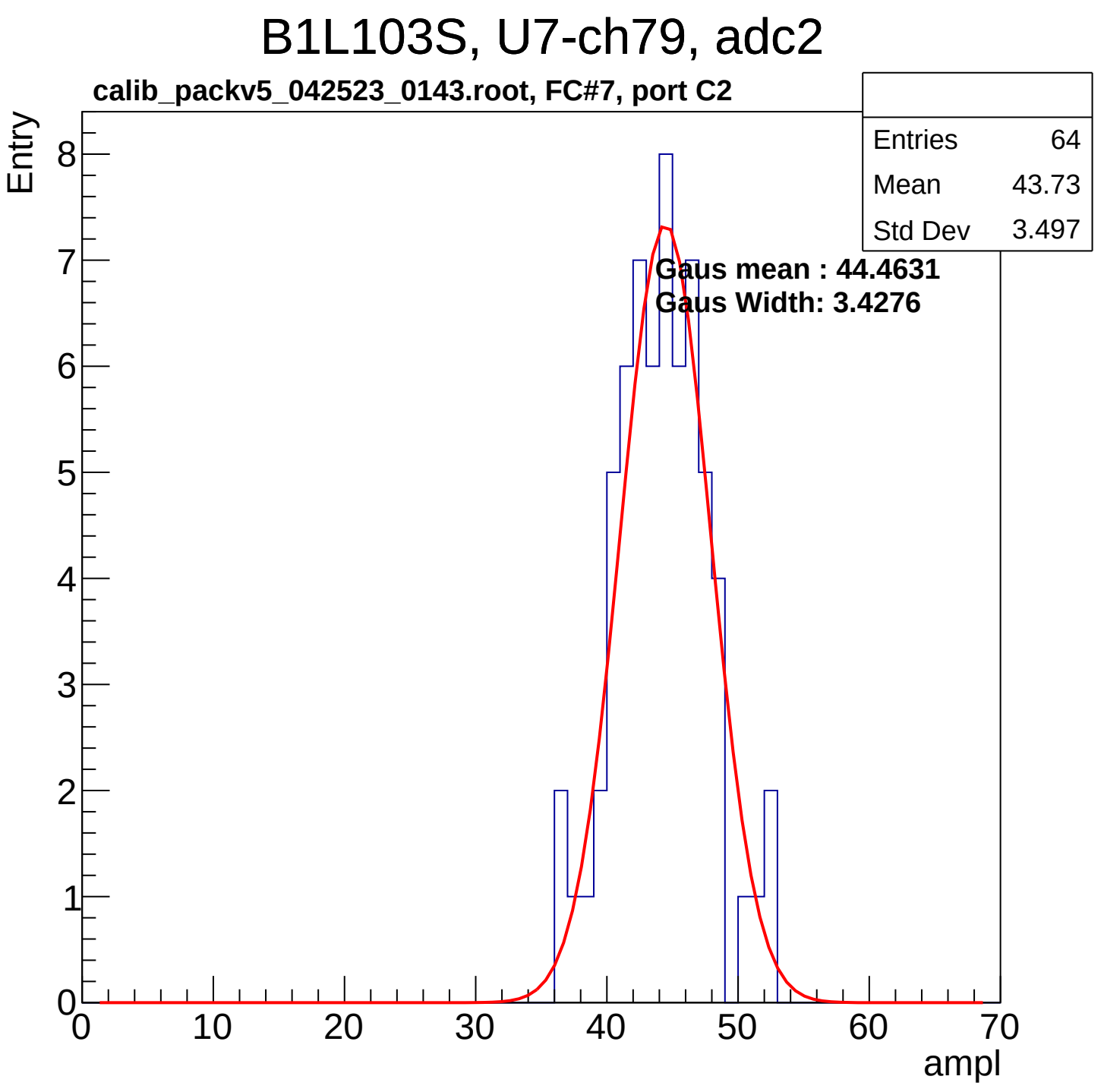
B1L103S, U7-ch79, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 43.73
Std Dev 3.497
Gaus mean : 44.4631
Gaus Width: 3.4276
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
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40
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60
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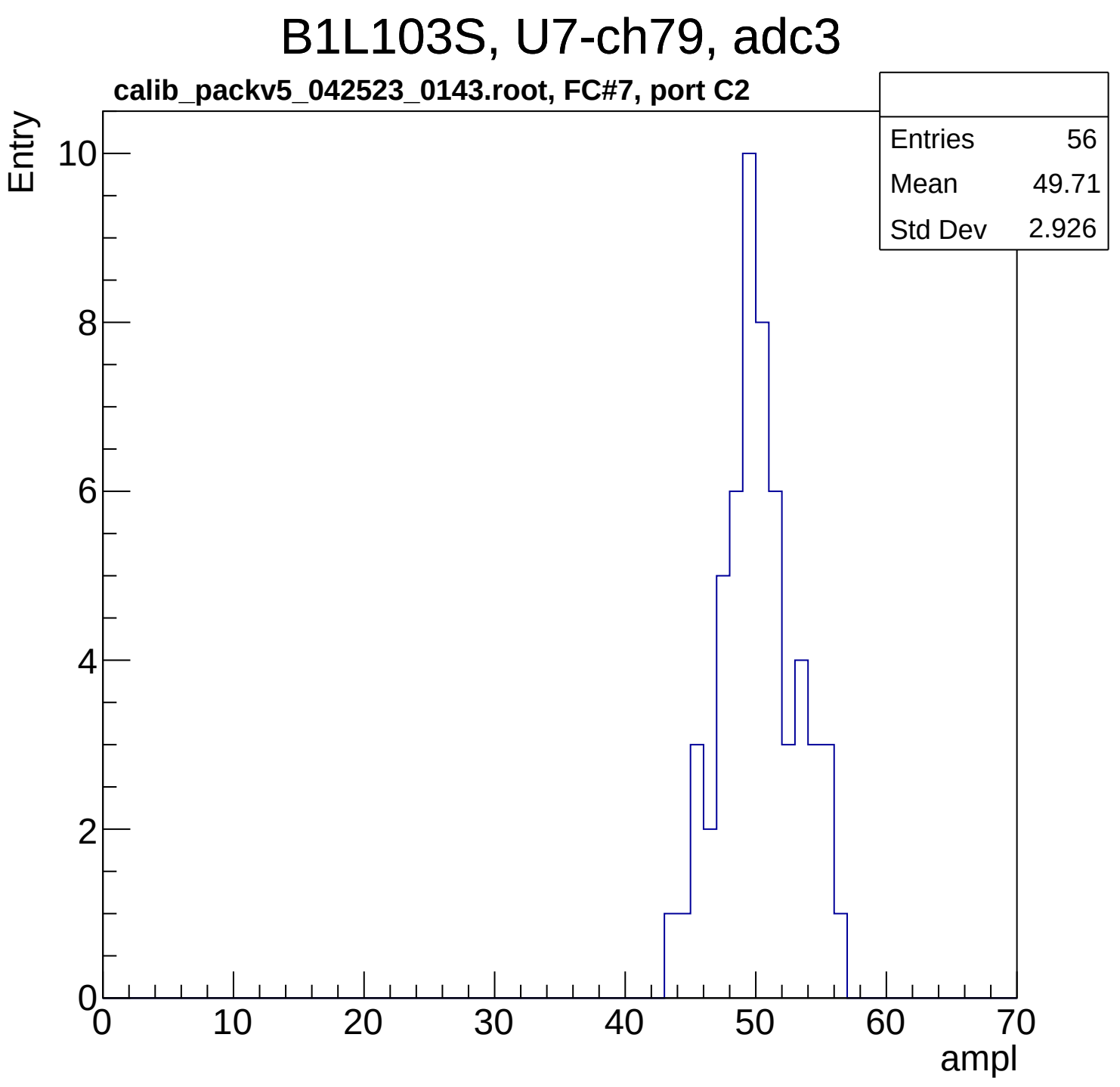
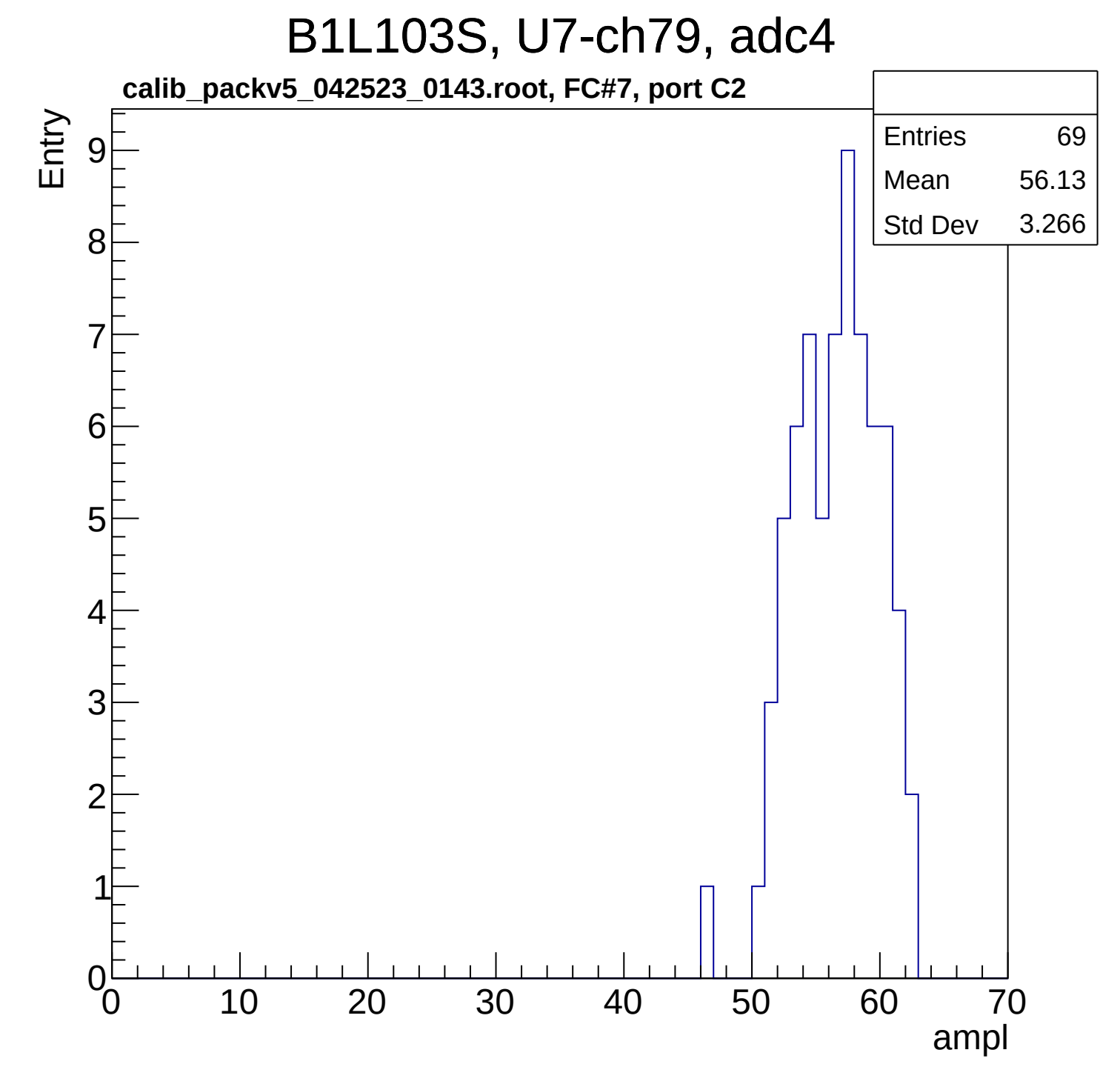

B1L103S, U7-ch79, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 49.71
Std Dev 2.926
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch79, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 56.13
Std Dev 3.266
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
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60
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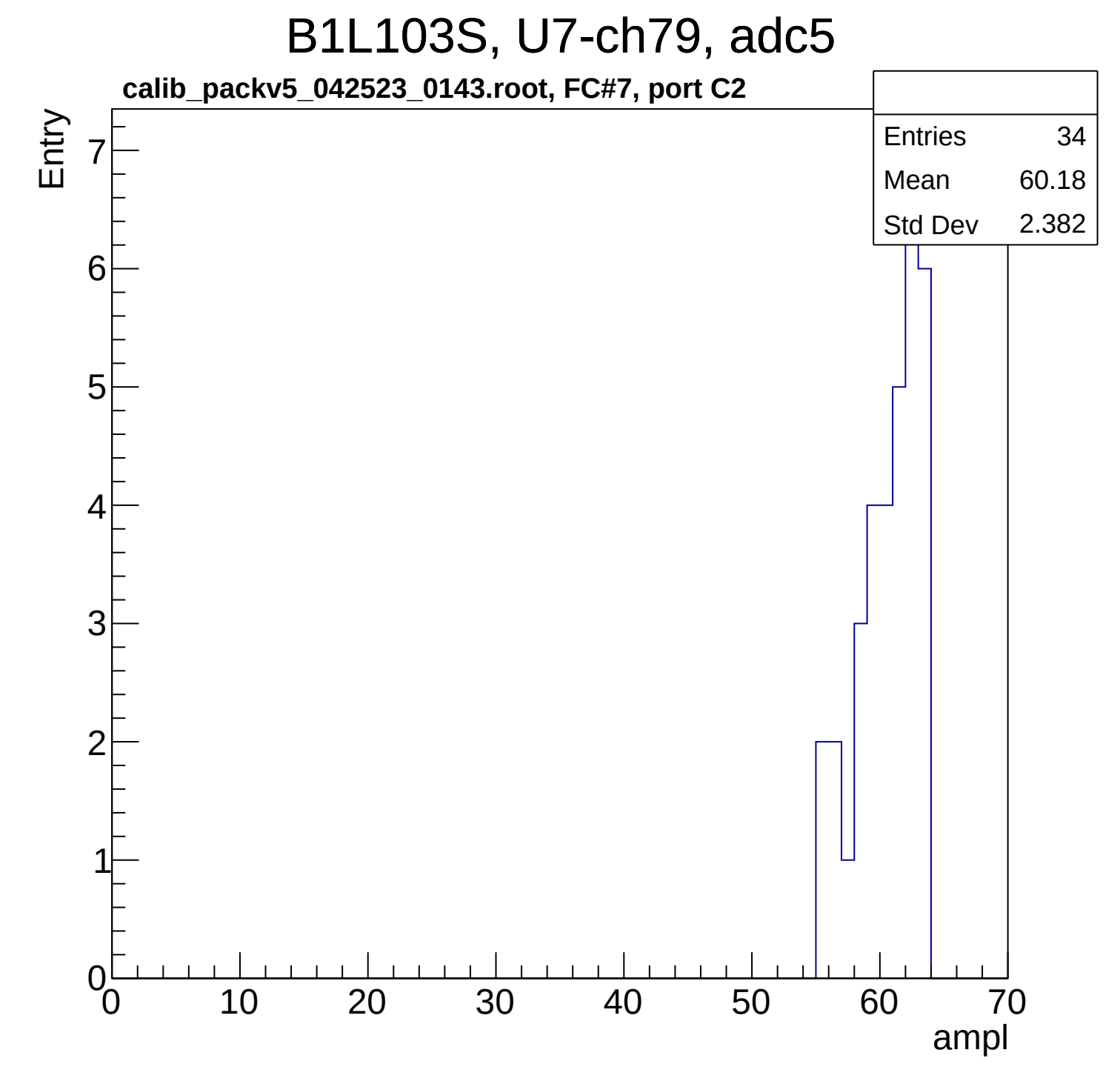
B1L103S, U7-ch79, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 34
Mean 60.18
Std Dev 2.382
Entry
ampl
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1
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0
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60
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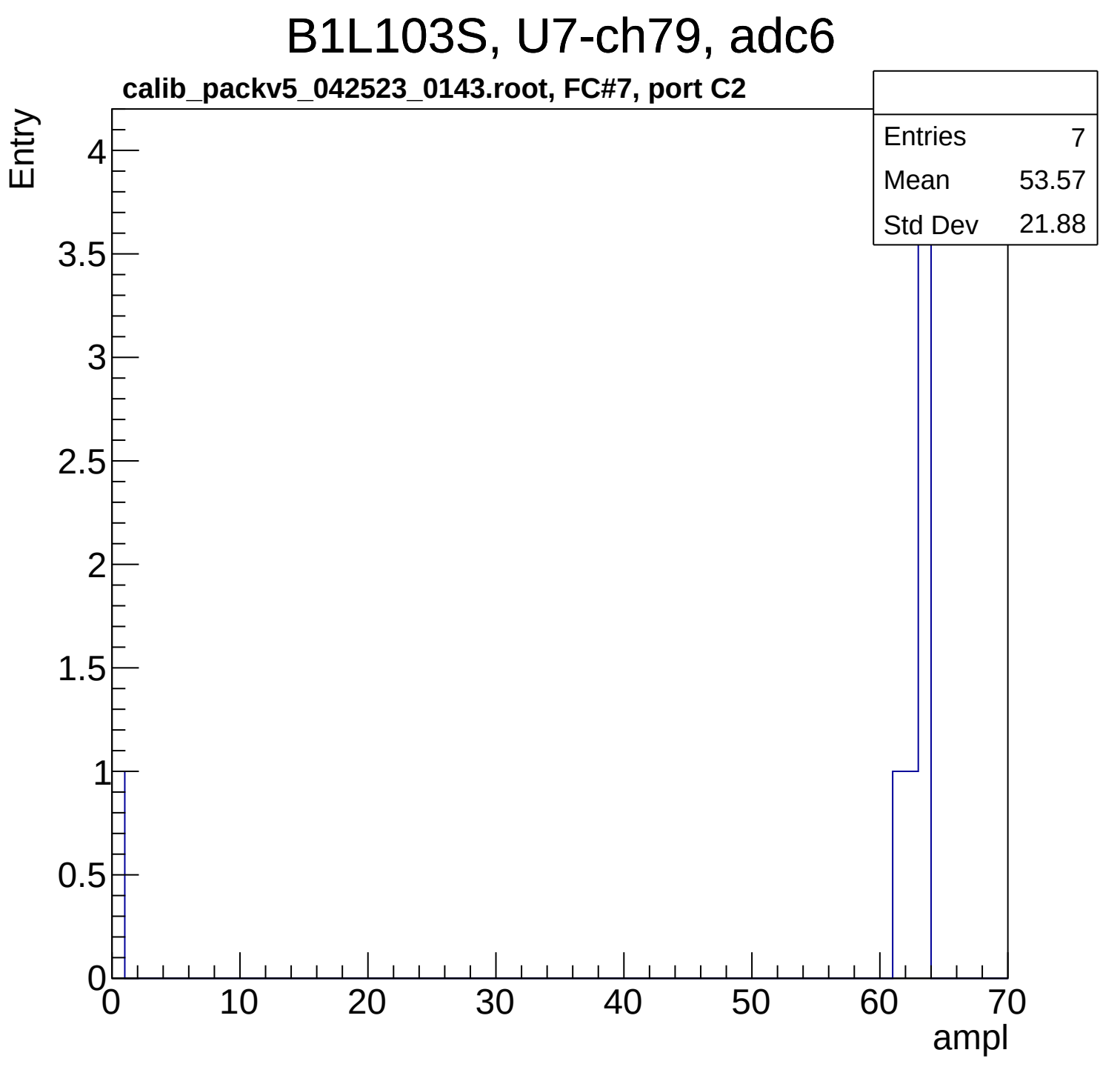
B1L103S, U7-ch79, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 7
Mean 53.57
Std Dev 21.88
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
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20
30
40
50
60
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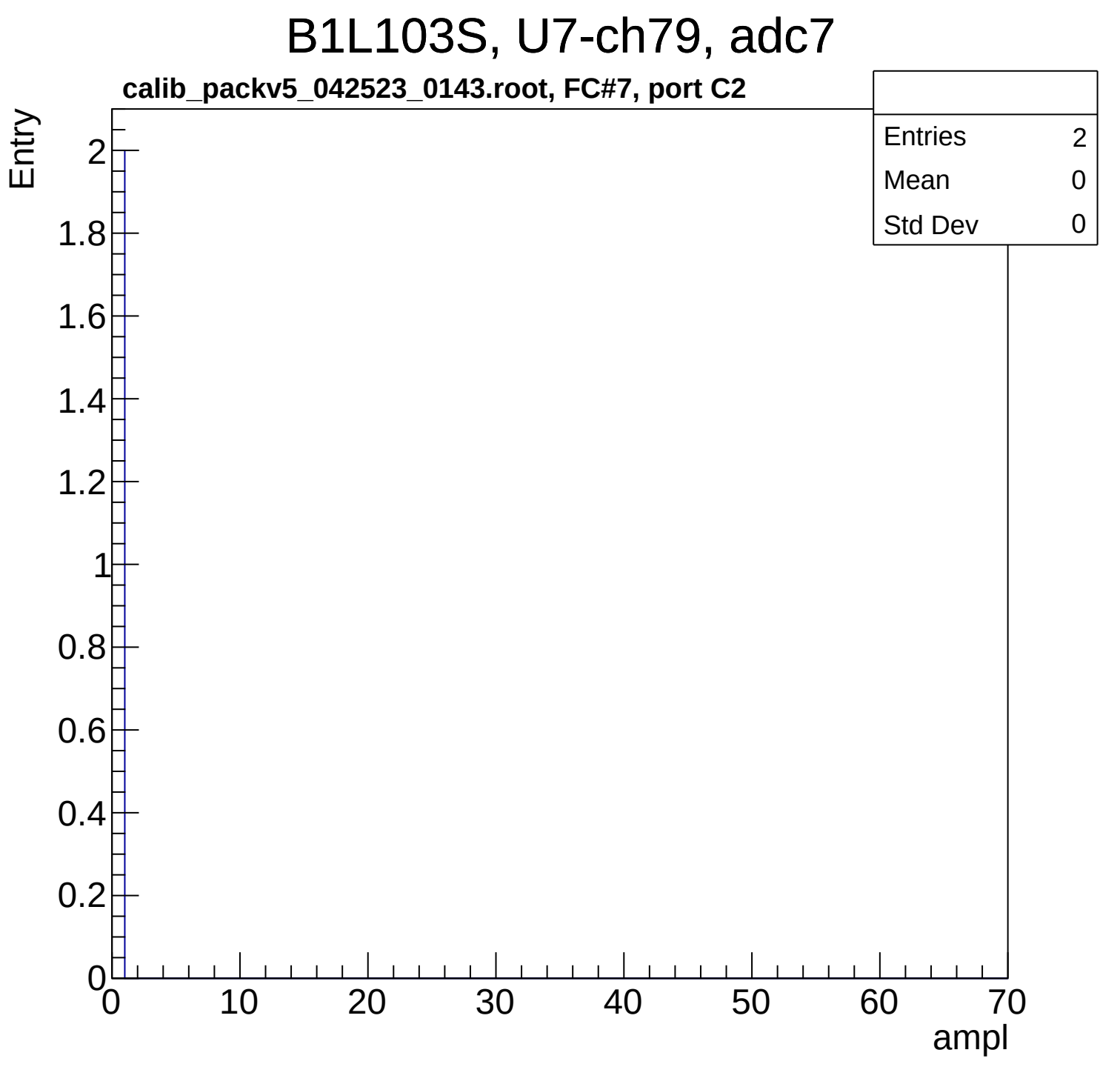
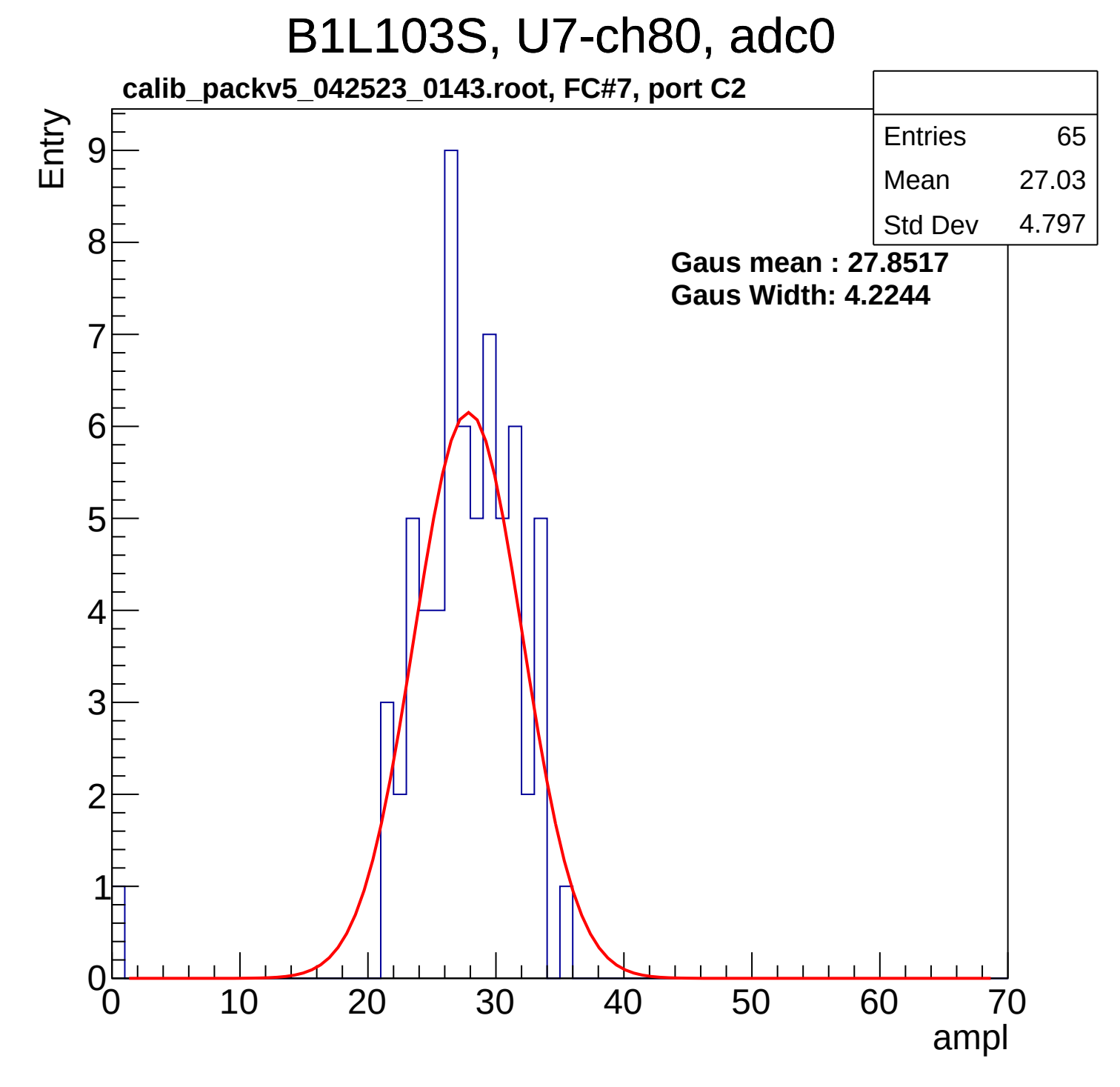

B1L103S, U7-ch79, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch80, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 27.03
Std Dev 4.797
Gaus mean : 27.8517
Gaus Width: 4.2244
Entry
ampl
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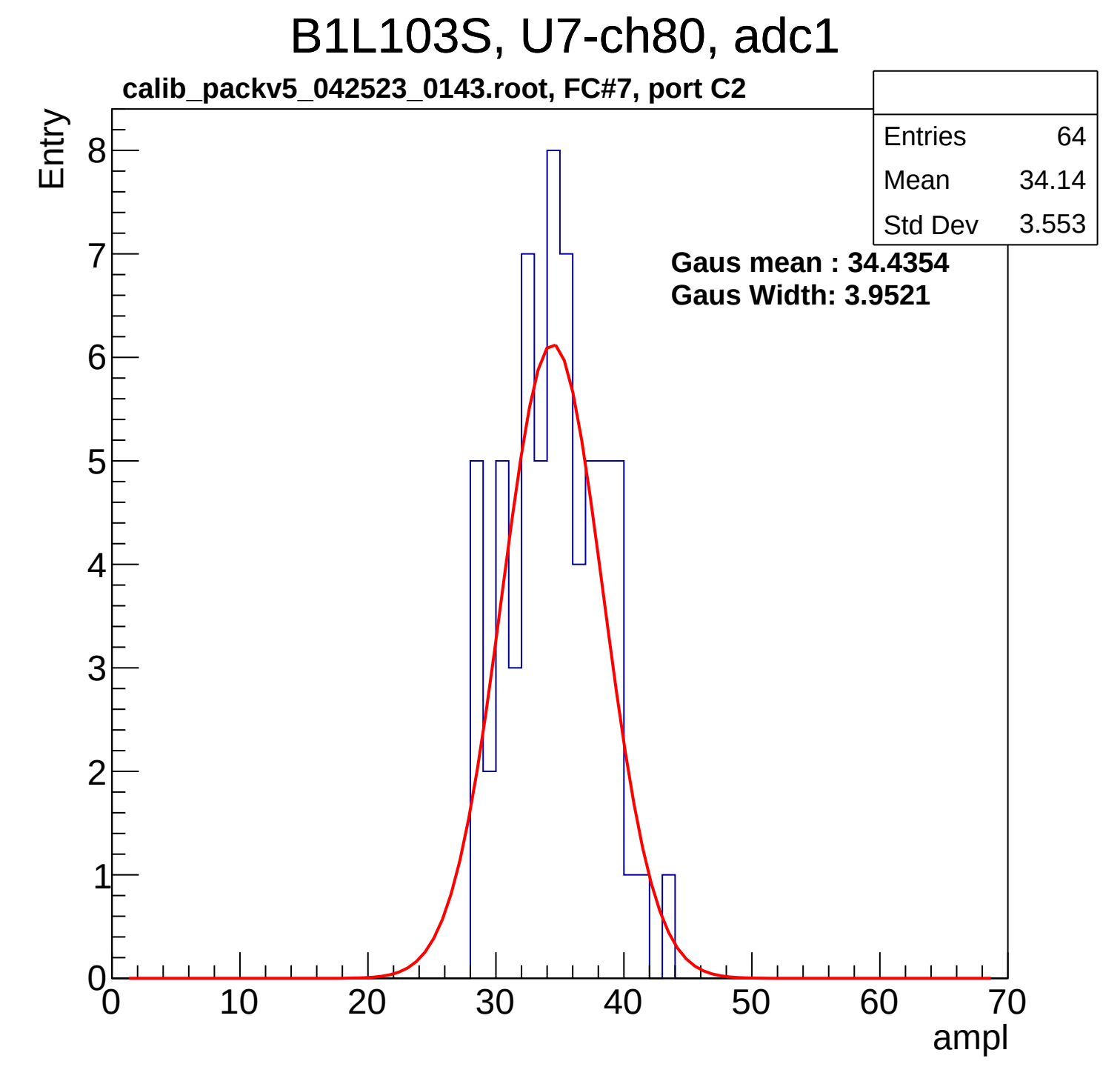
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch80, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 34.14
Std Dev 3.553
Gaus mean : 34.4354
Gaus Width: 3.9521
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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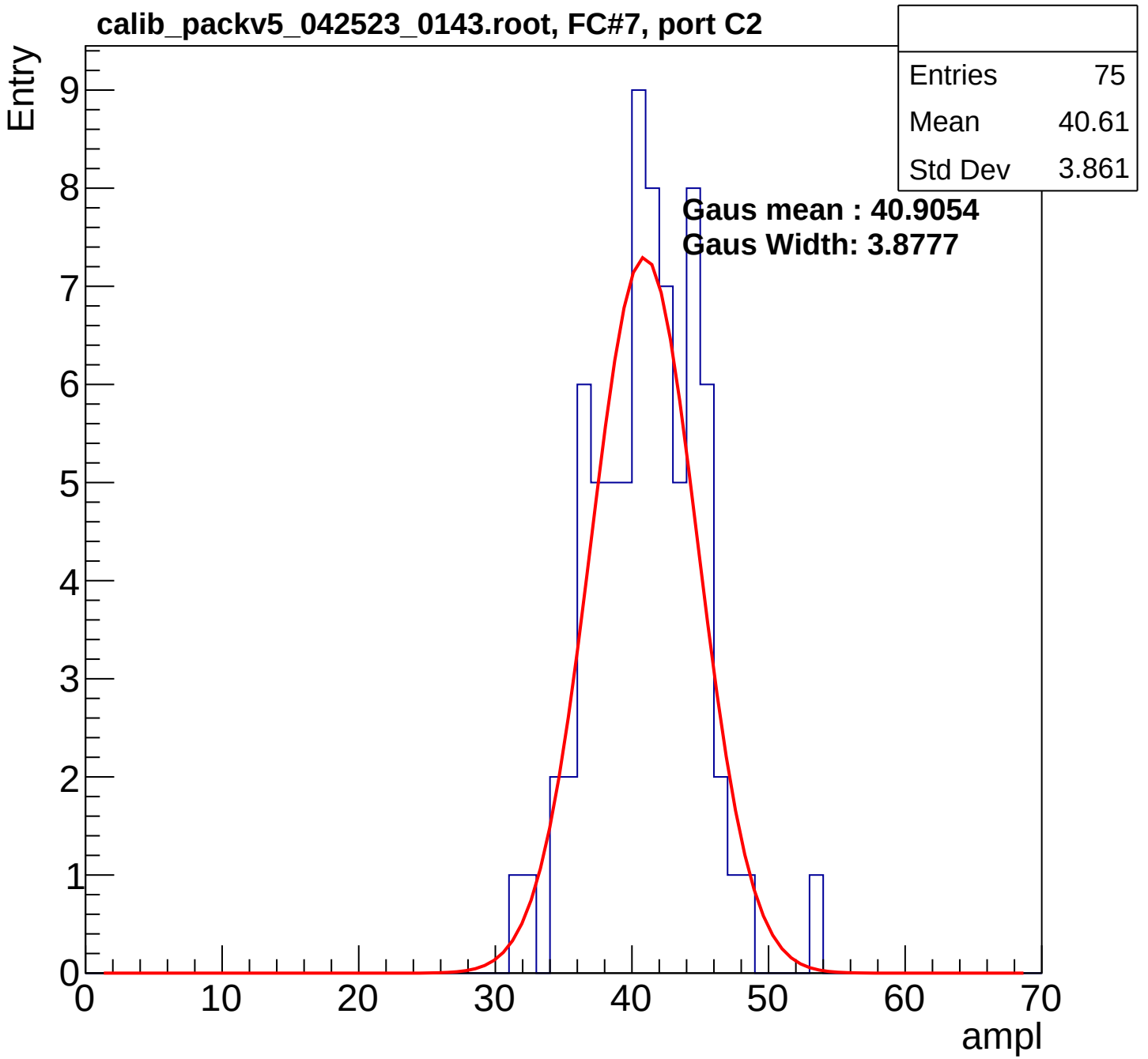
B1L103S, U7-ch80, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 75
Mean 40.61
Std Dev 3.861
Gaus mean : 40.9054
Gaus Width: 3.8777
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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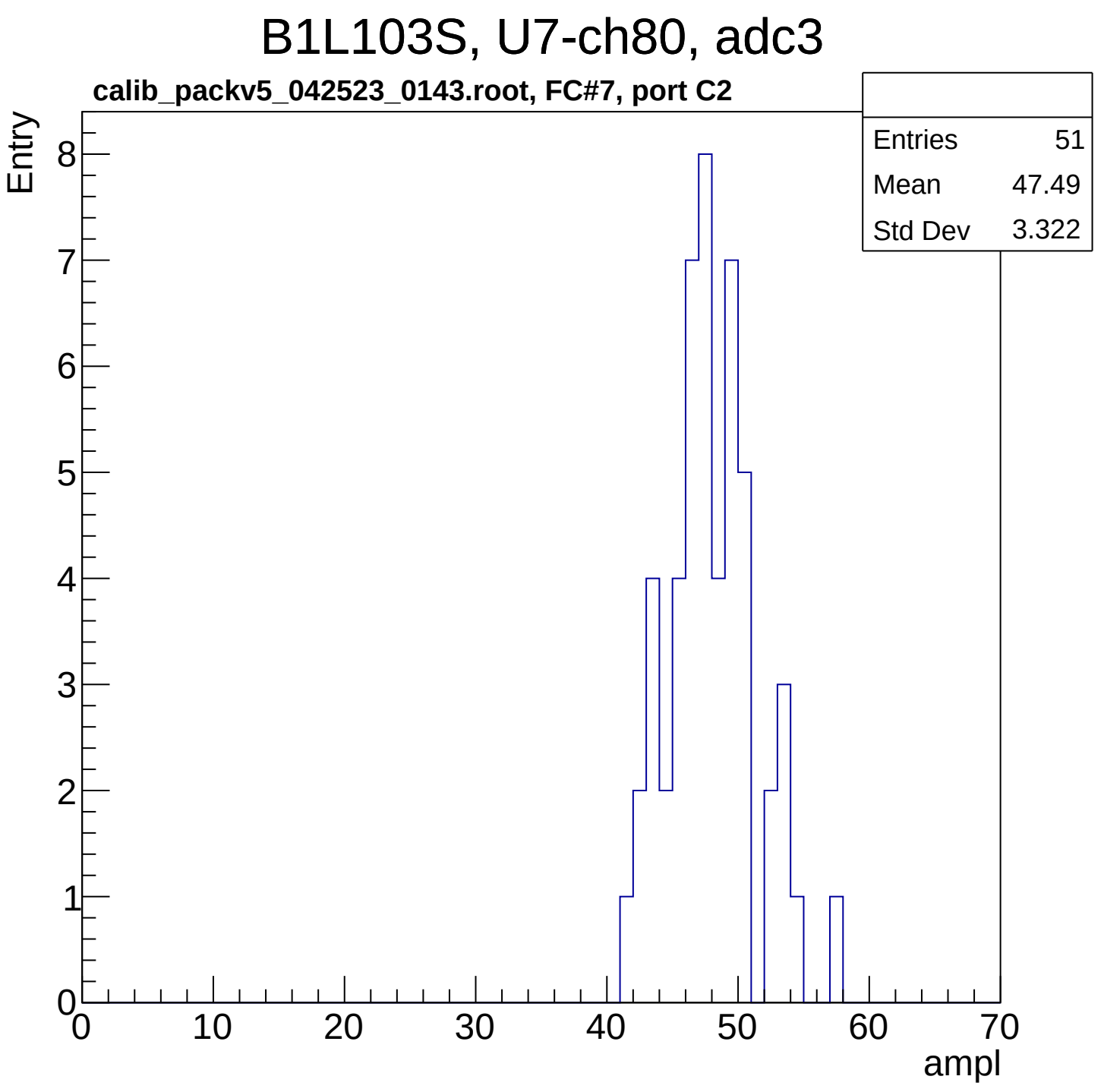
B1L103S, U7-ch80, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 51
Mean 47.49
Std Dev 3.322
Entry
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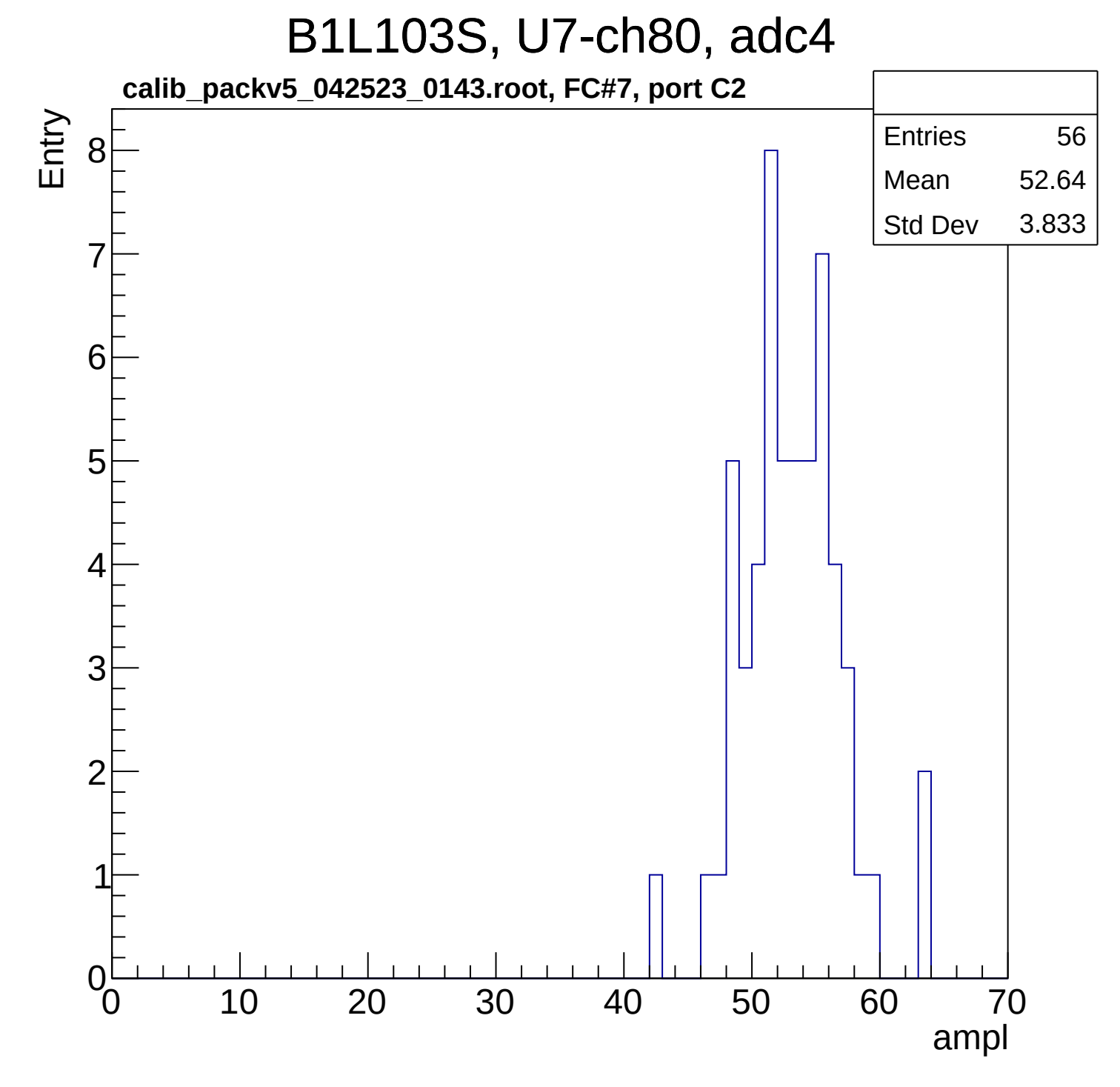
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch80, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 52.64
Std Dev 3.833
Entry
ampl
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1
2
3
4
5
6
7
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0
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20
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40
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60
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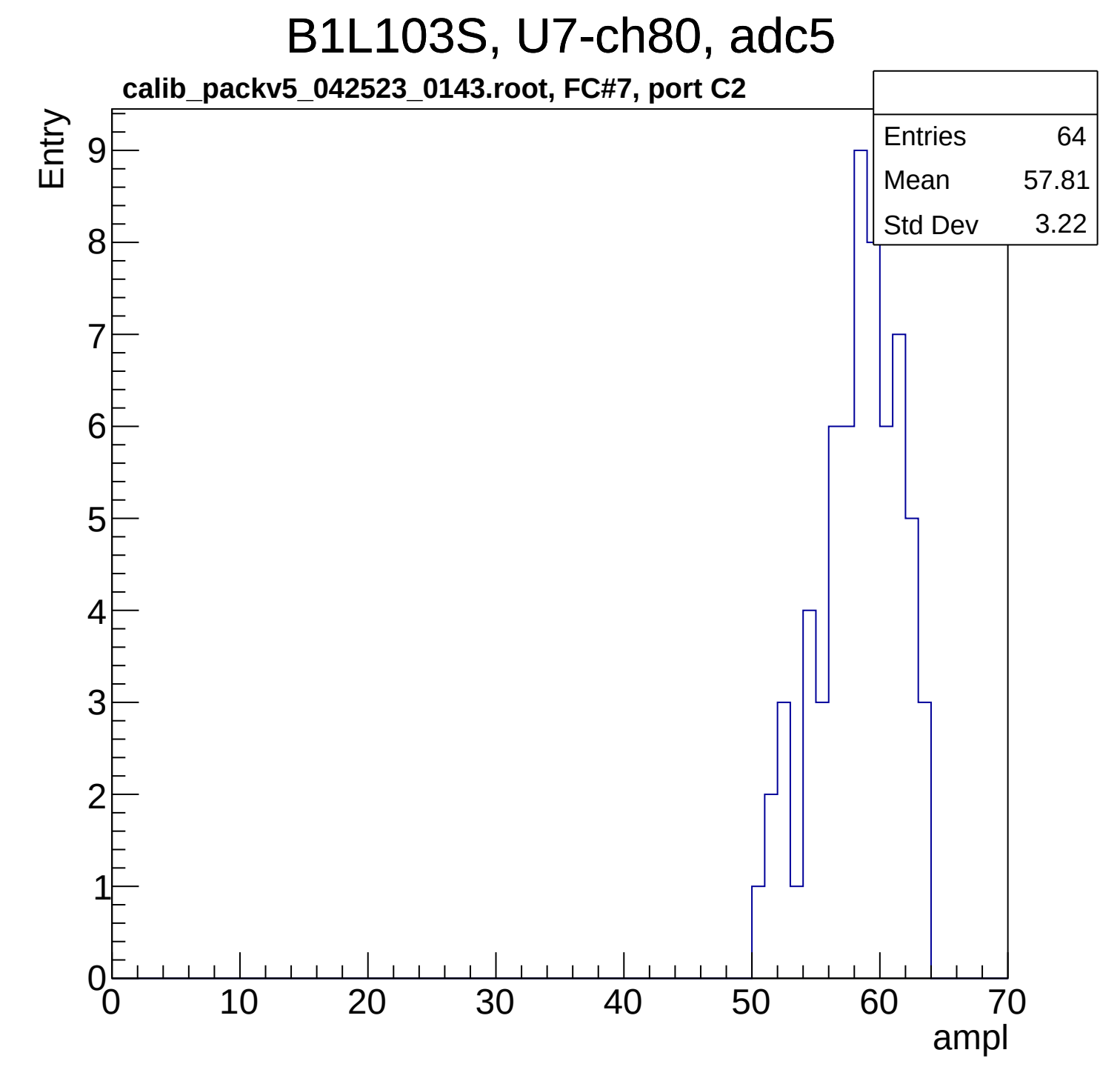
B1L103S, U7-ch80, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 57.81
Std Dev 3.22
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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60
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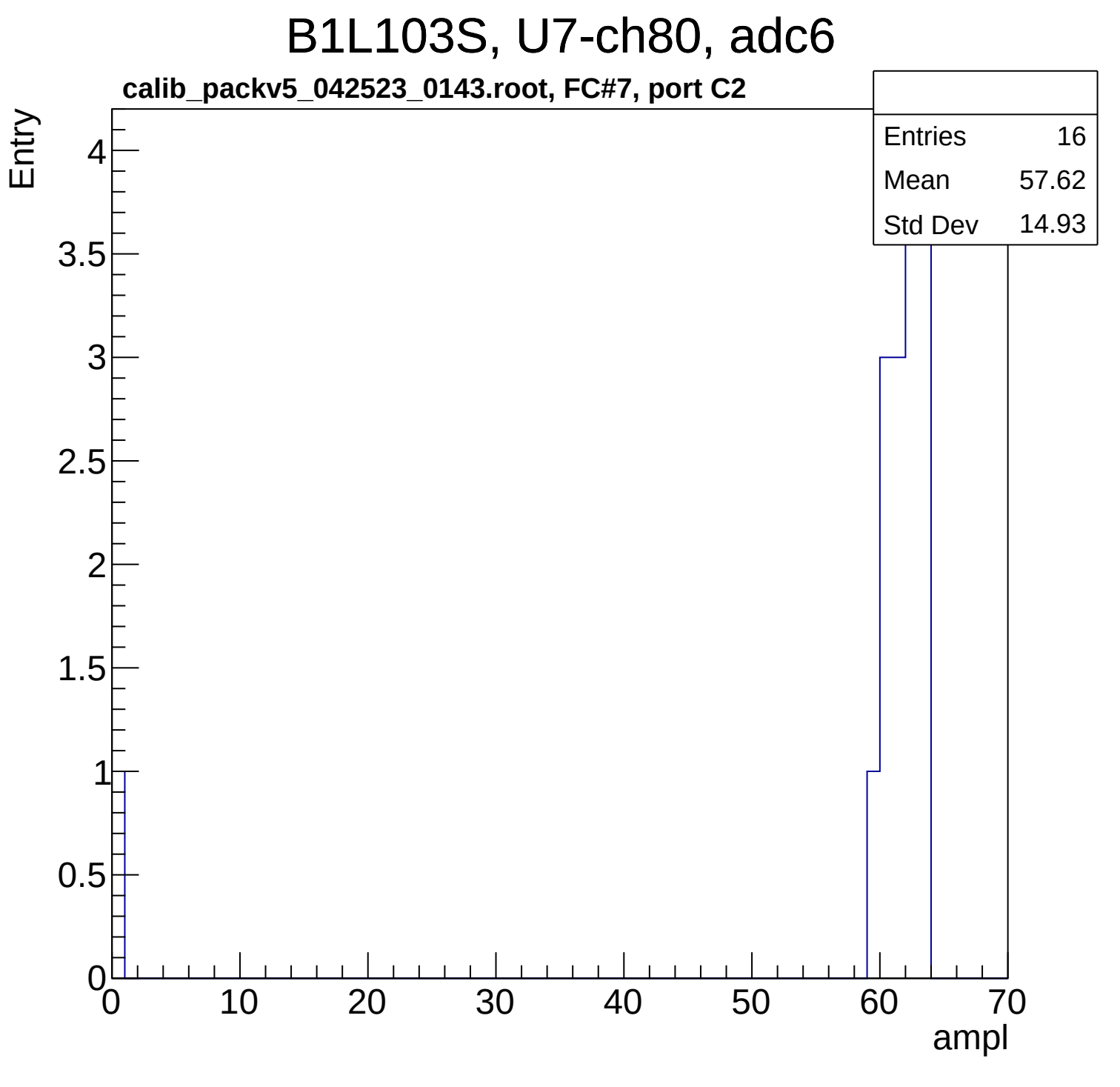
B1L103S, U7-ch80, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 16
Mean 57.62
Std Dev 14.93
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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40
50
60
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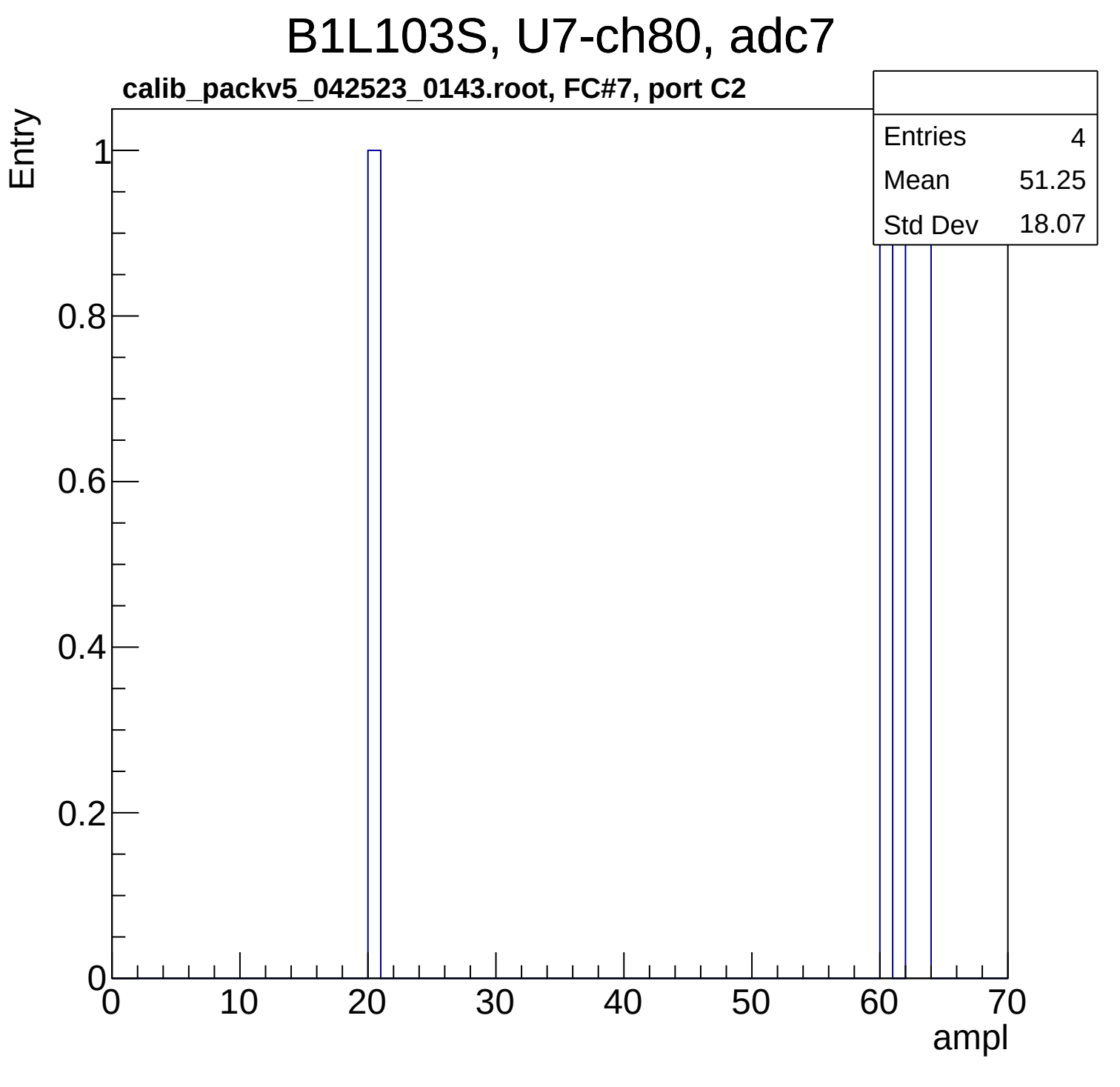
B1L103S, U7-ch80, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 4
Mean 51.25
Std Dev 18.07
Entry
ampl
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0.2
0.4
0.6
0.8
1
0
10
20
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40
50
60
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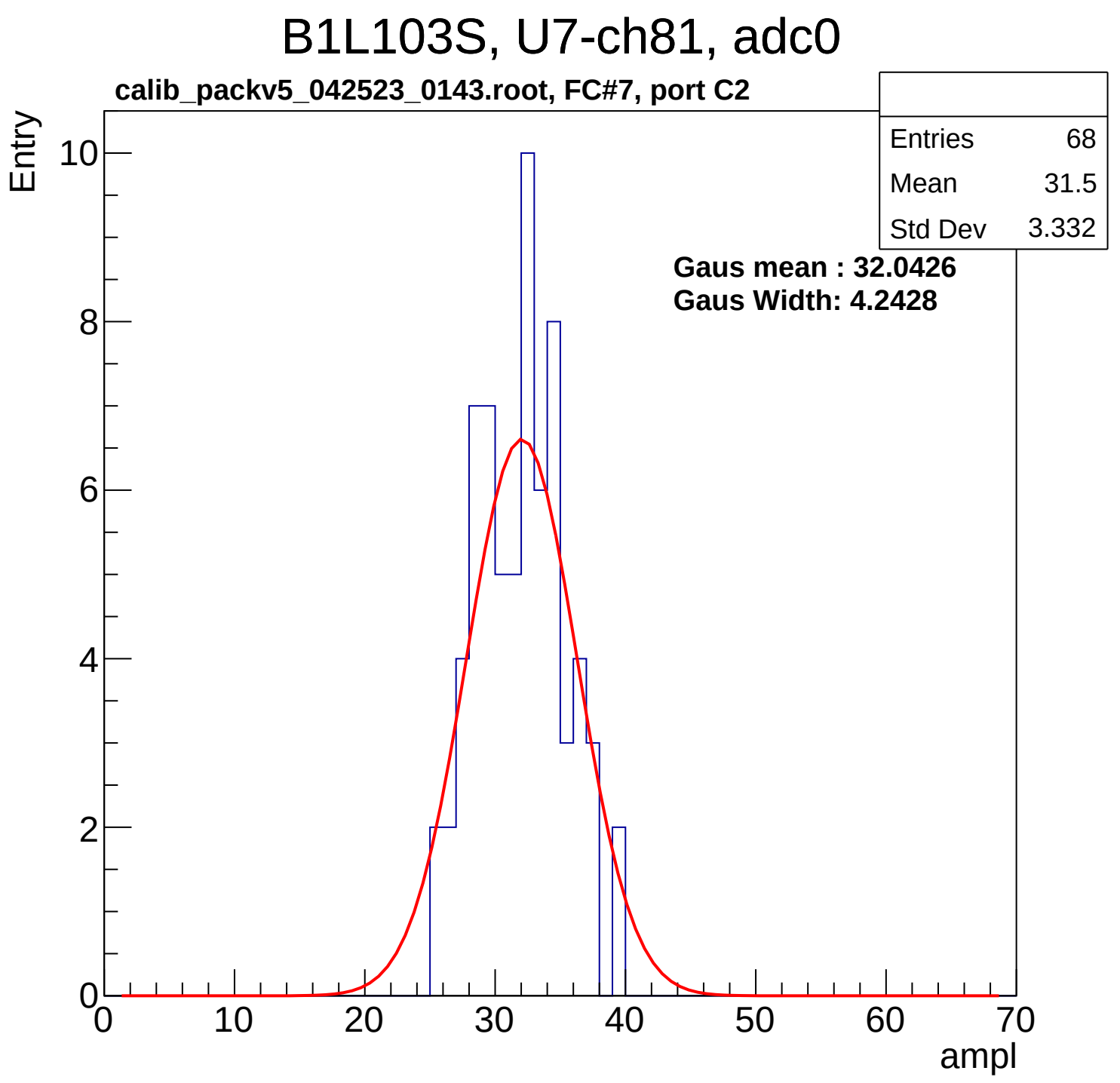
B1L103S, U7-ch81, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 31.5
Std Dev 3.332
Gaus mean : 32.0426
Gaus Width: 4.2428
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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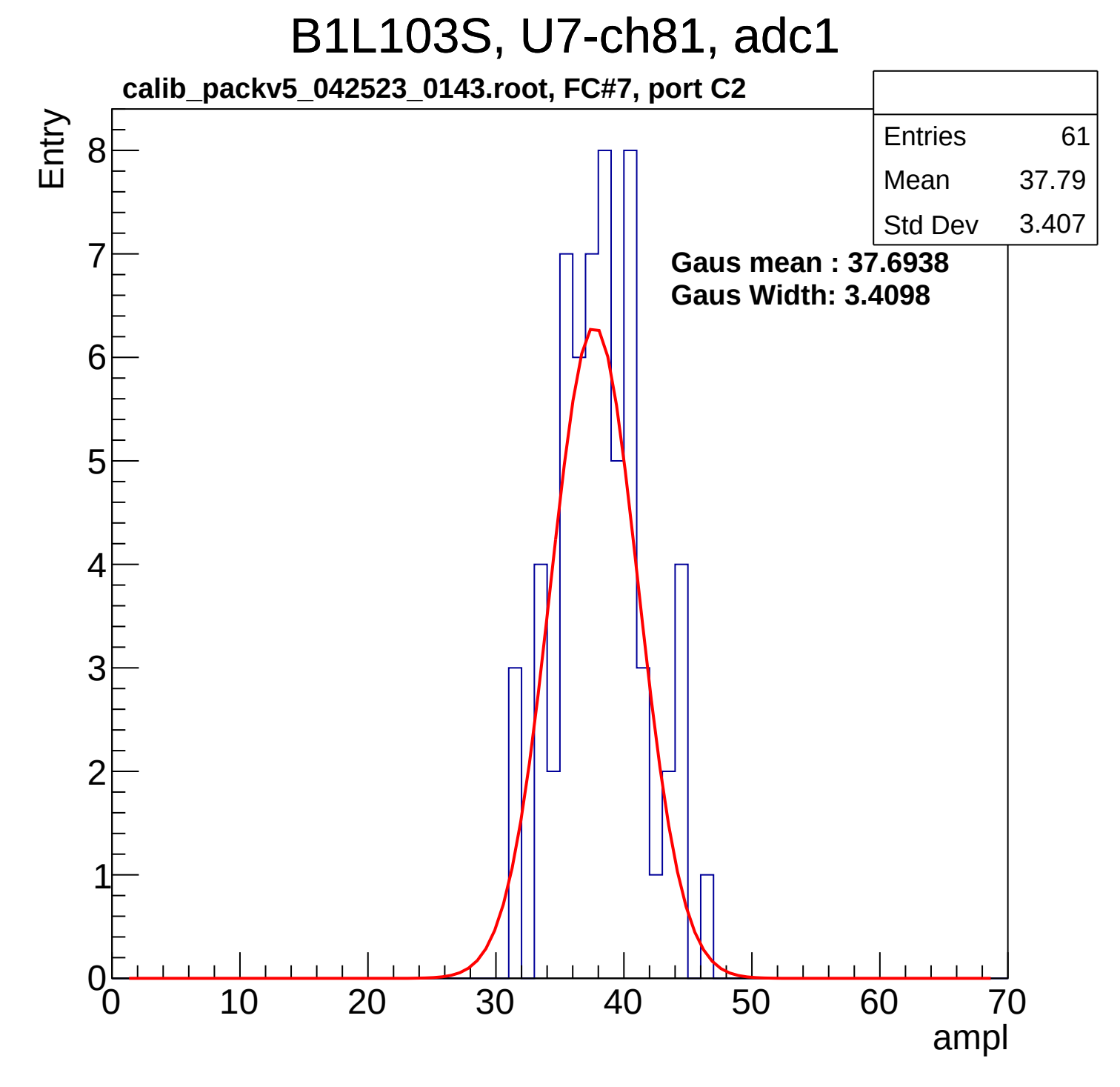
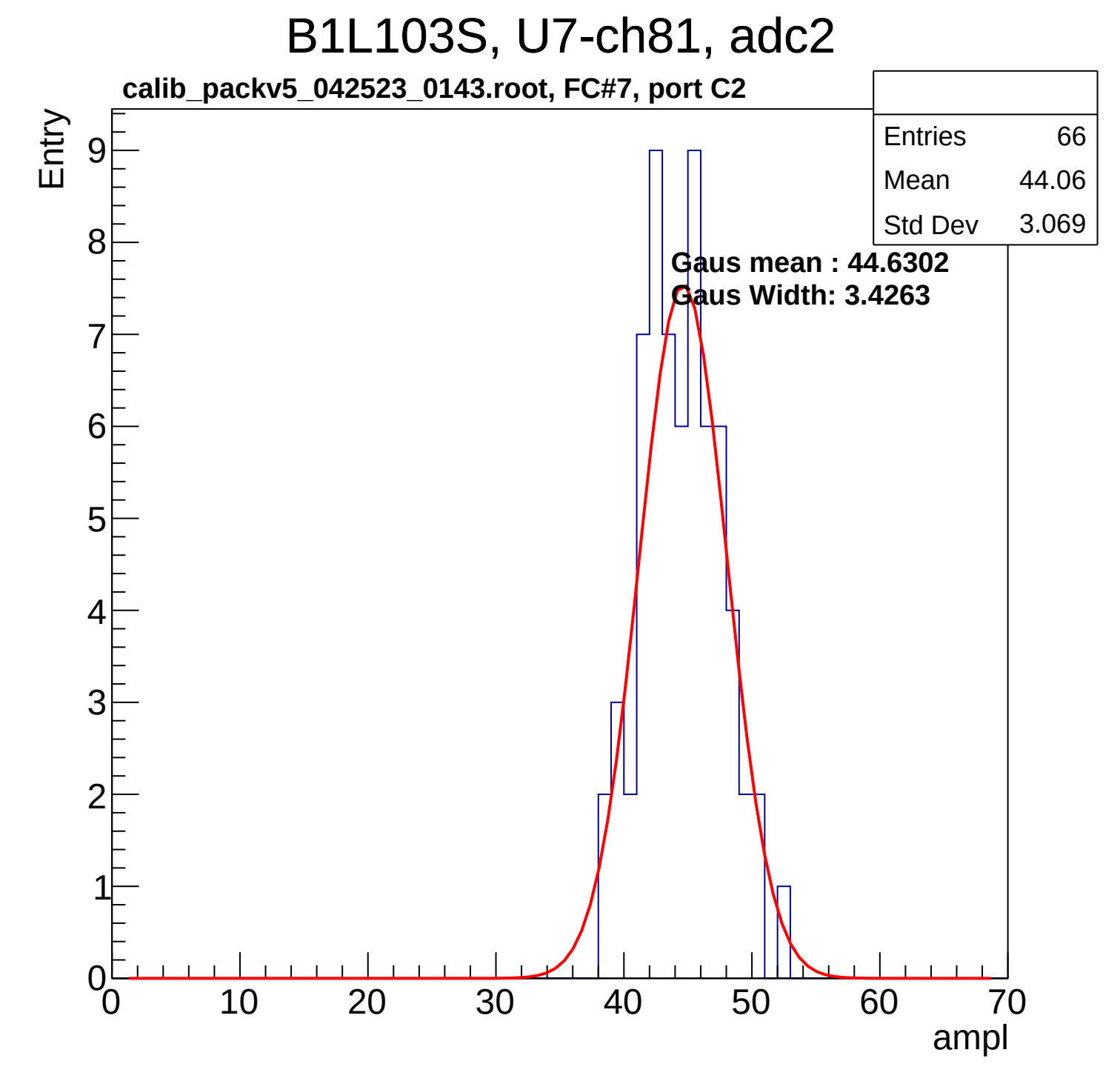

B1L103S, U7-ch81, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 61
Mean 37.79
Std Dev 3.407
Gaus mean : 37.6938
Gaus Width: 3.4098
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch81, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 44.06
Std Dev 3.069
Gaus mean : 44.6302
Gaus Width: 3.4263
Entry
ampl
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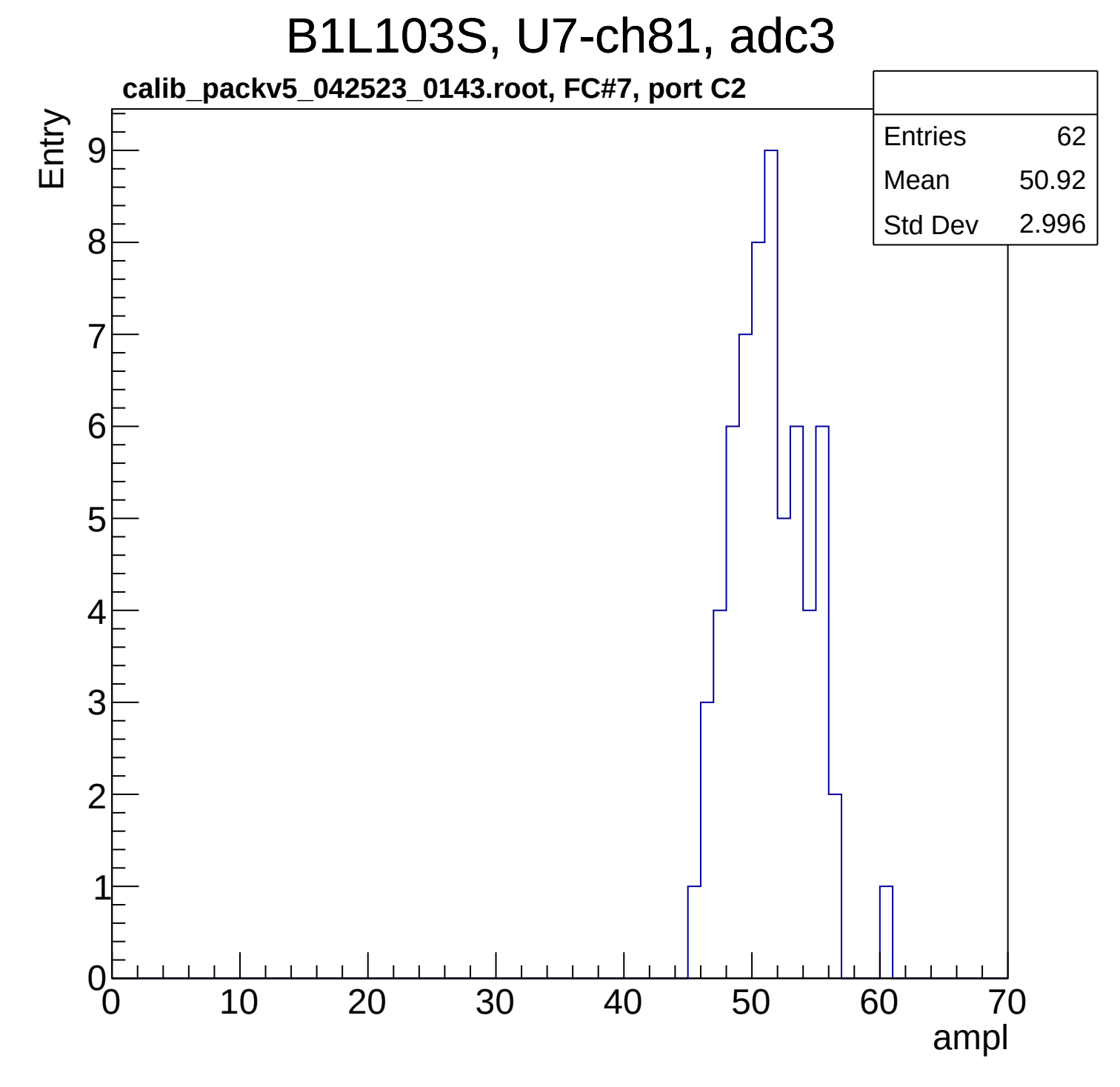
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch81, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 62
Mean 50.92
Std Dev 2.996
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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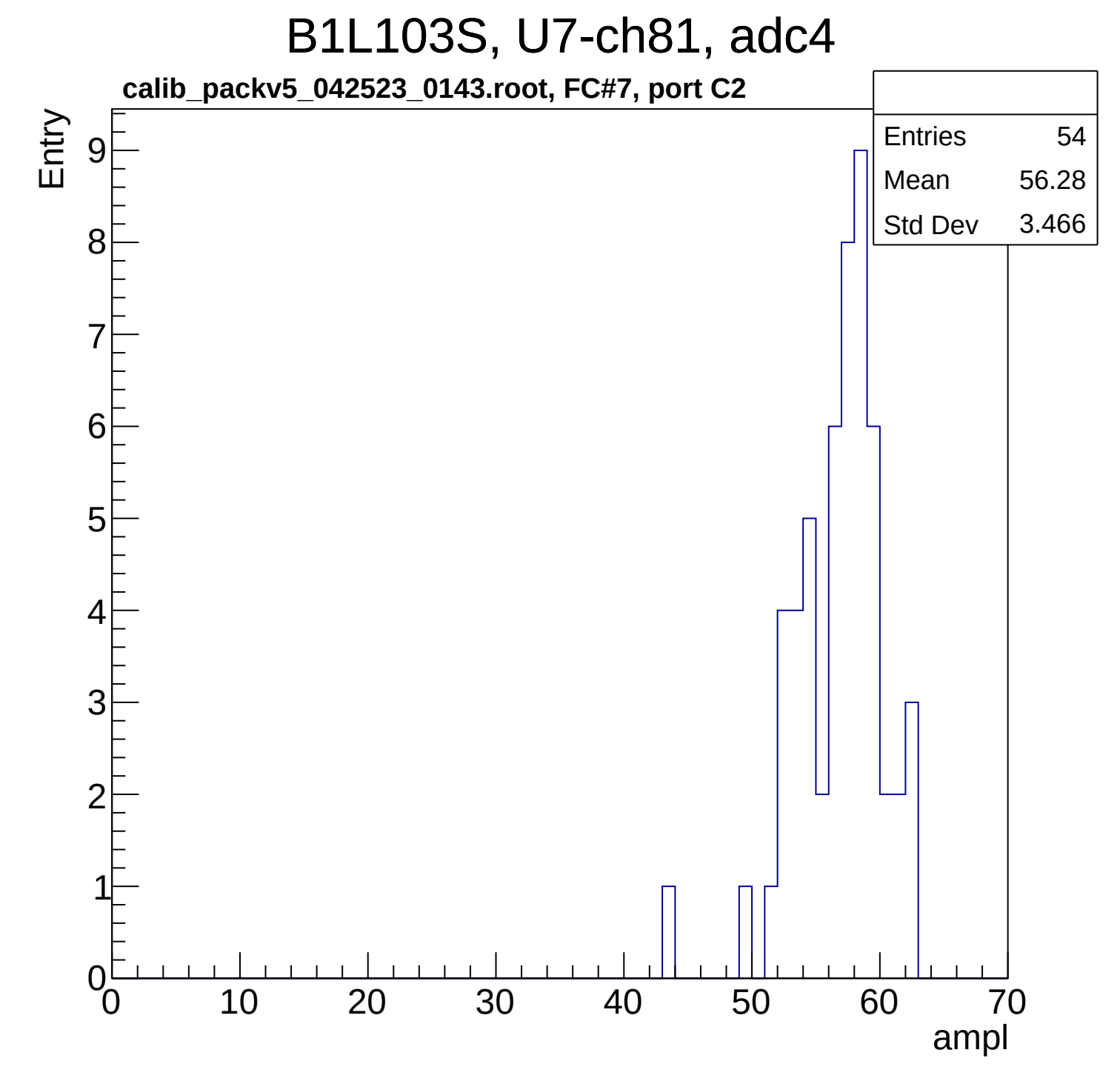
B1L103S, U7-ch81, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 54
Mean 56.28
Std Dev 3.466
Entry
ampl
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2
3
4
5
6
7
8
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0
10
20
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40
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60
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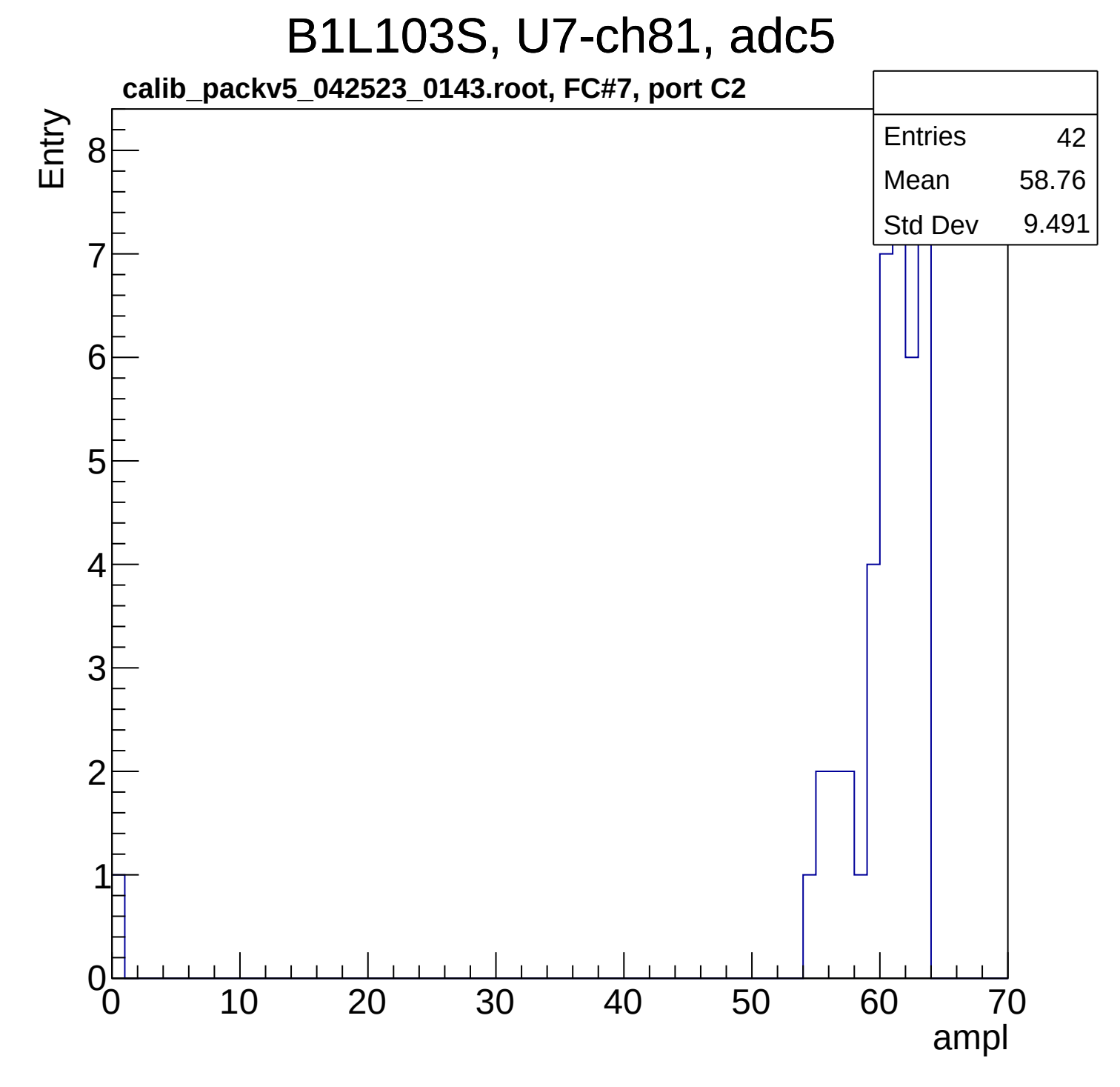
B1L103S, U7-ch81, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 42
Mean 58.76
Std Dev 9.491
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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60
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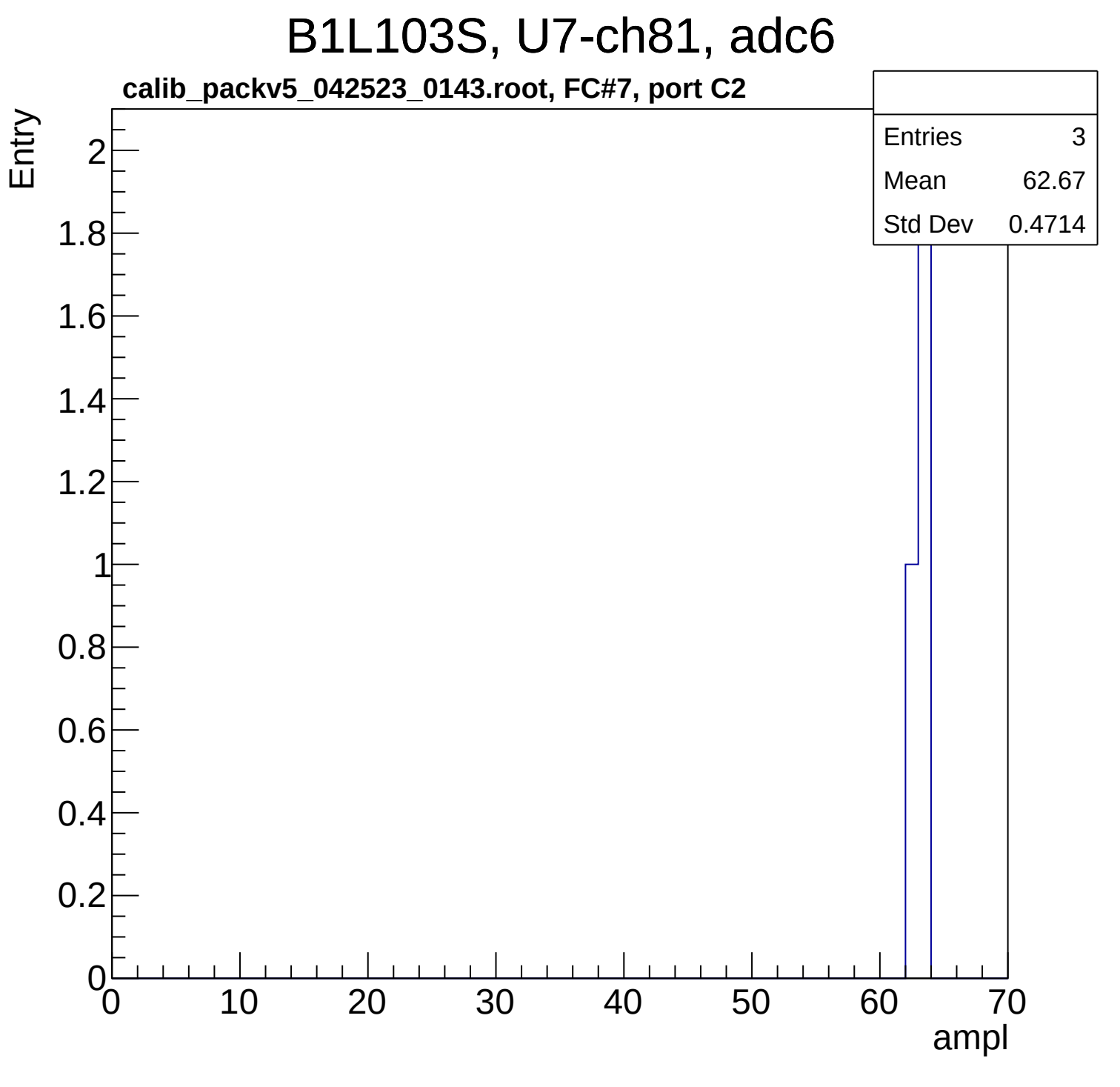
B1L103S, U7-ch81, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 62.67
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
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40
50
60
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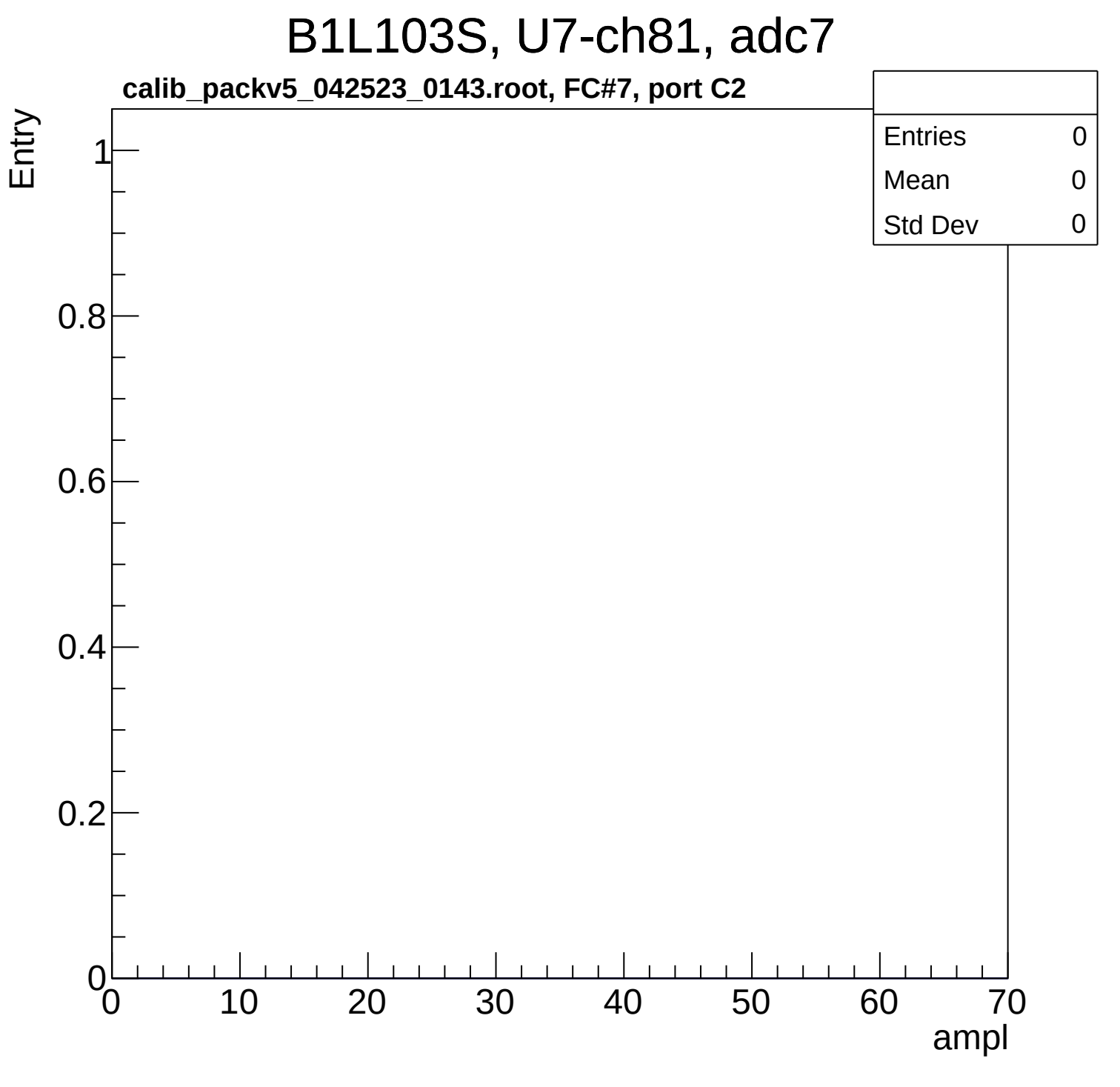
B1L103S, U7-ch81, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
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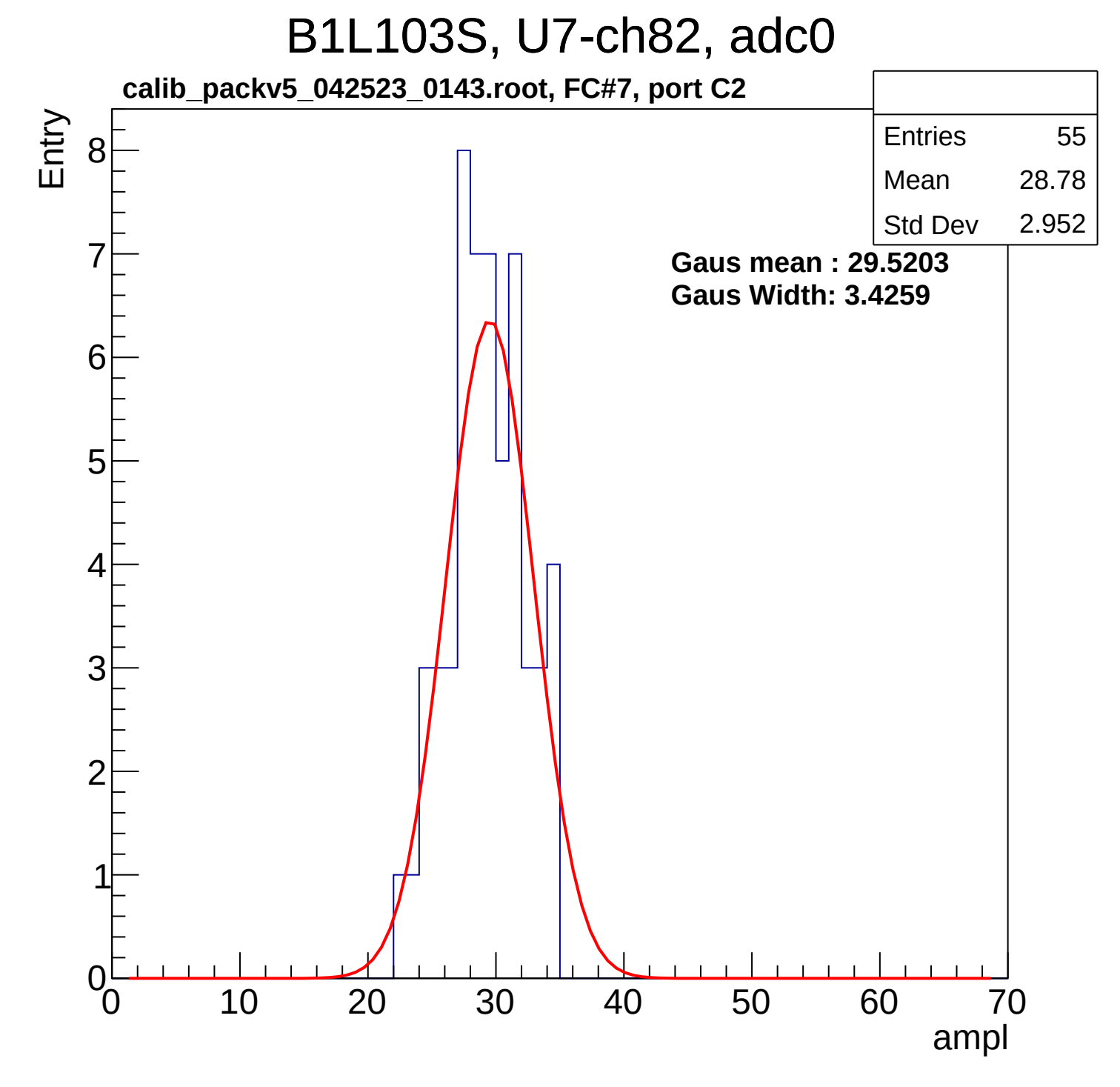
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch82, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 28.78
Std Dev 2.952
Gaus mean : 29.5203
Gaus Width: 3.4259
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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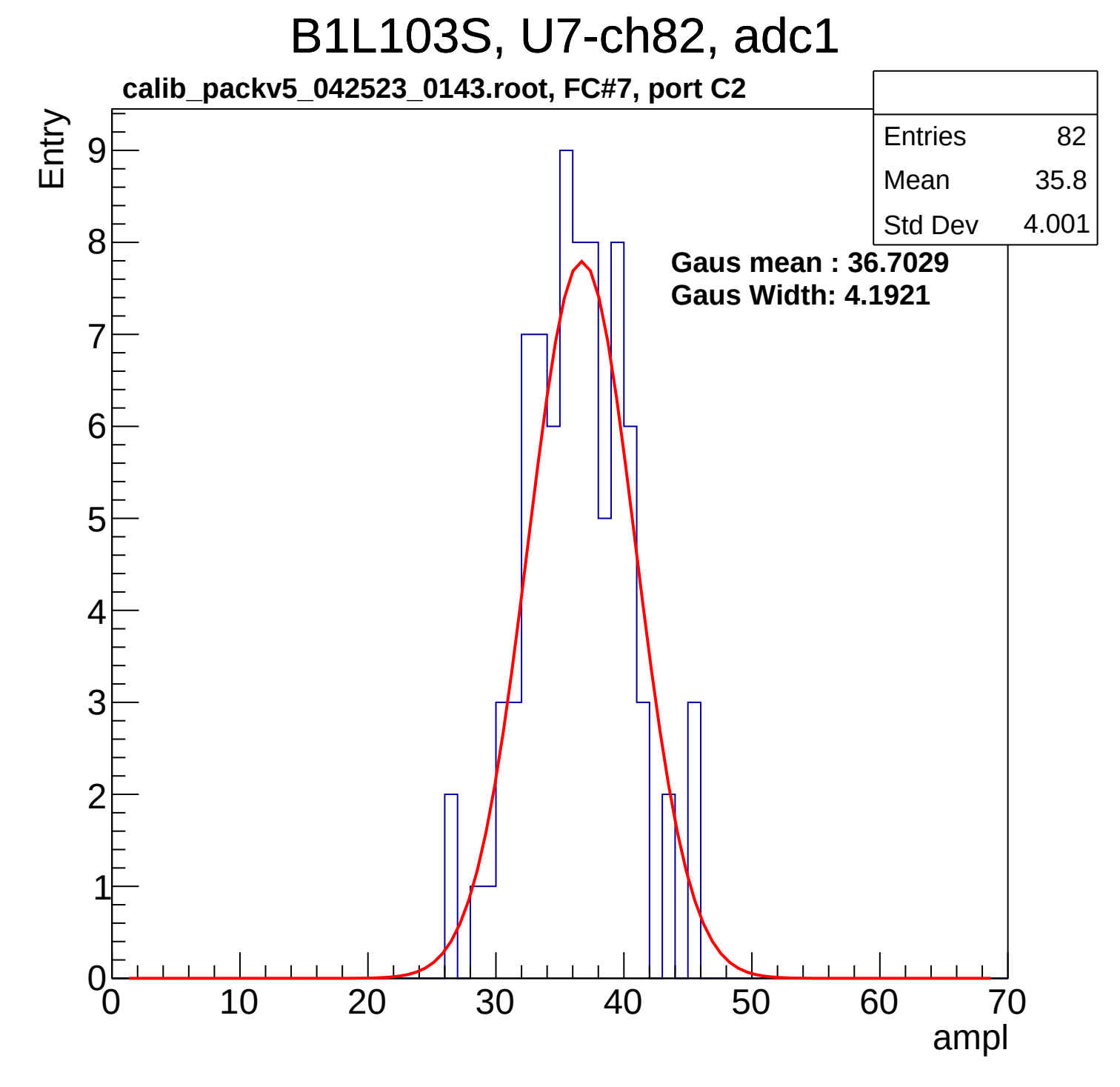
B1L103S, U7-ch82, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 82
Mean 35.8
Std Dev 4.001
Gaus mean : 36.7029
Gaus Width: 4.1921
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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60
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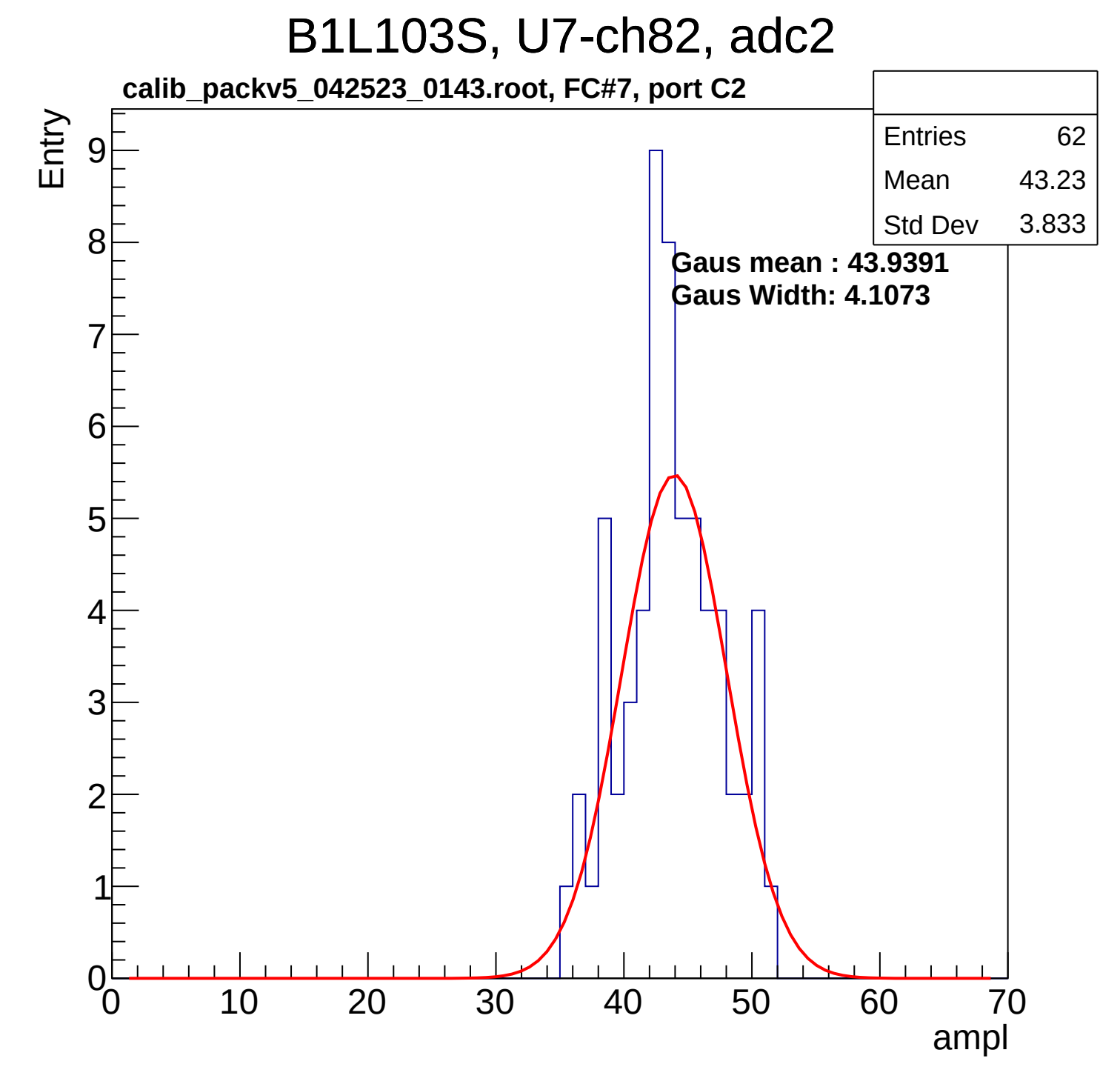
B1L103S, U7-ch82, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 62
Mean 43.23
Std Dev 3.833
Gaus mean : 43.9391
Gaus Width: 4.1073
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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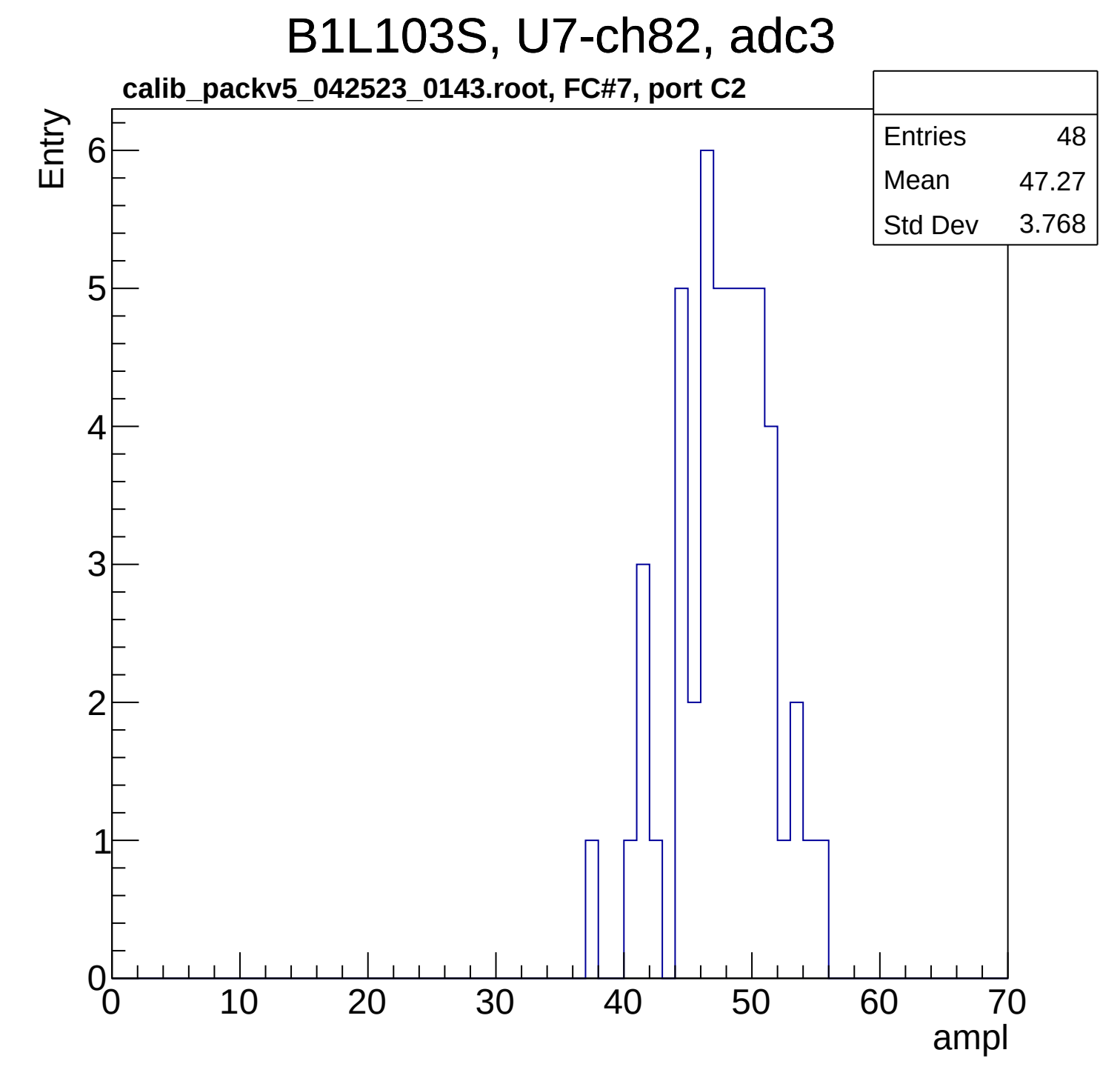
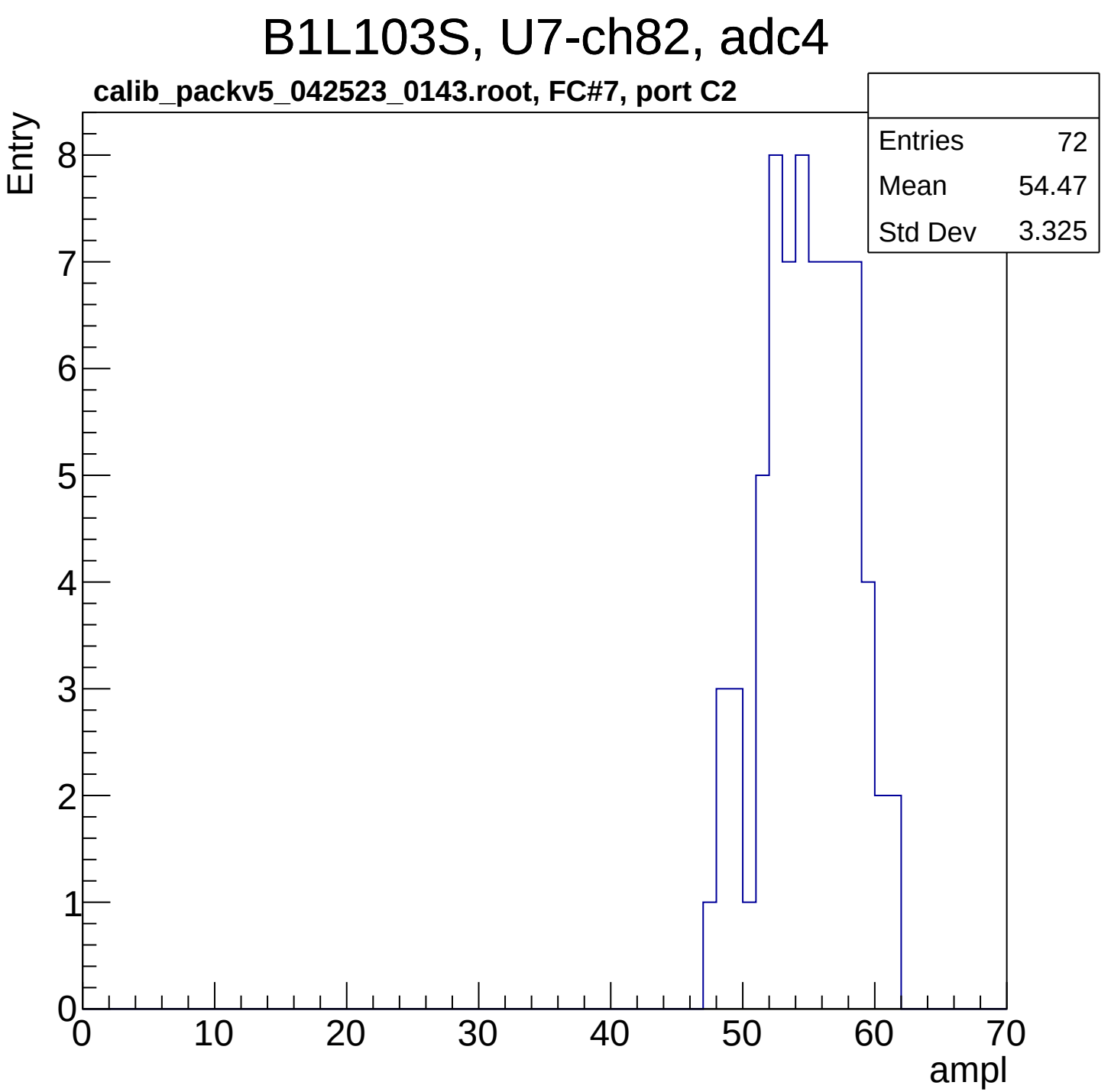

B1L103S, U7-ch82, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 48
Mean 47.27
Std Dev 3.768
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch82, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 72
Mean 54.47
Std Dev 3.325
Entry
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2
3
4
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8
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10
20
30
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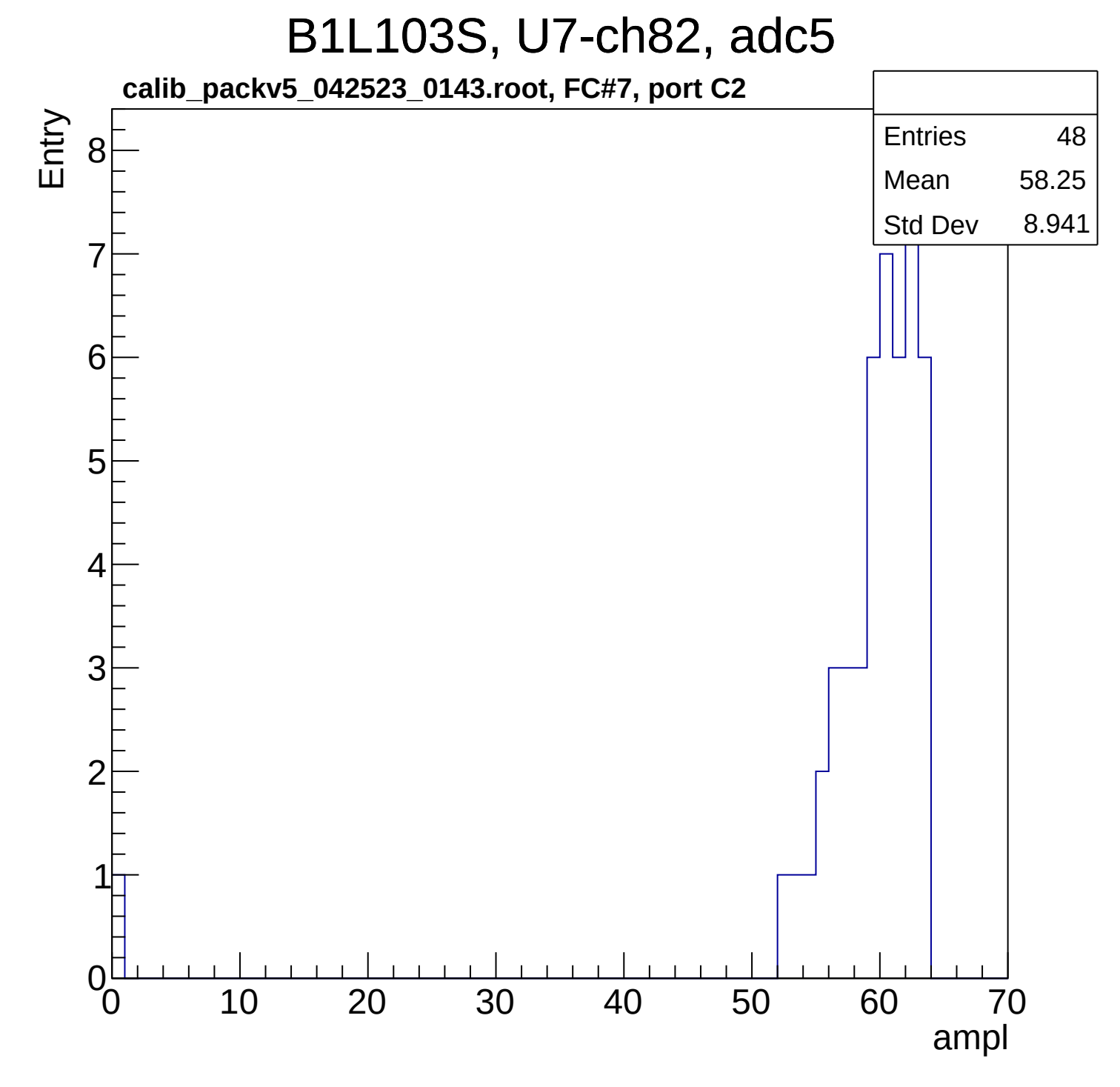
50
60
70
ampl


B1L103S, U7-ch82, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 48
Mean 58.25
Std Dev 8.941
Entry
ampl
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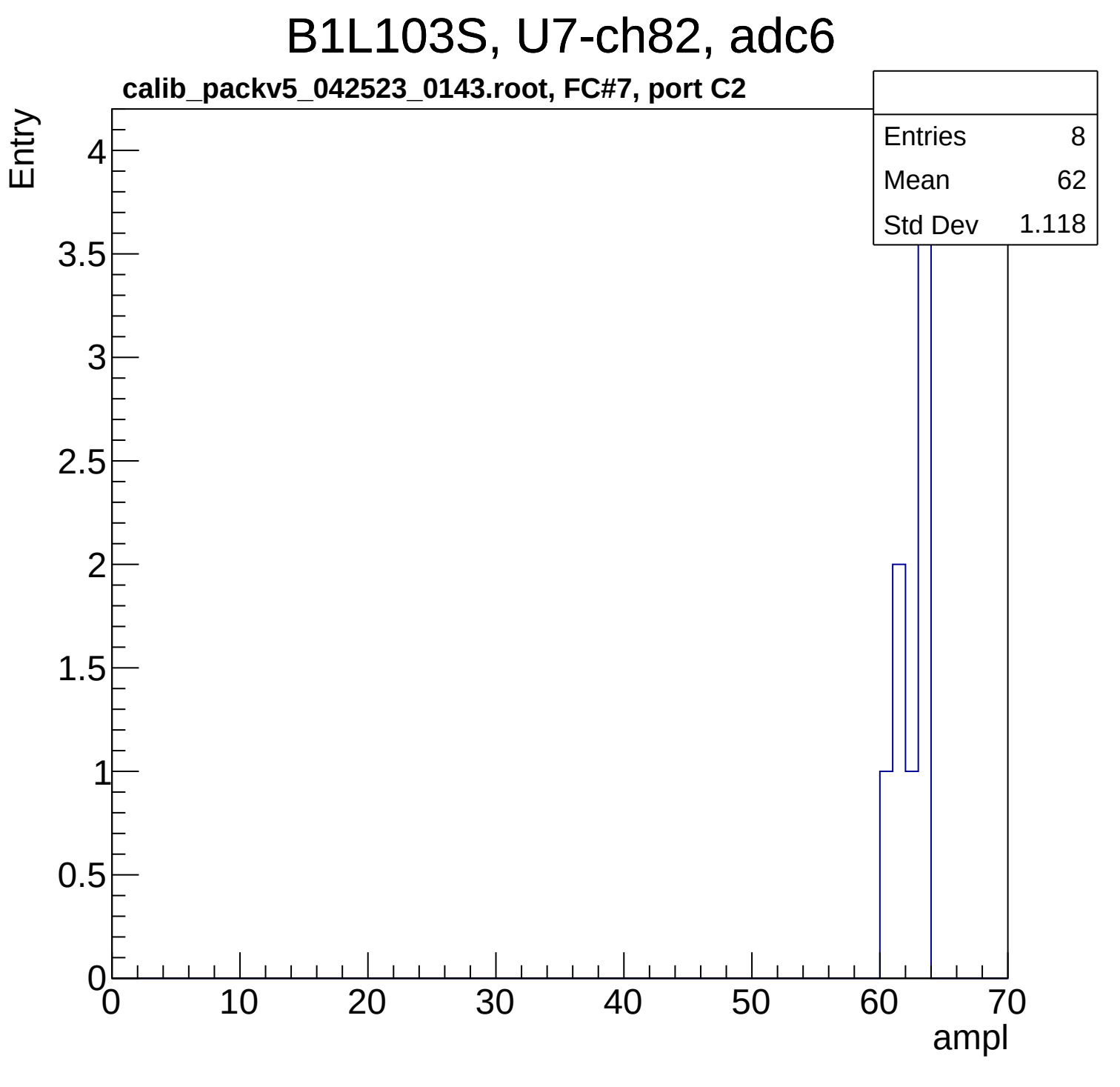
B1L103S, U7-ch82, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 8
Mean 62
Std Dev 1.118
Entry
ampl
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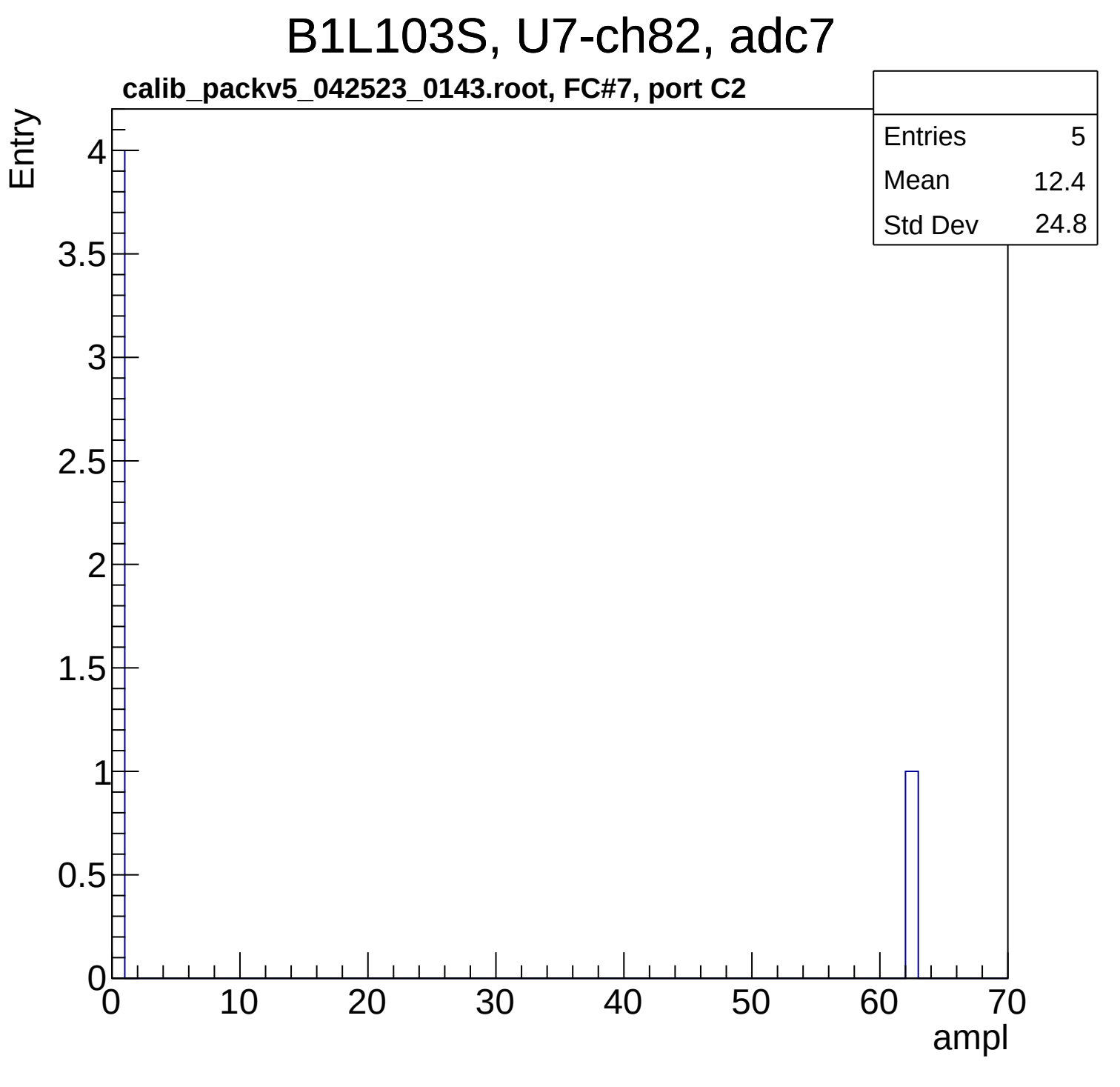
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U7-ch82, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 5
Mean 12.4
Std Dev 24.8
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
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40
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60
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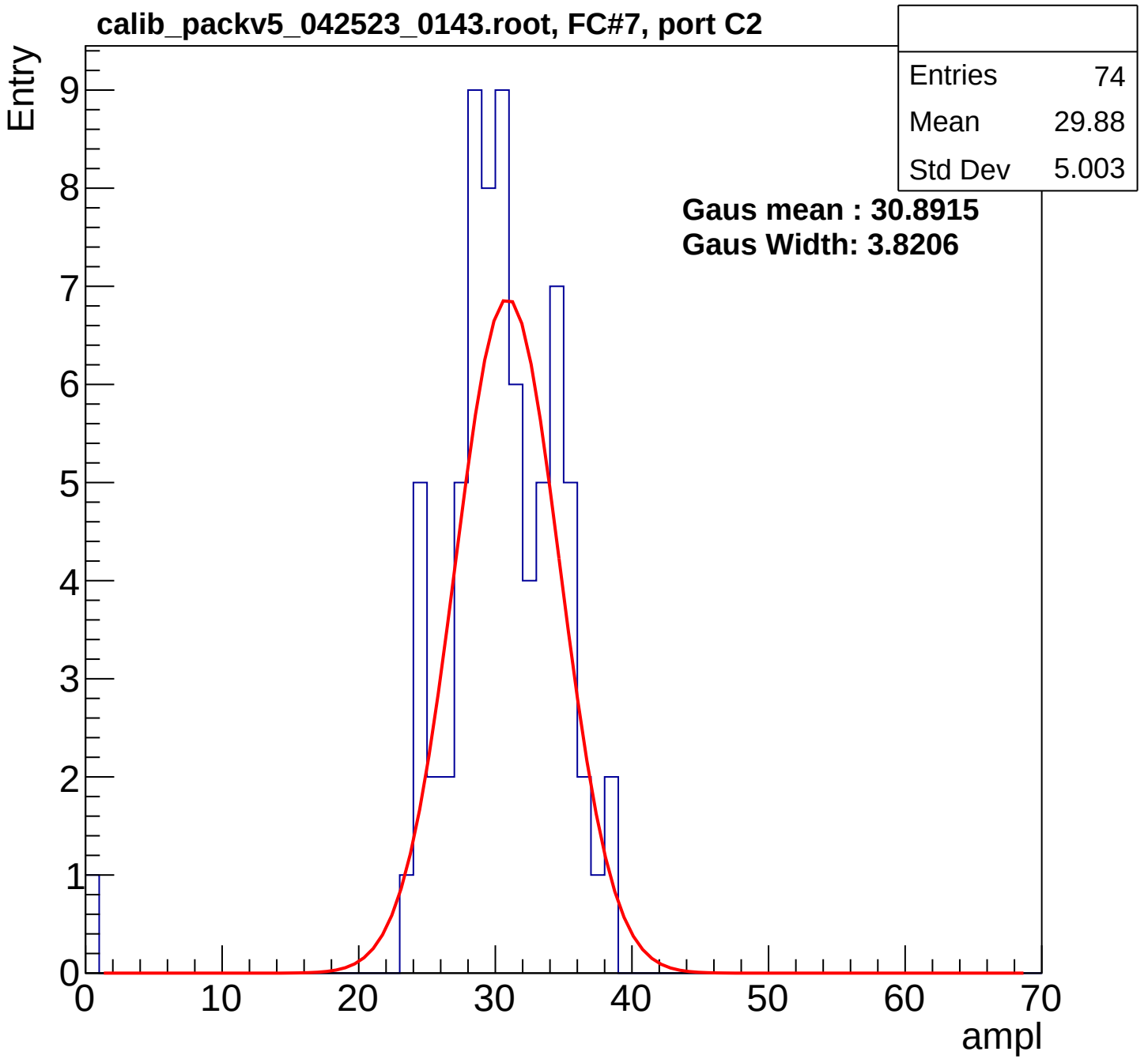
B1L103S, U7-ch83, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 74
Mean 29.88
Std Dev 5.003
Gaus mean : 30.8915
Gaus Width: 3.8206
Entry
ampl
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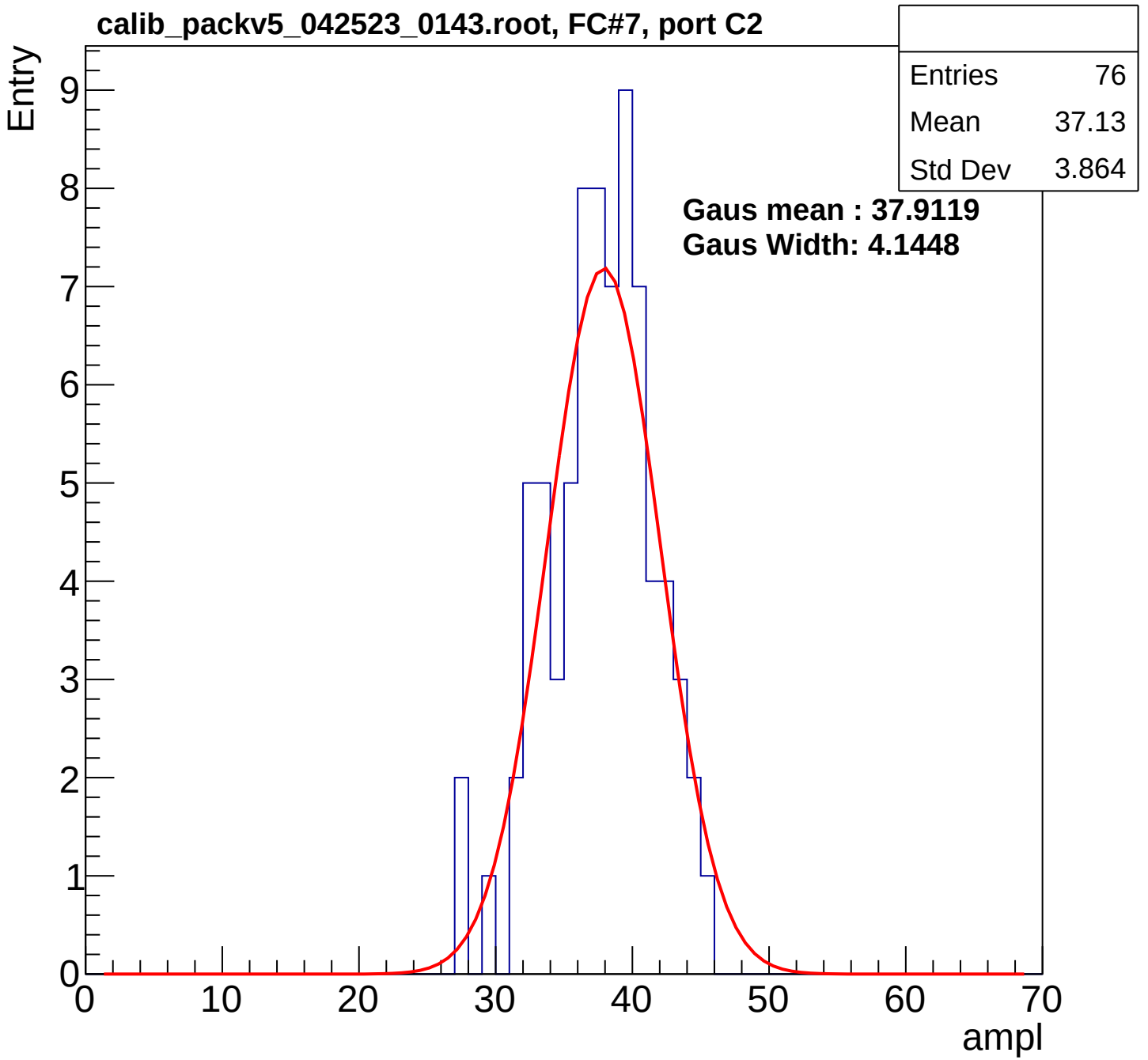
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L103S, U7-ch83, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 76
Mean 37.13
Std Dev 3.864
Gaus mean : 37.9119
Gaus Width: 4.1448
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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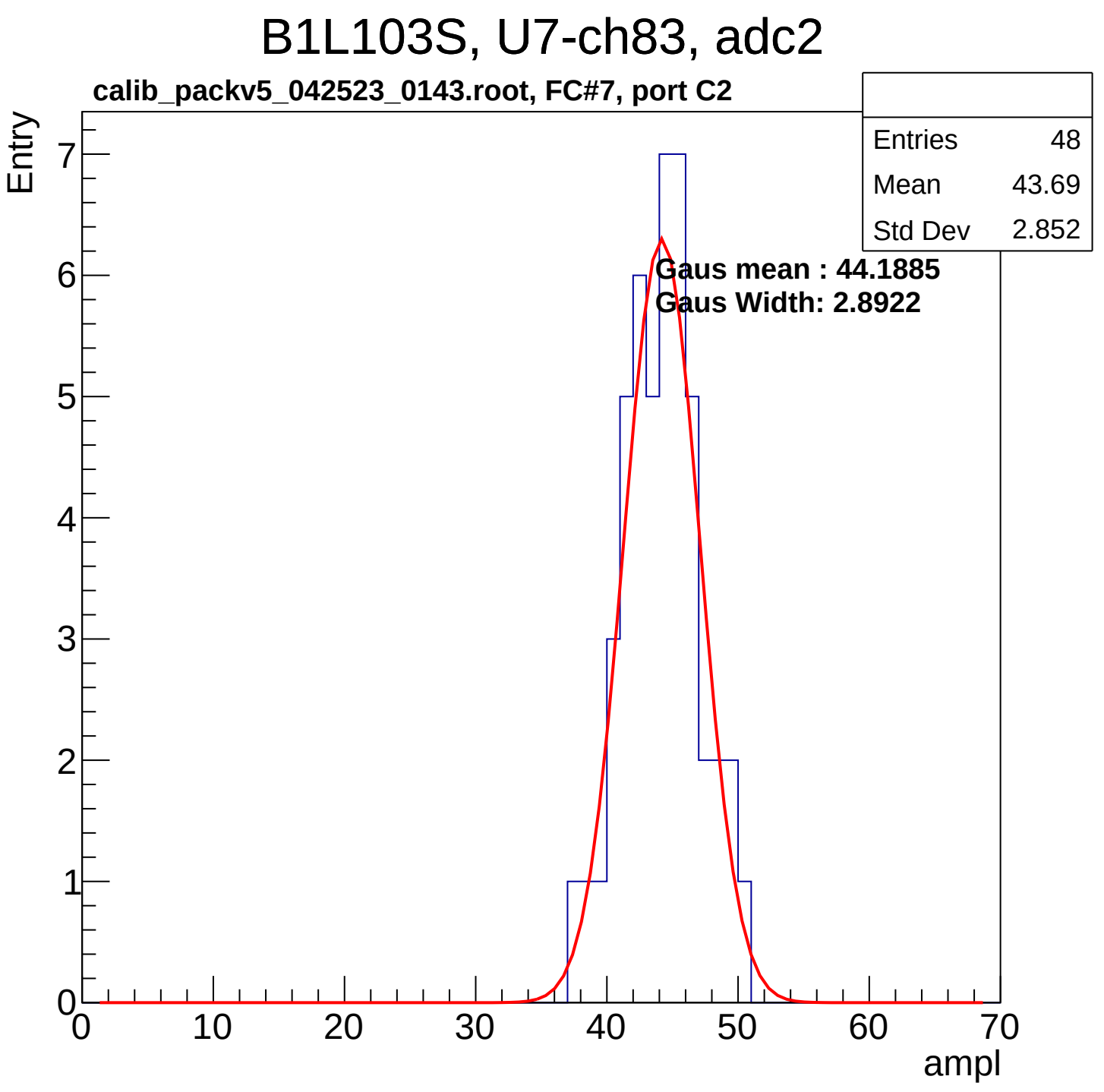
B1L103S, U7-ch83, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 48
Mean 43.69
Std Dev 2.852
Gaus mean : 44.1885
Gaus Width: 2.8922
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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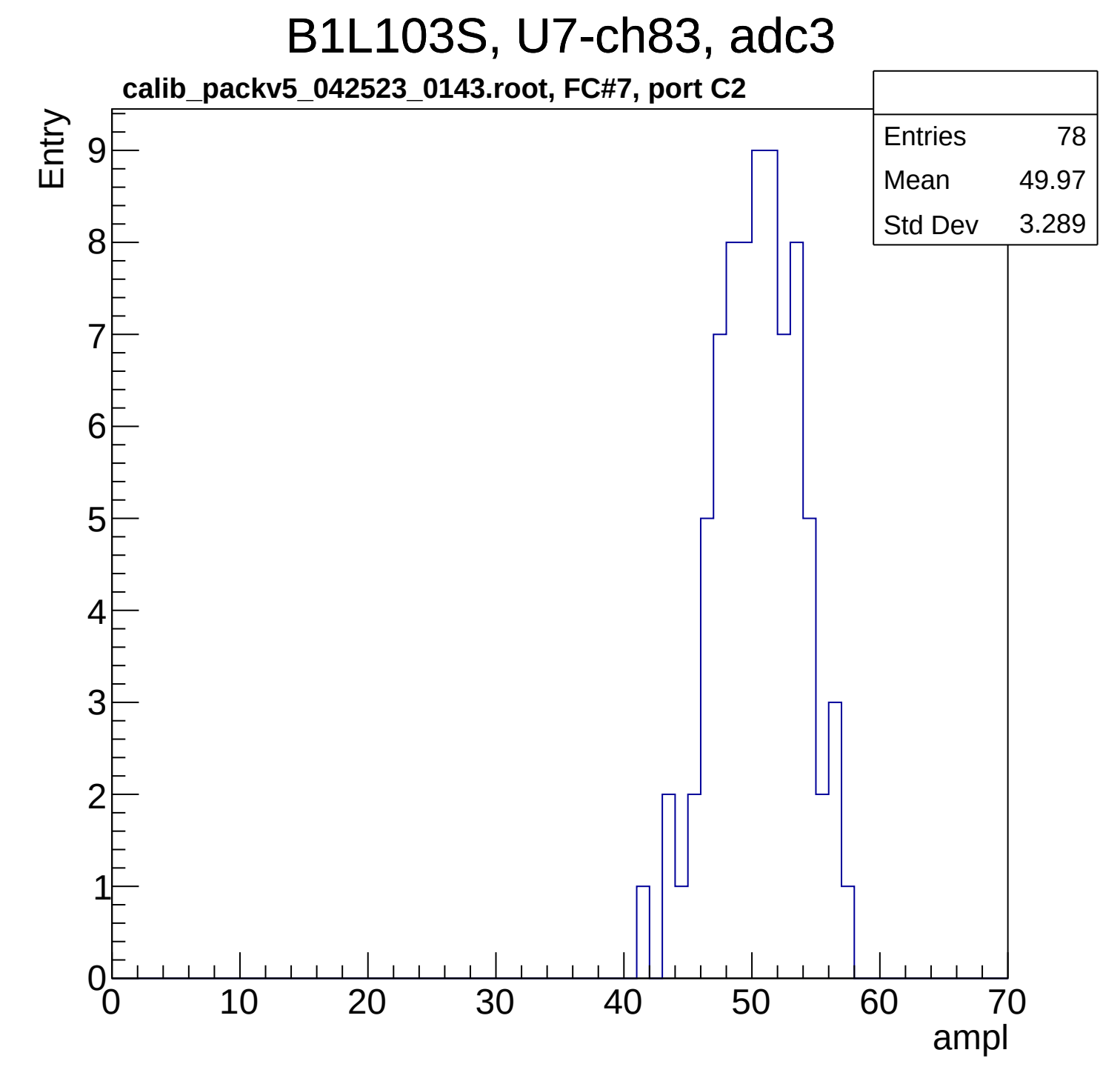
B1L103S, U7-ch83, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 78
Mean 49.97
Std Dev 3.289
Entry
ampl
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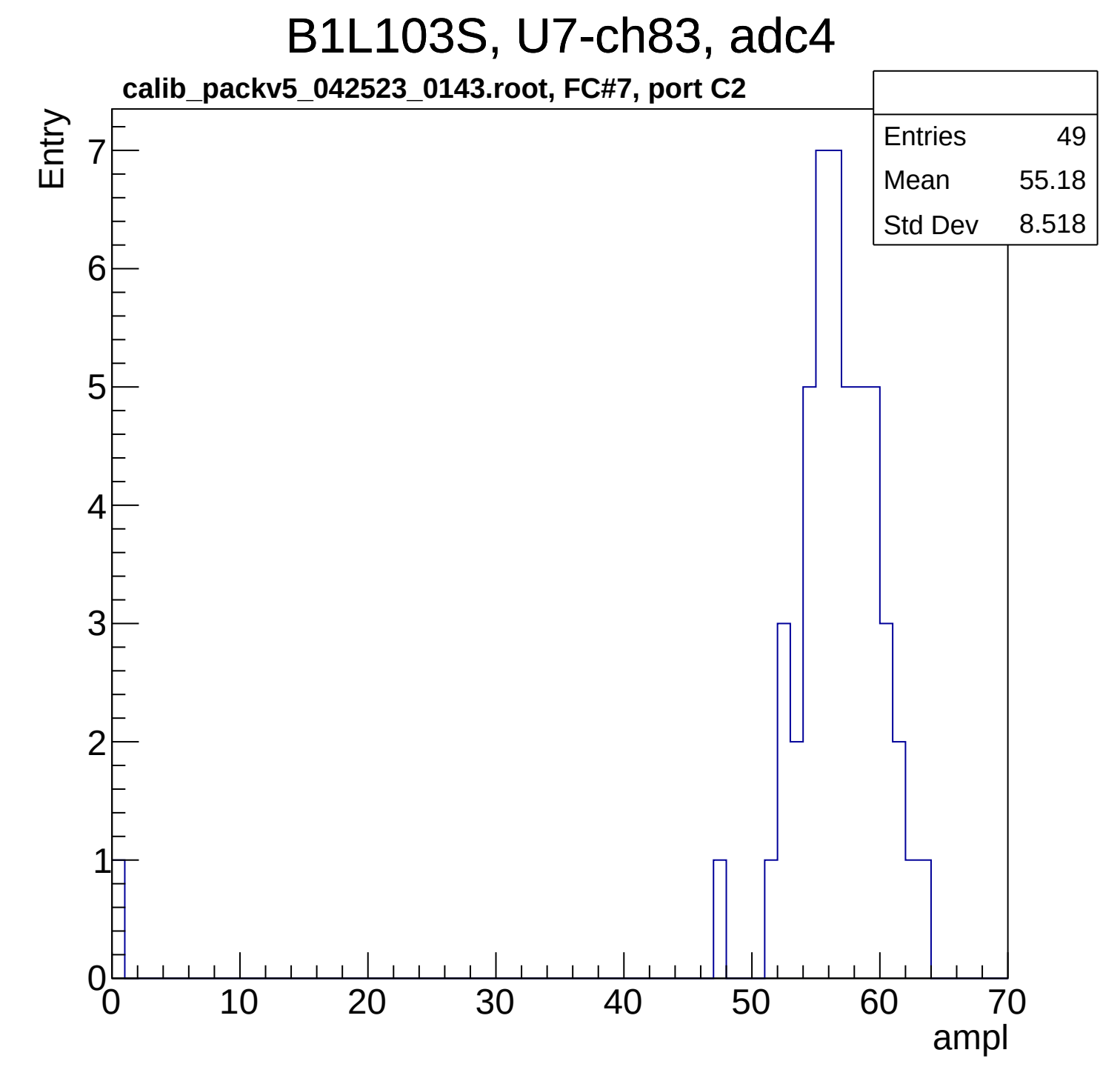
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch83, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 49
Mean 55.18
Std Dev 8.518
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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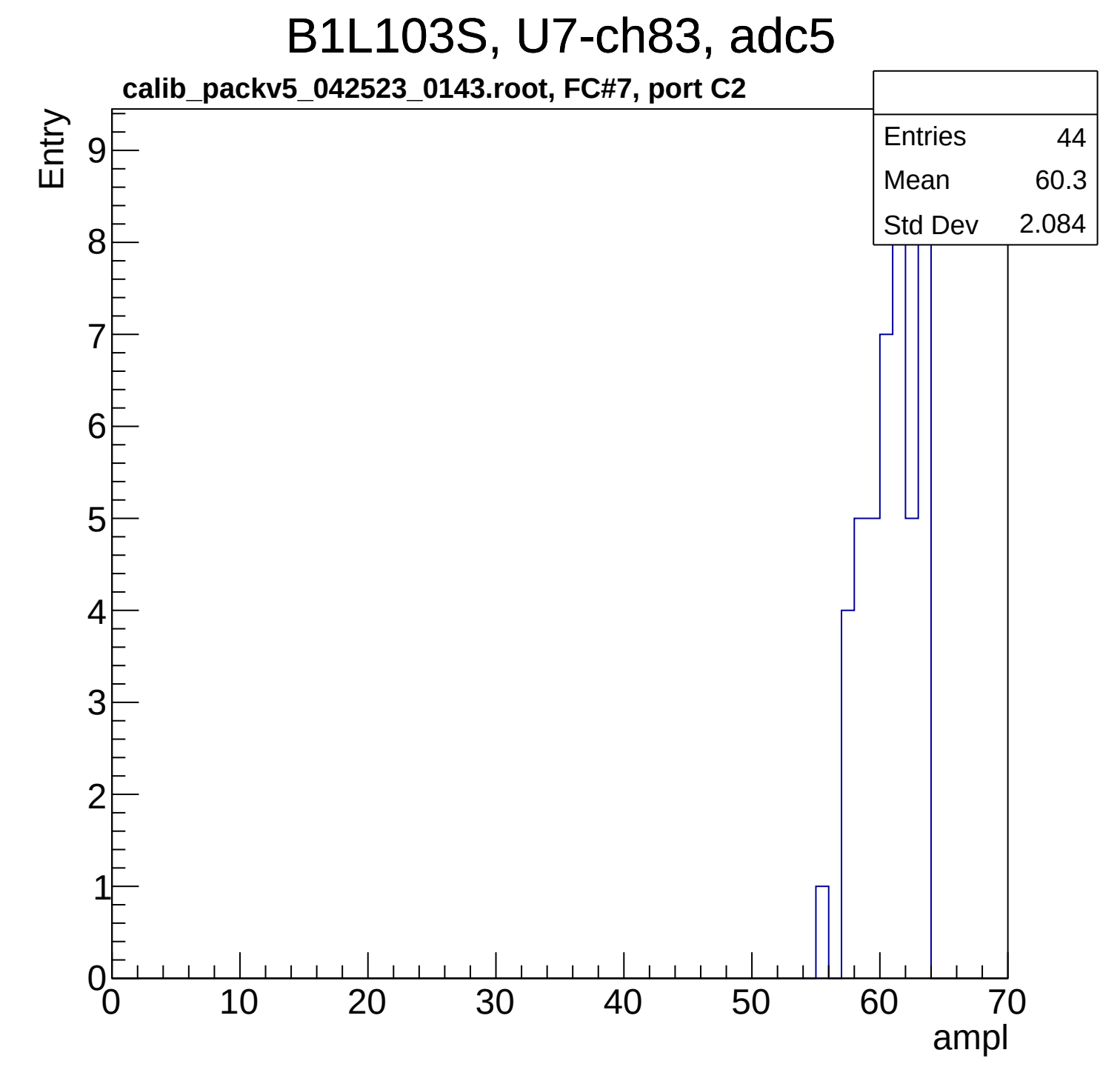
B1L103S, U7-ch83, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 44
Mean 60.3
Std Dev 2.084
Entry
ampl
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2
3
4
5
6
7
8
9
0
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30
40
50
60
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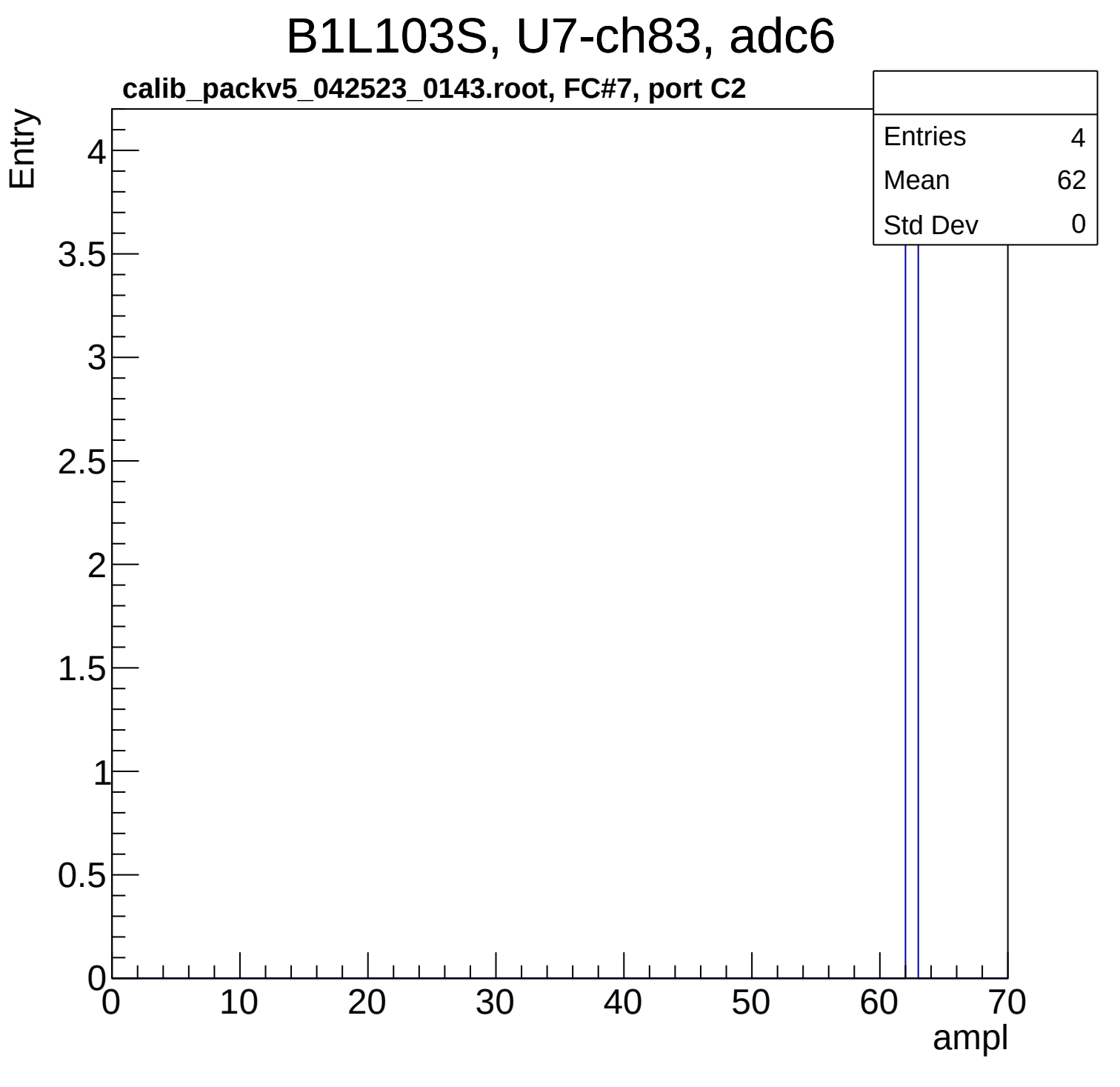
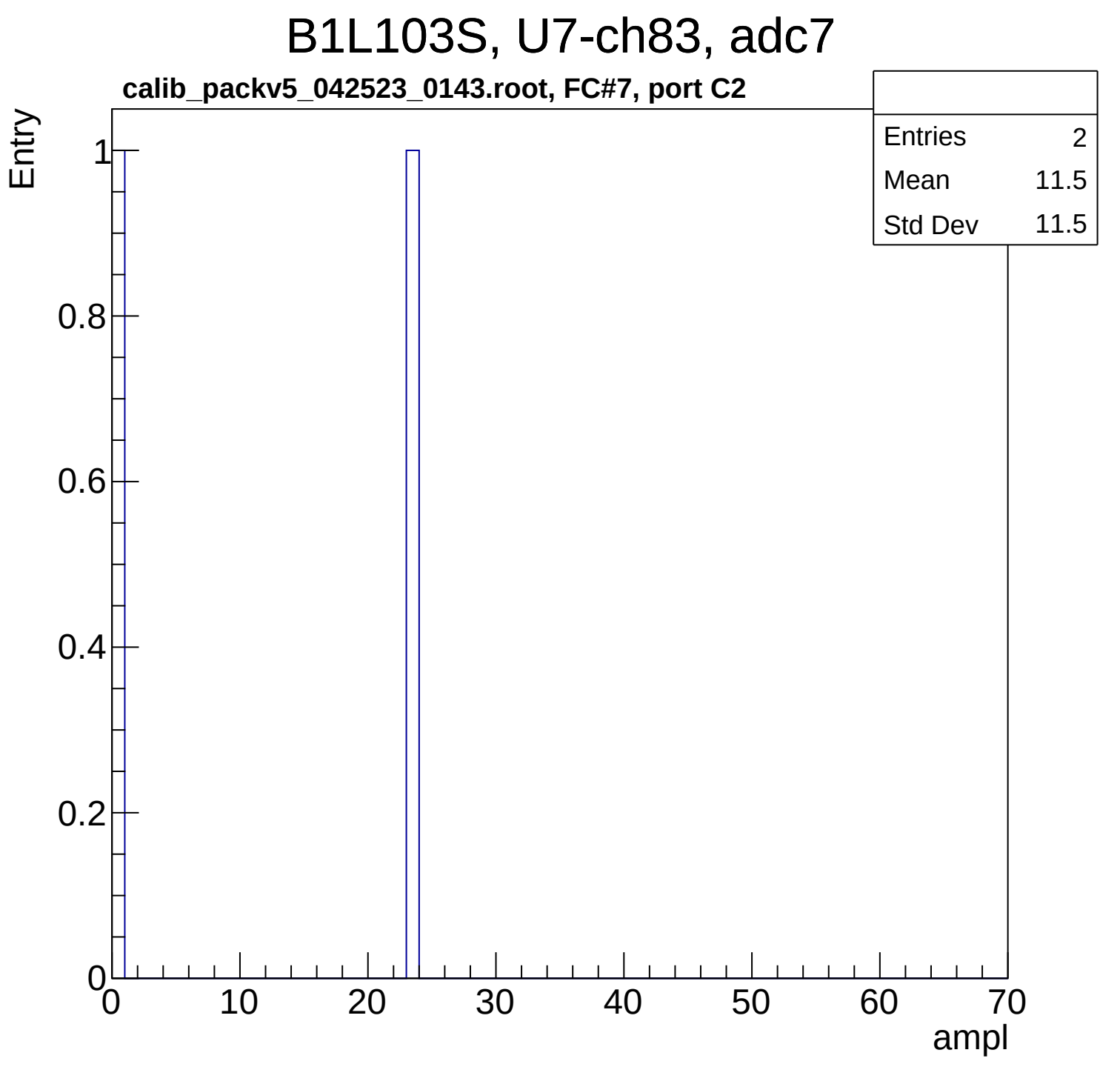
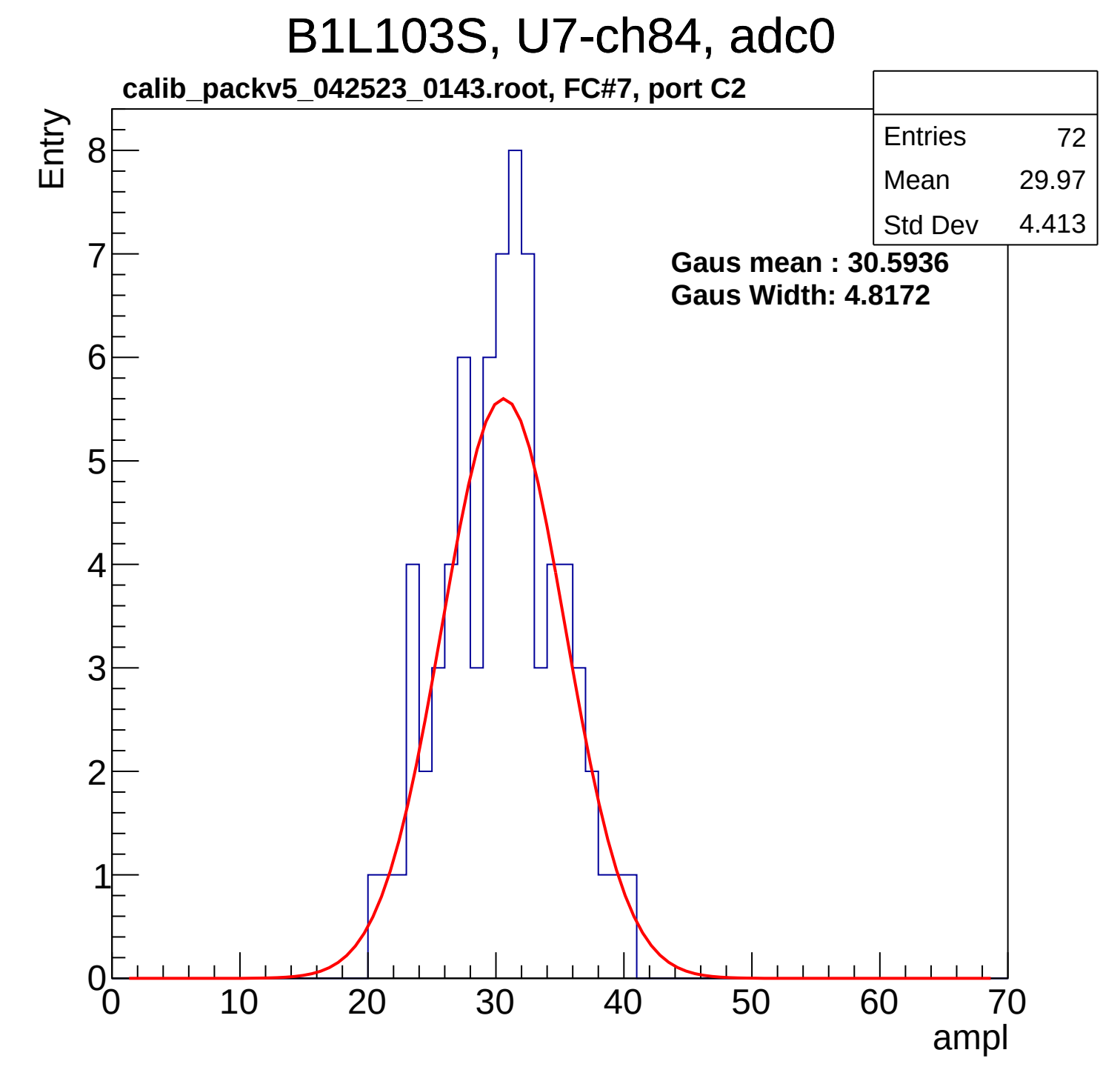

B1L103S, U7-ch83, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 4
Mean 62
Std Dev 0
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U7-ch83, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 11.5
Std Dev 11.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch84, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 72
Mean 29.97
Std Dev 4.413
Gaus mean : 30.5936
Gaus Width: 4.8172
Entry
ampl
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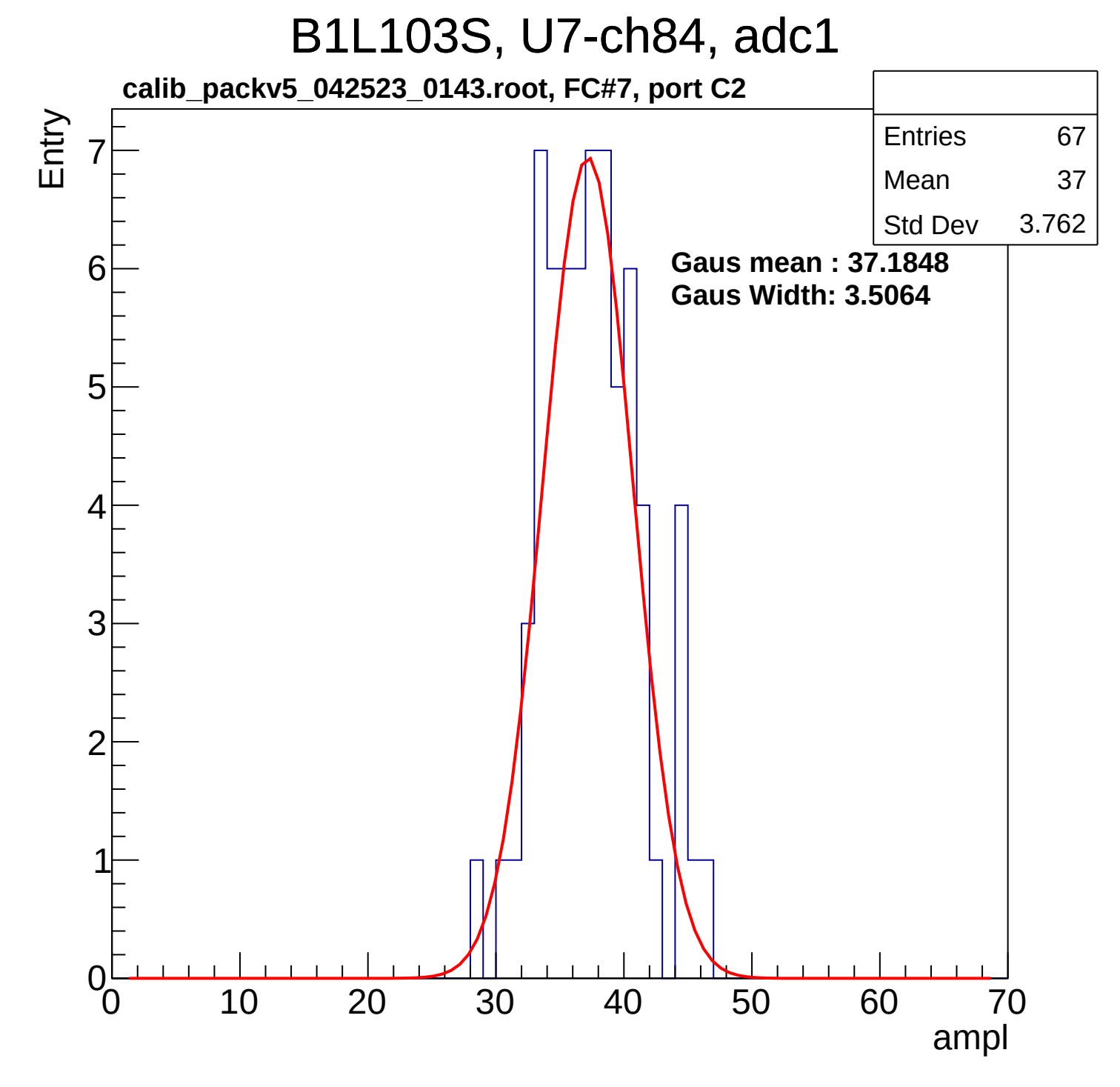
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch84, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 37
Std Dev 3.762
Gaus mean : 37.1848
Gaus Width: 3.5064
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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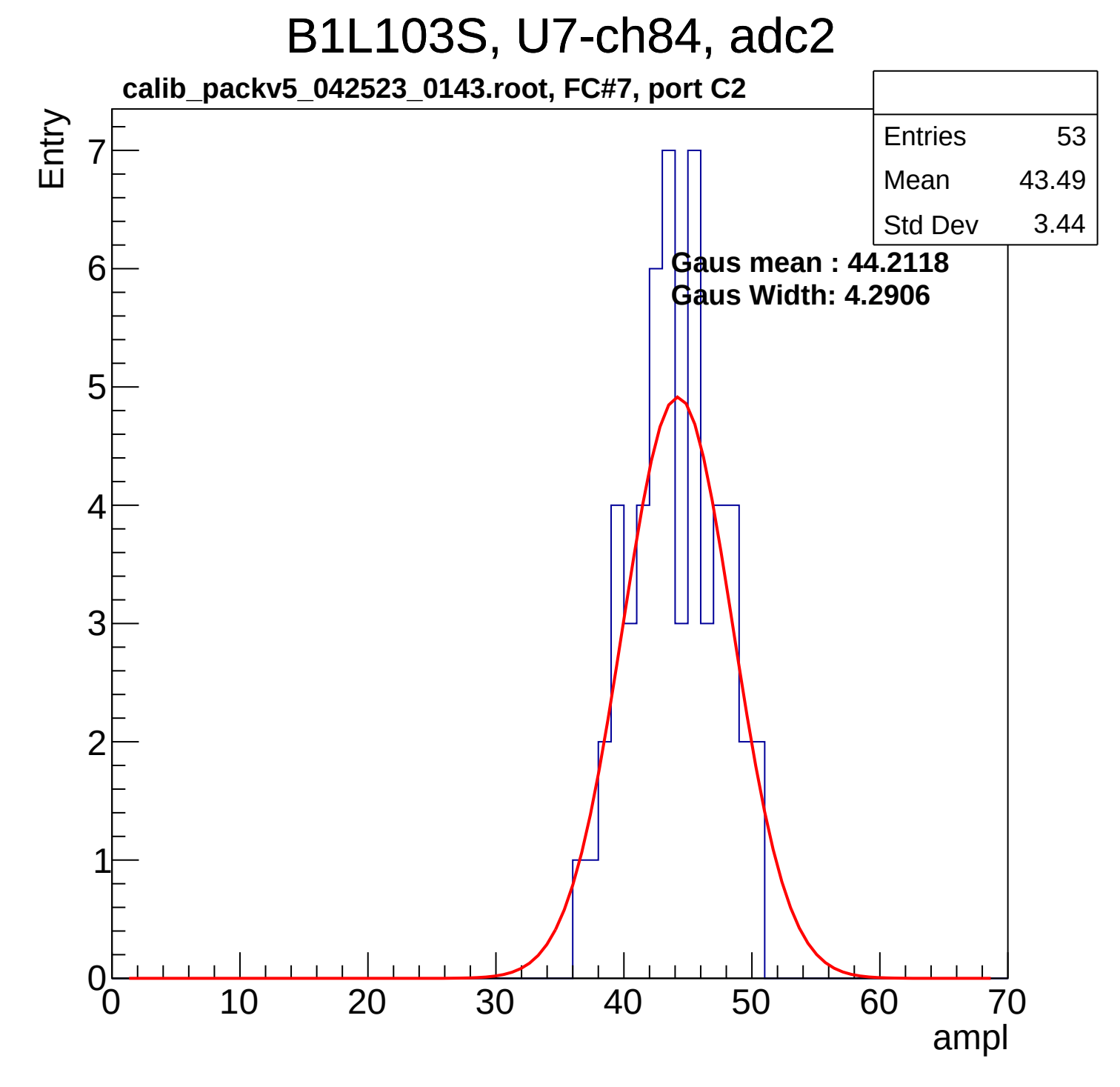
B1L103S, U7-ch84, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 43.49
Std Dev 3.44
Gaus mean : 44.2118
Gaus Width: 4.2906
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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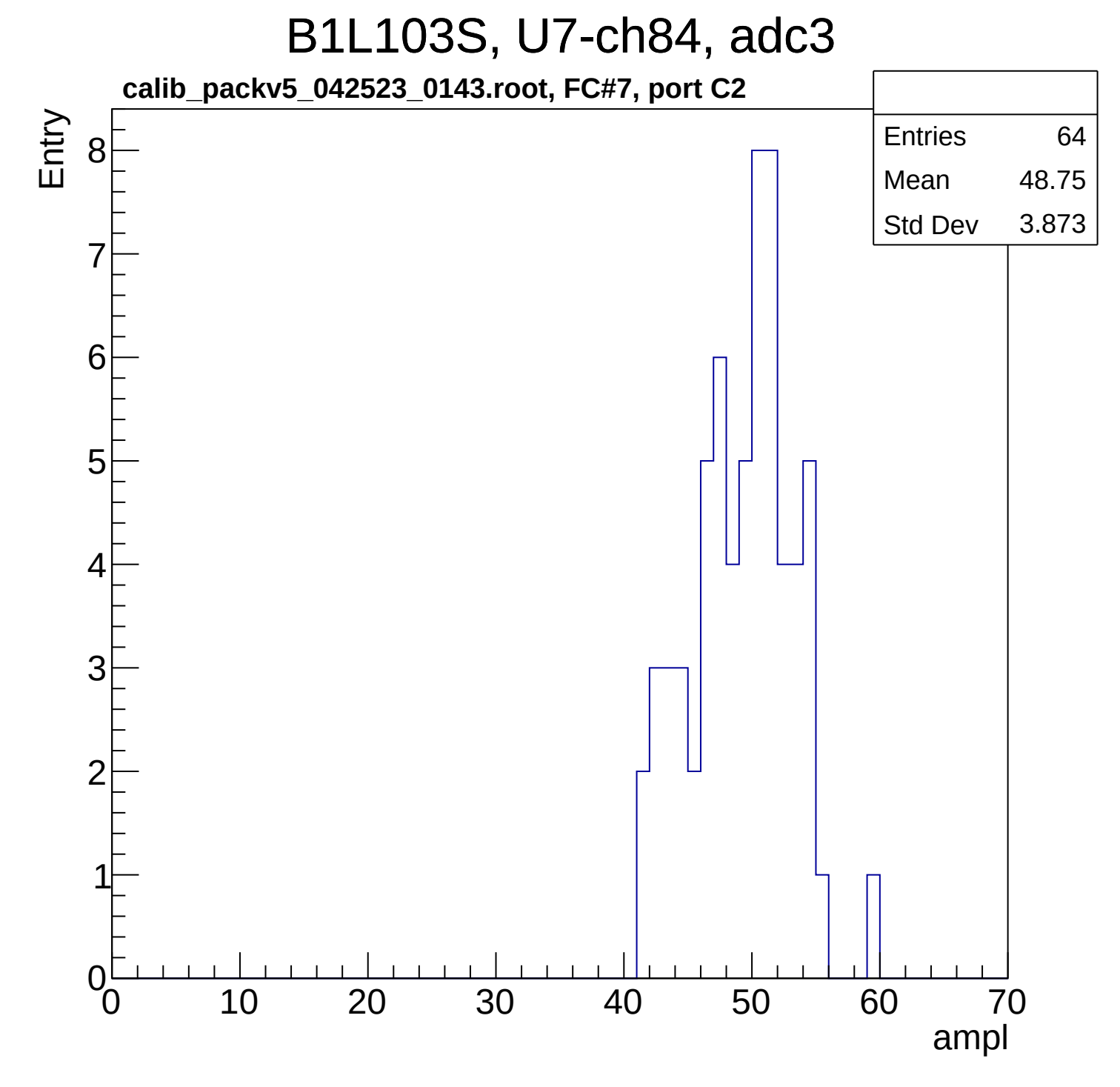
B1L103S, U7-ch84, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 48.75
Std Dev 3.873
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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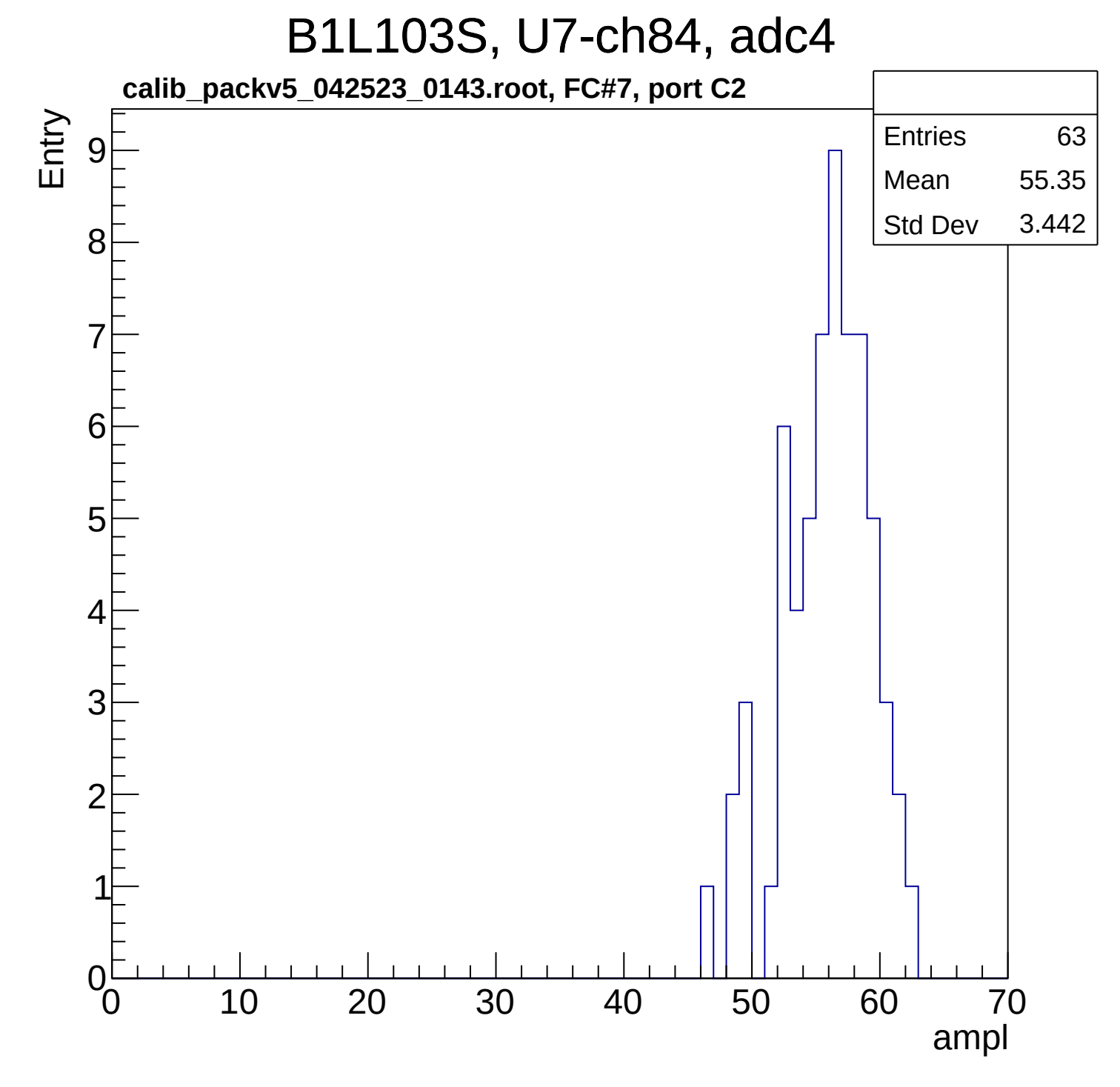
B1L103S, U7-ch84, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 55.35
Std Dev 3.442
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
30
40
50
60
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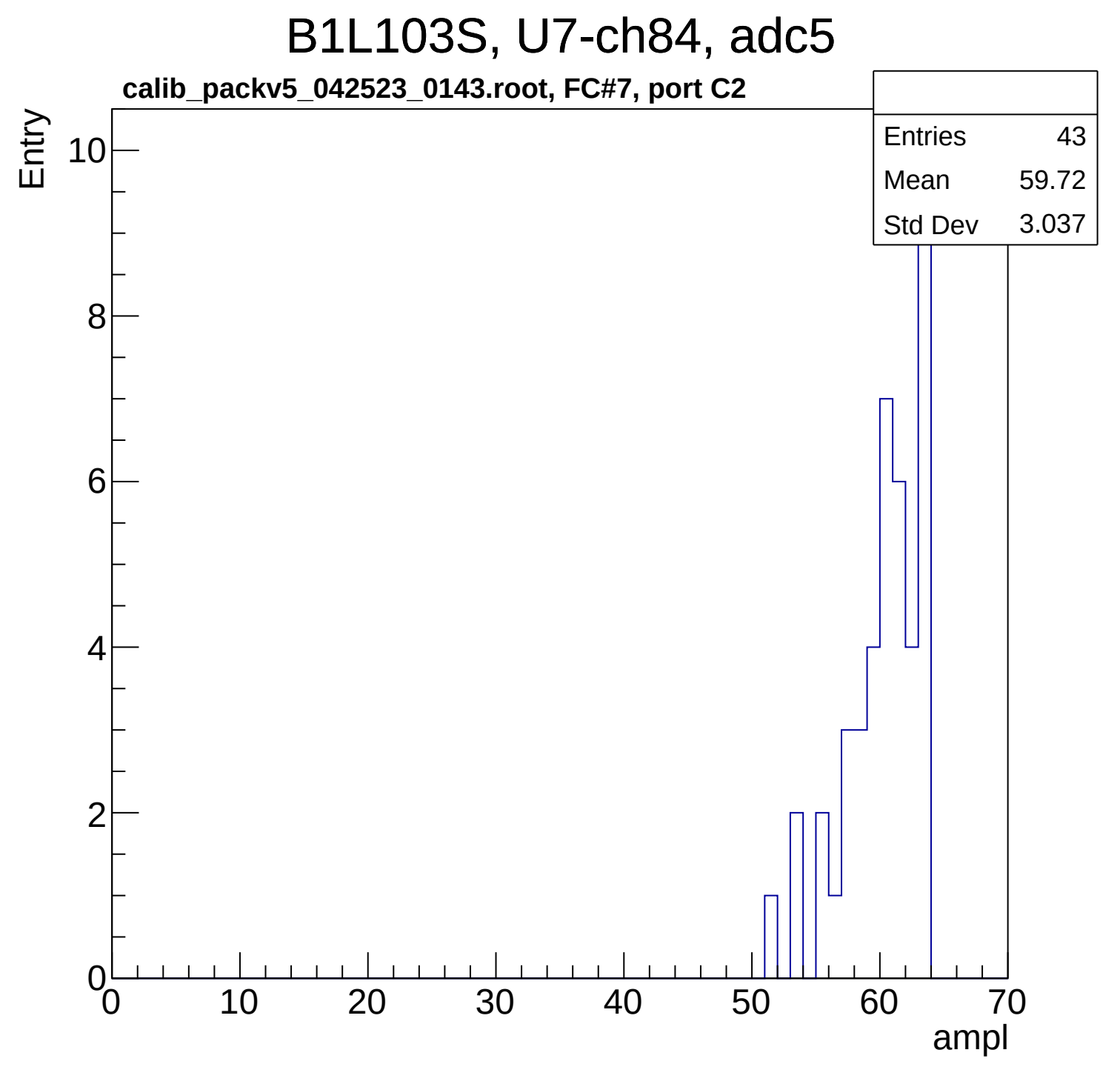
B1L103S, U7-ch84, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 43
Mean 59.72
Std Dev 3.037
Entry
ampl
0
2
4
6
8
10
0
10
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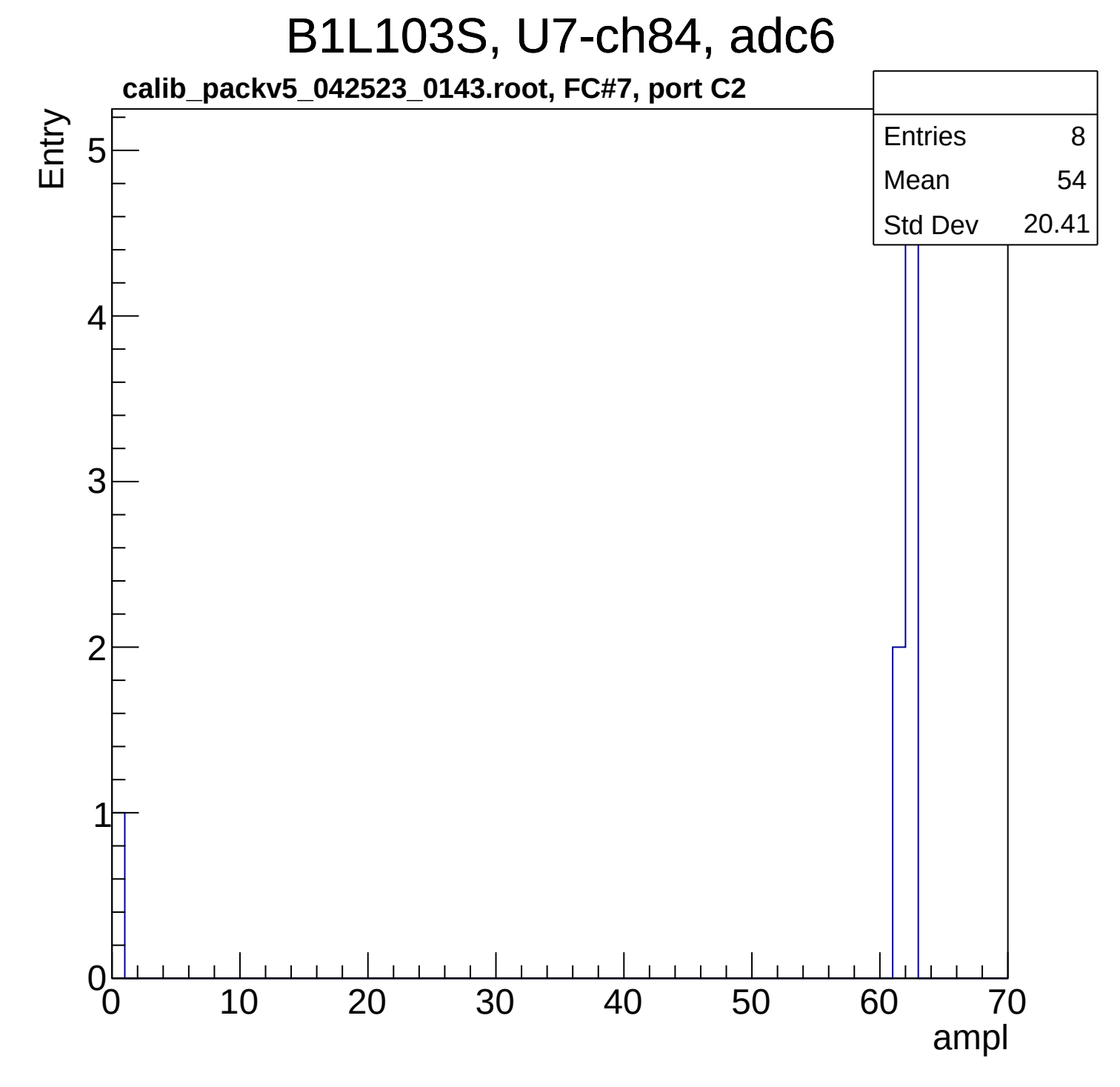
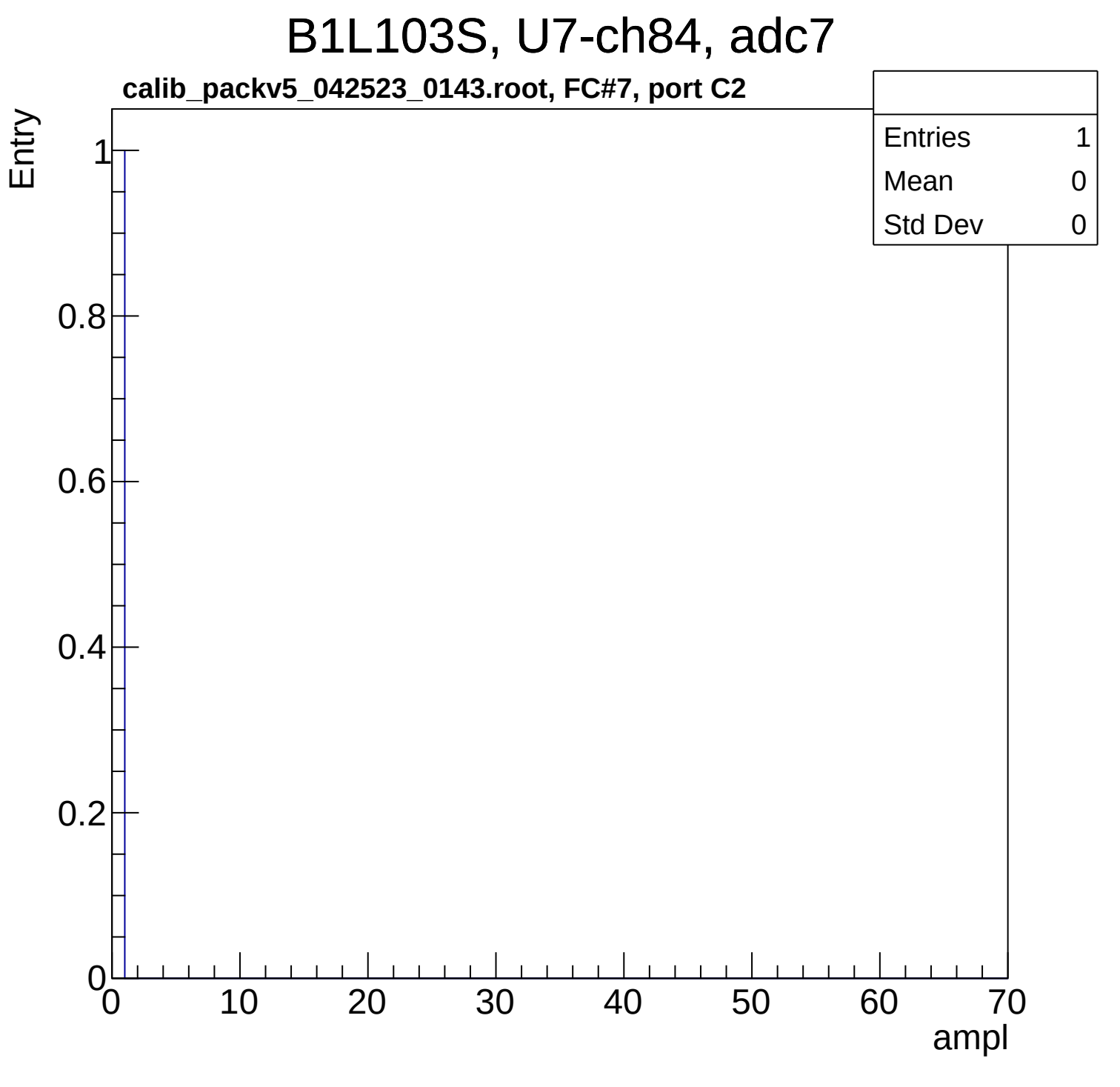
30
40
50
60
70


B1L103S, U7-ch84, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 8
Mean 54
Std Dev 20.41
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch84, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
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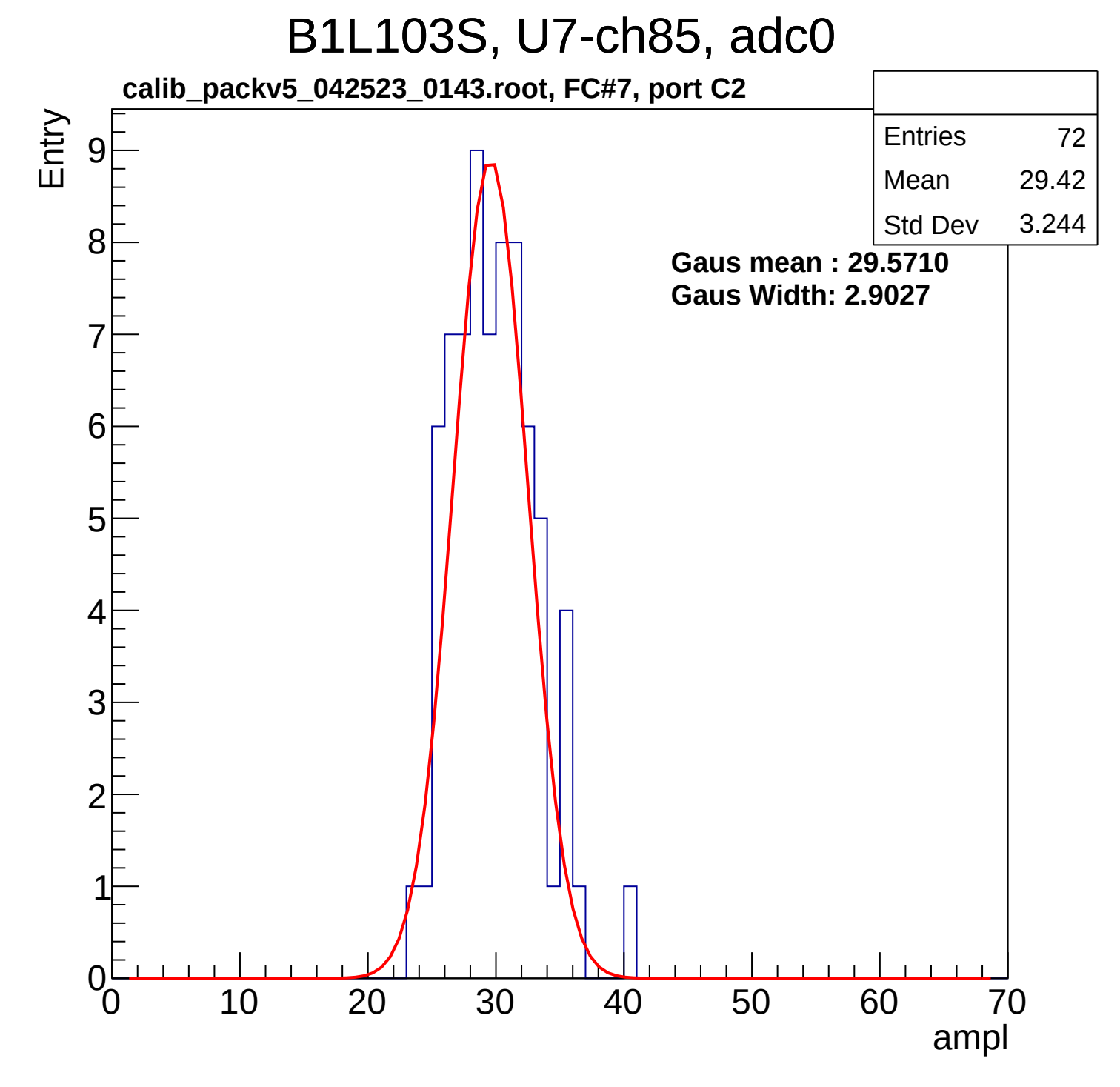
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch85, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 72
Mean 29.42
Std Dev 3.244
Gaus mean : 29.5710
Gaus Width: 2.9027
Entry
ampl
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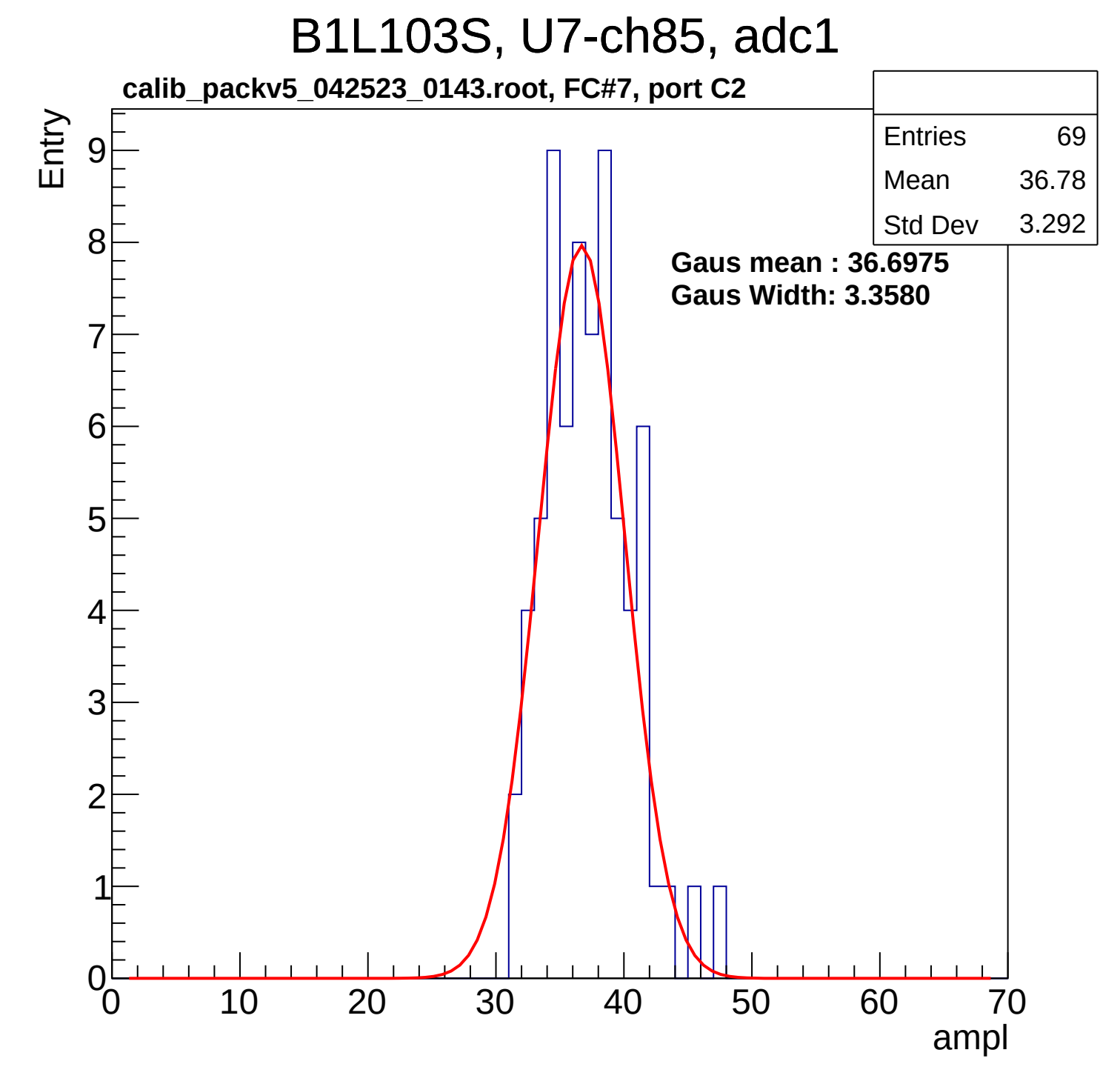
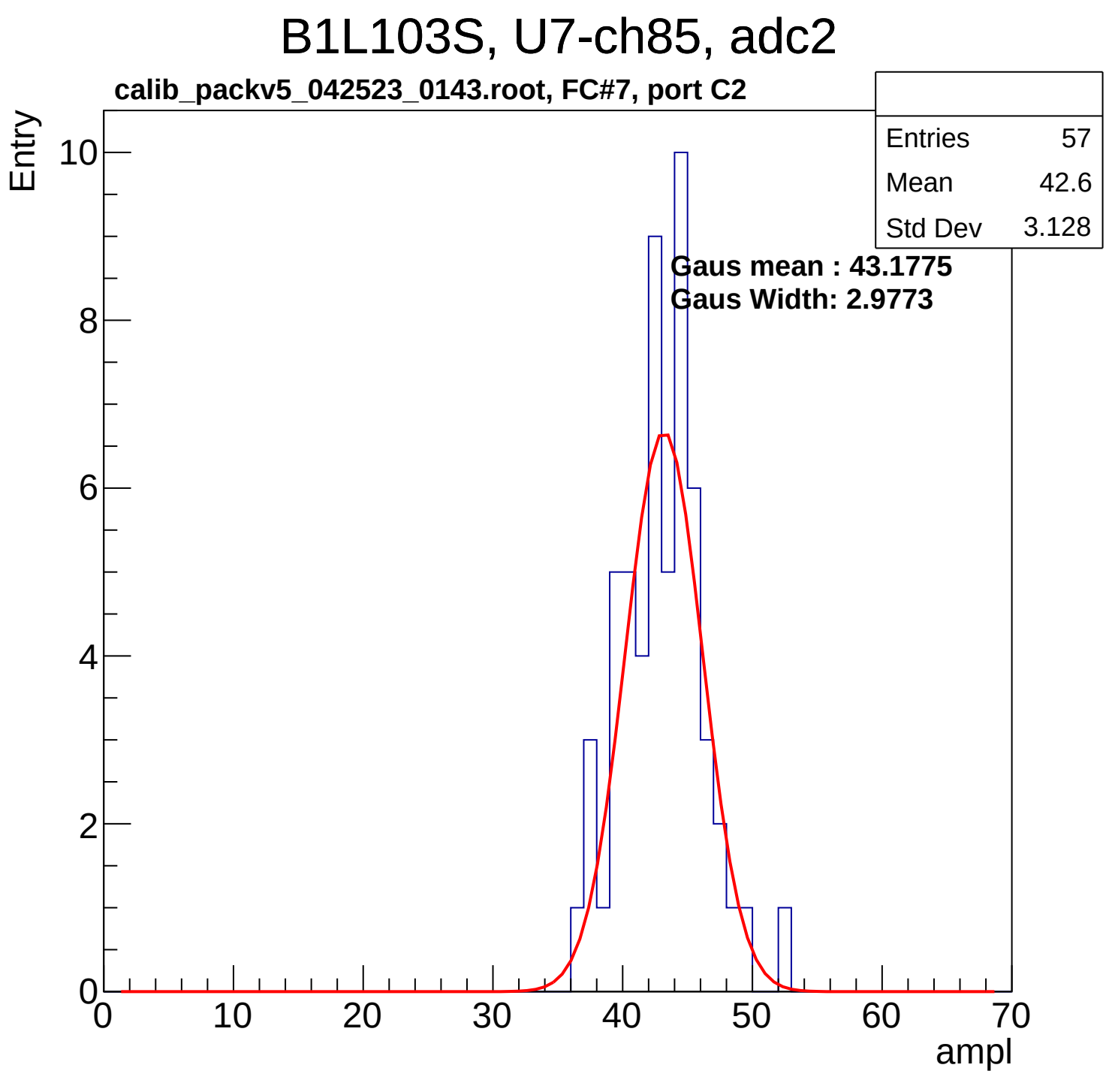
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch85, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 36.78
Std Dev 3.292
Gaus mean : 36.6975
Gaus Width: 3.3580
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch85, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 42.6
Std Dev 3.128
Gaus mean : 43.1775
Gaus Width: 2.9773
Entry
ampl
0
2
4
6
8
10
0
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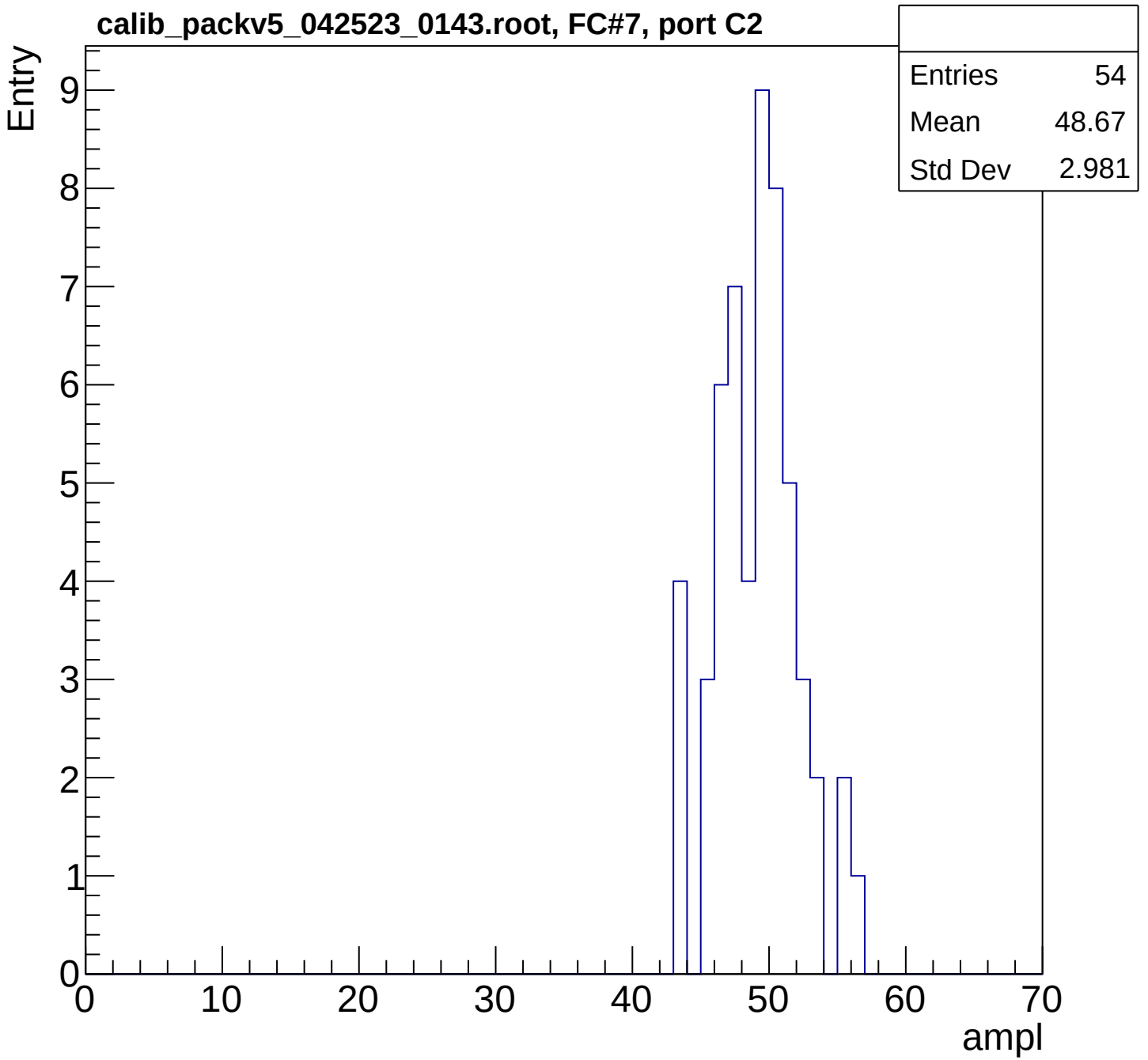
20
30
40
50
60
70


B1L103S, U7-ch85, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 54
Mean 48.67
Std Dev 2.981
Entry
ampl
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3
4
5
6
7
8
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0
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40
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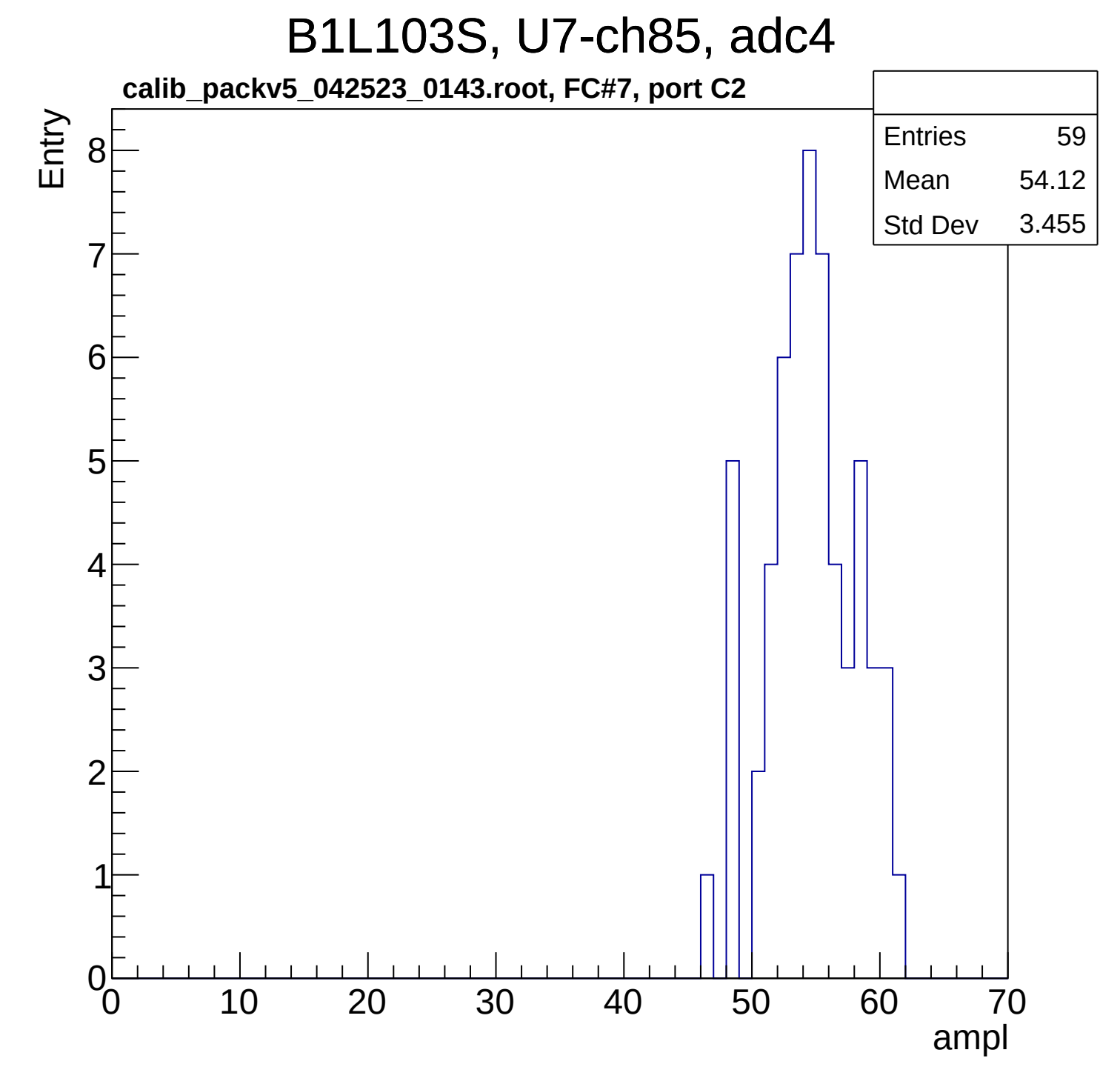
60
70


B1L103S, U7-ch85, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 54.12
Std Dev 3.455
Entry
ampl
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1
2
3
4
5
6
7
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0
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20
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60
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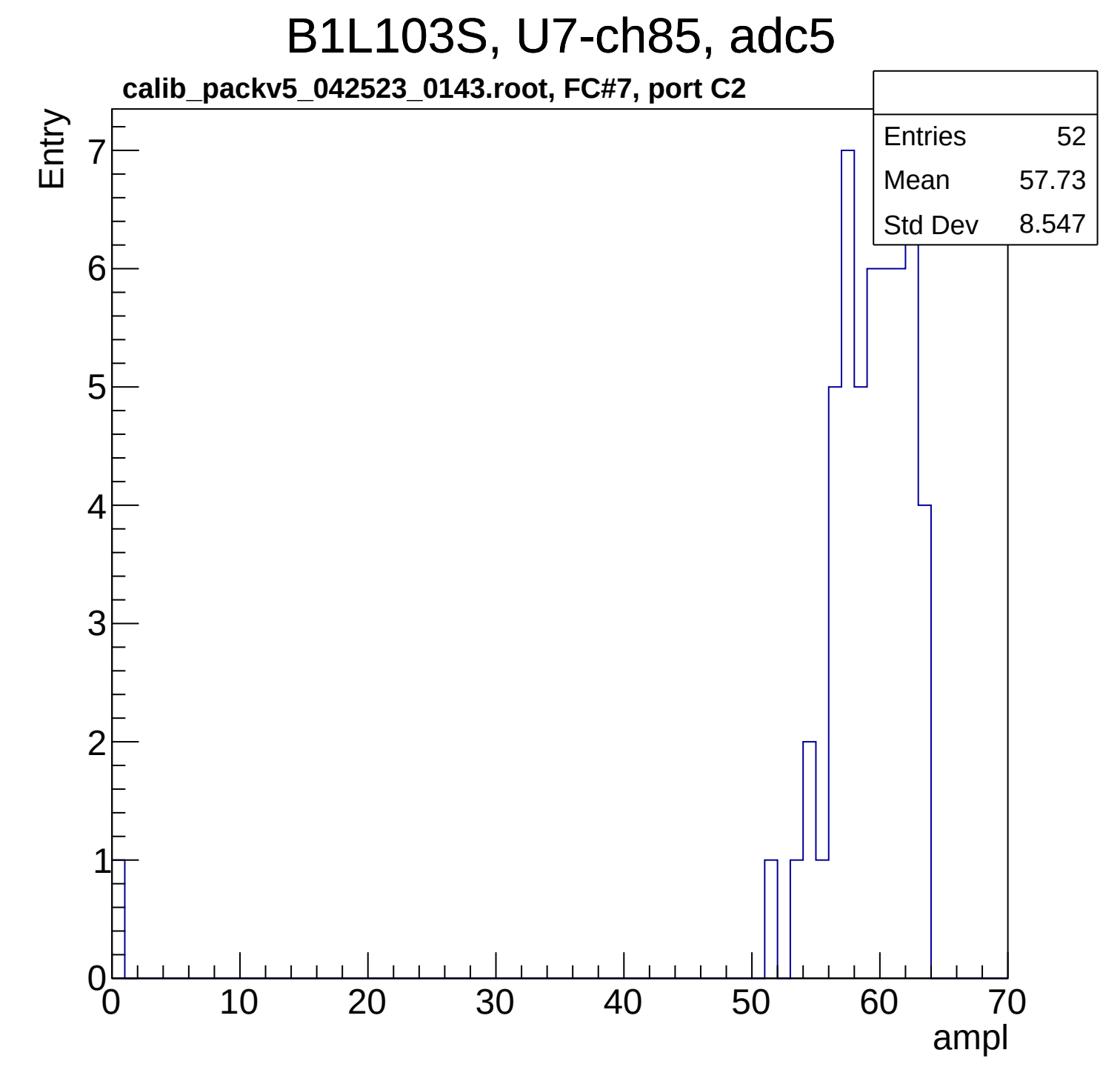
B1L103S, U7-ch85, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 52
Mean 57.73
Std Dev 8.547
Entry
ampl
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0
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60
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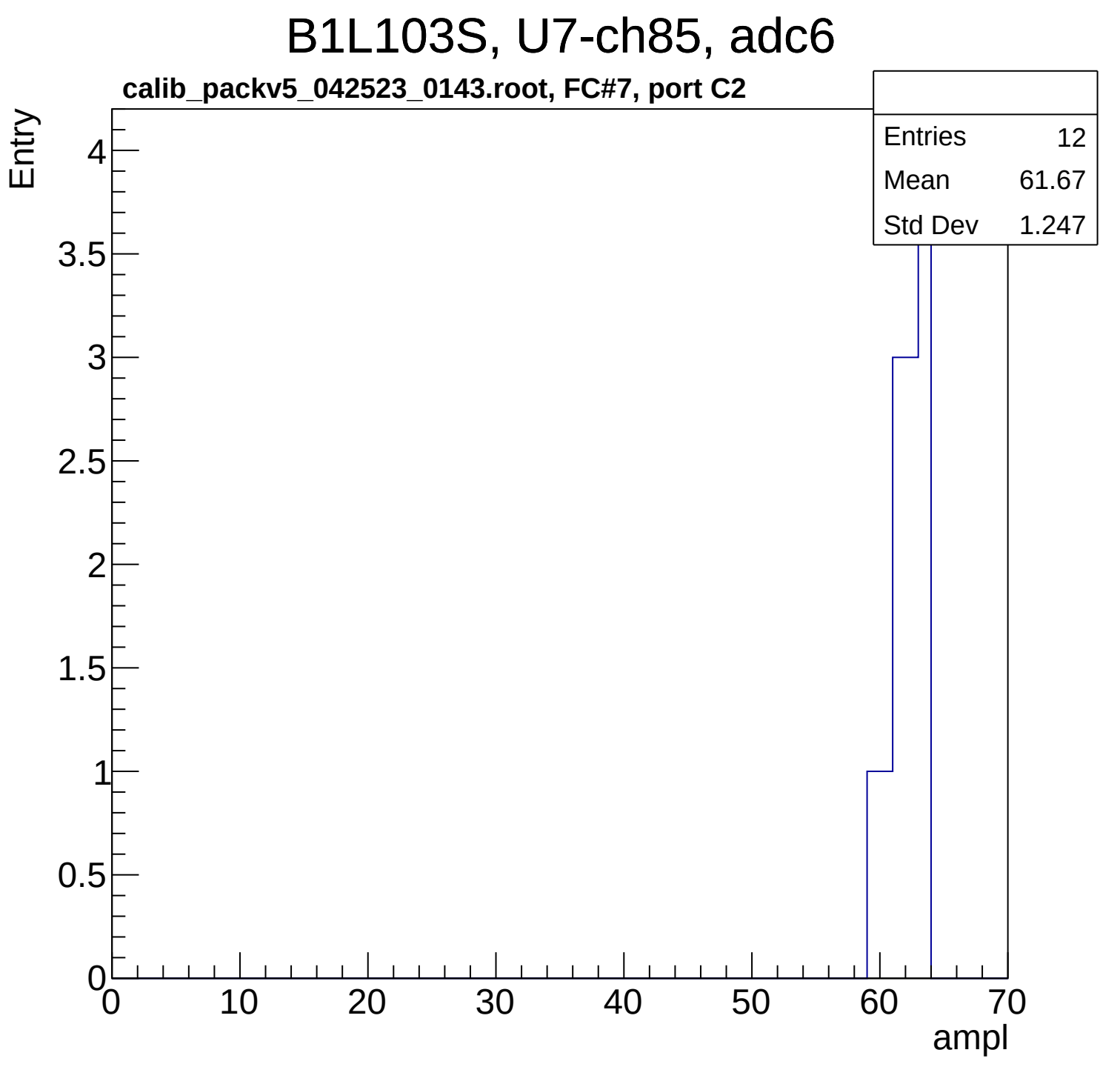
B1L103S, U7-ch85, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 12
Mean 61.67
Std Dev 1.247
Entry
ampl
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1.5
2
2.5
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3.5
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0
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60
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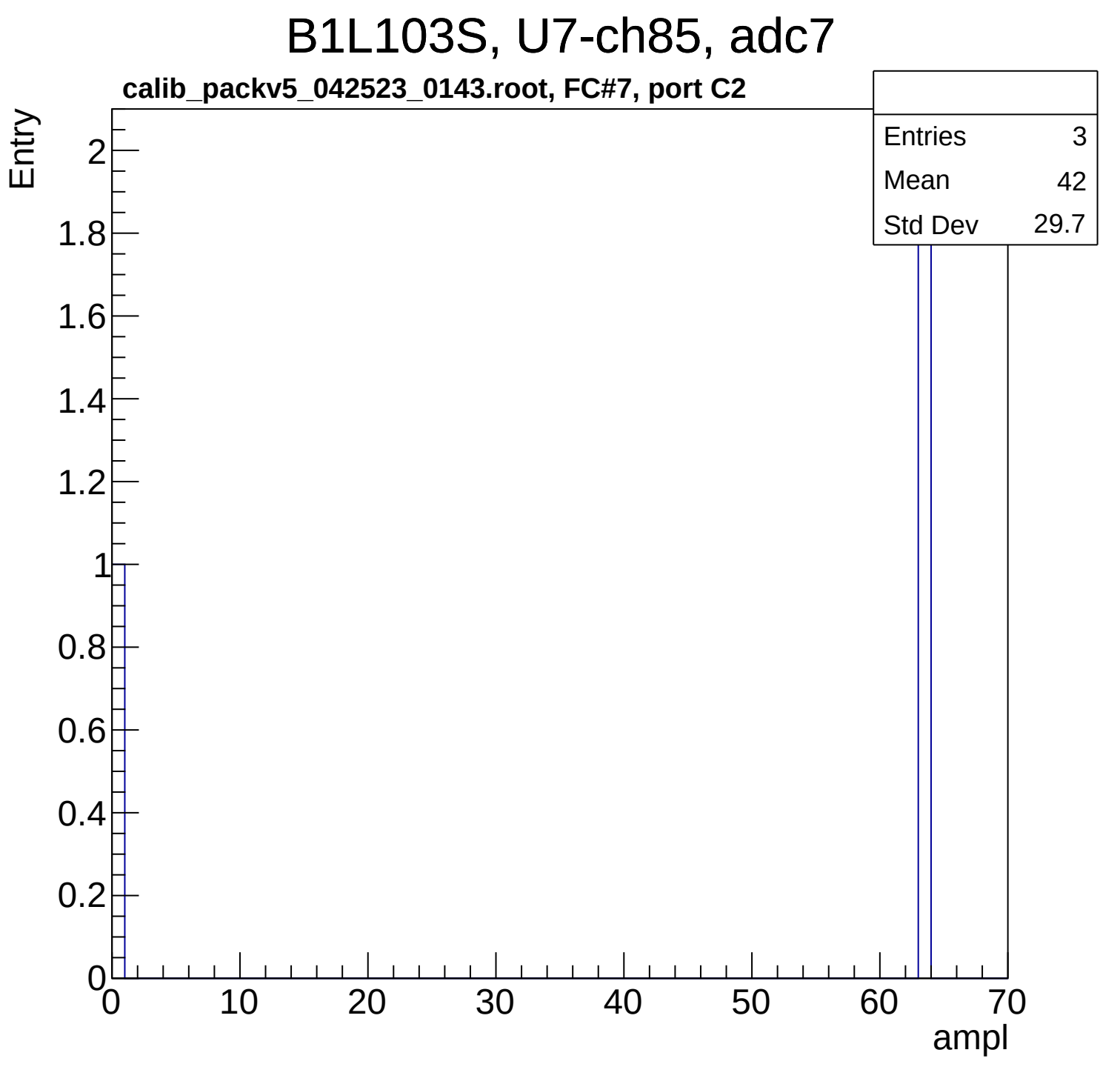
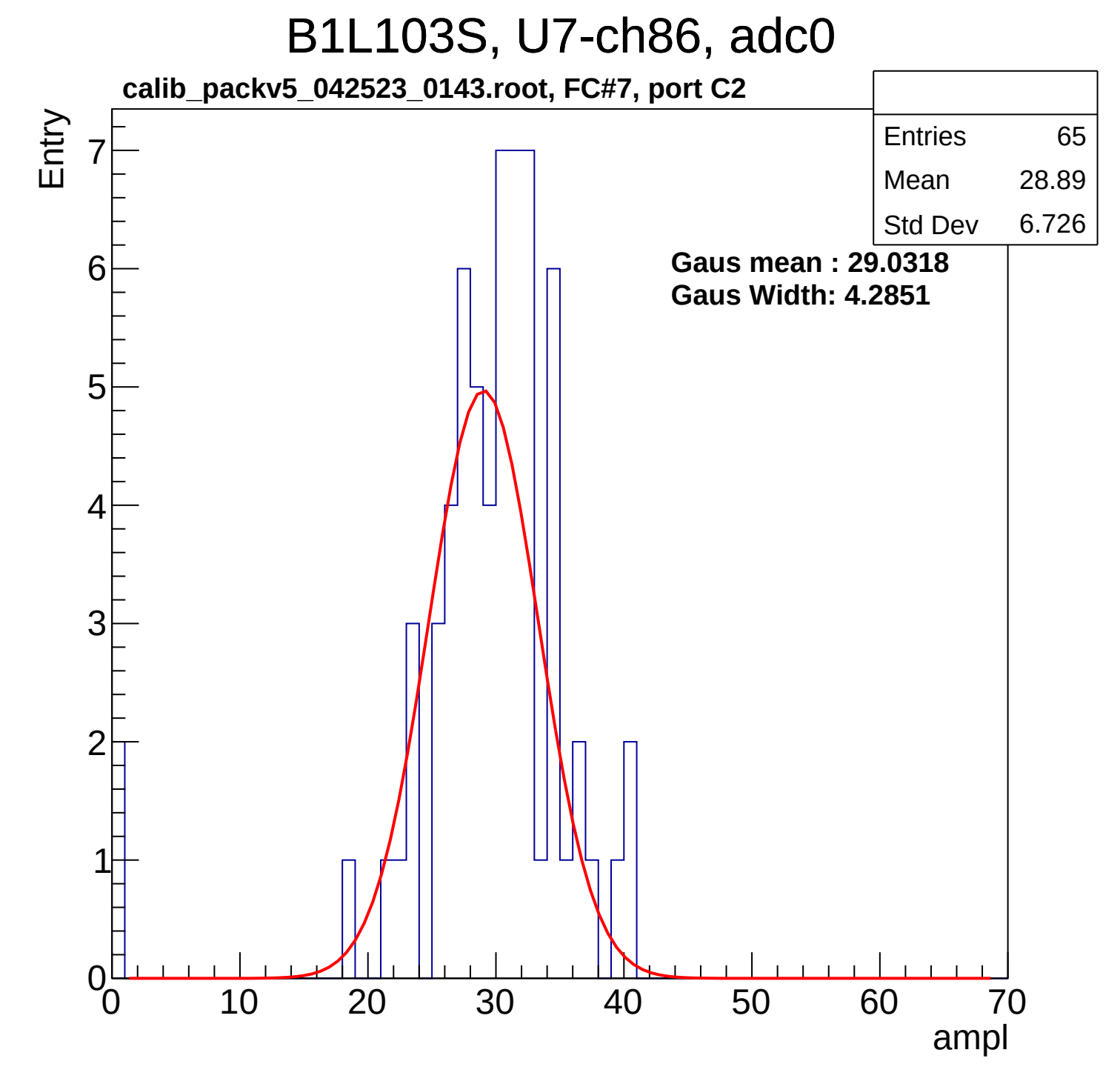

B1L103S, U7-ch85, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 42
Std Dev 29.7
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U7-ch86, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 28.89
Std Dev 6.726
Gaus mean : 29.0318
Gaus Width: 4.2851
Entry
ampl
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2
3
4
5
6
7
0
10
20
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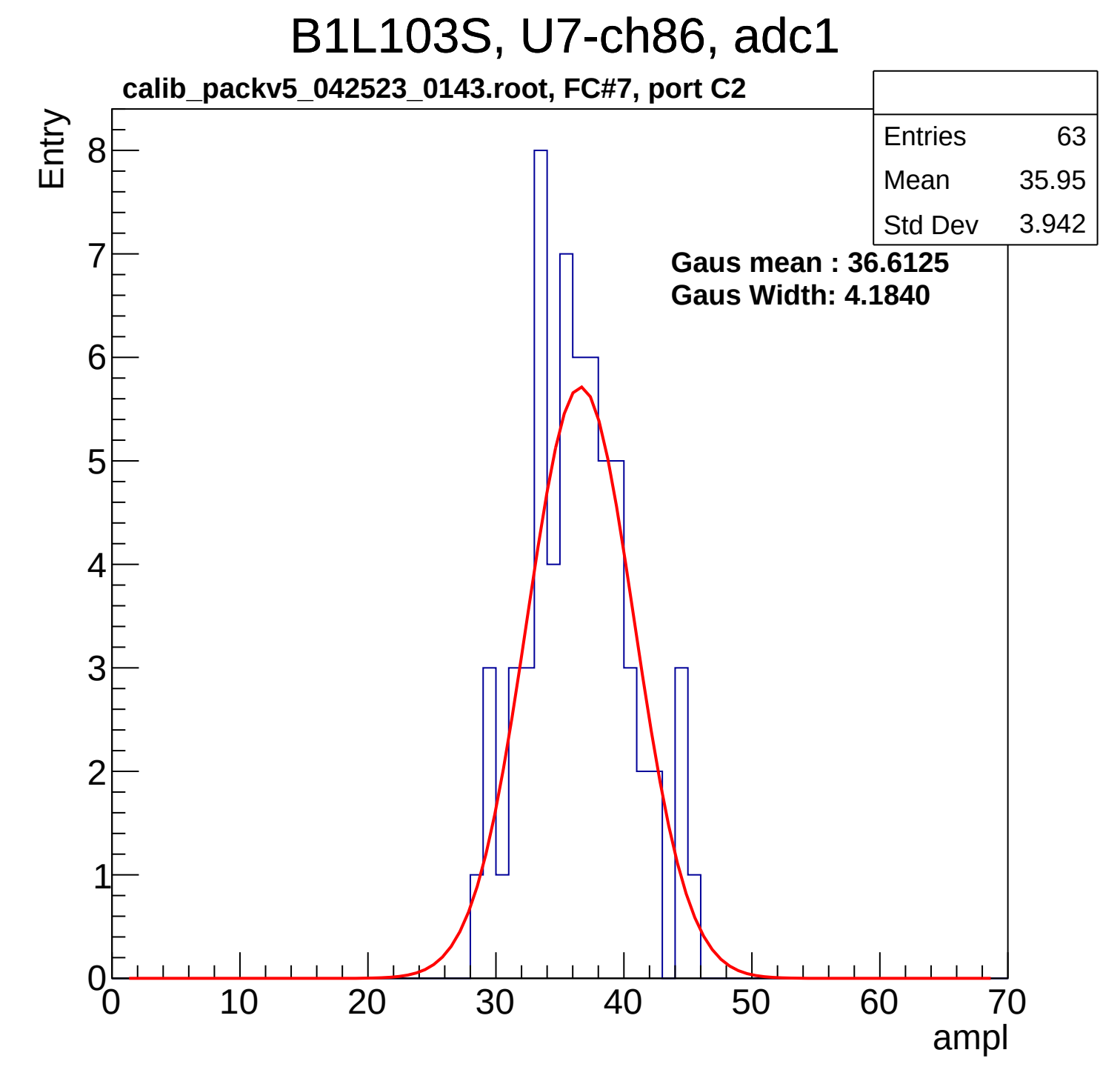
40
50
60
70


B1L103S, U7-ch86, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 35.95
Std Dev 3.942
Gaus mean : 36.6125
Gaus Width: 4.1840
Entry
ampl
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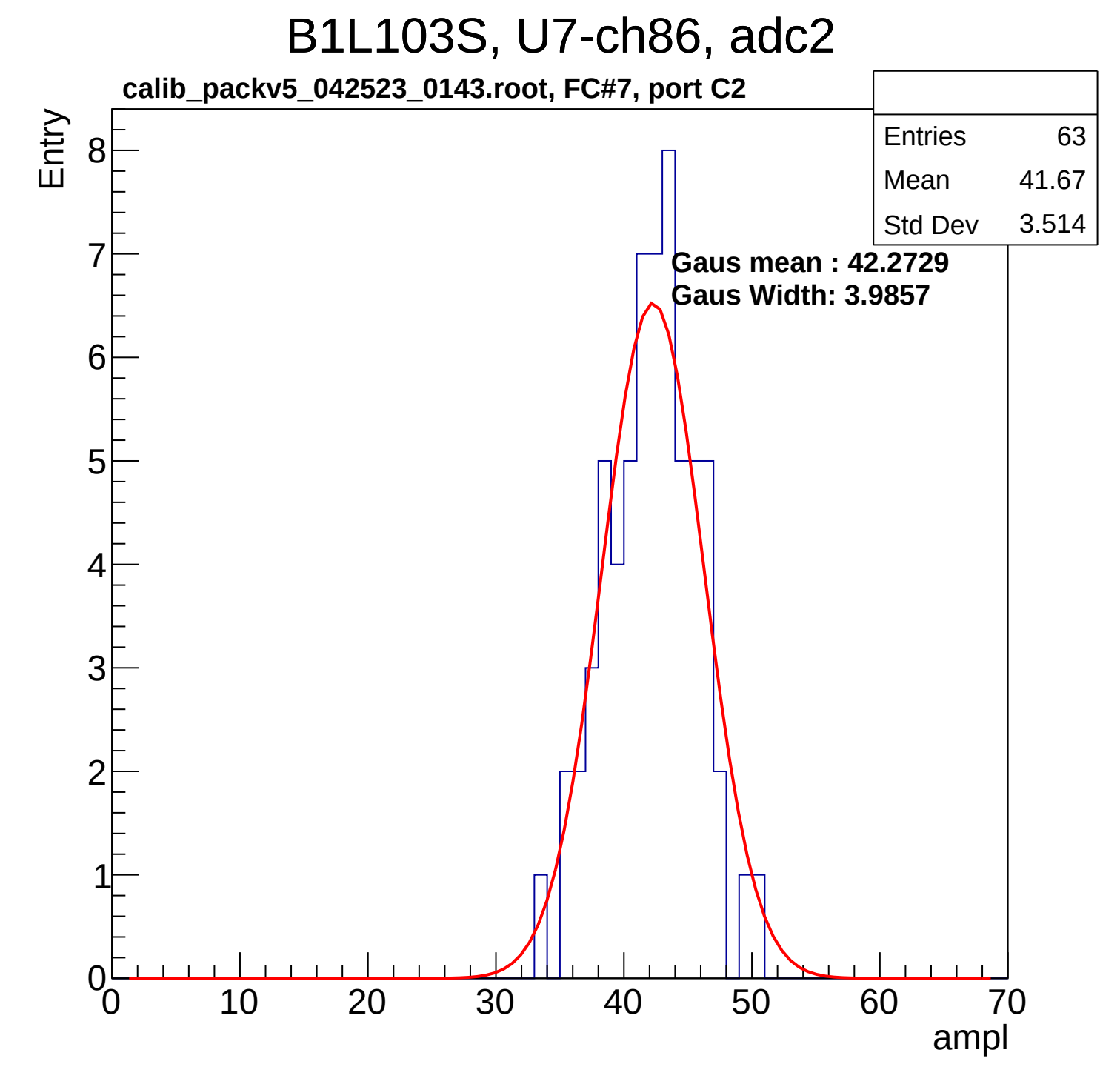
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch86, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 41.67
Std Dev 3.514
Gaus mean : 42.2729
Gaus Width: 3.9857
Entry
ampl
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1
2
3
4
5
6
7
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0
10
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60
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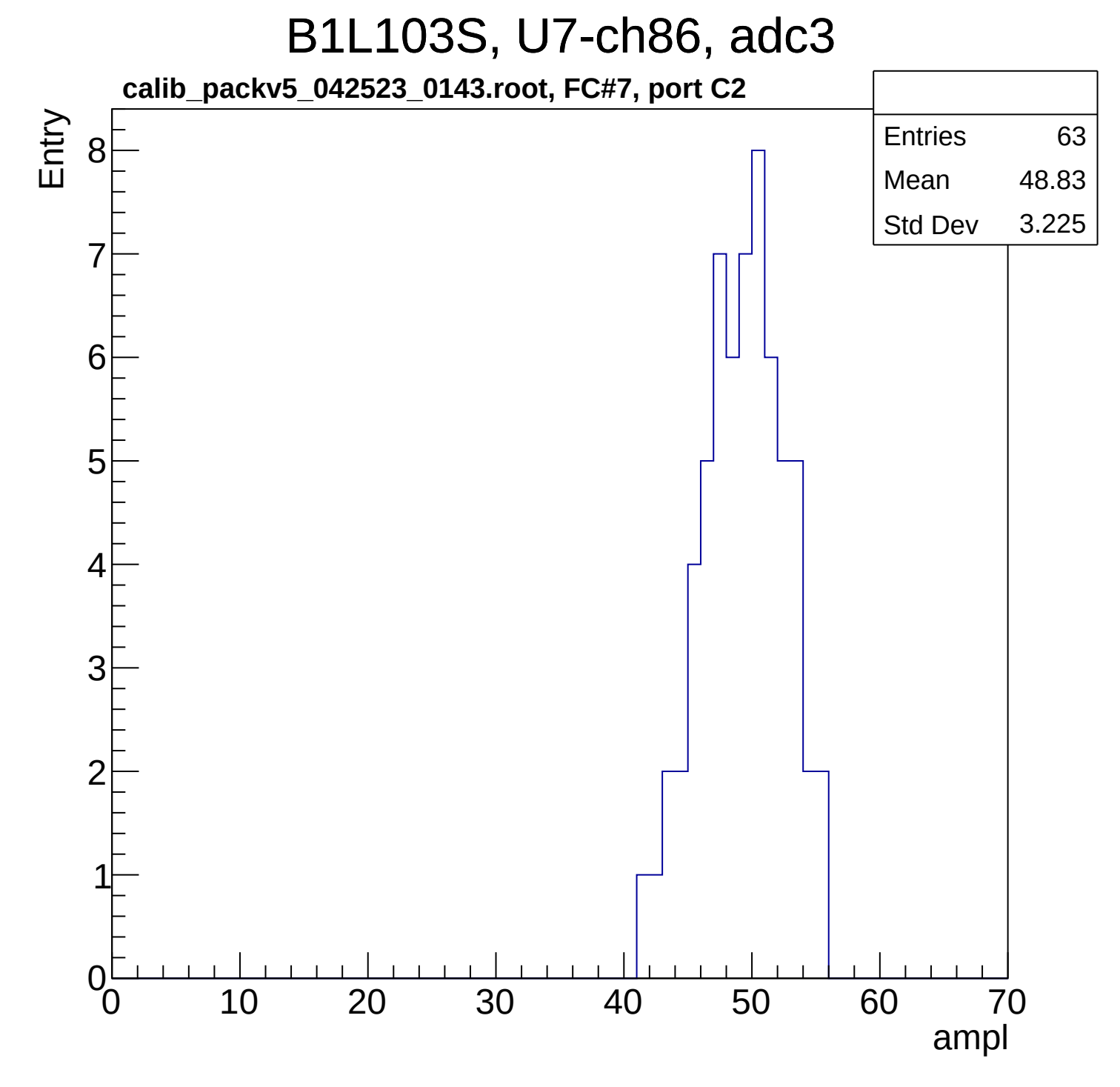
B1L103S, U7-ch86, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 48.83
Std Dev 3.225
Entry
ampl
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3
4
5
6
7
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0
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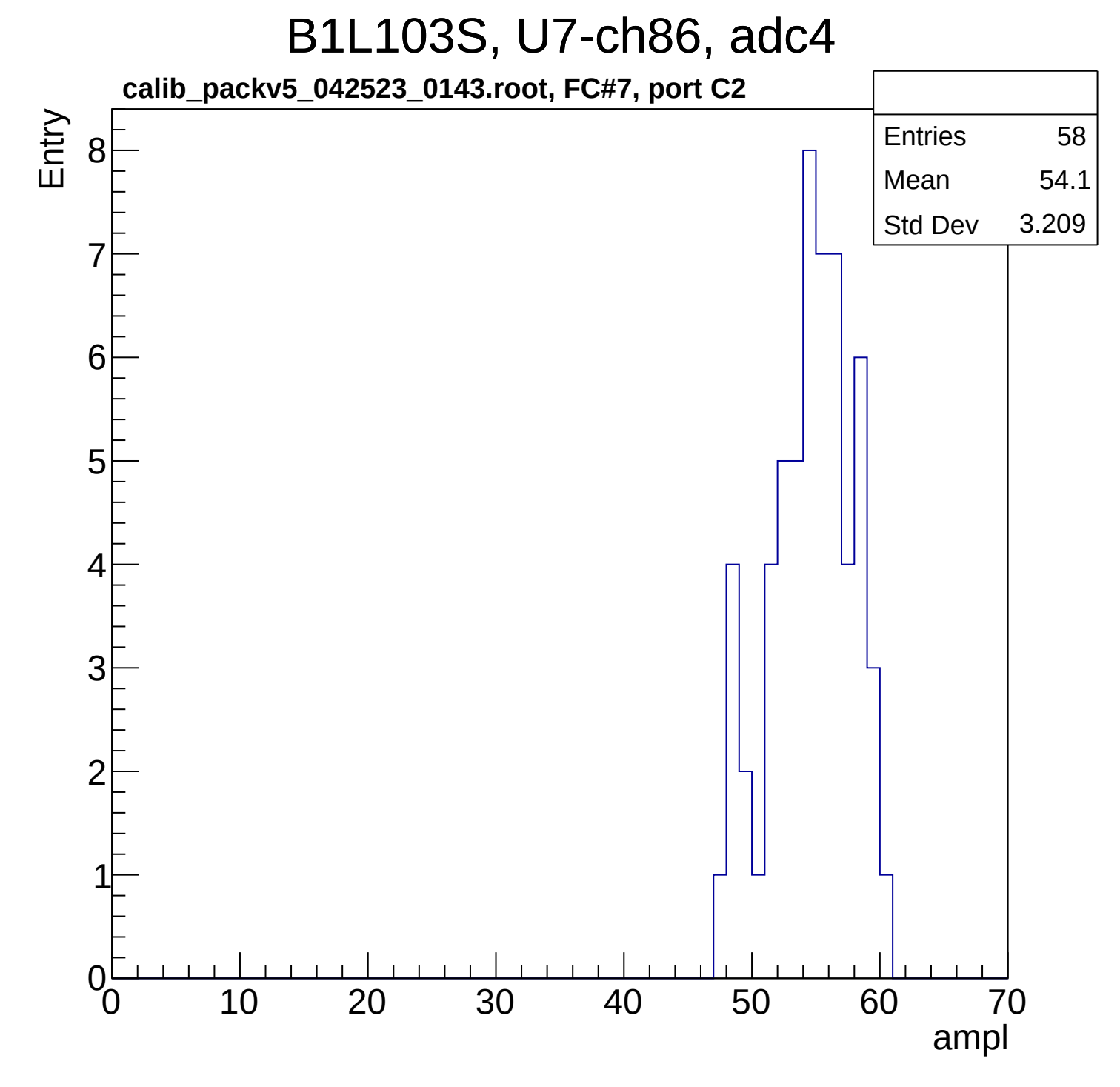
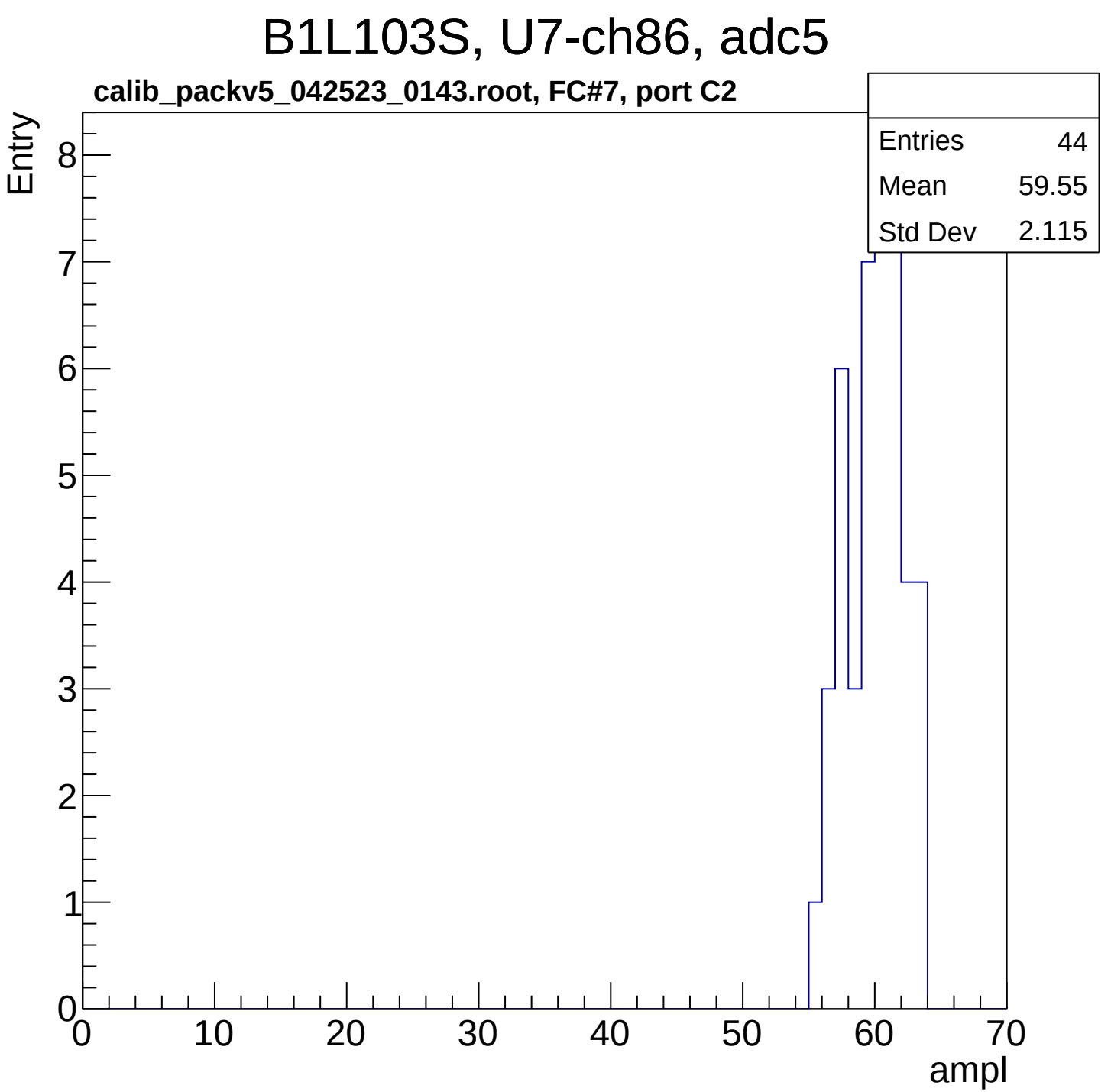

B1L103S, U7-ch86, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 58
Mean 54.1
Std Dev 3.209
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch86, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 44
Mean 59.55
Std Dev 2.115
Entry
0
1
2
3
4
5
6
7
8
0
10
20
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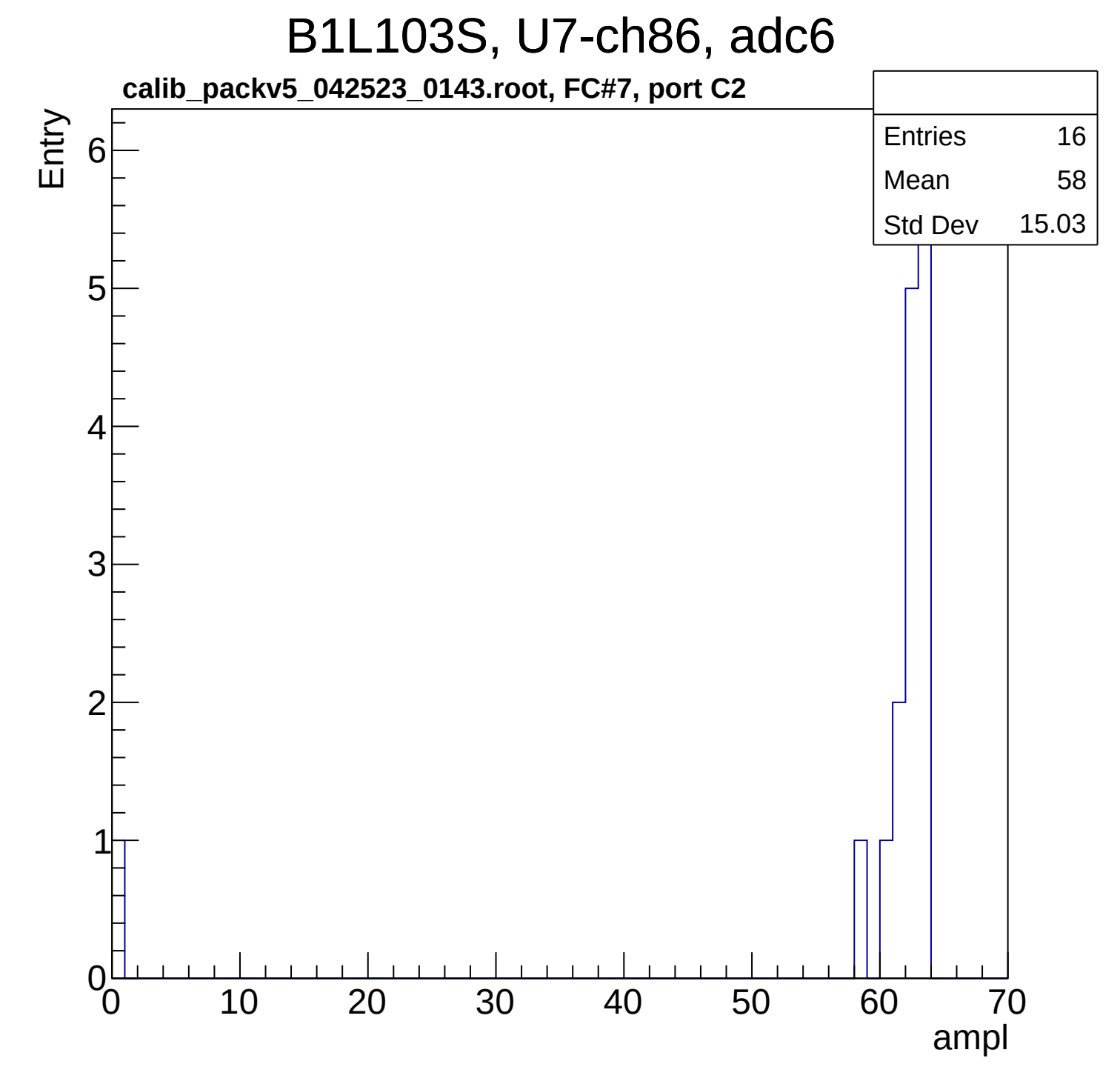
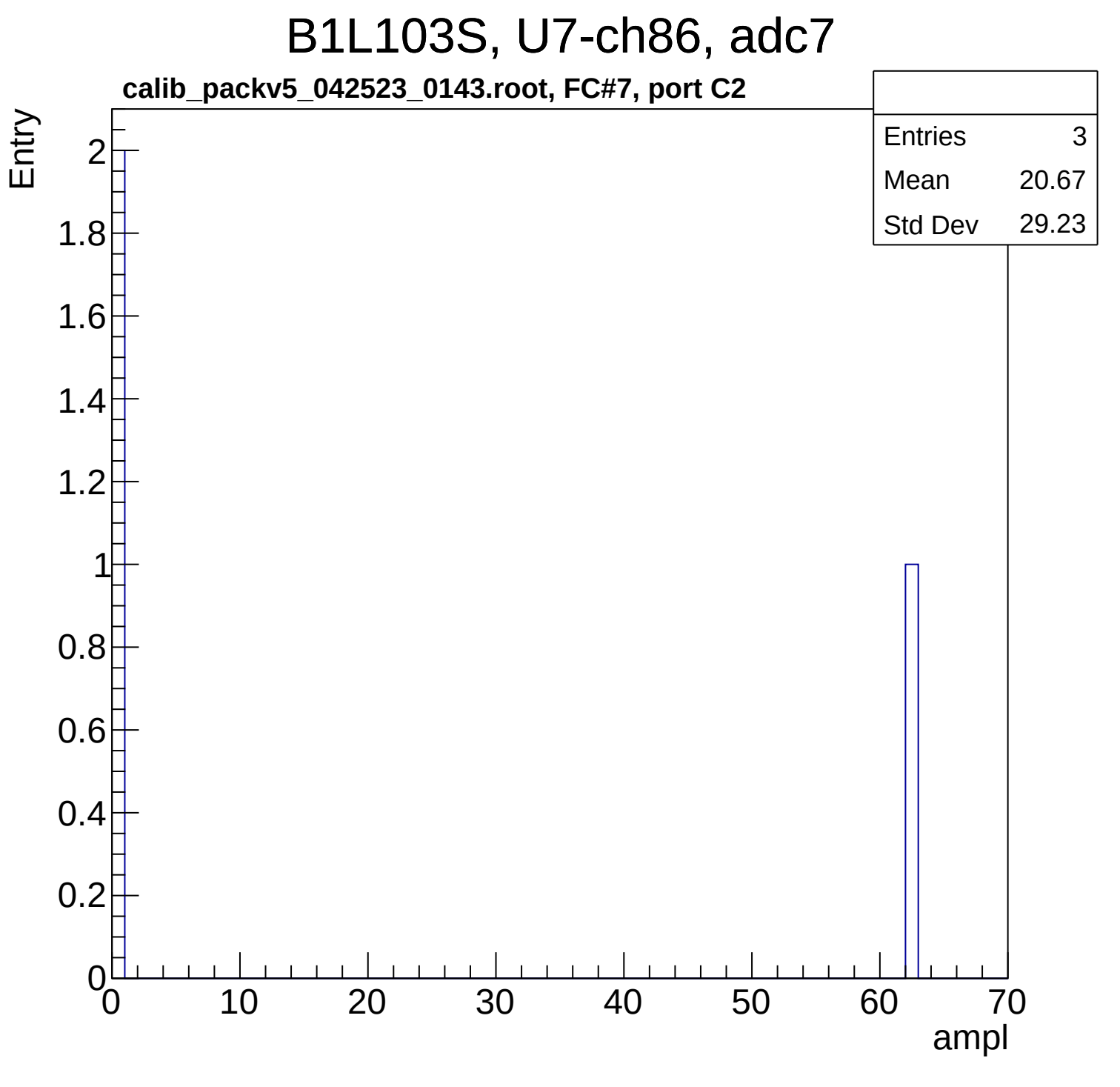
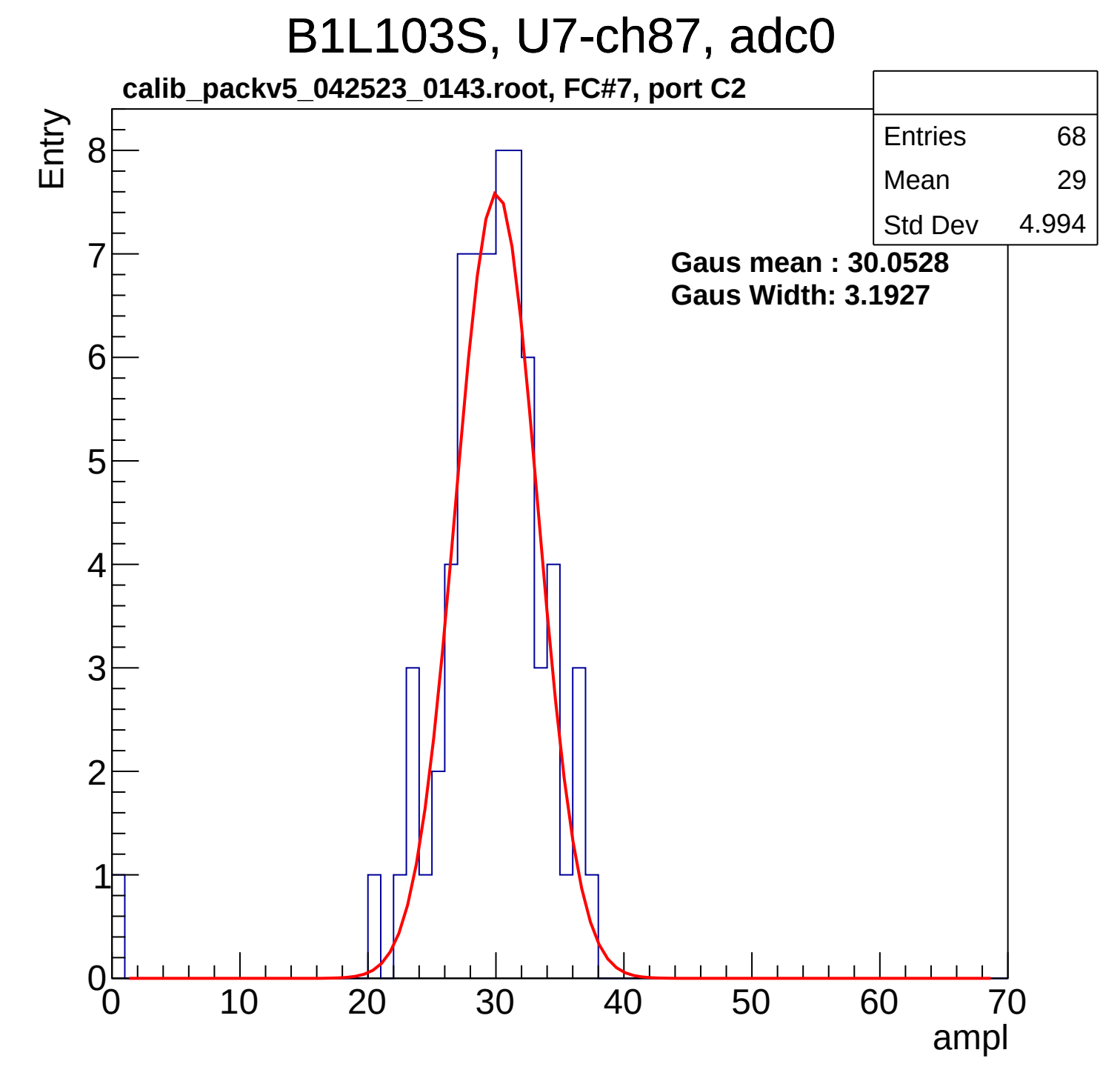
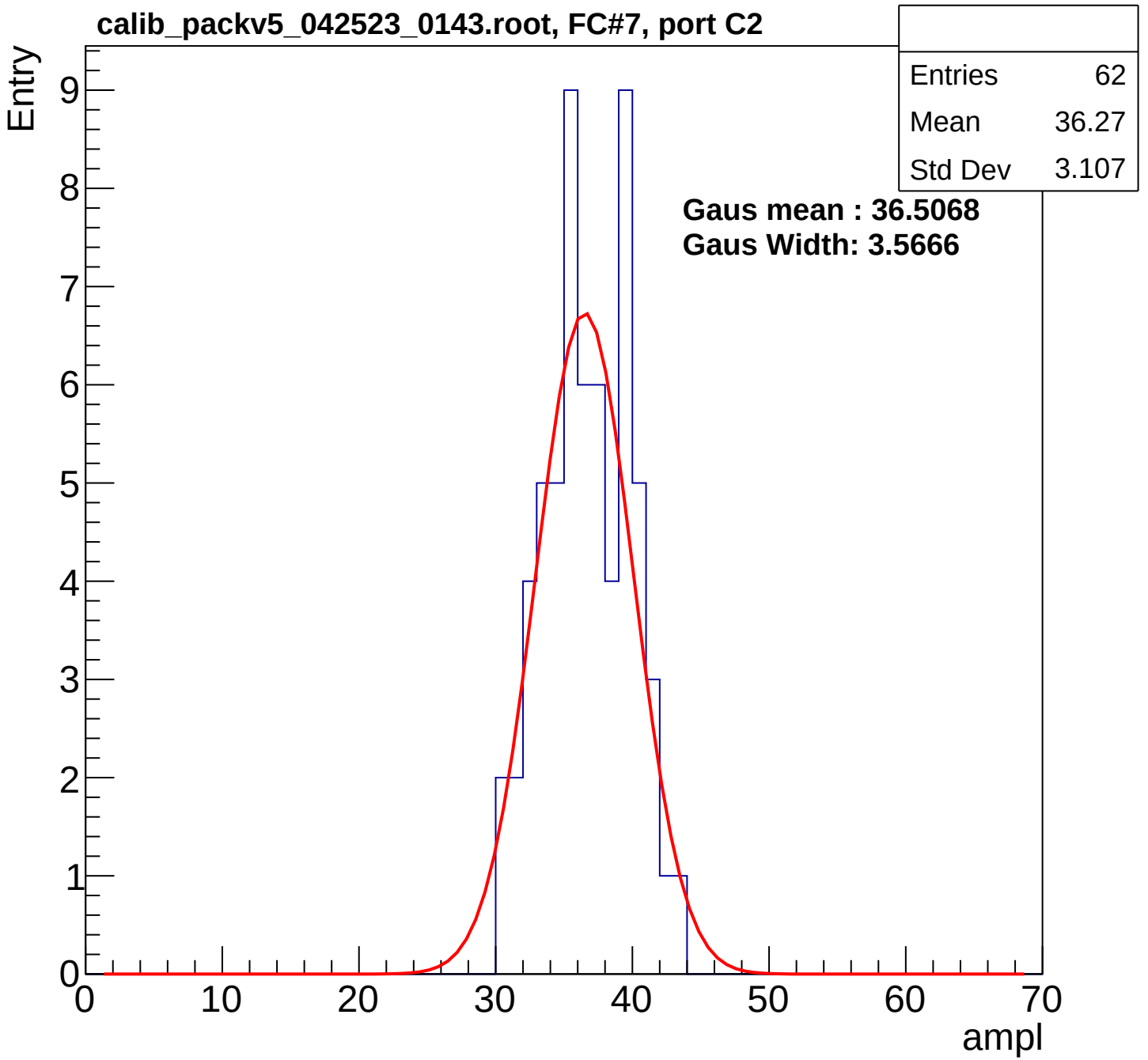
50
60
70
ampl


B1L103S, U7-ch86, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 16
Mean 58
Std Dev 15.03
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch86, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 20.67
Std Dev 29.23
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U7-ch87, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 29
Std Dev 4.994
Gaus mean : 30.0528
Gaus Width: 3.1927
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch87, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 62
Mean 36.27
Std Dev 3.107
Gaus mean : 36.5068
Gaus Width: 3.5666
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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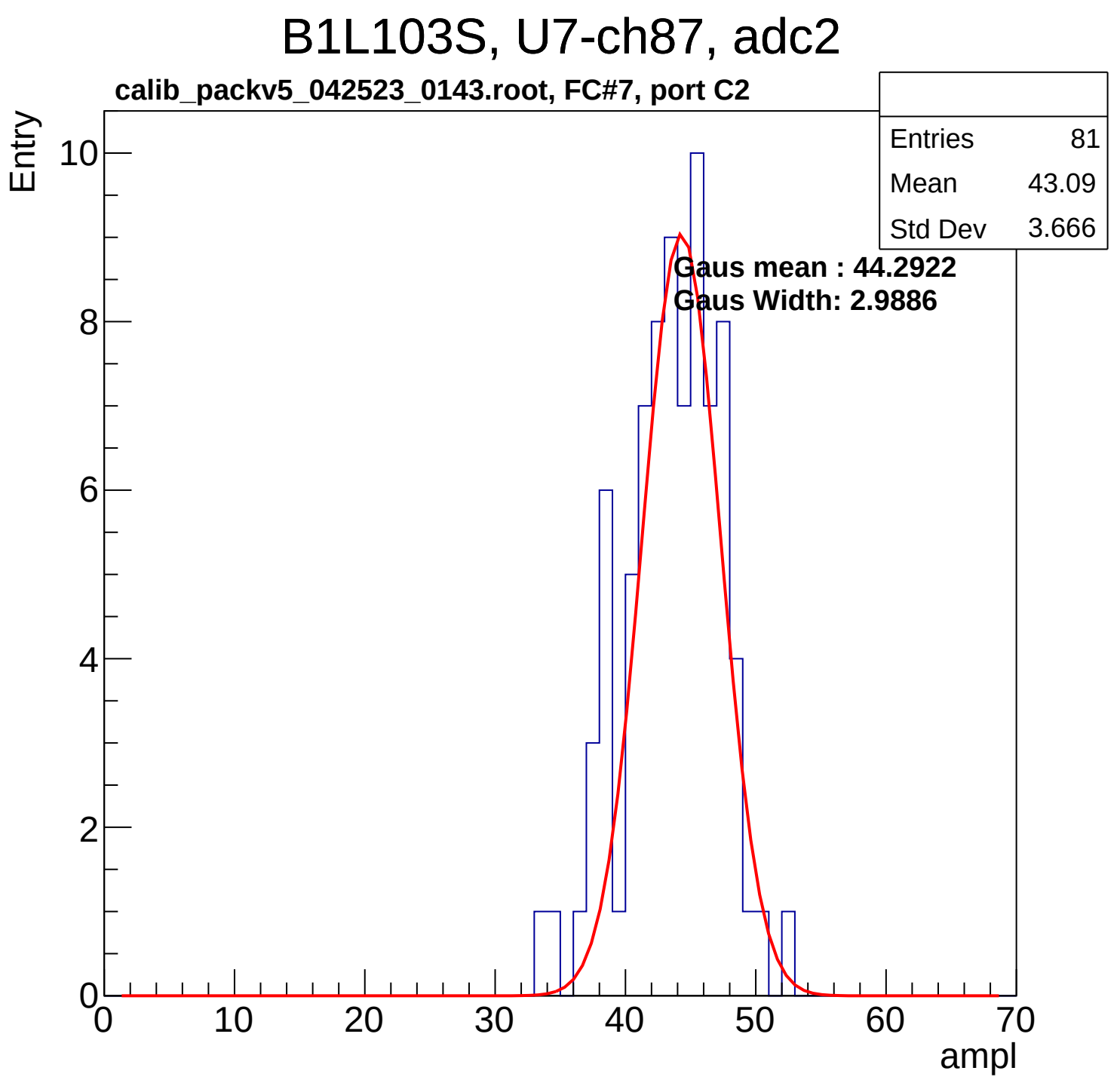
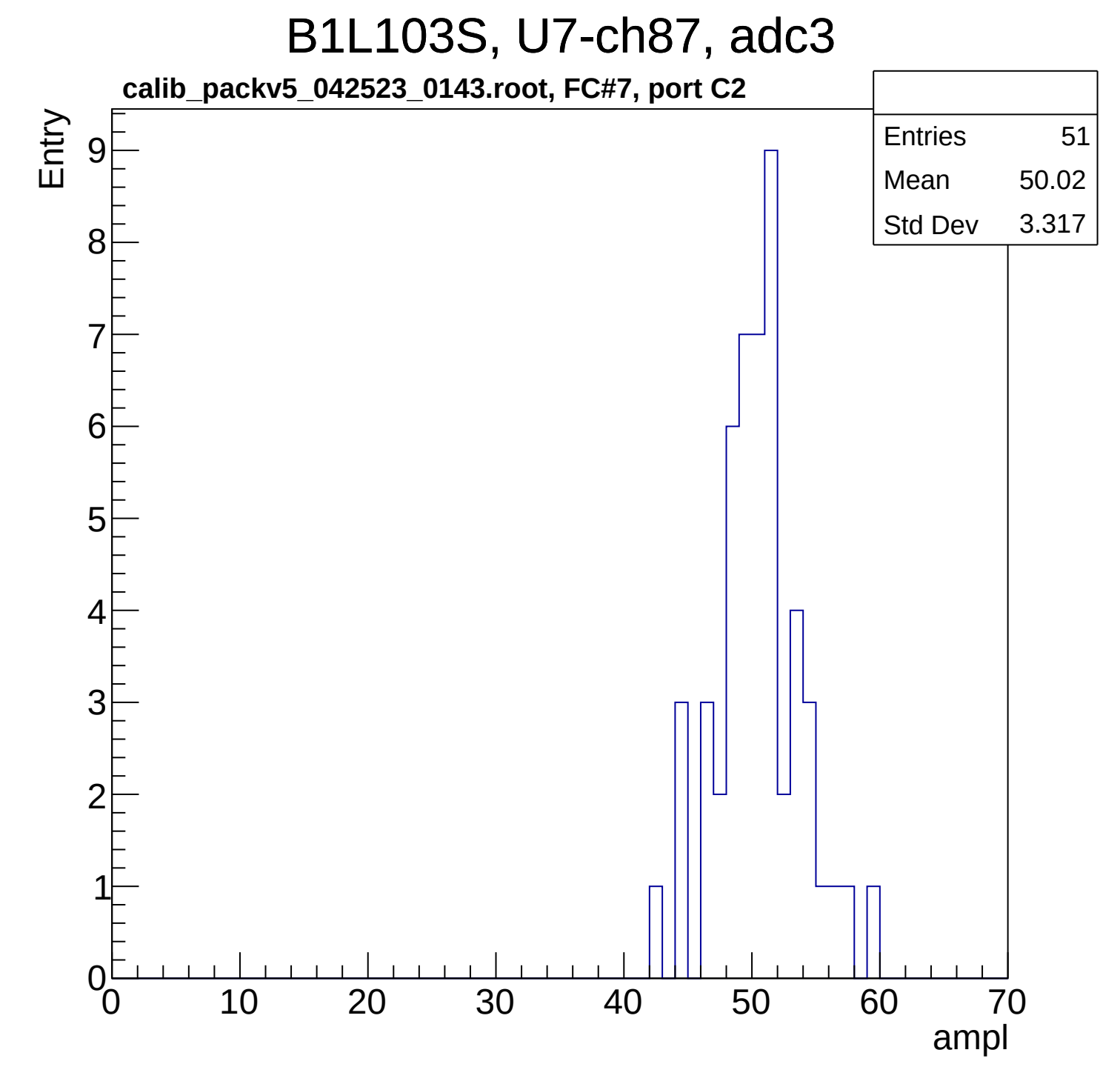
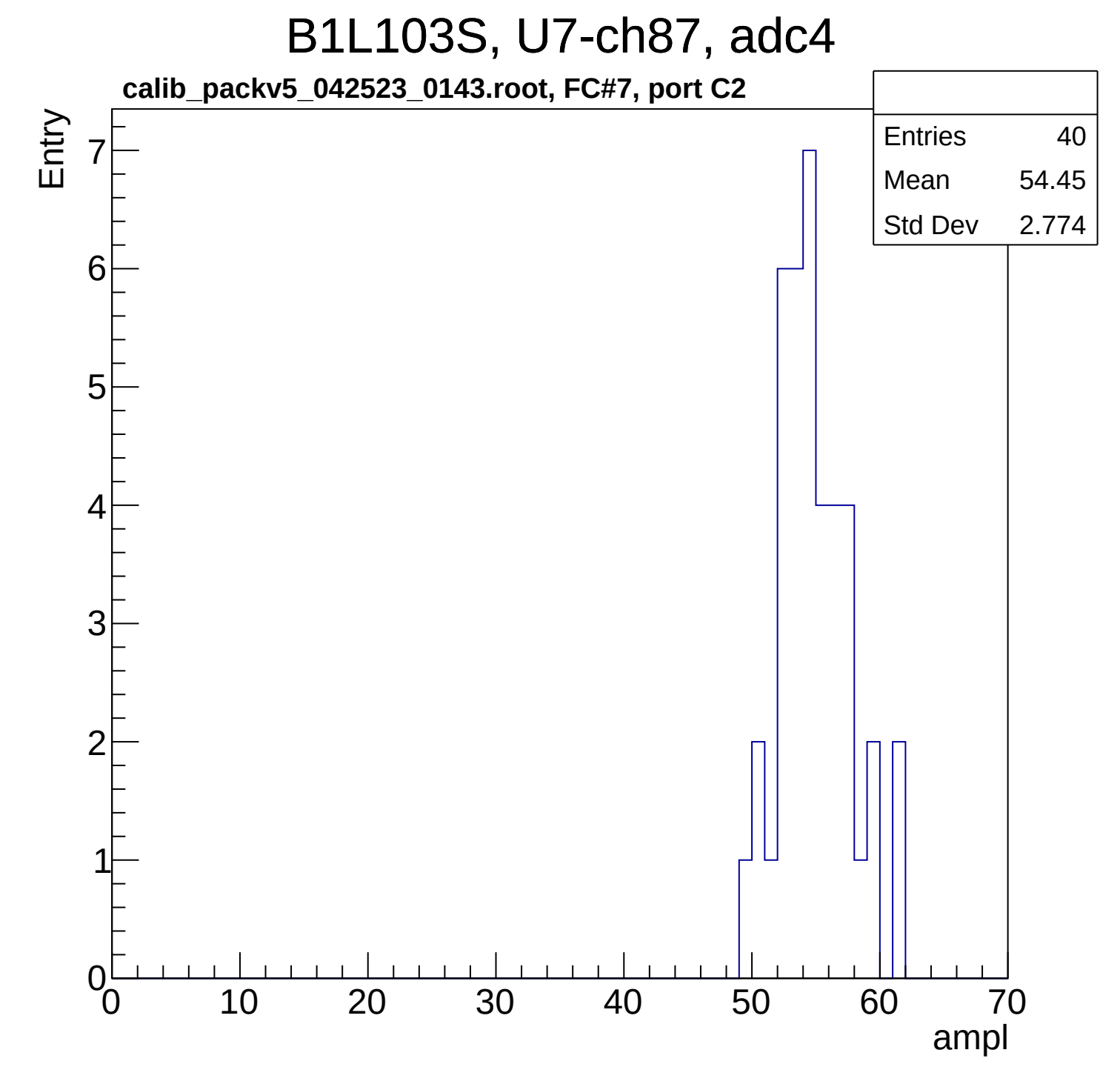
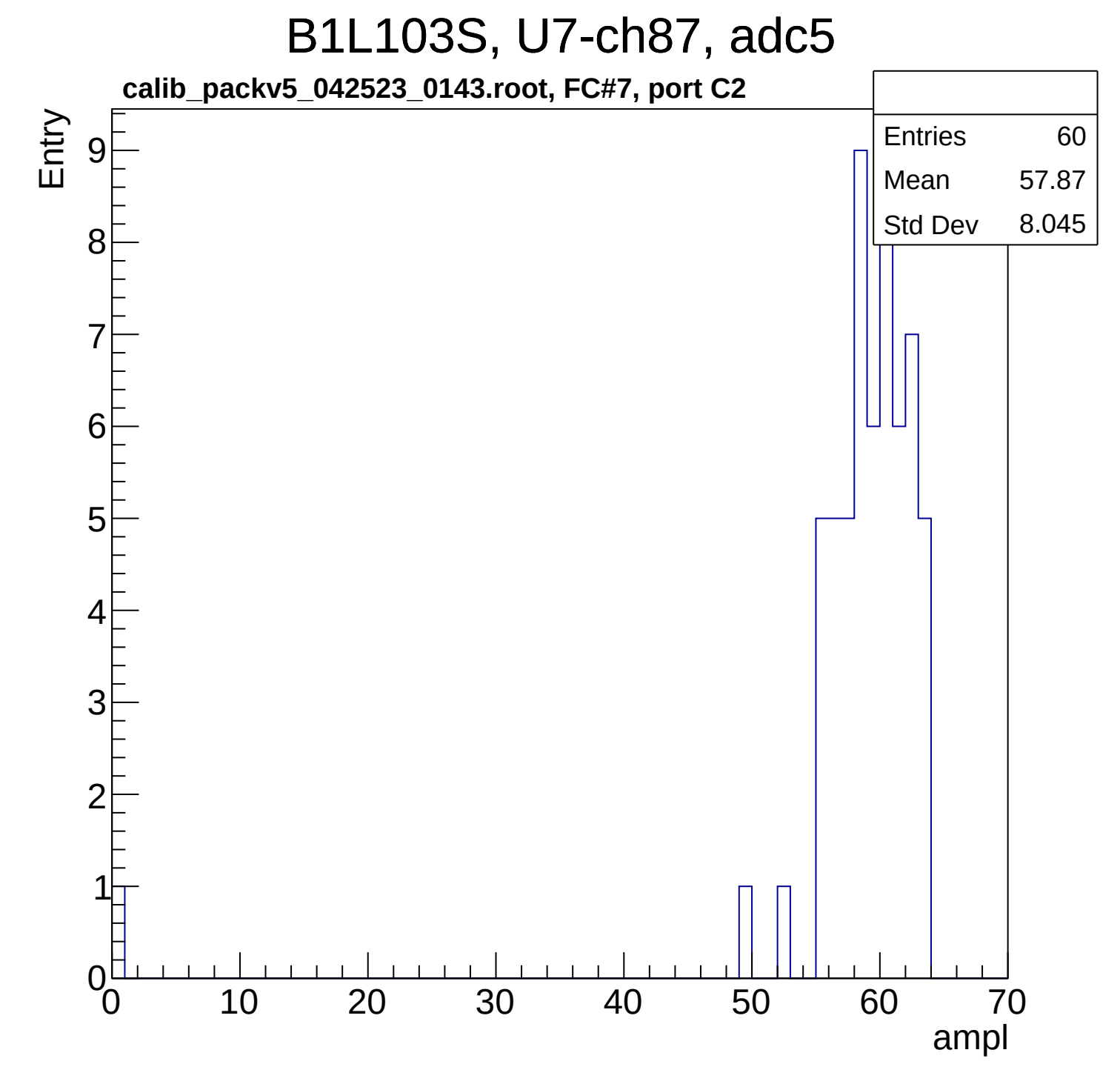
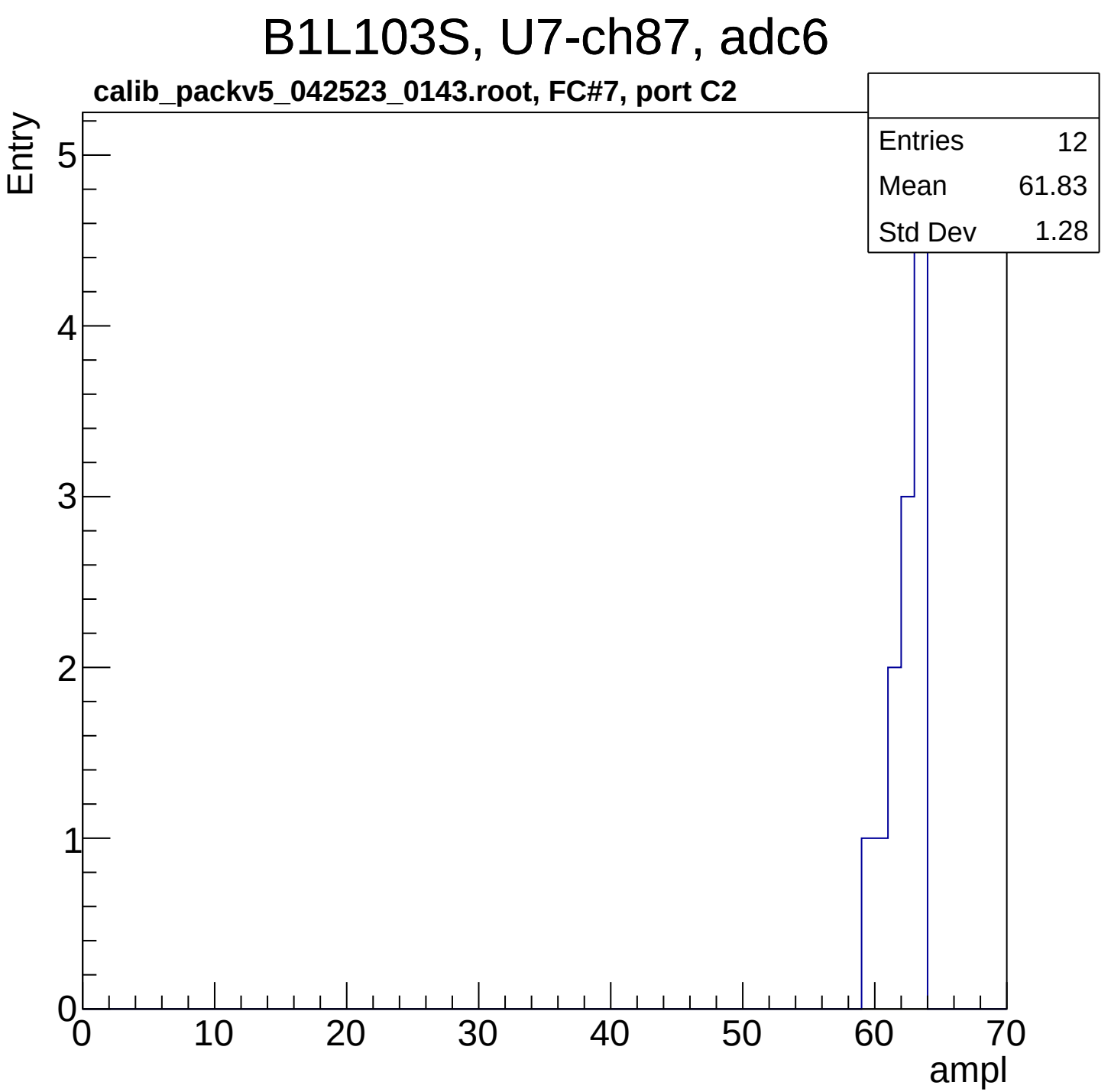
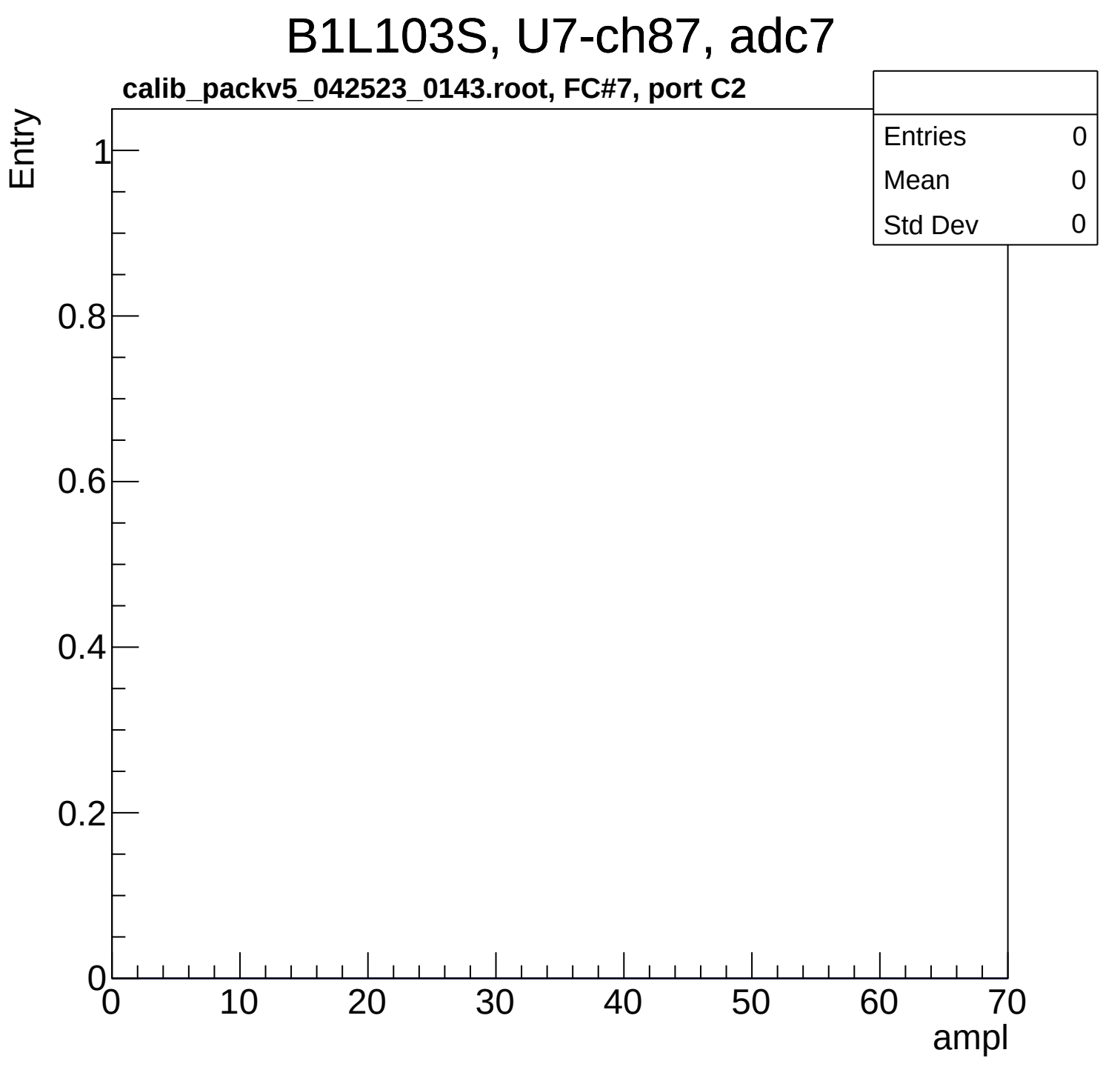

B1L103S, U7-ch87, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 81
Mean 43.09
Std Dev 3.666
Gaus mean : 44.2922
Gaus Width: 2.9886
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch87, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 51
Mean 50.02
Std Dev 3.317
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch87, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 40
Mean 54.45
Std Dev 2.774
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch87, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 60
Mean 57.87
Std Dev 8.045
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch87, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 12
Mean 61.83
Std Dev 1.28
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch87, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
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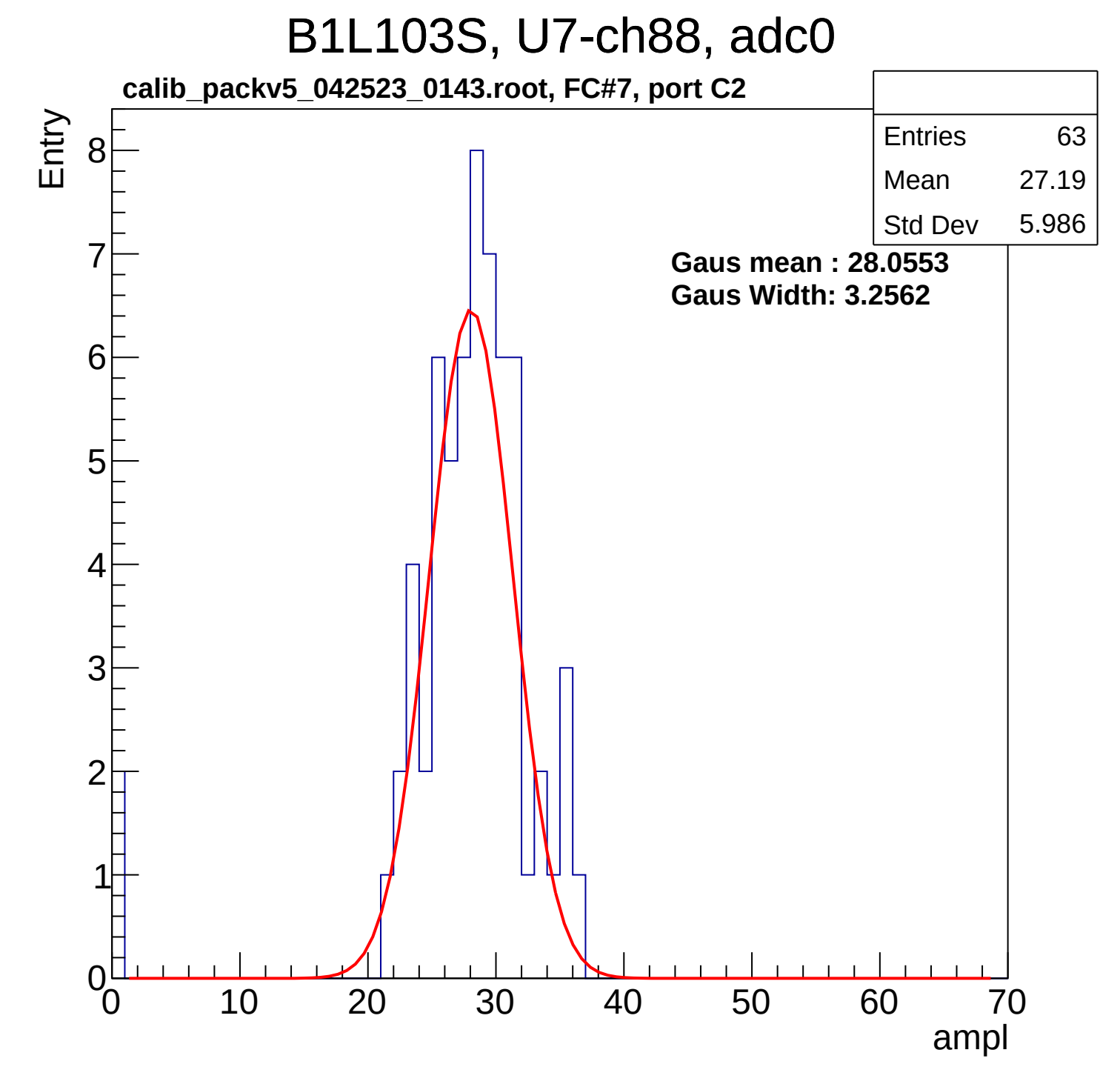
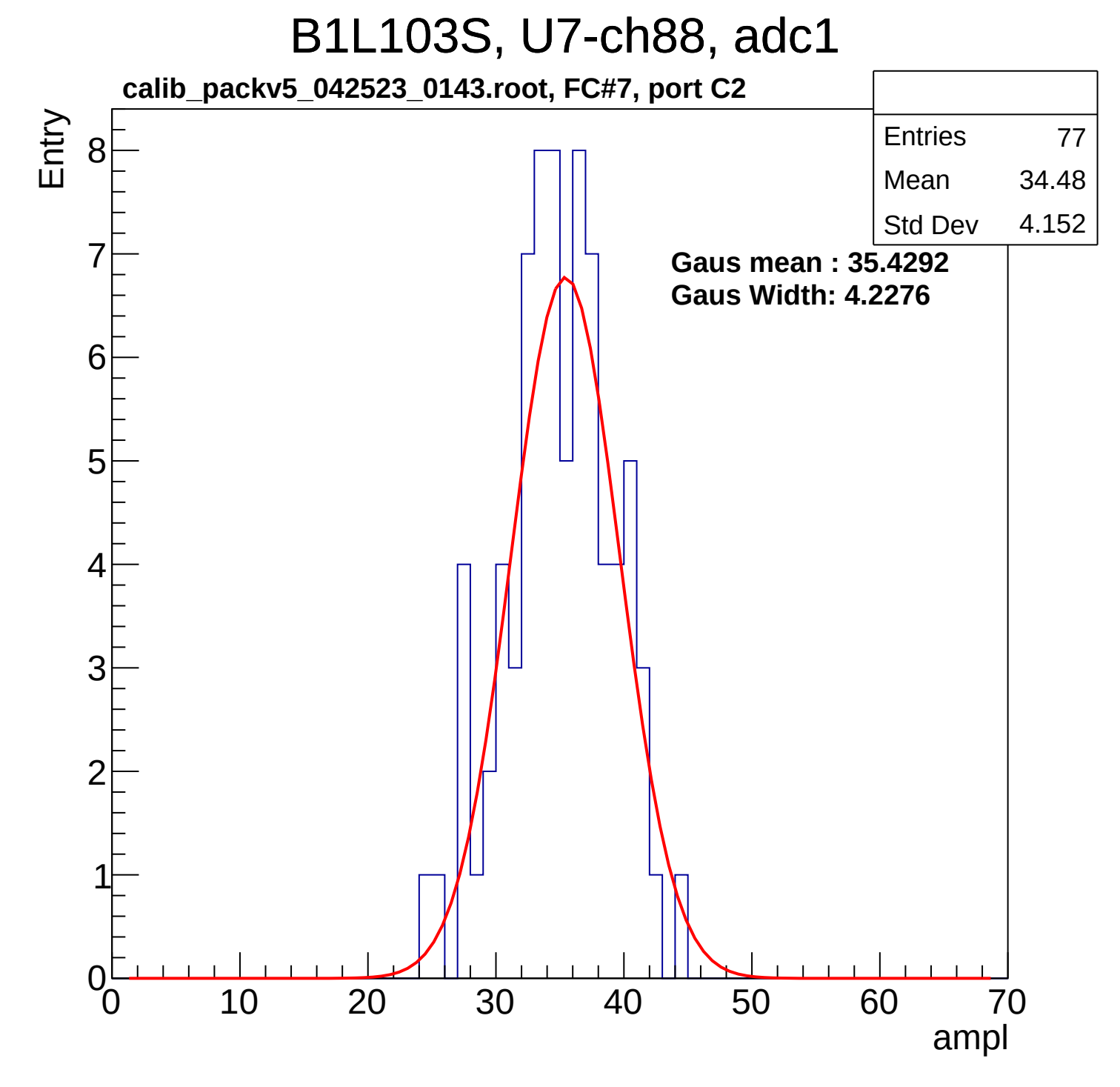
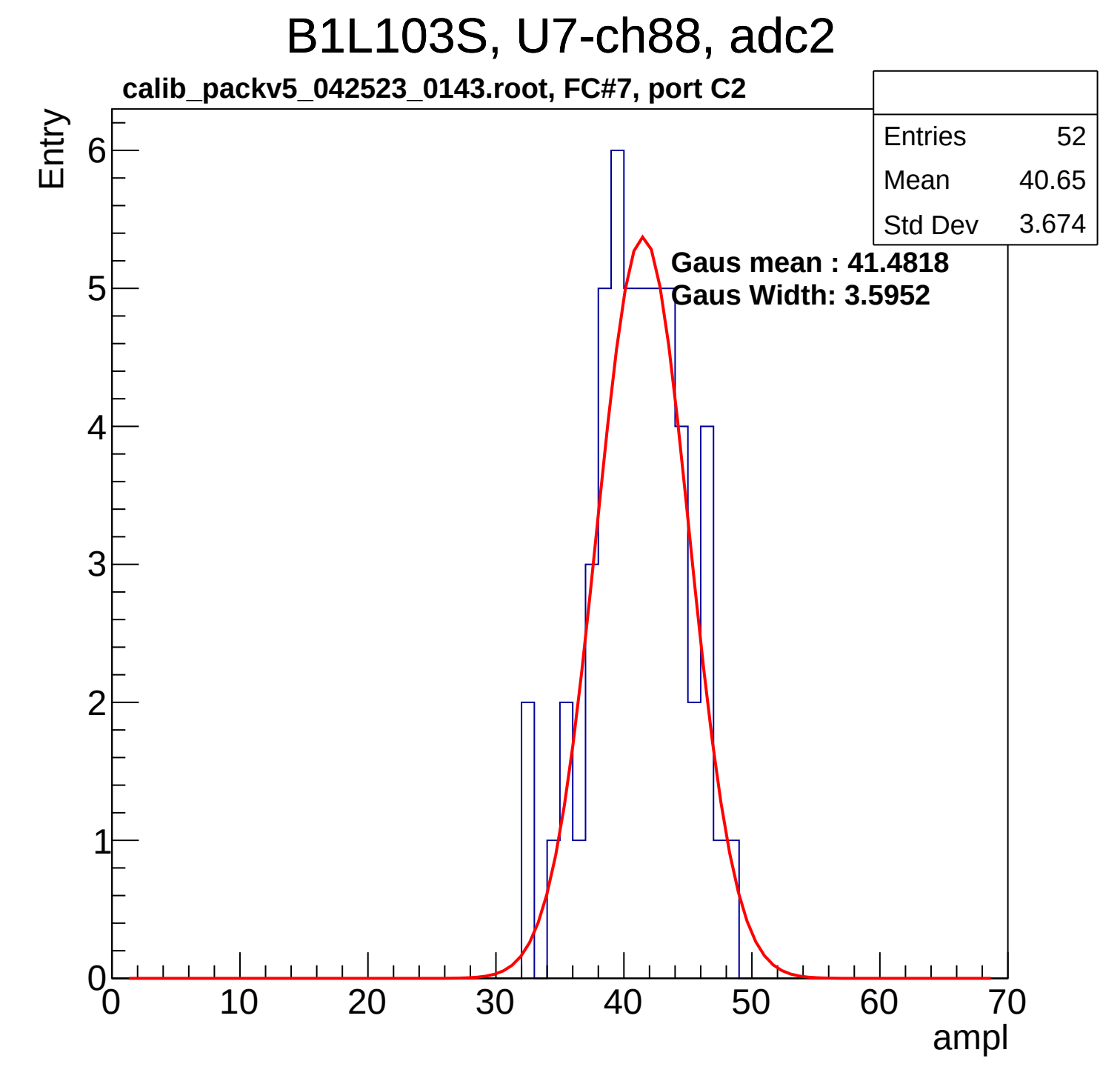
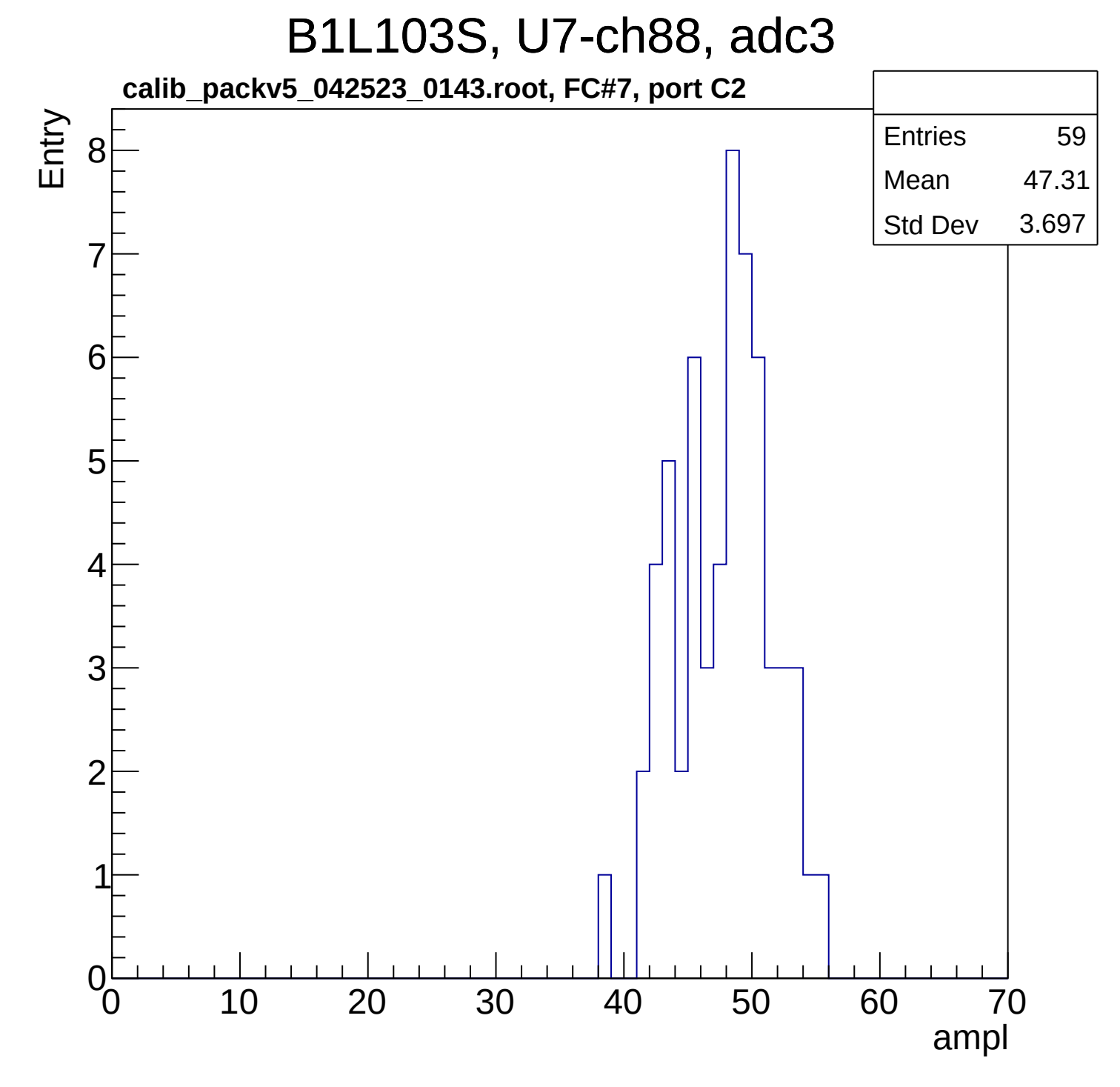
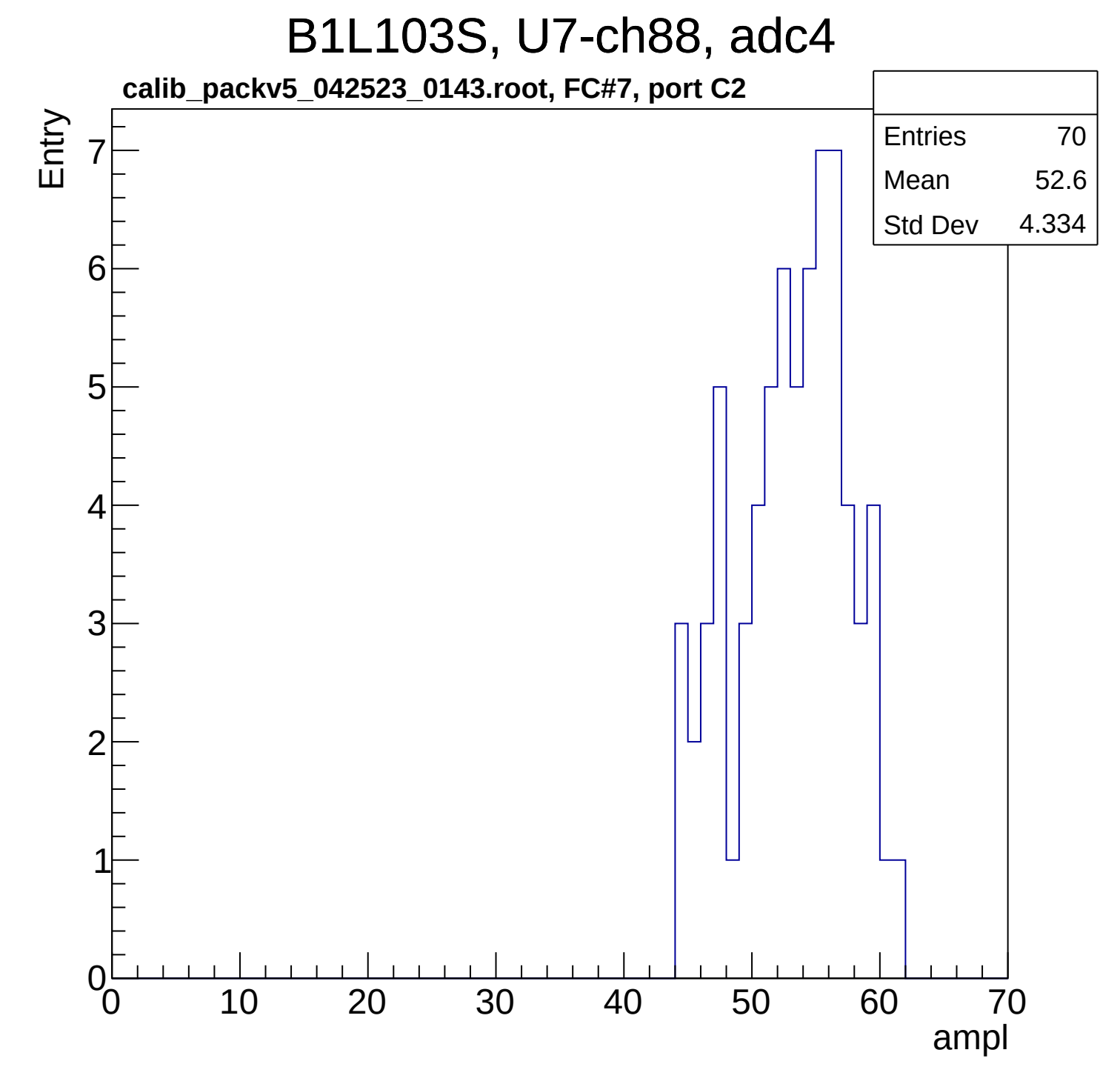
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

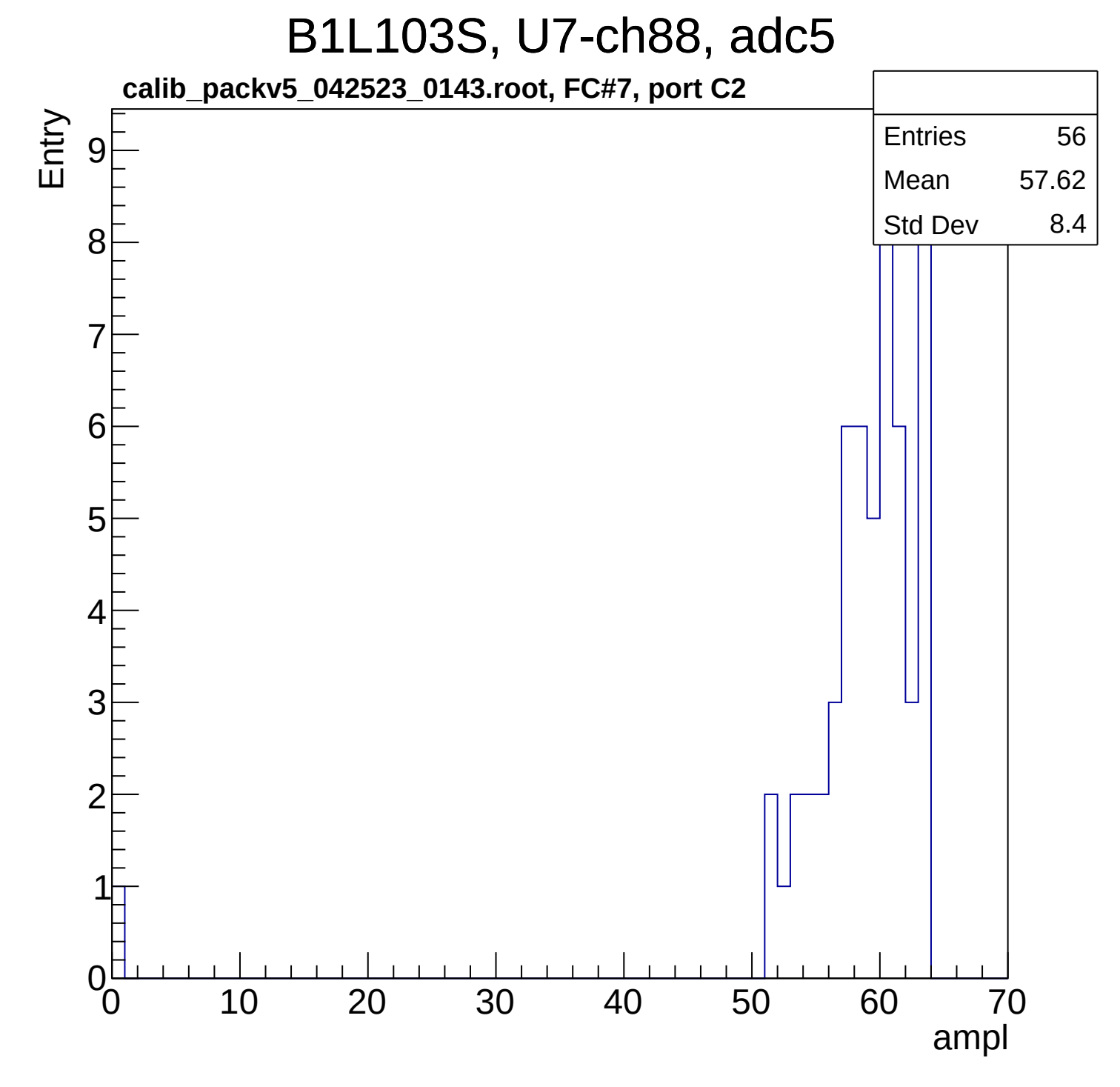

B1L103S, U7-ch88, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 27.19
Std Dev 5.986
Gaus mean : 28.0553
Gaus Width: 3.2562
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch88, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 77
Mean 34.48
Std Dev 4.152
Gaus mean : 35.4292
Gaus Width: 4.2276
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch88, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 52
Mean 40.65
Std Dev 3.674
Gaus mean : 41.4818
Gaus Width: 3.5952
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U7-ch88, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 47.31
Std Dev 3.697
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch88, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 52.6
Std Dev 4.334
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch88, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 57.62
Std Dev 8.4
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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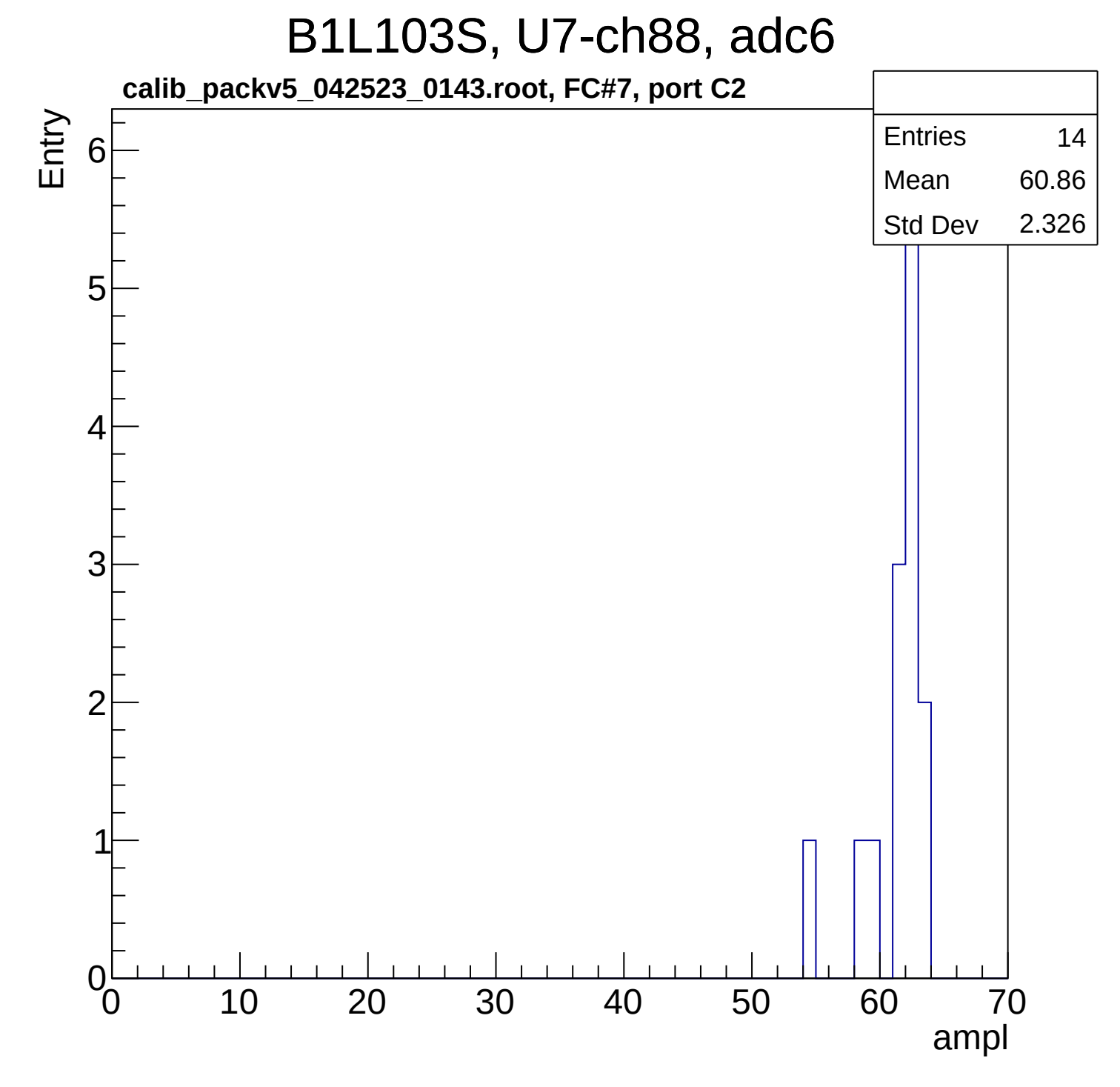
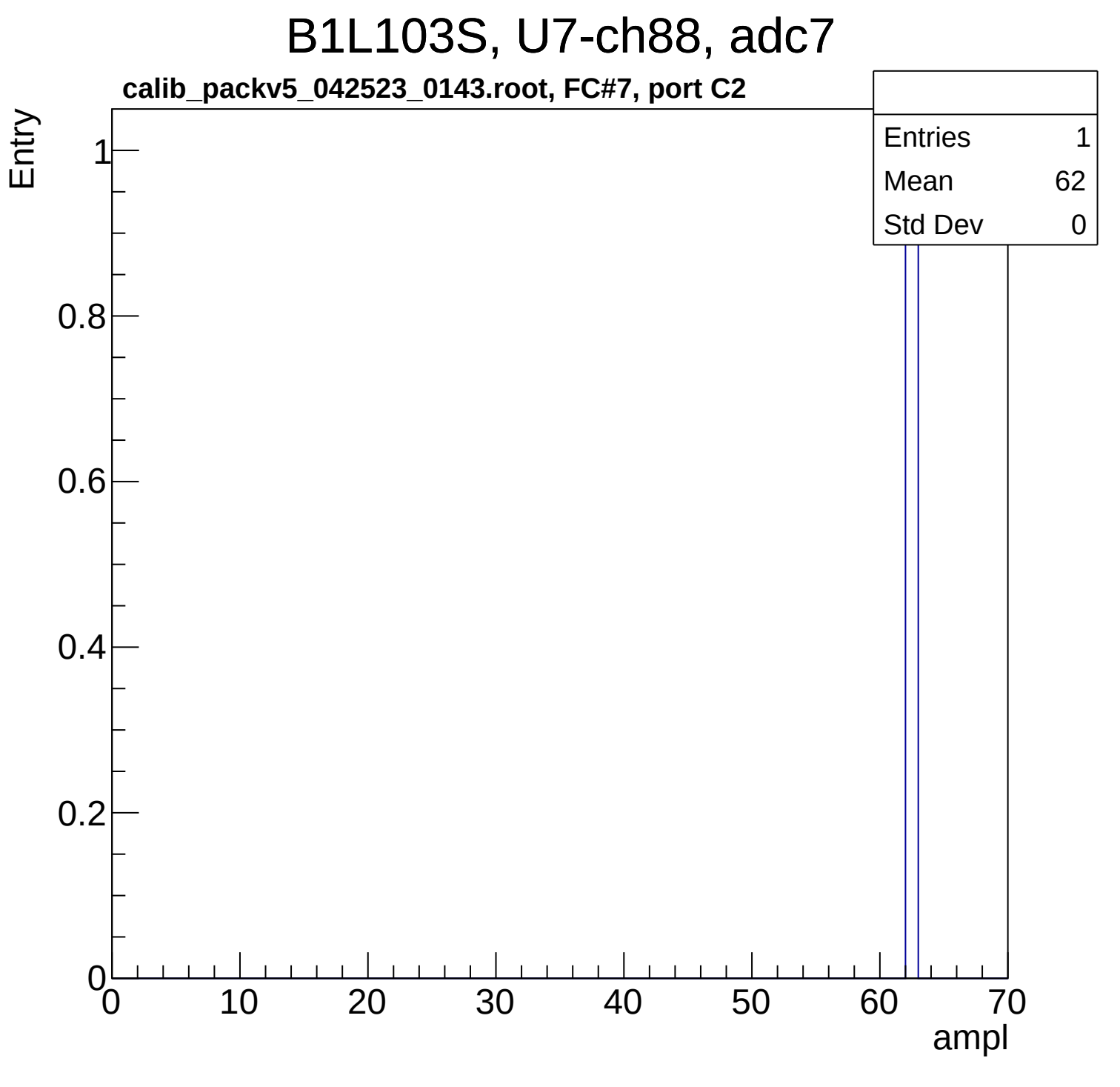
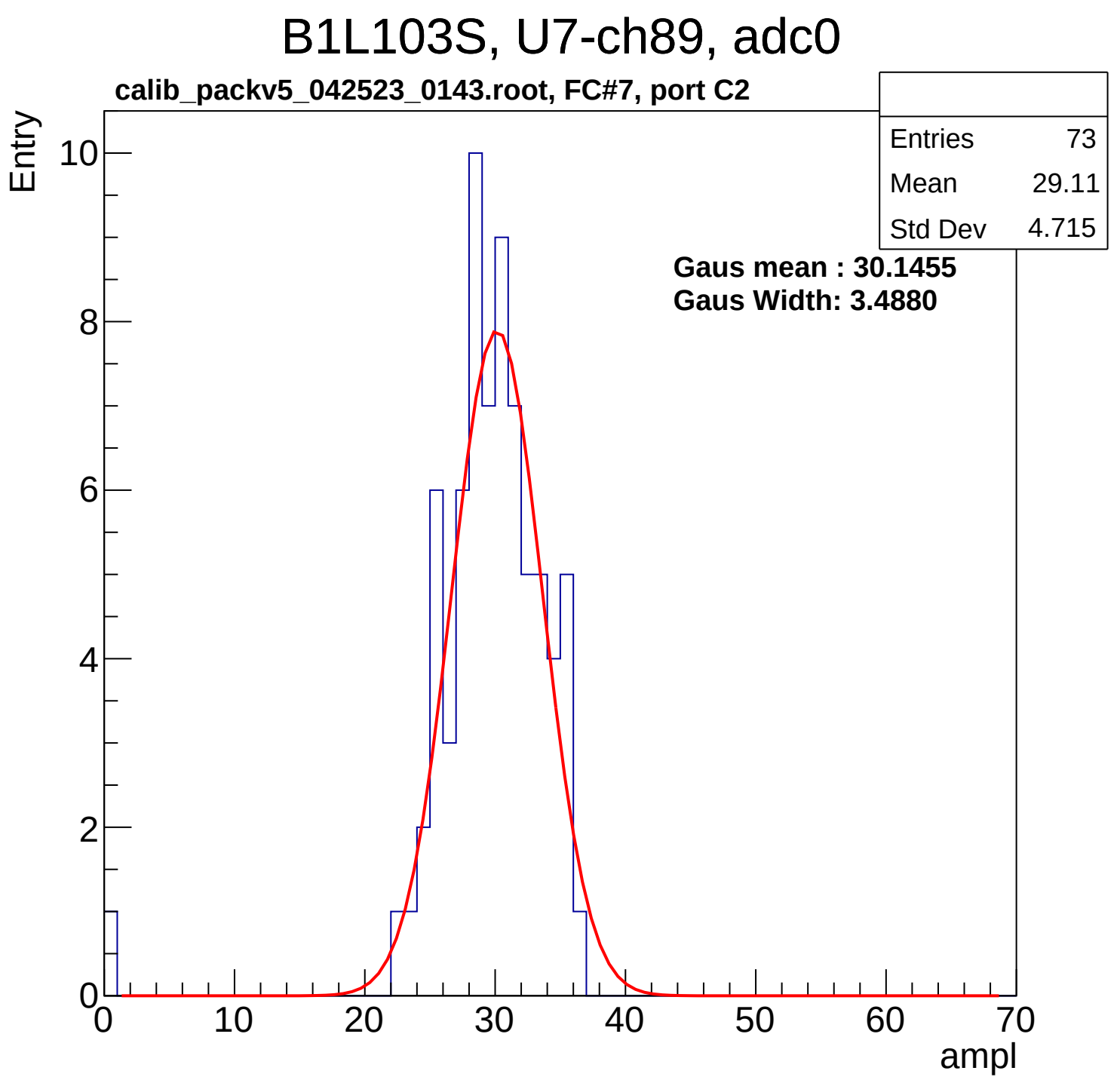
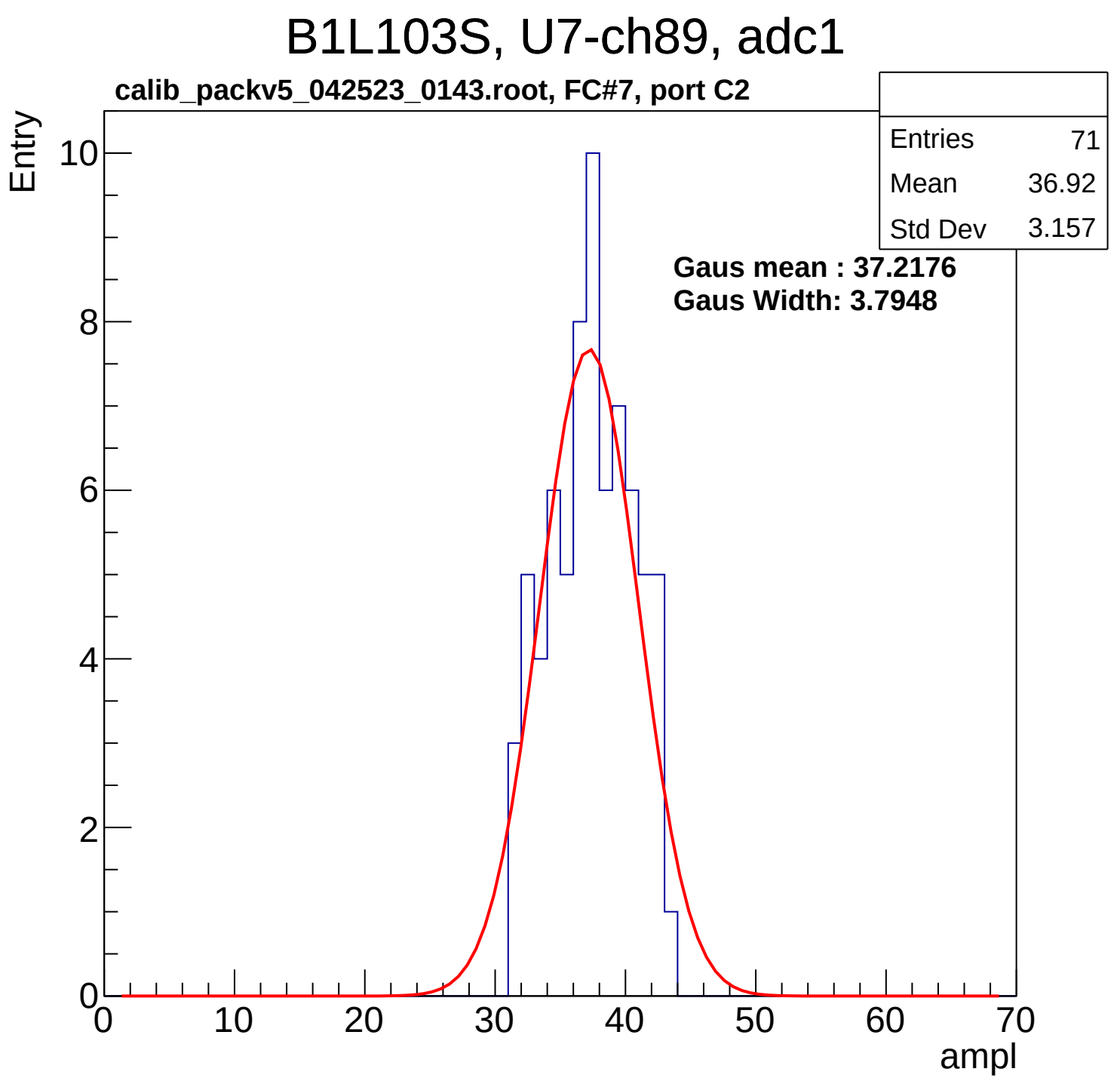
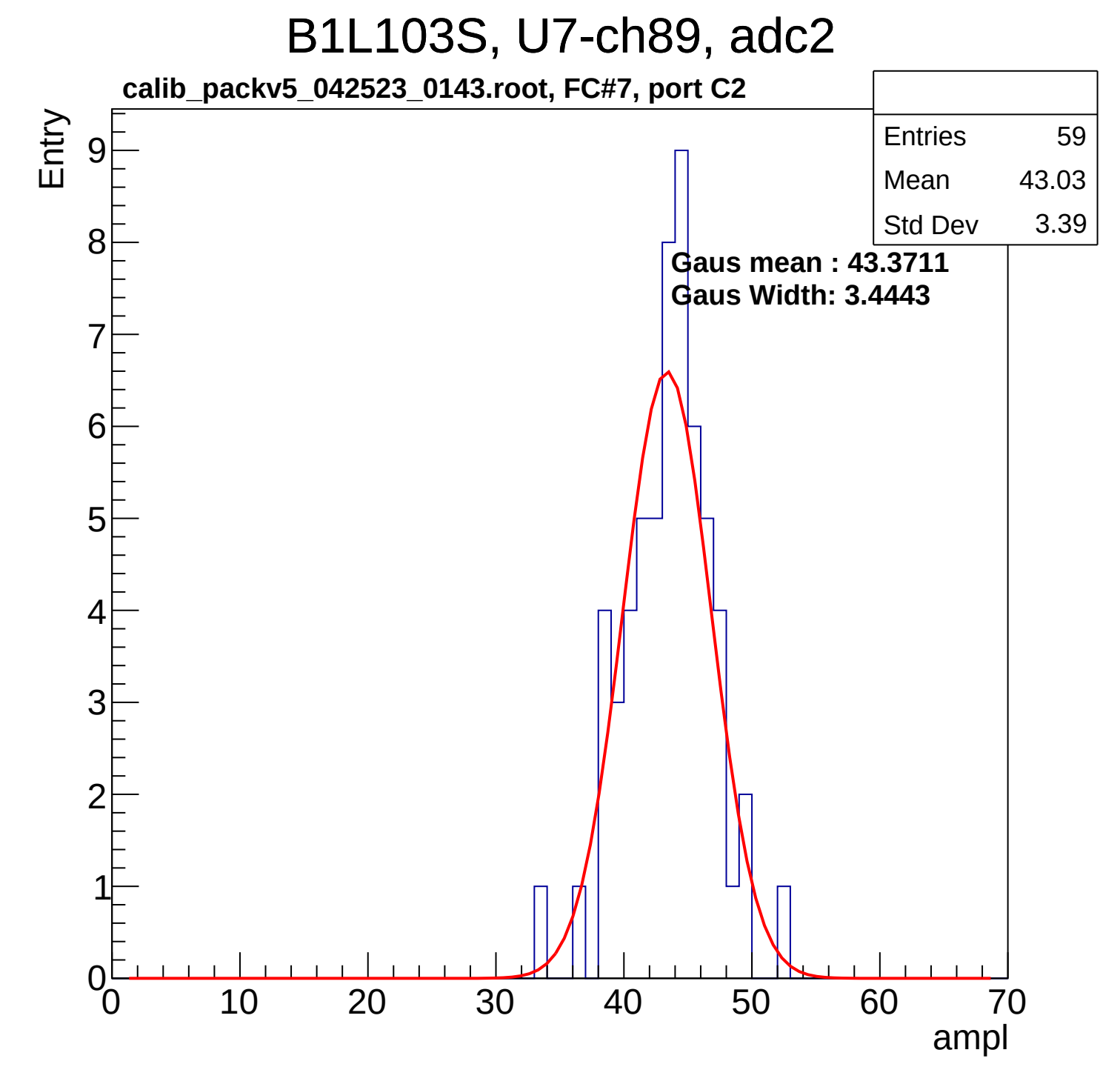
40
50
60
70


B1L103S, U7-ch88, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 14
Mean 60.86
Std Dev 2.326
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U7-ch88, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 62
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch89, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 73
Mean 29.11
Std Dev 4.715
Gaus mean : 30.1455
Gaus Width: 3.4880
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch89, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 71
Mean 36.92
Std Dev 3.157
Gaus mean : 37.2176
Gaus Width: 3.7948
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch89, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 43.03
Std Dev 3.39
Gaus mean : 43.3711
Gaus Width: 3.4443
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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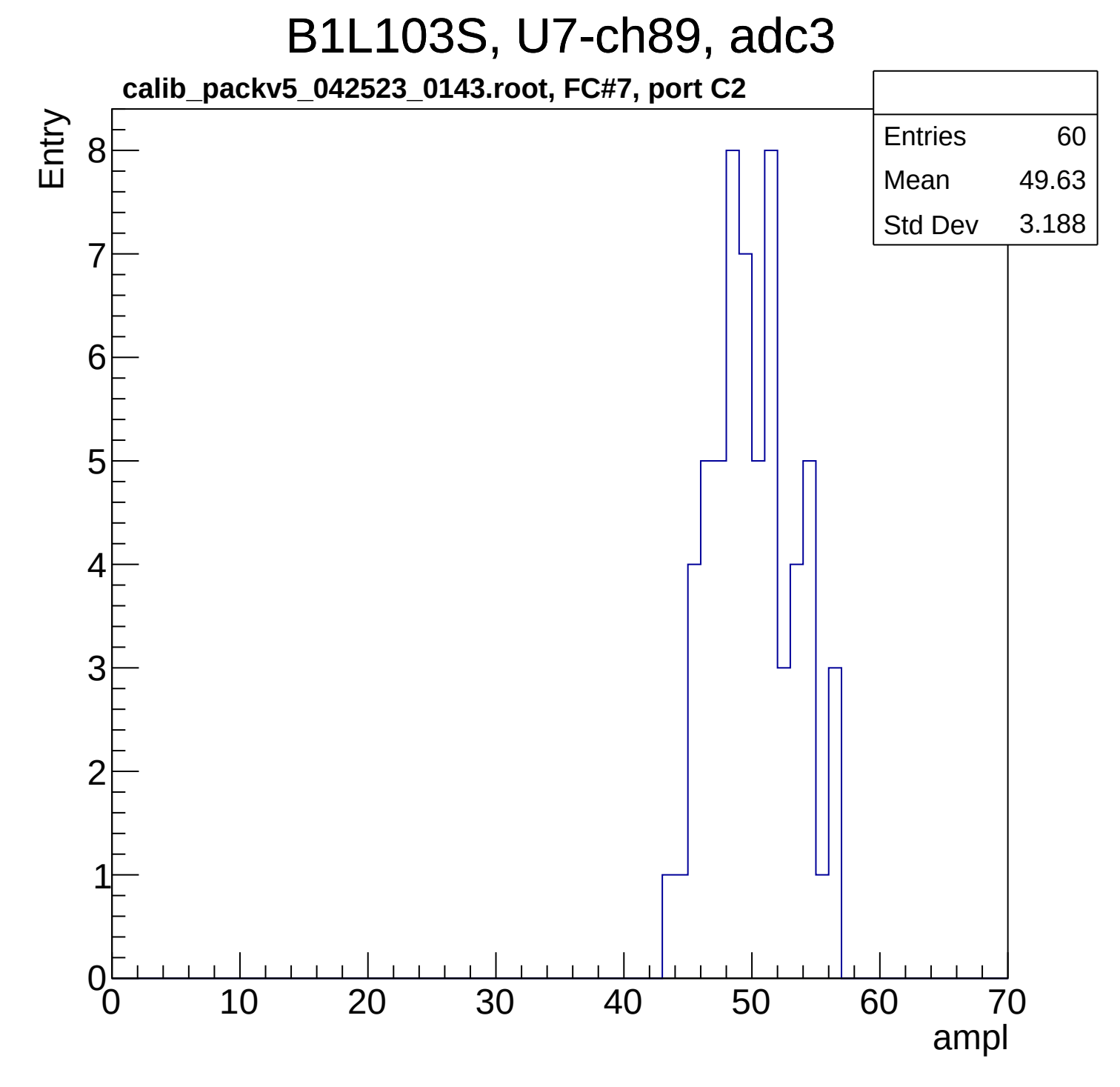
B1L103S, U7-ch89, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 60
Mean 49.63
Std Dev 3.188
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
50
60
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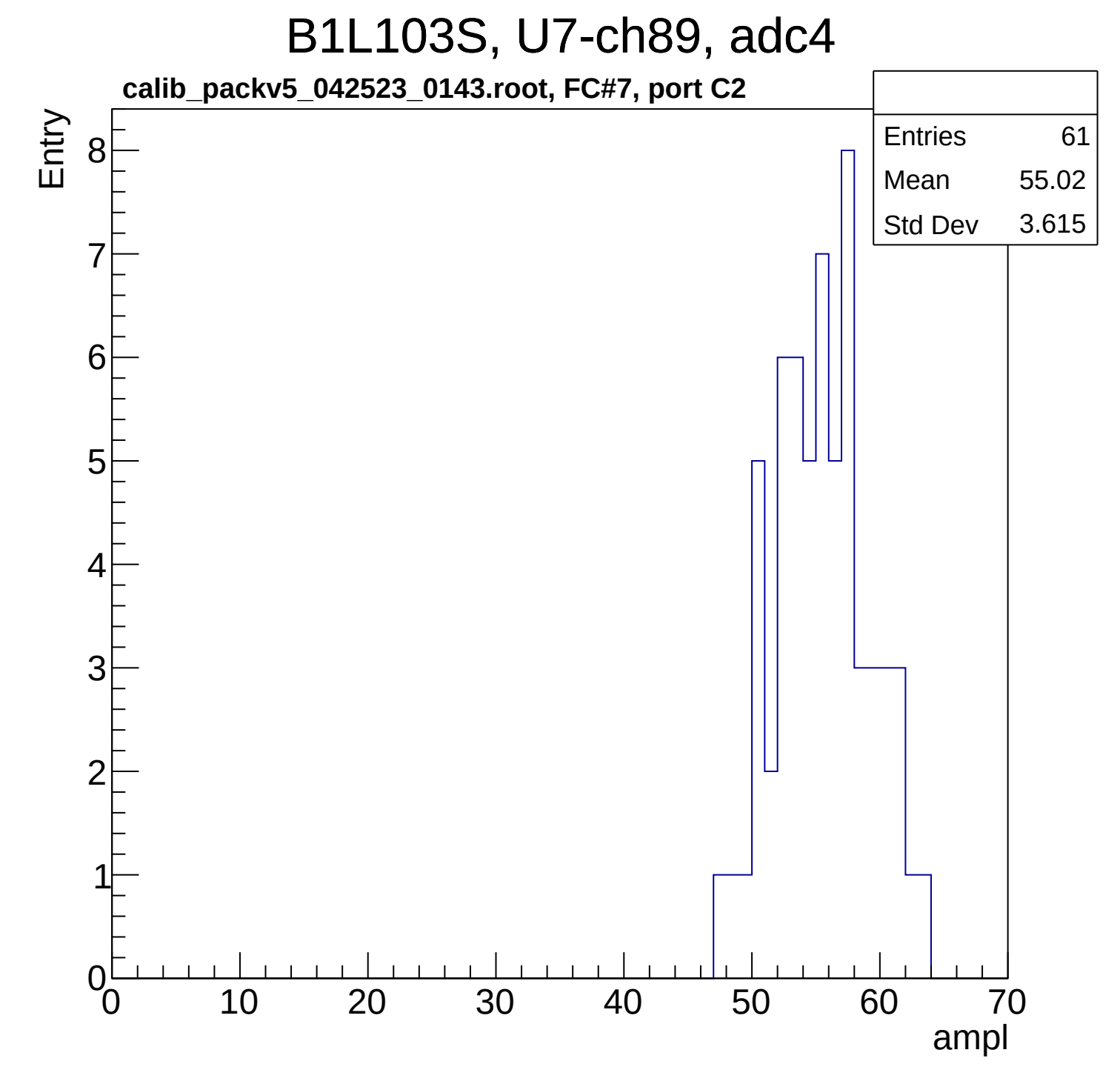
B1L103S, U7-ch89, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 61
Mean 55.02
Std Dev 3.615
Entry
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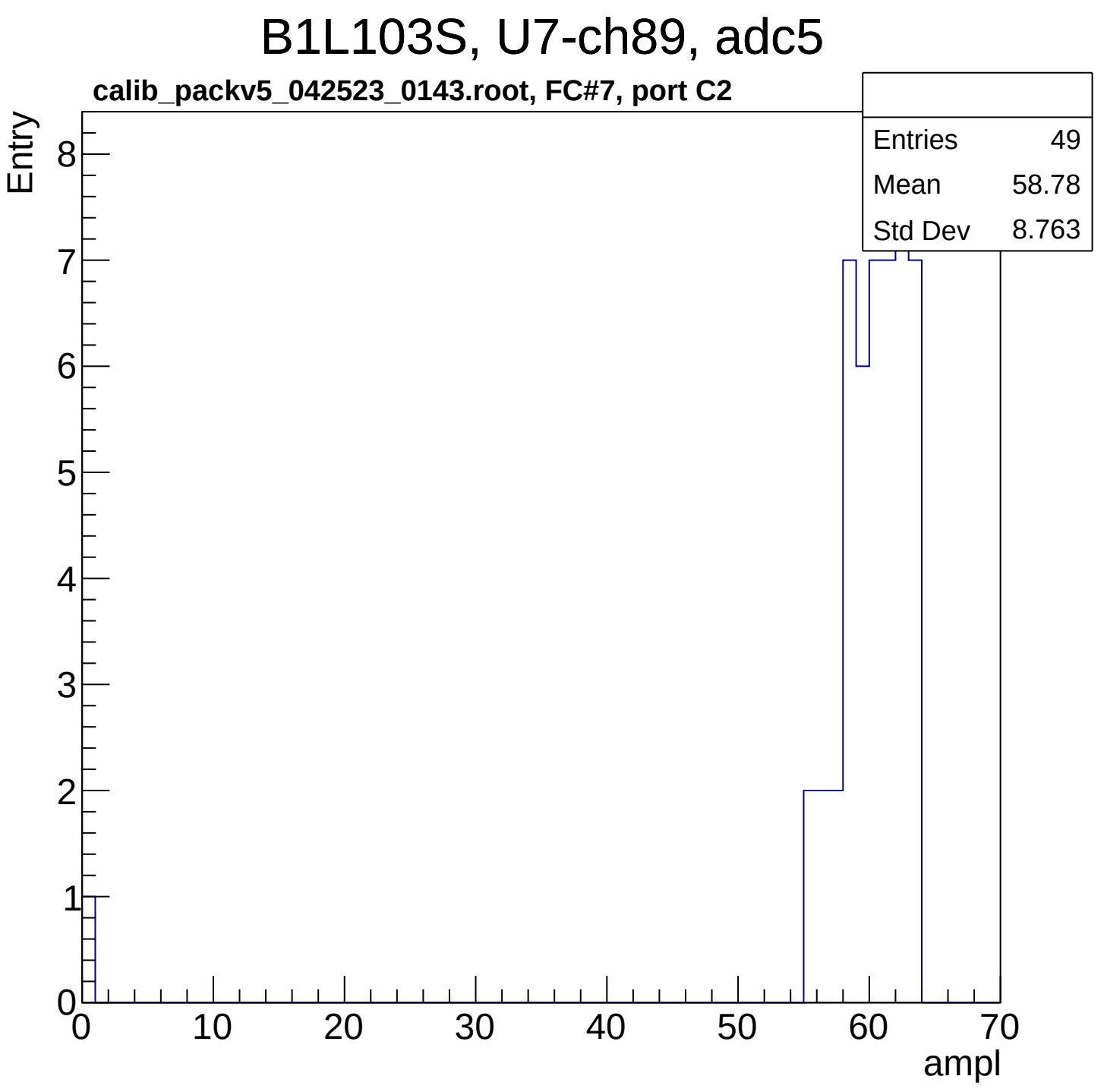
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch89, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 49
Mean 58.78
Std Dev 8.763
Entry
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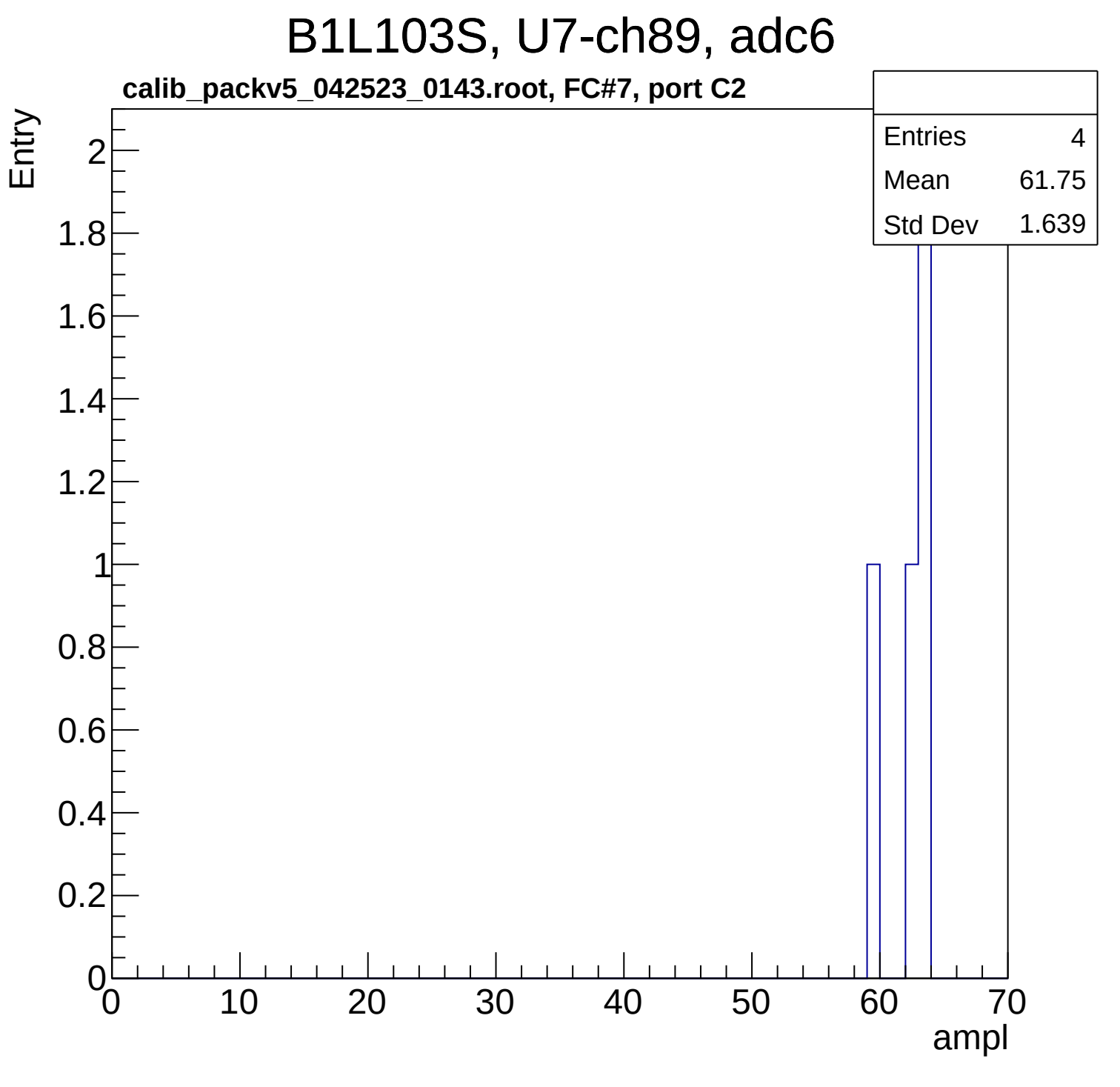
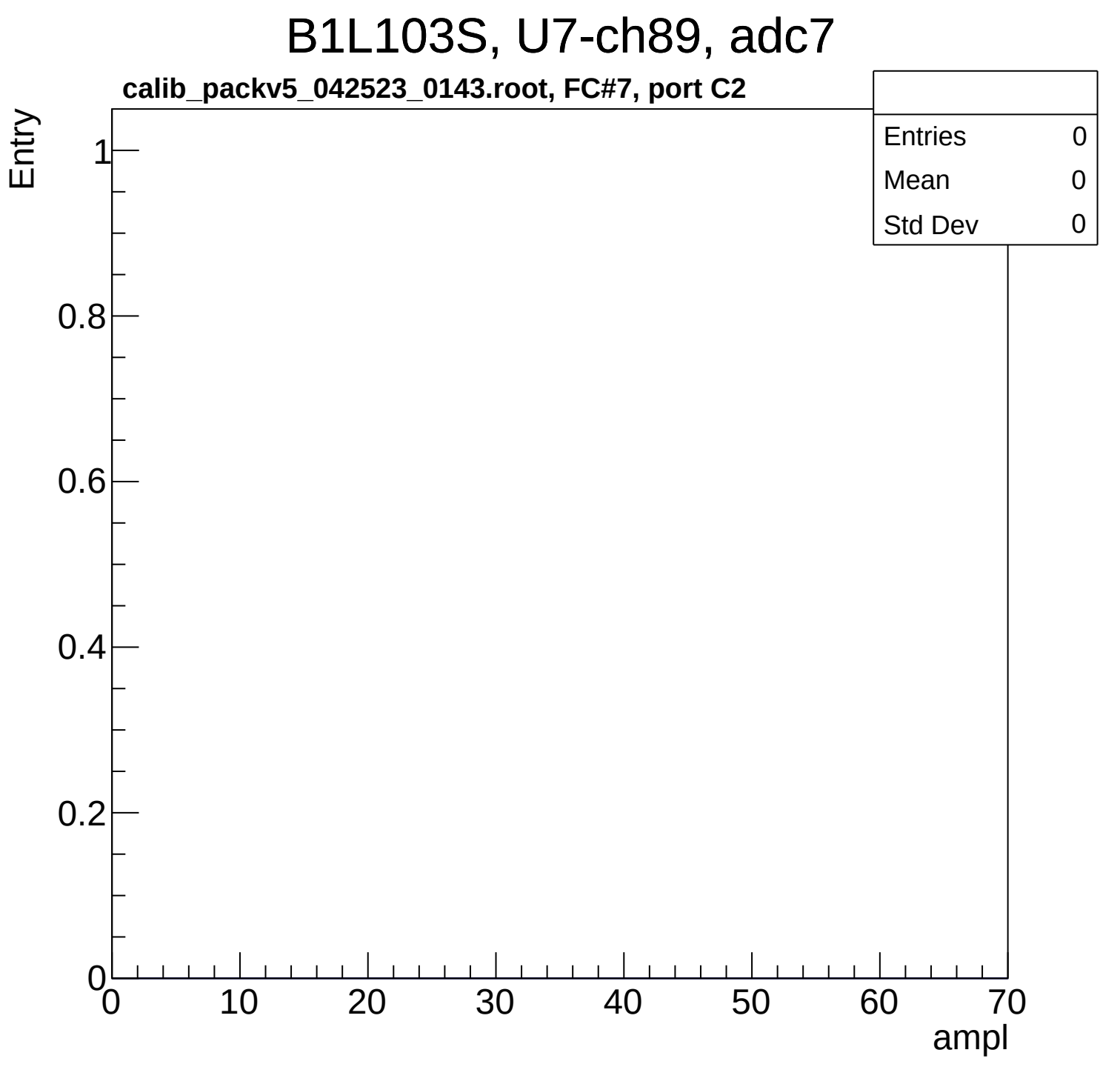
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch89, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 4
Mean 61.75
Std Dev 1.639
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U7-ch89, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
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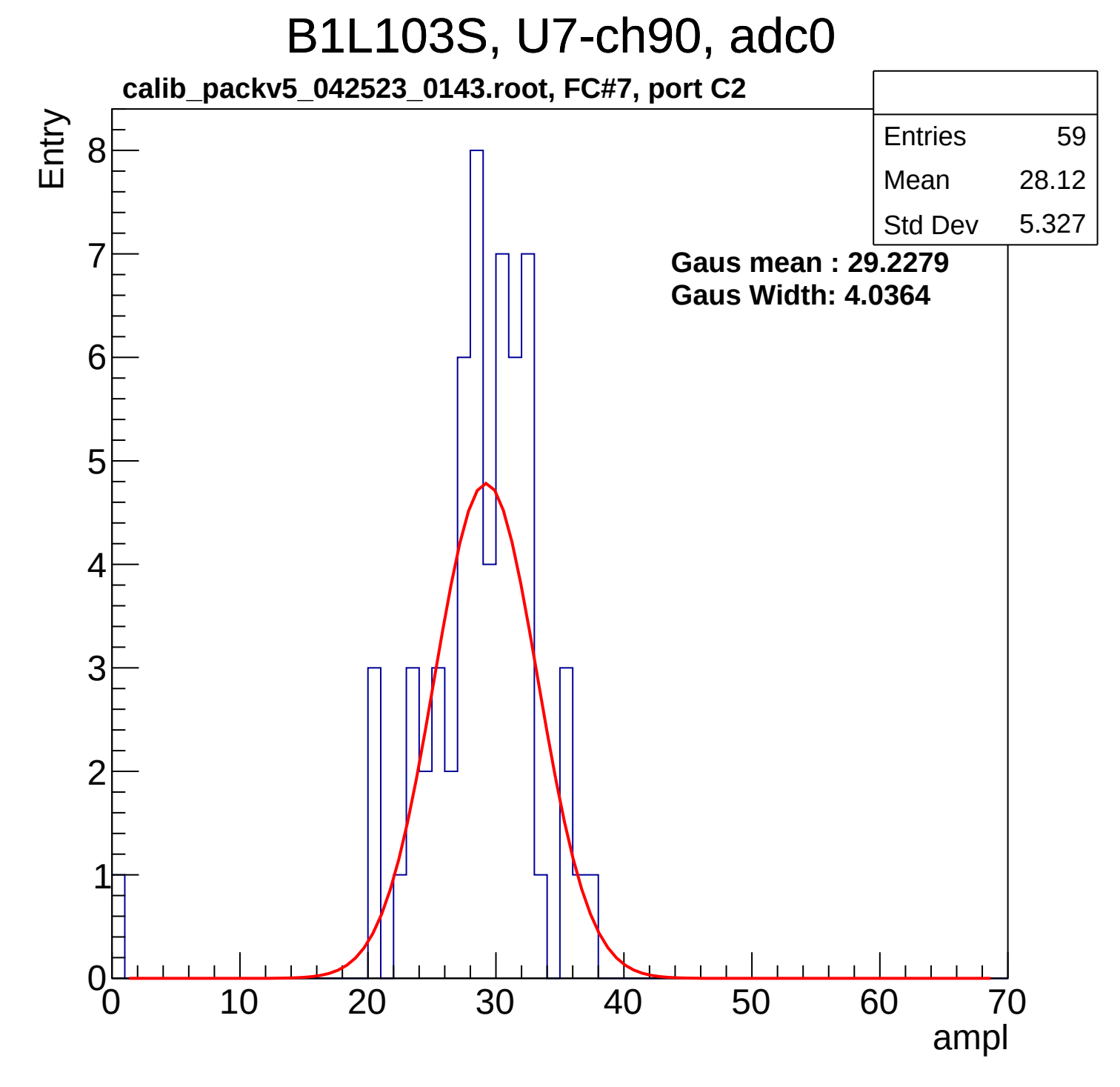
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch90, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 28.12
Std Dev 5.327
Gaus mean : 29.2279
Gaus Width: 4.0364
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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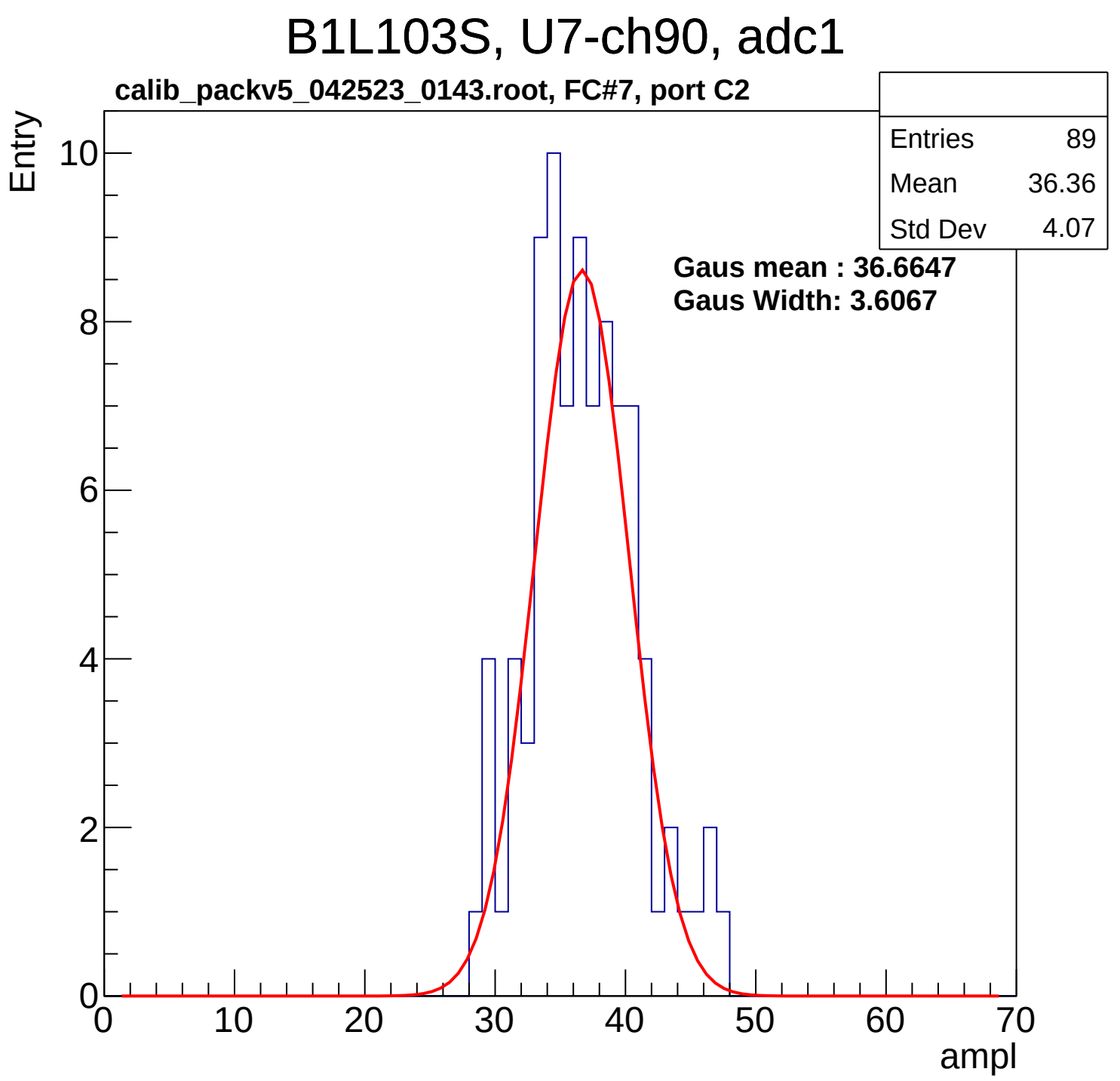
B1L103S, U7-ch90, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 89
Mean 36.36
Std Dev 4.07
Gaus mean : 36.6647
Gaus Width: 3.6067
Entry
ampl
0
2
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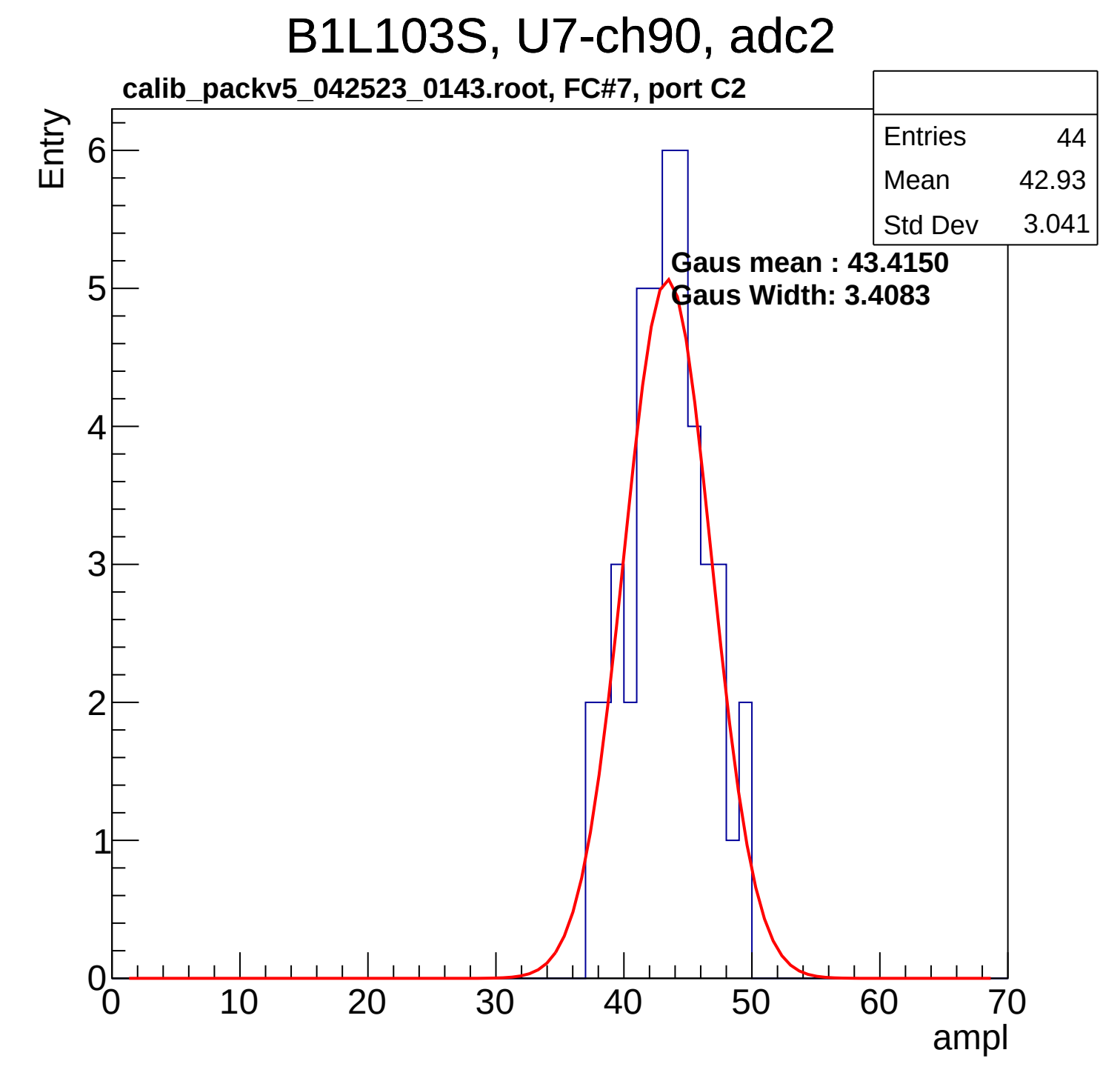
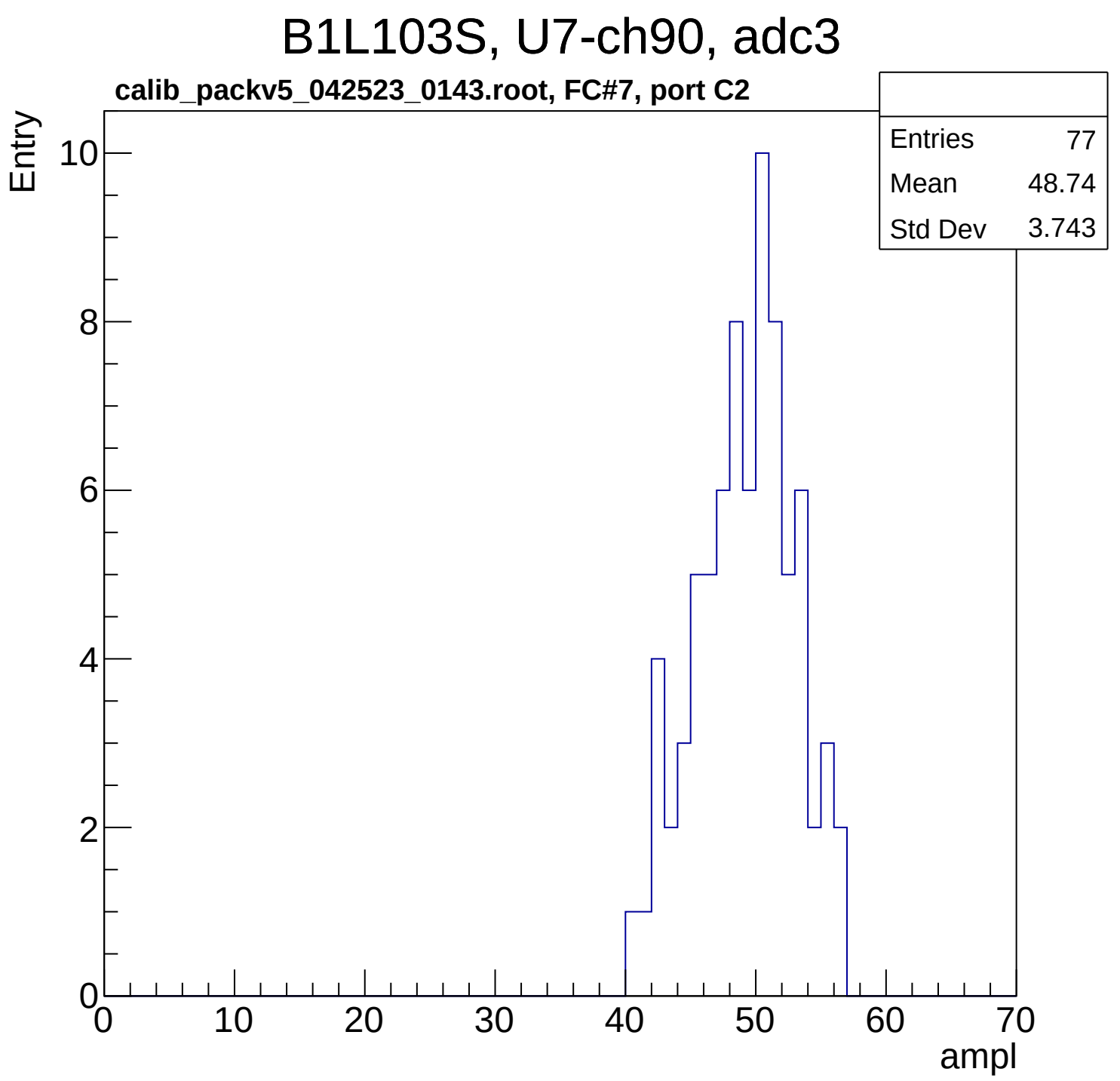
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch90, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 44
Mean 42.93
Std Dev 3.041
Gaus mean : 43.4150
Gaus Width: 3.4083
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U7-ch90, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 77
Mean 48.74
Std Dev 3.743
Entry
0
2
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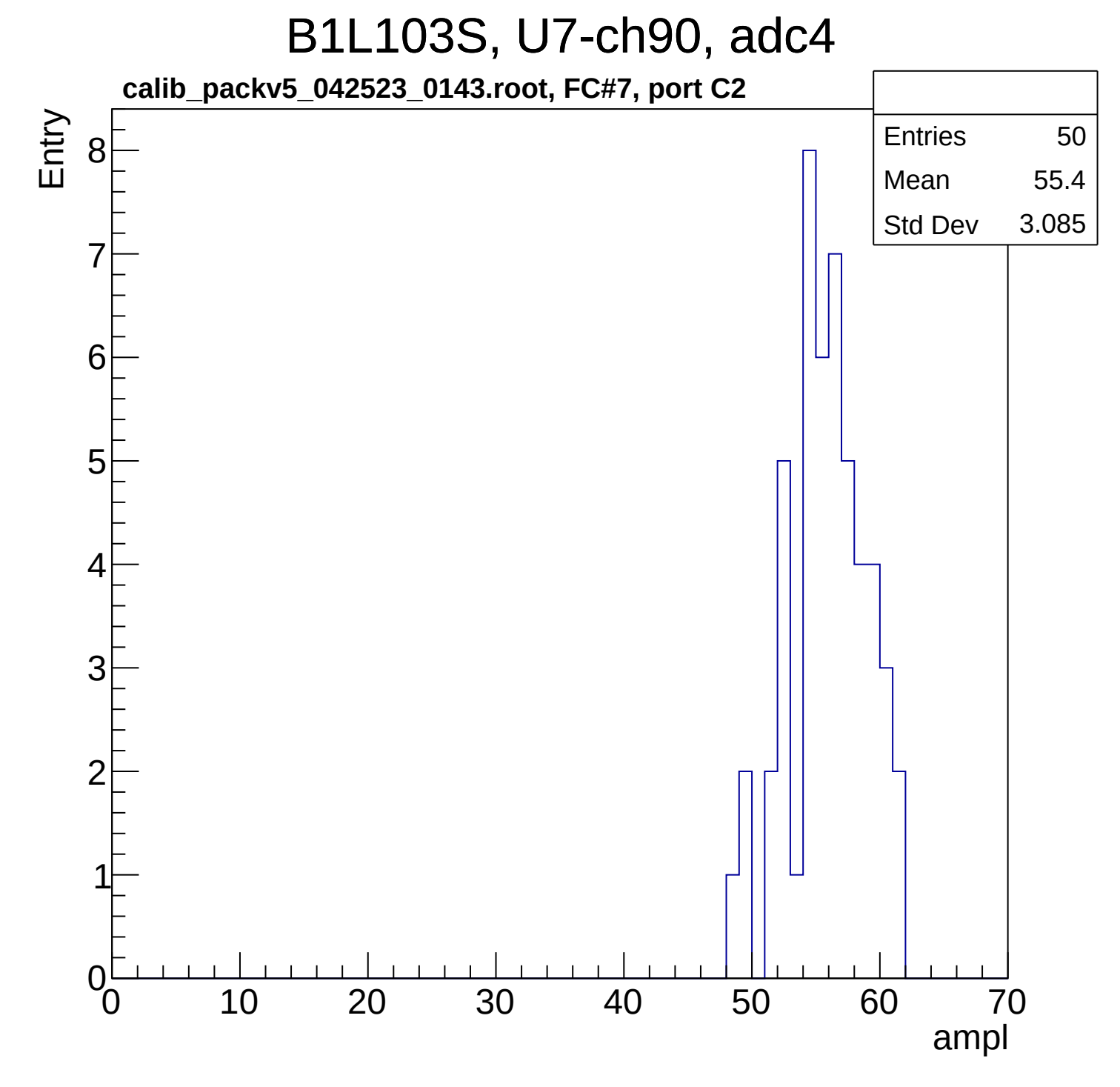
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch90, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 50
Mean 55.4
Std Dev 3.085
Entry
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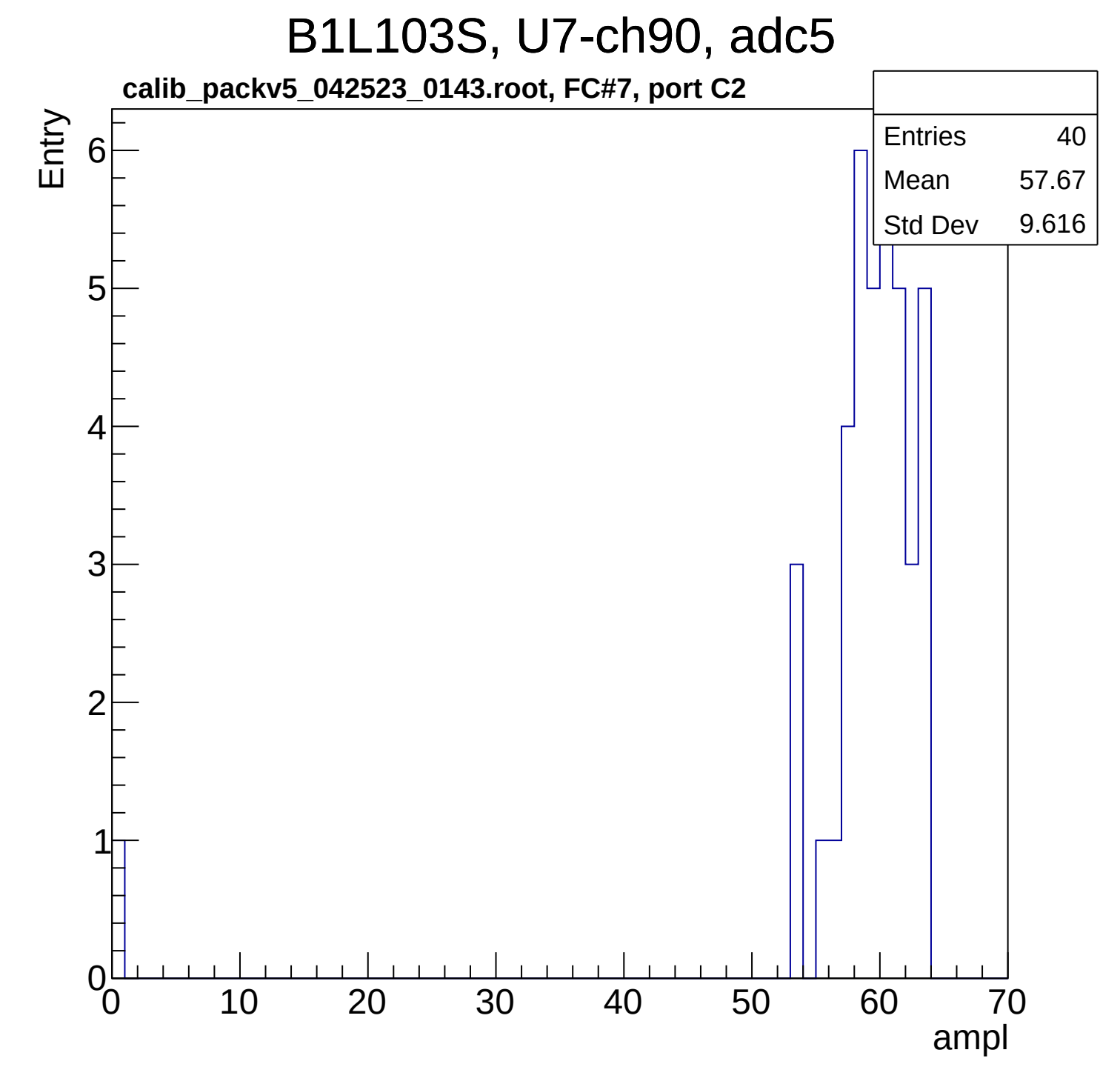
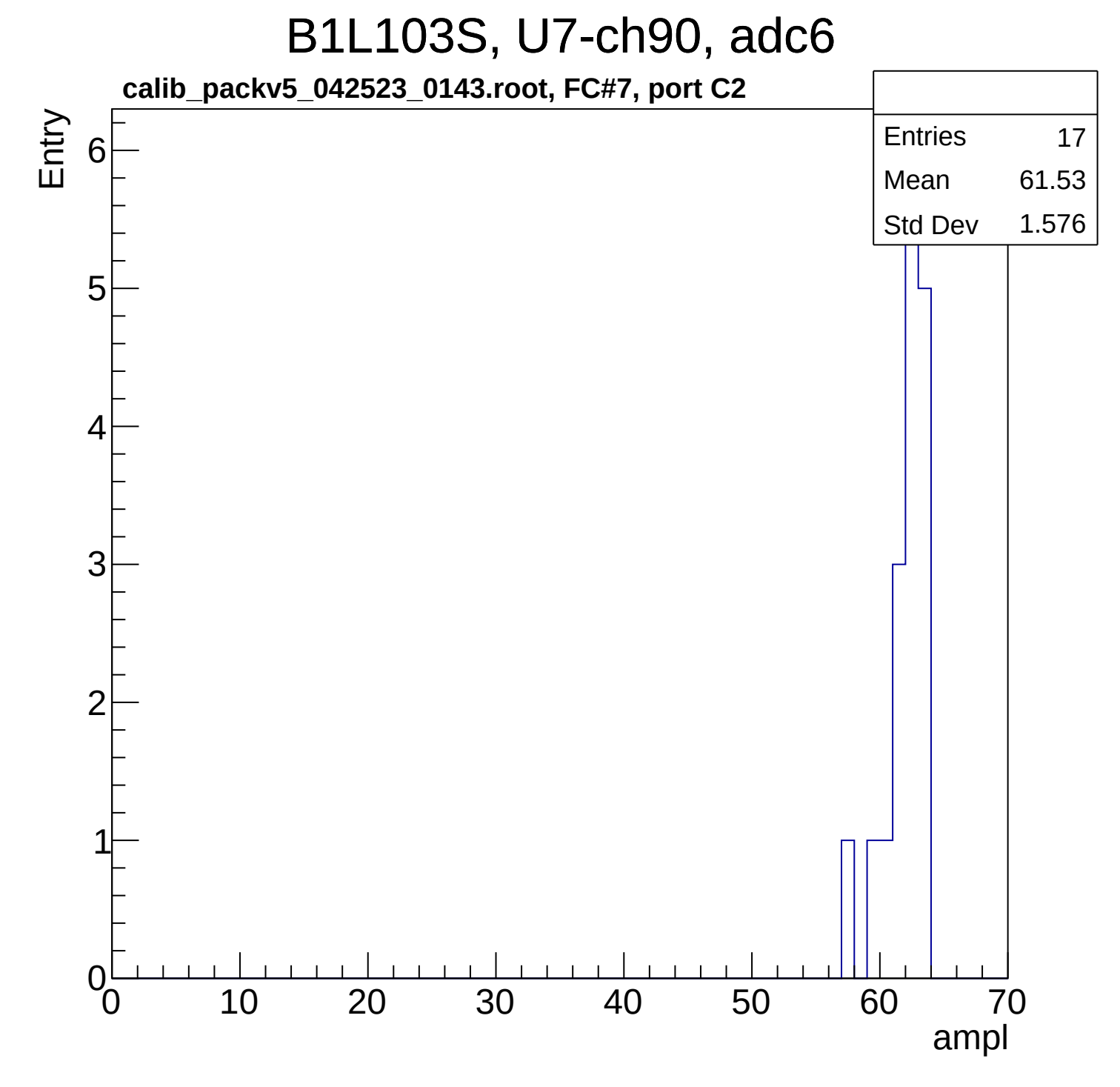
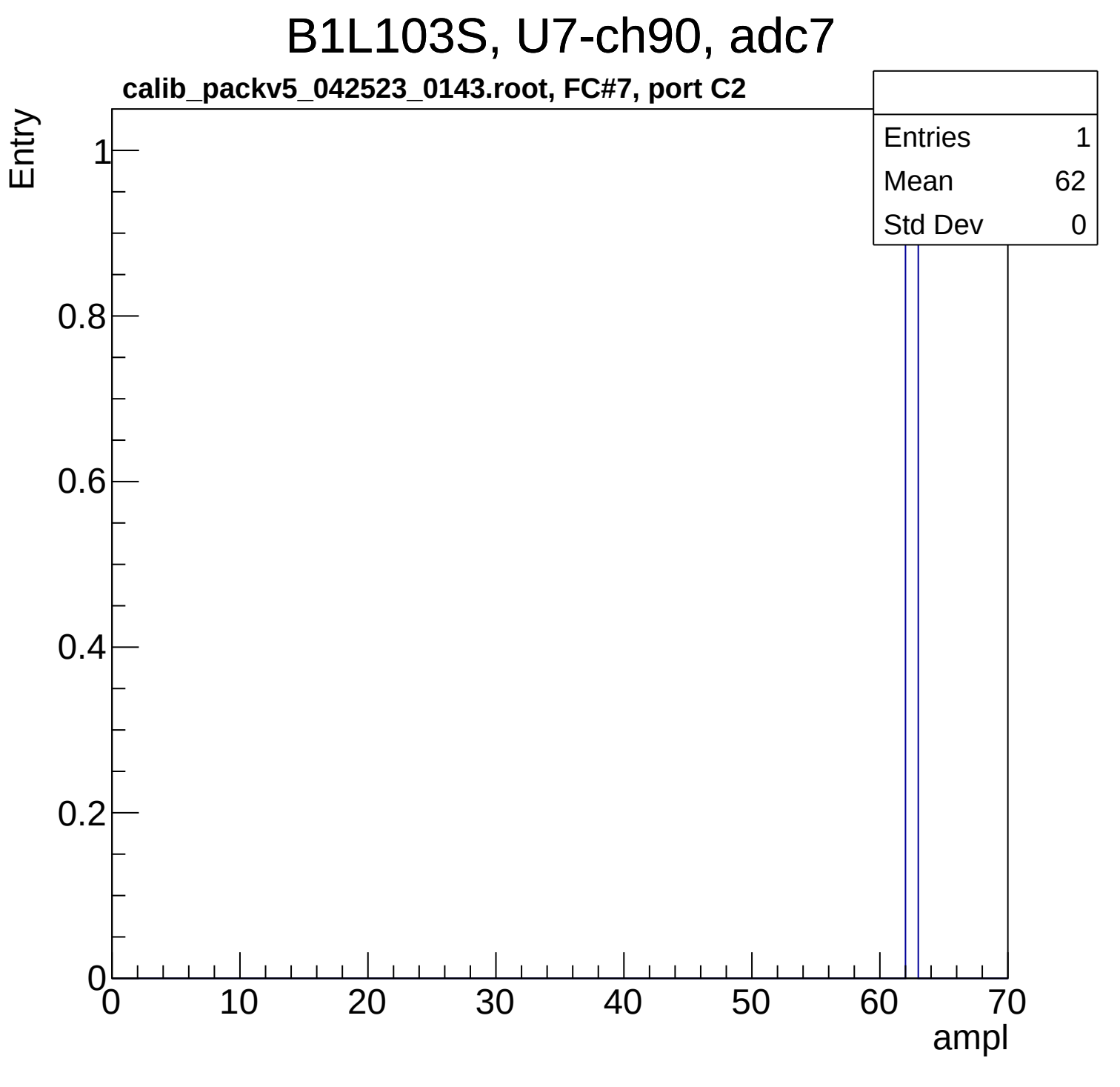
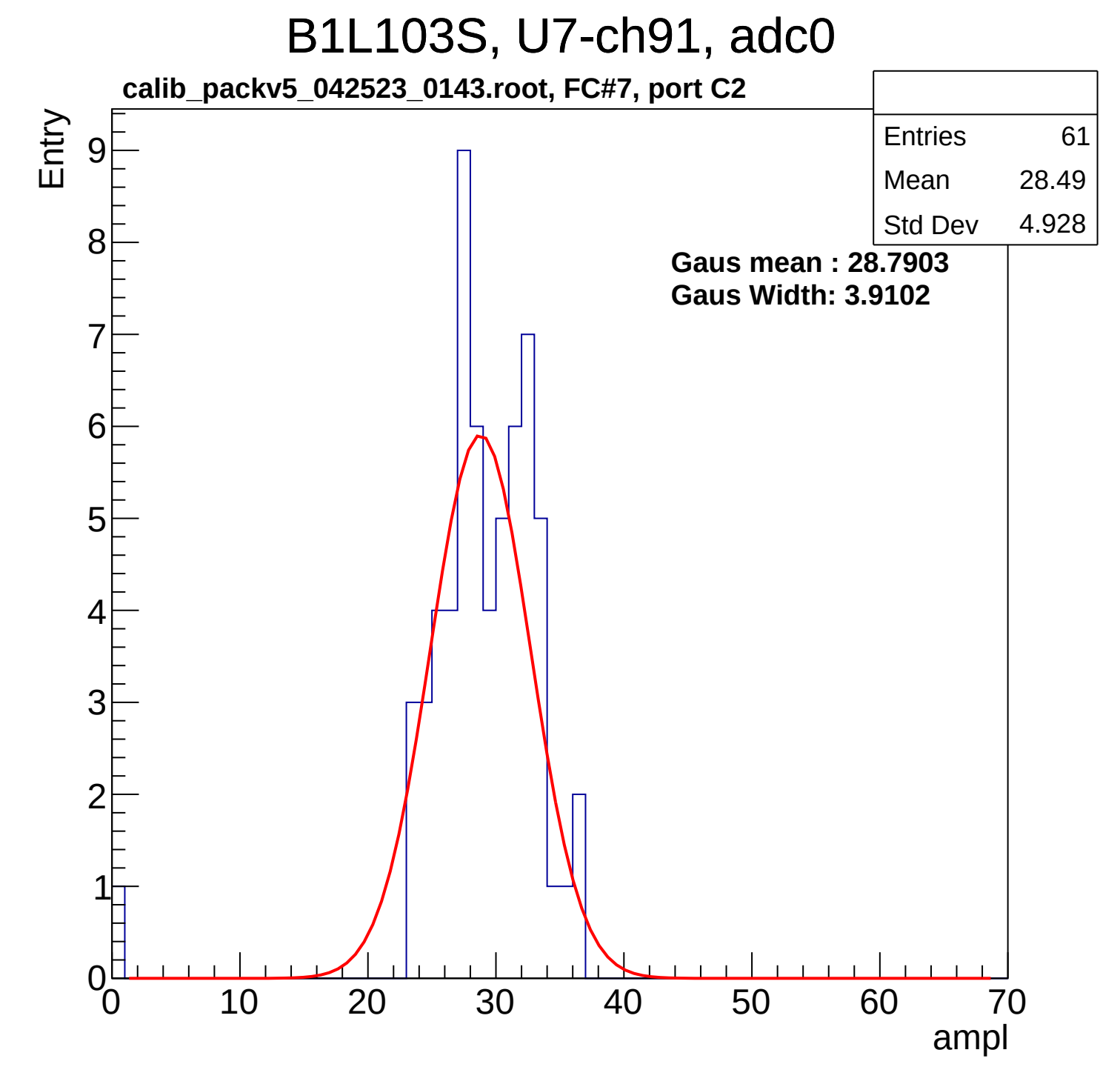
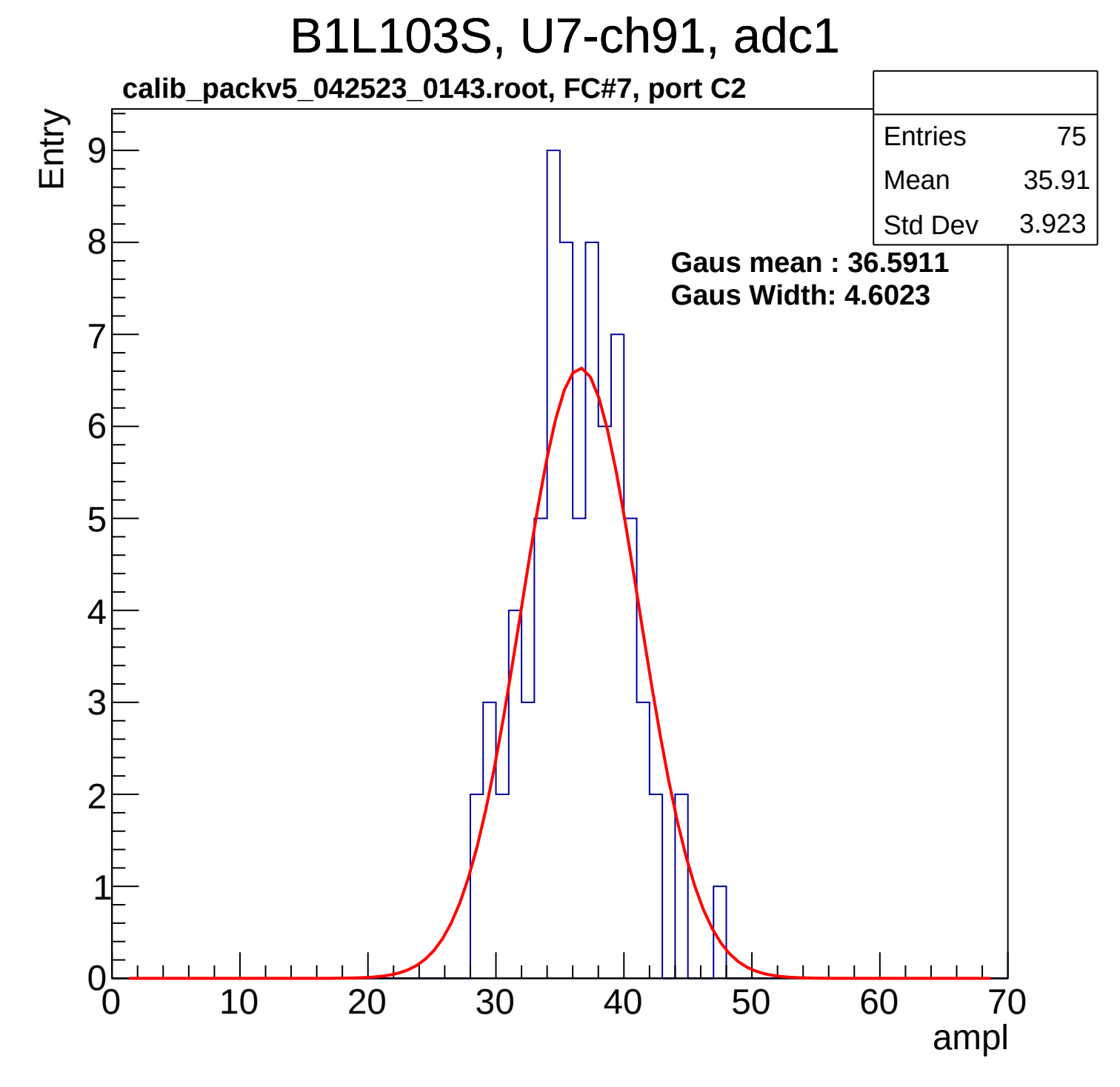
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

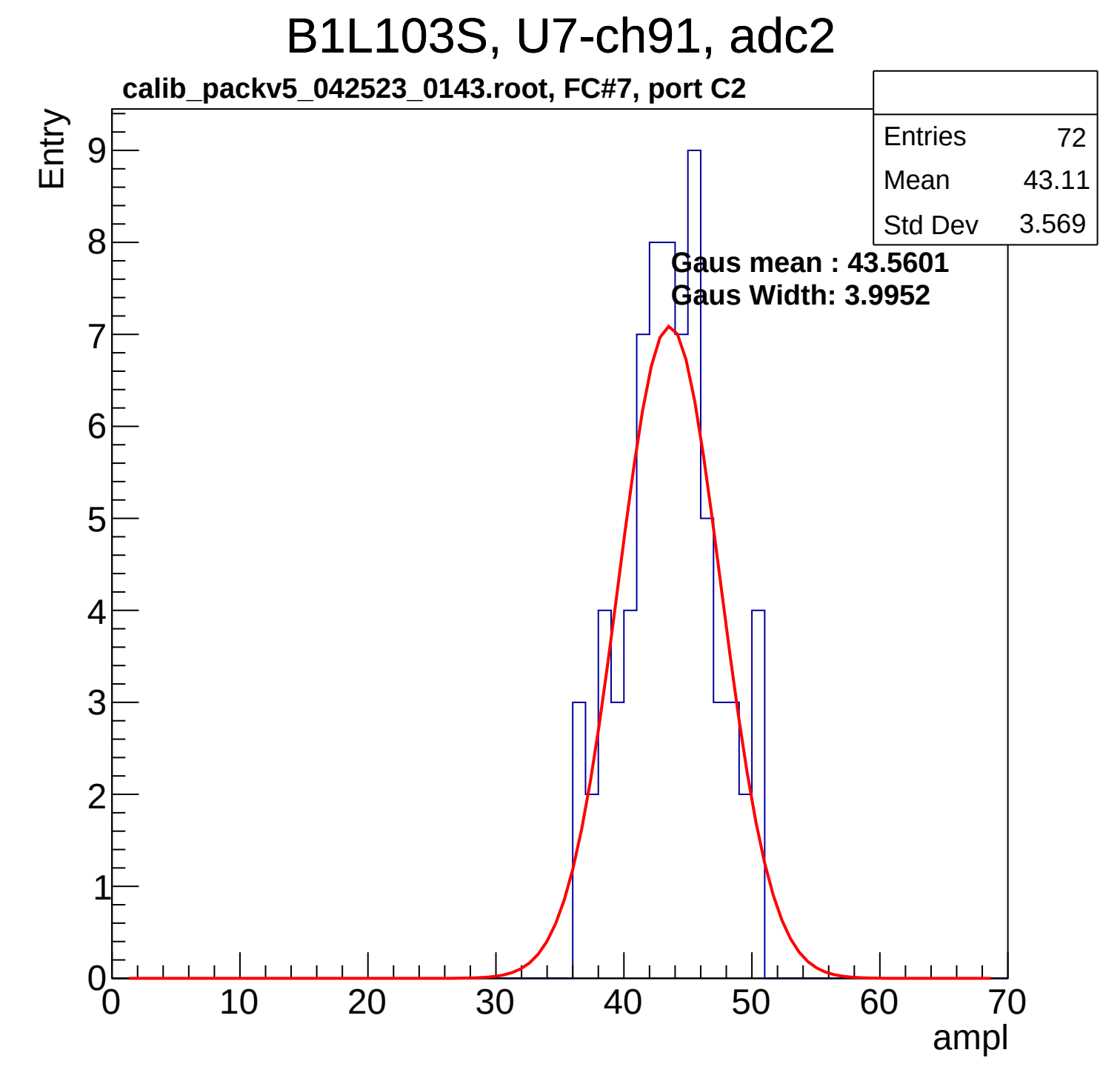

B1L103S, U7-ch90, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 40
Mean 57.67
Std Dev 9.616
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

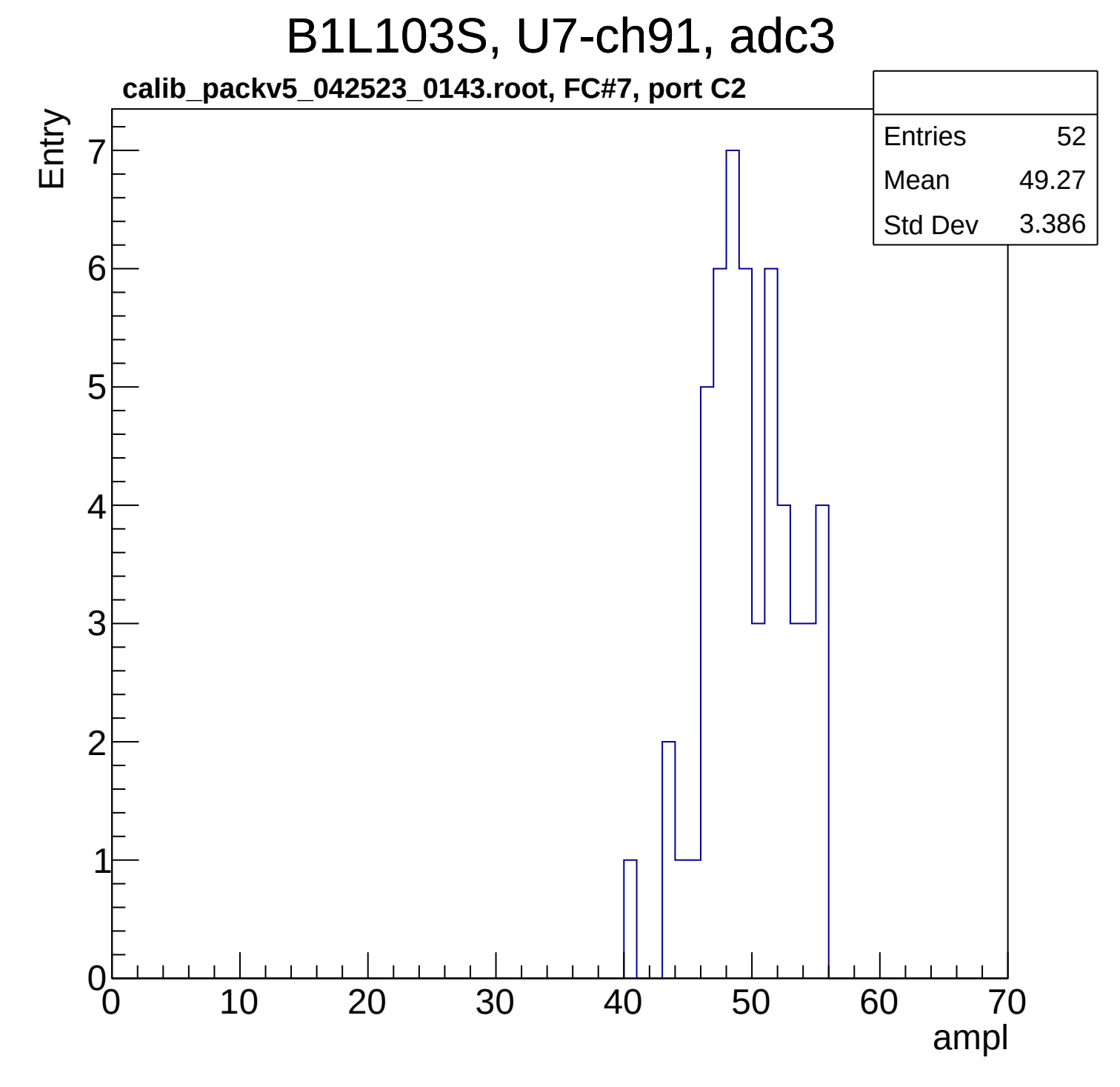

B1L103S, U7-ch90, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 17
Mean 61.53
Std Dev 1.576
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

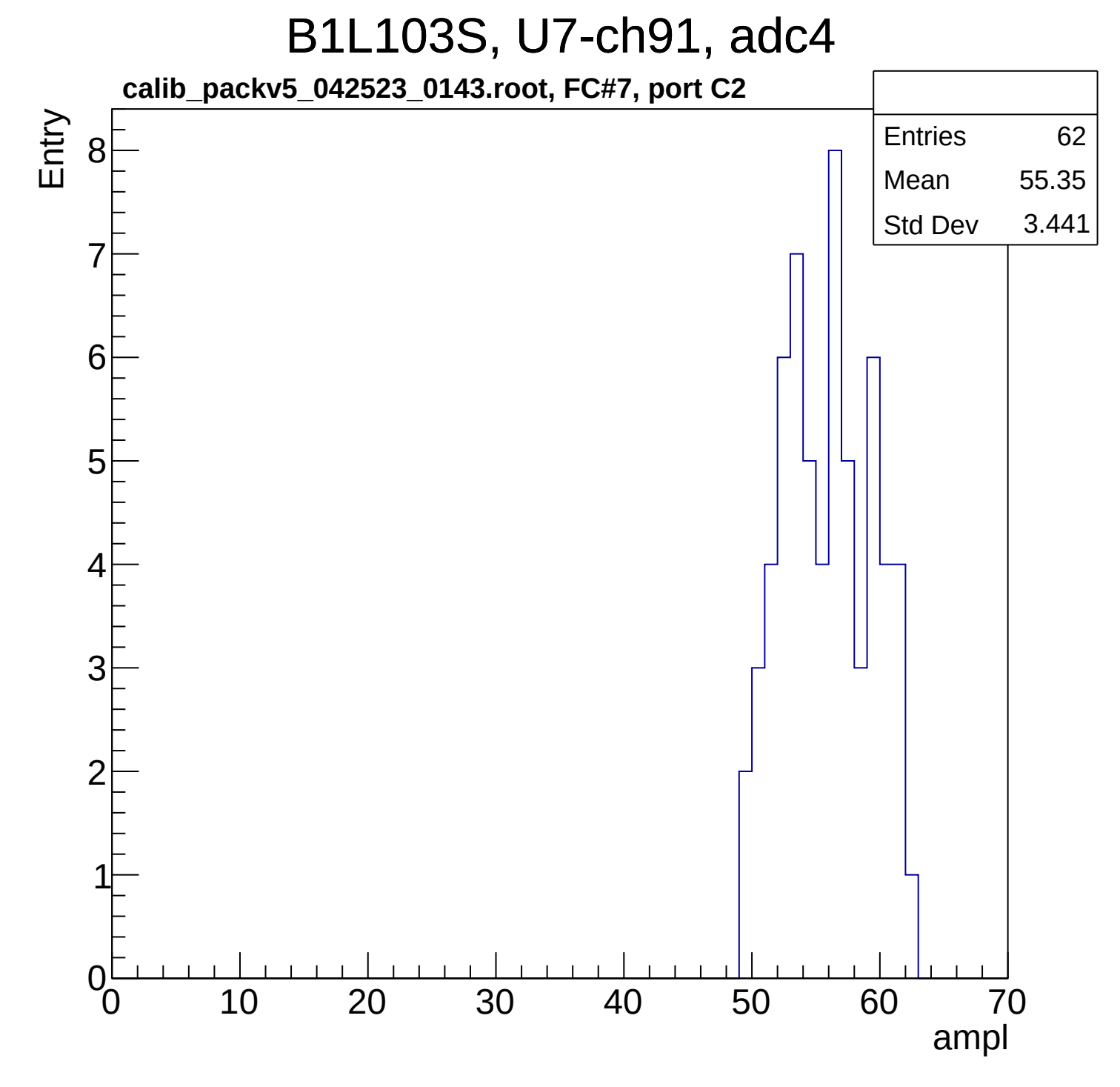

B1L103S, U7-ch90, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 62
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

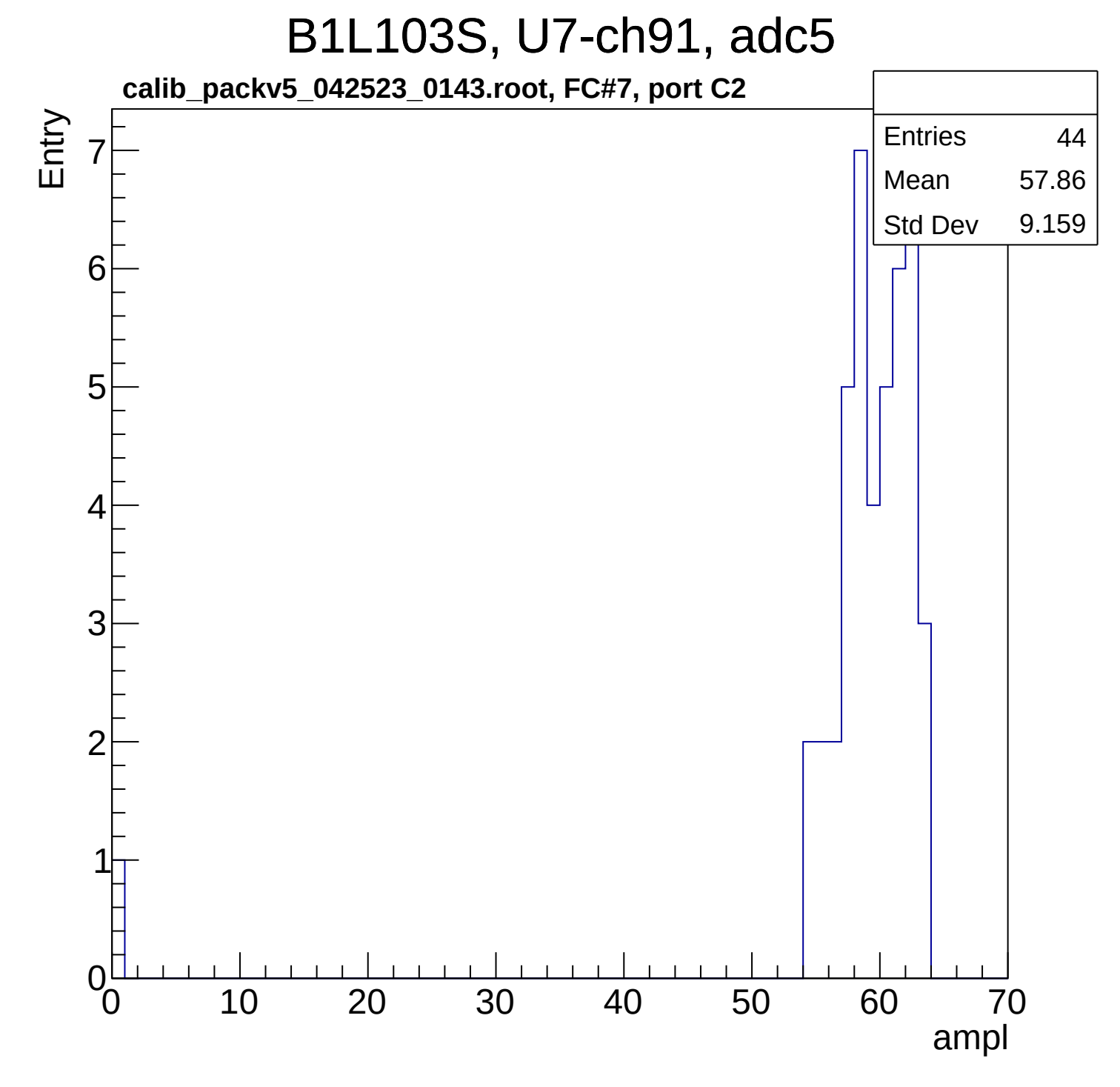

B1L103S, U7-ch91, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 61
Mean 28.49
Std Dev 4.928
Gaus mean : 28.7903
Gaus Width: 3.9102
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9

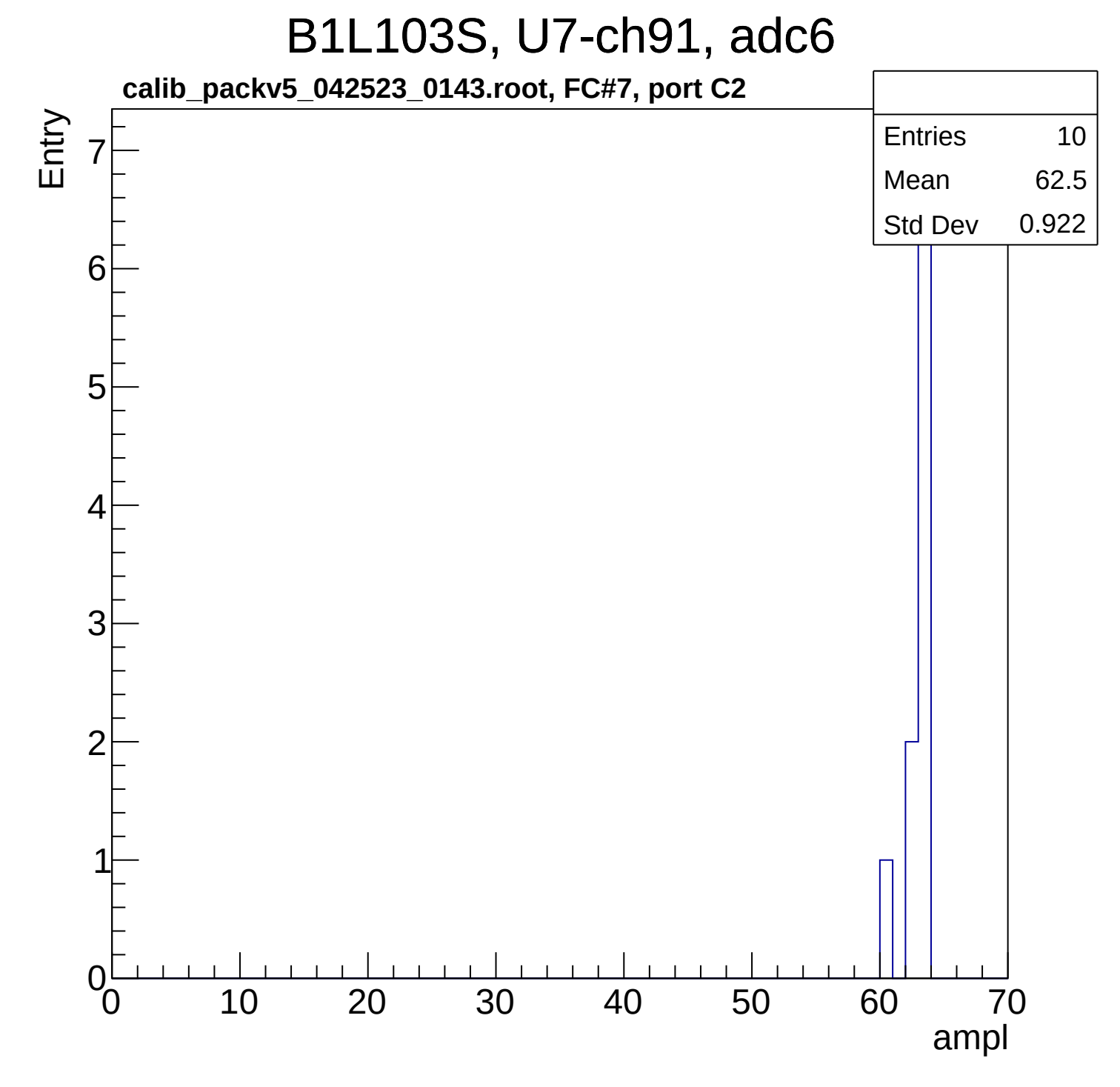

B1L103S, U7-ch91, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 75
Mean 35.91
Std Dev 3.923
Gaus mean : 36.5911
Gaus Width: 4.6023
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

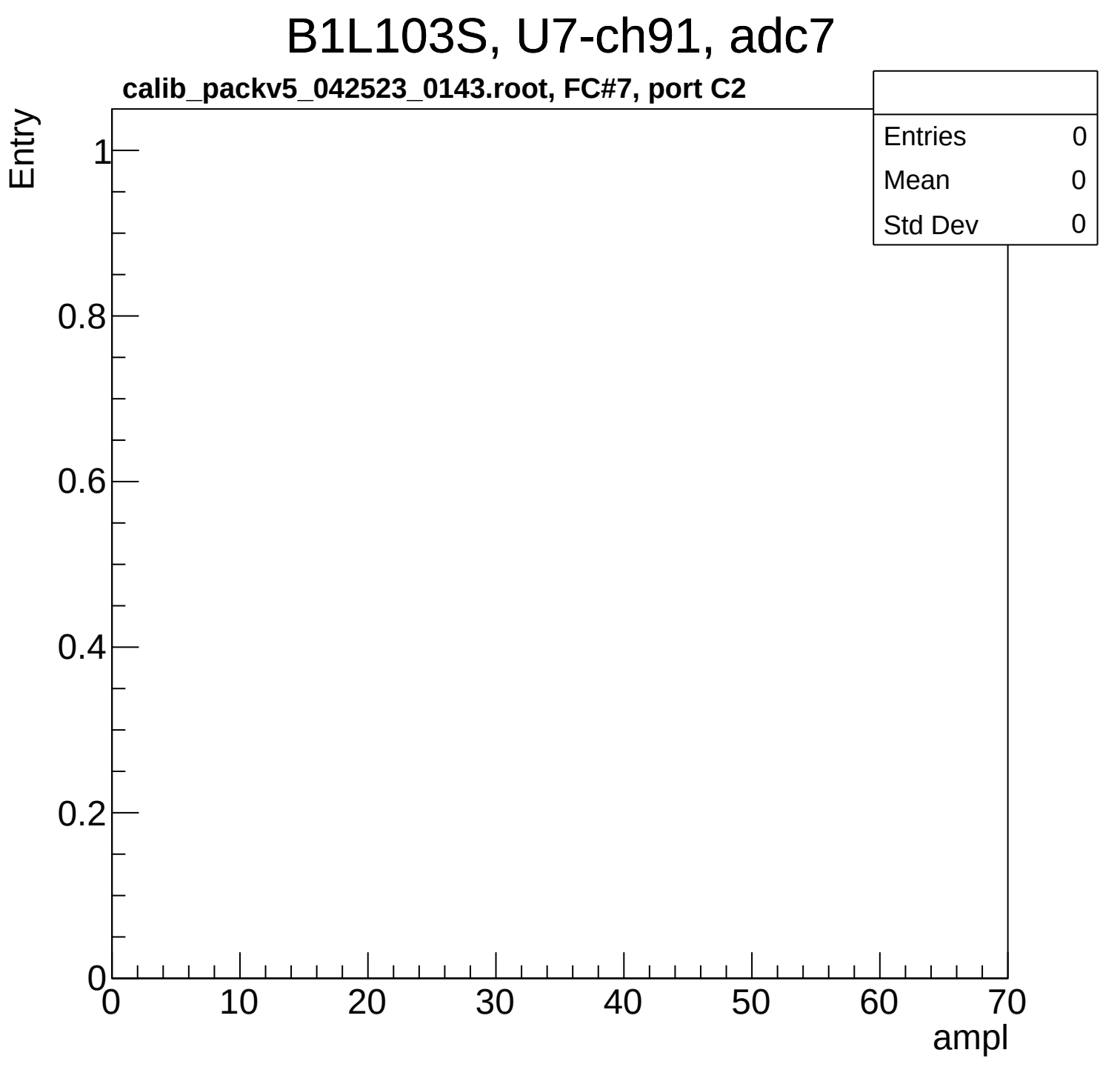

B1L103S, U7-ch91, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 72
Mean 43.11
Std Dev 3.569
Gaus mean : 43.5601
Gaus Width: 3.9952
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

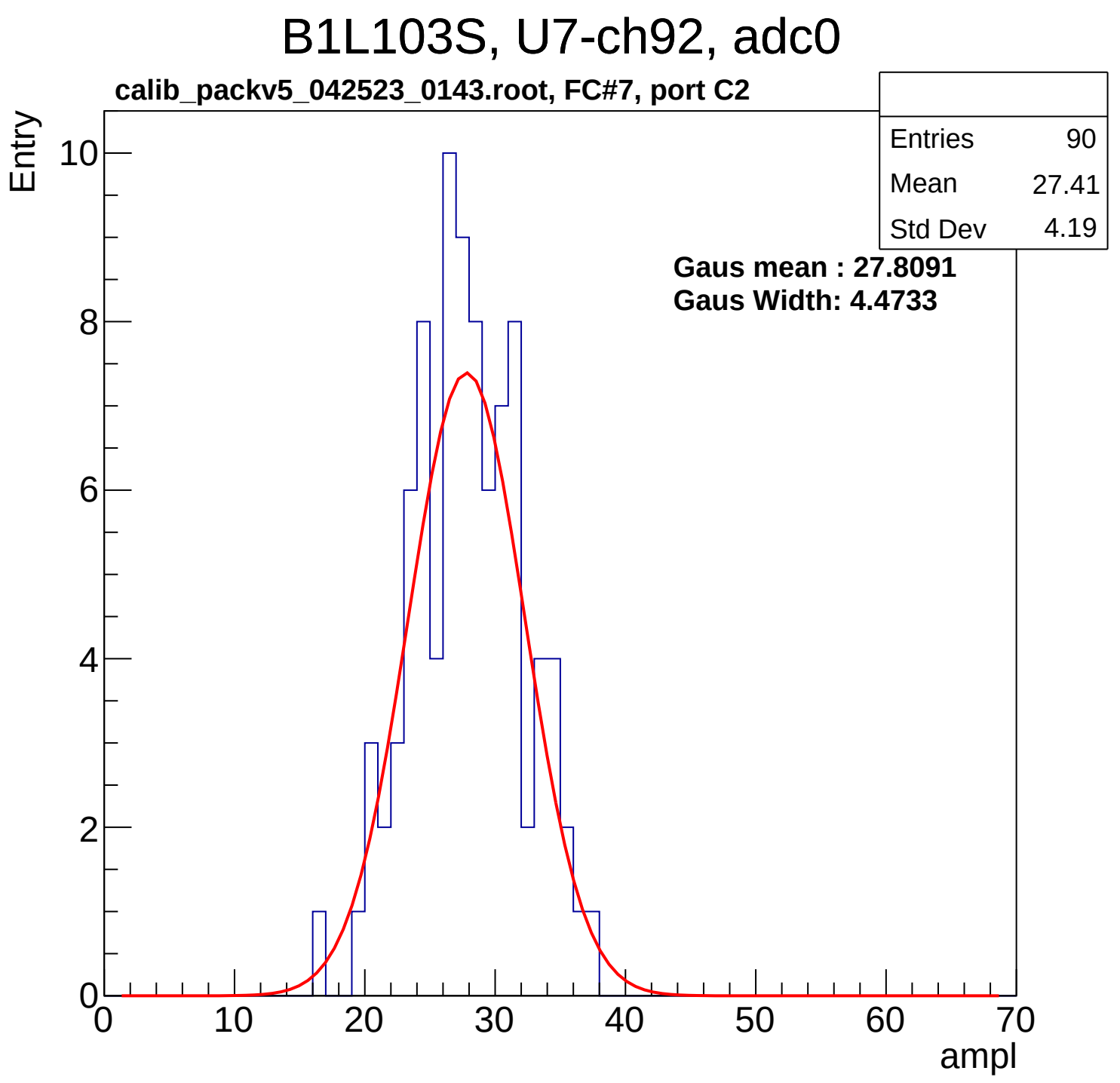

B1L103S, U7-ch91, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 52
Mean 49.27
Std Dev 3.386
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

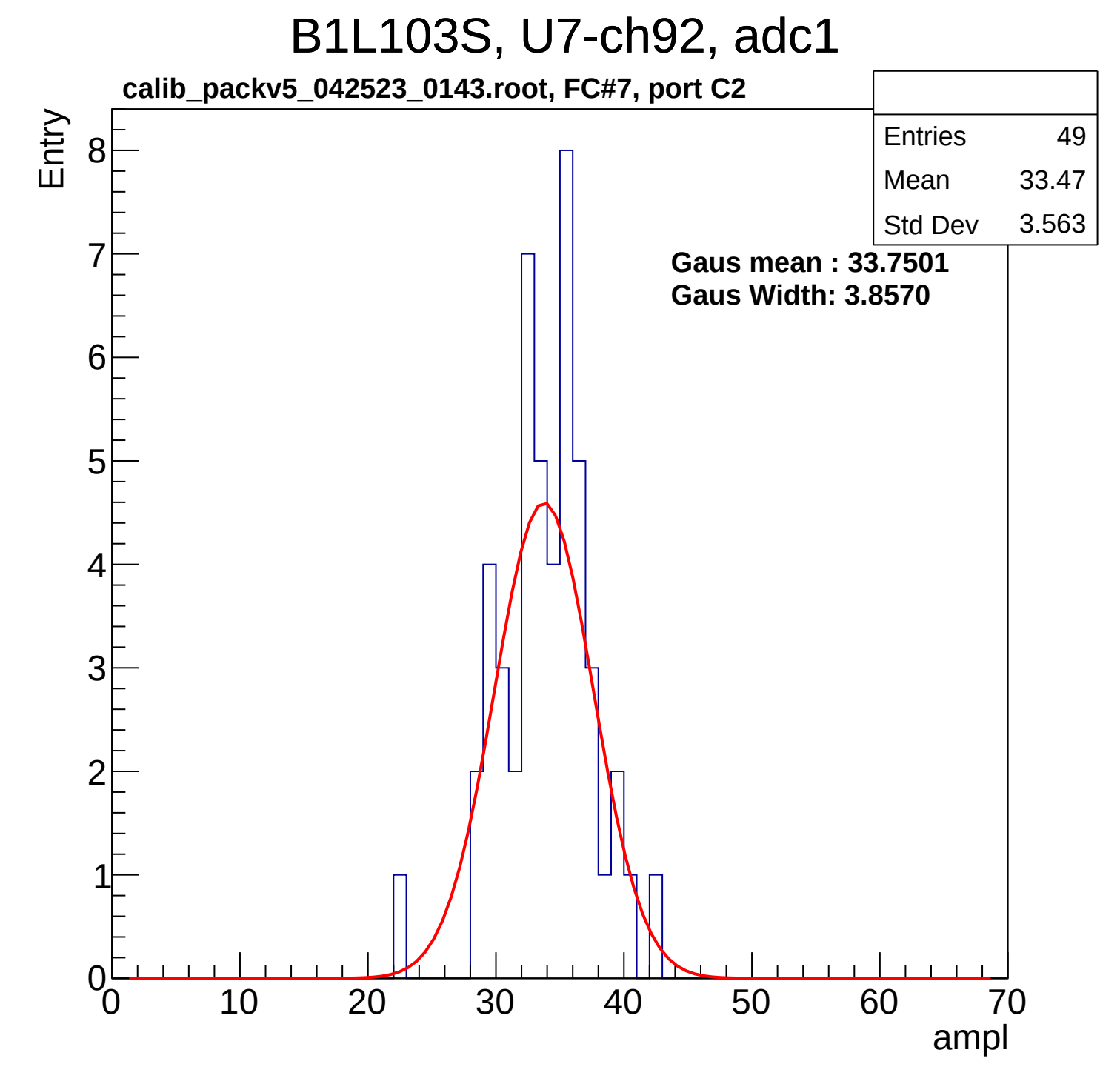

B1L103S, U7-ch91, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 62
Mean 55.35
Std Dev 3.441
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

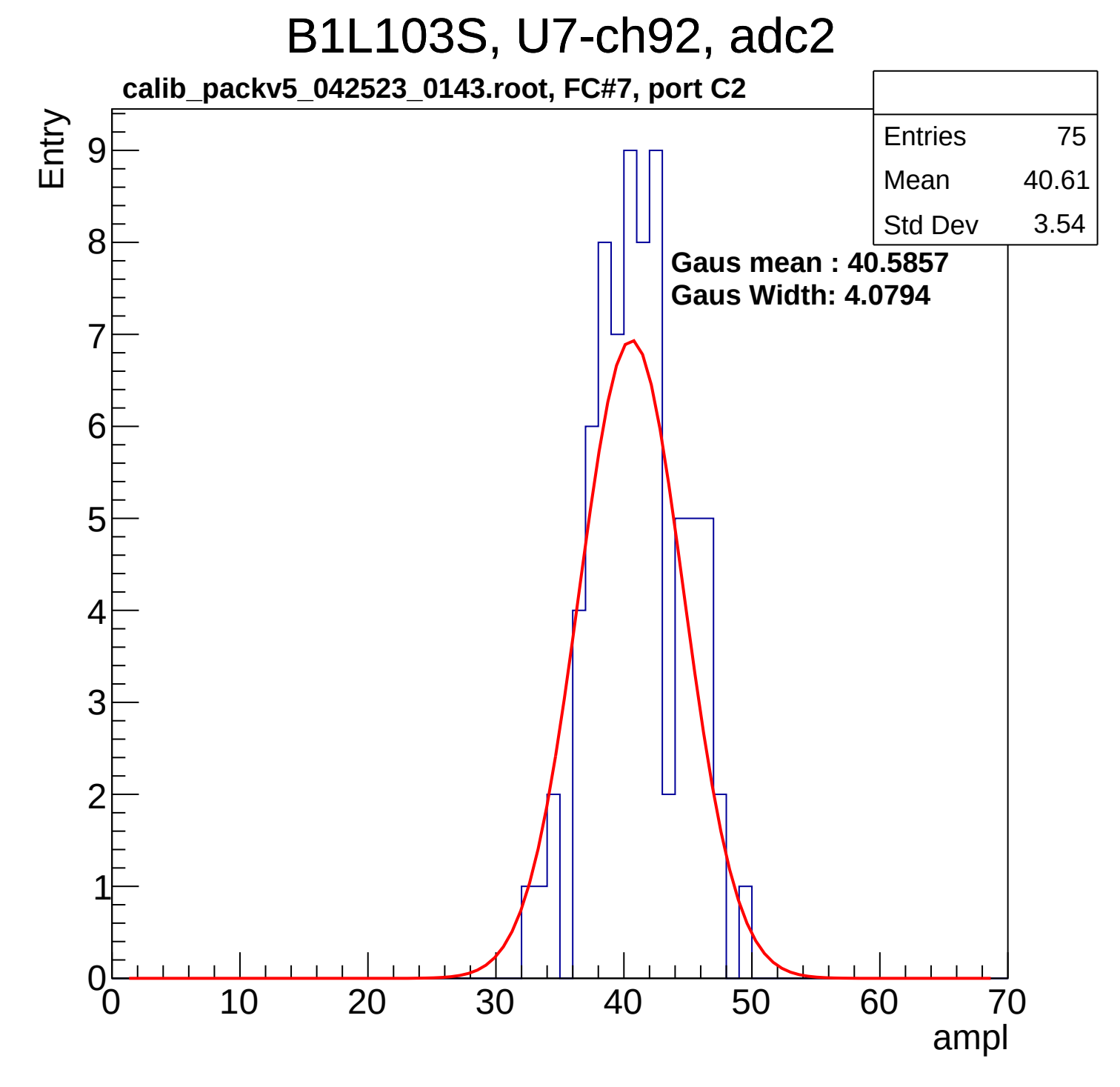

B1L103S, U7-ch91, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 44
Mean 57.86
Std Dev 9.159
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch91, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 10
Mean 62.5
Std Dev 0.922
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch91, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch92, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 90
Mean 27.41
Std Dev 4.19
Gaus mean : 27.8091
Gaus Width: 4.4733
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch92, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 49
Mean 33.47
Std Dev 3.563
Gaus mean : 33.7501
Gaus Width: 3.8570
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch92, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 75
Mean 40.61
Std Dev 3.54
Gaus mean : 40.5857
Gaus Width: 4.0794
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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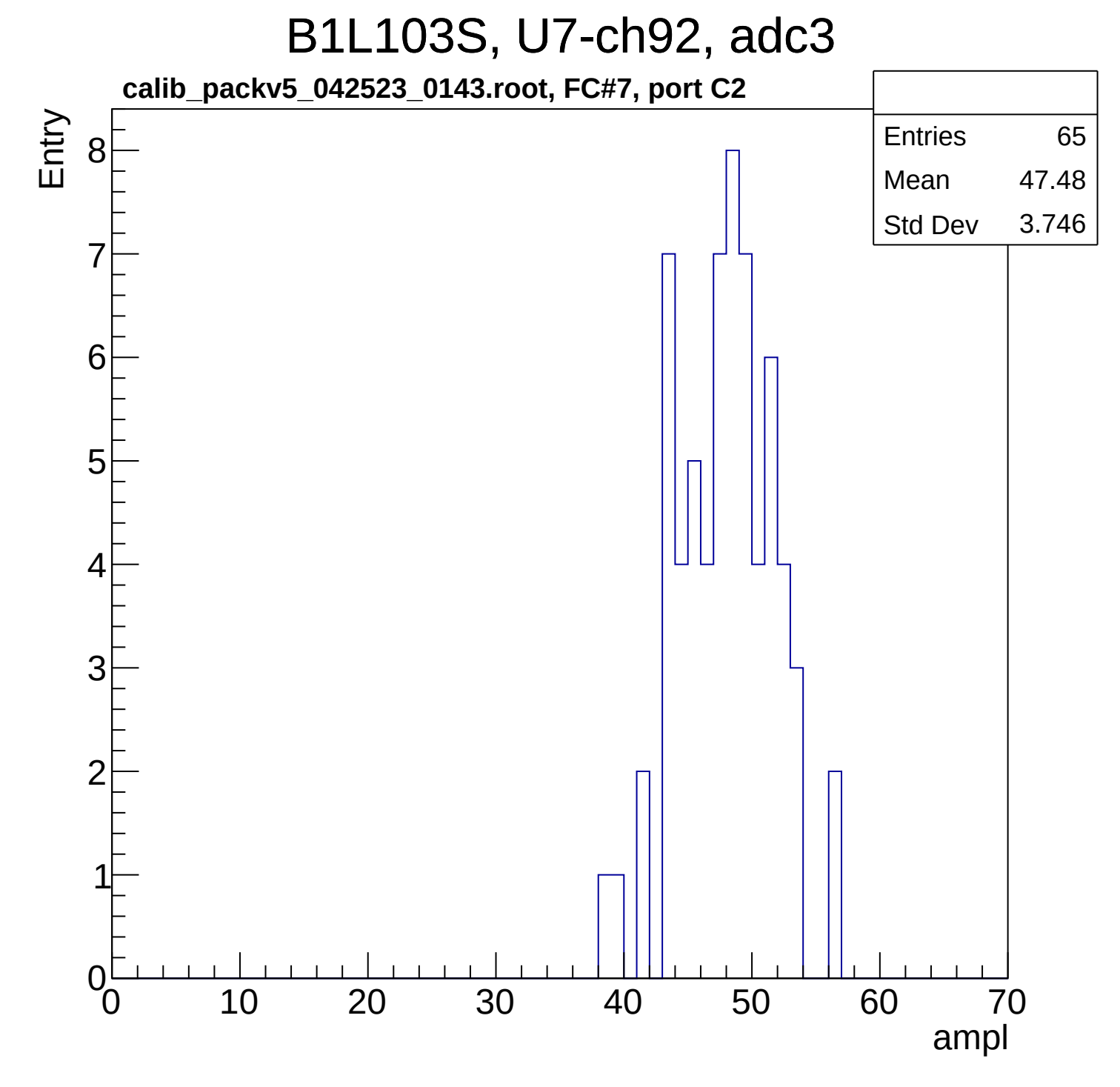
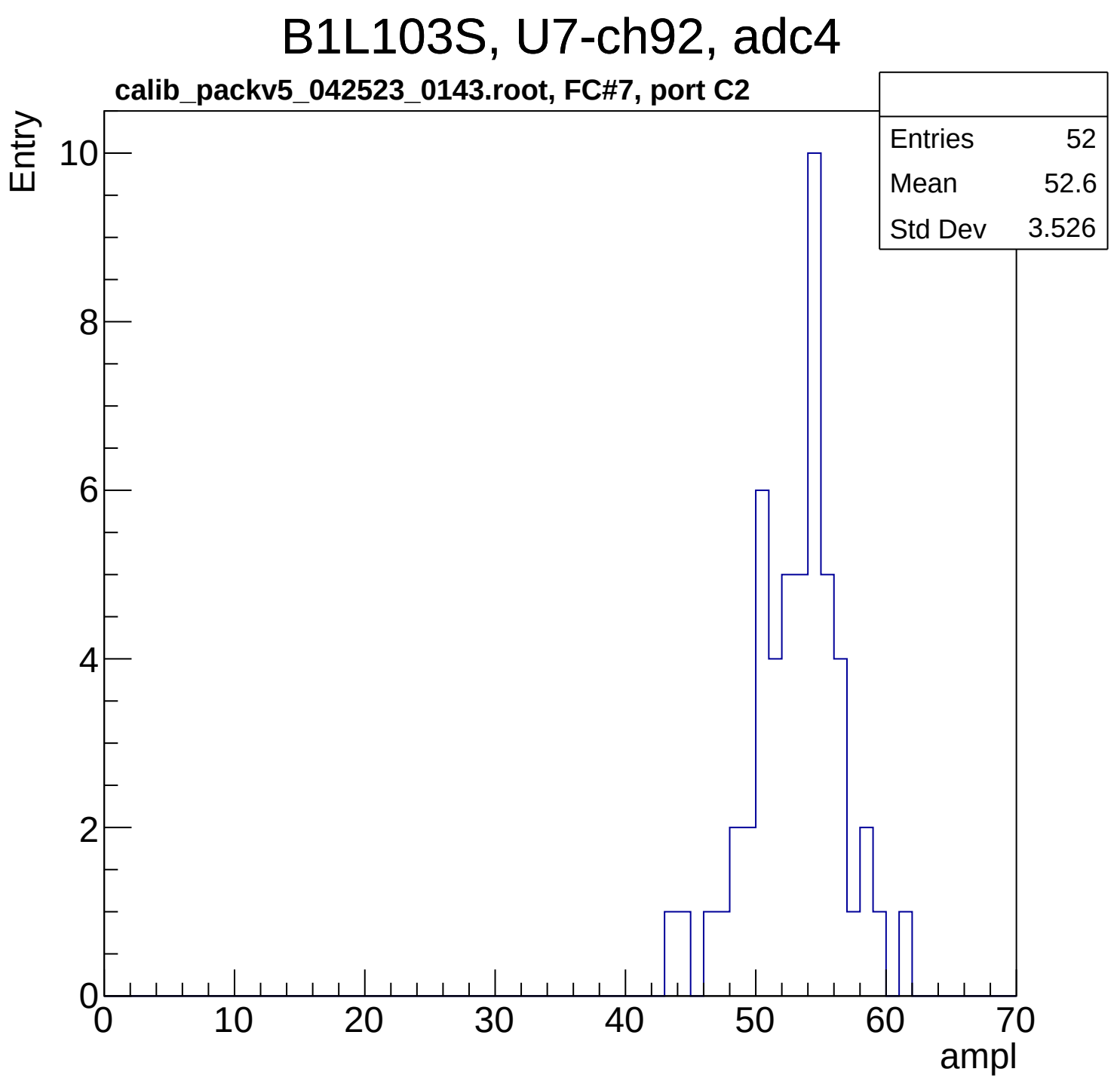
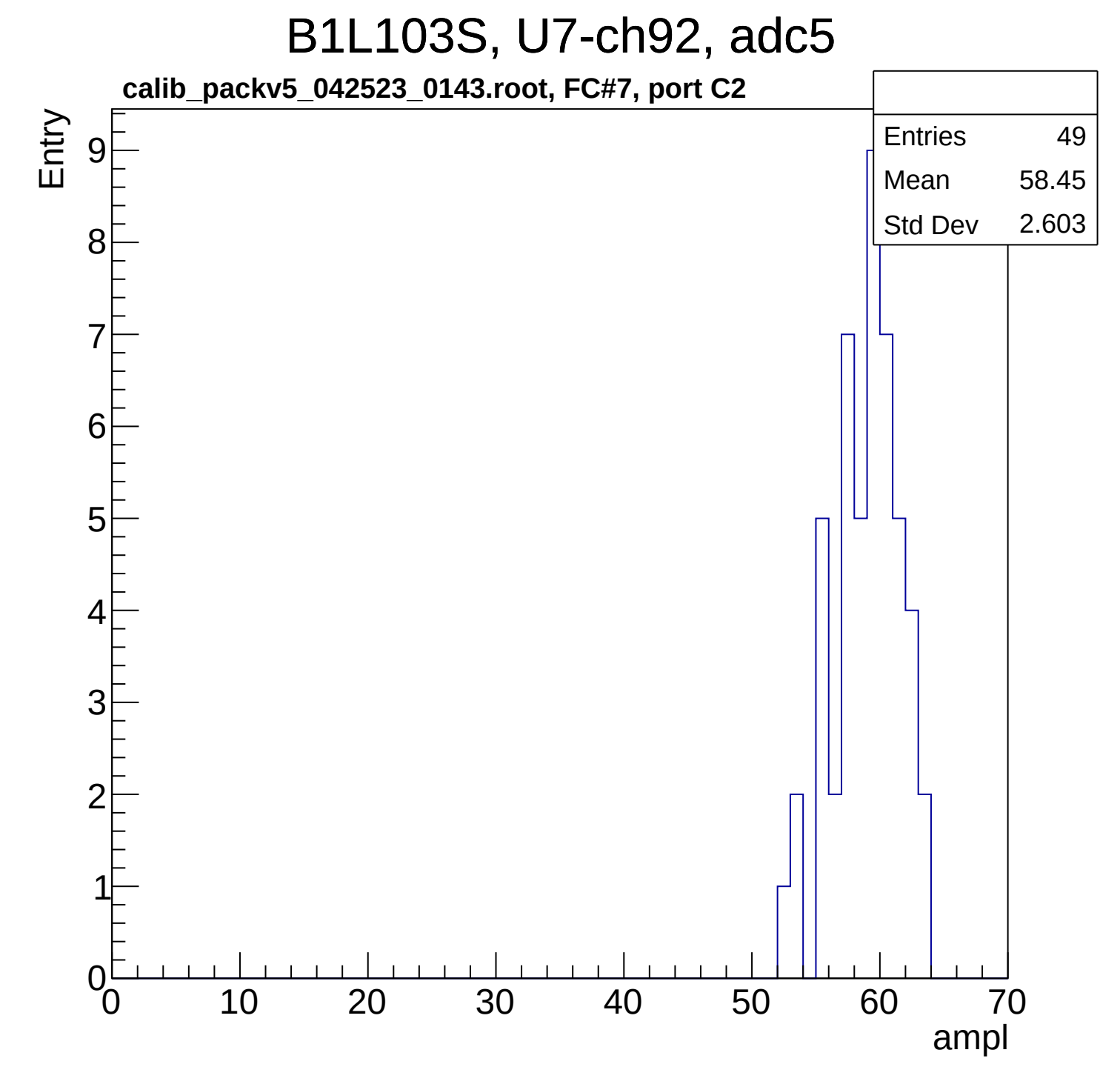

B1L103S, U7-ch92, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 47.48
Std Dev 3.746
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch92, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 52
Mean 52.6
Std Dev 3.526
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch92, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 49
Mean 58.45
Std Dev 2.603
Entry
ampl
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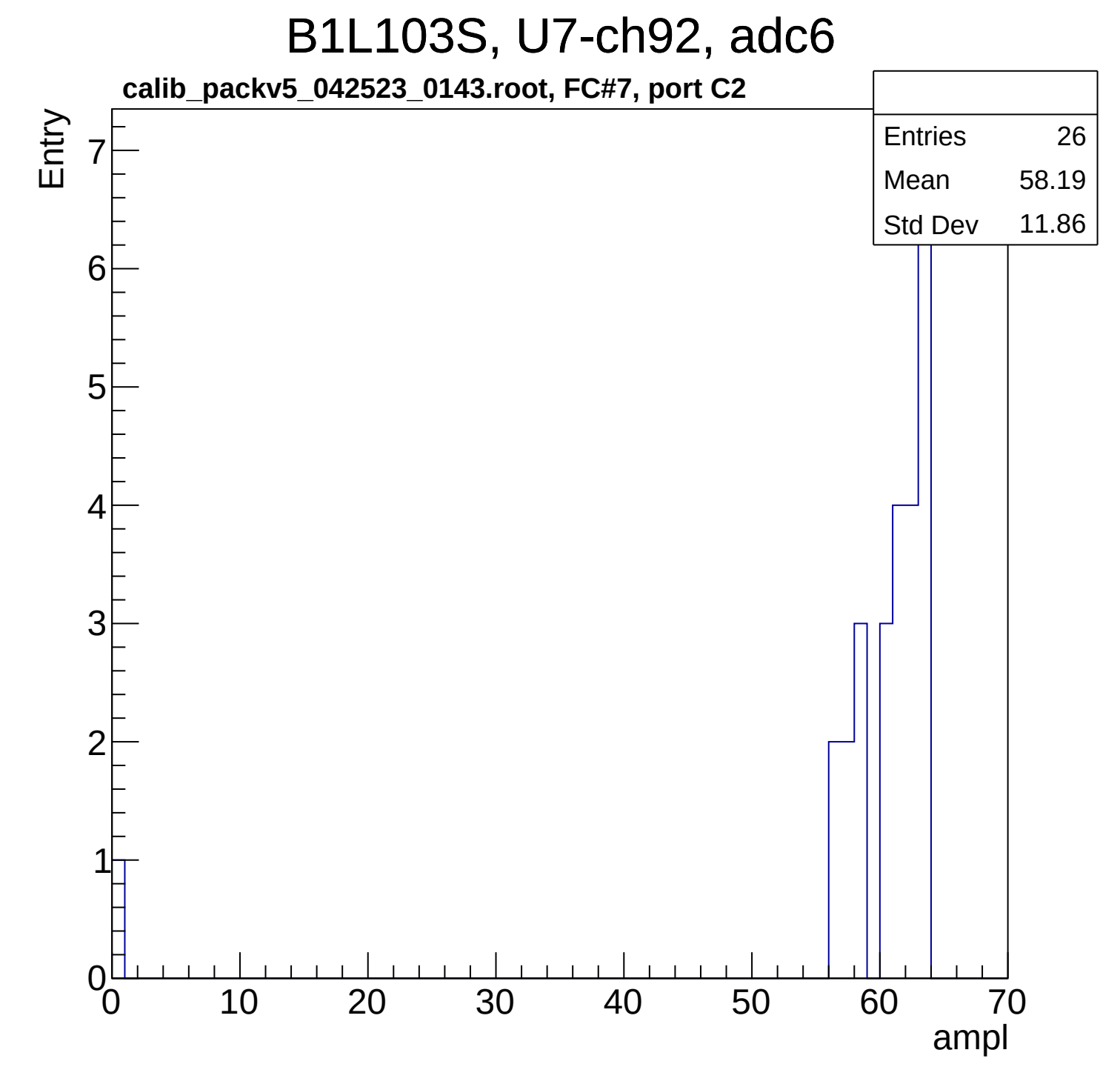
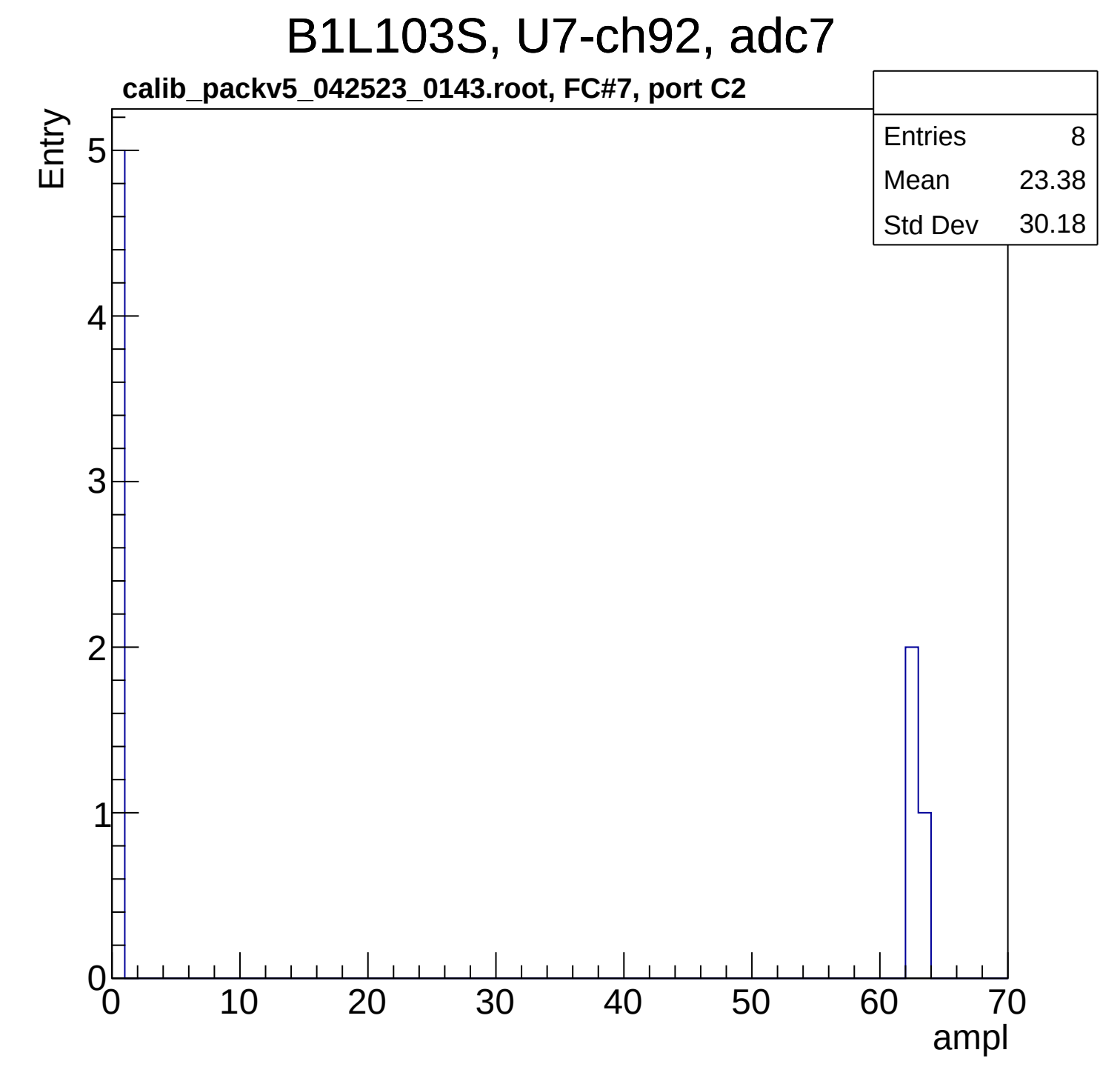
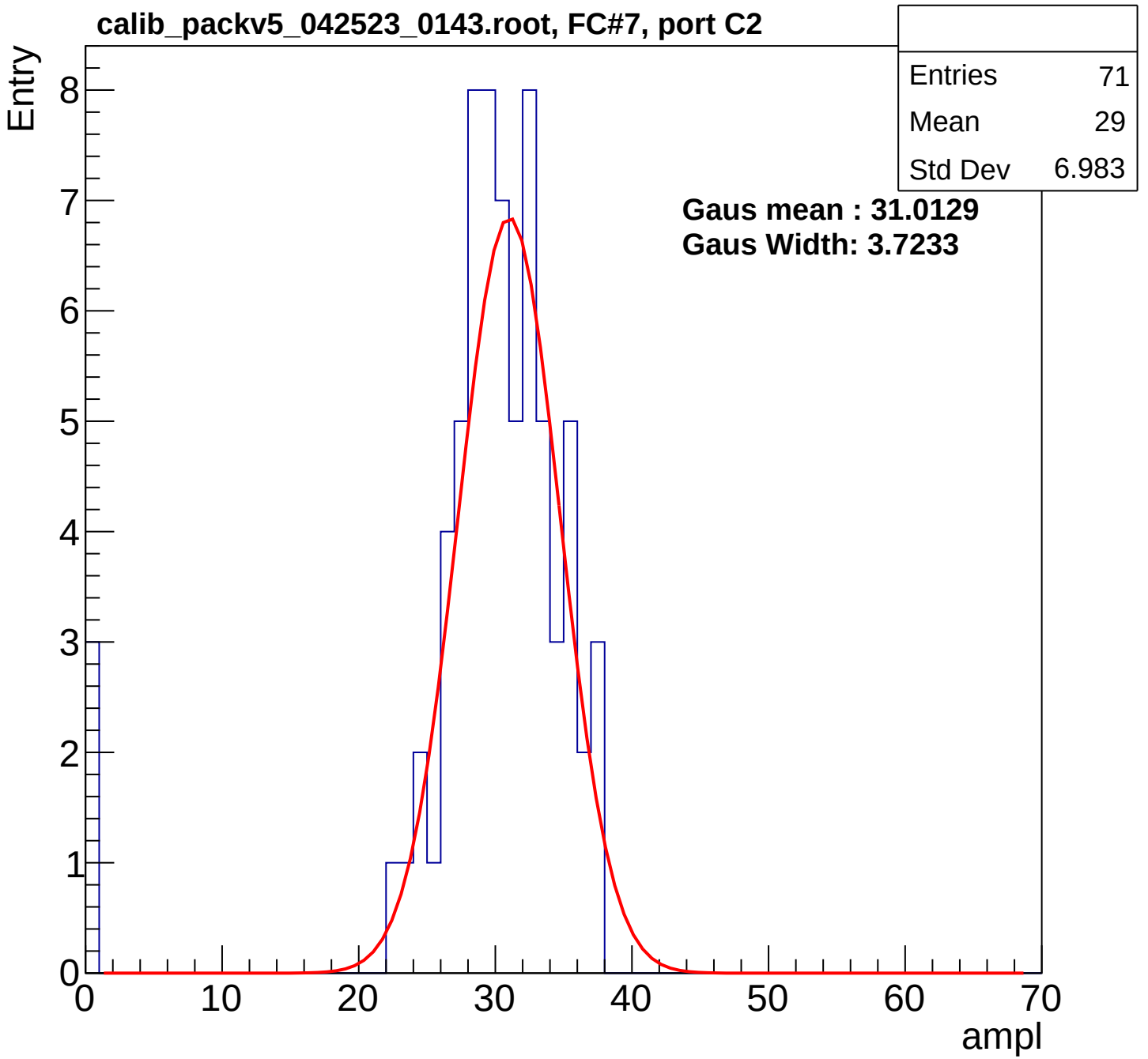
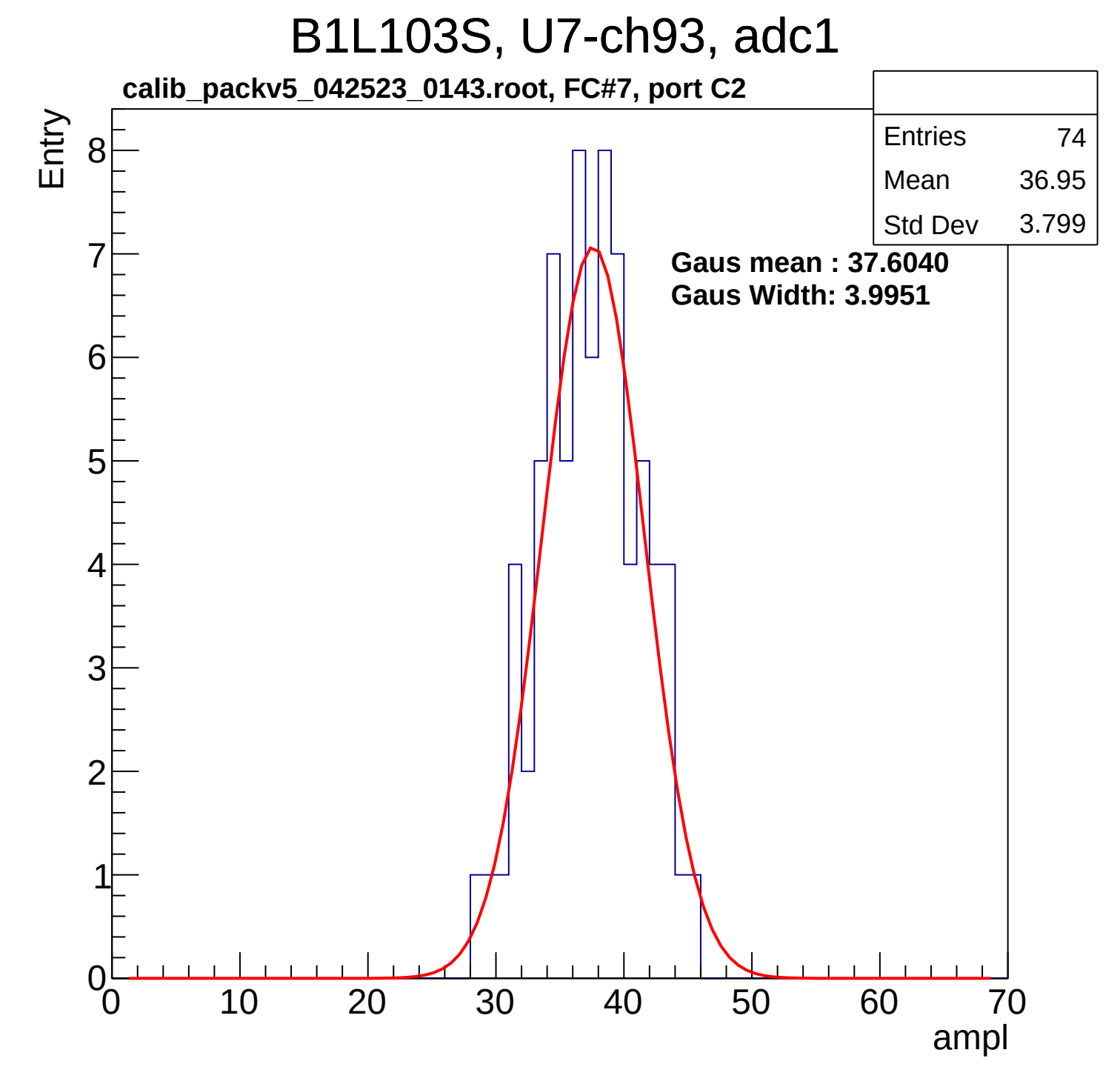
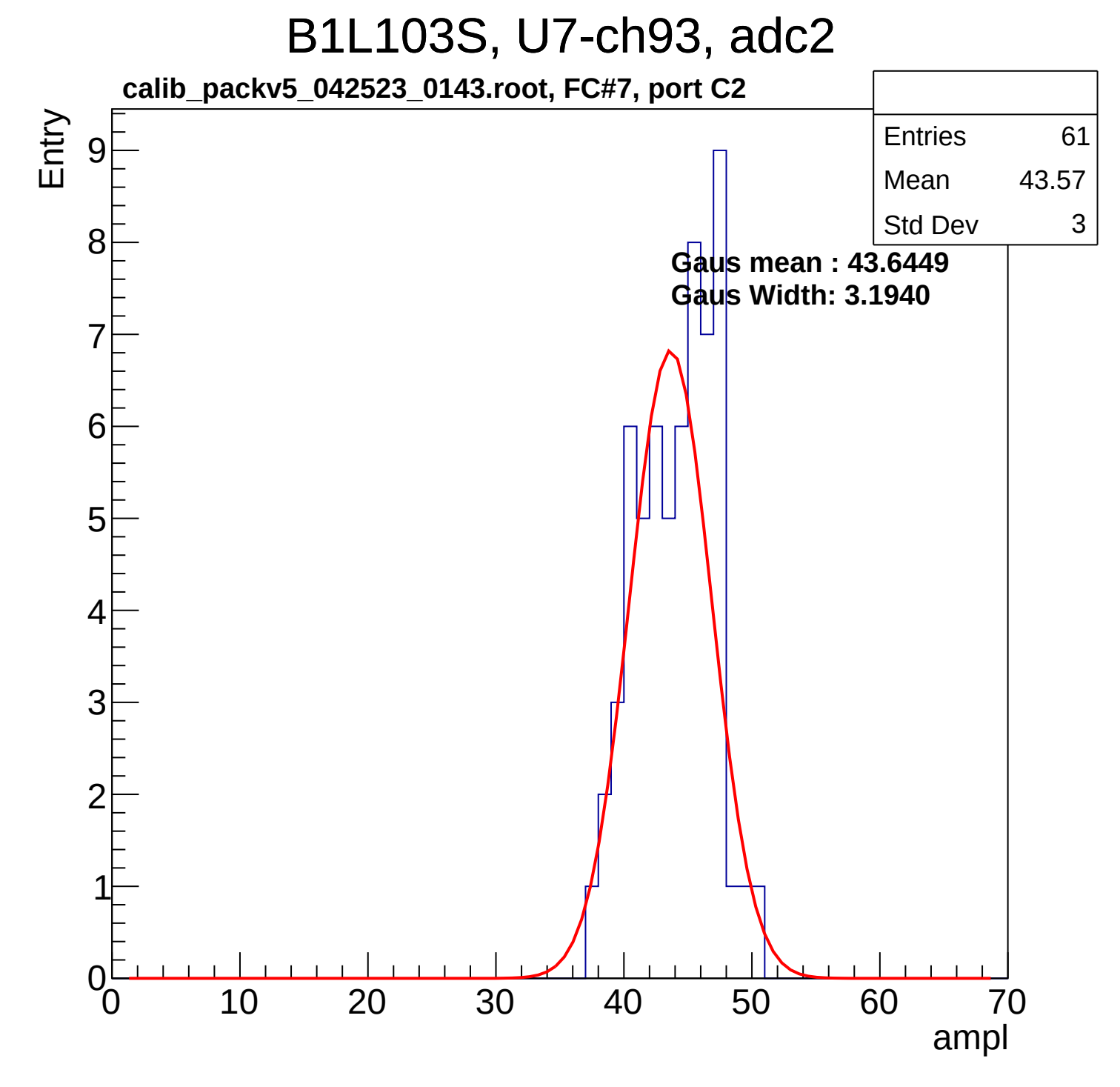
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

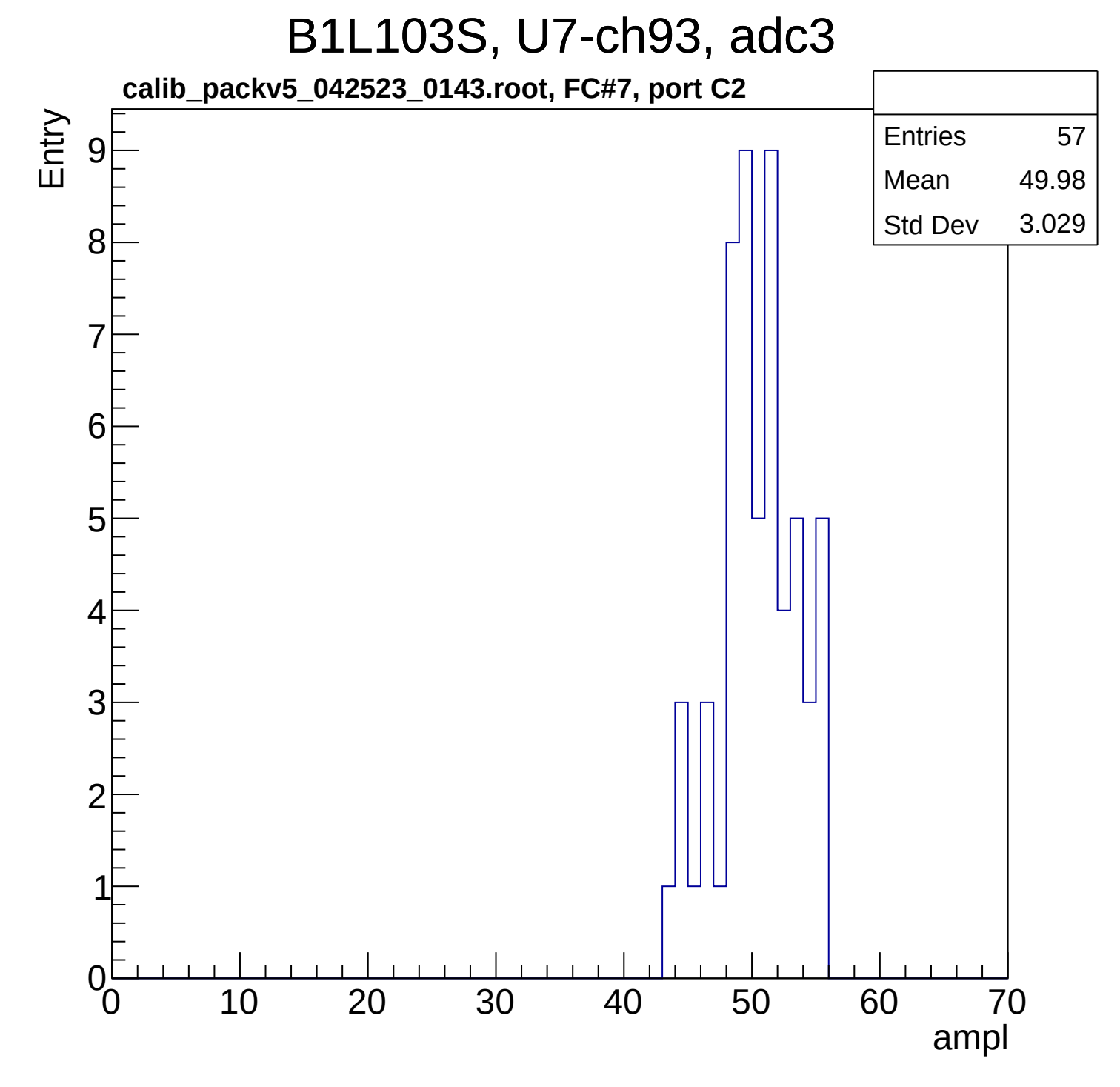

B1L103S, U7-ch92, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 26
Mean 58.19
Std Dev 11.86
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch92, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 8
Mean 23.38
Std Dev 30.18
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch93, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 71
Mean 29
Std Dev 6.983
Gaus mean : 31.0129
Gaus Width: 3.7233
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch93, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 74
Mean 36.95
Std Dev 3.799
Gaus mean : 37.6040
Gaus Width: 3.9951
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch93, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 61
Mean 43.57
Std Dev 3
Gaus mean : 43.6449
Gaus Width: 3.1940
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch93, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 49.98
Std Dev 3.029
Entry
ampl
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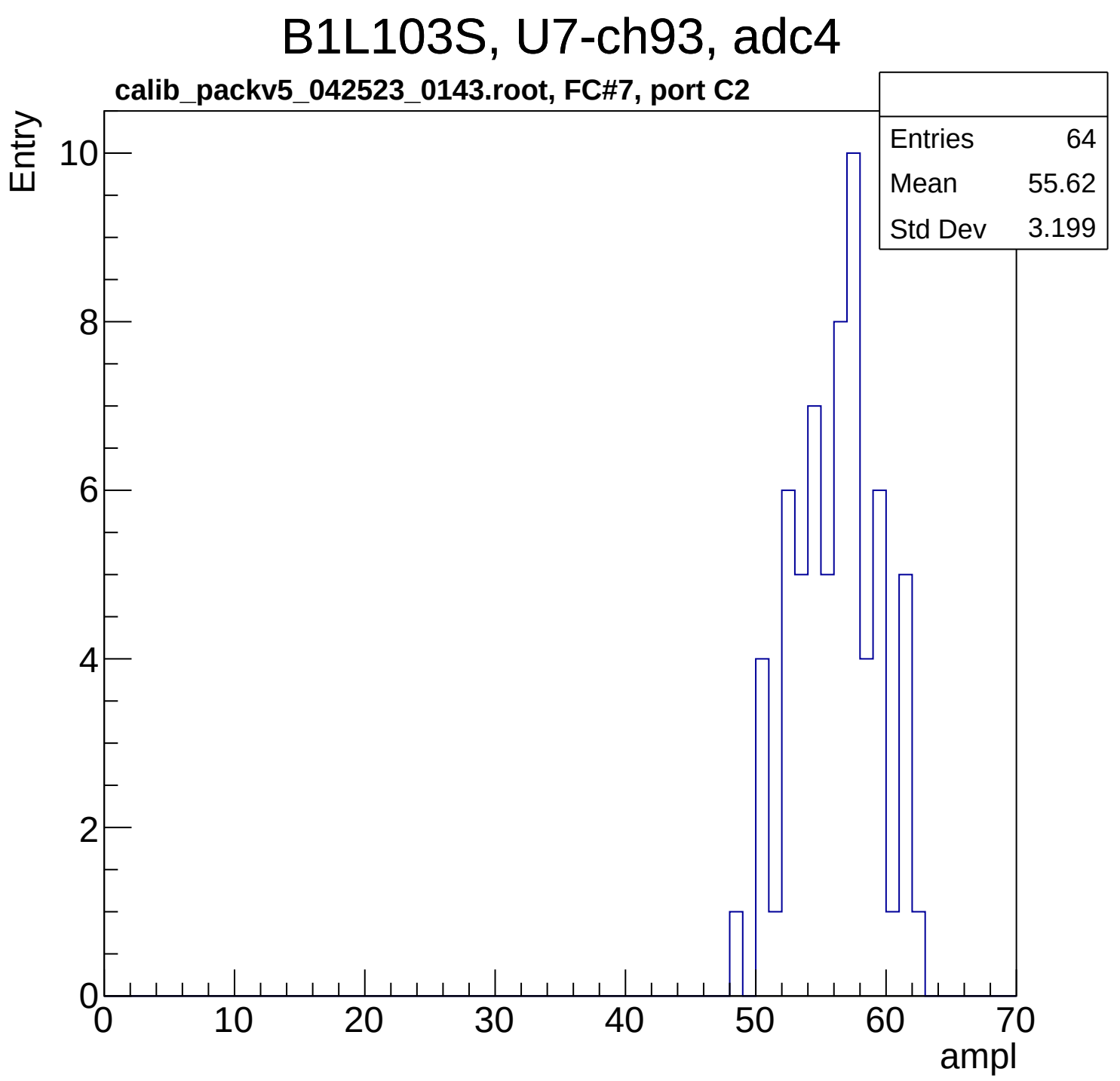
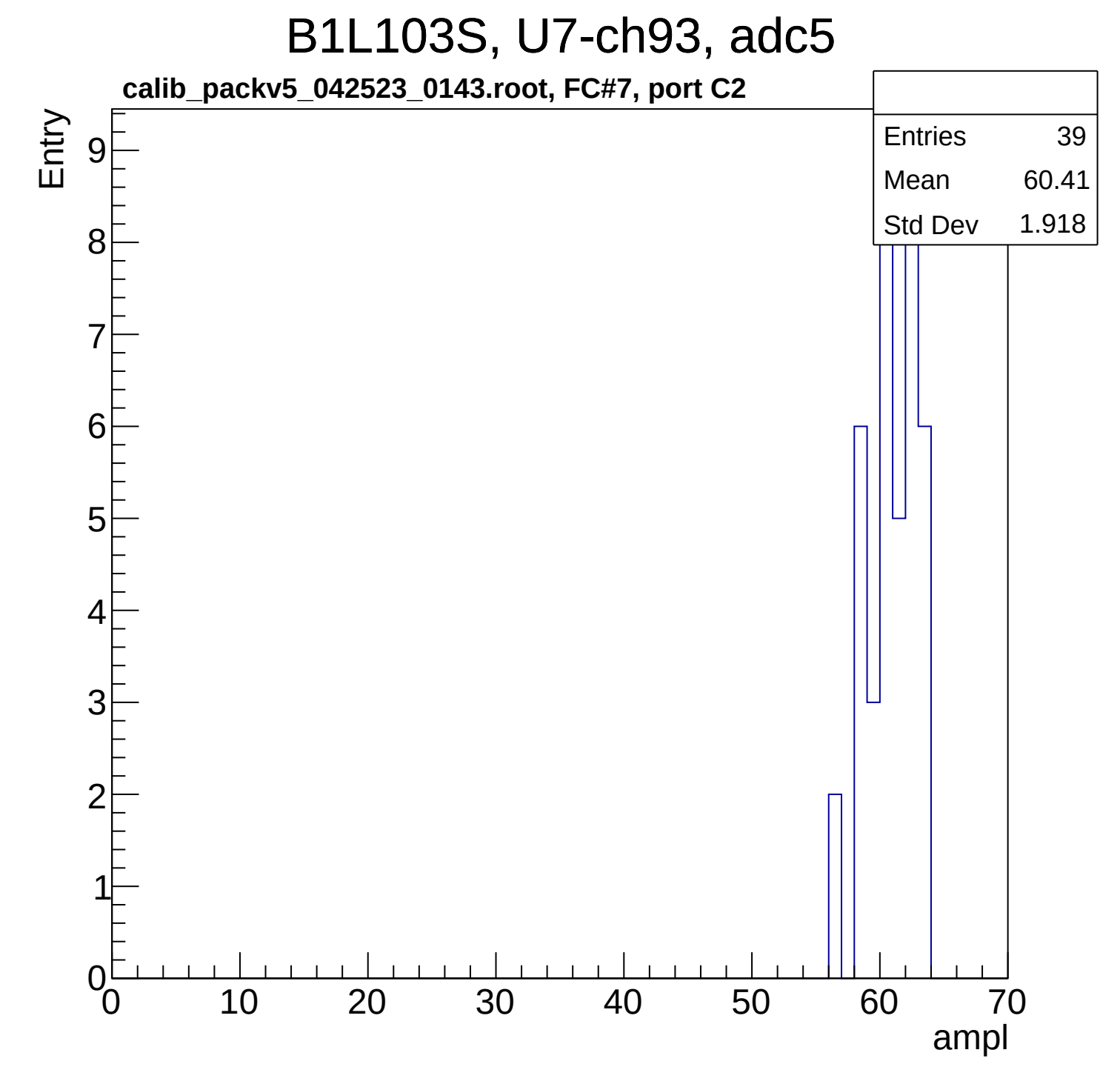
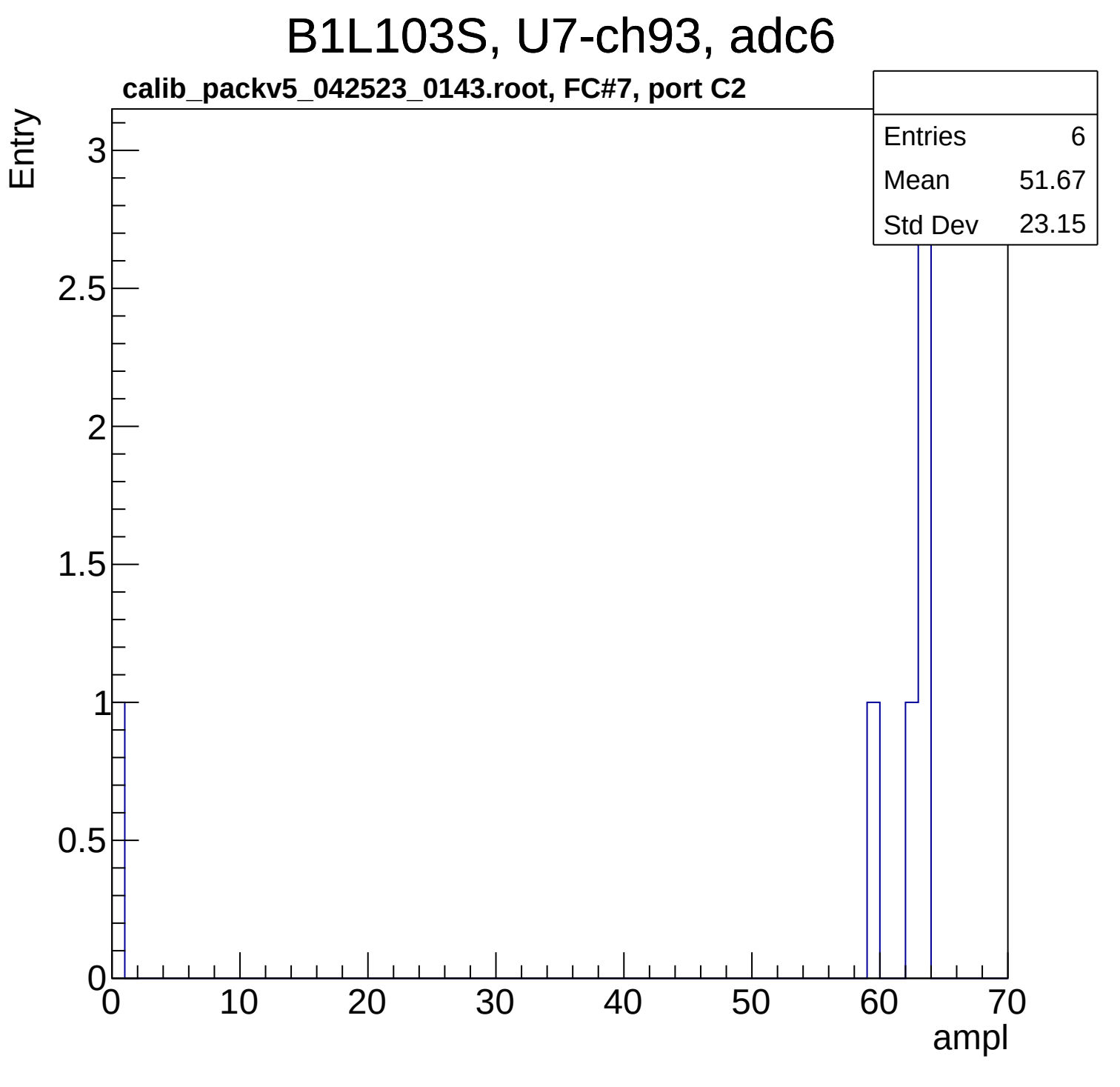
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch93, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 55.62
Std Dev 3.199
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch93, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 39
Mean 60.41
Std Dev 1.918
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch93, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 6
Mean 51.67
Std Dev 23.15
Entry
0
0.5
1
1.5
2
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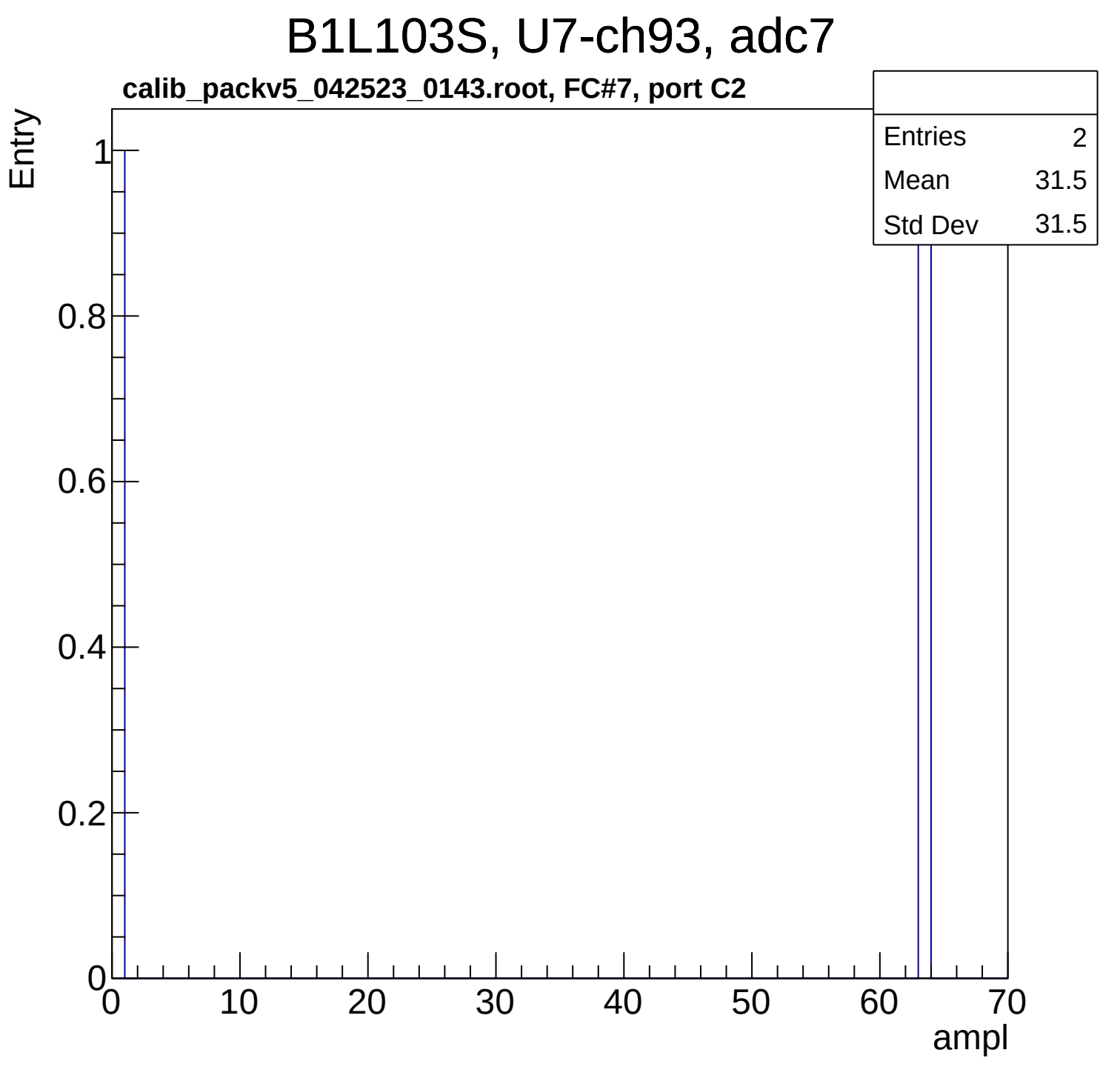
3
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch93, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 31.5
Std Dev 31.5
Entry
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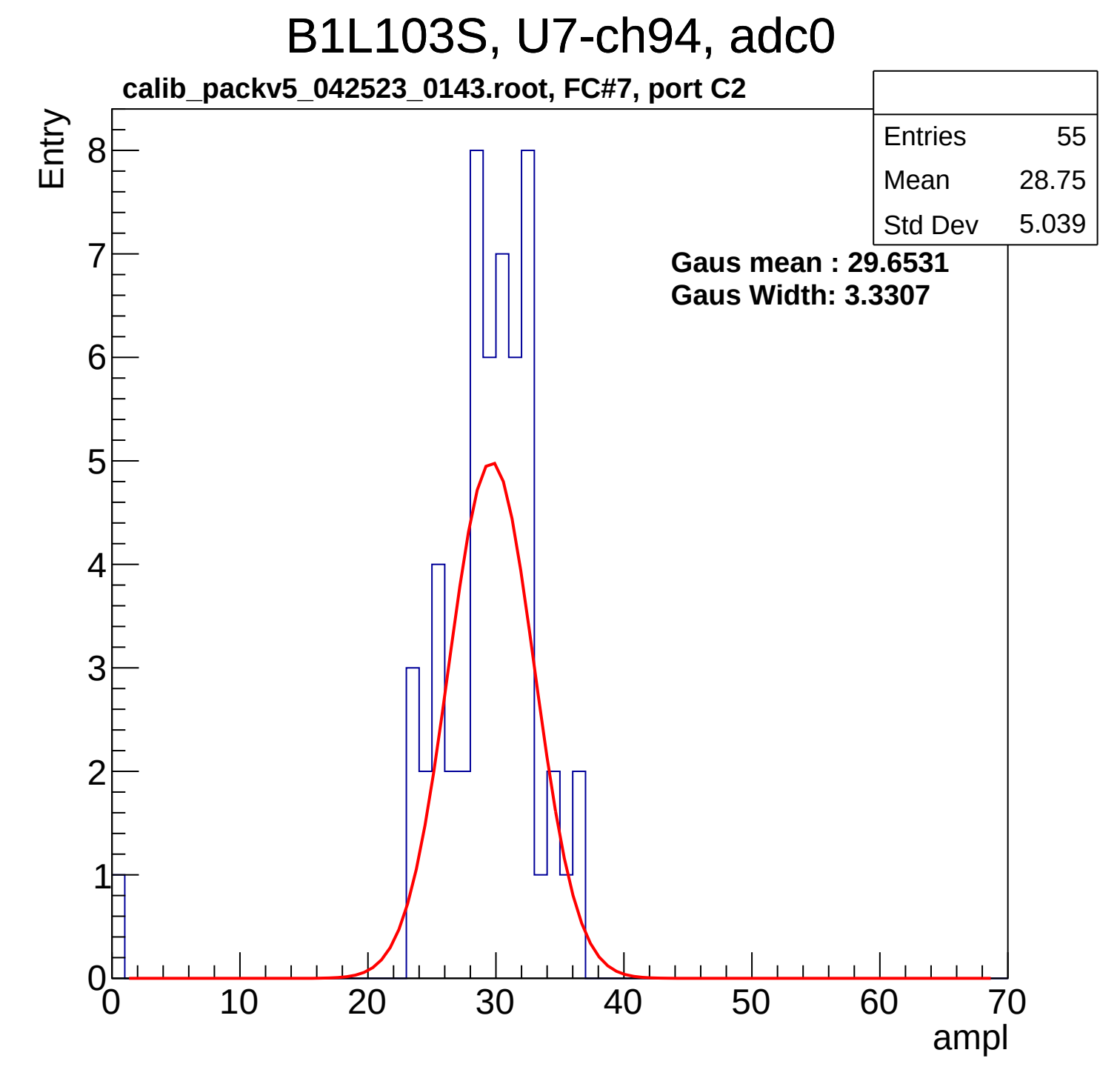
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch94, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 28.75
Std Dev 5.039
Gaus mean : 29.6531
Gaus Width: 3.3307
Entry
ampl
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1
2
3
4
5
6
7
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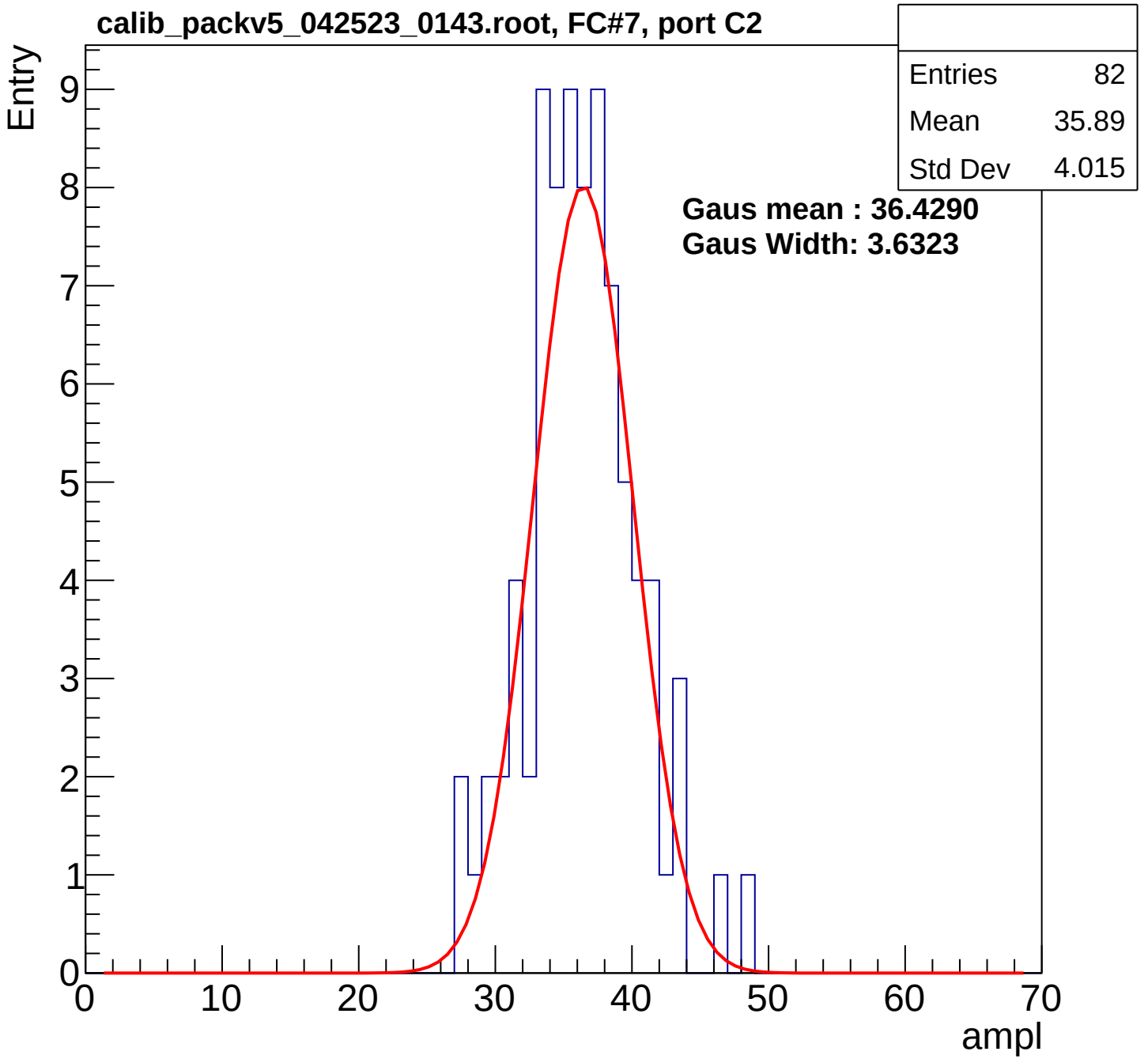
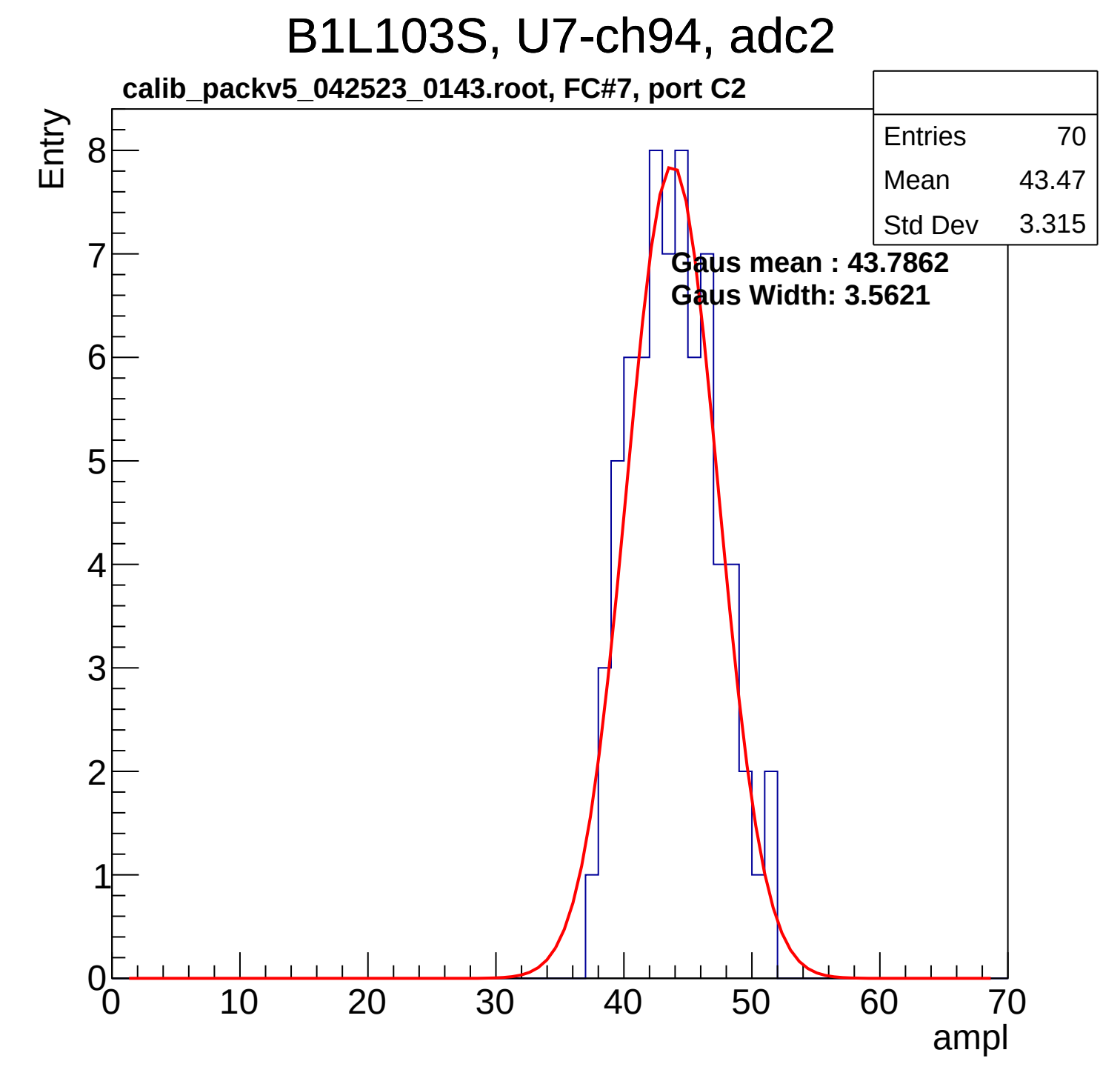
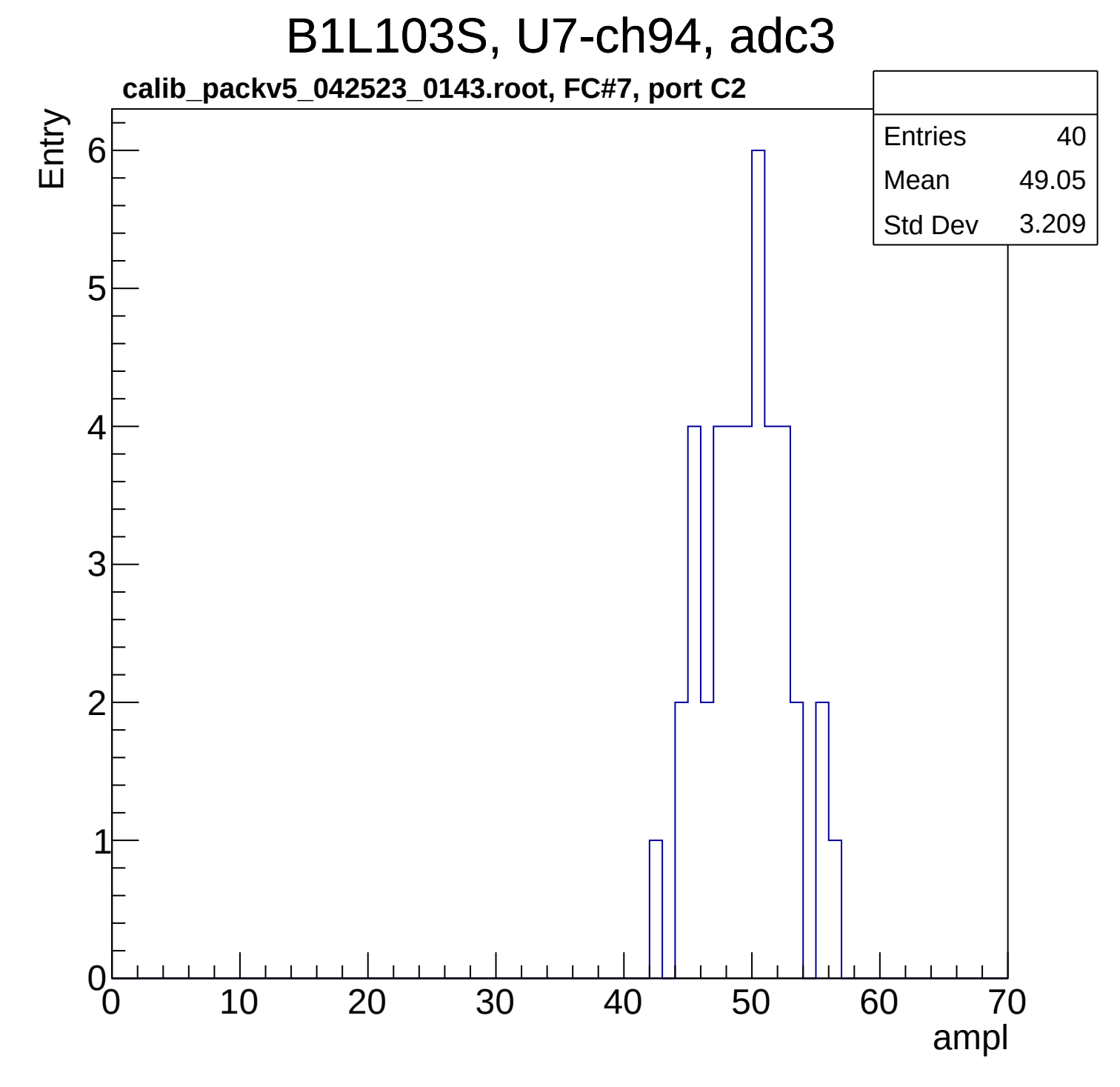
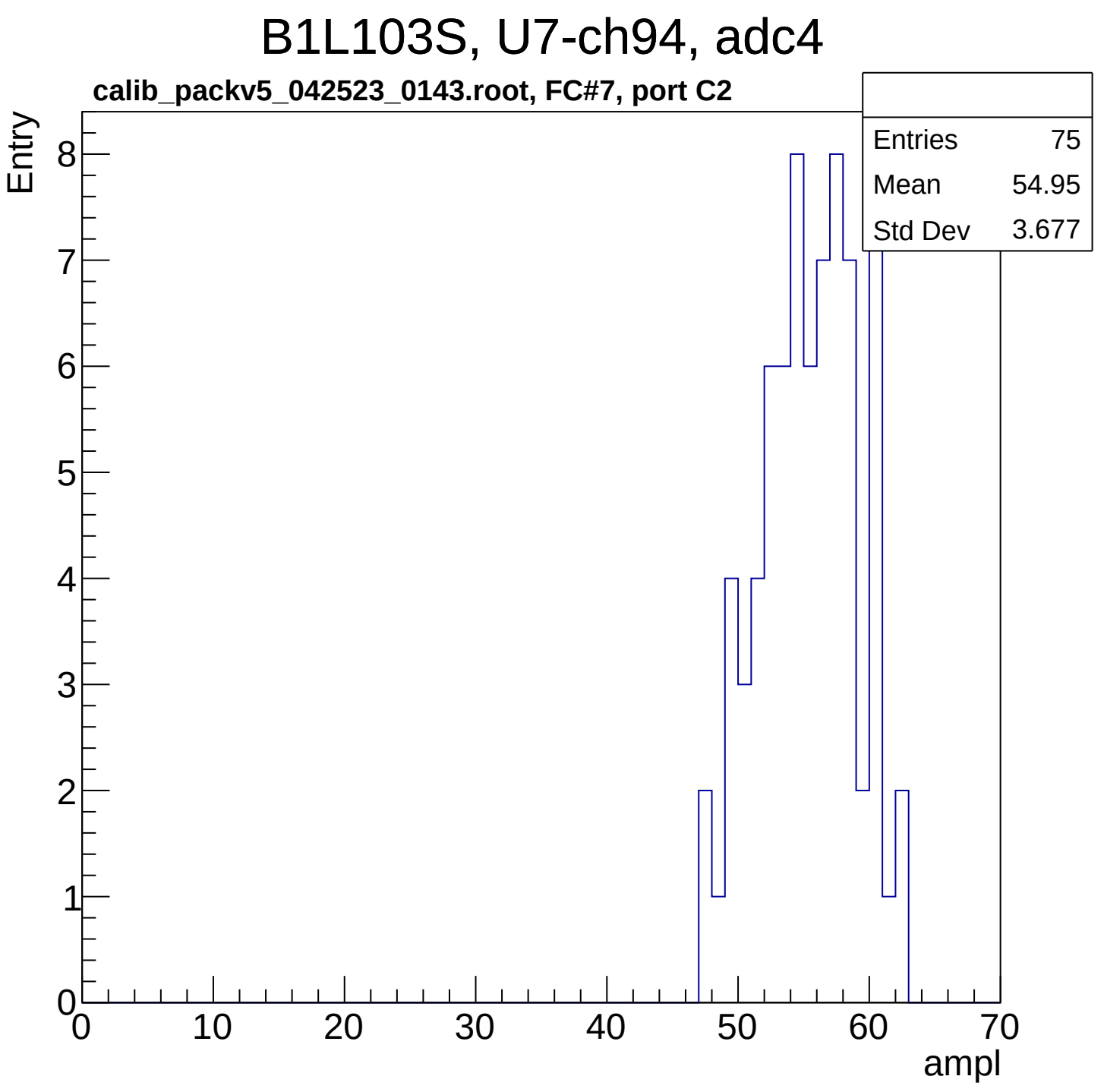
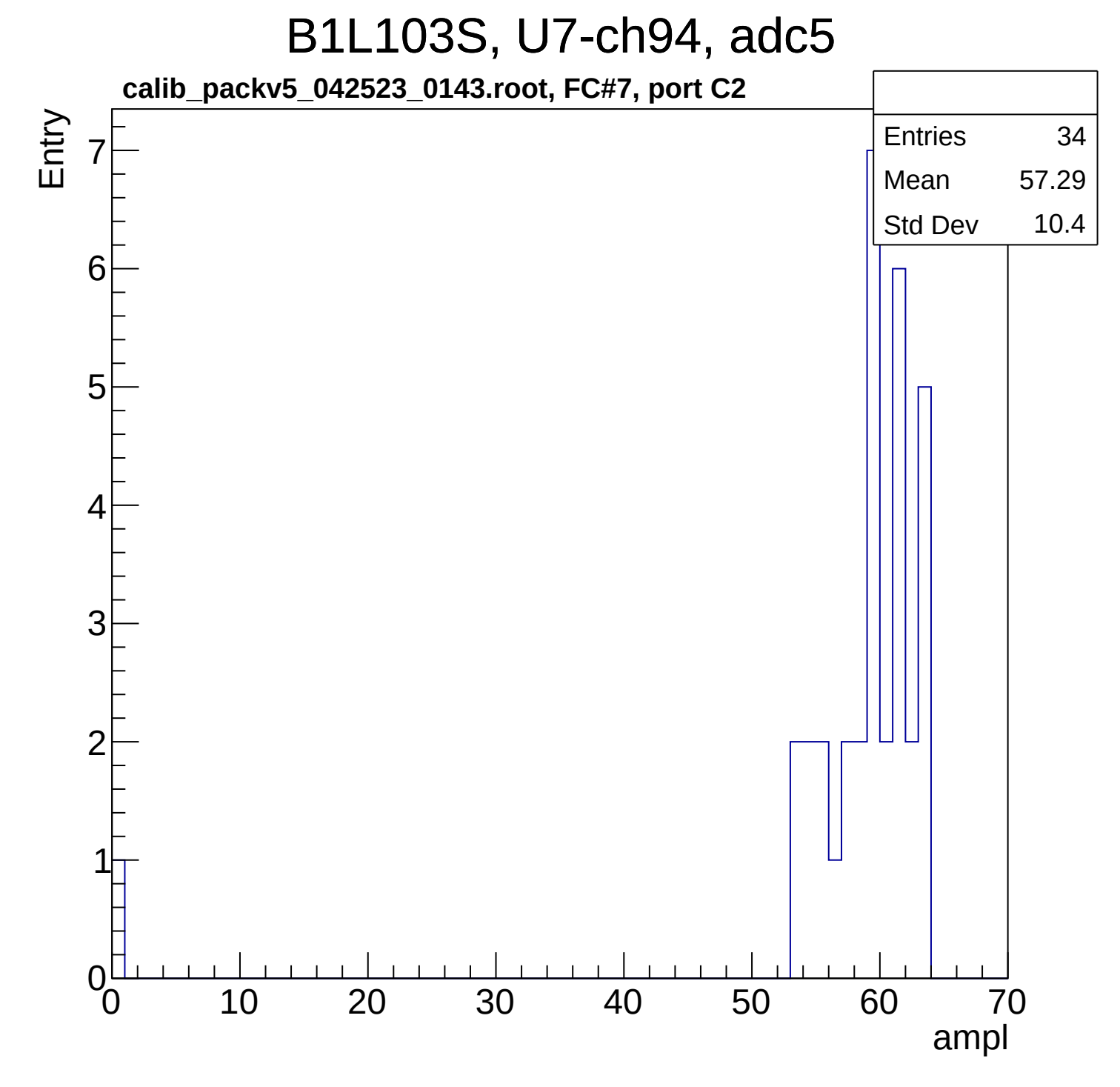
0
10
20
30
40
50
60
70

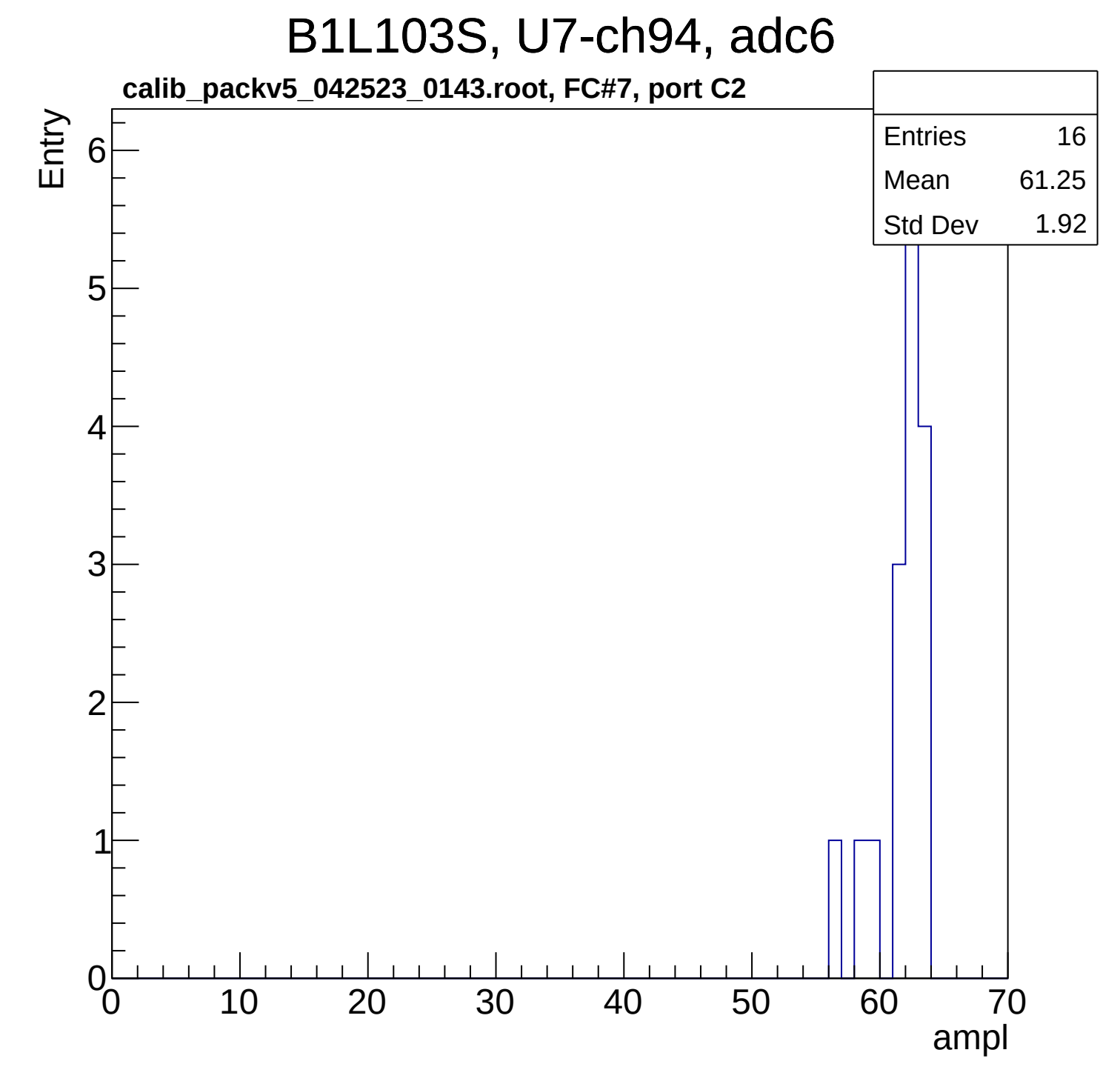

B1L103S, U7-ch94, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 82
Mean 35.89
Std Dev 4.015
Gaus mean : 36.4290
Gaus Width: 3.6323
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

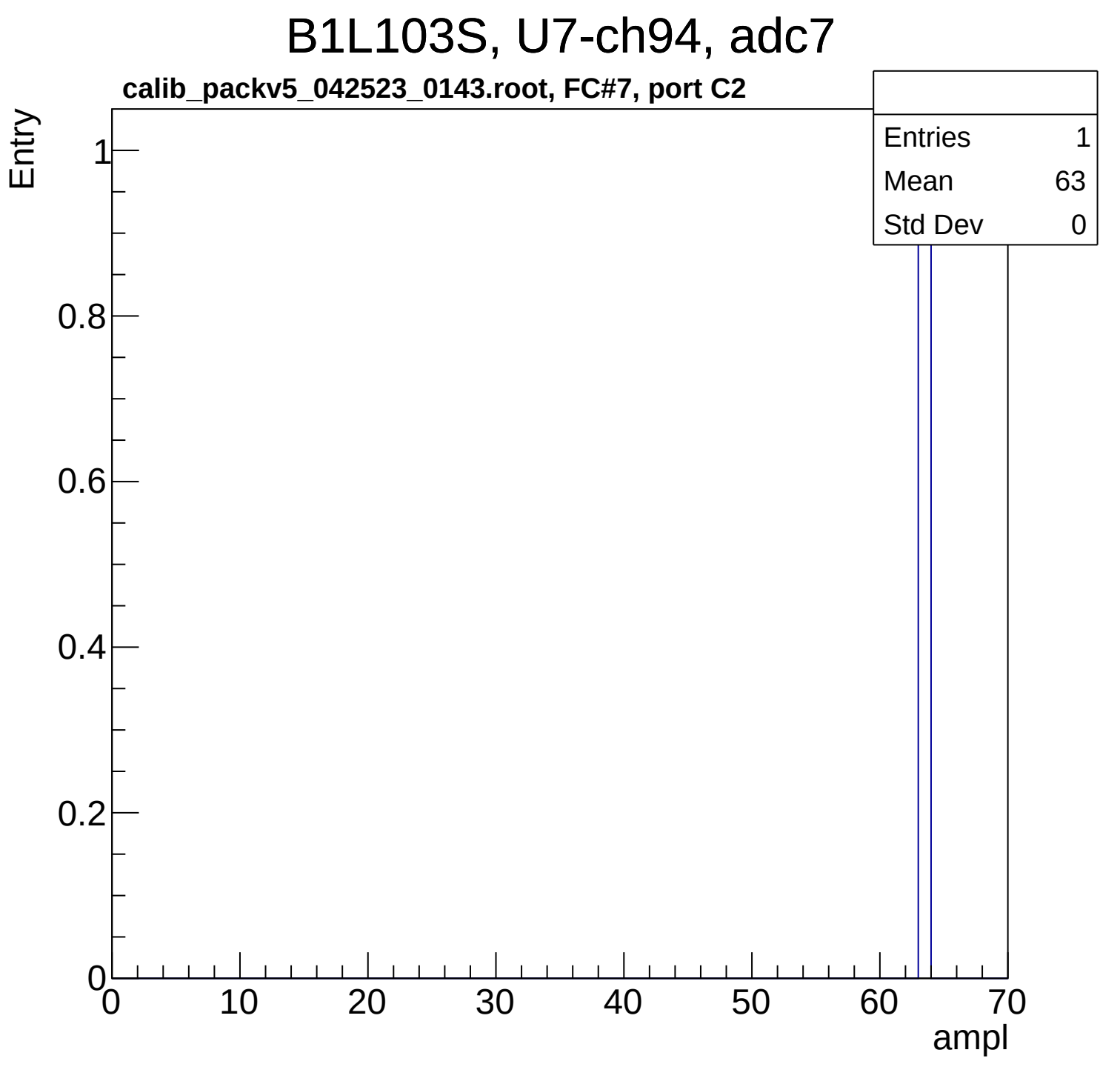

B1L103S, U7-ch94, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 43.47
Std Dev 3.315
Gaus mean : 43.7862
Gaus Width: 3.5621
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

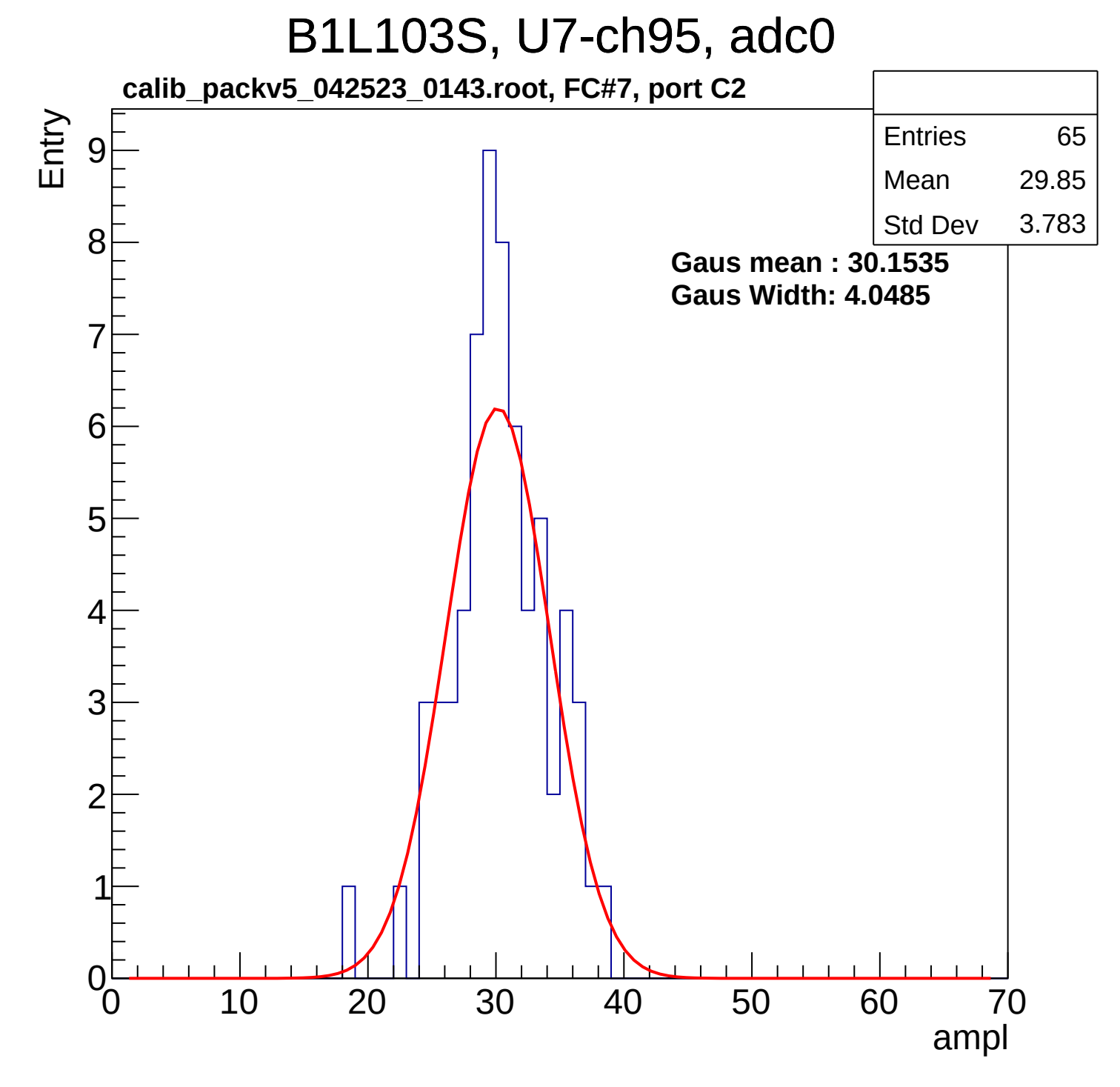

B1L103S, U7-ch94, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 40
Mean 49.05
Std Dev 3.209
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

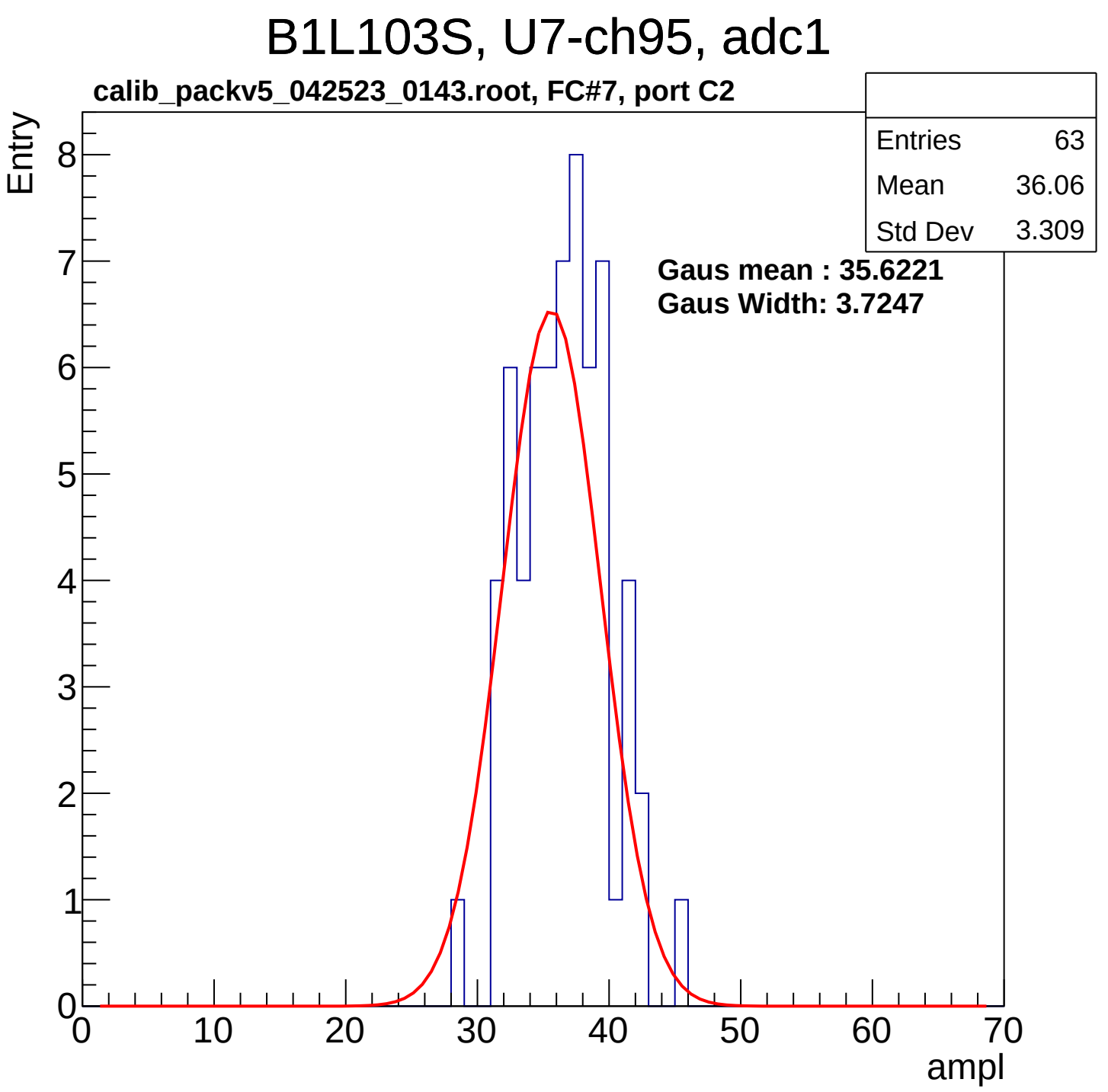

B1L103S, U7-ch94, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 75
Mean 54.95
Std Dev 3.677
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

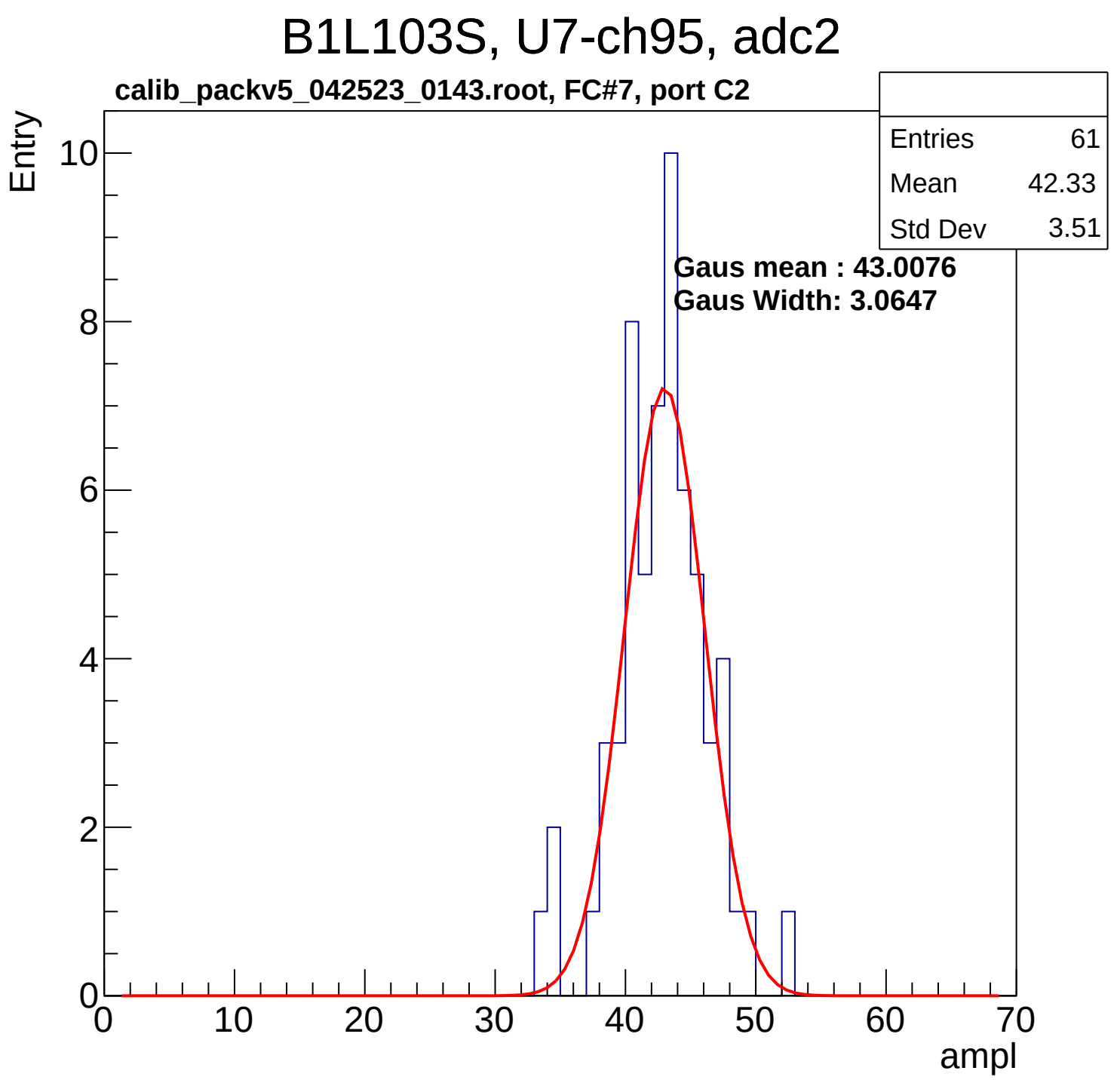

B1L103S, U7-ch94, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 34
Mean 57.29
Std Dev 10.4
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

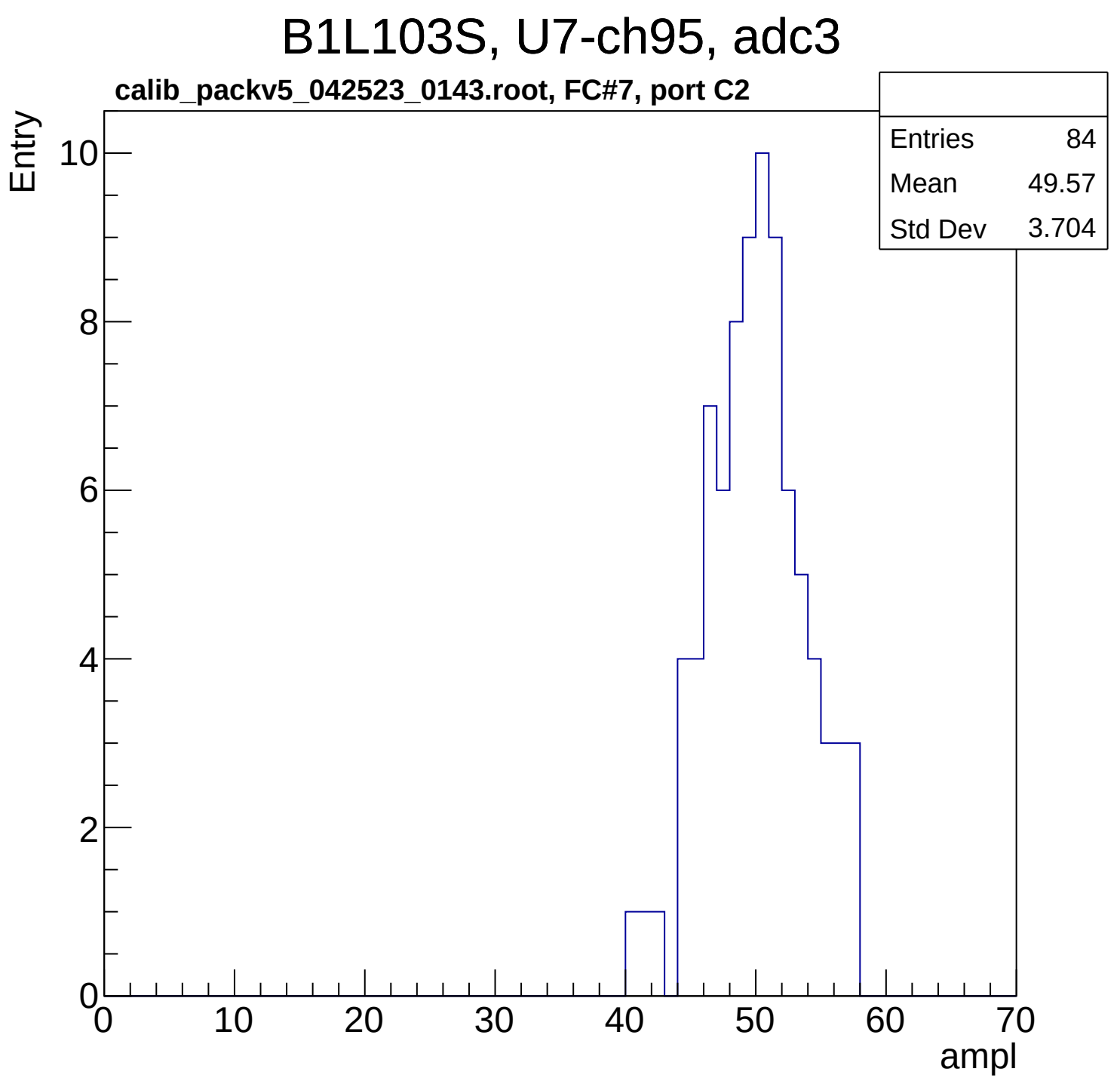

B1L103S, U7-ch94, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 16
Mean 61.25
Std Dev 1.92
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

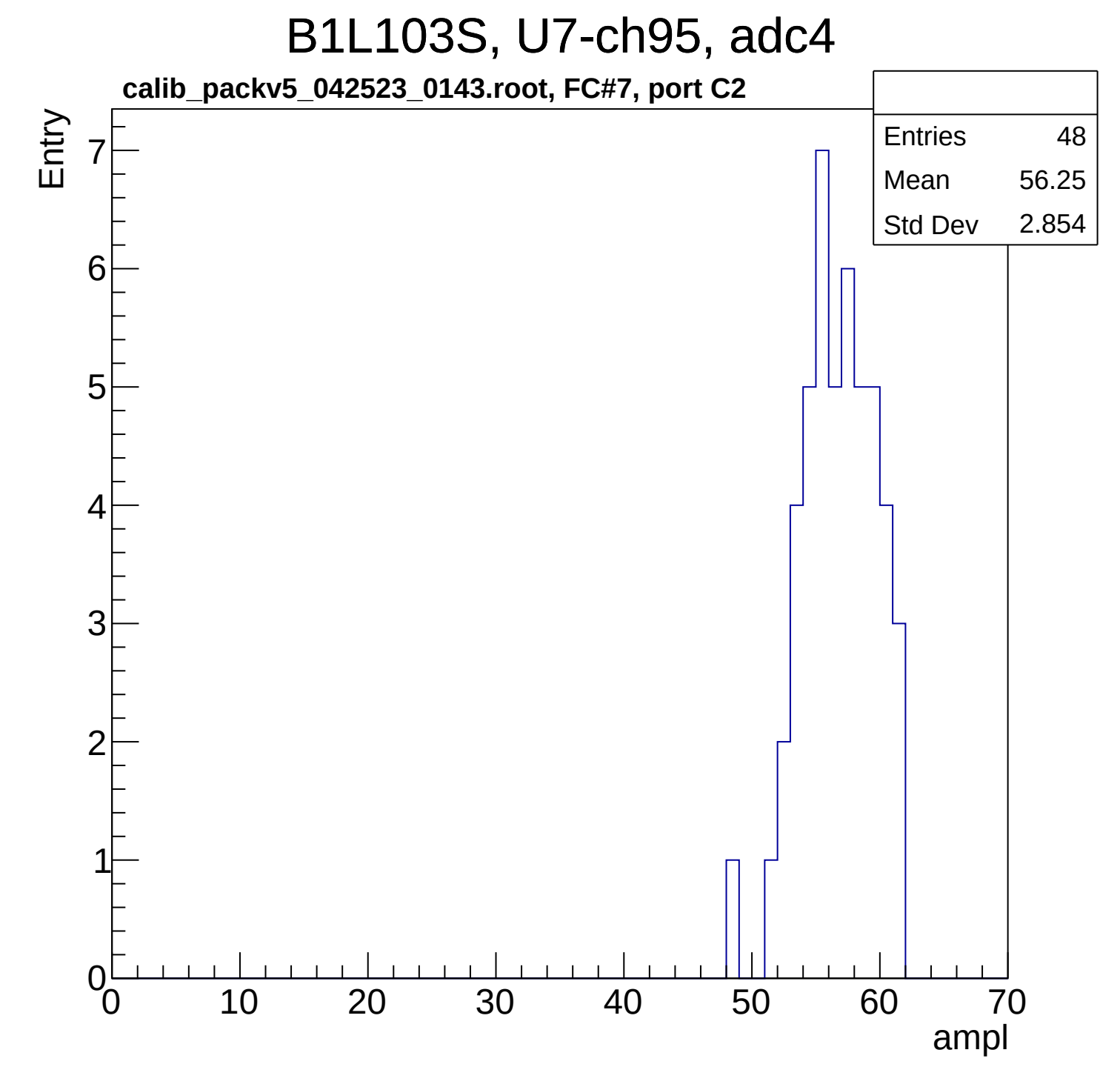

B1L103S, U7-ch94, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

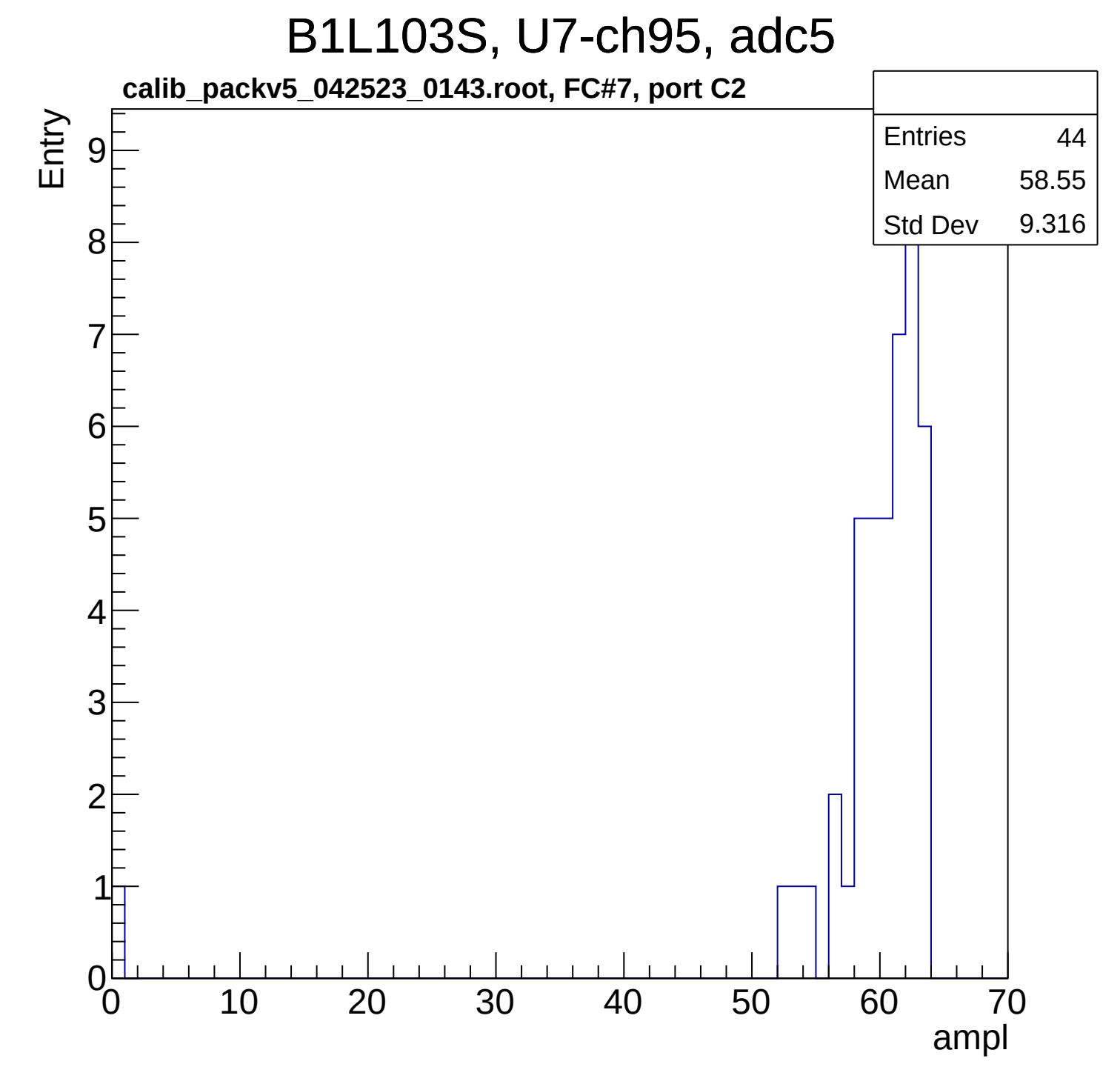

B1L103S, U7-ch95, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 29.85
Std Dev 3.783
Gaus mean : 30.1535
Gaus Width: 4.0485
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch95, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 36.06
Std Dev 3.309
Gaus mean : 35.6221
Gaus Width: 3.7247
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch95, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 61
Mean 42.33
Std Dev 3.51
Gaus mean : 43.0076
Gaus Width: 3.0647
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch95, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 84
Mean 49.57
Std Dev 3.704
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch95, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 48
Mean 56.25
Std Dev 2.854
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch95, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 44
Mean 58.55
Std Dev 9.316
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
10
20
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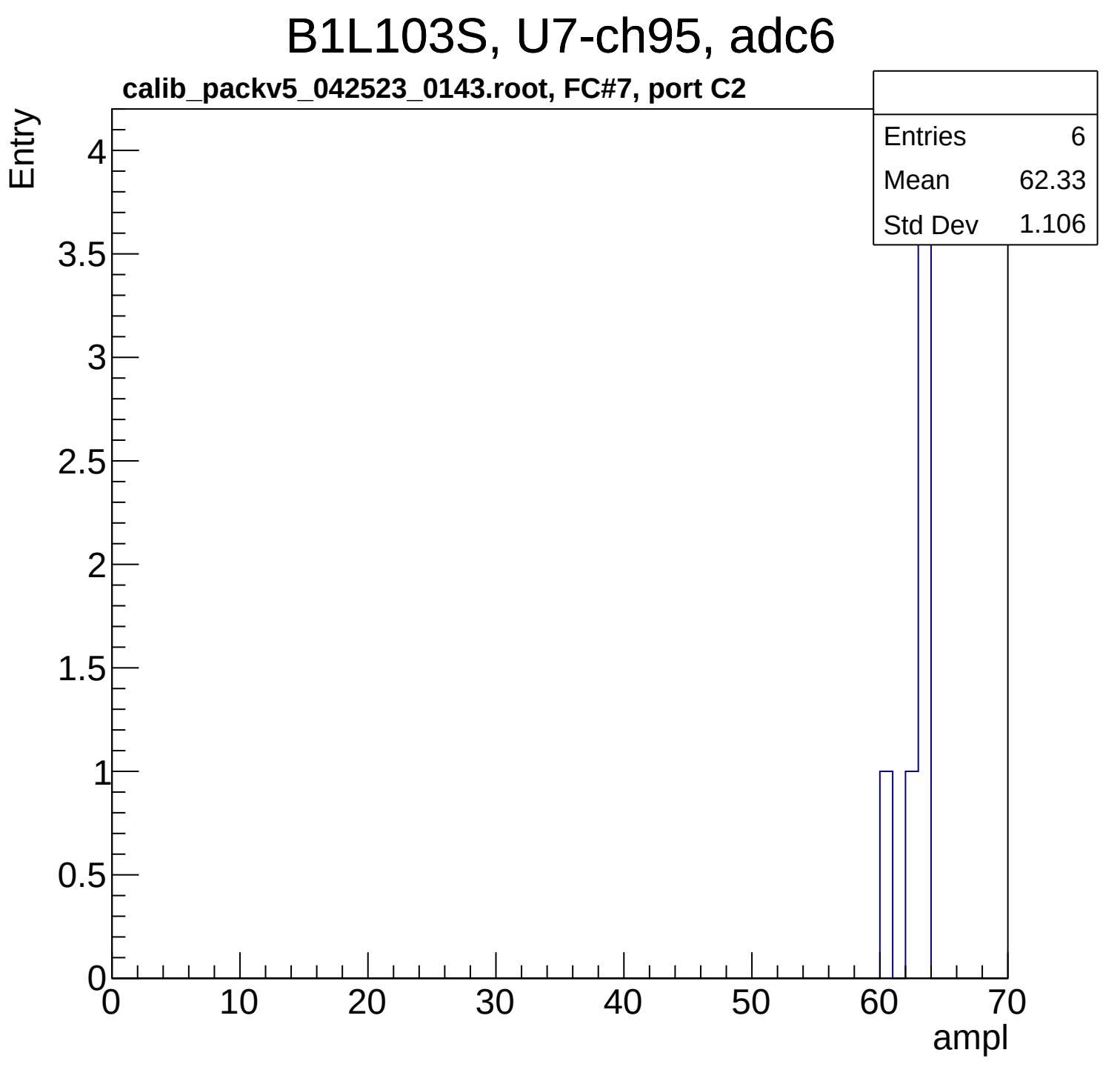
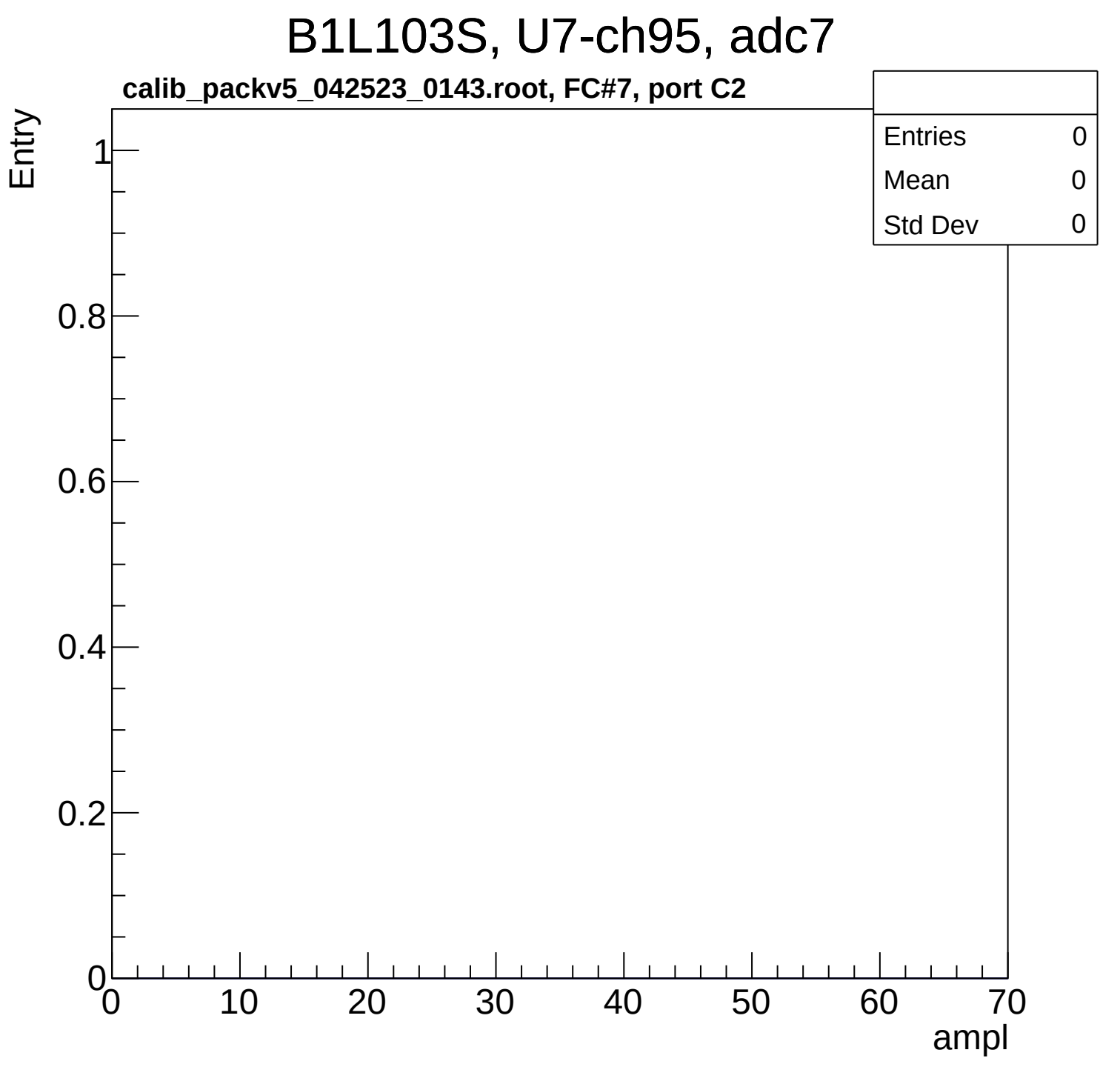
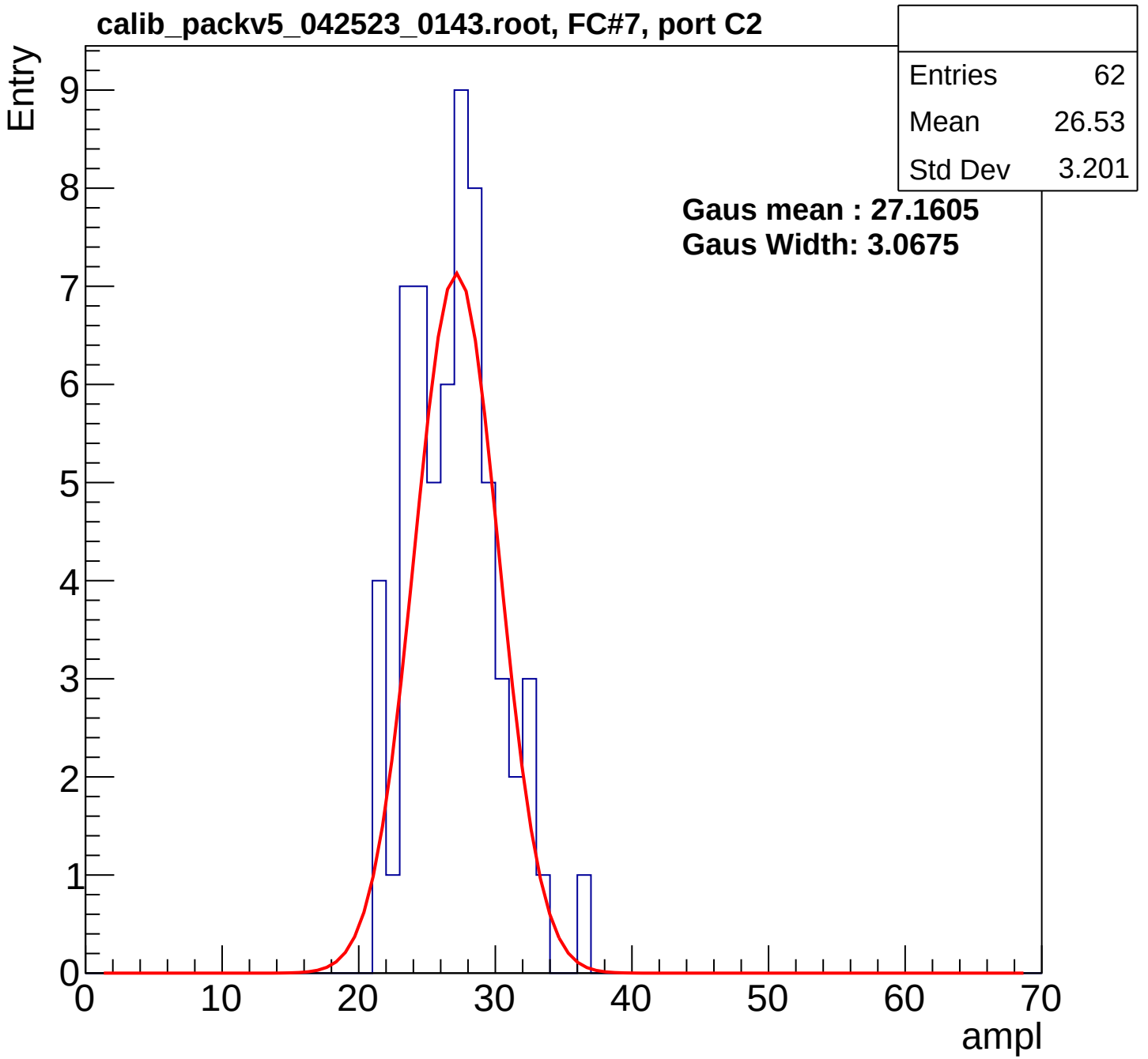
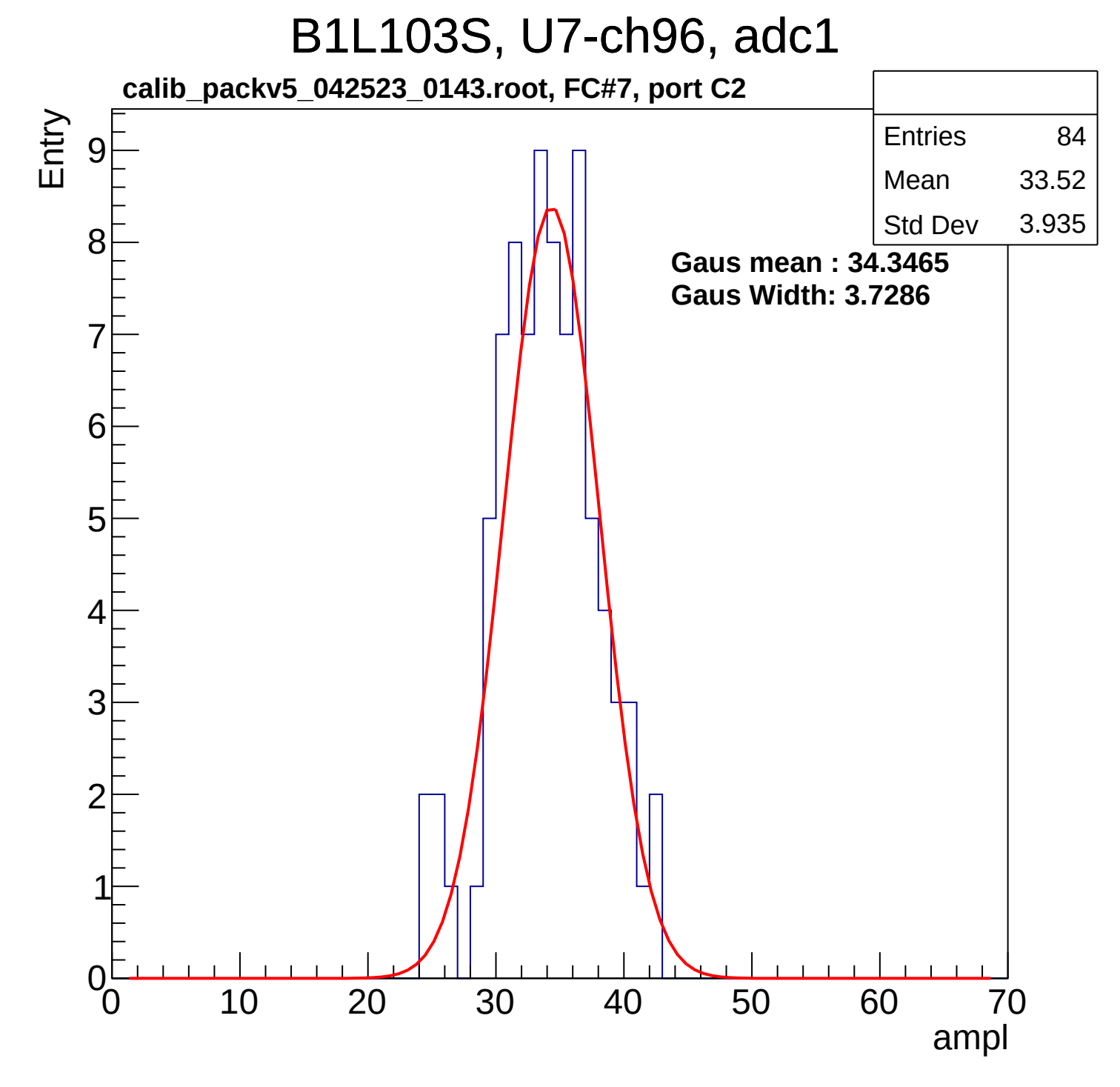
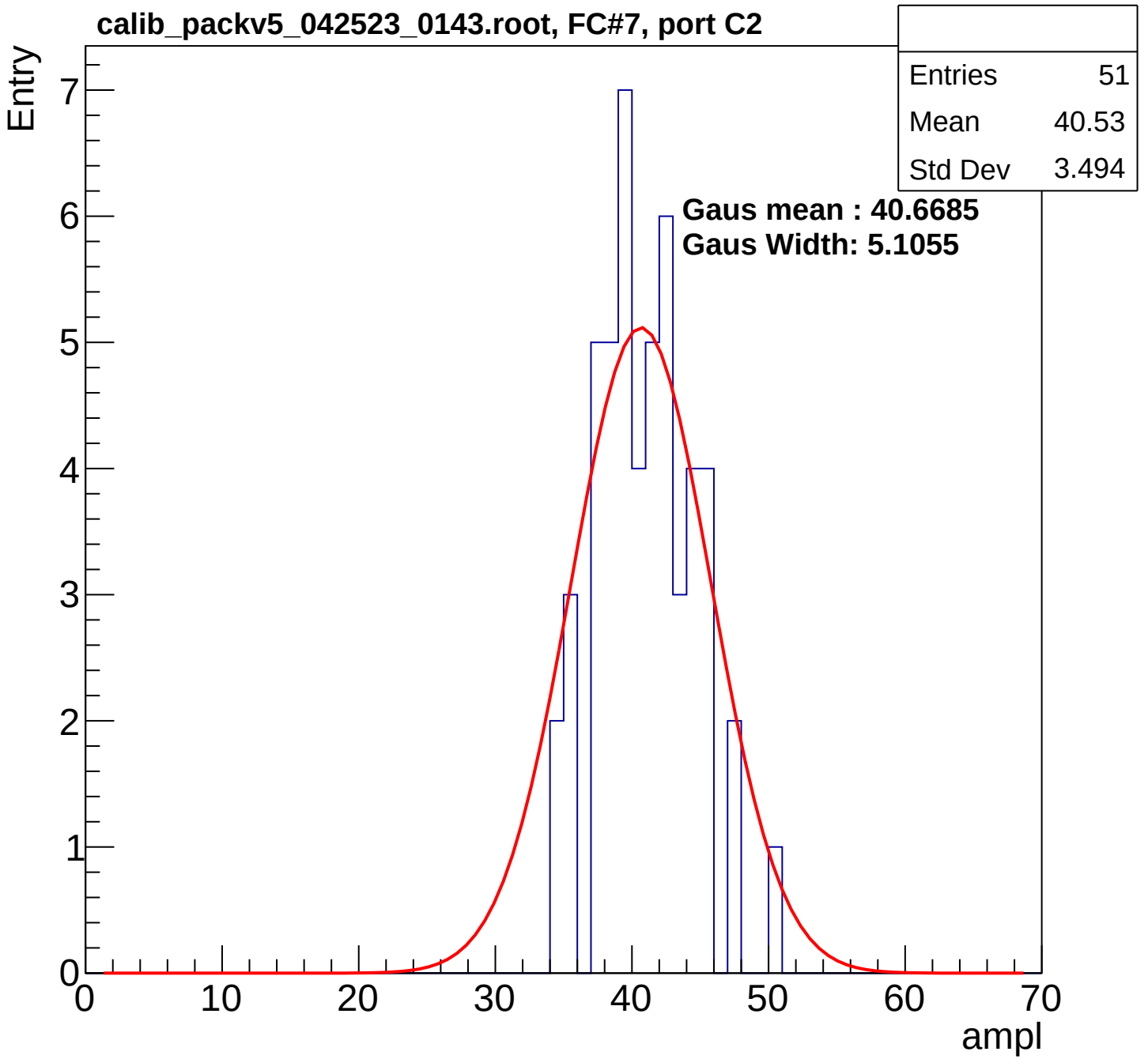
50
60
70

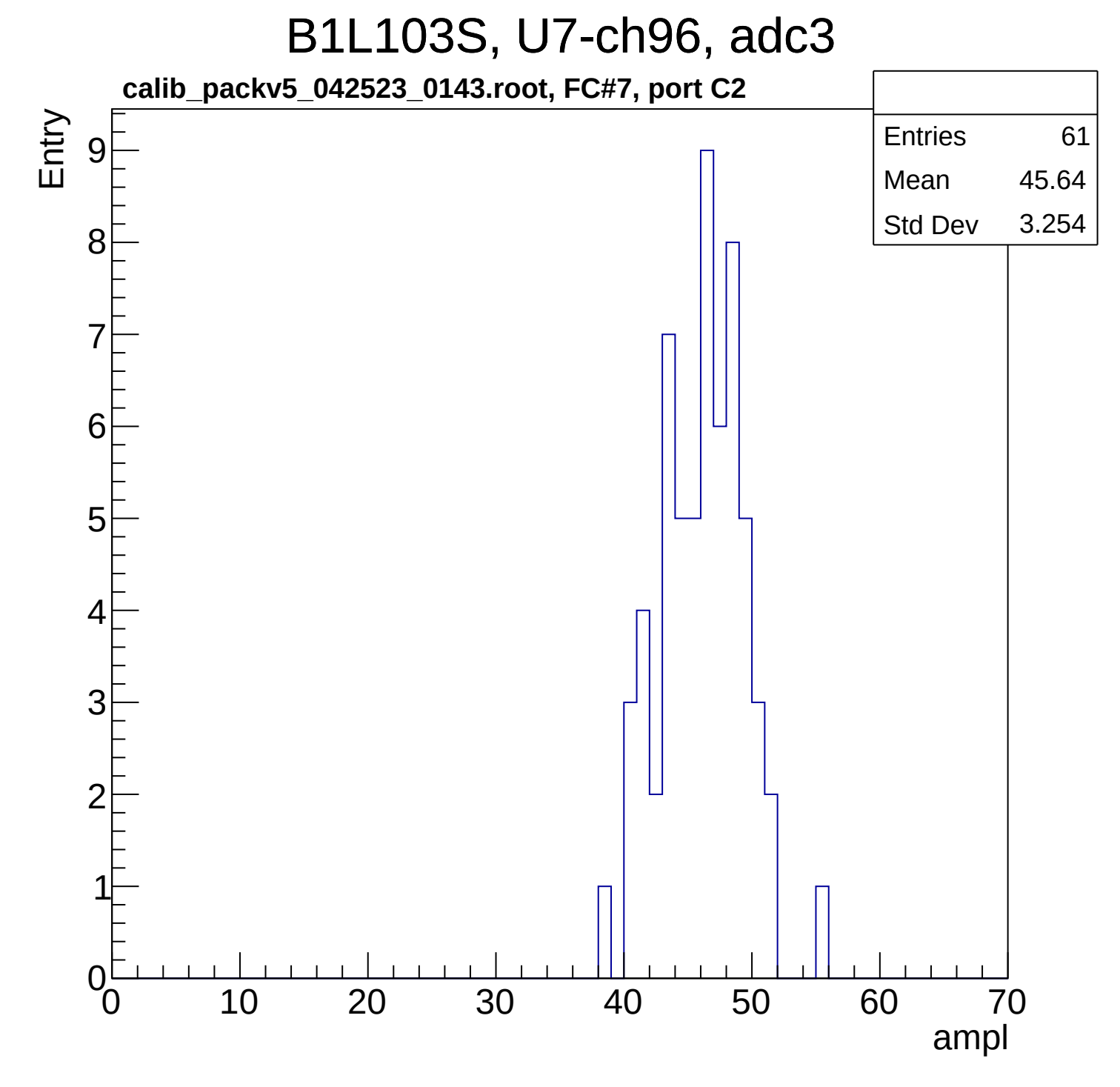

B1L103S, U7-ch95, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 6
Mean 62.33
Std Dev 1.106
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

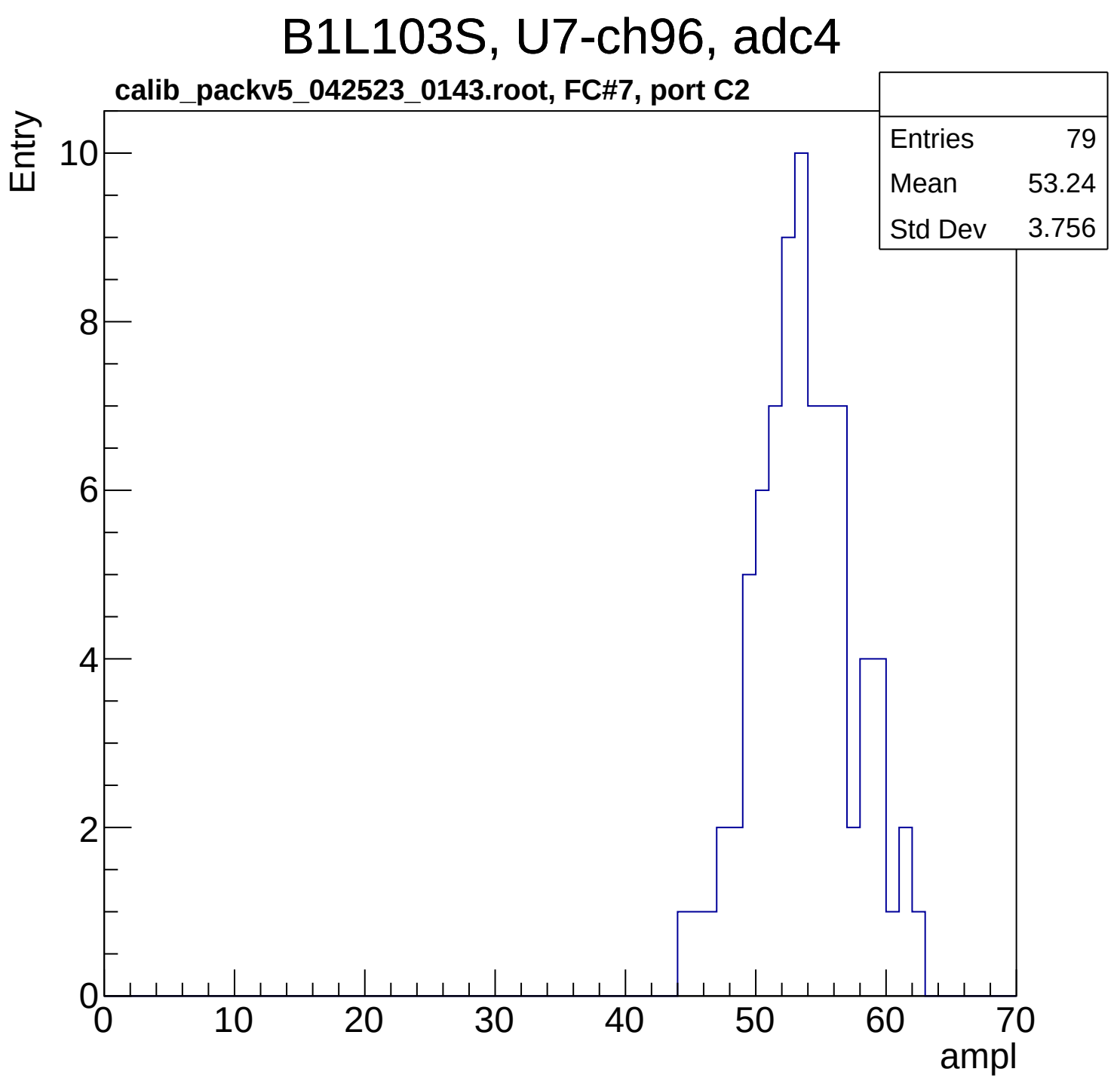

B1L103S, U7-ch95, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

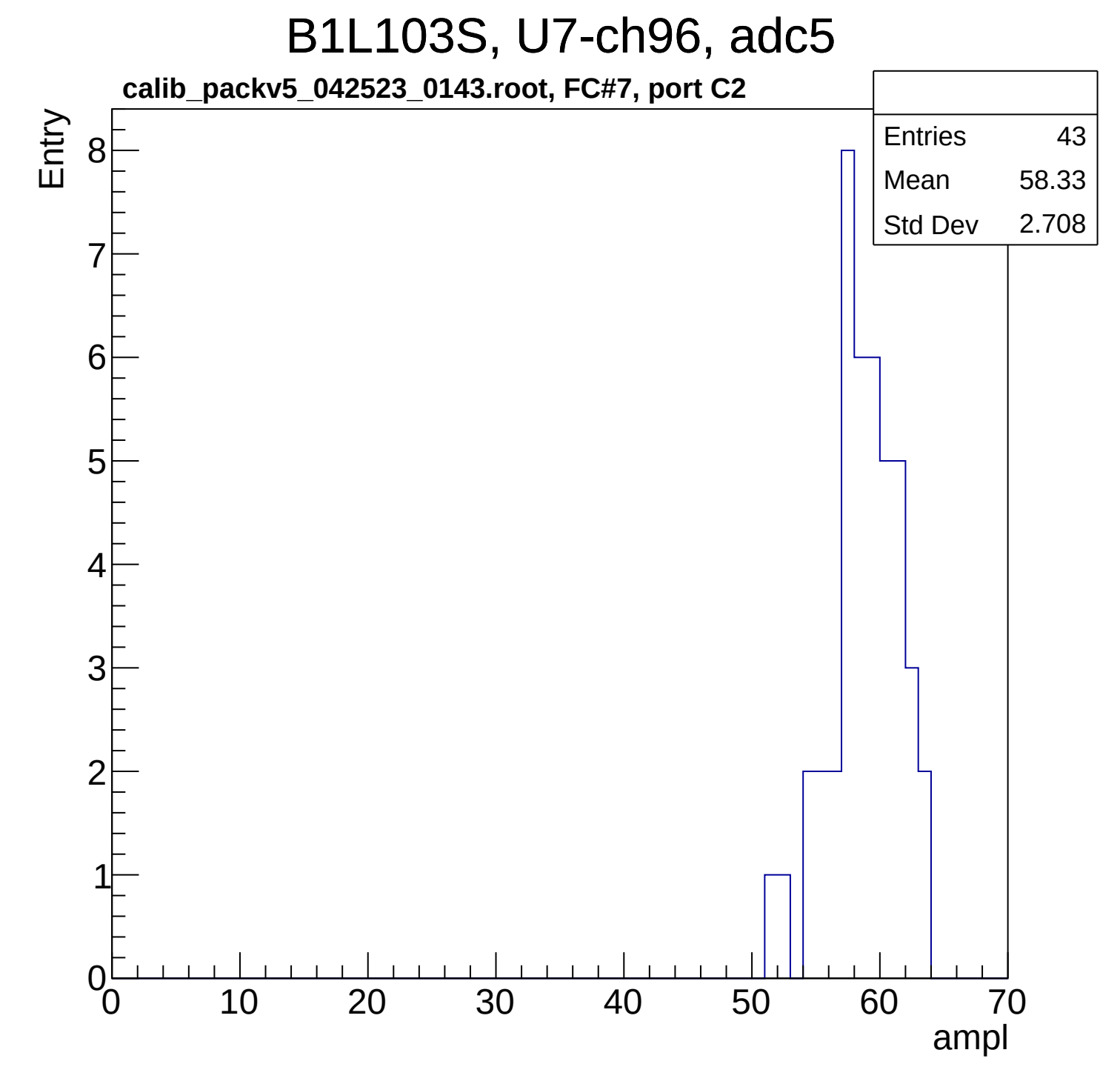

B1L103S, U7-ch96, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 62
Mean 26.53
Std Dev 3.201
Gaus mean : 27.1605
Gaus Width: 3.0675
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch96, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 84
Mean 33.52
Std Dev 3.935
Gaus mean : 34.3465
Gaus Width: 3.7286
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch96, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 51
Mean 40.53
Std Dev 3.494
Gaus mean : 40.6685
Gaus Width: 5.1055
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch96, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 61
Mean 45.64
Std Dev 3.254
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch96, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 79
Mean 53.24
Std Dev 3.756
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch96, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 43
Mean 58.33
Std Dev 2.708
Entry
ampl
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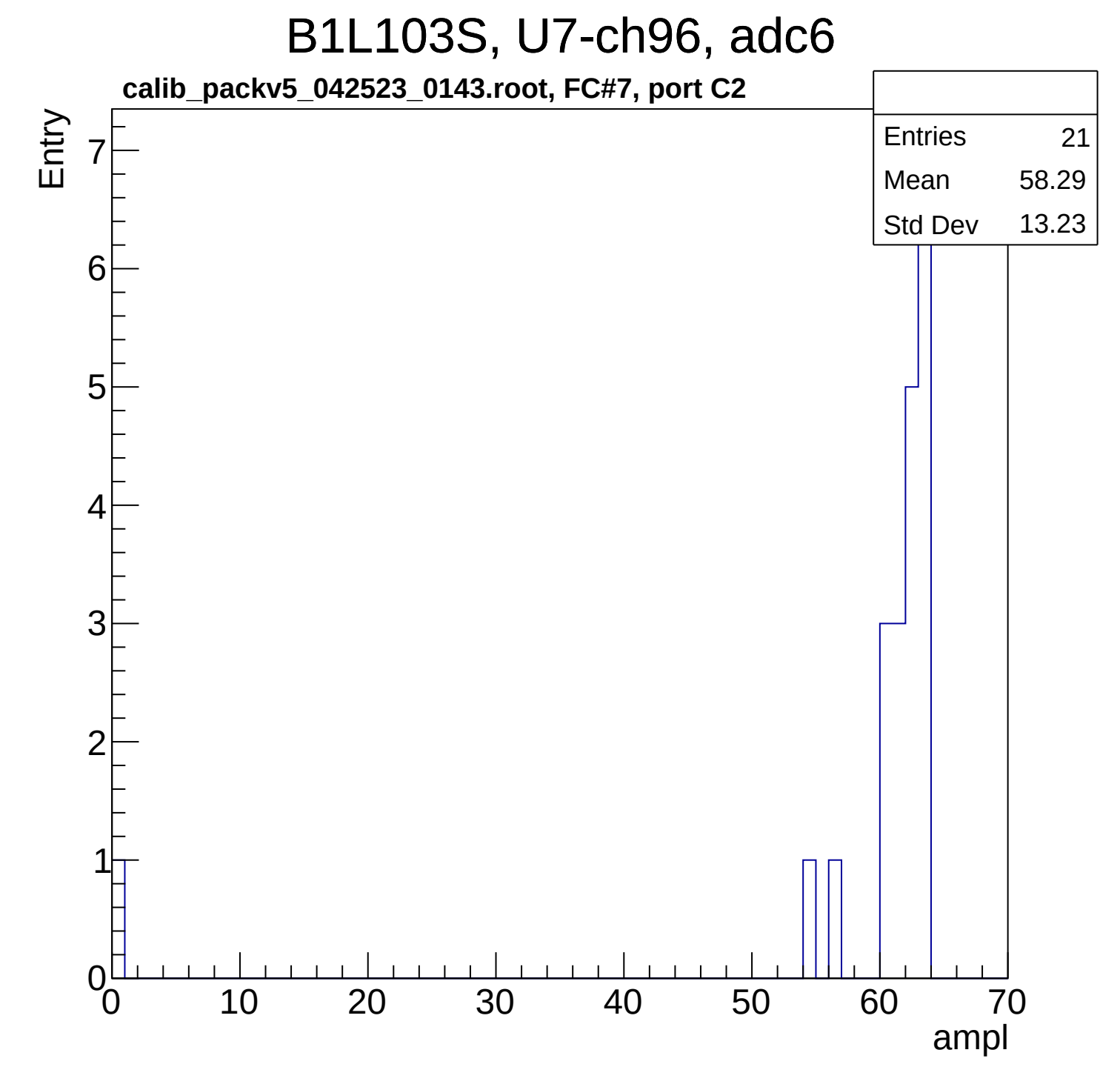
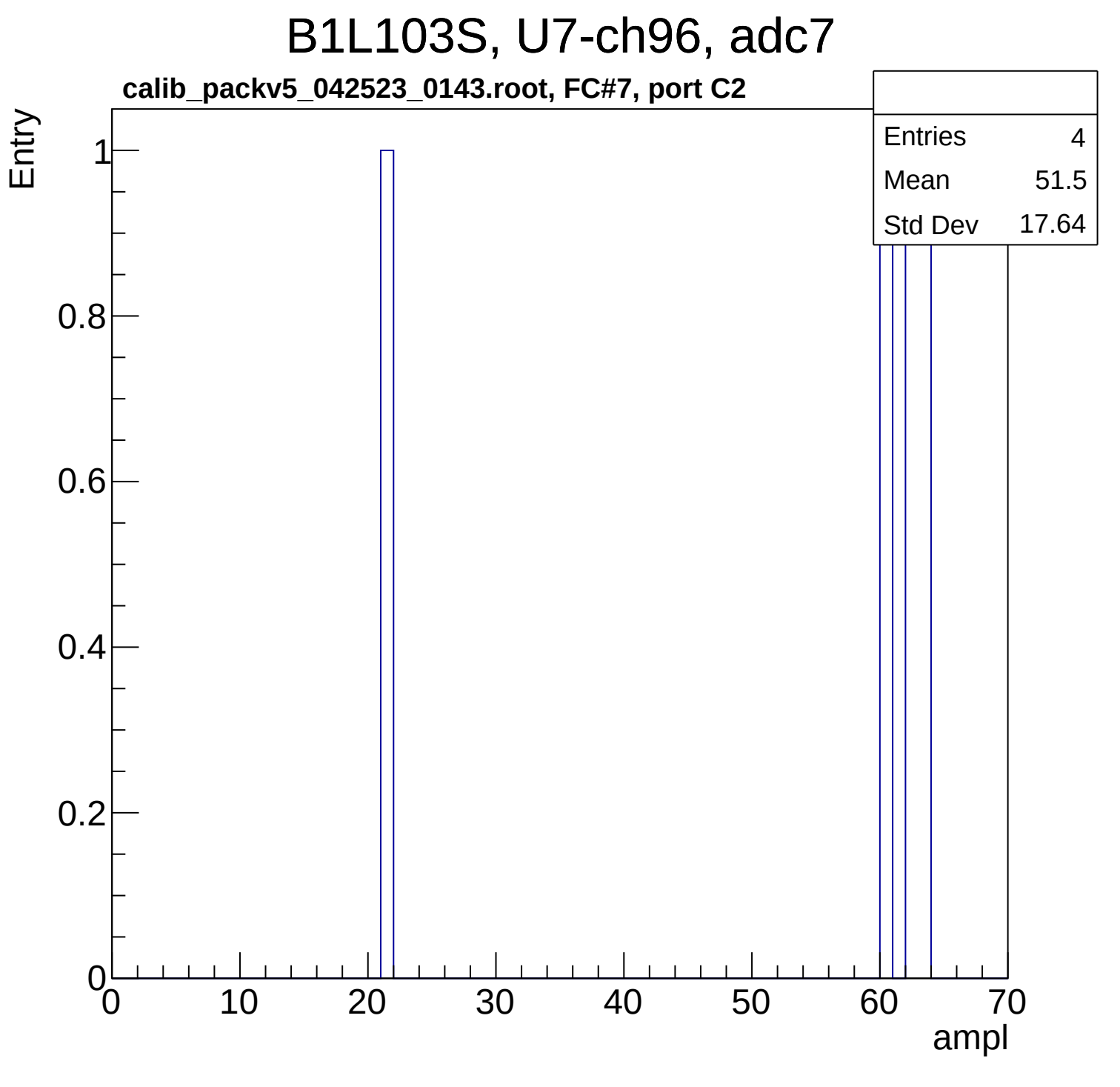
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch96, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 21
Mean 58.29
Std Dev 13.23
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch96, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 4
Mean 51.5
Std Dev 17.64
Entry
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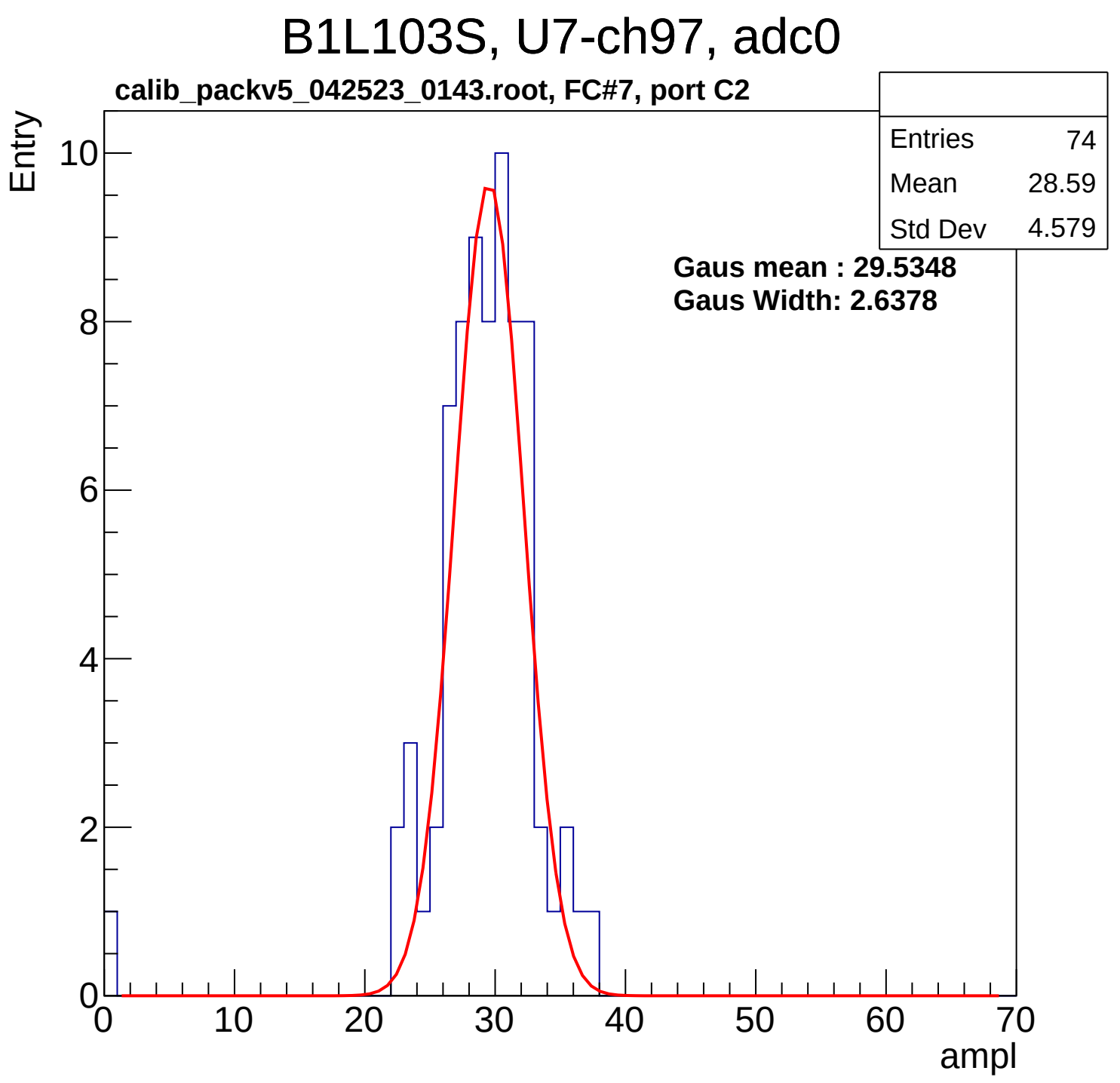
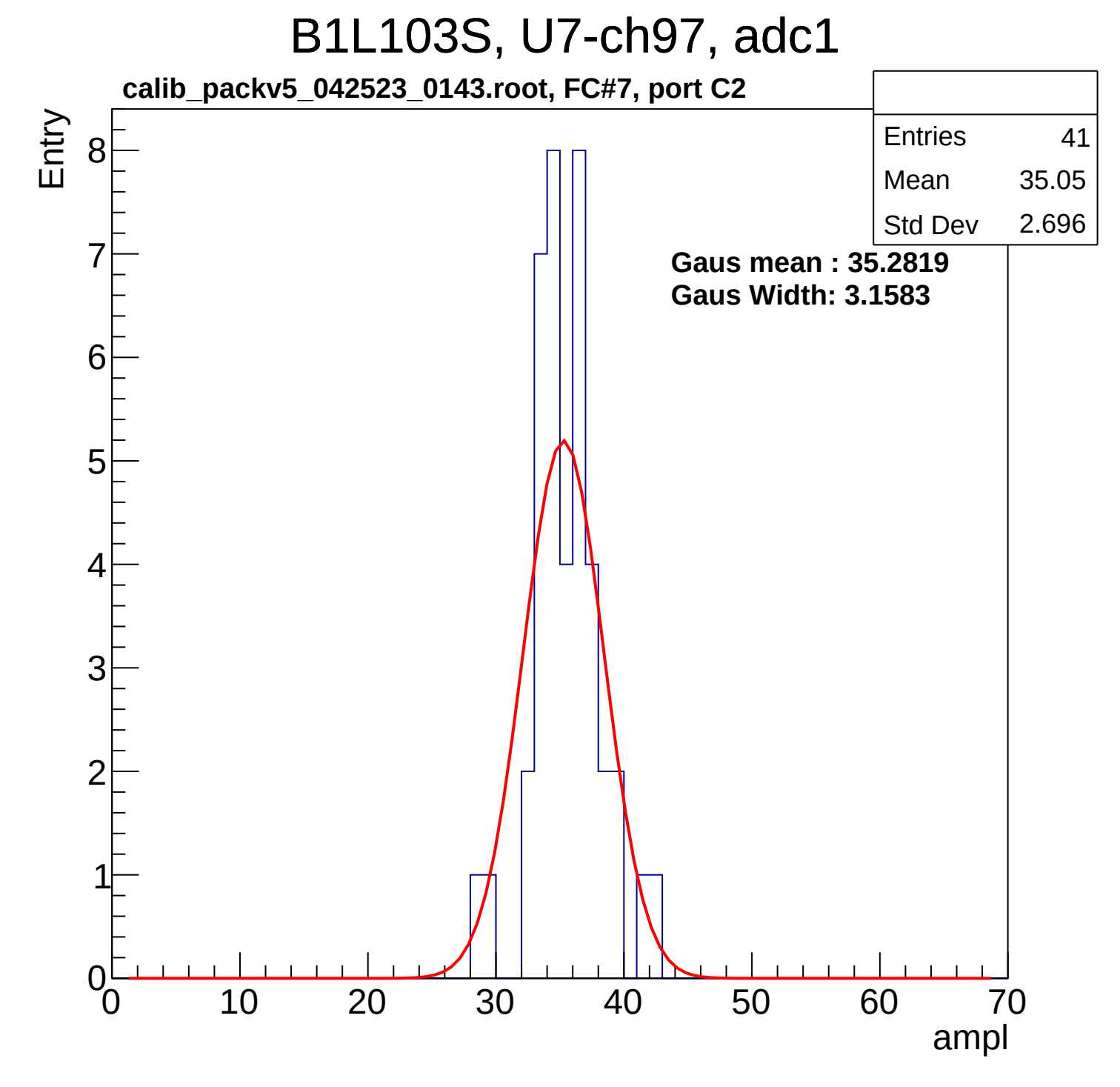
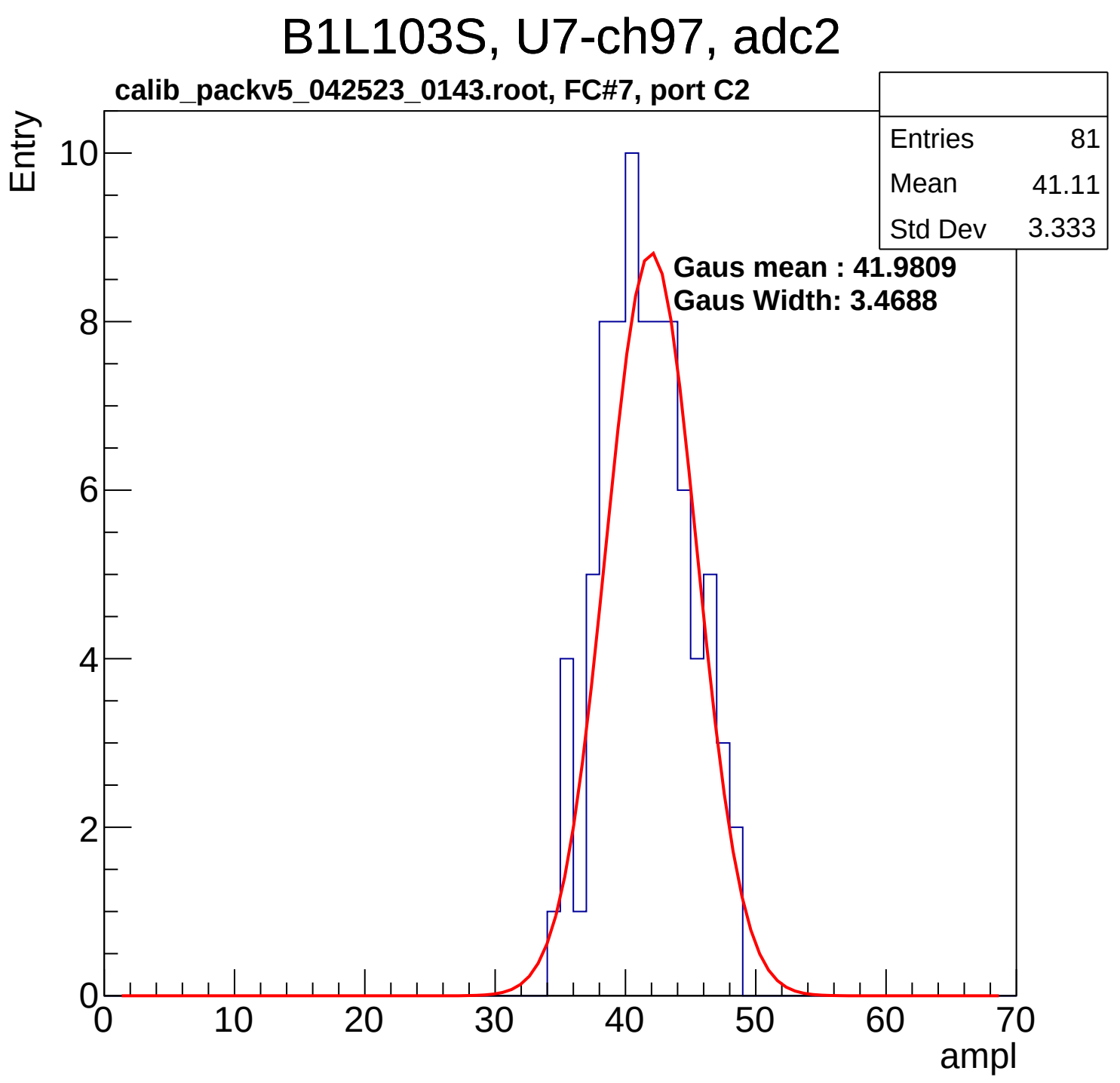
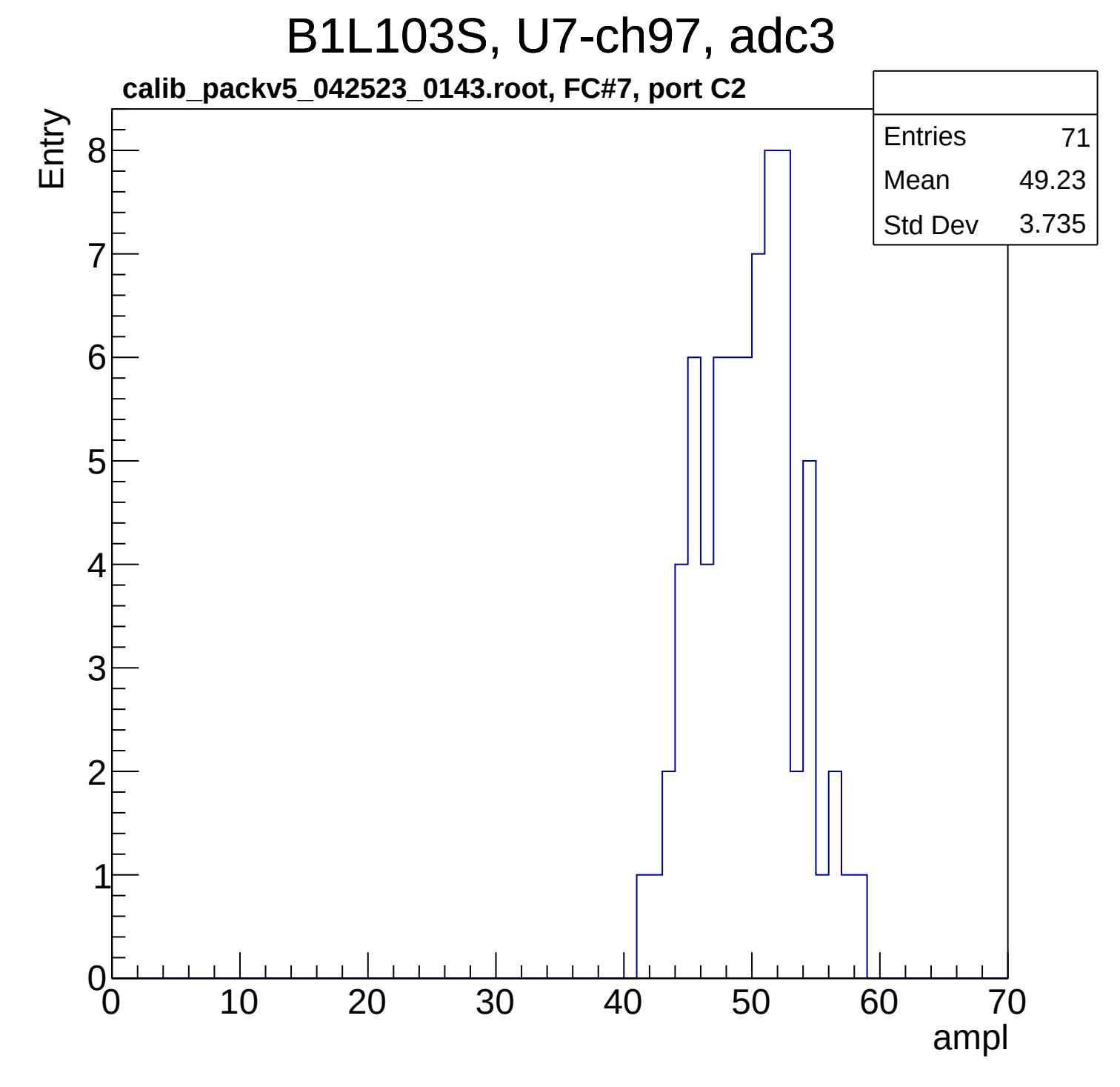
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch97, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 74
Mean 28.59
Std Dev 4.579
Gaus mean : 29.5348
Gaus Width: 2.6378
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch97, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 41
Mean 35.05
Std Dev 2.696
Gaus mean : 35.2819
Gaus Width: 3.1583
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch97, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 81
Mean 41.11
Std Dev 3.333
Gaus mean : 41.9809
Gaus Width: 3.4688
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch97, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 71
Mean 49.23
Std Dev 3.735
Entry
ampl
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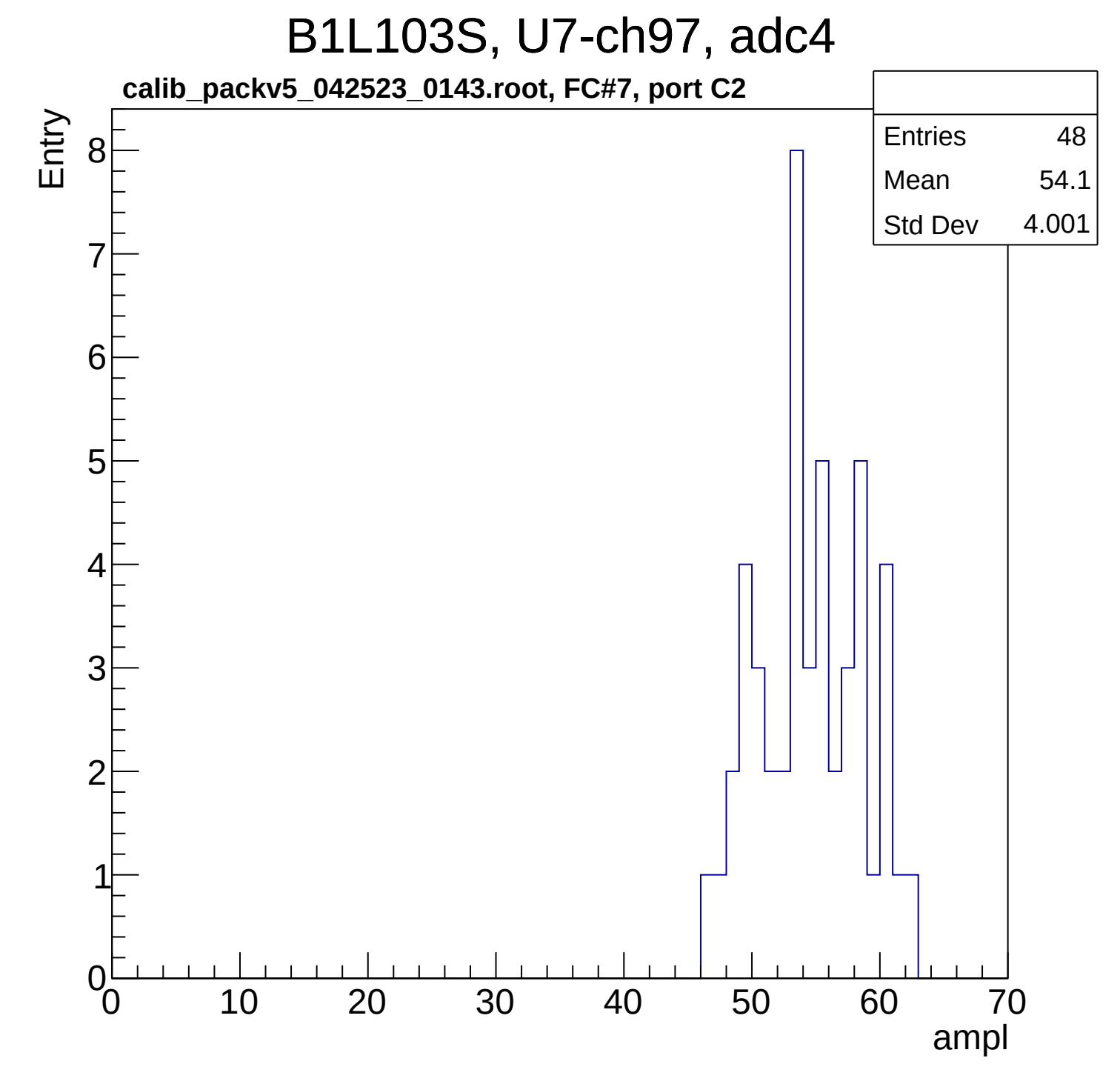
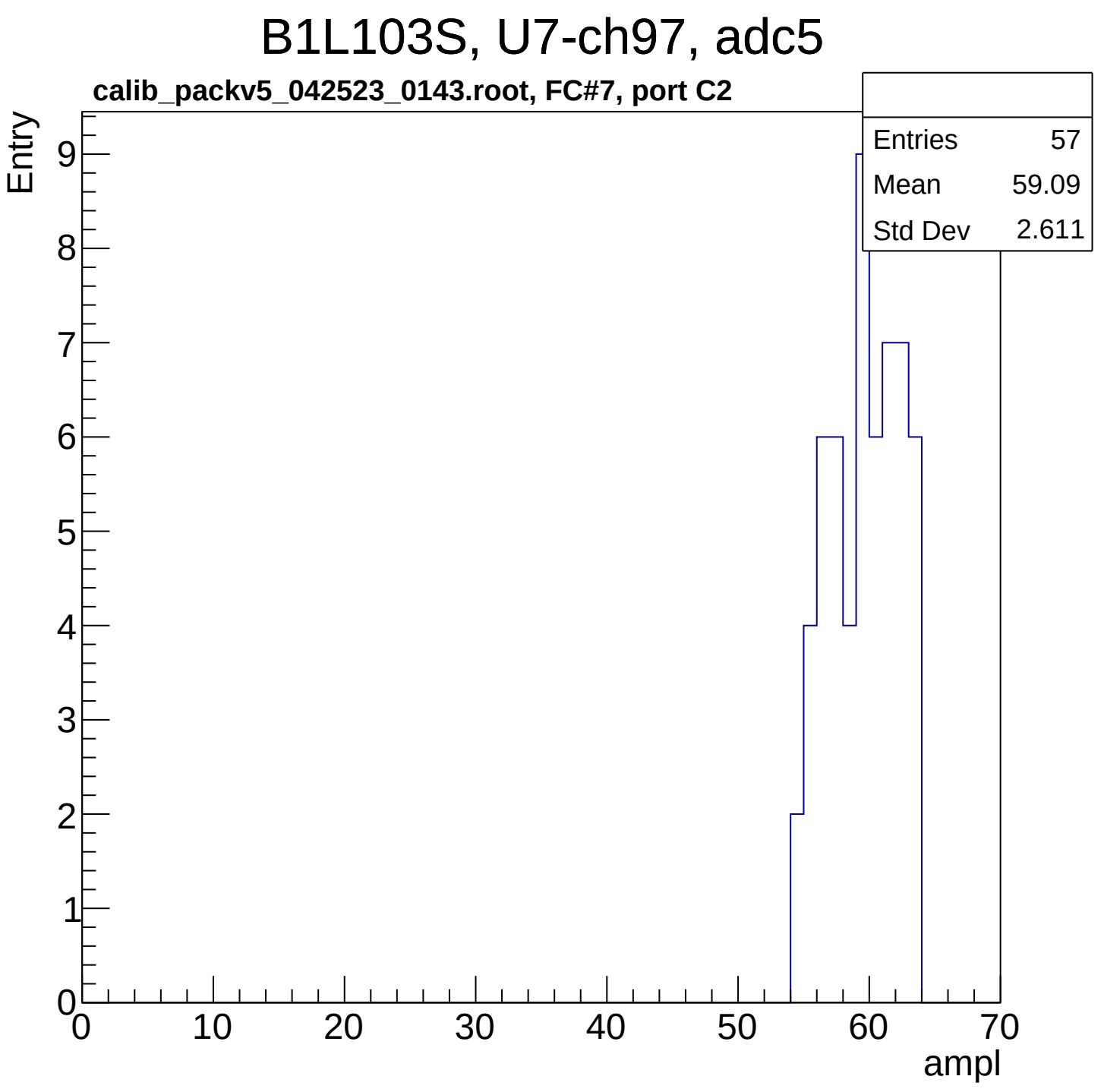
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch97, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 48
Mean 54.1
Std Dev 4.001
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch97, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 59.09
Std Dev 2.611
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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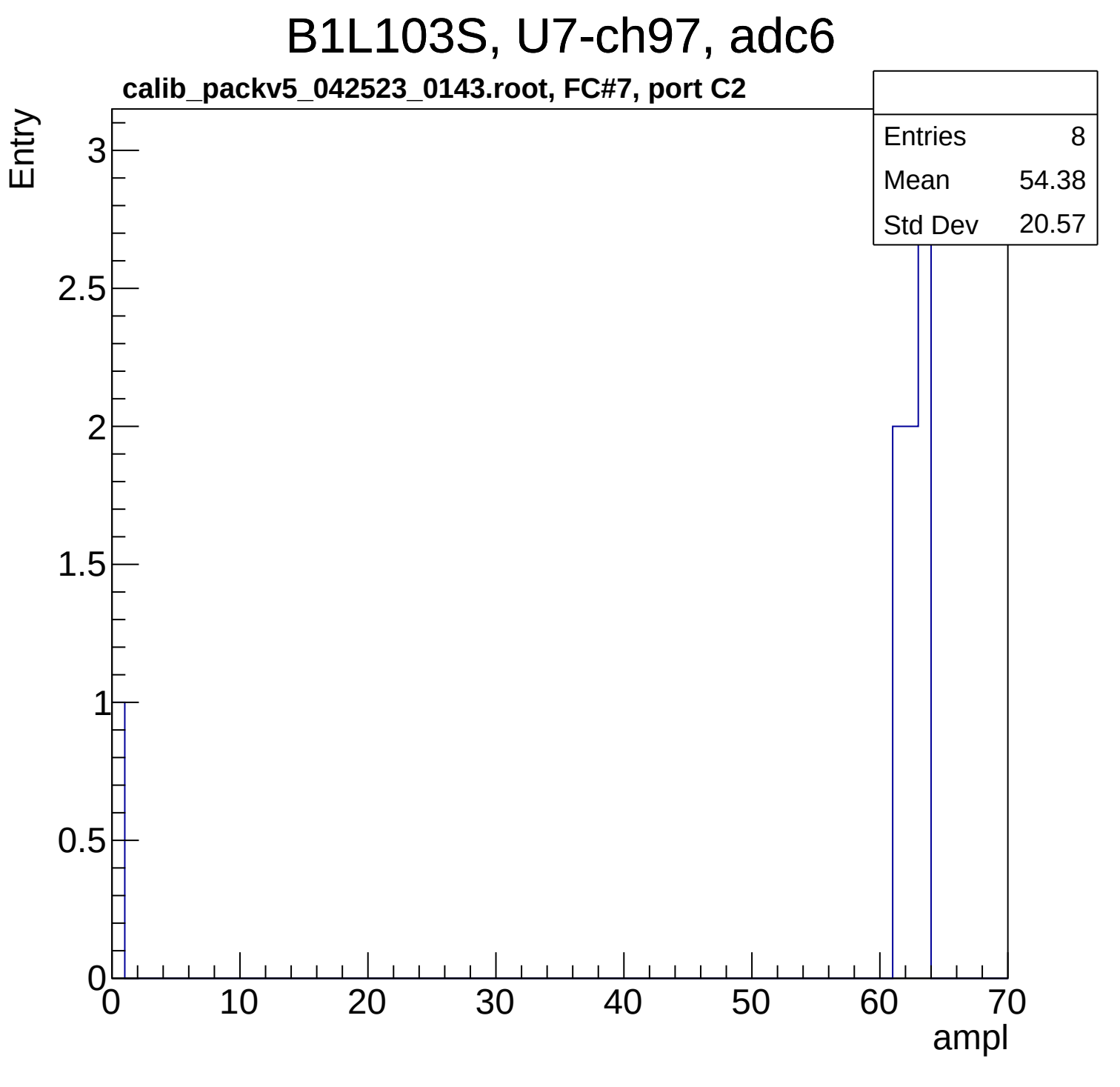
B1L103S, U7-ch97, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 8
Mean 54.38
Std Dev 20.57
Entry
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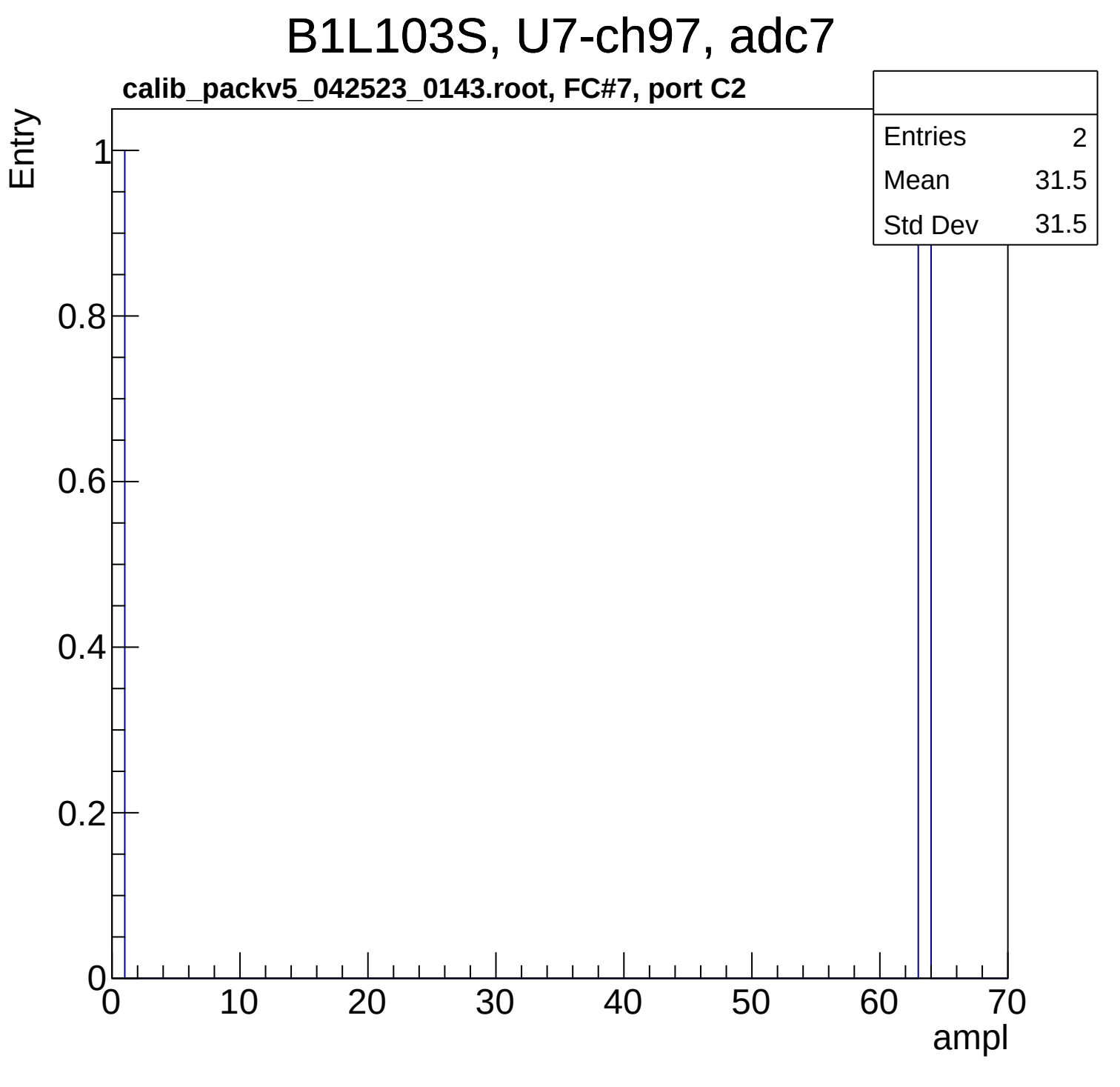
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch97, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 31.5
Std Dev 31.5
Entry
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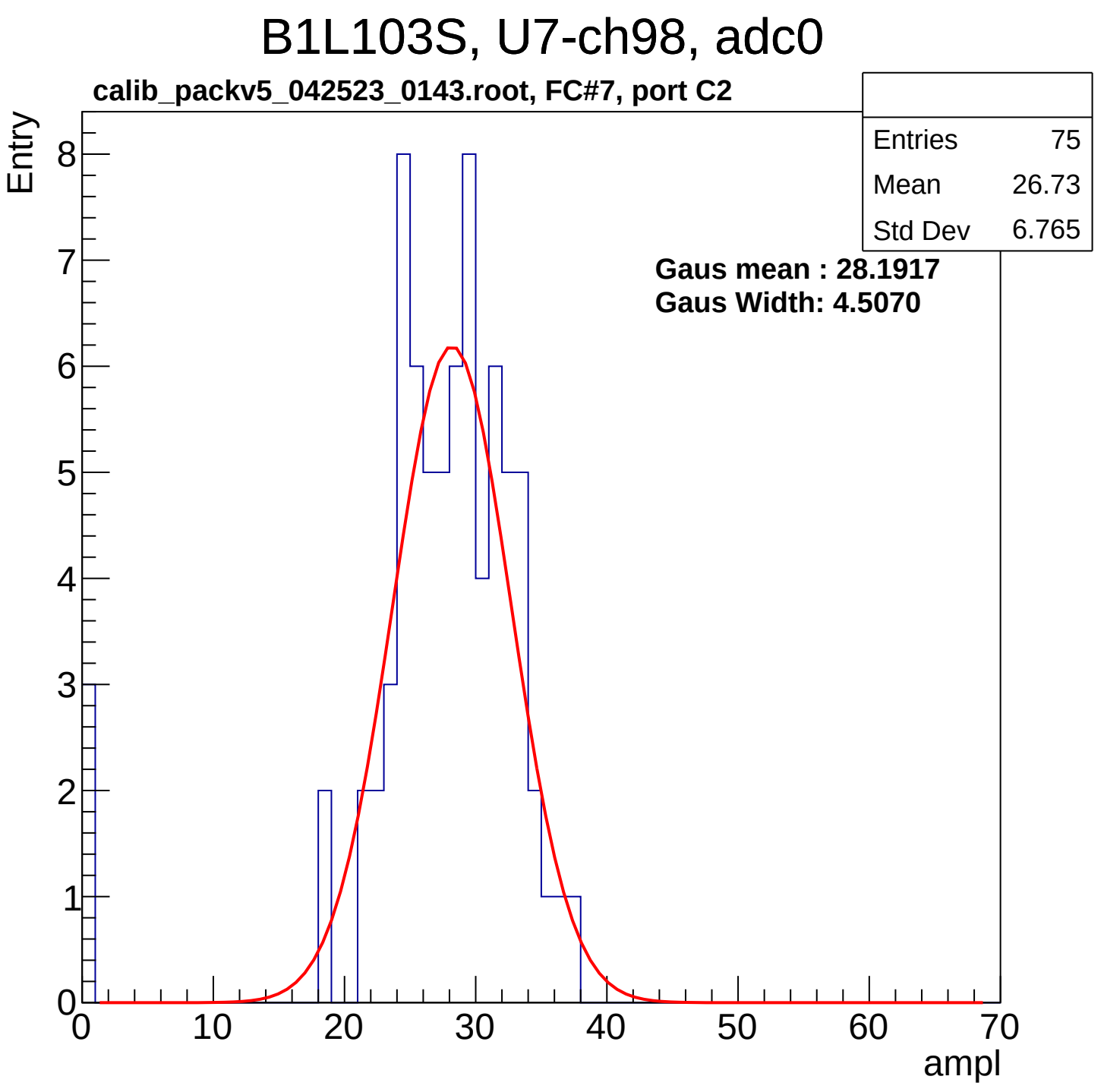
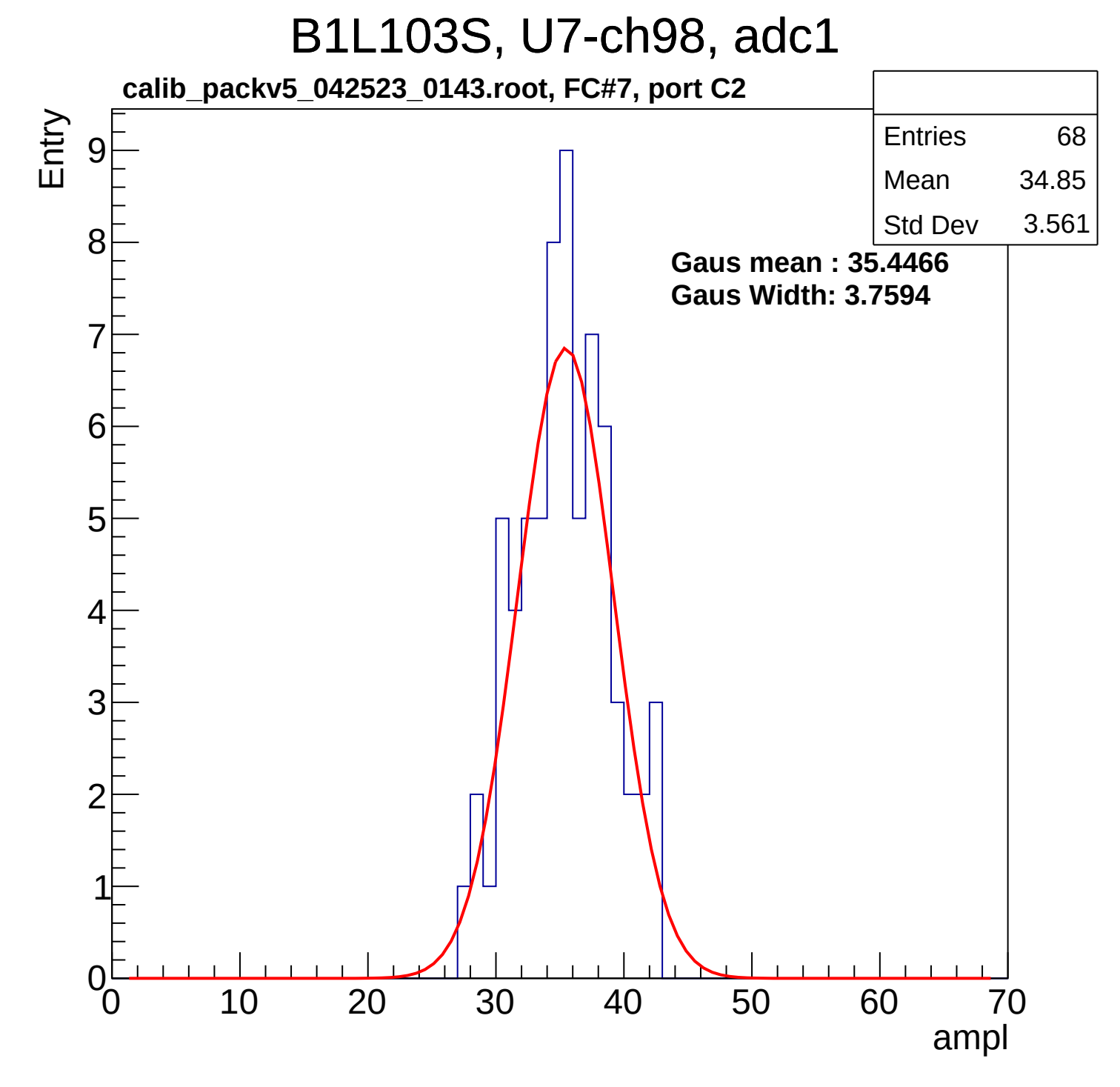
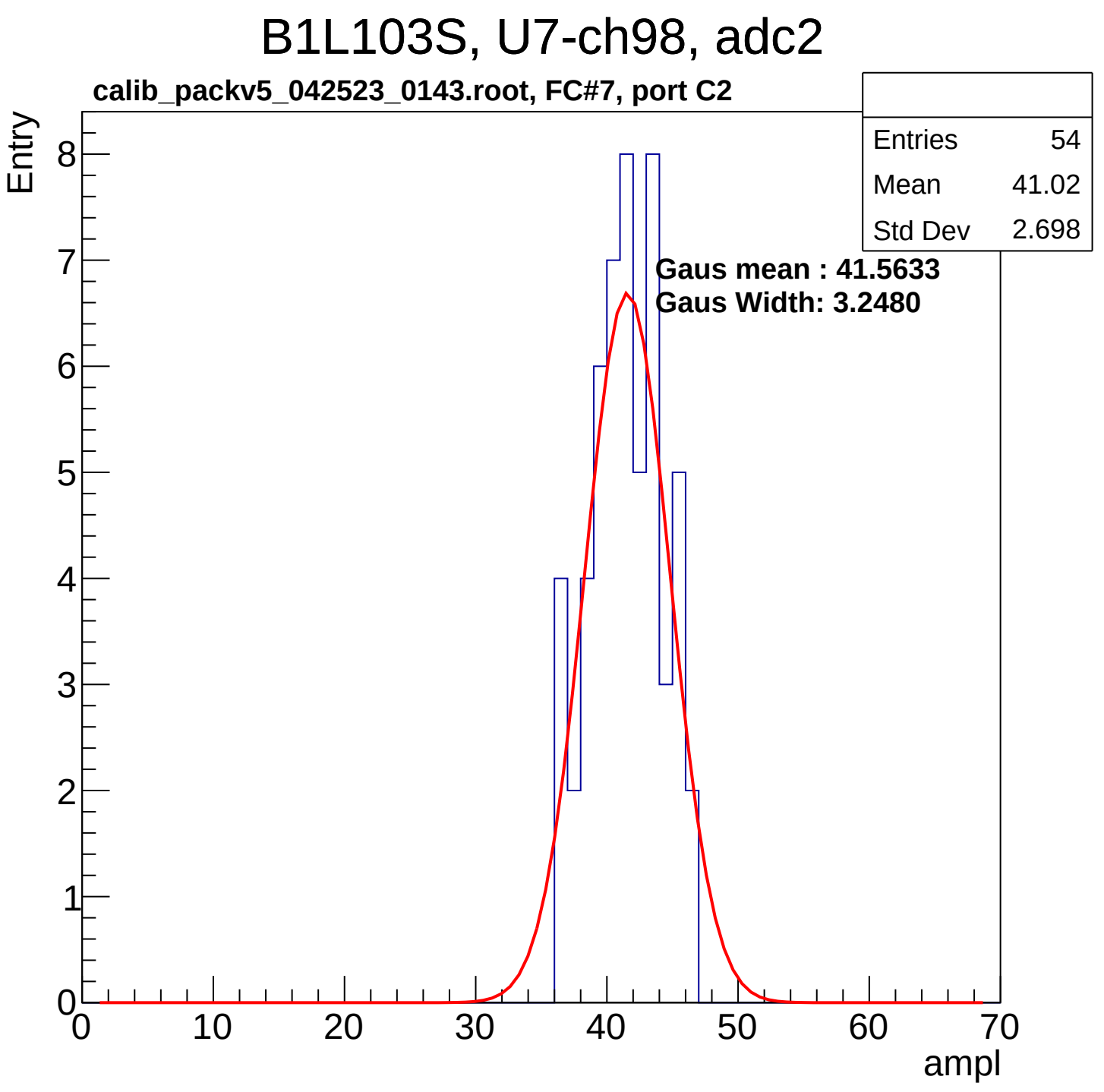
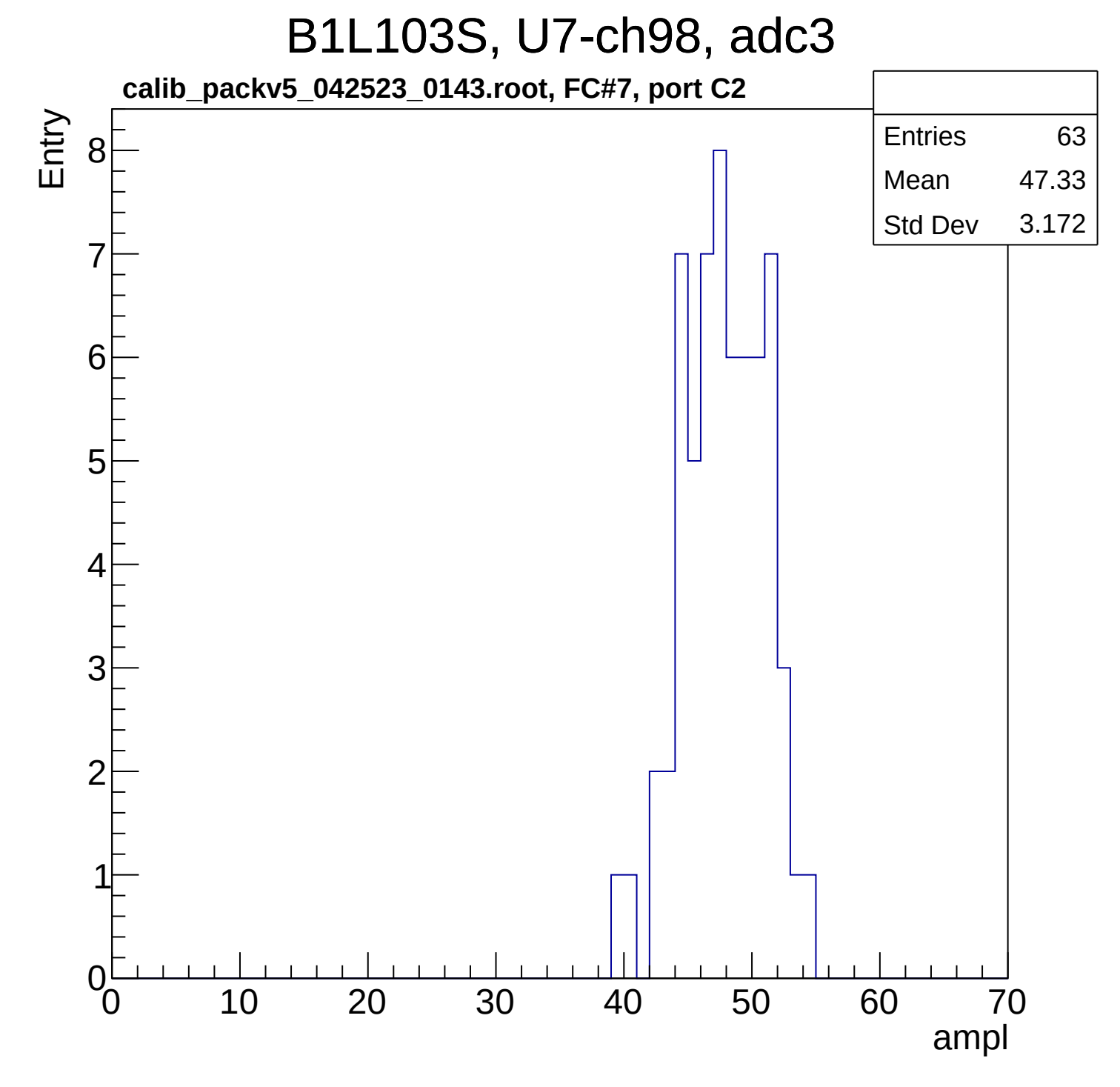
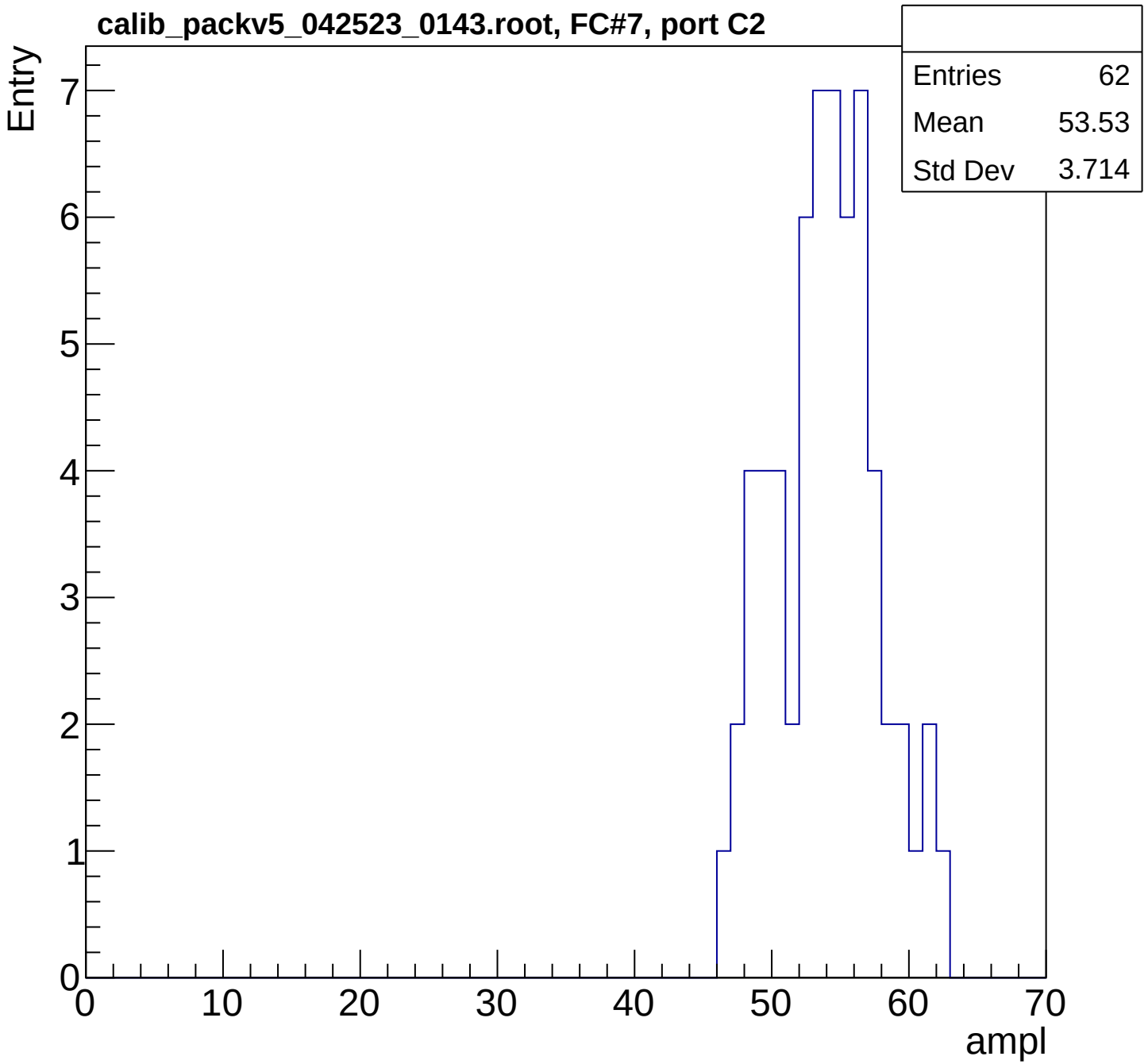
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

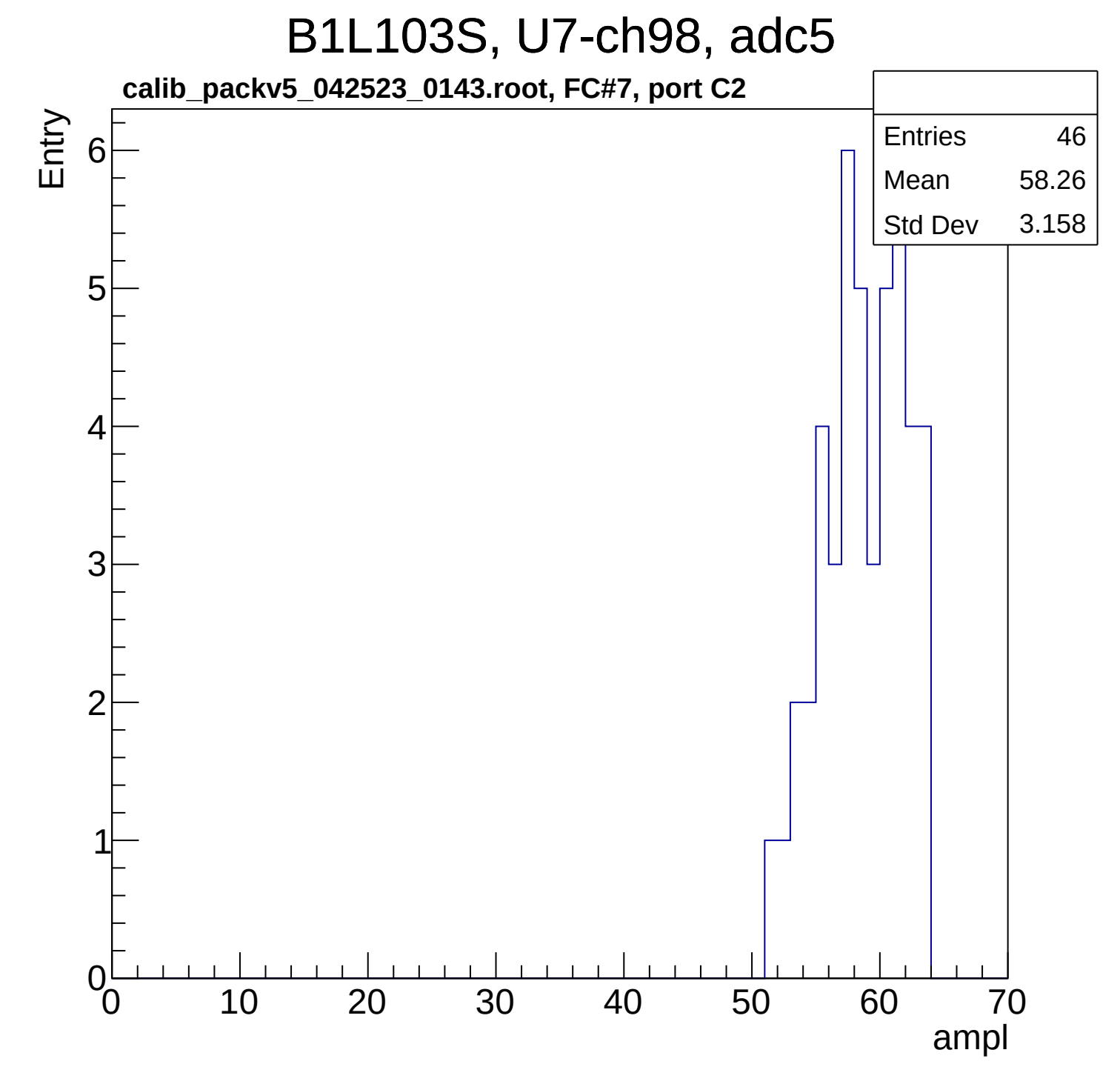

B1L103S, U7-ch98, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 75
Mean 26.73
Std Dev 6.765
Gaus mean : 28.1917
Gaus Width: 4.5070
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch98, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 34.85
Std Dev 3.561
Gaus mean : 35.4466
Gaus Width: 3.7594
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch98, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 54
Mean 41.02
Std Dev 2.698
Gaus mean : 41.5633
Gaus Width: 3.2480
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch98, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 47.33
Std Dev 3.172
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch98, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 62
Mean 53.53
Std Dev 3.714
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch98, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 46
Mean 58.26
Std Dev 3.158
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
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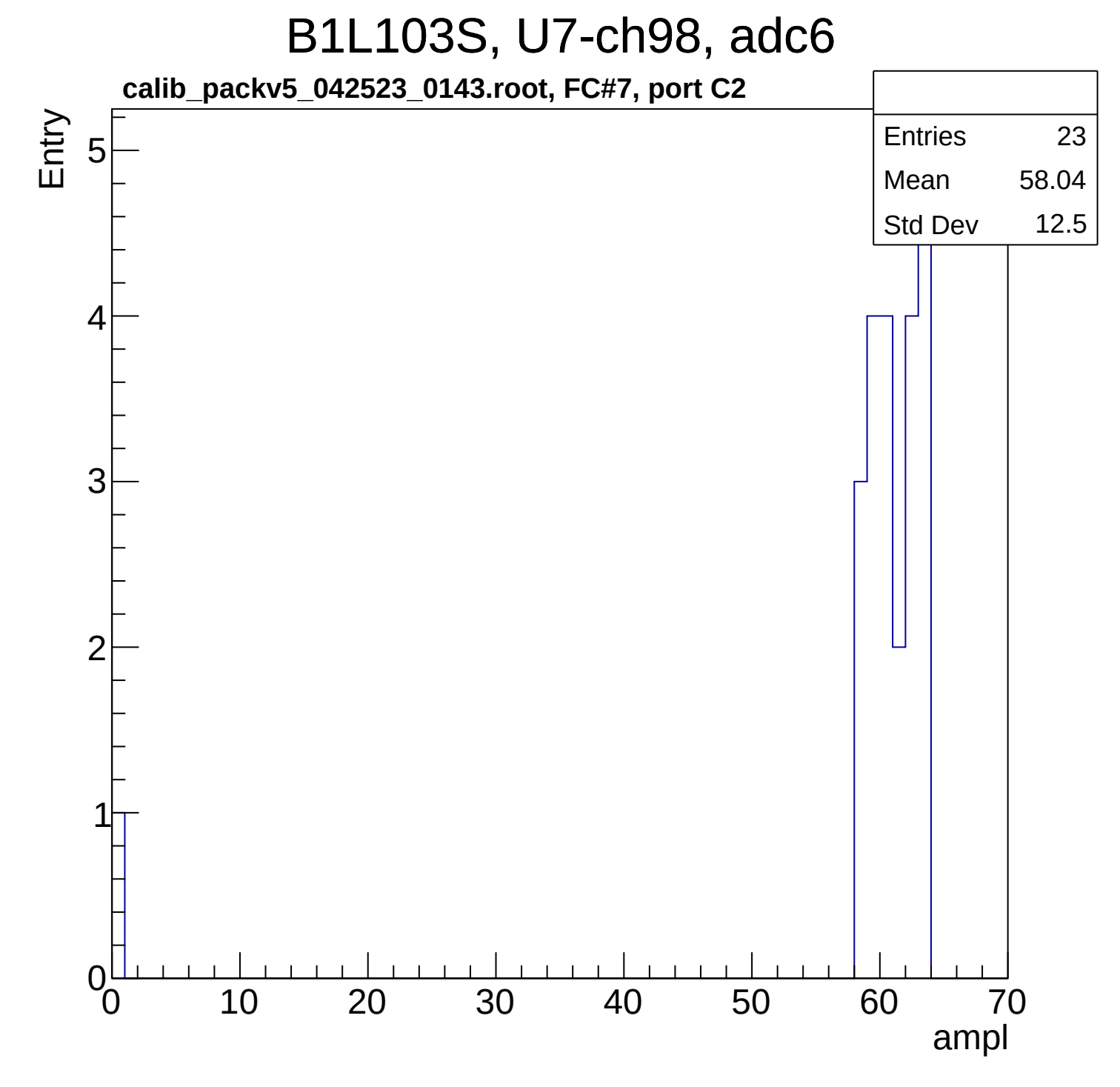
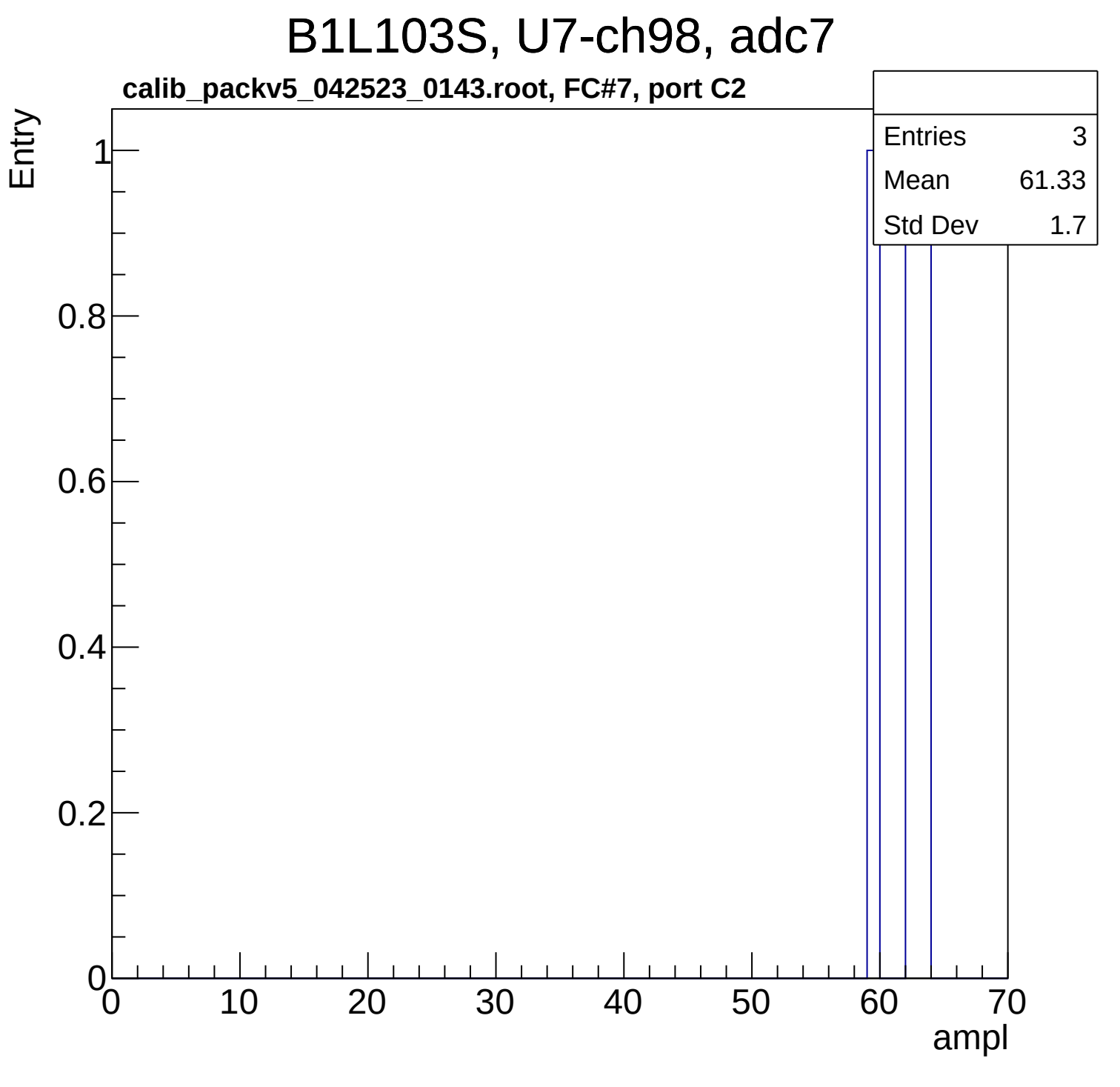
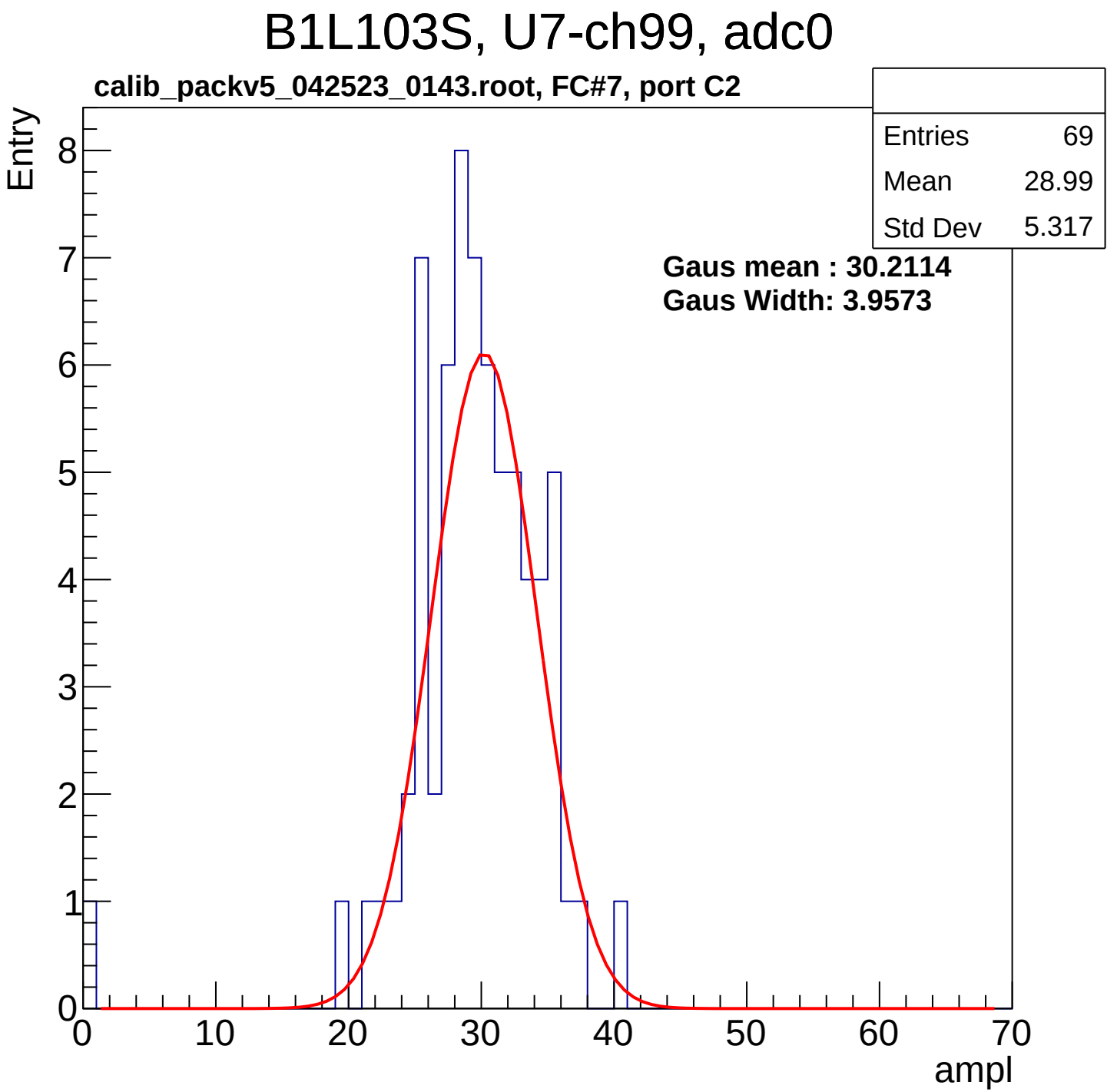
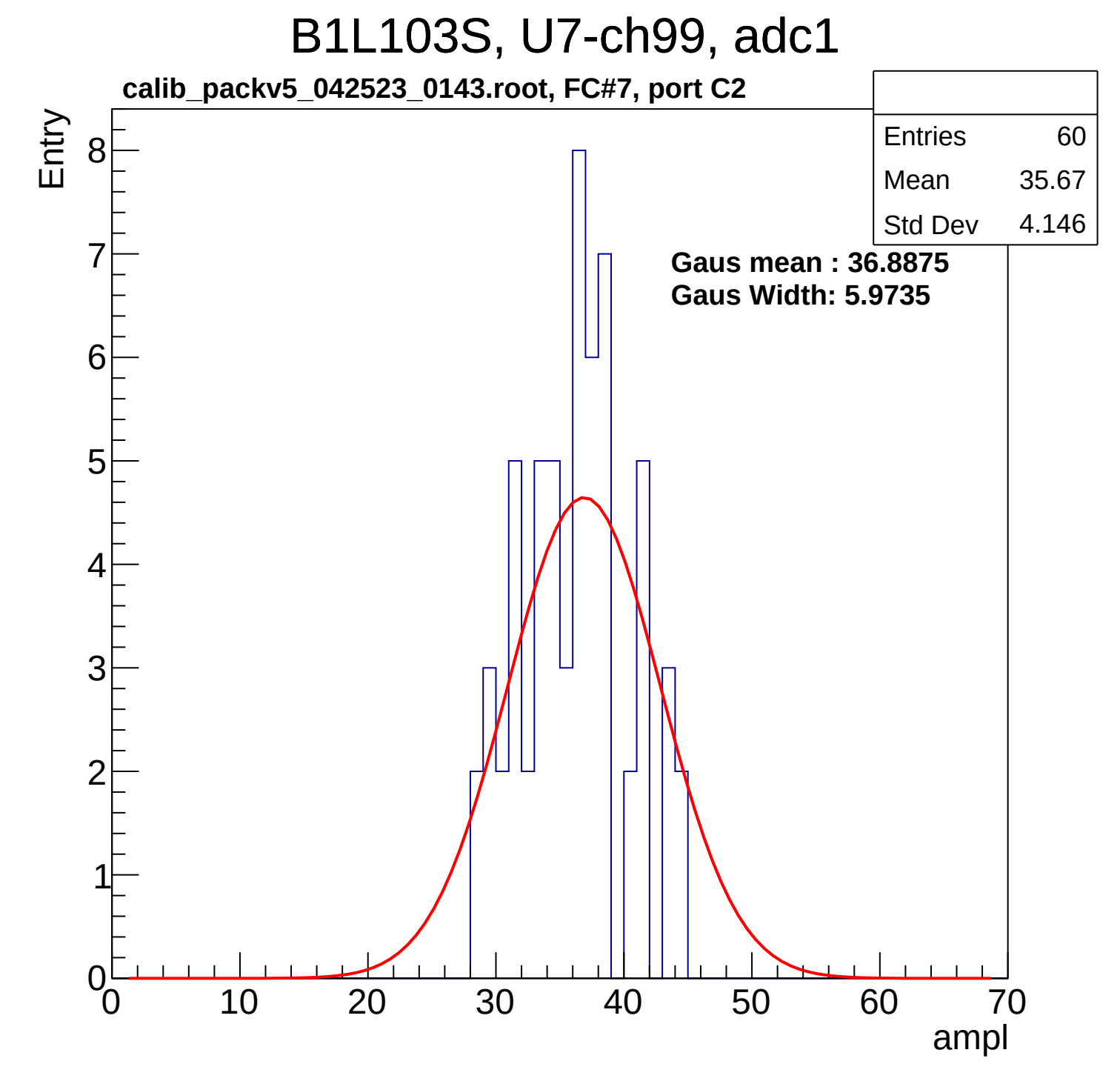
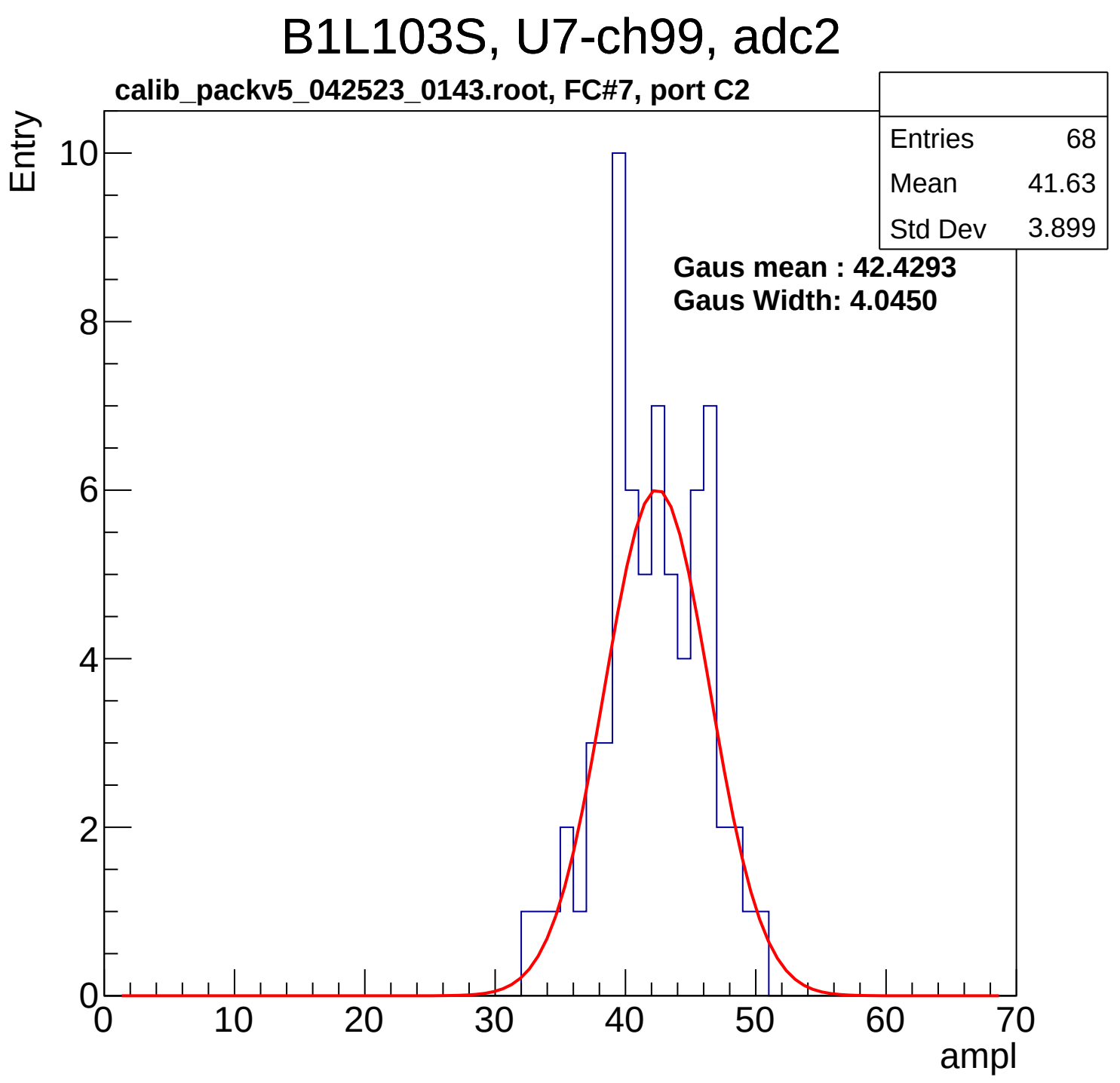
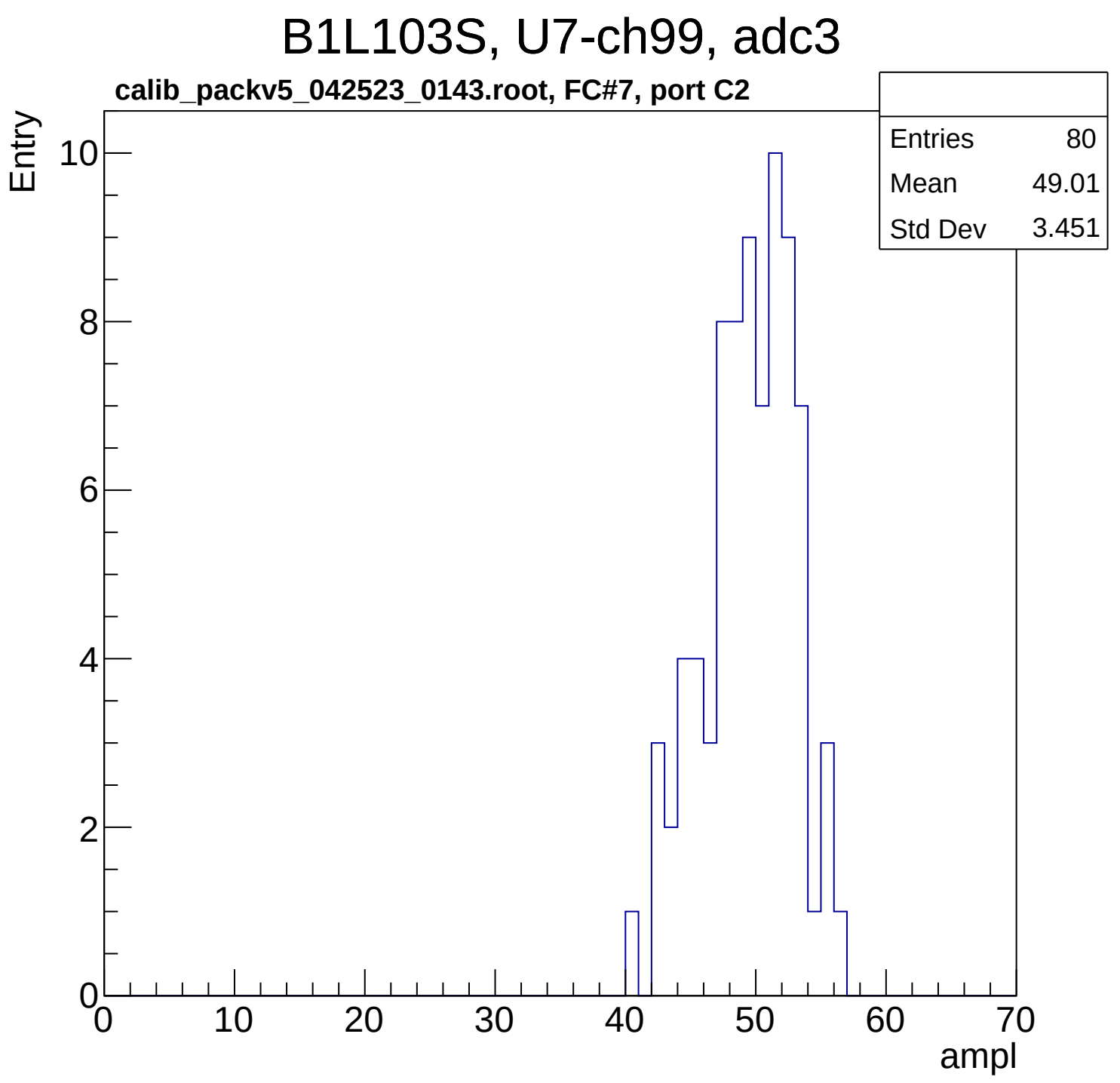

B1L103S, U7-ch98, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 23
Mean 58.04
Std Dev 12.5
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U7-ch98, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 61.33
Std Dev 1.7
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B1L103S, U7-ch99, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 28.99
Std Dev 5.317
Gaus mean : 30.2114
Gaus Width: 3.9573
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch99, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 60
Mean 35.67
Std Dev 4.146
Gaus mean : 36.8875
Gaus Width: 5.9735
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch99, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 41.63
Std Dev 3.899
Gaus mean : 42.4293
Gaus Width: 4.0450
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch99, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 80
Mean 49.01
Std Dev 3.451
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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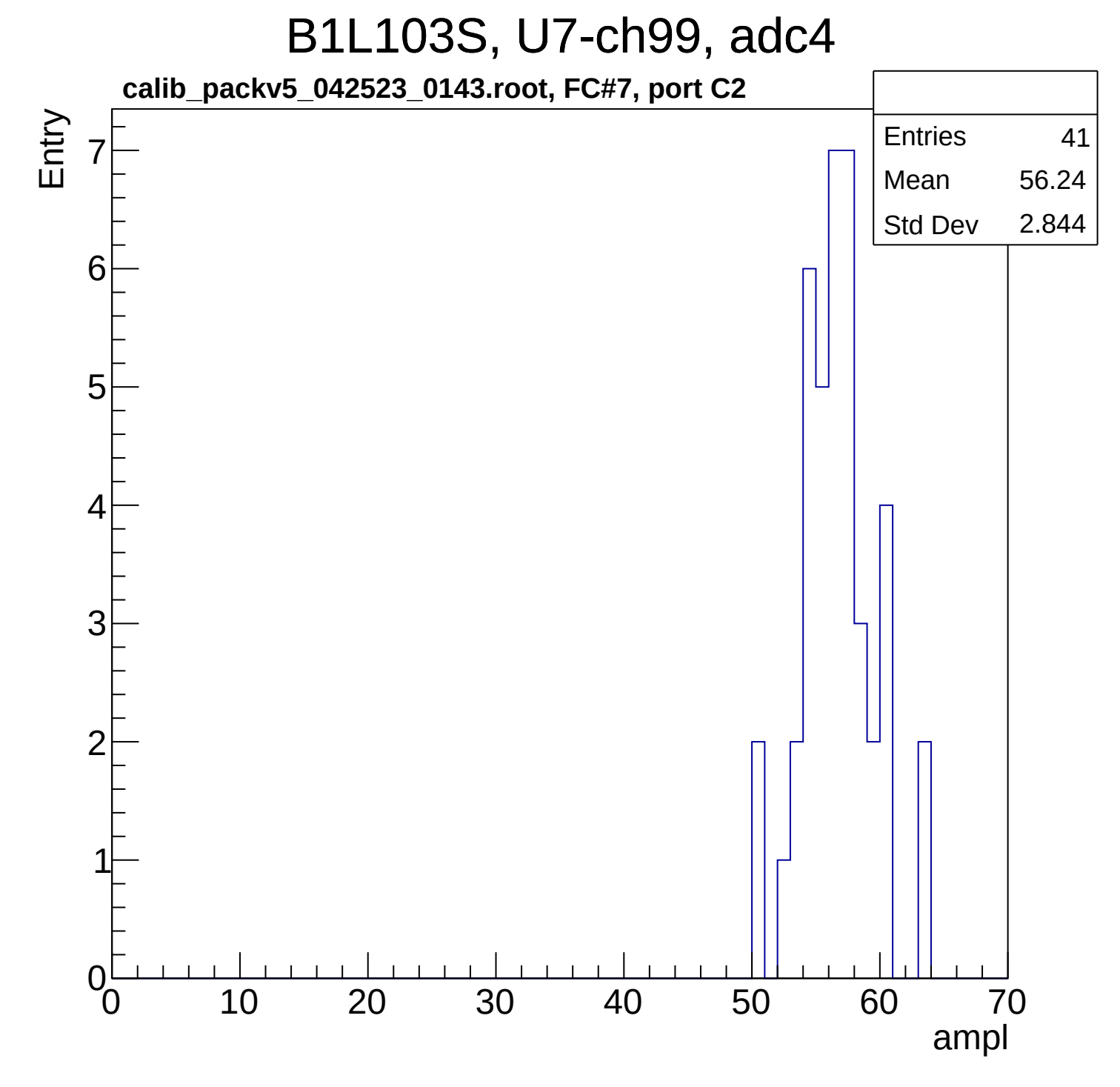
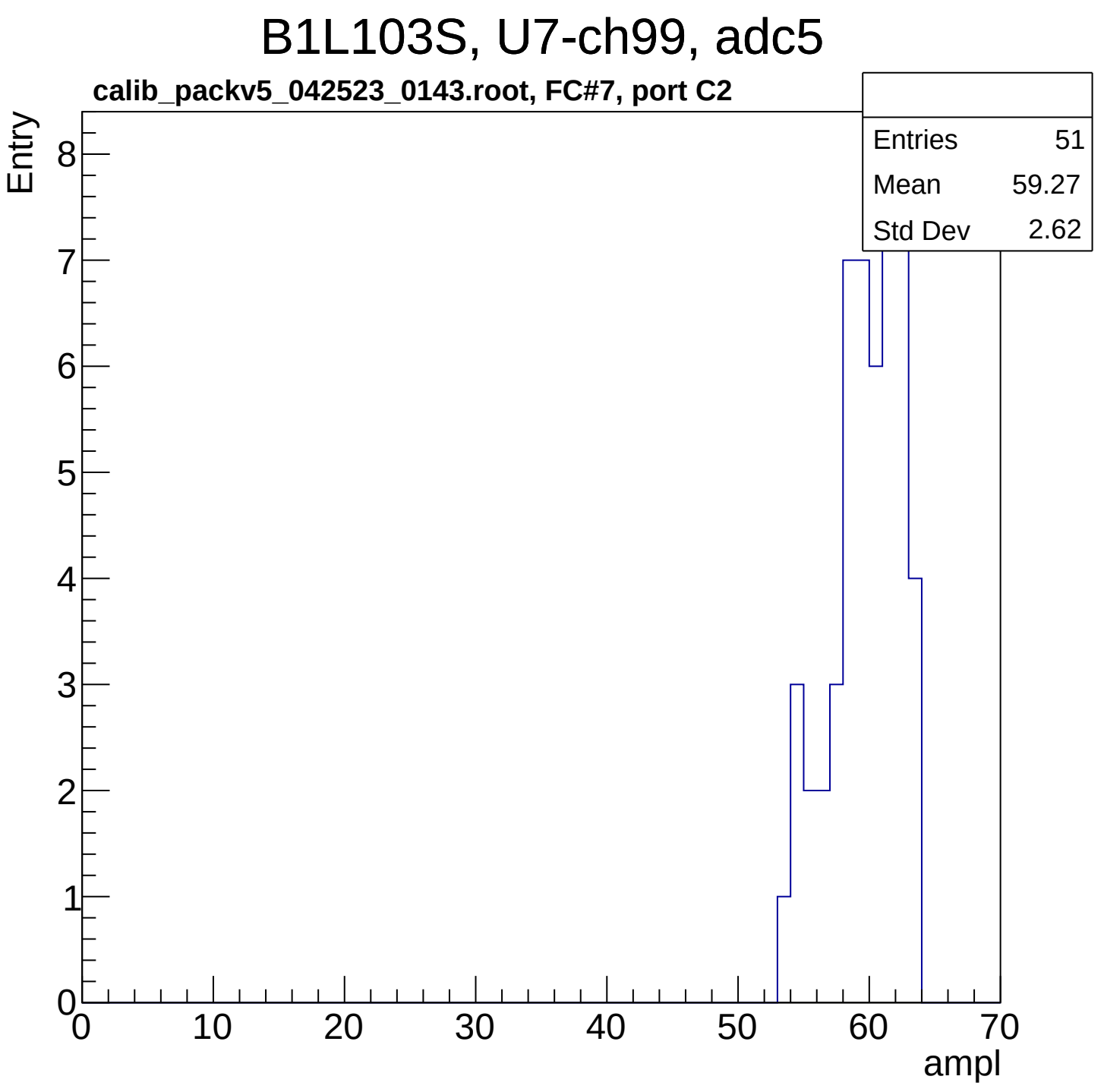

B1L103S, U7-ch99, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 41
Mean 56.24
Std Dev 2.844
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch99, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 51
Mean 59.27
Std Dev 2.62
Entry
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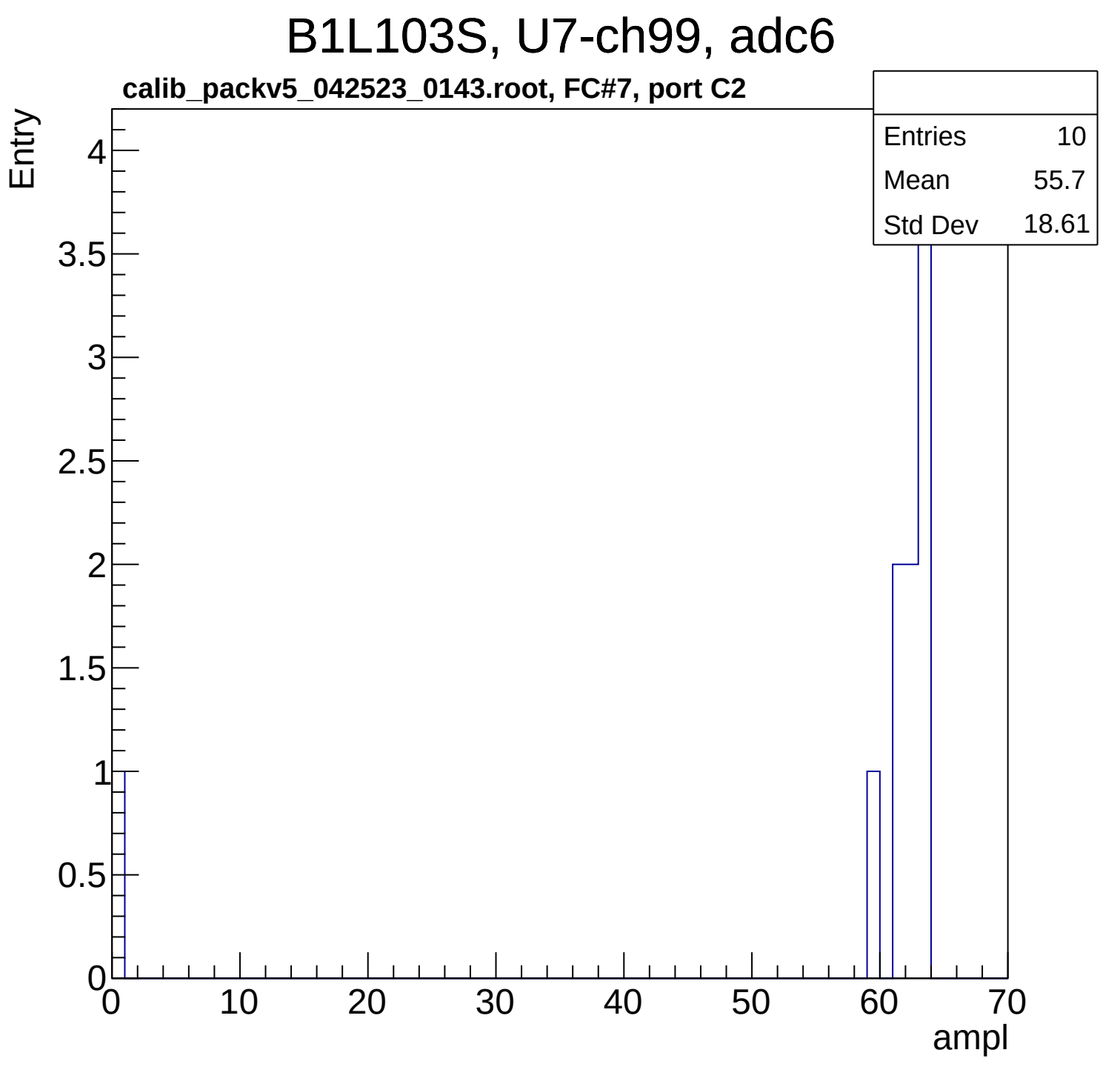
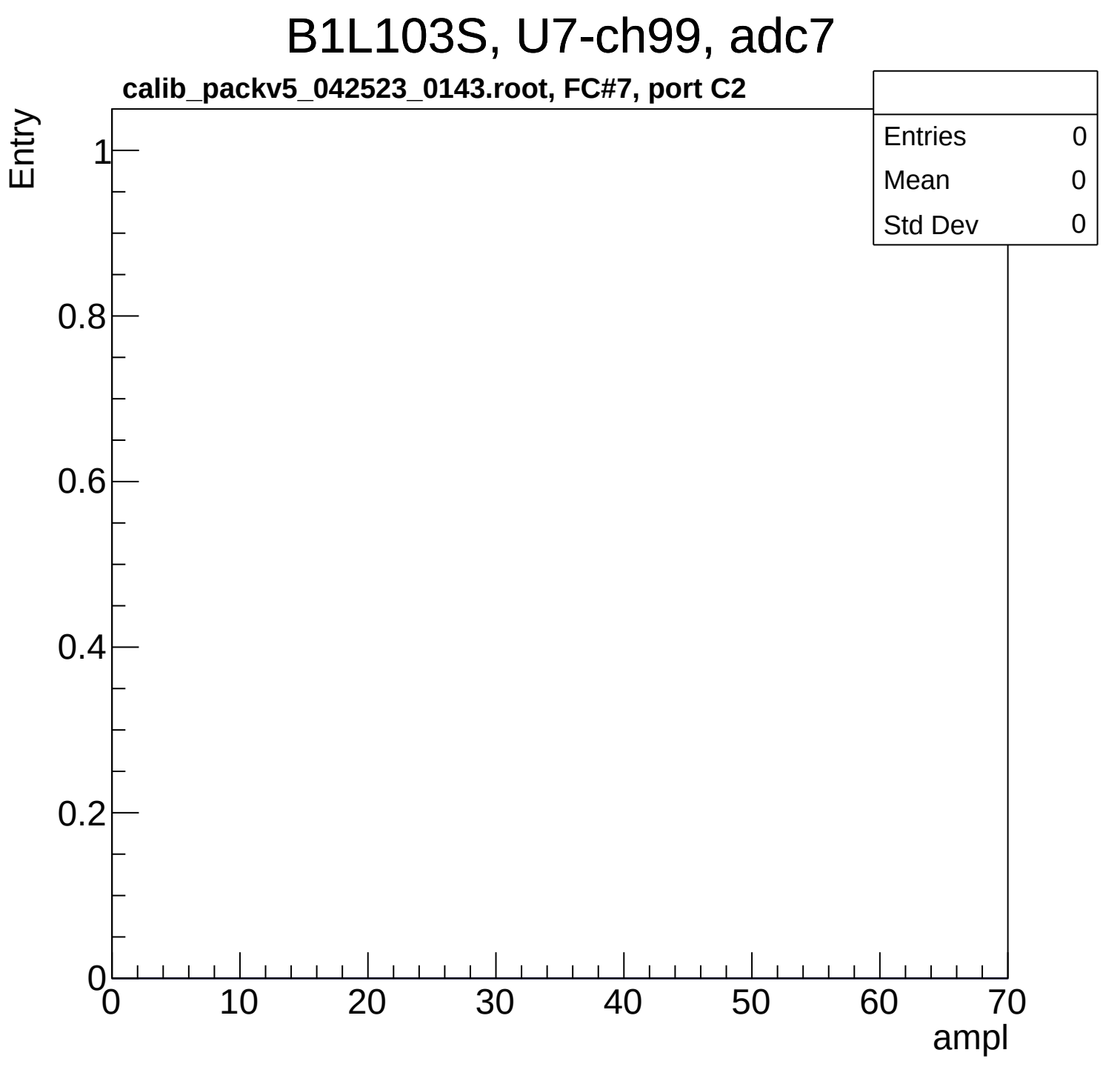
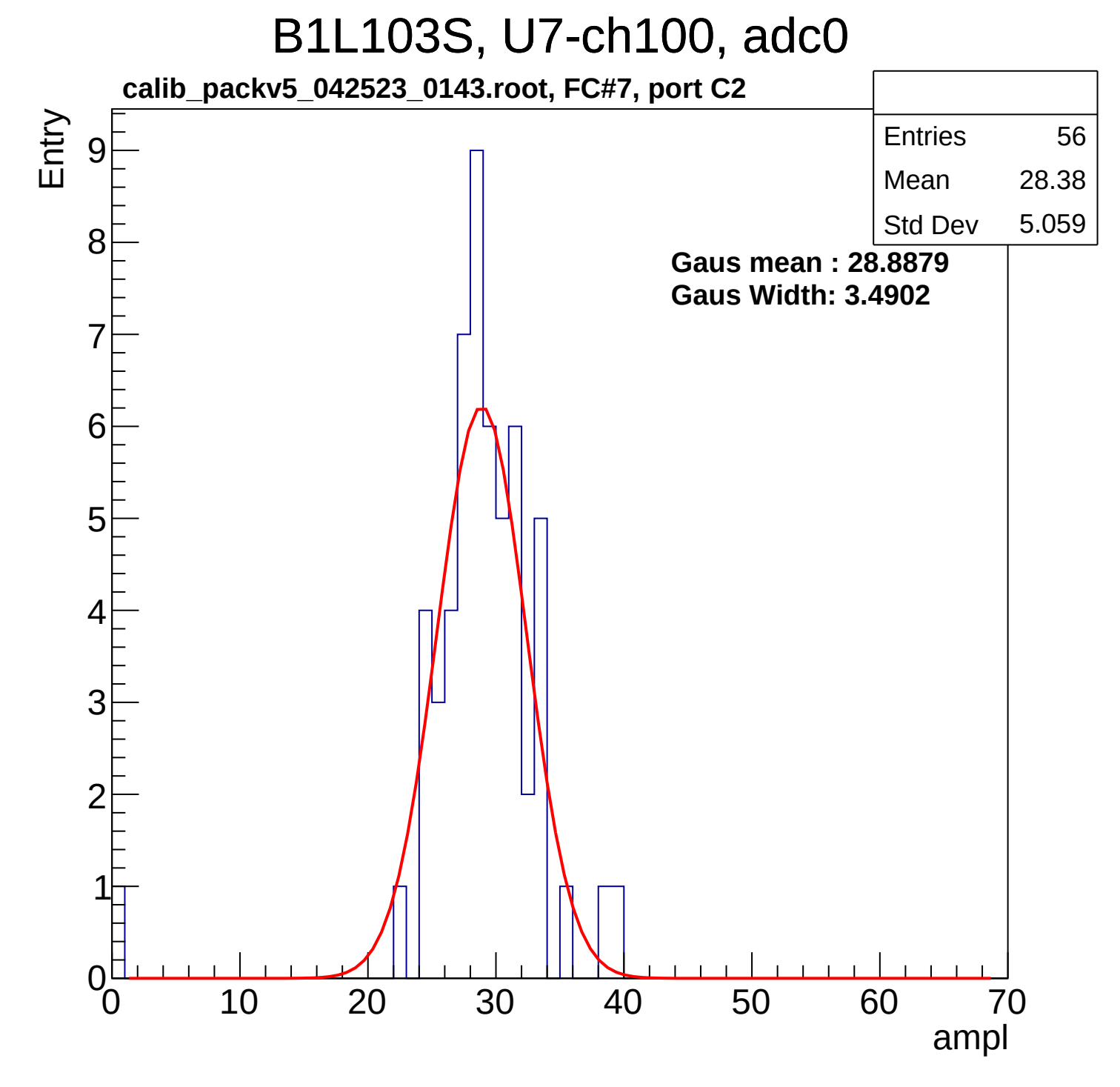
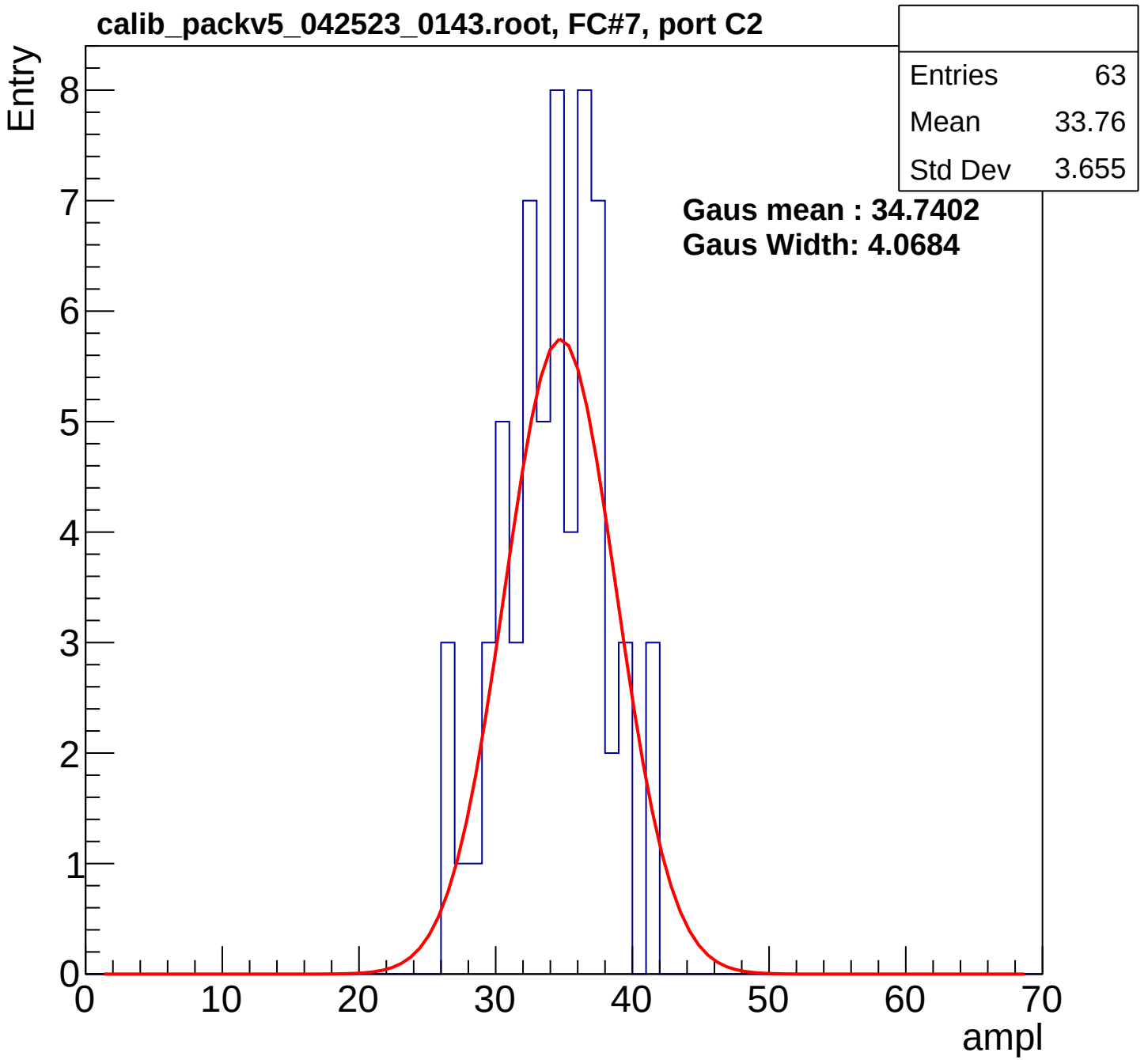
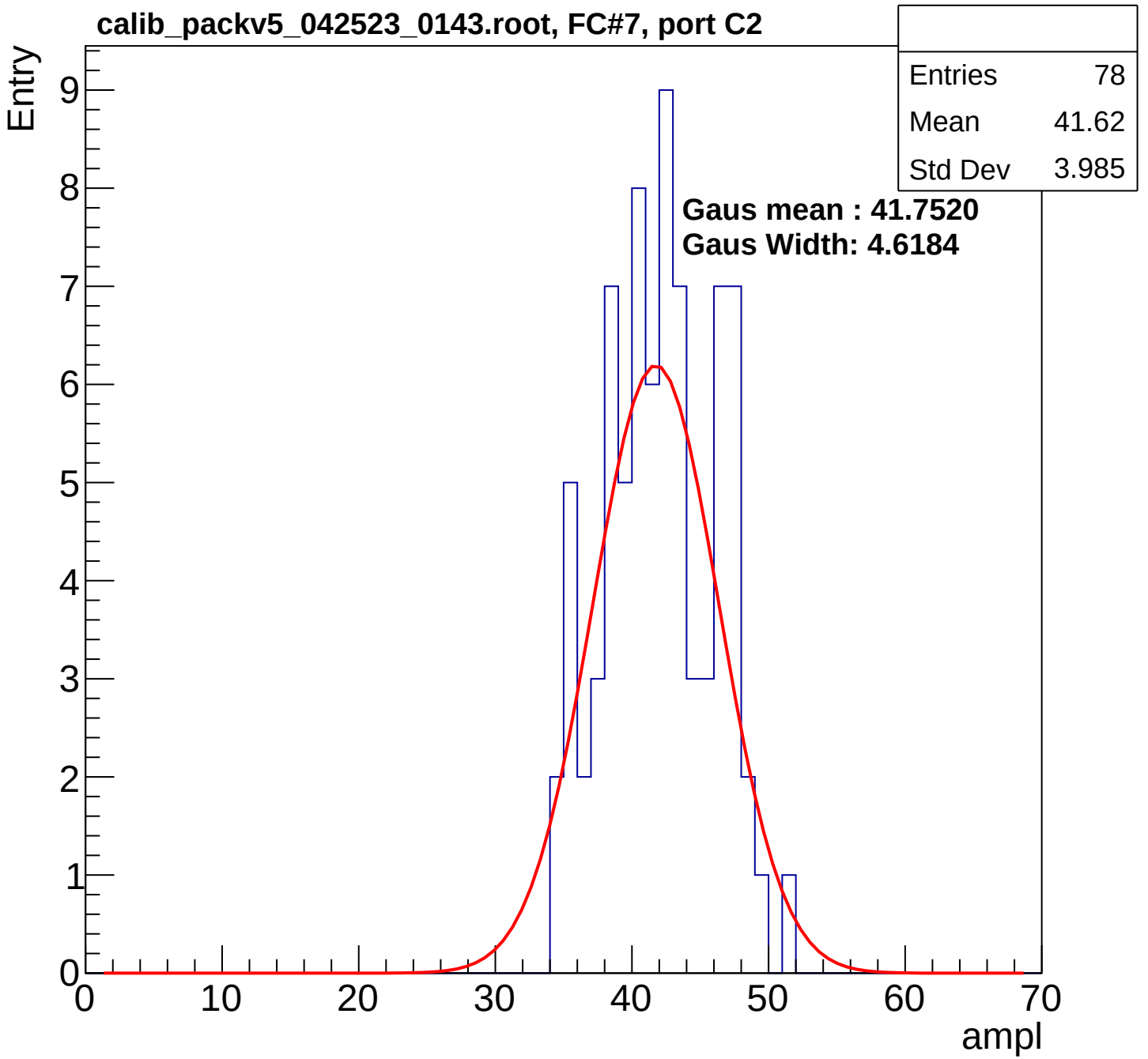
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch99, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 10
Mean 55.7
Std Dev 18.61
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U7-ch99, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch100, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 28.38
Std Dev 5.059
Gaus mean : 28.8879
Gaus Width: 3.4902
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch100, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 33.76
Std Dev 3.655
Gaus mean : 34.7402
Gaus Width: 4.0684
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch100, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 78
Mean 41.62
Std Dev 3.985
Gaus mean : 41.7520
Gaus Width: 4.6184
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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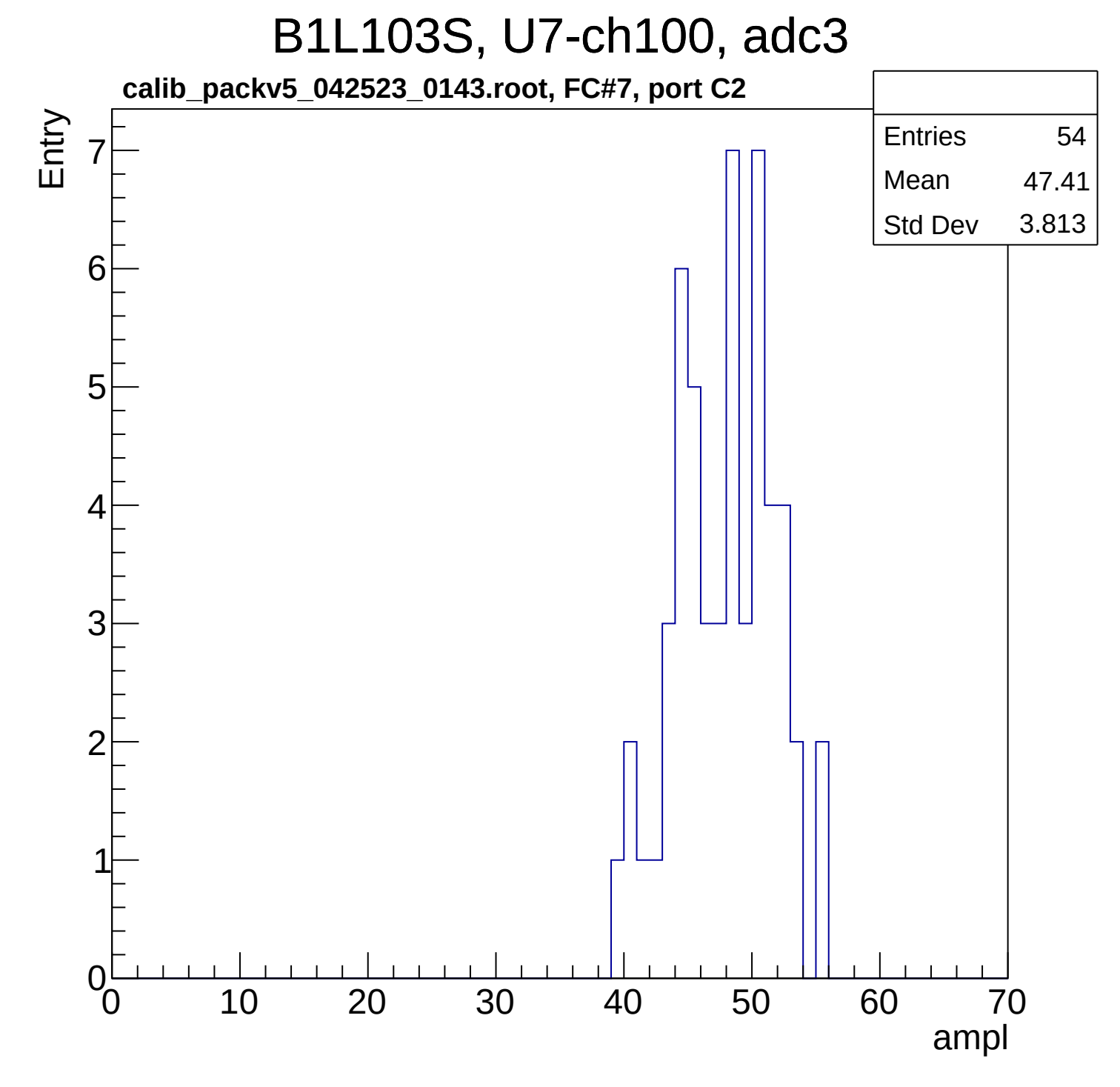
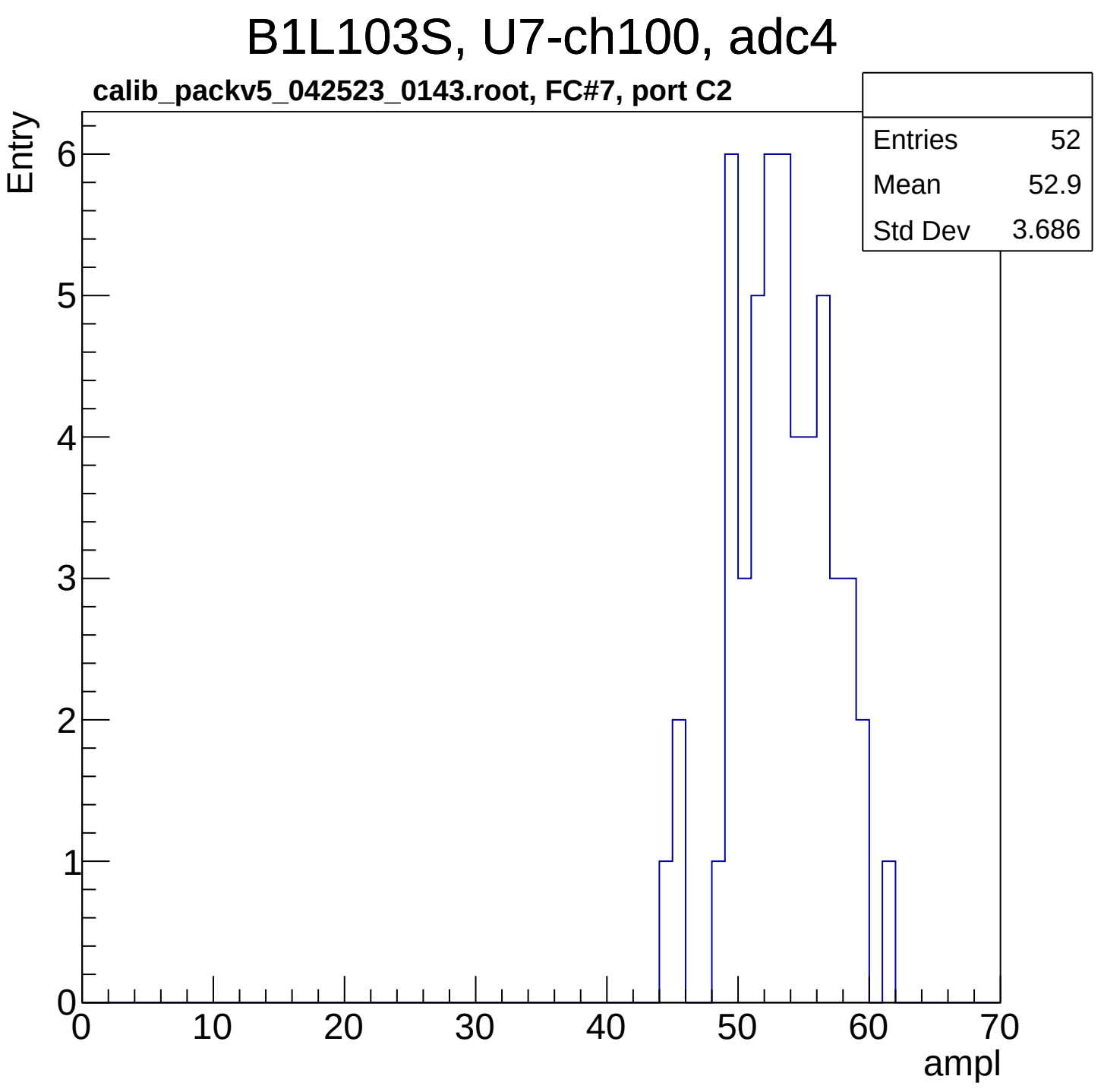

B1L103S, U7-ch100, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 54
Mean 47.41
Std Dev 3.813
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch100, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 52
Mean 52.9
Std Dev 3.686
Entry
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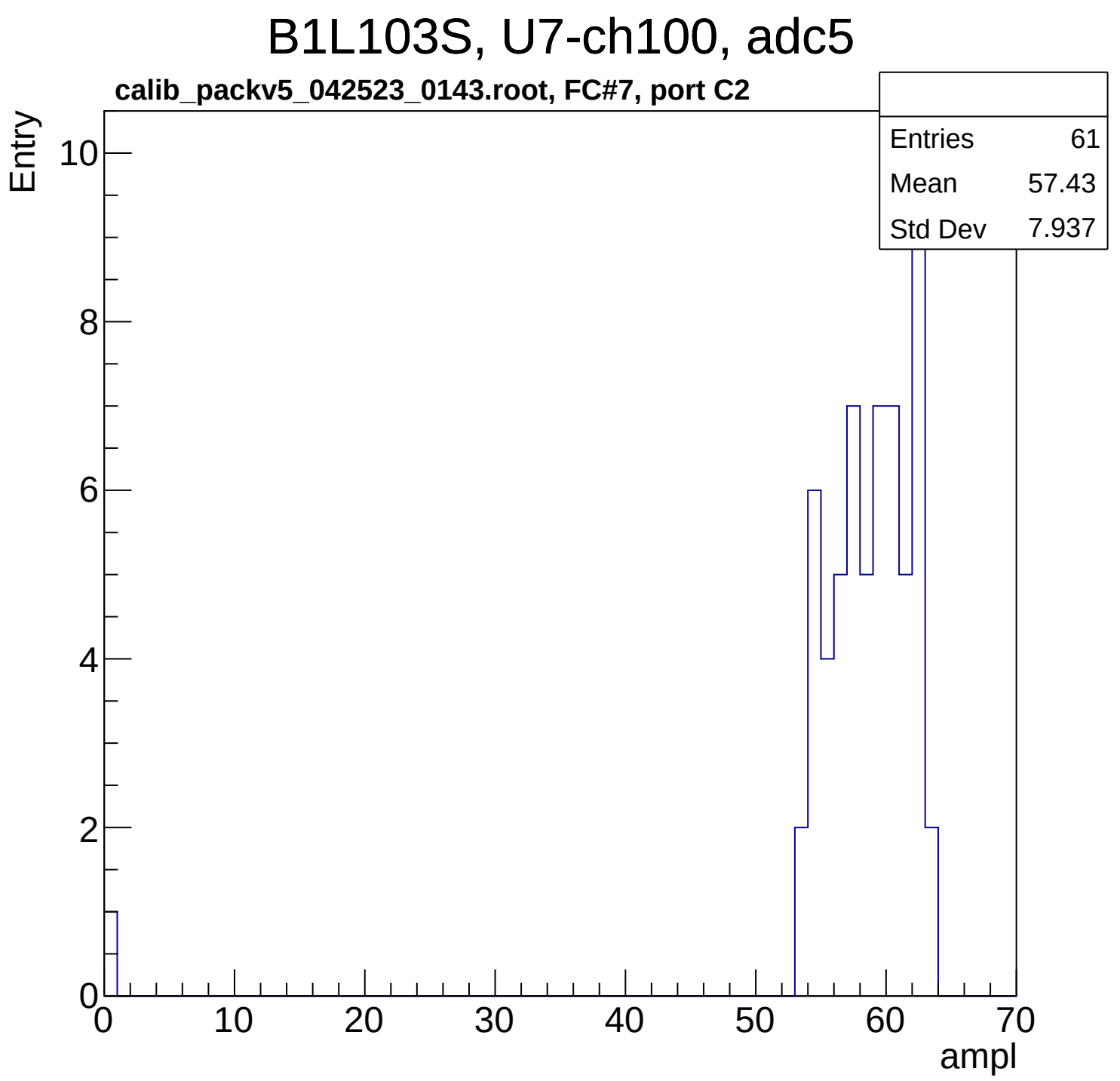
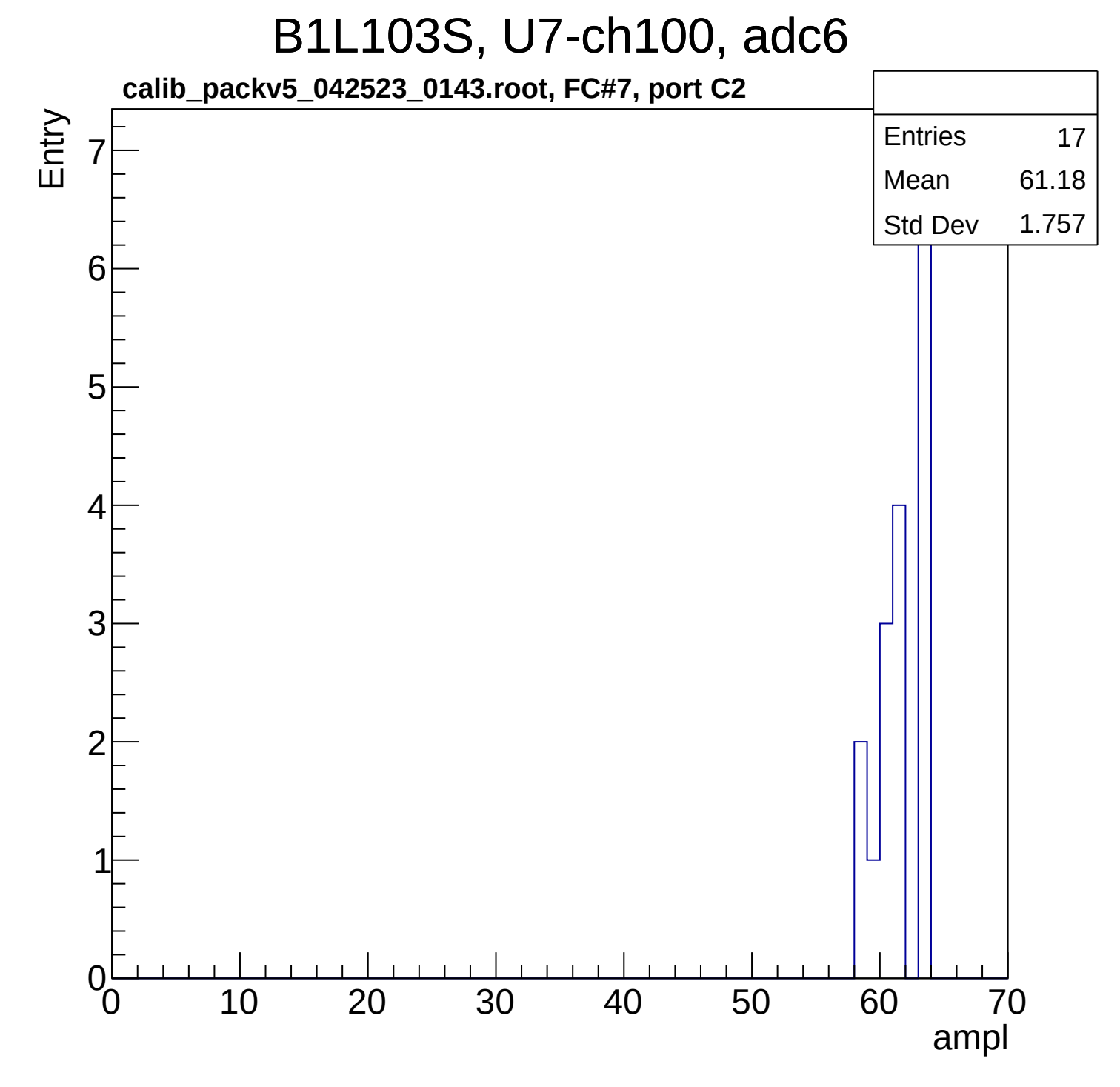
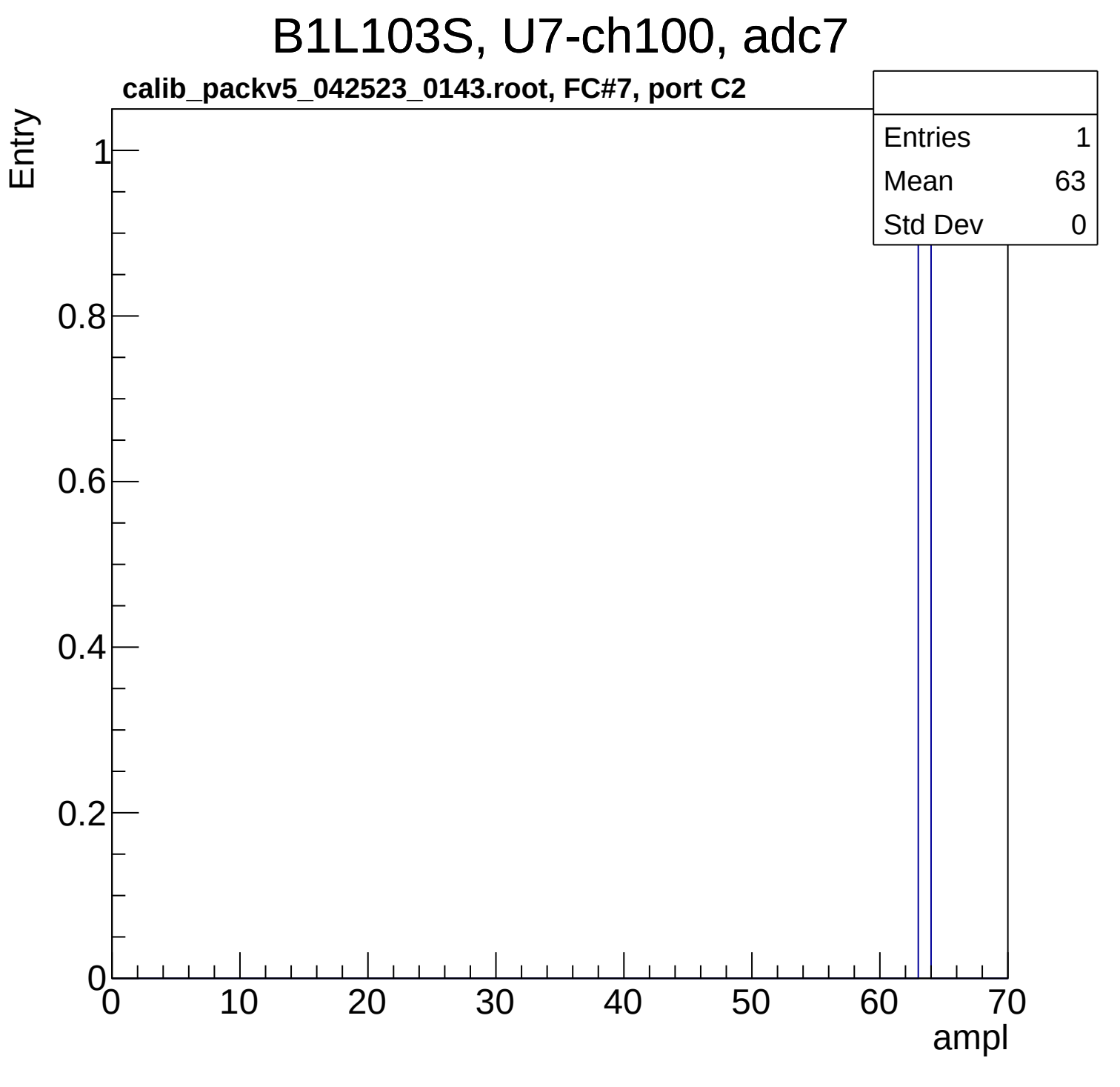
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch100, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 61
Mean 57.43
Std Dev 7.937
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch100, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 17
Mean 61.18
Std Dev 1.757
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch100, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 63
Std Dev 0
Entry
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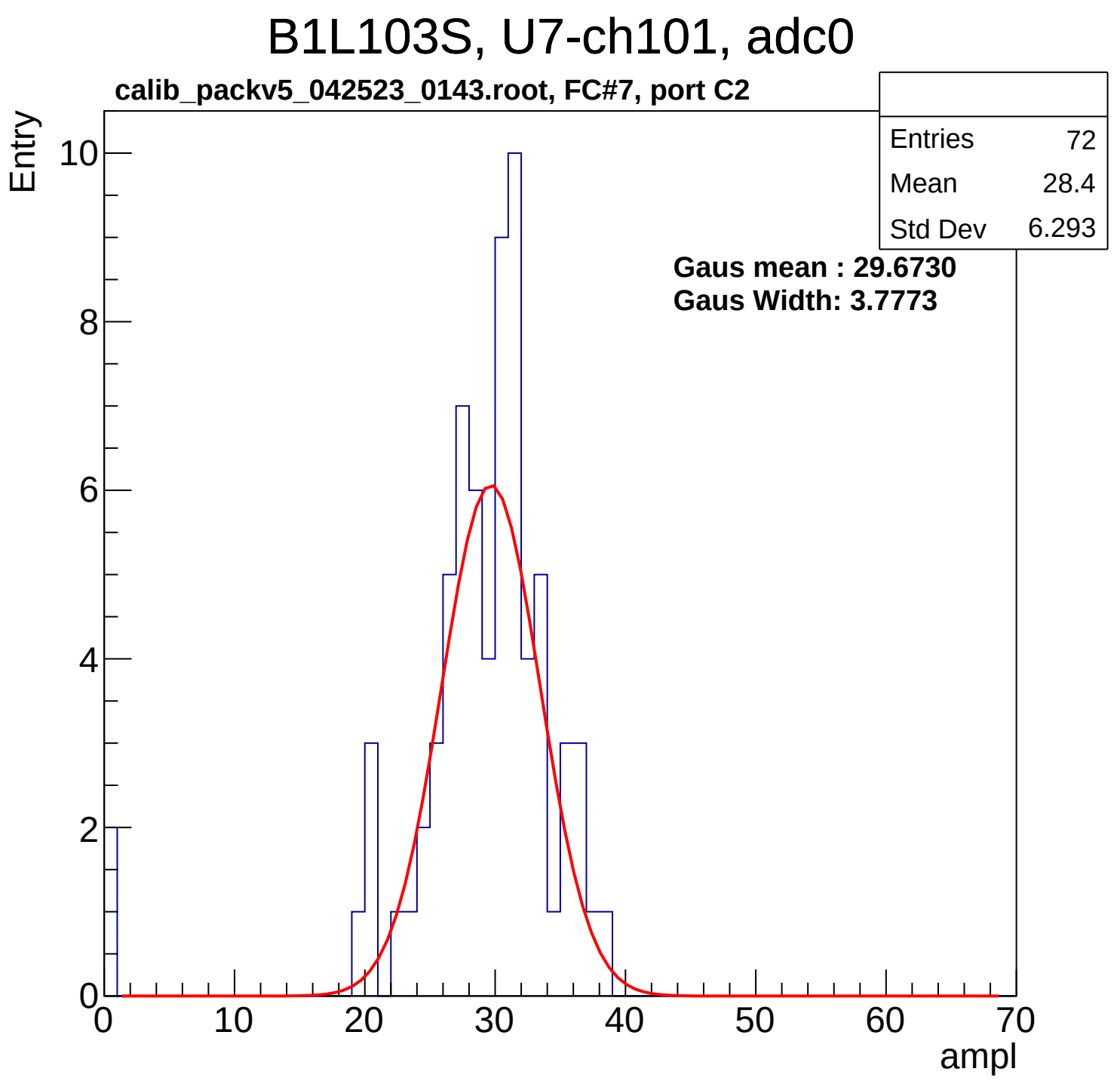
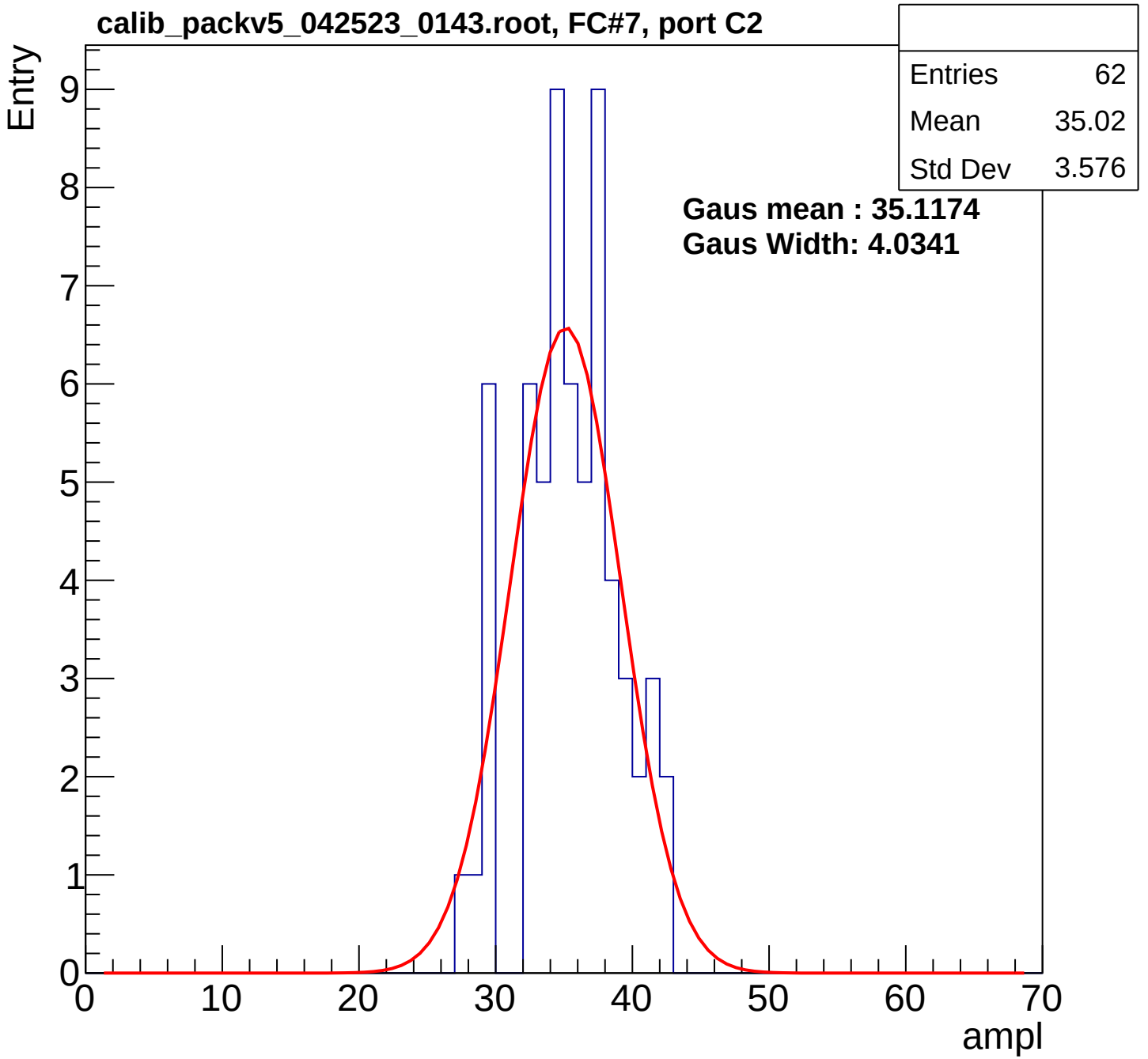
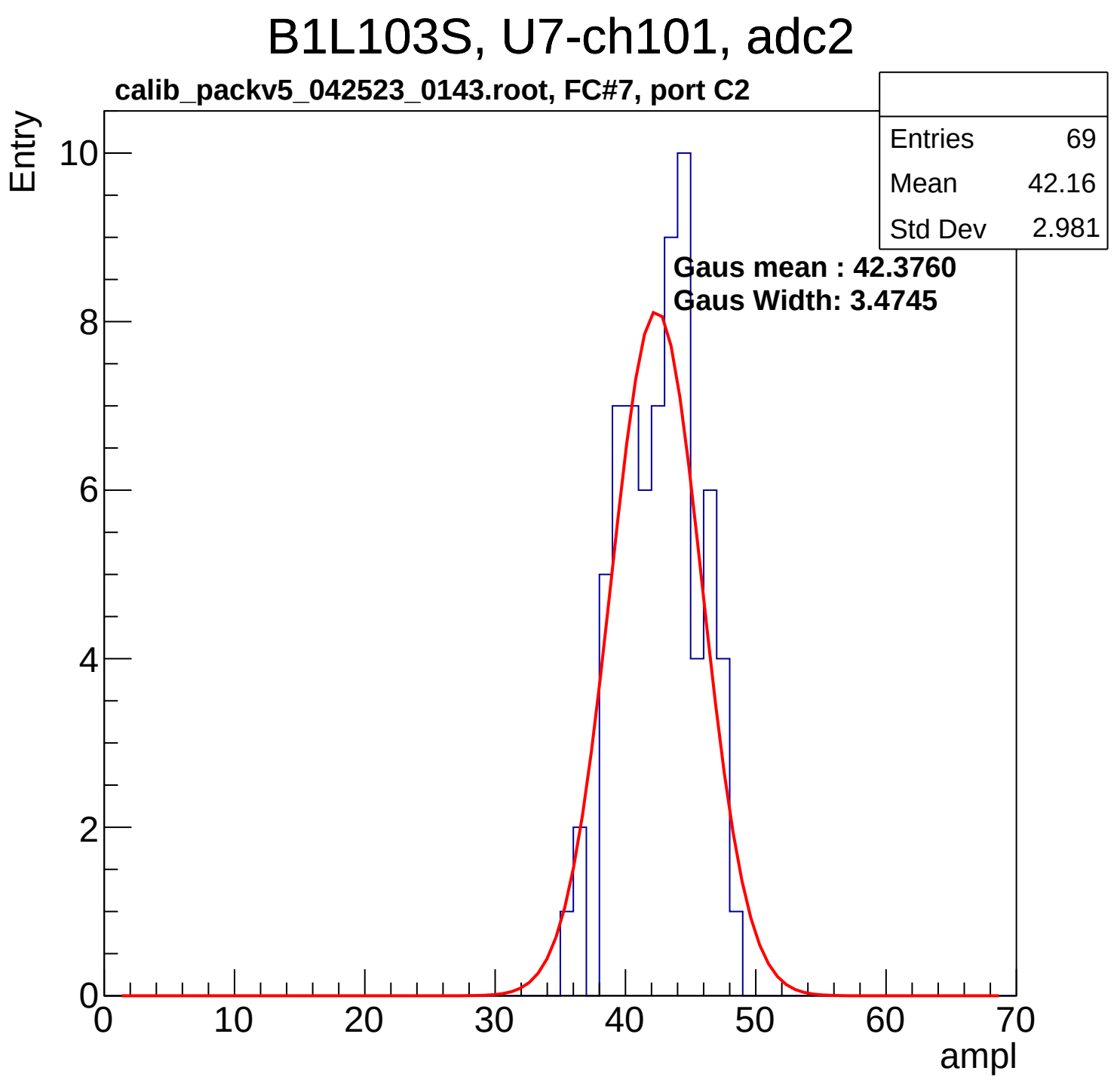
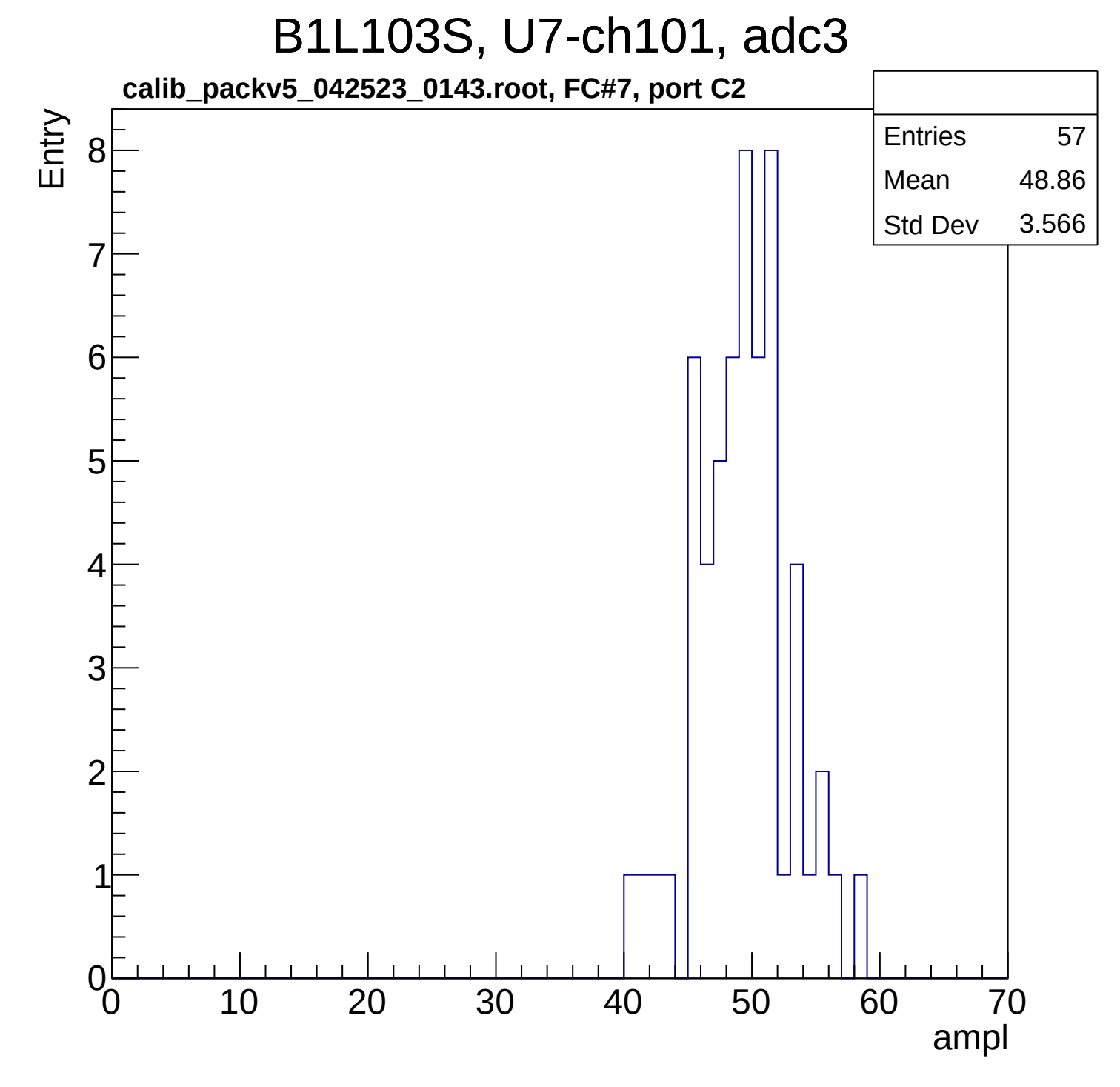
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch101, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 72
Mean 28.4
Std Dev 6.293
Gaus mean : 29.6730
Gaus Width: 3.7773
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch101, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 62
Mean 35.02
Std Dev 3.576
Gaus mean : 35.1174
Gaus Width: 4.0341
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch101, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 42.16
Std Dev 2.981
Gaus mean : 42.3760
Gaus Width: 3.4745
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch101, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 48.86
Std Dev 3.566
Entry
ampl
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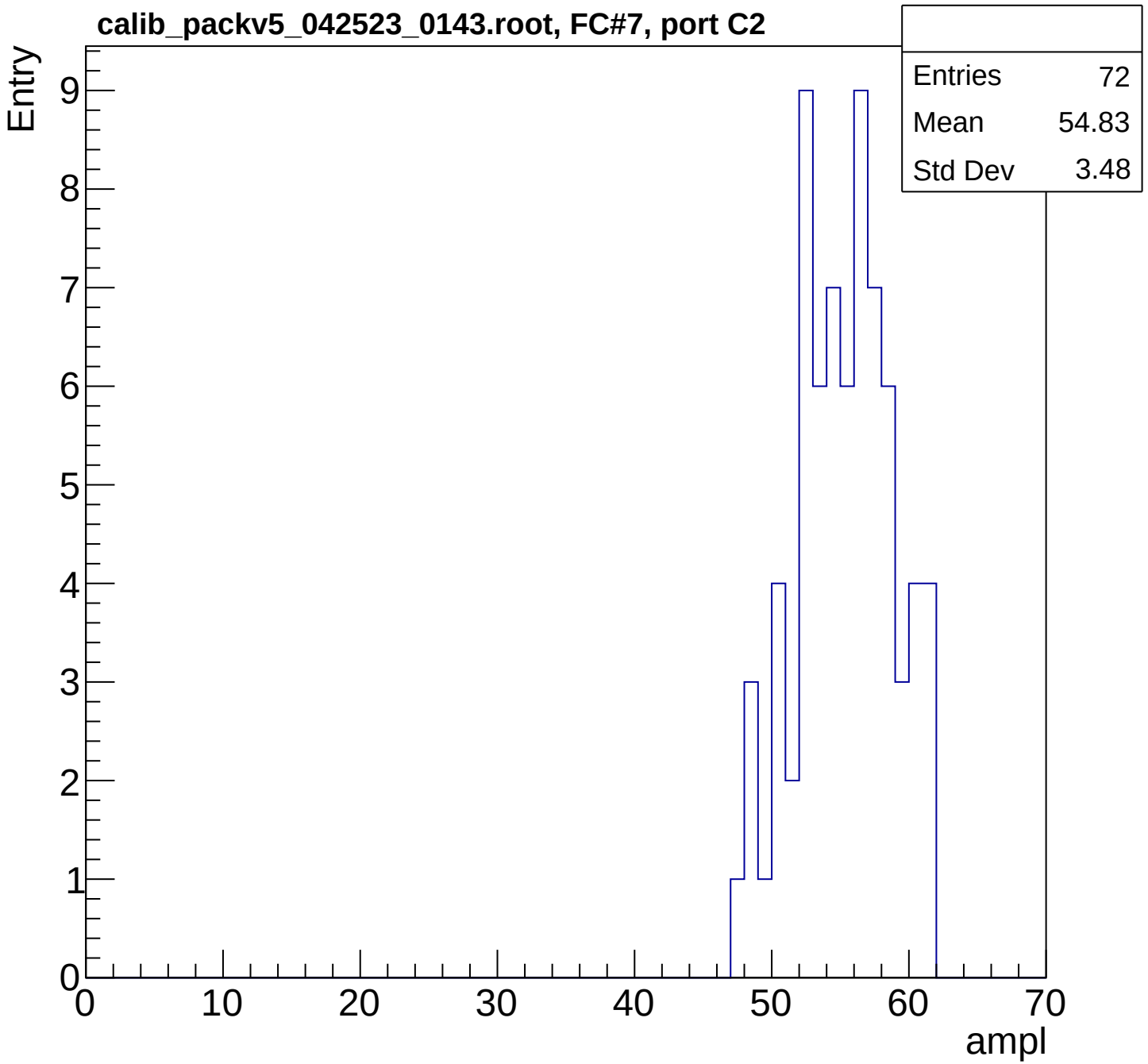
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch101, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 72
Mean 54.83
Std Dev 3.48
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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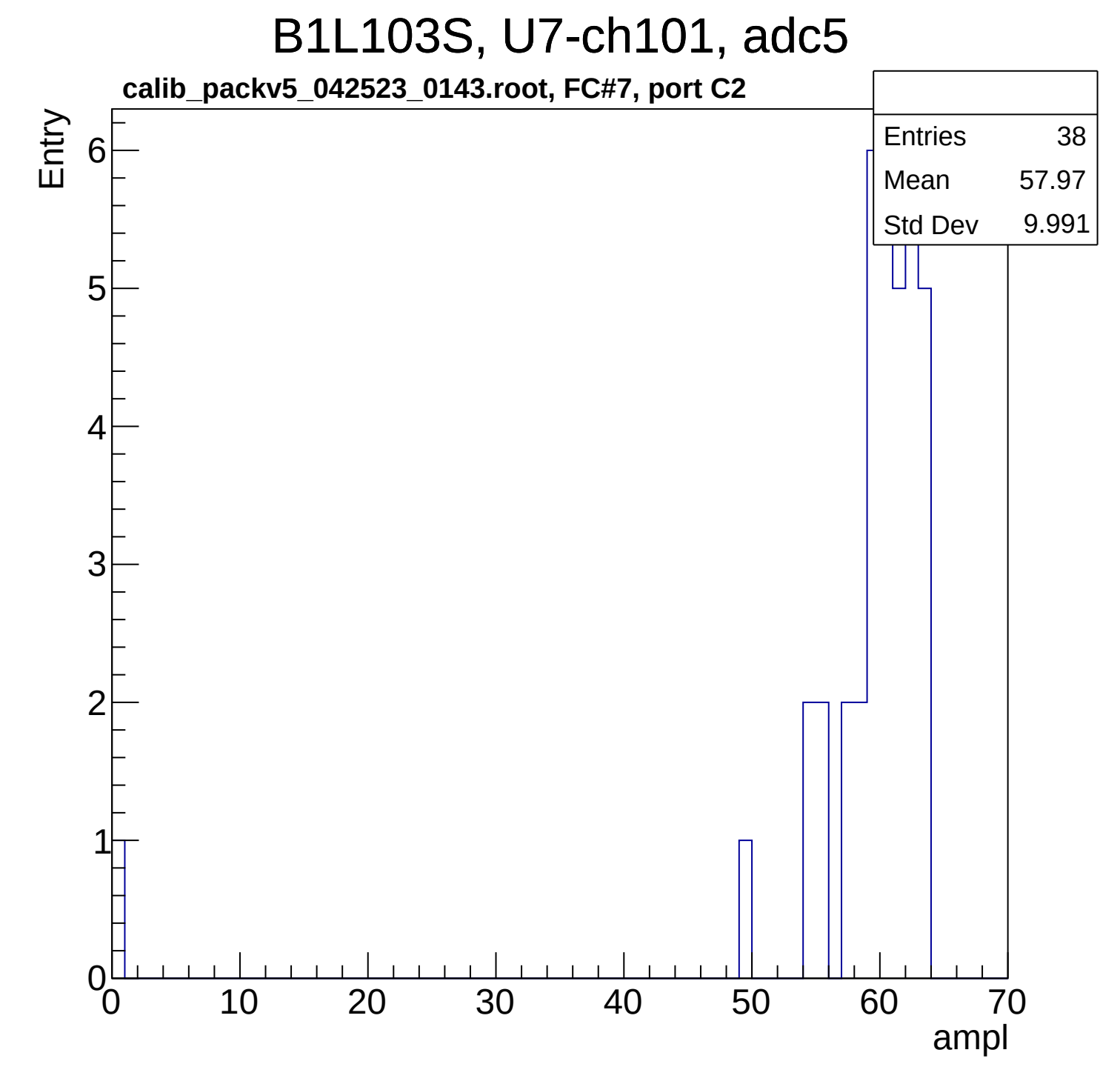
B1L103S, U7-ch101, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 38
Mean 57.97
Std Dev 9.991
Entry
ampl
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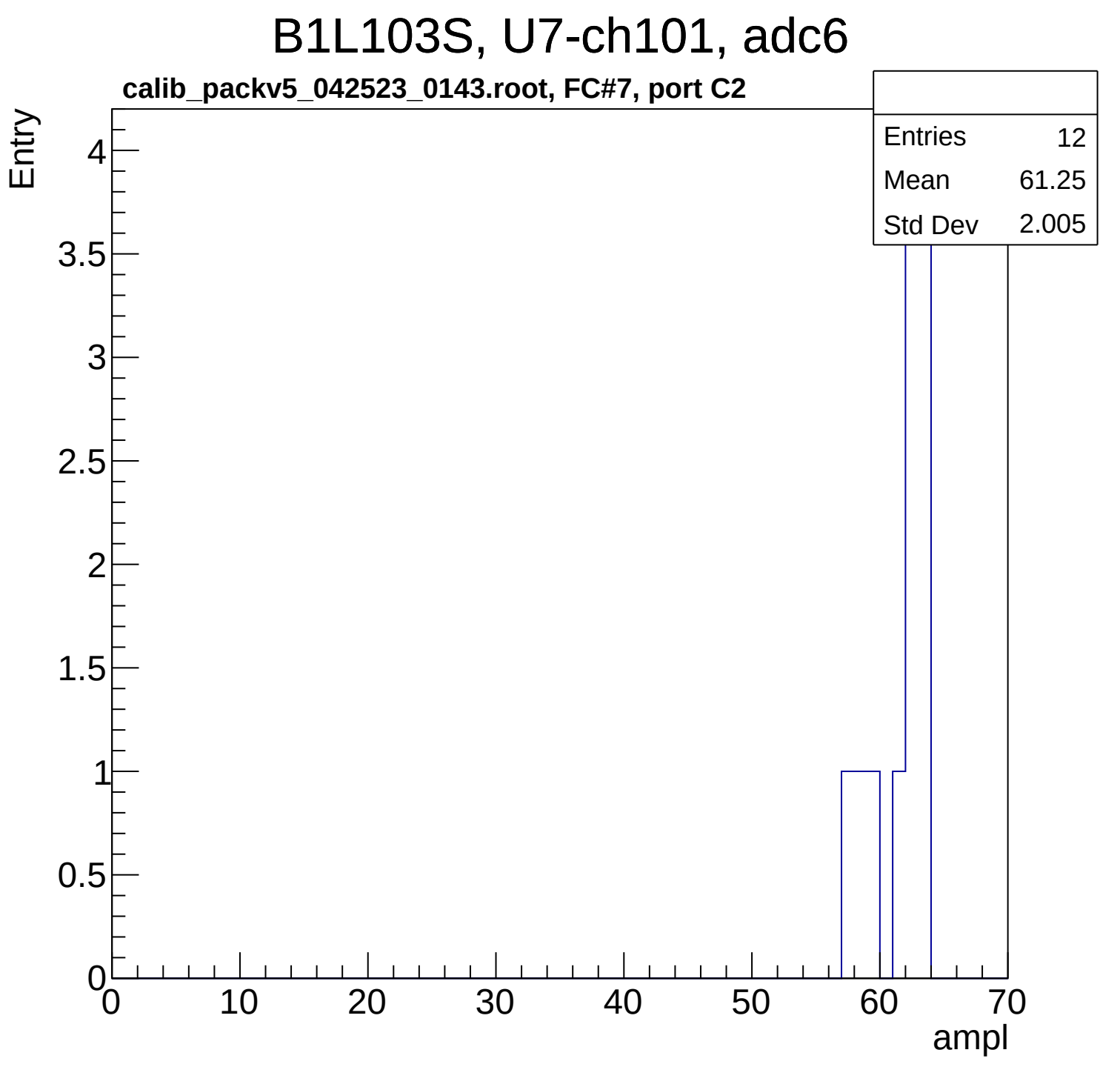
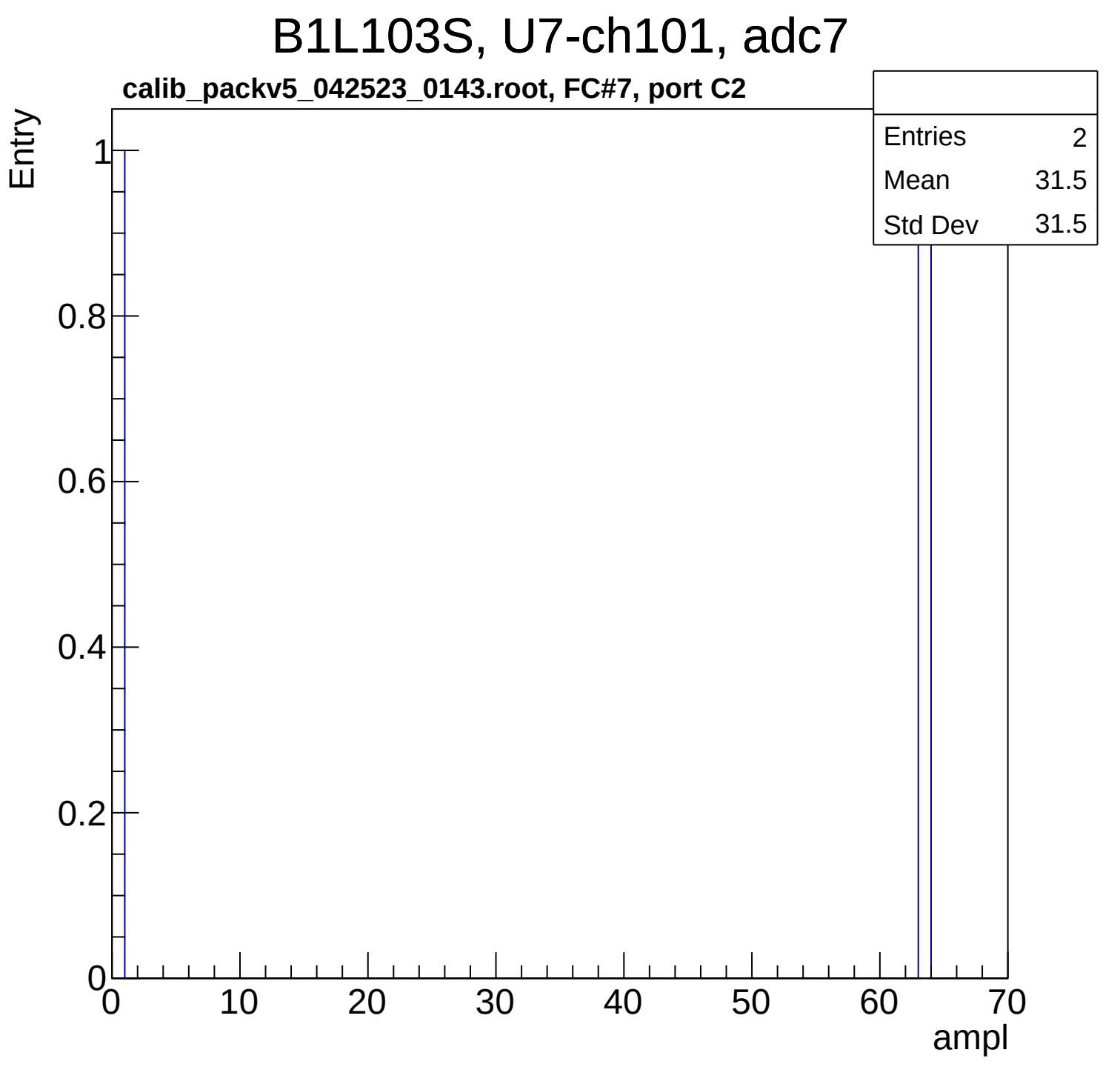
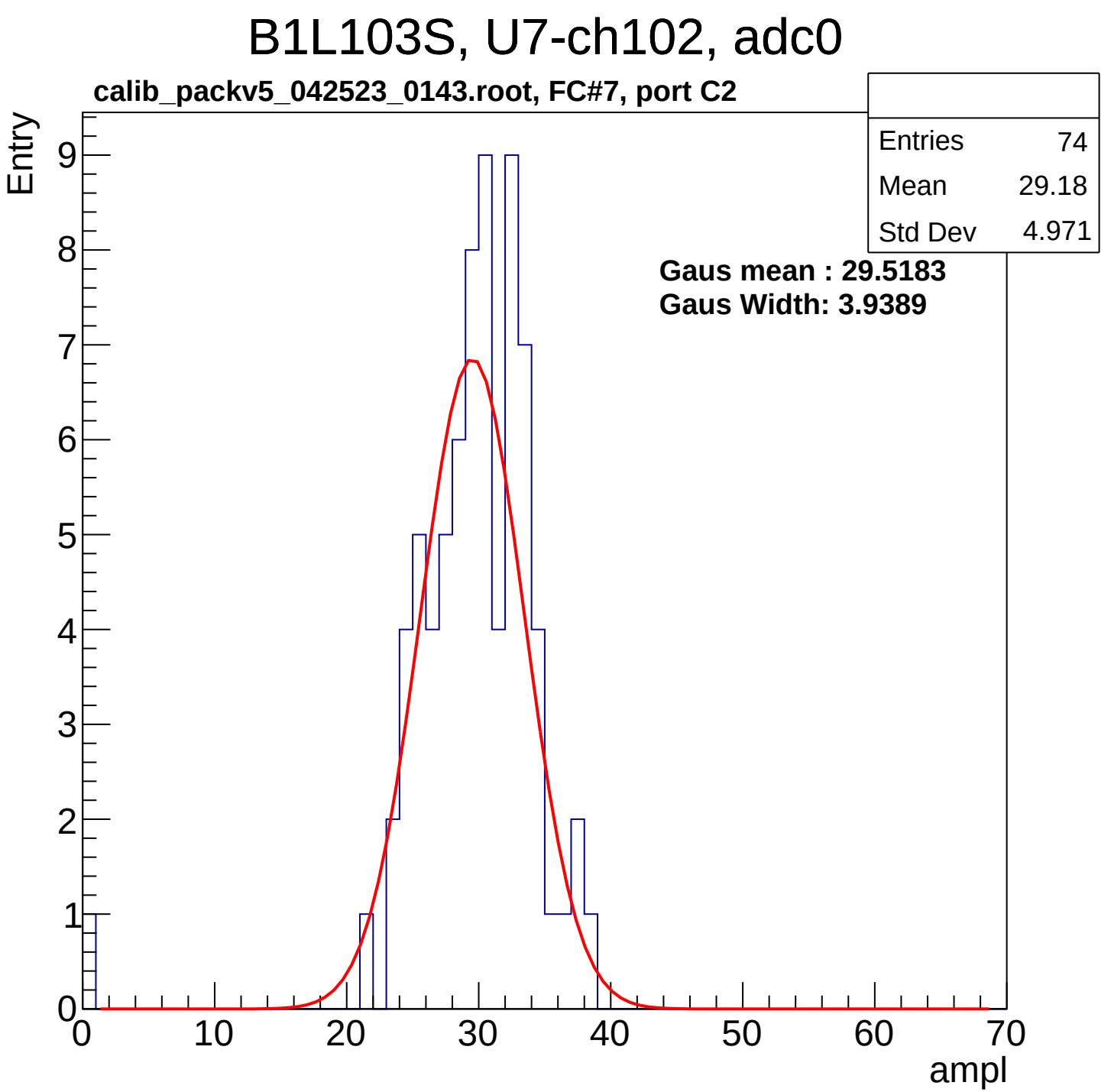
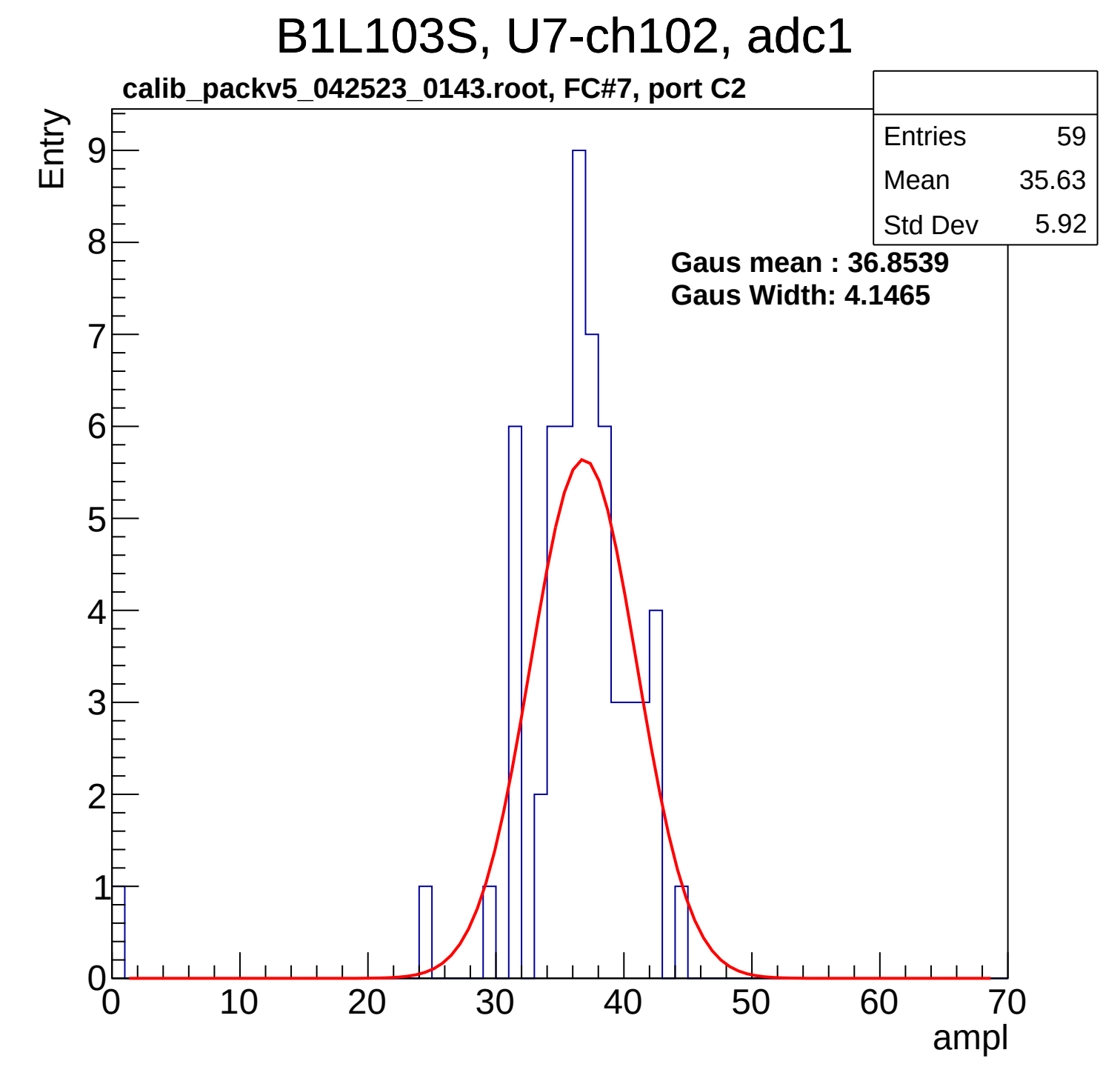
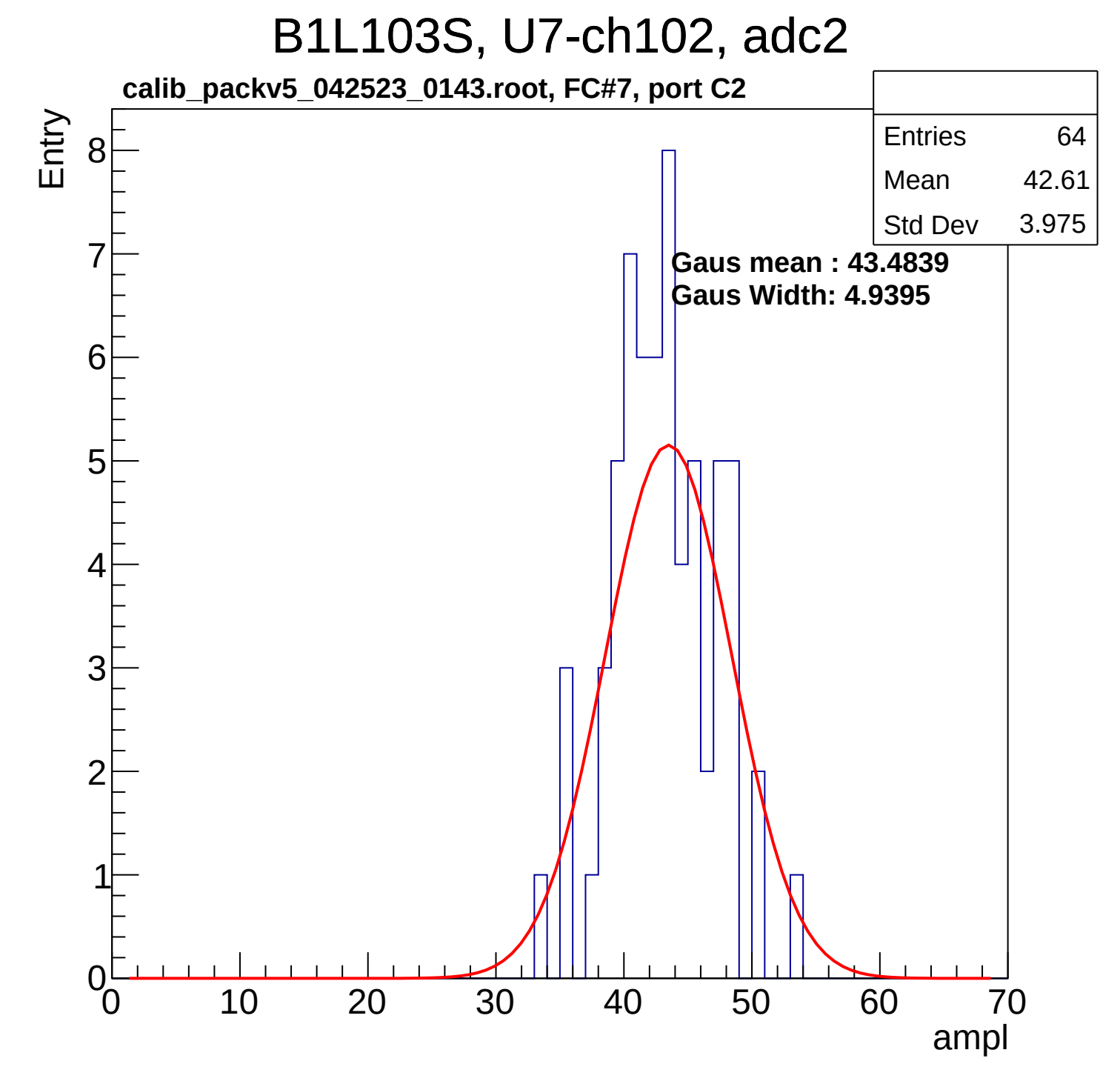
3
4
5
6
0
10
20
30
40
50
60
70

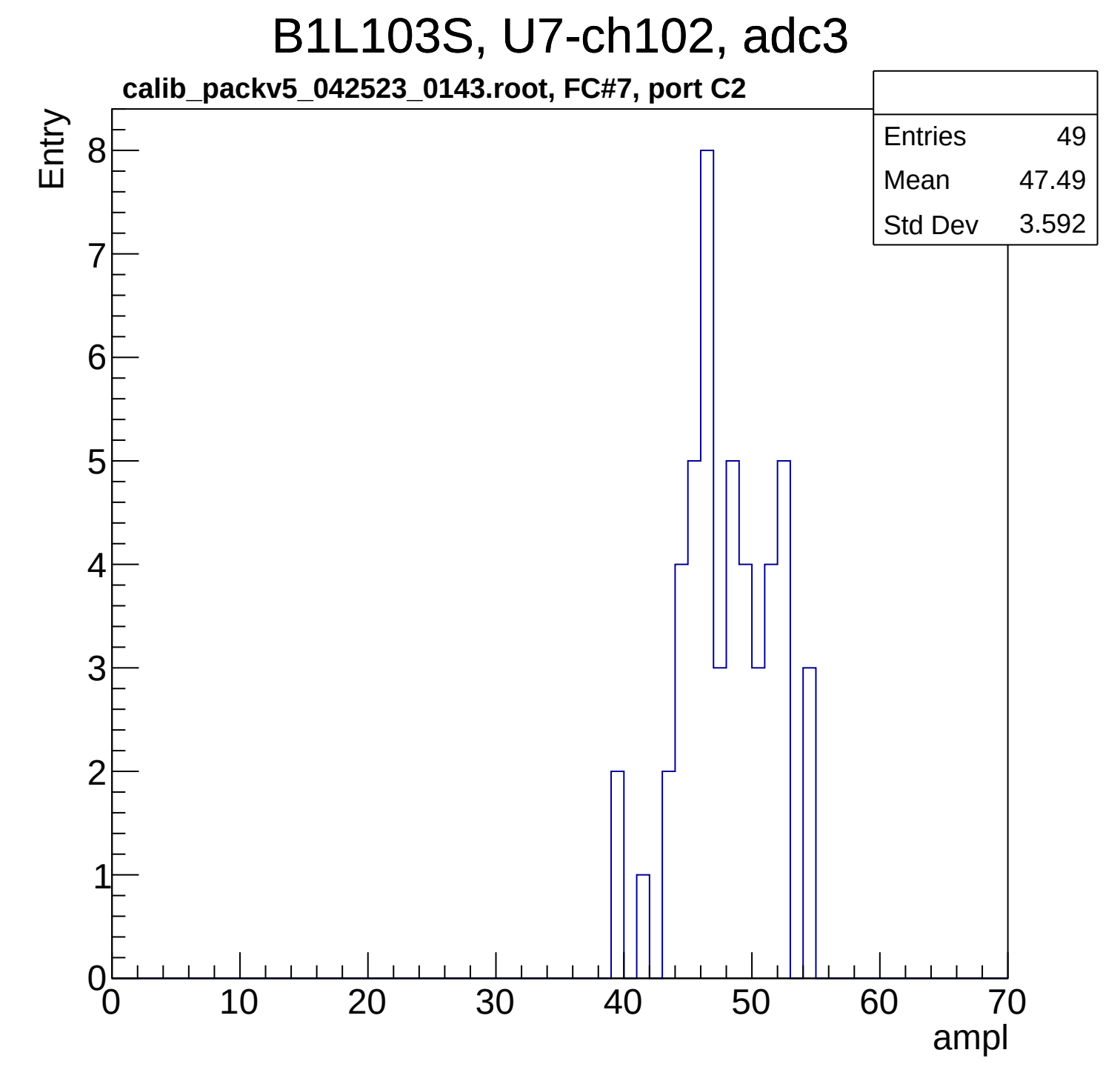

B1L103S, U7-ch101, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 12
Mean 61.25
Std Dev 2.005
Entry
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70
ampl

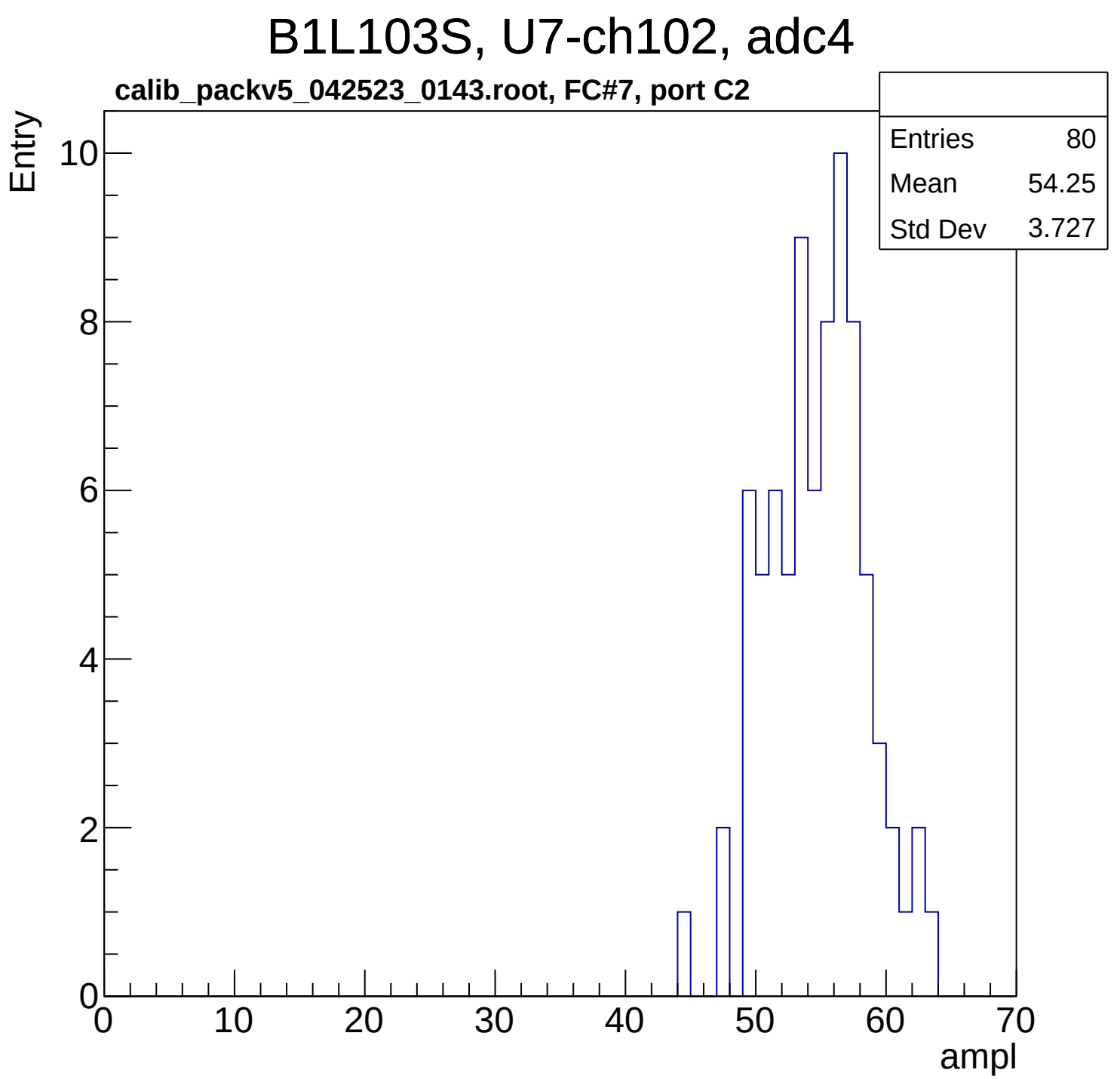

B1L103S, U7-ch101, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 31.5
Std Dev 31.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

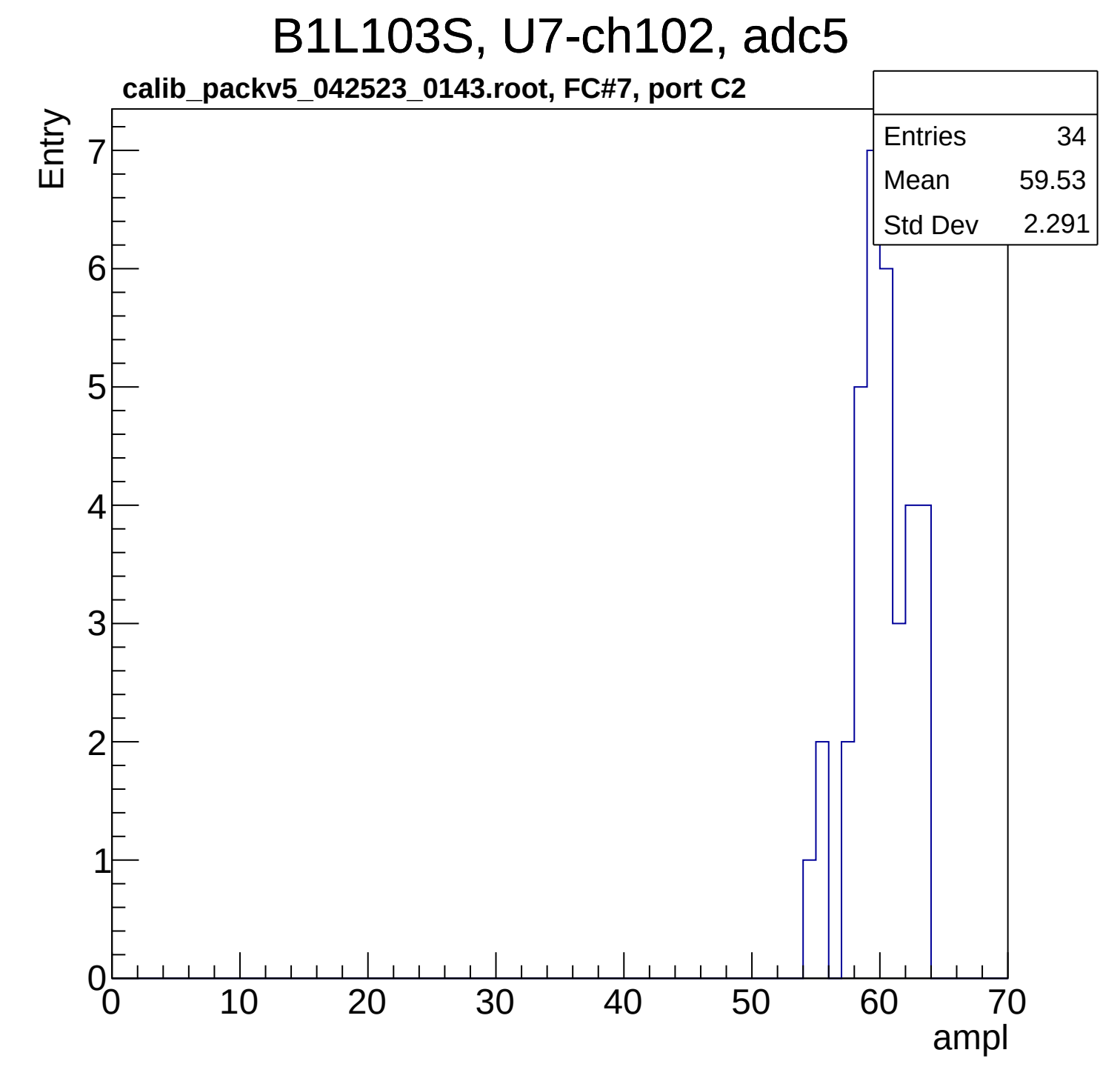

B1L103S, U7-ch102, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 74
Mean 29.18
Std Dev 4.971
Gaus mean : 29.5183
Gaus Width: 3.9389
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch102, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 35.63
Std Dev 5.92
Gaus mean : 36.8539
Gaus Width: 4.1465
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch102, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 42.61
Std Dev 3.975
Gaus mean : 43.4839
Gaus Width: 4.9395
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch102, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 49
Mean 47.49
Std Dev 3.592
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch102, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 80
Mean 54.25
Std Dev 3.727
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch102, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 34
Mean 59.53
Std Dev 2.291
Entry
ampl
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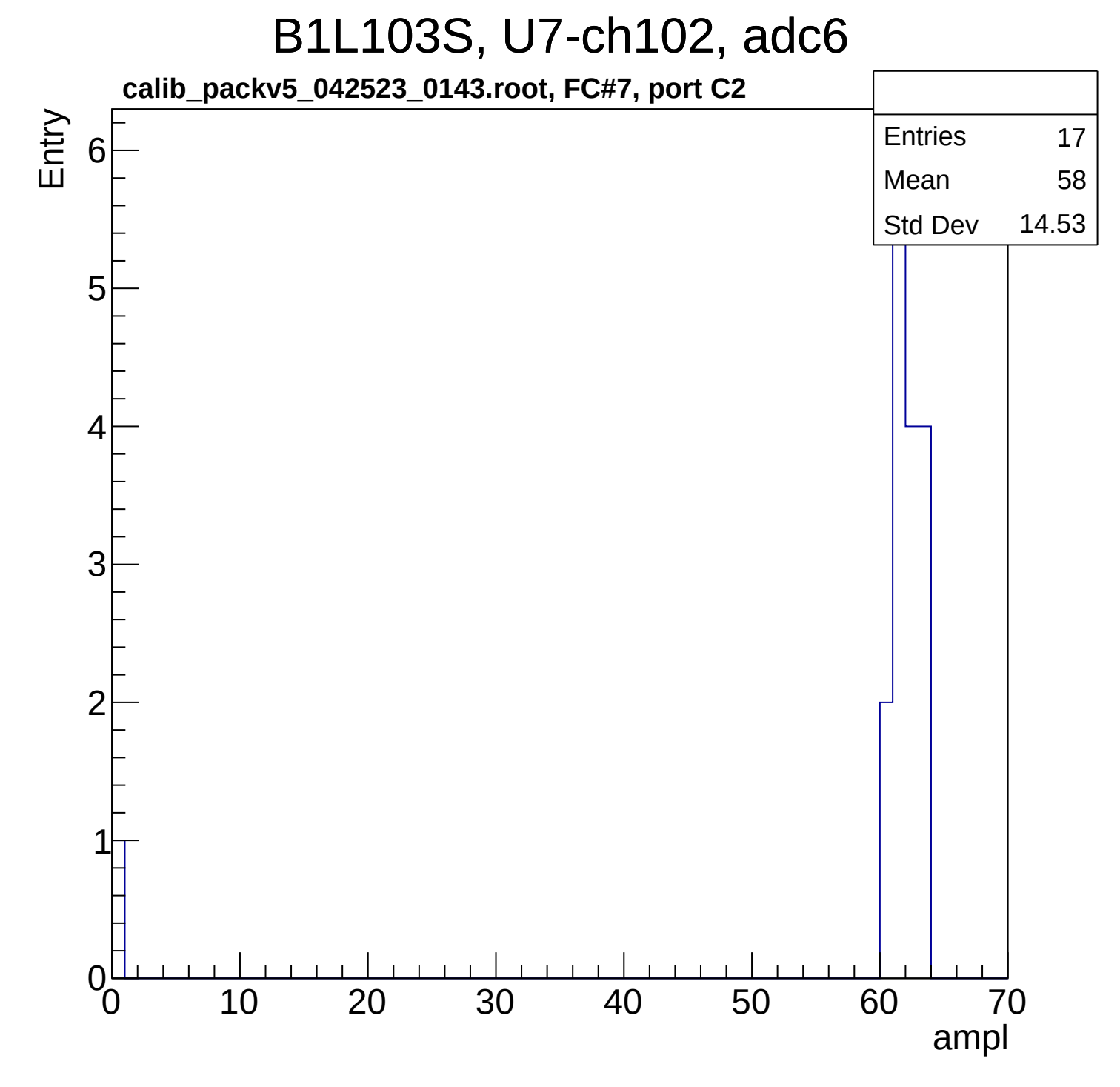
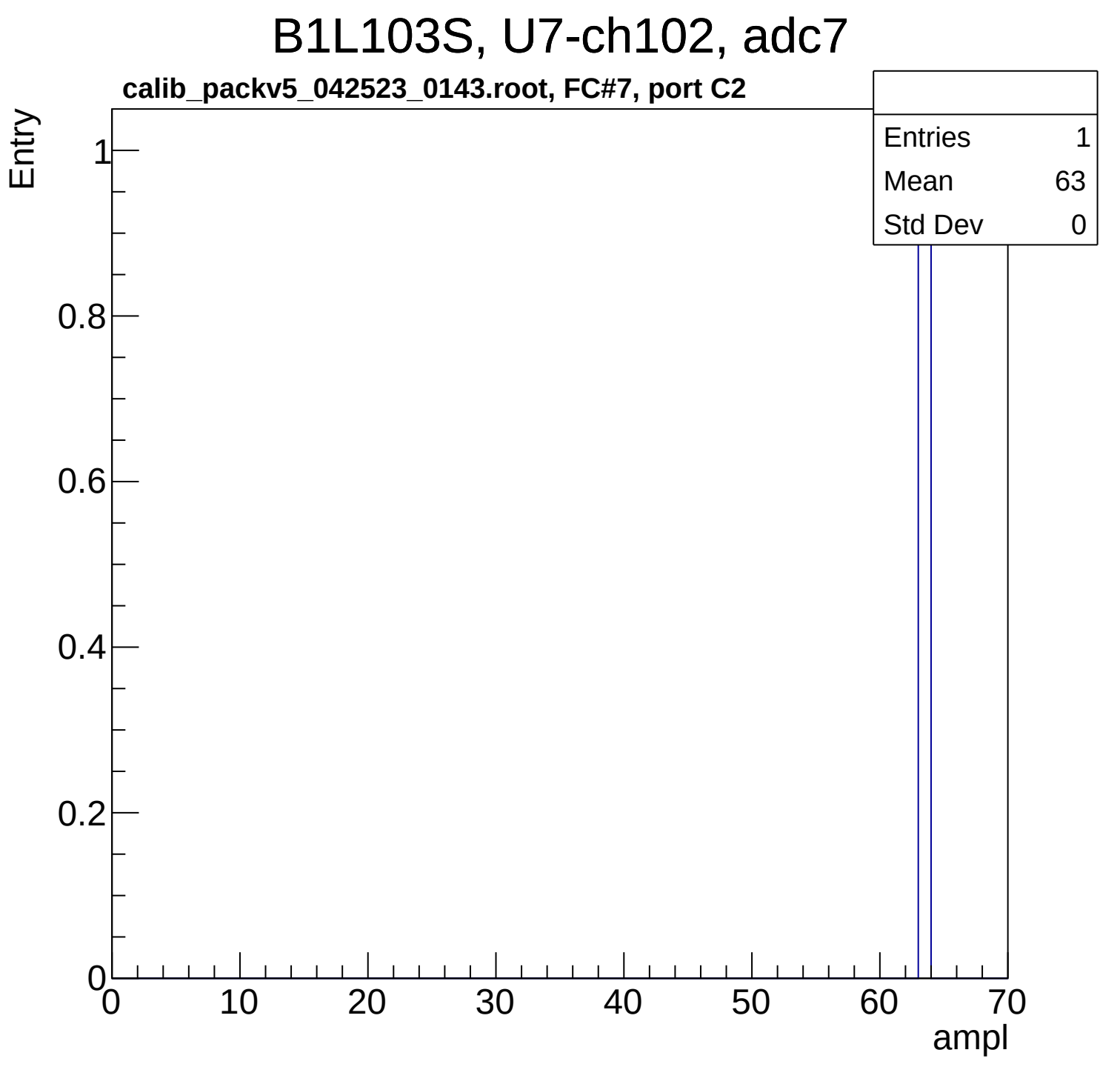
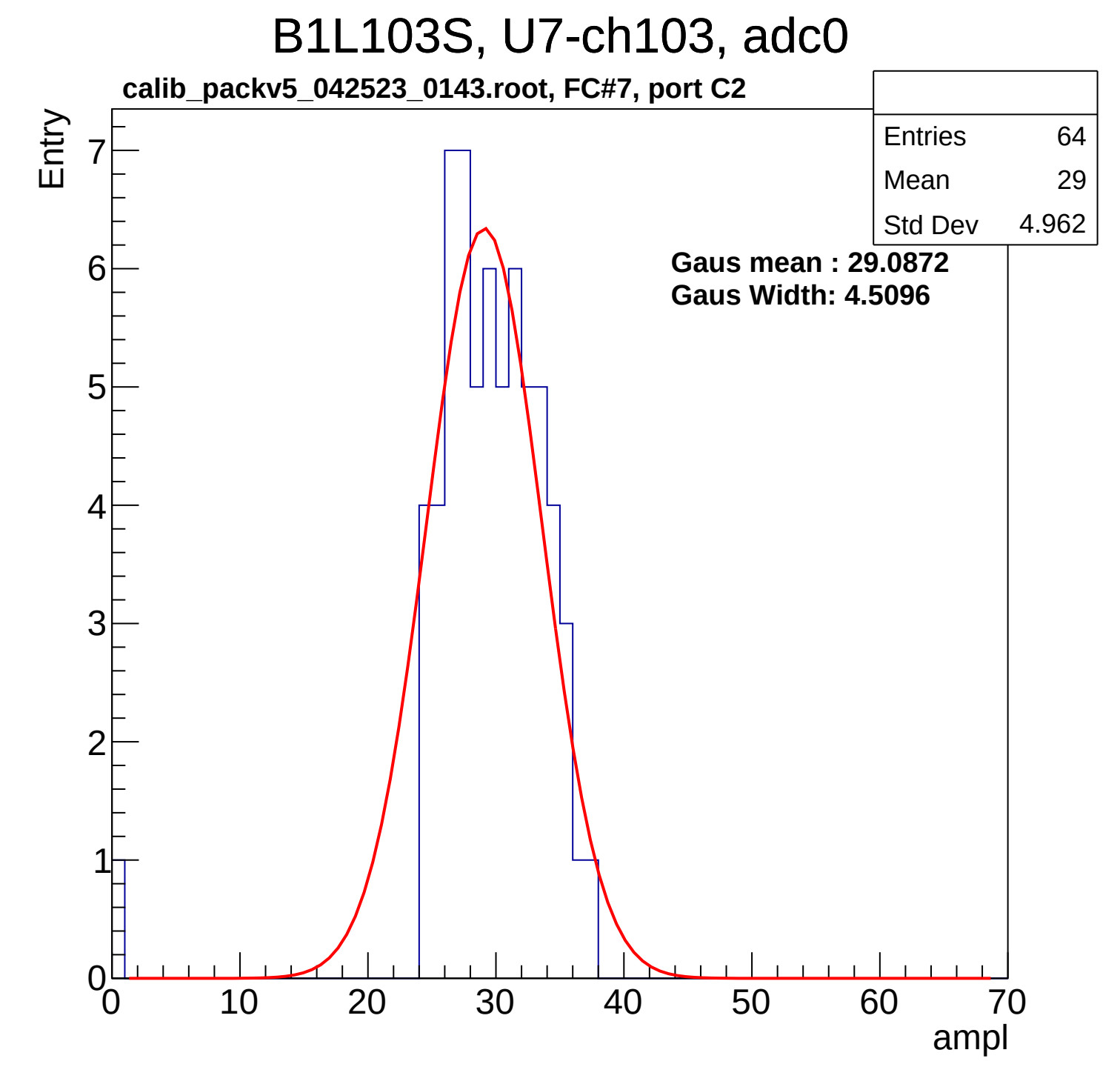
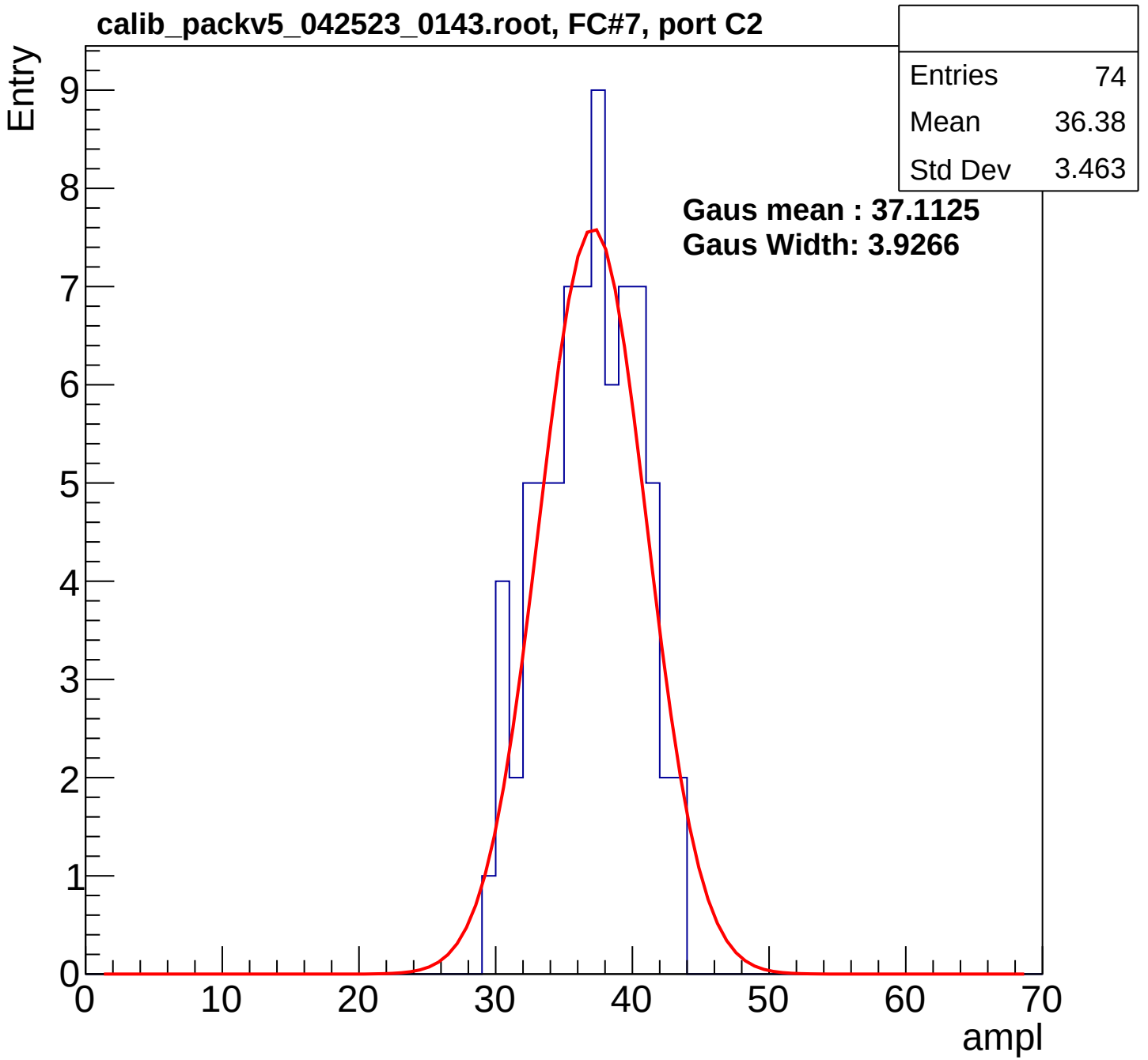
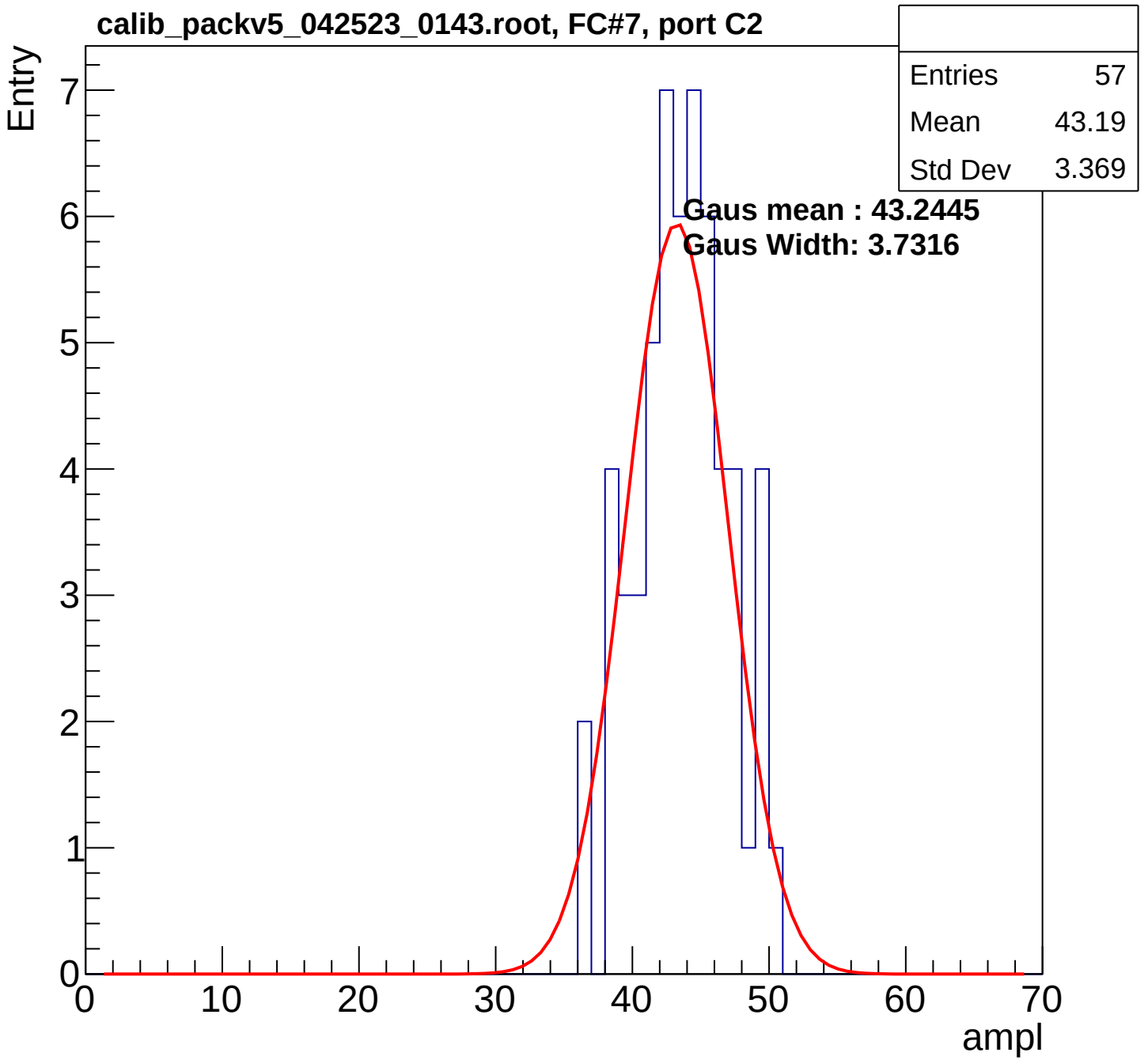
2
3
4
5
6
7
0
10
20
30
40
50
60
70

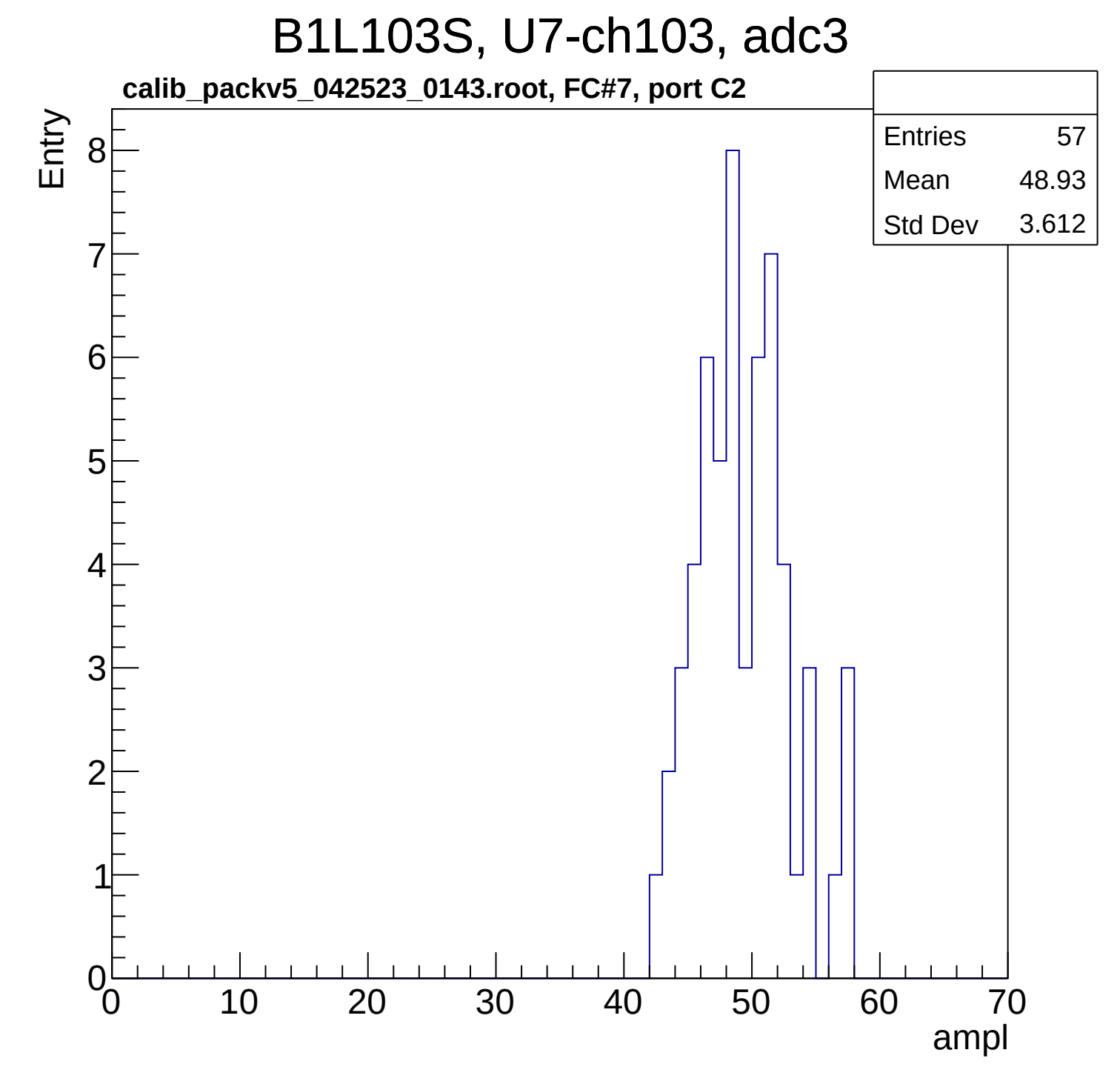

B1L103S, U7-ch102, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 17
Mean 58
Std Dev 14.53
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

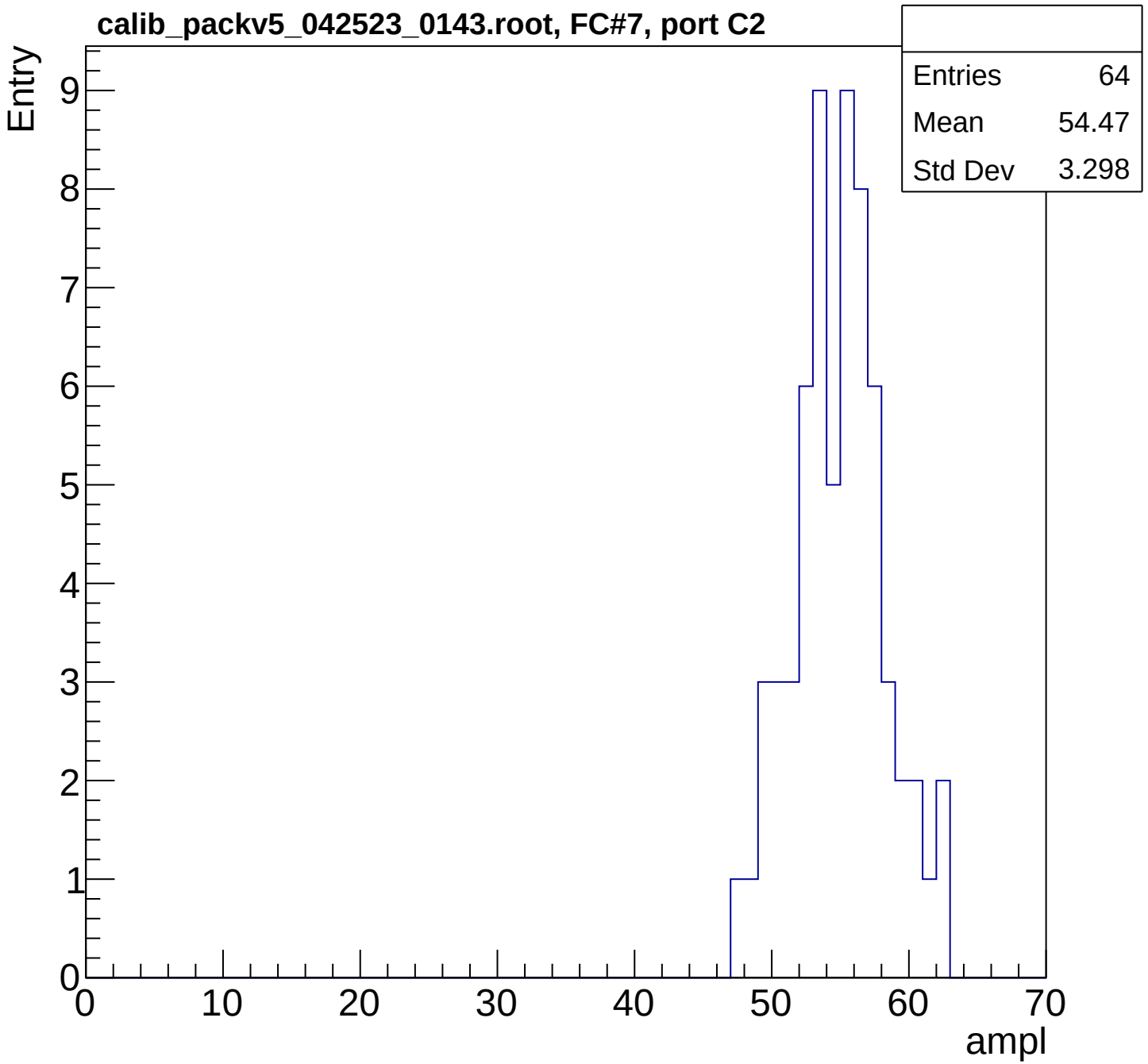

B1L103S, U7-ch102, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

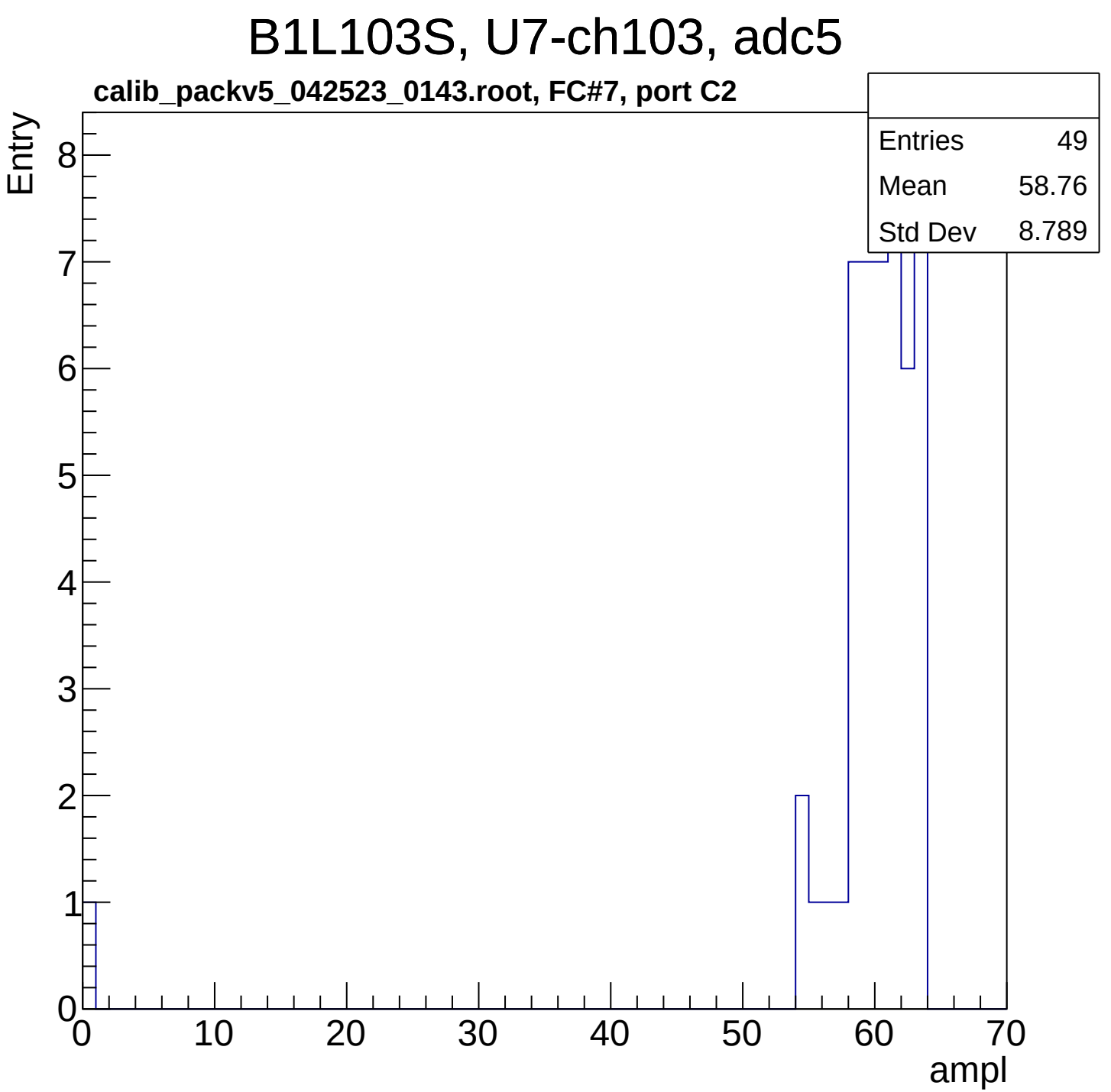

B1L103S, U7-ch103, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 29
Std Dev 4.962
Gaus mean : 29.0872
Gaus Width: 4.5096
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

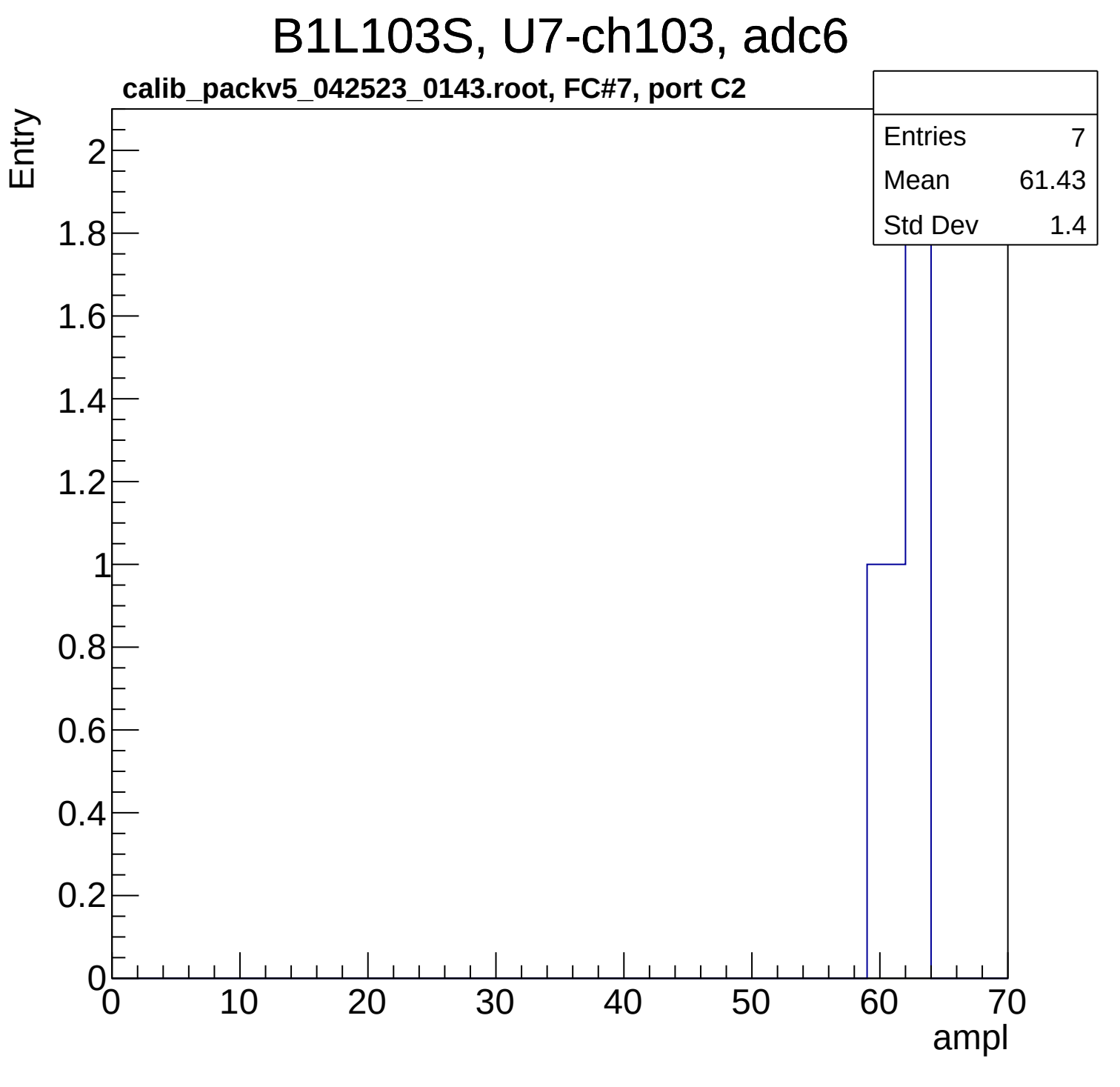

B1L103S, U7-ch103, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 74
Mean 36.38
Std Dev 3.463
Gaus mean : 37.1125
Gaus Width: 3.9266
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

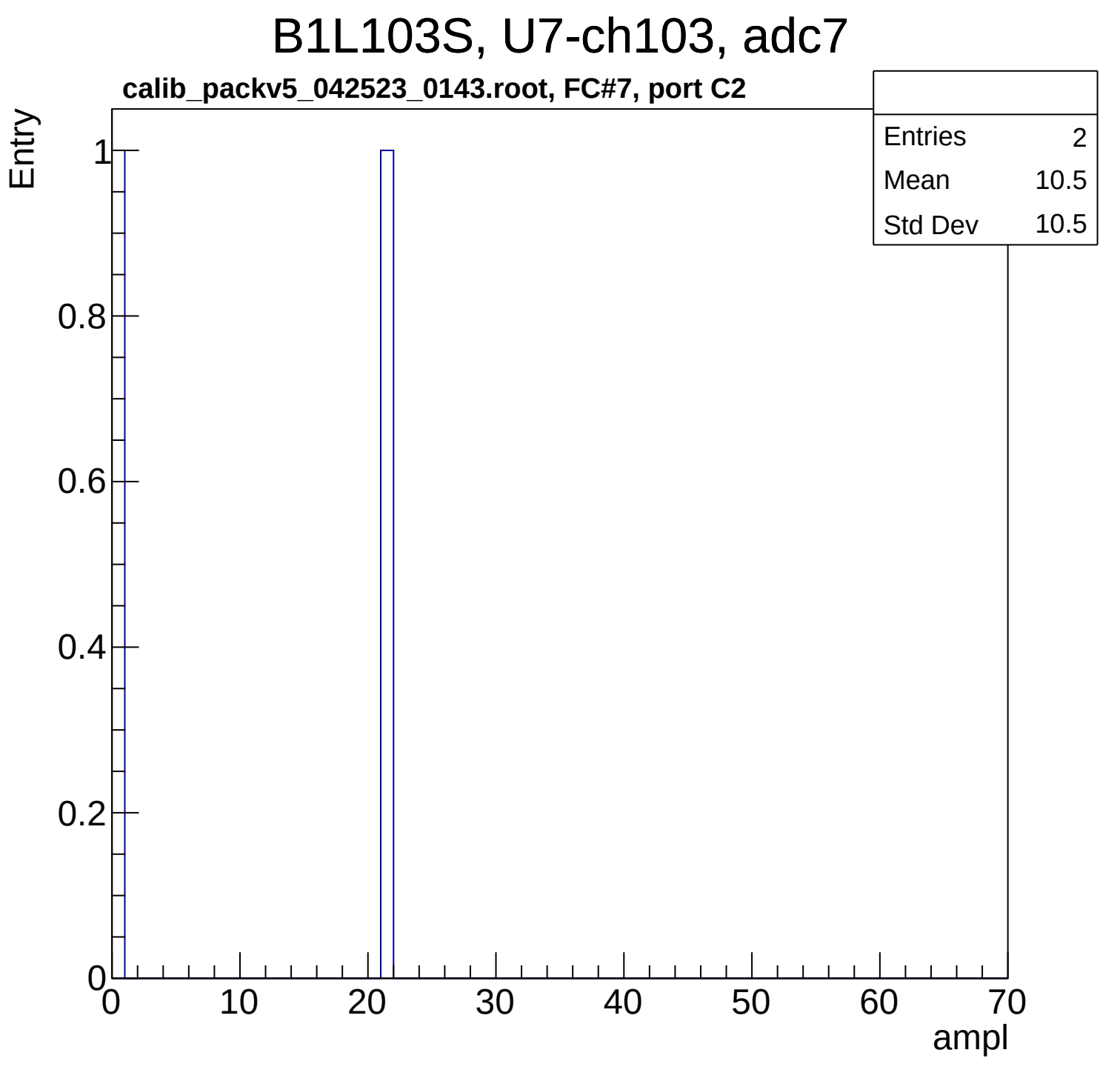

B1L103S, U7-ch103, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 43.19
Std Dev 3.369
Gaus mean : 43.2445
Gaus Width: 3.7316
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

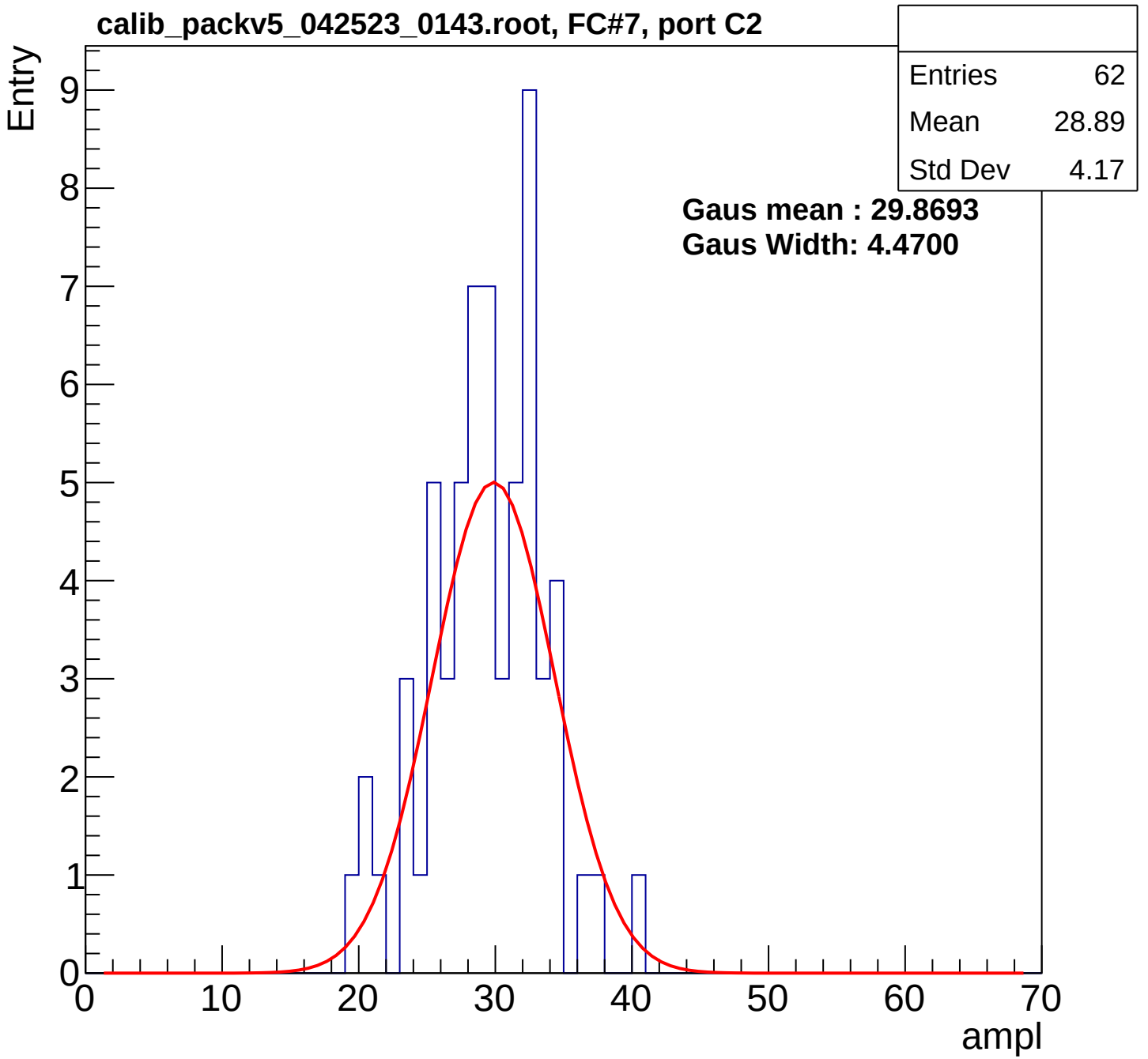

B1L103S, U7-ch103, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 48.93
Std Dev 3.612
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

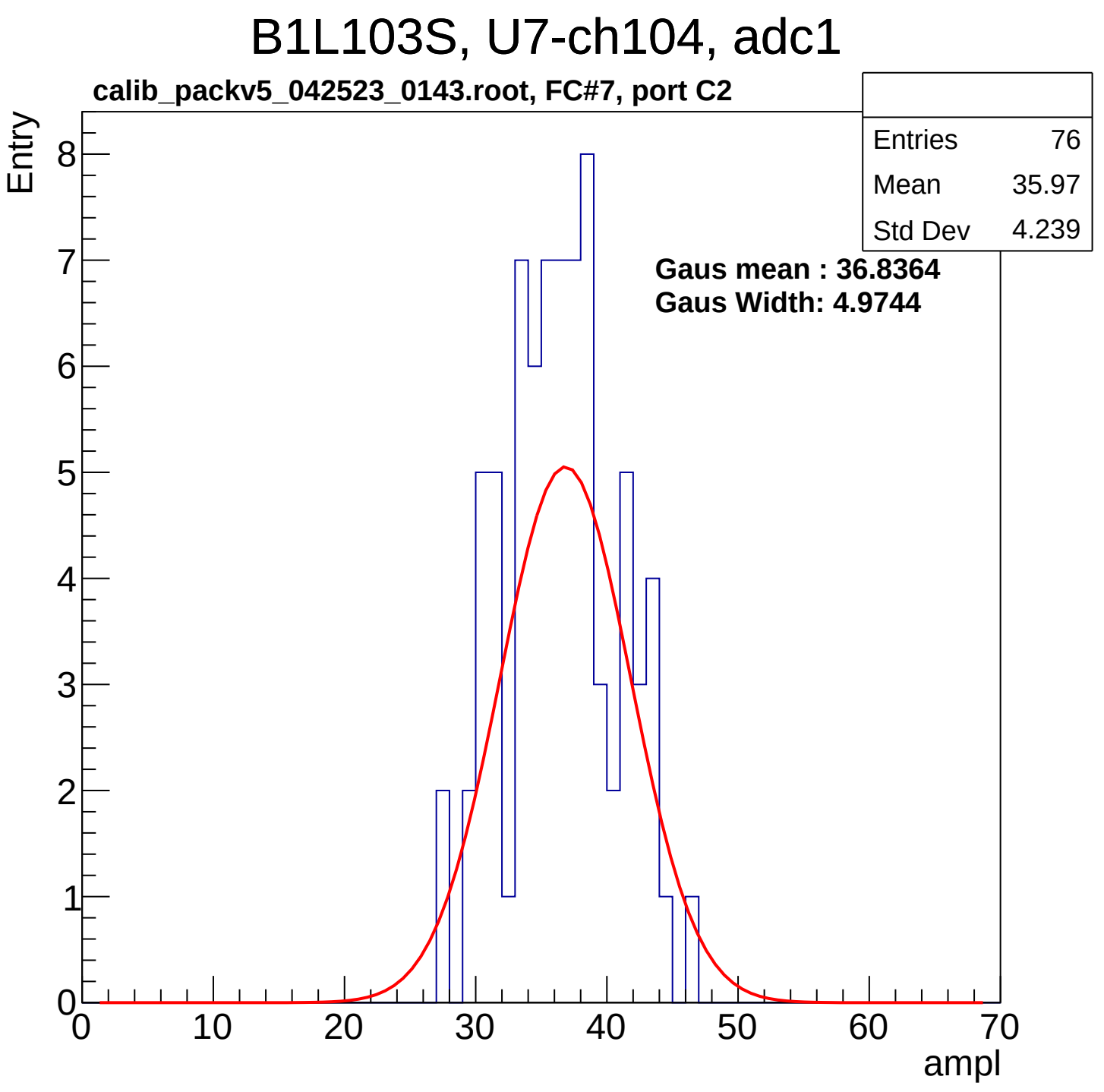

B1L103S, U7-ch103, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 54.47
Std Dev 3.298
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

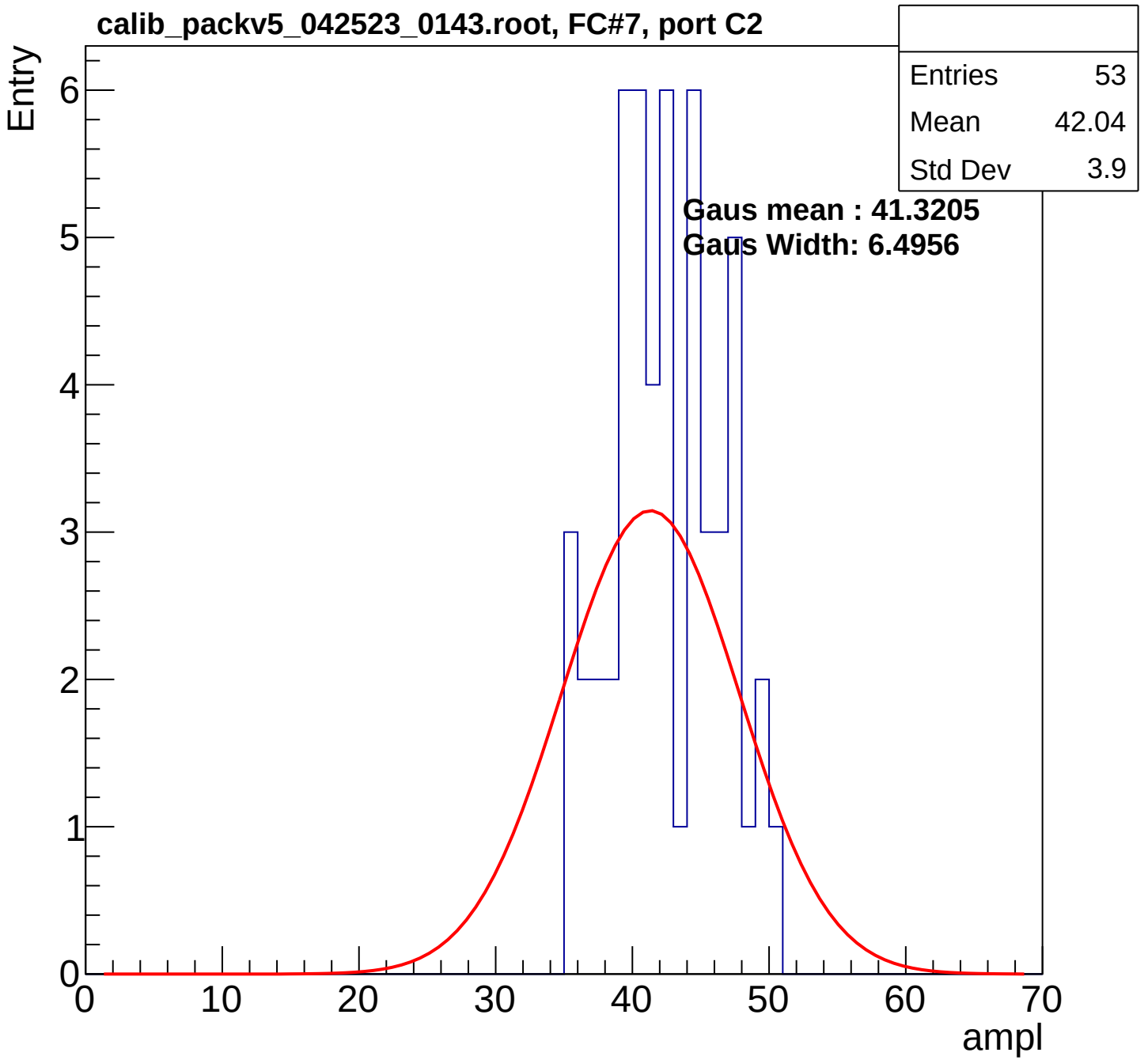

B1L103S, U7-ch103, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 49
Mean 58.76
Std Dev 8.789
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch103, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 7
Mean 61.43
Std Dev 1.4
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U7-ch103, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 10.5
Std Dev 10.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch104, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 62
Mean 28.89
Std Dev 4.17
Gaus mean : 29.8693
Gaus Width: 4.4700
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch104, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 76
Mean 35.97
Std Dev 4.239
Gaus mean : 36.8364
Gaus Width: 4.9744
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch104, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 42.04
Std Dev 3.9
Gaus mean : 41.3205
Gaus Width: 6.4956
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
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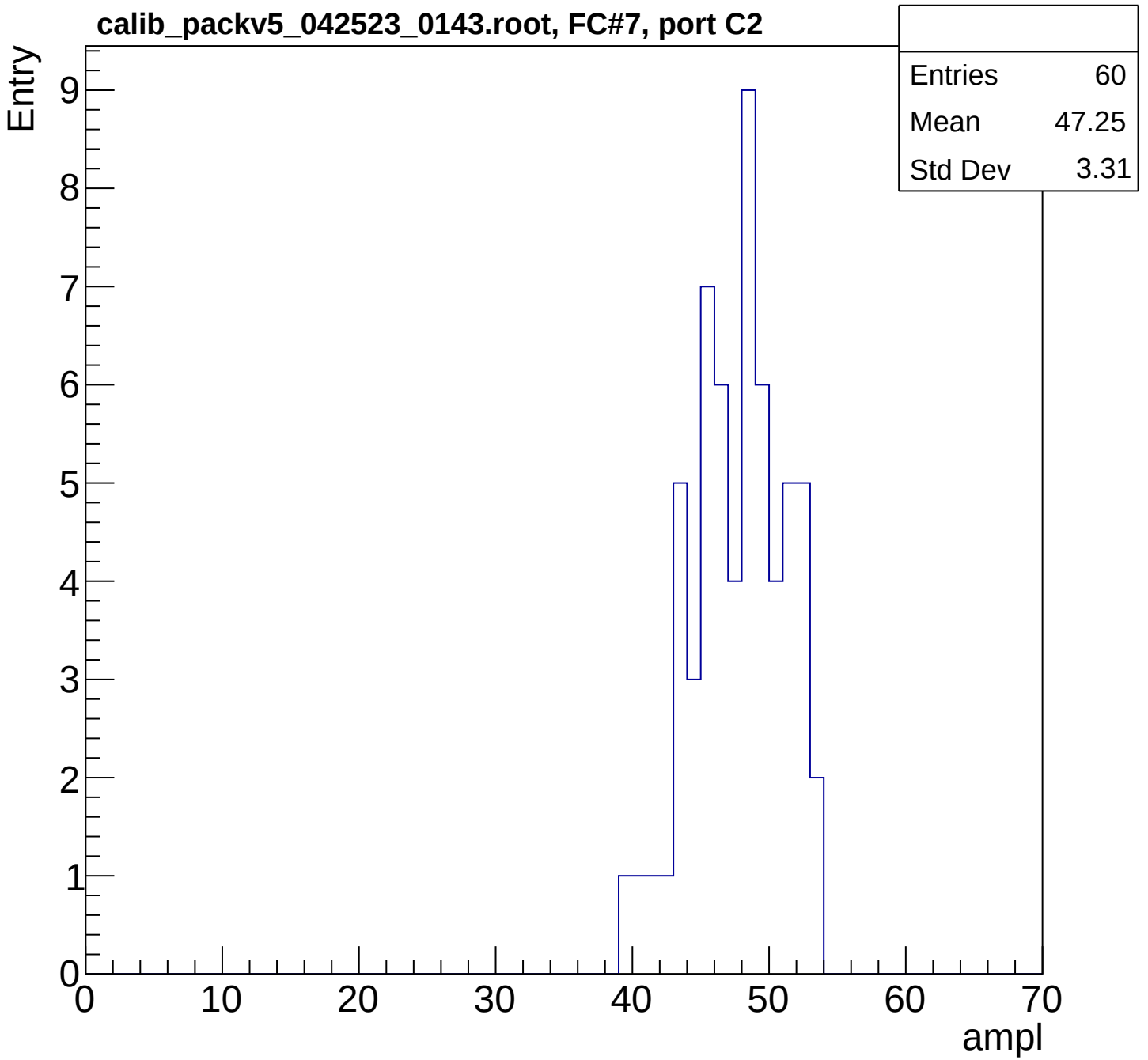
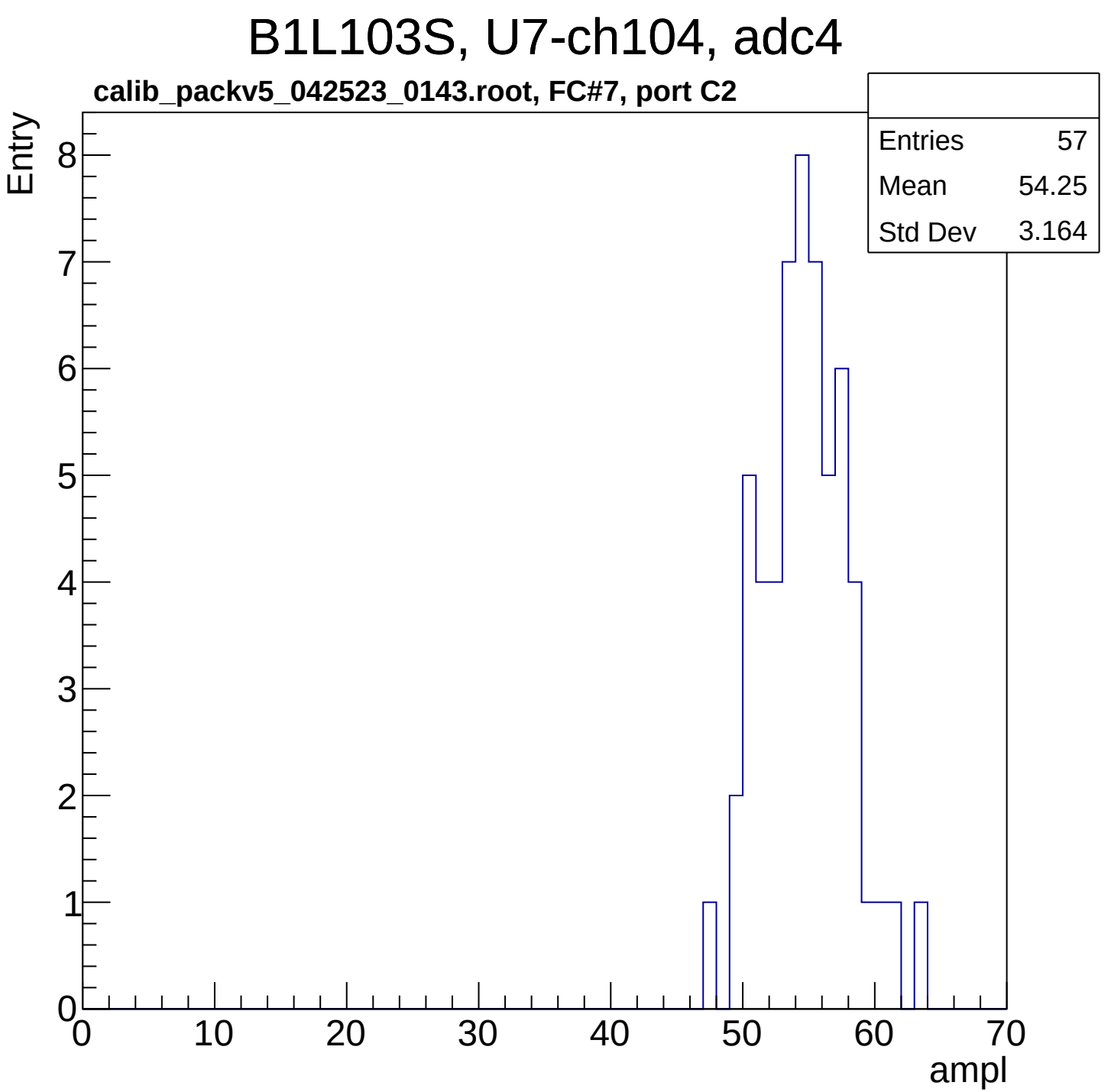

B1L103S, U7-ch104, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 60
Mean 47.25
Std Dev 3.31
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch104, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 54.25
Std Dev 3.164
Entry
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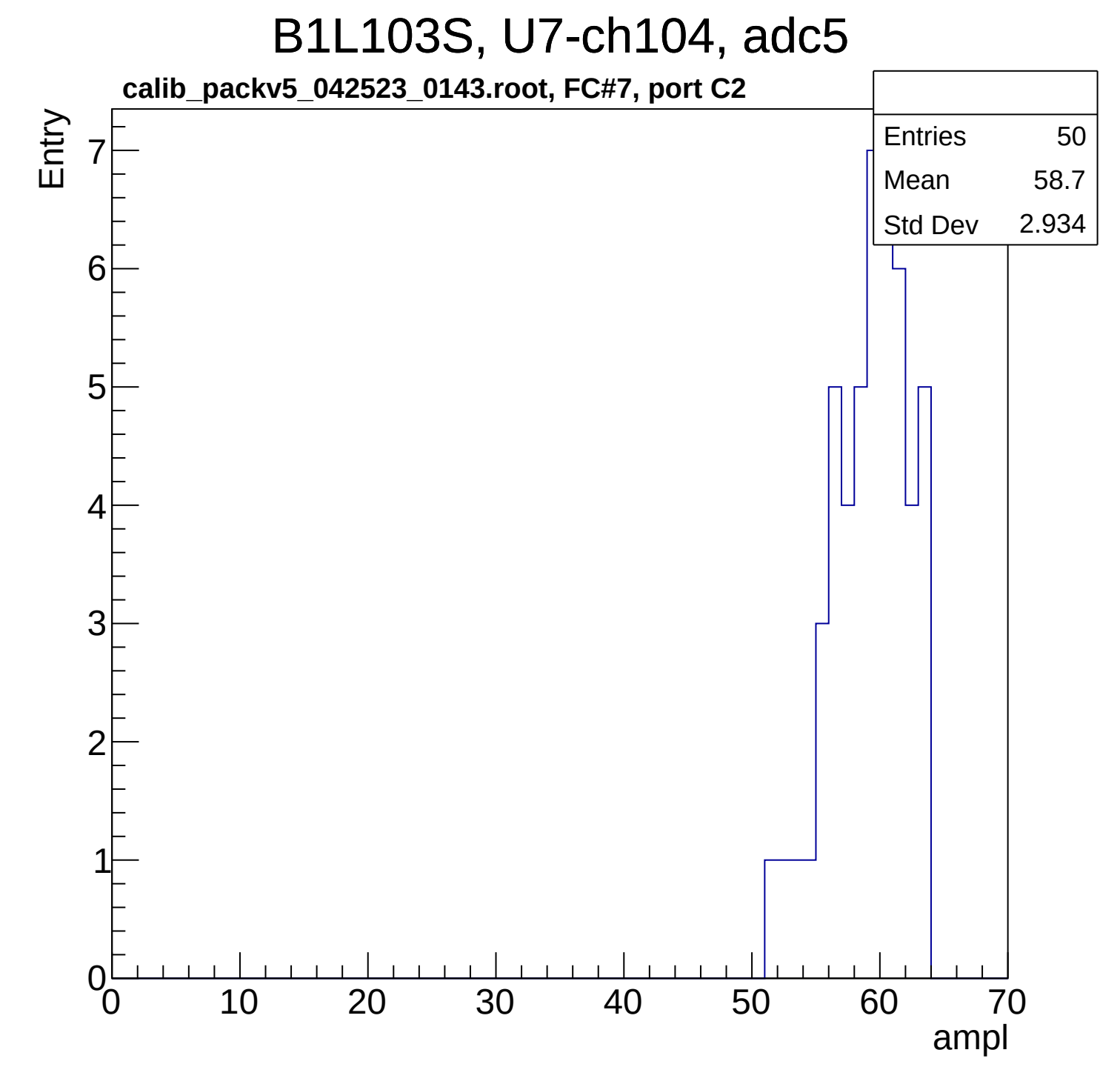
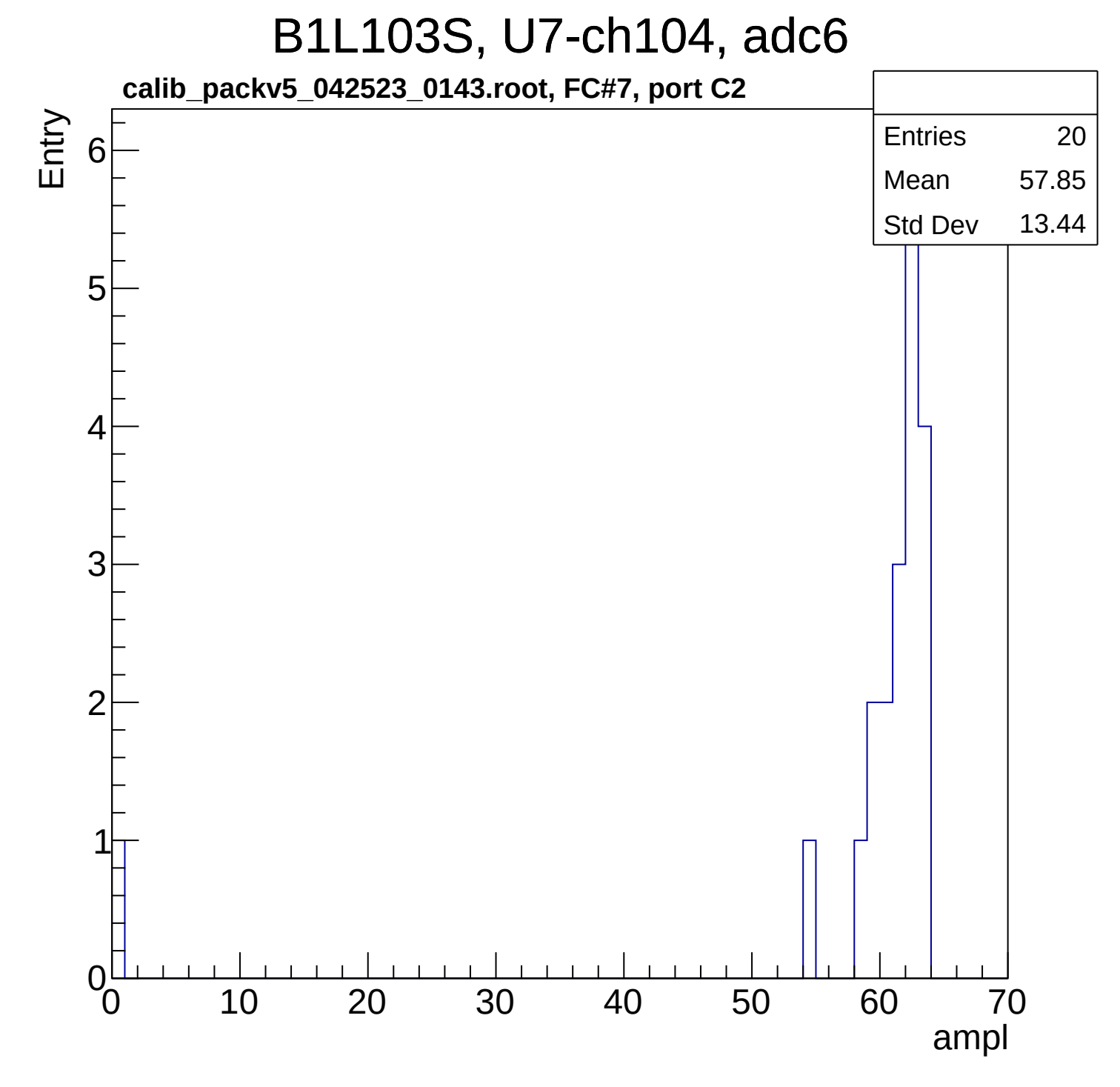
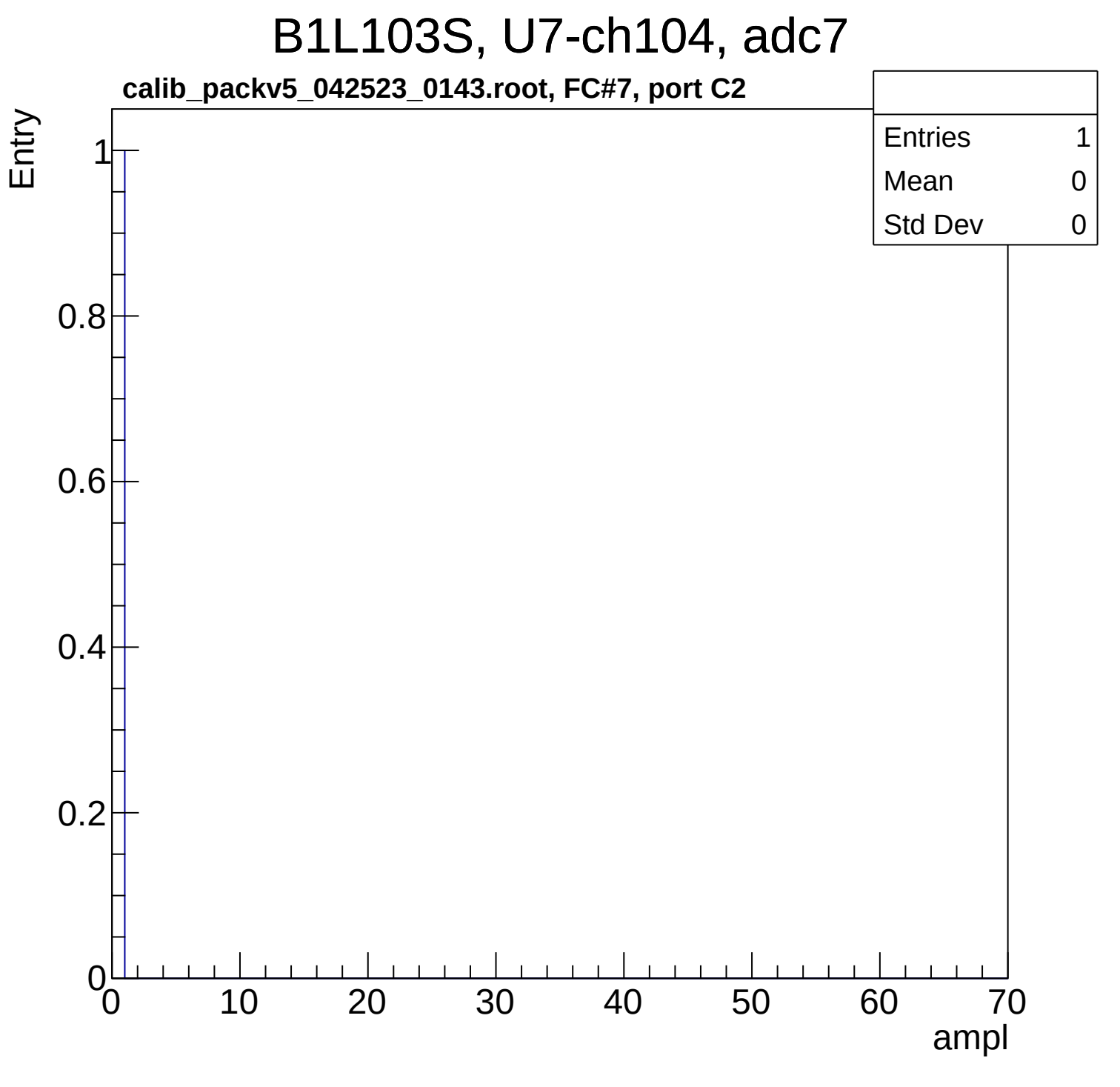
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch104, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 50
Mean 58.7
Std Dev 2.934
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch104, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 20
Mean 57.85
Std Dev 13.44
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch104, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
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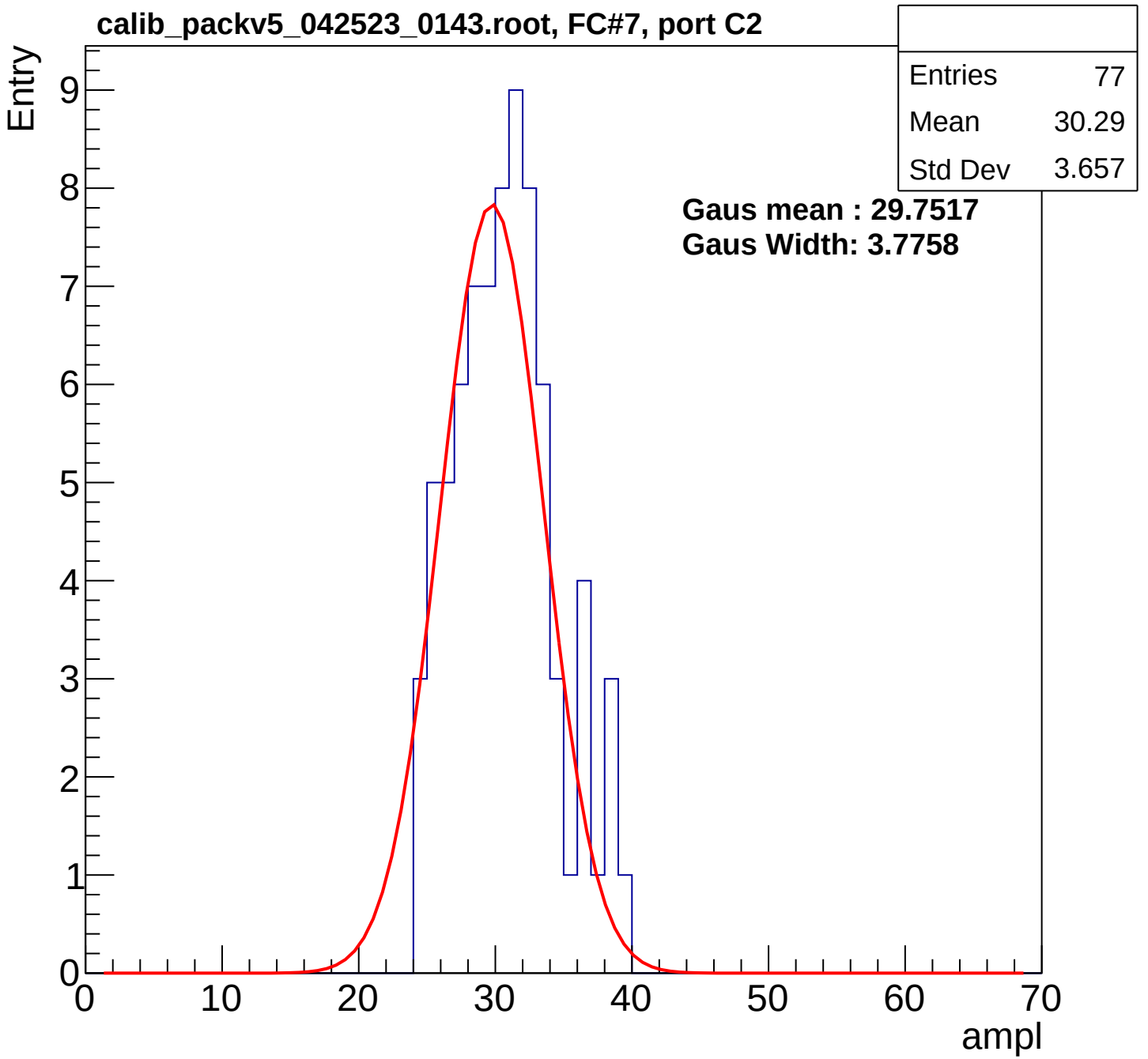
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch105, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 77
Mean 30.29
Std Dev 3.657
Gaus mean : 29.7517
Gaus Width: 3.7758
Entry
ampl
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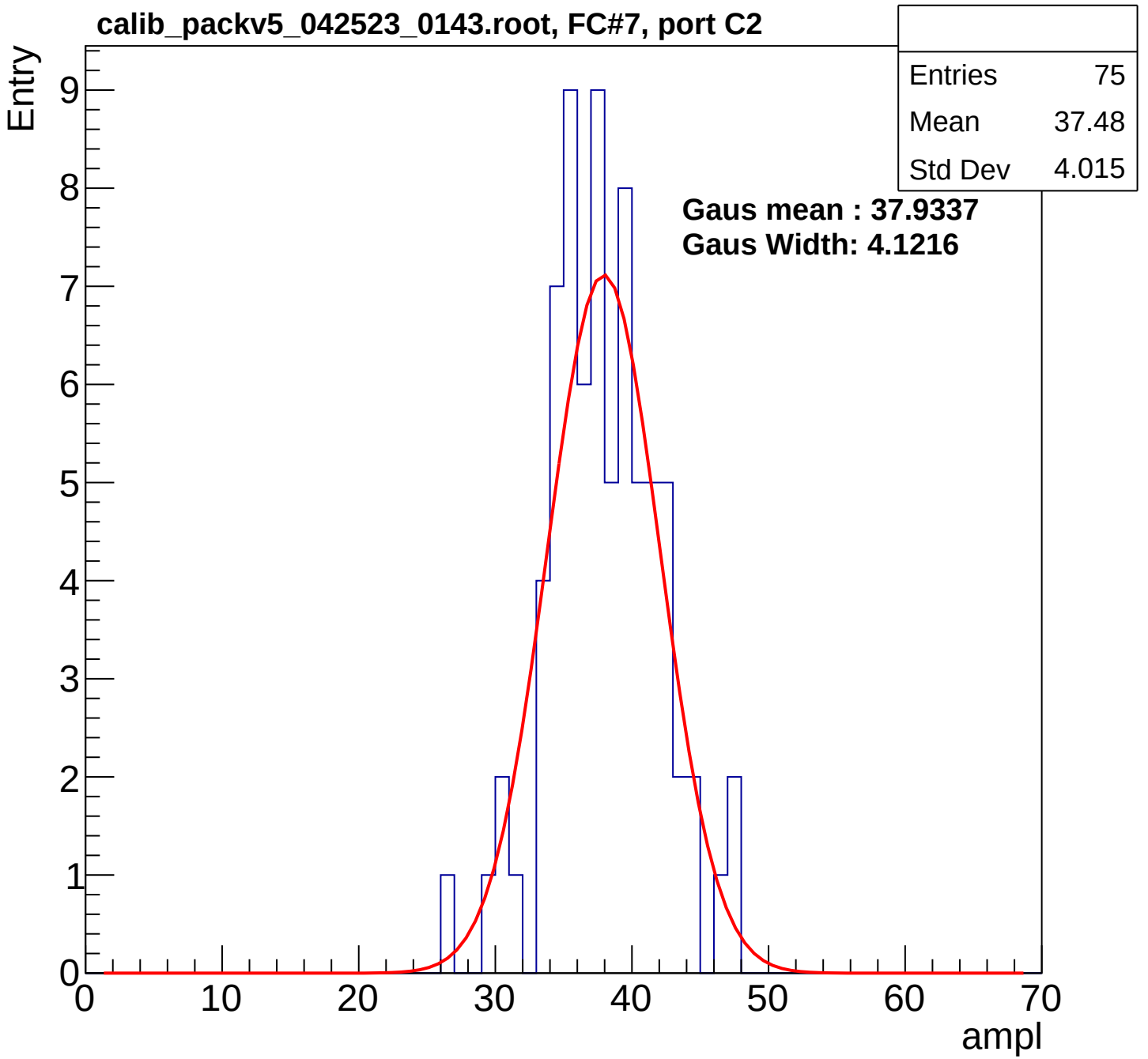
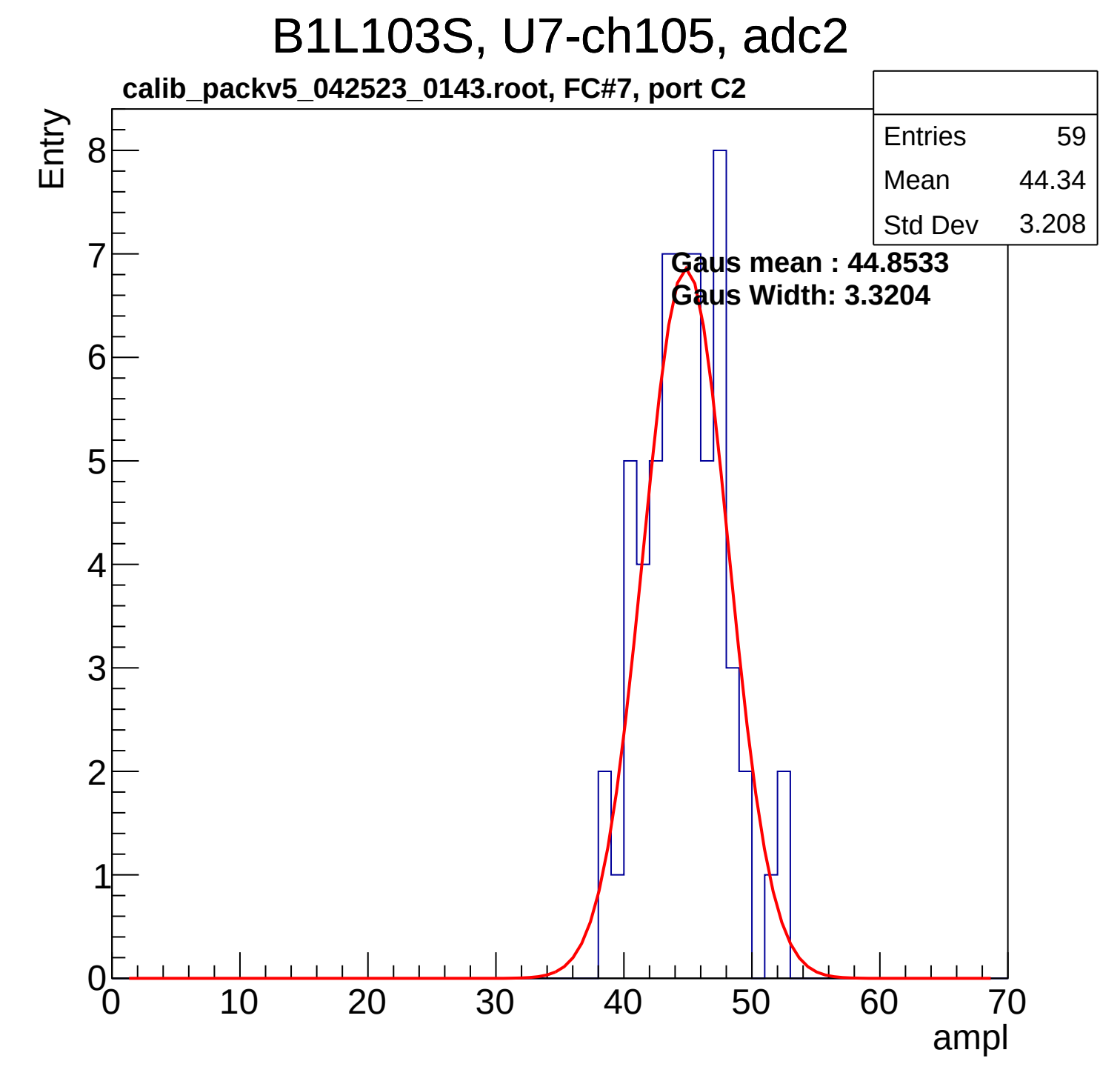
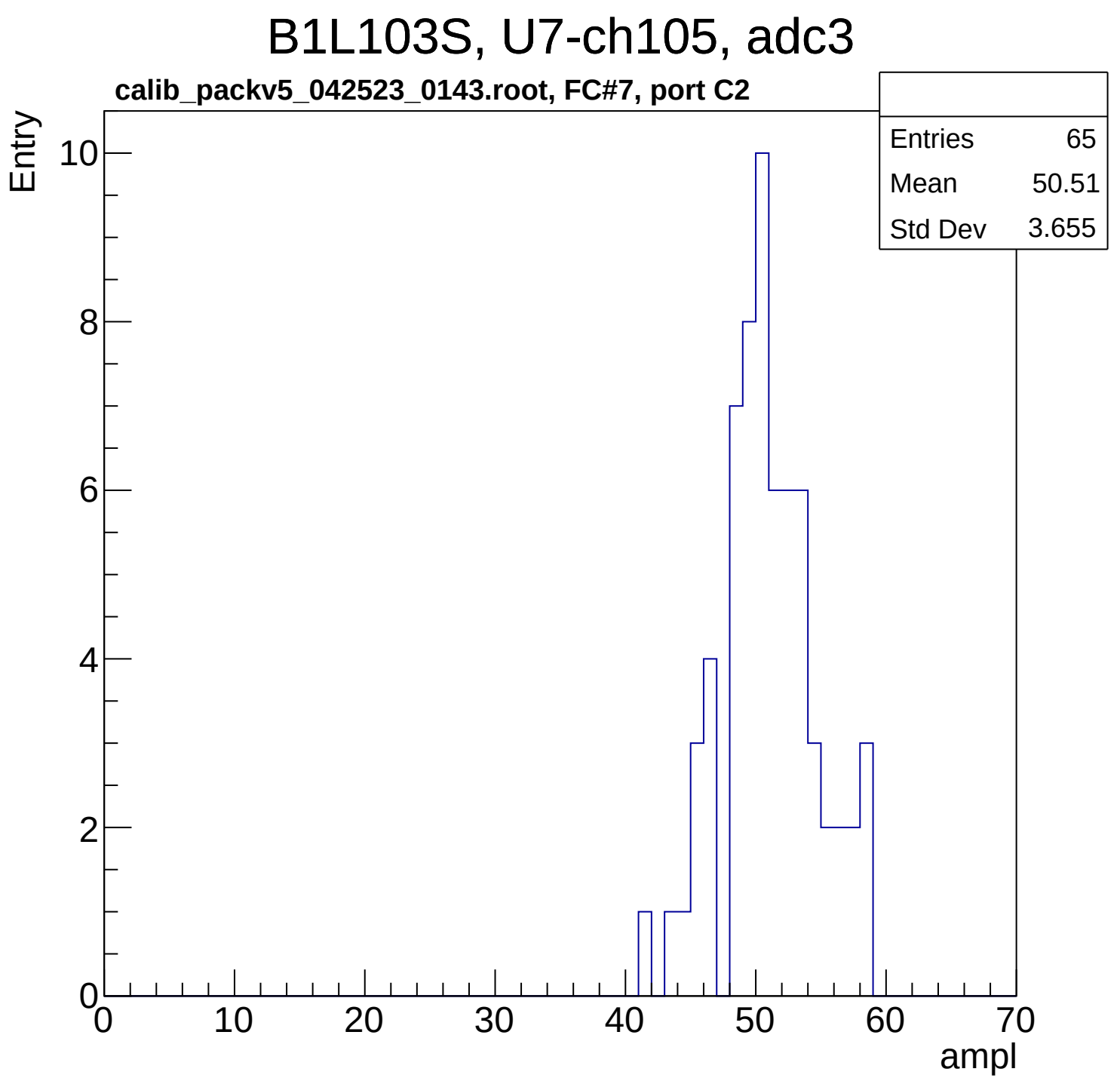
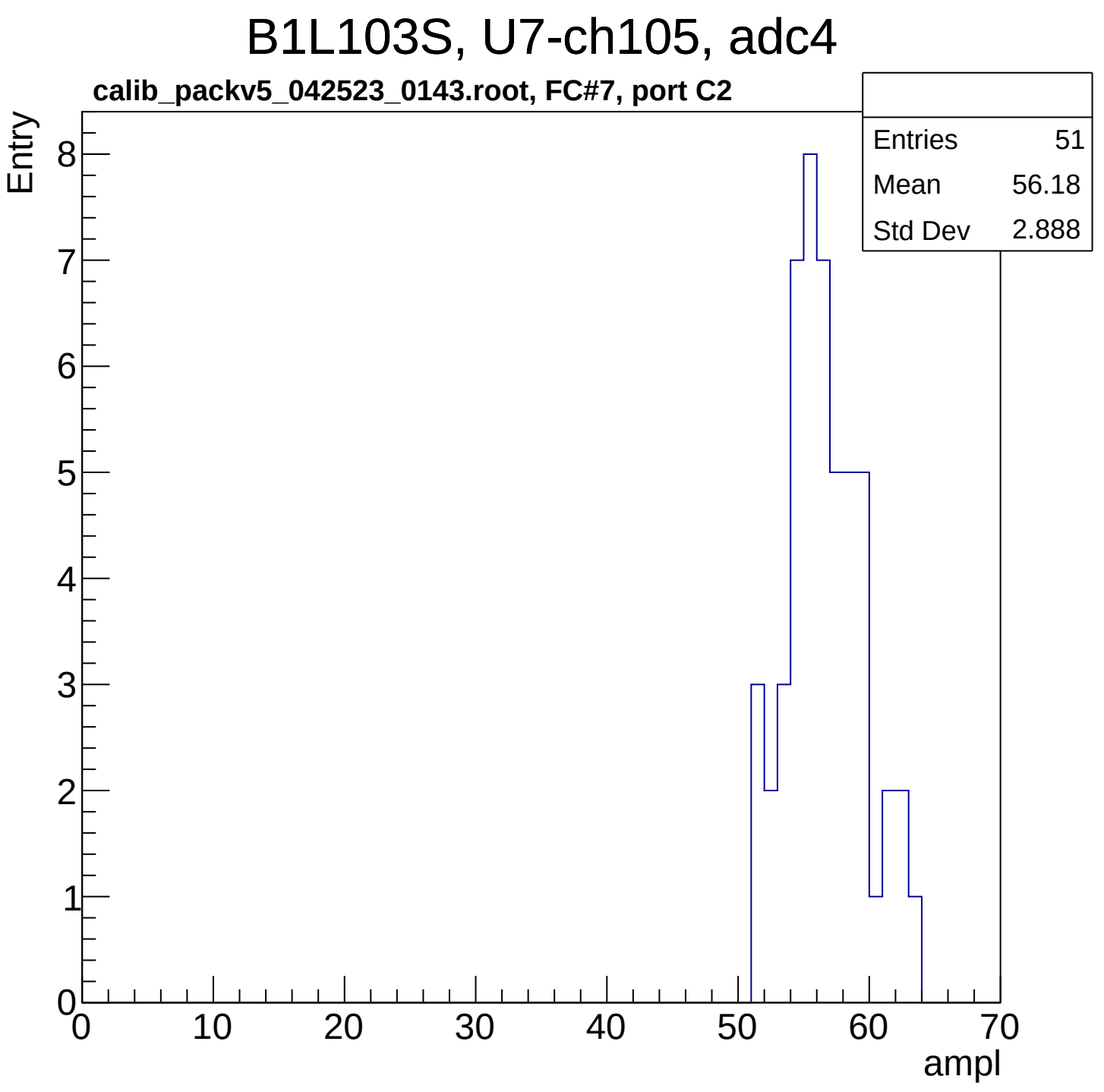
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch105, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 75
Mean 37.48
Std Dev 4.015
Gaus mean : 37.9337
Gaus Width: 4.1216
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch105, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 44.34
Std Dev 3.208
Gaus mean : 44.8533
Gaus Width: 3.3204
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch105, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 50.51
Std Dev 3.655
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch105, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 51
Mean 56.18
Std Dev 2.888
Entry
ampl
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2
3
4
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7
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0
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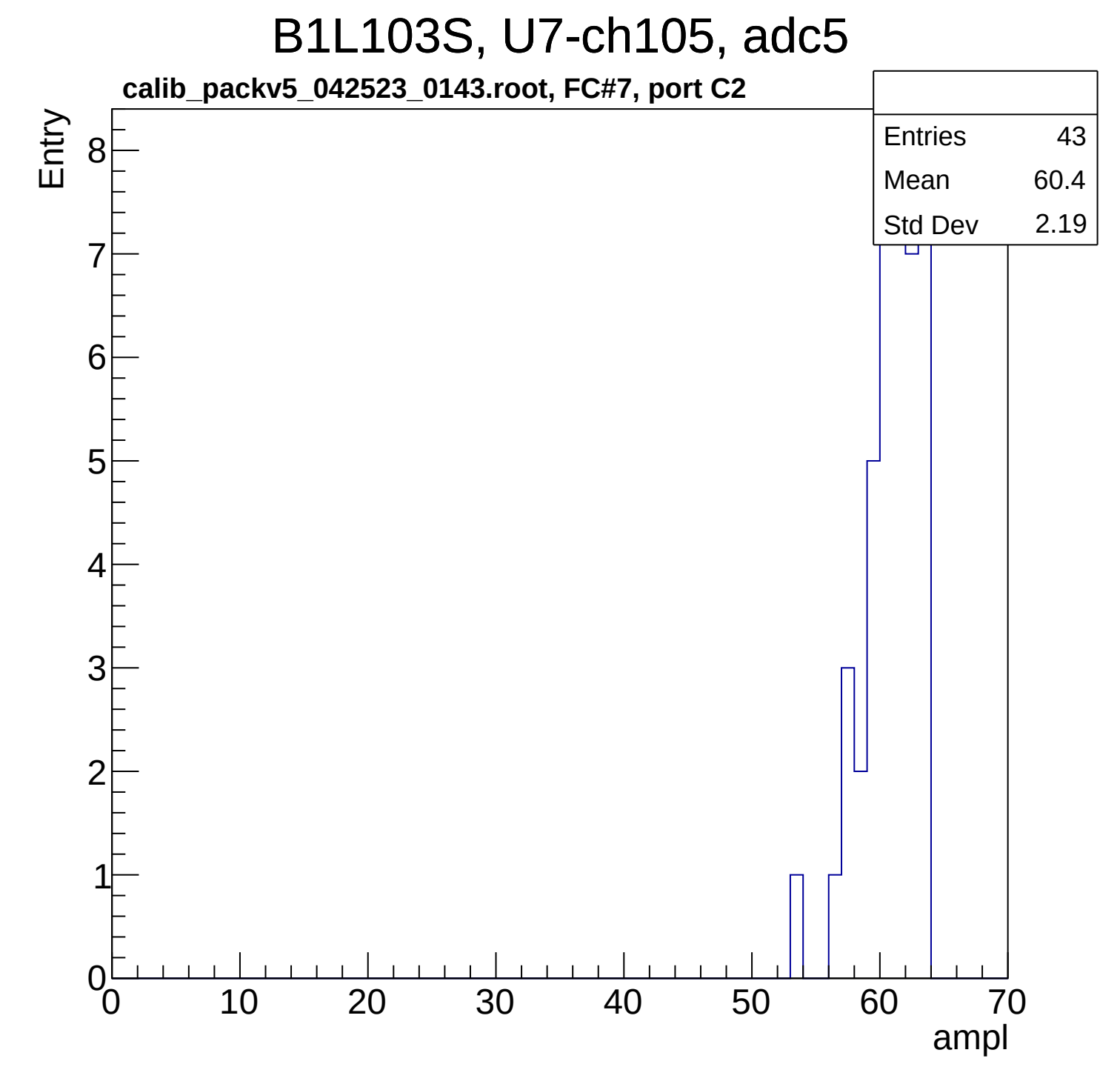
B1L103S, U7-ch105, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 43
Mean 60.4
Std Dev 2.19
Entry
ampl
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1
2
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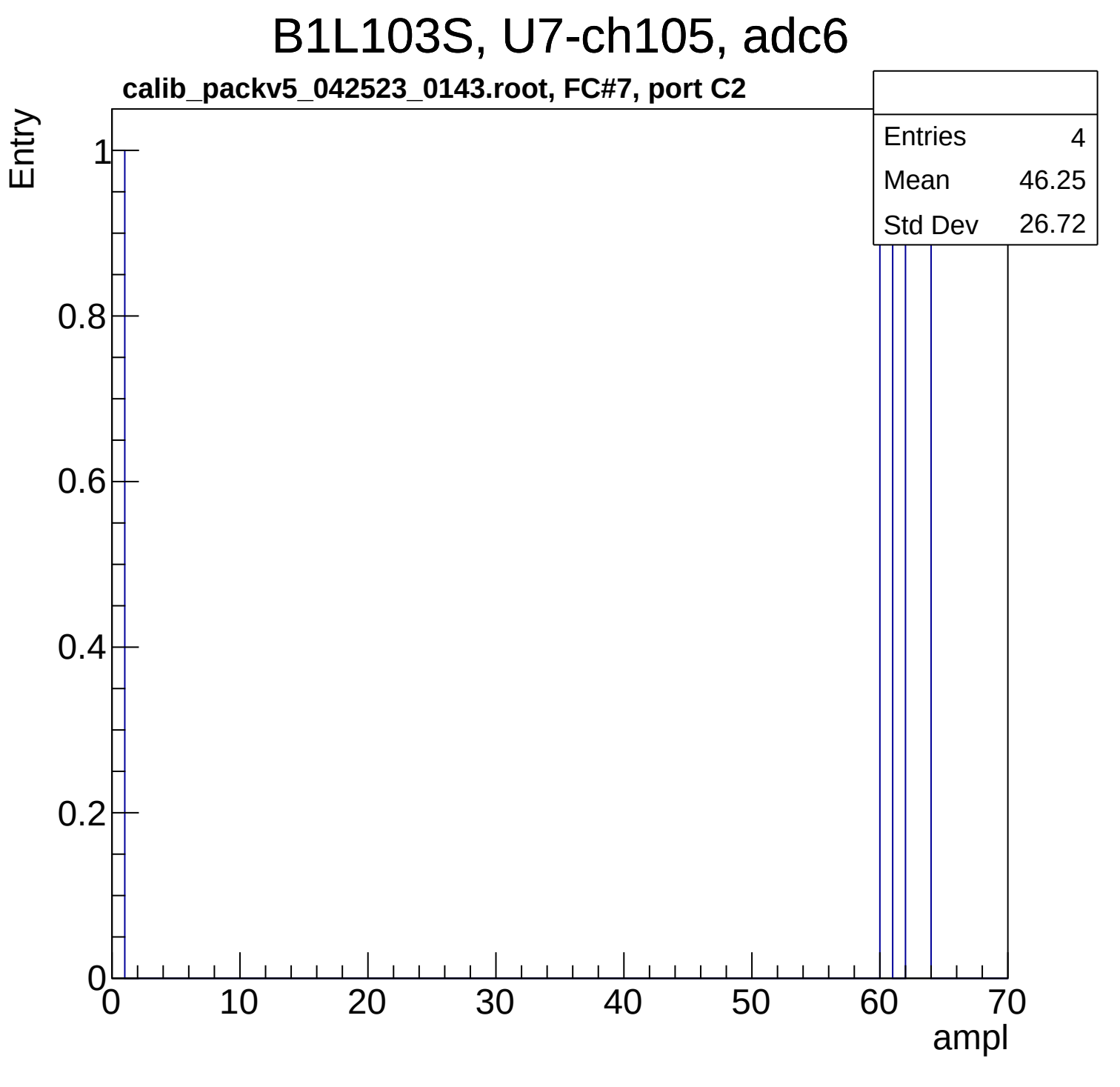
B1L103S, U7-ch105, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 4
Mean 46.25
Std Dev 26.72
Entry
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0.6
0.4
0.2
0
0
10
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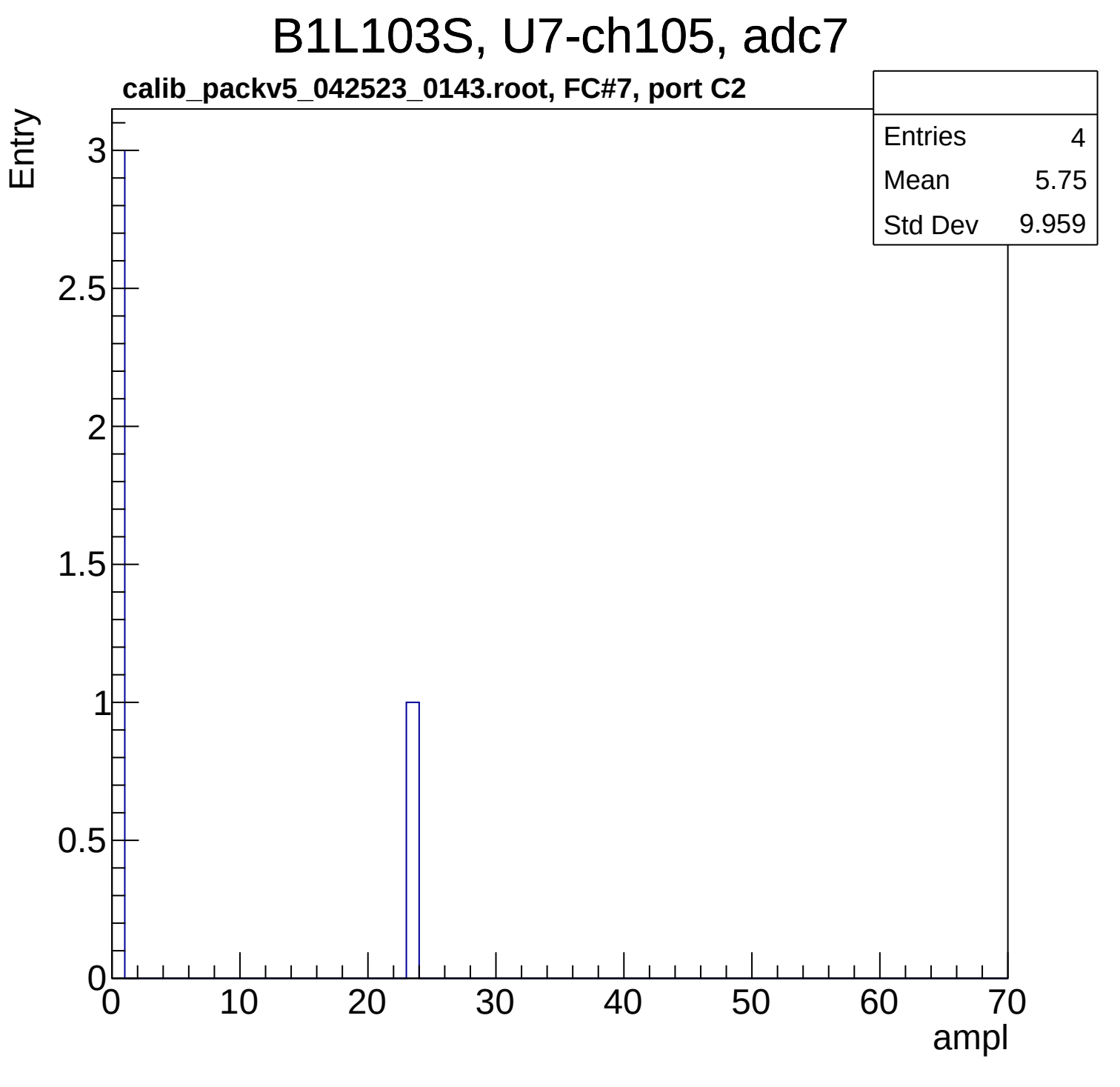
30
40
50
60
70
ampl


B1L103S, U7-ch105, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 4
Mean 5.75
Std Dev 9.959
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
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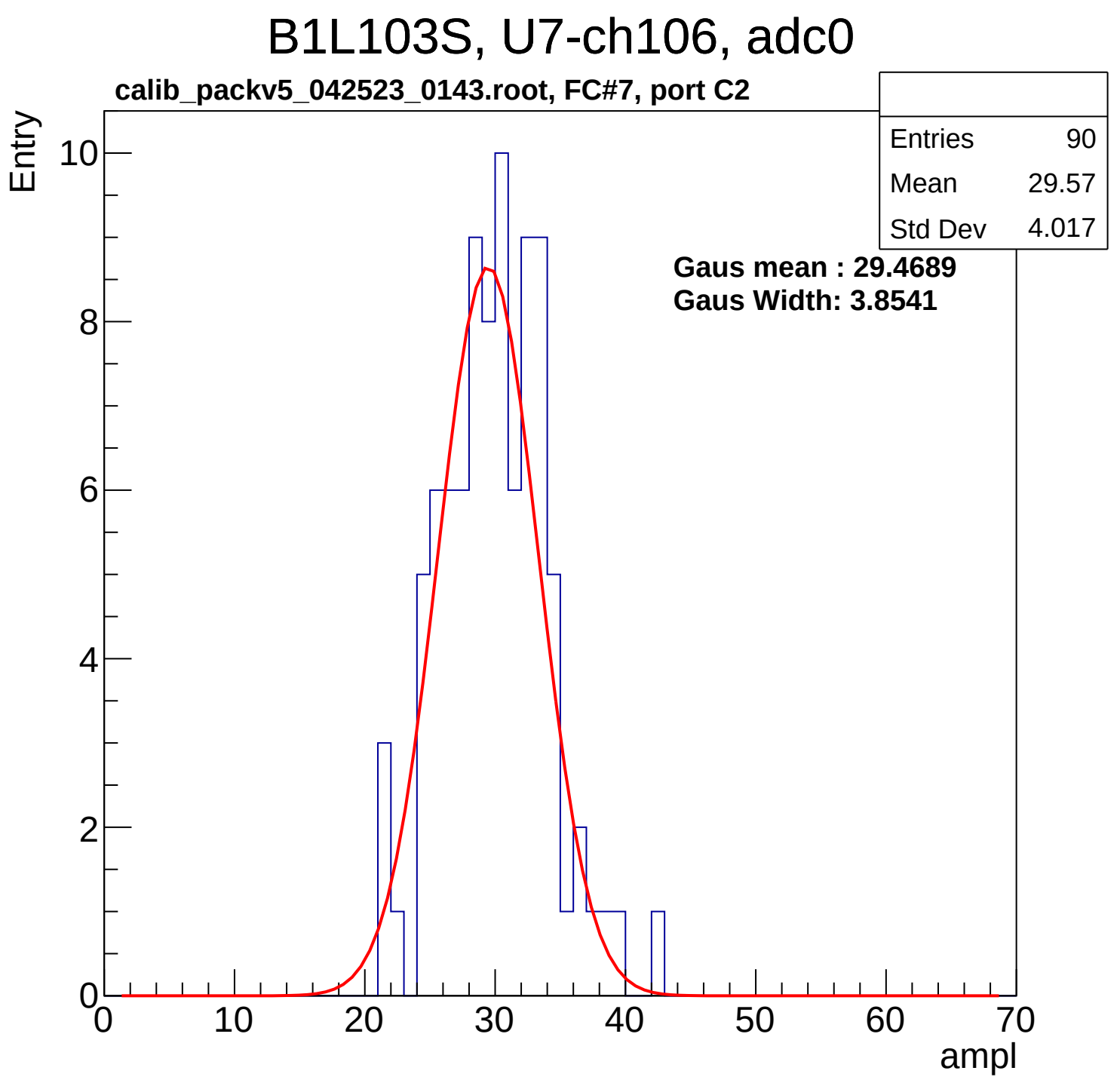
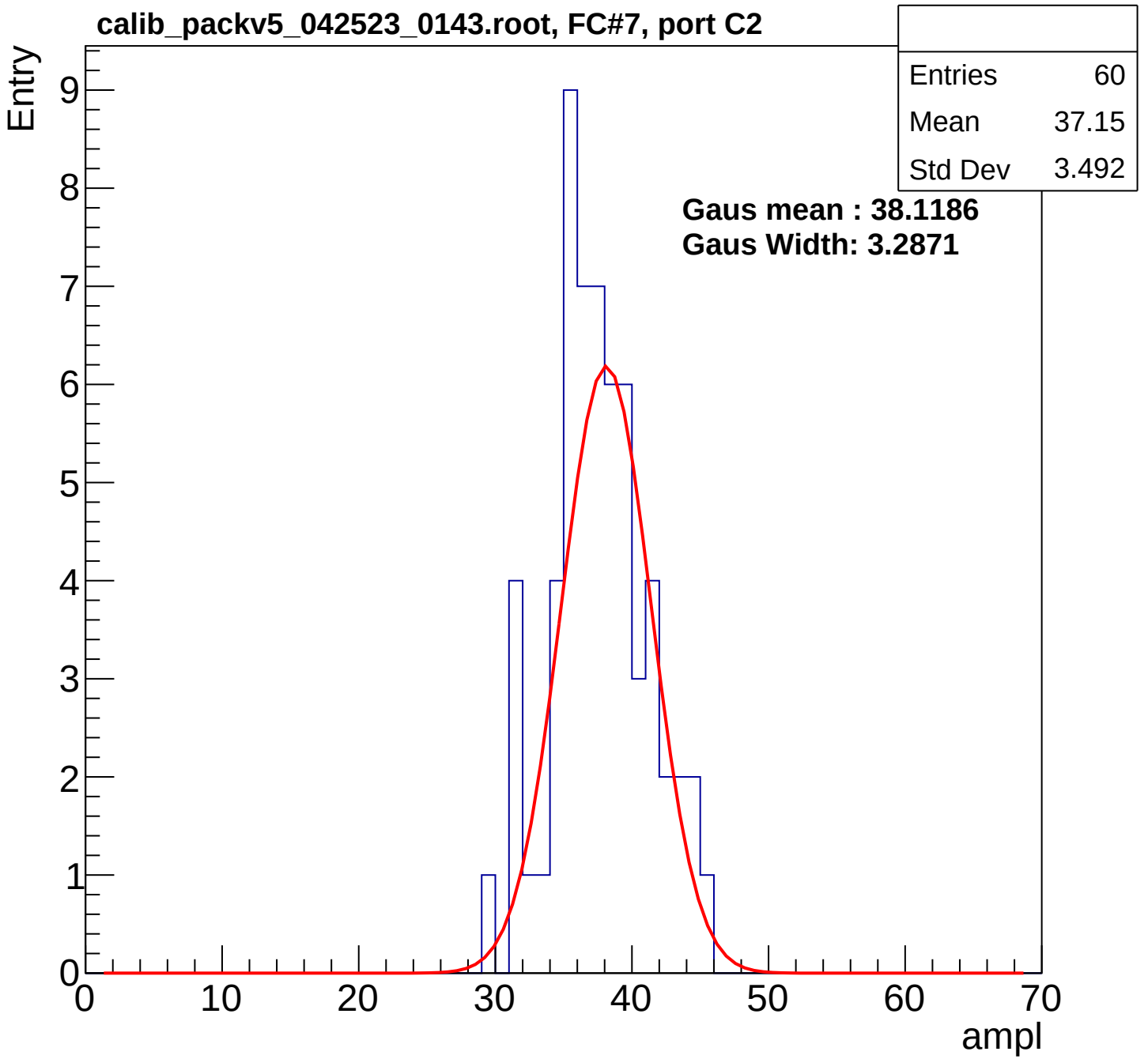

B1L103S, U7-ch106, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 90
Mean 29.57
Std Dev 4.017
Gaus mean : 29.4689
Gaus Width: 3.8541
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch106, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 60
Mean 37.15
Std Dev 3.492
Gaus mean : 38.1186
Gaus Width: 3.2871
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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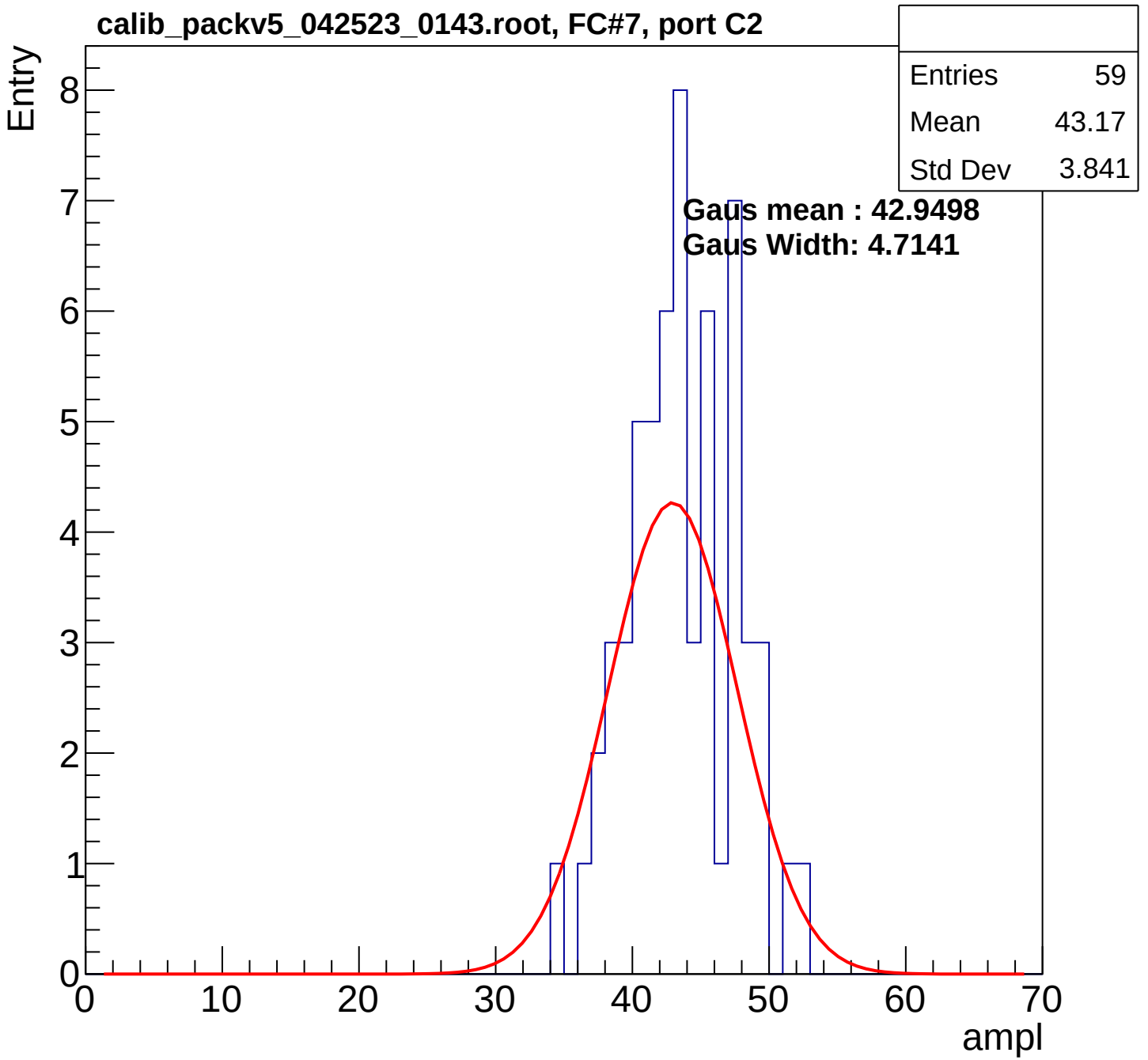
B1L103S, U7-ch106, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 43.17
Std Dev 3.841
Gaus mean : 42.9498
Gaus Width: 4.7141
Entry
ampl
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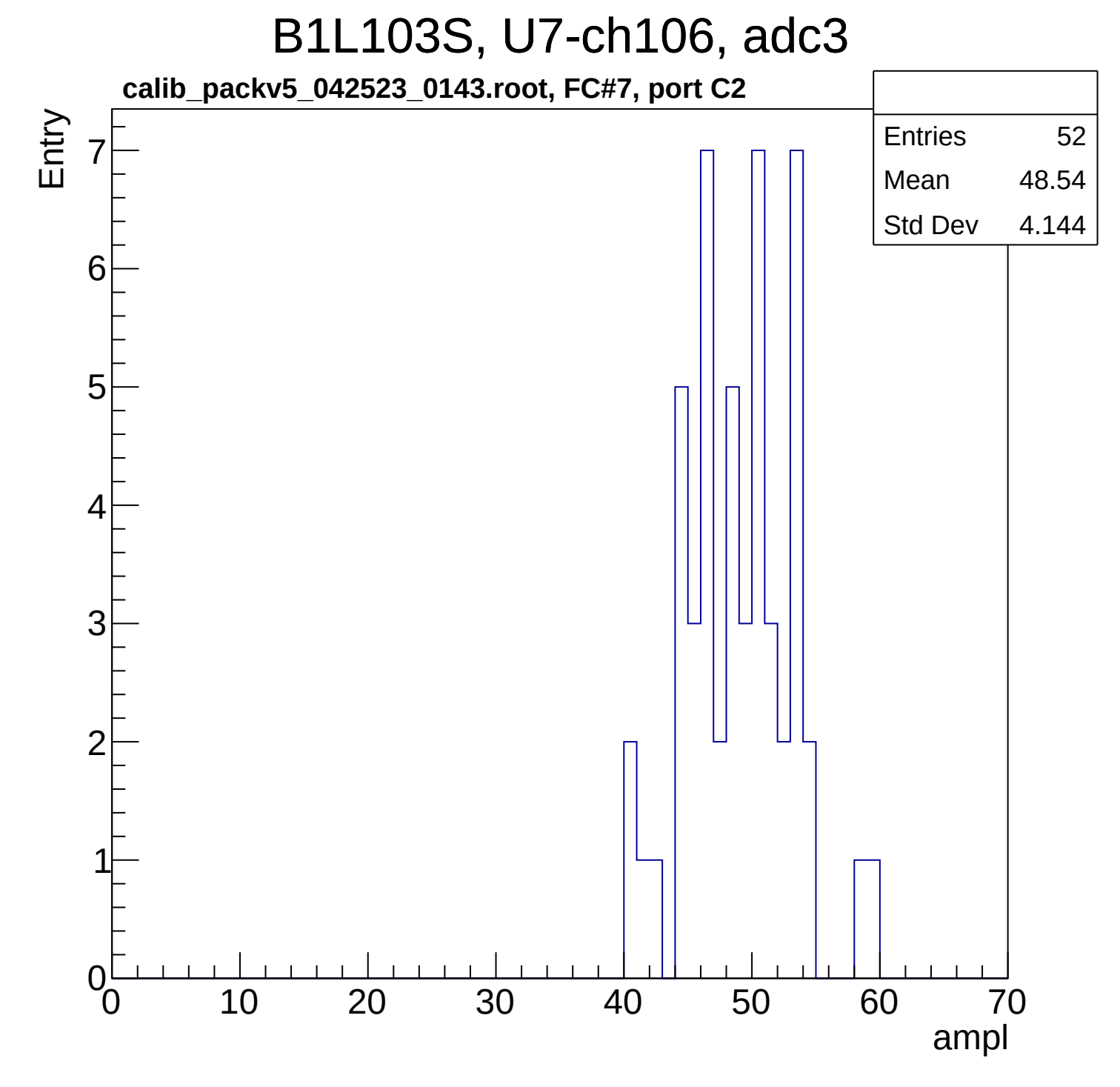
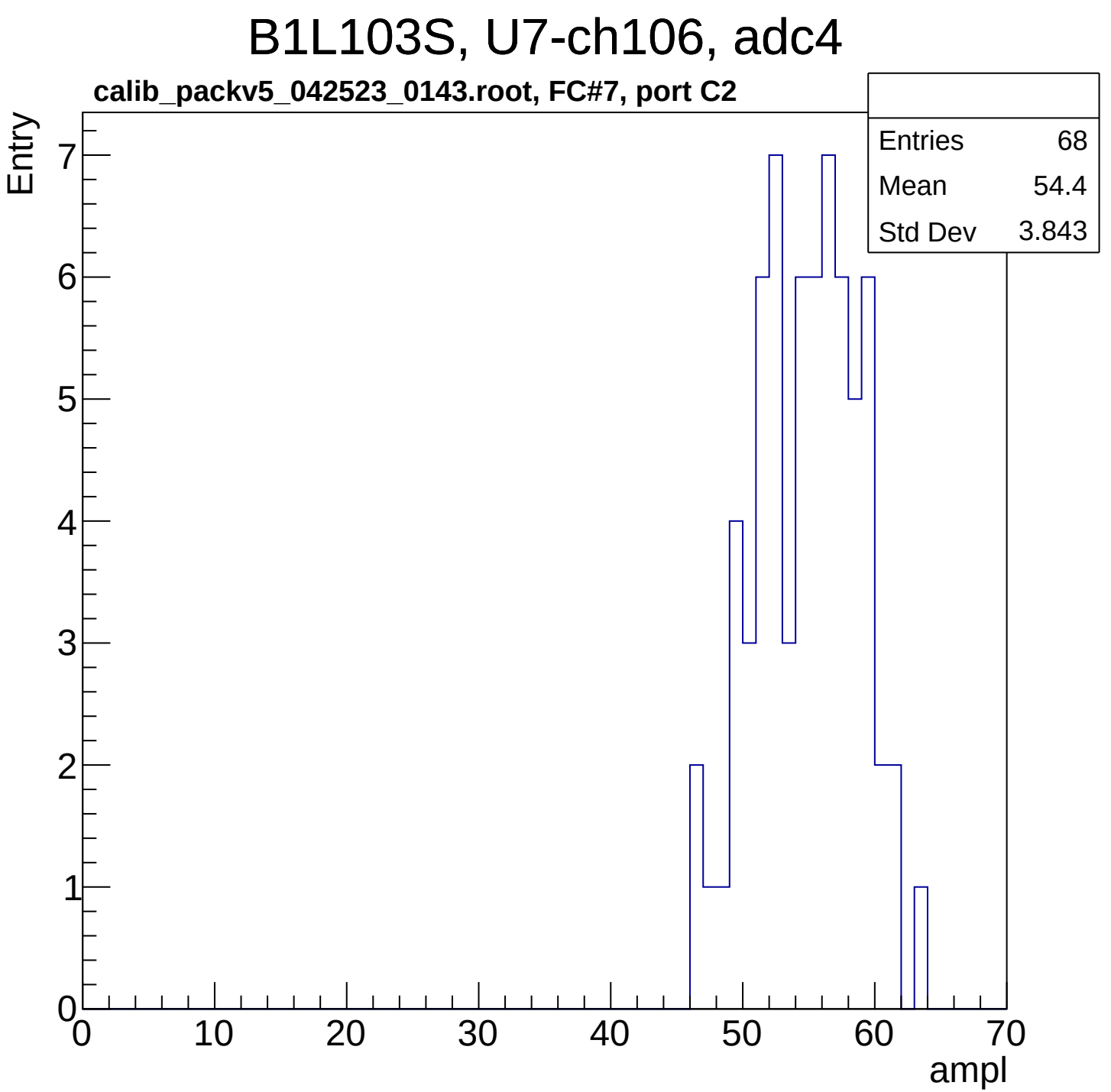
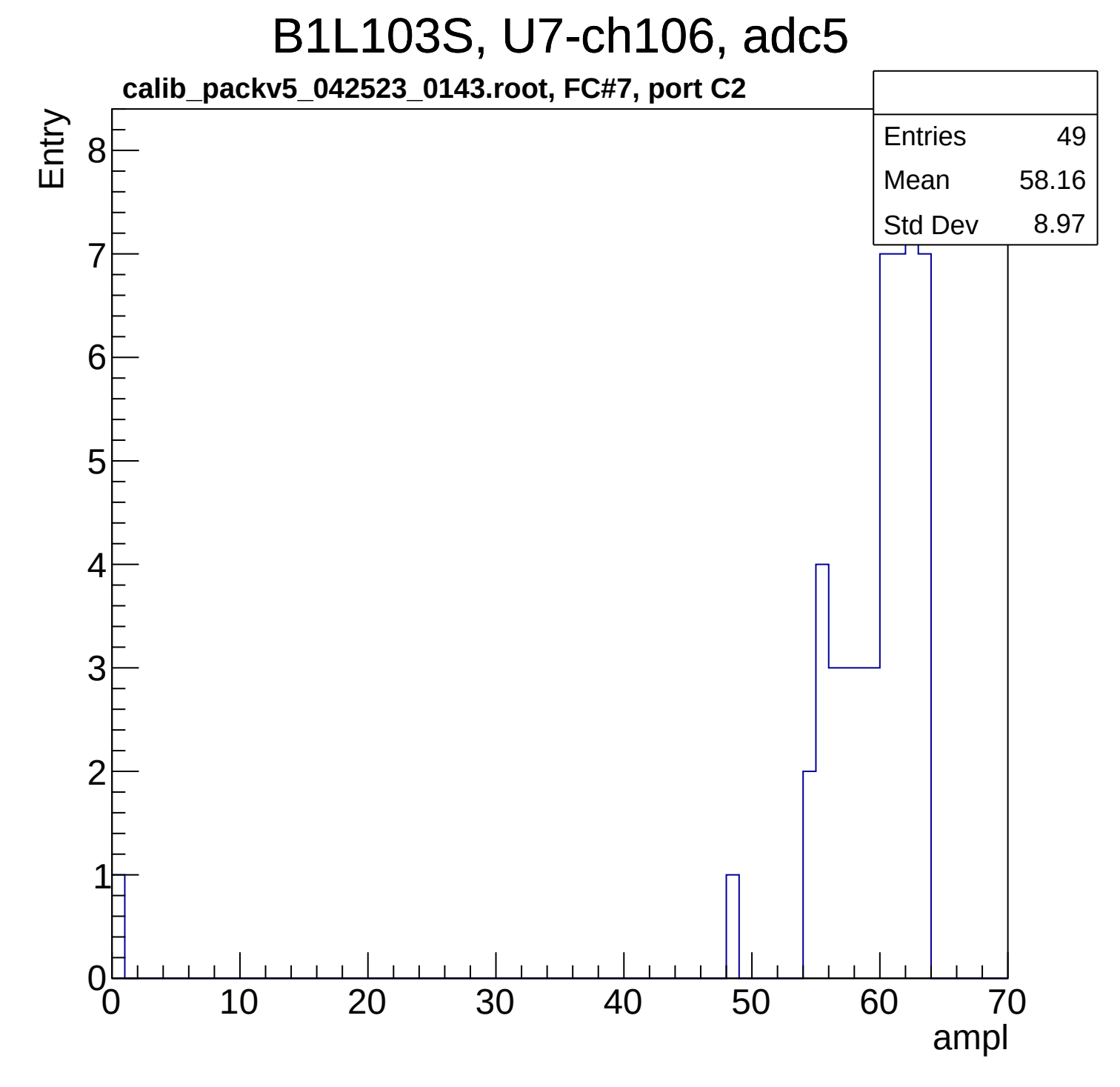
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch106, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 52
Mean 48.54
Std Dev 4.144
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch106, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 54.4
Std Dev 3.843
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch106, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 49
Mean 58.16
Std Dev 8.97
Entry
ampl
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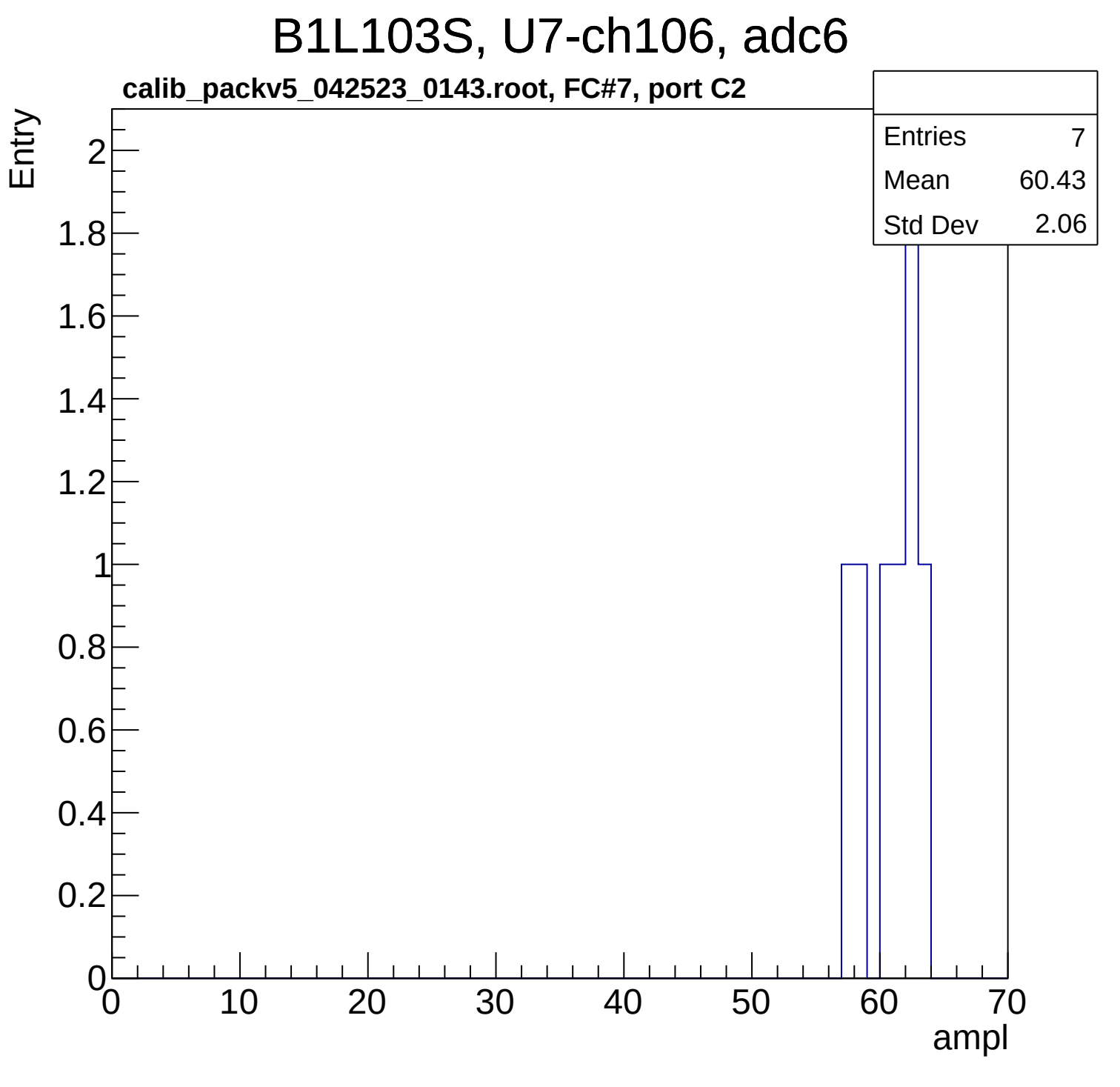
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch106, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 7
Mean 60.43
Std Dev 2.06
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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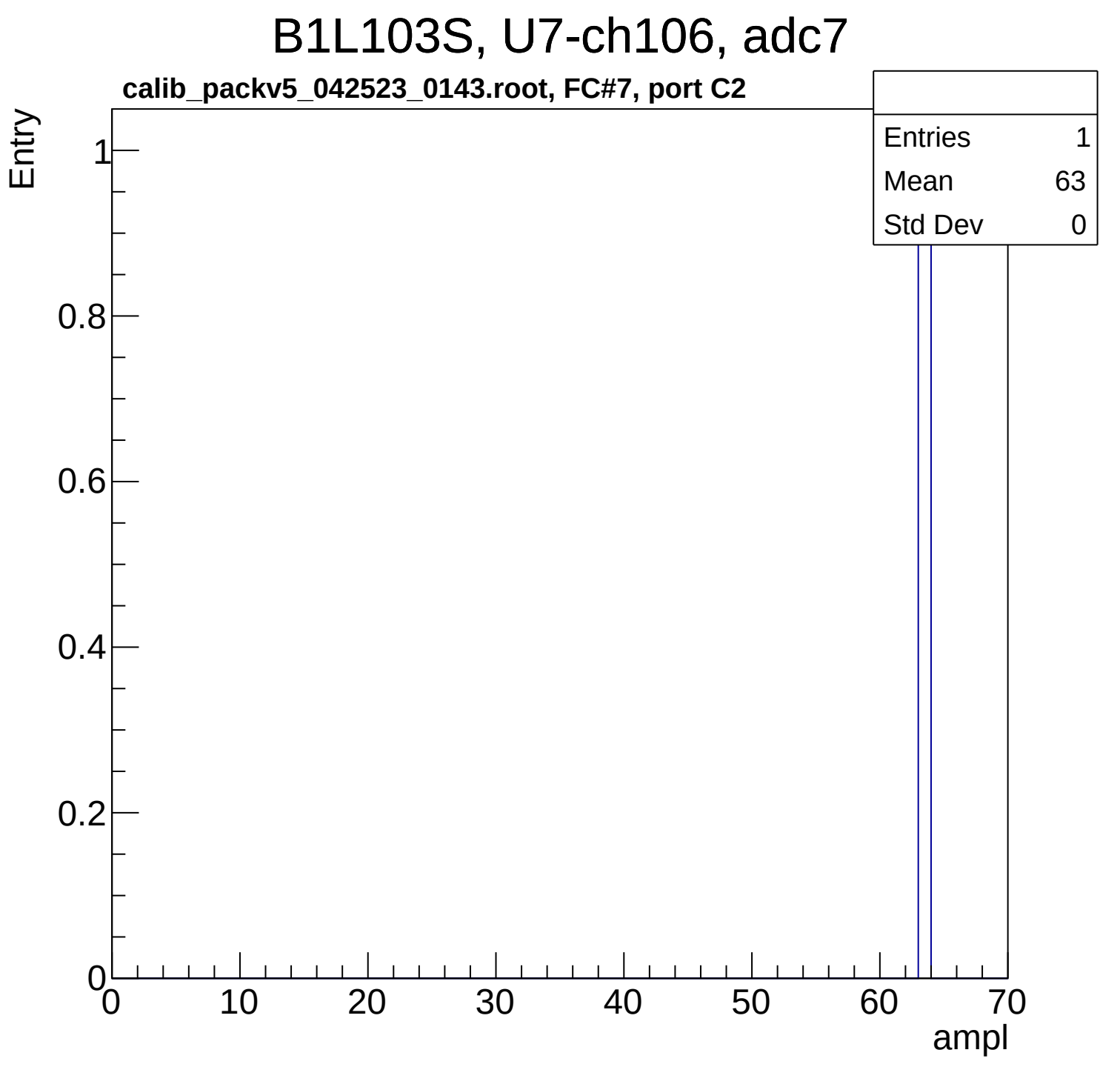
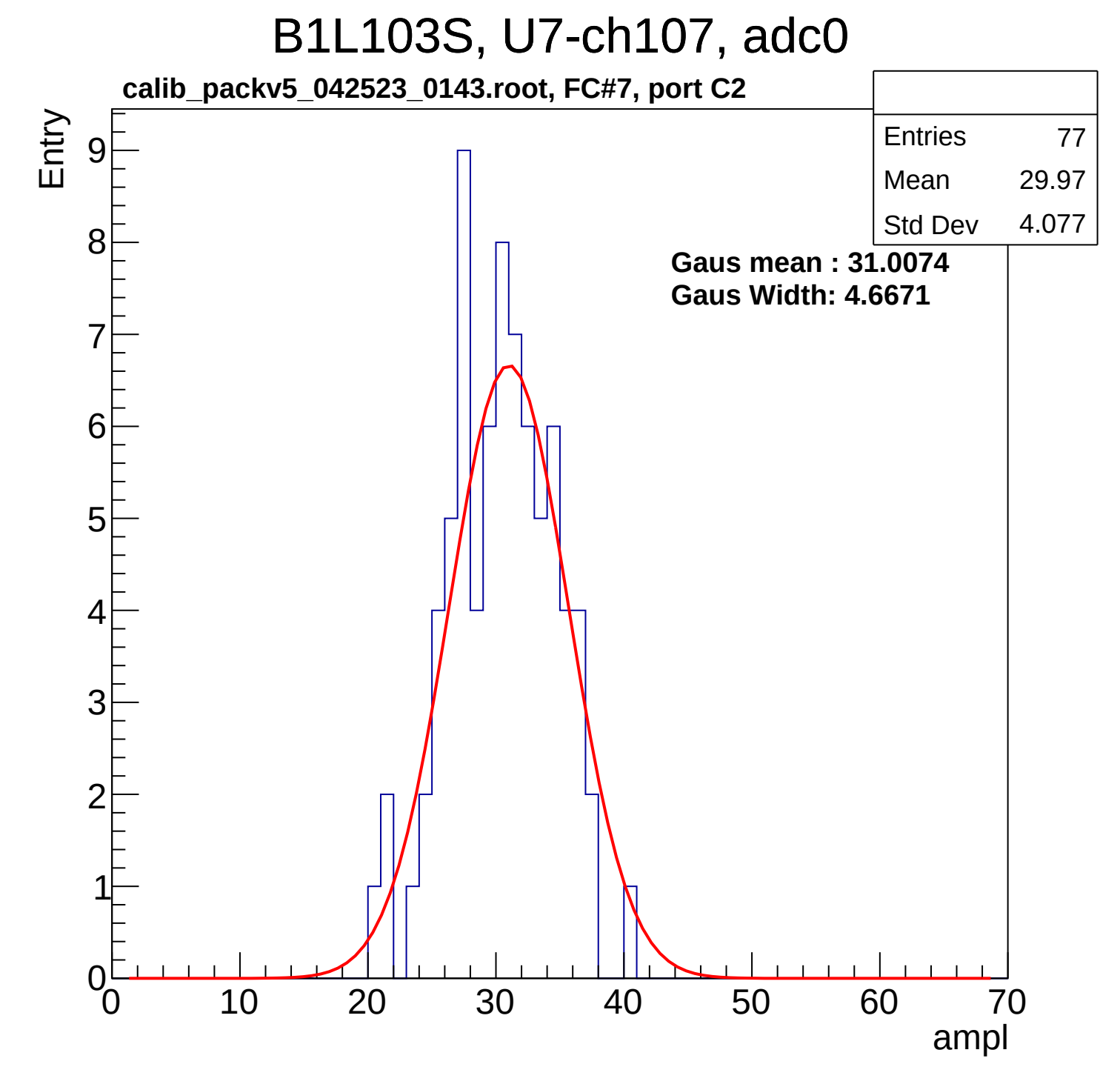
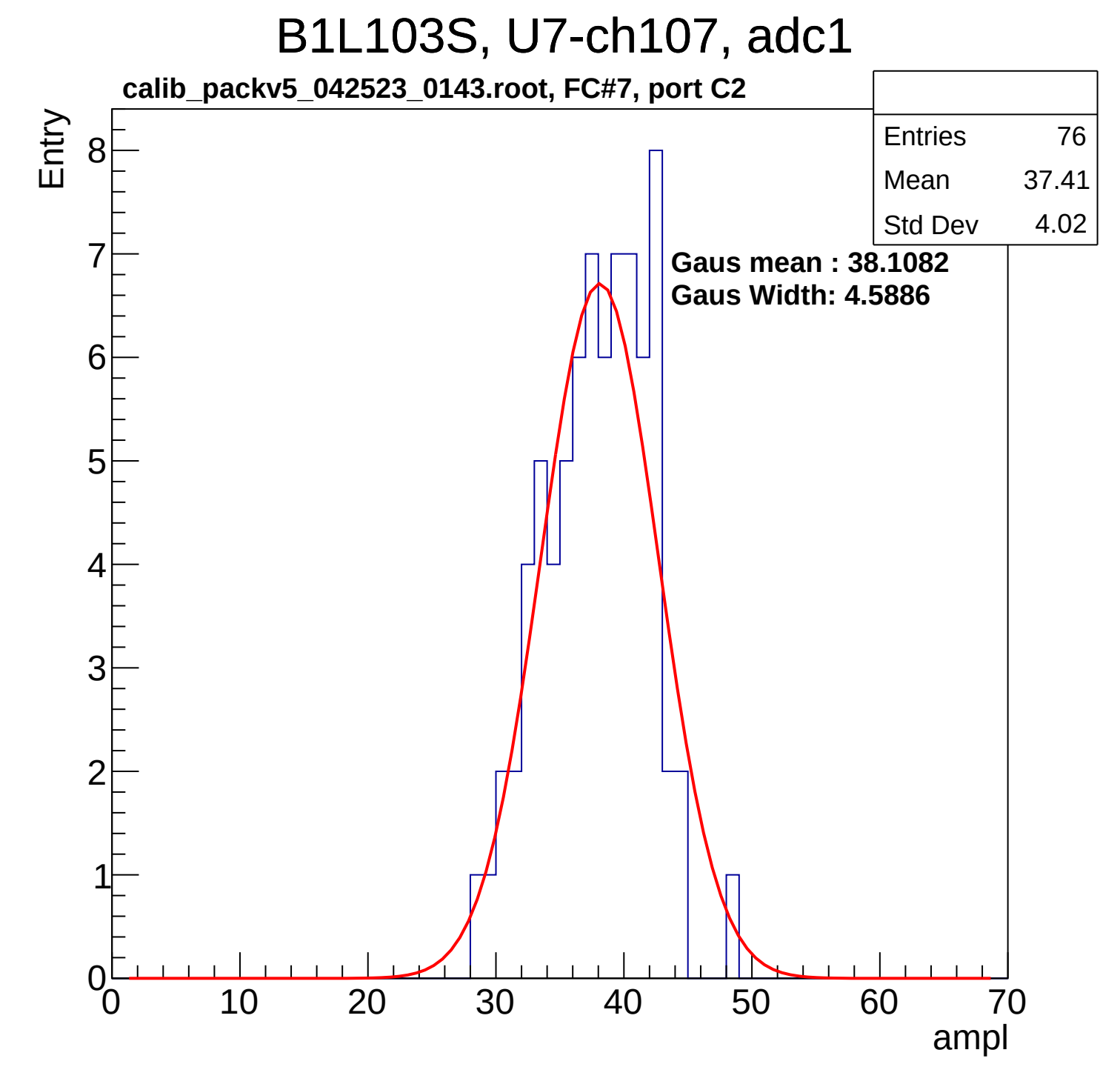

B1L103S, U7-ch106, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch107, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 77
Mean 29.97
Std Dev 4.077
Gaus mean : 31.0074
Gaus Width: 4.6671
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch107, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 76
Mean 37.41
Std Dev 4.02
Gaus mean : 38.1082
Gaus Width: 4.5886
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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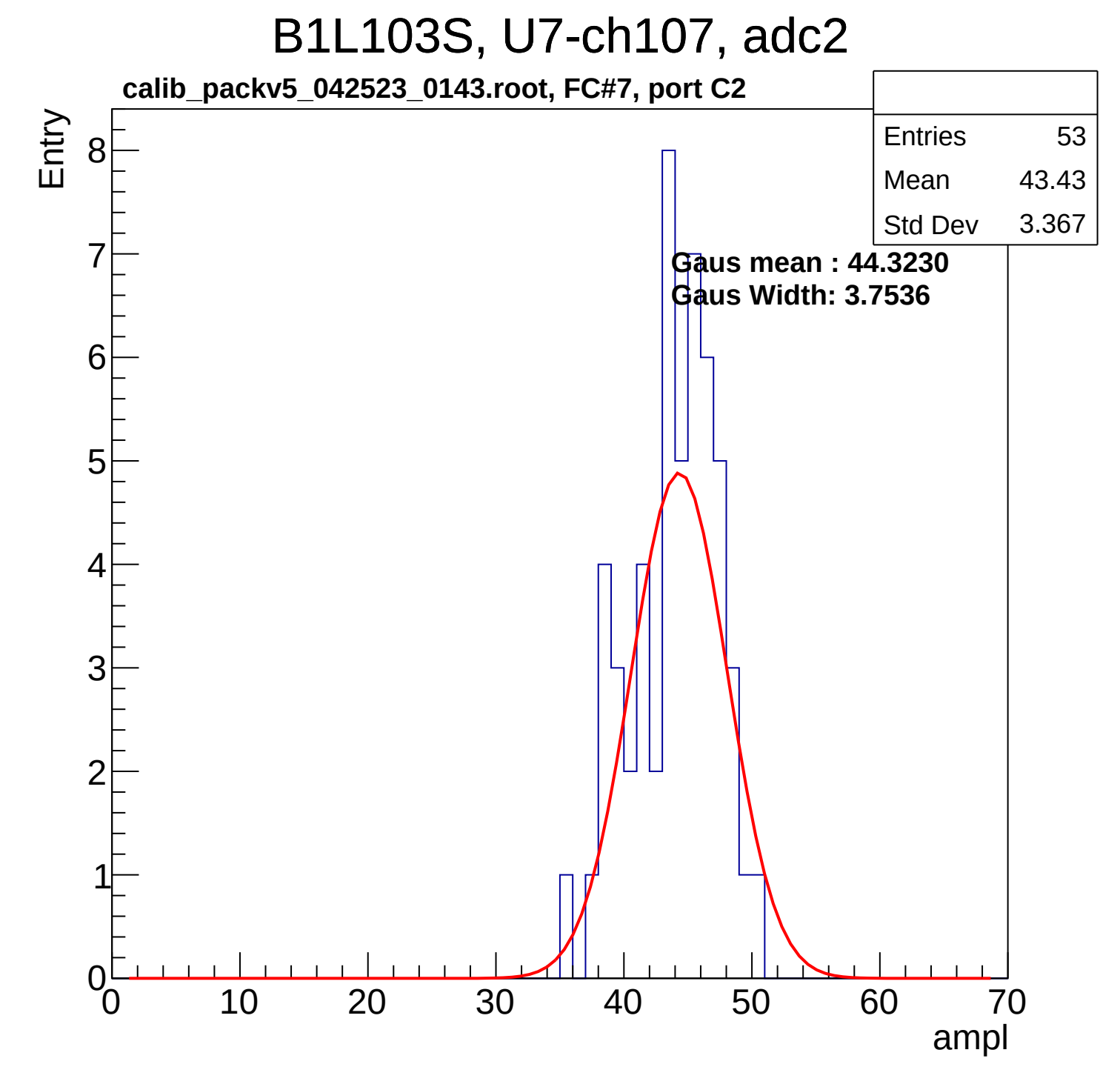
B1L103S, U7-ch107, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 43.43
Std Dev 3.367
Gaus mean : 44.3230
Gaus Width: 3.7536
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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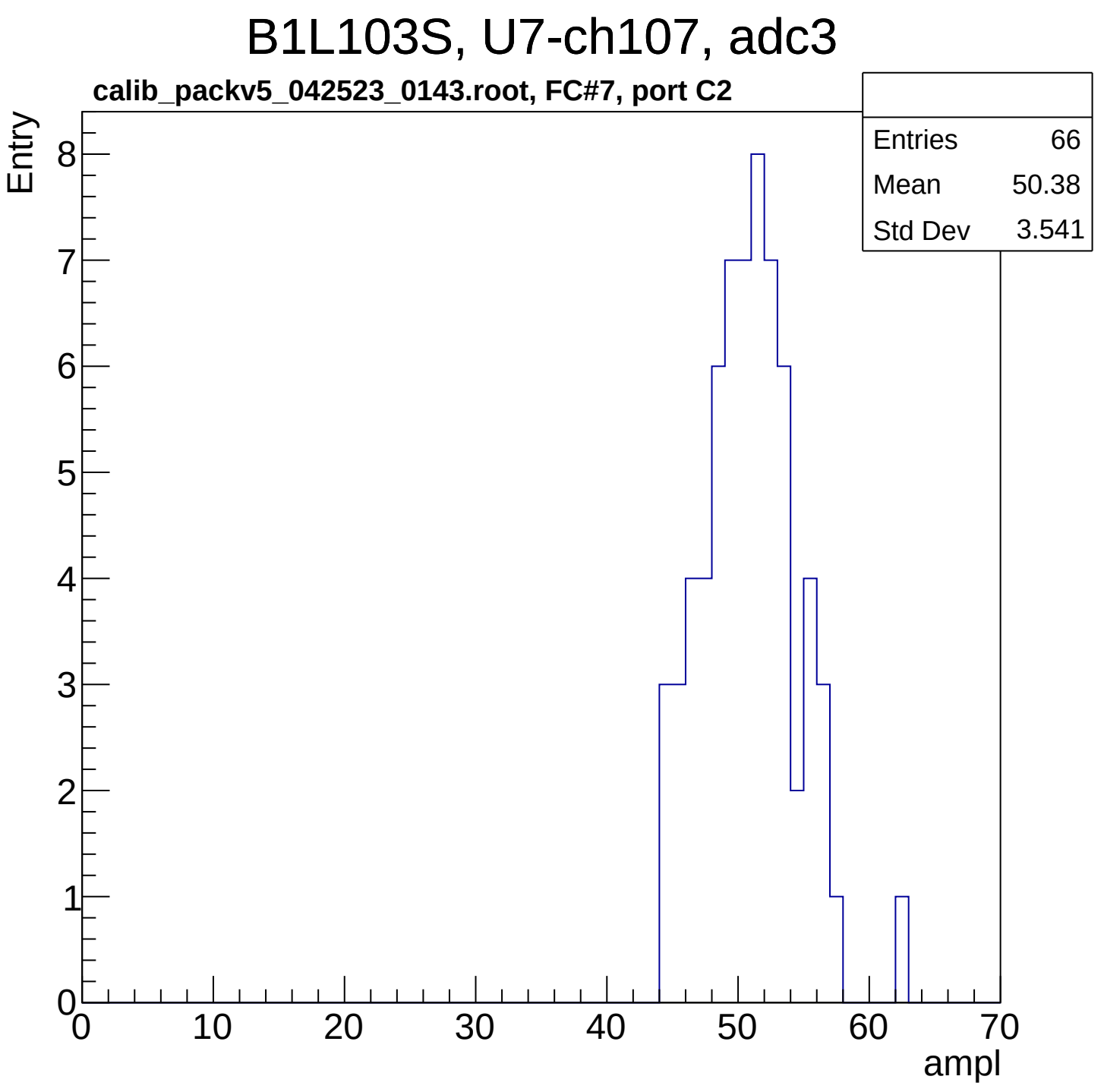
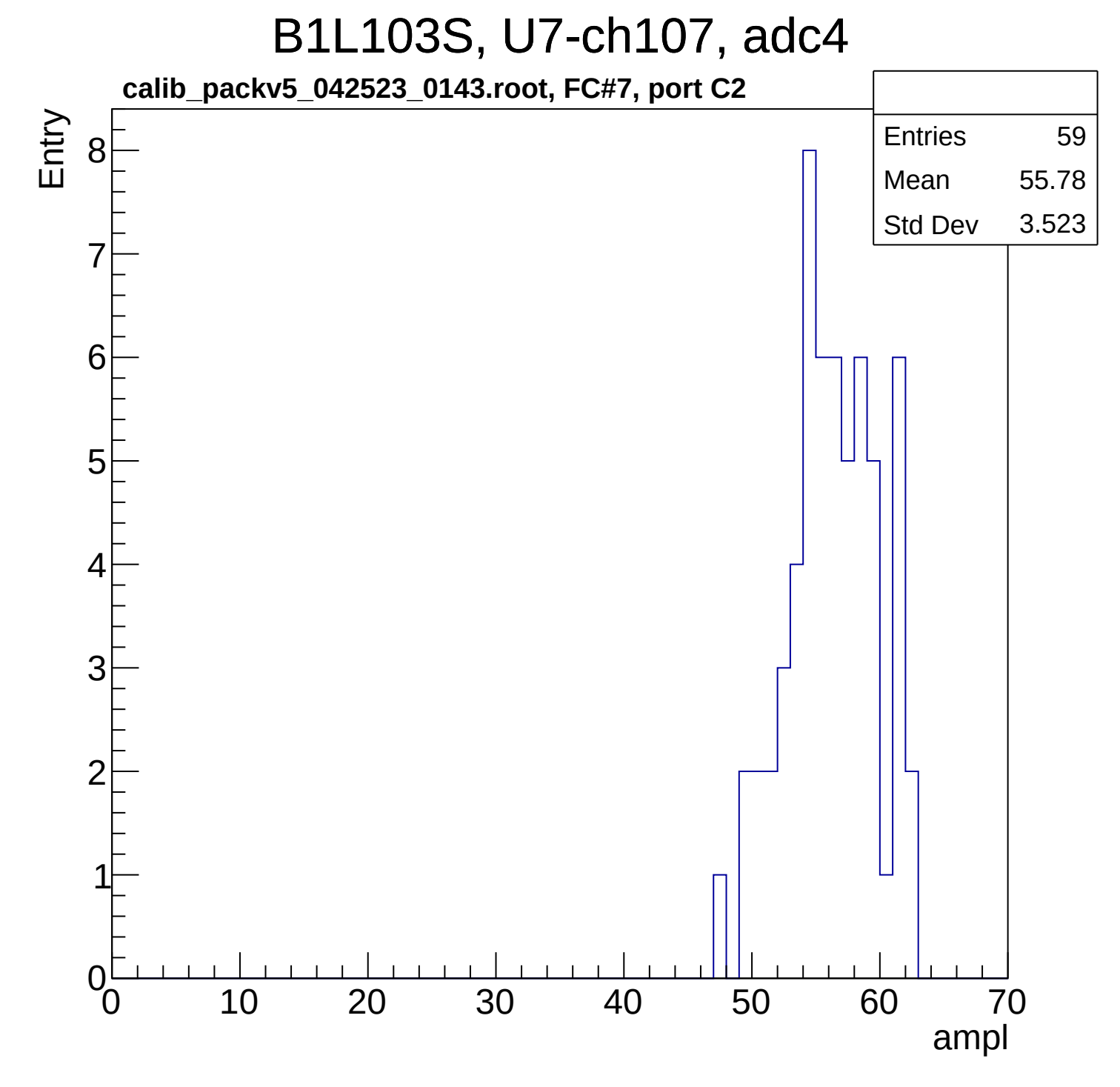

B1L103S, U7-ch107, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 50.38
Std Dev 3.541
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch107, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 55.78
Std Dev 3.523
Entry
ampl
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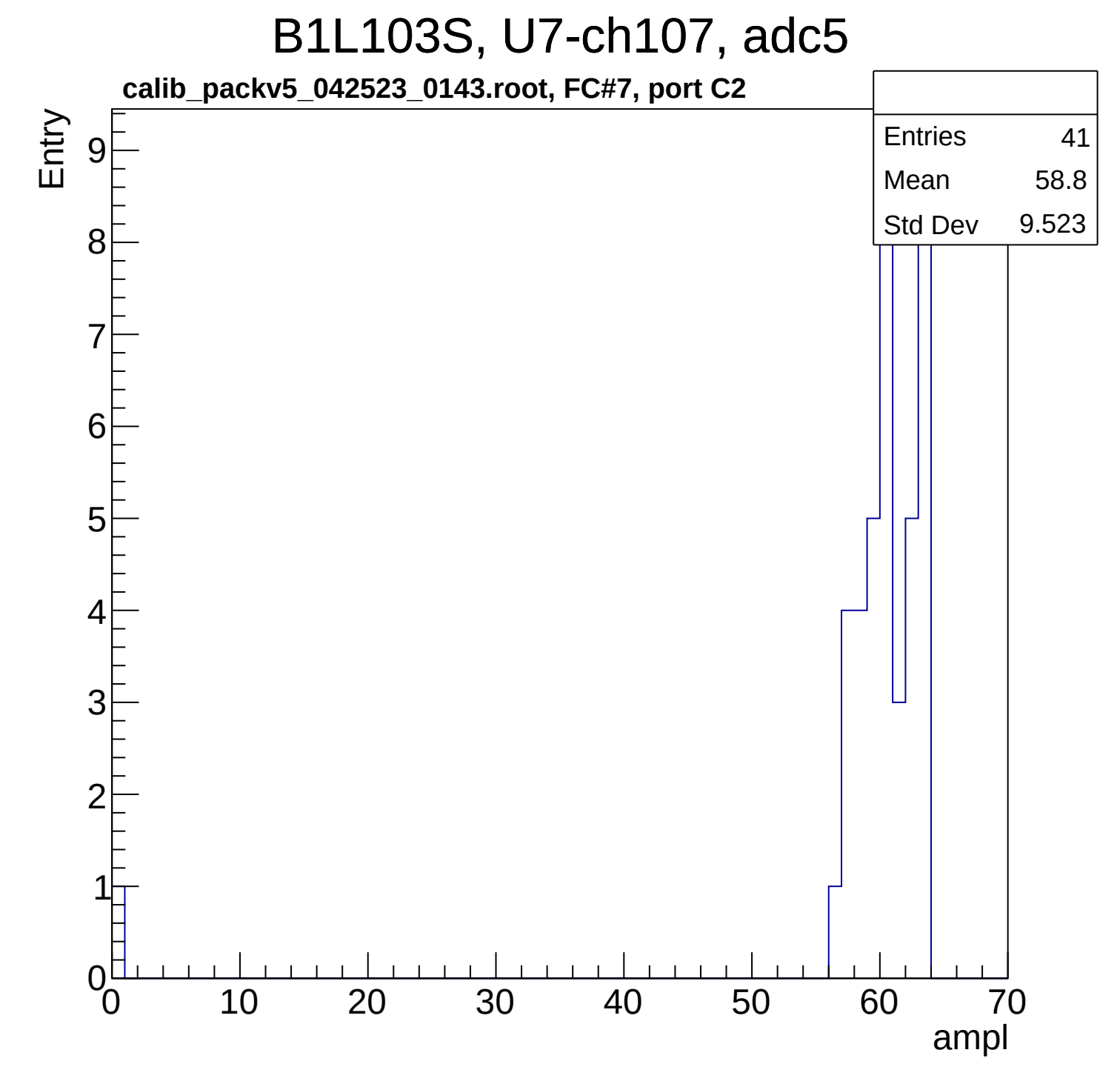
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch107, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 41
Mean 58.8
Std Dev 9.523
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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20
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40
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60
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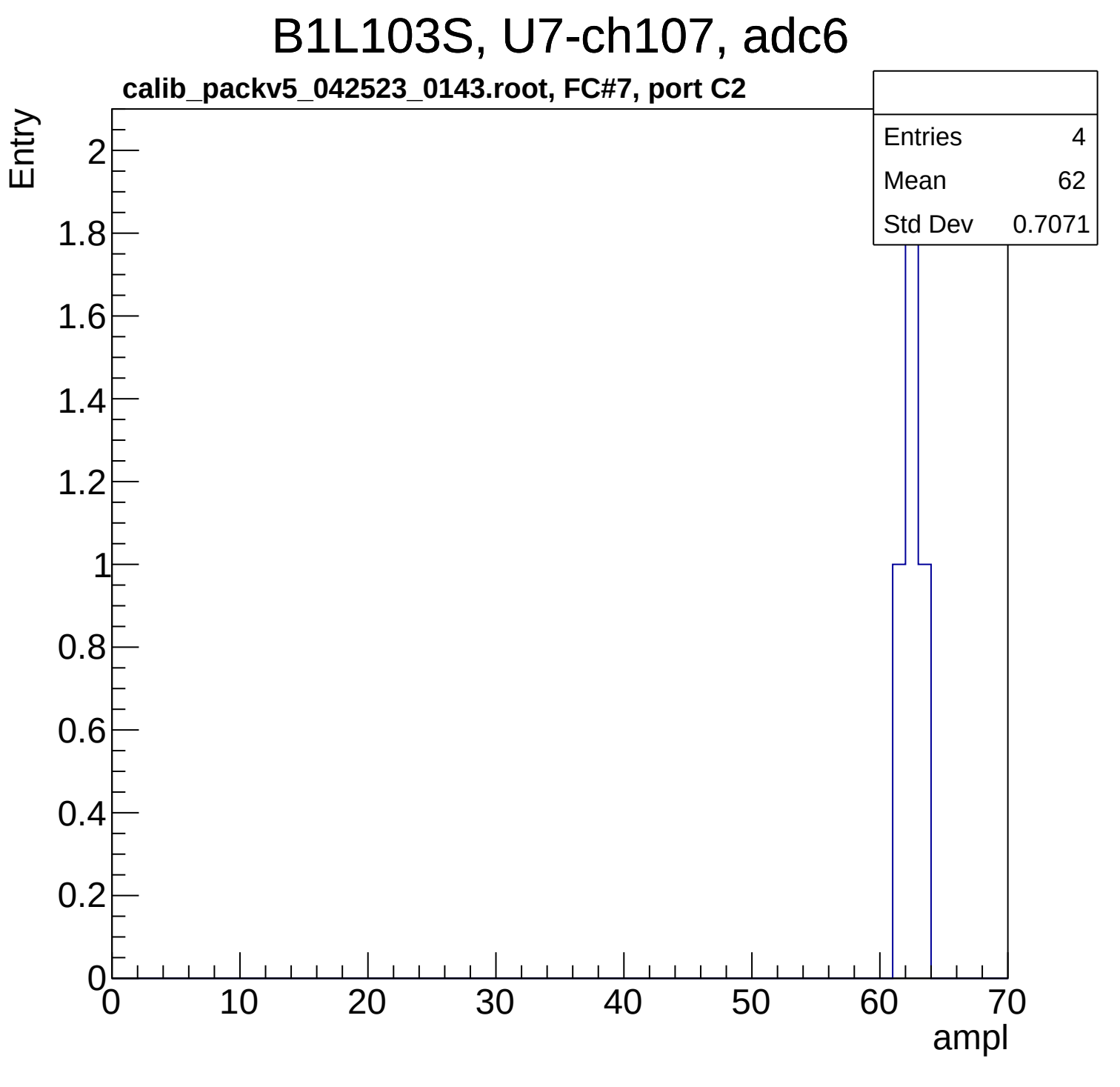
B1L103S, U7-ch107, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 4
Mean 62
Std Dev 0.7071
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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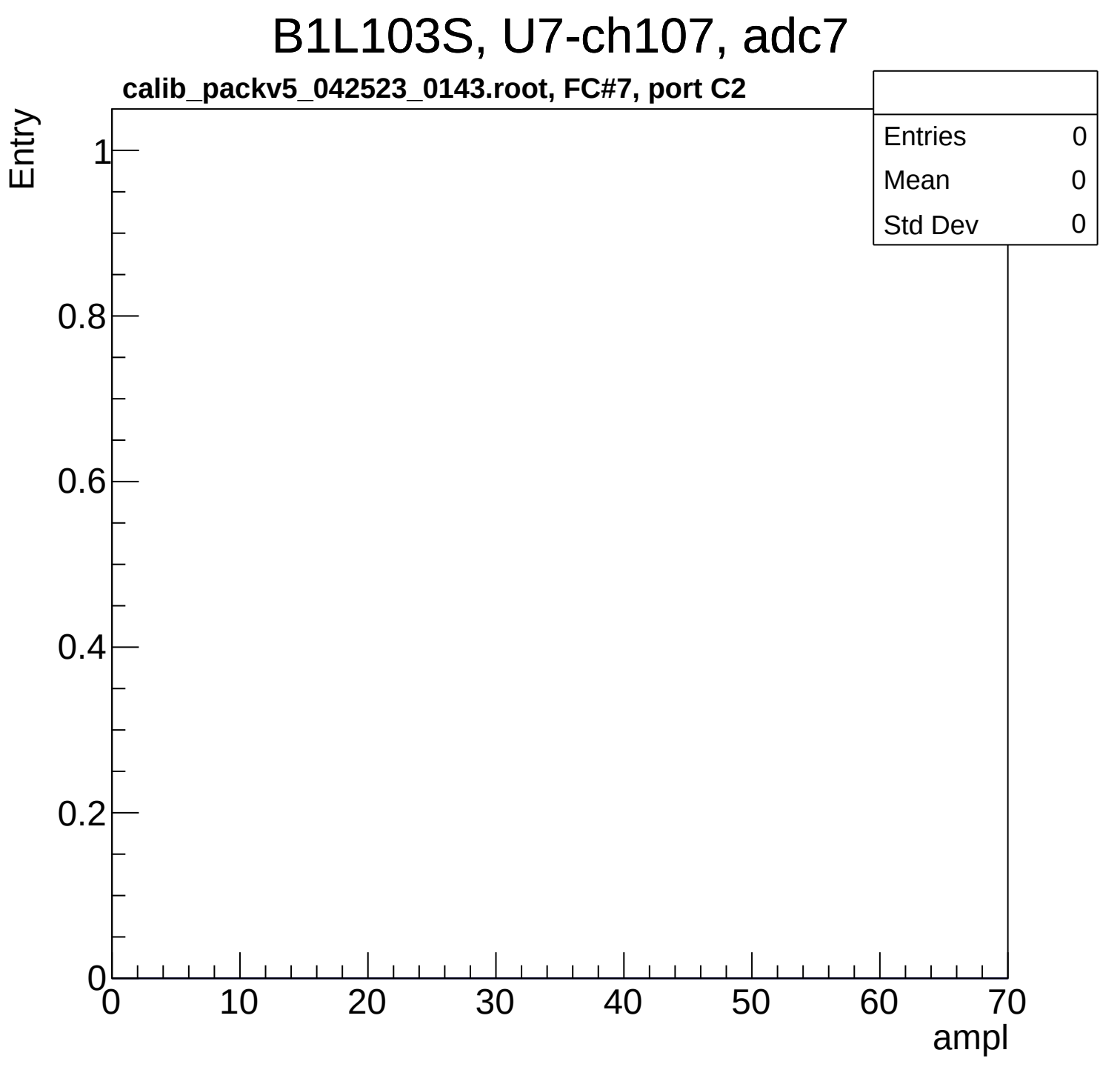
50
60
70


B1L103S, U7-ch107, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
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0.6
0.4
0.2
0
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10
20
30
40
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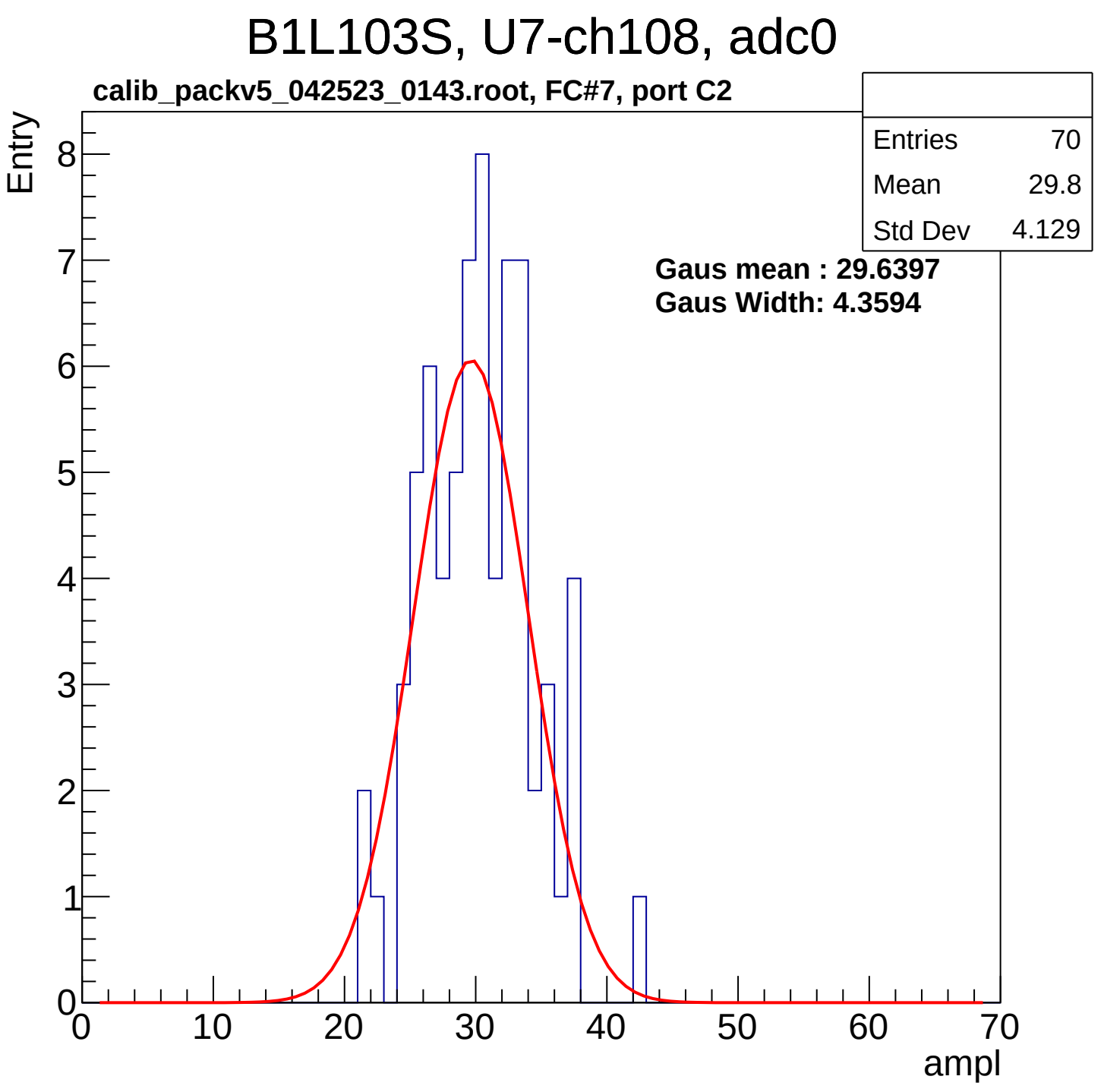
60
70
ampl


B1L103S, U7-ch108, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 29.8
Std Dev 4.129
Gaus mean : 29.6397
Gaus Width: 4.3594
Entry
ampl
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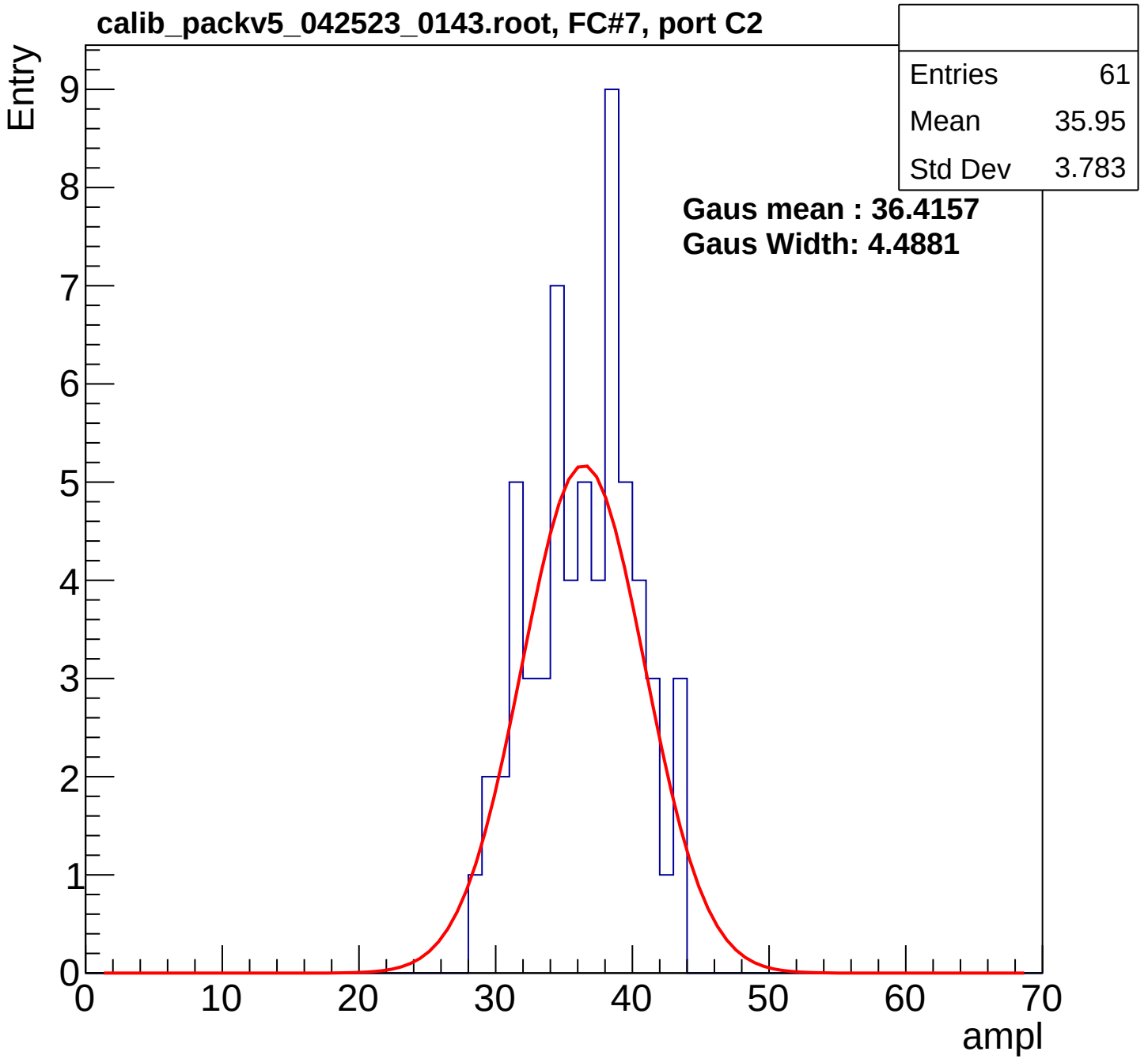
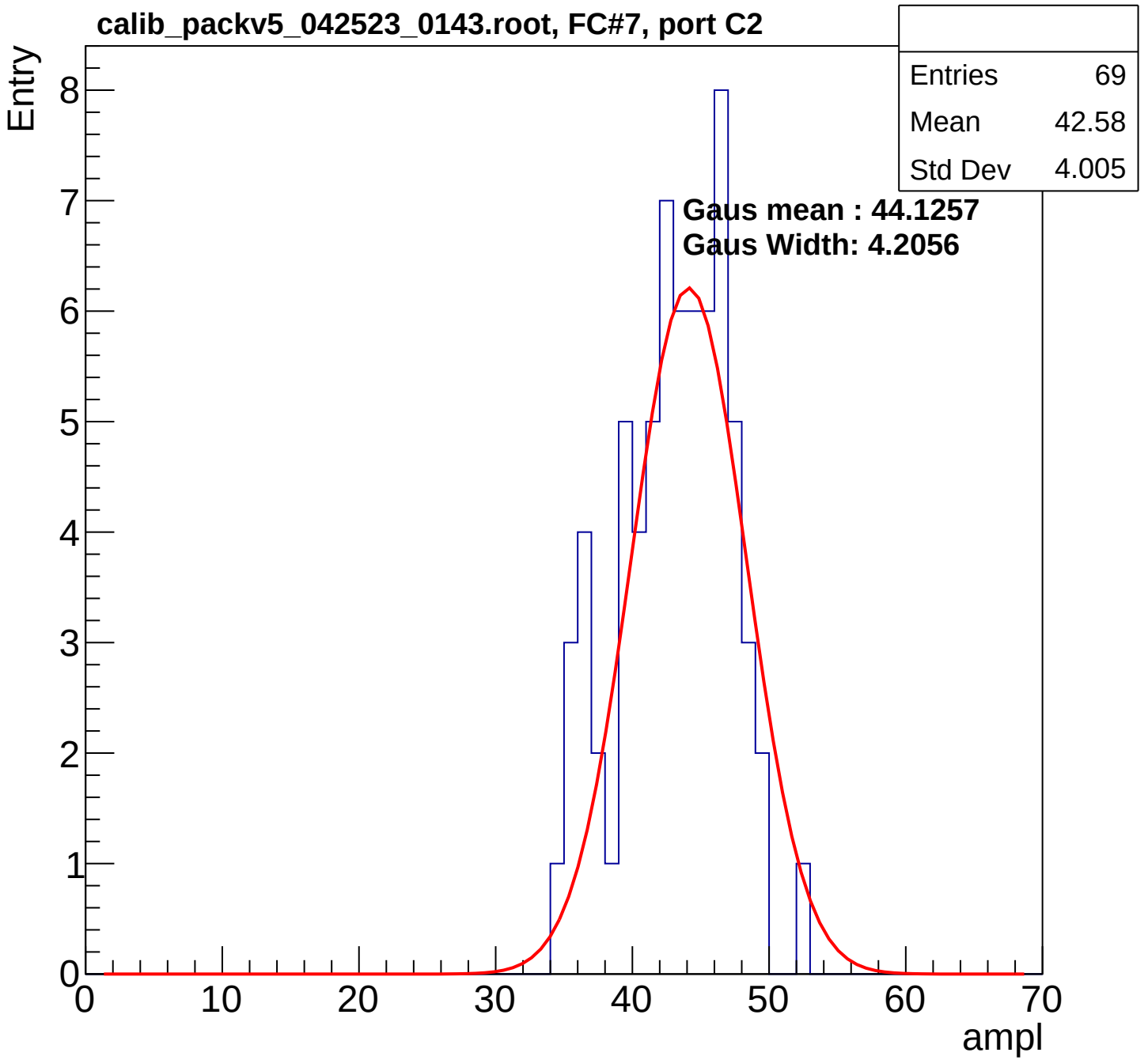
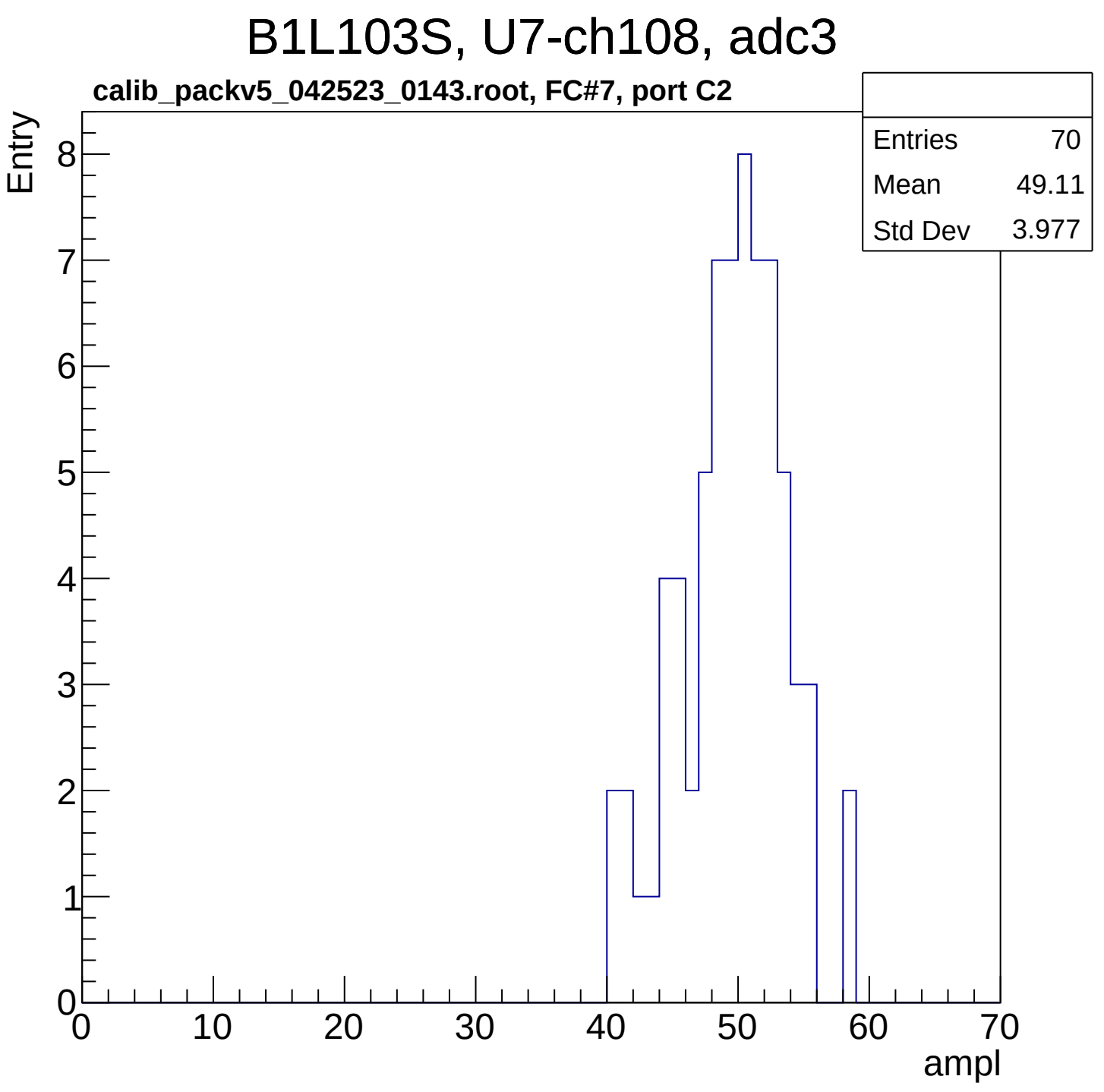
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch108, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 61
Mean 35.95
Std Dev 3.783
Gaus mean : 36.4157
Gaus Width: 4.4881
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch108, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 42.58
Std Dev 4.005
Gaus mean : 44.1257
Gaus Width: 4.2056
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch108, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 49.11
Std Dev 3.977
Entry
ampl
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1
2
3
4
5
6
7
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0
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60
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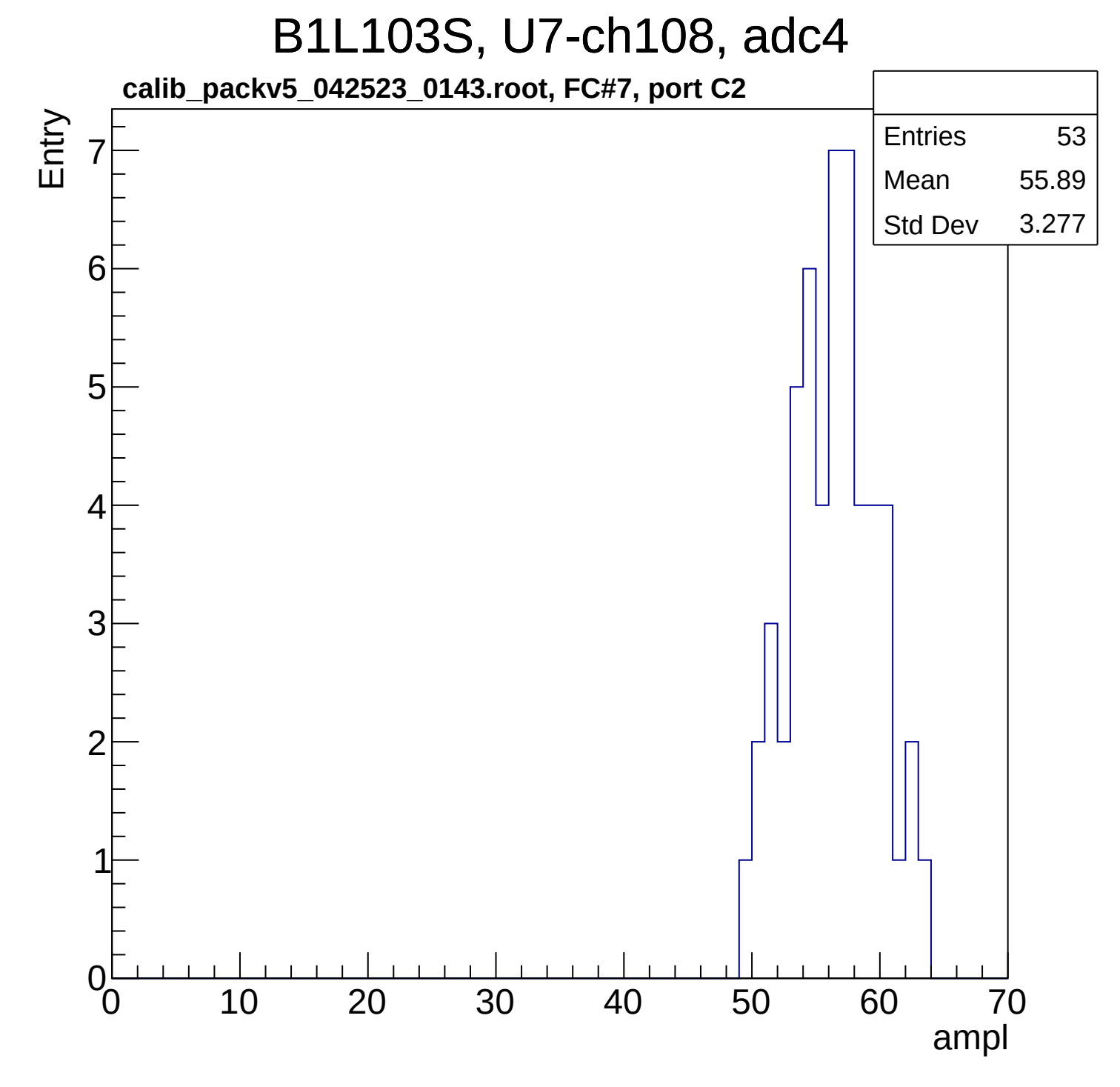
B1L103S, U7-ch108, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 55.89
Std Dev 3.277
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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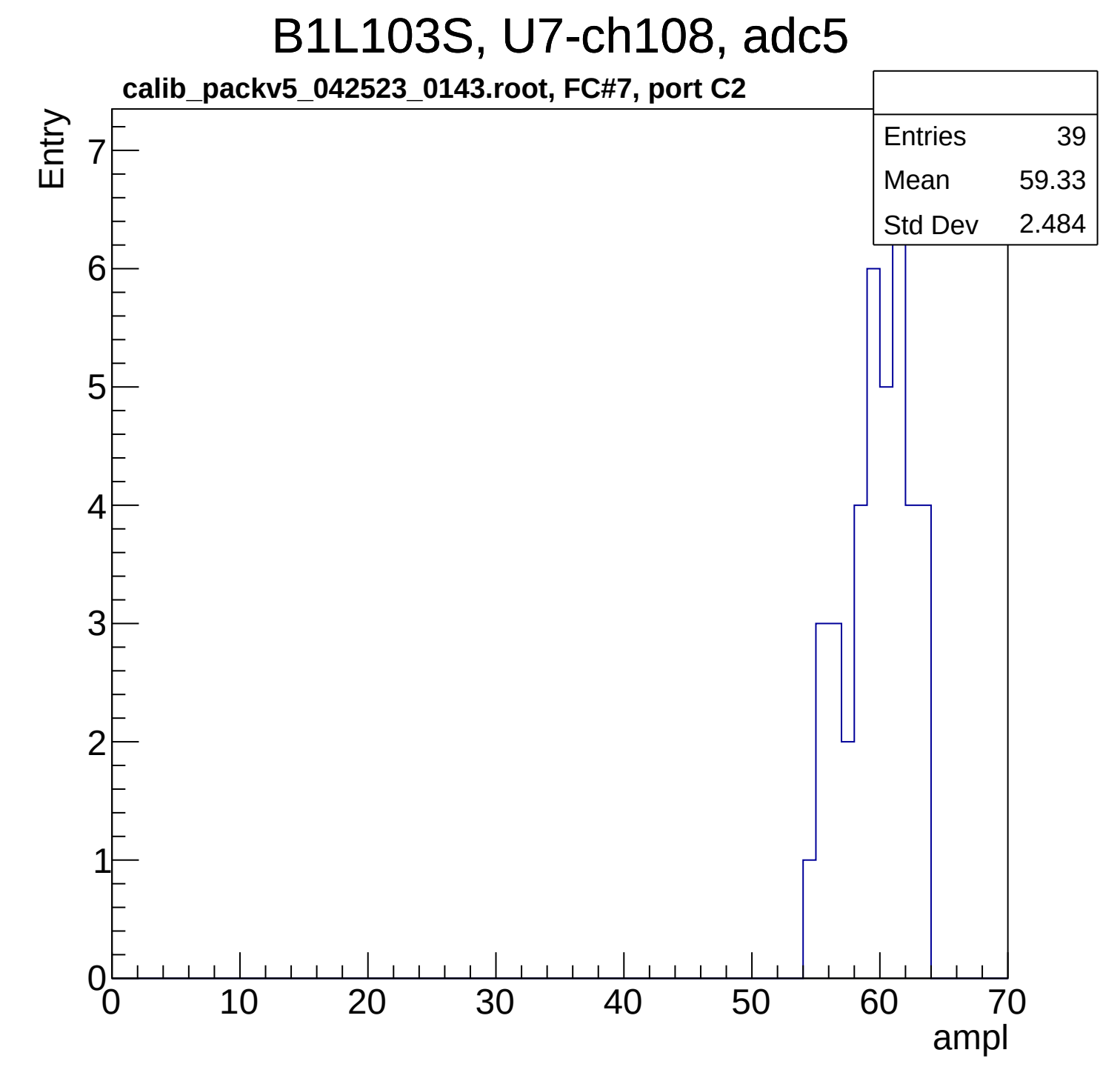
B1L103S, U7-ch108, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 39
Mean 59.33
Std Dev 2.484
Entry
ampl
0
1
2
3
4
5
6
7
0
10
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30
40
50
60
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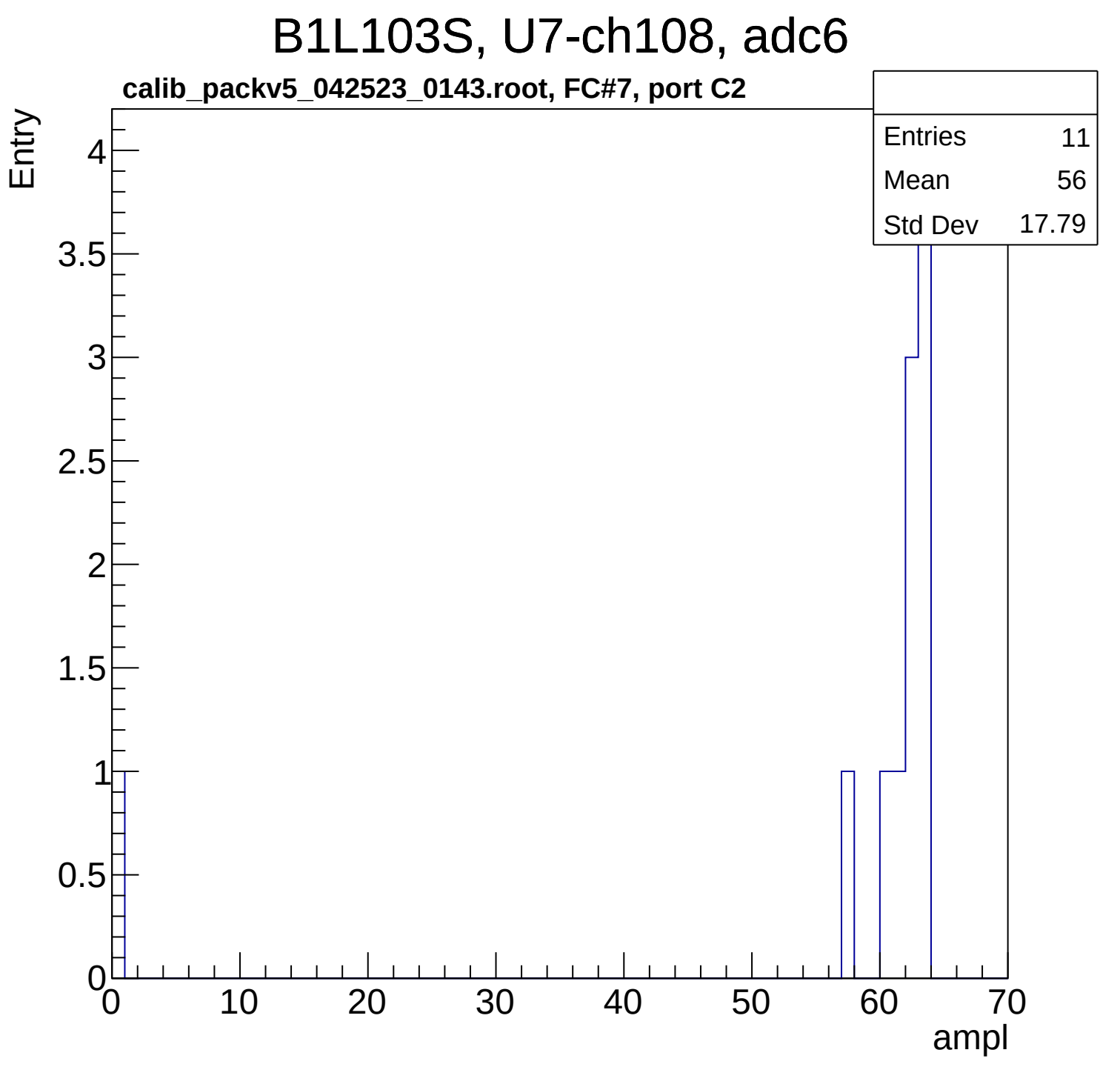
B1L103S, U7-ch108, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 11
Mean 56
Std Dev 17.79
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
10
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40
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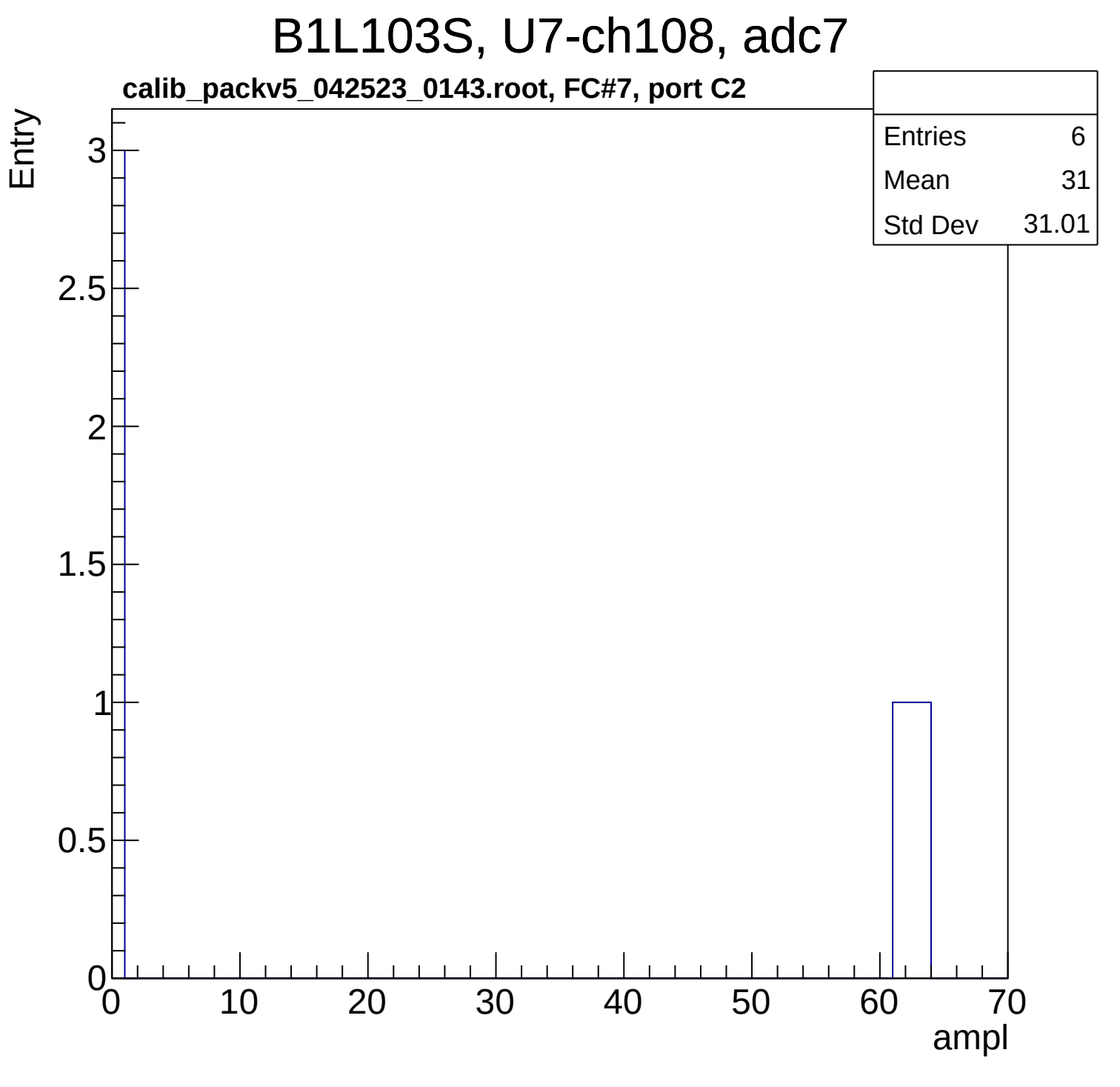
60
70


B1L103S, U7-ch108, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 6
Mean 31
Std Dev 31.01
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
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40
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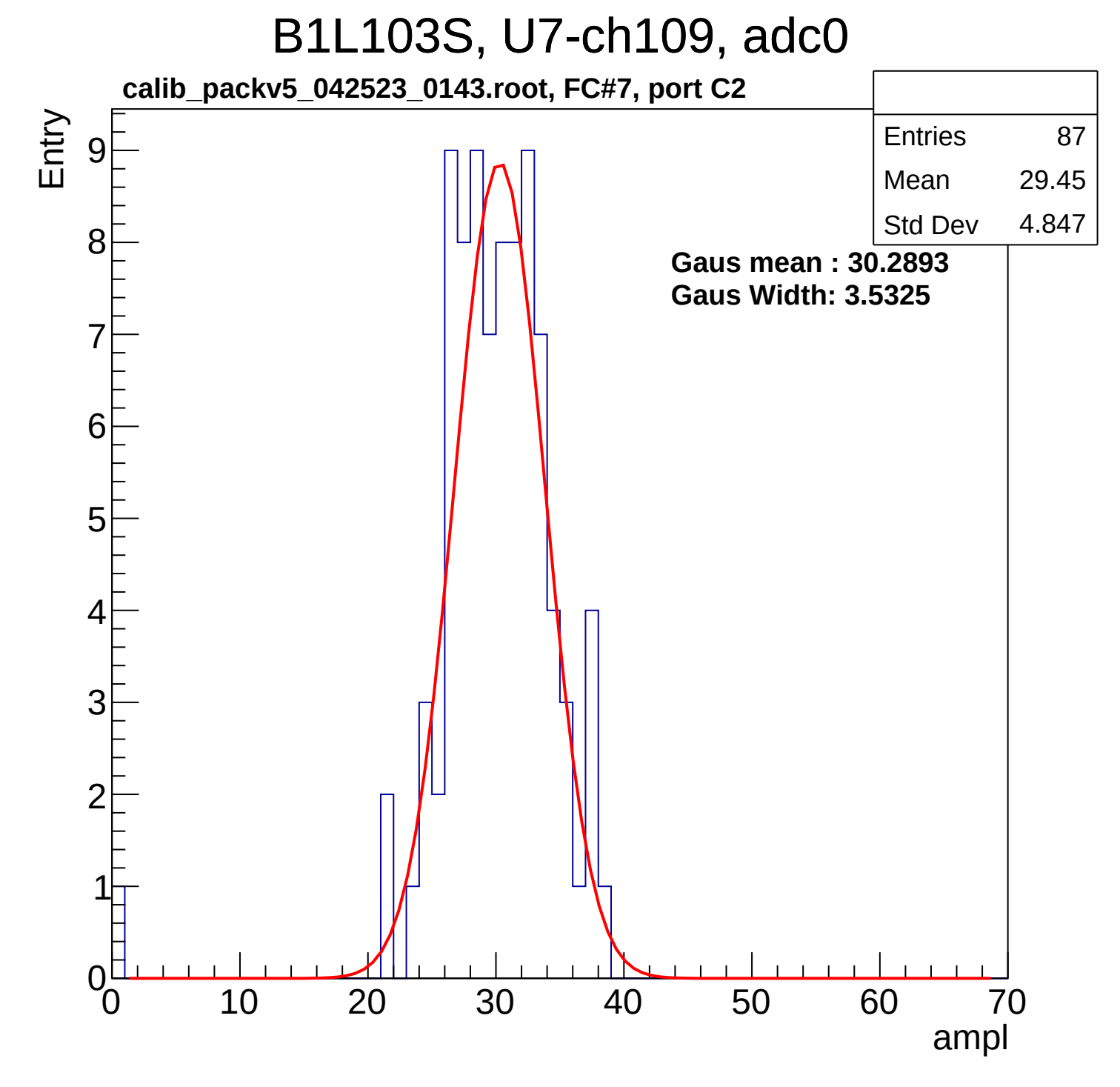
B1L103S, U7-ch109, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 87
Mean 29.45
Std Dev 4.847
Gaus mean : 30.2893
Gaus Width: 3.5325
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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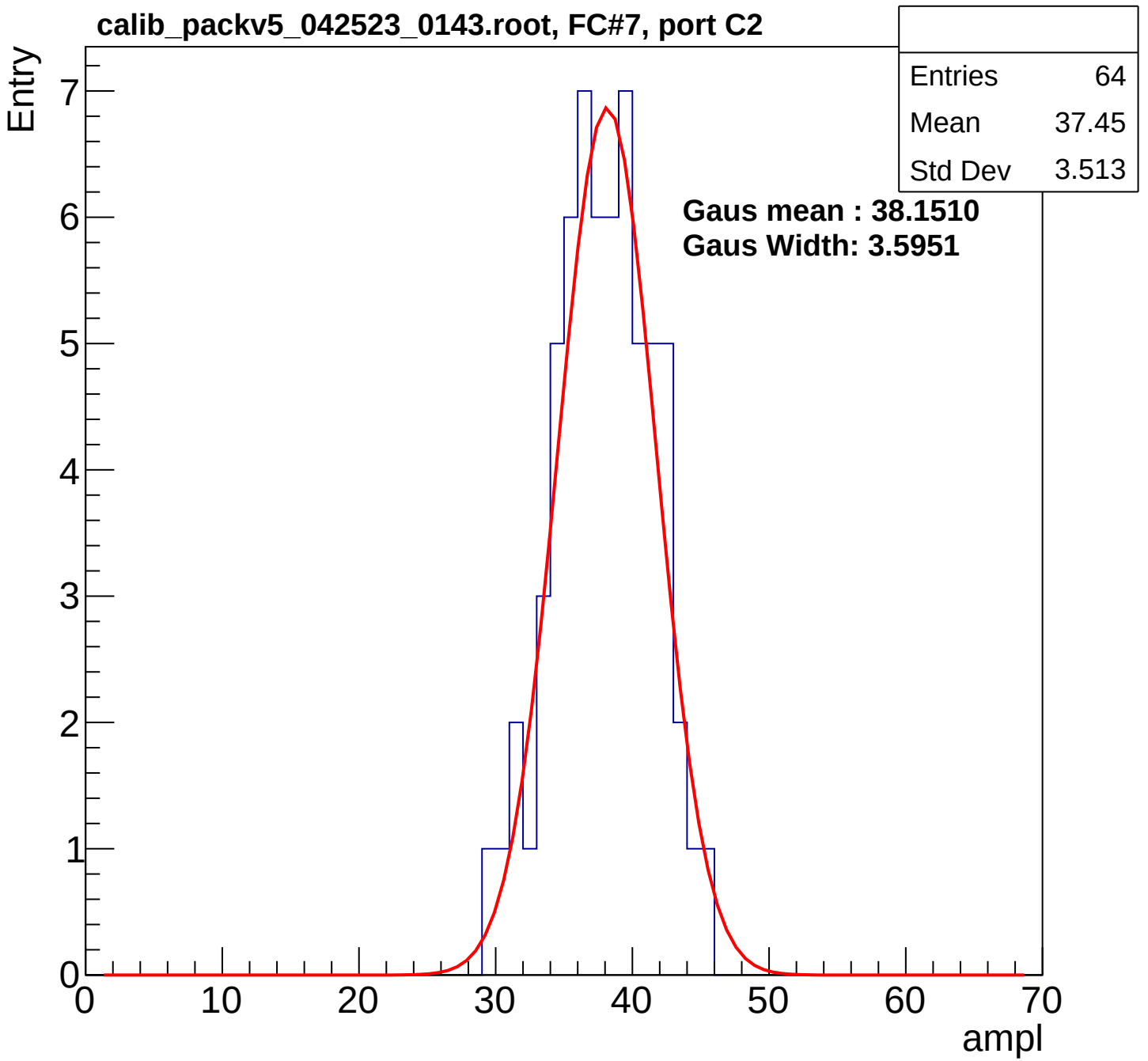
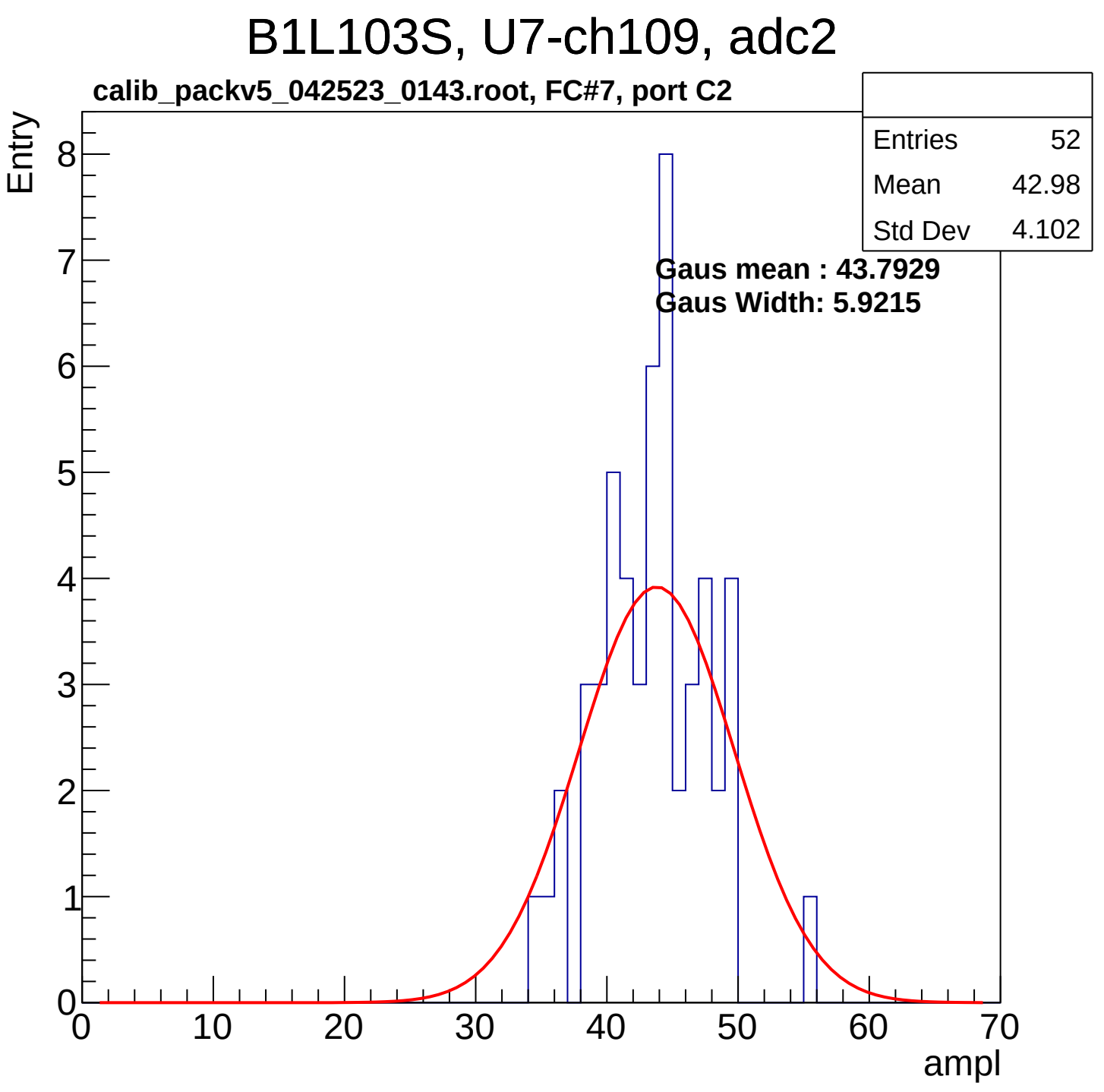

B1L103S, U7-ch109, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 37.45
Std Dev 3.513
Gaus mean : 38.1510
Gaus Width: 3.5951
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch109, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 52
Mean 42.98
Std Dev 4.102
Gaus mean : 43.7929
Gaus Width: 5.9215
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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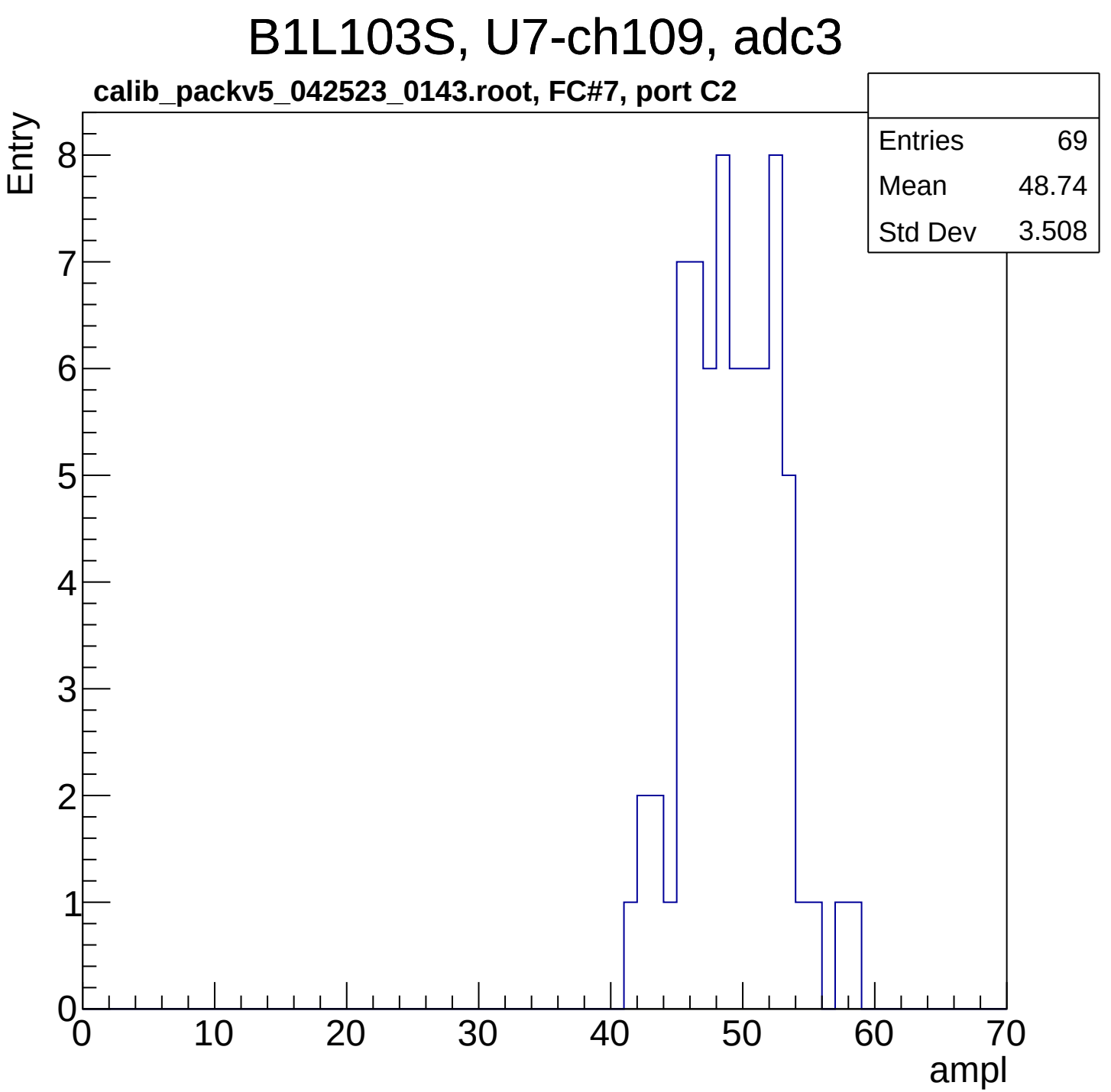
B1L103S, U7-ch109, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 48.74
Std Dev 3.508
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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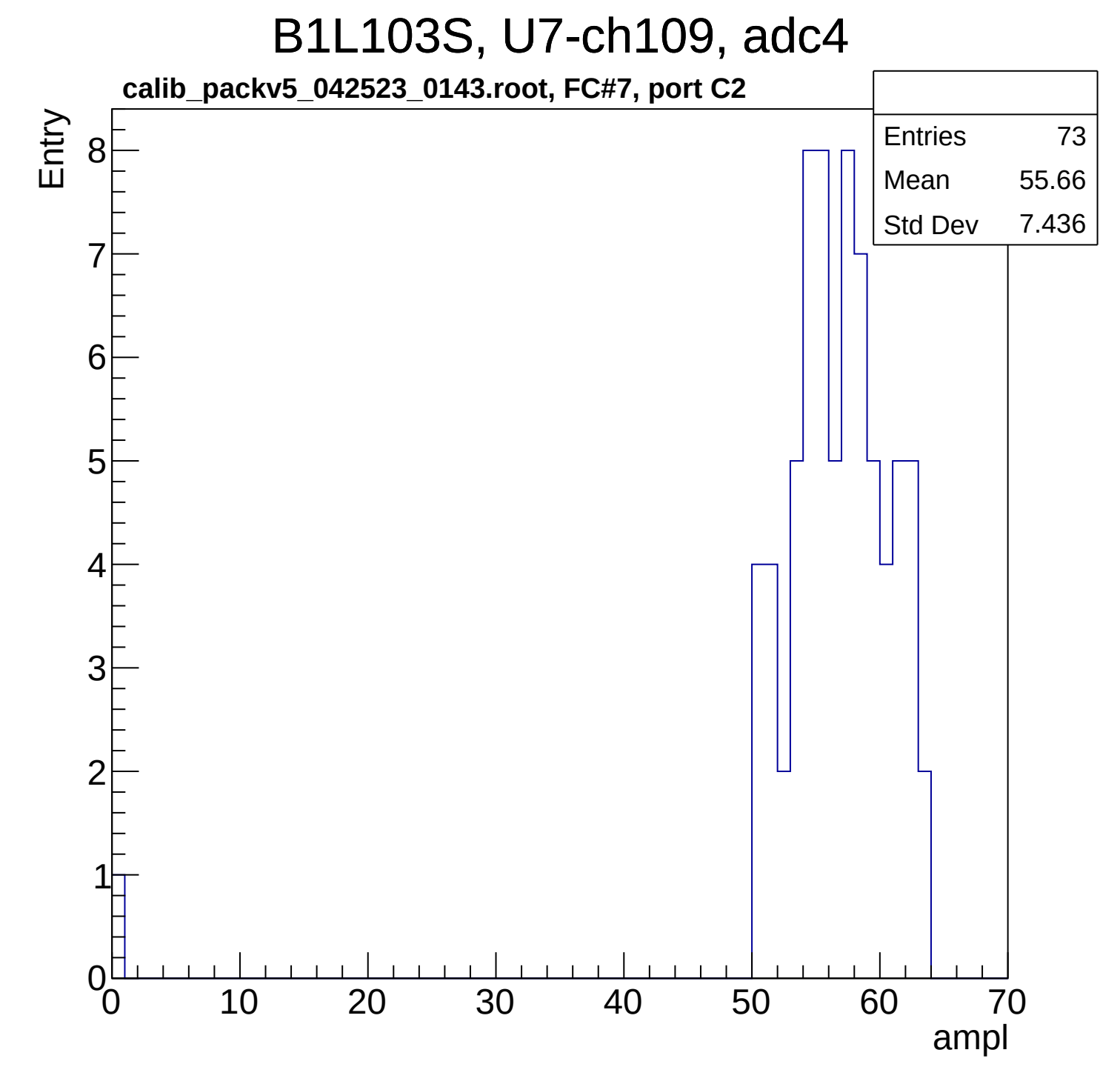
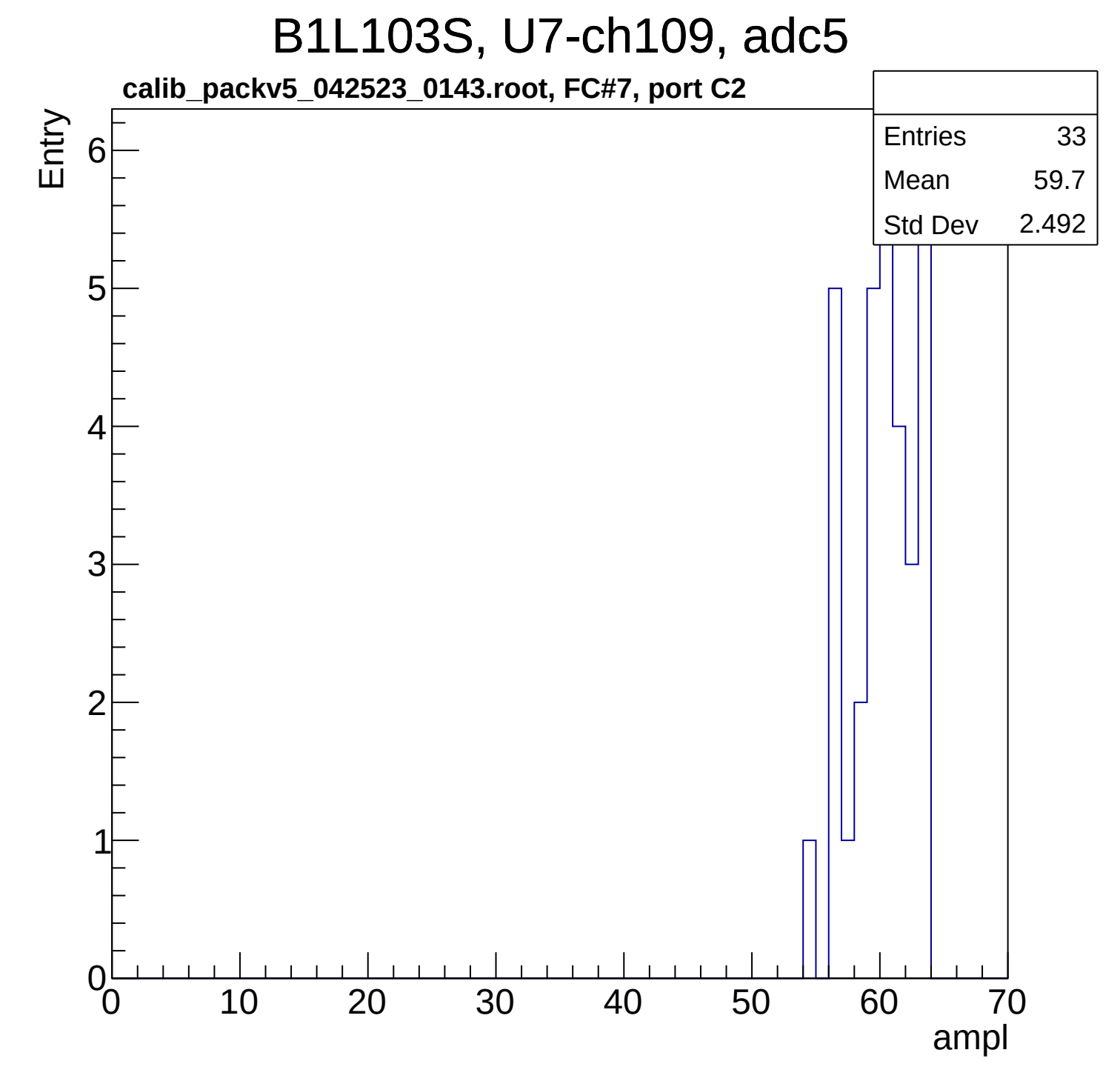

B1L103S, U7-ch109, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 73
Mean 55.66
Std Dev 7.436
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch109, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 33
Mean 59.7
Std Dev 2.492
Entry
ampl
0
1
2
3
4
5
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0
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60
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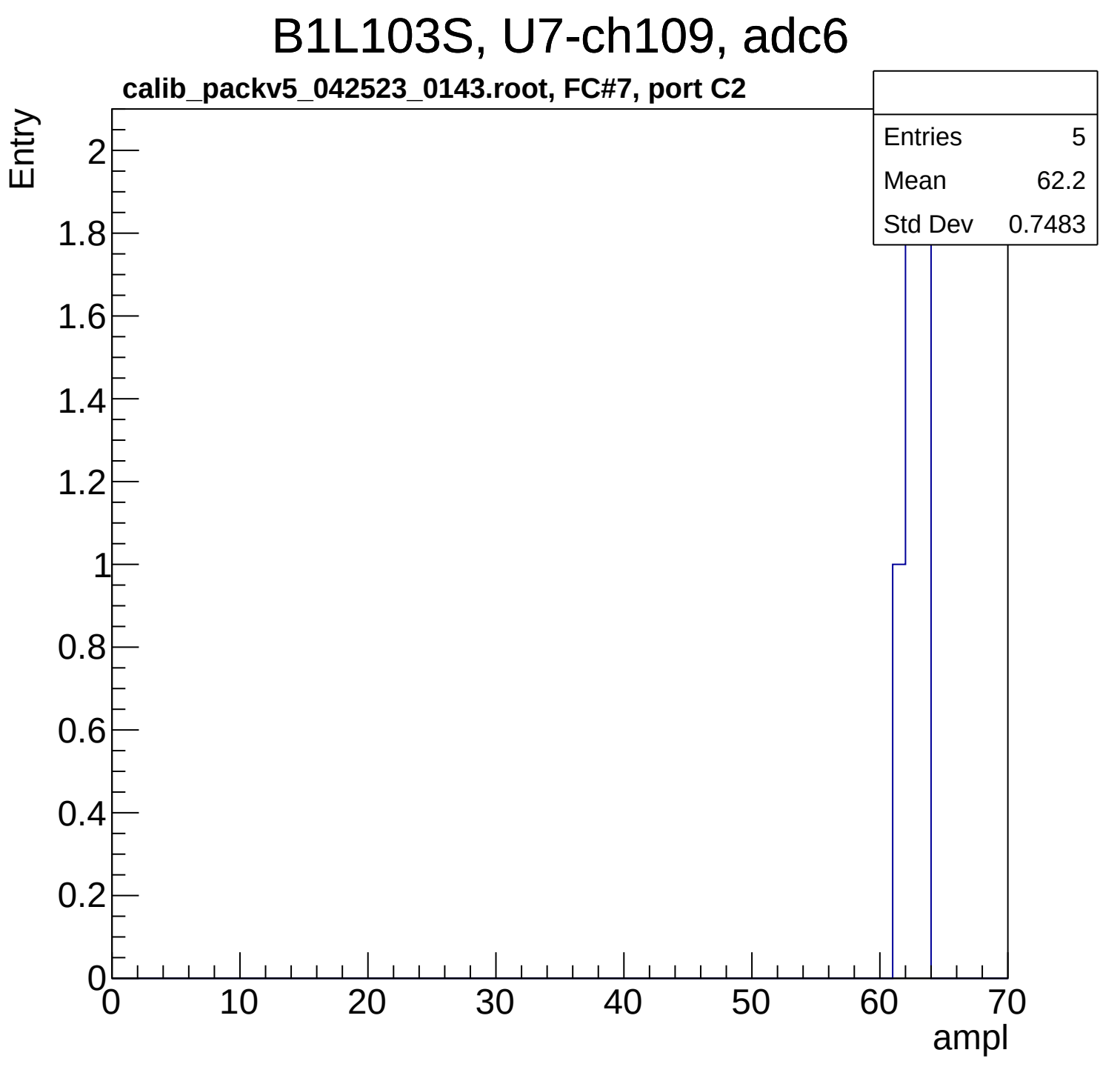
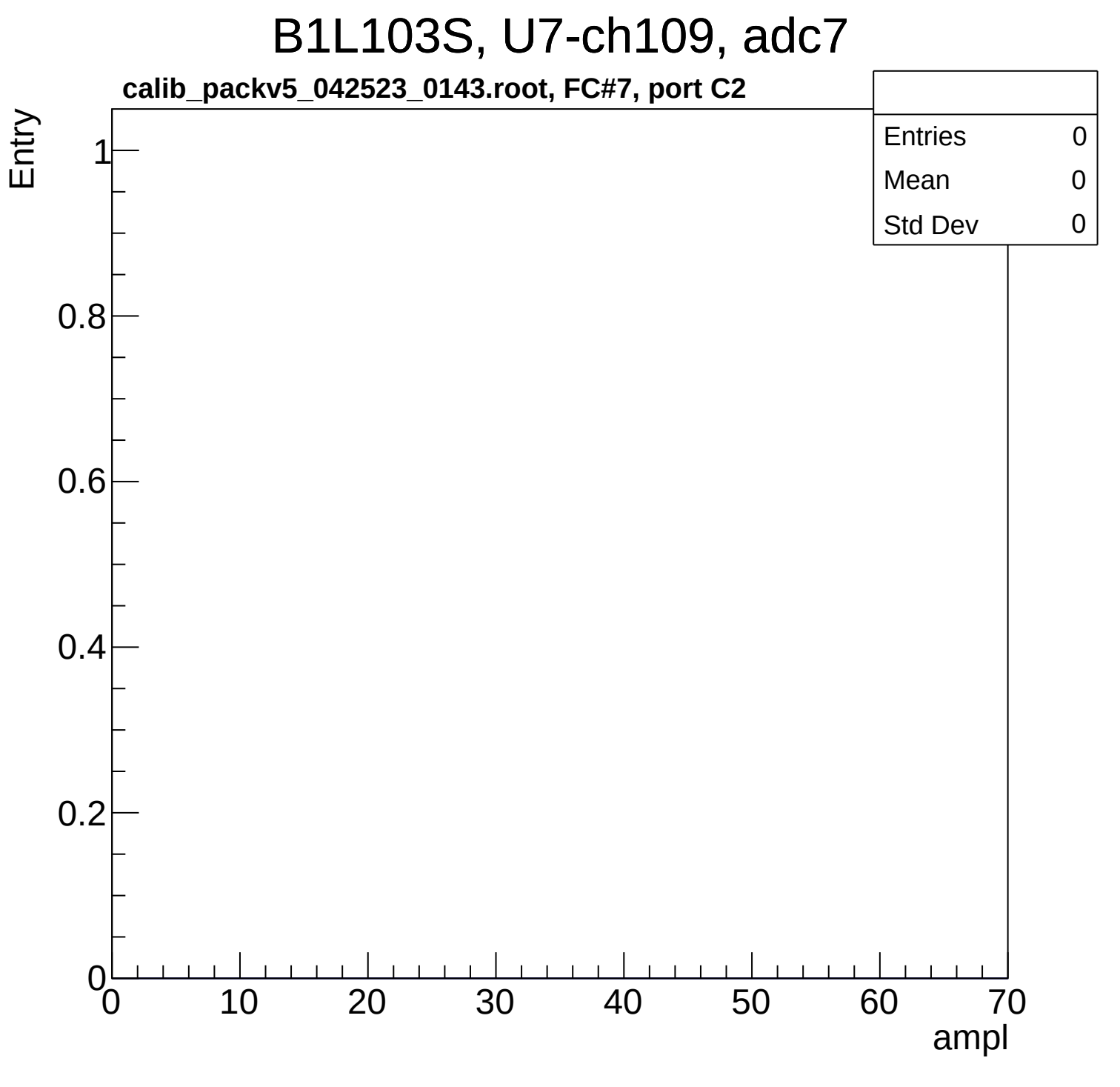
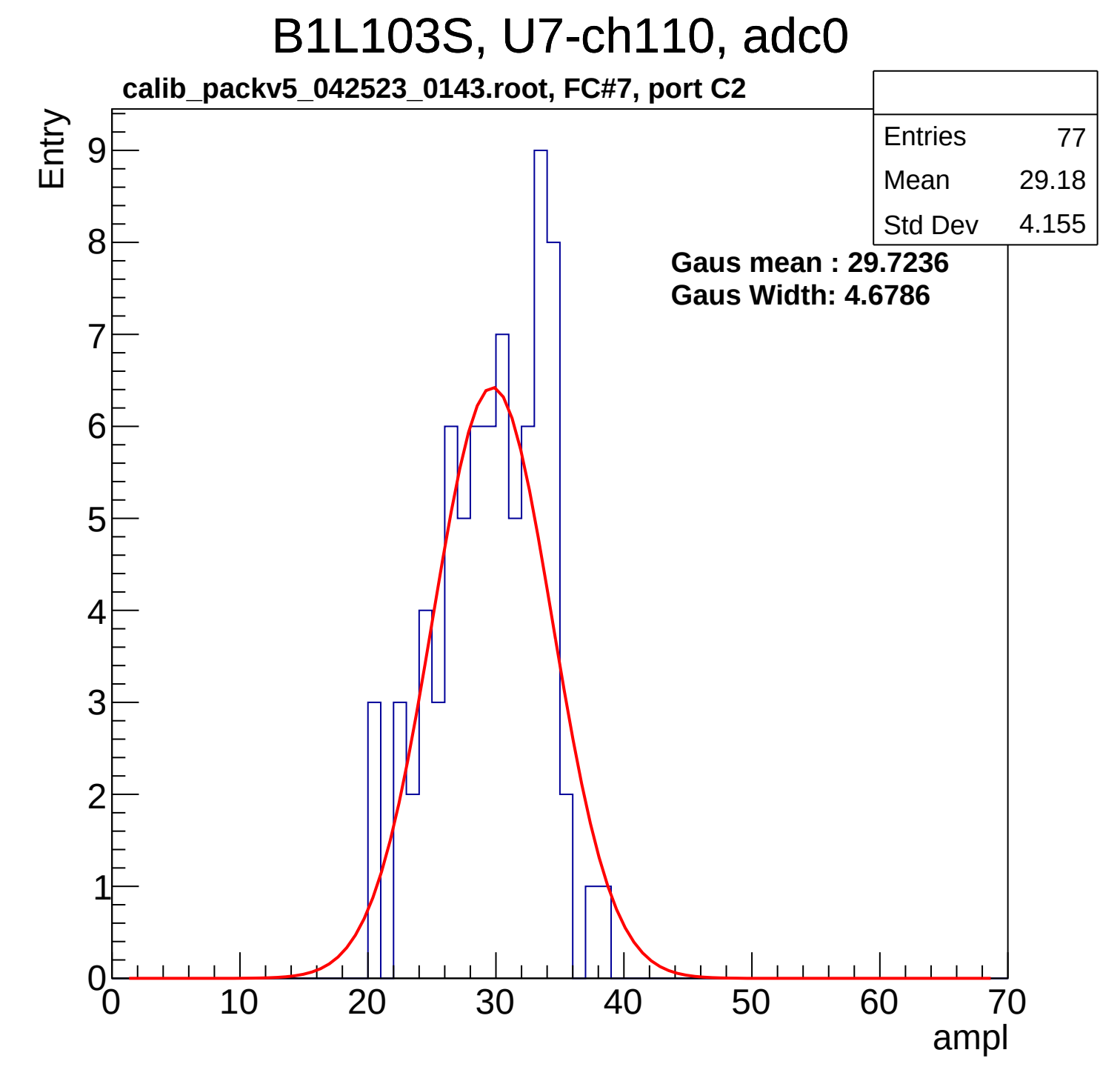

B1L103S, U7-ch109, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 5
Mean 62.2
Std Dev 0.7483
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U7-ch109, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch110, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 77
Mean 29.18
Std Dev 4.155
Gaus mean : 29.7236
Gaus Width: 4.6786
Entry
ampl
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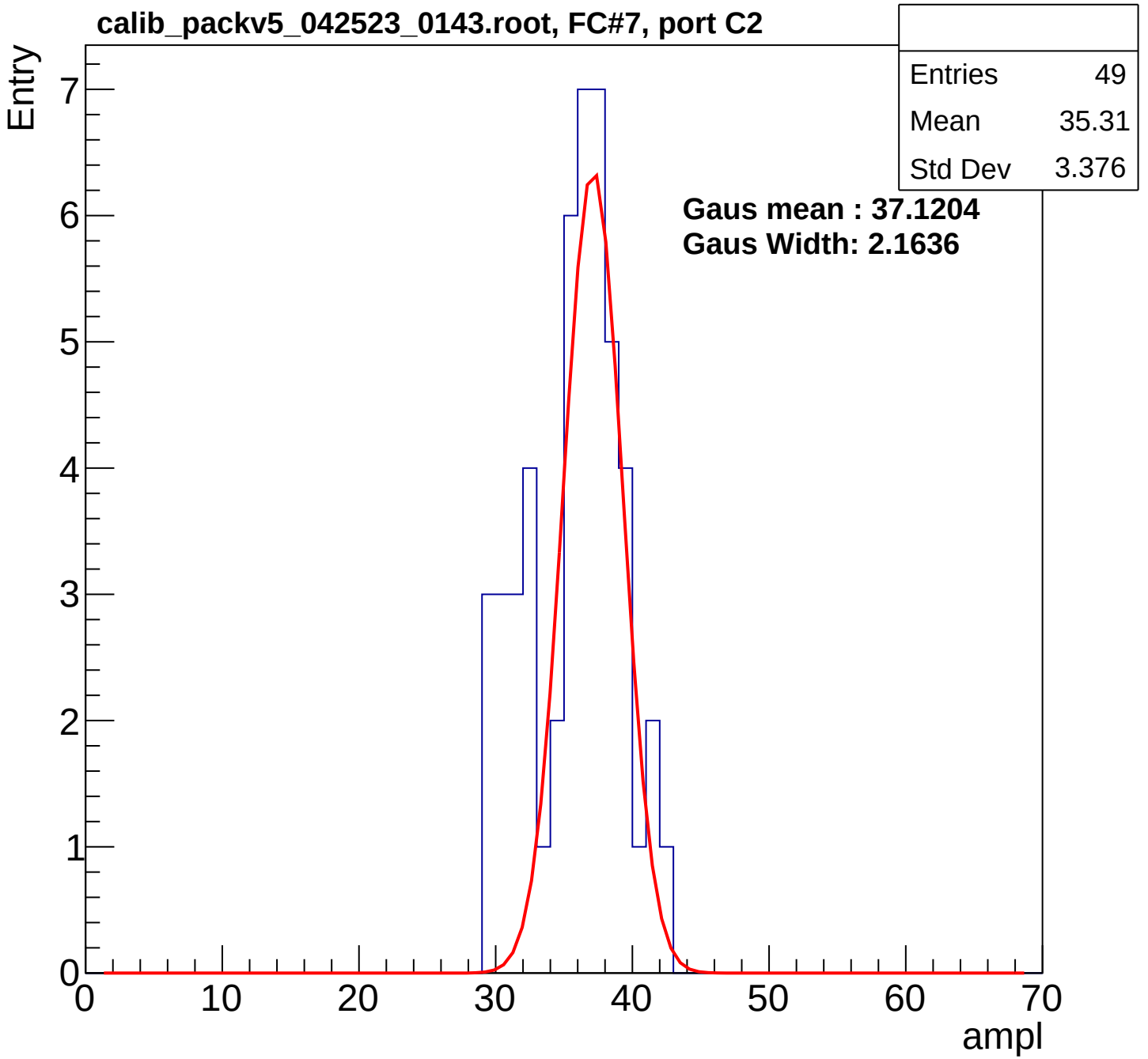
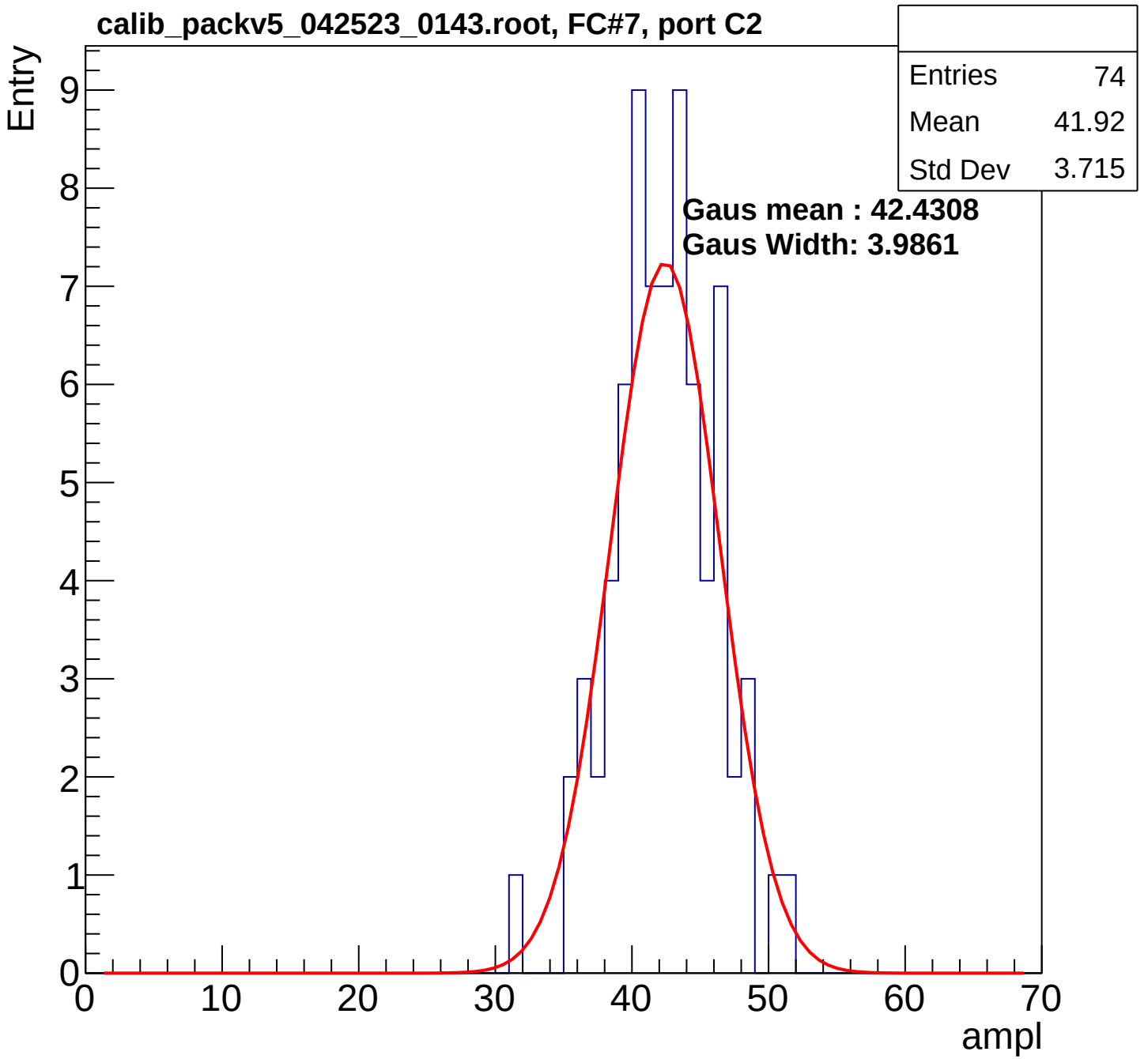
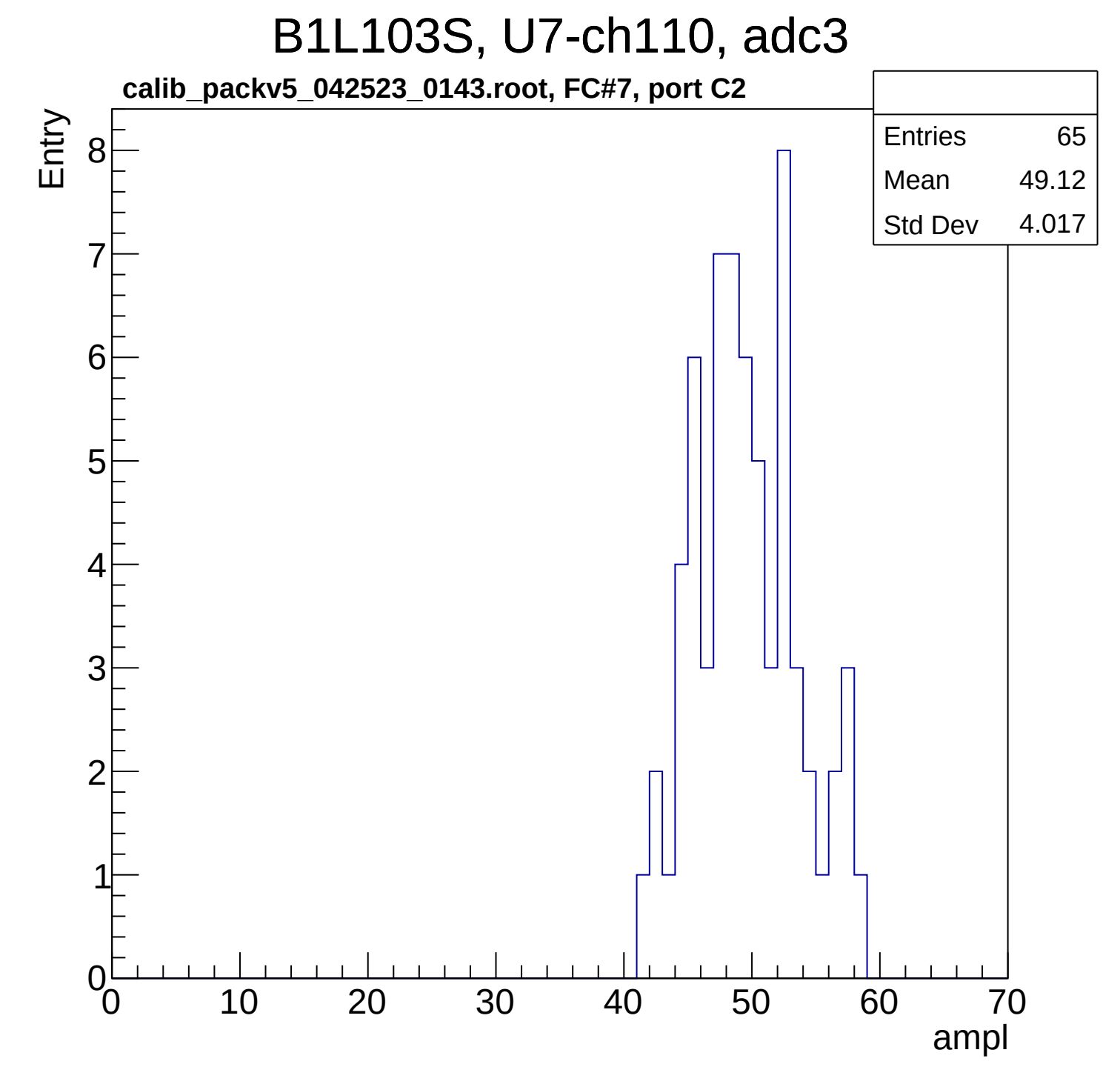
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch110, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 49
Mean 35.31
Std Dev 3.376
Gaus mean : 37.1204
Gaus Width: 2.1636
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch110, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 74
Mean 41.92
Std Dev 3.715
Gaus mean : 42.4308
Gaus Width: 3.9861
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch110, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 49.12
Std Dev 4.017
Entry
ampl
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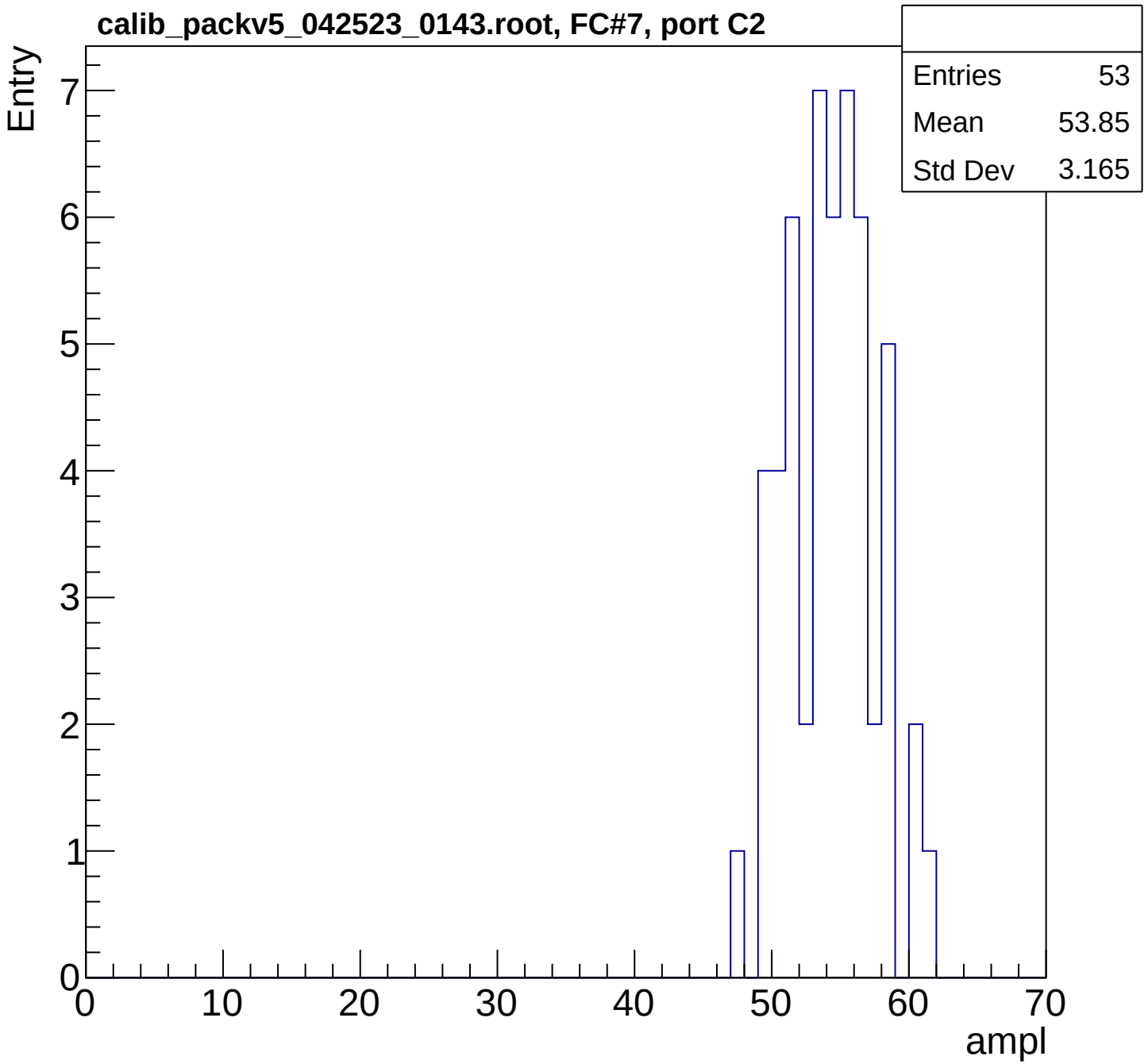
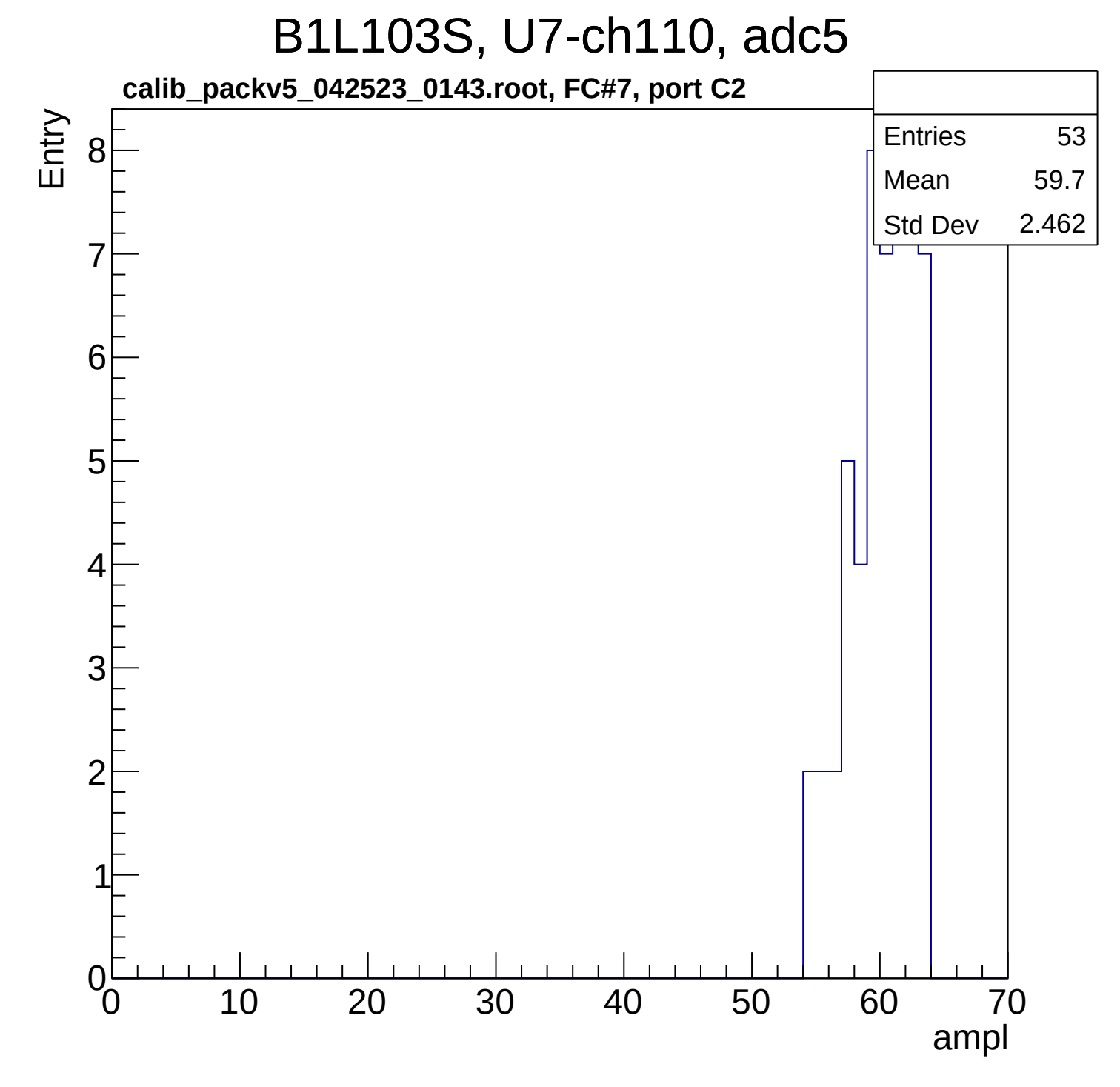
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch110, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 53.85
Std Dev 3.165
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch110, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 59.7
Std Dev 2.462
Entry
ampl
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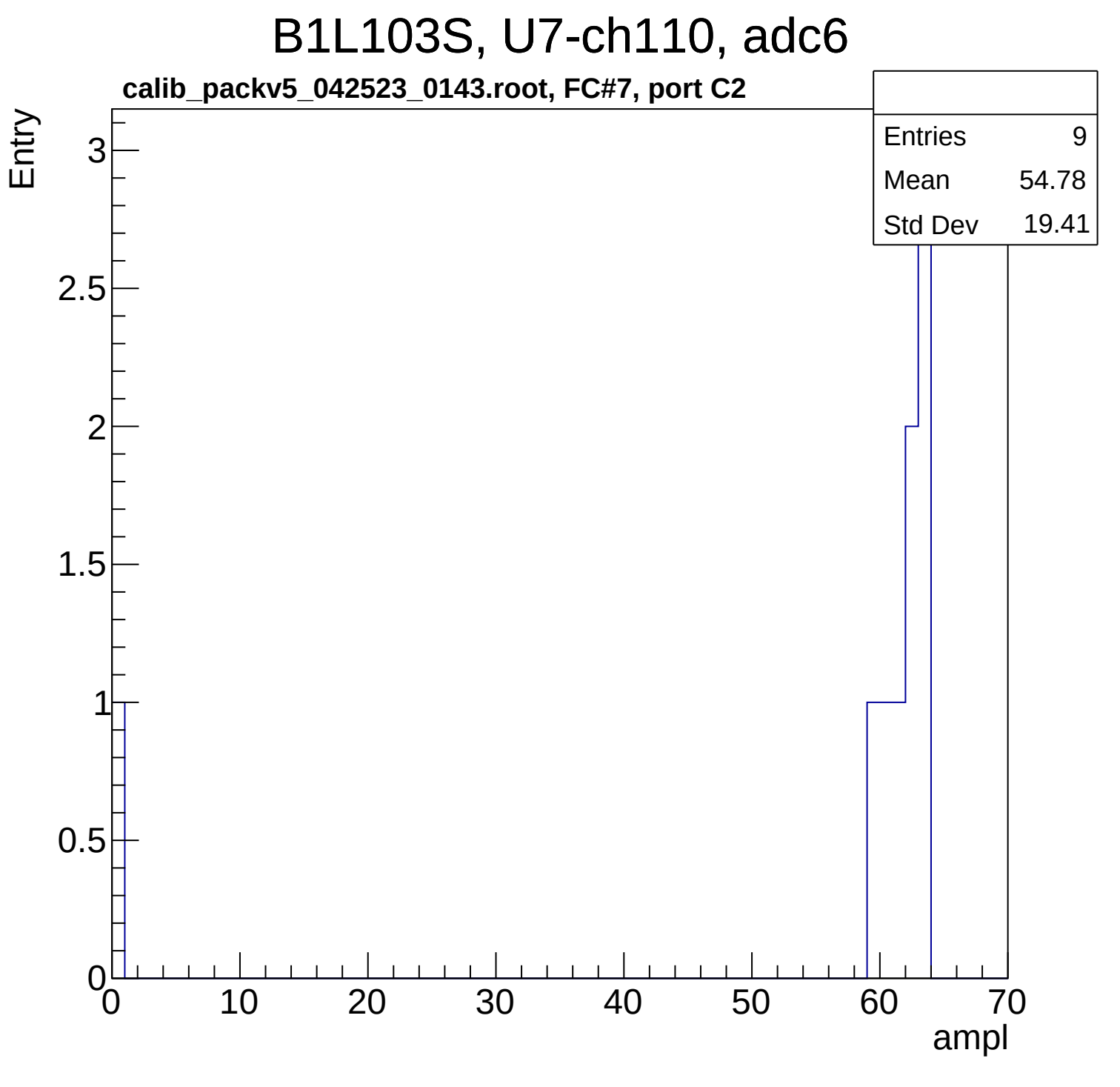
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch110, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 9
Mean 54.78
Std Dev 19.41
Entry
ampl
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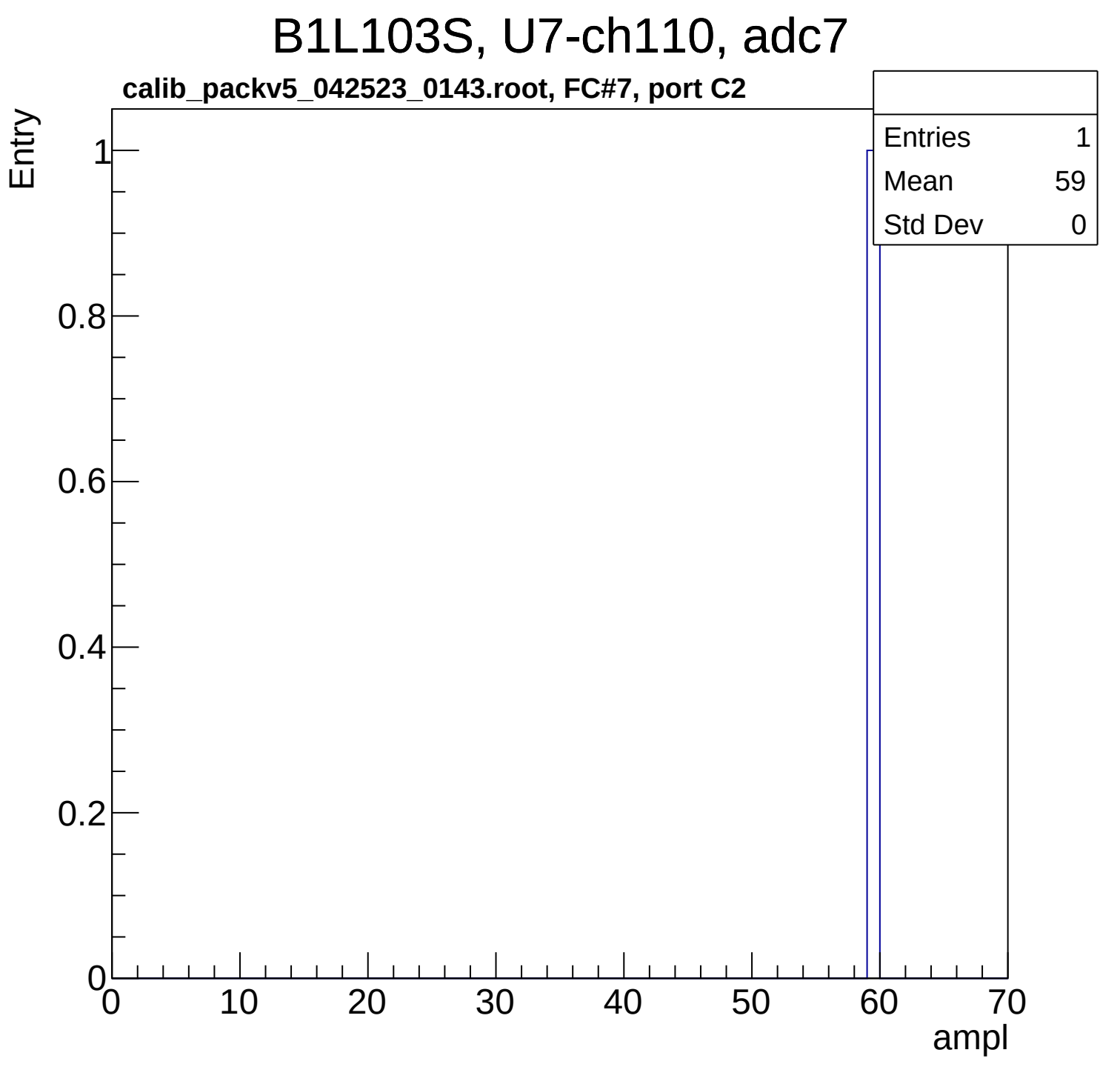
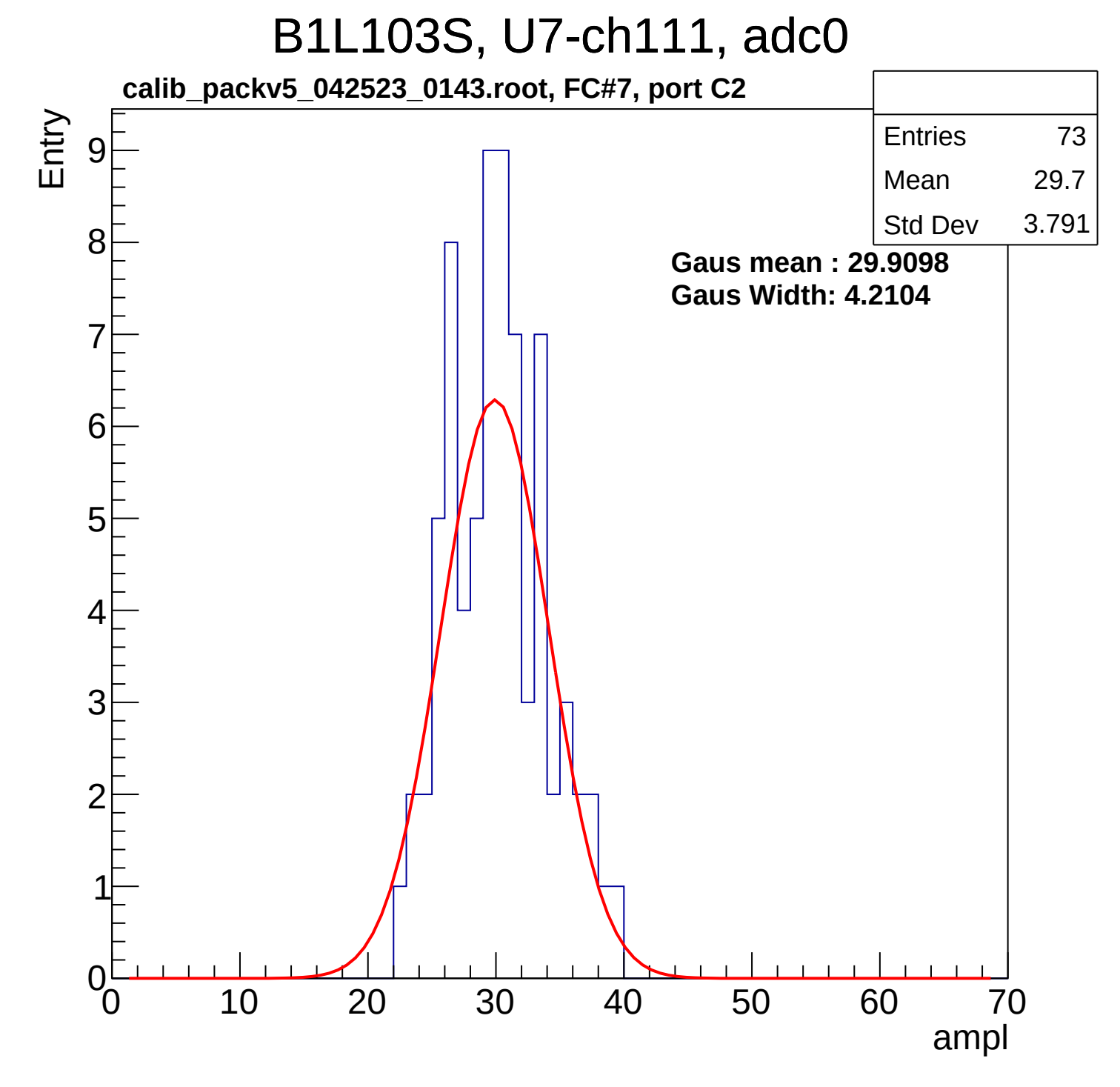
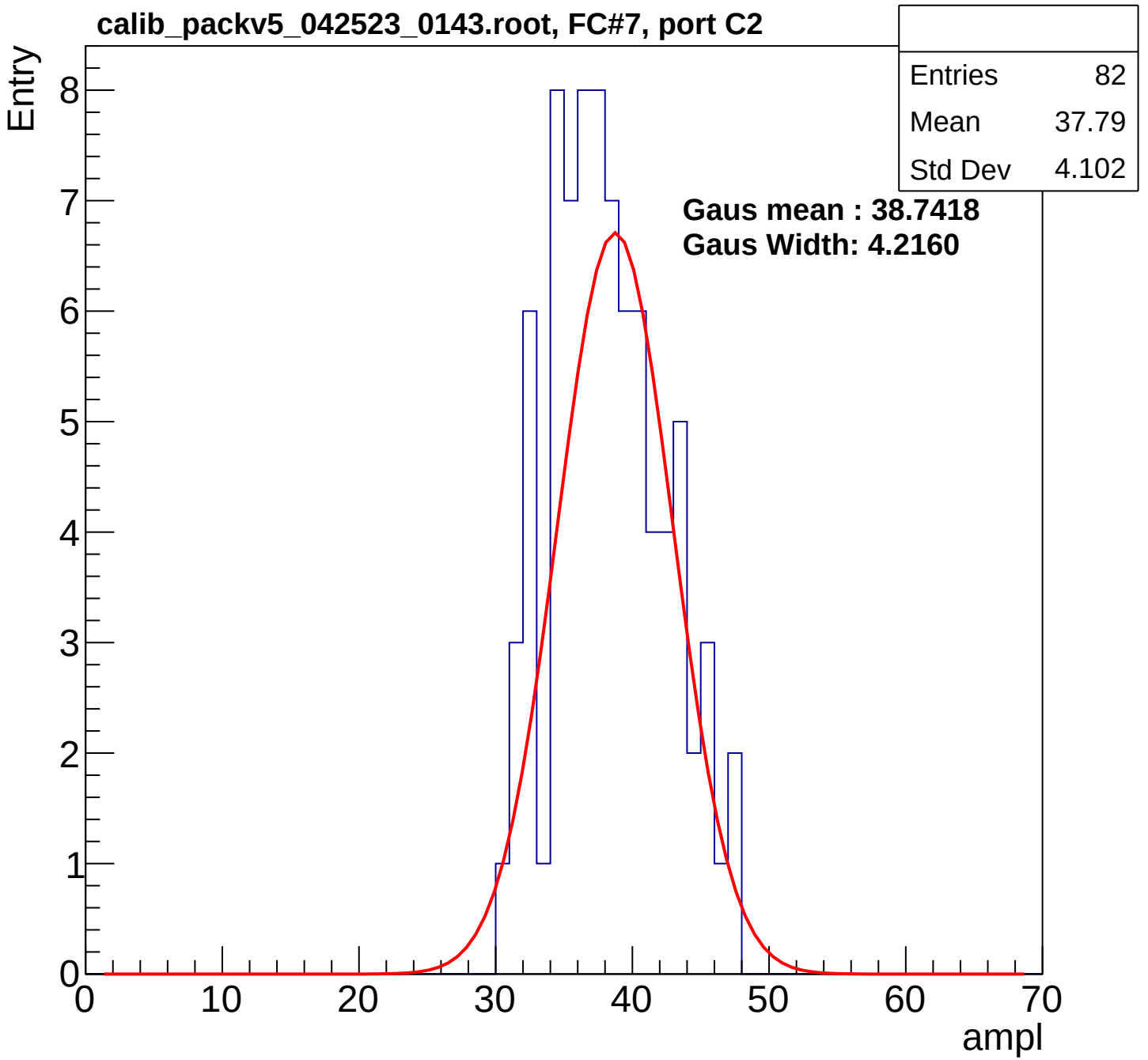
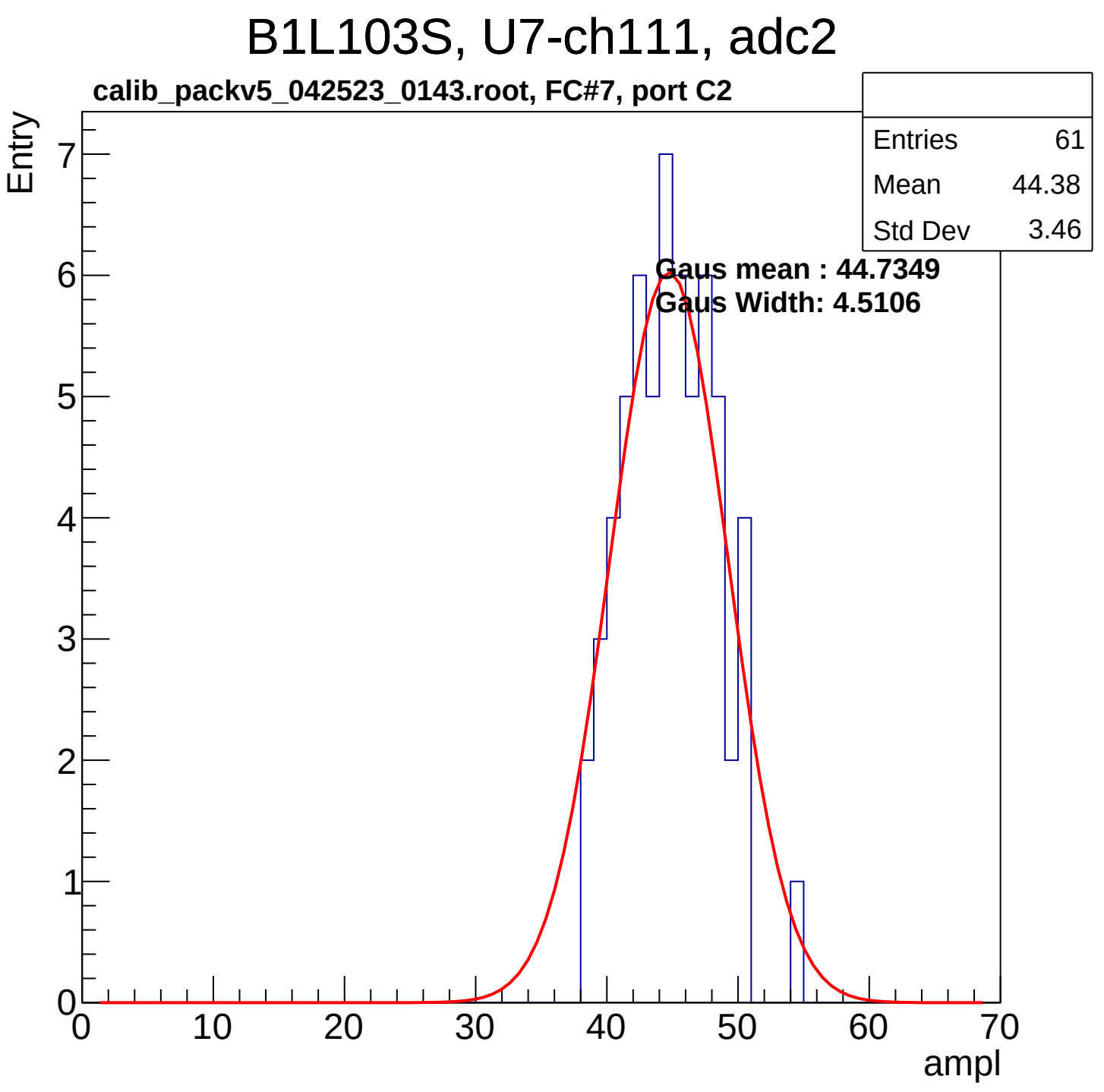
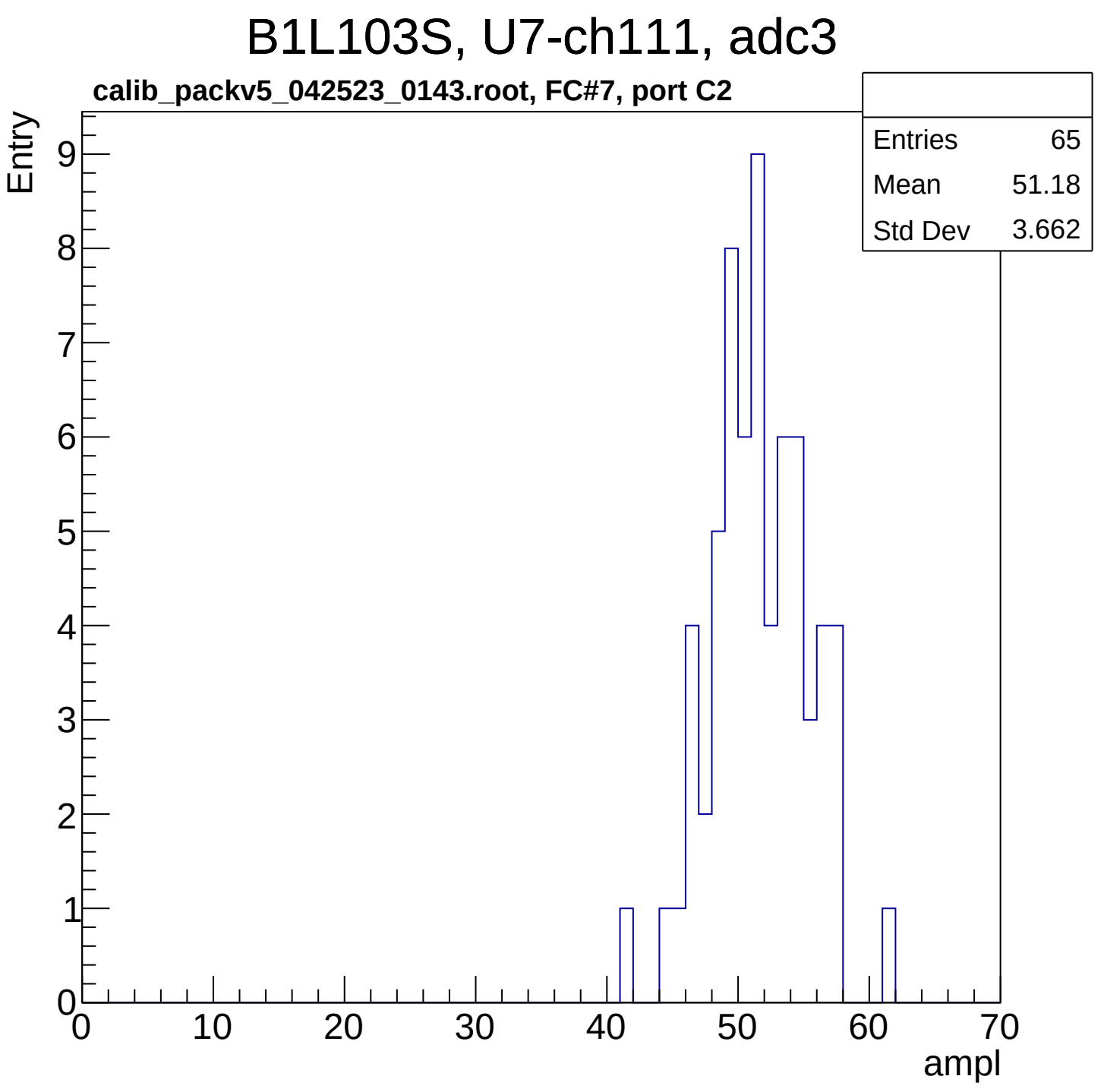
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U7-ch110, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 59
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch111, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 73
Mean 29.7
Std Dev 3.791
Gaus mean : 29.9098
Gaus Width: 4.2104
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch111, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 82
Mean 37.79
Std Dev 4.102
Gaus mean : 38.7418
Gaus Width: 4.2160
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch111, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 61
Mean 44.38
Std Dev 3.46
Gaus mean : 44.7349
Gaus Width: 4.5106
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch111, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 51.18
Std Dev 3.662
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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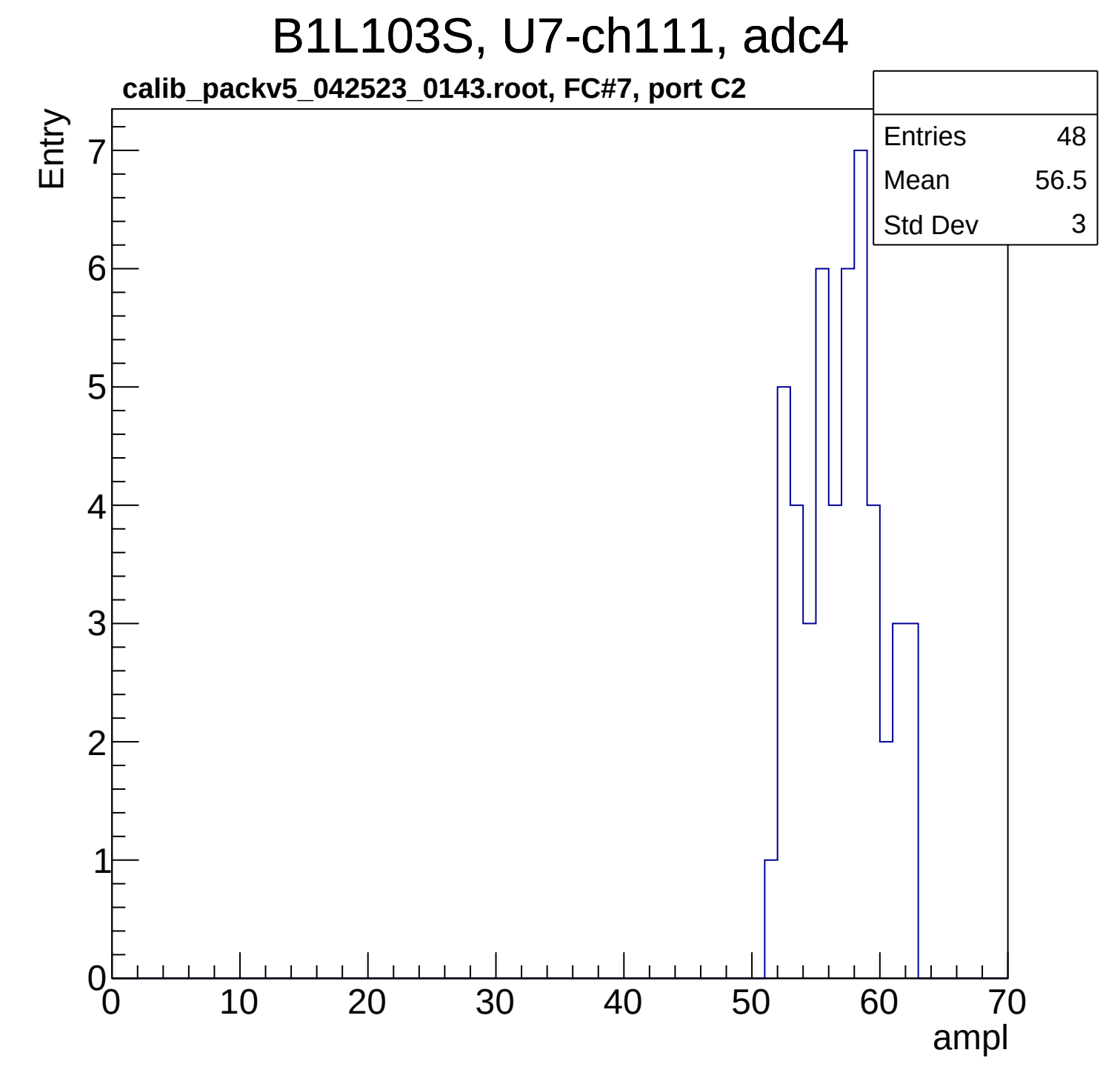
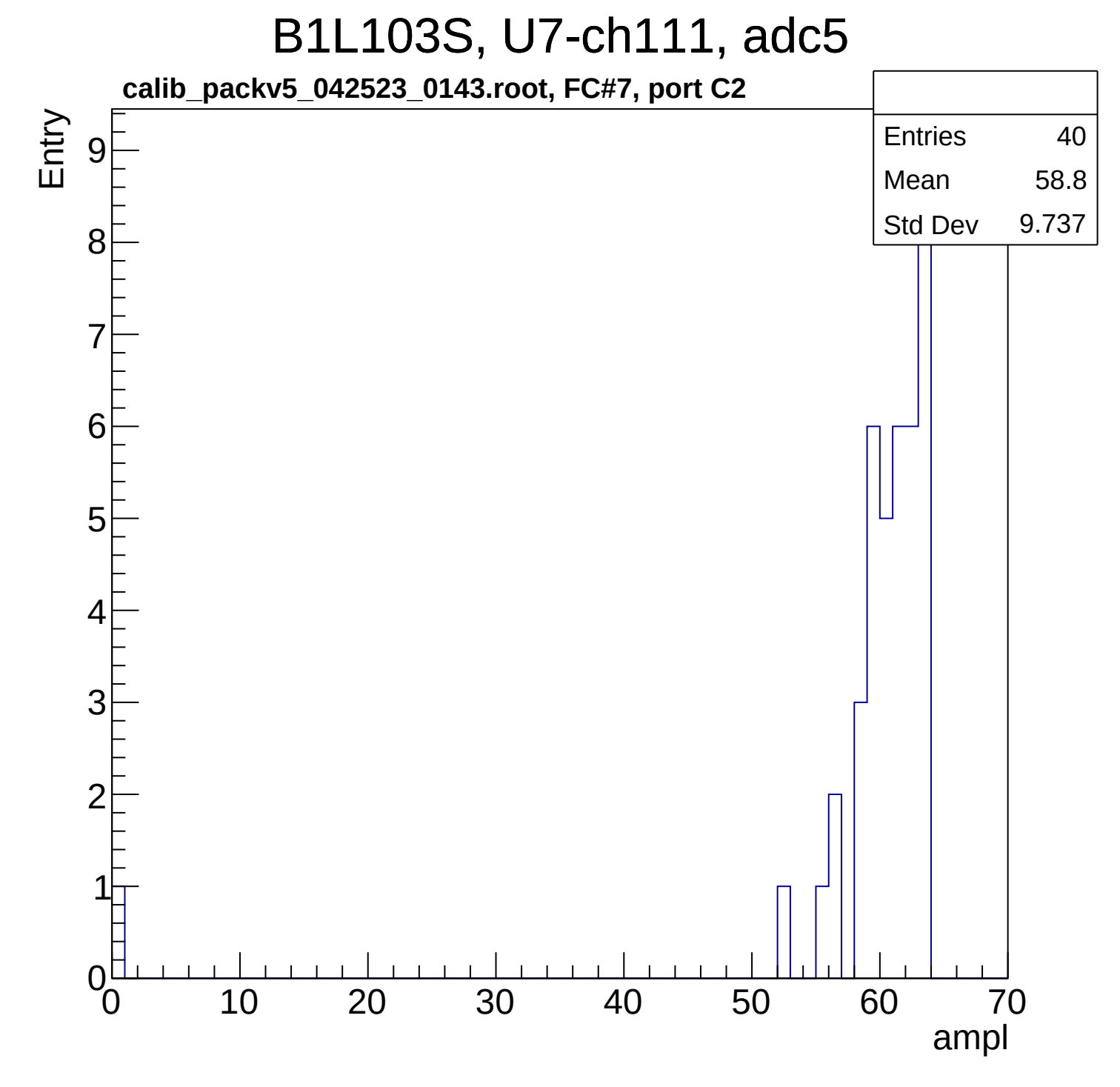

B1L103S, U7-ch111, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 48
Mean 56.5
Std Dev 3
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch111, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 40
Mean 58.8
Std Dev 9.737
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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60
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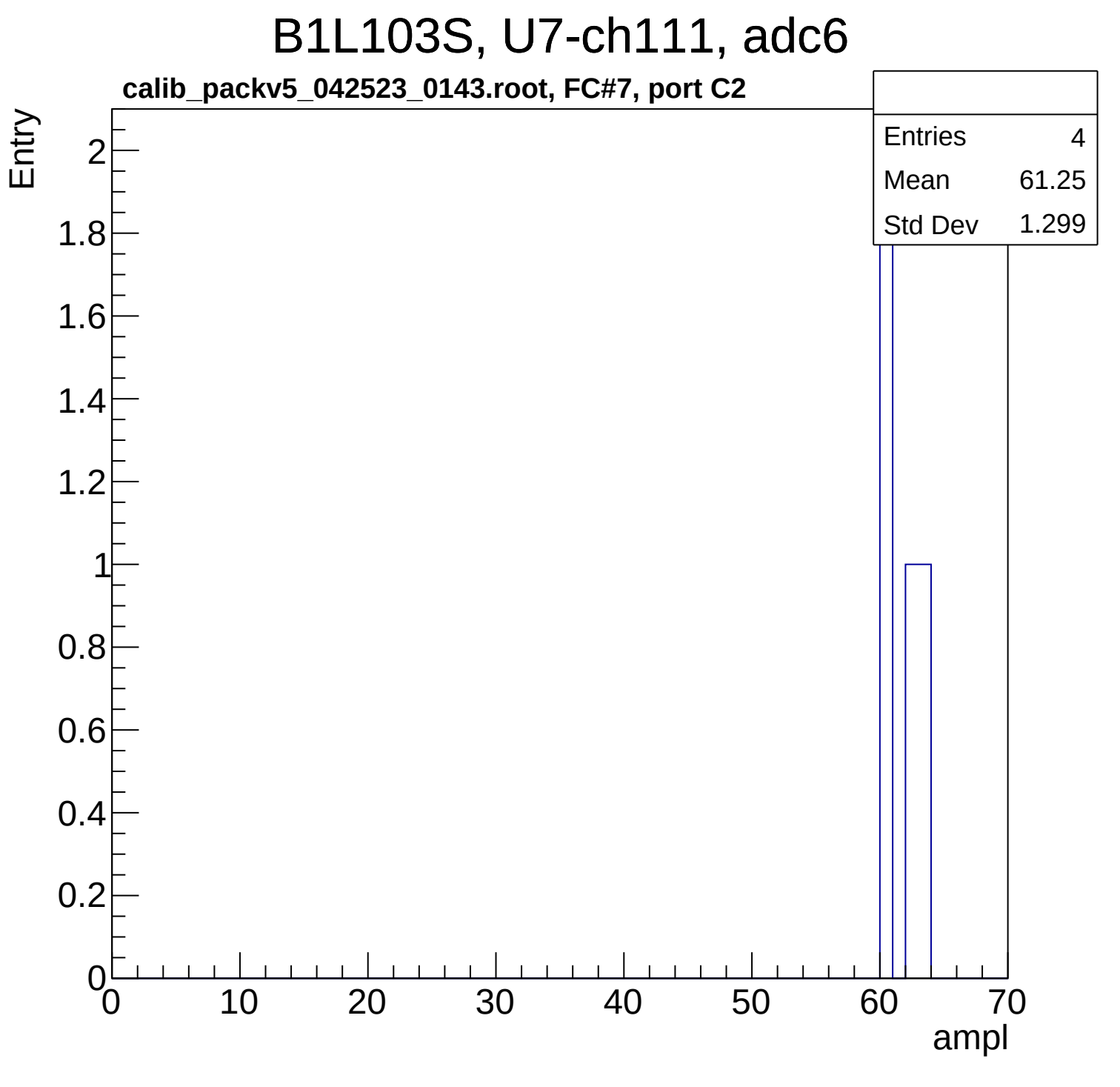
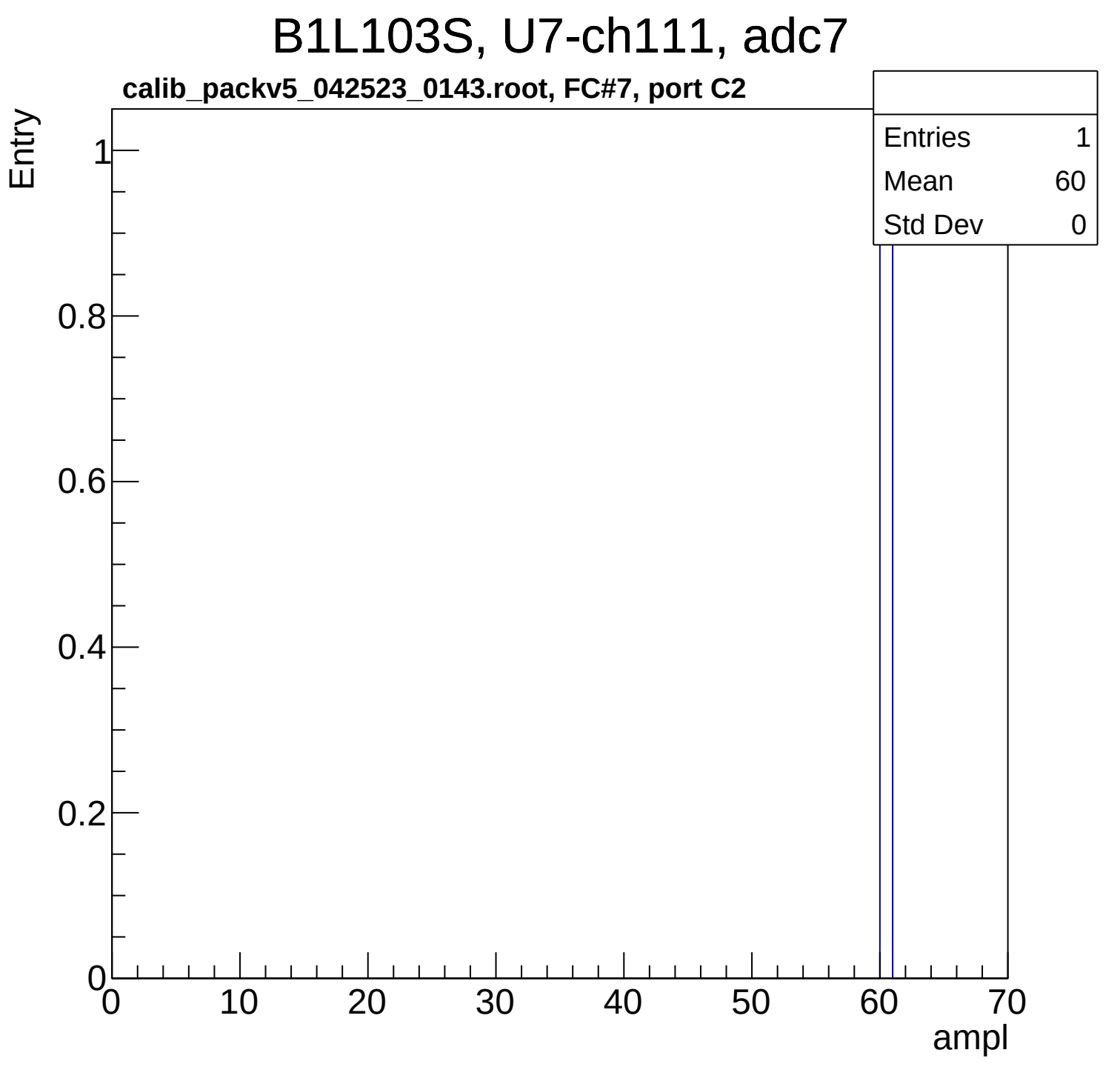

B1L103S, U7-ch111, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 4
Mean 61.25
Std Dev 1.299
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U7-ch111, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 60
Std Dev 0
Entry
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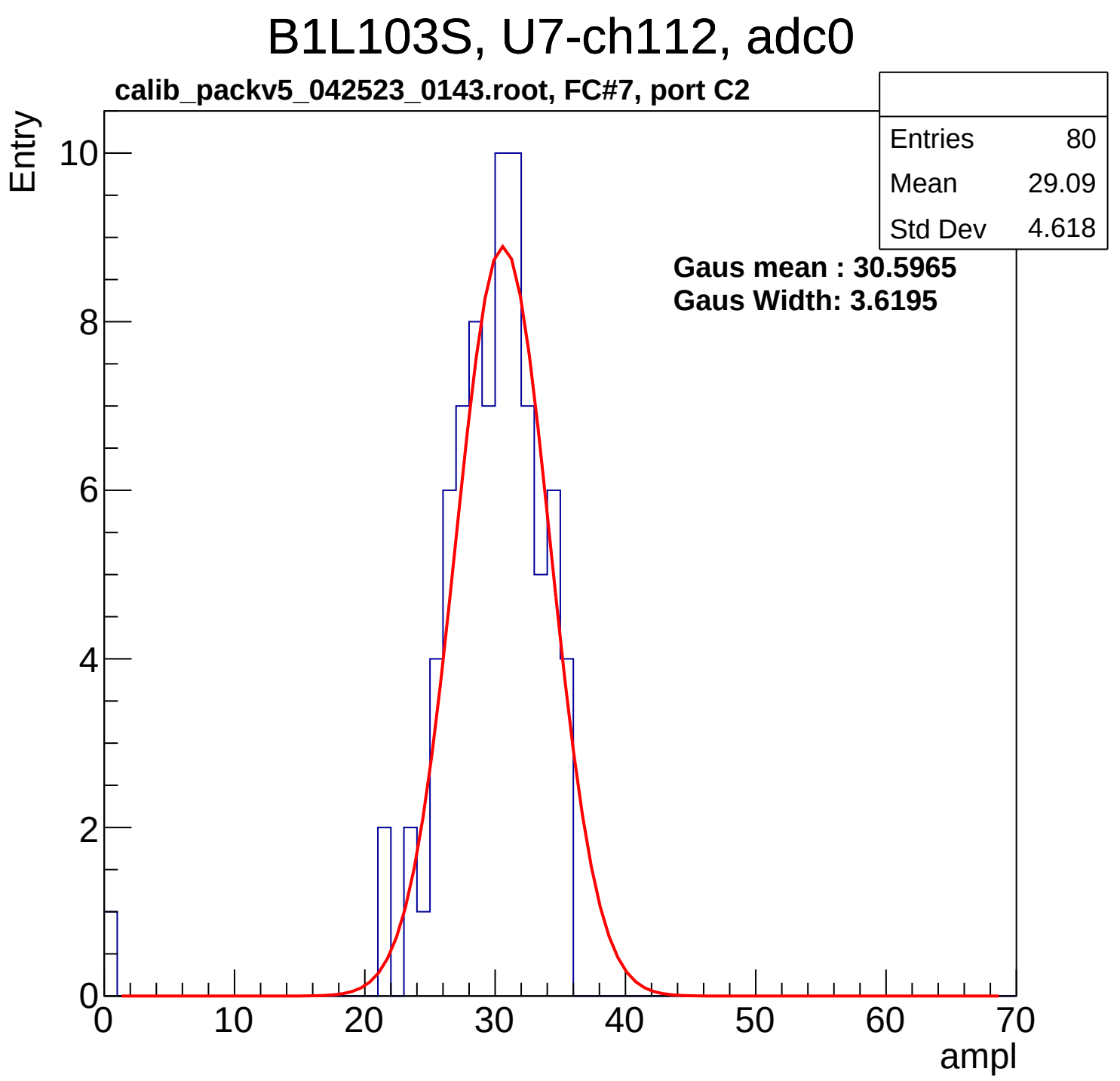
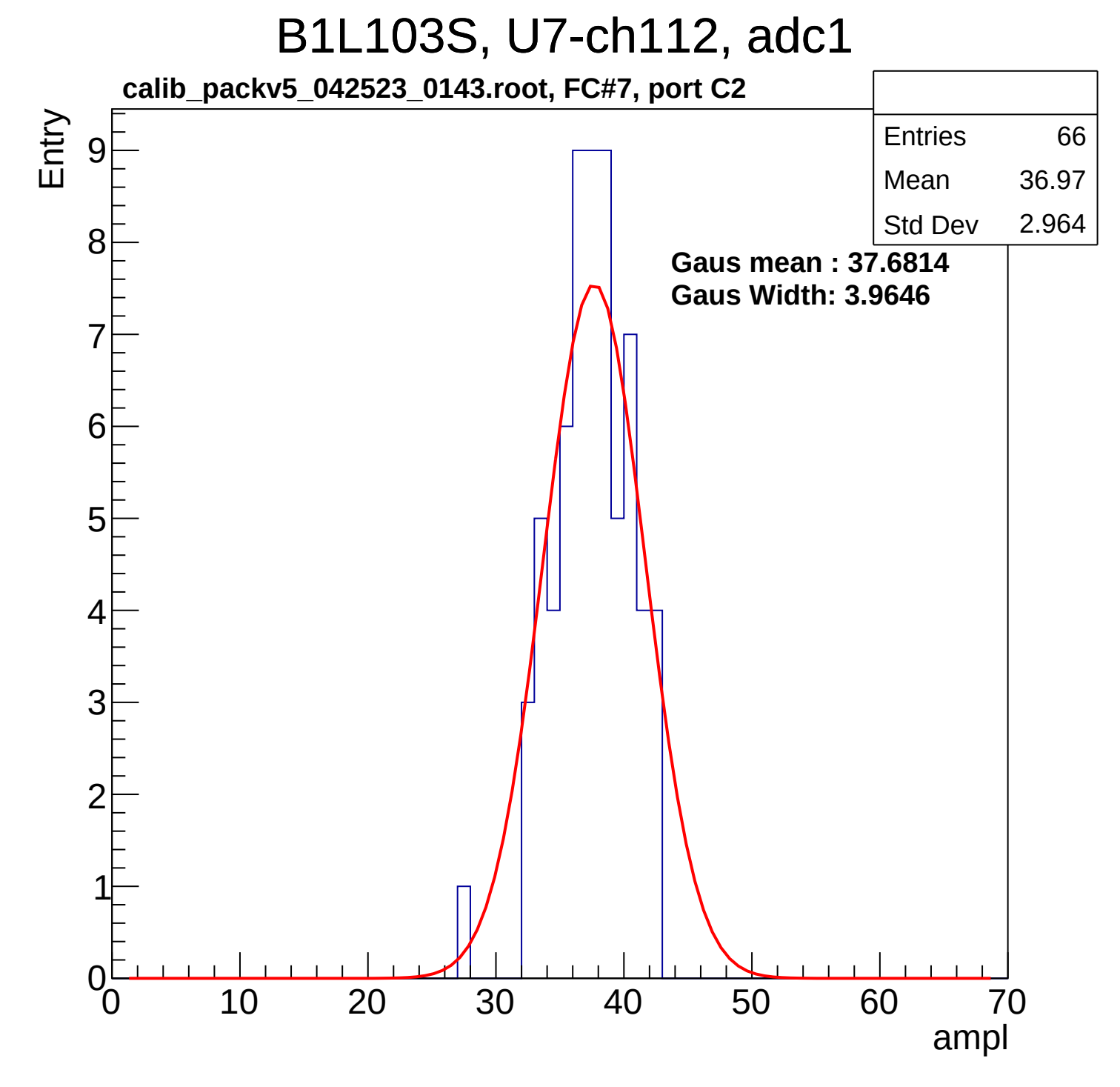
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch112, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 80
Mean 29.09
Std Dev 4.618
Gaus mean : 30.5965
Gaus Width: 3.6195
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch112, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 36.97
Std Dev 2.964
Gaus mean : 37.6814
Gaus Width: 3.9646
Entry
ampl
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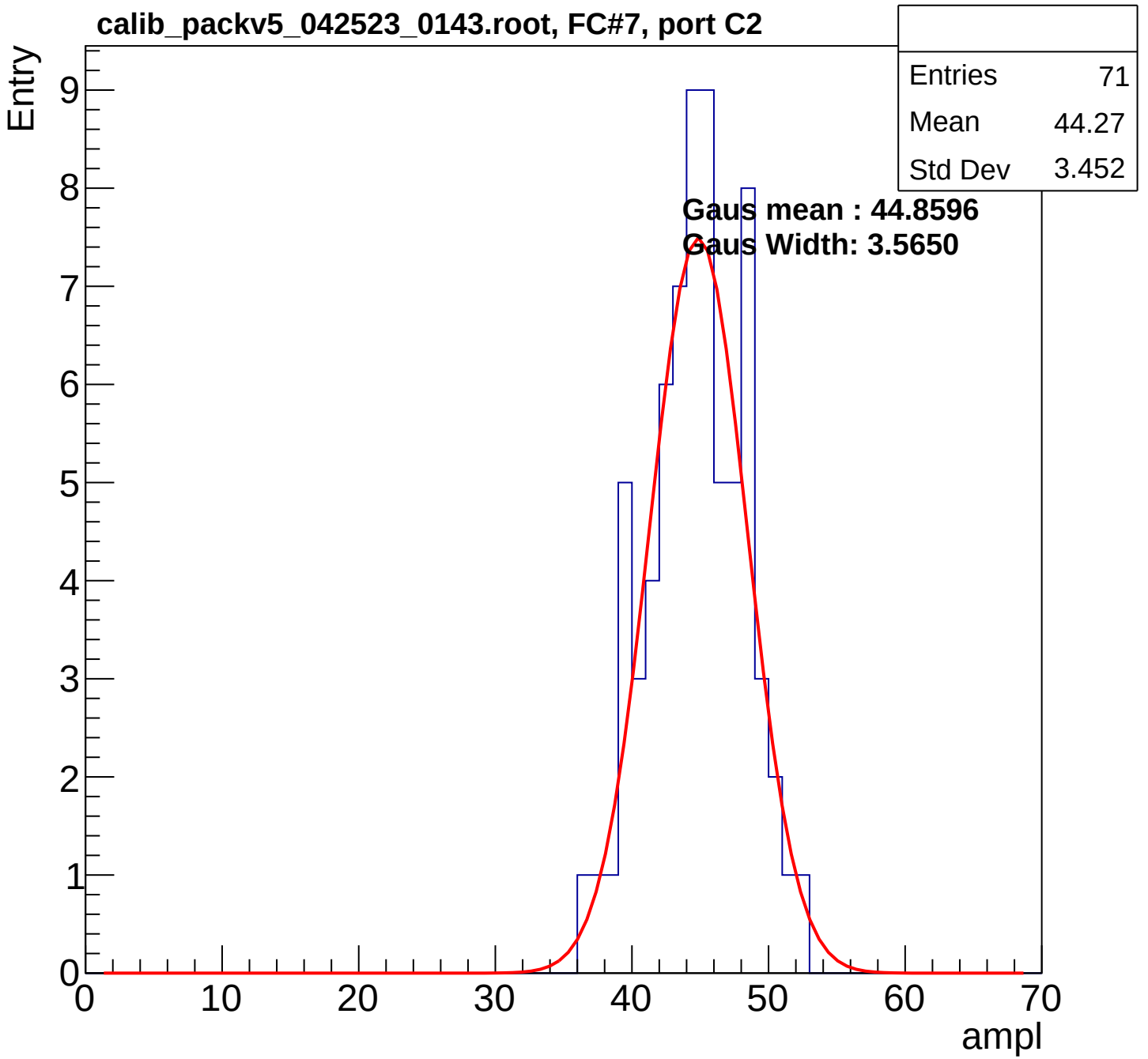
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch112, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 71
Mean 44.27
Std Dev 3.452
Gaus mean : 44.8596
Gaus Width: 3.5650
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
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40
50
60
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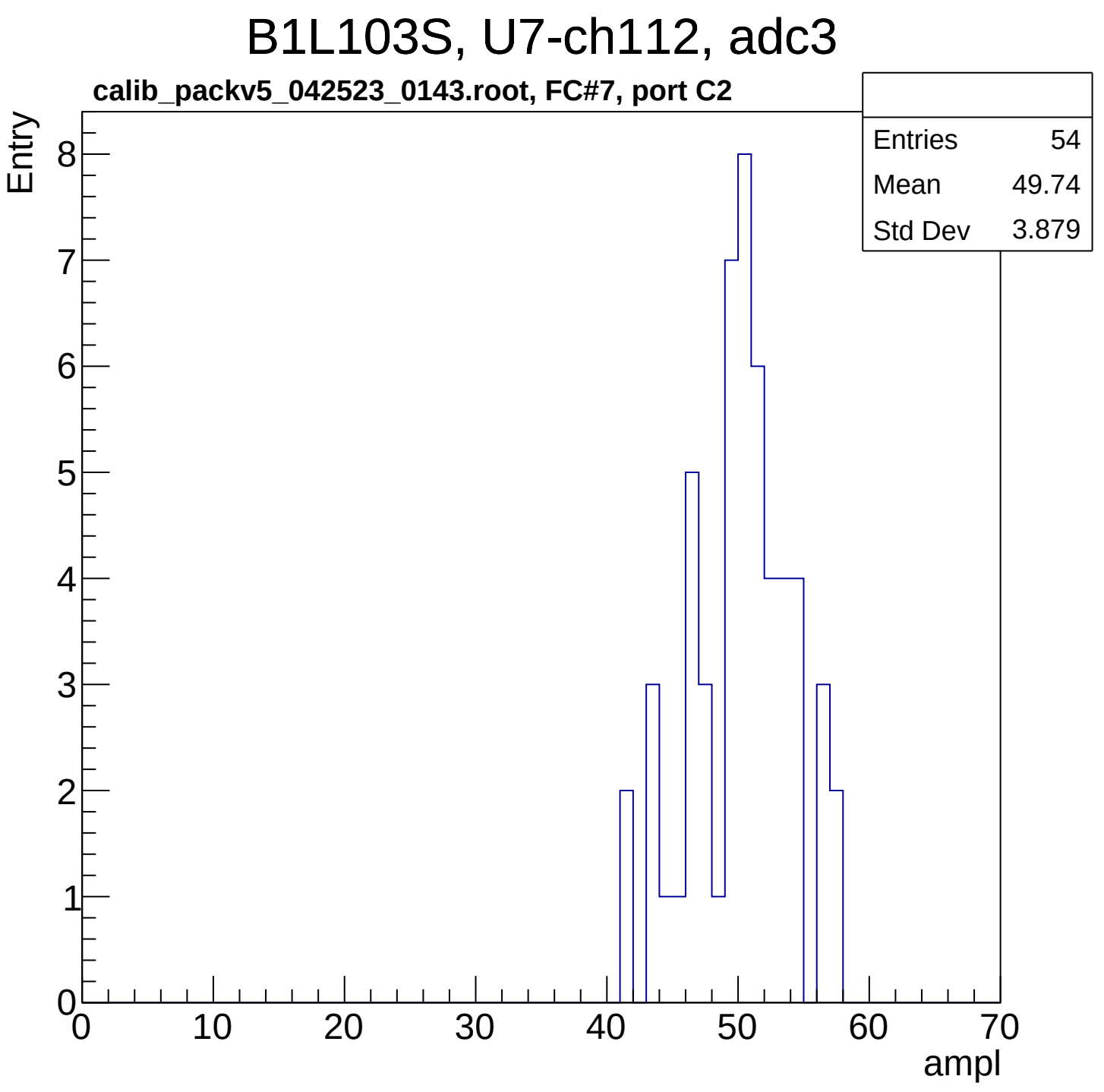
B1L103S, U7-ch112, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 54
Mean 49.74
Std Dev 3.879
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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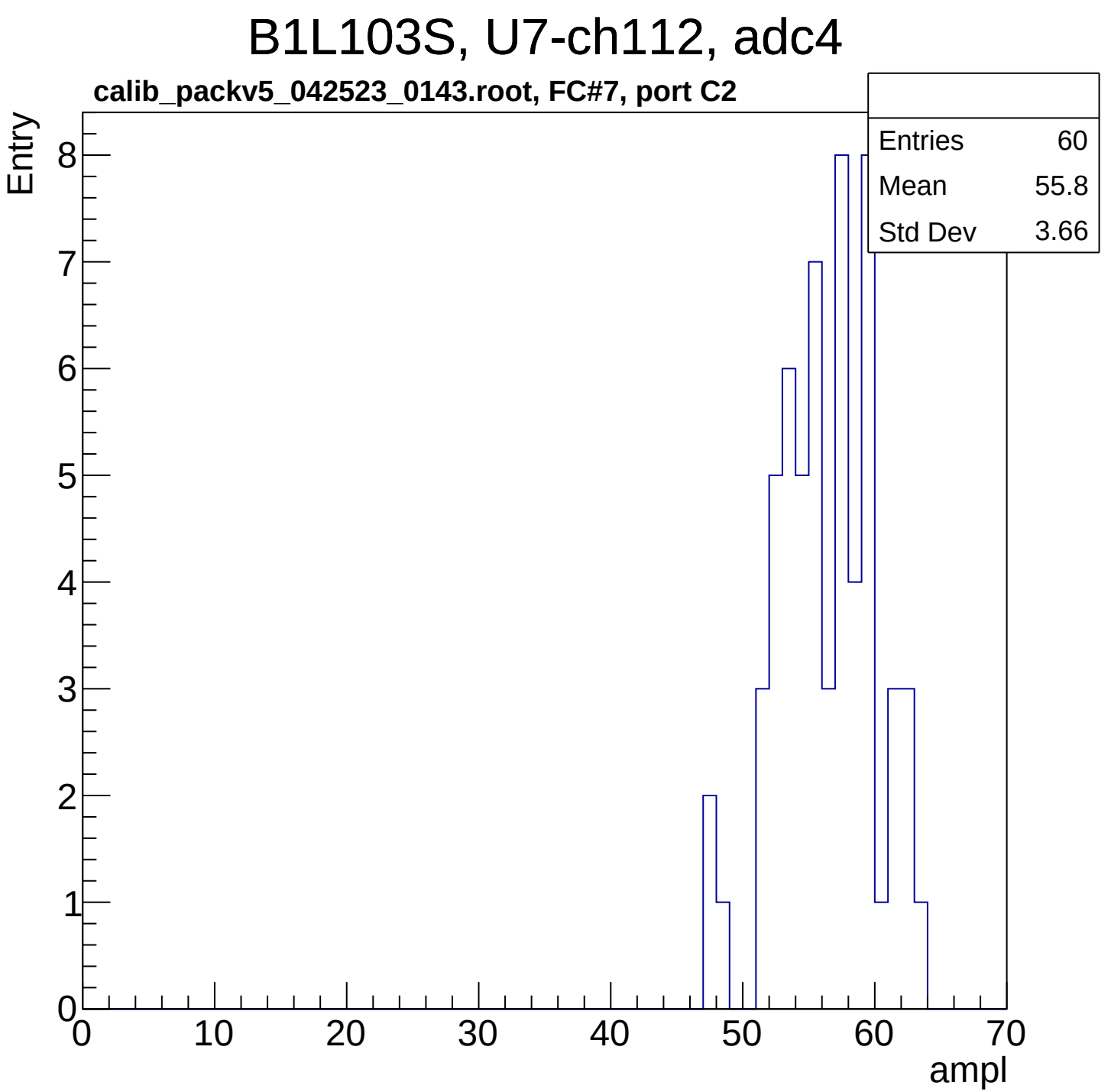
B1L103S, U7-ch112, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 60
Mean 55.8
Std Dev 3.66
Entry
ampl
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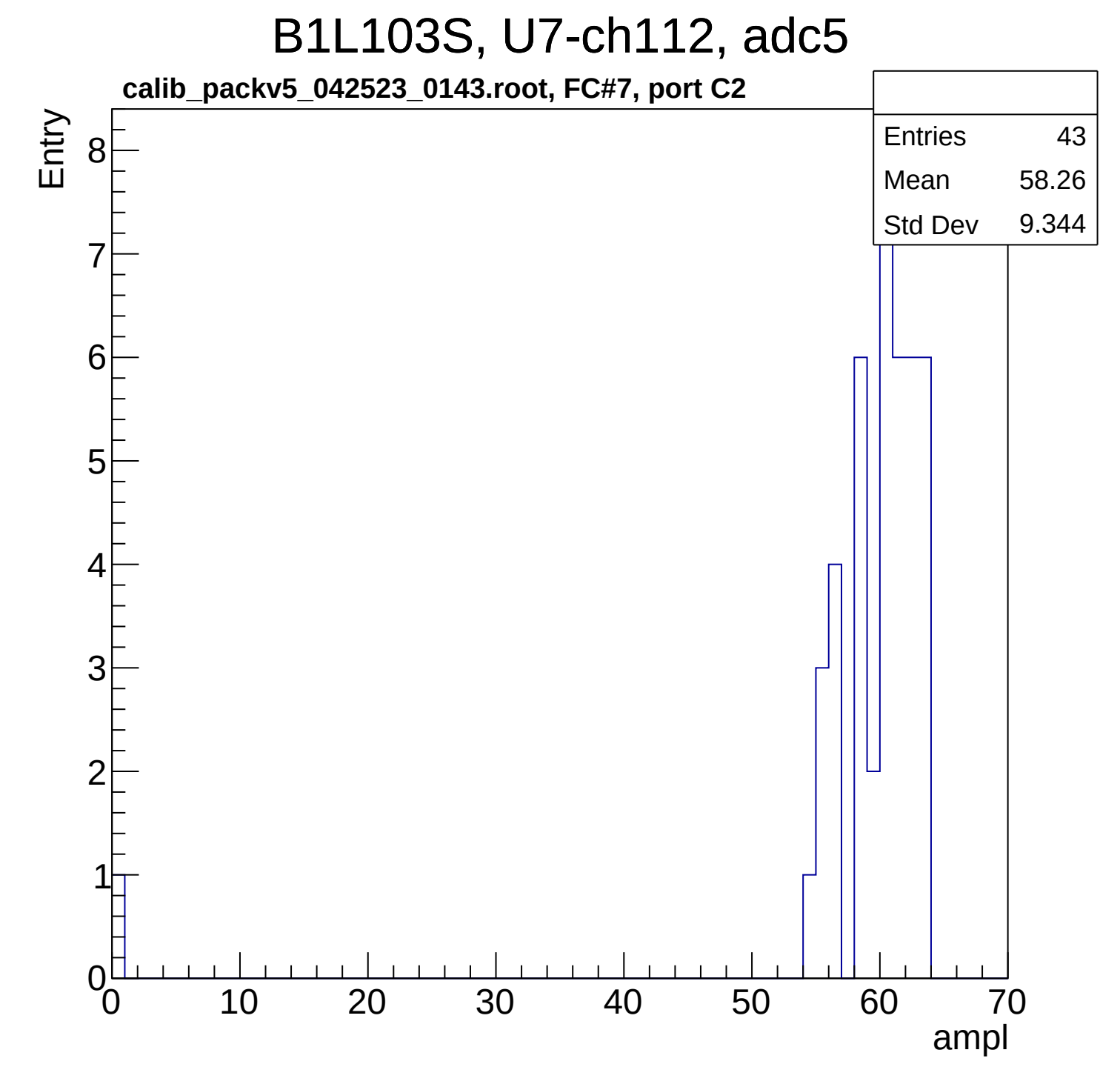
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch112, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 43
Mean 58.26
Std Dev 9.344
Entry
ampl
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2
3
4
5
6
7
8
0
10
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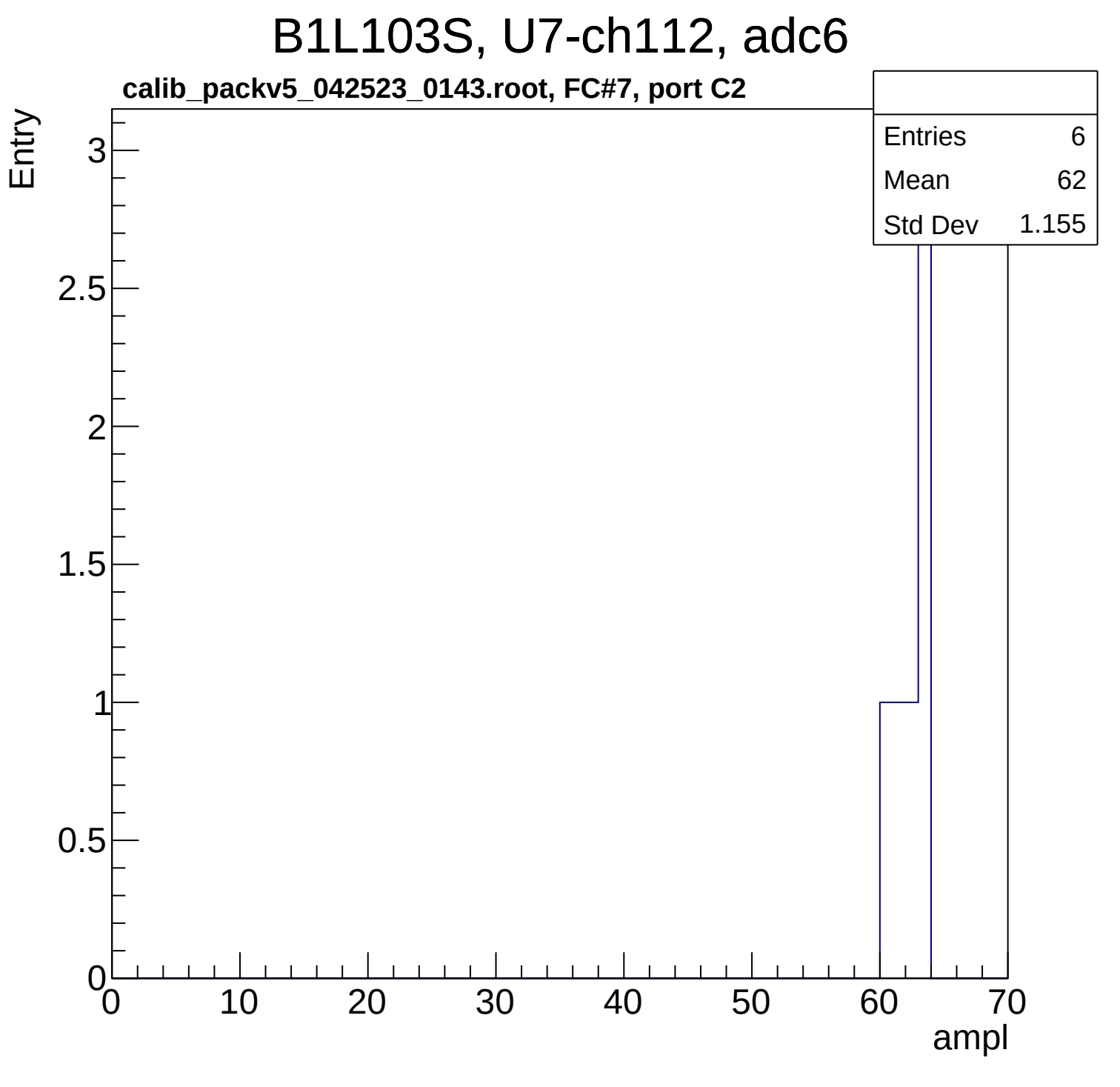
B1L103S, U7-ch112, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 6
Mean 62
Std Dev 1.155
Entry
ampl
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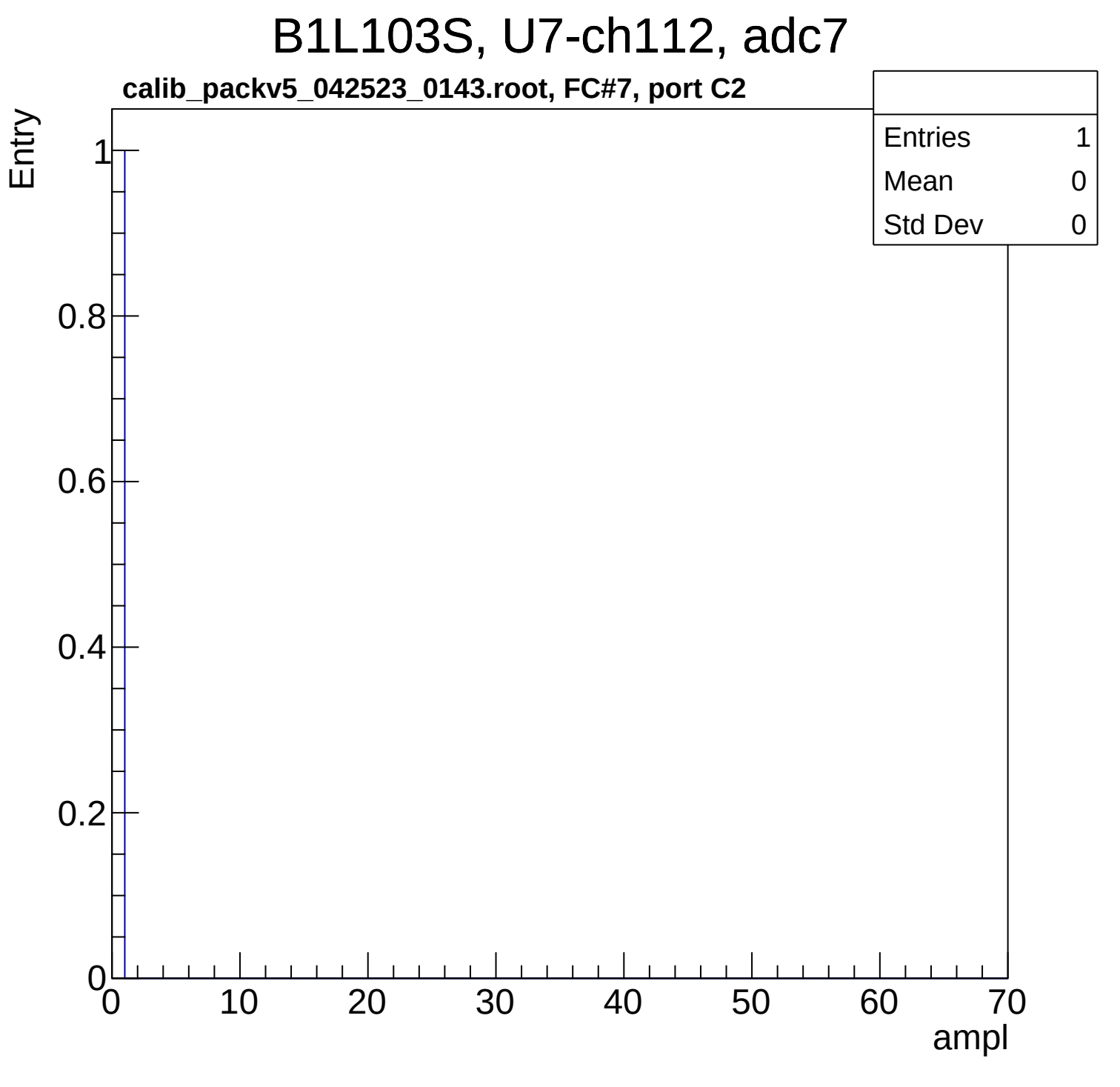
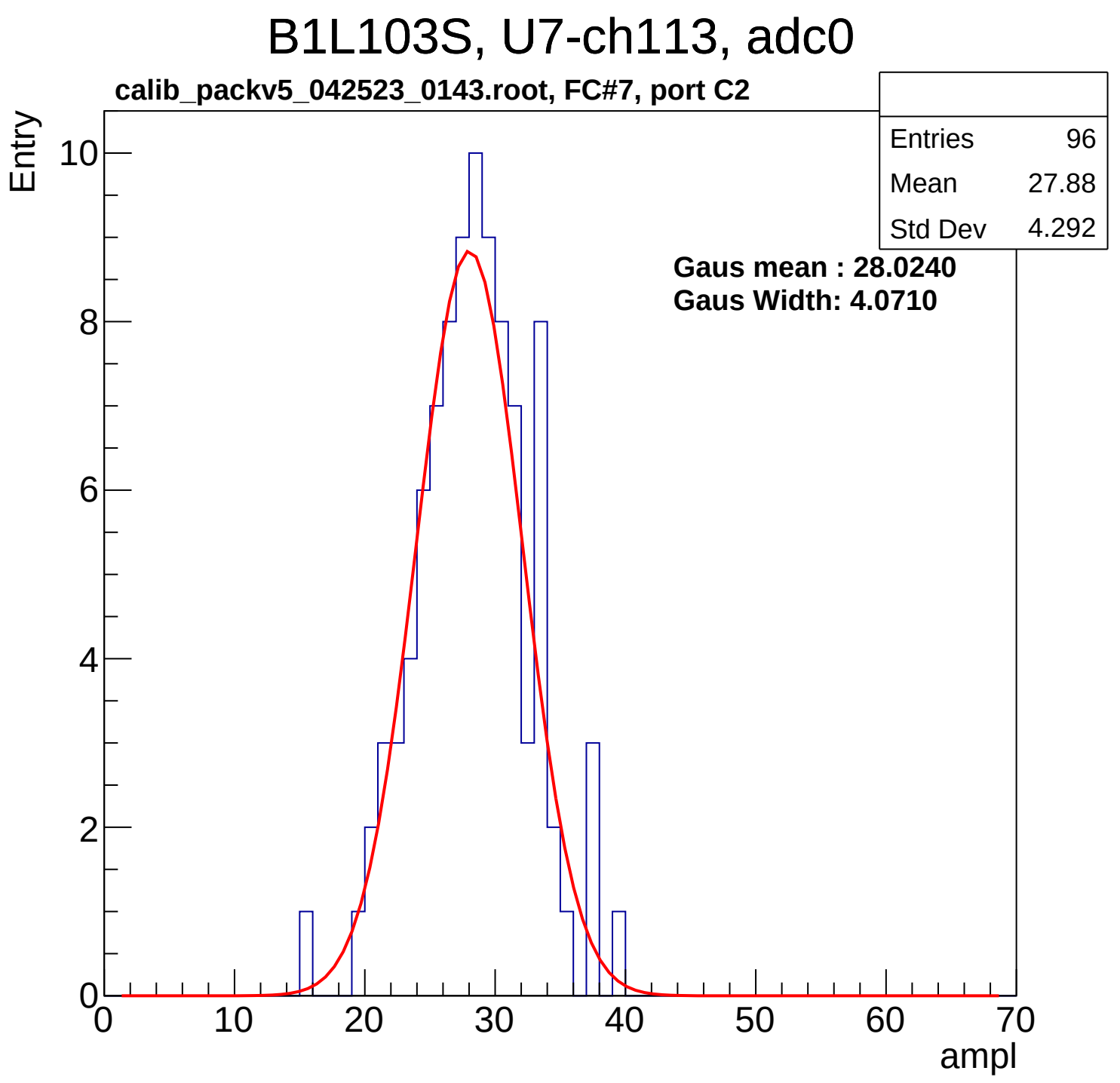
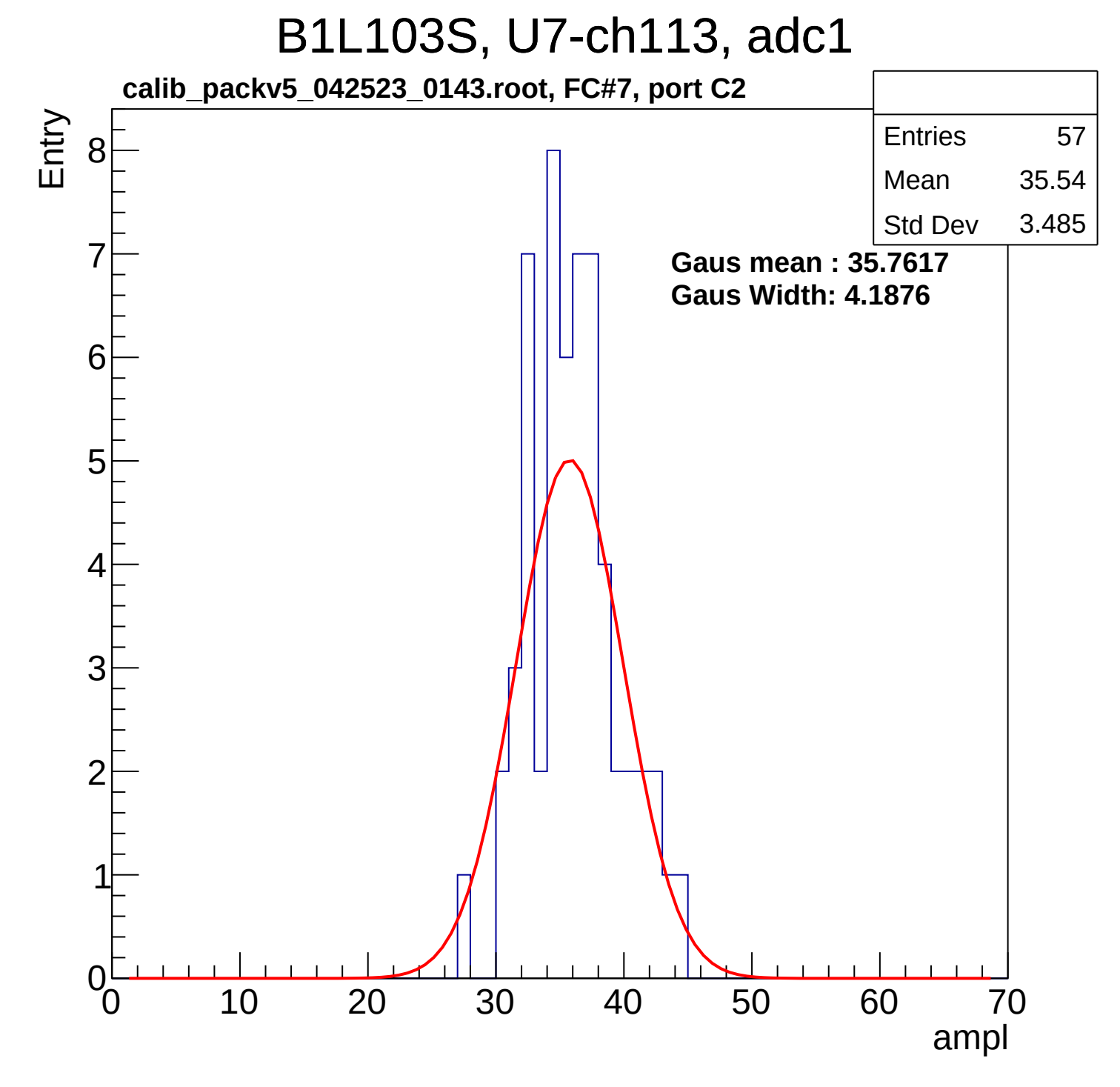
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U7-ch112, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch113, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 96
Mean 27.88
Std Dev 4.292
Gaus mean : 28.0240
Gaus Width: 4.0710
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch113, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 35.54
Std Dev 3.485
Gaus mean : 35.7617
Gaus Width: 4.1876
Entry
ampl
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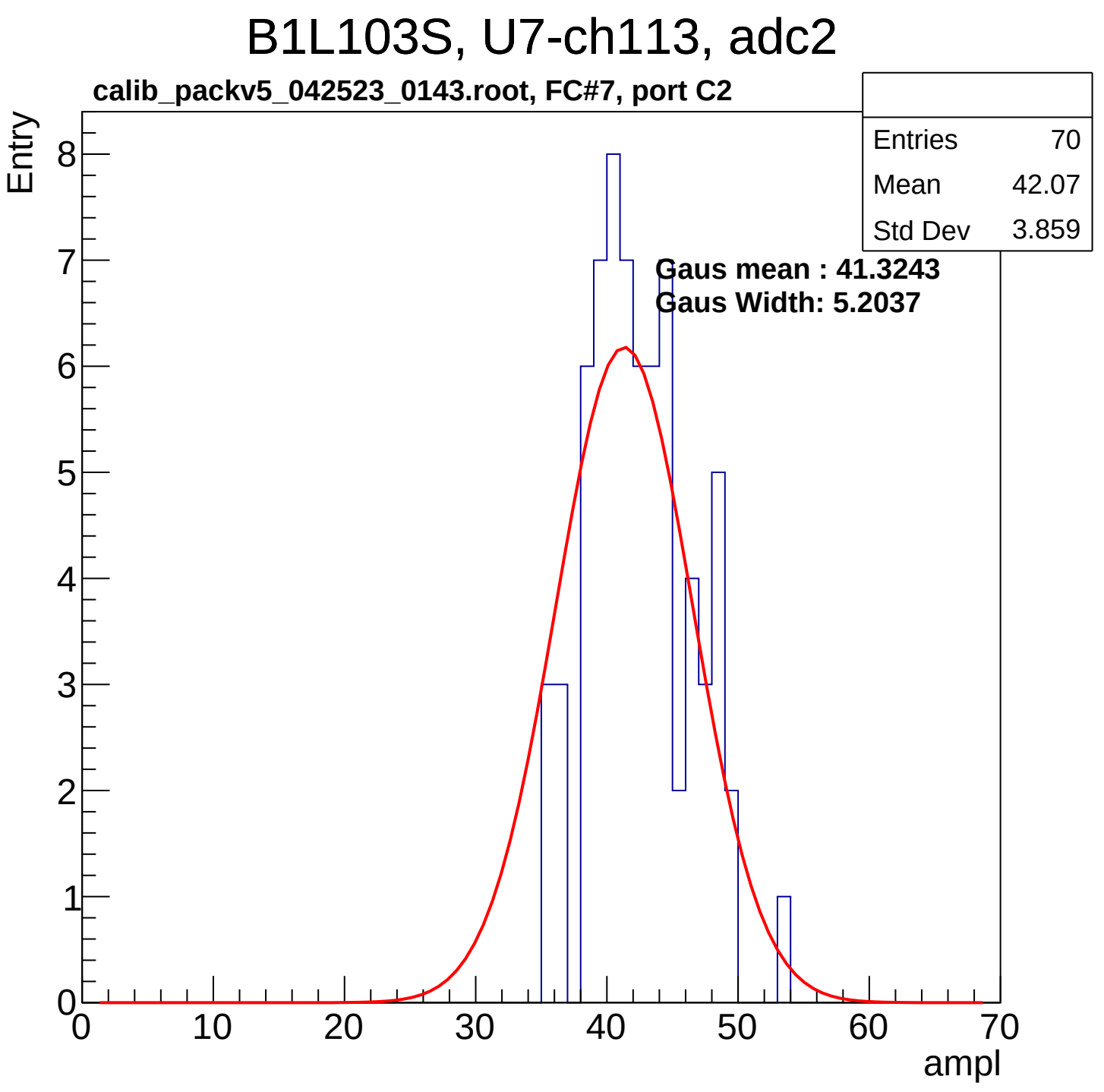
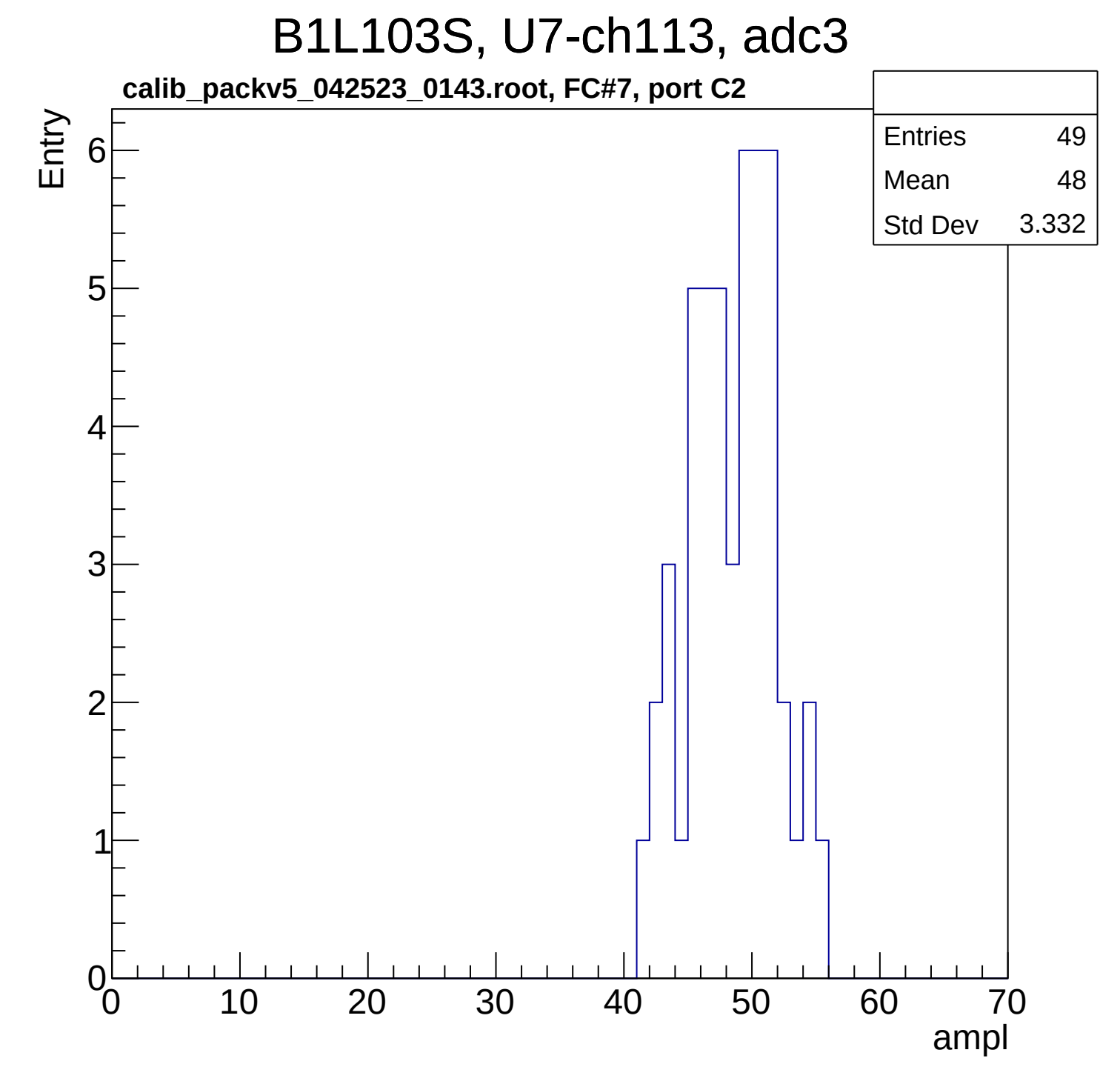
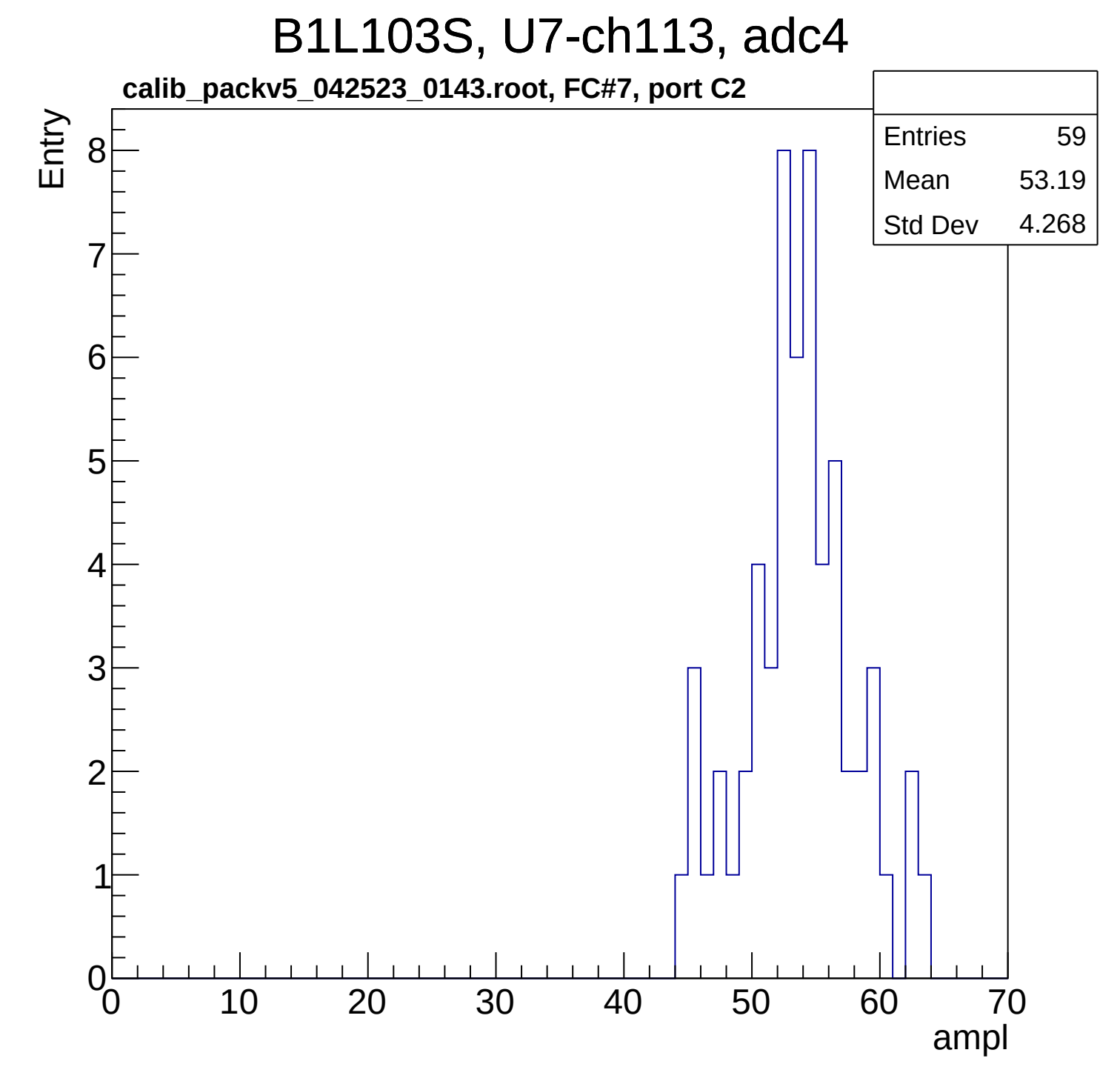
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch113, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 42.07
Std Dev 3.859
Gaus mean : 41.3243
Gaus Width: 5.2037
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch113, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 49
Mean 48
Std Dev 3.332
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U7-ch113, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 53.19
Std Dev 4.268
Entry
ampl
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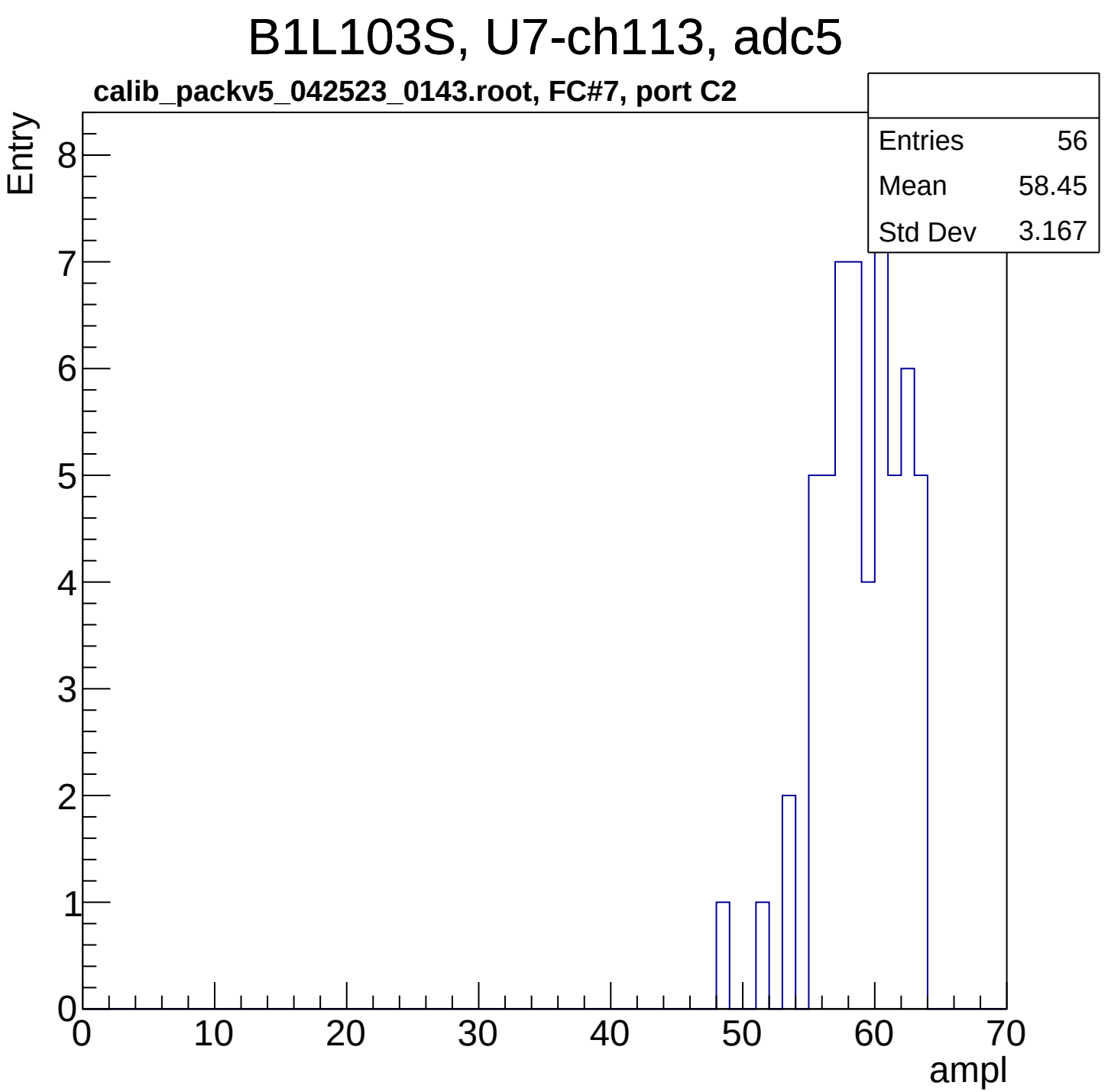
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch113, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 58.45
Std Dev 3.167
Entry
ampl
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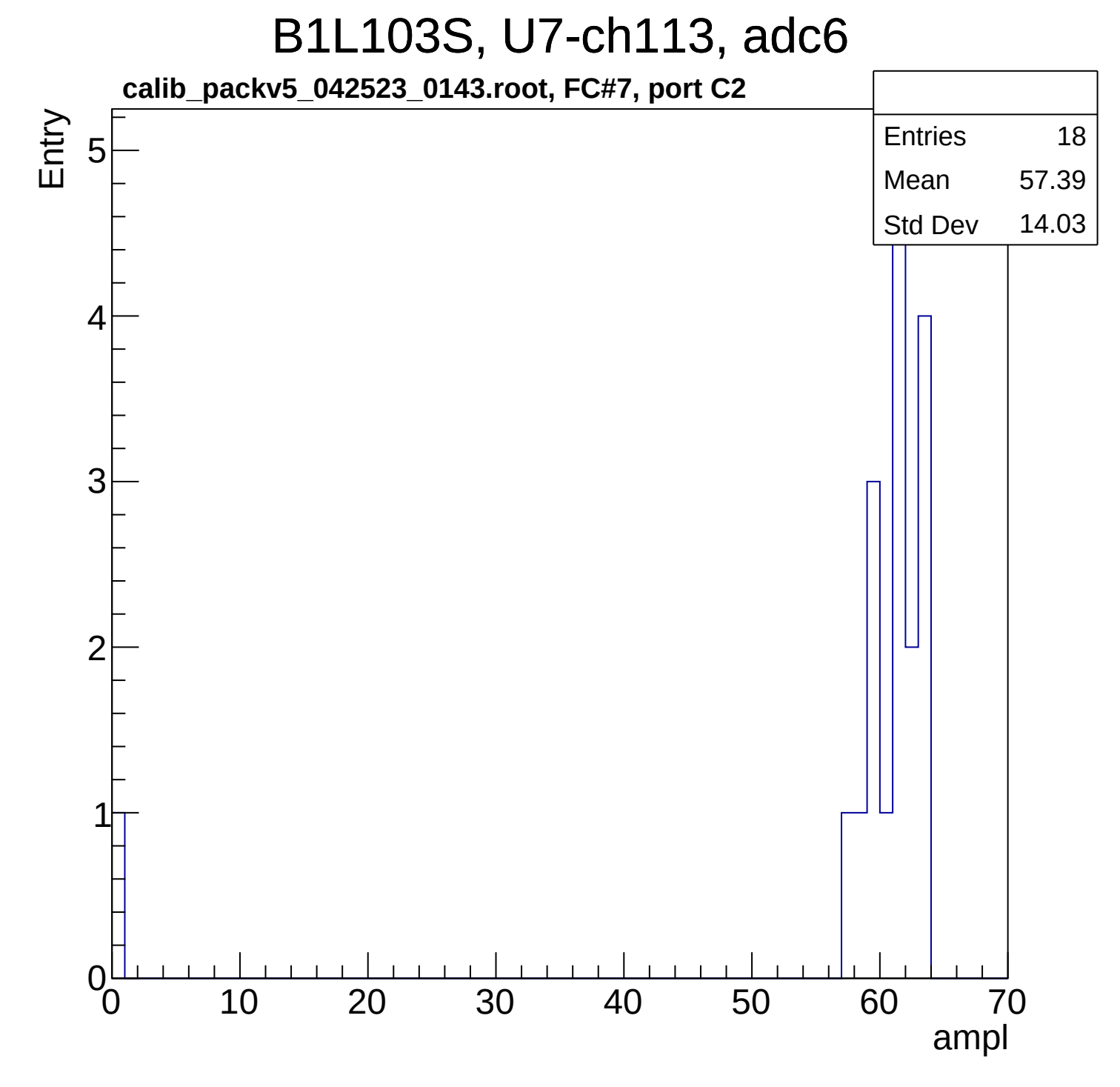
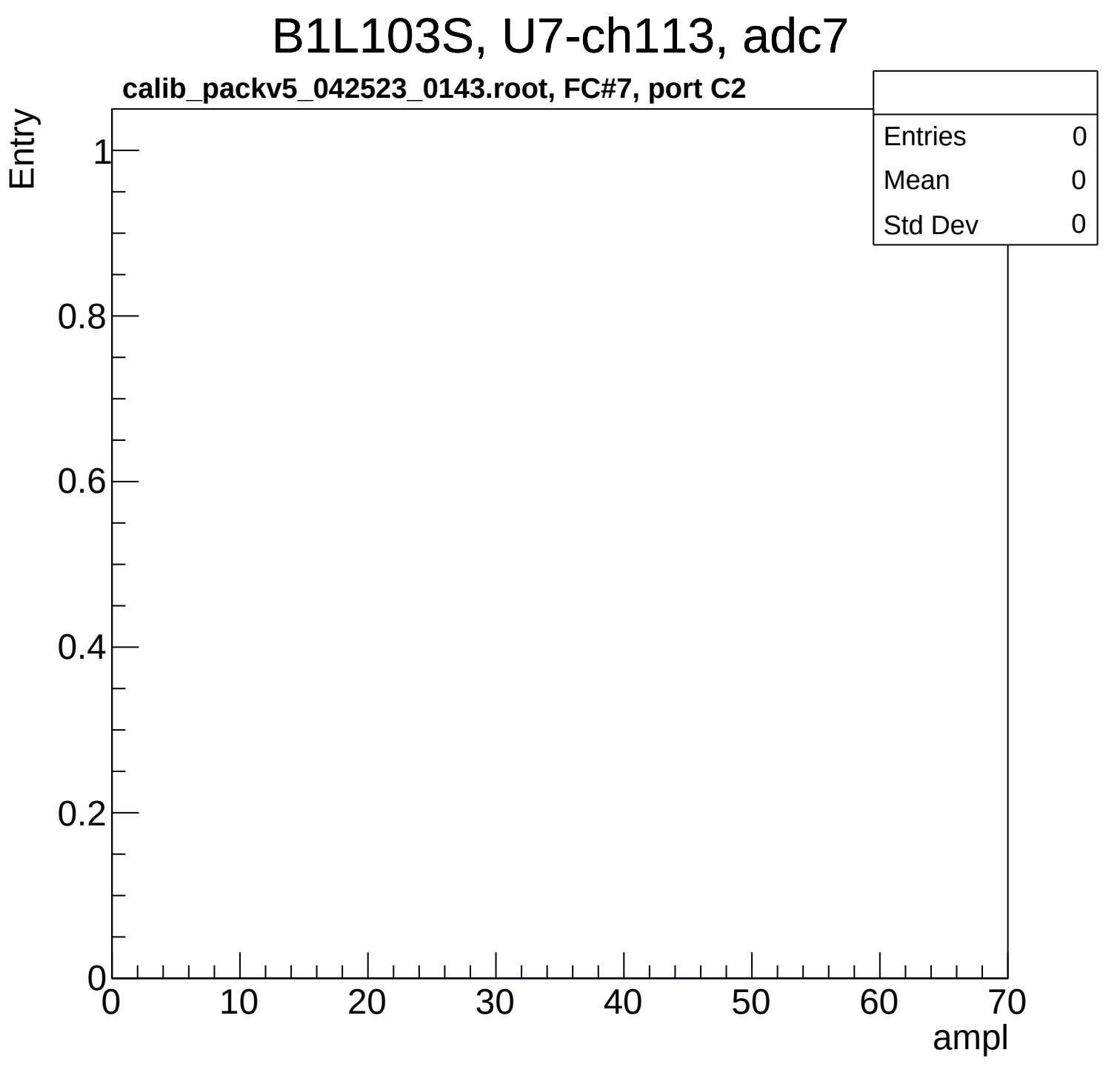
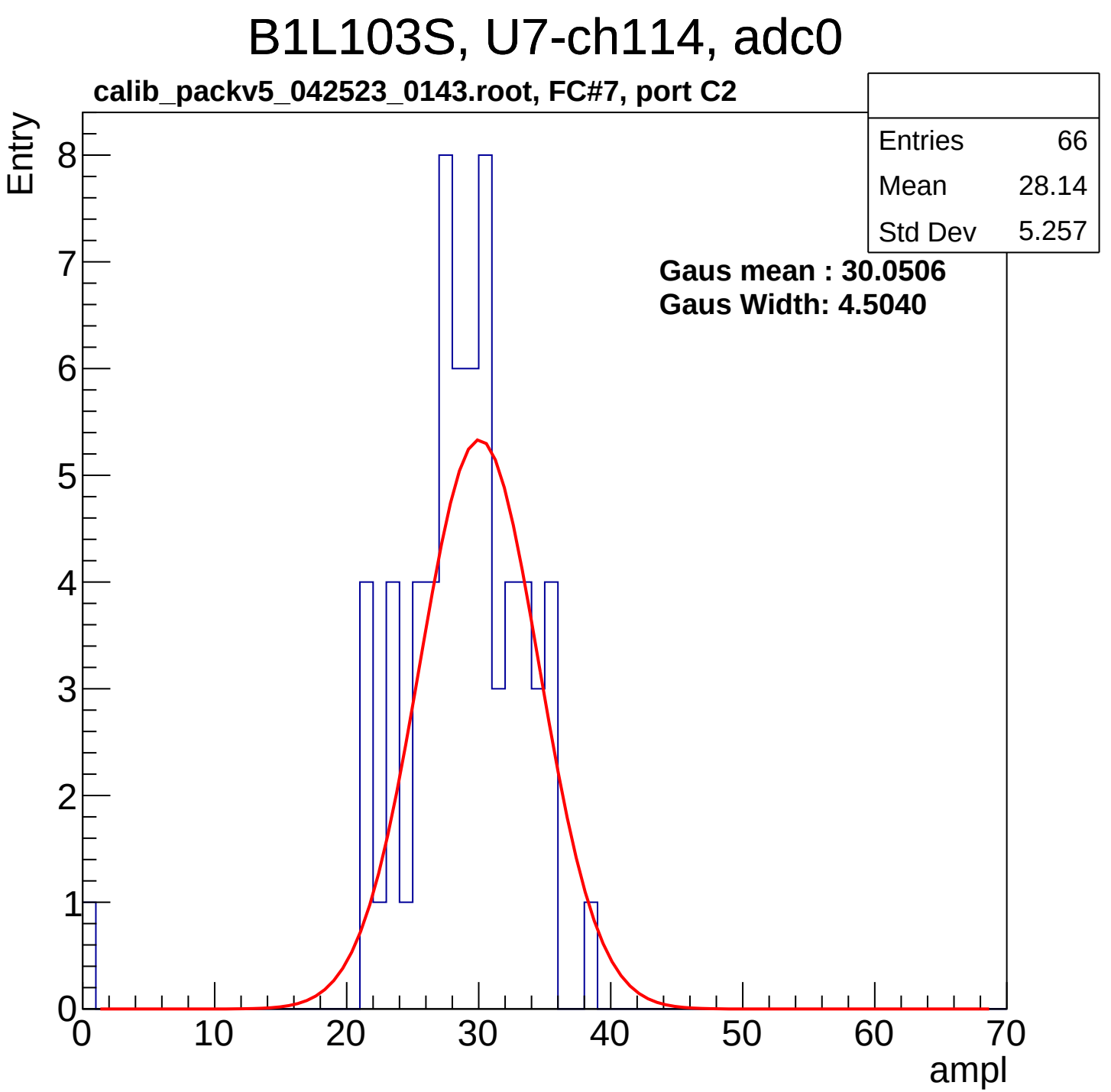
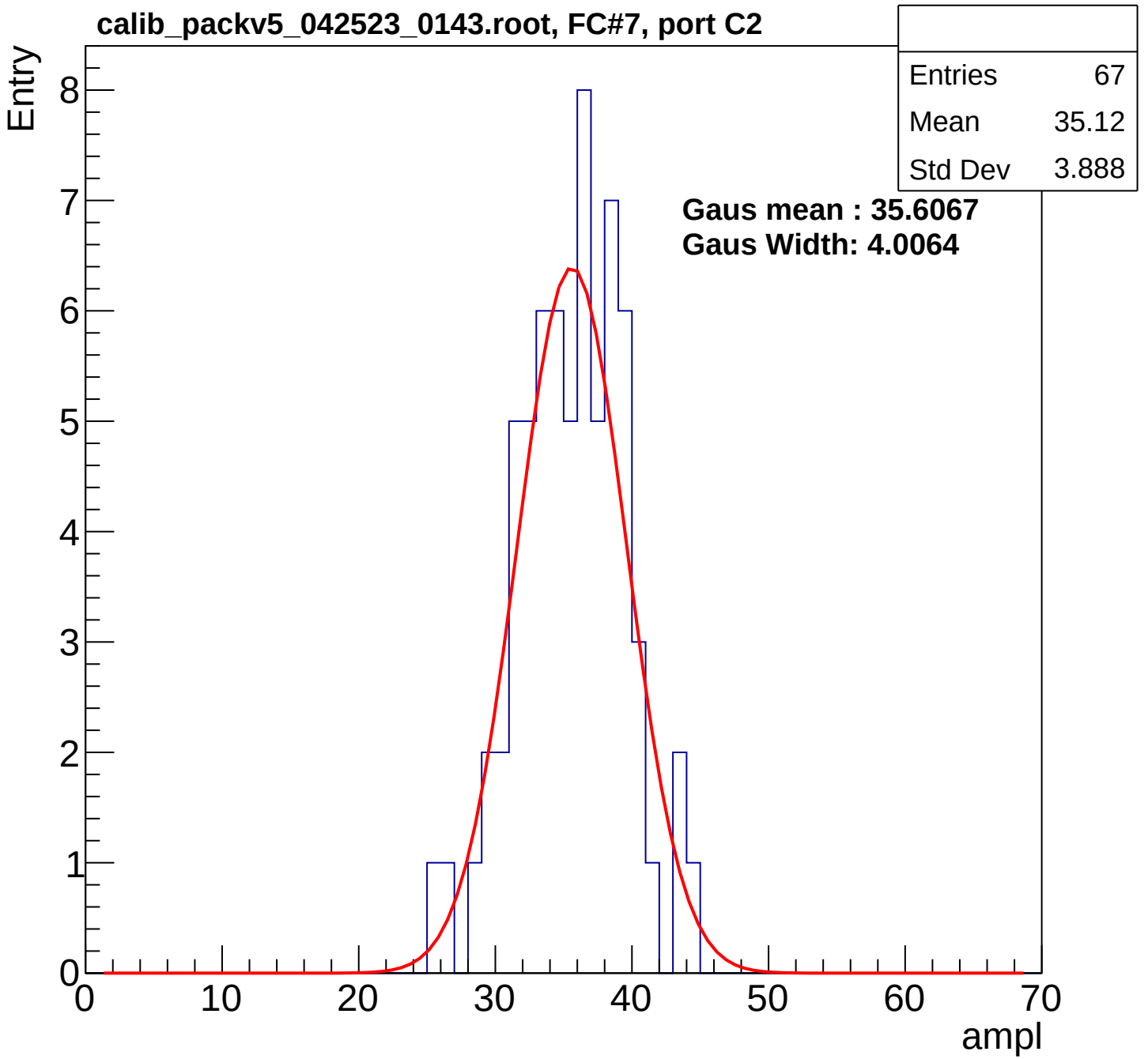
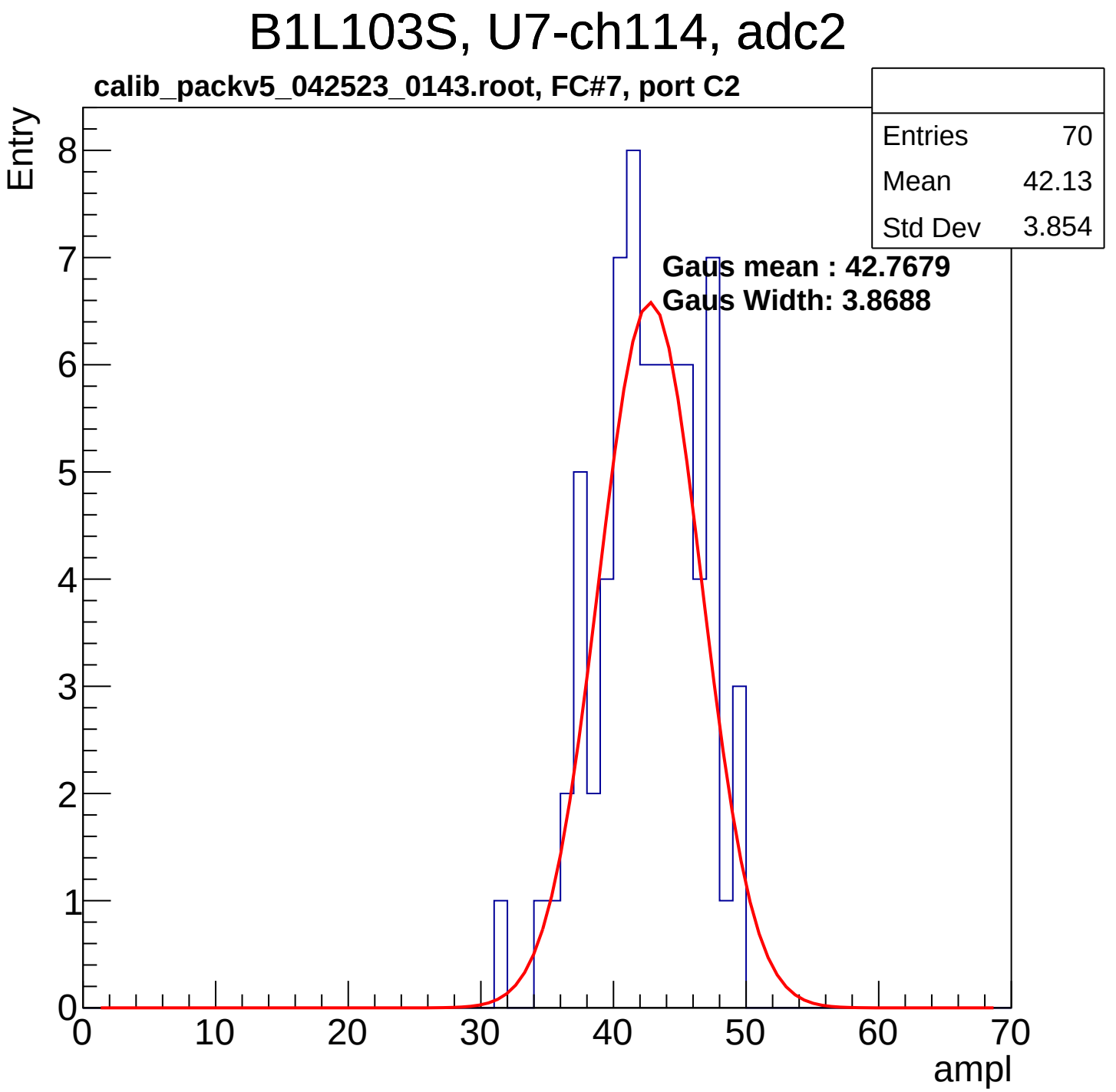
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

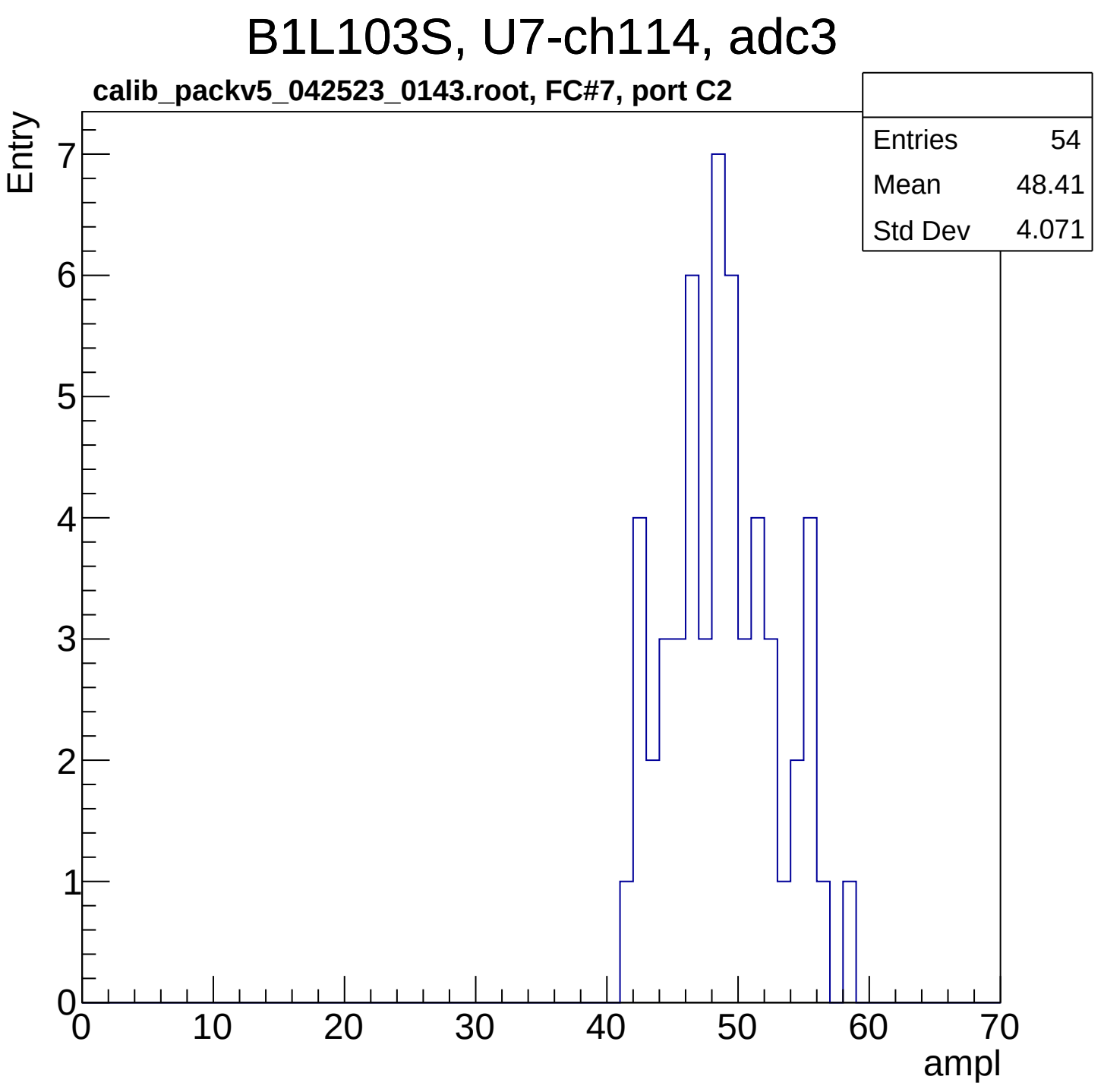

B1L103S, U7-ch113, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 18
Mean 57.39
Std Dev 14.03
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch113, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch114, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 28.14
Std Dev 5.257
Gaus mean : 30.0506
Gaus Width: 4.5040
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch114, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 35.12
Std Dev 3.888
Gaus mean : 35.6067
Gaus Width: 4.0064
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch114, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 42.13
Std Dev 3.854
Gaus mean : 42.7679
Gaus Width: 3.8688
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch114, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 54
Mean 48.41
Std Dev 4.071
Entry
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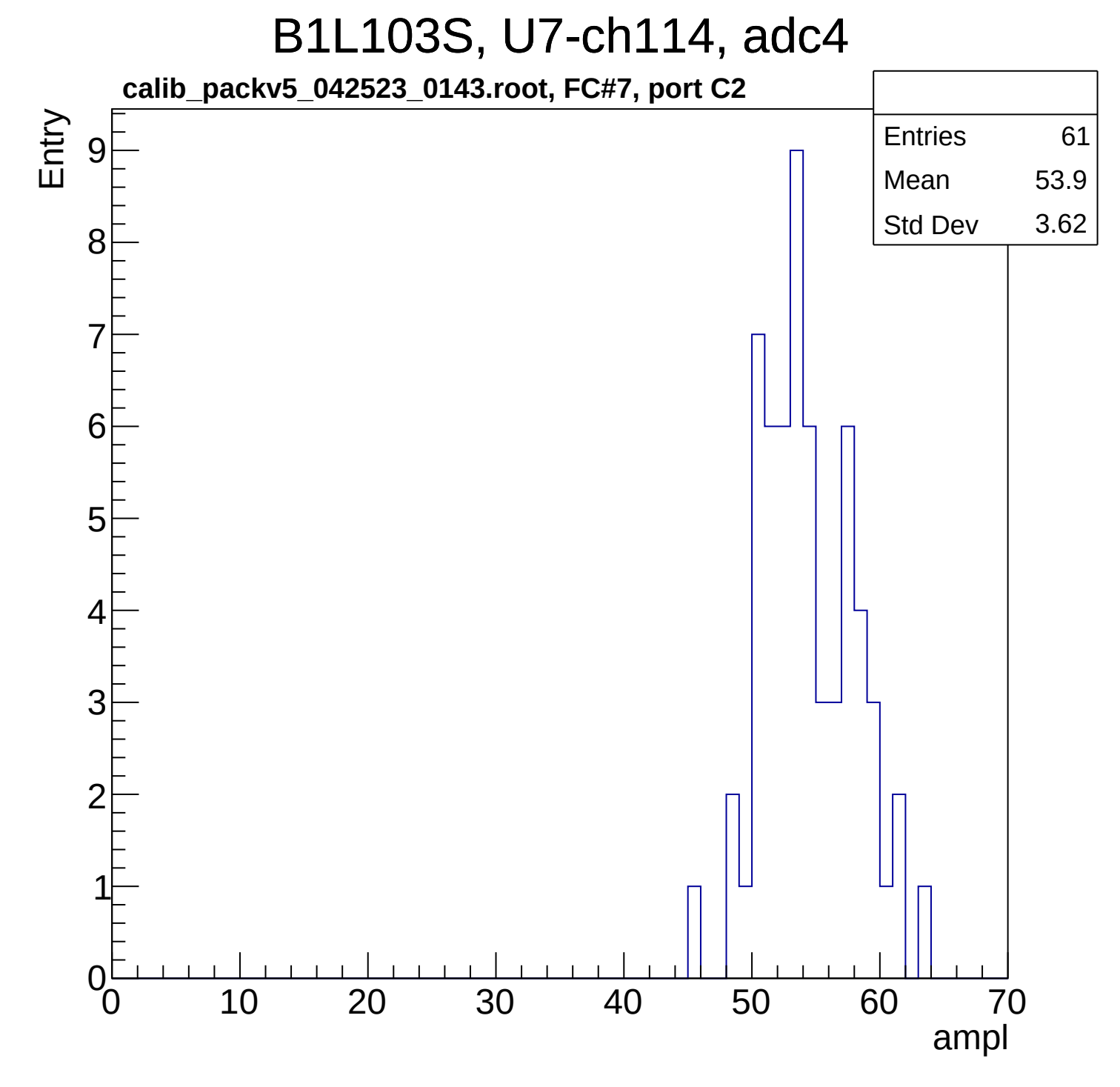
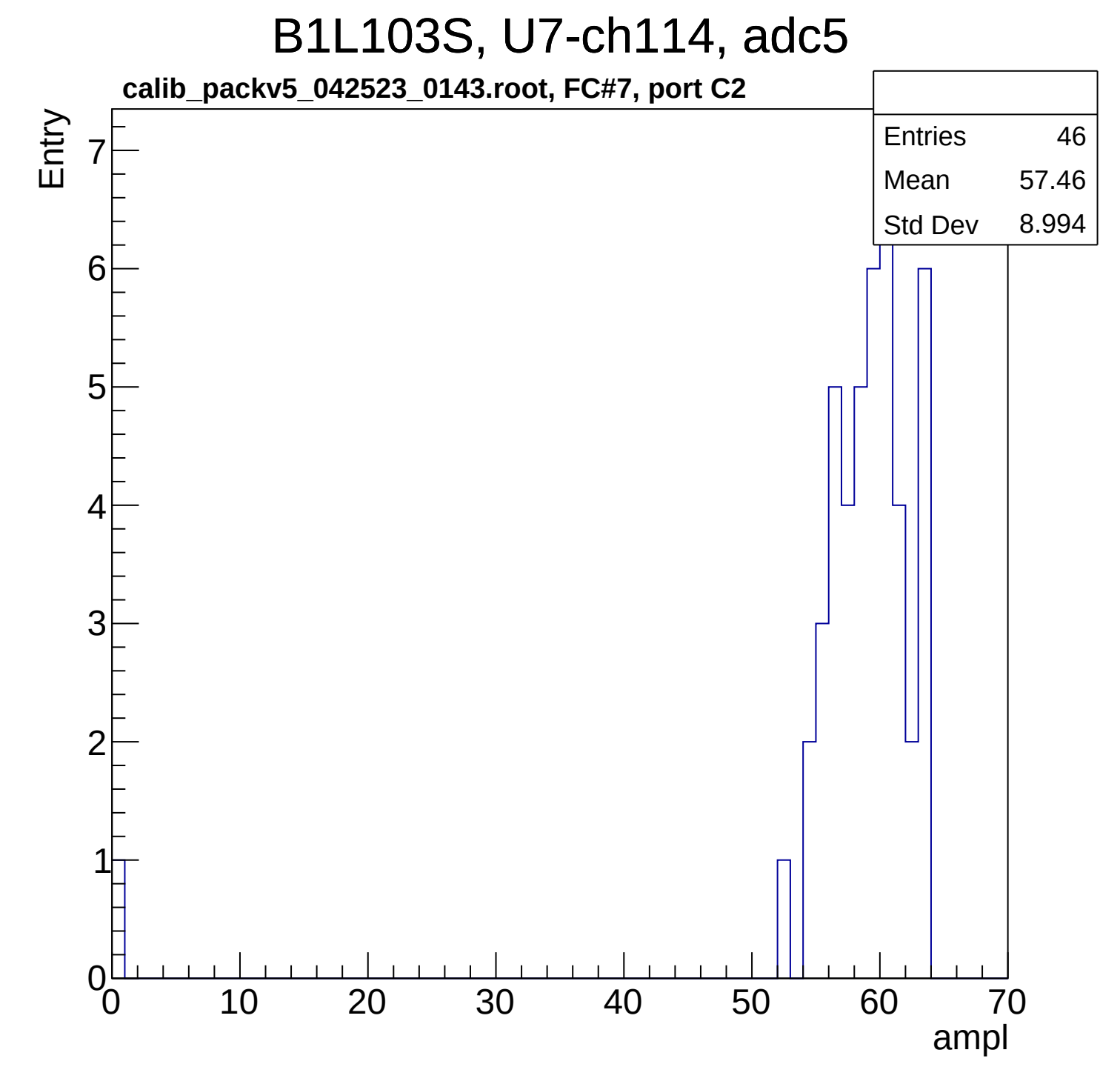
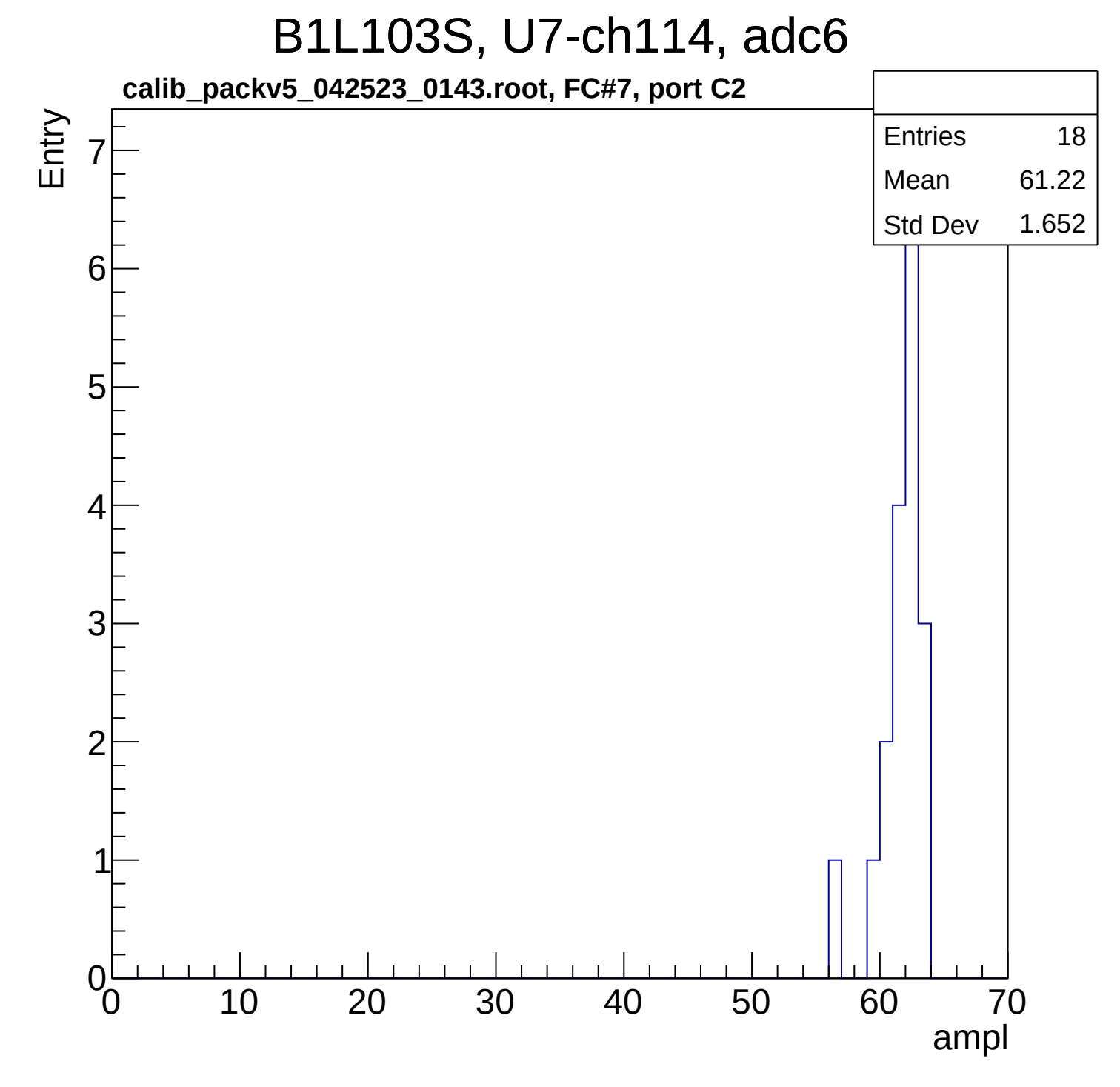
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch114, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 61
Mean 53.9
Std Dev 3.62
Entry
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch114, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 46
Mean 57.46
Std Dev 8.994
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch114, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 18
Mean 61.22
Std Dev 1.652
Entry
ampl
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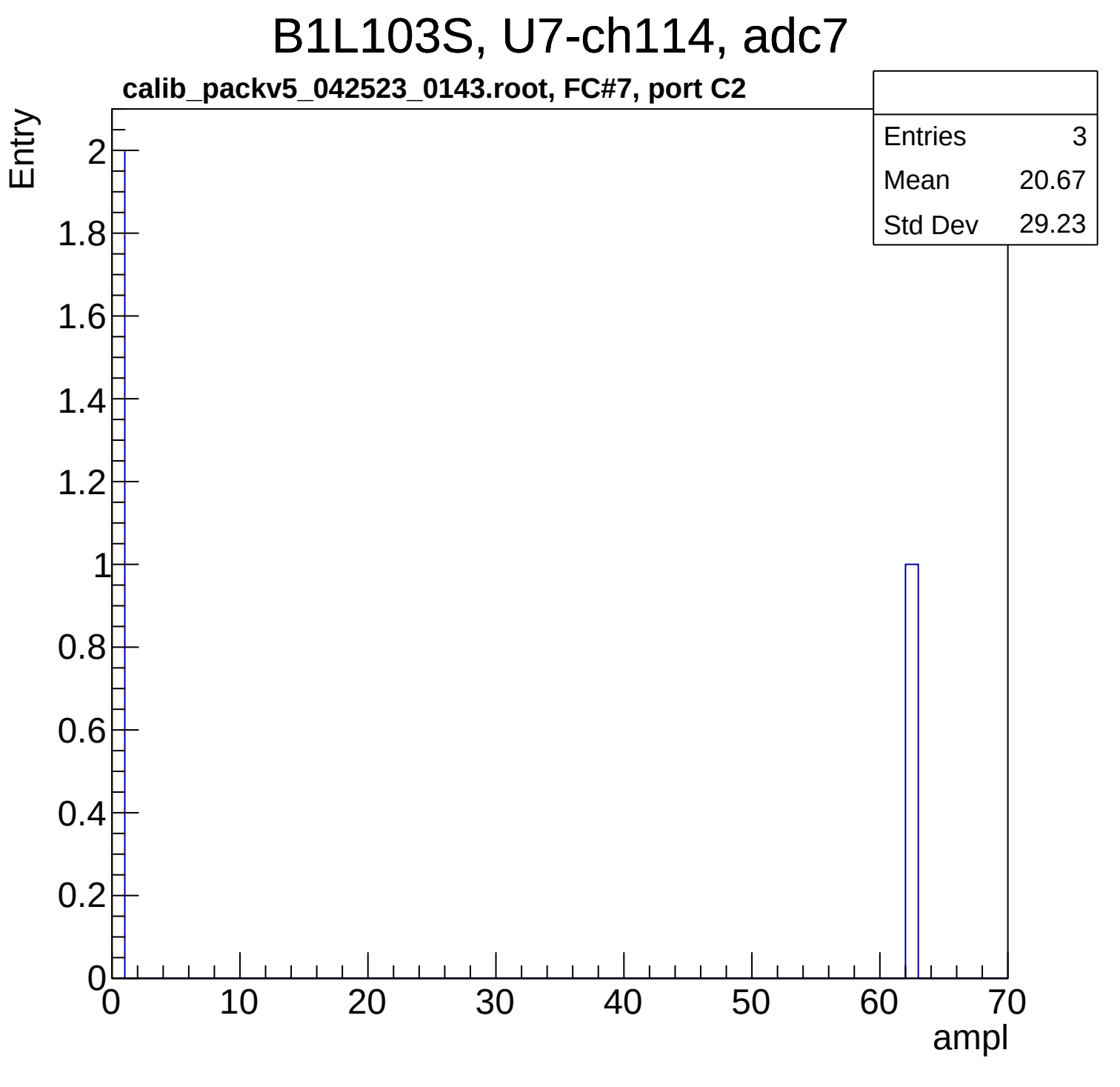
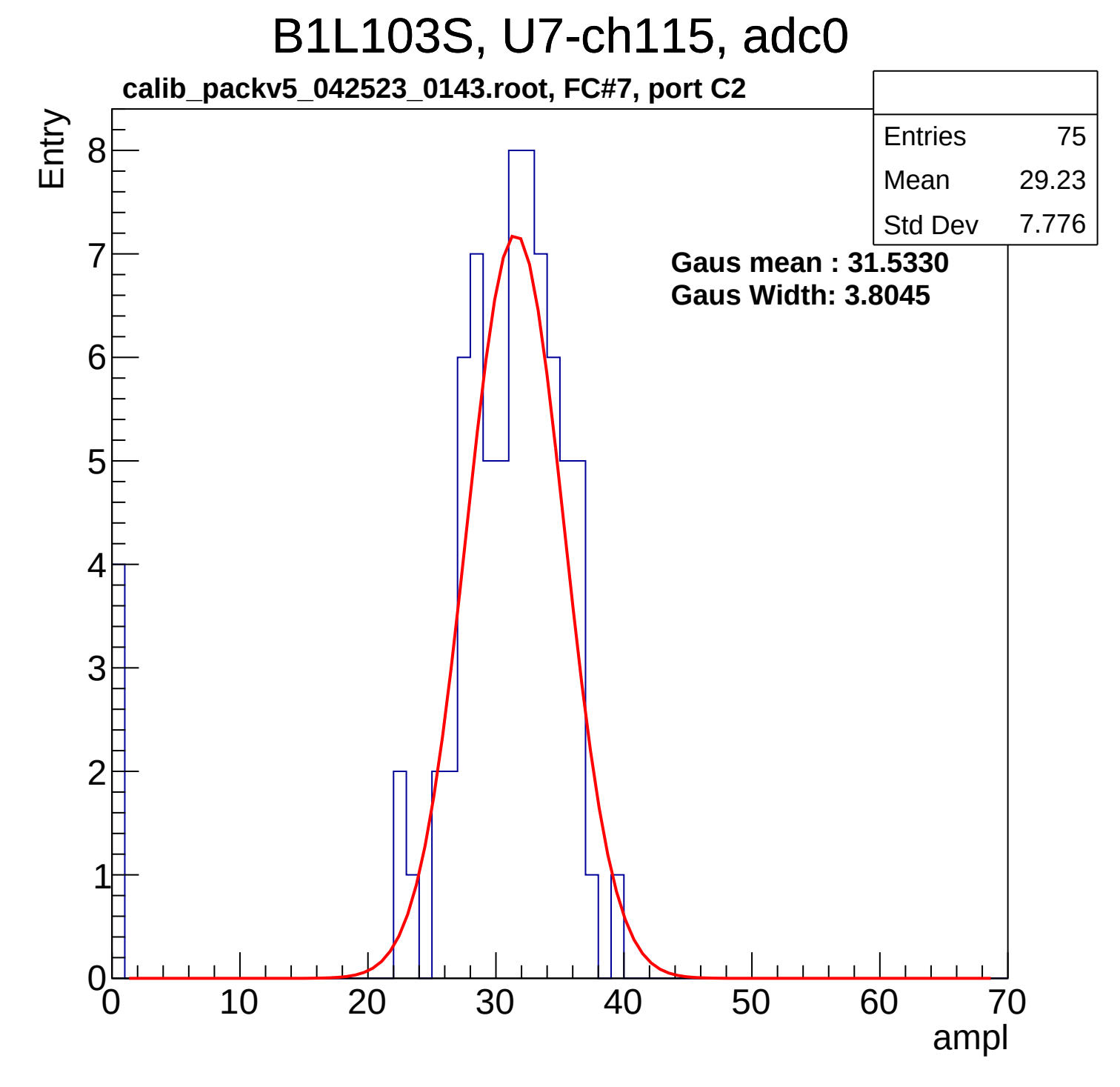
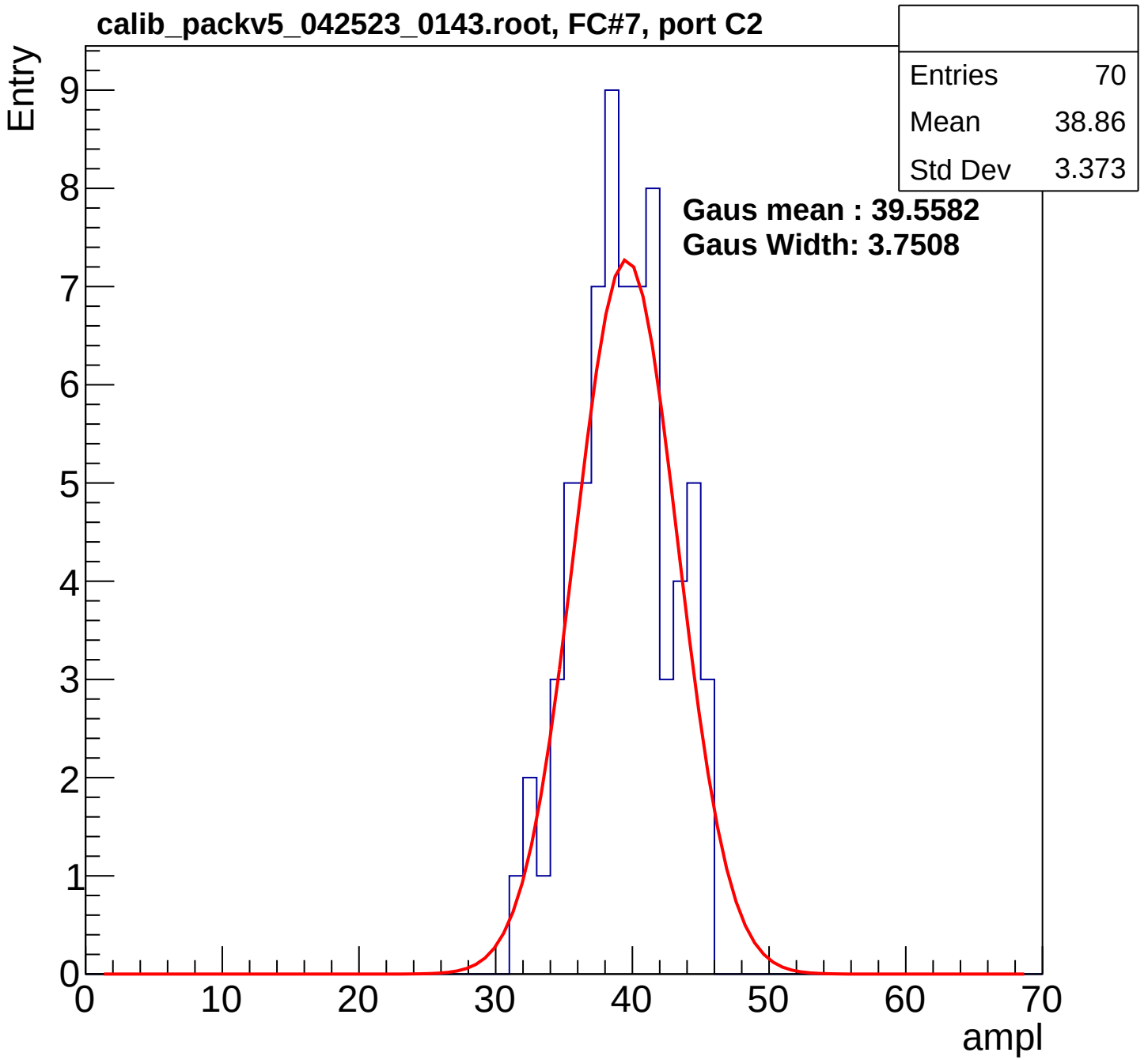
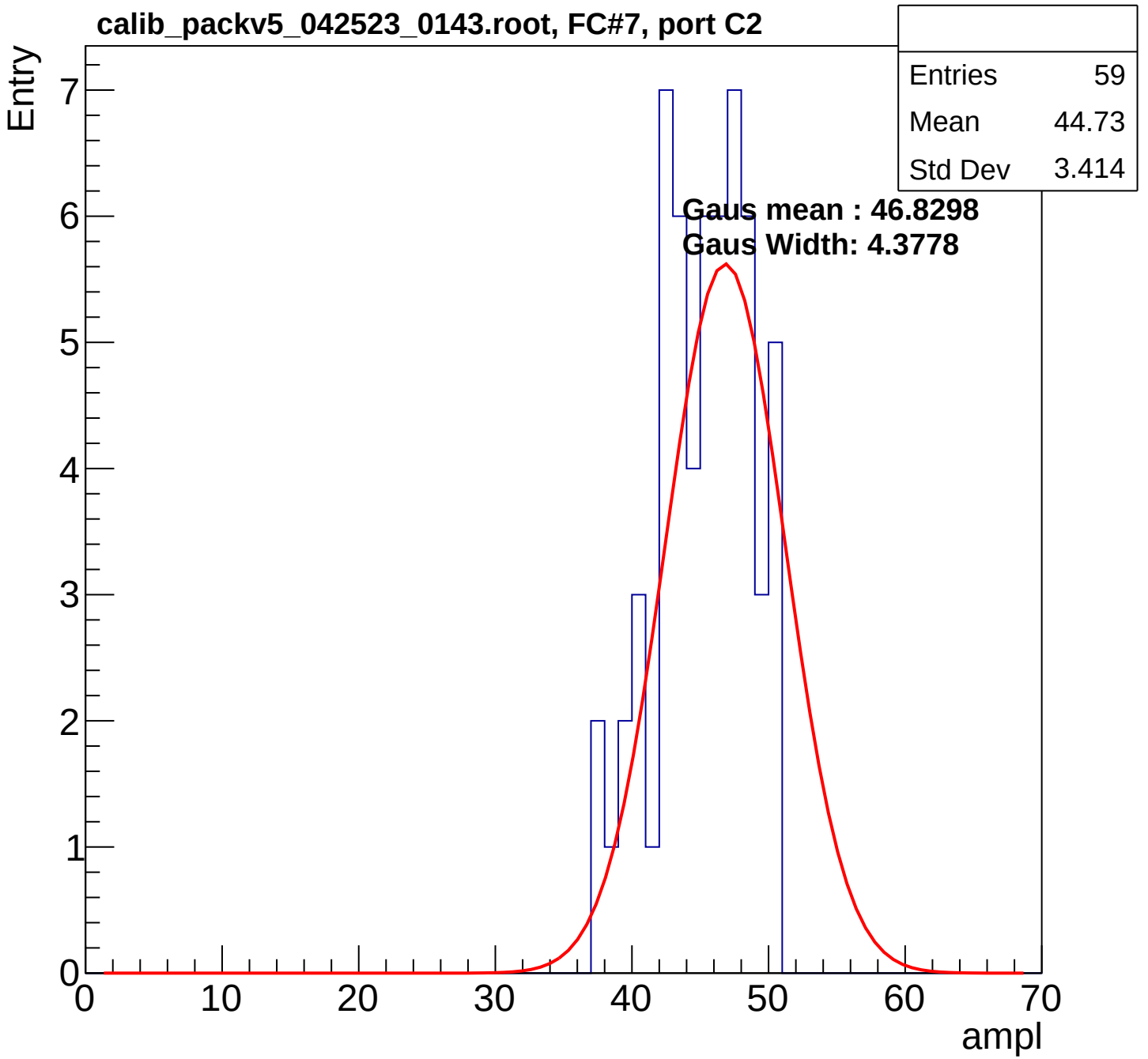
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch114, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 20.67
Std Dev 29.23
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U7-ch115, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 75
Mean 29.23
Std Dev 7.776
Gaus mean : 31.5330
Gaus Width: 3.8045
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch115, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 38.86
Std Dev 3.373
Gaus mean : 39.5582
Gaus Width: 3.7508
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch115, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 44.73
Std Dev 3.414
Gaus mean : 46.8298
Gaus Width: 4.3778
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
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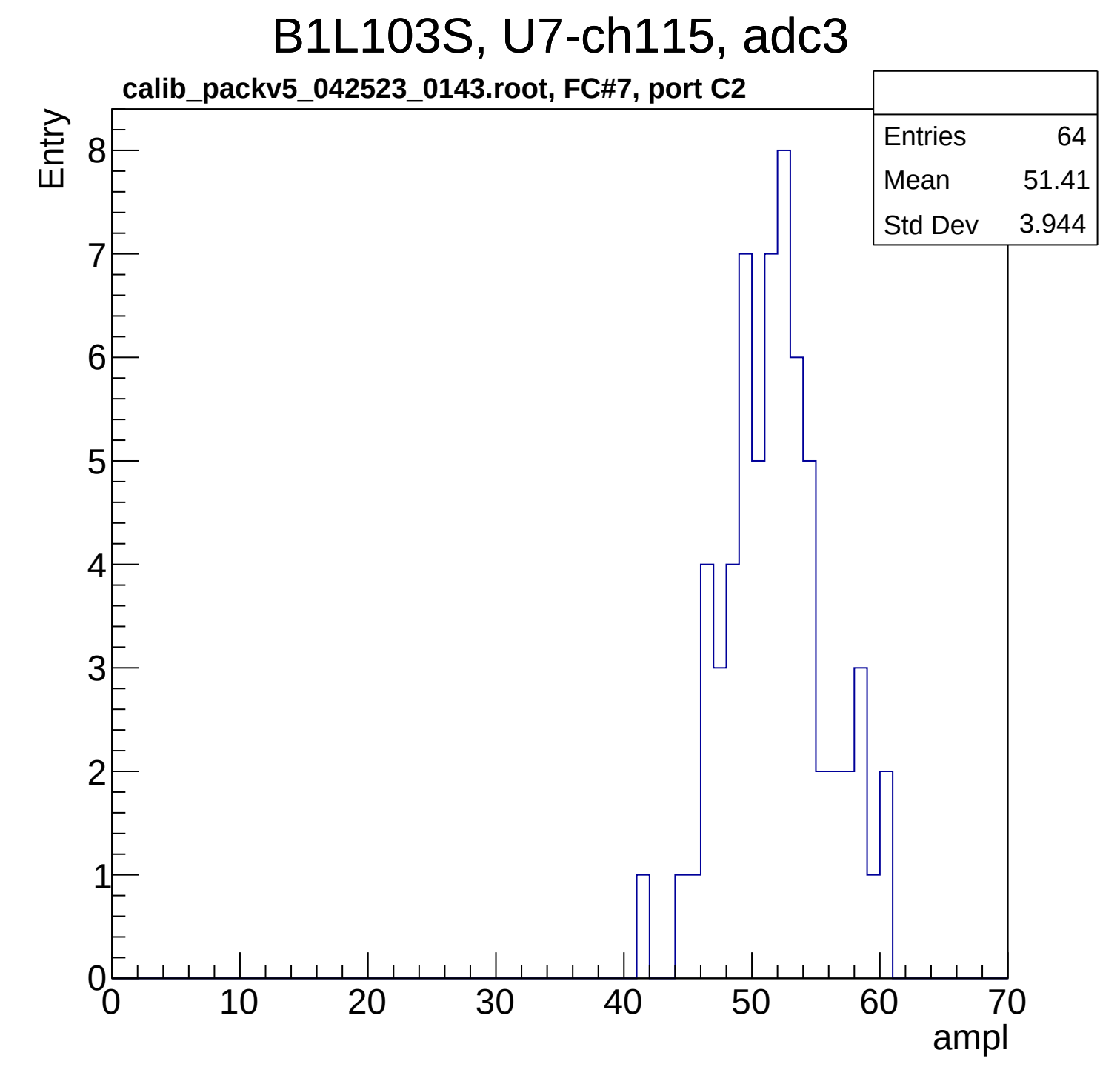
60
70


B1L103S, U7-ch115, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 51.41
Std Dev 3.944
Entry
ampl
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0
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60
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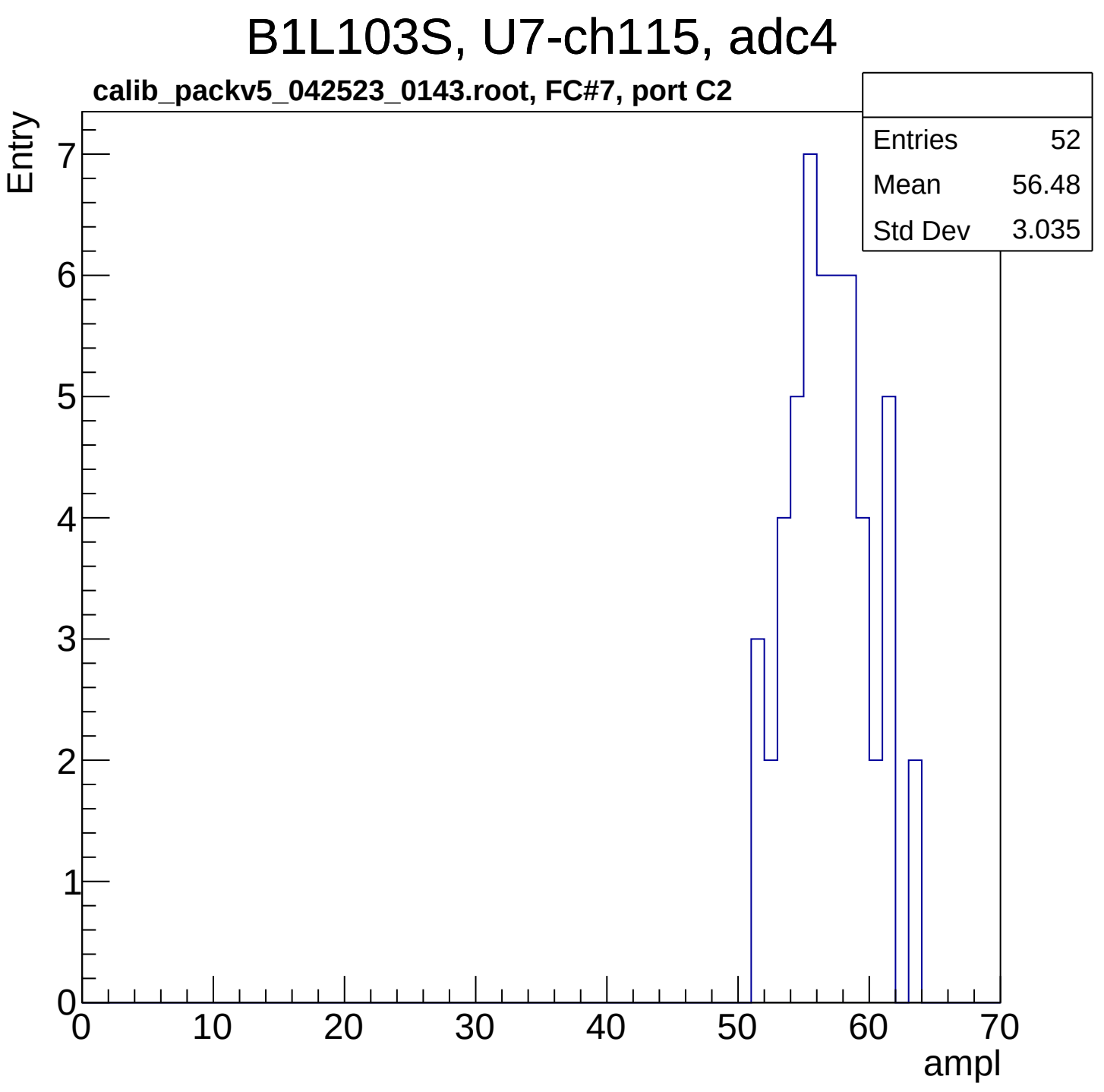
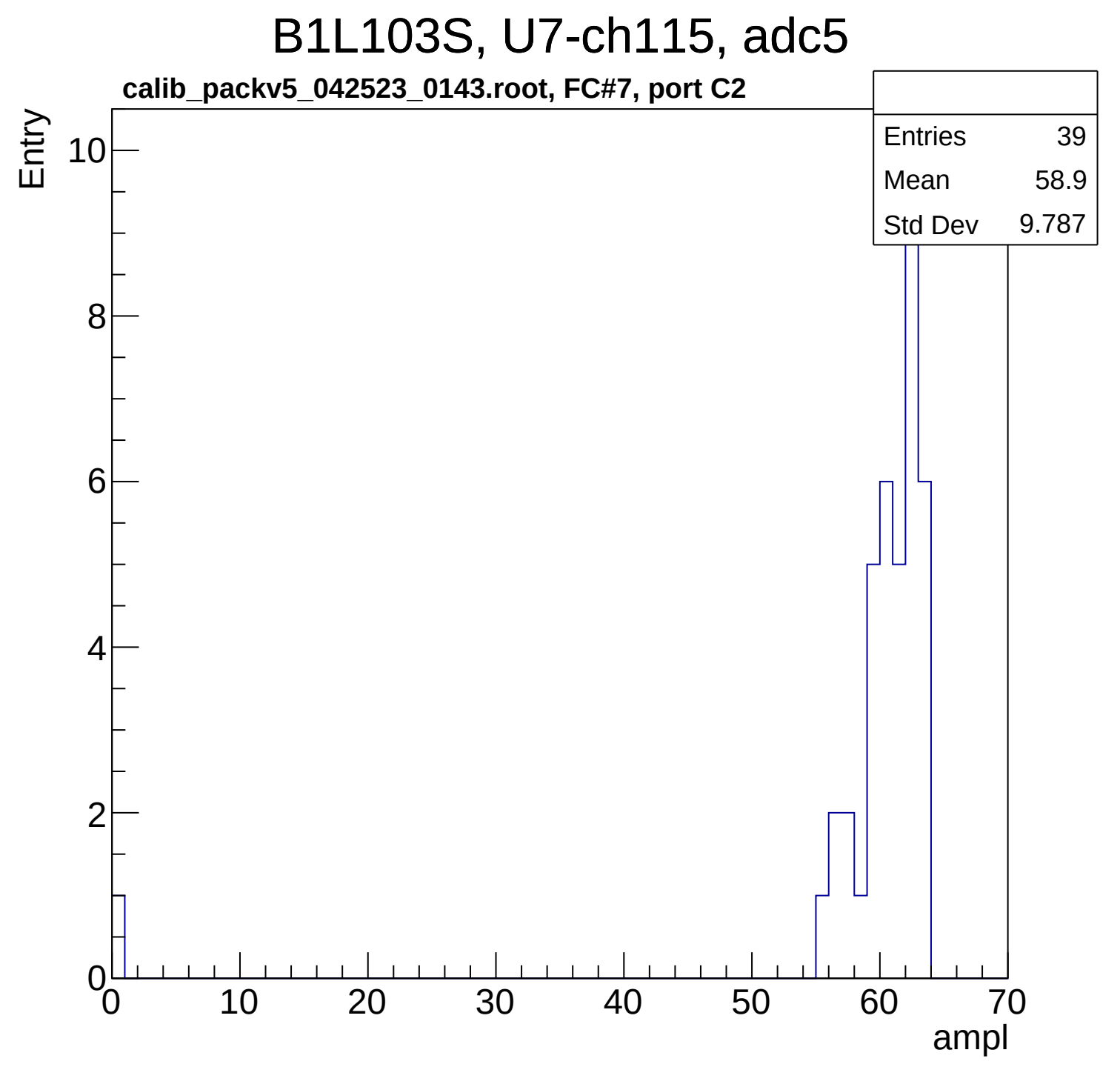
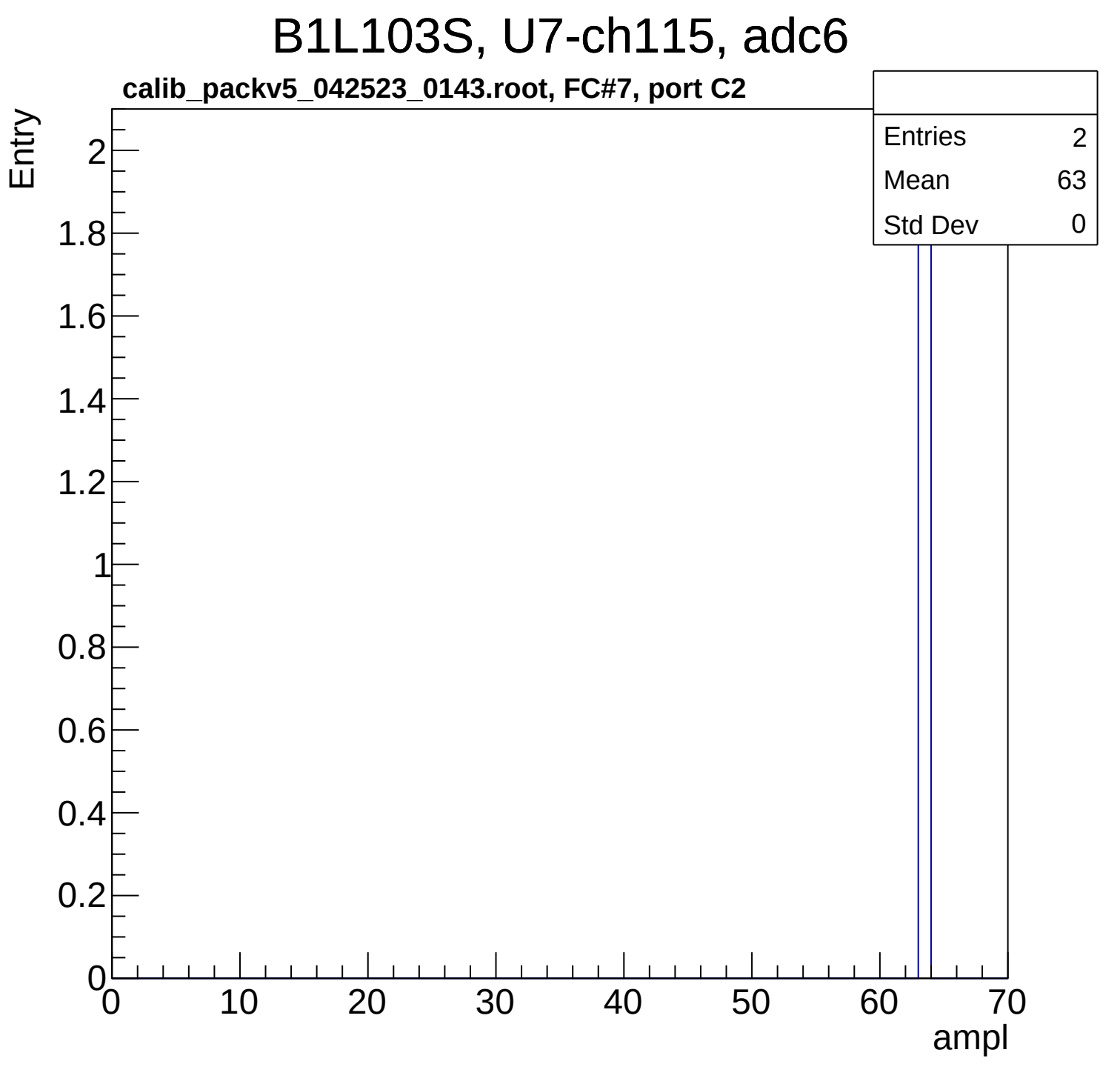
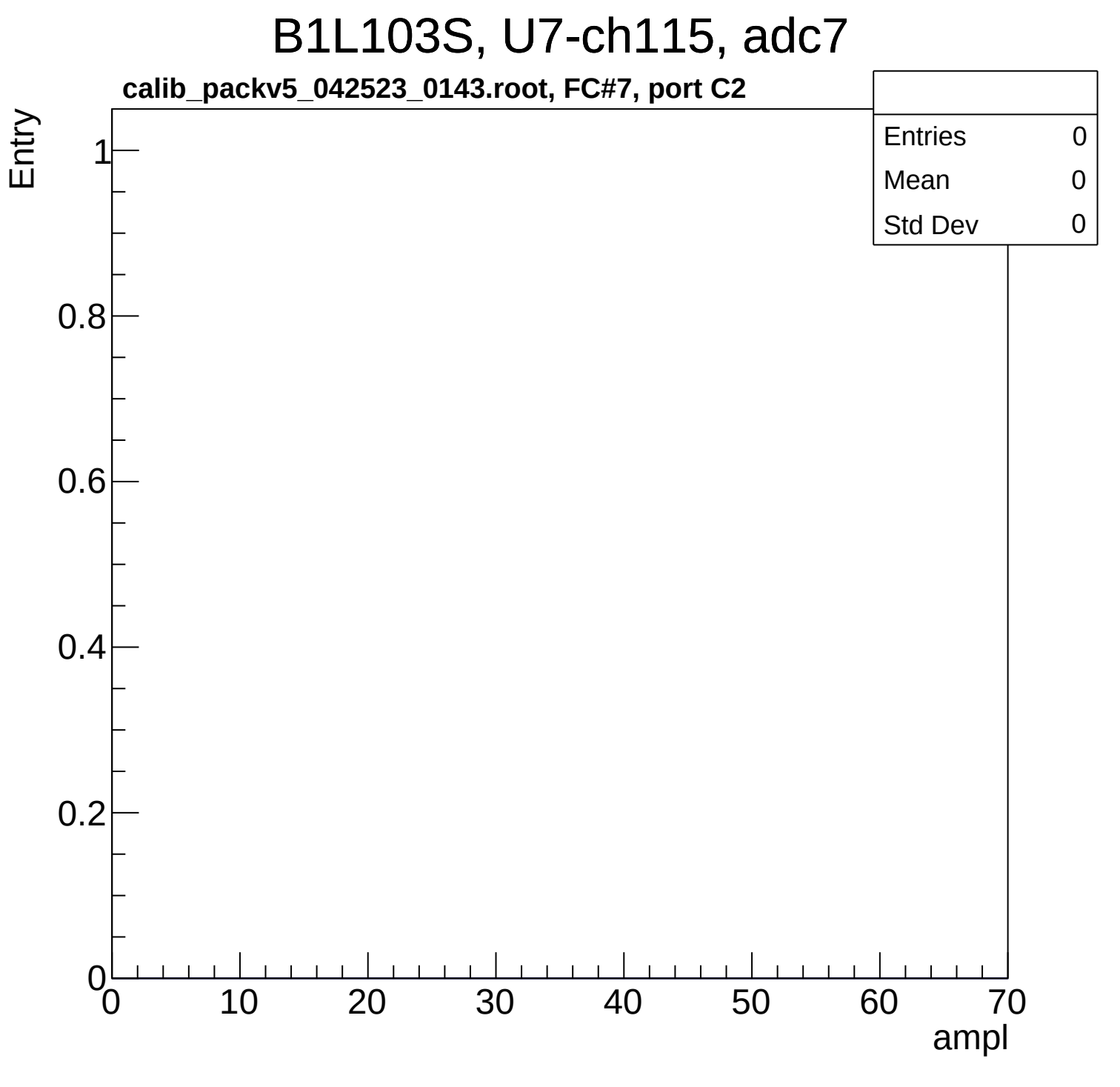

B1L103S, U7-ch115, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 52
Mean 56.48
Std Dev 3.035
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch115, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 39
Mean 58.9
Std Dev 9.787
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch115, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 63
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U7-ch115, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
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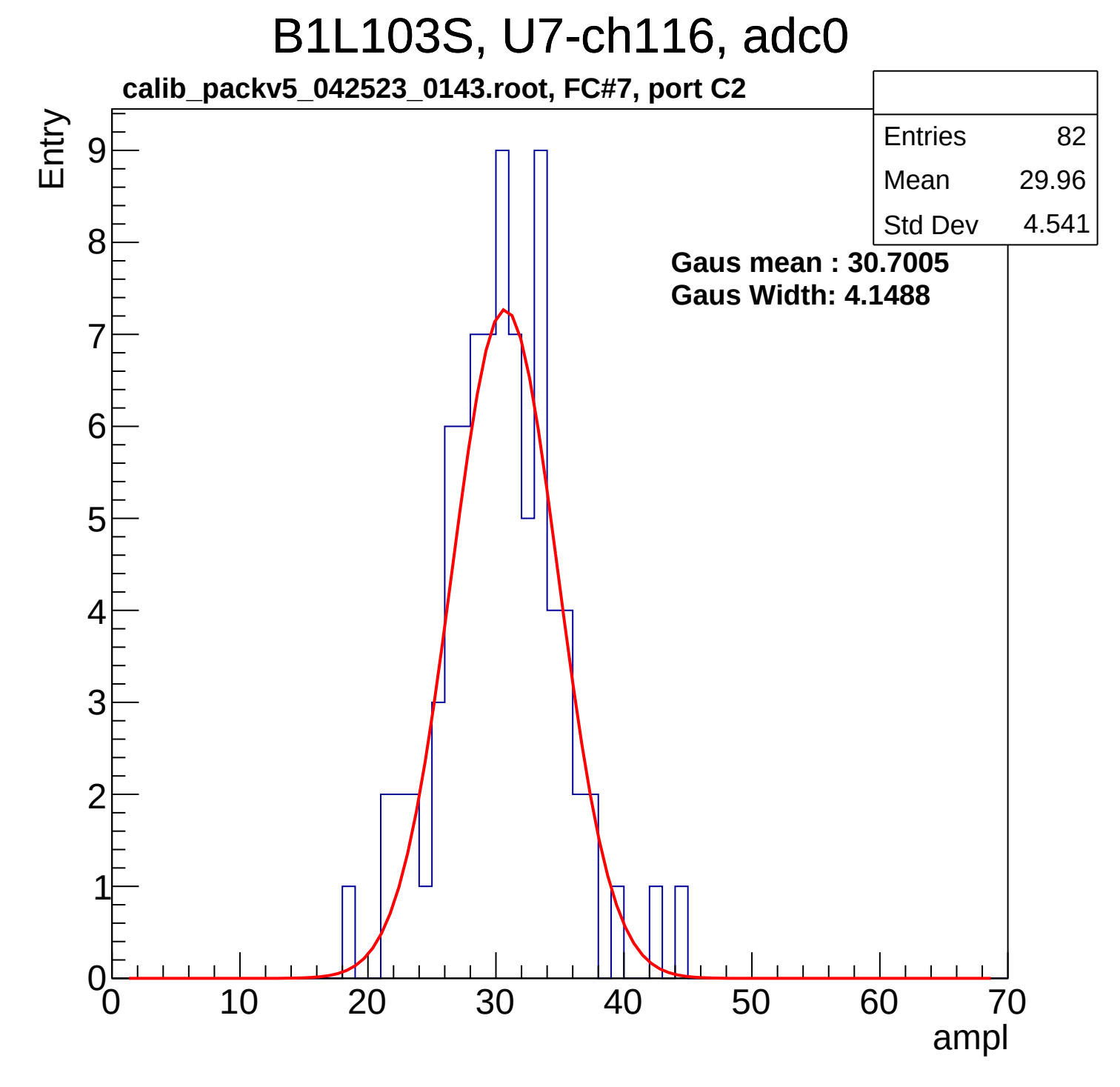
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch116, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 82
Mean 29.96
Std Dev 4.541
Gaus mean : 30.7005
Gaus Width: 4.1488
Entry
ampl
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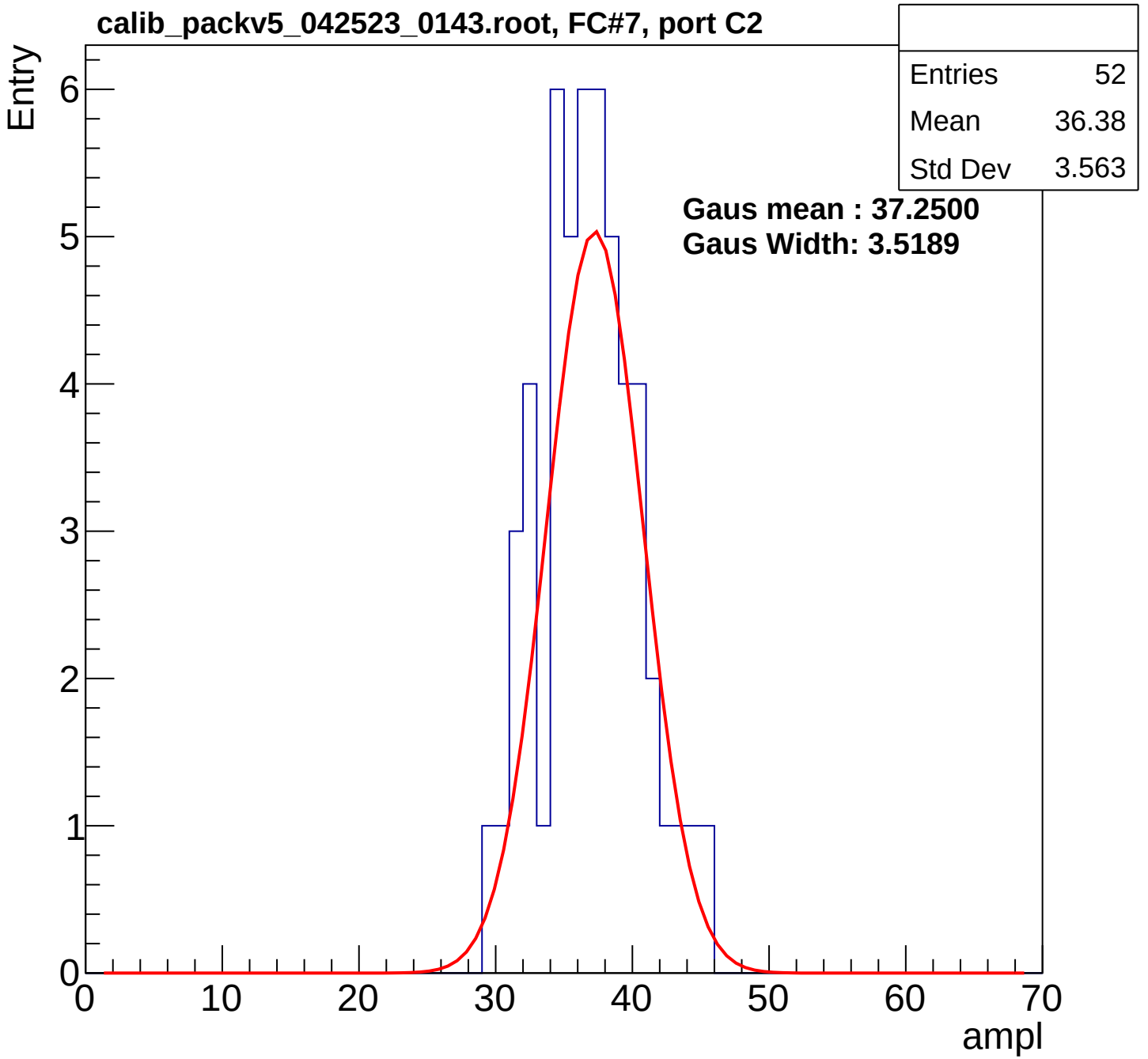
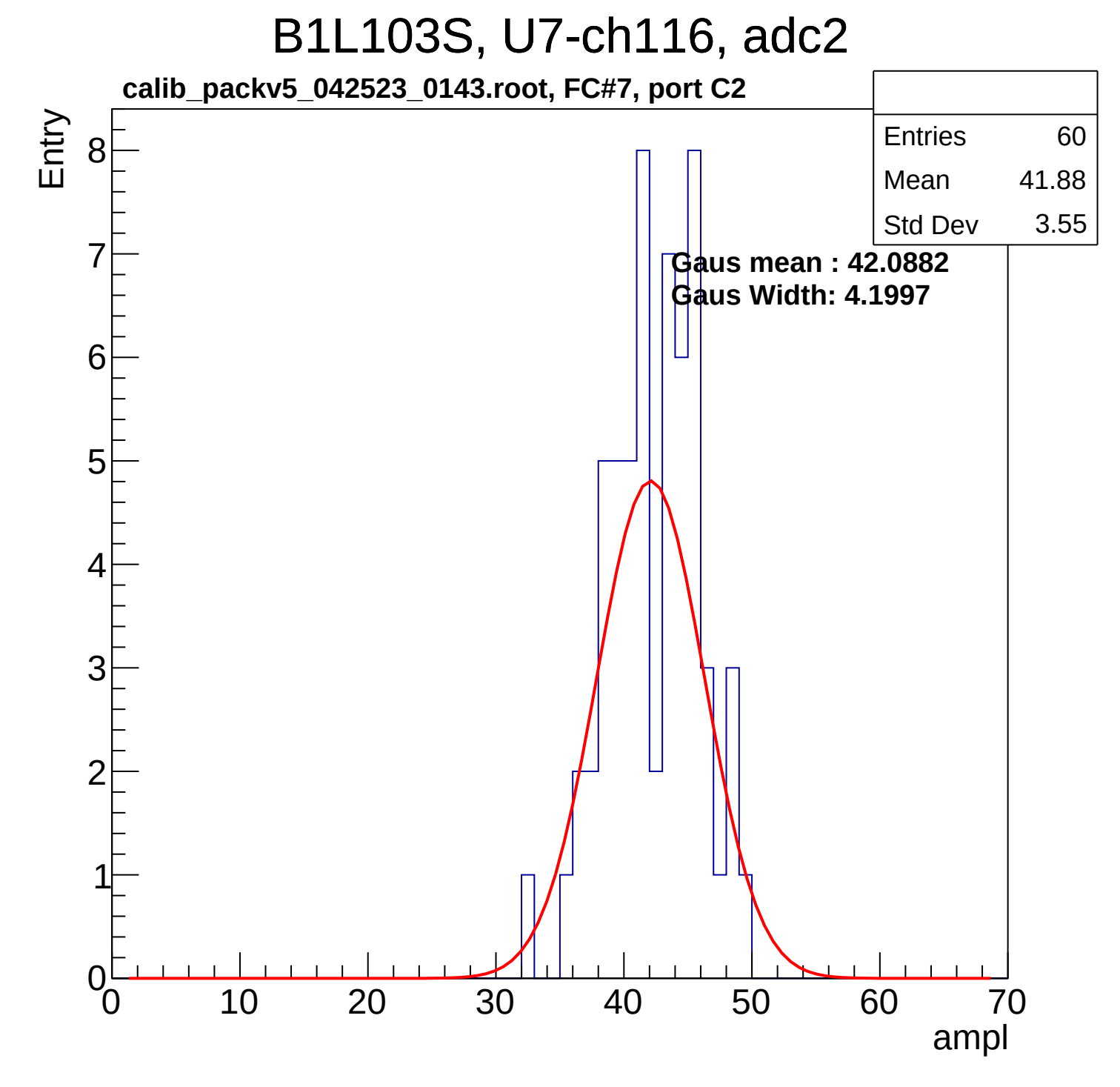
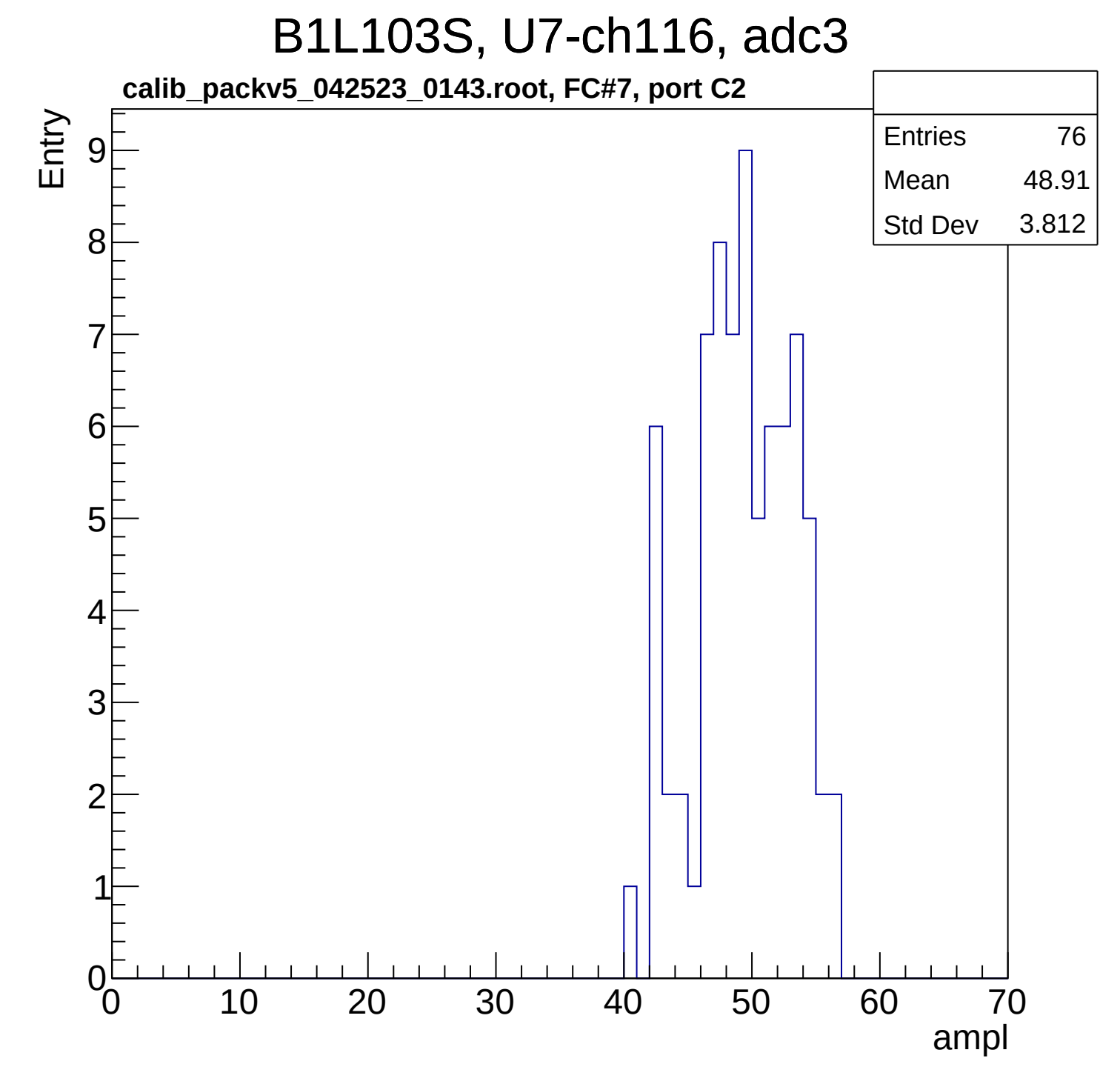
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch116, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 52
Mean 36.38
Std Dev 3.563
Gaus mean : 37.2500
Gaus Width: 3.5189
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U7-ch116, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 60
Mean 41.88
Std Dev 3.55
Gaus mean : 42.0882
Gaus Width: 4.1997
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch116, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 76
Mean 48.91
Std Dev 3.812
Entry
ampl
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2
3
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7
8
9
0
10
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40
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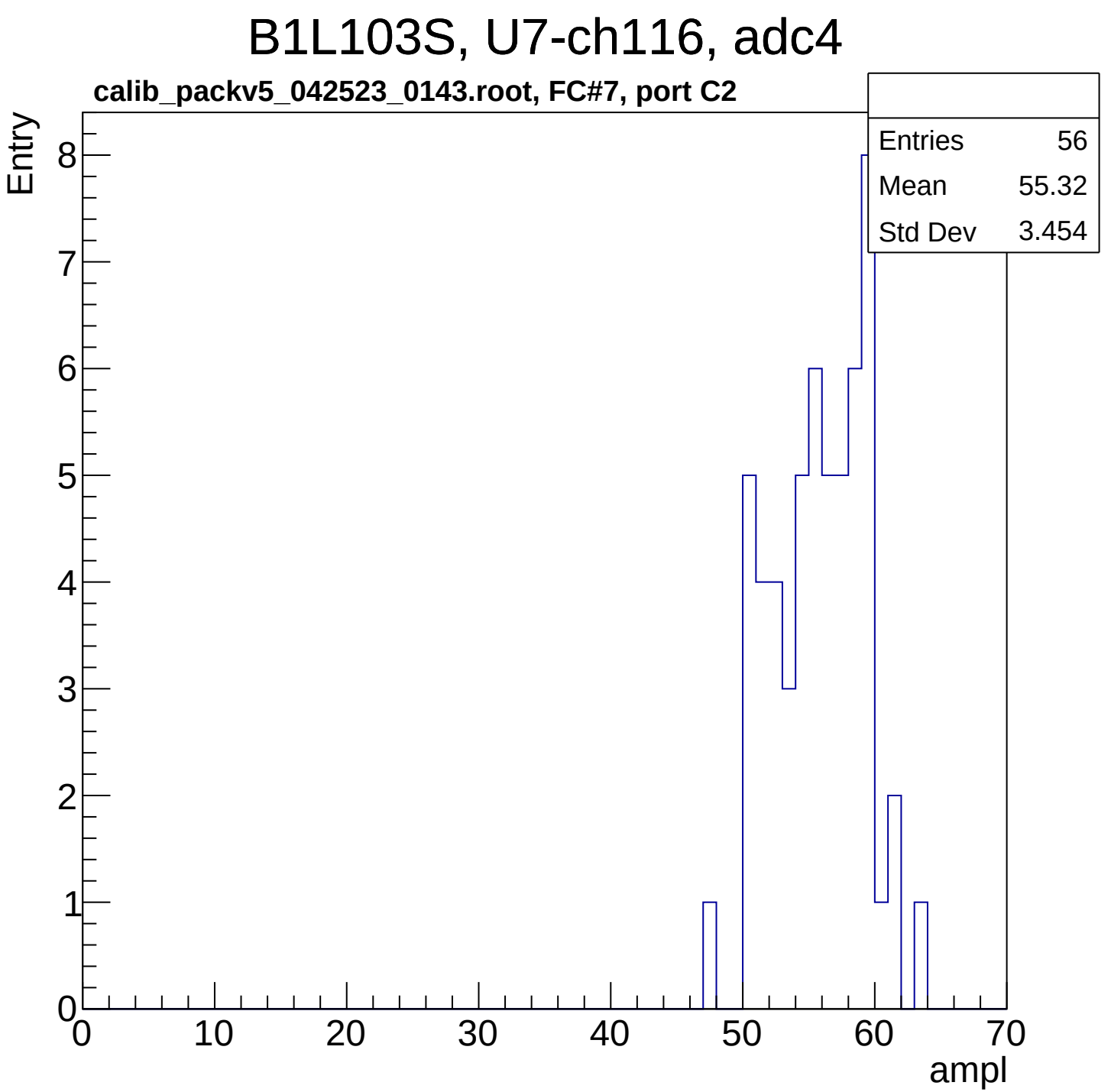
B1L103S, U7-ch116, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 55.32
Std Dev 3.454
Entry
ampl
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3
4
5
6
7
8
0
10
20
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40
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60
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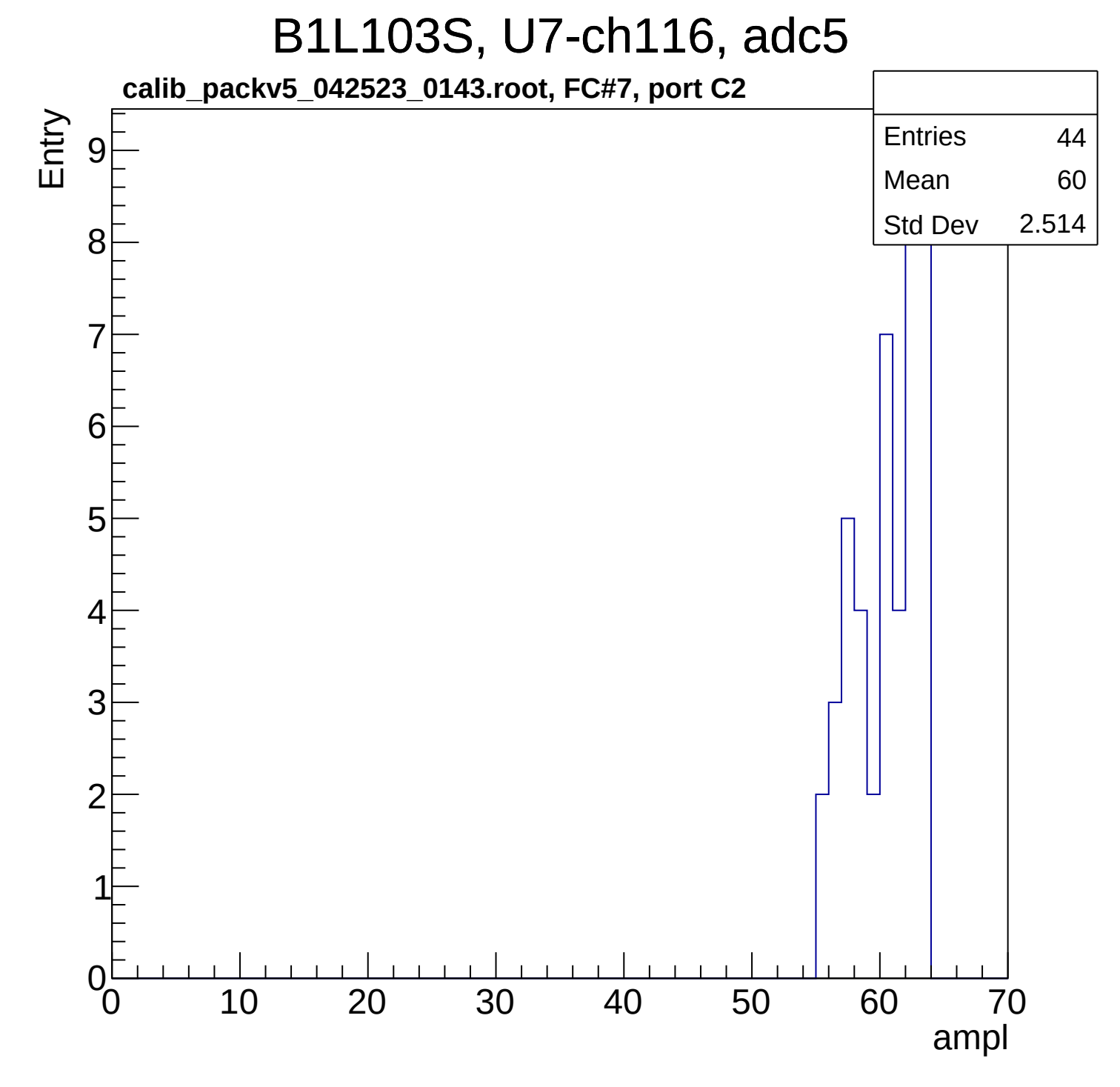
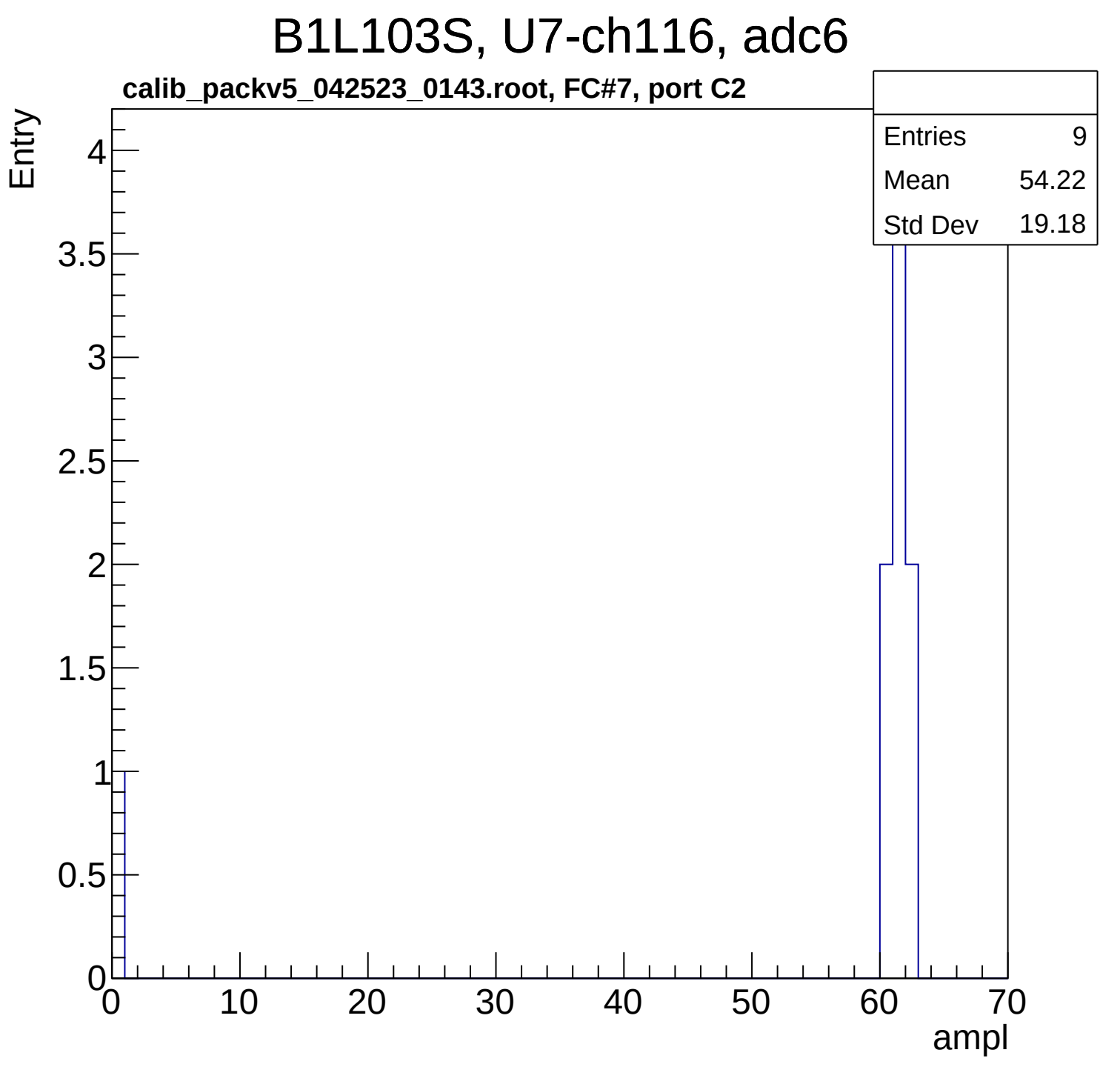

B1L103S, U7-ch116, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 44
Mean 60
Std Dev 2.514
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch116, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 9
Mean 54.22
Std Dev 19.18
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
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20
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40
50
60
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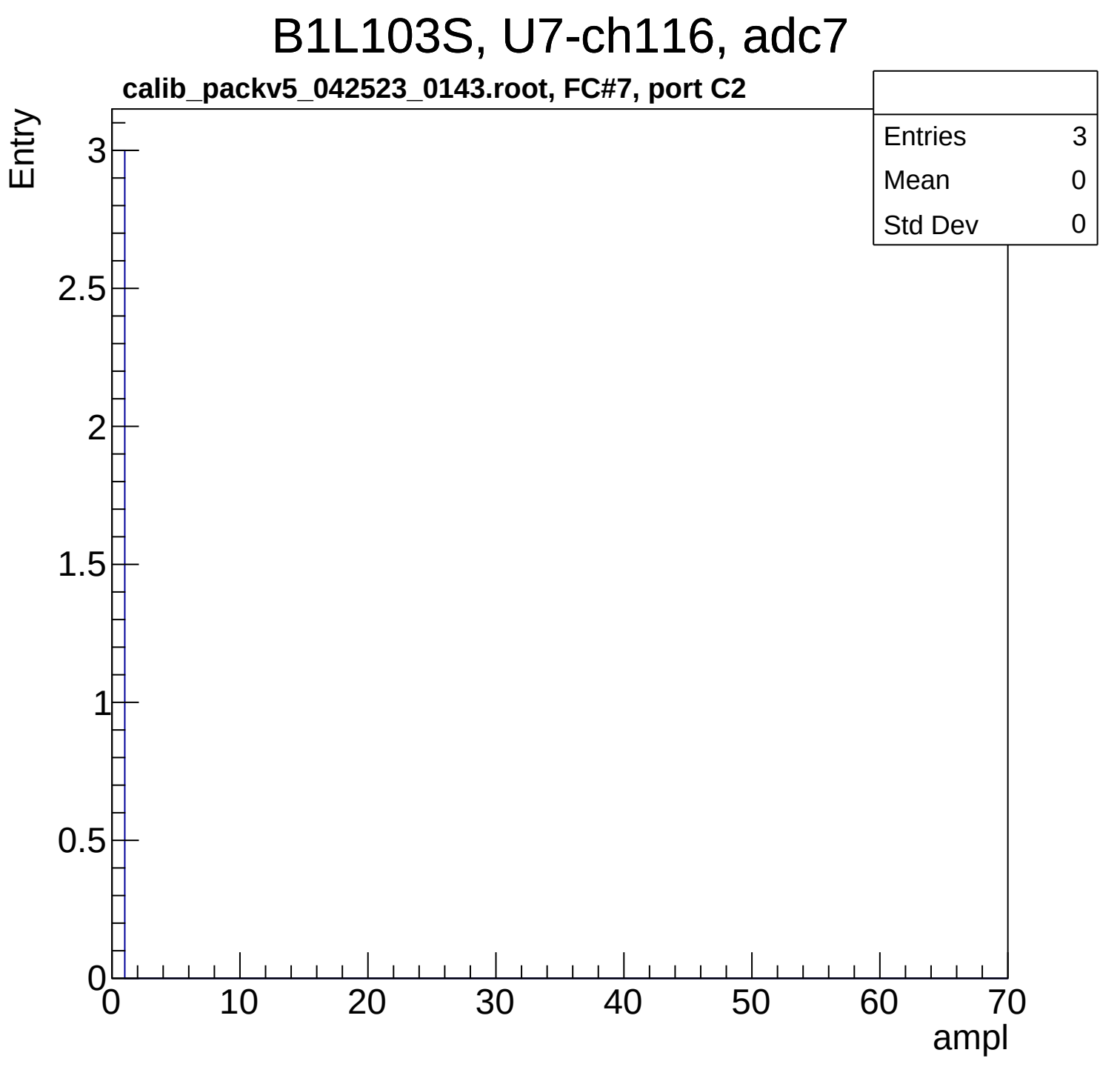
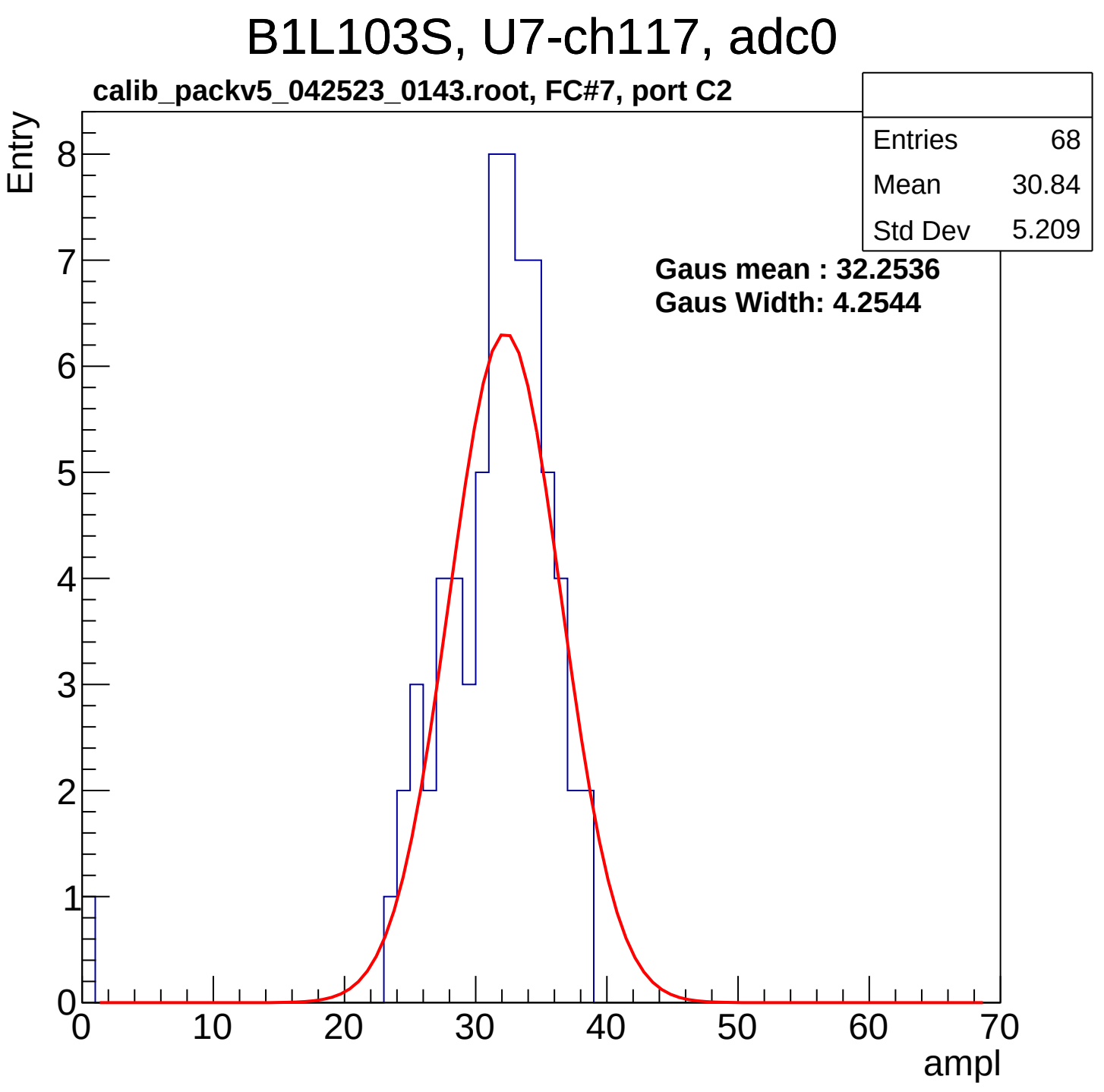

B1L103S, U7-ch116, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 0
Std Dev 0
Entry
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch117, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 30.84
Std Dev 5.209
Gaus mean : 32.2536
Gaus Width: 4.2544
Entry
ampl
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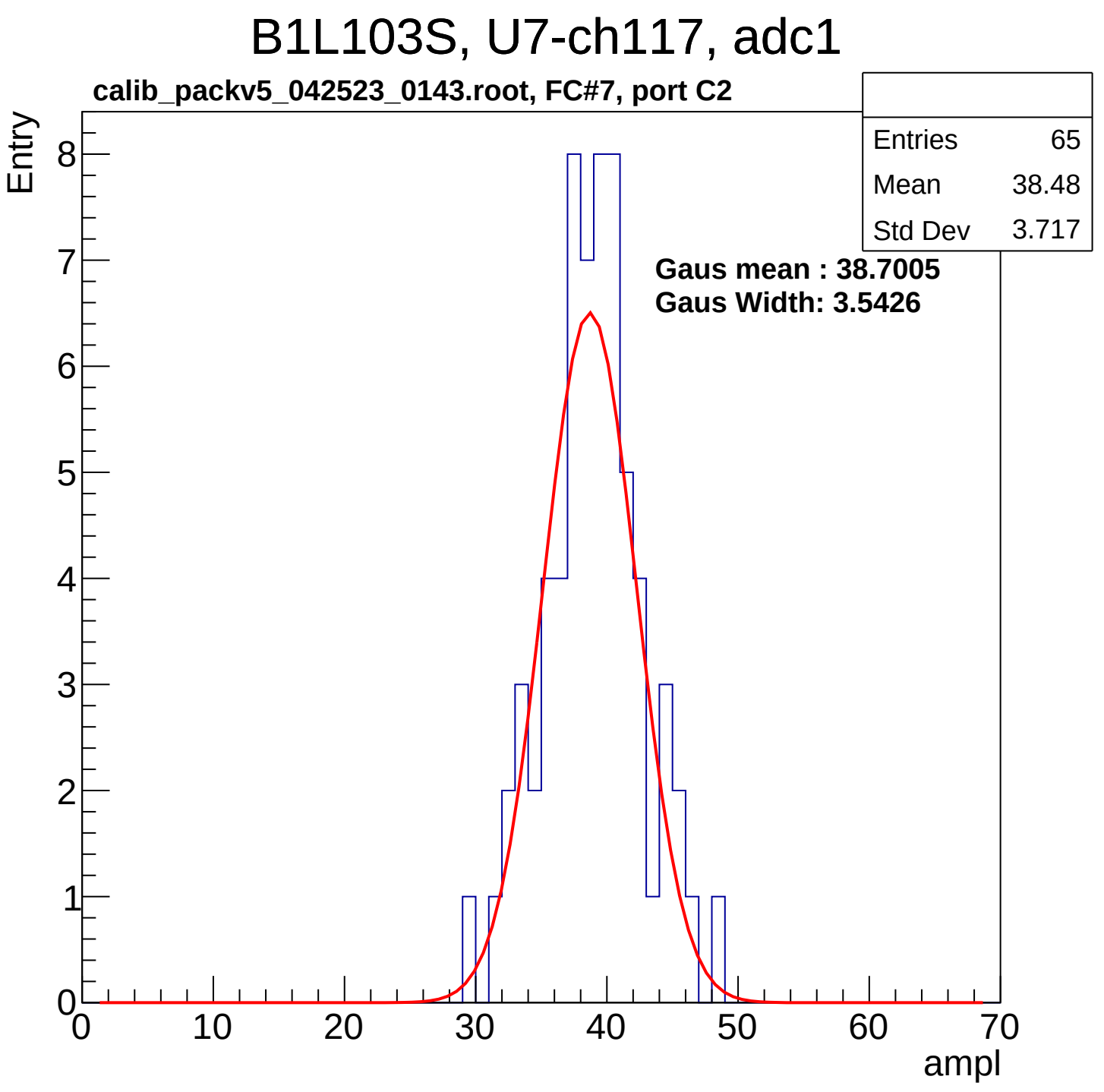
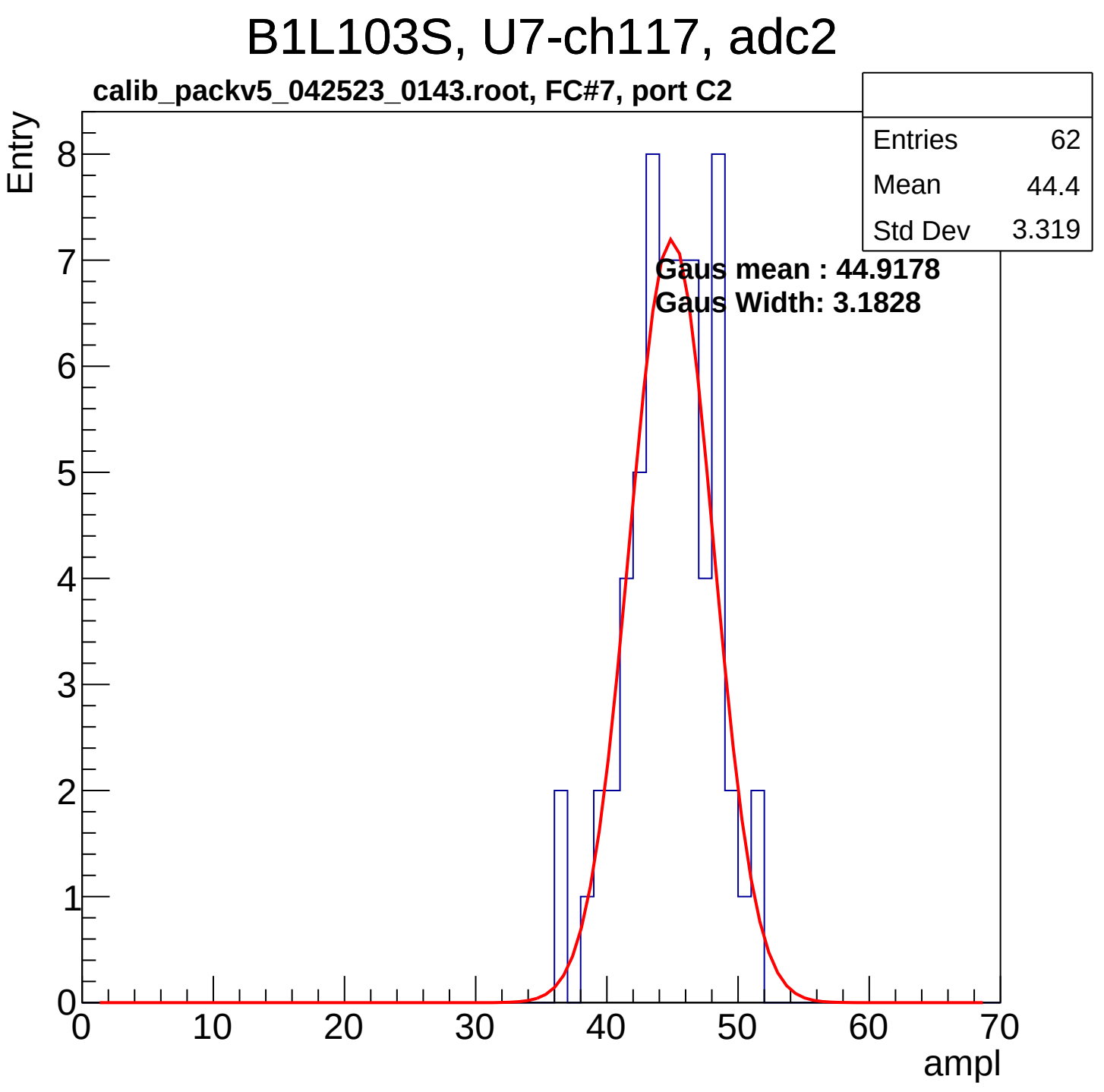
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch117, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 38.48
Std Dev 3.717
Gaus mean : 38.7005
Gaus Width: 3.5426
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch117, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 62
Mean 44.4
Std Dev 3.319
Gaus mean : 44.9178
Gaus Width: 3.1828
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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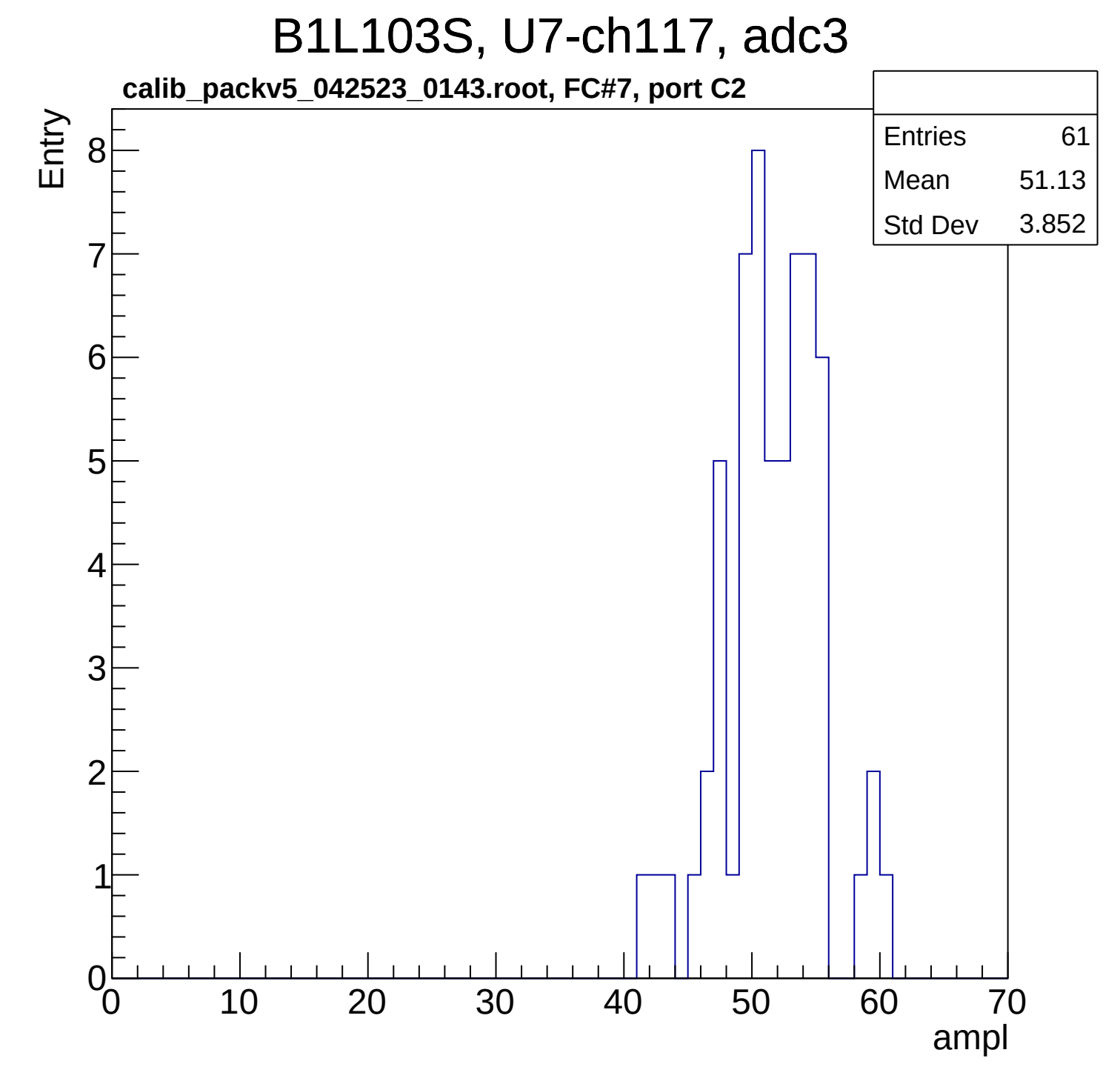
B1L103S, U7-ch117, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 61
Mean 51.13
Std Dev 3.852
Entry
ampl
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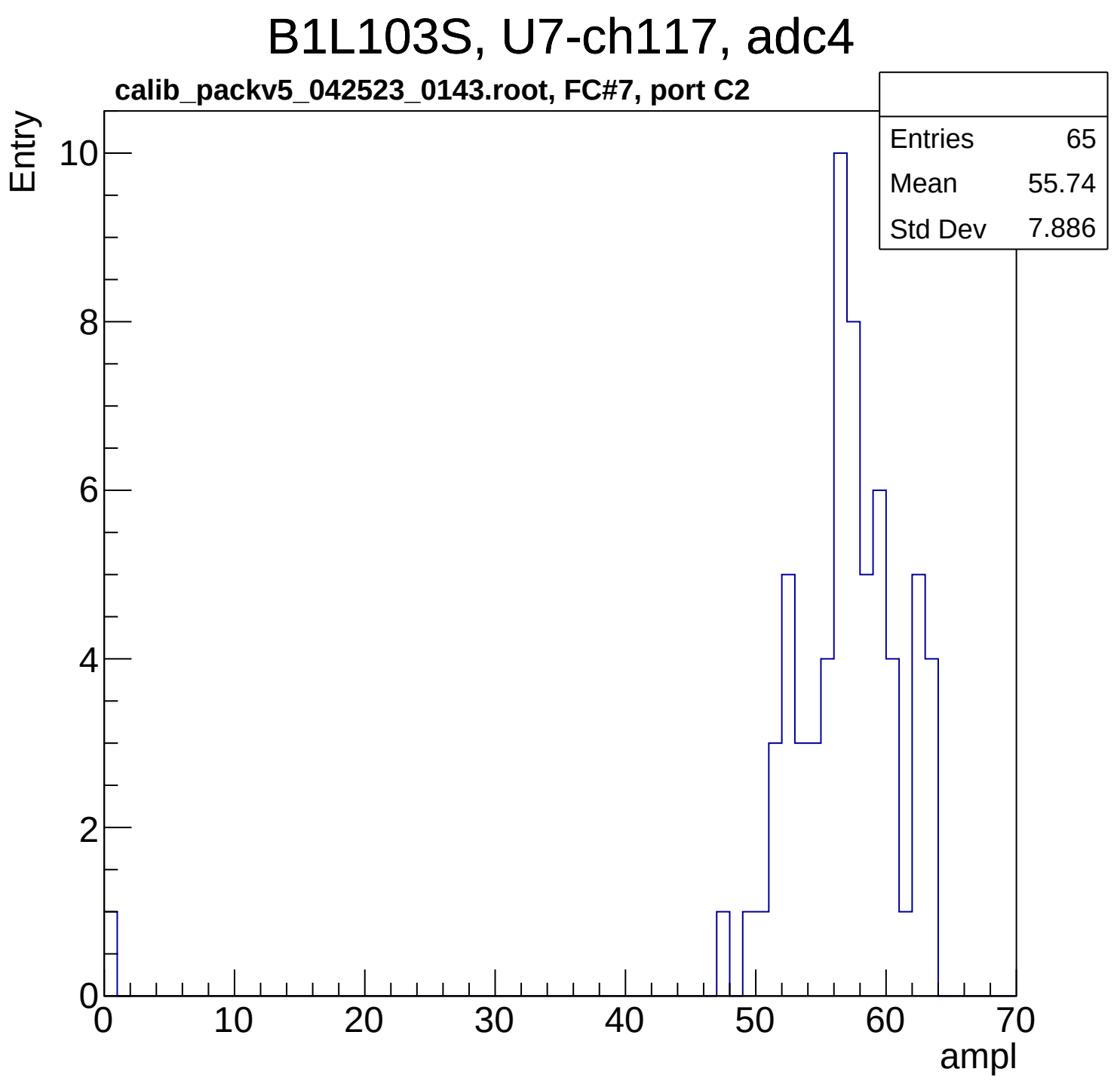
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch117, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 55.74
Std Dev 7.886
Entry
ampl
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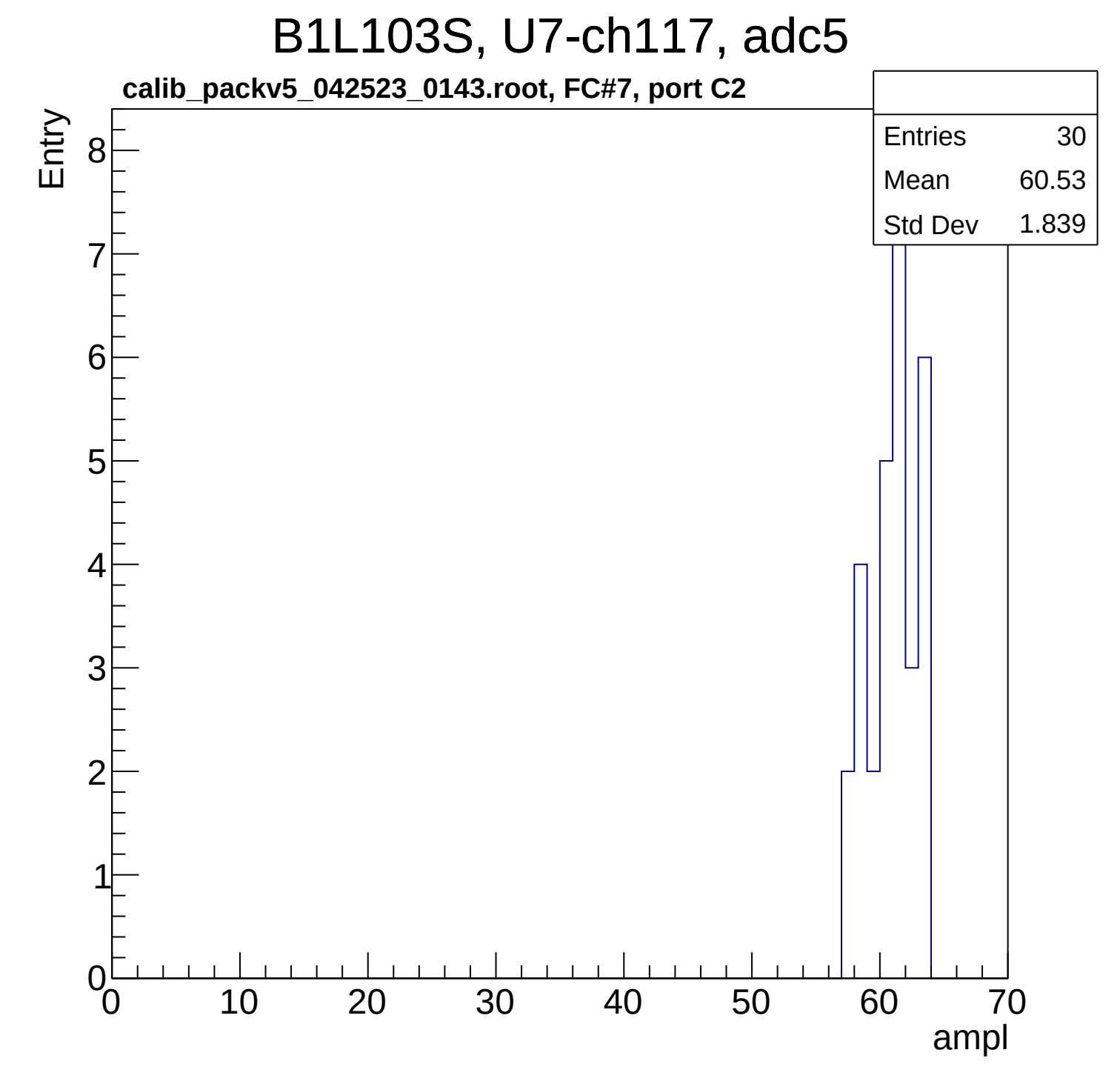
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch117, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 30
Mean 60.53
Std Dev 1.839
Entry
0
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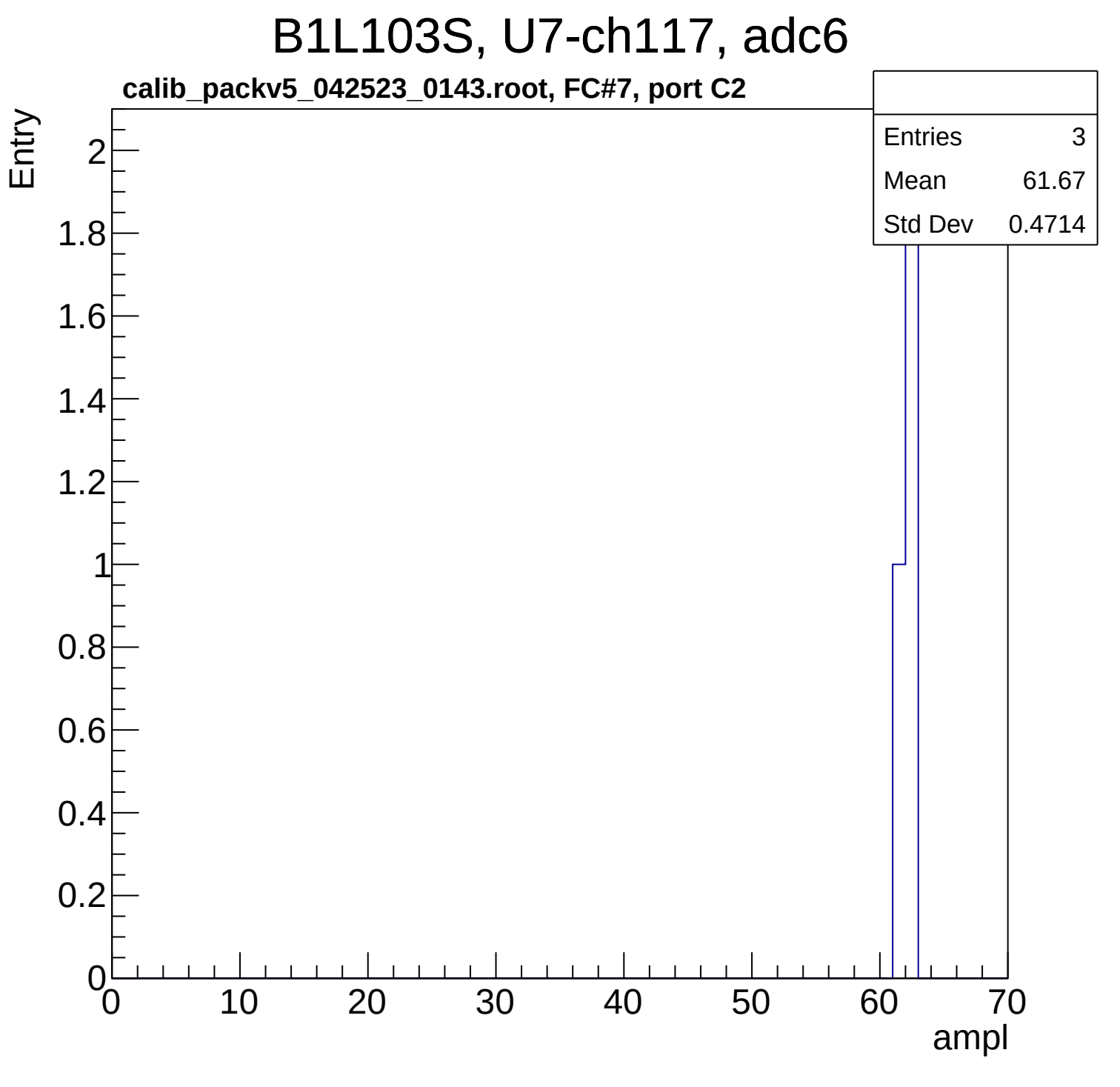
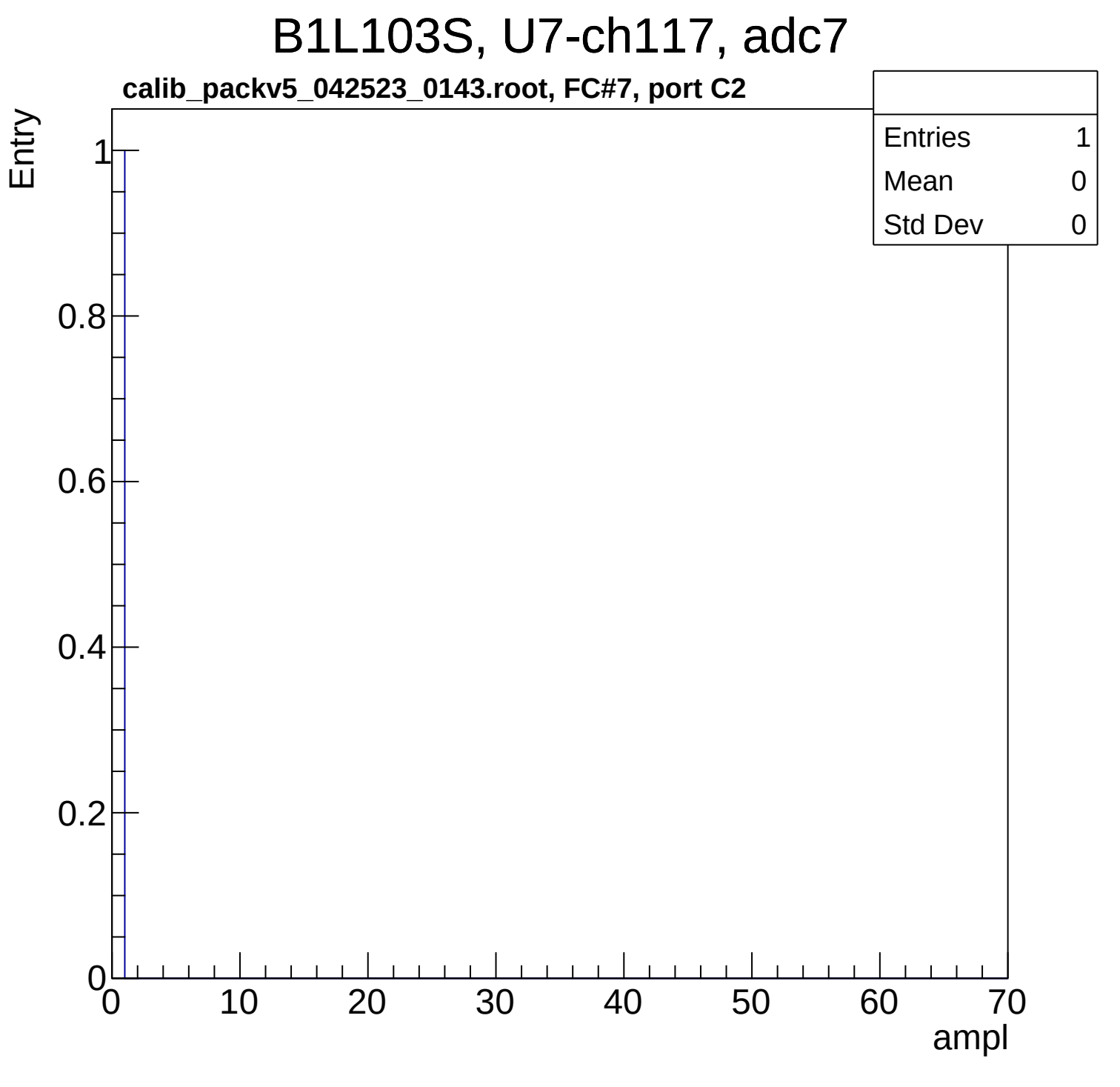
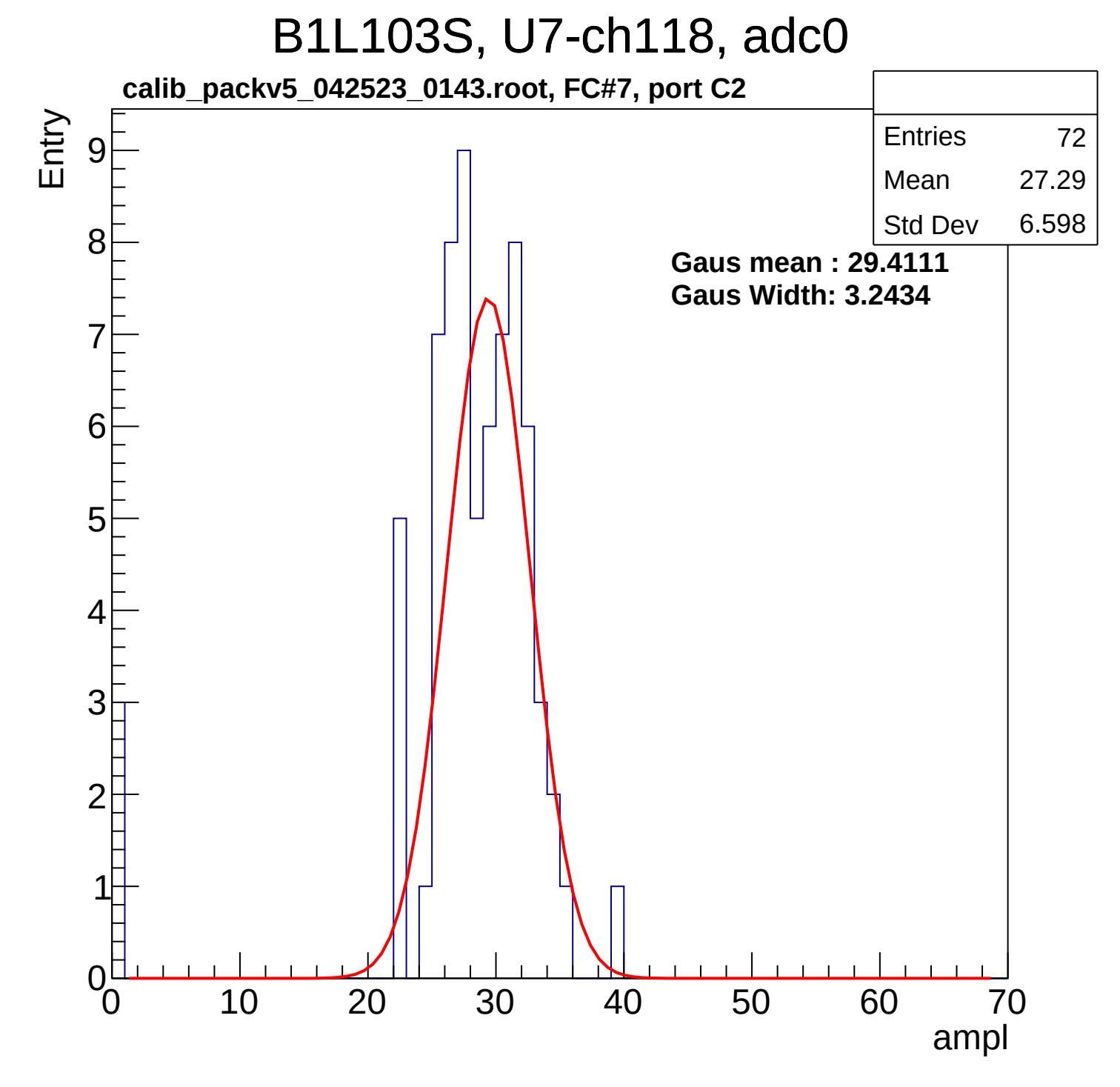
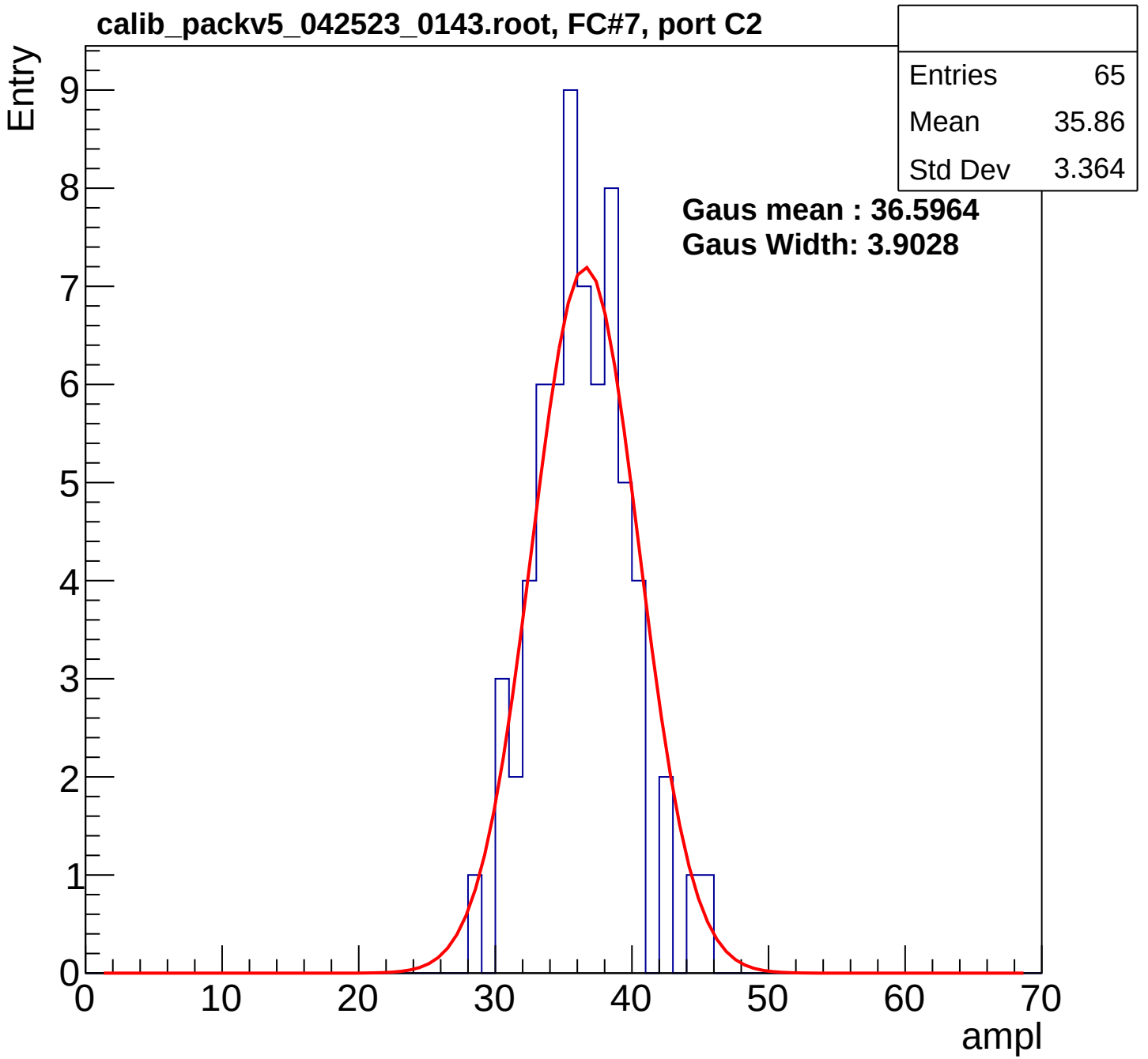
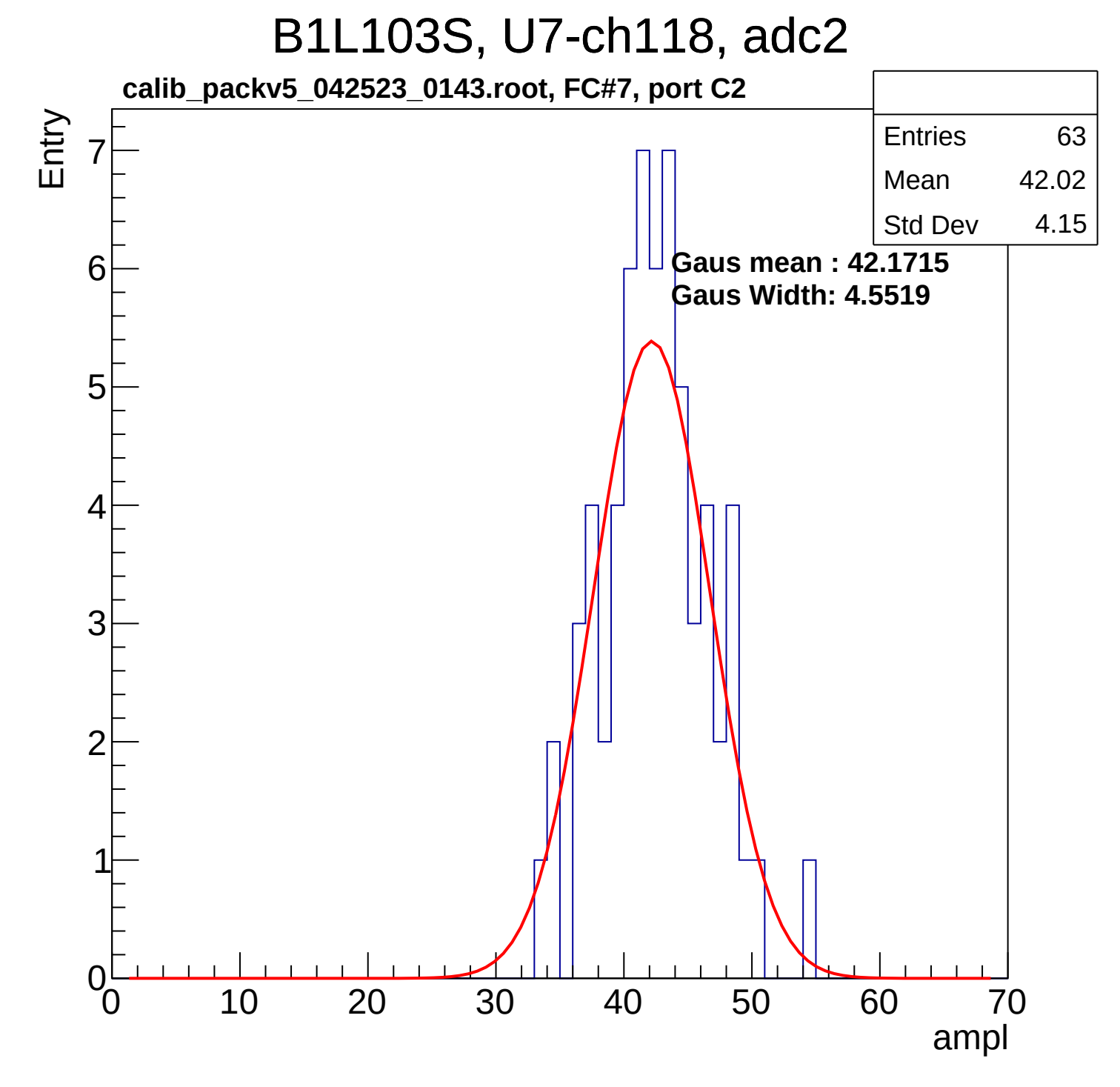
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

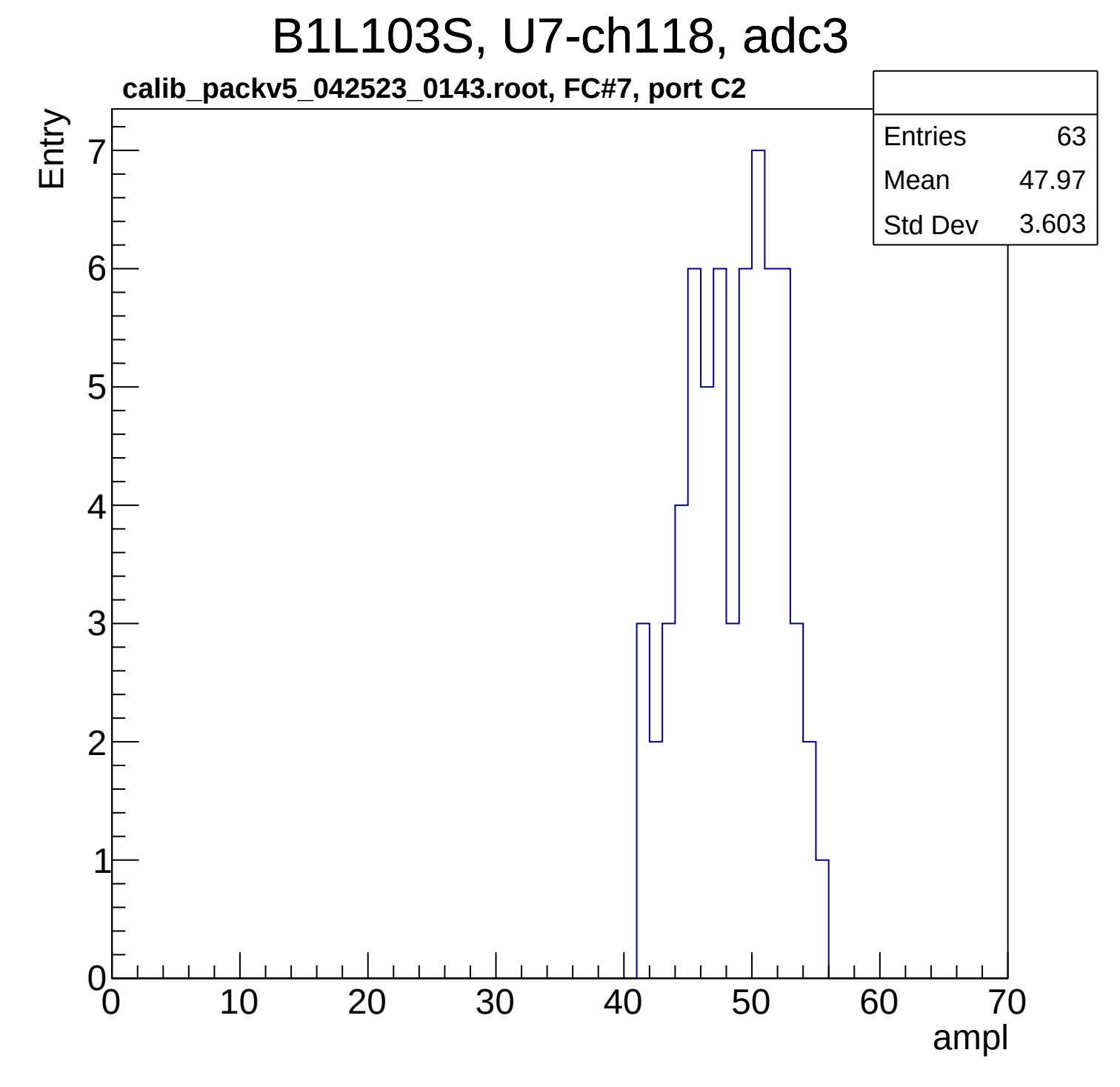

B1L103S, U7-ch117, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 61.67
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

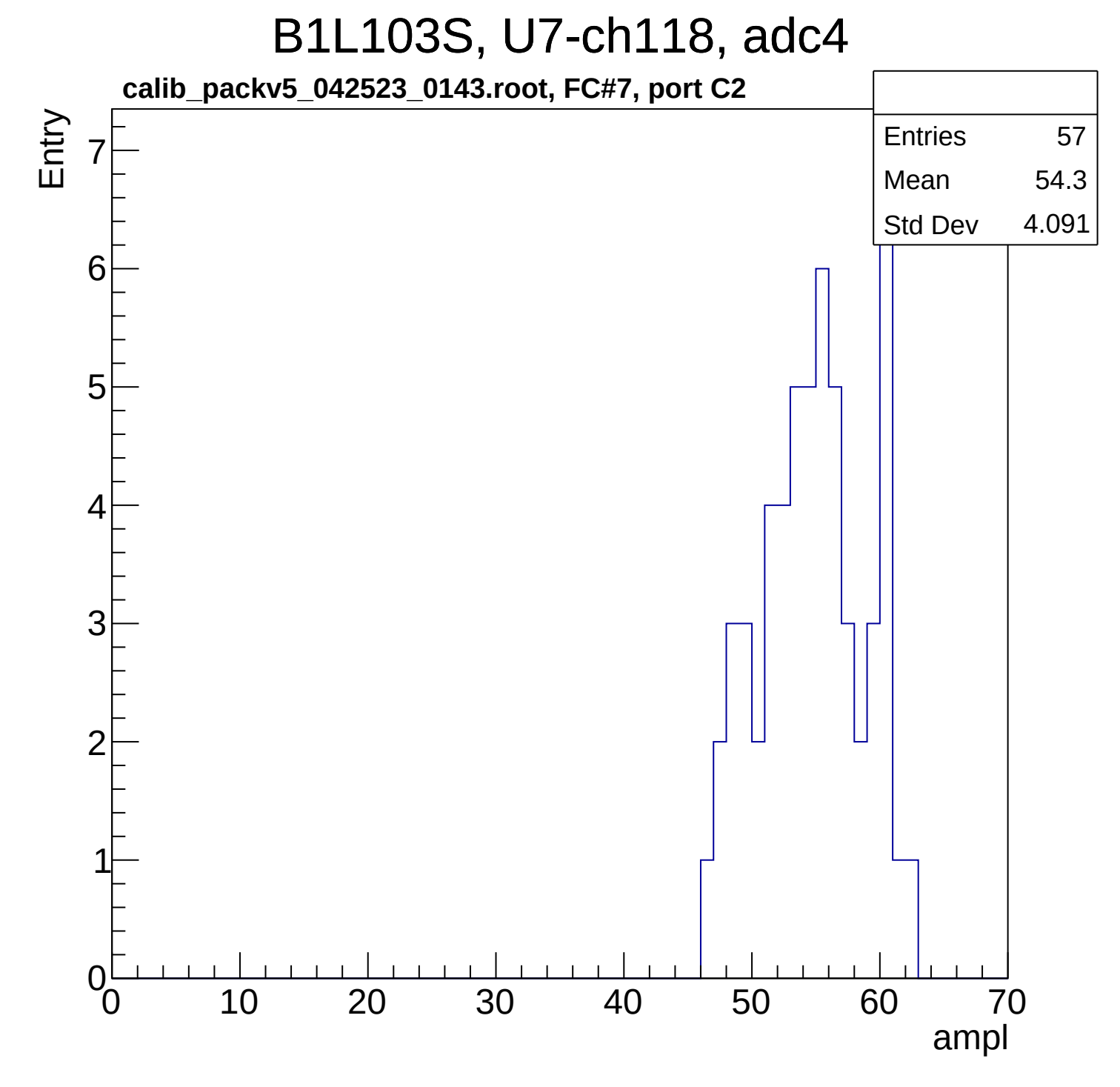

B1L103S, U7-ch117, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

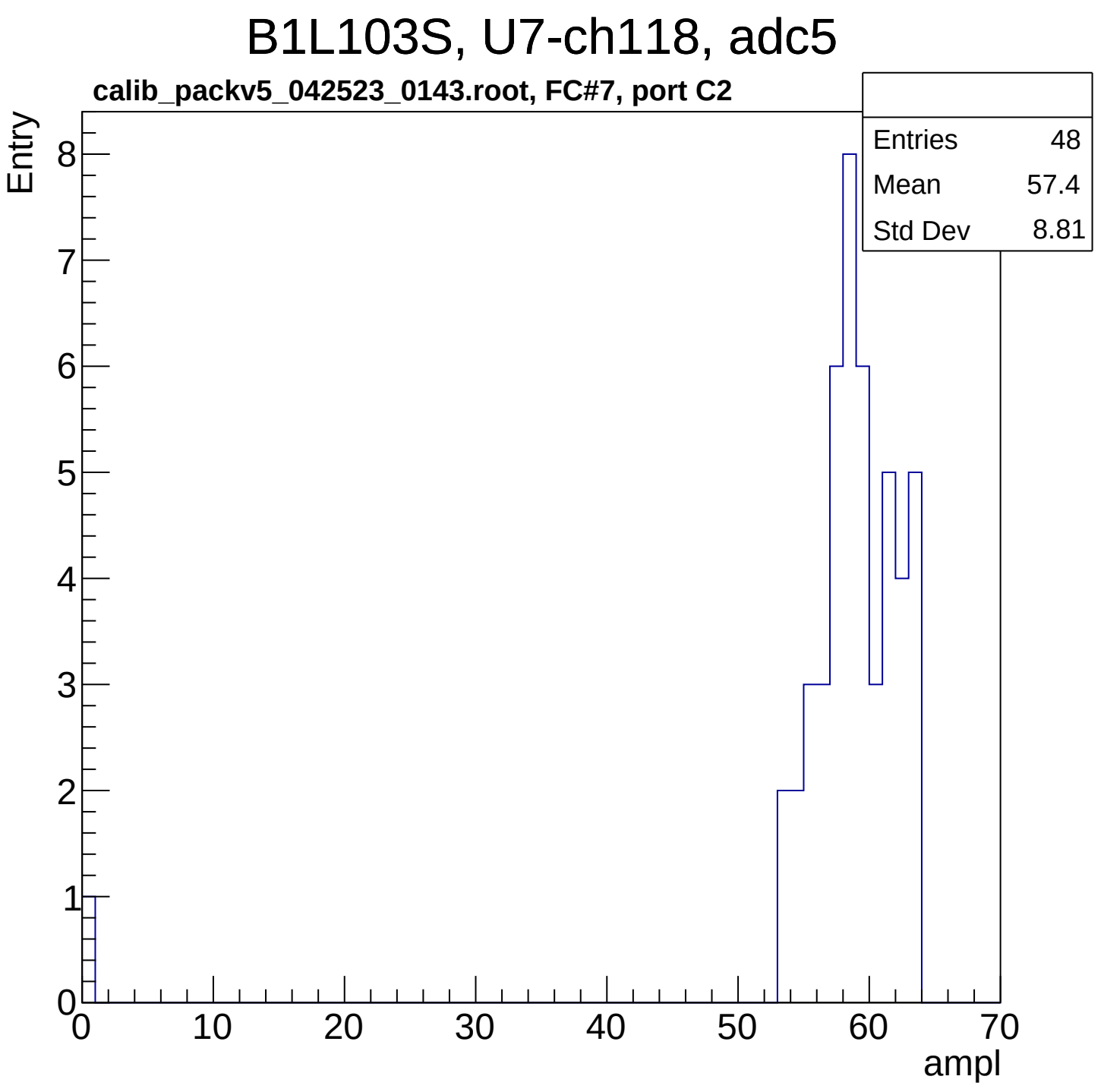

B1L103S, U7-ch118, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 72
Mean 27.29
Std Dev 6.598
Gaus mean : 29.4111
Gaus Width: 3.2434
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

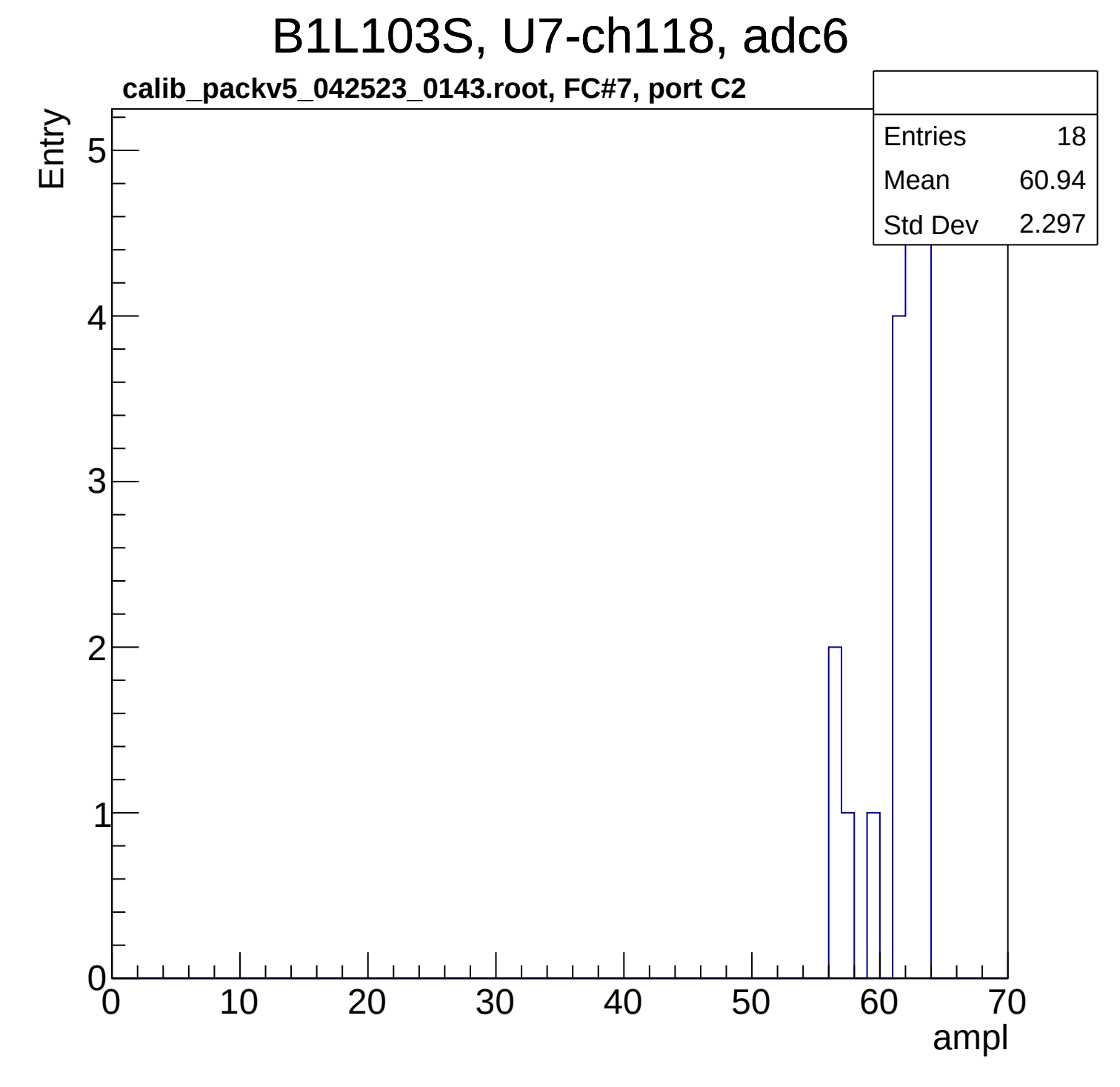

B1L103S, U7-ch118, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 35.86
Std Dev 3.364
Gaus mean : 36.5964
Gaus Width: 3.9028
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

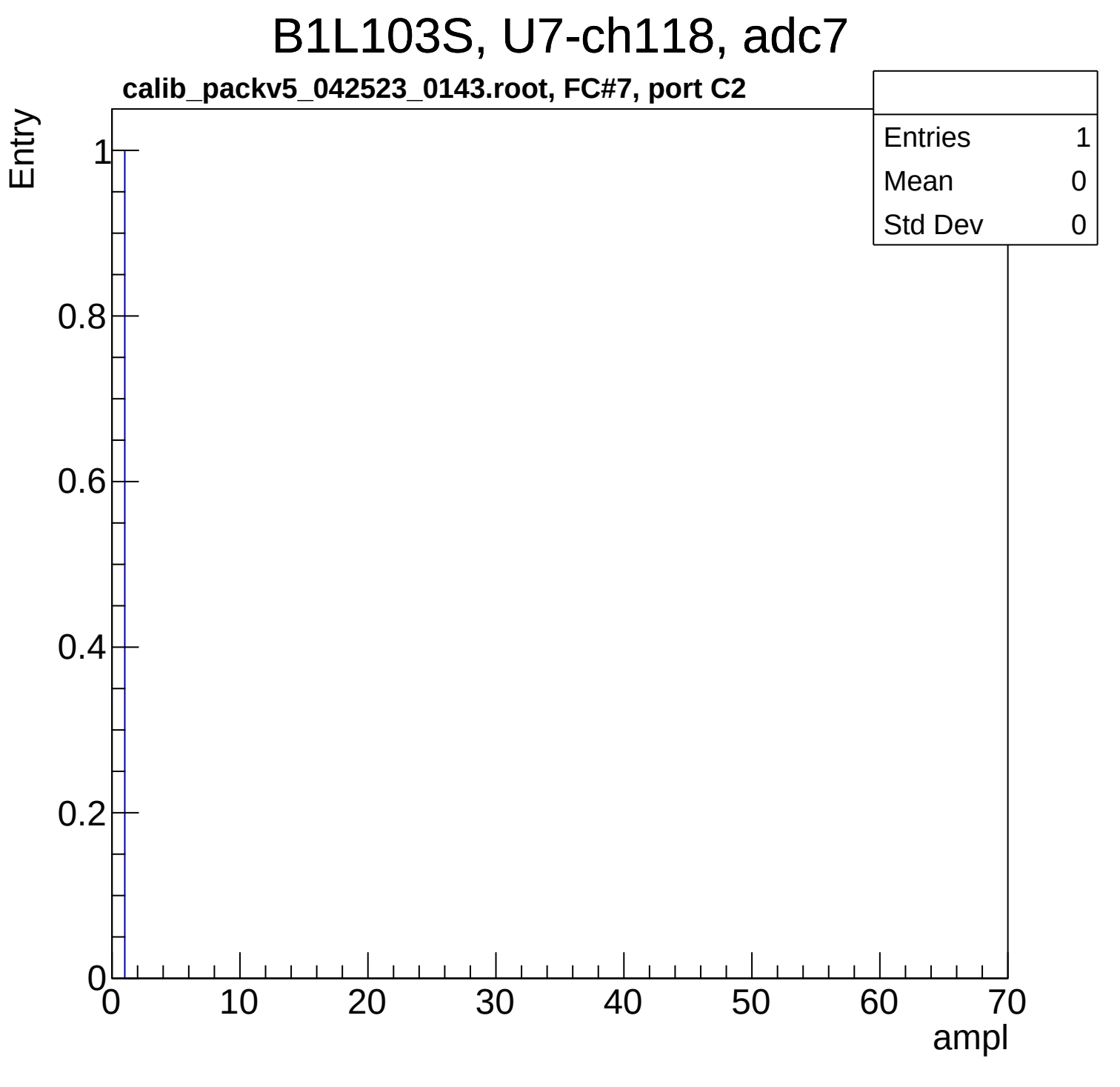

B1L103S, U7-ch118, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 42.02
Std Dev 4.15
Gaus mean : 42.1715
Gaus Width: 4.5519
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

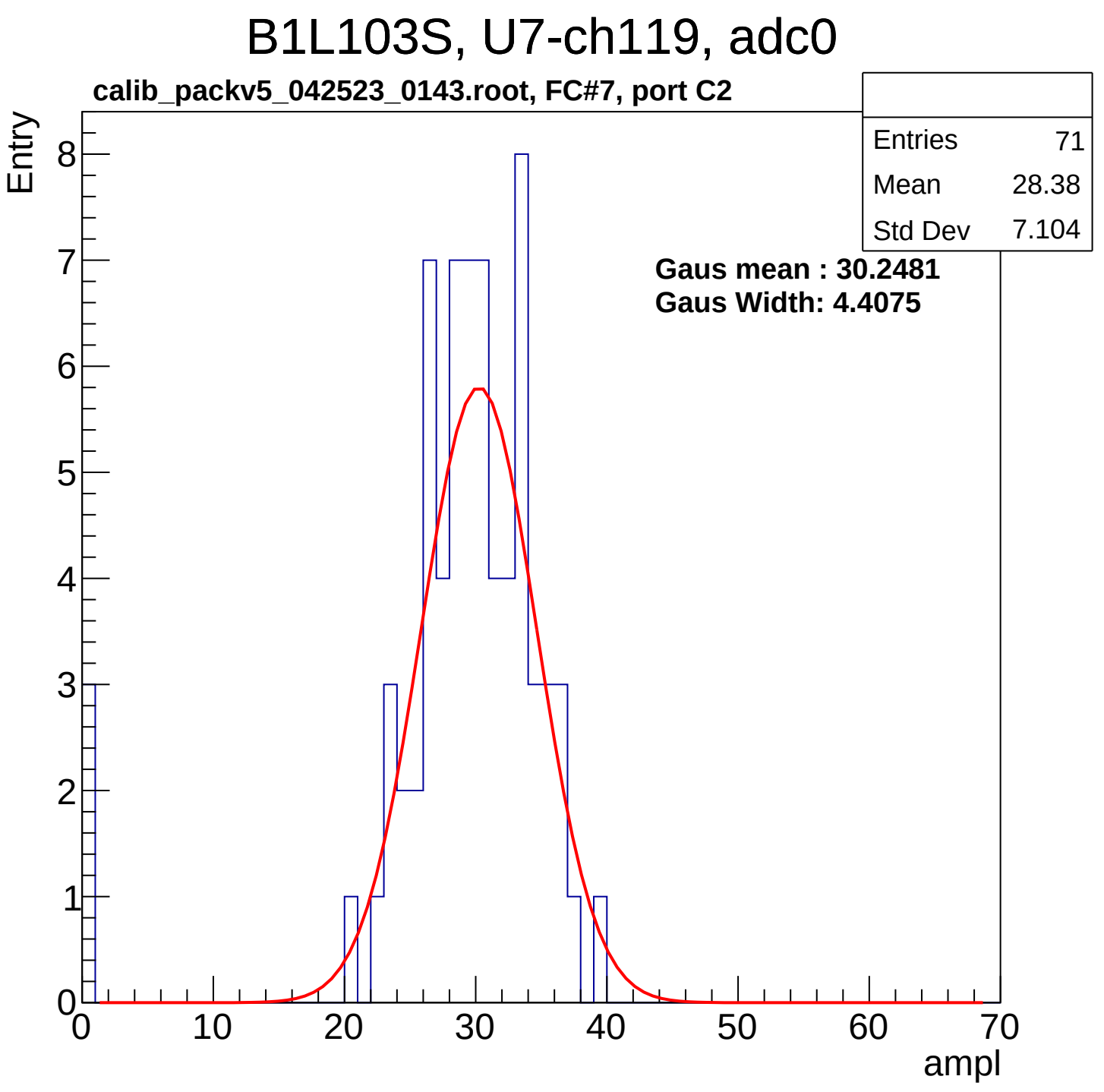

B1L103S, U7-ch118, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 47.97
Std Dev 3.603
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch118, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 54.3
Std Dev 4.091
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch118, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 48
Mean 57.4
Std Dev 8.81
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch118, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 18
Mean 60.94
Std Dev 2.297
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U7-ch118, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch119, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 71
Mean 28.38
Std Dev 7.104
Gaus mean : 30.2481
Gaus Width: 4.4075
Entry
ampl
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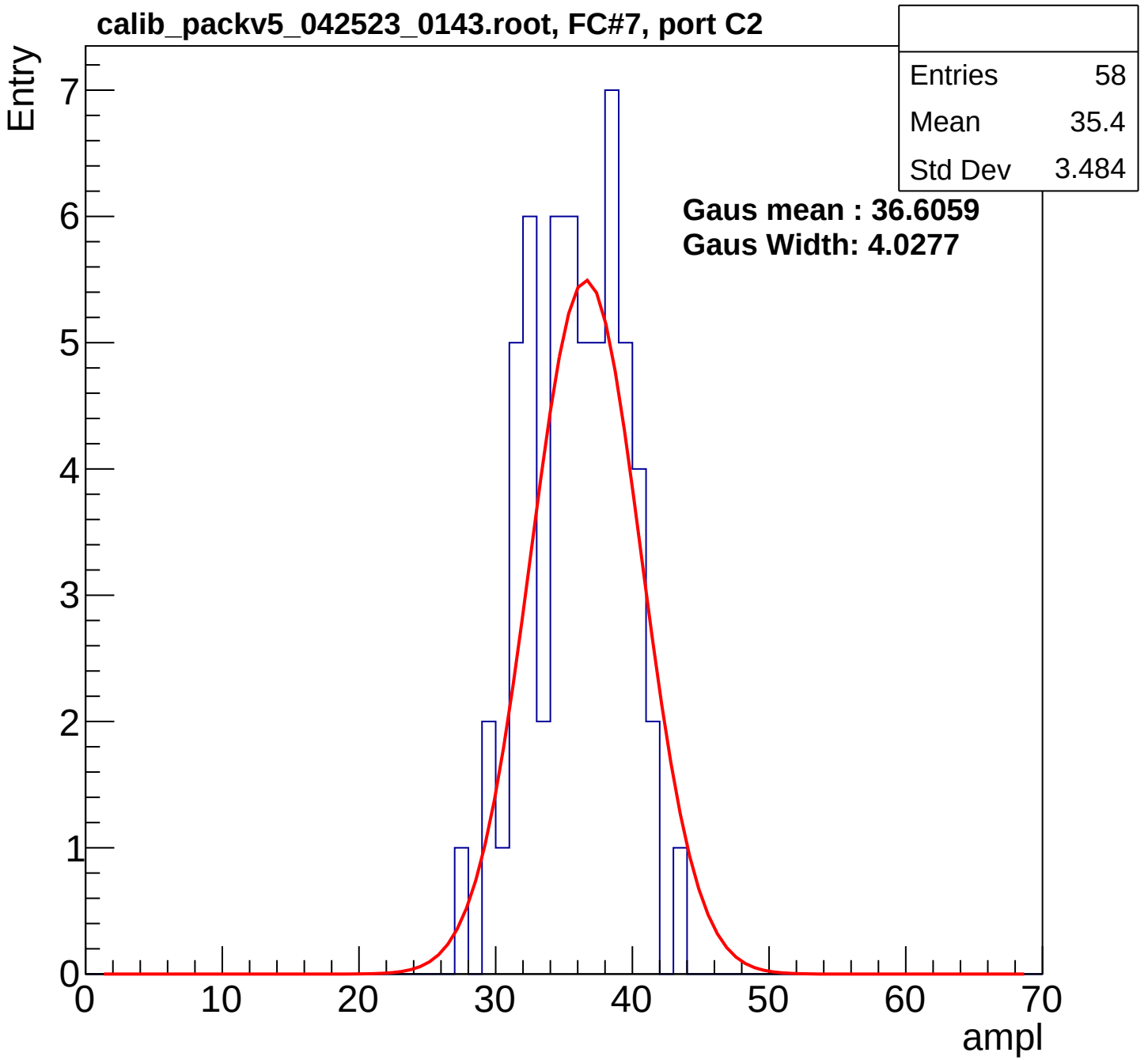
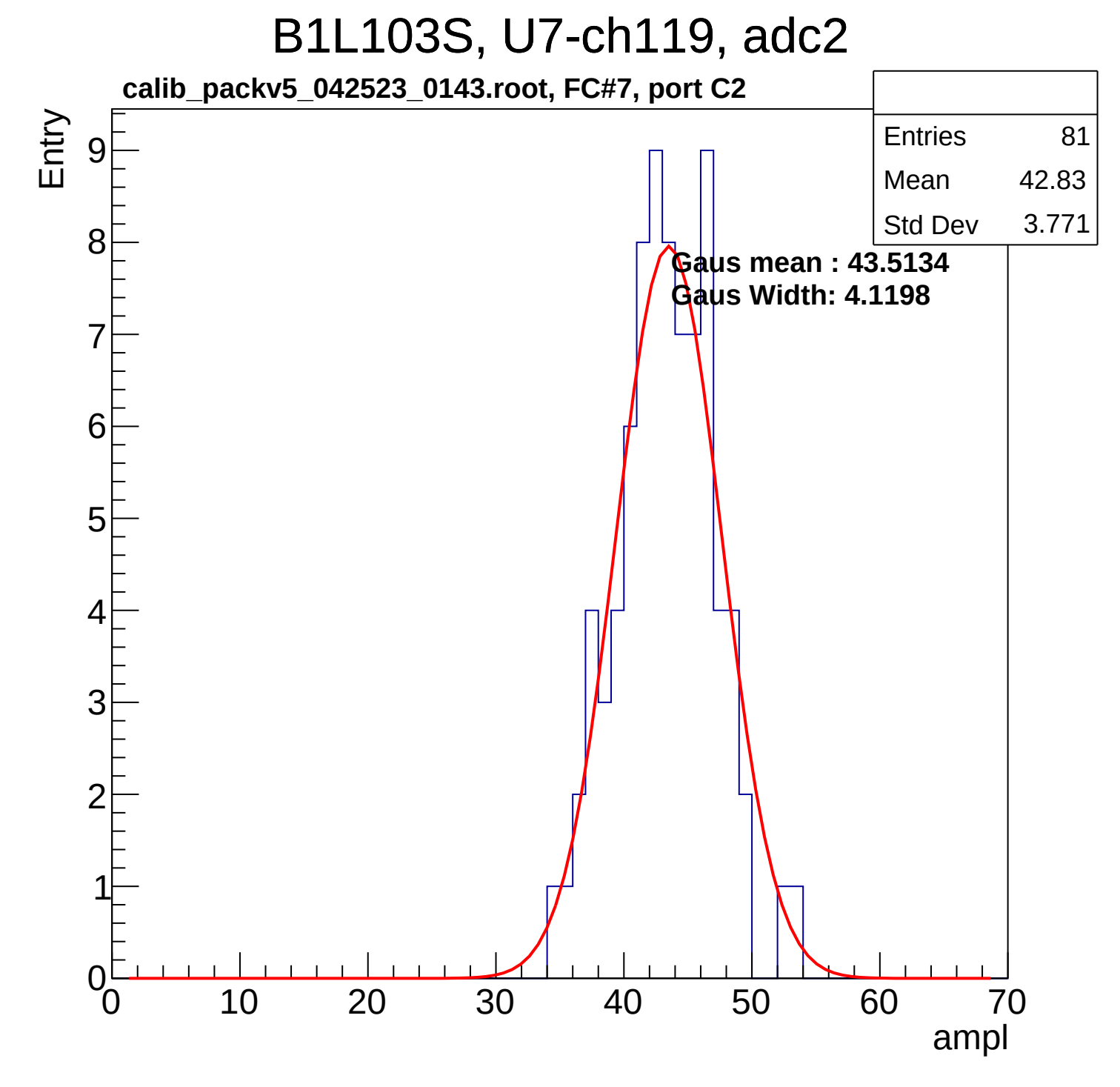
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch119, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 58
Mean 35.4
Std Dev 3.484
Gaus mean : 36.6059
Gaus Width: 4.0277
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch119, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 81
Mean 42.83
Std Dev 3.771
Gaus mean : 43.5134
Gaus Width: 4.1198
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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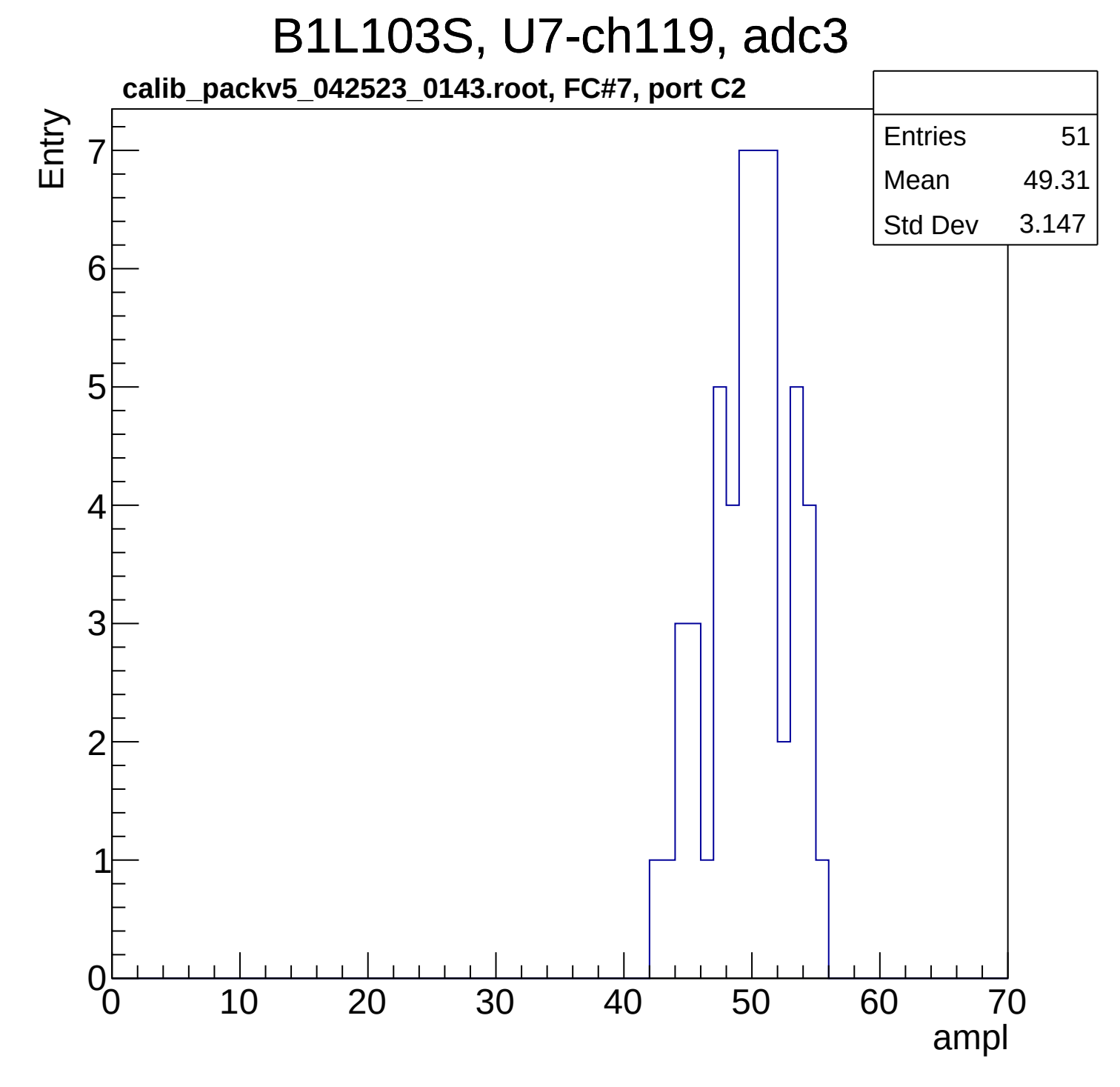
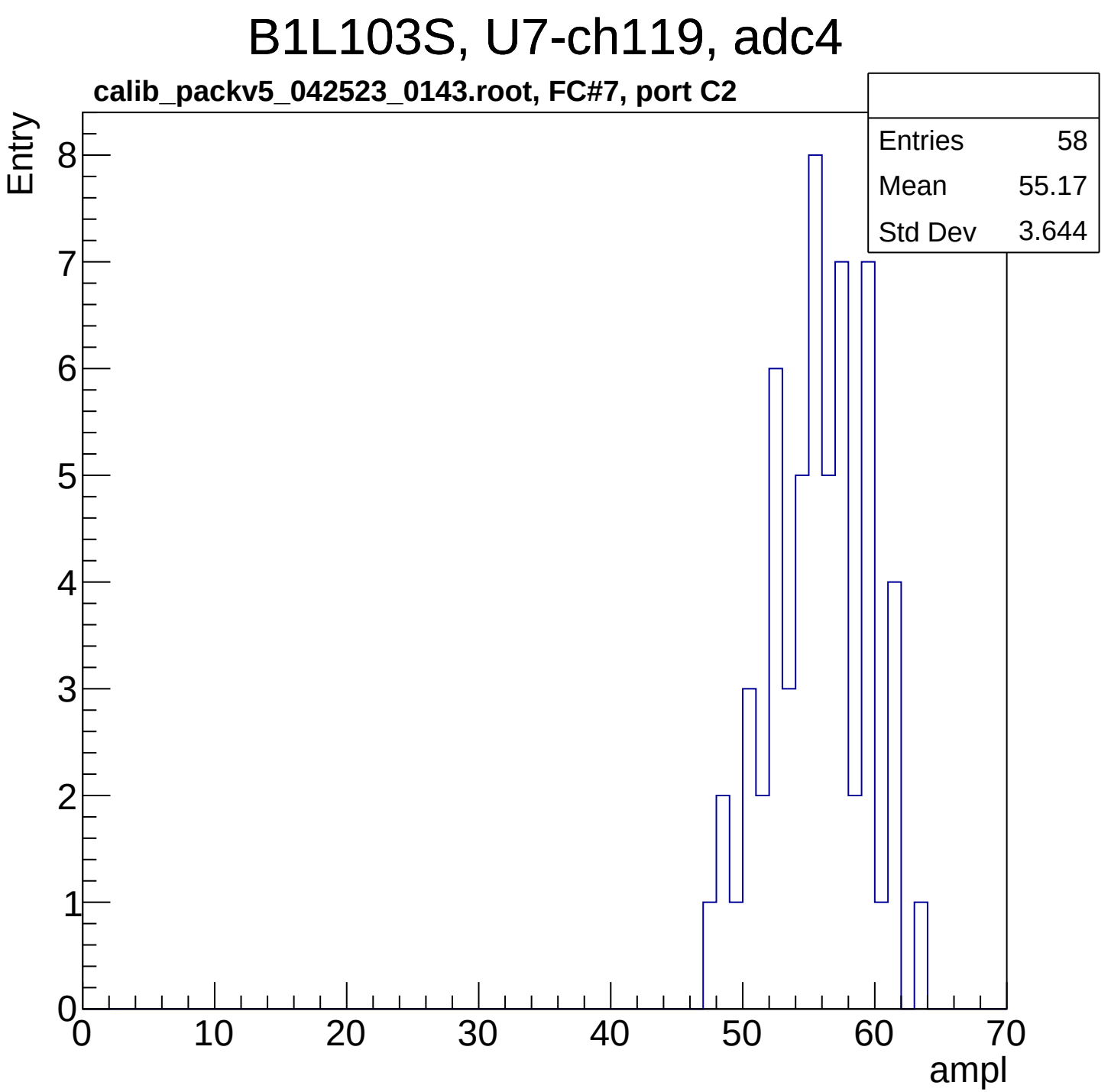
40
50
60
70


B1L103S, U7-ch119, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 51
Mean 49.31
Std Dev 3.147
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch119, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 58
Mean 55.17
Std Dev 3.644
Entry
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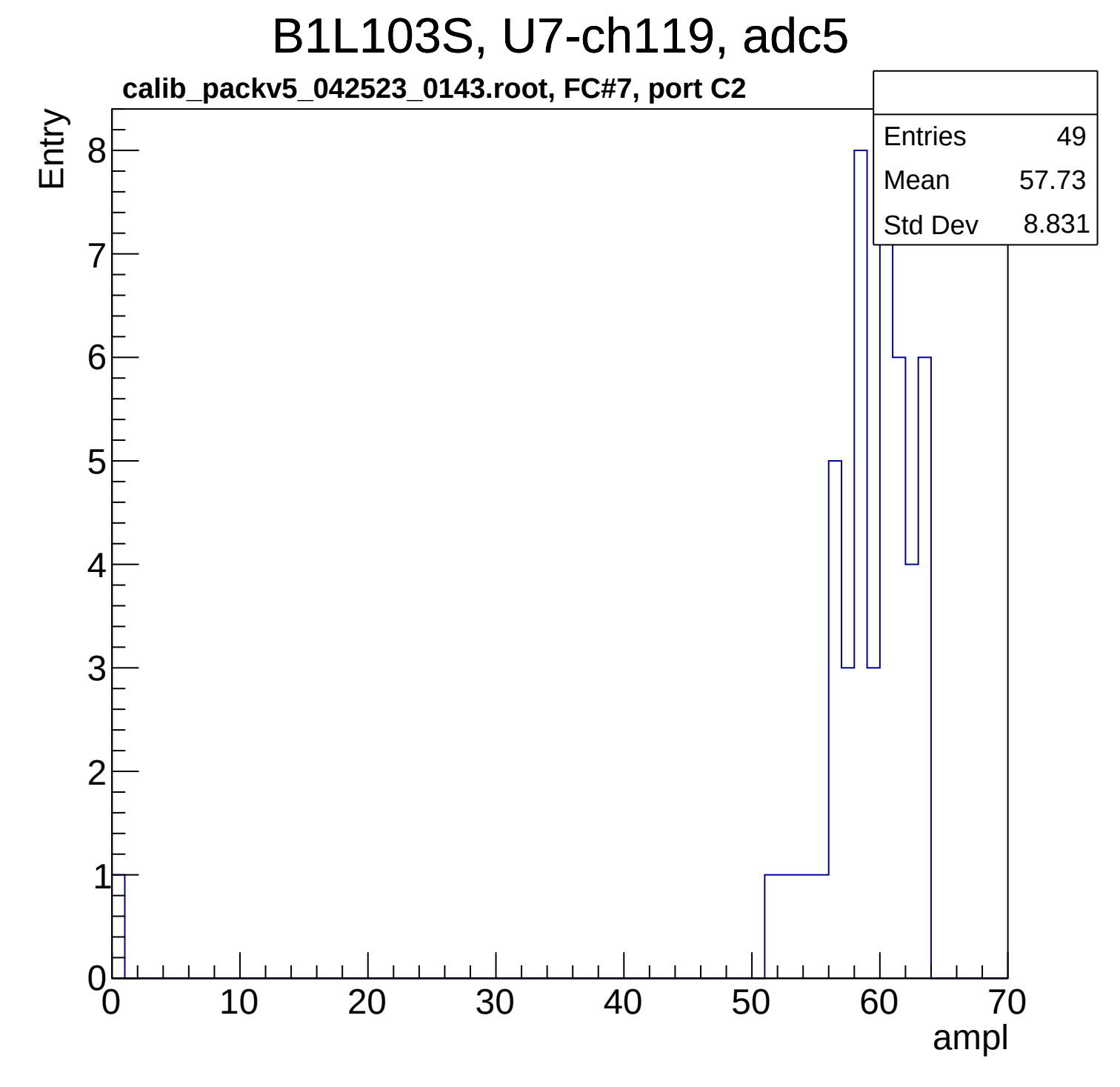
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch119, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 49
Mean 57.73
Std Dev 8.831
Entry
ampl
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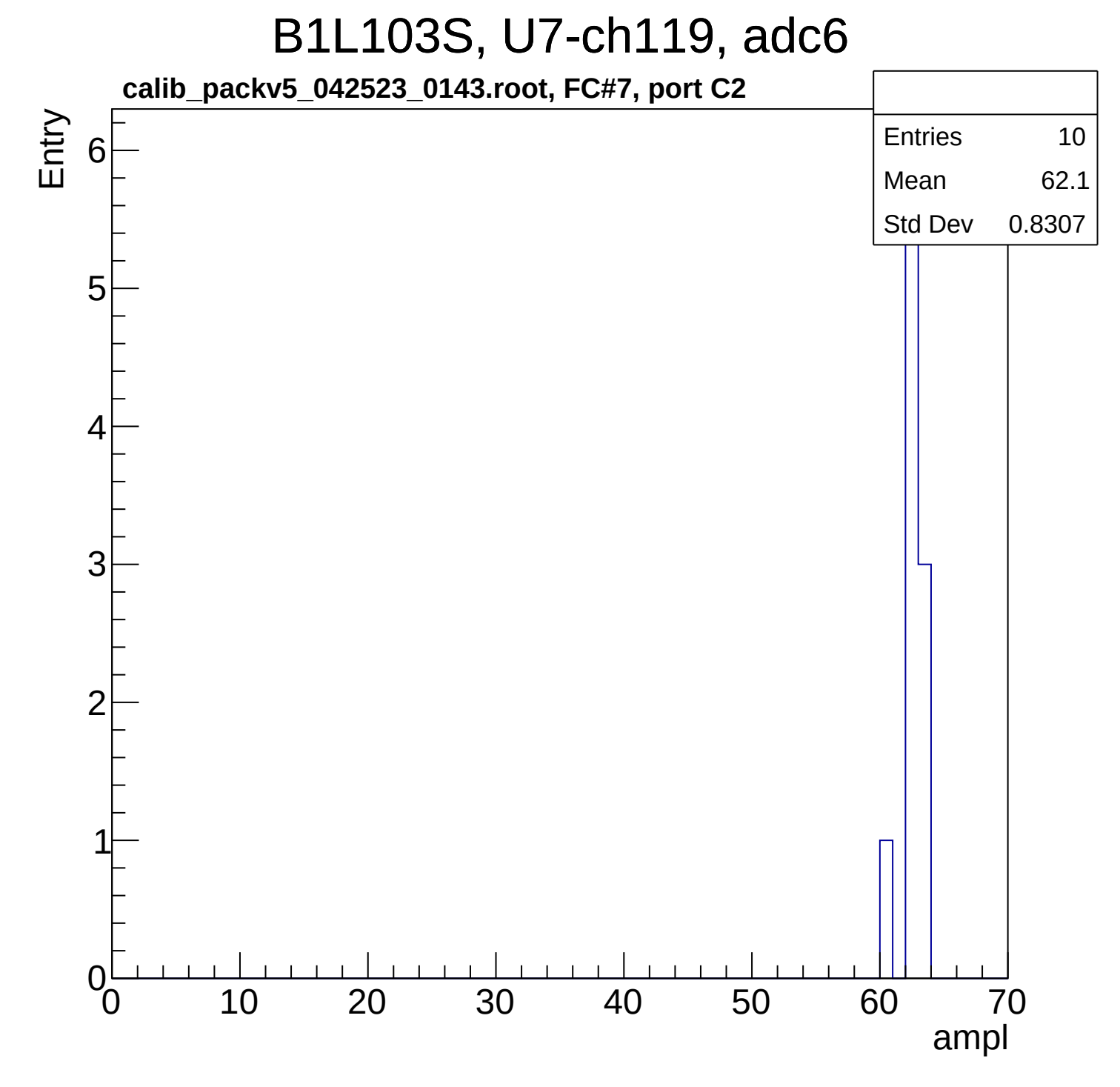
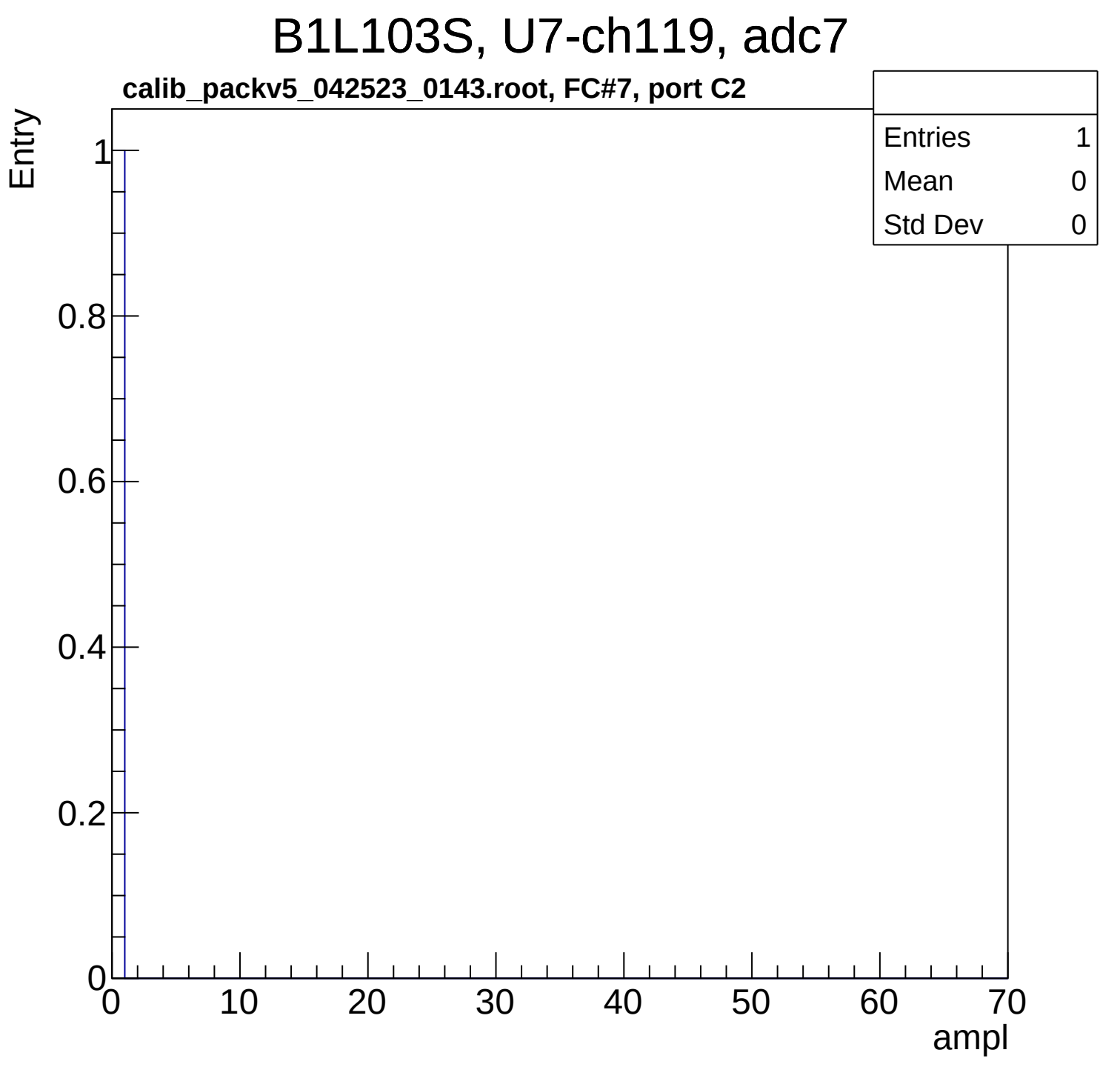
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch119, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 10
Mean 62.1
Std Dev 0.8307
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch119, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
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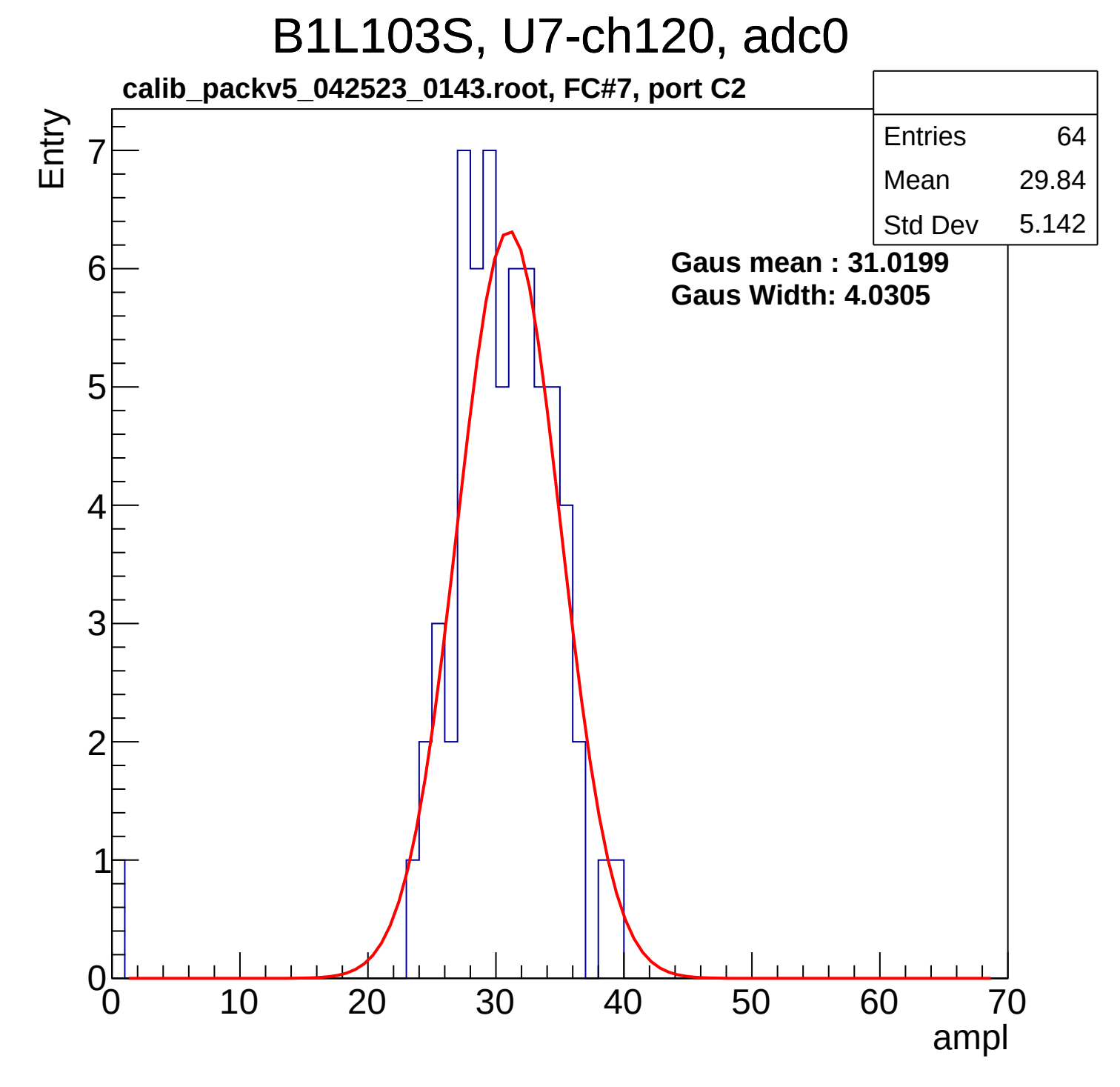
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch120, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 29.84
Std Dev 5.142
Gaus mean : 31.0199
Gaus Width: 4.0305
Entry
ampl
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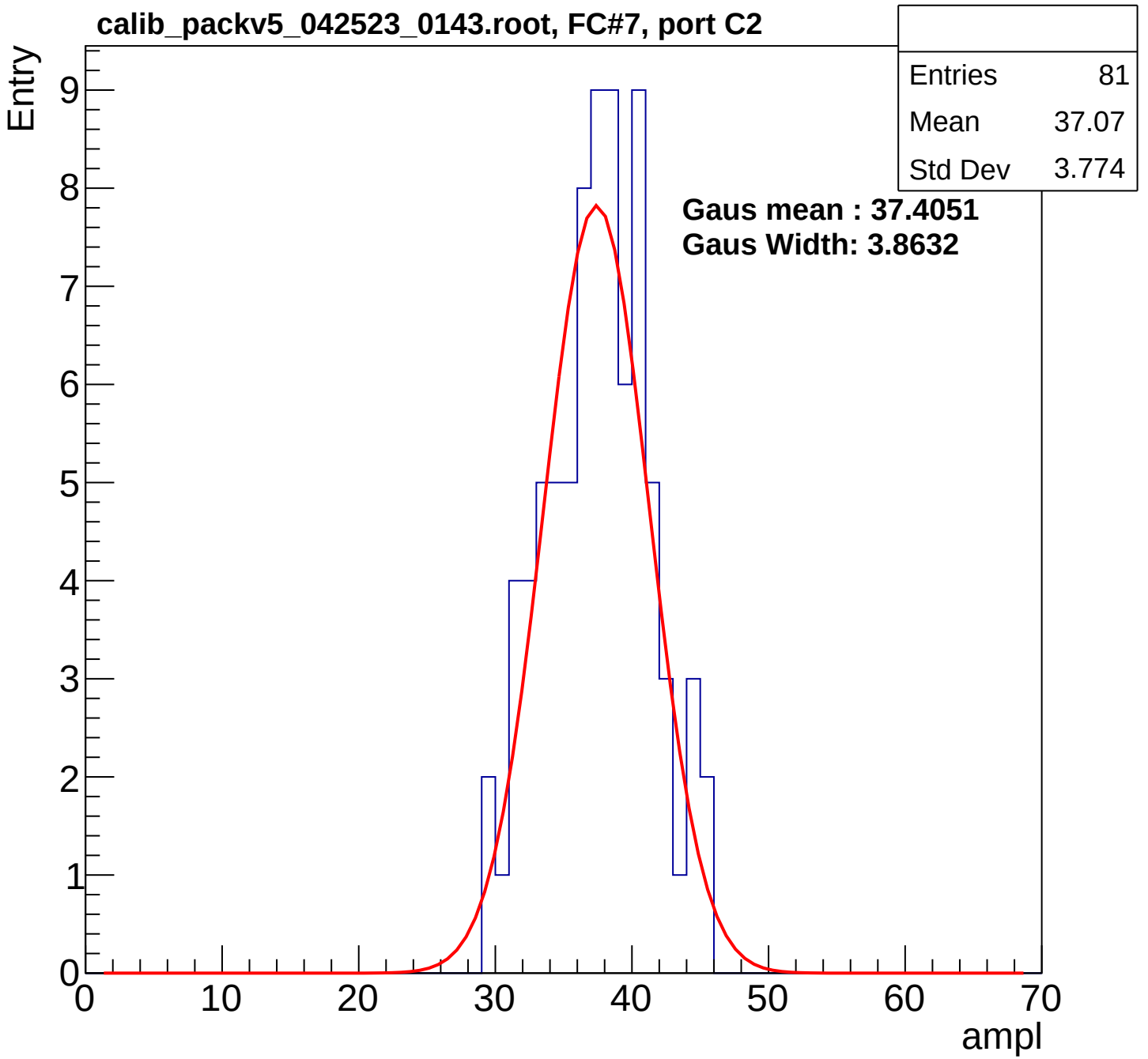
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch120, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 81
Mean 37.07
Std Dev 3.774
Gaus mean : 37.4051
Gaus Width: 3.8632
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
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40
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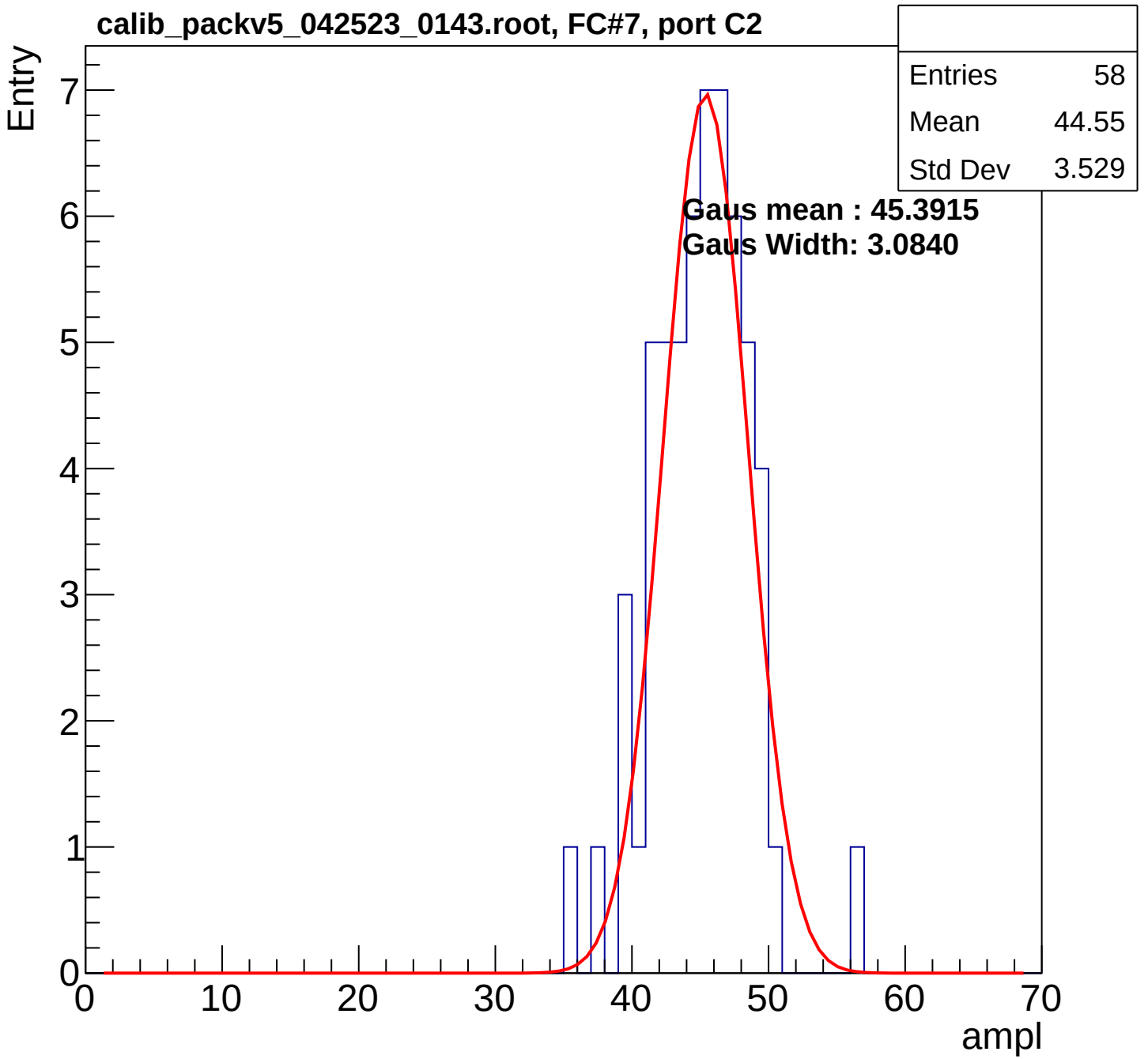
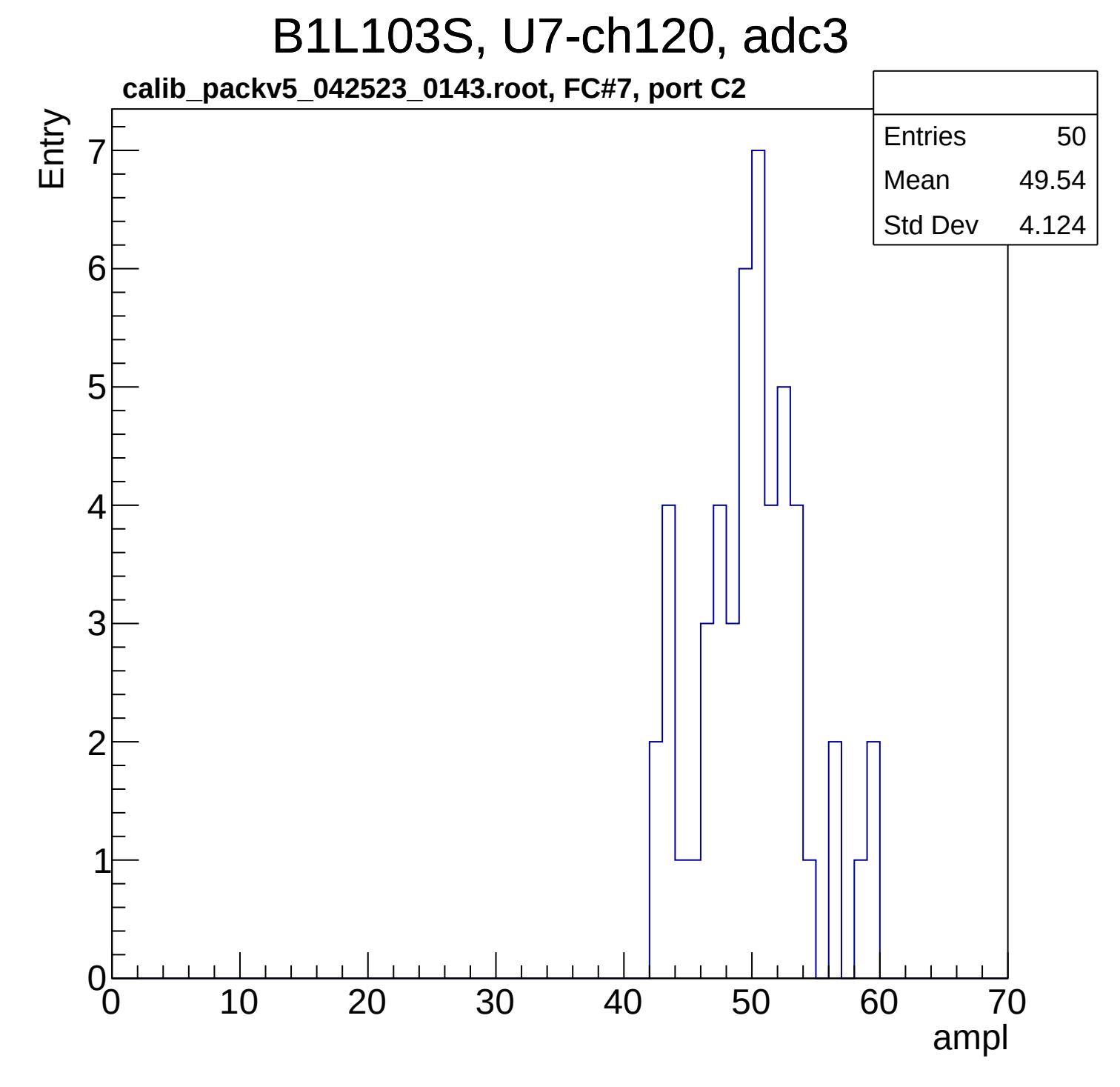

B1L103S, U7-ch120, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 58
Mean 44.55
Std Dev 3.529
Gaus mean : 45.3915
Gaus Width: 3.0840
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch120, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 50
Mean 49.54
Std Dev 4.124
Entry
ampl
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3
4
5
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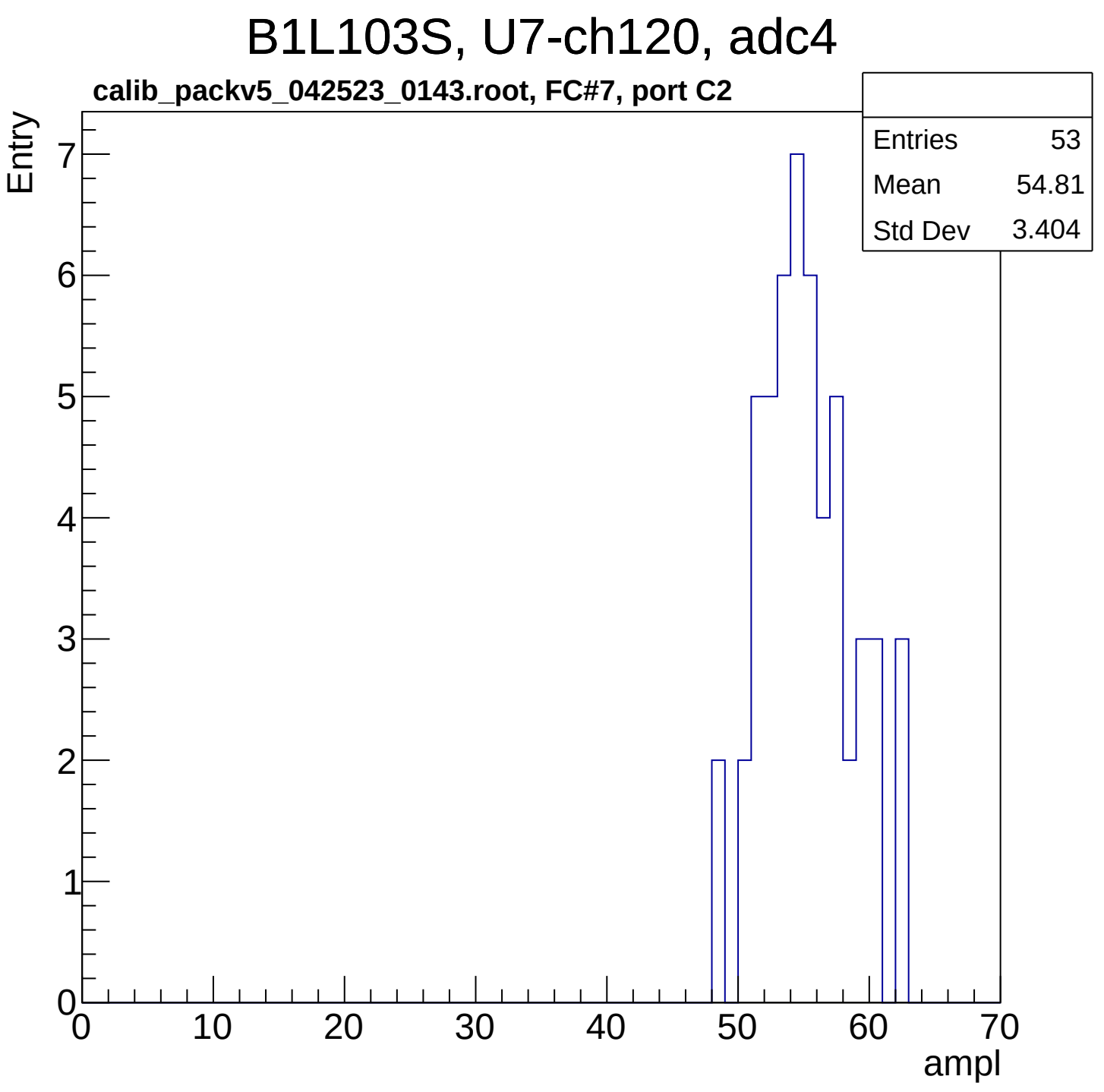
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch120, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 54.81
Std Dev 3.404
Entry
ampl
0
1
2
3
4
5
6
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0
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20
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60
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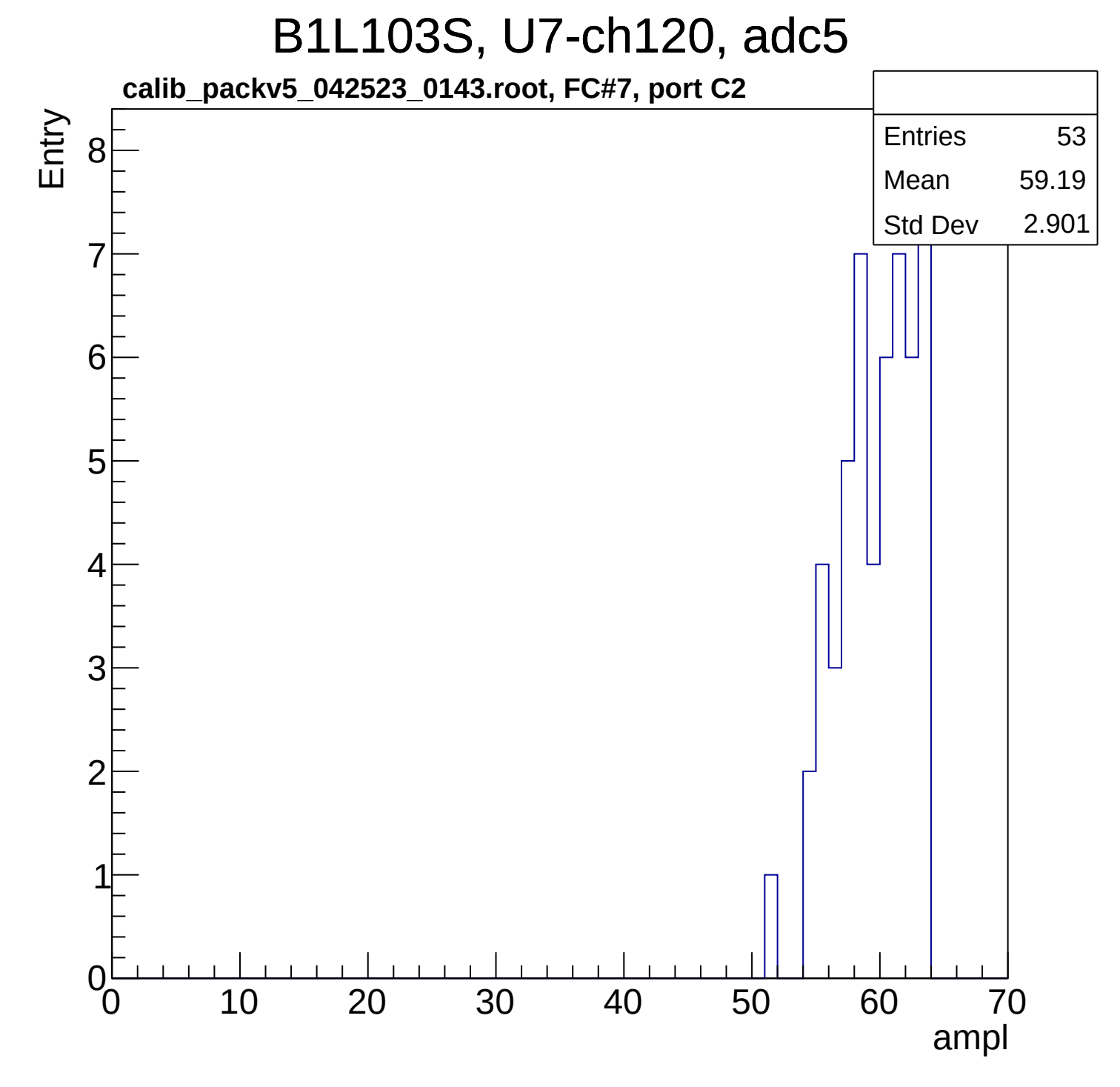
B1L103S, U7-ch120, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 59.19
Std Dev 2.901
Entry
ampl
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40
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60
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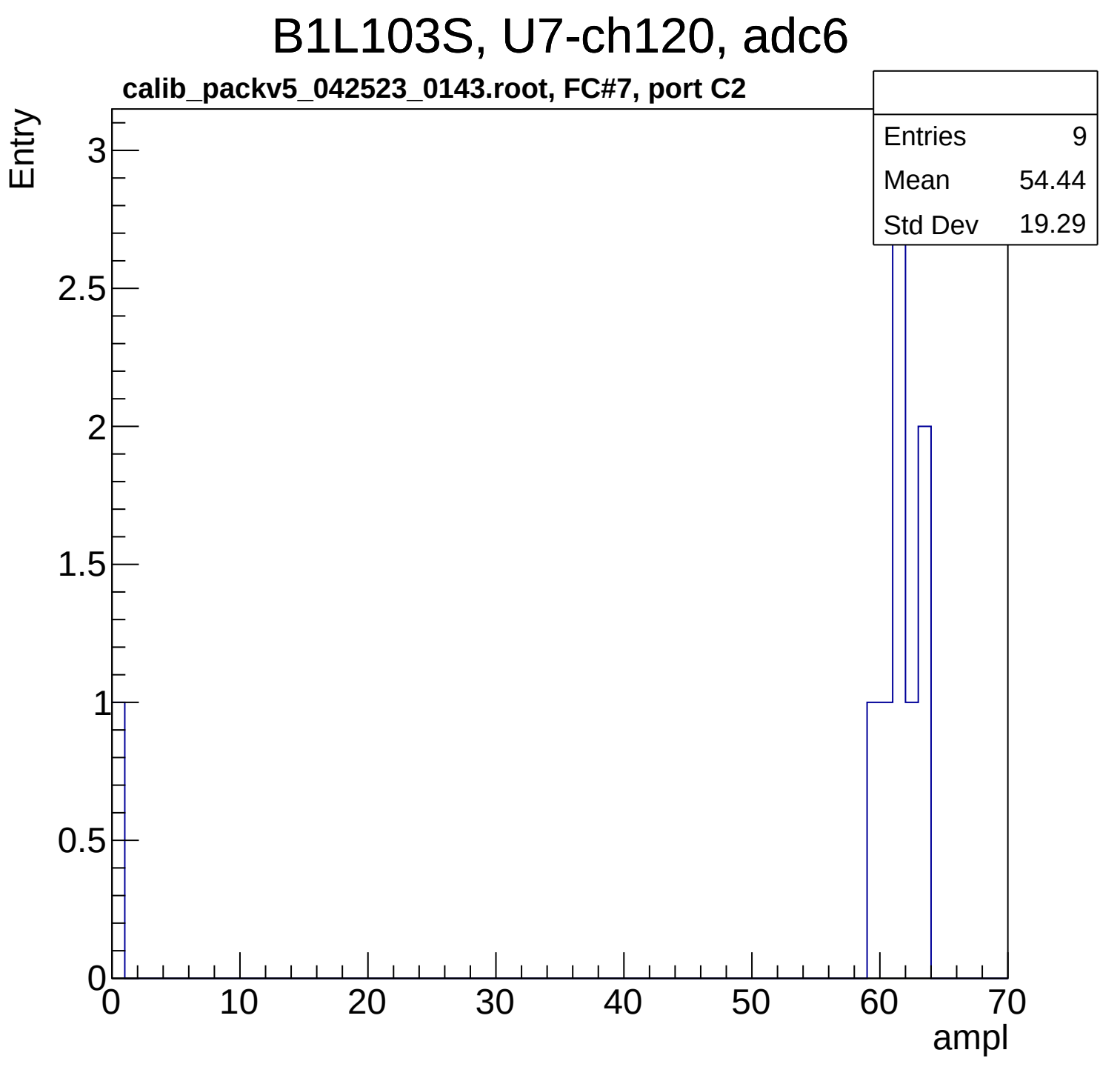
B1L103S, U7-ch120, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 9
Mean 54.44
Std Dev 19.29
Entry
ampl
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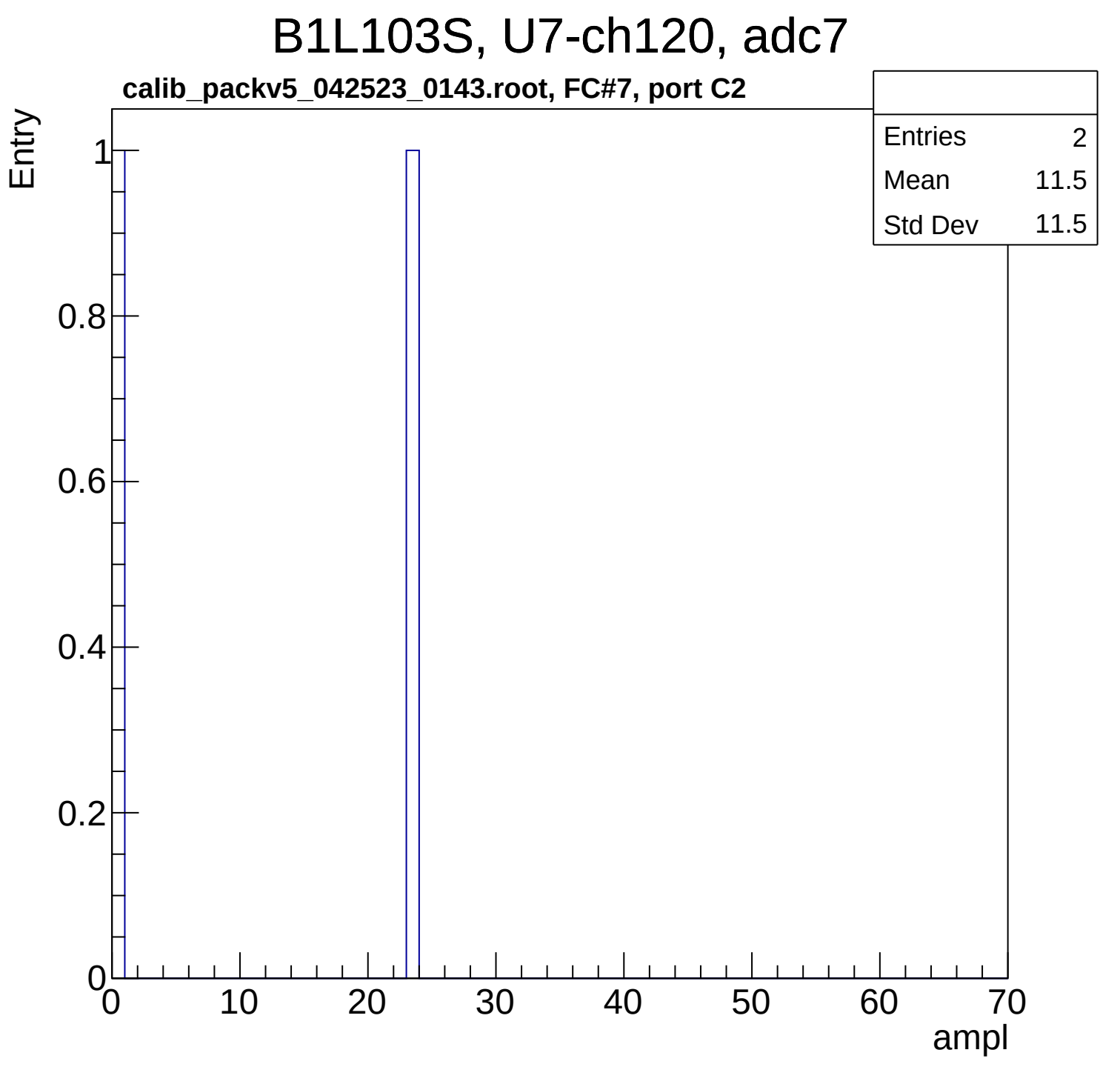
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U7-ch120, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 11.5
Std Dev 11.5
Entry
1
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0.6
0.4
0.2
0
0
10
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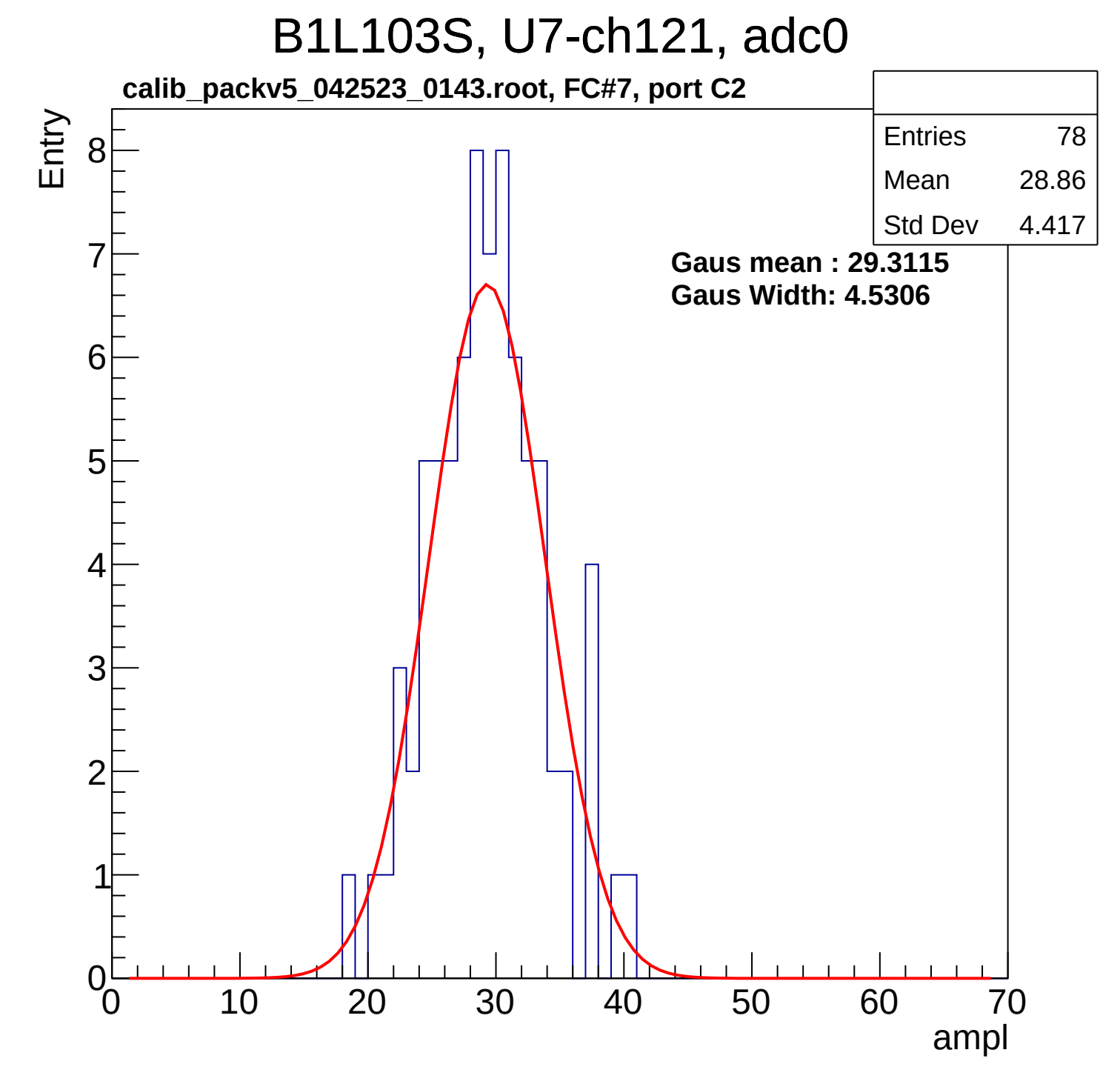
40
50
60
70
ampl


B1L103S, U7-ch121, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 78
Mean 28.86
Std Dev 4.417
Gaus mean : 29.3115
Gaus Width: 4.5306
Entry
ampl
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2
3
4
5
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7
8
0
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40
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60
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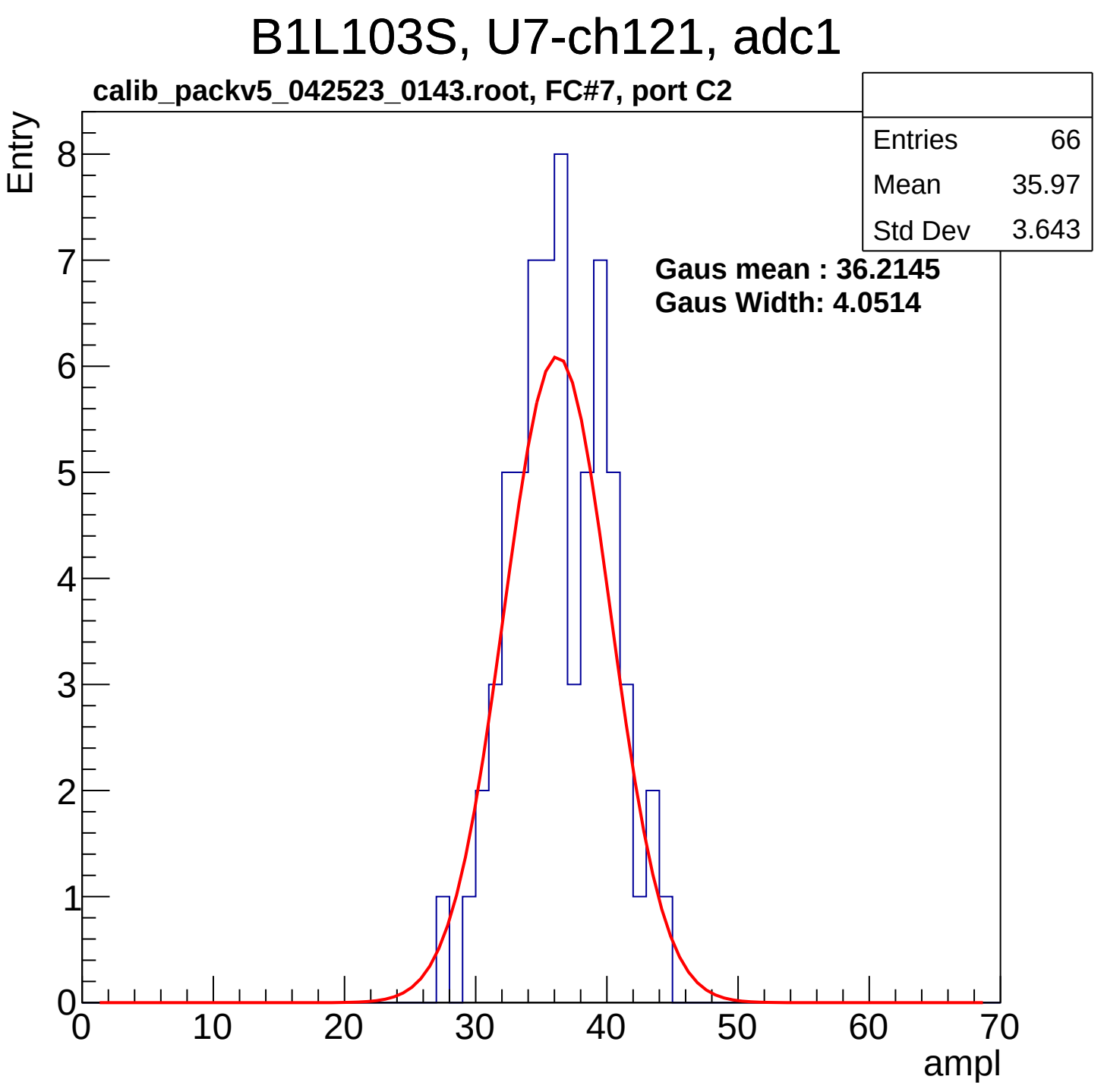
B1L103S, U7-ch121, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 35.97
Std Dev 3.643
Gaus mean : 36.2145
Gaus Width: 4.0514
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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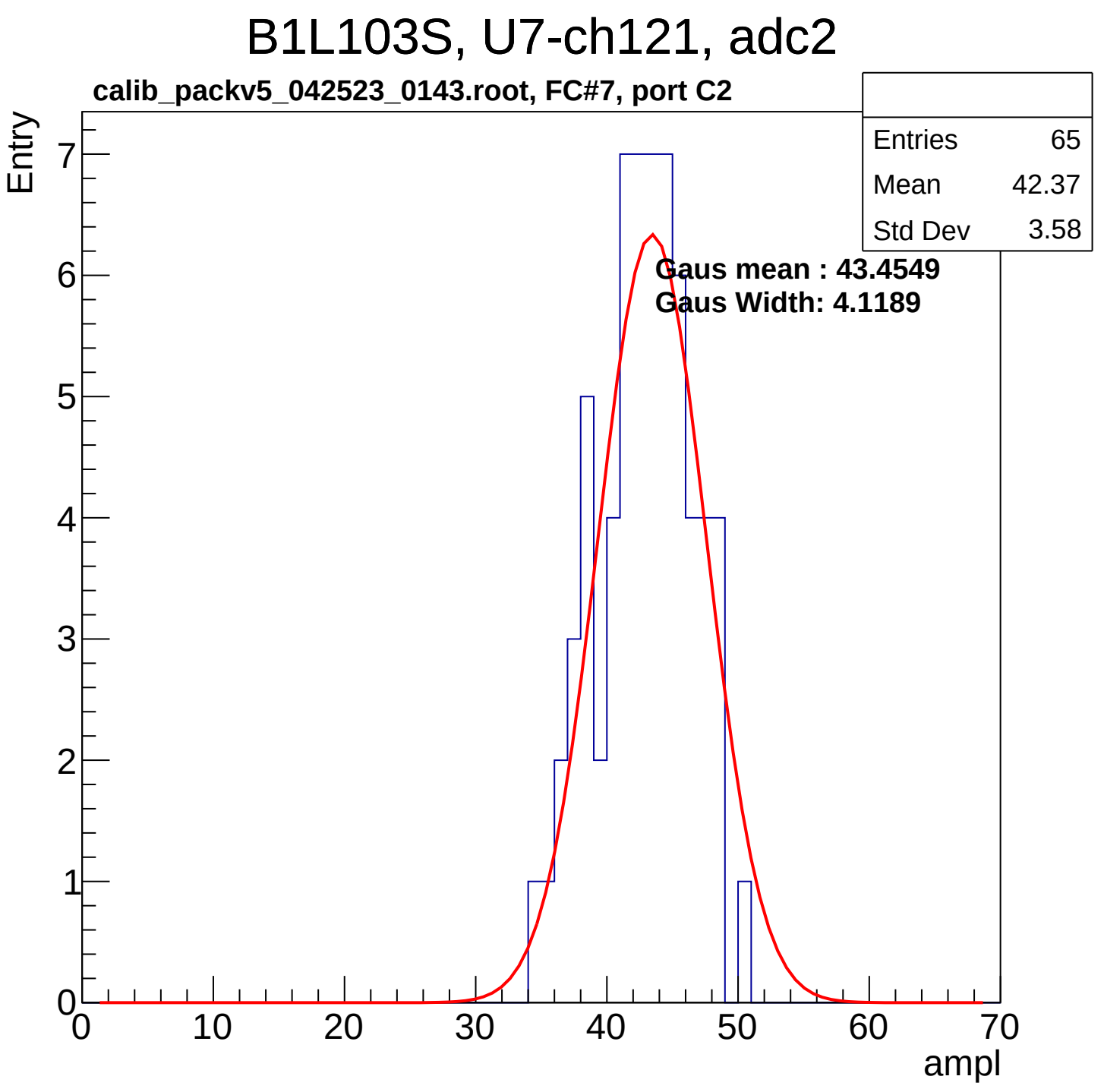
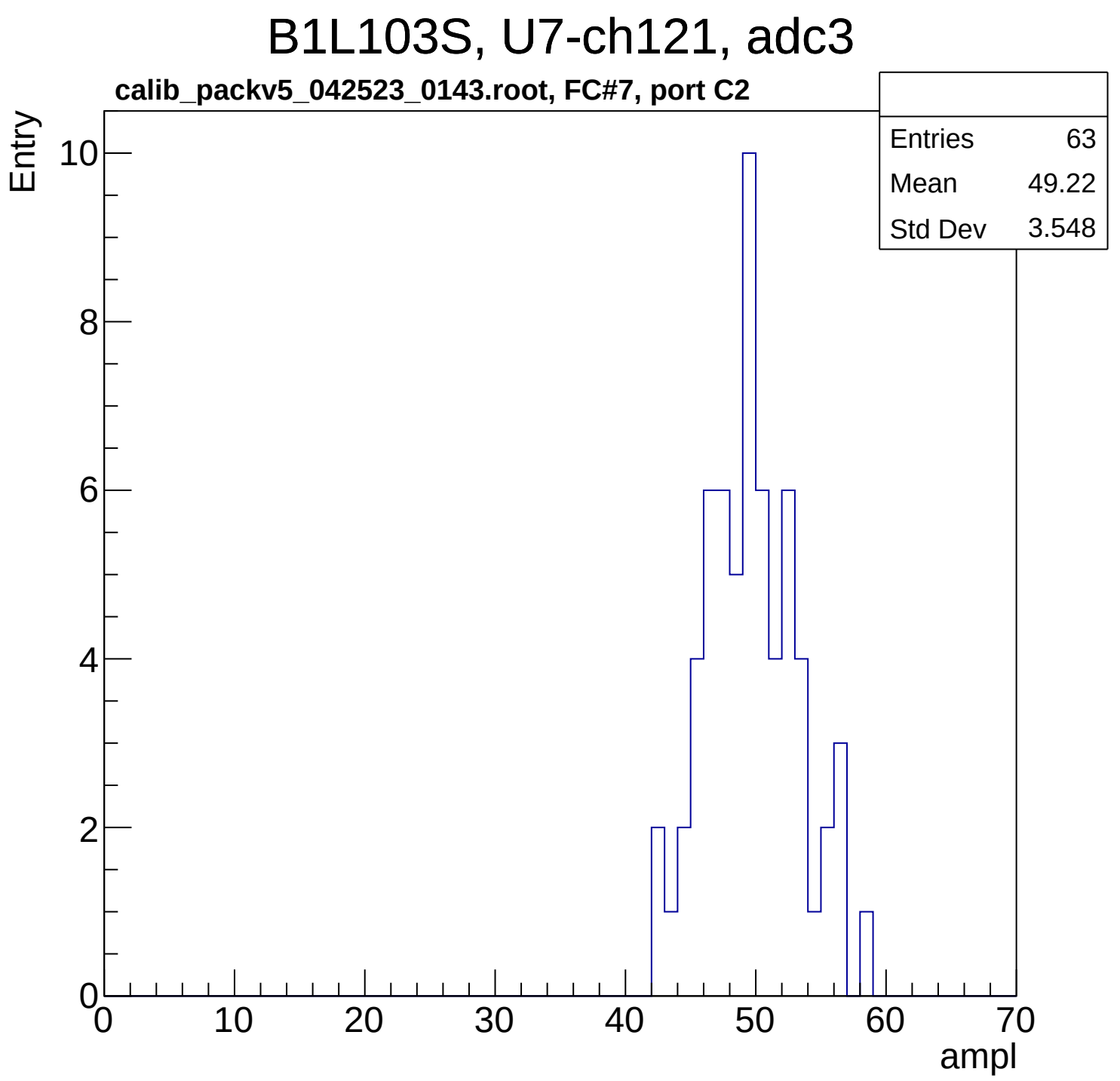
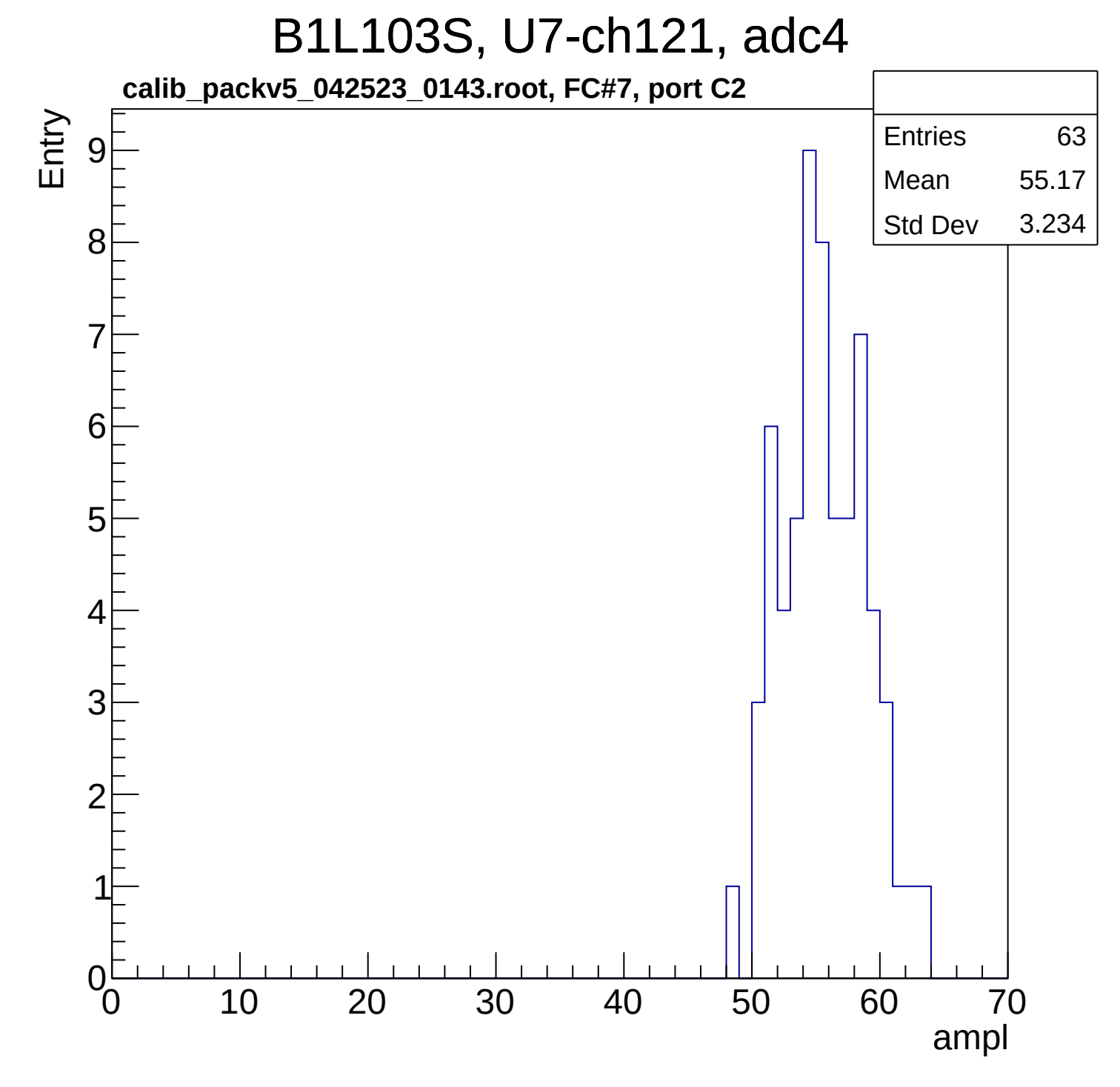

B1L103S, U7-ch121, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 42.37
Std Dev 3.58
Gaus mean : 43.4549
Gaus Width: 4.1189
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch121, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 49.22
Std Dev 3.548
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch121, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 55.17
Std Dev 3.234
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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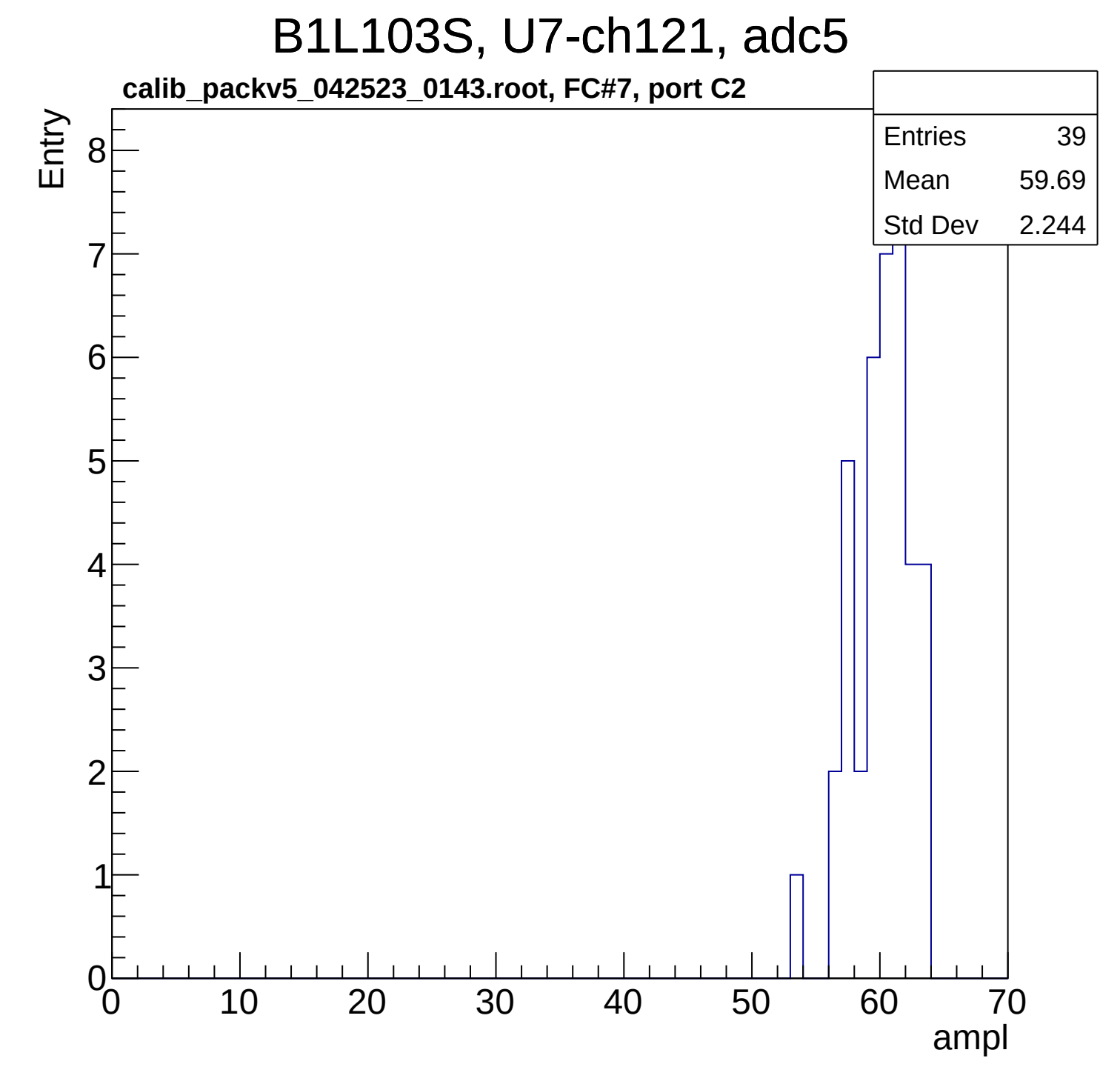
B1L103S, U7-ch121, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 39
Mean 59.69
Std Dev 2.244
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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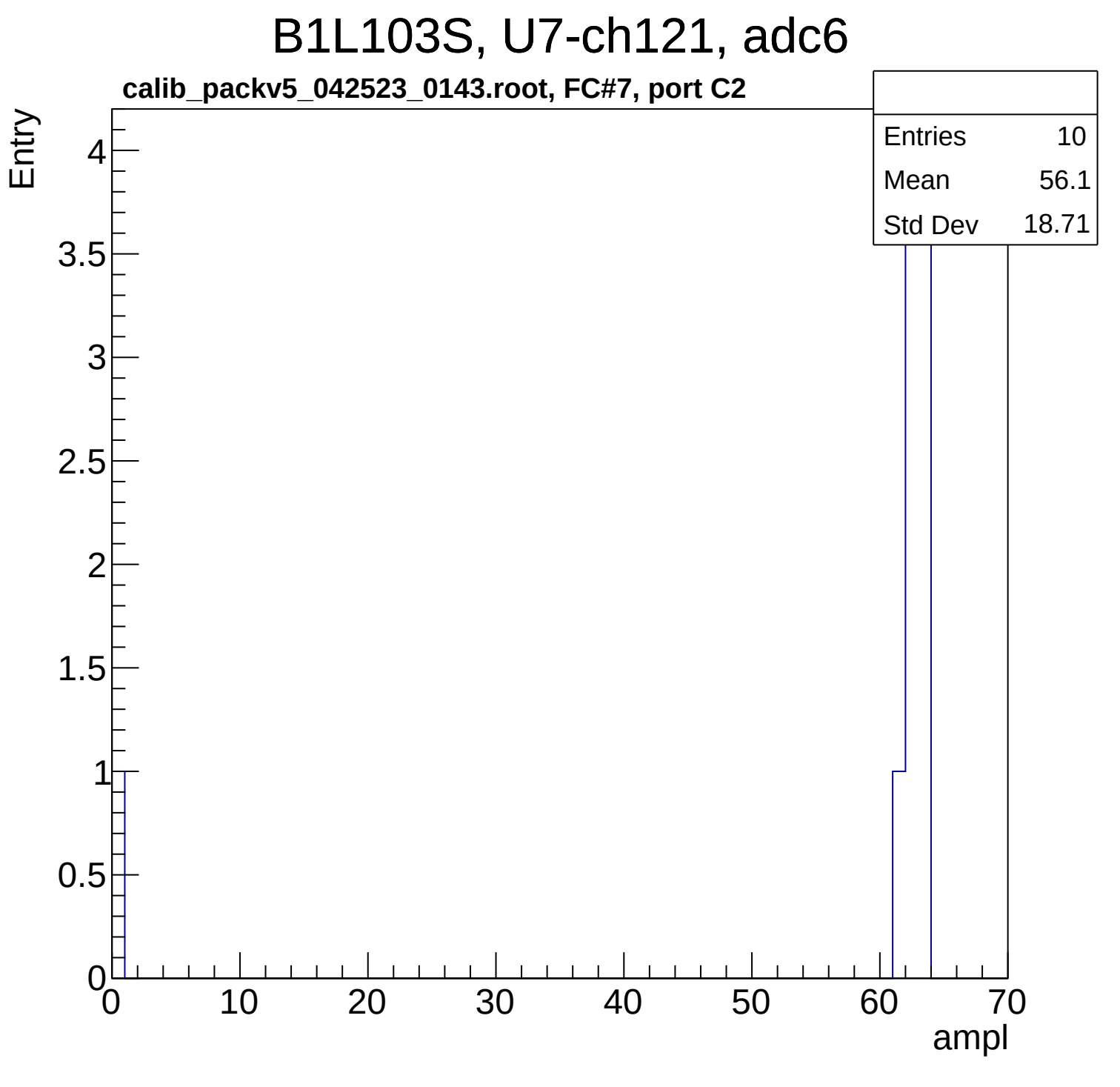
B1L103S, U7-ch121, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 10
Mean 56.1
Std Dev 18.71
Entry
ampl
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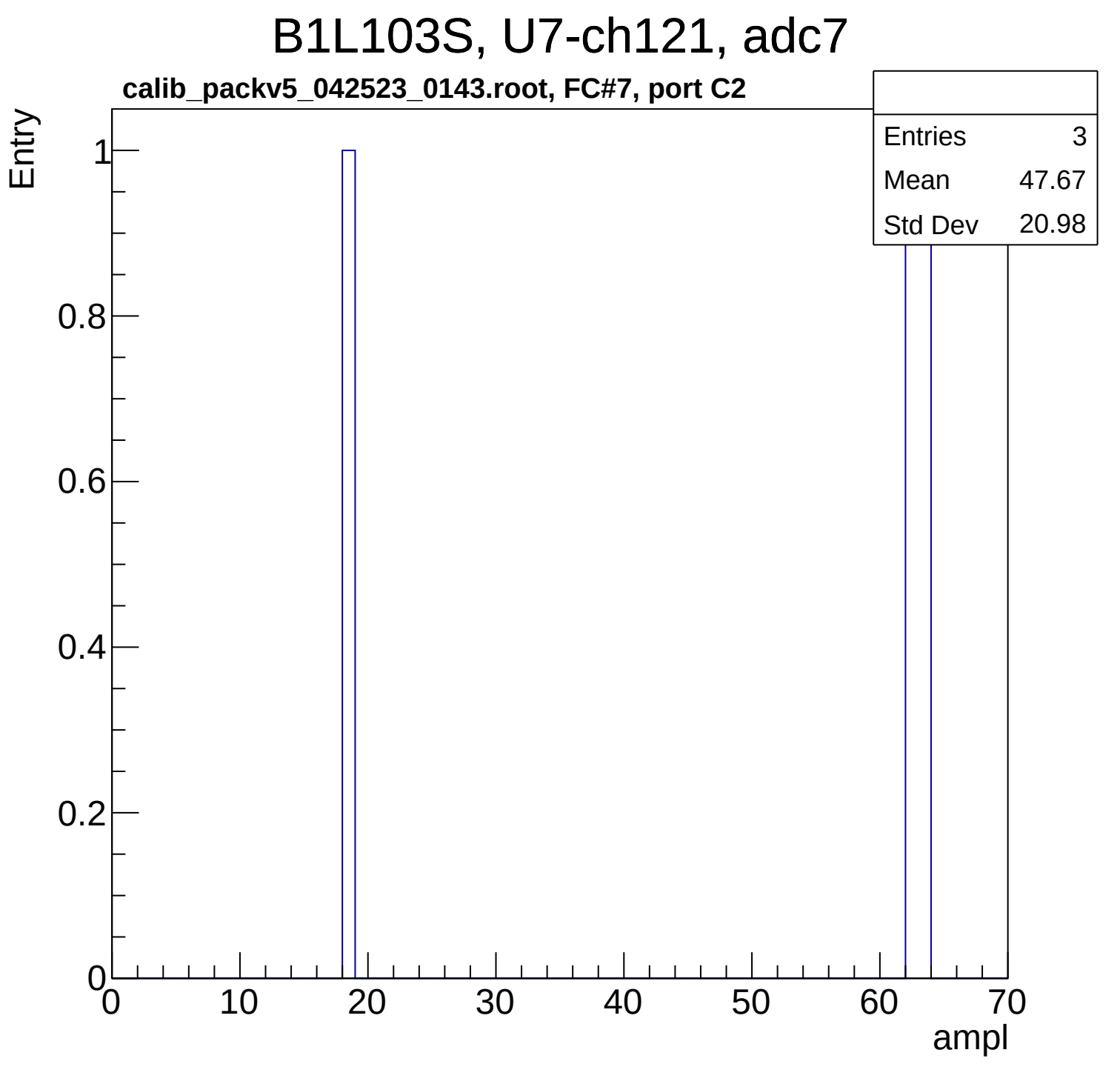
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U7-ch121, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 47.67
Std Dev 20.98
Entry
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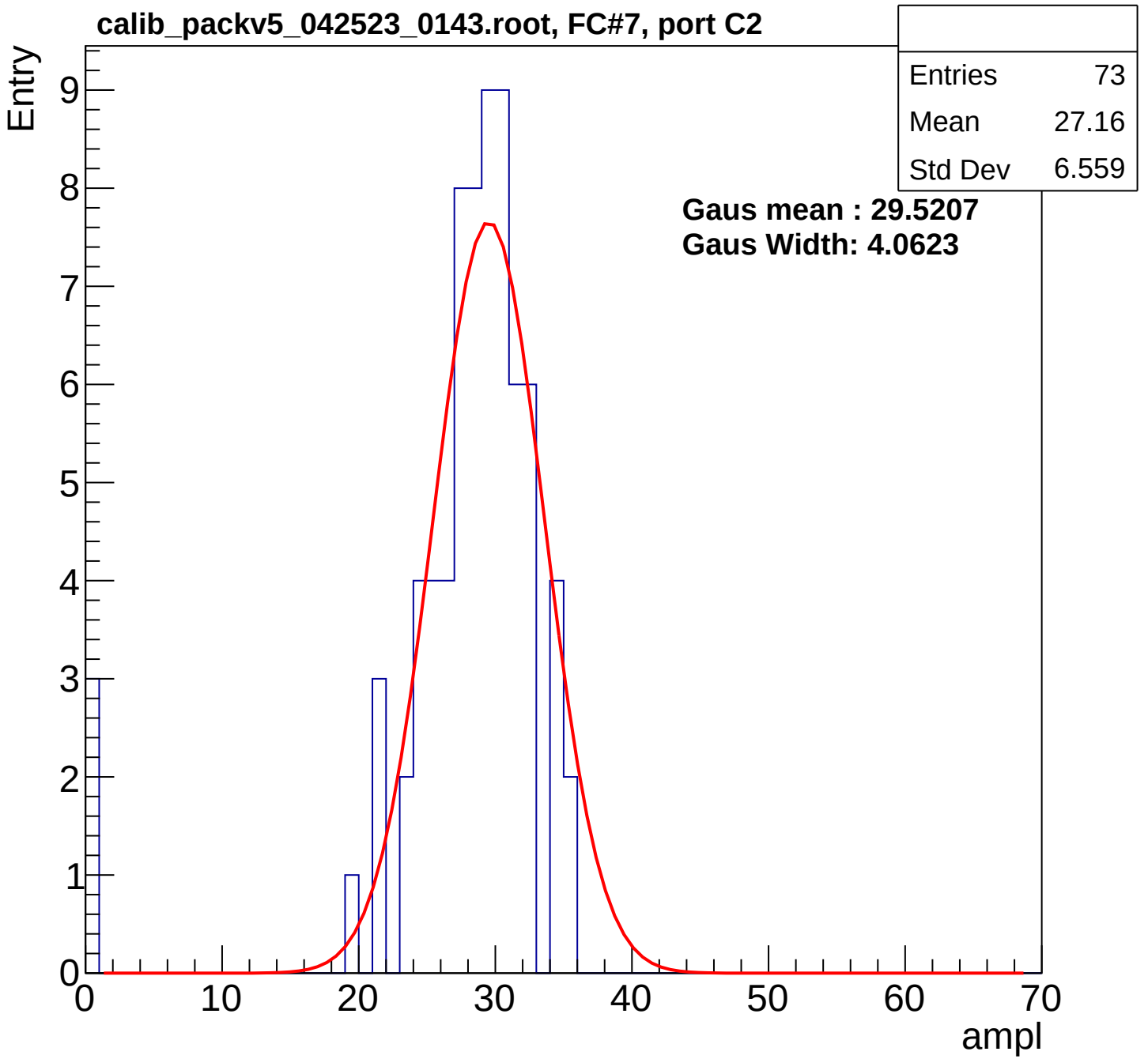
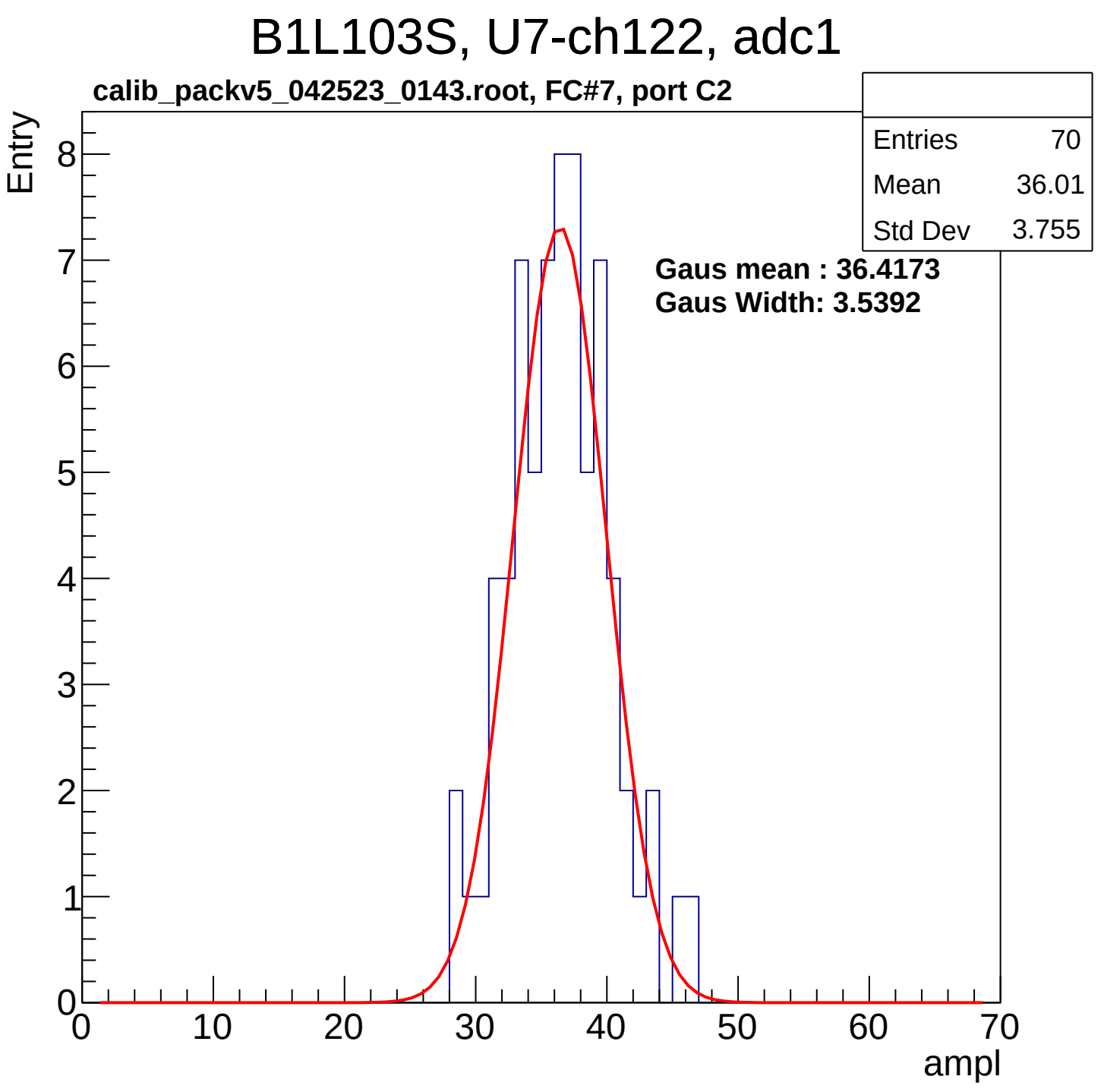
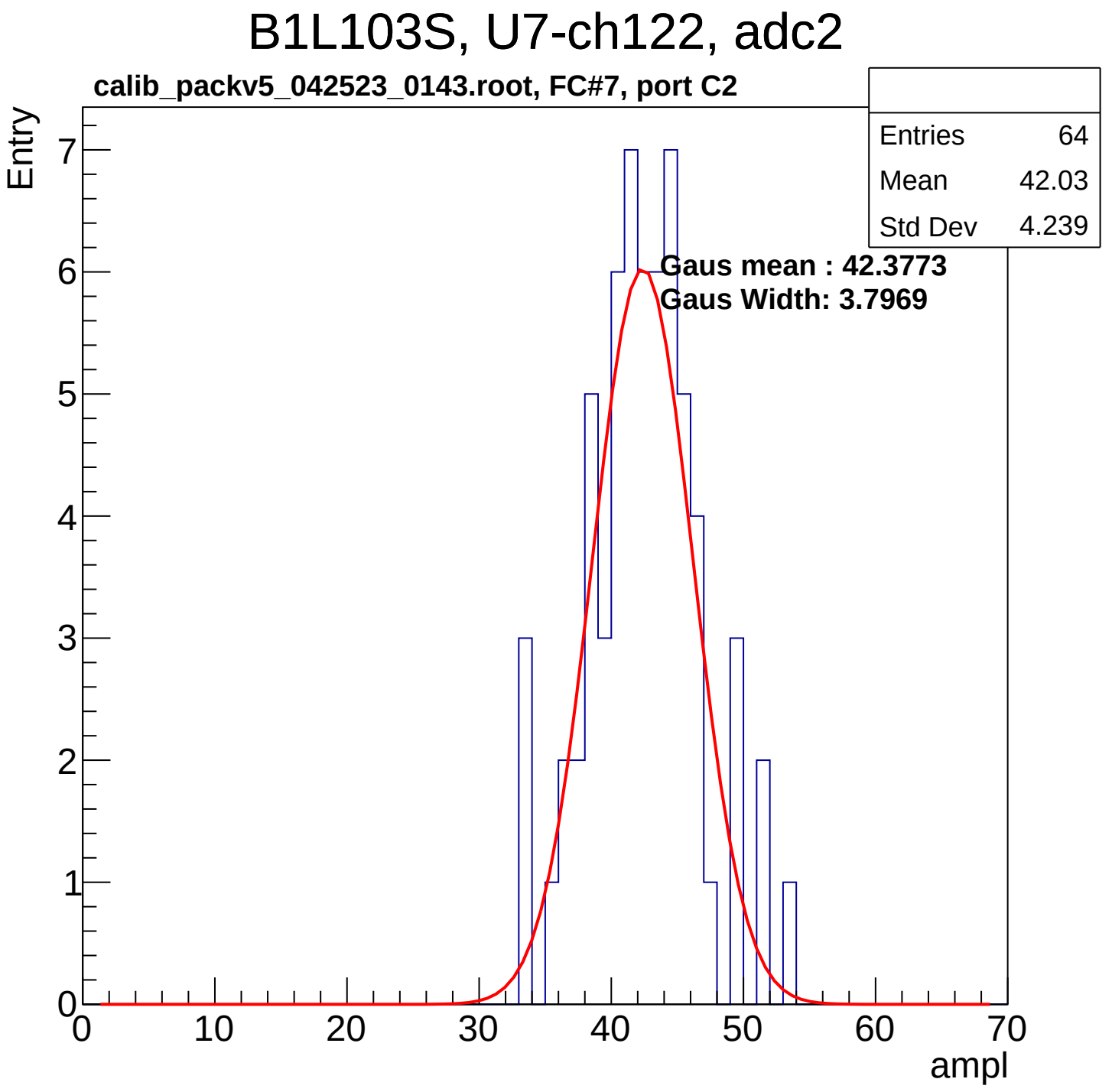
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch122, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 73
Mean 27.16
Std Dev 6.559
Gaus mean : 29.5207
Gaus Width: 4.0623
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch122, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 36.01
Std Dev 3.755
Gaus mean : 36.4173
Gaus Width: 3.5392
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch122, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 42.03
Std Dev 4.239
Gaus mean : 42.3773
Gaus Width: 3.7969
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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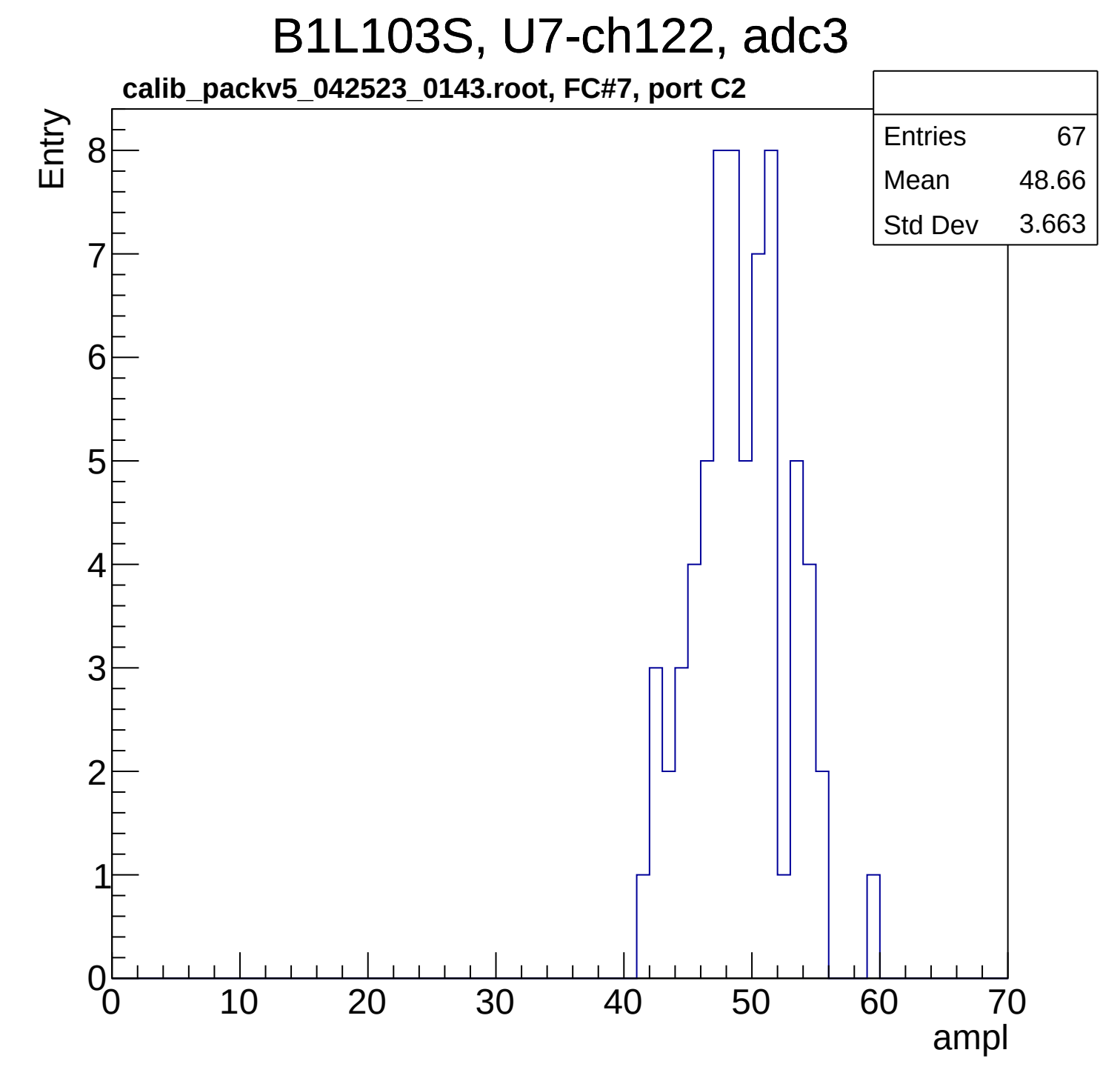
B1L103S, U7-ch122, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 48.66
Std Dev 3.663
Entry
ampl
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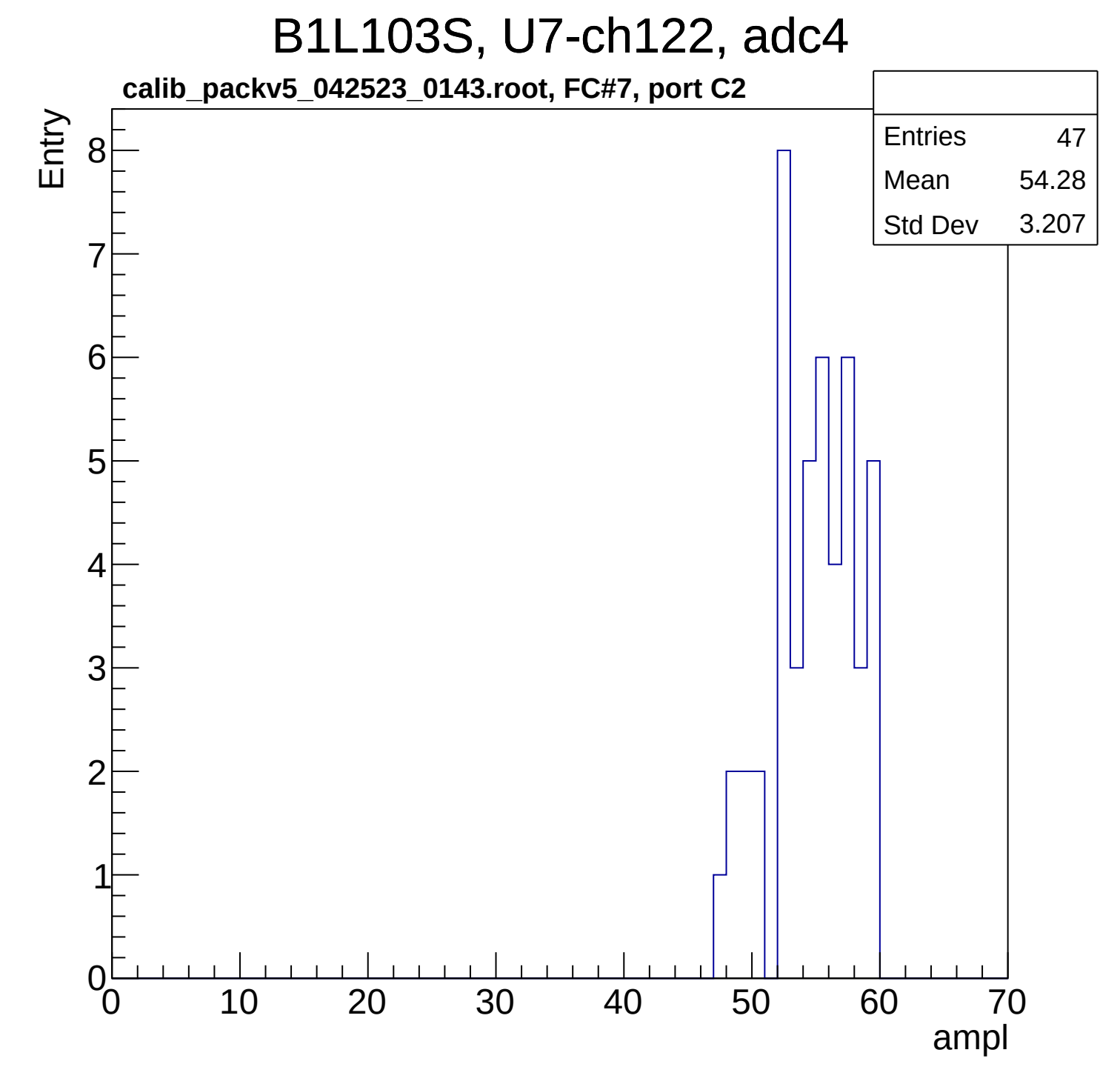
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch122, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 47
Mean 54.28
Std Dev 3.207
Entry
ampl
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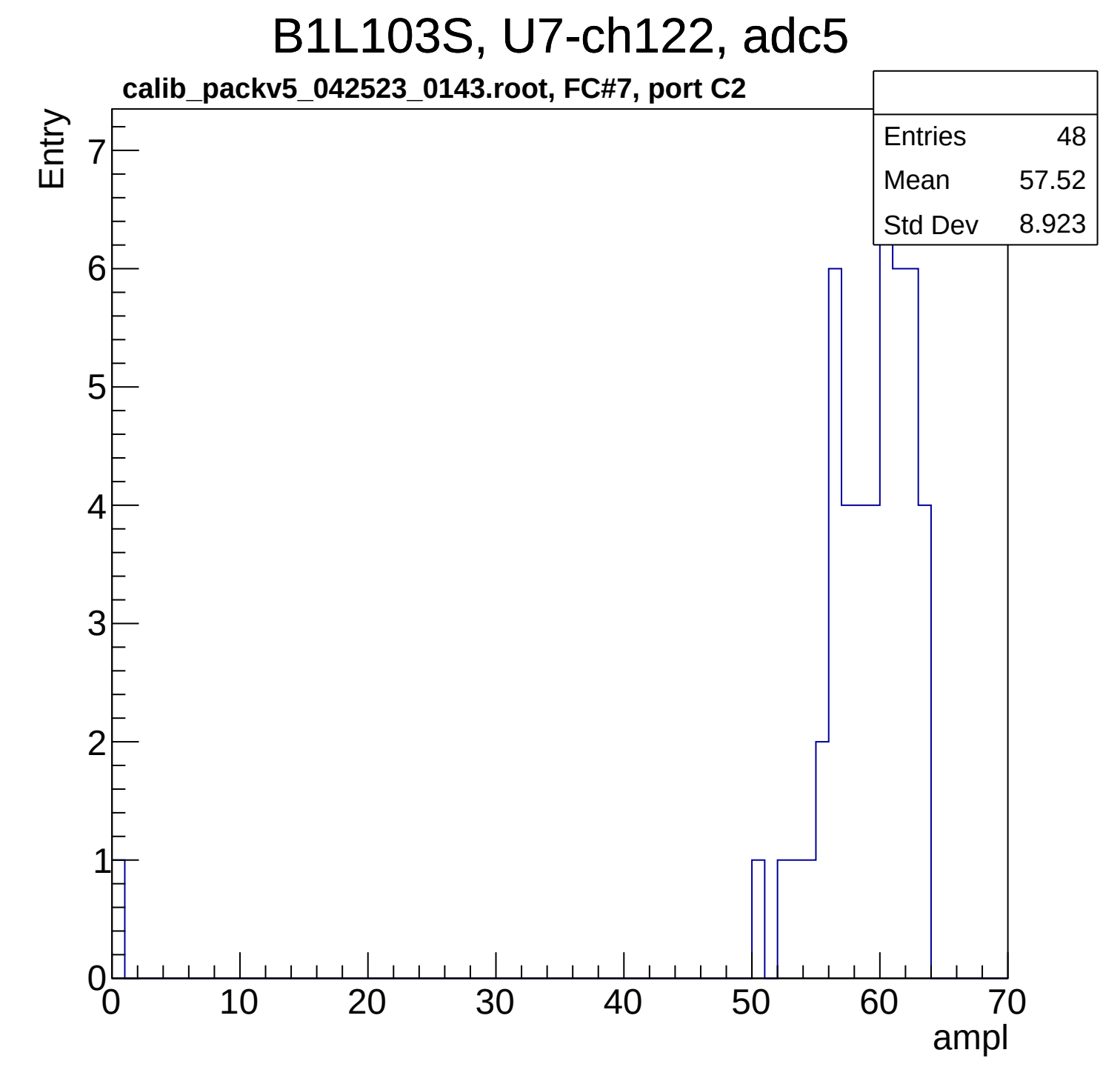
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch122, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 48
Mean 57.52
Std Dev 8.923
Entry
ampl
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1
2
3
4
5
6
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0
10
20
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40
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60
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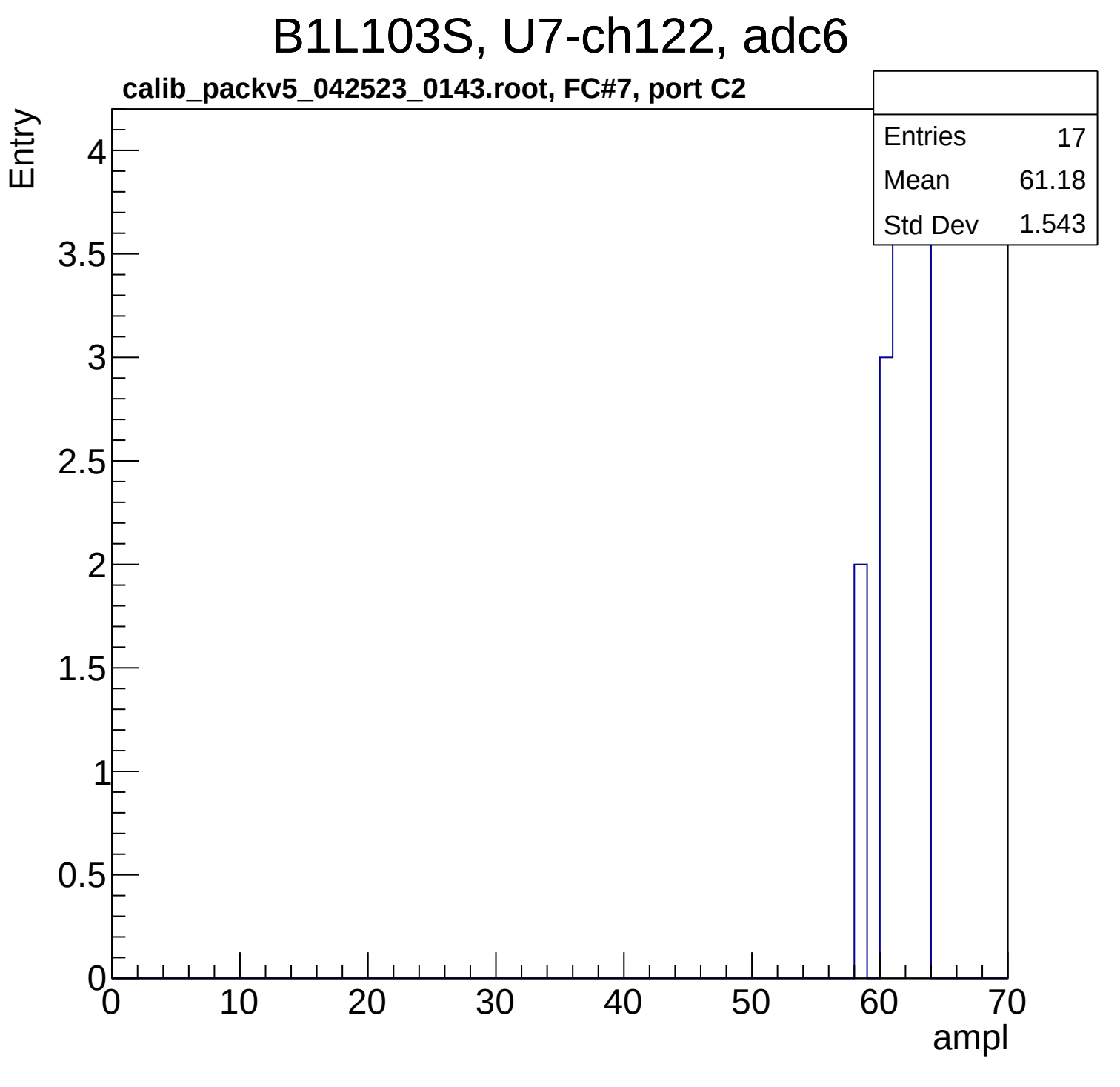
B1L103S, U7-ch122, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 17
Mean 61.18
Std Dev 1.543
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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40
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60
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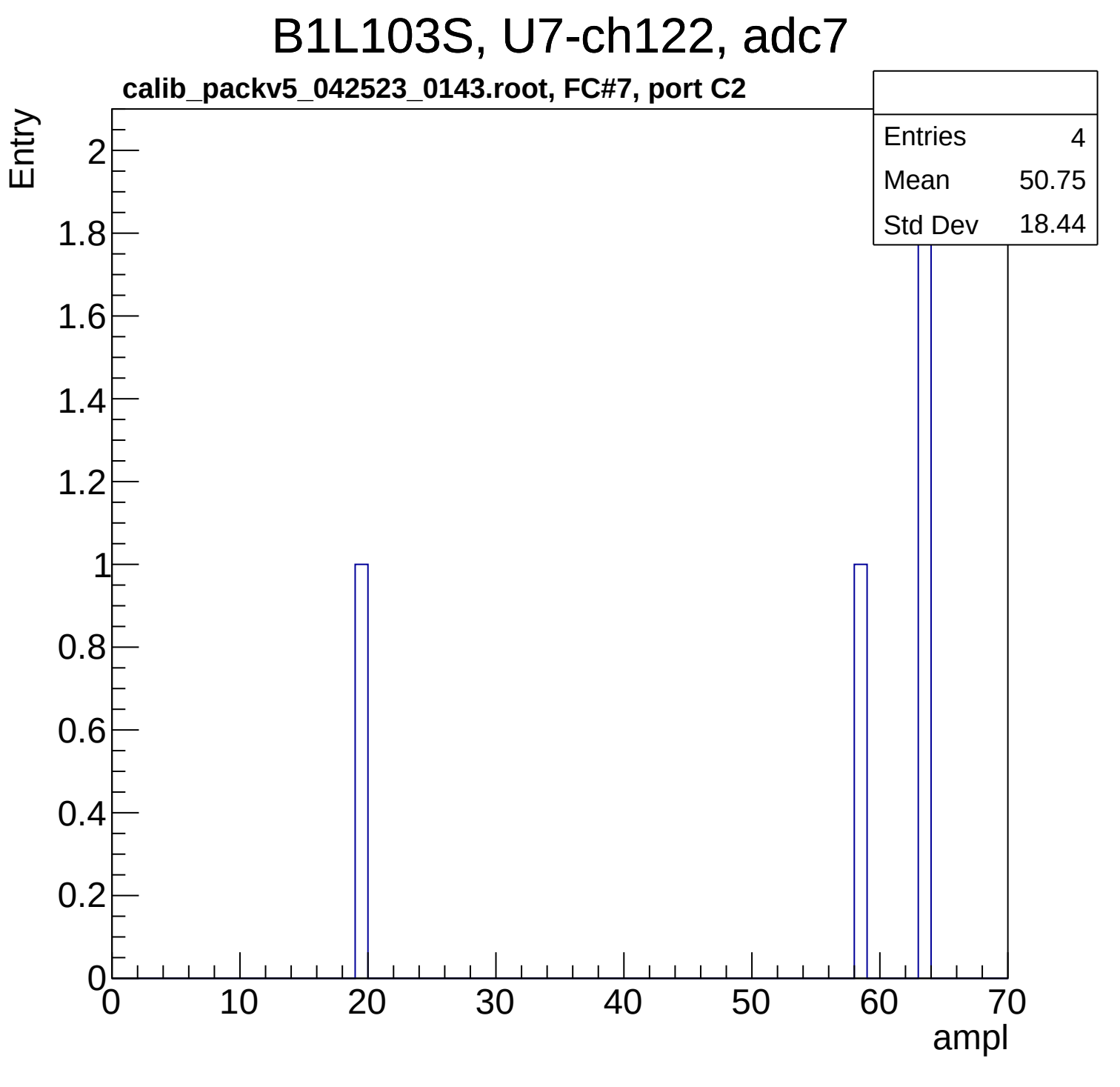
B1L103S, U7-ch122, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 4
Mean 50.75
Std Dev 18.44
Entry
ampl
0
0.2
0.4
0.6
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1
1.2
1.4
1.6
1.8
2
0
10
20
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60
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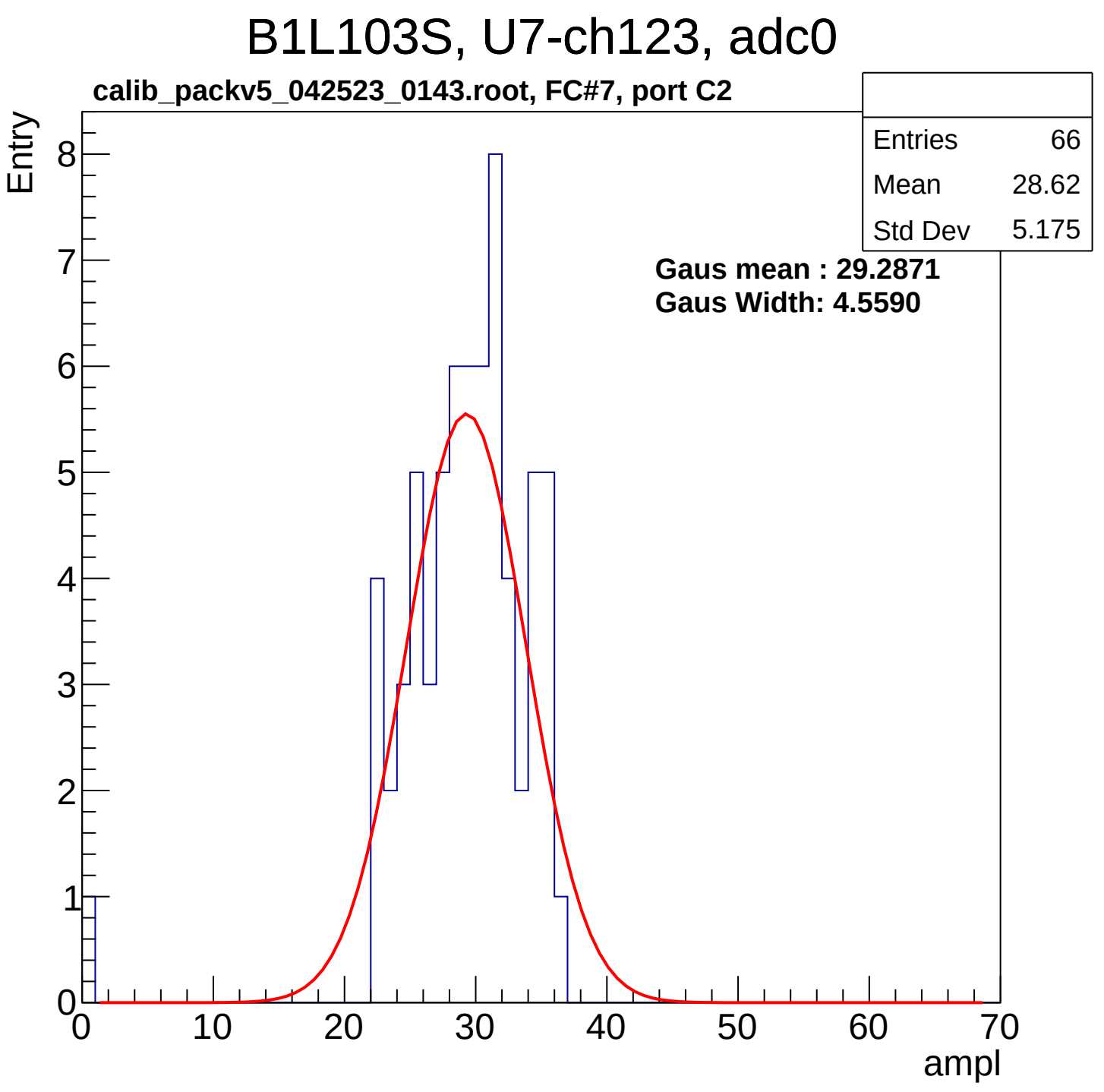
B1L103S, U7-ch123, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 28.62
Std Dev 5.175
Gaus mean : 29.2871
Gaus Width: 4.5590
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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20
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40
50
60
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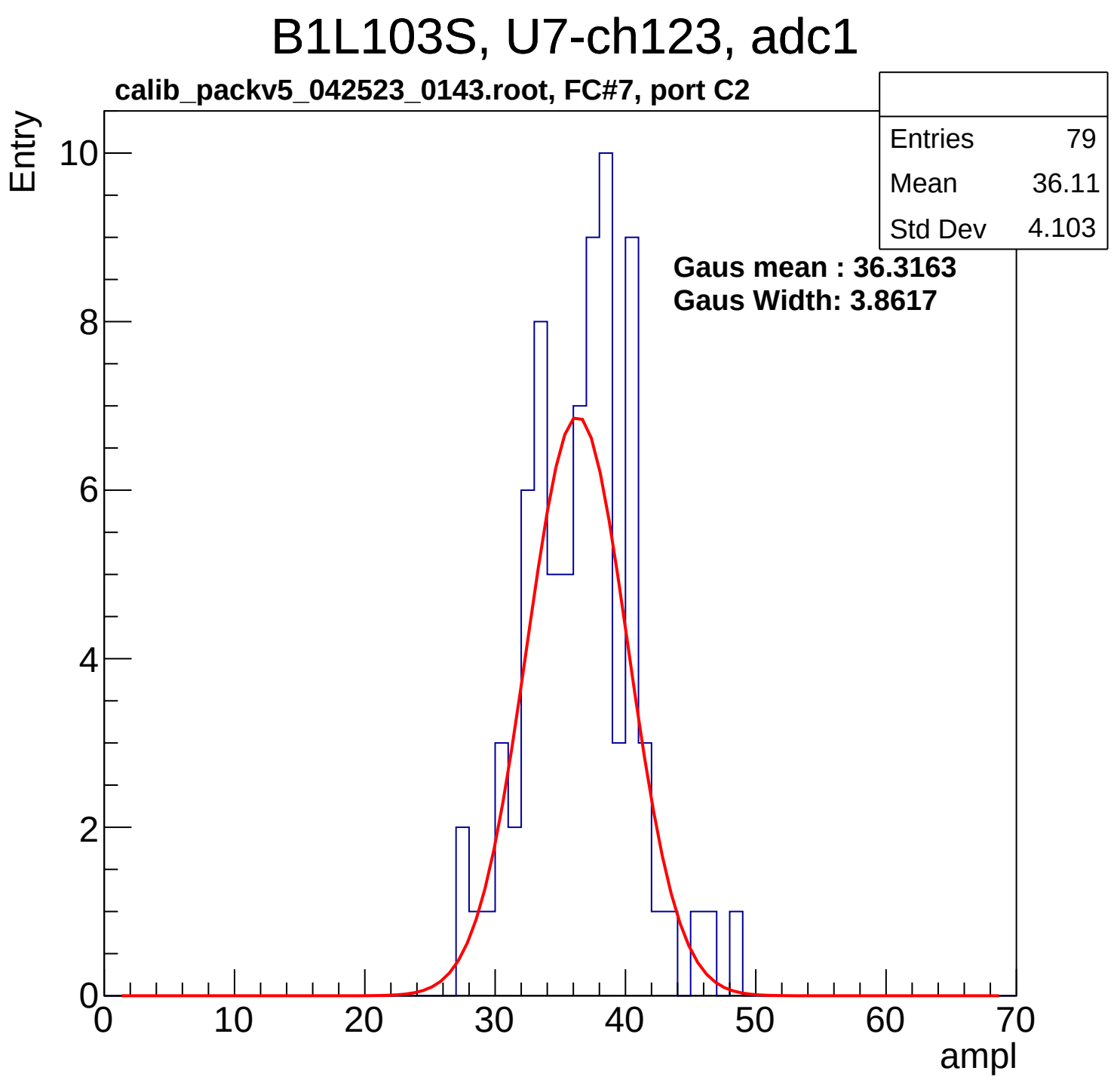
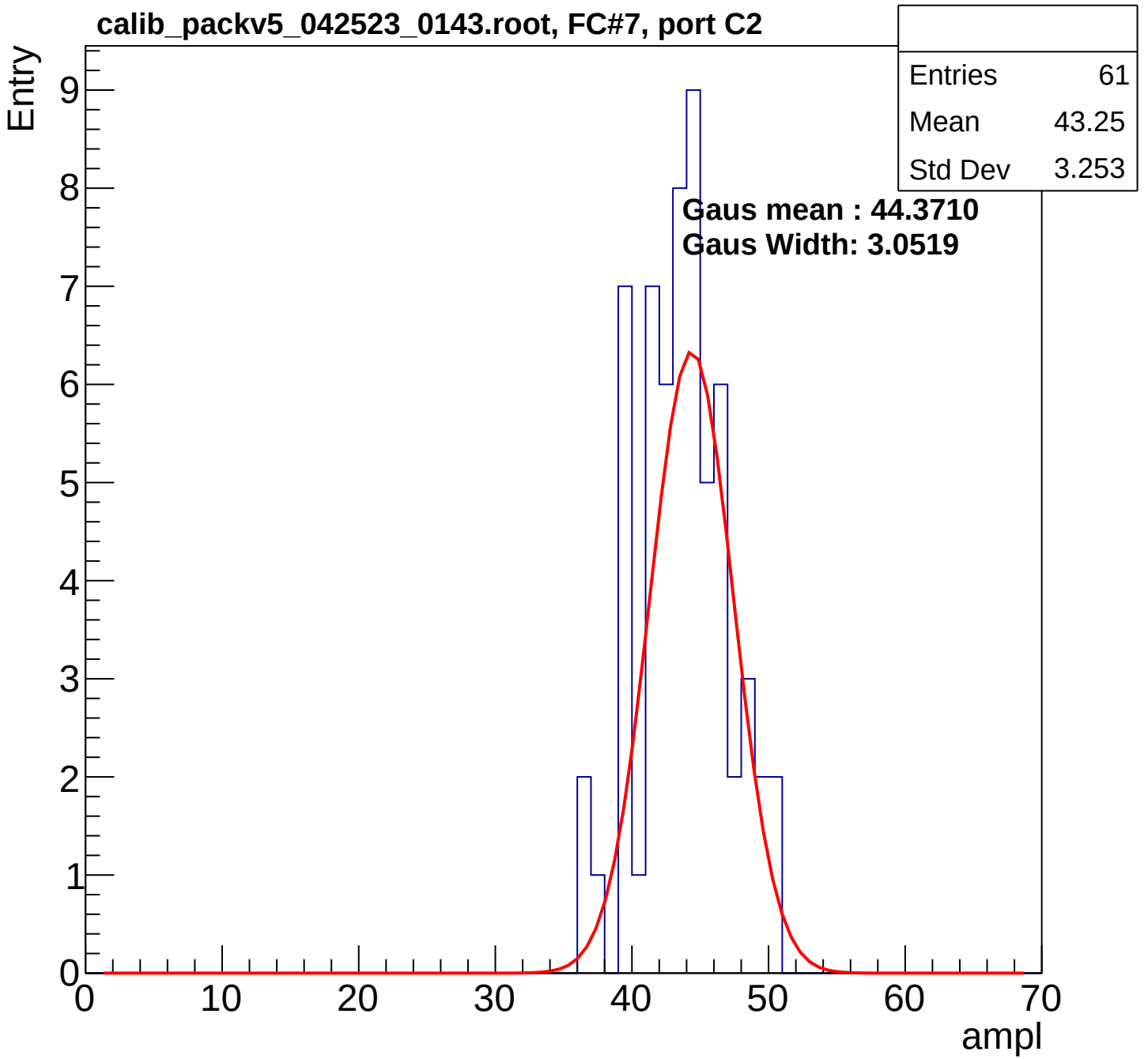

B1L103S, U7-ch123, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 79
Mean 36.11
Std Dev 4.103
Gaus mean : 36.3163
Gaus Width: 3.8617
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch123, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 61
Mean 43.25
Std Dev 3.253
Gaus mean : 44.3710
Gaus Width: 3.0519
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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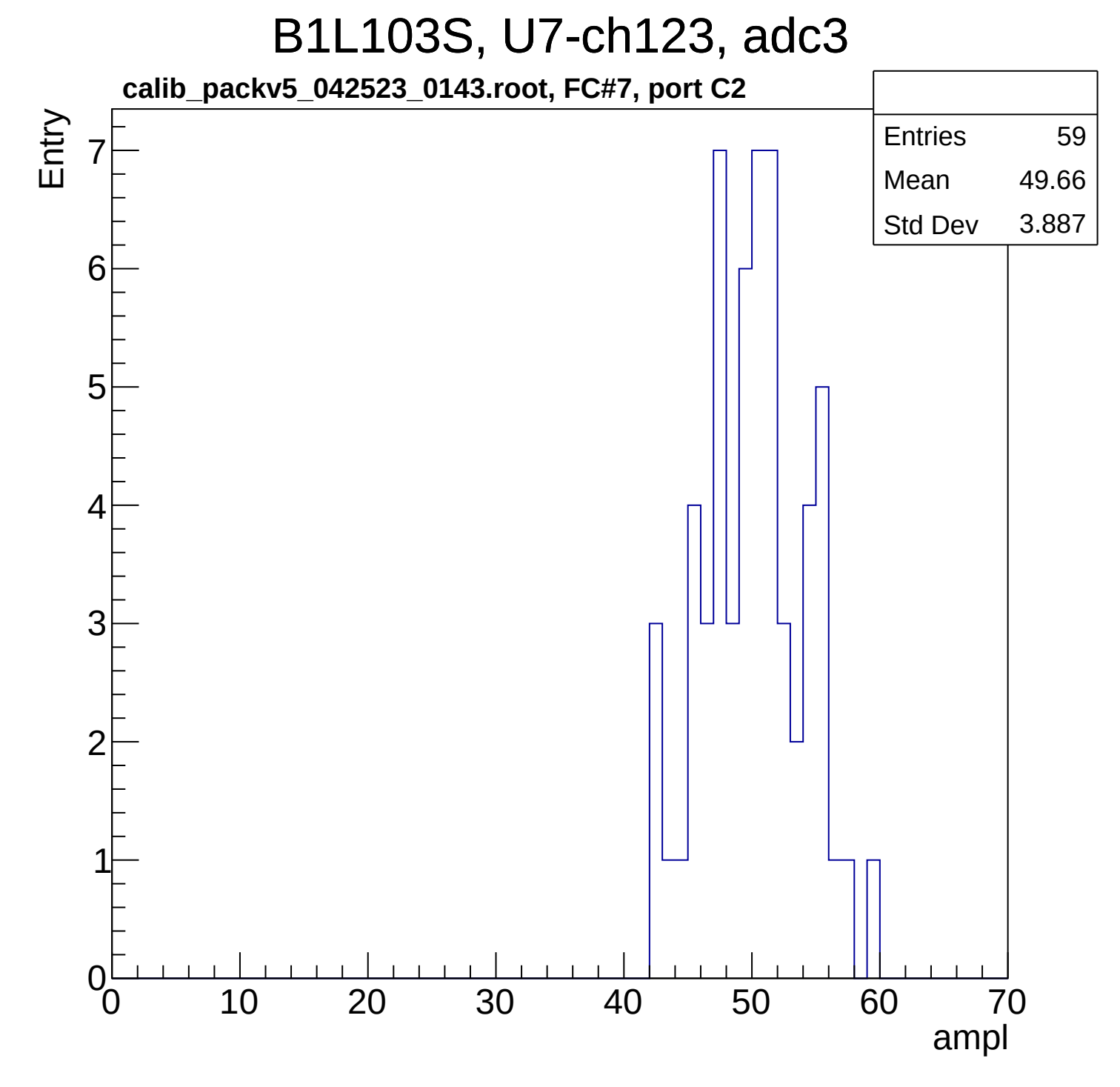
60
70


B1L103S, U7-ch123, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 49.66
Std Dev 3.887
Entry
ampl
0
1
2
3
4
5
6
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0
10
20
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40
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60
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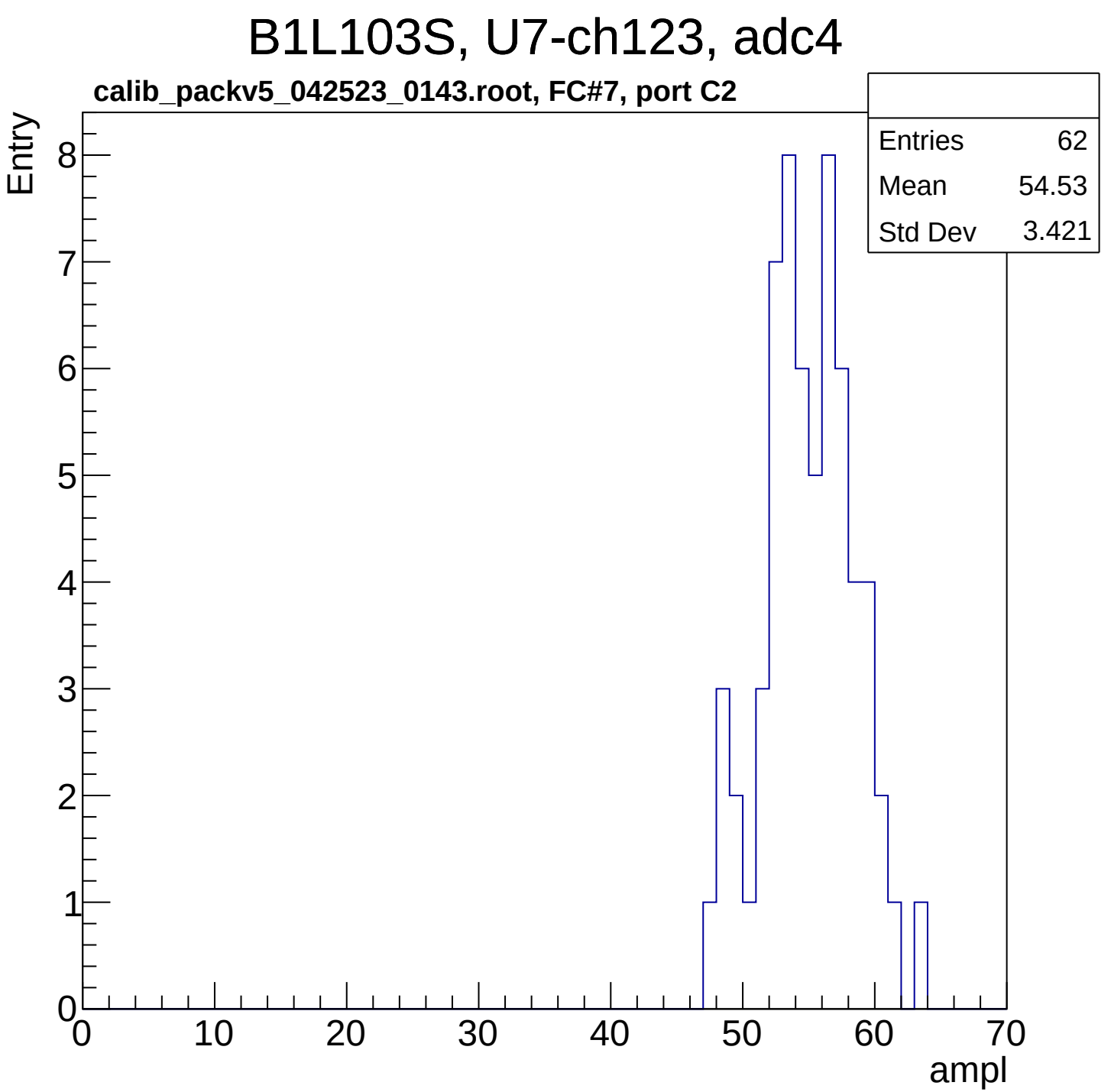
B1L103S, U7-ch123, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 62
Mean 54.53
Std Dev 3.421
Entry
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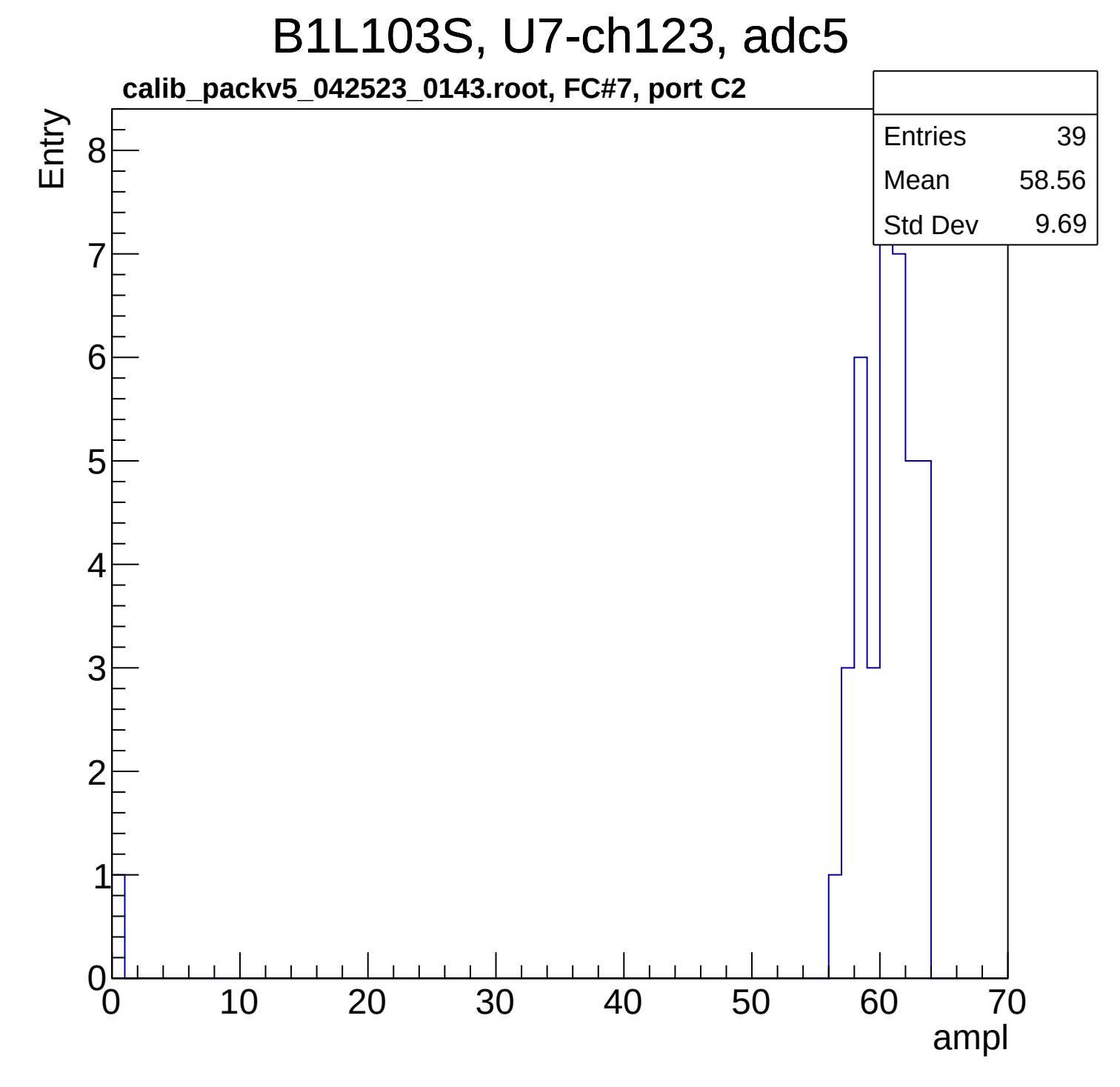
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch123, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 39
Mean 58.56
Std Dev 9.69
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
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40
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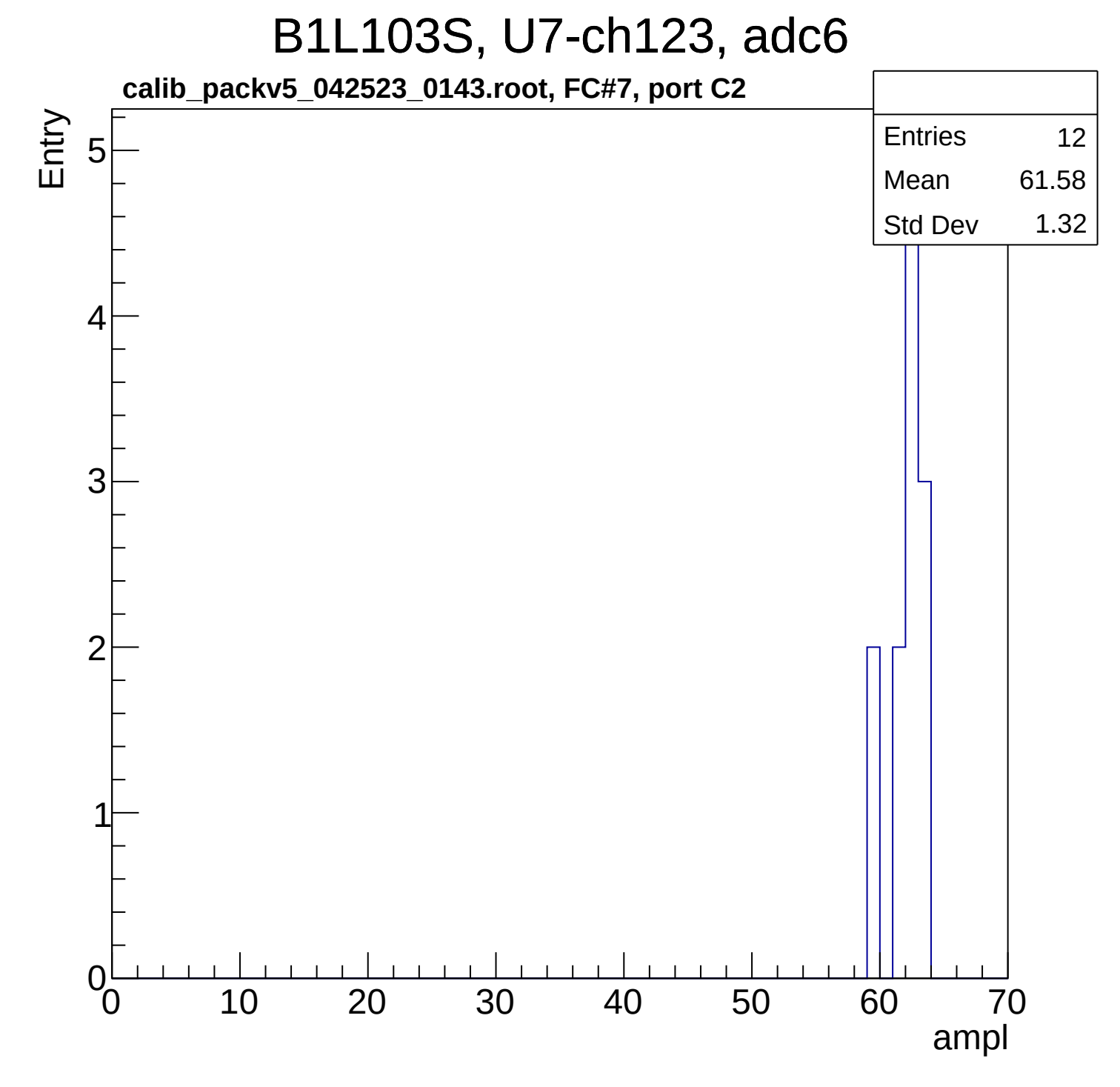
B1L103S, U7-ch123, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 12
Mean 61.58
Std Dev 1.32
Entry
0
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2
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4
5
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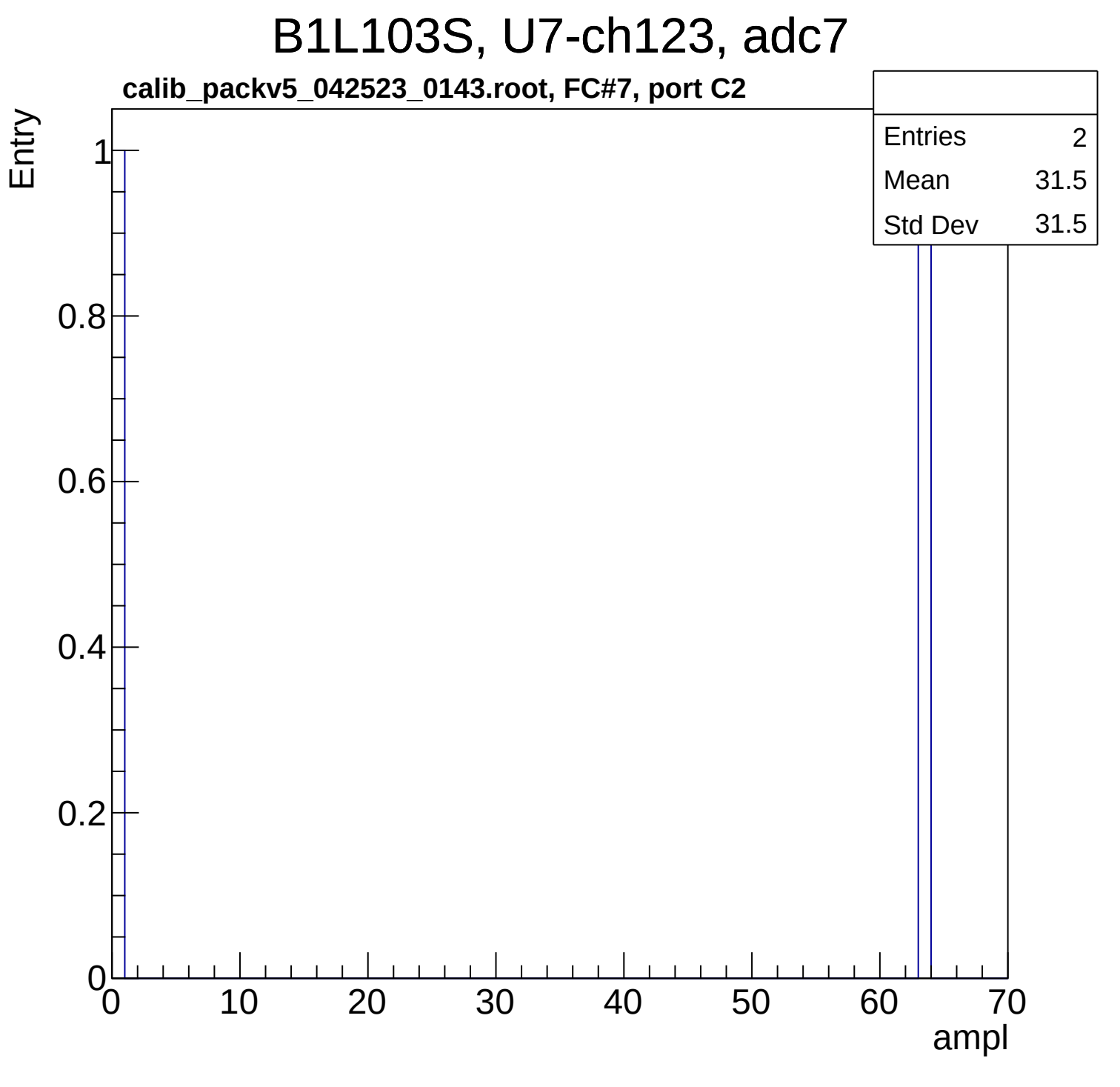
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch123, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 31.5
Std Dev 31.5
Entry
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0.6
0.4
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0
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20
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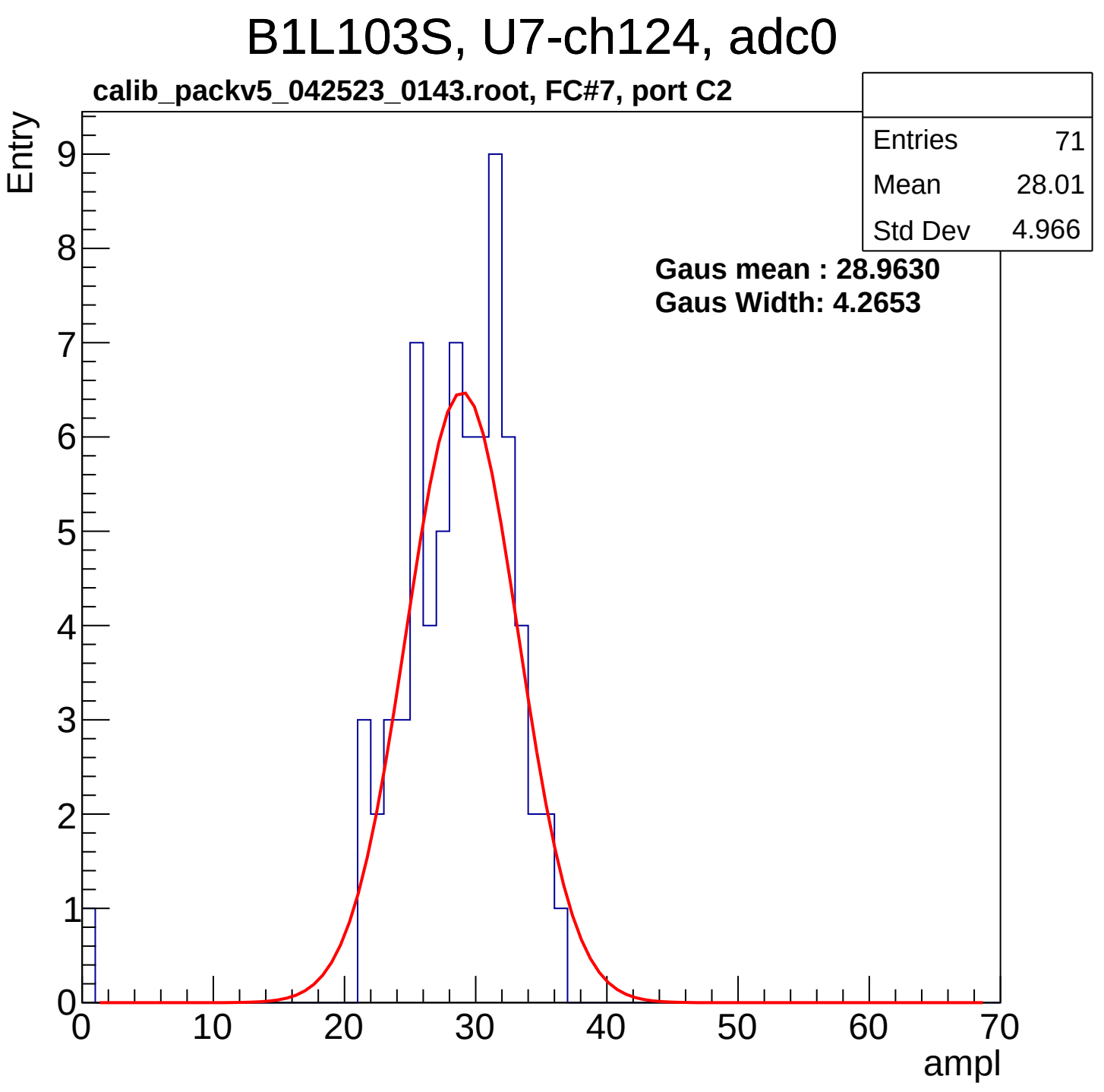
50
60
70
ampl


B1L103S, U7-ch124, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 71
Mean 28.01
Std Dev 4.966
Gaus mean : 28.9630
Gaus Width: 4.2653
Entry
ampl
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3
4
5
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7
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9
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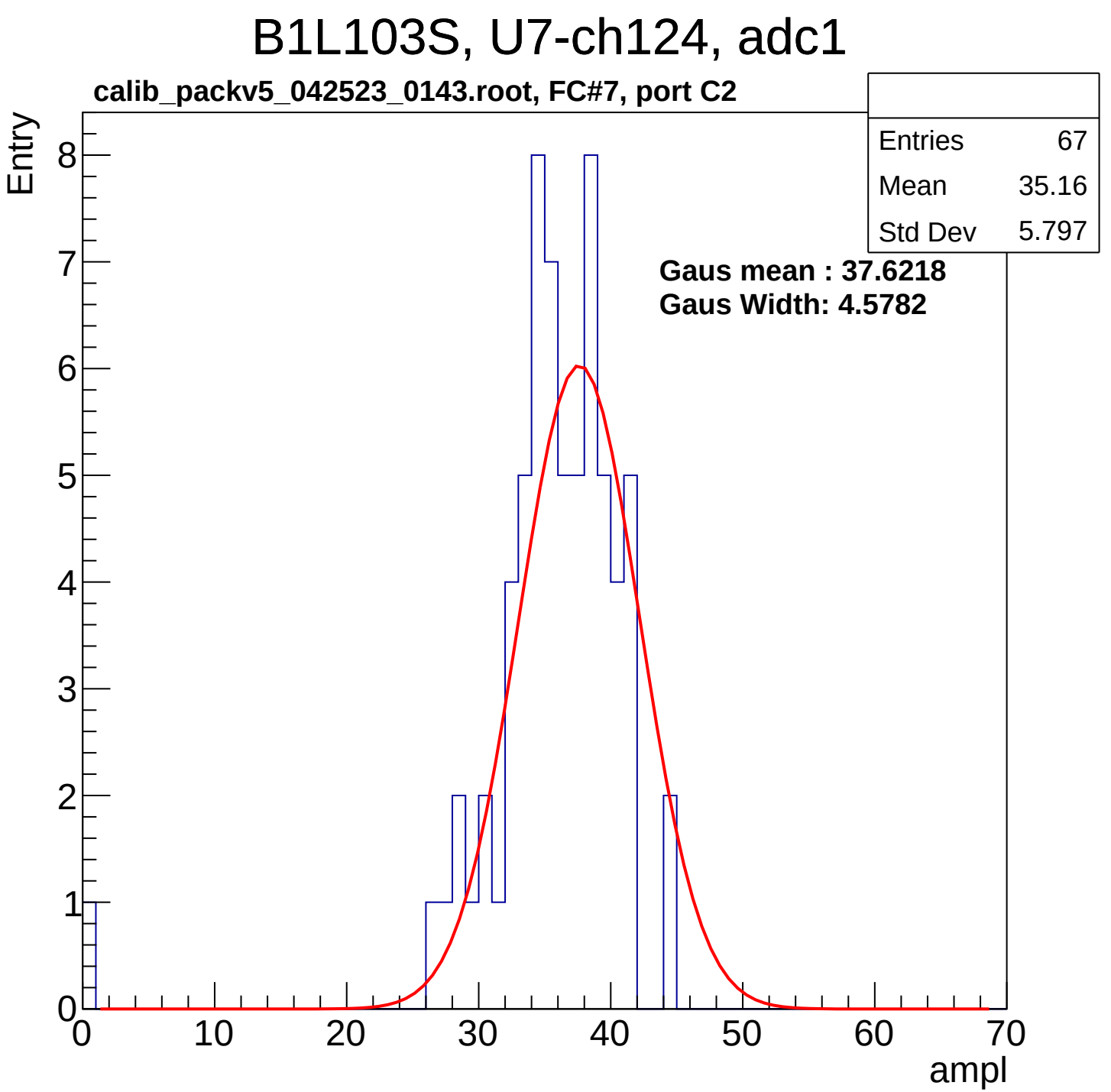
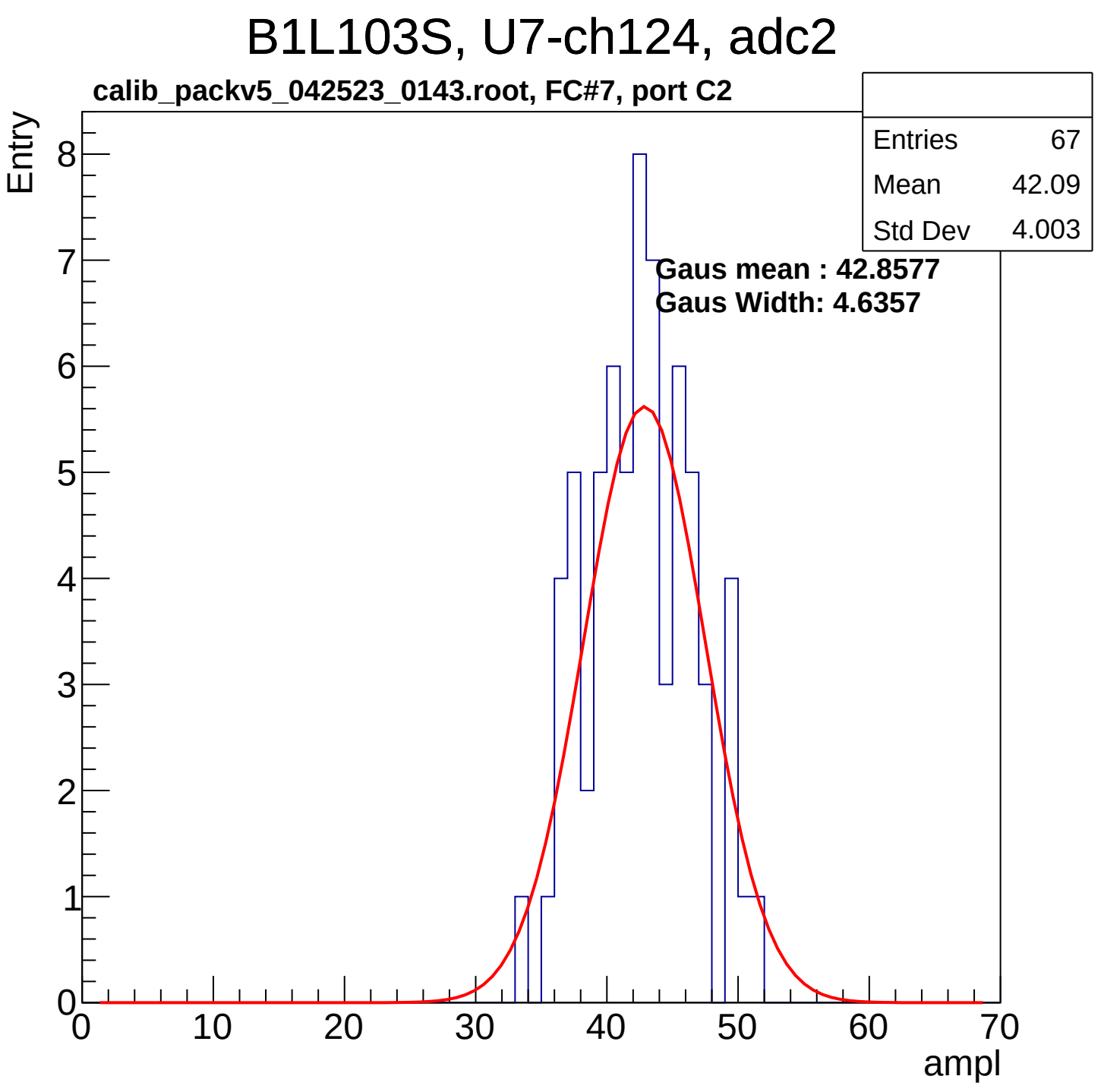
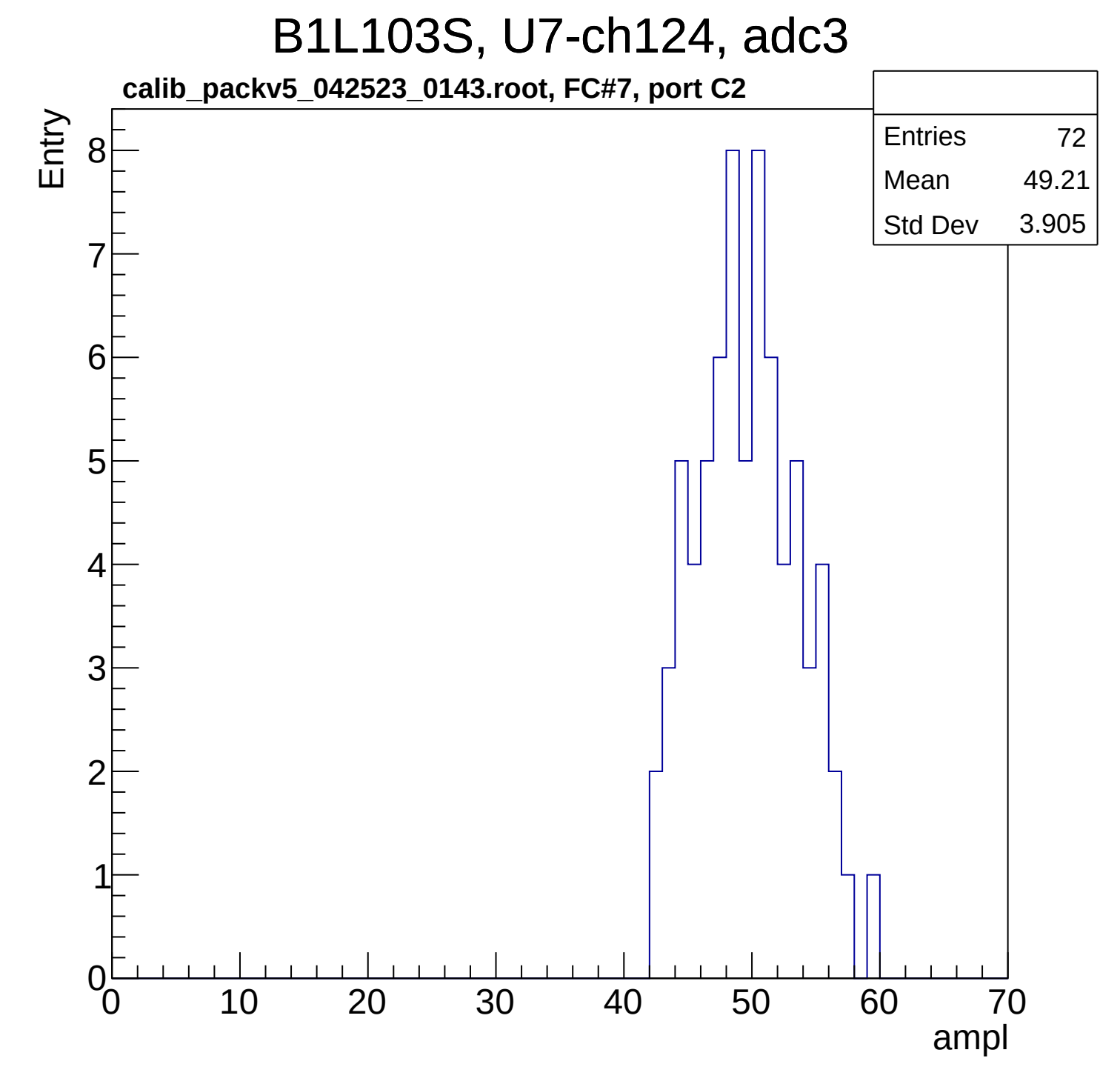
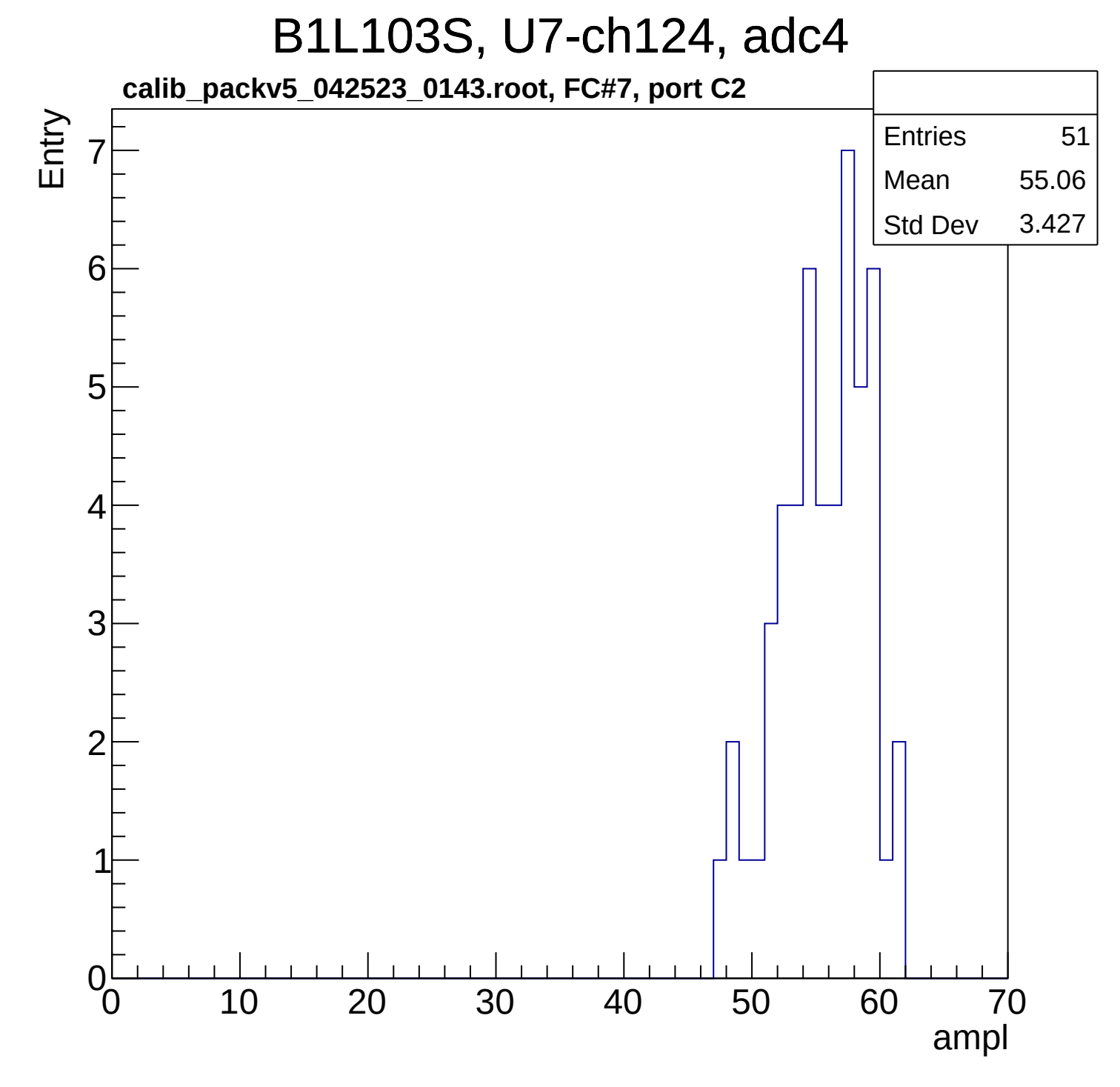
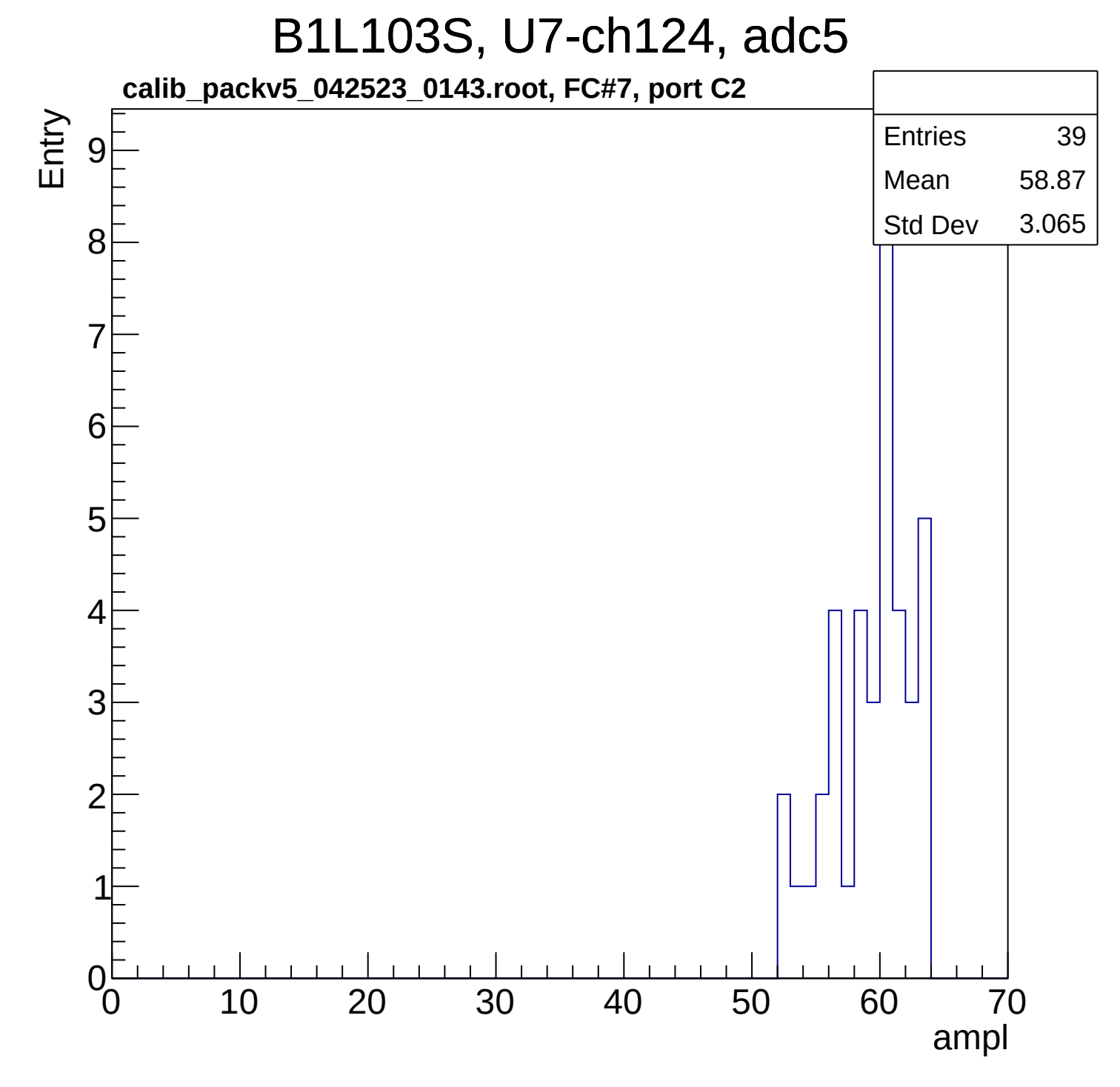

B1L103S, U7-ch124, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 35.16
Std Dev 5.797
Gaus mean : 37.6218
Gaus Width: 4.5782
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch124, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 42.09
Std Dev 4.003
Gaus mean : 42.8577
Gaus Width: 4.6357
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch124, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 72
Mean 49.21
Std Dev 3.905
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch124, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 51
Mean 55.06
Std Dev 3.427
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch124, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 39
Mean 58.87
Std Dev 3.065
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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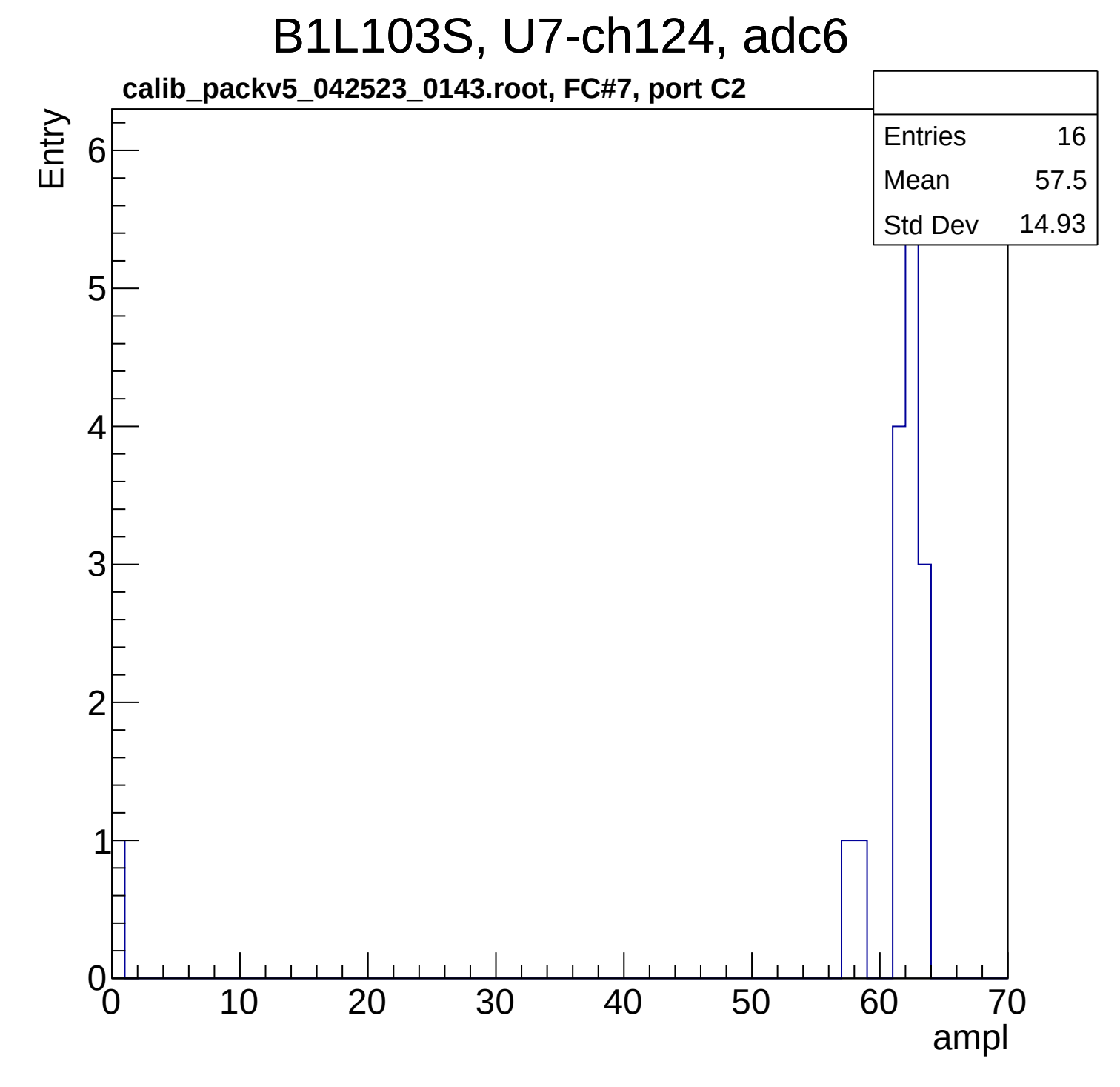
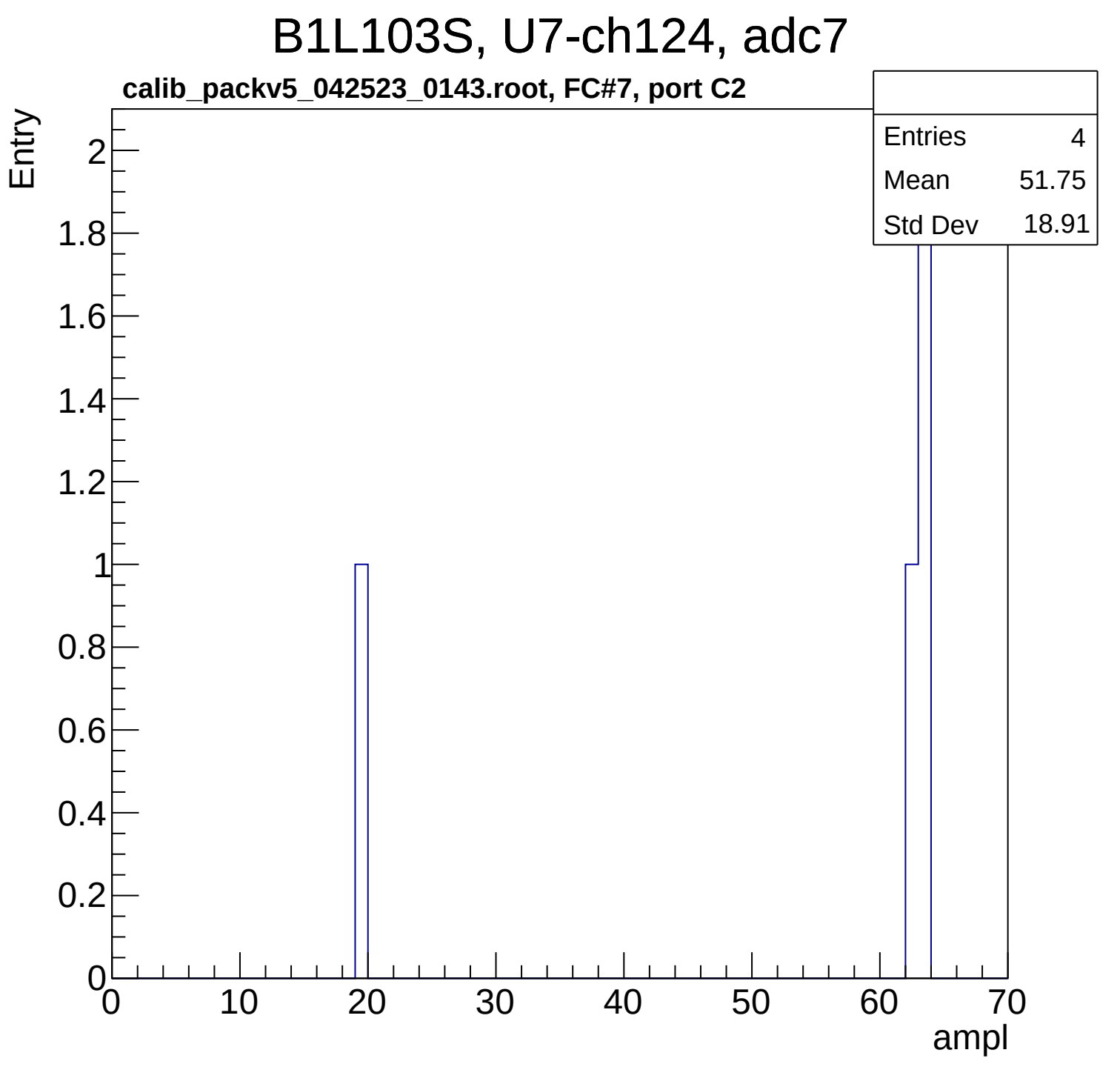
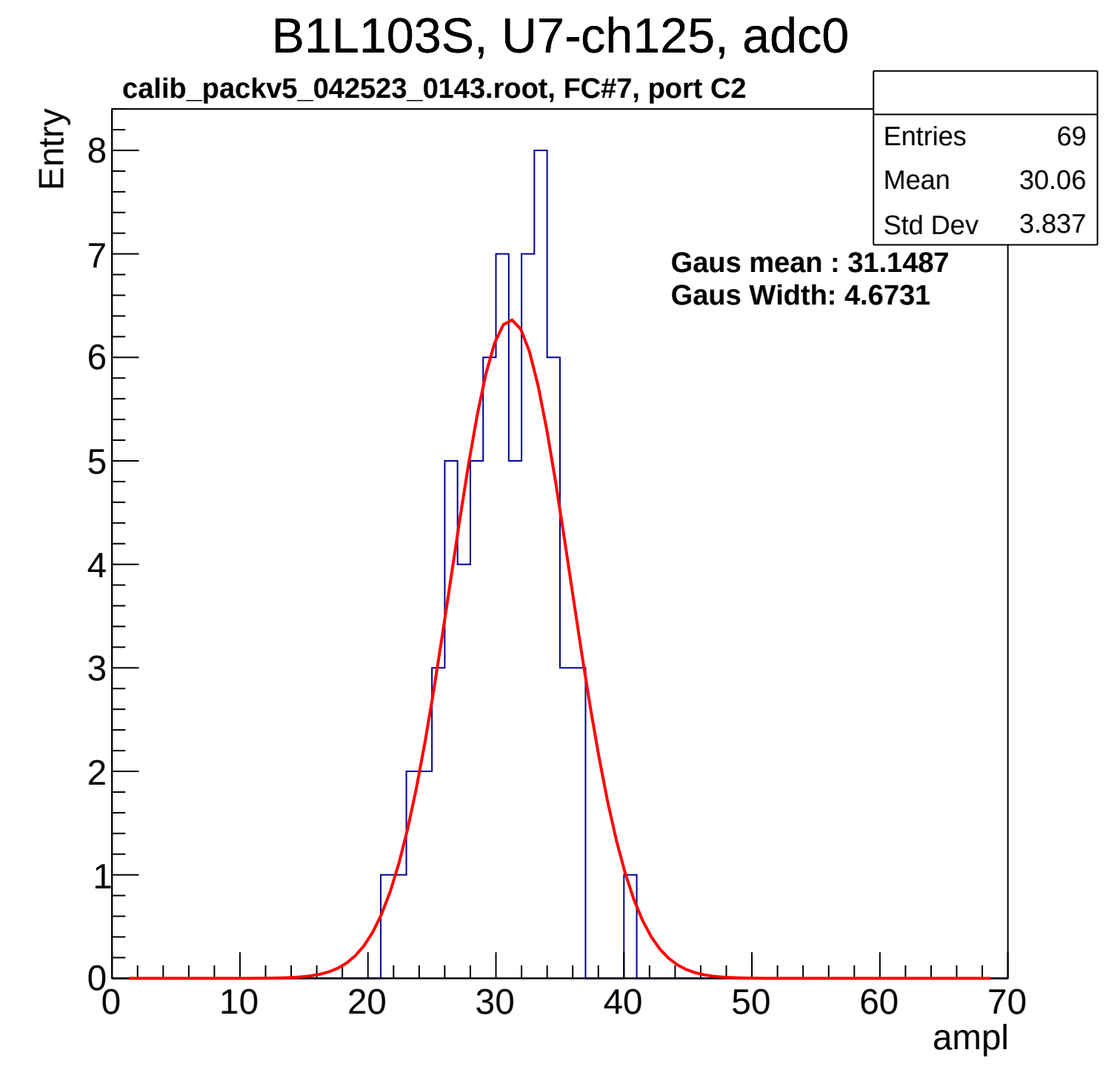
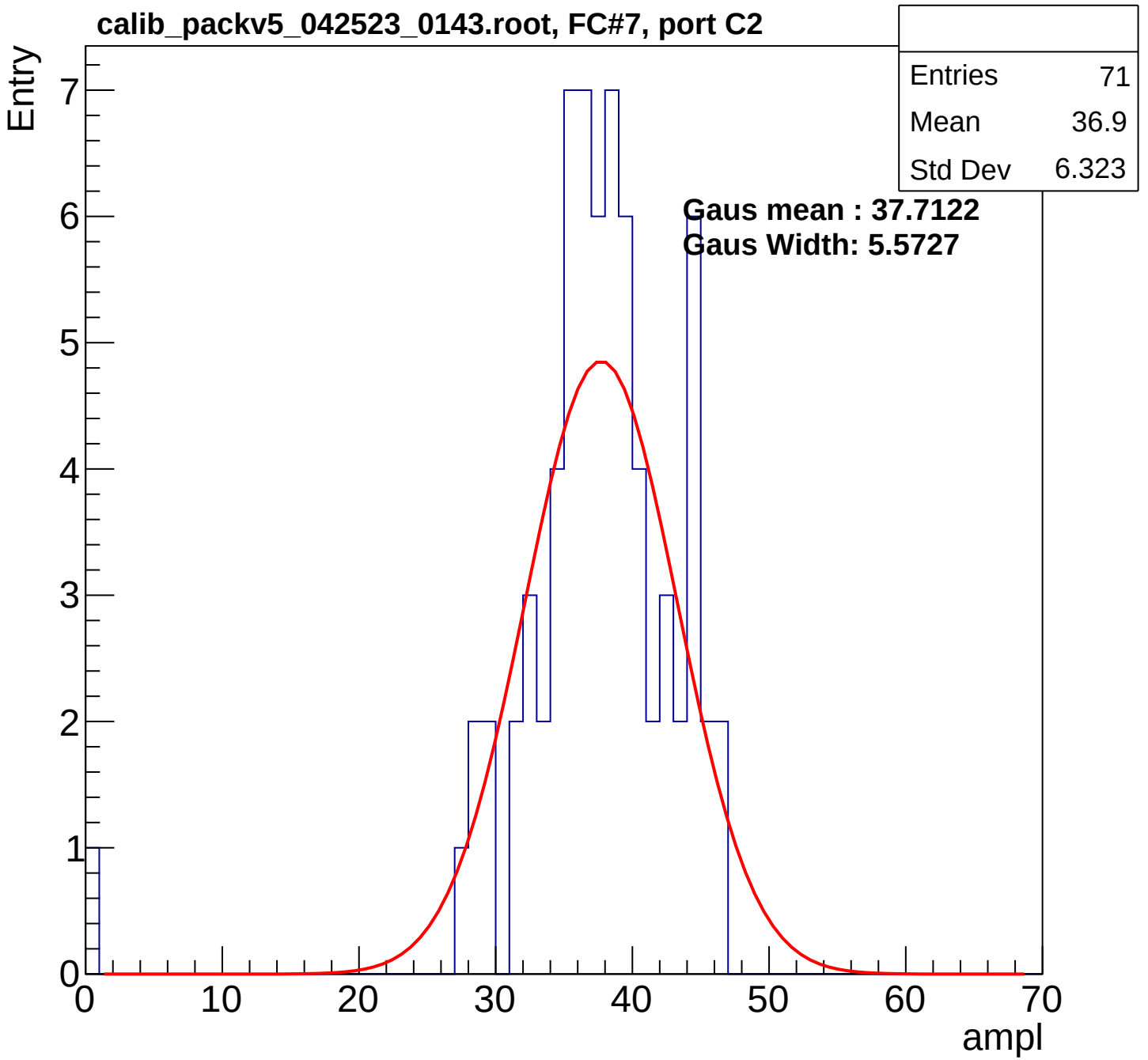
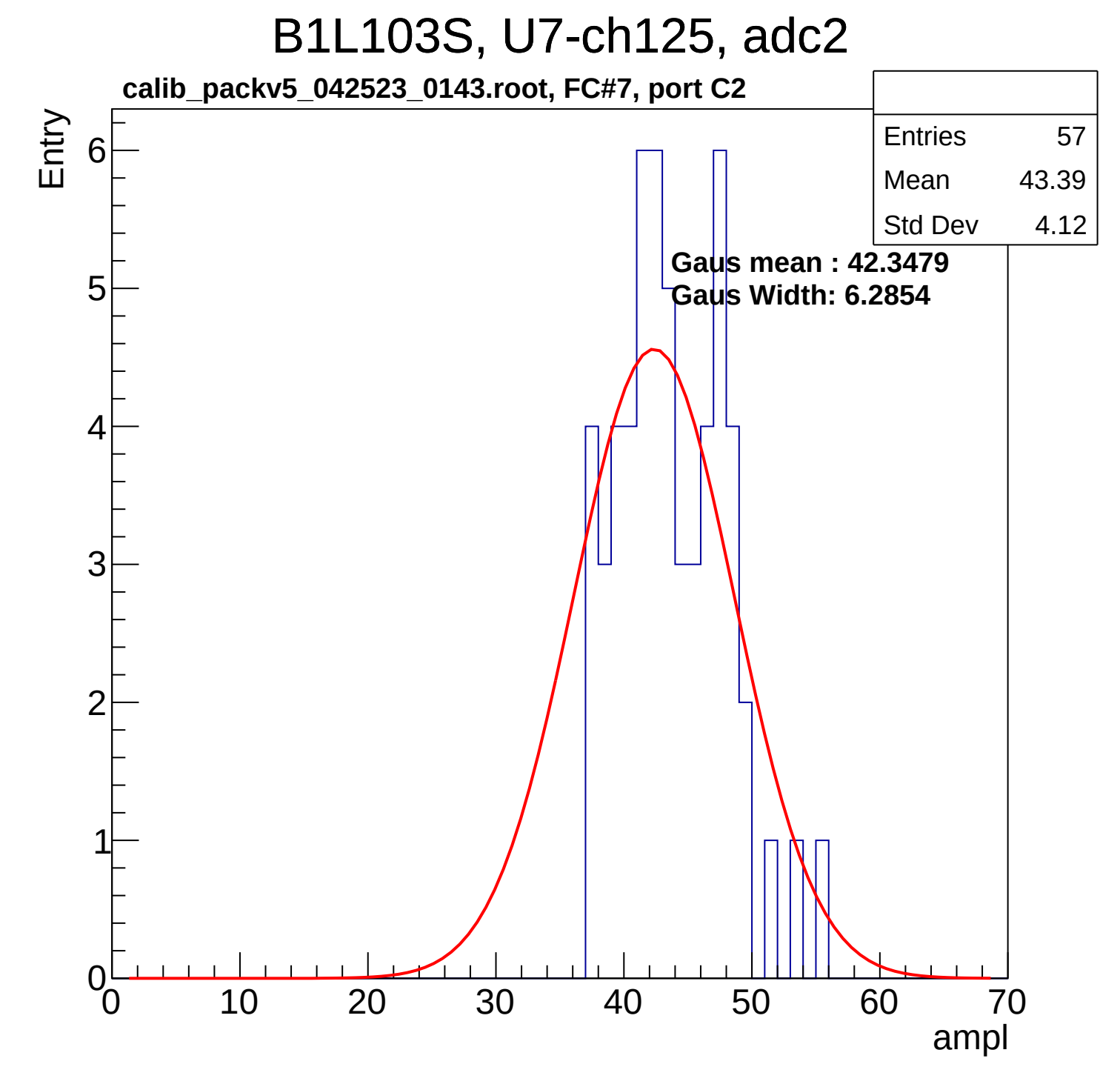
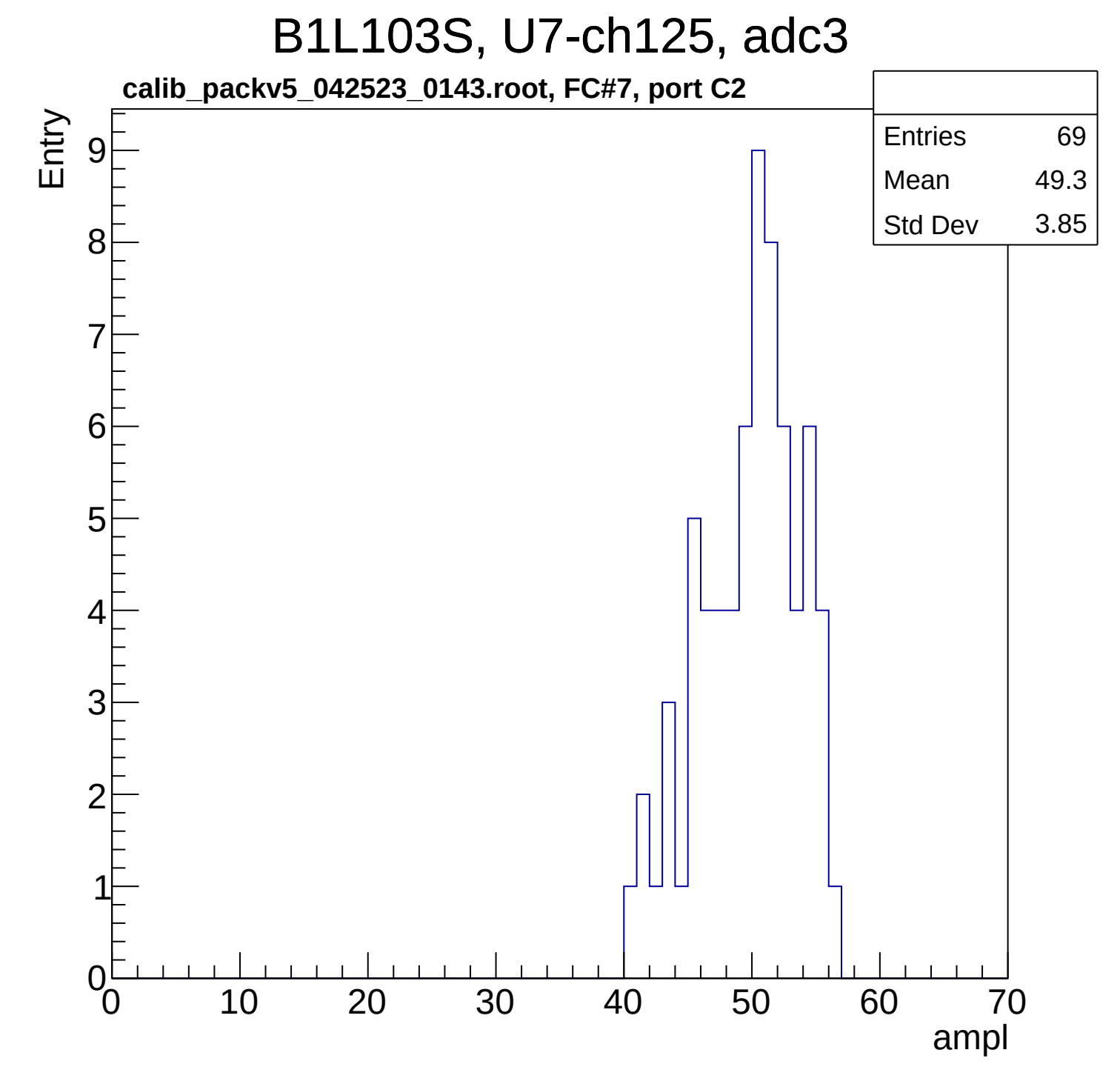

B1L103S, U7-ch124, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 16
Mean 57.5
Std Dev 14.93
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

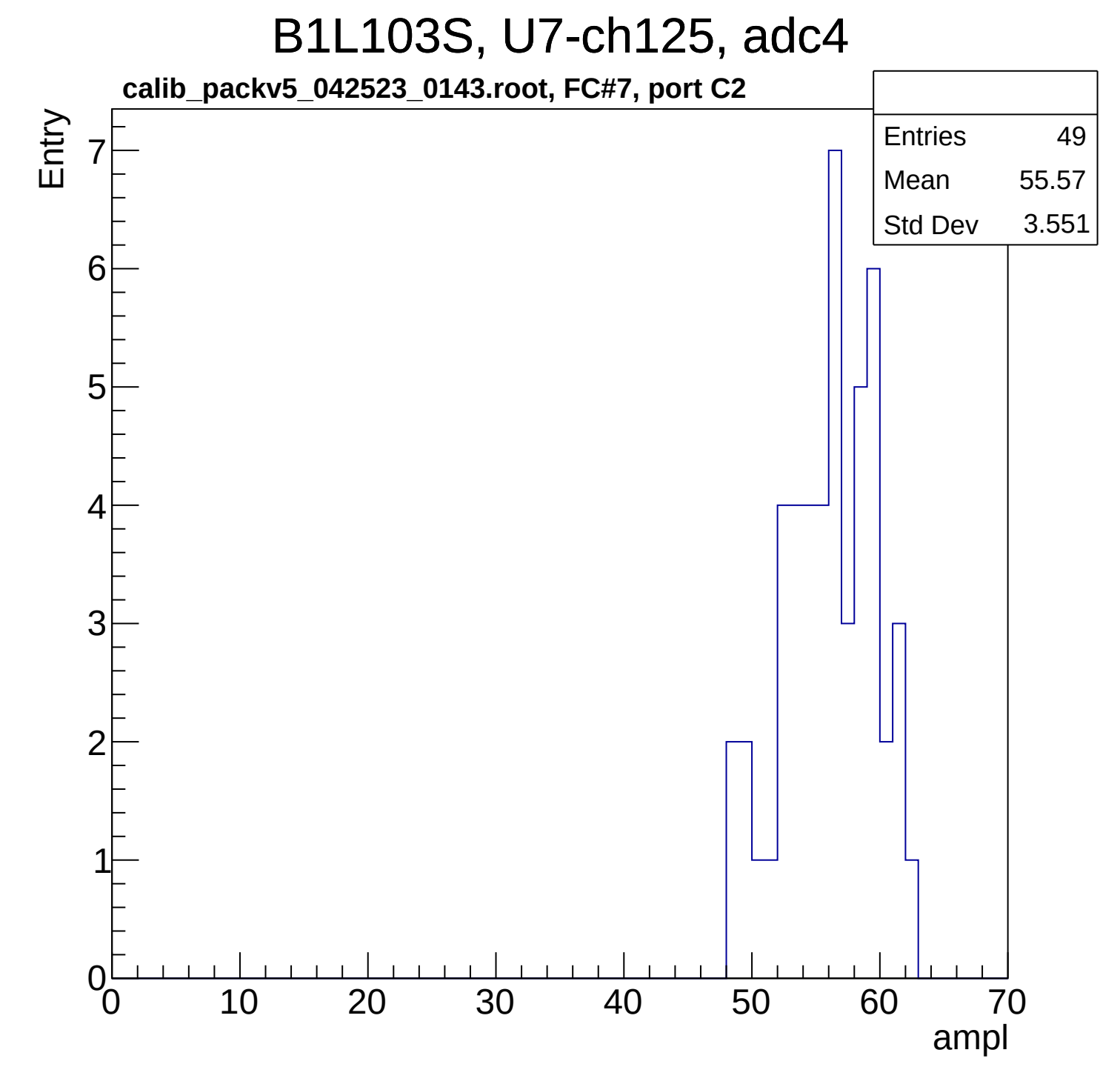

B1L103S, U7-ch124, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 4
Mean 51.75
Std Dev 18.91
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

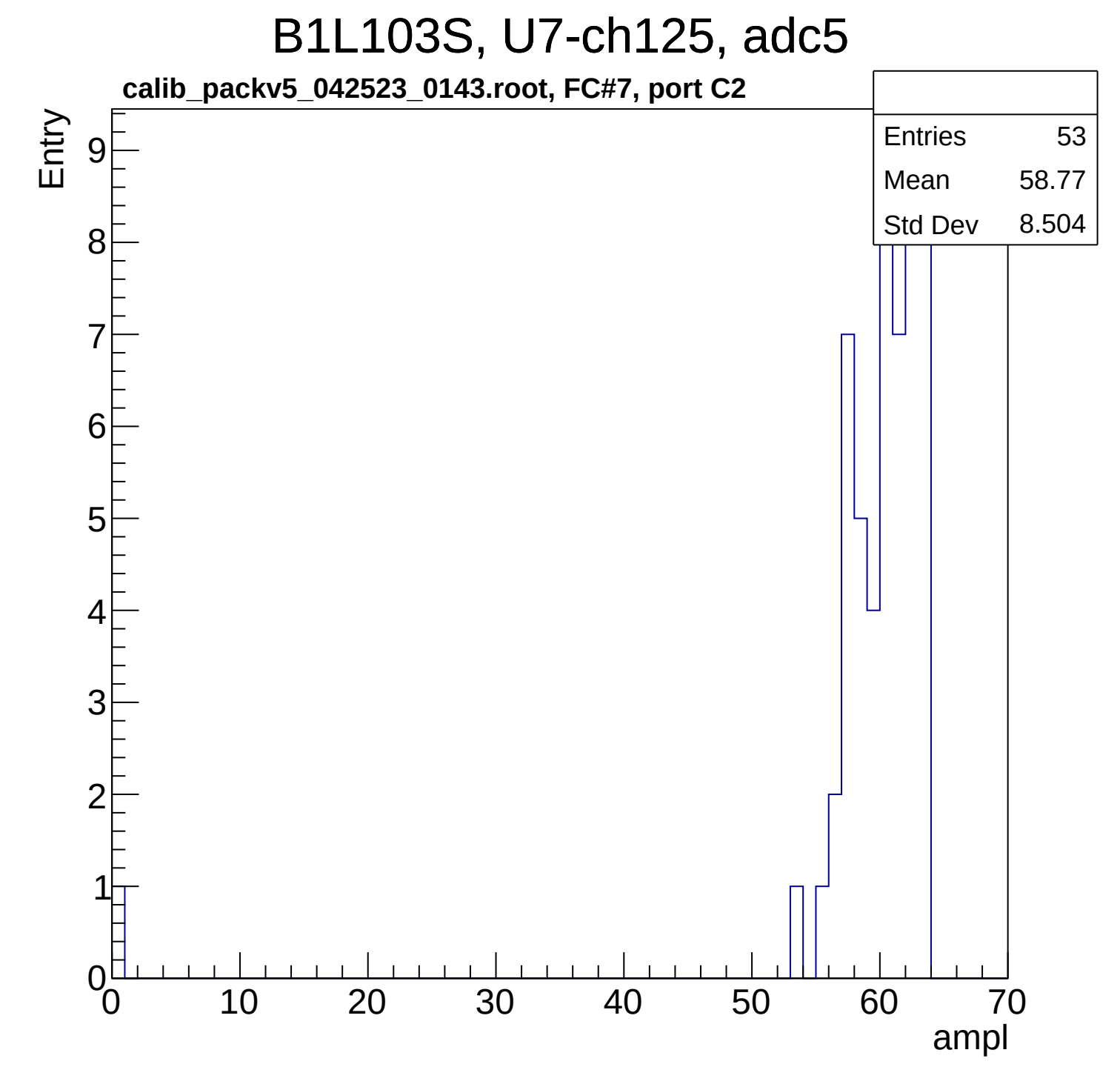

B1L103S, U7-ch125, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 30.06
Std Dev 3.837
Gaus mean : 31.1487
Gaus Width: 4.6731
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

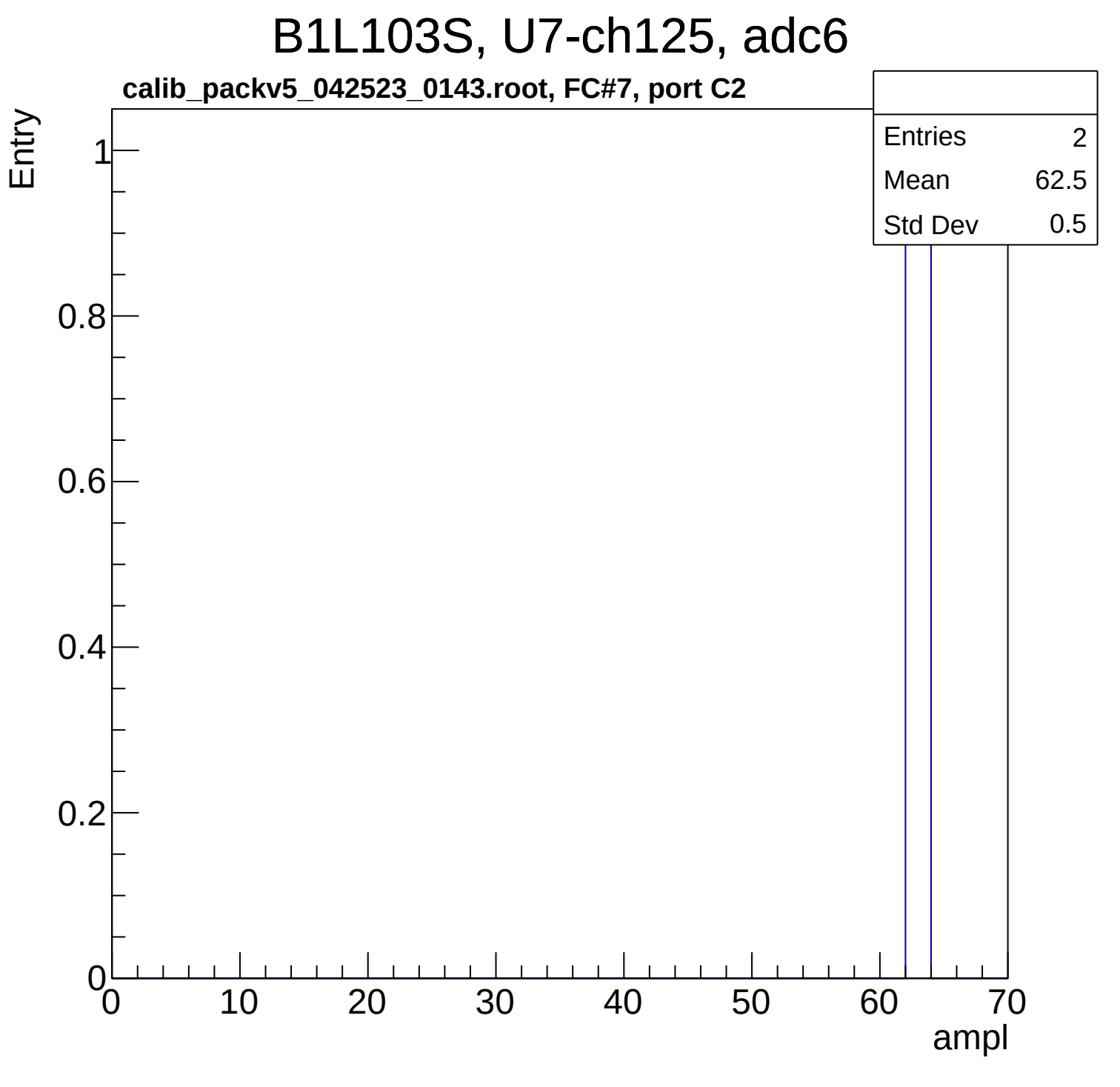

B1L103S, U7-ch125, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 71
Mean 36.9
Std Dev 6.323
Gaus mean : 37.7122
Gaus Width: 5.5727
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

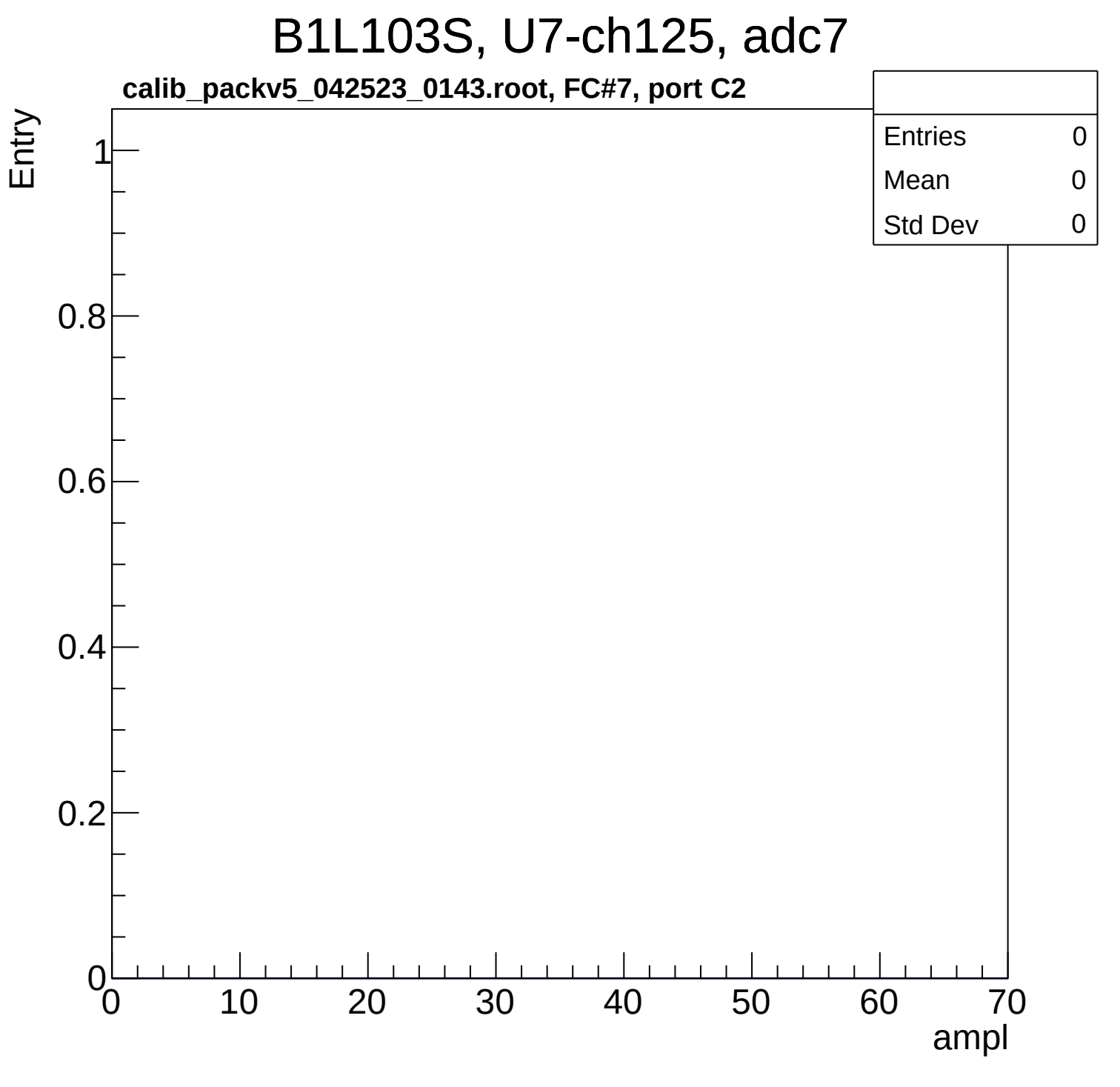

B1L103S, U7-ch125, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 43.39
Std Dev 4.12
Gaus mean : 42.3479
Gaus Width: 6.2854
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

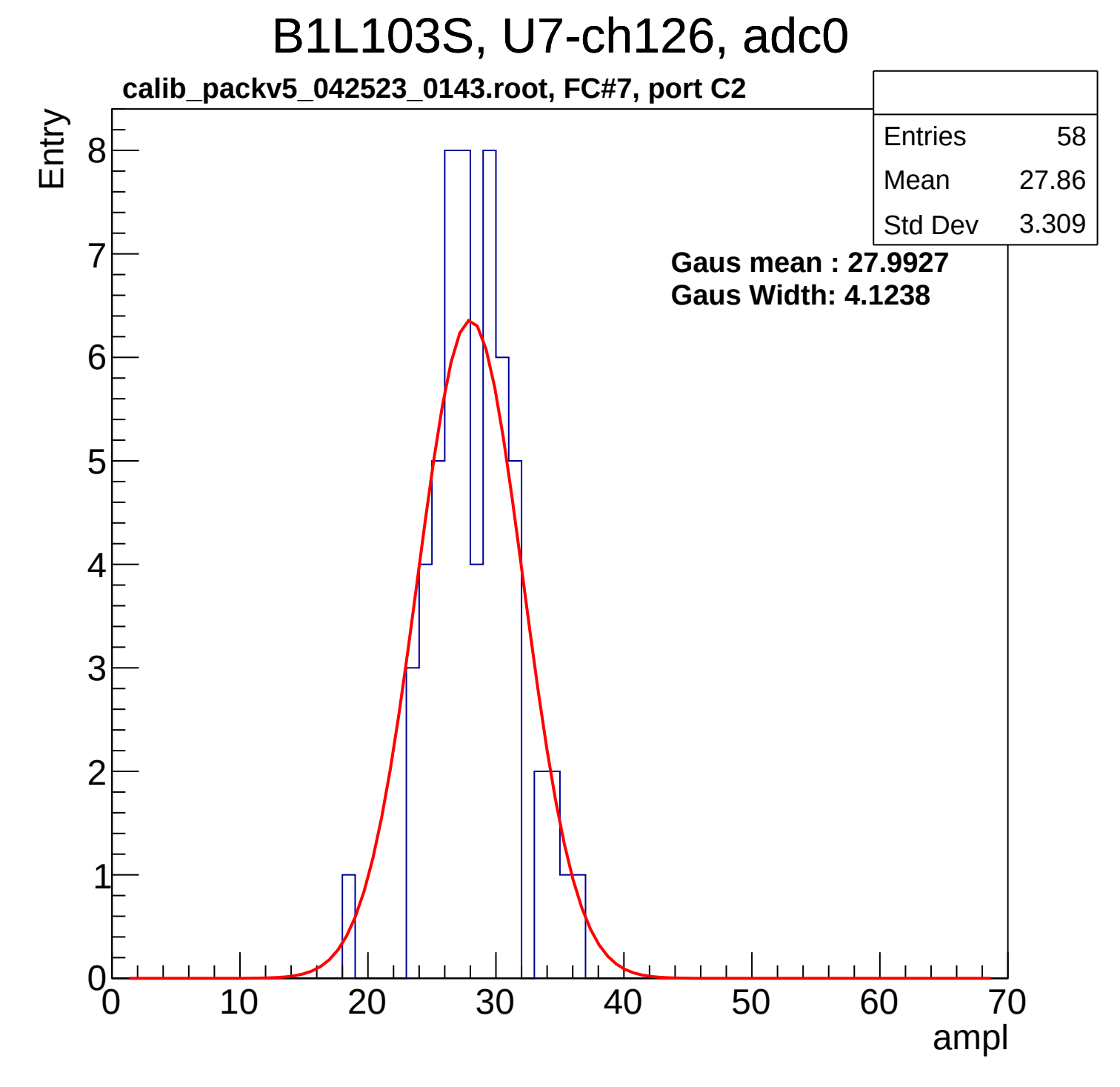

B1L103S, U7-ch125, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 49.3
Std Dev 3.85
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

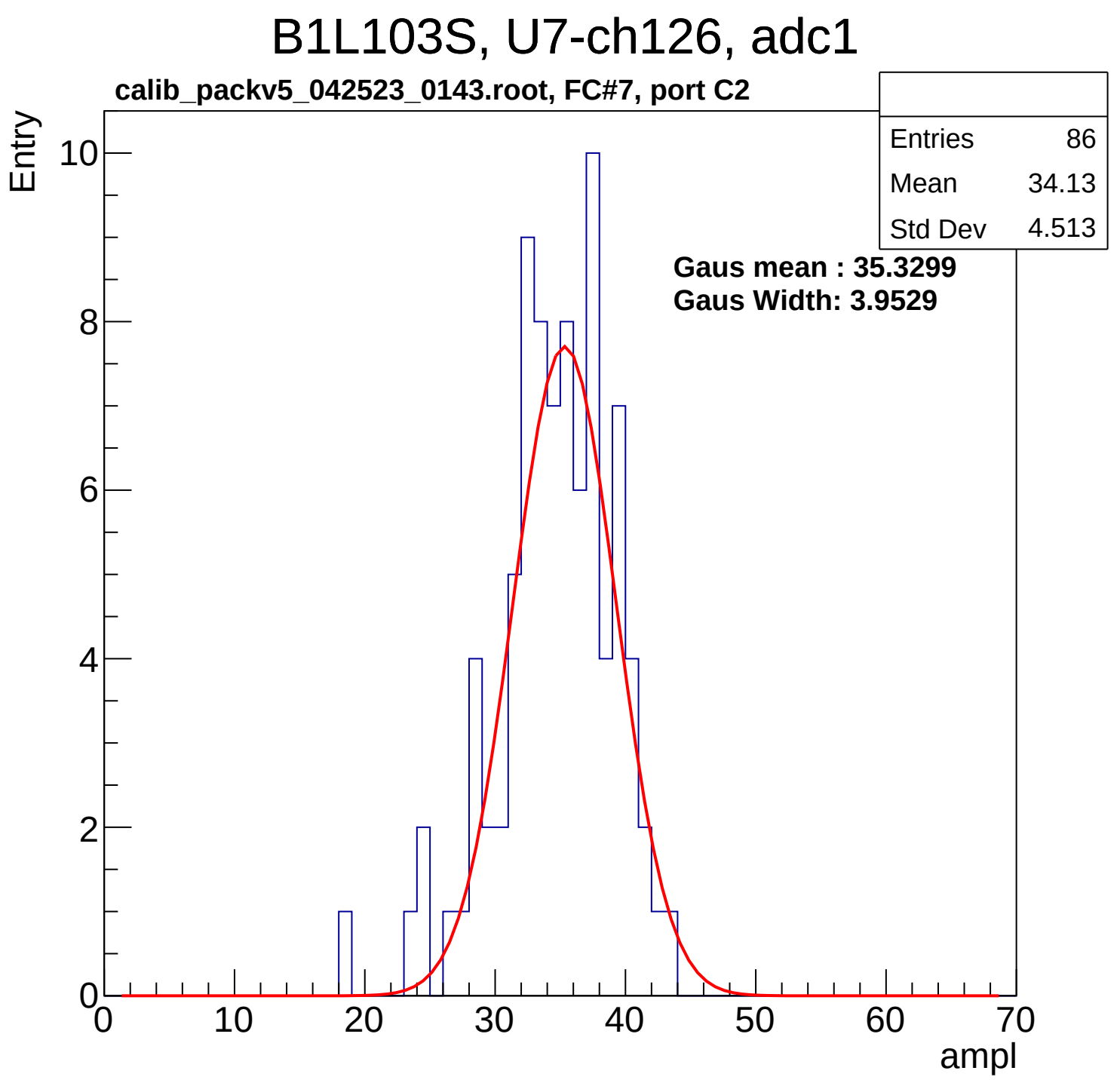

B1L103S, U7-ch125, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 49
Mean 55.57
Std Dev 3.551
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

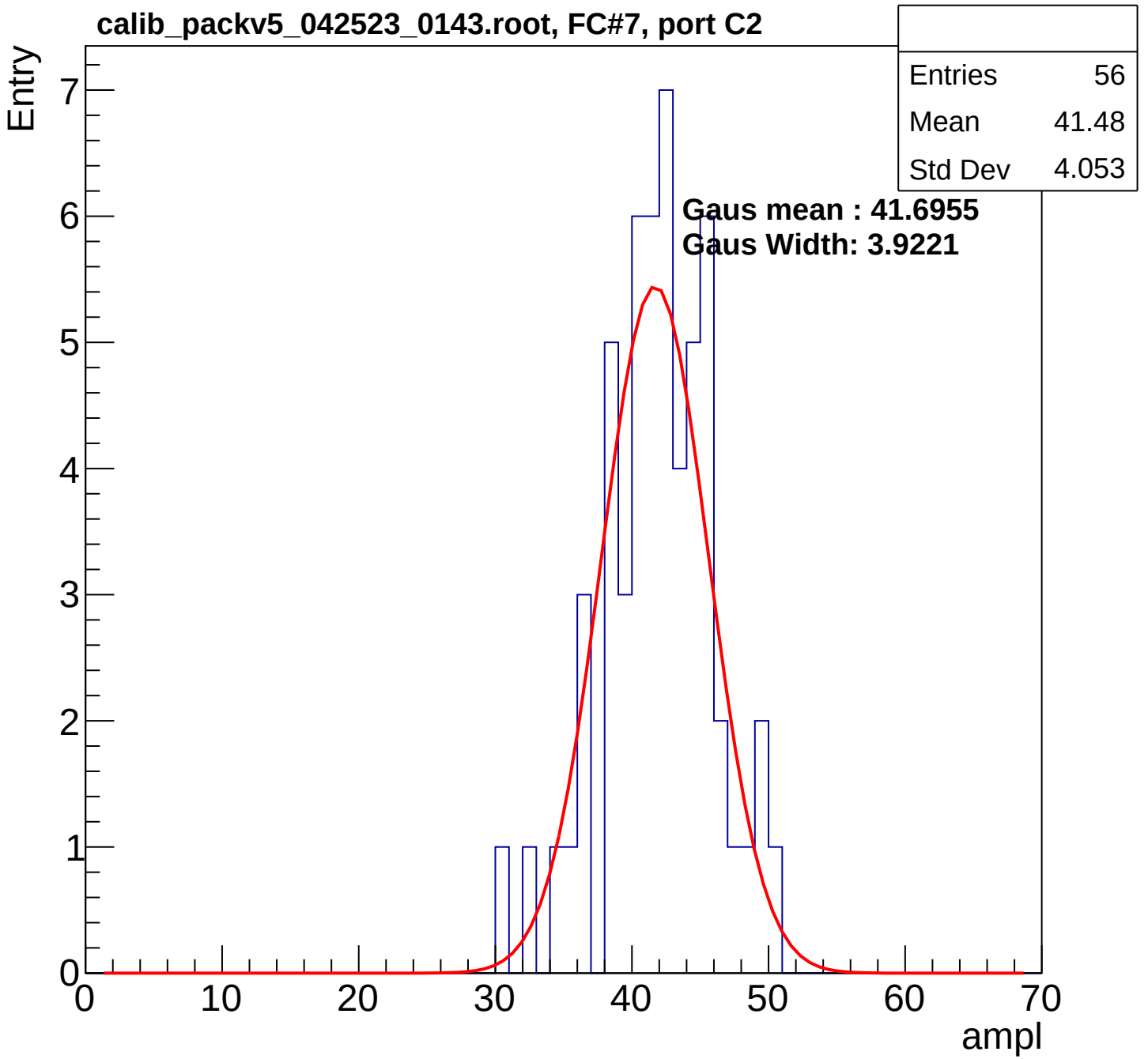

B1L103S, U7-ch125, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 58.77
Std Dev 8.504
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

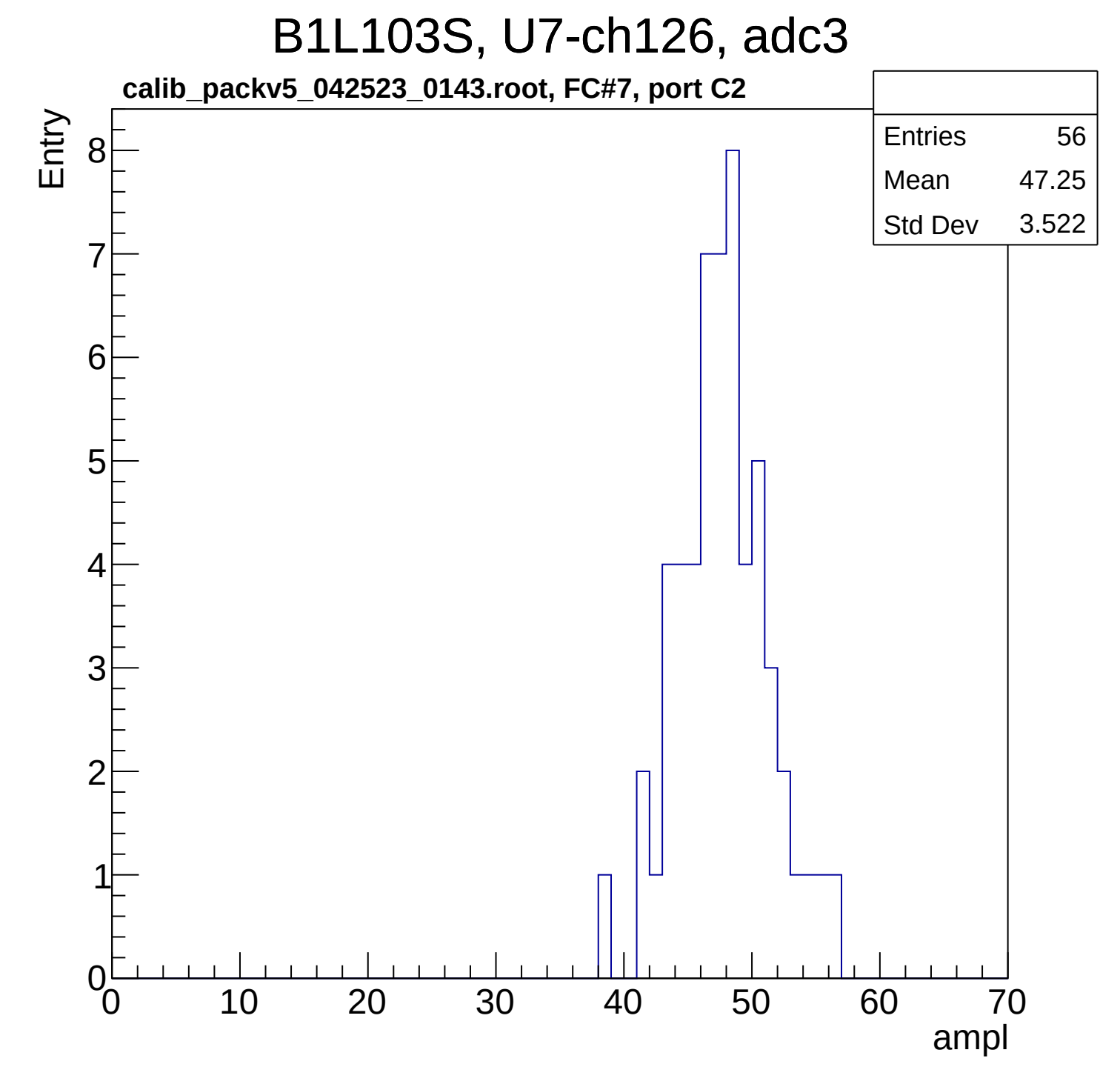

B1L103S, U7-ch125, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

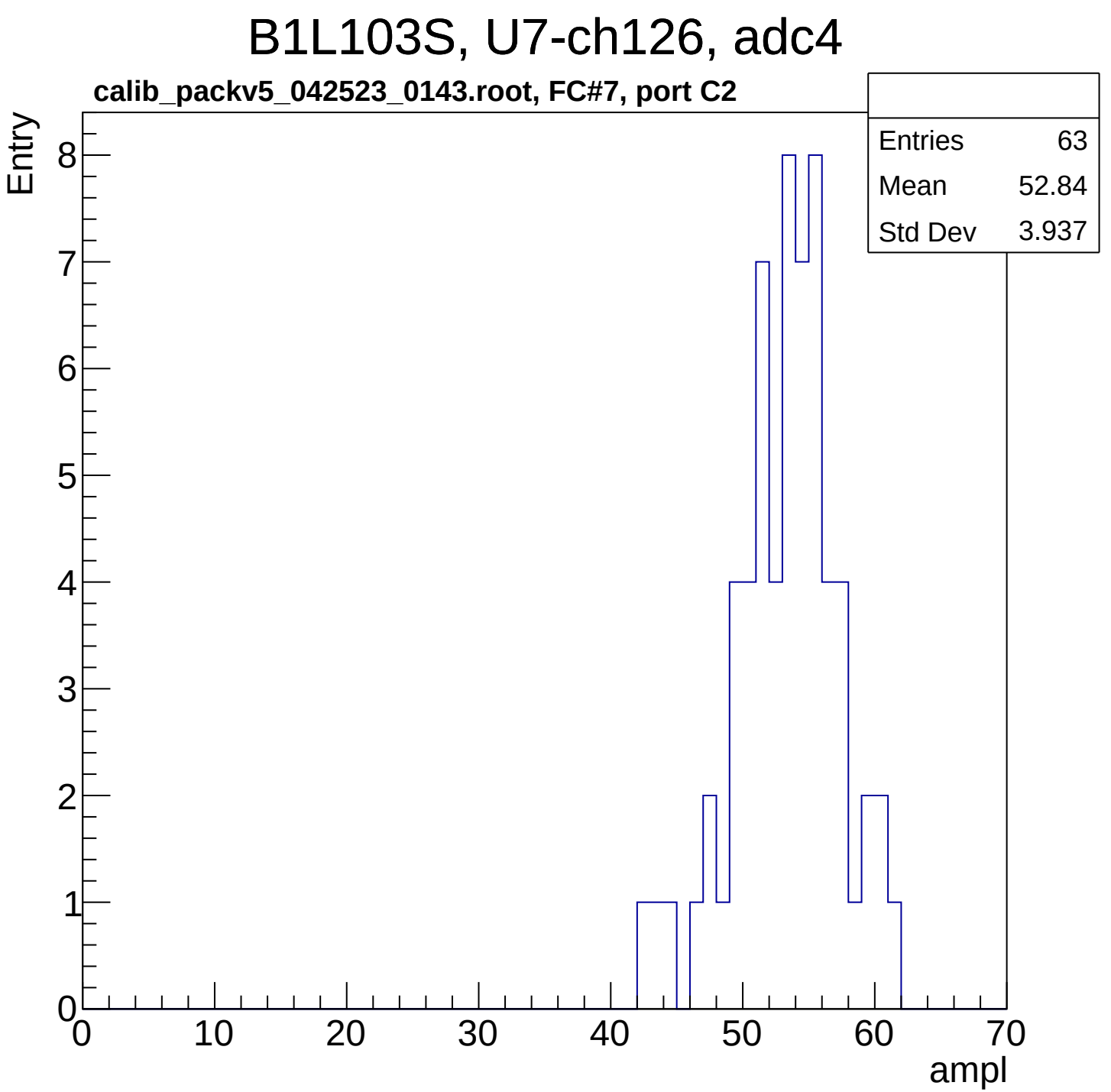

B1L103S, U7-ch125, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

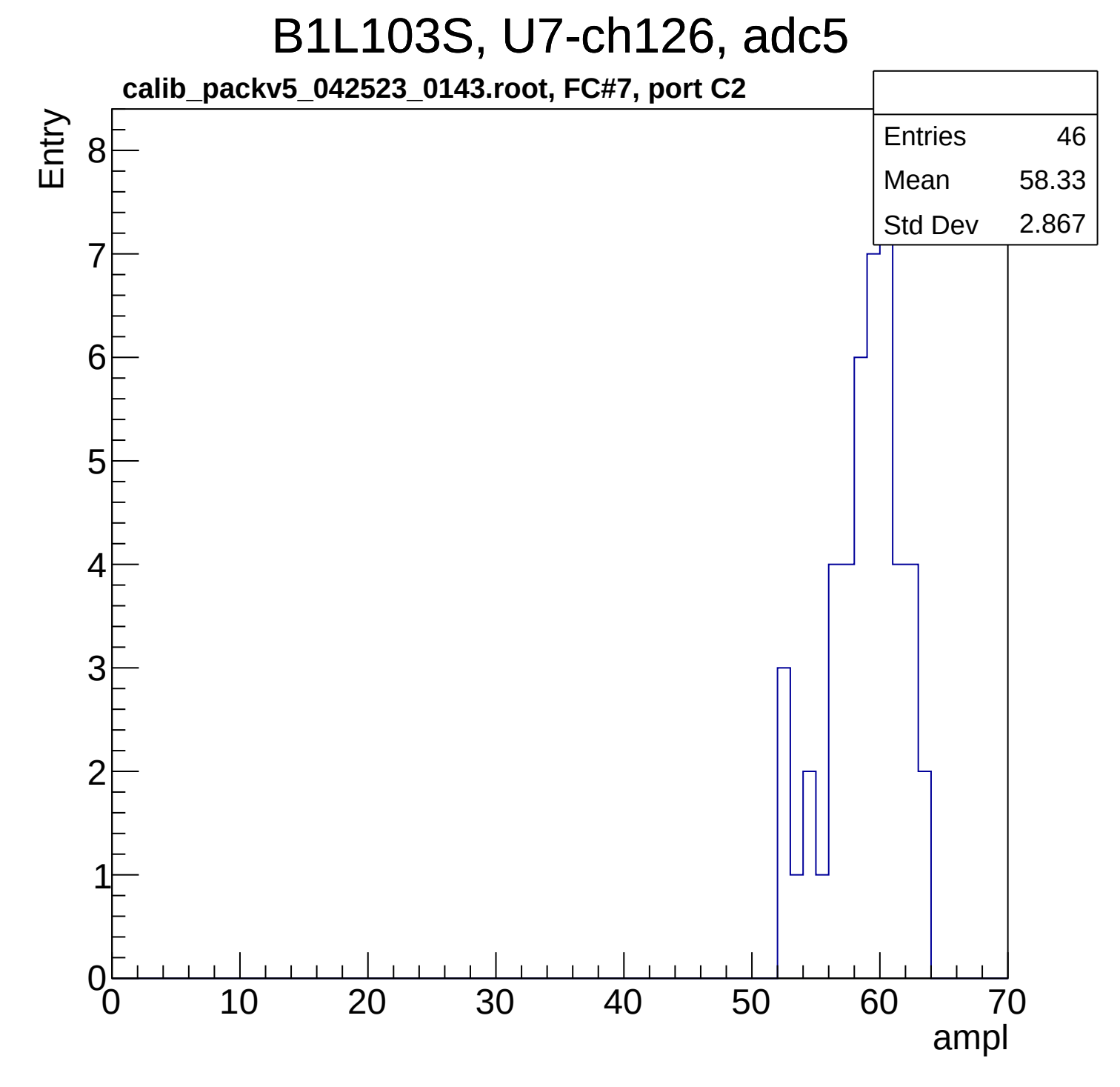

B1L103S, U7-ch126, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 58
Mean 27.86
Std Dev 3.309
Gaus mean : 27.9927
Gaus Width: 4.1238
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

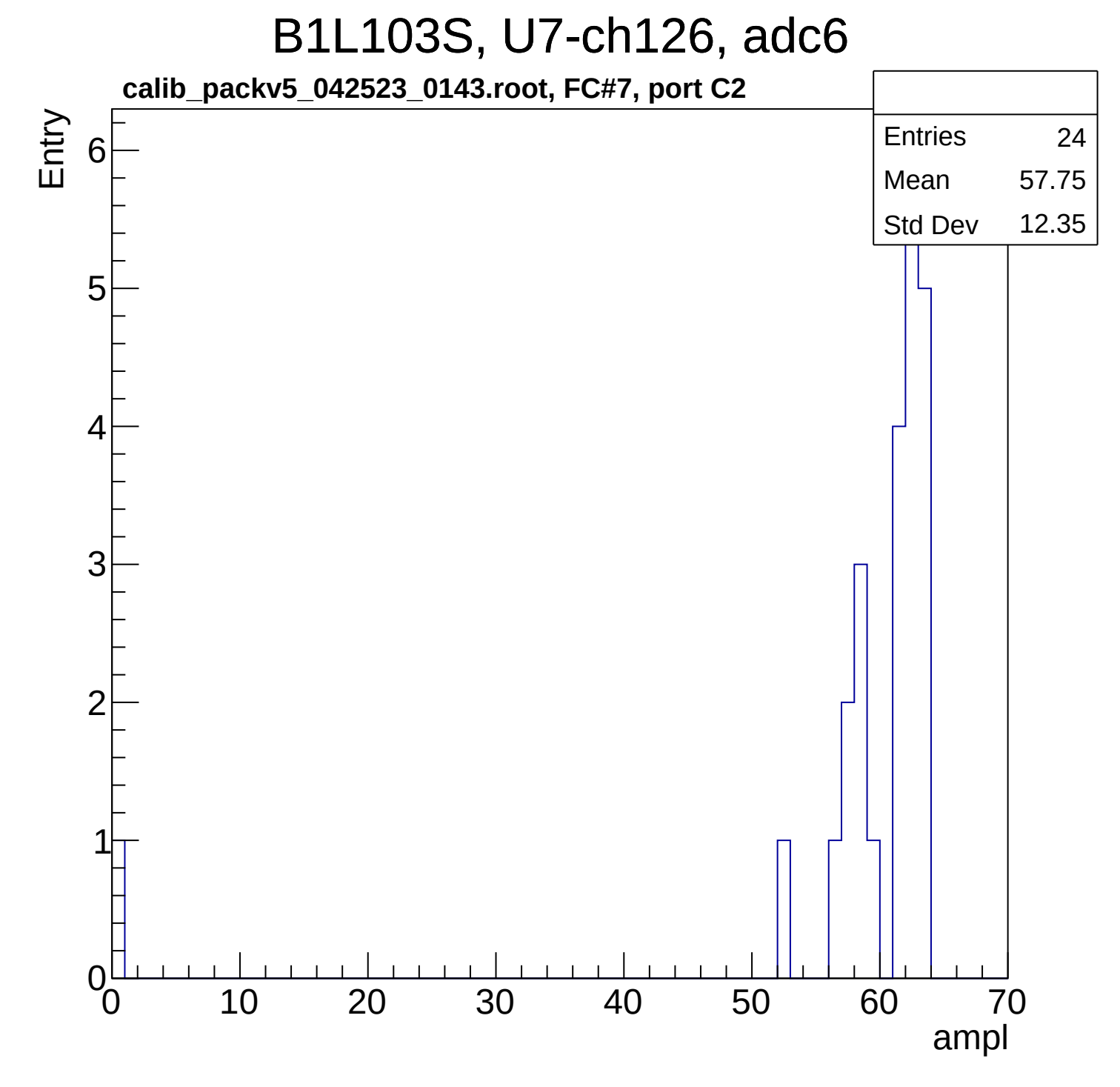

B1L103S, U7-ch126, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 86
Mean 34.13
Std Dev 4.513
Gaus mean : 35.3299
Gaus Width: 3.9529
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

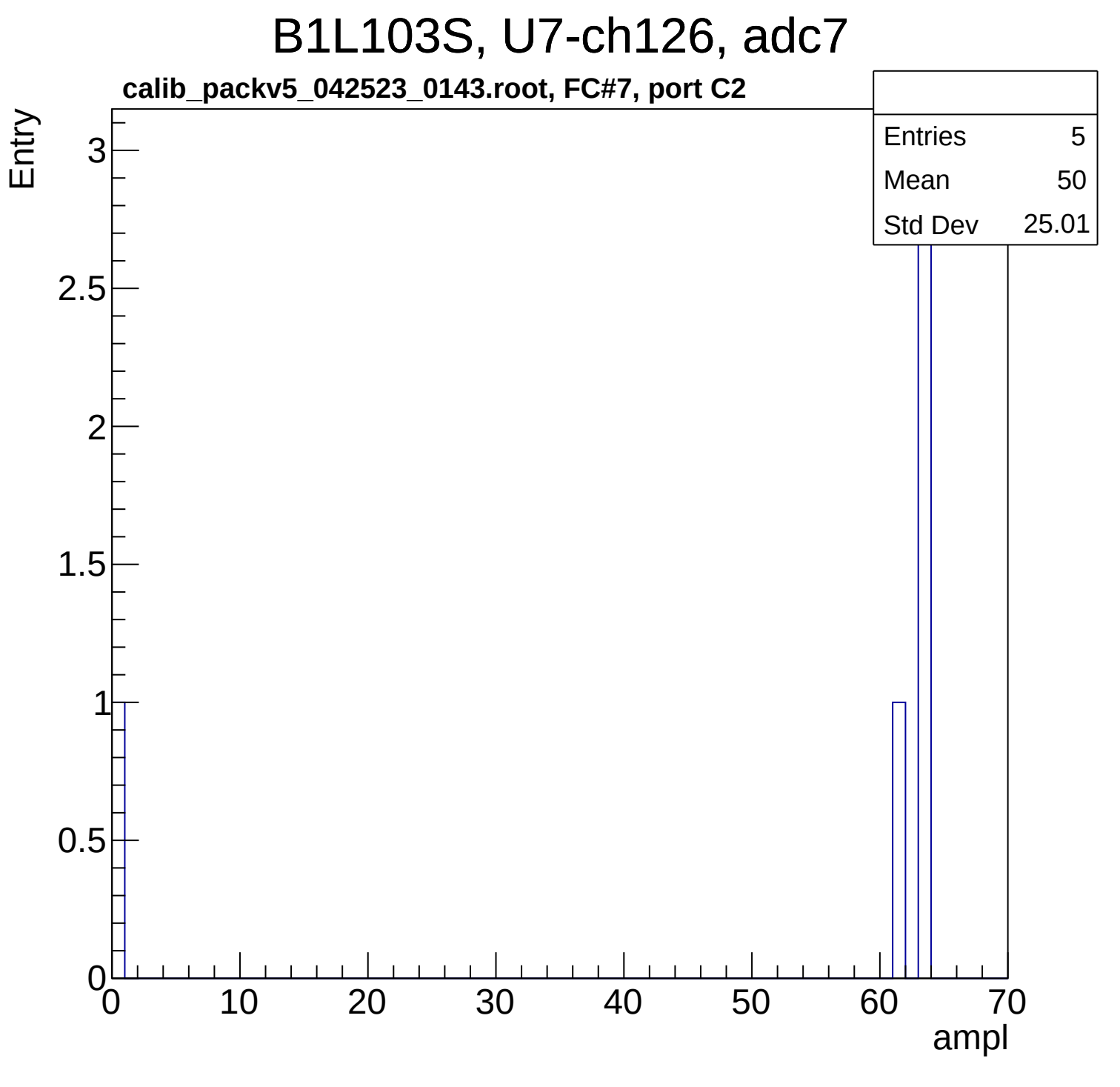

B1L103S, U7-ch126, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 41.48
Std Dev 4.053
Gaus mean : 41.6955
Gaus Width: 3.9221
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

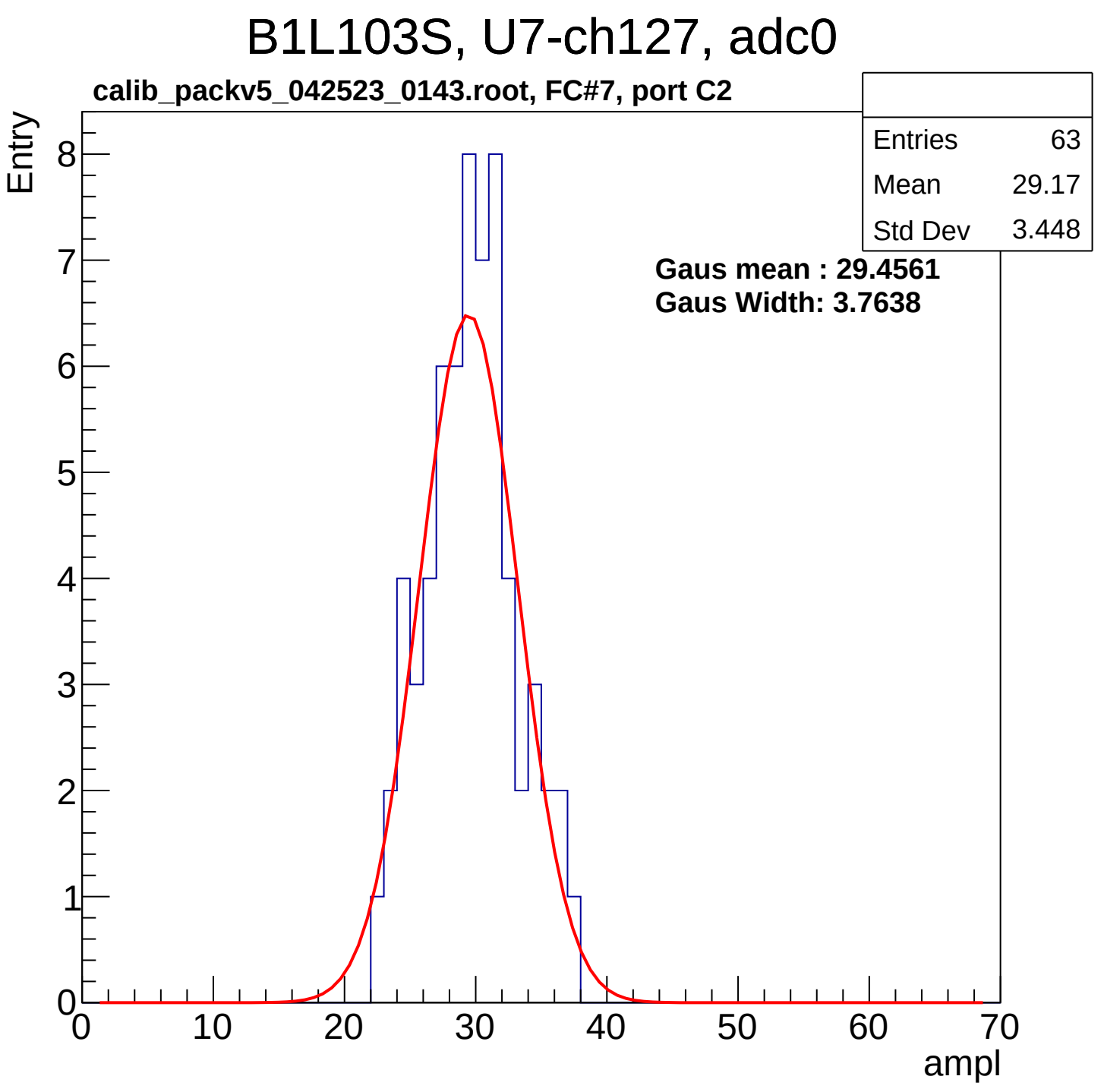

B1L103S, U7-ch126, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 47.25
Std Dev 3.522
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

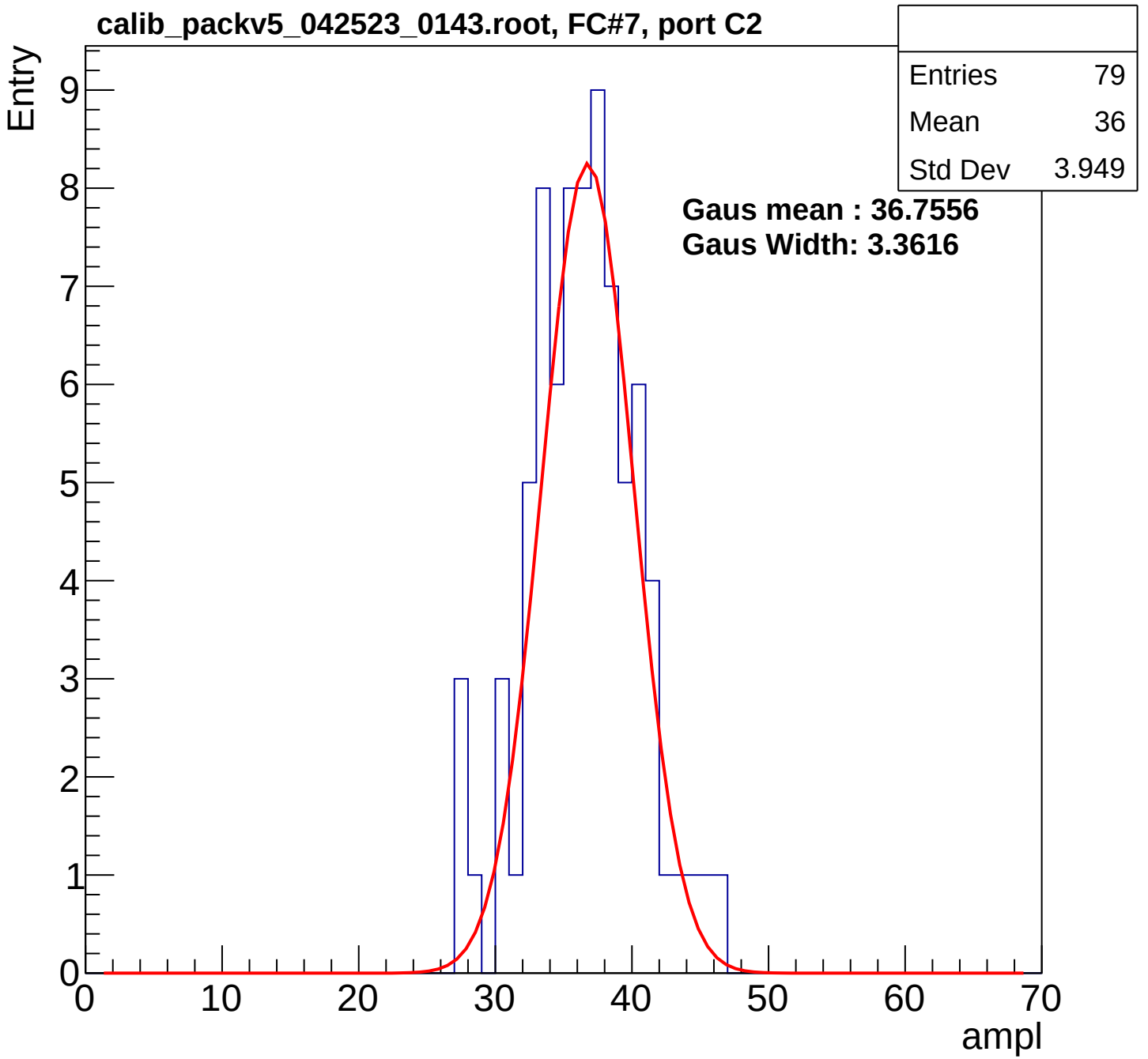

B1L103S, U7-ch126, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 52.84
Std Dev 3.937
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

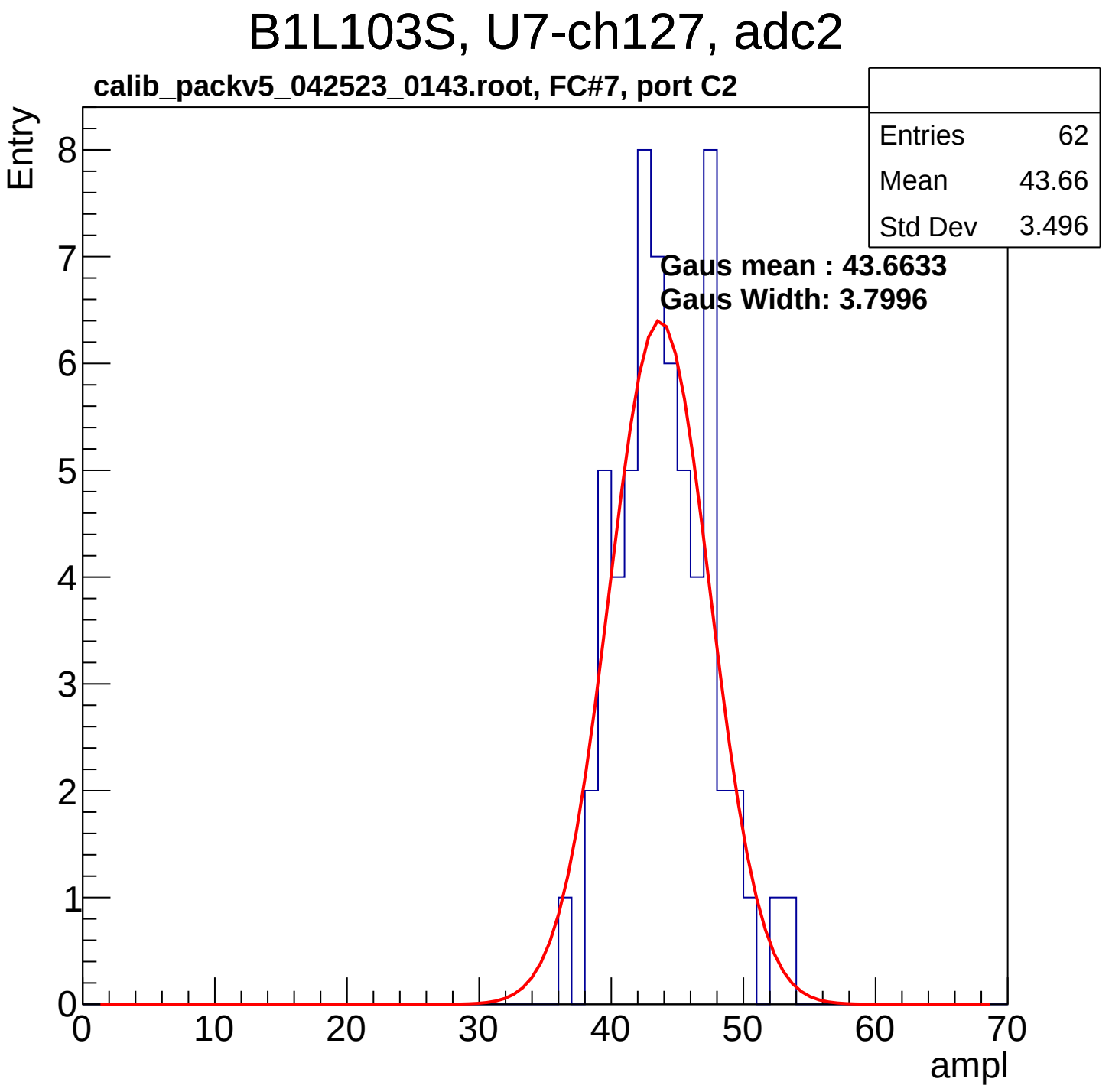

B1L103S, U7-ch126, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 46
Mean 58.33
Std Dev 2.867
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

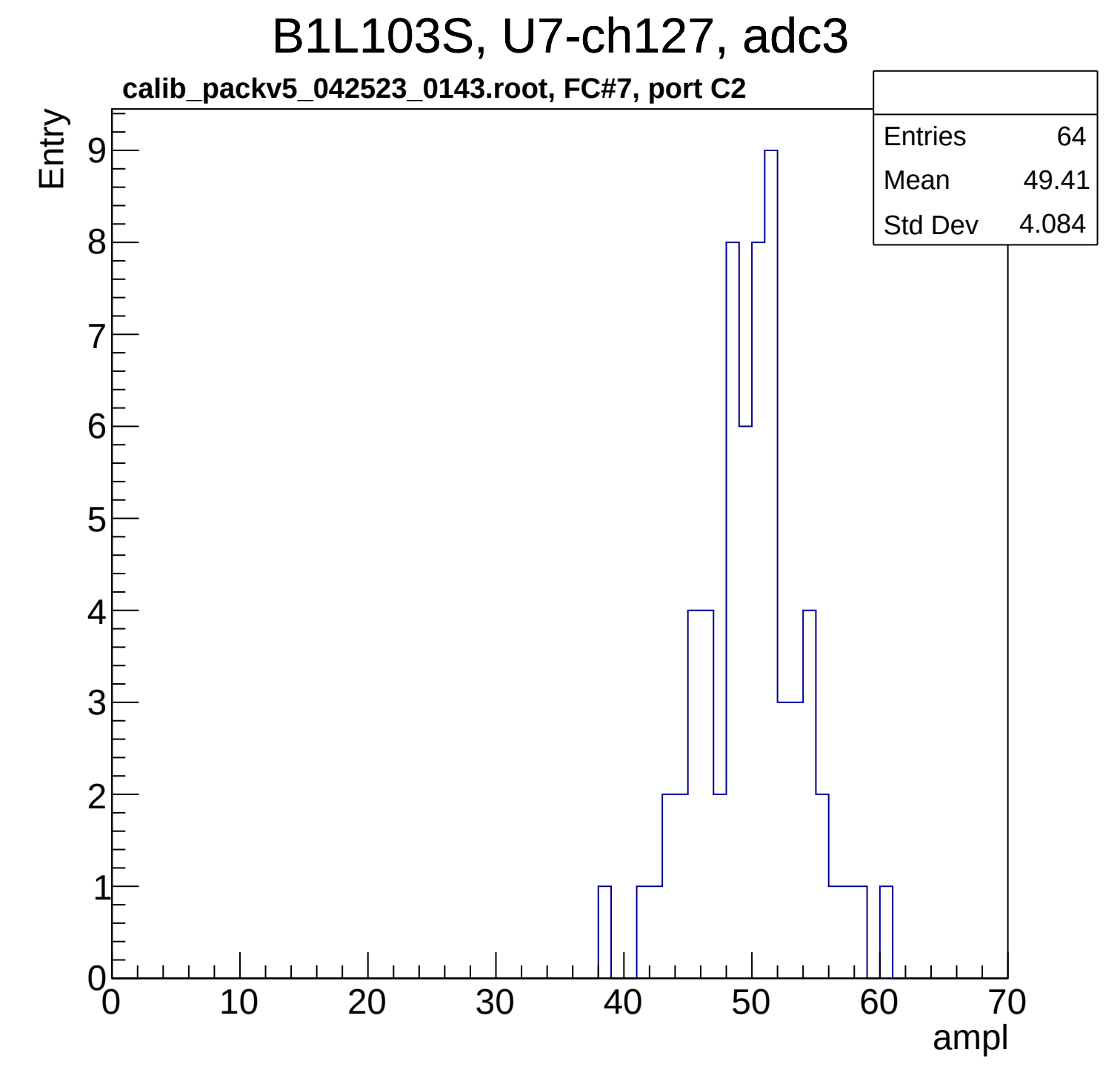

B1L103S, U7-ch126, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 24
Mean 57.75
Std Dev 12.35
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U7-ch126, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 5
Mean 50
Std Dev 25.01
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U7-ch127, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 29.17
Std Dev 3.448
Gaus mean : 29.4561
Gaus Width: 3.7638
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch127, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 79
Mean 36
Std Dev 3.949
Gaus mean : 36.7556
Gaus Width: 3.3616
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch127, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 62
Mean 43.66
Std Dev 3.496
Gaus mean : 43.6633
Gaus Width: 3.7996
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch127, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 49.41
Std Dev 4.084
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
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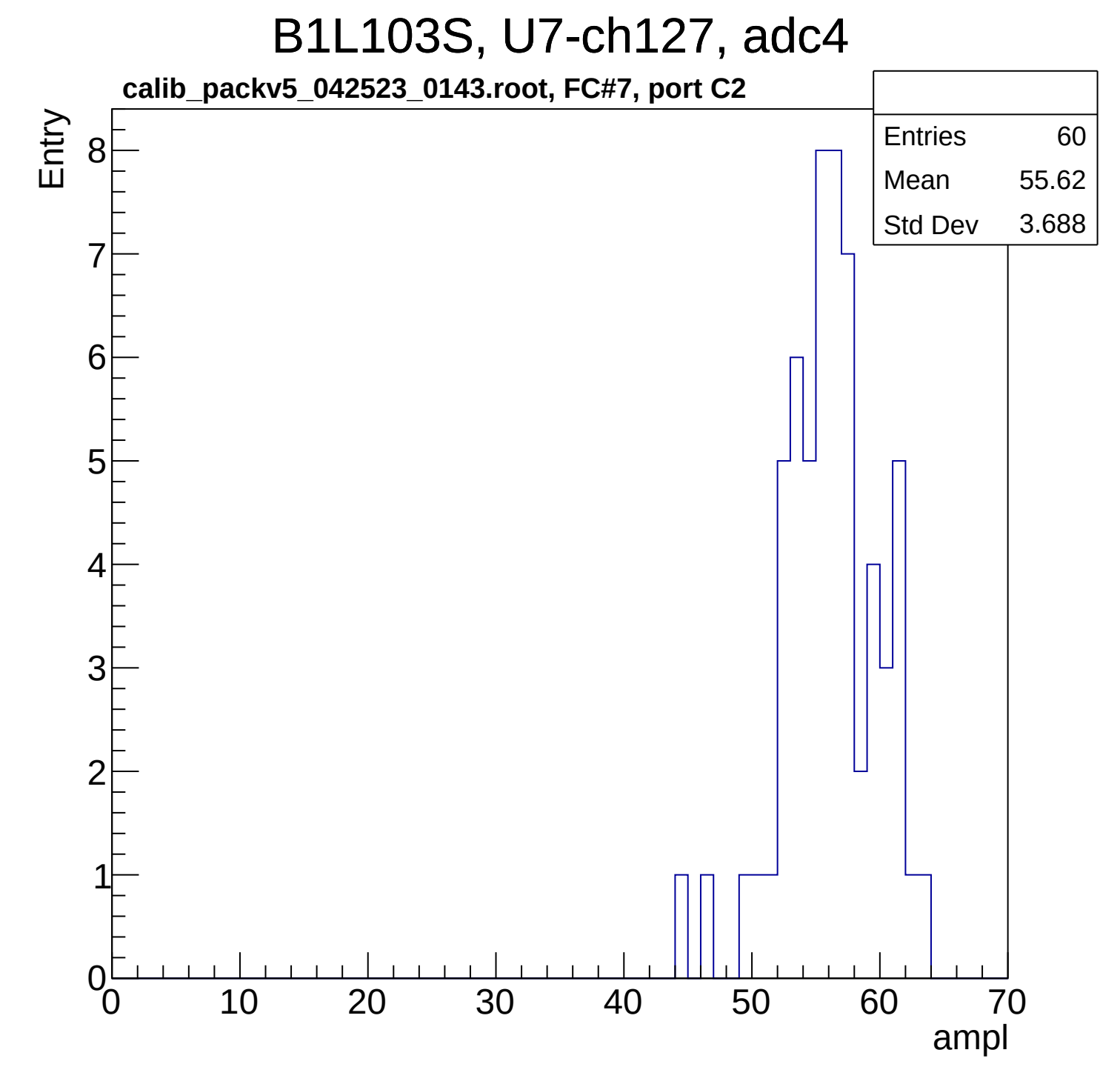
40
50
60
70


B1L103S, U7-ch127, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 60
Mean 55.62
Std Dev 3.688
Entry
ampl
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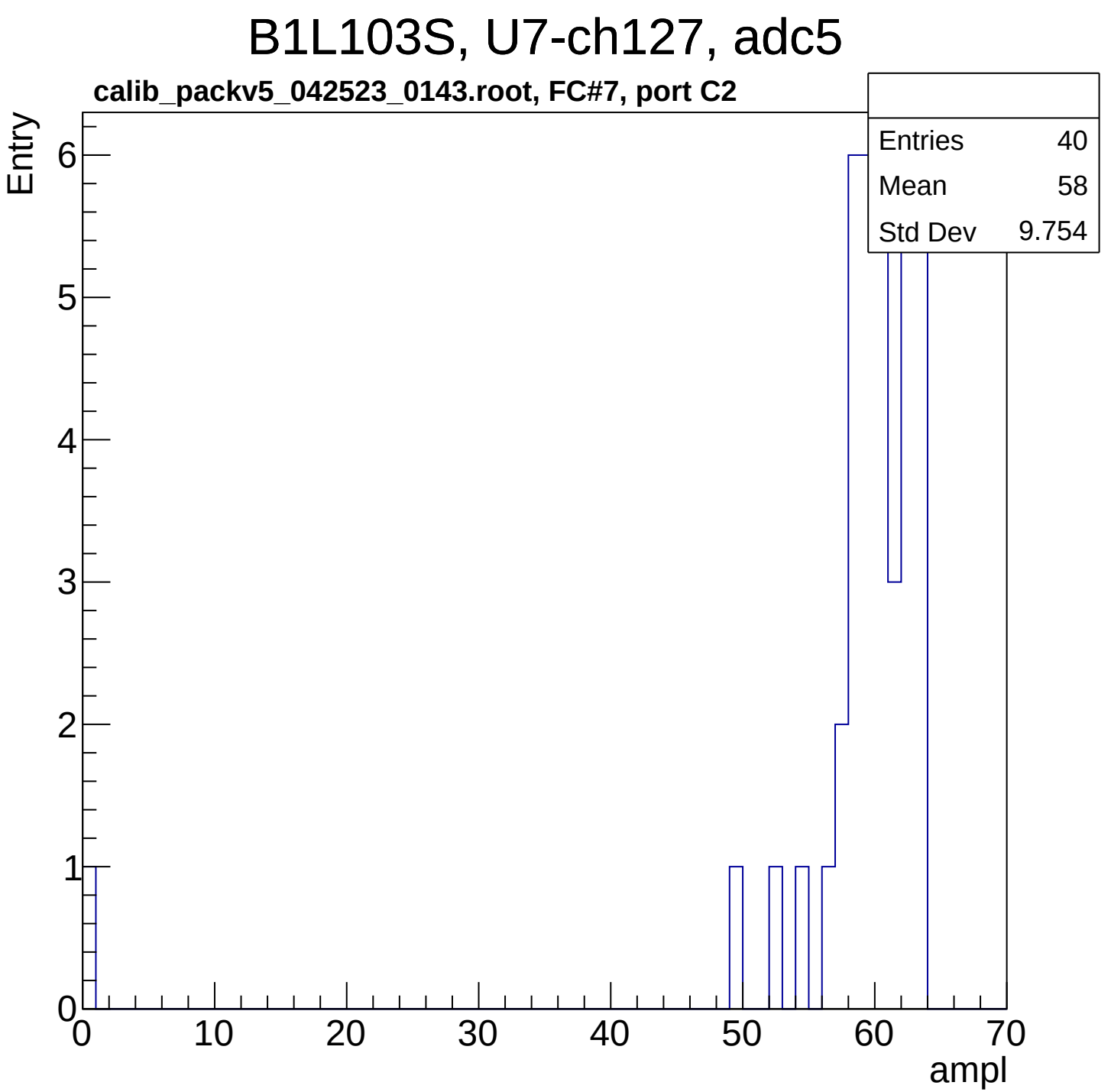
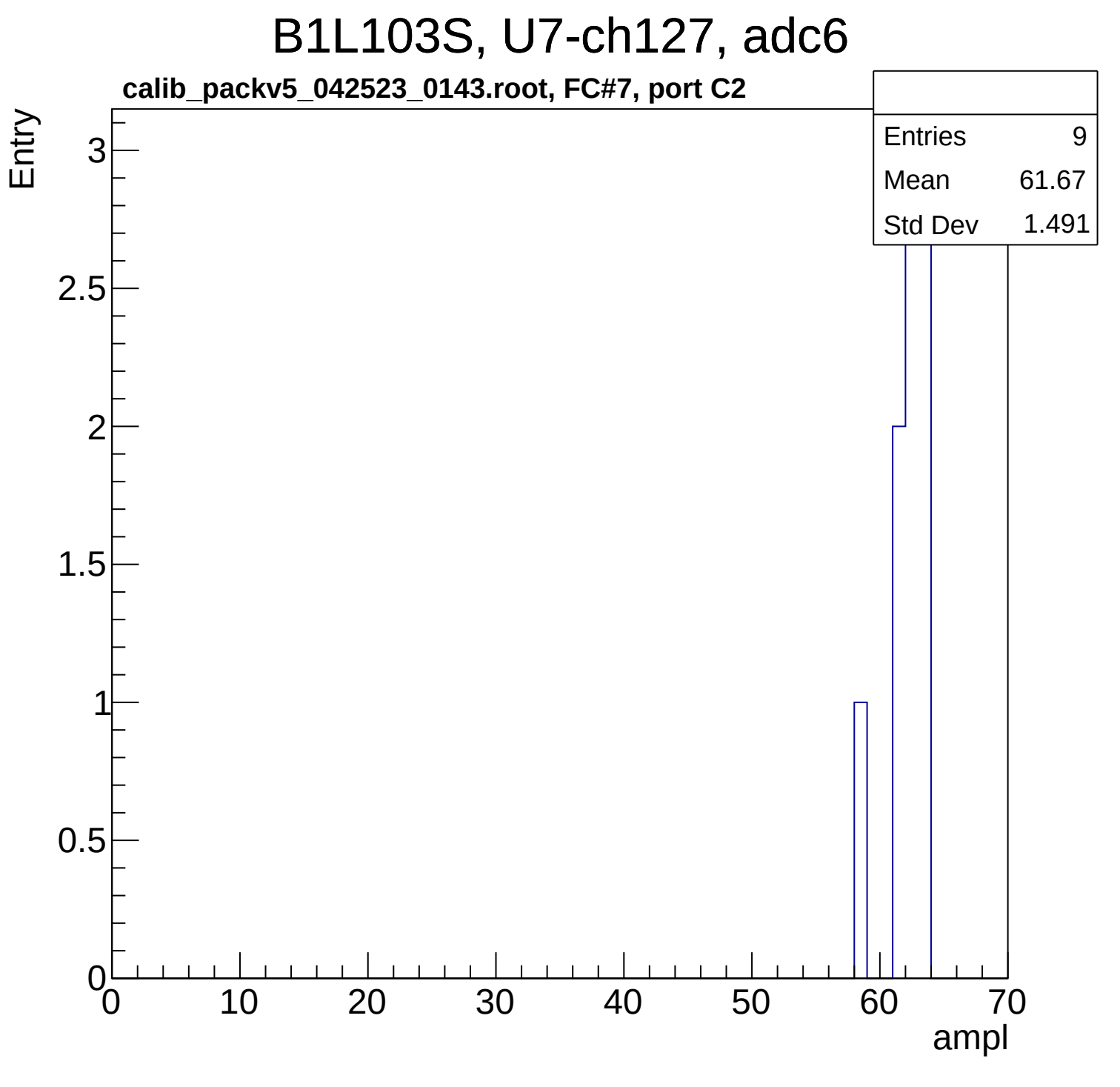
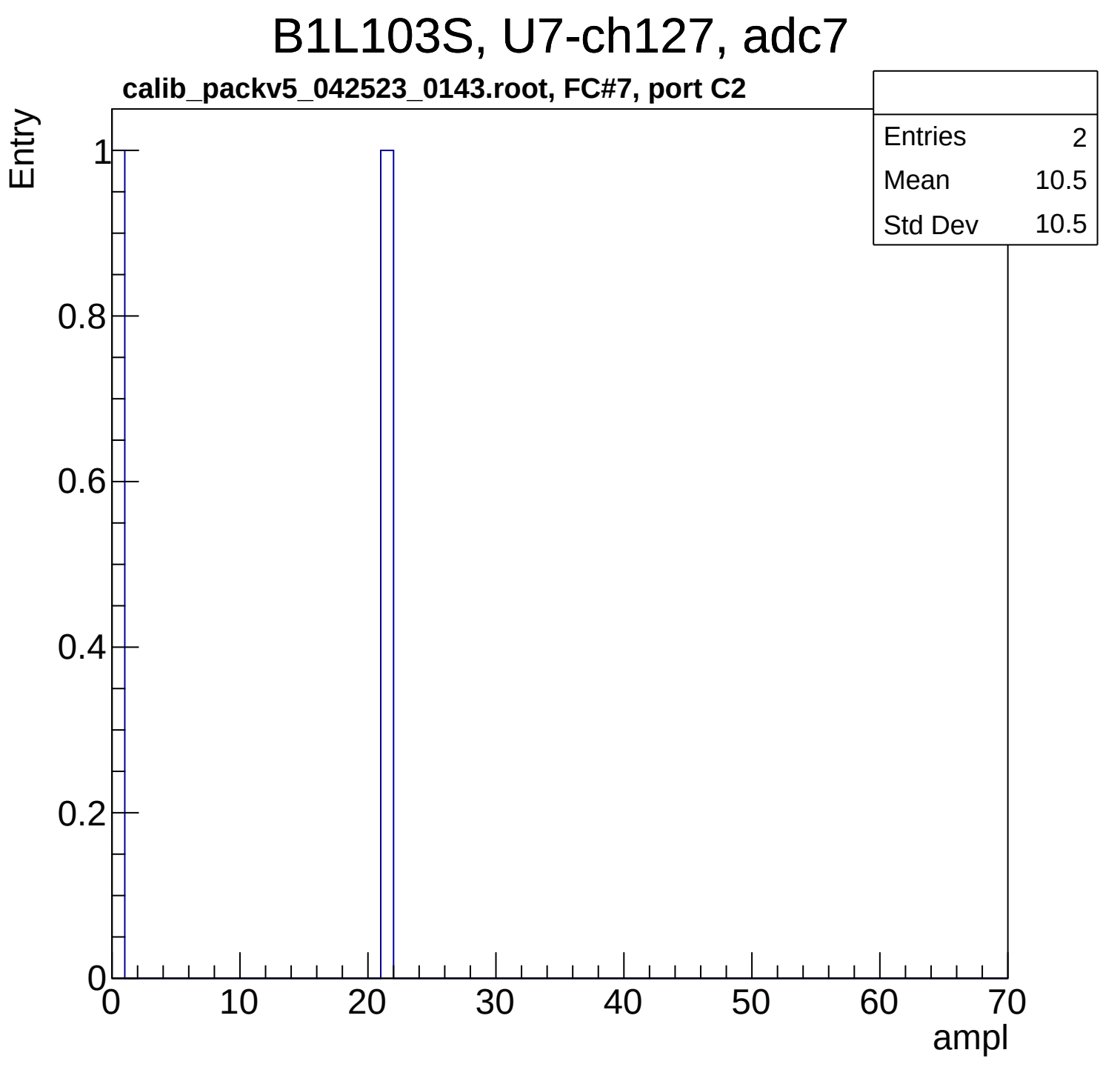
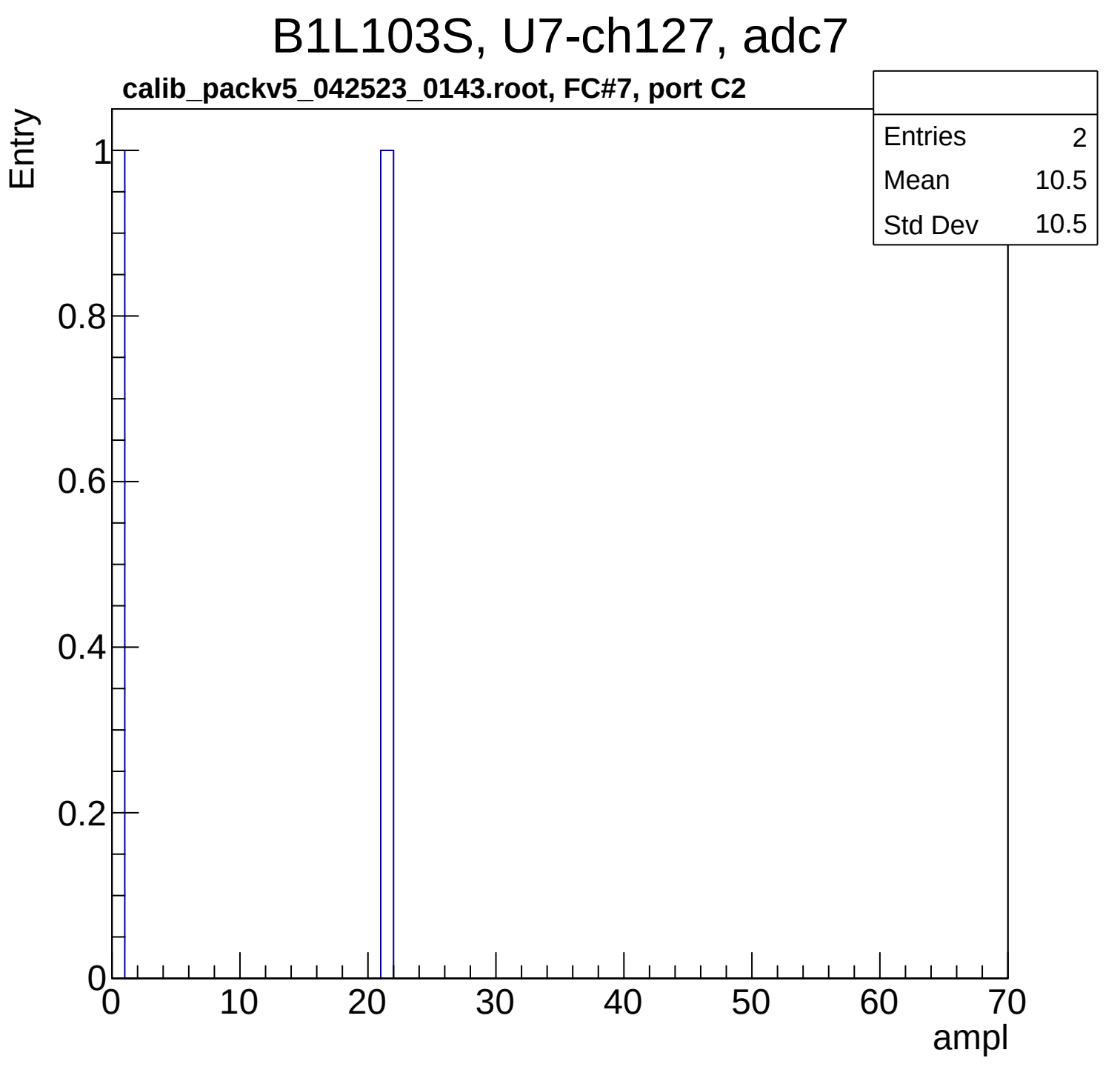
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch127, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 40
Mean 58
Std Dev 9.754
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch127, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 9
Mean 61.67
Std Dev 1.491
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U7-ch127, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 10.5
Std Dev 10.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch127, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 10.5
Std Dev 10.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl