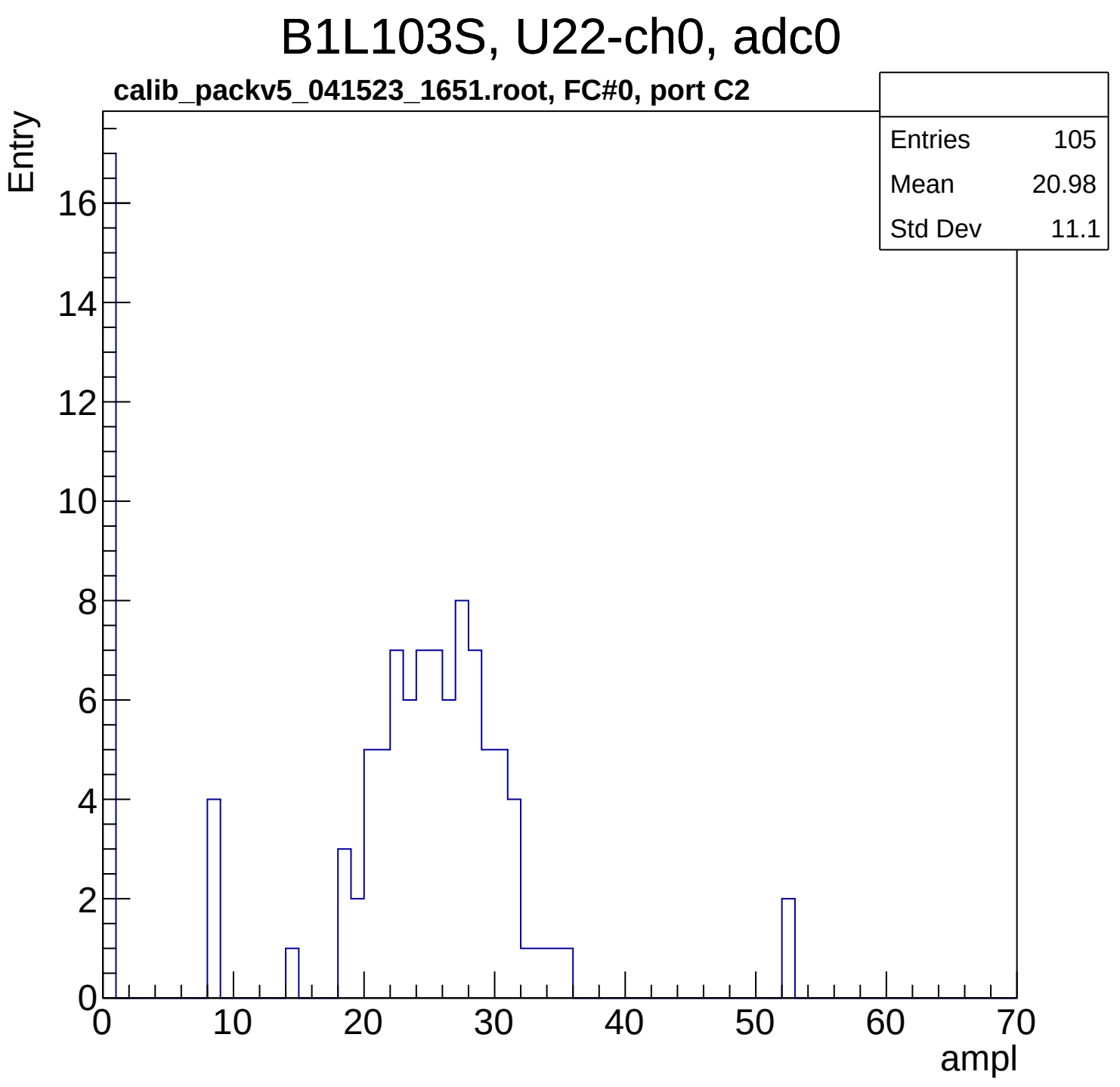
B1L103S, U22-ch0, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 105
Mean 20.98
Std Dev 11.1
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
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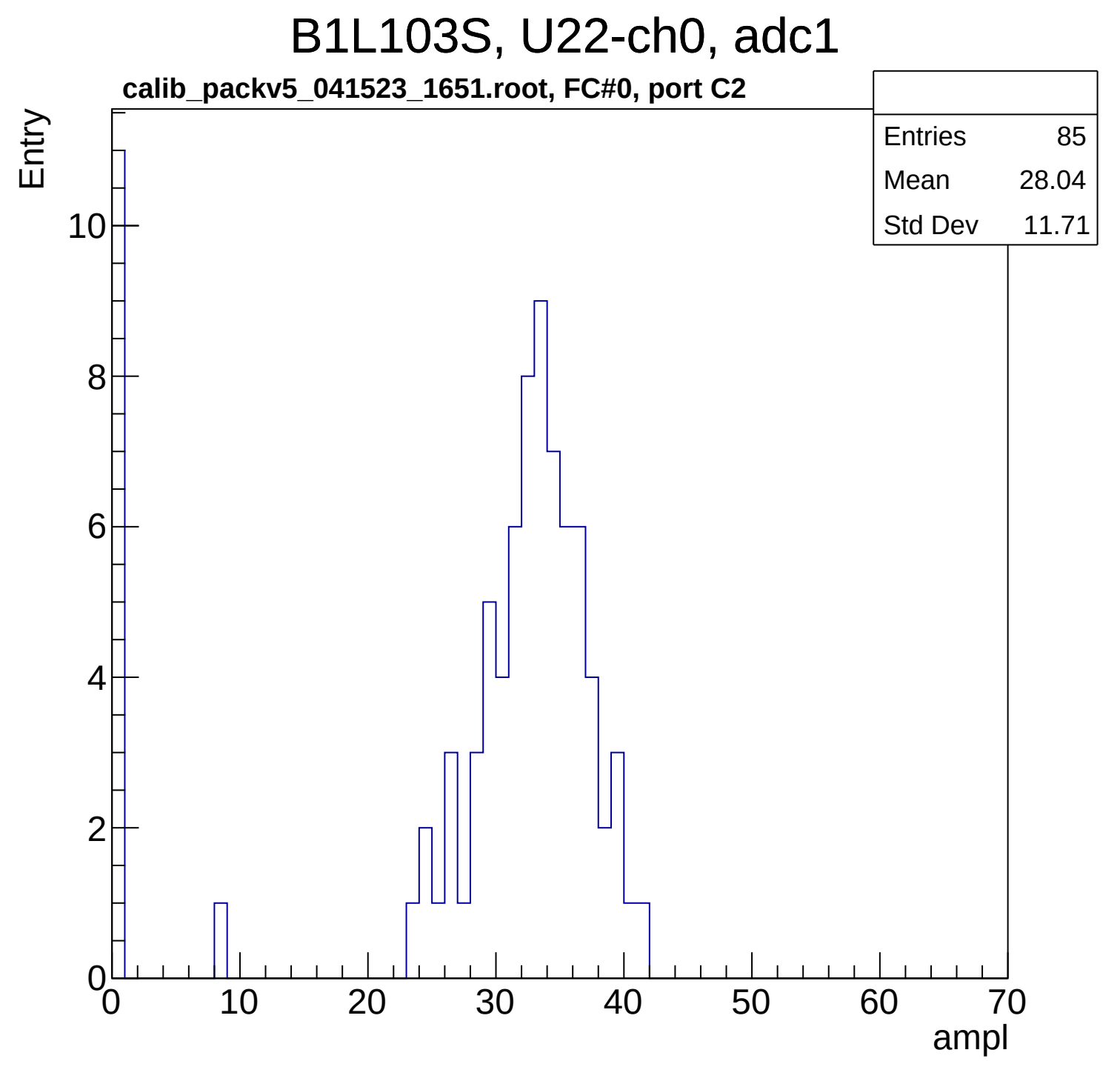
50
60
70
ampl


B1L103S, U22-ch0, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 28.04
Std Dev 11.71
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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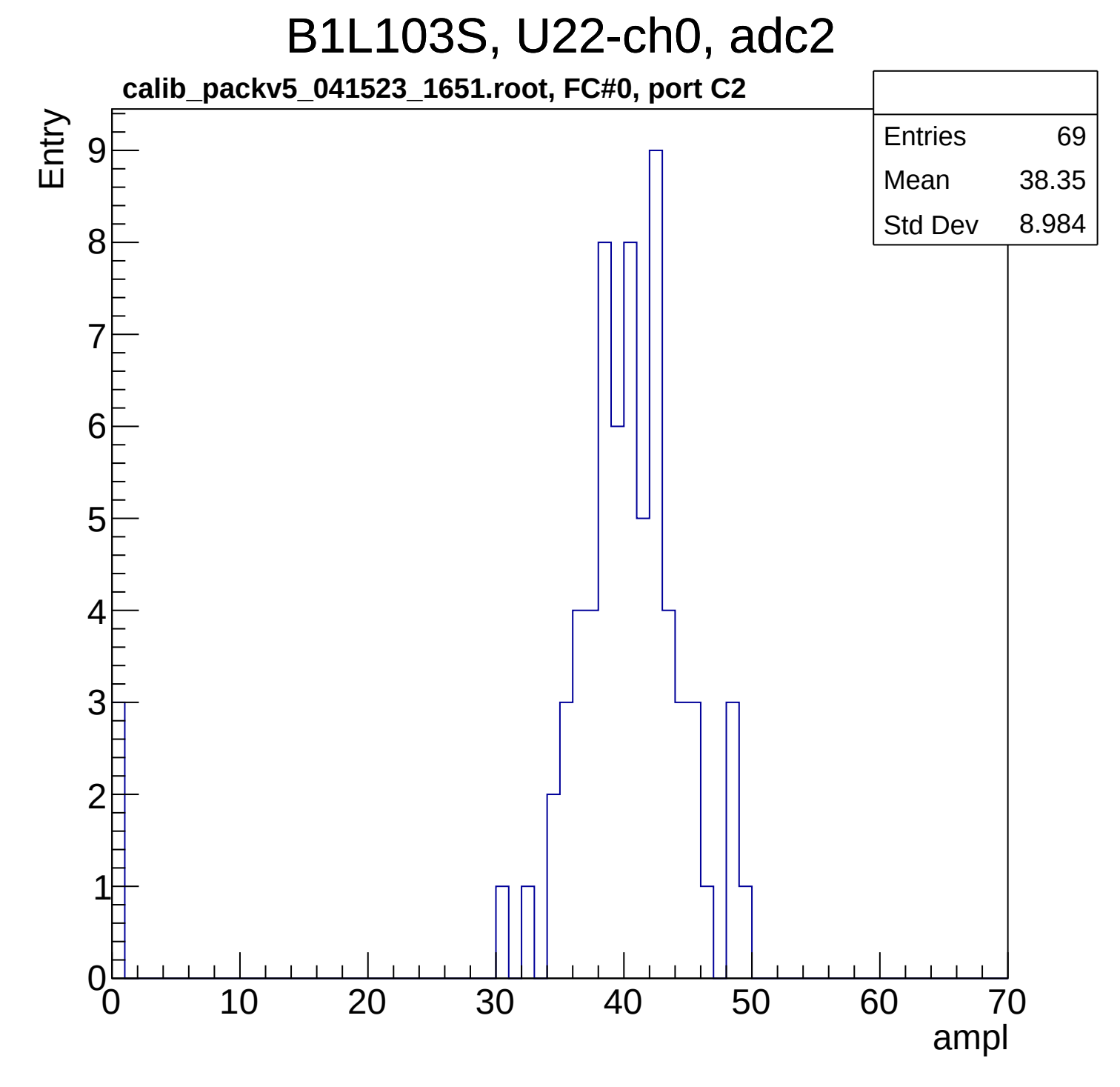
B1L103S, U22-ch0, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 38.35
Std Dev 8.984
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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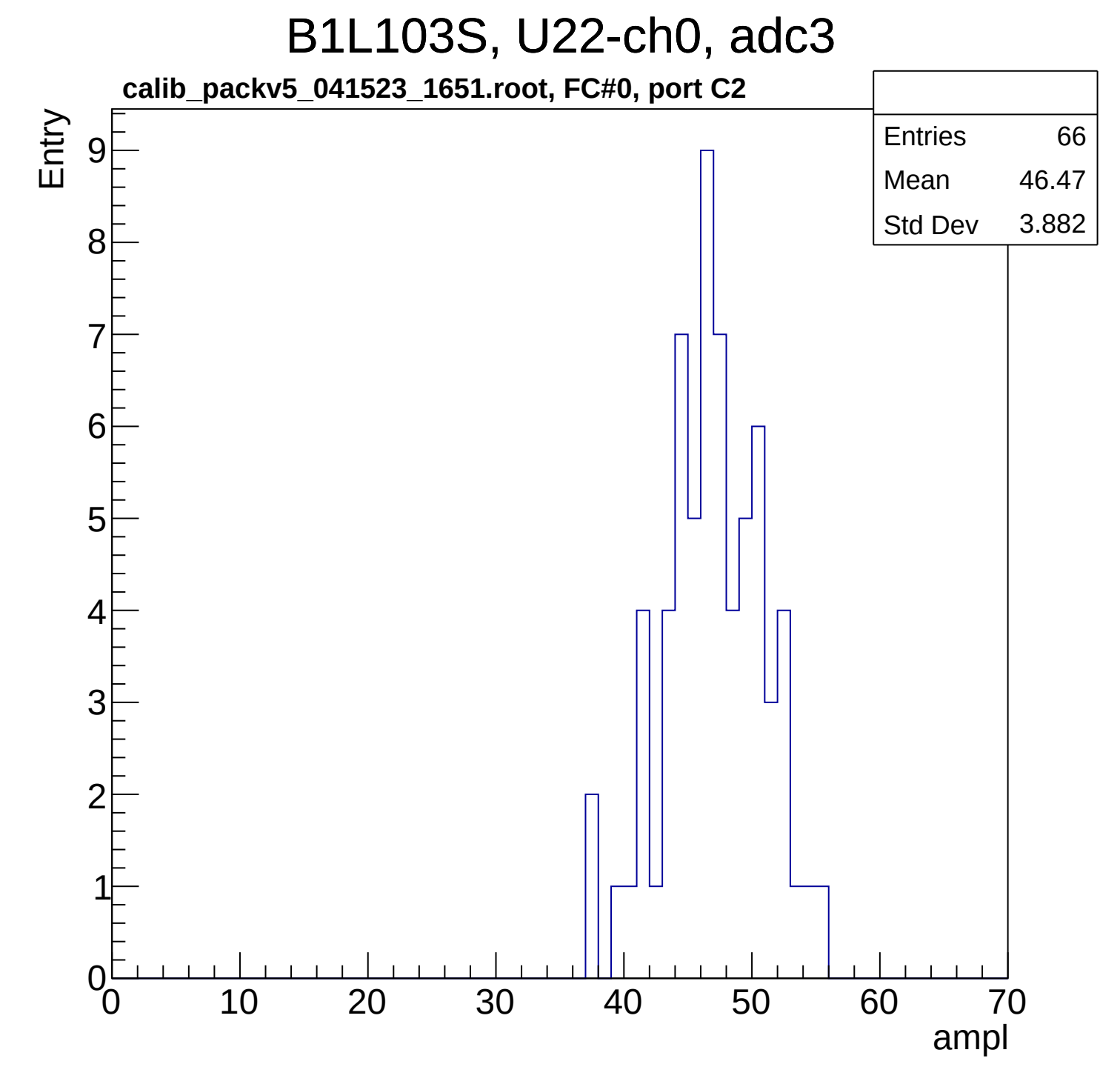
B1L103S, U22-ch0, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 46.47
Std Dev 3.882
Entry
ampl
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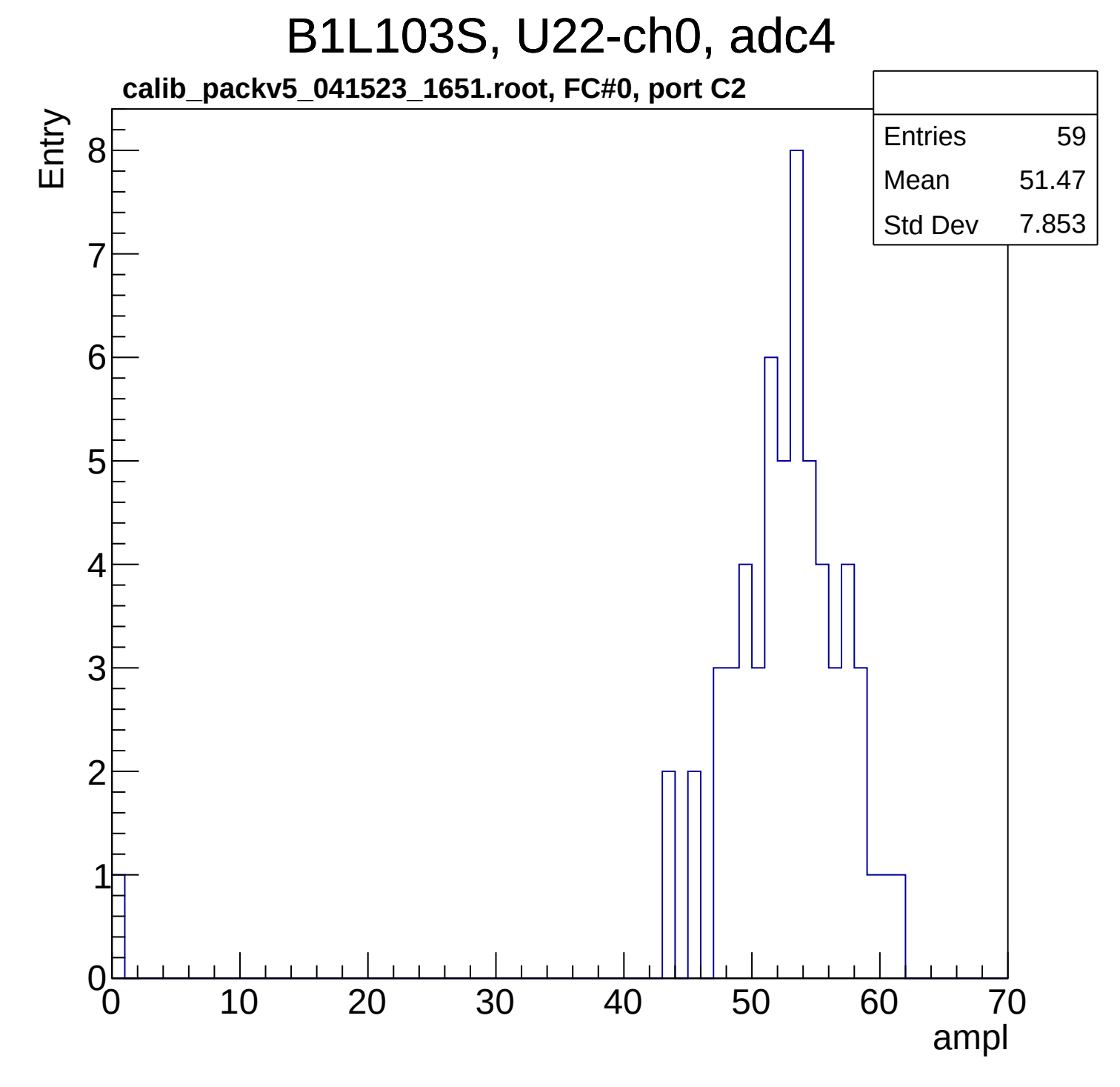
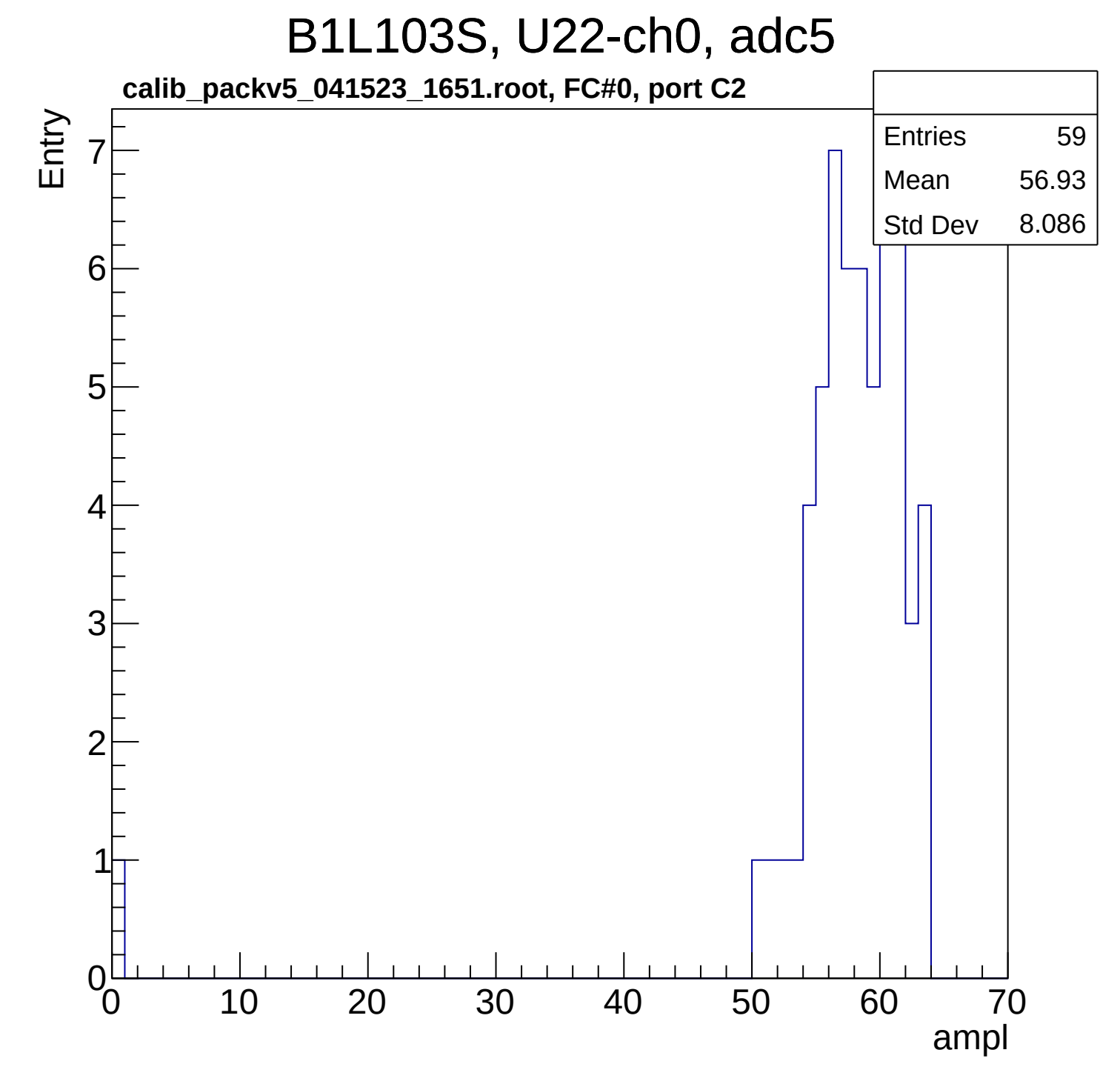
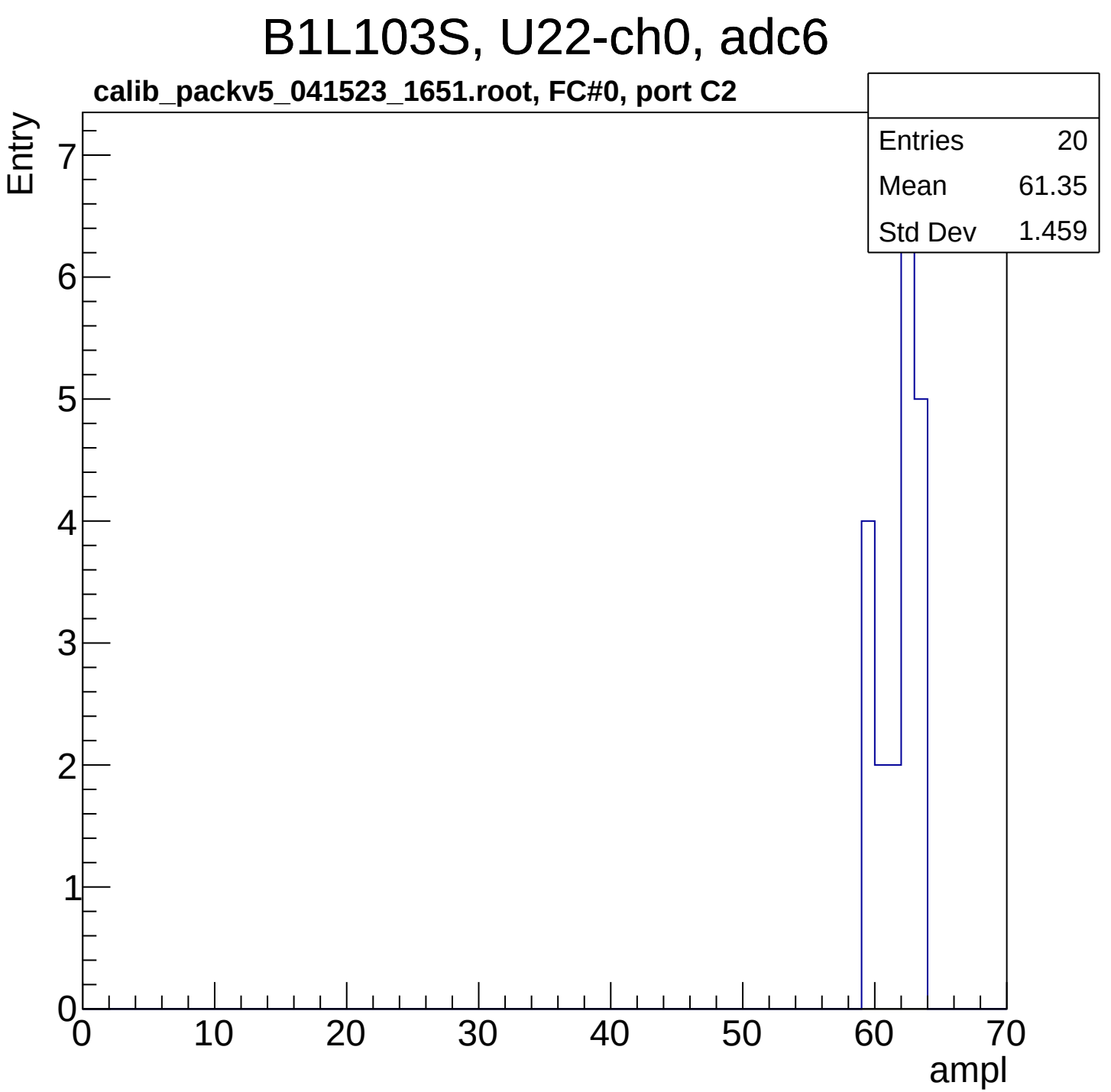
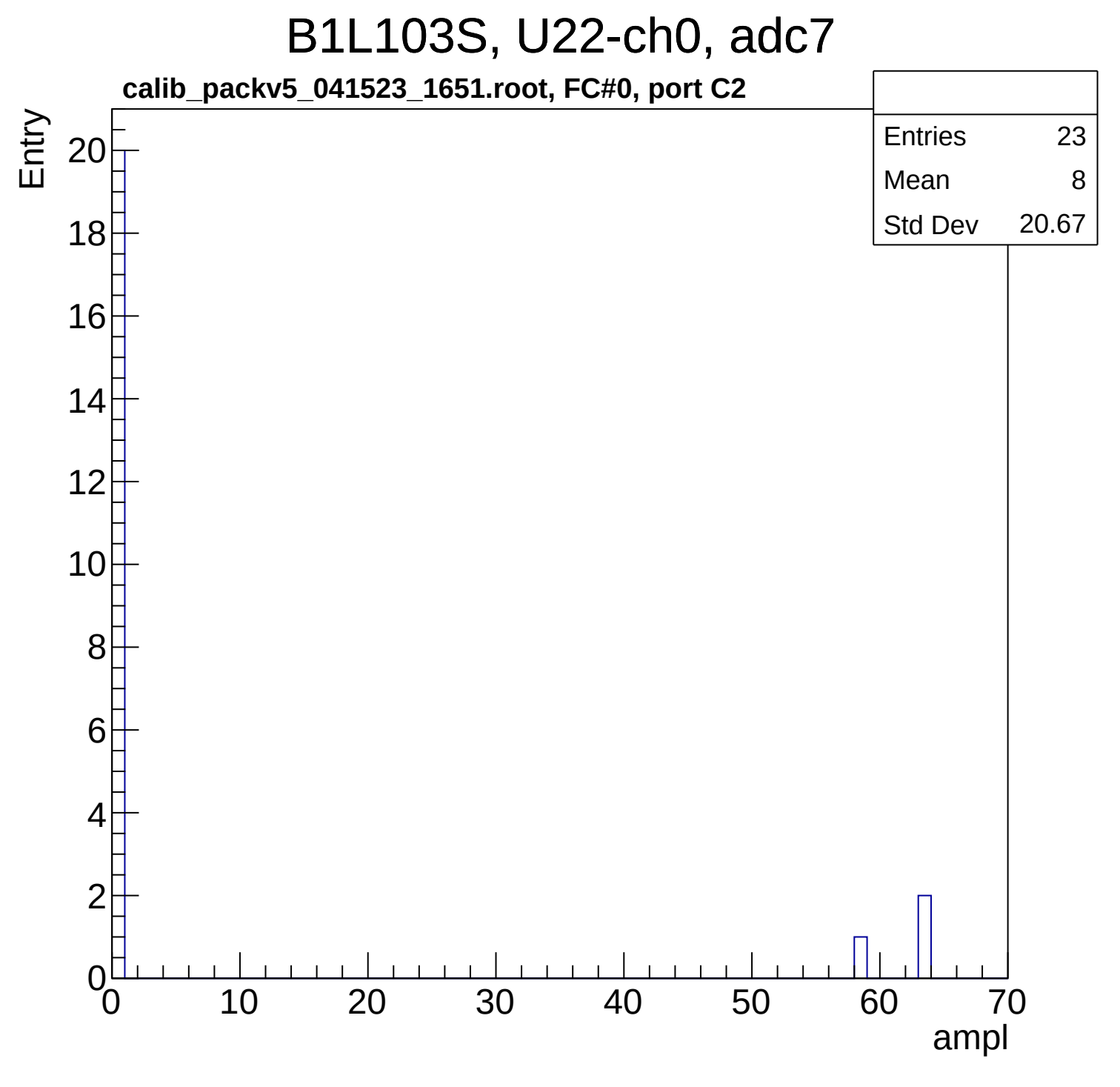
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch0, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 51.47
Std Dev 7.853
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch0, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 56.93
Std Dev 8.086
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U22-ch0, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 61.35
Std Dev 1.459
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U22-ch0, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 8
Std Dev 20.67
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
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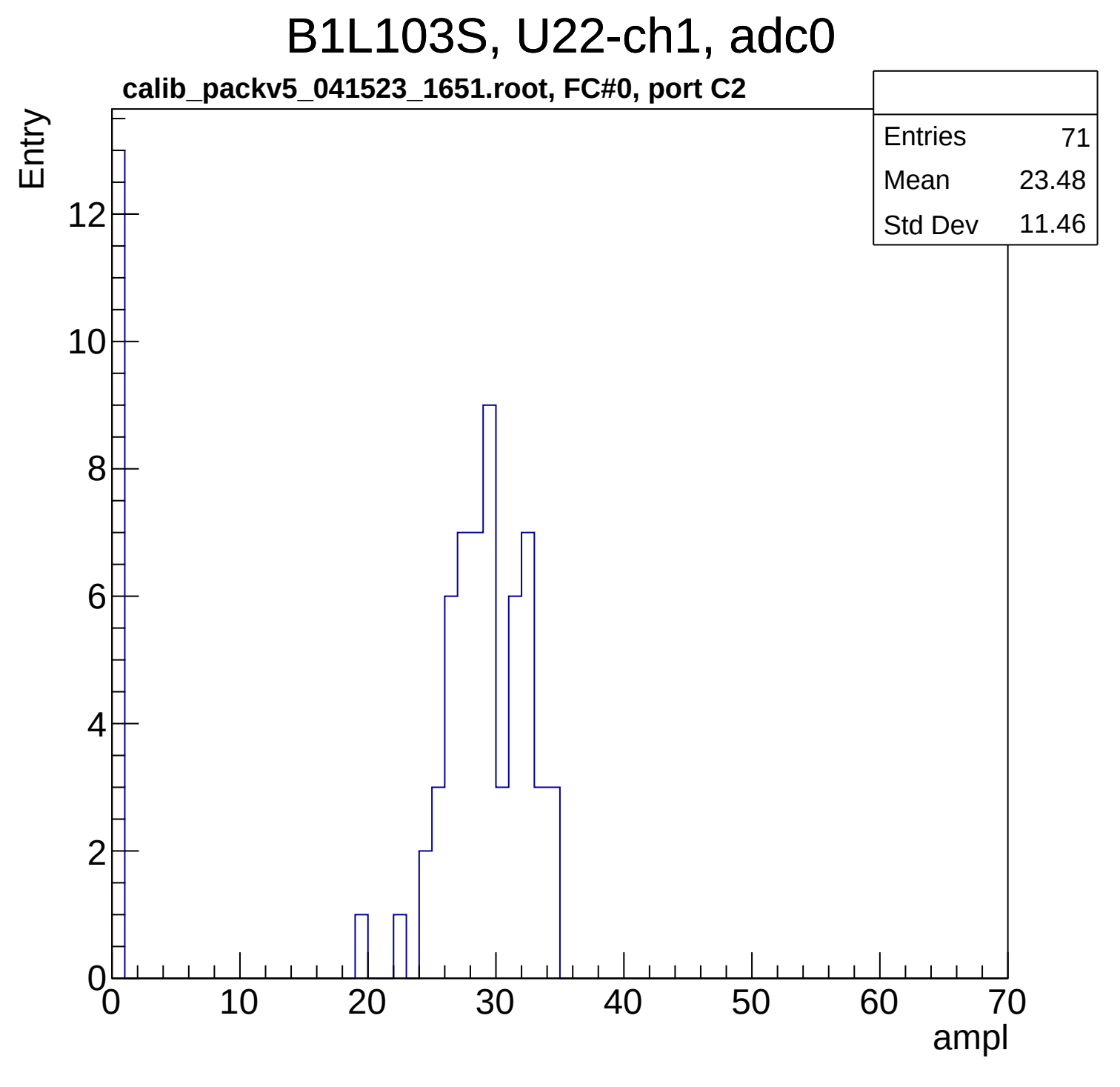
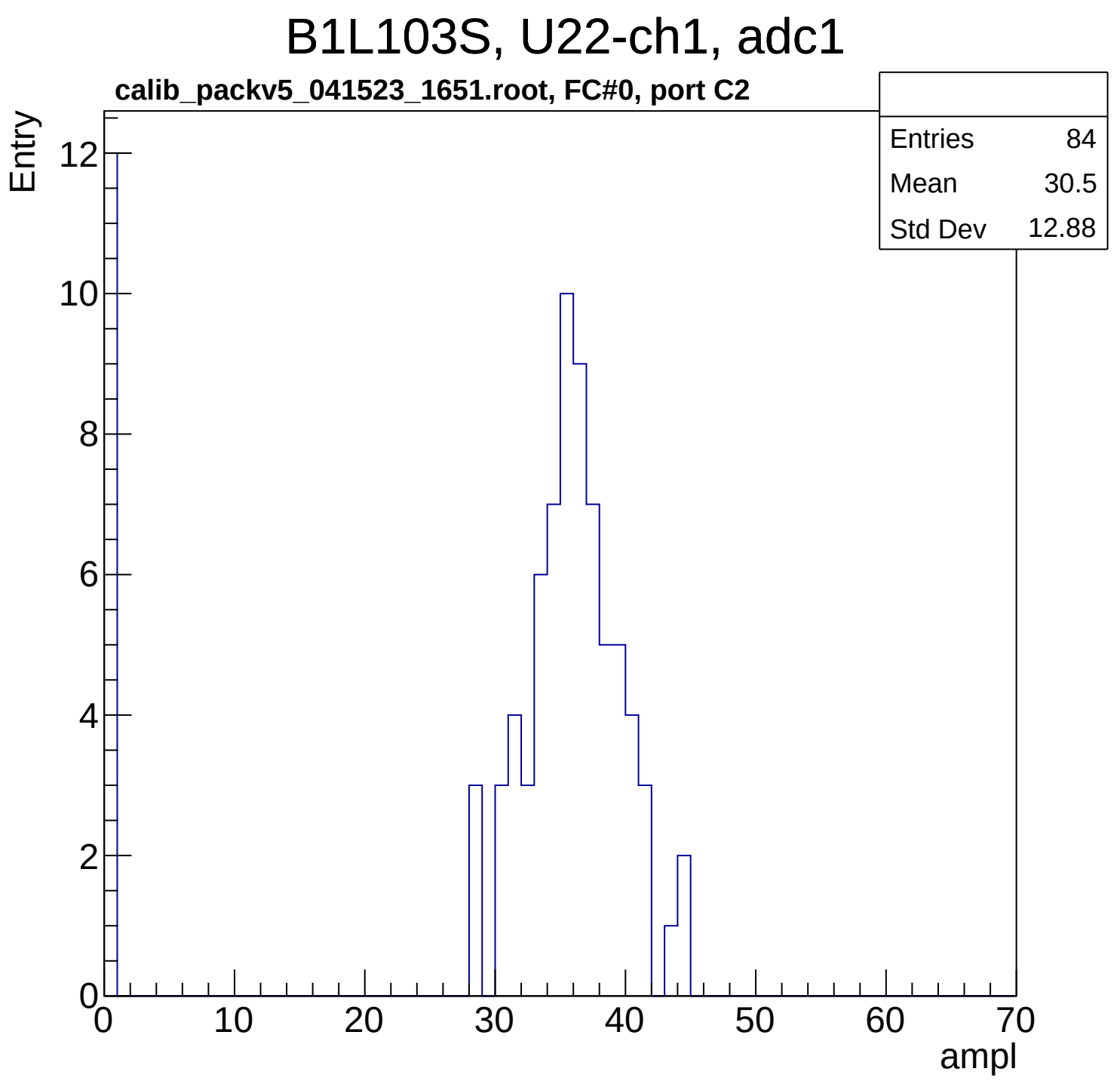
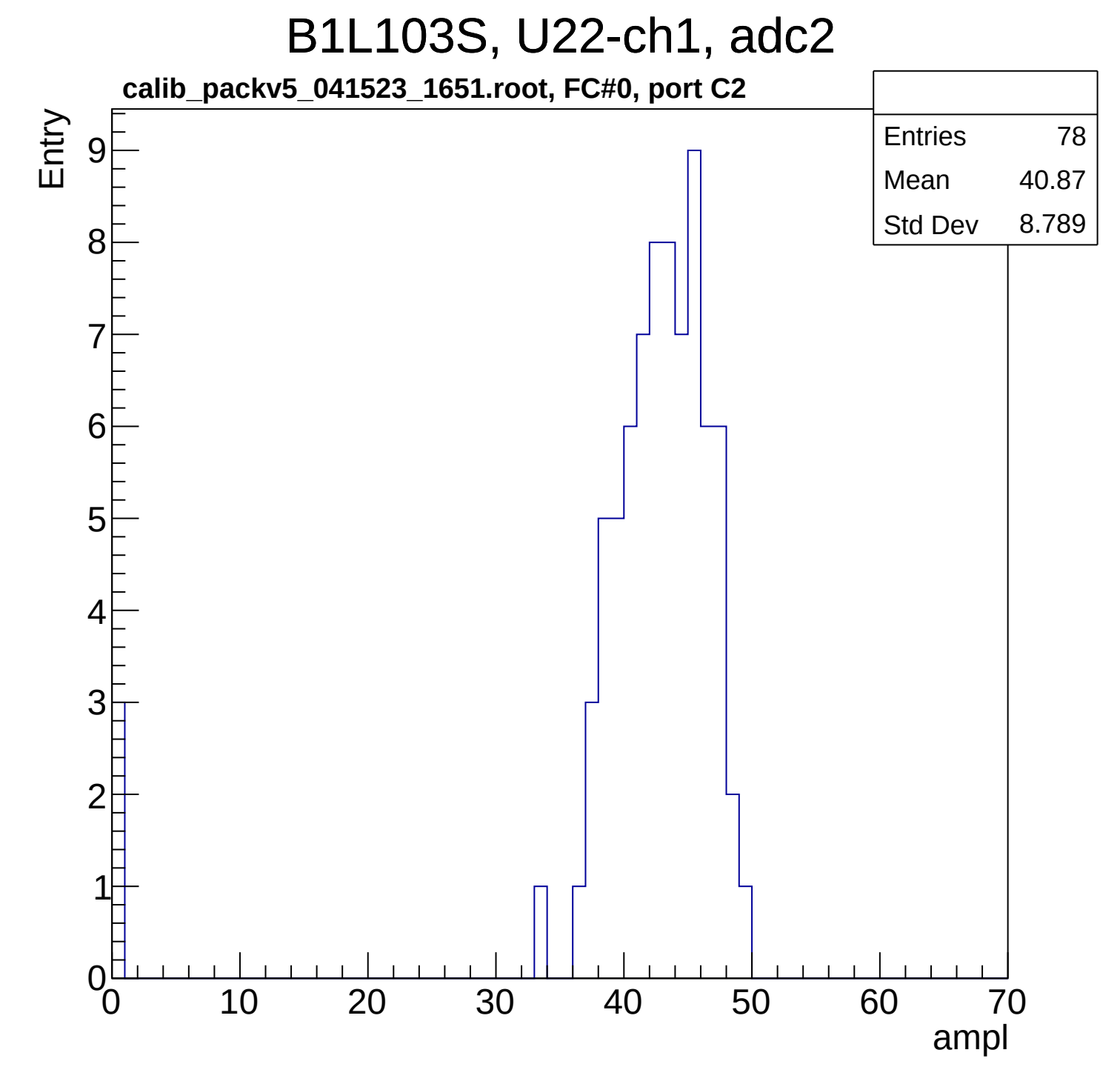
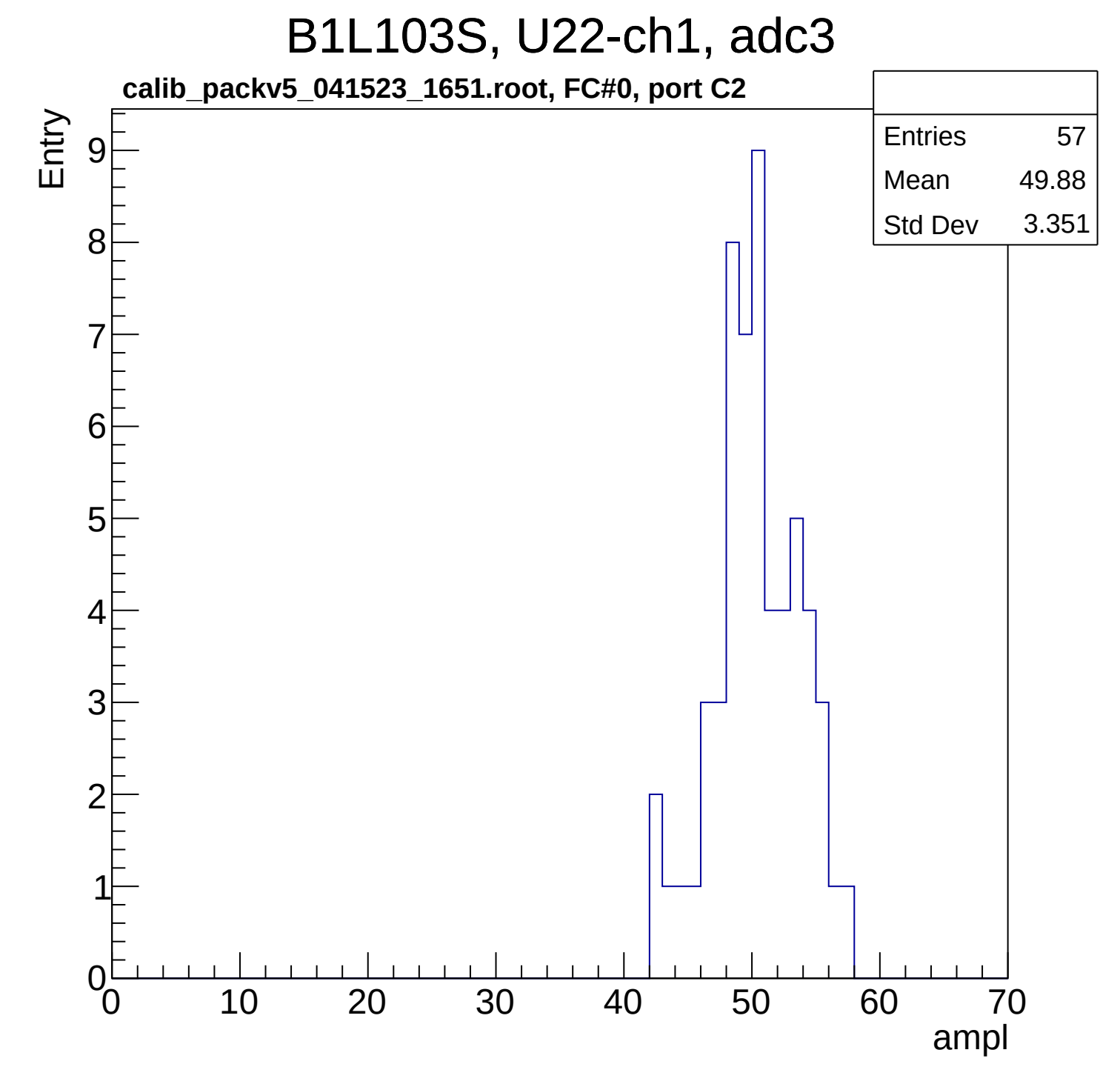

B1L103S, U22-ch1, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 23.48
Std Dev 11.46
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch1, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 30.5
Std Dev 12.88
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch1, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 40.87
Std Dev 8.789
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch1, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 49.88
Std Dev 3.351
Entry
ampl
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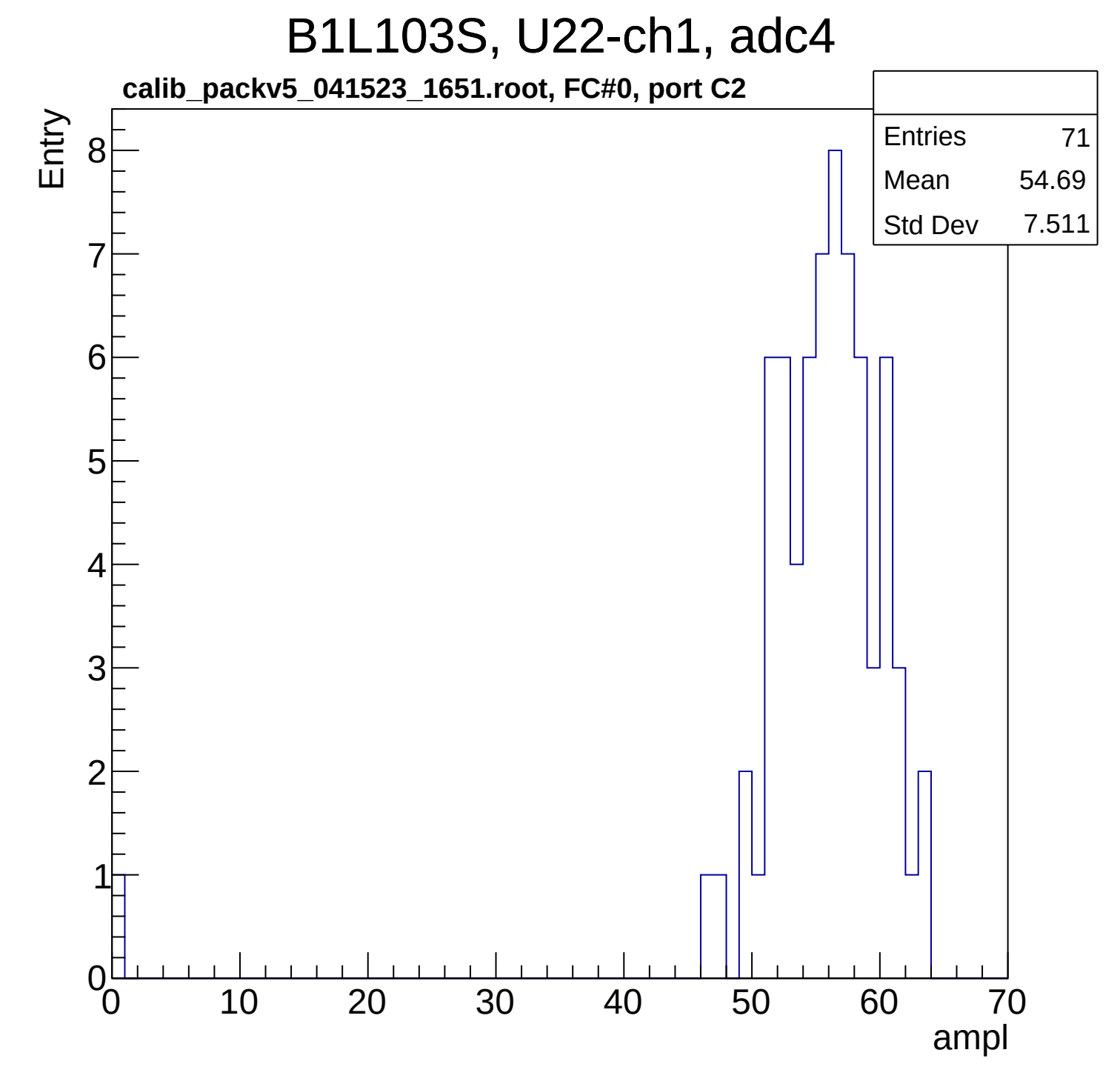
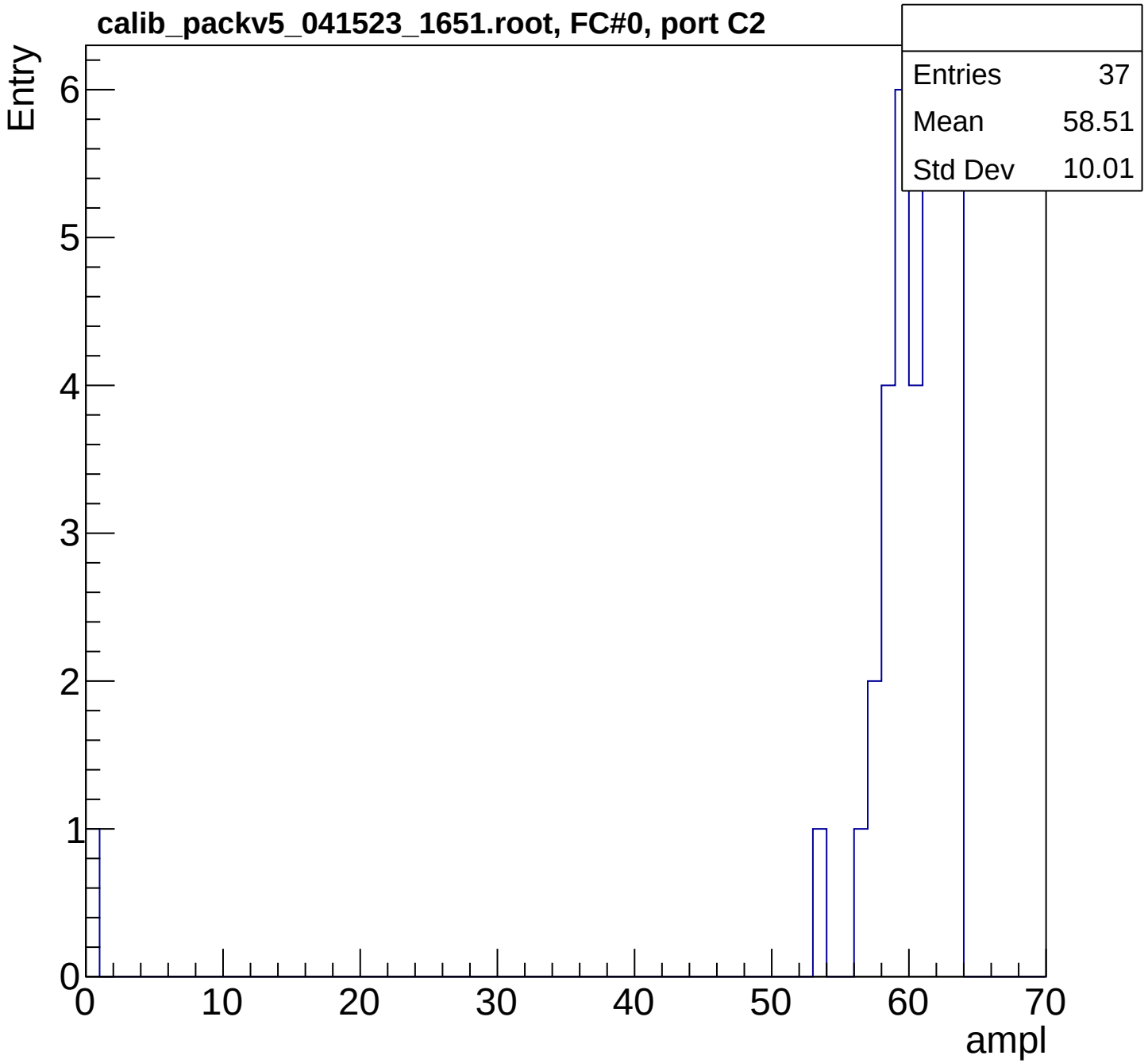
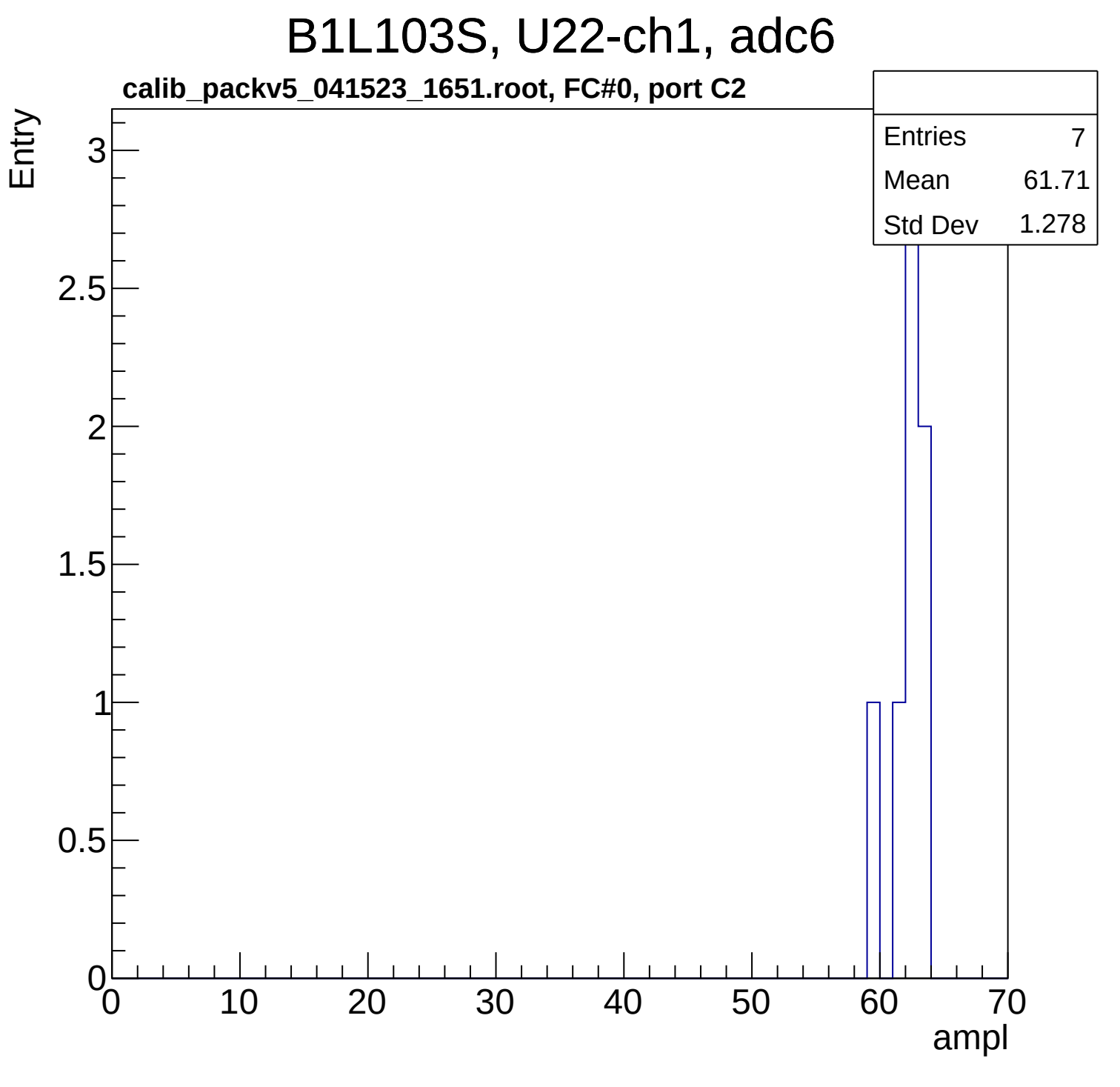
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch1, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 54.69
Std Dev 7.511
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch1, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 58.51
Std Dev 10.01
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U22-ch1, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 61.71
Std Dev 1.278
Entry
ampl
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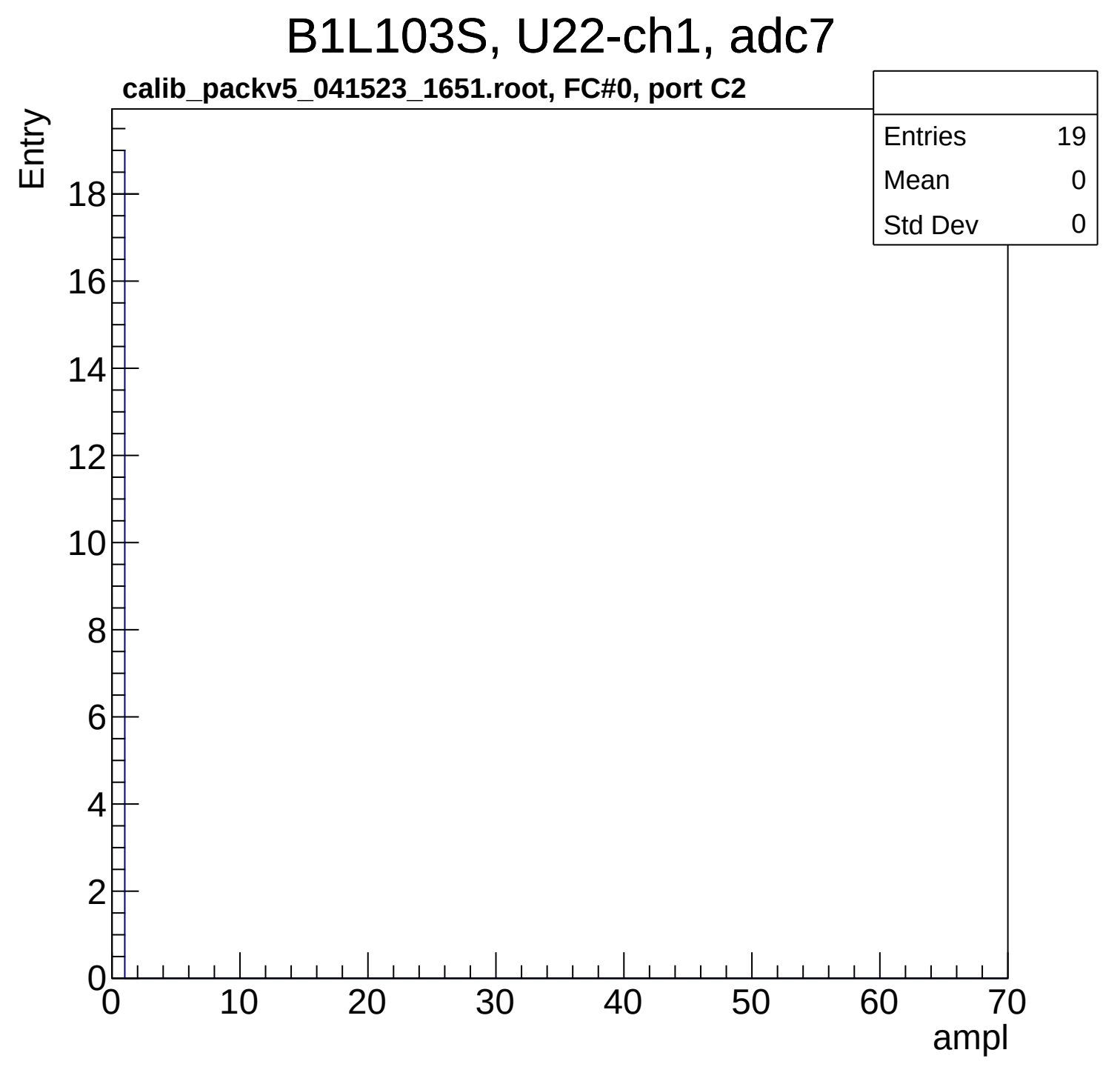
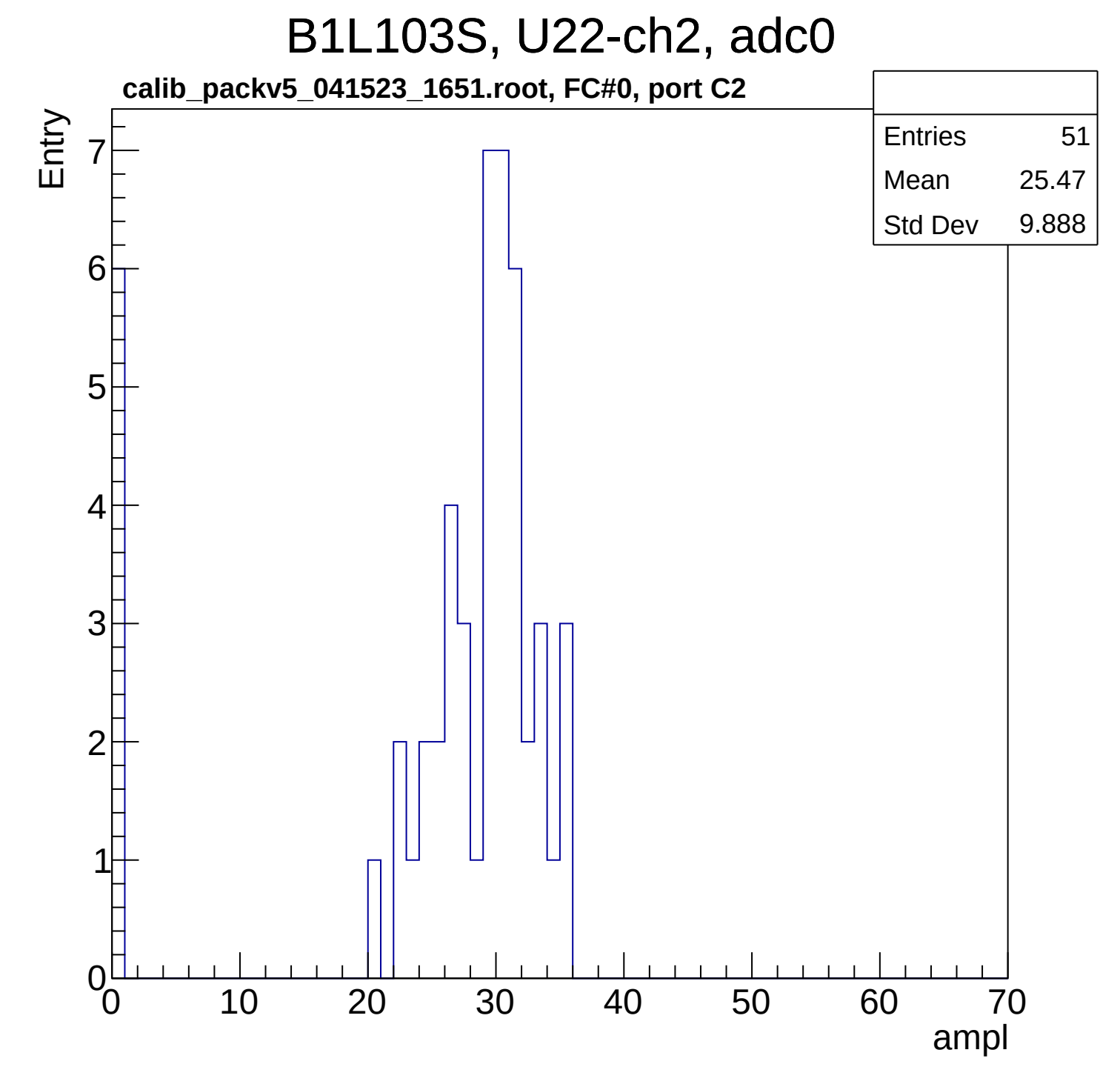
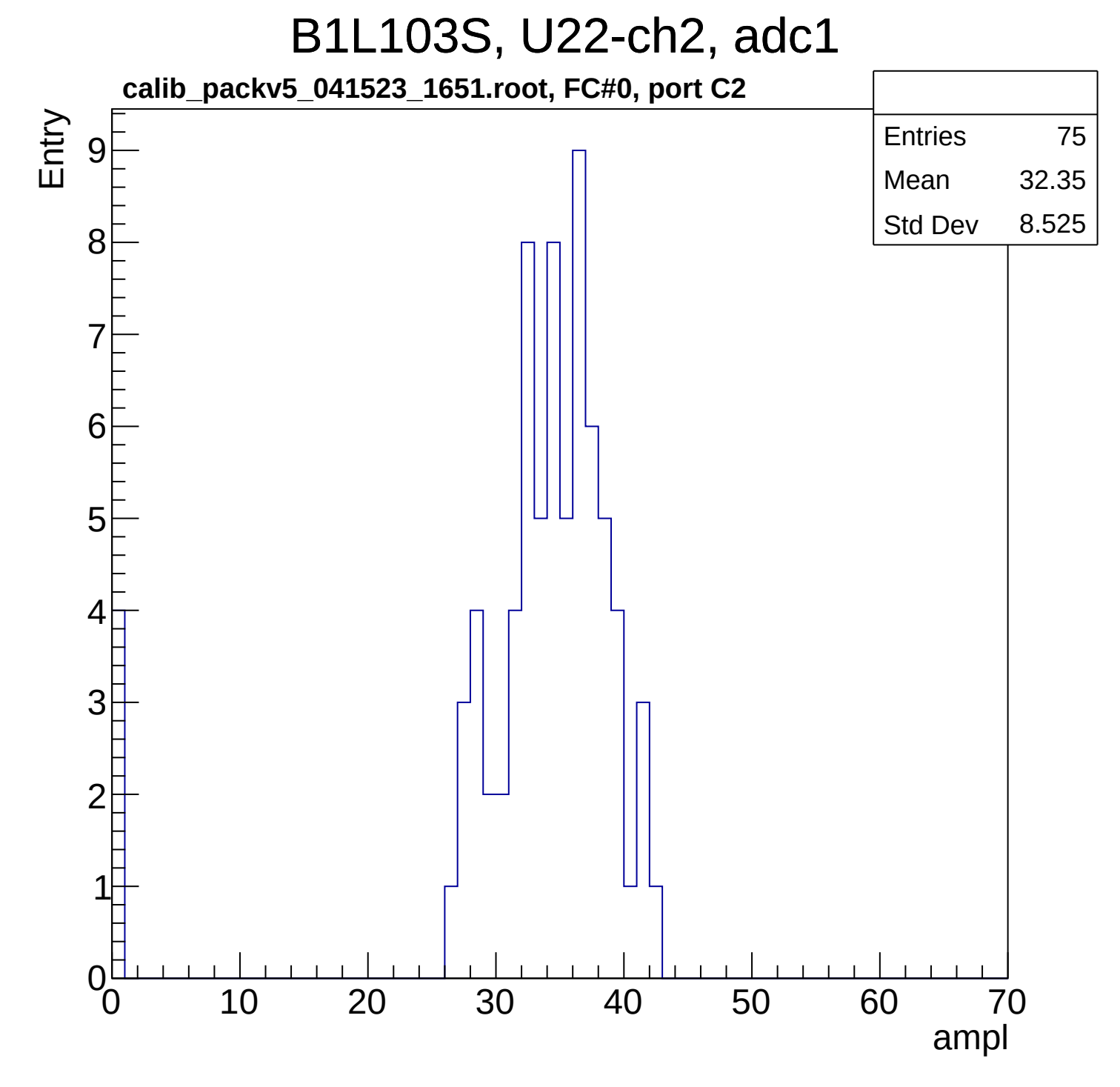
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U22-ch1, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch2, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 25.47
Std Dev 9.888
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U22-ch2, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 32.35
Std Dev 8.525
Entry
ampl
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2
3
4
5
6
7
8
9
0
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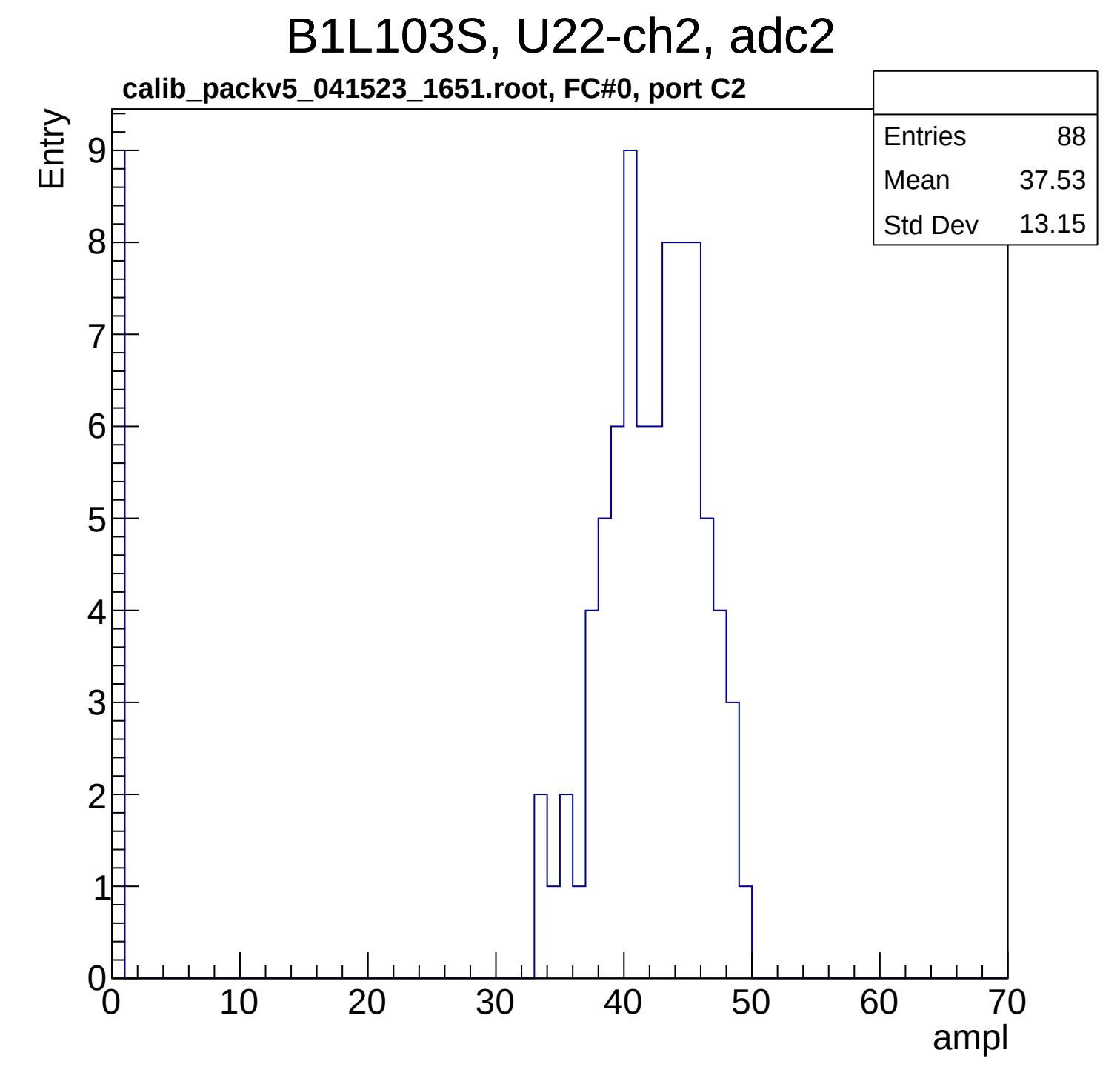
20
30
40
50
60
70


B1L103S, U22-ch2, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 37.53
Std Dev 13.15
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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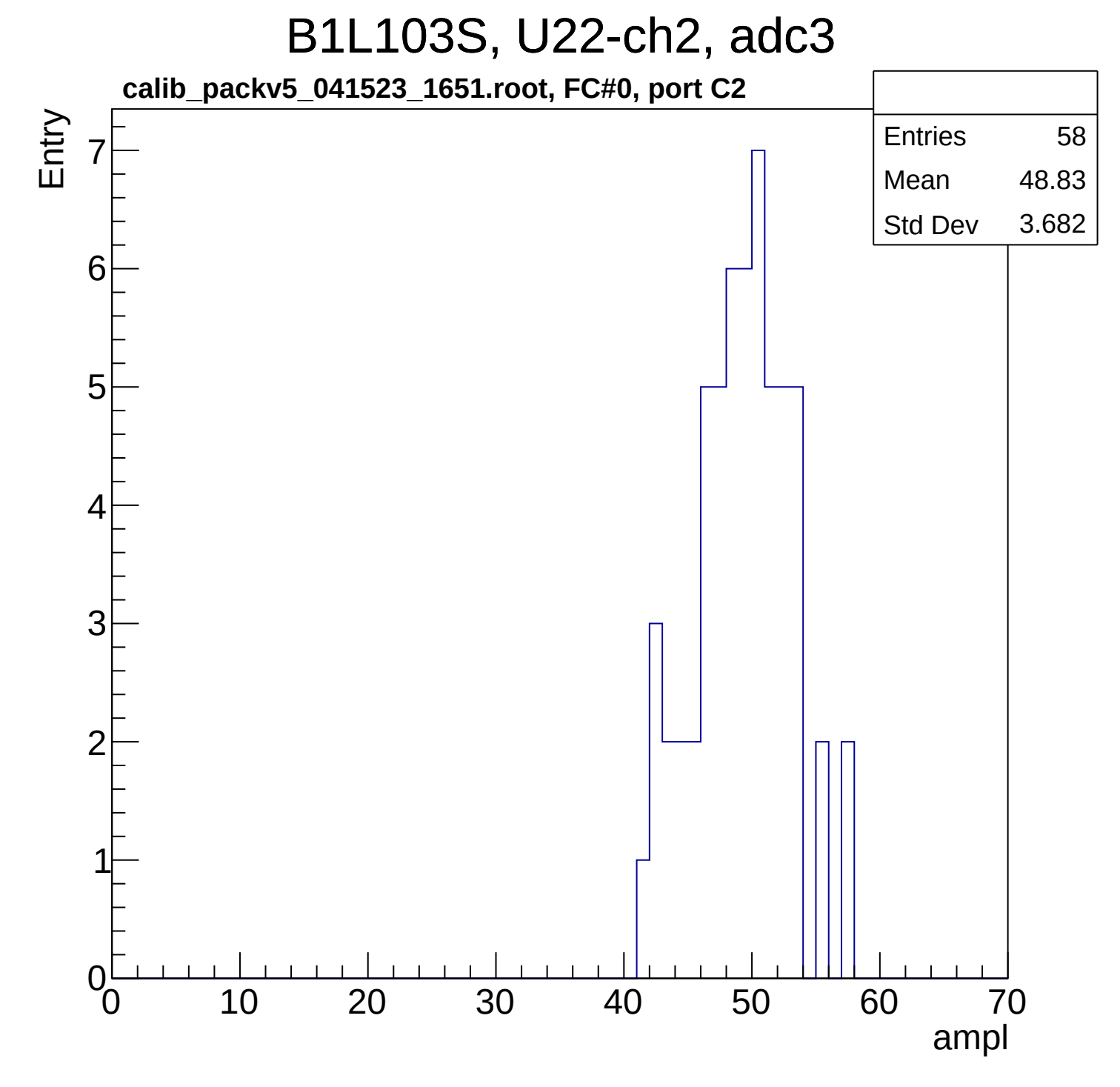
20
30
40
50
60
70


B1L103S, U22-ch2, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 48.83
Std Dev 3.682
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
30
40
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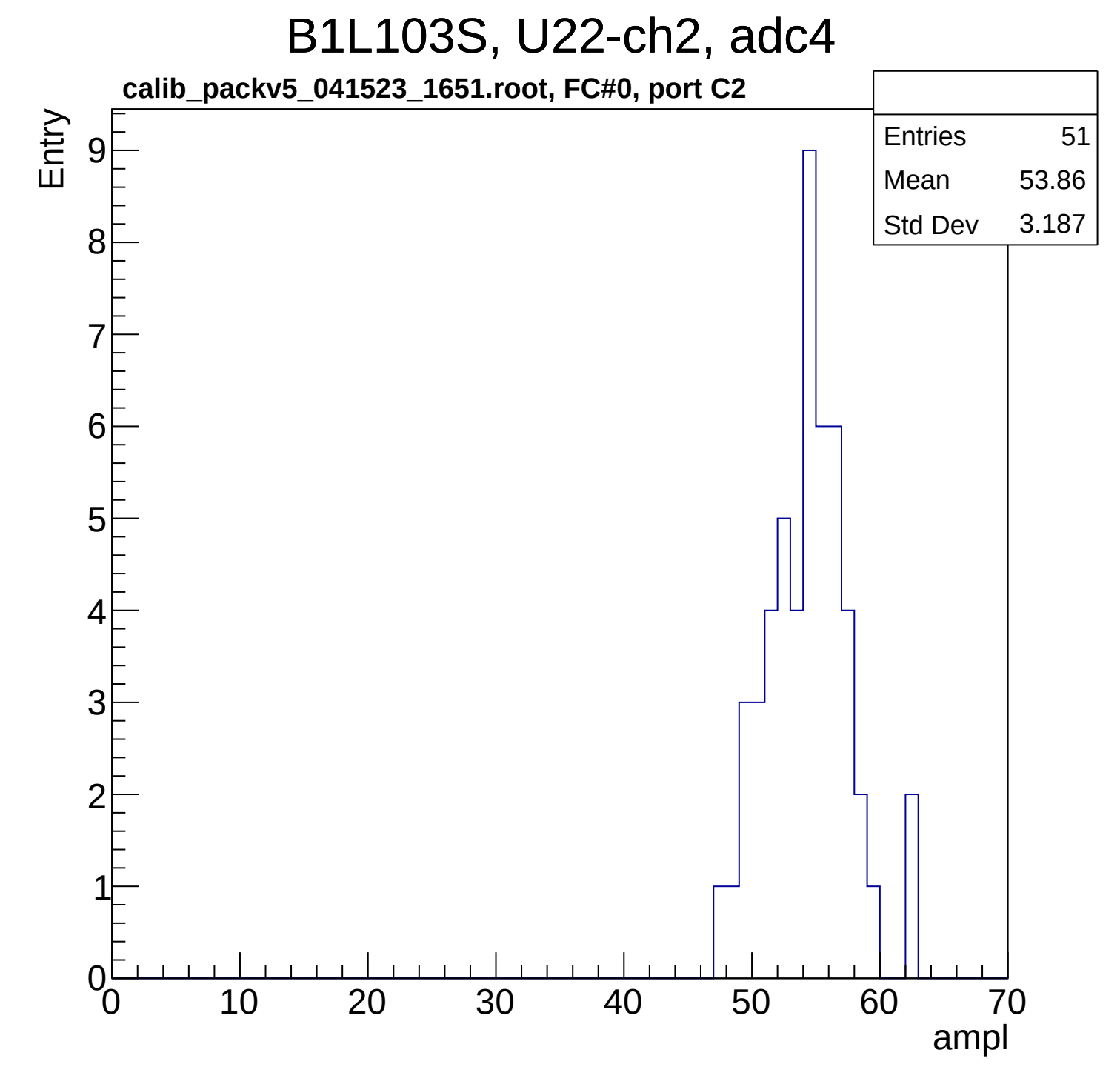
60
70


B1L103S, U22-ch2, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 53.86
Std Dev 3.187
Entry
ampl
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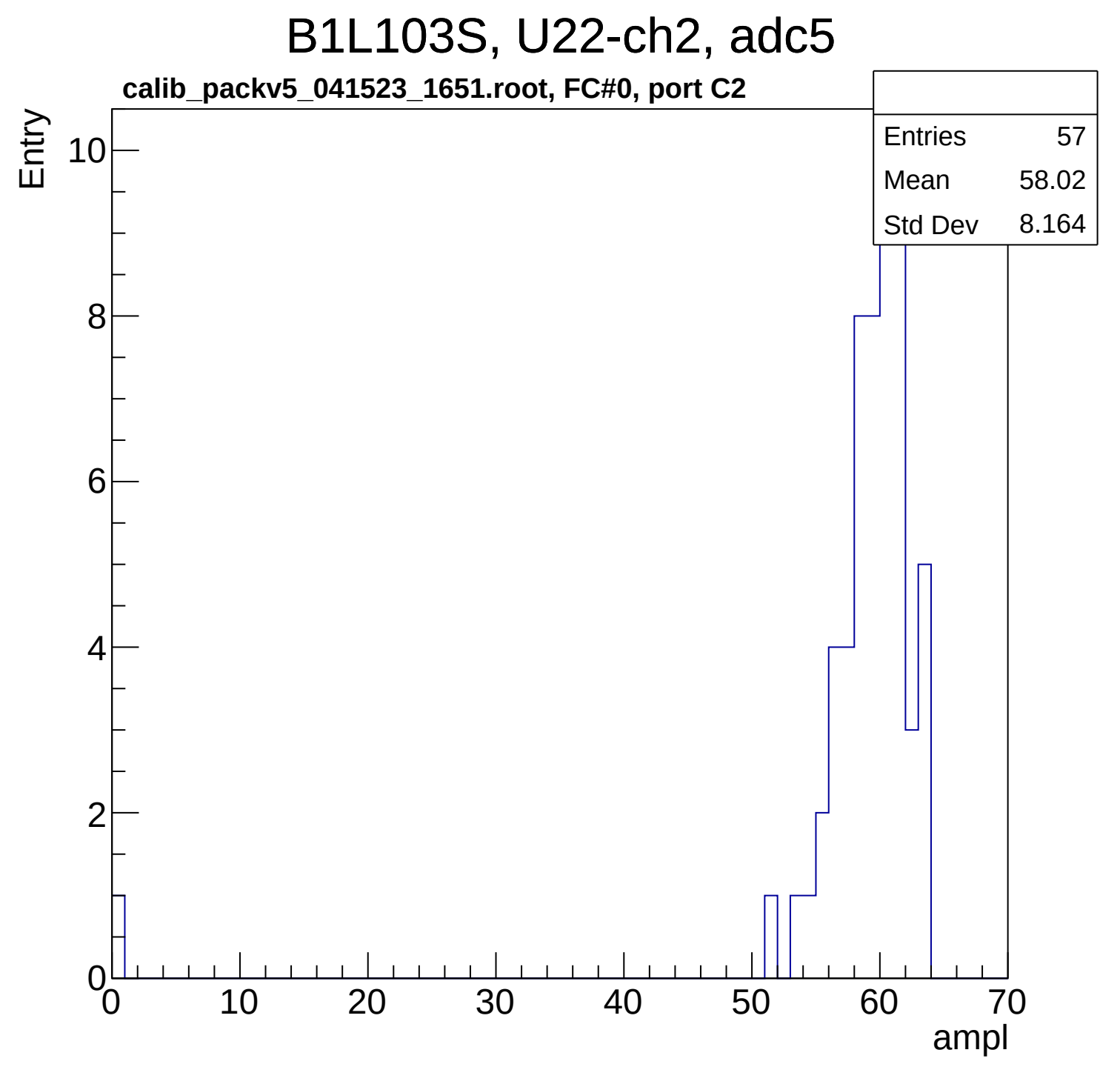
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch2, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 58.02
Std Dev 8.164
Entry
0
2
4
6
8
10
0
10
20
30
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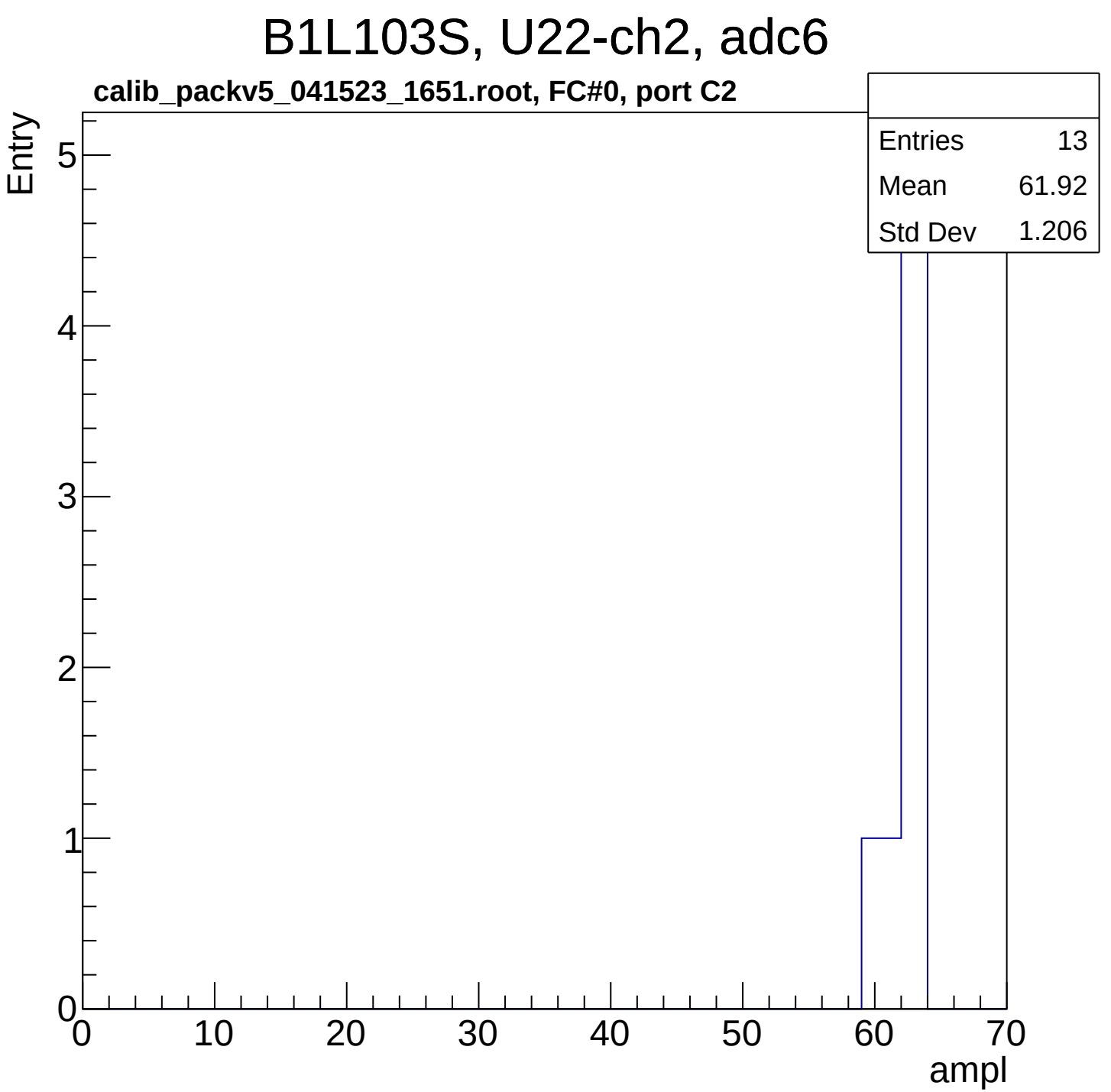
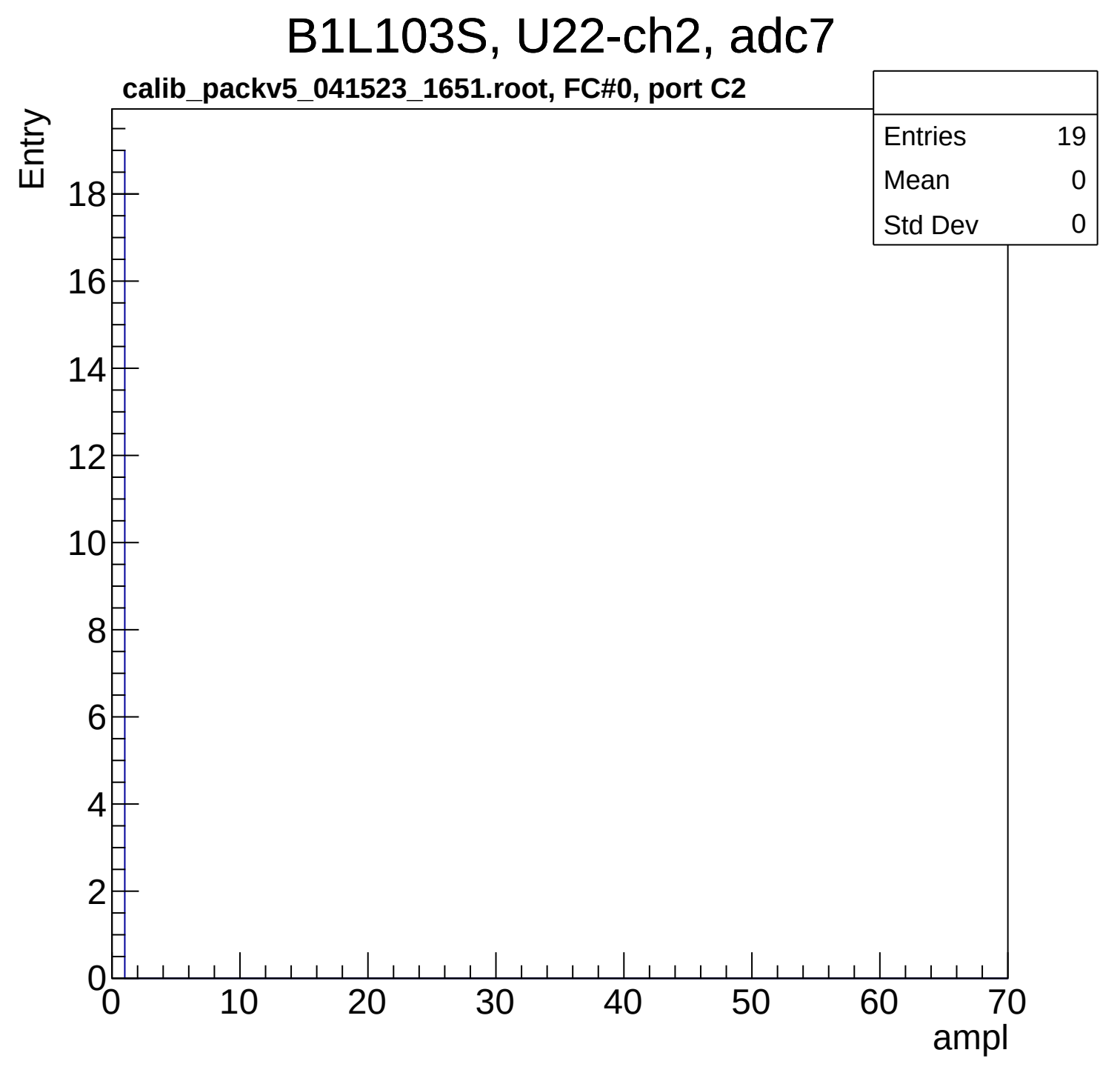
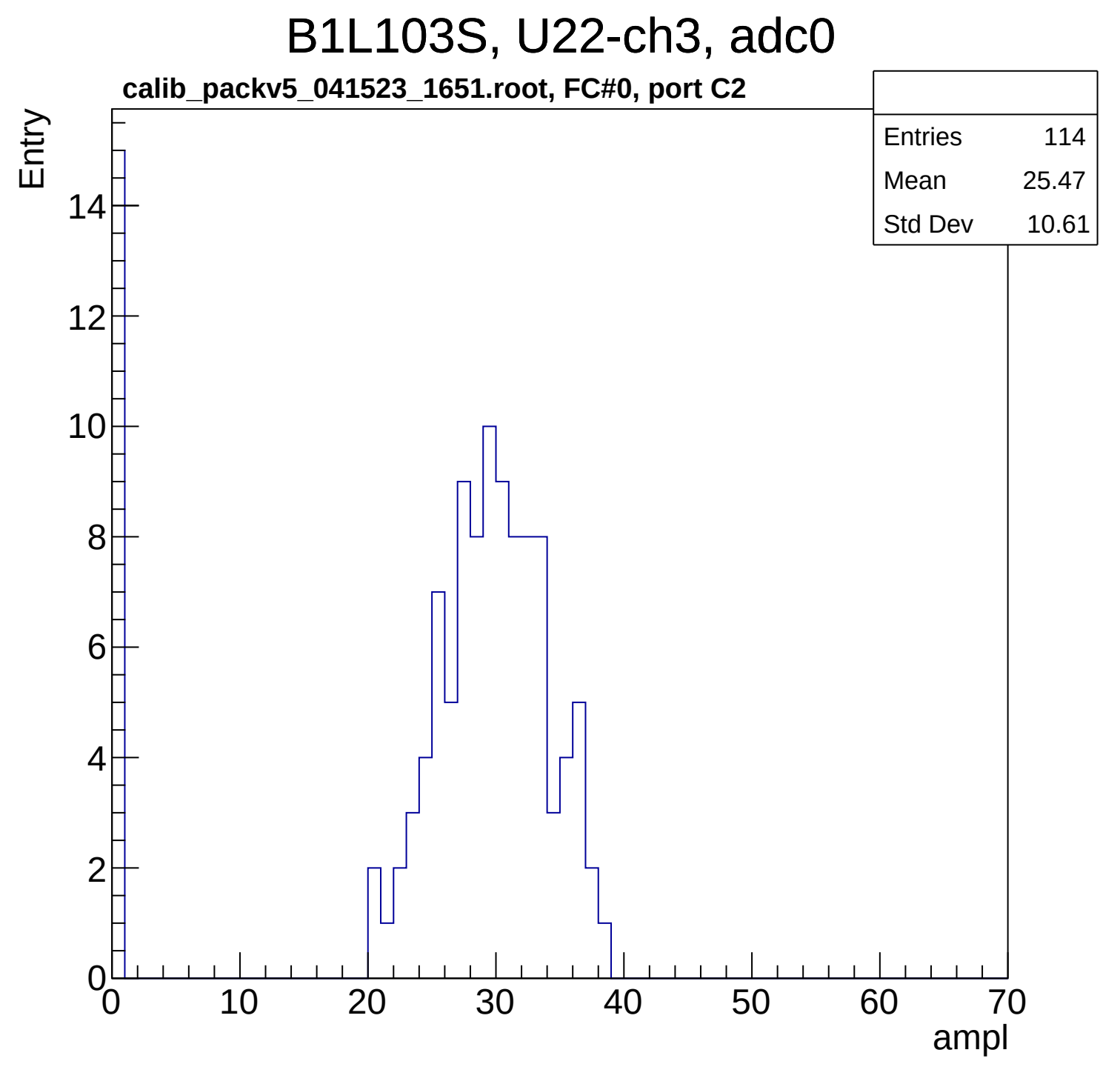
50
60
70
ampl


B1L103S, U22-ch2, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 61.92
Std Dev 1.206
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch2, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch3, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 114
Mean 25.47
Std Dev 10.61
Entry
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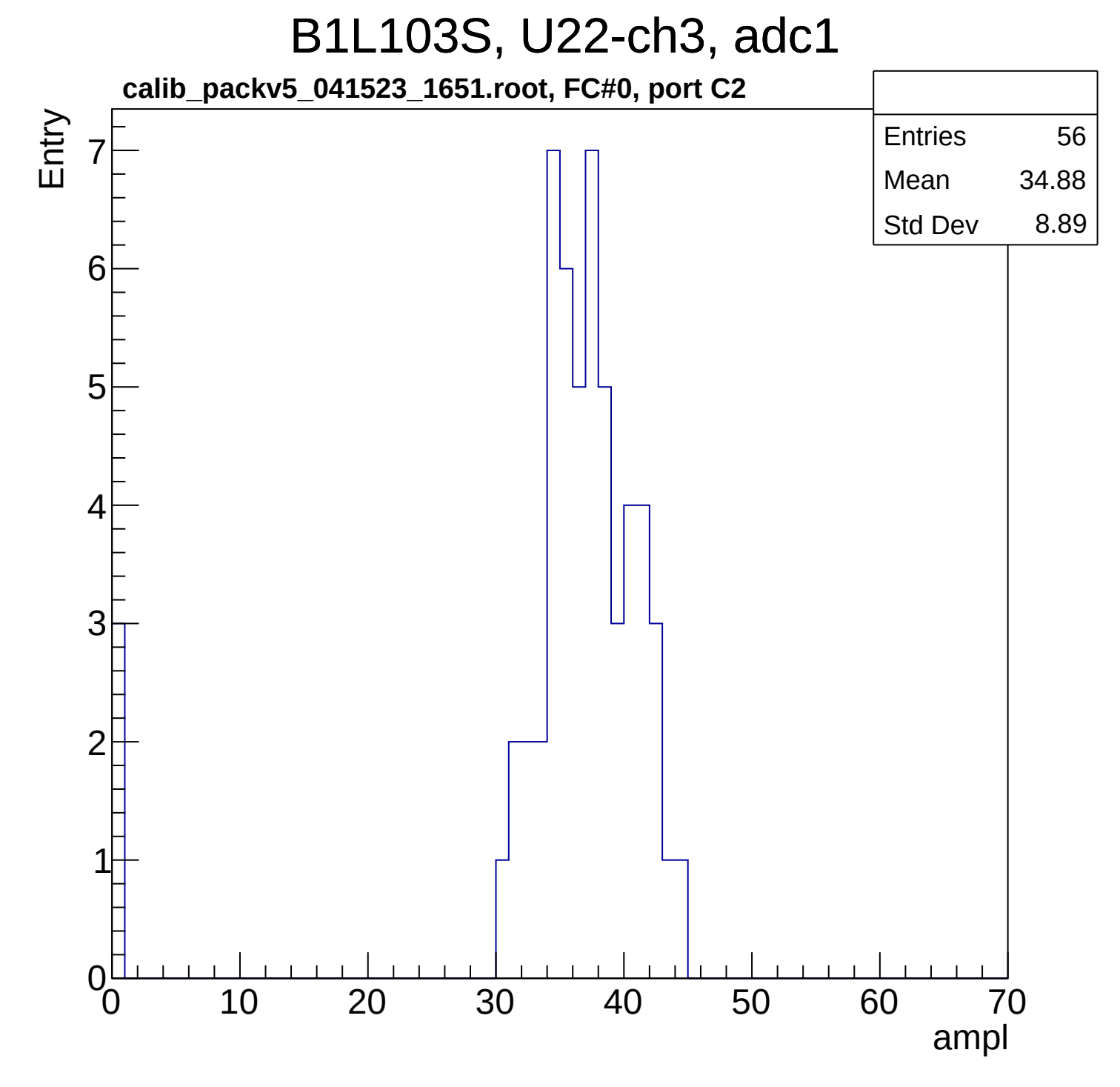
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch3, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 34.88
Std Dev 8.89
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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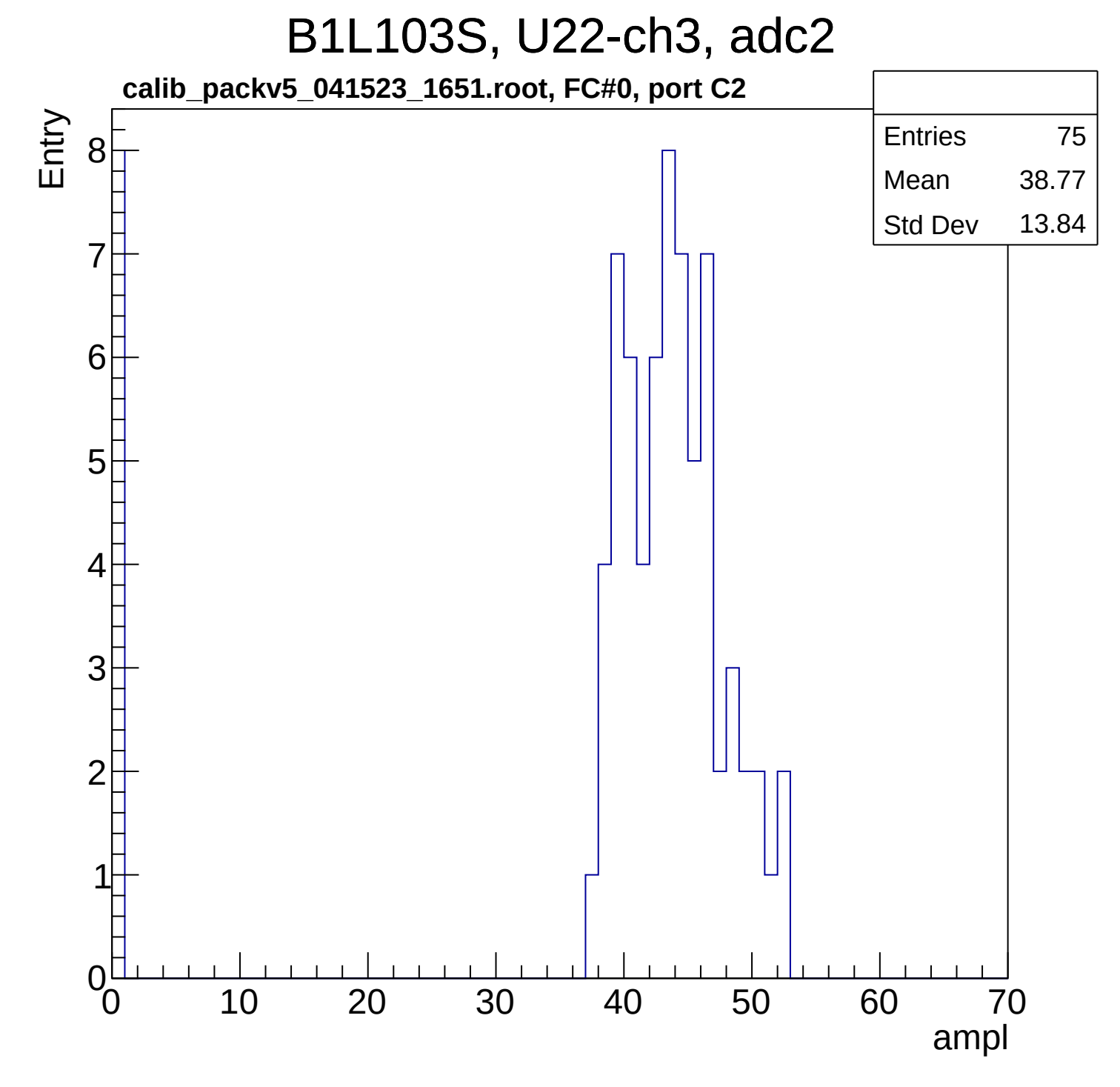
B1L103S, U22-ch3, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 38.77
Std Dev 13.84
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
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30
40
50
60
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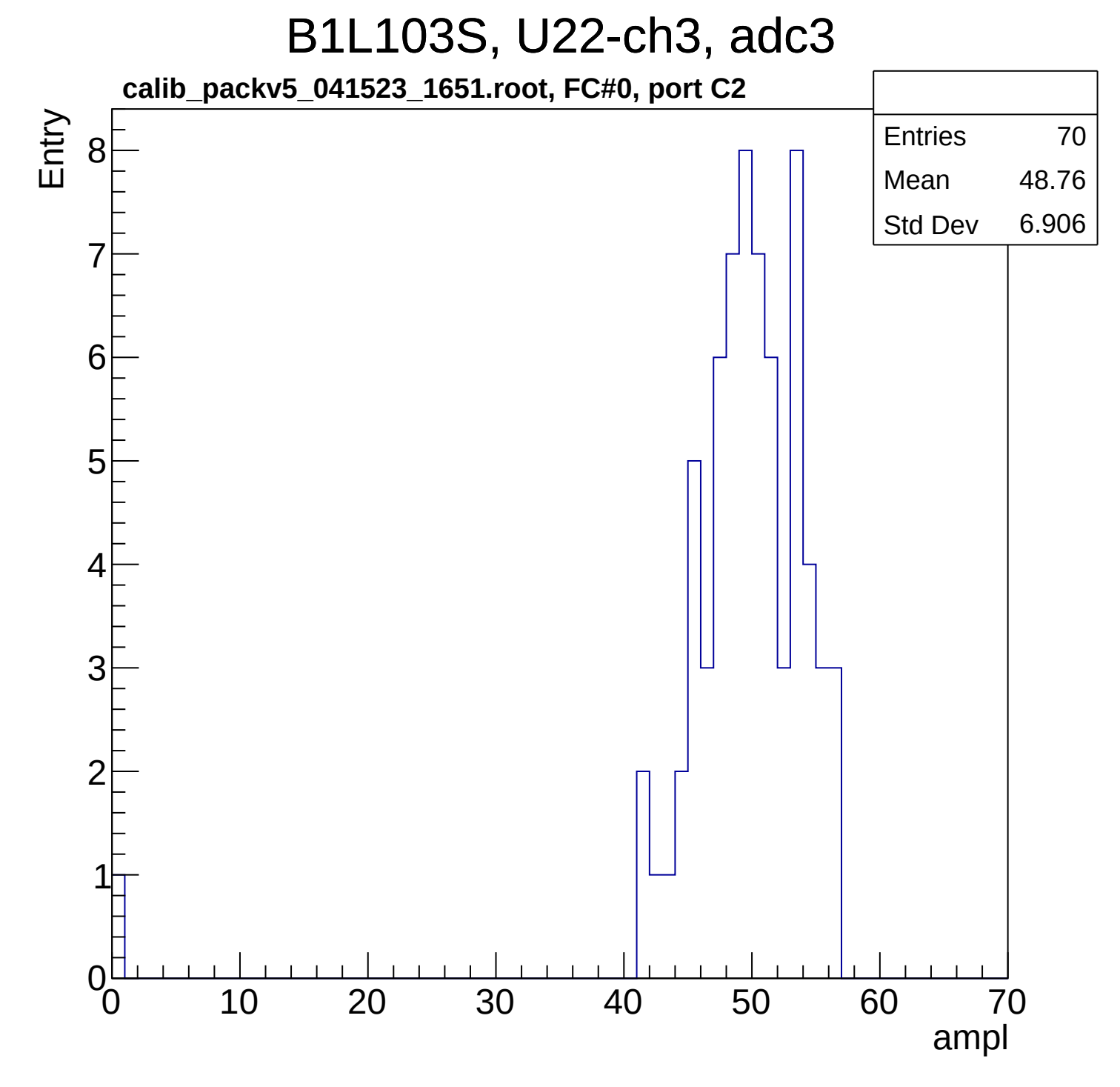
B1L103S, U22-ch3, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 48.76
Std Dev 6.906
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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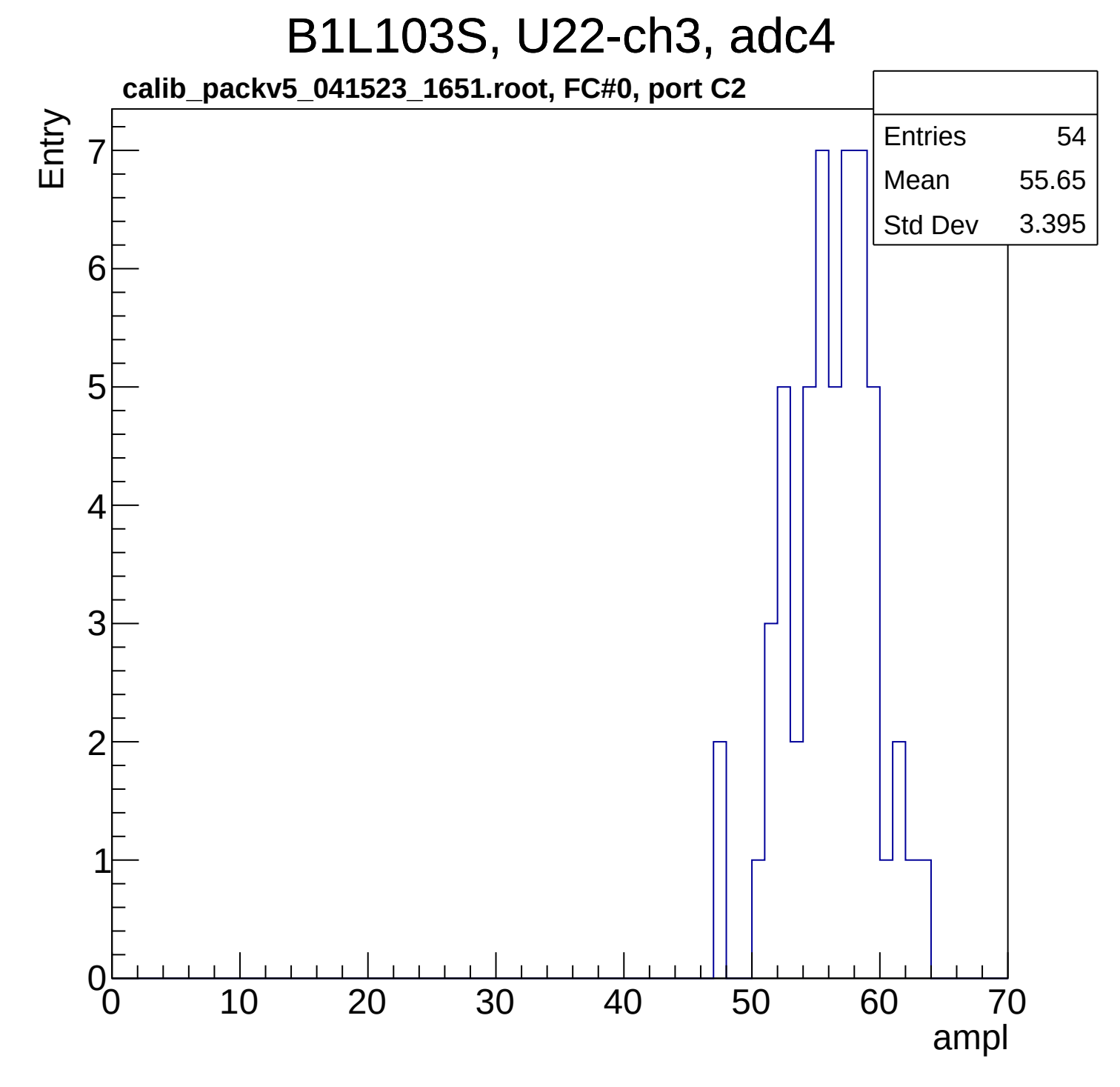
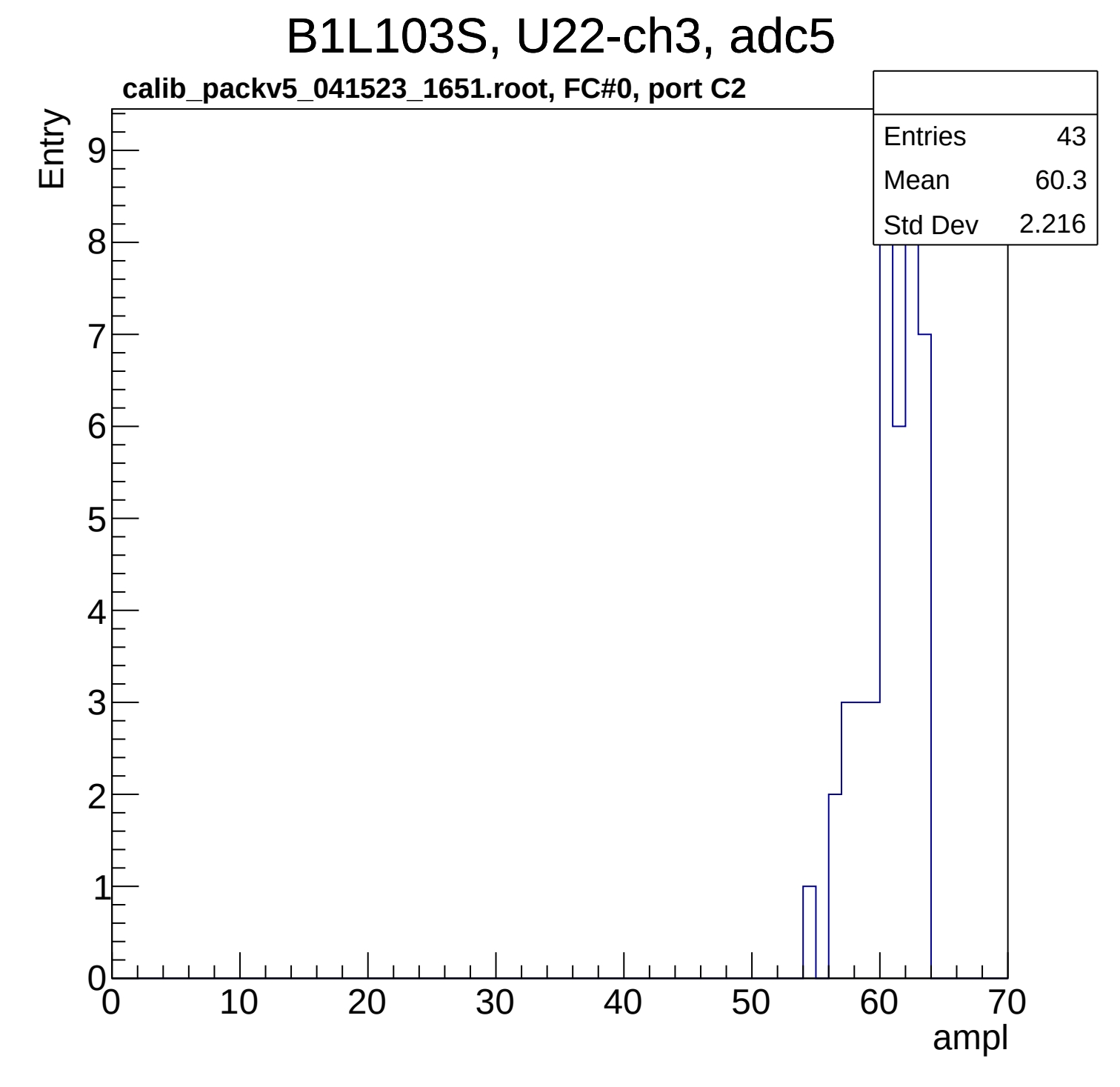
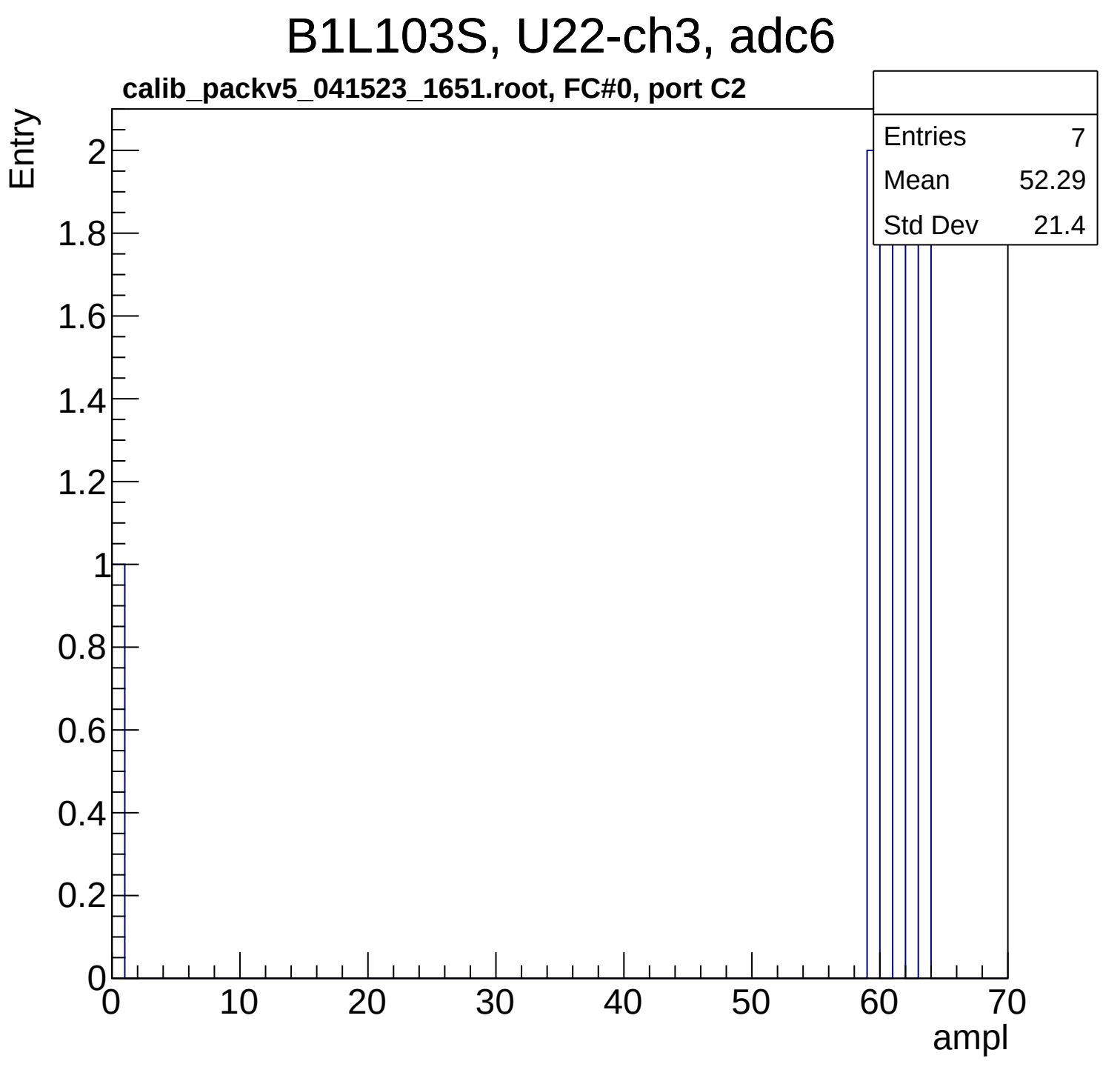
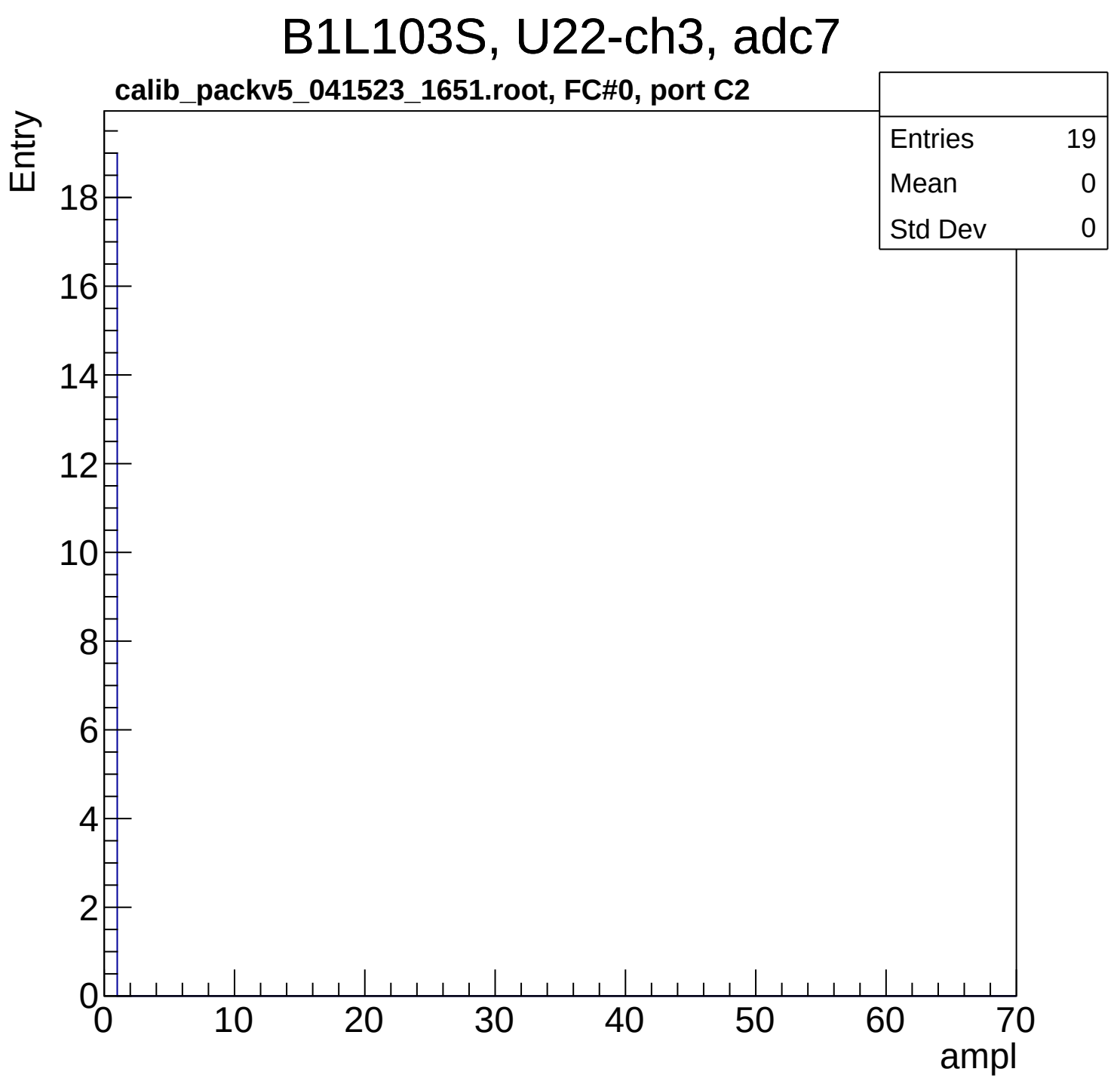
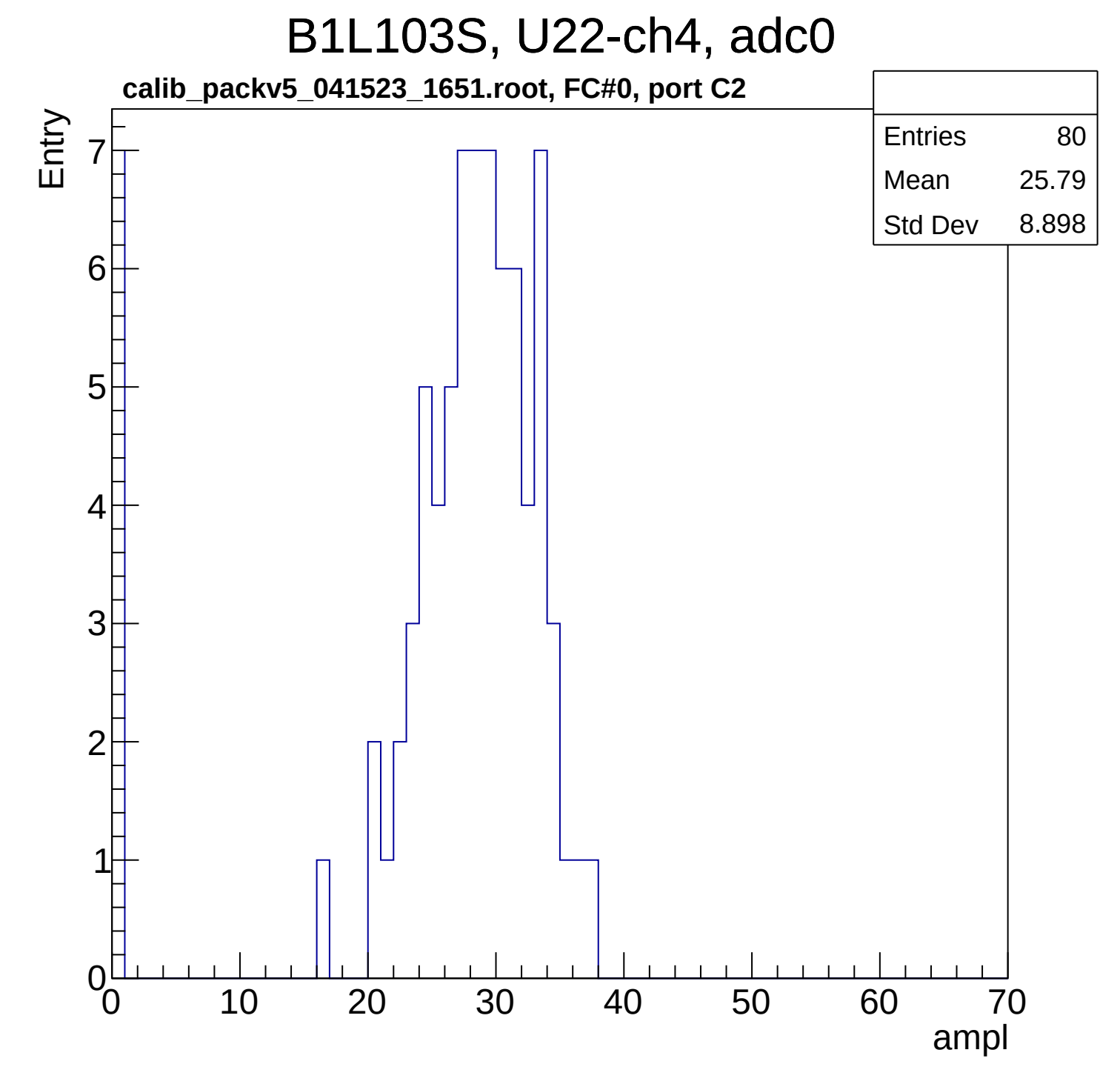

B1L103S, U22-ch3, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 55.65
Std Dev 3.395
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U22-ch3, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 60.3
Std Dev 2.216
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch3, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 52.29
Std Dev 21.4
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U22-ch3, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch4, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 25.79
Std Dev 8.898
Entry
ampl
0
1
2
3
4
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6
7
0
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20
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40
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60
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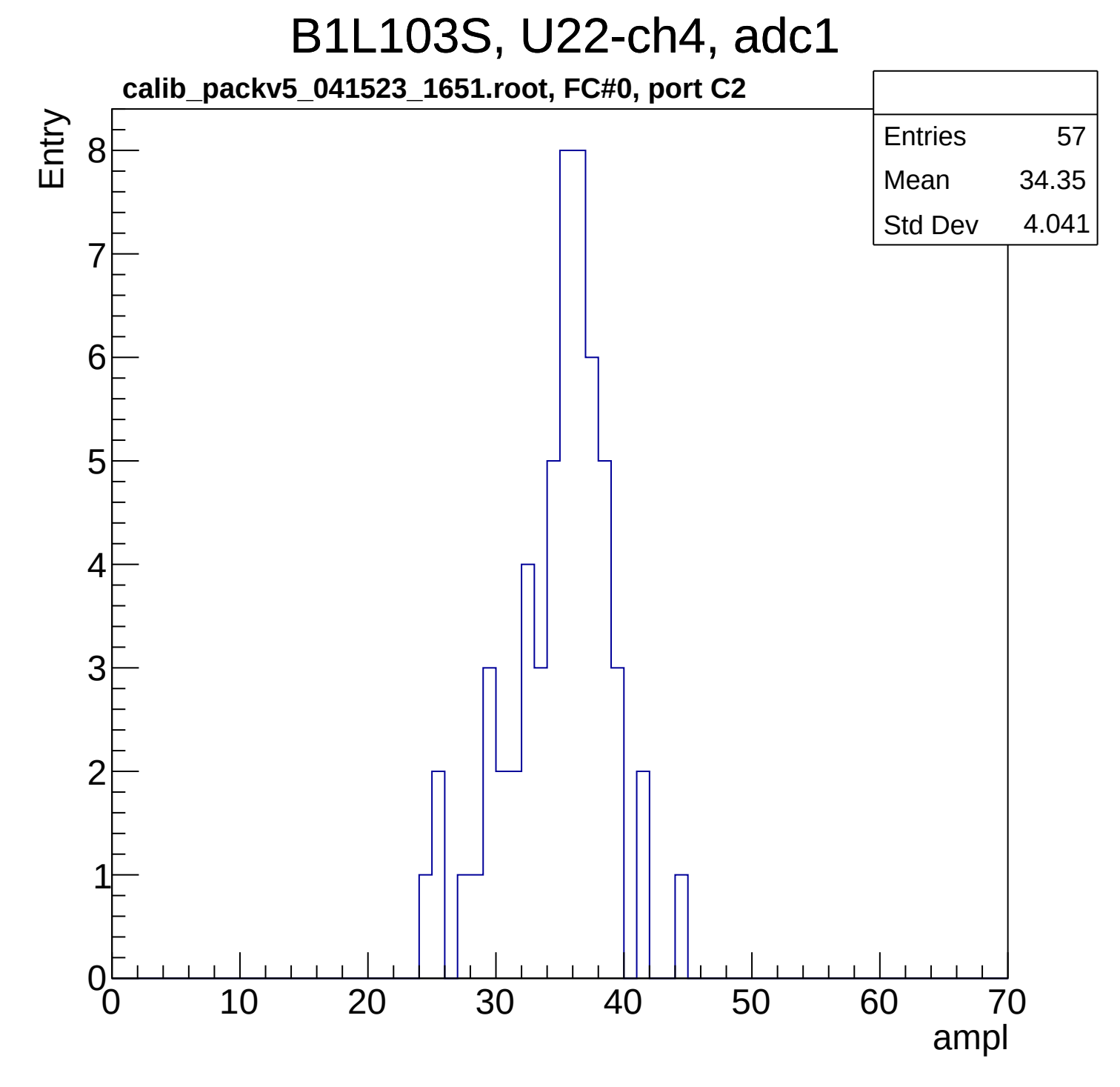
B1L103S, U22-ch4, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 34.35
Std Dev 4.041
Entry
ampl
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2
3
4
5
6
7
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0
10
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30
40
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60
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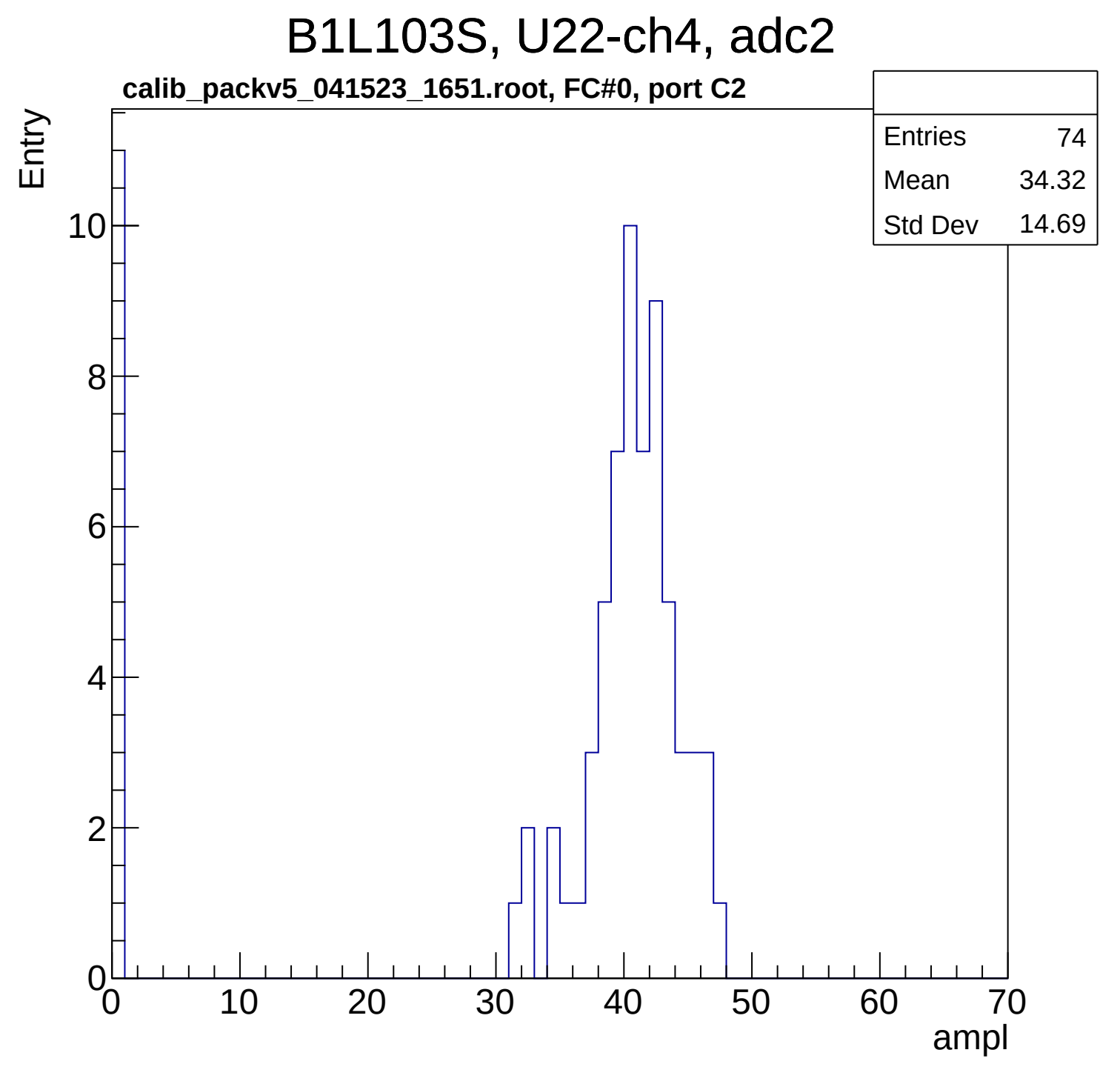
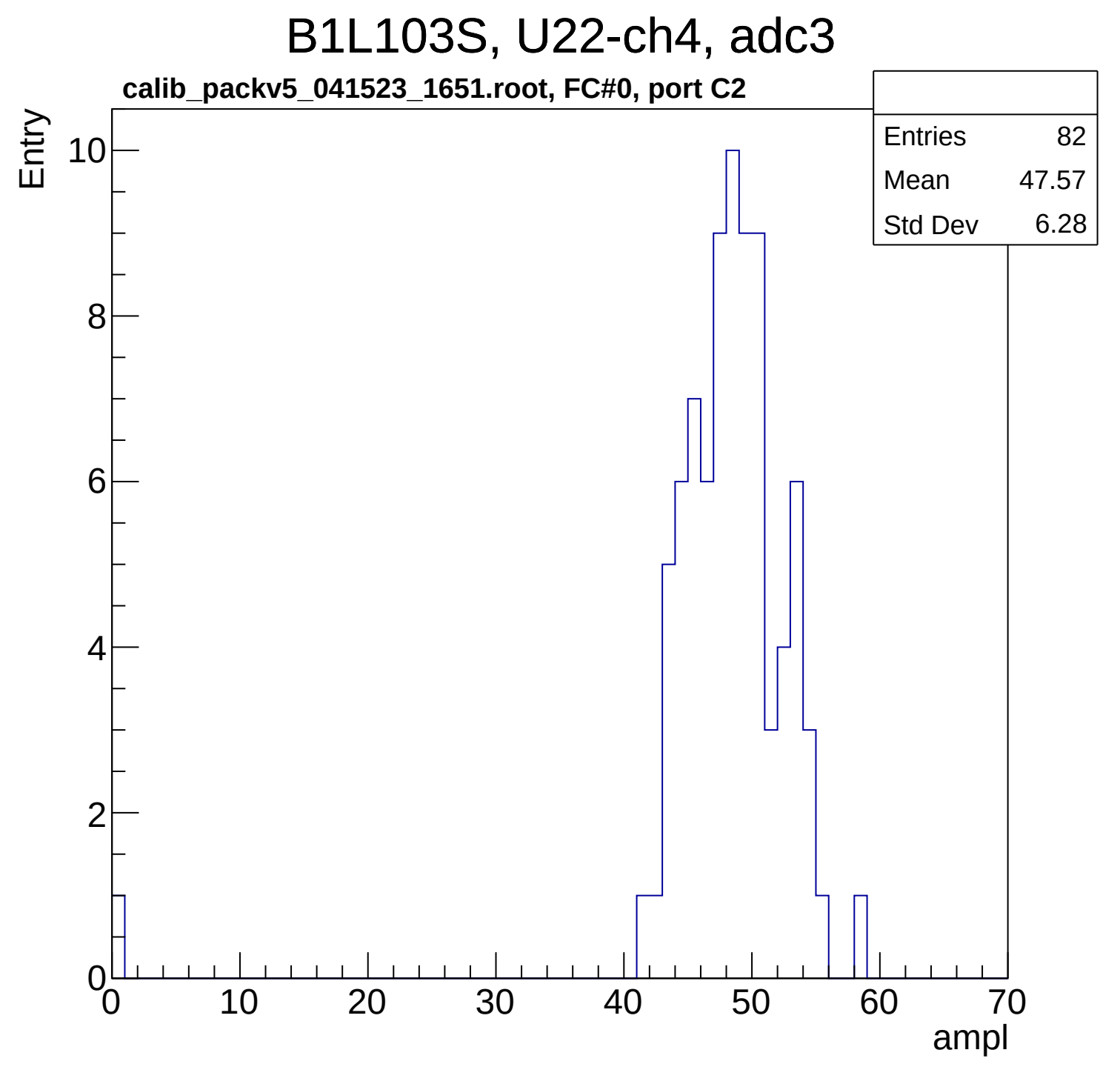

B1L103S, U22-ch4, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 34.32
Std Dev 14.69
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch4, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 47.57
Std Dev 6.28
Entry
ampl
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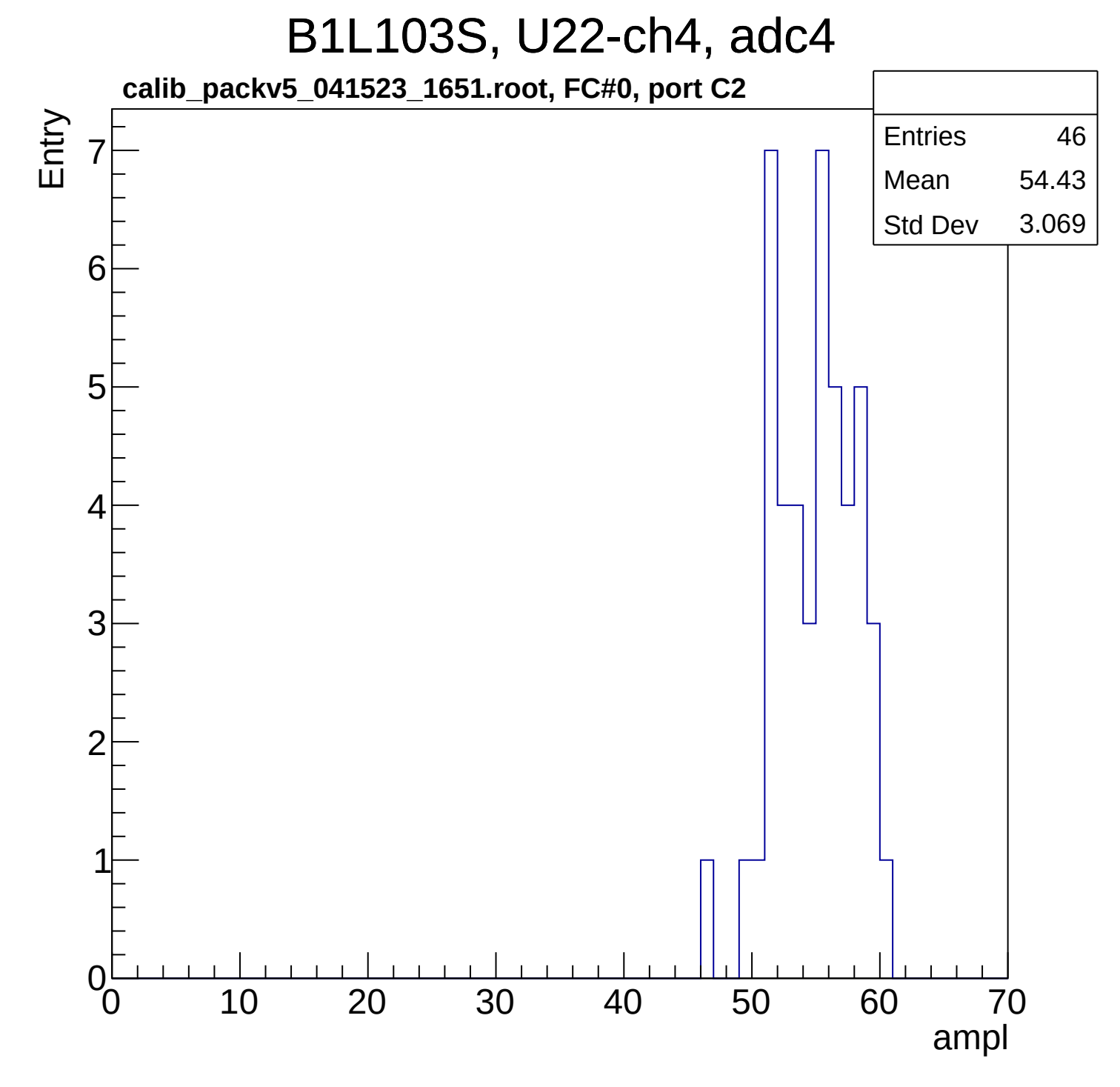
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U22-ch4, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 54.43
Std Dev 3.069
Entry
ampl
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2
3
4
5
6
7
0
10
20
30
40
50
60
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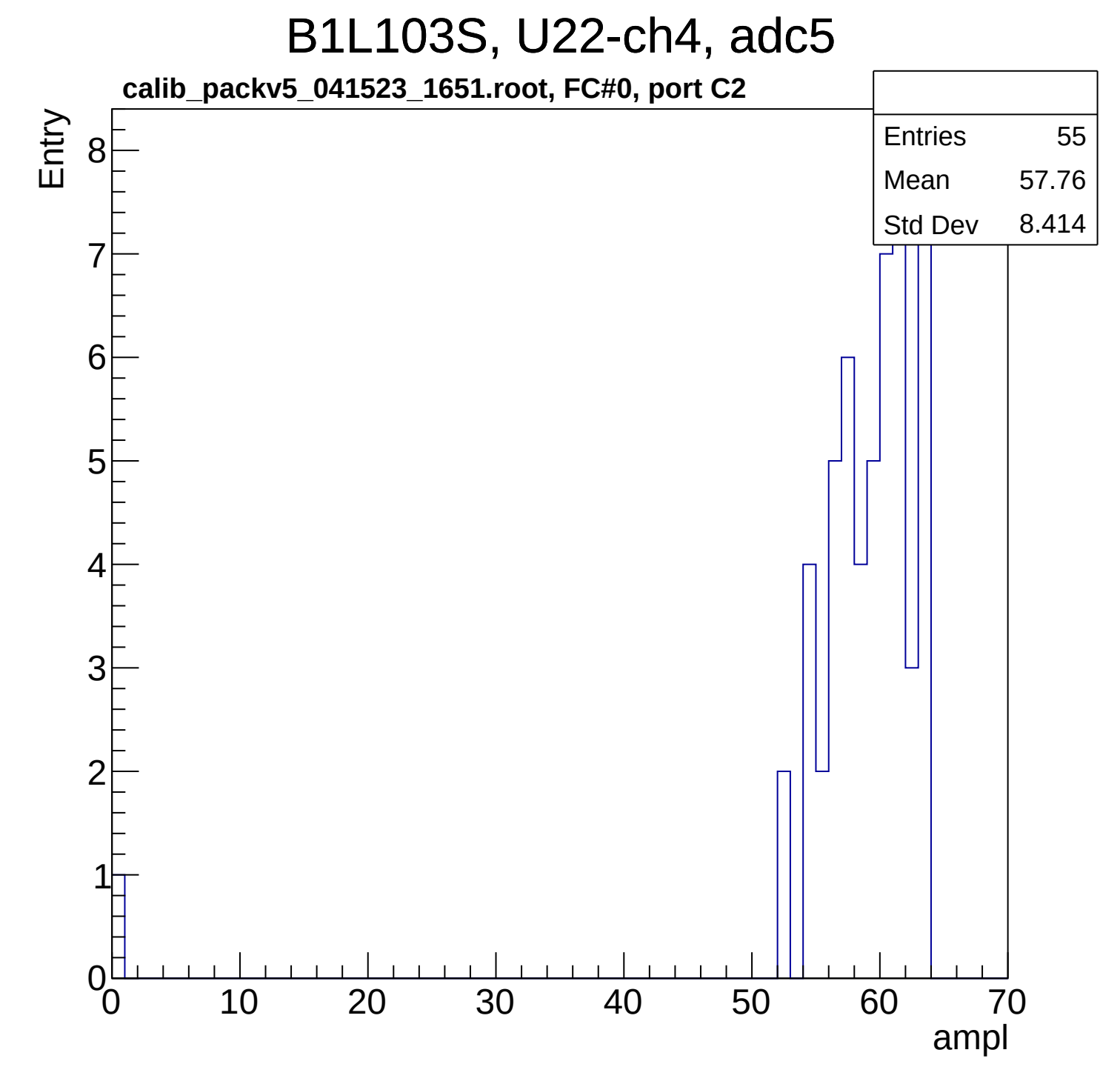
B1L103S, U22-ch4, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 57.76
Std Dev 8.414
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
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60
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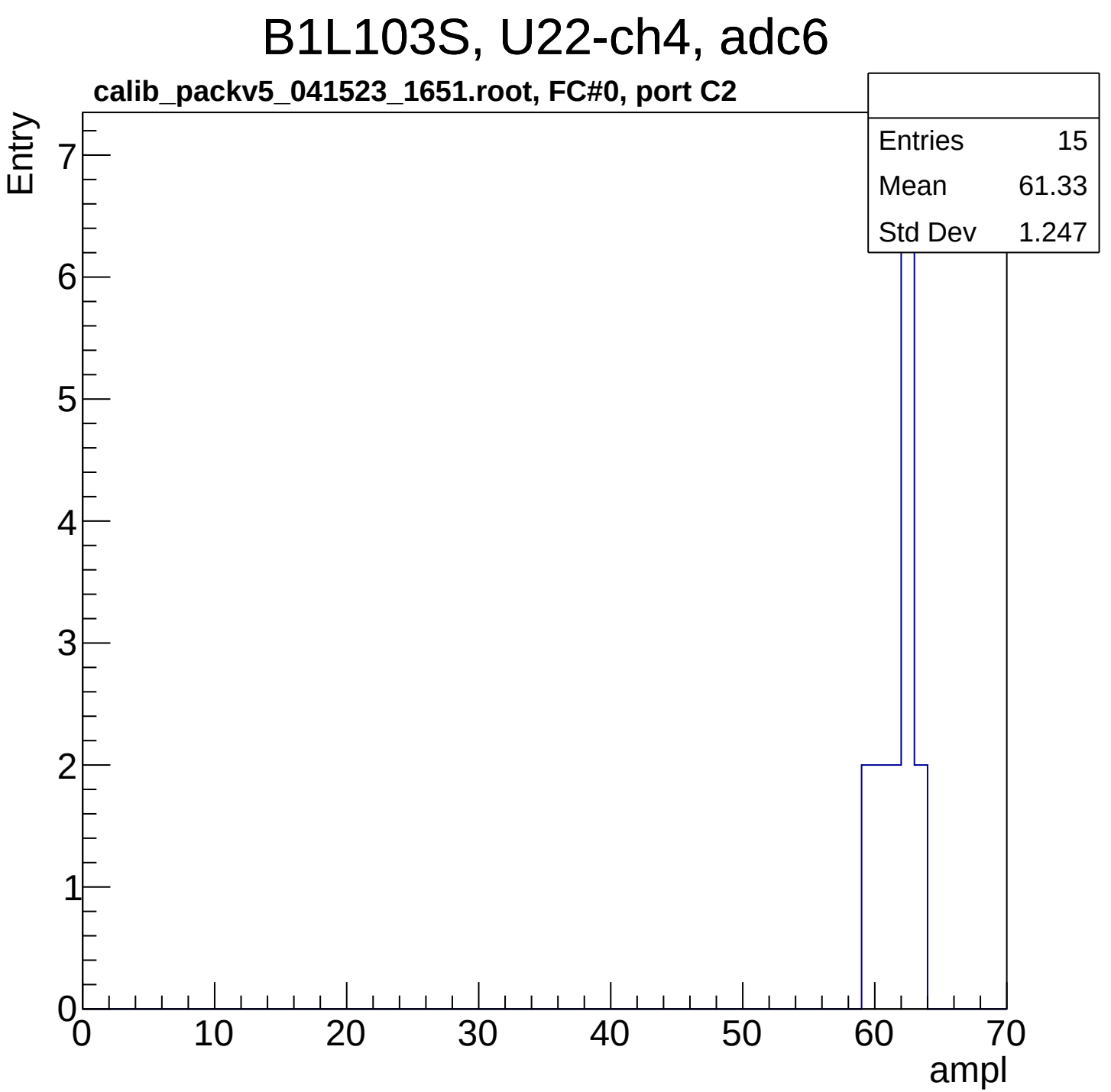
B1L103S, U22-ch4, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 61.33
Std Dev 1.247
Entry
ampl
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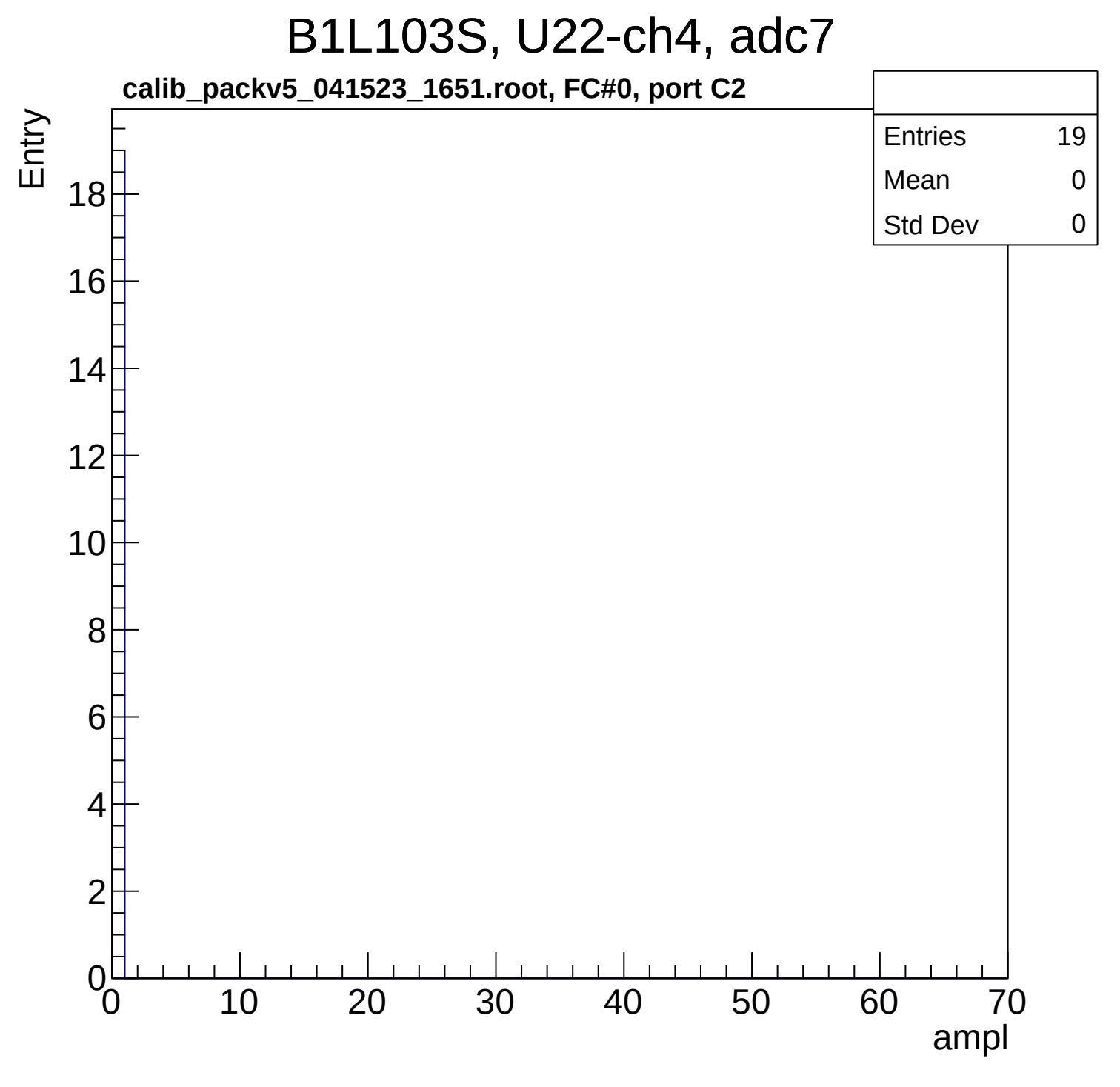
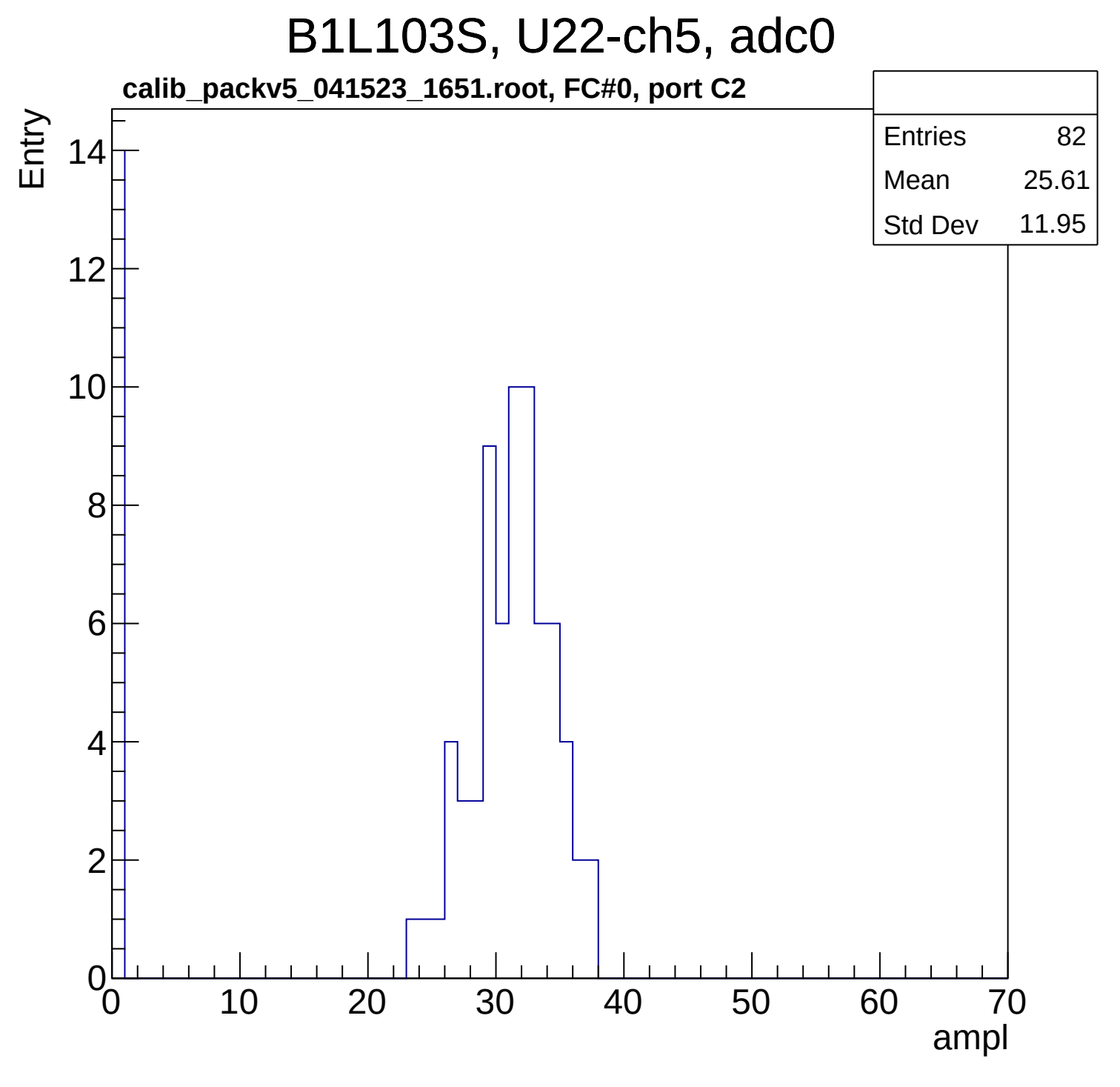
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U22-ch4, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch5, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 25.61
Std Dev 11.95
Entry
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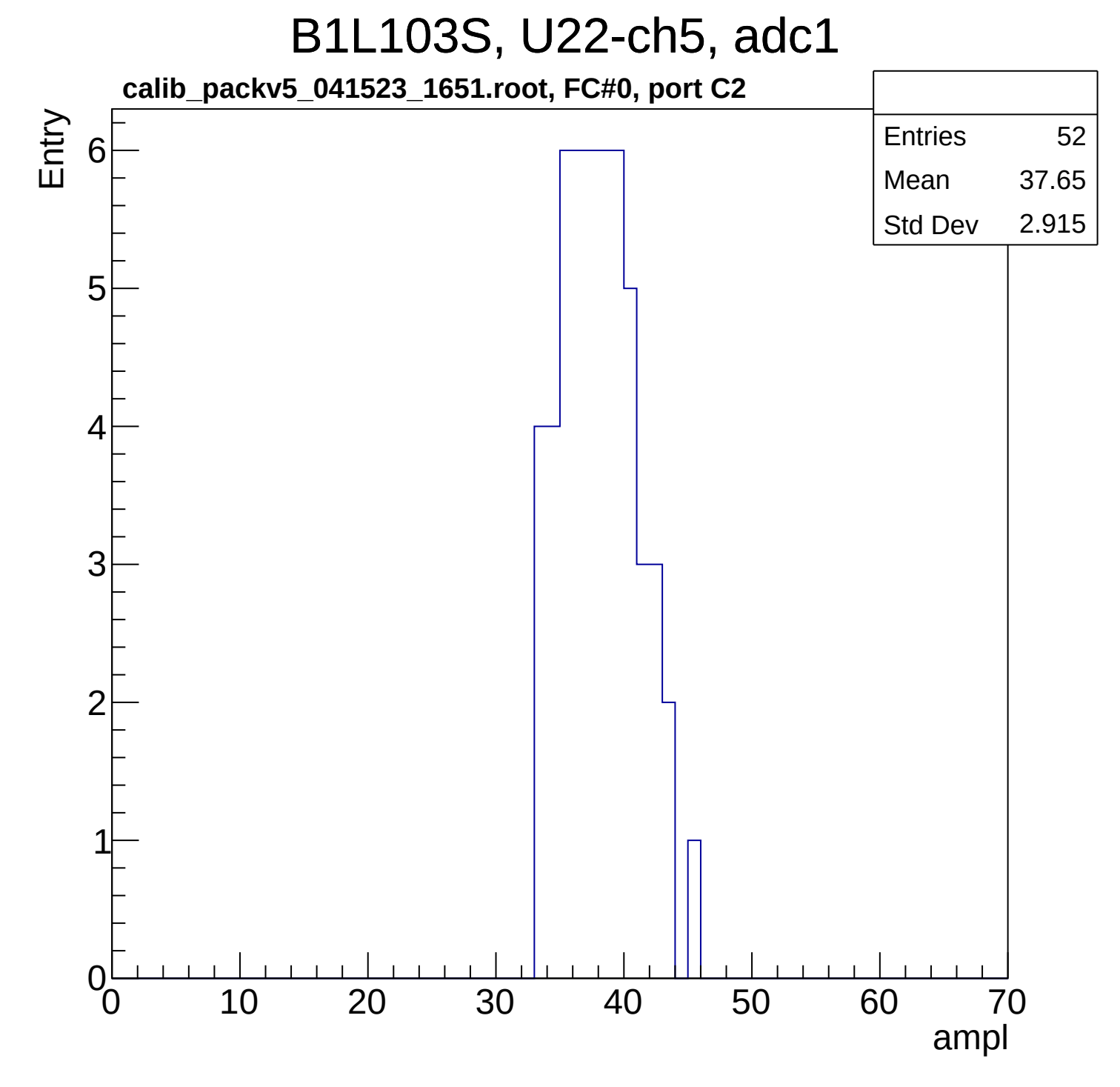
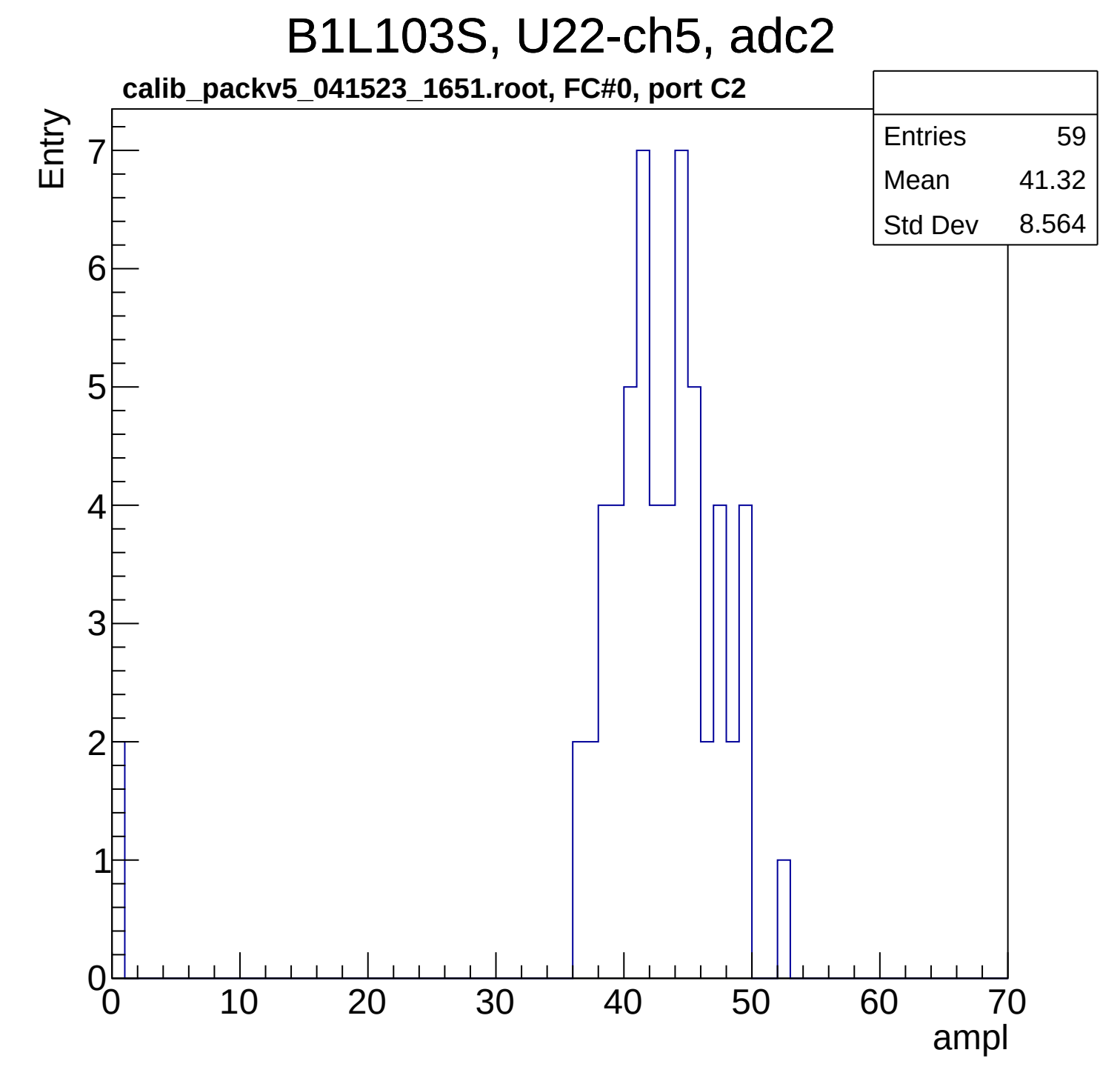
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch5, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 37.65
Std Dev 2.915
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U22-ch5, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 41.32
Std Dev 8.564
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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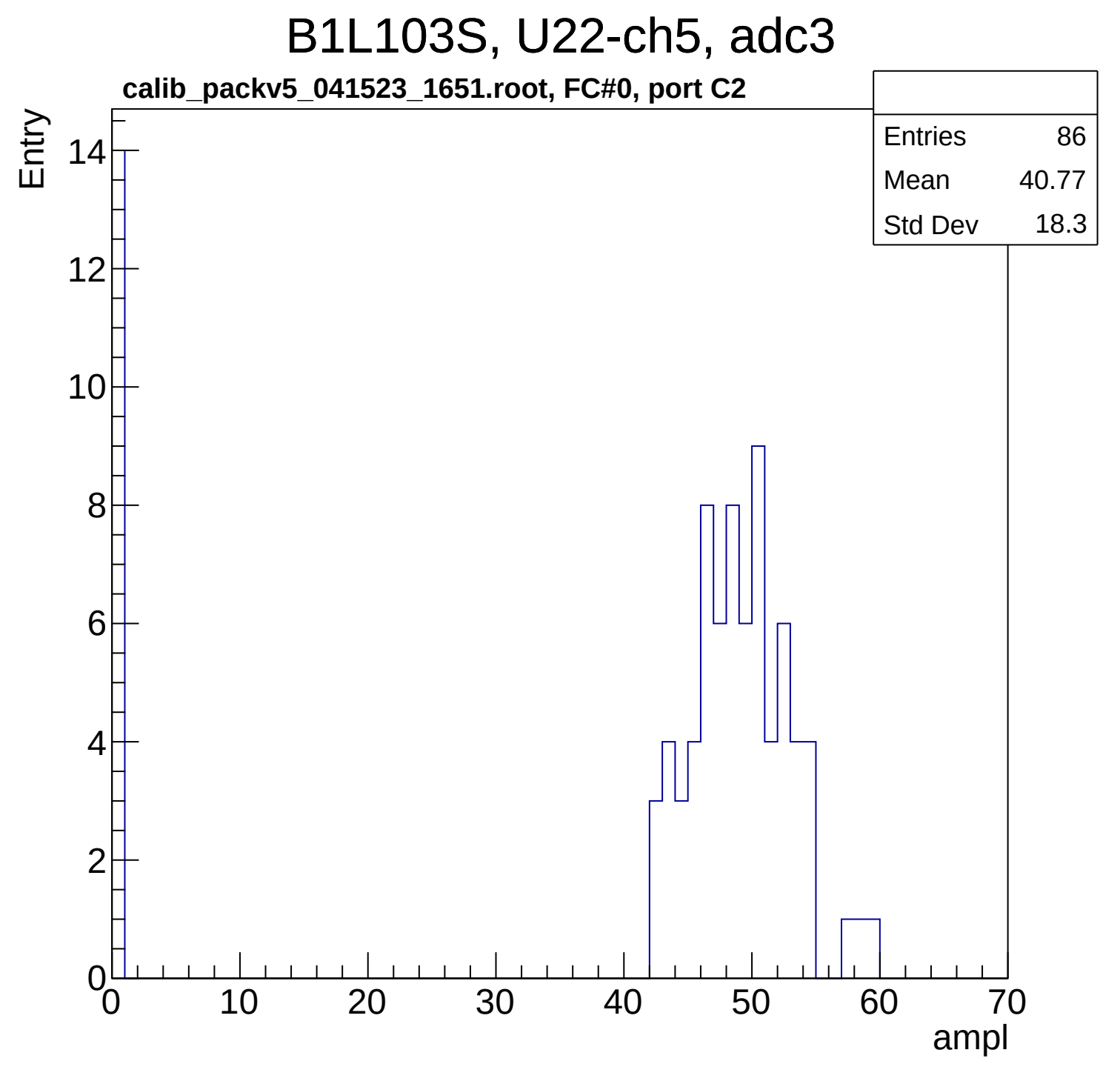
B1L103S, U22-ch5, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 40.77
Std Dev 18.3
Entry
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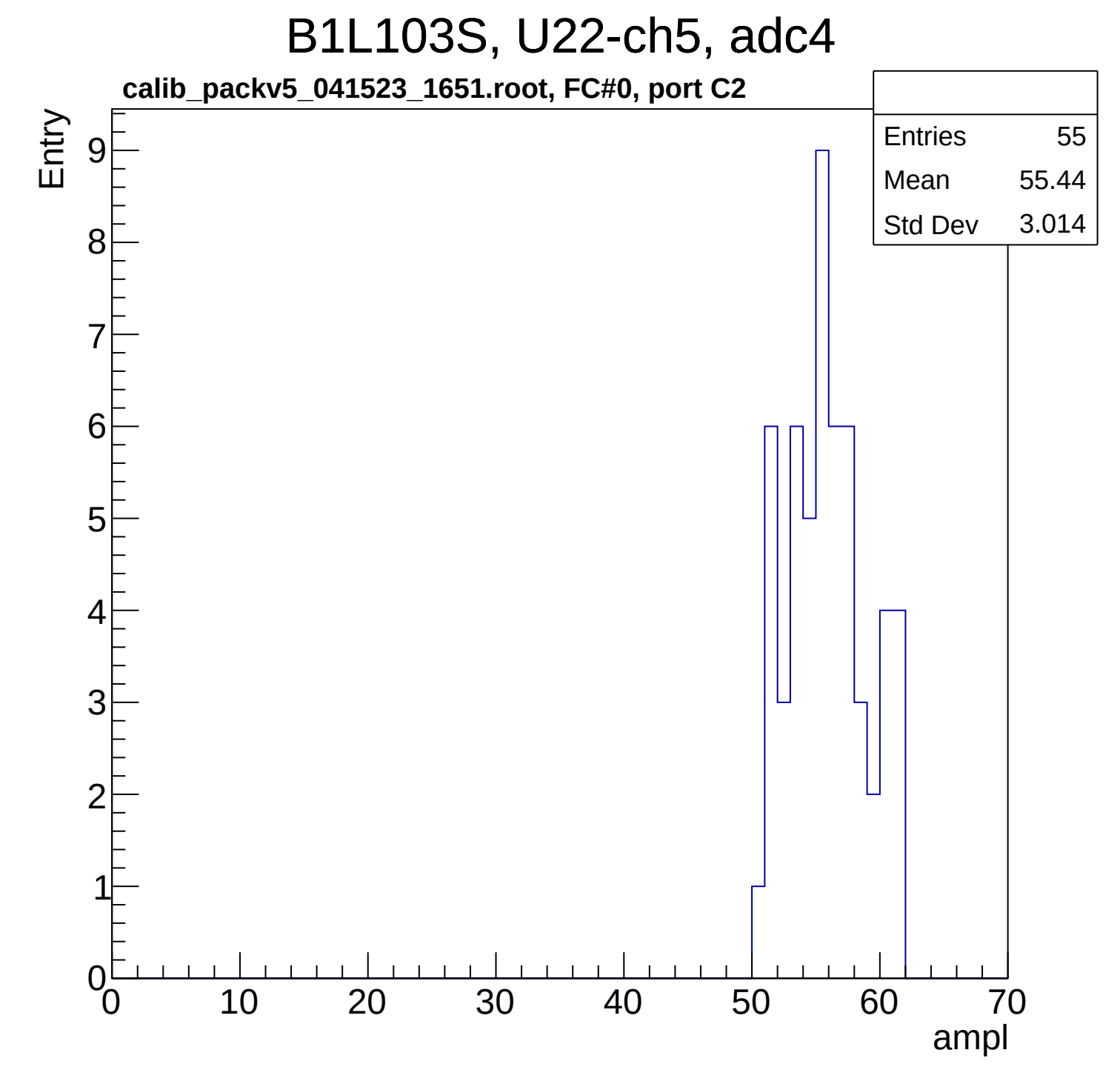
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch5, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 55.44
Std Dev 3.014
Entry
ampl
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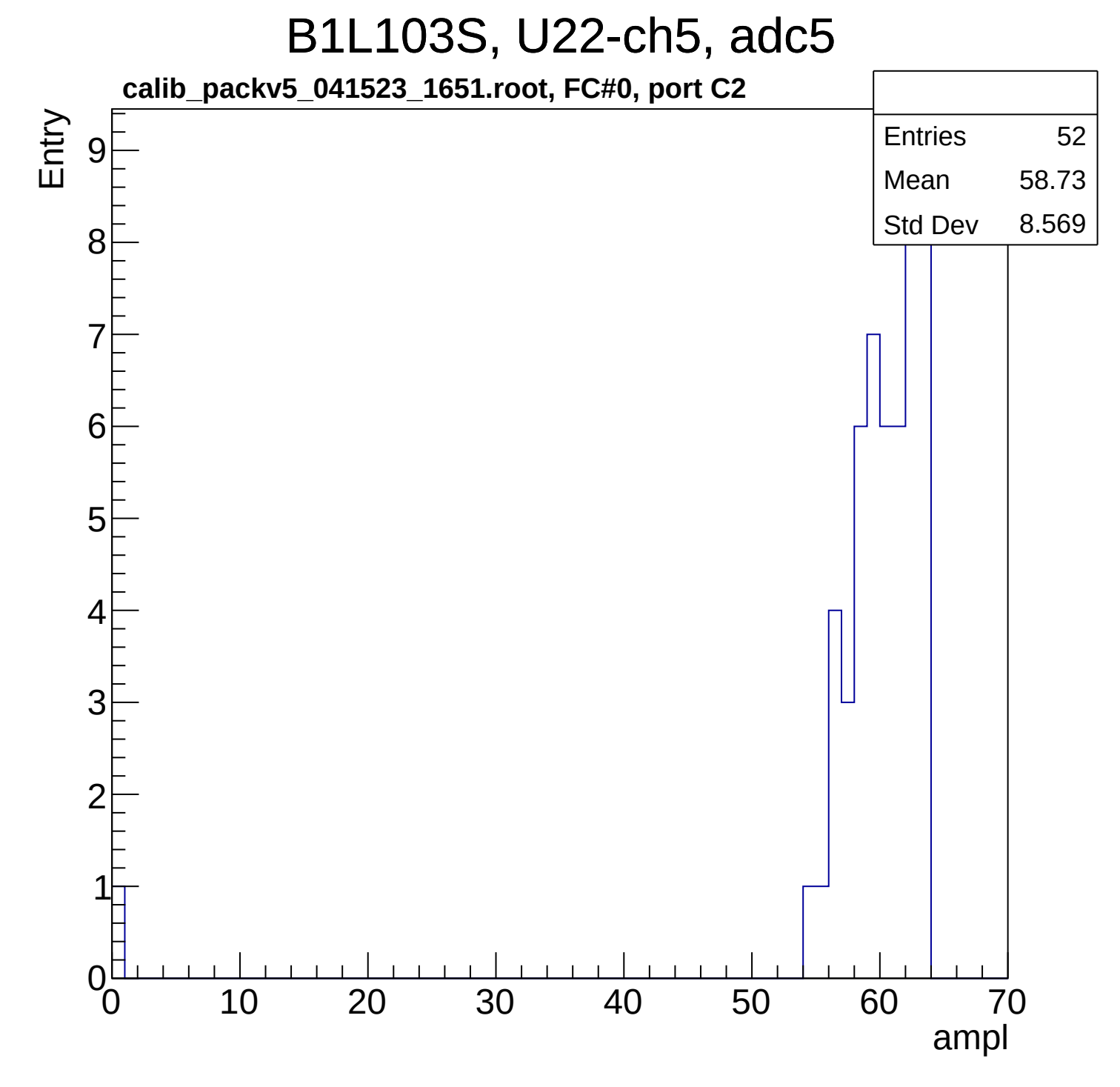
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch5, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 58.73
Std Dev 8.569
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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20
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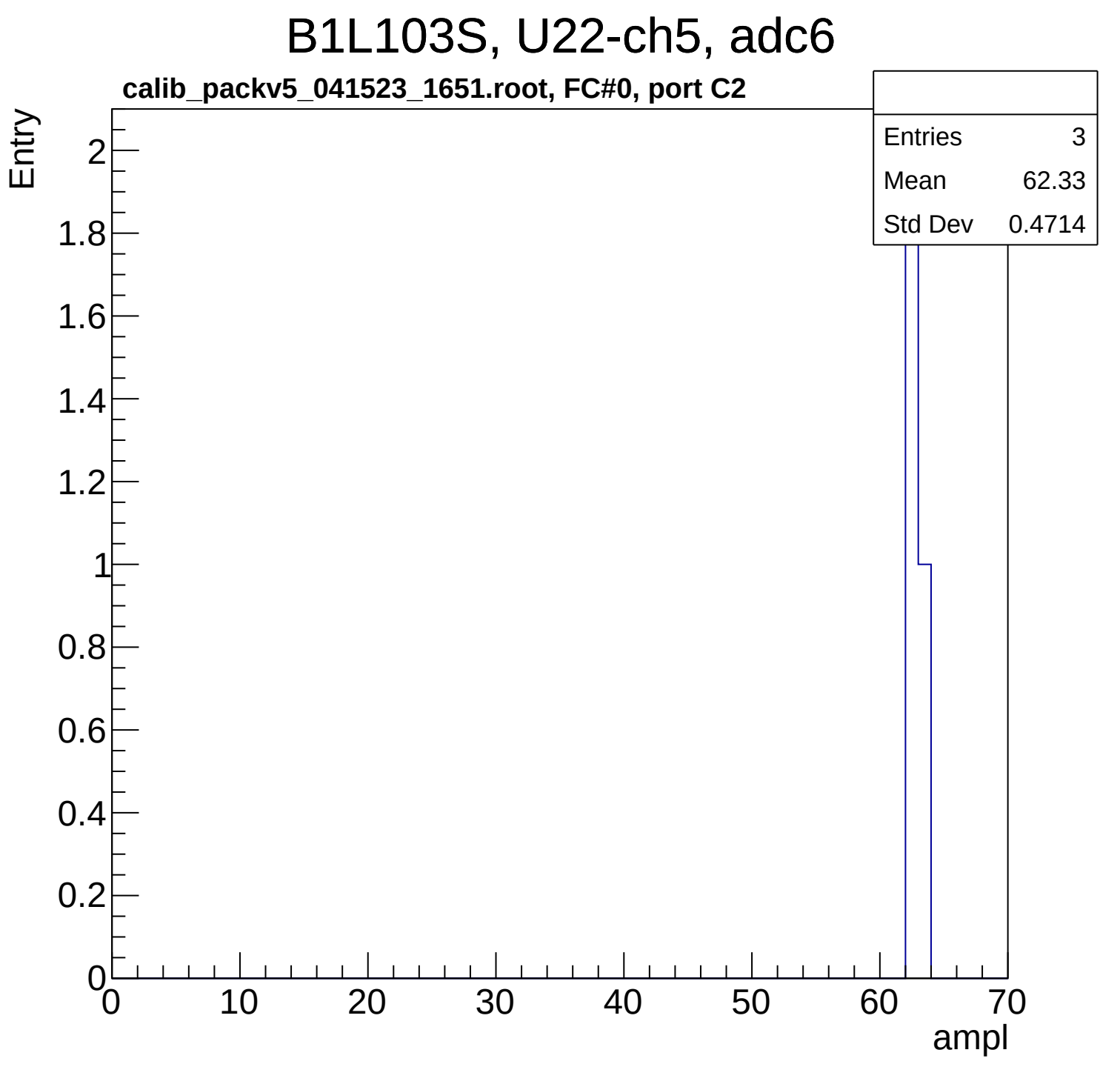
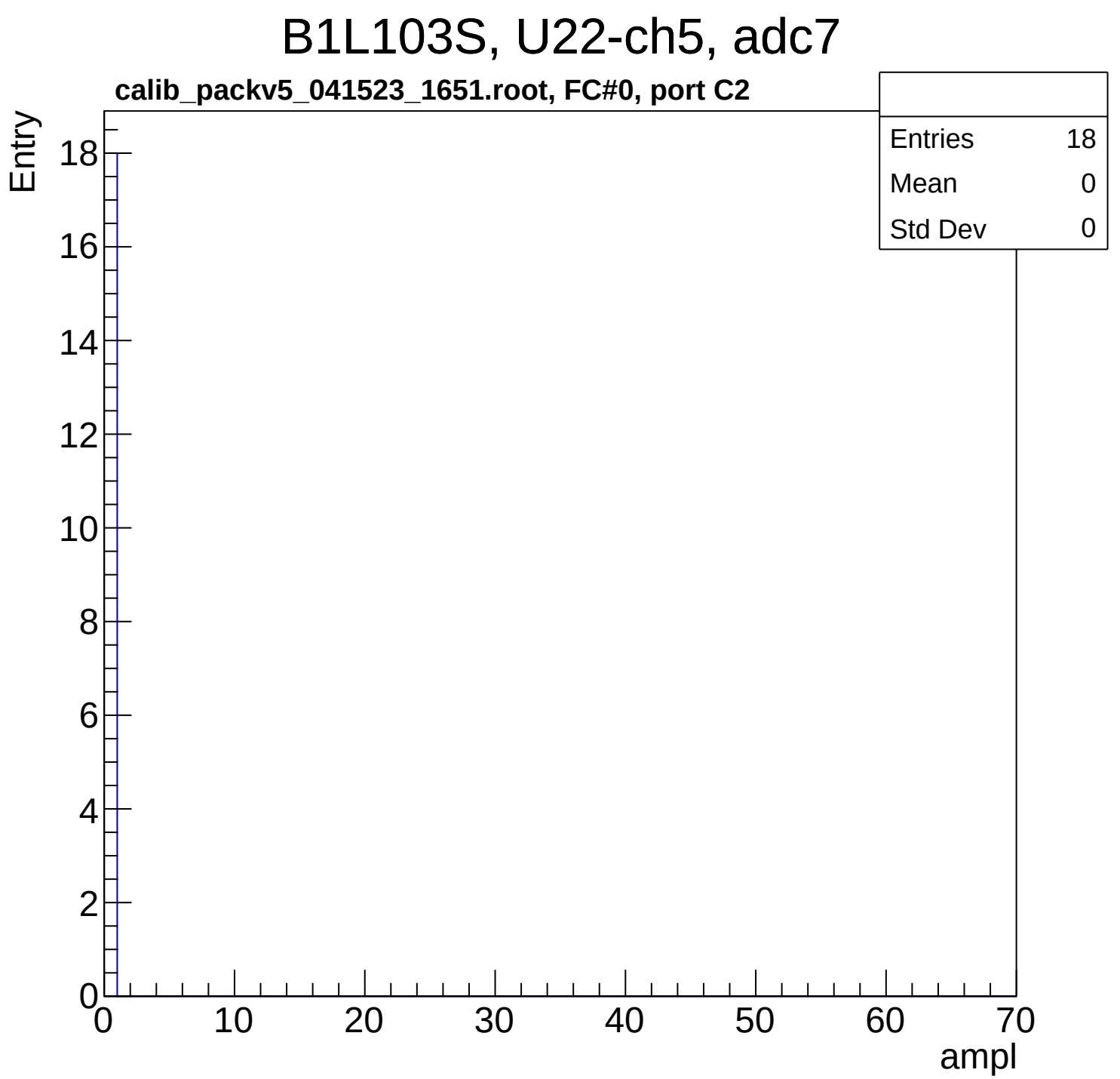
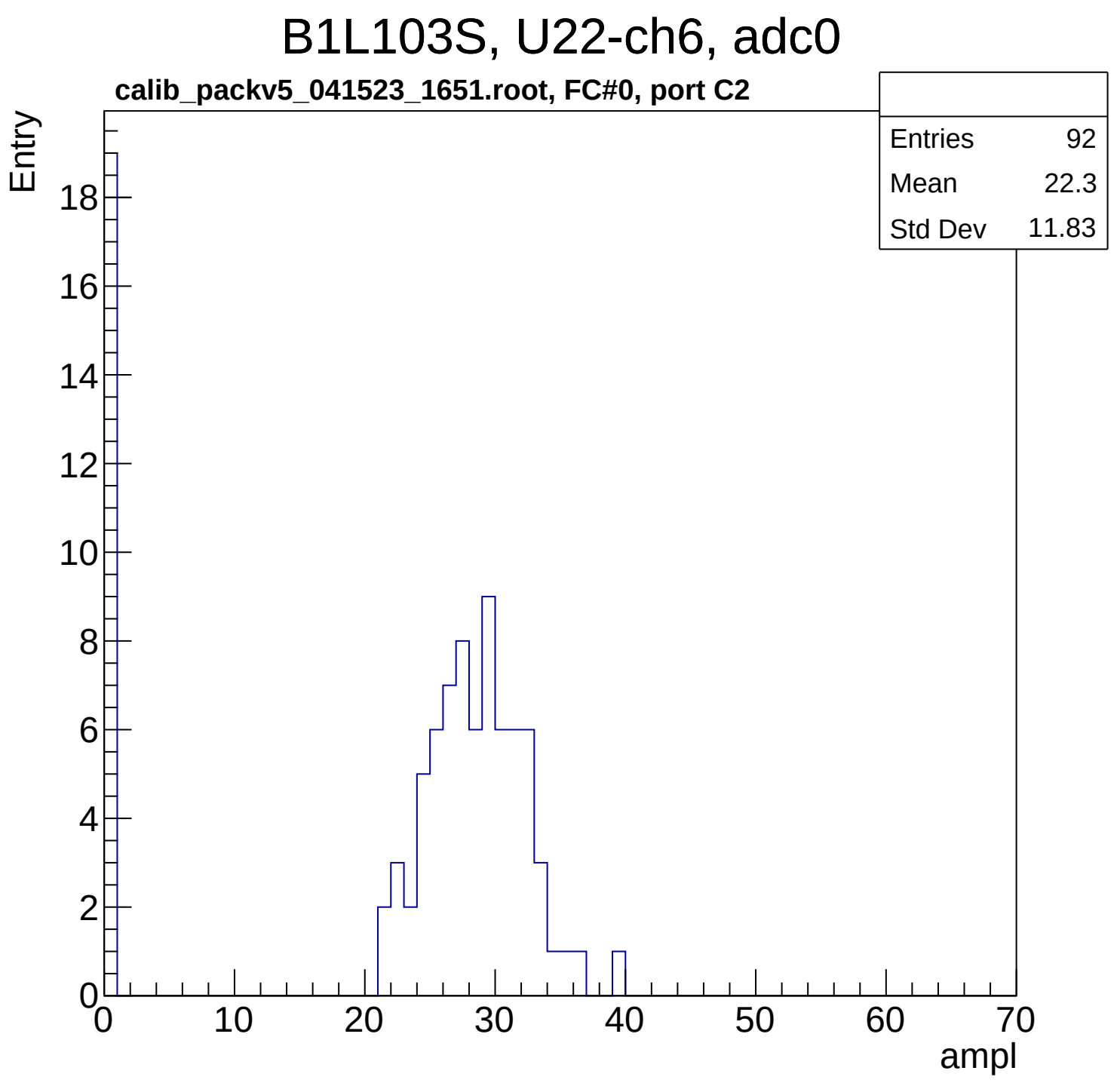
40
50
60
70


B1L103S, U22-ch5, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 62.33
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U22-ch5, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch6, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 22.3
Std Dev 11.83
Entry
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6
8
10
12
14
16
18
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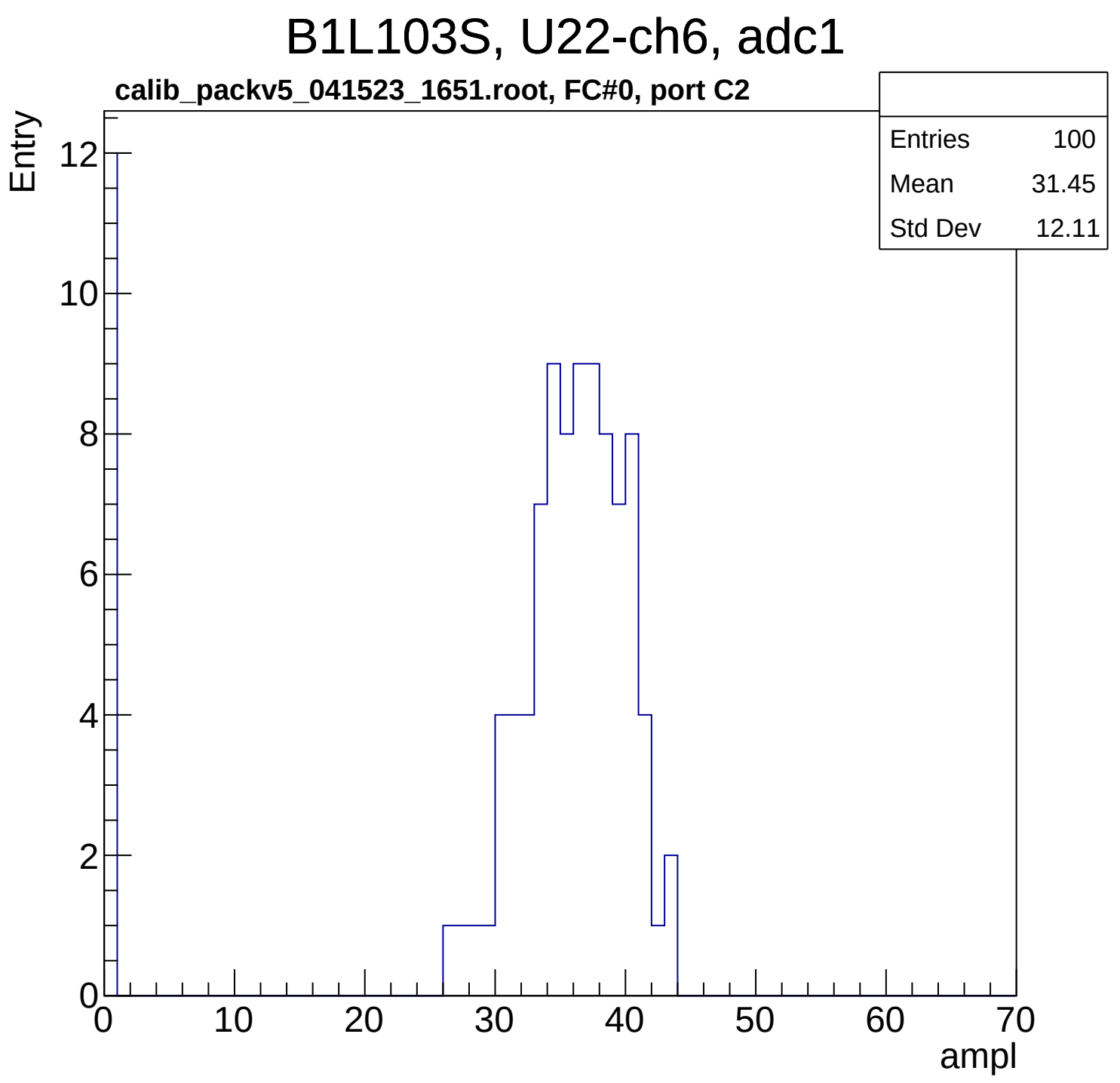
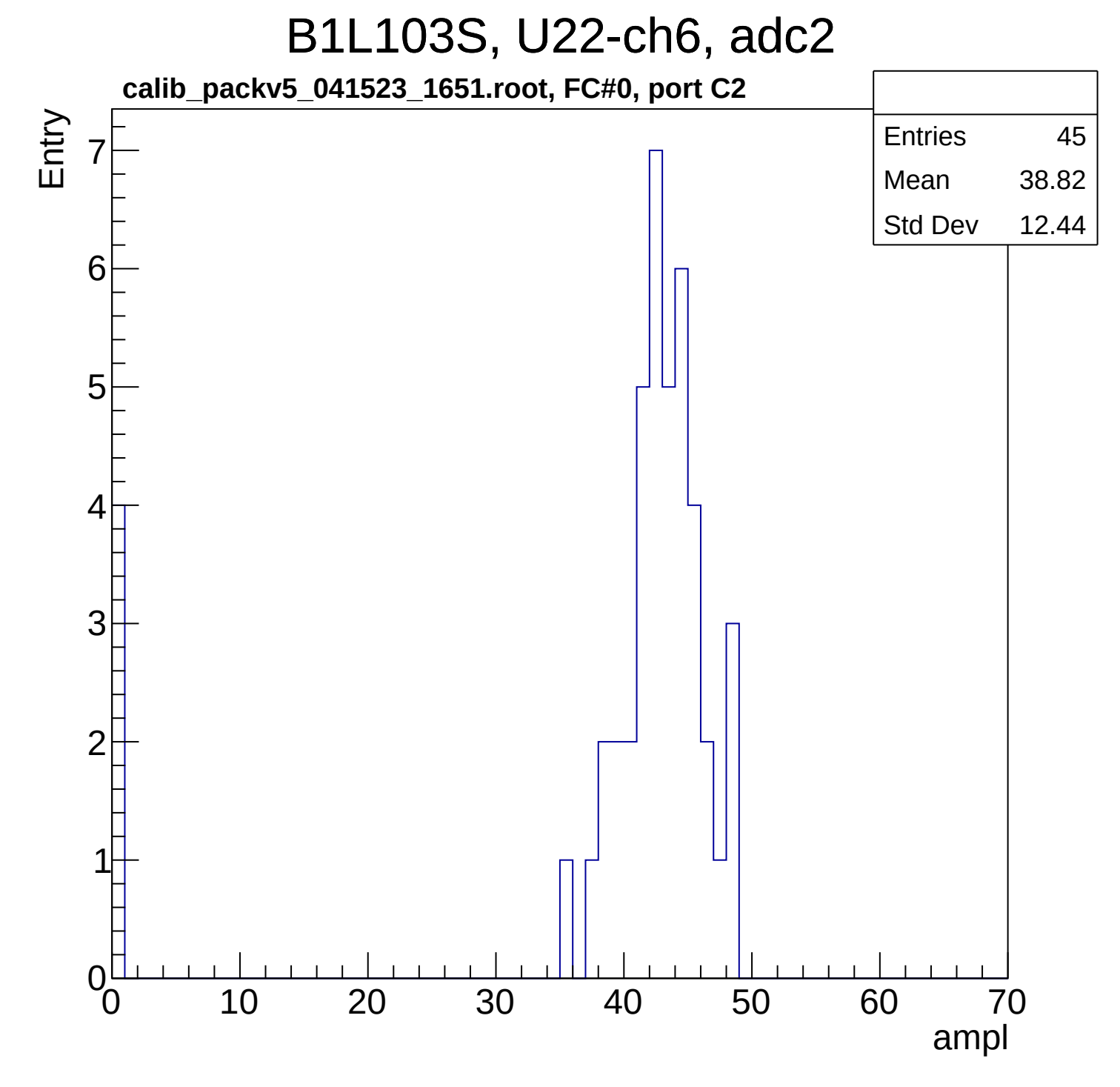
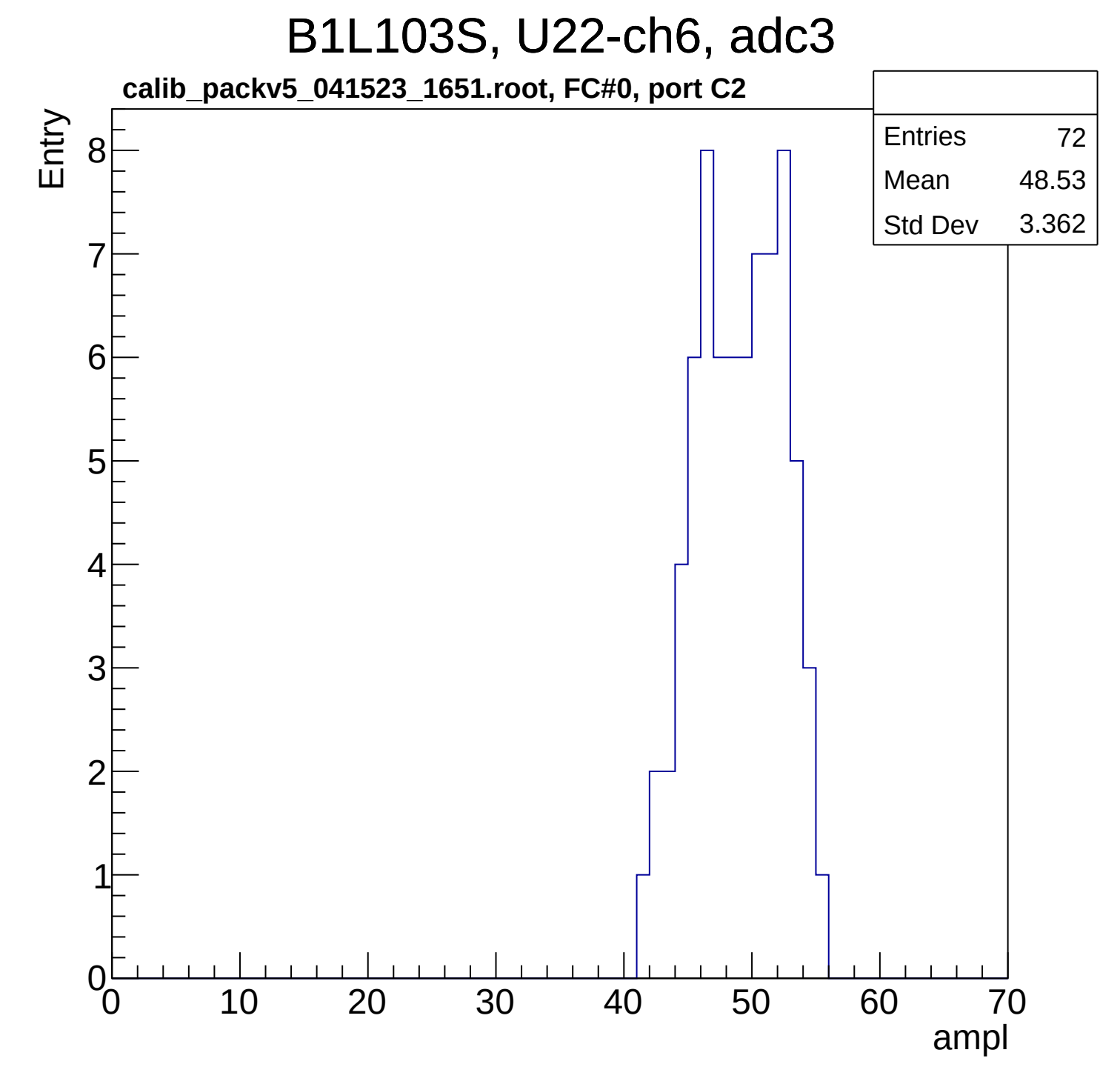
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch6, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 100
Mean 31.45
Std Dev 12.11
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch6, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 38.82
Std Dev 12.44
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U22-ch6, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 48.53
Std Dev 3.362
Entry
ampl
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2
3
4
5
6
7
8
0
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40
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60
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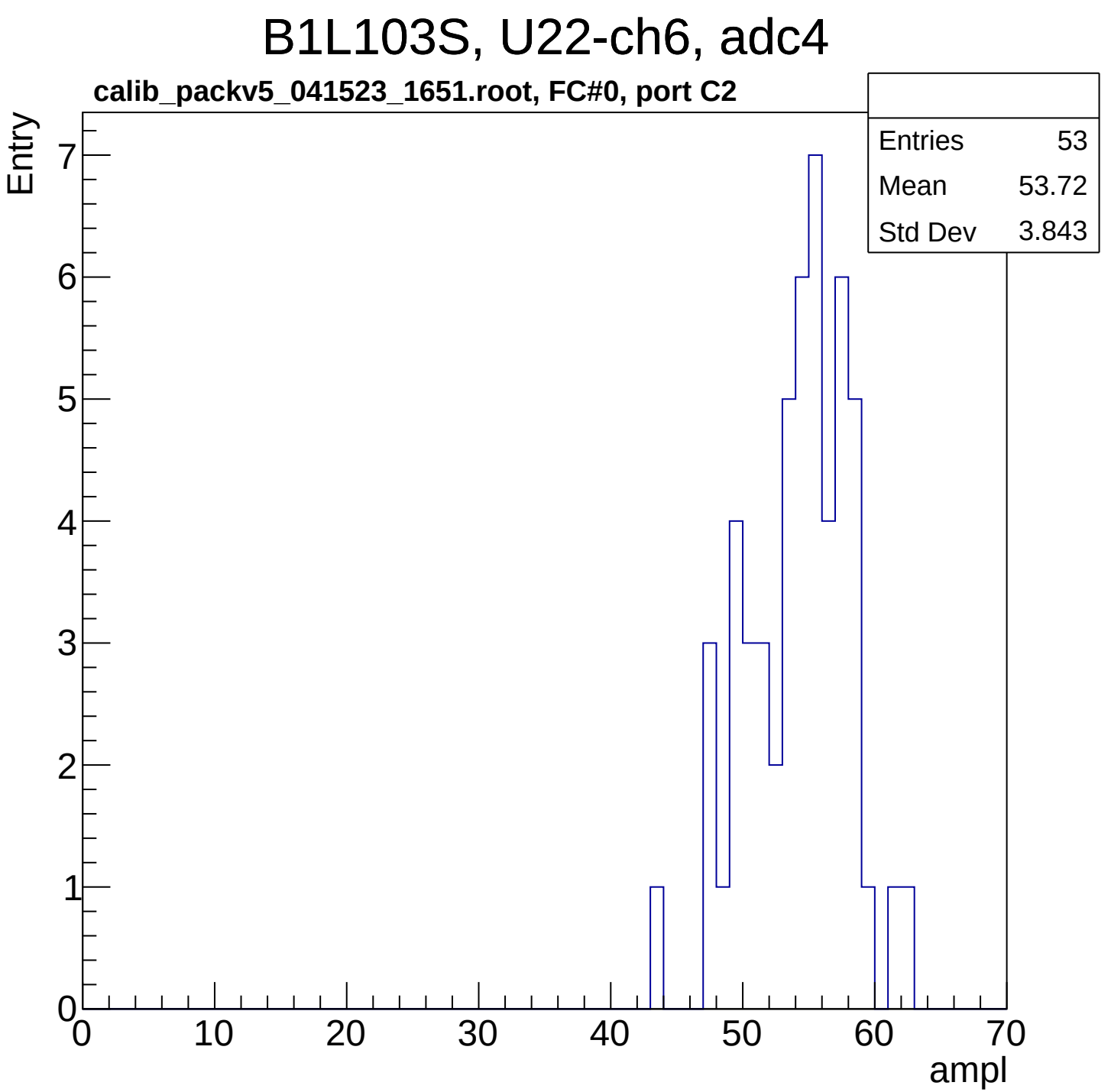
B1L103S, U22-ch6, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 53.72
Std Dev 3.843
Entry
ampl
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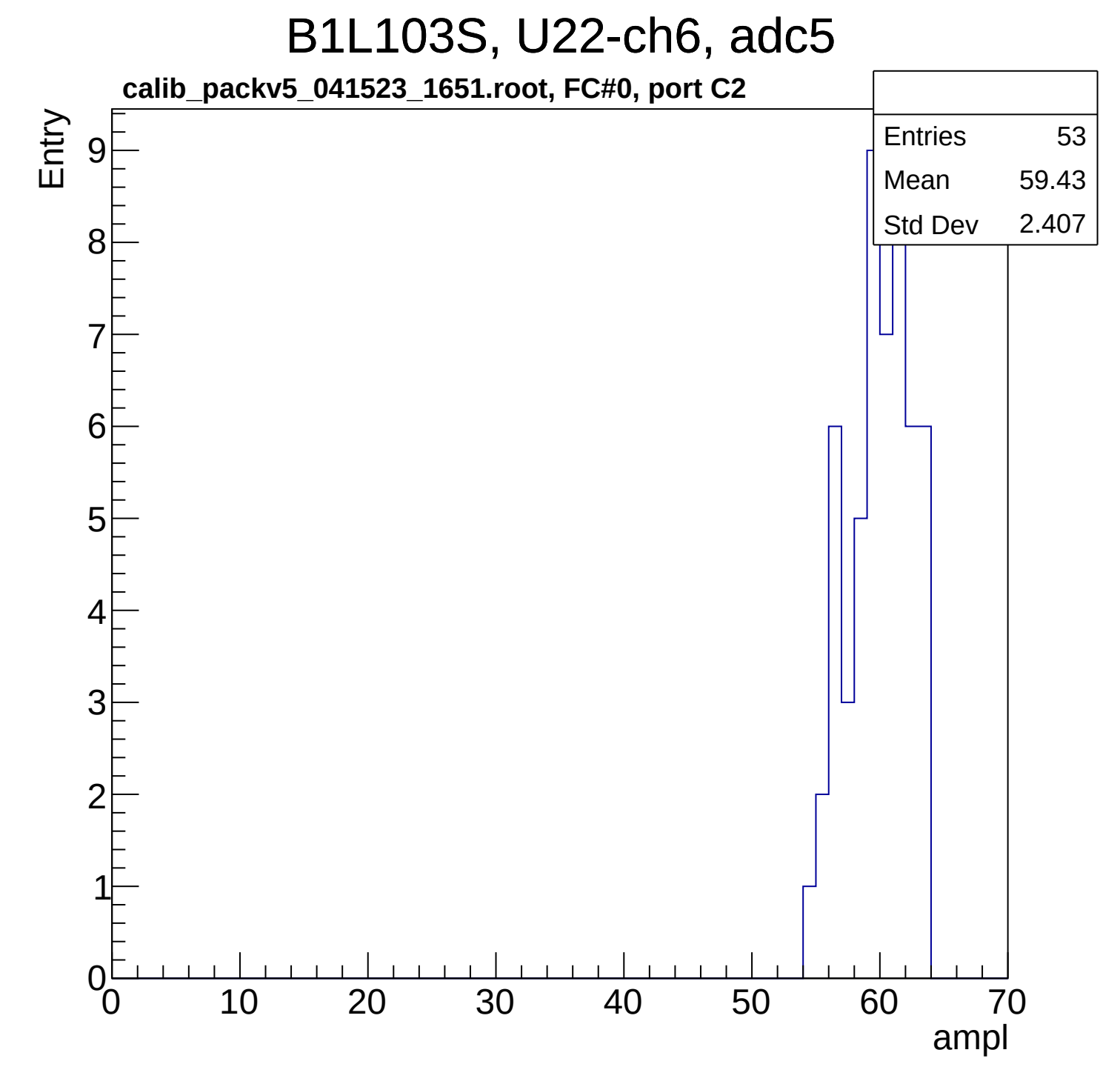
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U22-ch6, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 59.43
Std Dev 2.407
Entry
ampl
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2
3
4
5
6
7
8
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0
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60
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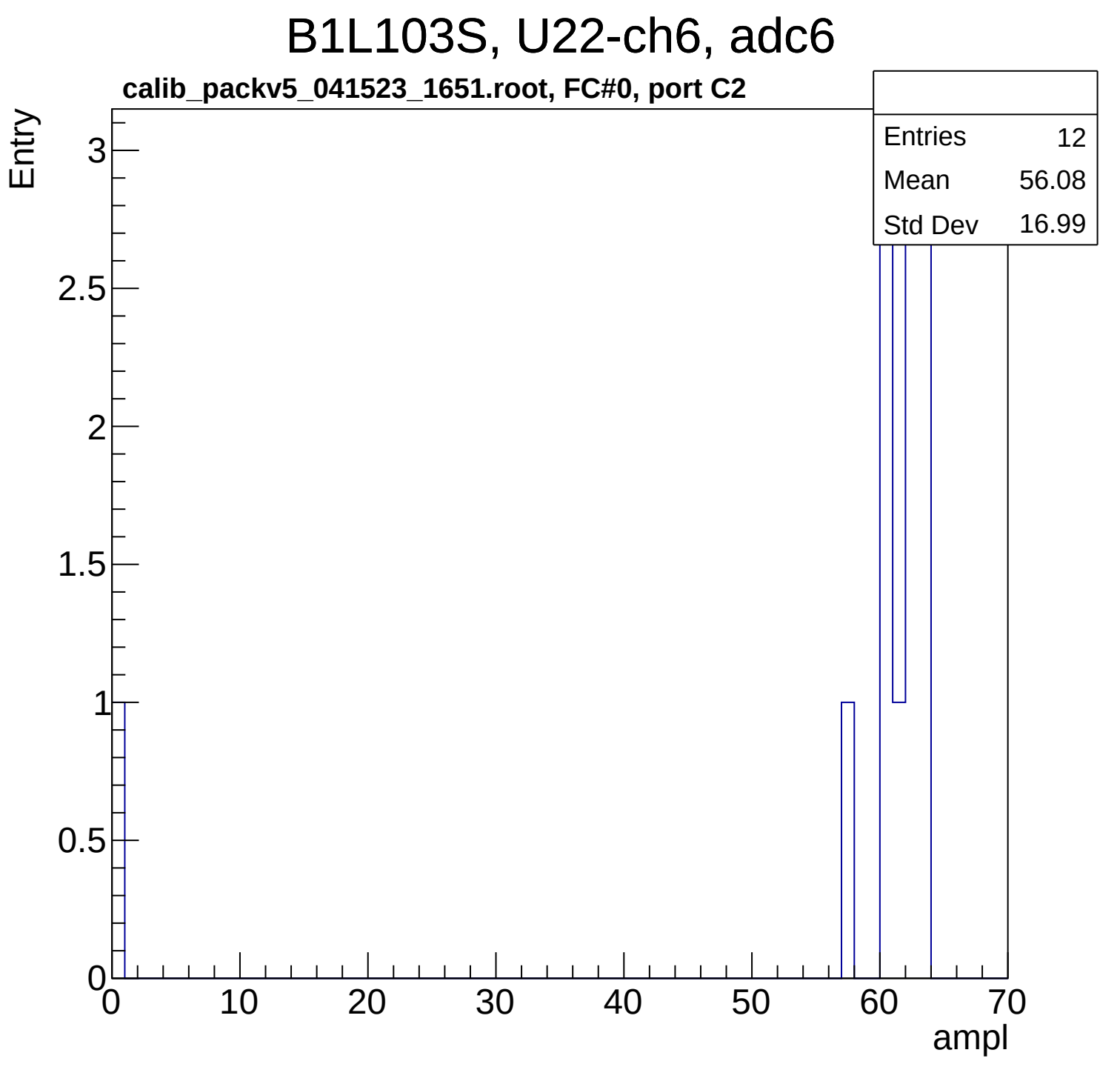
B1L103S, U22-ch6, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 56.08
Std Dev 16.99
Entry
ampl
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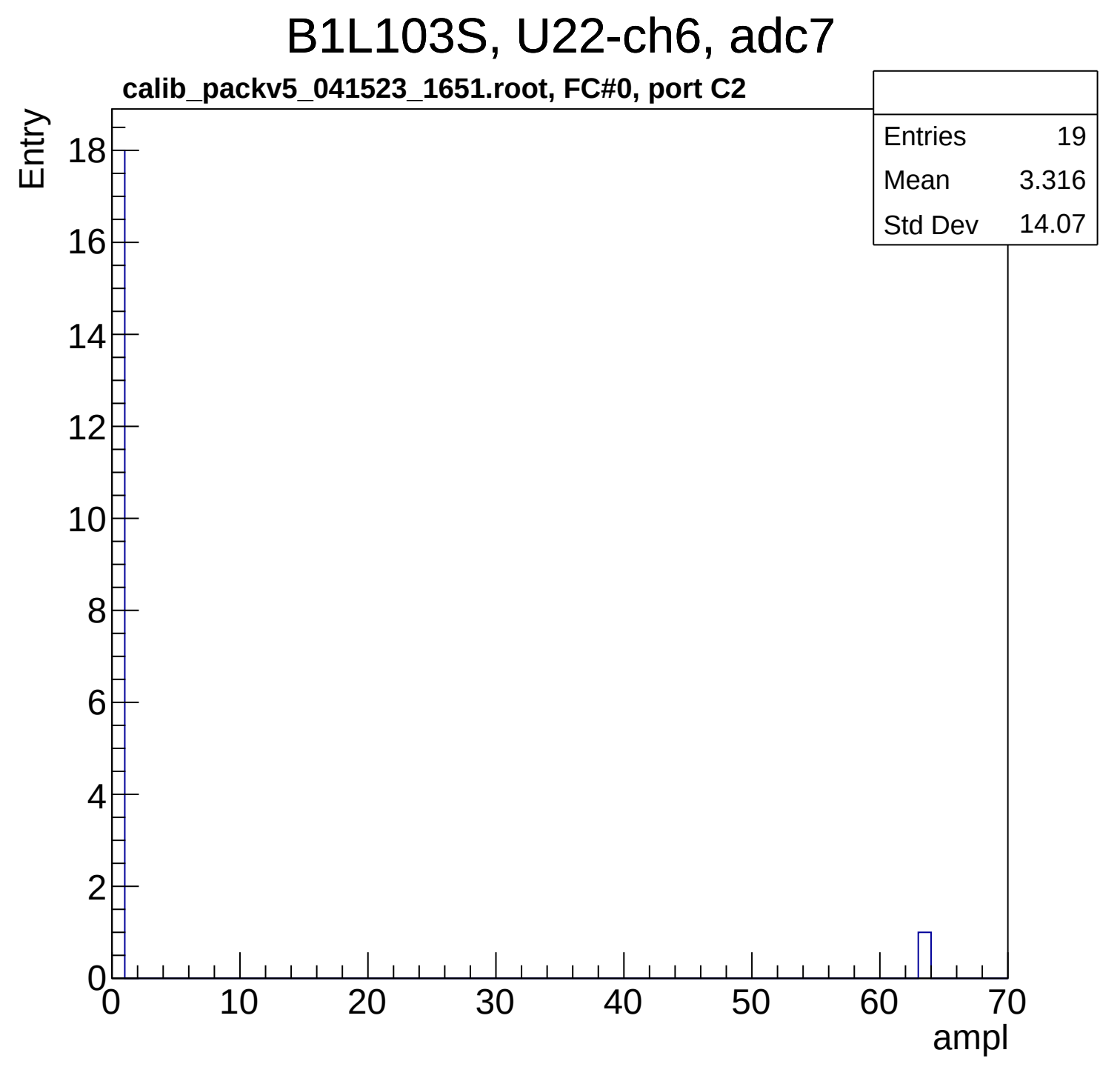
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U22-ch6, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.316
Std Dev 14.07
Entry
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6
8
10
12
14
16
18
0
10
20
30
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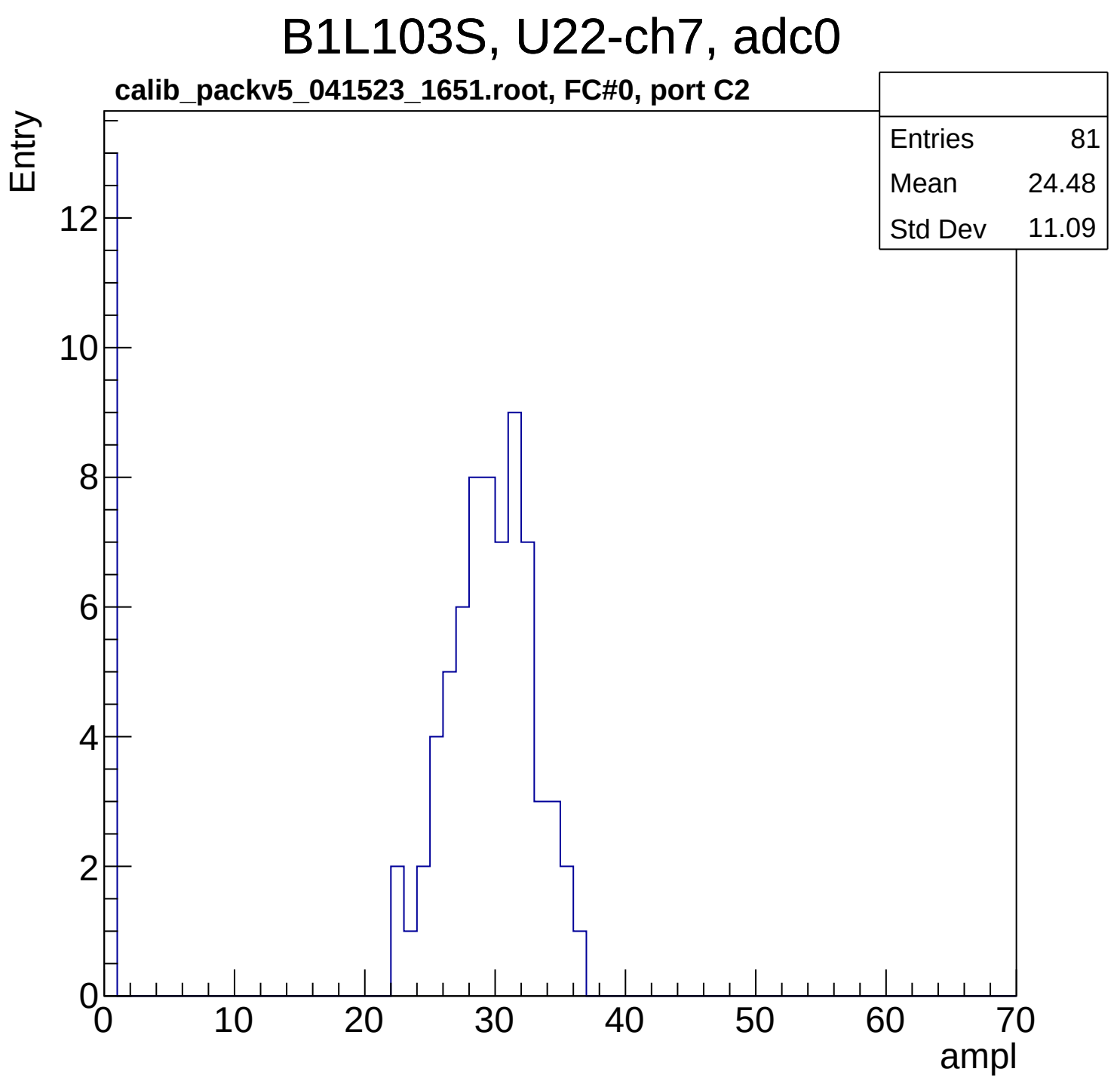
50
60
70
ampl


B1L103S, U22-ch7, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 24.48
Std Dev 11.09
Entry
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8
10
12
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10
20
30
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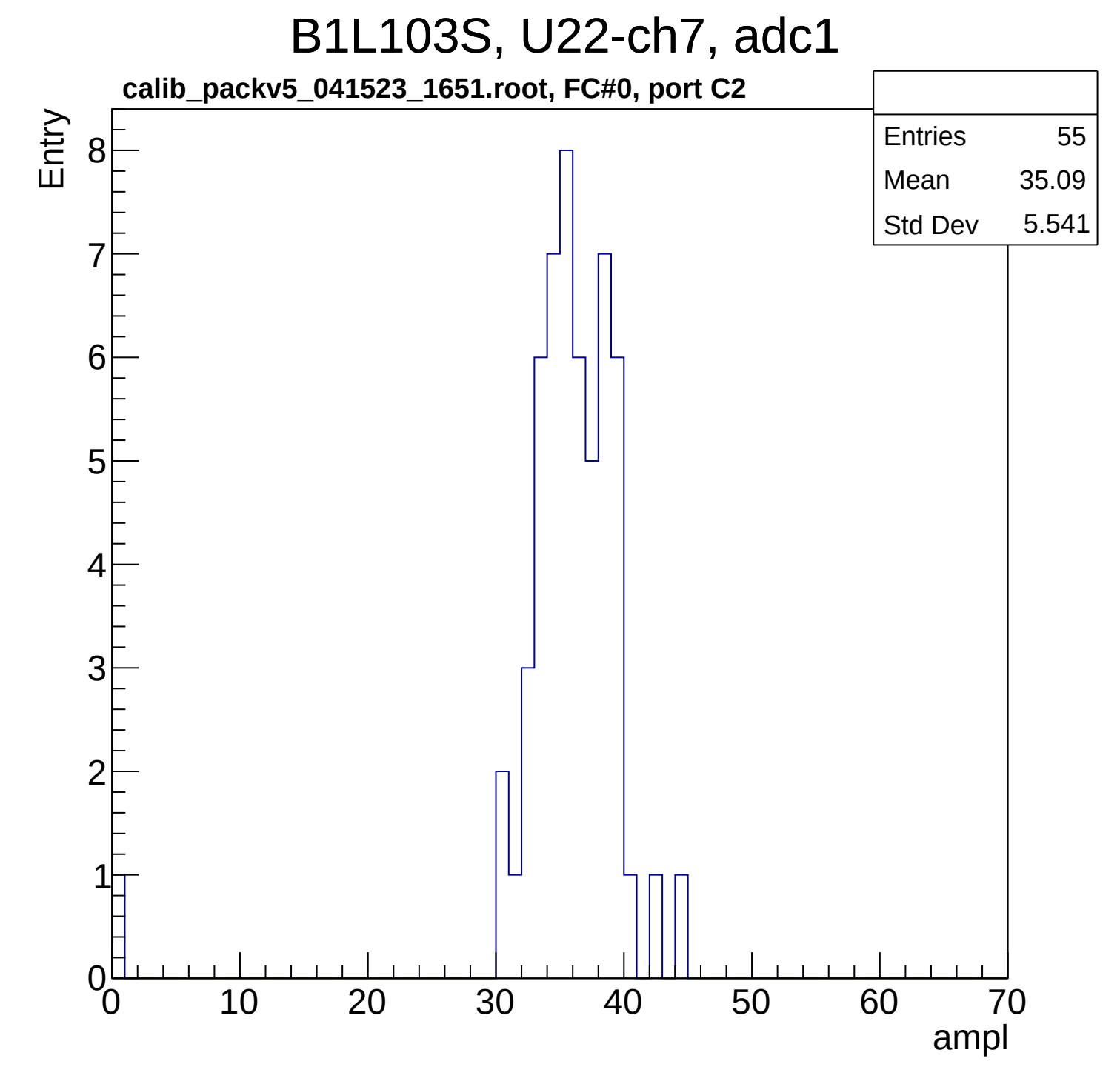
50
60
70
ampl


B1L103S, U22-ch7, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 35.09
Std Dev 5.541
Entry
ampl
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2
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4
5
6
7
8
0
10
20
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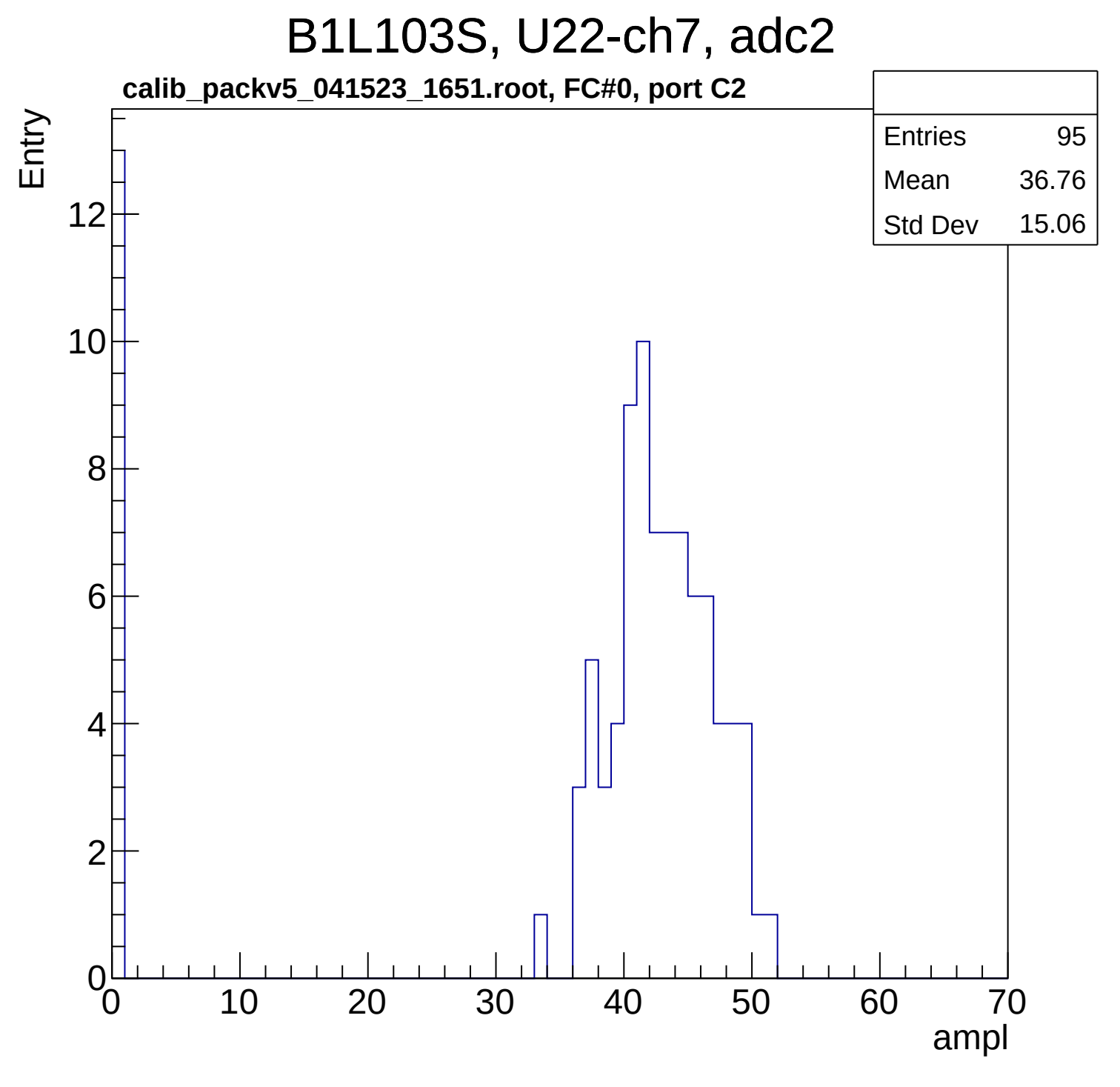
40
50
60
70


B1L103S, U22-ch7, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 36.76
Std Dev 15.06
Entry
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4
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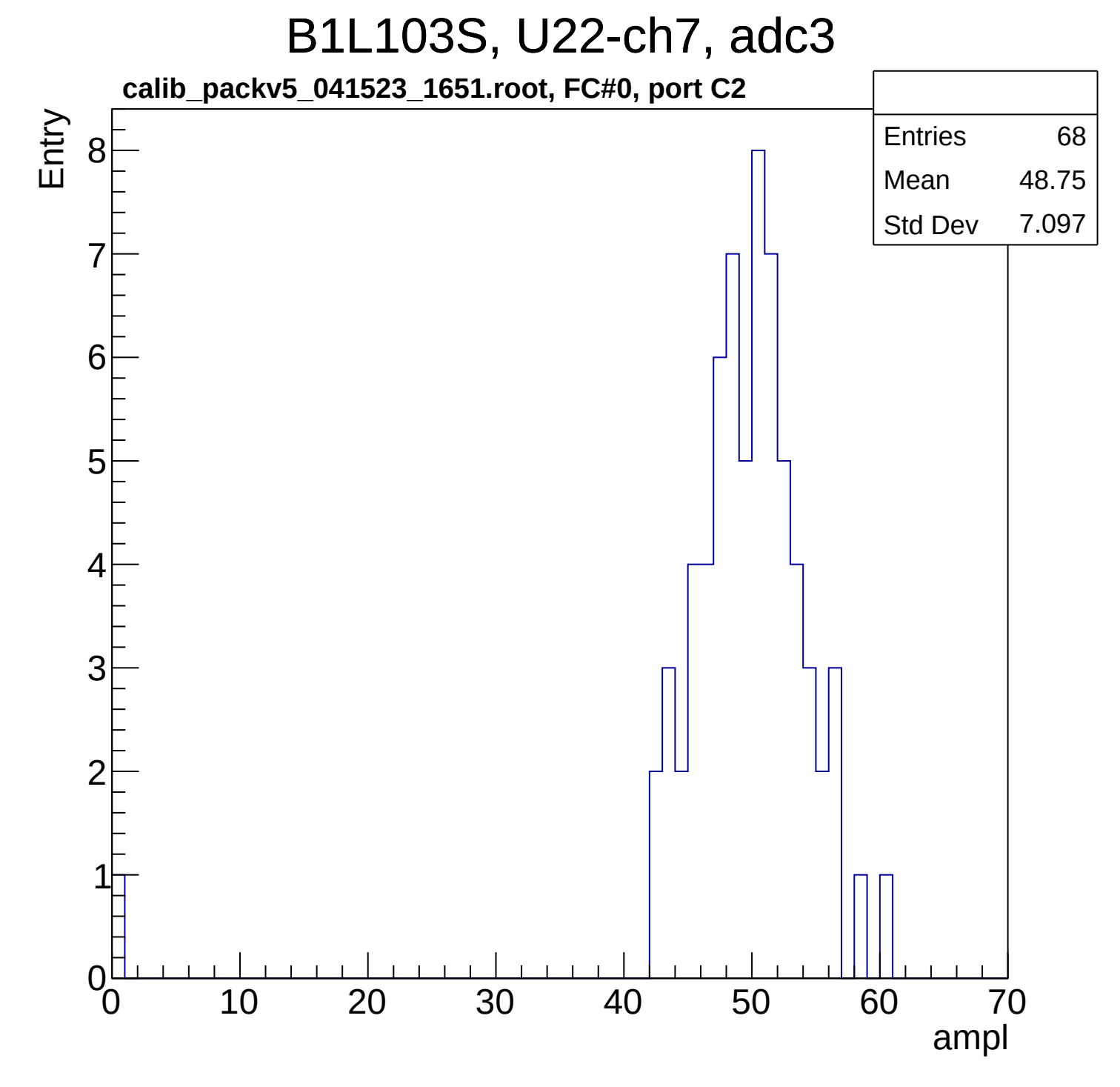
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch7, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 48.75
Std Dev 7.097
Entry
ampl
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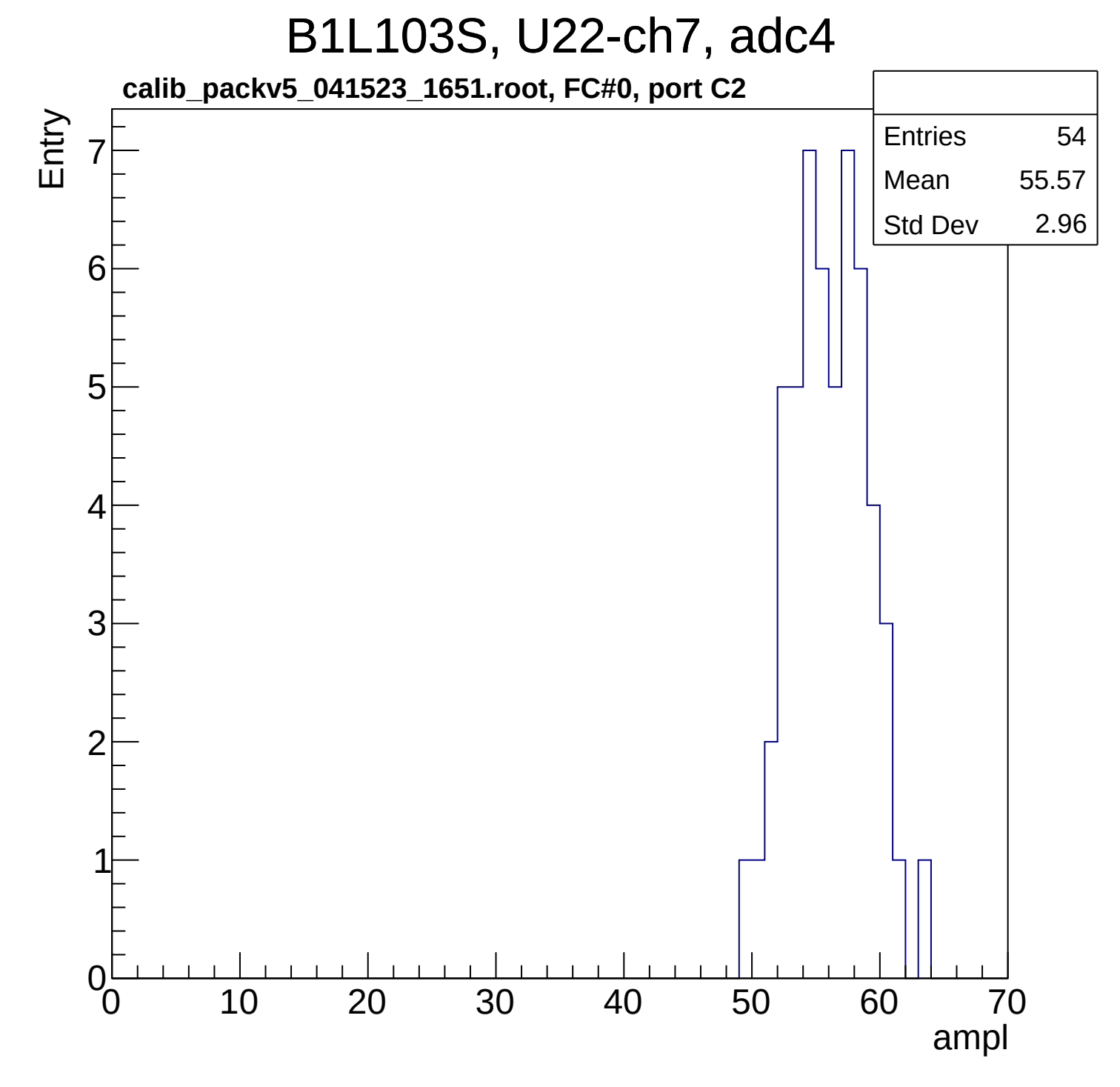
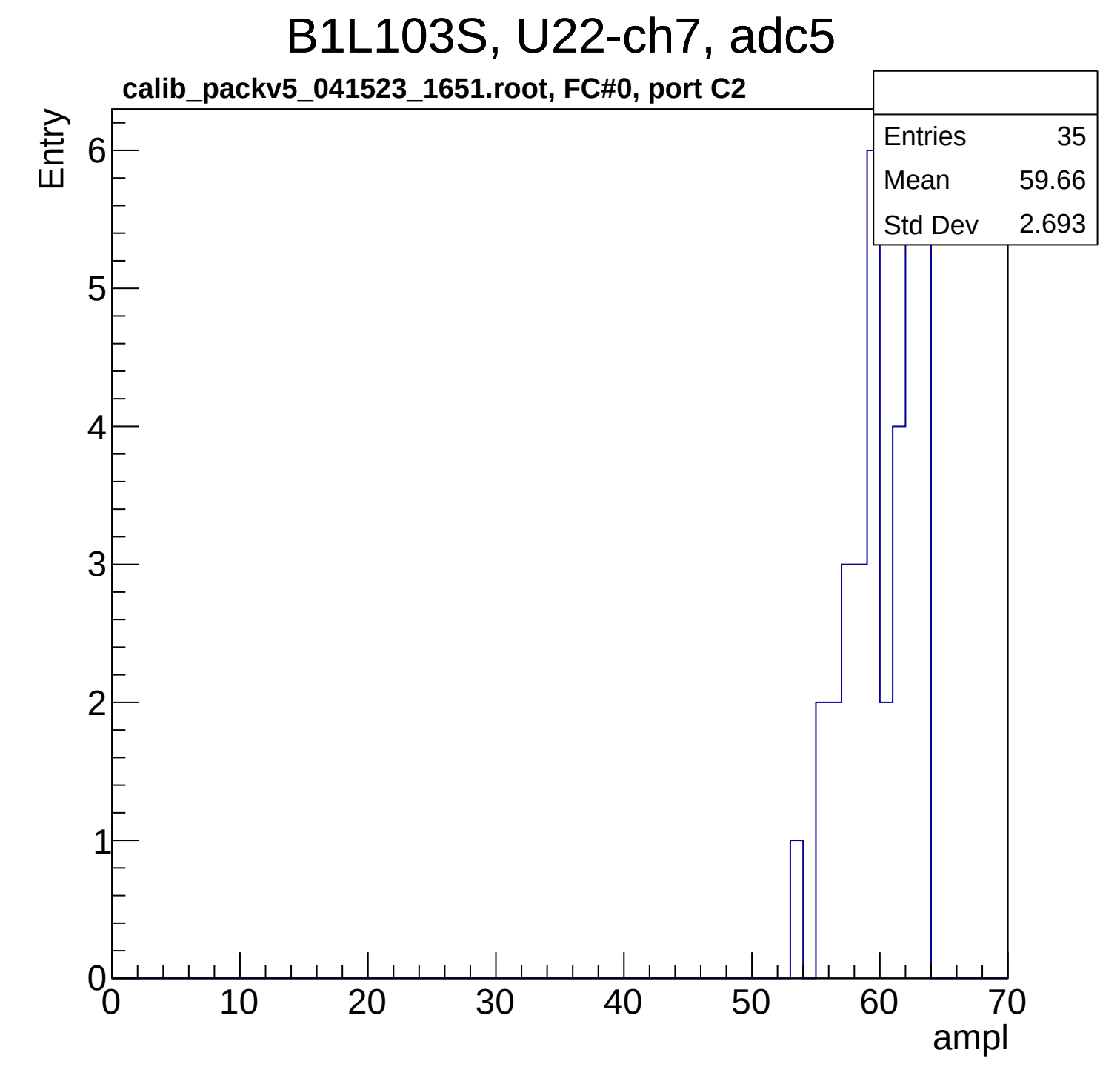
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch7, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 55.57
Std Dev 2.96
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U22-ch7, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 59.66
Std Dev 2.693
Entry
ampl
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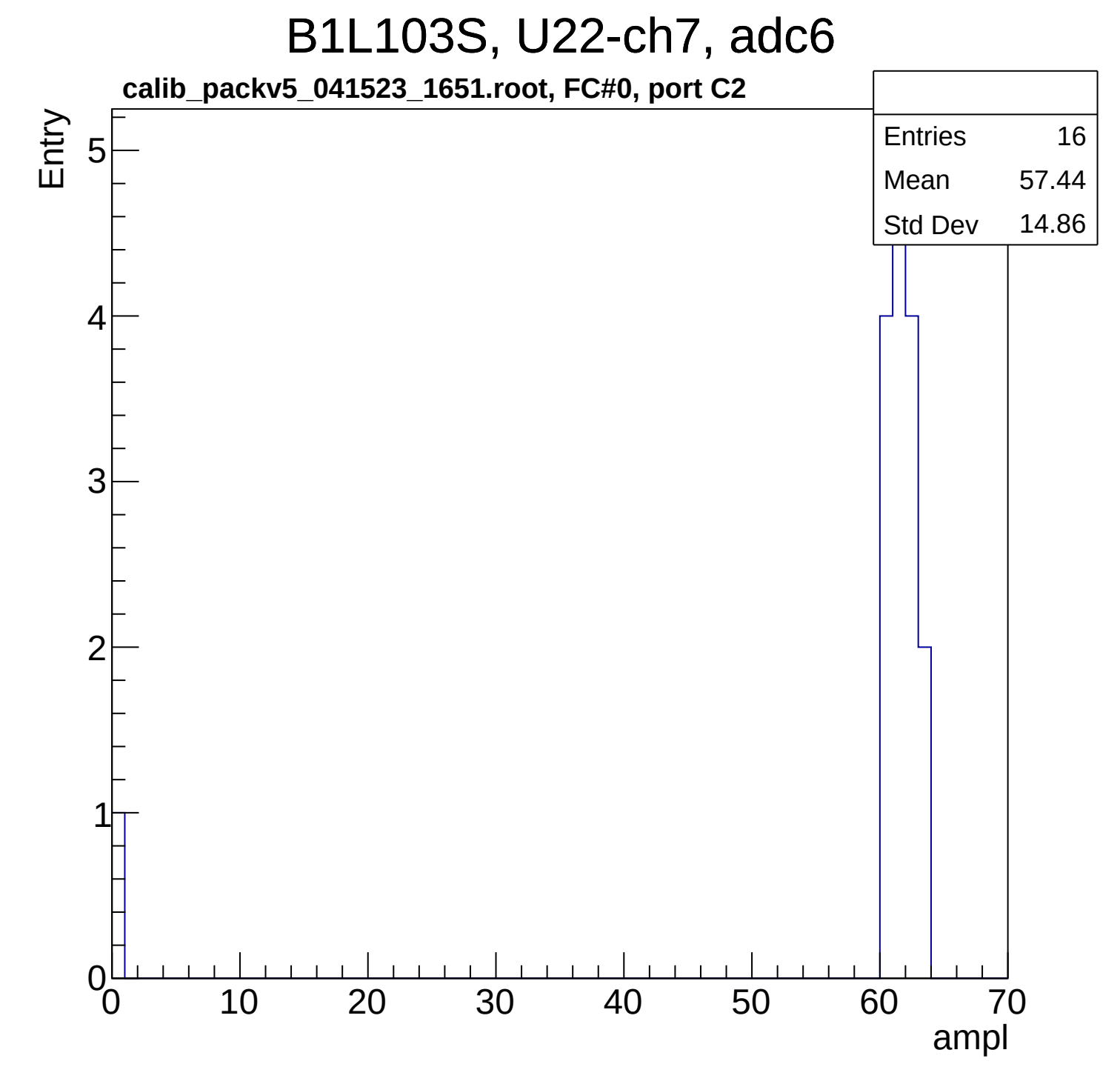
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U22-ch7, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 57.44
Std Dev 14.86
Entry
ampl
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4
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0
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60
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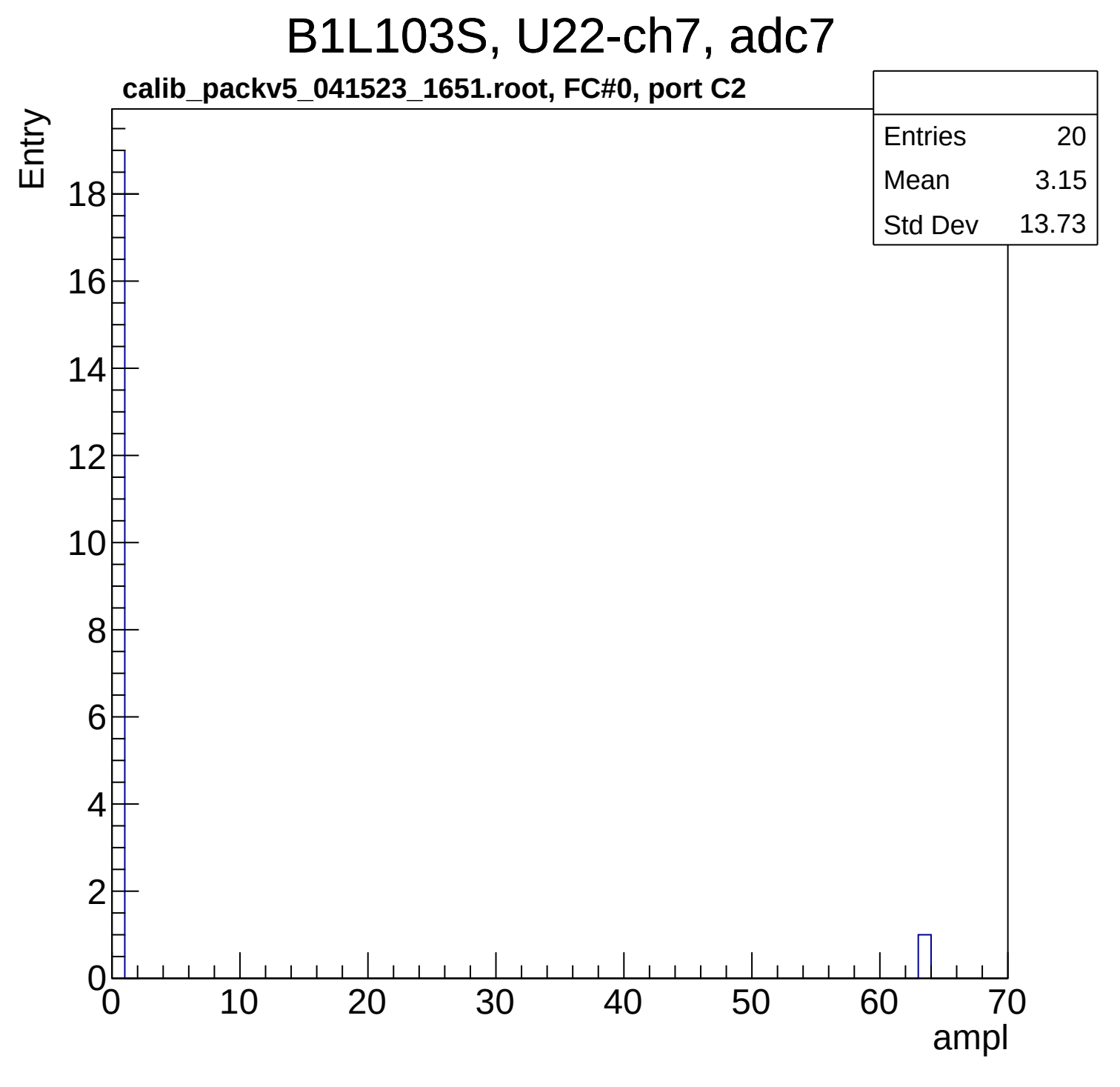
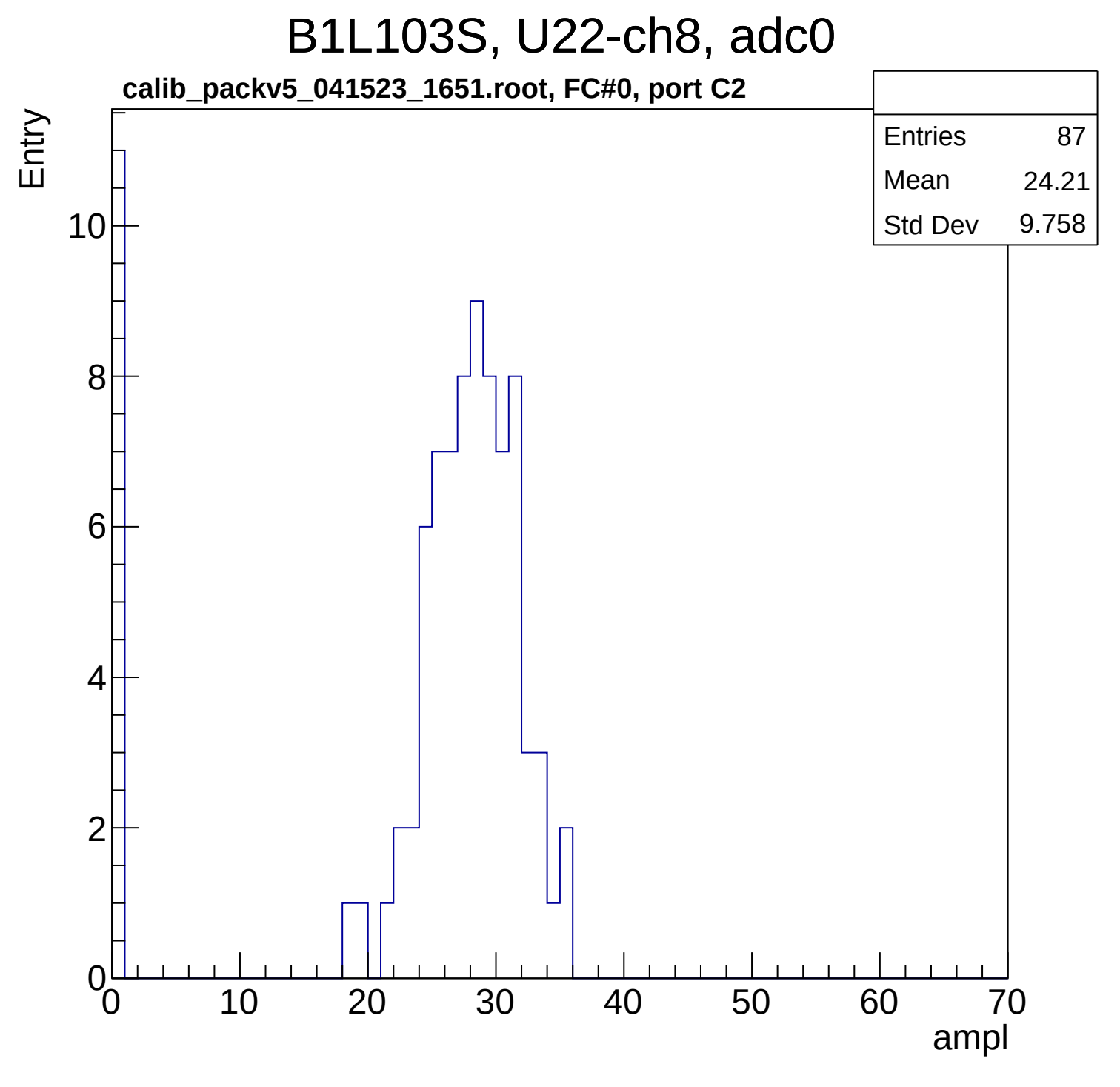

B1L103S, U22-ch7, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch8, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 24.21
Std Dev 9.758
Entry
ampl
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2
4
6
8
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0
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40
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60
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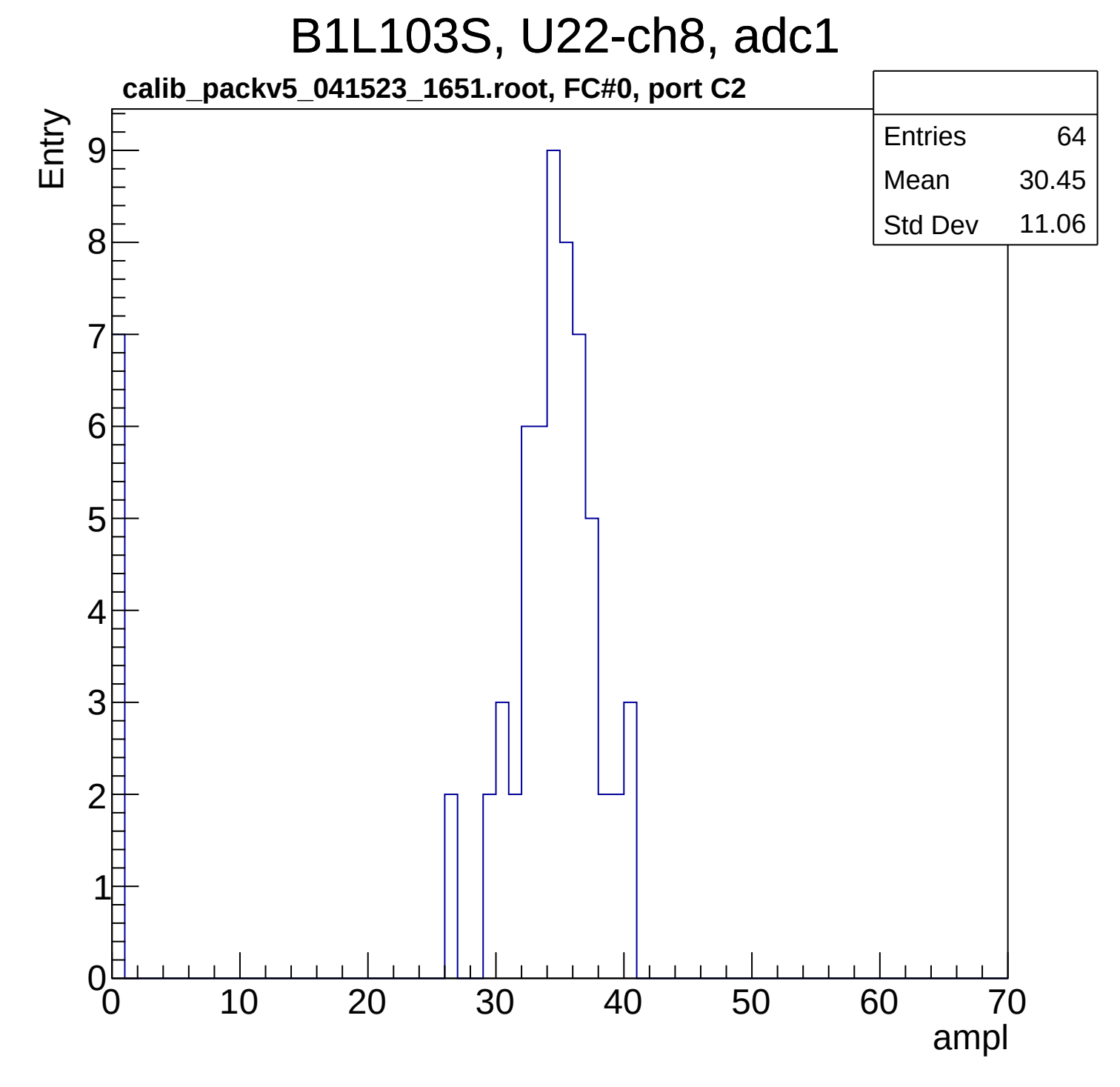
B1L103S, U22-ch8, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 30.45
Std Dev 11.06
Entry
ampl
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4
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6
7
8
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0
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40
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60
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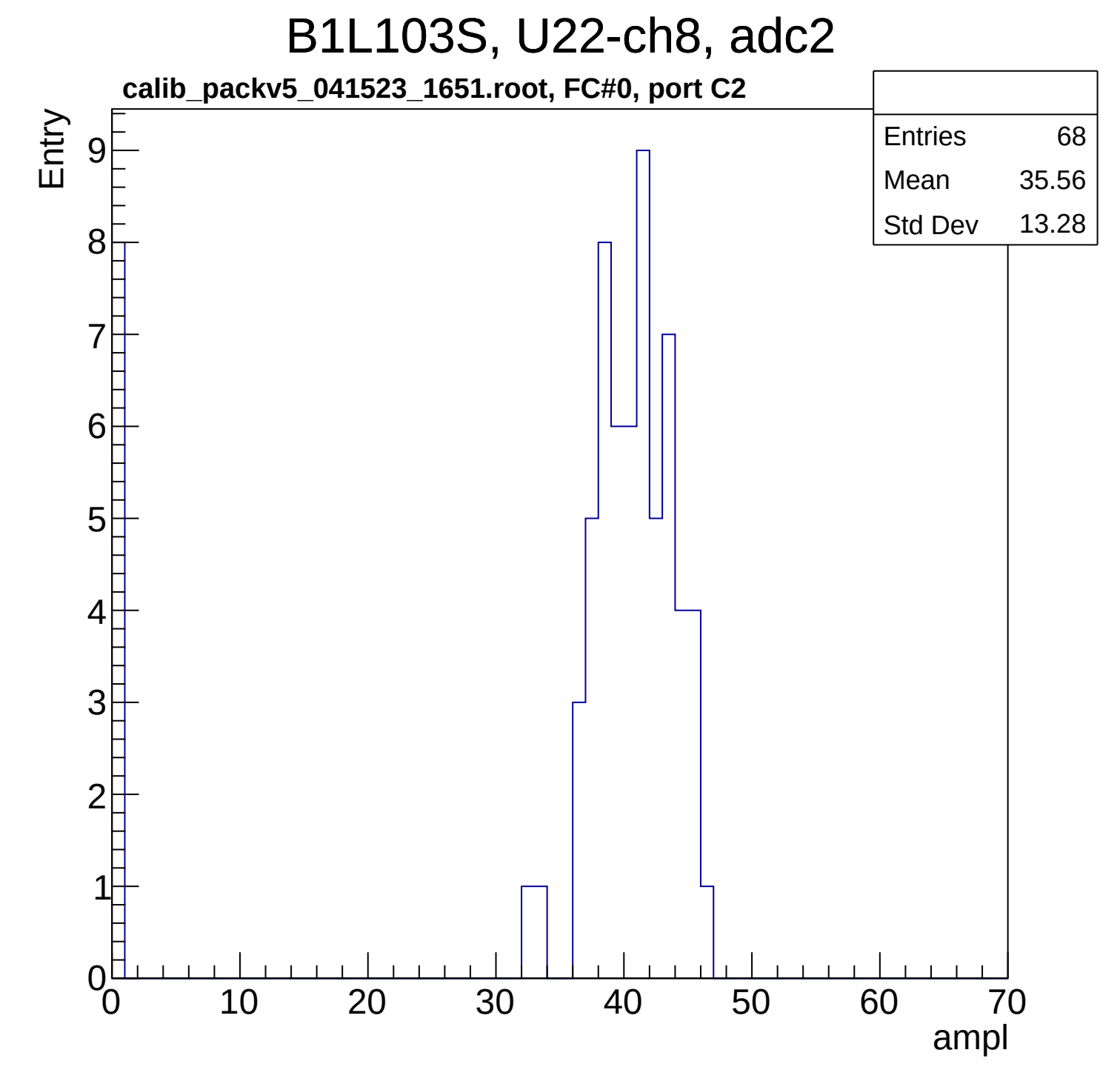
B1L103S, U22-ch8, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 35.56
Std Dev 13.28
Entry
ampl
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2
3
4
5
6
7
8
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0
10
20
30
40
50
60
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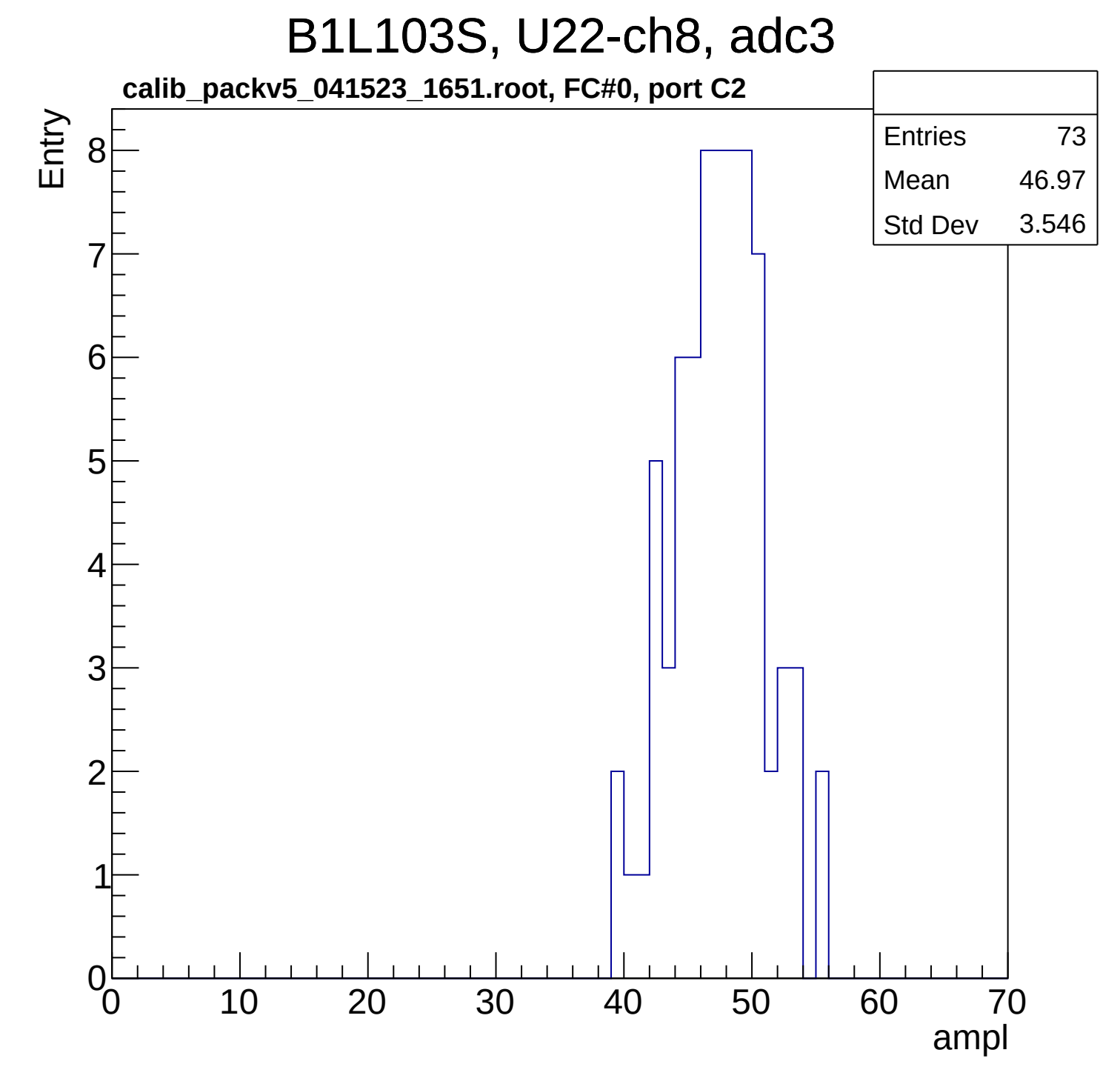
B1L103S, U22-ch8, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 46.97
Std Dev 3.546
Entry
ampl
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5
6
7
8
0
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20
30
40
50
60
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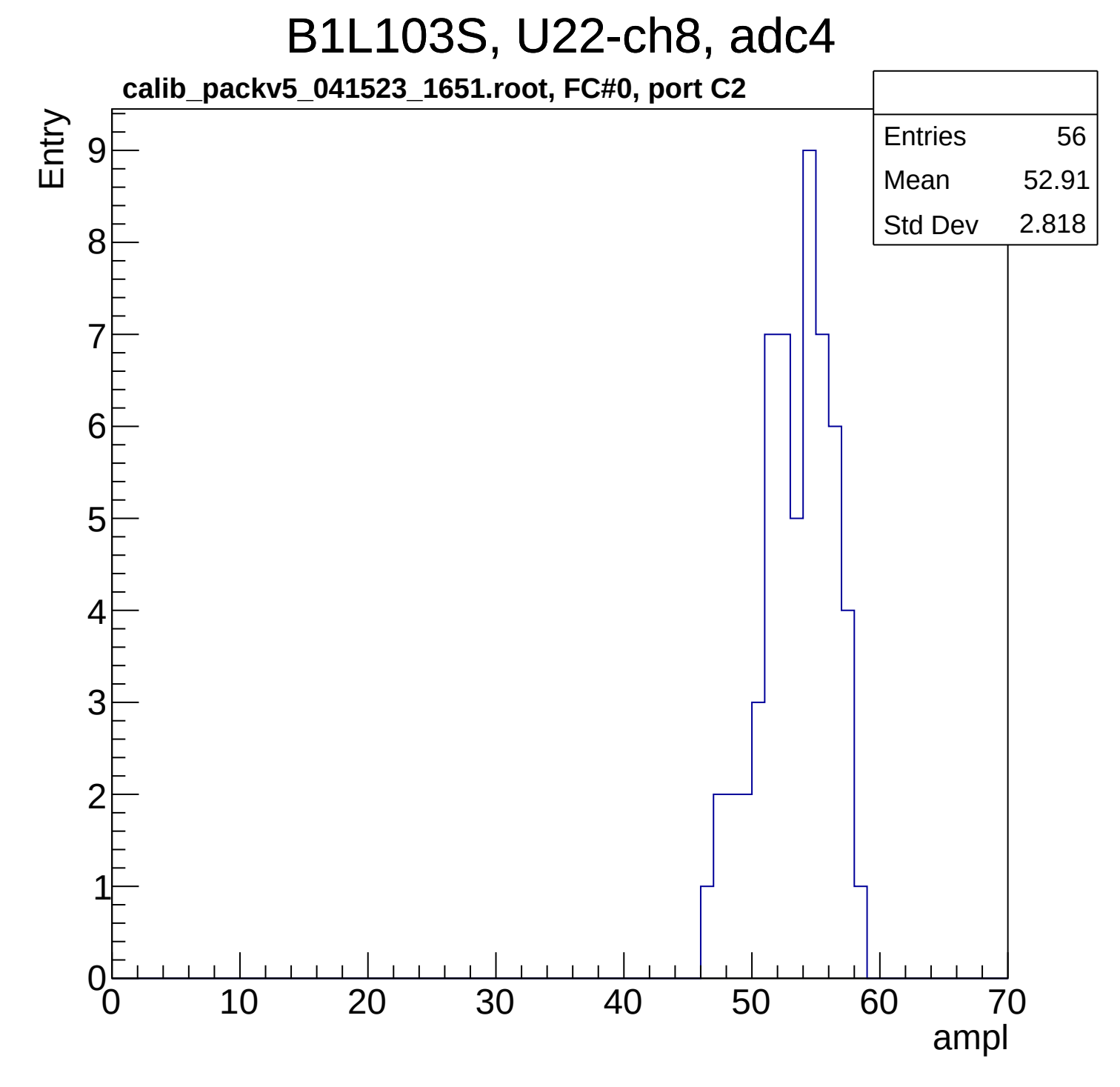
B1L103S, U22-ch8, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 52.91
Std Dev 2.818
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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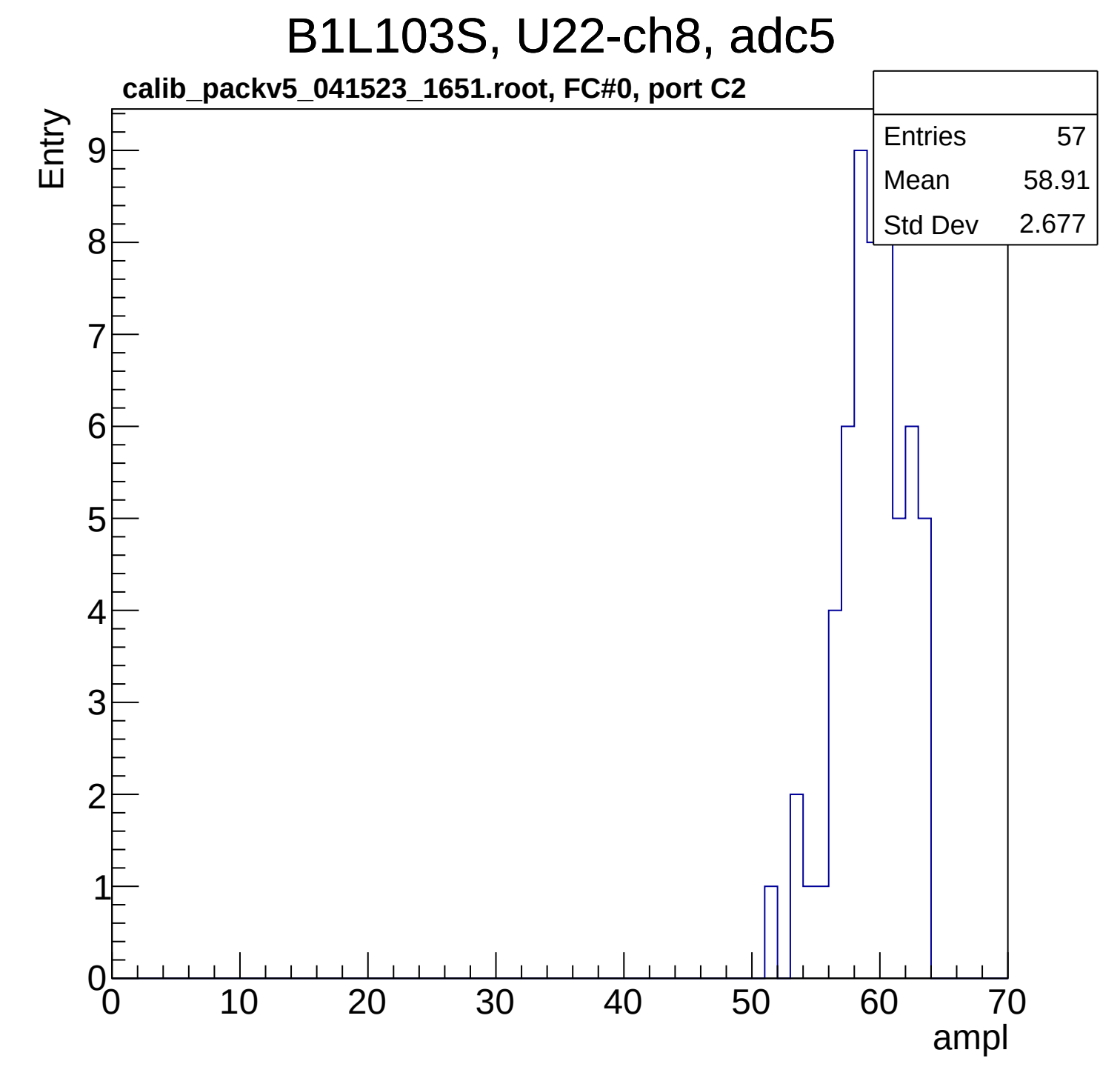
B1L103S, U22-ch8, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 58.91
Std Dev 2.677
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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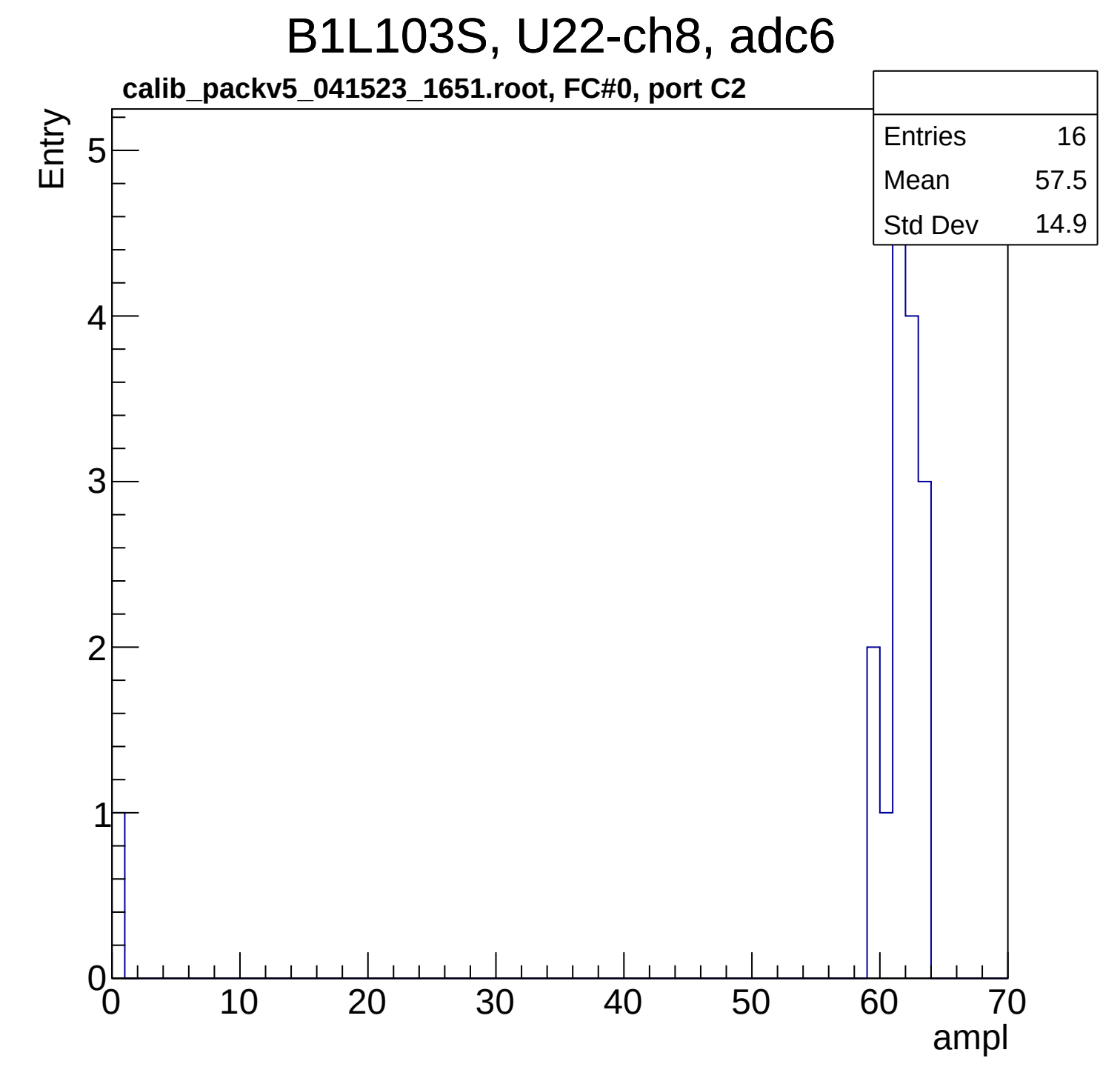
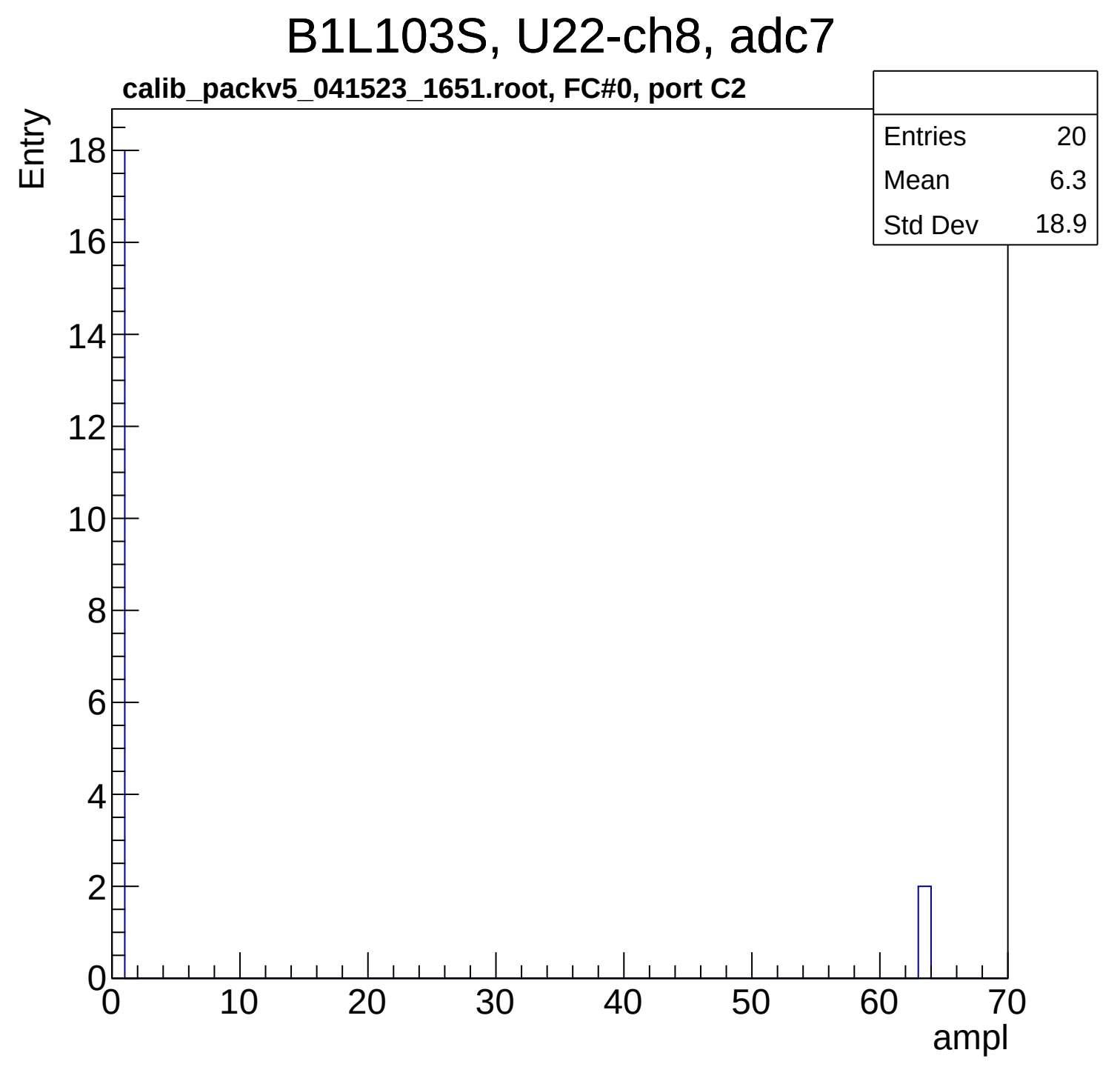
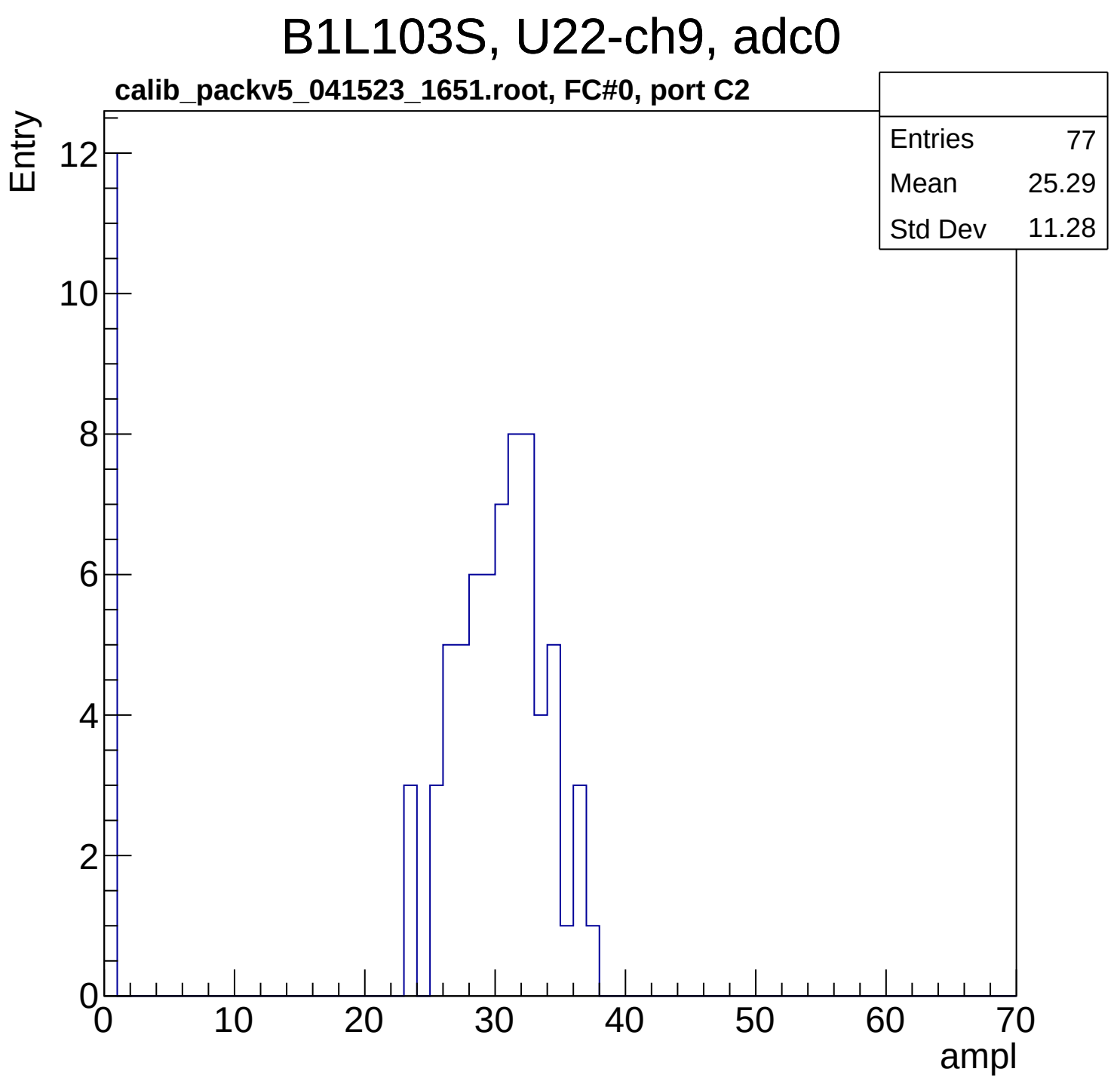
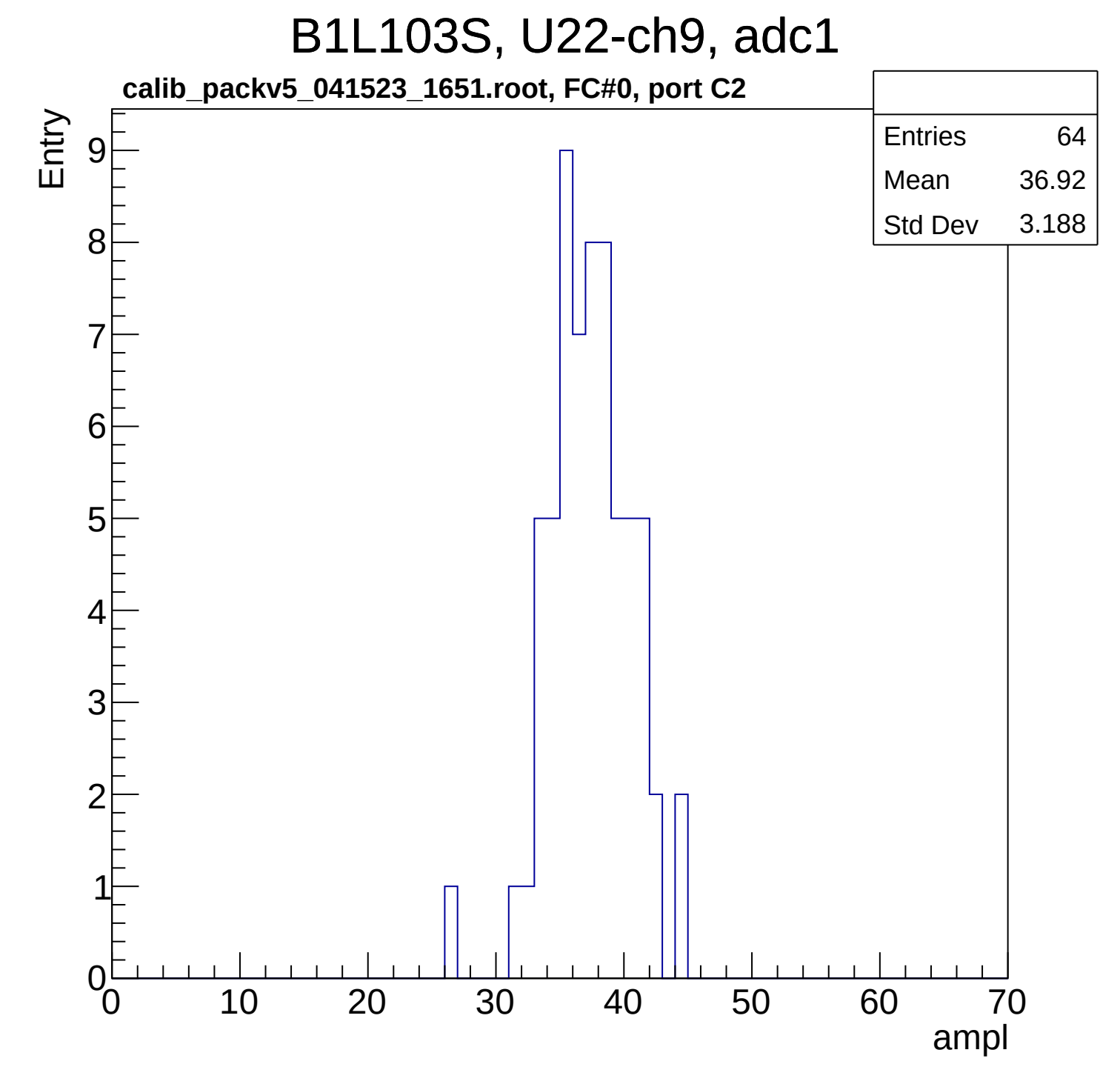
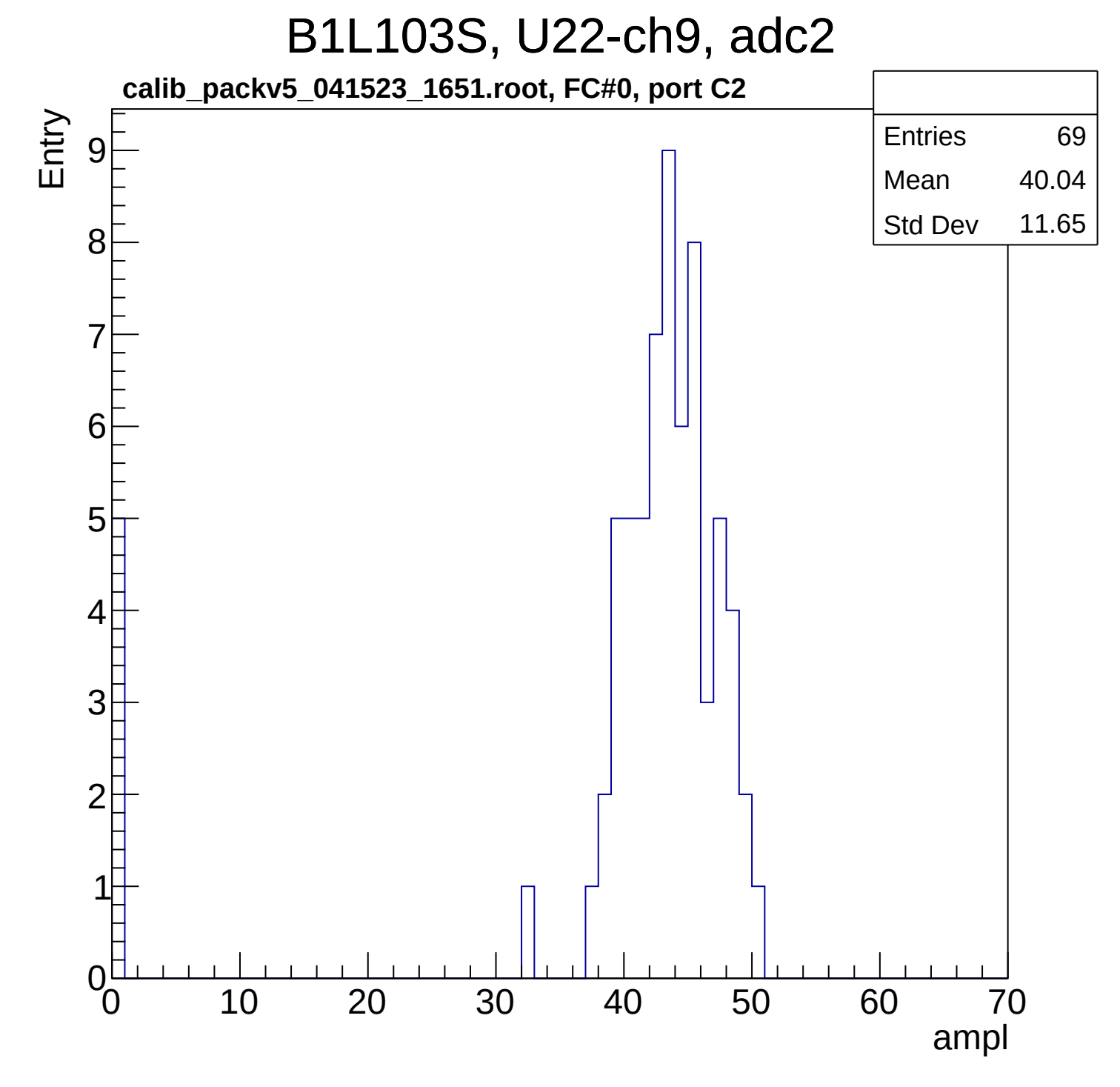
60
70


B1L103S, U22-ch8, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 57.5
Std Dev 14.9
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch8, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 6.3
Std Dev 18.9
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch9, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 25.29
Std Dev 11.28
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch9, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 36.92
Std Dev 3.188
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch9, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 40.04
Std Dev 11.65
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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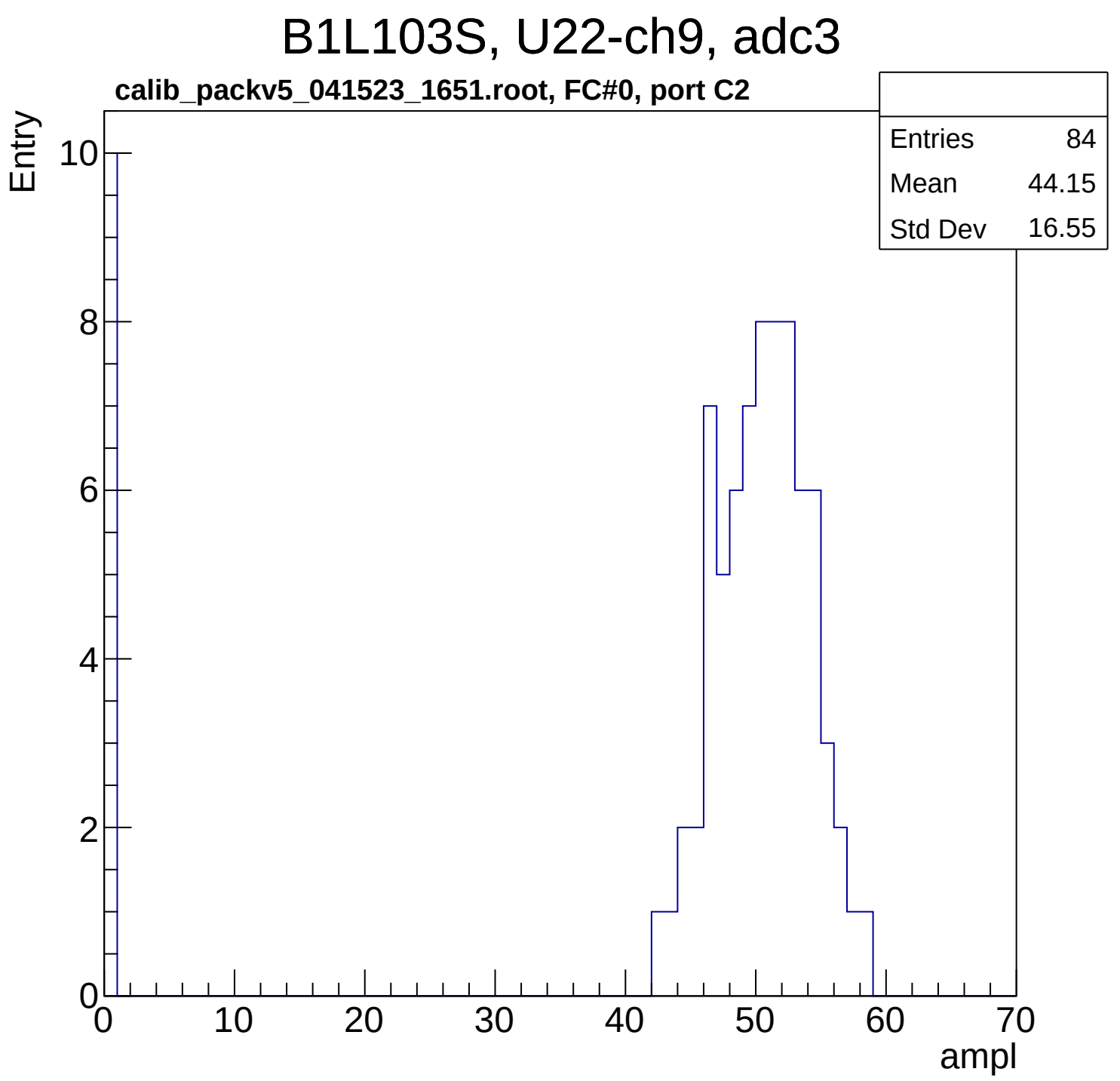
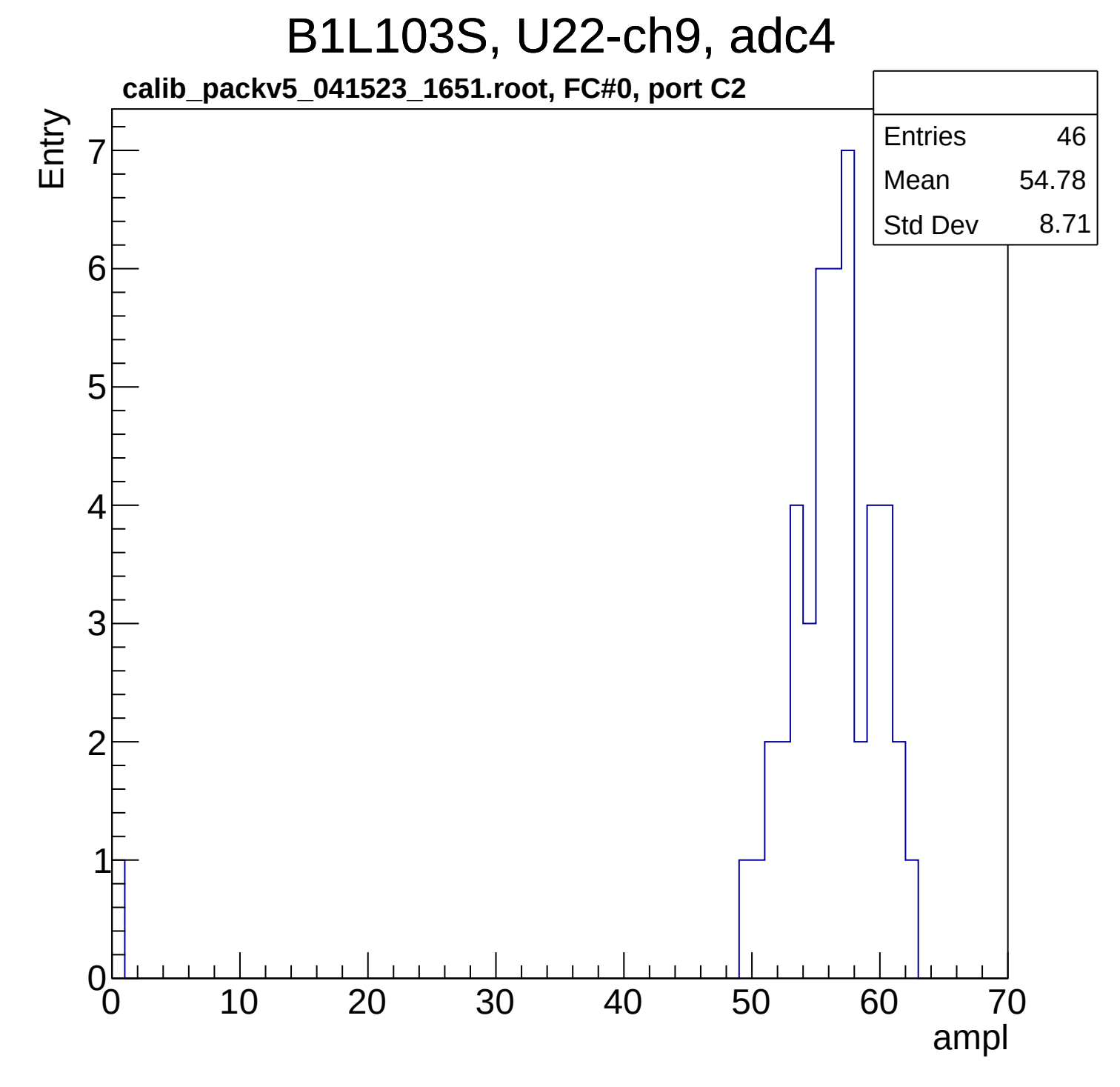
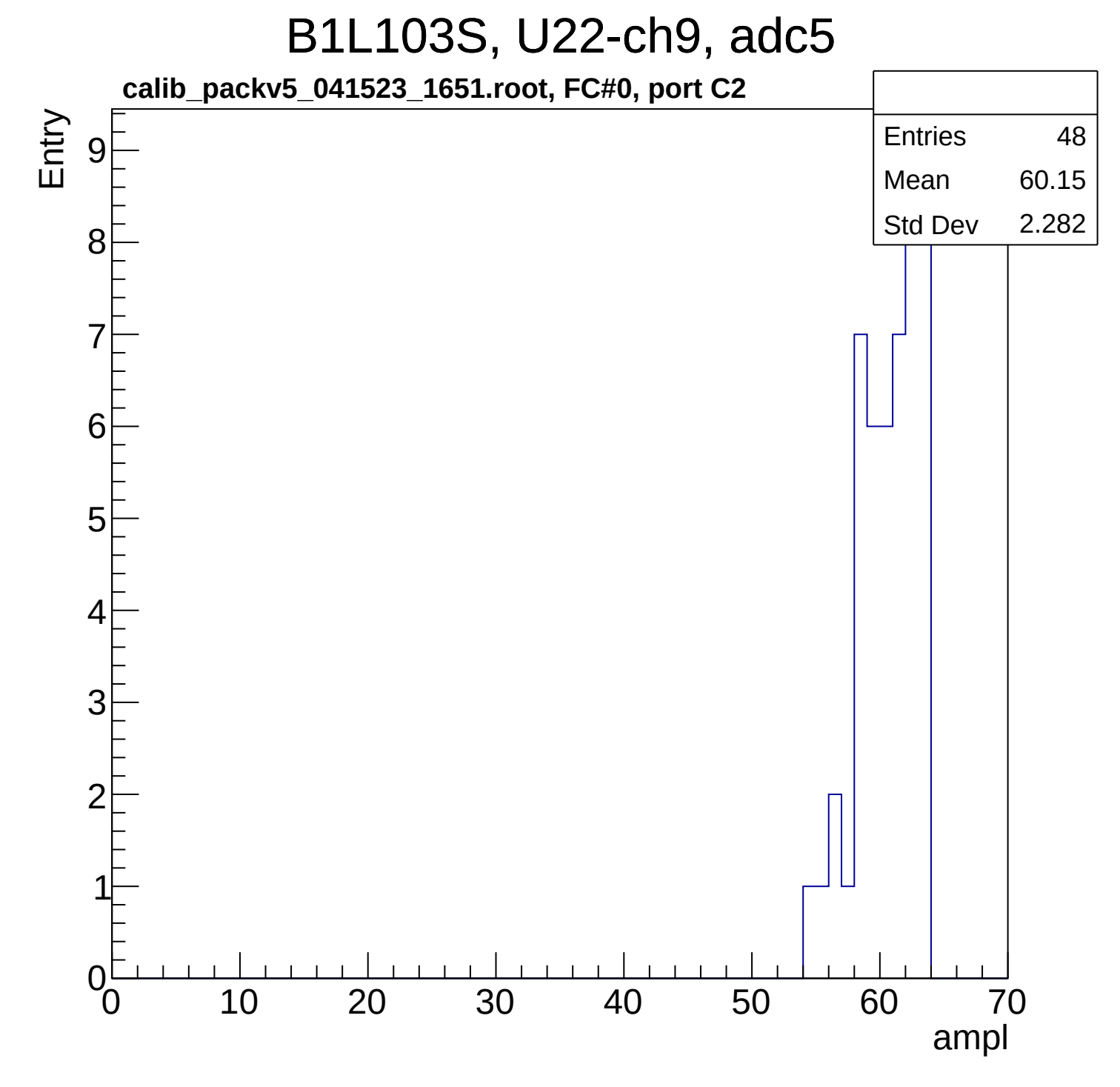
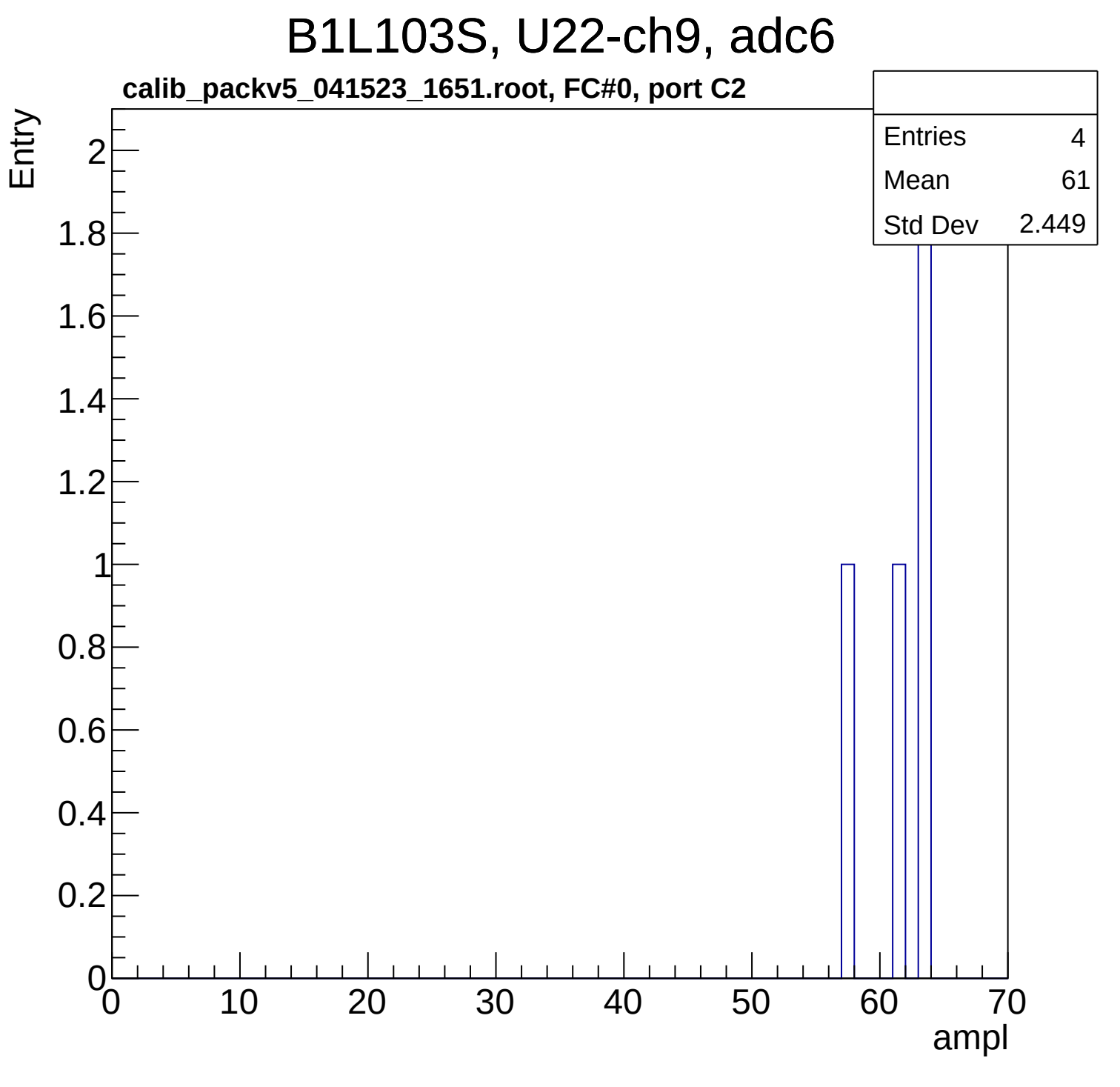

B1L103S, U22-ch9, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 44.15
Std Dev 16.55
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch9, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 54.78
Std Dev 8.71
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U22-ch9, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 60.15
Std Dev 2.282
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch9, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 61
Std Dev 2.449
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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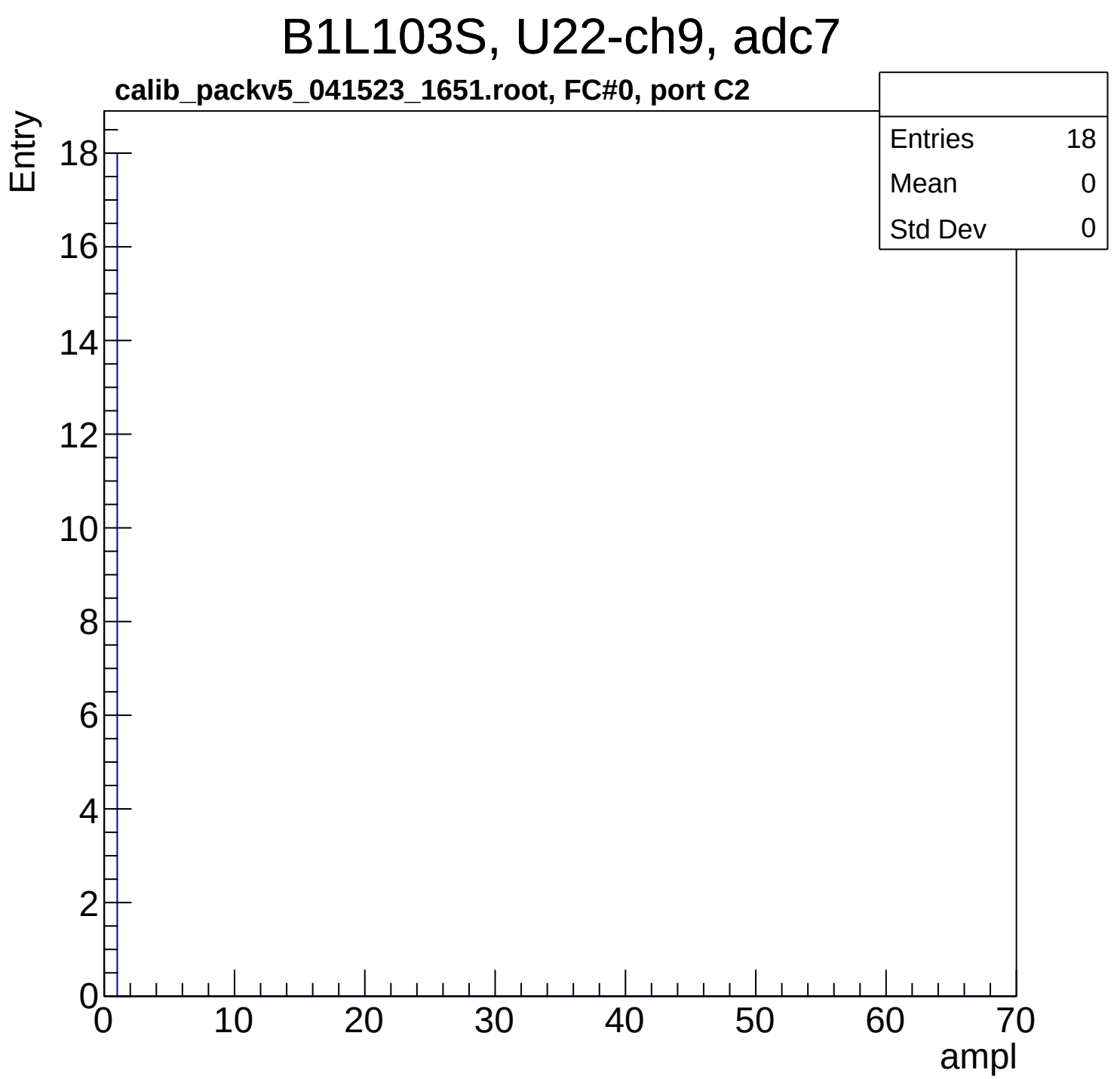
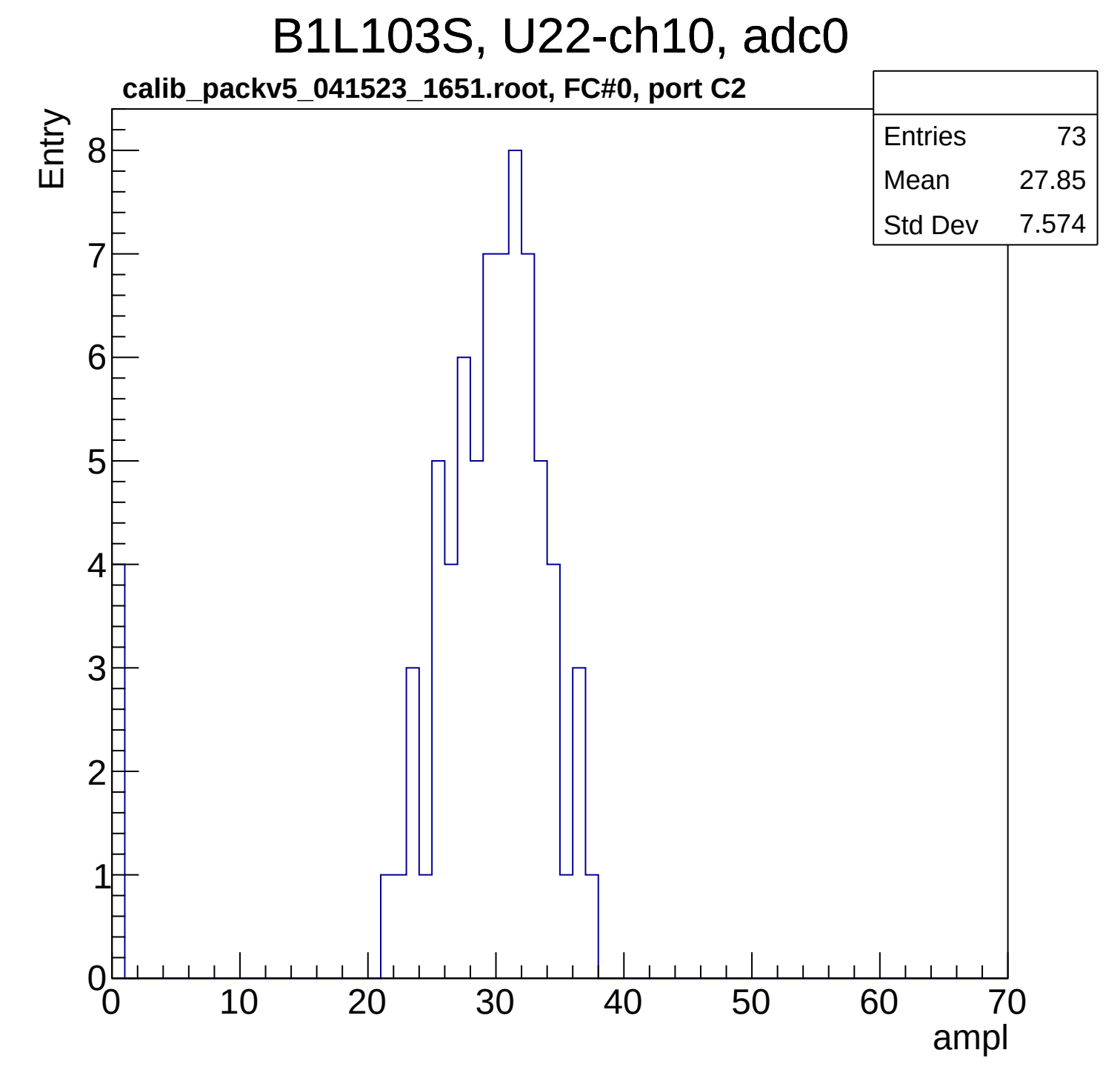

B1L103S, U22-ch9, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch10, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 27.85
Std Dev 7.574
Entry
ampl
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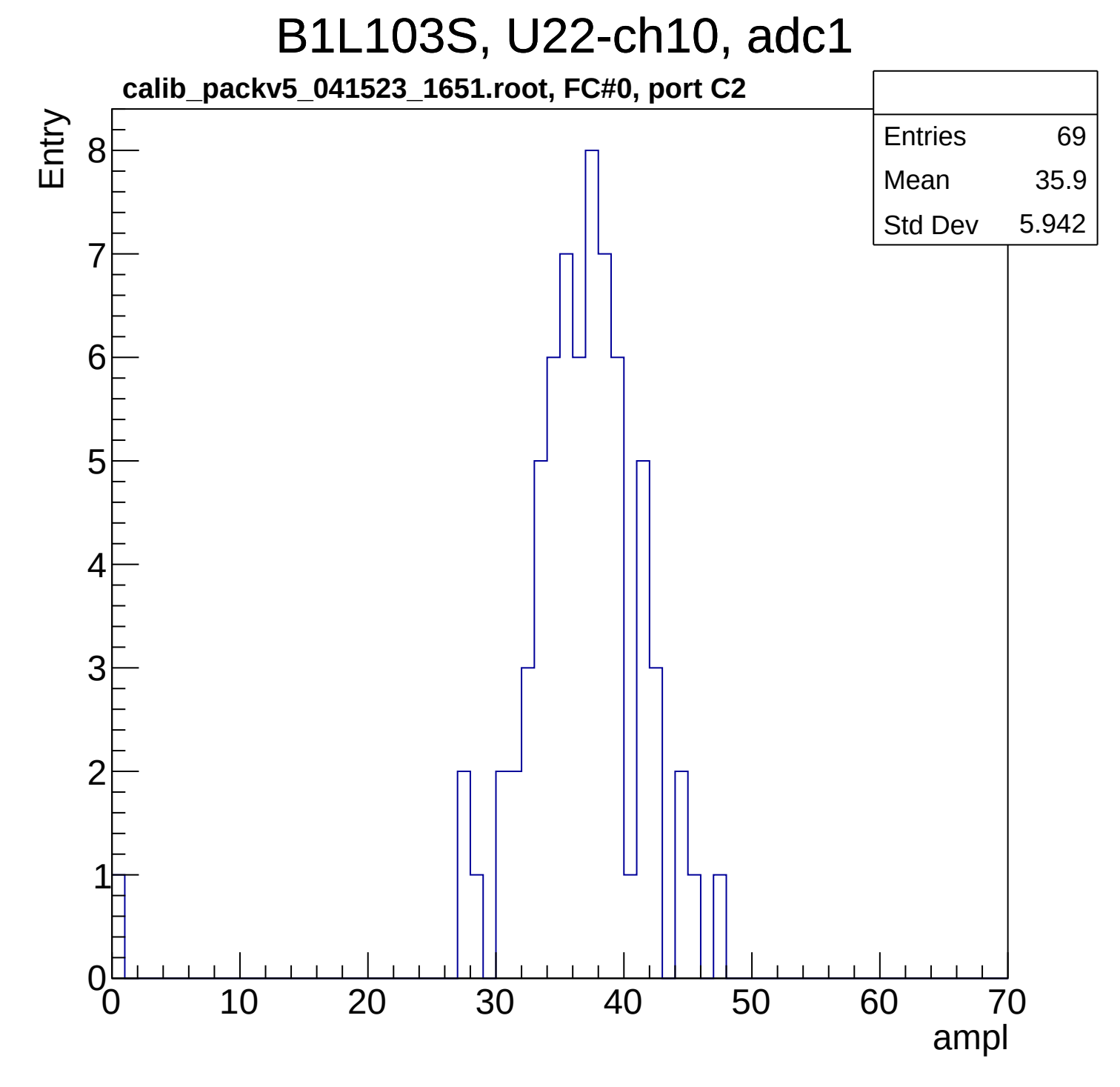
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch10, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 35.9
Std Dev 5.942
Entry
ampl
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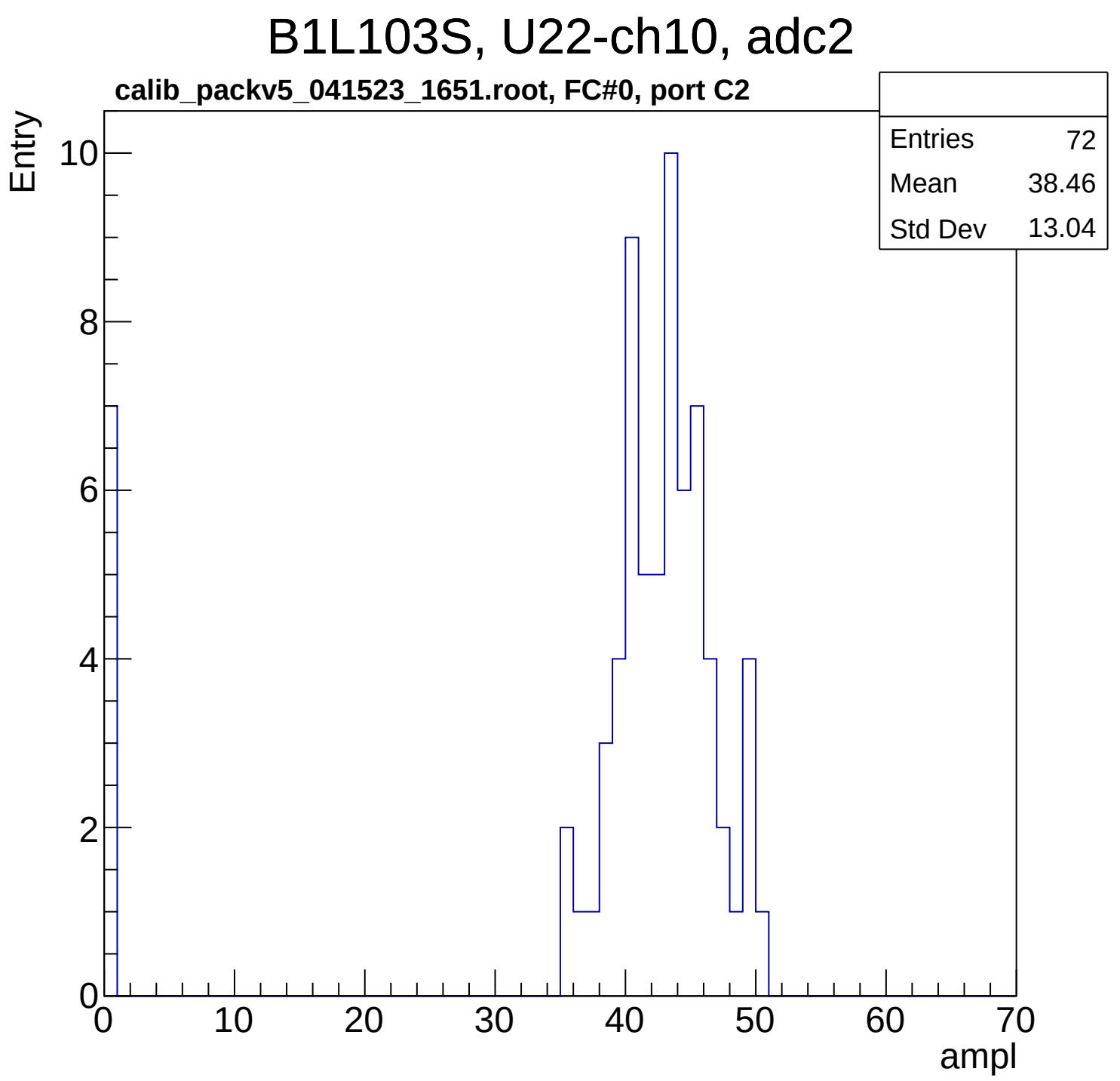
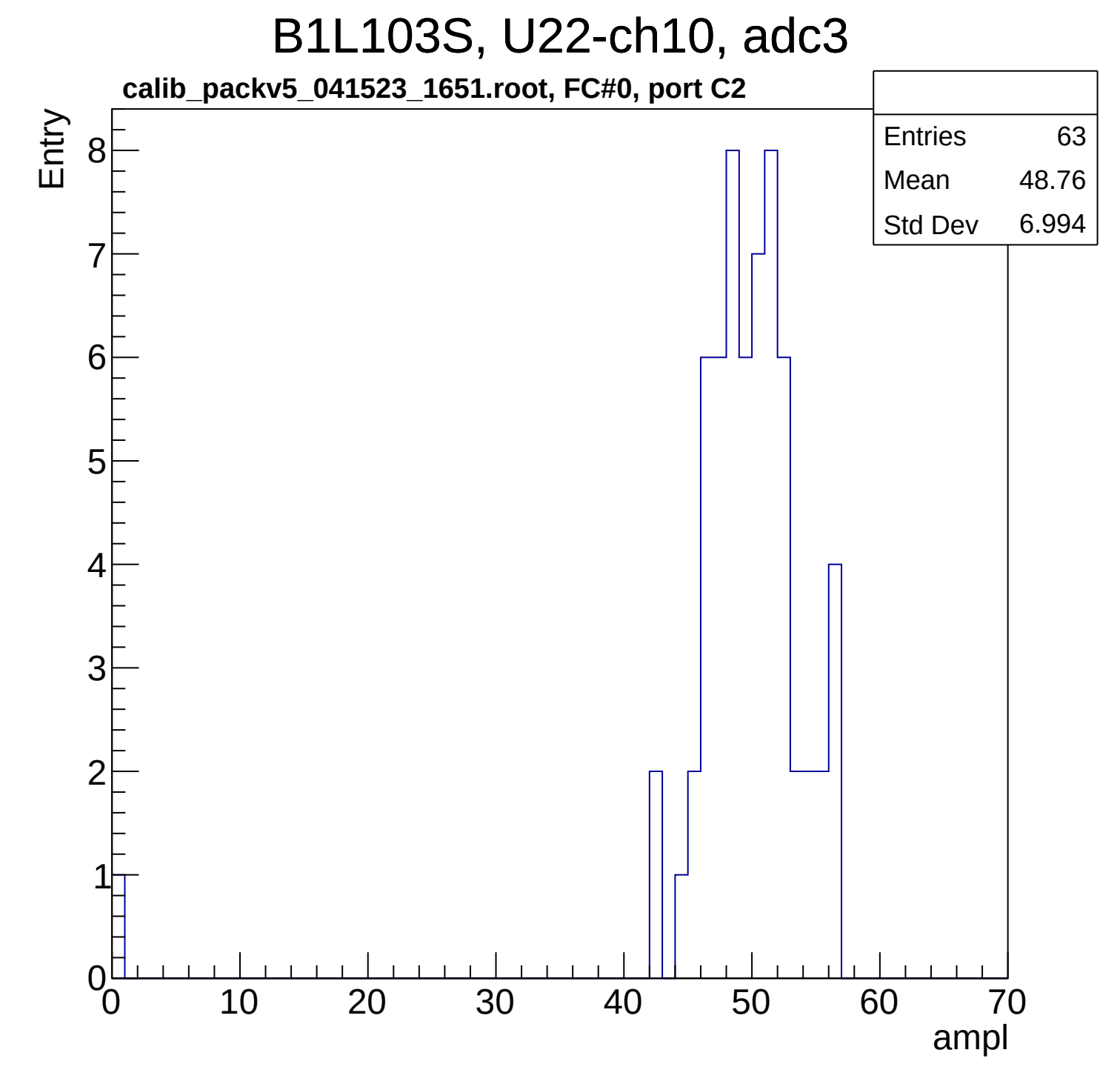
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch10, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 38.46
Std Dev 13.04
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U22-ch10, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 48.76
Std Dev 6.994
Entry
ampl
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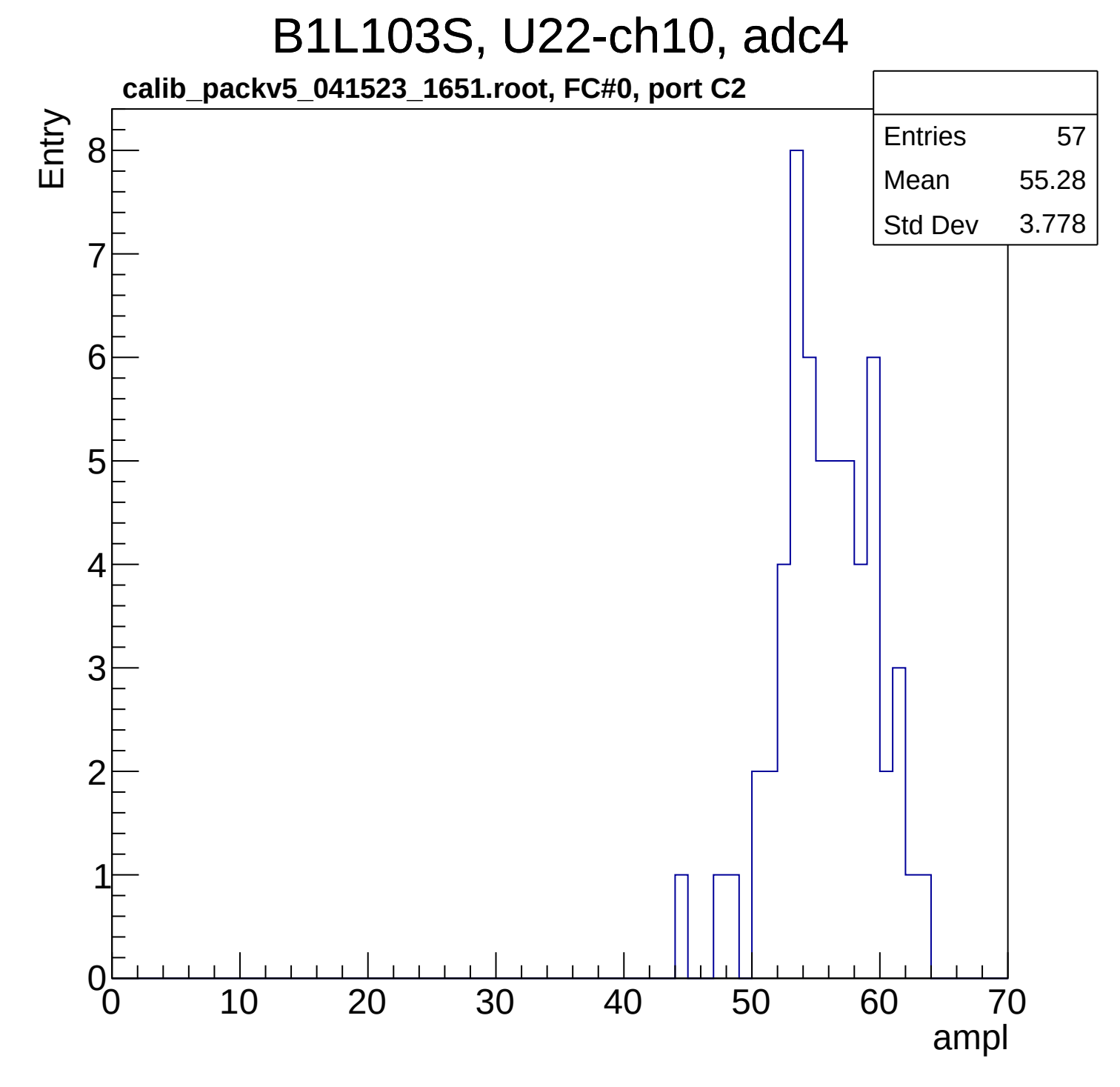
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch10, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 55.28
Std Dev 3.778
Entry
ampl
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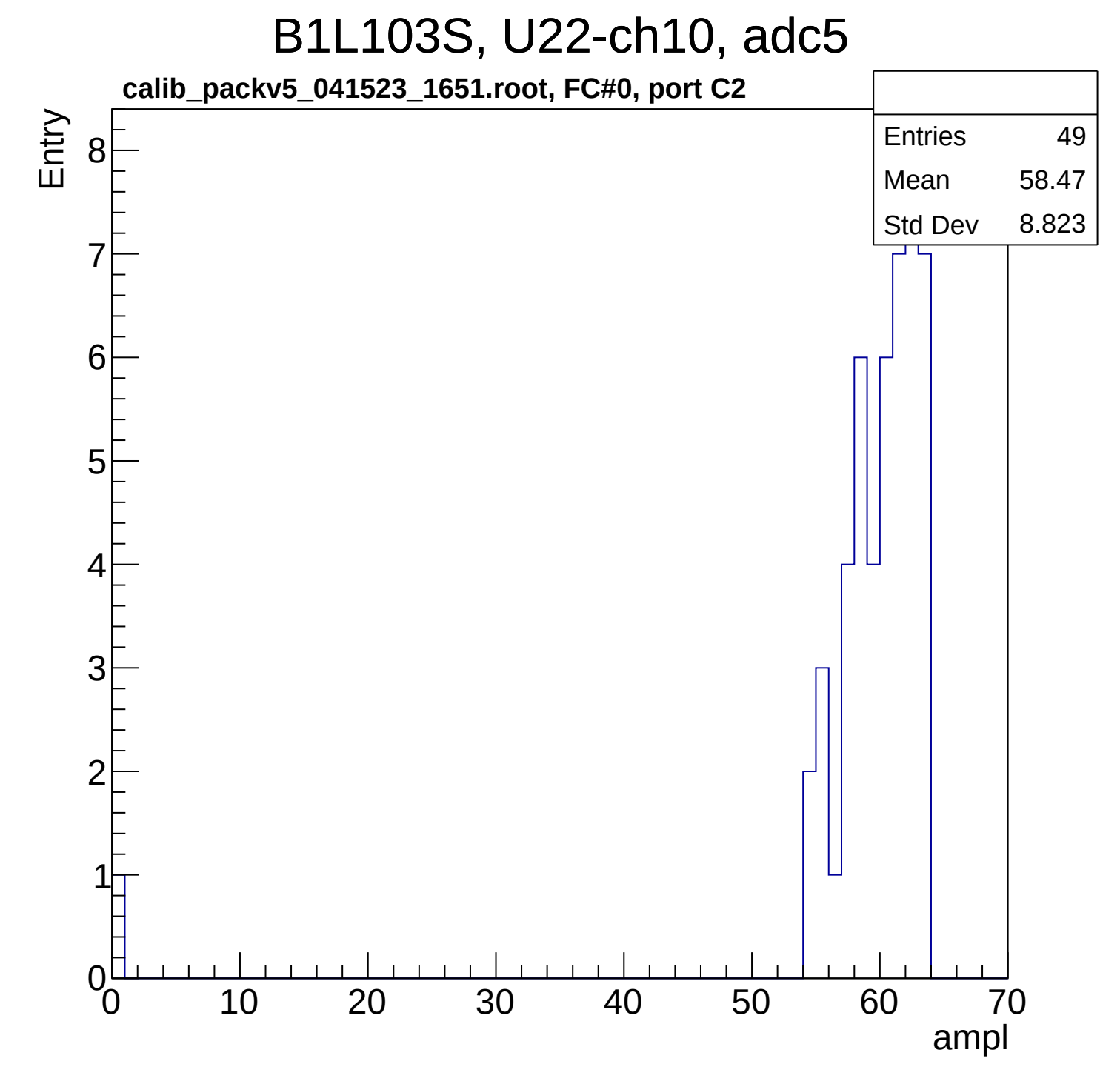
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch10, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 58.47
Std Dev 8.823
Entry
ampl
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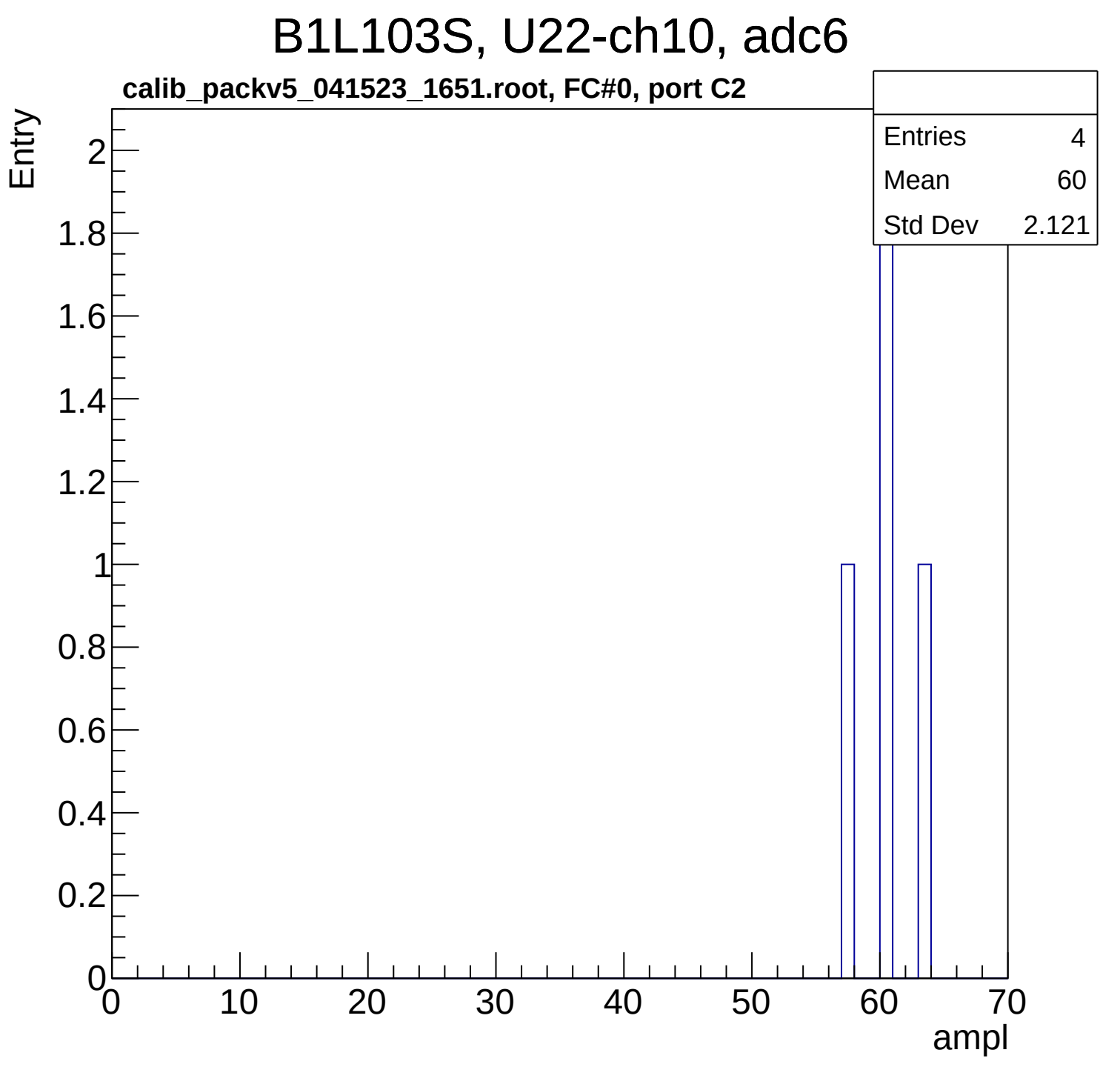
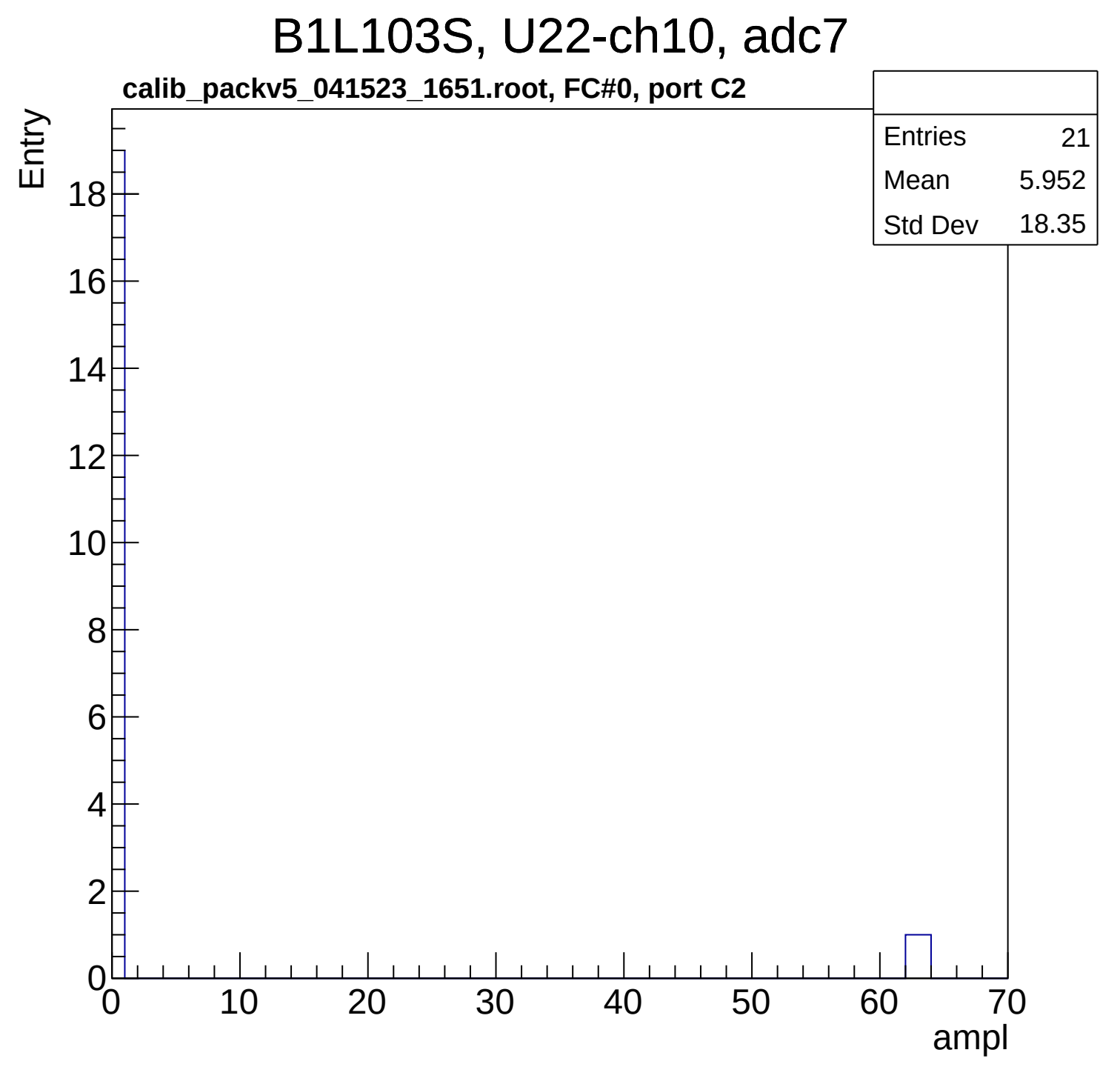
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch10, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 60
Std Dev 2.121
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U22-ch10, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.952
Std Dev 18.35
Entry
0
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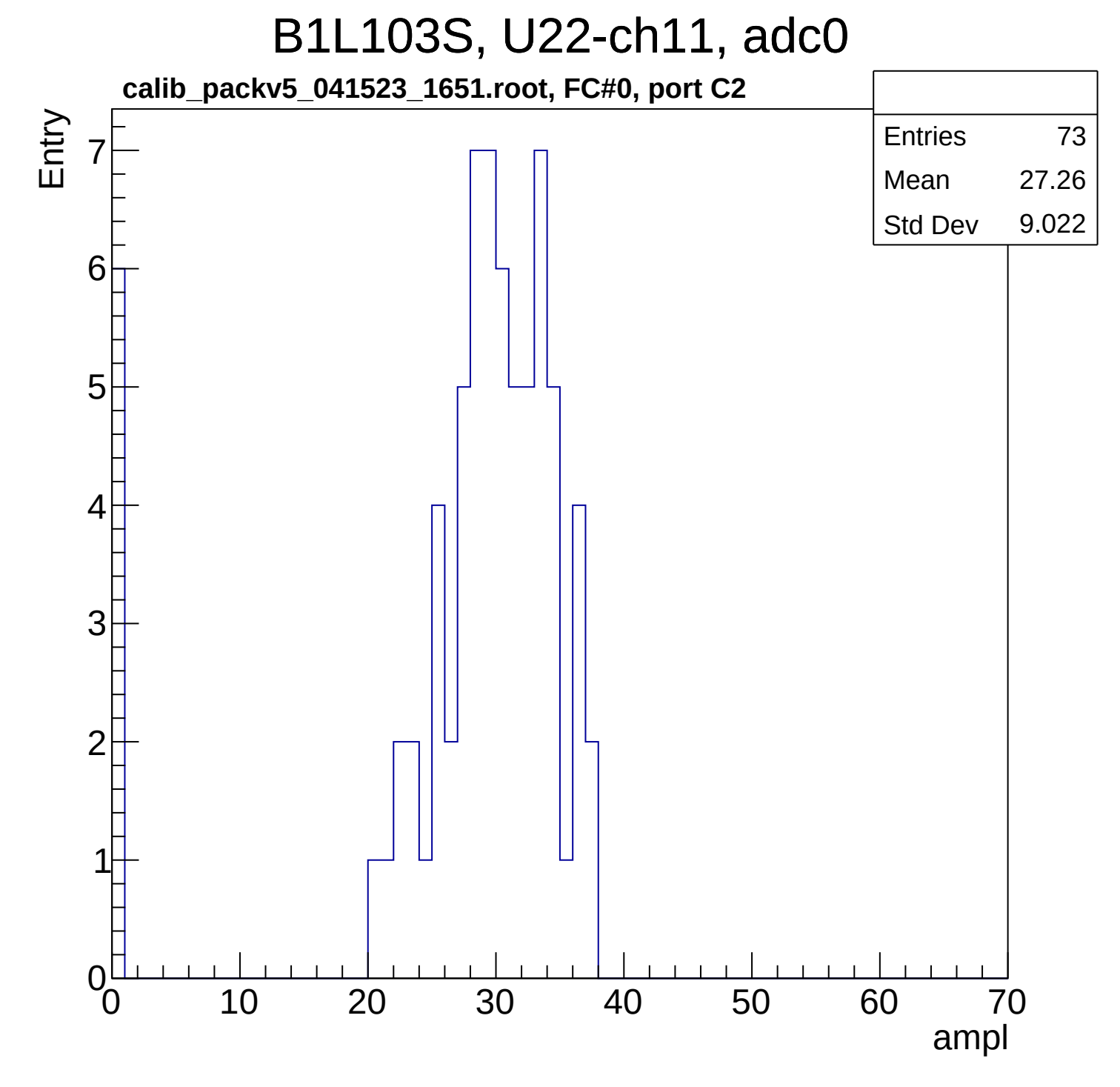
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch11, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 27.26
Std Dev 9.022
Entry
ampl
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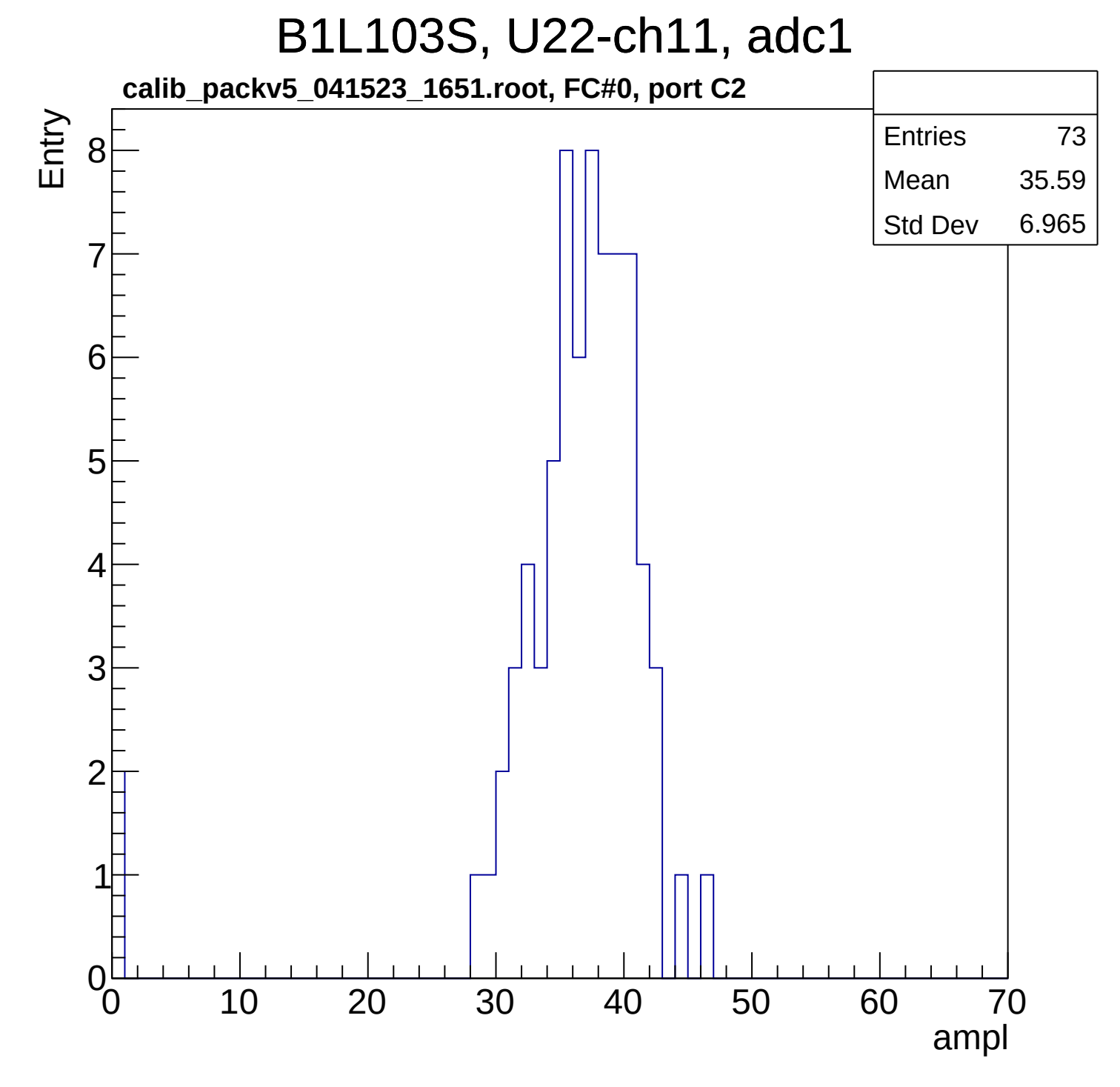
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U22-ch11, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 35.59
Std Dev 6.965
Entry
ampl
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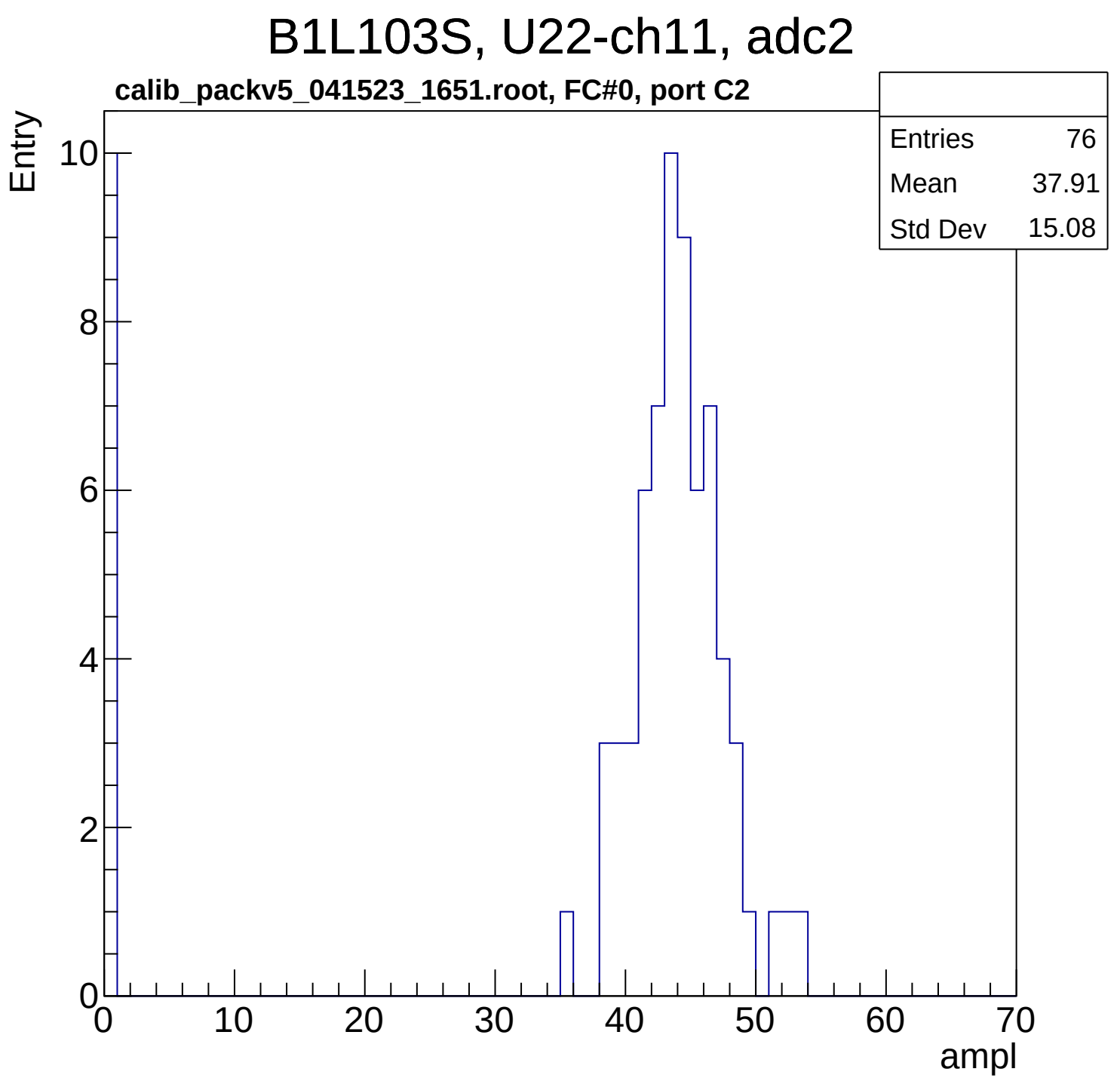
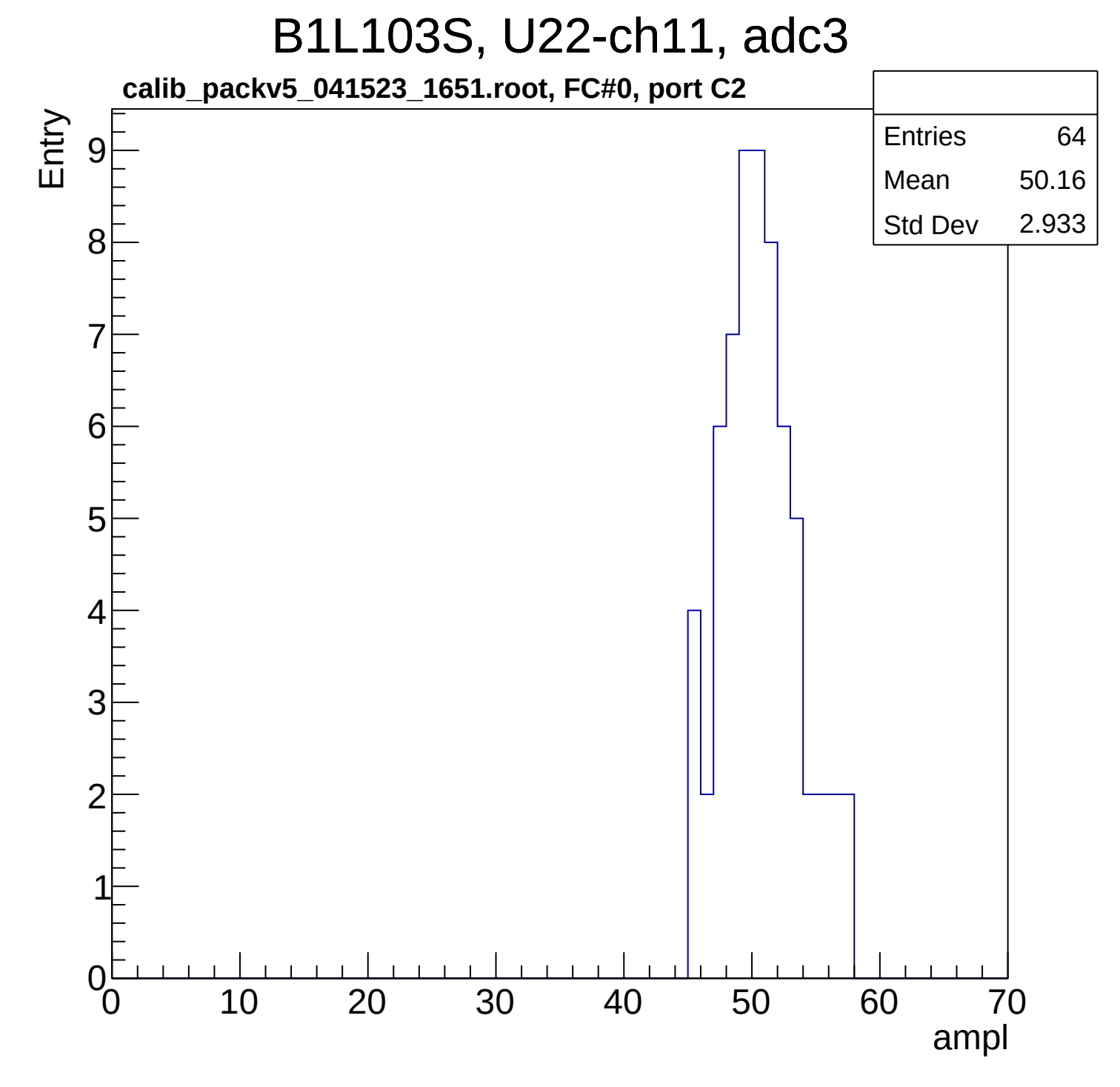
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch11, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 37.91
Std Dev 15.08
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch11, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 50.16
Std Dev 2.933
Entry
ampl
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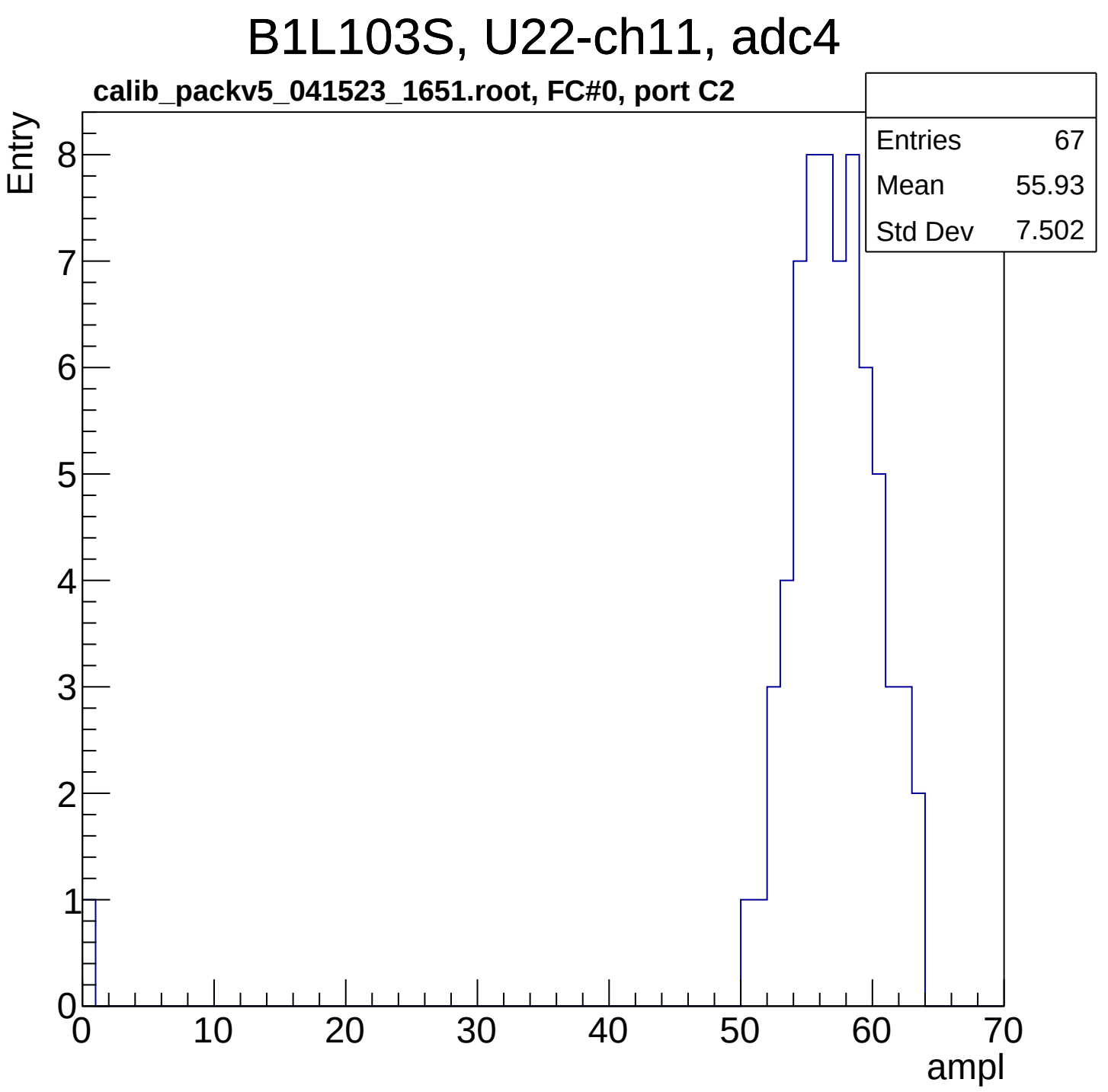
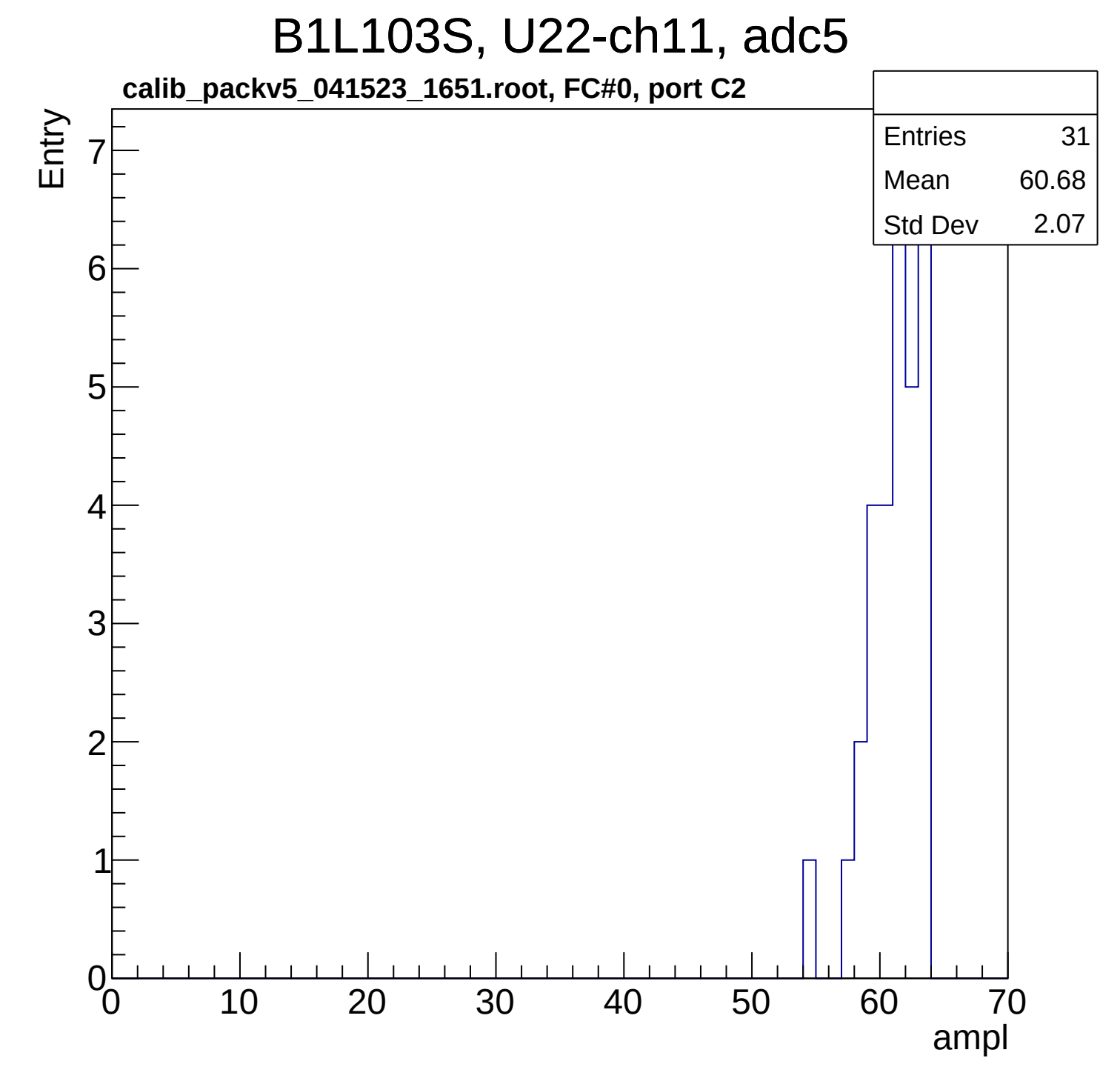
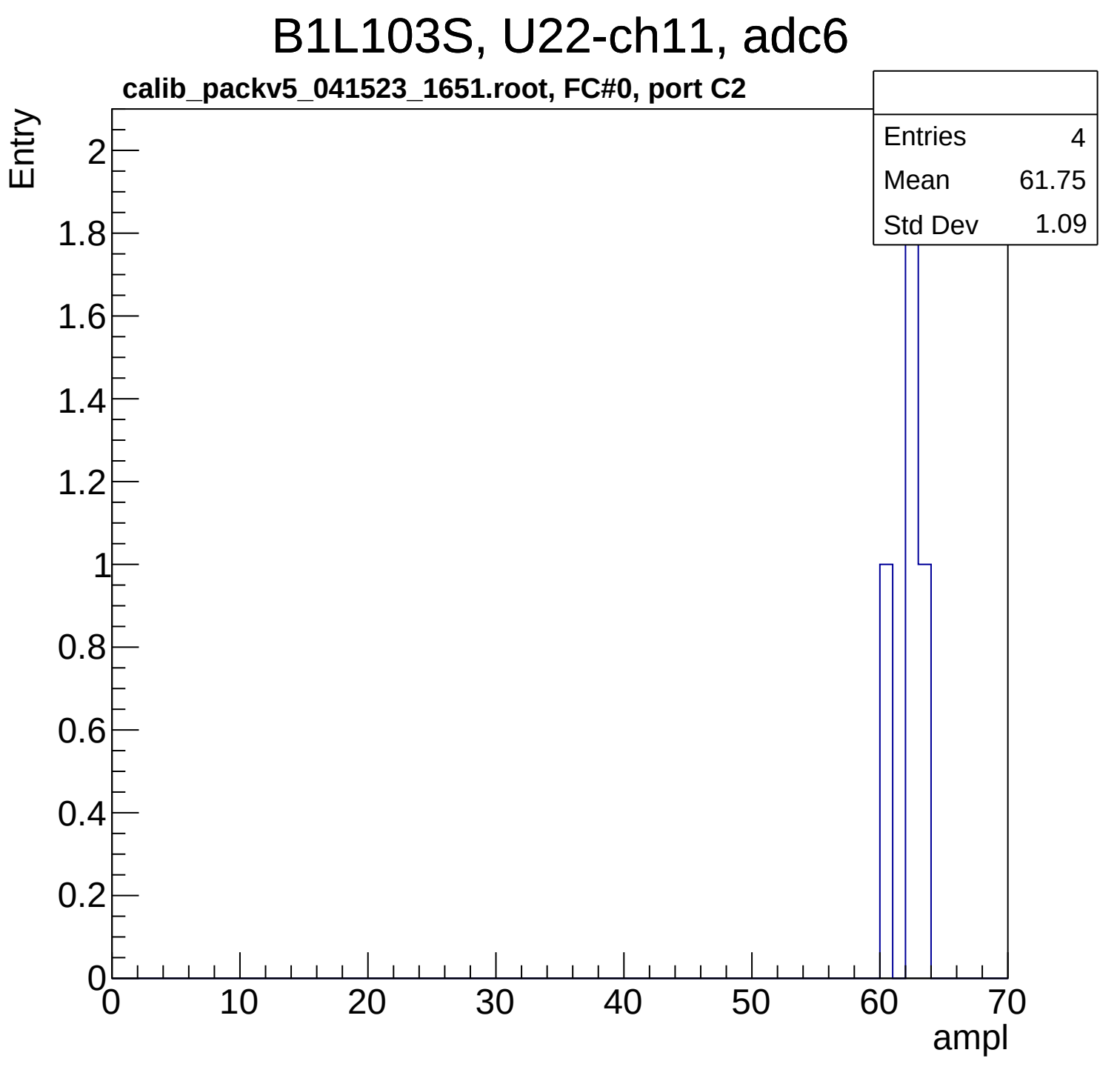
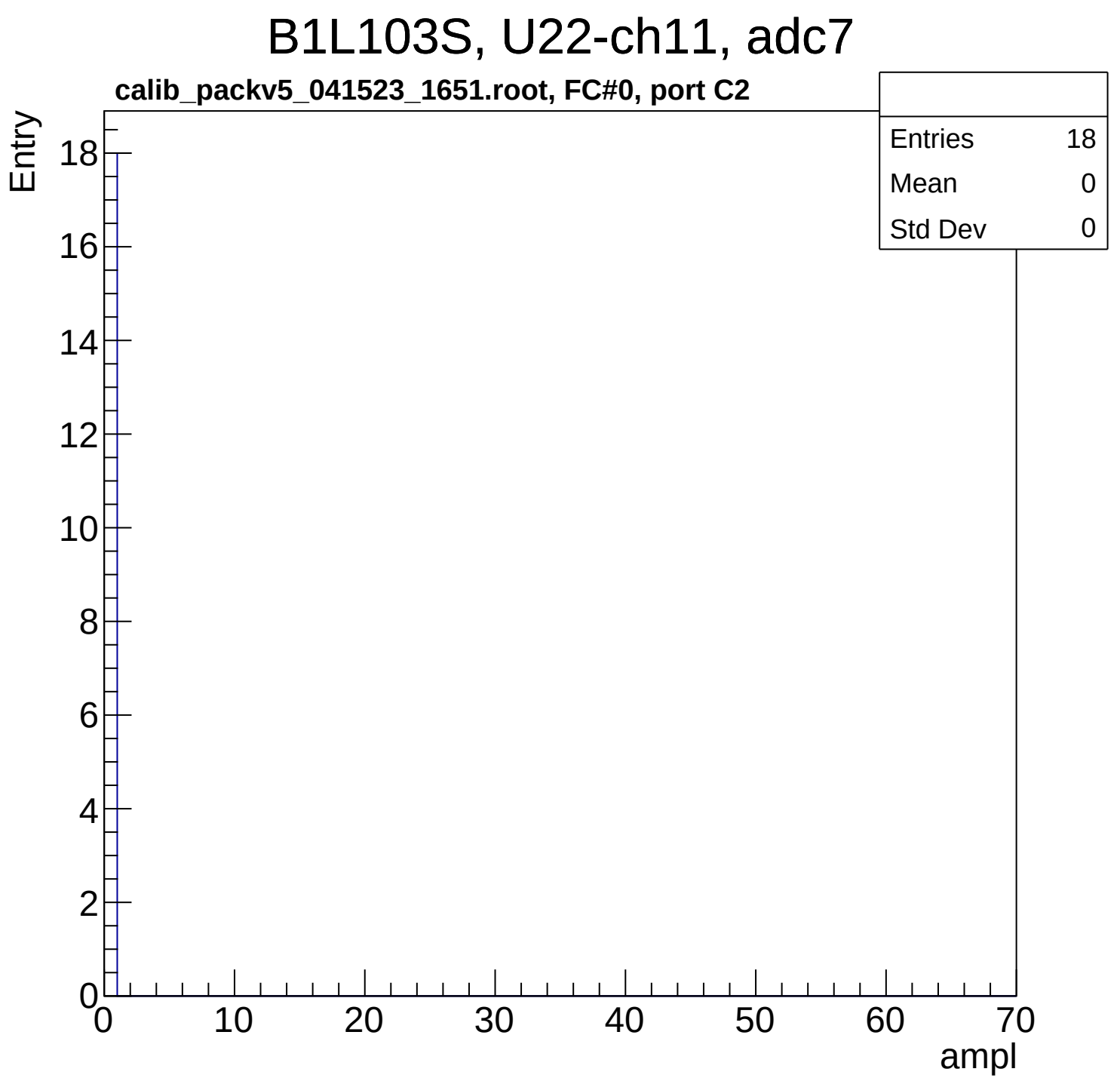
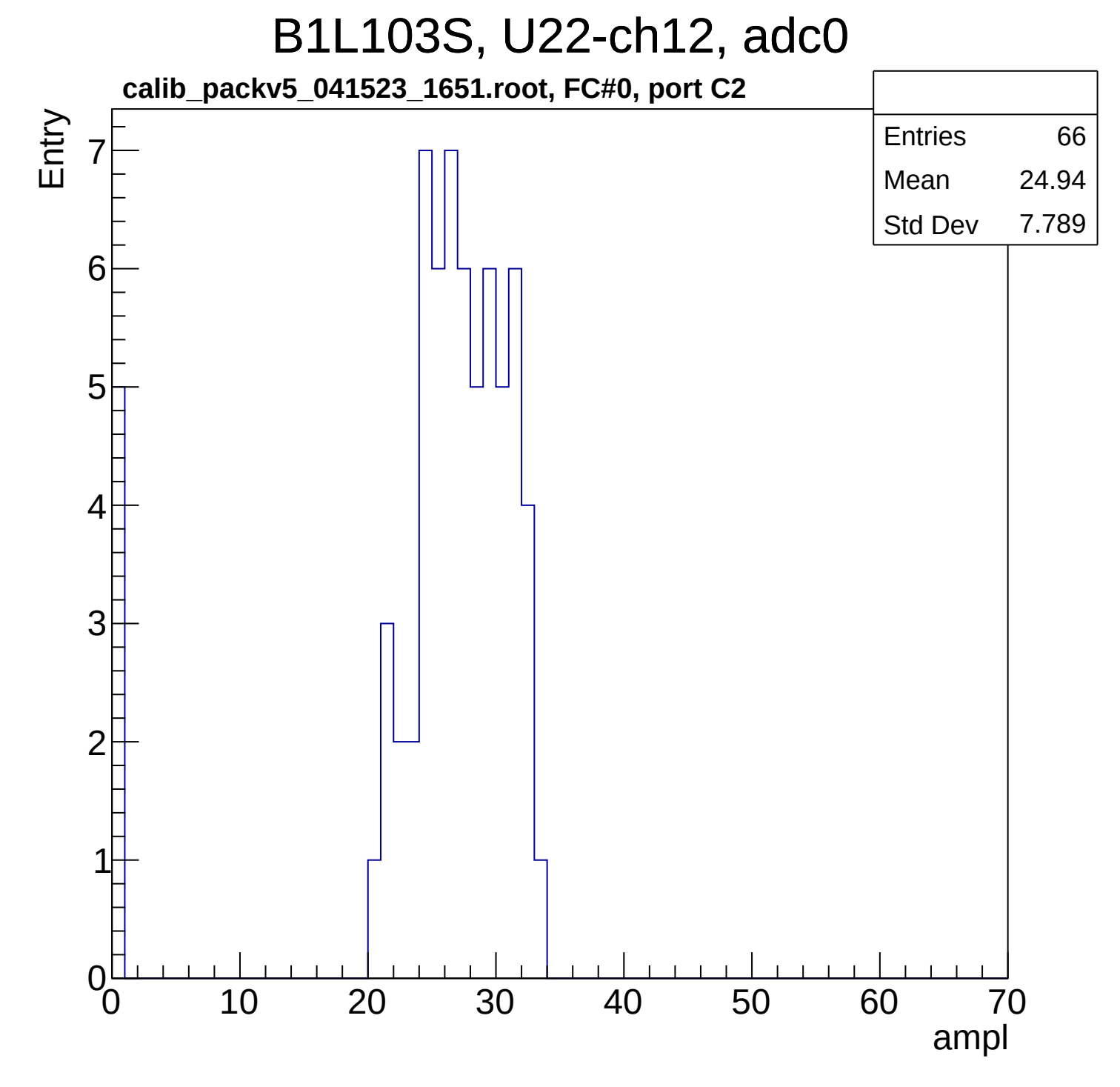
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch11, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 55.93
Std Dev 7.502
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch11, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 60.68
Std Dev 2.07
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U22-ch11, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 61.75
Std Dev 1.09
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U22-ch11, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch12, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 24.94
Std Dev 7.789
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
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40
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60
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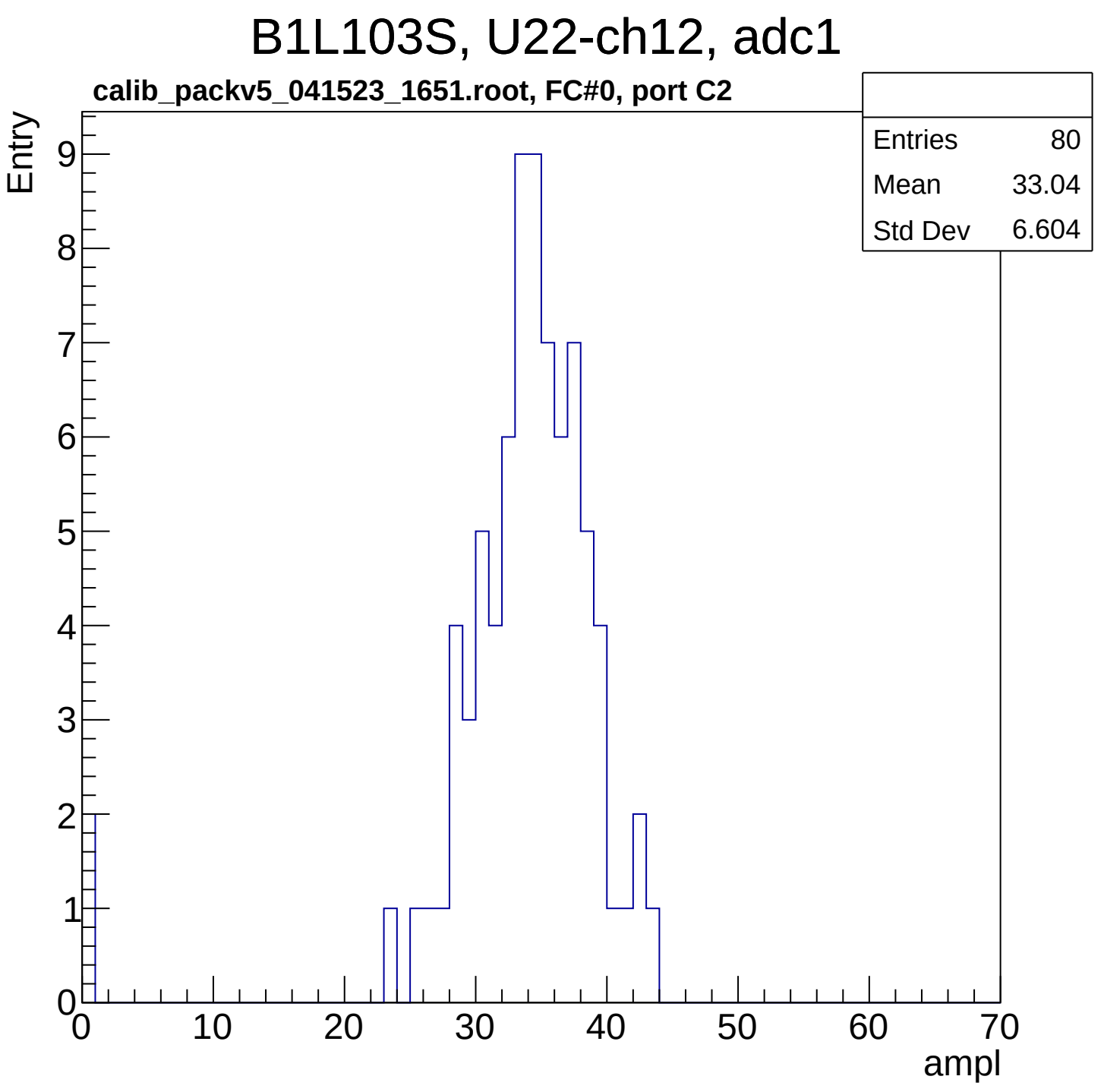
B1L103S, U22-ch12, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 33.04
Std Dev 6.604
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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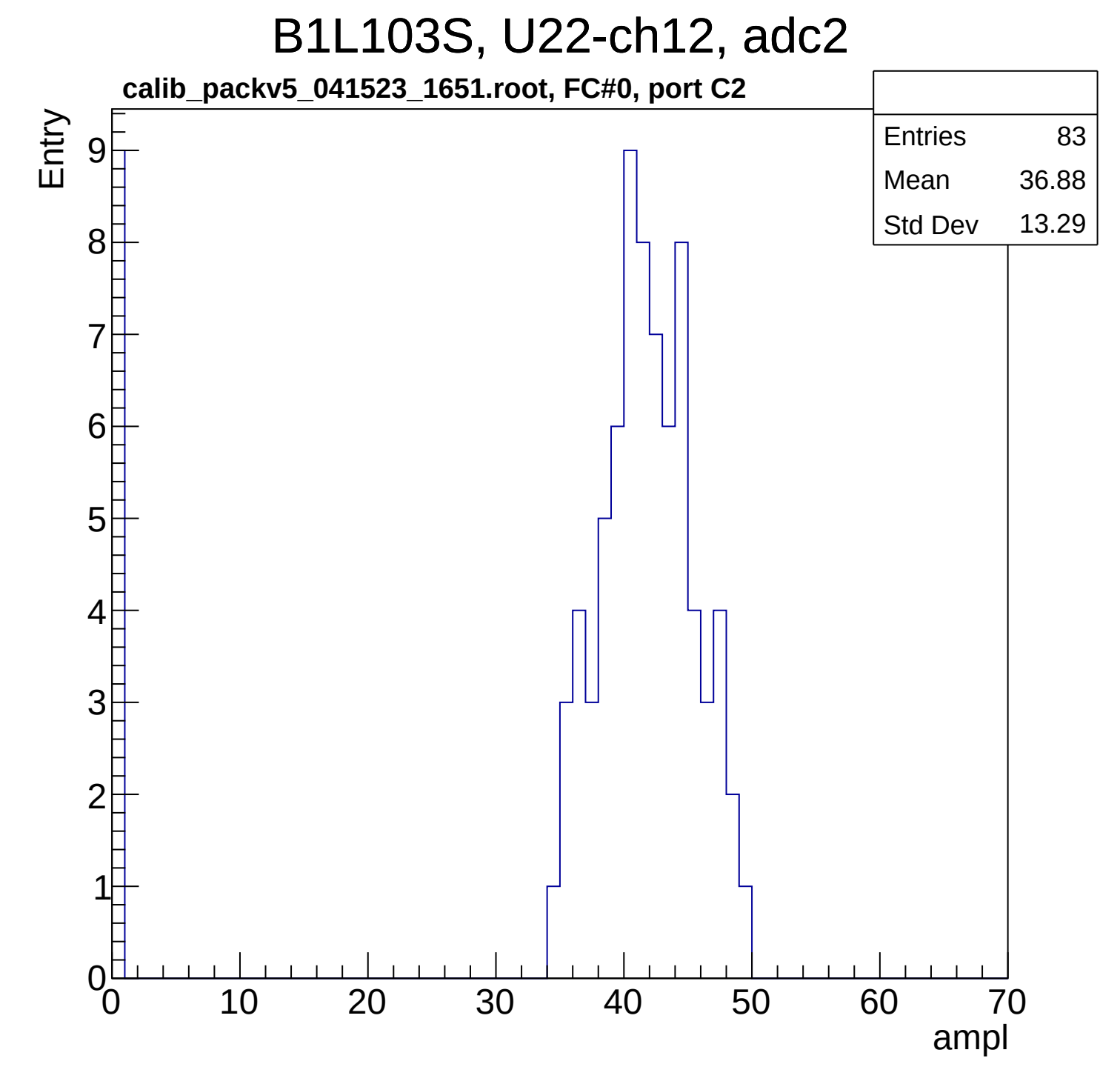
B1L103S, U22-ch12, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 36.88
Std Dev 13.29
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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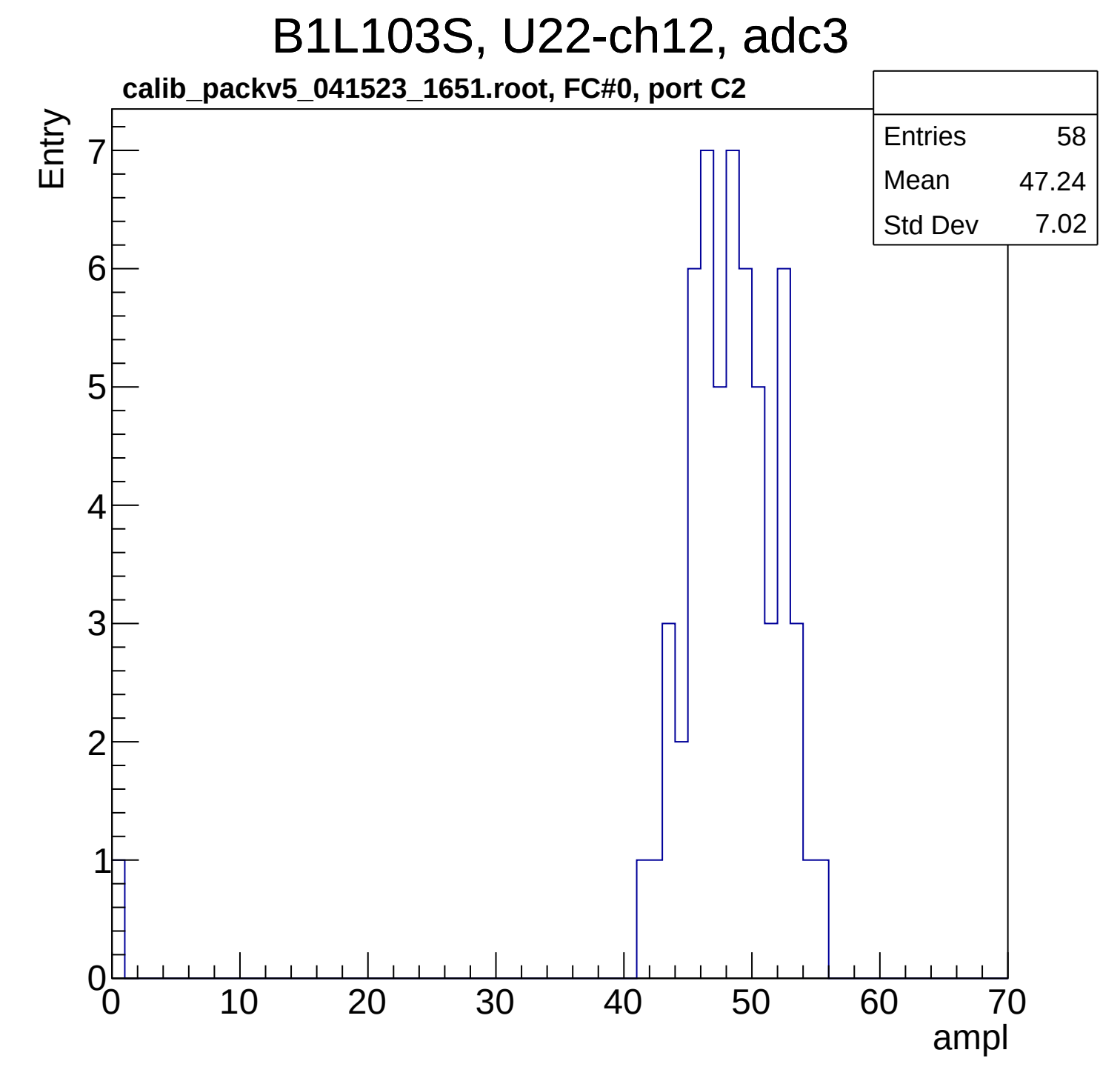
B1L103S, U22-ch12, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 47.24
Std Dev 7.02
Entry
ampl
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1
2
3
4
5
6
7
0
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20
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40
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60
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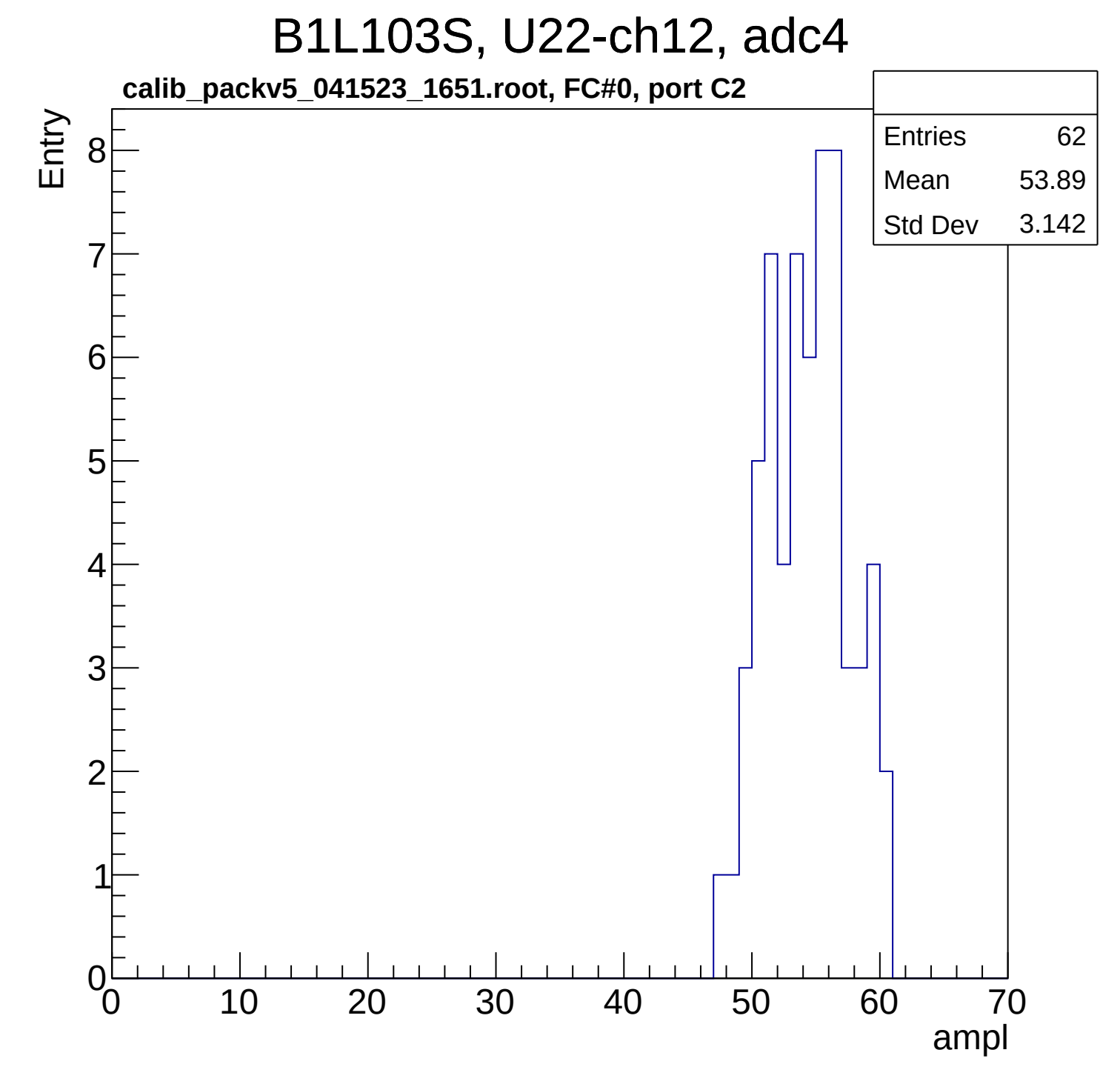
B1L103S, U22-ch12, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 53.89
Std Dev 3.142
Entry
ampl
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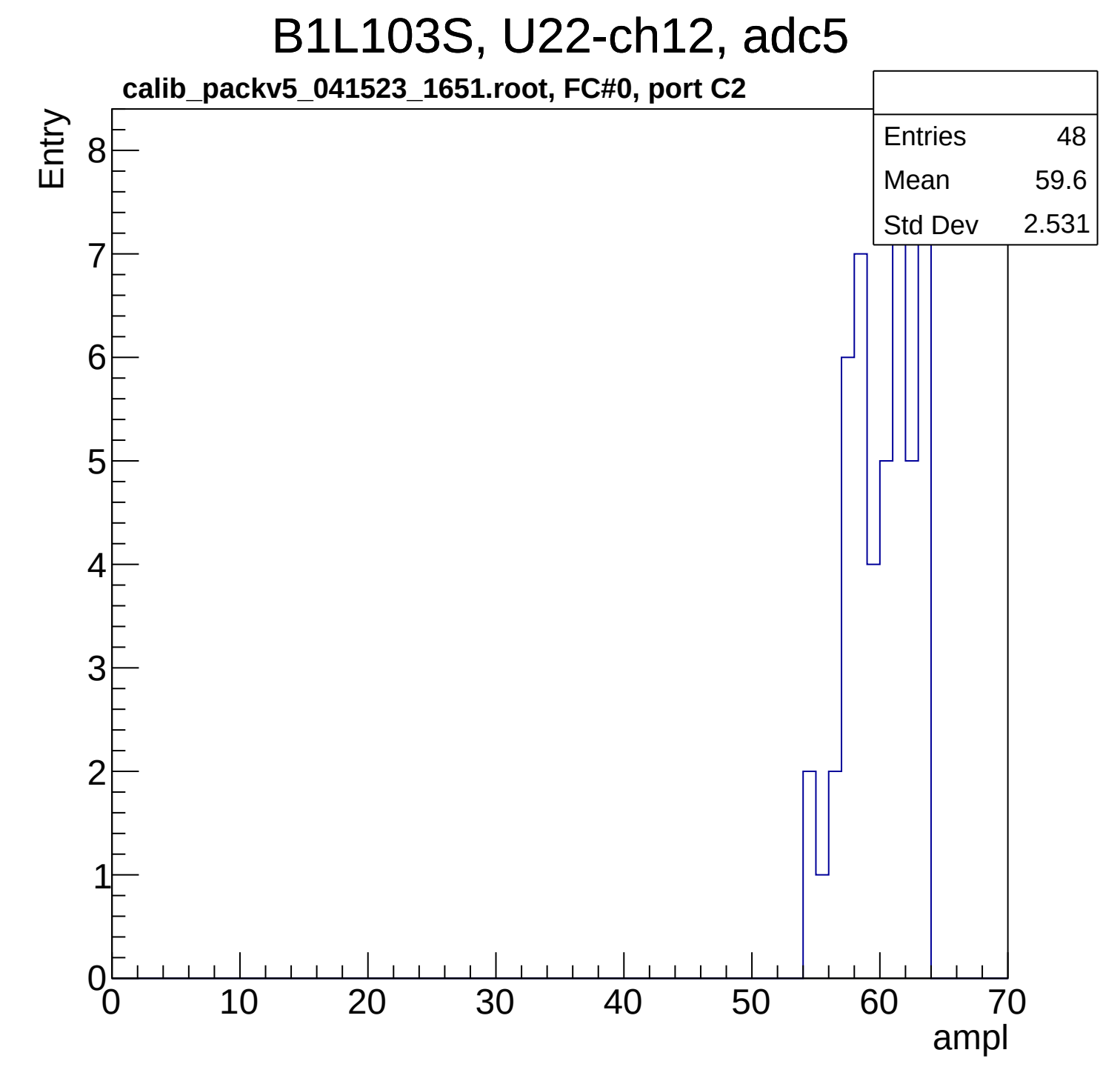
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch12, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 59.6
Std Dev 2.531
Entry
ampl
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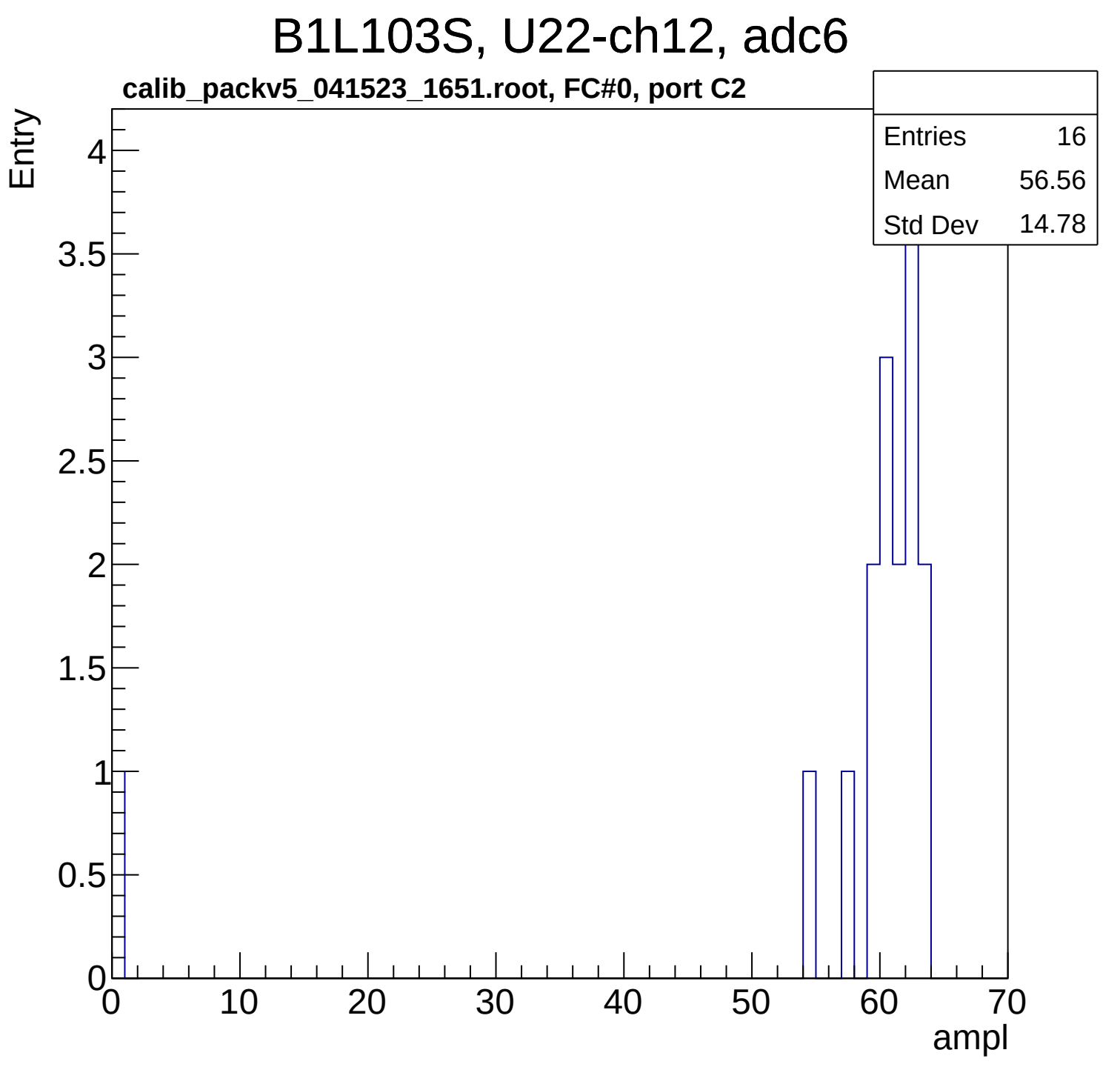
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch12, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 56.56
Std Dev 14.78
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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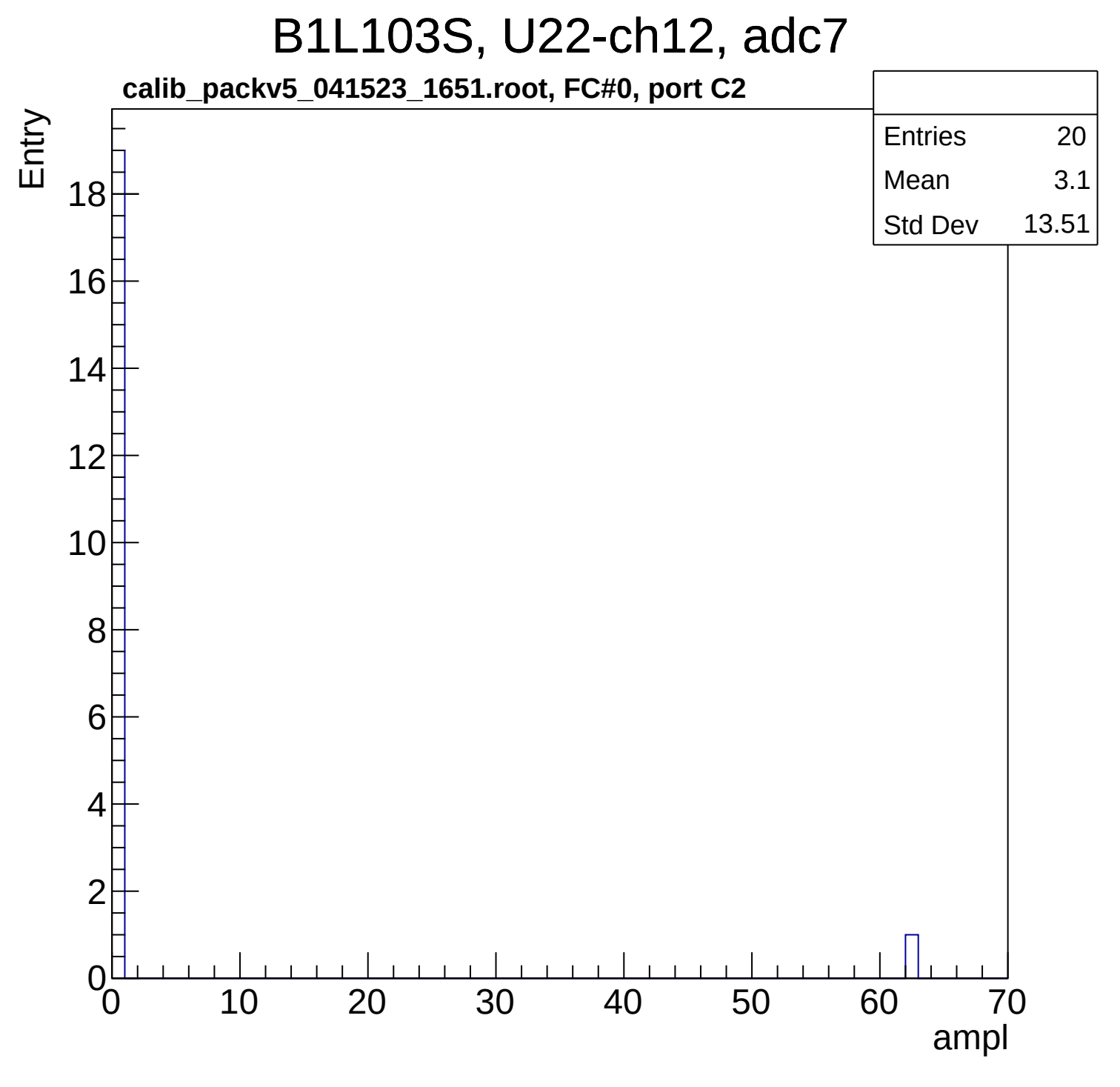
B1L103S, U22-ch12, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
2
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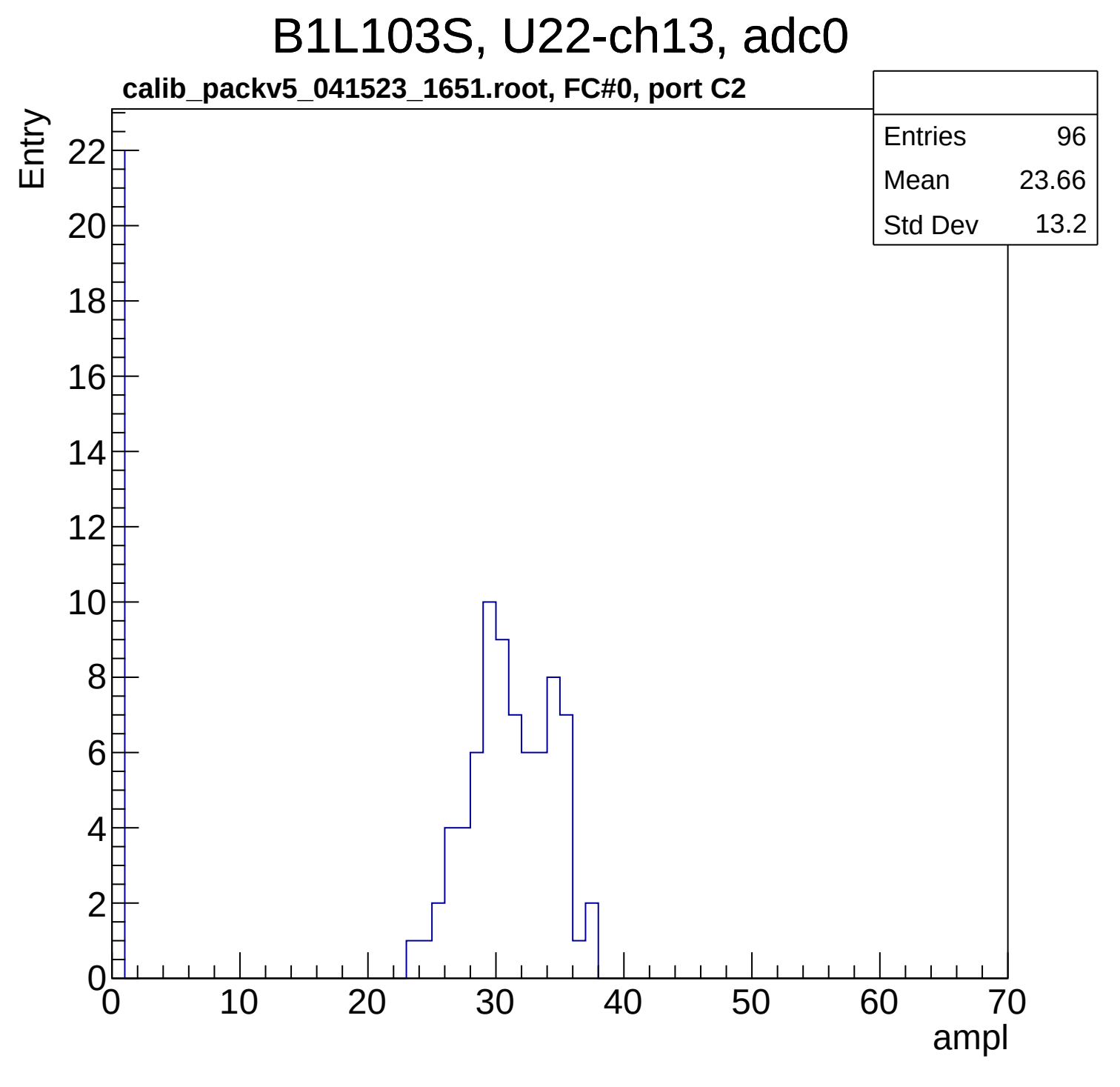
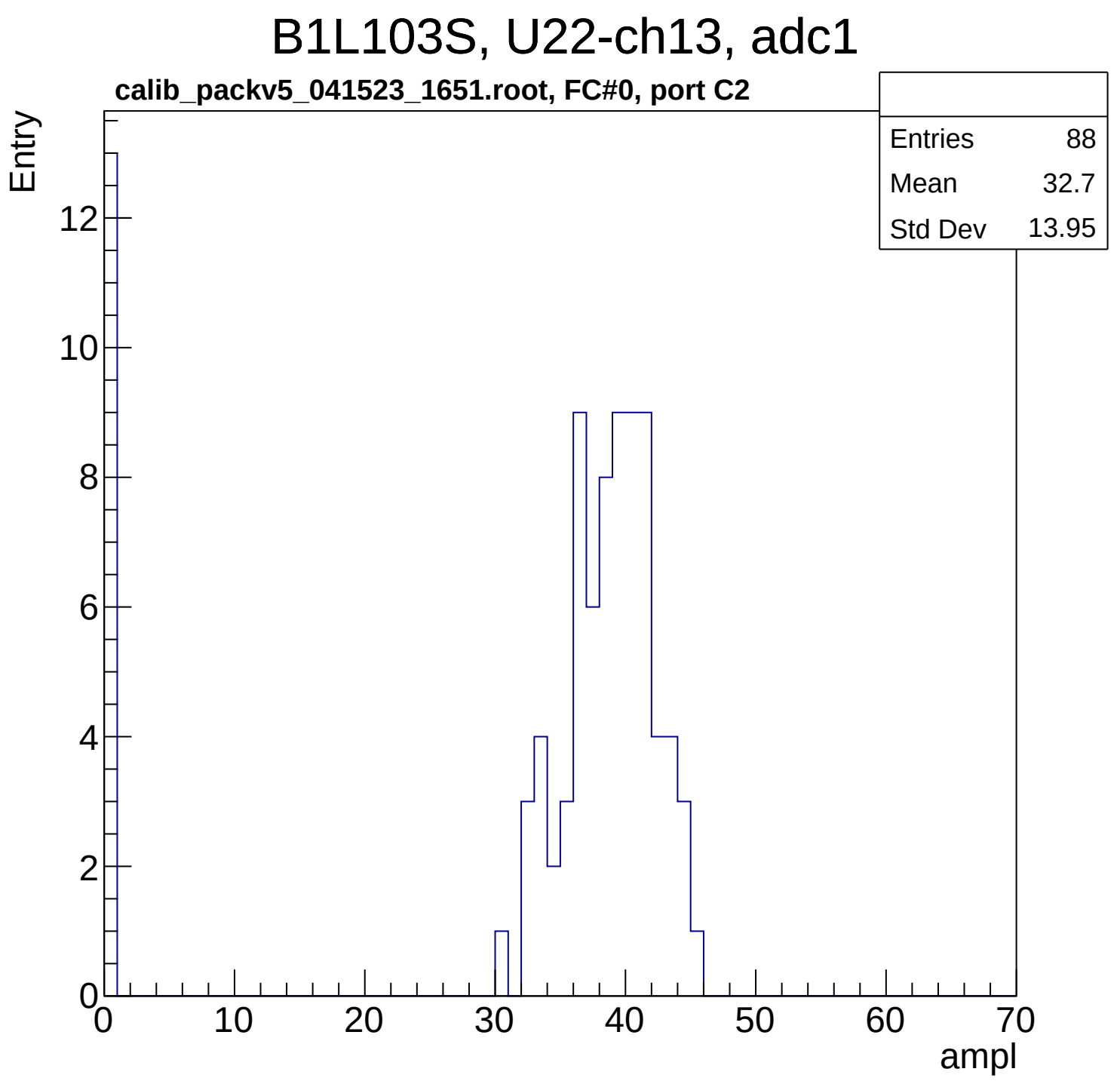
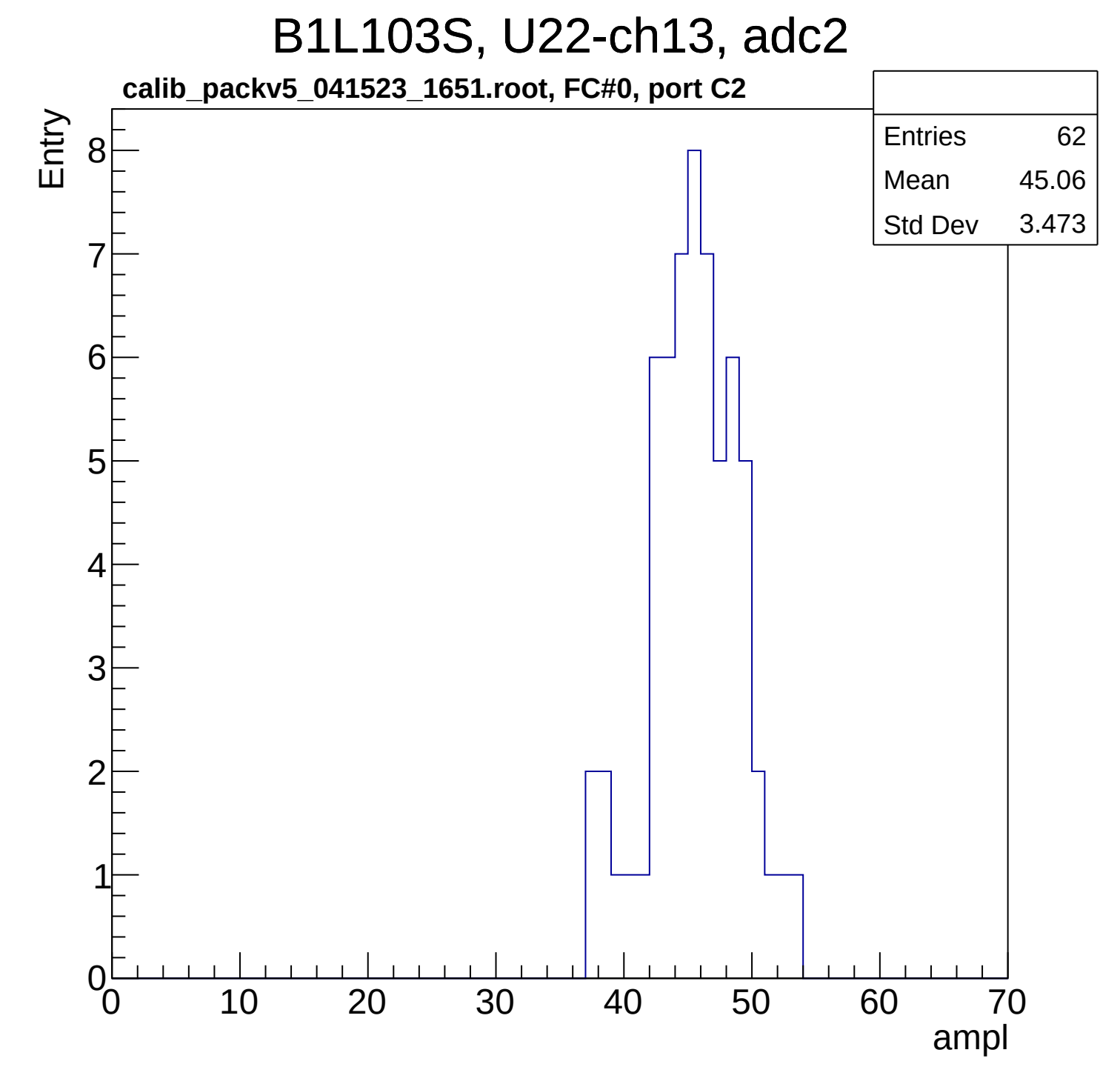
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch13, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 96
Mean 23.66
Std Dev 13.2
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70


B1L103S, U22-ch13, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 32.7
Std Dev 13.95
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch13, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 45.06
Std Dev 3.473
Entry
ampl
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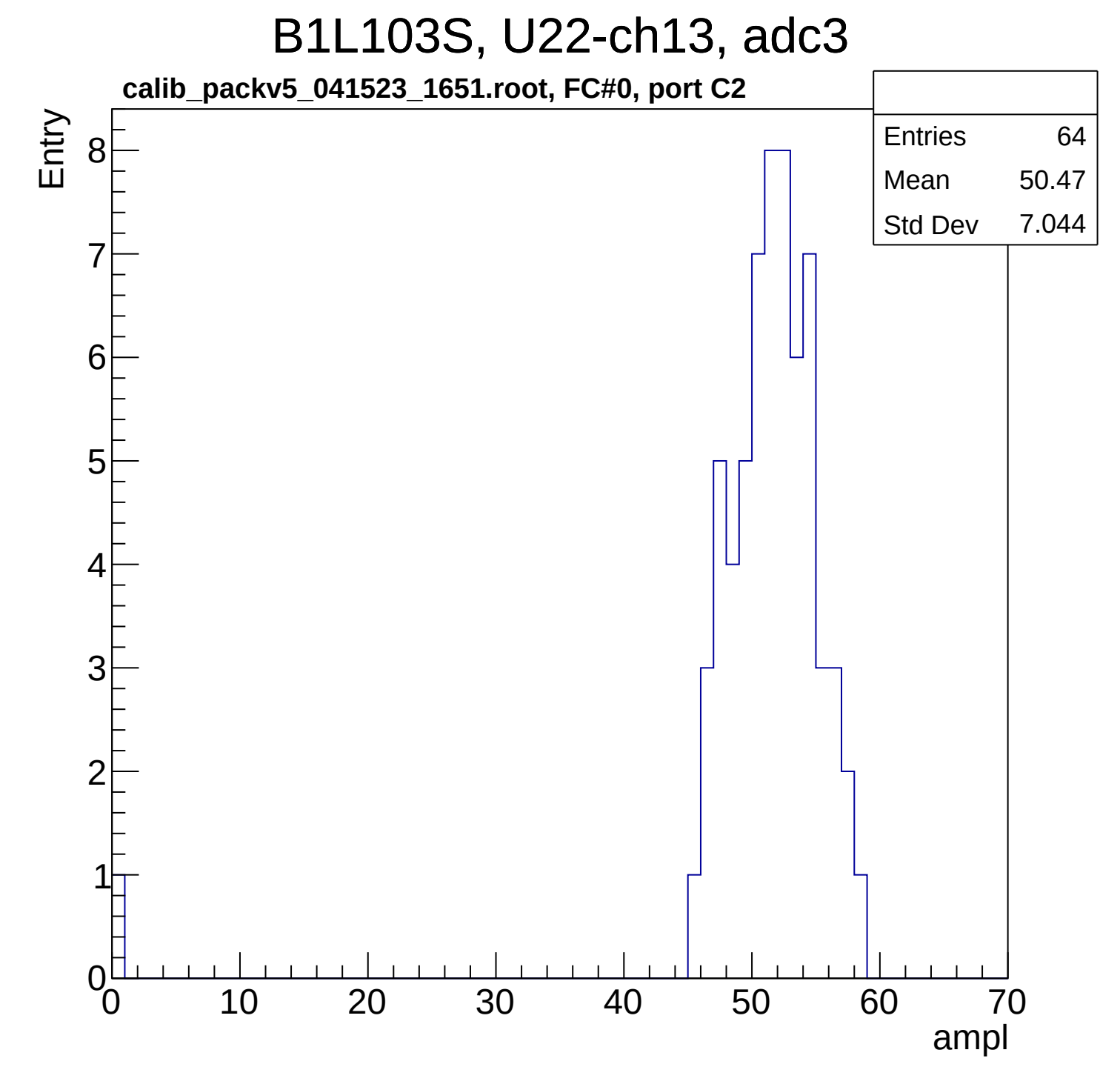
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch13, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 50.47
Std Dev 7.044
Entry
ampl
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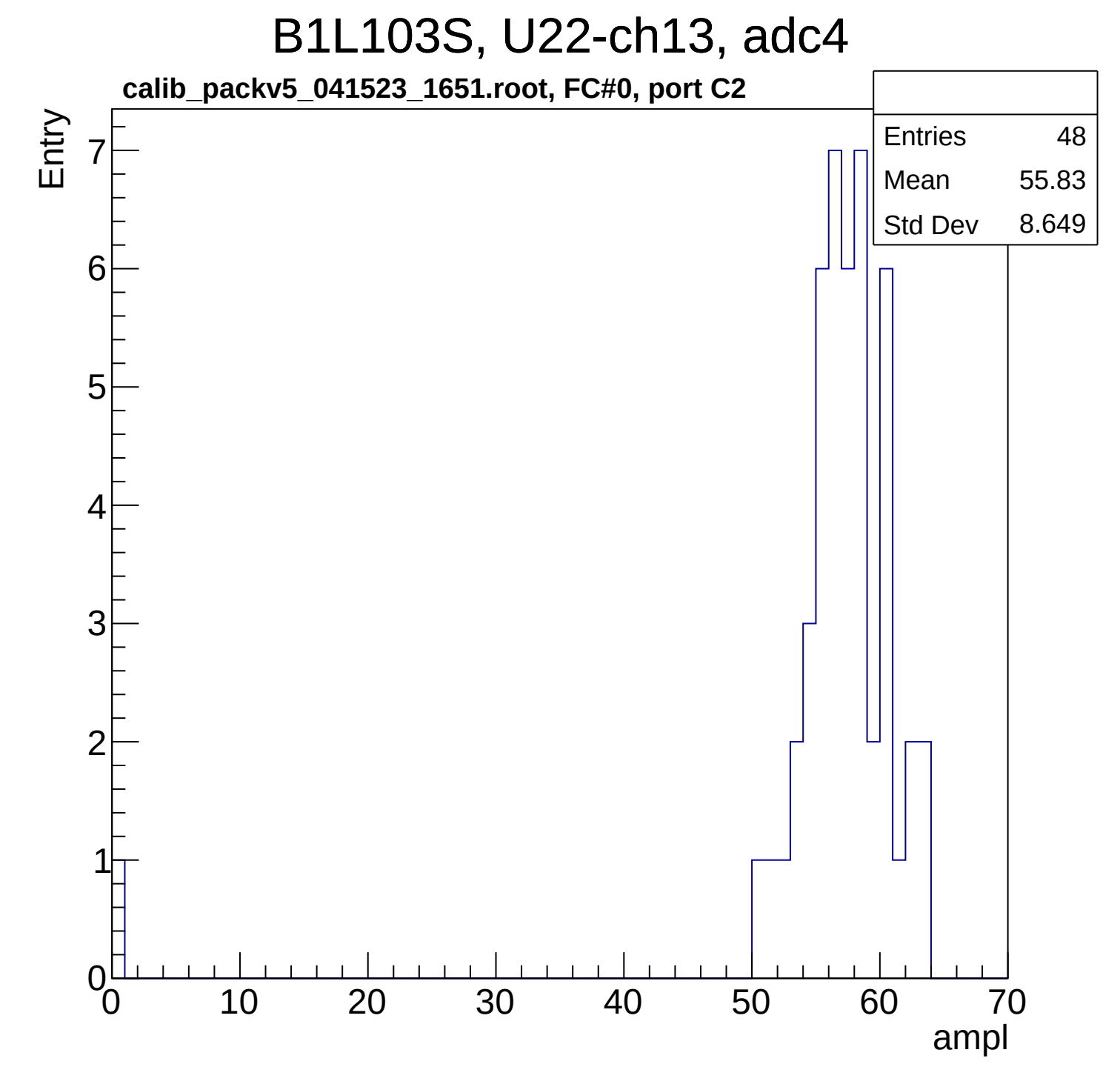
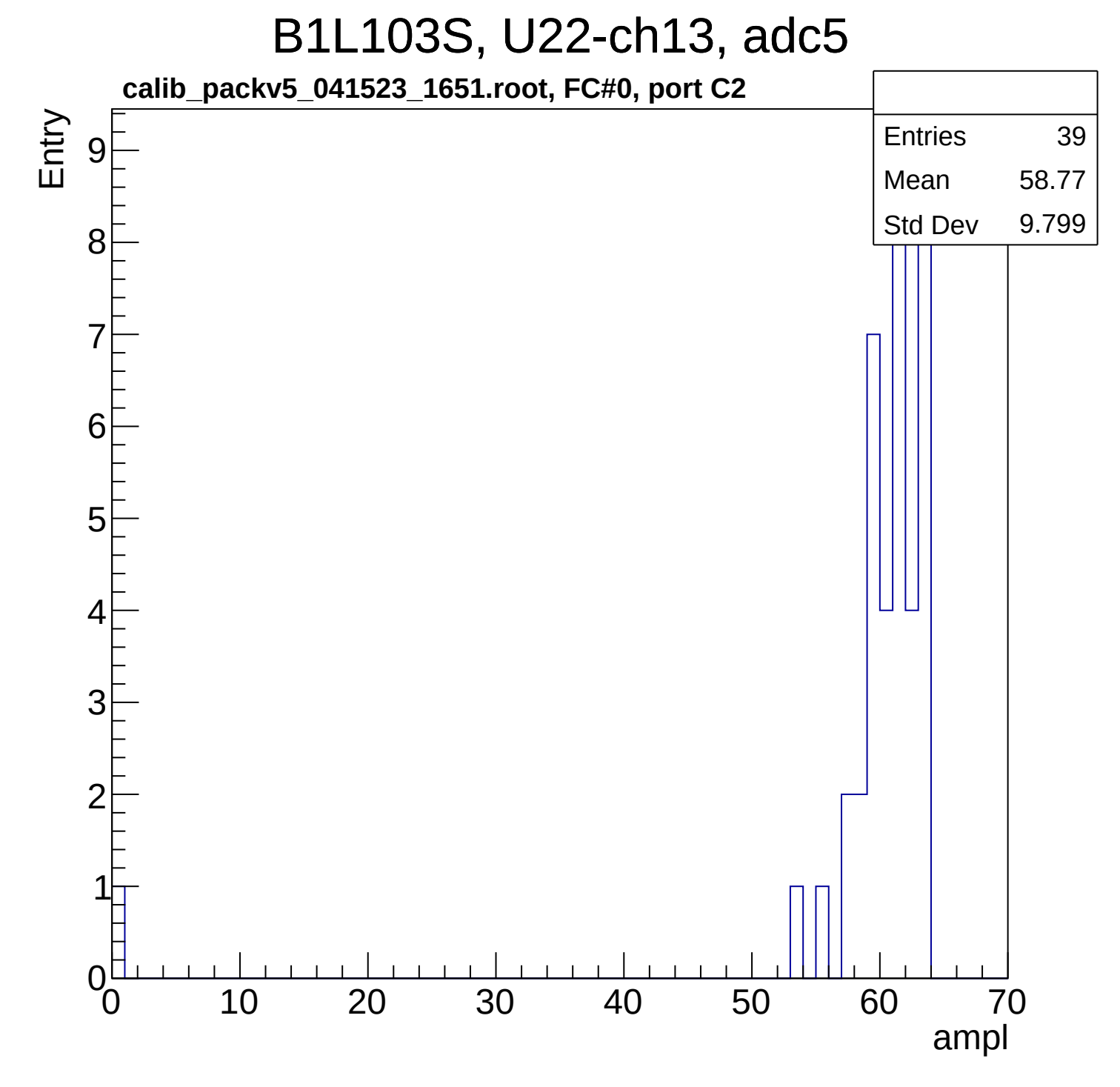
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch13, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 55.83
Std Dev 8.649
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U22-ch13, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 58.77
Std Dev 9.799
Entry
ampl
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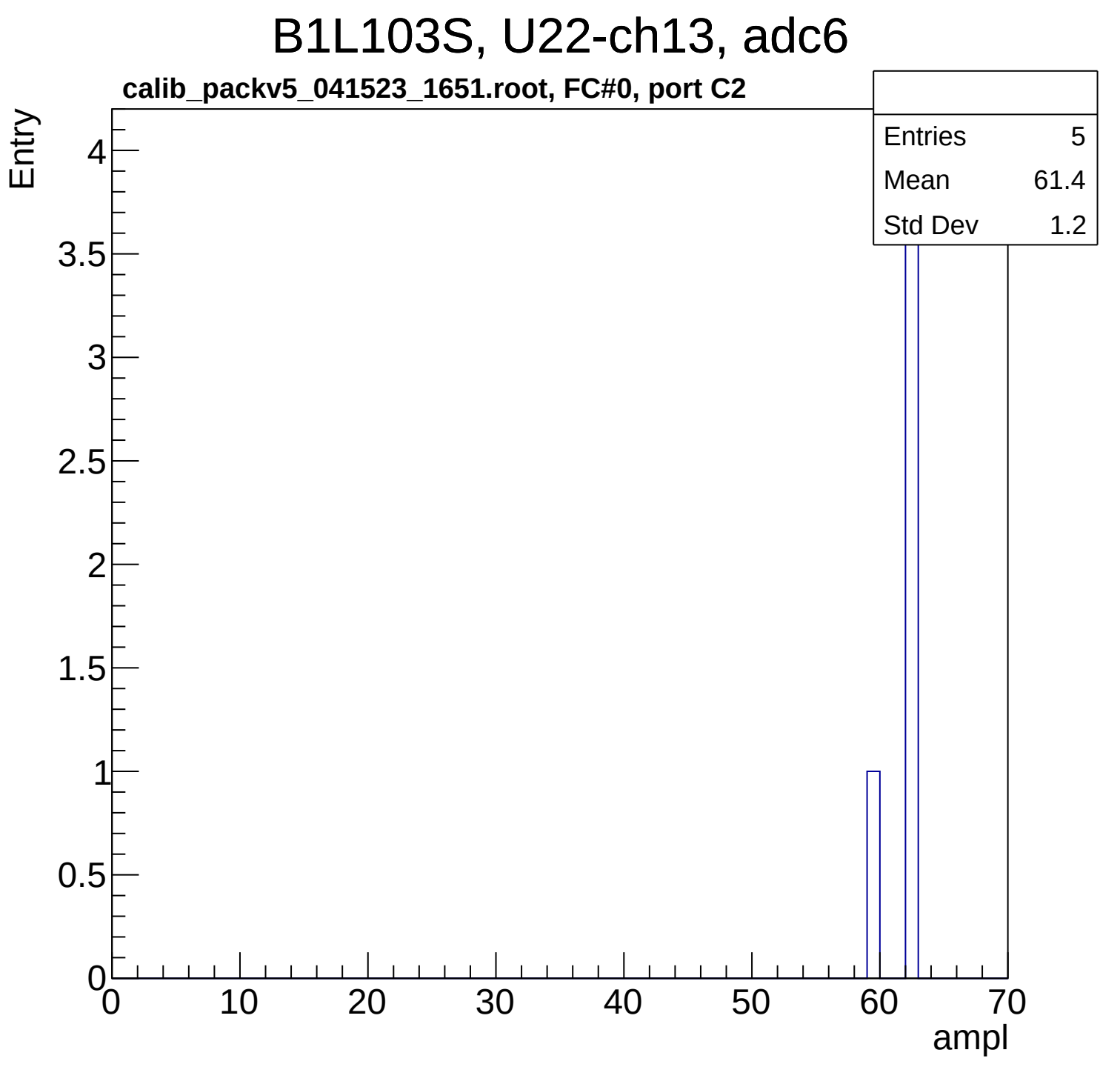
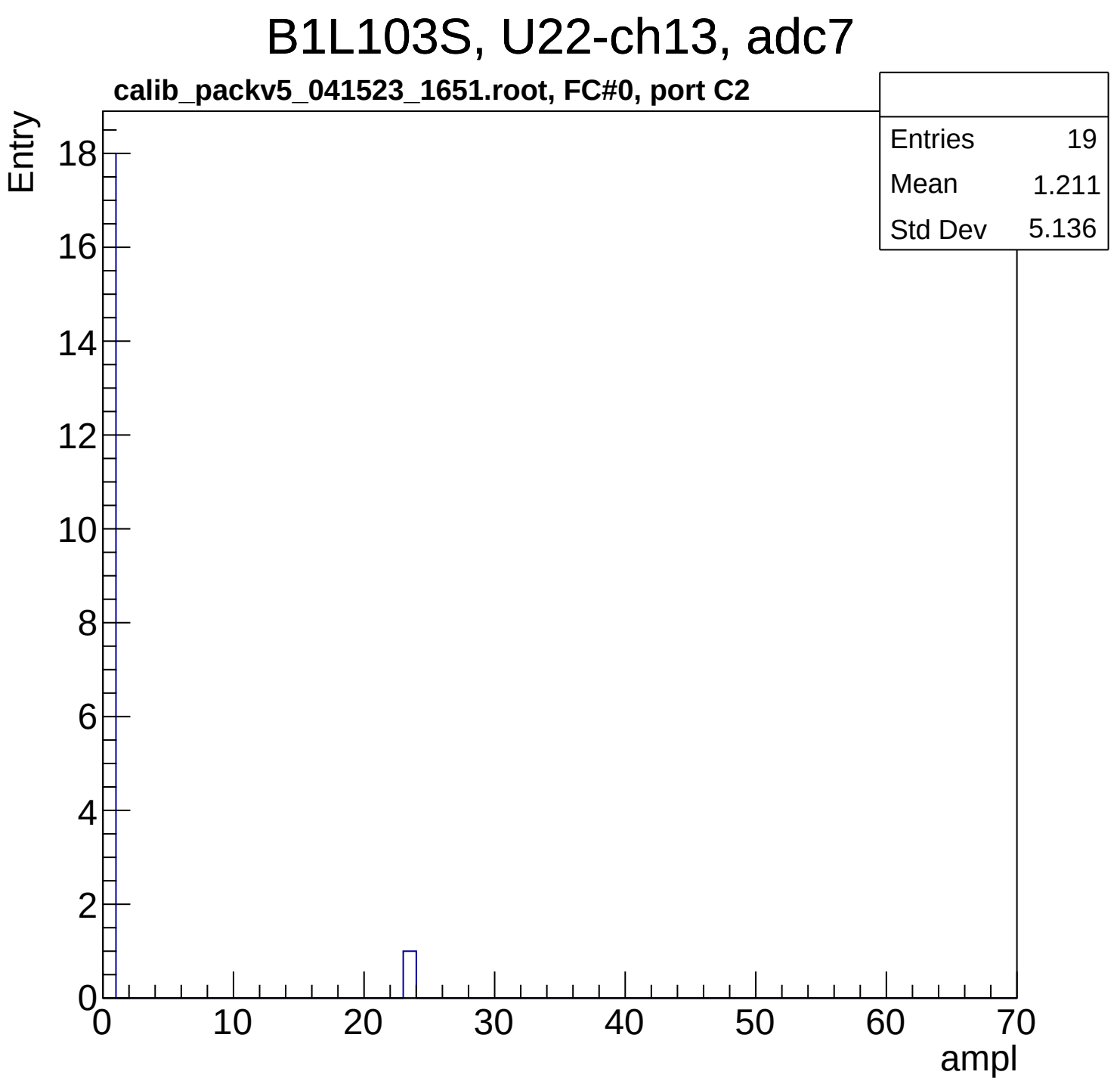
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch13, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 61.4
Std Dev 1.2
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U22-ch13, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.211
Std Dev 5.136
Entry
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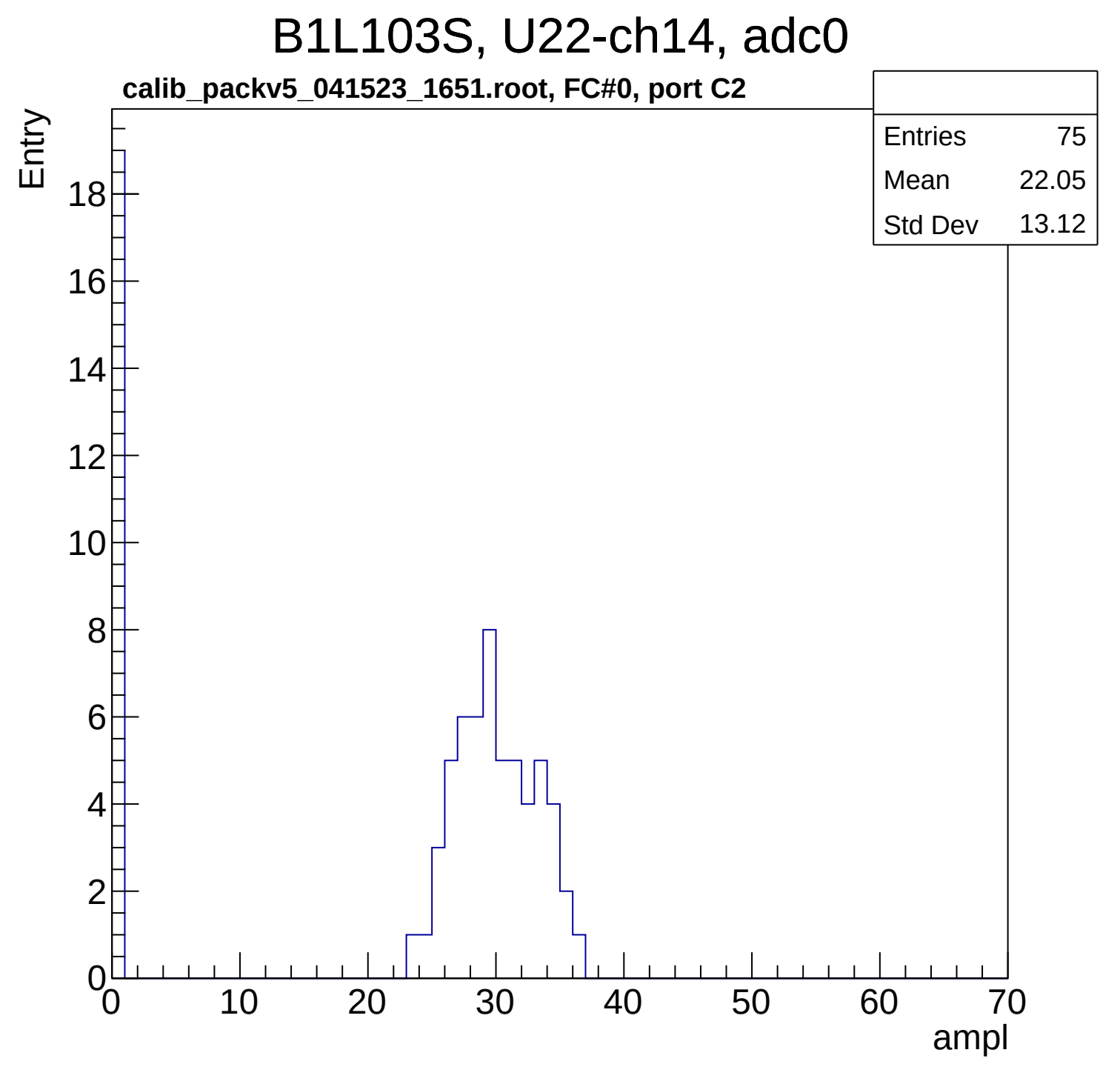
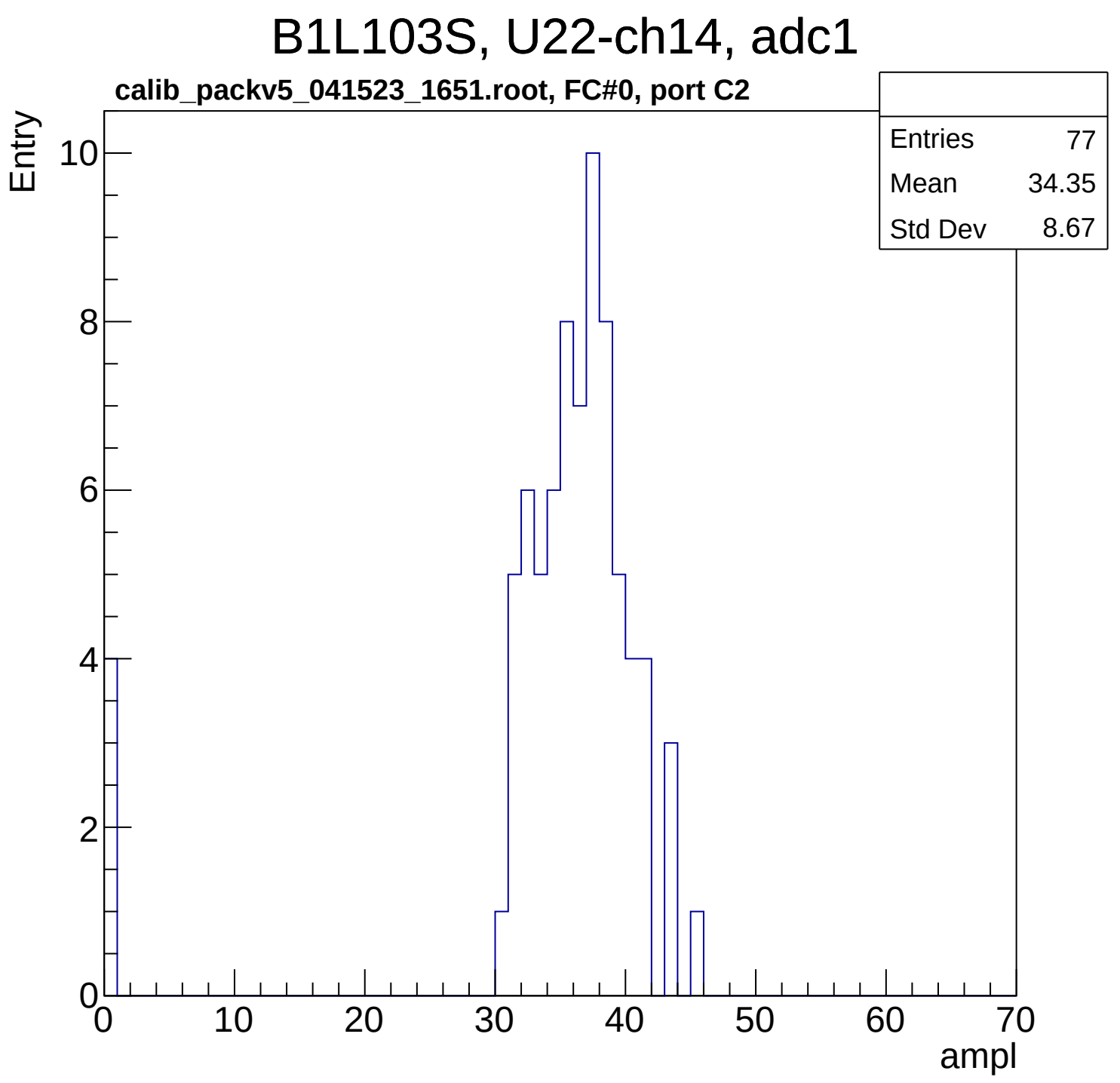
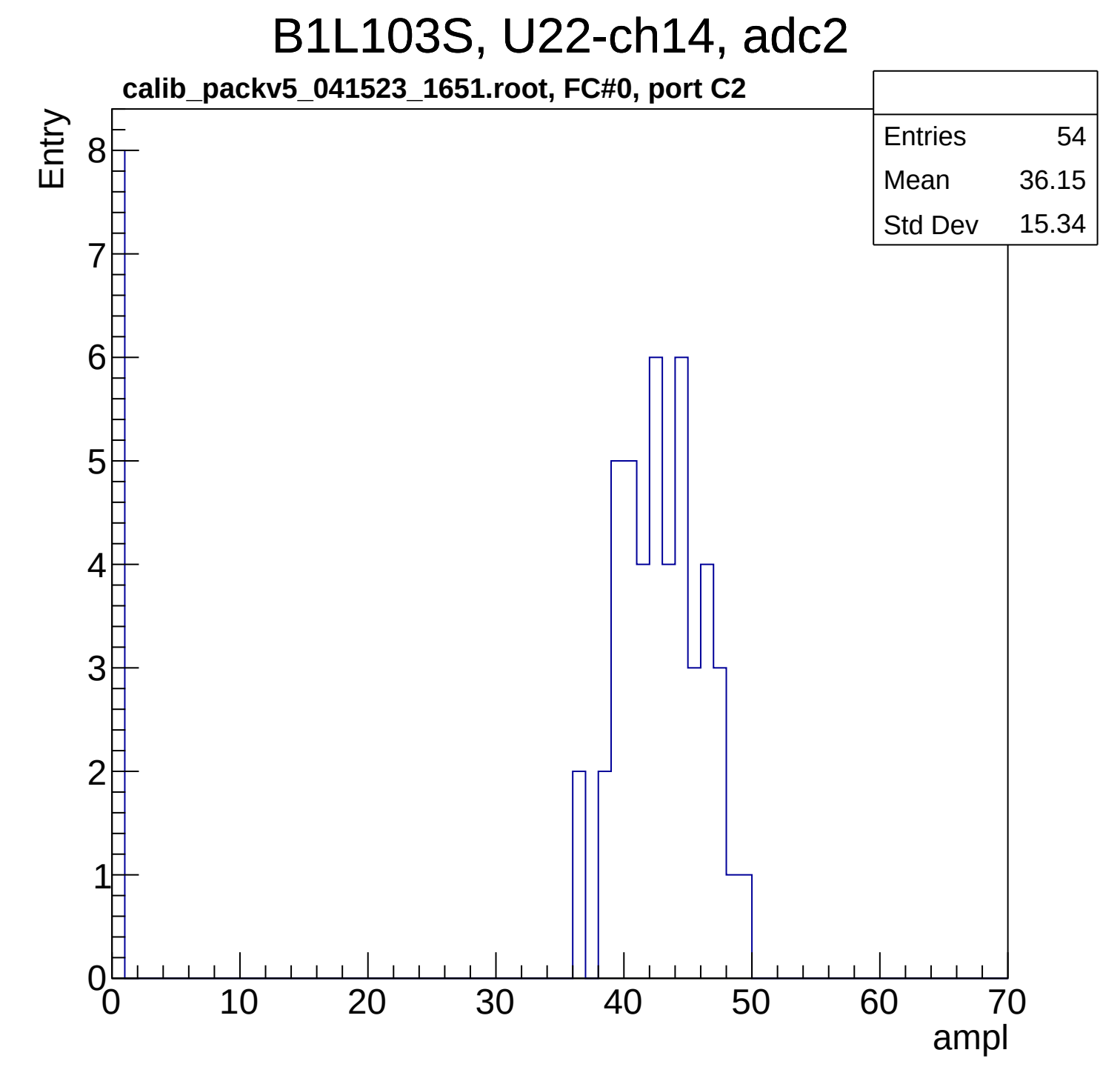
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch14, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 22.05
Std Dev 13.12
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch14, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 34.35
Std Dev 8.67
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch14, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 36.15
Std Dev 15.34
Entry
ampl
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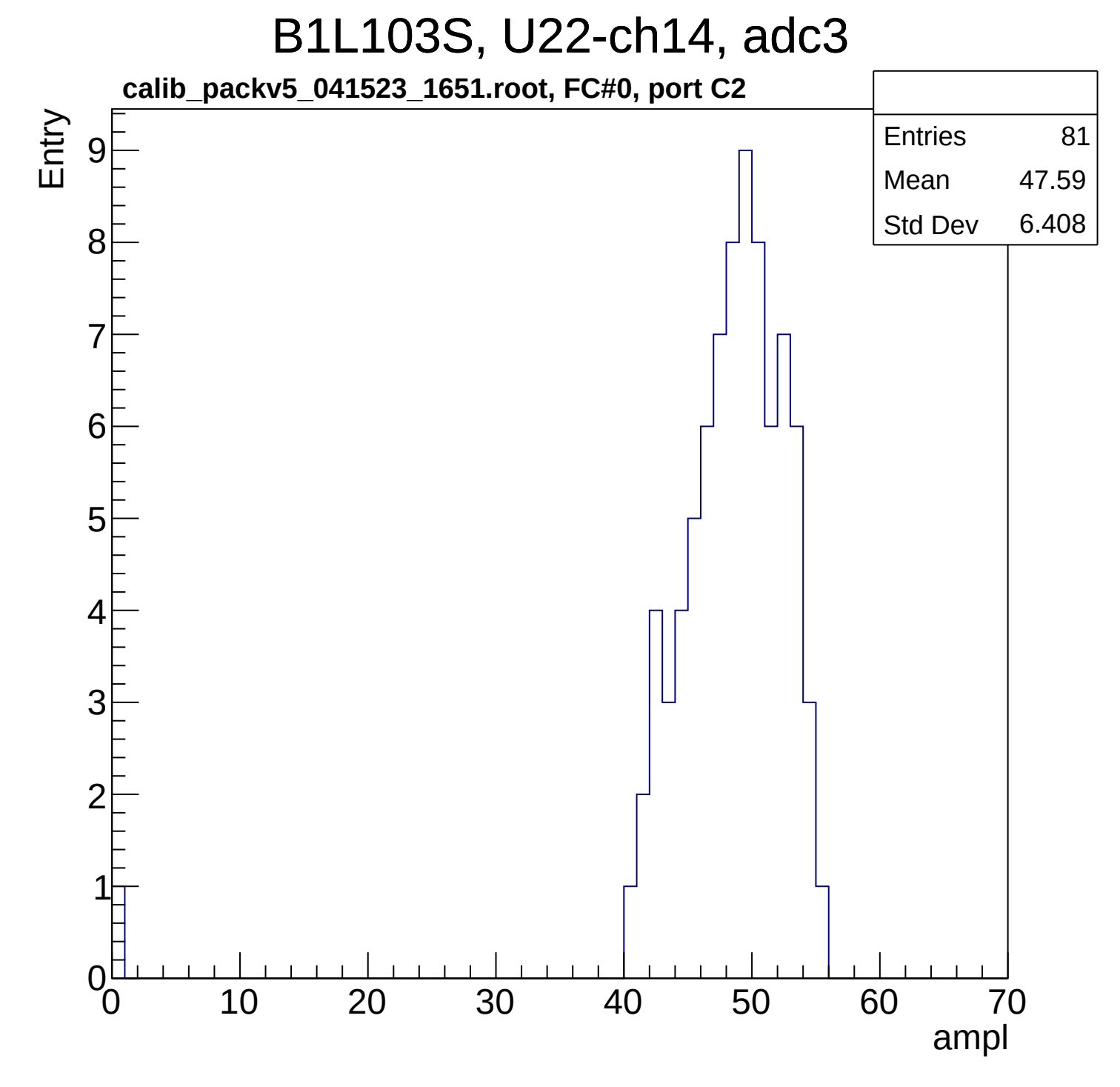
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch14, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 47.59
Std Dev 6.408
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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60
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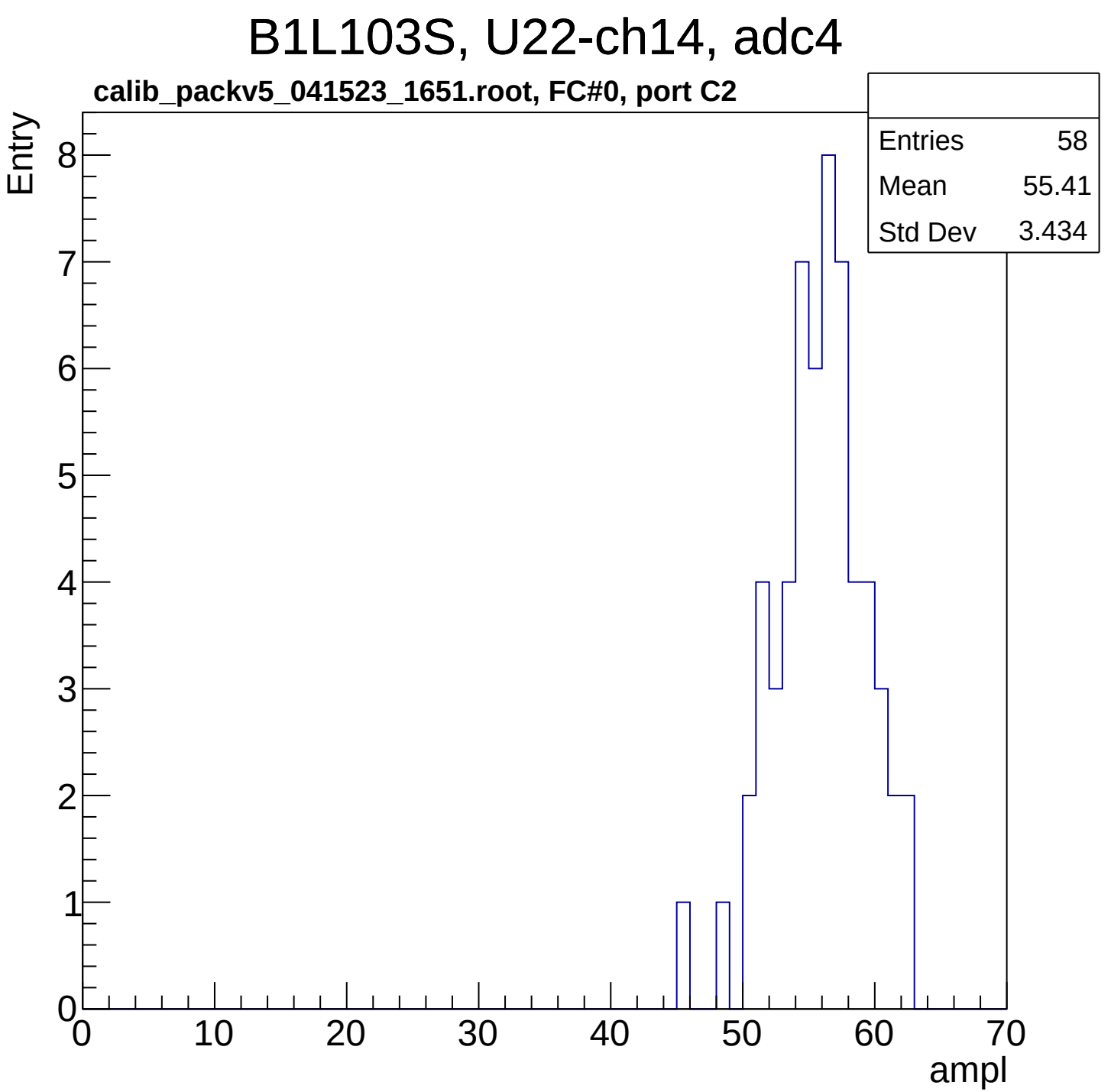
B1L103S, U22-ch14, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 55.41
Std Dev 3.434
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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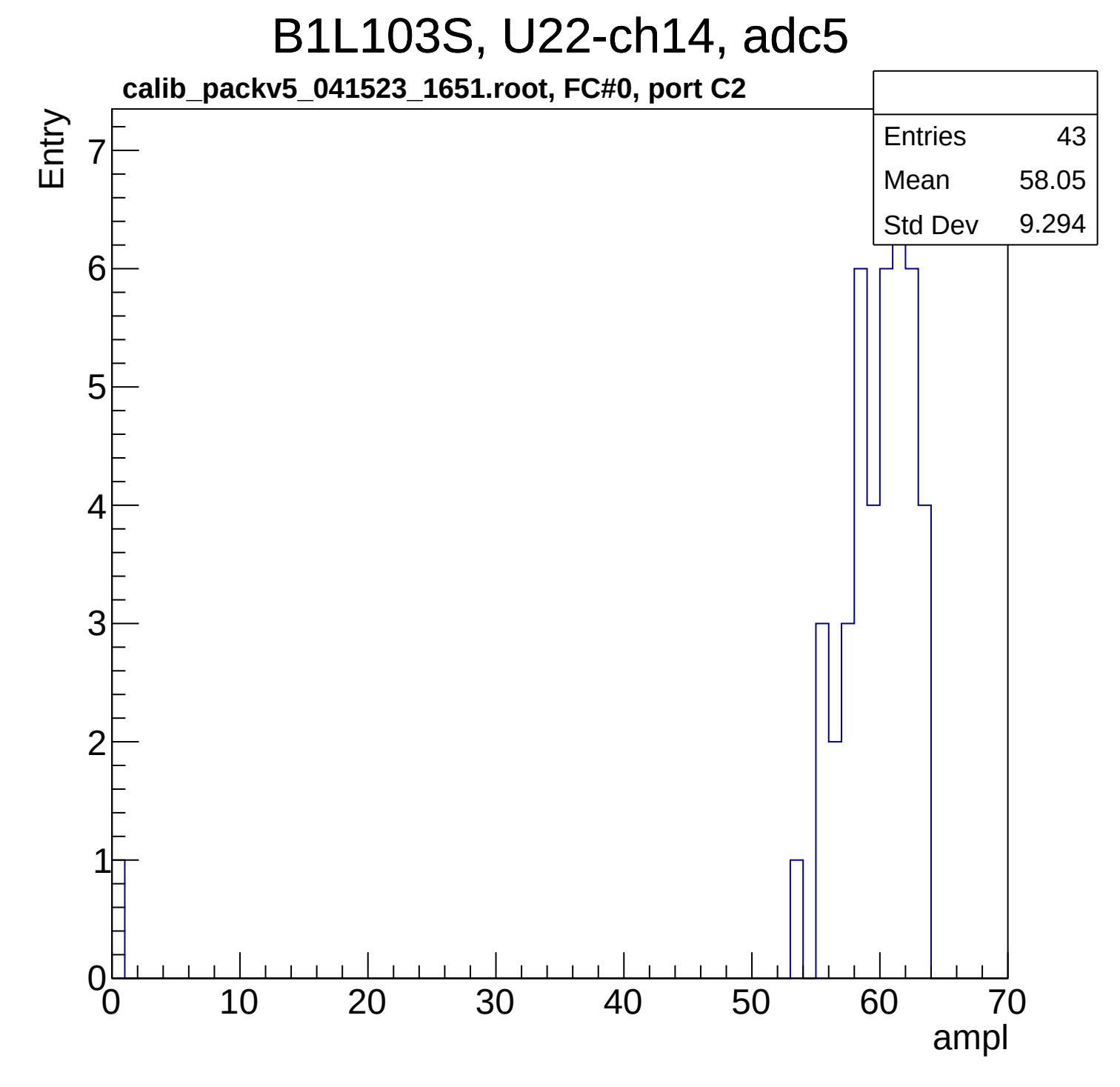
B1L103S, U22-ch14, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 58.05
Std Dev 9.294
Entry
ampl
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1
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3
4
5
6
7
0
10
20
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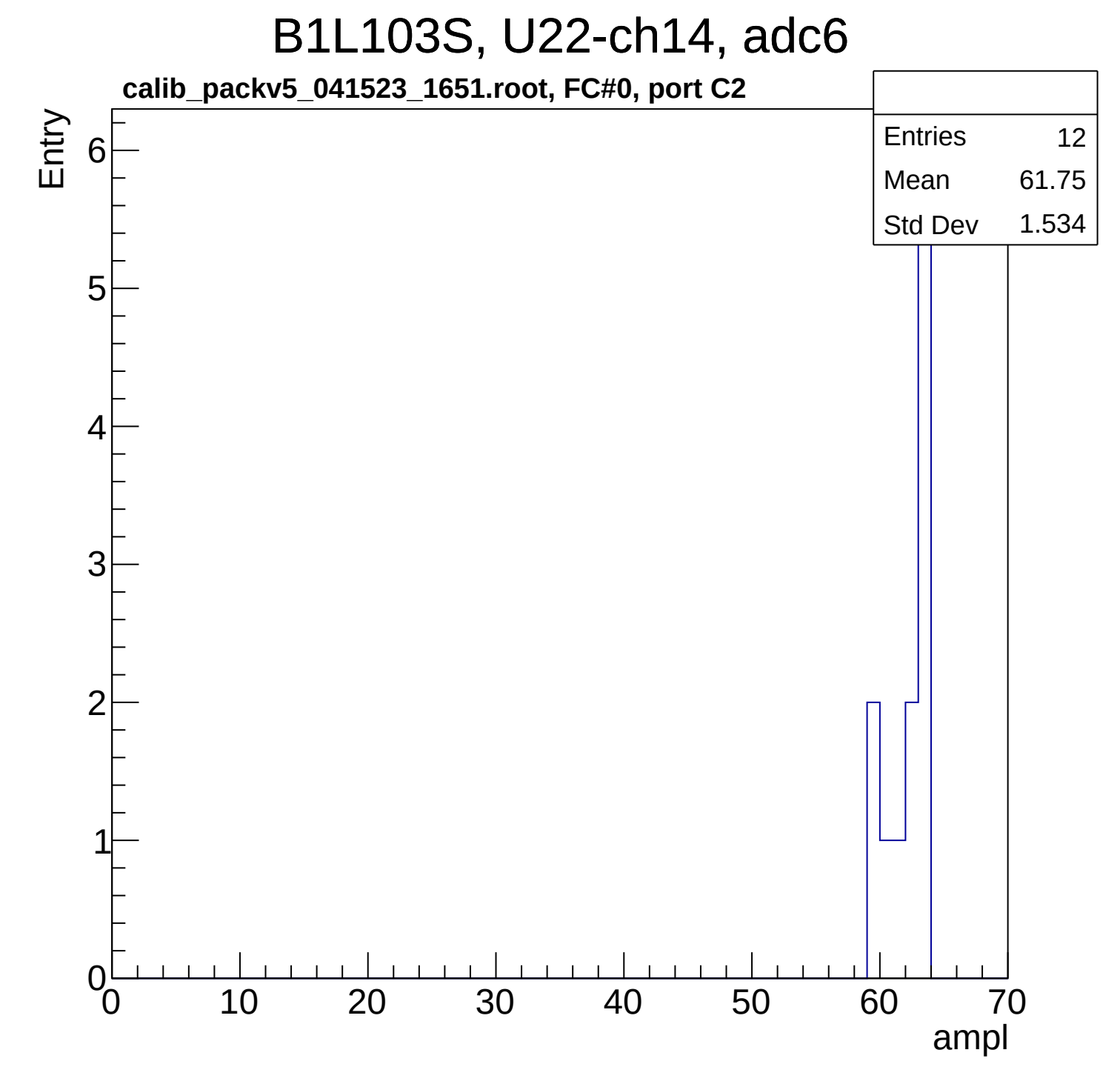
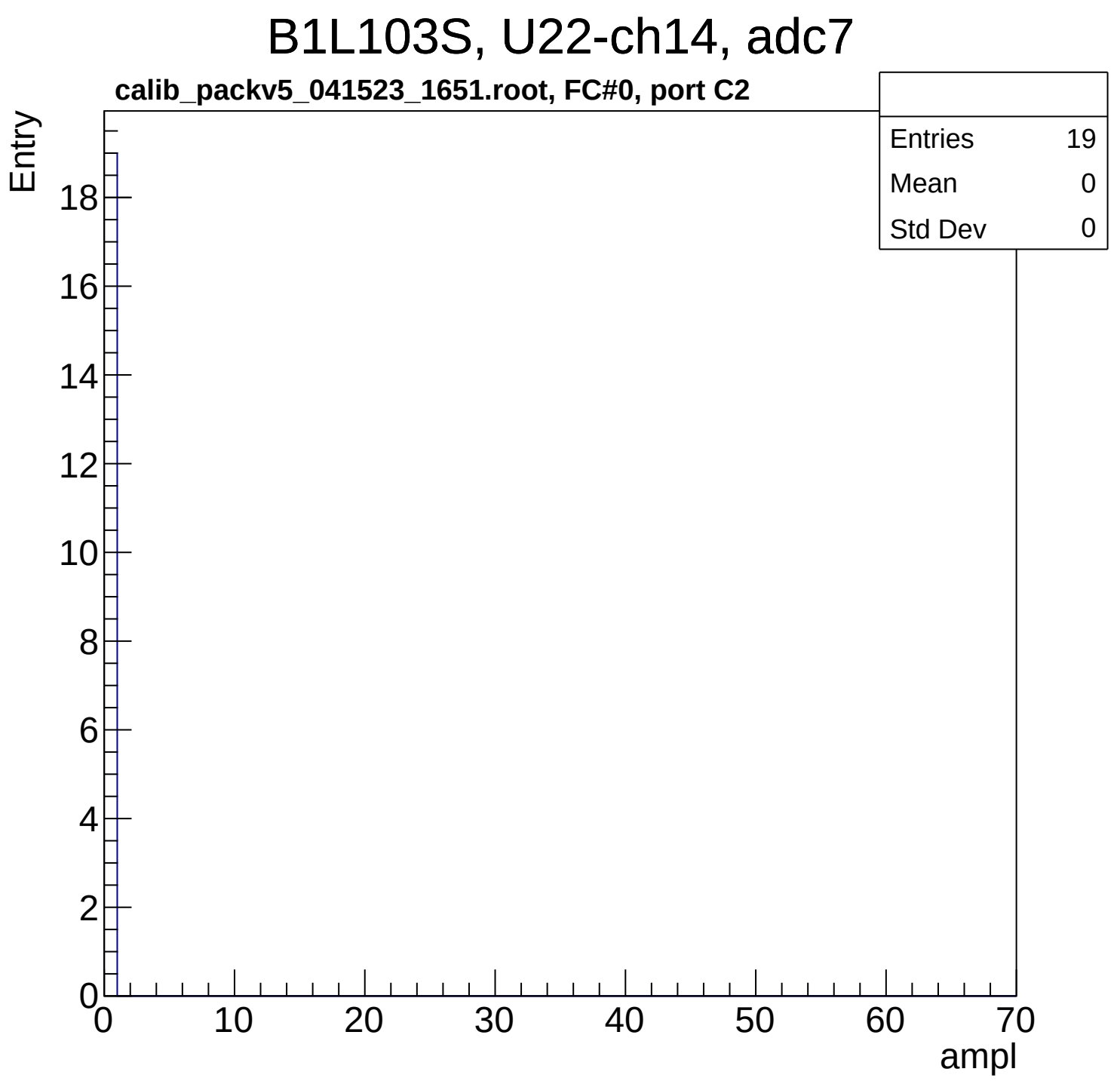
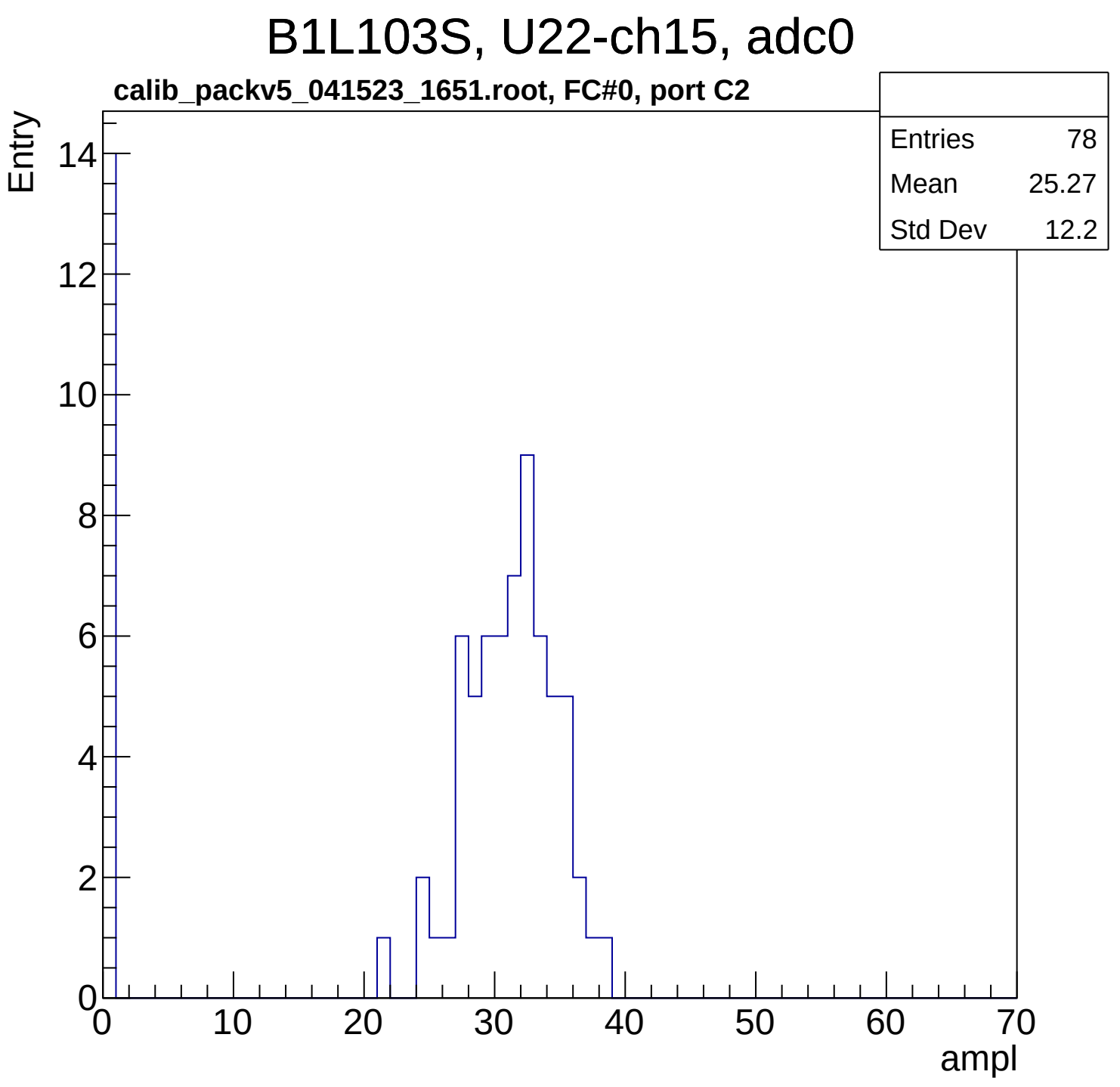
40
50
60
70


B1L103S, U22-ch14, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.75
Std Dev 1.534
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U22-ch14, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch15, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 25.27
Std Dev 12.2
Entry
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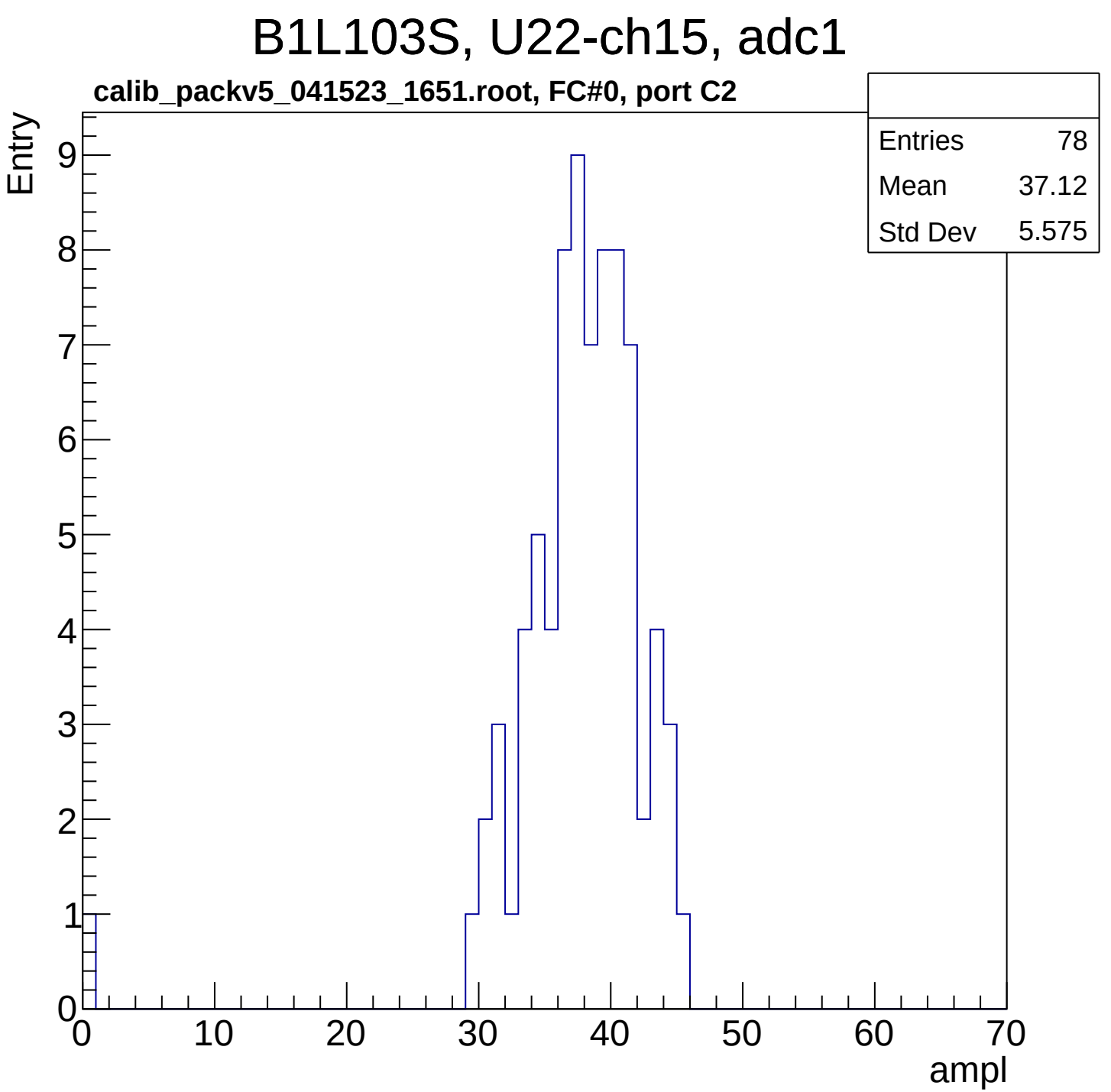
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch15, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 37.12
Std Dev 5.575
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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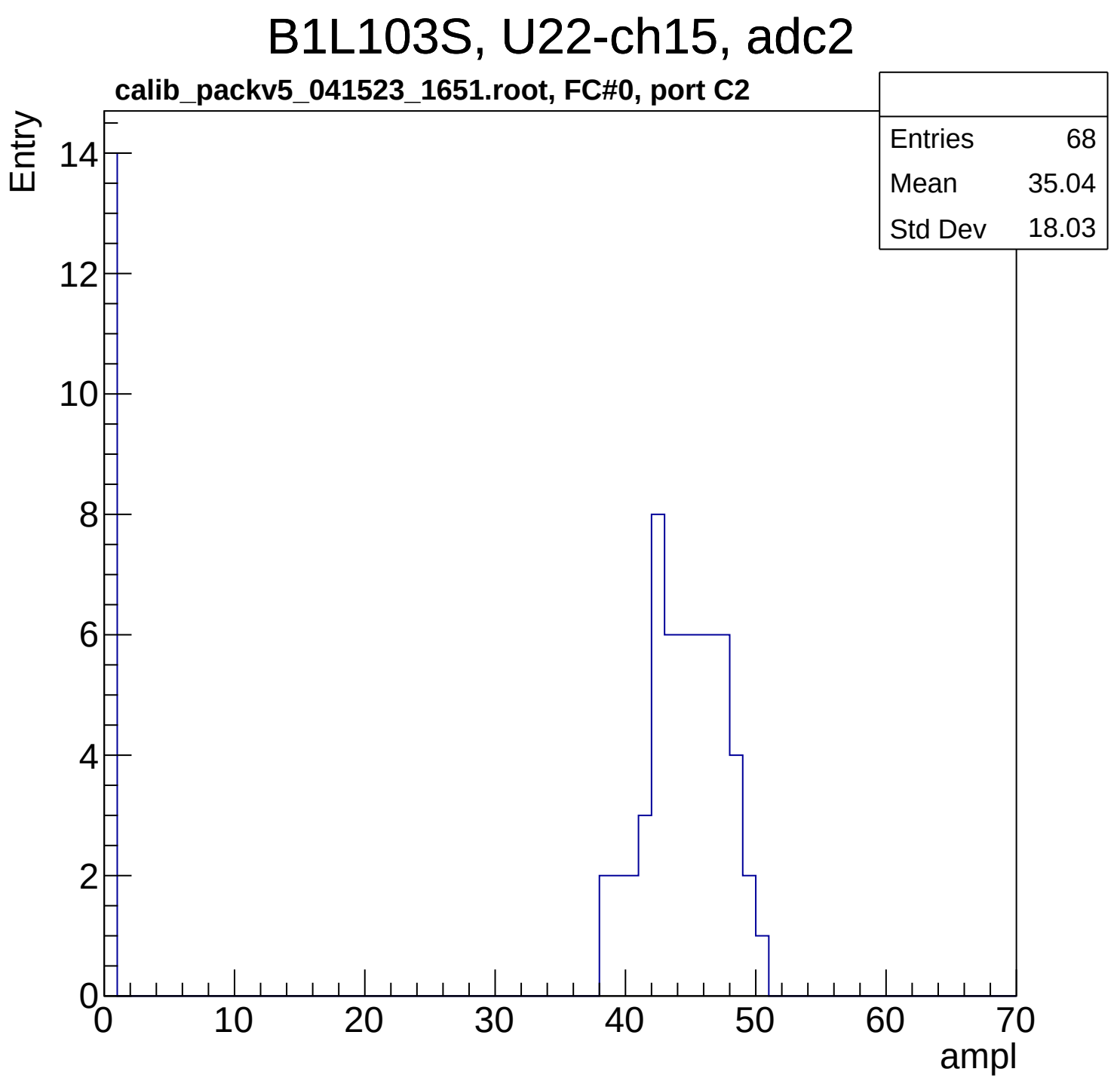
60
70


B1L103S, U22-ch15, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 35.04
Std Dev 18.03
Entry
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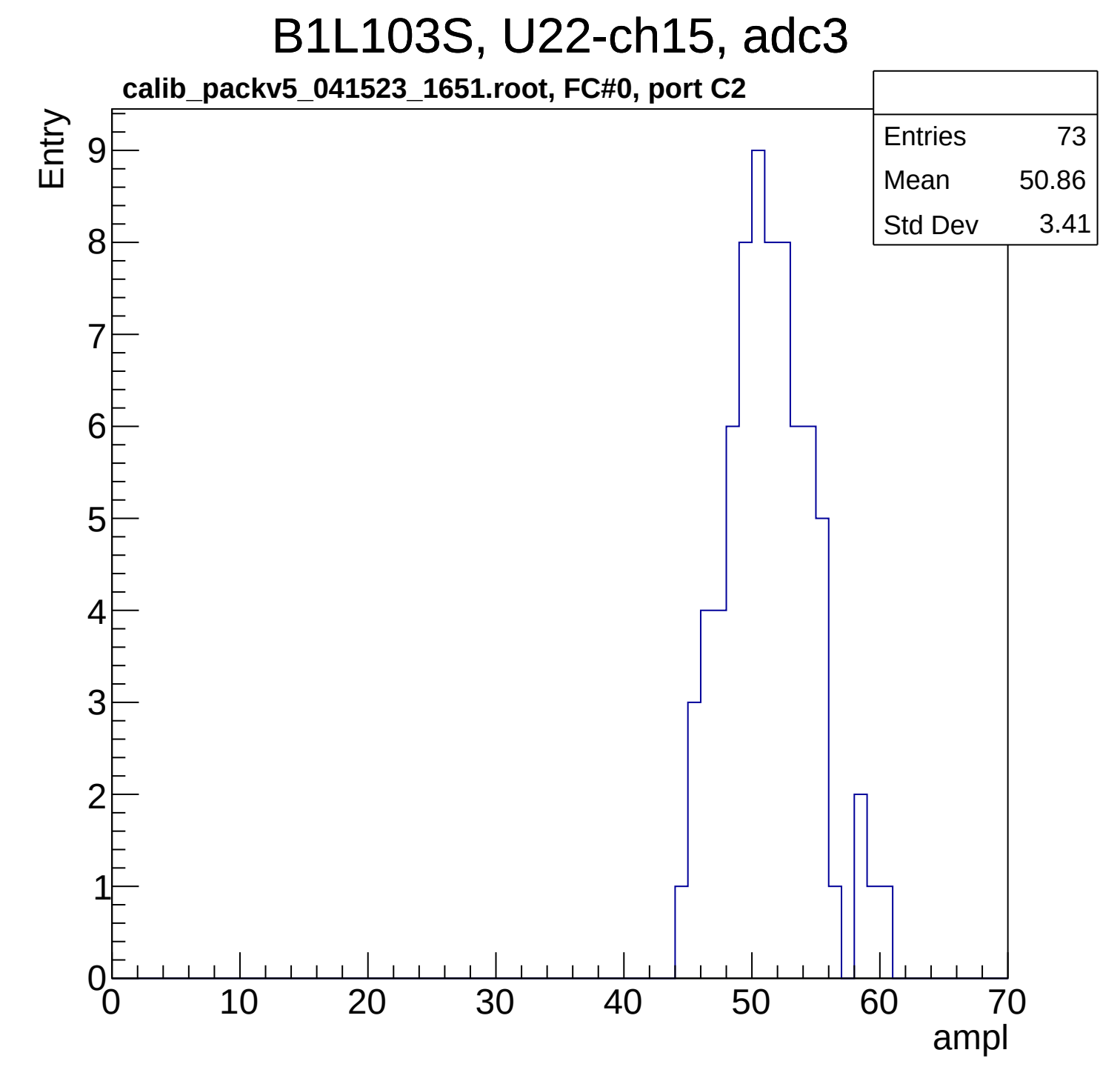
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch15, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 50.86
Std Dev 3.41
Entry
ampl
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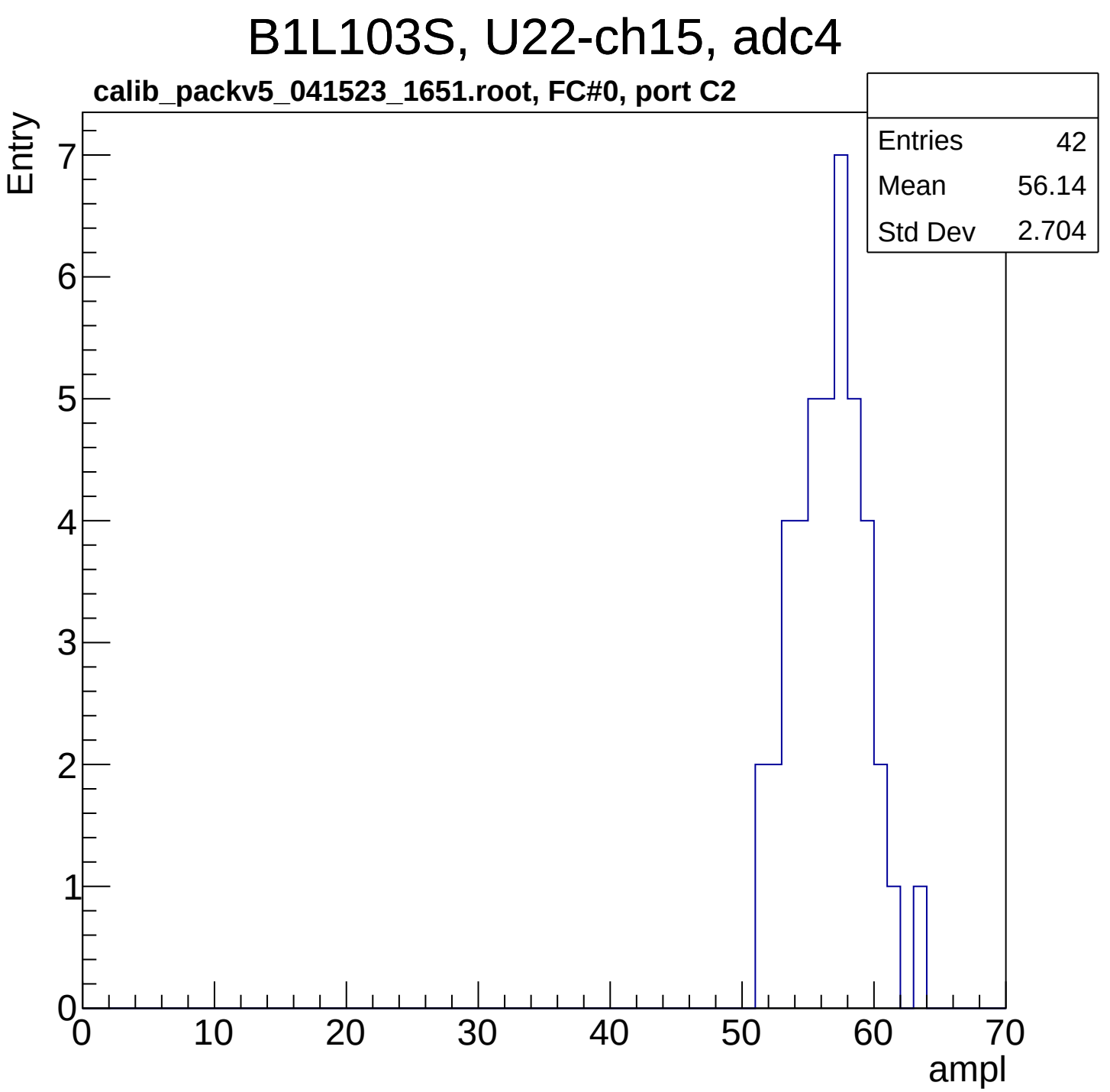
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch15, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 56.14
Std Dev 2.704
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
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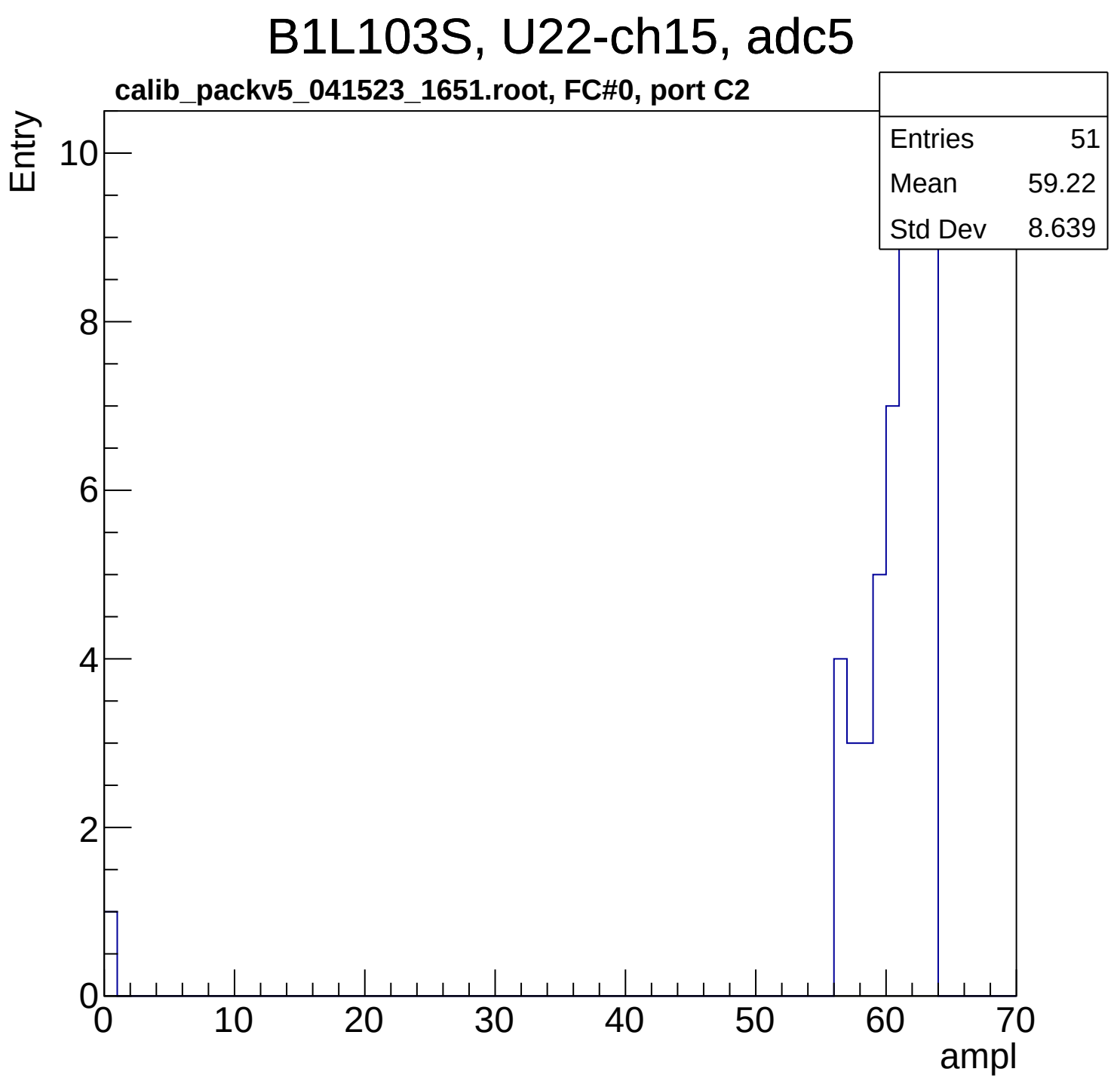
40
50
60
70


B1L103S, U22-ch15, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 59.22
Std Dev 8.639
Entry
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2
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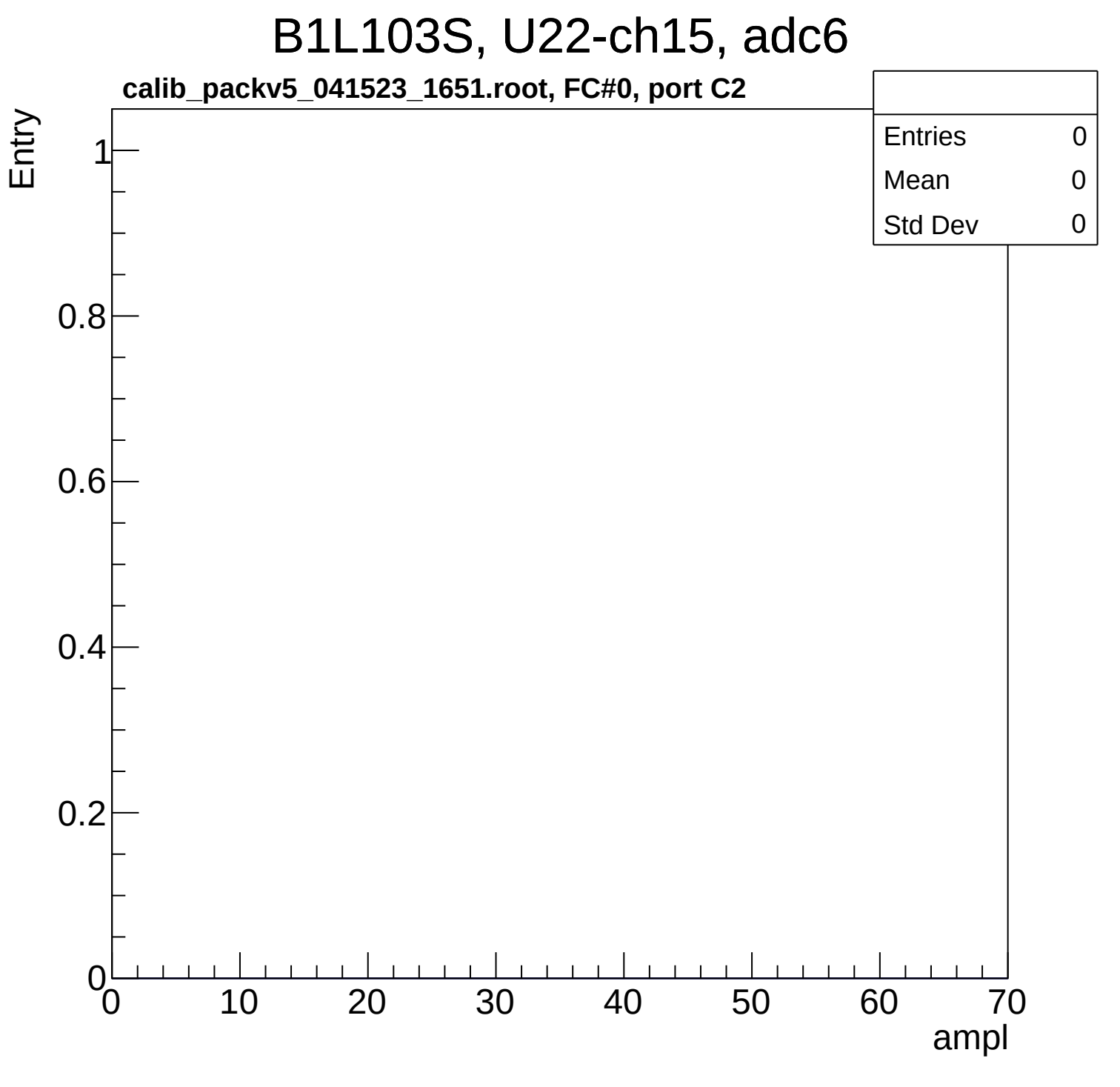
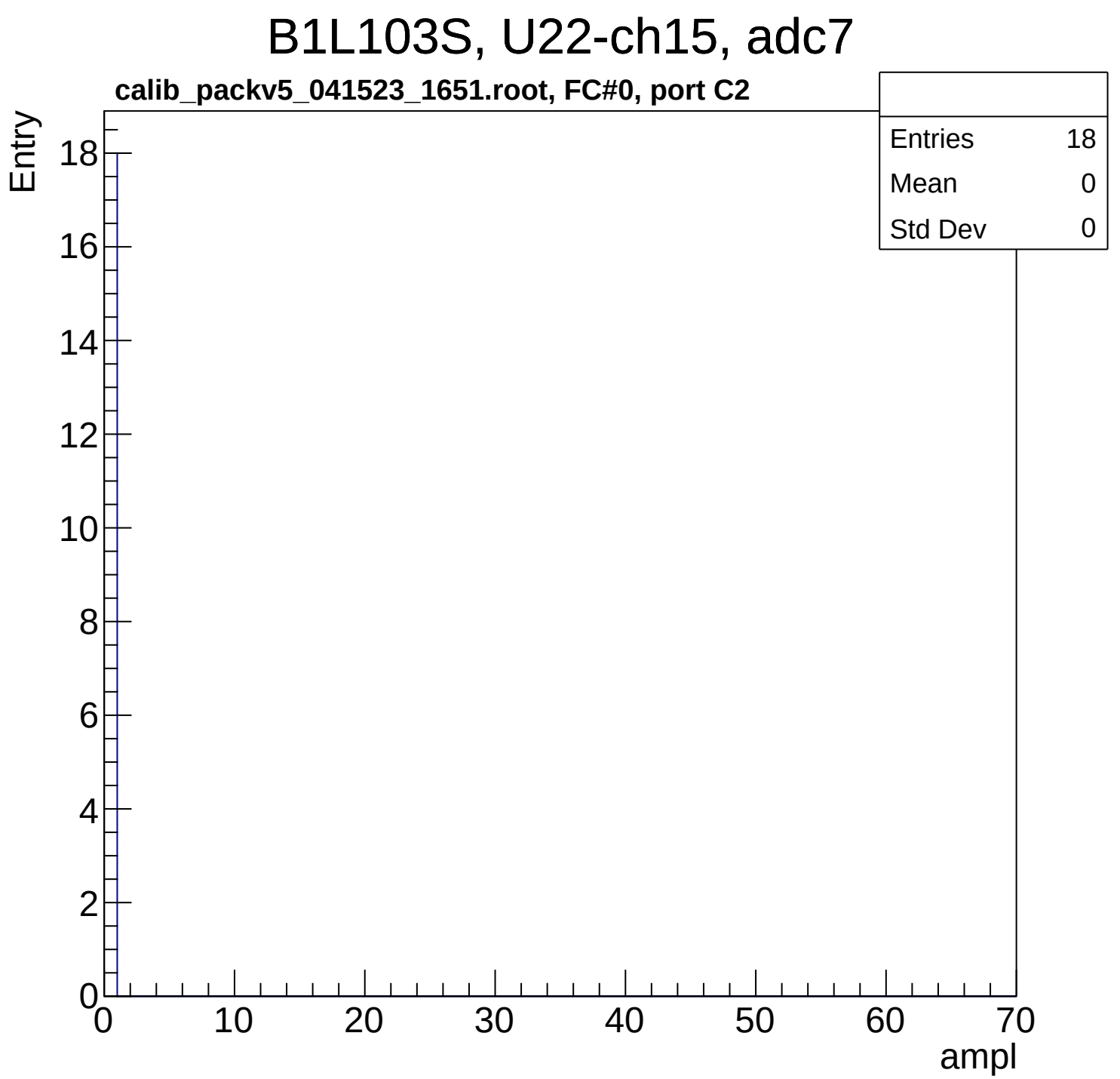
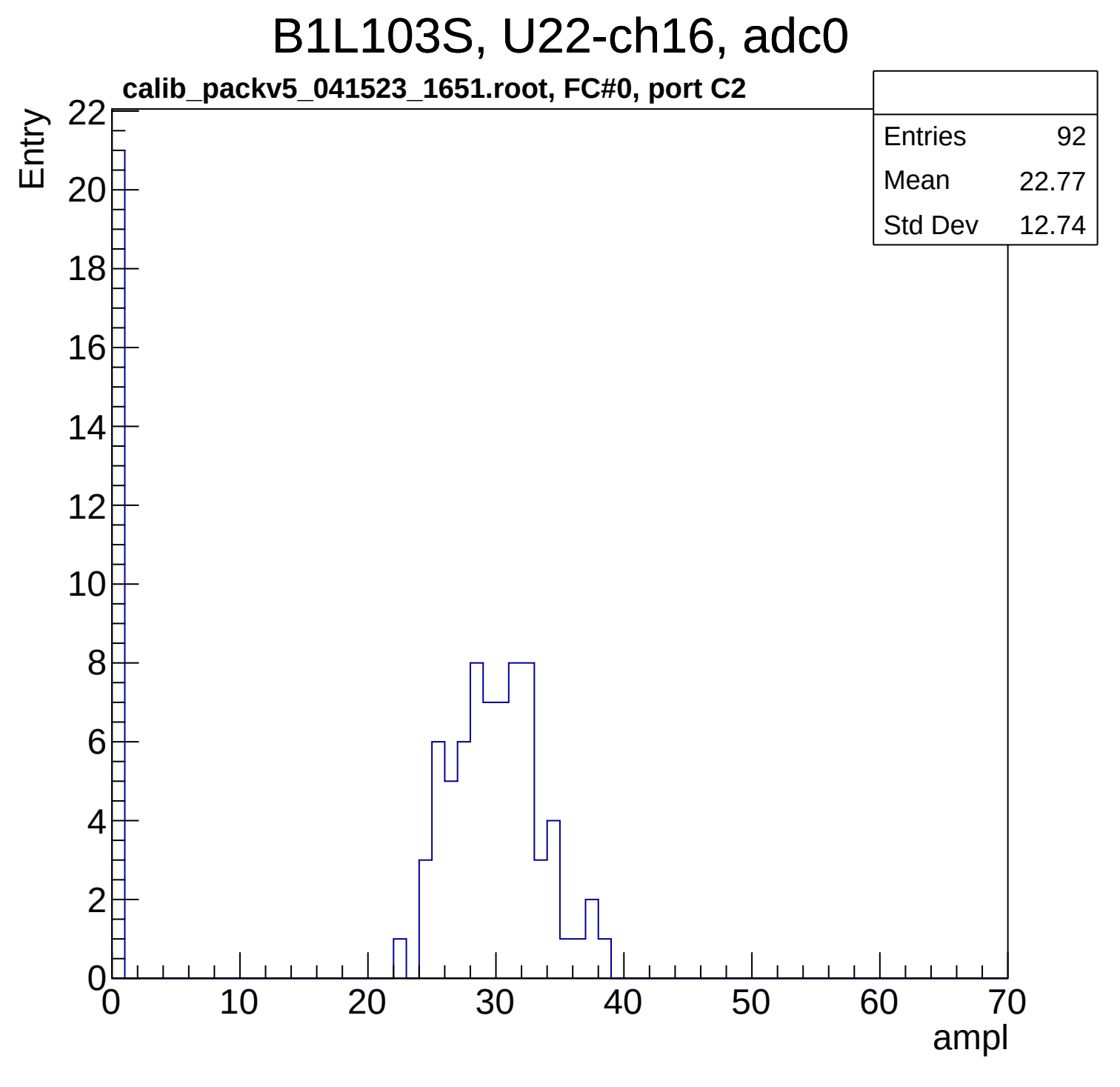
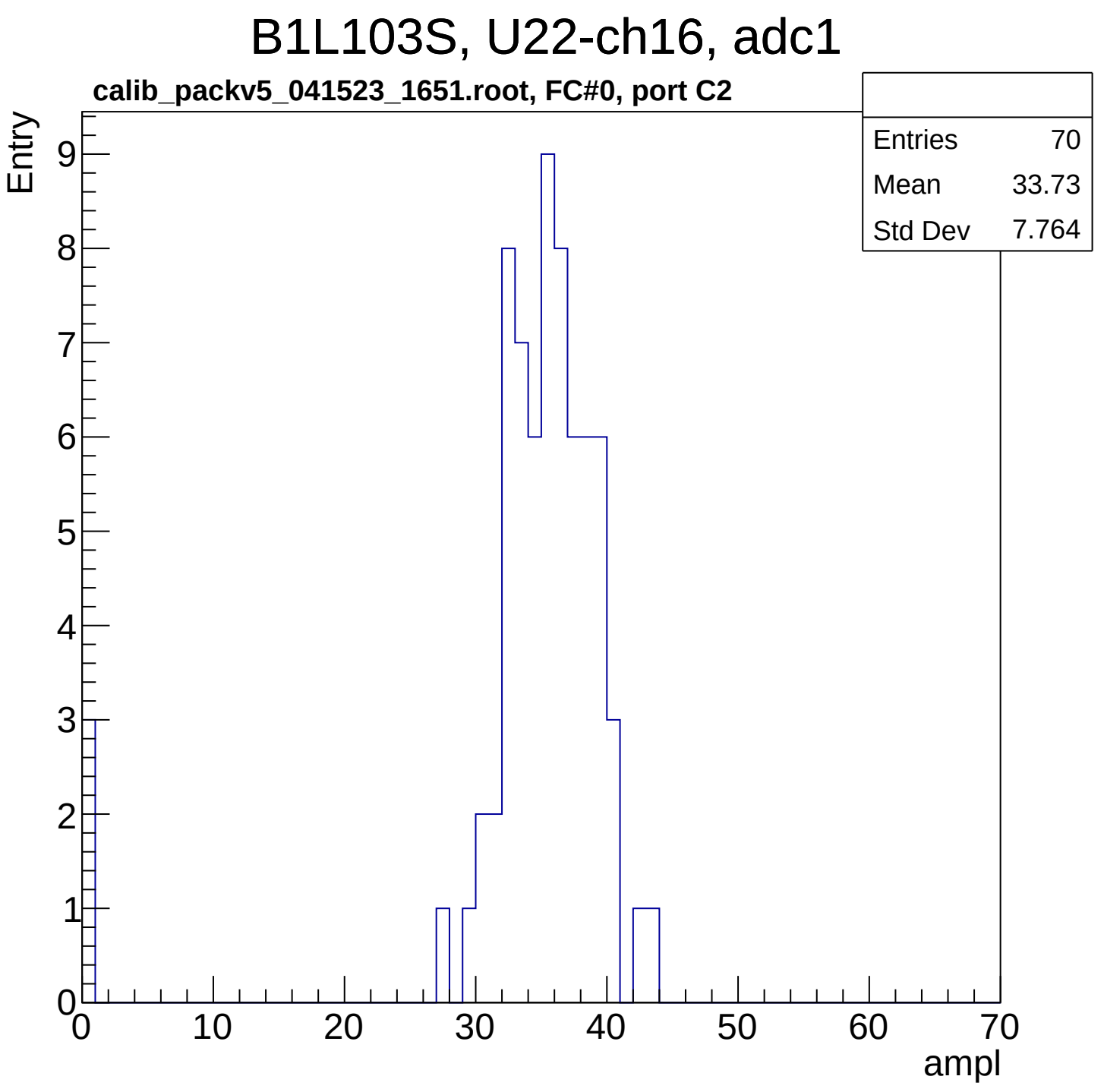
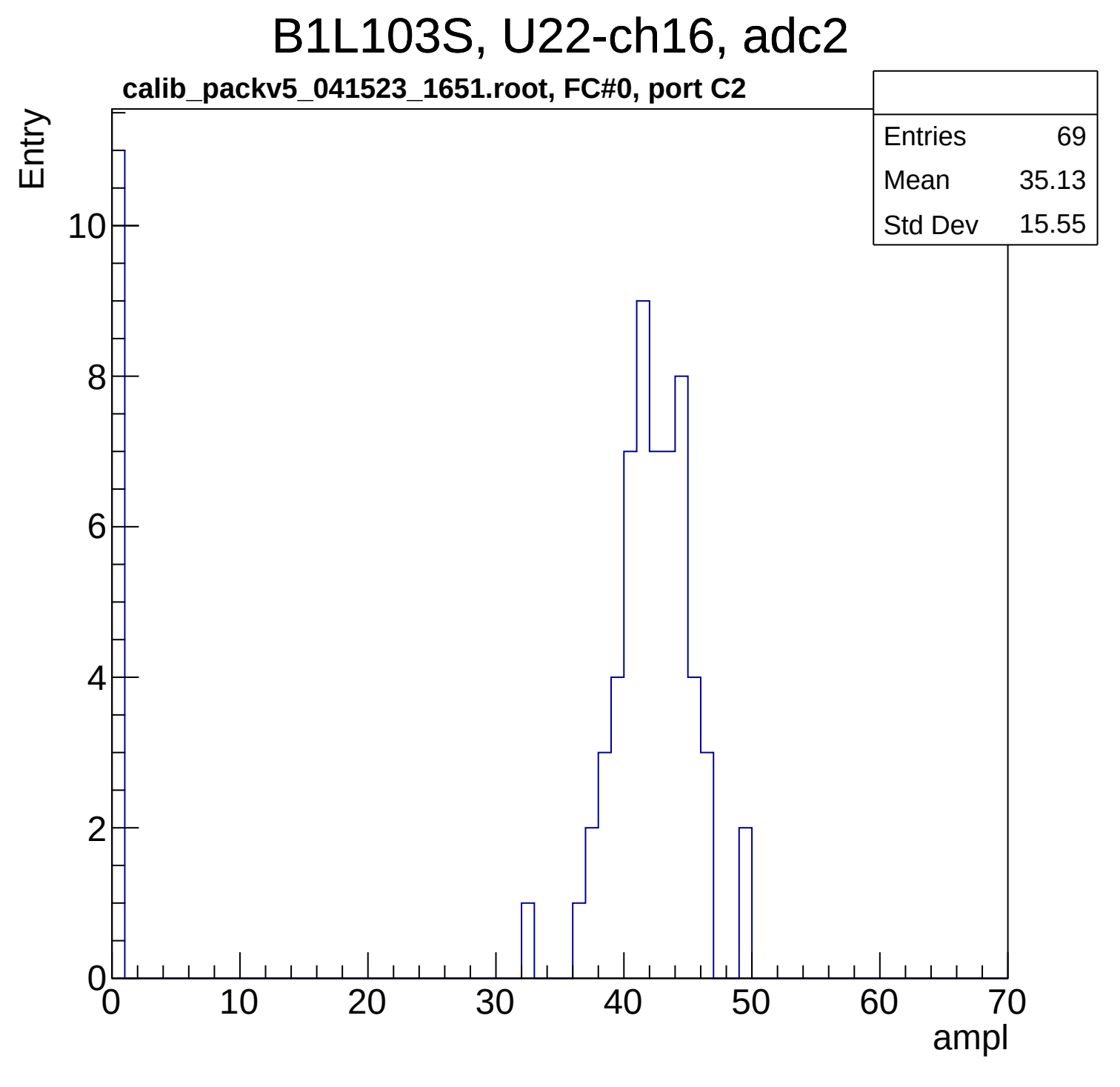
6
8
10
0
10
20
30
40
50
60
70
ampl

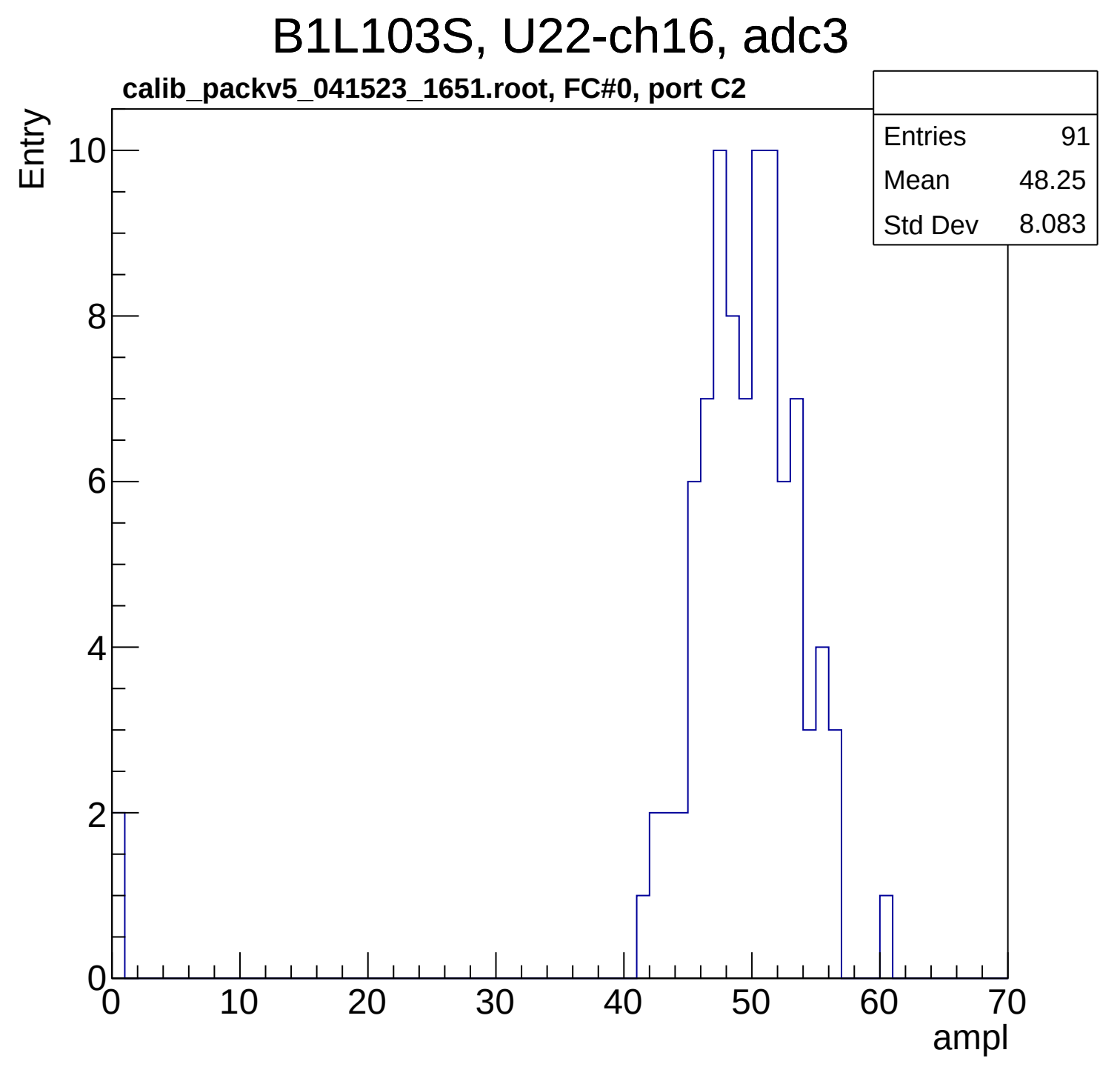

B1L103S, U22-ch15, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

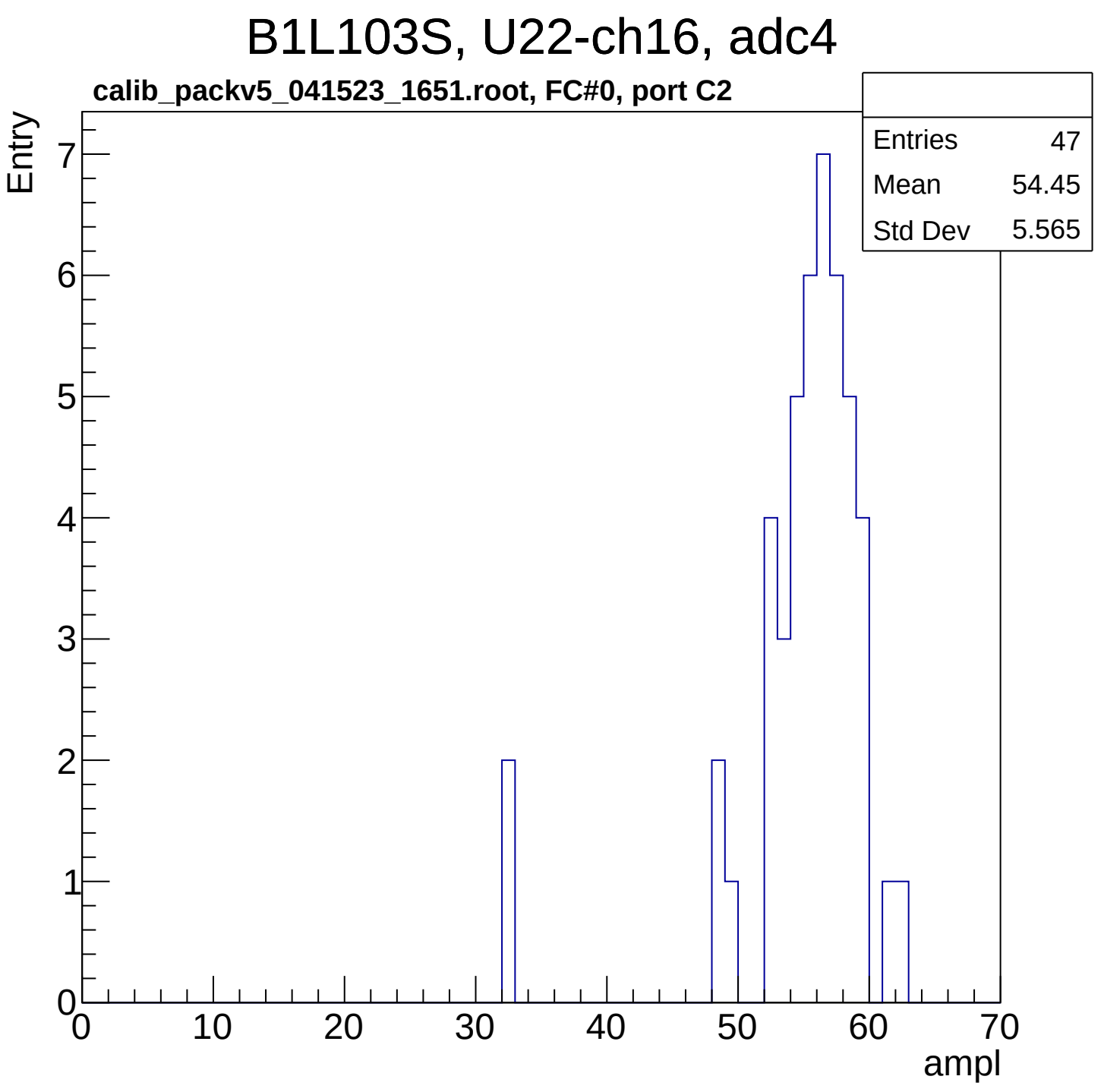

B1L103S, U22-ch15, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

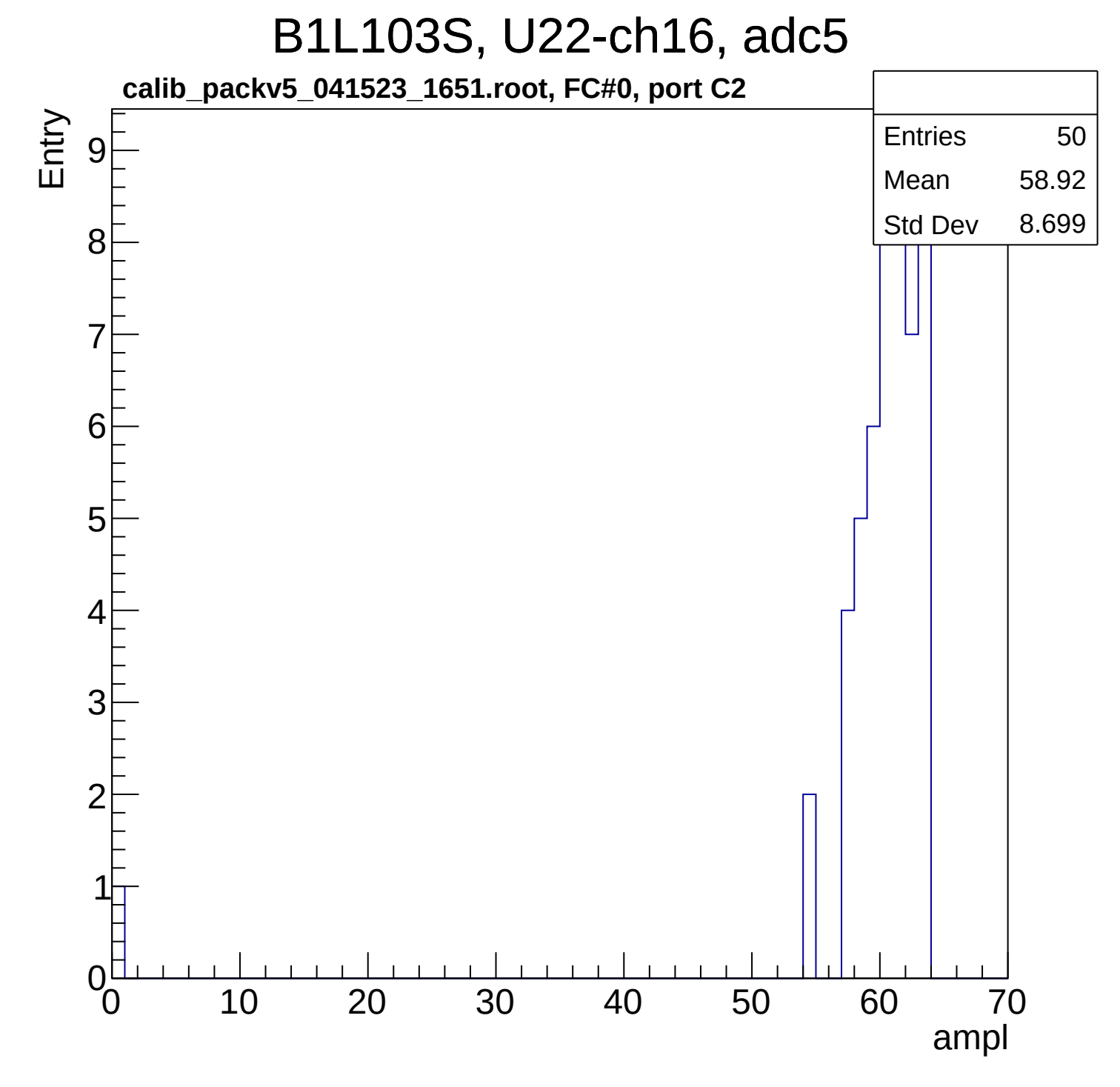

B1L103S, U22-ch16, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 22.77
Std Dev 12.74
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70

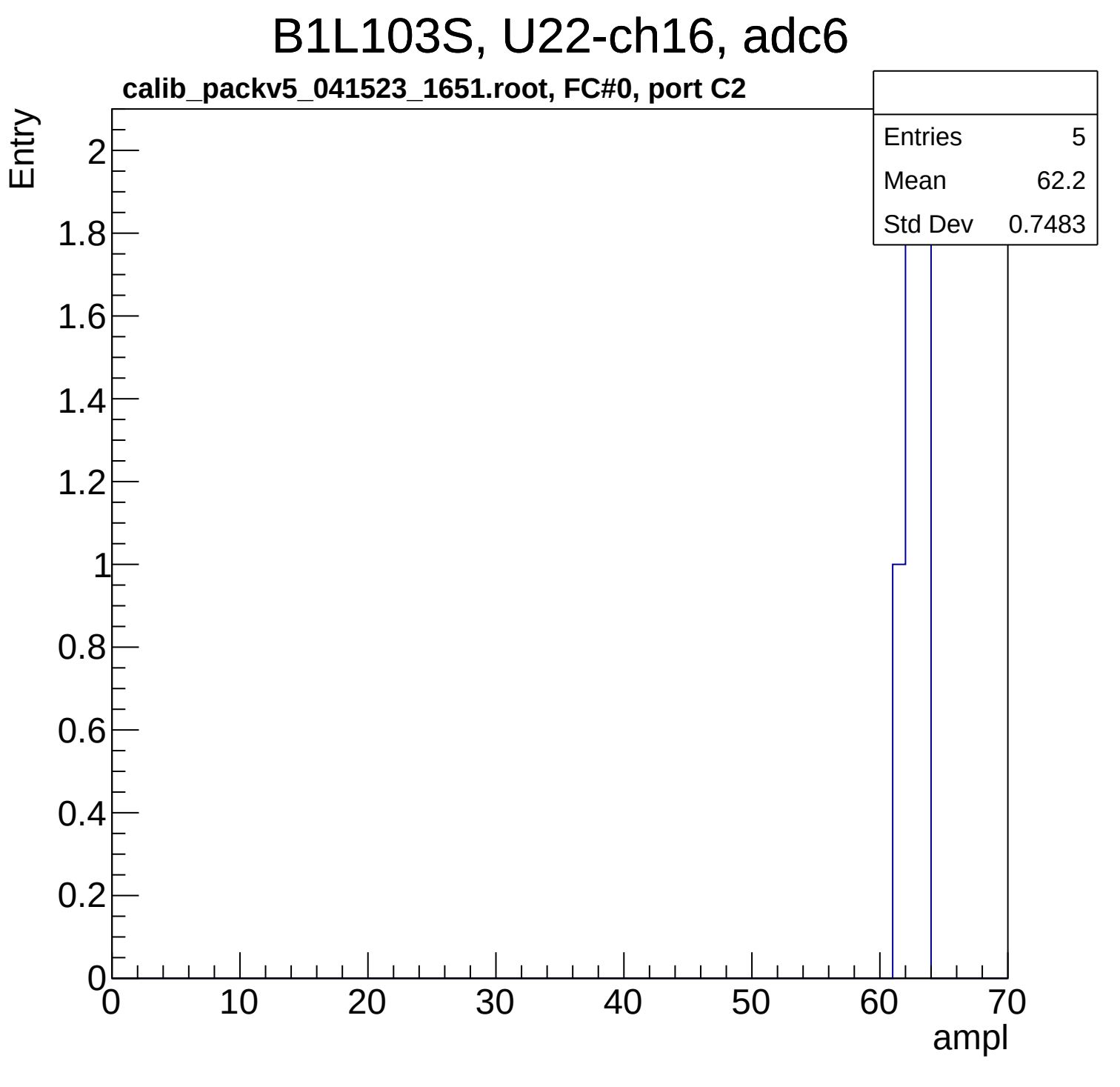

B1L103S, U22-ch16, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 33.73
Std Dev 7.764
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

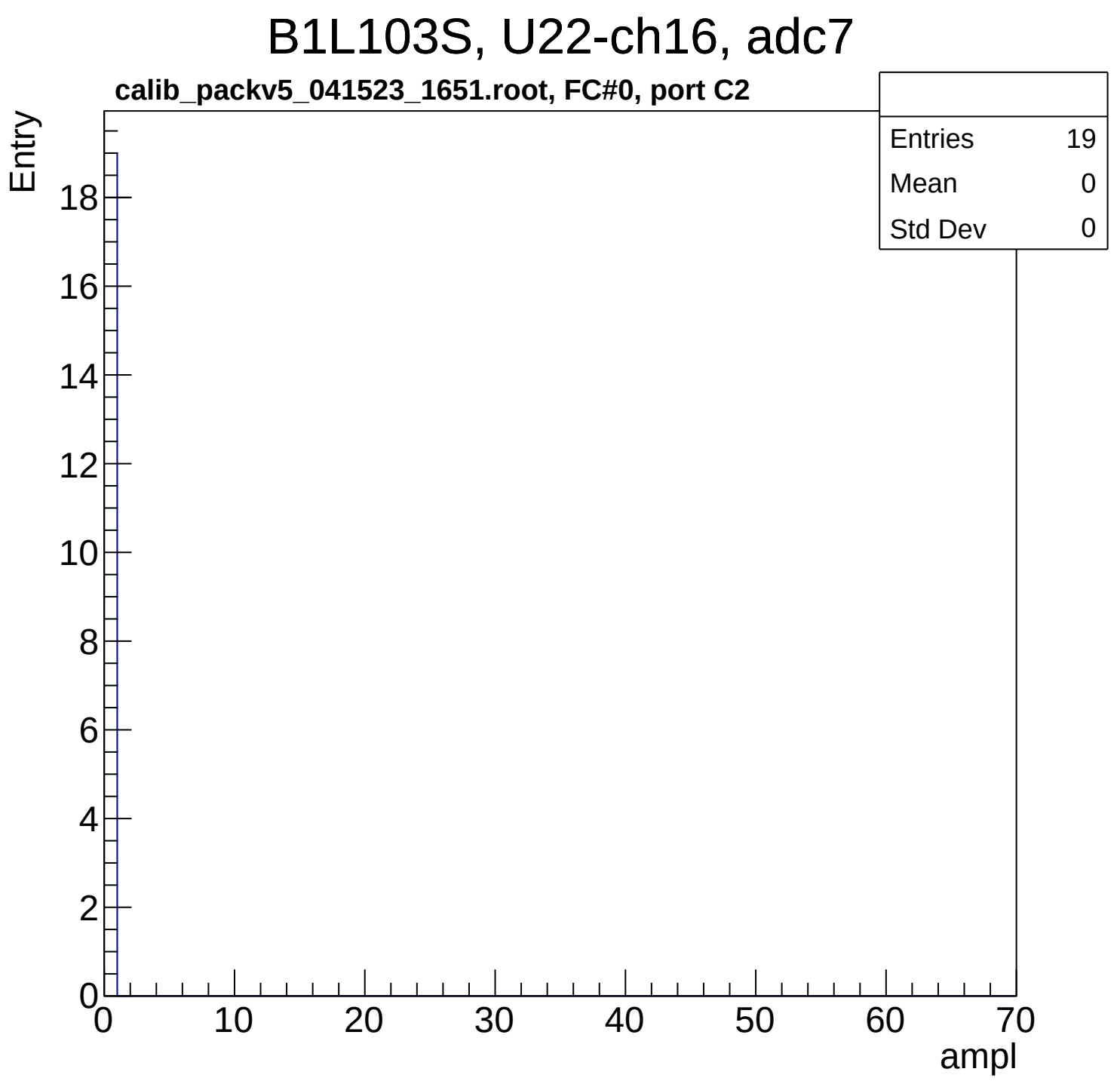

B1L103S, U22-ch16, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 35.13
Std Dev 15.55
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

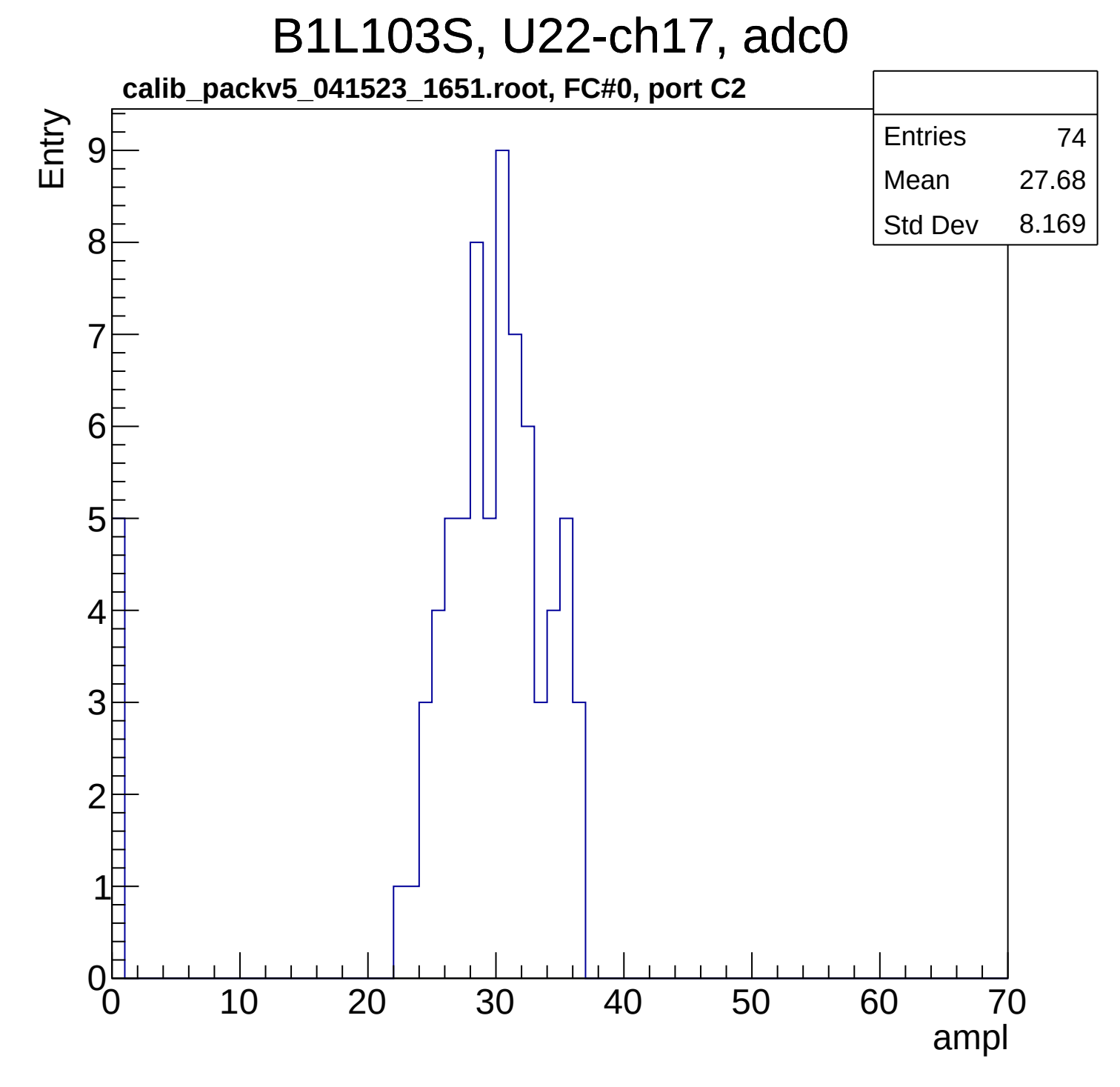

B1L103S, U22-ch16, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 48.25
Std Dev 8.083
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

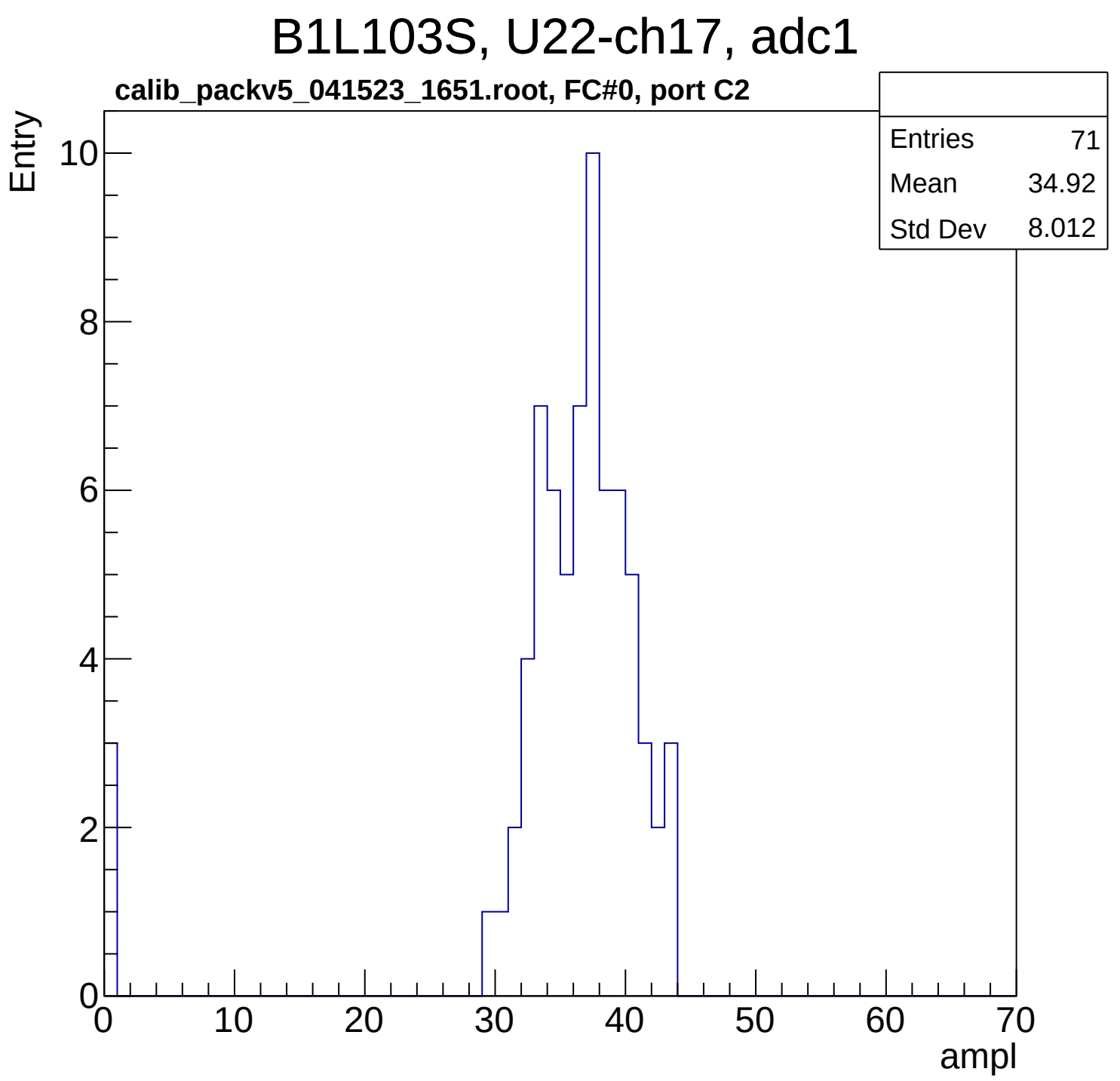

B1L103S, U22-ch16, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 54.45
Std Dev 5.565
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

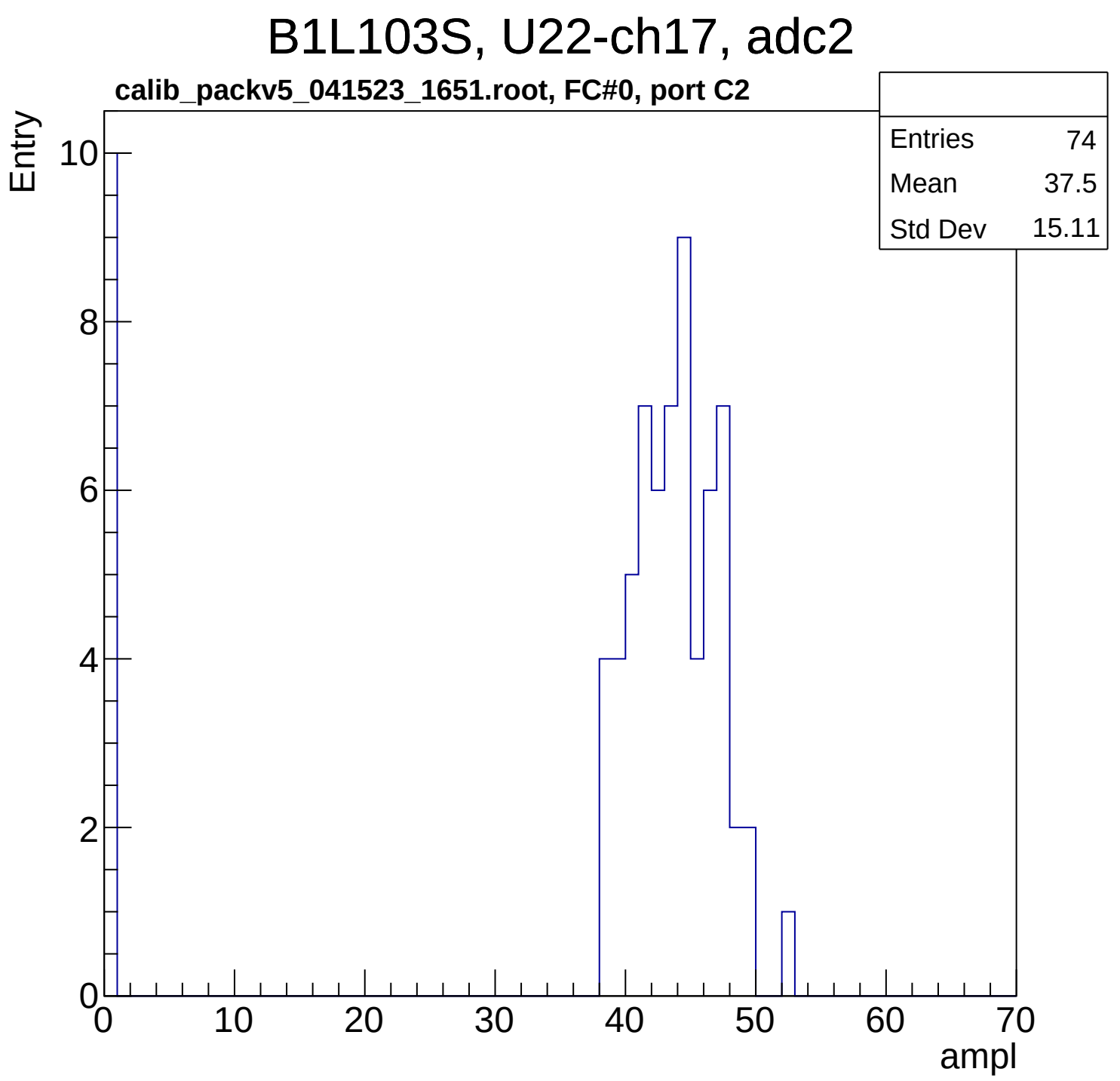

B1L103S, U22-ch16, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 58.92
Std Dev 8.699
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

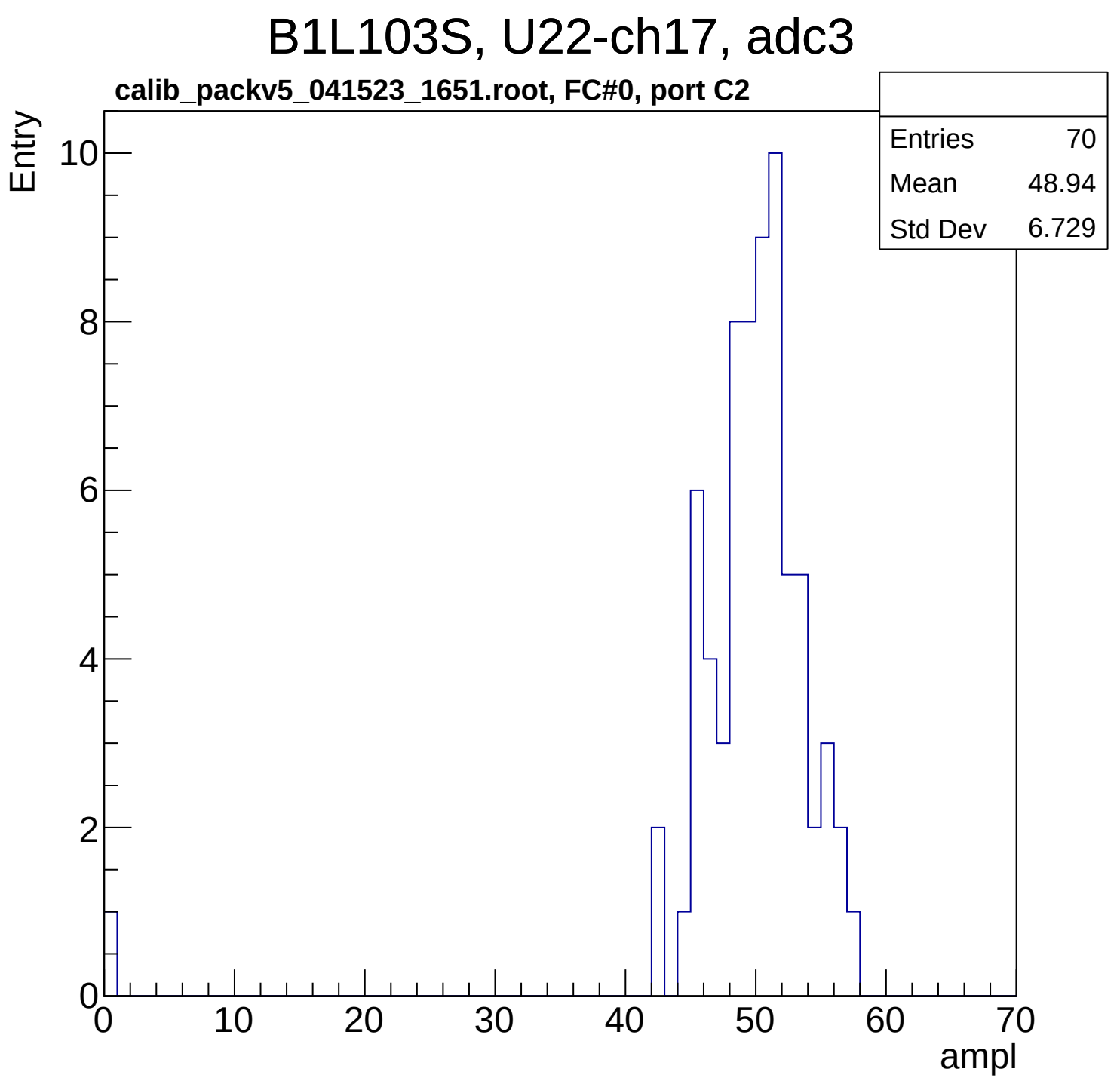

B1L103S, U22-ch16, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 62.2
Std Dev 0.7483
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

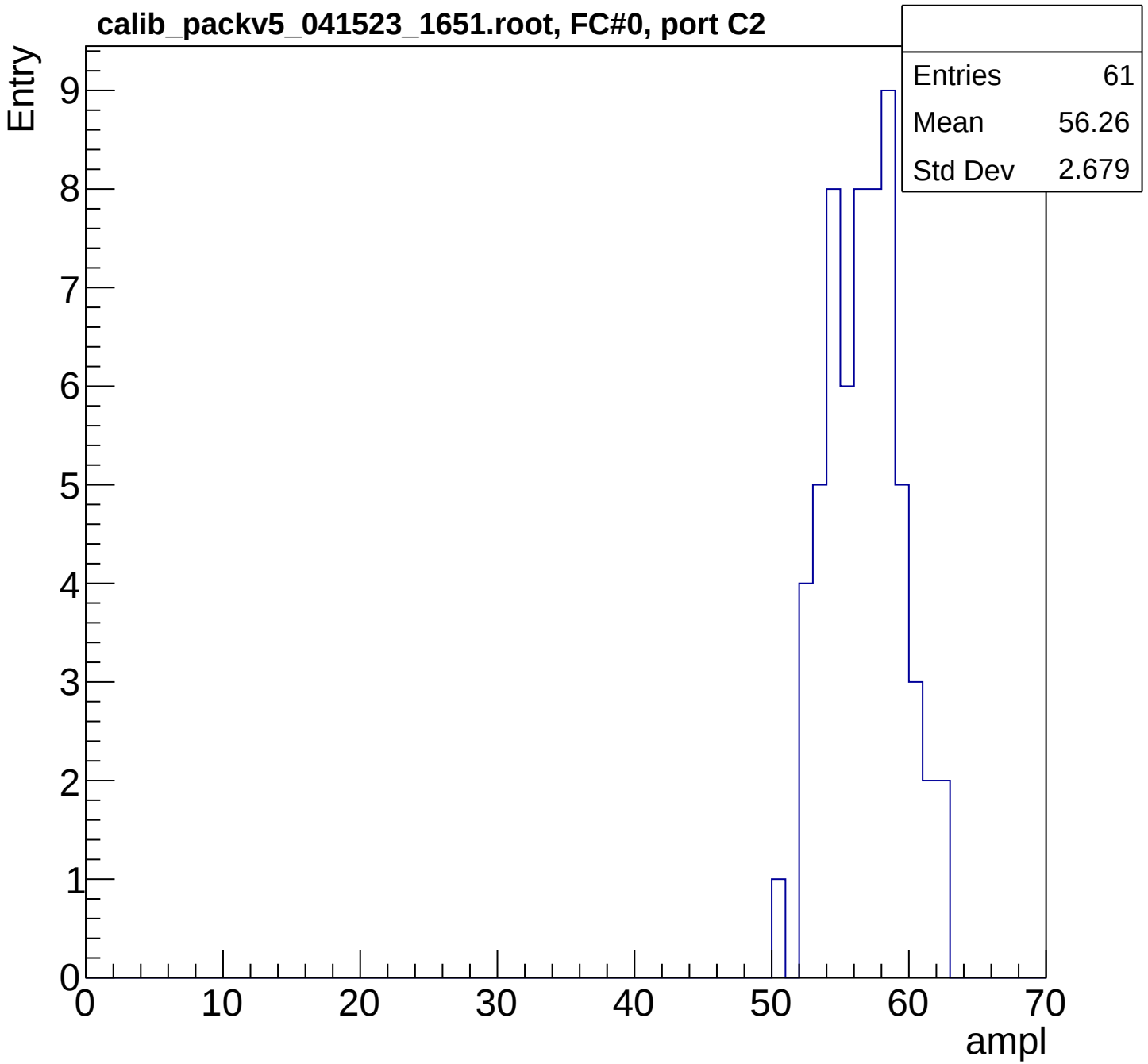

B1L103S, U22-ch16, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

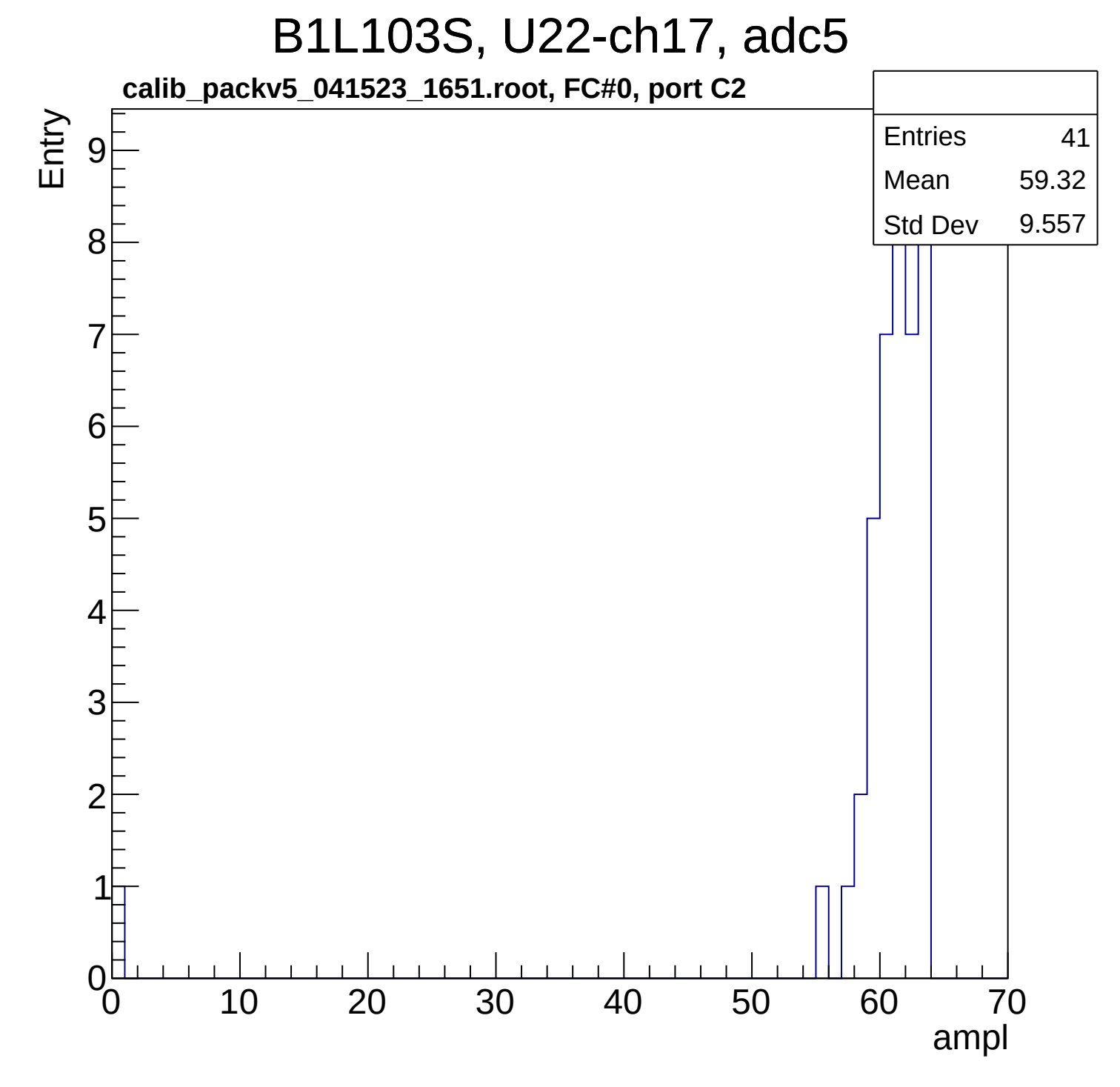

B1L103S, U22-ch17, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 27.68
Std Dev 8.169
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

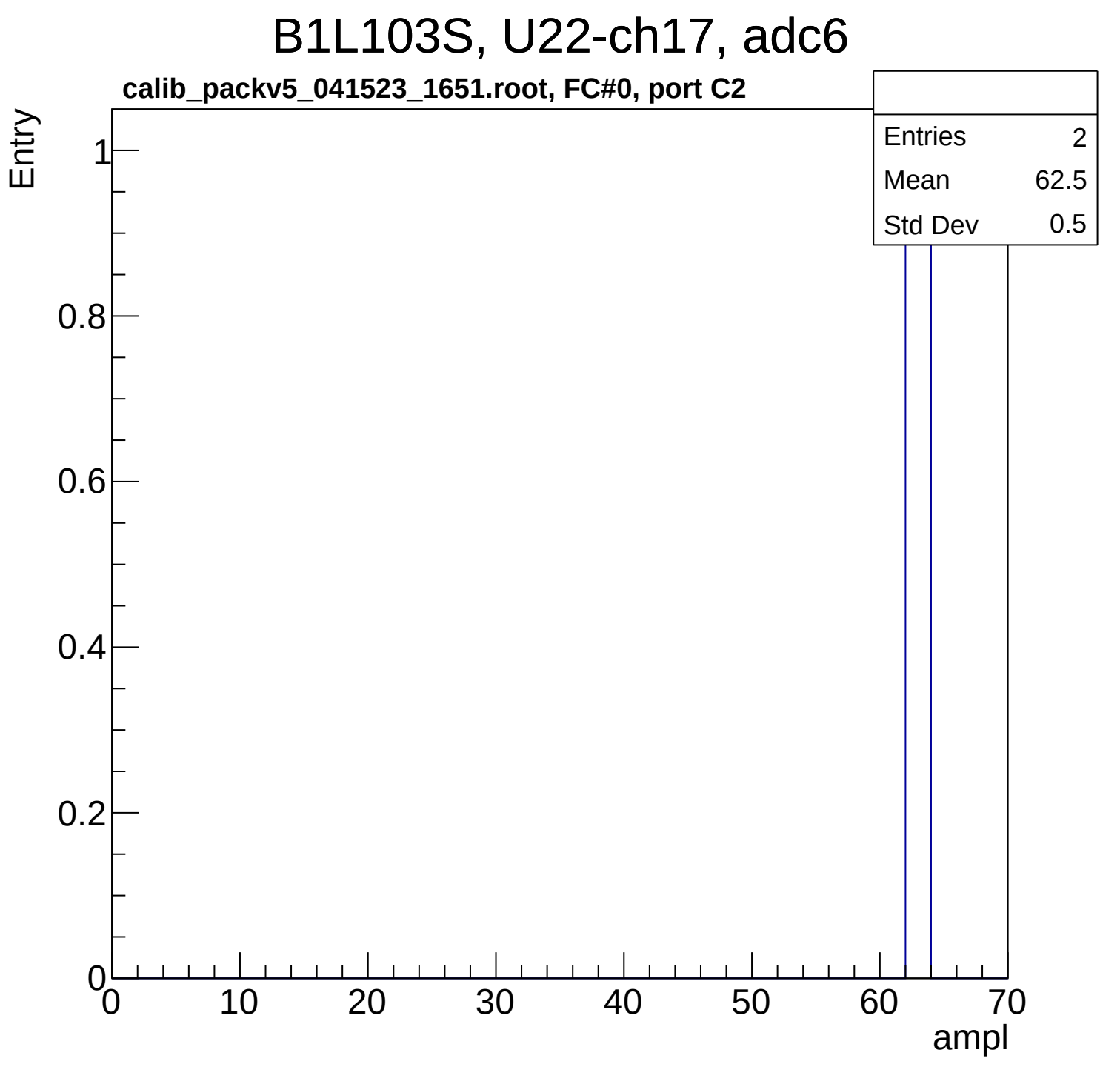

B1L103S, U22-ch17, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 34.92
Std Dev 8.012
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

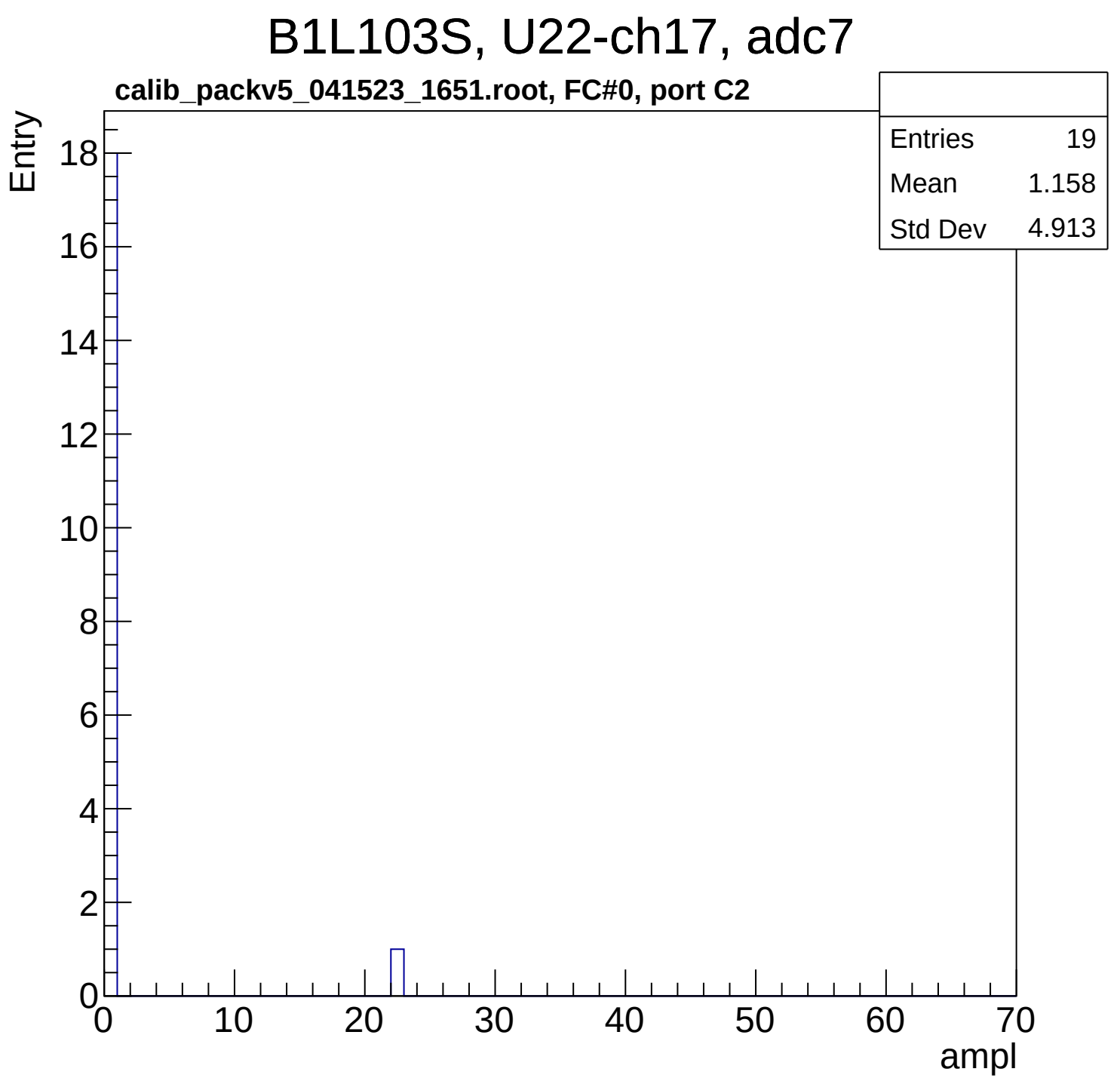

B1L103S, U22-ch17, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 37.5
Std Dev 15.11
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

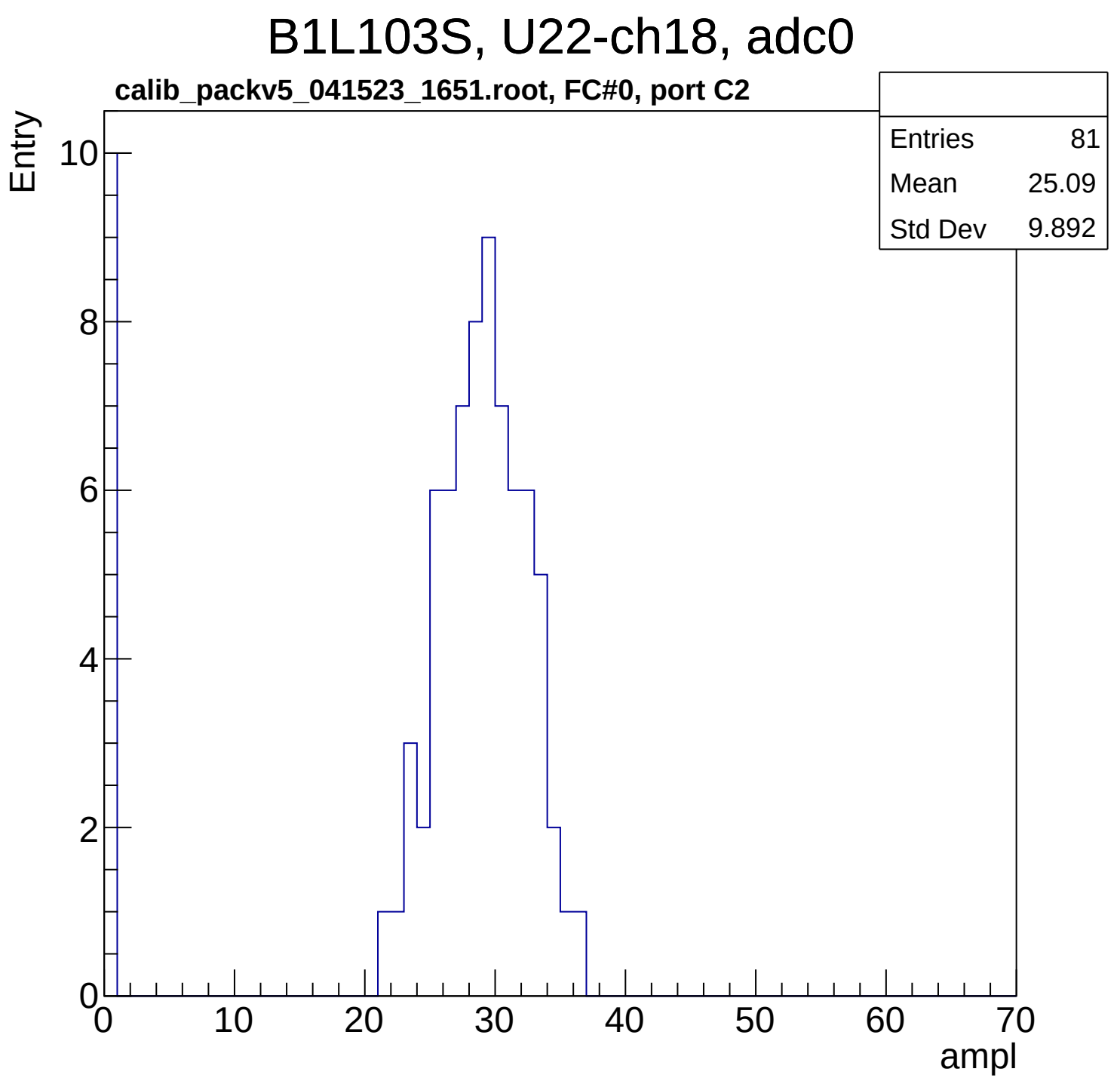

B1L103S, U22-ch17, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 48.94
Std Dev 6.729
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

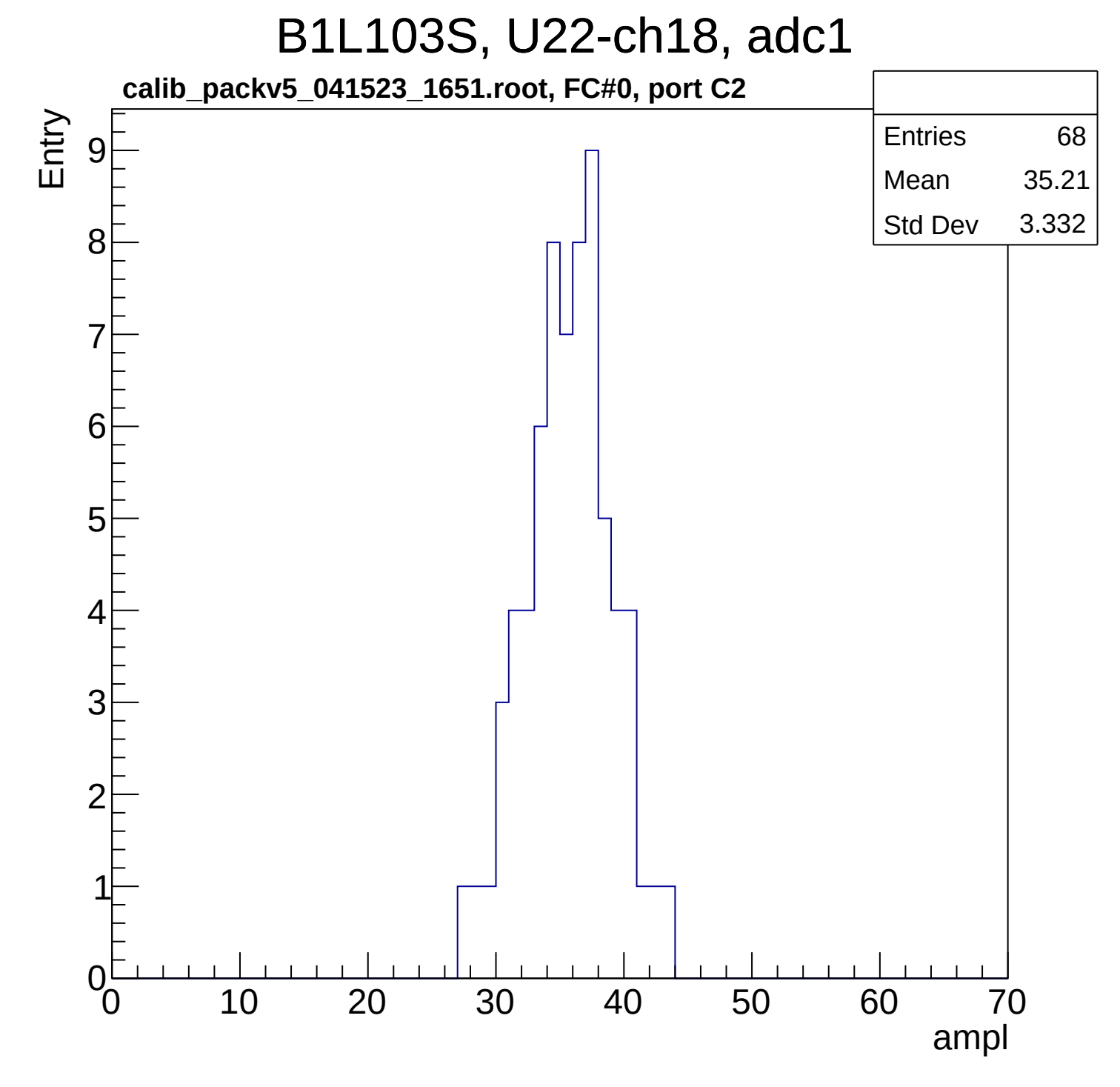

B1L103S, U22-ch17, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 56.26
Std Dev 2.679
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

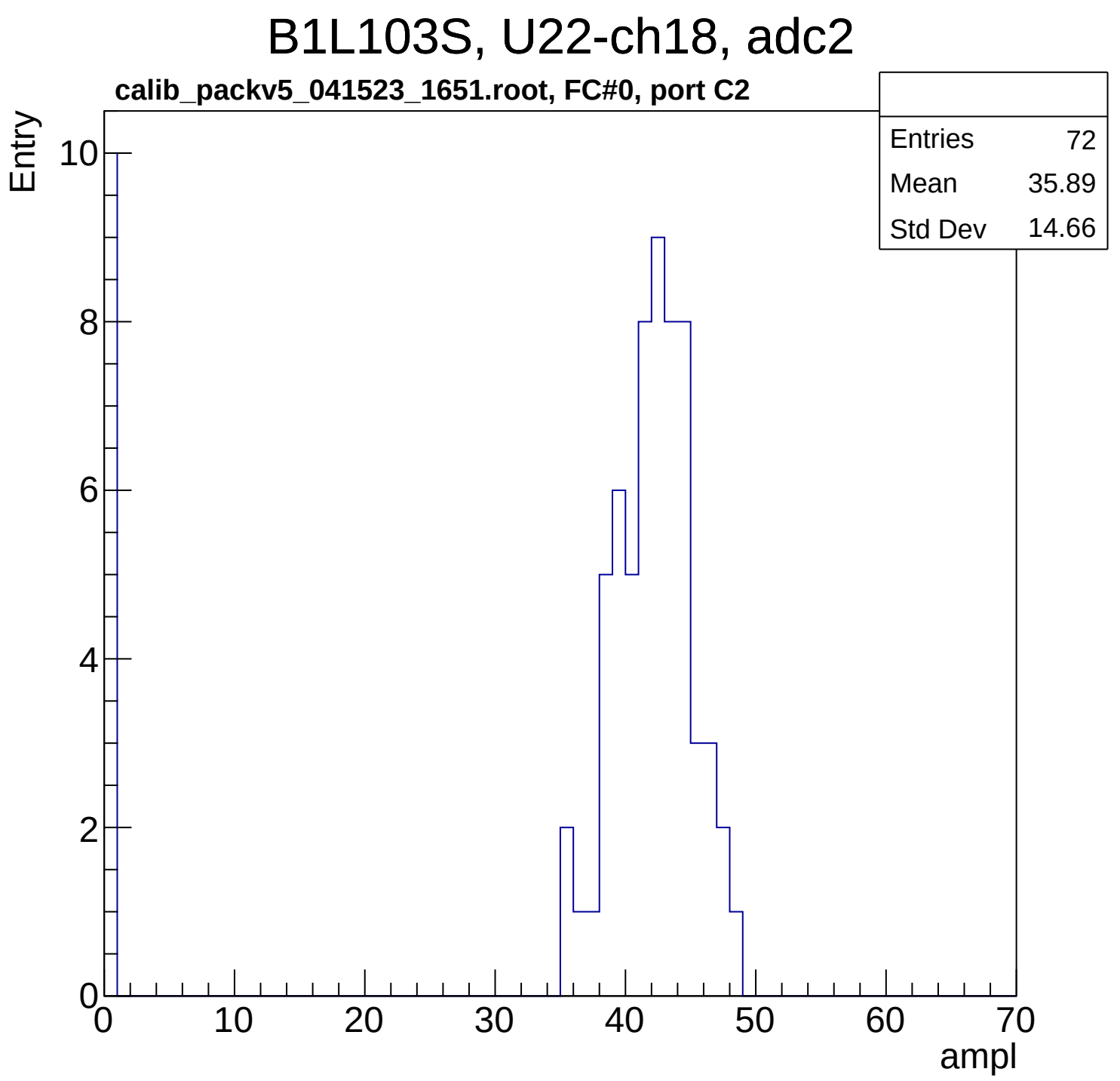

B1L103S, U22-ch17, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 59.32
Std Dev 9.557
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

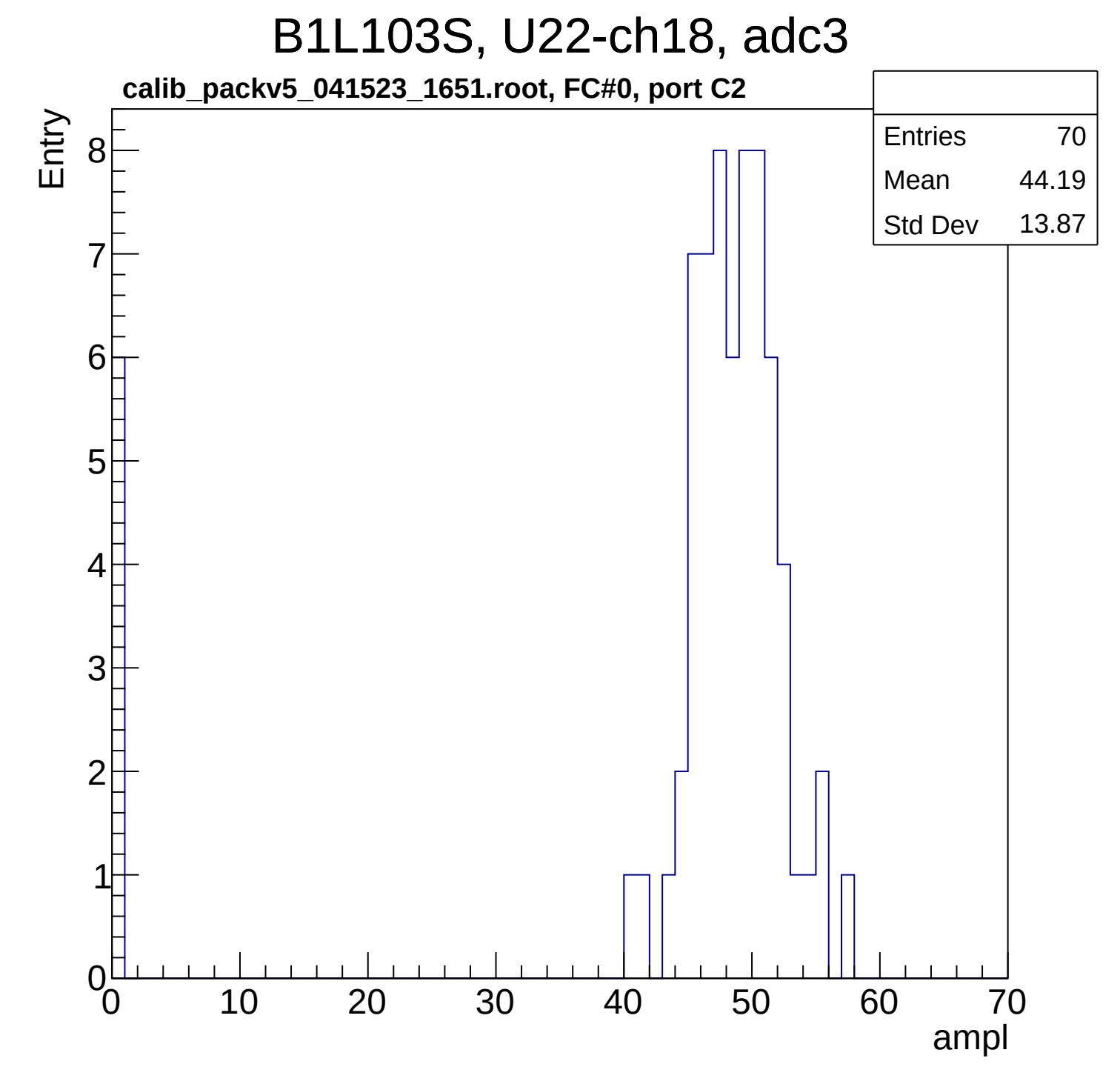

B1L103S, U22-ch17, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

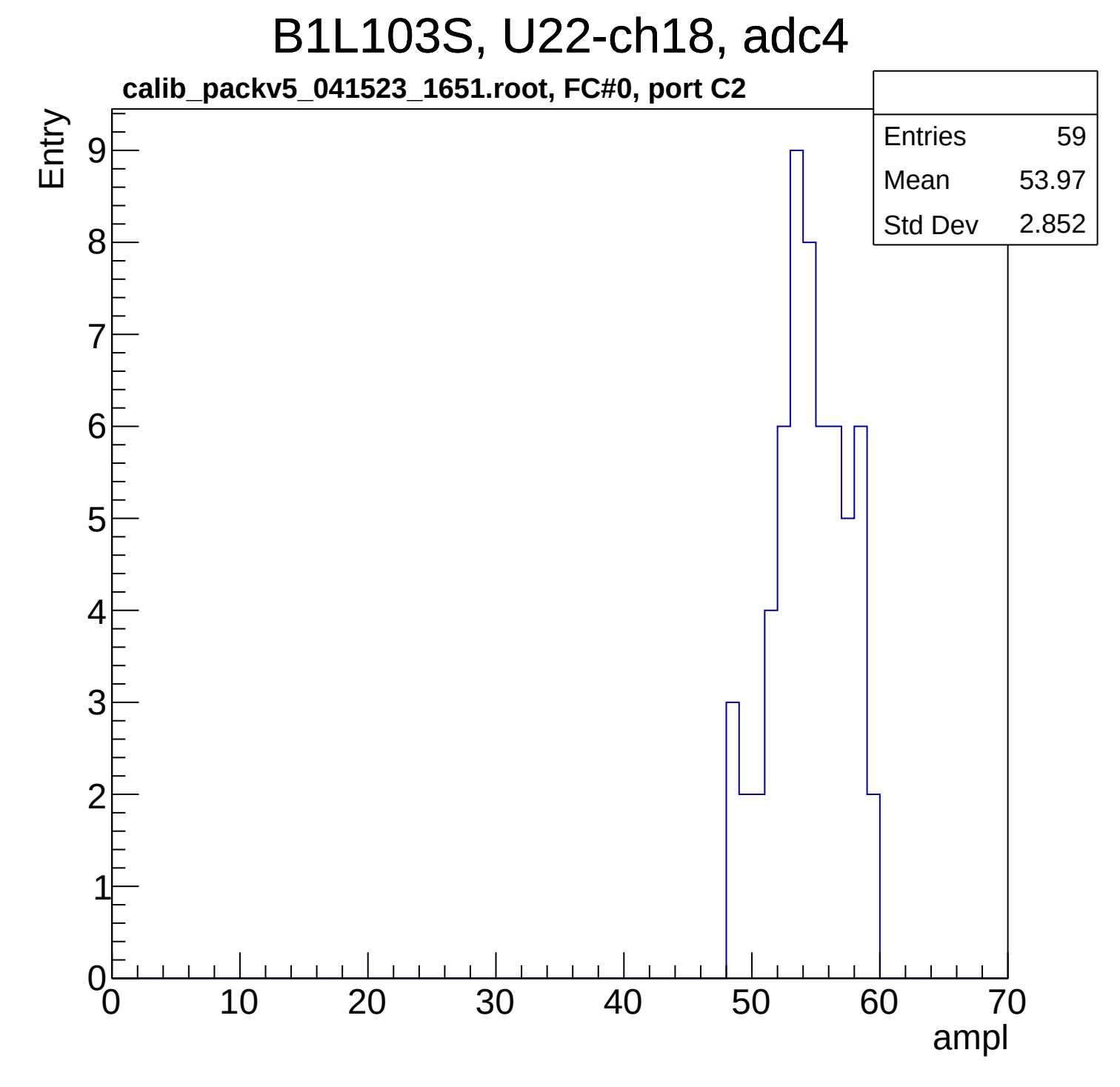

B1L103S, U22-ch17, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.158
Std Dev 4.913
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

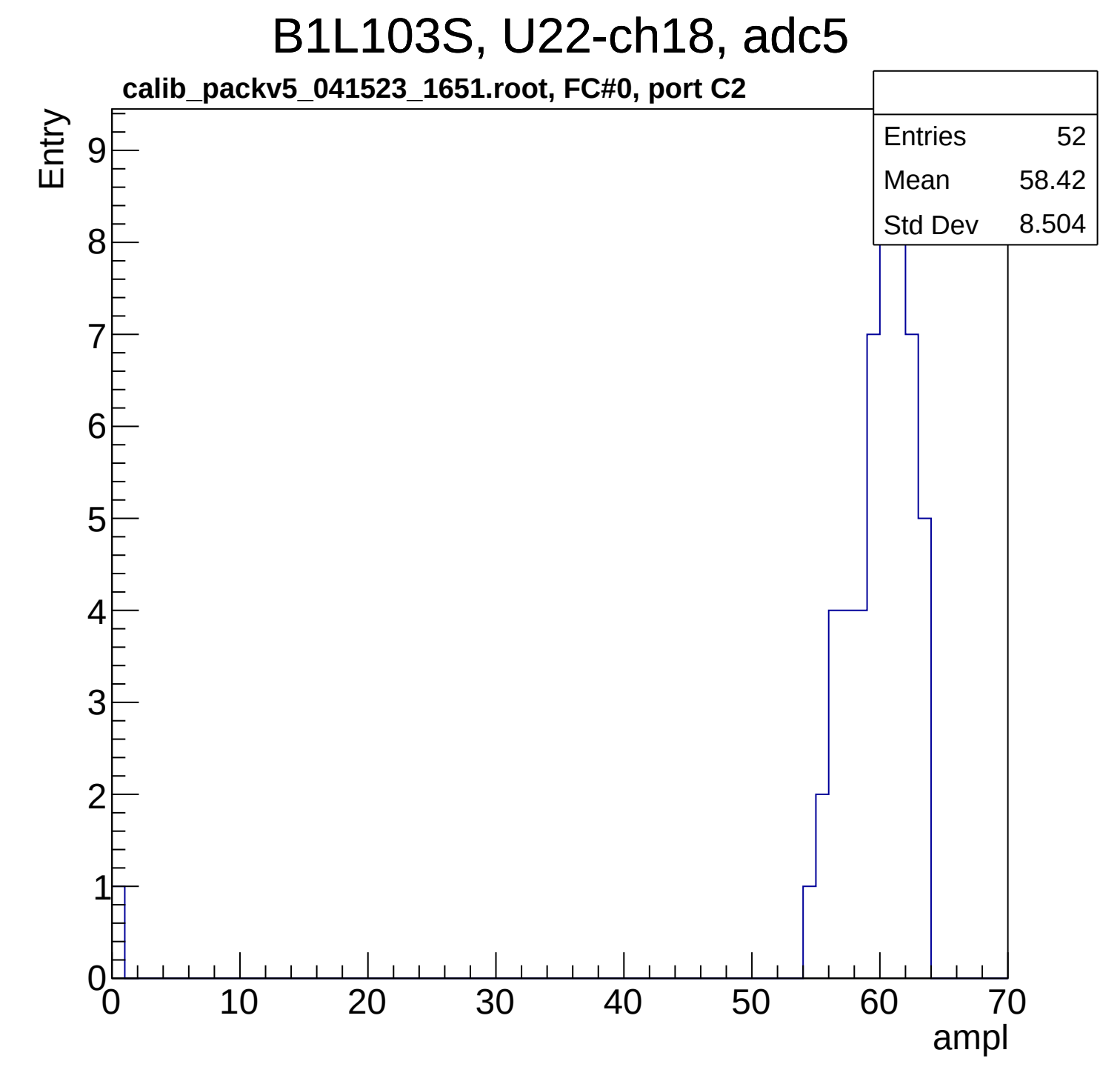

B1L103S, U22-ch18, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 25.09
Std Dev 9.892
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch18, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 35.21
Std Dev 3.332
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch18, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 35.89
Std Dev 14.66
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch18, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 44.19
Std Dev 13.87
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch18, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 53.97
Std Dev 2.852
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch18, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 58.42
Std Dev 8.504
Entry
ampl
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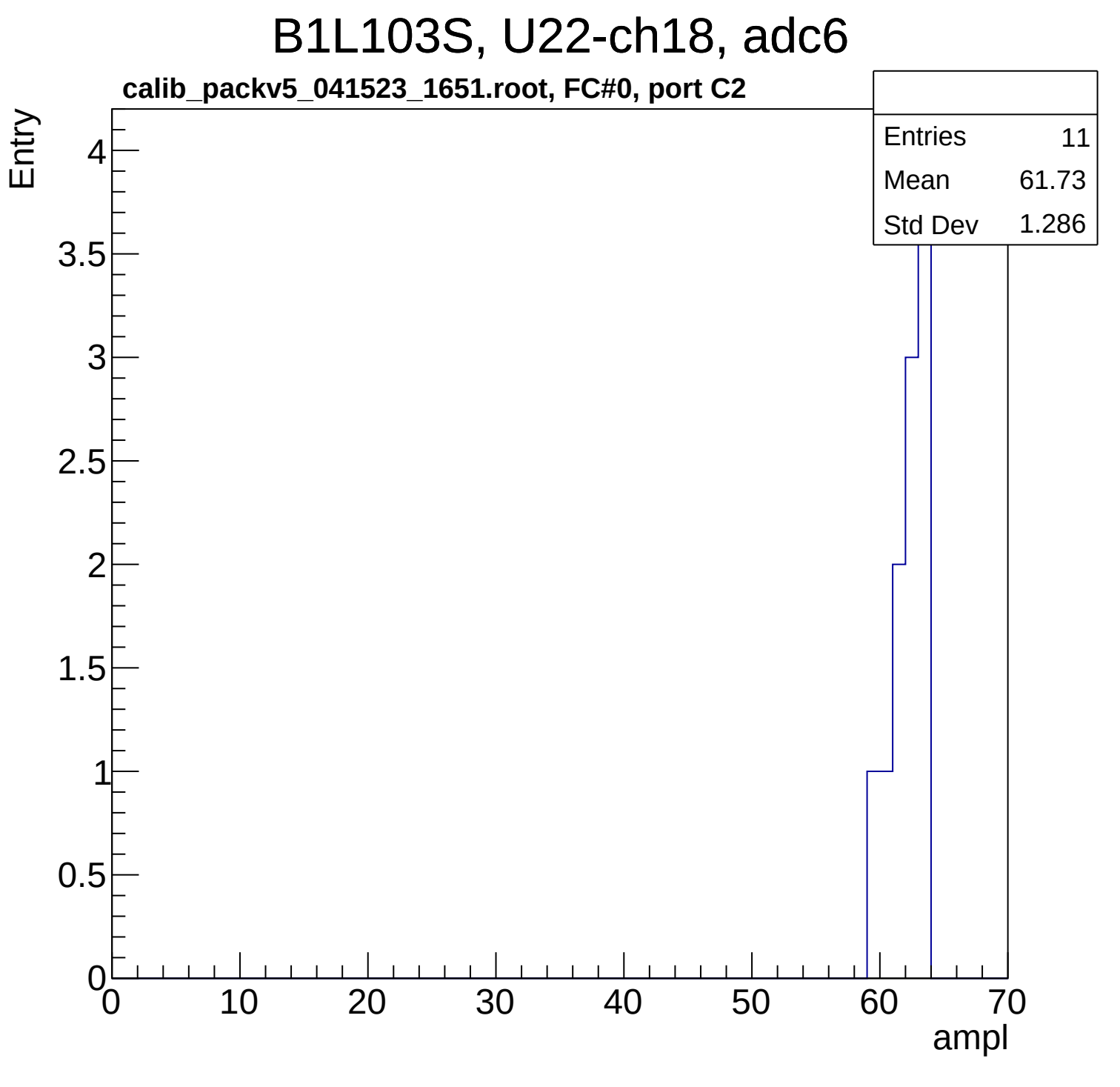
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch18, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 61.73
Std Dev 1.286
Entry
ampl
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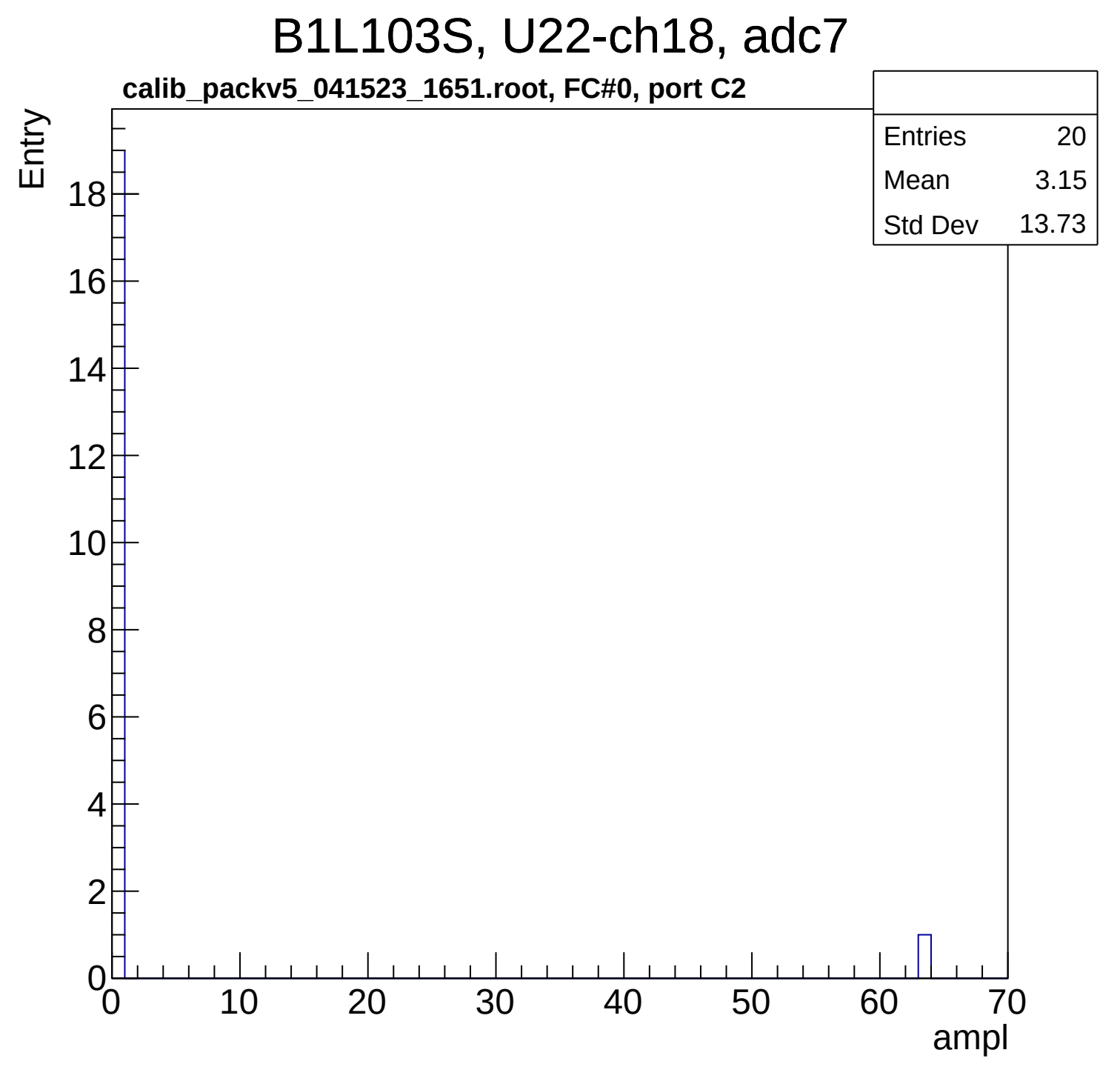
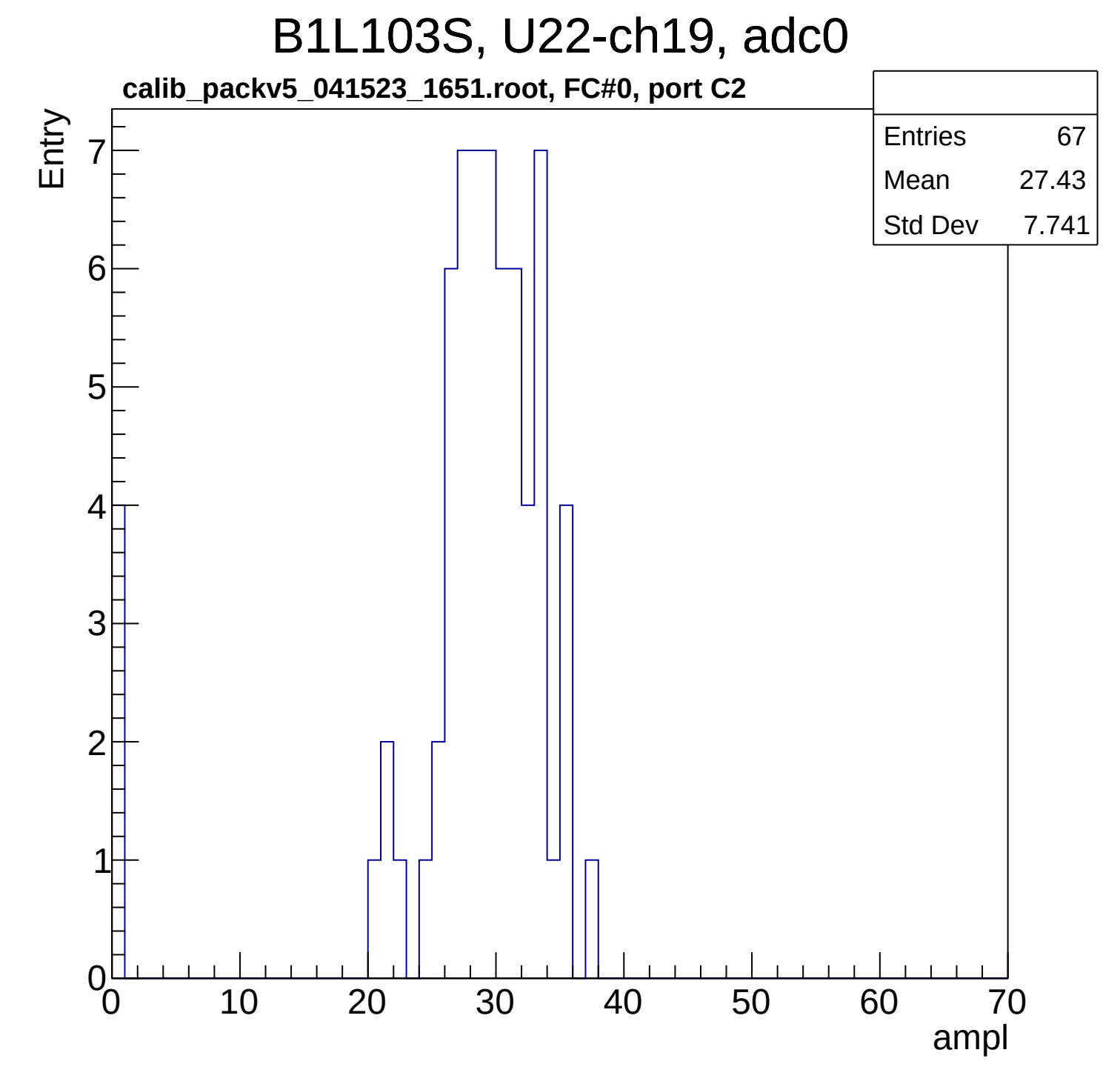
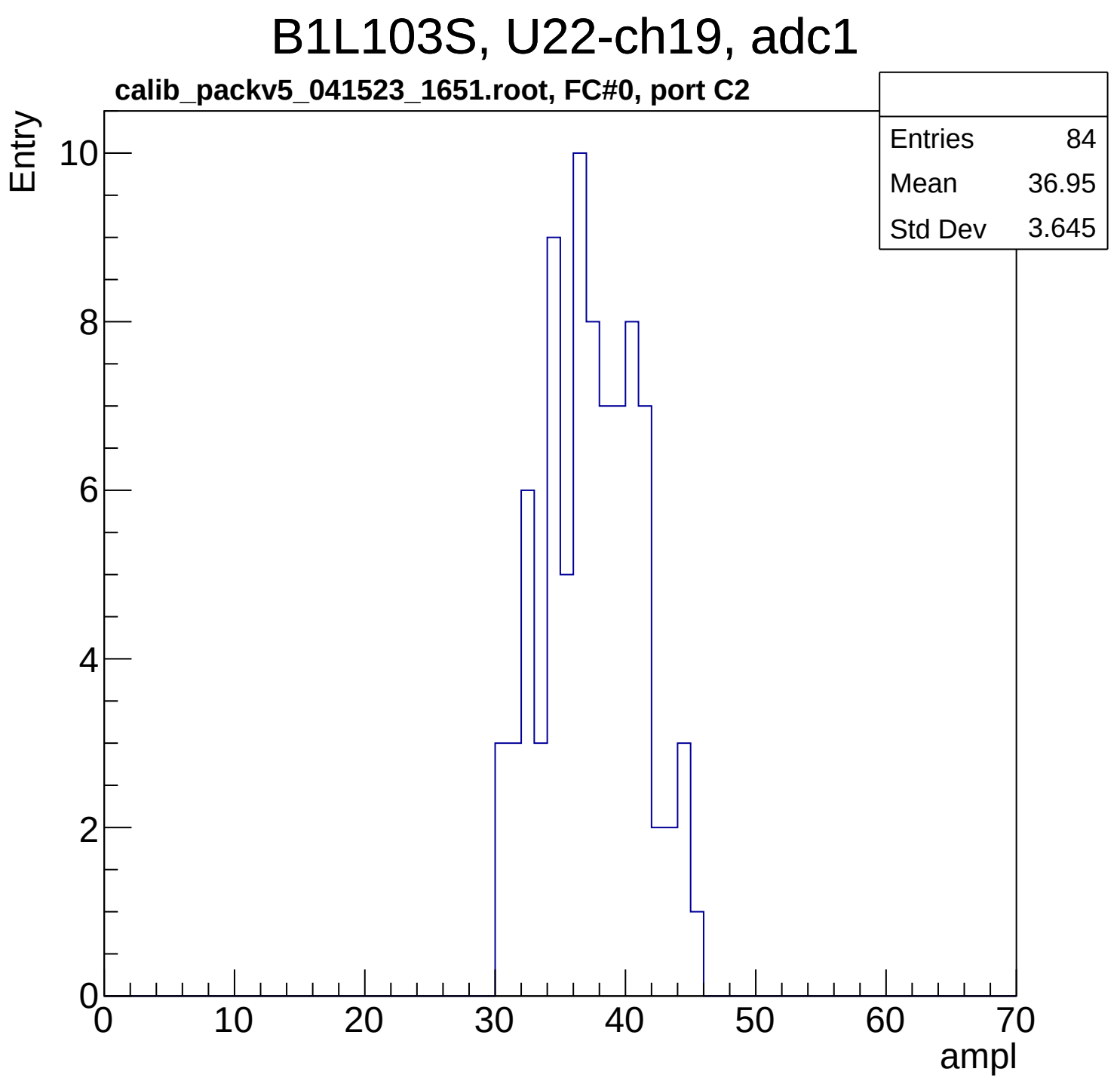
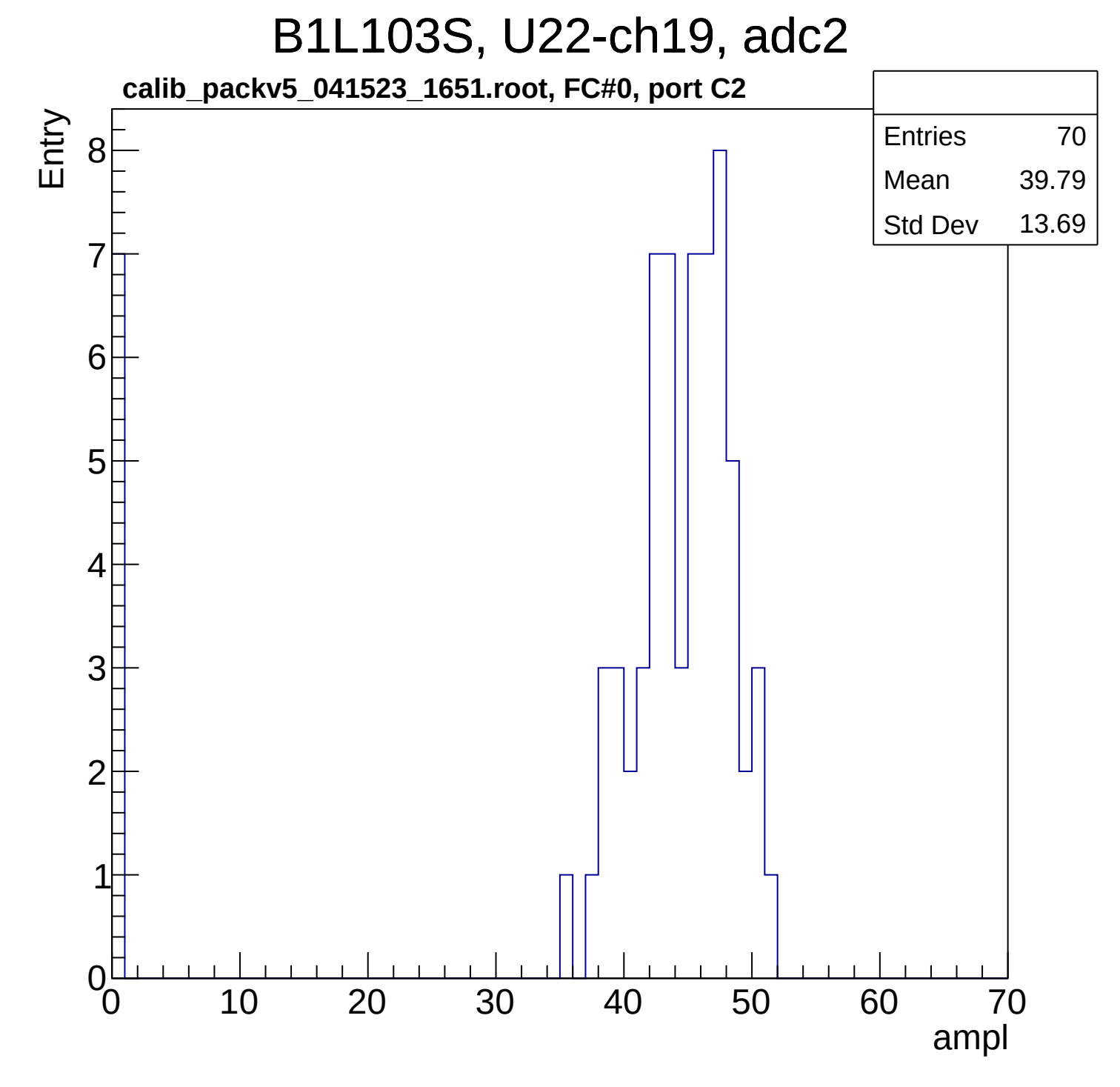
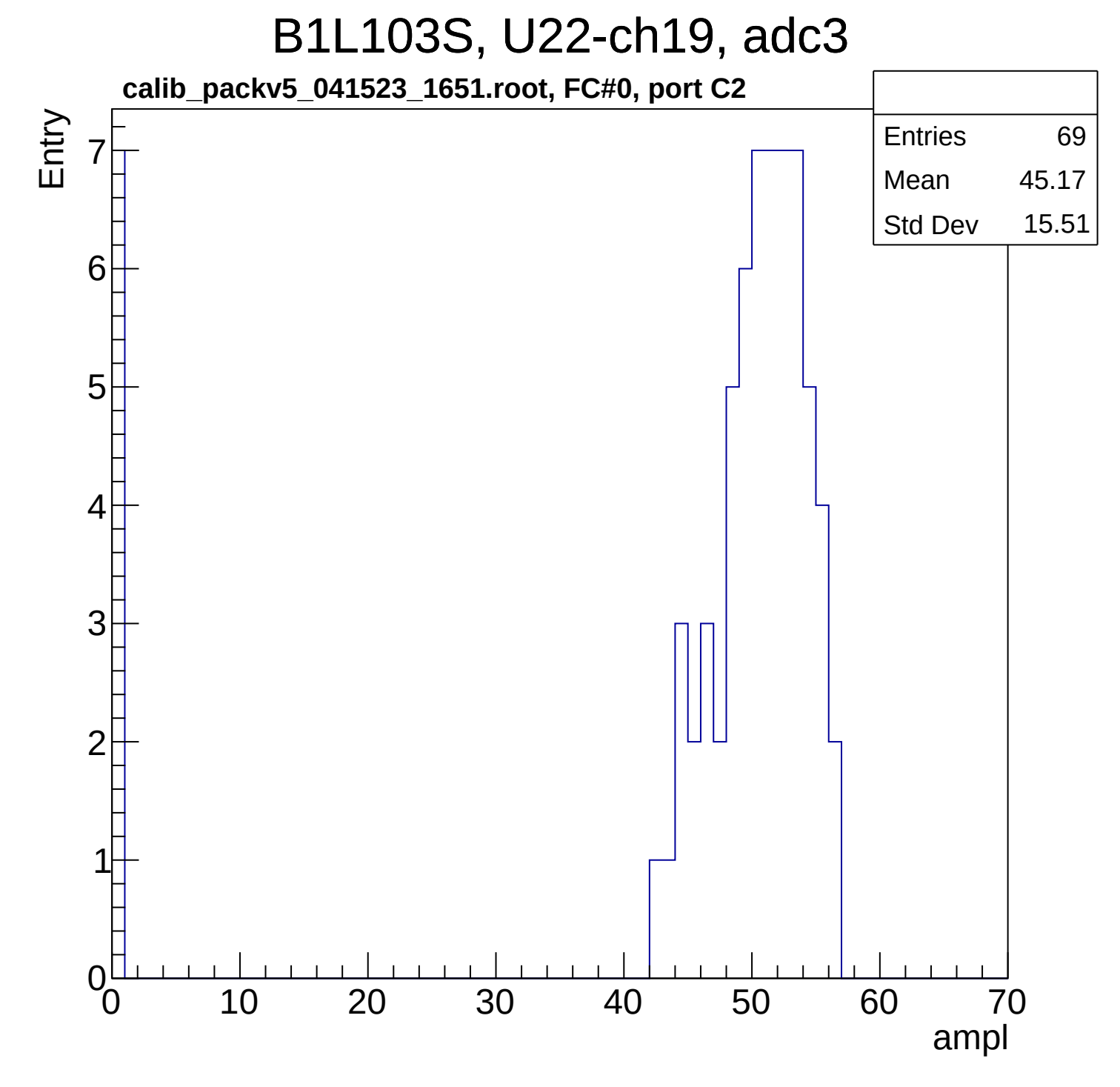
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

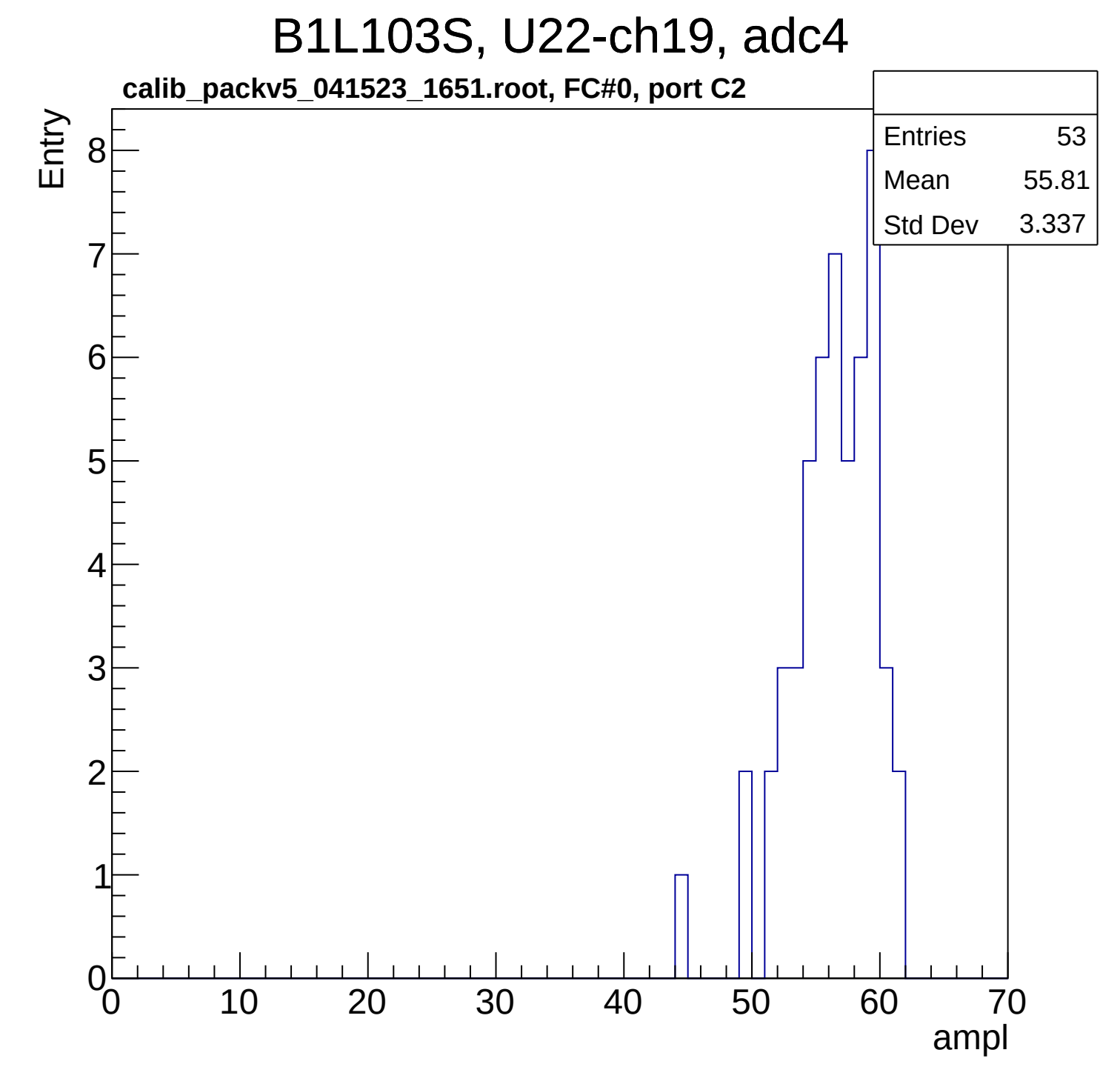

B1L103S, U22-ch18, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

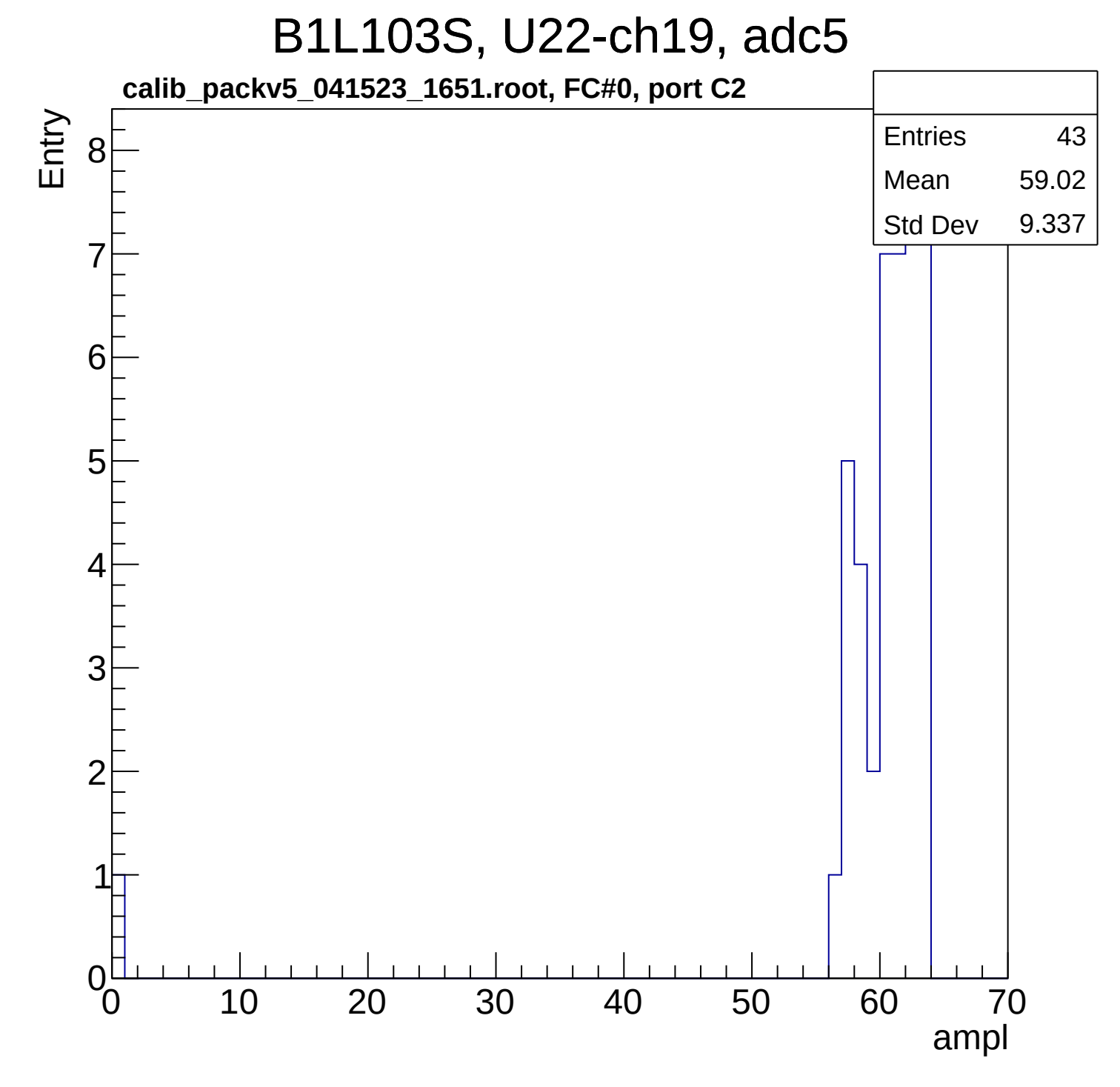

B1L103S, U22-ch19, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 27.43
Std Dev 7.741
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

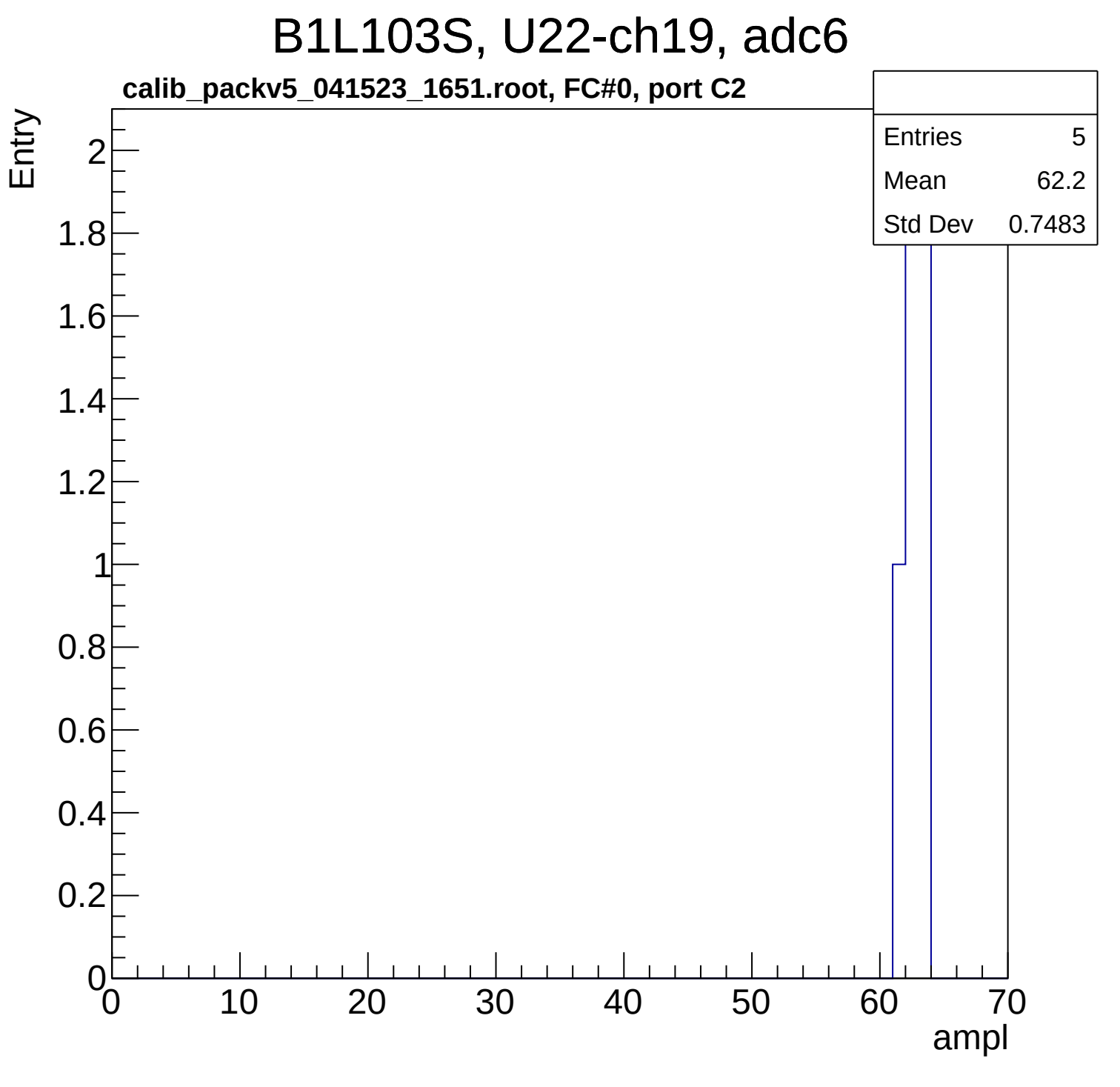

B1L103S, U22-ch19, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 36.95
Std Dev 3.645
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

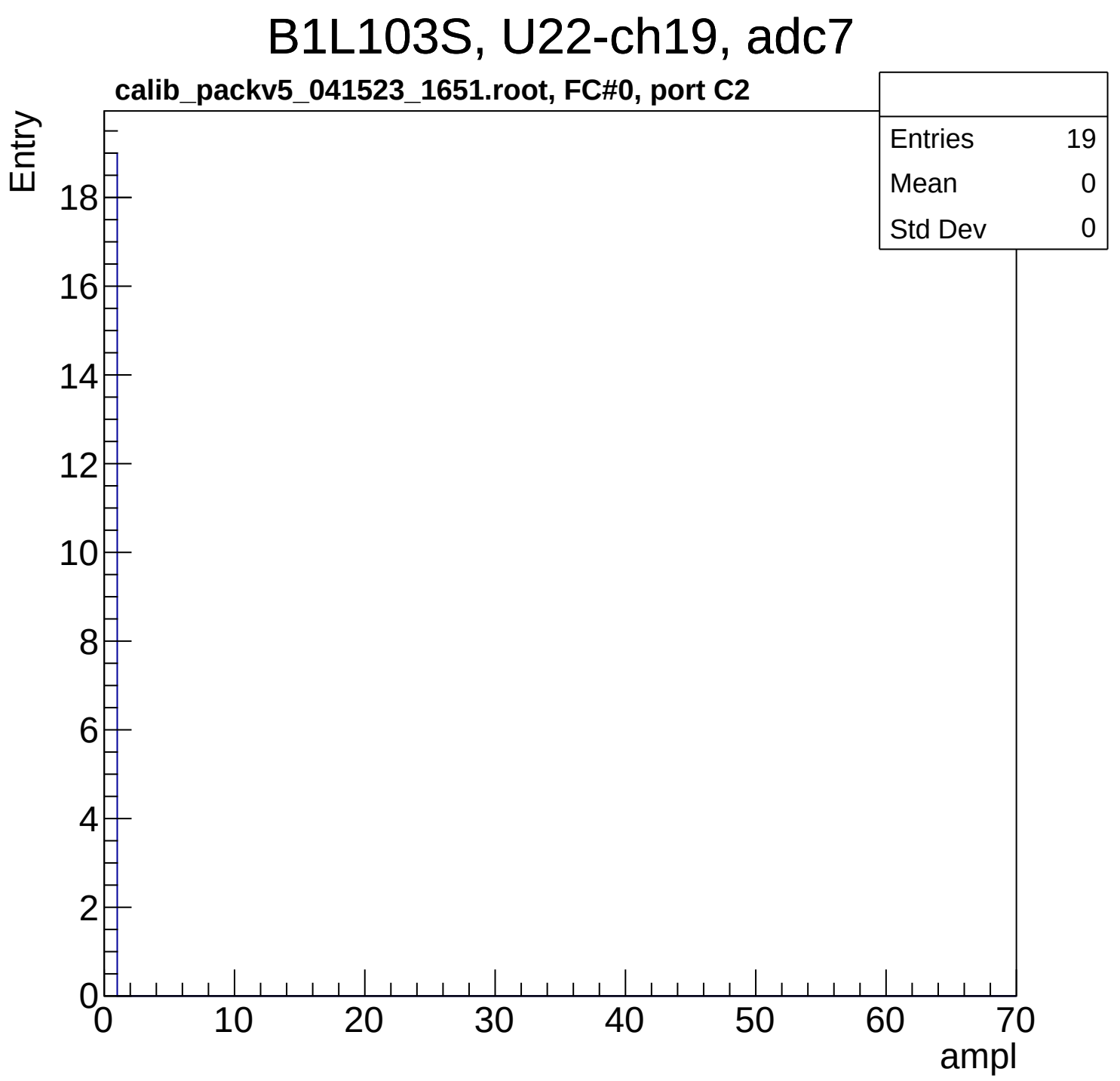

B1L103S, U22-ch19, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 39.79
Std Dev 13.69
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

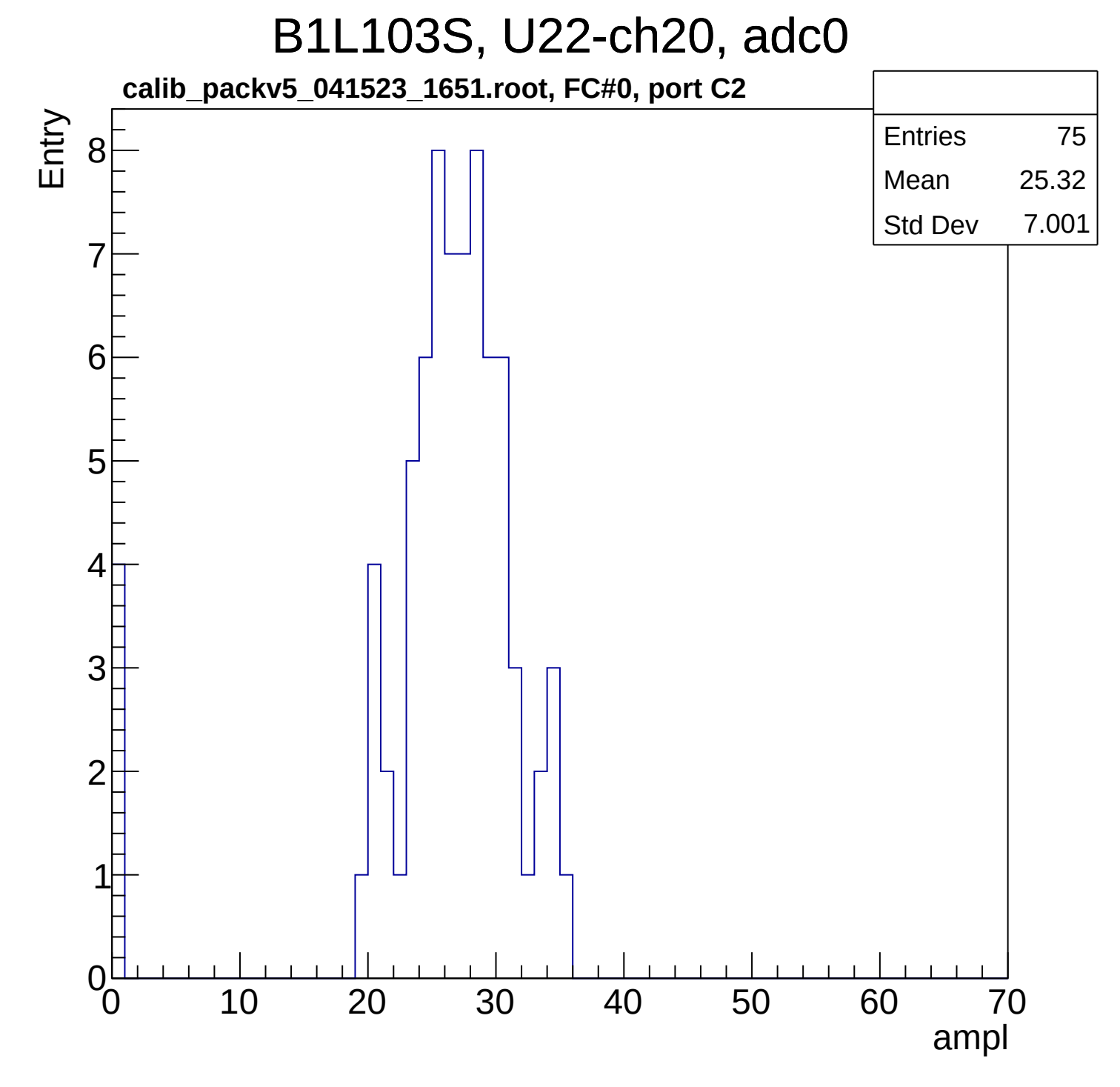

B1L103S, U22-ch19, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 45.17
Std Dev 15.51
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

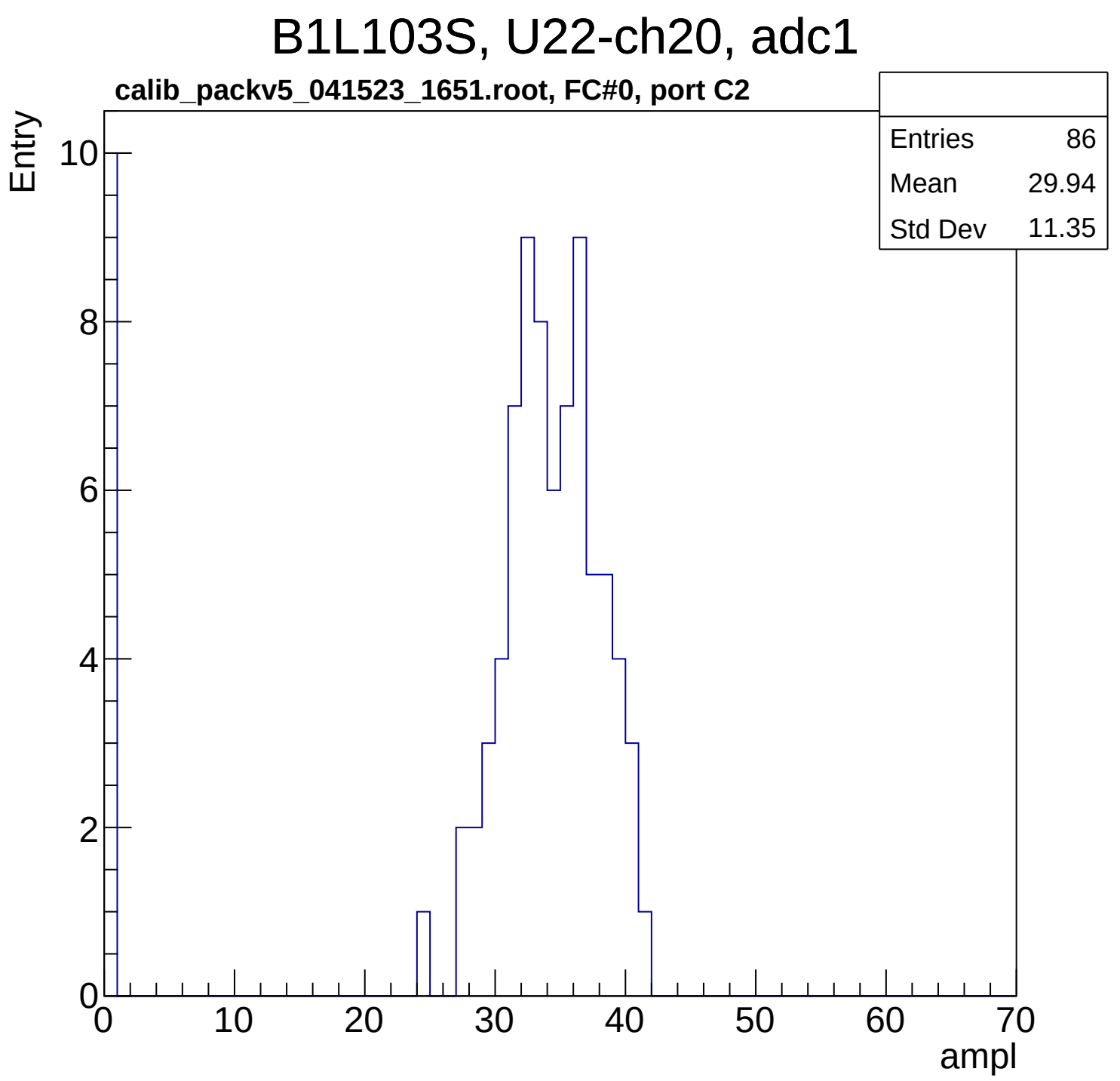

B1L103S, U22-ch19, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 55.81
Std Dev 3.337
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

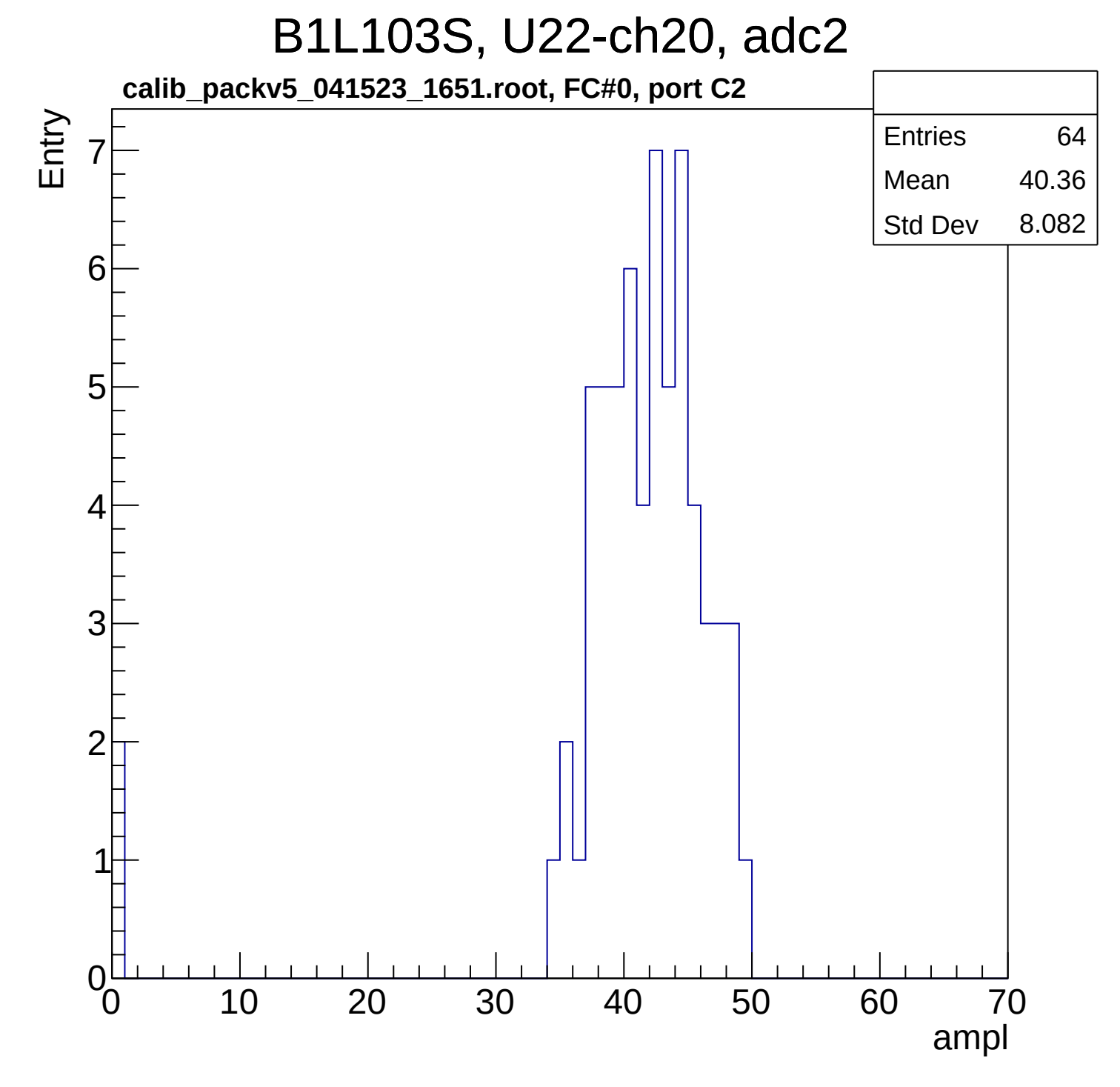

B1L103S, U22-ch19, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 59.02
Std Dev 9.337
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

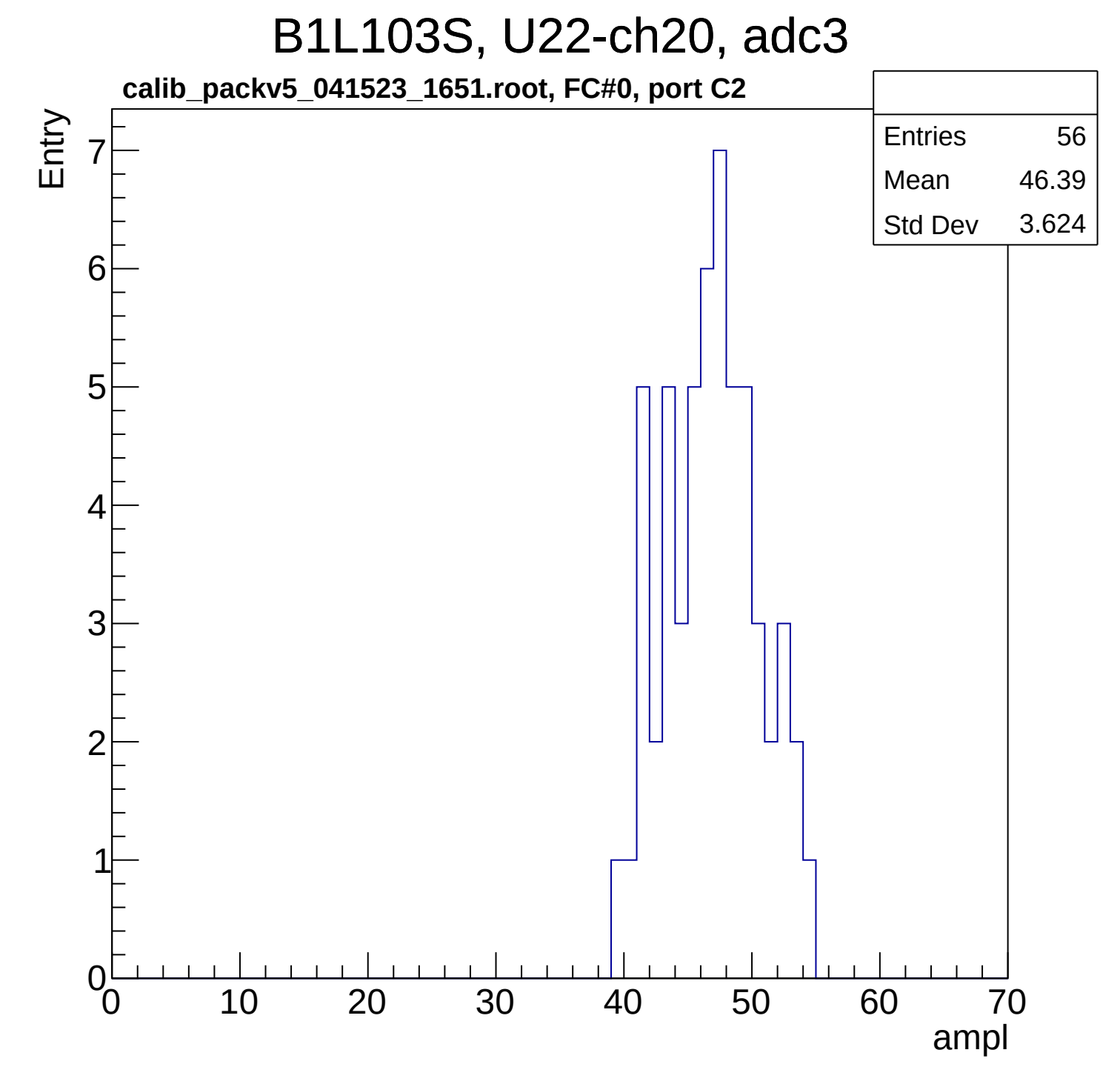

B1L103S, U22-ch19, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 62.2
Std Dev 0.7483
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

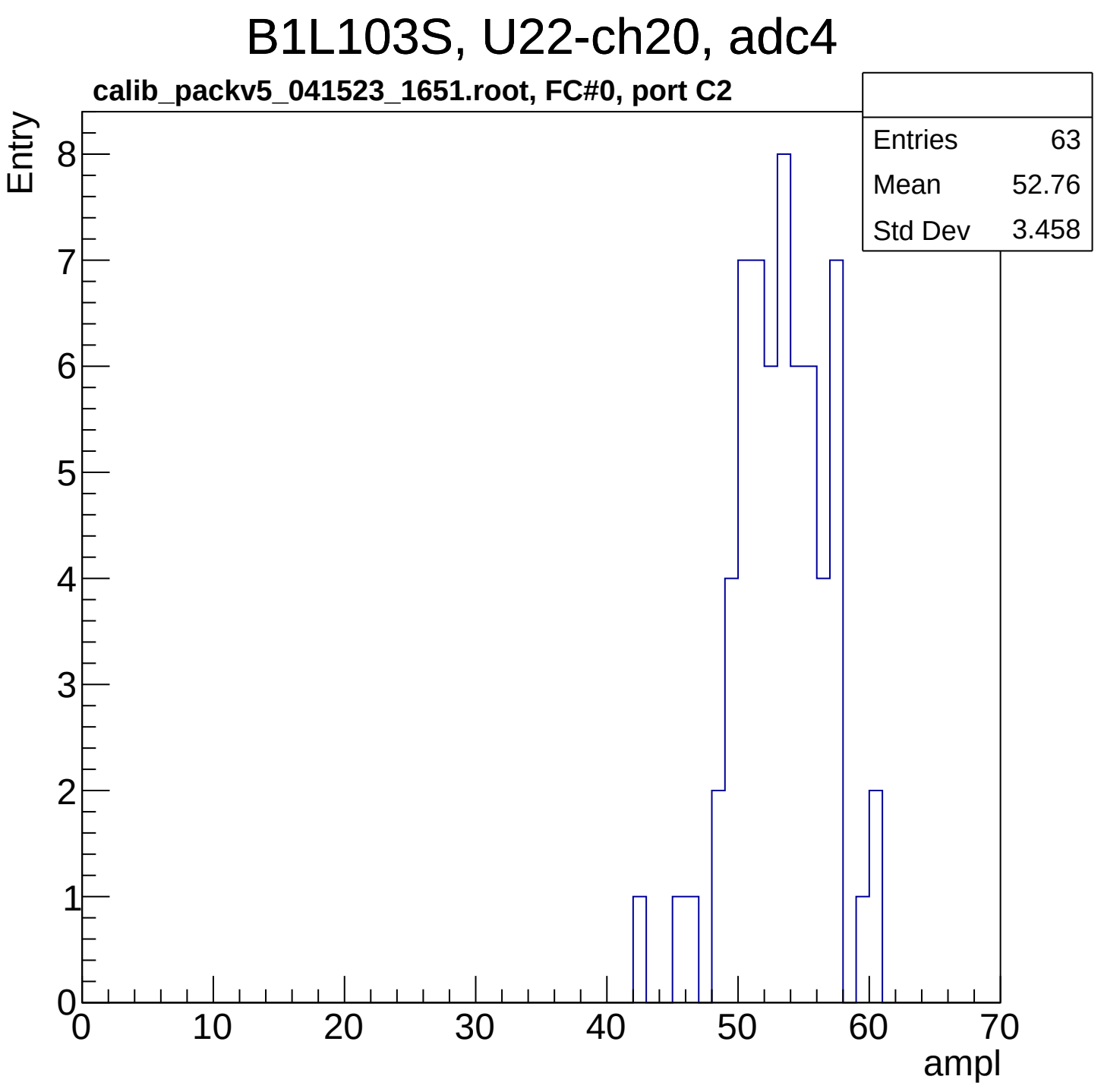

B1L103S, U22-ch19, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

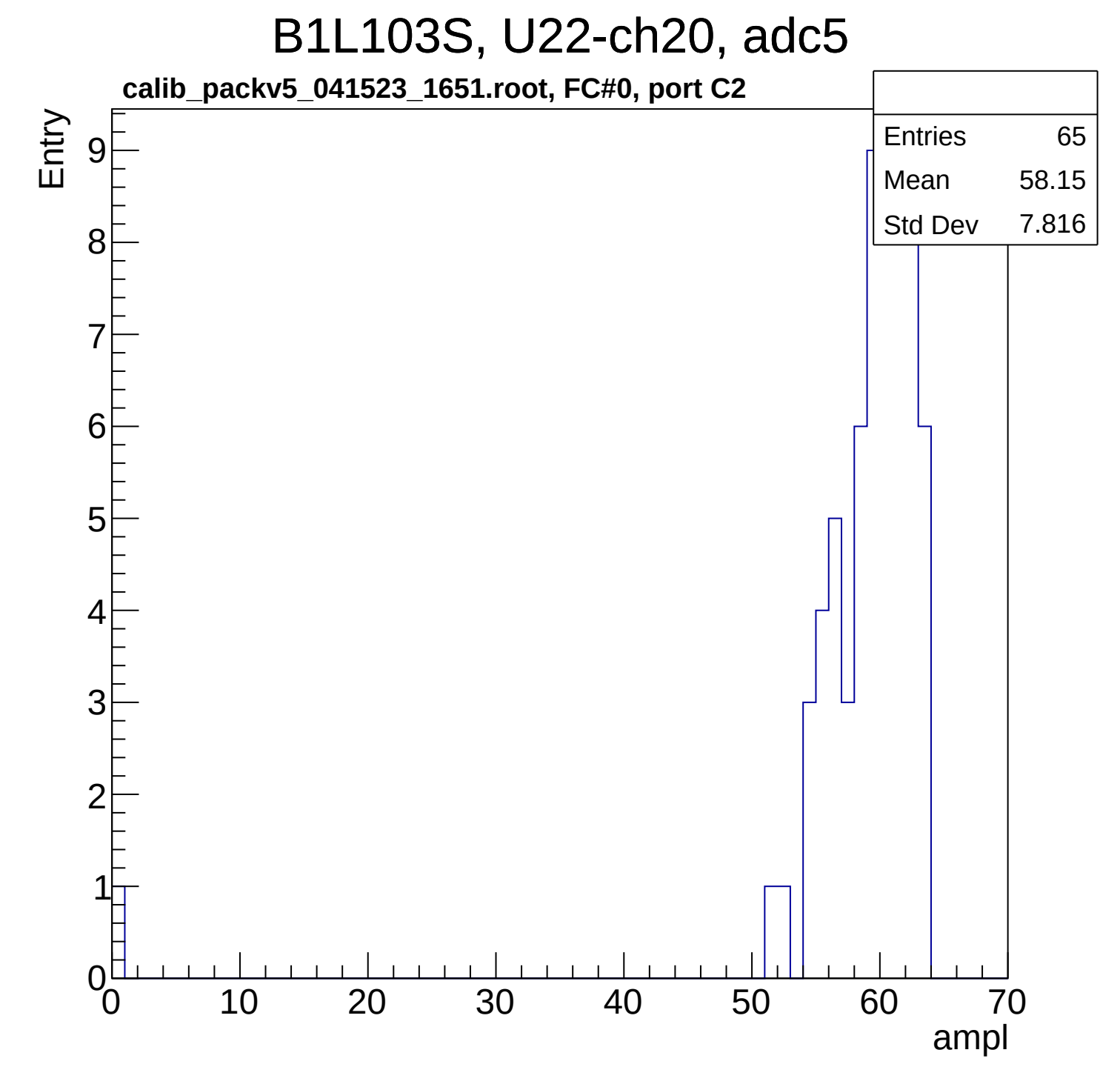

B1L103S, U22-ch20, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 25.32
Std Dev 7.001
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch20, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 29.94
Std Dev 11.35
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch20, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 40.36
Std Dev 8.082
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U22-ch20, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 46.39
Std Dev 3.624
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U22-ch20, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 52.76
Std Dev 3.458
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch20, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 58.15
Std Dev 7.816
Entry
ampl
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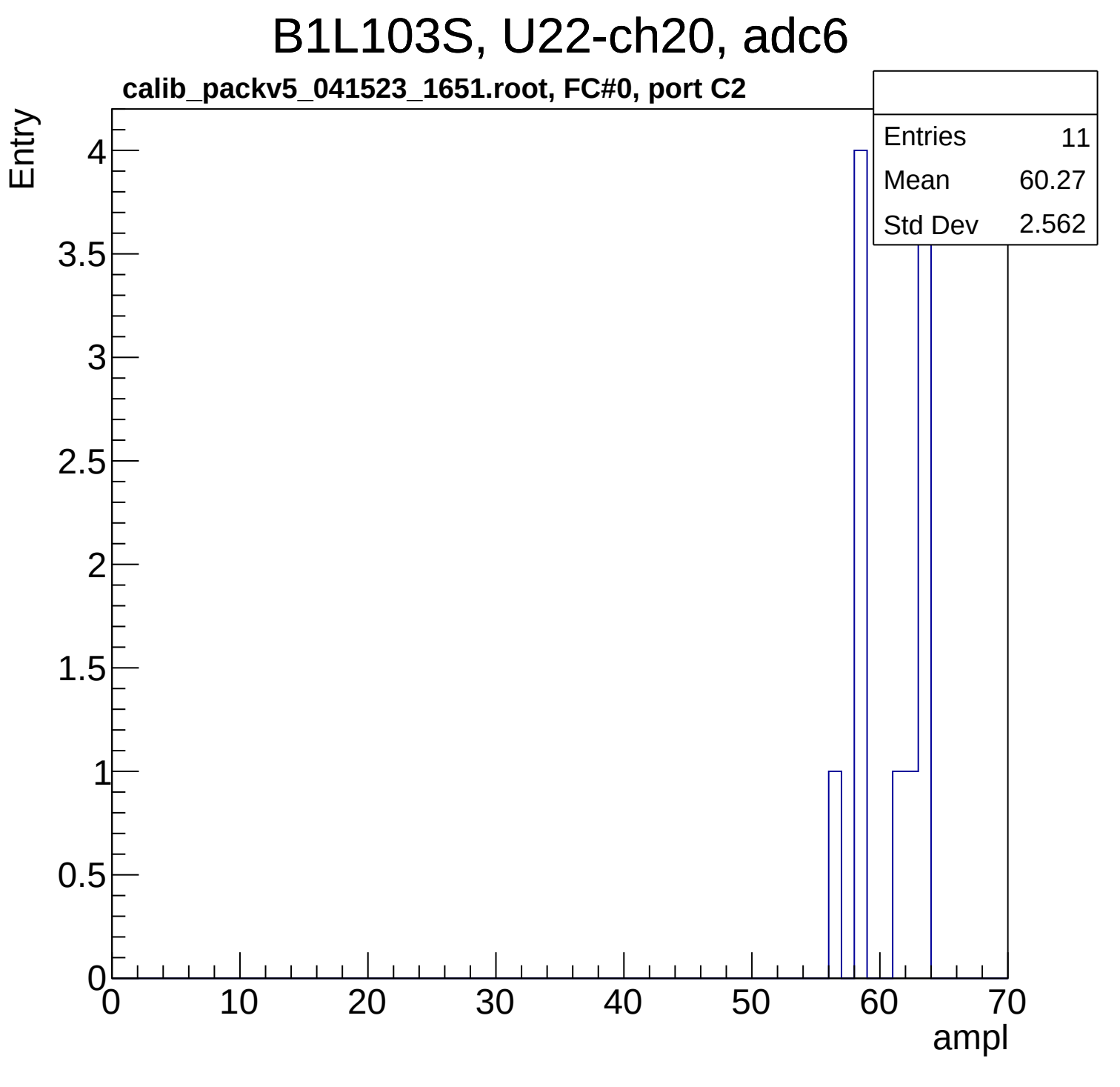
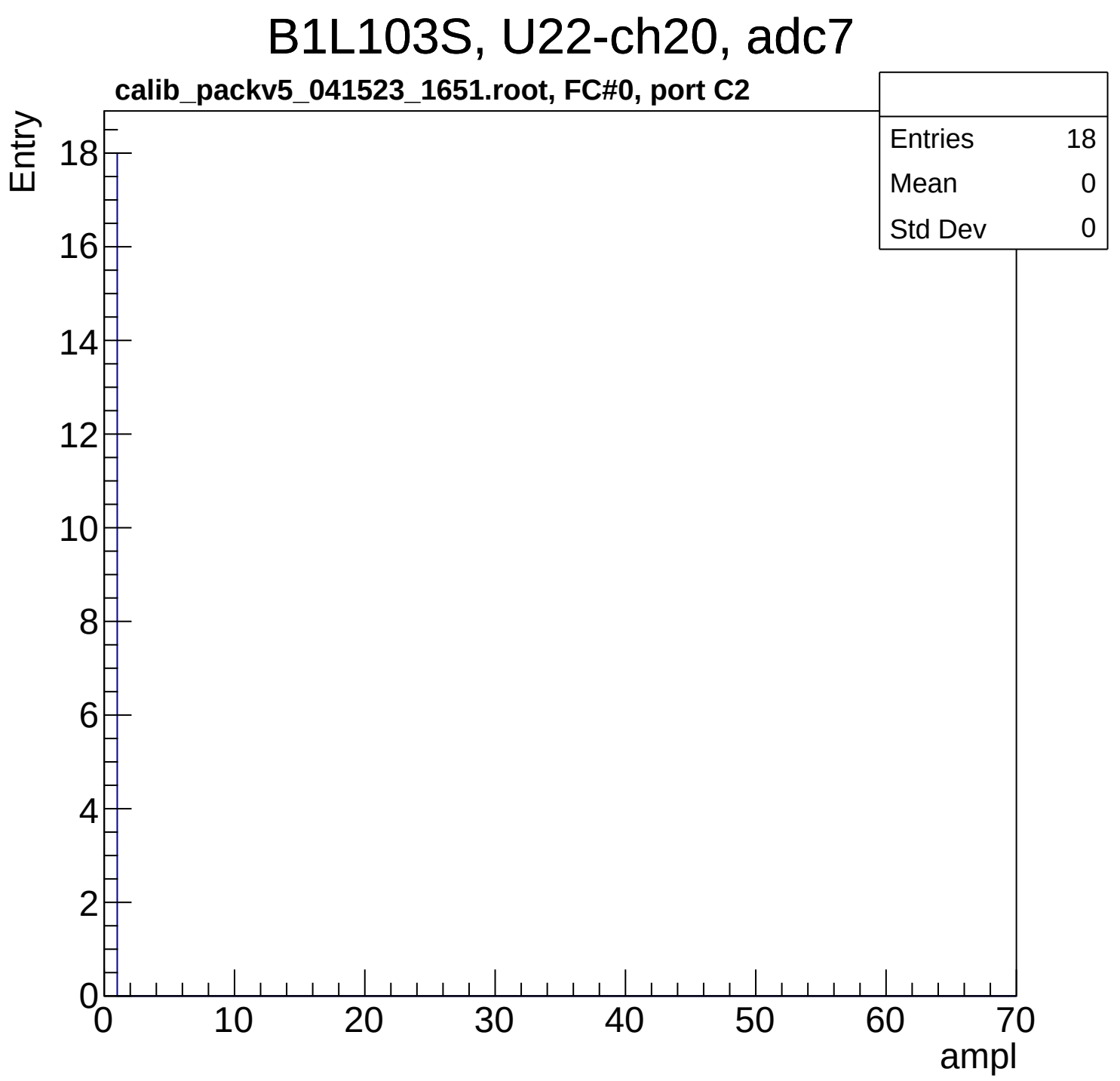
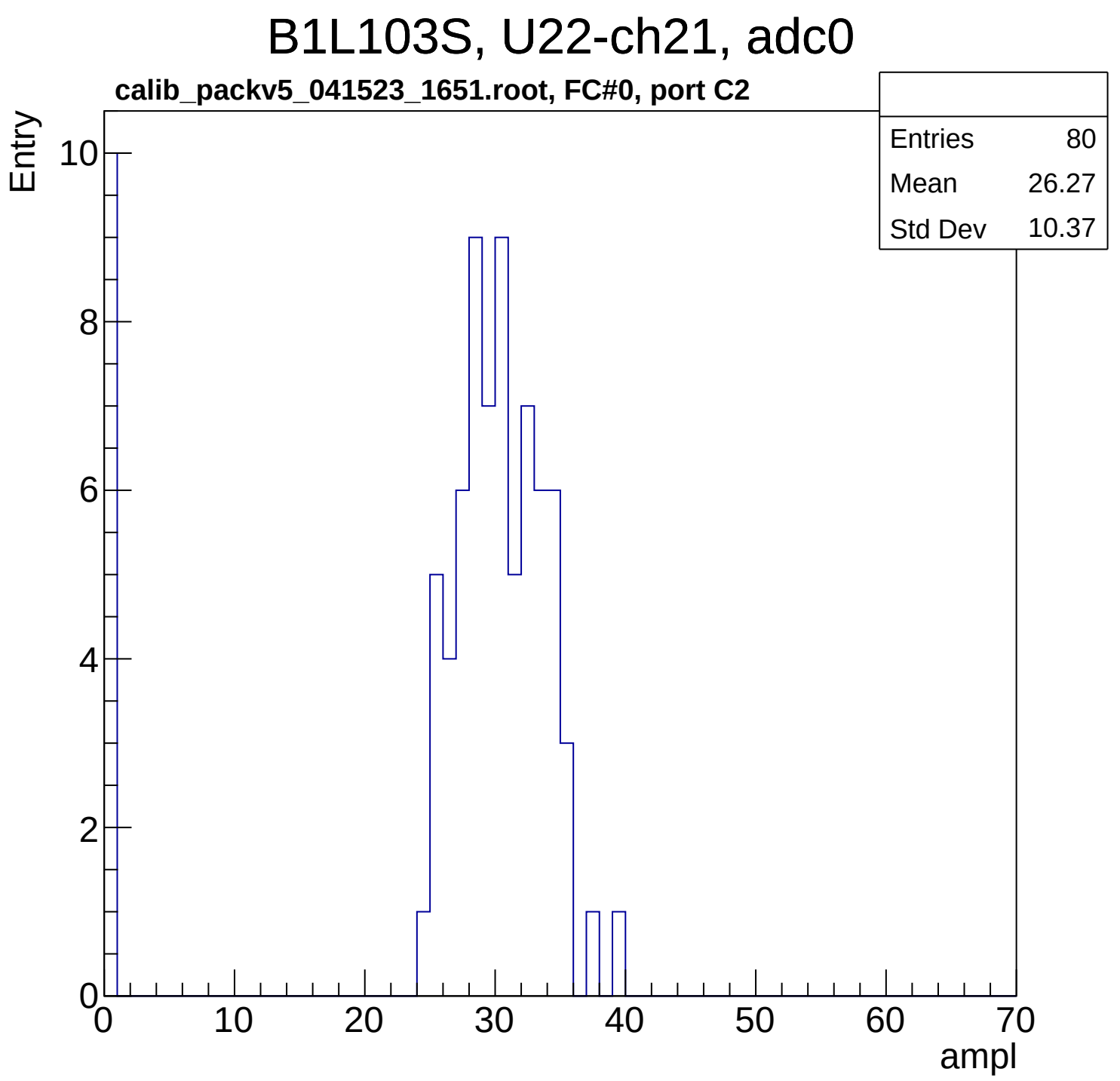
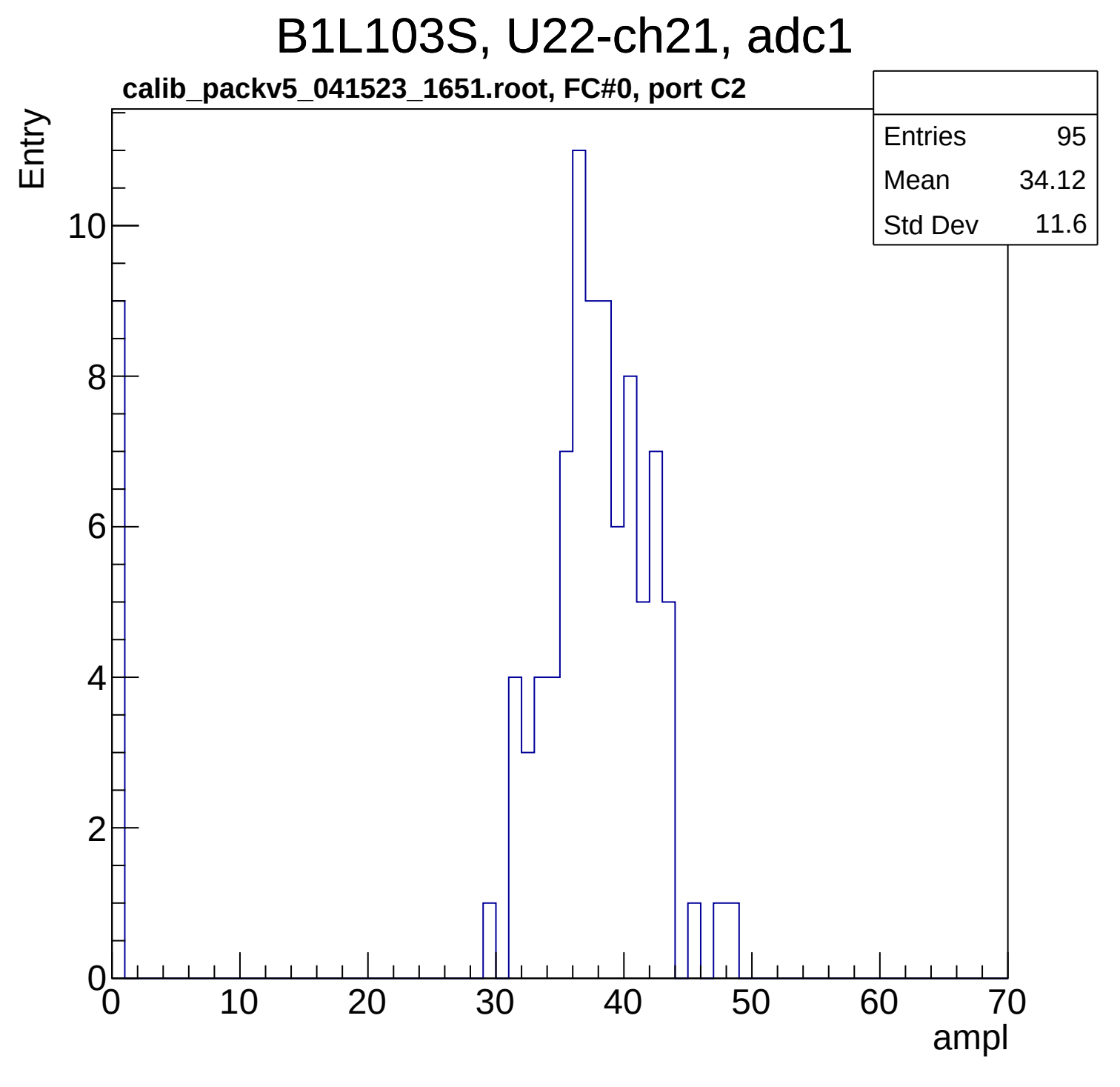
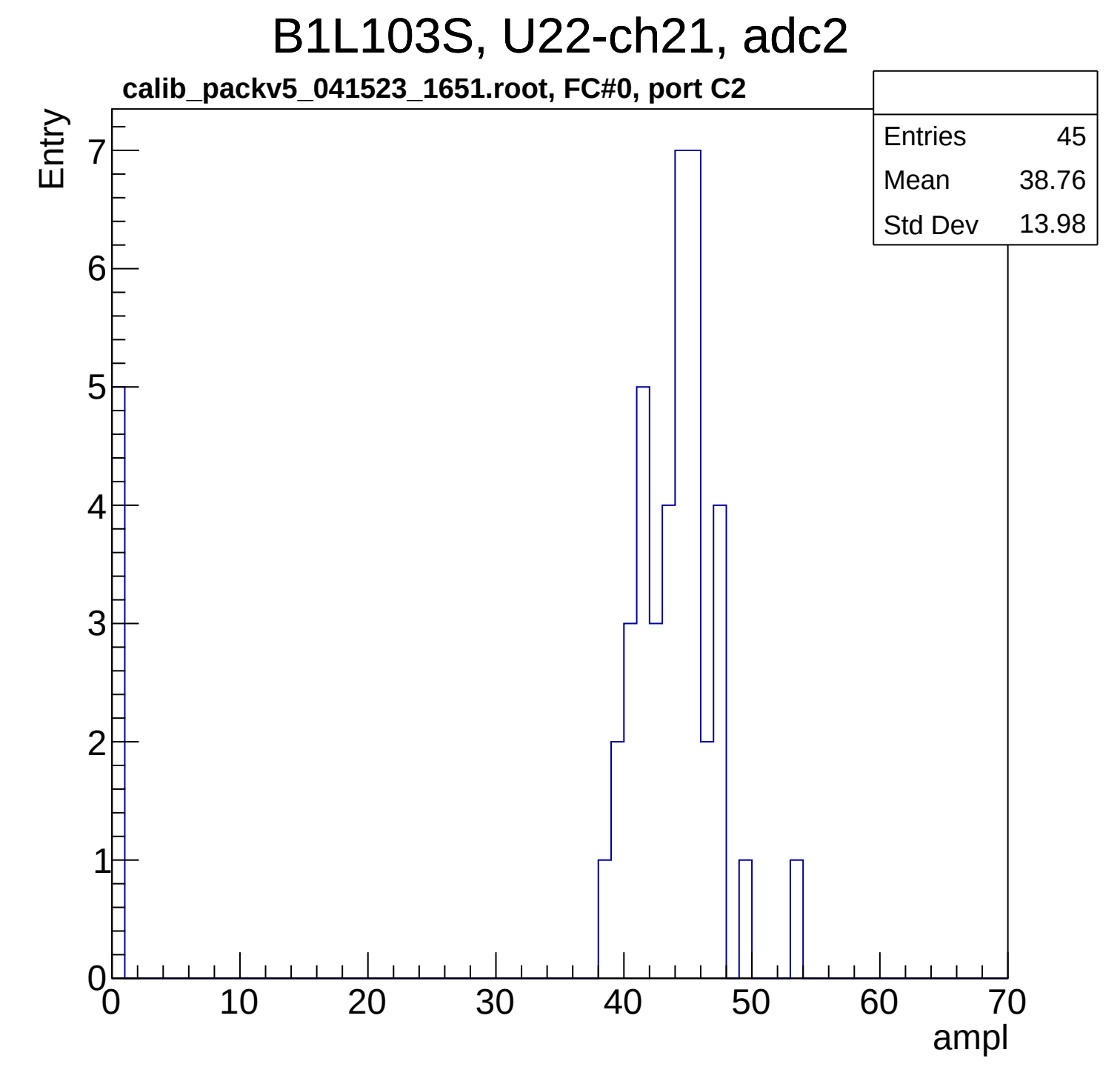
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

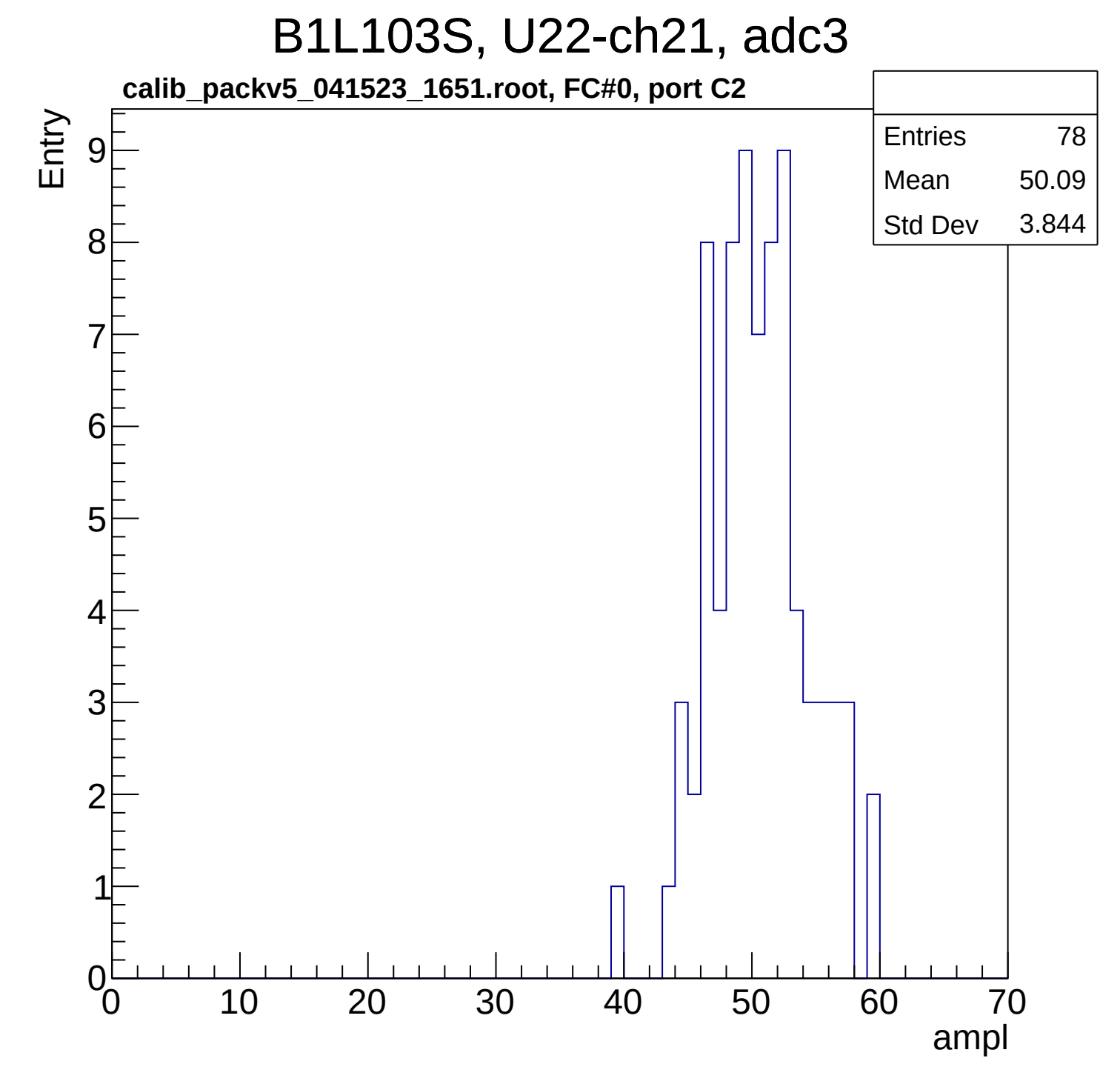

B1L103S, U22-ch20, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 60.27
Std Dev 2.562
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

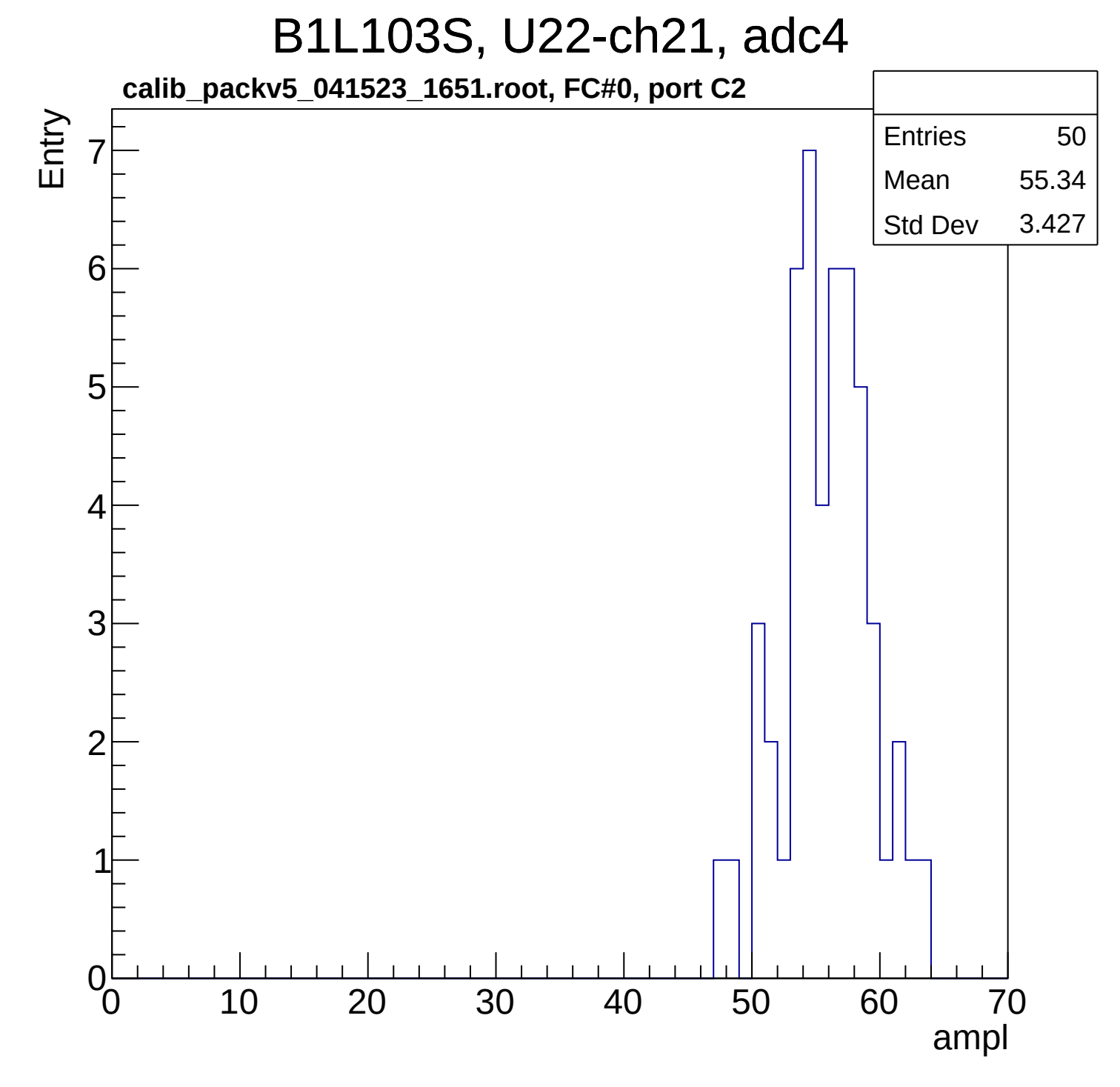

B1L103S, U22-ch20, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

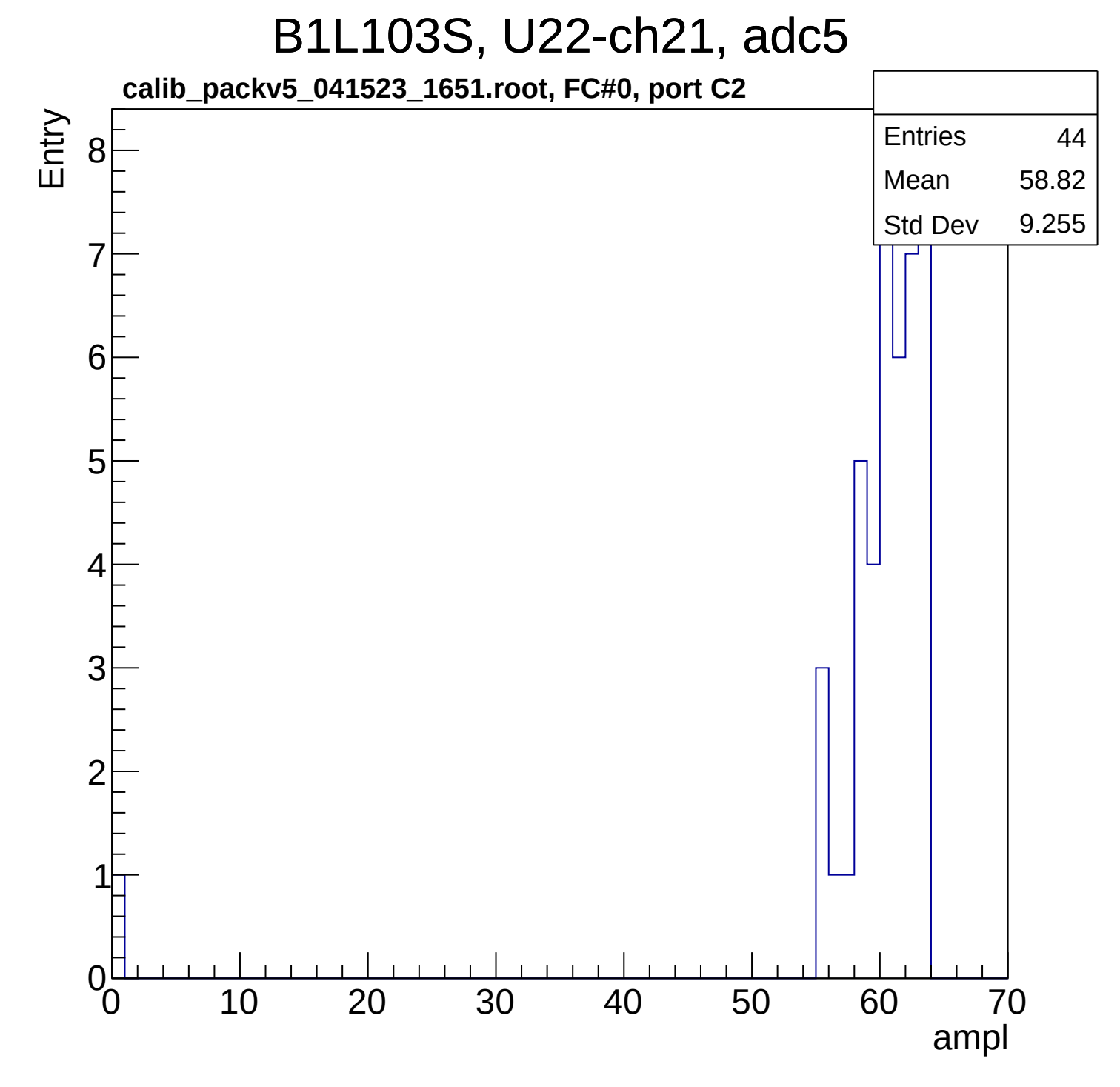

B1L103S, U22-ch21, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 26.27
Std Dev 10.37
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U22-ch21, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 34.12
Std Dev 11.6
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch21, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 38.76
Std Dev 13.98
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U22-ch21, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 50.09
Std Dev 3.844
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch21, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 55.34
Std Dev 3.427
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U22-ch21, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 58.82
Std Dev 9.255
Entry
ampl
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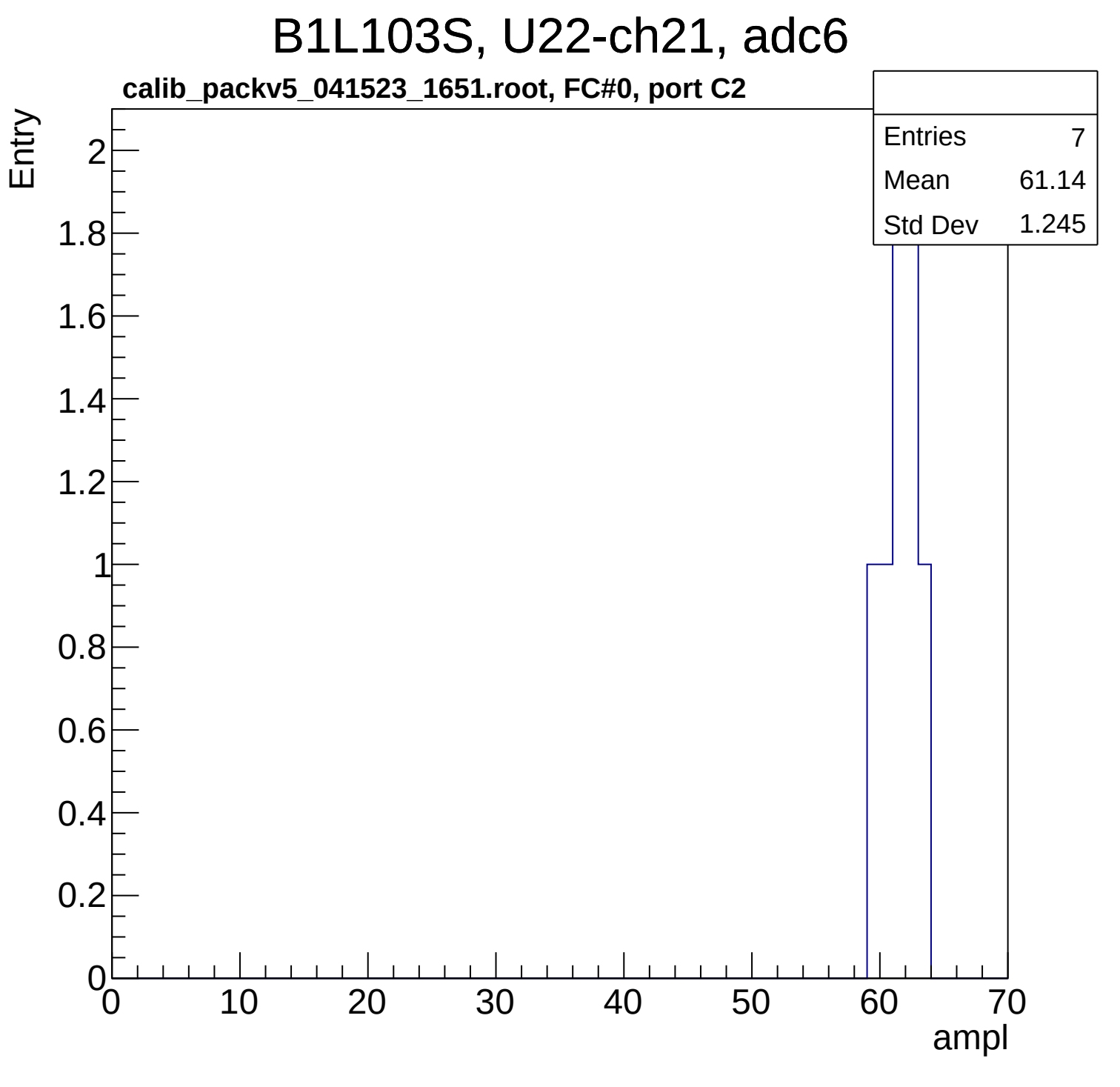
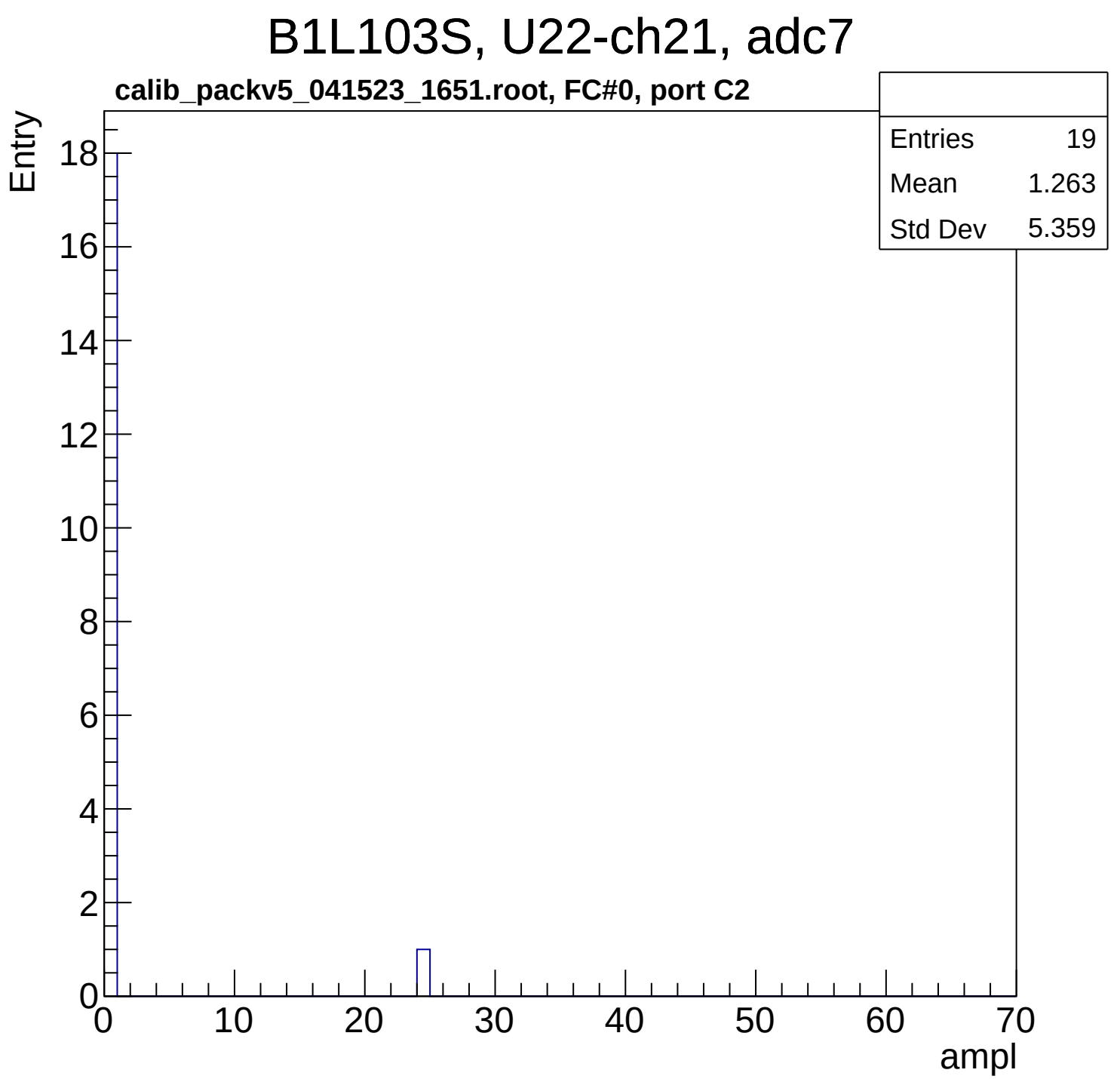
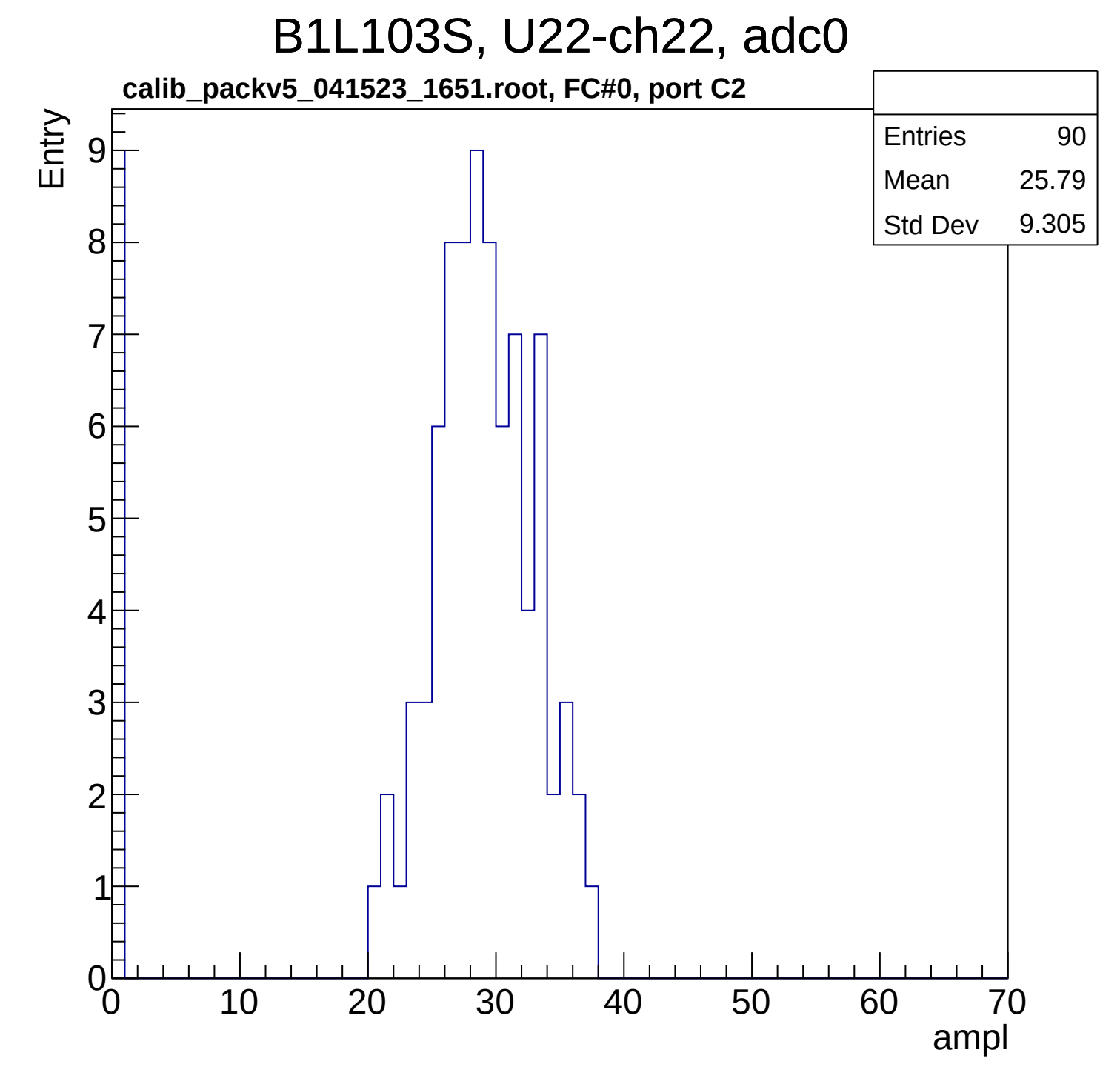
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch21, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 61.14
Std Dev 1.245
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U22-ch21, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.263
Std Dev 5.359
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L103S, U22-ch22, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 25.79
Std Dev 9.305
Entry
ampl
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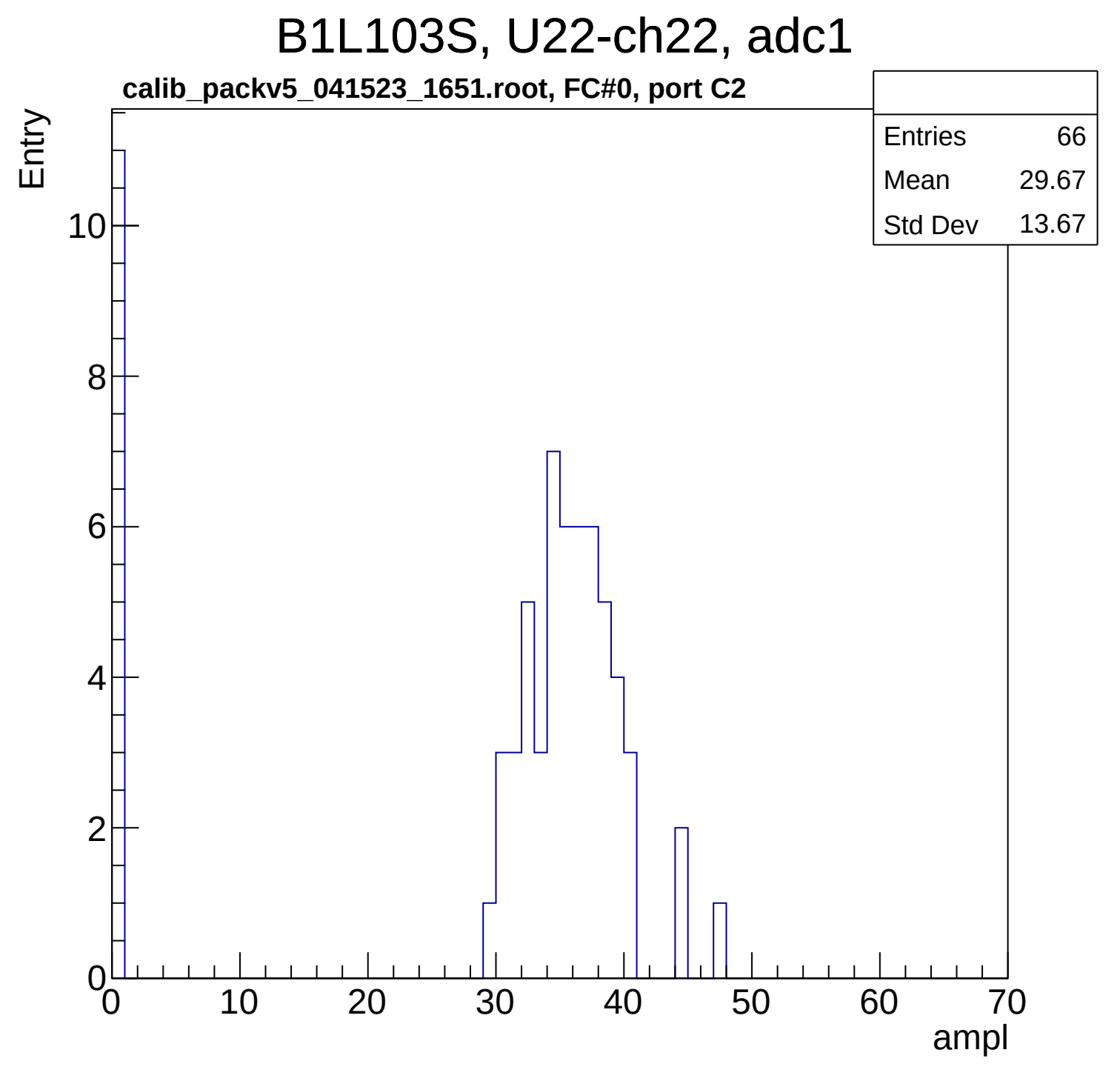
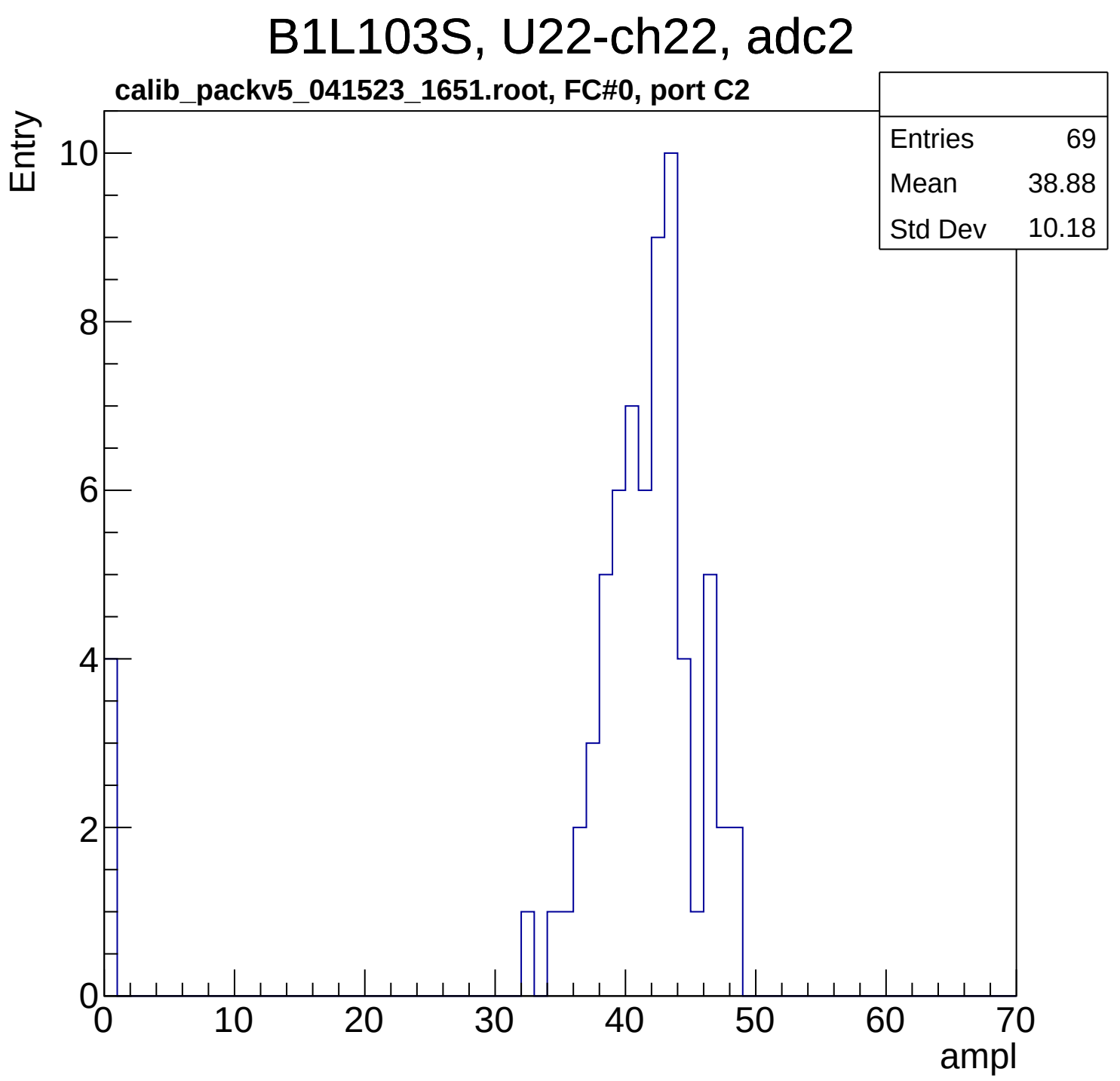
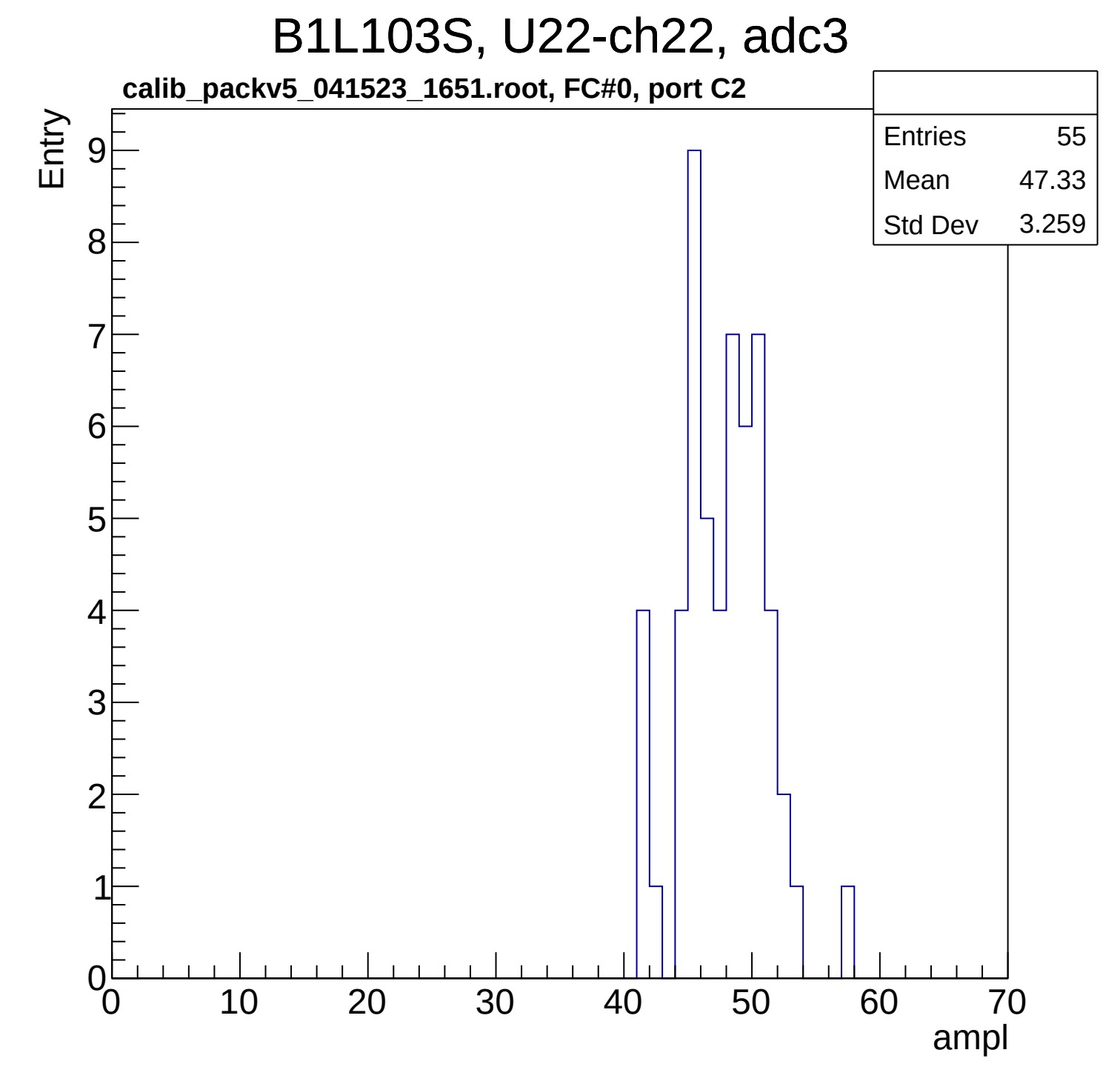
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch22, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 29.67
Std Dev 13.67
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch22, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 38.88
Std Dev 10.18
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U22-ch22, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 47.33
Std Dev 3.259
Entry
ampl
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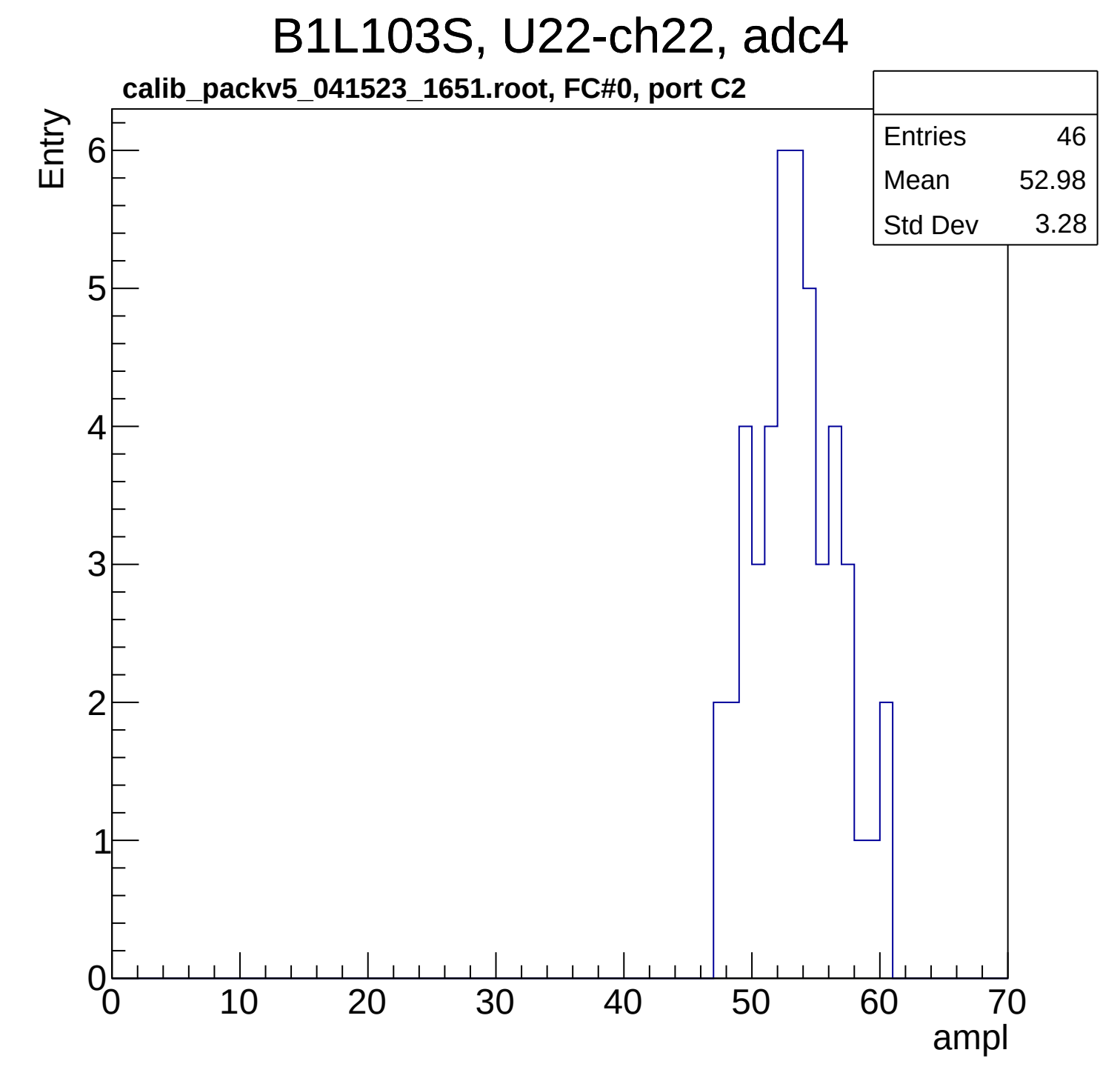
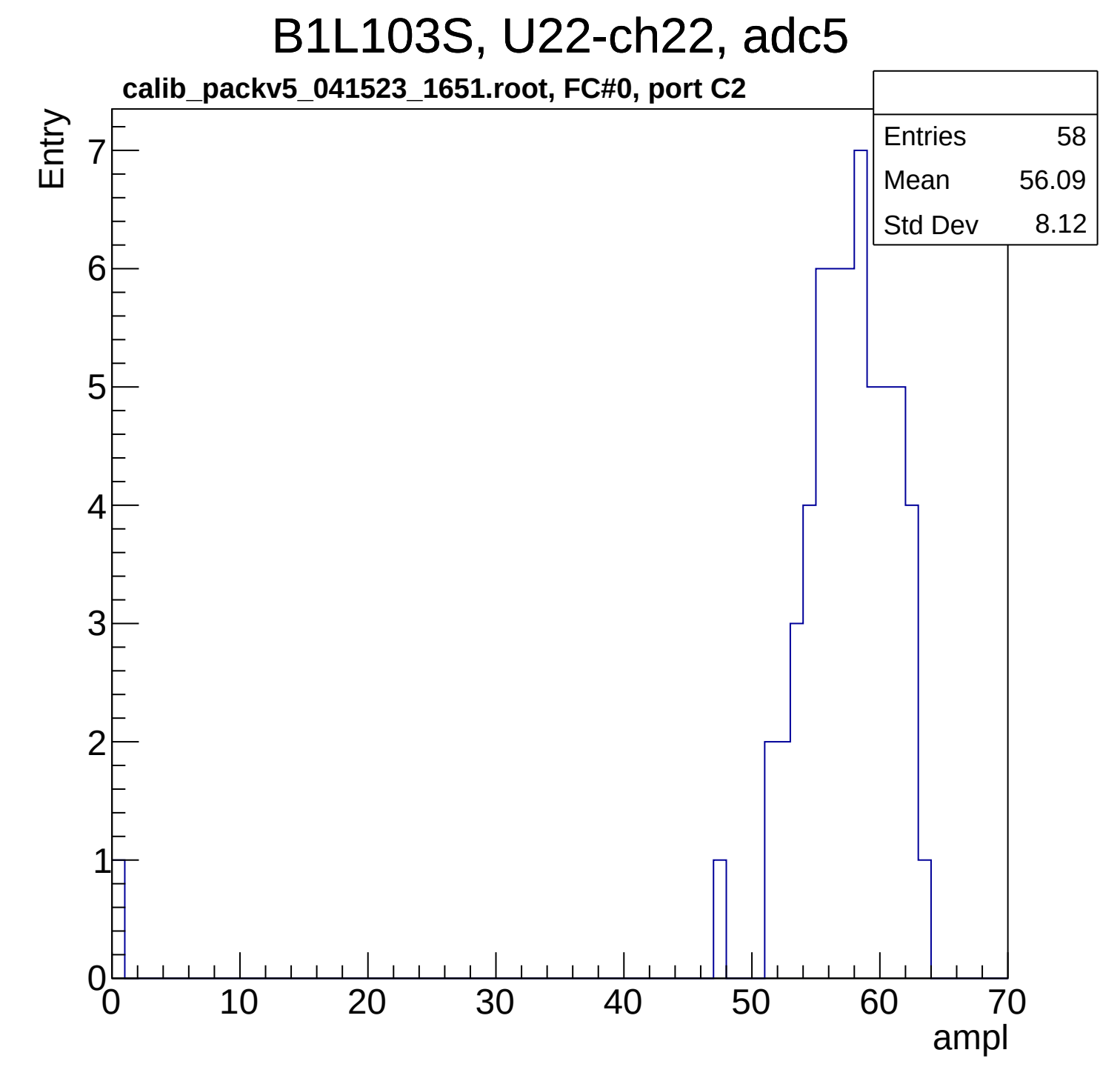
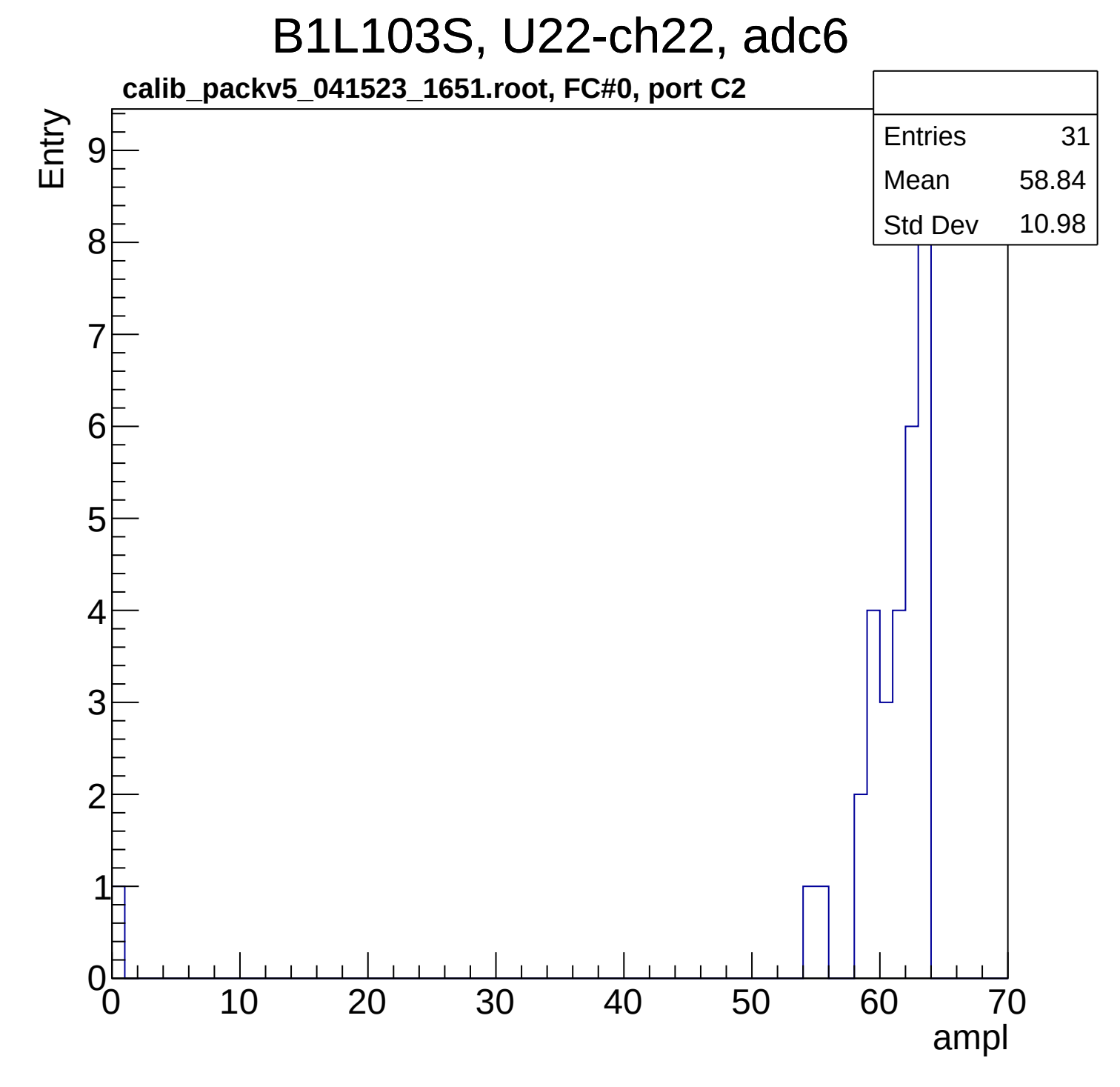
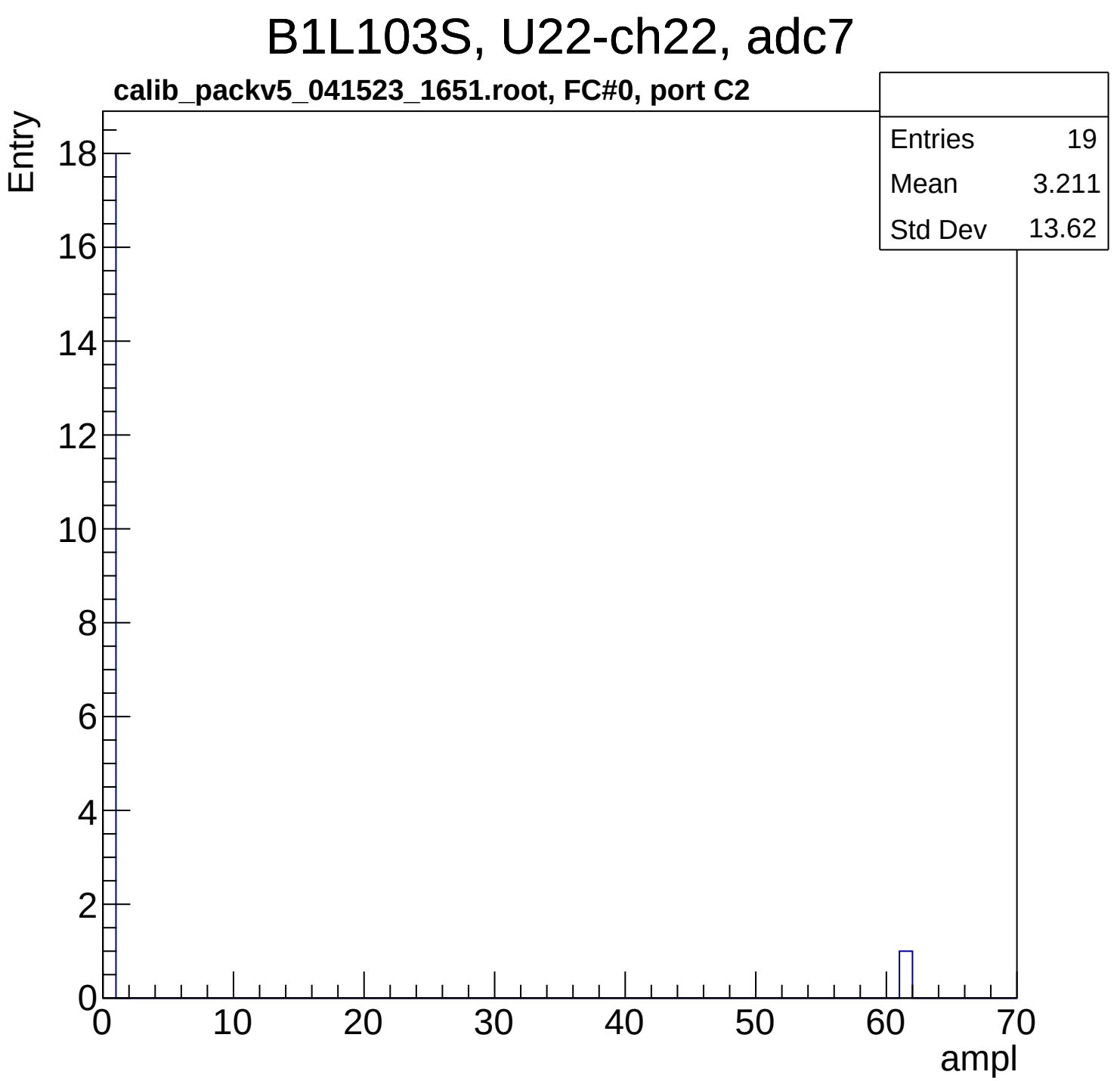
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch22, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 52.98
Std Dev 3.28
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U22-ch22, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 56.09
Std Dev 8.12
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U22-ch22, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 58.84
Std Dev 10.98
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch22, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.211
Std Dev 13.62
Entry
ampl
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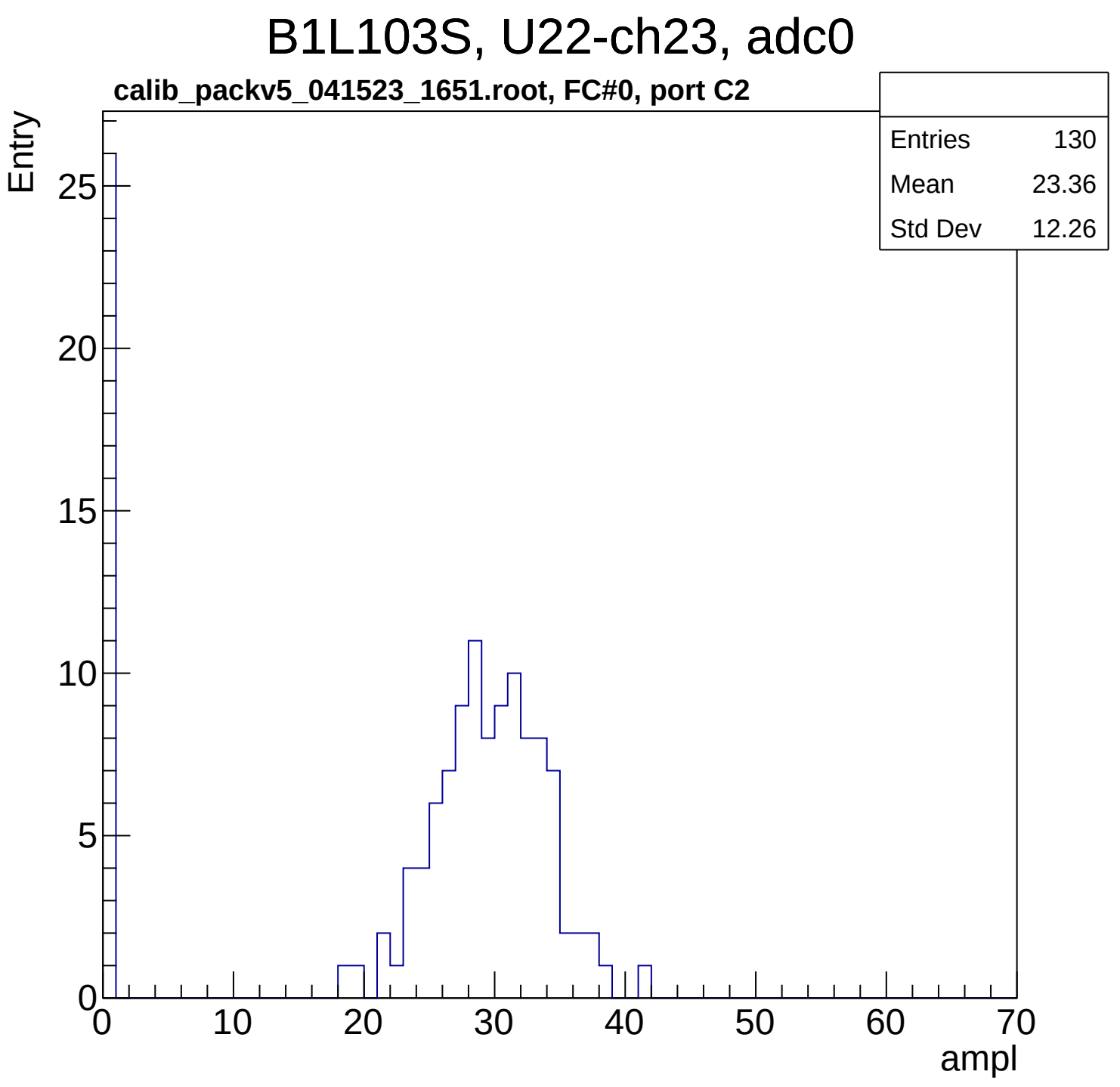
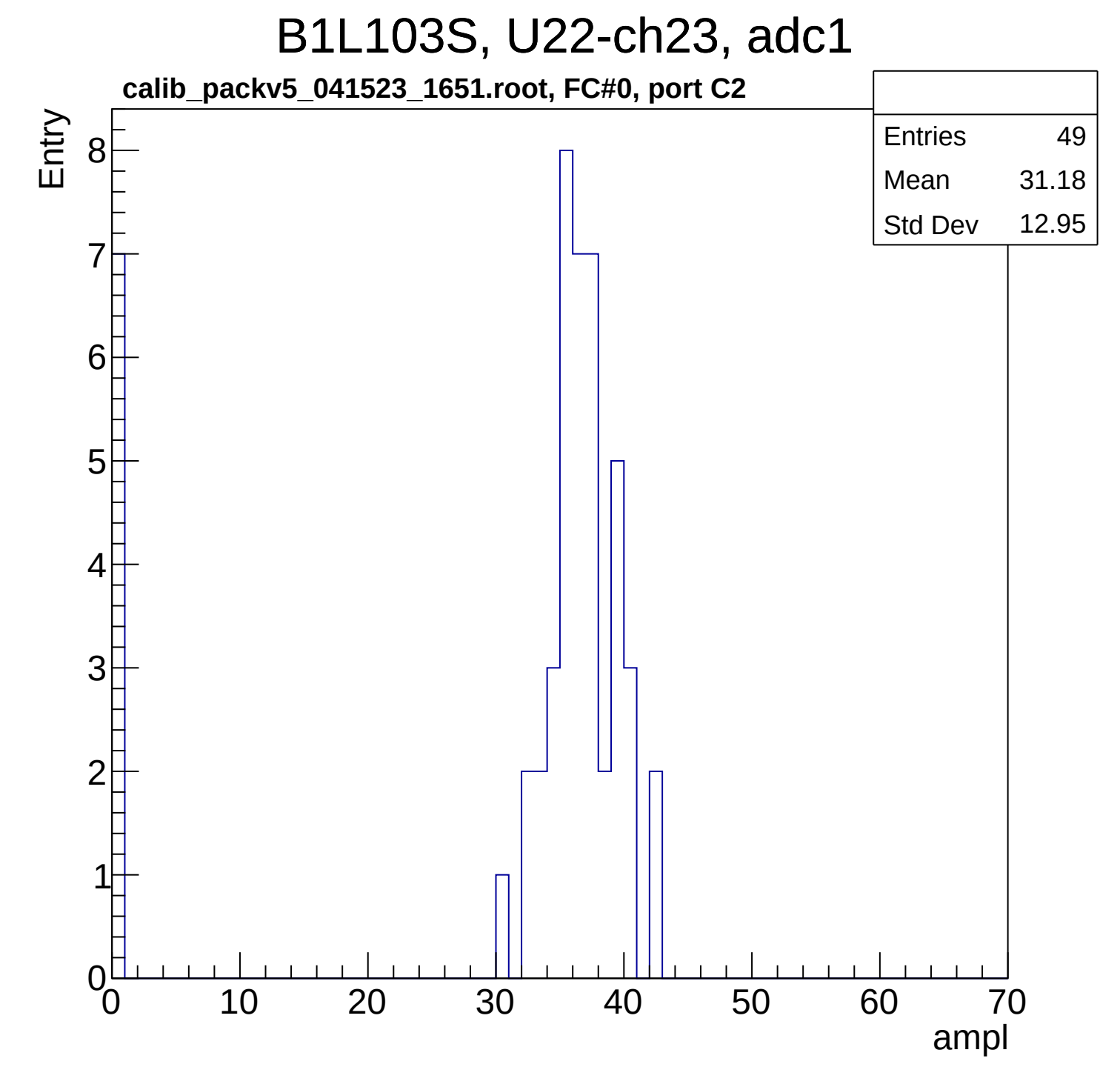
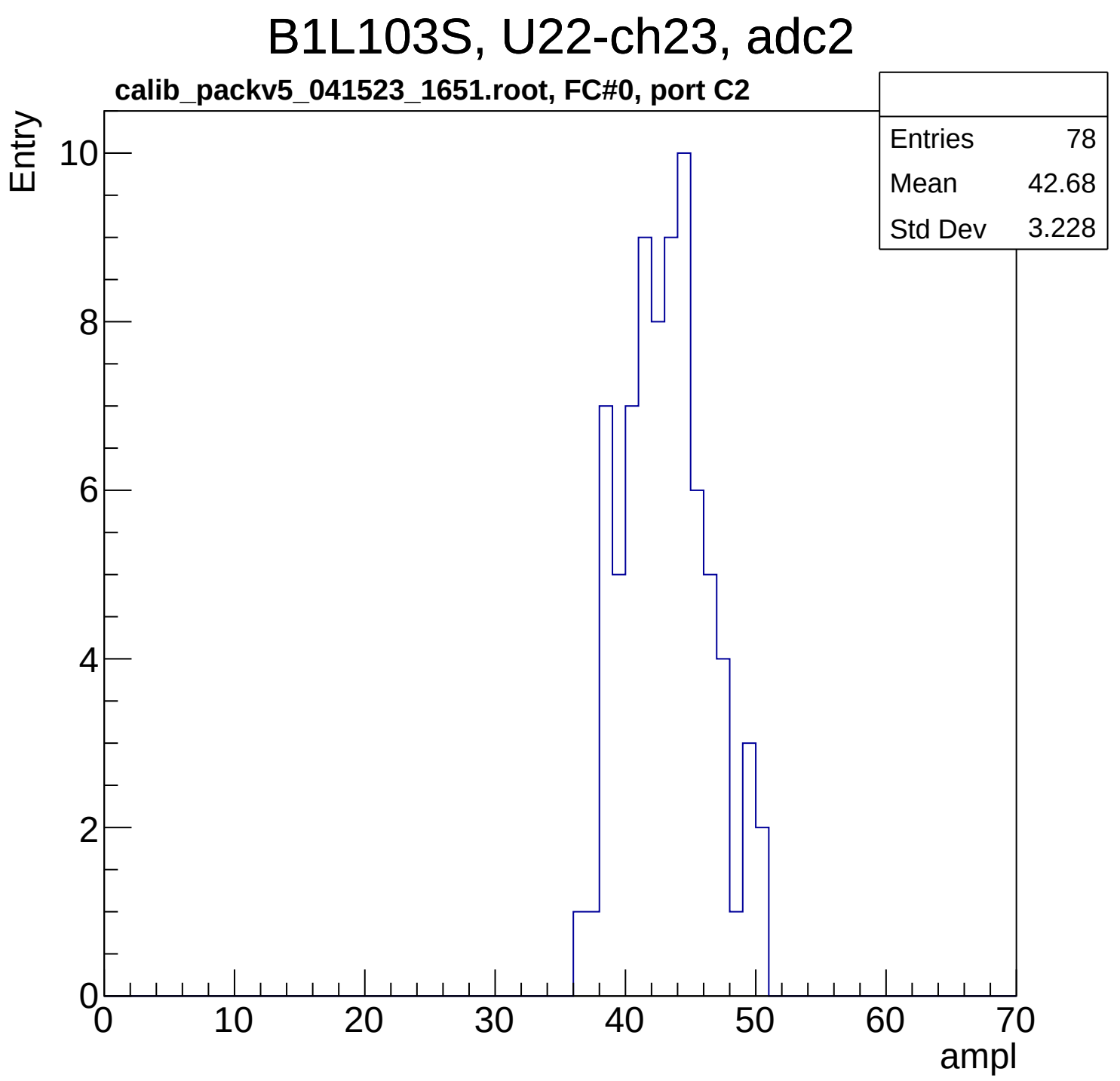
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L103S, U22-ch23, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 130
Mean 23.36
Std Dev 12.26
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch23, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 31.18
Std Dev 12.95
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch23, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 42.68
Std Dev 3.228
Entry
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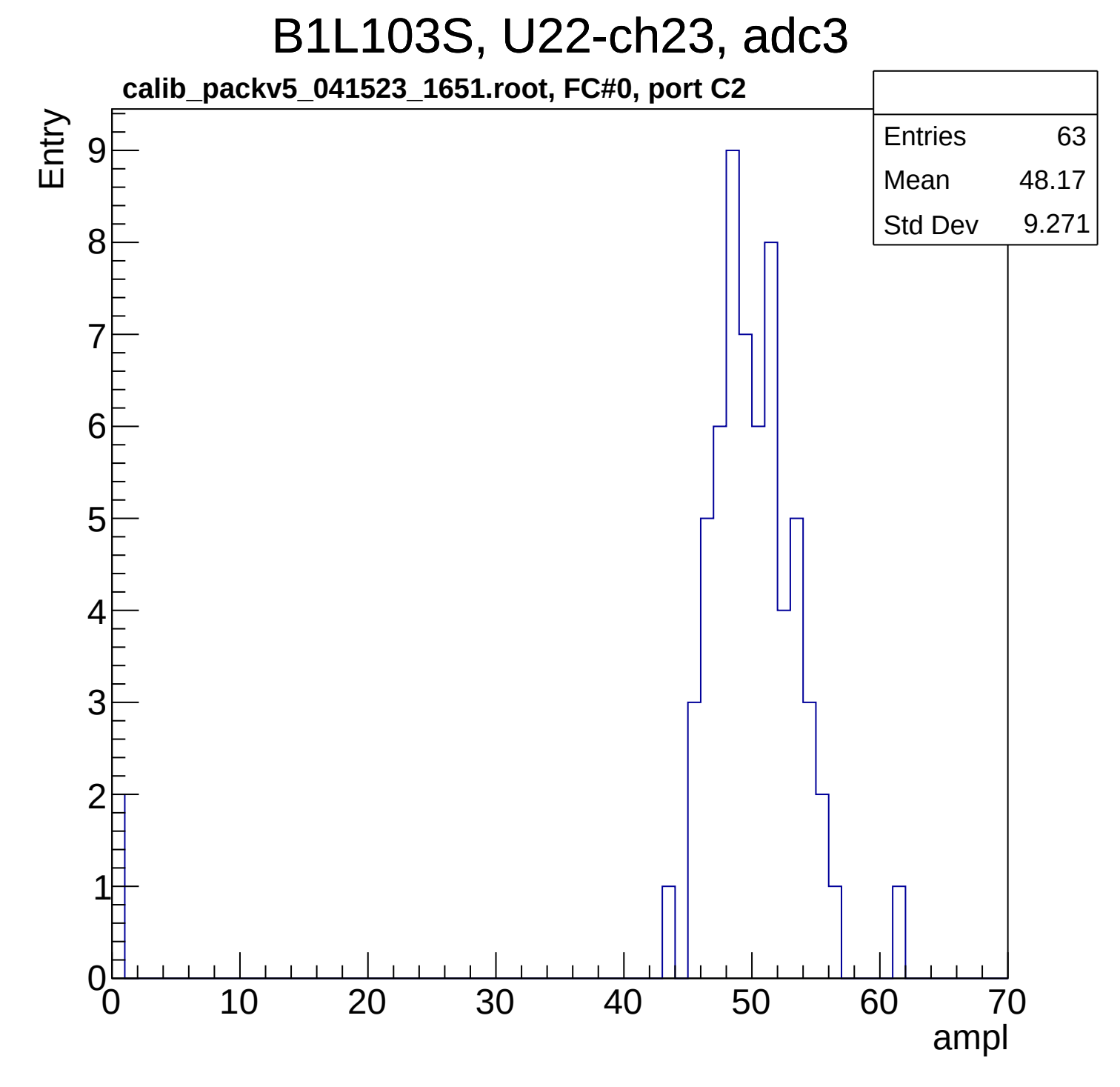
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch23, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 48.17
Std Dev 9.271
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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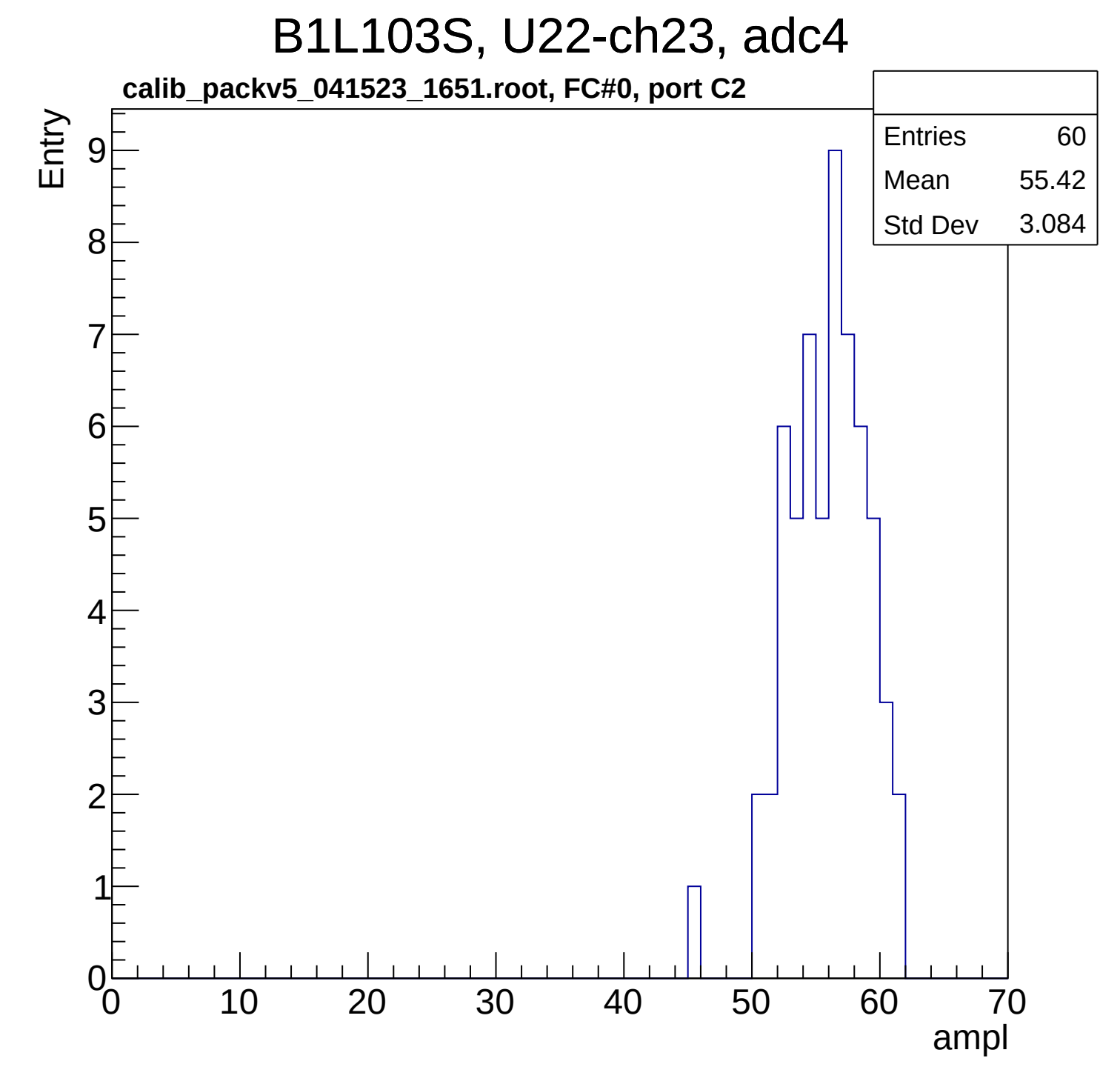
50
60
70


B1L103S, U22-ch23, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 55.42
Std Dev 3.084
Entry
ampl
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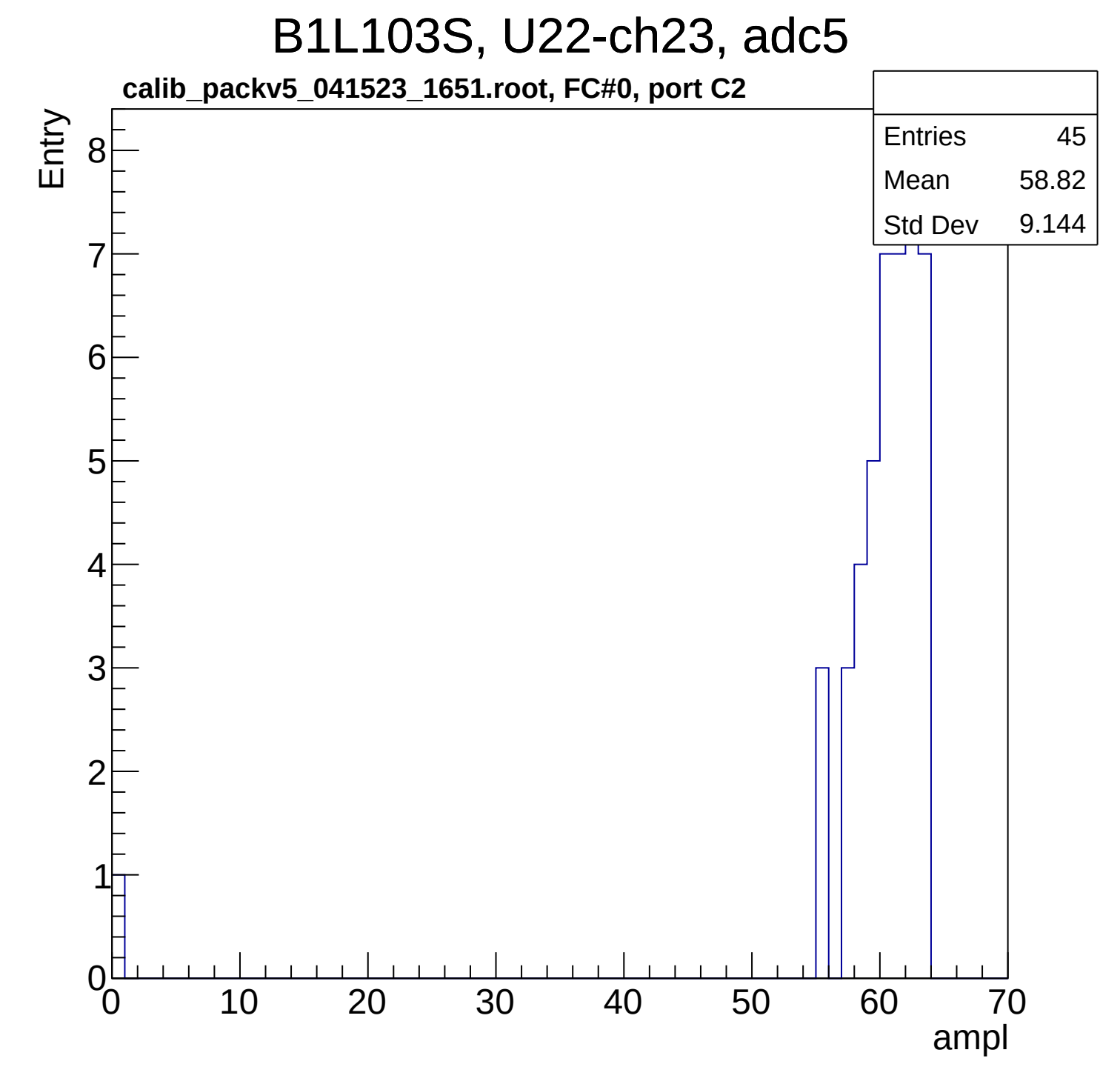
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch23, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 58.82
Std Dev 9.144
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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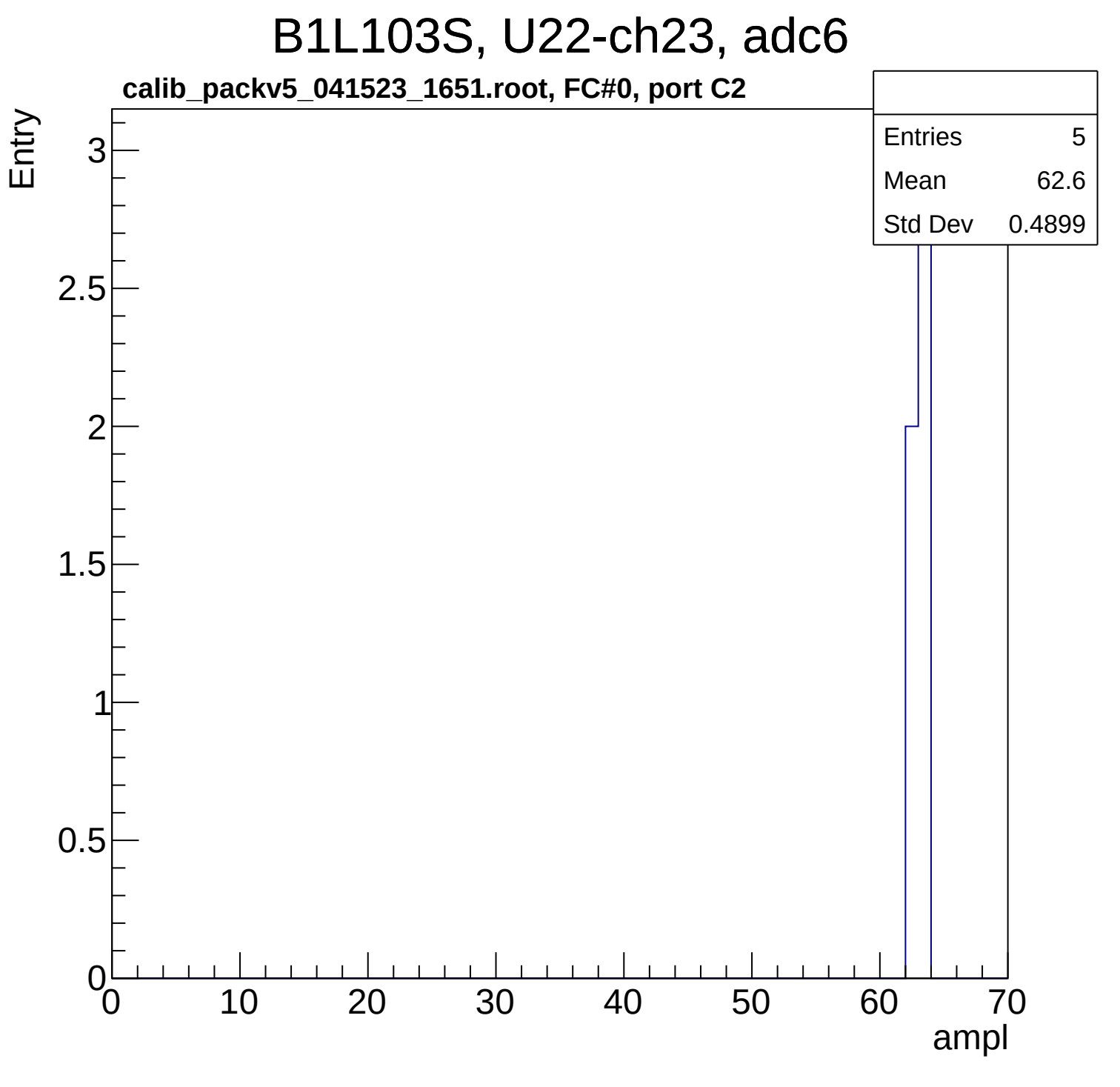
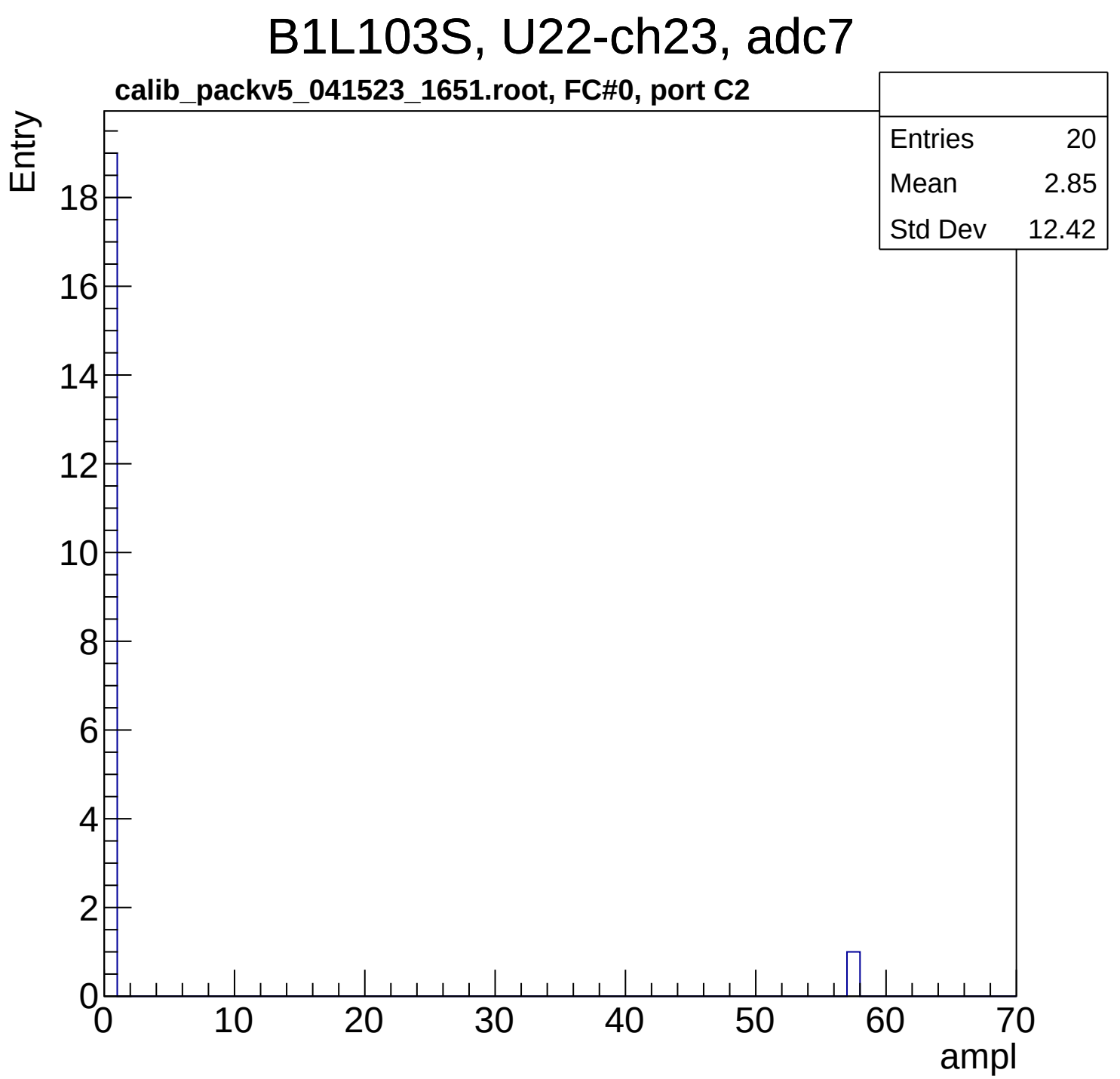
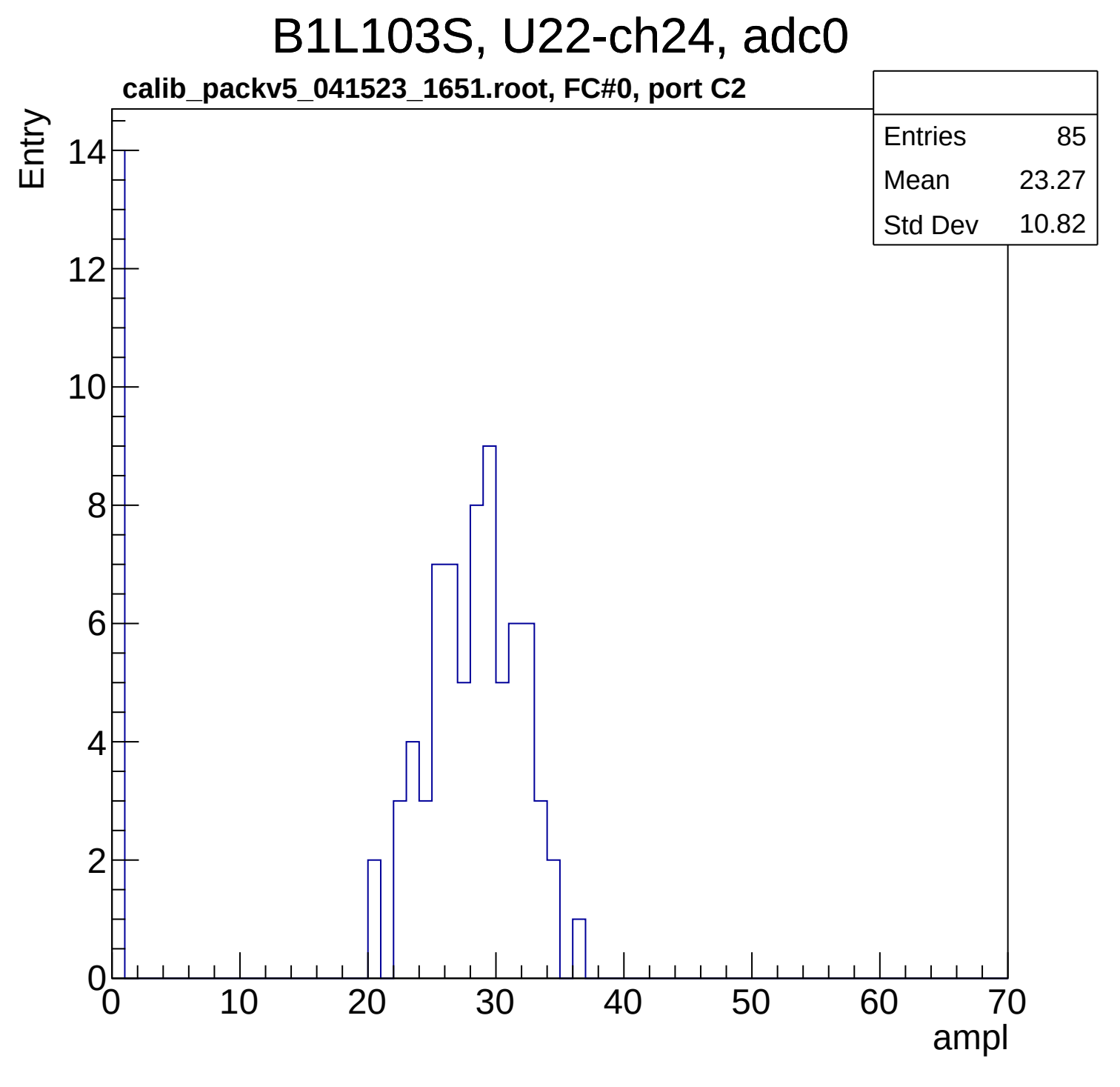
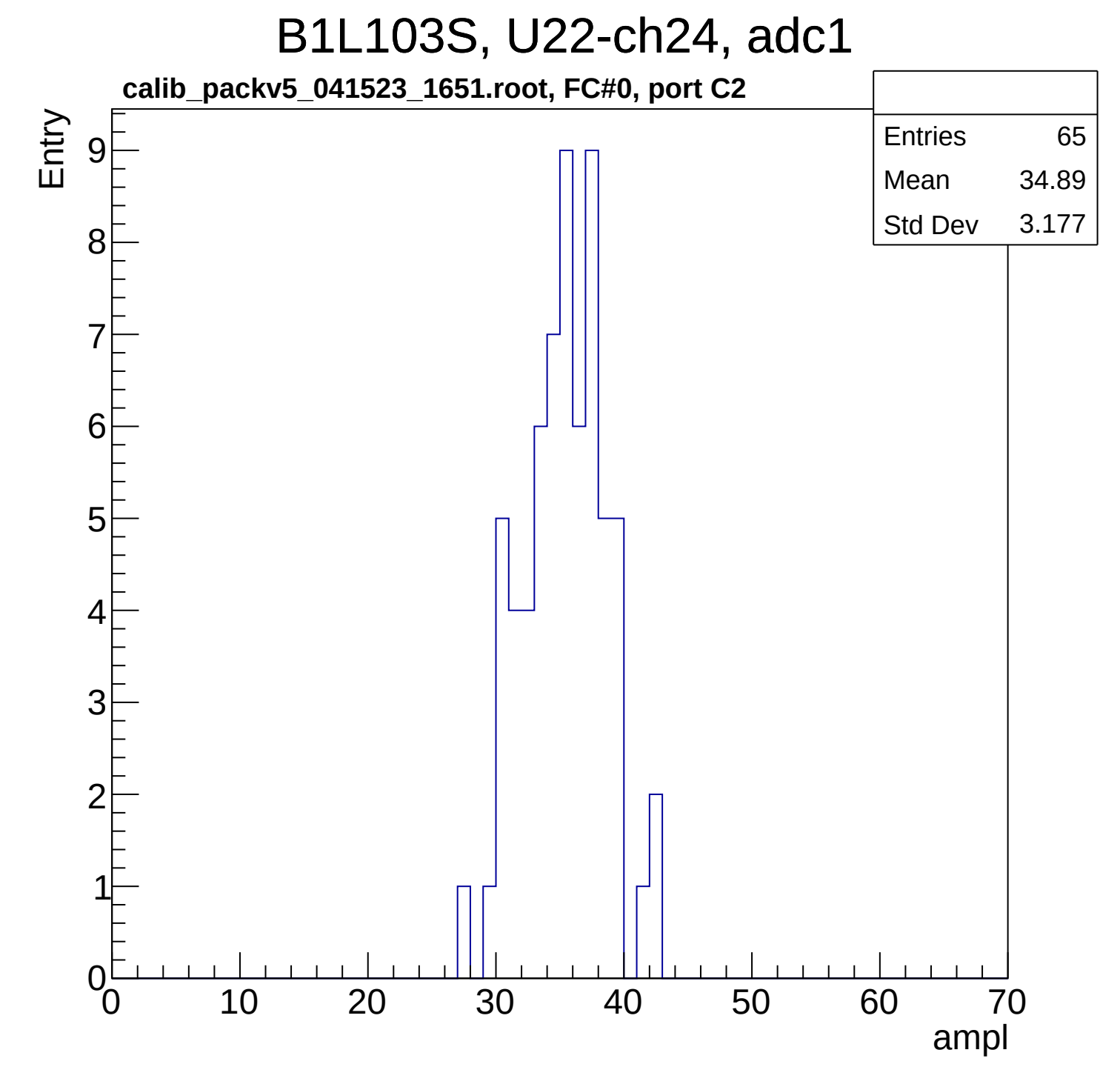
40
50
60
70


B1L103S, U22-ch23, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 62.6
Std Dev 0.4899
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U22-ch23, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 2.85
Std Dev 12.42
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch24, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 23.27
Std Dev 10.82
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U22-ch24, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 34.89
Std Dev 3.177
Entry
ampl
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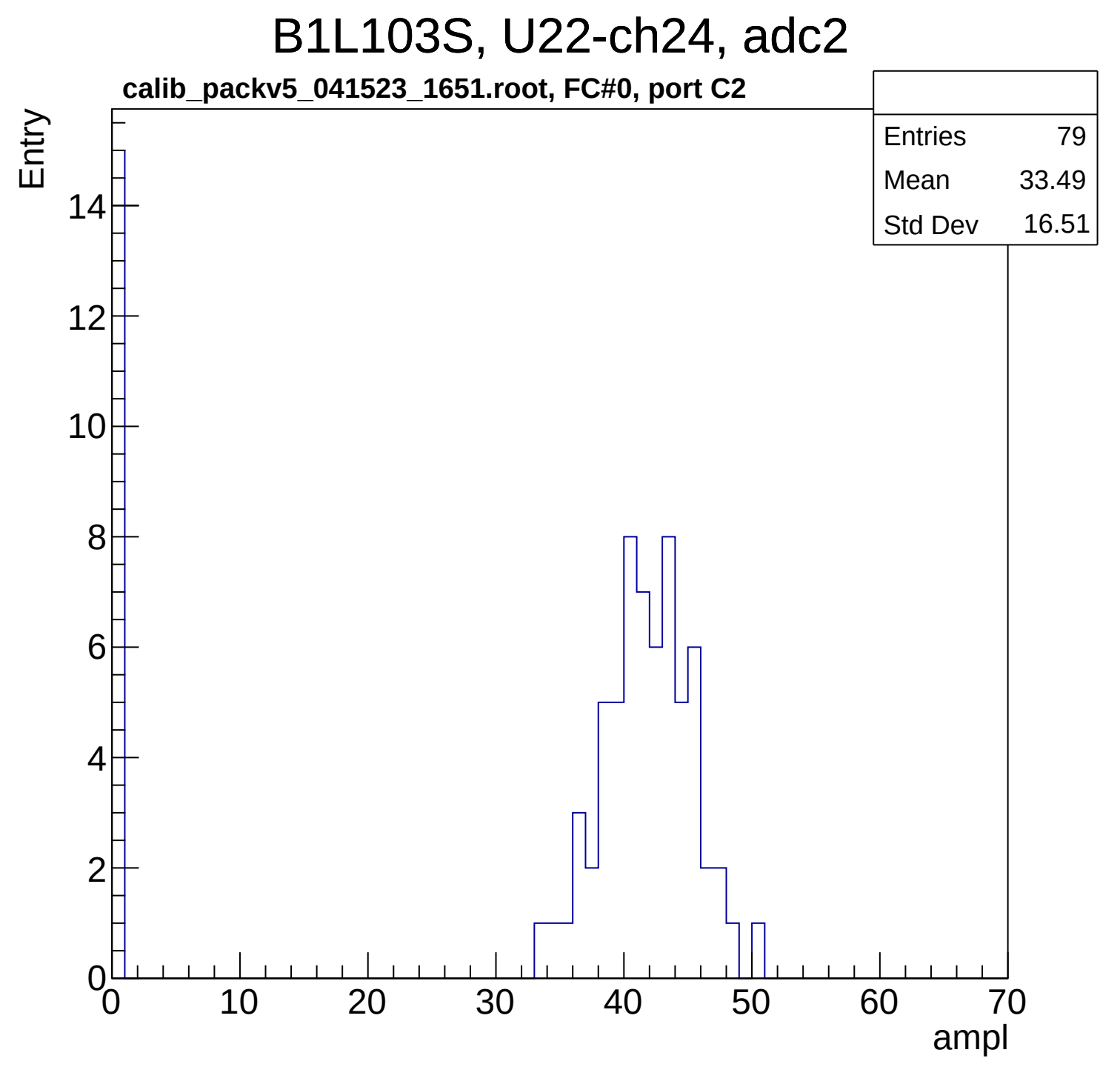
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch24, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 33.49
Std Dev 16.51
Entry
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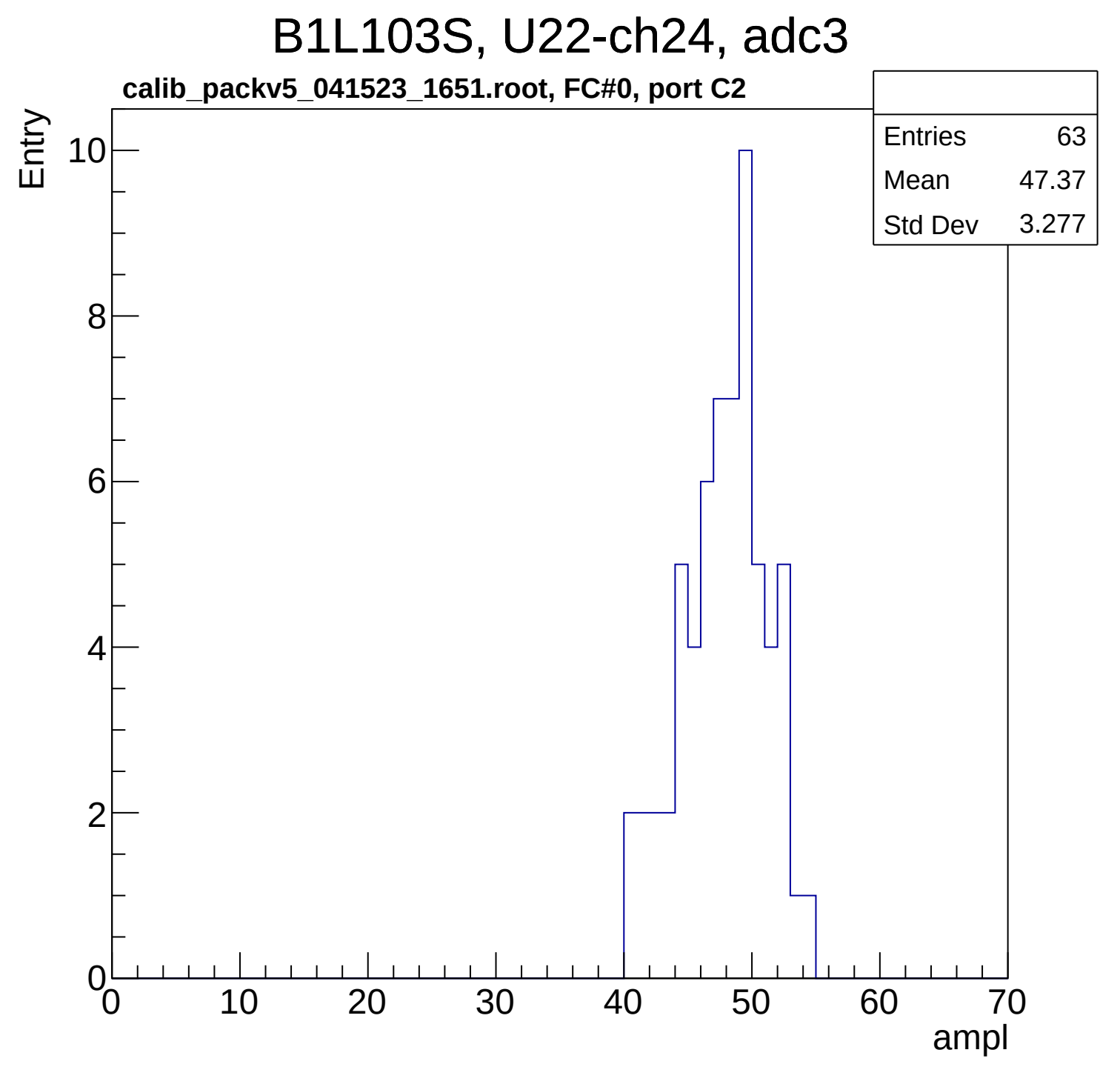
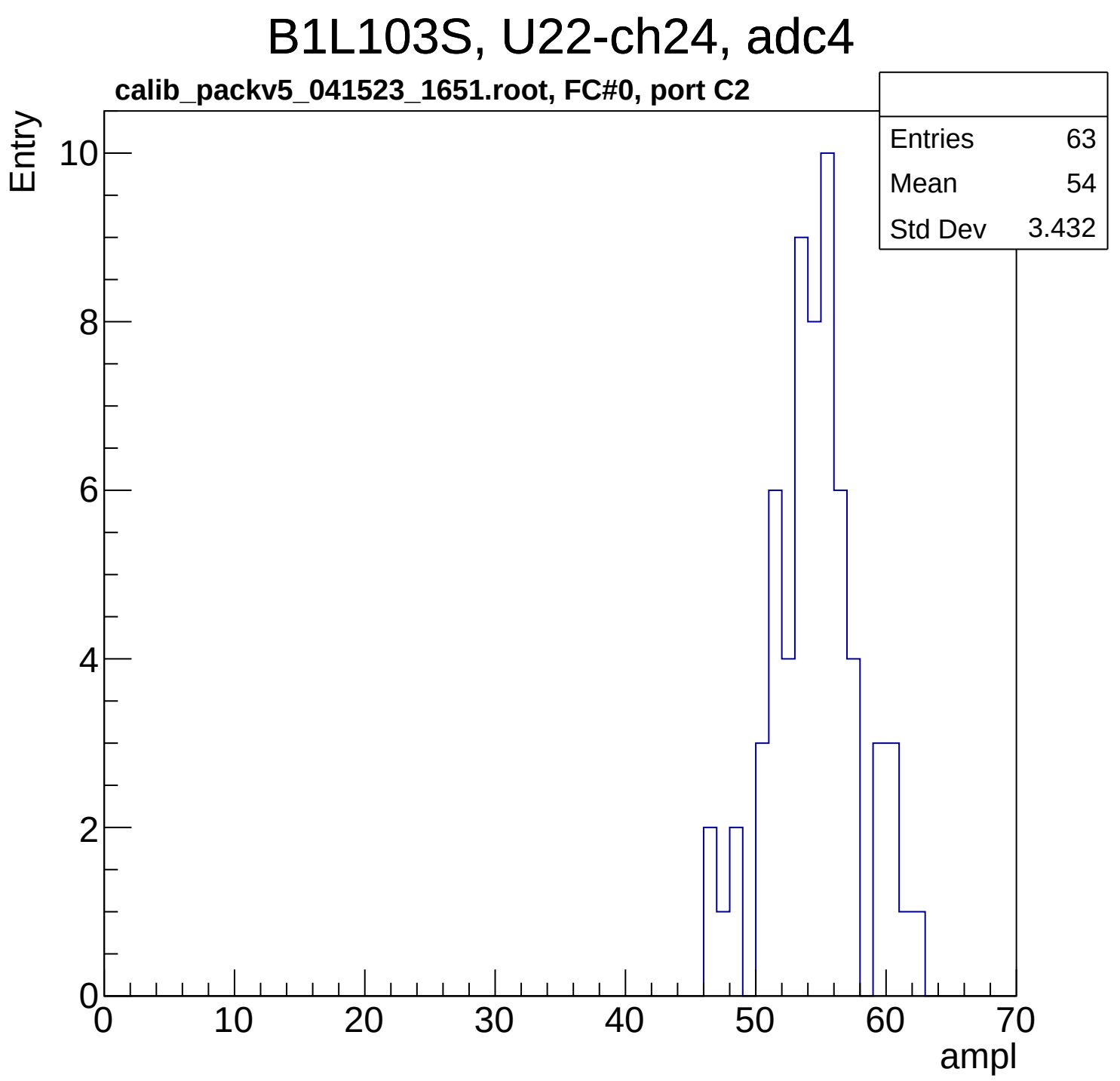
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch24, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 47.37
Std Dev 3.277
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U22-ch24, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 54
Std Dev 3.432
Entry
ampl
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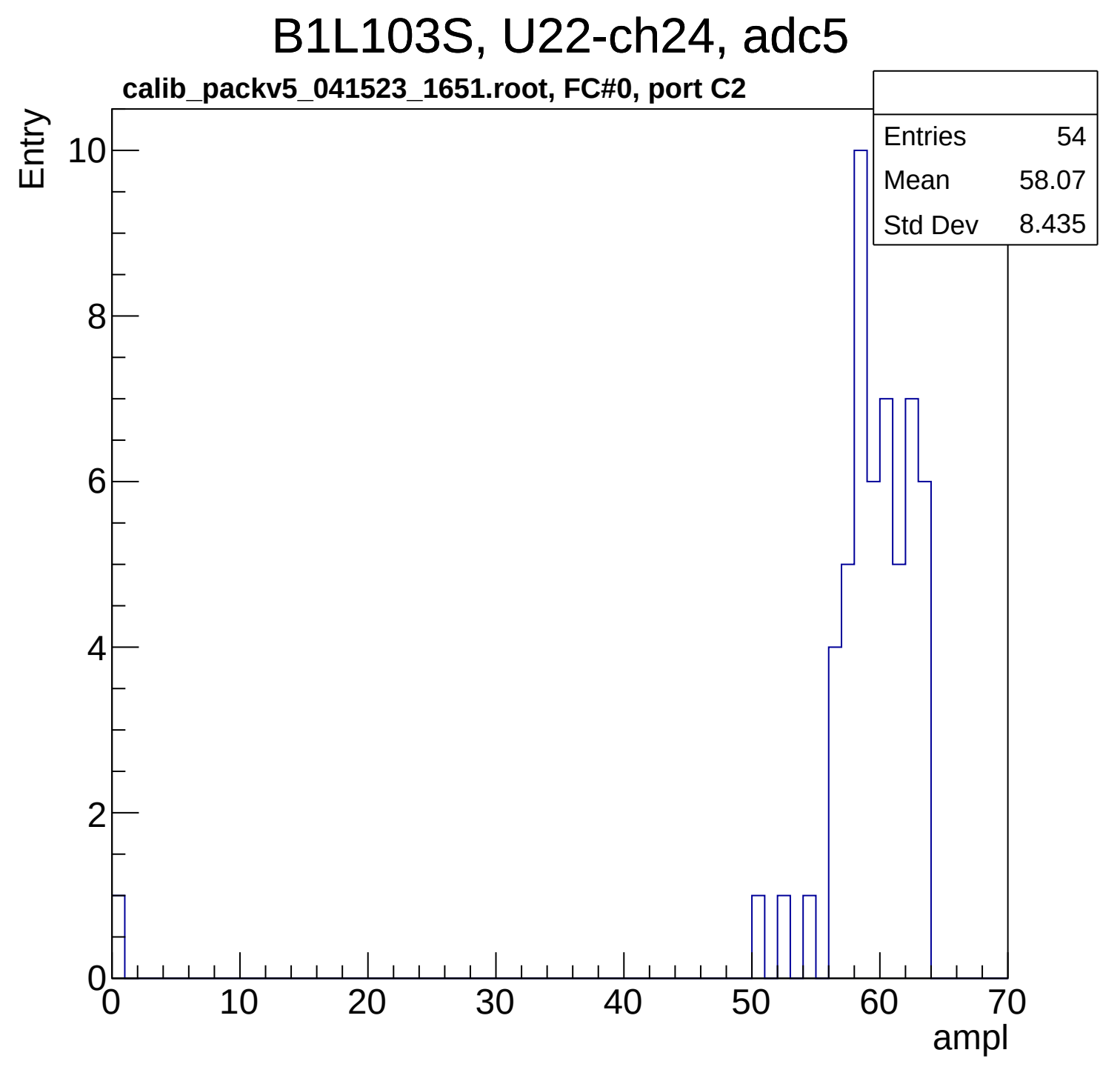
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U22-ch24, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 58.07
Std Dev 8.435
Entry
ampl
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4
6
8
10
0
10
20
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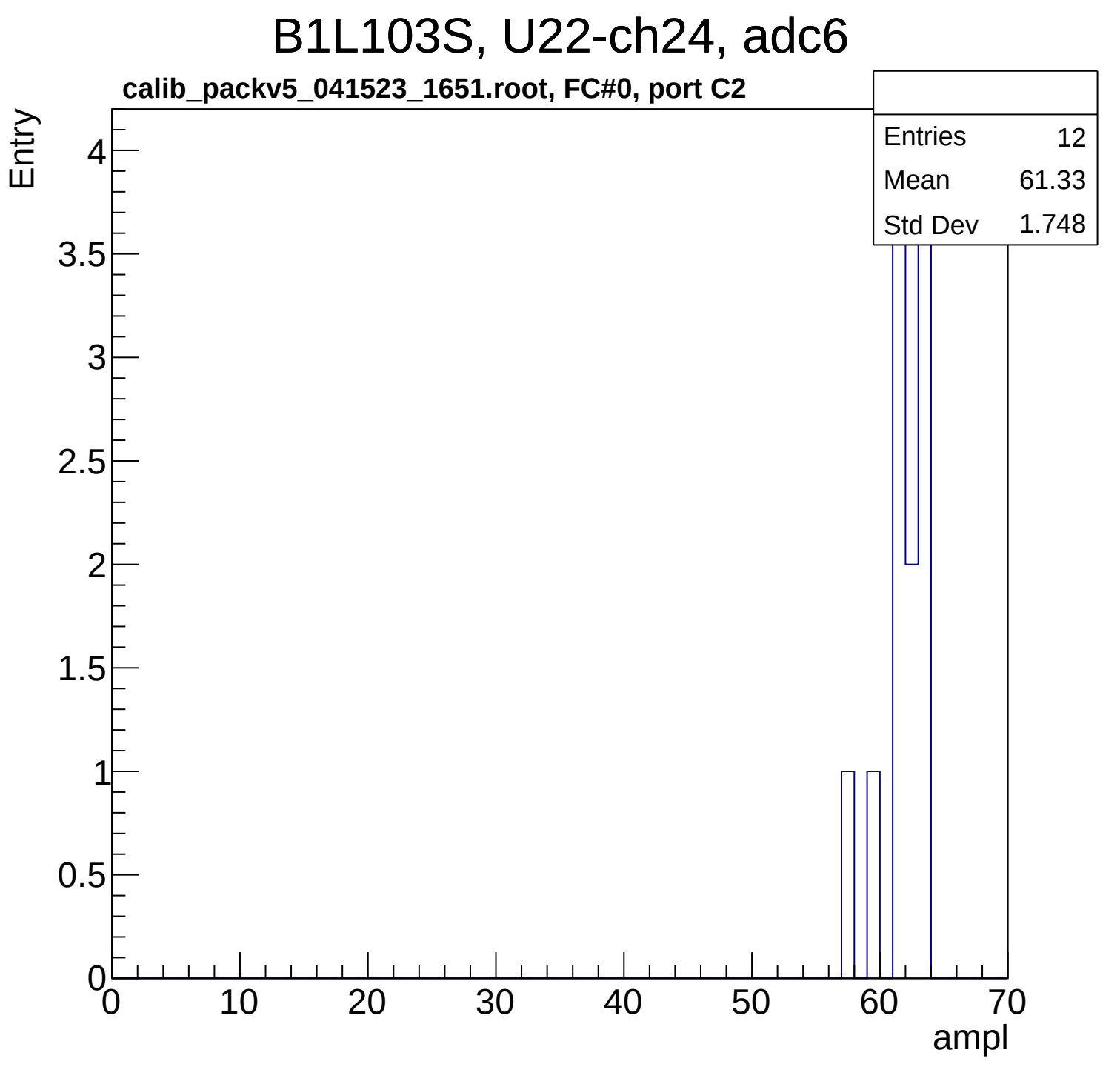
40
50
60
70


B1L103S, U22-ch24, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.33
Std Dev 1.748
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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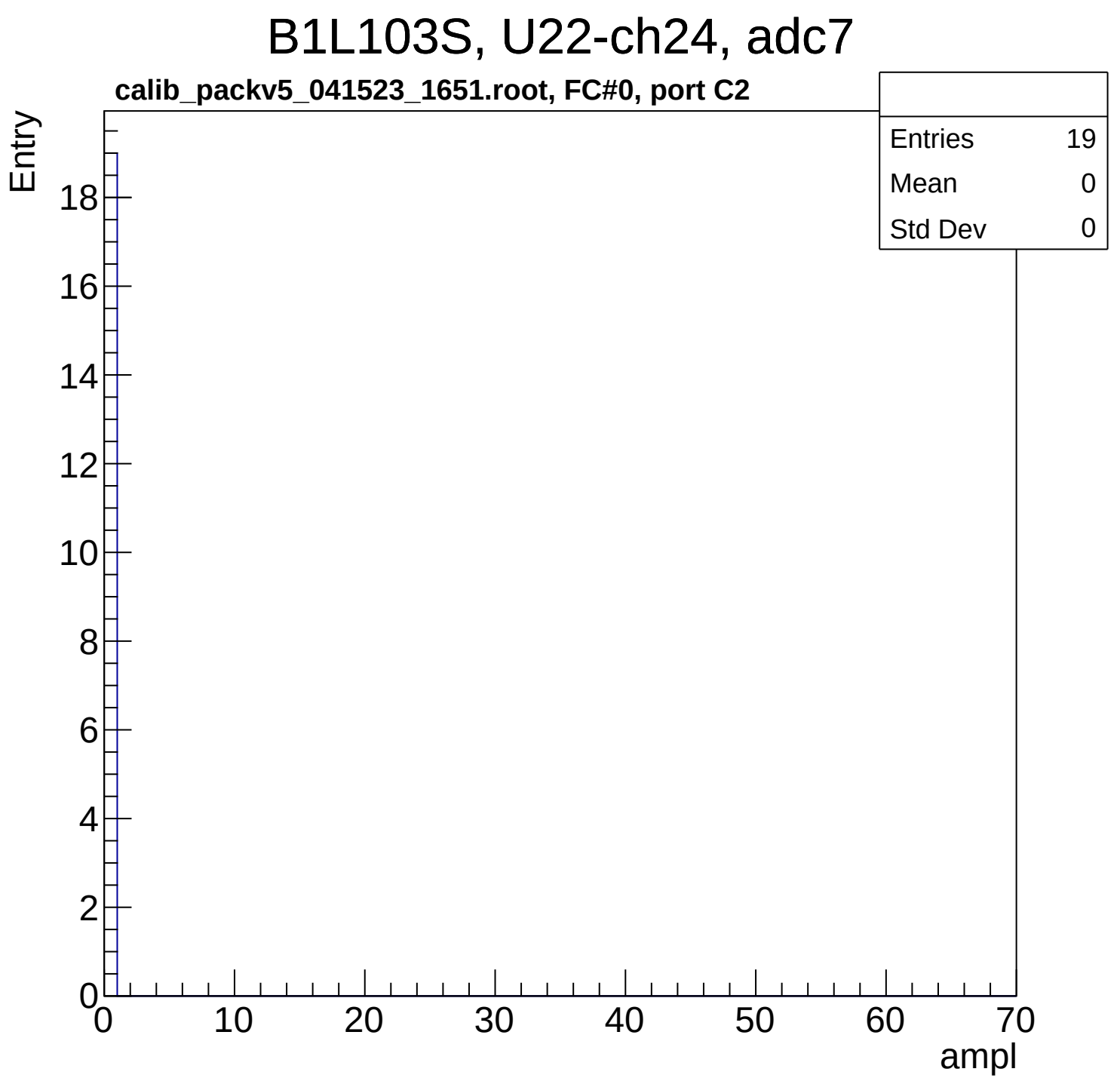
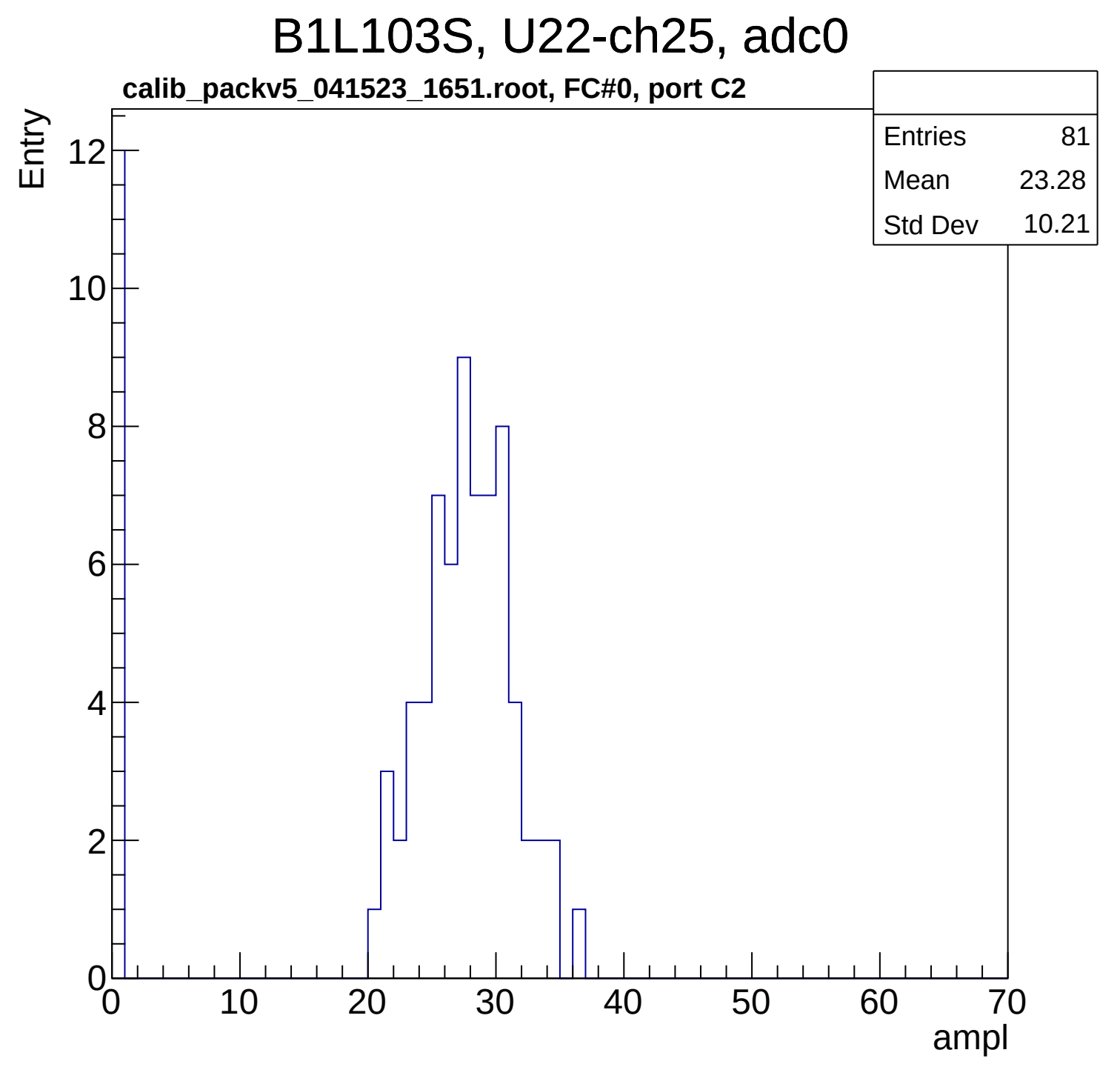
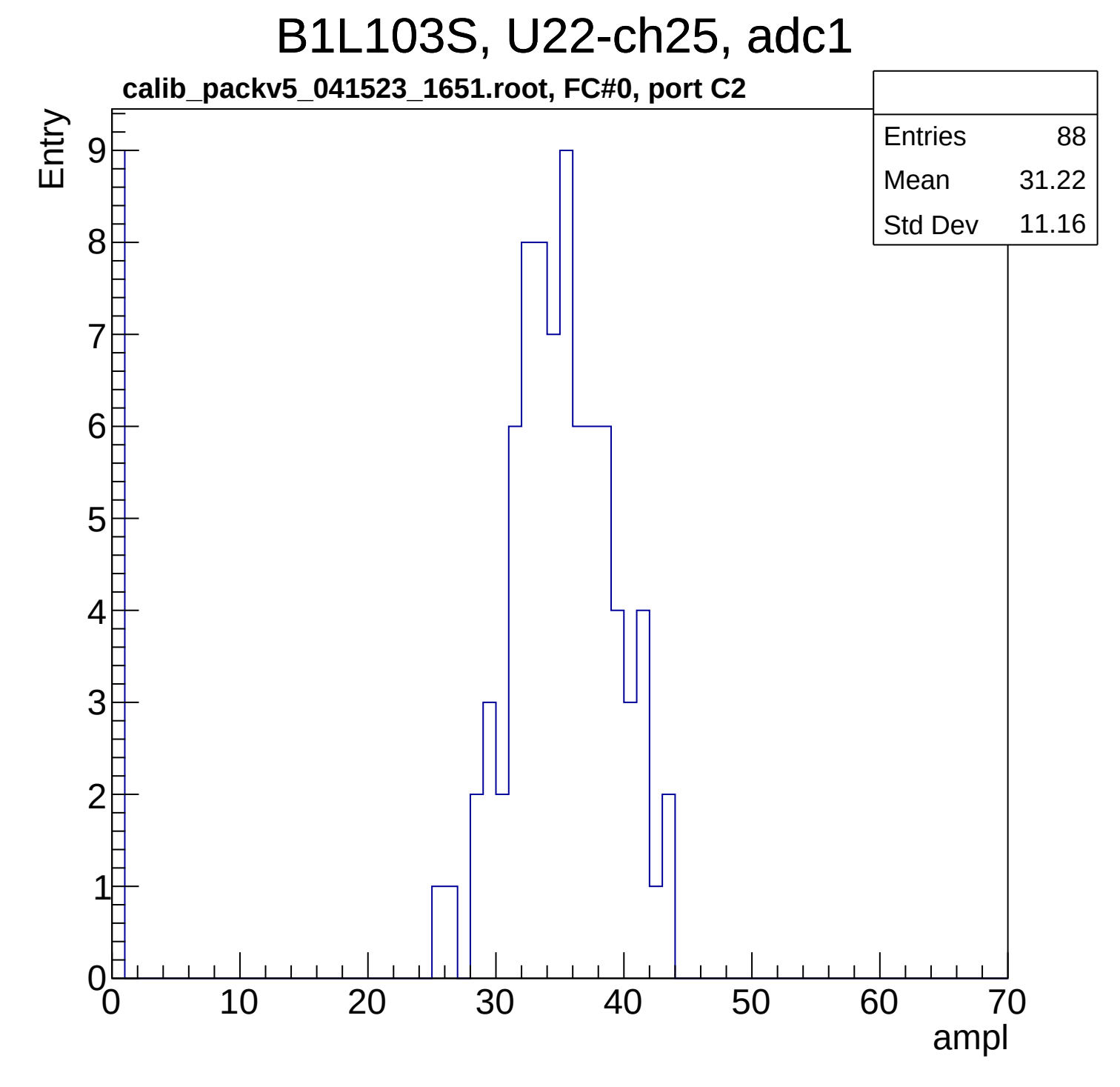

B1L103S, U22-ch24, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch25, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 23.28
Std Dev 10.21
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch25, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 31.22
Std Dev 11.16
Entry
ampl
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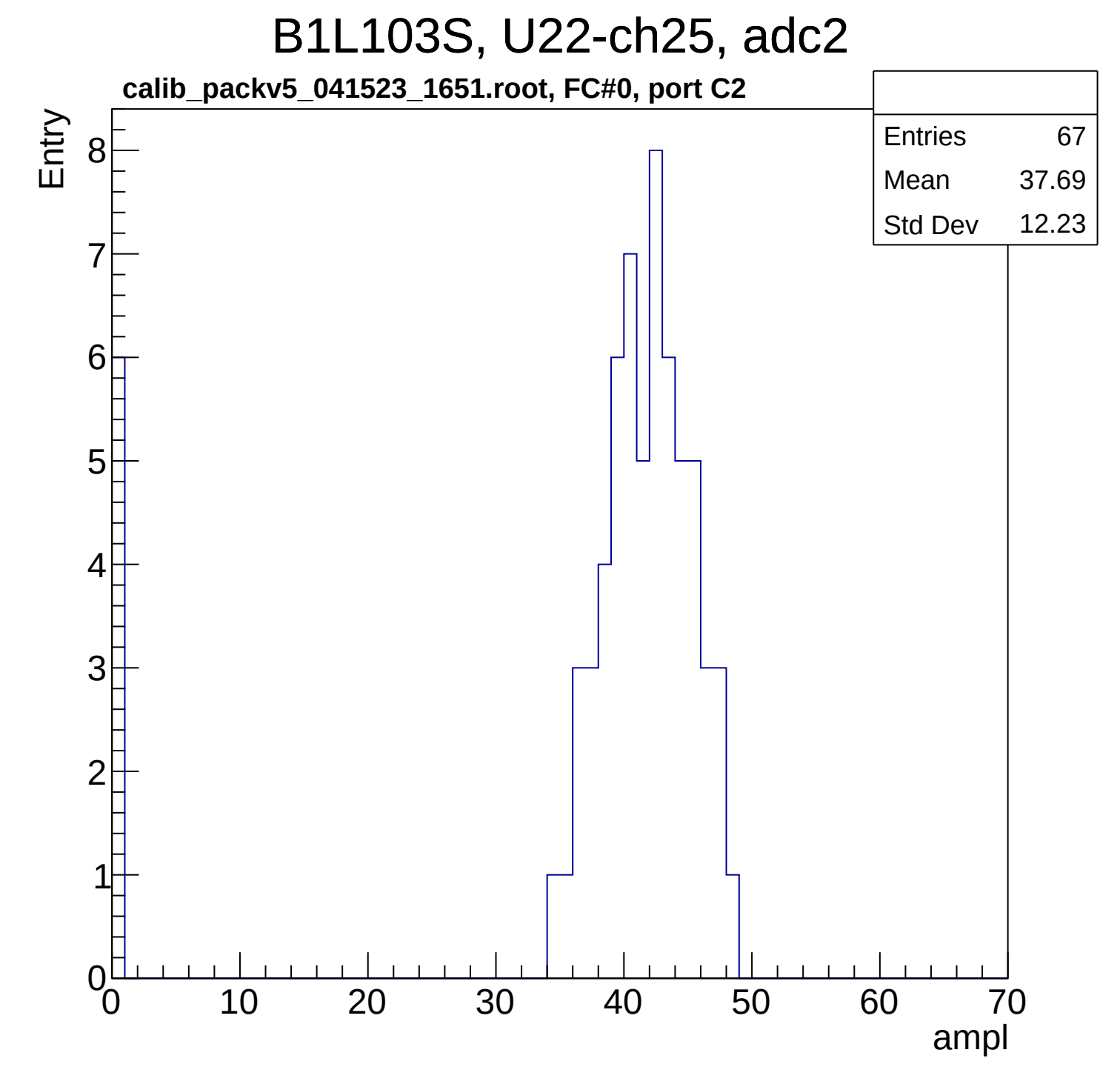
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch25, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 37.69
Std Dev 12.23
Entry
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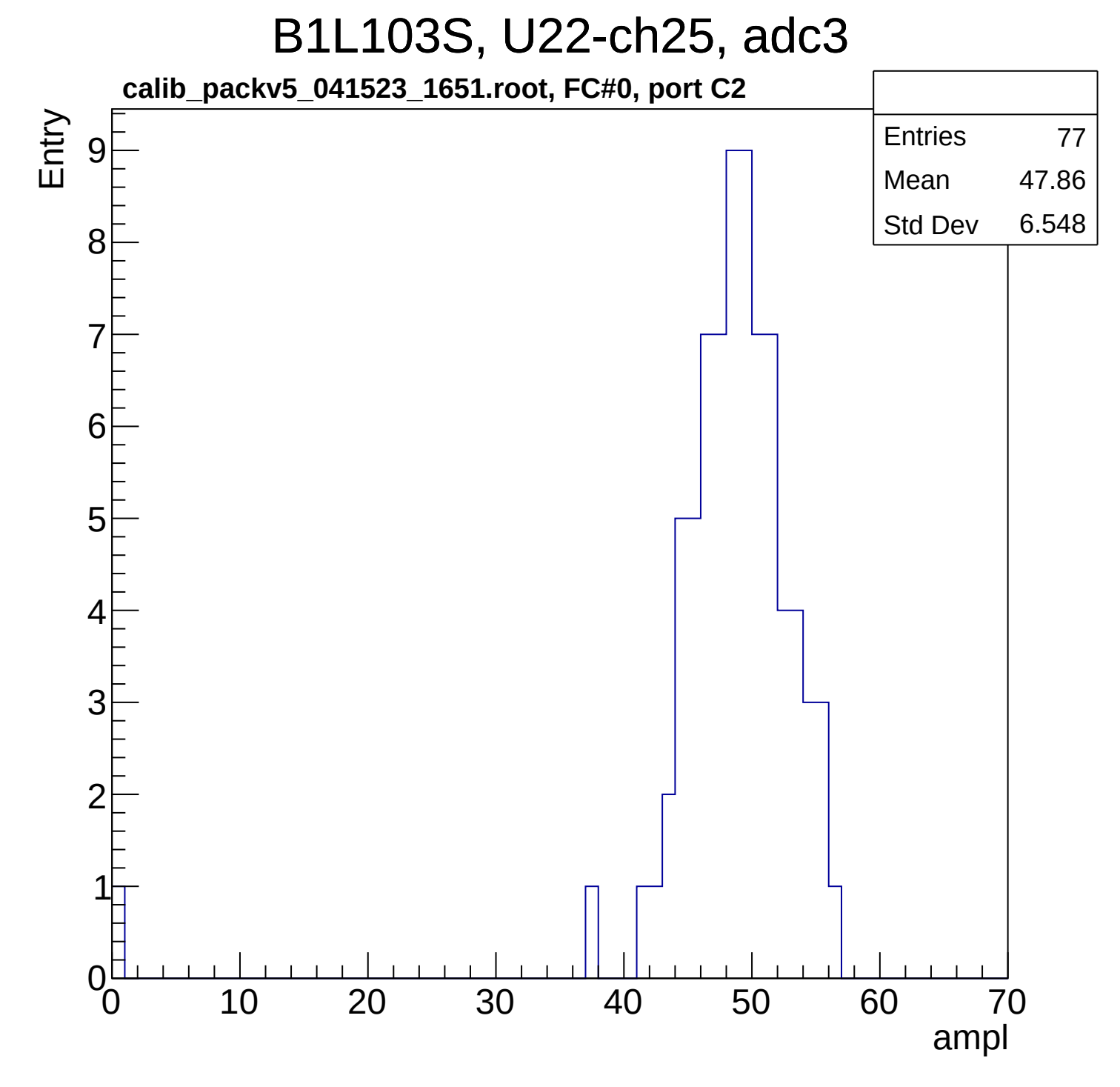
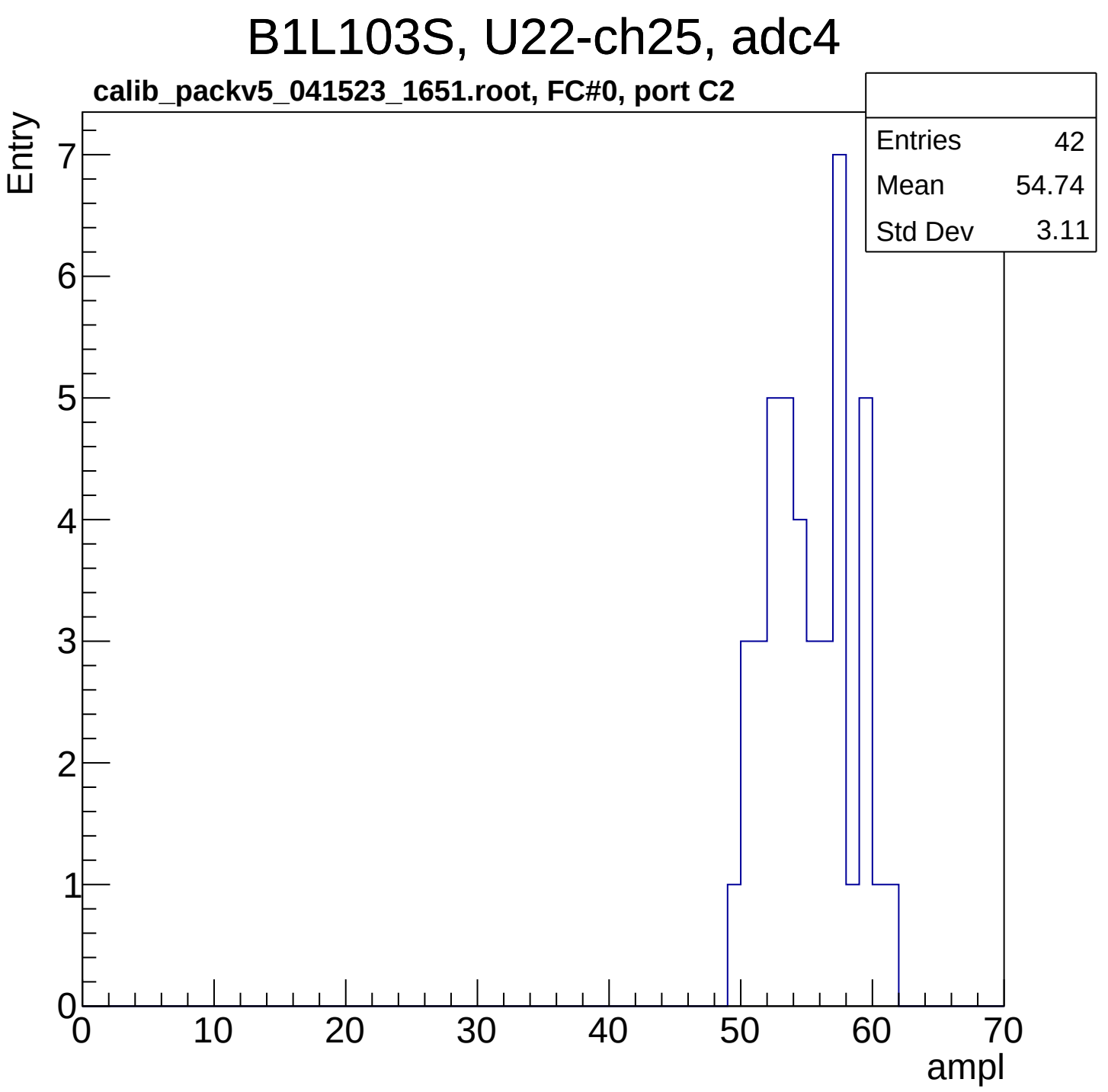
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch25, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 47.86
Std Dev 6.548
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch25, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 54.74
Std Dev 3.11
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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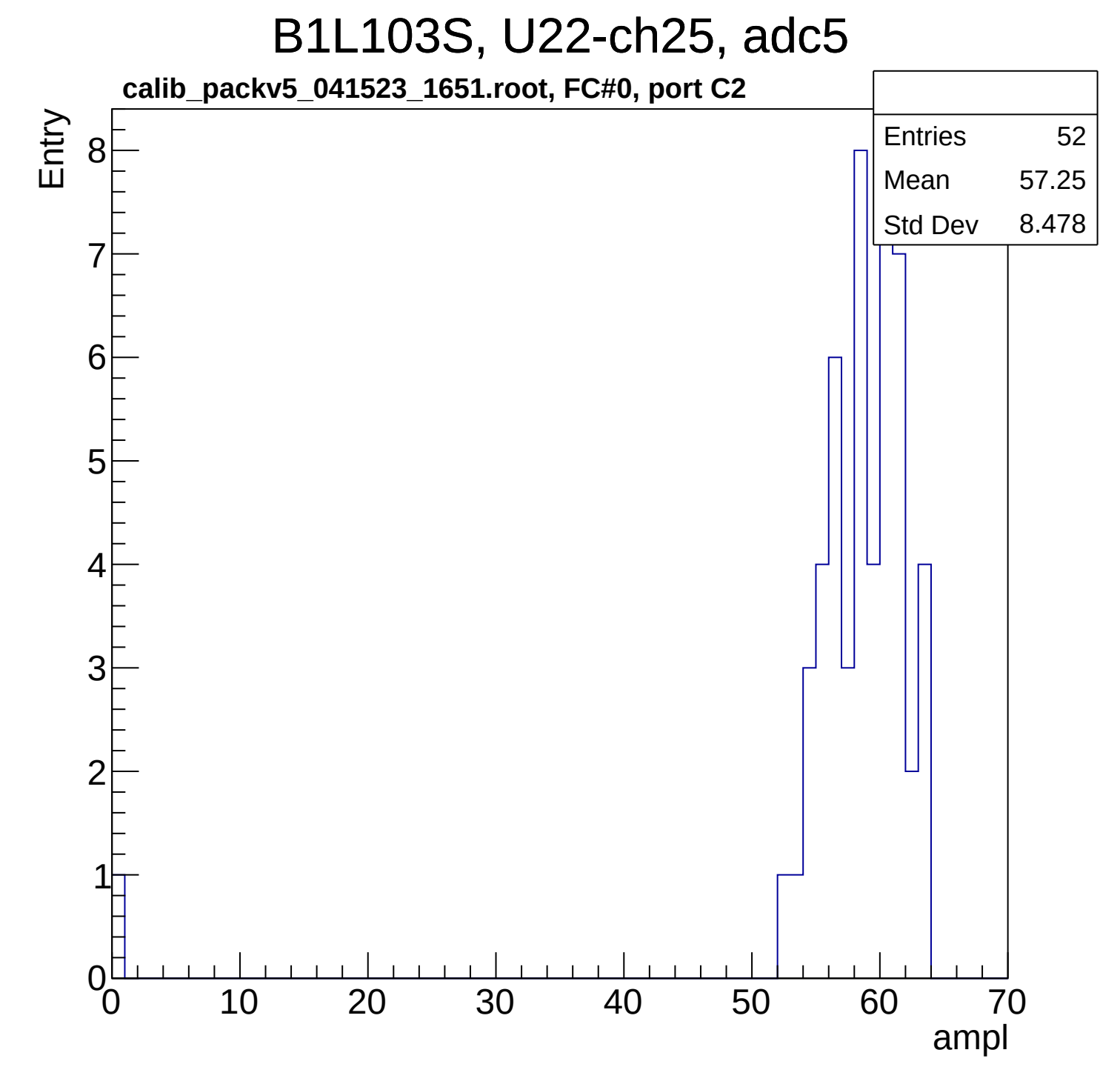
B1L103S, U22-ch25, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 57.25
Std Dev 8.478
Entry
ampl
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1
2
3
4
5
6
7
8
0
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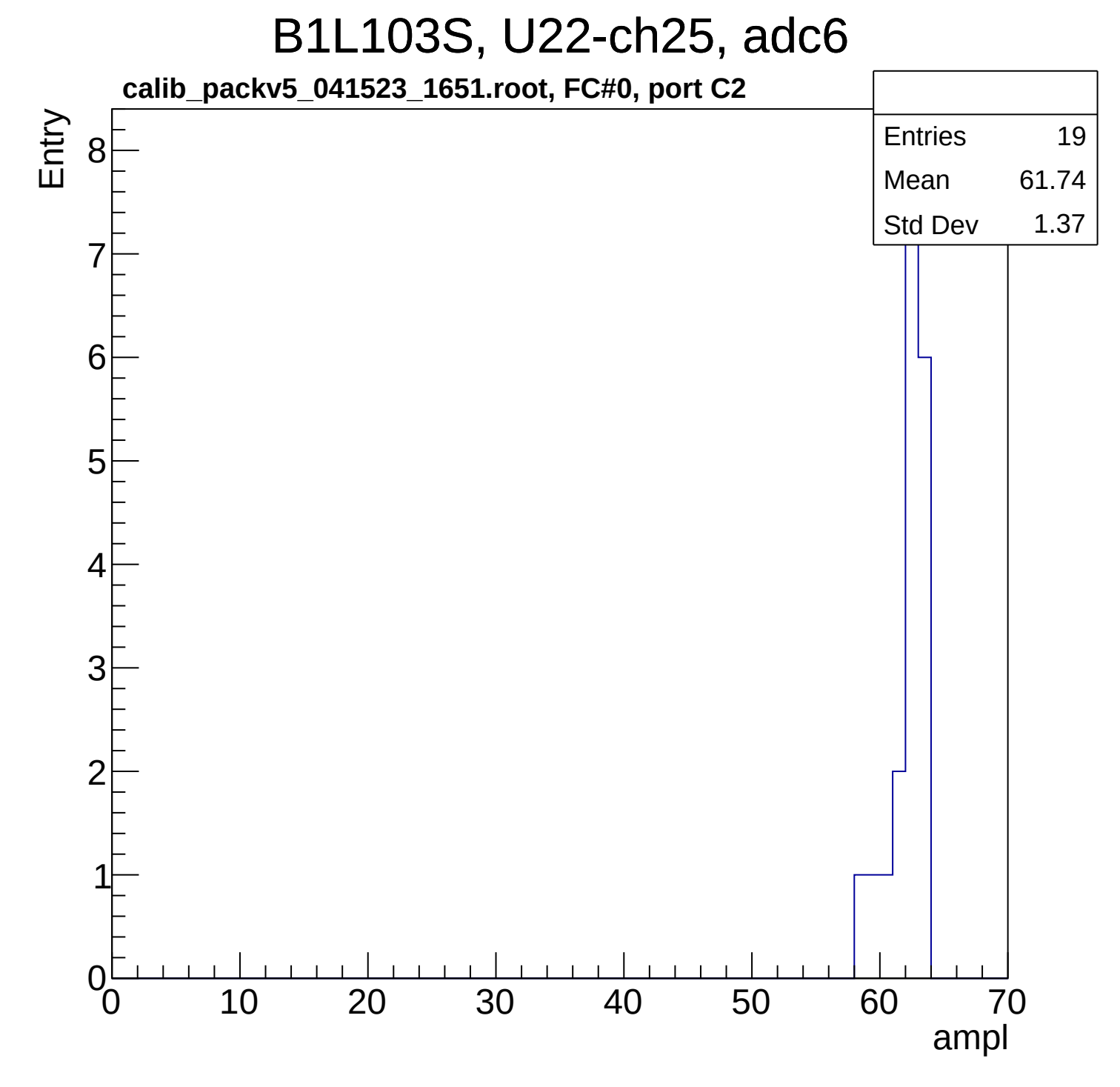
50
60
70


B1L103S, U22-ch25, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 61.74
Std Dev 1.37
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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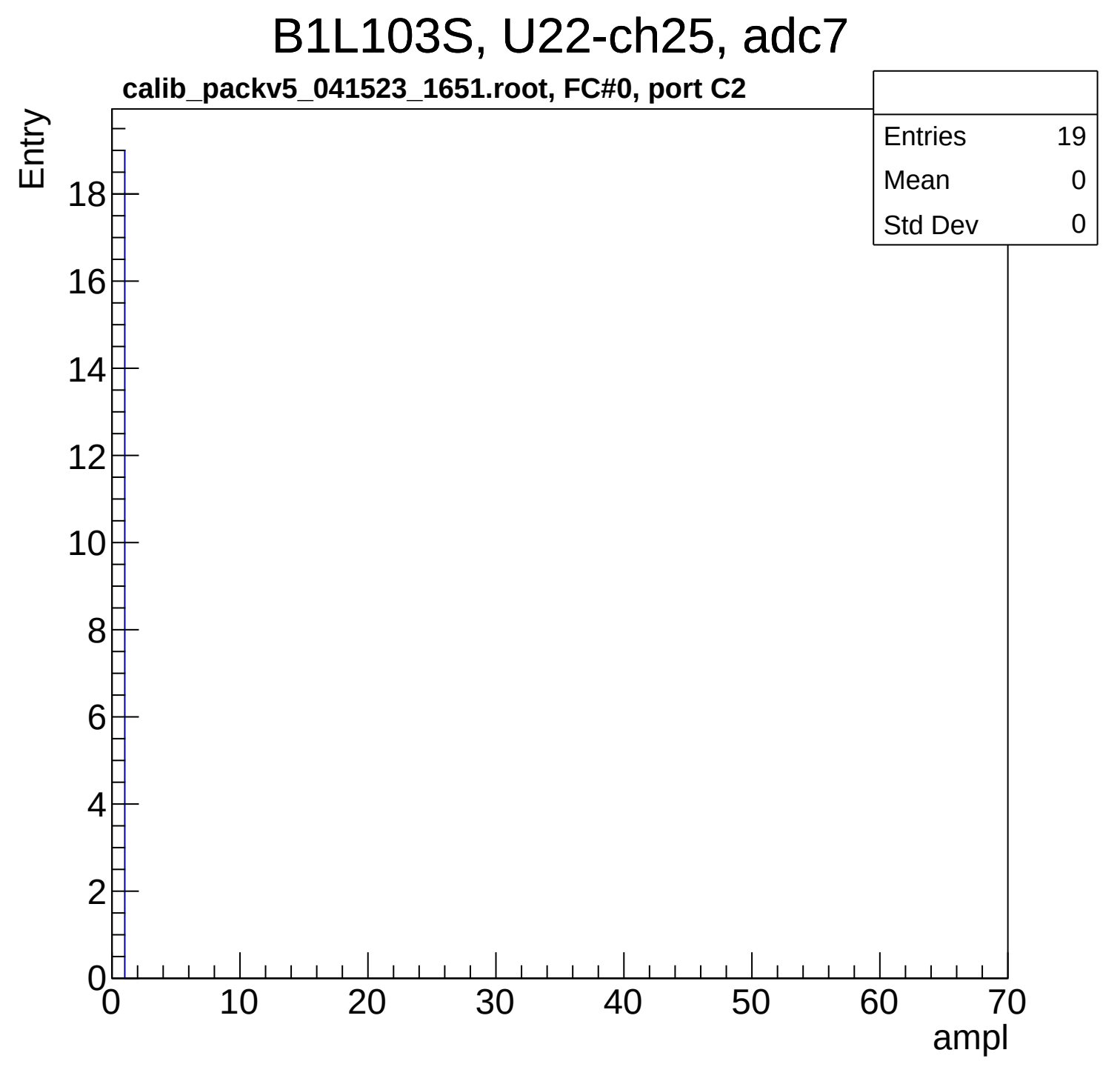
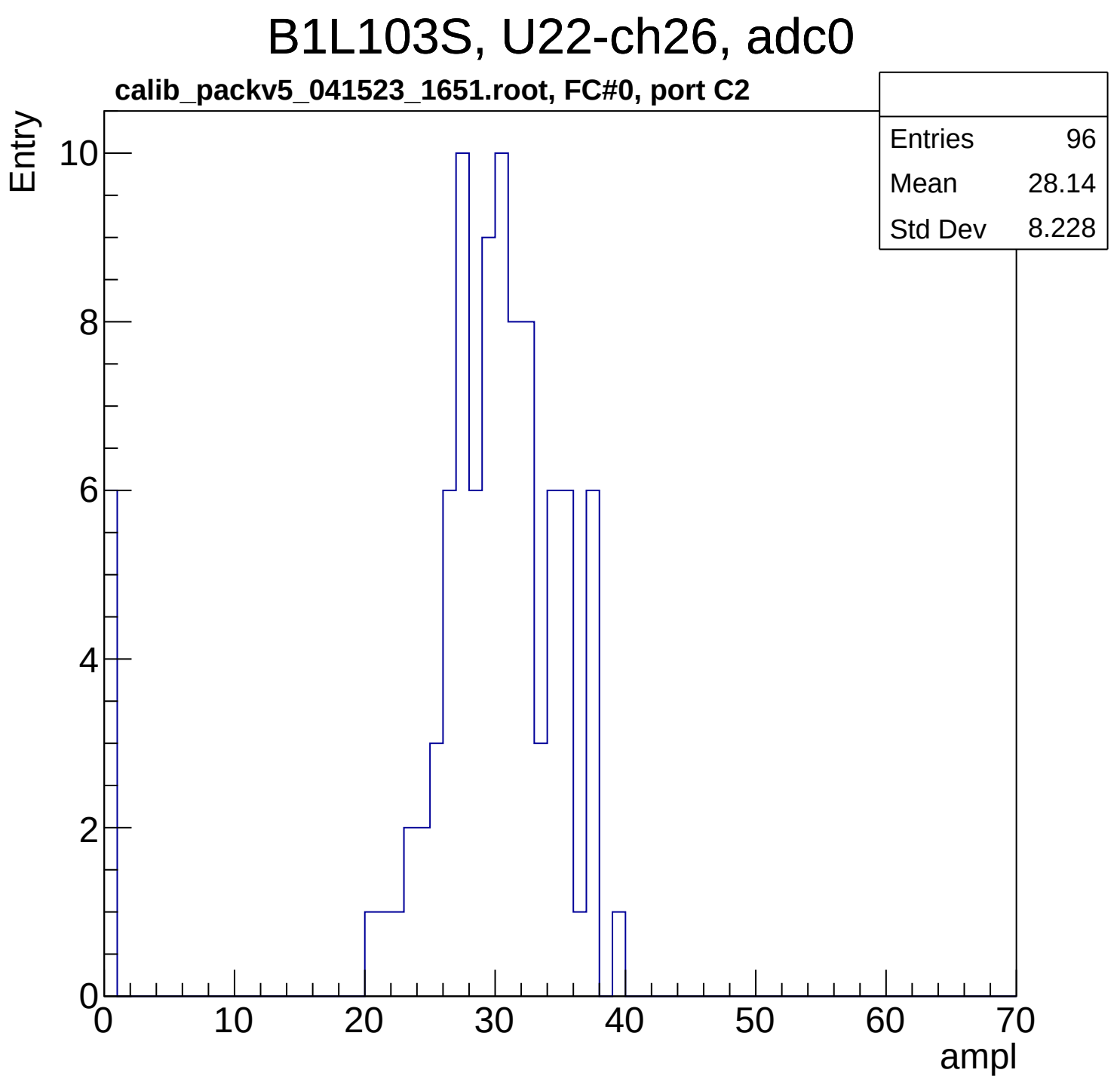

B1L103S, U22-ch25, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch26, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 96
Mean 28.14
Std Dev 8.228
Entry
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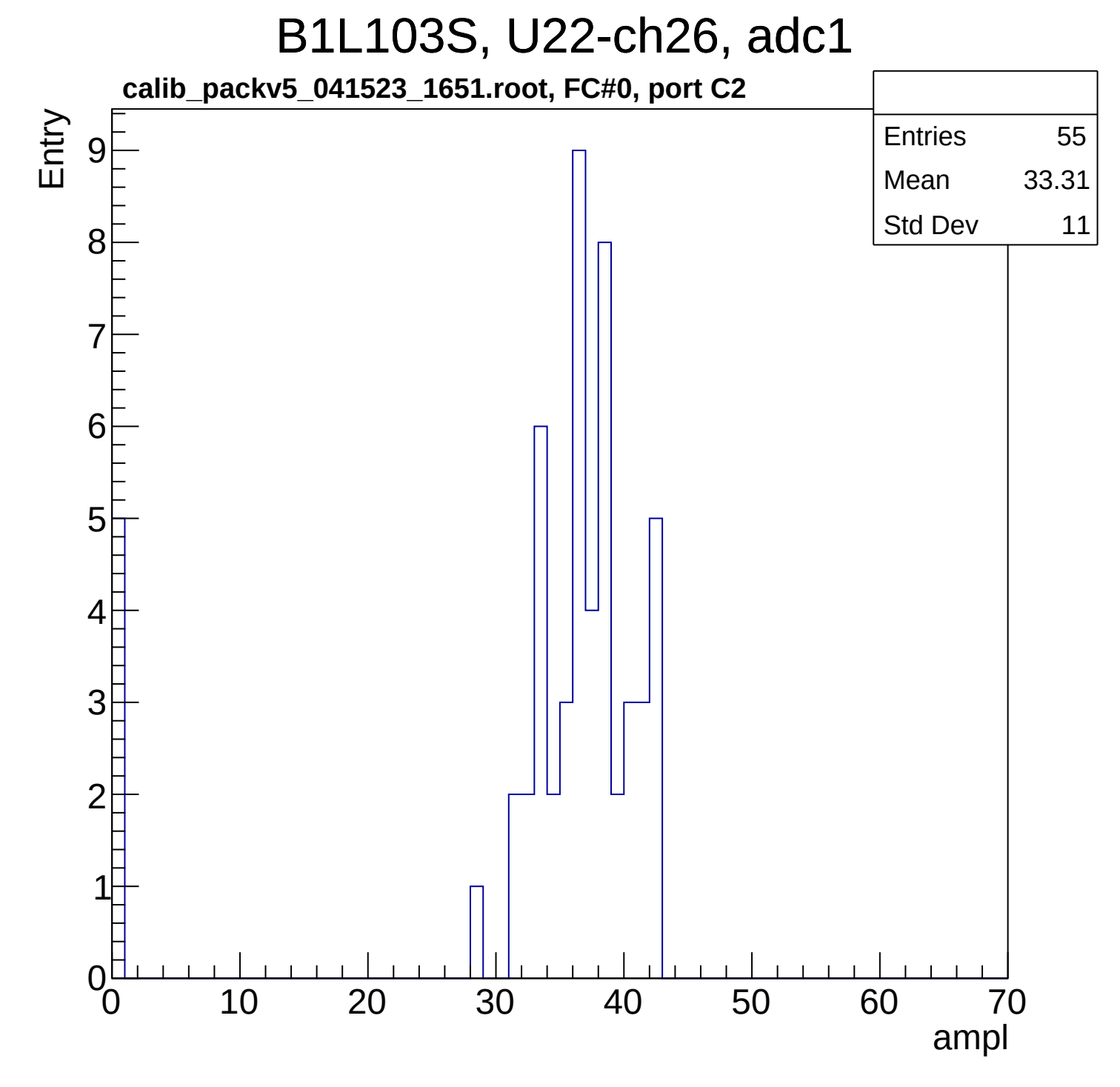
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch26, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 33.31
Std Dev 11
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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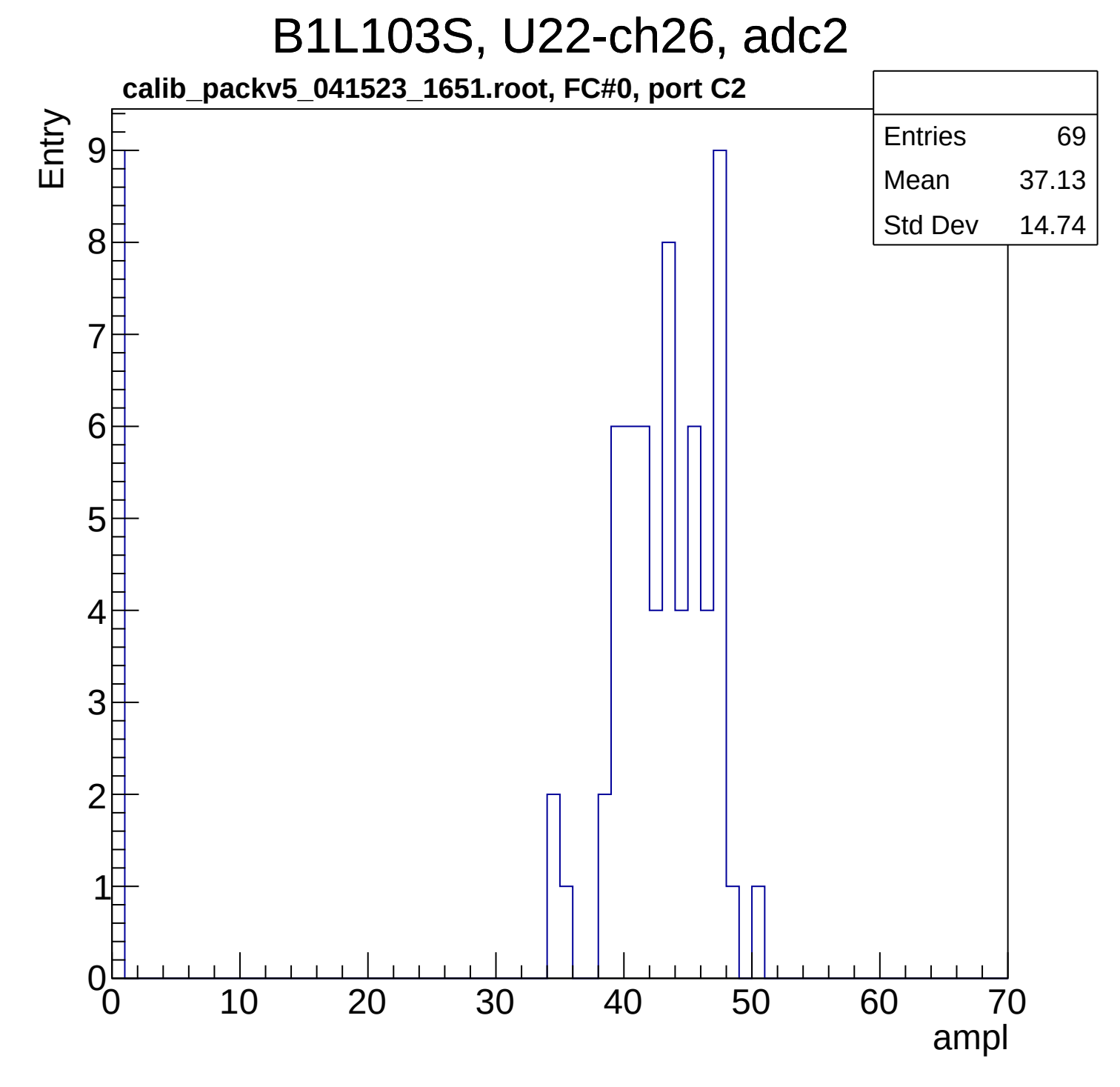
60
70


B1L103S, U22-ch26, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 37.13
Std Dev 14.74
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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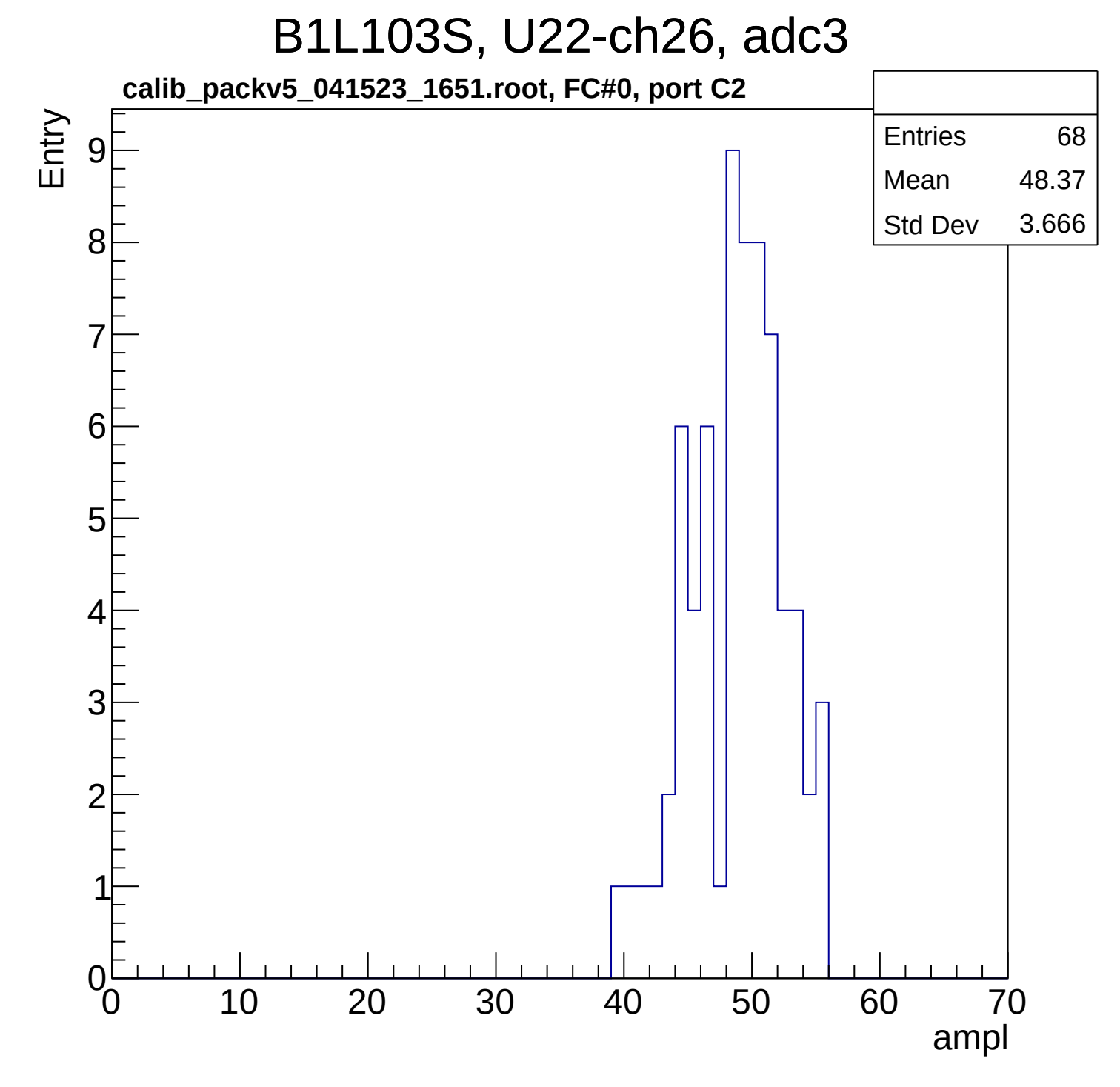
40
50
60
70


B1L103S, U22-ch26, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 48.37
Std Dev 3.666
Entry
ampl
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3
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5
6
7
8
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0
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60
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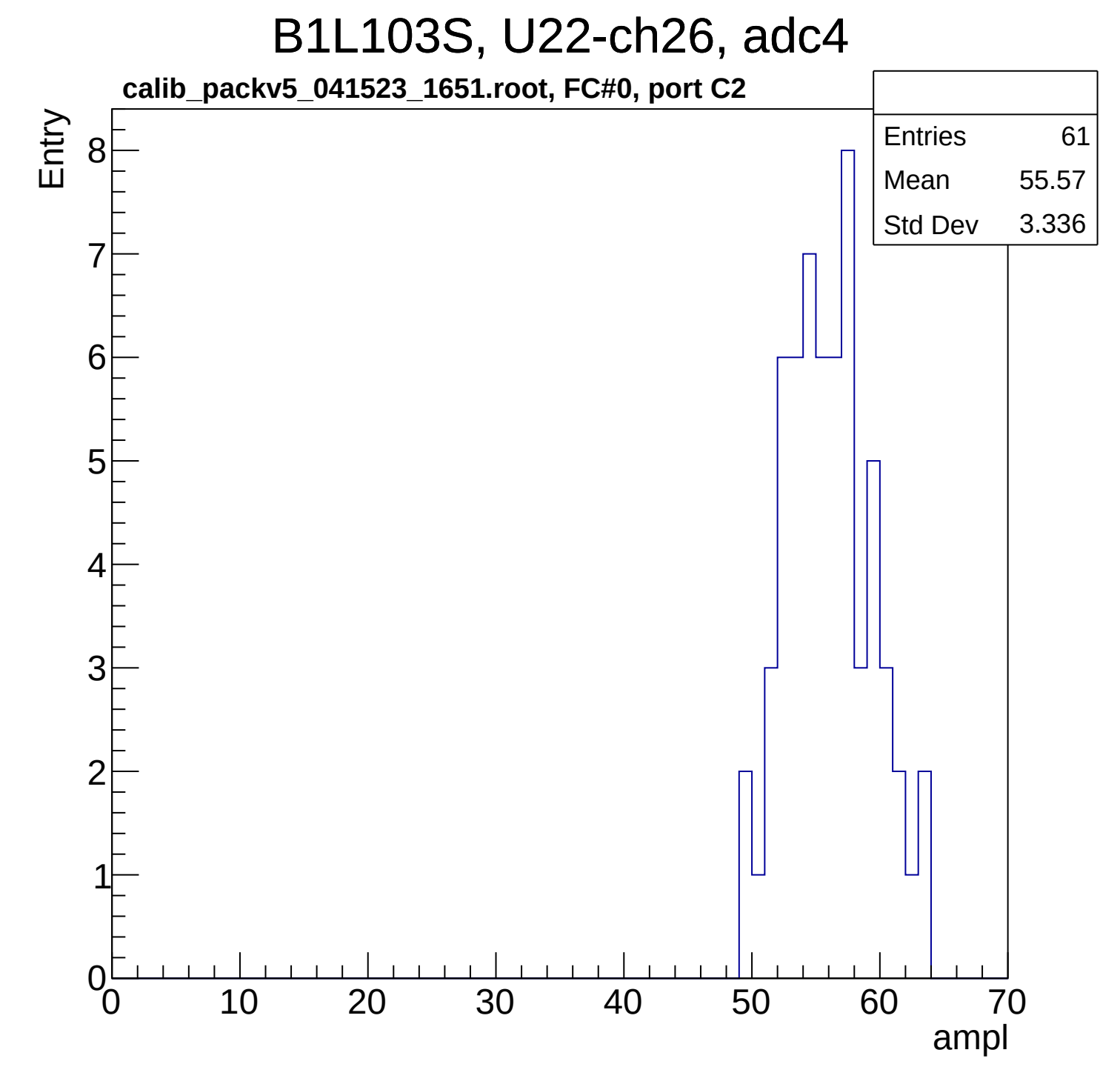
B1L103S, U22-ch26, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 55.57
Std Dev 3.336
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
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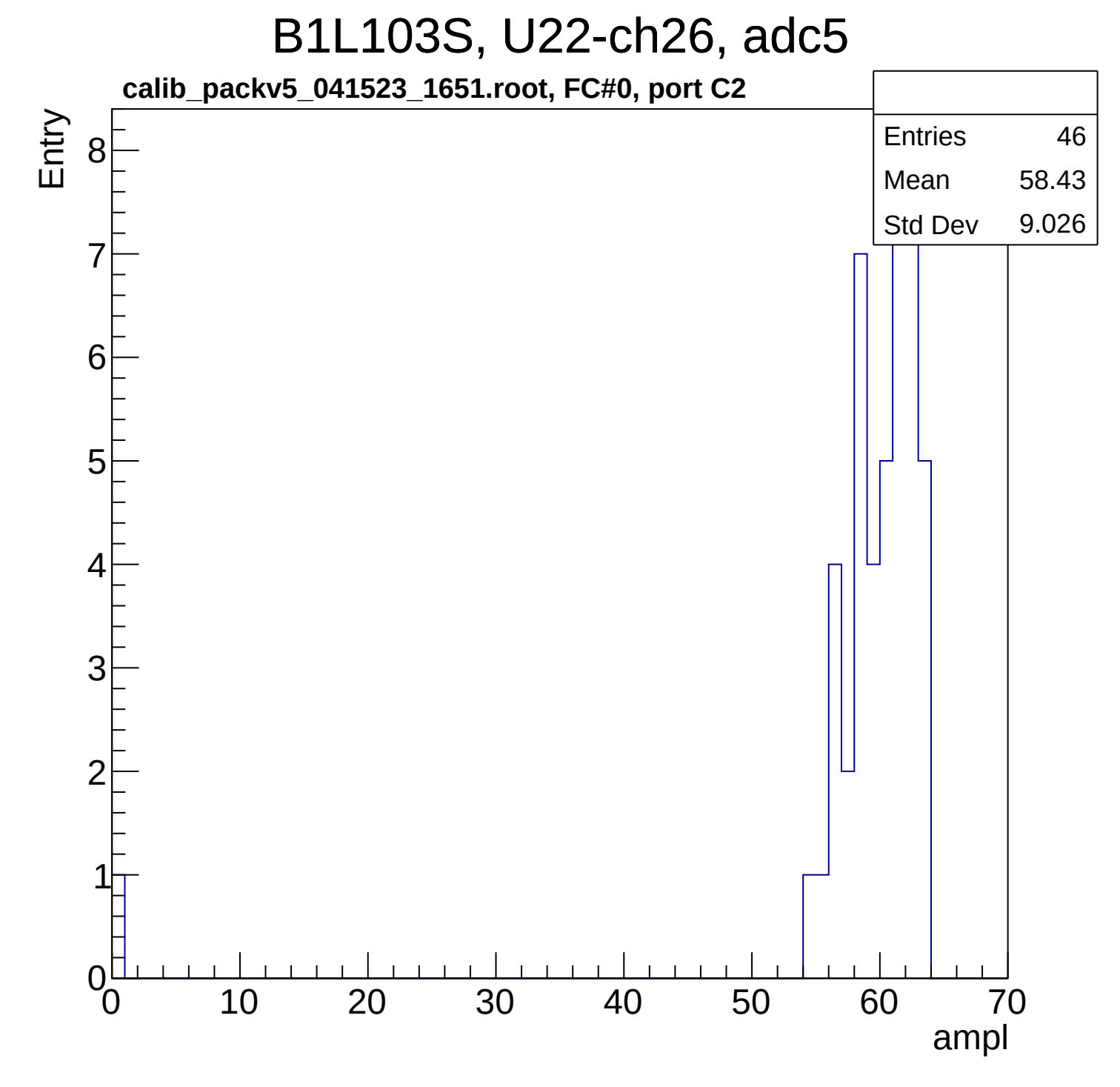
60
70


B1L103S, U22-ch26, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 58.43
Std Dev 9.026
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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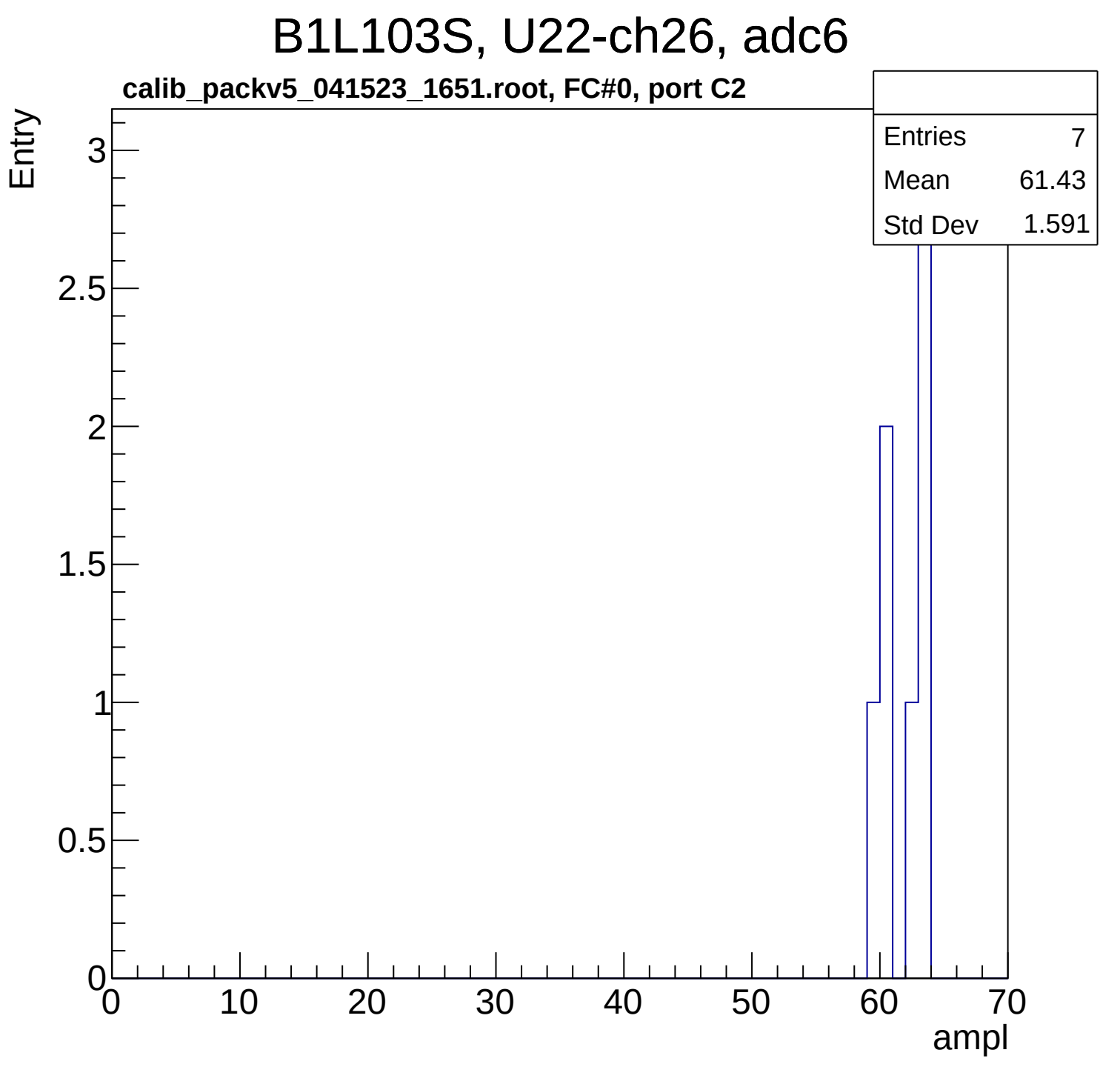
40
50
60
70


B1L103S, U22-ch26, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 61.43
Std Dev 1.591
Entry
ampl
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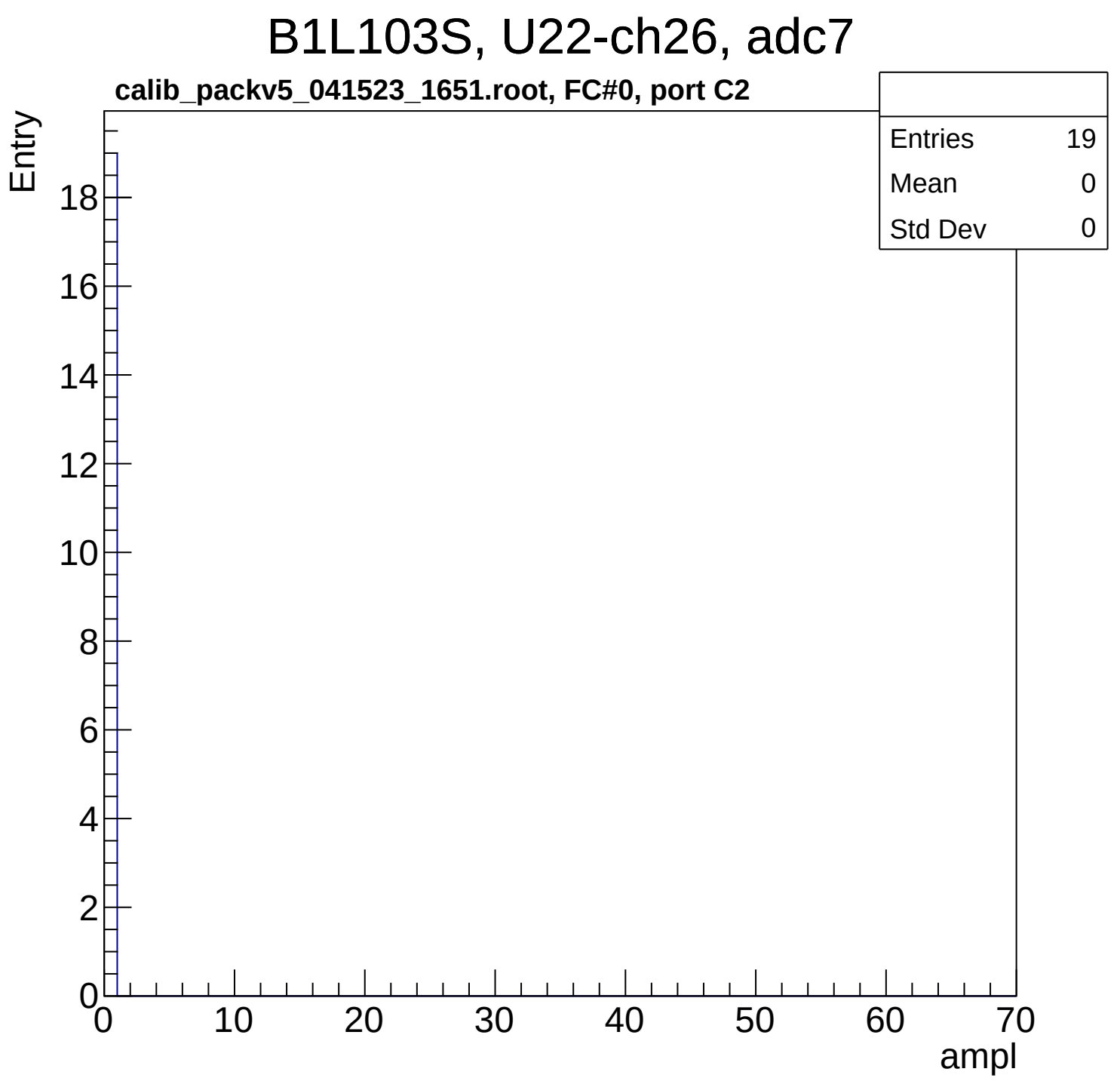
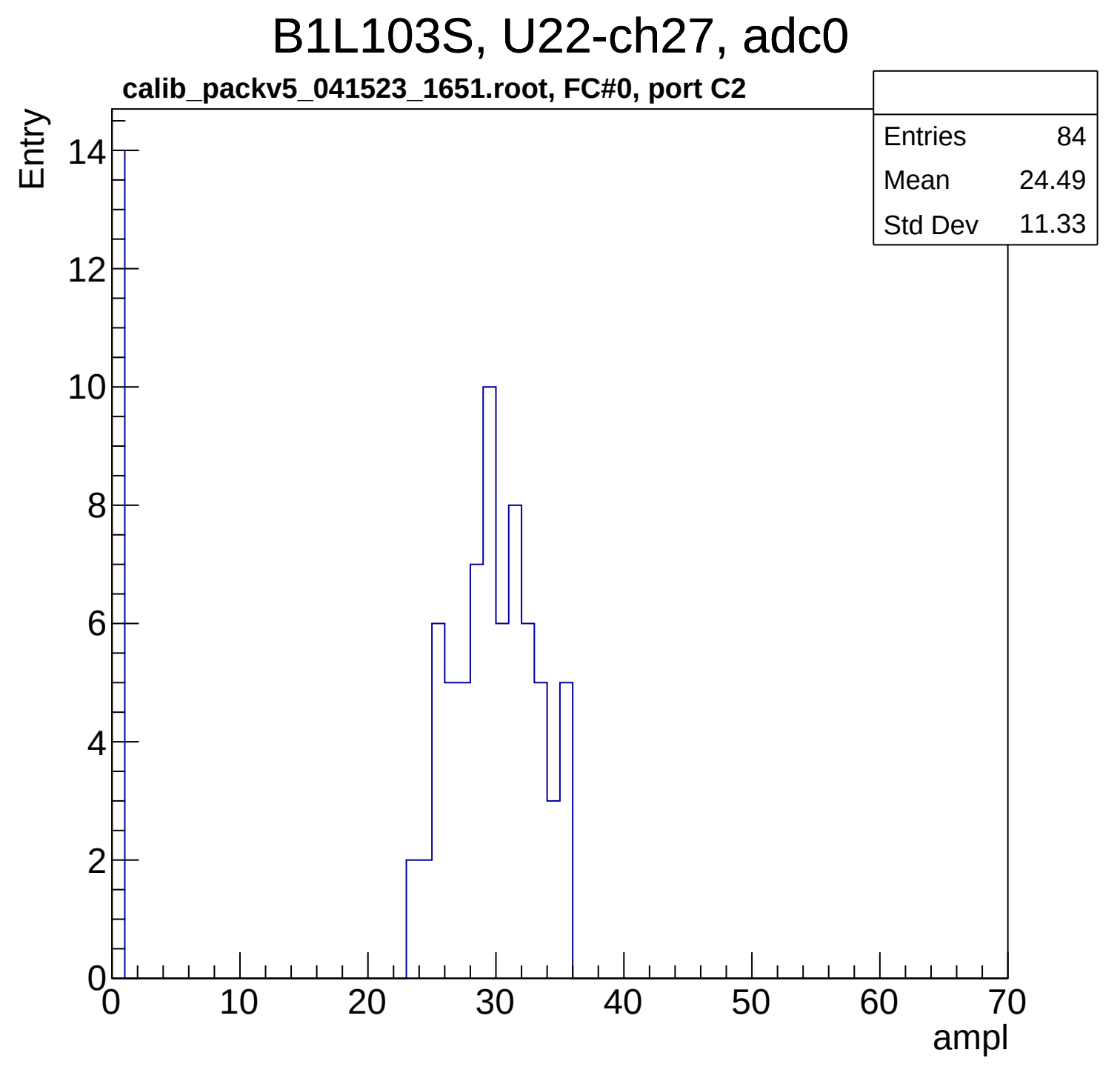
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U22-ch26, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch27, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 24.49
Std Dev 11.33
Entry
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6
8
10
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14
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10
20
30
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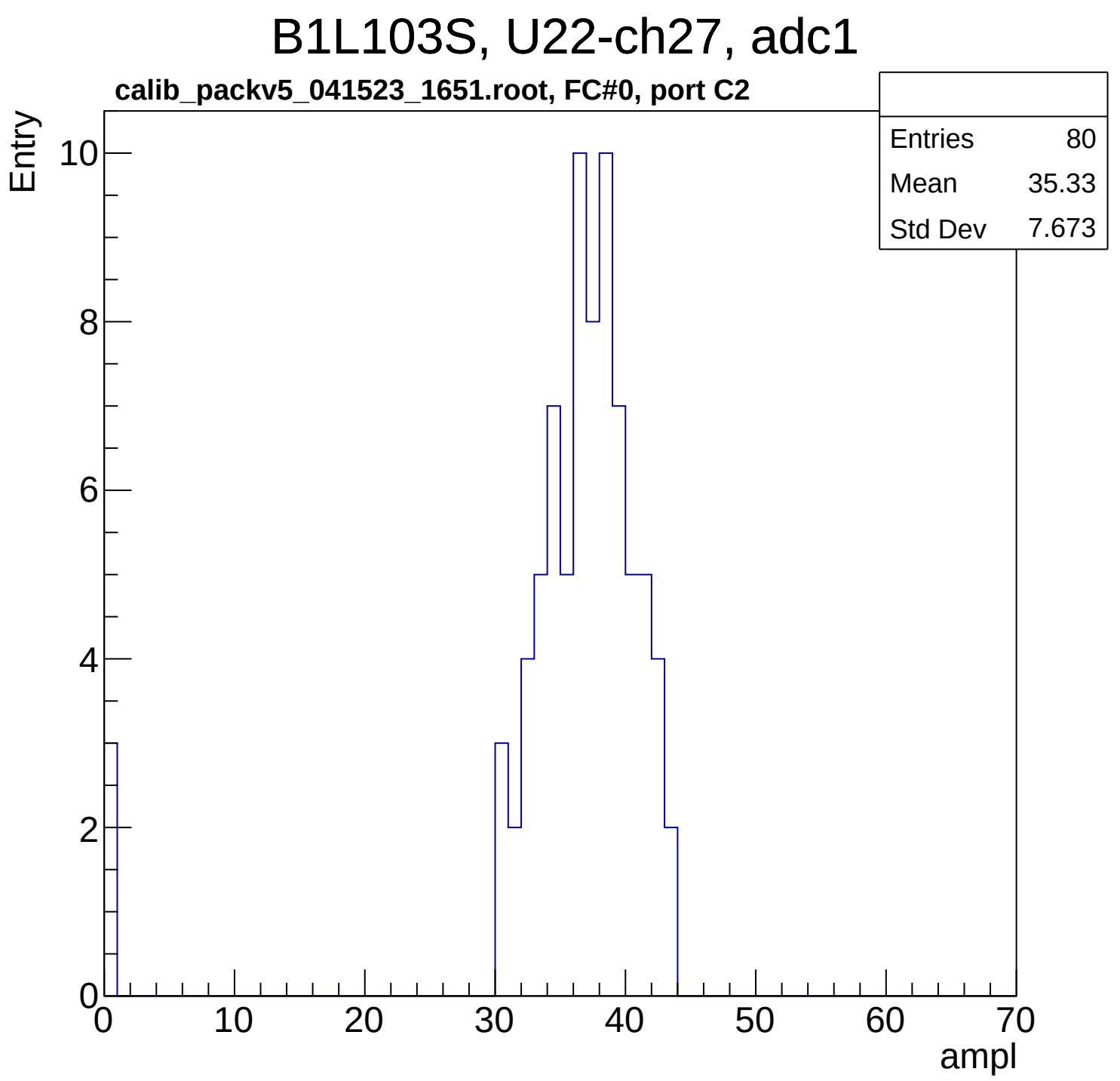
50
60
70
ampl


B1L103S, U22-ch27, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 35.33
Std Dev 7.673
Entry
ampl
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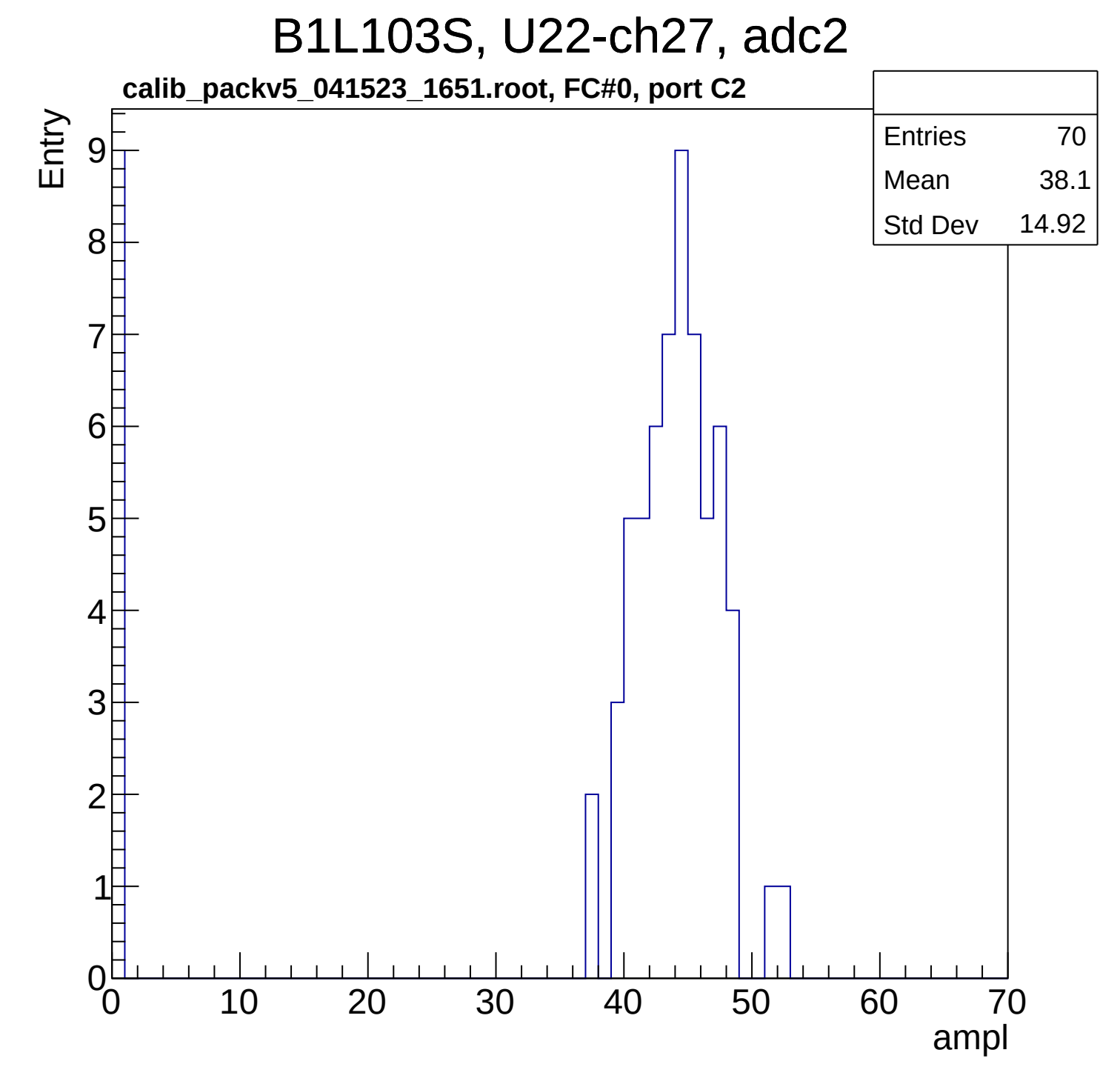
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U22-ch27, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 38.1
Std Dev 14.92
Entry
ampl
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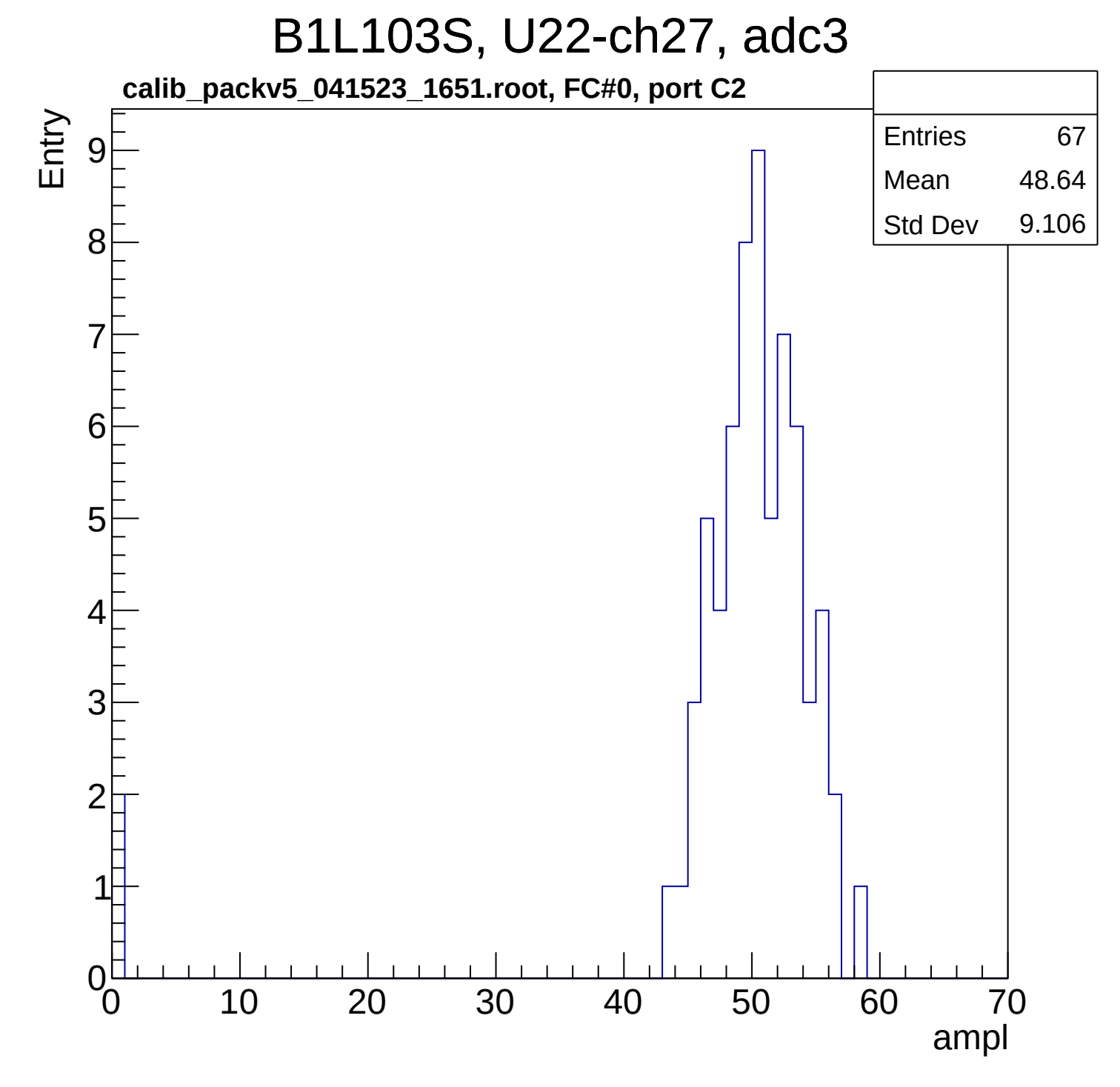
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch27, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 48.64
Std Dev 9.106
Entry
ampl
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3
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5
6
7
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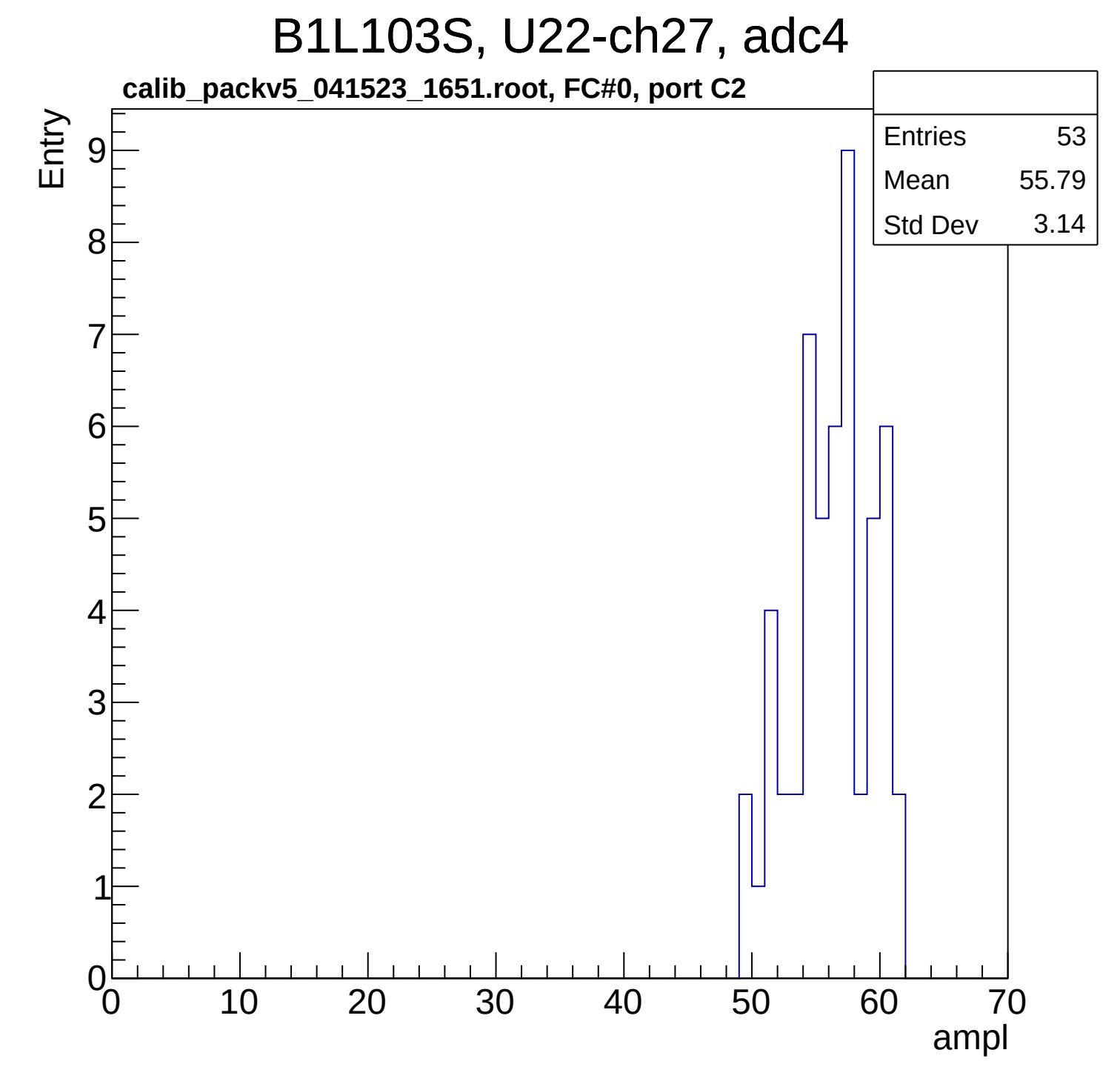
B1L103S, U22-ch27, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 55.79
Std Dev 3.14
Entry
ampl
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5
6
7
8
9
0
10
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30
40
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60
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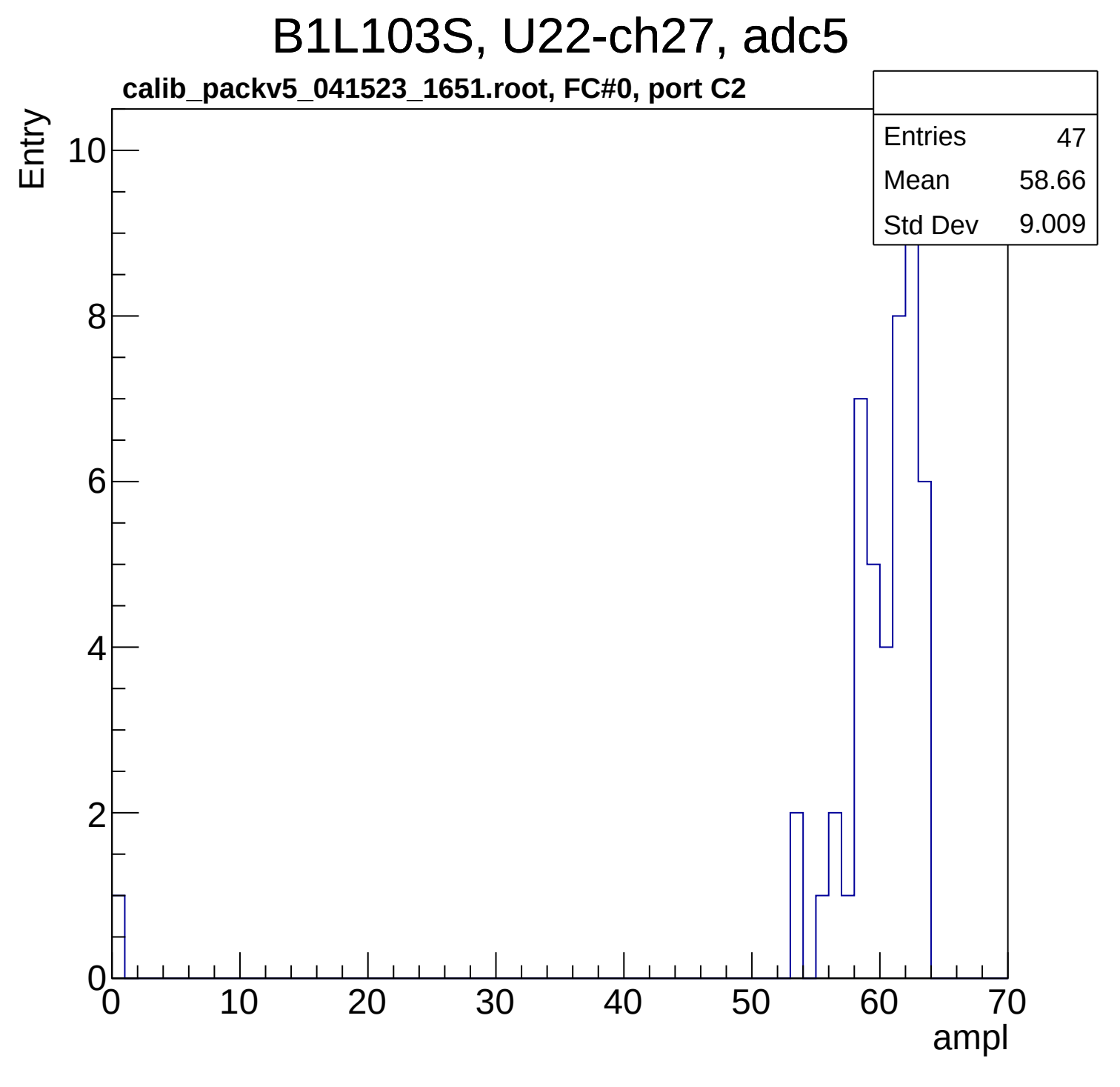
B1L103S, U22-ch27, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 58.66
Std Dev 9.009
Entry
ampl
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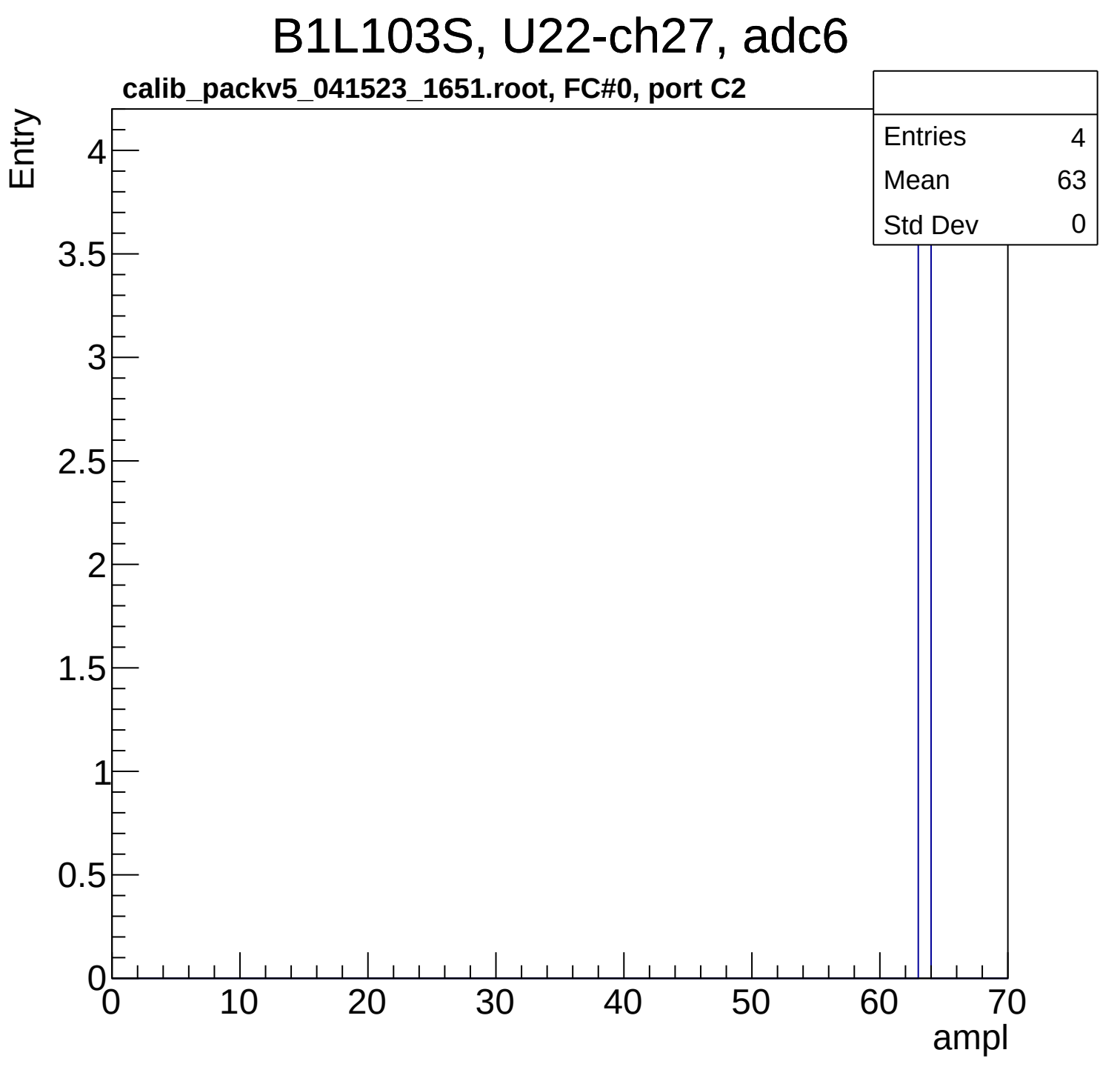
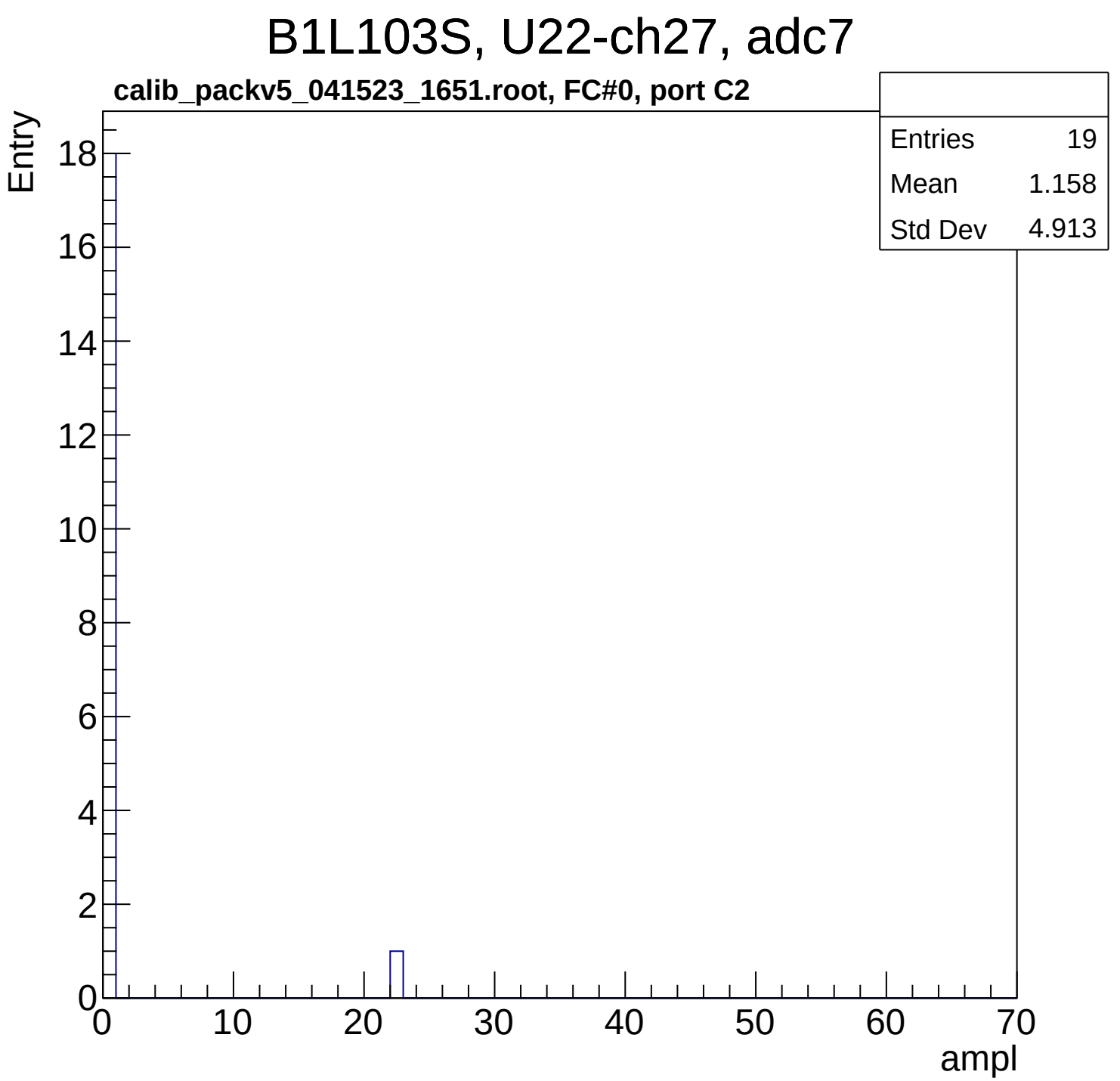
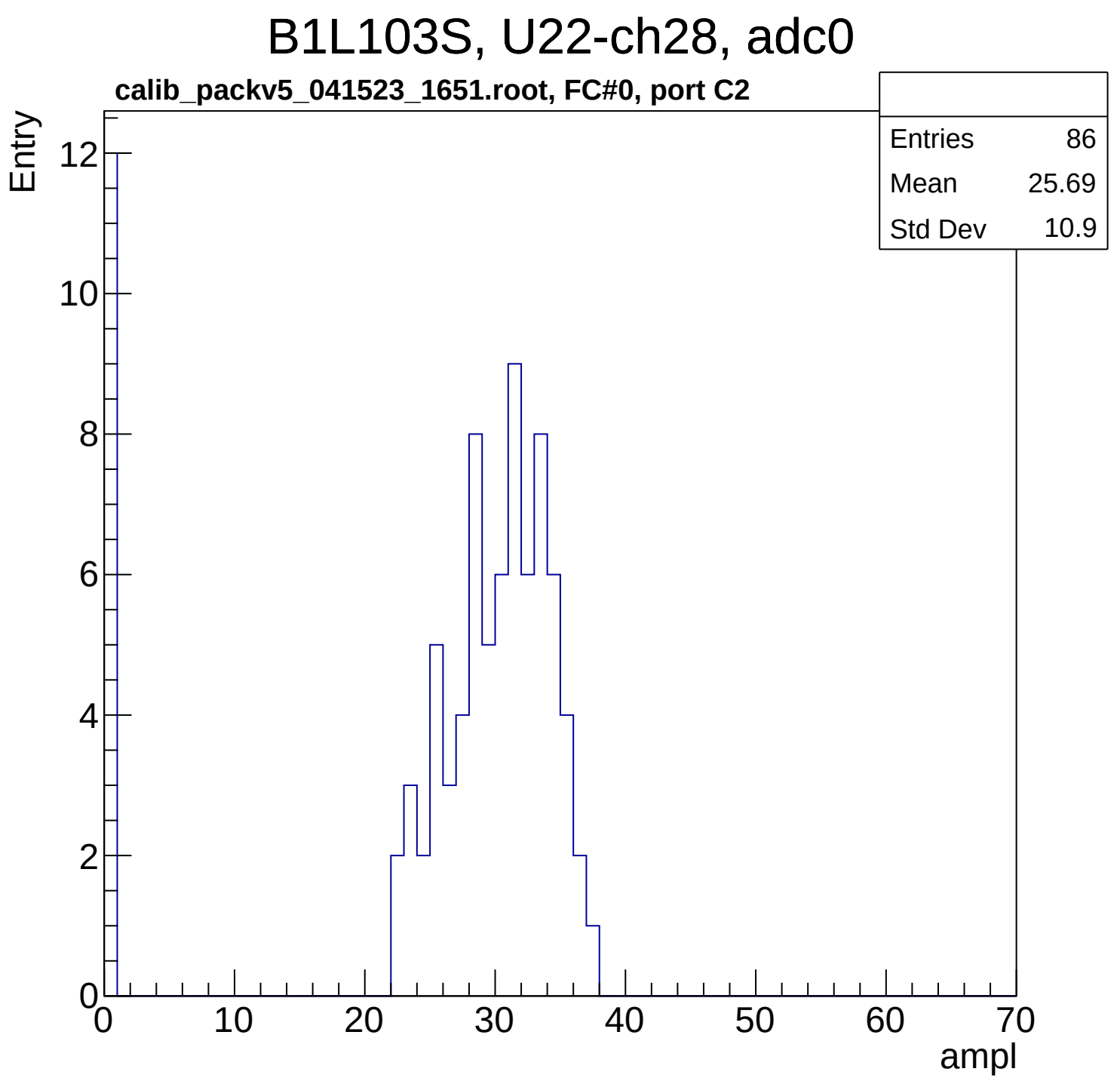
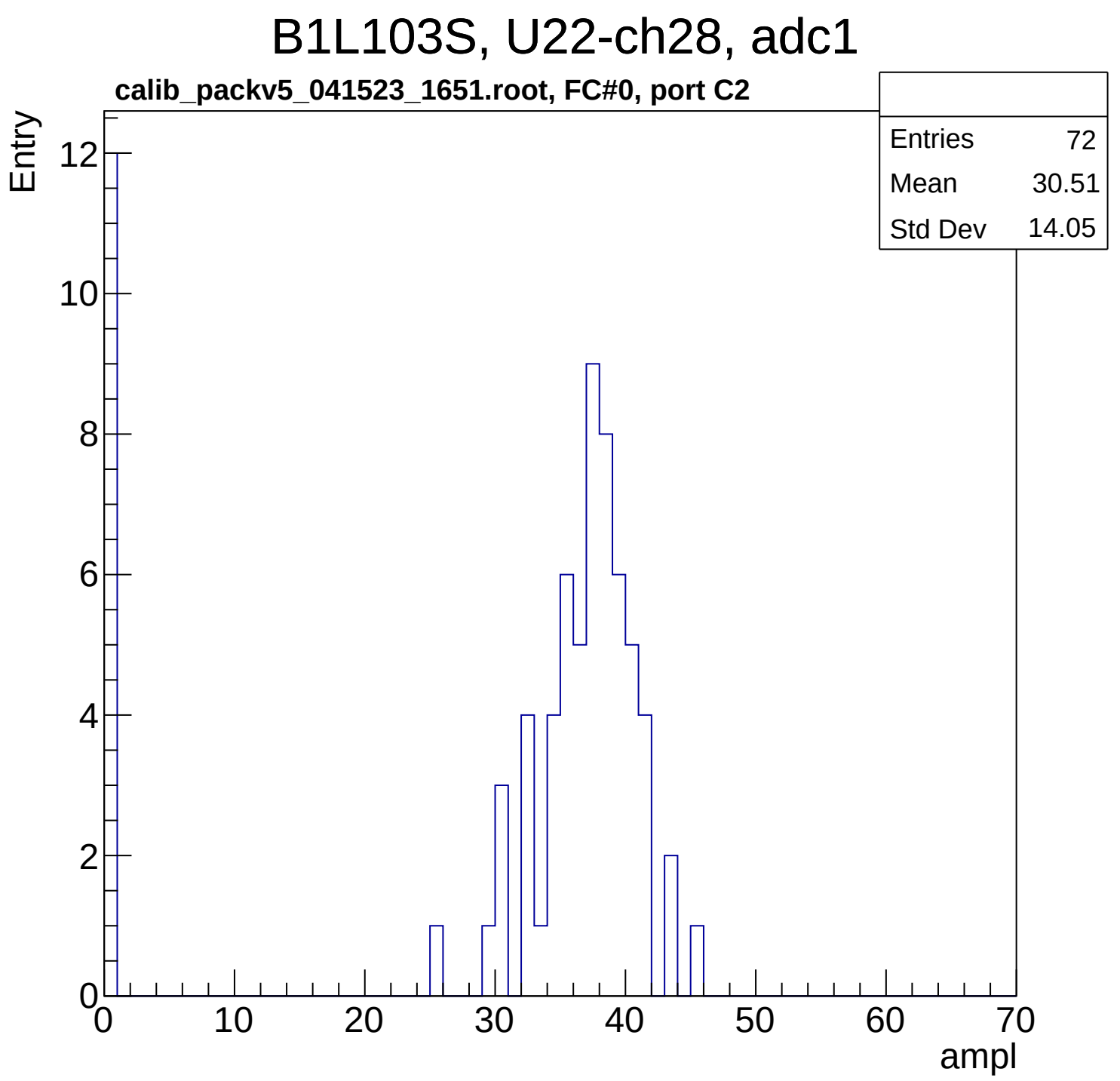
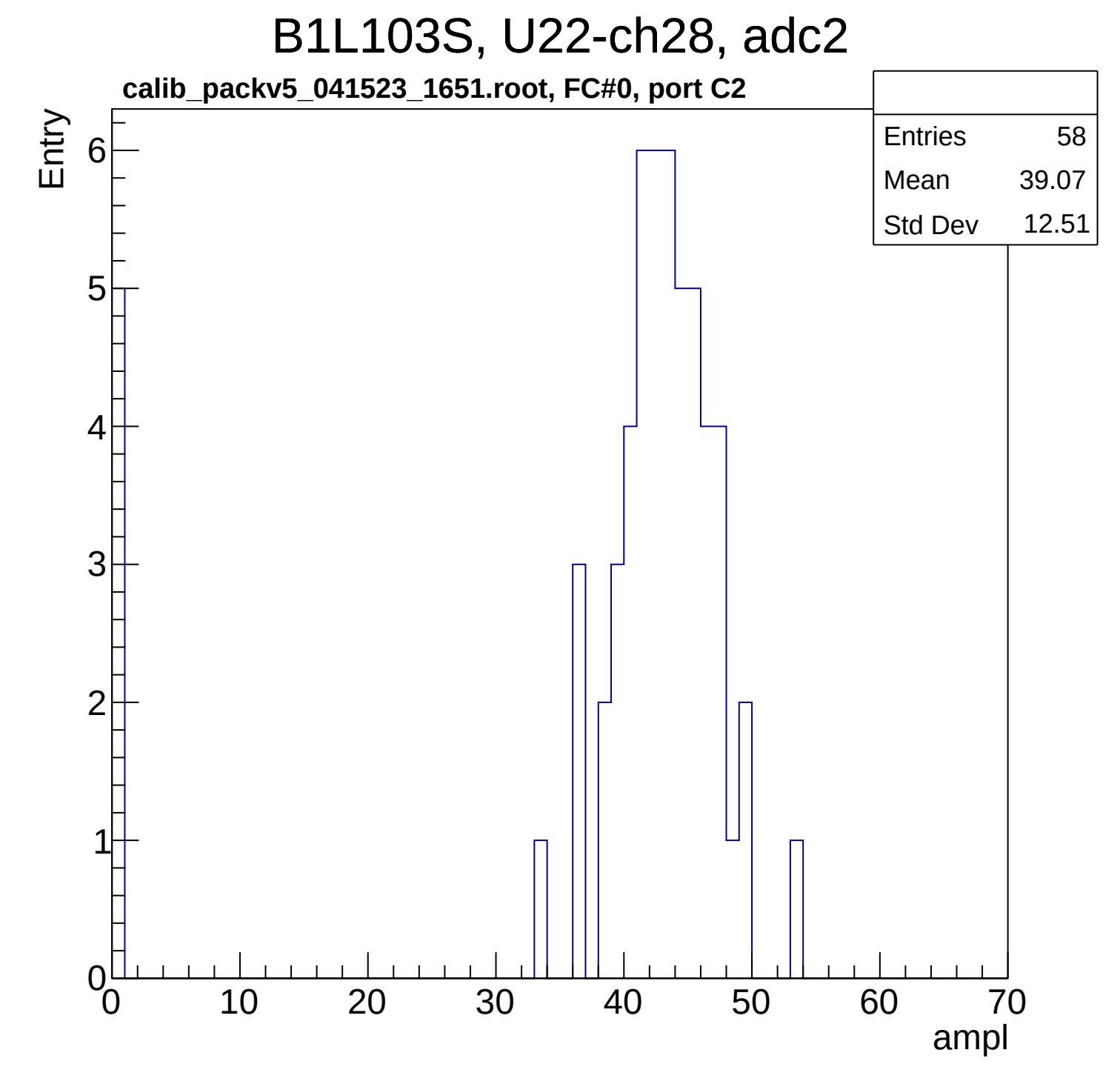
4
6
8
10
0
10
20
30
40
50
60
70

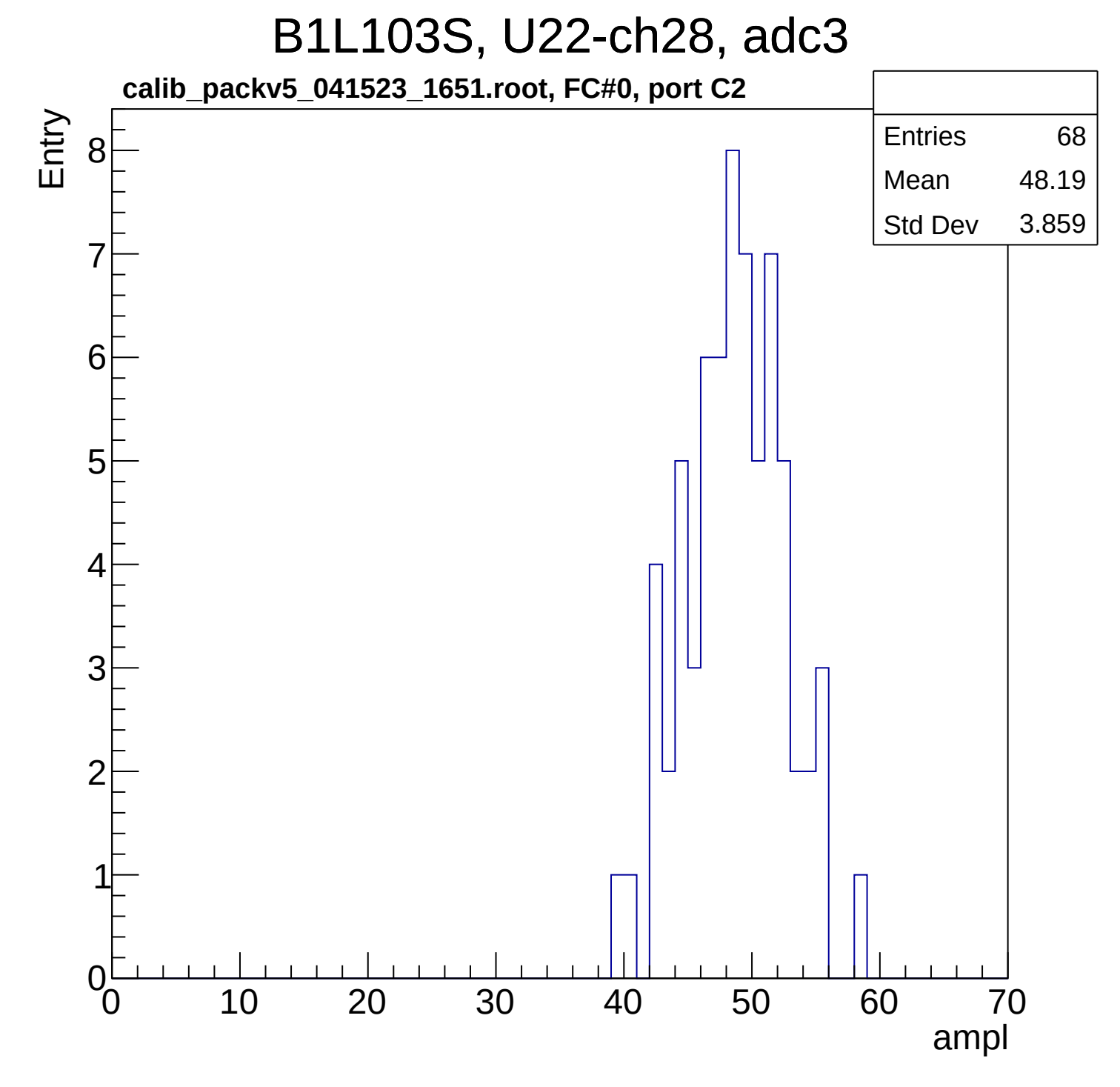

B1L103S, U22-ch27, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 63
Std Dev 0
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U22-ch27, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.158
Std Dev 4.913
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch28, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 25.69
Std Dev 10.9
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch28, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 30.51
Std Dev 14.05
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch28, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 39.07
Std Dev 12.51
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch28, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 48.19
Std Dev 3.859
Entry
ampl
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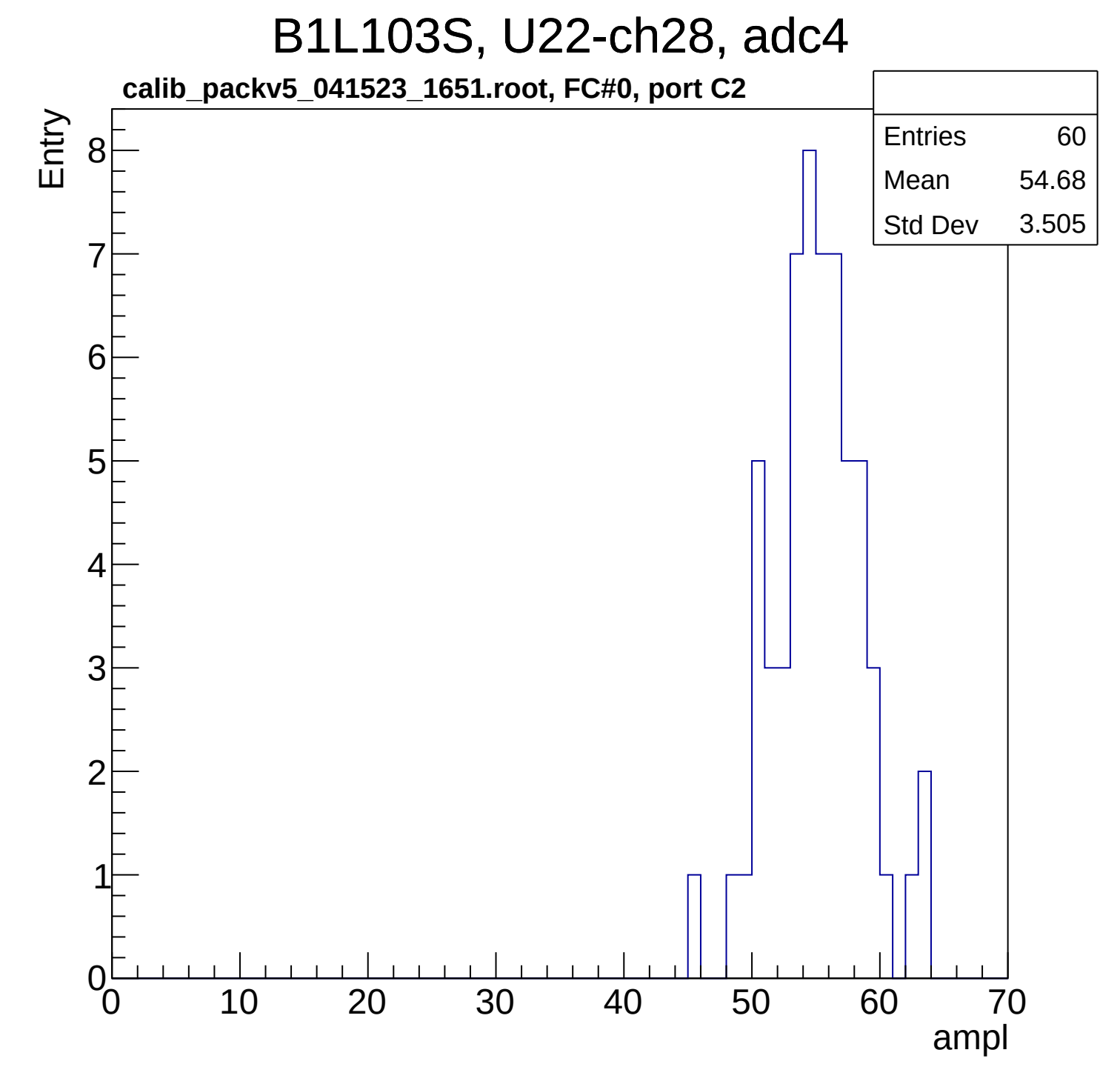
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch28, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 54.68
Std Dev 3.505
Entry
ampl
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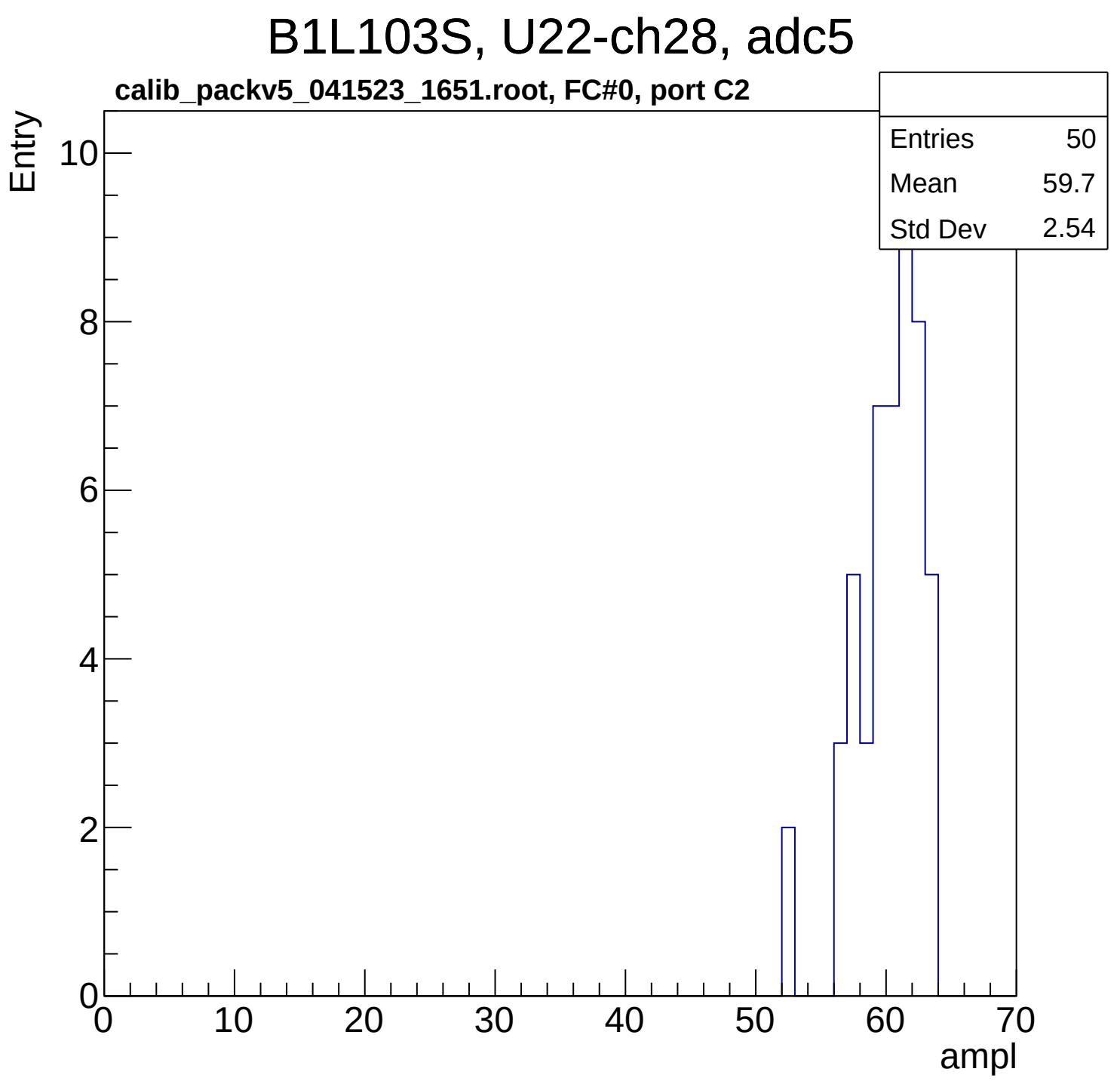
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch28, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 59.7
Std Dev 2.54
Entry
ampl
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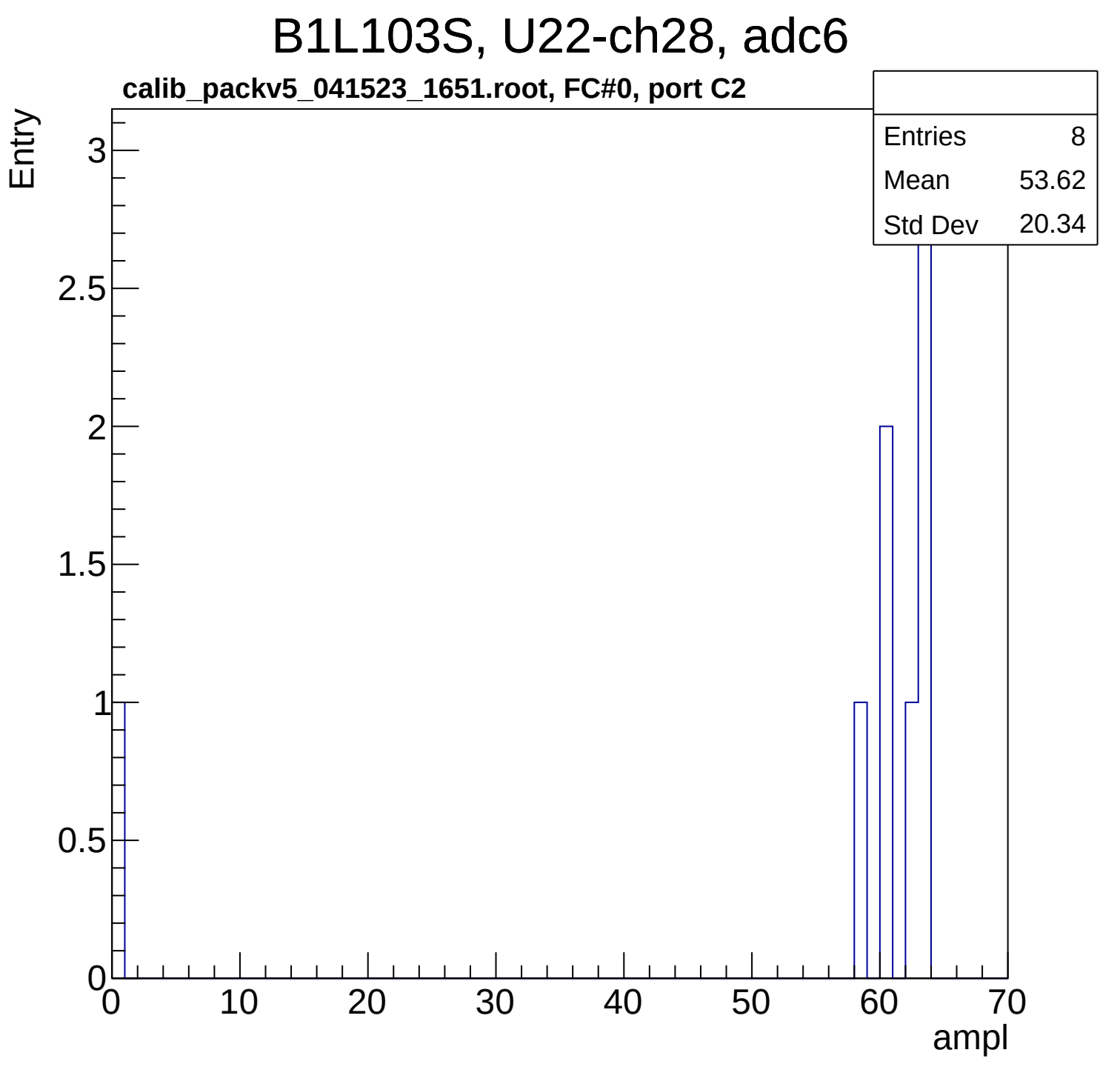
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U22-ch28, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 53.62
Std Dev 20.34
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
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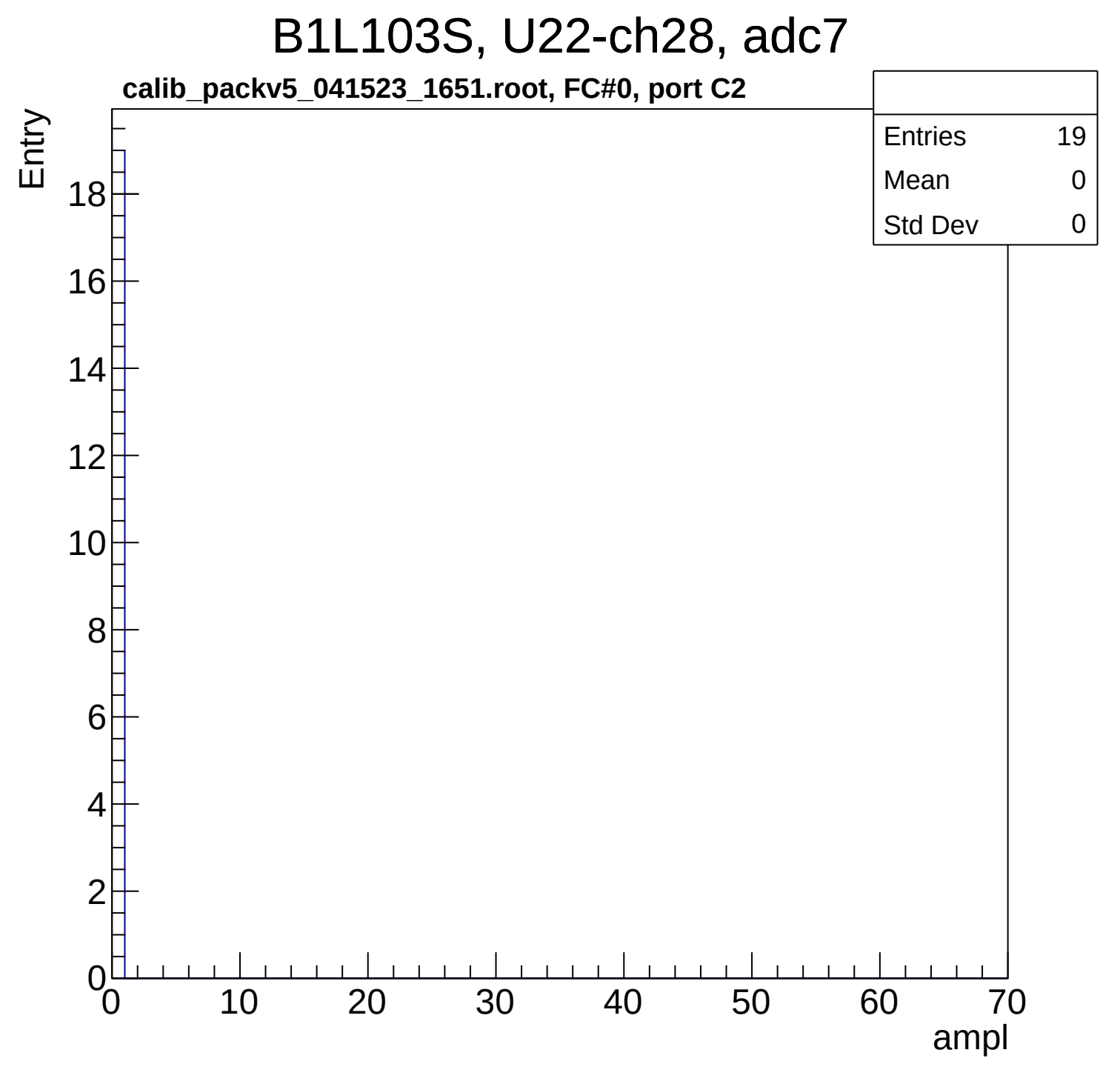
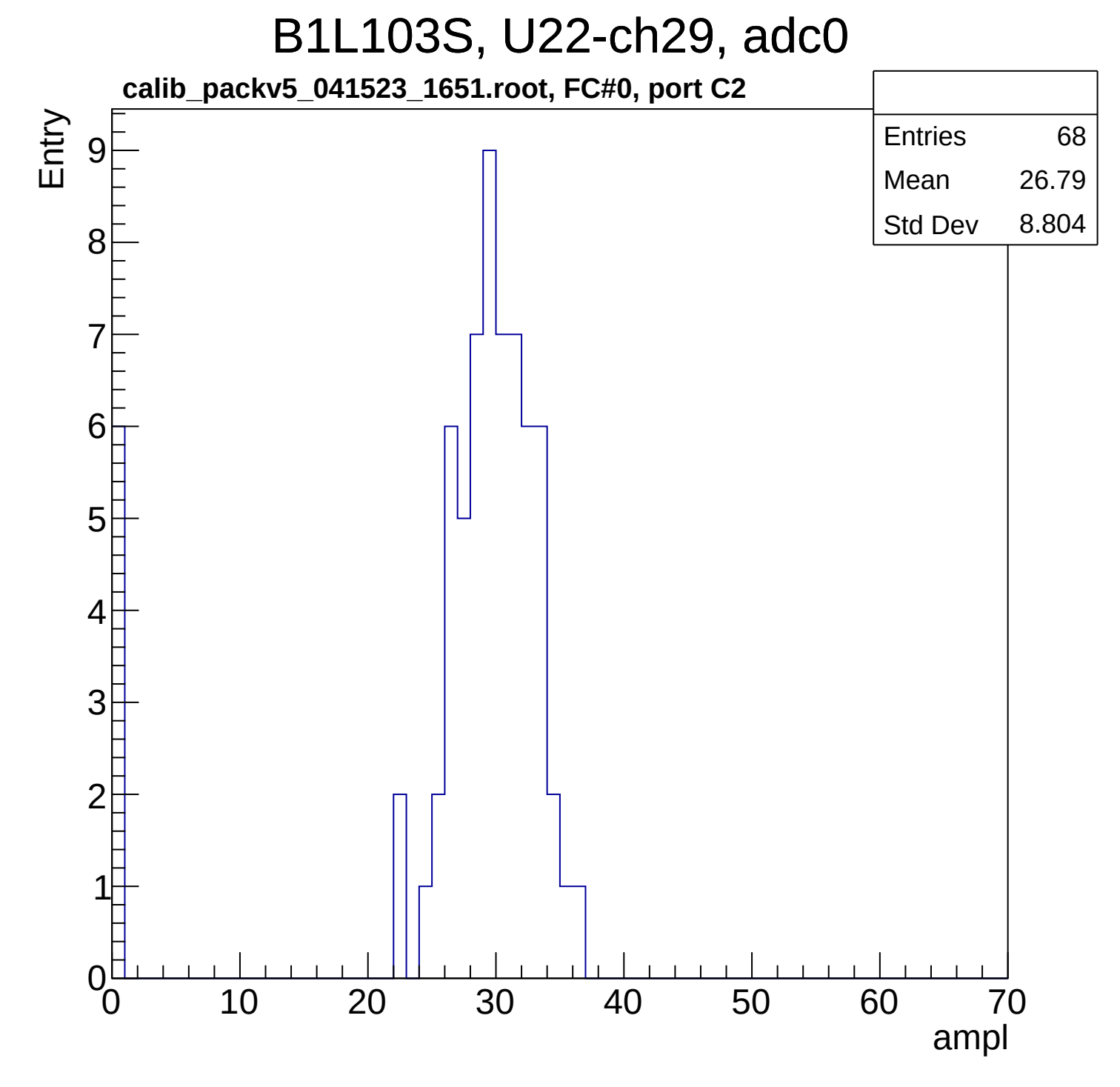

B1L103S, U22-ch28, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch29, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 26.79
Std Dev 8.804
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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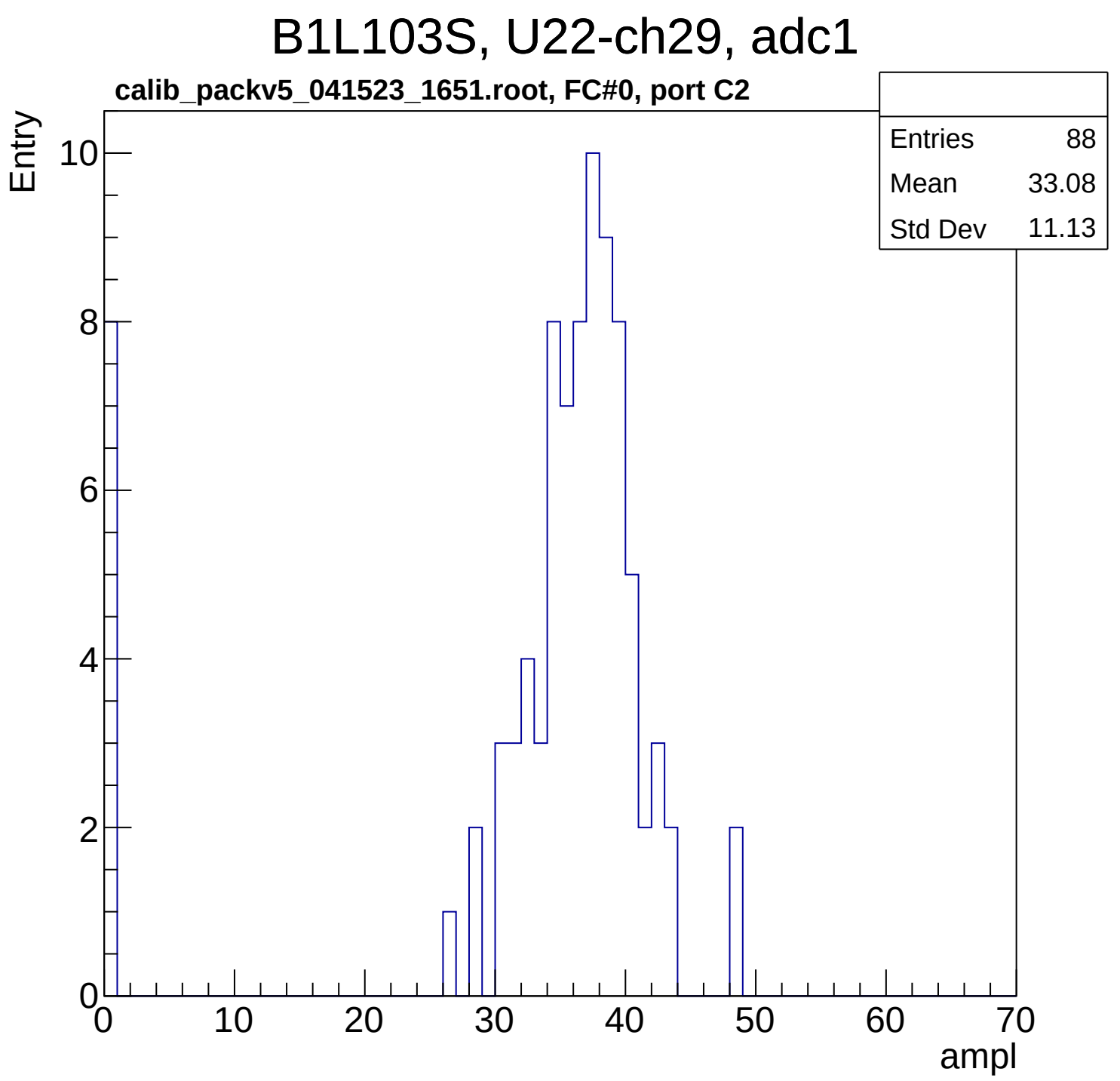
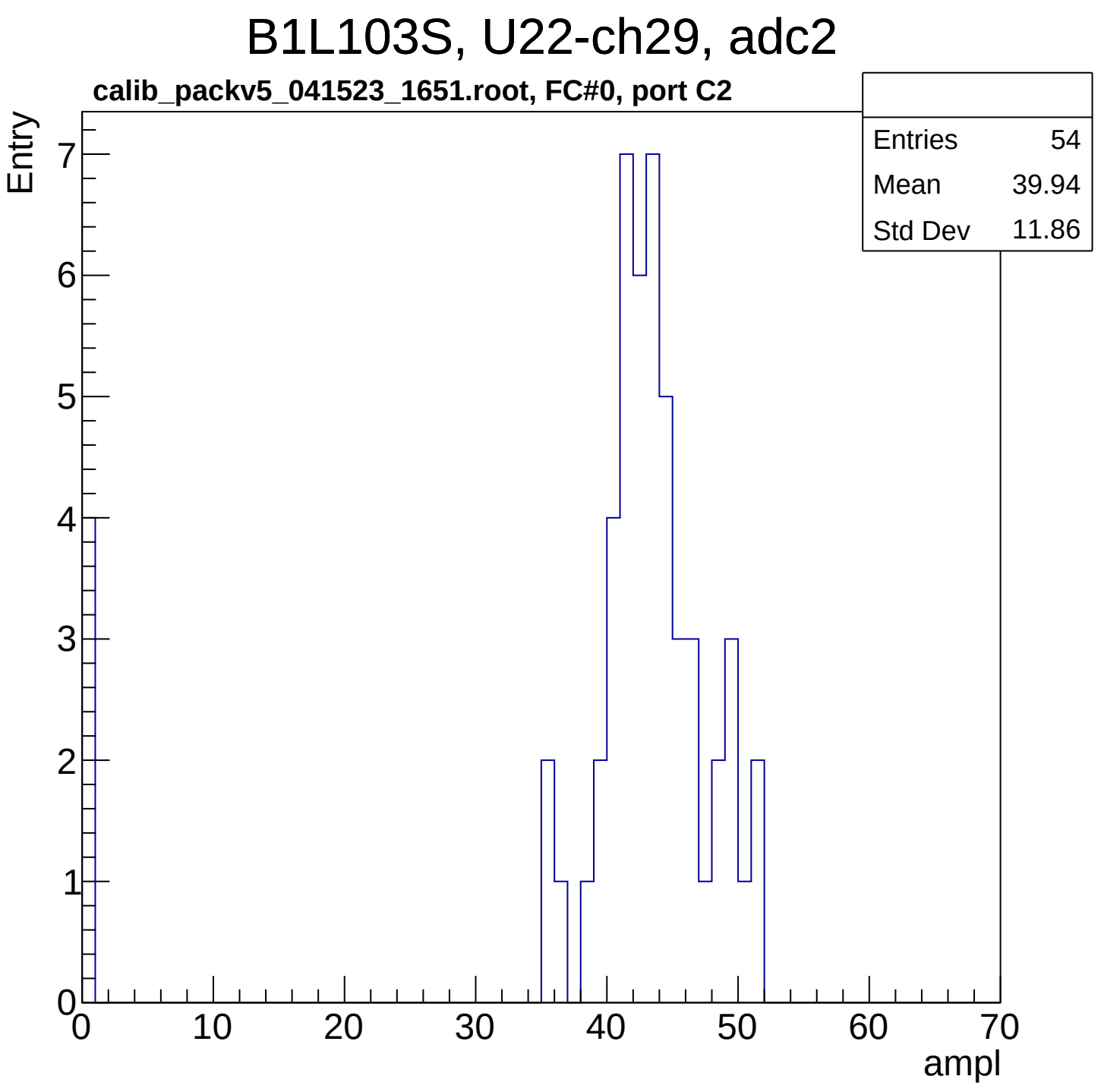
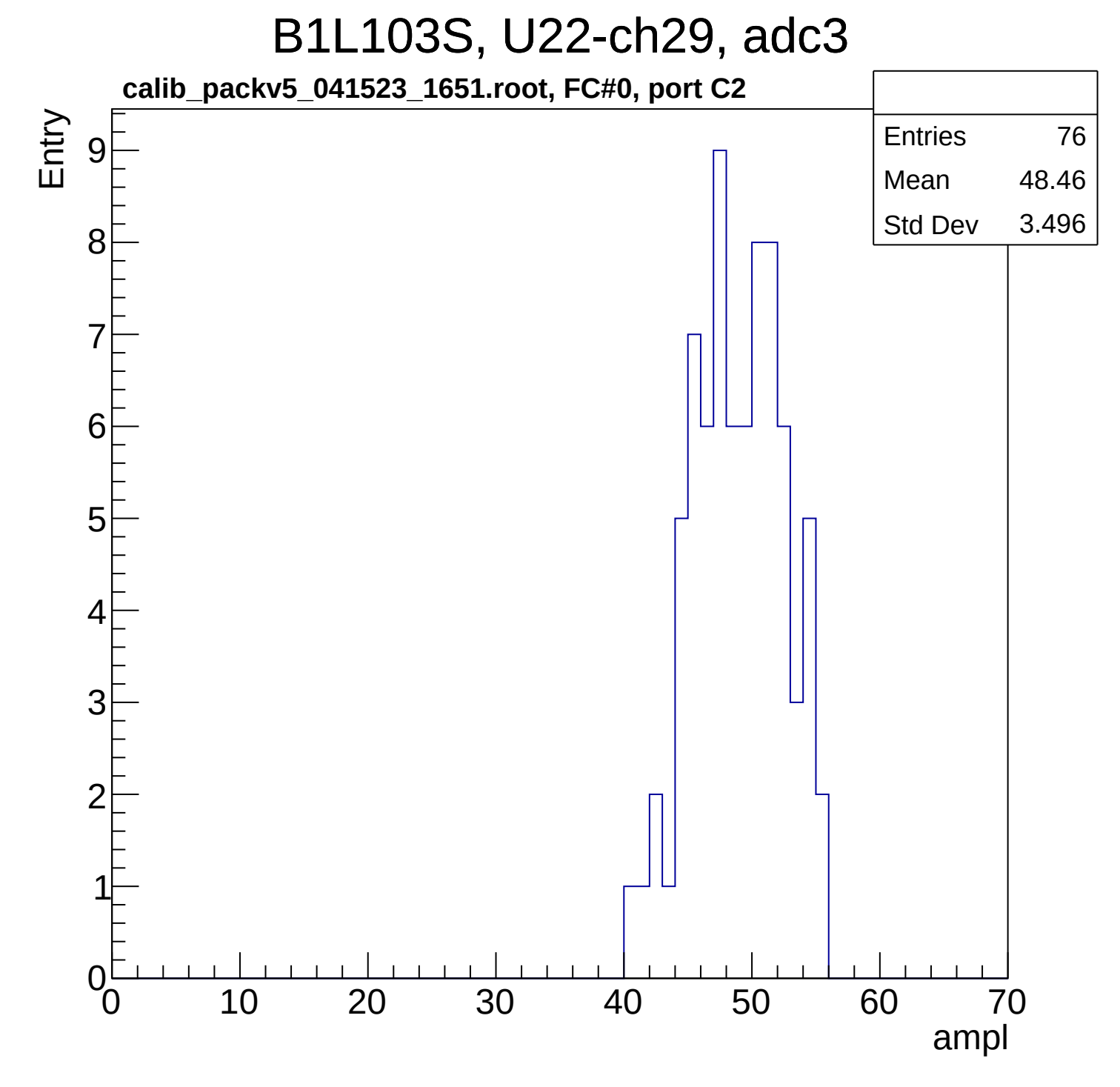

B1L103S, U22-ch29, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 33.08
Std Dev 11.13
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch29, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 39.94
Std Dev 11.86
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U22-ch29, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 48.46
Std Dev 3.496
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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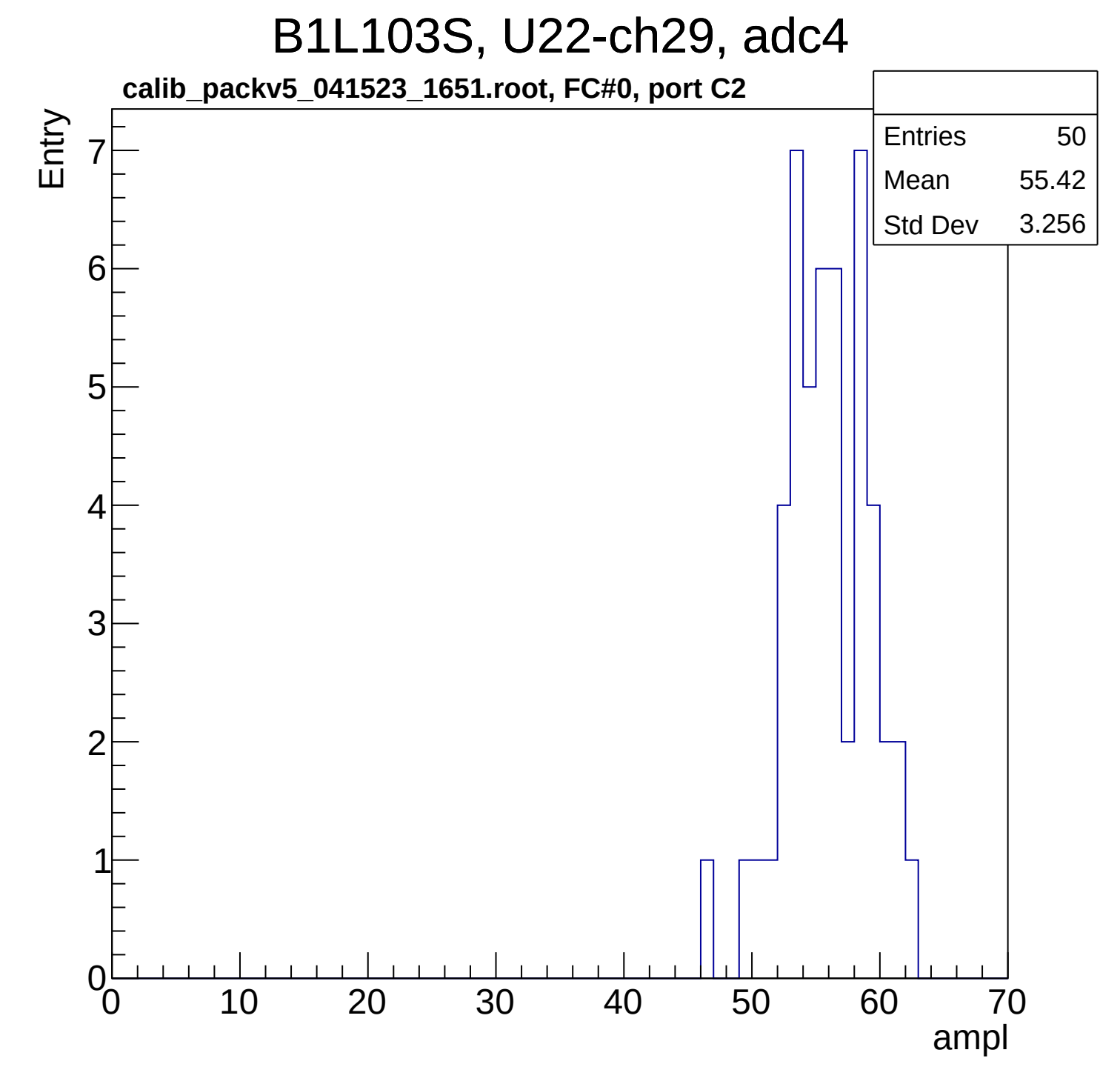
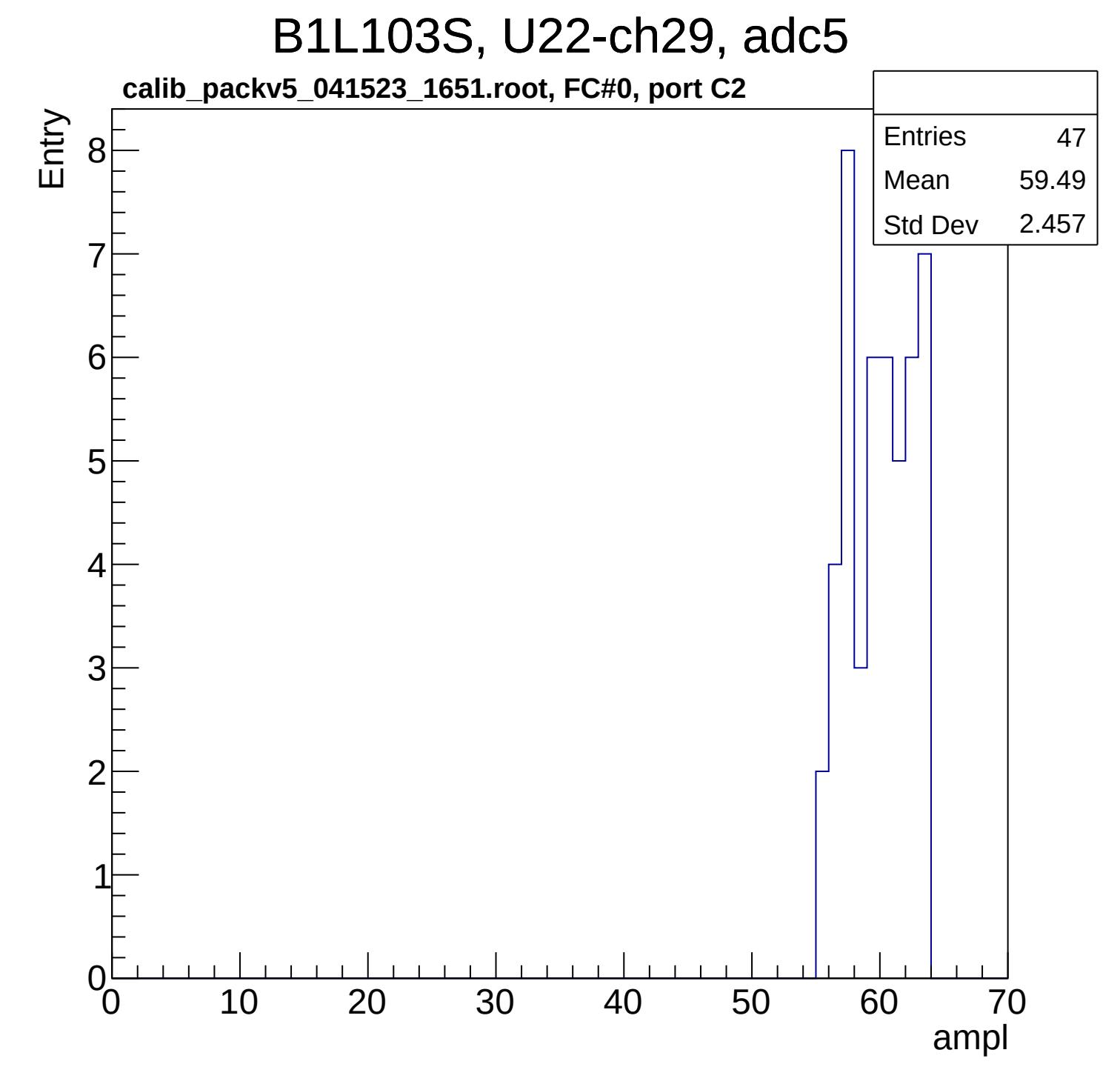

B1L103S, U22-ch29, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 55.42
Std Dev 3.256
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U22-ch29, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 59.49
Std Dev 2.457
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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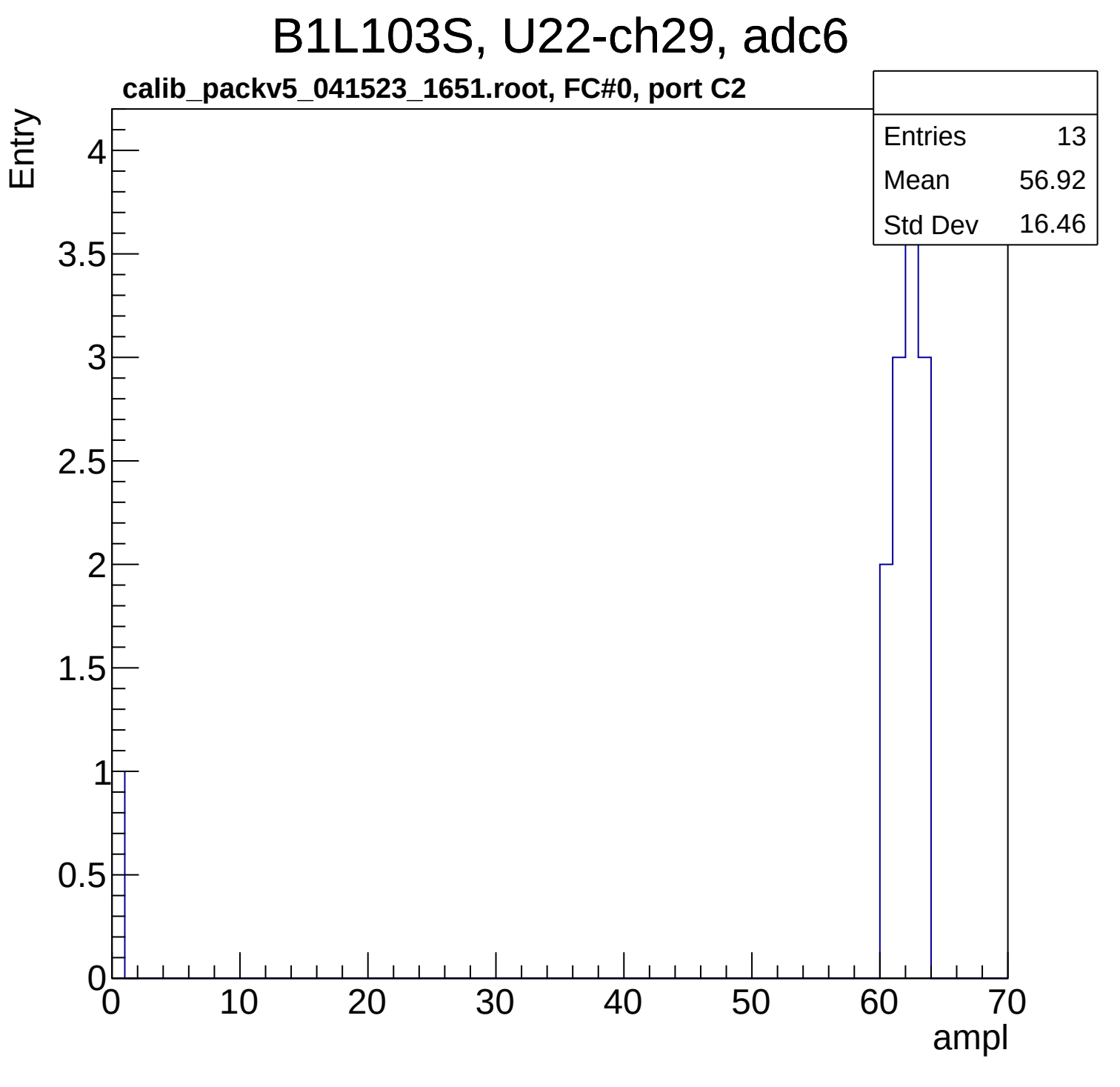
B1L103S, U22-ch29, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 56.92
Std Dev 16.46
Entry
ampl
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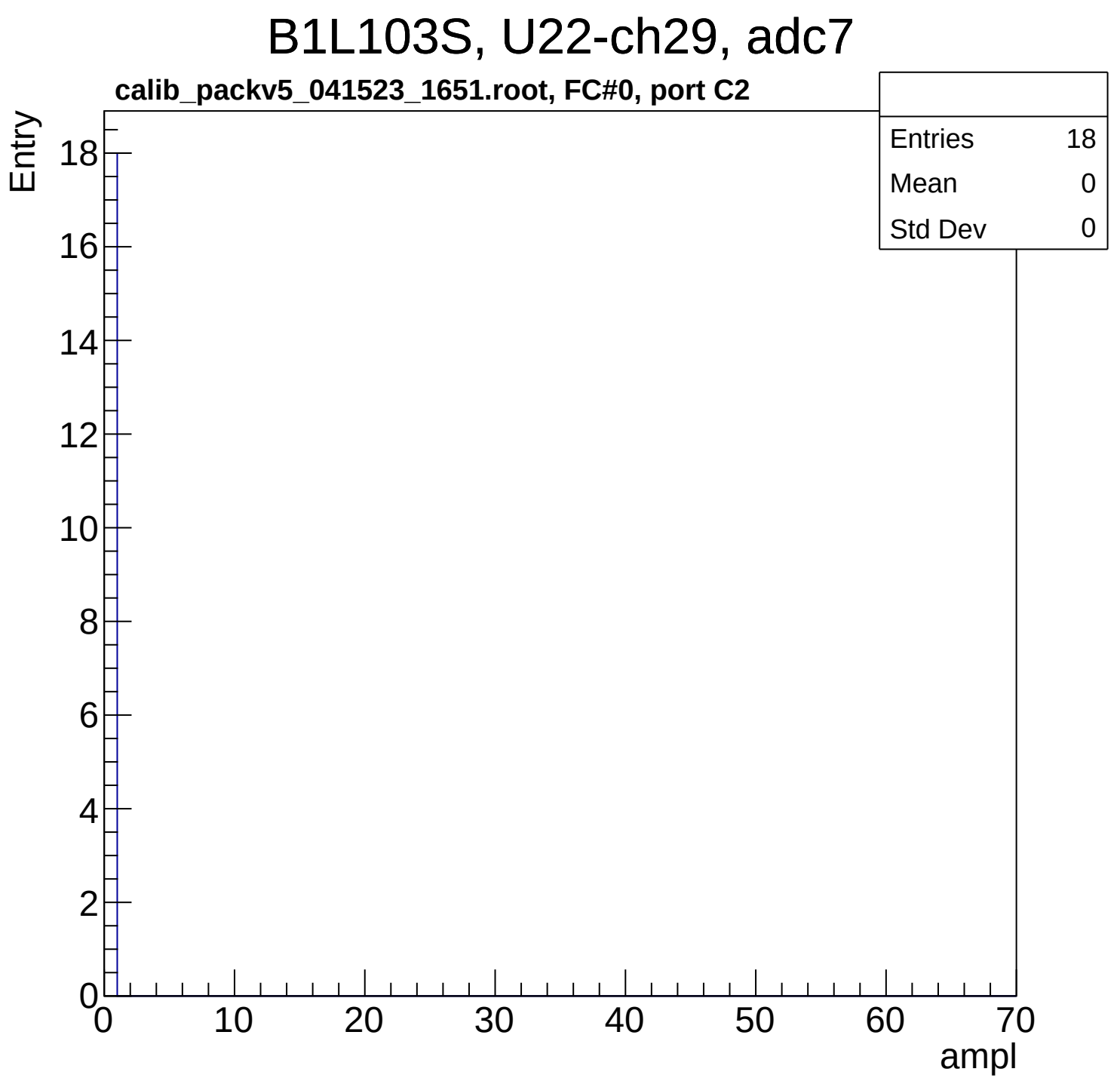
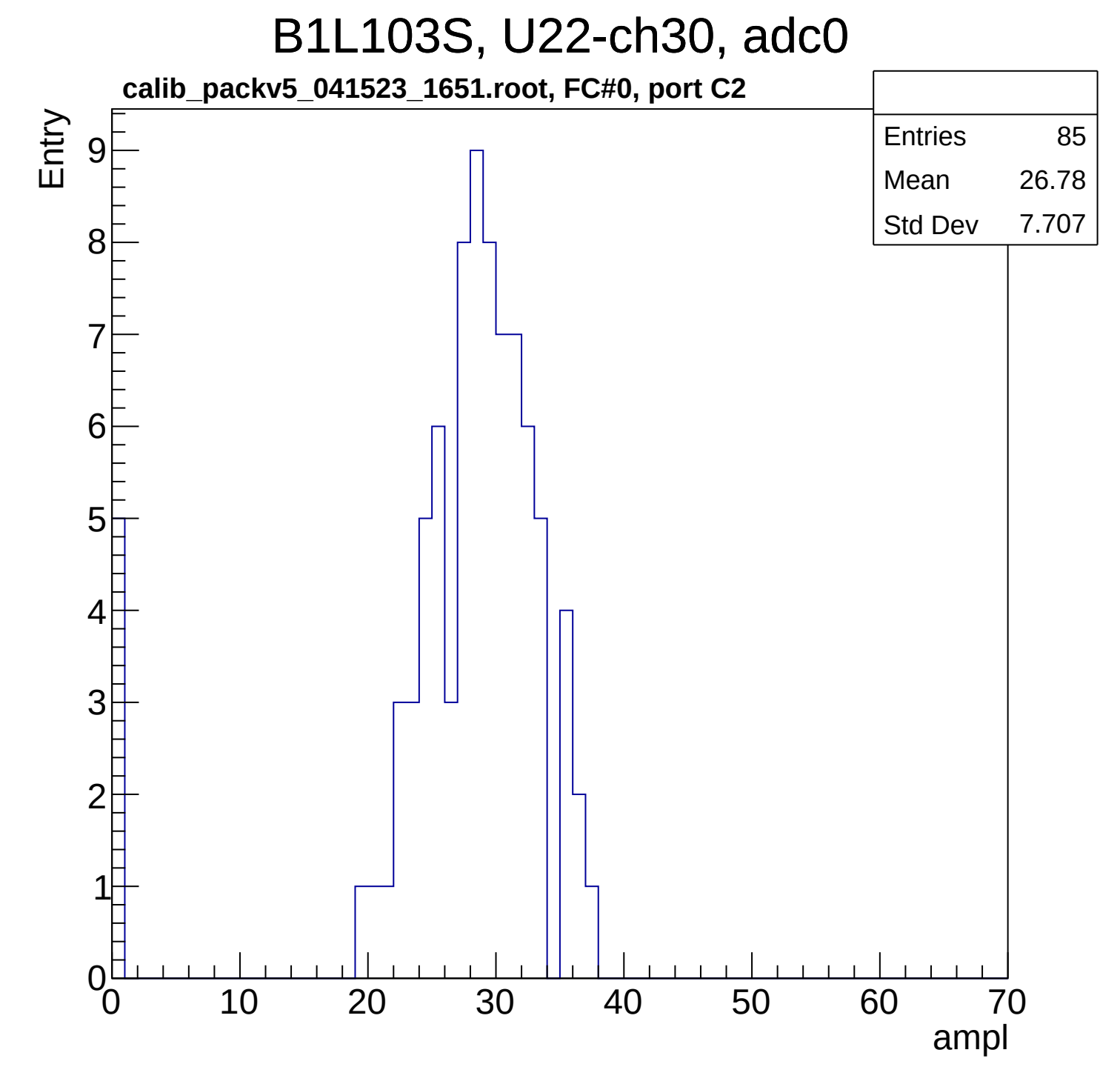
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U22-ch29, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch30, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 26.78
Std Dev 7.707
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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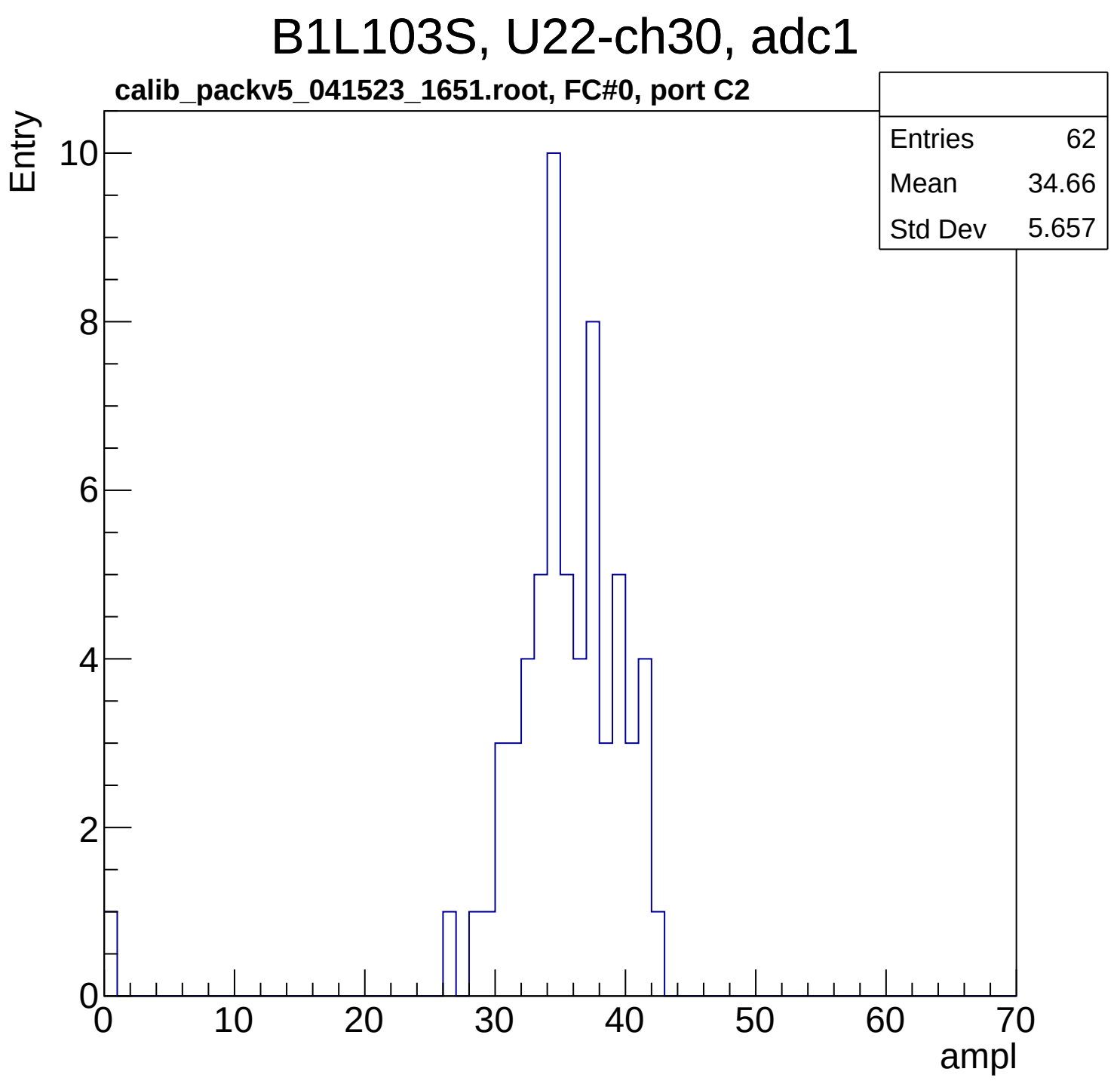
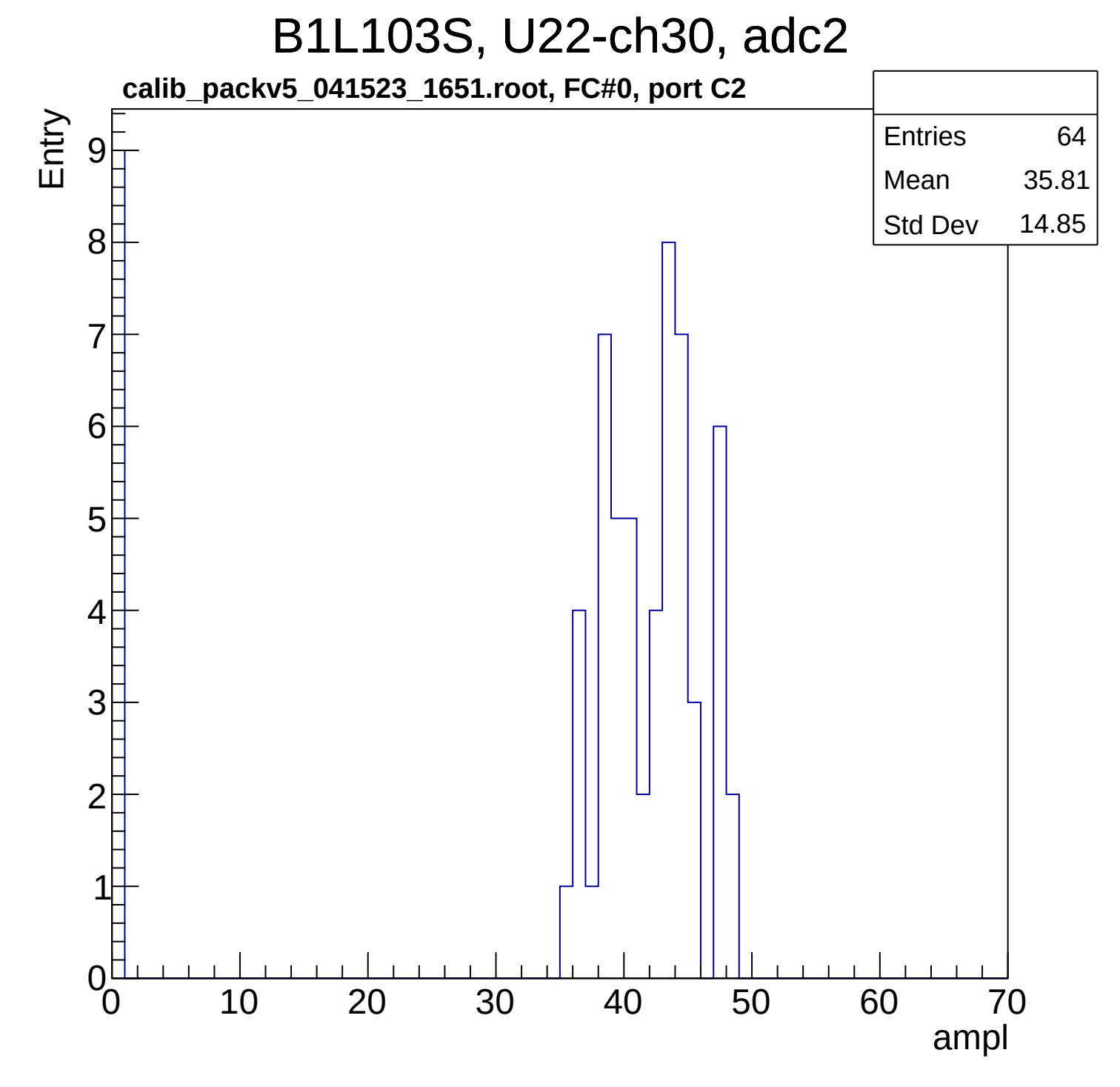
60
70


B1L103S, U22-ch30, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 34.66
Std Dev 5.657
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U22-ch30, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 35.81
Std Dev 14.85
Entry
ampl
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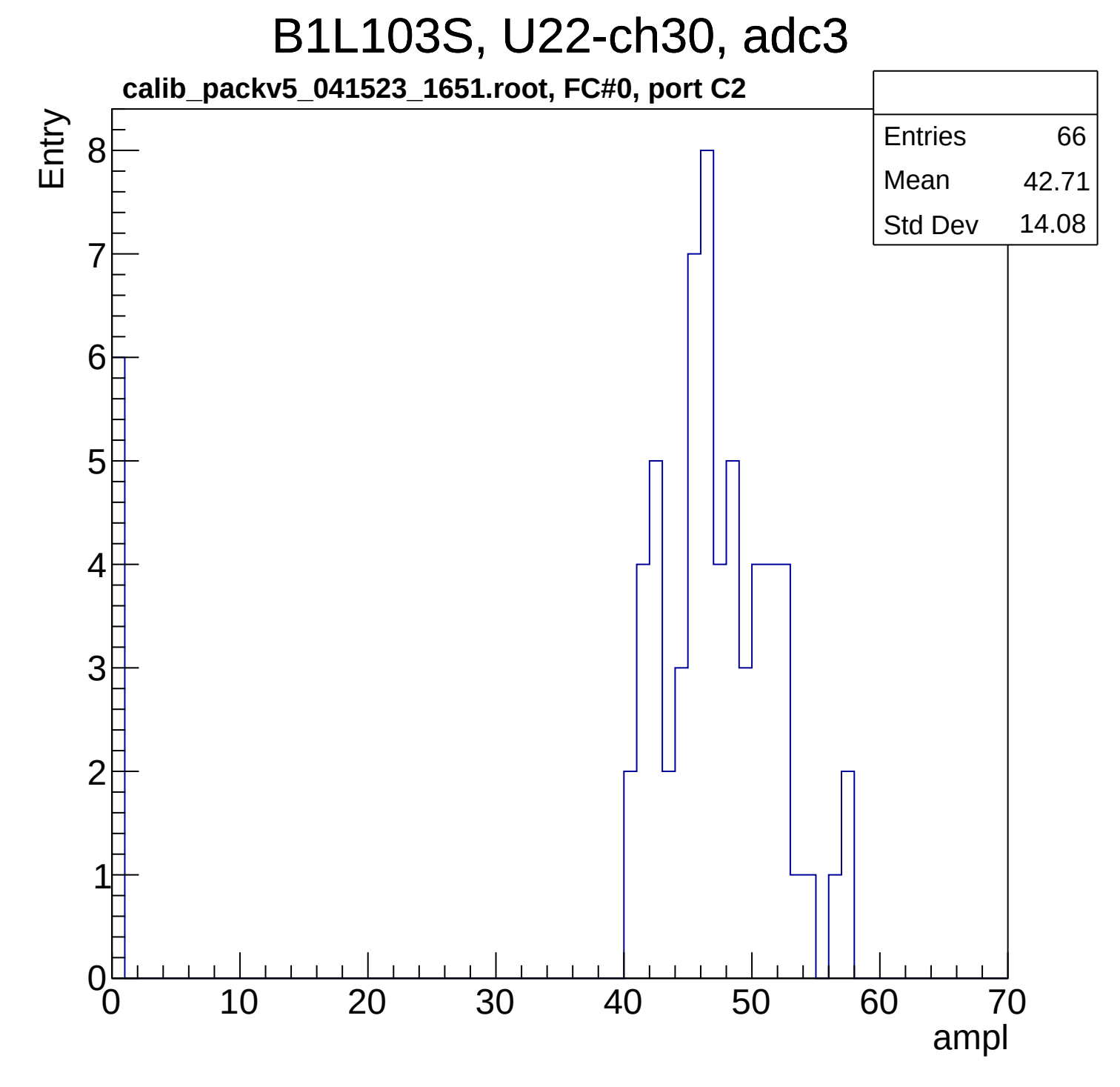
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch30, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 42.71
Std Dev 14.08
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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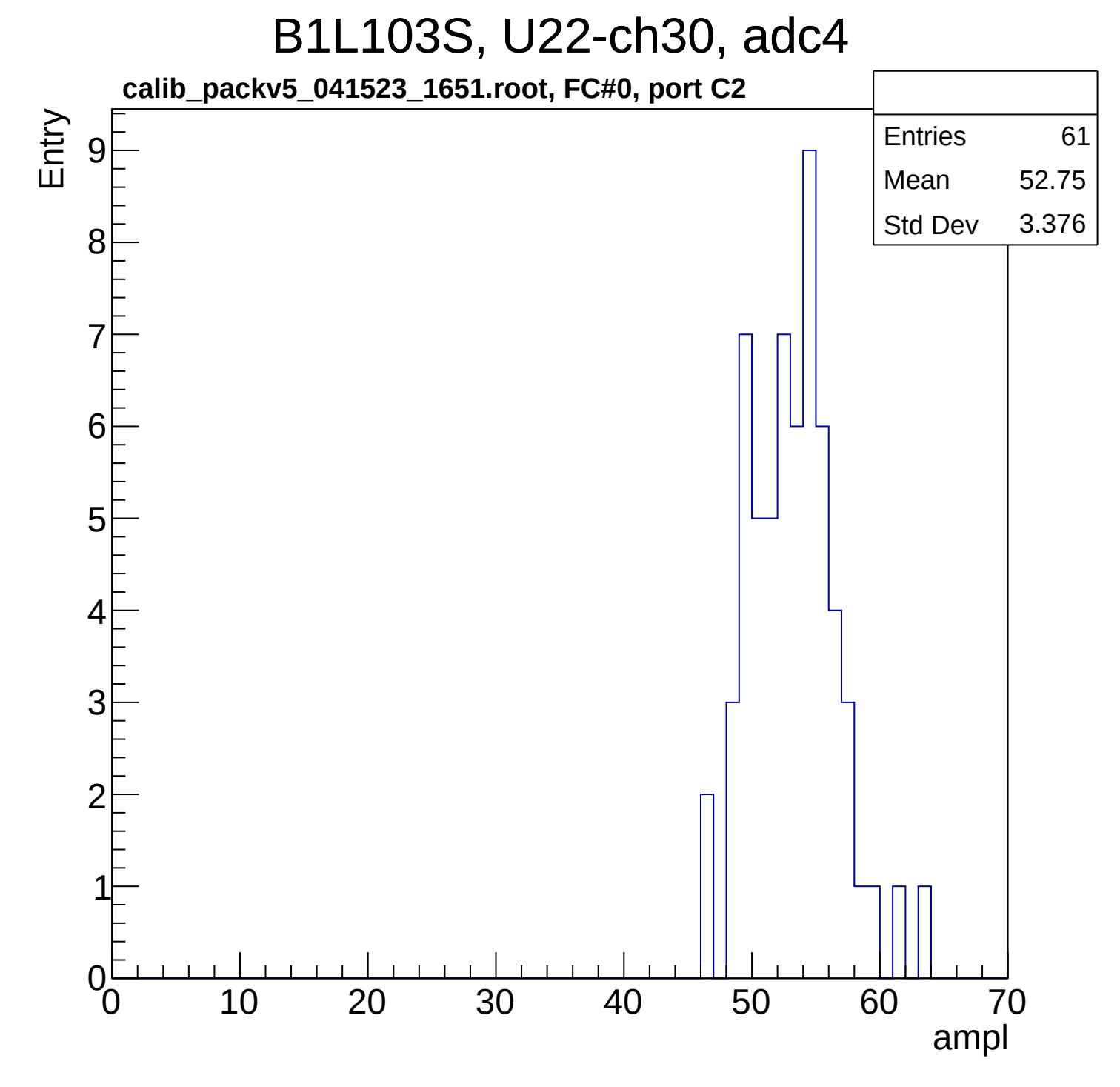
40
50
60
70


B1L103S, U22-ch30, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 52.75
Std Dev 3.376
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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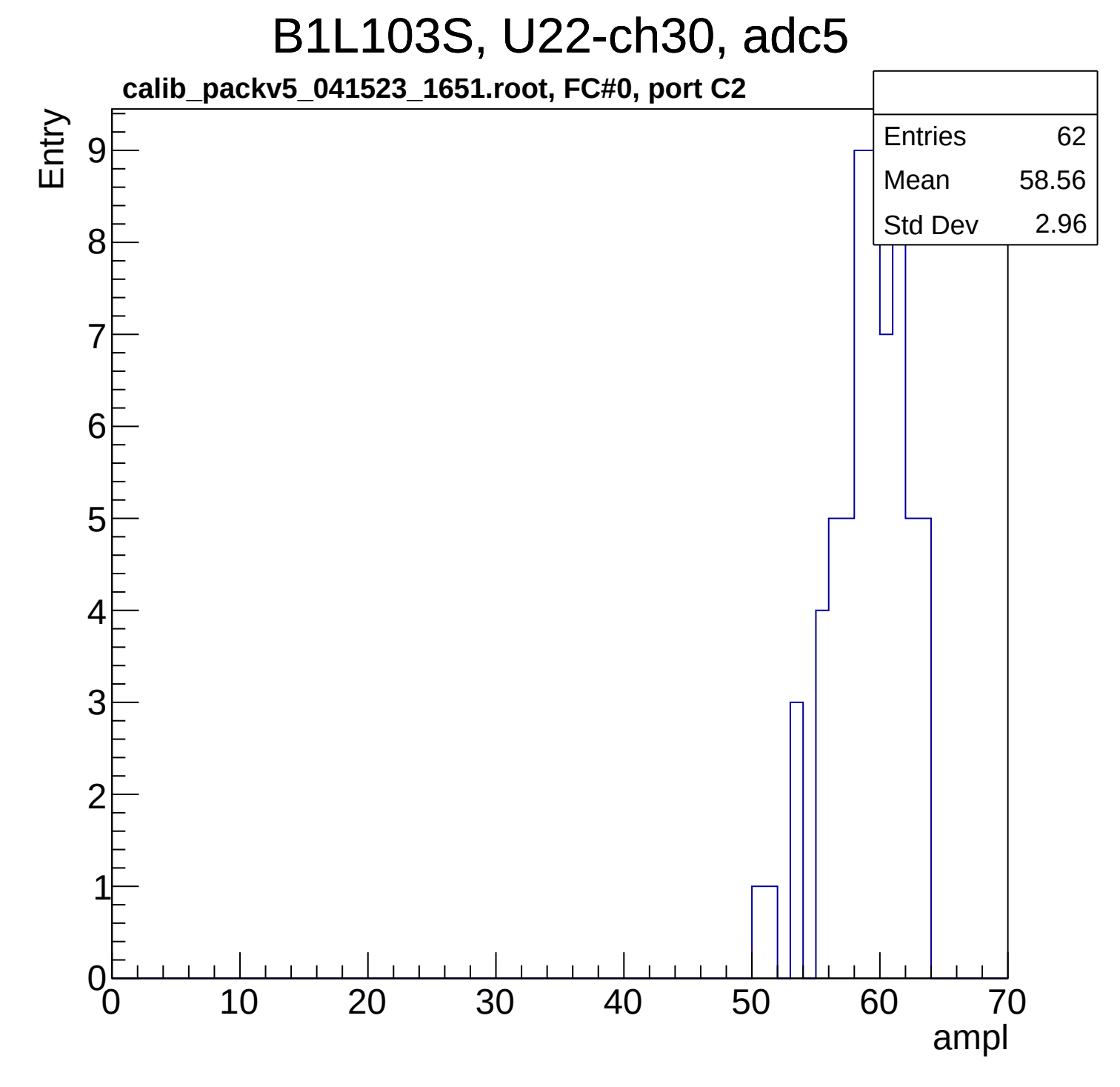
60
70


B1L103S, U22-ch30, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 58.56
Std Dev 2.96
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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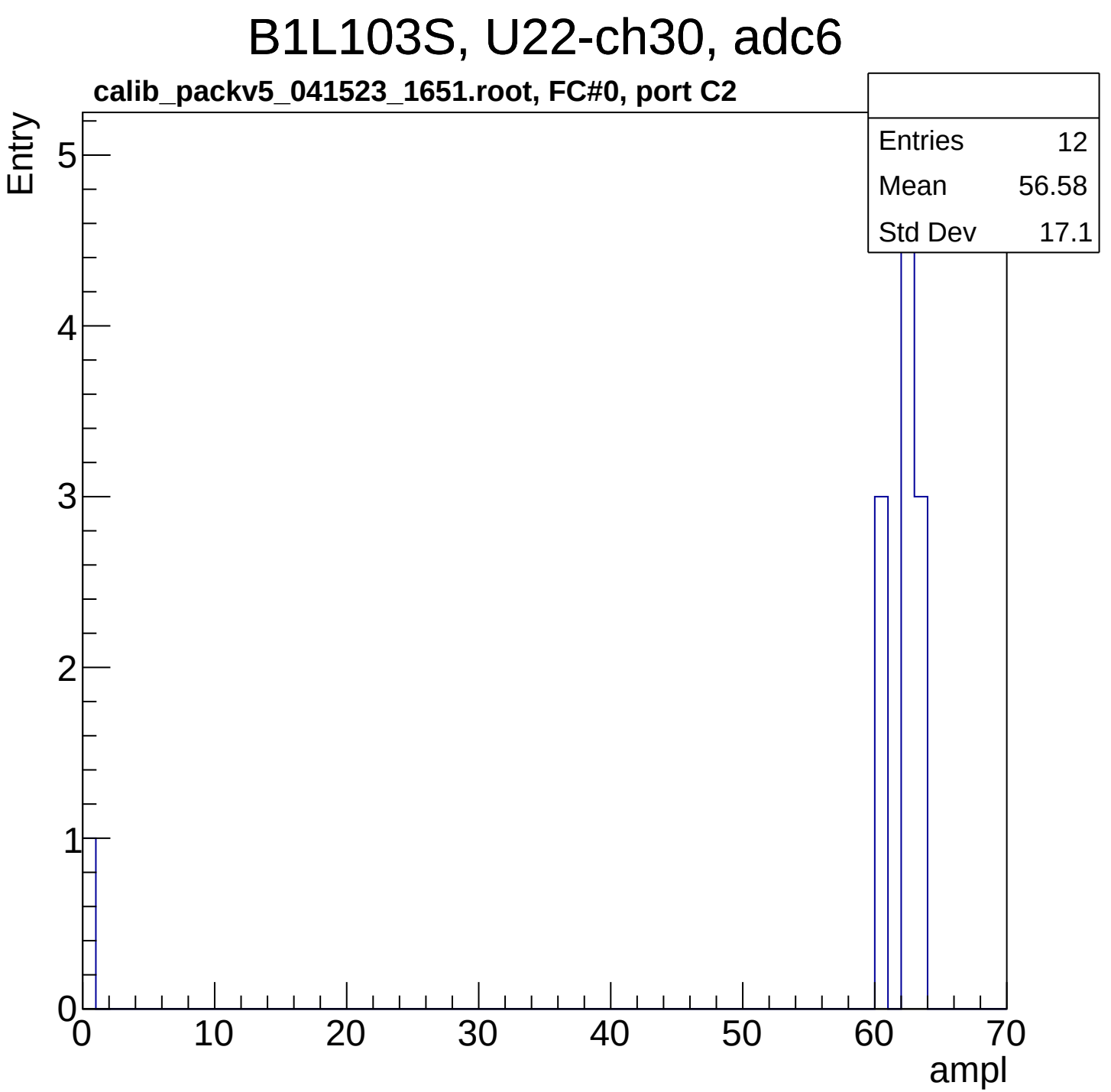
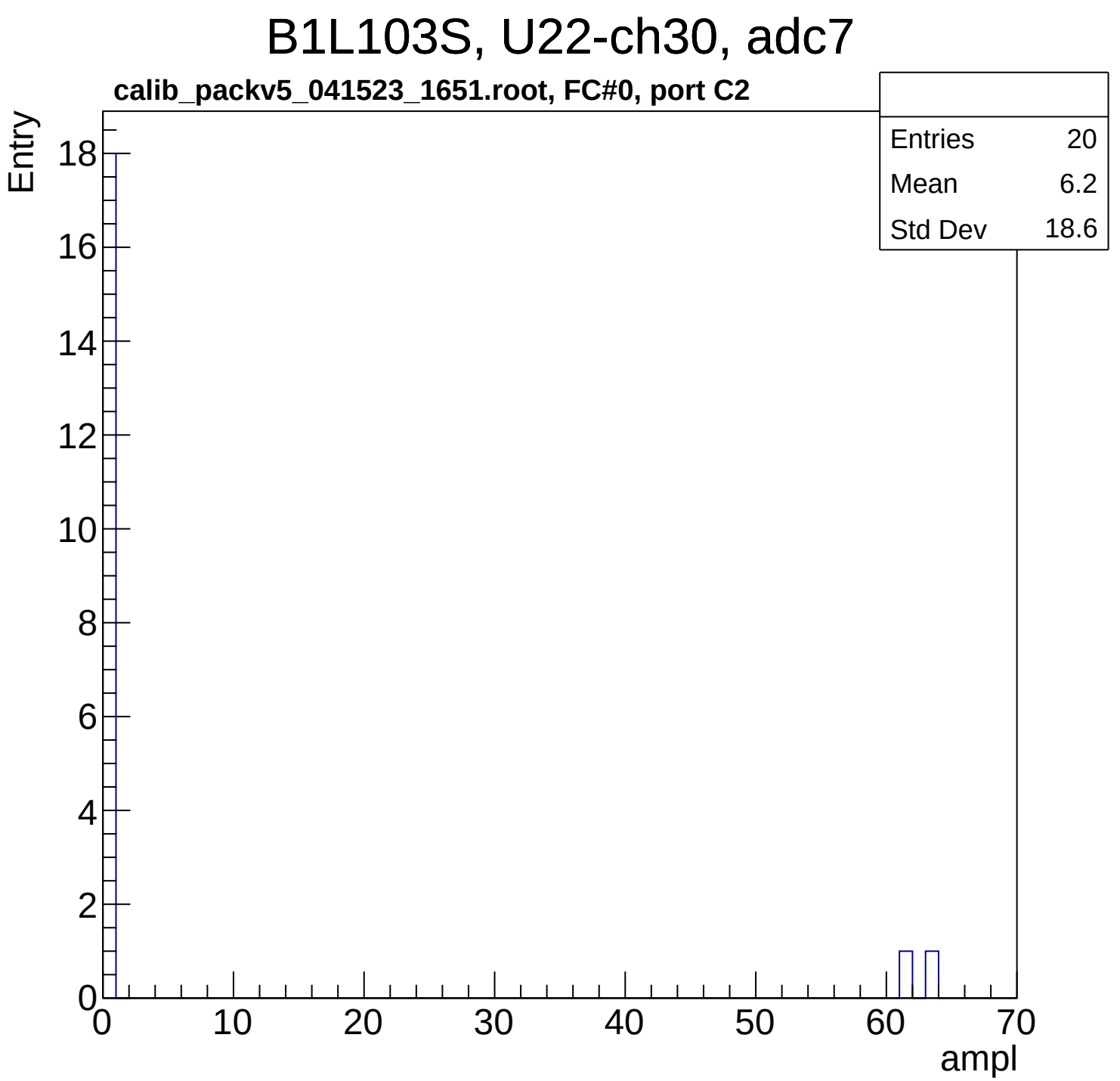

B1L103S, U22-ch30, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 56.58
Std Dev 17.1
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch30, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 6.2
Std Dev 18.6
Entry
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6
8
10
12
14
16
18
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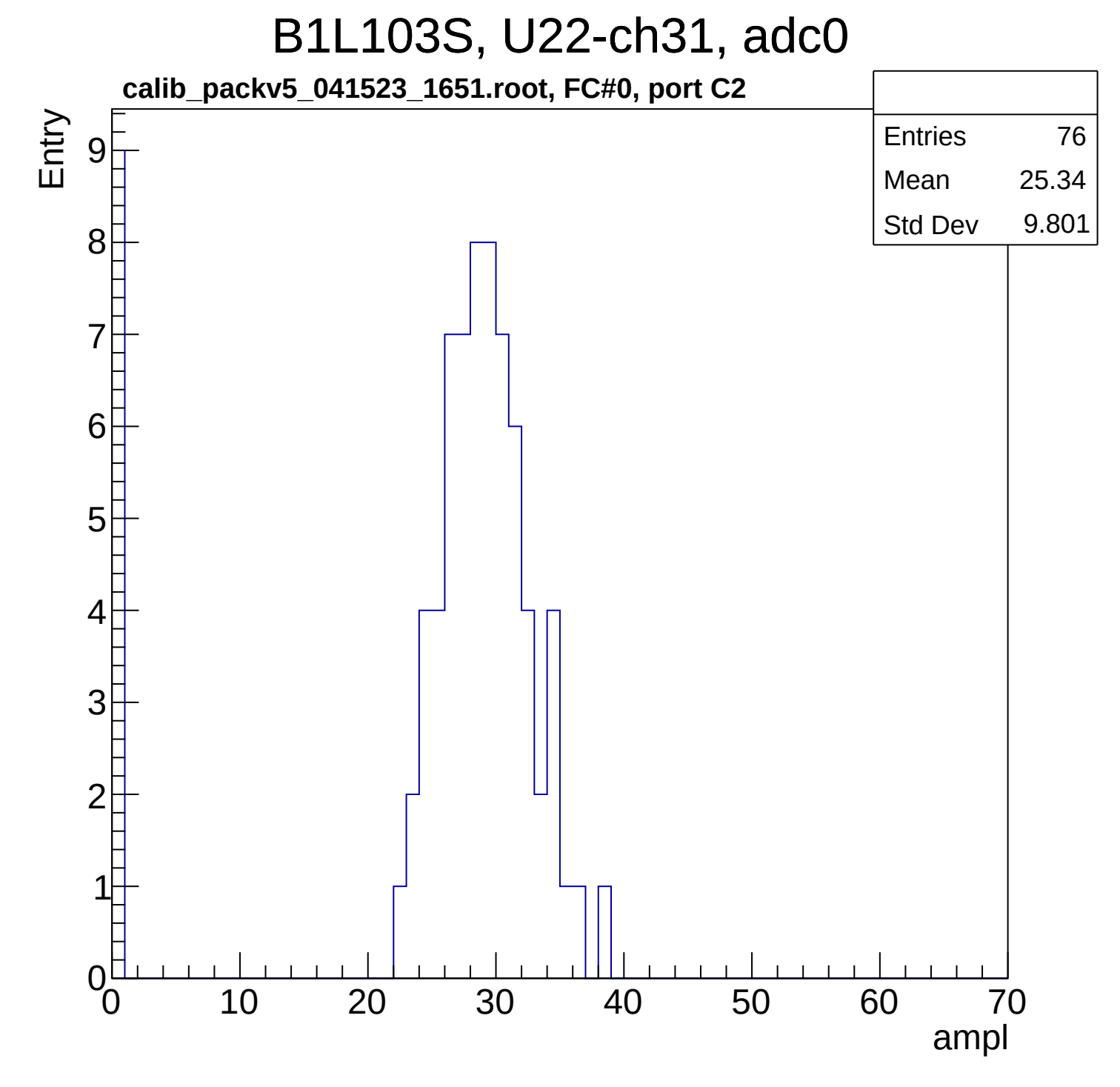
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch31, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 25.34
Std Dev 9.801
Entry
ampl
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2
3
4
5
6
7
8
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0
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60
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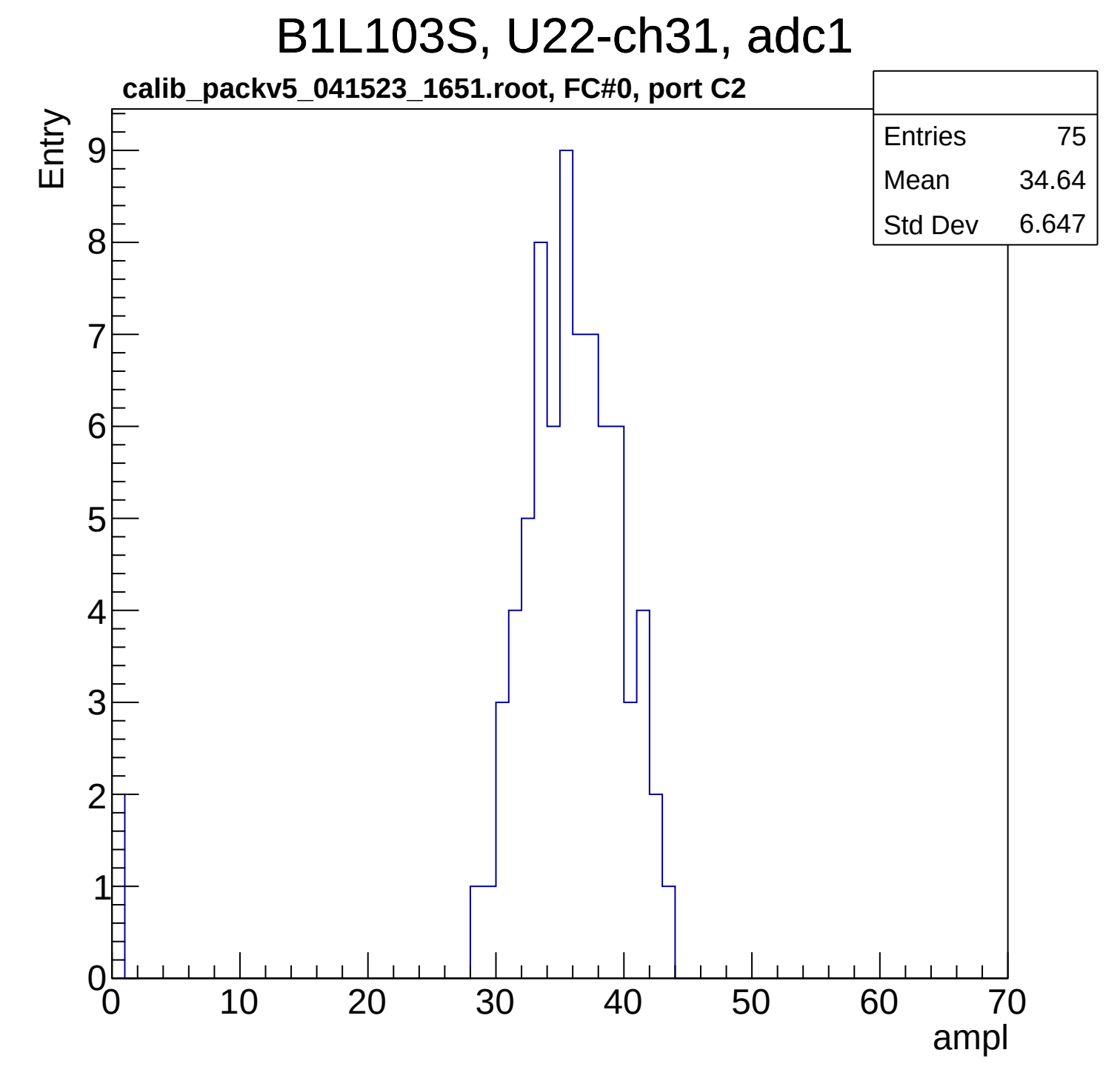
B1L103S, U22-ch31, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 34.64
Std Dev 6.647
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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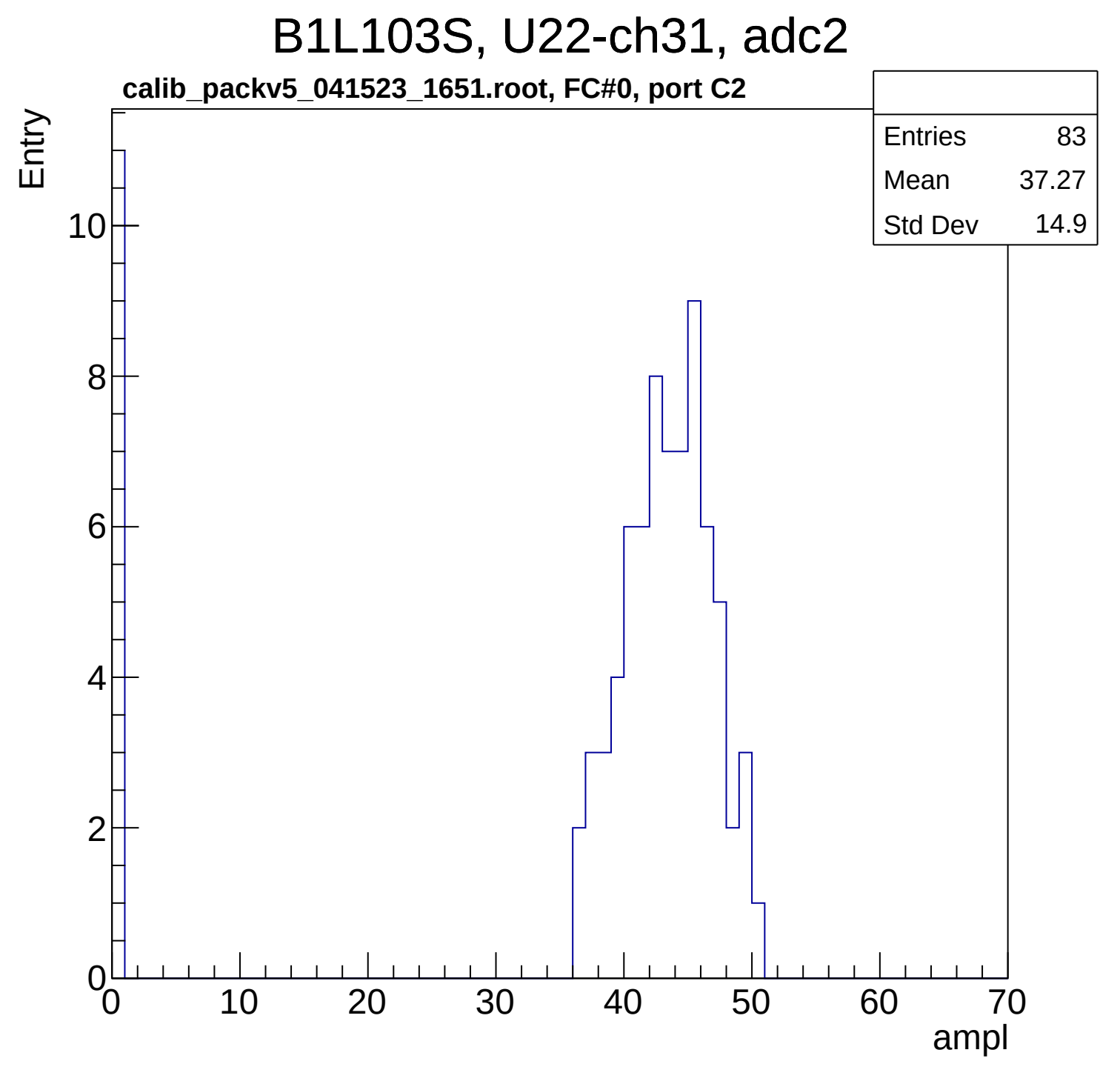
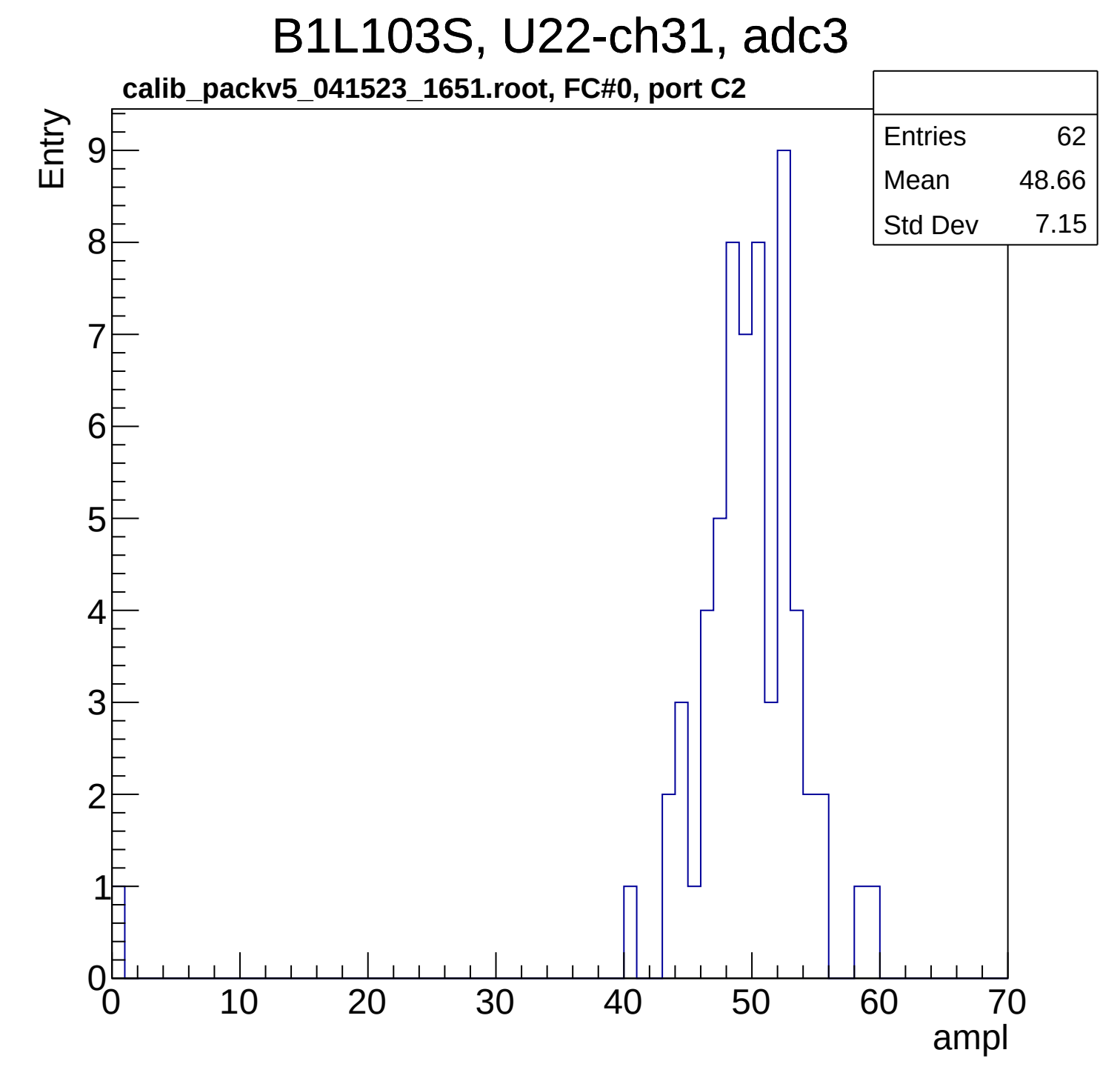
40
50
60
70


B1L103S, U22-ch31, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 37.27
Std Dev 14.9
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch31, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 48.66
Std Dev 7.15
Entry
ampl
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10
20
30
40
50
60
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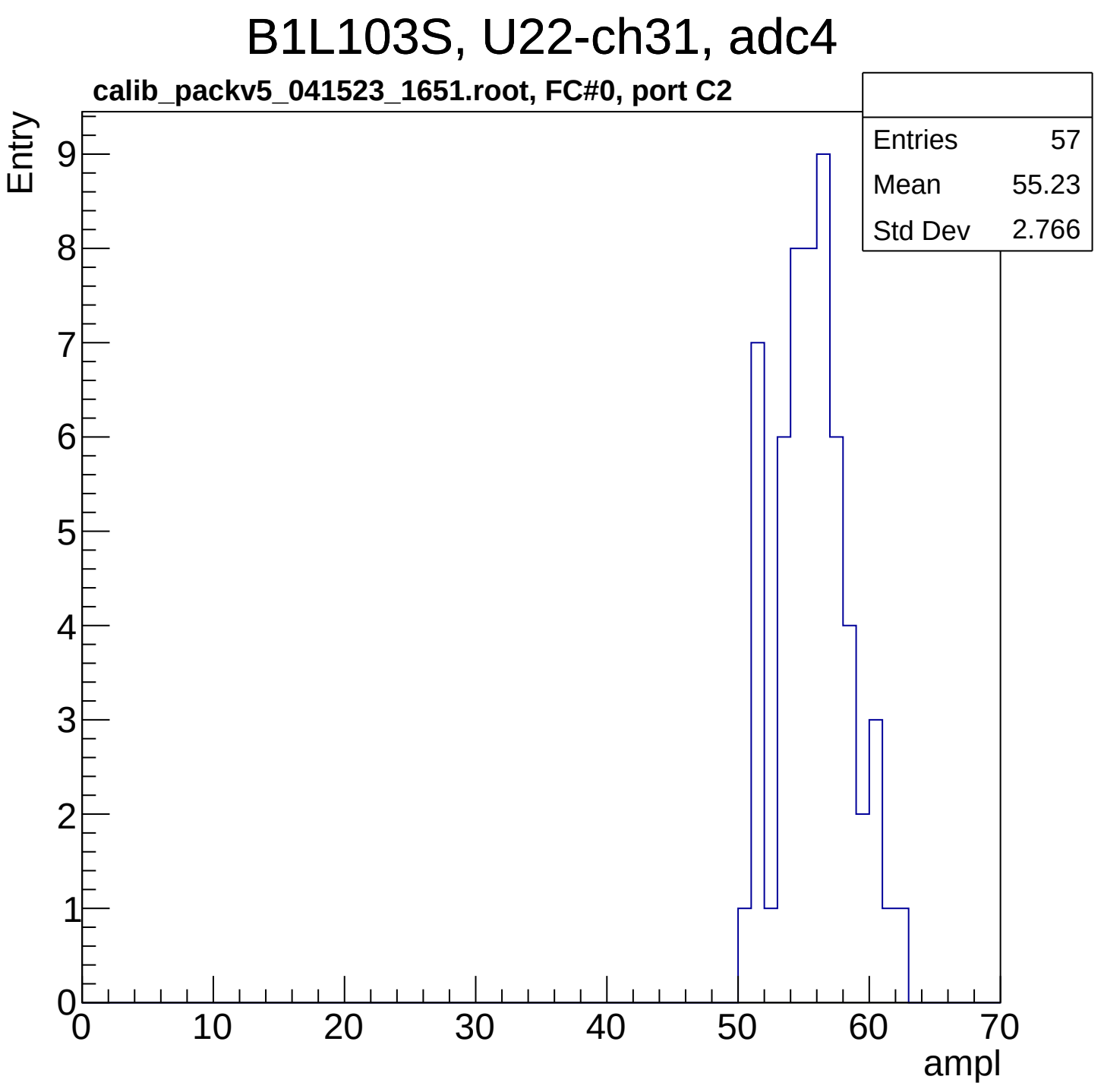
1
2
3
4
5
6
7
8
9


B1L103S, U22-ch31, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 55.23
Std Dev 2.766
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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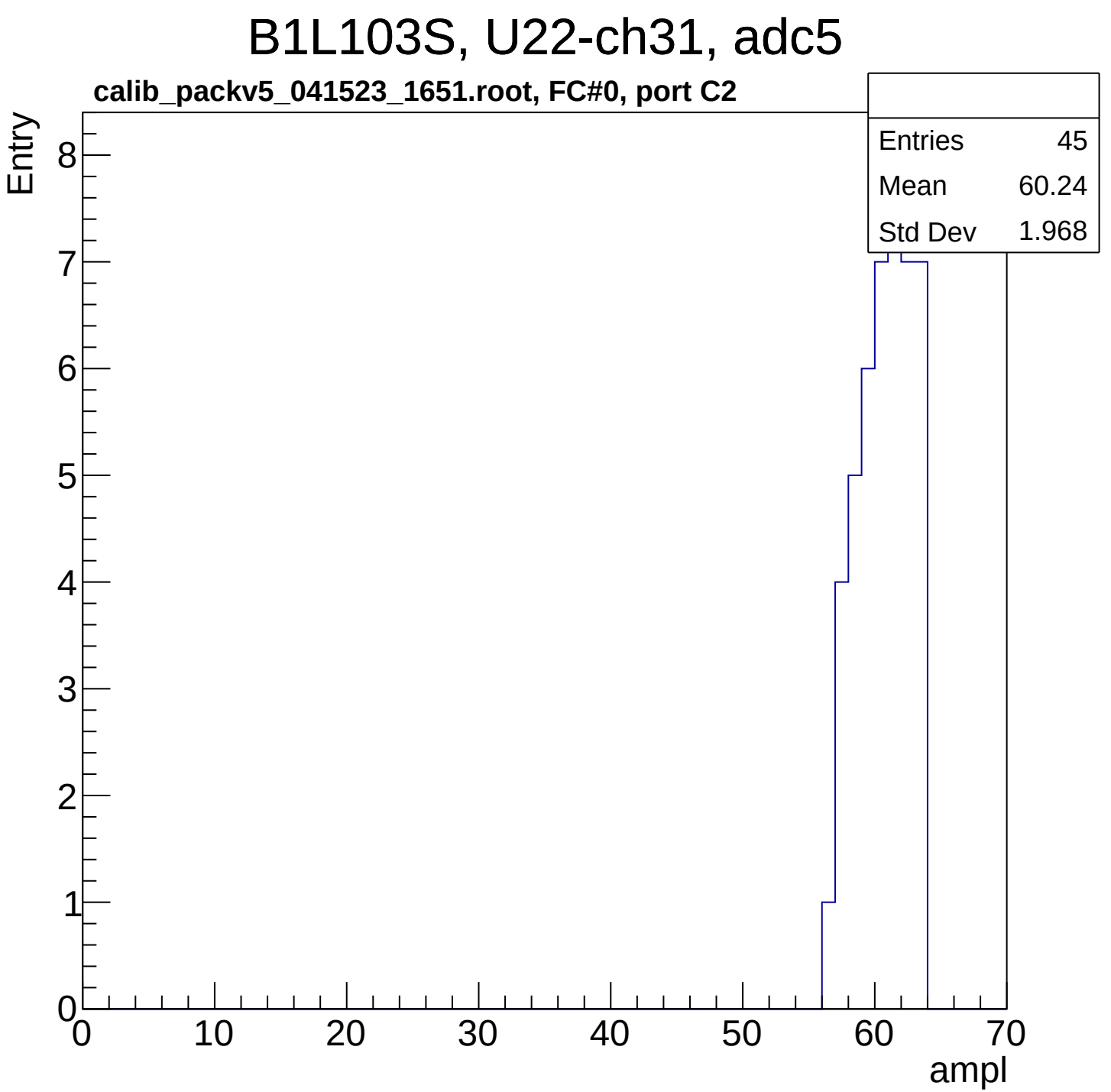
40
50
60
70


B1L103S, U22-ch31, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 60.24
Std Dev 1.968
Entry
ampl
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1
2
3
4
5
6
7
8
0
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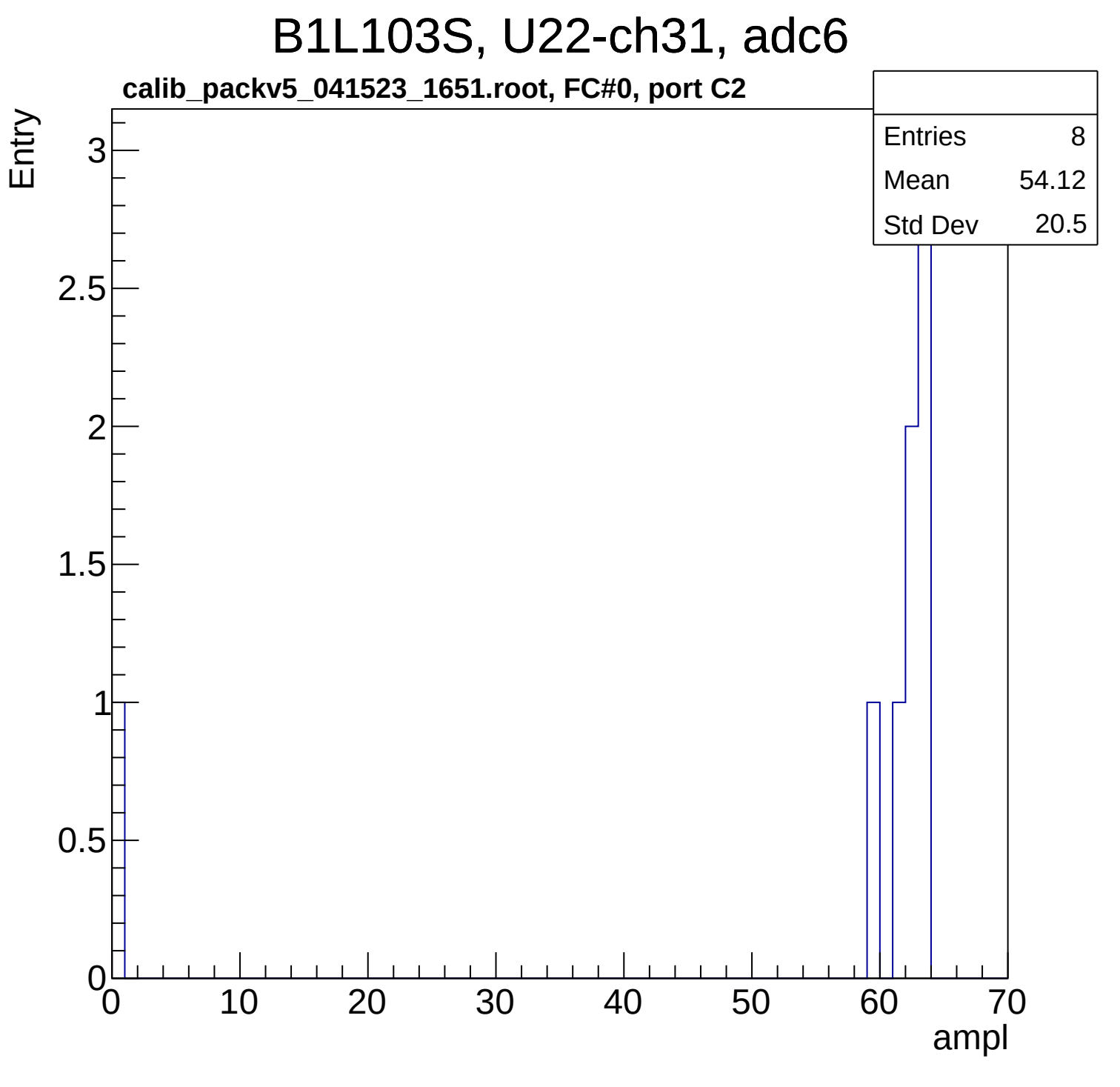
40
50
60
70


B1L103S, U22-ch31, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 54.12
Std Dev 20.5
Entry
ampl
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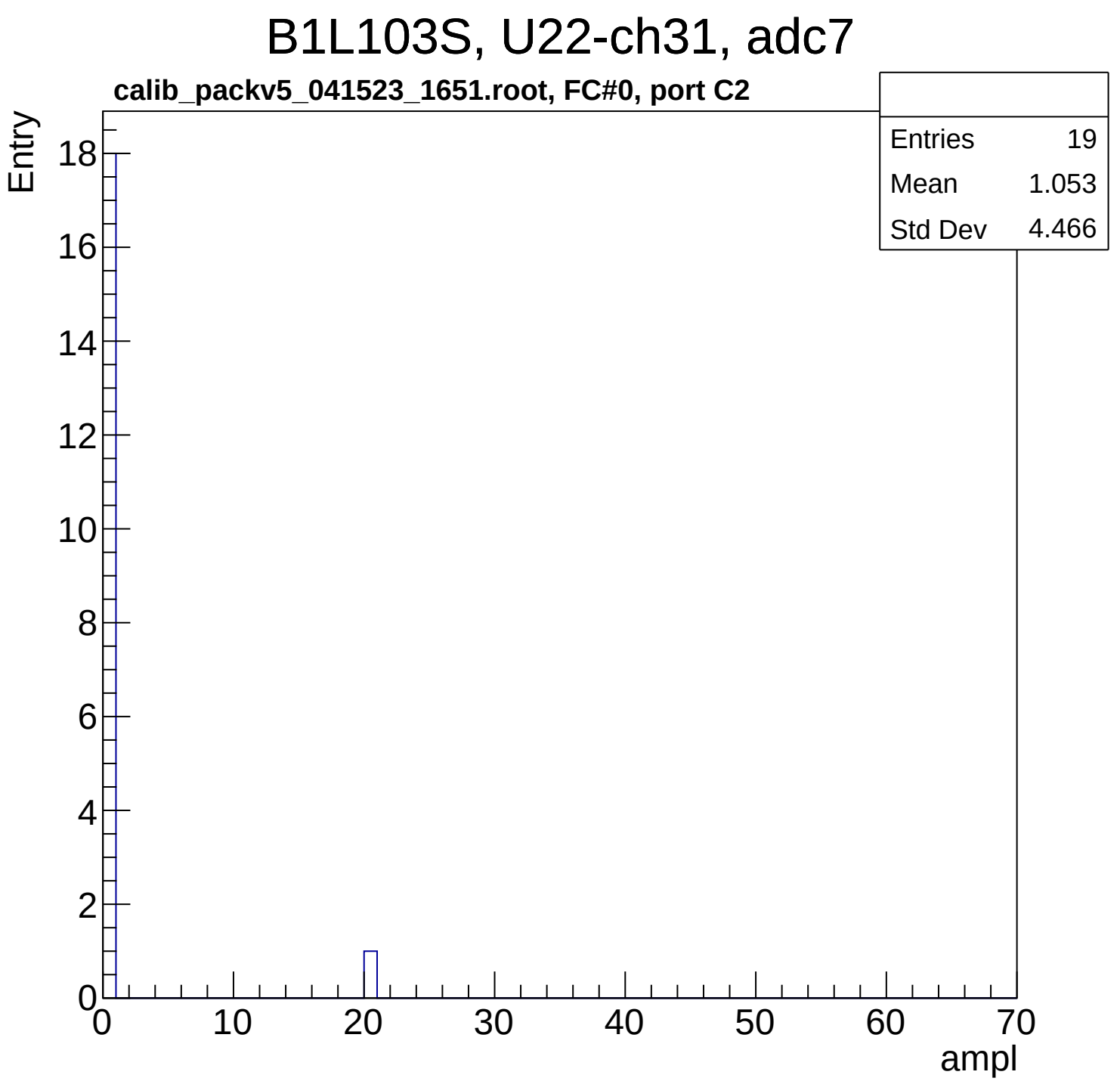
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U22-ch31, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.053
Std Dev 4.466
Entry
ampl
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2
4
6
8
10
12
14
16
18
0
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30
40
50
60
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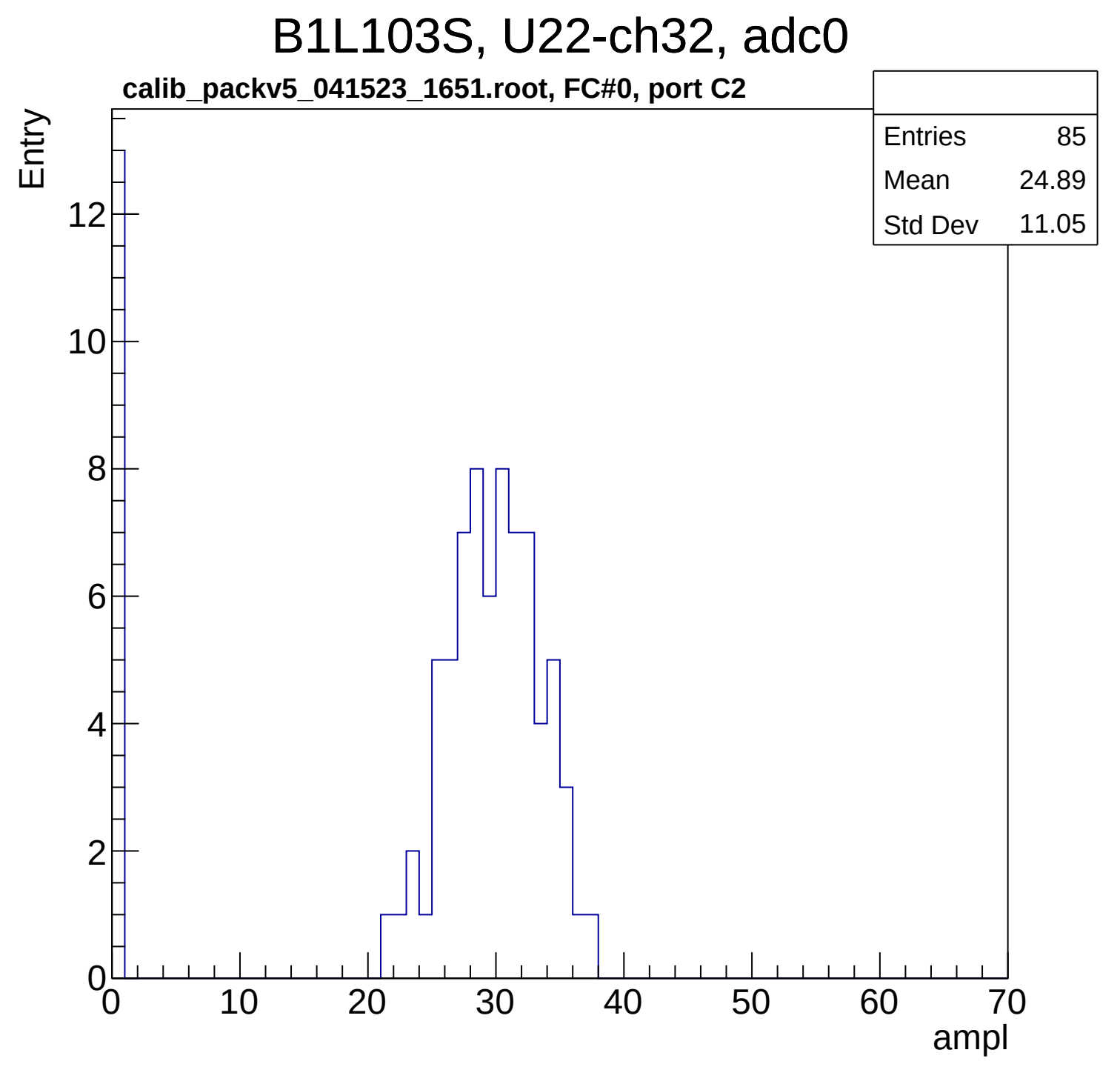
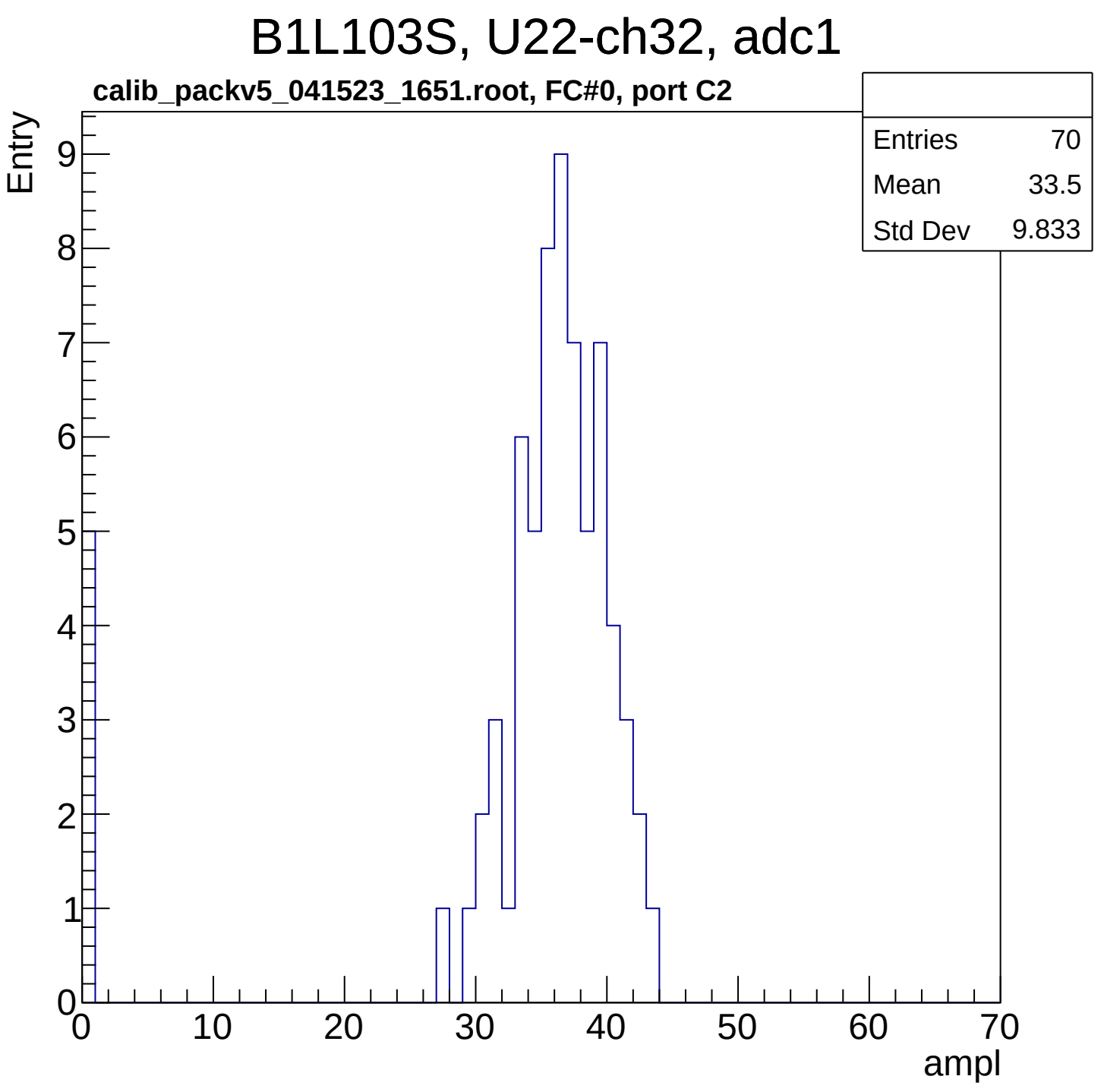

B1L103S, U22-ch32, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 24.89
Std Dev 11.05
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch32, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 33.5
Std Dev 9.833
Entry
ampl
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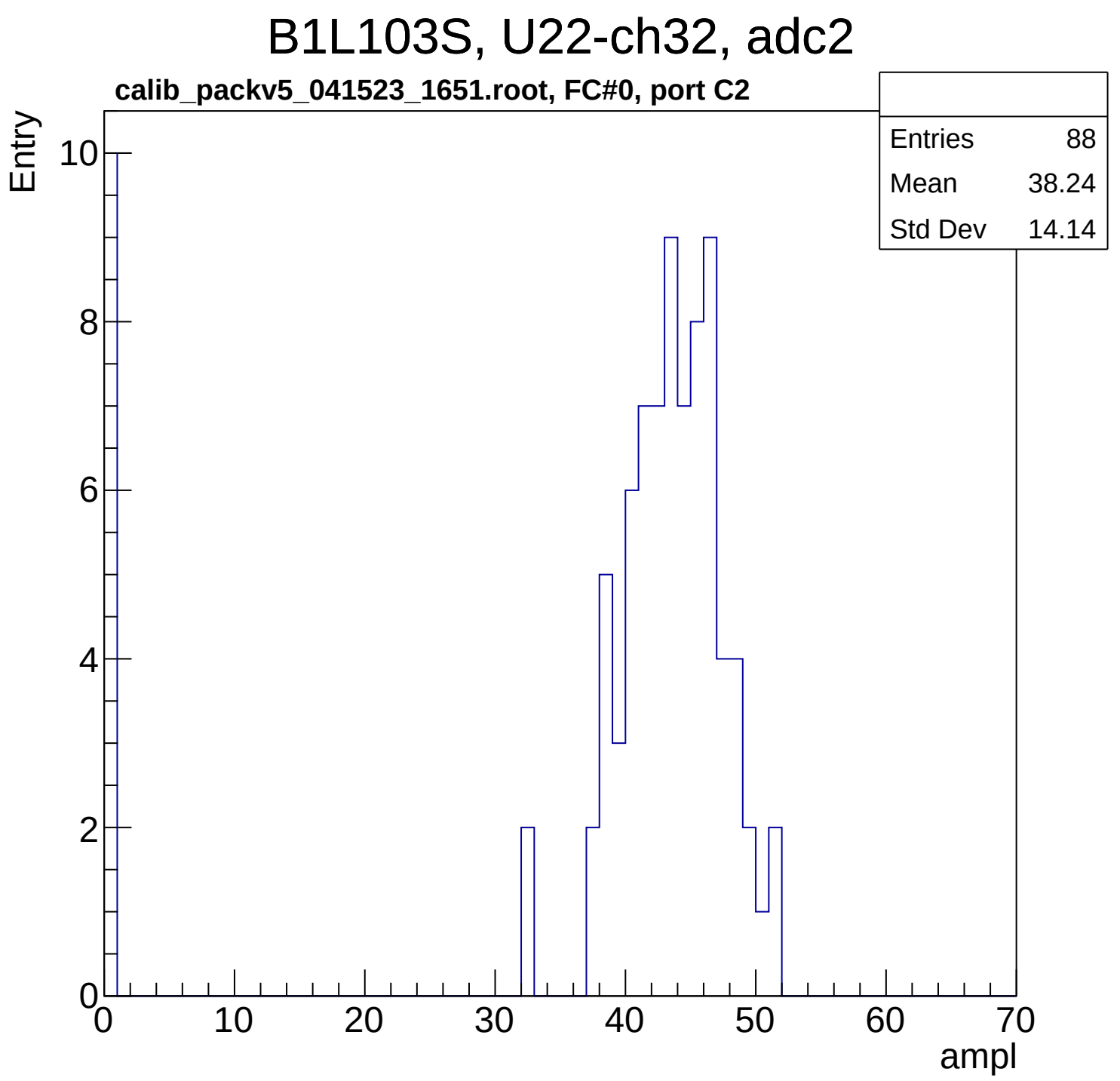
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch32, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 38.24
Std Dev 14.14
Entry
ampl
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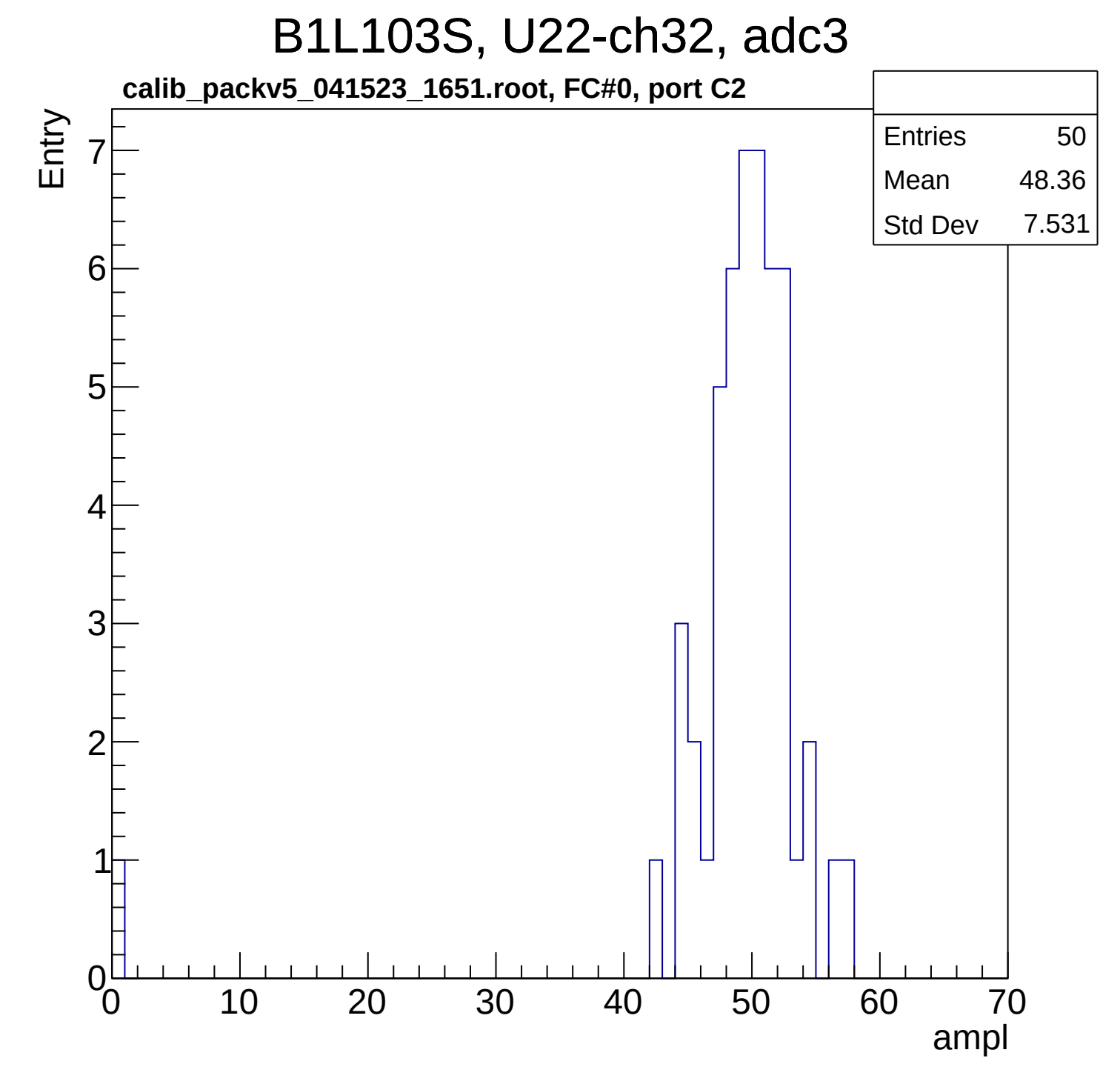
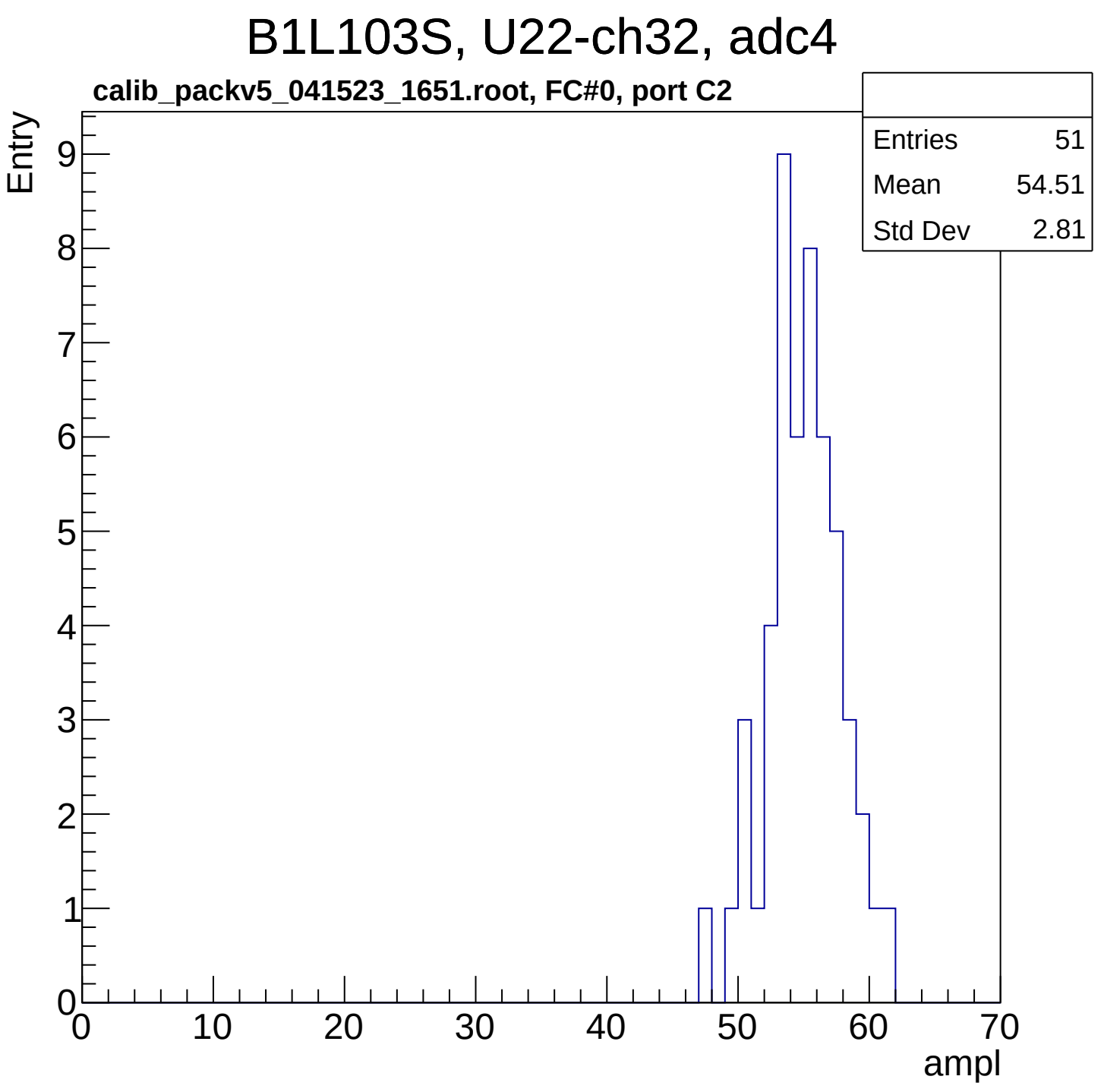
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U22-ch32, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 48.36
Std Dev 7.531
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U22-ch32, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 54.51
Std Dev 2.81
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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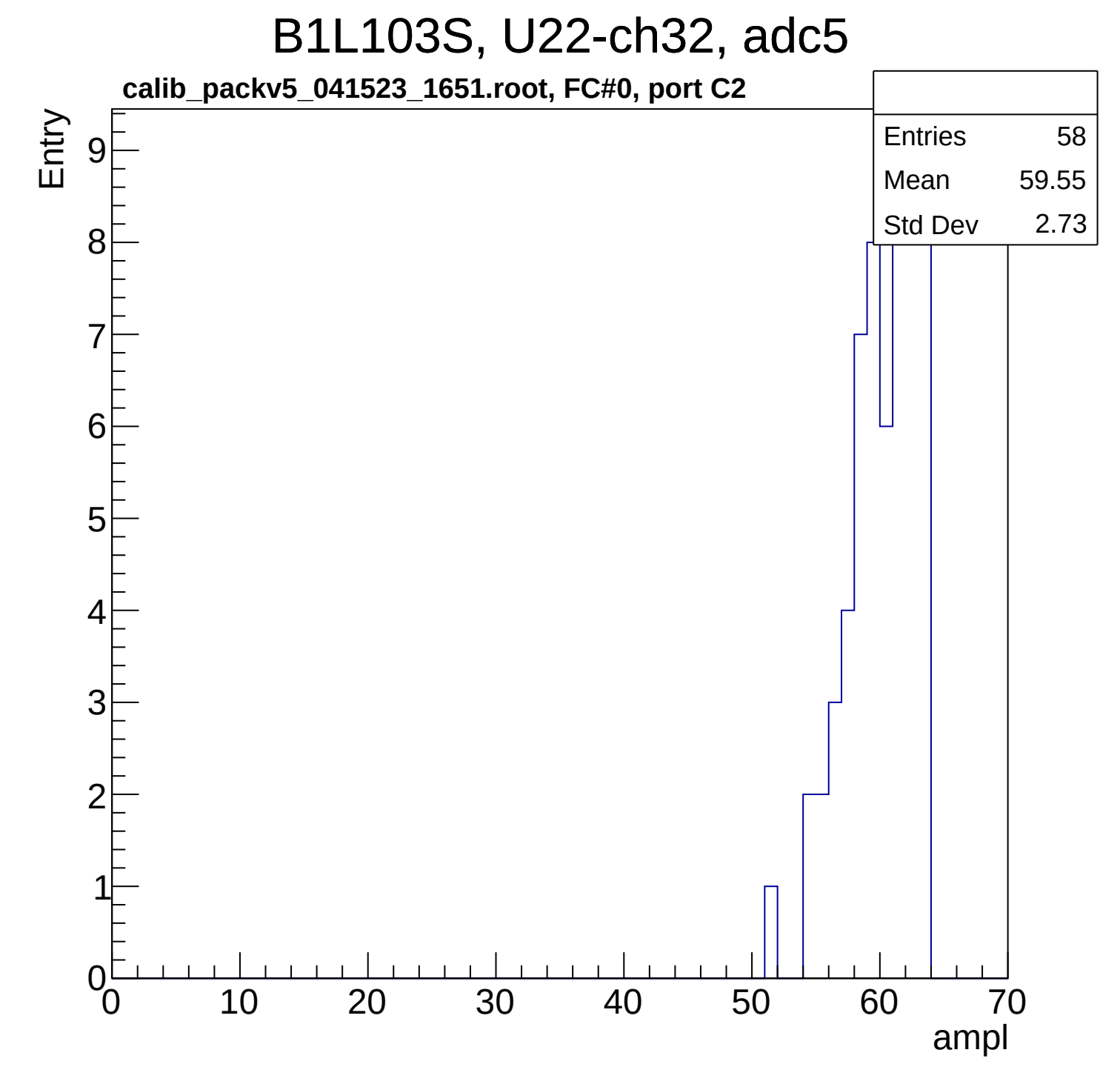
B1L103S, U22-ch32, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 59.55
Std Dev 2.73
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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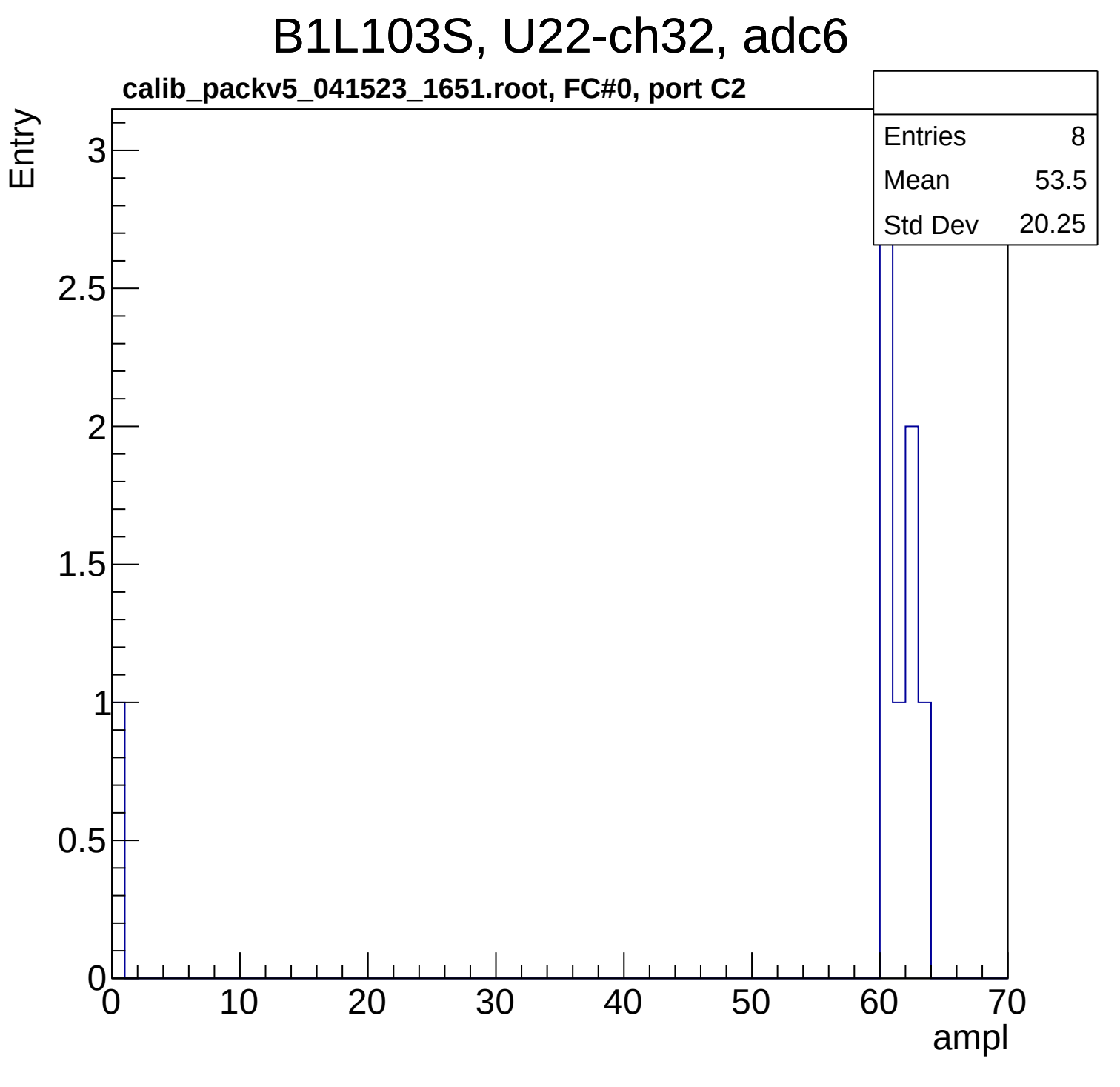
B1L103S, U22-ch32, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 53.5
Std Dev 20.25
Entry
ampl
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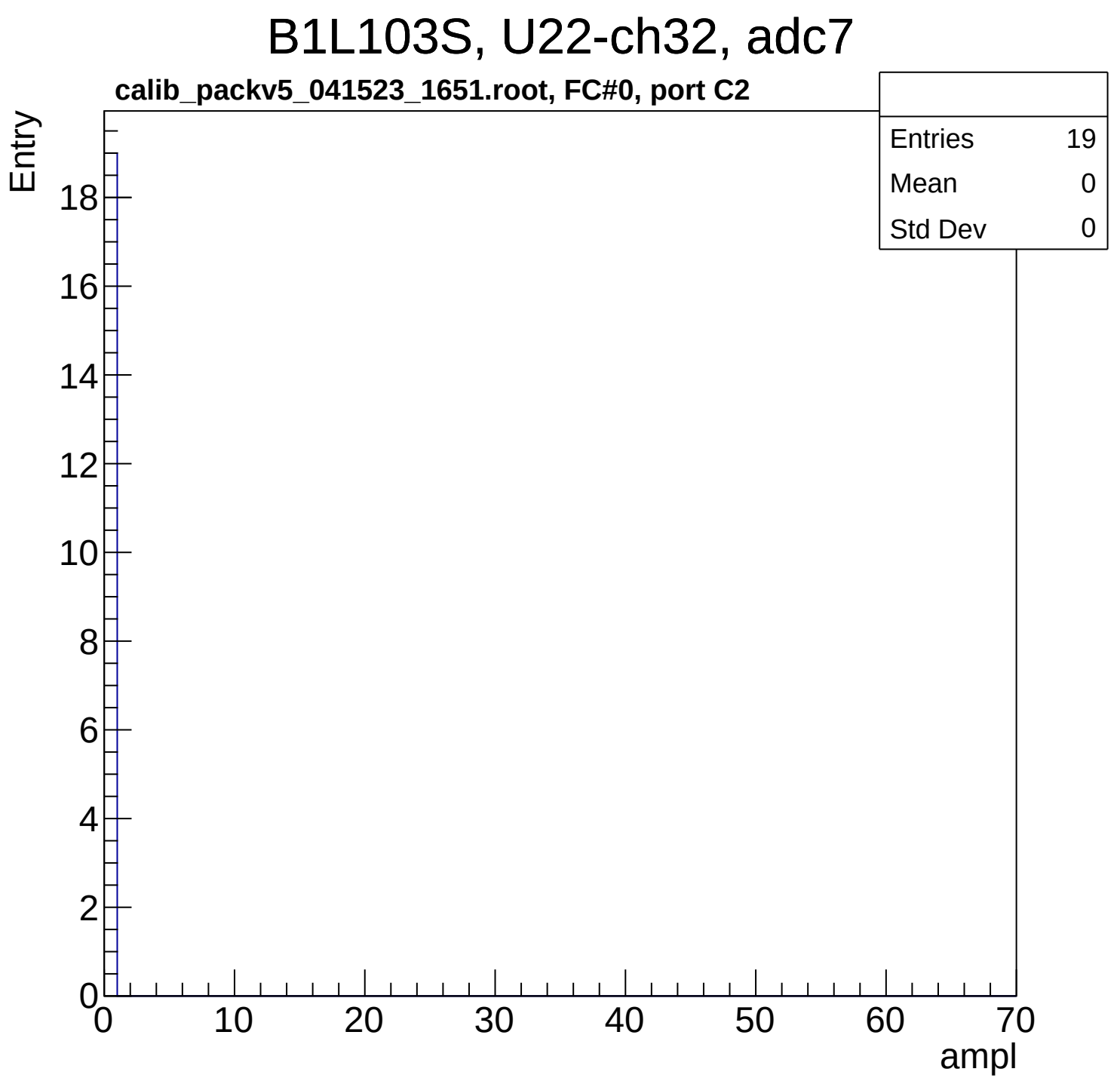
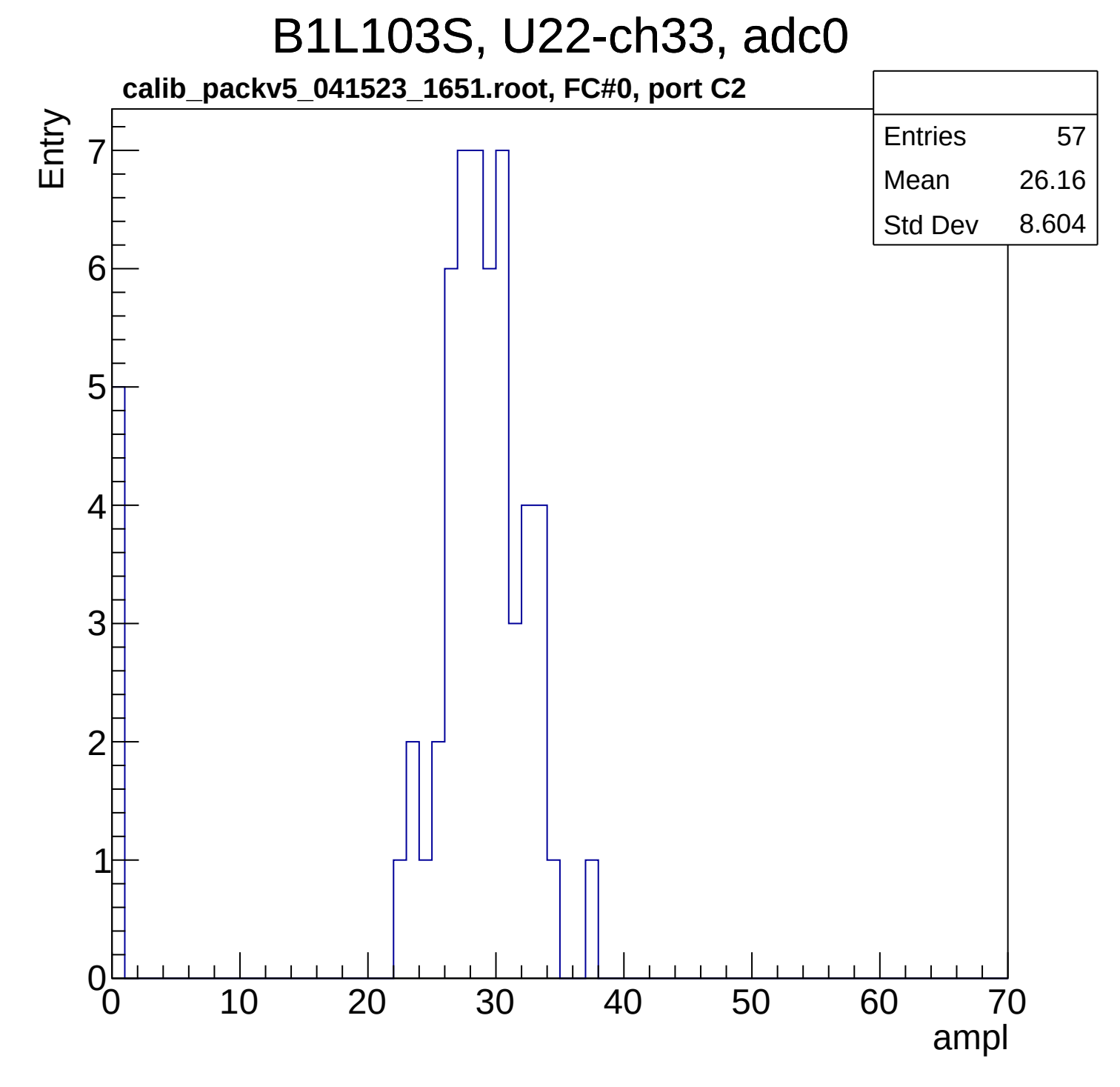
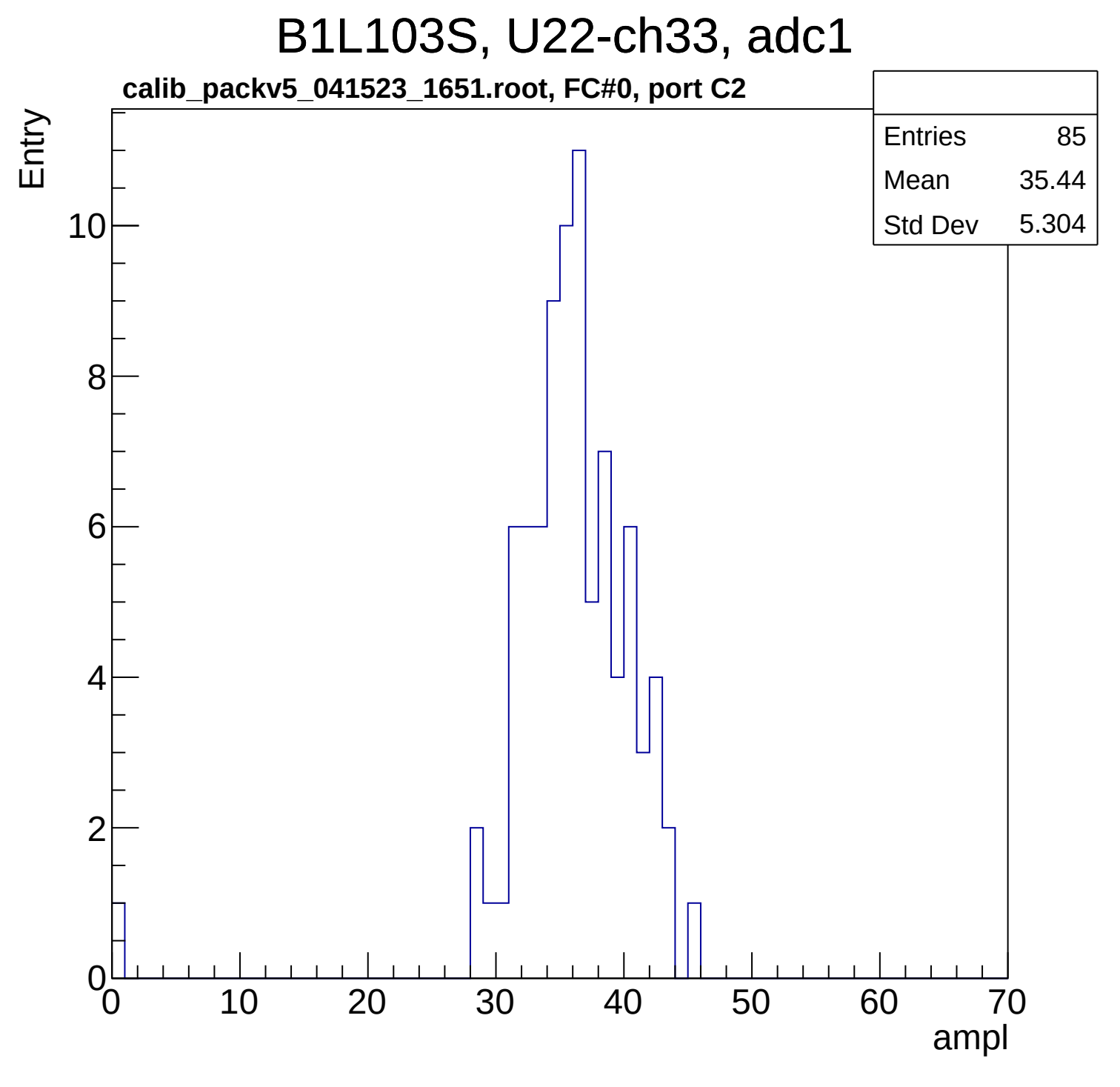
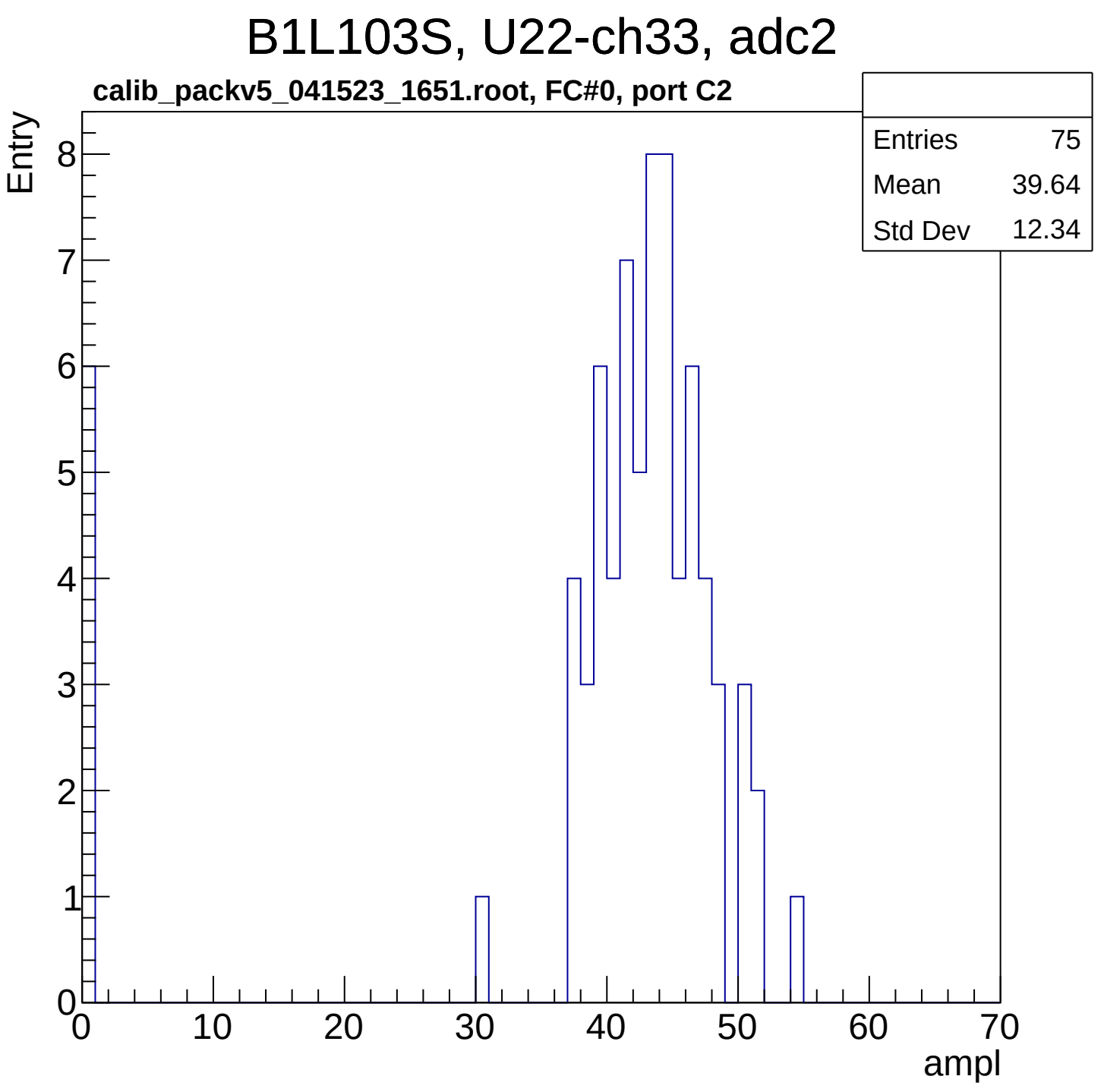
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U22-ch32, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch33, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 26.16
Std Dev 8.604
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U22-ch33, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 35.44
Std Dev 5.304
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch33, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 39.64
Std Dev 12.34
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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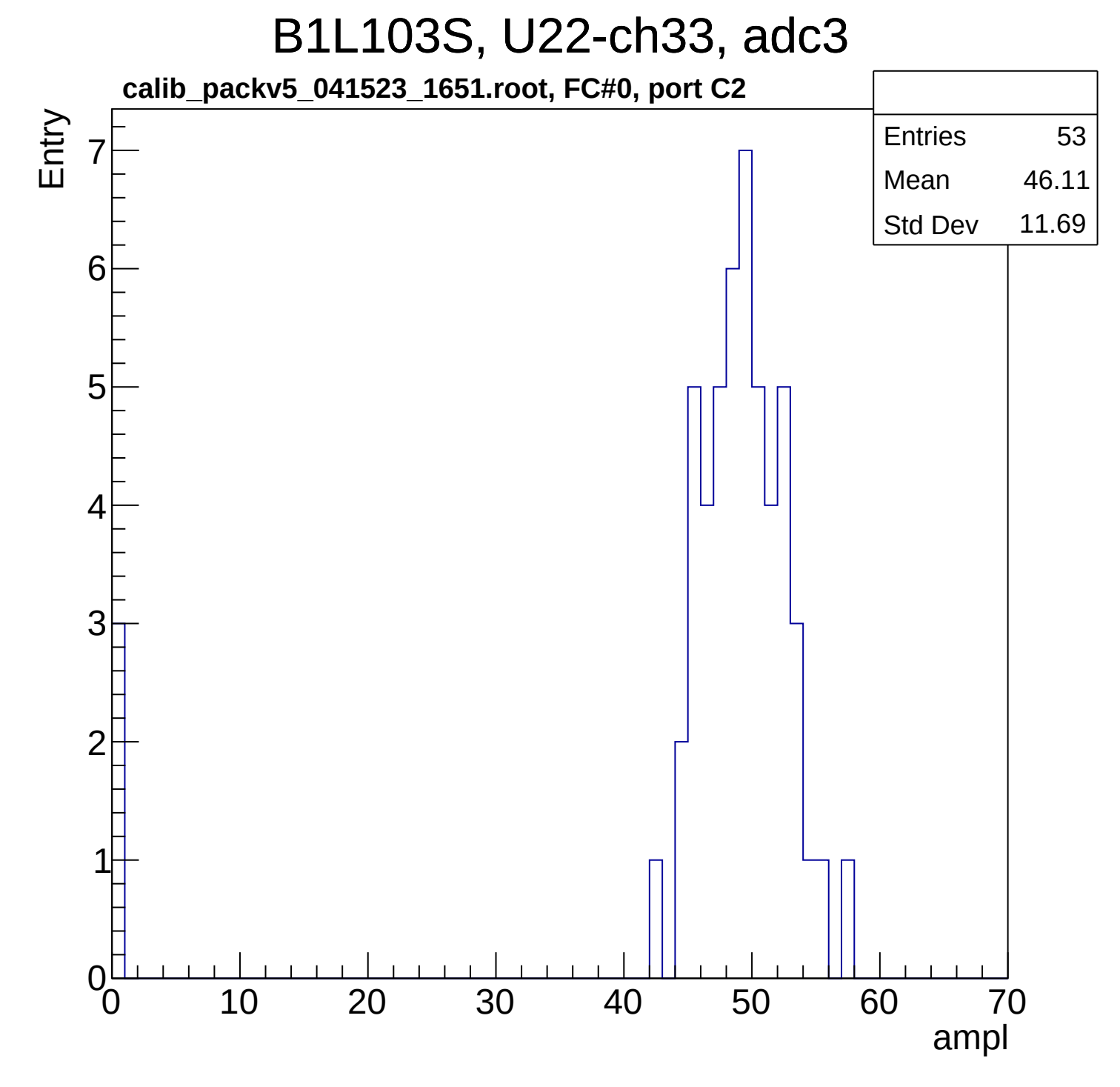
B1L103S, U22-ch33, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 46.11
Std Dev 11.69
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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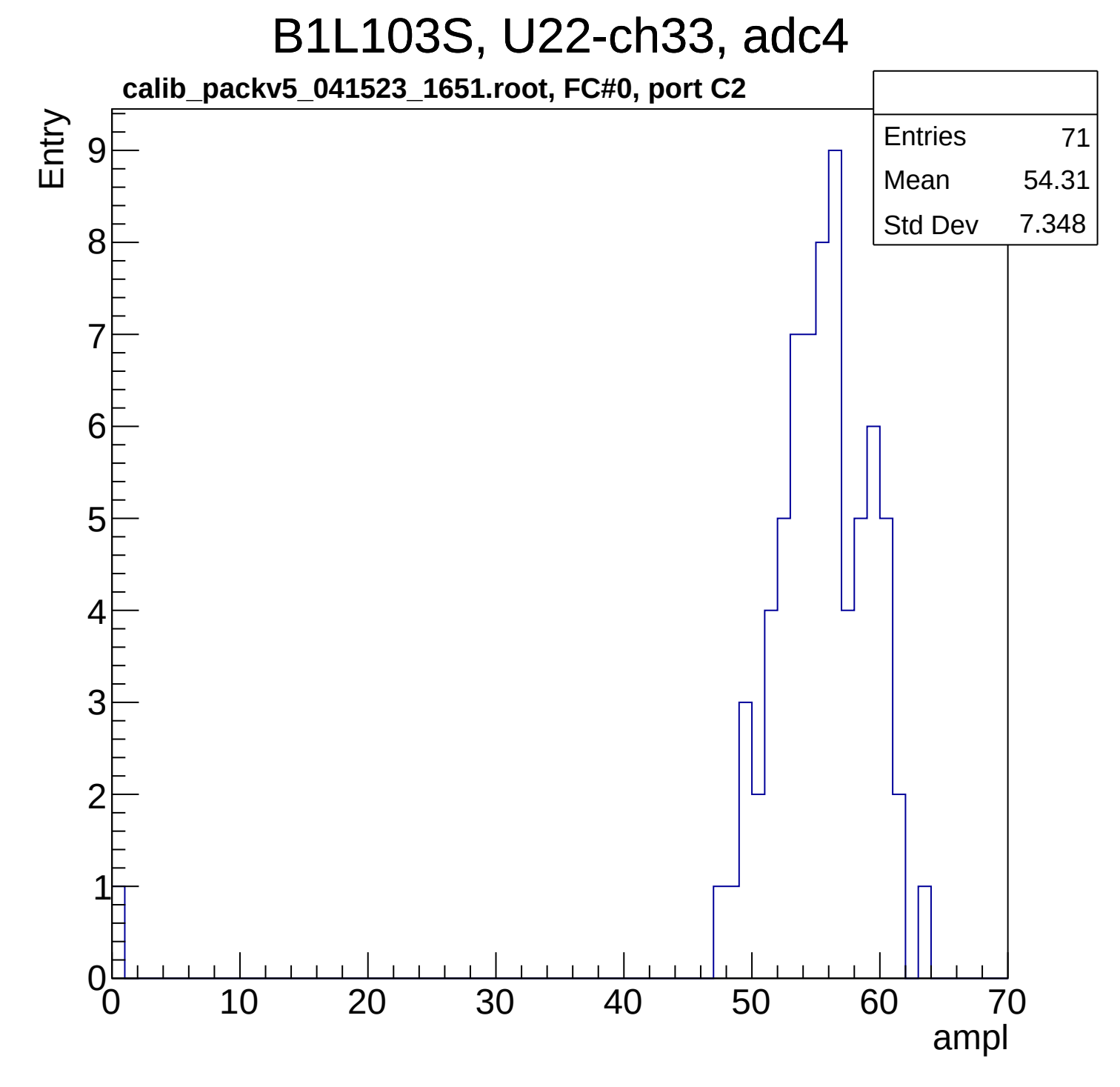
B1L103S, U22-ch33, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 54.31
Std Dev 7.348
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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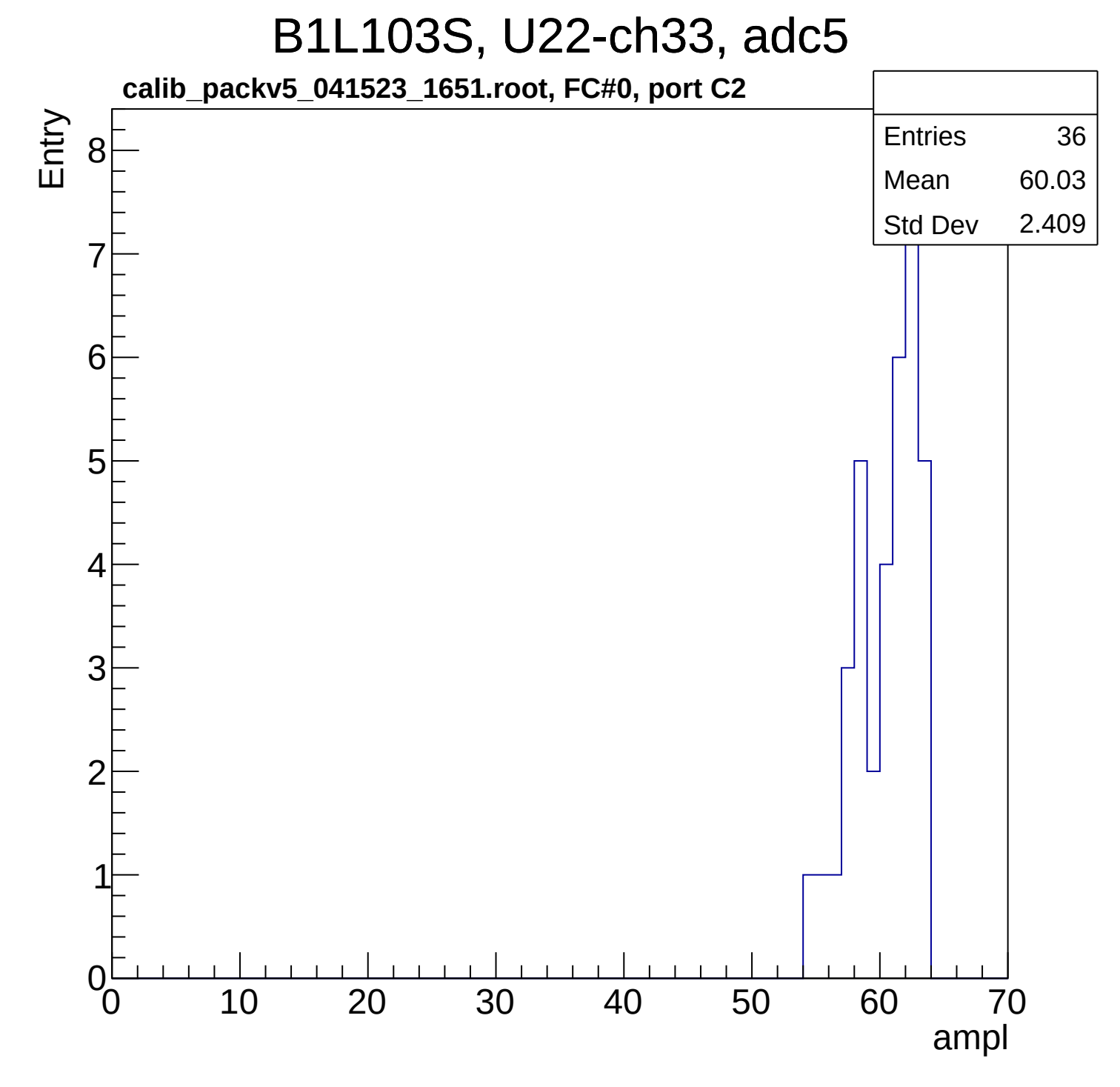
B1L103S, U22-ch33, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 60.03
Std Dev 2.409
Entry
ampl
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1
2
3
4
5
6
7
8
0
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40
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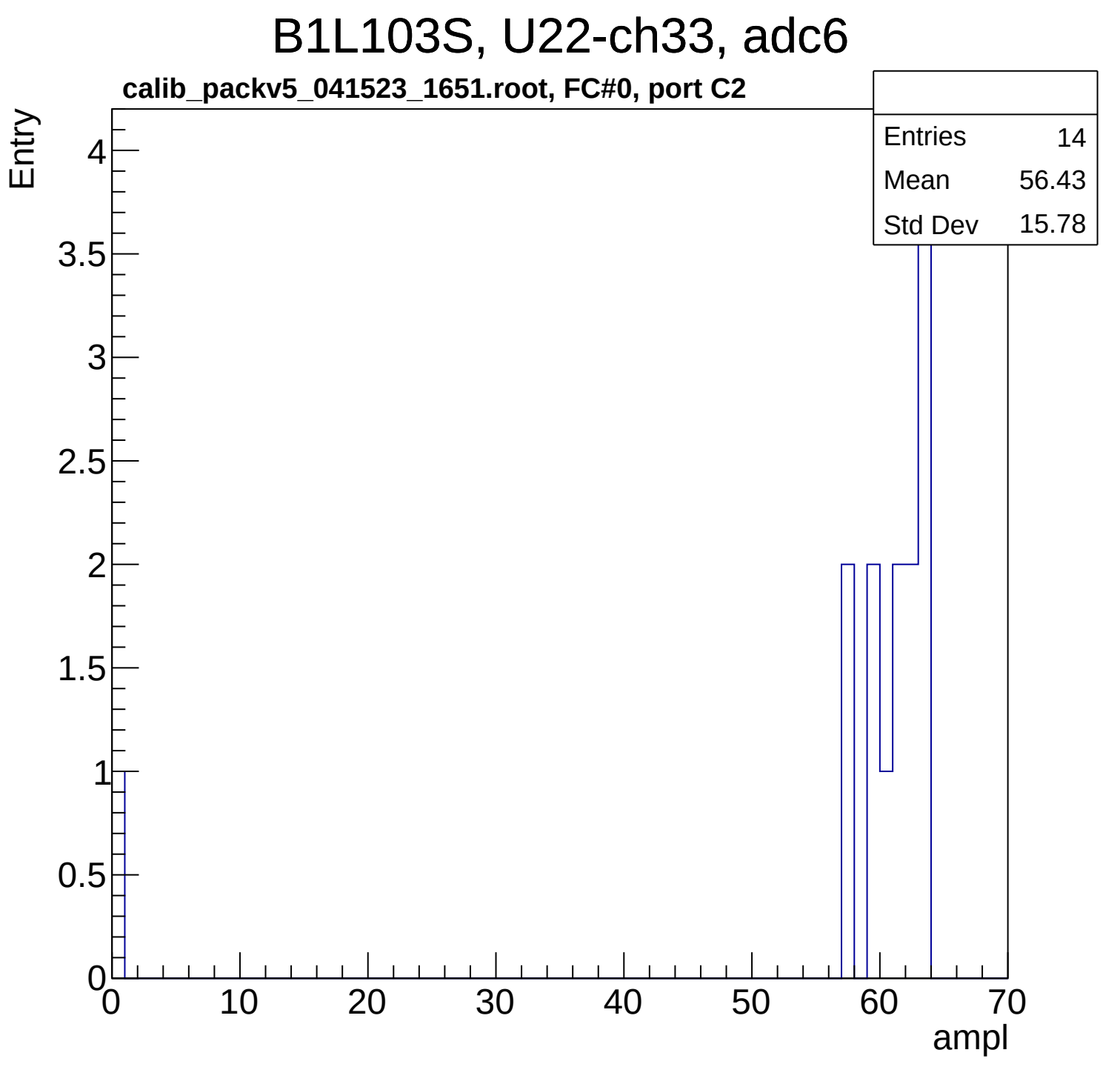
60
70


B1L103S, U22-ch33, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 56.43
Std Dev 15.78
Entry
ampl
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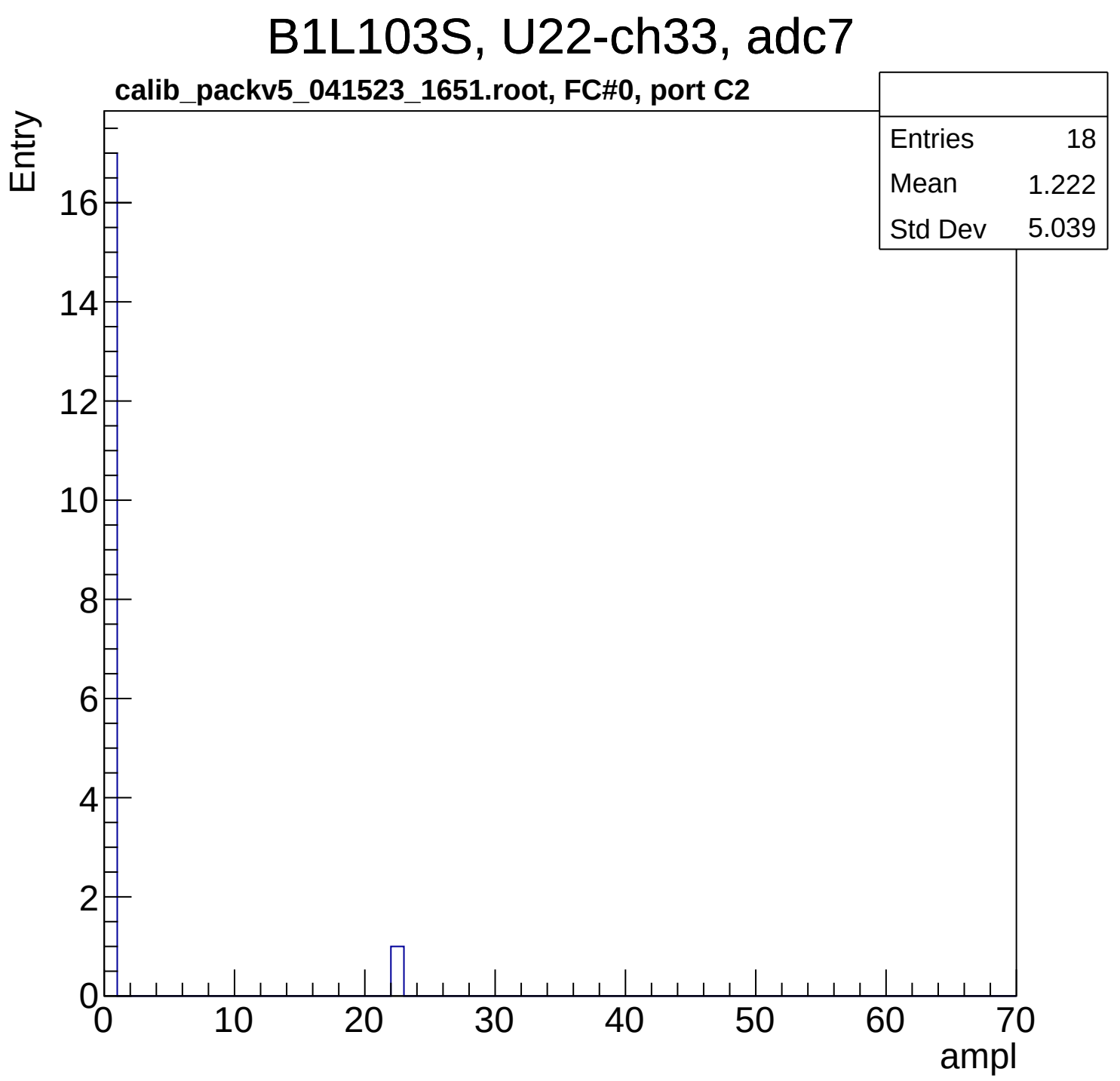
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U22-ch33, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.222
Std Dev 5.039
Entry
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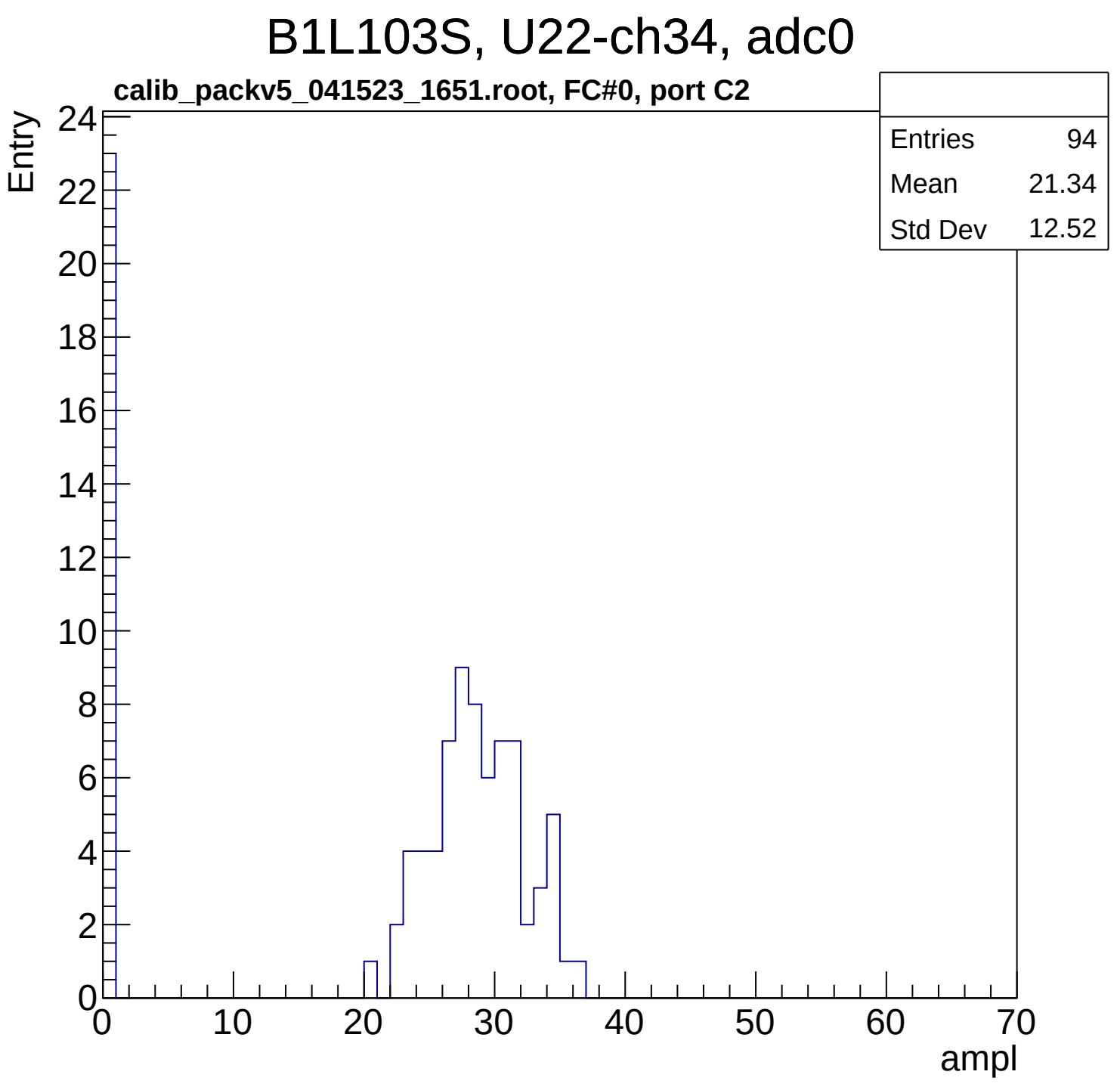
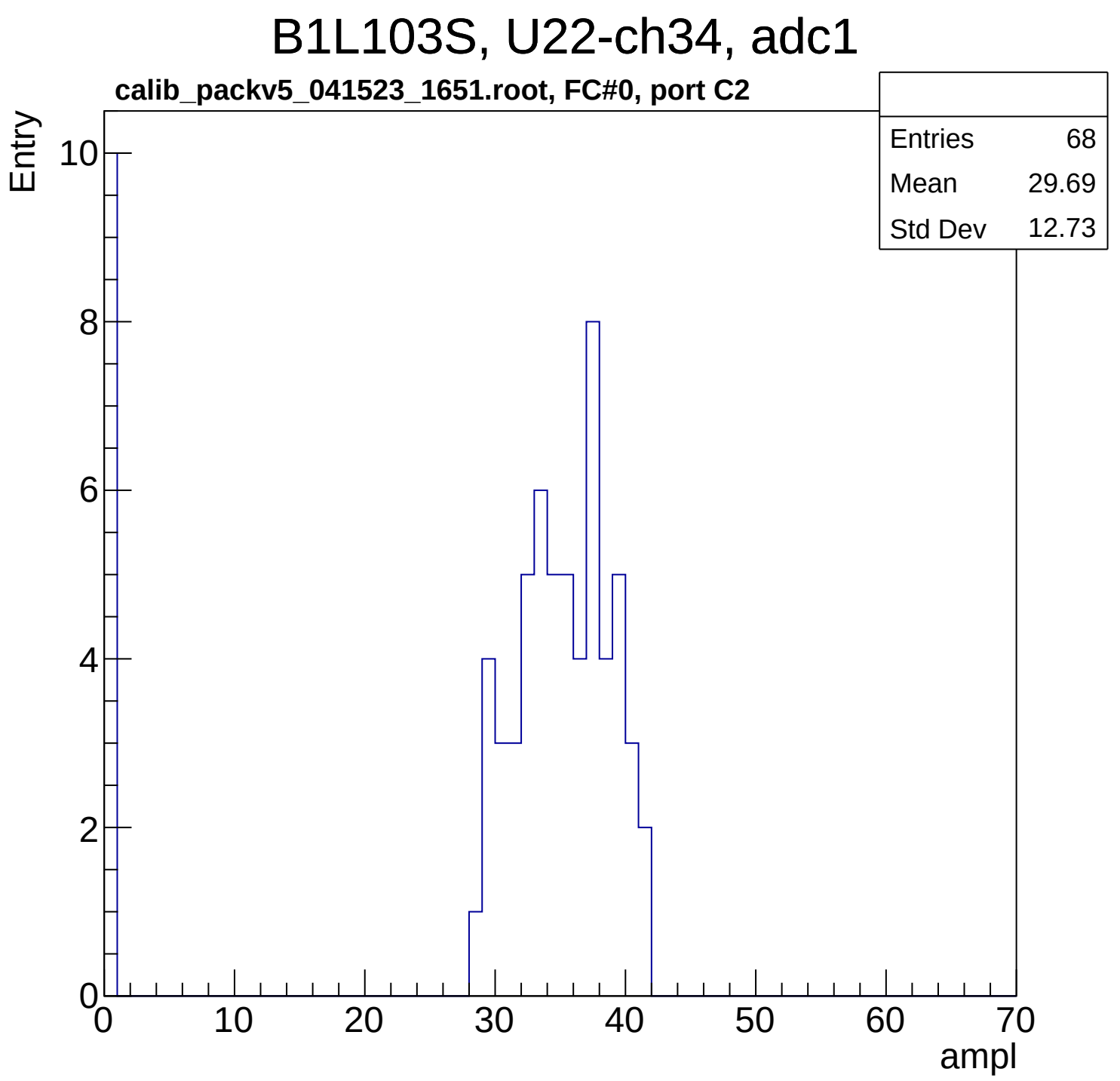
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch34, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 21.34
Std Dev 12.52
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
24
0
10
20
30
40
50
60
70


B1L103S, U22-ch34, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 29.69
Std Dev 12.73
Entry
ampl
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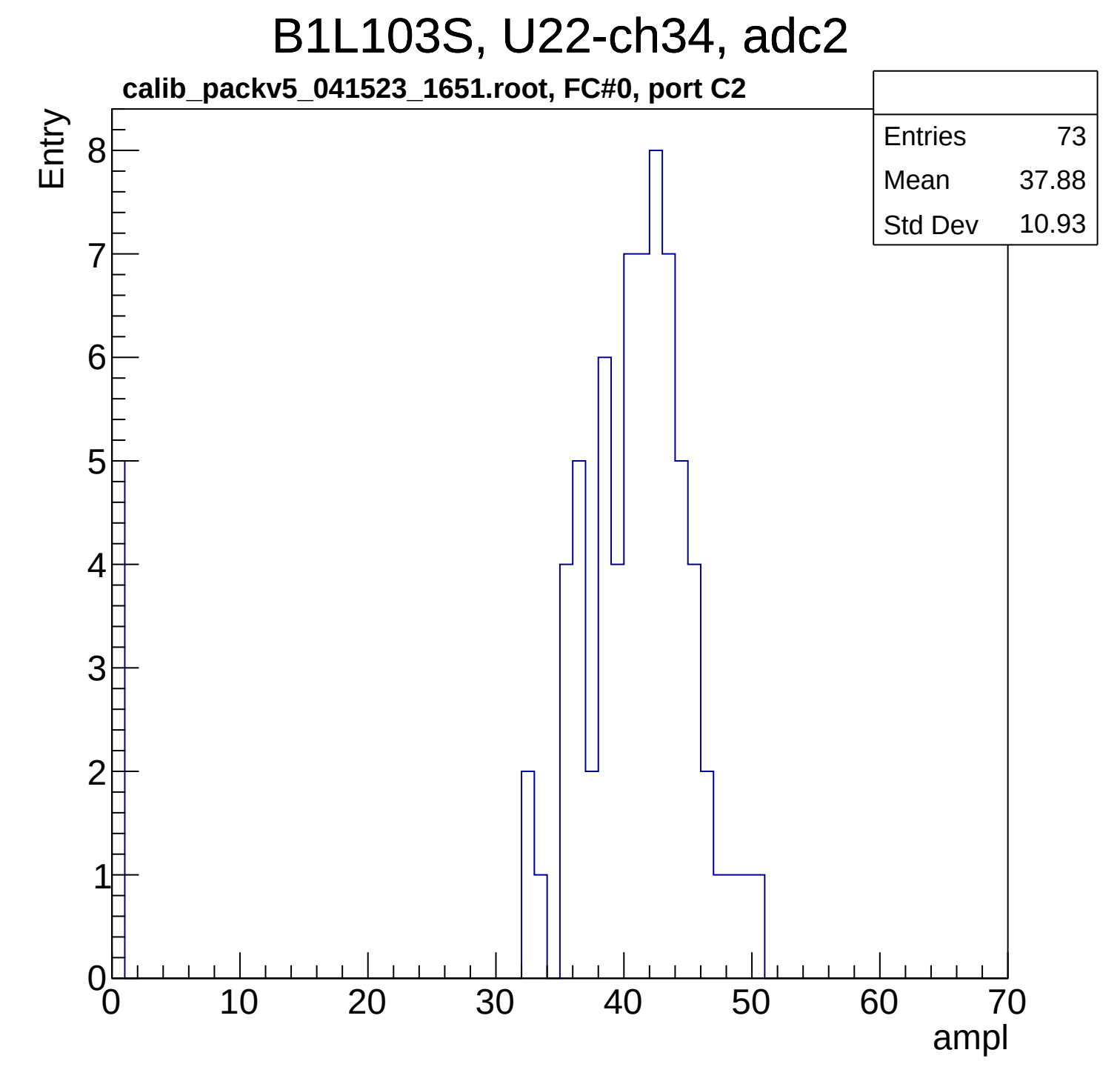
8
10
0
10
20
30
40
50
60
70


B1L103S, U22-ch34, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 37.88
Std Dev 10.93
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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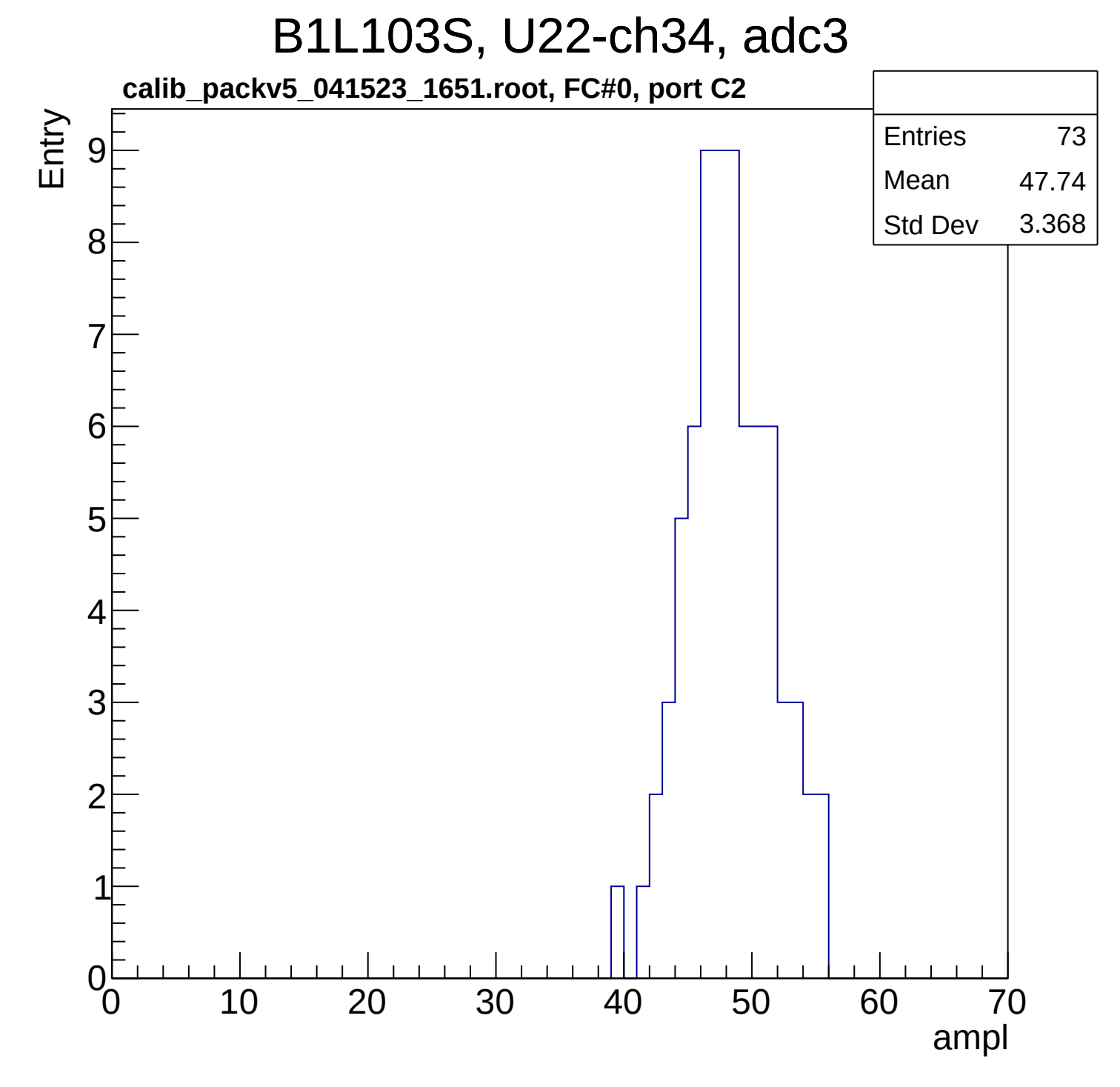
40
50
60
70


B1L103S, U22-ch34, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 47.74
Std Dev 3.368
Entry
ampl
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3
4
5
6
7
8
9
0
10
20
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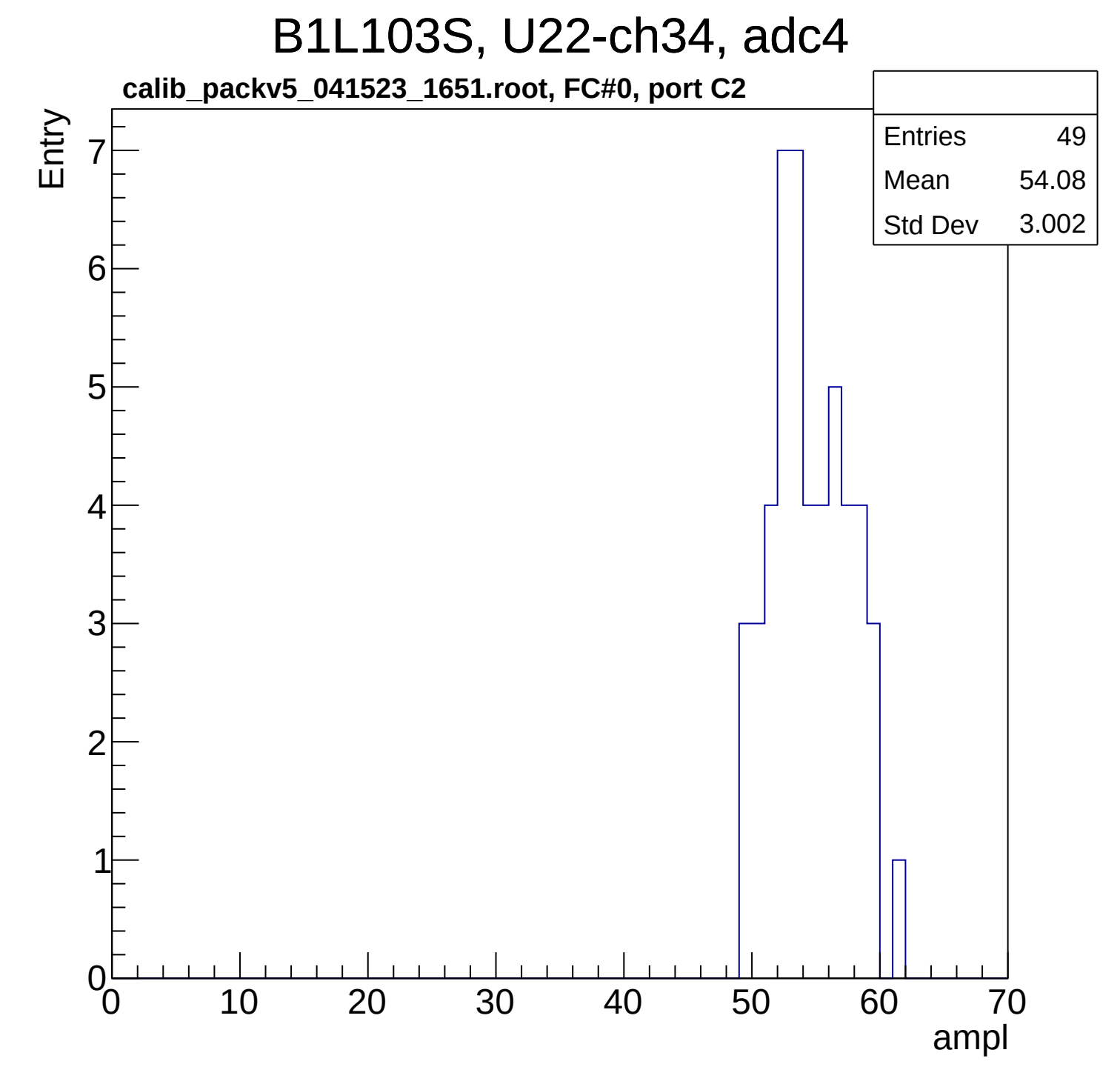
40
50
60
70


B1L103S, U22-ch34, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 54.08
Std Dev 3.002
Entry
ampl
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1
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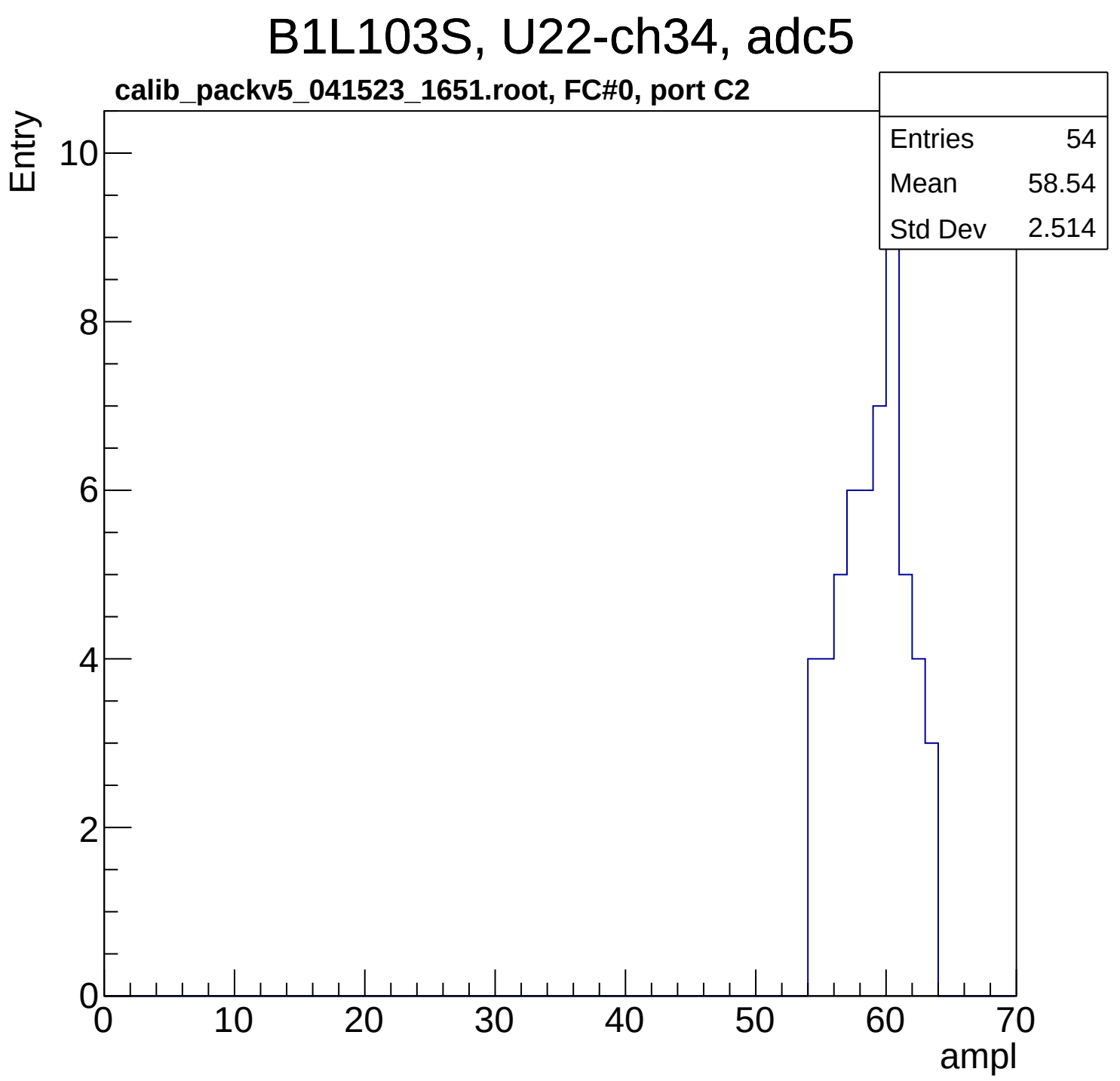
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U22-ch34, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 58.54
Std Dev 2.514
Entry
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4
6
8
10
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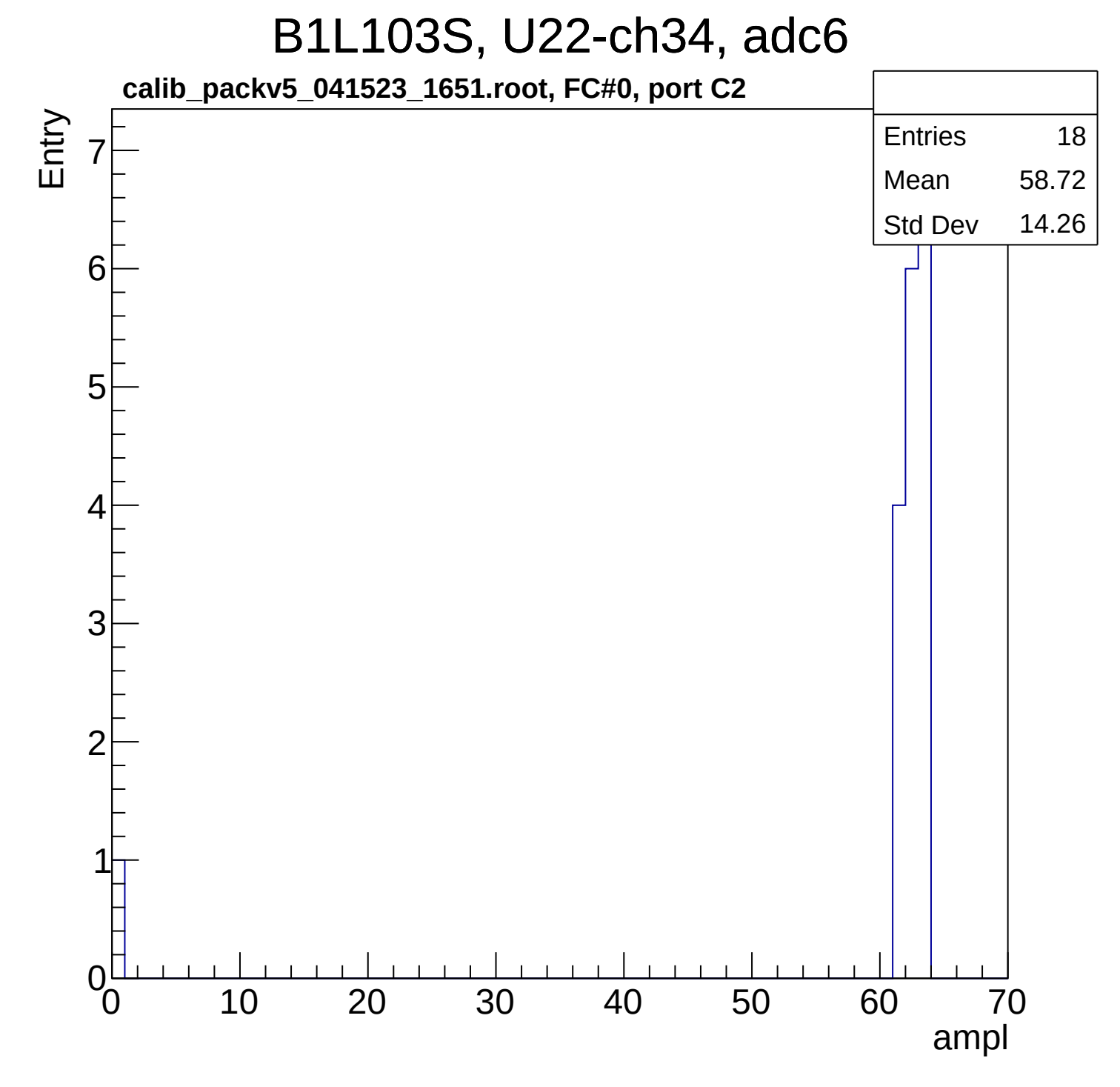
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch34, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 58.72
Std Dev 14.26
Entry
ampl
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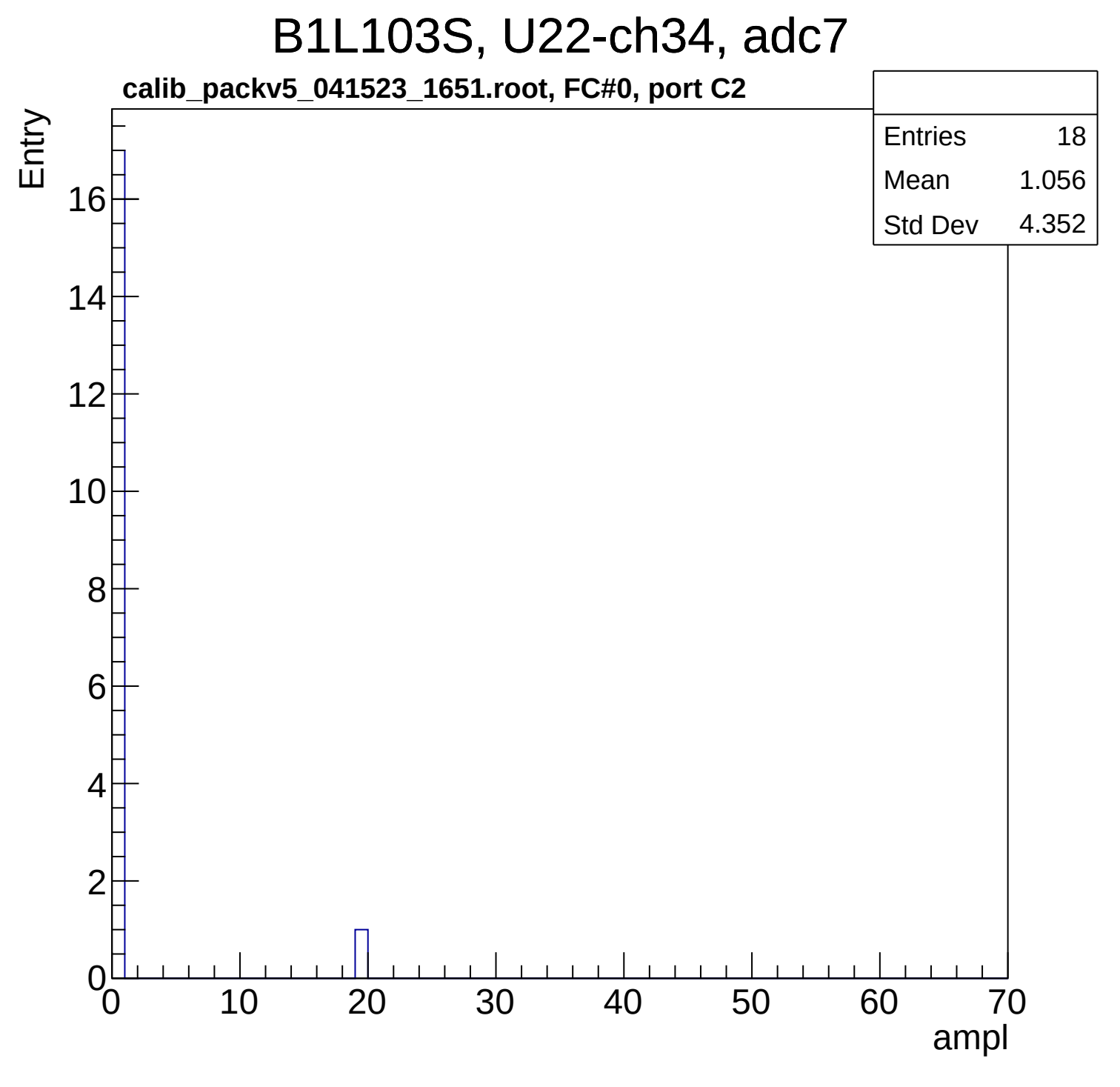
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U22-ch34, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.056
Std Dev 4.352
Entry
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6
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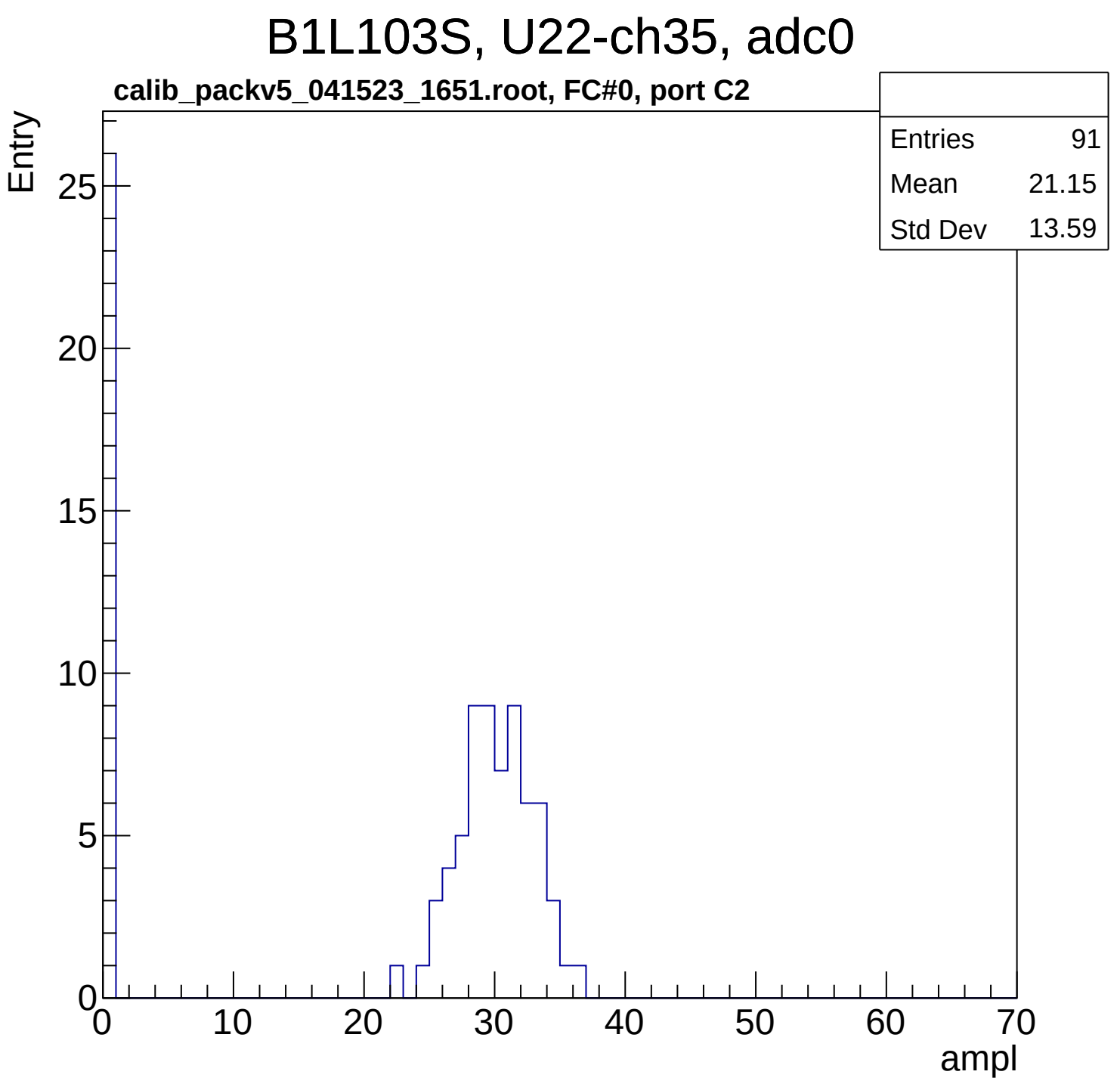
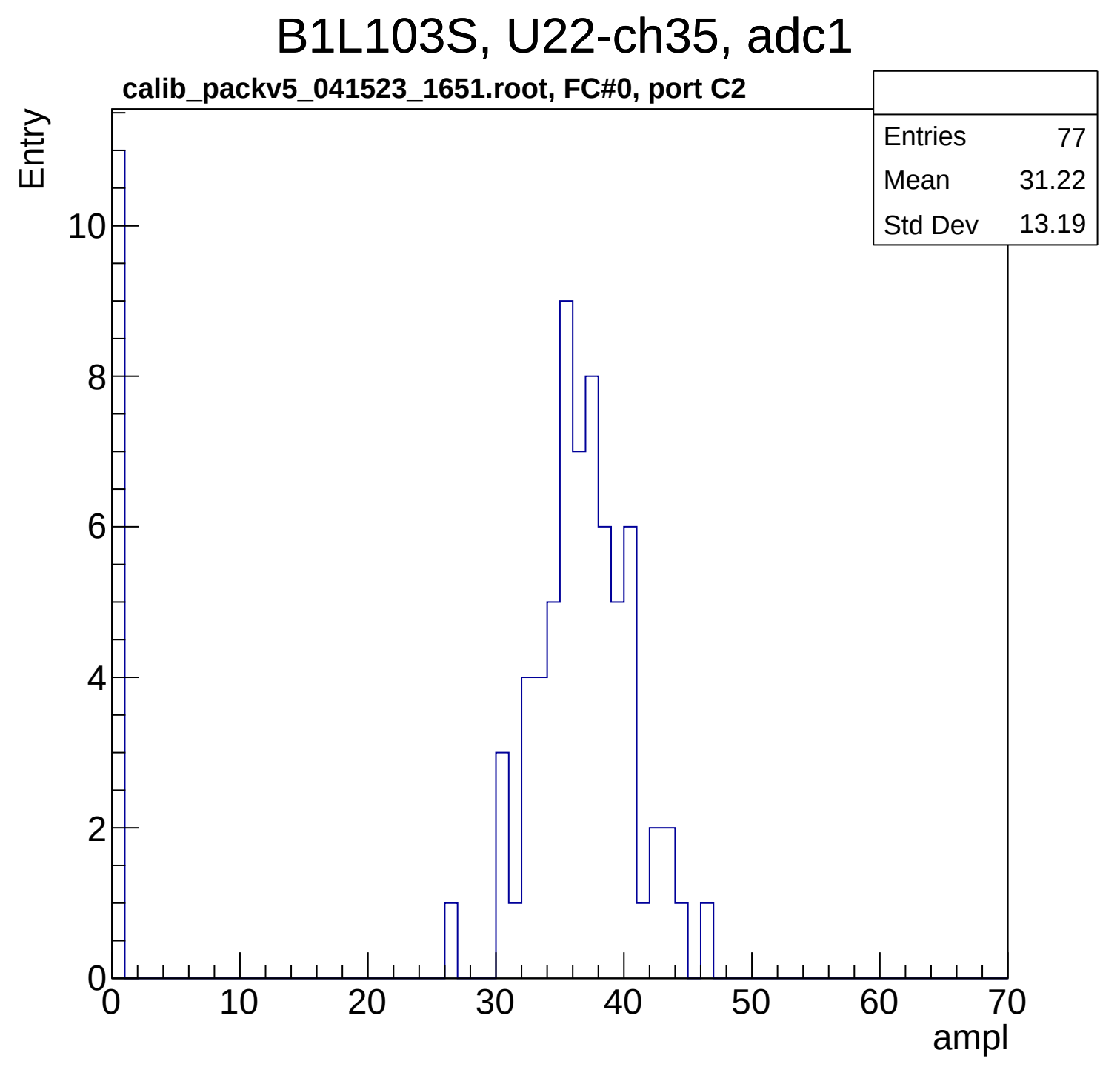
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch35, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 21.15
Std Dev 13.59
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch35, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 31.22
Std Dev 13.19
Entry
0
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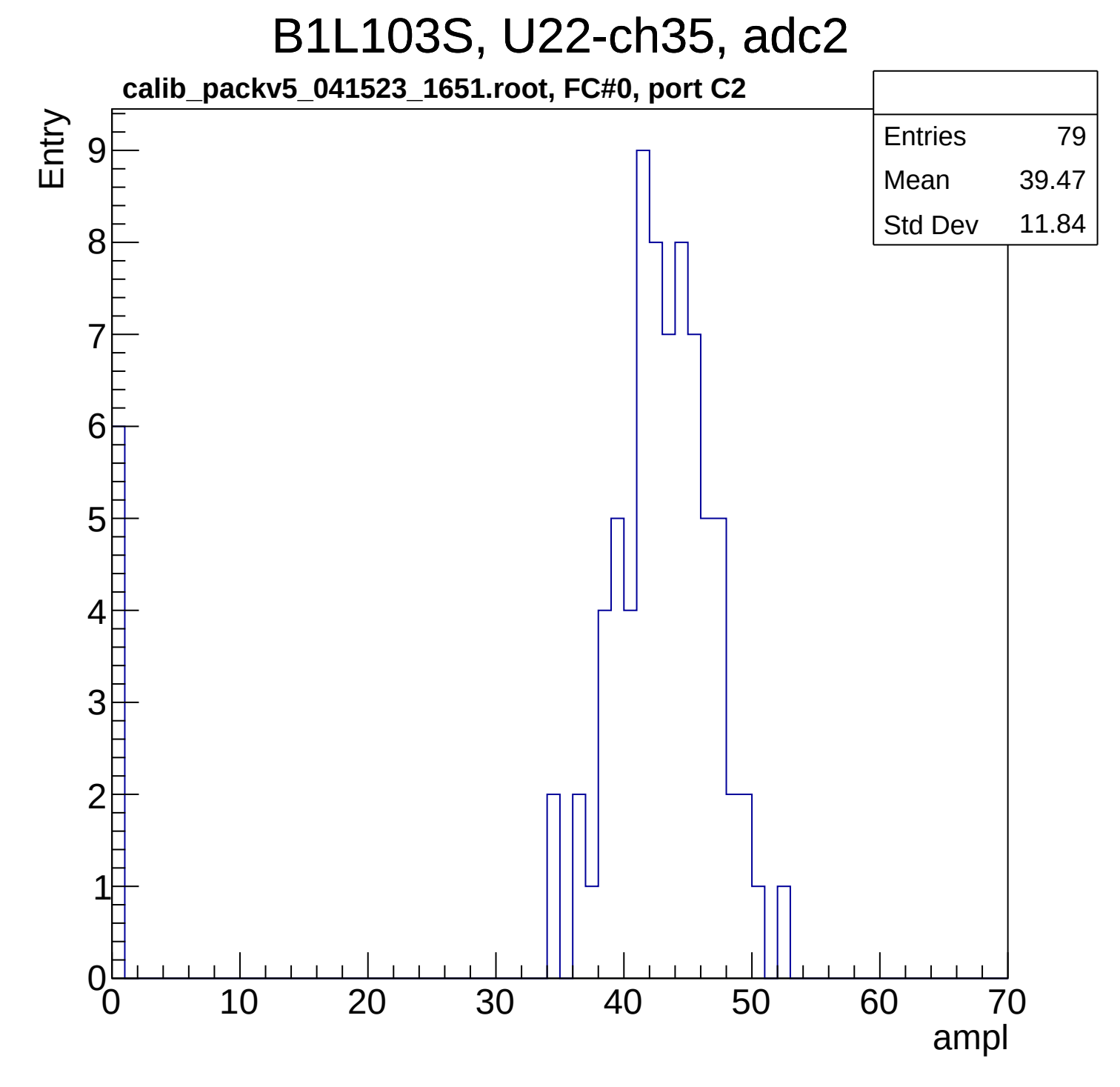
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch35, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 39.47
Std Dev 11.84
Entry
ampl
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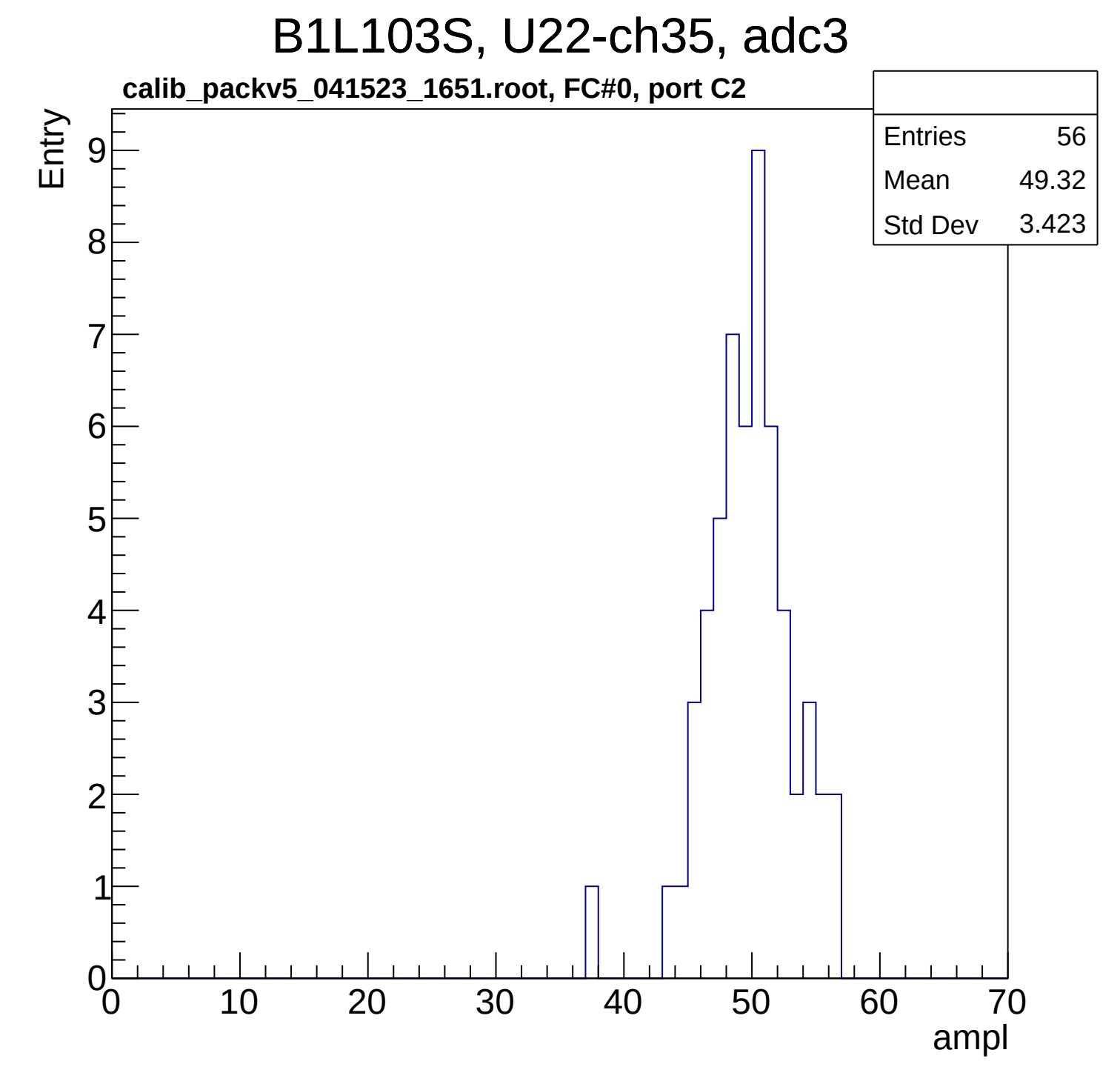
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch35, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 49.32
Std Dev 3.423
Entry
ampl
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4
5
6
7
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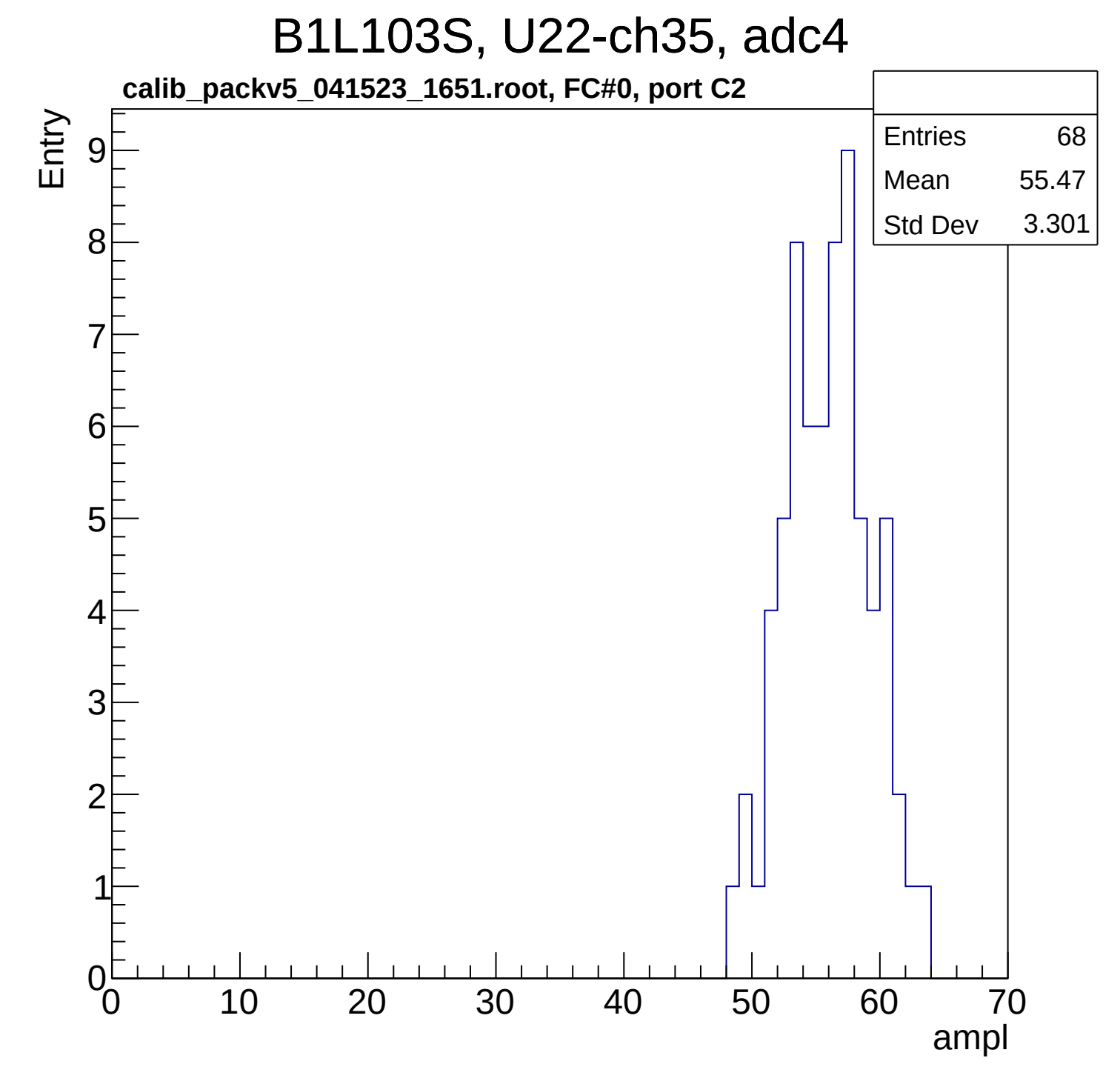
B1L103S, U22-ch35, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 55.47
Std Dev 3.301
Entry
ampl
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2
3
4
5
6
7
8
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0
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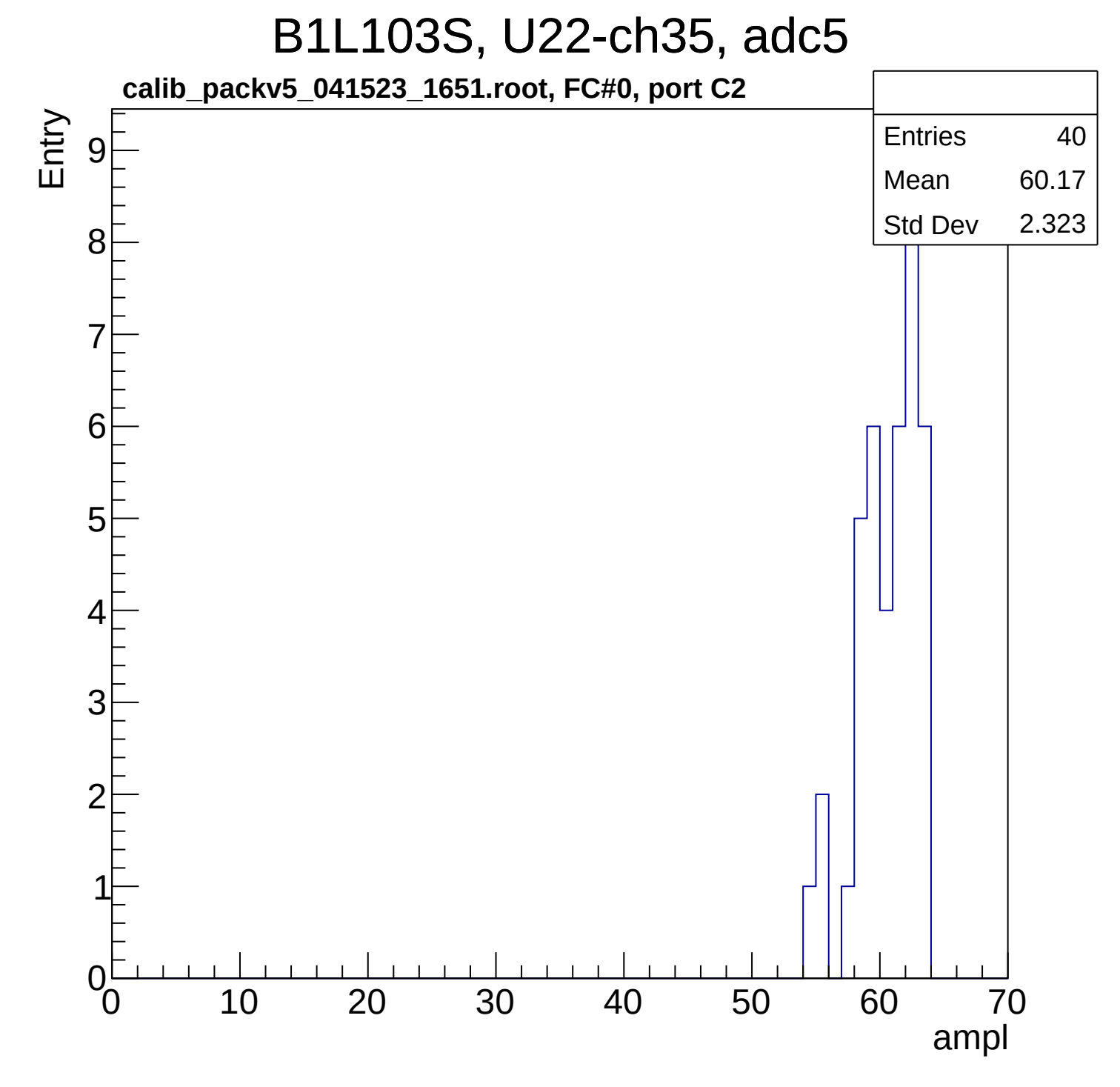
50
60
70


B1L103S, U22-ch35, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 60.17
Std Dev 2.323
Entry
ampl
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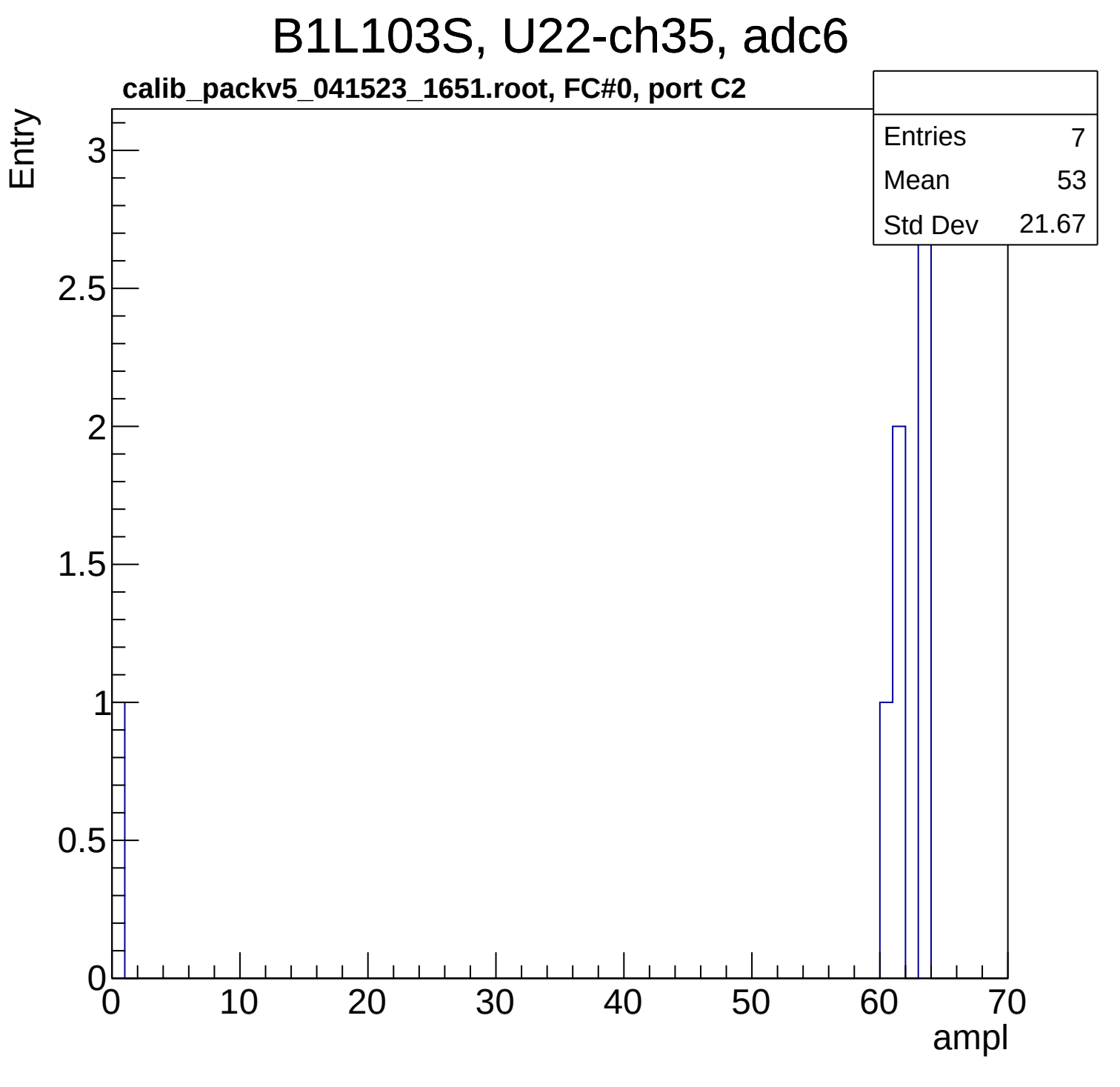
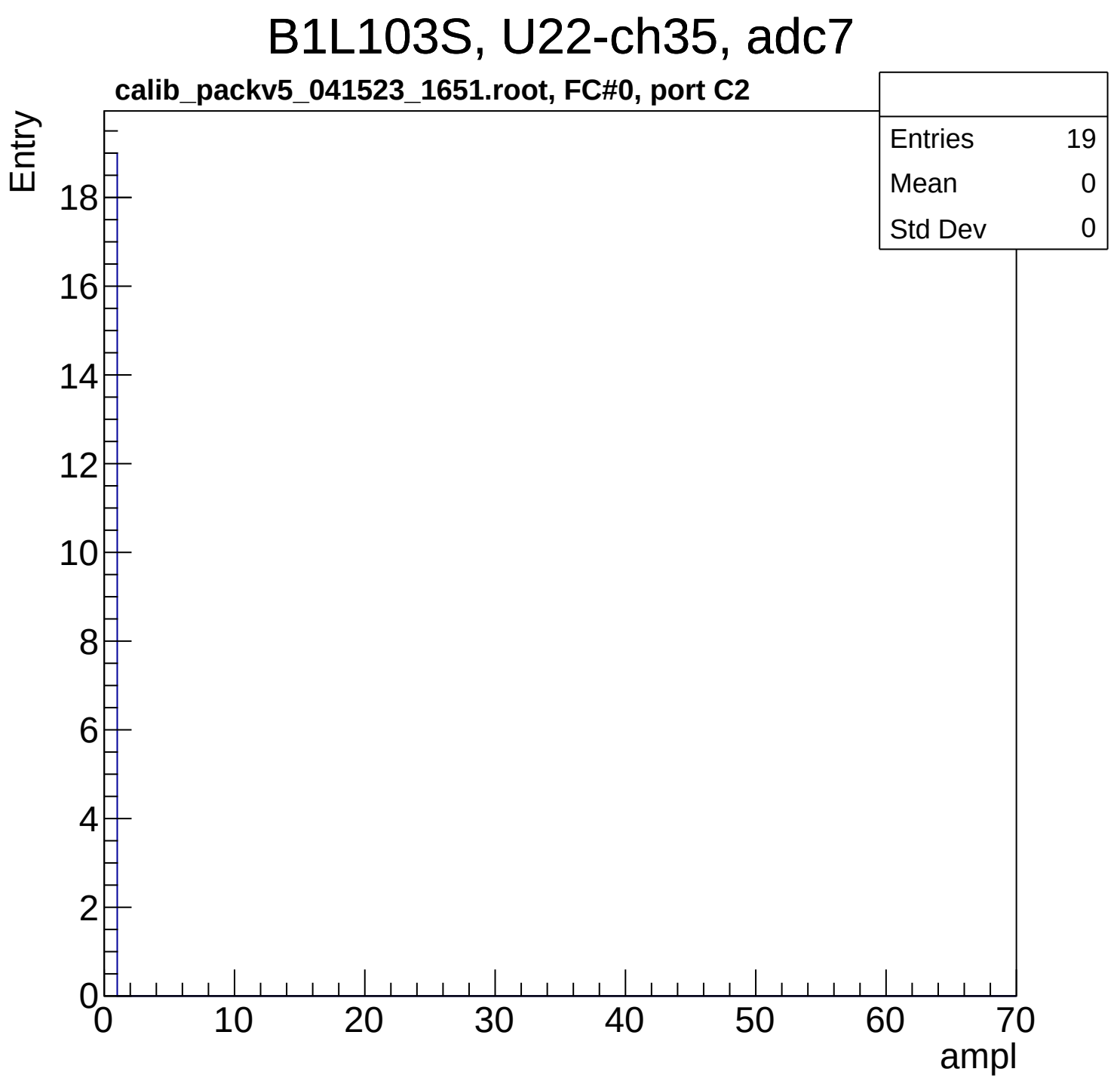
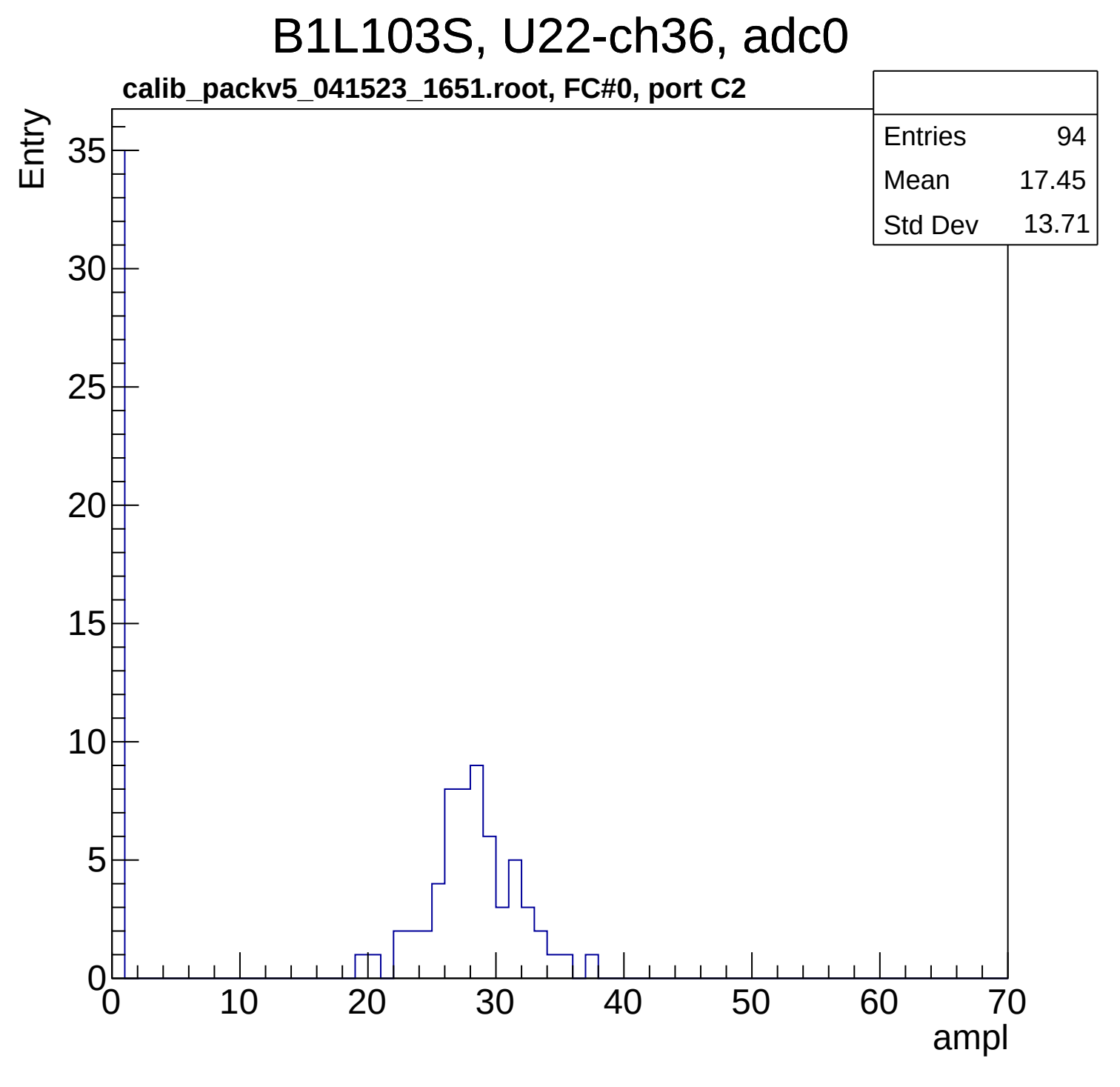
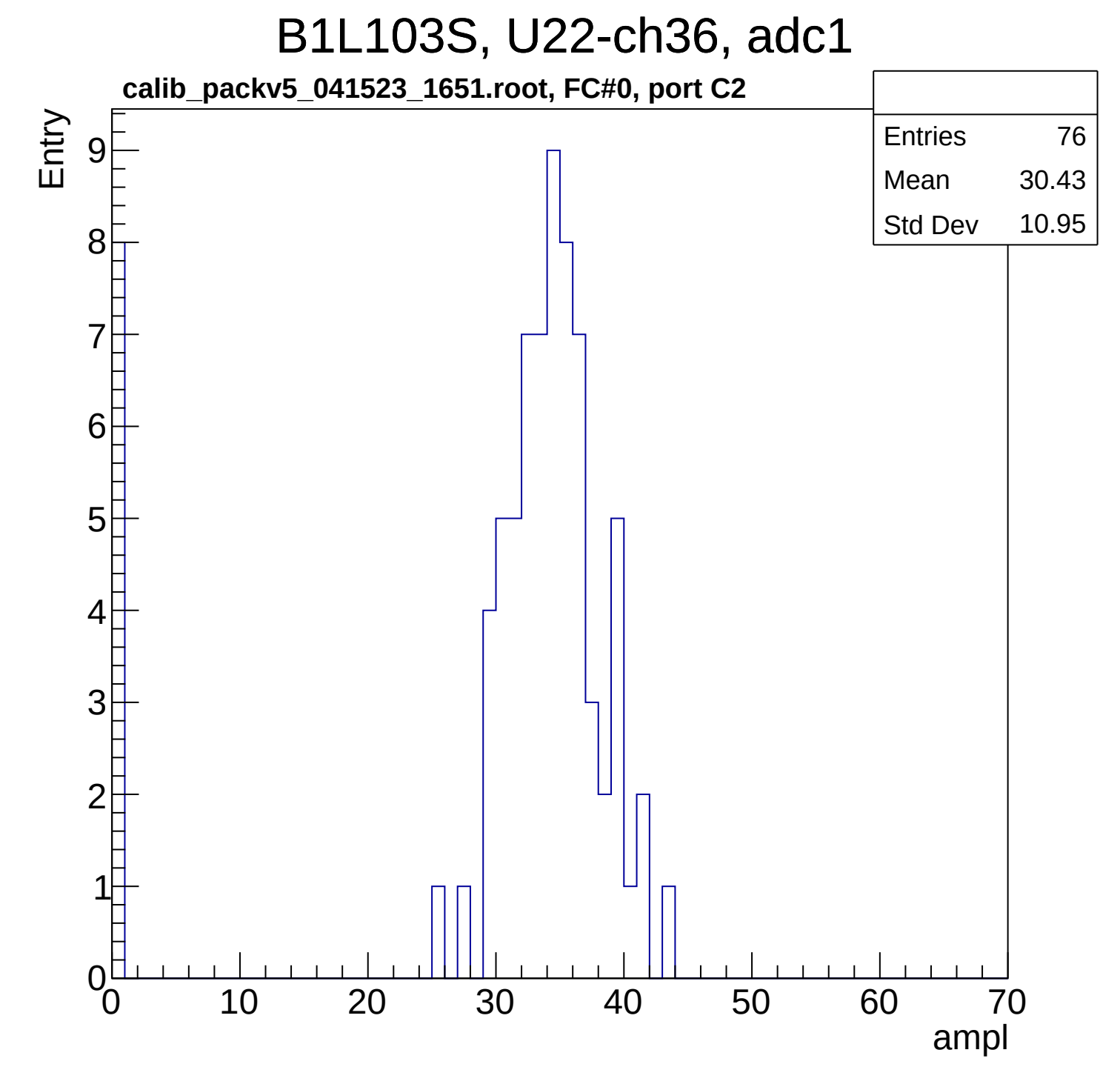
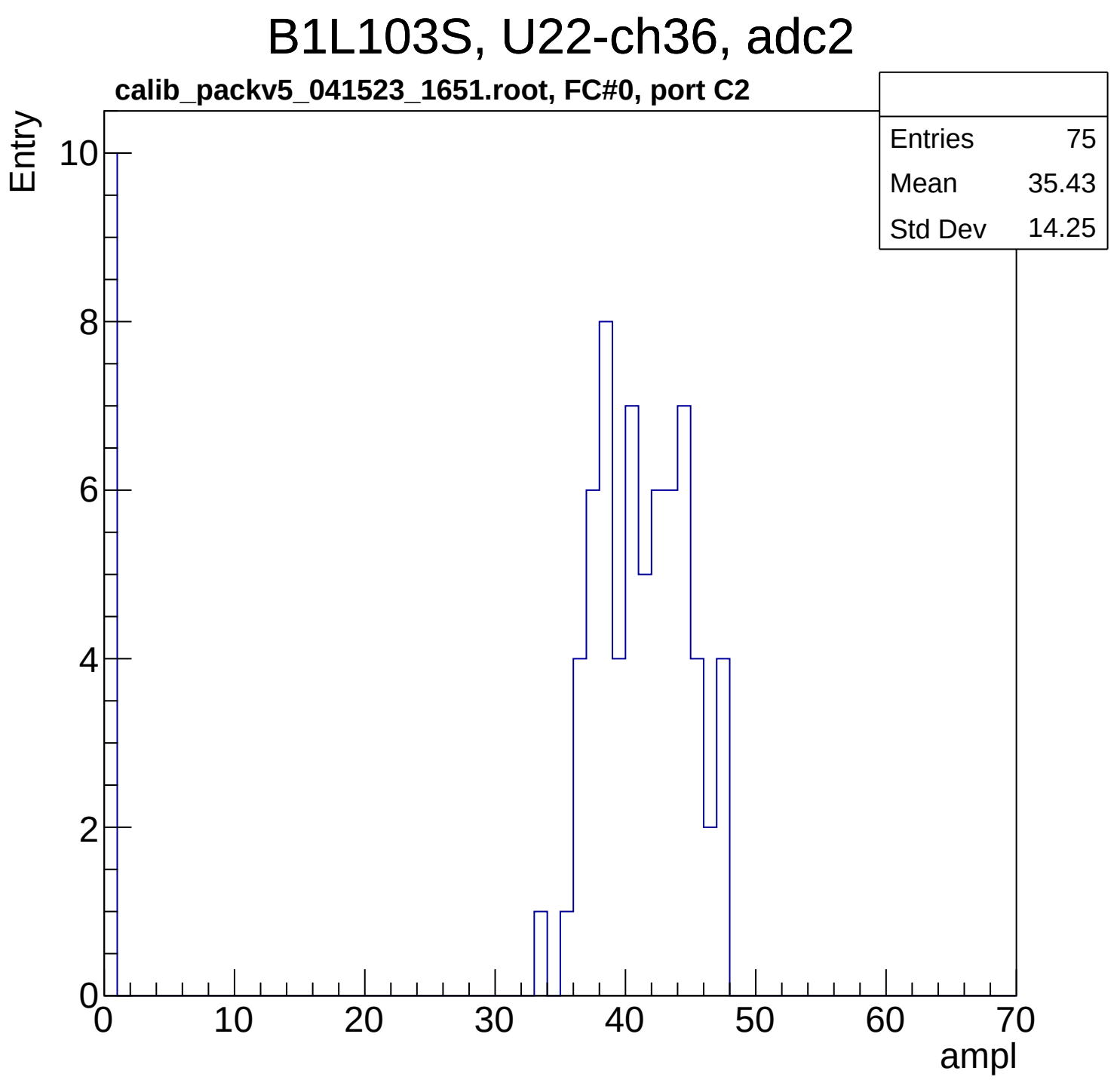
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

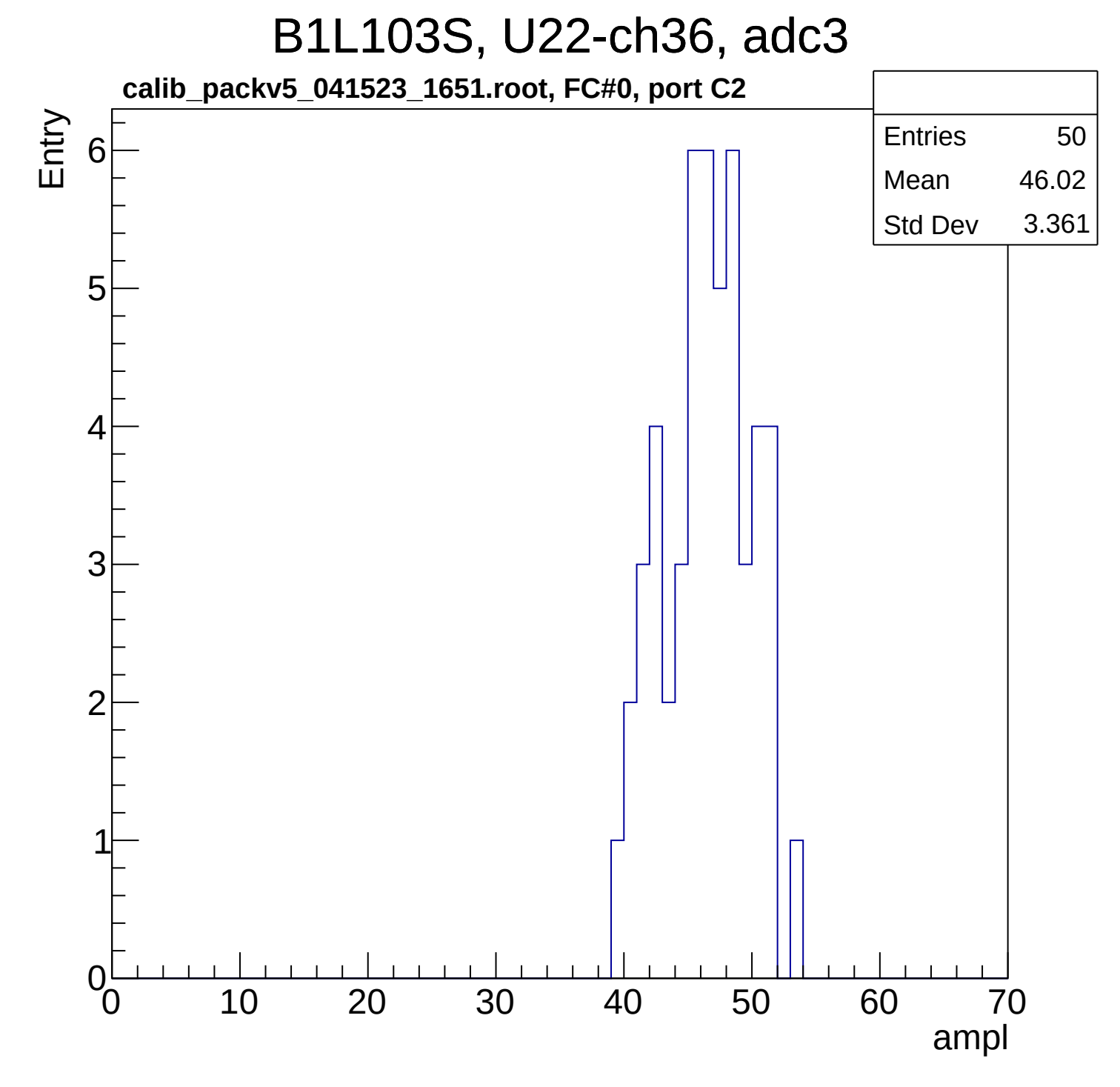

B1L103S, U22-ch35, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 53
Std Dev 21.67
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

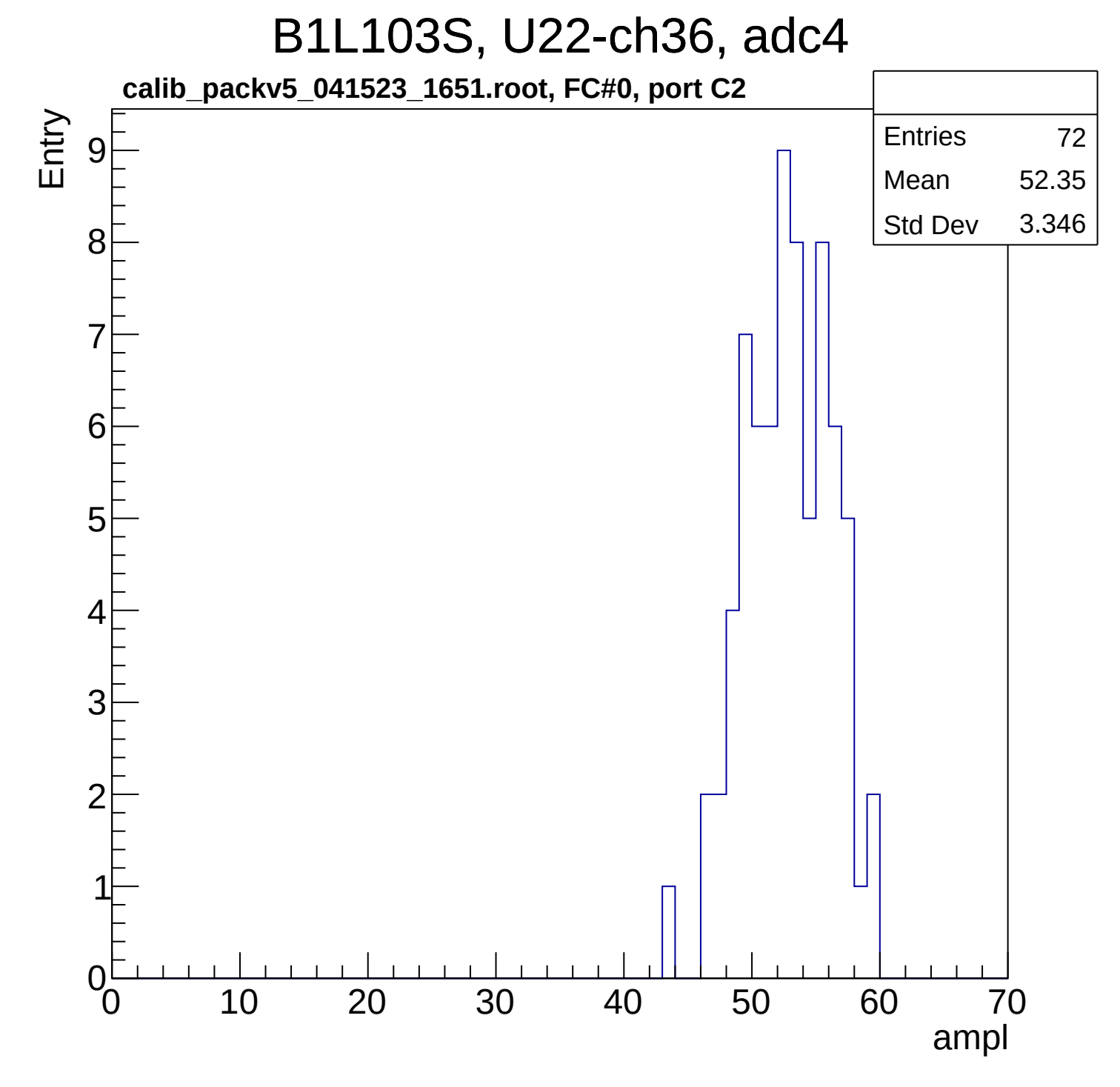

B1L103S, U22-ch35, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

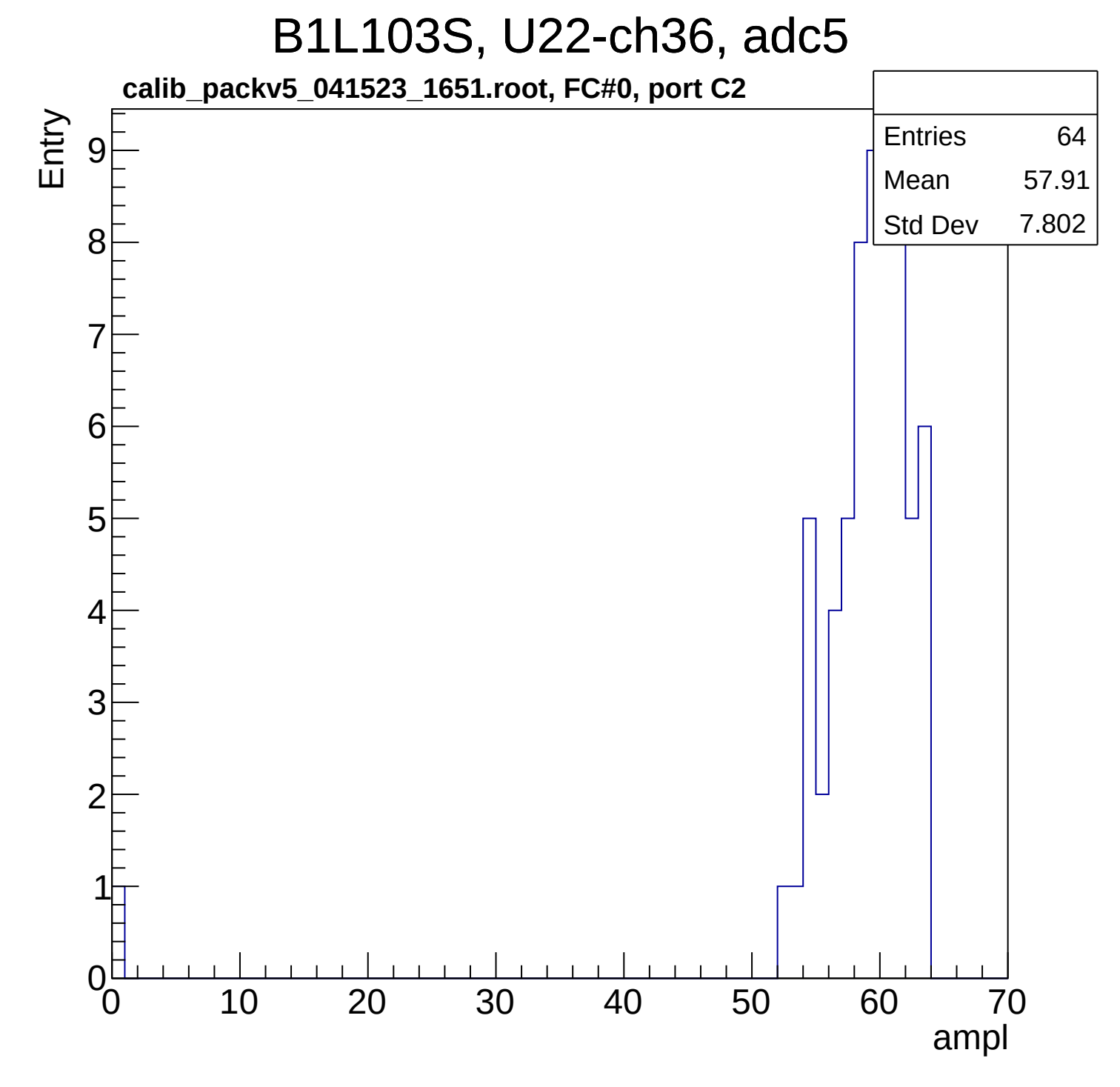

B1L103S, U22-ch36, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 17.45
Std Dev 13.71
Entry
ampl
0
5
10
15
20
25
30
35
0
10
20
30
40
50
60
70


B1L103S, U22-ch36, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 30.43
Std Dev 10.95
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch36, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 35.43
Std Dev 14.25
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U22-ch36, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 46.02
Std Dev 3.361
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U22-ch36, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 52.35
Std Dev 3.346
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch36, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 57.91
Std Dev 7.802
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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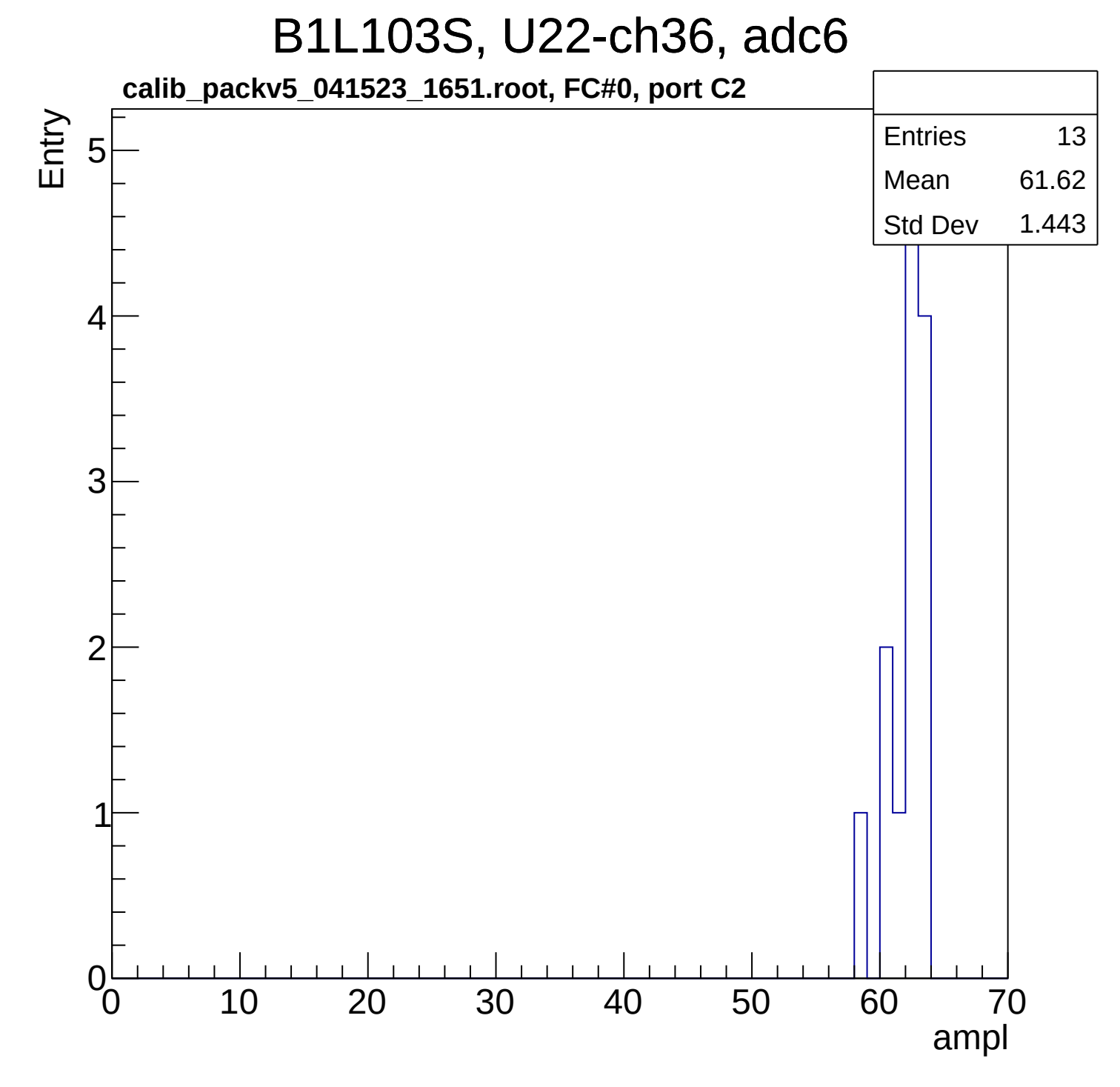
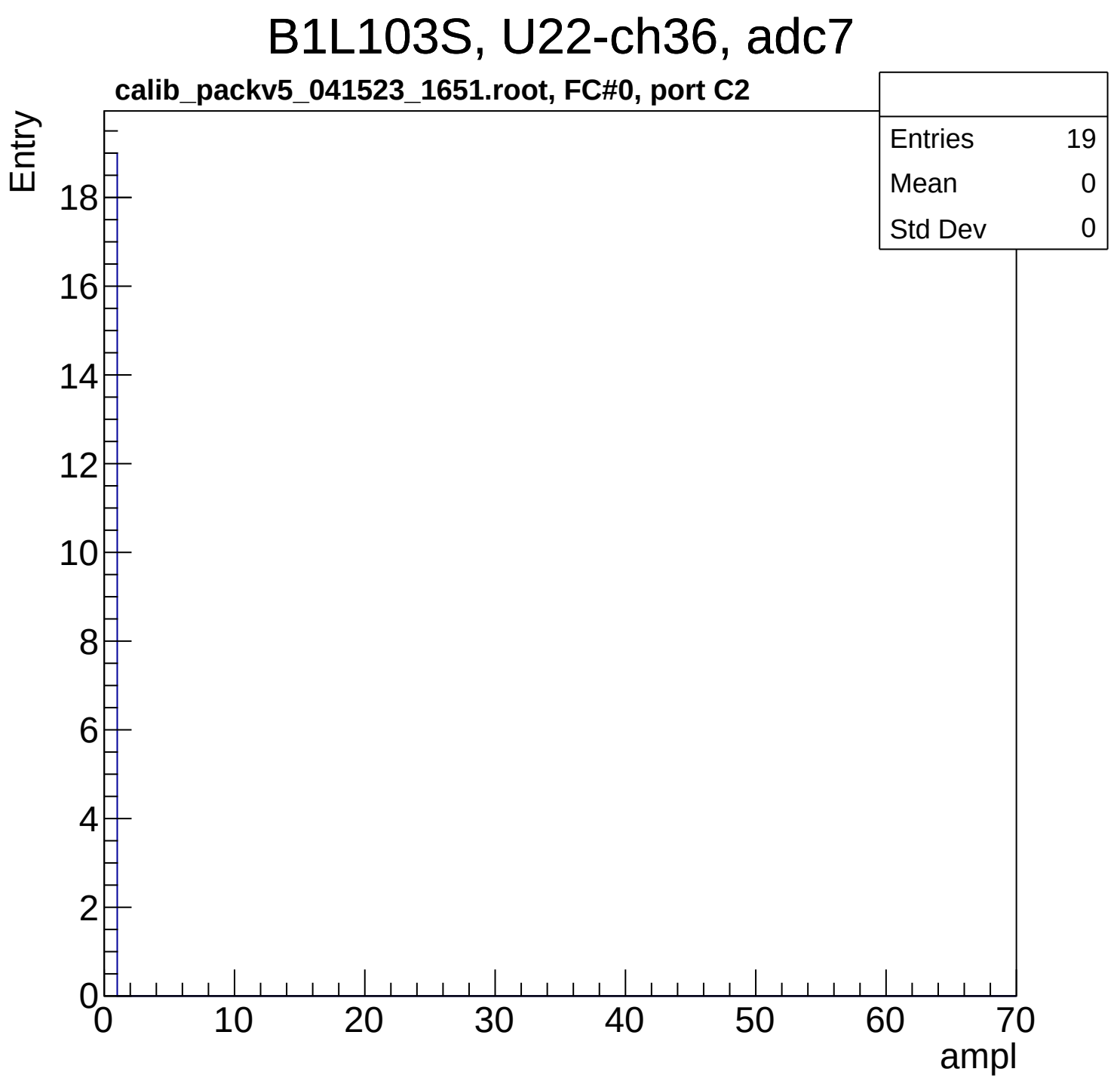
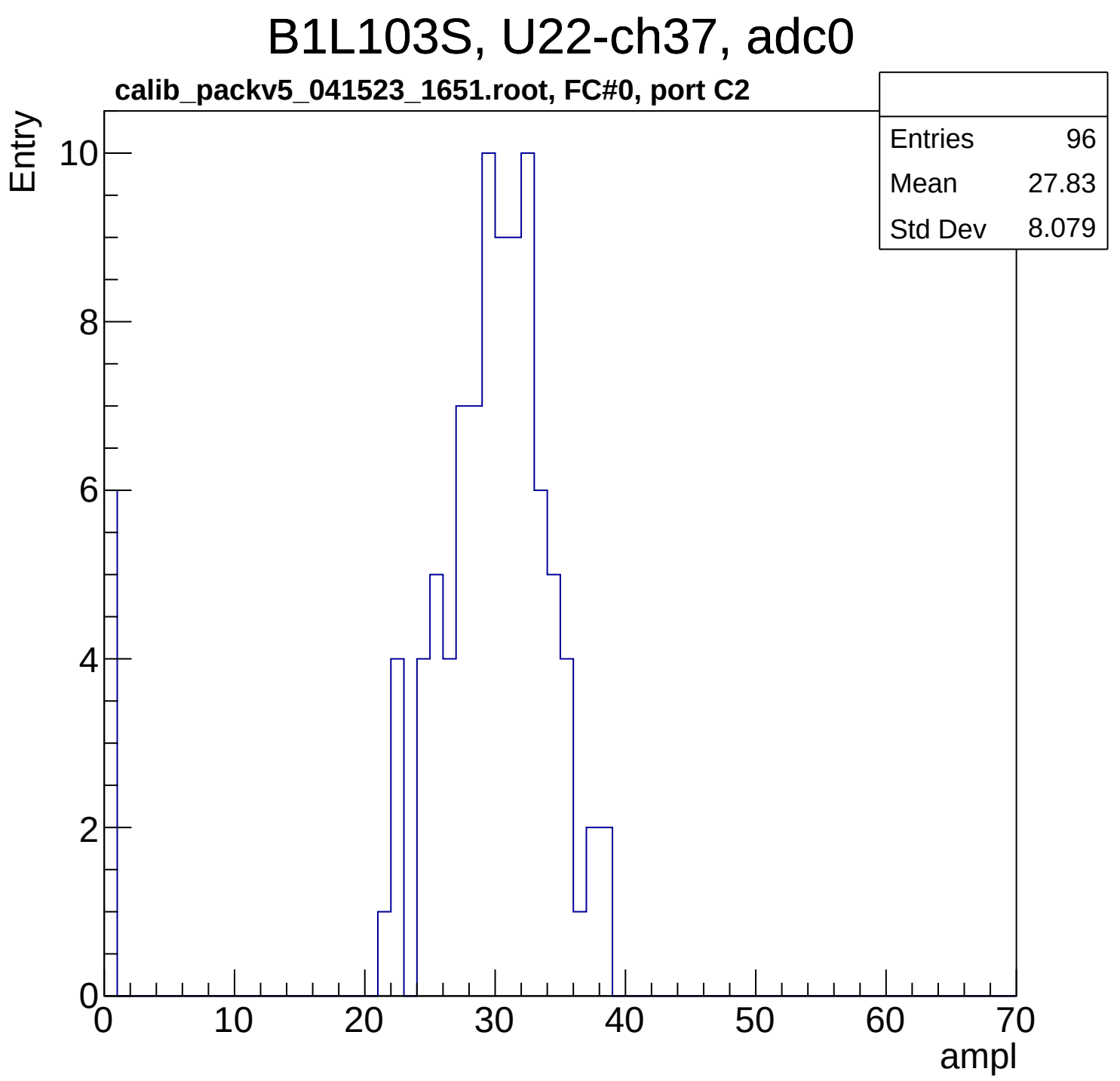
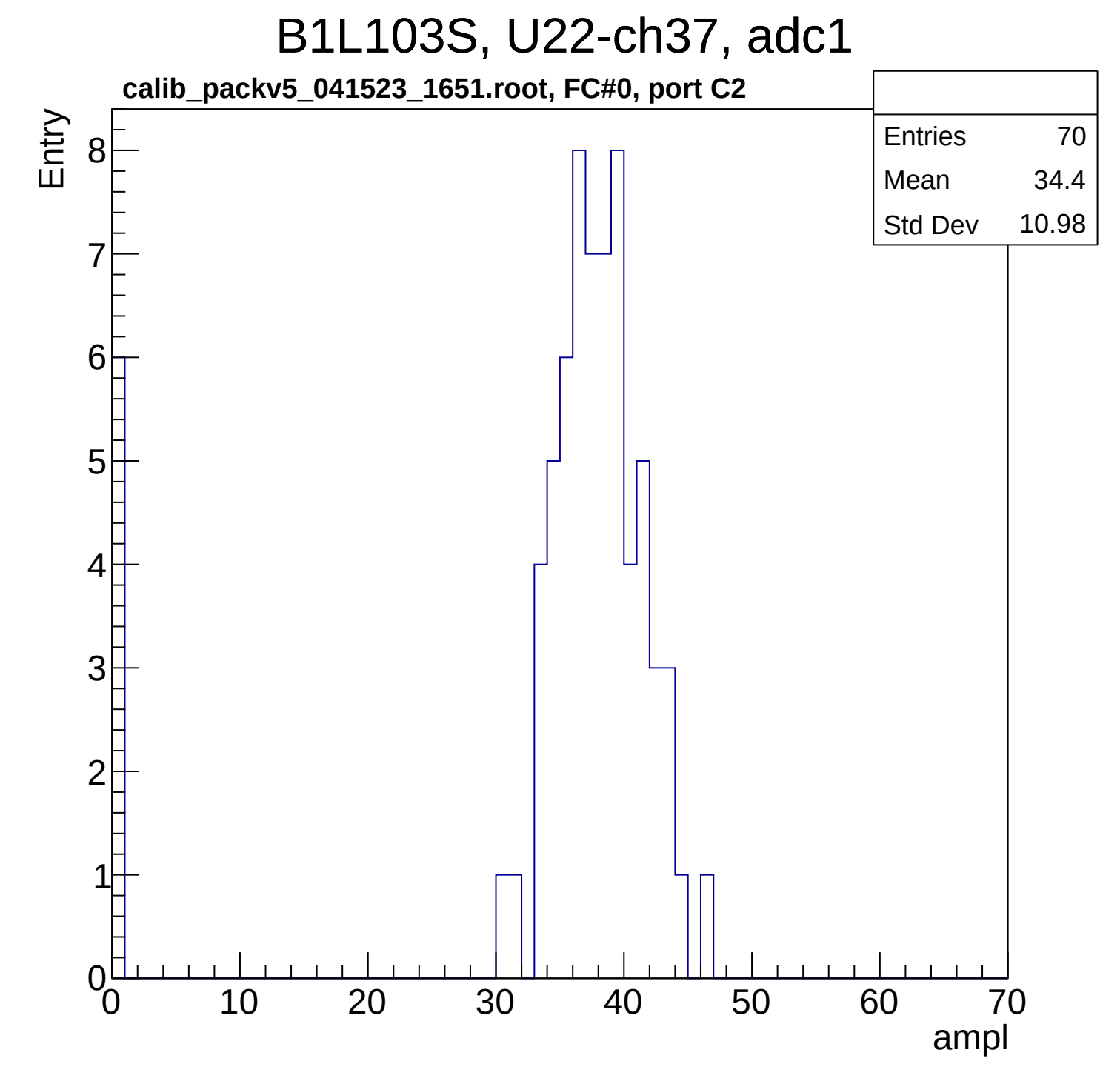
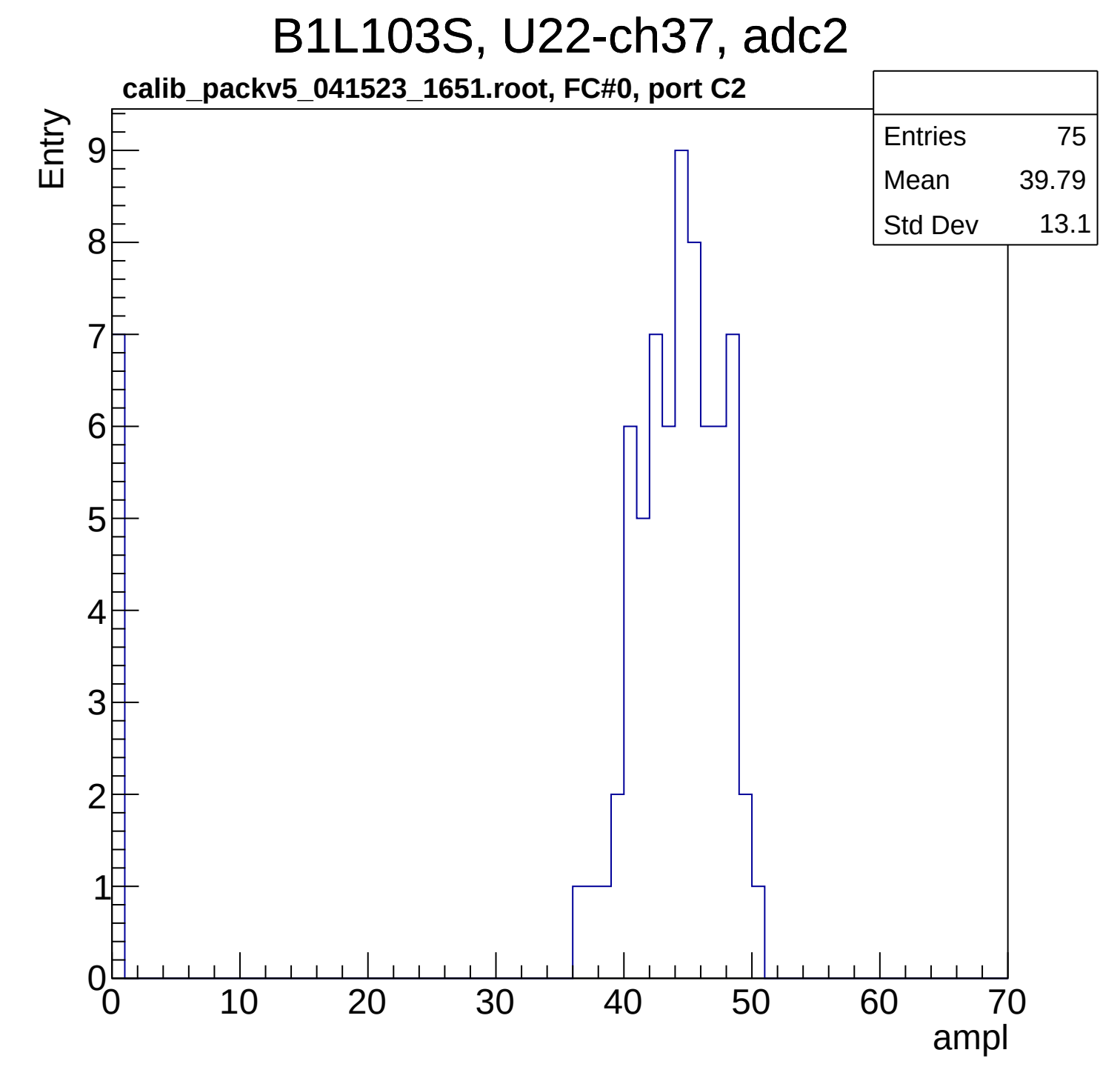
40
50
60
70


B1L103S, U22-ch36, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 61.62
Std Dev 1.443
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U22-ch36, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch37, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 96
Mean 27.83
Std Dev 8.079
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U22-ch37, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 34.4
Std Dev 10.98
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch37, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 39.79
Std Dev 13.1
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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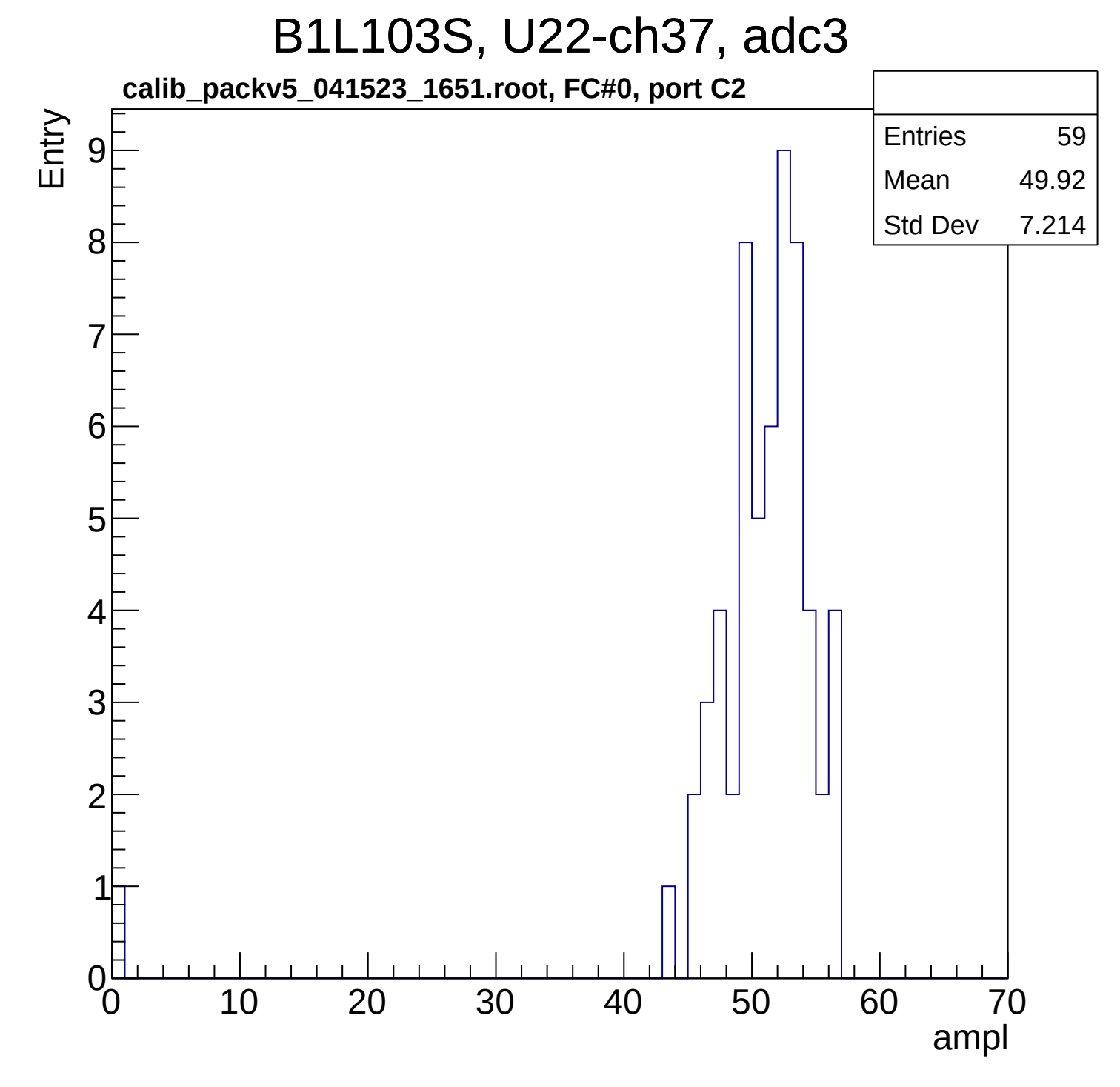
B1L103S, U22-ch37, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 49.92
Std Dev 7.214
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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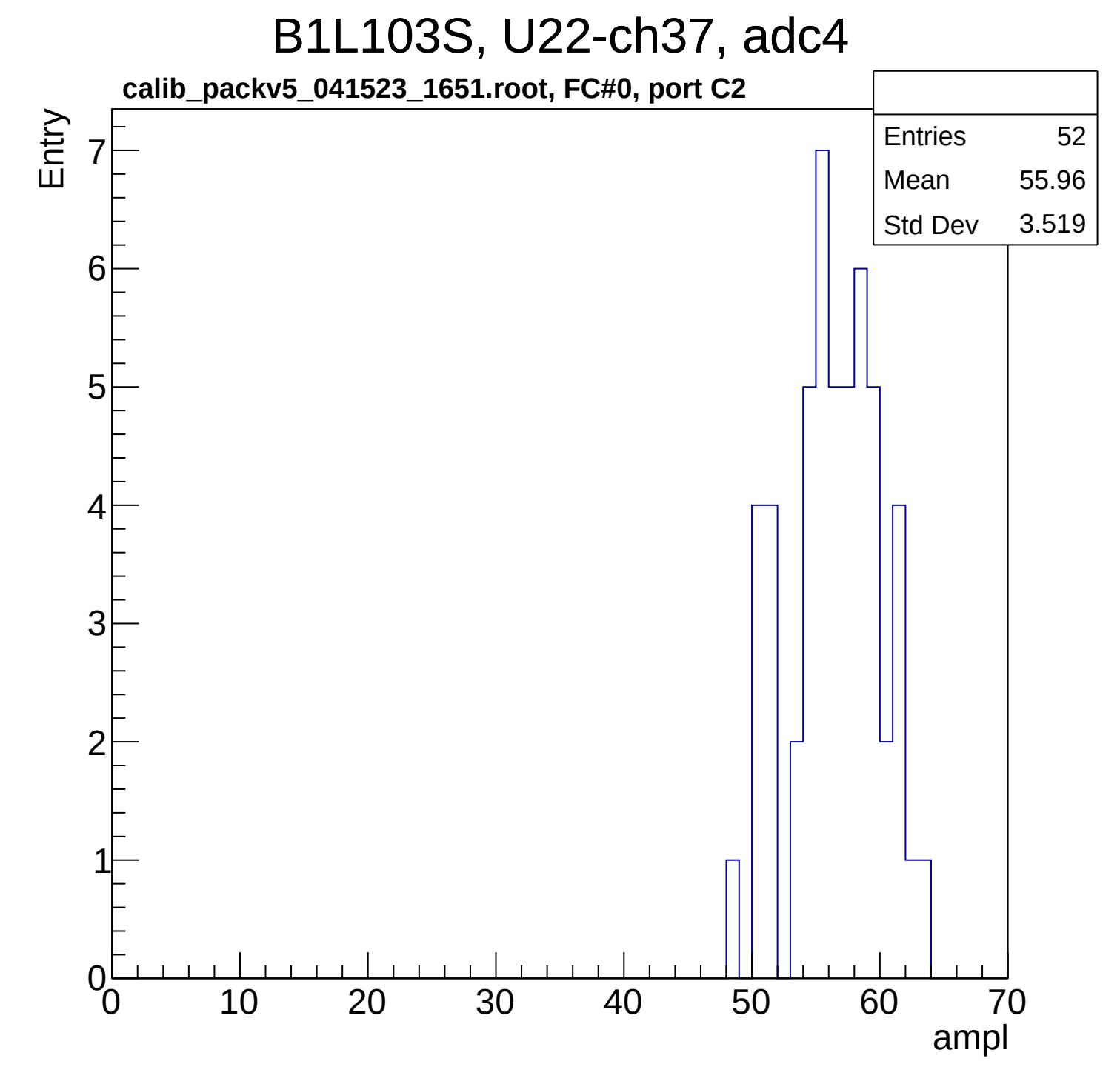
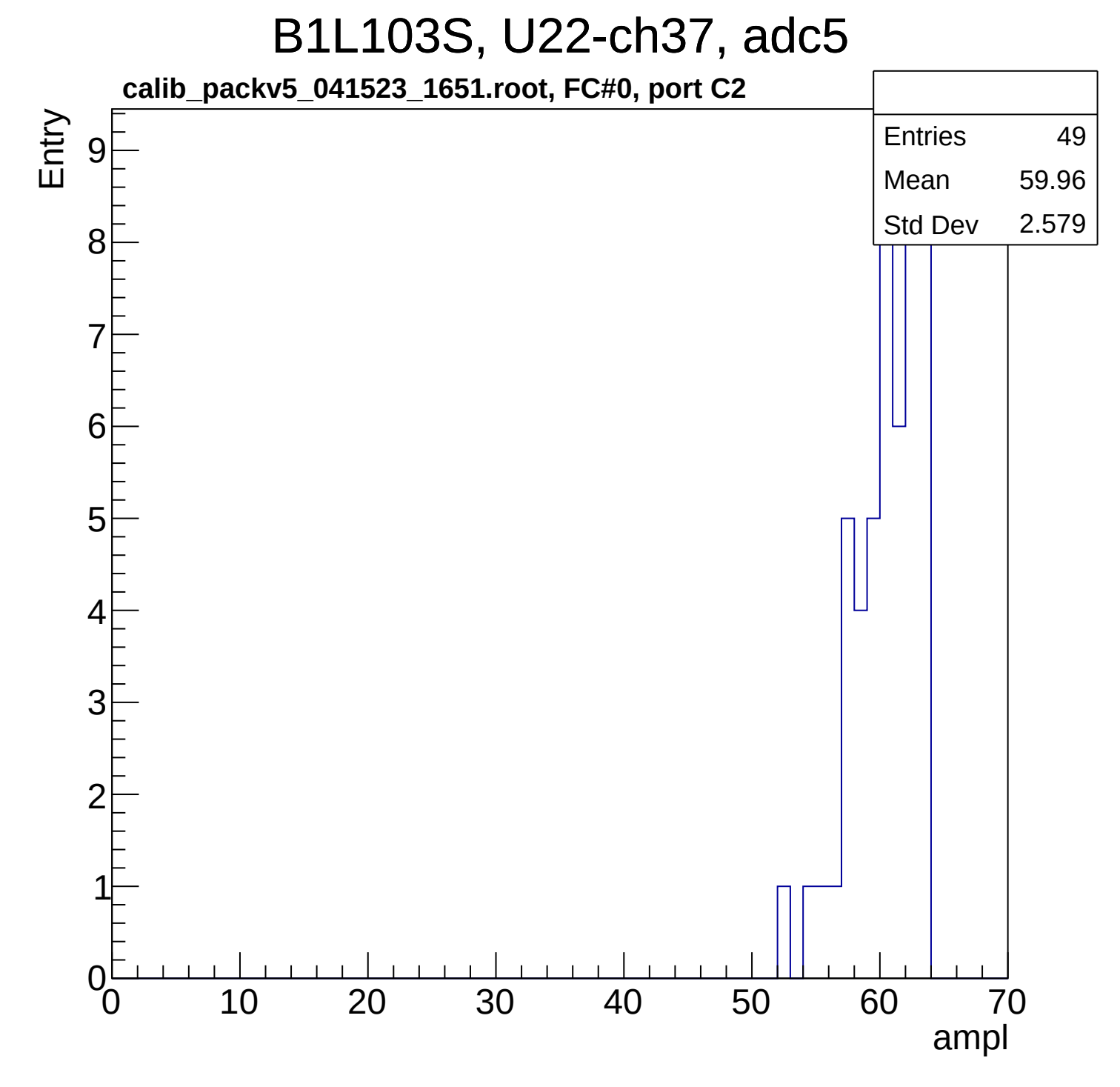
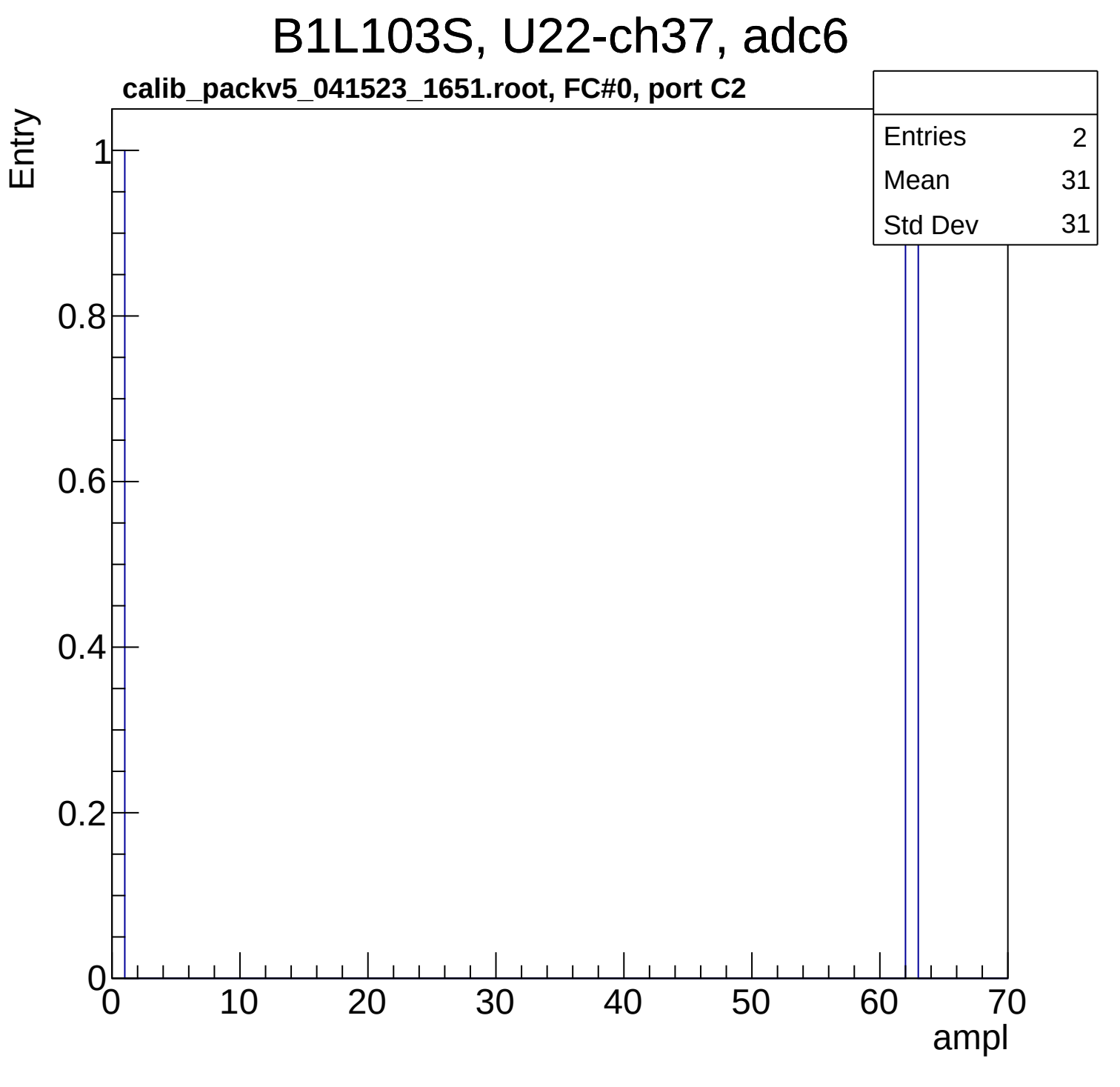
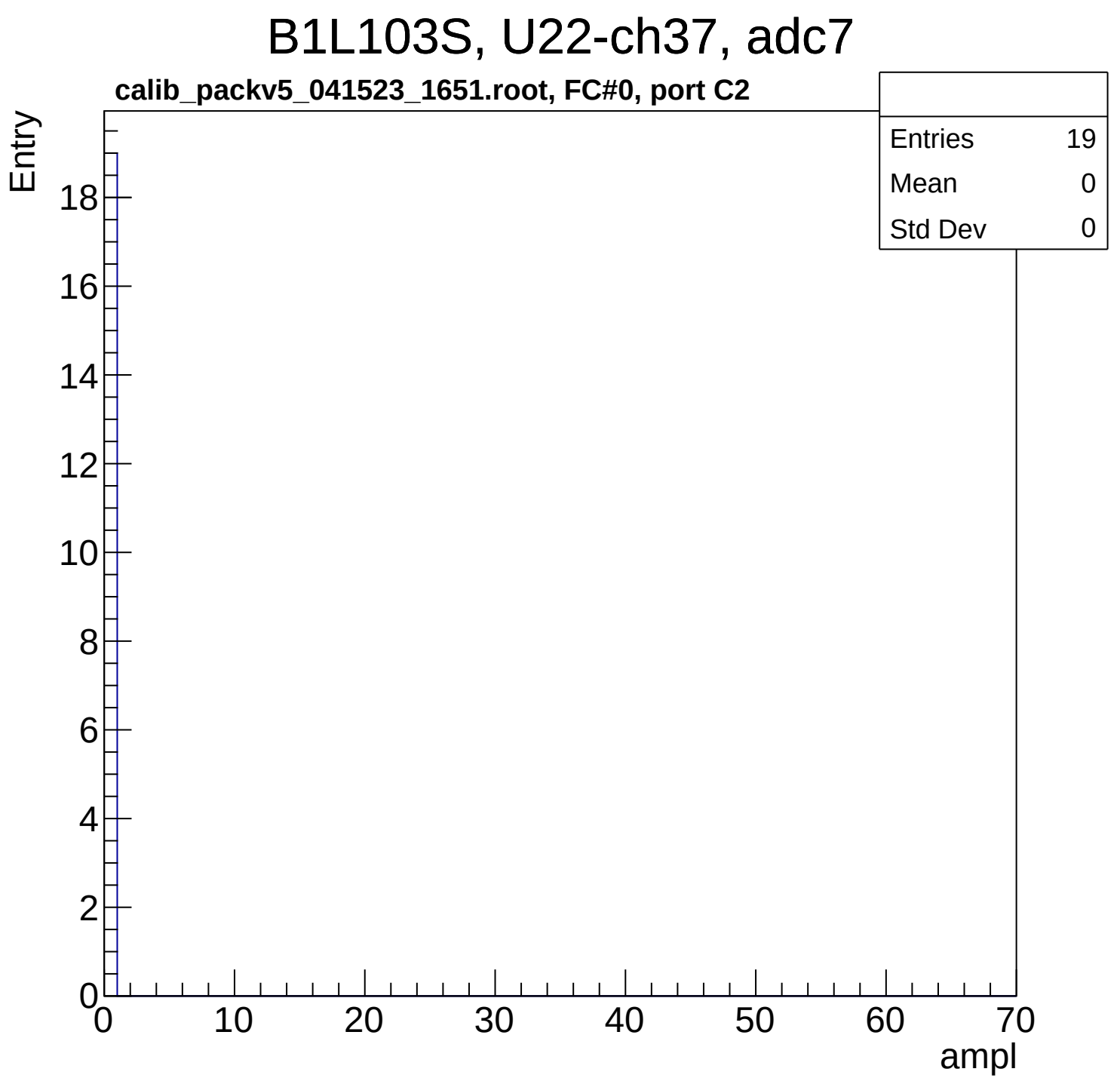
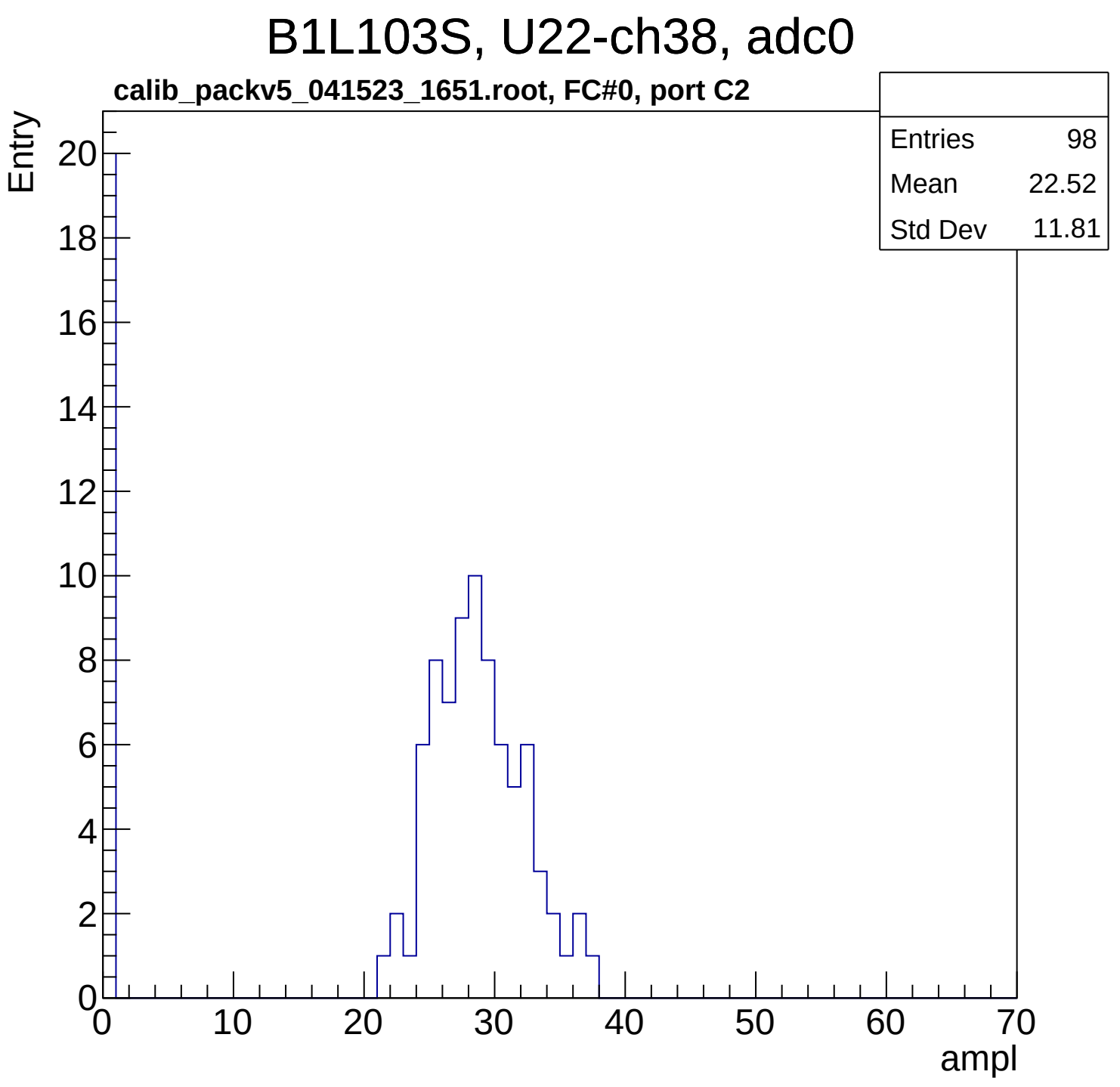
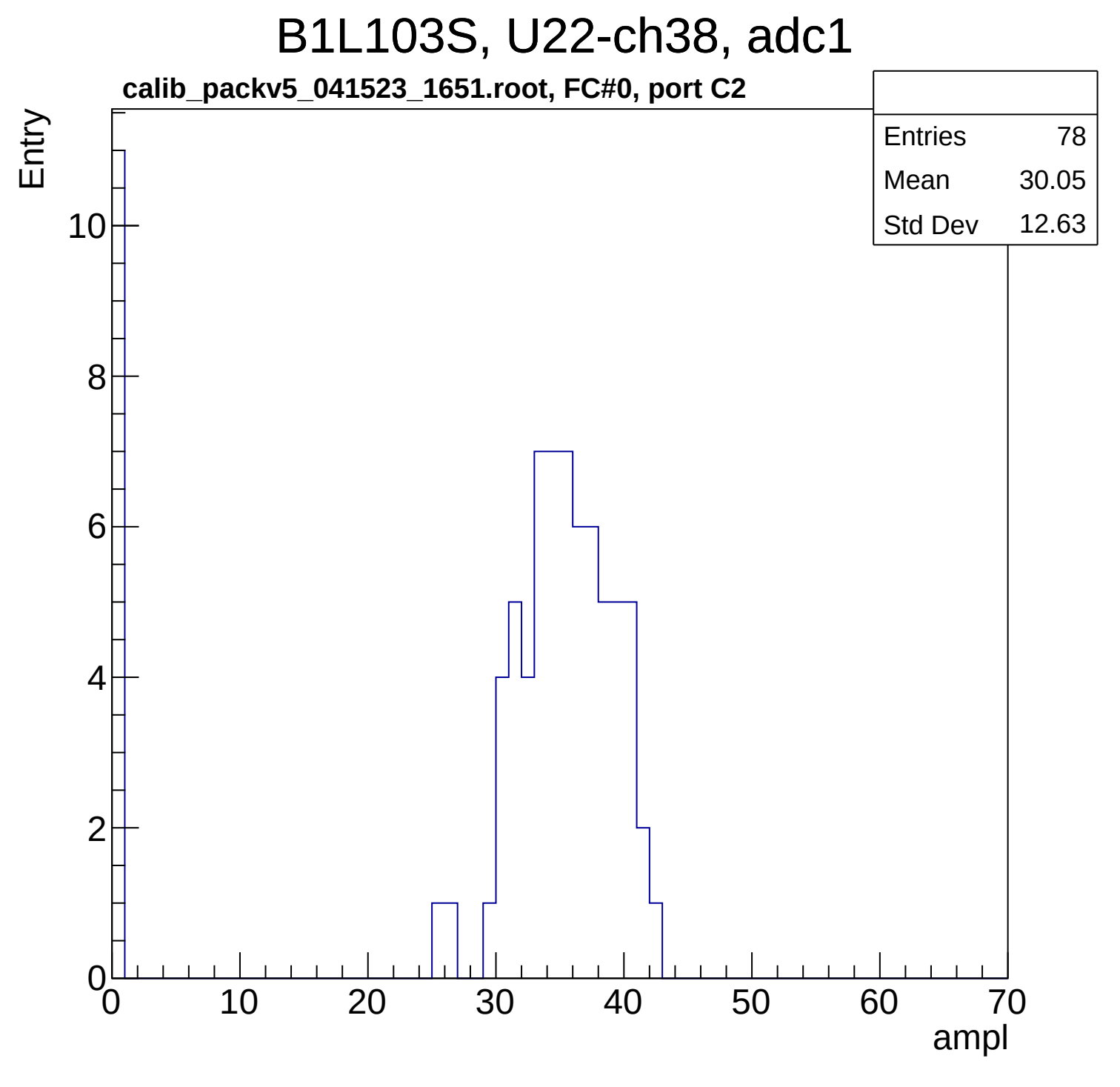

B1L103S, U22-ch37, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 55.96
Std Dev 3.519
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

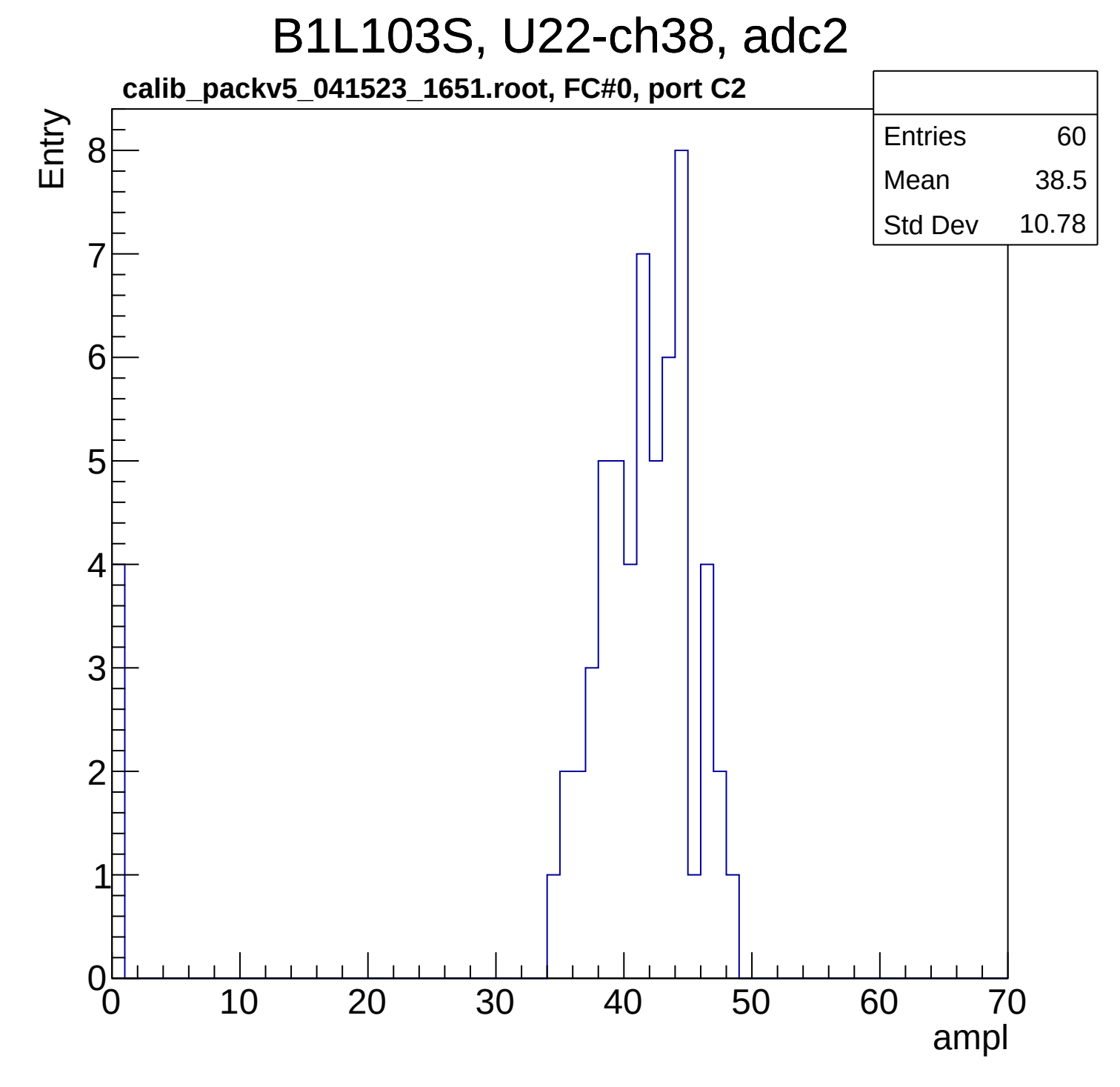

B1L103S, U22-ch37, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 59.96
Std Dev 2.579
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch37, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 31
Std Dev 31
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch37, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch38, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 98
Mean 22.52
Std Dev 11.81
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70


B1L103S, U22-ch38, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 30.05
Std Dev 12.63
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch38, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 38.5
Std Dev 10.78
Entry
ampl
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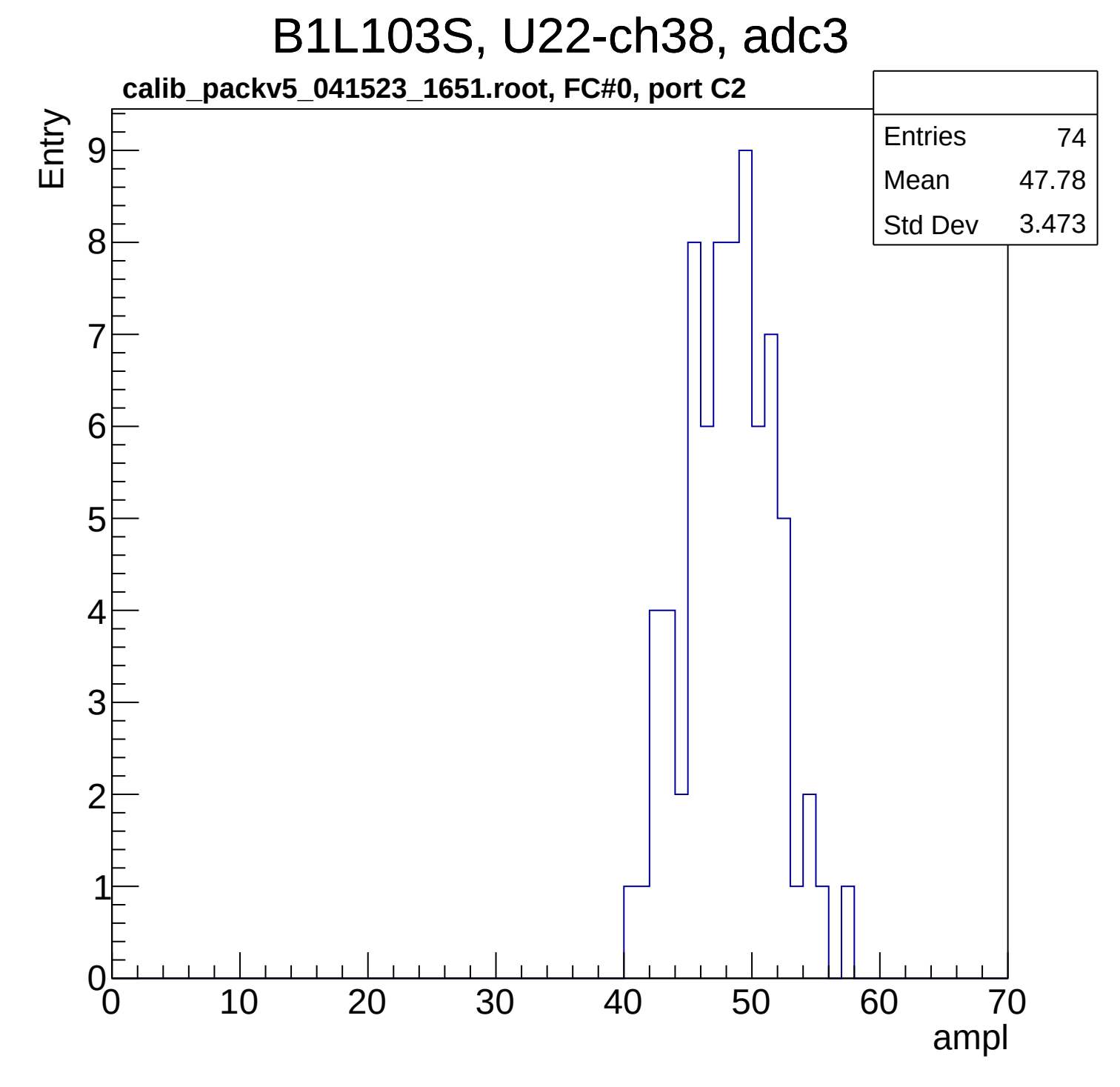
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch38, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 47.78
Std Dev 3.473
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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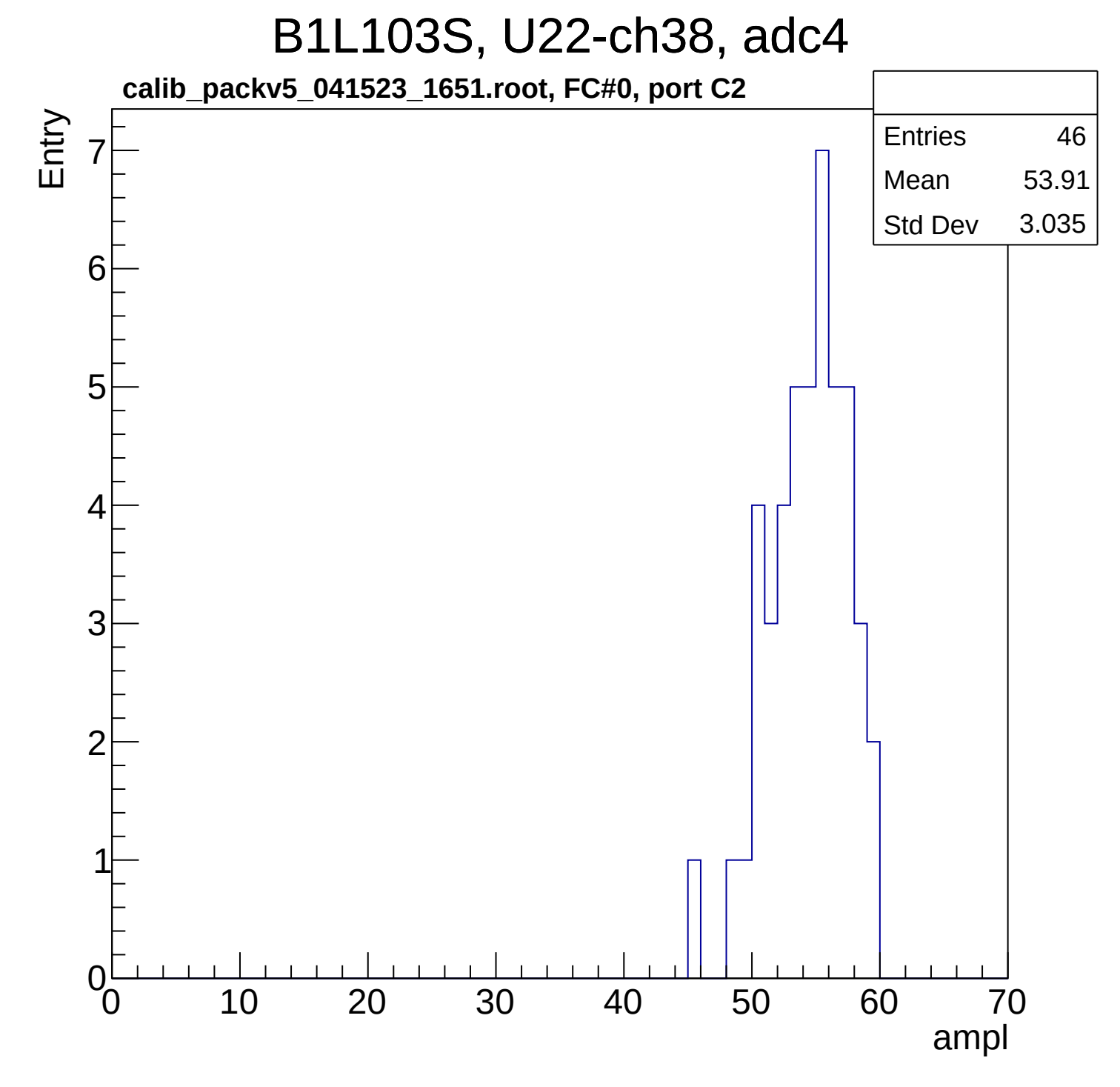
30
40
50
60
70


B1L103S, U22-ch38, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 53.91
Std Dev 3.035
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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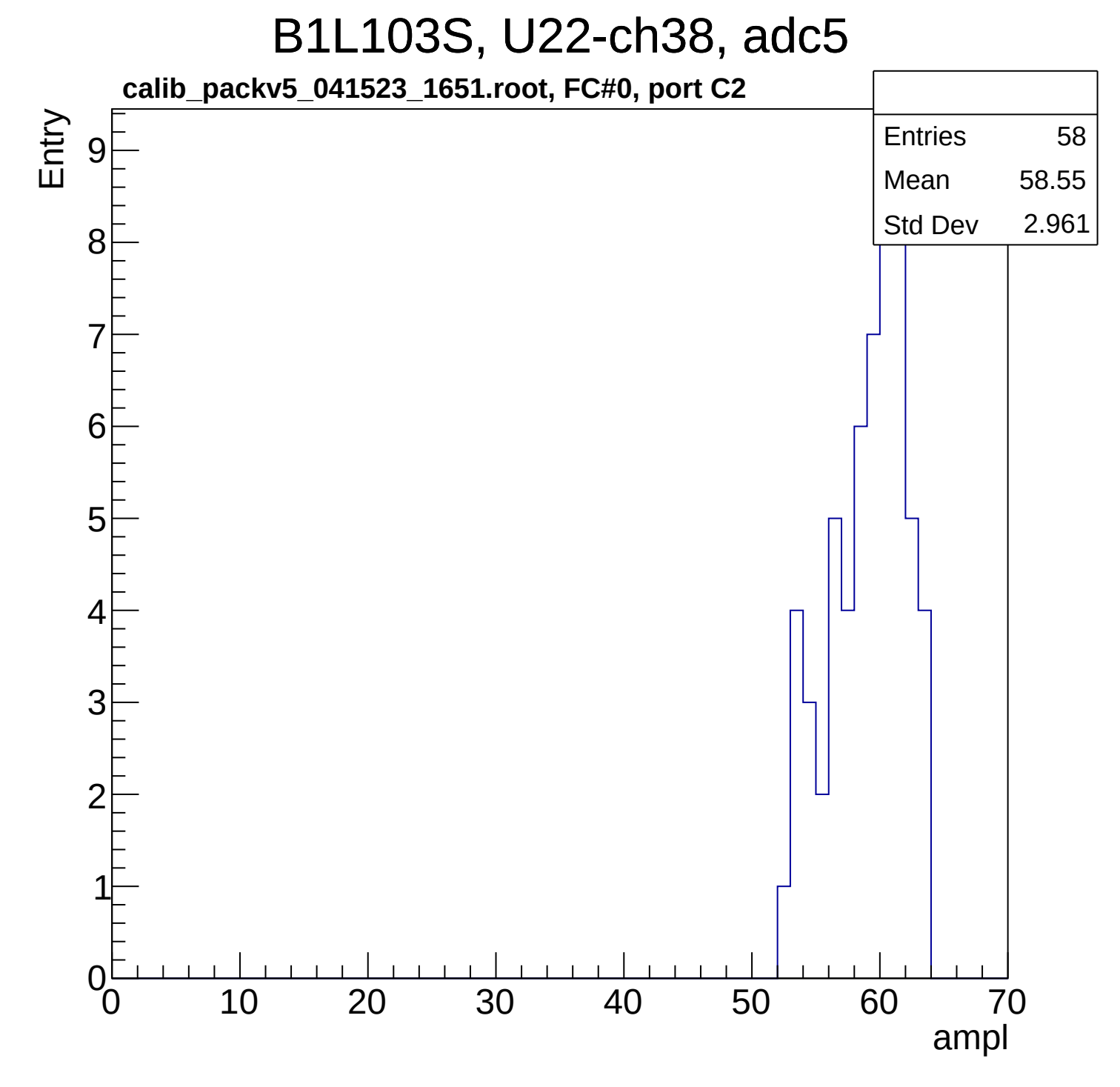
40
50
60
70


B1L103S, U22-ch38, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 58.55
Std Dev 2.961
Entry
ampl
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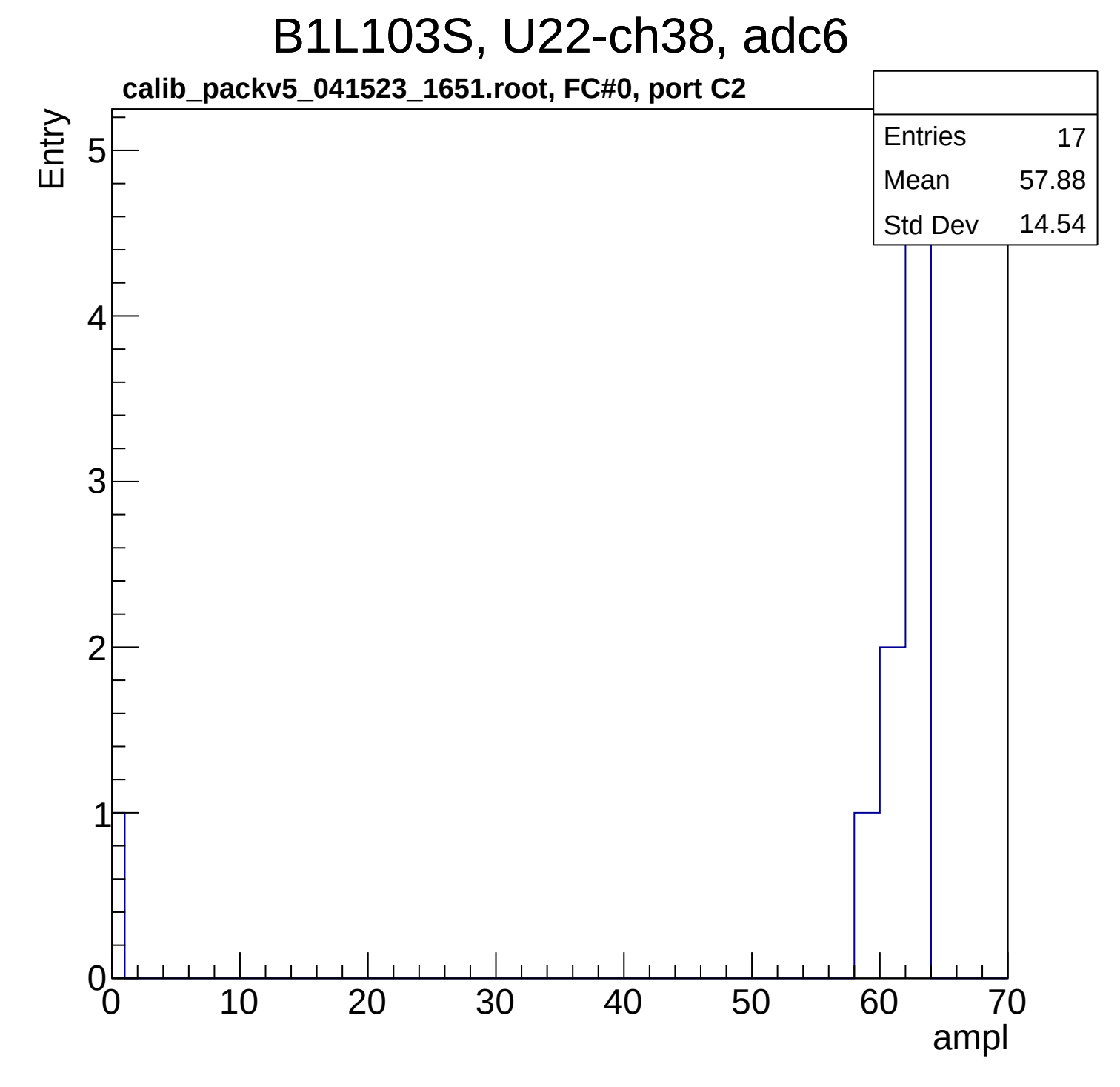
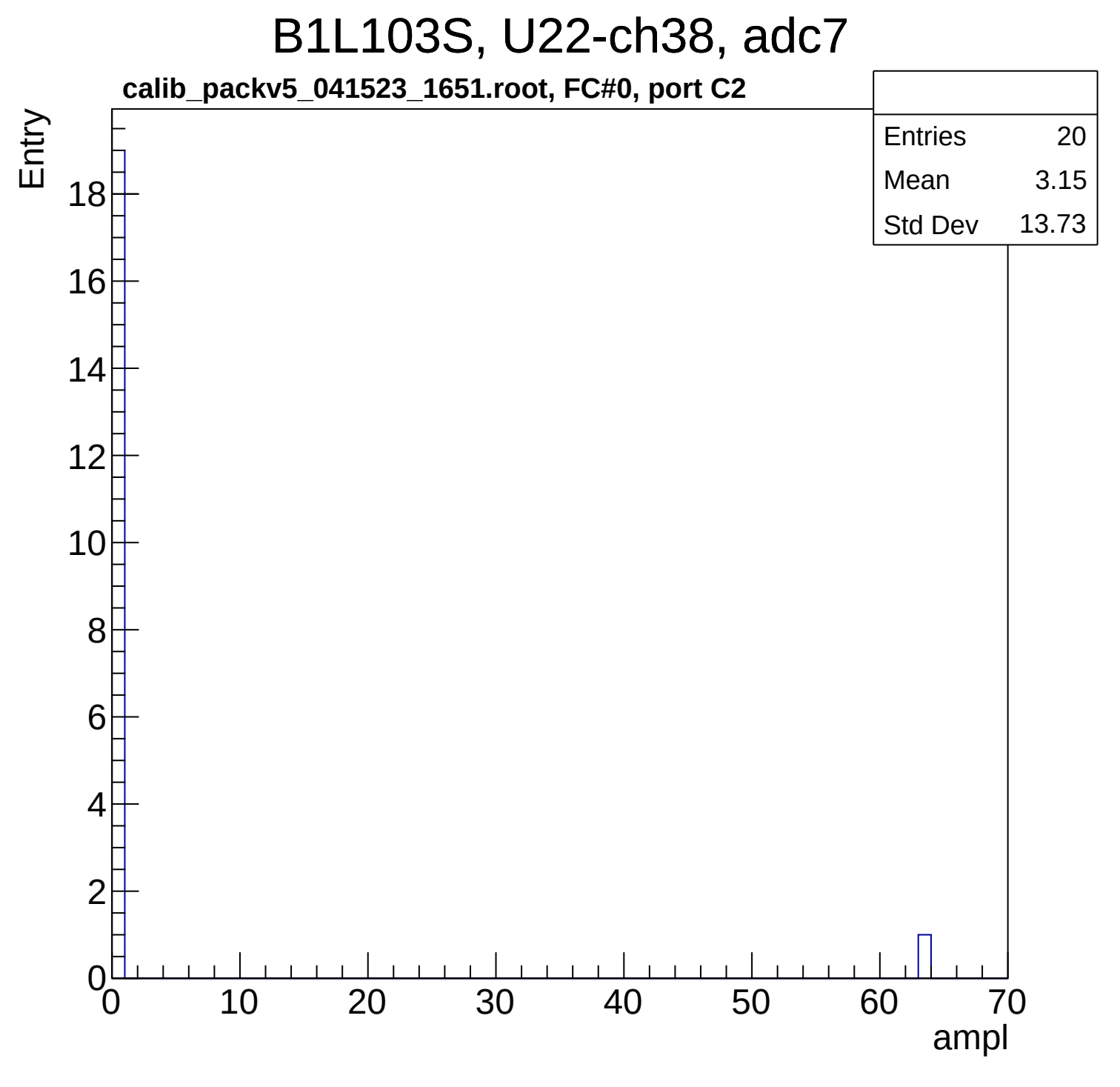
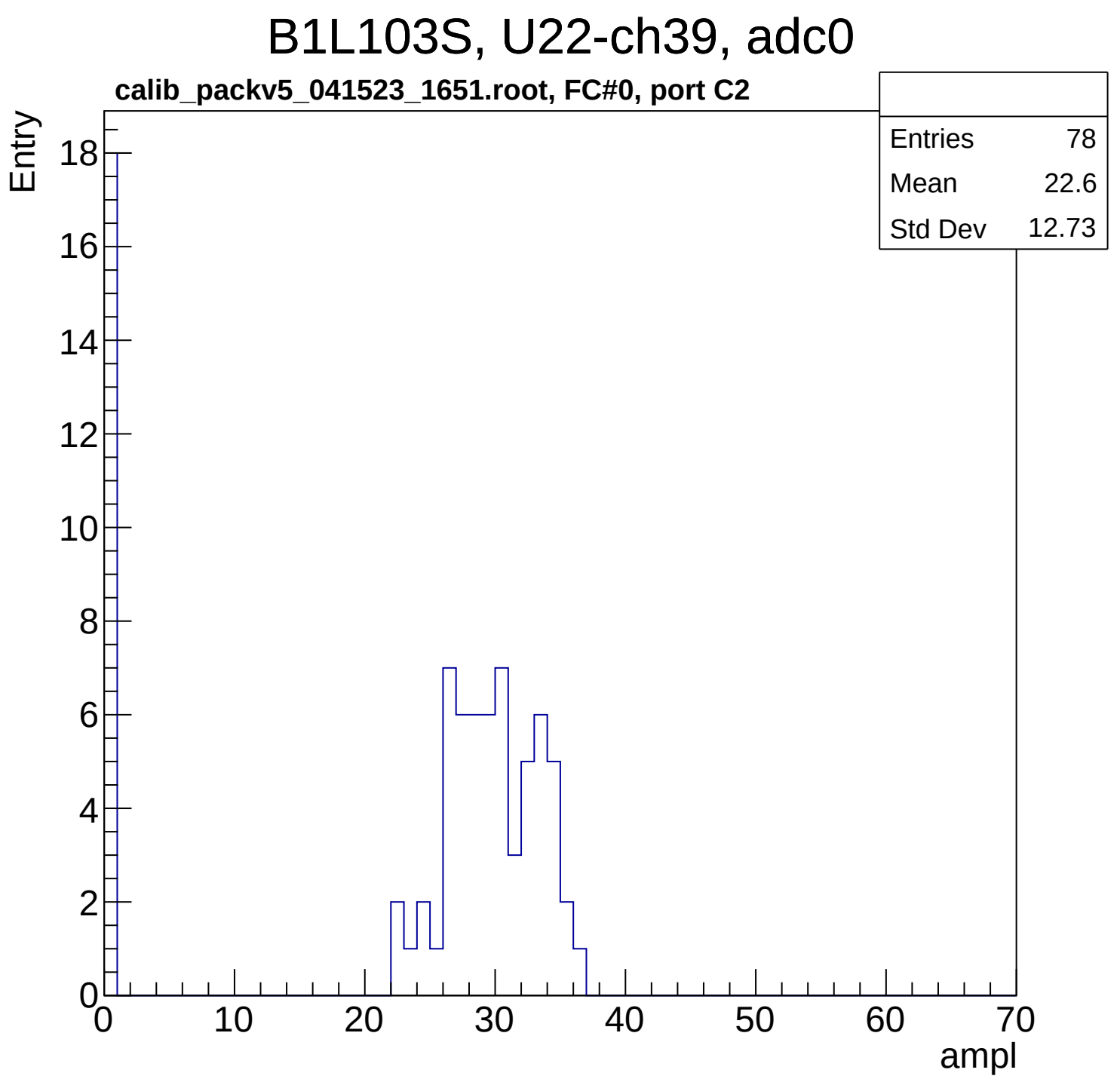
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch38, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 57.88
Std Dev 14.54
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U22-ch38, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch39, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 22.6
Std Dev 12.73
Entry
0
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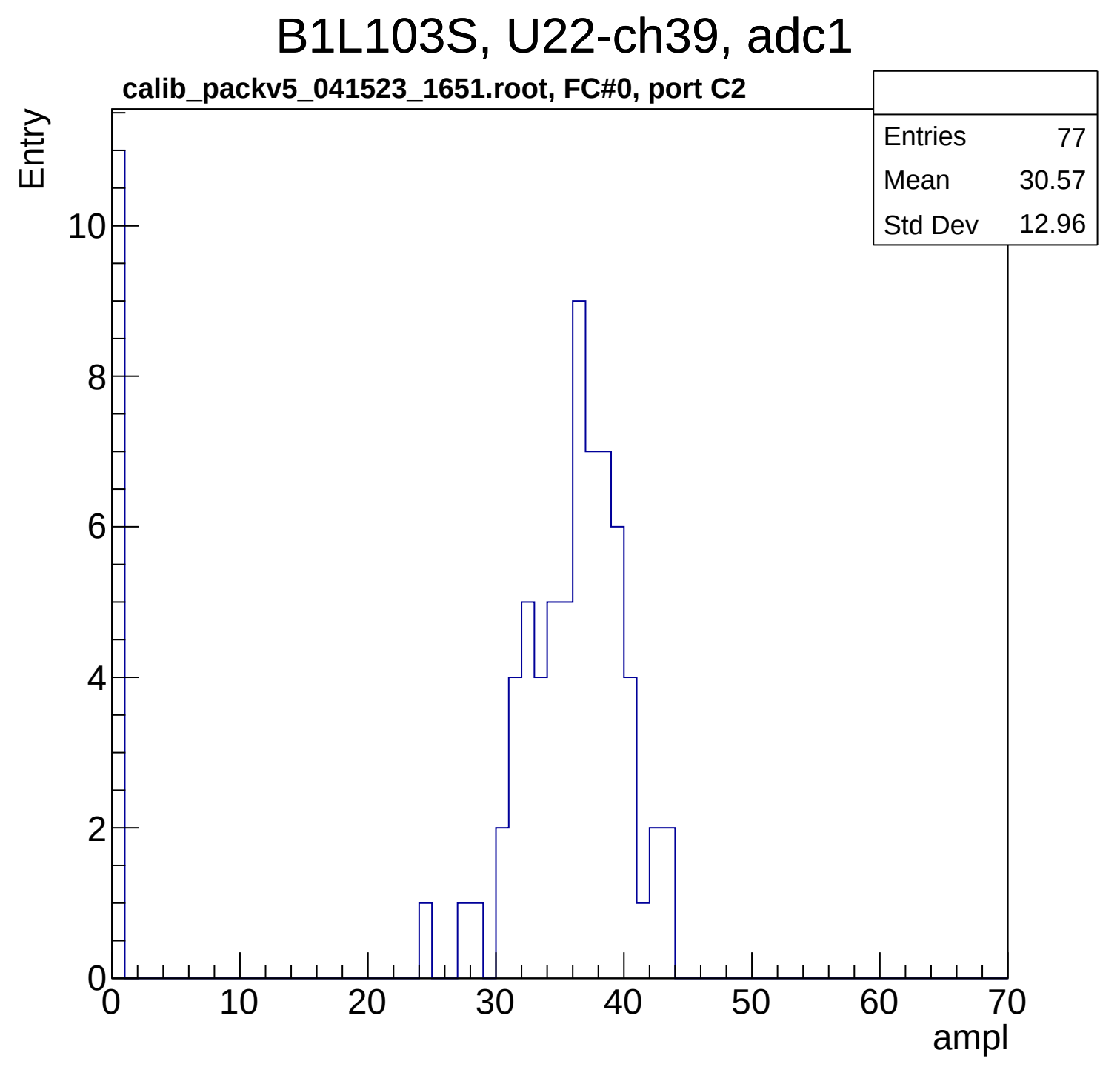
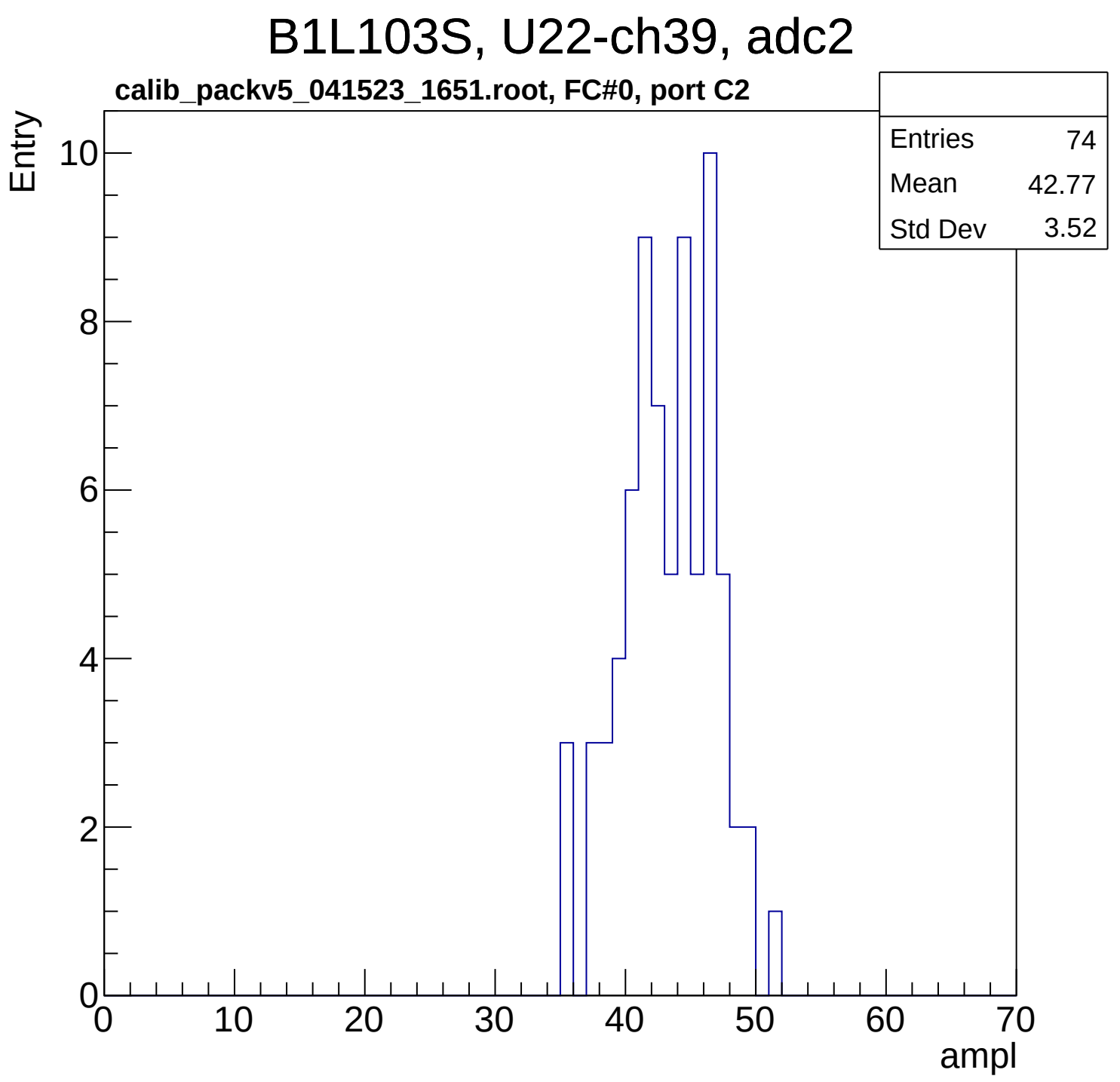
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch39, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 30.57
Std Dev 12.96
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch39, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 42.77
Std Dev 3.52
Entry
ampl
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2
4
6
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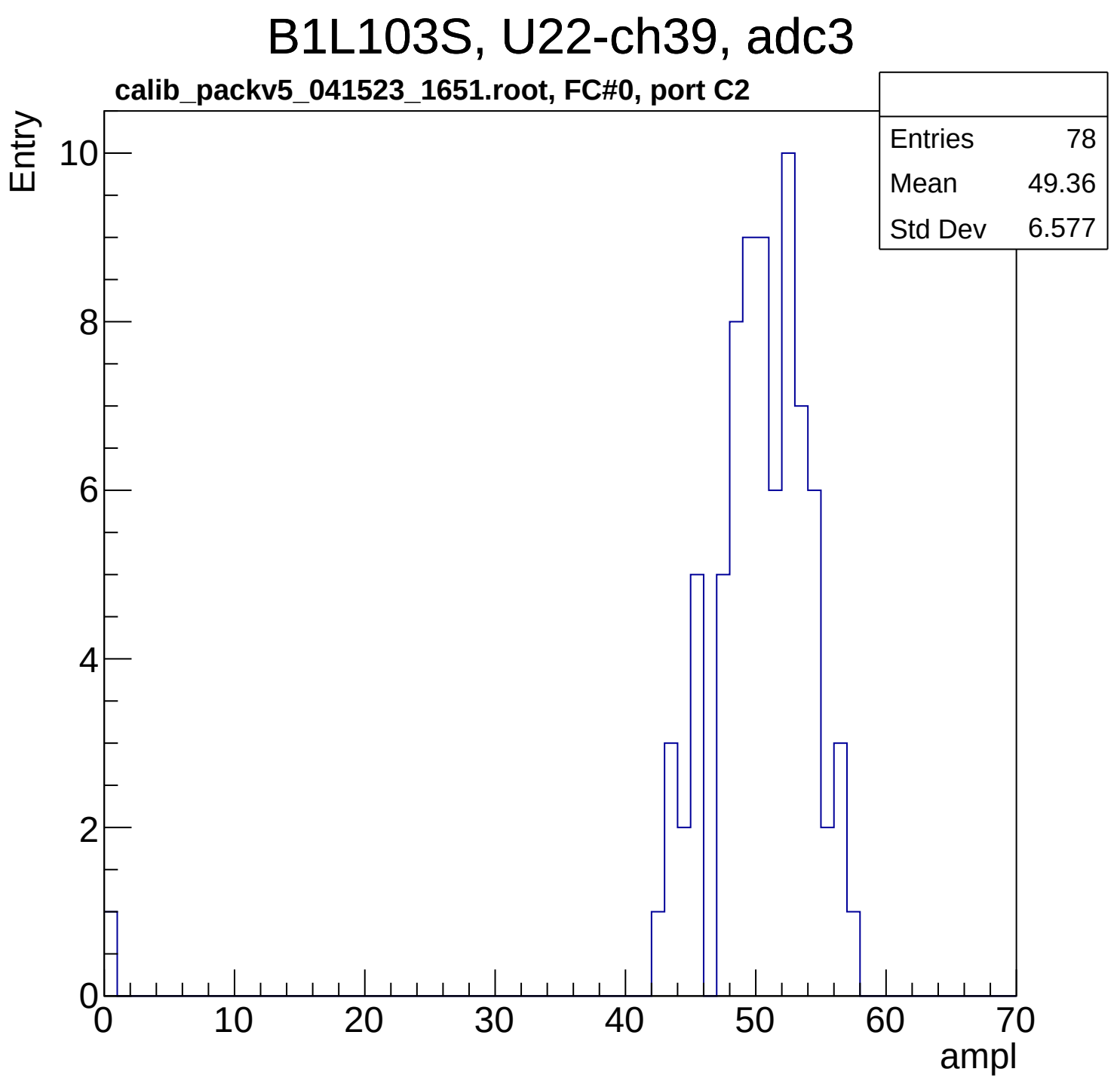
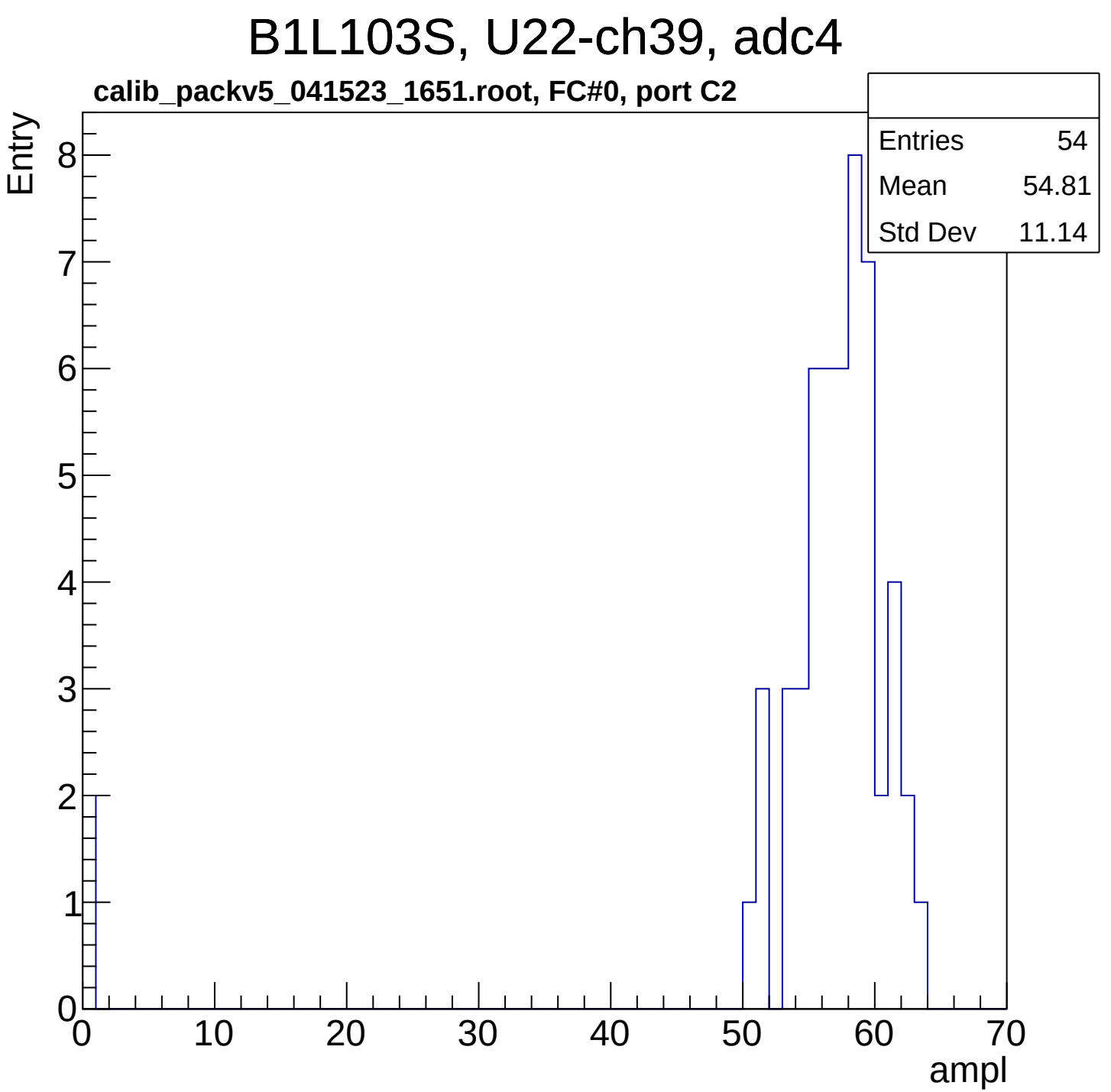
10
0
10
20
30
40
50
60
70


B1L103S, U22-ch39, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 49.36
Std Dev 6.577
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch39, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 54.81
Std Dev 11.14
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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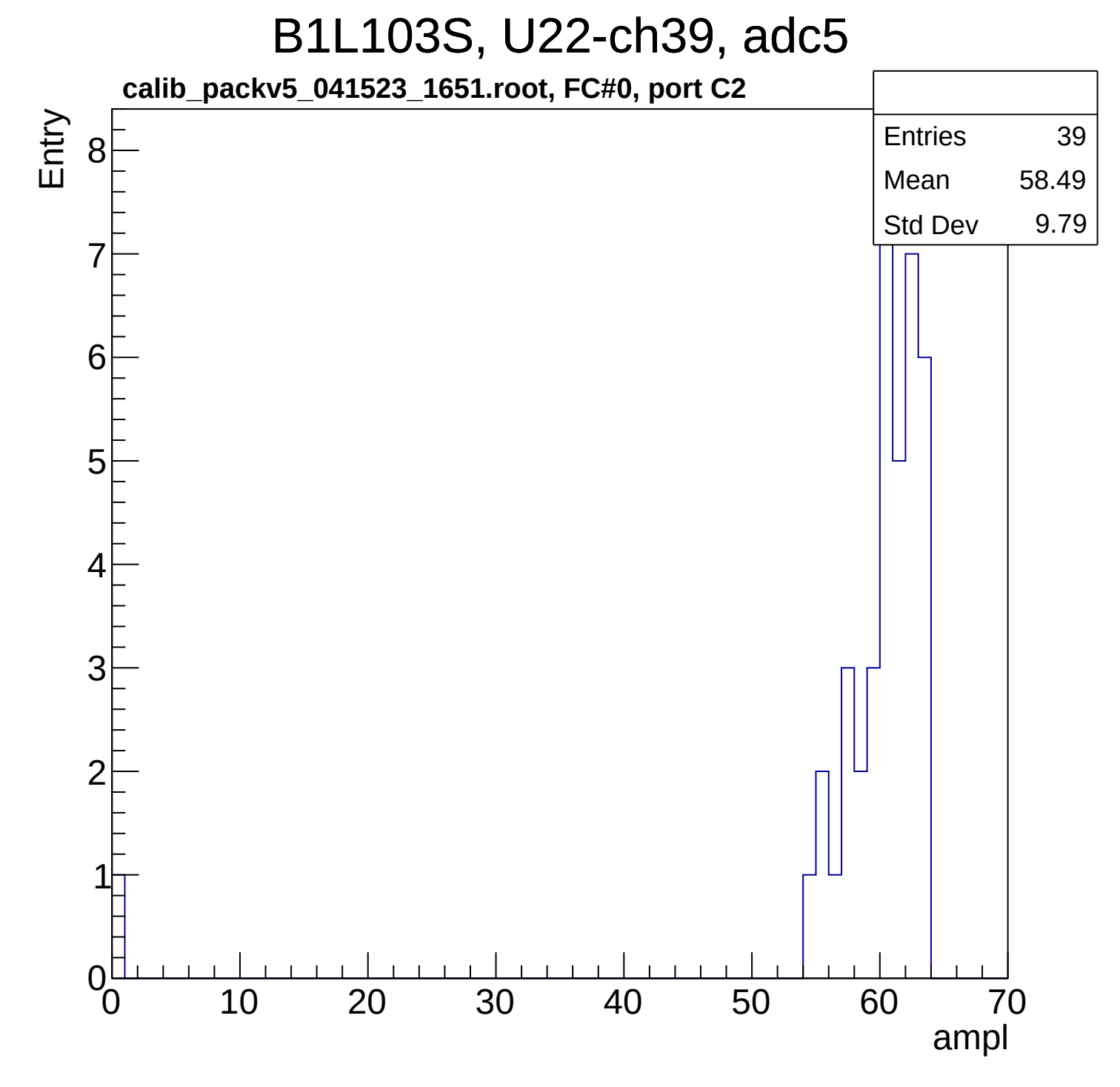
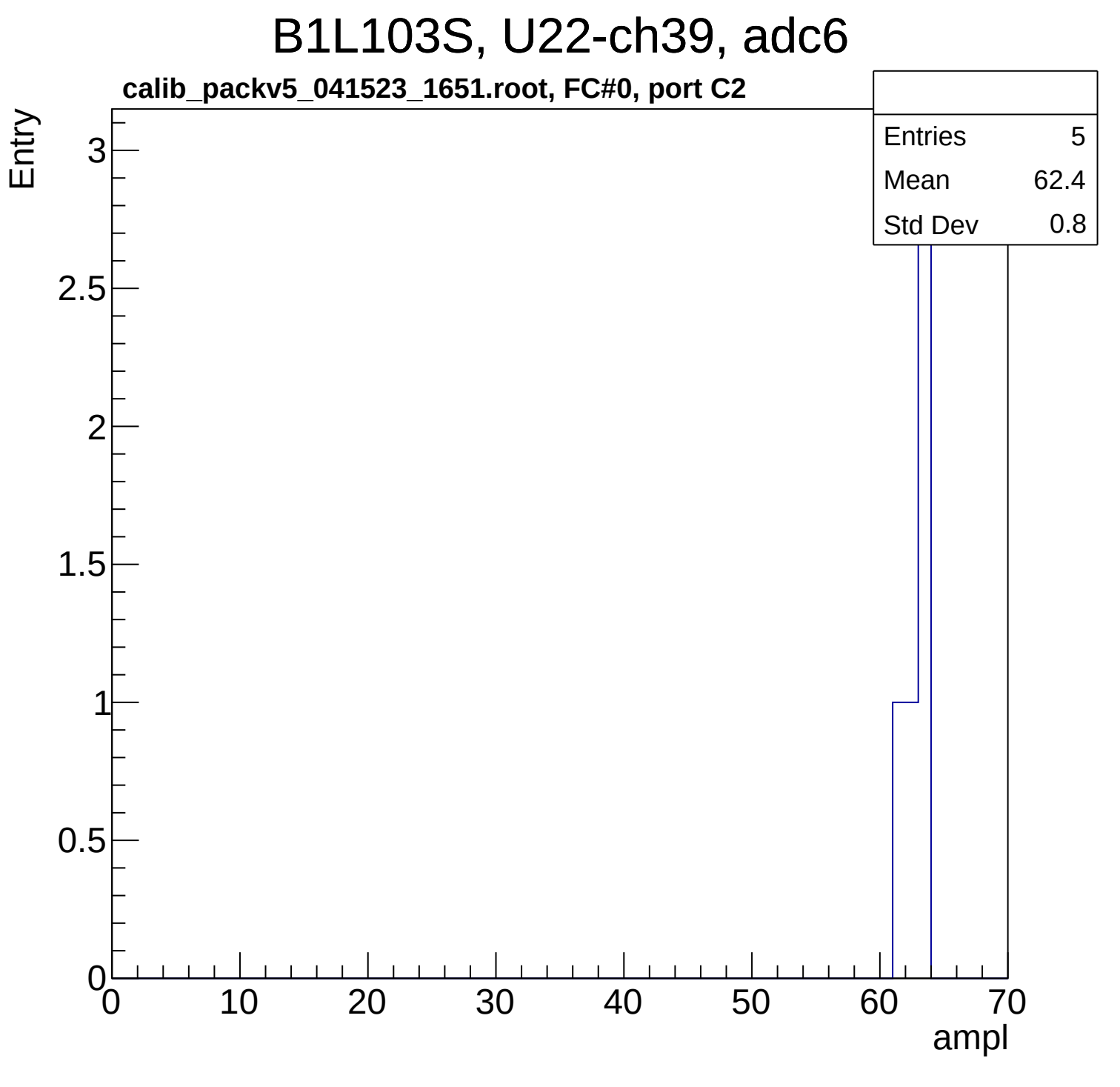
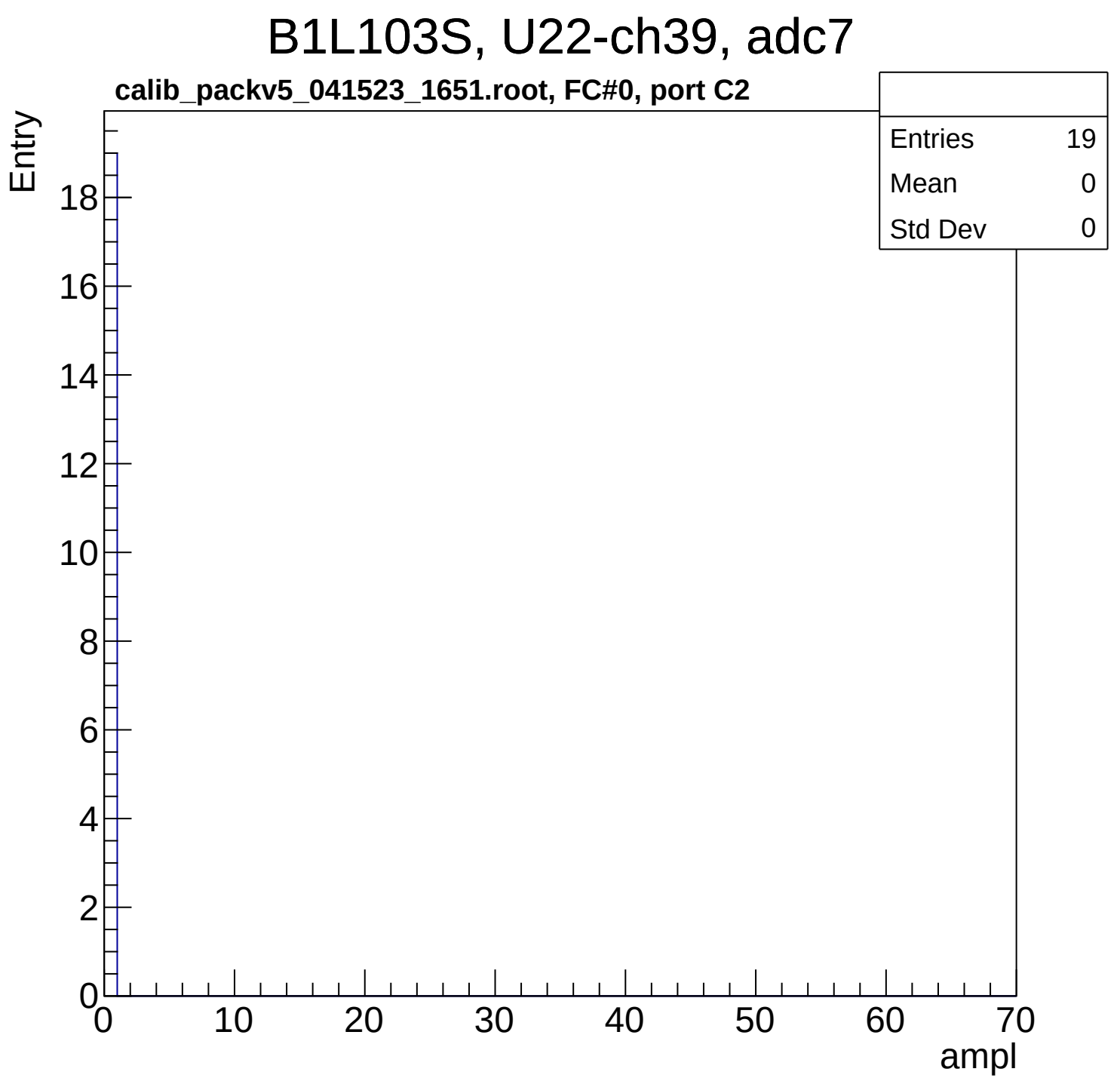
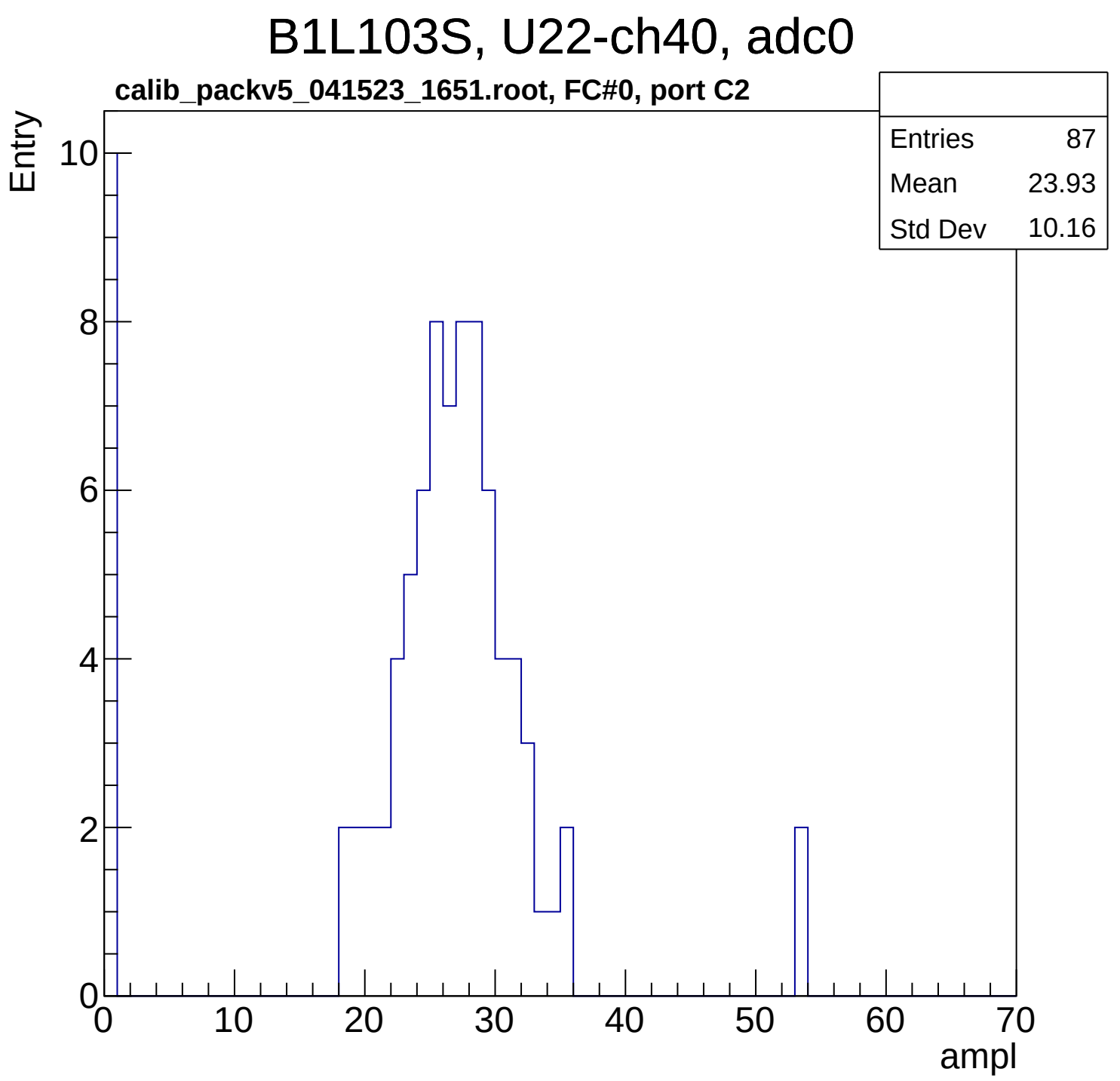
40
50
60
70


B1L103S, U22-ch39, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 58.49
Std Dev 9.79
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch39, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 62.4
Std Dev 0.8
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U22-ch39, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch40, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 23.93
Std Dev 10.16
Entry
ampl
0
2
4
6
8
10
0
10
20
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40
50
60
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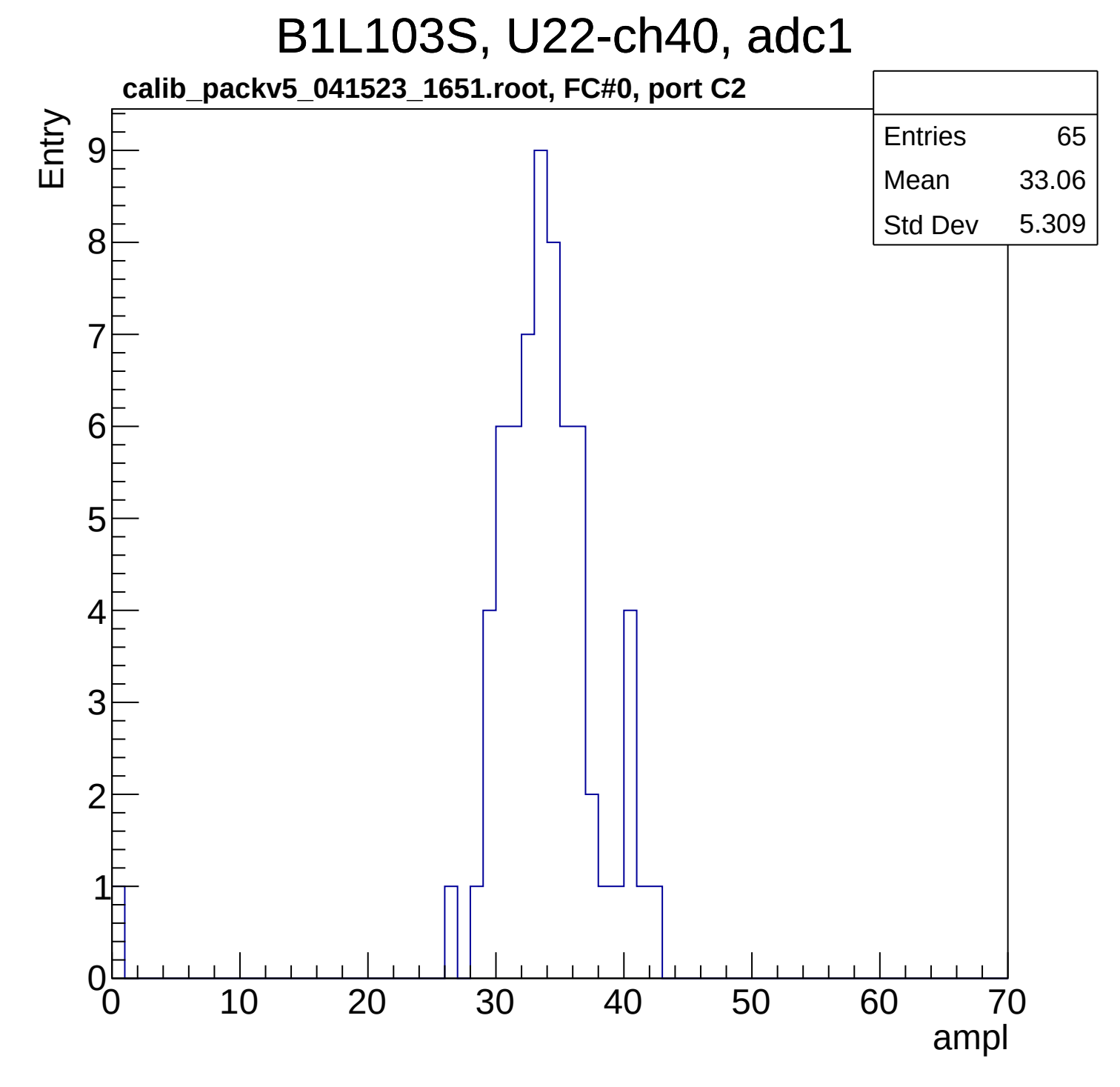
B1L103S, U22-ch40, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 33.06
Std Dev 5.309
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
30
40
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60
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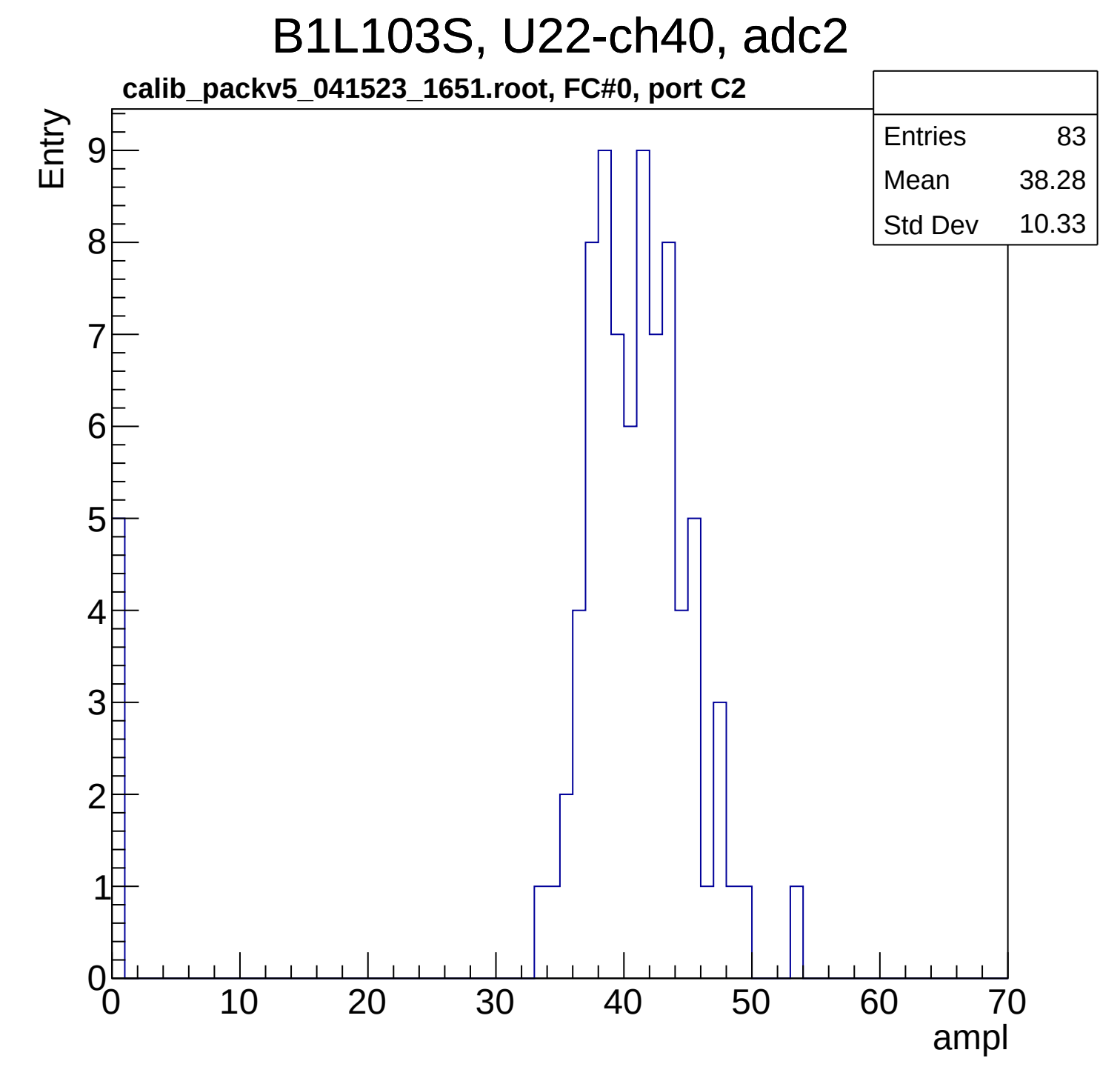
B1L103S, U22-ch40, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 38.28
Std Dev 10.33
Entry
ampl
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3
4
5
6
7
8
9
0
10
20
30
40
50
60
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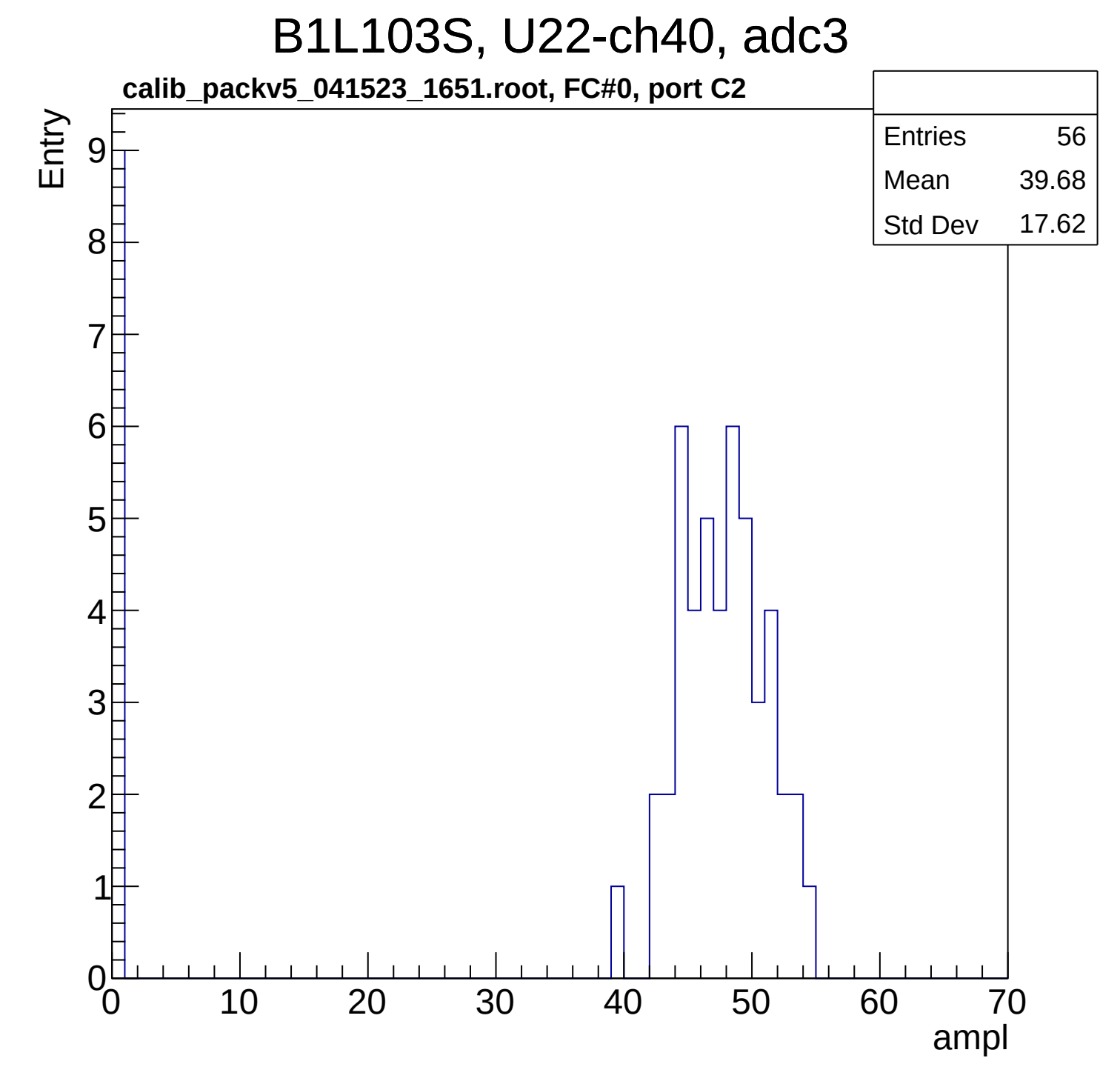
B1L103S, U22-ch40, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 39.68
Std Dev 17.62
Entry
ampl
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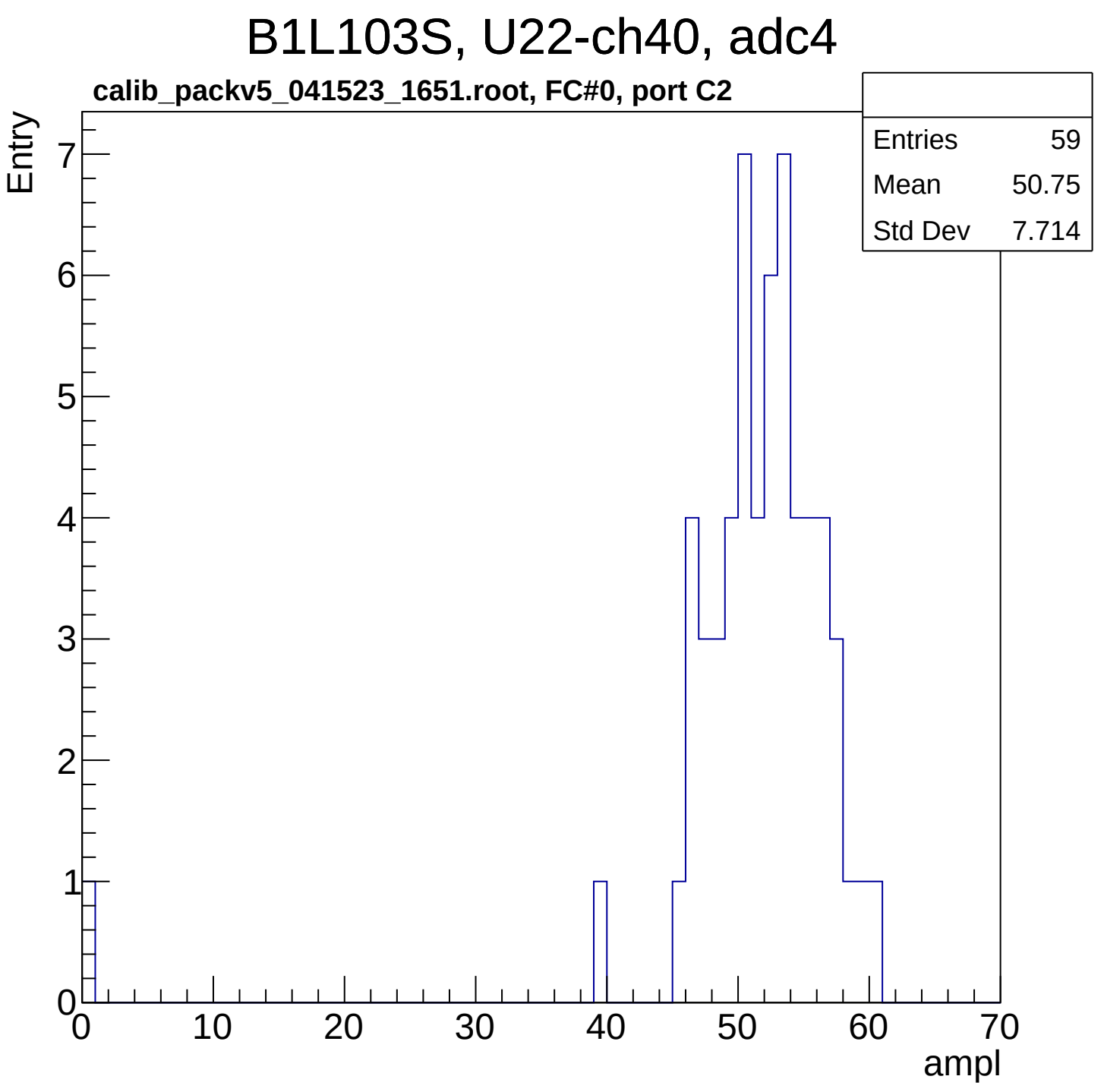
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch40, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 50.75
Std Dev 7.714
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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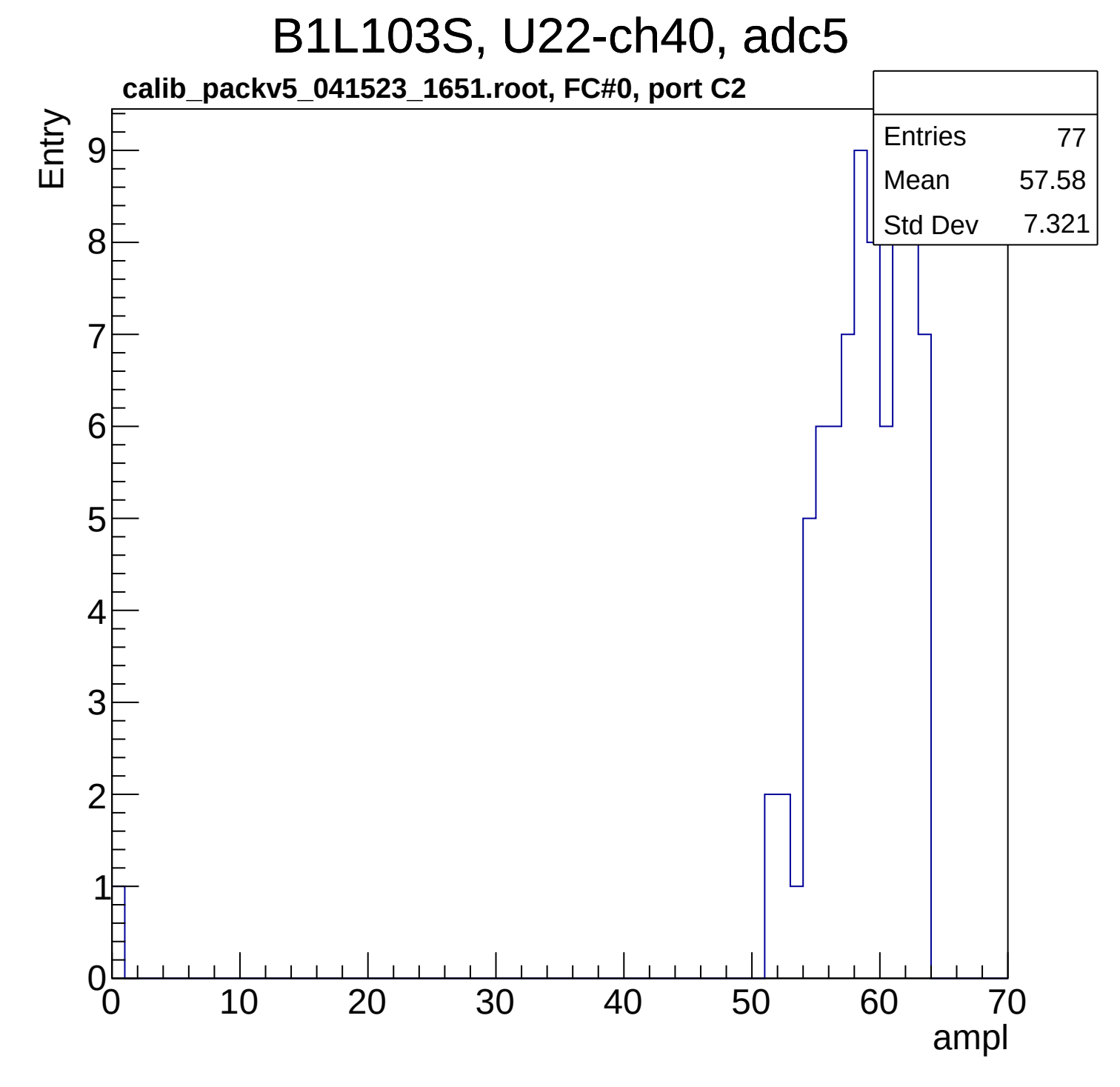
B1L103S, U22-ch40, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 57.58
Std Dev 7.321
Entry
ampl
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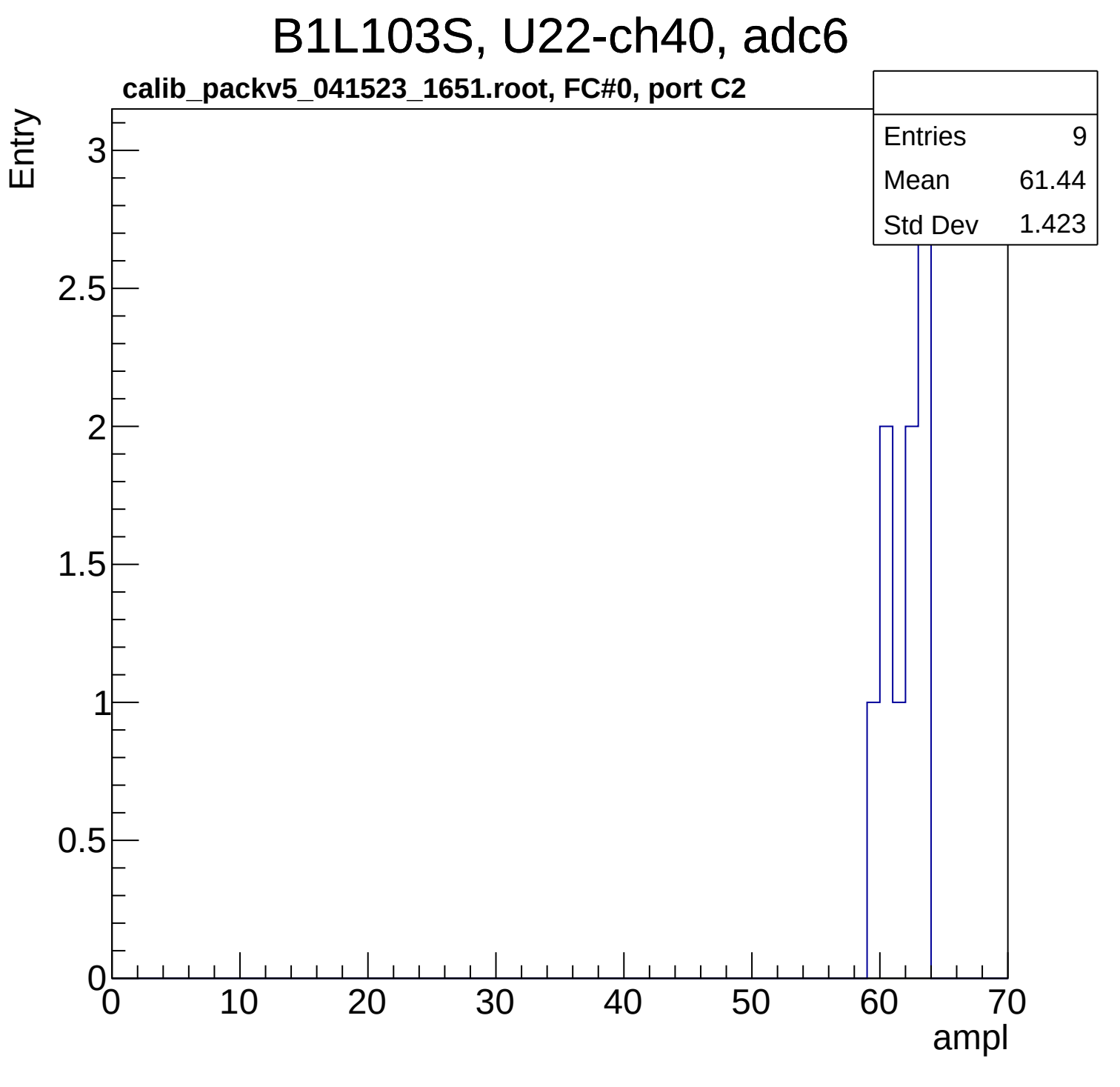
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch40, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 61.44
Std Dev 1.423
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
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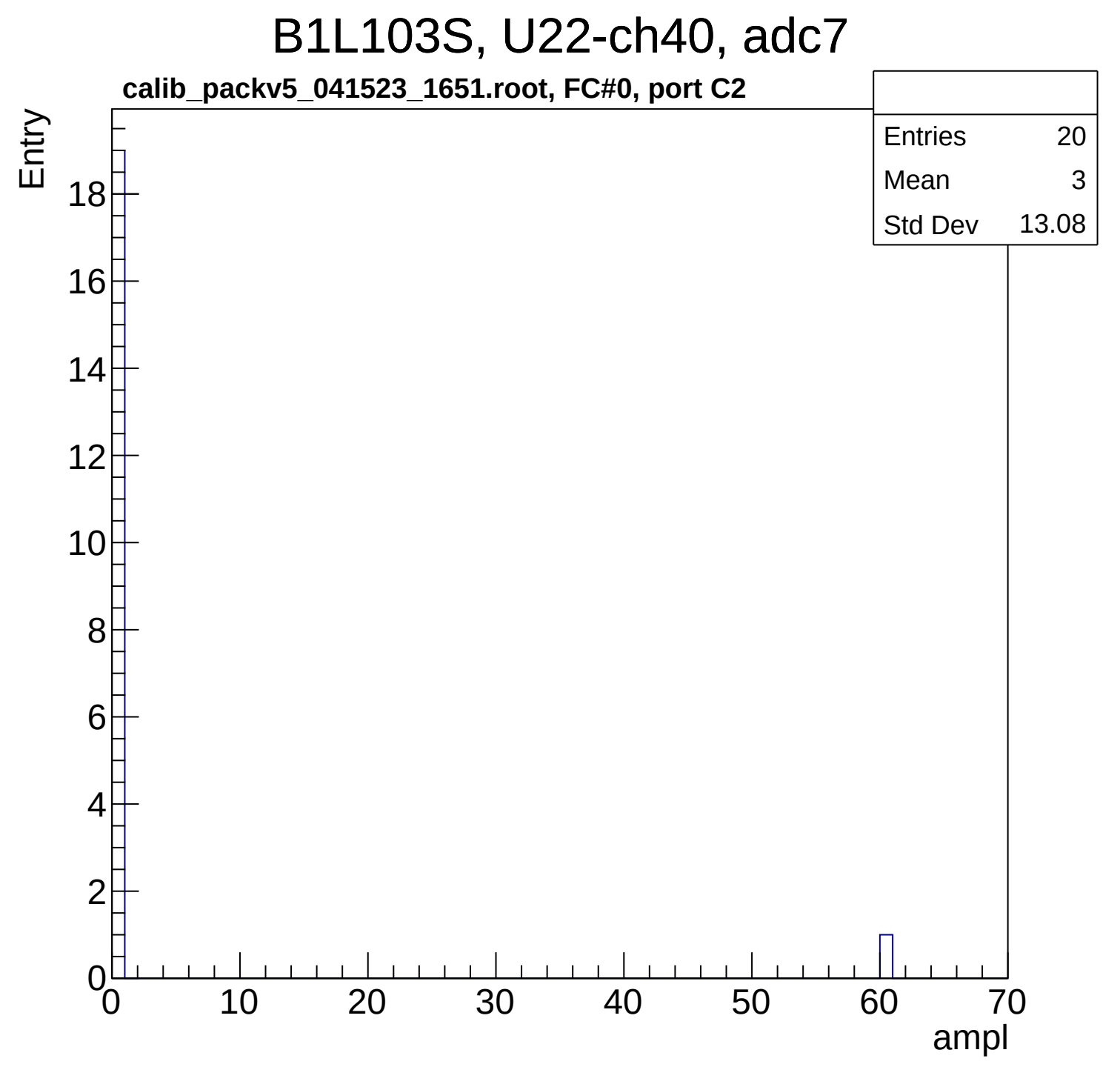
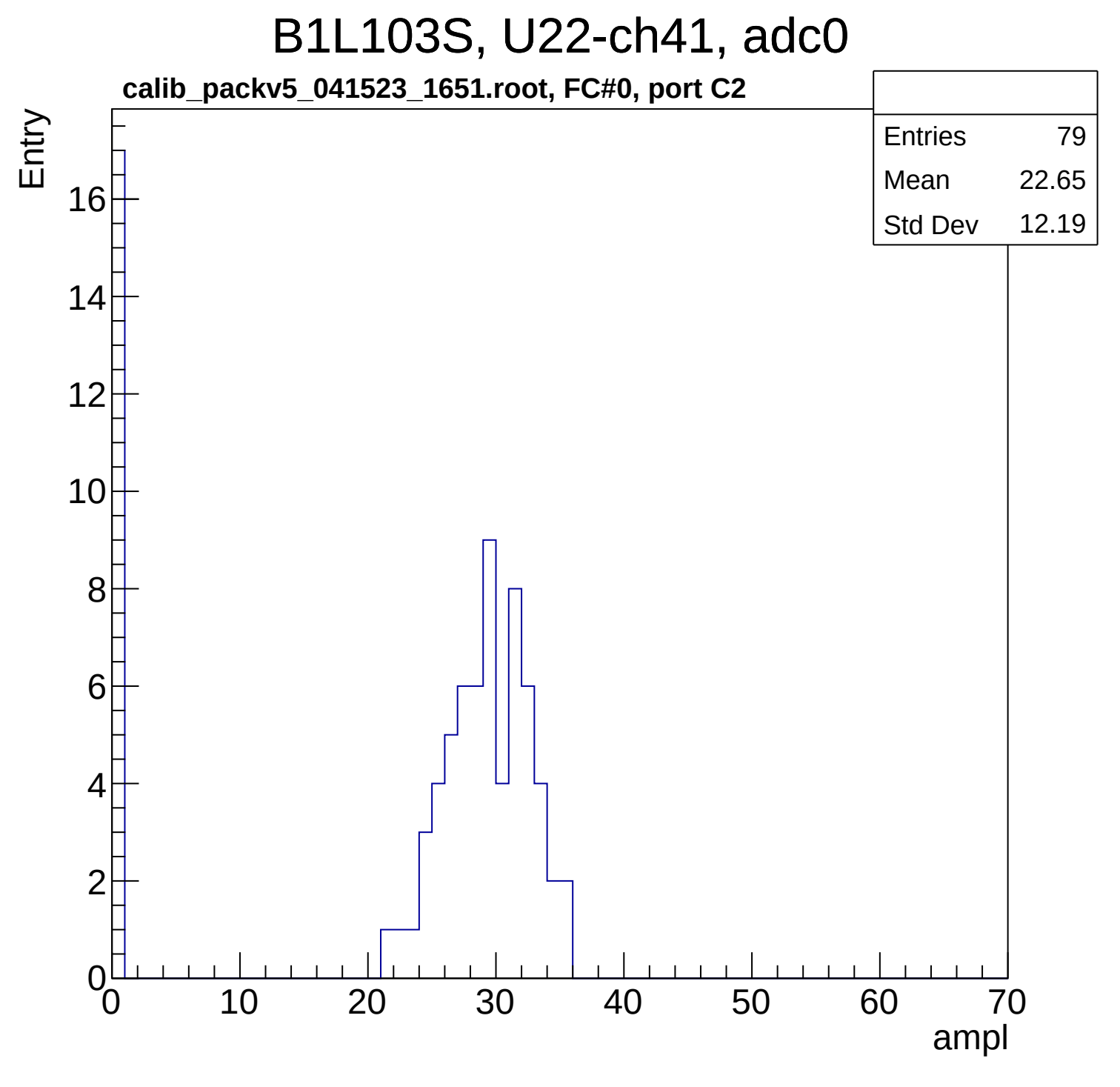
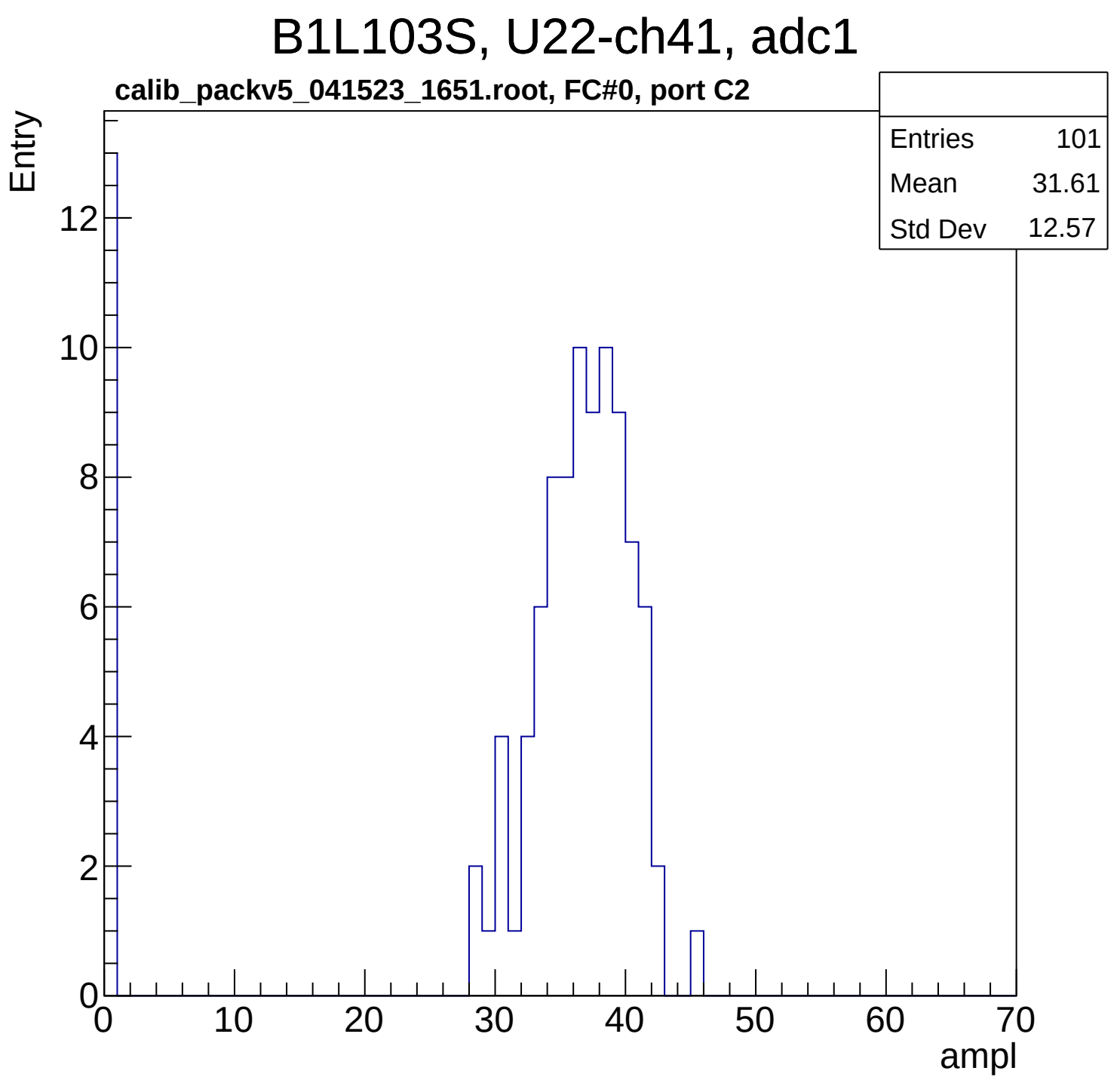
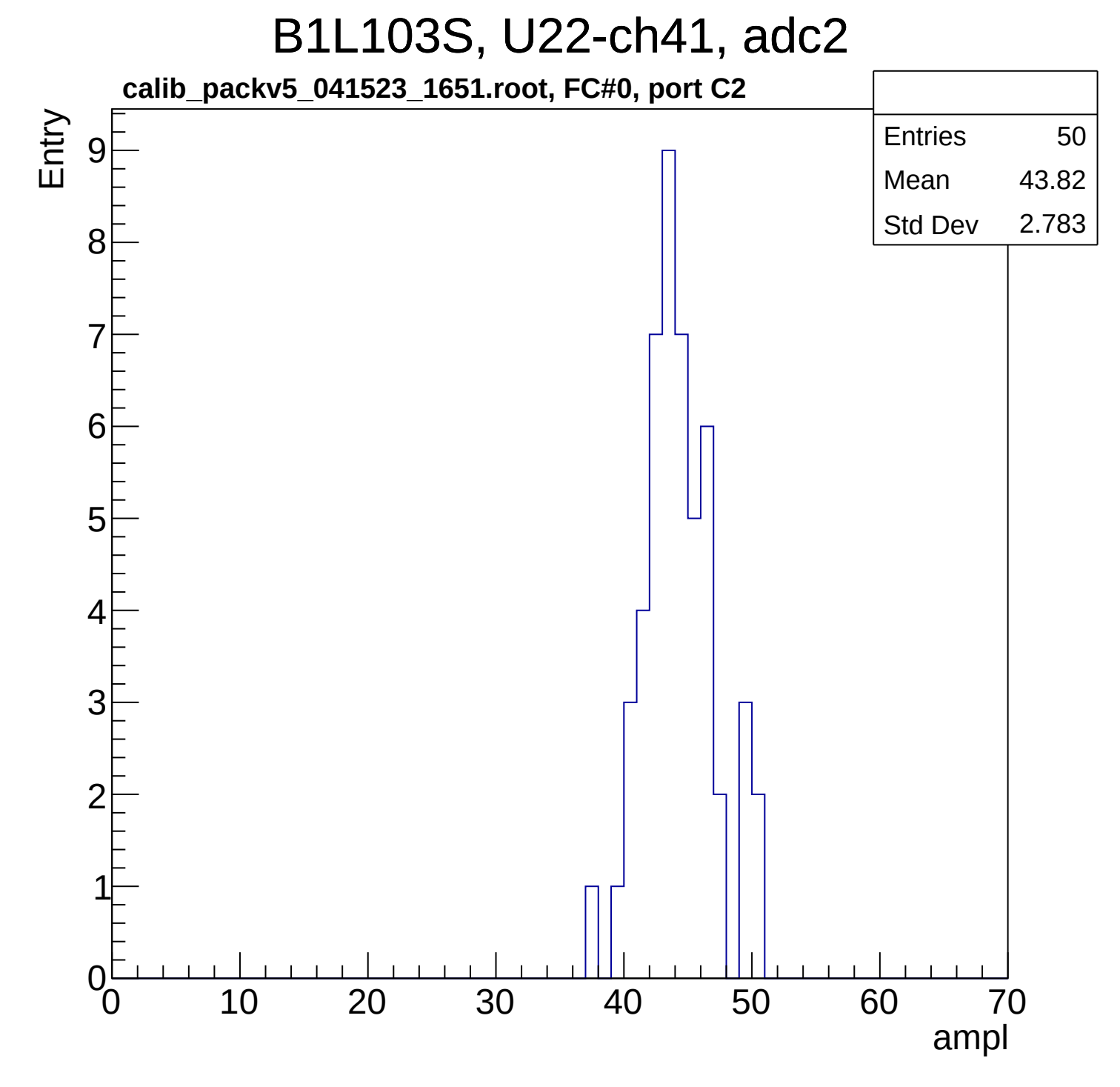

B1L103S, U22-ch40, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3
Std Dev 13.08
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch41, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 22.65
Std Dev 12.19
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch41, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 101
Mean 31.61
Std Dev 12.57
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch41, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 43.82
Std Dev 2.783
Entry
ampl
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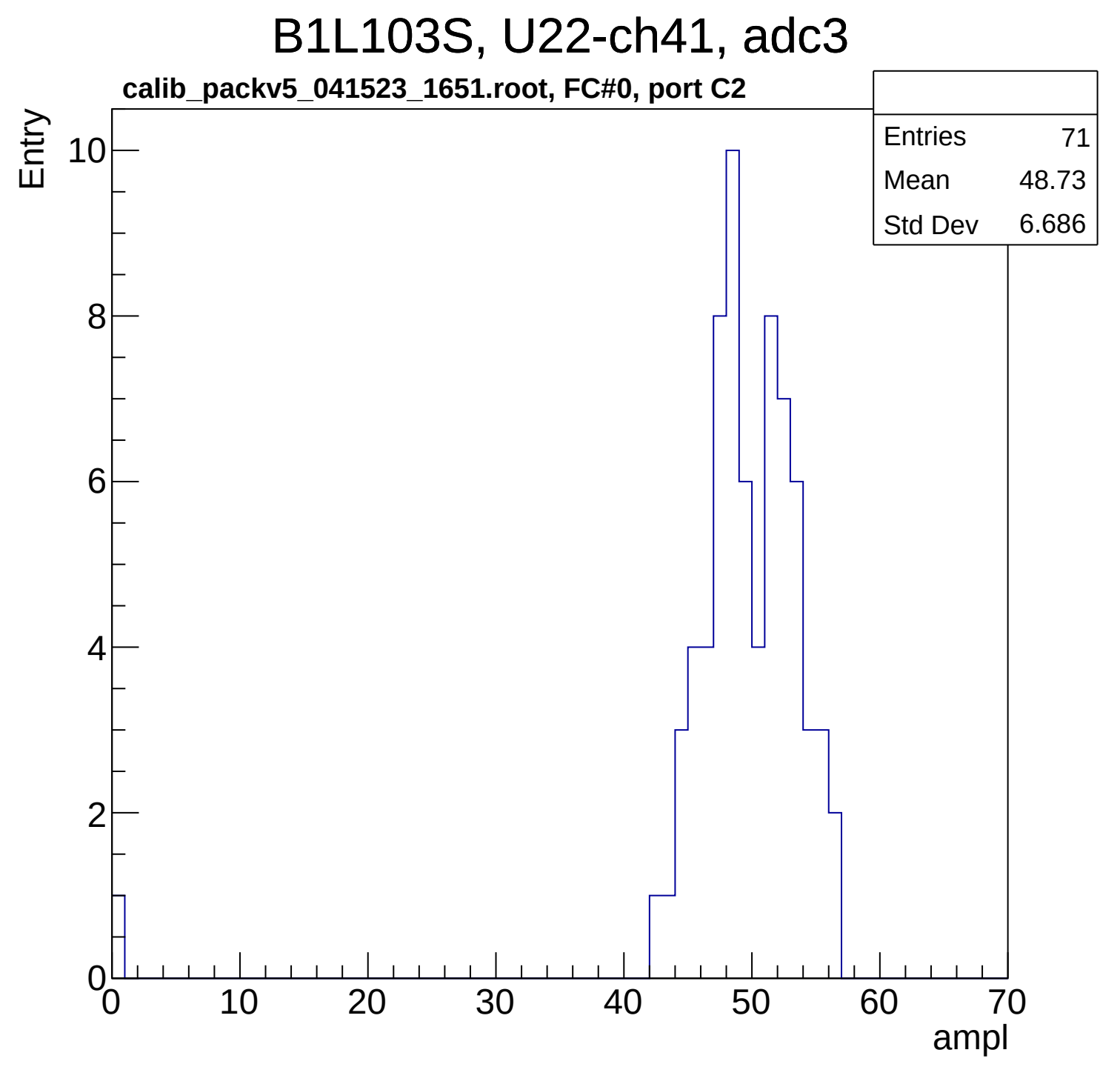
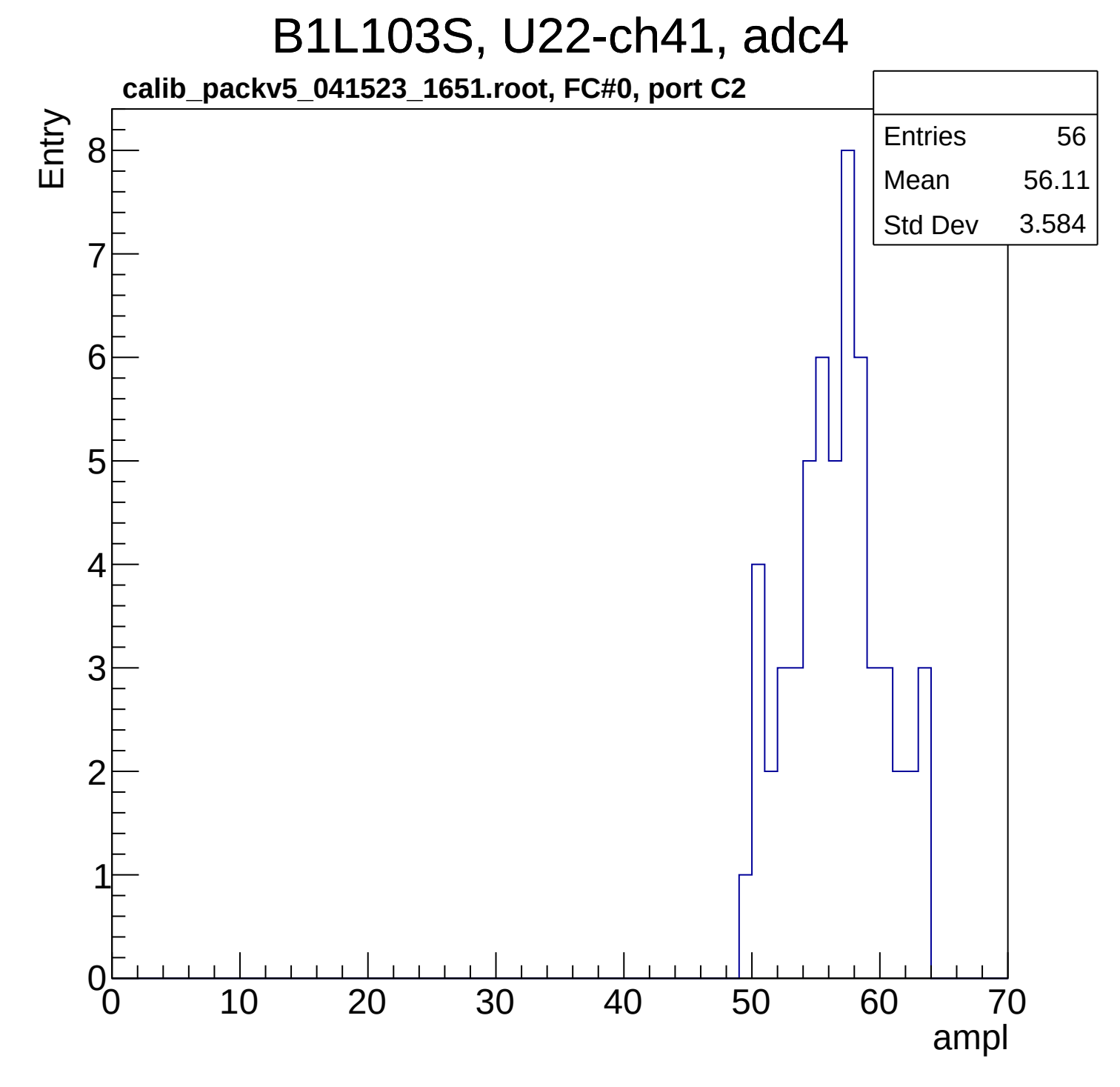
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch41, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 48.73
Std Dev 6.686
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U22-ch41, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 56.11
Std Dev 3.584
Entry
ampl
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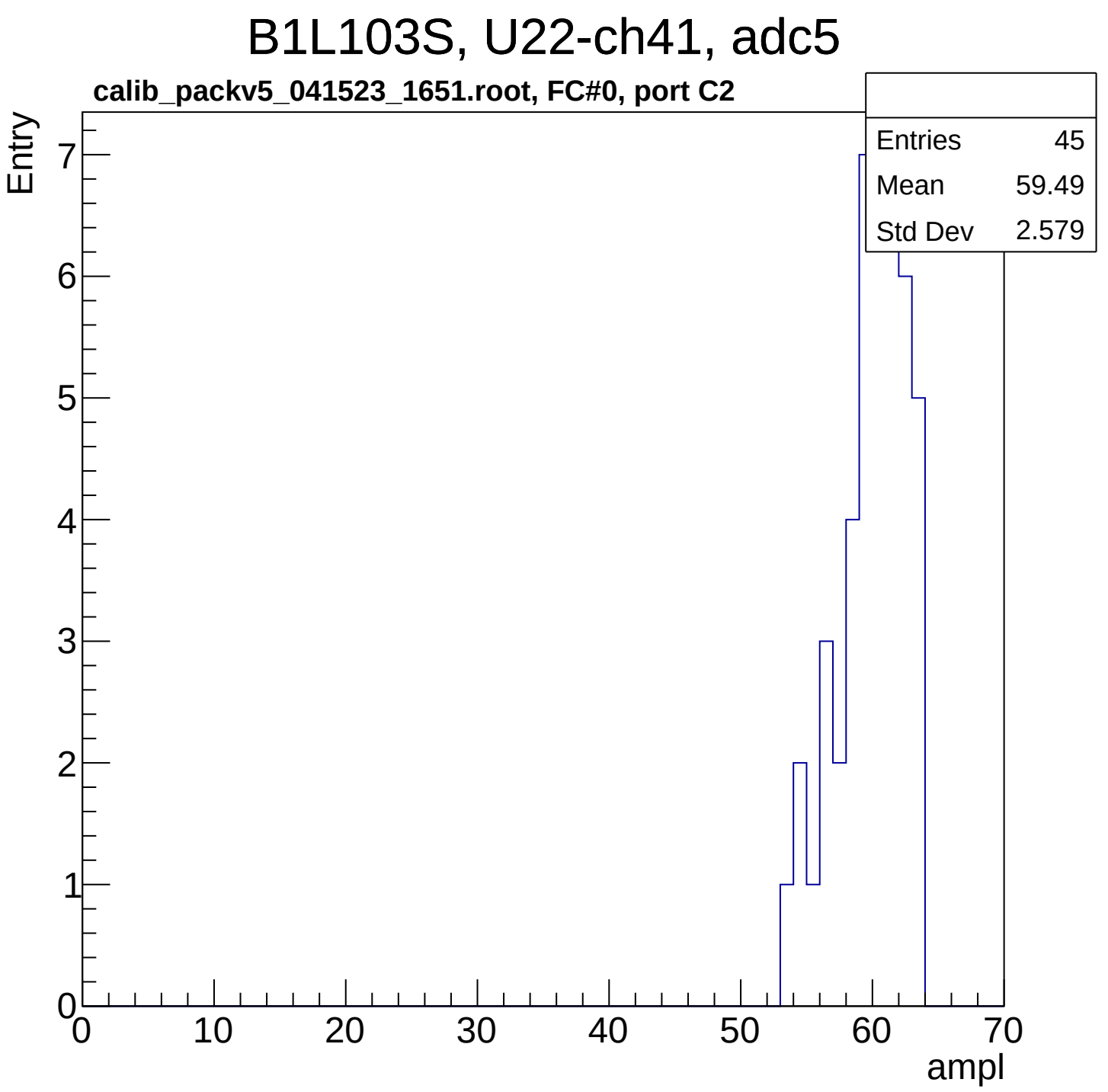
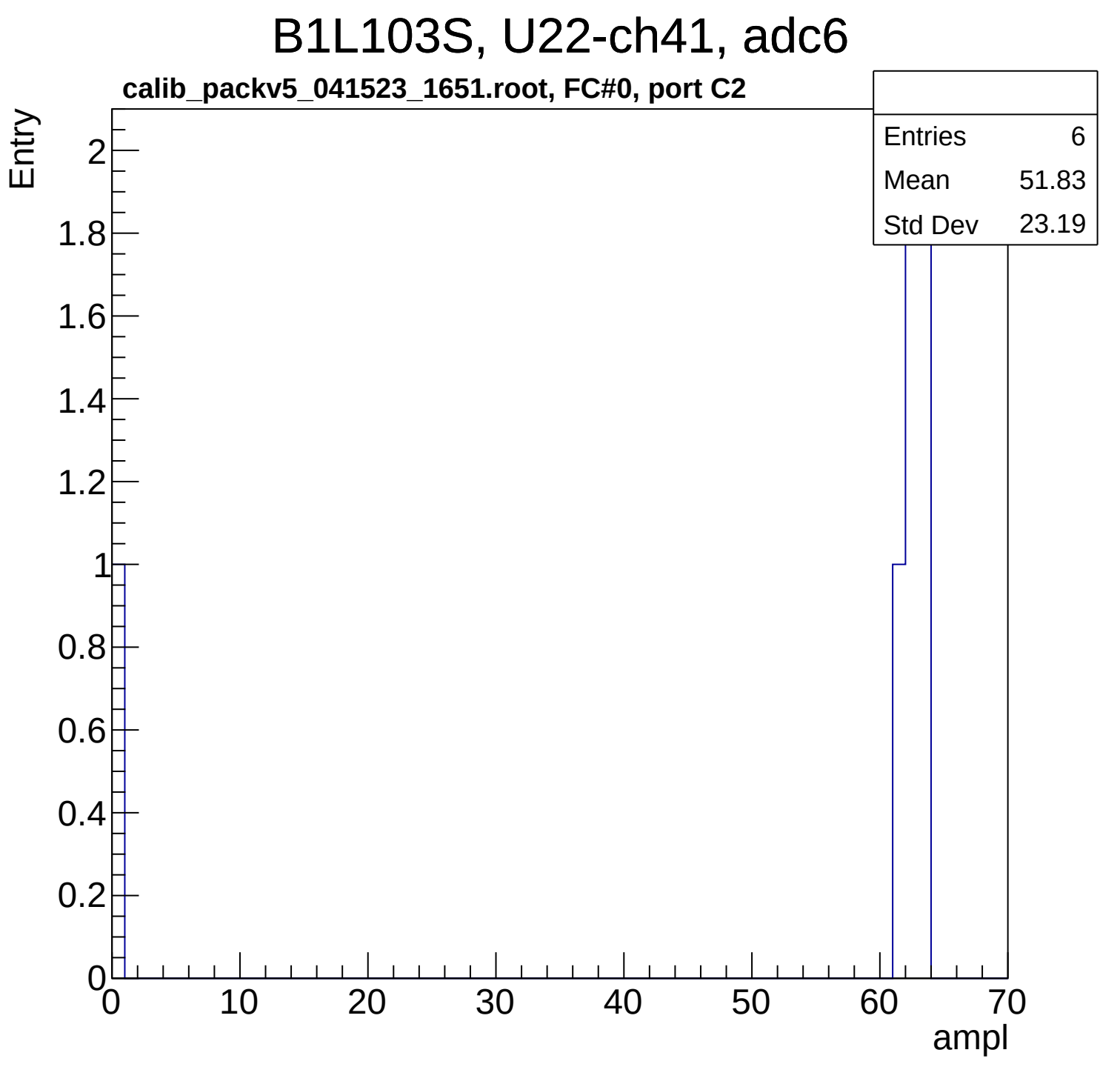
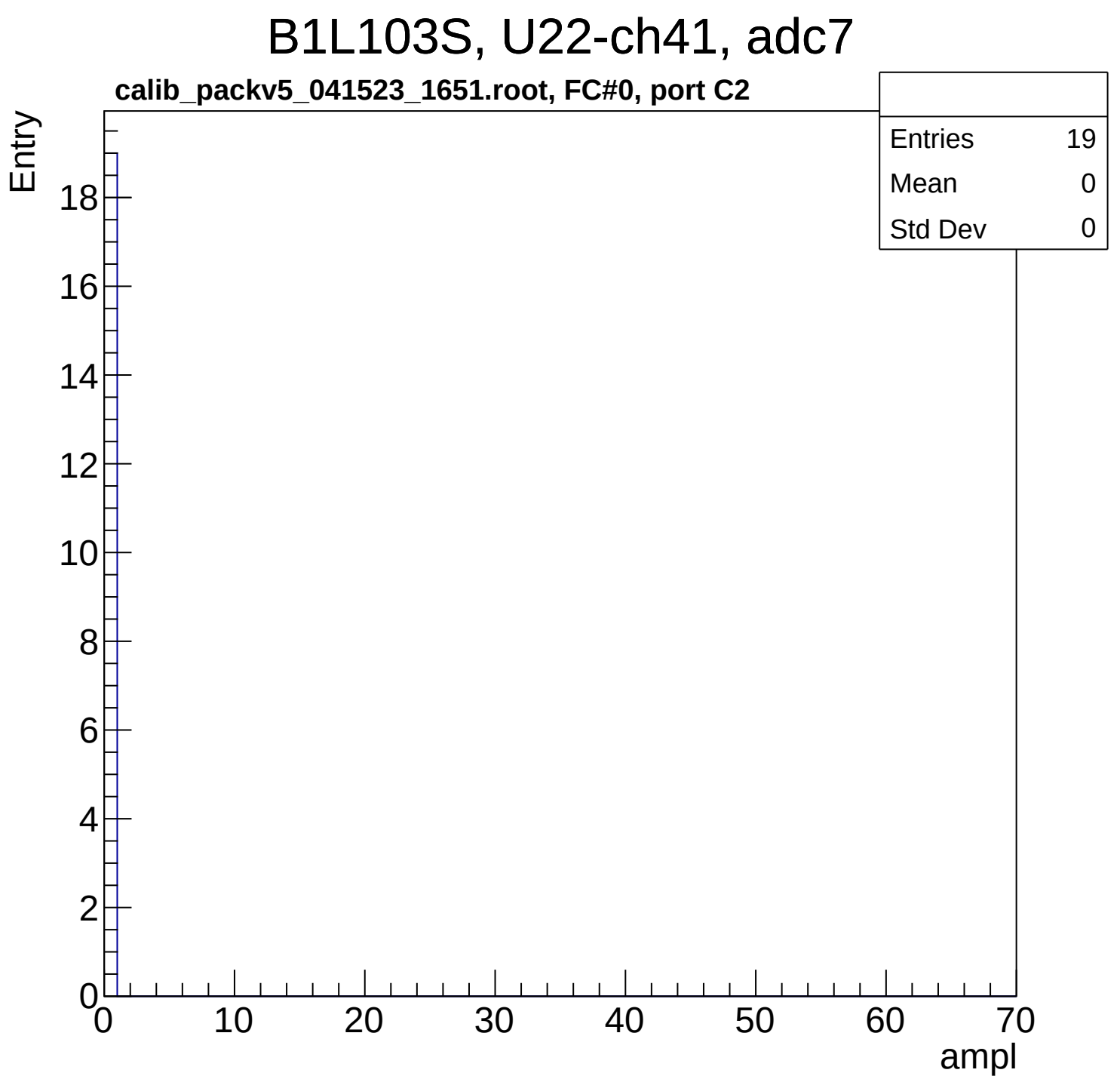
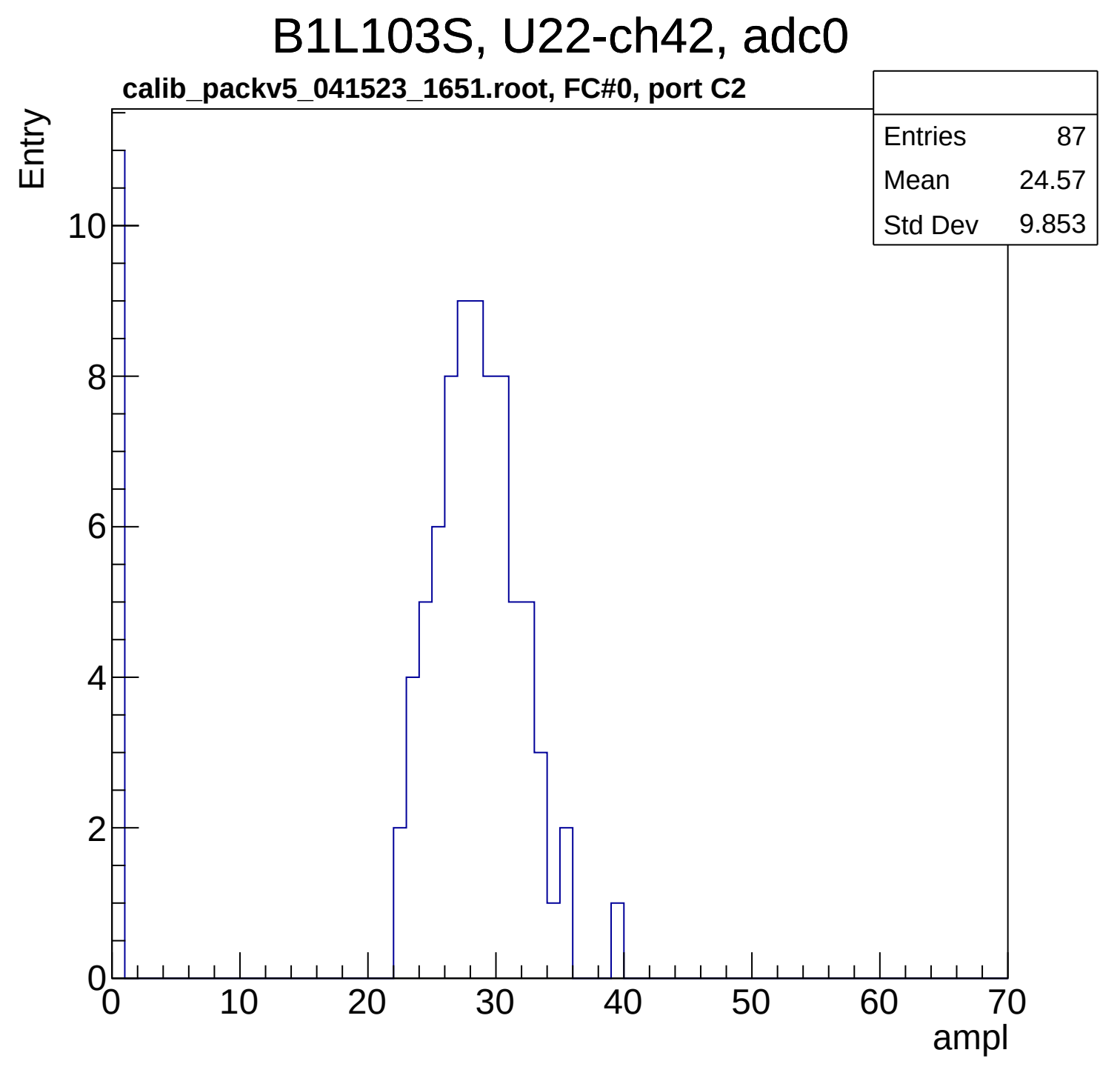
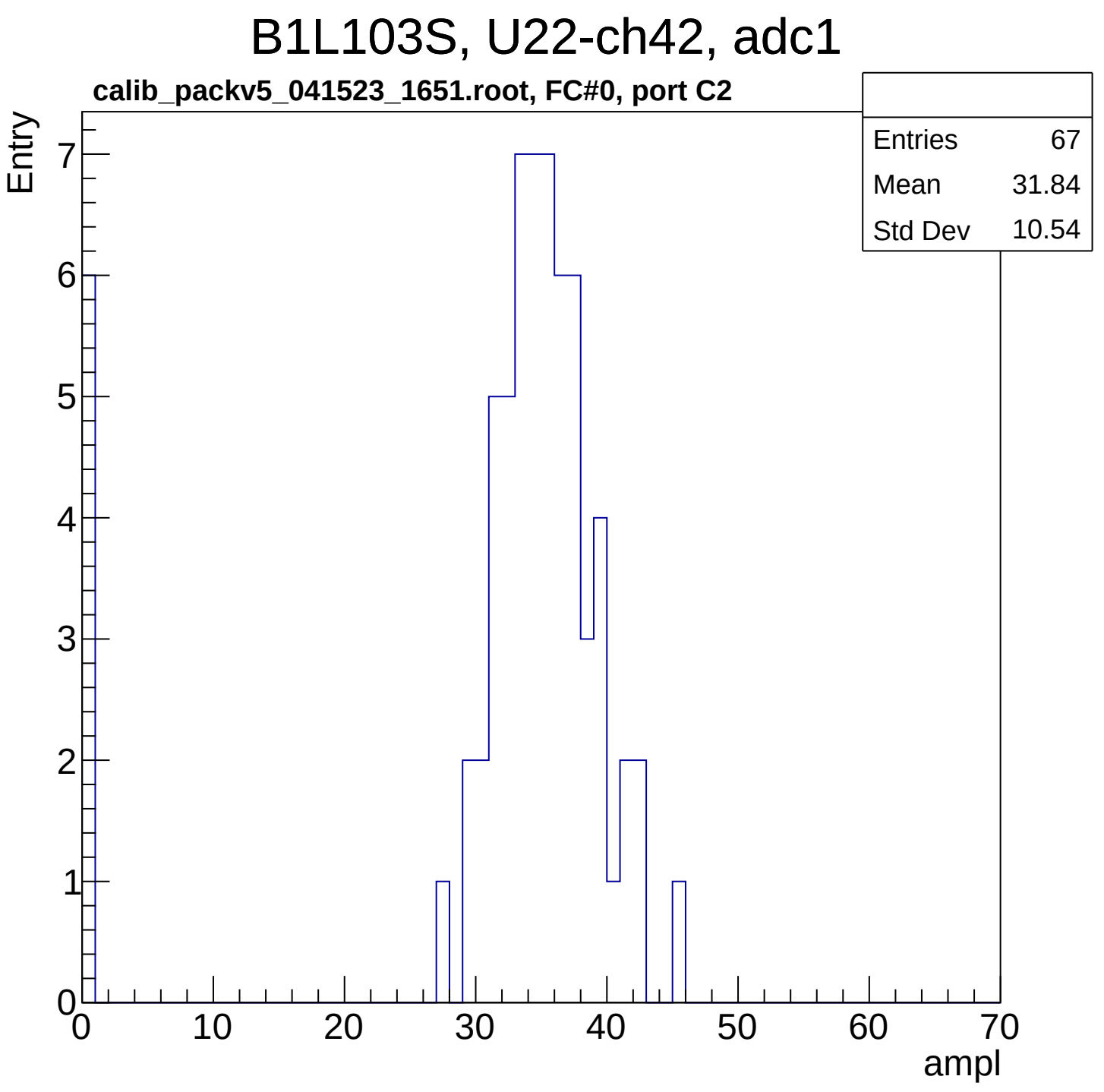
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

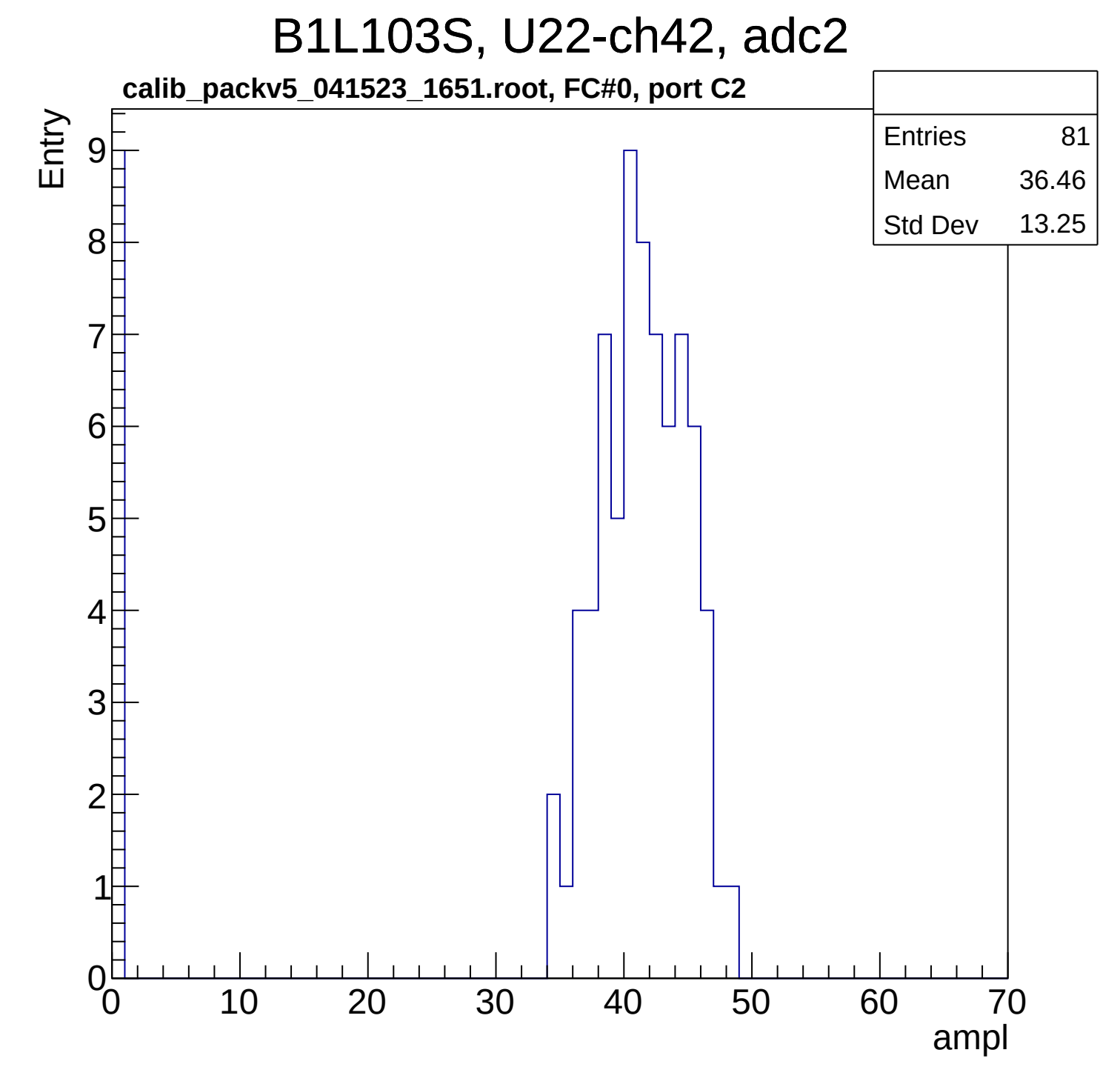

B1L103S, U22-ch41, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 59.49
Std Dev 2.579
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U22-ch41, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 51.83
Std Dev 23.19
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U22-ch41, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch42, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 24.57
Std Dev 9.853
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U22-ch42, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 31.84
Std Dev 10.54
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U22-ch42, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 36.46
Std Dev 13.25
Entry
ampl
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2
3
4
5
6
7
8
9
0
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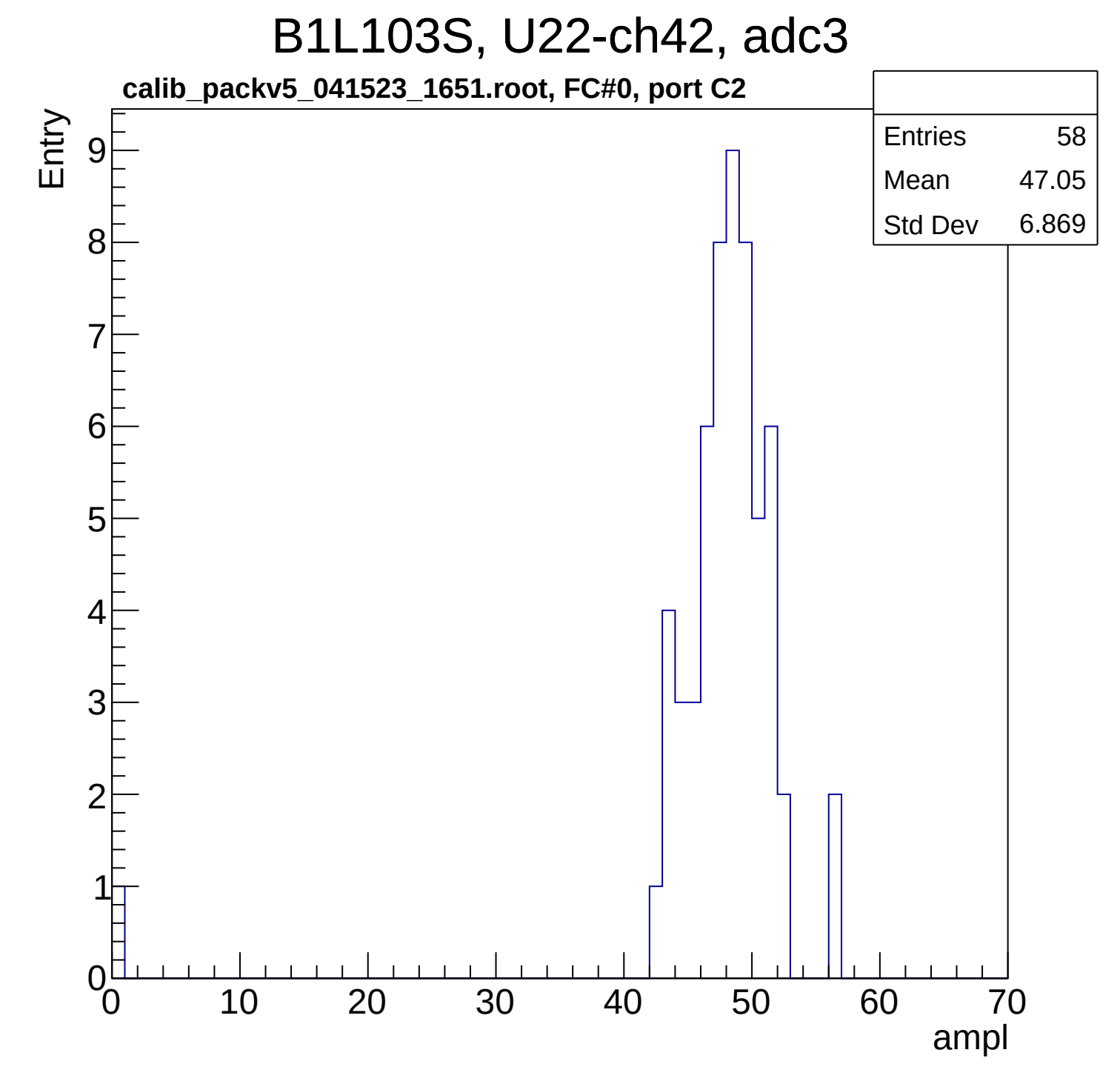
20
30
40
50
60
70


B1L103S, U22-ch42, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 47.05
Std Dev 6.869
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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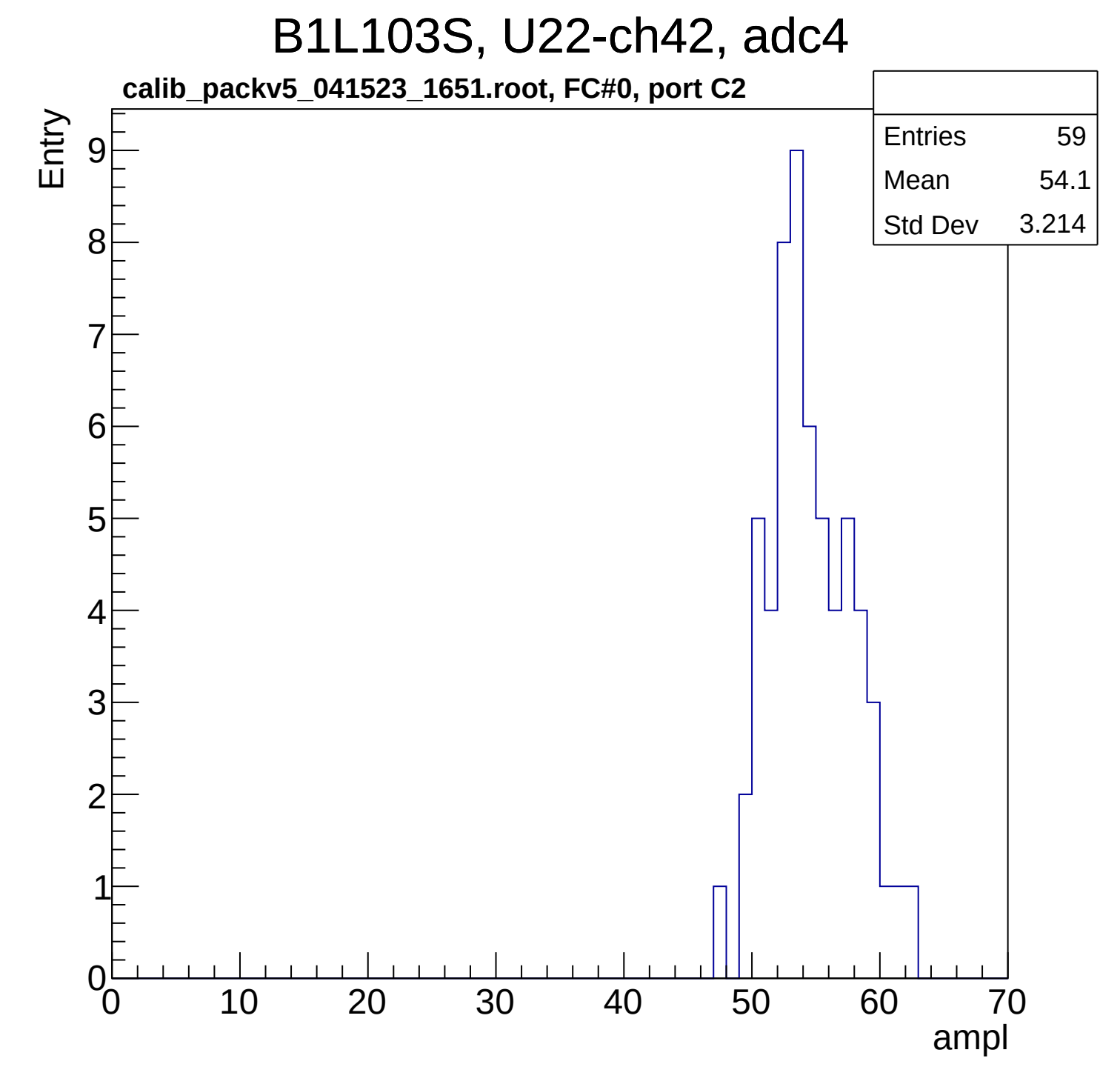
B1L103S, U22-ch42, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 54.1
Std Dev 3.214
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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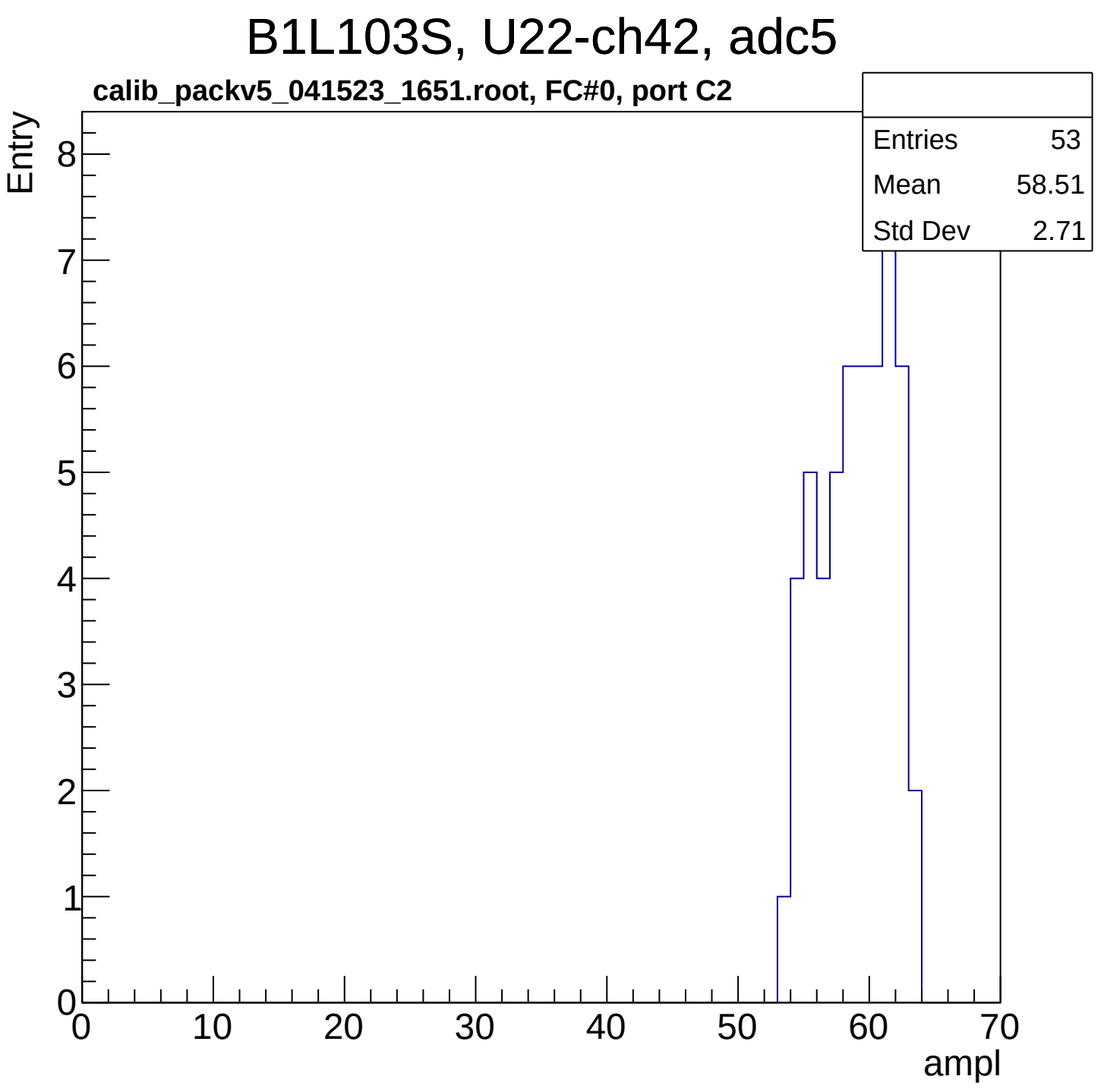
60
70


B1L103S, U22-ch42, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 58.51
Std Dev 2.71
Entry
ampl
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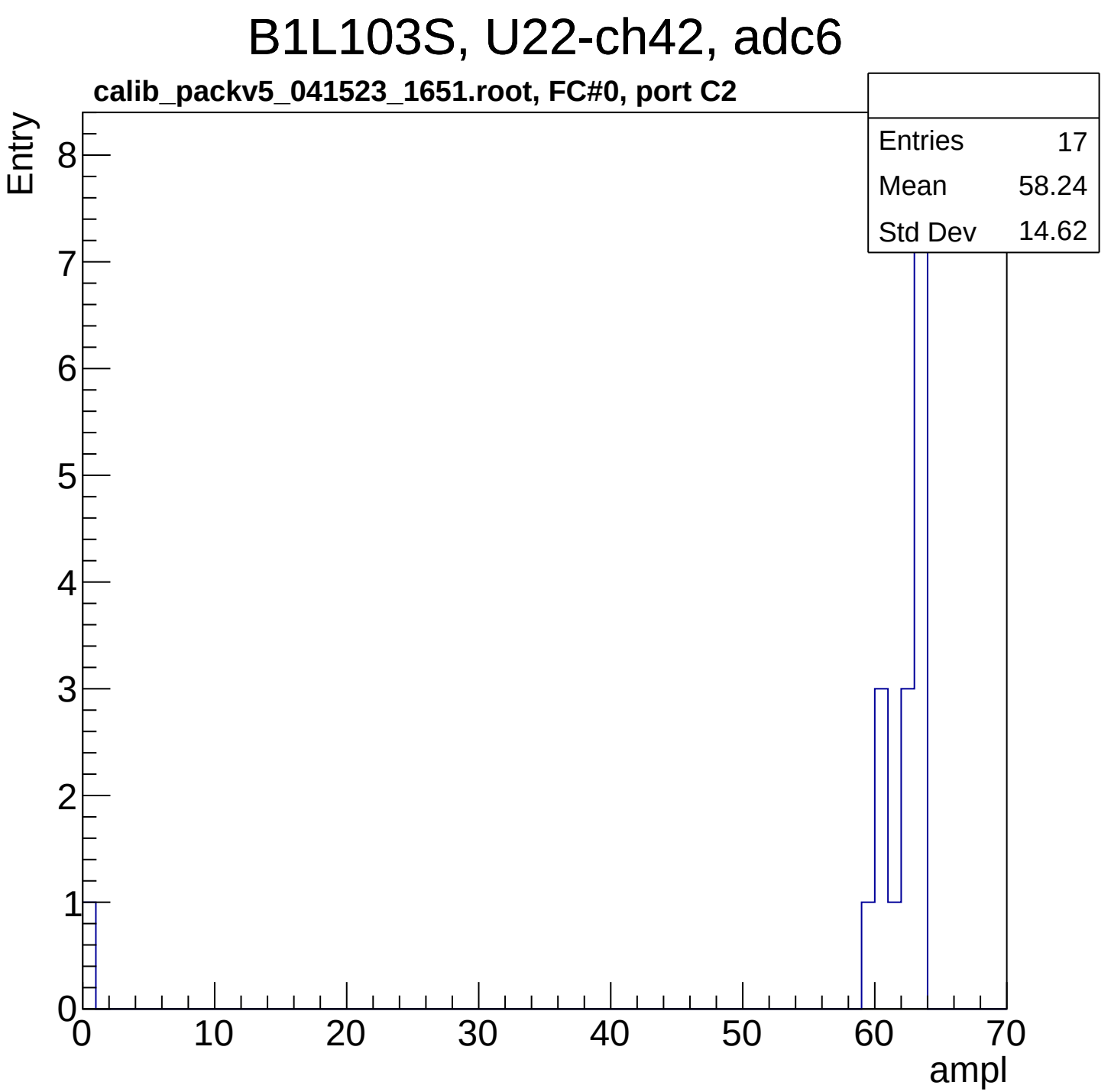
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch42, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 58.24
Std Dev 14.62
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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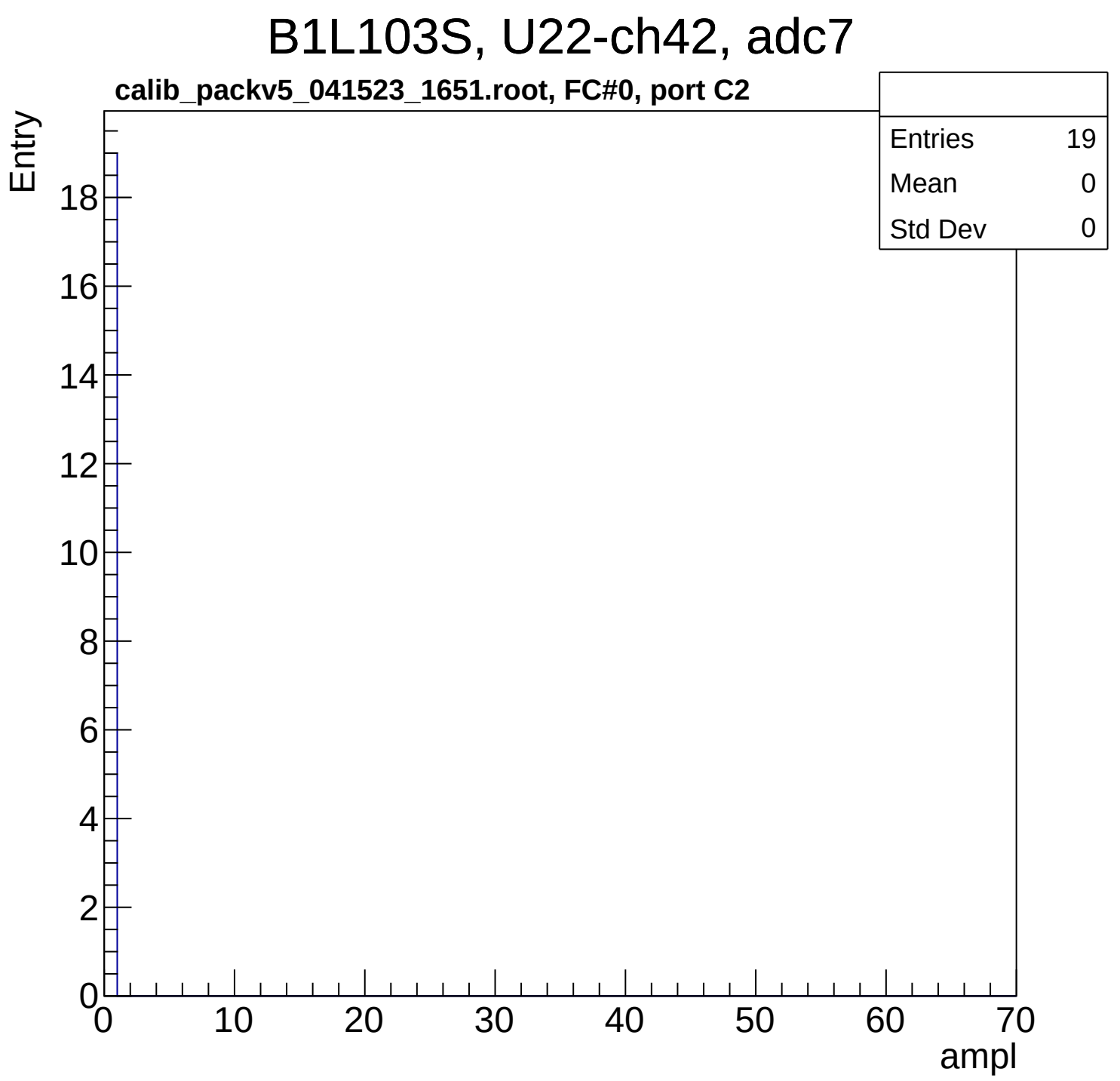
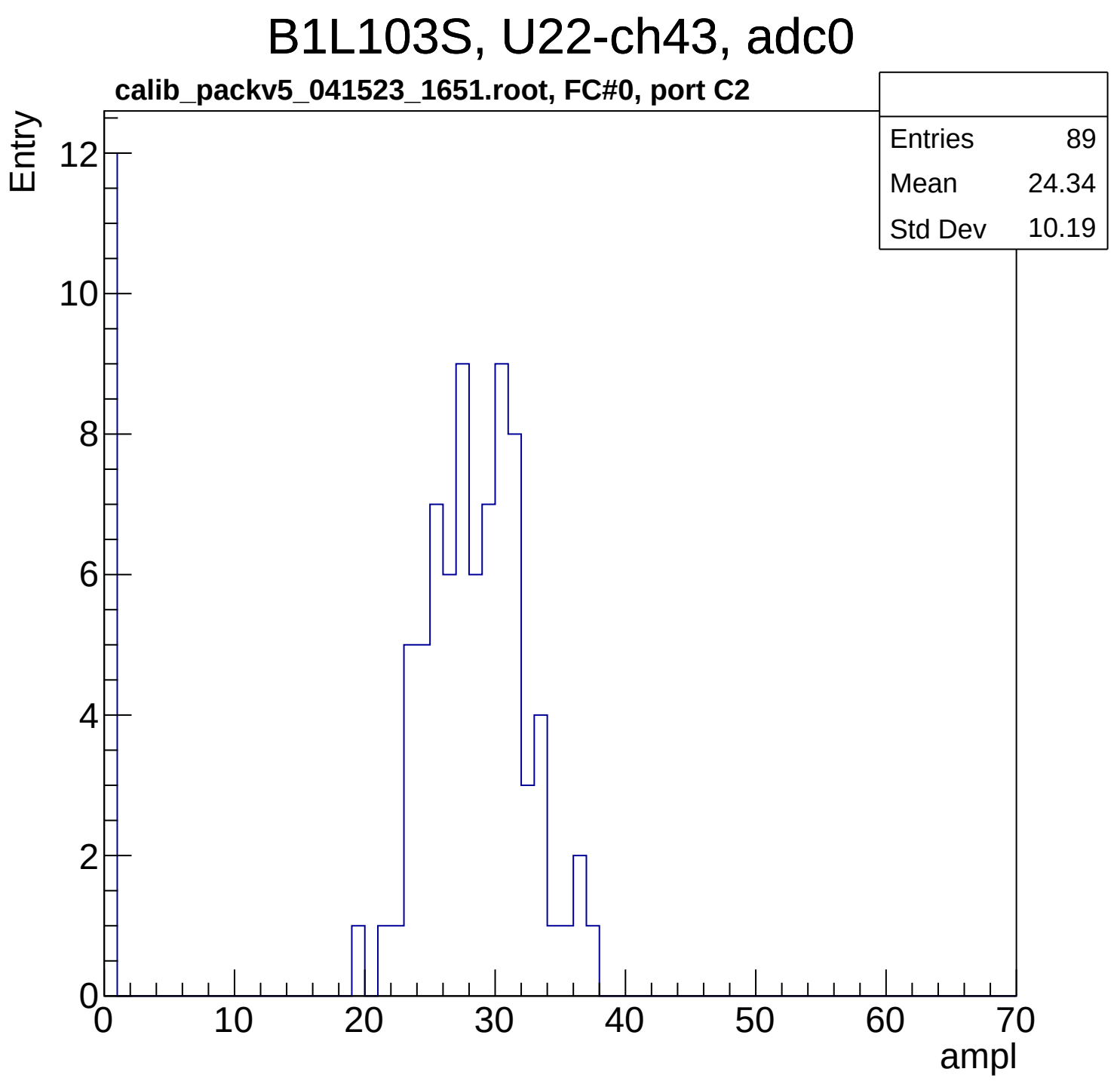
60
70


B1L103S, U22-ch42, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch43, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 24.34
Std Dev 10.19
Entry
ampl
0
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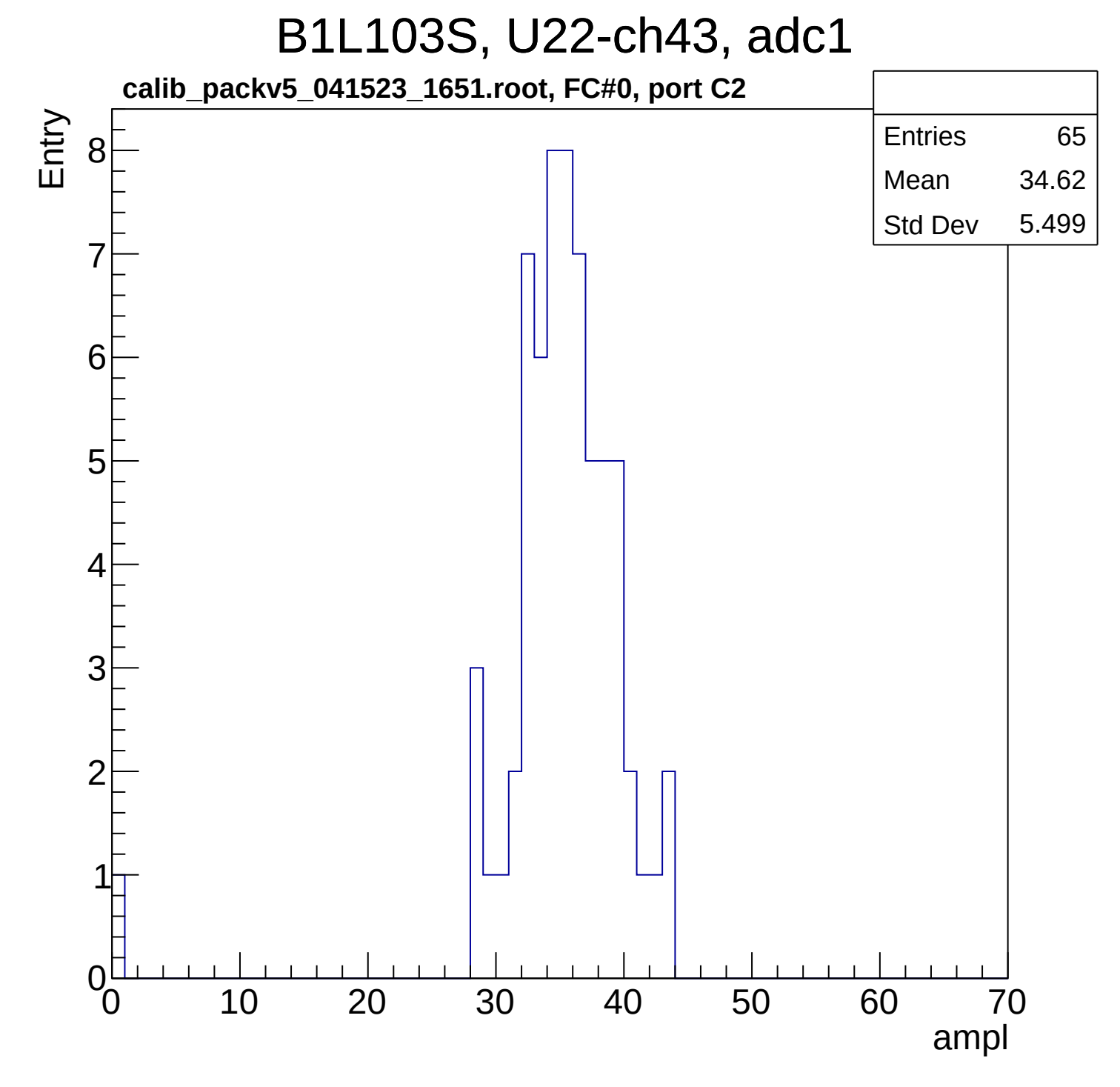
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U22-ch43, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 34.62
Std Dev 5.499
Entry
ampl
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4
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6
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0
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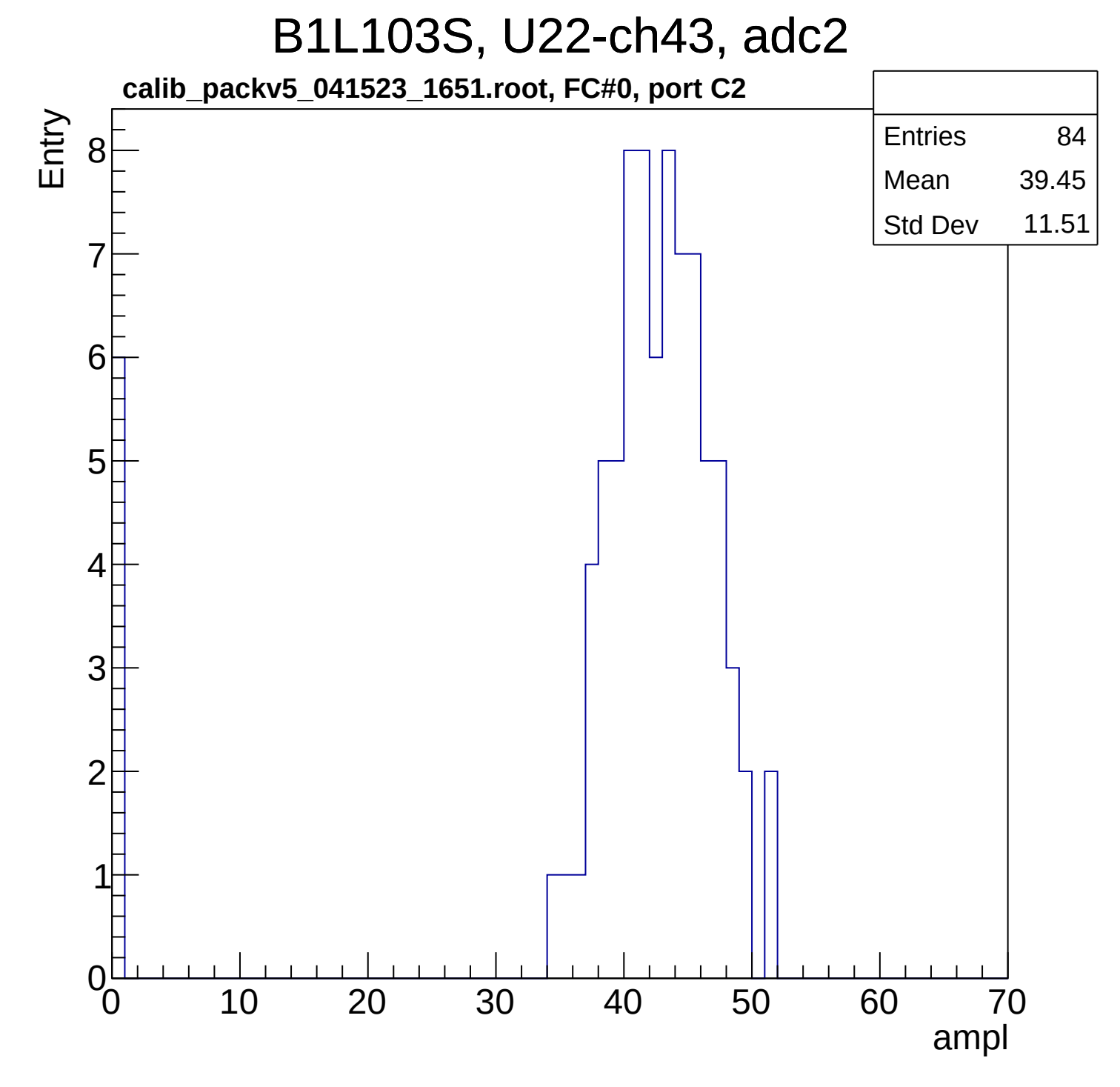
60
70


B1L103S, U22-ch43, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 39.45
Std Dev 11.51
Entry
ampl
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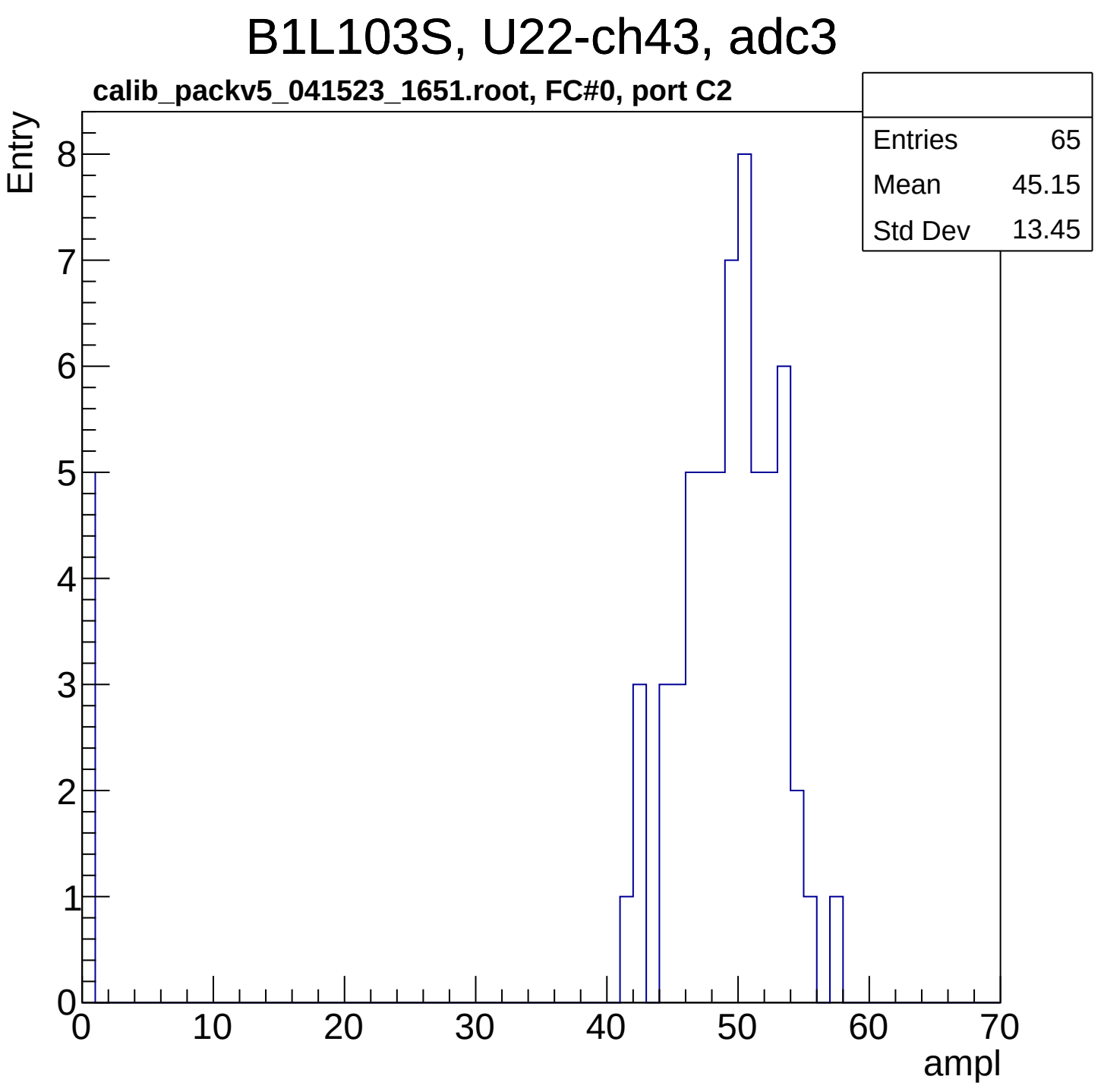
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch43, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 45.15
Std Dev 13.45
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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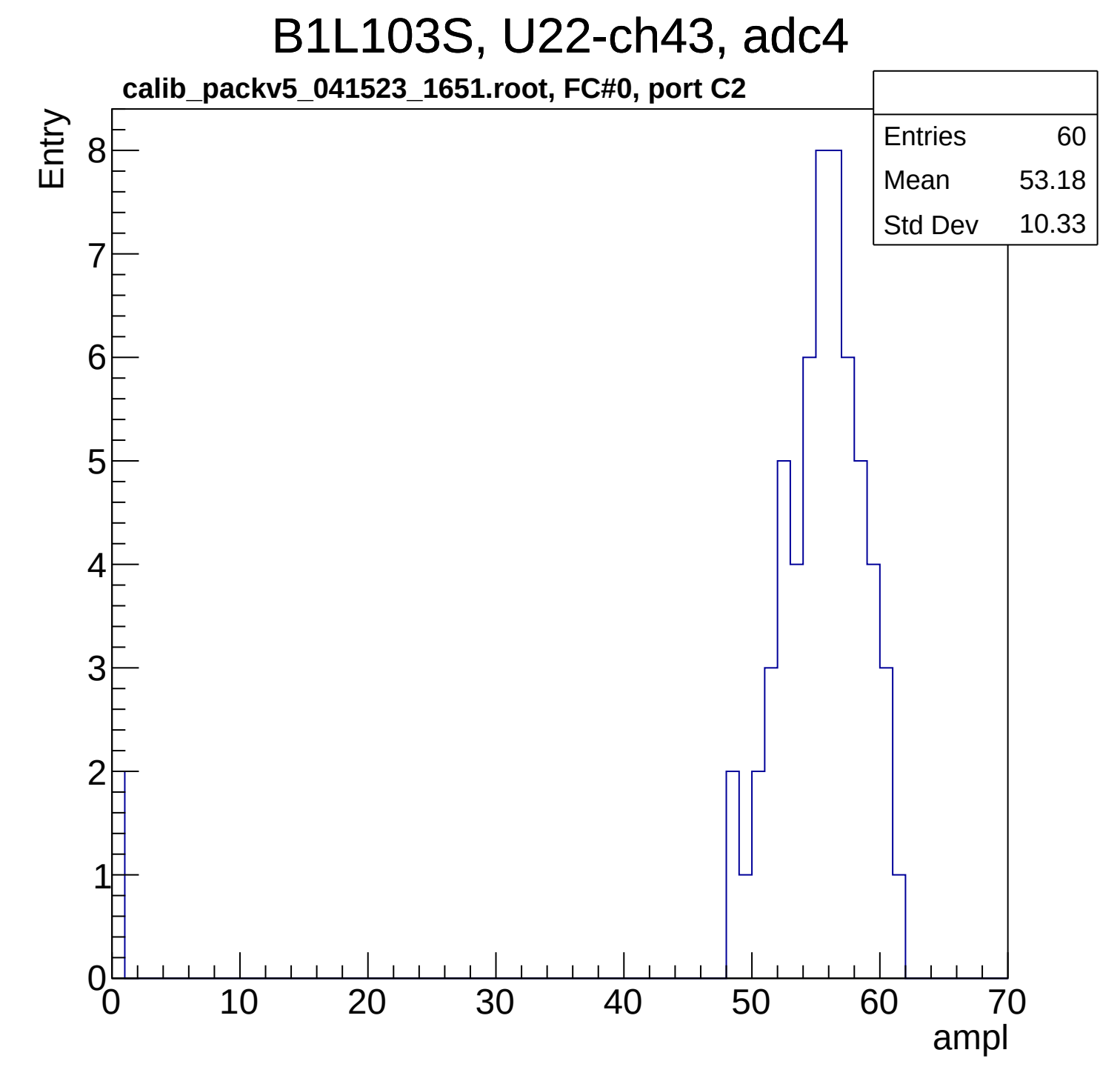
40
50
60
70


B1L103S, U22-ch43, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 53.18
Std Dev 10.33
Entry
ampl
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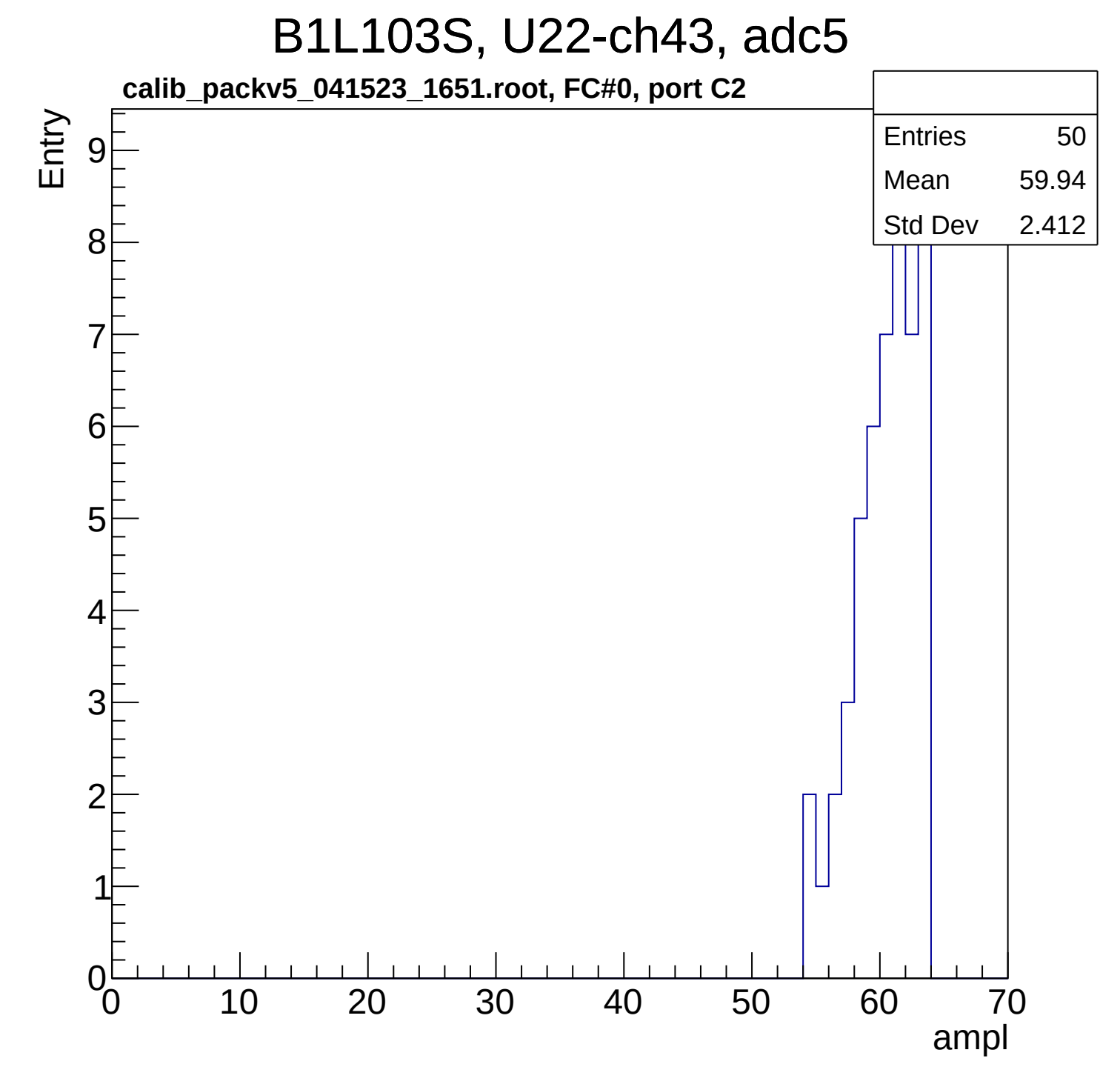
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch43, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 59.94
Std Dev 2.412
Entry
ampl
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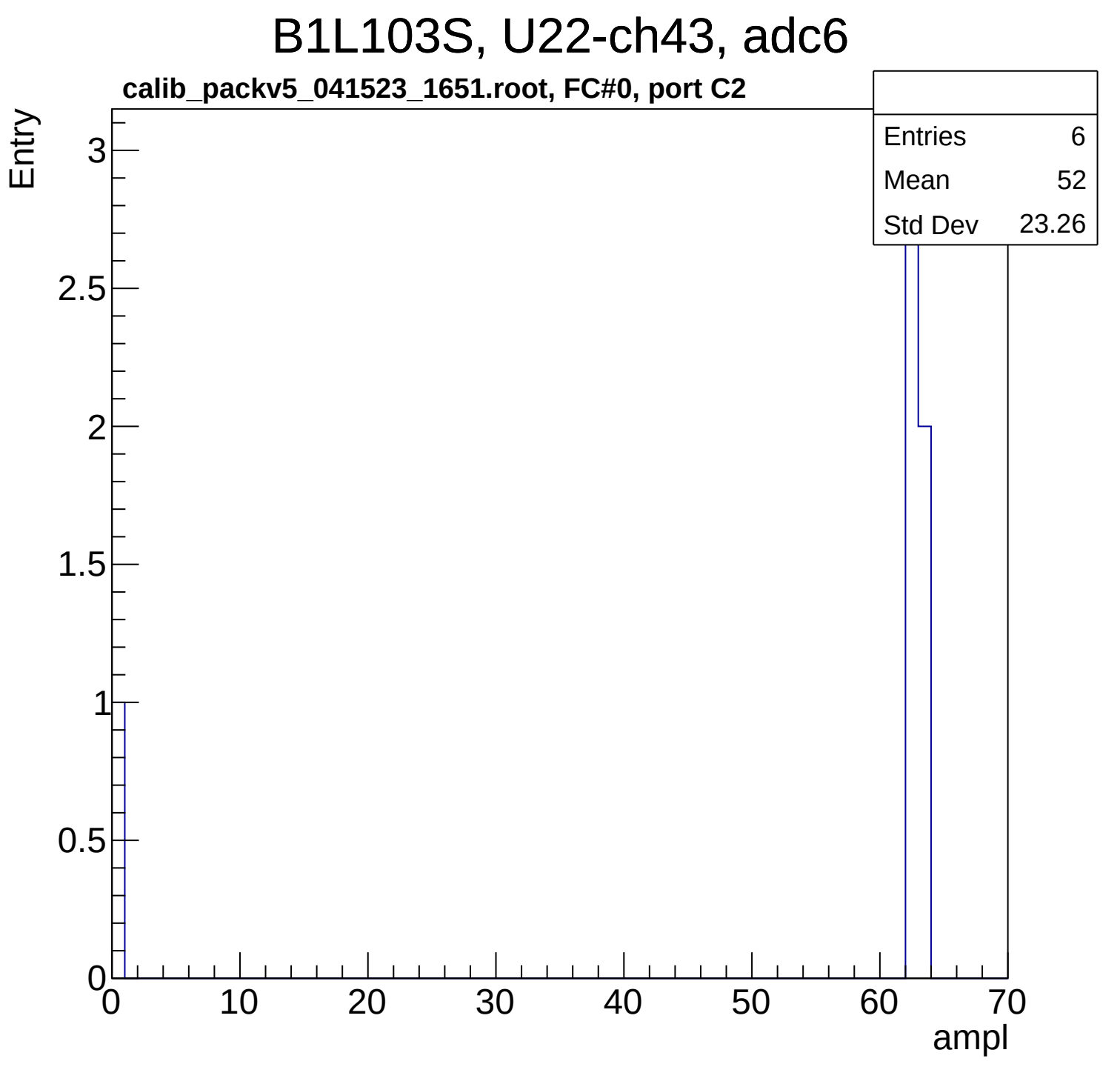
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch43, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 52
Std Dev 23.26
Entry
ampl
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0.5
1
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2
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3
0
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60
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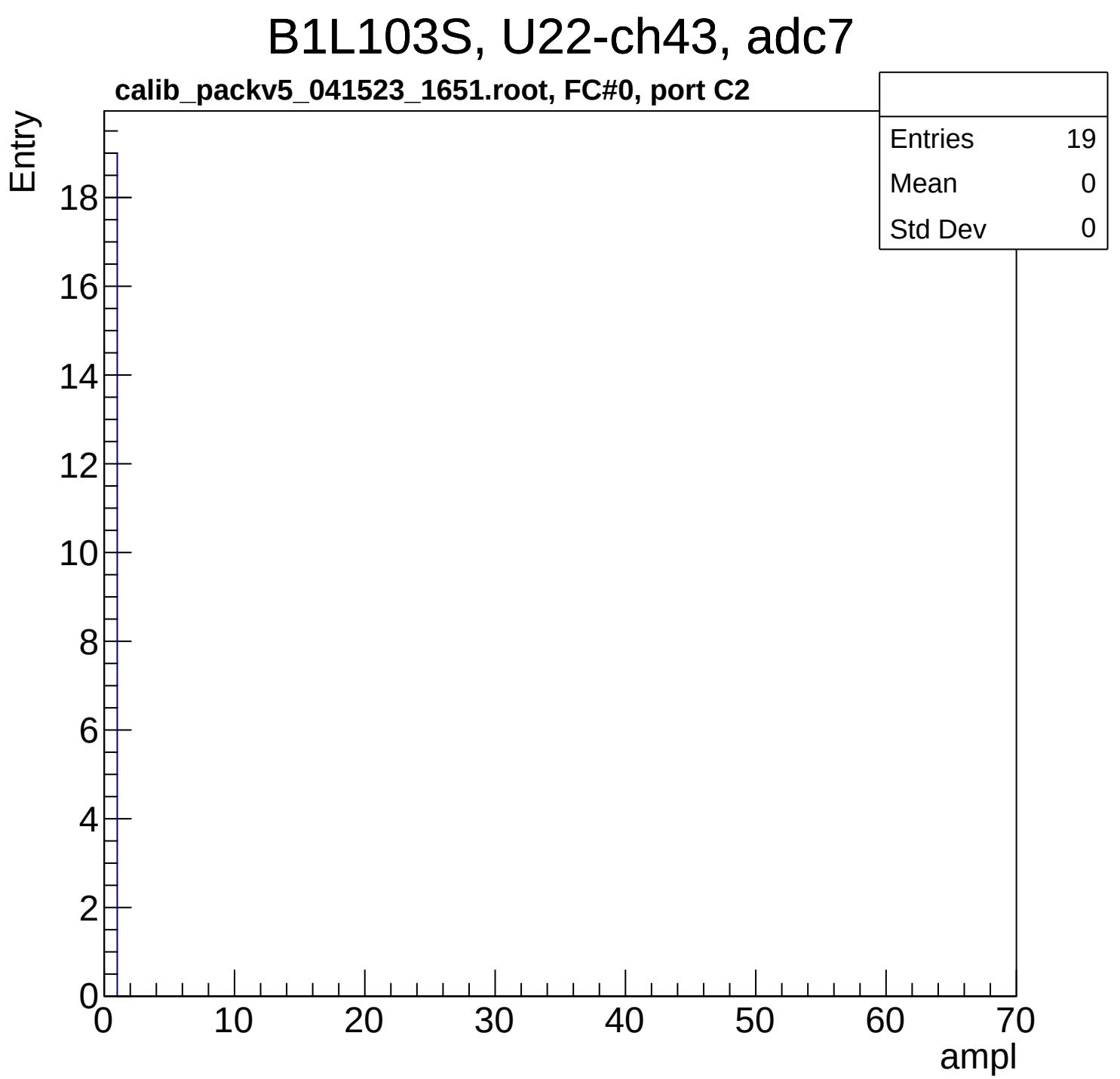
B1L103S, U22-ch43, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
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6
8
10
12
14
16
18
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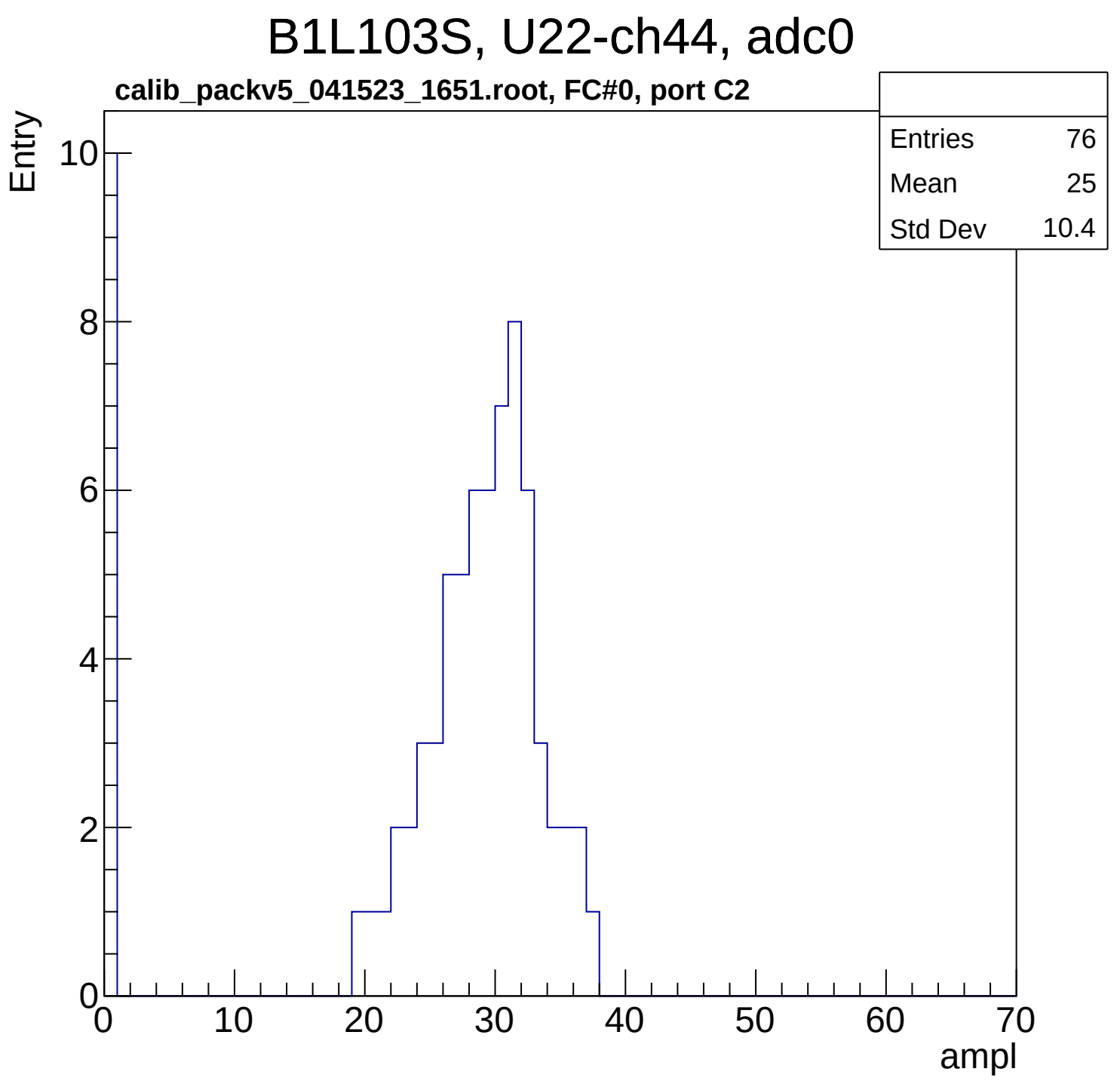
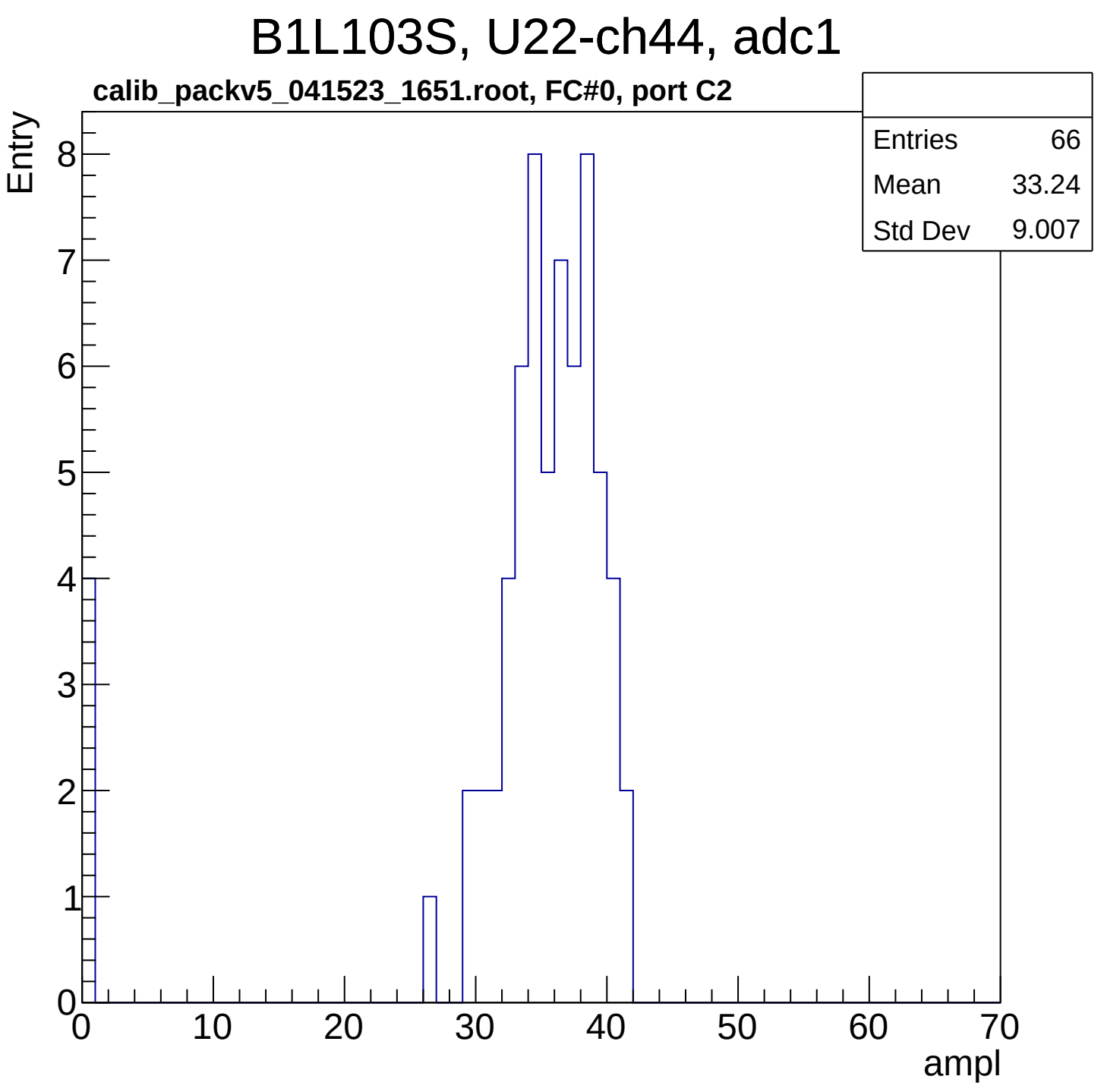
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch44, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 25
Std Dev 10.4
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch44, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 33.24
Std Dev 9.007
Entry
ampl
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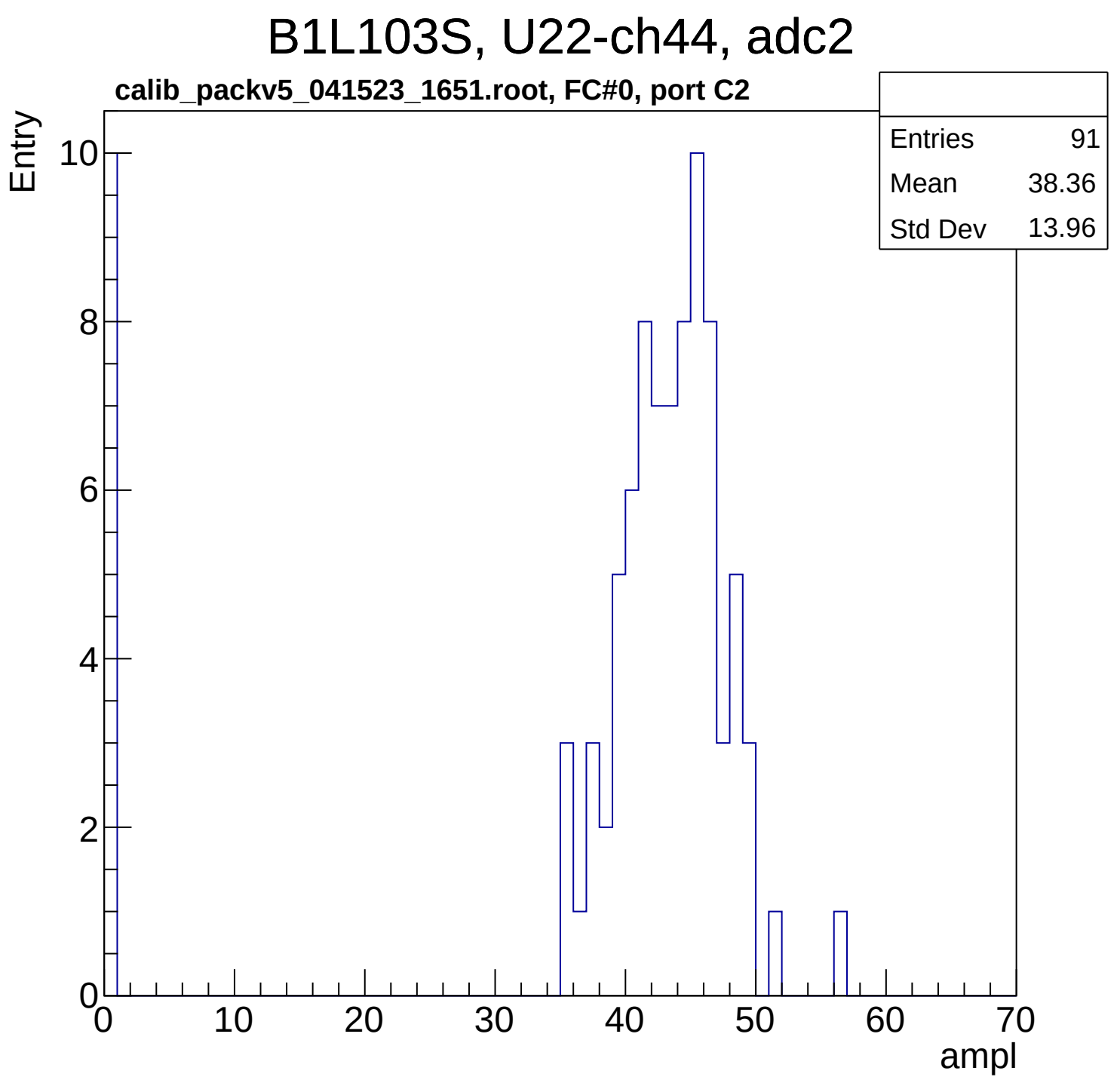
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch44, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 38.36
Std Dev 13.96
Entry
ampl
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4
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8
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0
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40
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60
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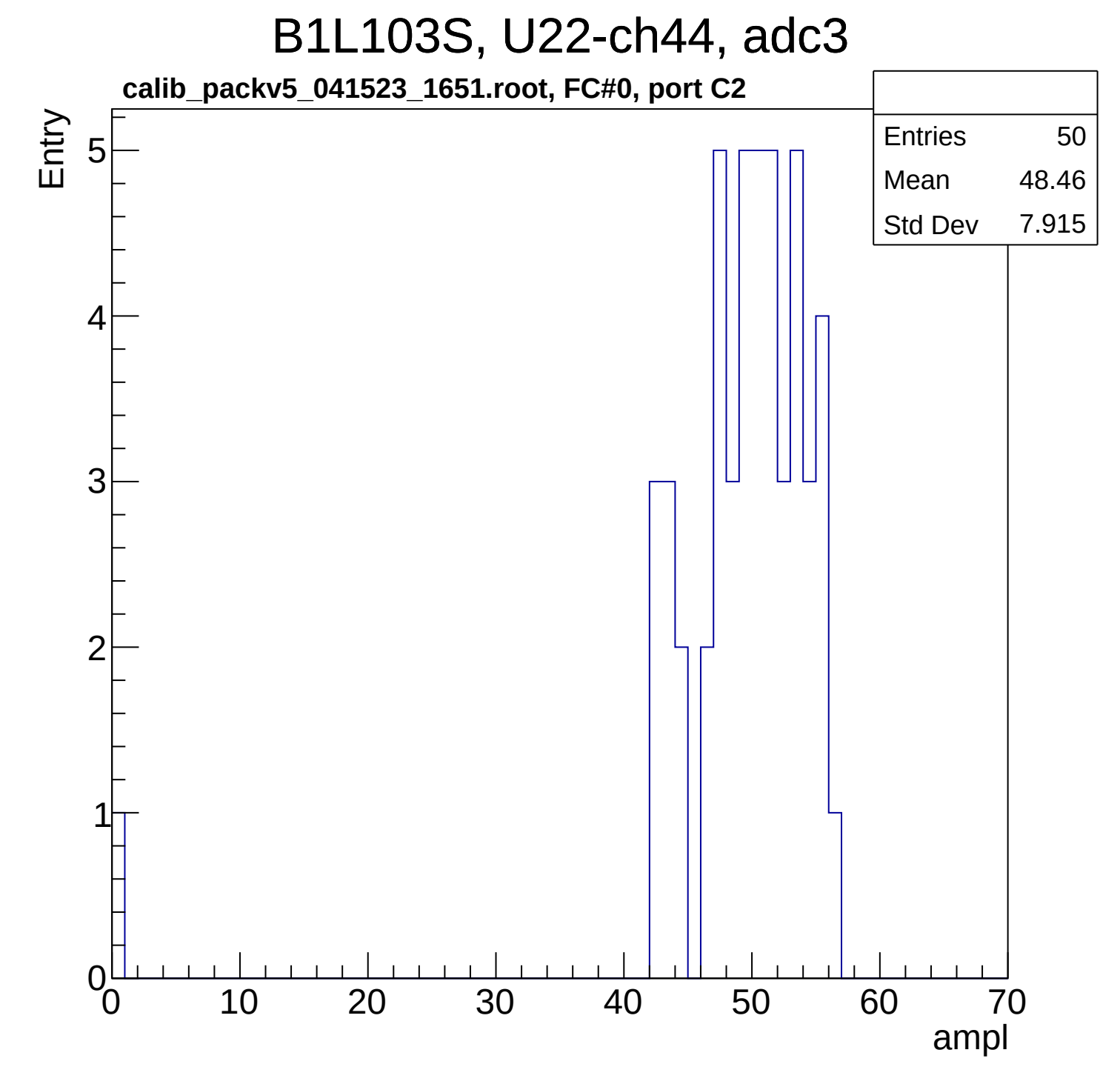
B1L103S, U22-ch44, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 48.46
Std Dev 7.915
Entry
ampl
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2
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4
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0
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20
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40
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60
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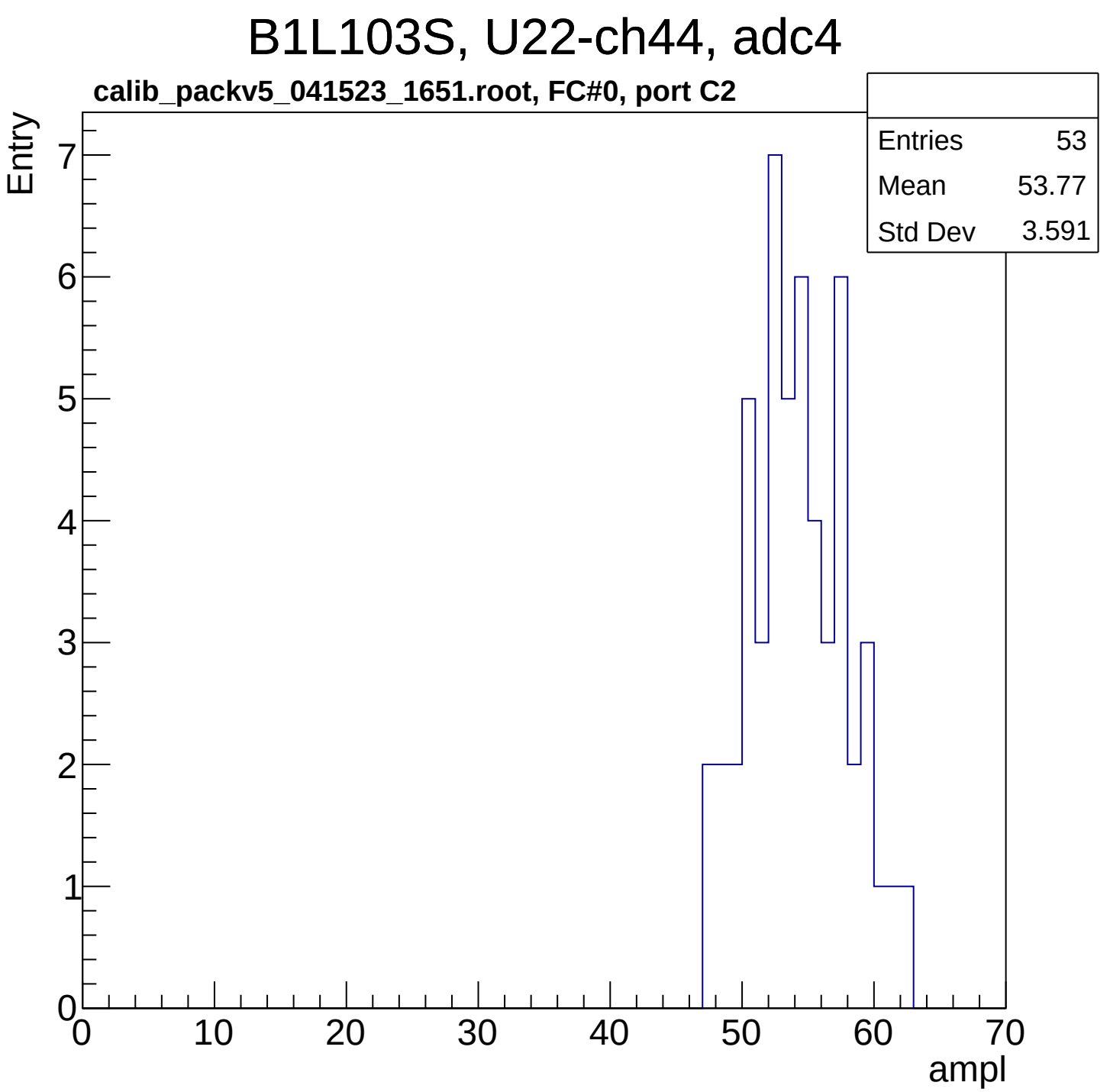
B1L103S, U22-ch44, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 53.77
Std Dev 3.591
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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40
50
60
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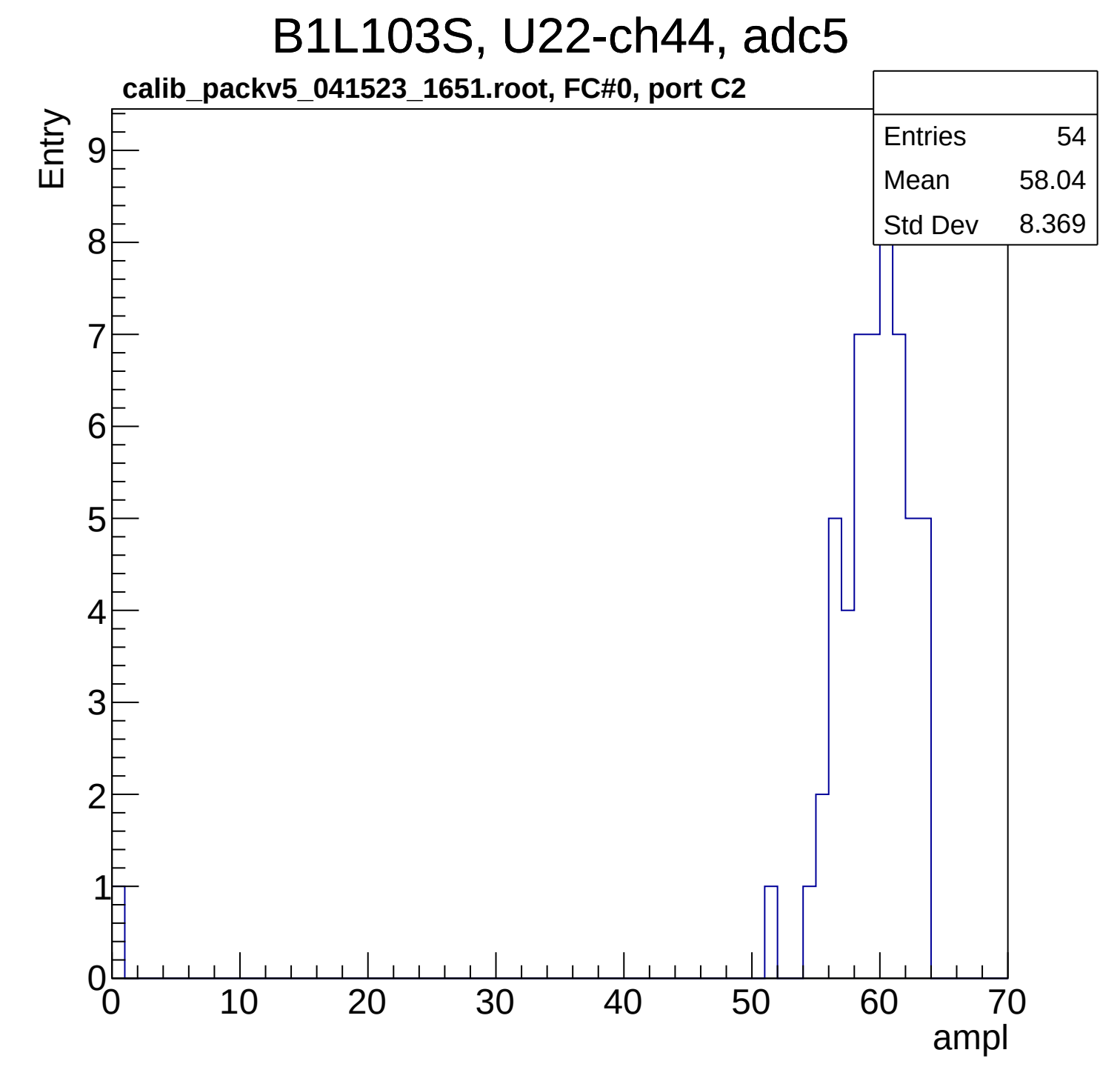
B1L103S, U22-ch44, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 58.04
Std Dev 8.369
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
50
60
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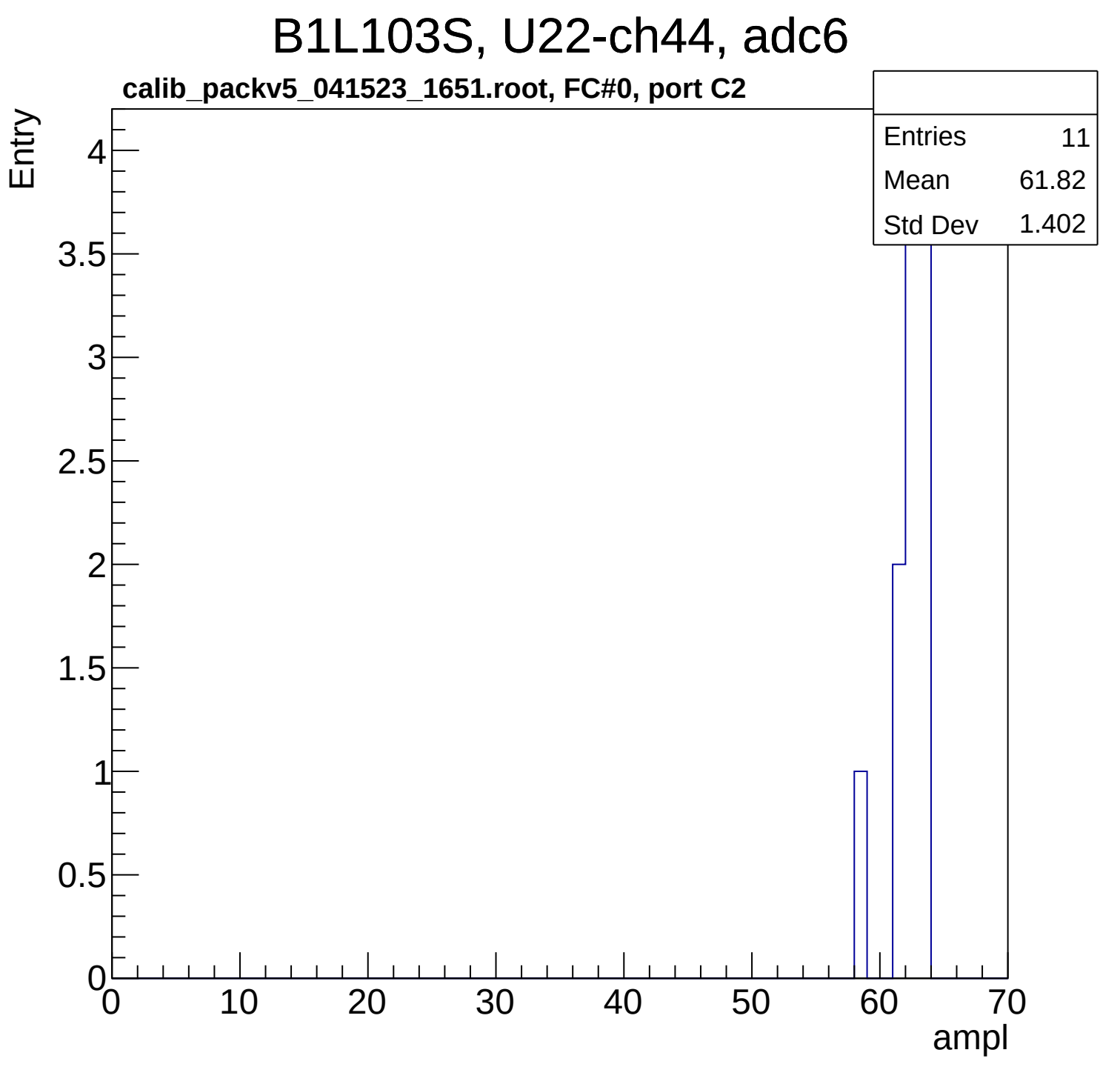
B1L103S, U22-ch44, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 61.82
Std Dev 1.402
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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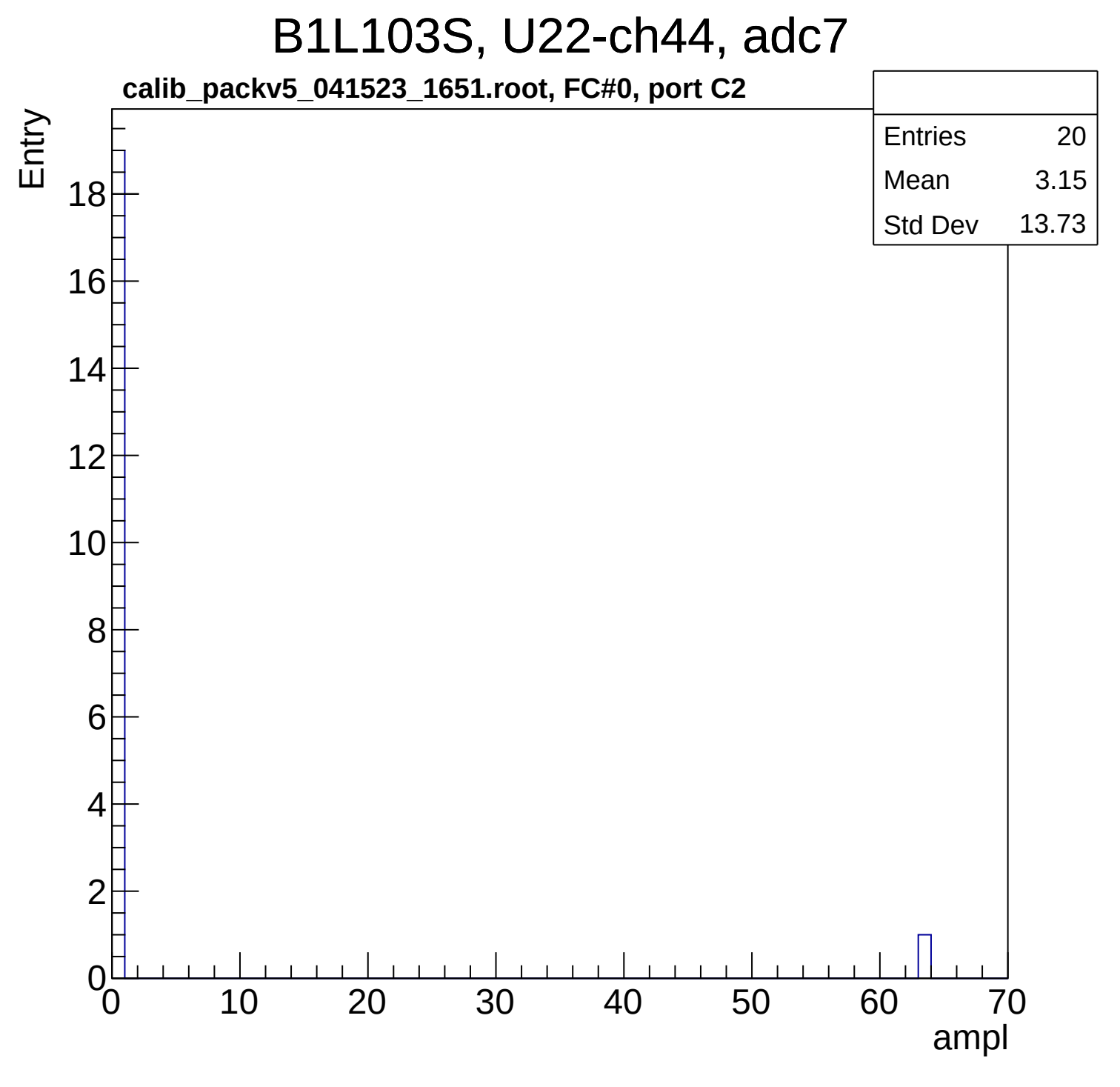
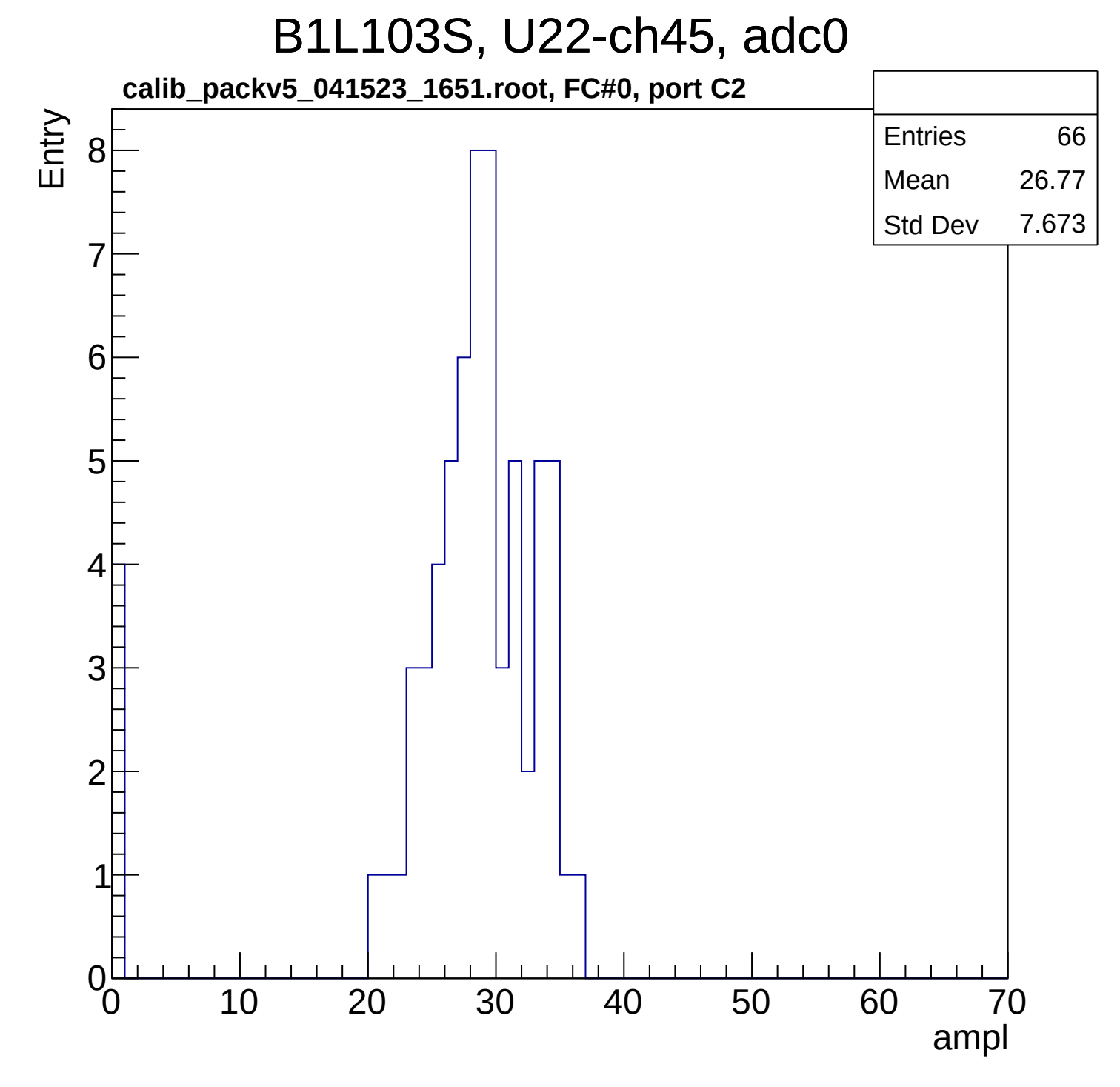
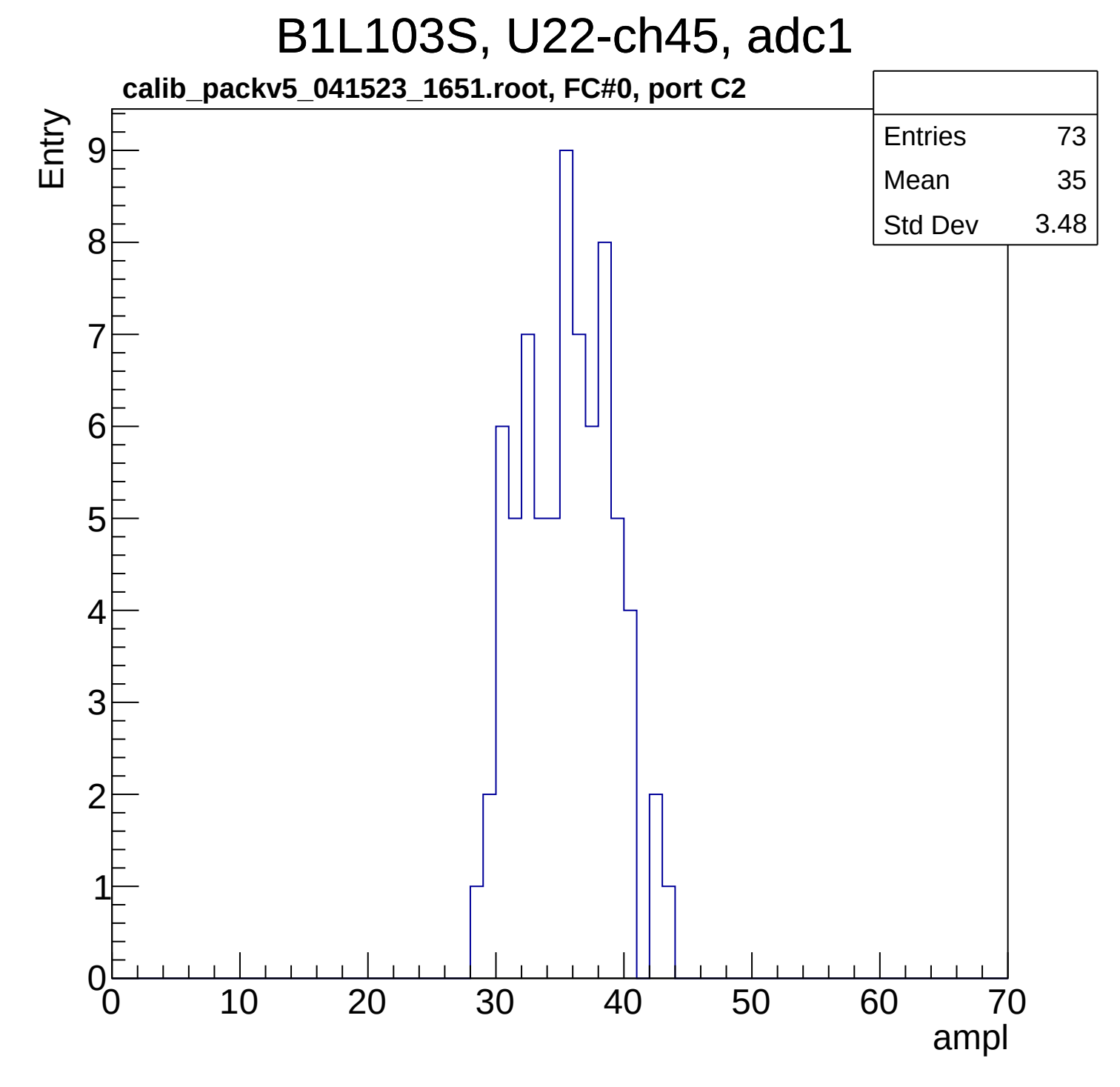

B1L103S, U22-ch44, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch45, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 26.77
Std Dev 7.673
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch45, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 35
Std Dev 3.48
Entry
ampl
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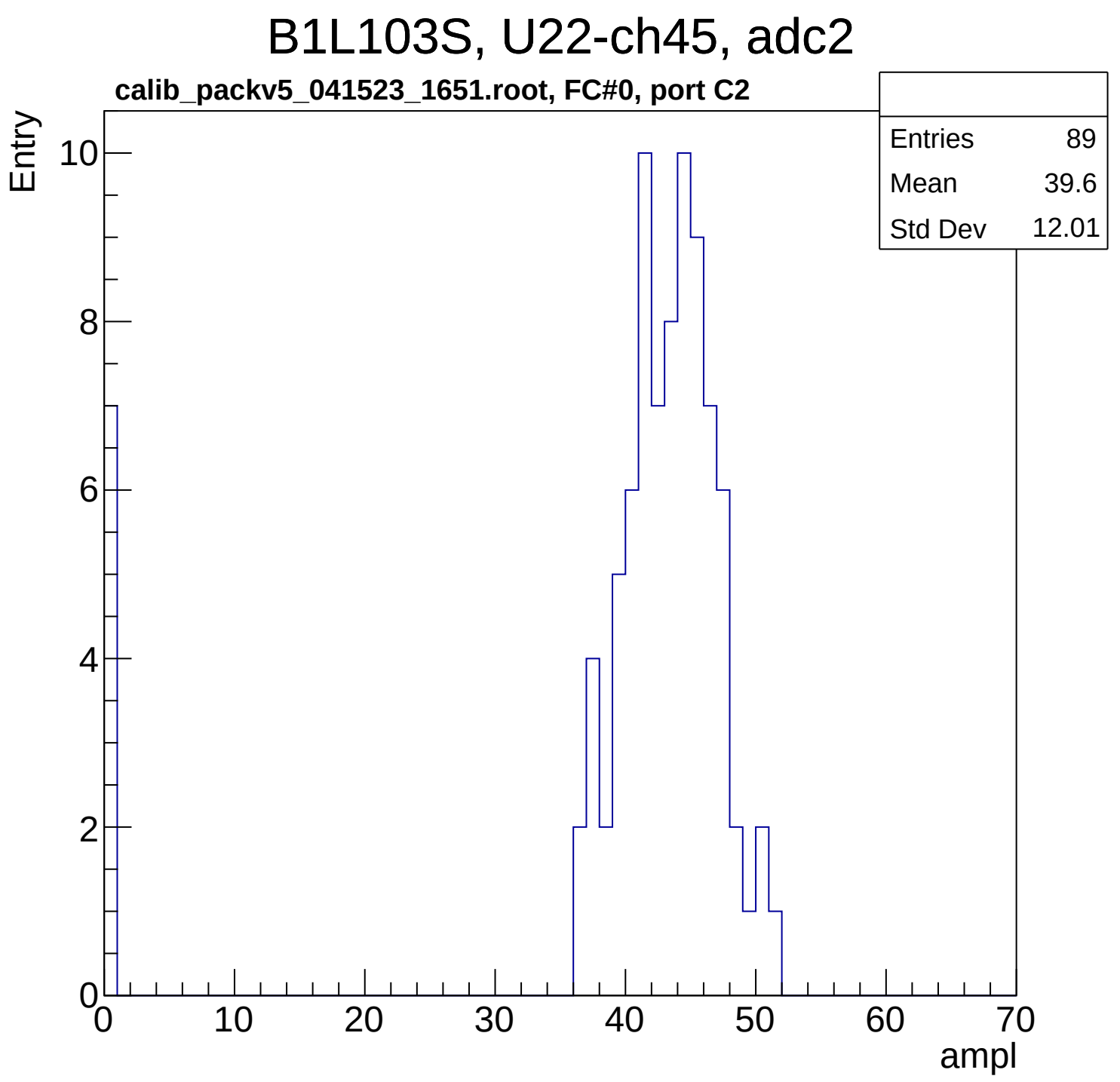
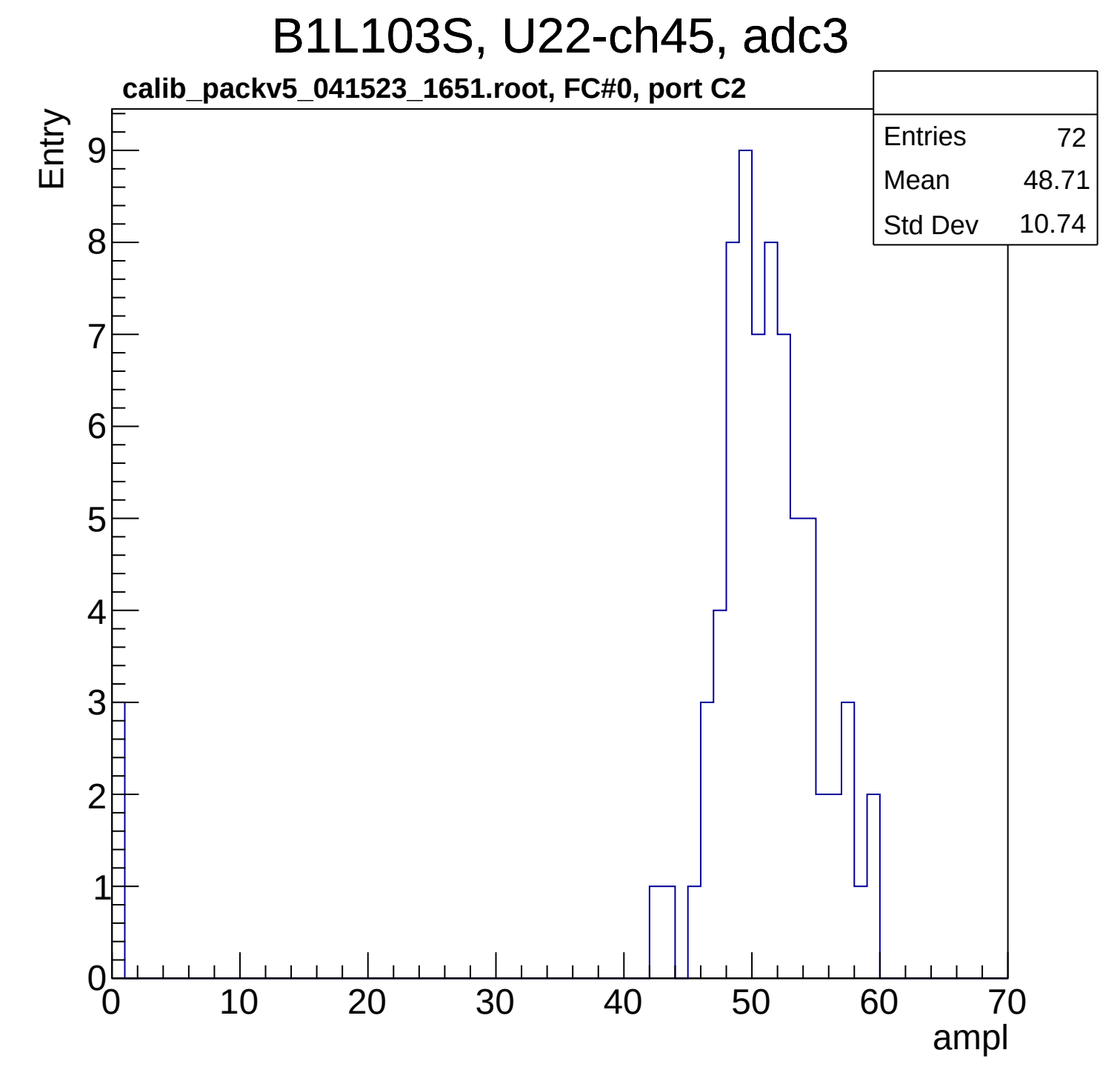
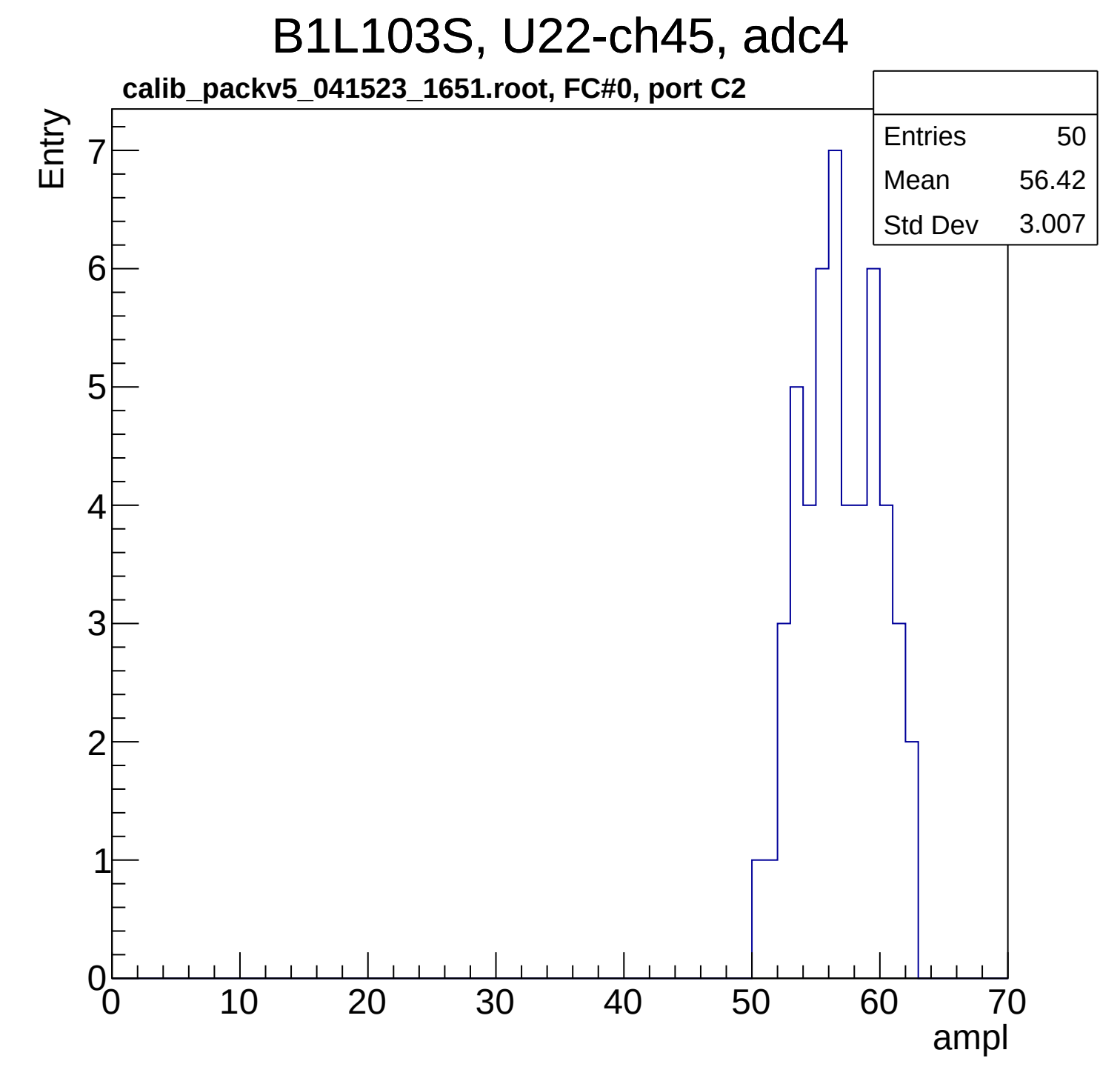
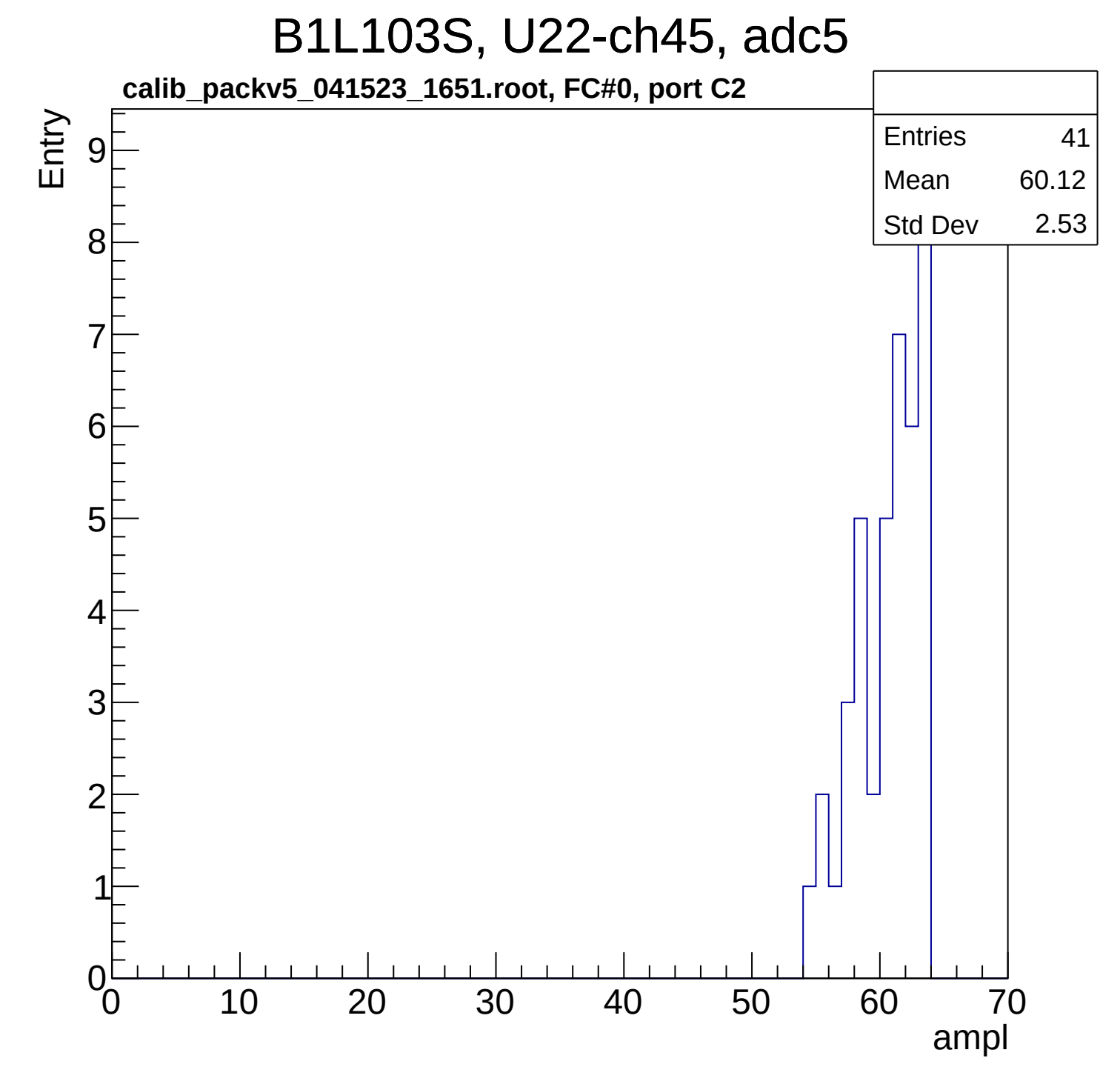
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch45, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 39.6
Std Dev 12.01
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch45, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 48.71
Std Dev 10.74
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch45, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 56.42
Std Dev 3.007
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U22-ch45, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 60.12
Std Dev 2.53
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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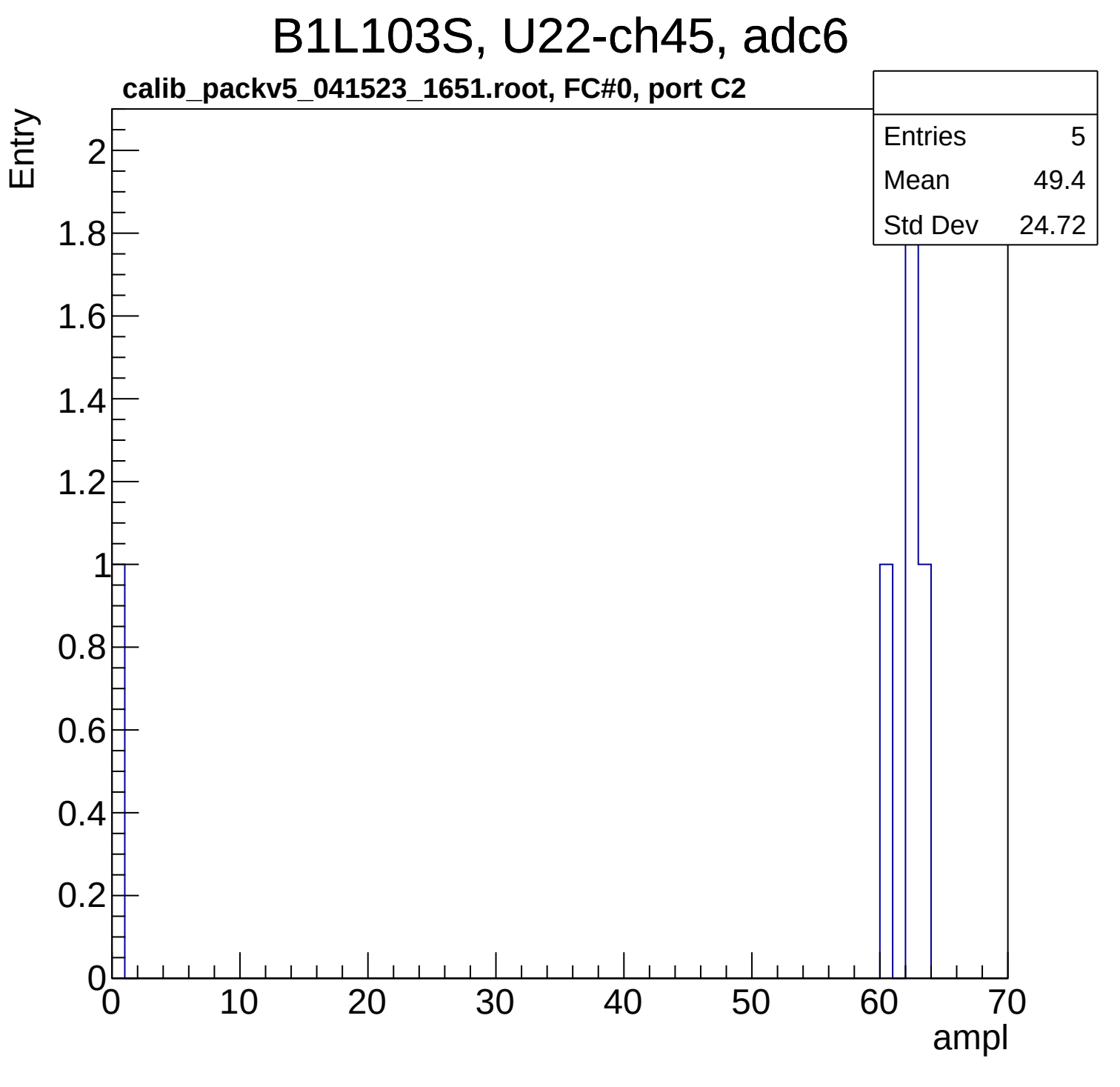
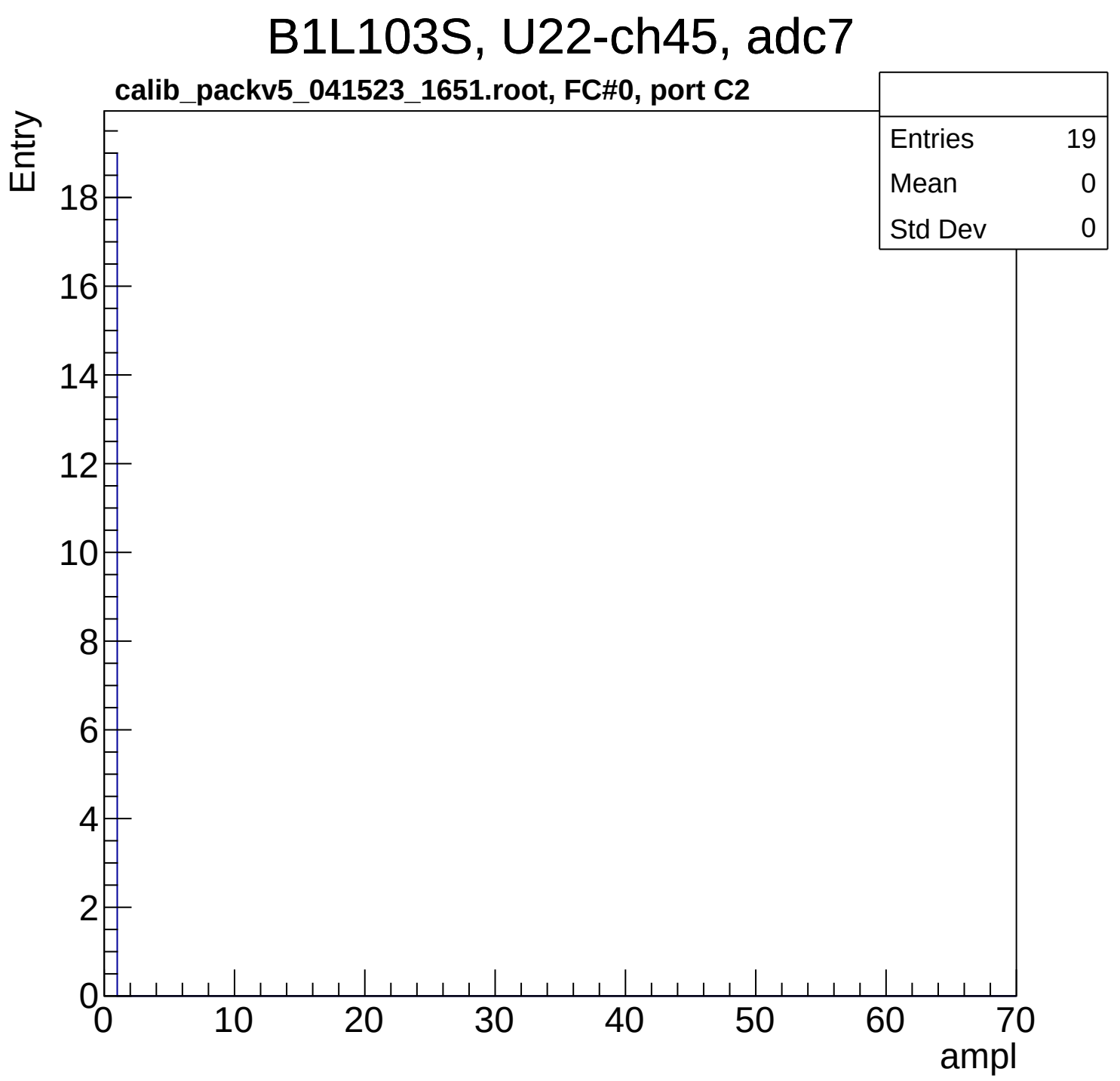
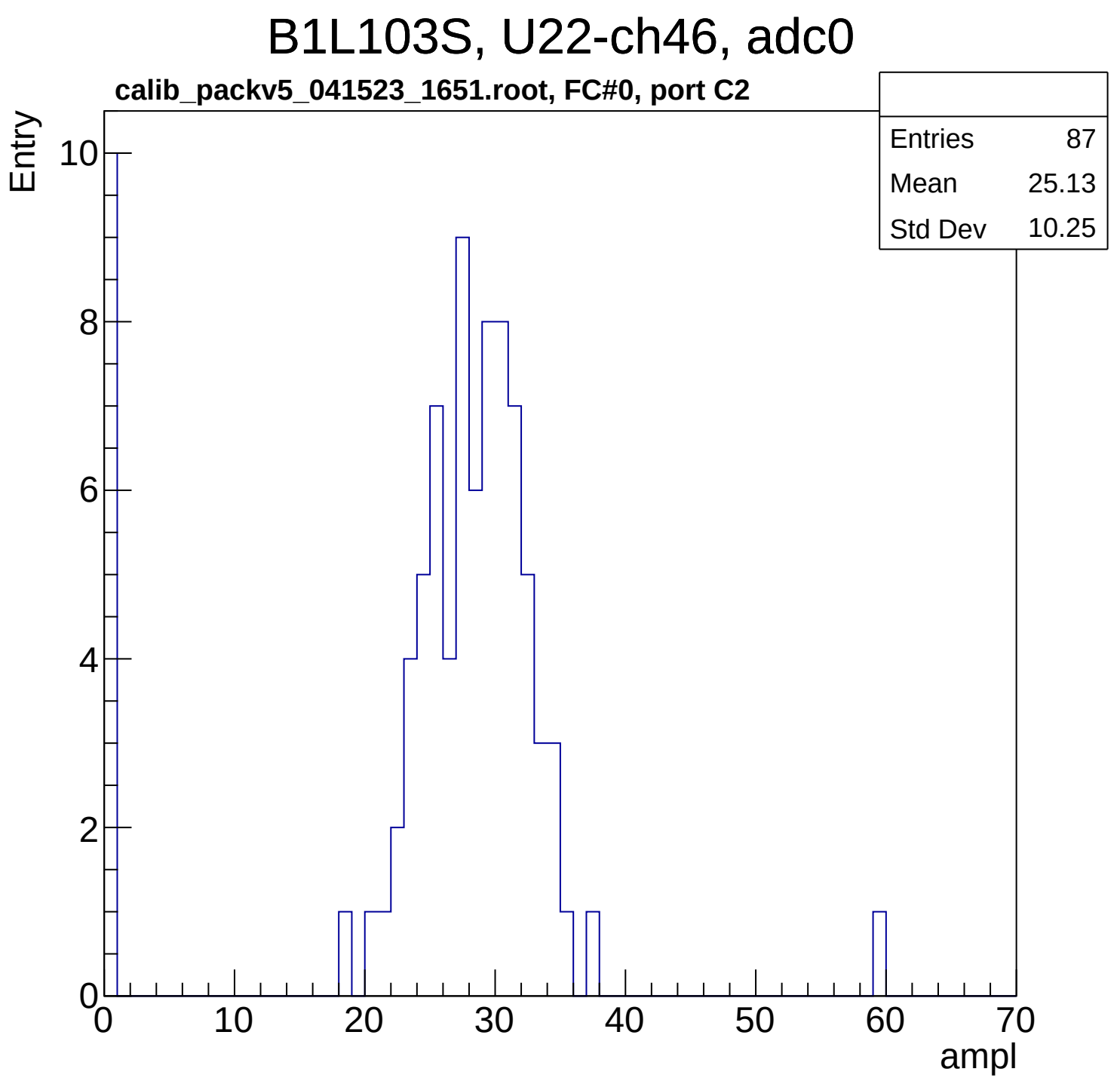

B1L103S, U22-ch45, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 49.4
Std Dev 24.72
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U22-ch45, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch46, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 25.13
Std Dev 10.25
Entry
ampl
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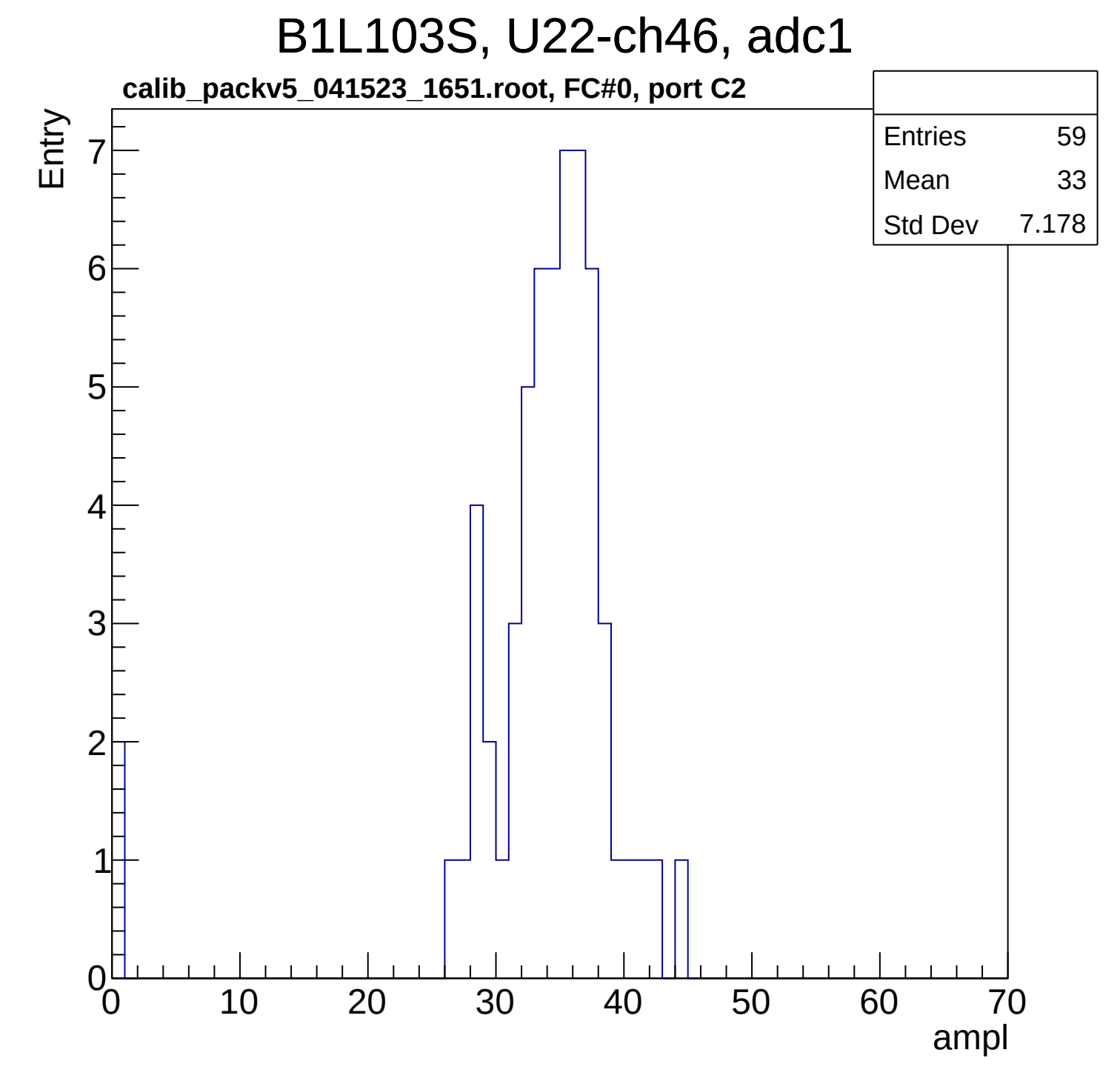
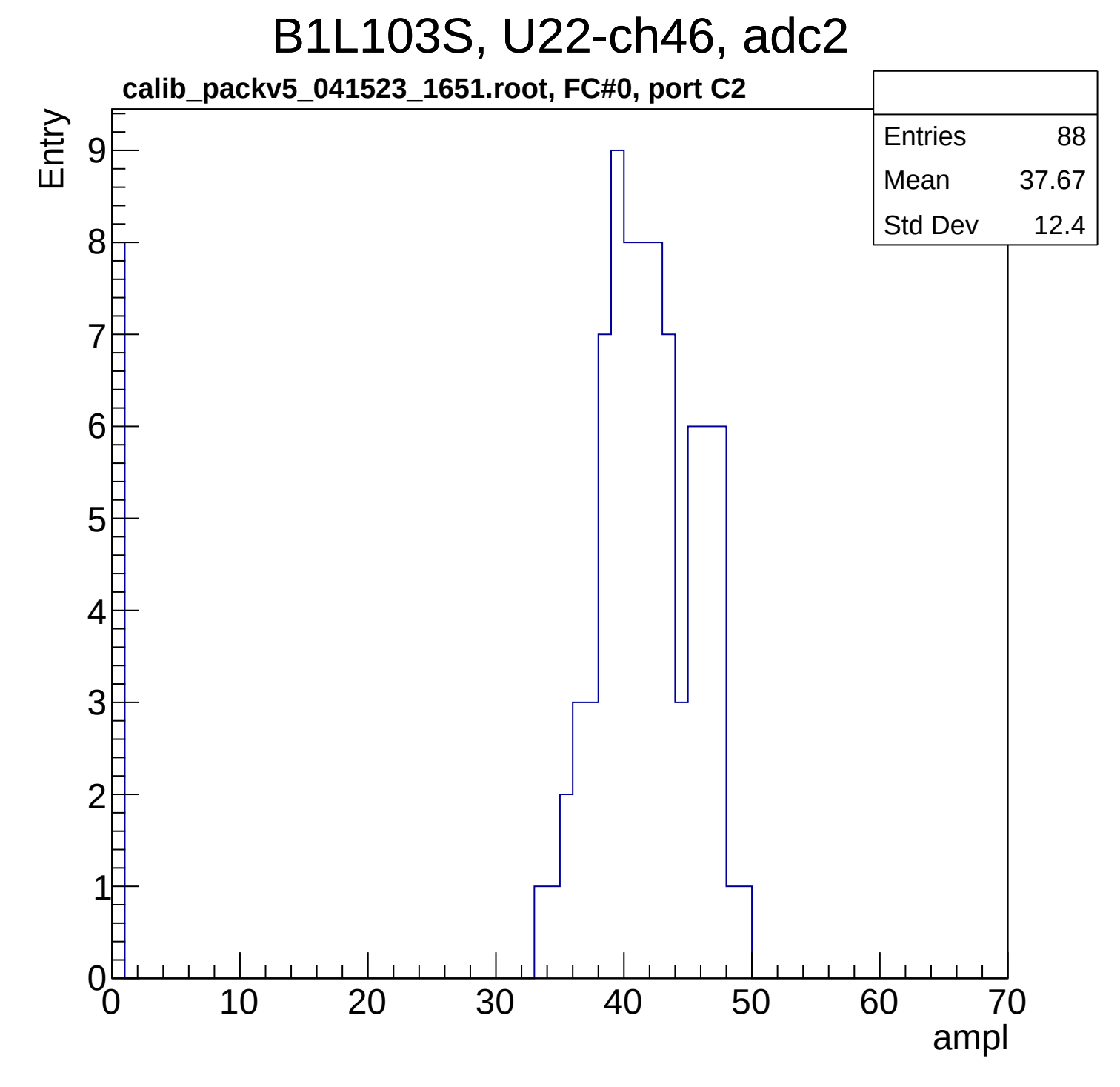
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U22-ch46, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 33
Std Dev 7.178
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U22-ch46, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 37.67
Std Dev 12.4
Entry
ampl
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2
3
4
5
6
7
8
9
0
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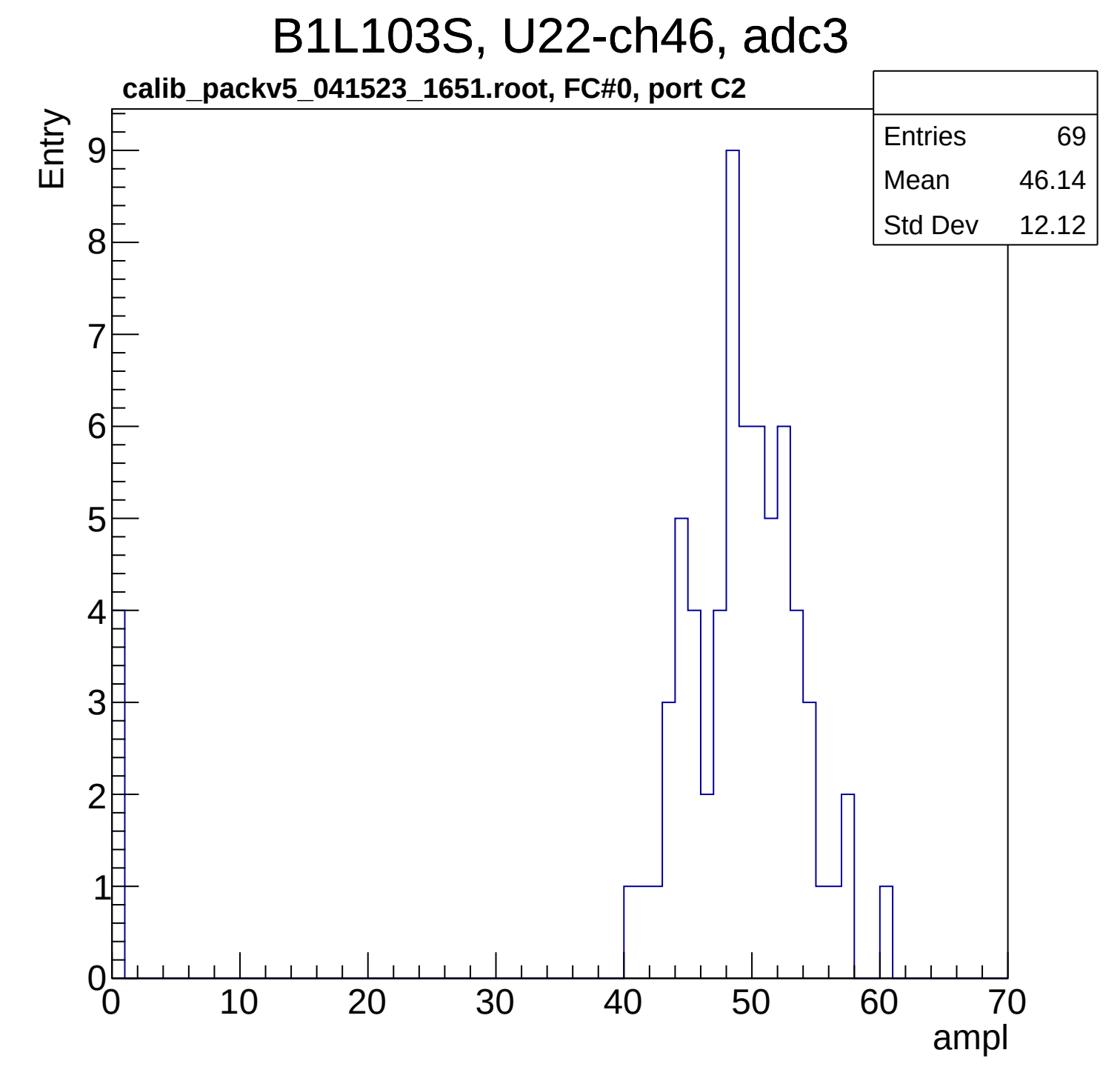
20
30
40
50
60
70


B1L103S, U22-ch46, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 46.14
Std Dev 12.12
Entry
ampl
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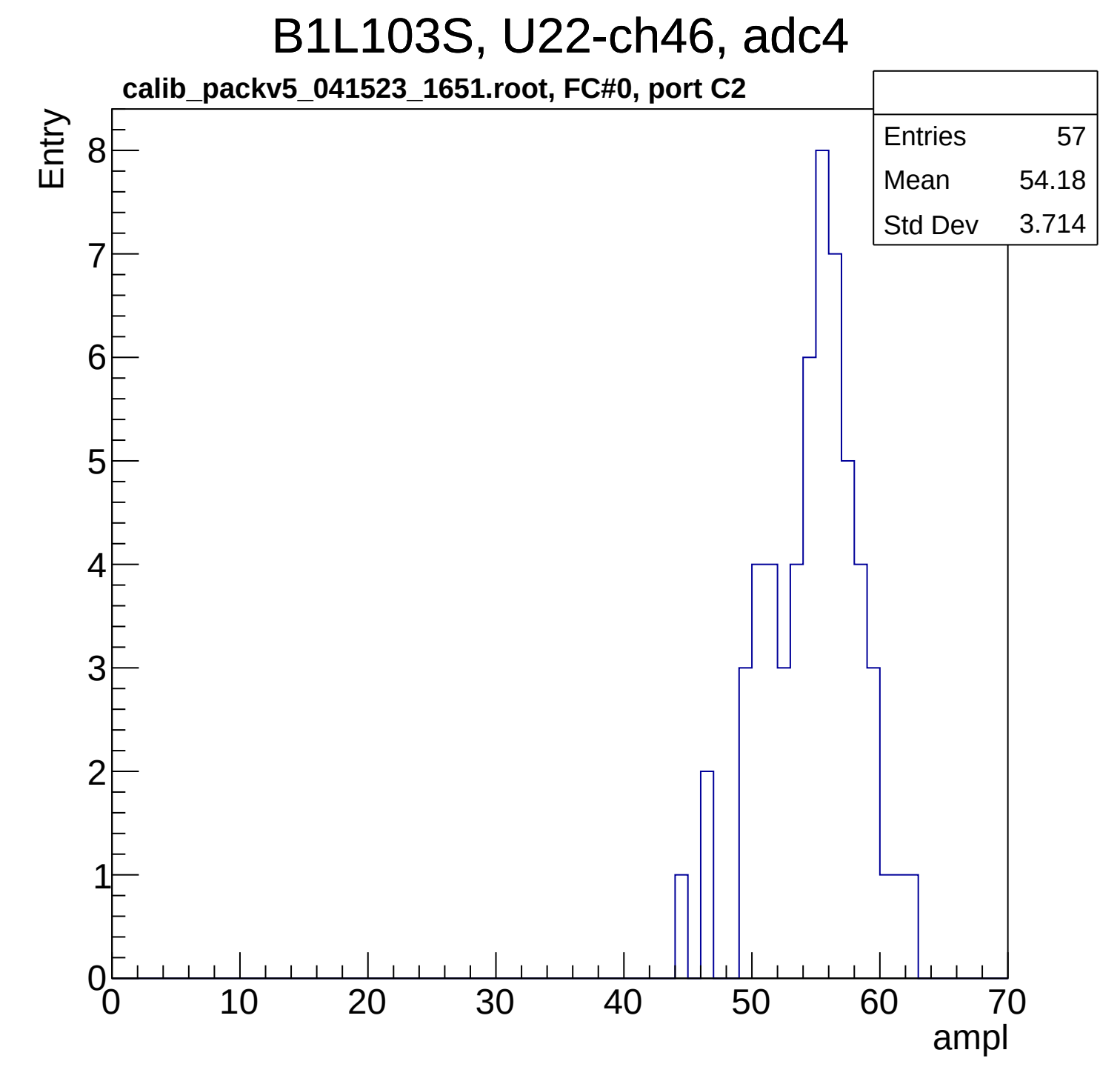
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch46, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 54.18
Std Dev 3.714
Entry
ampl
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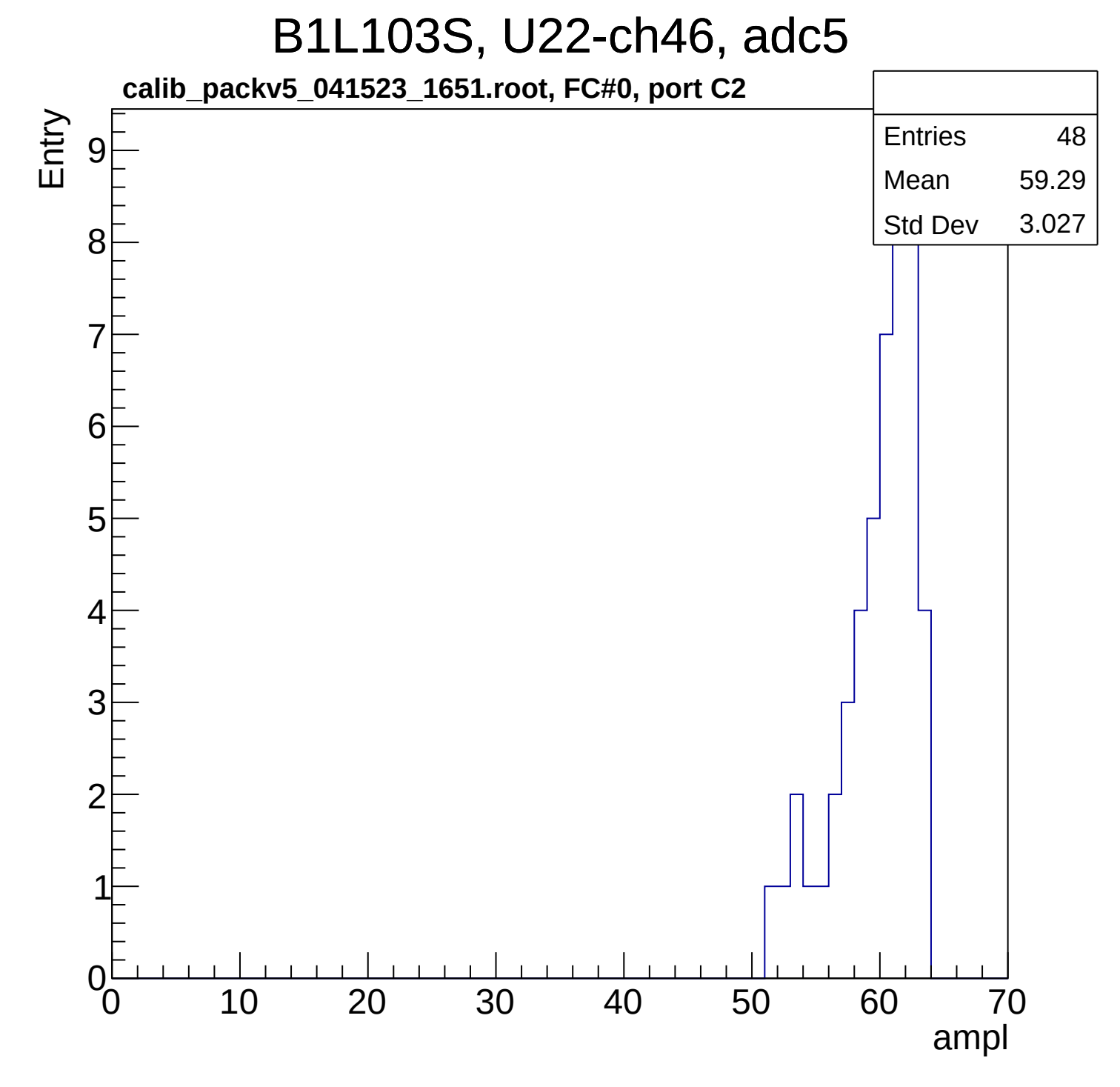
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch46, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 59.29
Std Dev 3.027
Entry
ampl
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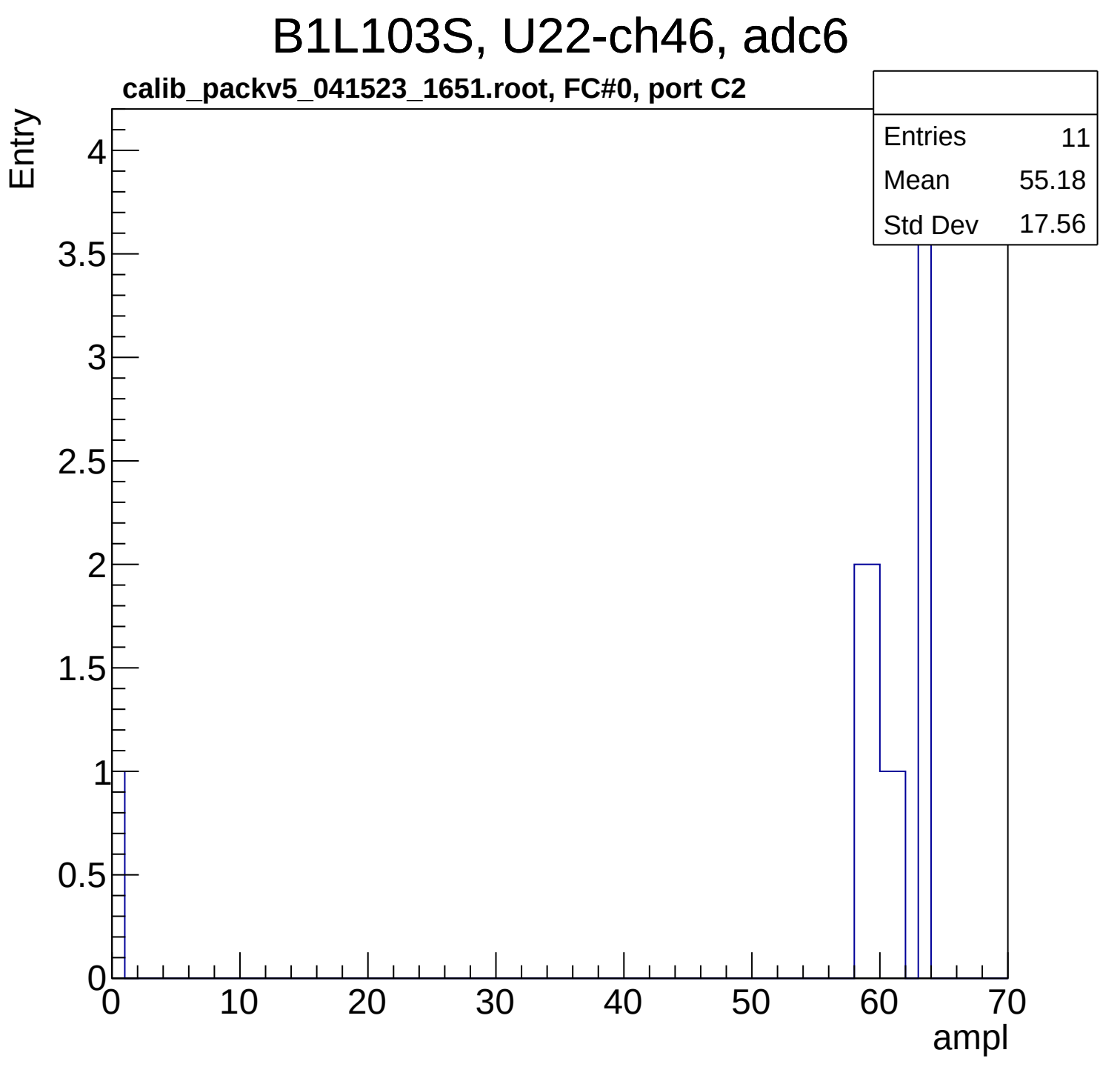
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch46, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 55.18
Std Dev 17.56
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
10
20
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60
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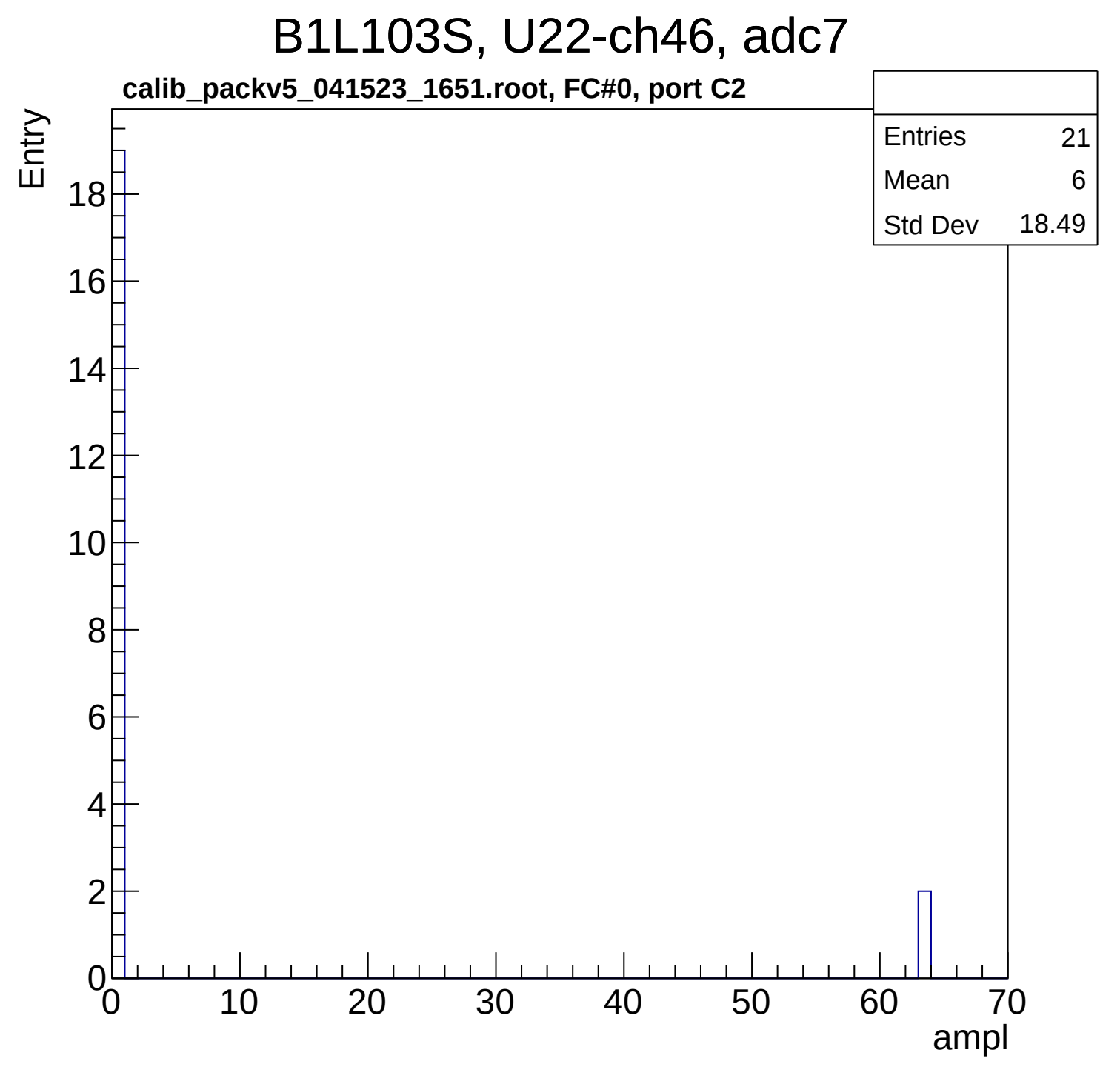
B1L103S, U22-ch46, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 6
Std Dev 18.49
Entry
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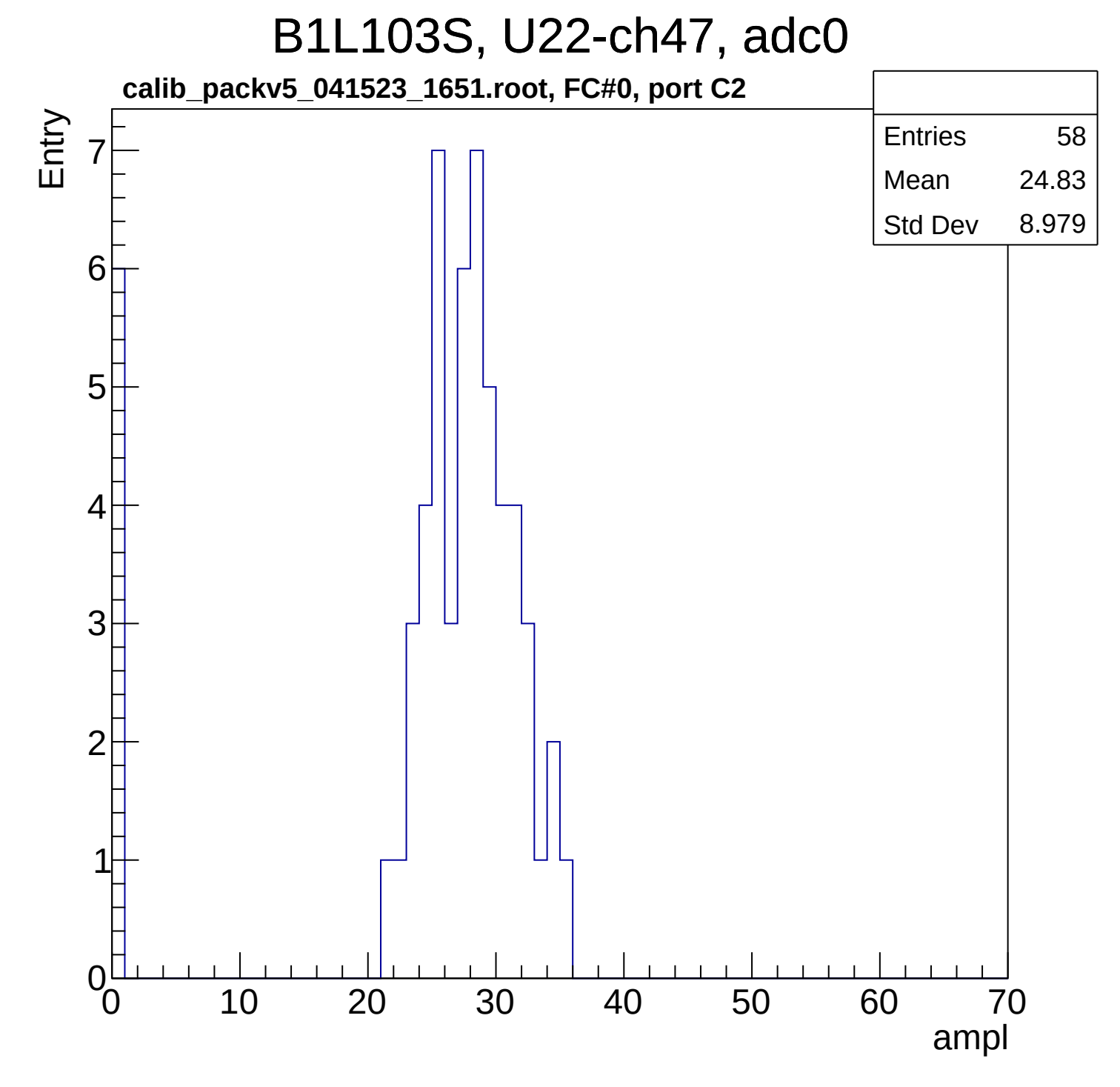
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch47, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 24.83
Std Dev 8.979
Entry
ampl
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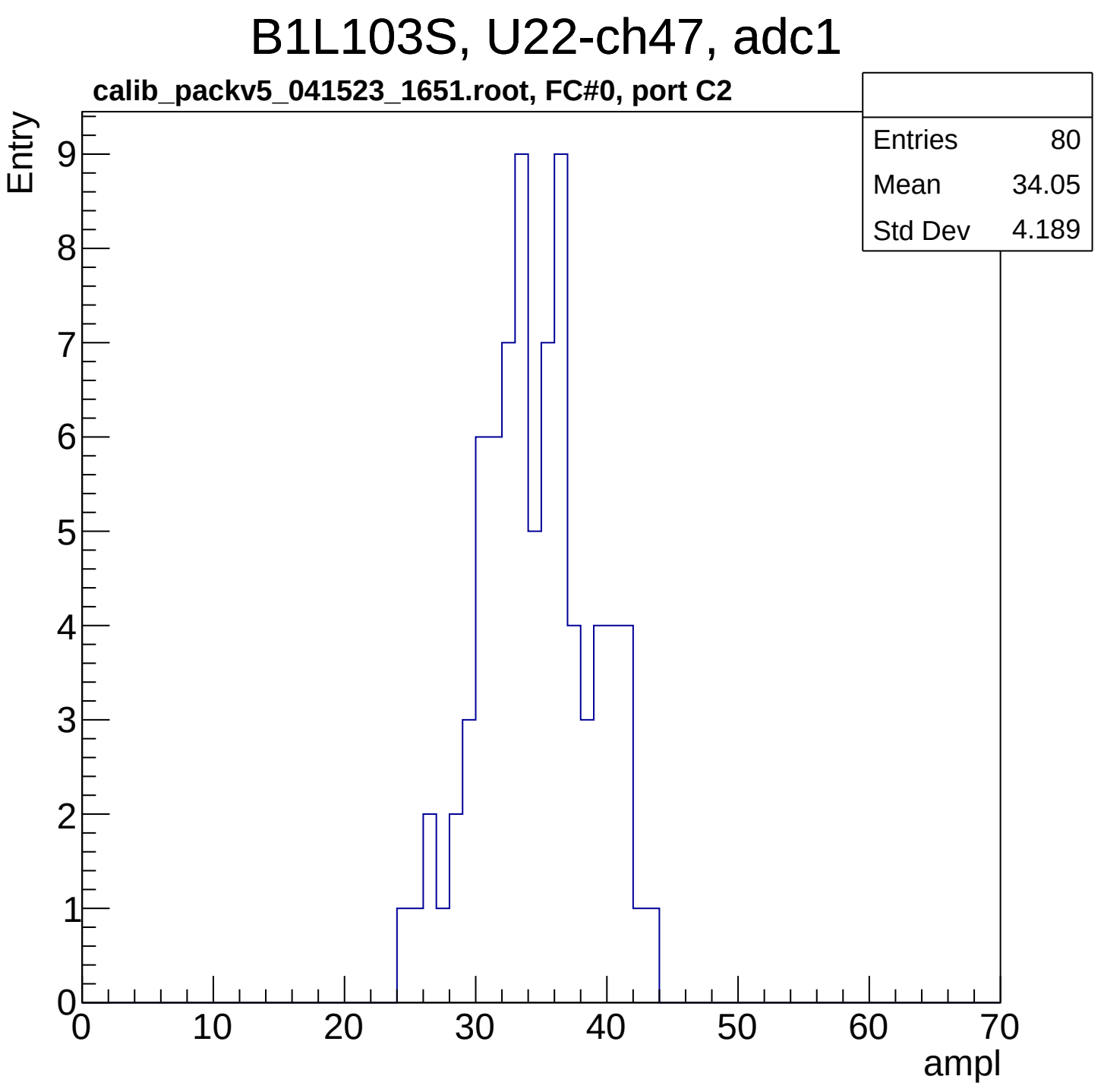
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U22-ch47, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 34.05
Std Dev 4.189
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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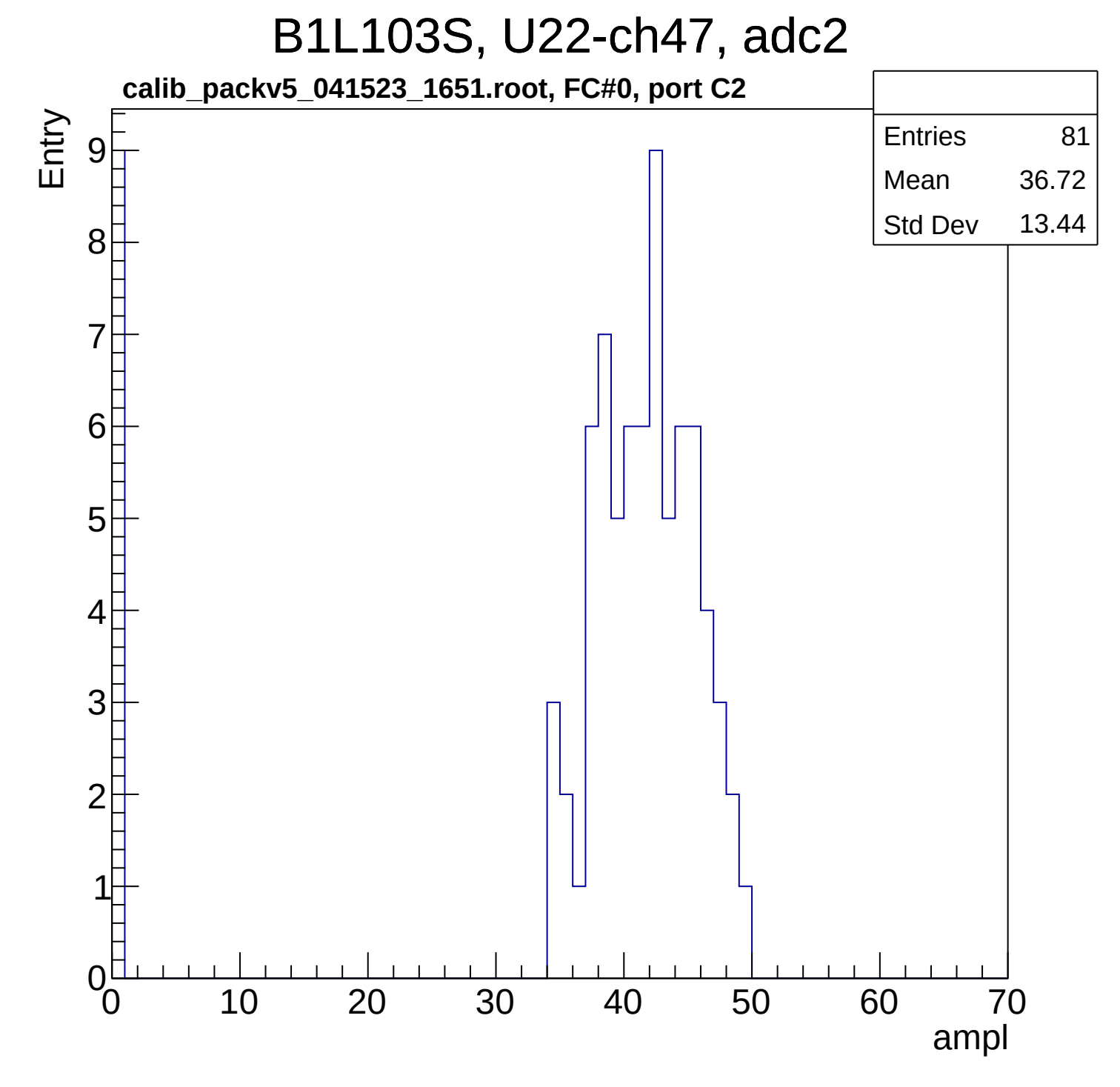
B1L103S, U22-ch47, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 36.72
Std Dev 13.44
Entry
ampl
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3
4
5
6
7
8
9
0
10
20
30
40
50
60
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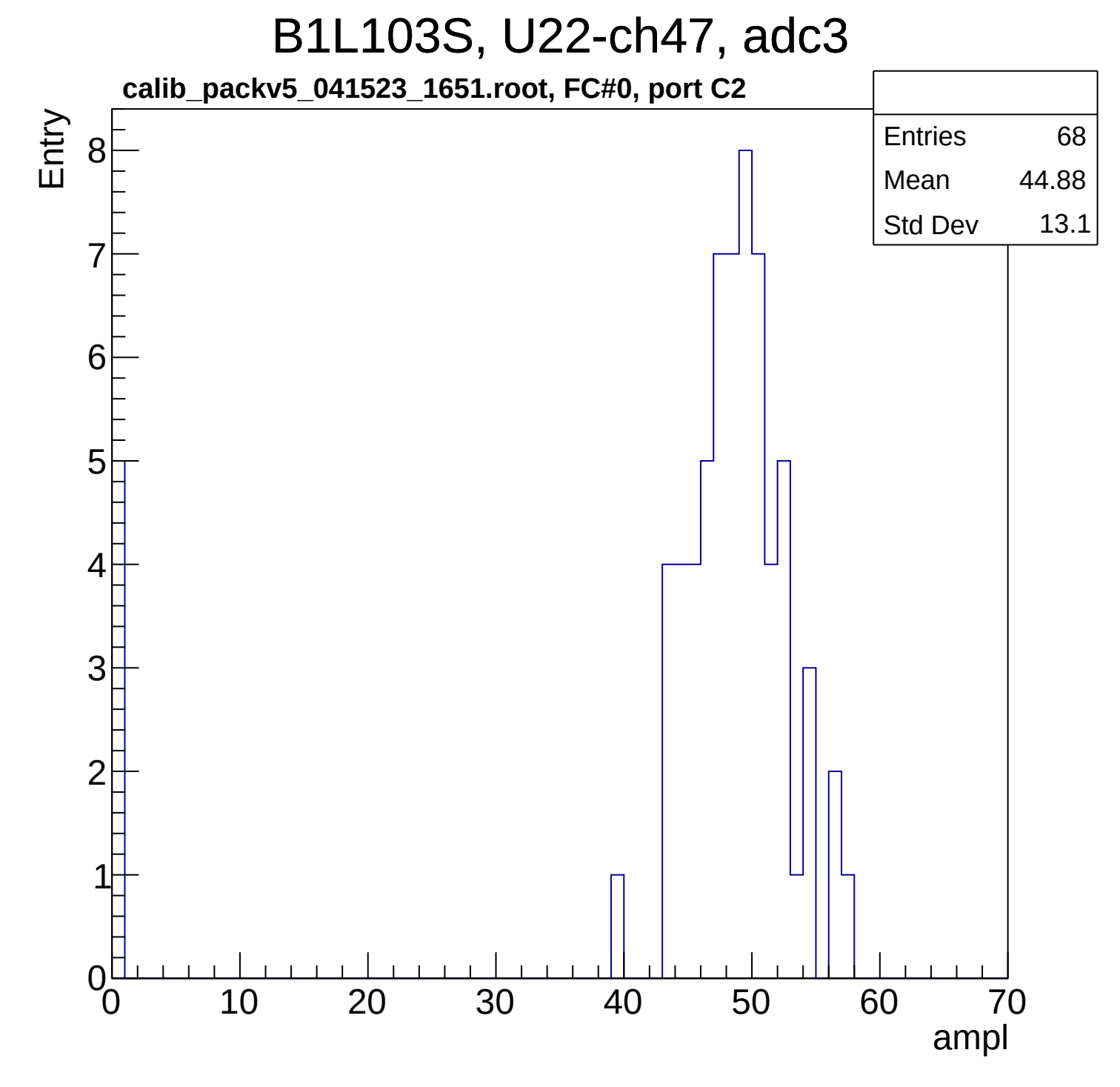
B1L103S, U22-ch47, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 44.88
Std Dev 13.1
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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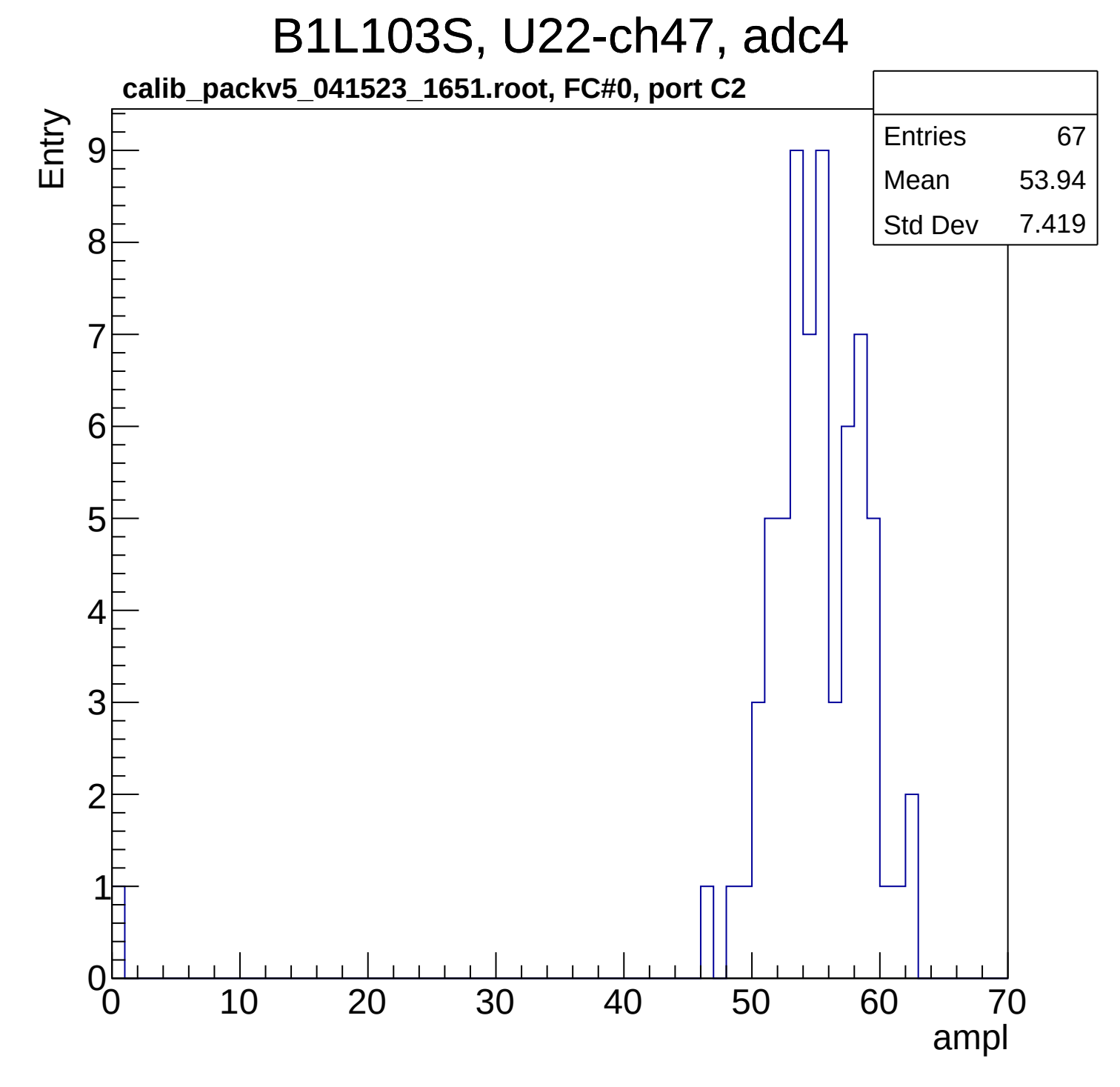
B1L103S, U22-ch47, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 53.94
Std Dev 7.419
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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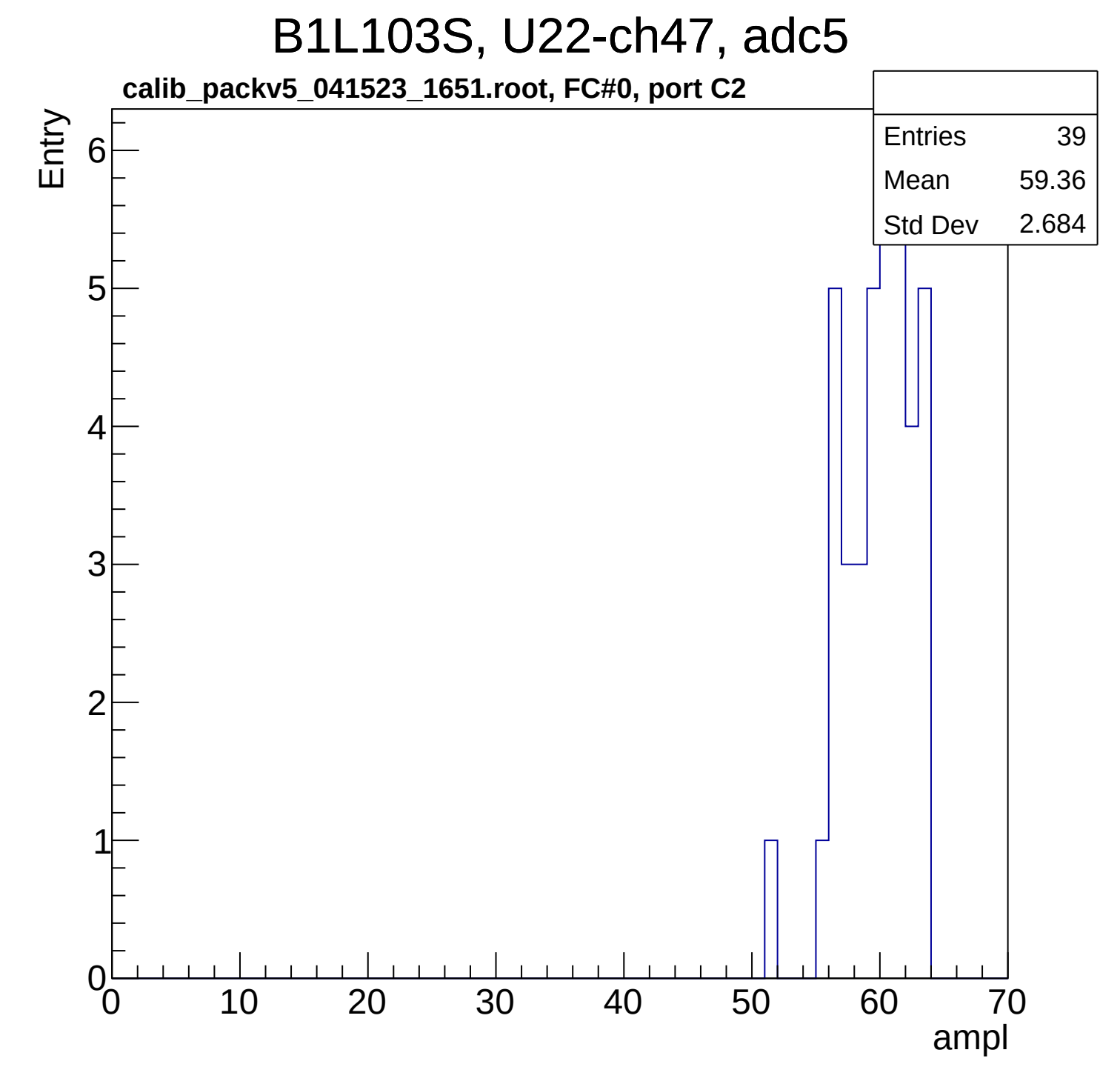
B1L103S, U22-ch47, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 59.36
Std Dev 2.684
Entry
ampl
0
1
2
3
4
5
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60
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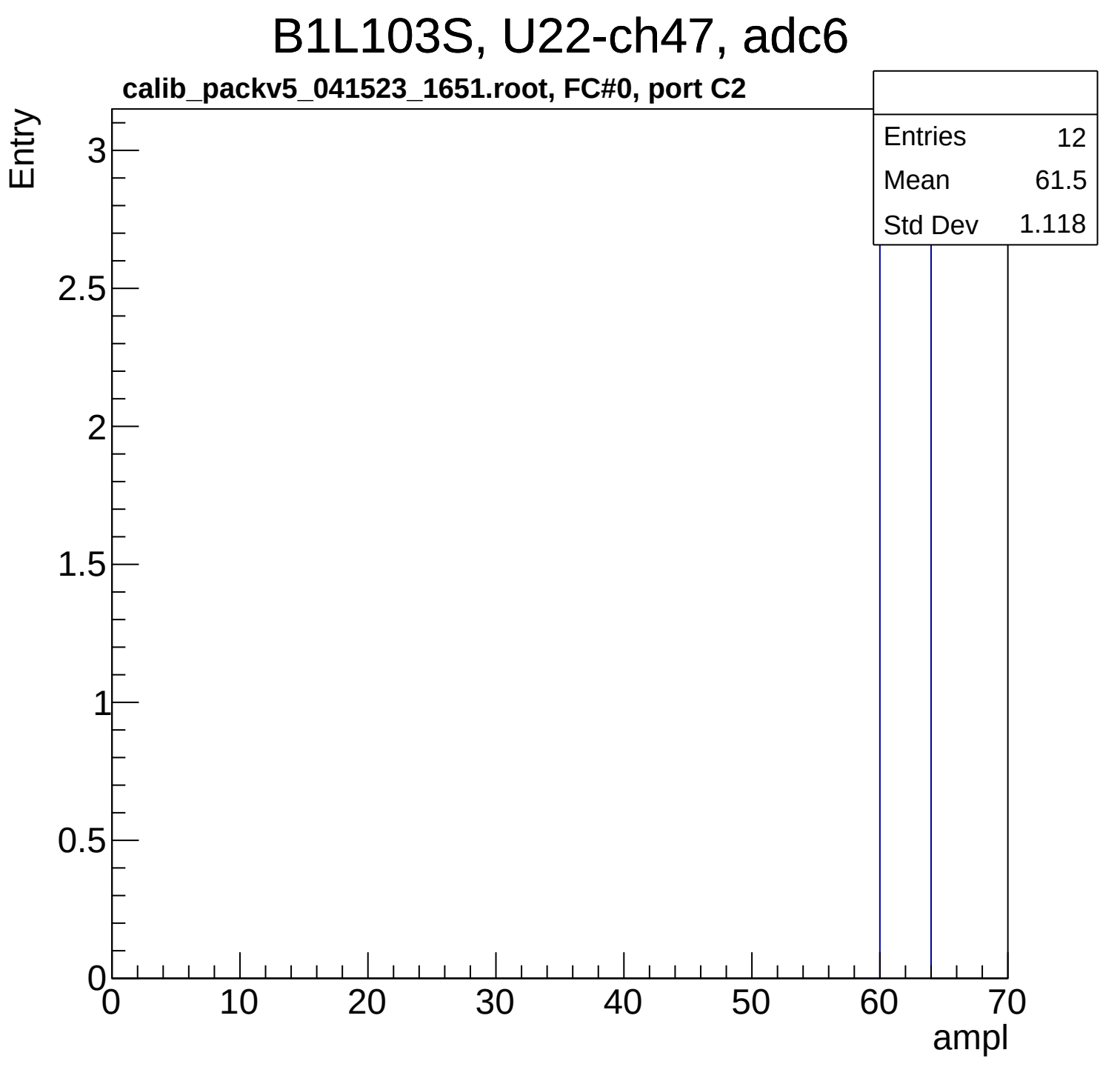
B1L103S, U22-ch47, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.5
Std Dev 1.118
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
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40
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60
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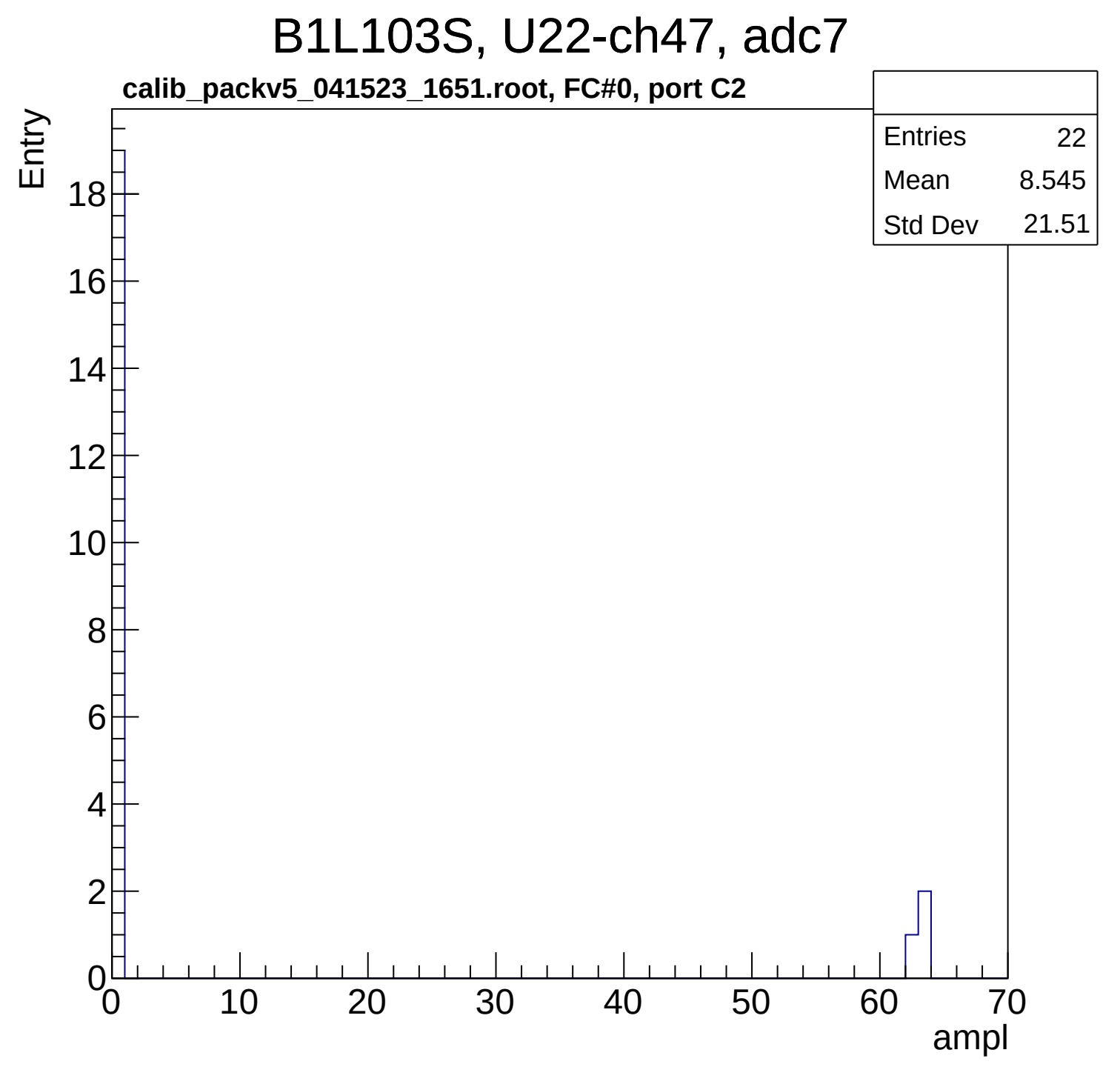
B1L103S, U22-ch47, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.545
Std Dev 21.51
Entry
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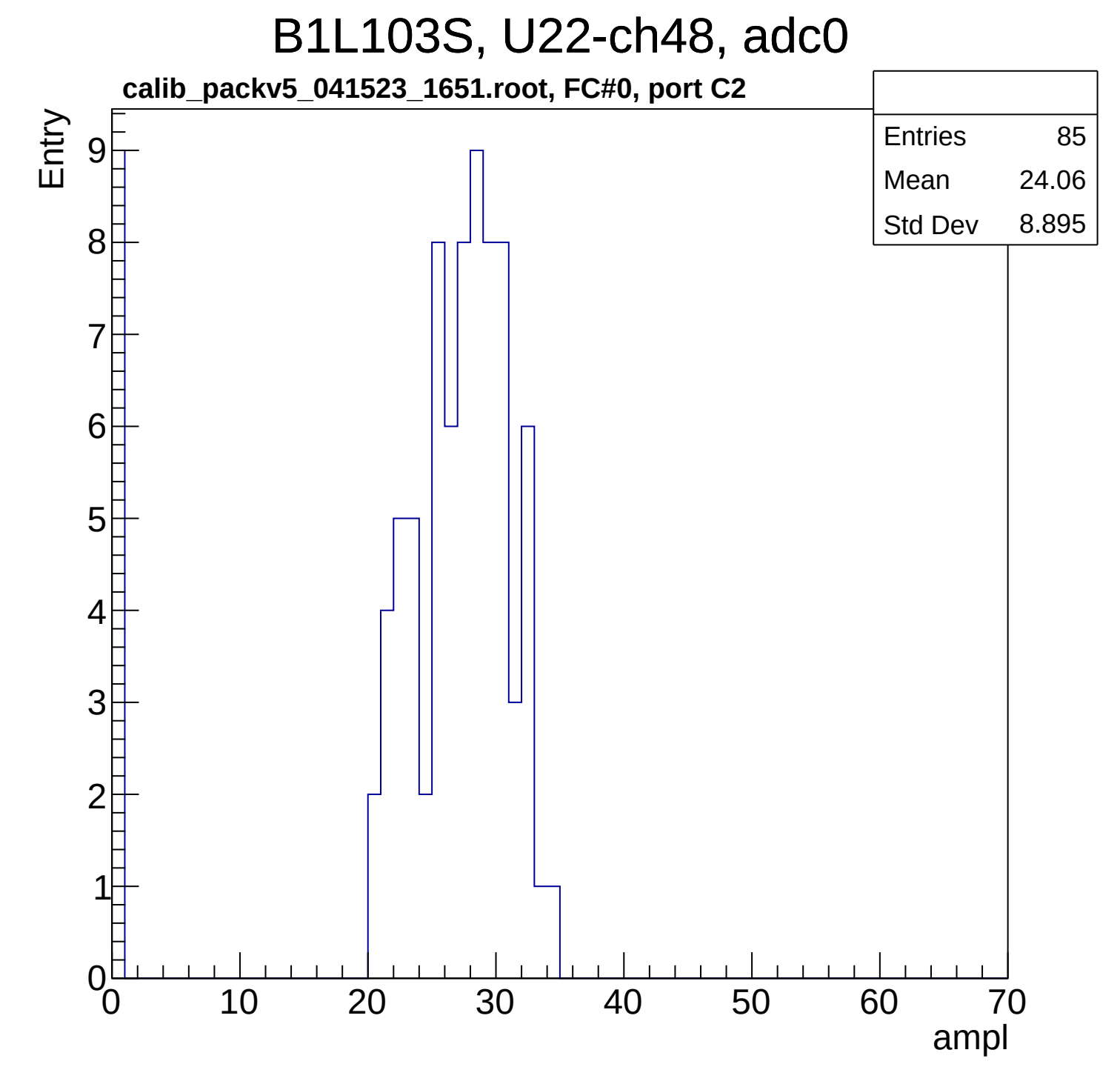
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch48, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 24.06
Std Dev 8.895
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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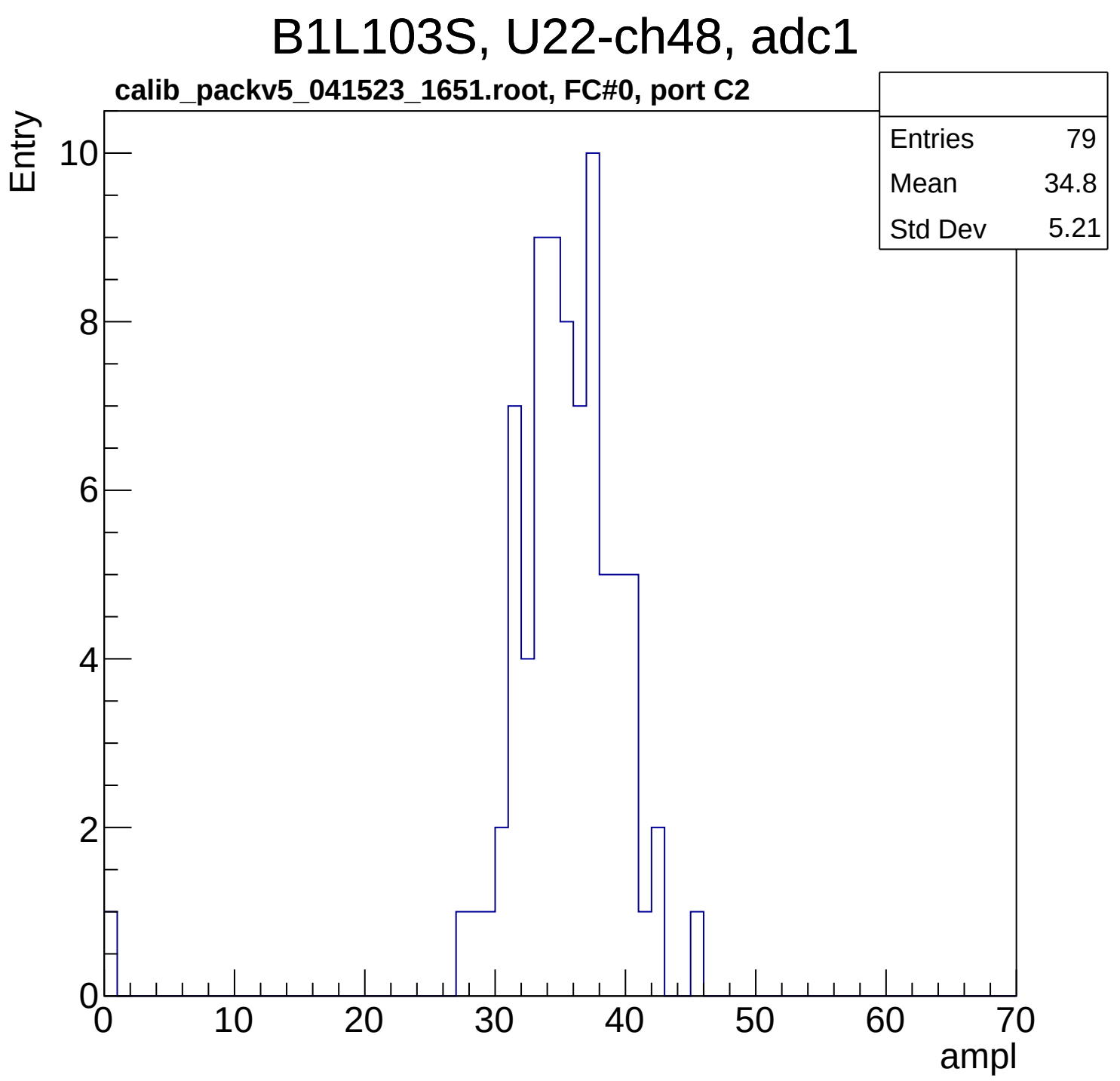
B1L103S, U22-ch48, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 34.8
Std Dev 5.21
Entry
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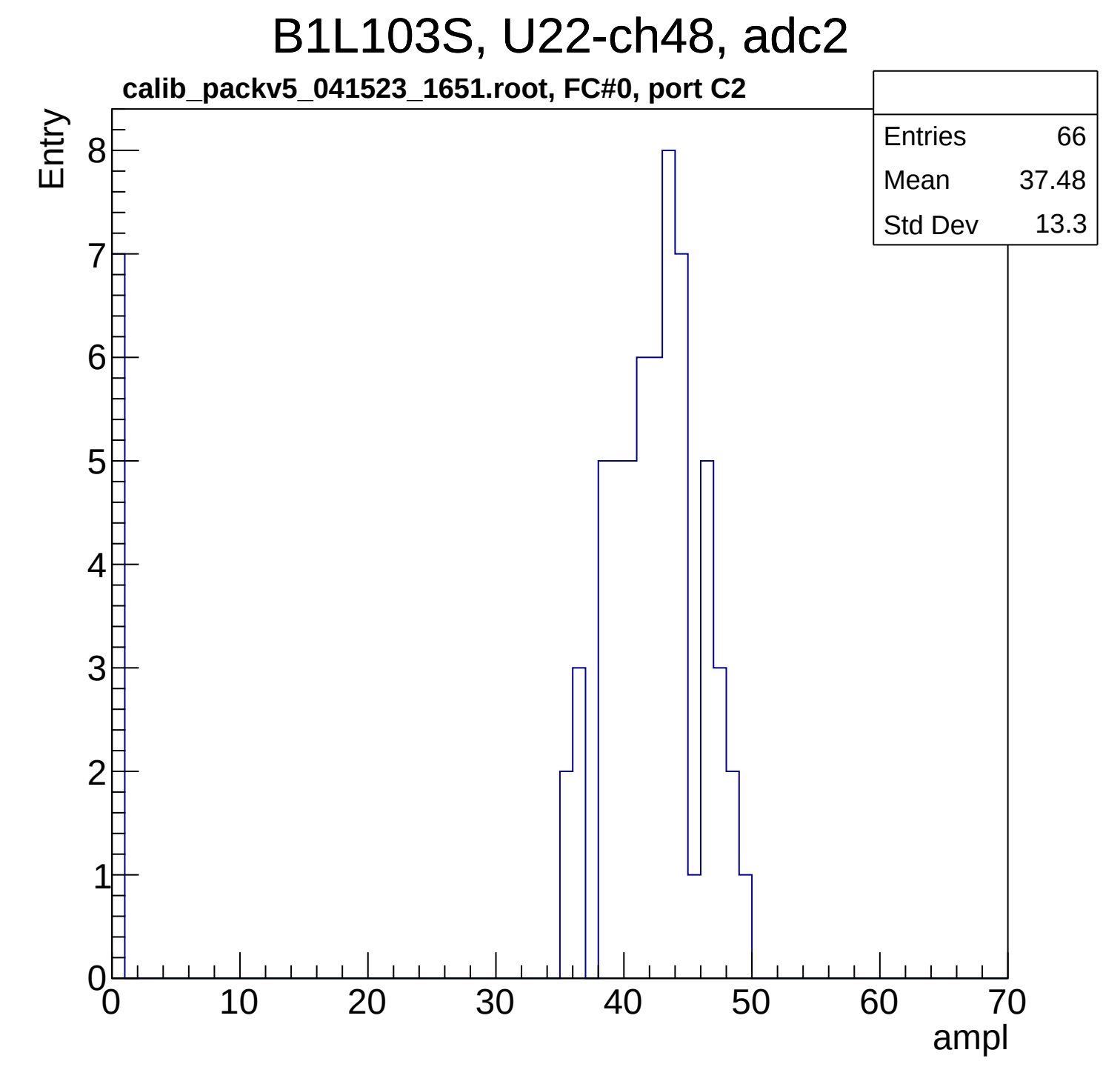
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch48, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 37.48
Std Dev 13.3
Entry
ampl
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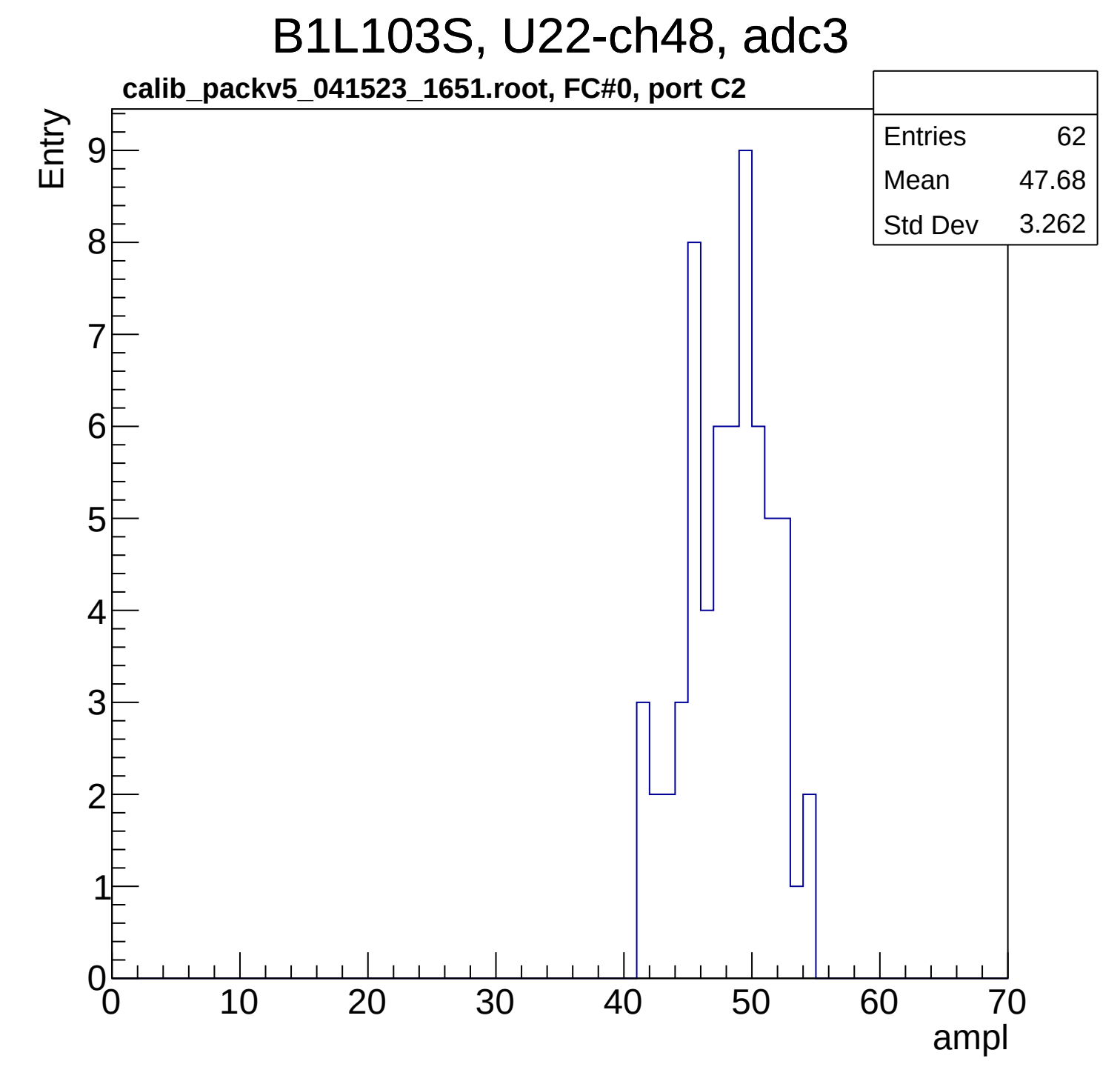
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch48, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 47.68
Std Dev 3.262
Entry
ampl
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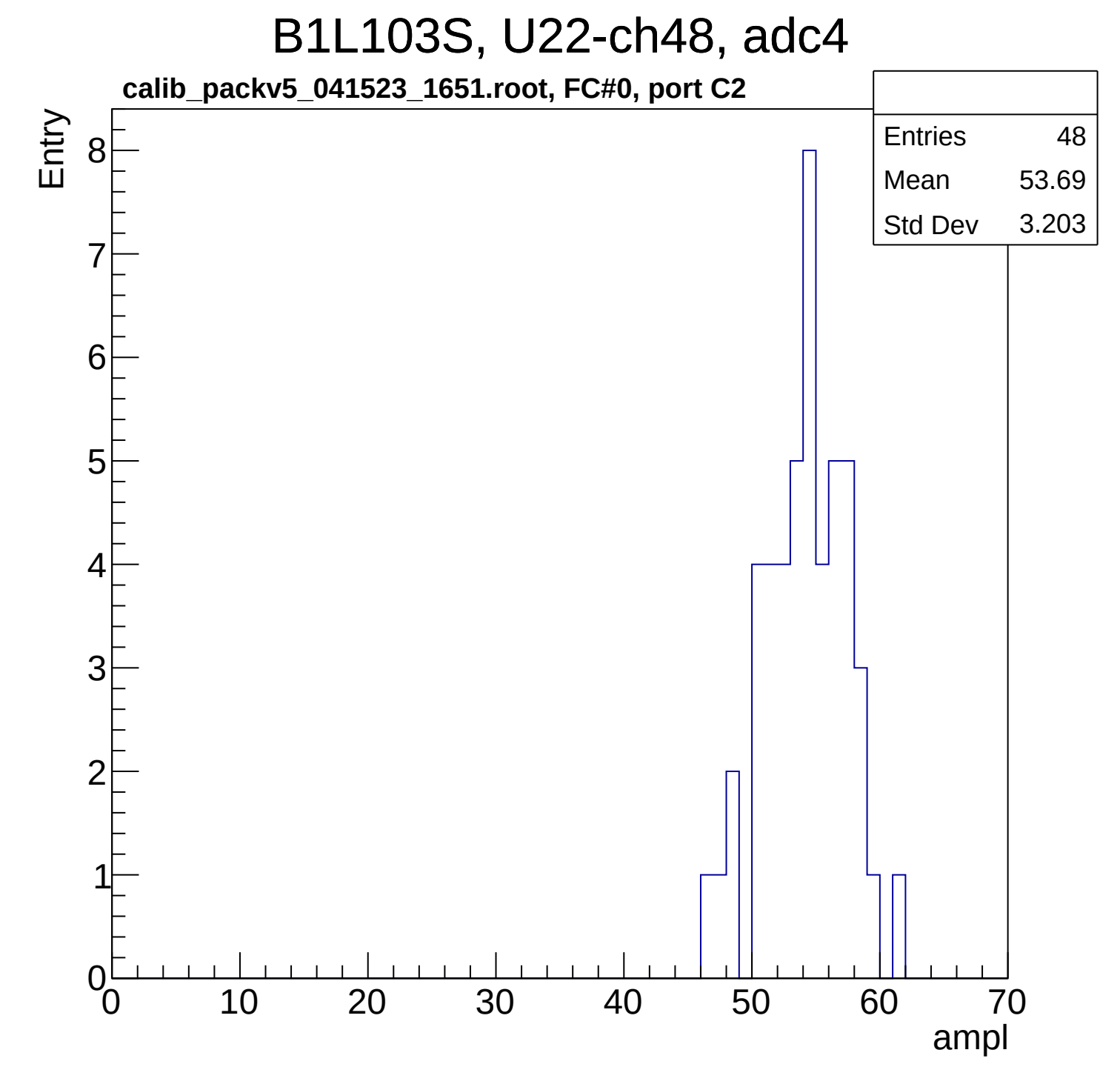
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch48, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 53.69
Std Dev 3.203
Entry
ampl
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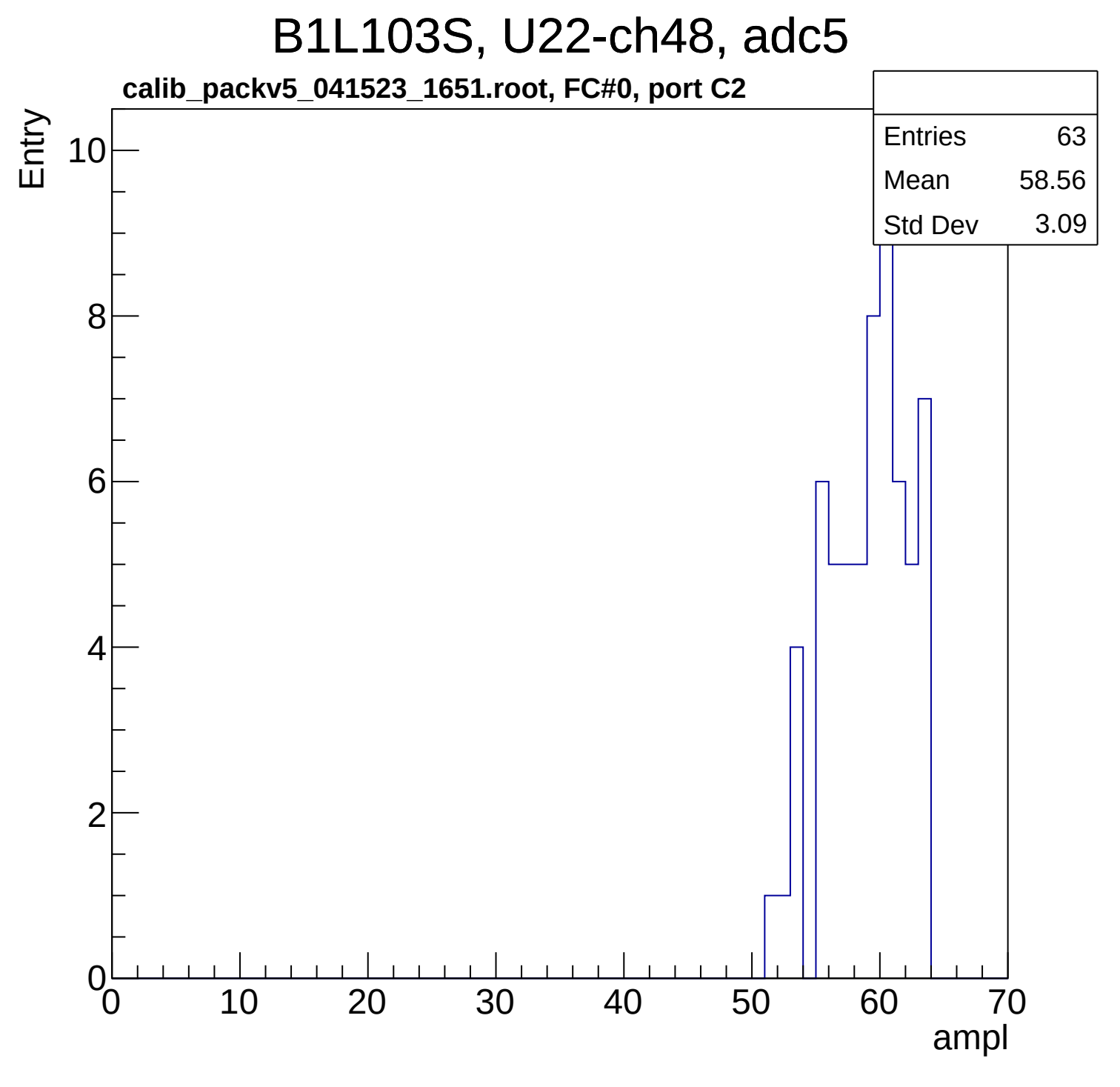
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch48, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 58.56
Std Dev 3.09
Entry
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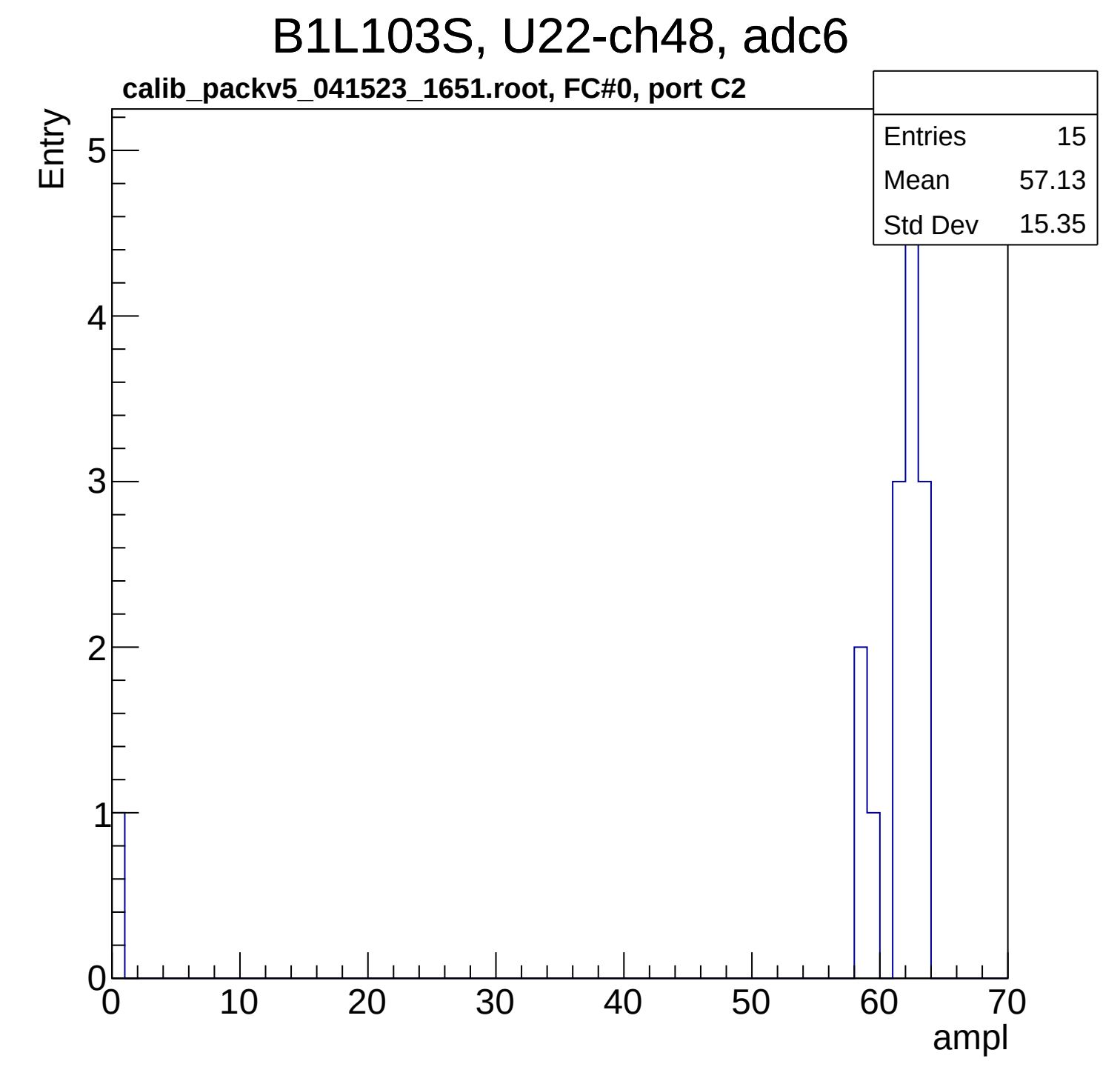
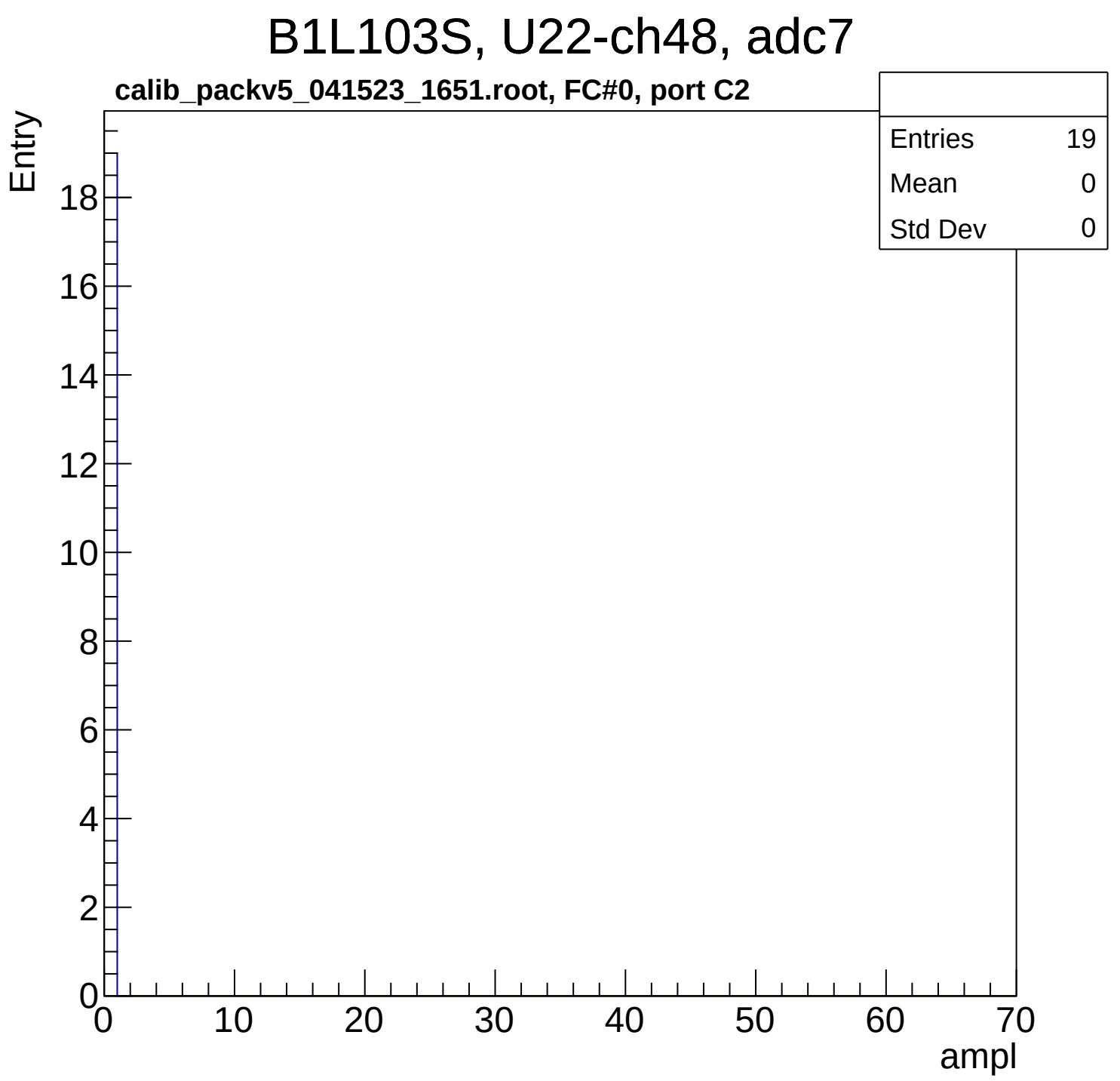
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch48, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 57.13
Std Dev 15.35
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch48, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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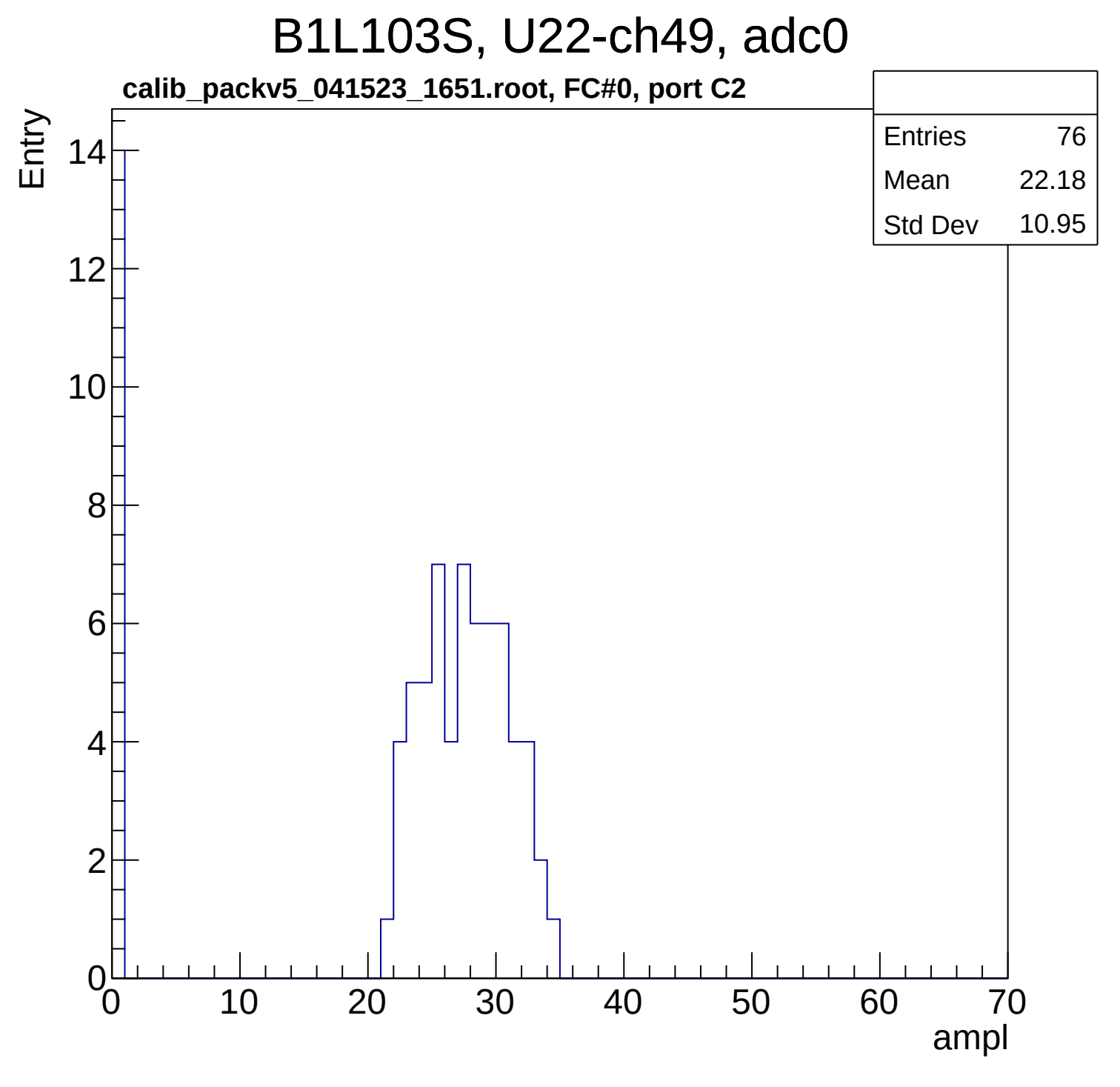
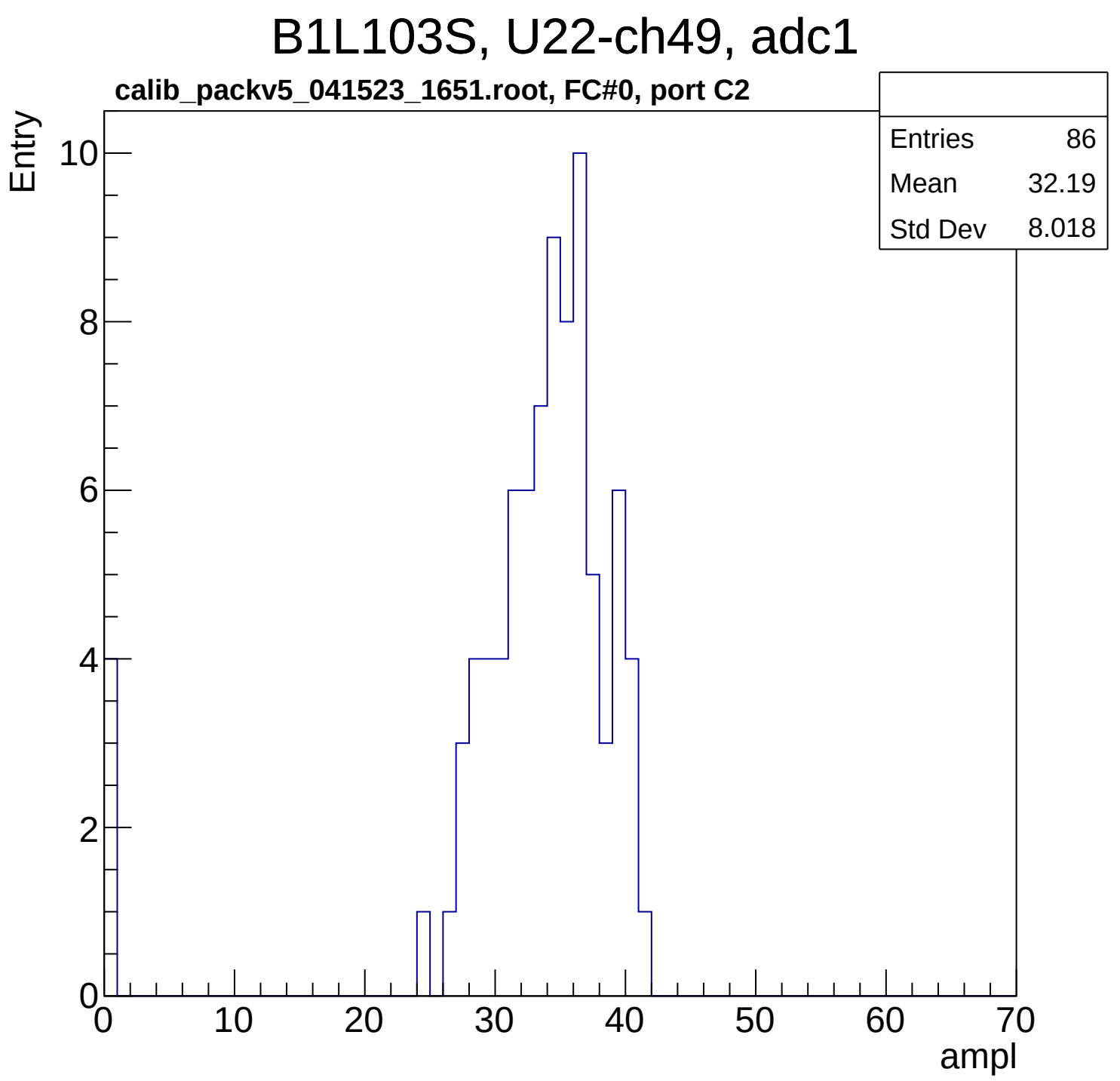
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch49, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 22.18
Std Dev 10.95
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch49, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 32.19
Std Dev 8.018
Entry
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2
4
6
8
10
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10
20
30
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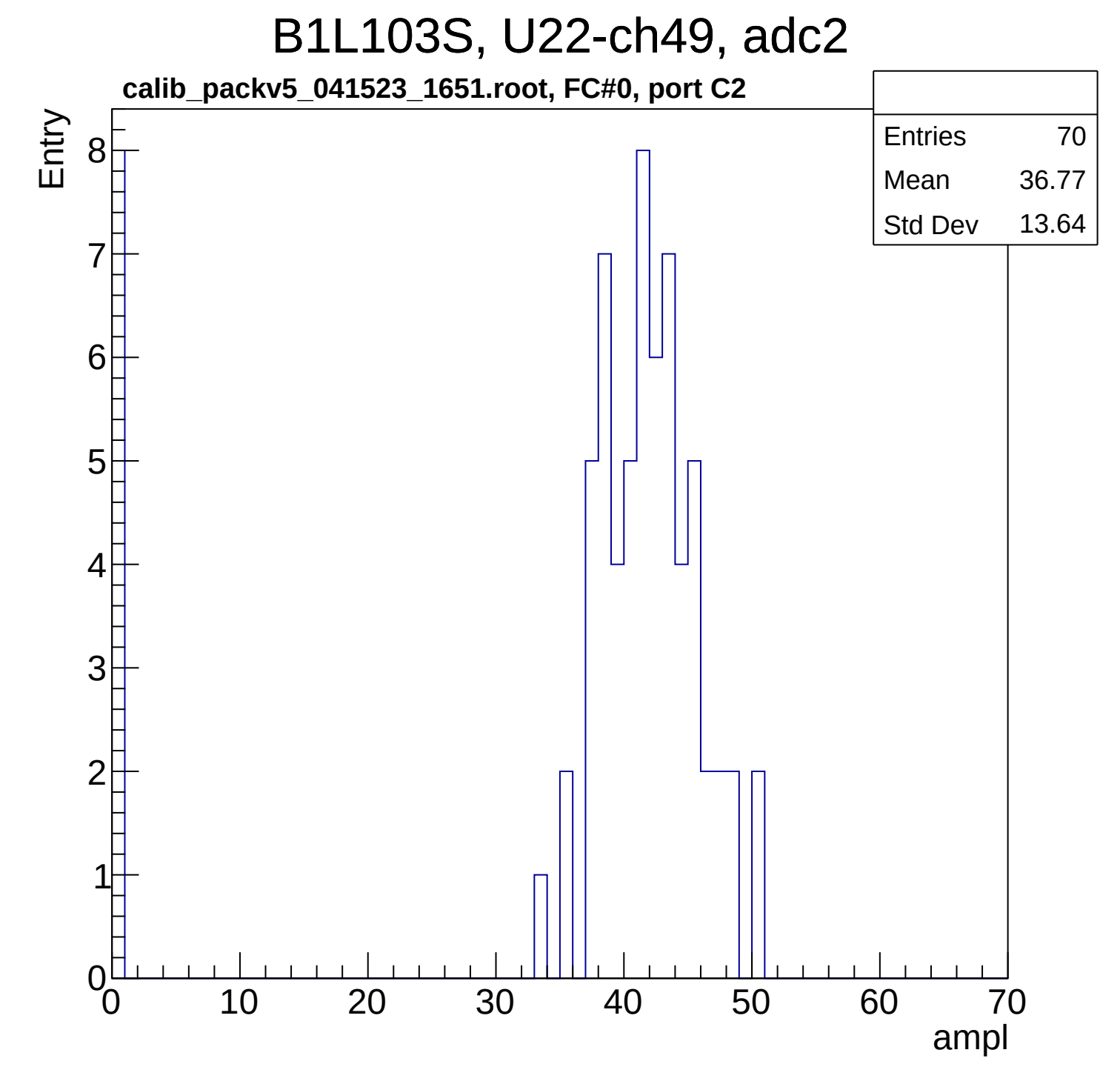
50
60
70
ampl


B1L103S, U22-ch49, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 36.77
Std Dev 13.64
Entry
ampl
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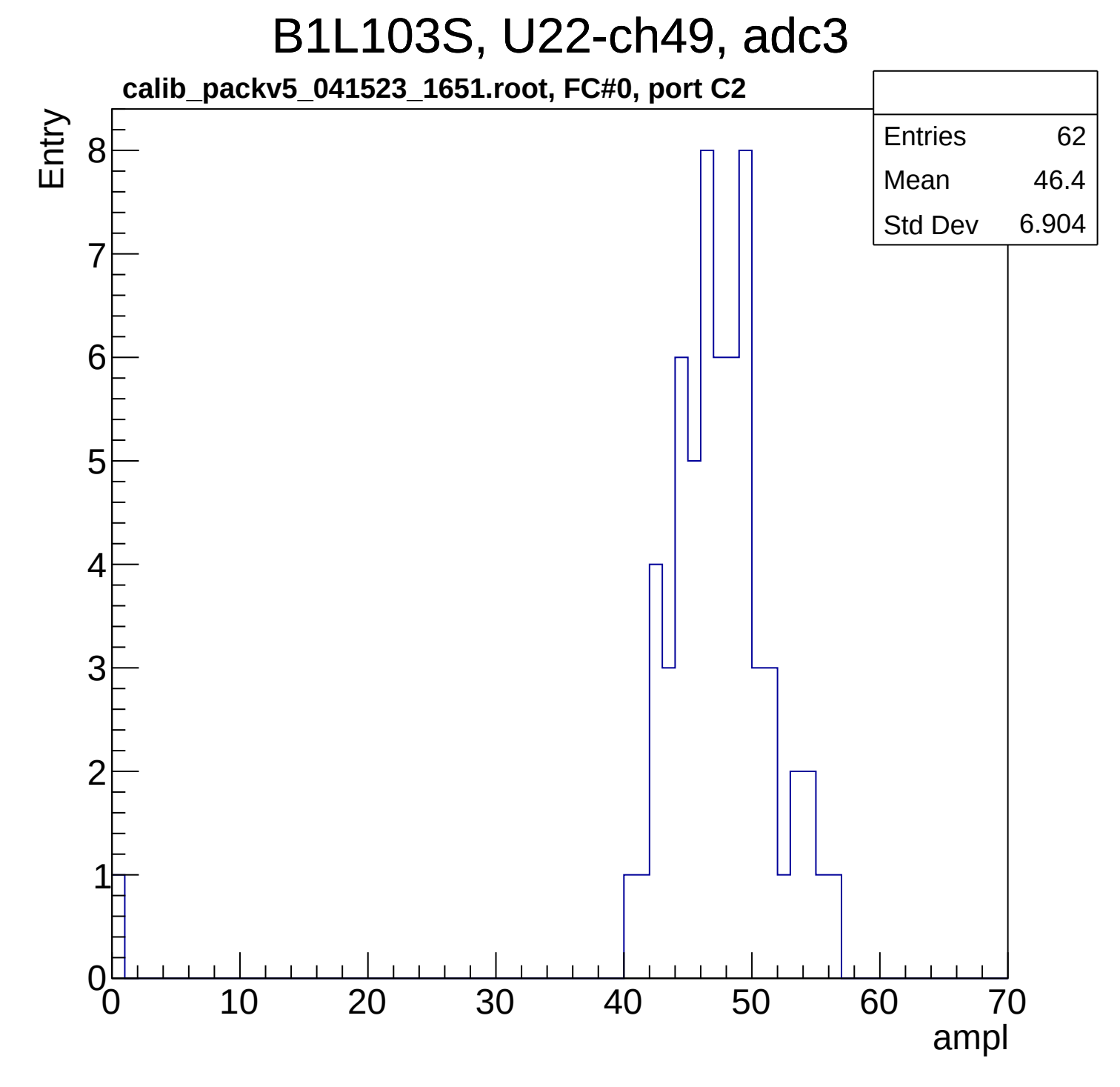
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch49, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 46.4
Std Dev 6.904
Entry
ampl
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1
2
3
4
5
6
7
8
0
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60
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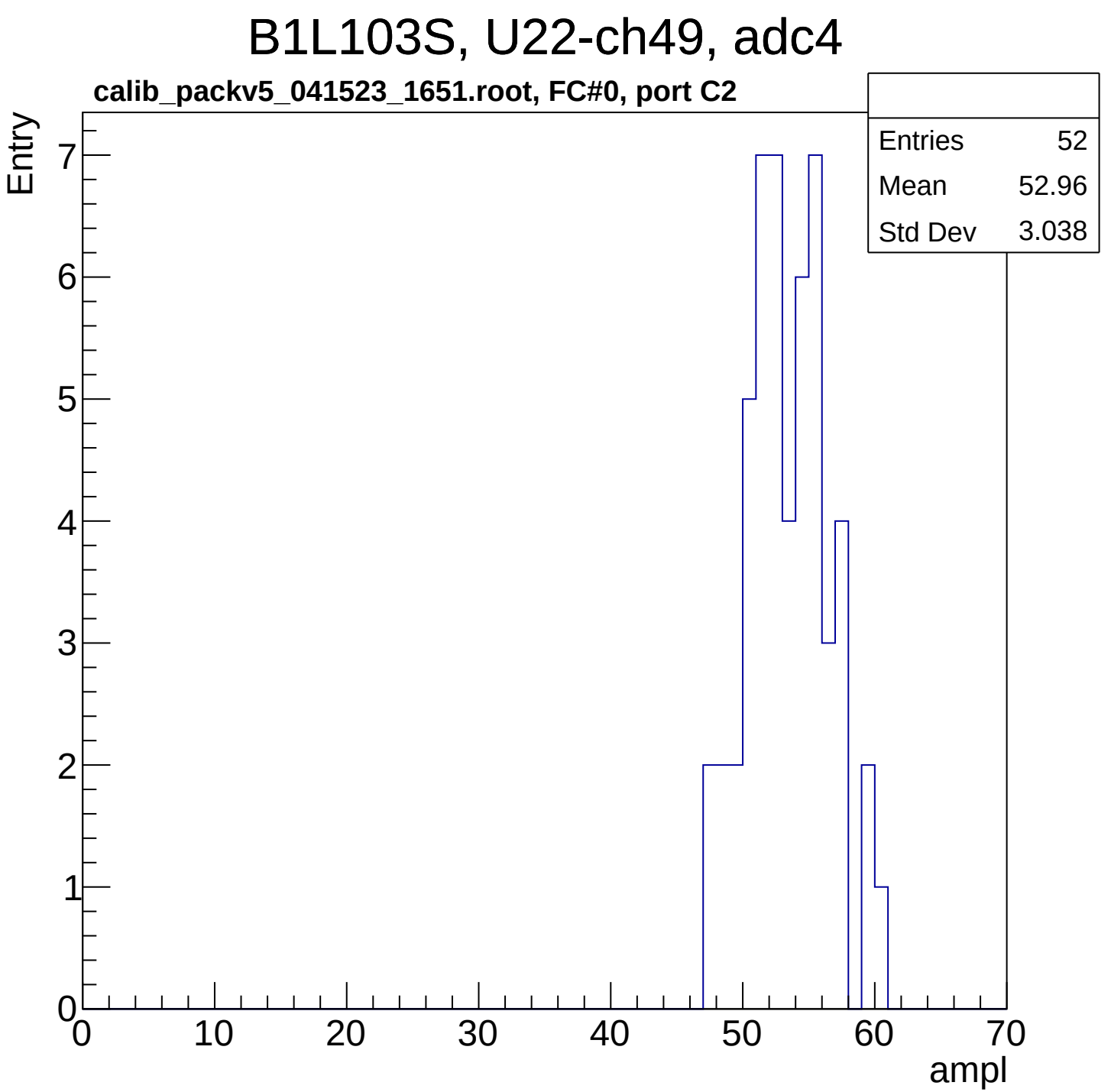
B1L103S, U22-ch49, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 52.96
Std Dev 3.038
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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60
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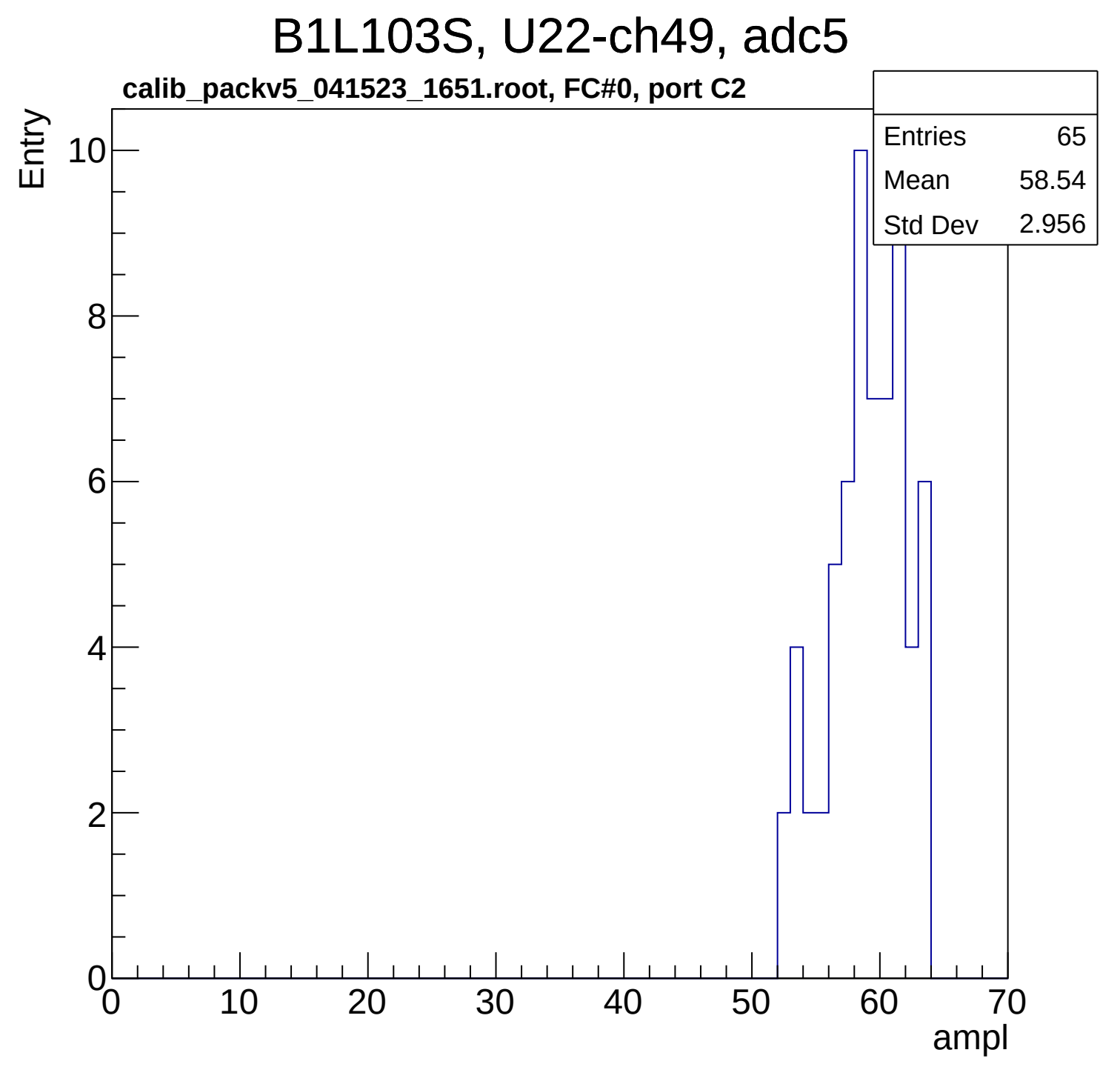
B1L103S, U22-ch49, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 58.54
Std Dev 2.956
Entry
ampl
0
2
4
6
8
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0
10
20
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40
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60
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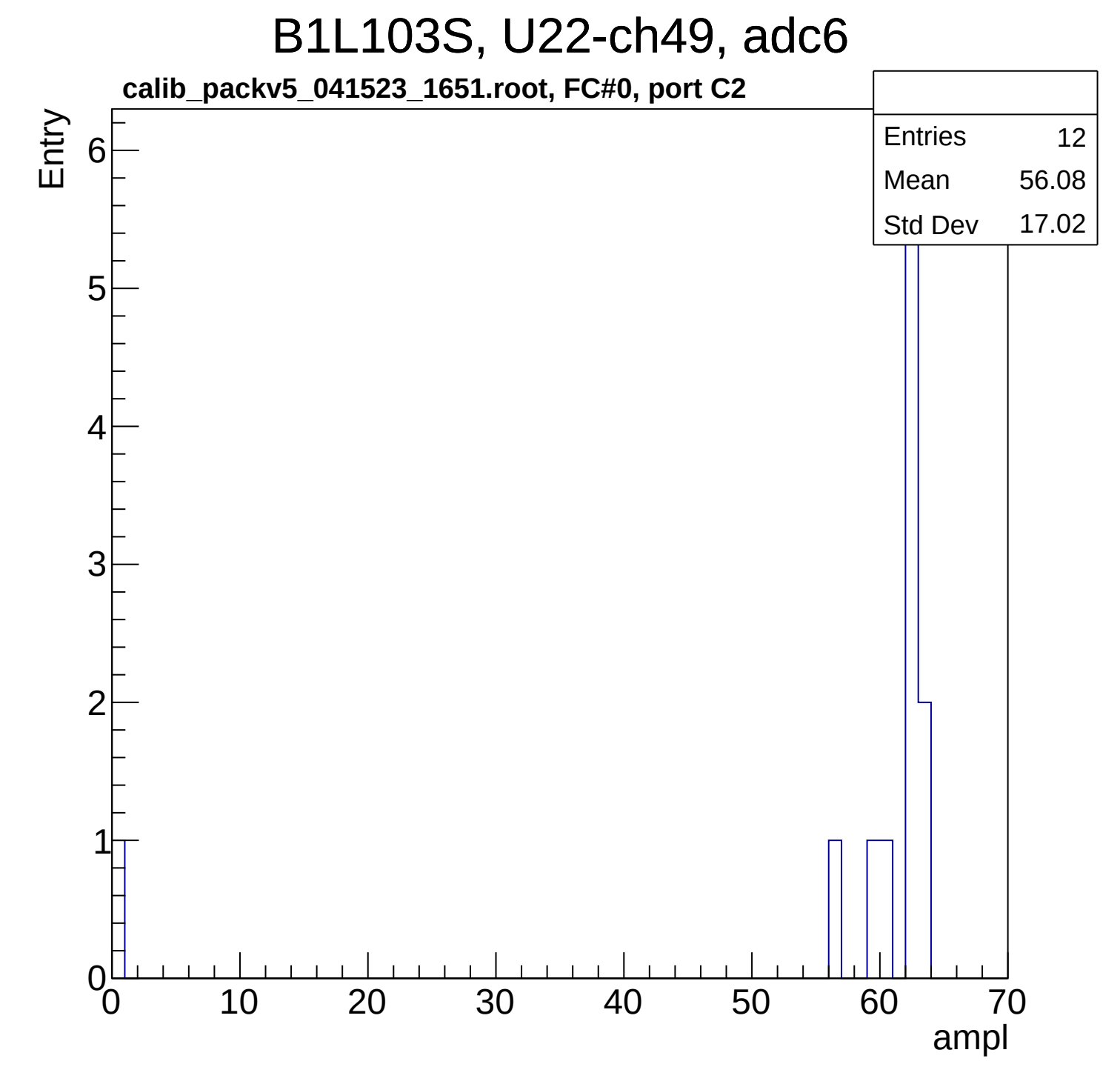
B1L103S, U22-ch49, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 56.08
Std Dev 17.02
Entry
ampl
0
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3
4
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0
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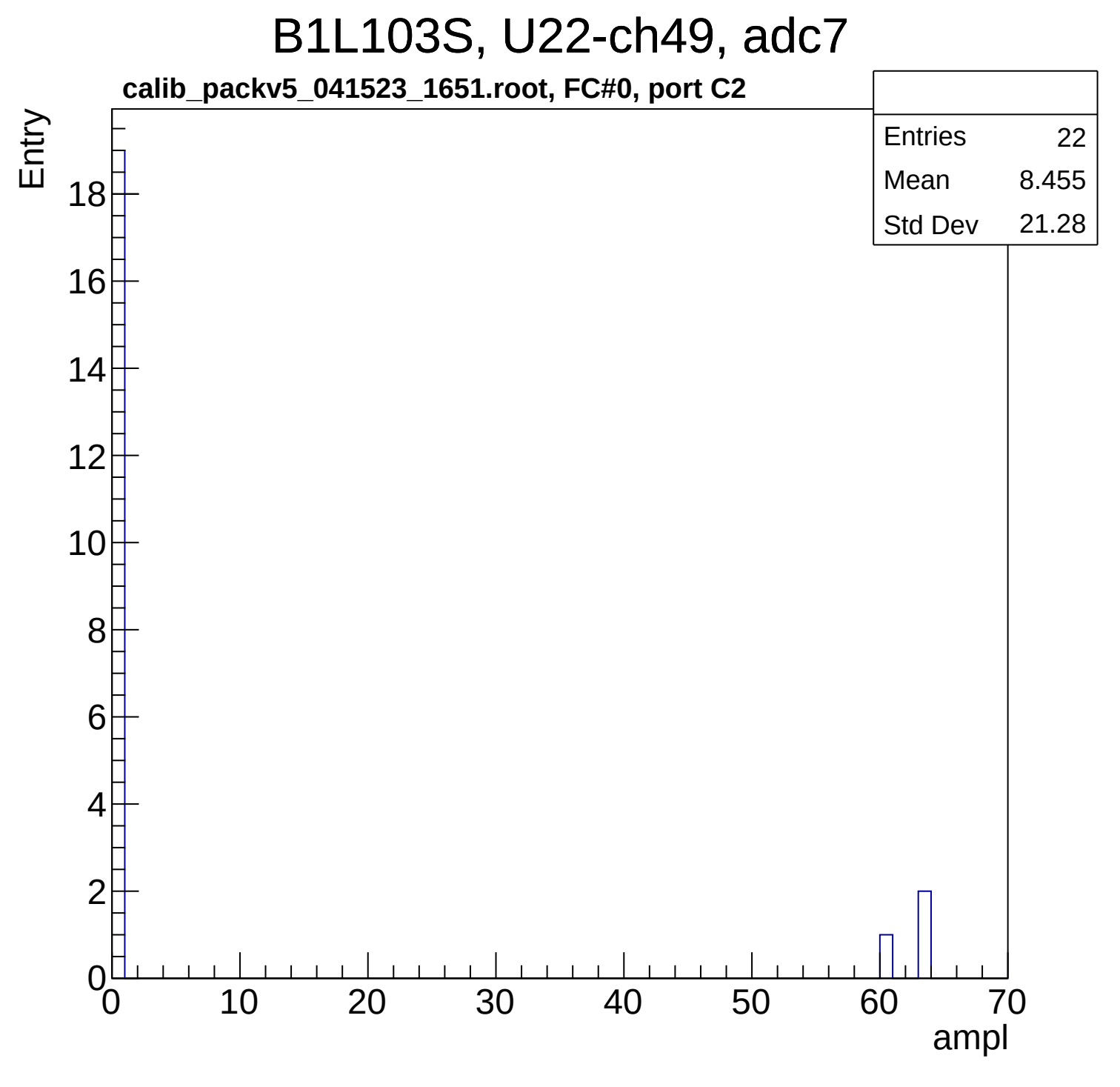
B1L103S, U22-ch49, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.455
Std Dev 21.28
Entry
0
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6
8
10
12
14
16
18
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10
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30
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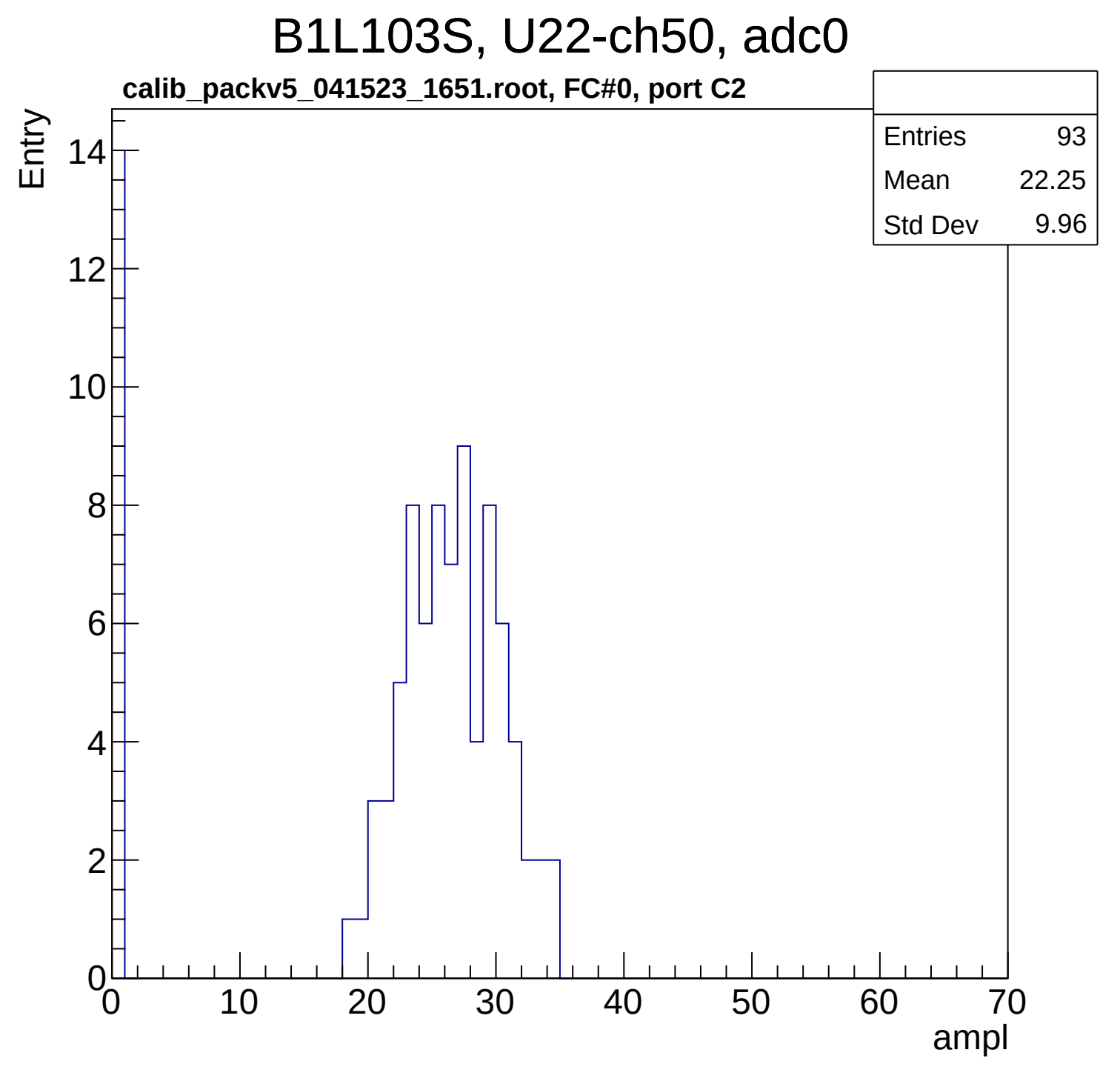
50
60
70
ampl


B1L103S, U22-ch50, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 22.25
Std Dev 9.96
Entry
ampl
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2
4
6
8
10
12
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0
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60
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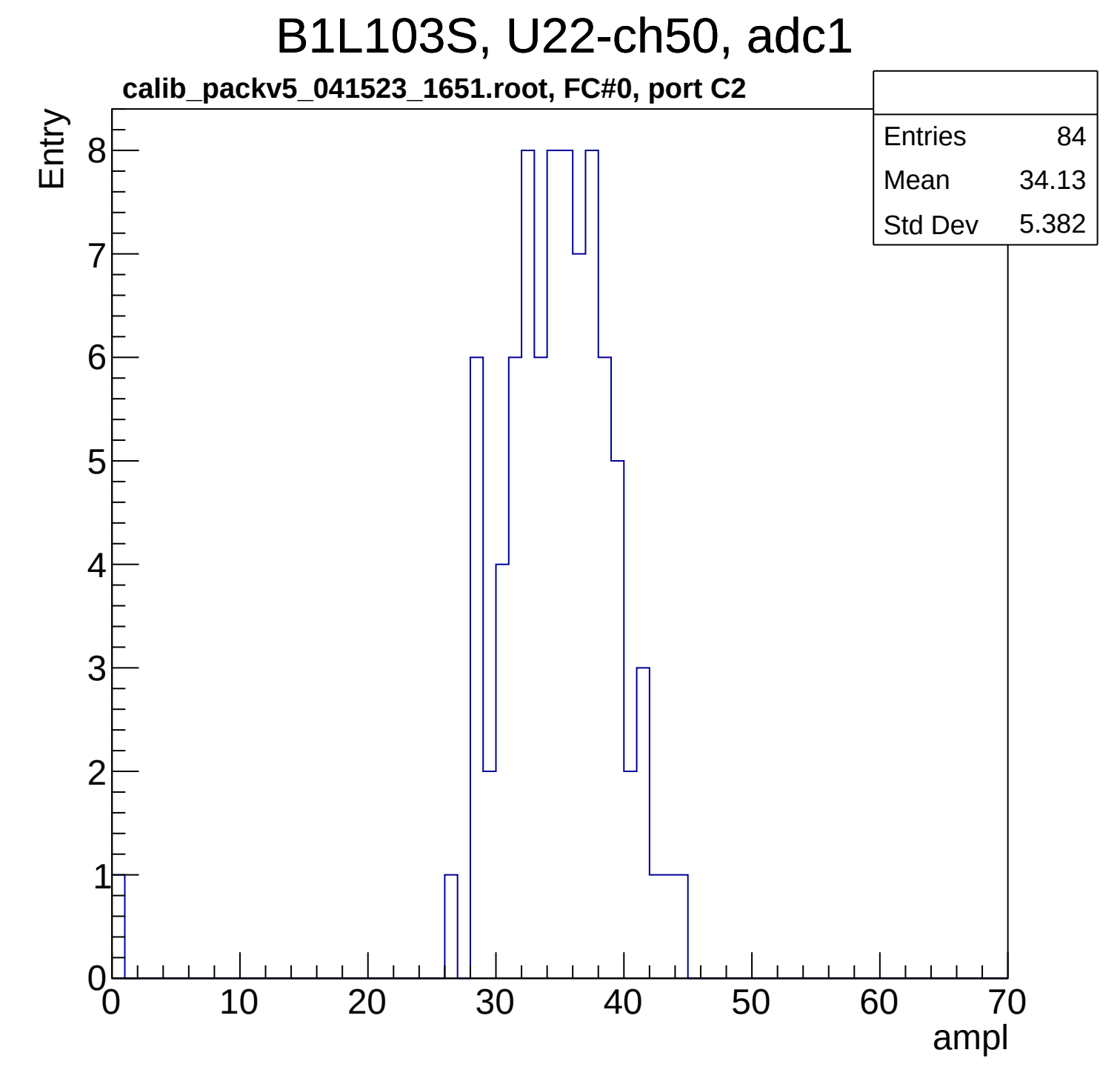
B1L103S, U22-ch50, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 34.13
Std Dev 5.382
Entry
ampl
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2
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4
5
6
7
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0
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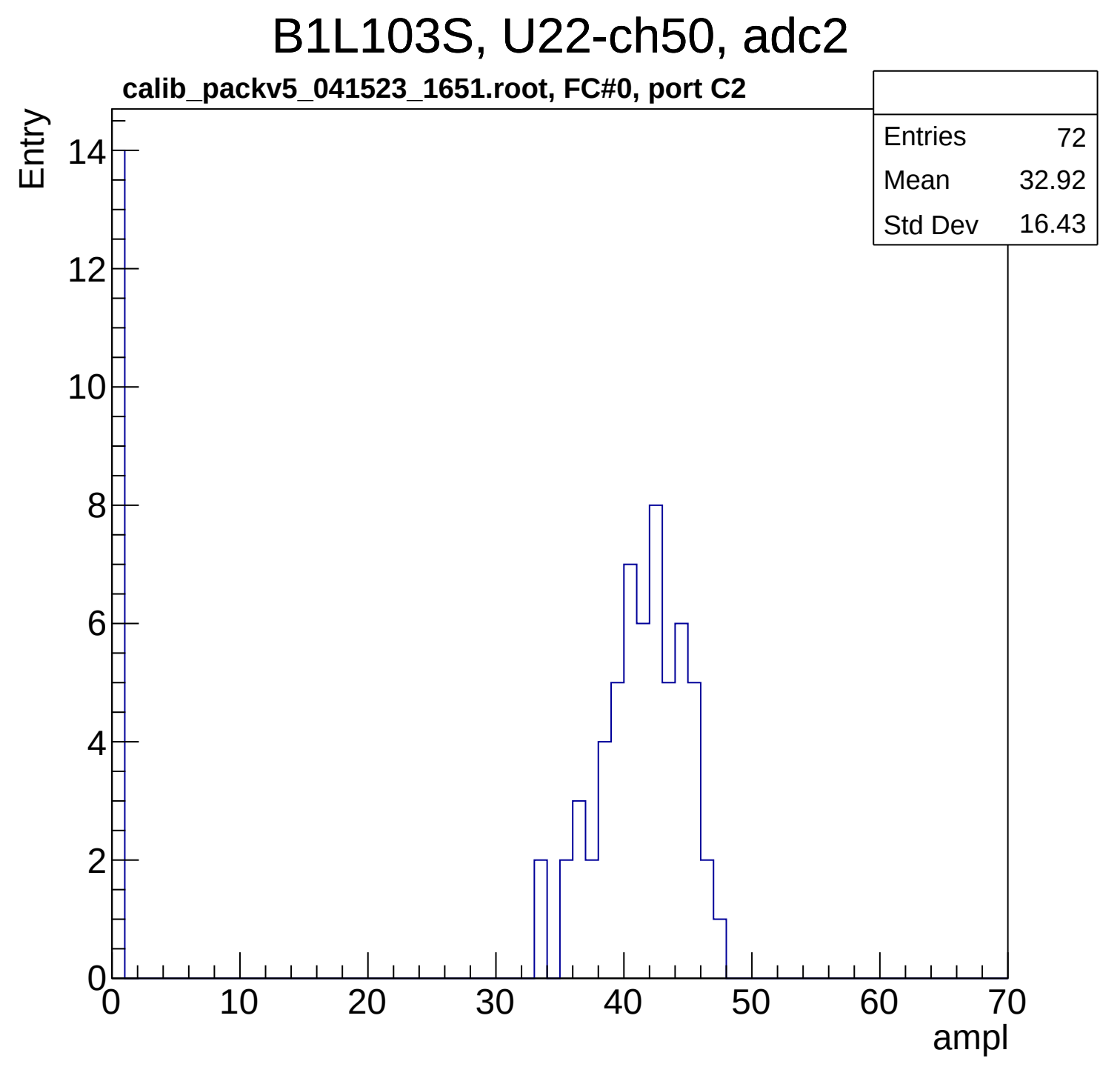
B1L103S, U22-ch50, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 32.92
Std Dev 16.43
Entry
ampl
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2
4
6
8
10
12
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0
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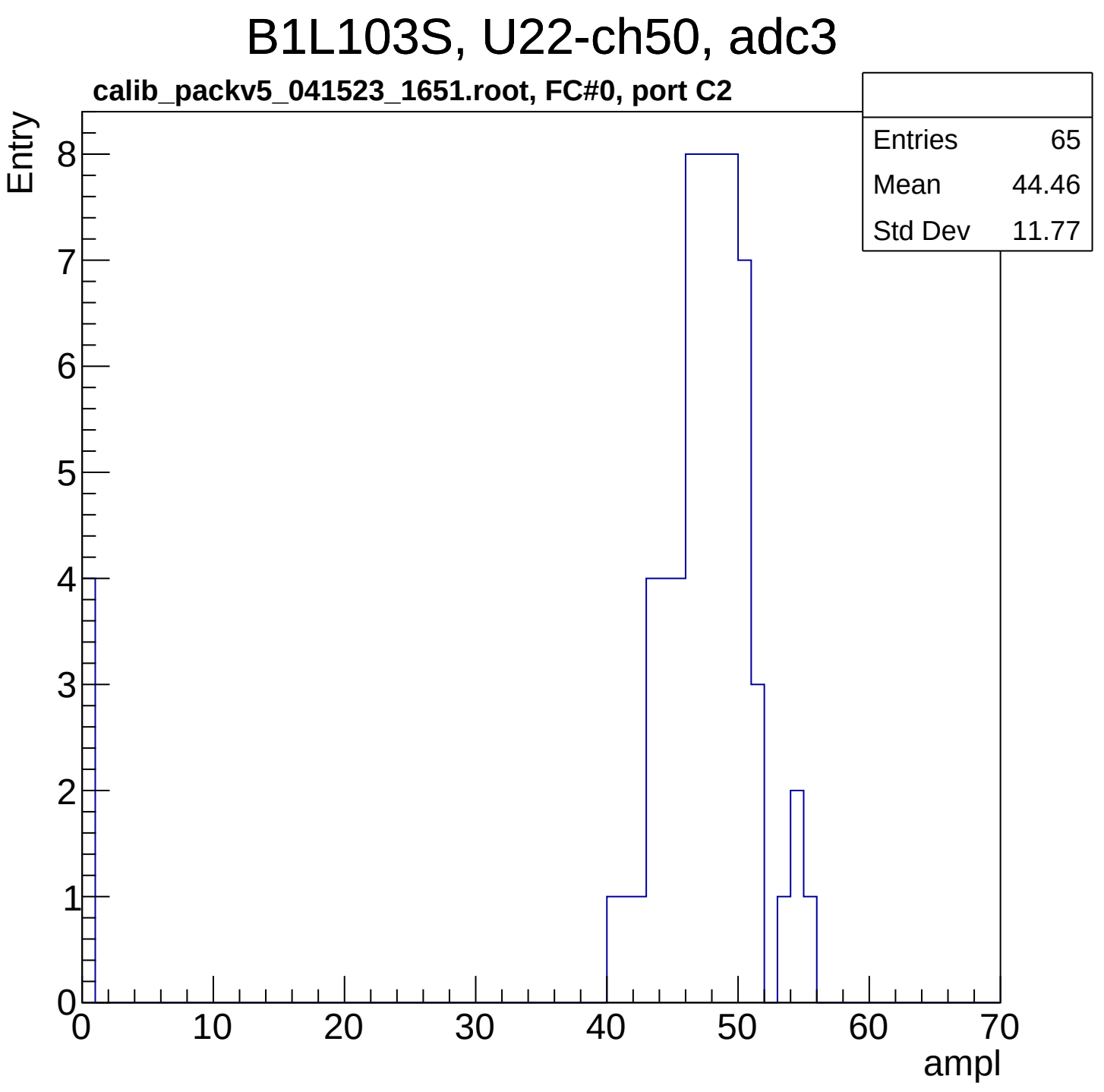
B1L103S, U22-ch50, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 44.46
Std Dev 11.77
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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60
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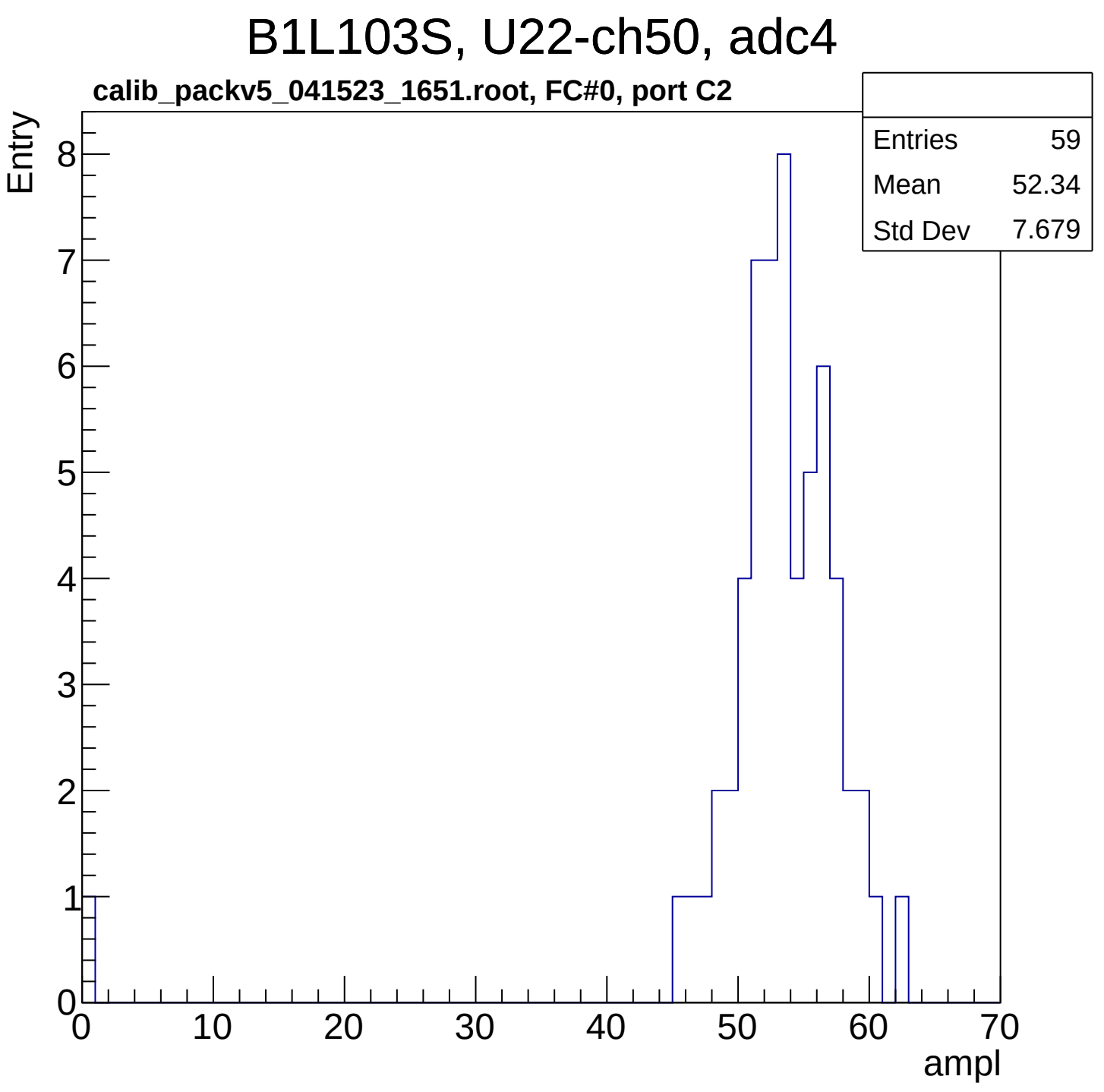
B1L103S, U22-ch50, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 52.34
Std Dev 7.679
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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60
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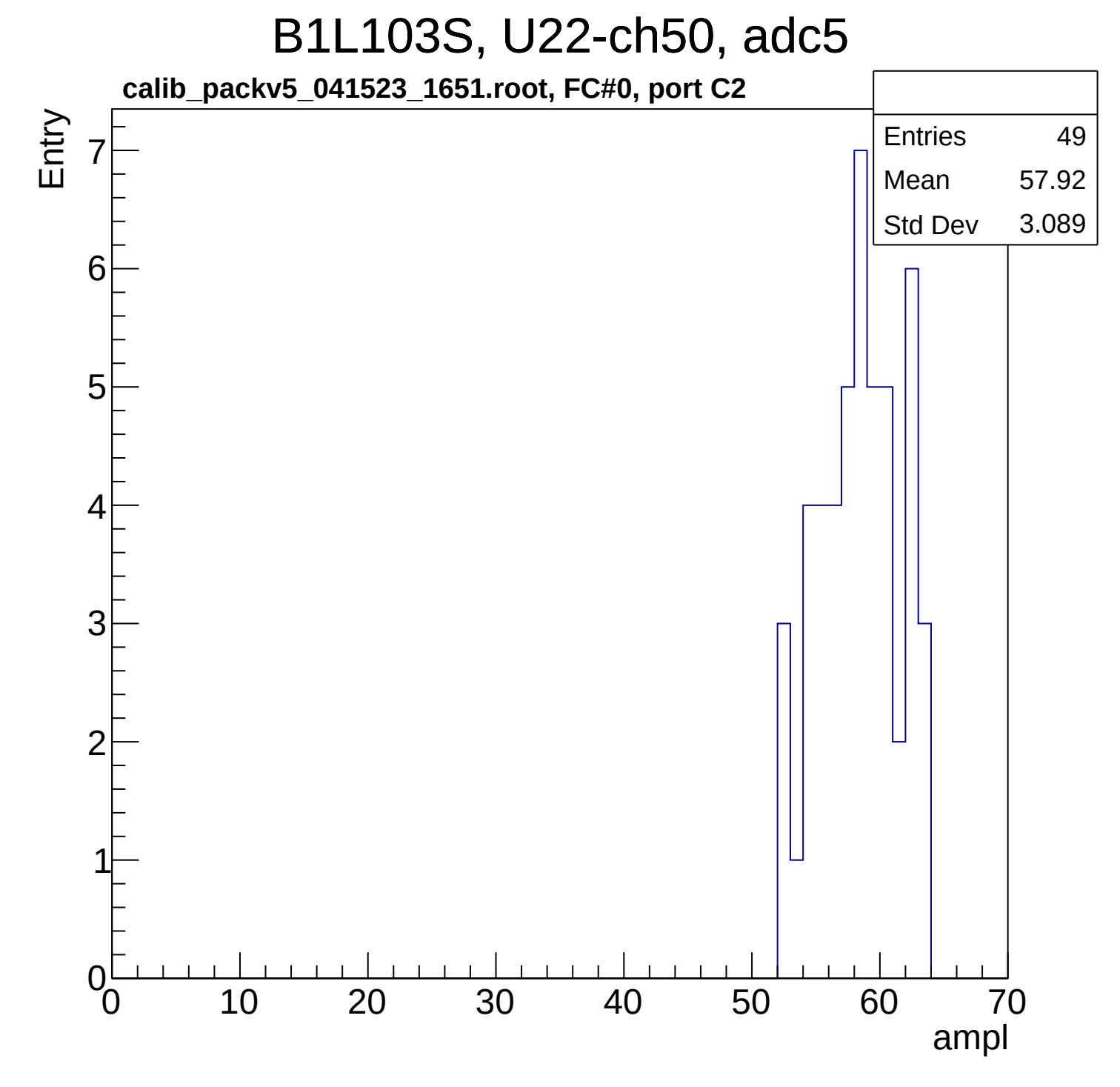
B1L103S, U22-ch50, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 57.92
Std Dev 3.089
Entry
ampl
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4
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6
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0
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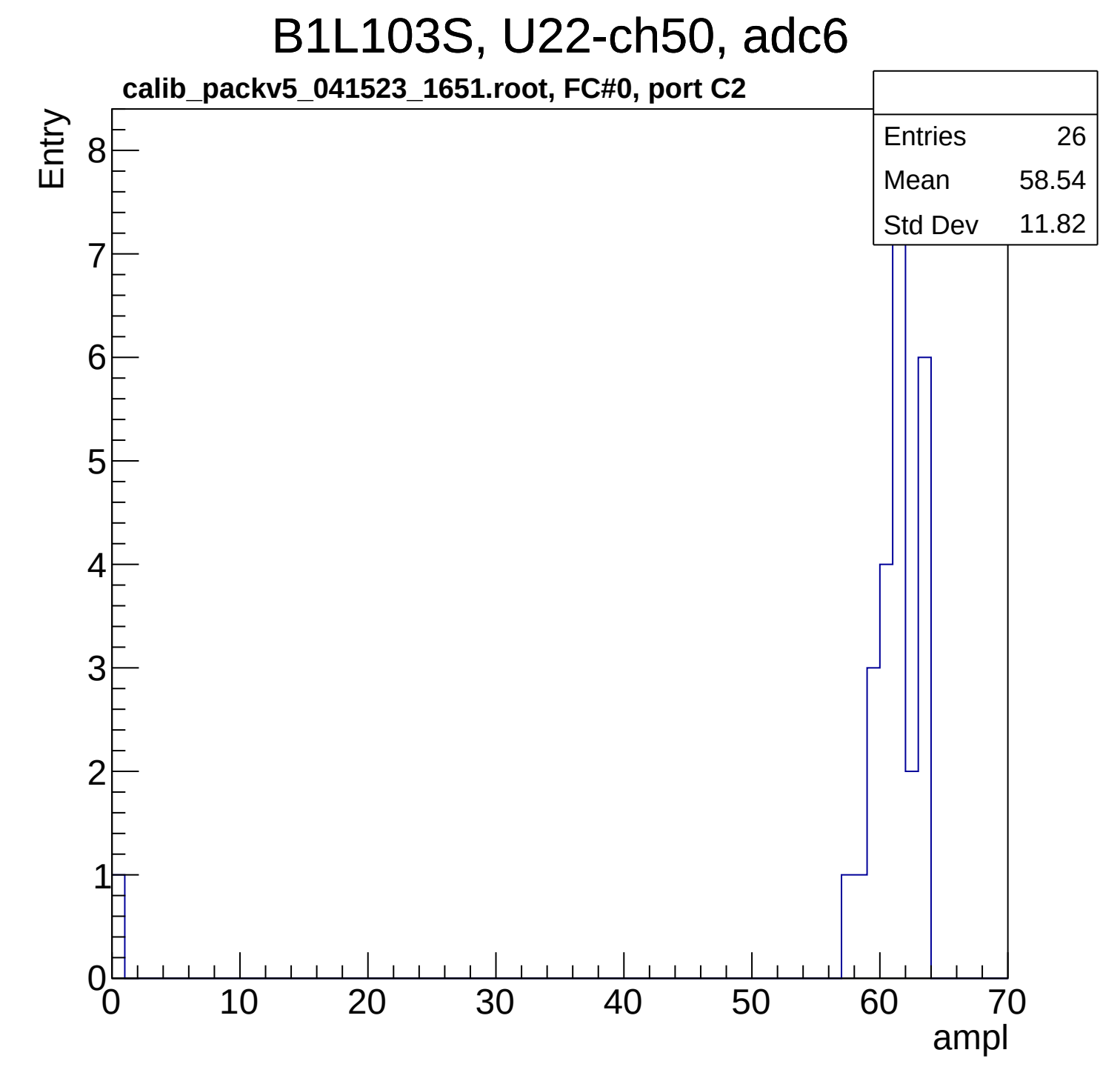
B1L103S, U22-ch50, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 58.54
Std Dev 11.82
Entry
ampl
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5
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7
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0
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60
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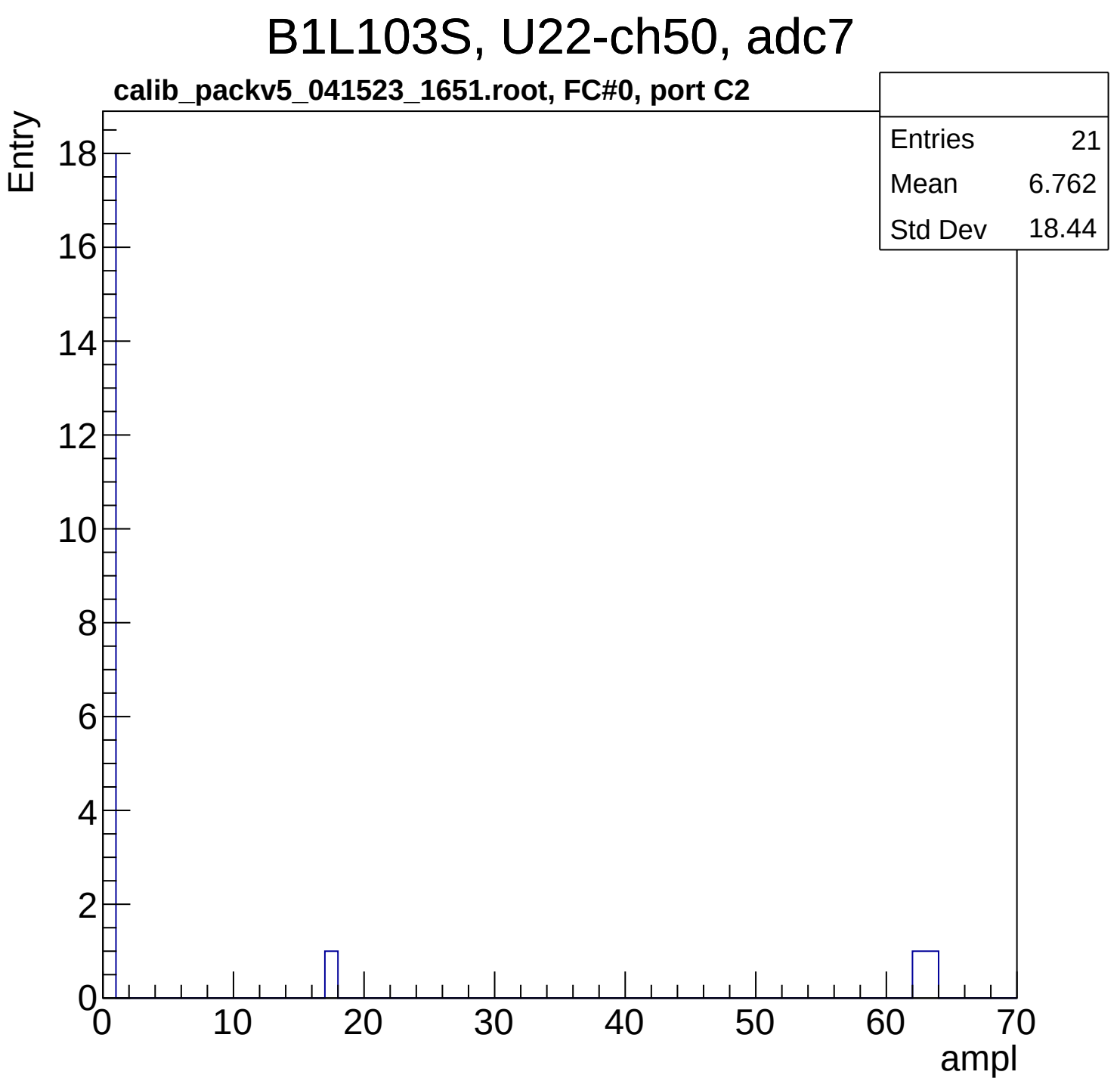
B1L103S, U22-ch50, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 6.762
Std Dev 18.44
Entry
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6
8
10
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14
16
18
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30
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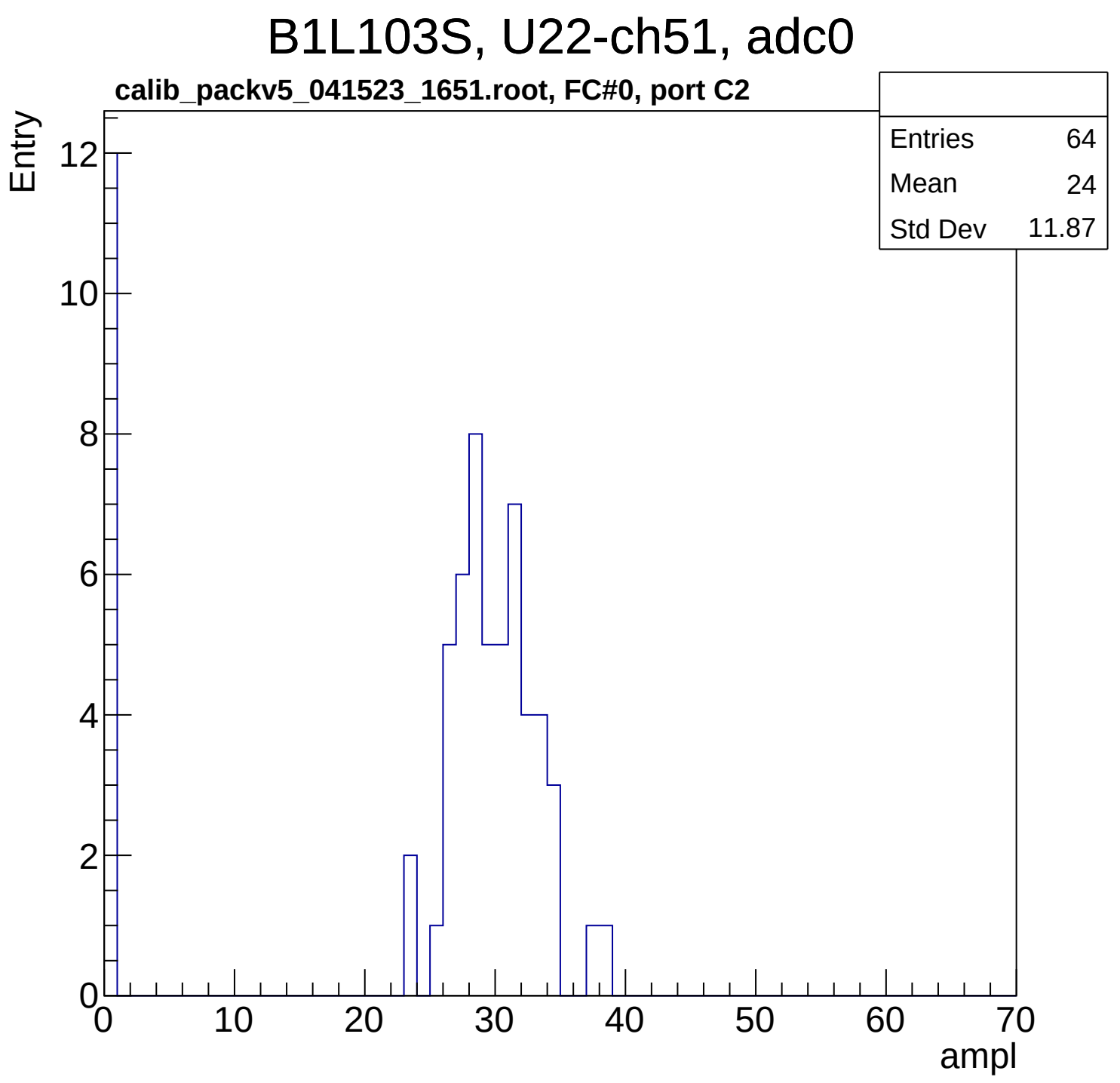
50
60
70
ampl


B1L103S, U22-ch51, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 24
Std Dev 11.87
Entry
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8
10
12
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10
20
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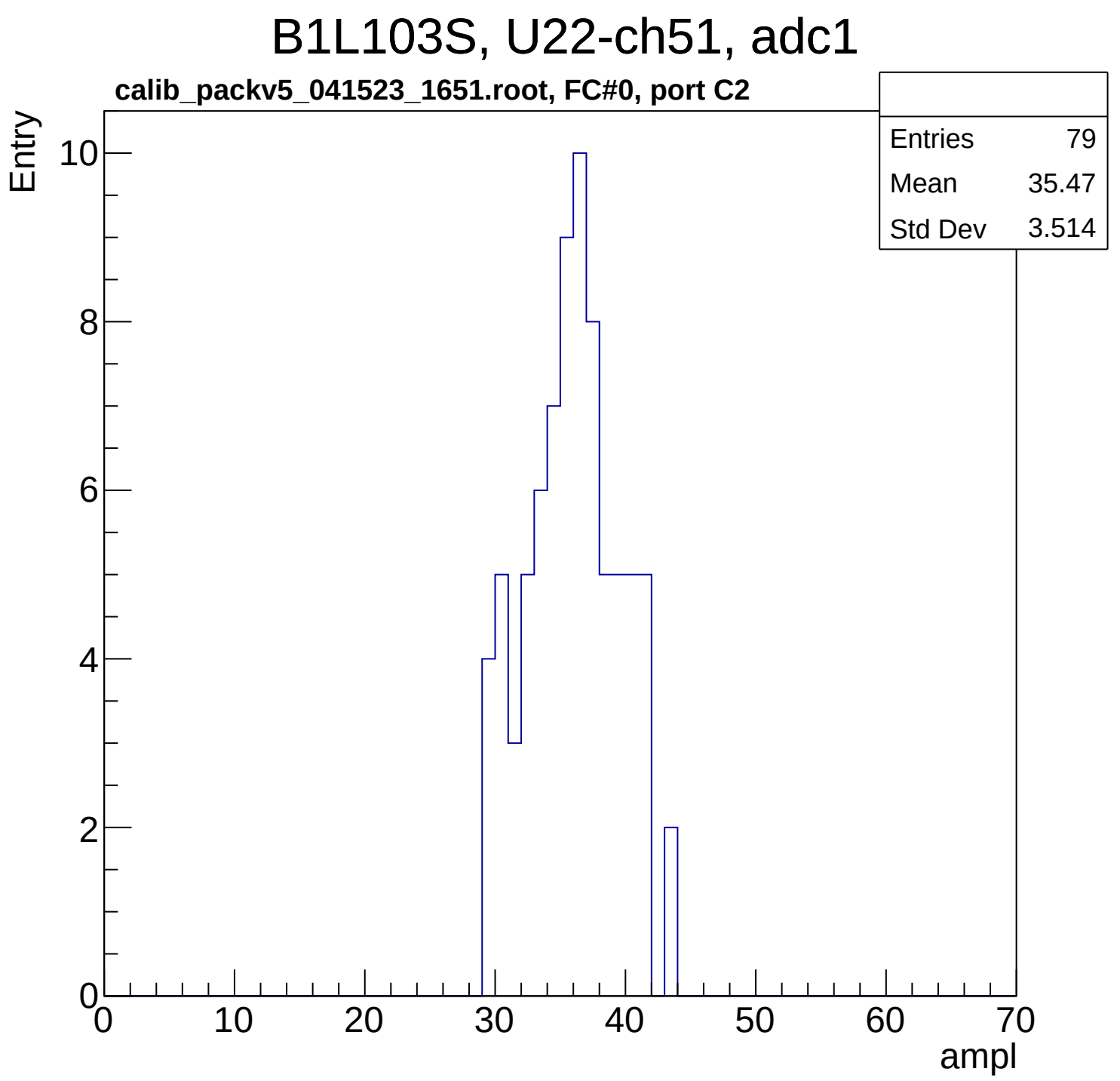
50
60
70
ampl


B1L103S, U22-ch51, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 35.47
Std Dev 3.514
Entry
ampl
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6
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0
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60
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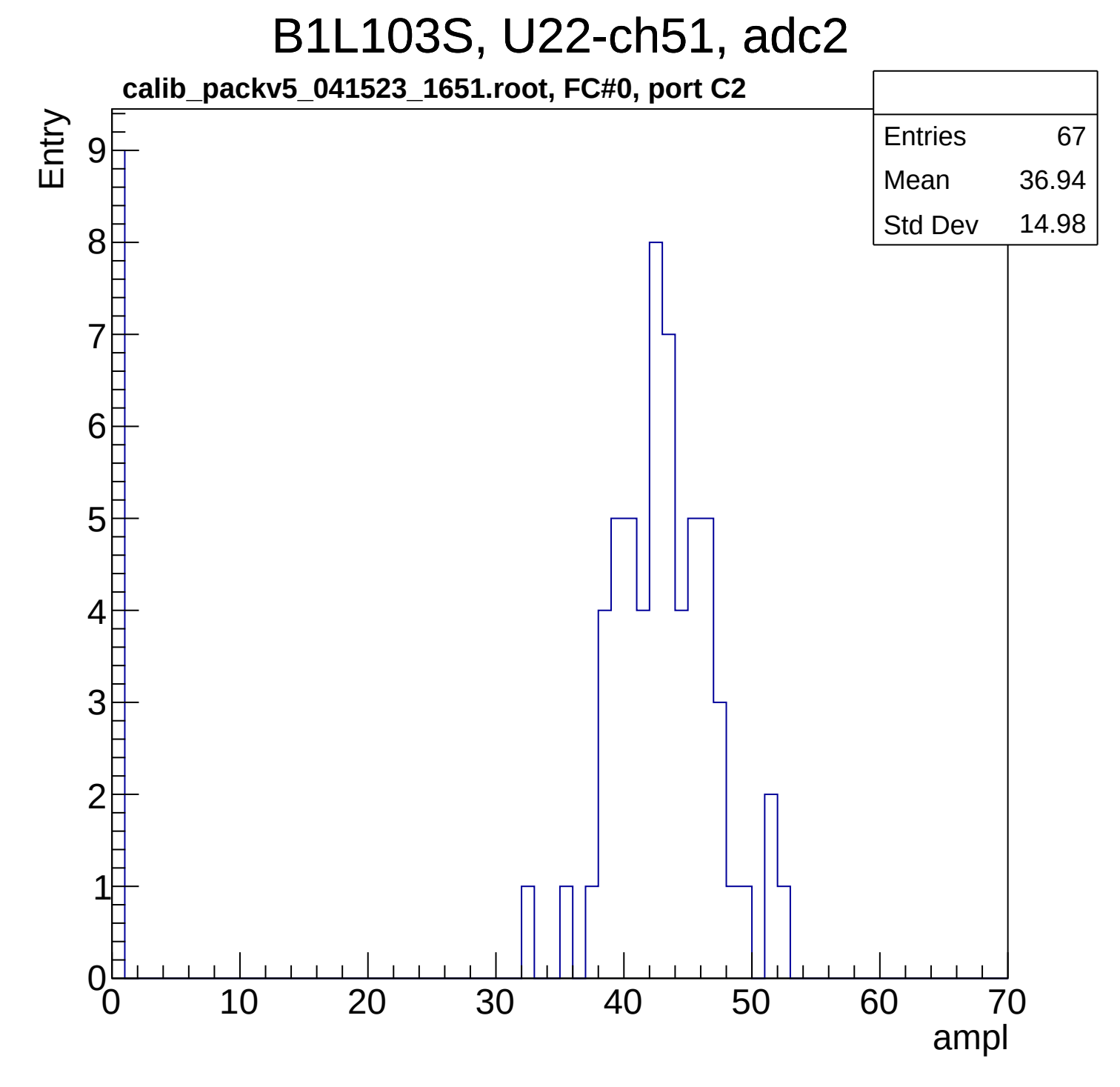
B1L103S, U22-ch51, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 36.94
Std Dev 14.98
Entry
ampl
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4
5
6
7
8
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0
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40
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60
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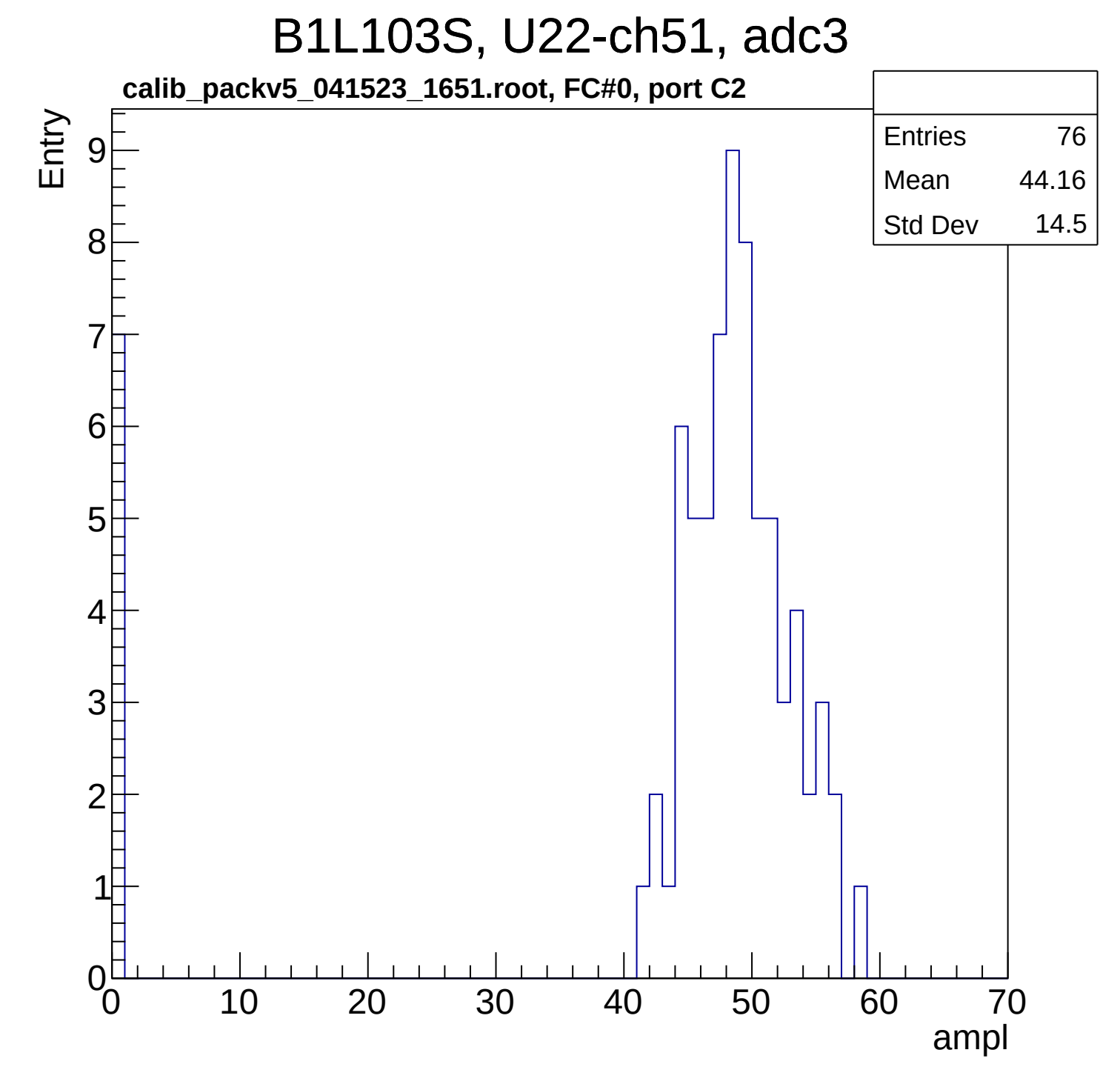
B1L103S, U22-ch51, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 44.16
Std Dev 14.5
Entry
ampl
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2
3
4
5
6
7
8
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0
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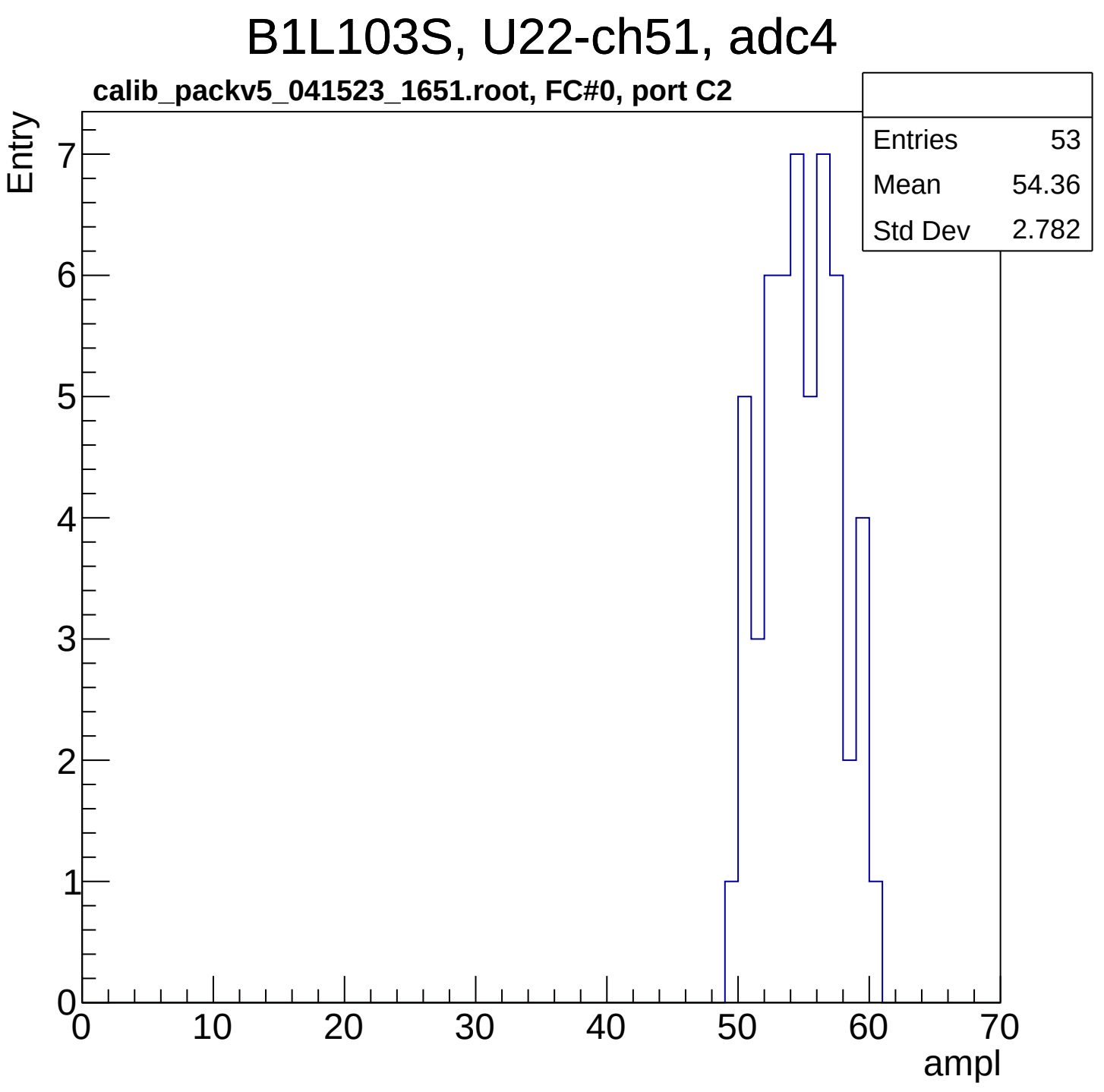
B1L103S, U22-ch51, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 54.36
Std Dev 2.782
Entry
ampl
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4
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6
7
0
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60
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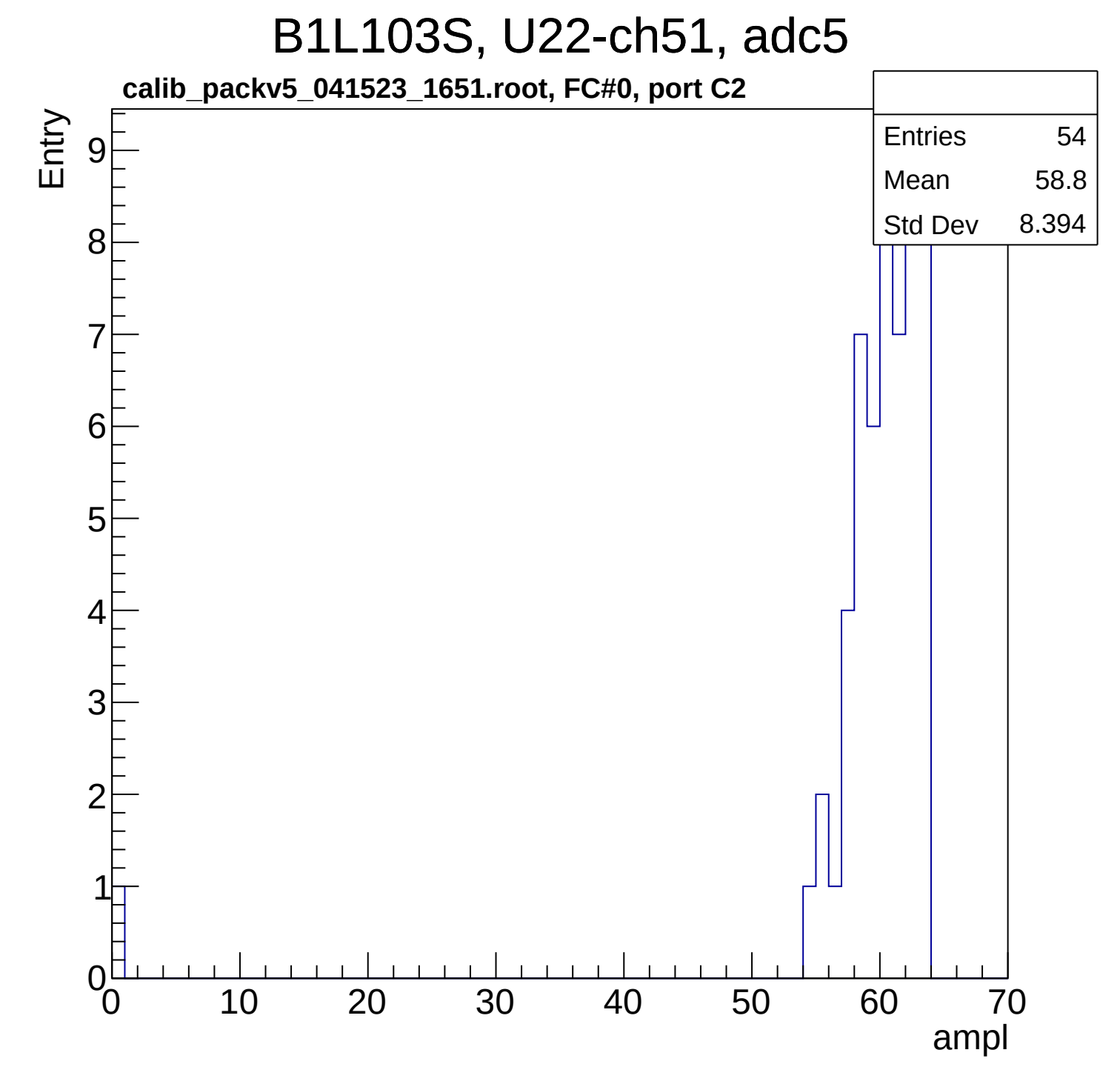
B1L103S, U22-ch51, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 58.8
Std Dev 8.394
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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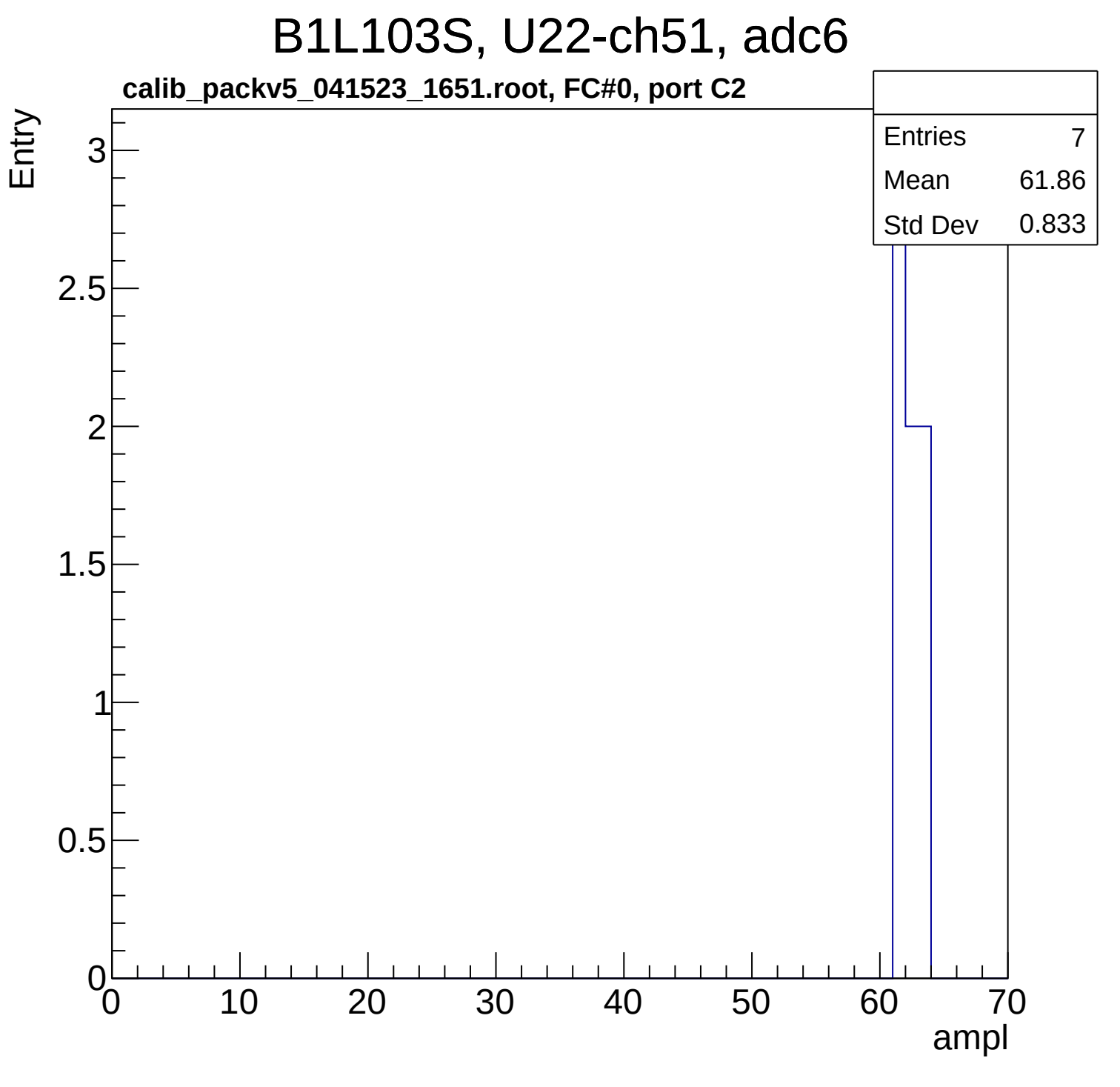
B1L103S, U22-ch51, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 61.86
Std Dev 0.833
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
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20
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40
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60
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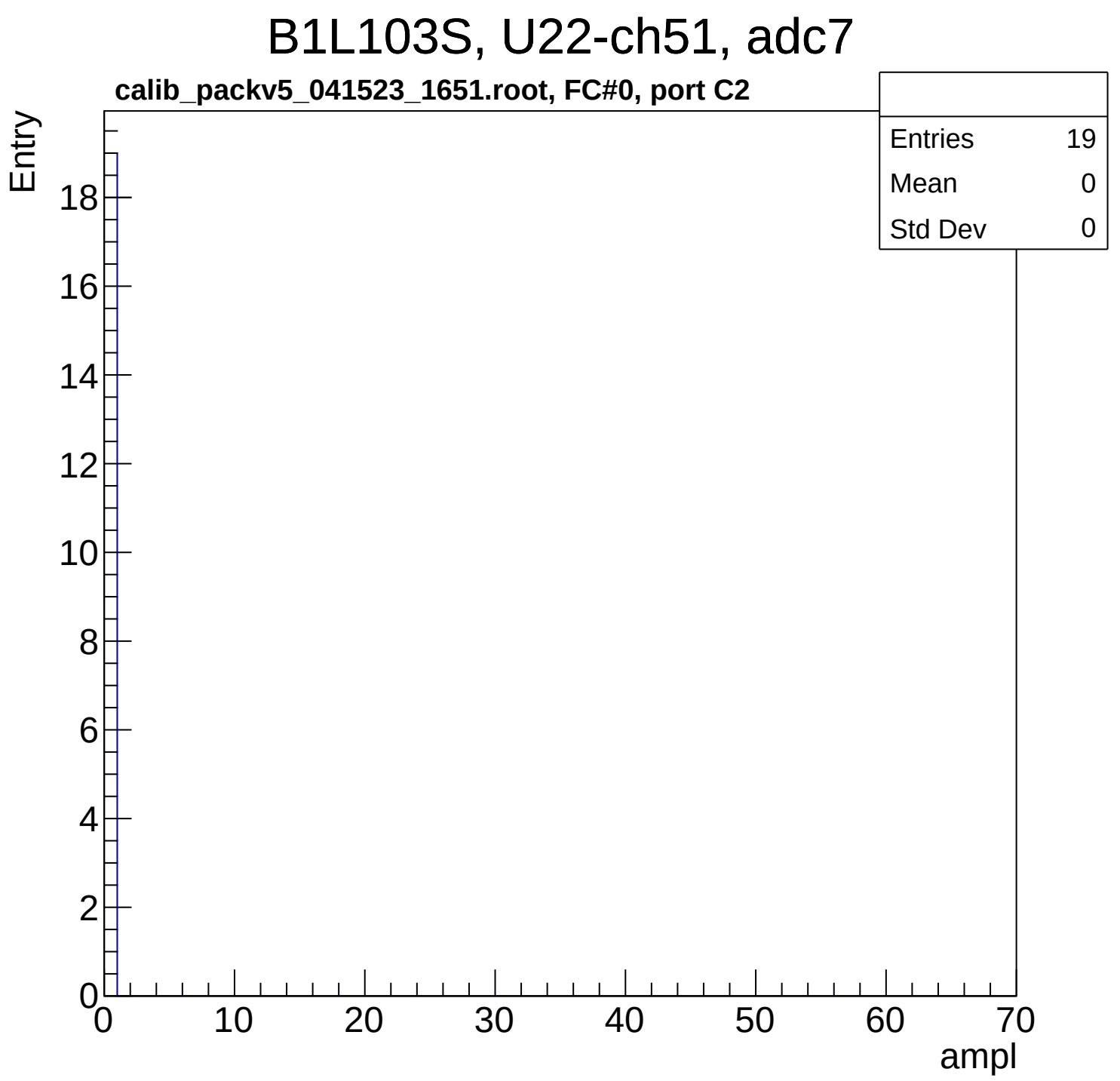
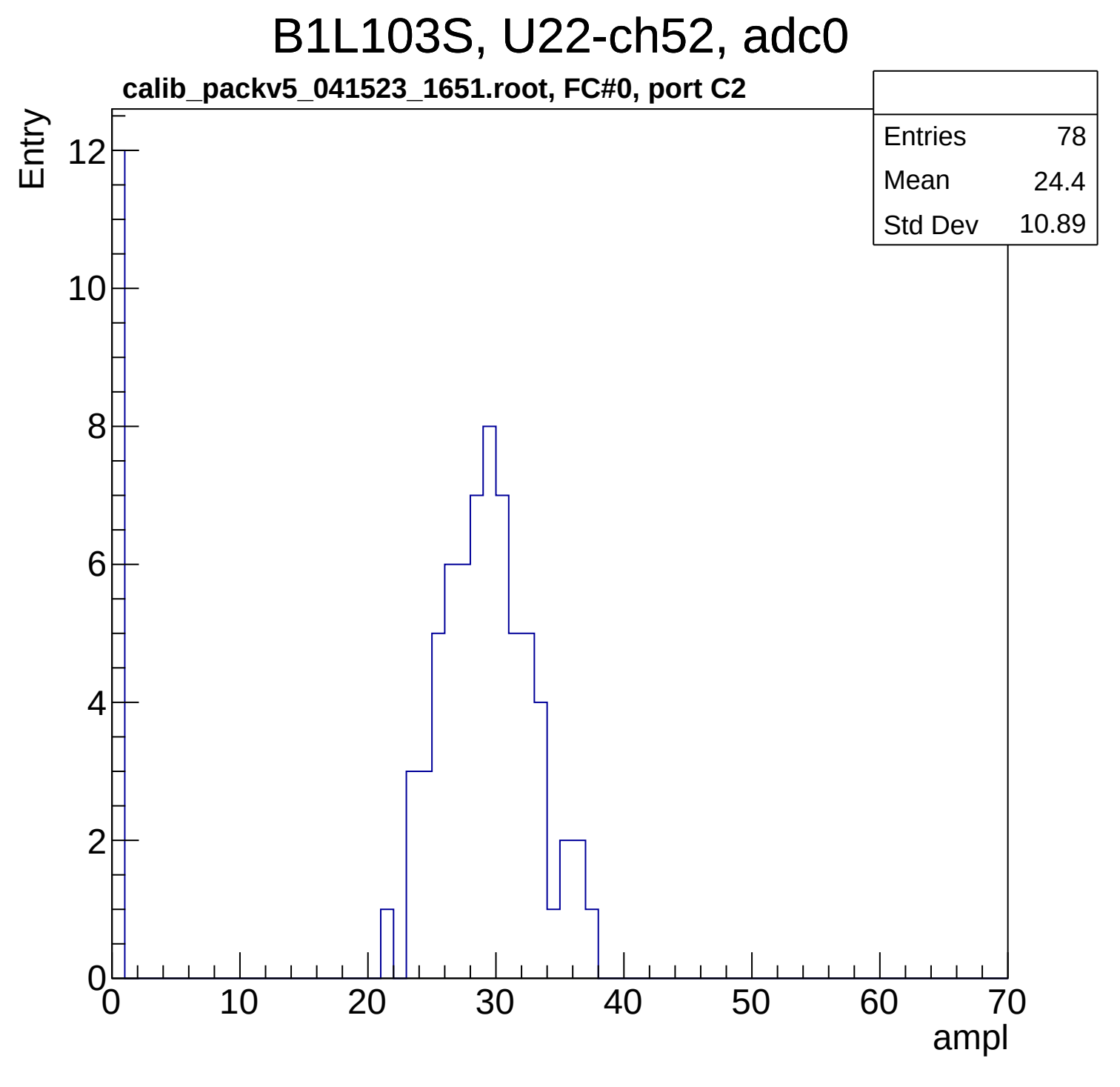
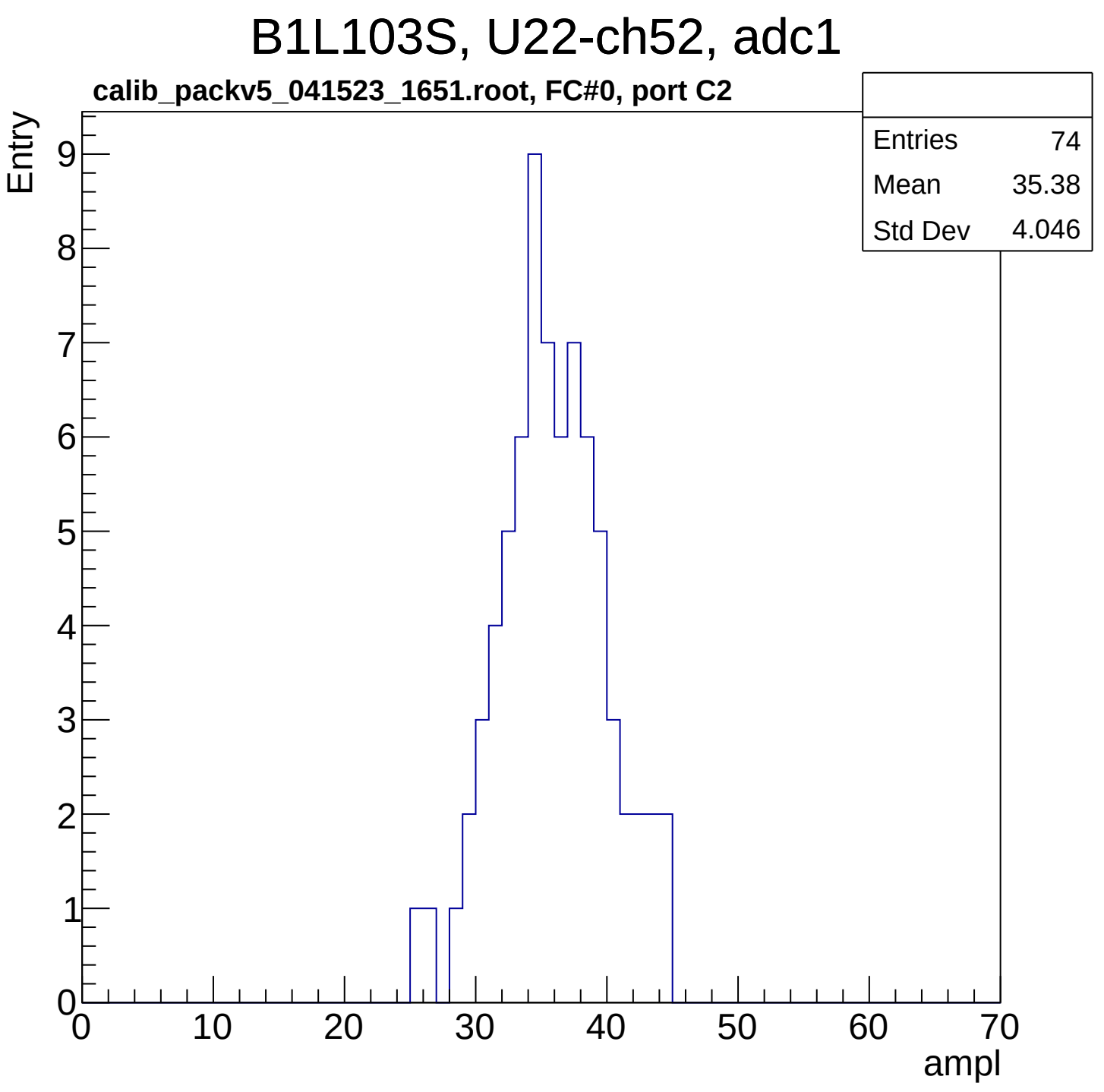

B1L103S, U22-ch51, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch52, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 24.4
Std Dev 10.89
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U22-ch52, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 35.38
Std Dev 4.046
Entry
ampl
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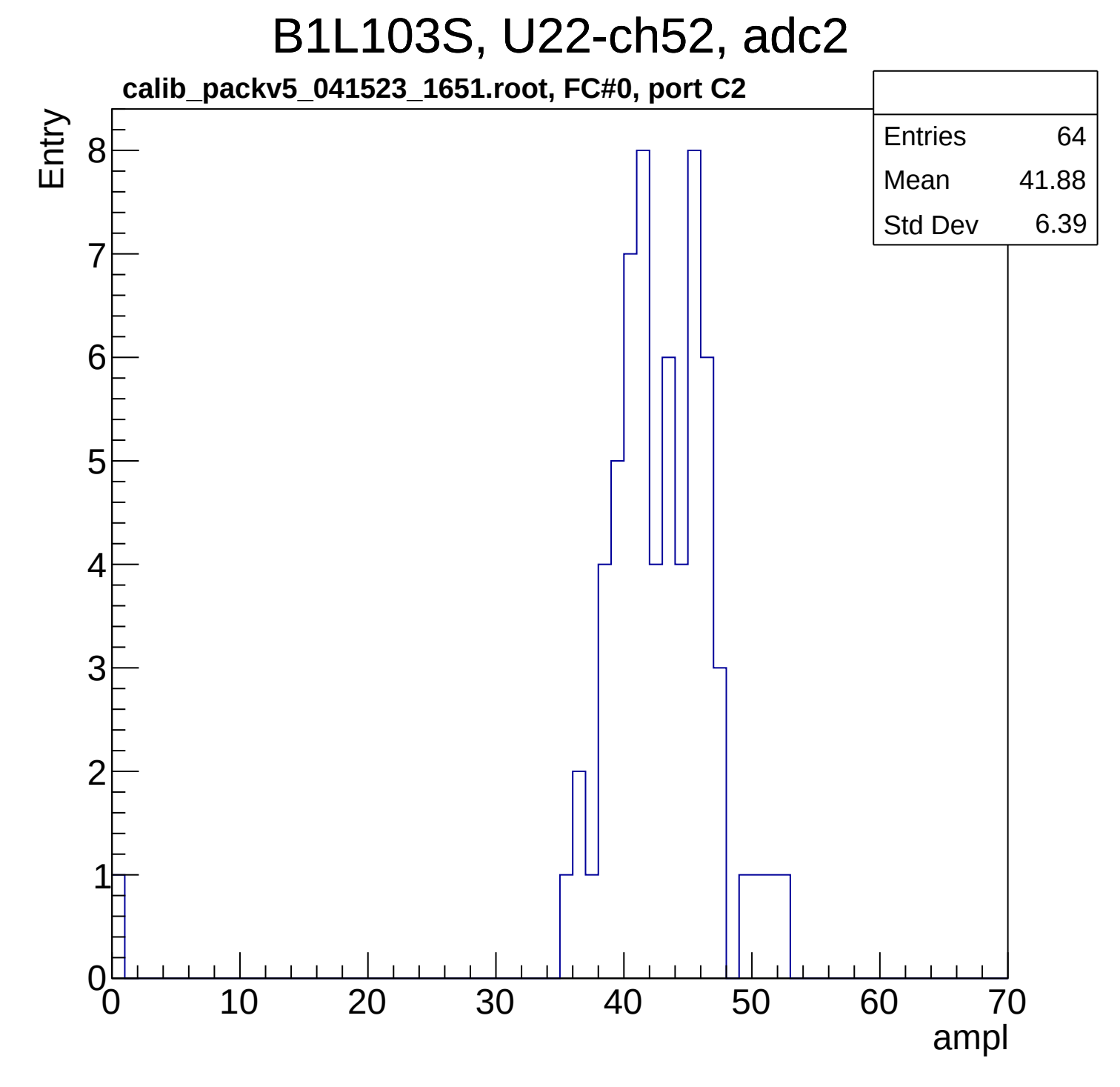
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch52, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 41.88
Std Dev 6.39
Entry
ampl
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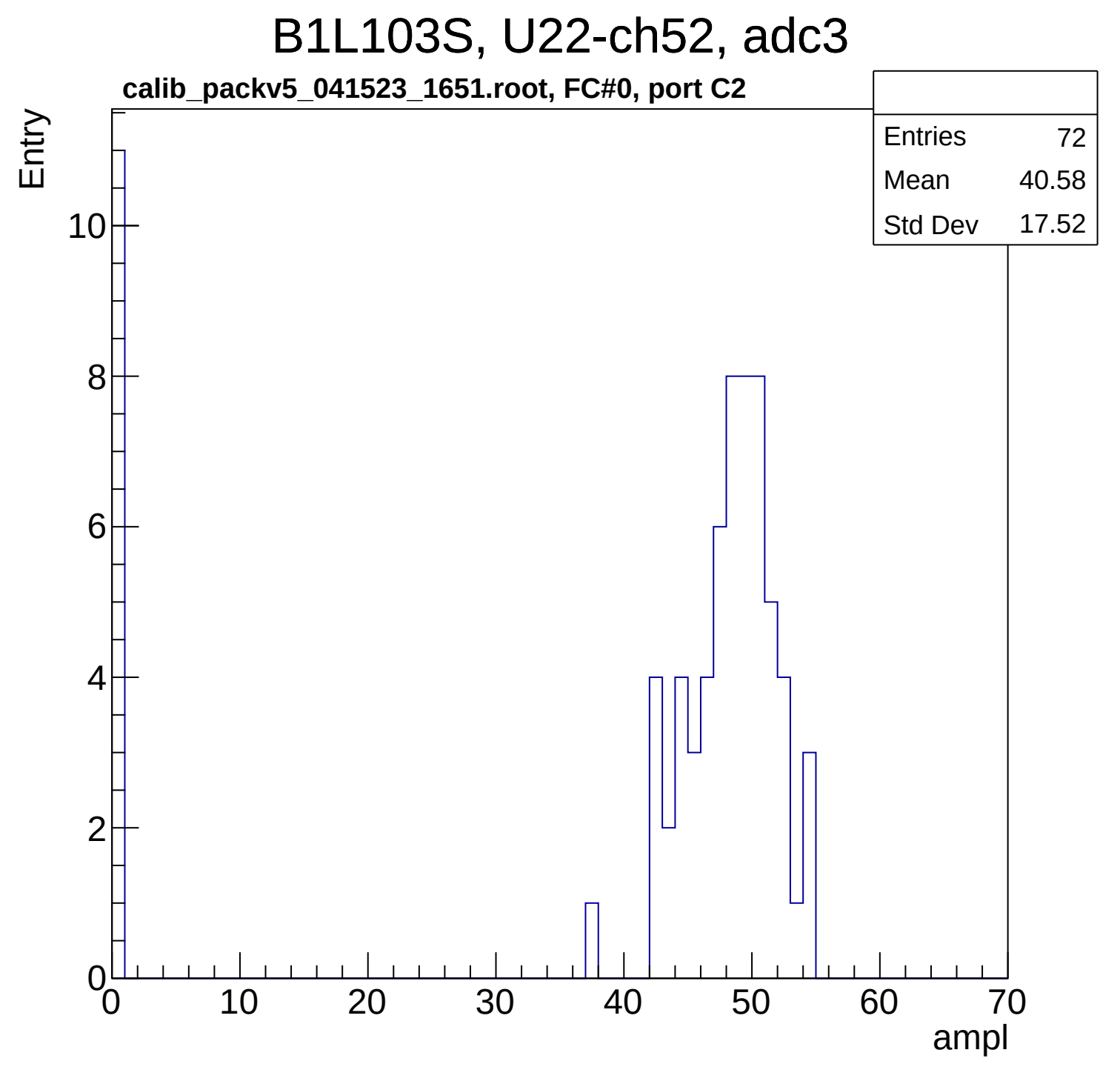
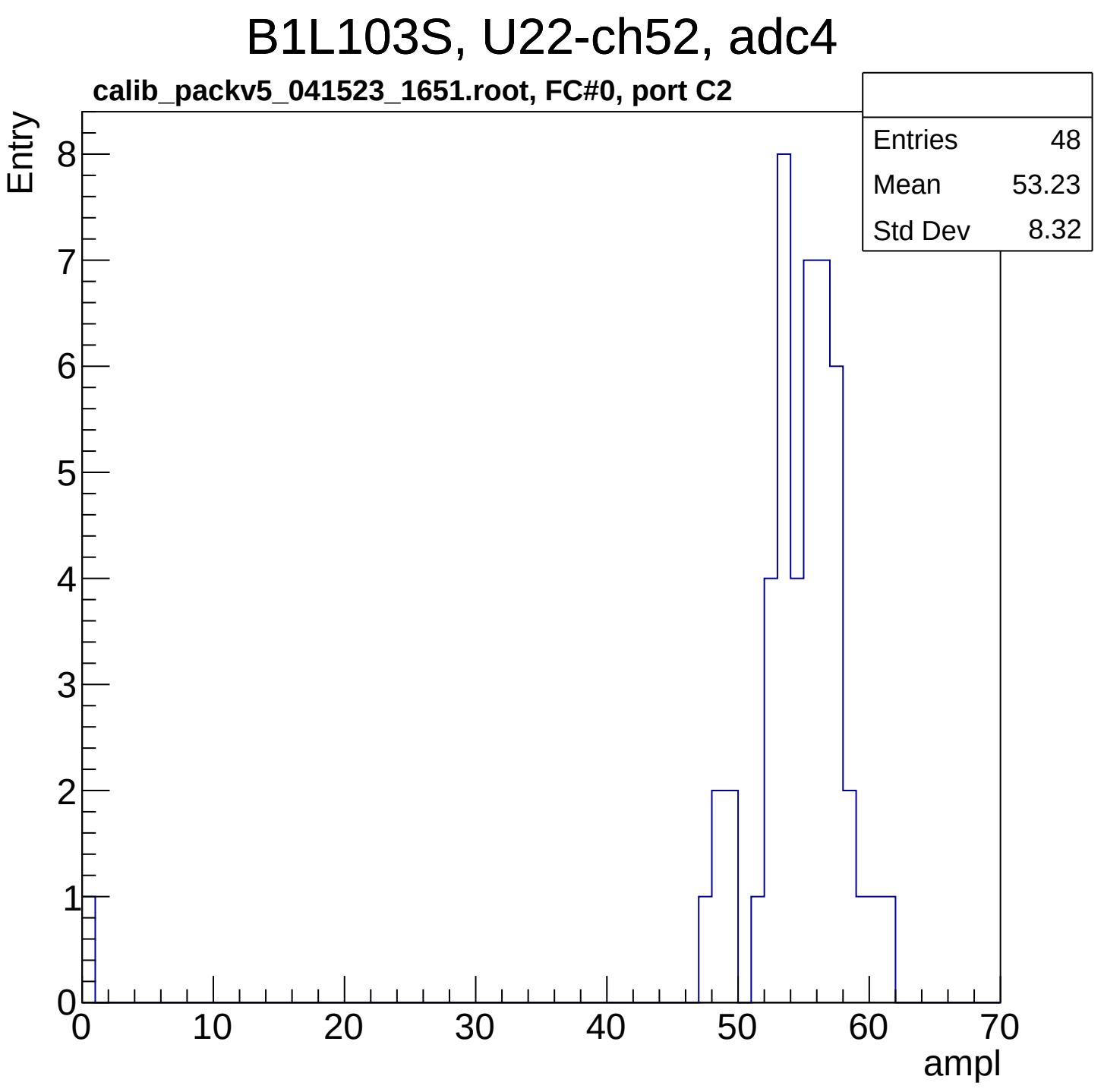
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch52, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 40.58
Std Dev 17.52
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch52, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 53.23
Std Dev 8.32
Entry
ampl
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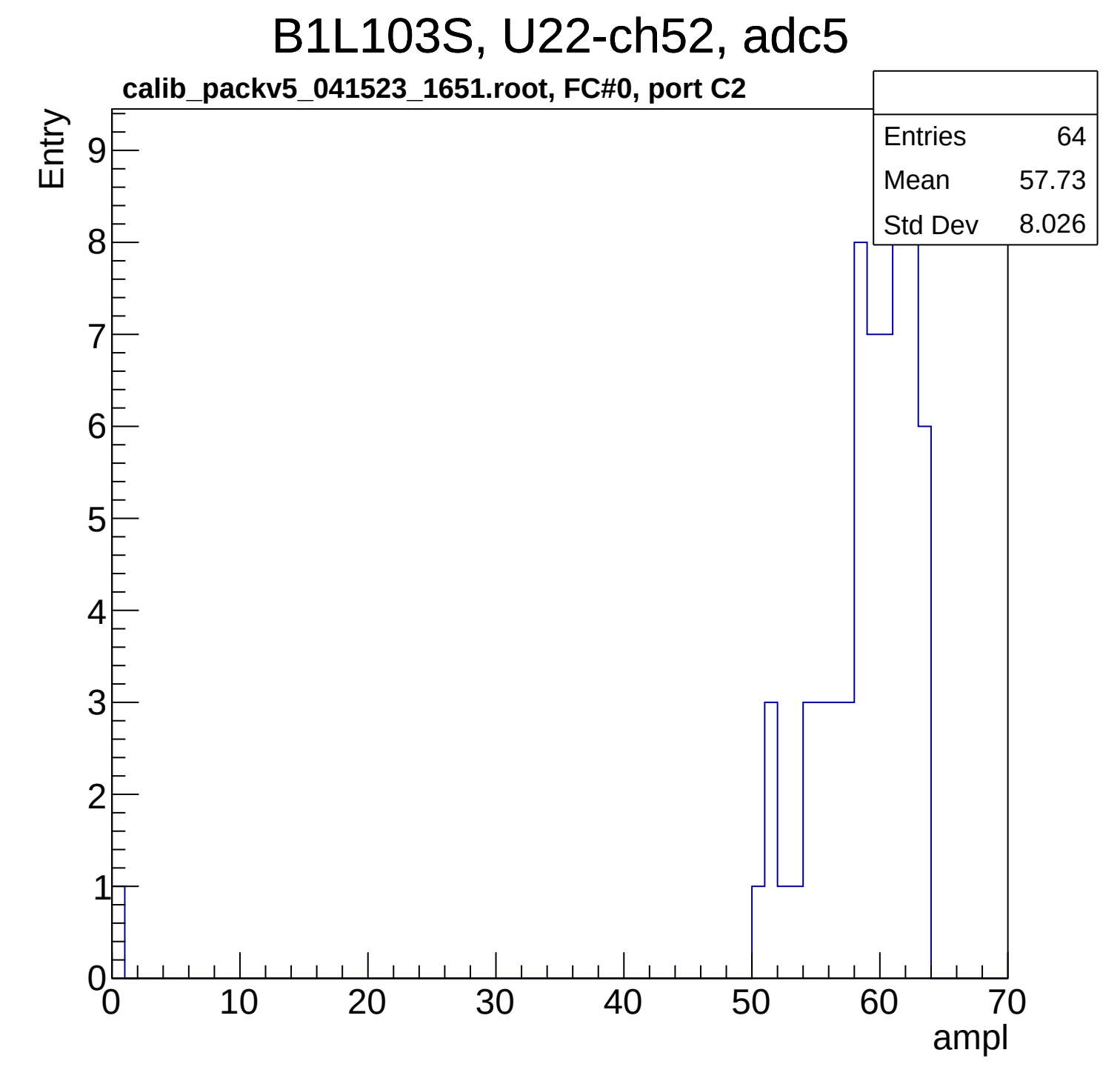
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch52, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 57.73
Std Dev 8.026
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
30
40
50
60
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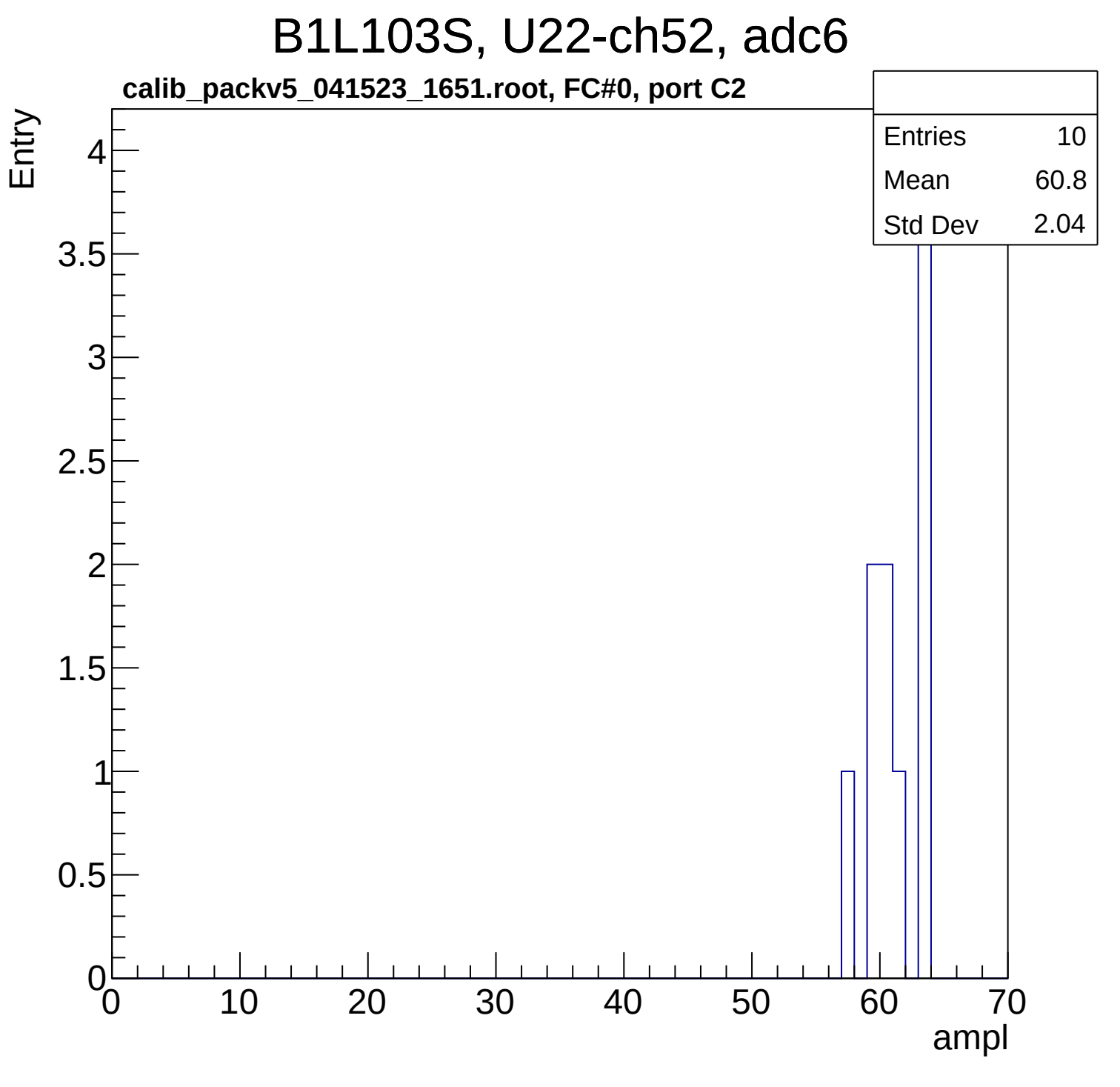
B1L103S, U22-ch52, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 60.8
Std Dev 2.04
Entry
ampl
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0.5
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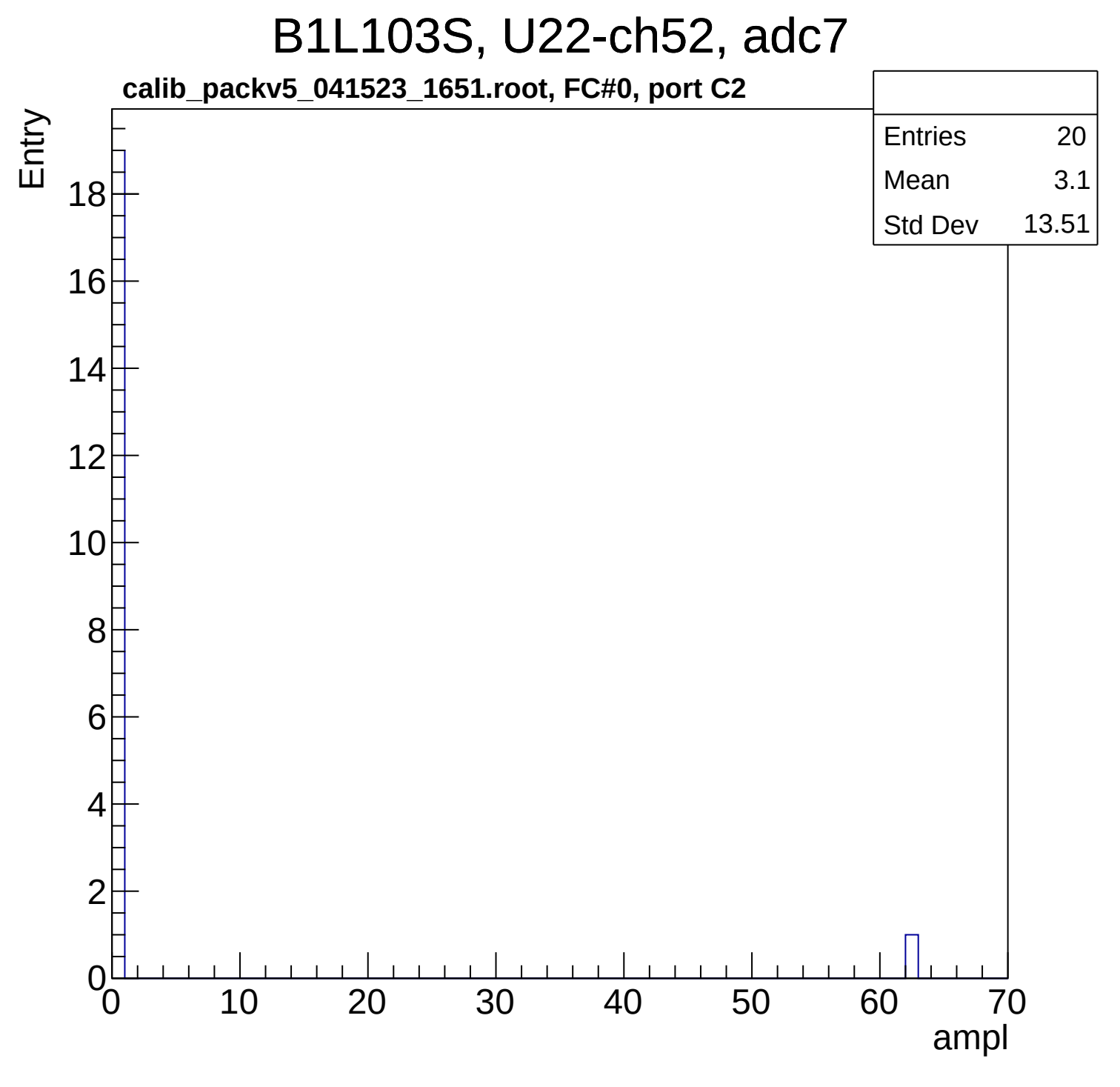
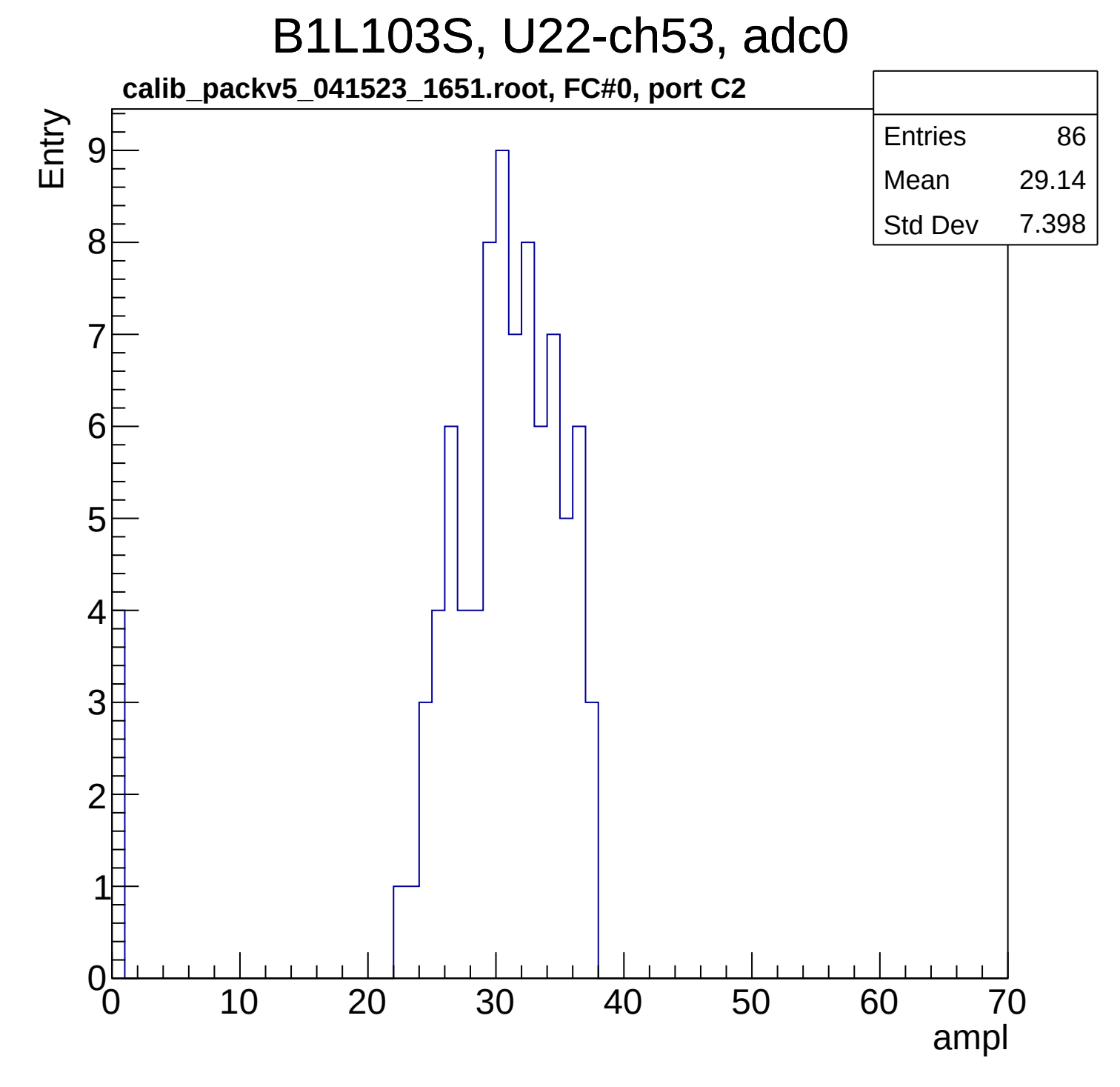
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U22-ch52, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch53, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 29.14
Std Dev 7.398
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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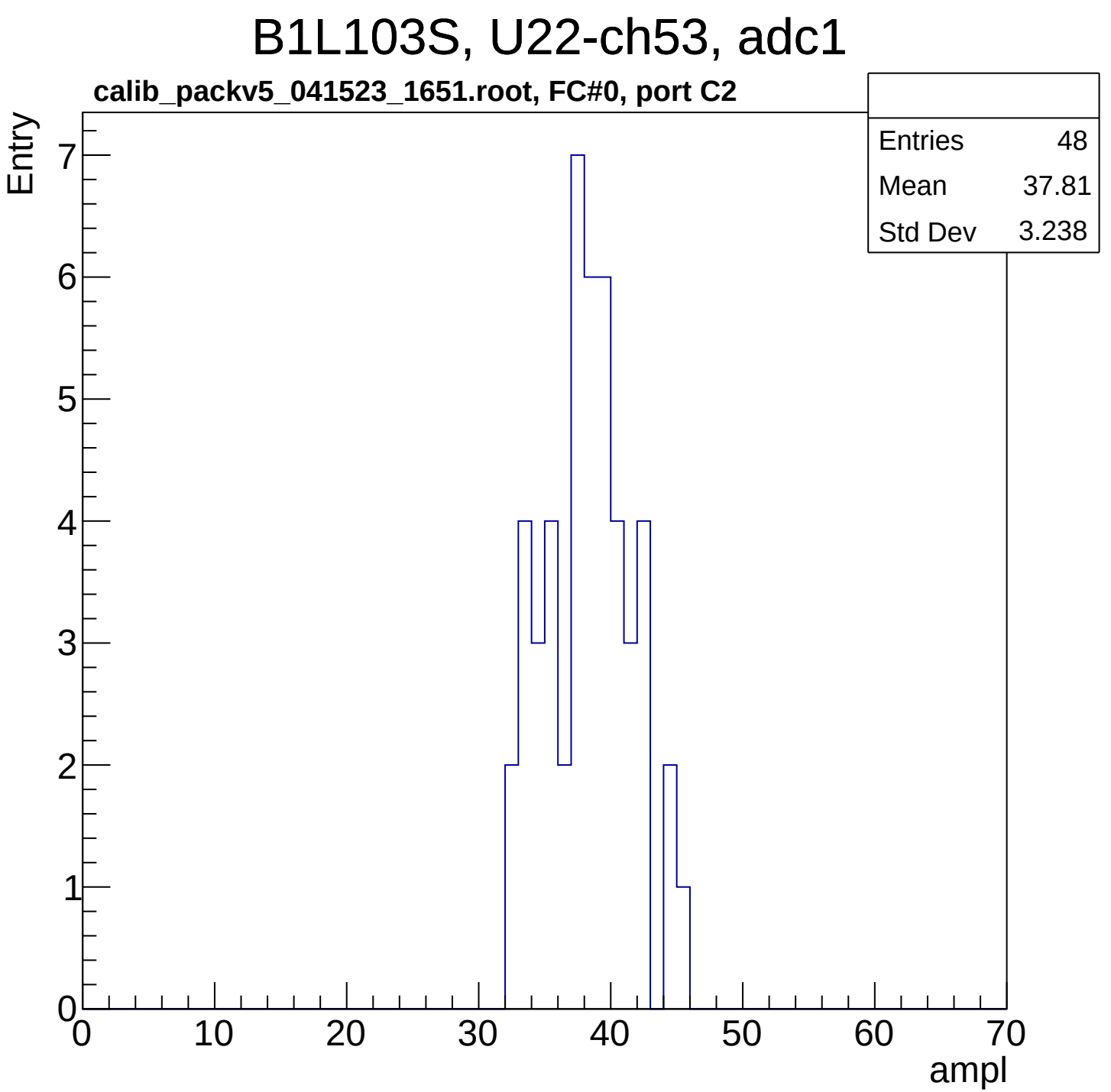
B1L103S, U22-ch53, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 37.81
Std Dev 3.238
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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40
50
60
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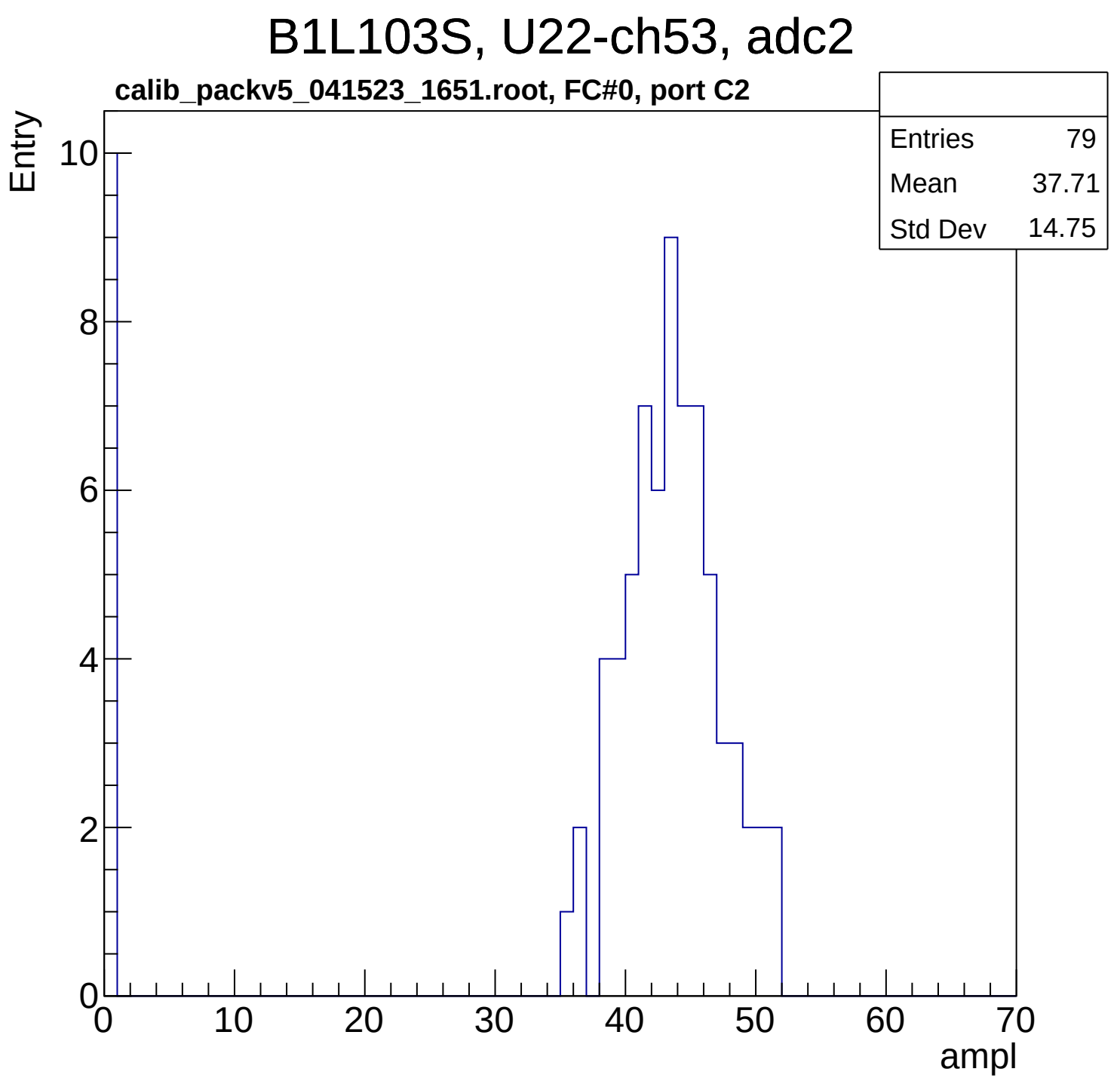
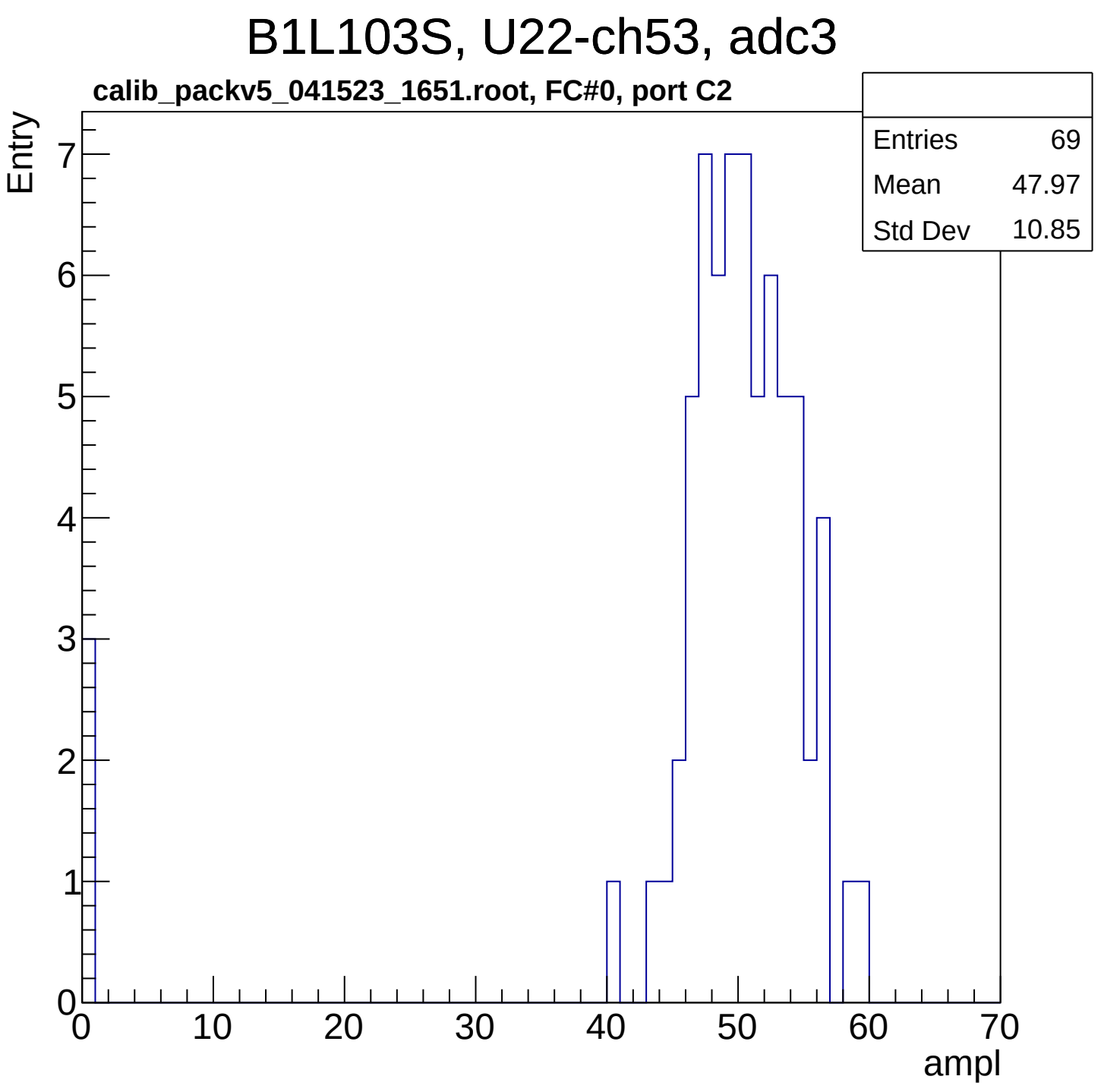
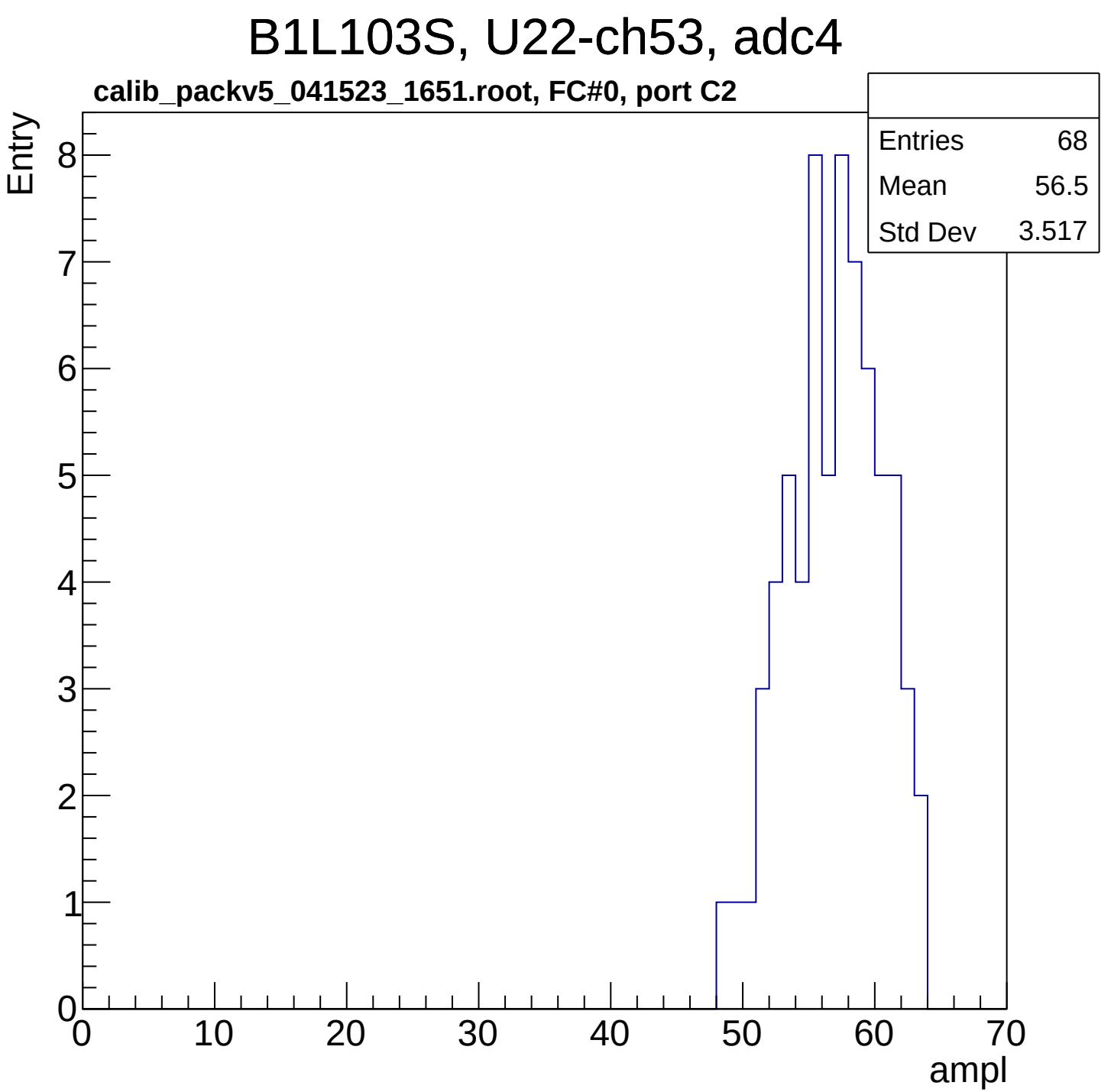

B1L103S, U22-ch53, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 37.71
Std Dev 14.75
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U22-ch53, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 47.97
Std Dev 10.85
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U22-ch53, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 56.5
Std Dev 3.517
Entry
ampl
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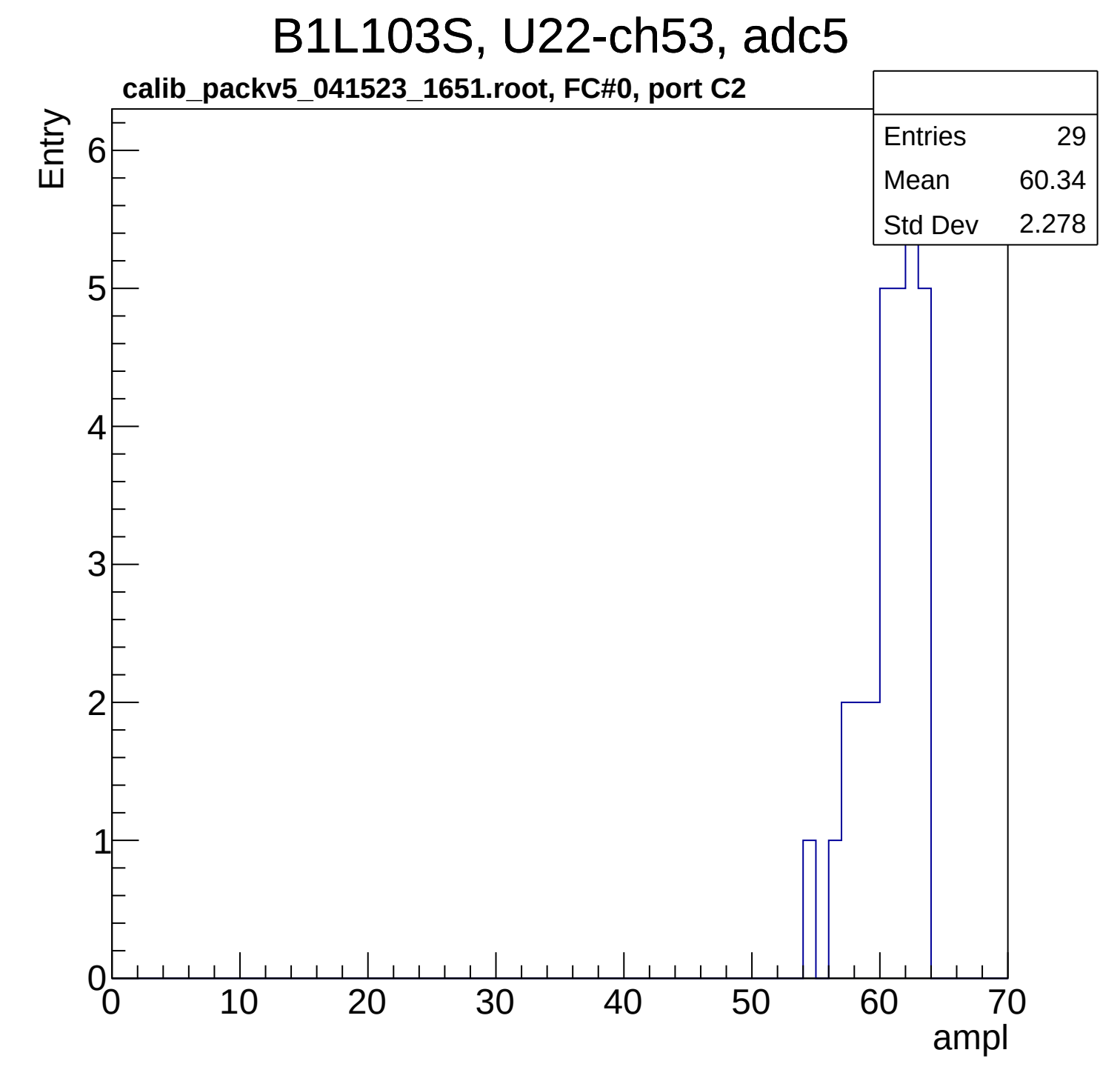
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch53, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 60.34
Std Dev 2.278
Entry
ampl
0
1
2
3
4
5
6
0
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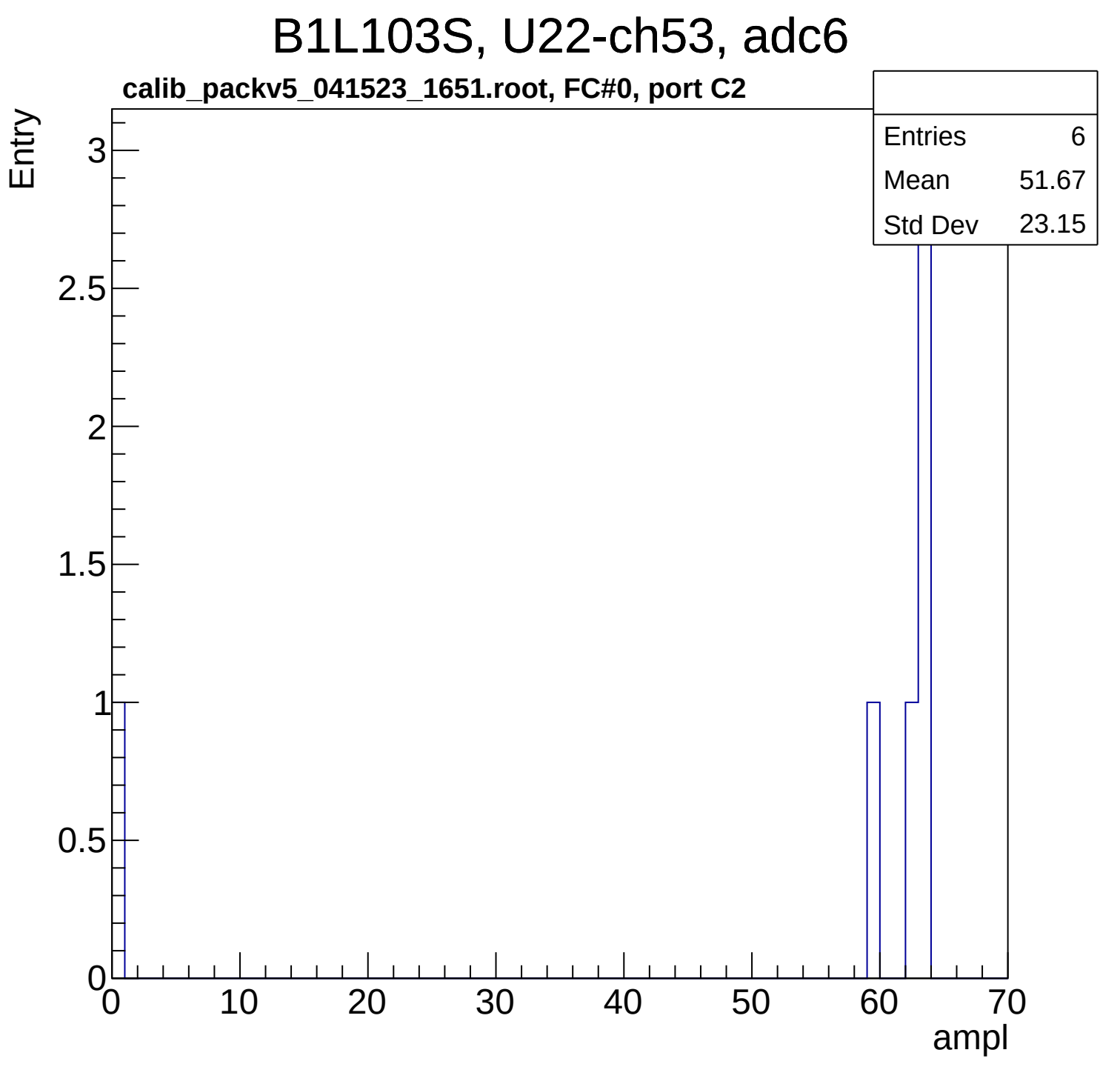
20
30
40
50
60
70


B1L103S, U22-ch53, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 51.67
Std Dev 23.15
Entry
ampl
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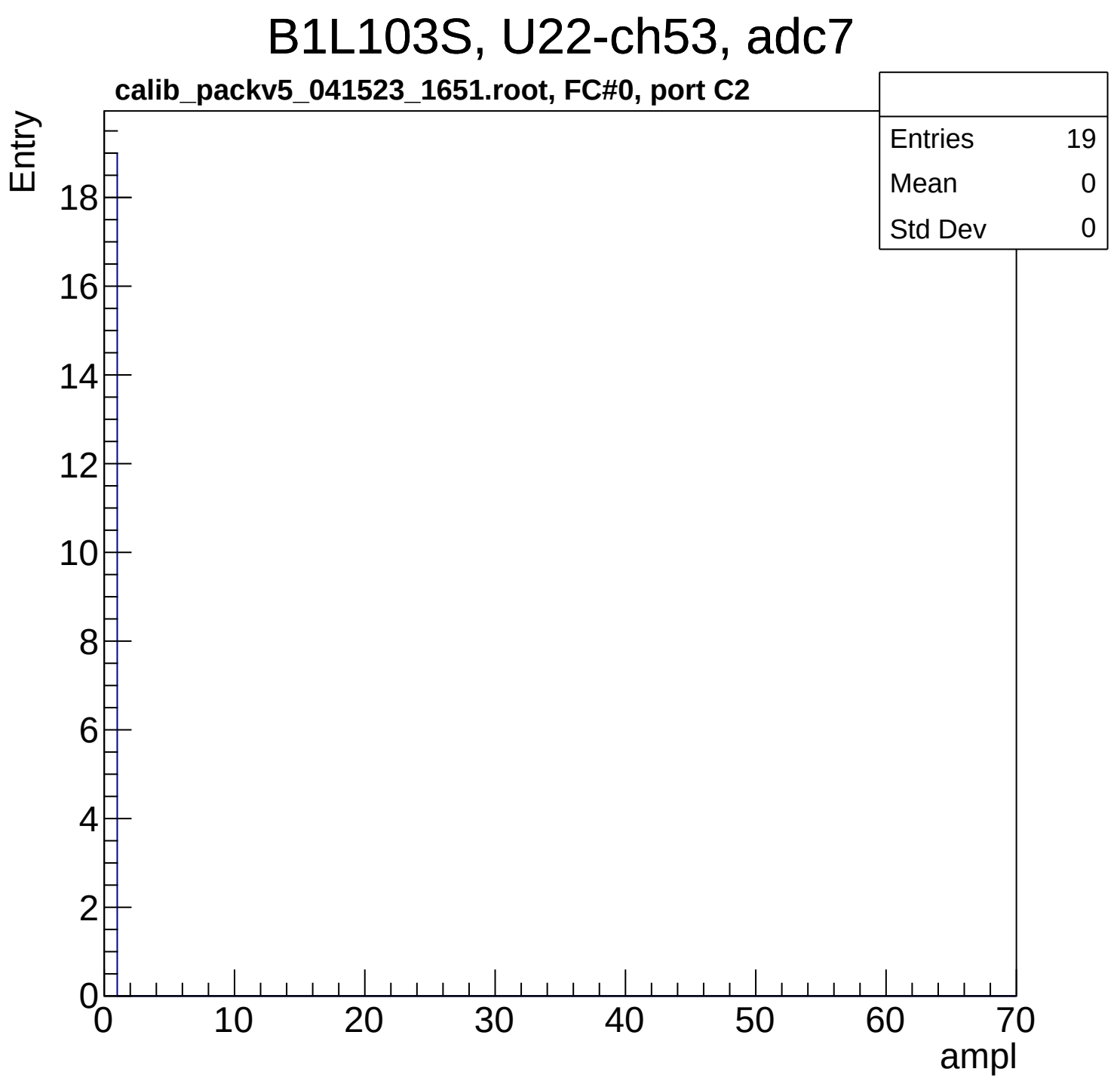
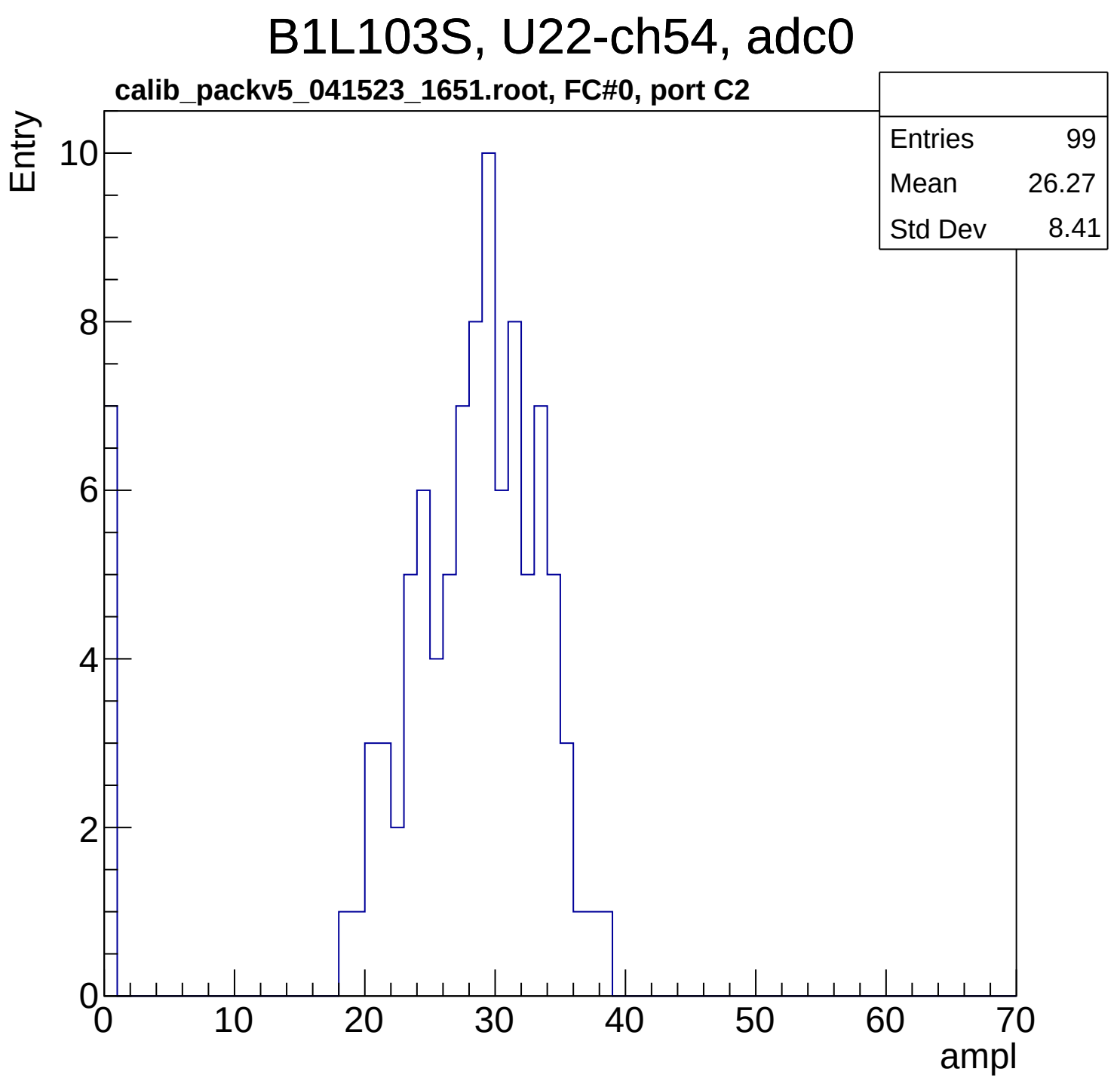
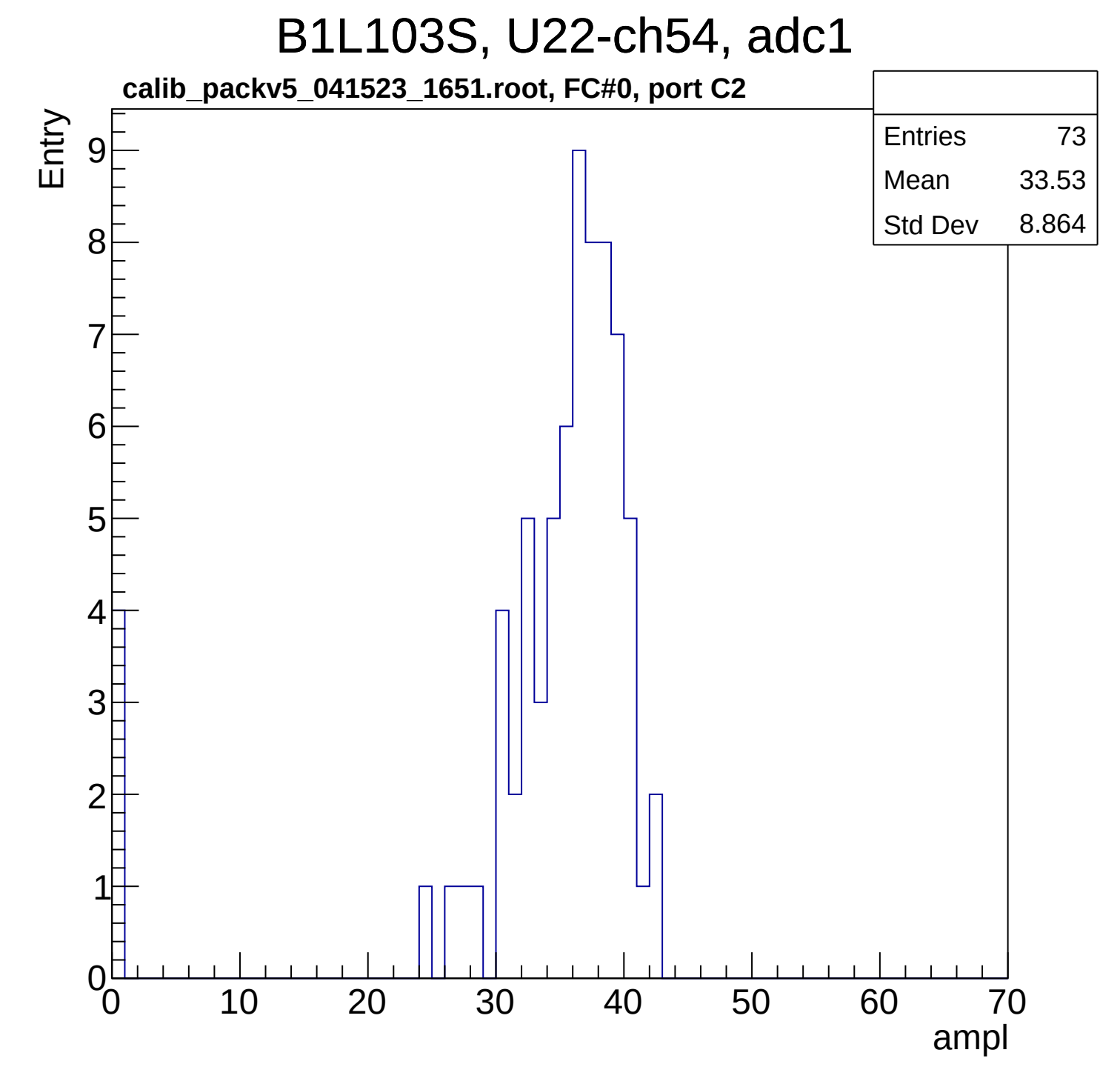
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U22-ch53, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch54, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 26.27
Std Dev 8.41
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch54, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 33.53
Std Dev 8.864
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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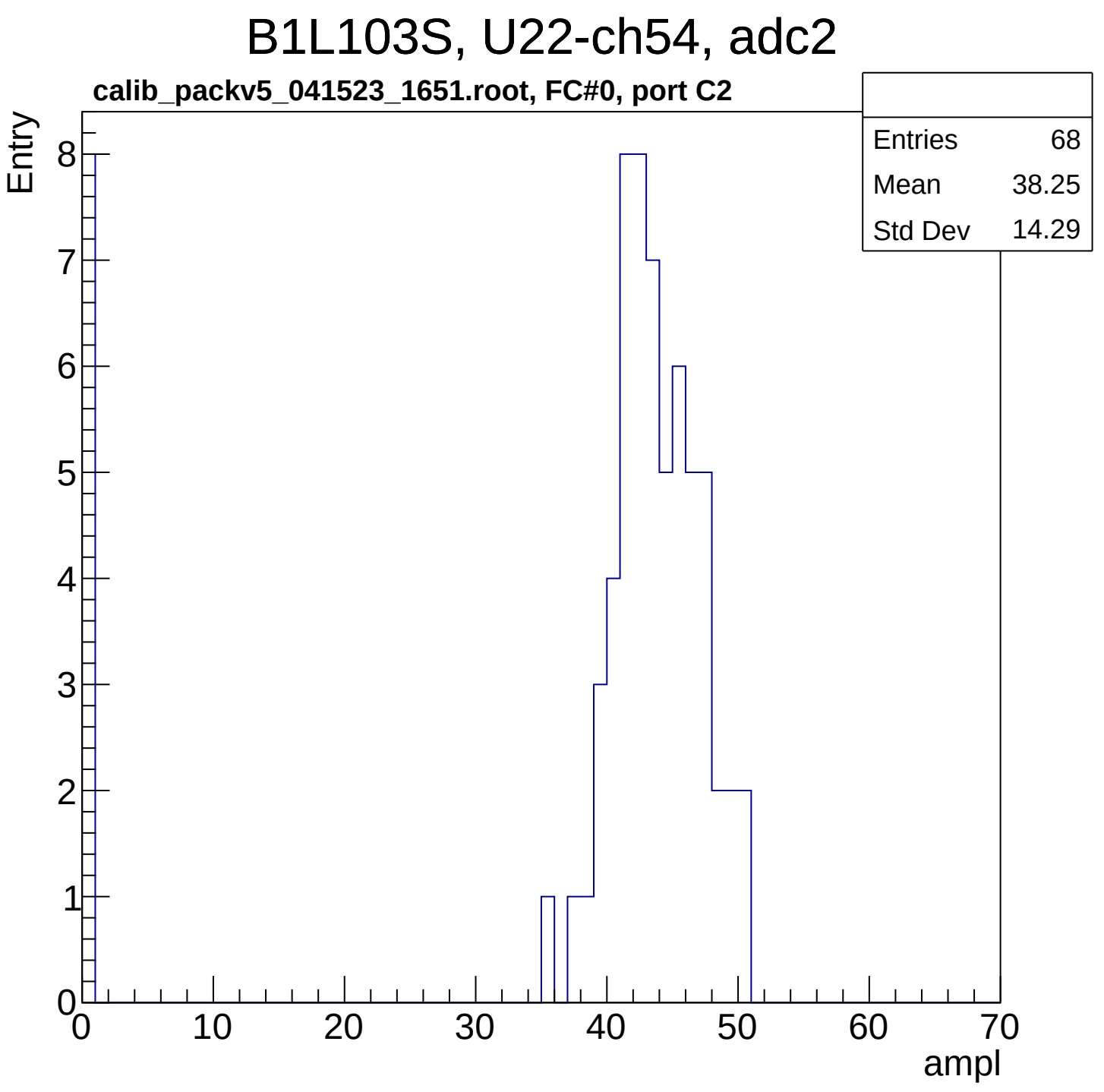
40
50
60
70


B1L103S, U22-ch54, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 38.25
Std Dev 14.29
Entry
ampl
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2
3
4
5
6
7
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0
10
20
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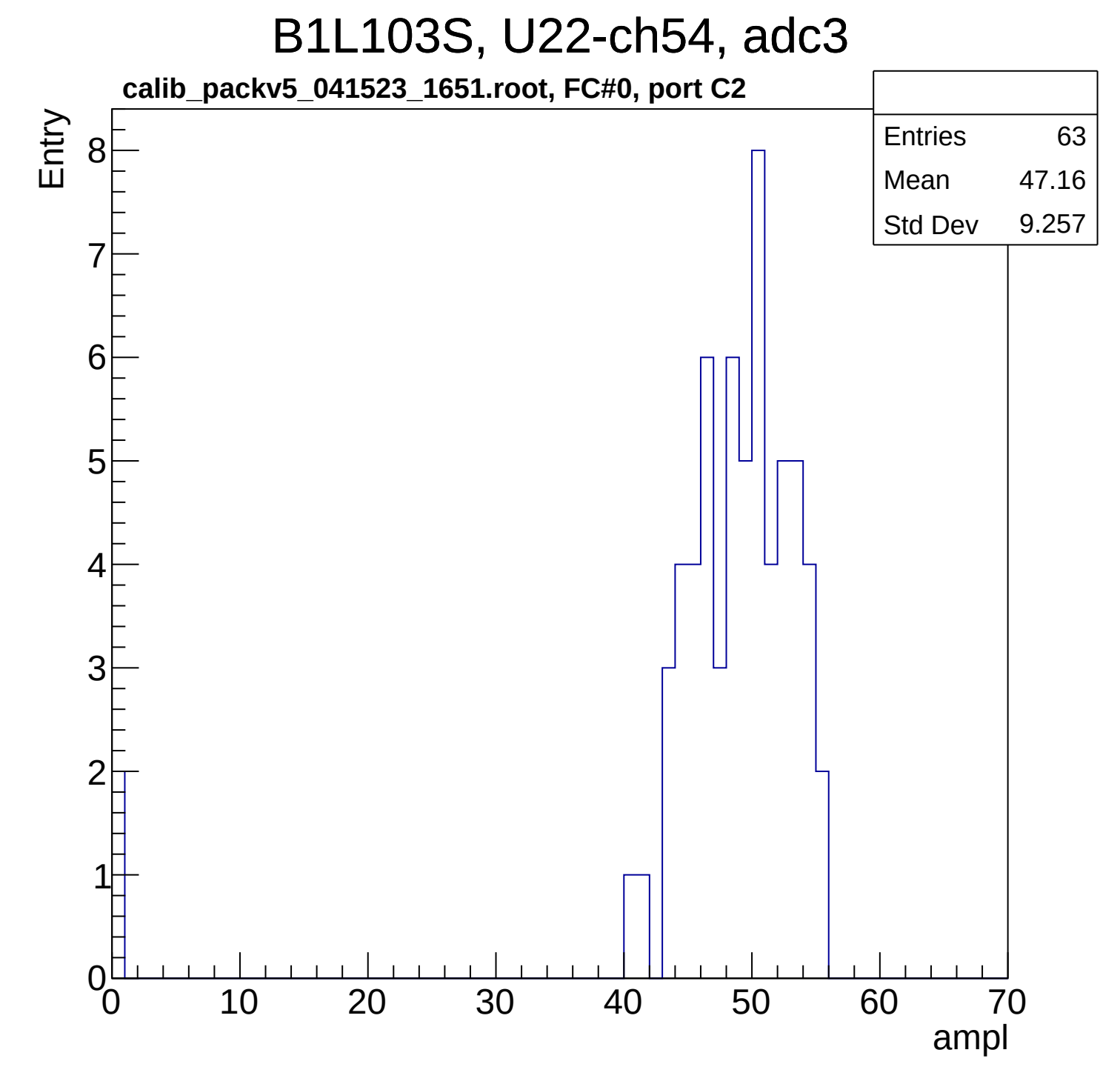
40
50
60
70


B1L103S, U22-ch54, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 47.16
Std Dev 9.257
Entry
ampl
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1
2
3
4
5
6
7
8
0
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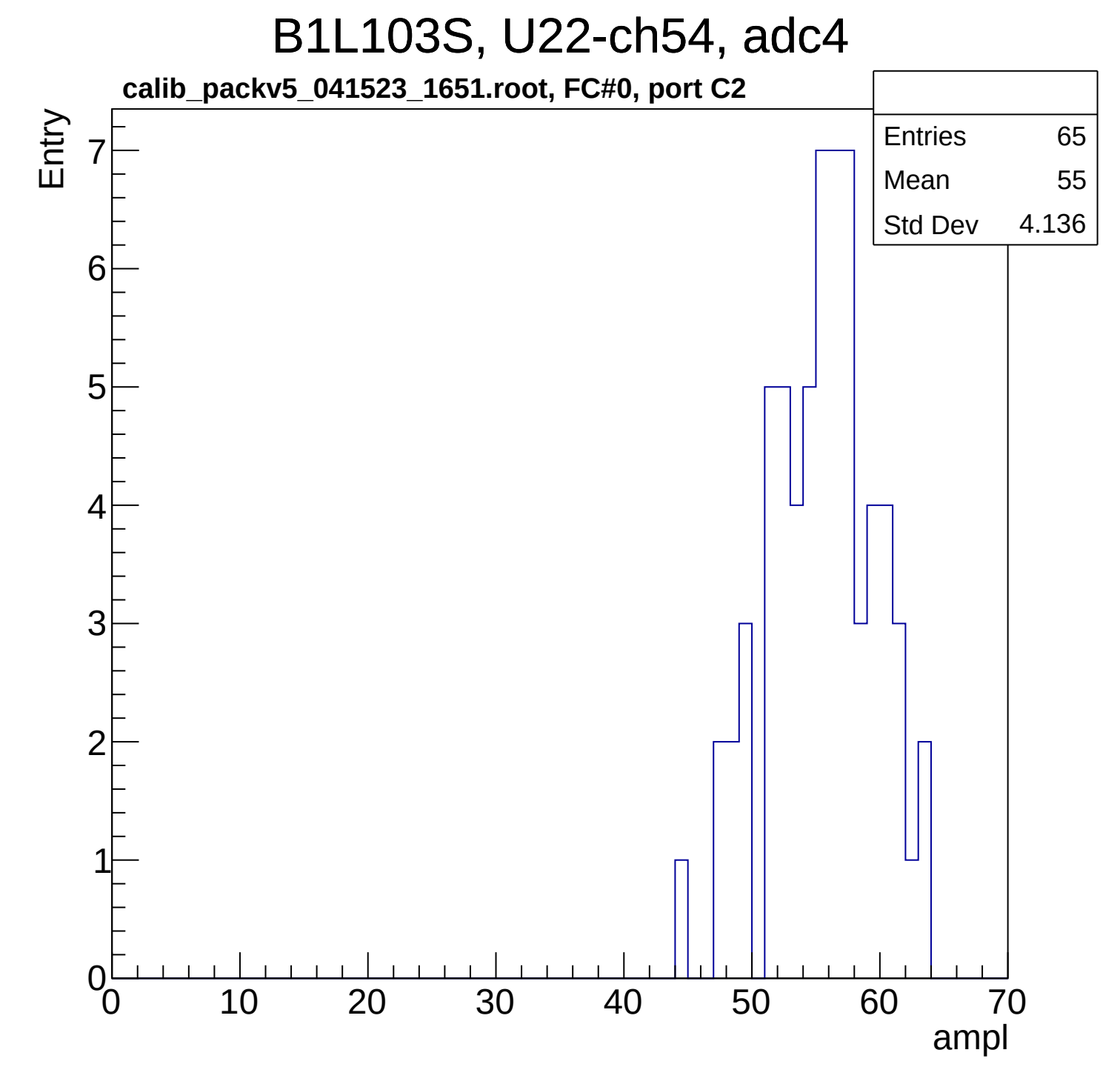
20
30
40
50
60
70


B1L103S, U22-ch54, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 55
Std Dev 4.136
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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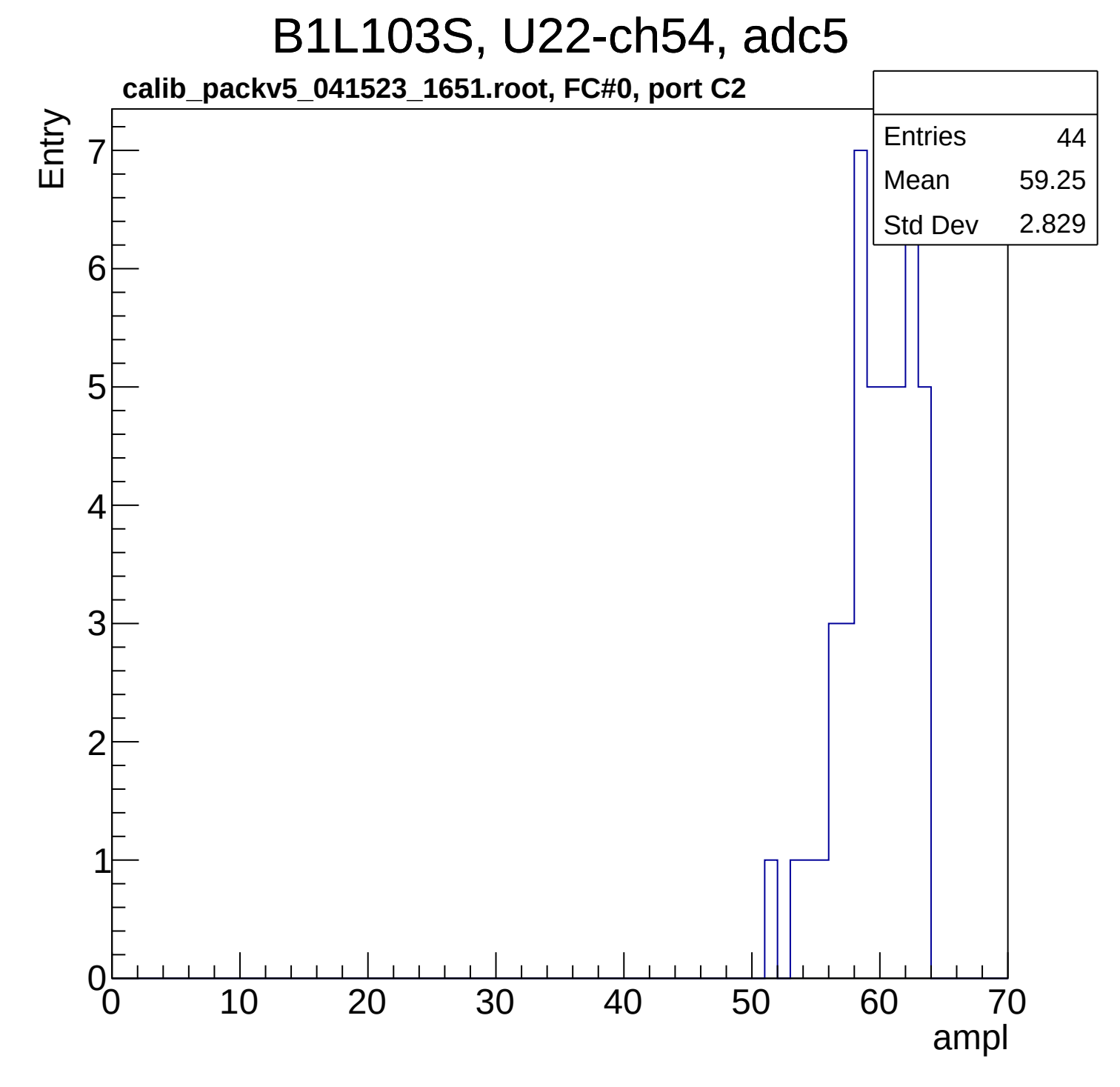
40
50
60
70


B1L103S, U22-ch54, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 59.25
Std Dev 2.829
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
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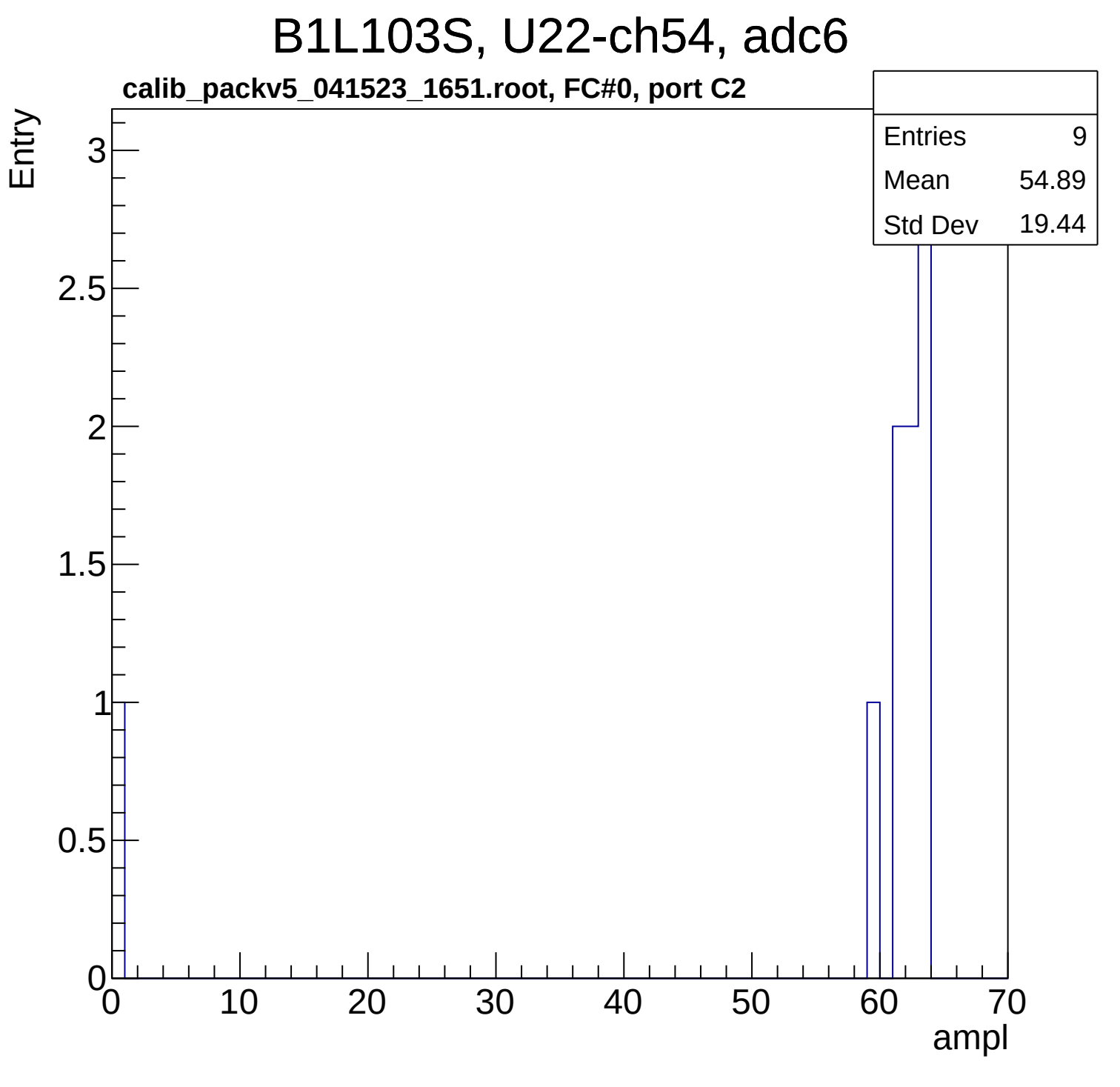
60
70


B1L103S, U22-ch54, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 54.89
Std Dev 19.44
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
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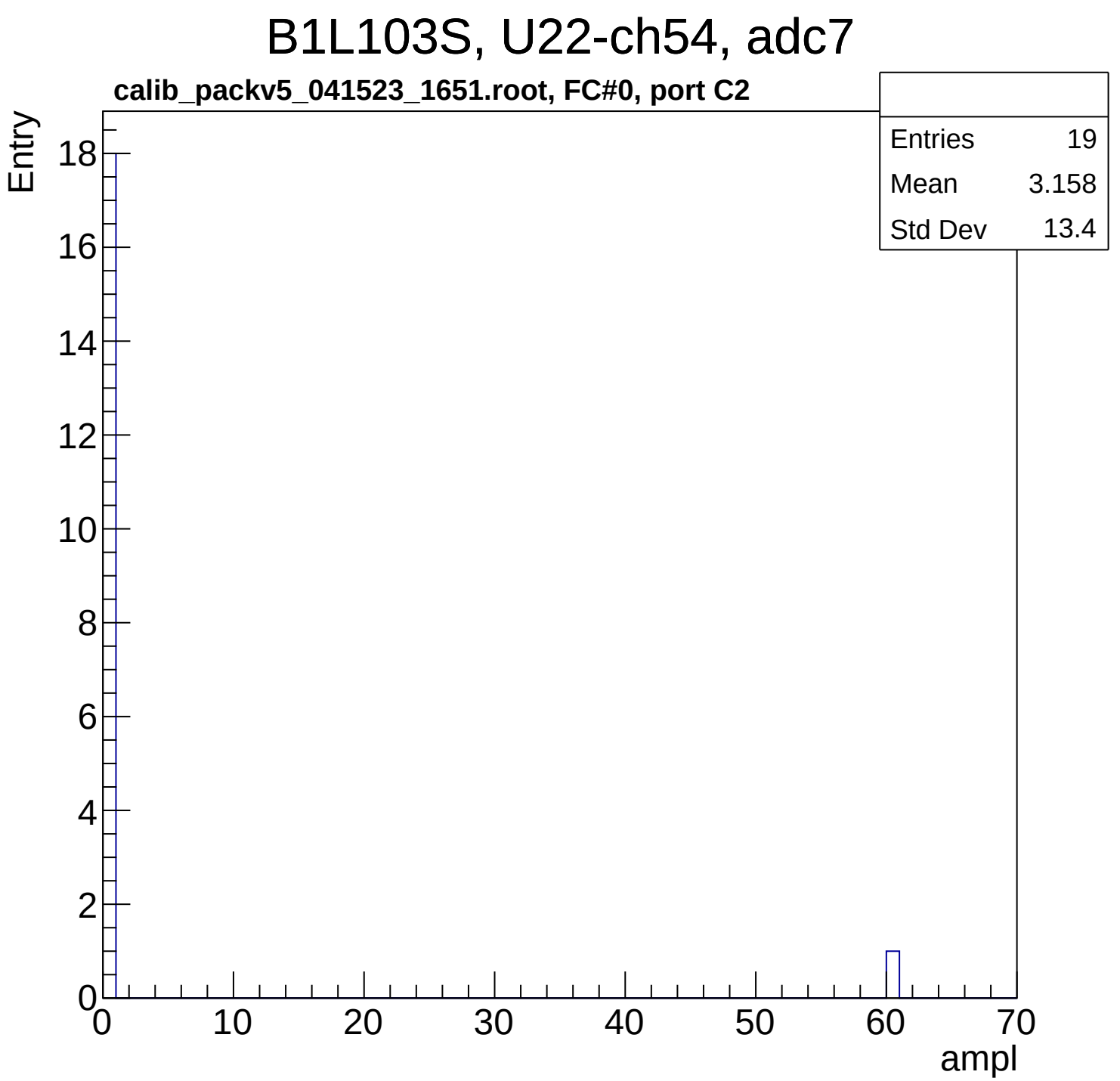
50
60
70


B1L103S, U22-ch54, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.158
Std Dev 13.4
Entry
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2
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6
8
10
12
14
16
18
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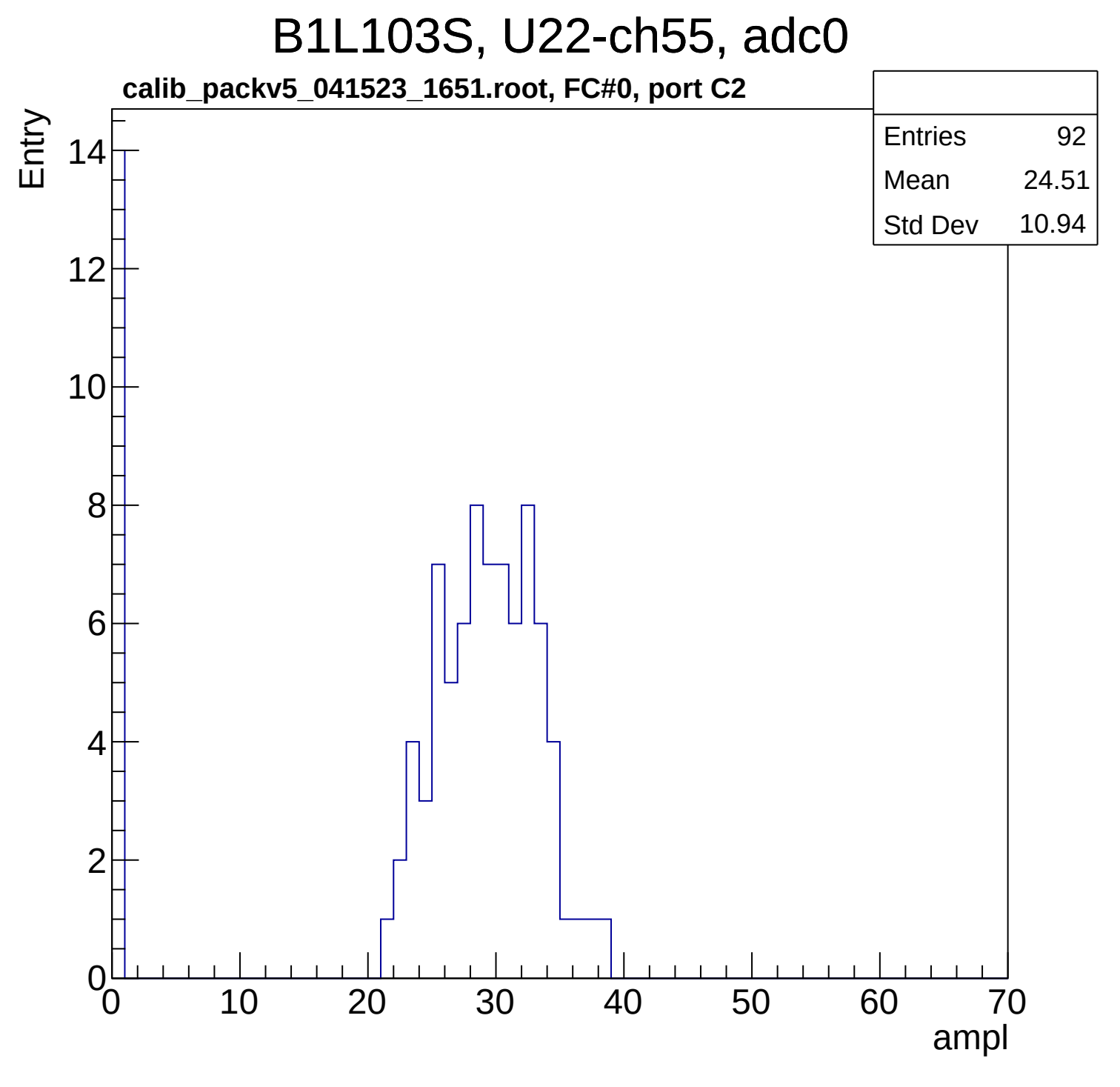
50
60
70
ampl


B1L103S, U22-ch55, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 24.51
Std Dev 10.94
Entry
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2
4
6
8
10
12
14
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10
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30
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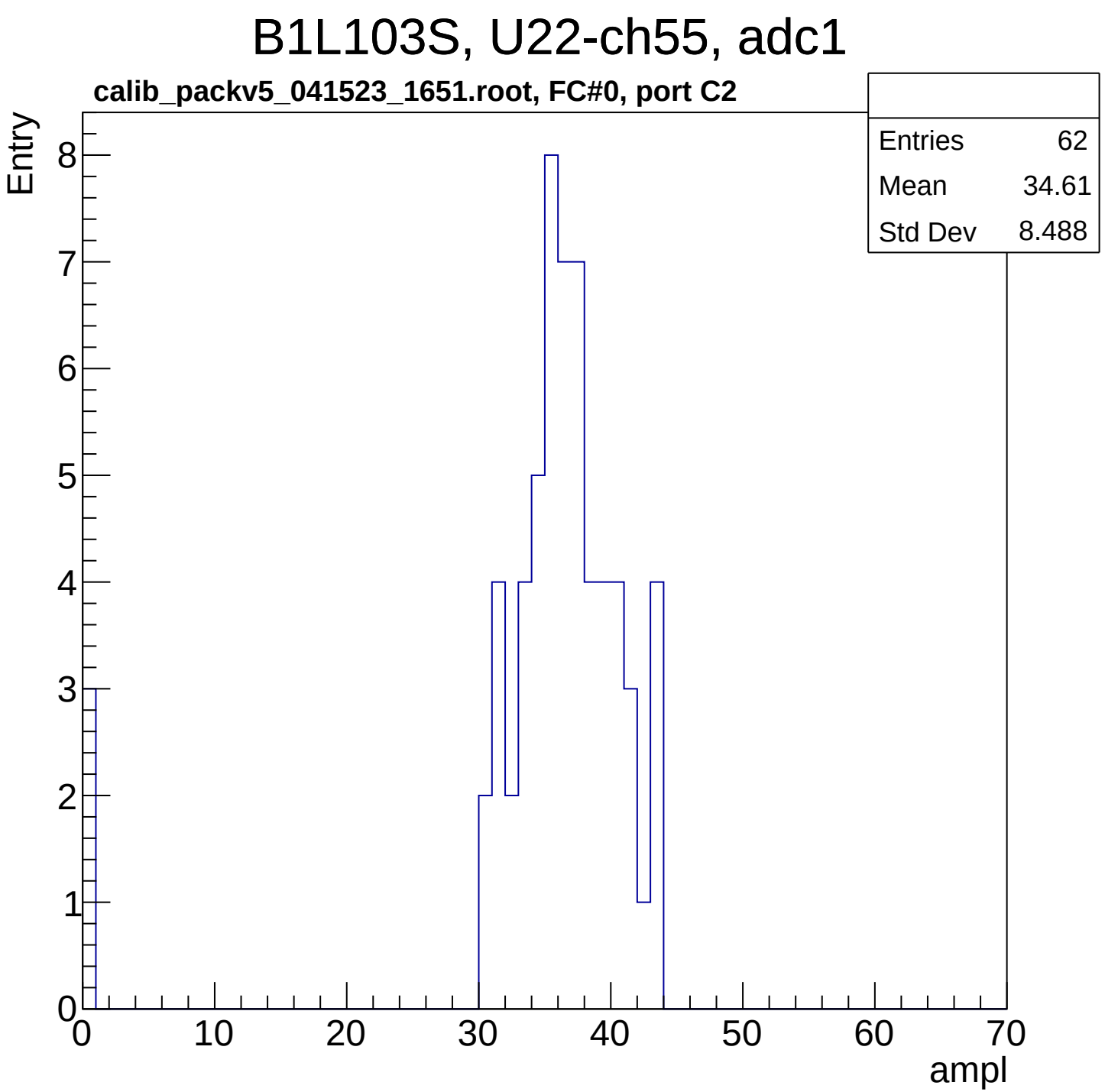
50
60
70
ampl


B1L103S, U22-ch55, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 34.61
Std Dev 8.488
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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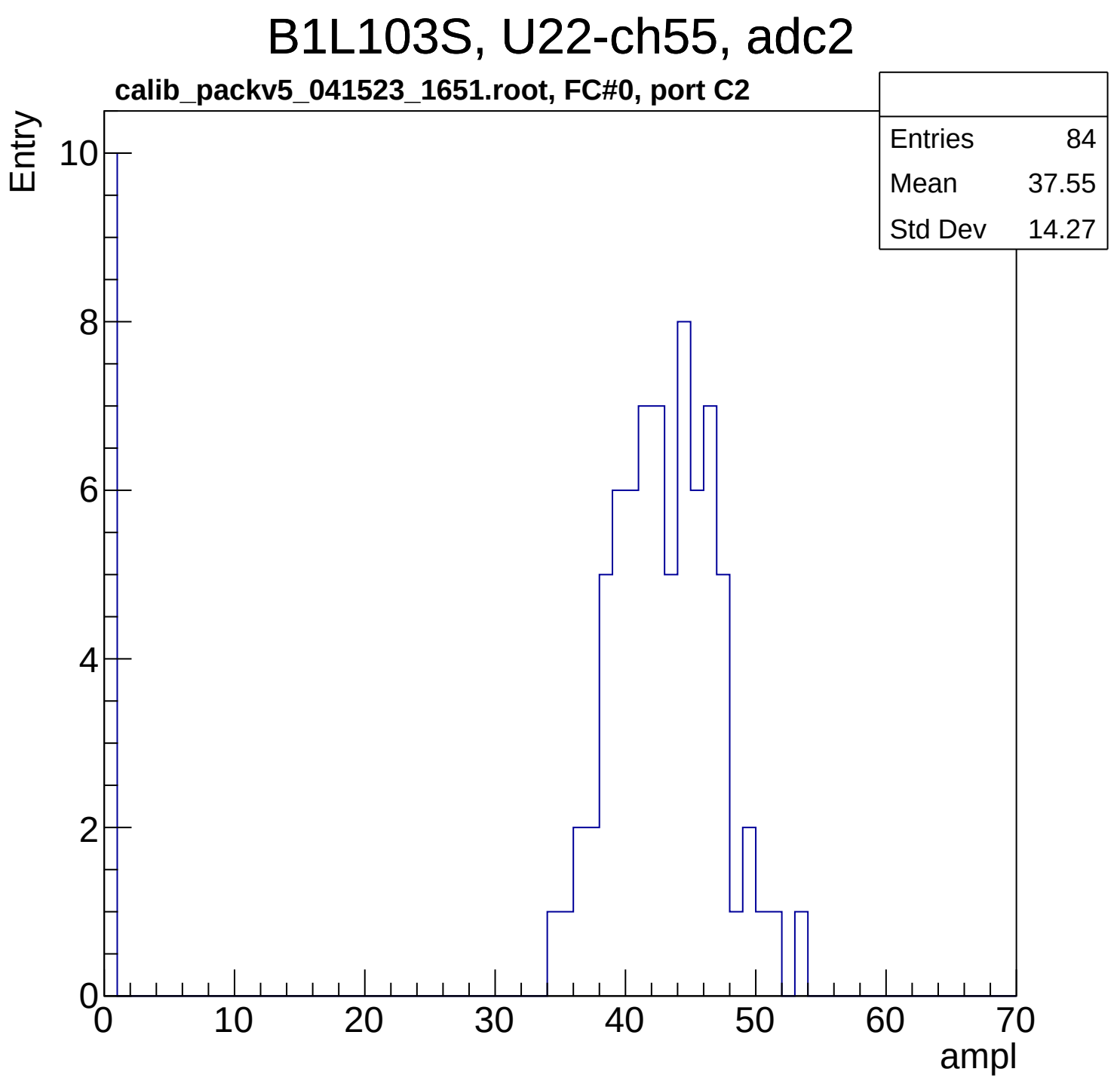
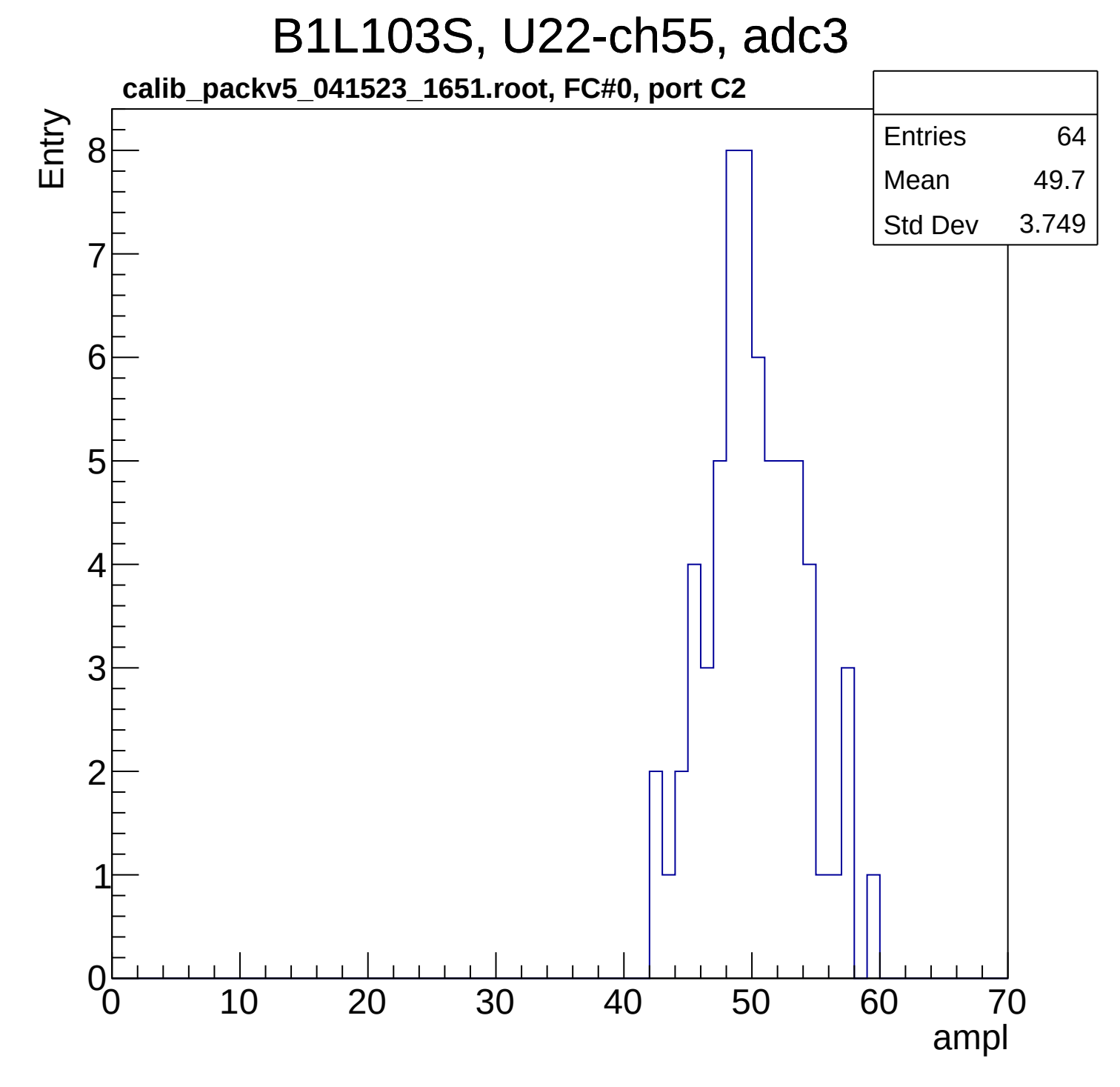
40
50
60
70


B1L103S, U22-ch55, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 37.55
Std Dev 14.27
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch55, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 49.7
Std Dev 3.749
Entry
ampl
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2
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4
5
6
7
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0
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40
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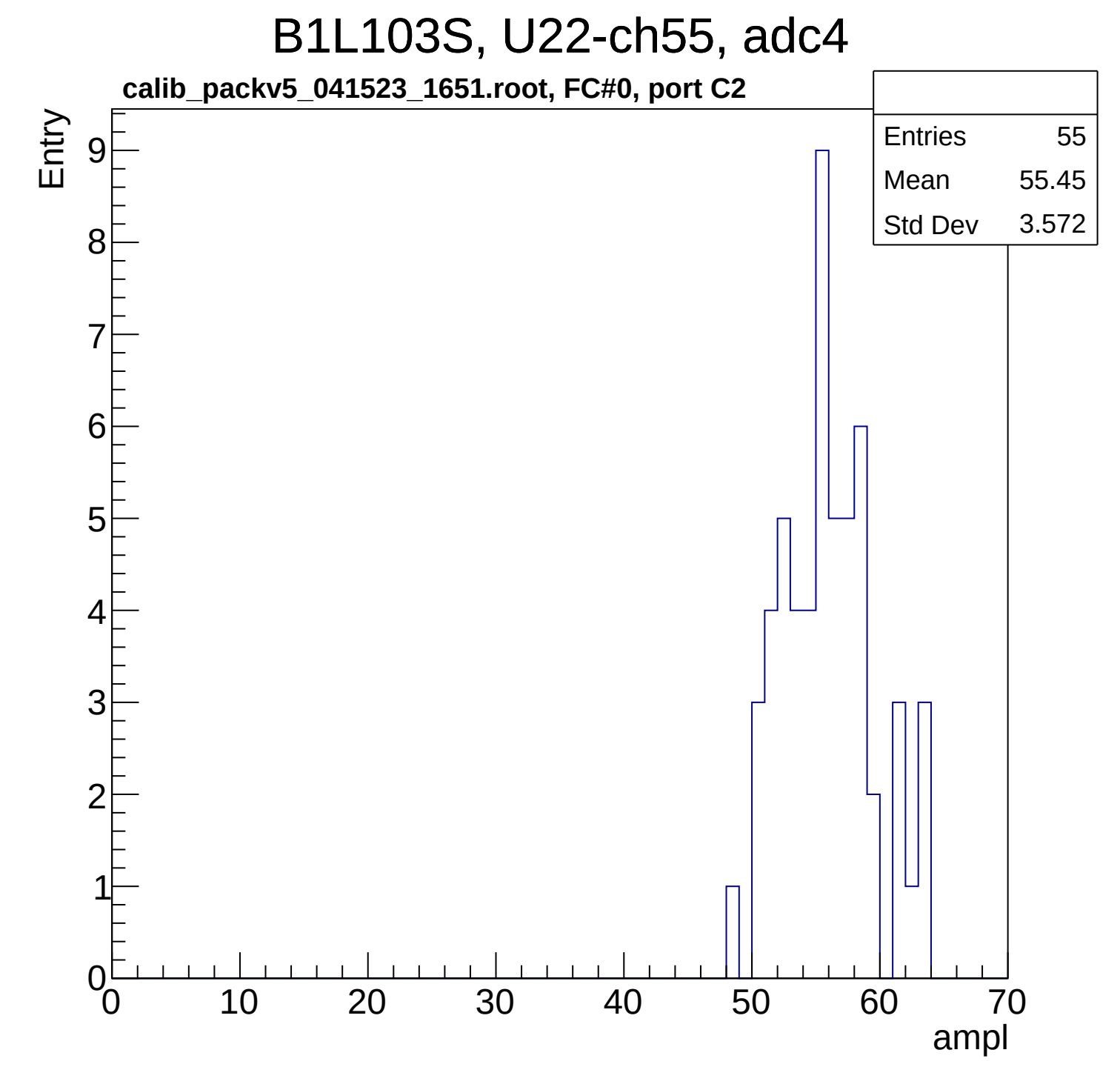
B1L103S, U22-ch55, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 55.45
Std Dev 3.572
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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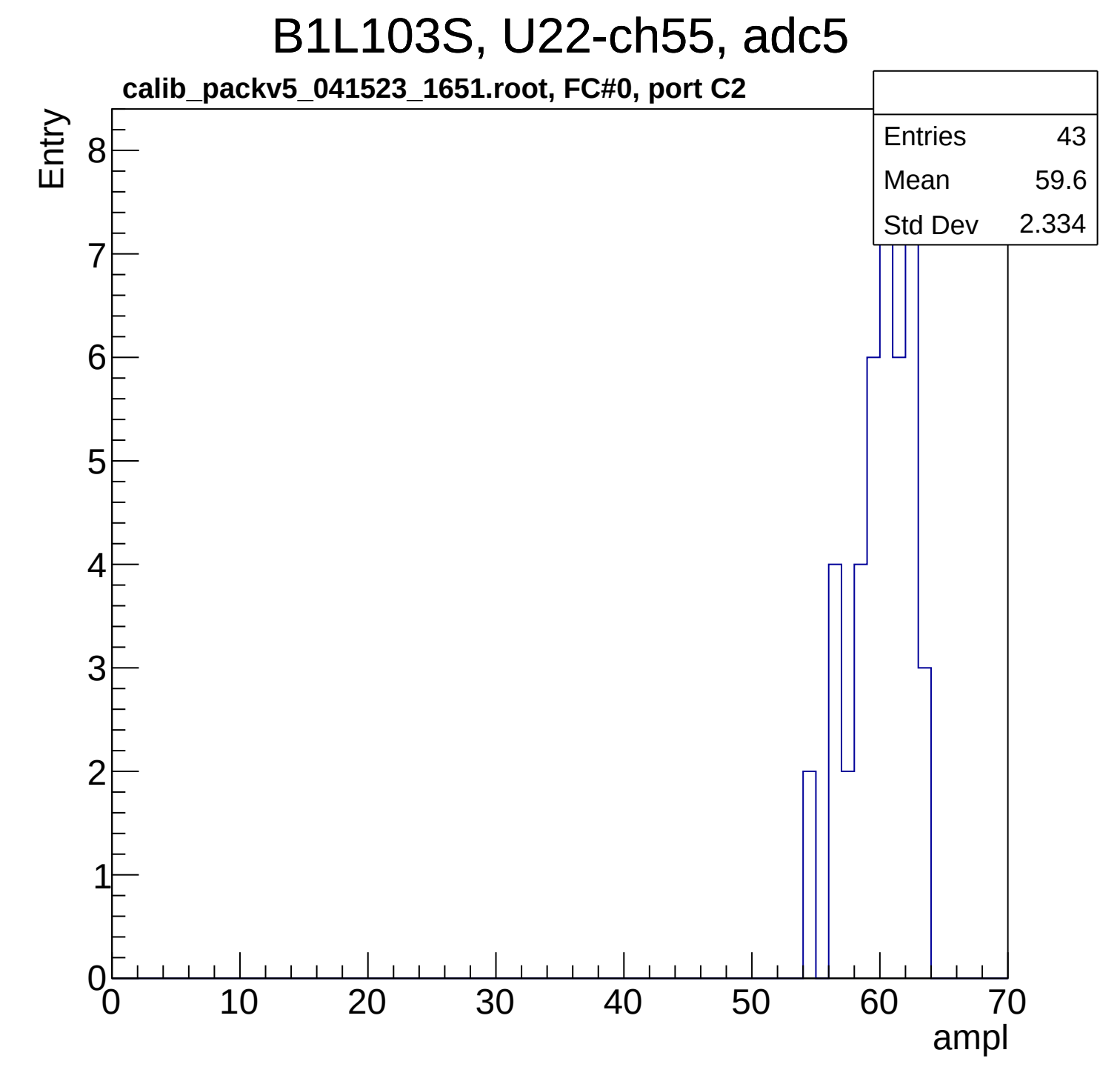
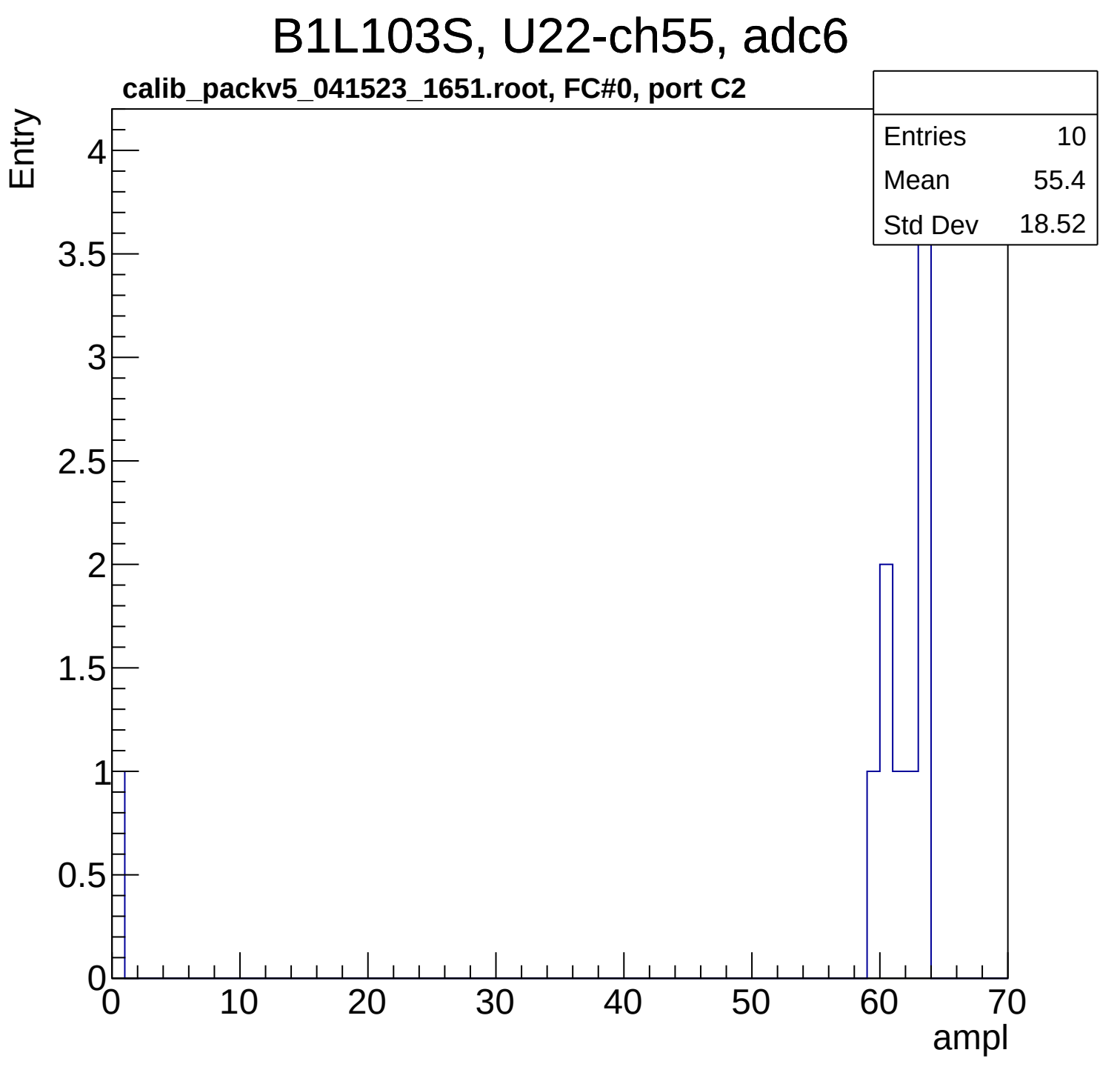
60
70


B1L103S, U22-ch55, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 59.6
Std Dev 2.334
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch55, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 55.4
Std Dev 18.52
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
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60
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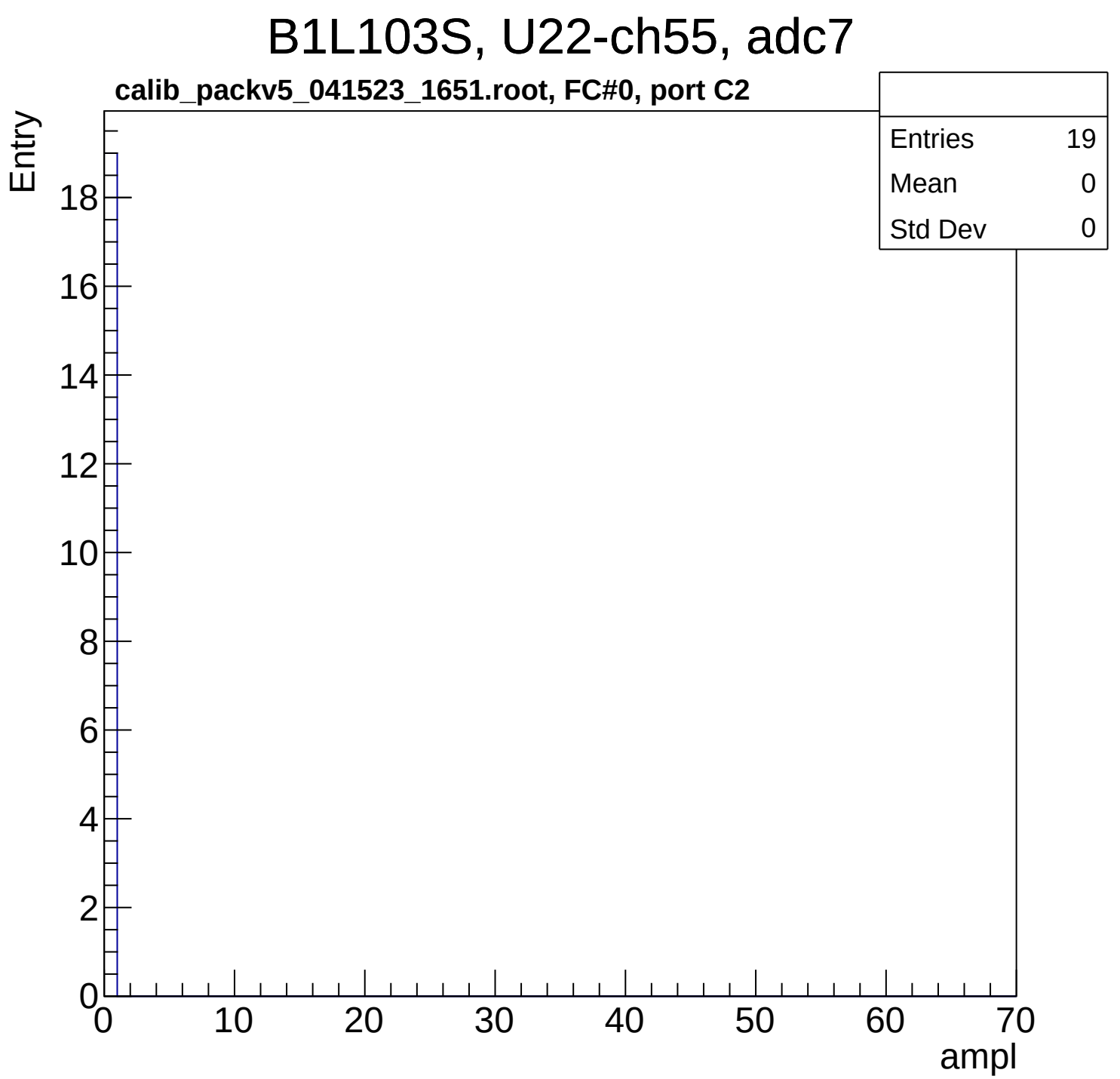
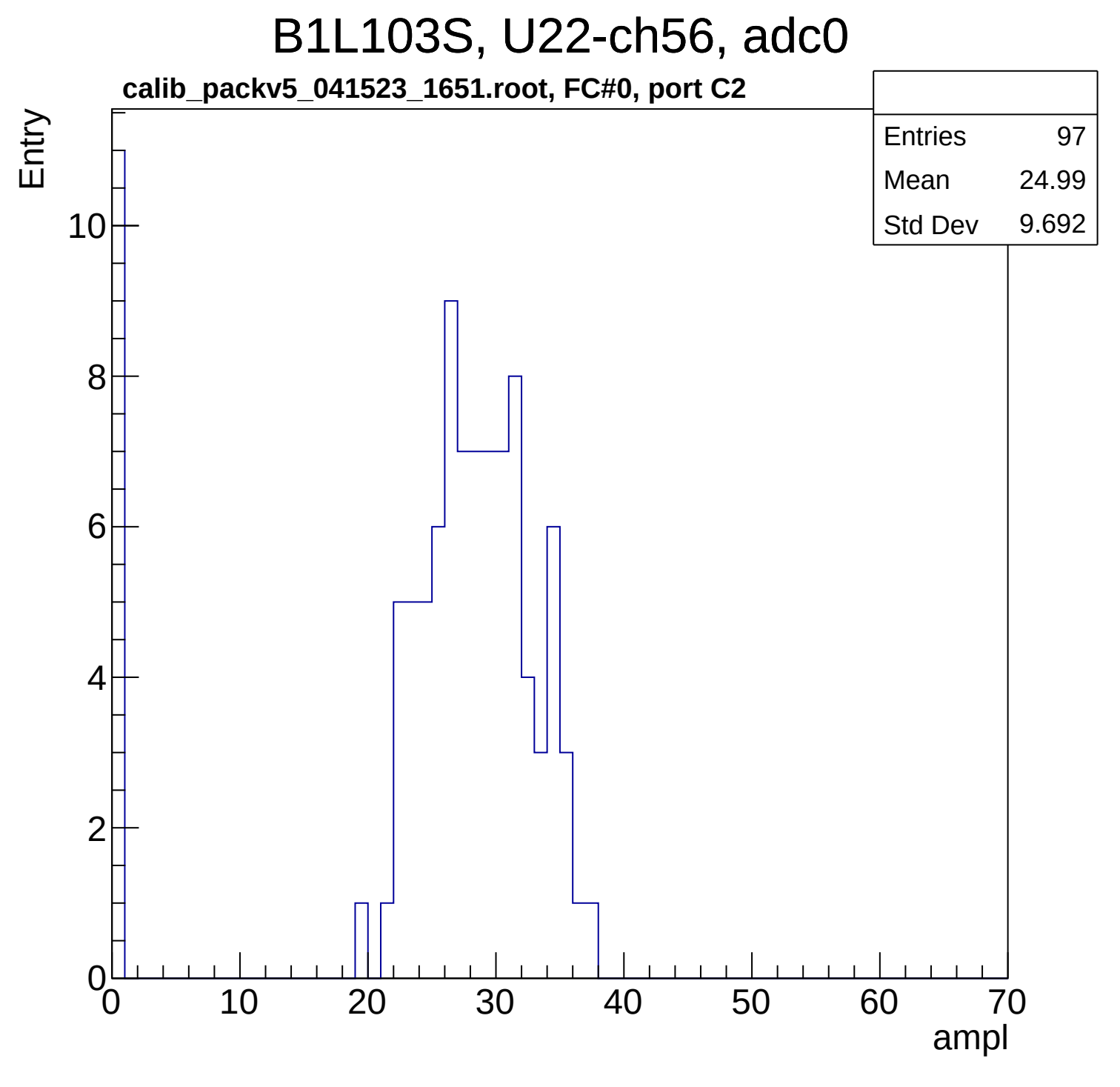
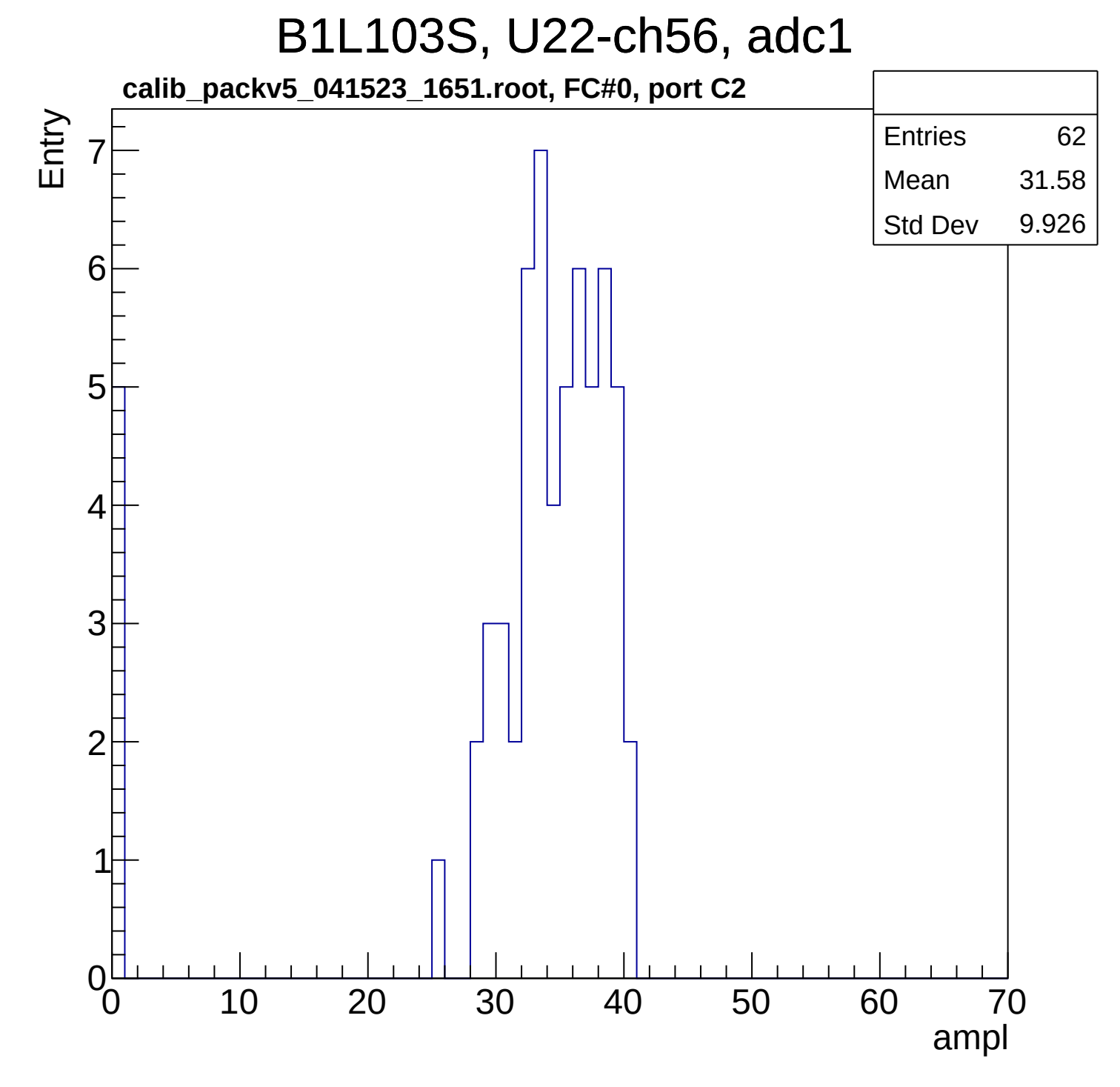
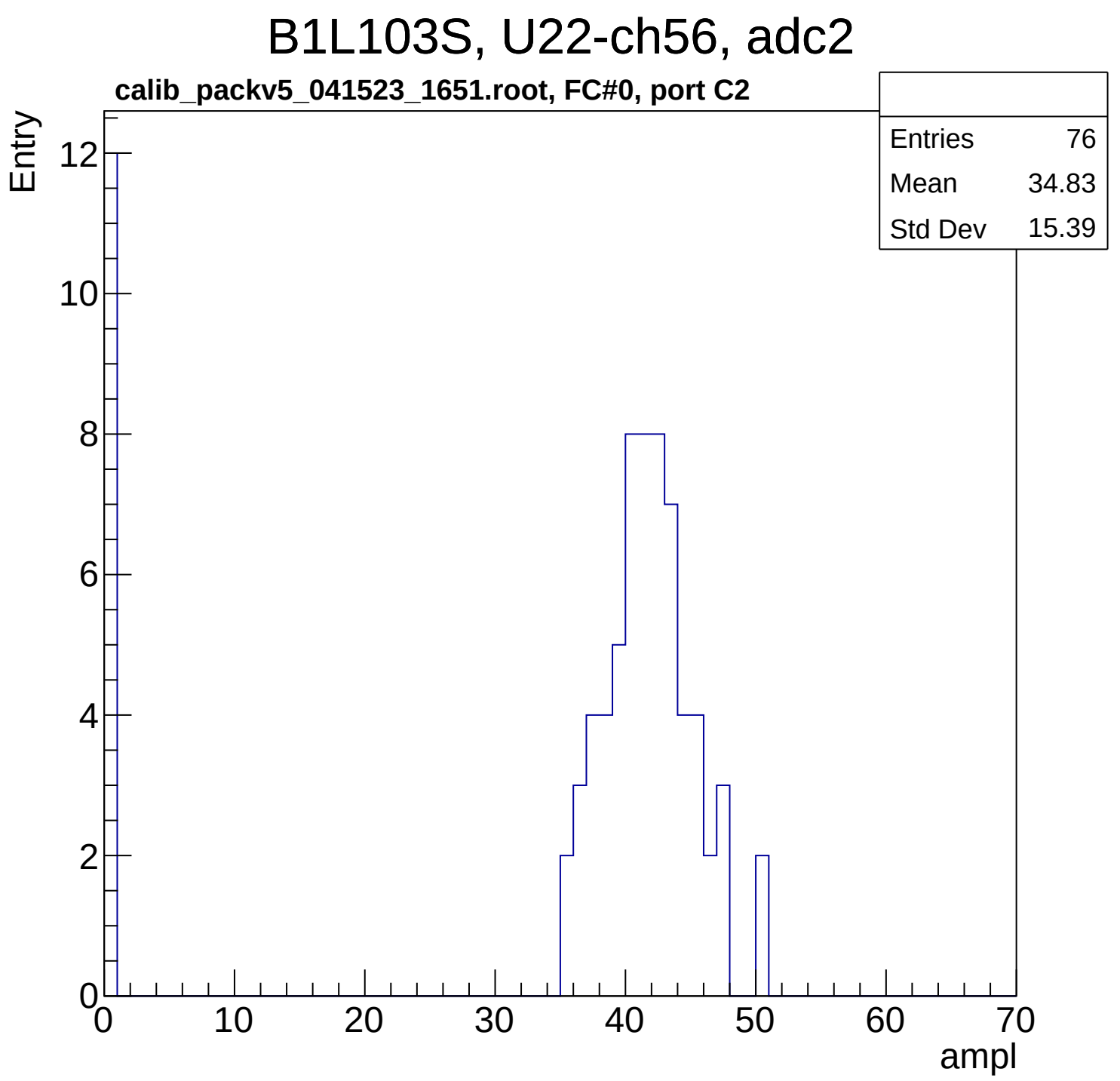
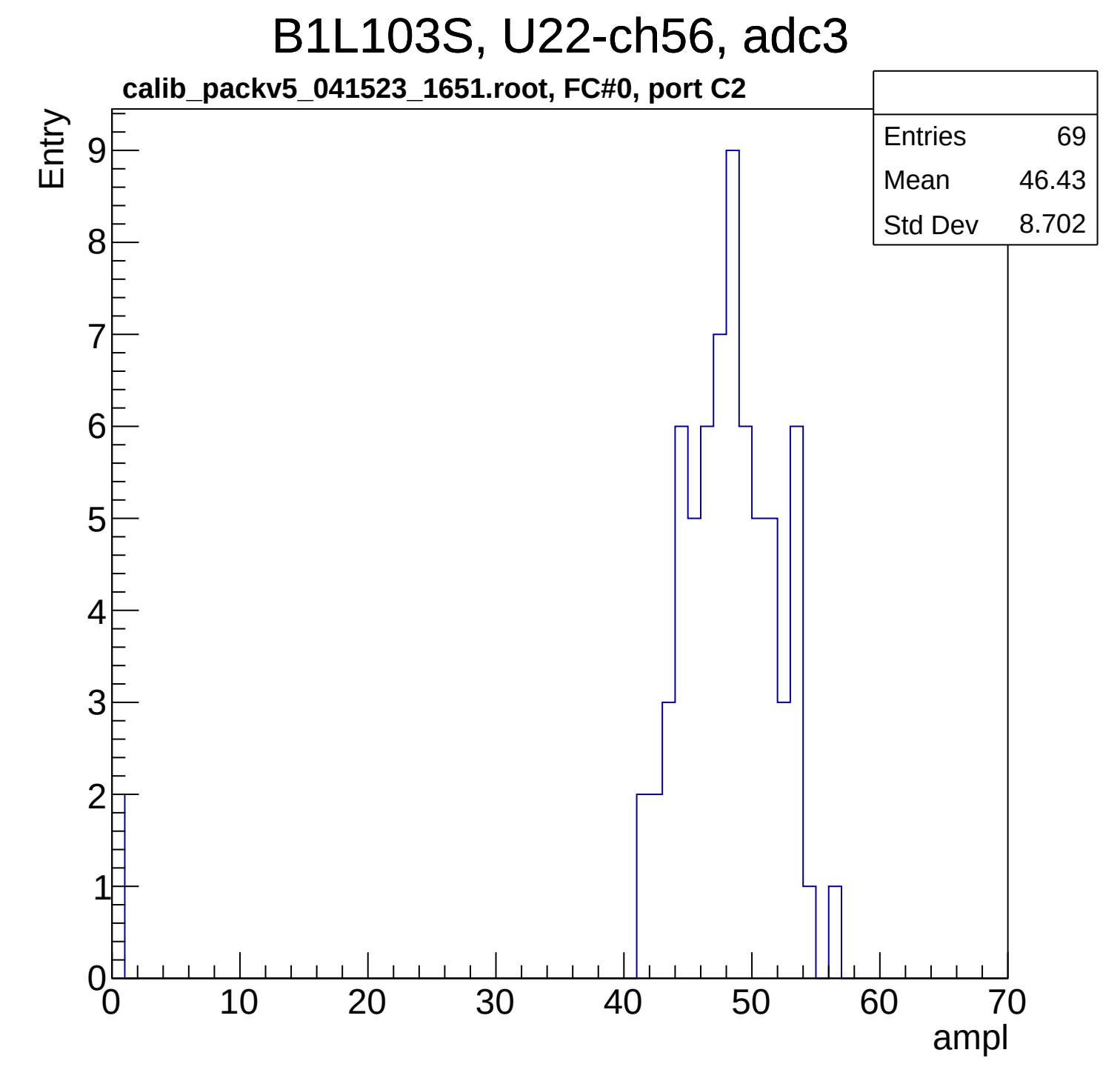

B1L103S, U22-ch55, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch56, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 24.99
Std Dev 9.692
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch56, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 31.58
Std Dev 9.926
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U22-ch56, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 34.83
Std Dev 15.39
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch56, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 46.43
Std Dev 8.702
Entry
ampl
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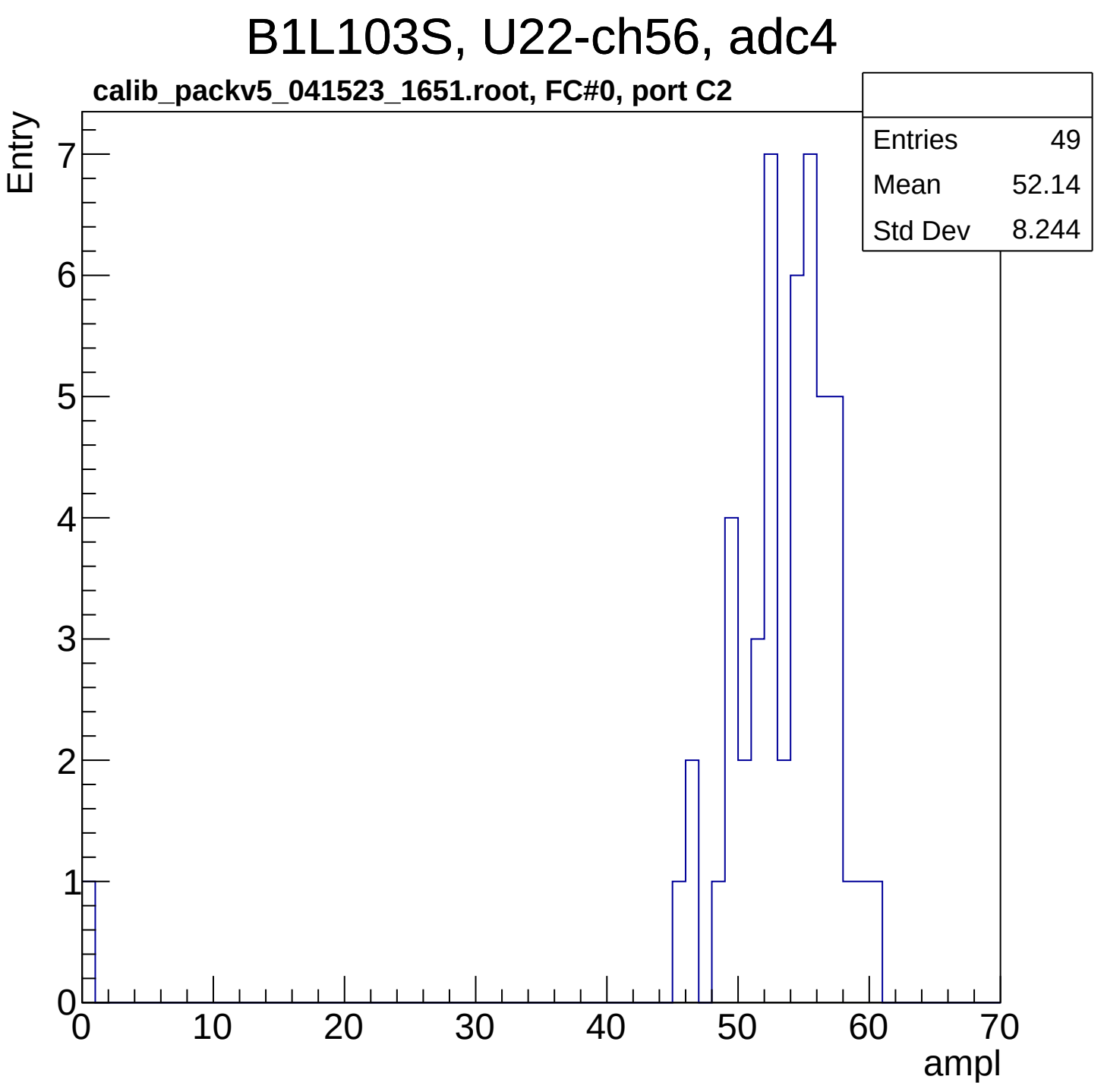
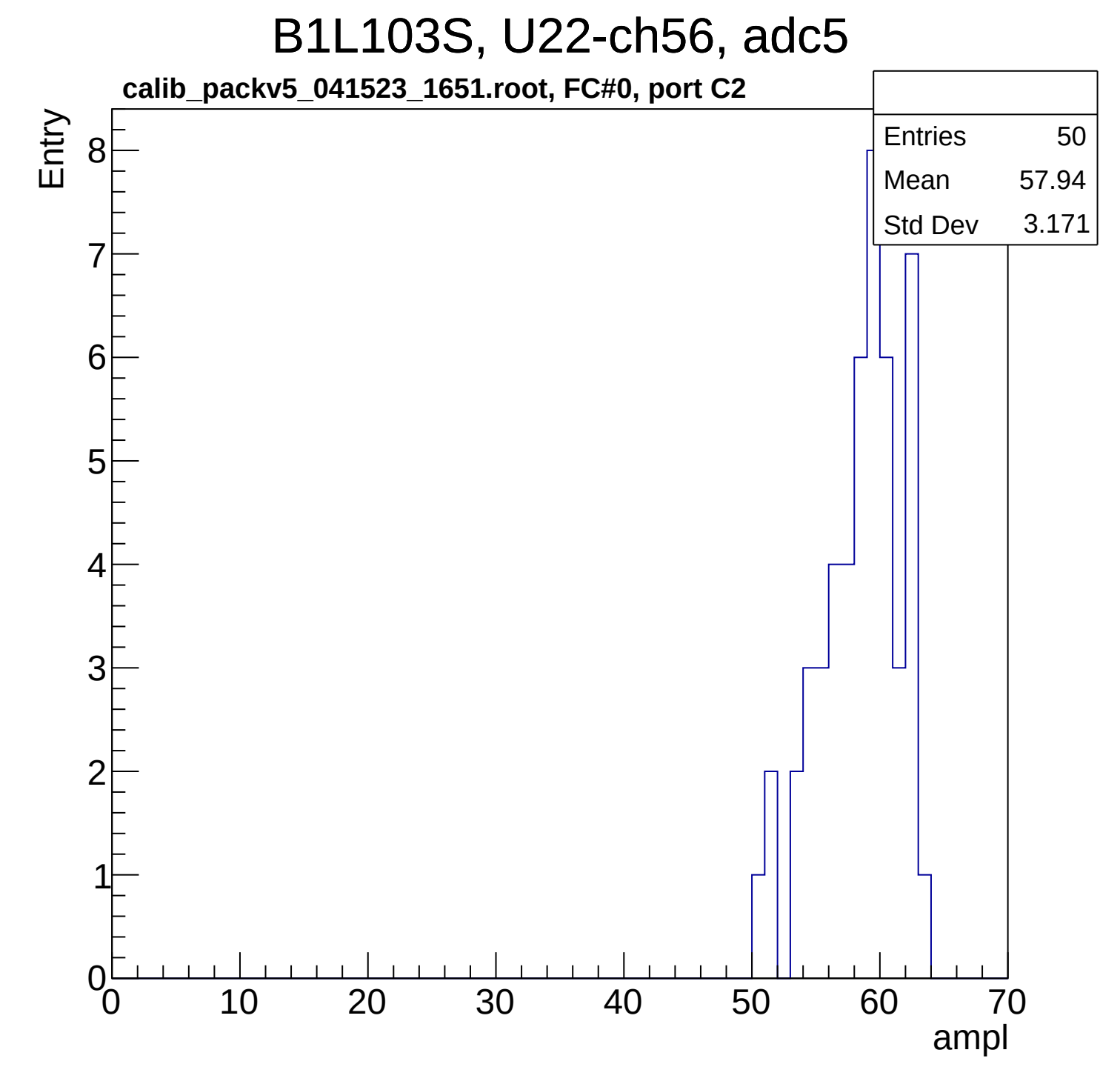
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch56, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 52.14
Std Dev 8.244
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U22-ch56, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 57.94
Std Dev 3.171
Entry
ampl
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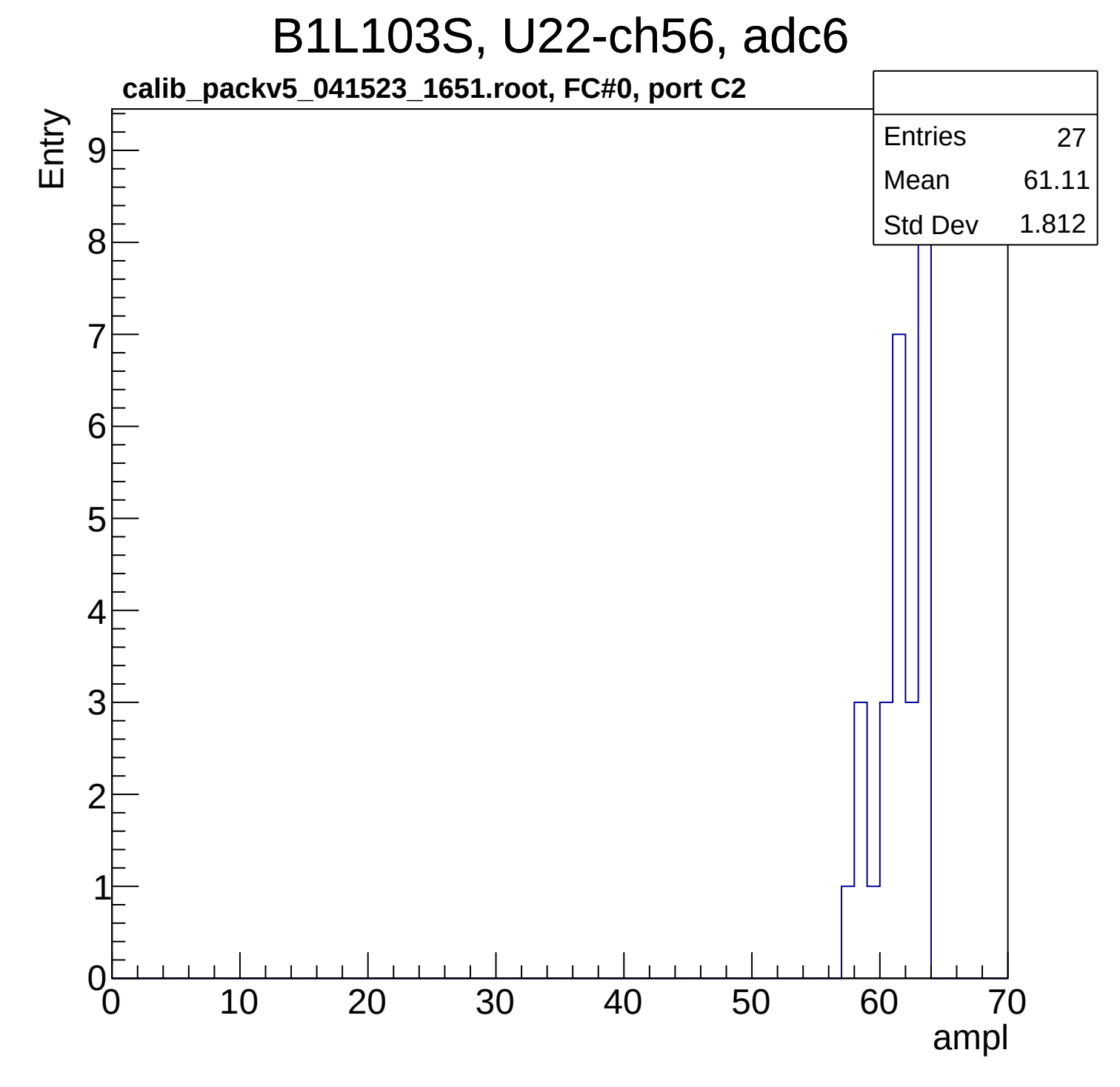
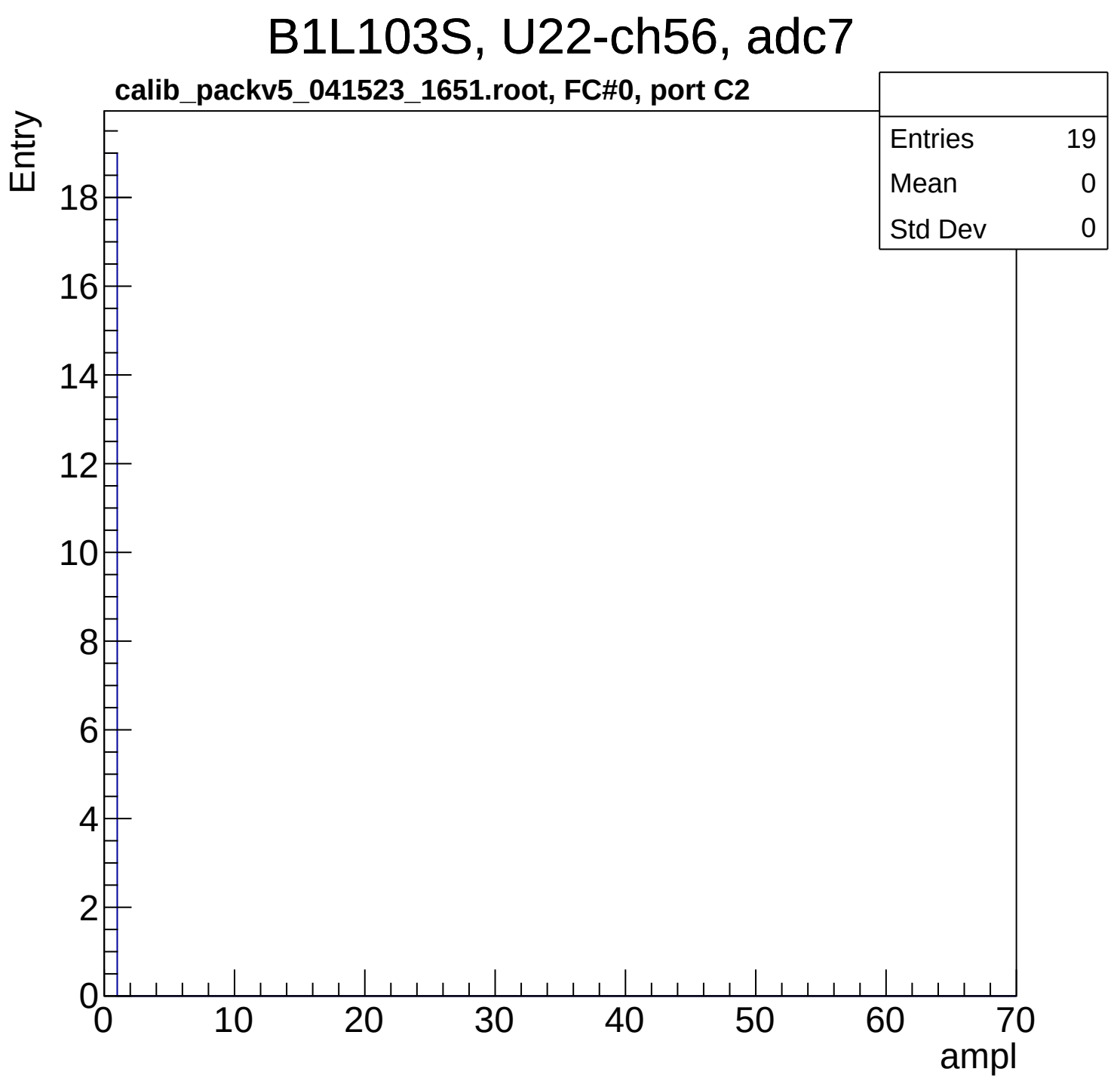
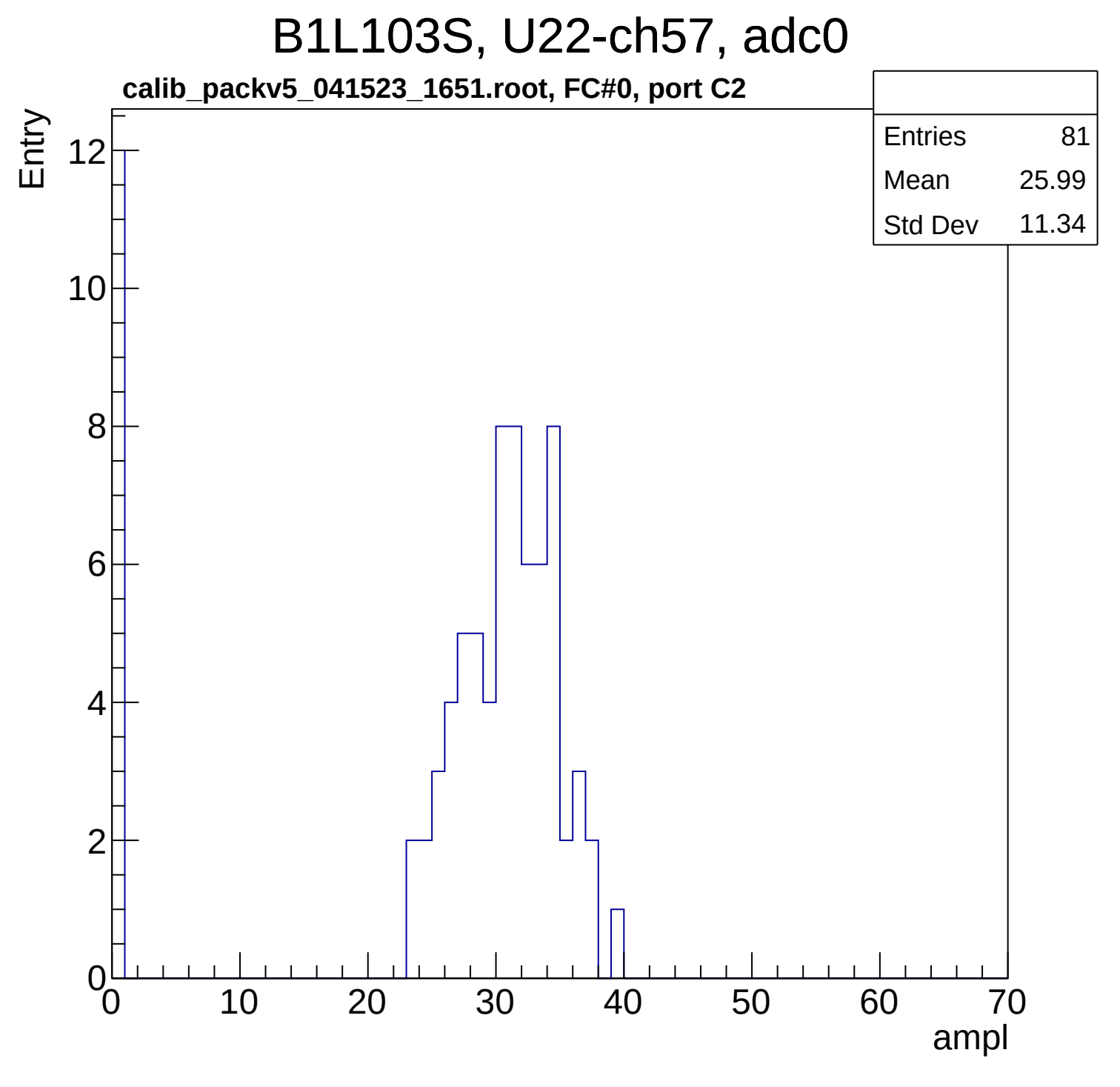
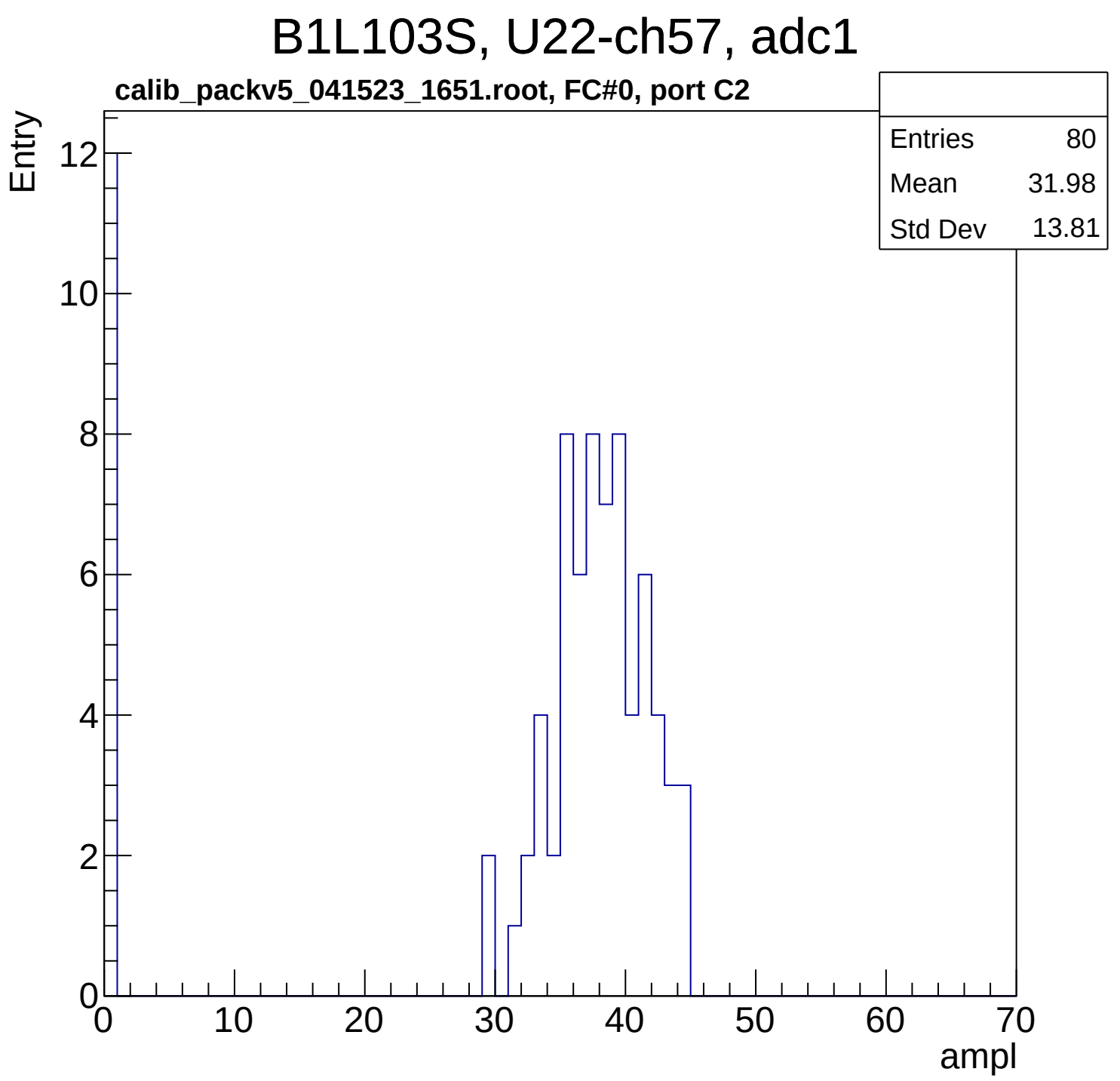
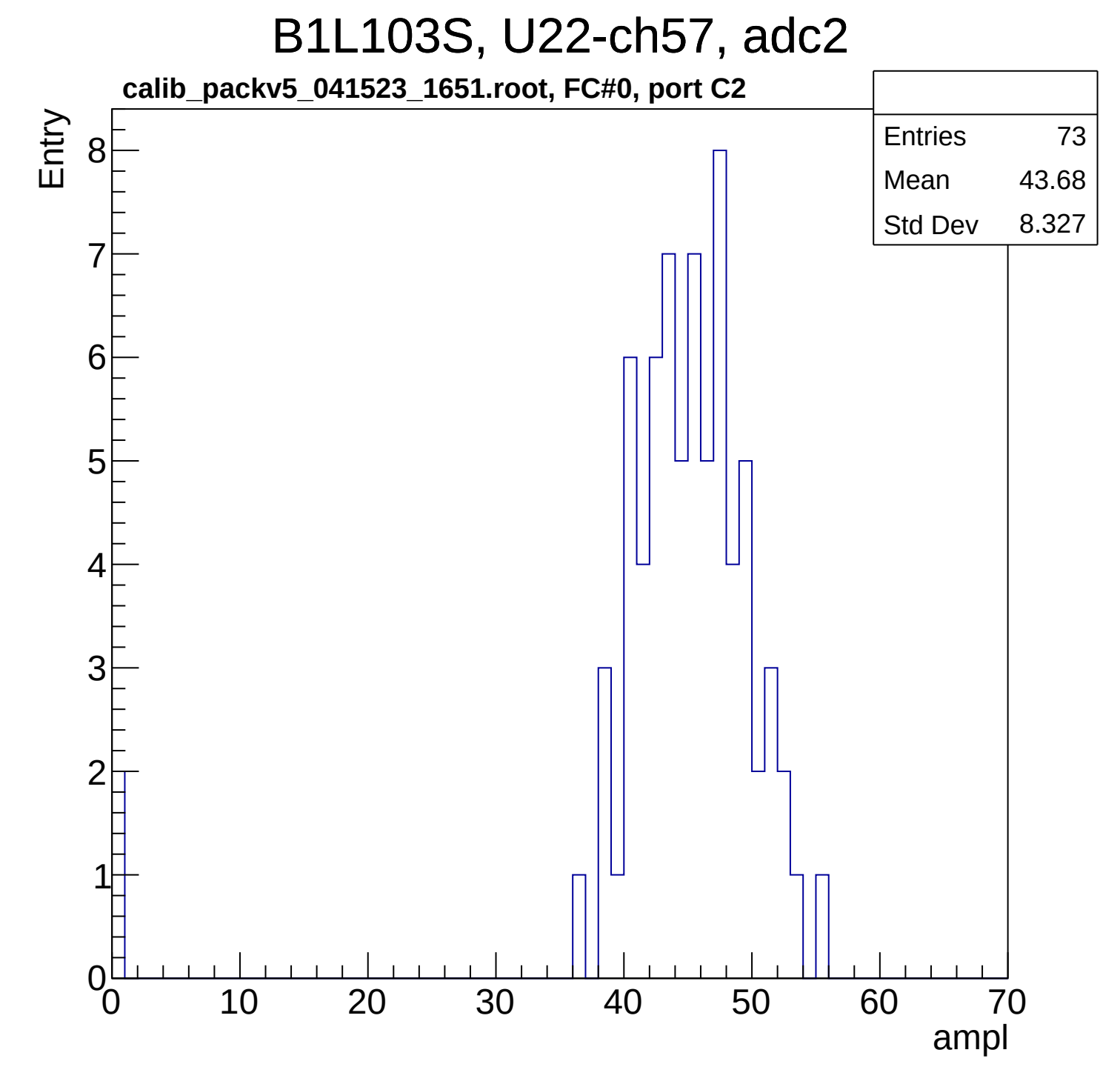
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

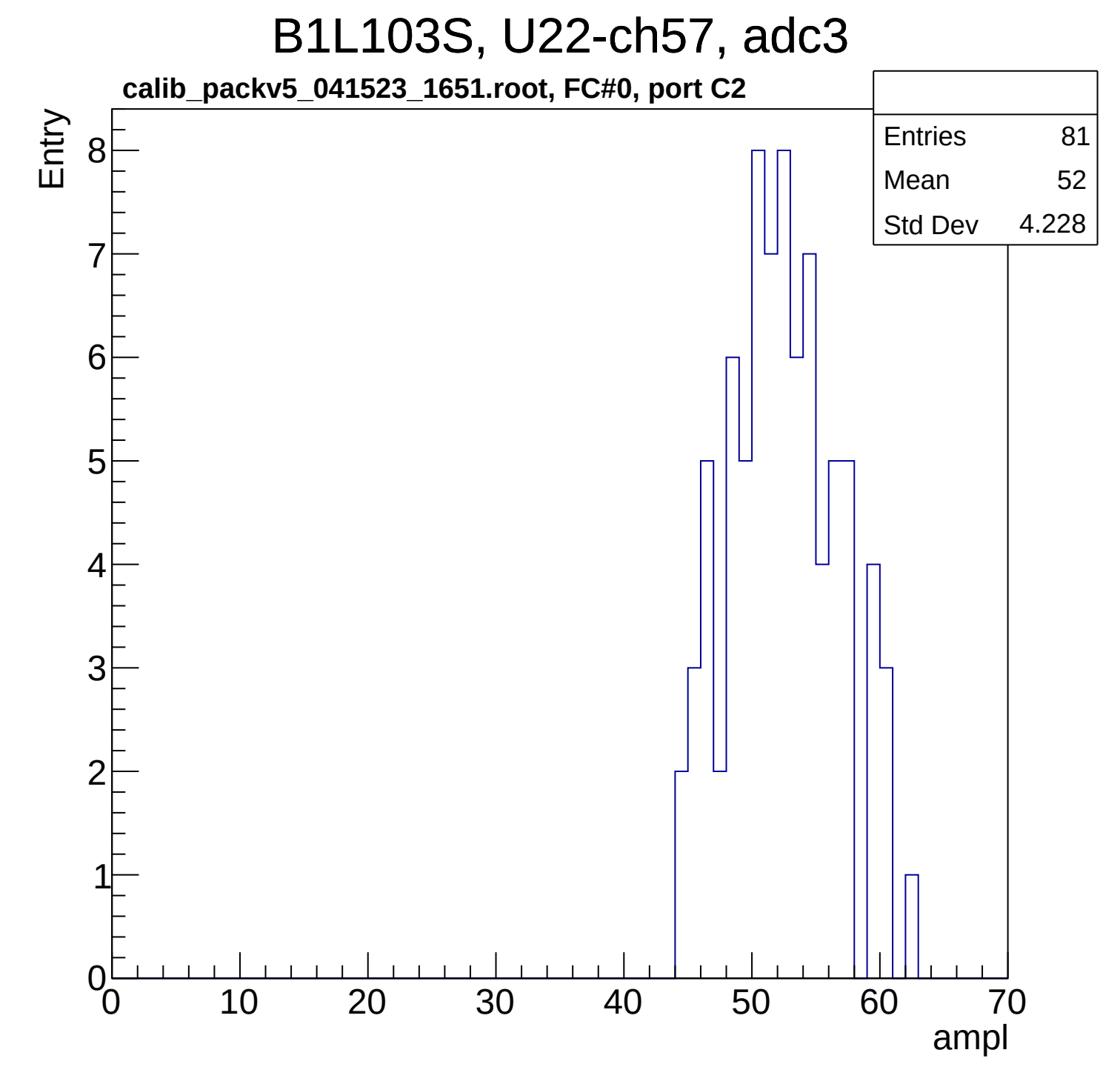

B1L103S, U22-ch56, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 61.11
Std Dev 1.812
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch56, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch57, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 25.99
Std Dev 11.34
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch57, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 31.98
Std Dev 13.81
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch57, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 43.68
Std Dev 8.327
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch57, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 52
Std Dev 4.228
Entry
ampl
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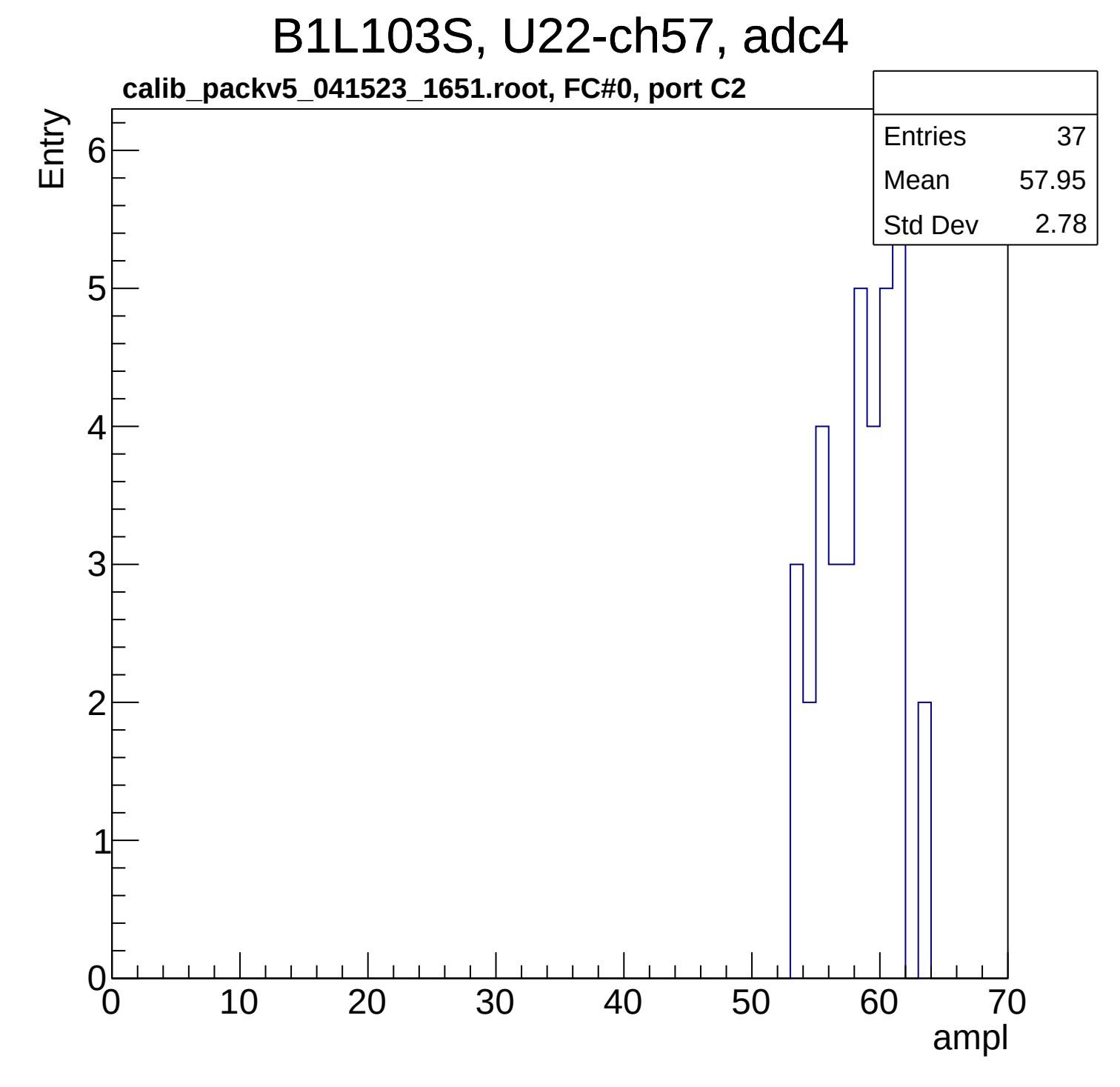
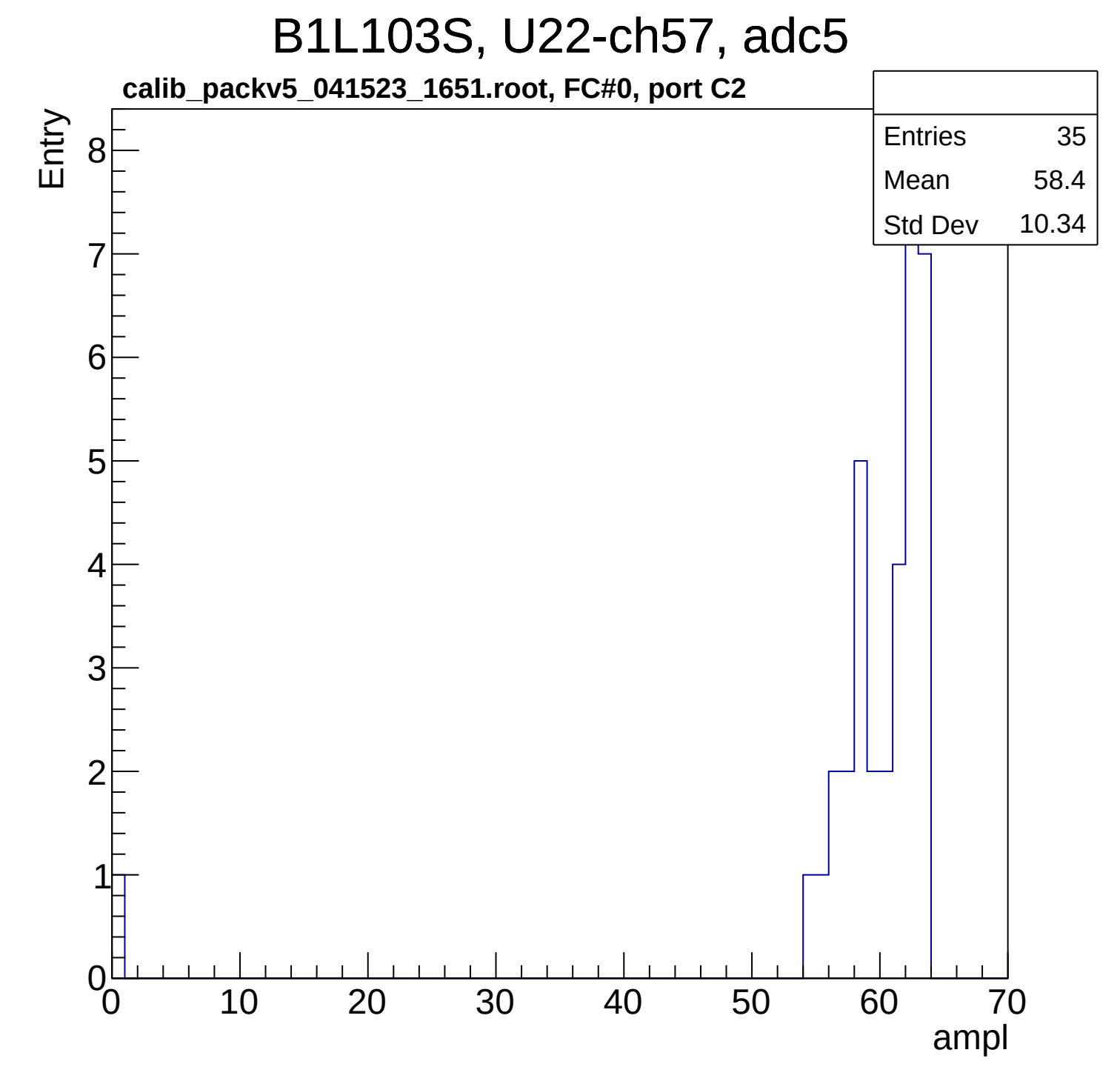
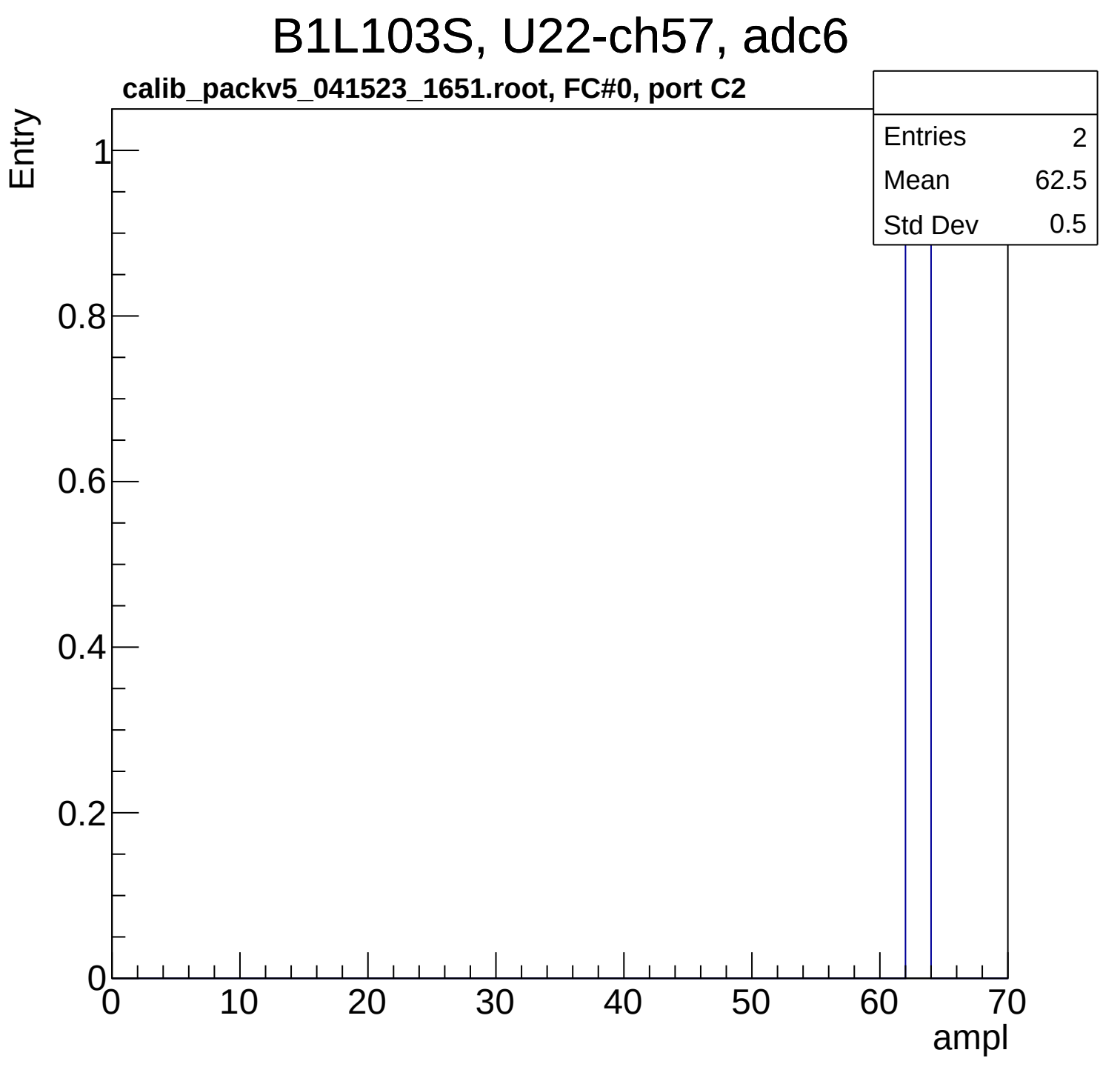
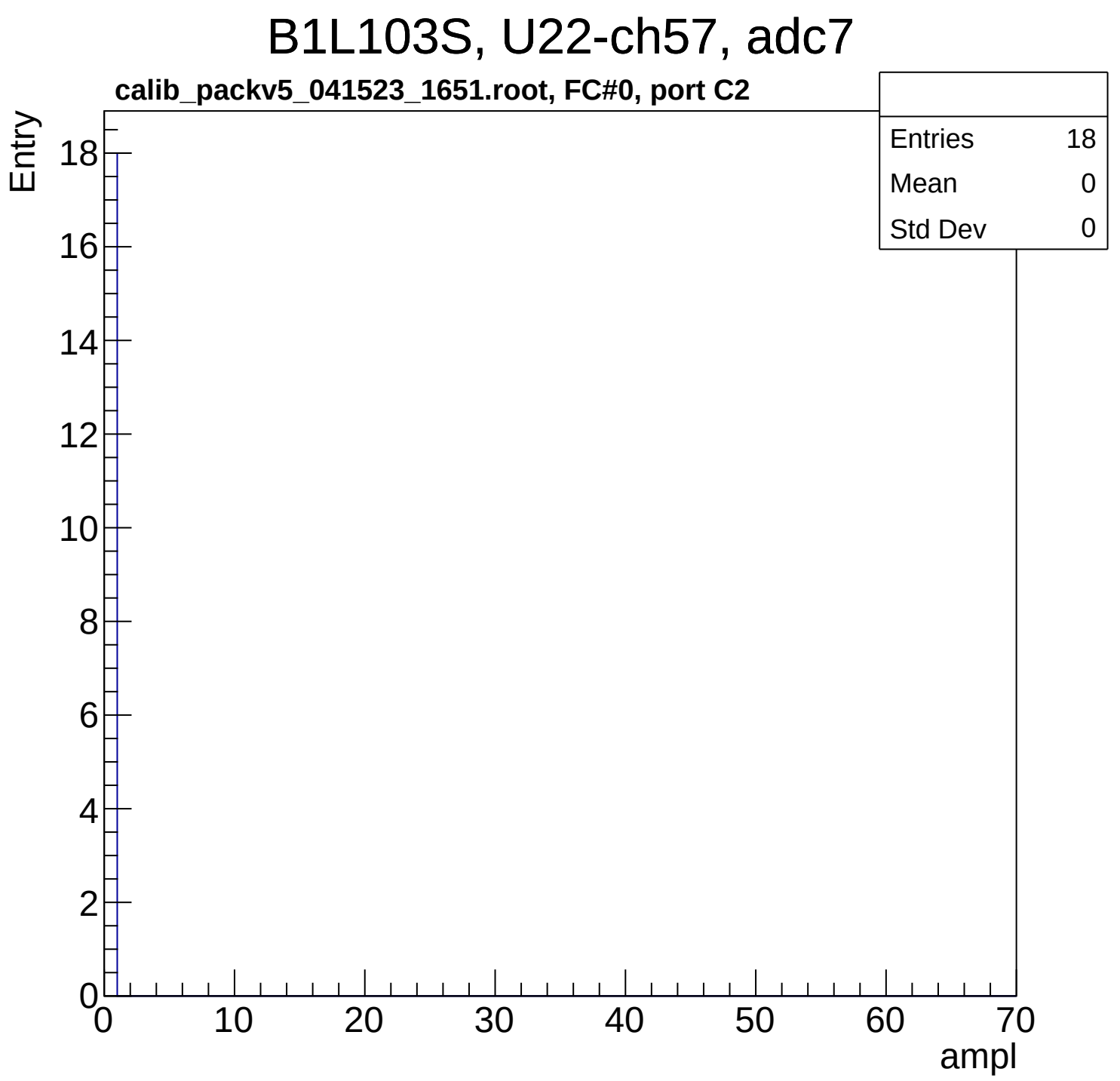
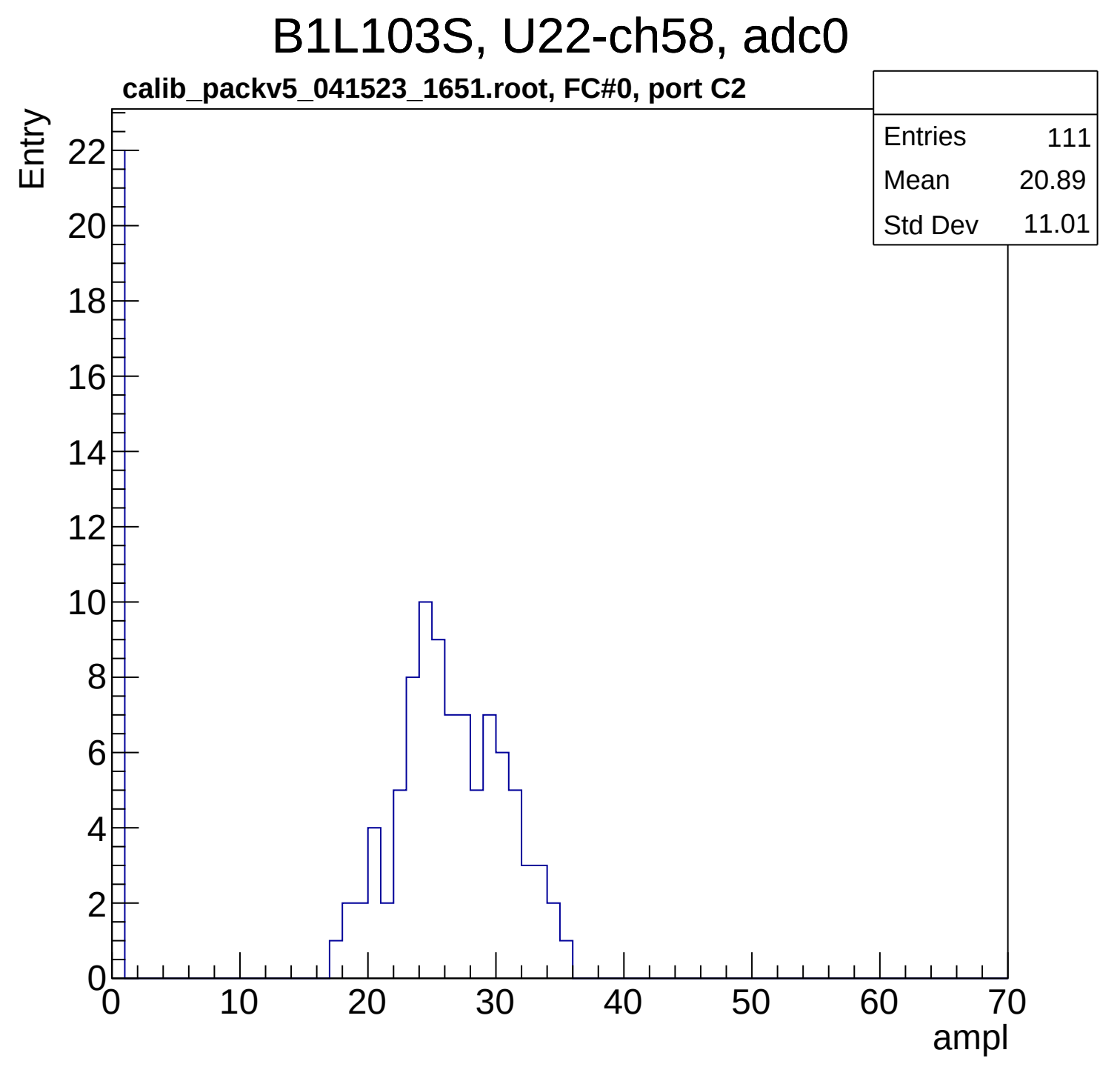
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

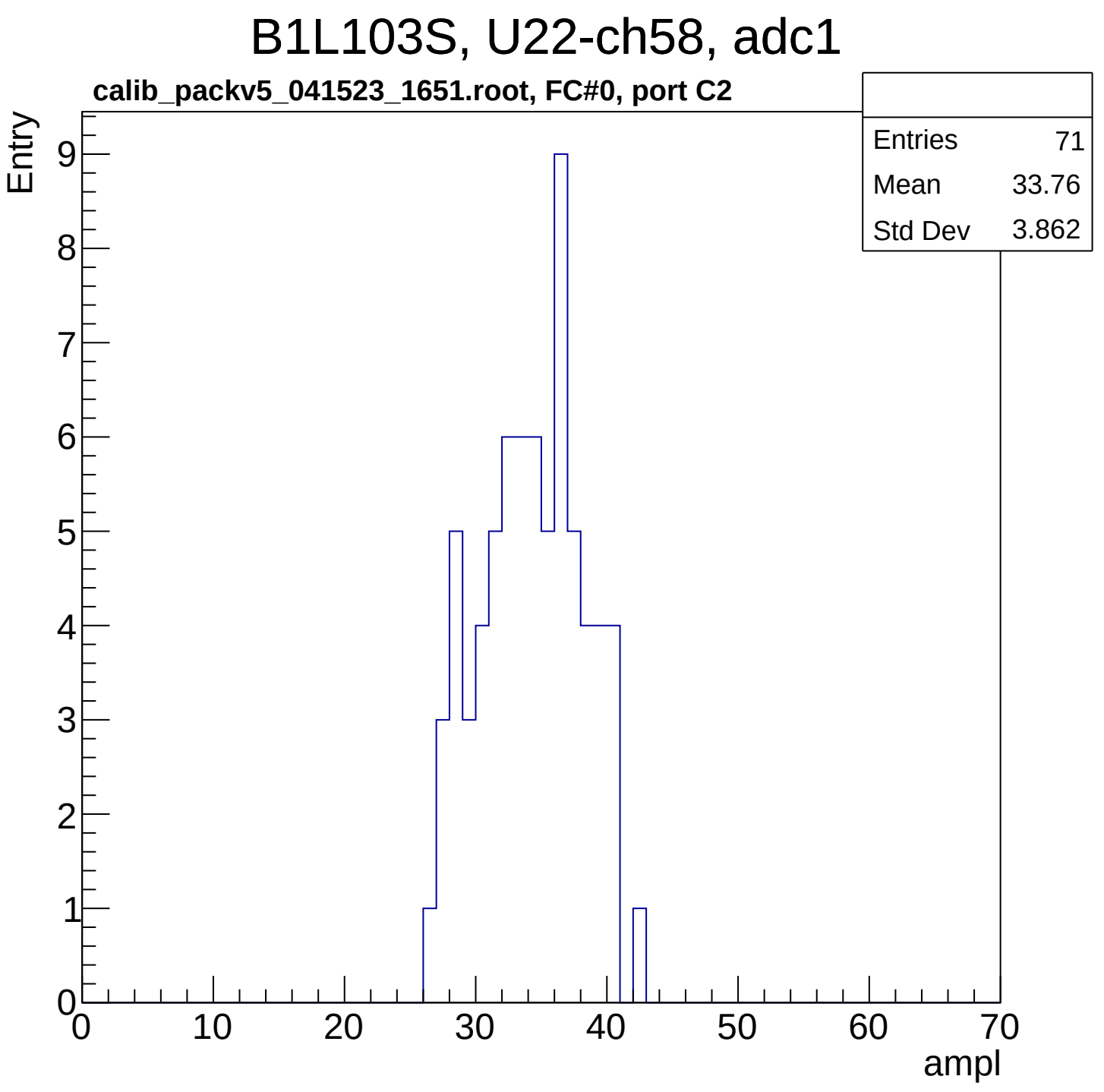

B1L103S, U22-ch57, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 57.95
Std Dev 2.78
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

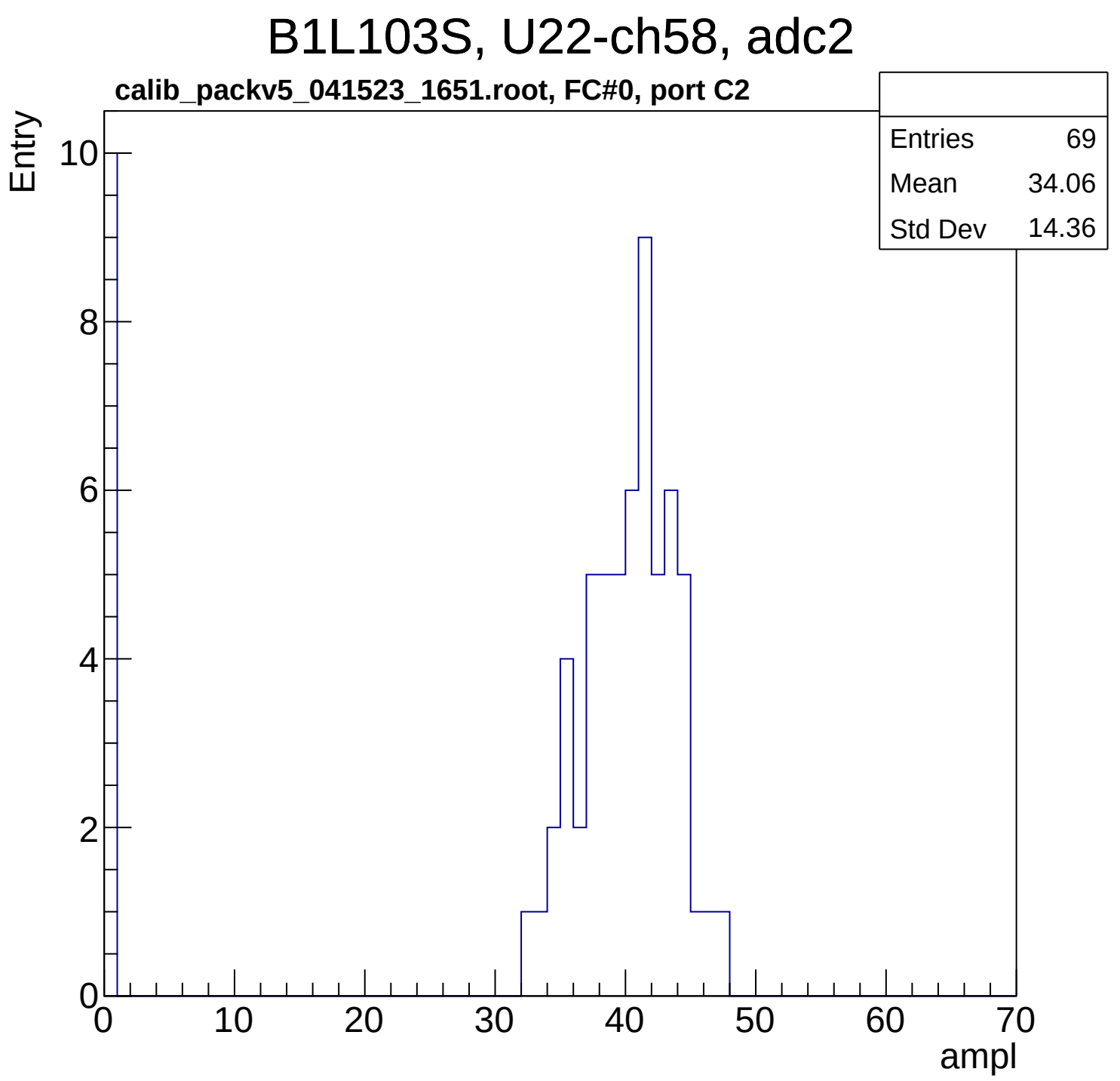

B1L103S, U22-ch57, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 58.4
Std Dev 10.34
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

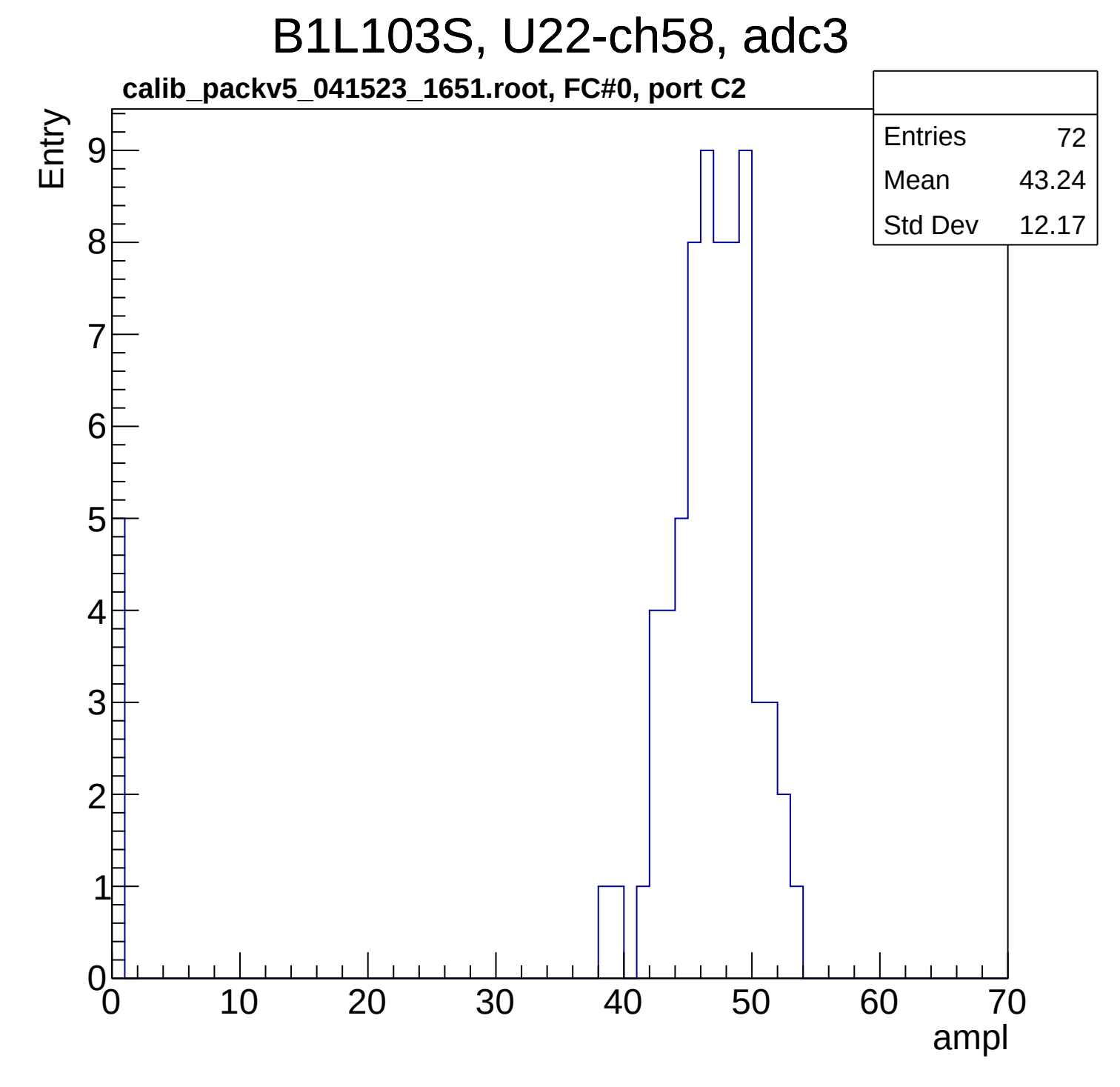

B1L103S, U22-ch57, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch57, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch58, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 111
Mean 20.89
Std Dev 11.01
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70


B1L103S, U22-ch58, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 33.76
Std Dev 3.862
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch58, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 34.06
Std Dev 14.36
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch58, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 43.24
Std Dev 12.17
Entry
ampl
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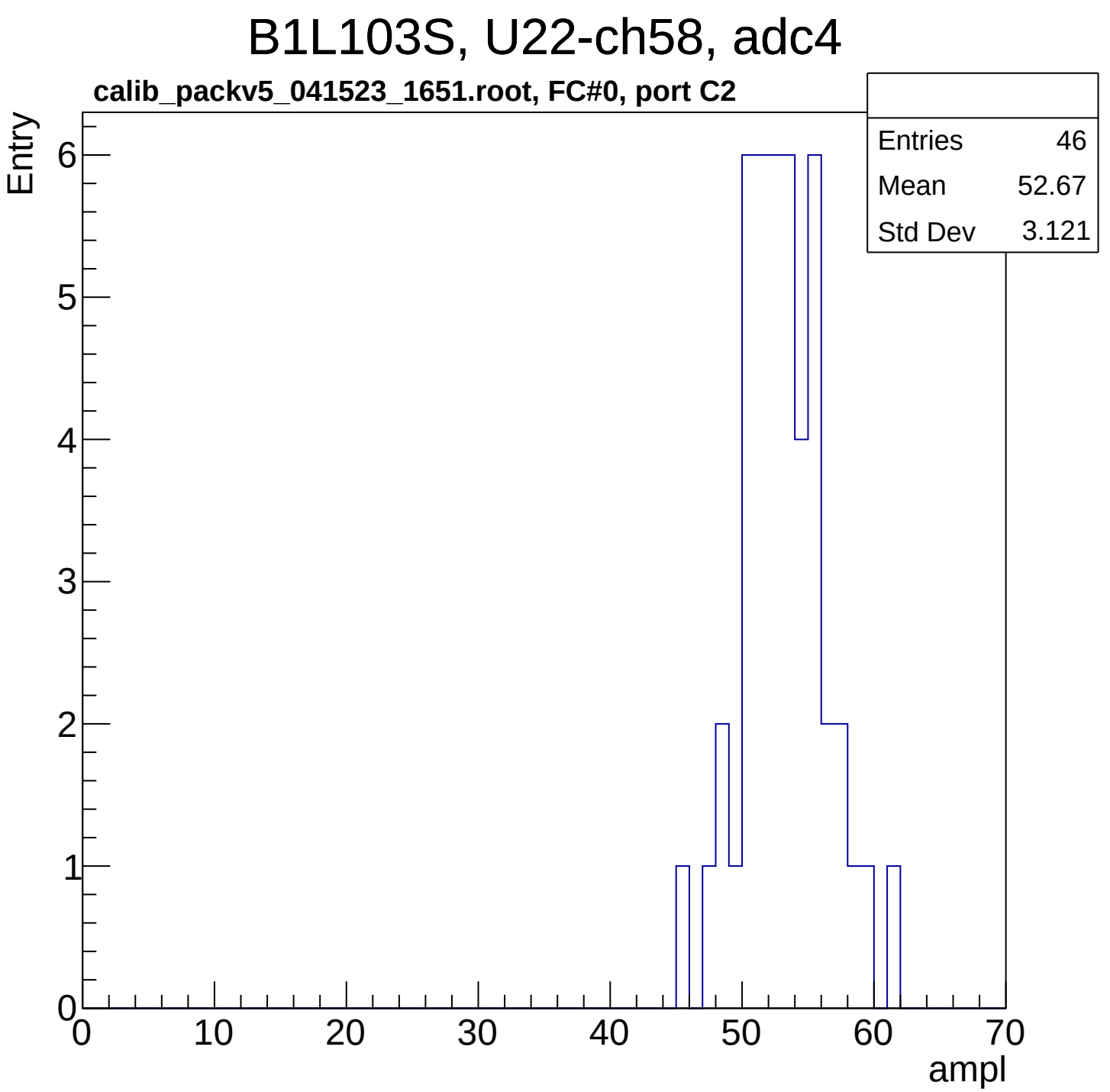
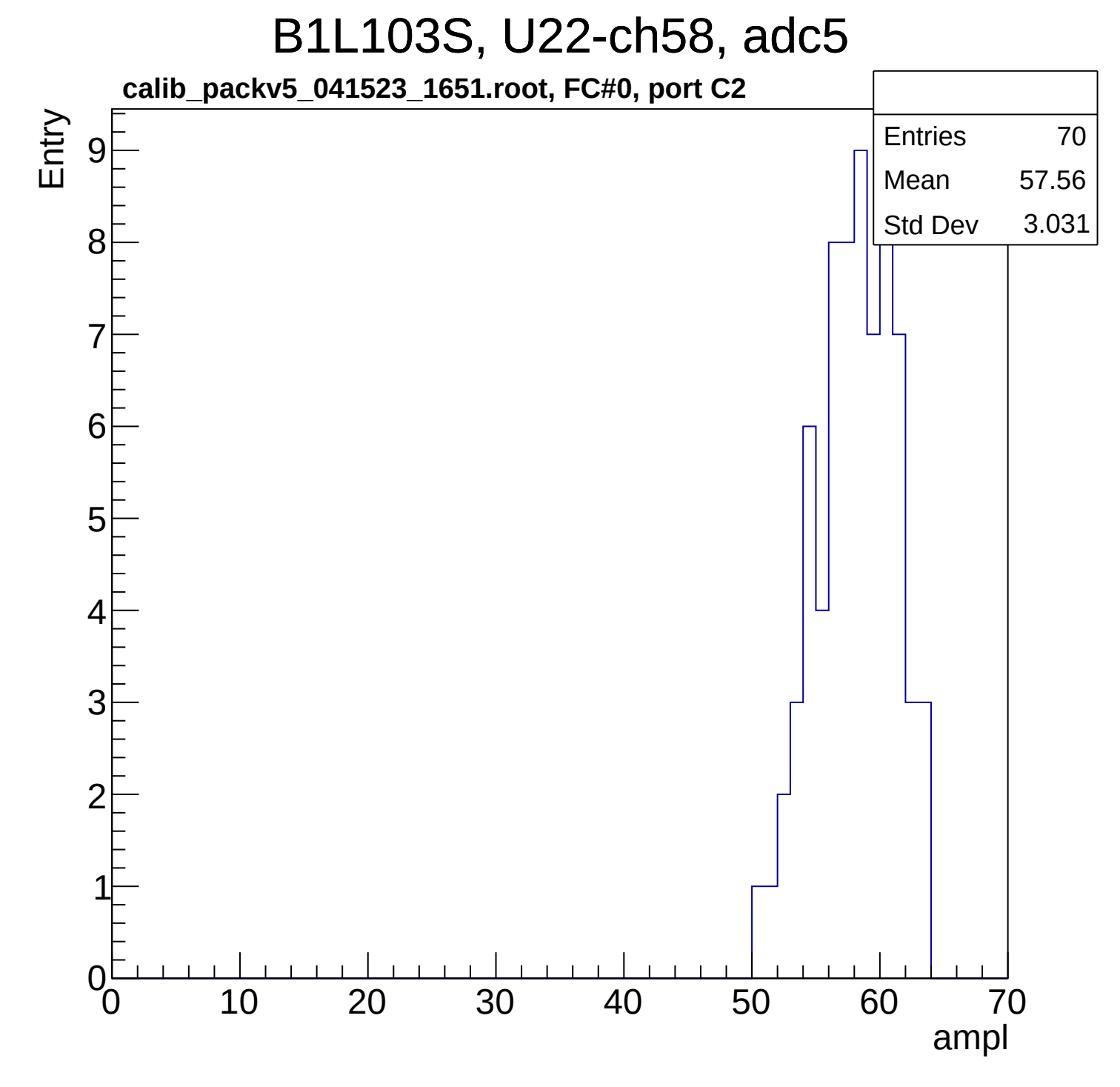
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch58, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 52.67
Std Dev 3.121
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U22-ch58, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 57.56
Std Dev 3.031
Entry
ampl
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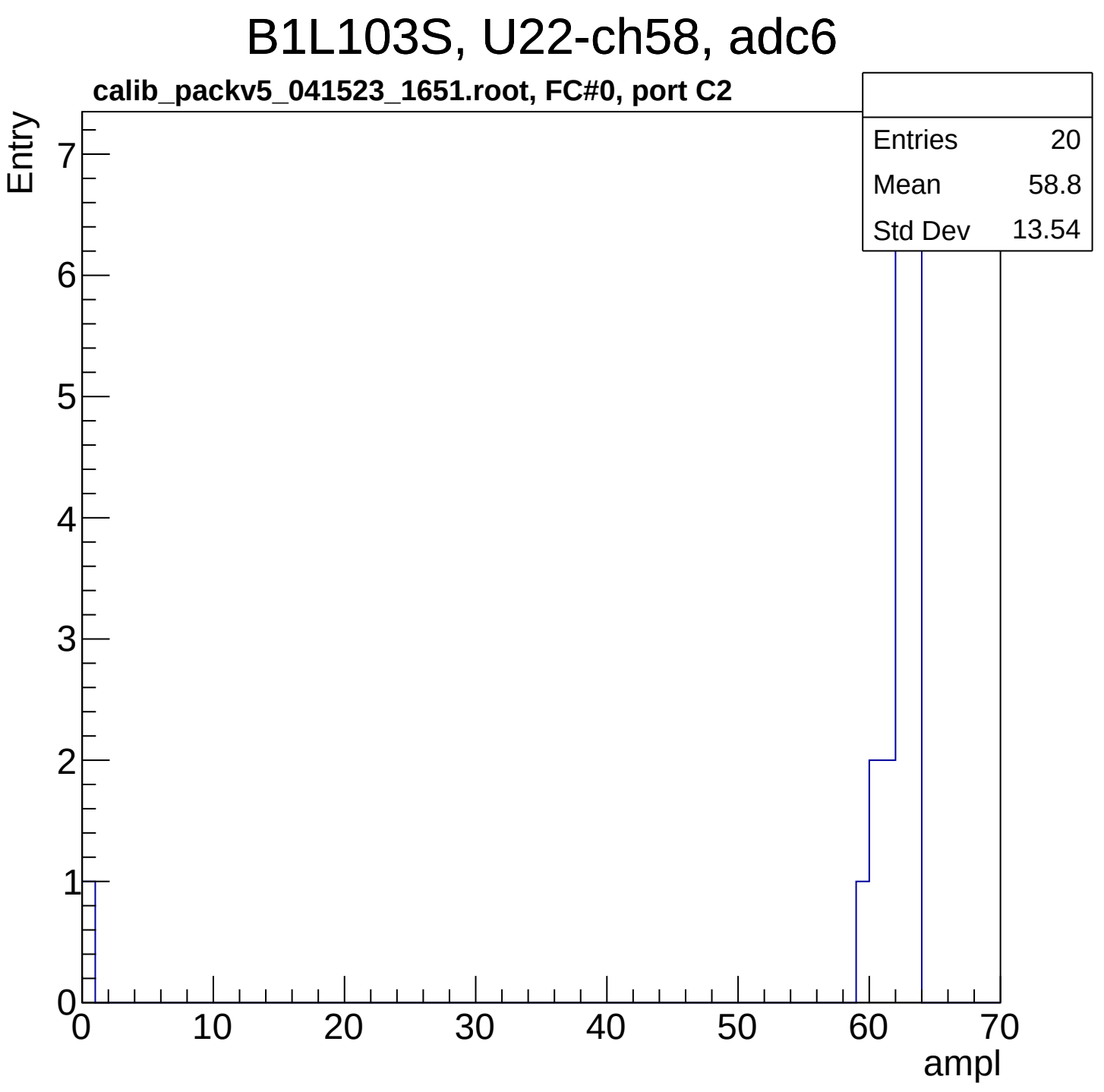
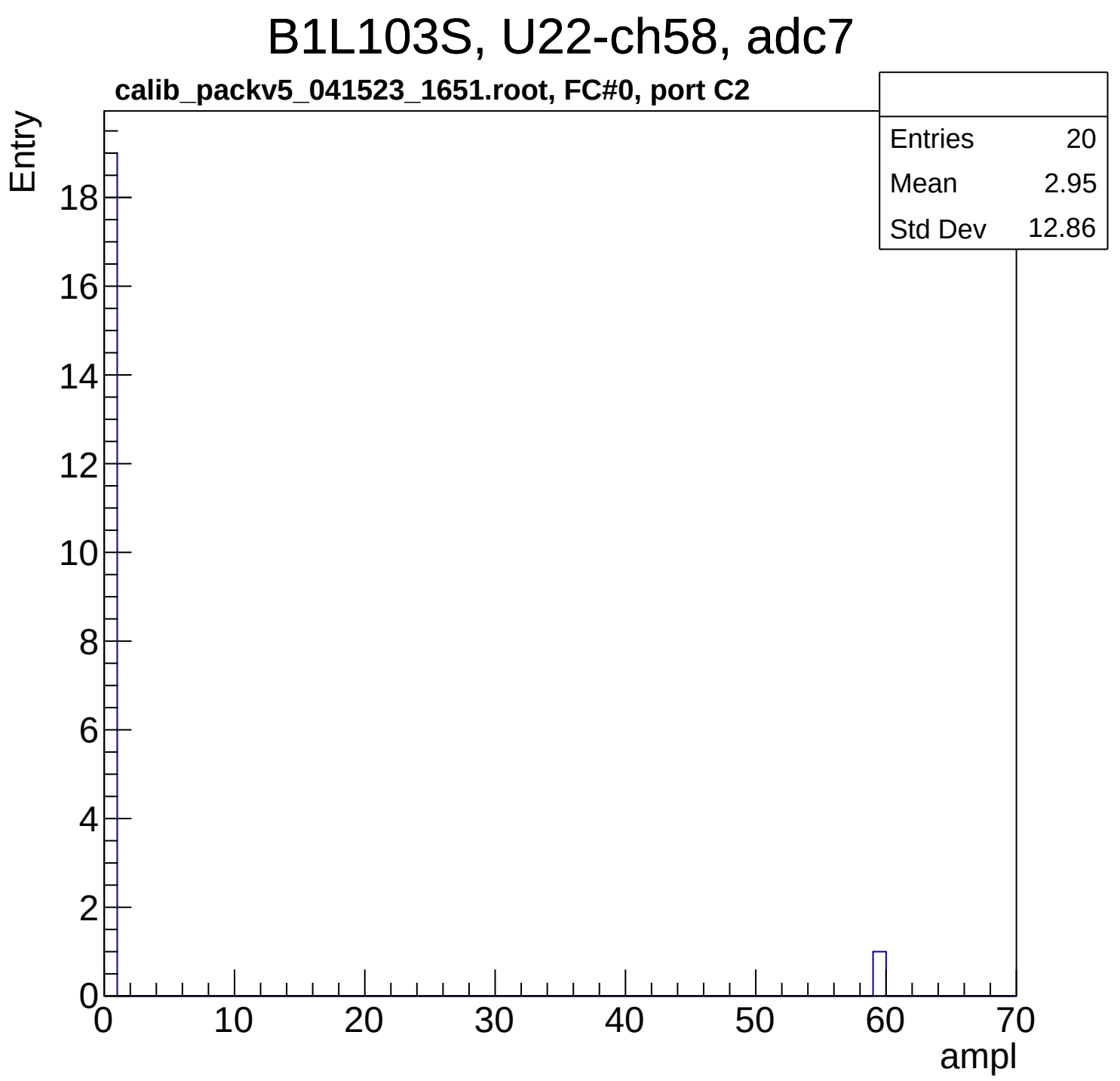
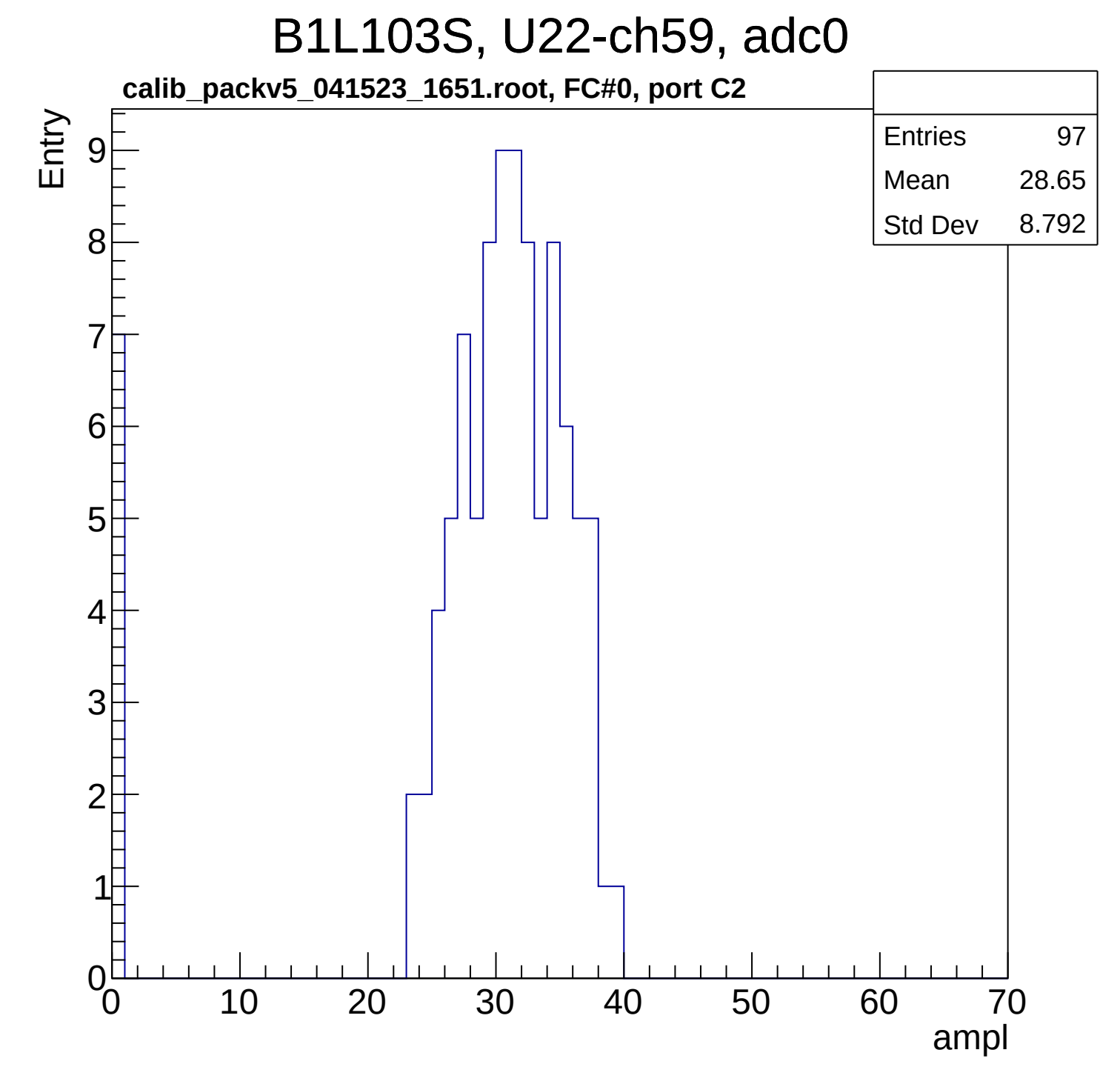
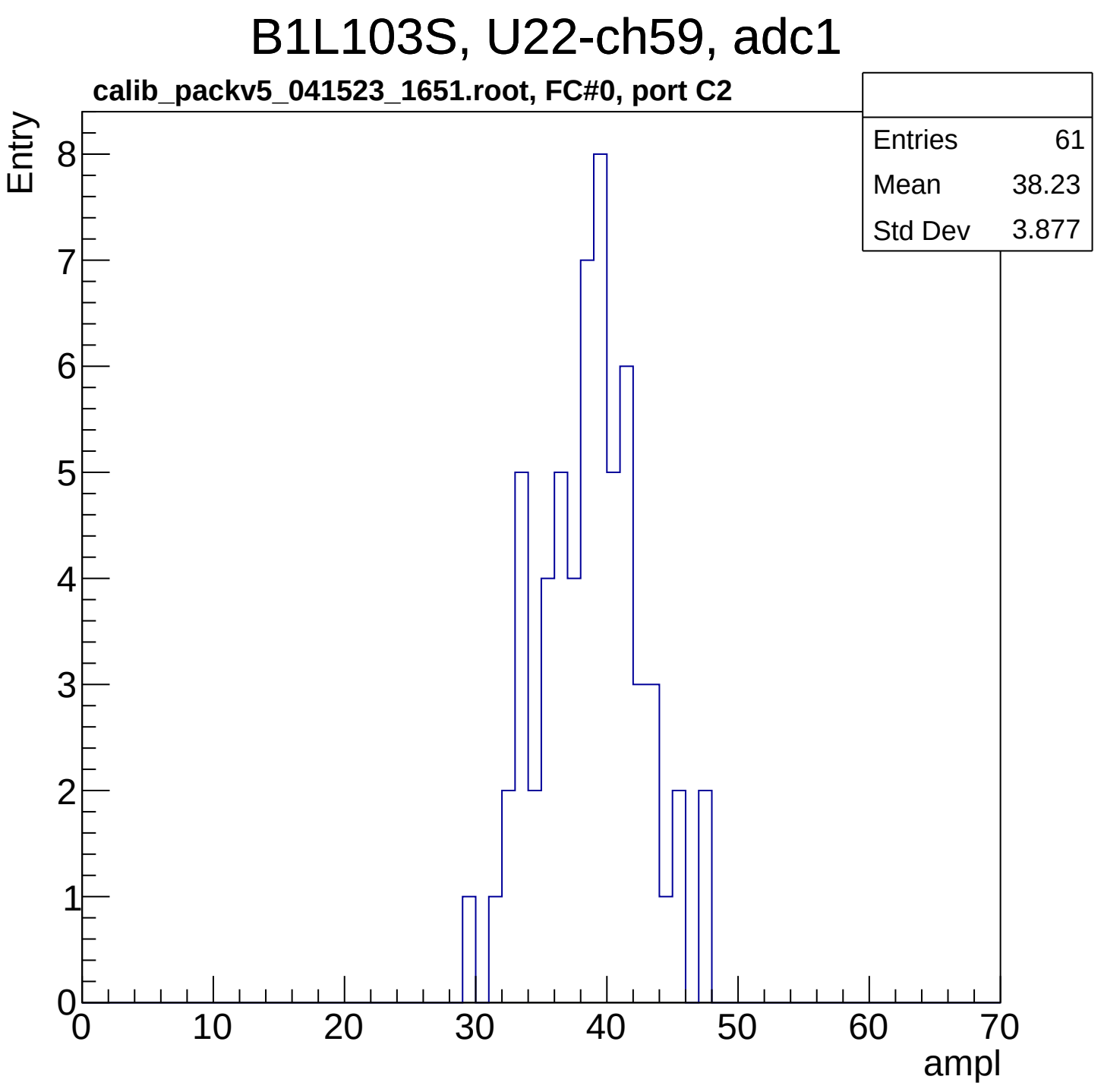
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch58, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 58.8
Std Dev 13.54
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U22-ch58, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 2.95
Std Dev 12.86
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch59, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 28.65
Std Dev 8.792
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch59, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 38.23
Std Dev 3.877
Entry
ampl
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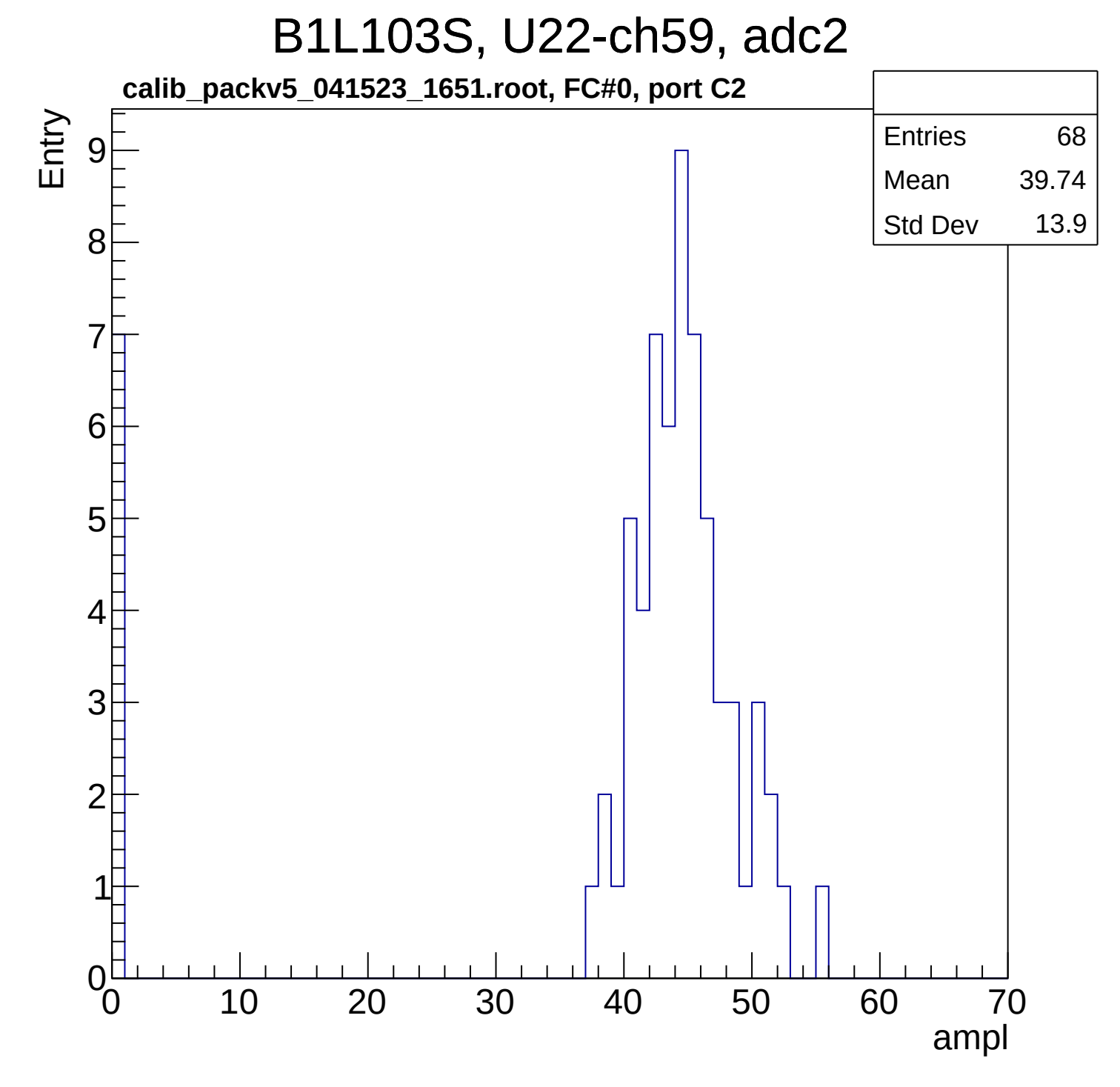
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch59, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 39.74
Std Dev 13.9
Entry
ampl
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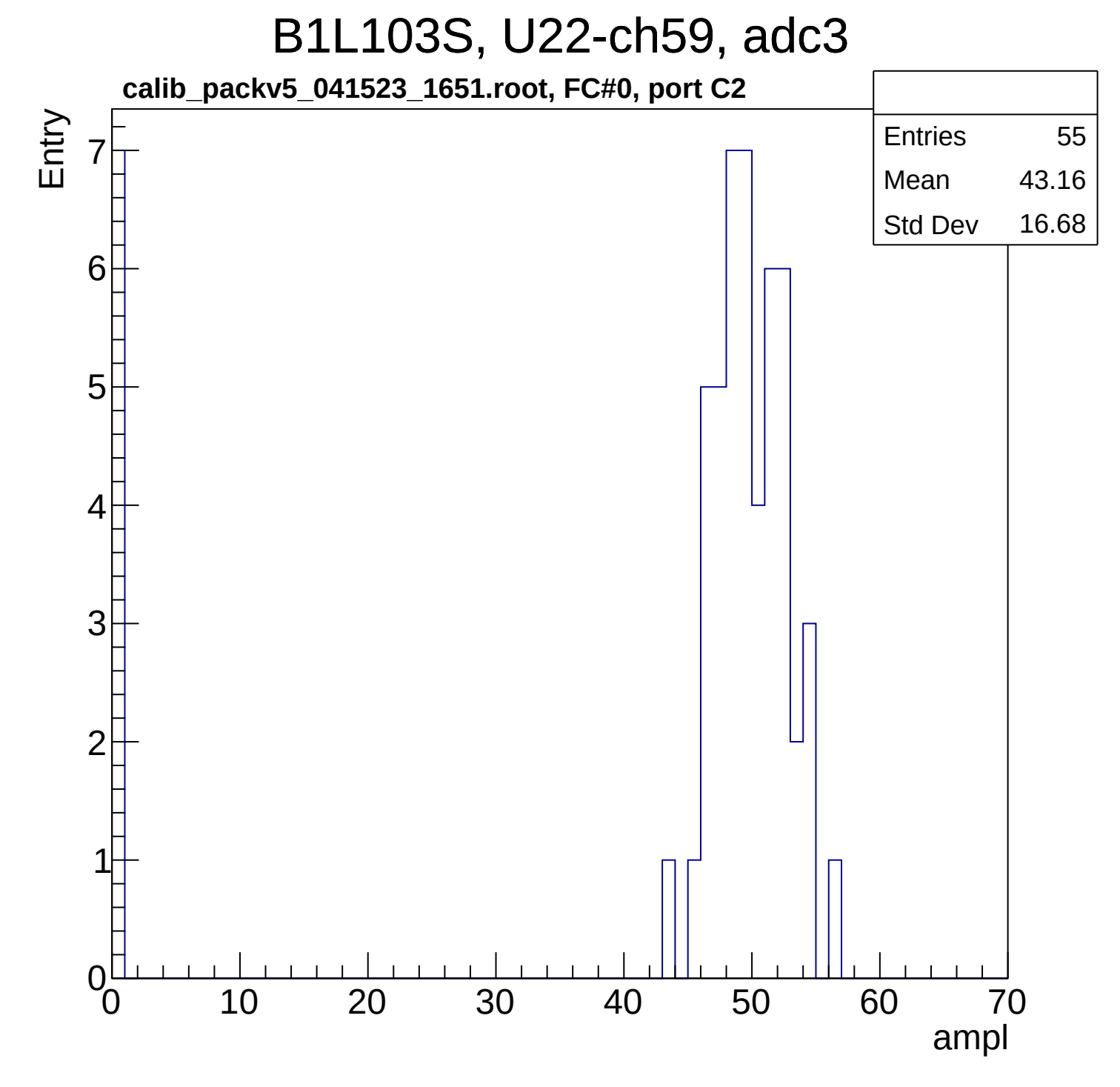
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch59, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 43.16
Std Dev 16.68
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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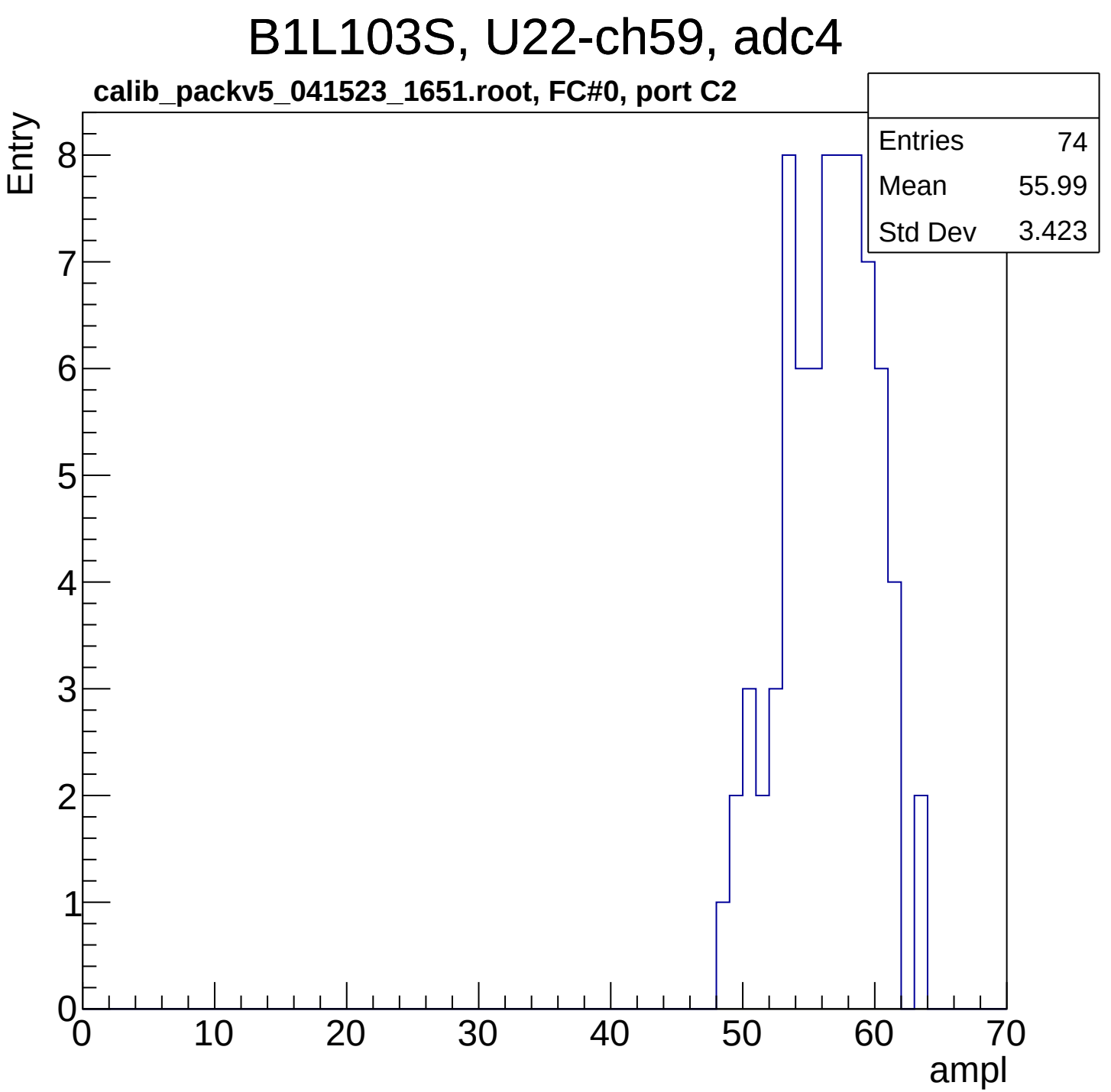
B1L103S, U22-ch59, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 55.99
Std Dev 3.423
Entry
ampl
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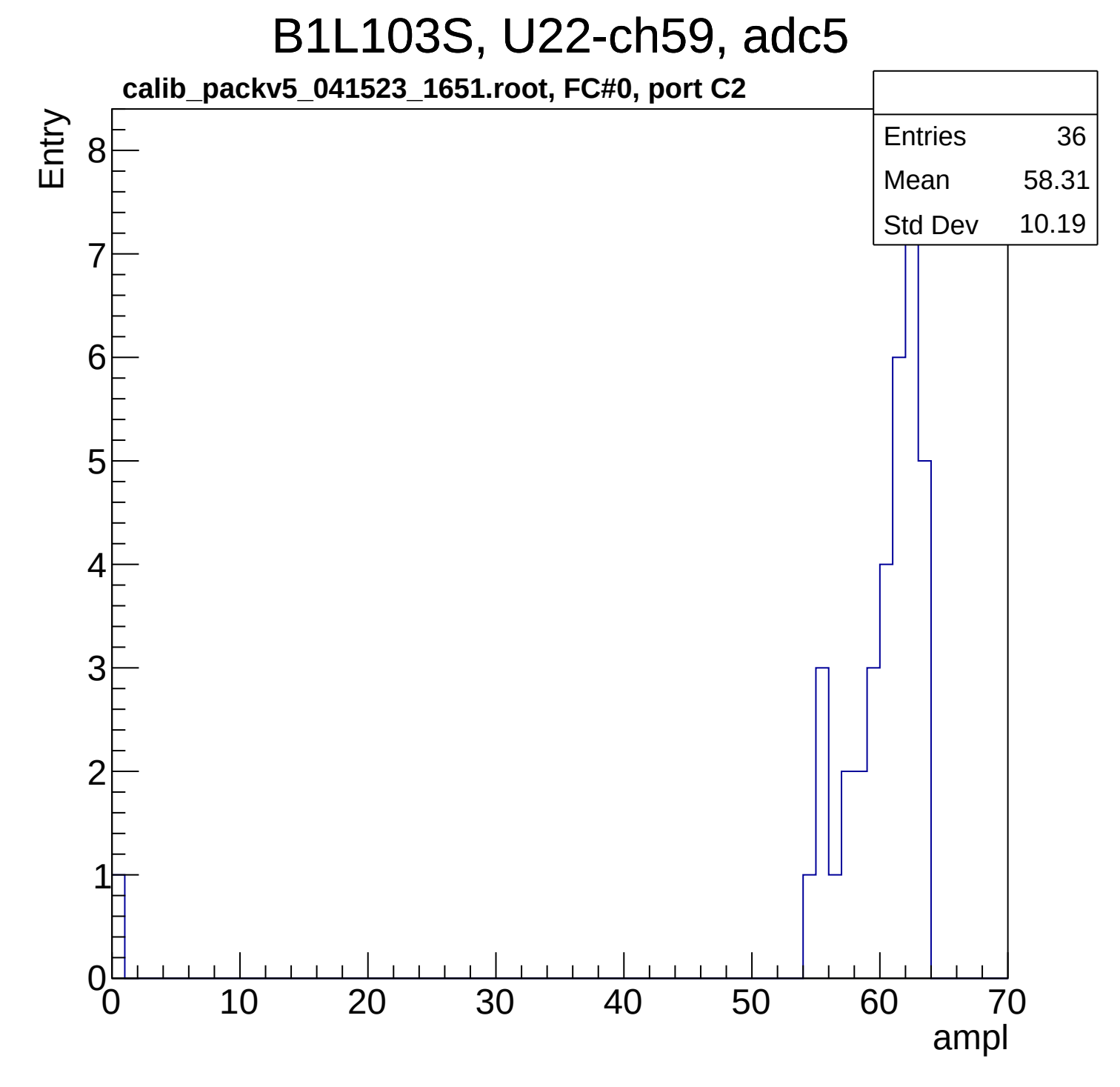
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch59, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 58.31
Std Dev 10.19
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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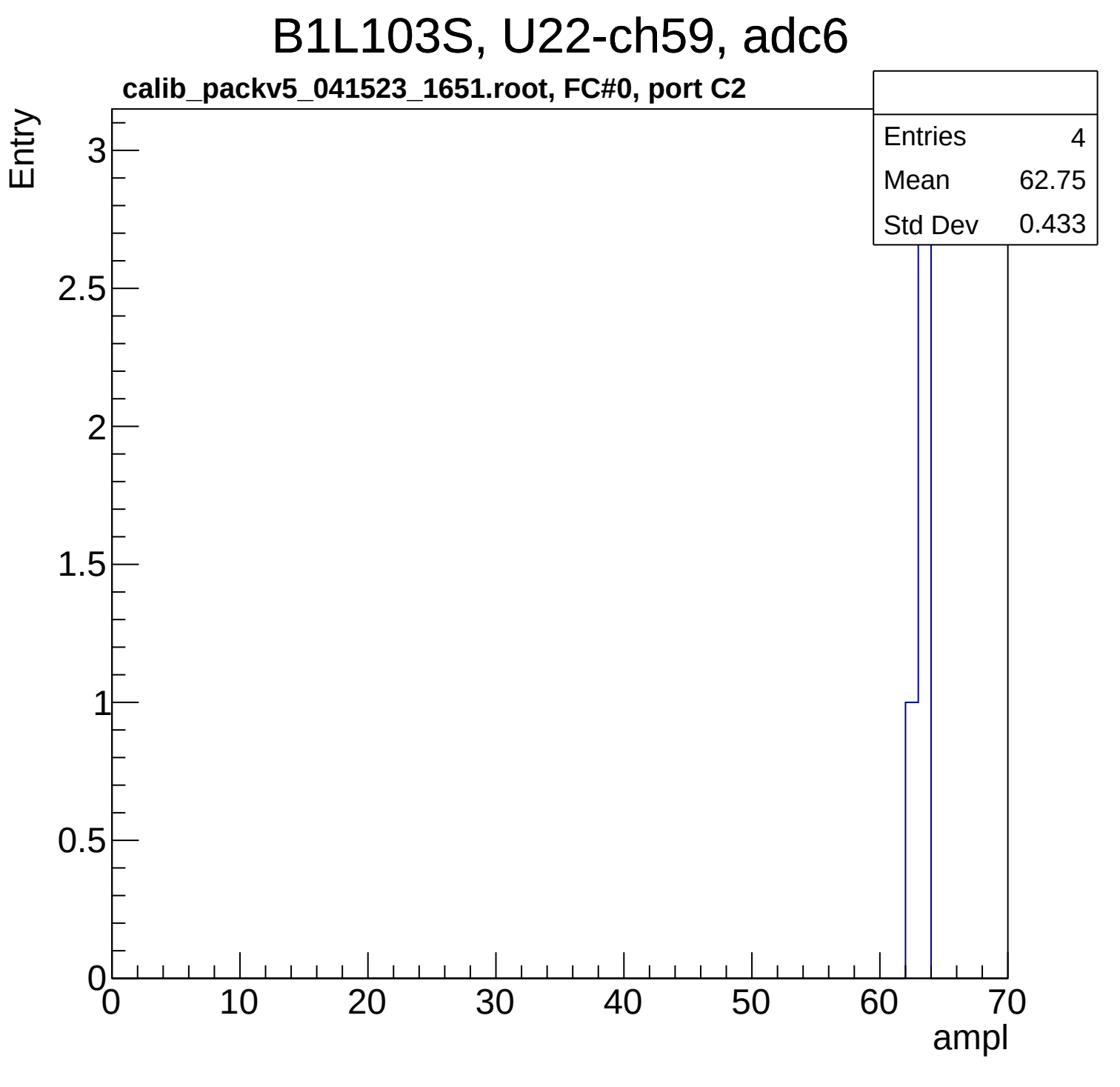
B1L103S, U22-ch59, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 62.75
Std Dev 0.433
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
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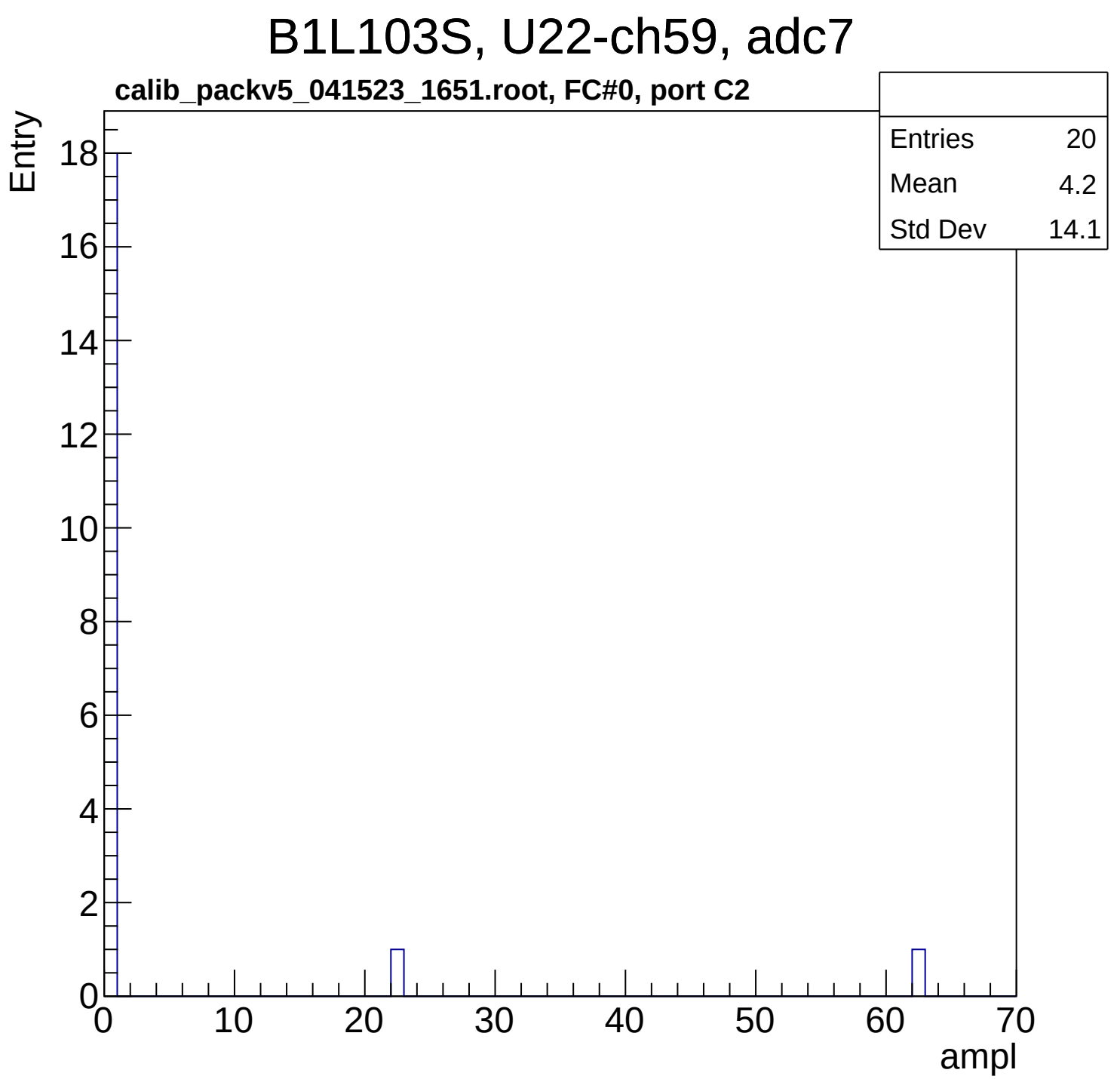
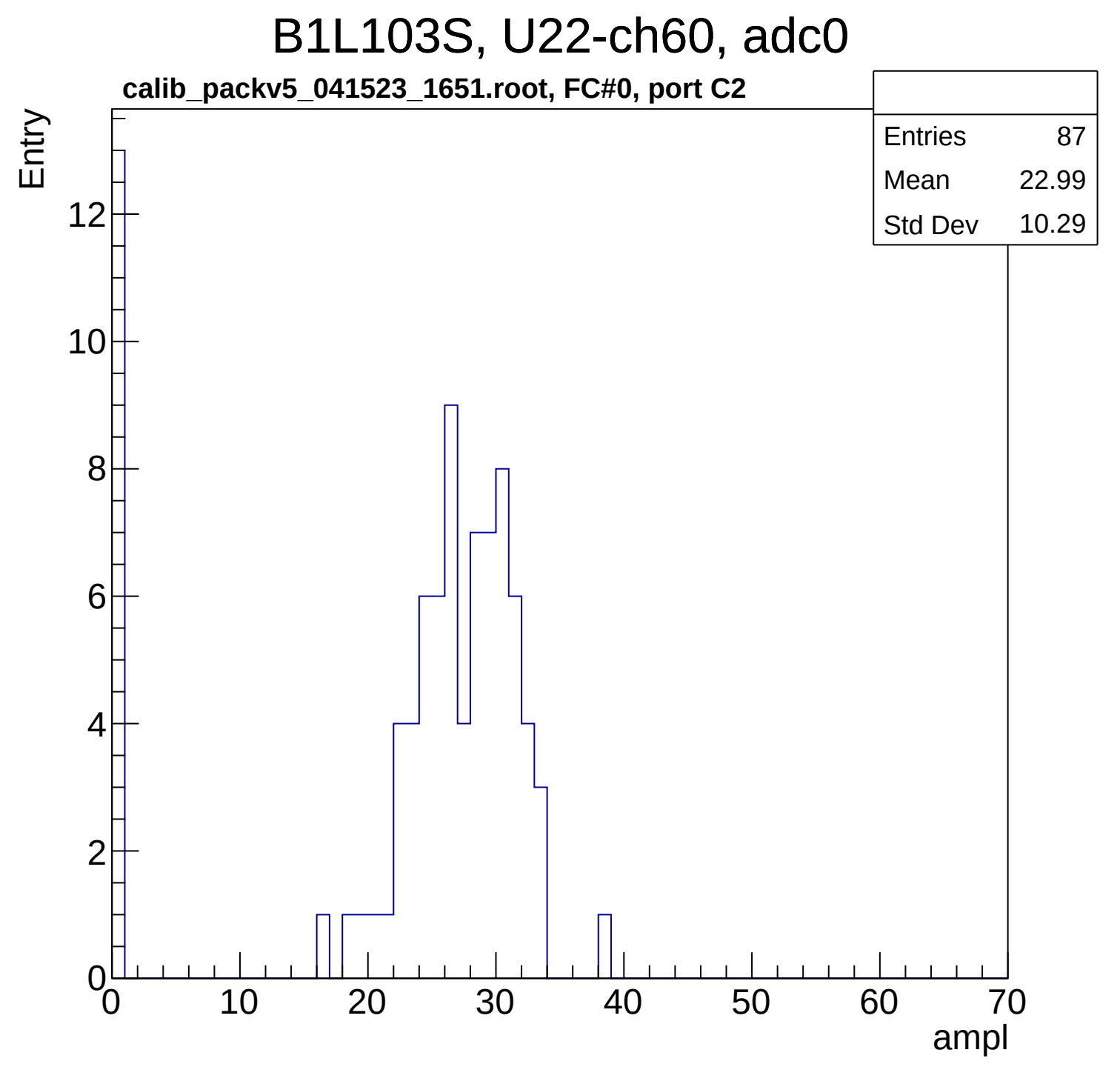
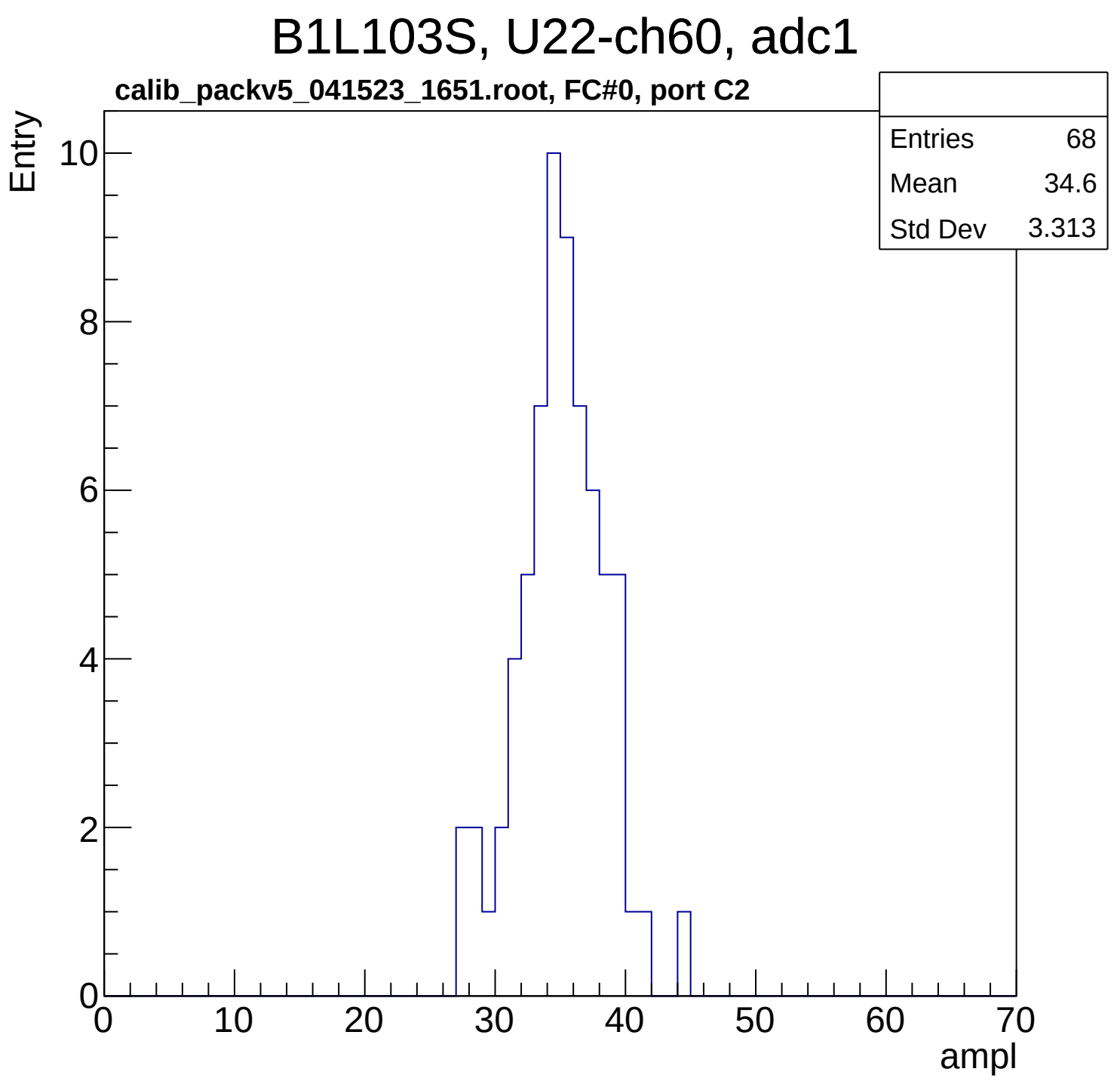
40
50
60
70


B1L103S, U22-ch59, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4.2
Std Dev 14.1
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch60, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 22.99
Std Dev 10.29
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch60, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 34.6
Std Dev 3.313
Entry
ampl
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2
4
6
8
10
0
10
20
30
40
50
60
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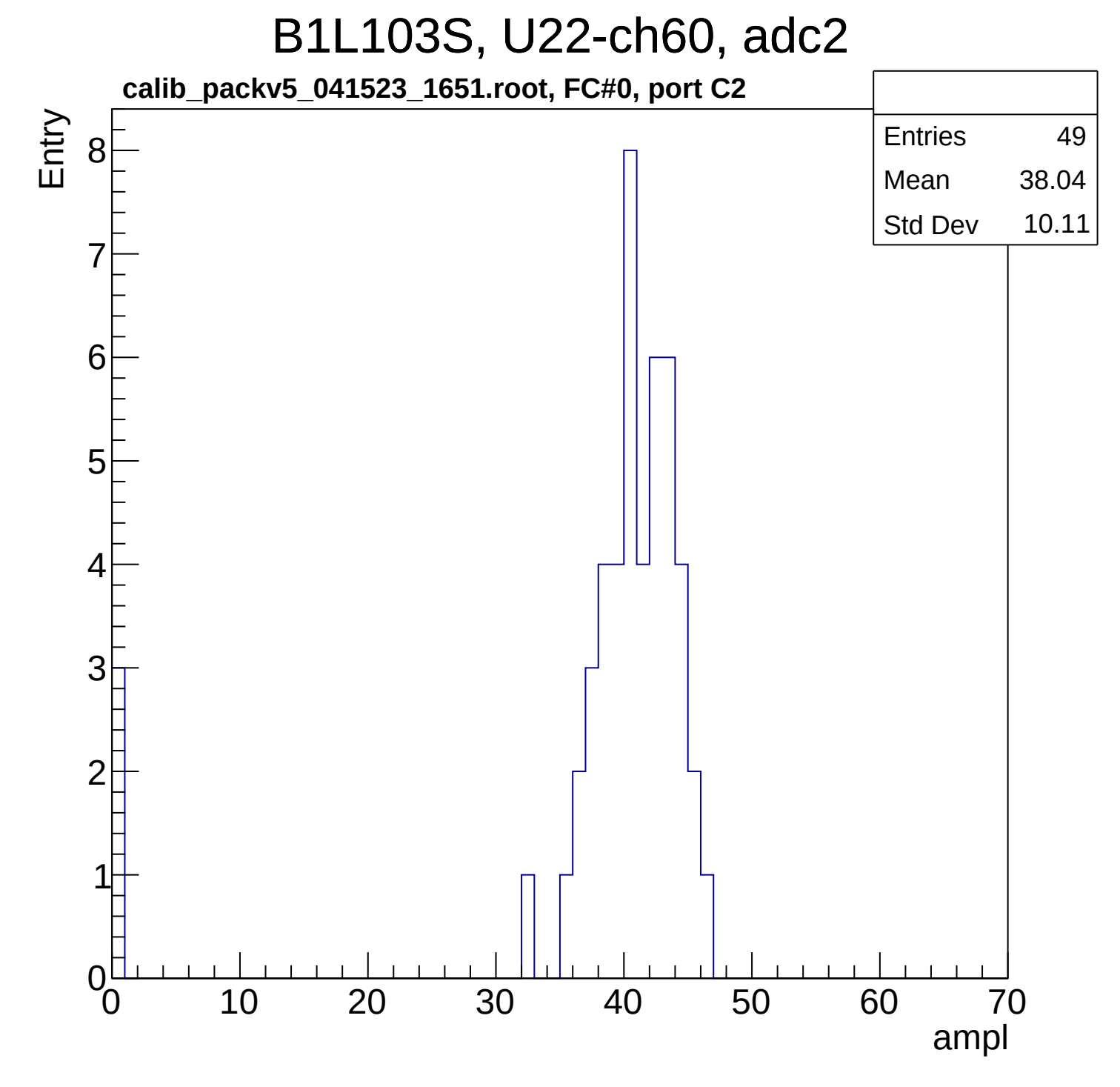
B1L103S, U22-ch60, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 38.04
Std Dev 10.11
Entry
ampl
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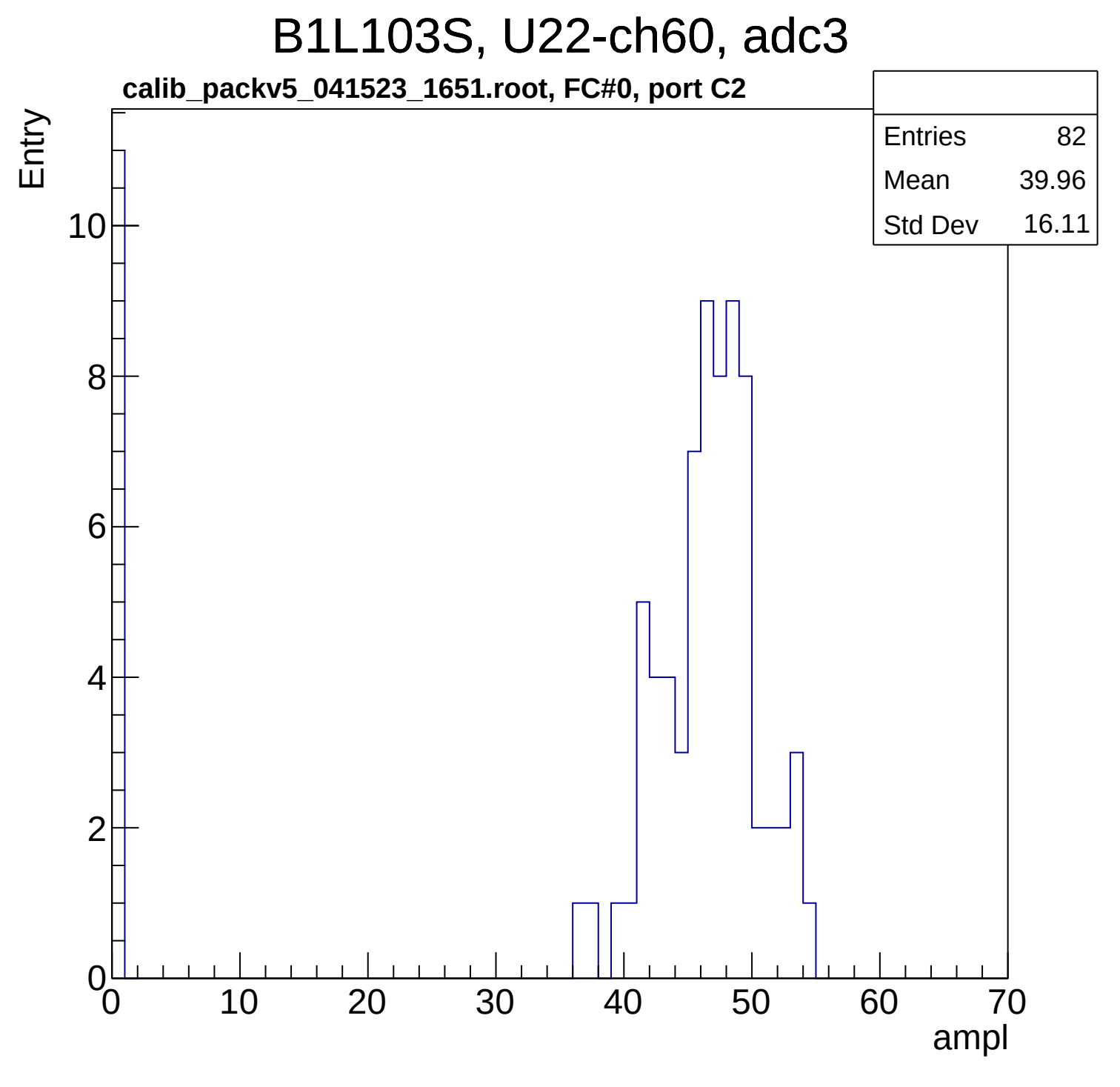
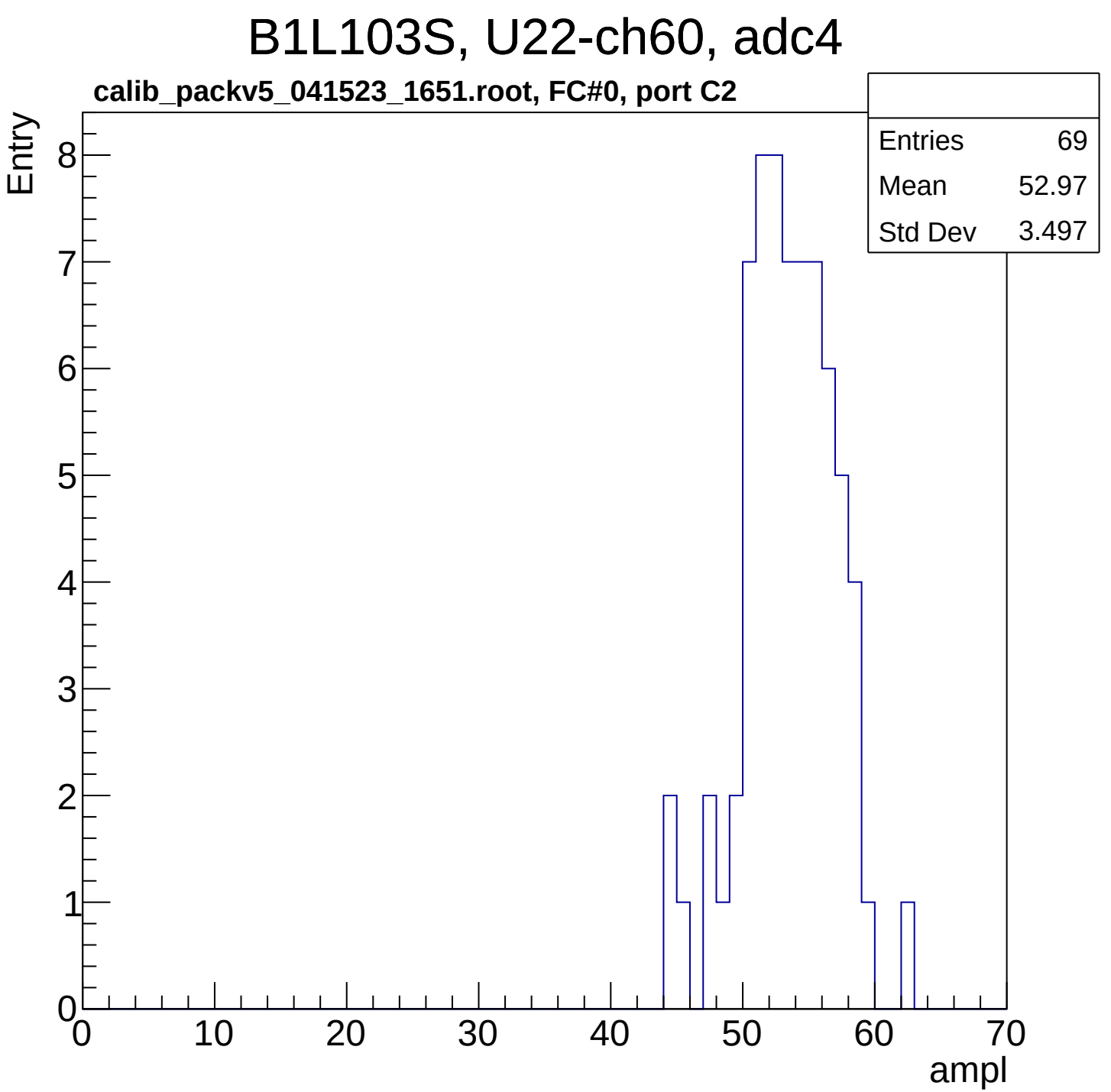
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch60, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 39.96
Std Dev 16.11
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch60, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 52.97
Std Dev 3.497
Entry
ampl
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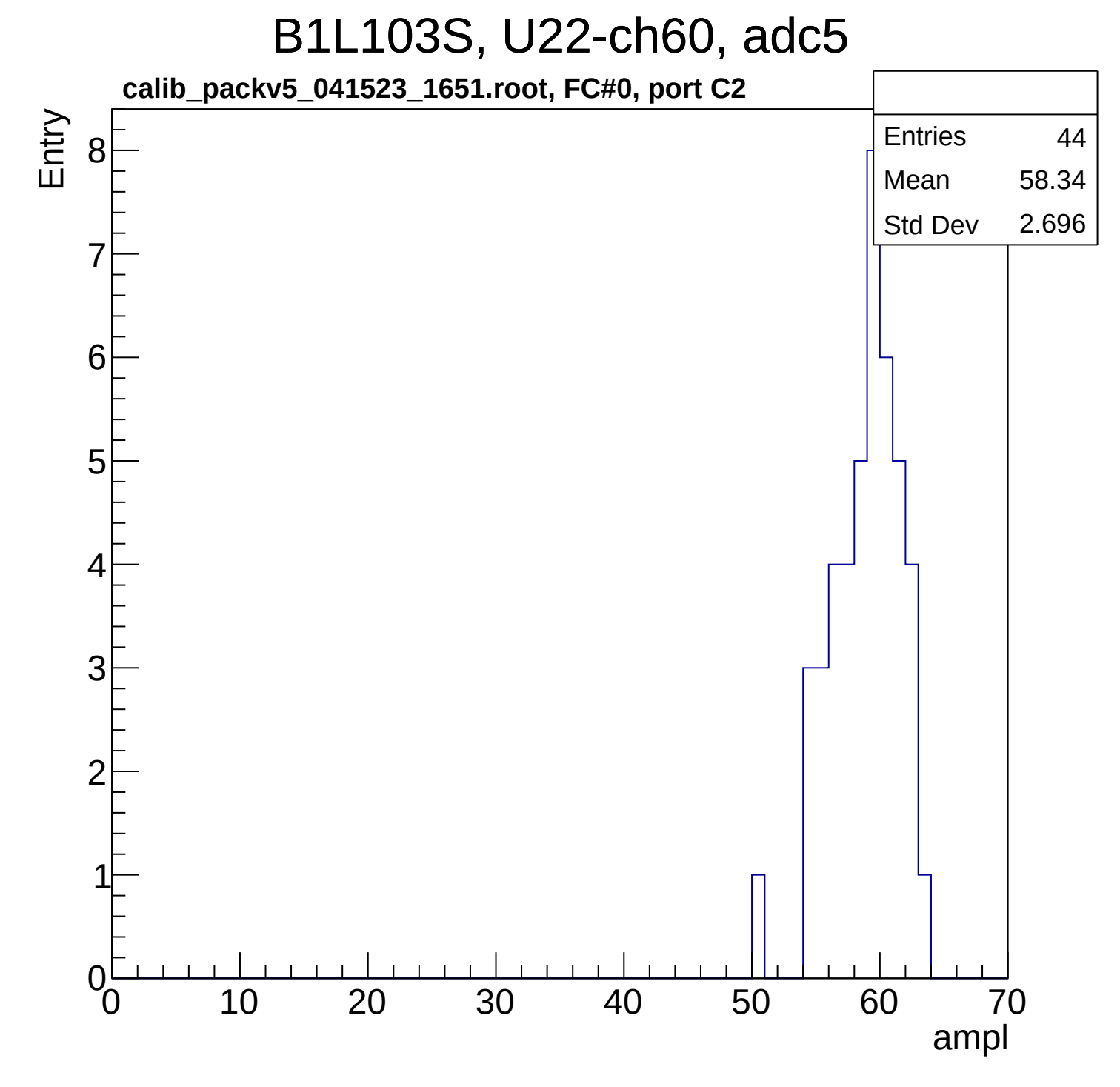
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch60, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 58.34
Std Dev 2.696
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
50
60
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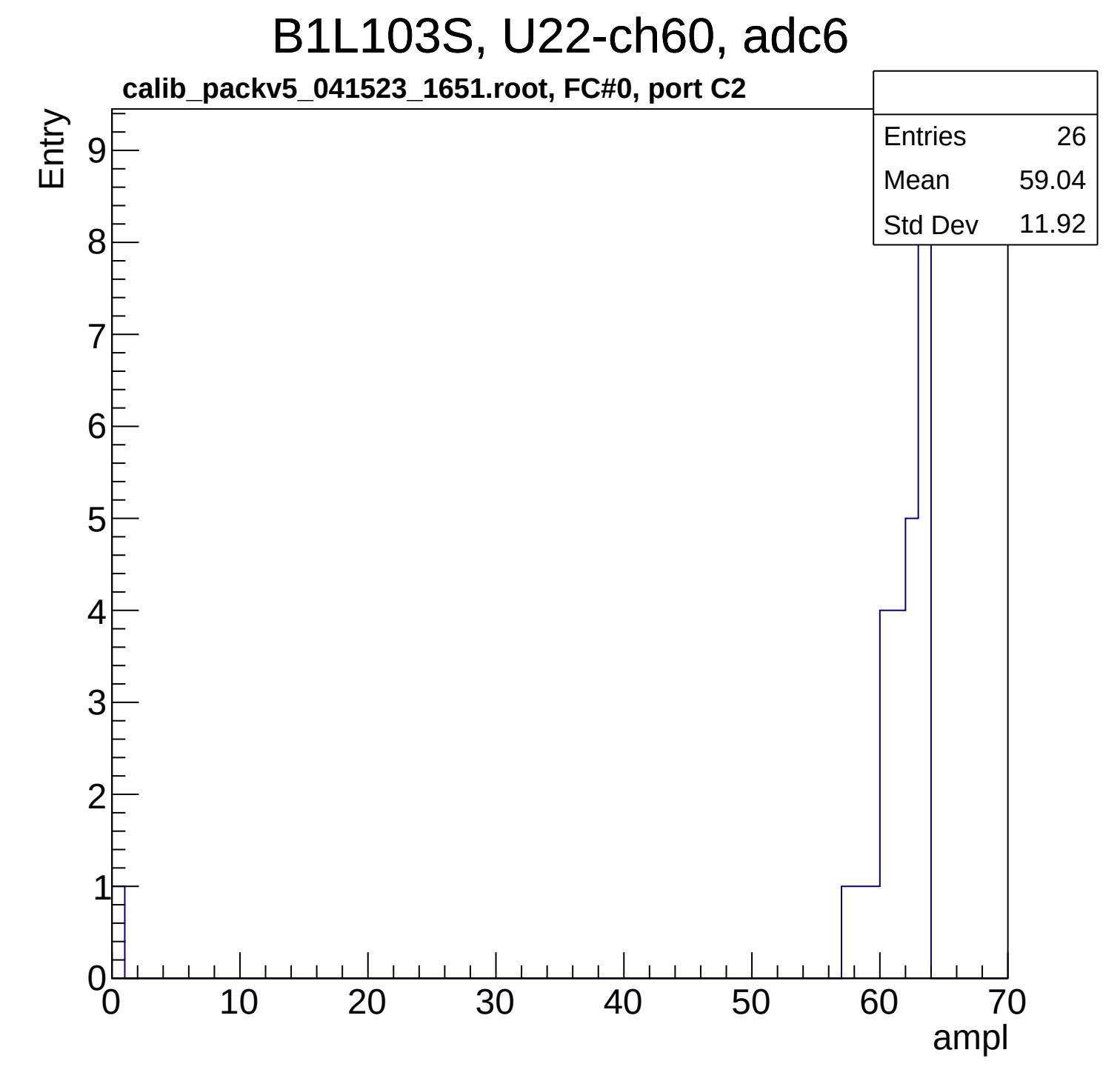
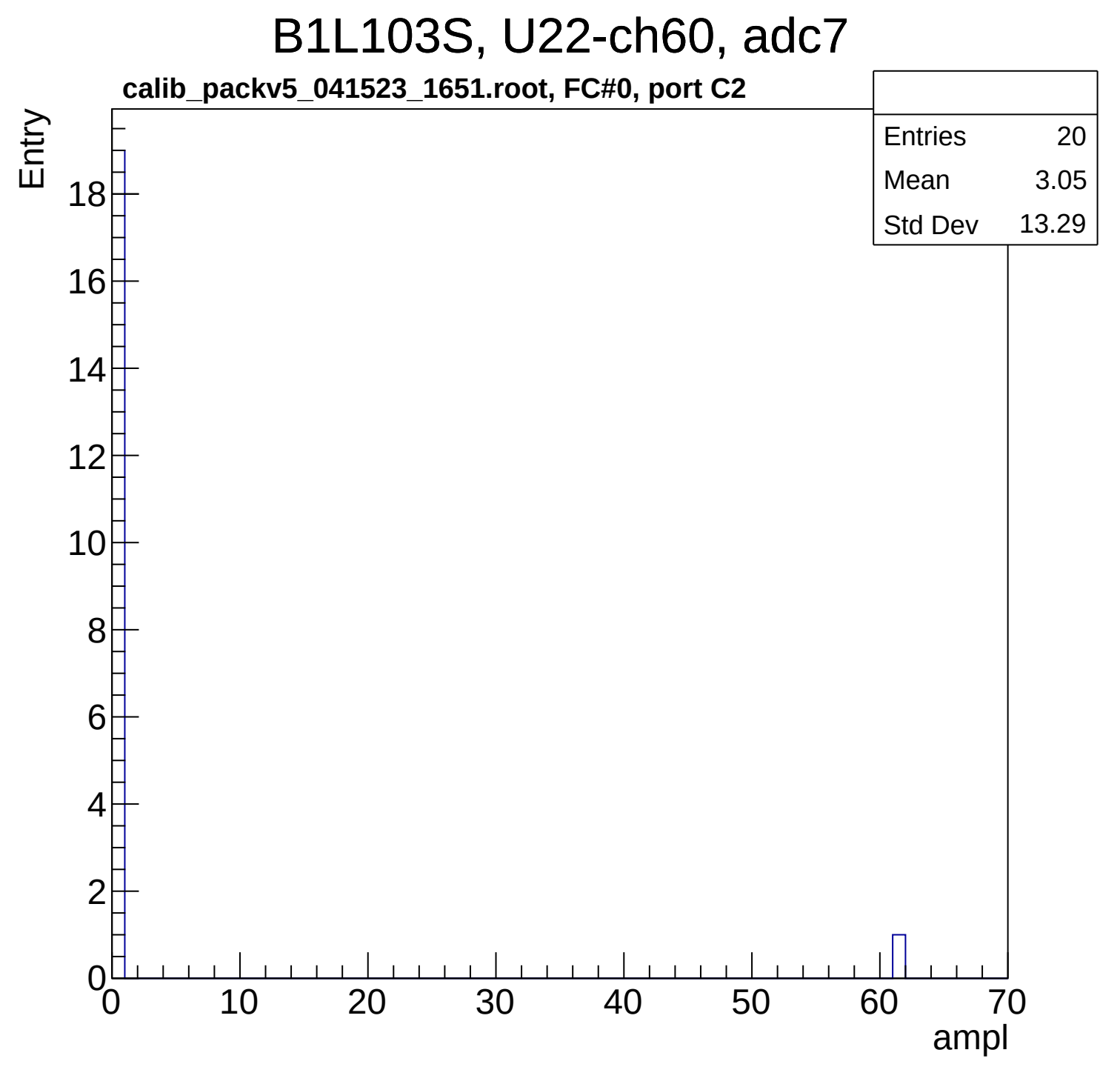
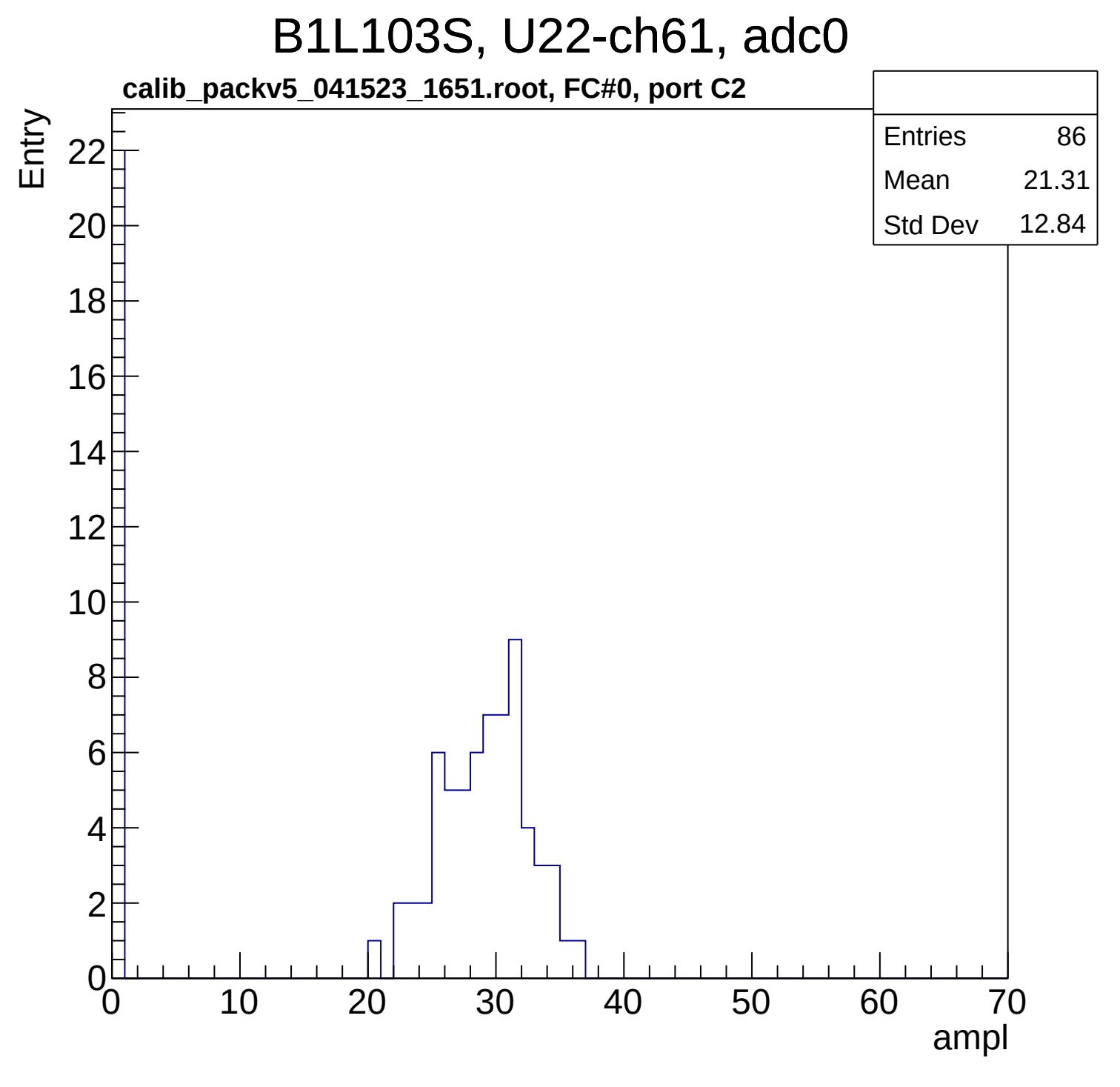
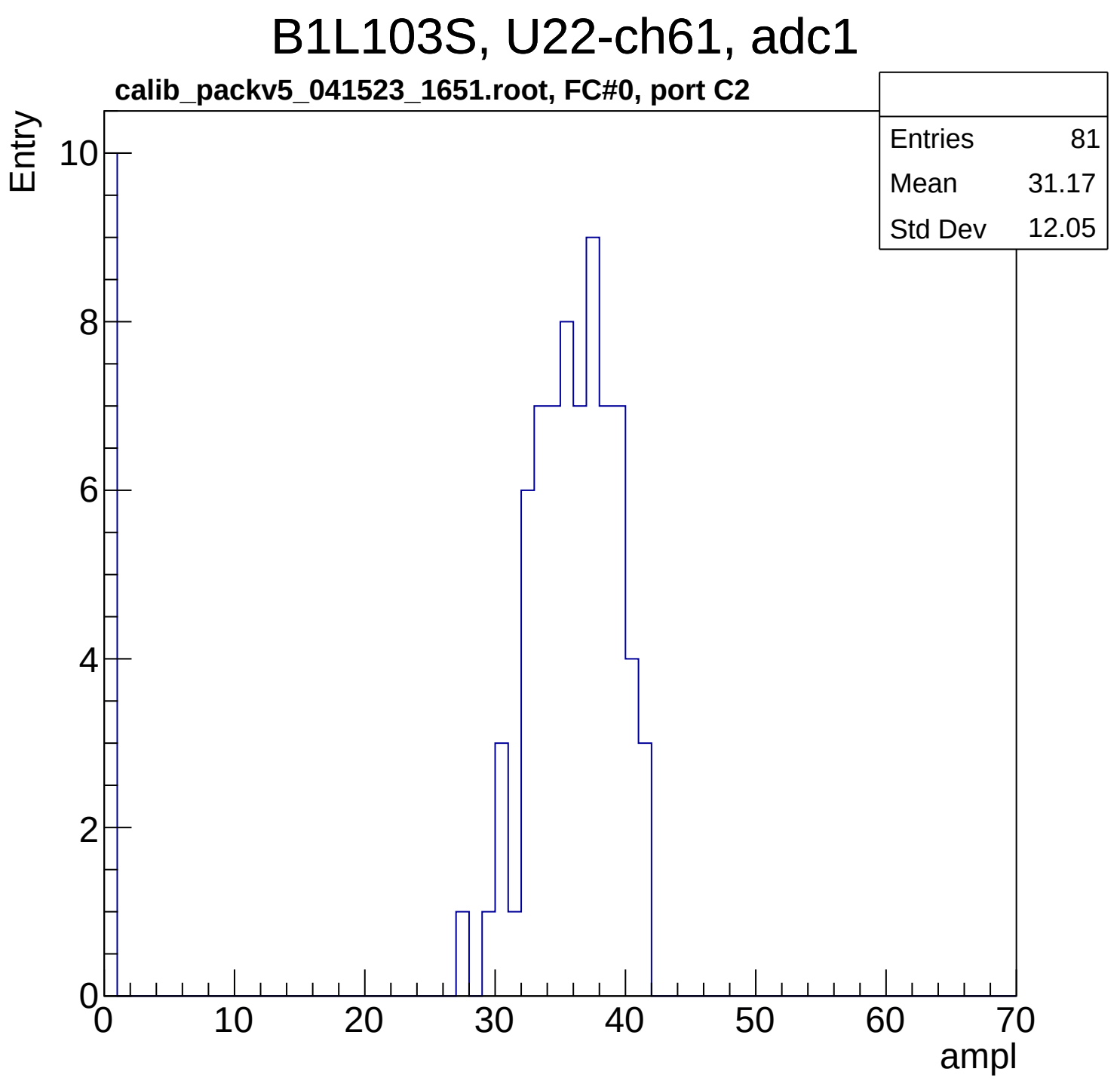
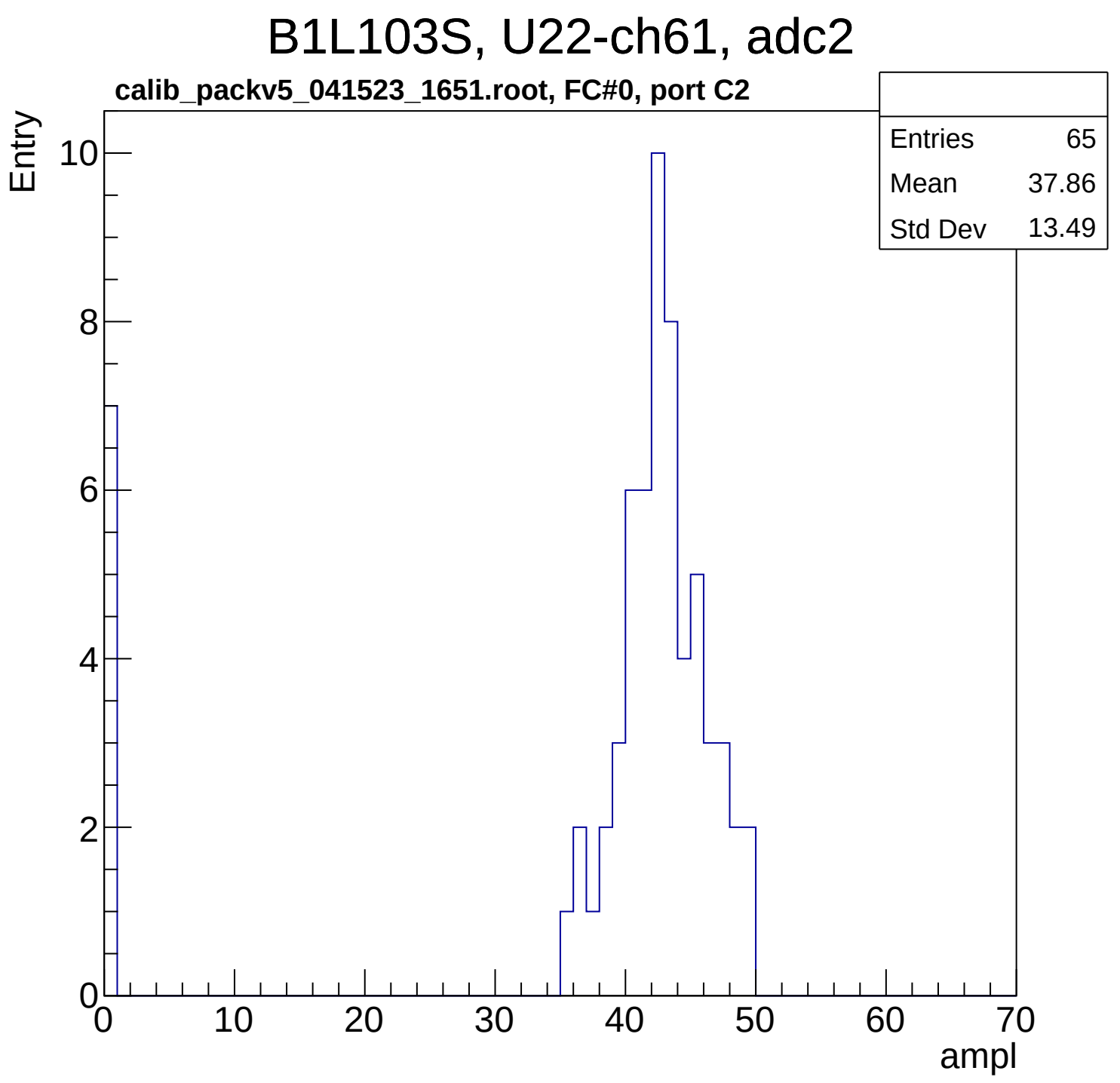
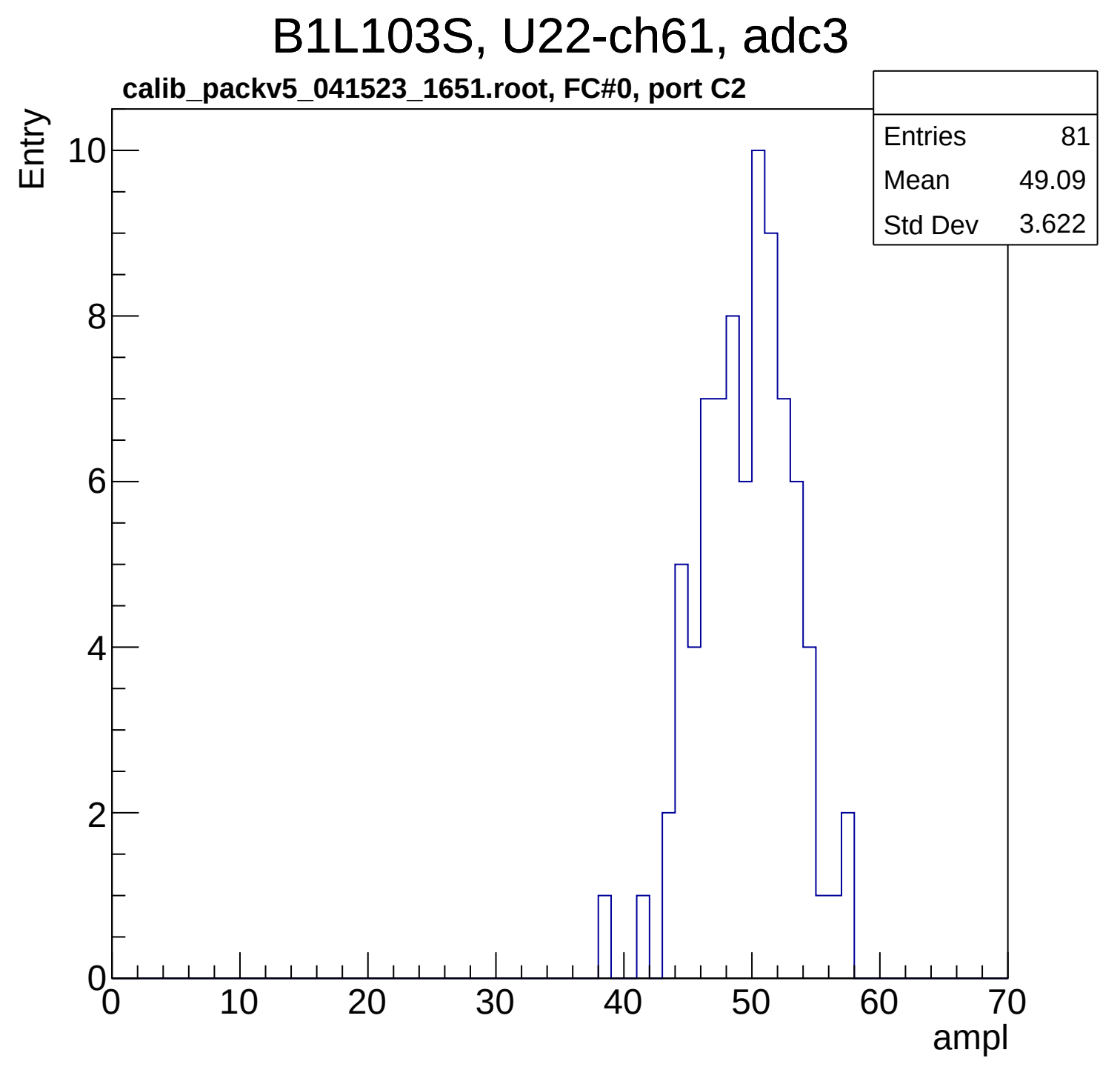

B1L103S, U22-ch60, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 59.04
Std Dev 11.92
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

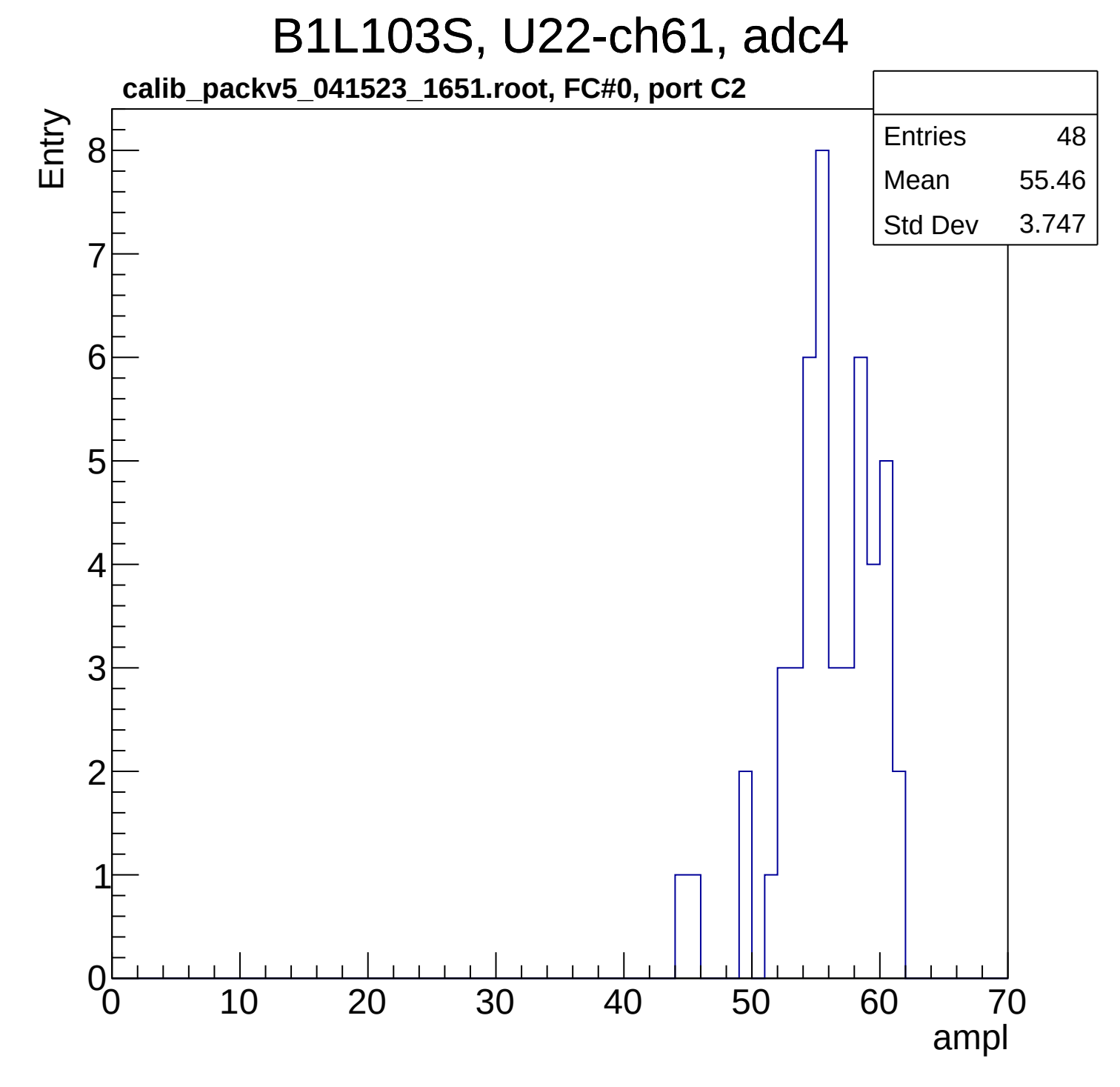

B1L103S, U22-ch60, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.05
Std Dev 13.29
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch61, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 21.31
Std Dev 12.84
Entry
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch61, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 31.17
Std Dev 12.05
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch61, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 37.86
Std Dev 13.49
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U22-ch61, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 49.09
Std Dev 3.622
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U22-ch61, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 55.46
Std Dev 3.747
Entry
ampl
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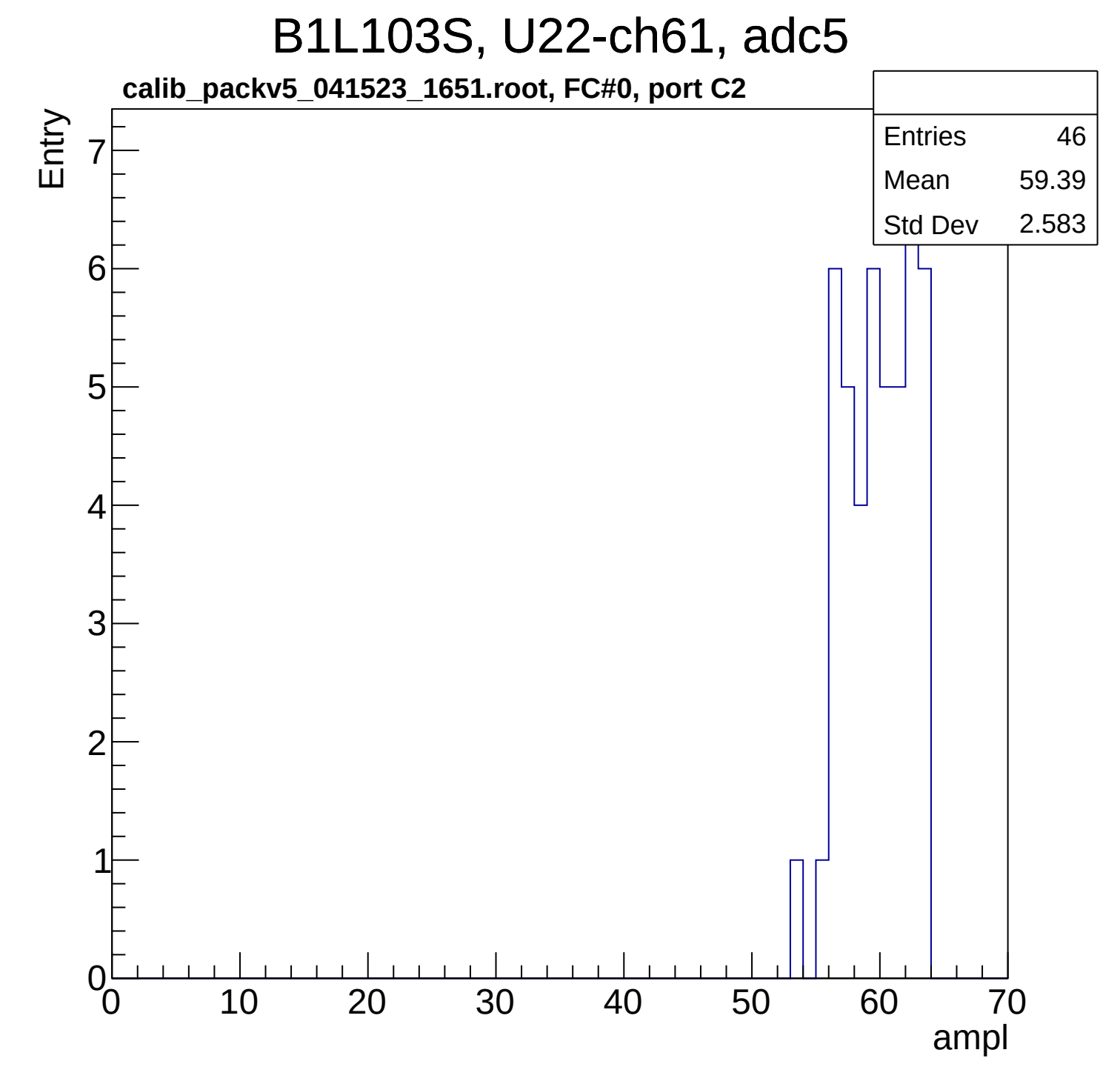
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch61, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 59.39
Std Dev 2.583
Entry
ampl
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1
2
3
4
5
6
7
0
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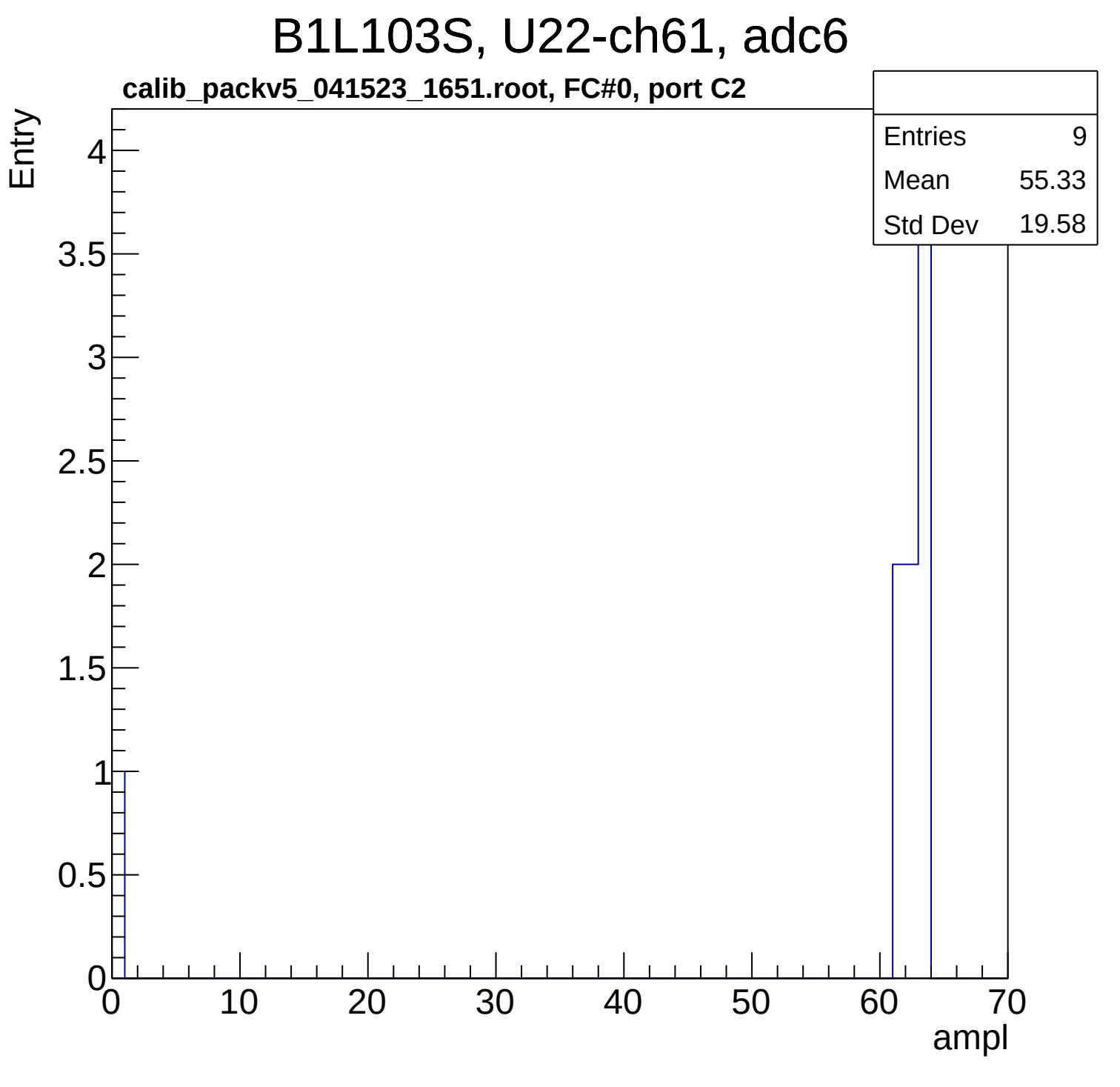
20
30
40
50
60
70


B1L103S, U22-ch61, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 55.33
Std Dev 19.58
Entry
ampl
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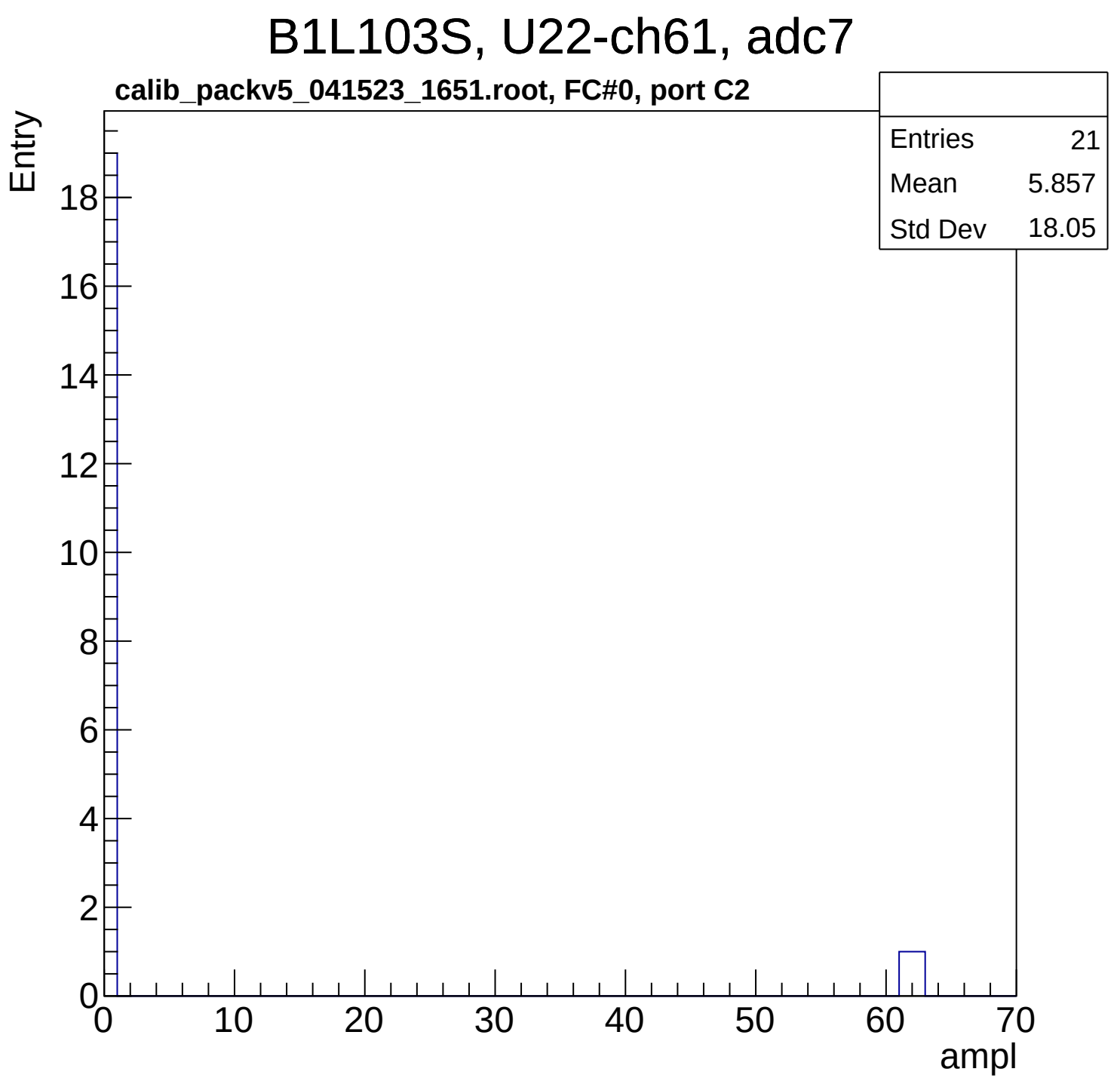
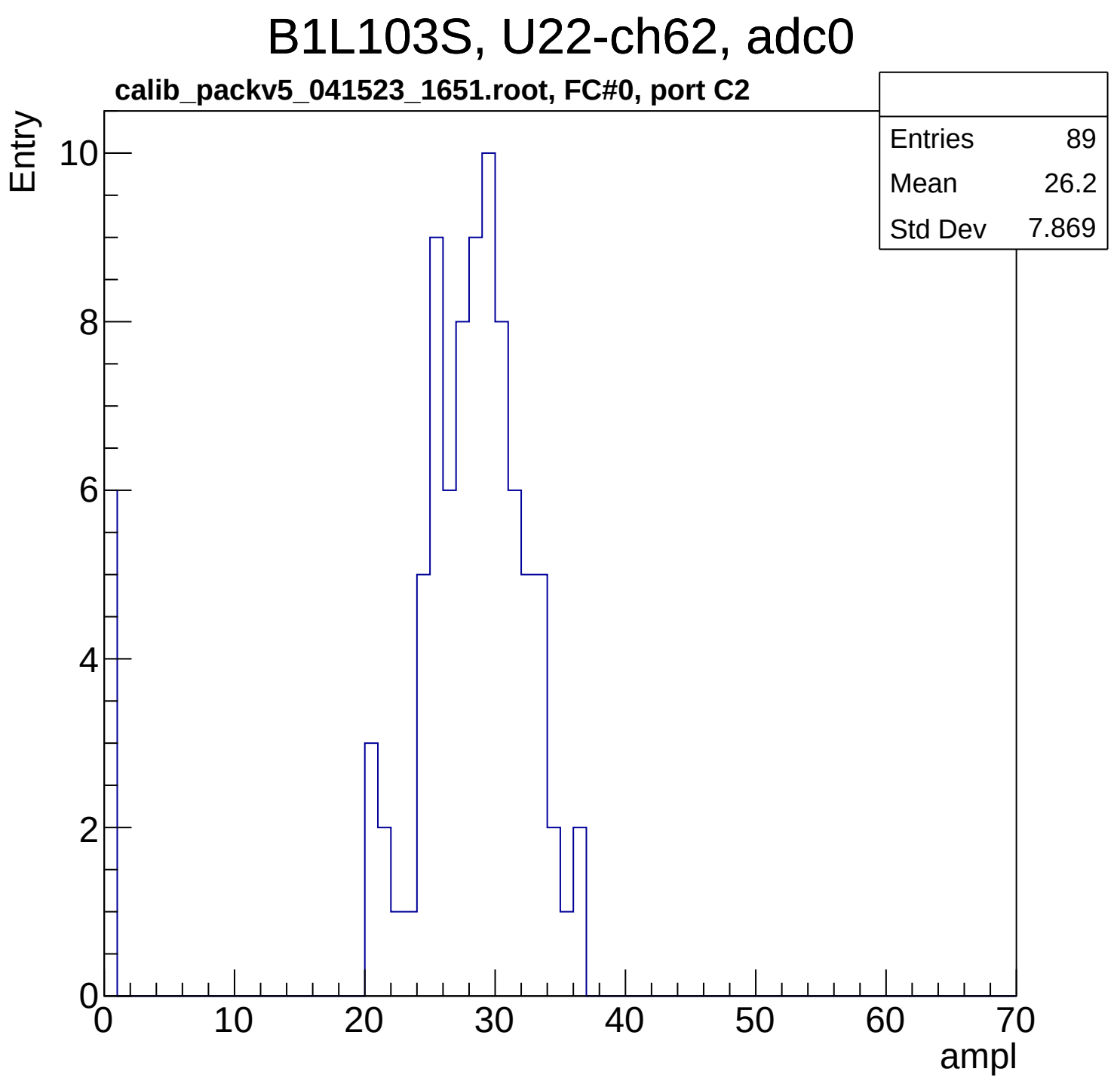
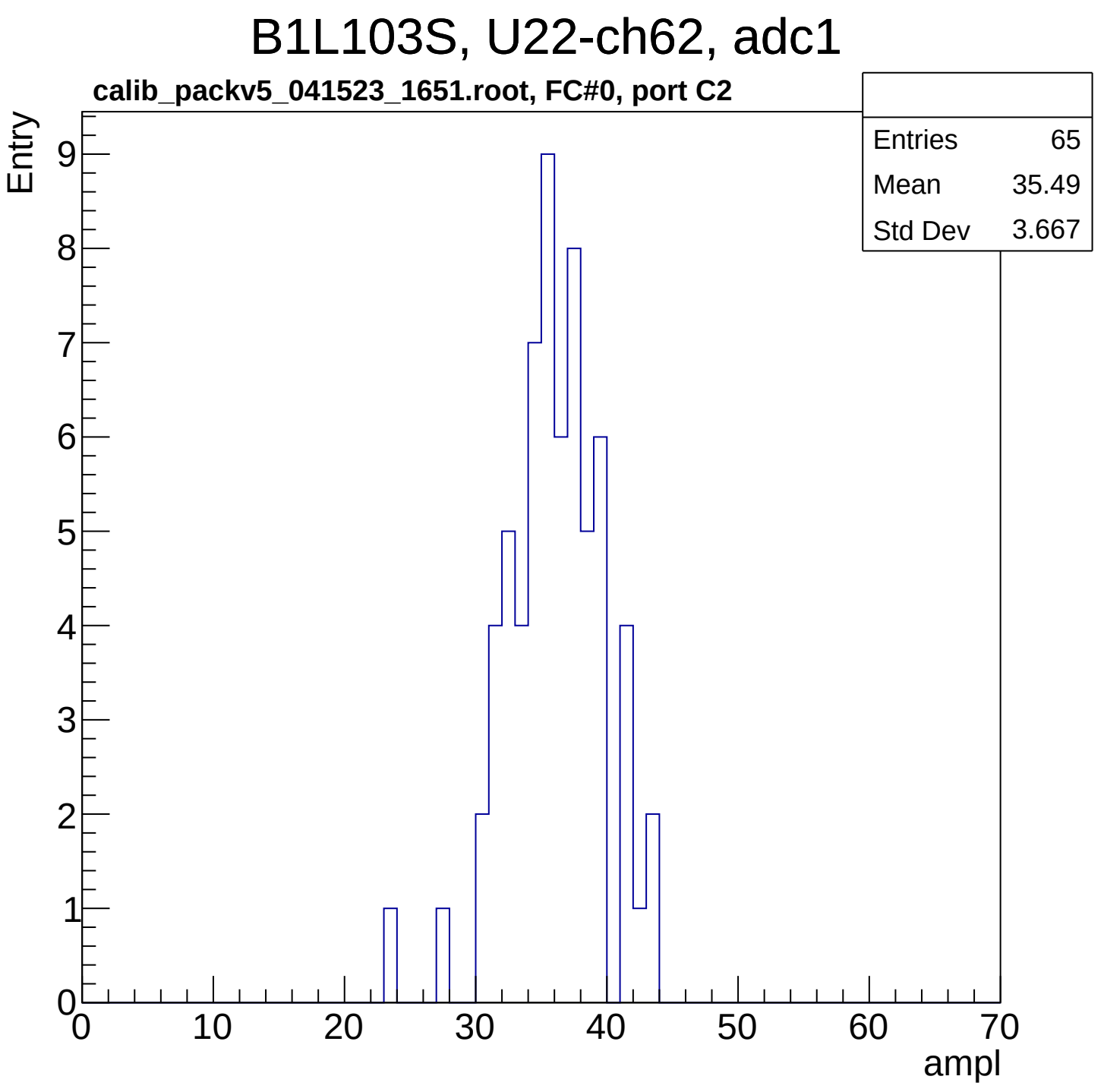
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U22-ch61, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.857
Std Dev 18.05
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch62, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 26.2
Std Dev 7.869
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch62, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 35.49
Std Dev 3.667
Entry
ampl
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2
3
4
5
6
7
8
9
0
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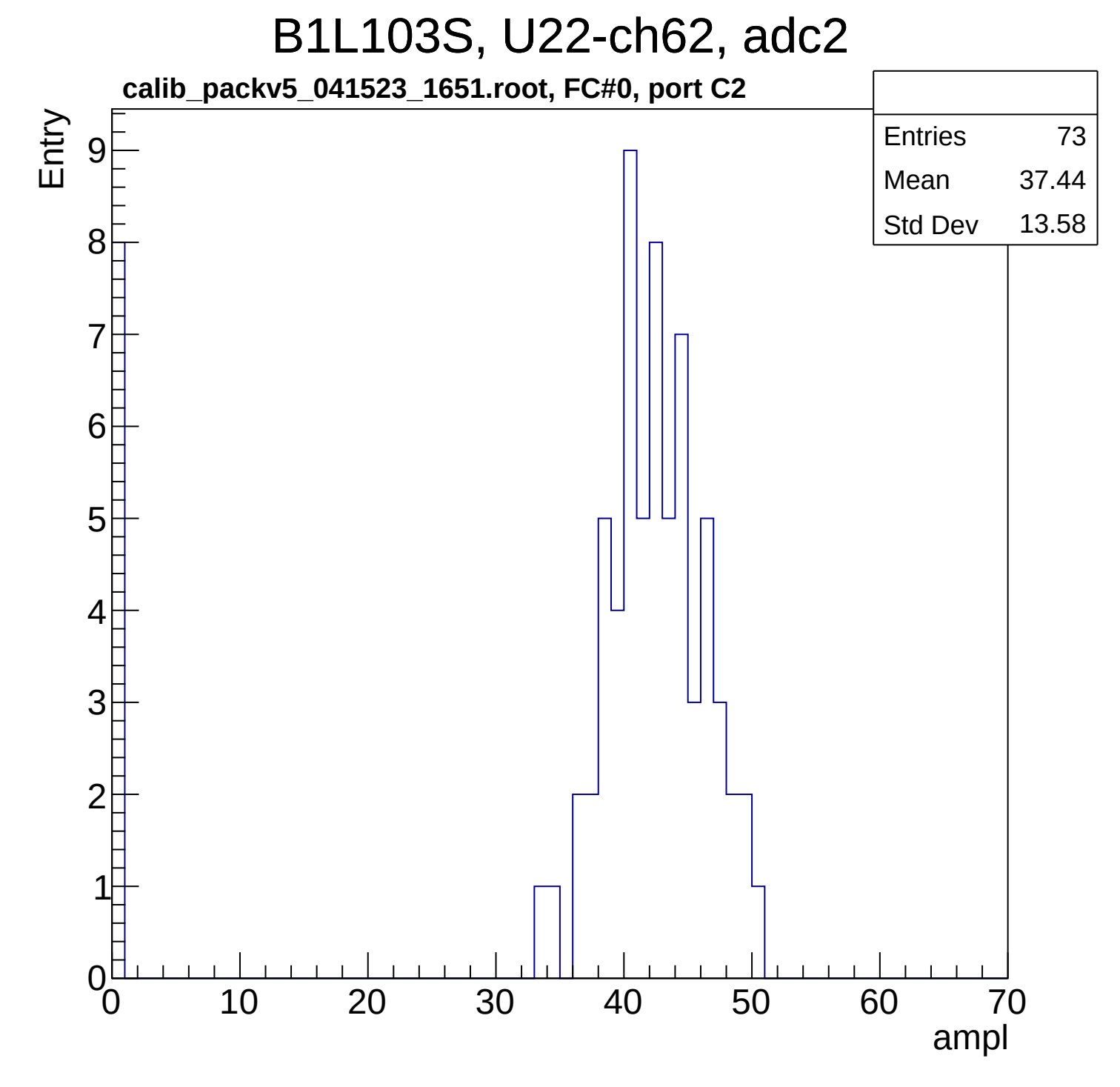
20
30
40
50
60
70


B1L103S, U22-ch62, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 37.44
Std Dev 13.58
Entry
ampl
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2
3
4
5
6
7
8
9
0
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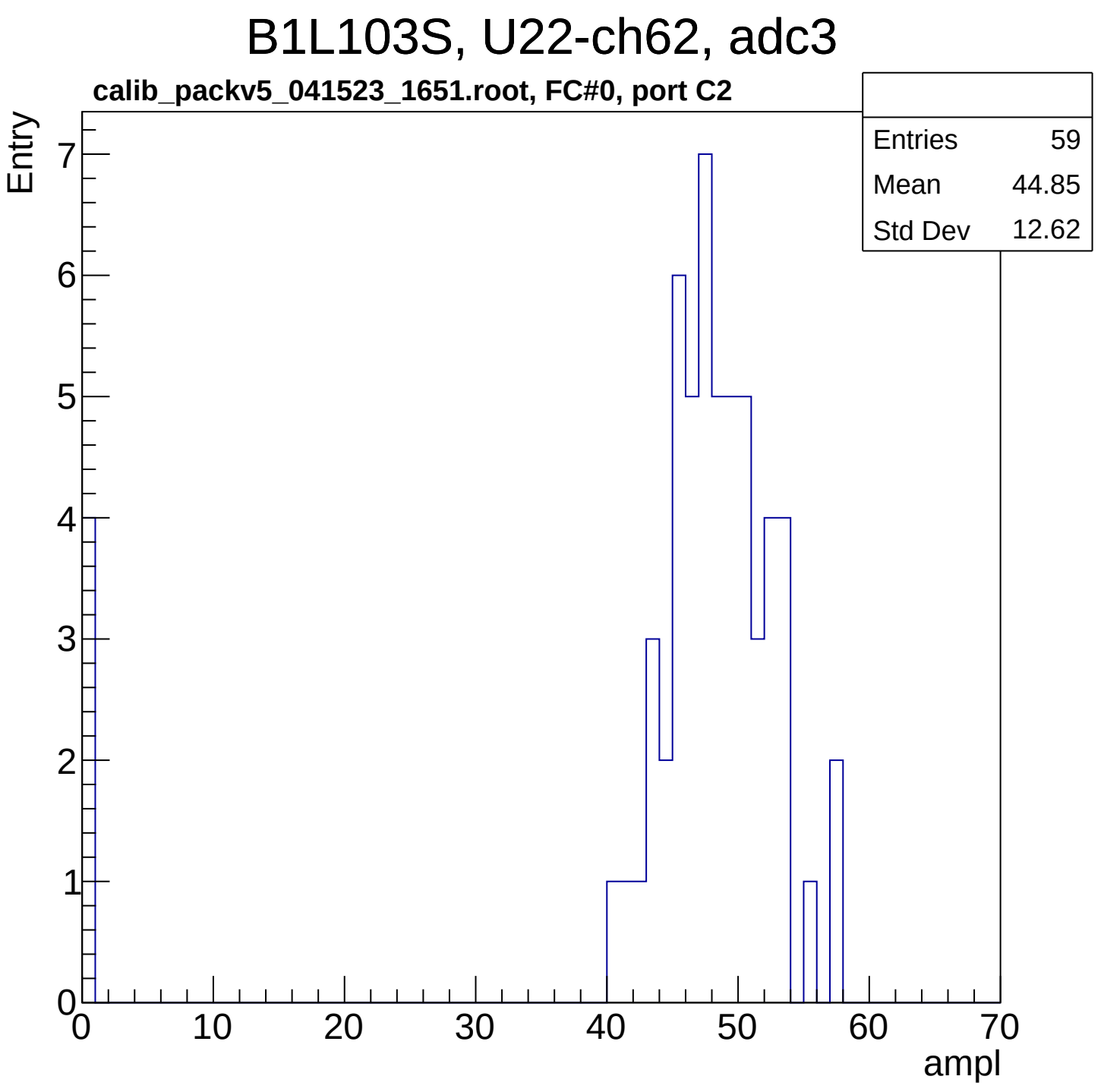
20
30
40
50
60
70


B1L103S, U22-ch62, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 44.85
Std Dev 12.62
Entry
ampl
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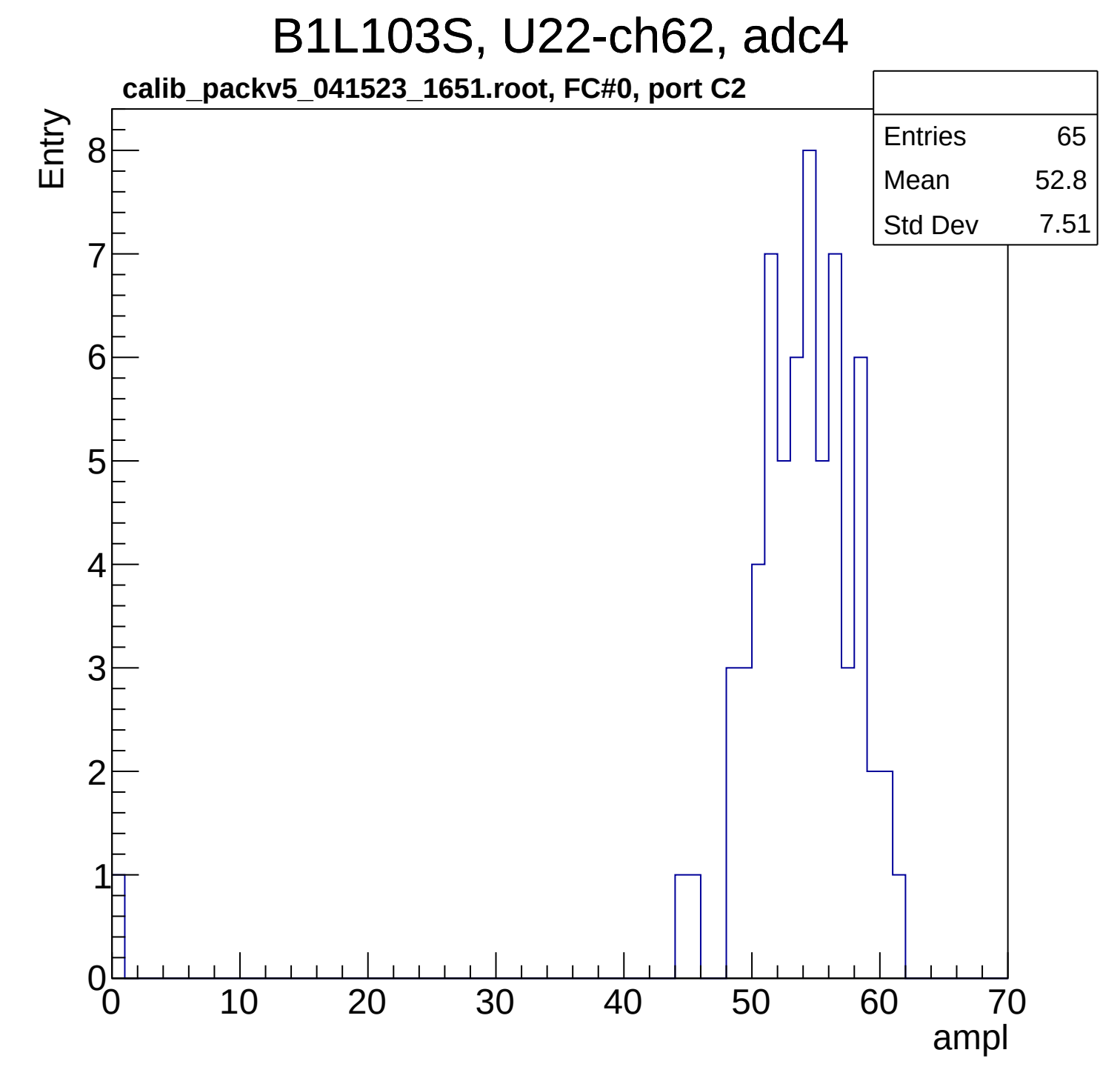
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U22-ch62, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 52.8
Std Dev 7.51
Entry
ampl
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2
3
4
5
6
7
8
0
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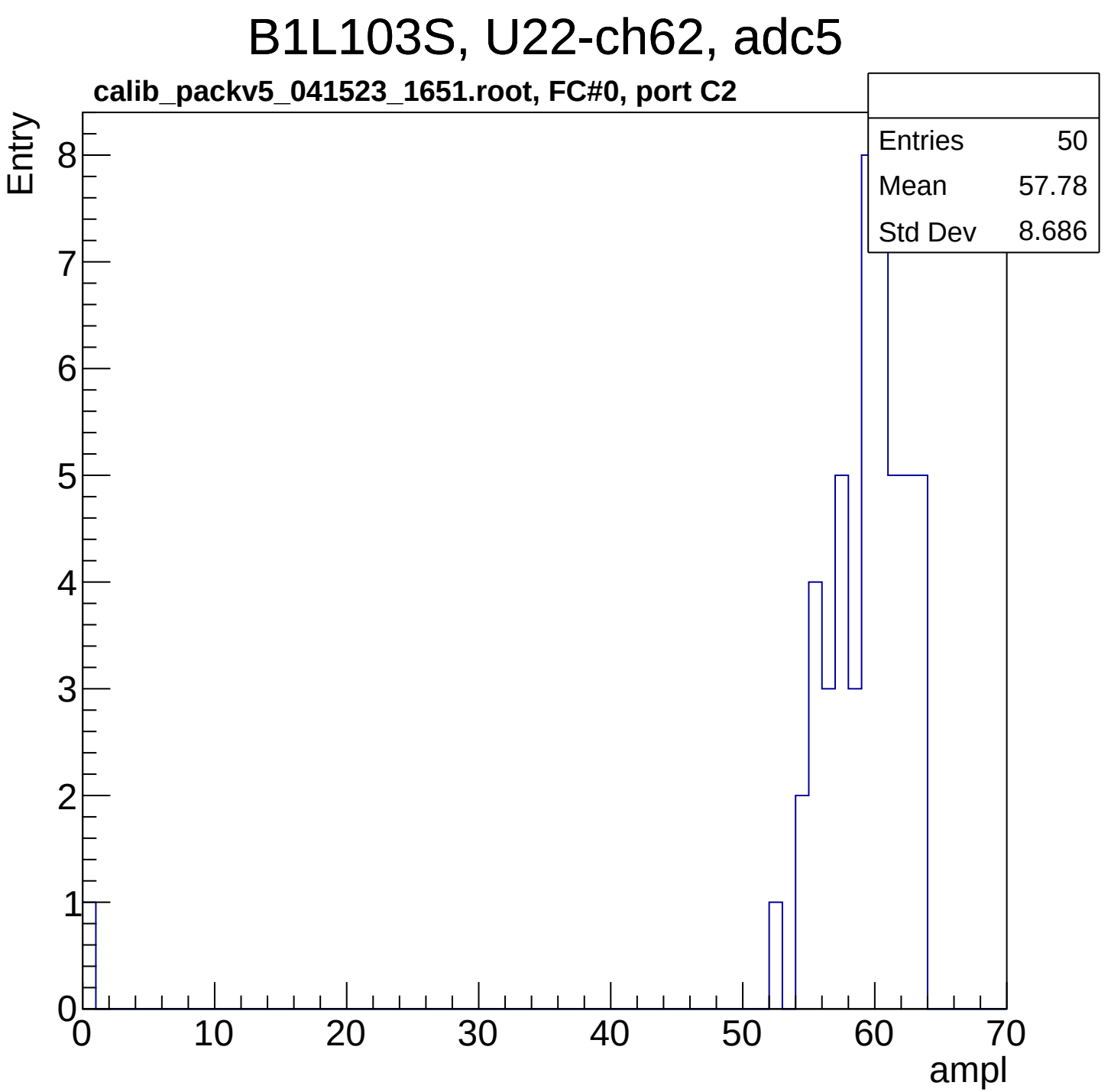
20
30
40
50
60
70


B1L103S, U22-ch62, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 57.78
Std Dev 8.686
Entry
ampl
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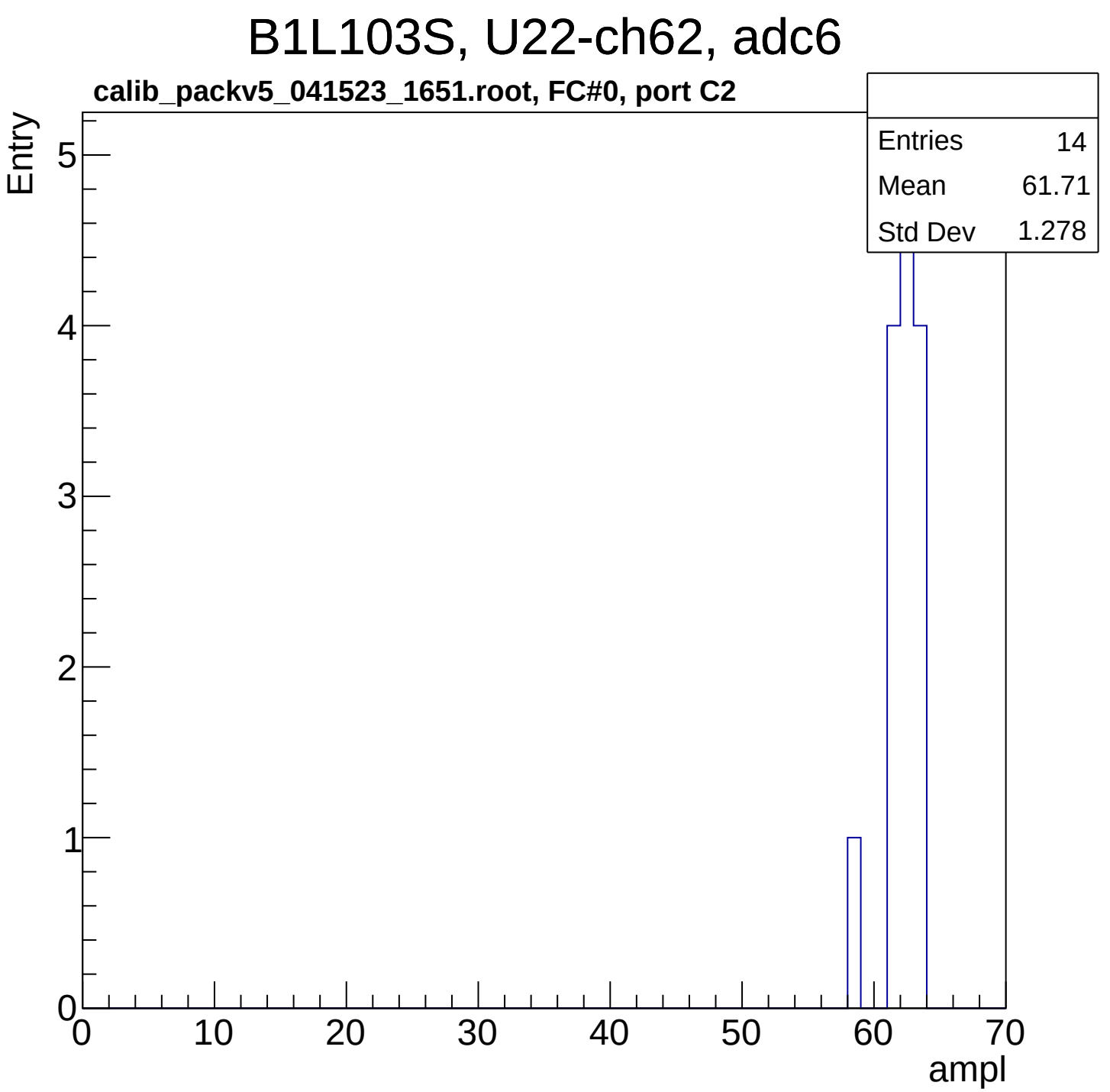
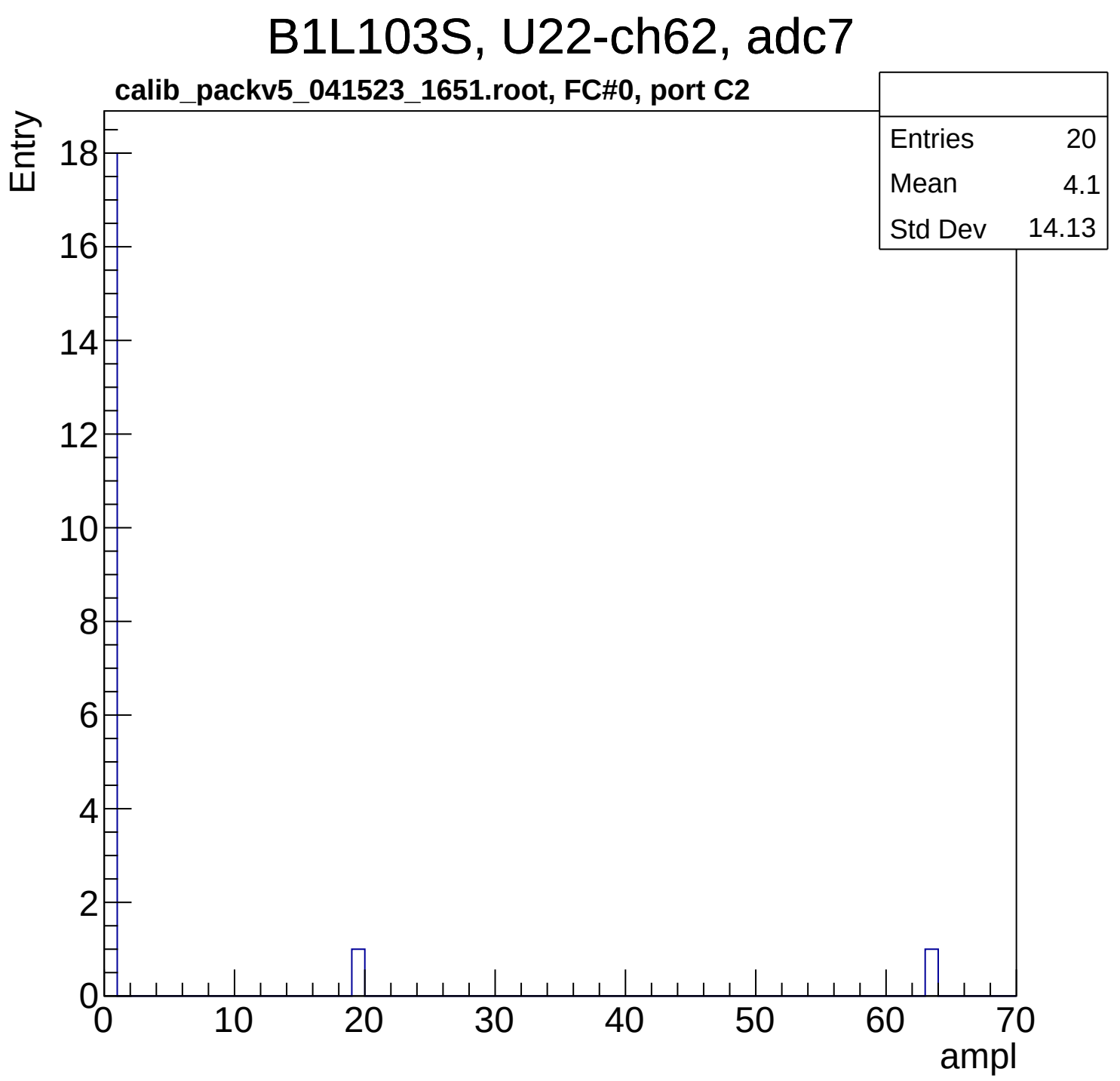
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch62, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 61.71
Std Dev 1.278
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch62, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4.1
Std Dev 14.13
Entry
0
2
4
6
8
10
12
14
16
18
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10
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30
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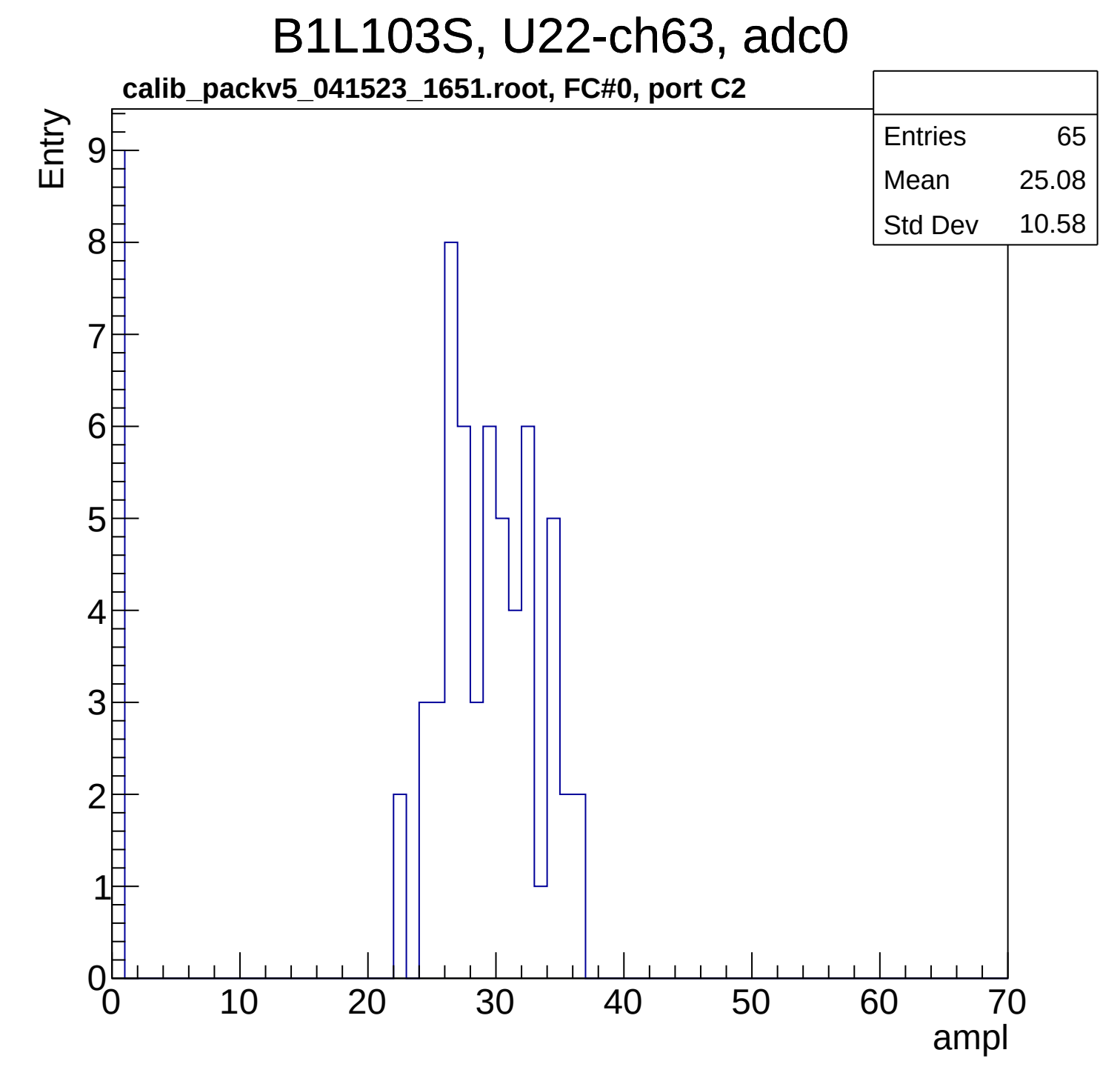
50
60
70
ampl


B1L103S, U22-ch63, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 25.08
Std Dev 10.58
Entry
ampl
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2
3
4
5
6
7
8
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0
10
20
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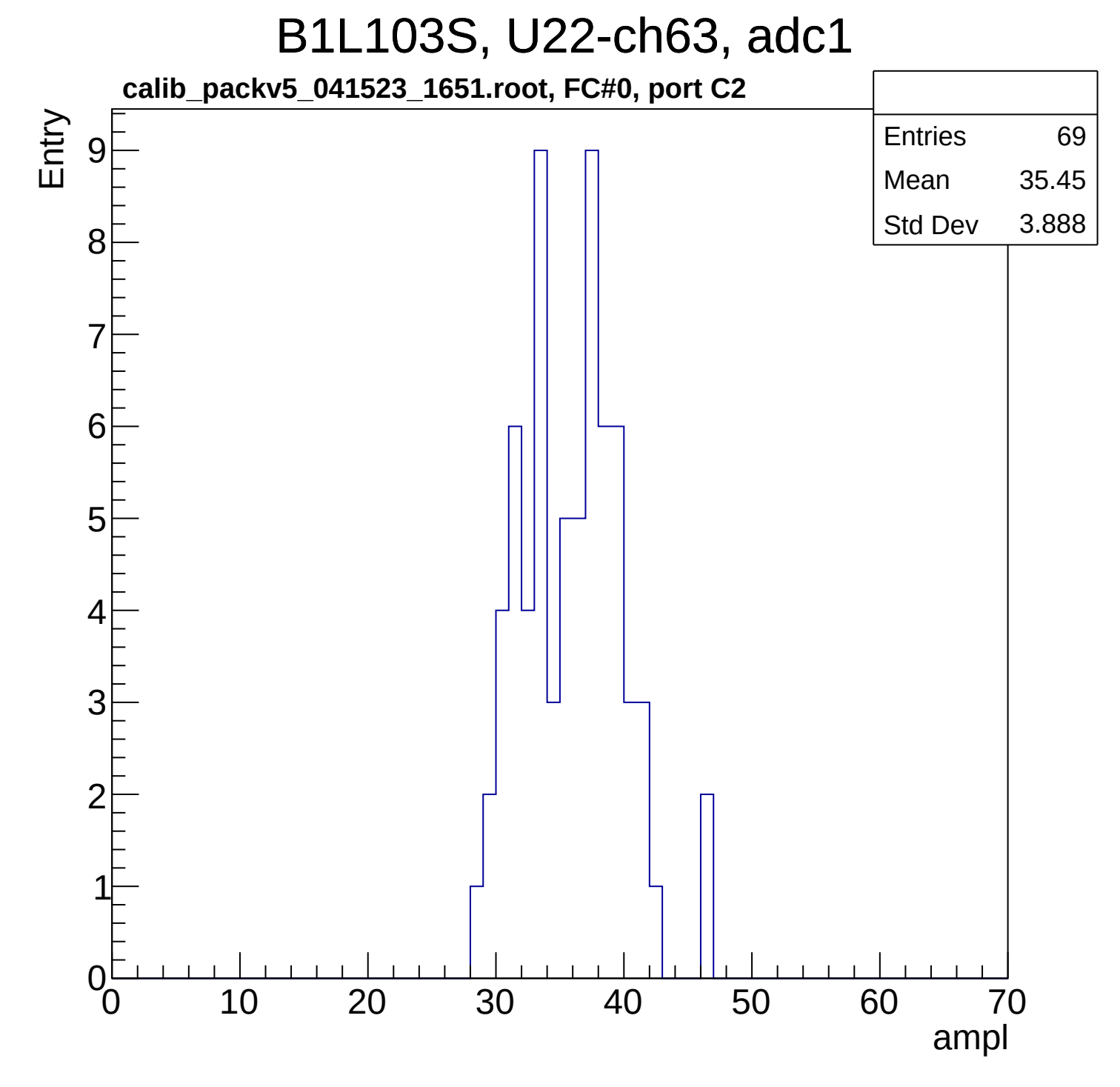
60
70


B1L103S, U22-ch63, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 35.45
Std Dev 3.888
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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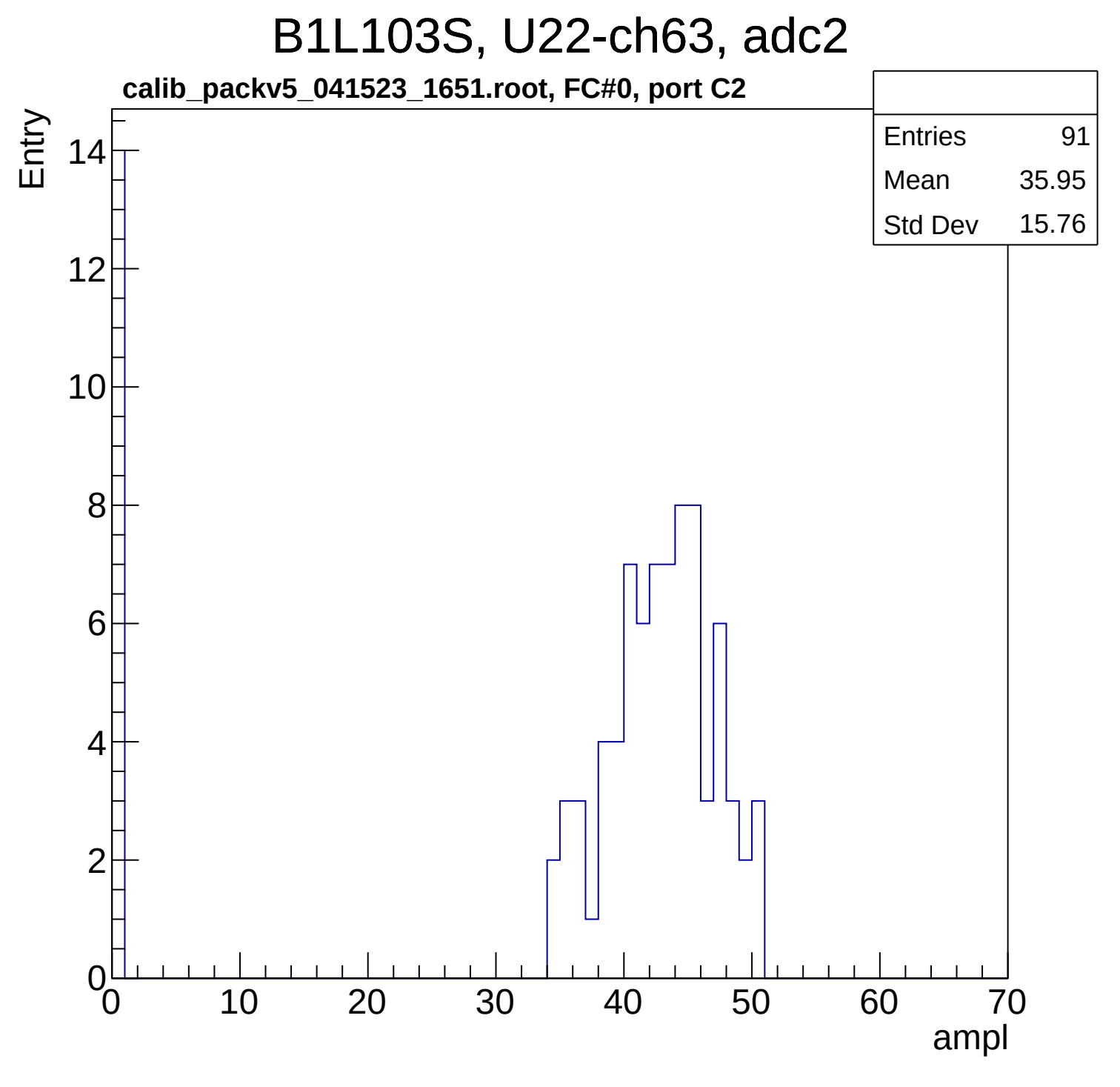
B1L103S, U22-ch63, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 35.95
Std Dev 15.76
Entry
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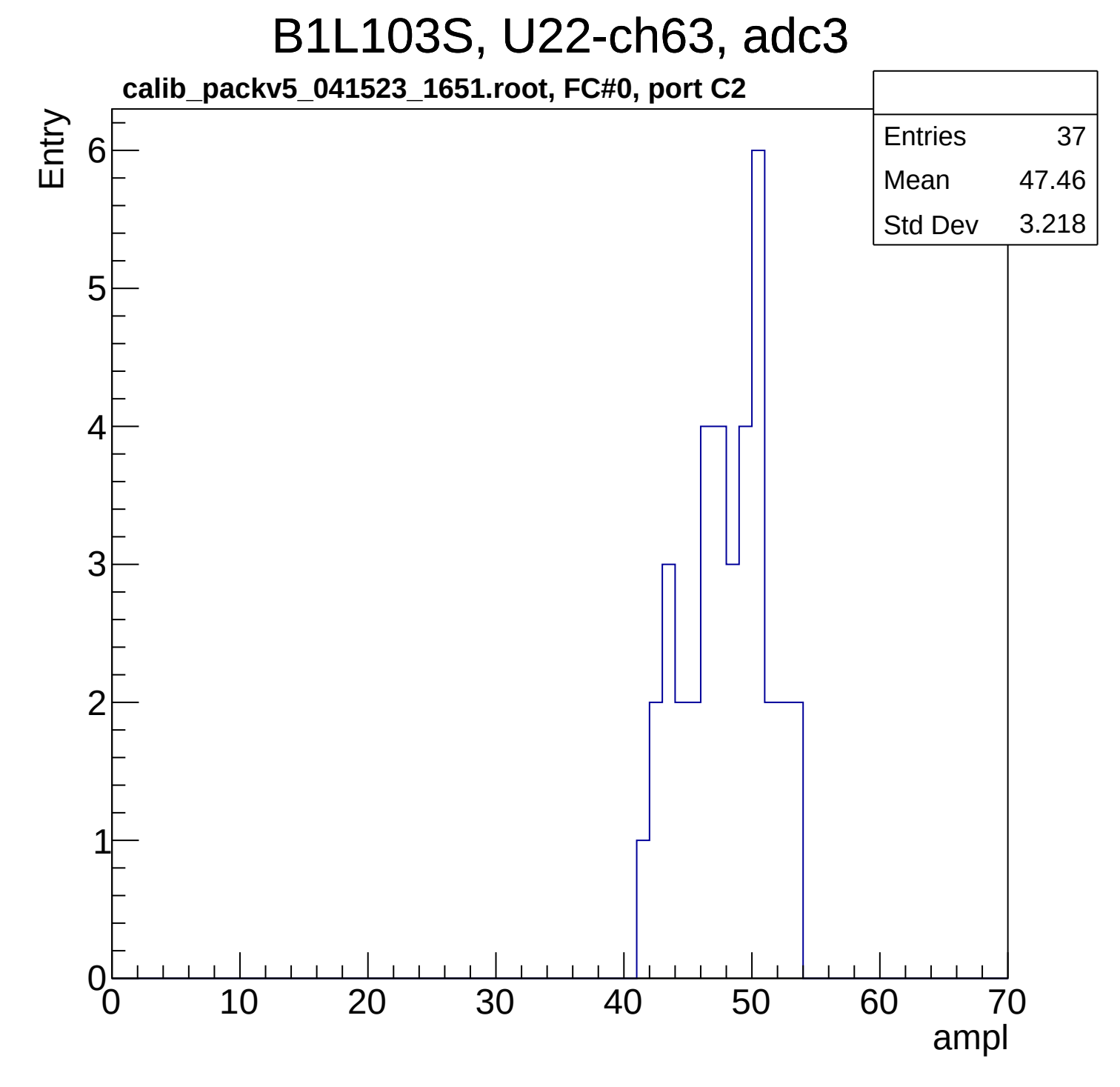
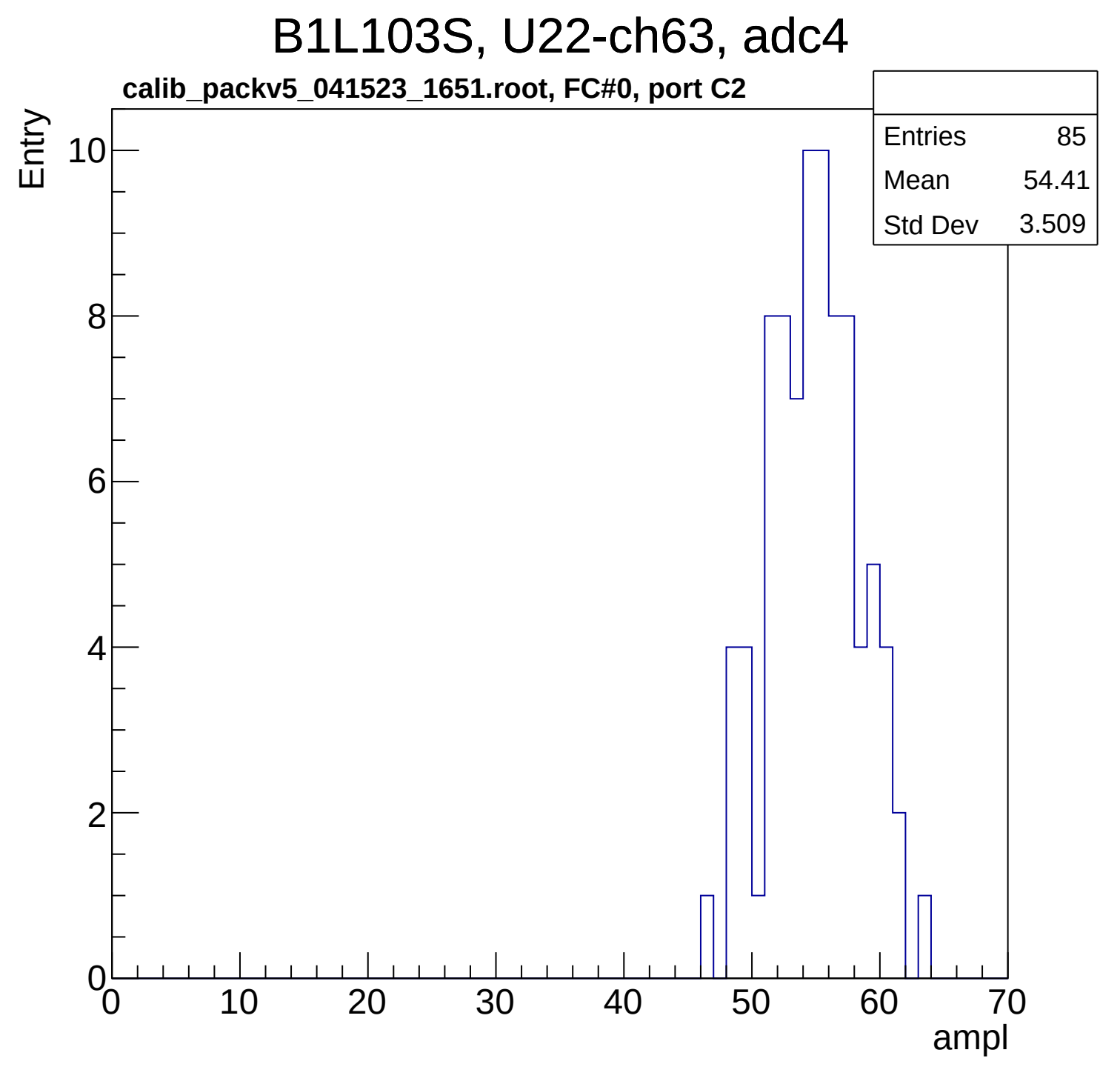
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch63, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 47.46
Std Dev 3.218
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U22-ch63, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 54.41
Std Dev 3.509
Entry
ampl
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4
6
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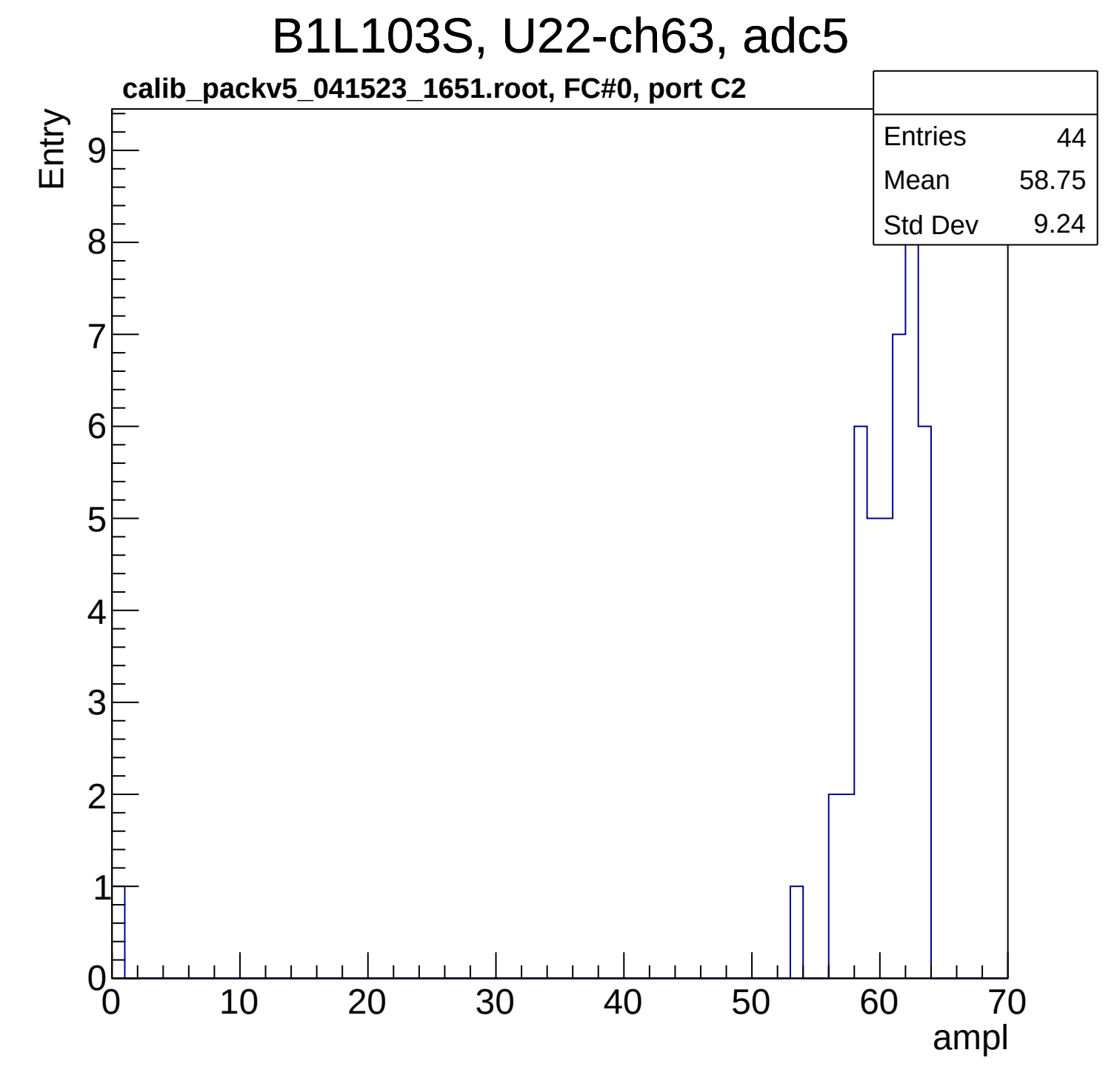
10
0
10
20
30
40
50
60
70


B1L103S, U22-ch63, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 58.75
Std Dev 9.24
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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20
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40
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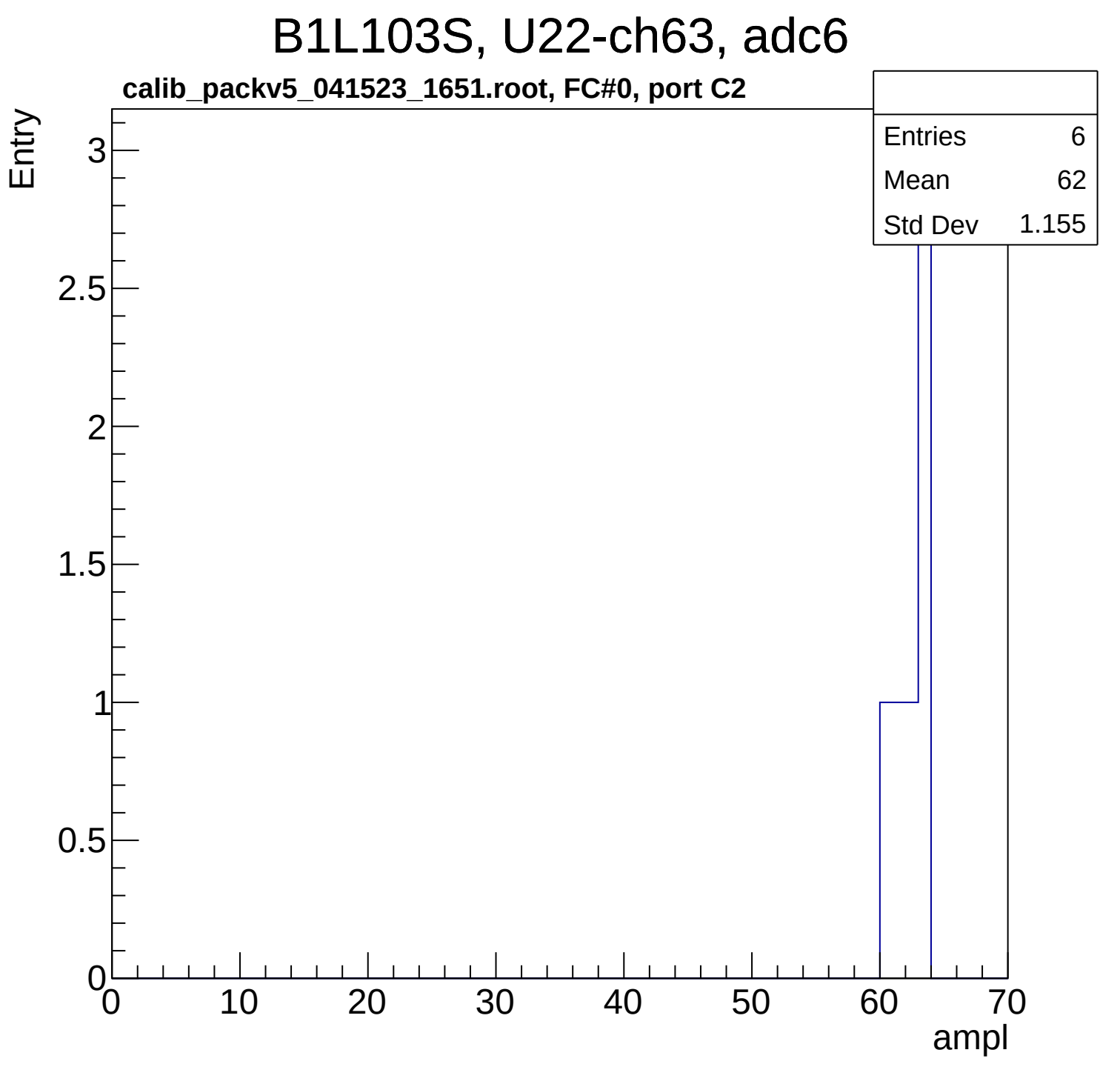
60
70


B1L103S, U22-ch63, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 62
Std Dev 1.155
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
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20
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40
50
60
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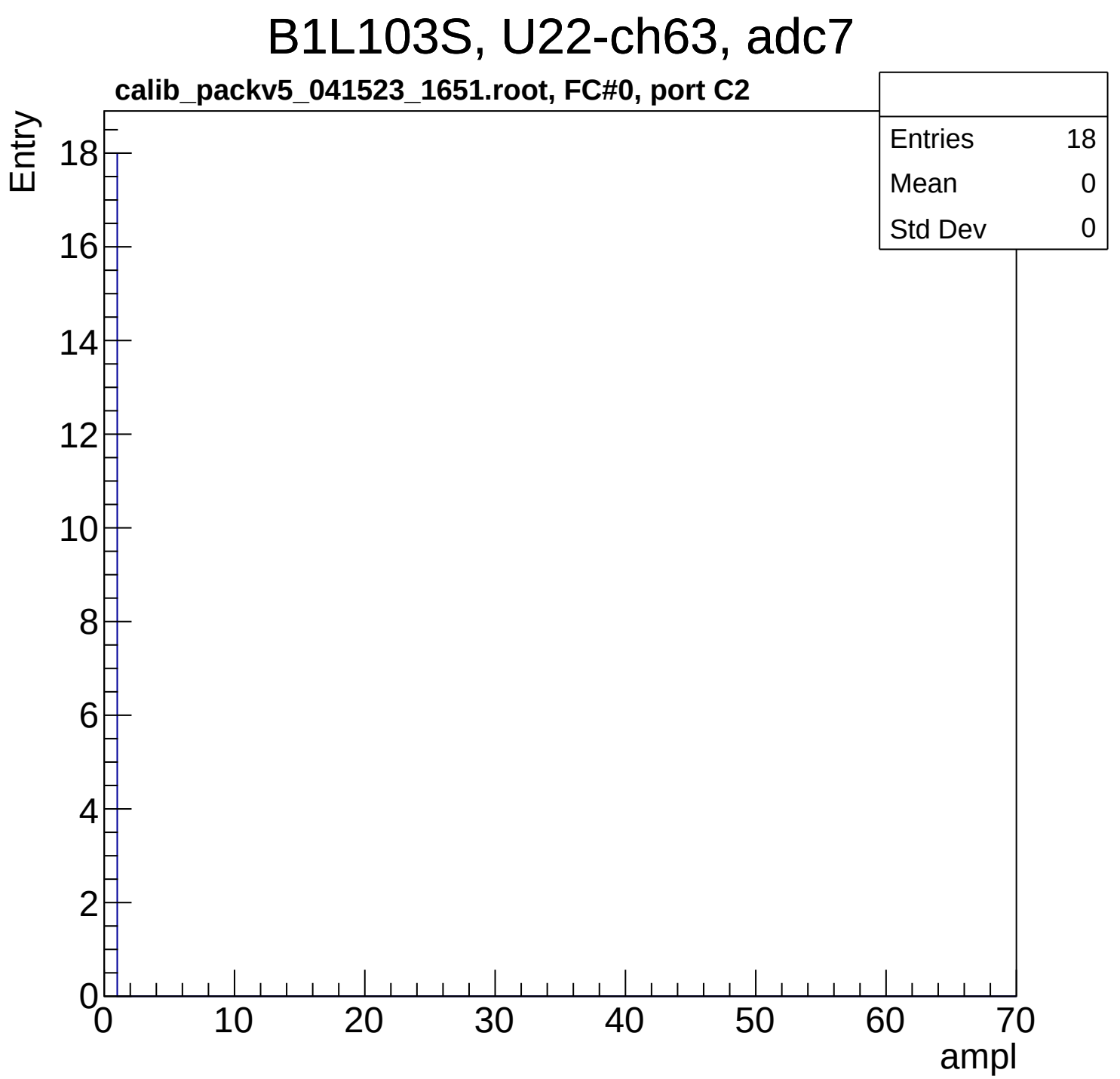
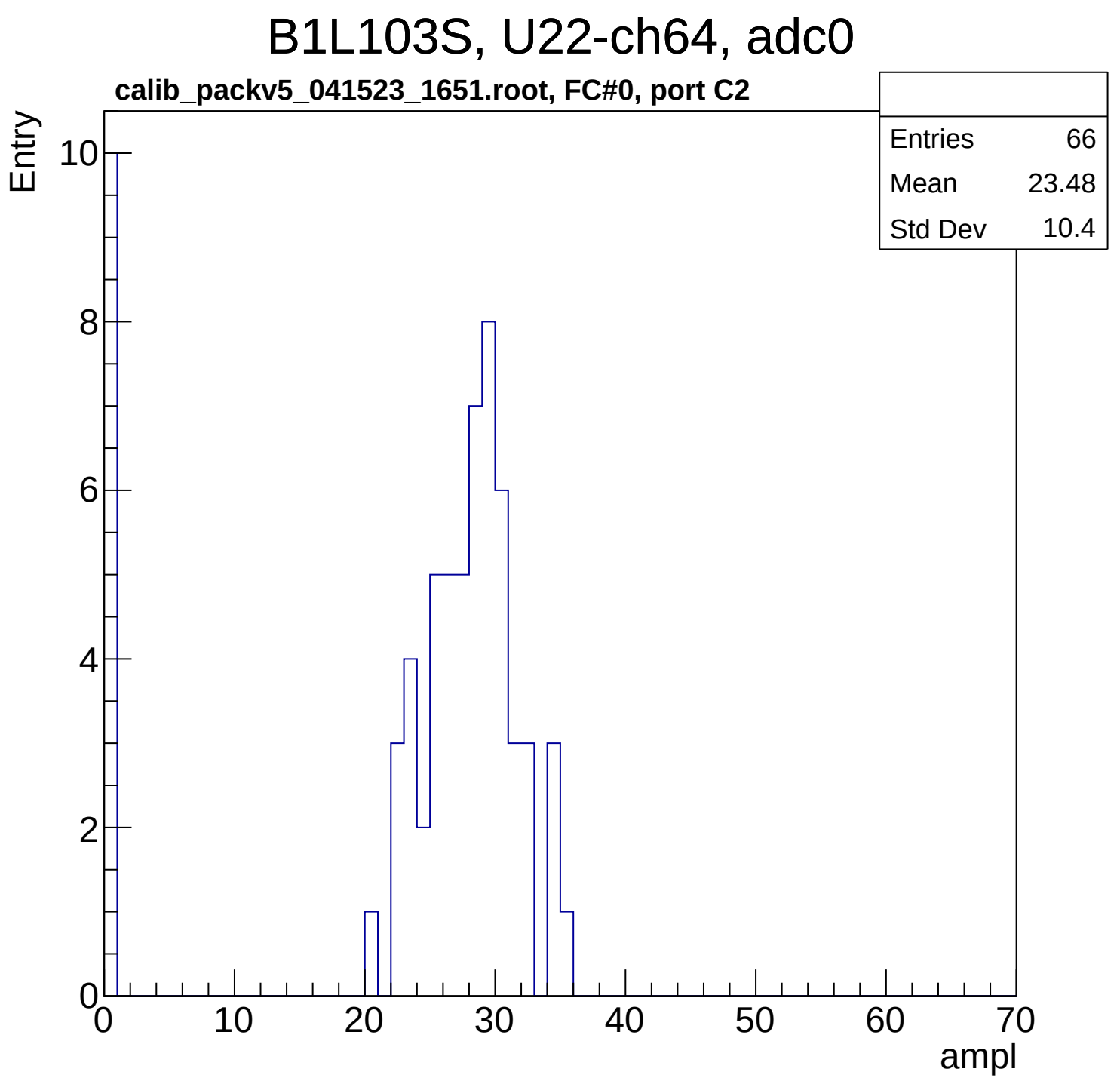
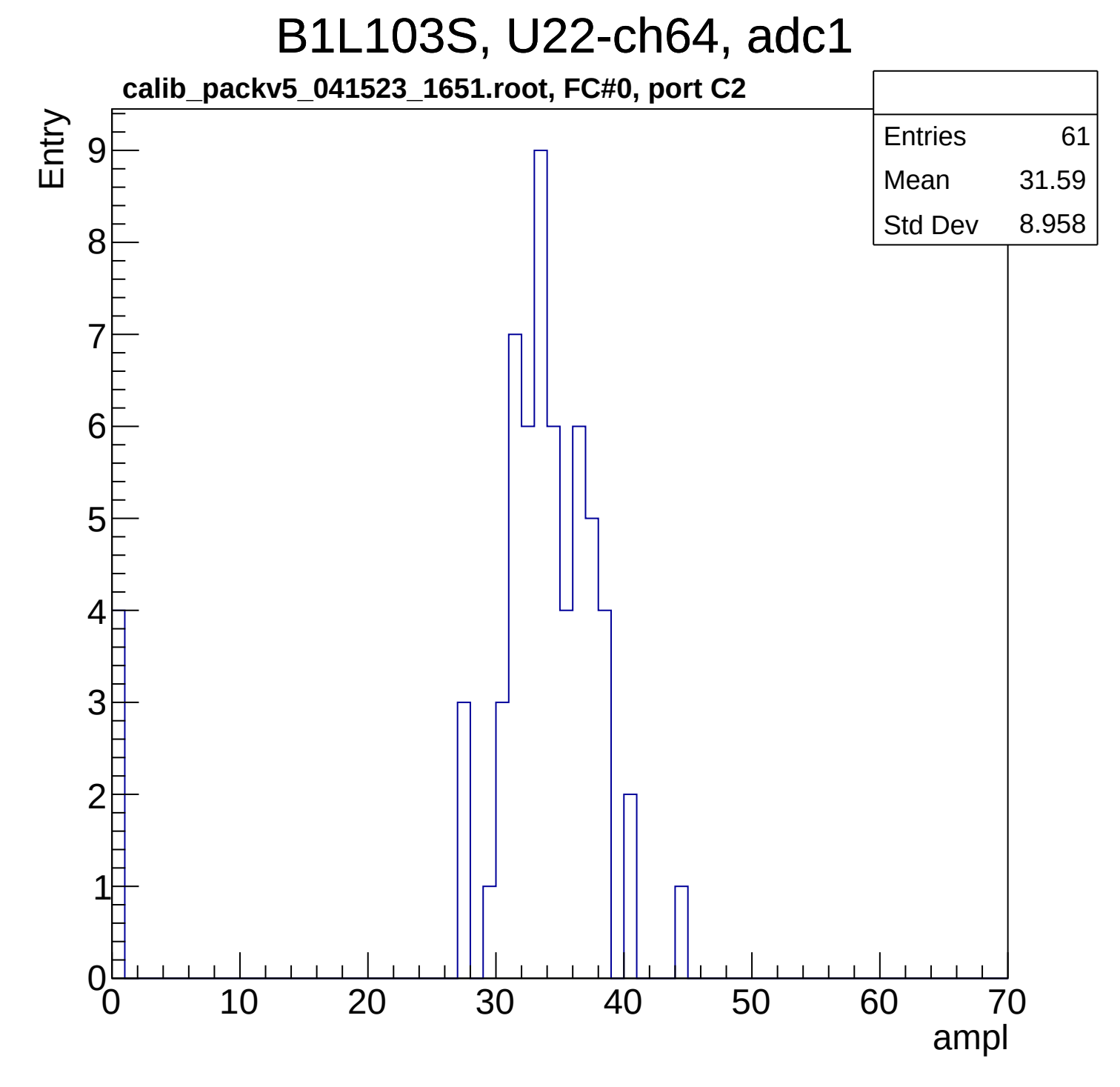

B1L103S, U22-ch63, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch64, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 23.48
Std Dev 10.4
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U22-ch64, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 31.59
Std Dev 8.958
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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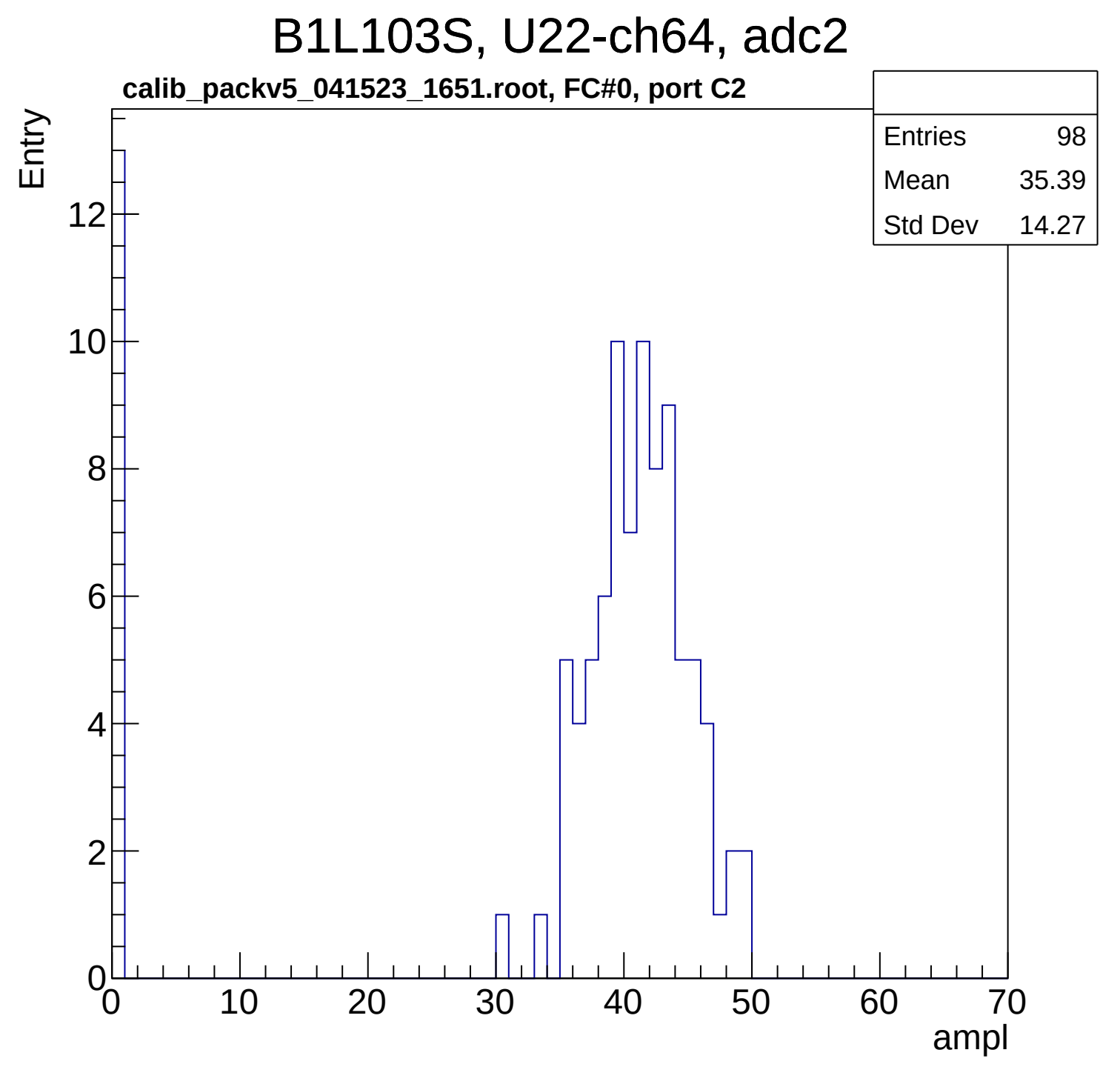
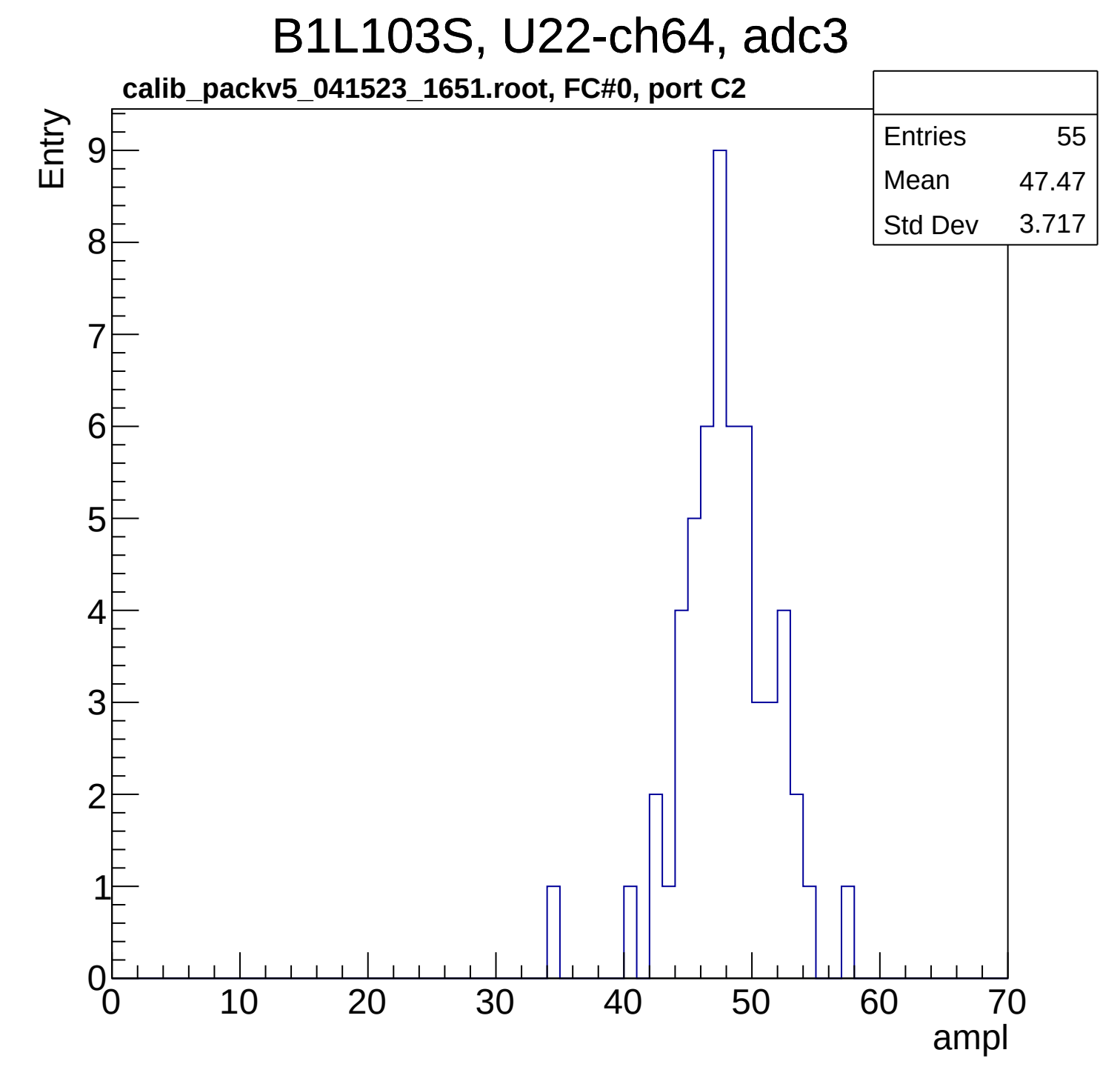

B1L103S, U22-ch64, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 98
Mean 35.39
Std Dev 14.27
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch64, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 47.47
Std Dev 3.717
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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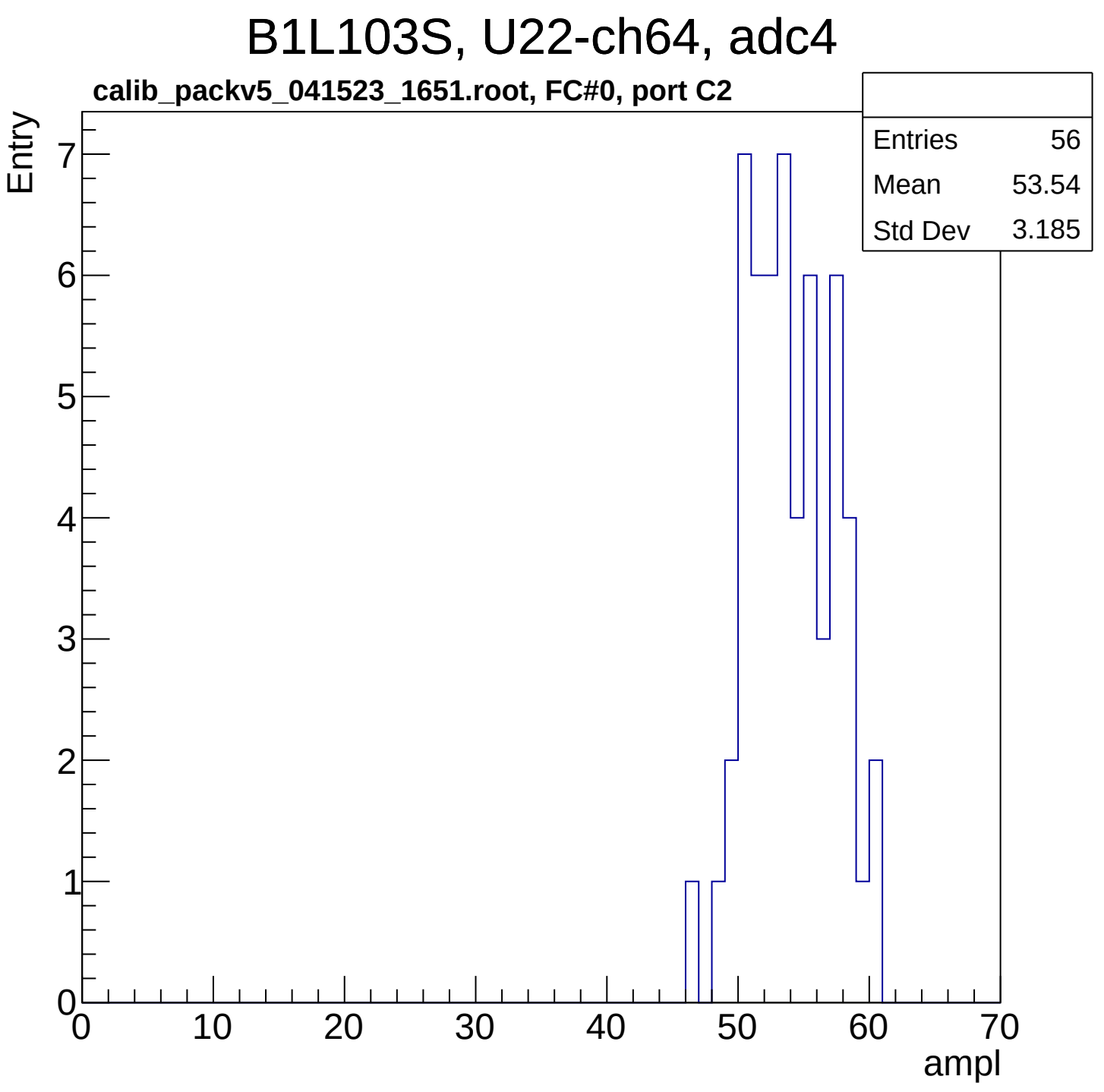
30
40
50
60
70


B1L103S, U22-ch64, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 53.54
Std Dev 3.185
Entry
ampl
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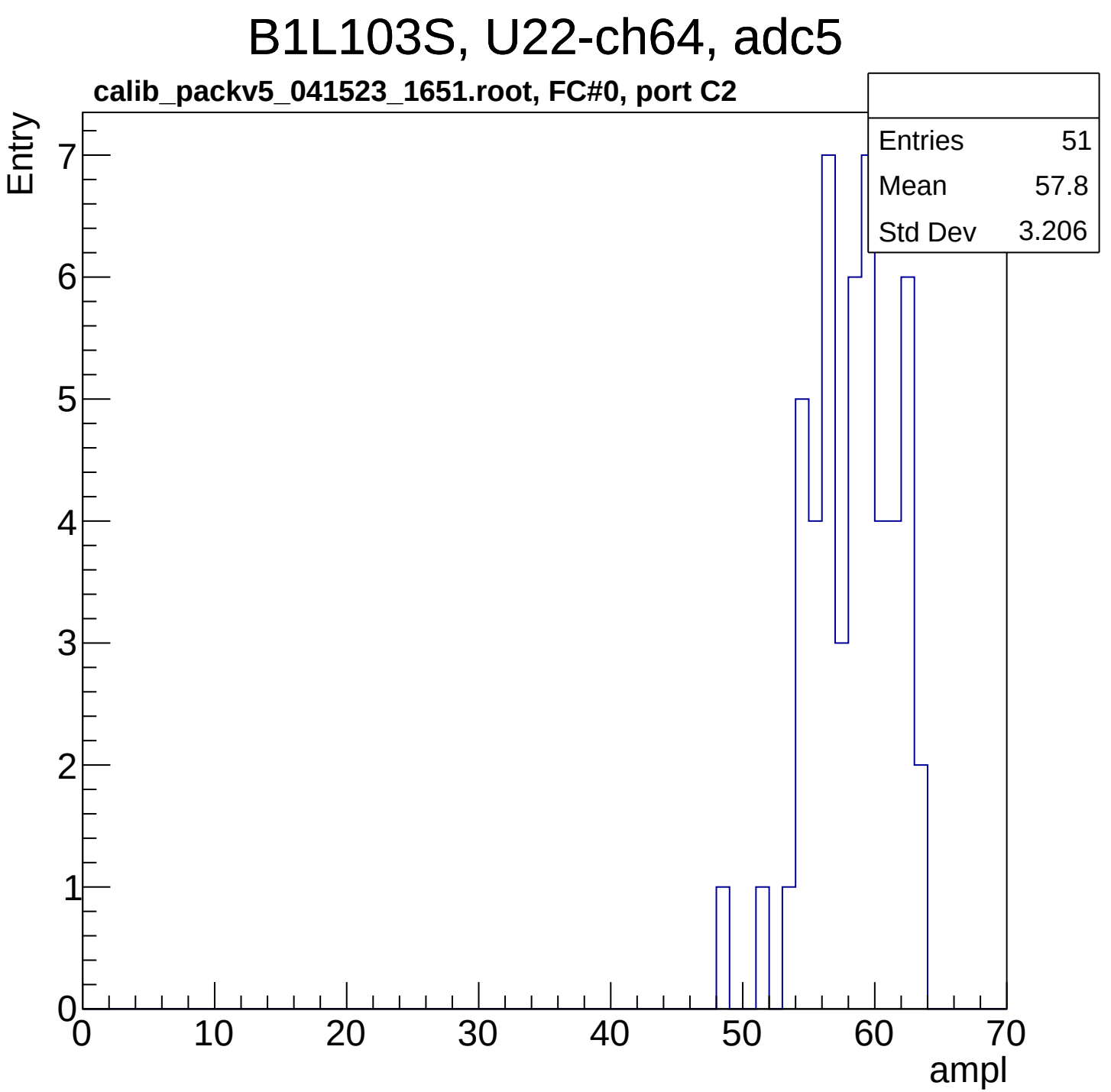
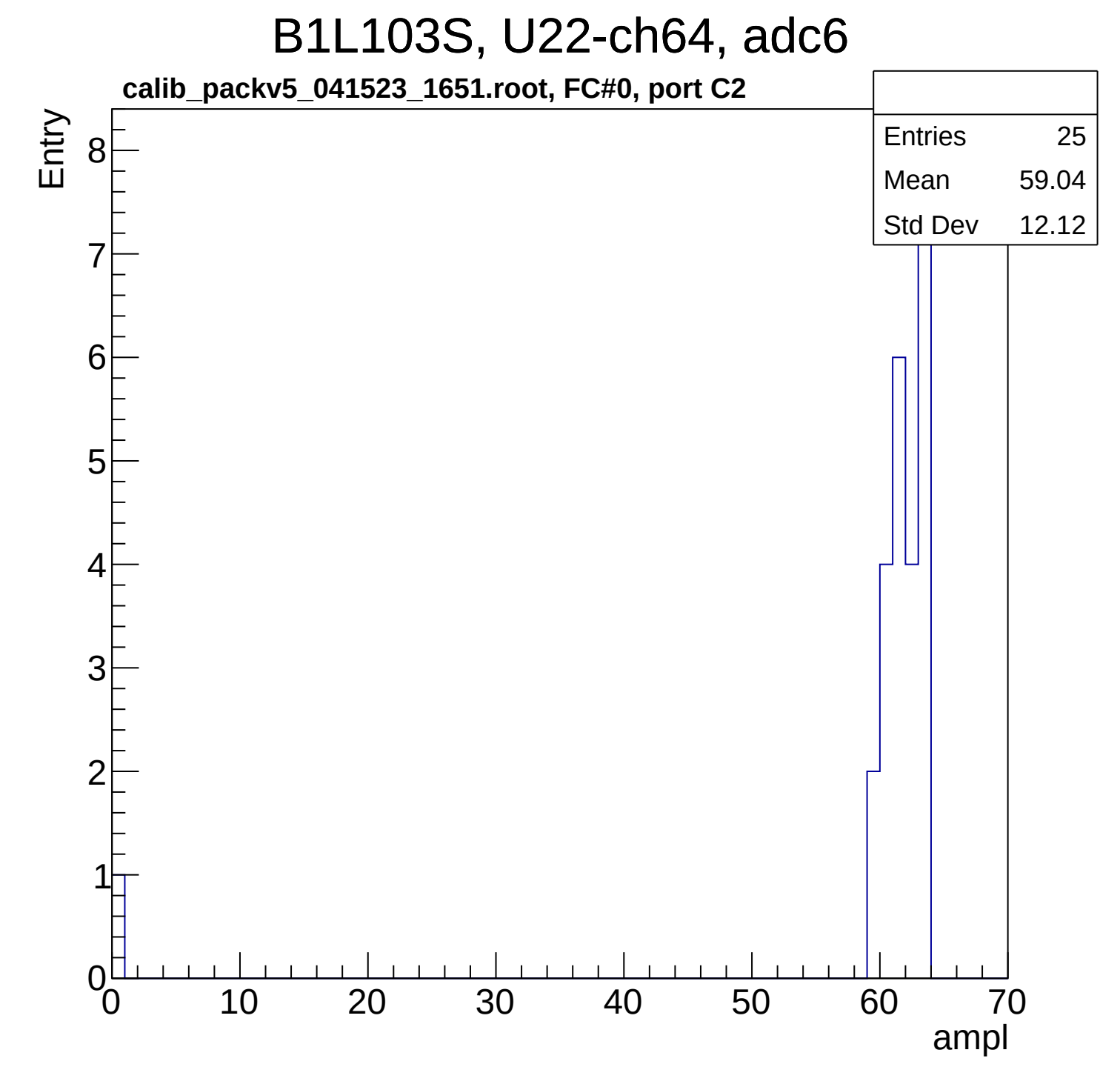
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U22-ch64, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 57.8
Std Dev 3.206
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U22-ch64, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 59.04
Std Dev 12.12
Entry
ampl
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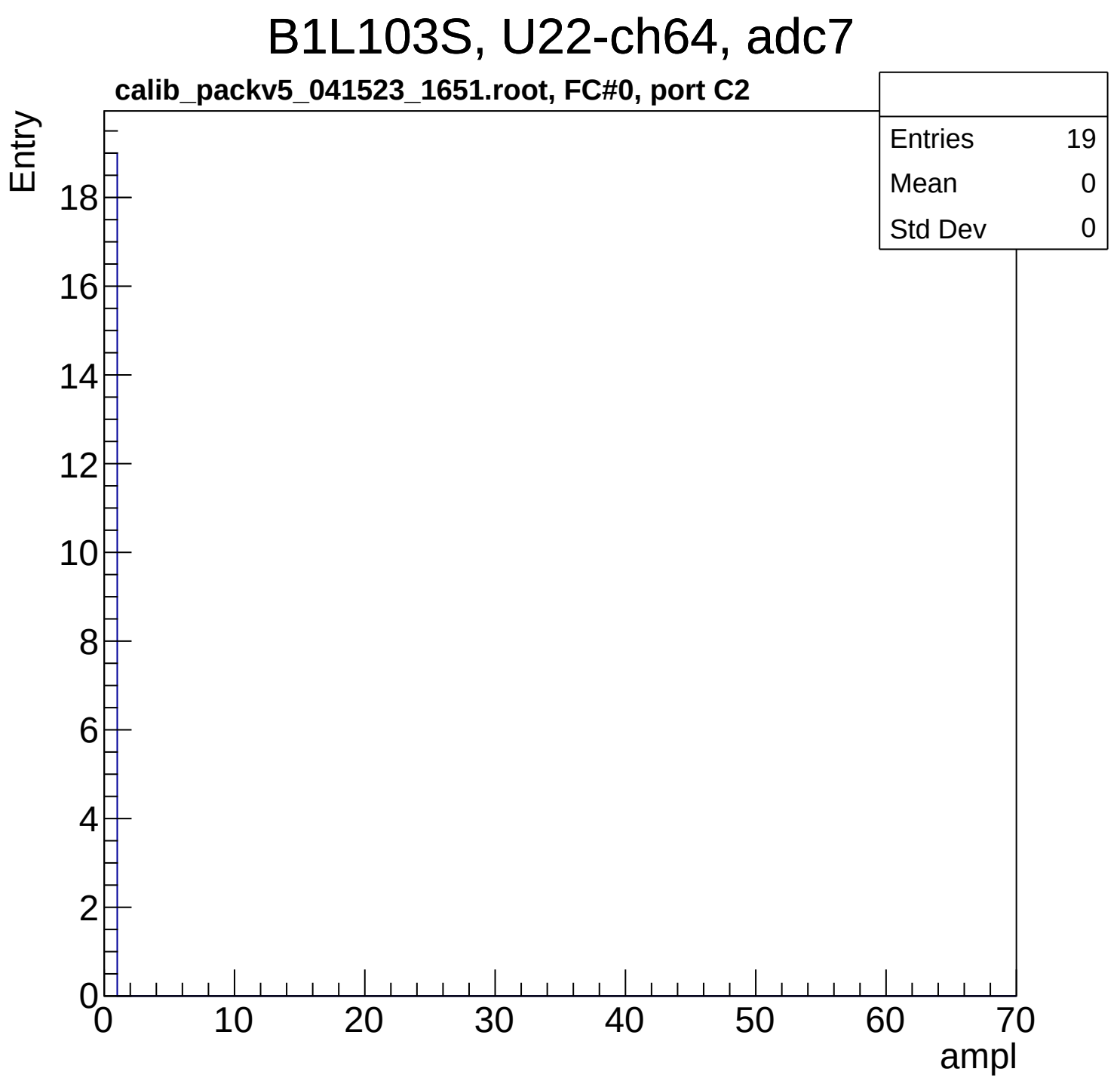
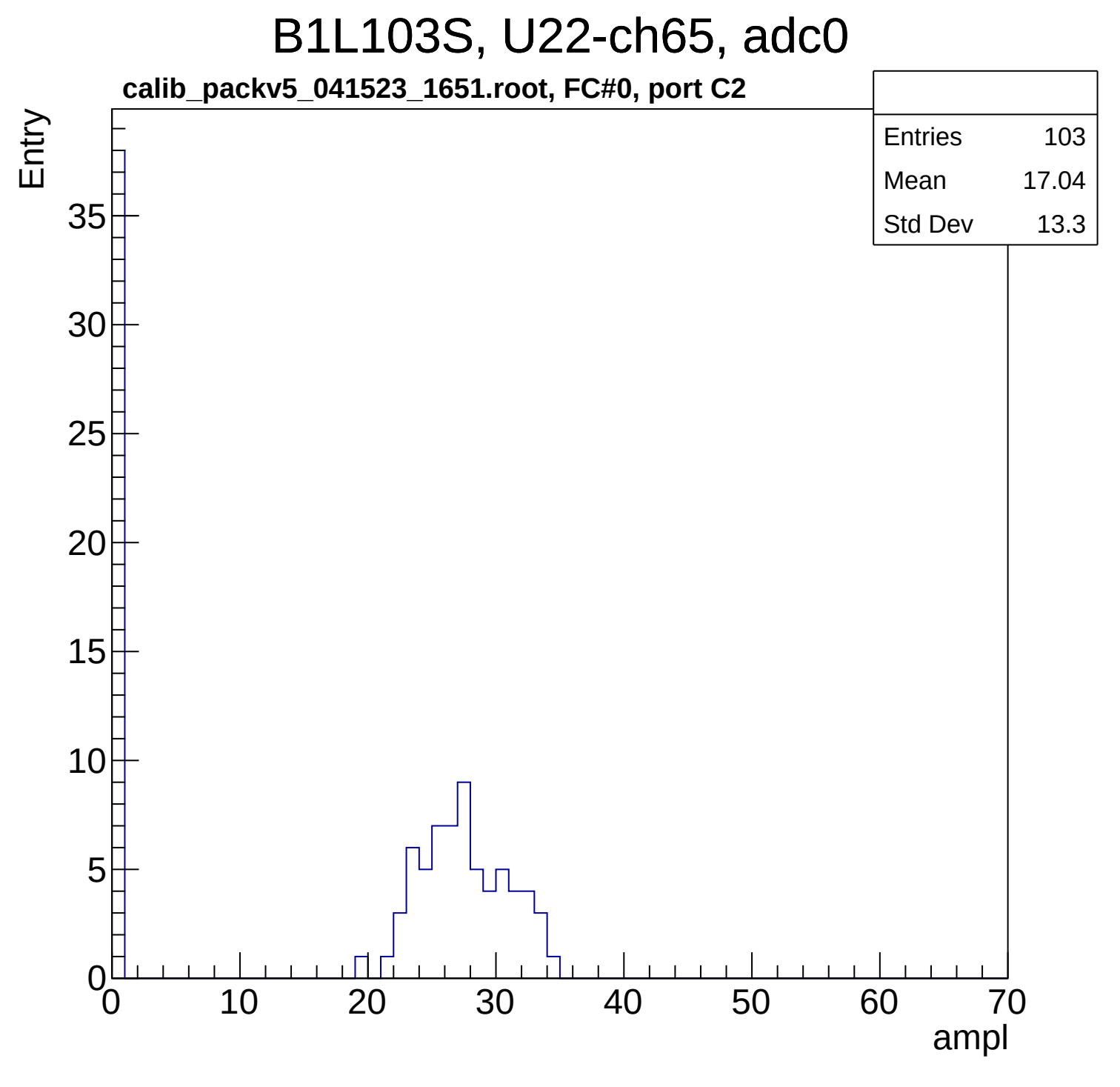
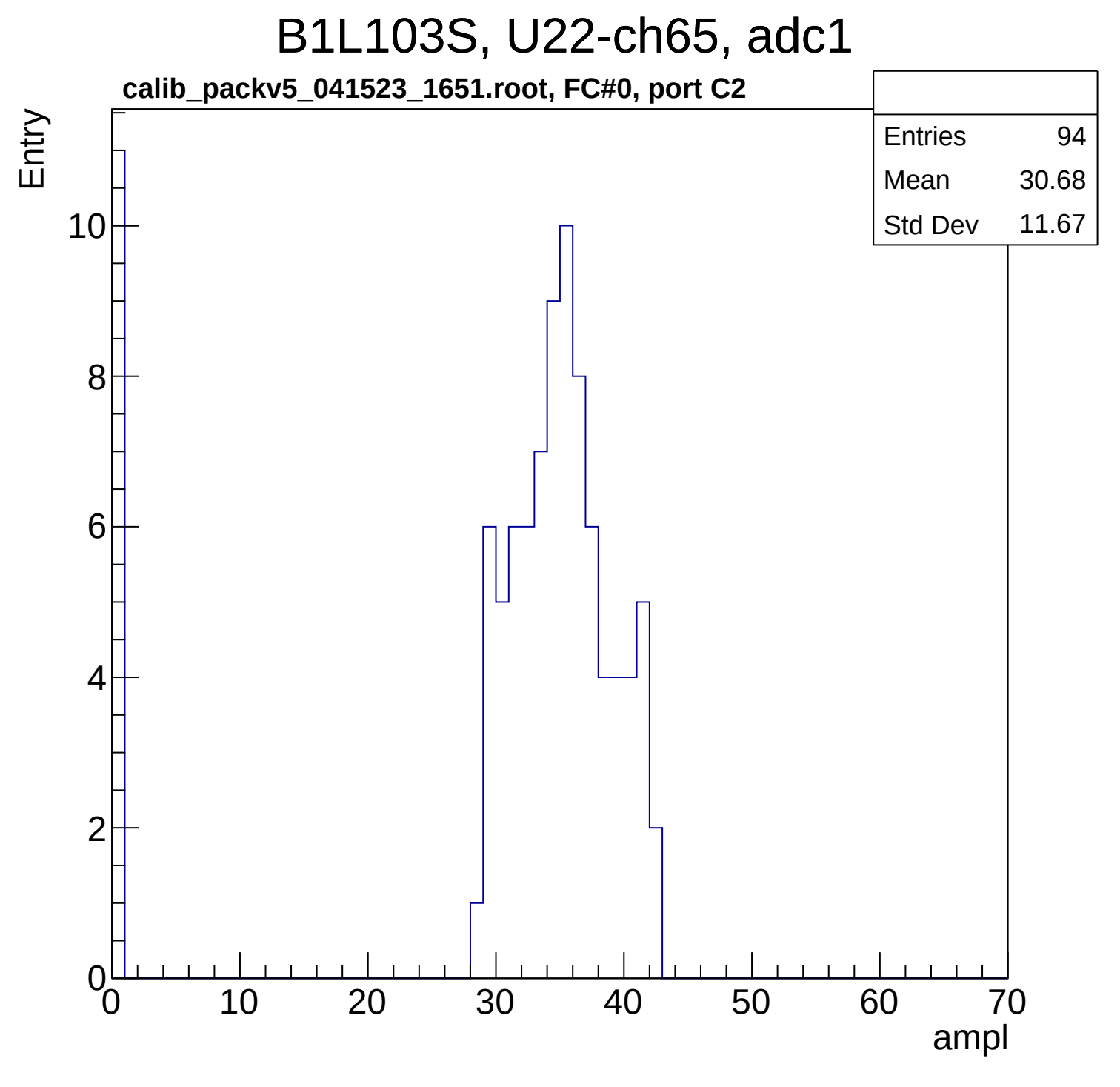
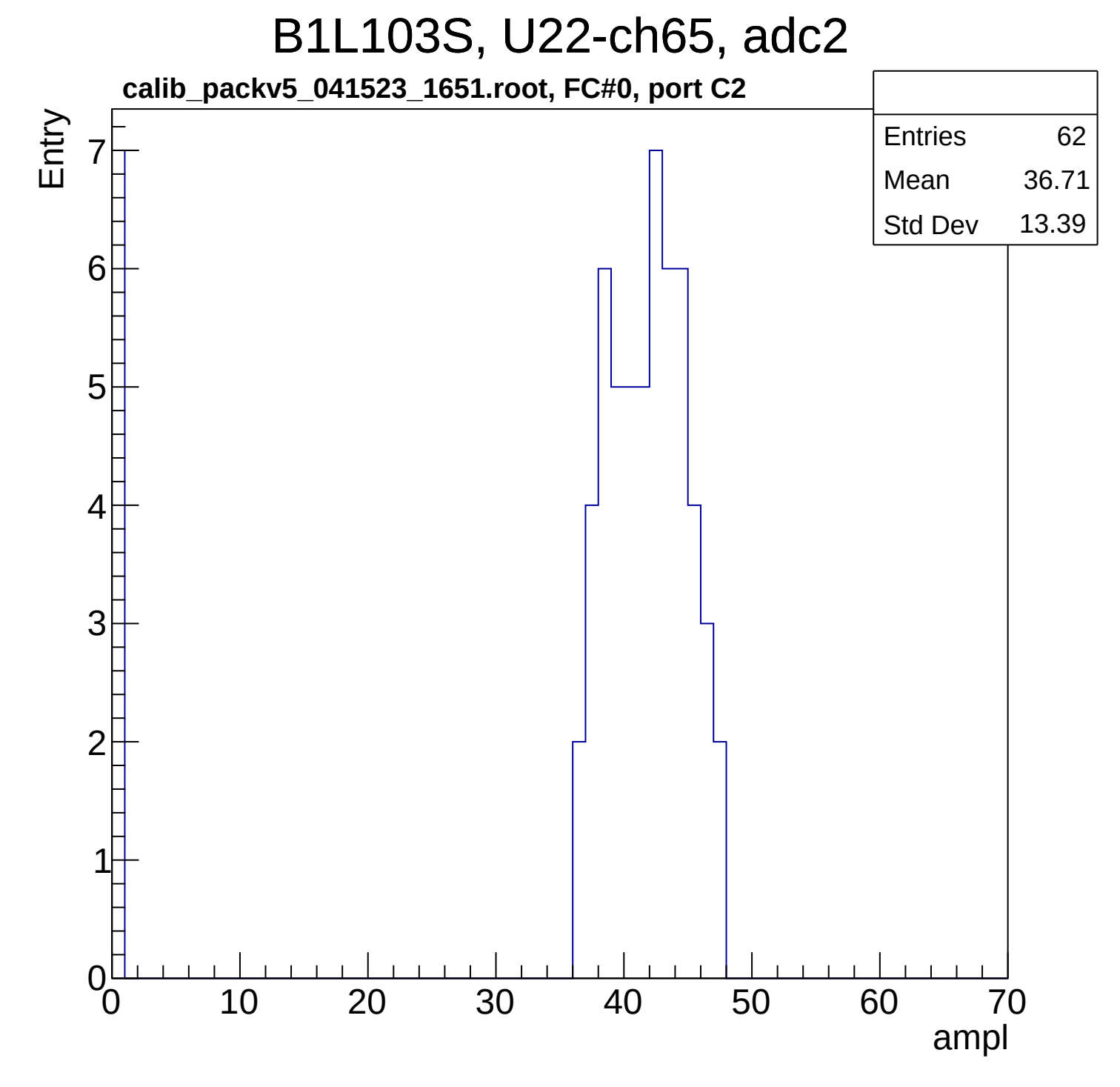
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch64, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch65, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 103
Mean 17.04
Std Dev 13.3
Entry
0
5
10
15
20
25
30
35
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch65, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 30.68
Std Dev 11.67
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch65, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 36.71
Std Dev 13.39
Entry
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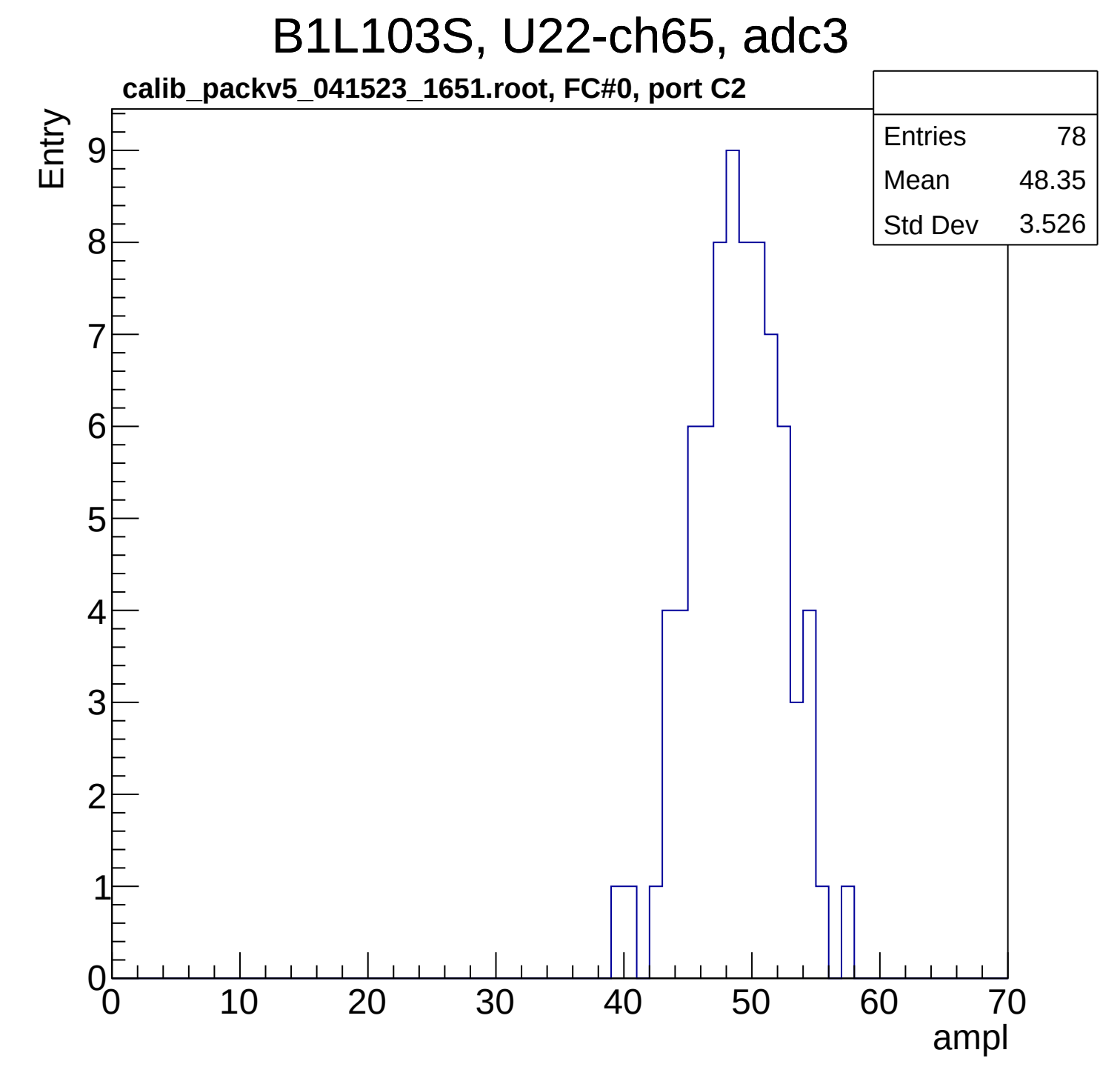
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch65, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 48.35
Std Dev 3.526
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
10
20
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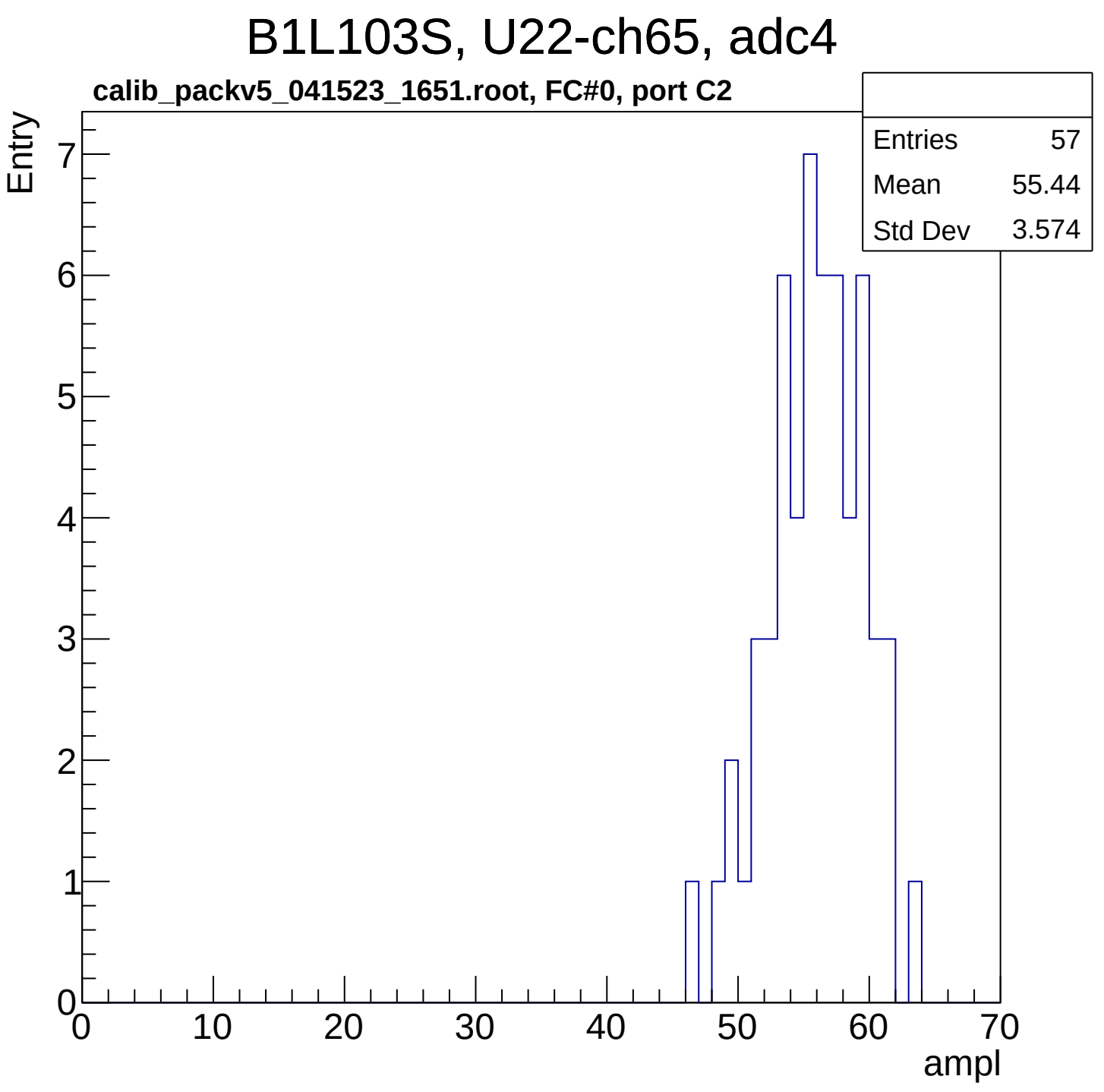
40
50
60
70


B1L103S, U22-ch65, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 55.44
Std Dev 3.574
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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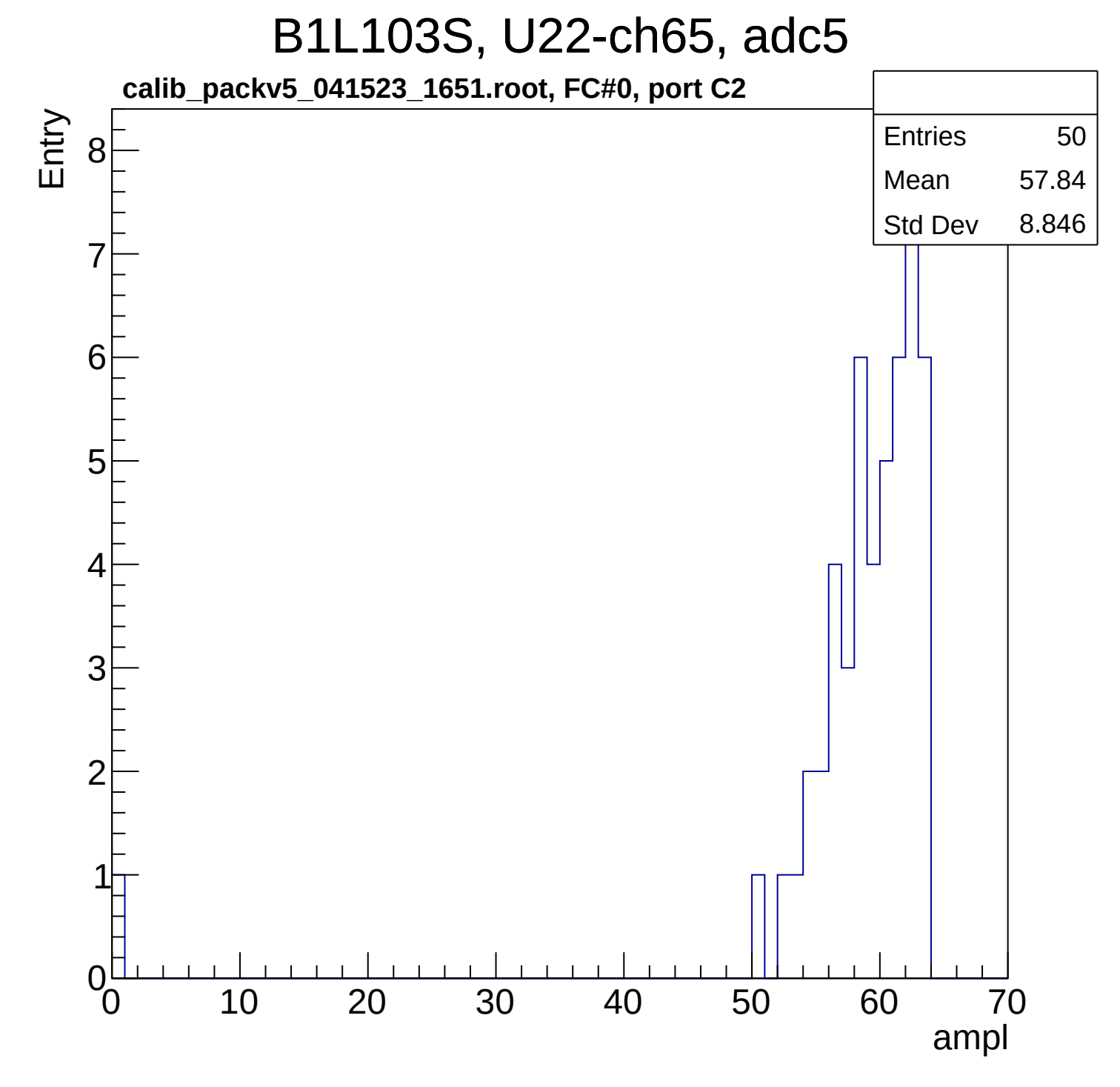
B1L103S, U22-ch65, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 57.84
Std Dev 8.846
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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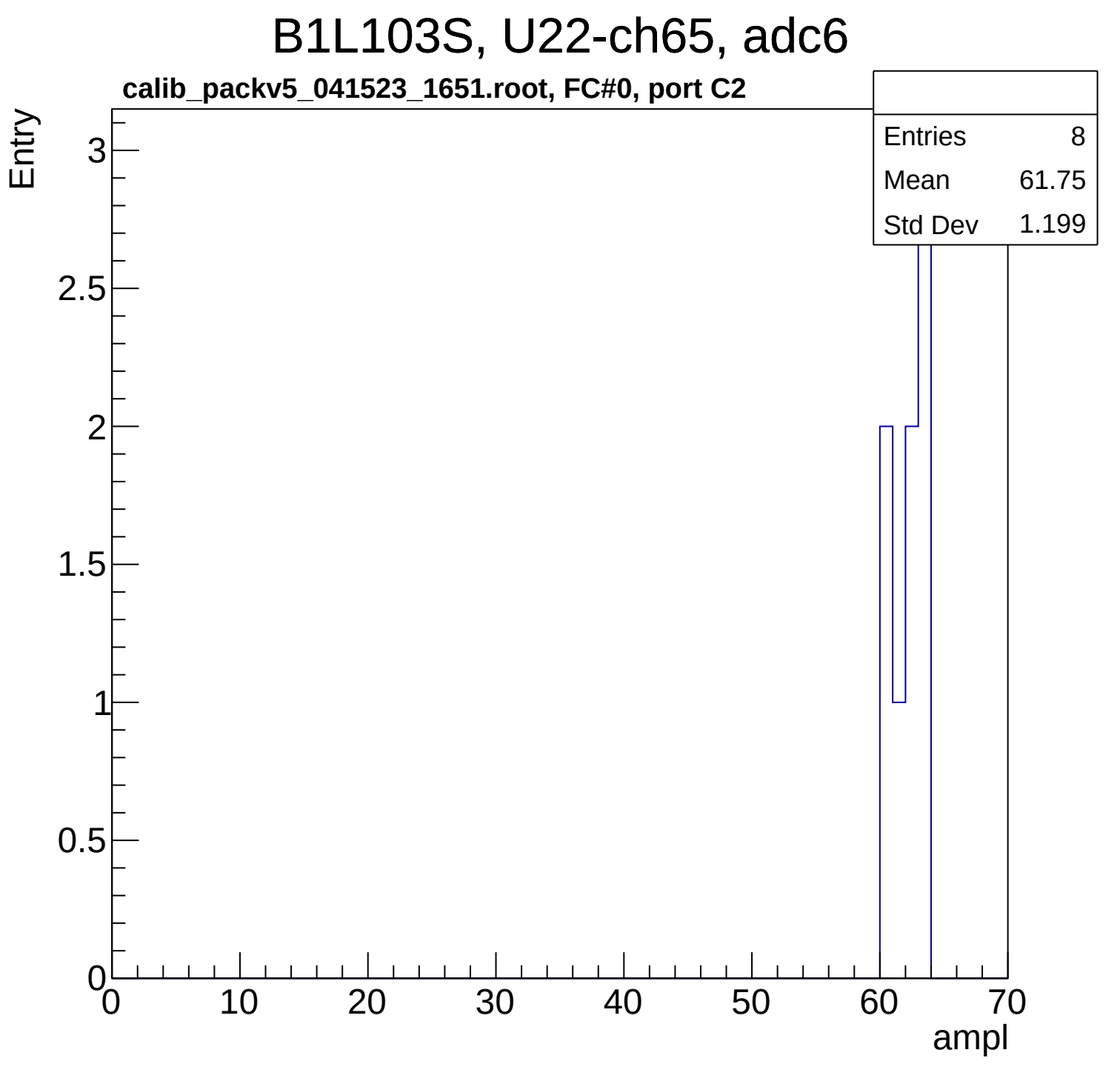
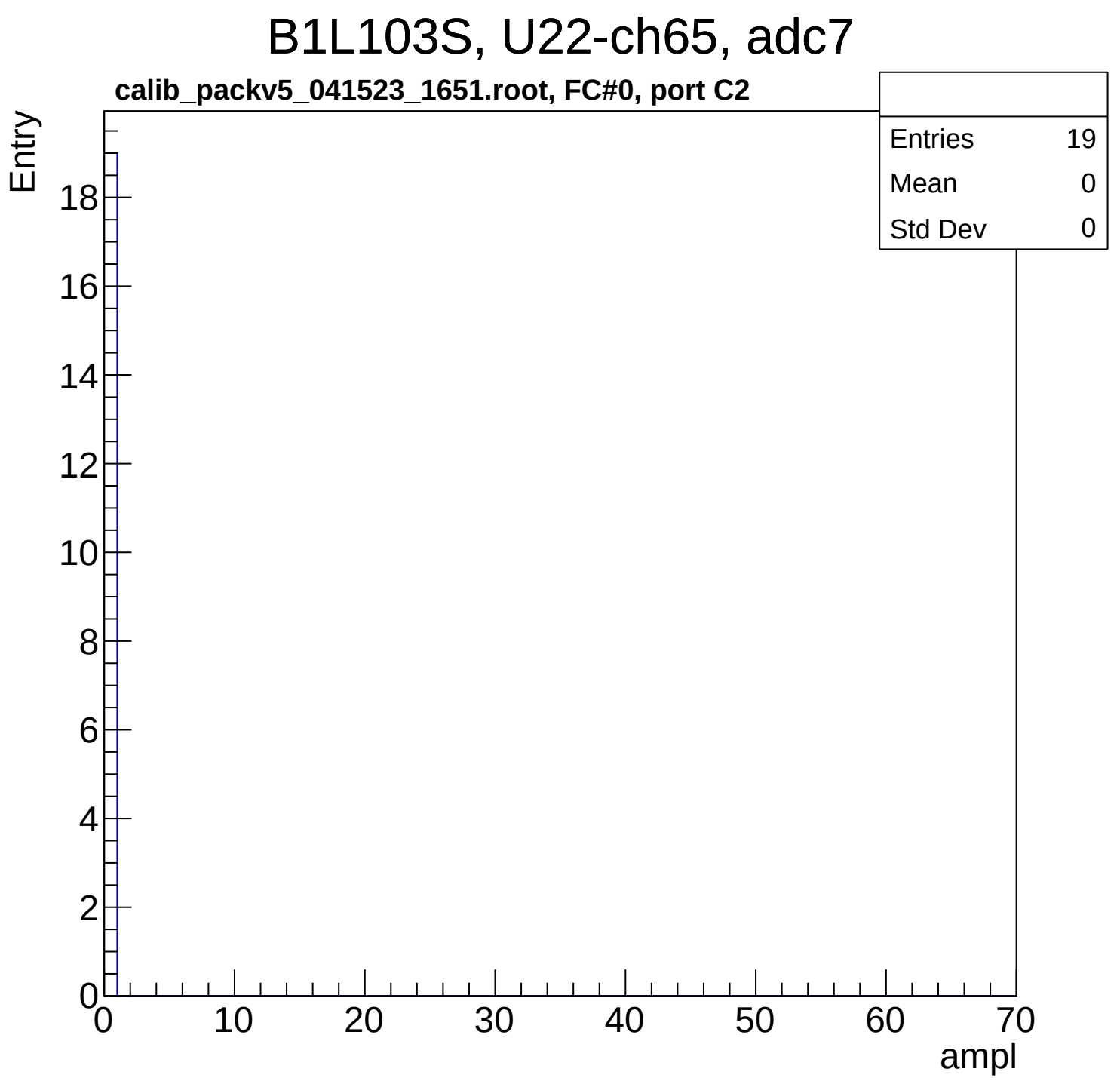
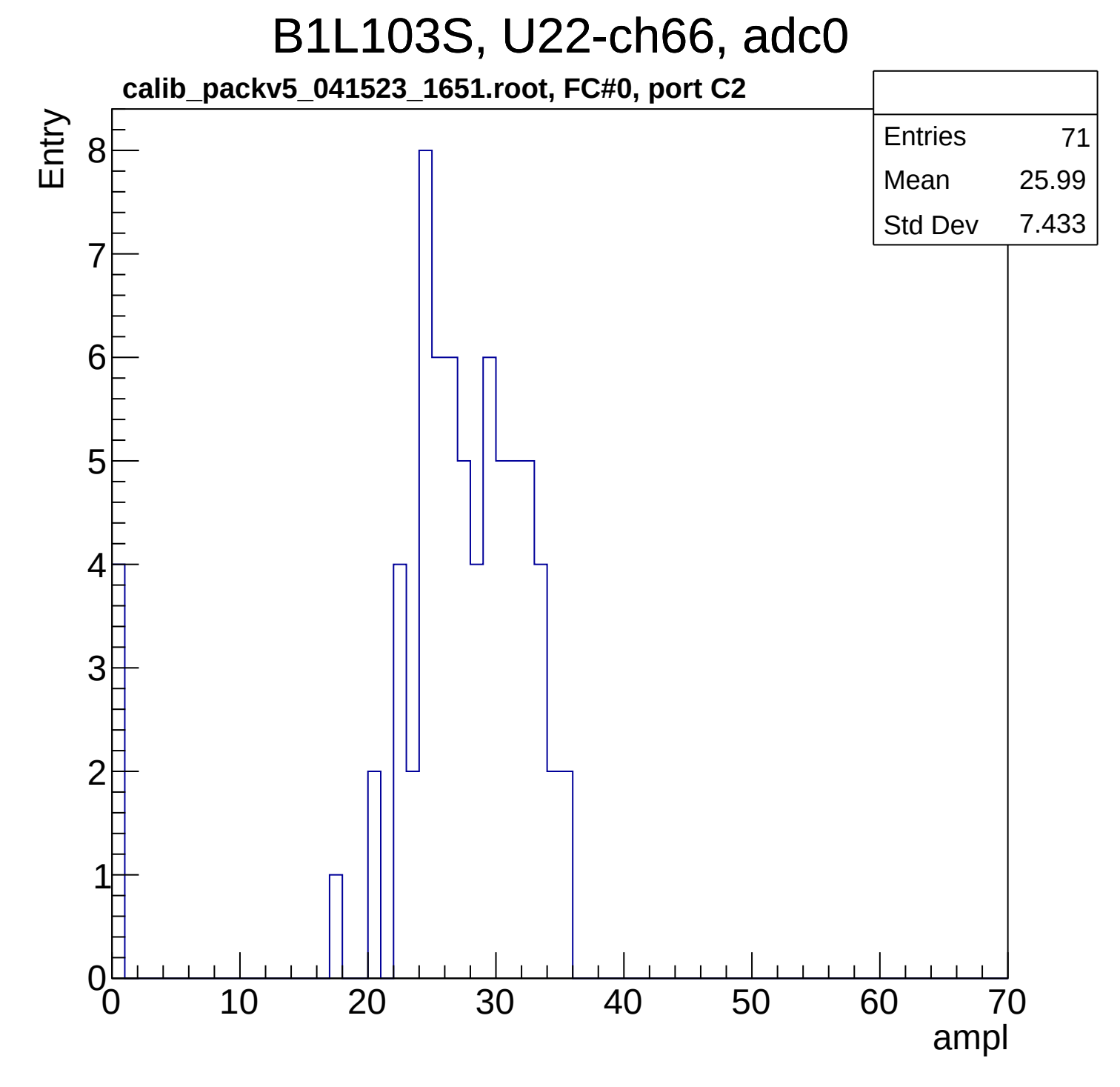

B1L103S, U22-ch65, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 61.75
Std Dev 1.199
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U22-ch65, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch66, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 25.99
Std Dev 7.433
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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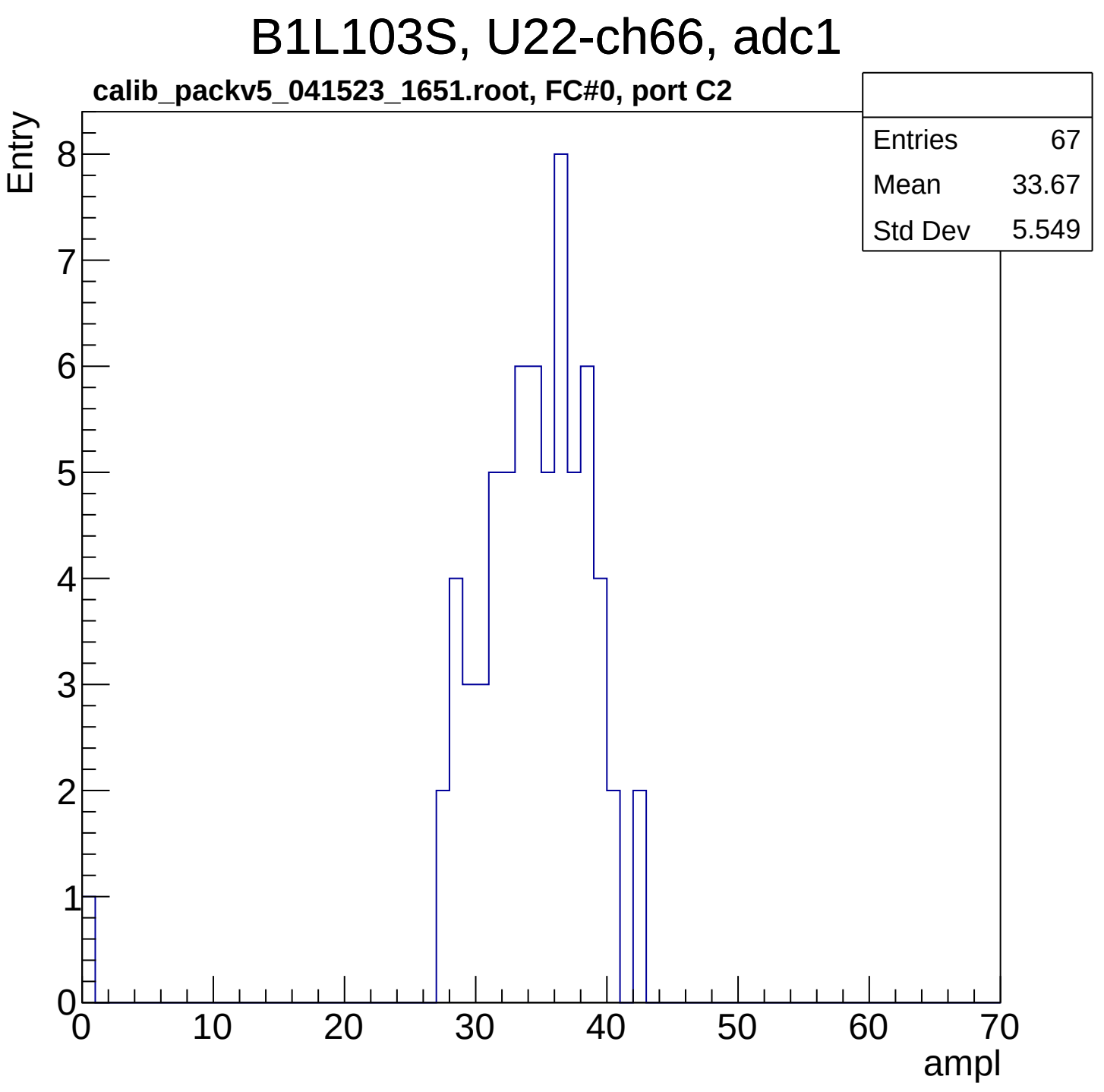
60
70


B1L103S, U22-ch66, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 33.67
Std Dev 5.549
Entry
ampl
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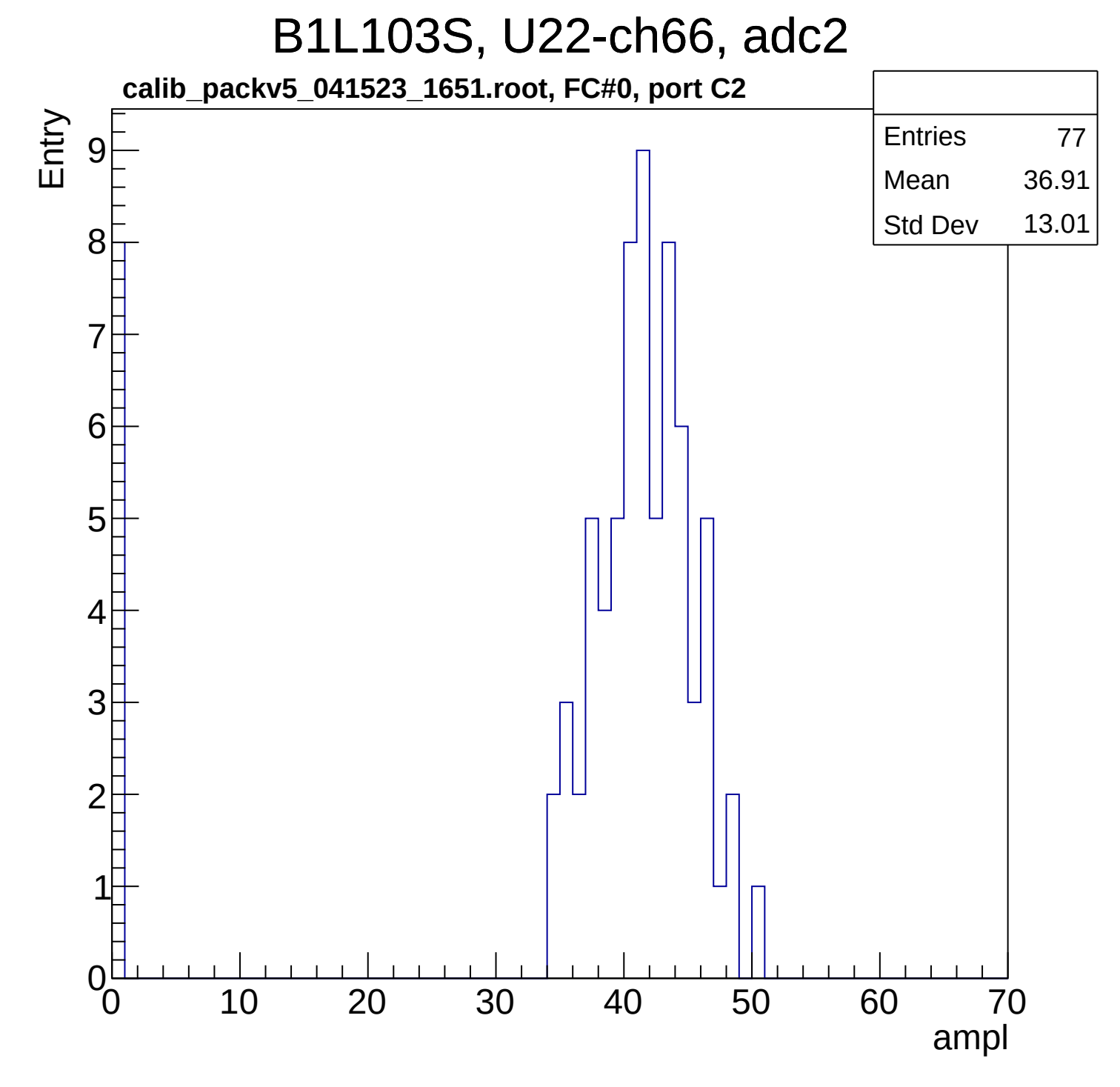
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch66, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 36.91
Std Dev 13.01
Entry
ampl
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2
3
4
5
6
7
8
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0
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20
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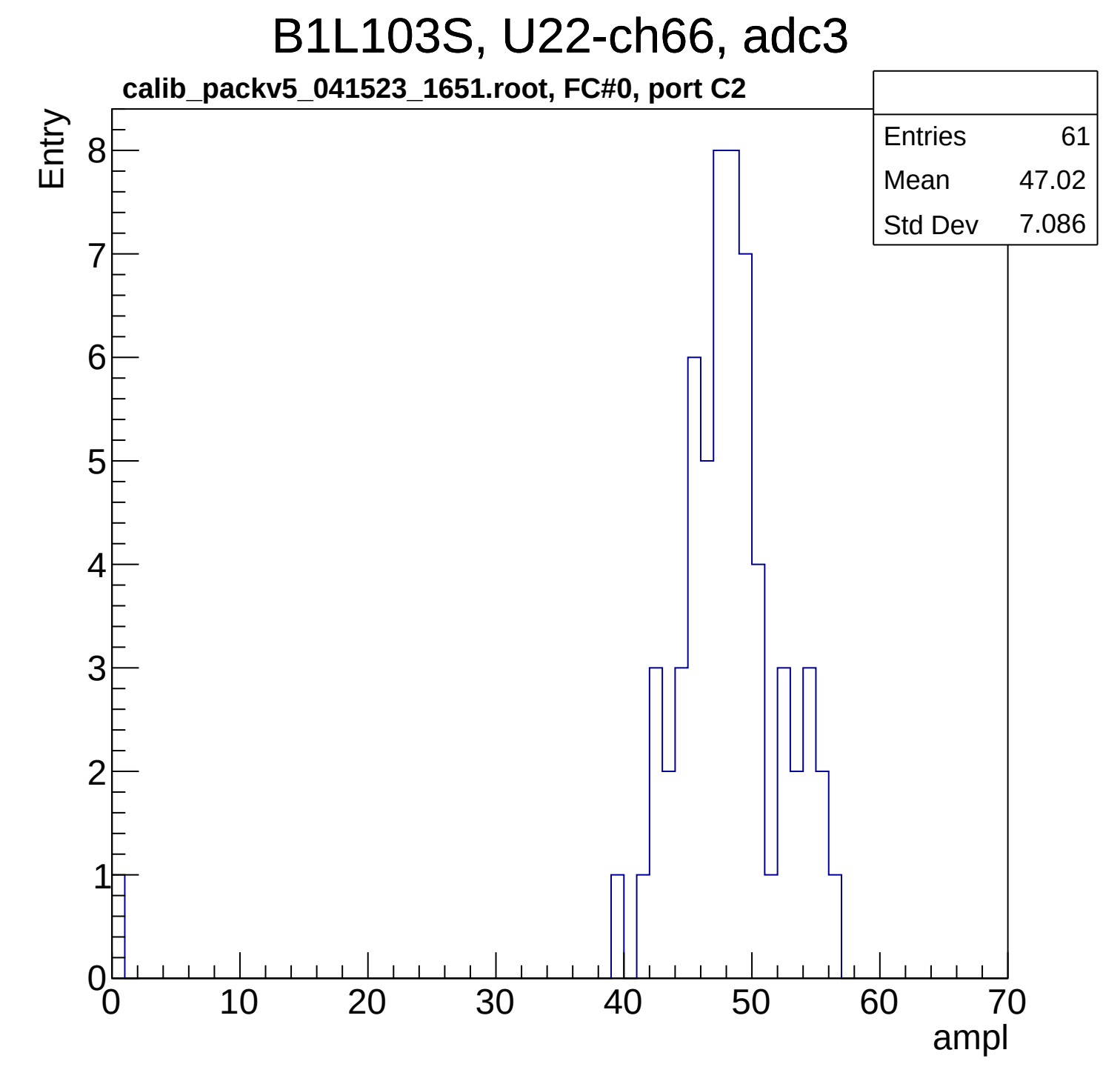
50
60
70


B1L103S, U22-ch66, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 47.02
Std Dev 7.086
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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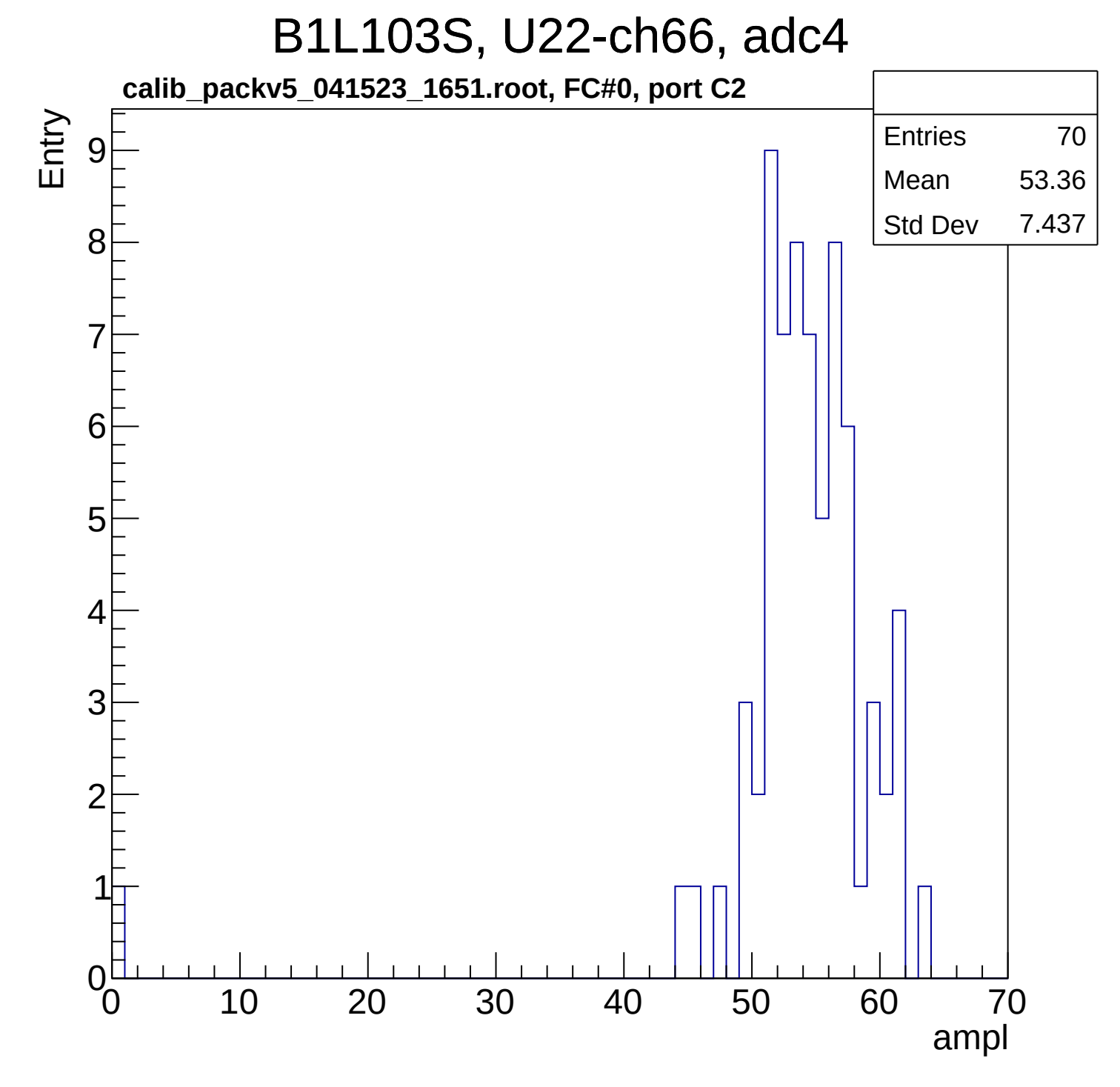
40
50
60
70


B1L103S, U22-ch66, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 53.36
Std Dev 7.437
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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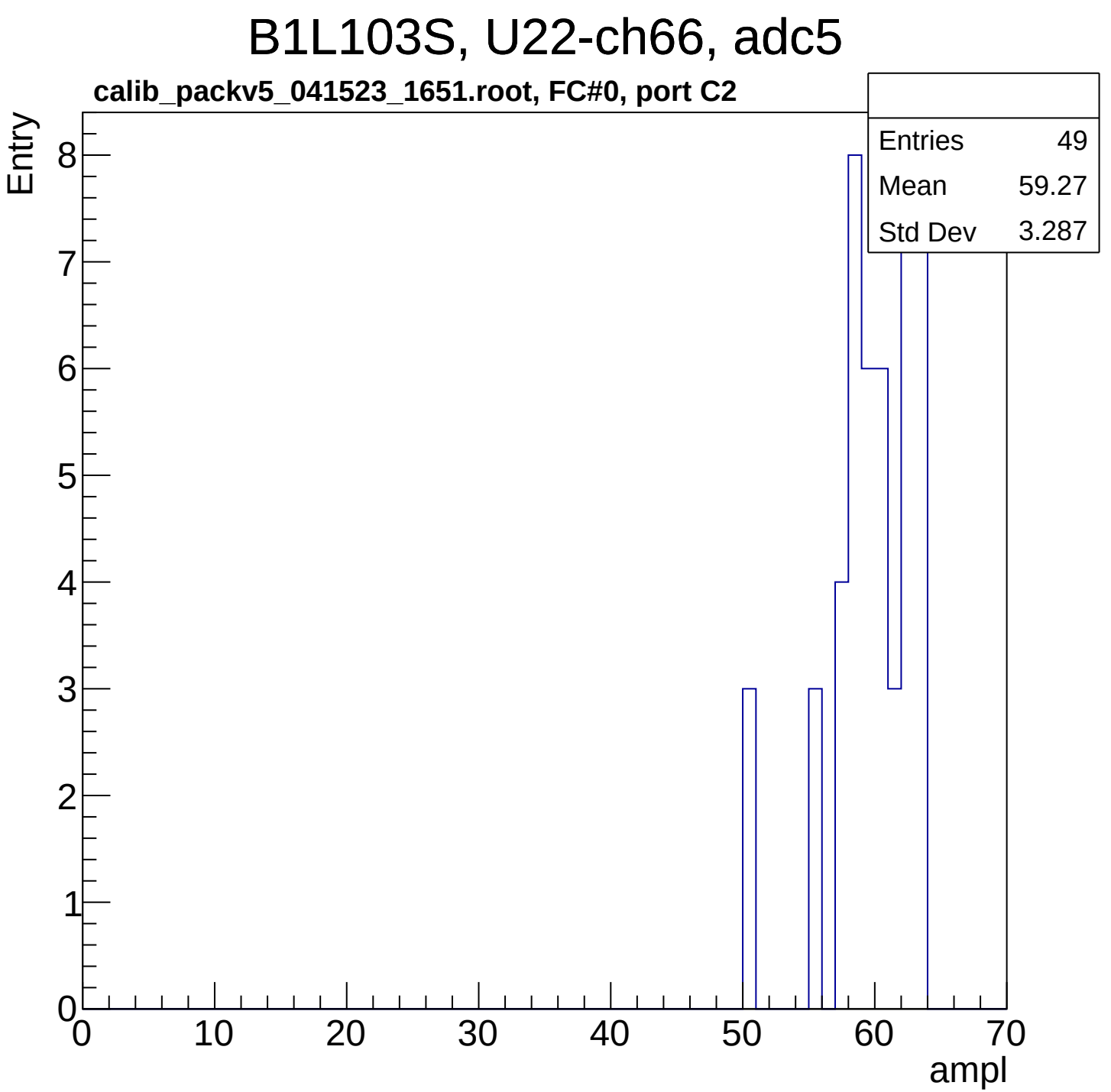
40
50
60
70


B1L103S, U22-ch66, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 59.27
Std Dev 3.287
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
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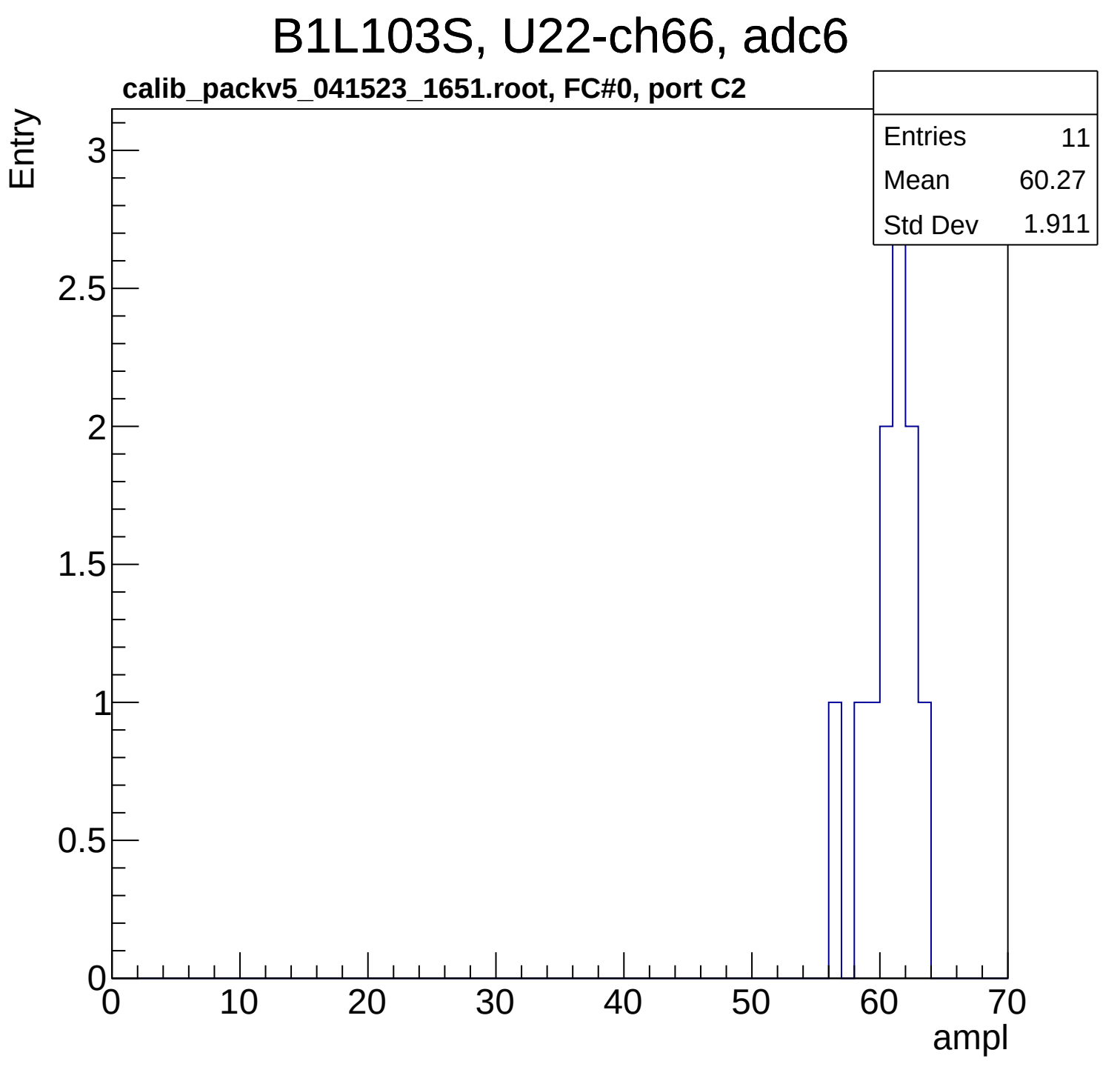
50
60
70


B1L103S, U22-ch66, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 60.27
Std Dev 1.911
Entry
ampl
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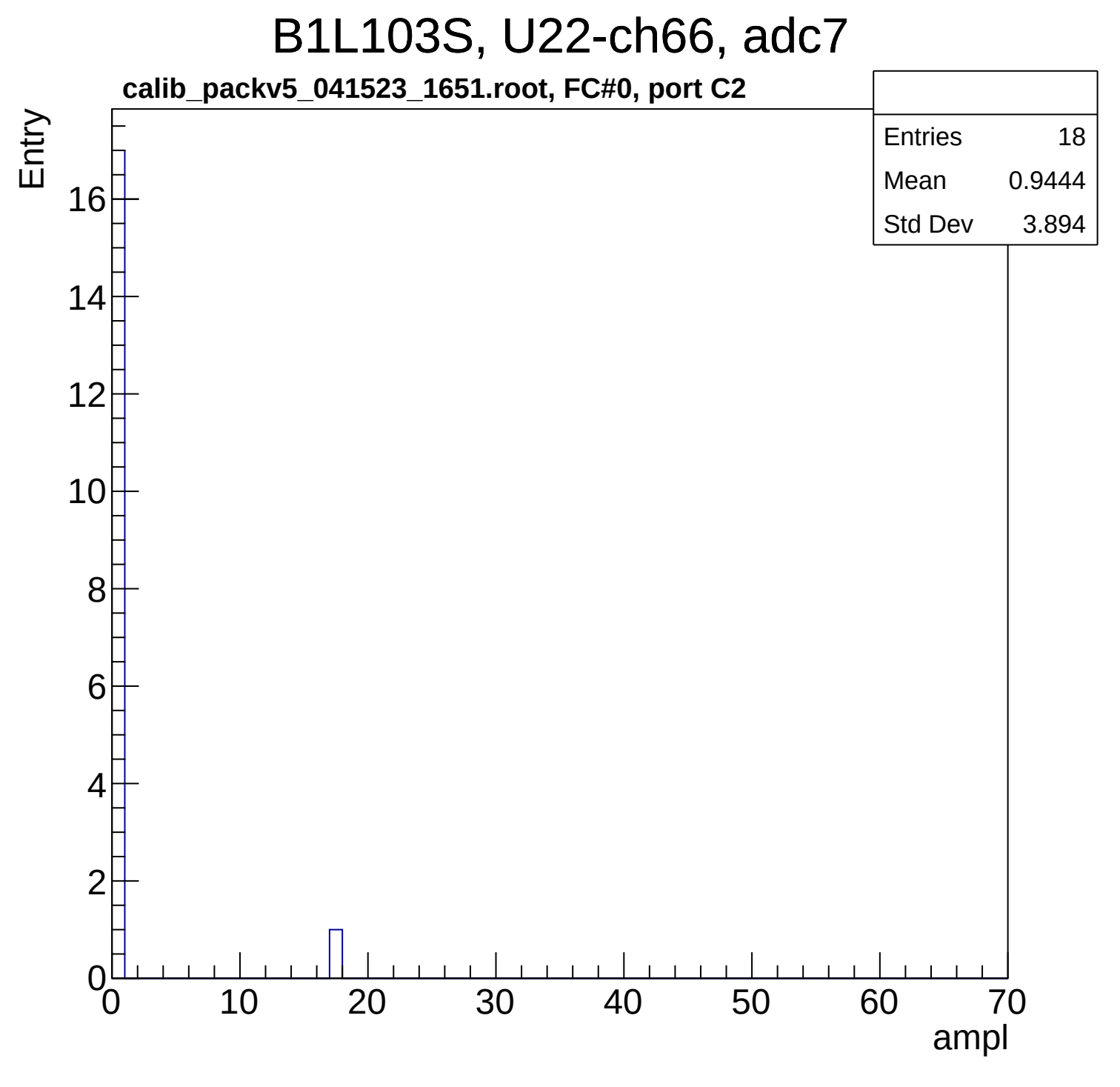
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U22-ch66, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0.9444
Std Dev 3.894
Entry
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4
6
8
10
12
14
16
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10
20
30
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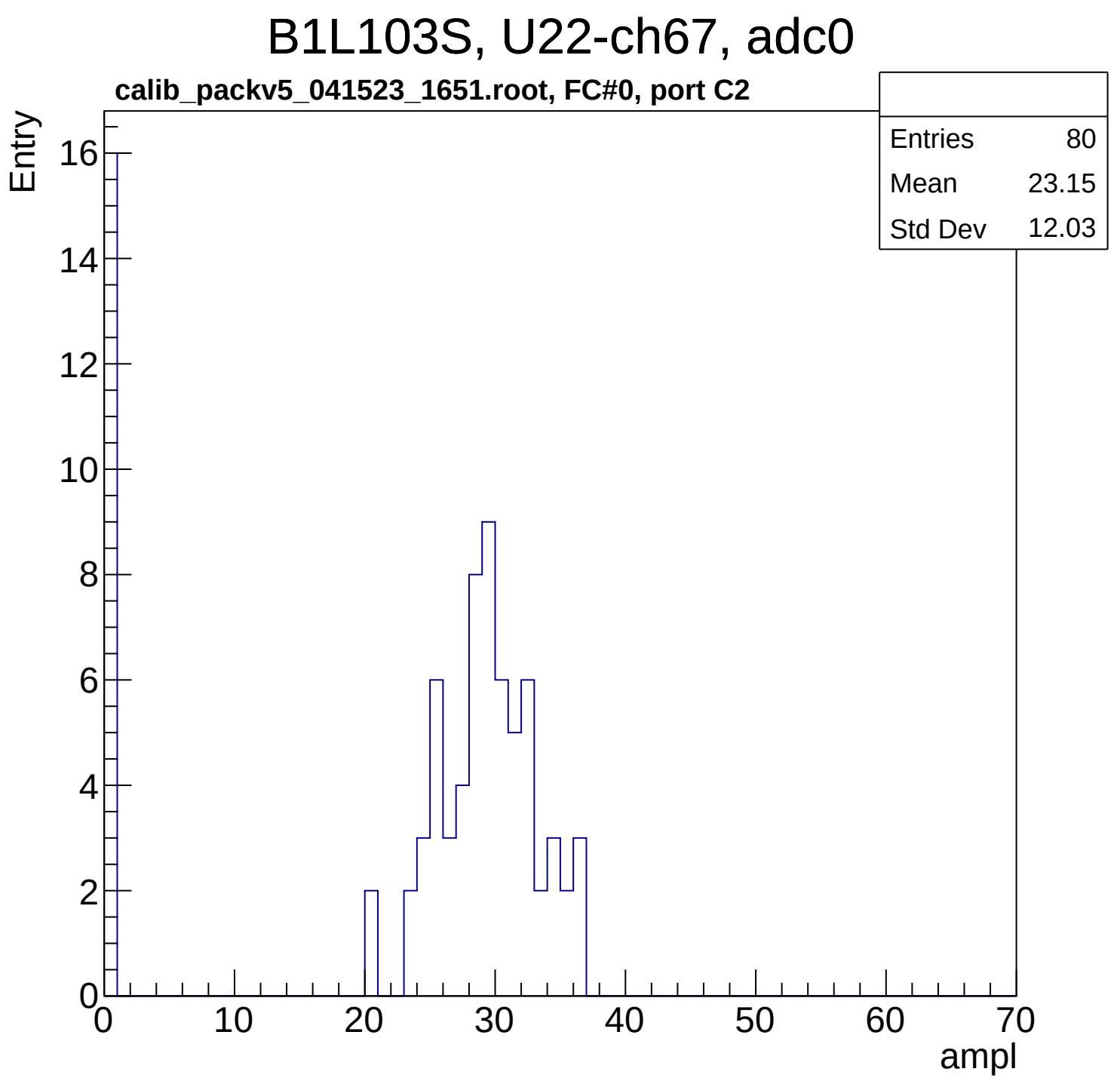
50
60
70
ampl


B1L103S, U22-ch67, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 23.15
Std Dev 12.03
Entry
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4
6
8
10
12
14
16
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10
20
30
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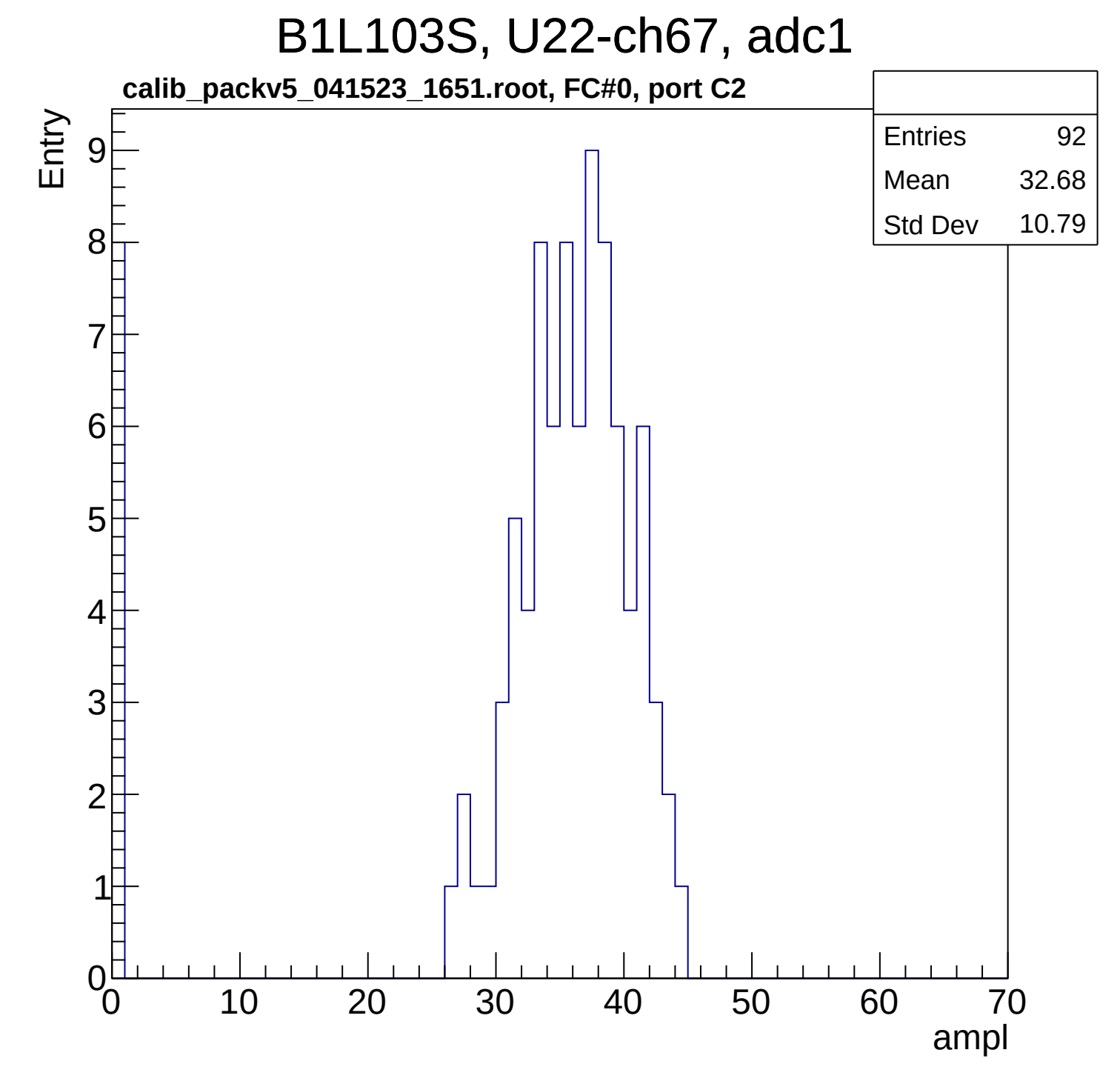
50
60
70
ampl


B1L103S, U22-ch67, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 32.68
Std Dev 10.79
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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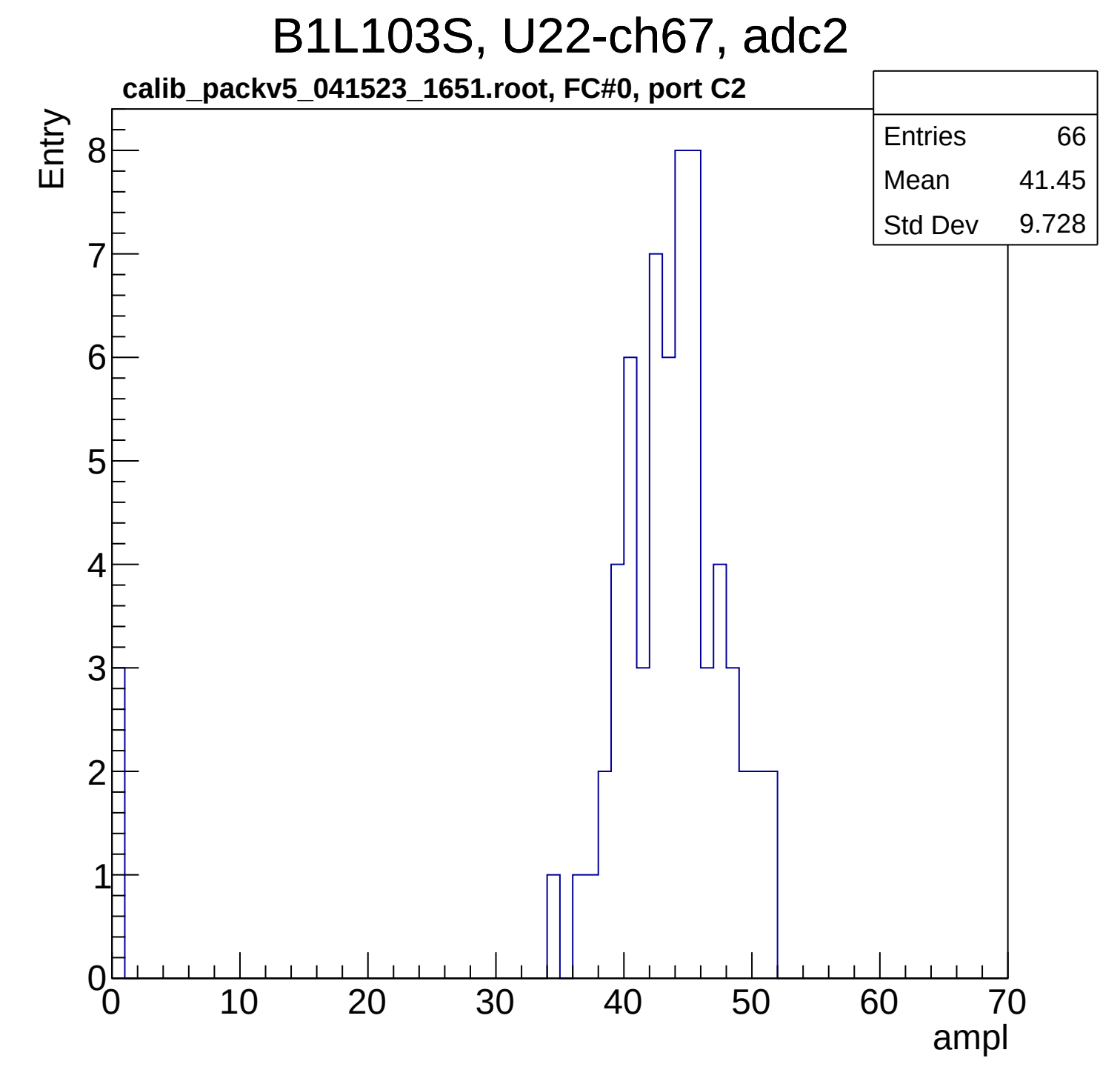
40
50
60
70


B1L103S, U22-ch67, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 41.45
Std Dev 9.728
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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40
50
60
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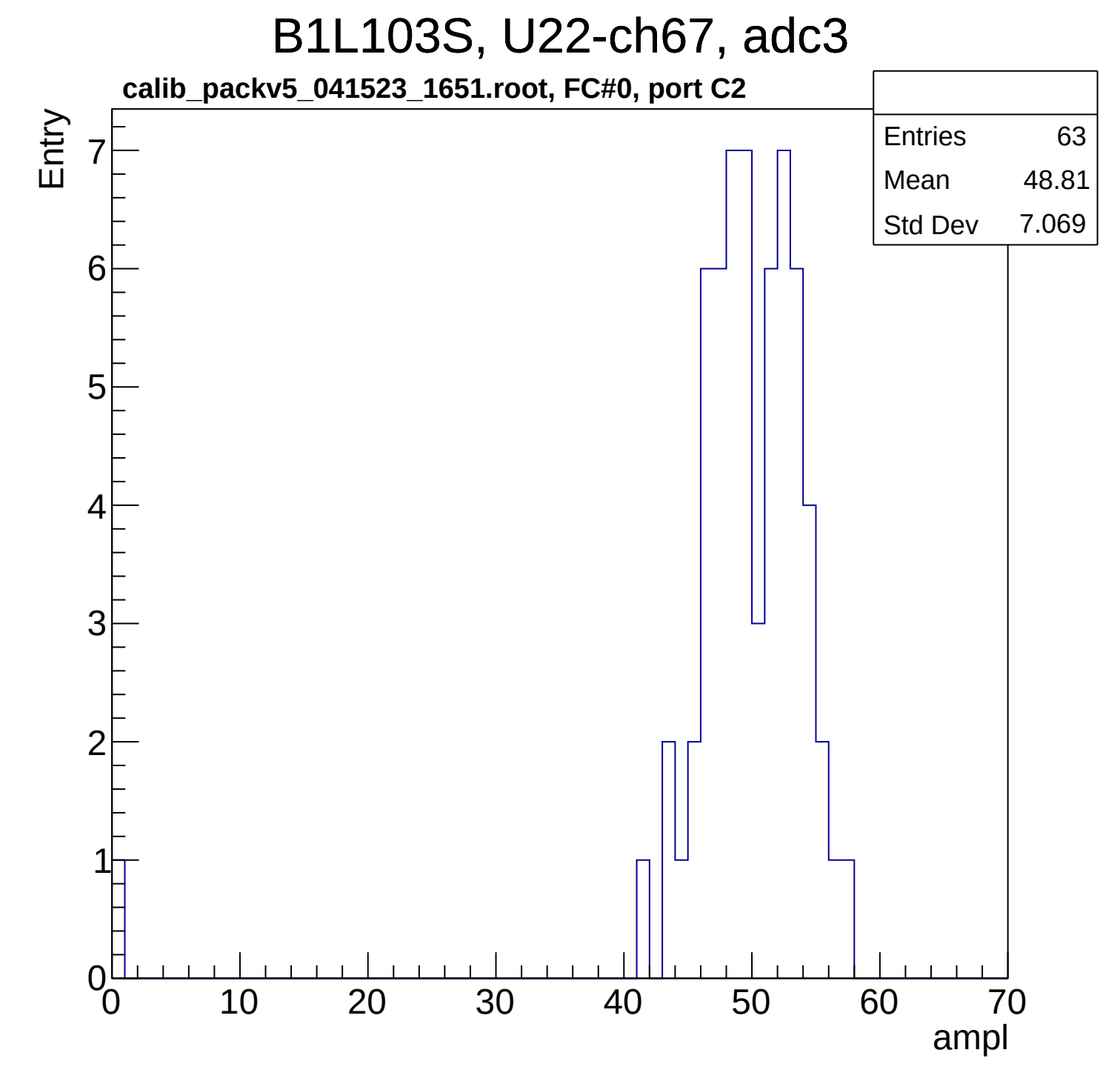
B1L103S, U22-ch67, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 48.81
Std Dev 7.069
Entry
ampl
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2
3
4
5
6
7
0
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20
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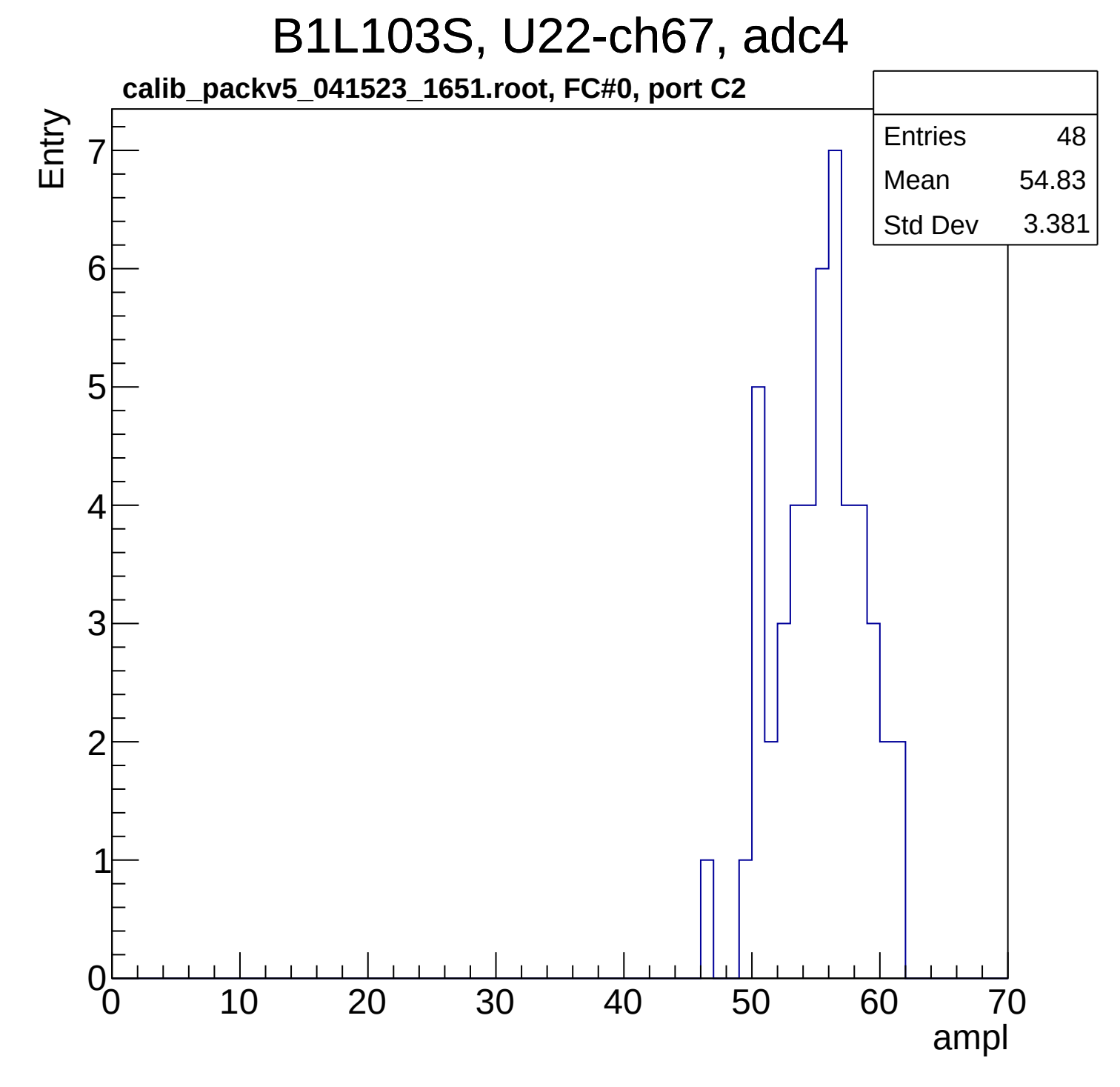
40
50
60
70


B1L103S, U22-ch67, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 54.83
Std Dev 3.381
Entry
ampl
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0
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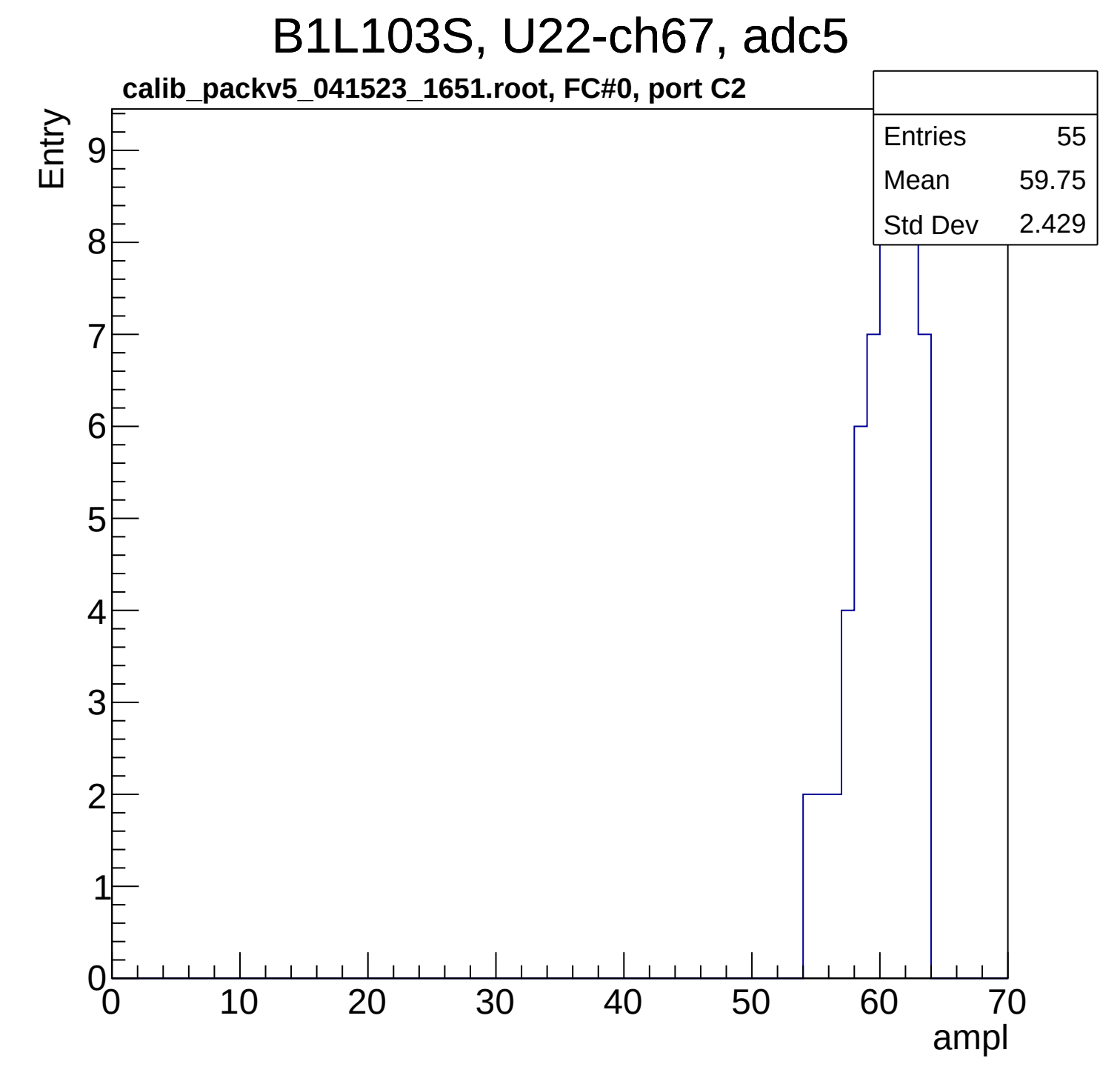
40
50
60
70


B1L103S, U22-ch67, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 59.75
Std Dev 2.429
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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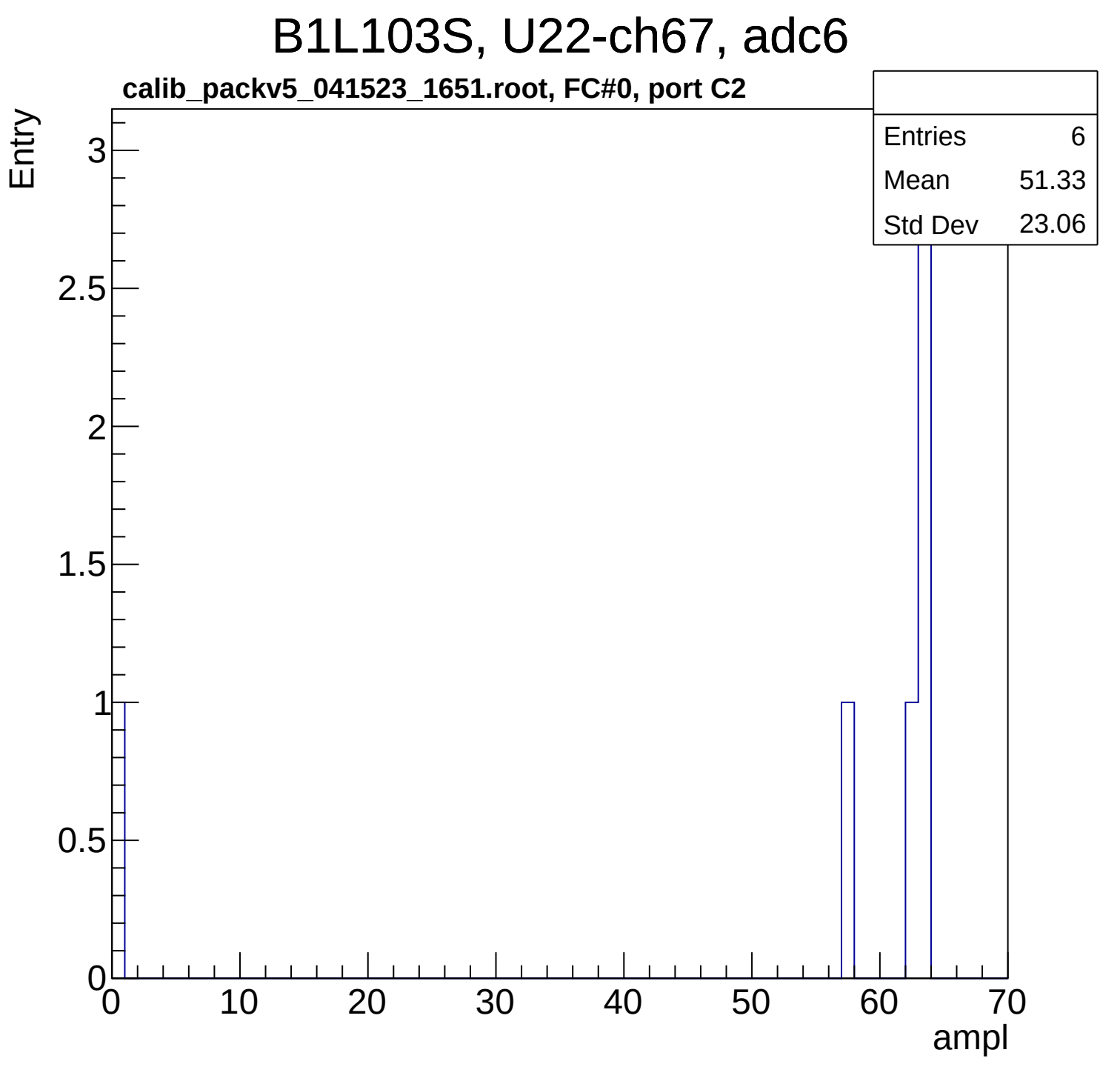
60
70


B1L103S, U22-ch67, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 51.33
Std Dev 23.06
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
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20
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40
50
60
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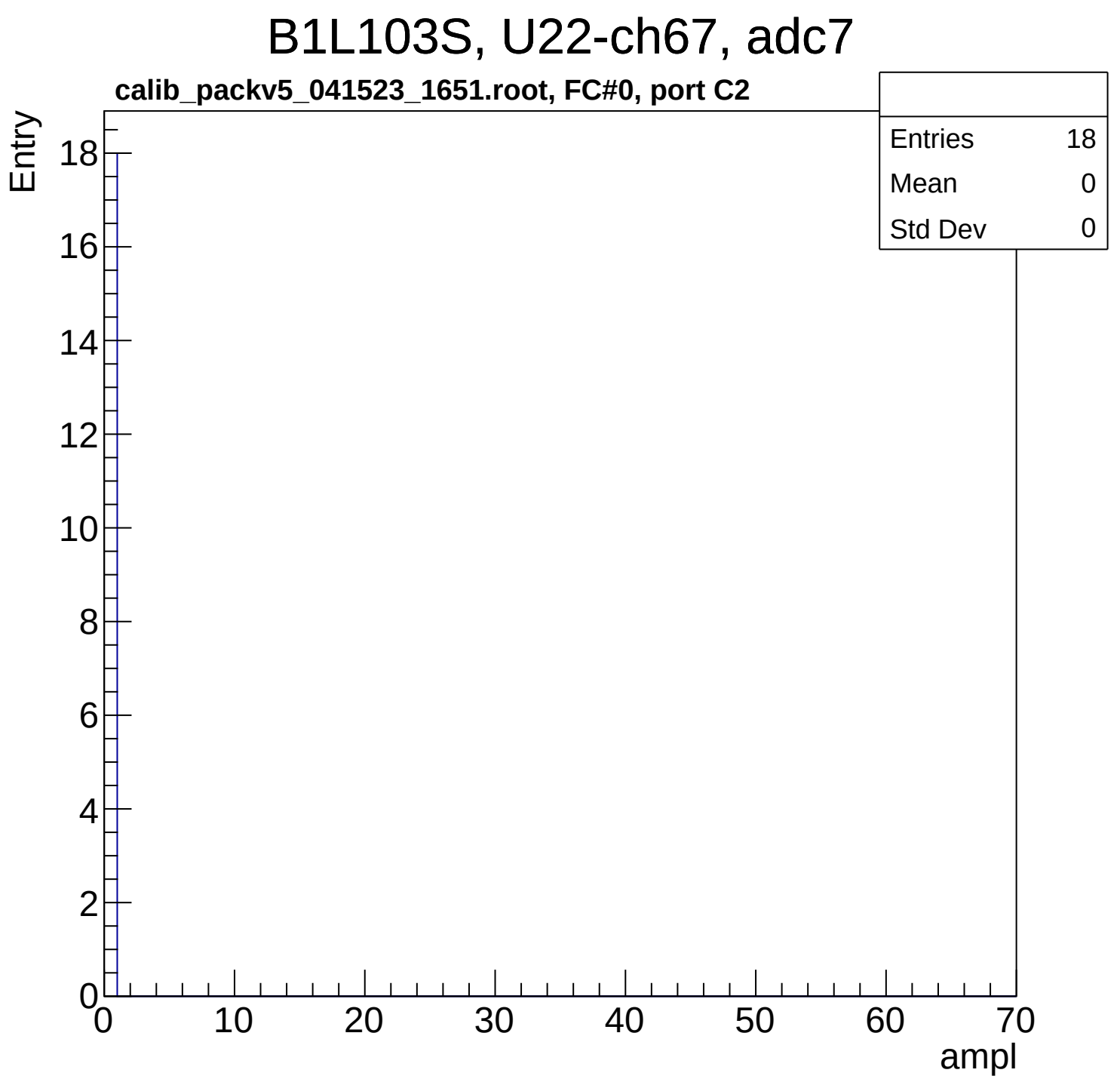
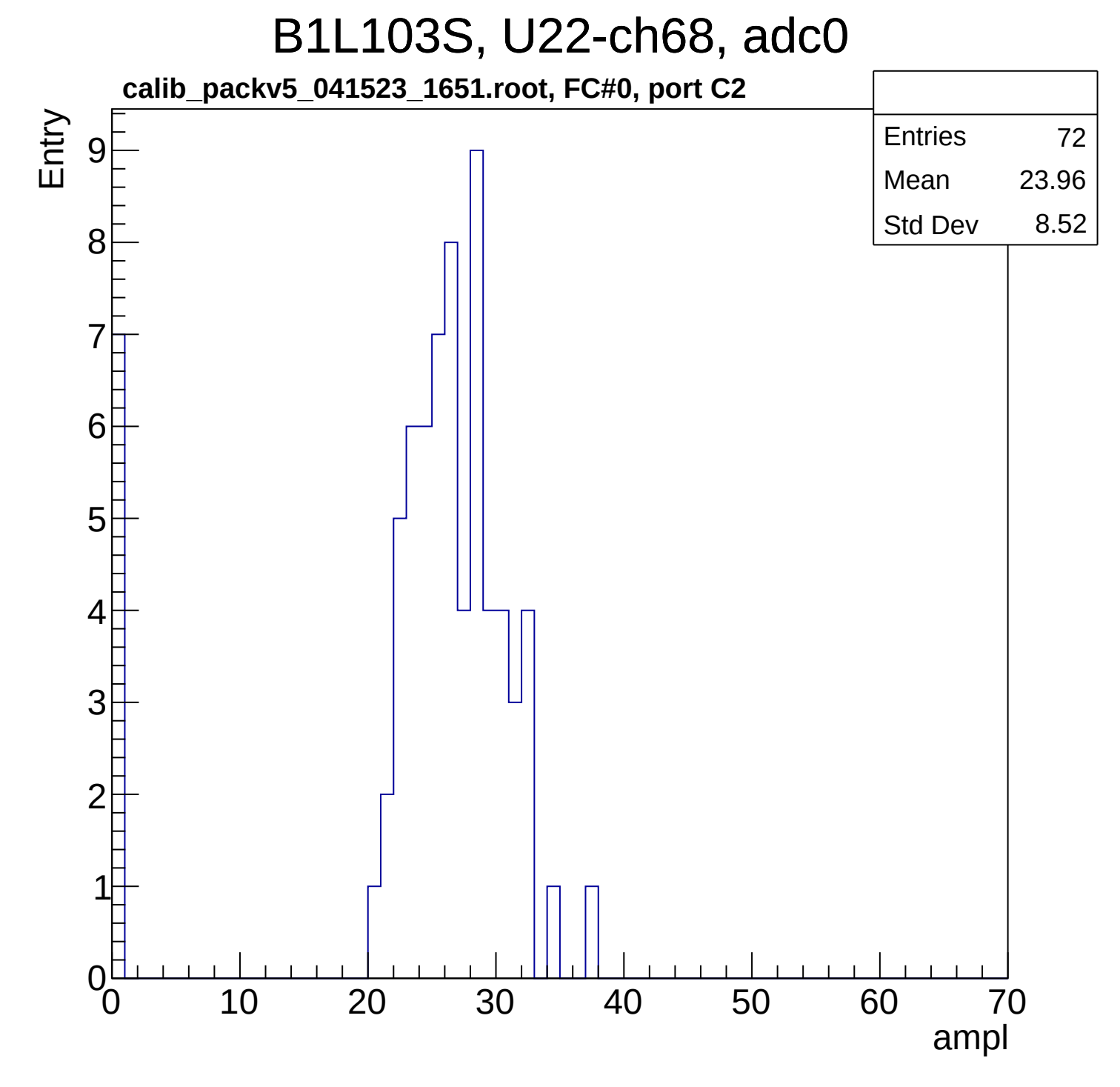
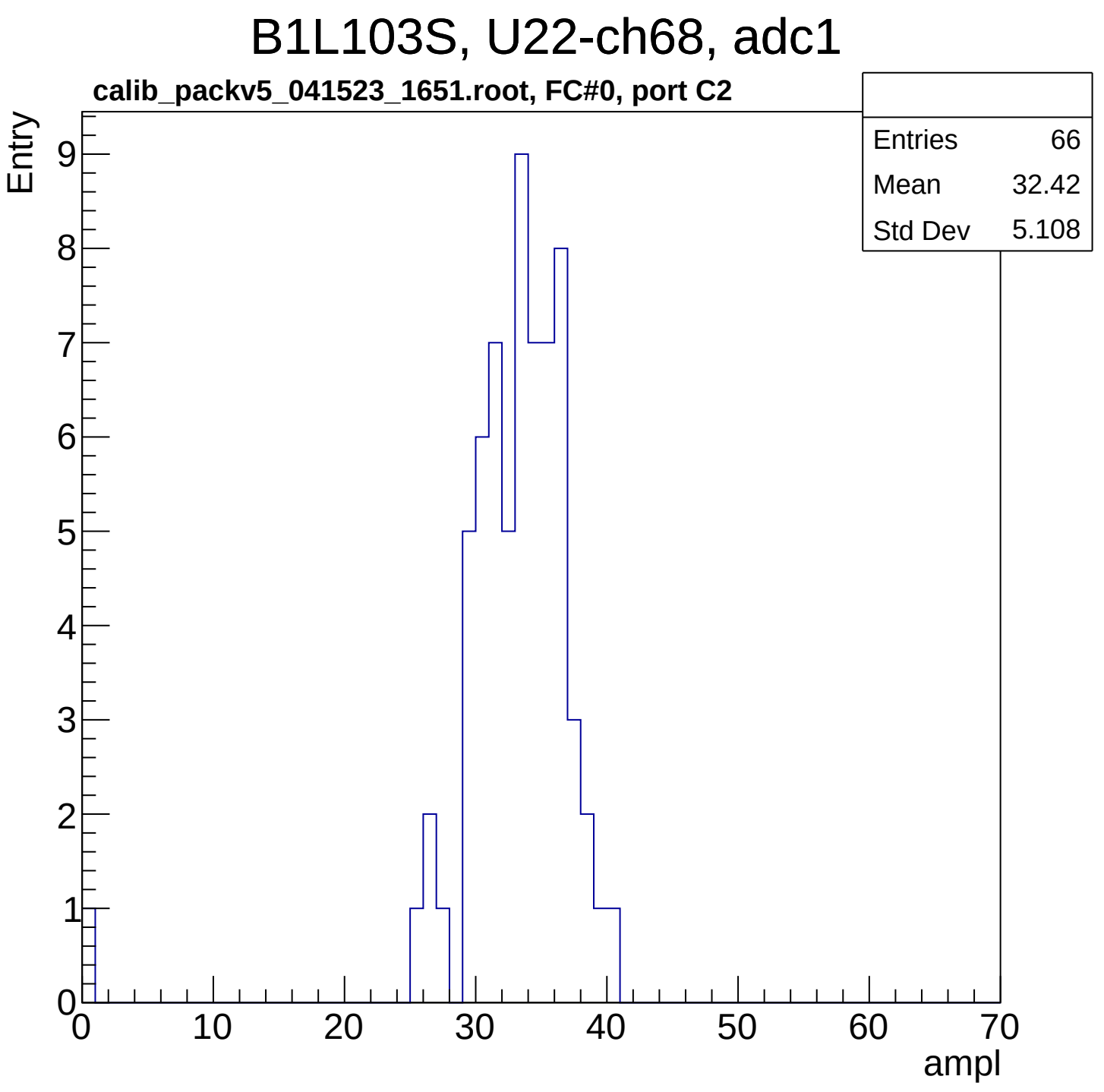

B1L103S, U22-ch67, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch68, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 23.96
Std Dev 8.52
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch68, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 32.42
Std Dev 5.108
Entry
ampl
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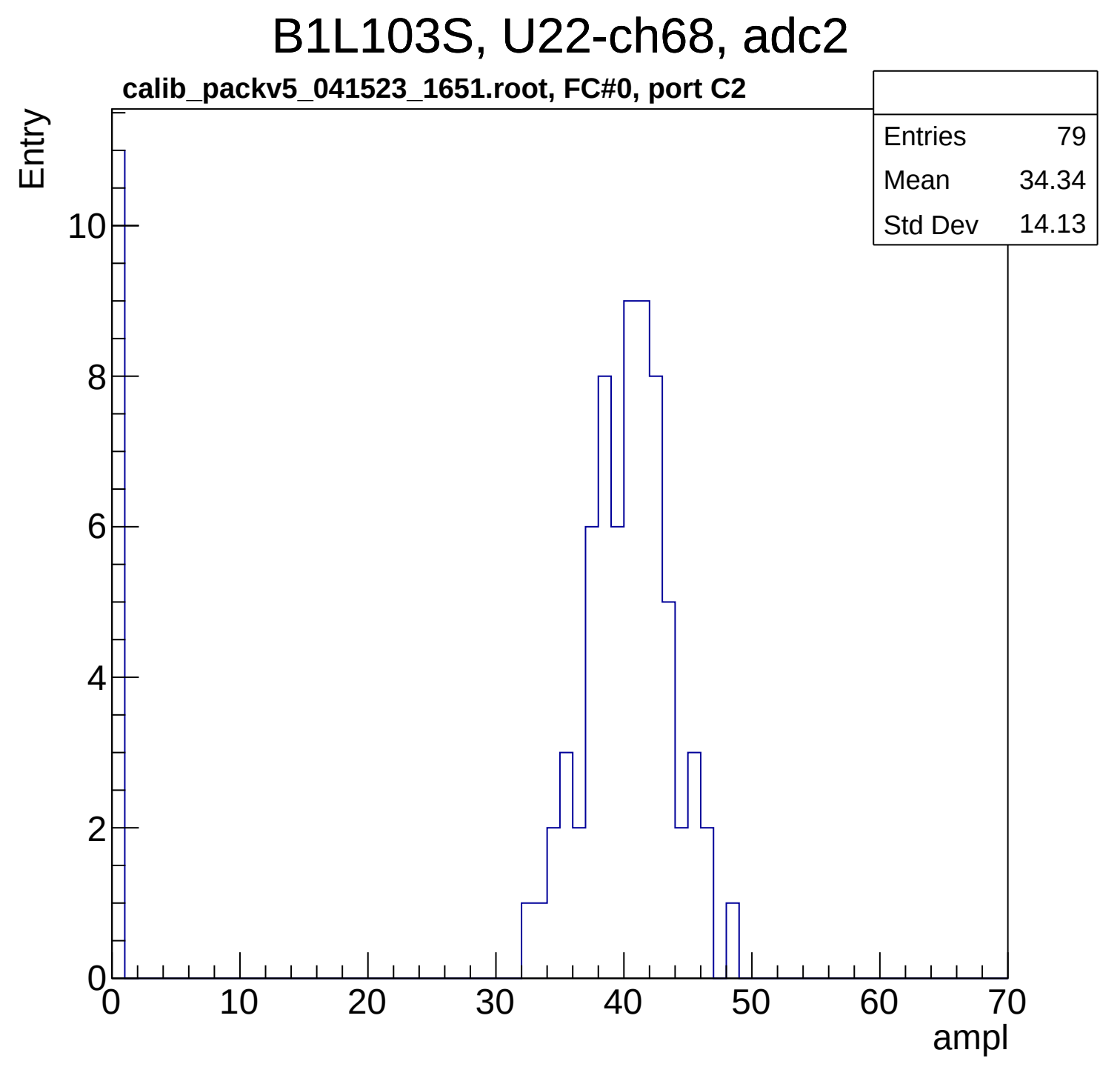
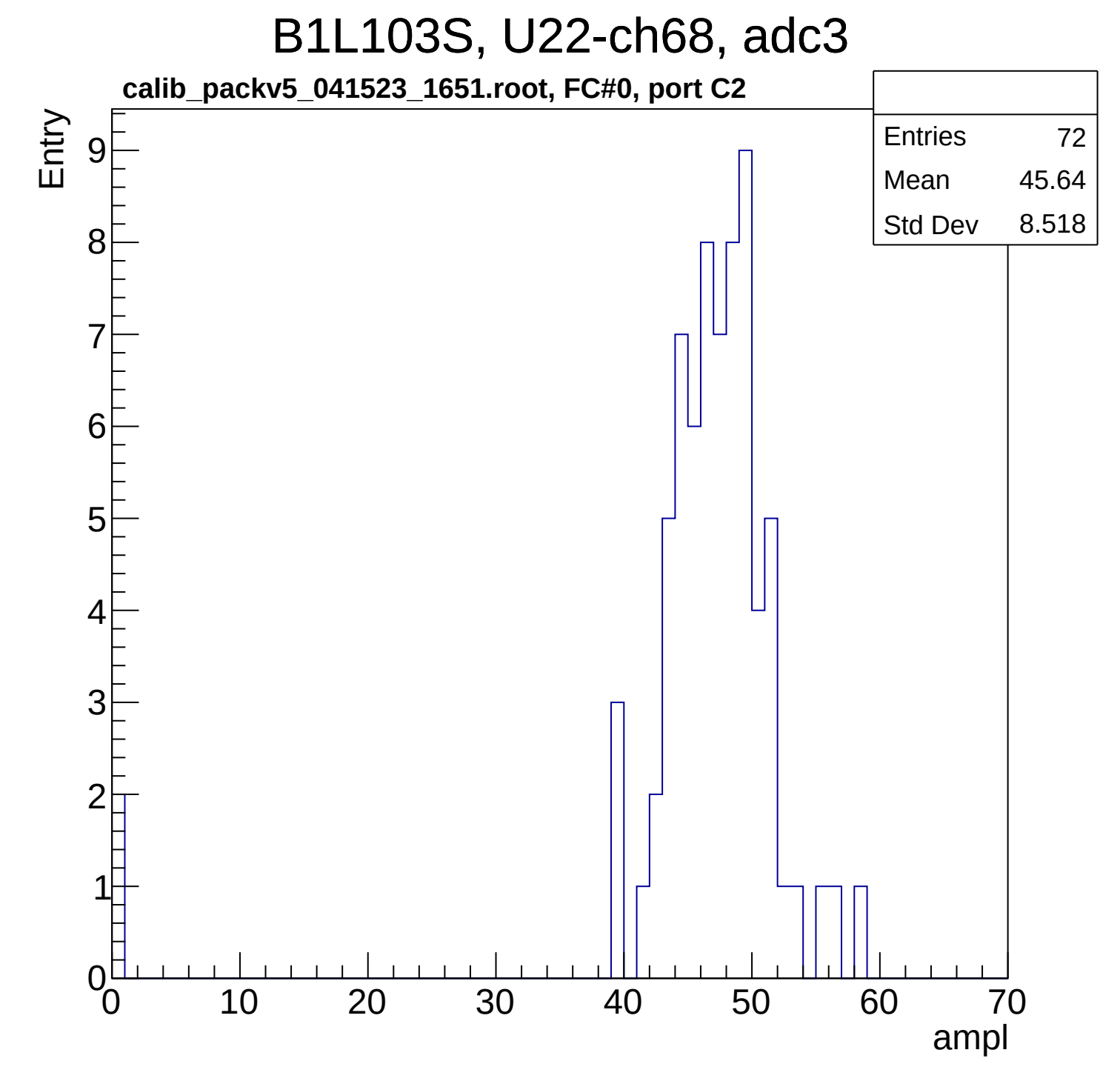
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch68, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 34.34
Std Dev 14.13
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch68, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 45.64
Std Dev 8.518
Entry
ampl
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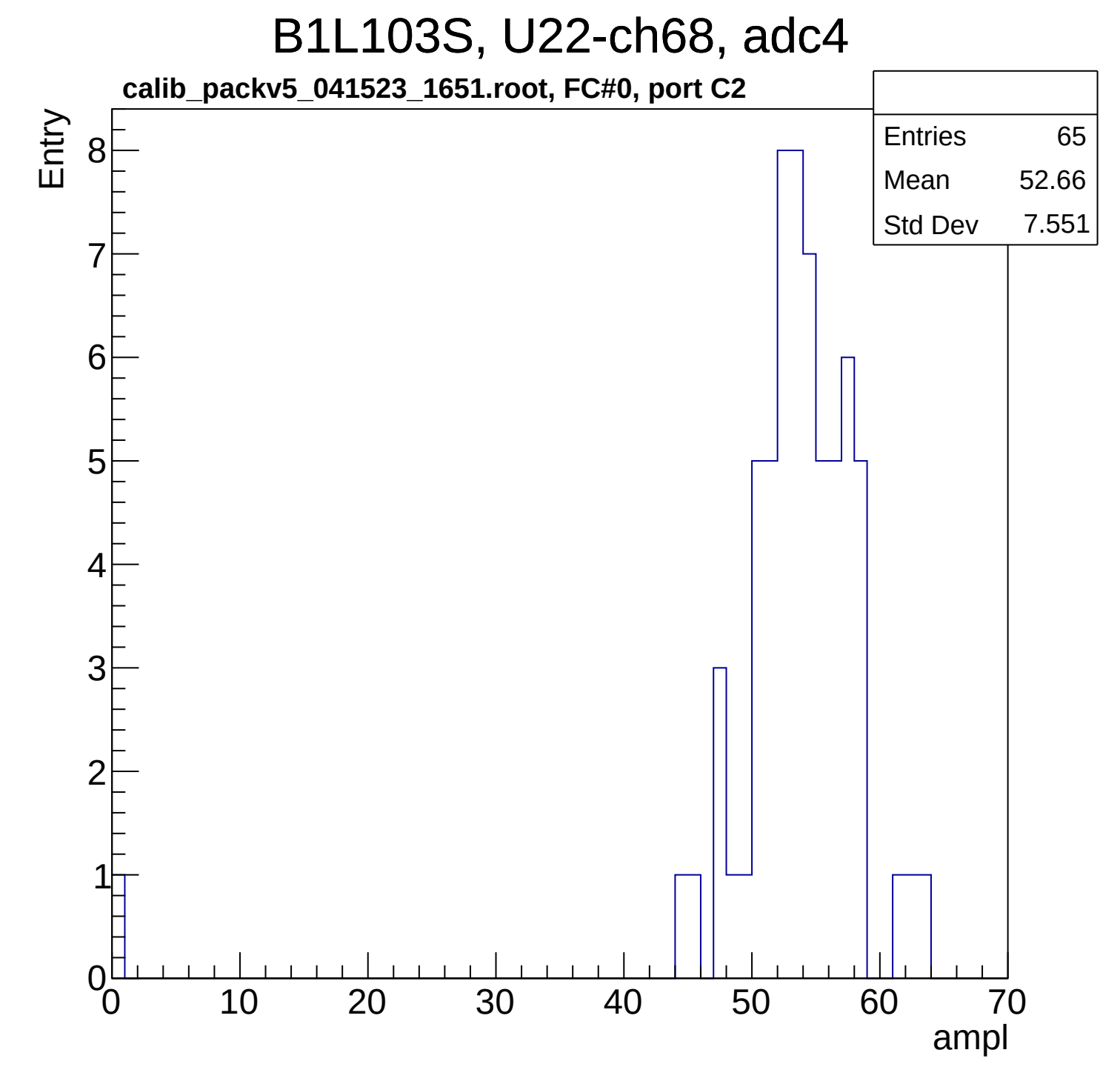
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch68, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 52.66
Std Dev 7.551
Entry
ampl
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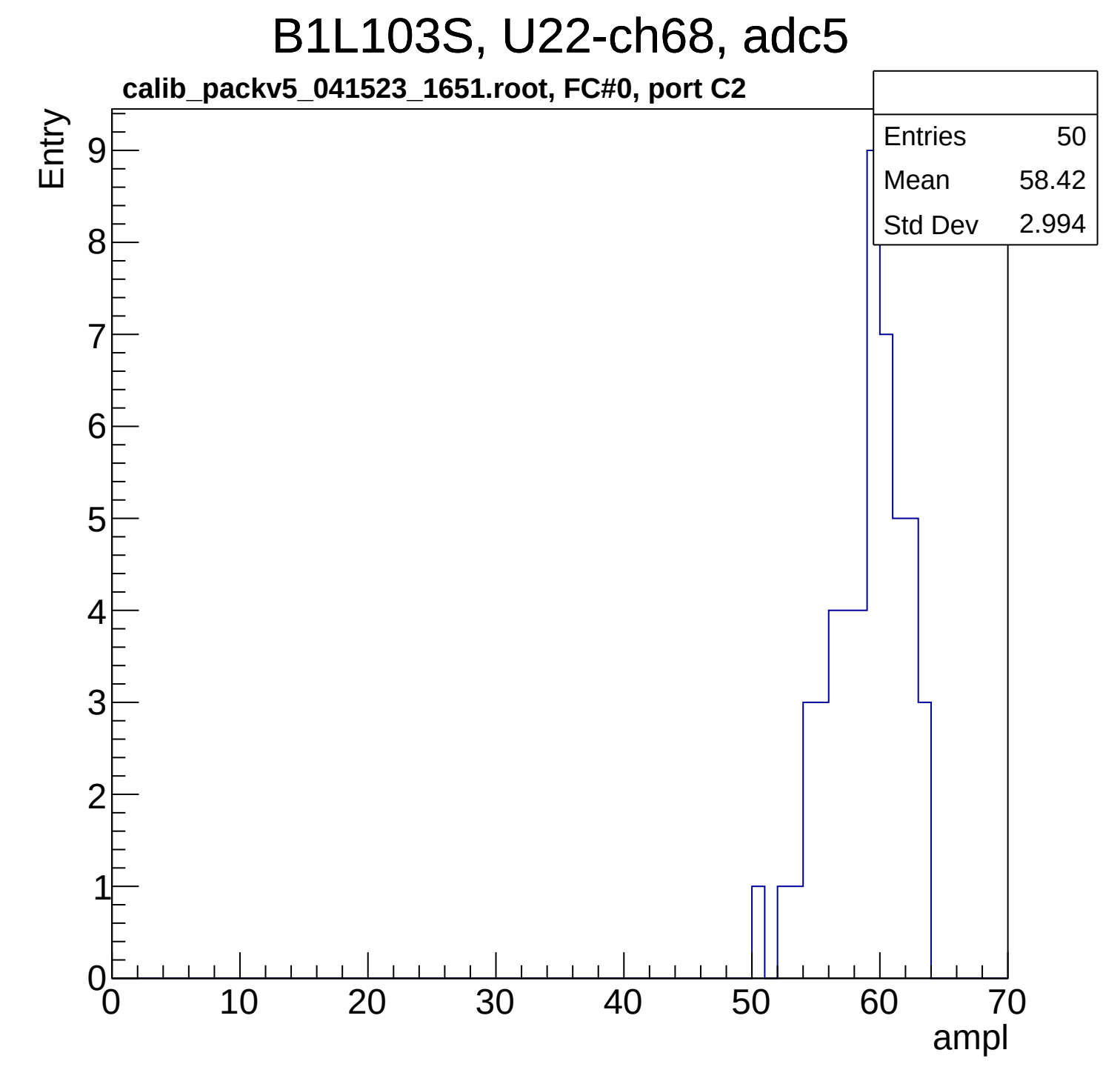
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch68, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 58.42
Std Dev 2.994
Entry
ampl
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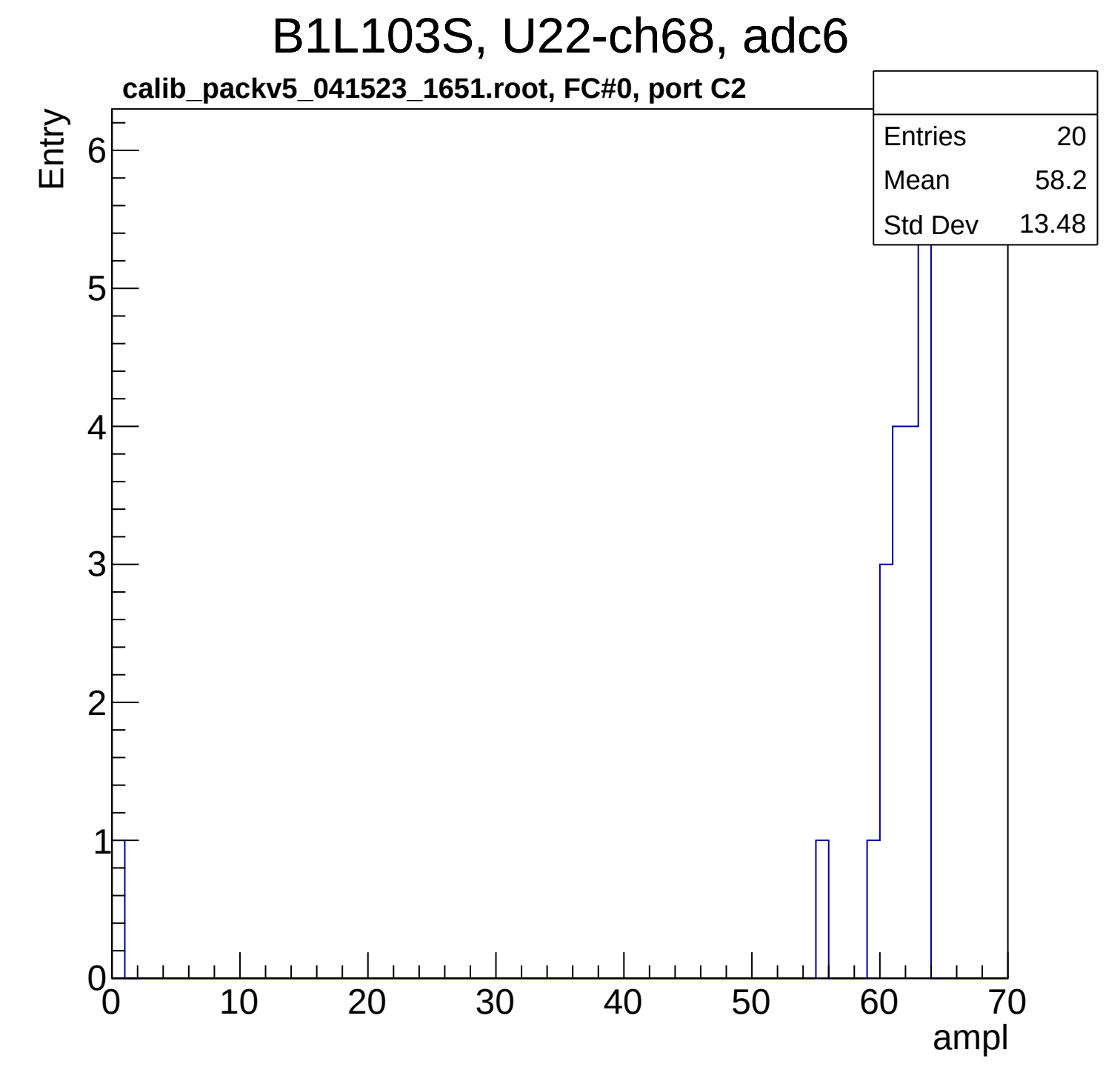
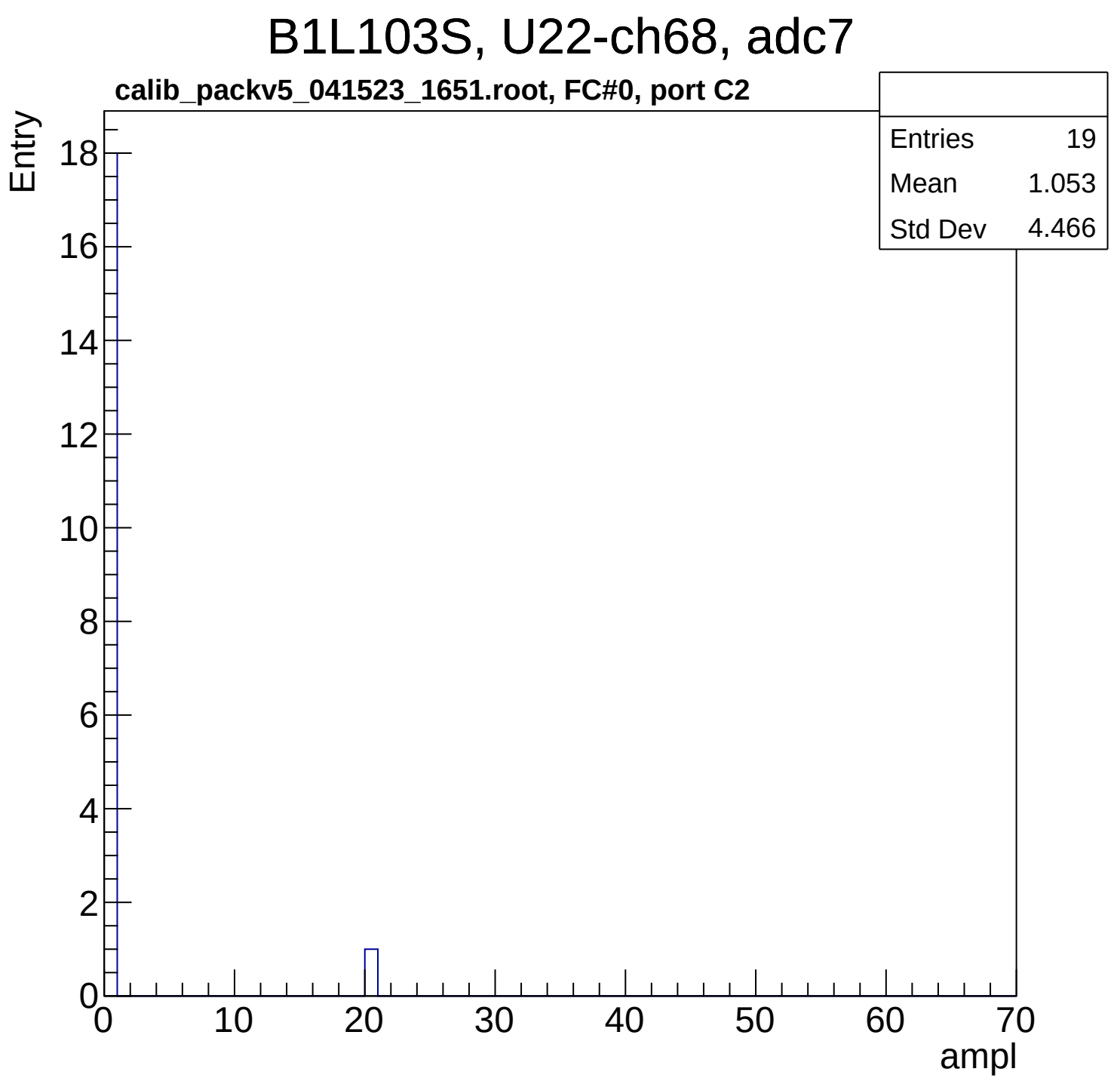
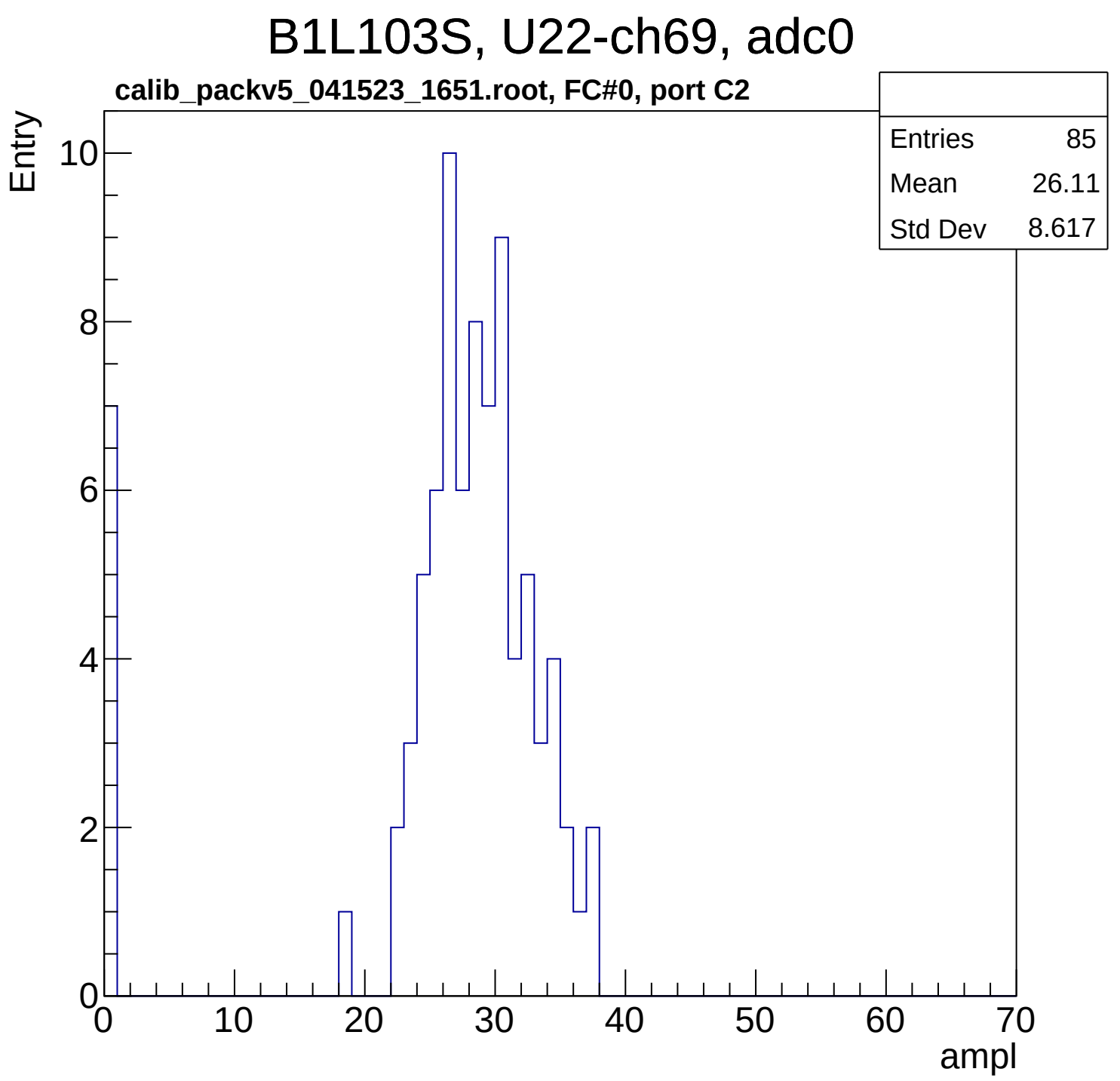
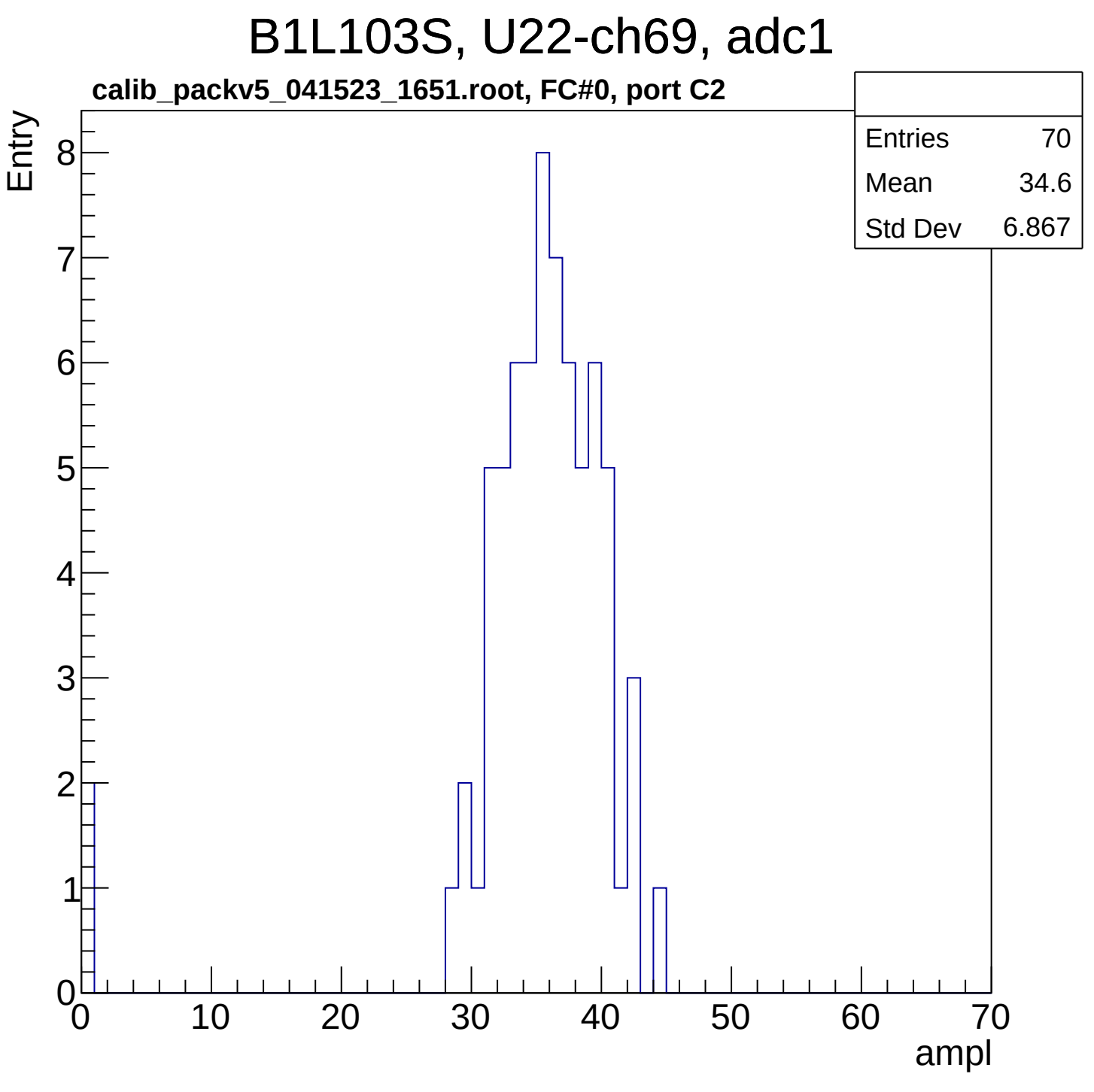
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch68, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 58.2
Std Dev 13.48
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch68, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.053
Std Dev 4.466
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L103S, U22-ch69, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 26.11
Std Dev 8.617
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U22-ch69, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 34.6
Std Dev 6.867
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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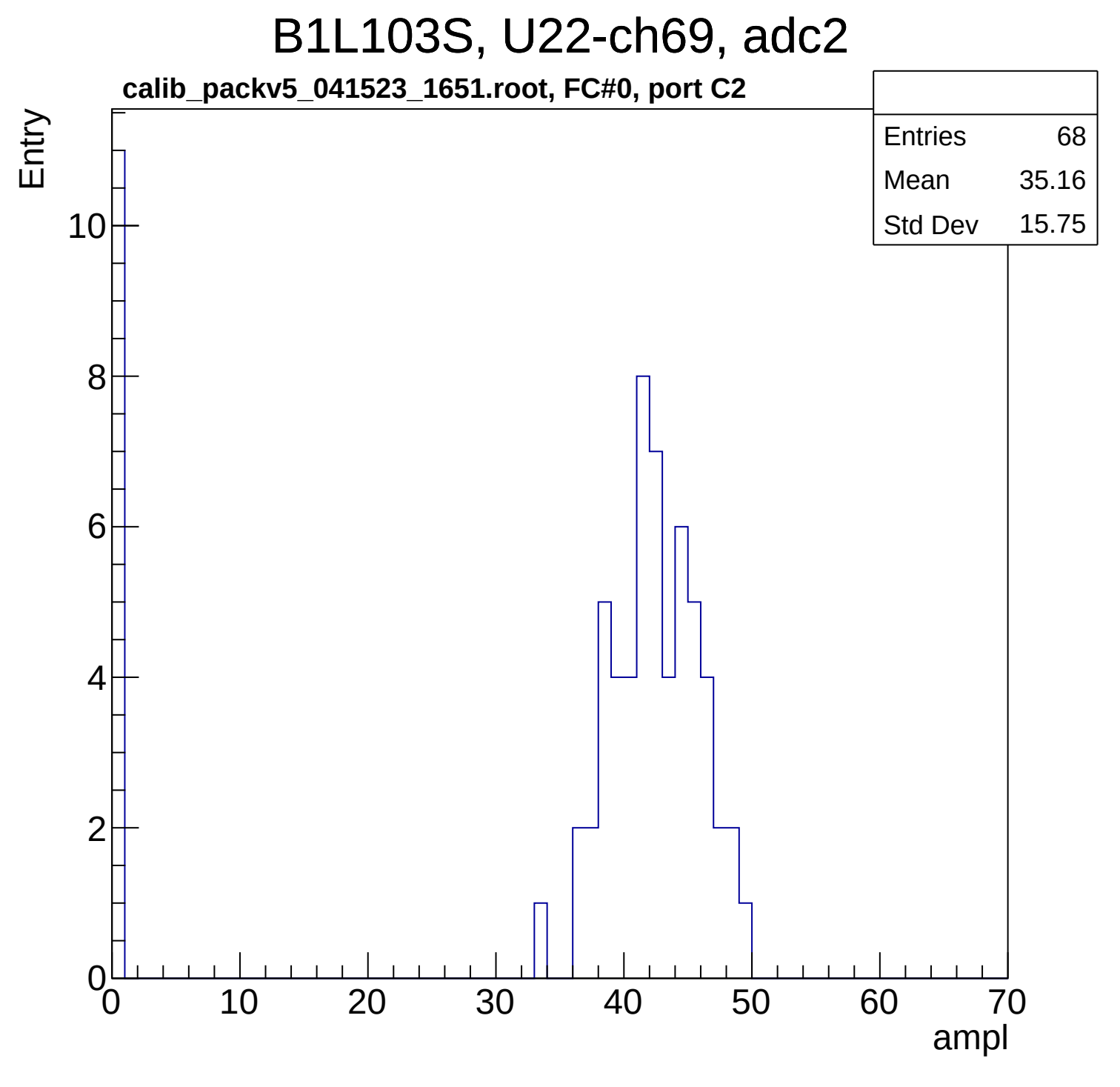
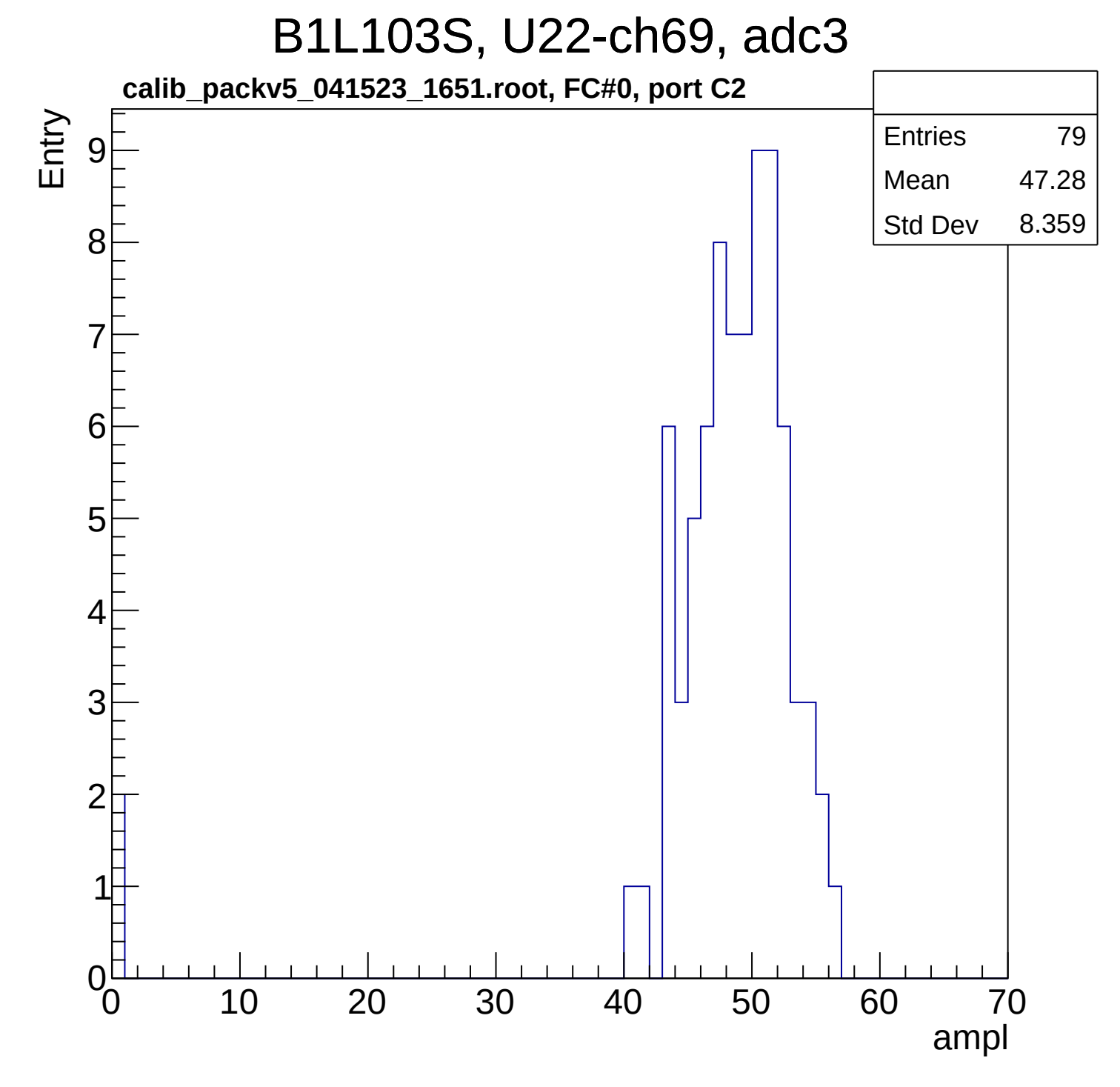

B1L103S, U22-ch69, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 35.16
Std Dev 15.75
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch69, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 47.28
Std Dev 8.359
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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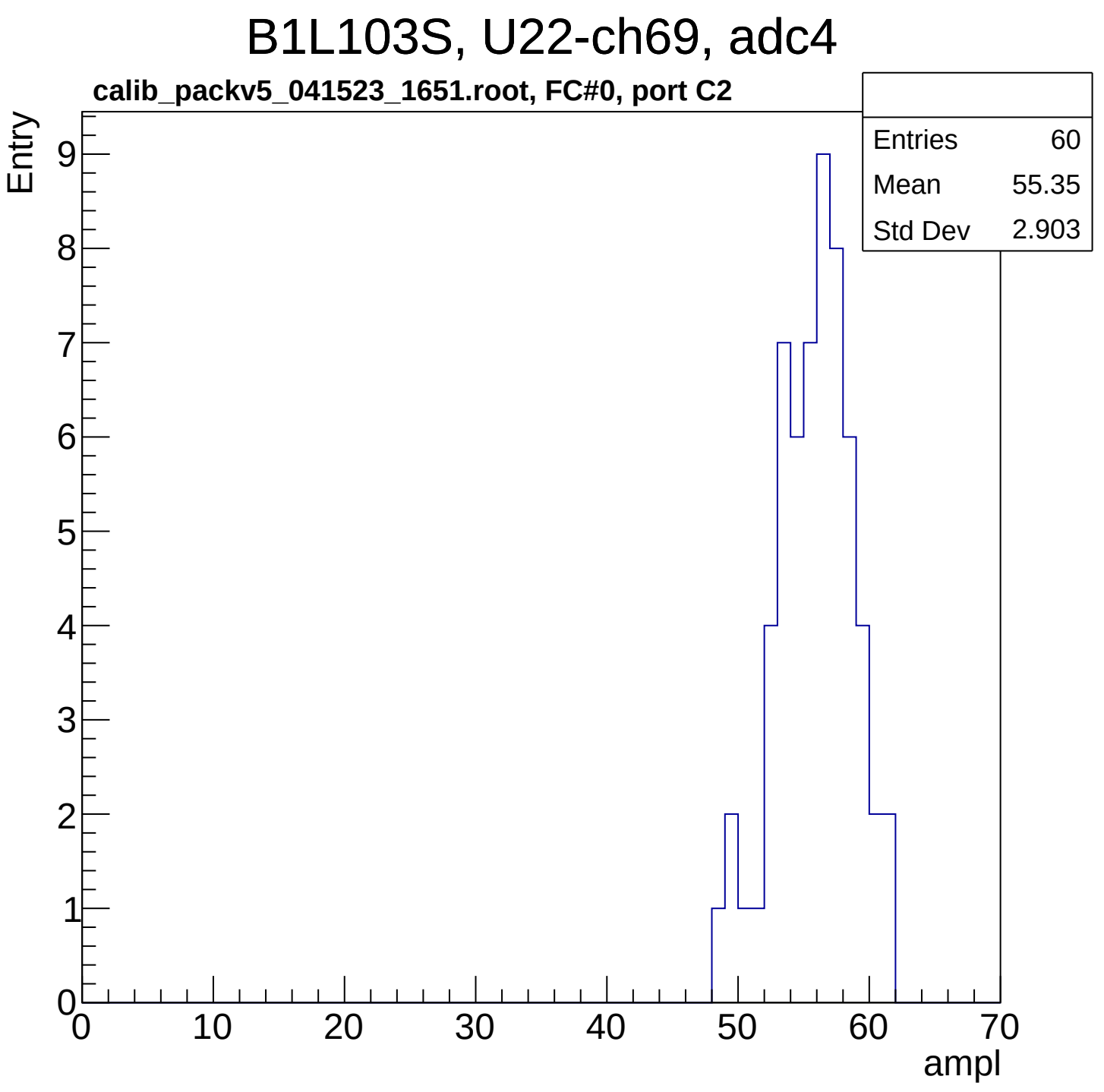
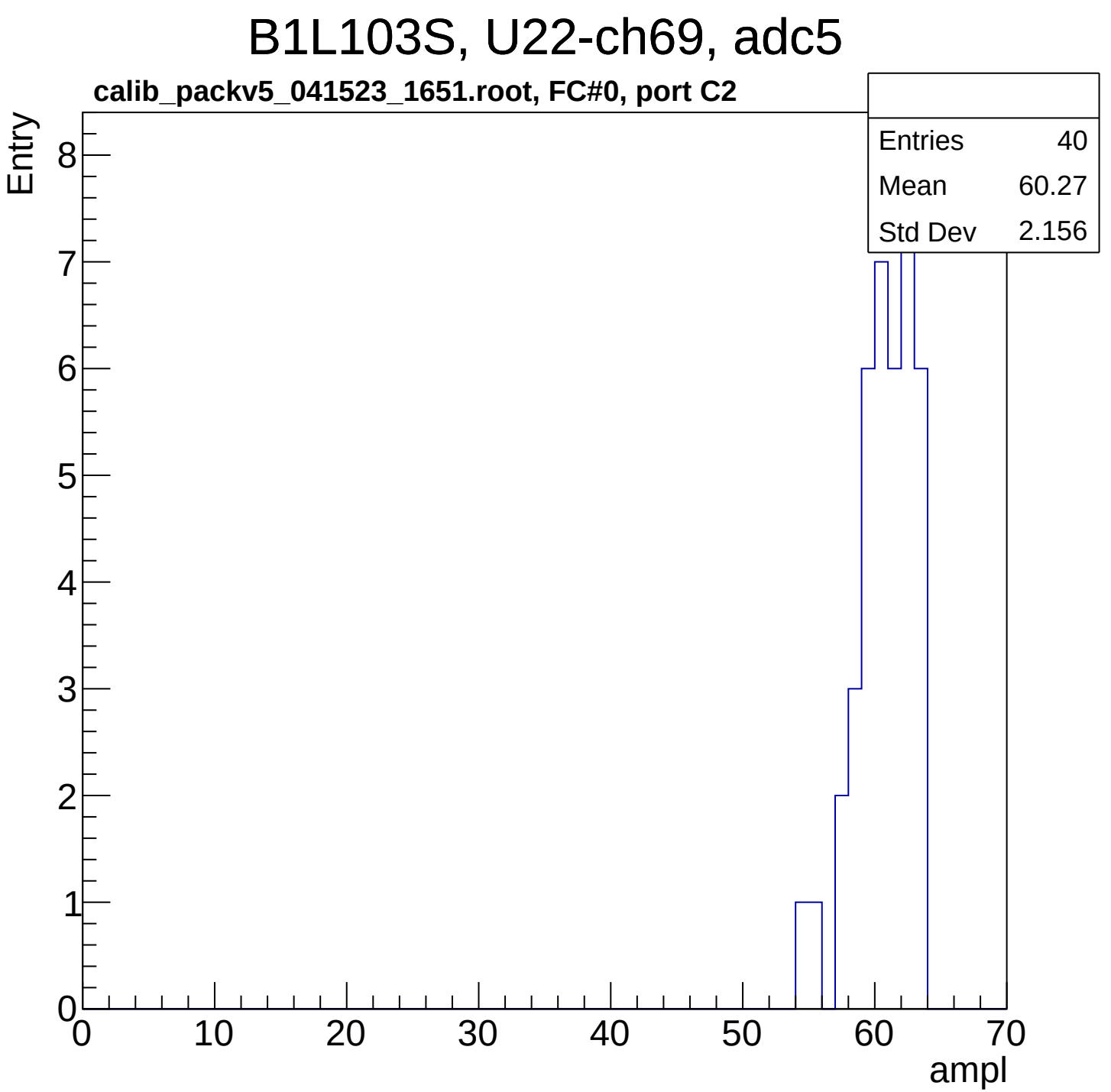
40
50
60
70


B1L103S, U22-ch69, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 55.35
Std Dev 2.903
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch69, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 60.27
Std Dev 2.156
Entry
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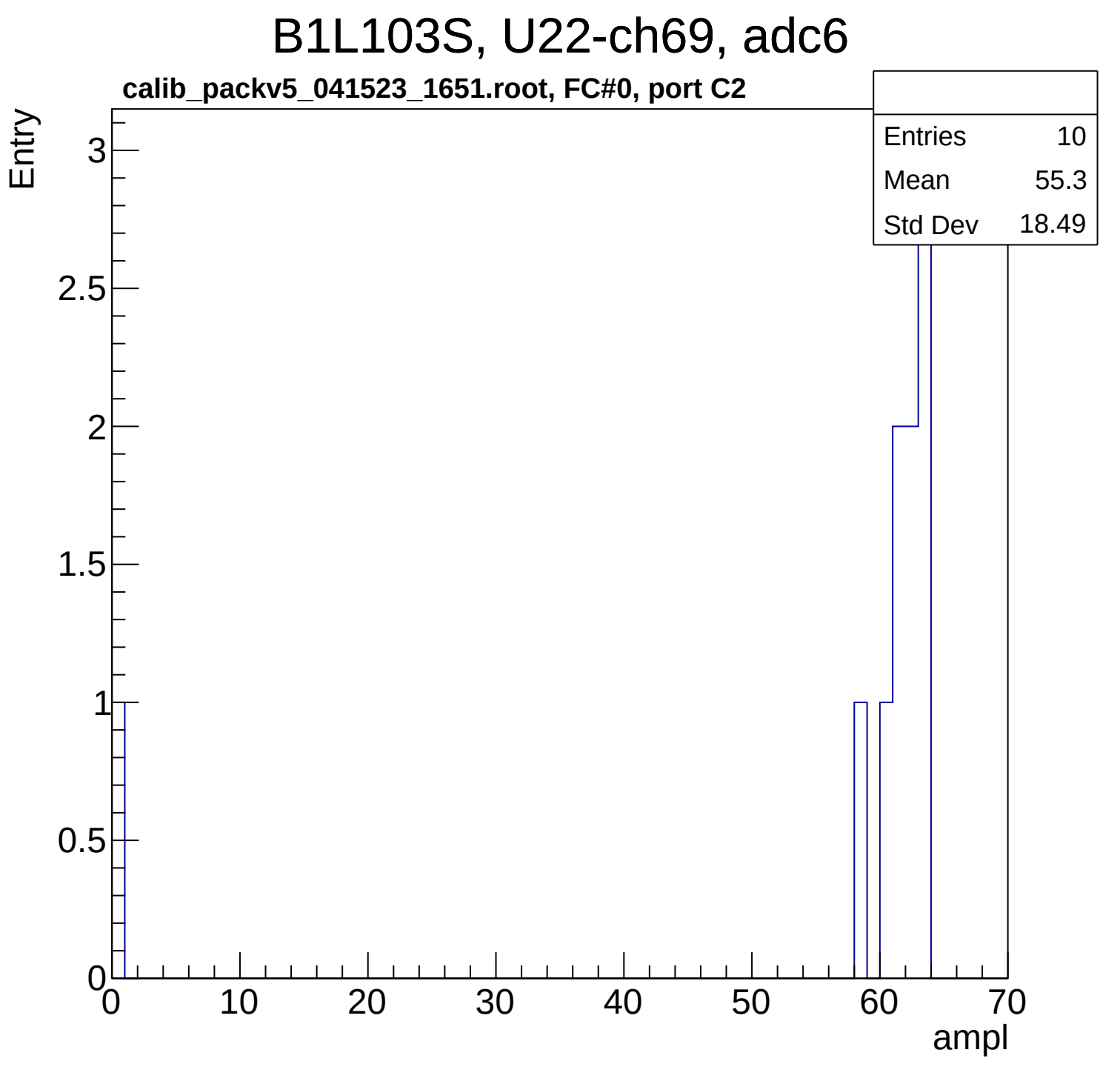
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch69, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 55.3
Std Dev 18.49
Entry
ampl
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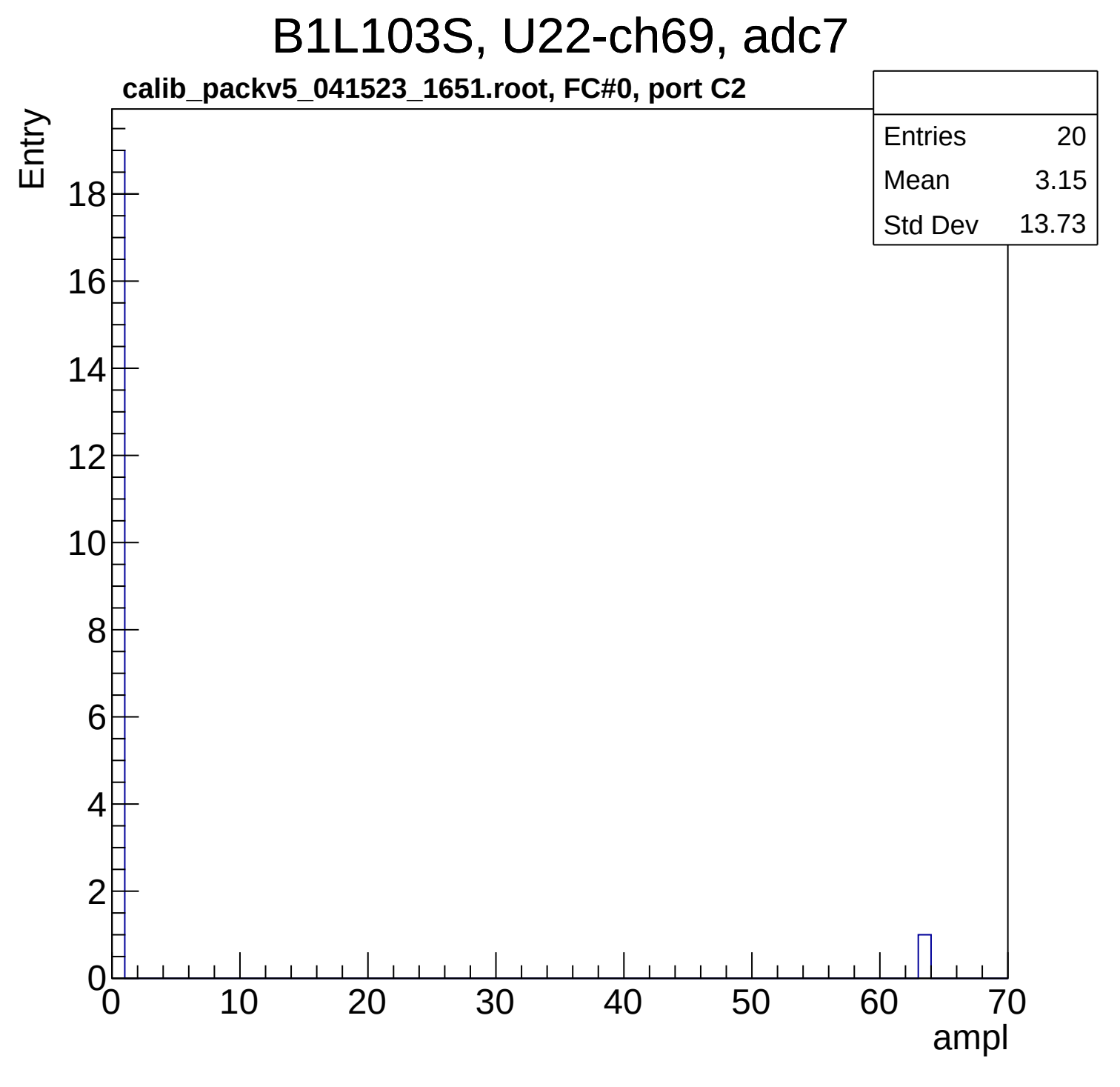
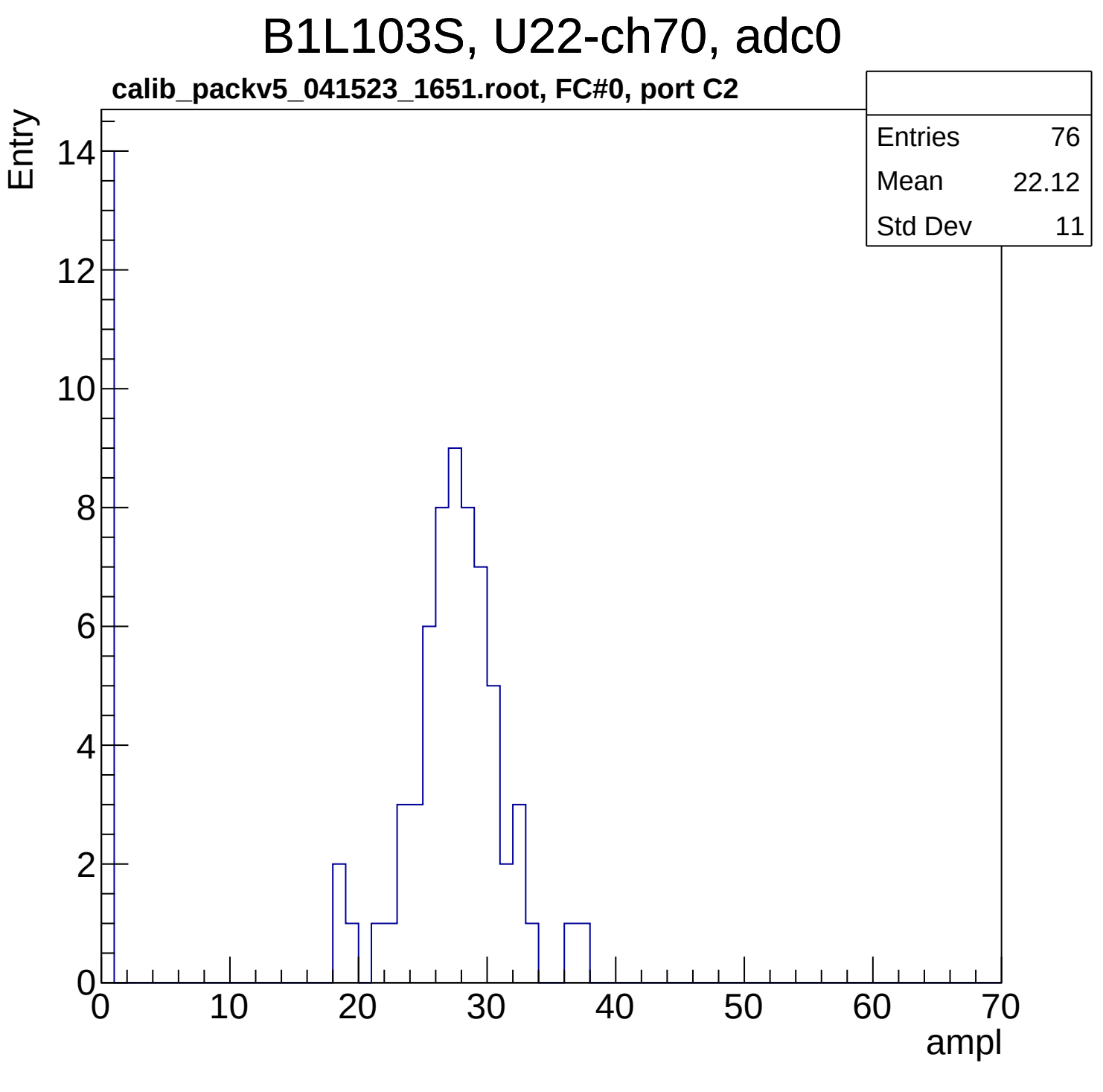
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U22-ch69, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch70, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 22.12
Std Dev 11
Entry
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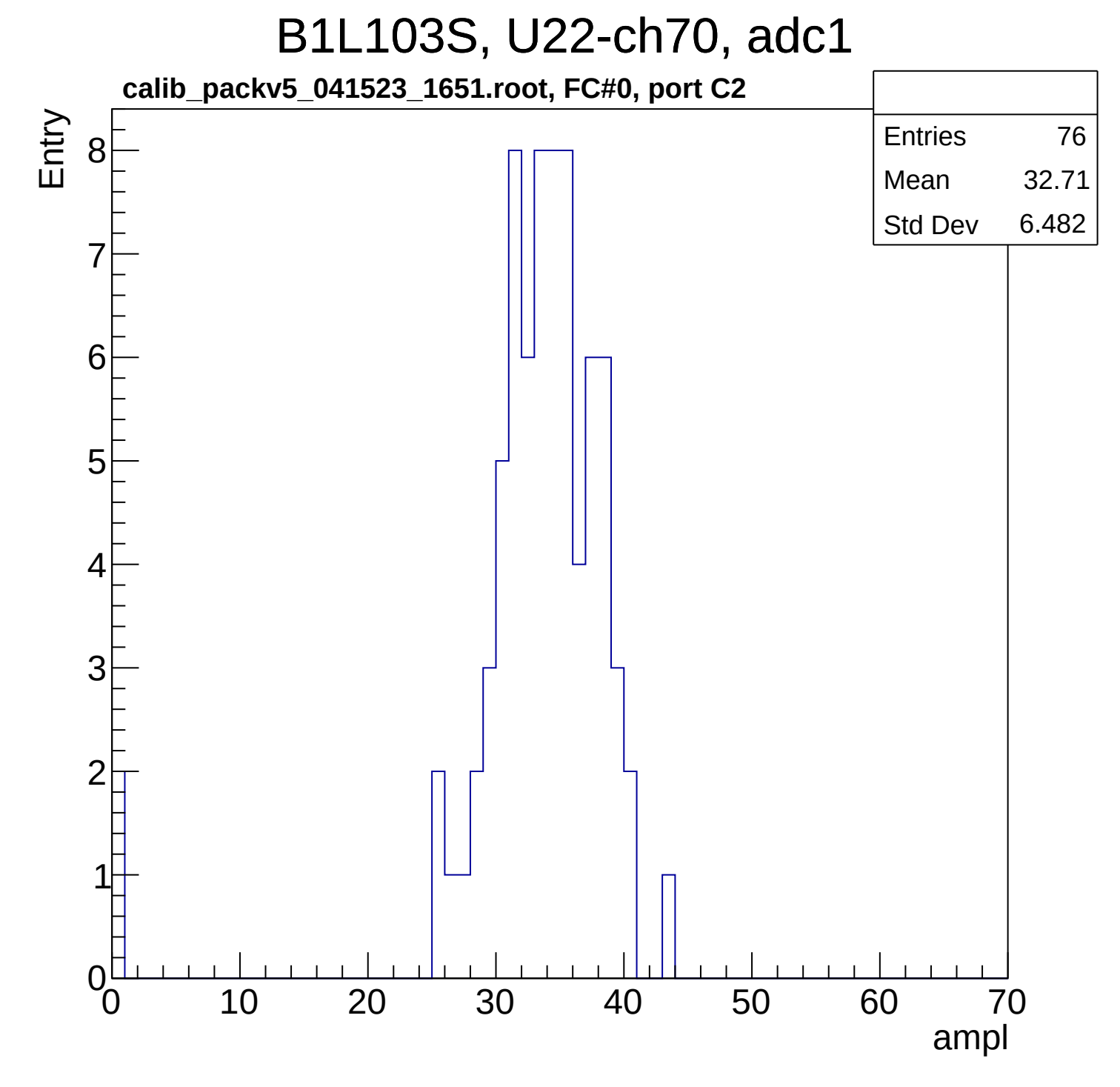
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch70, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 32.71
Std Dev 6.482
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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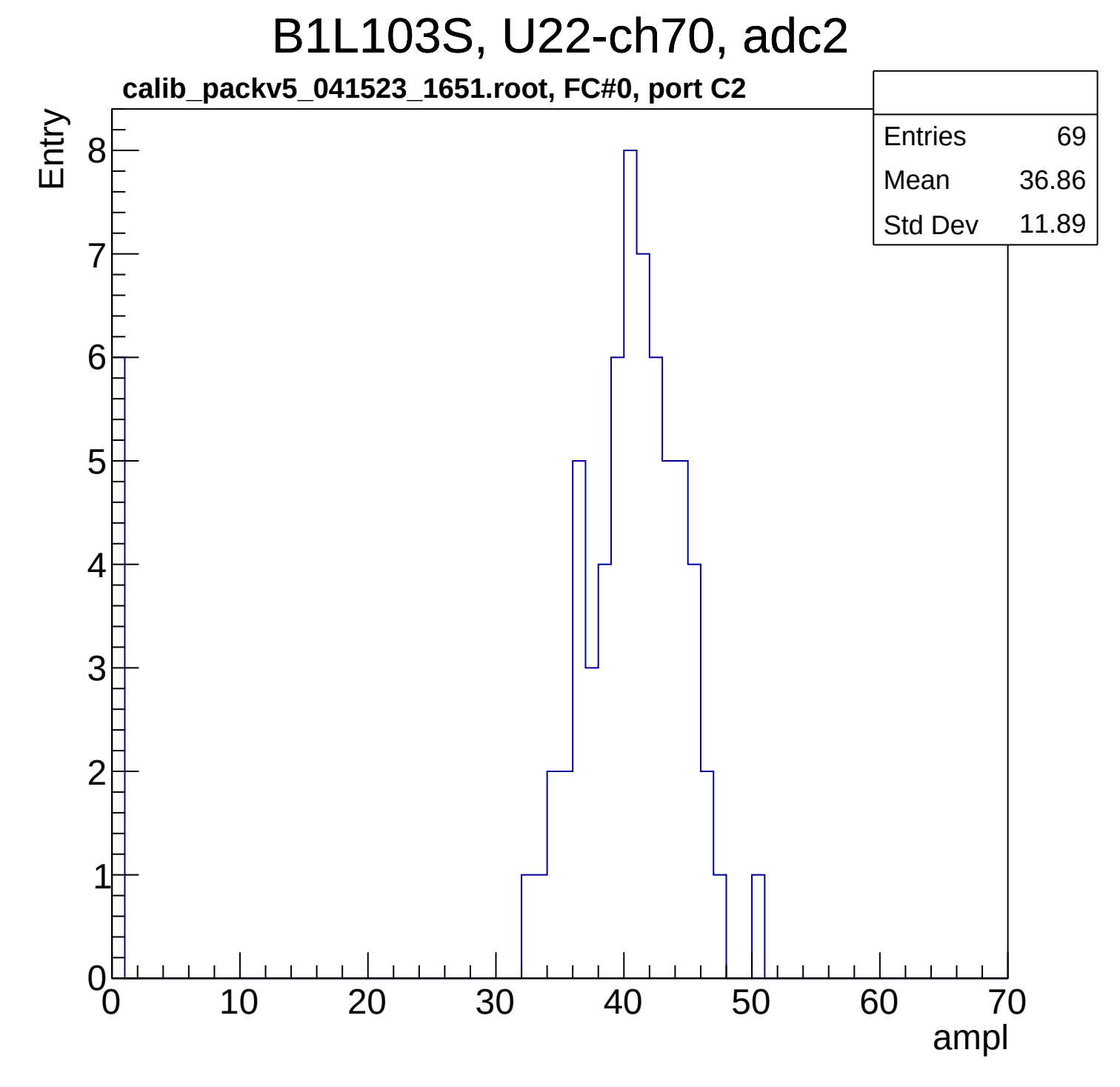
40
50
60
70


B1L103S, U22-ch70, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 36.86
Std Dev 11.89
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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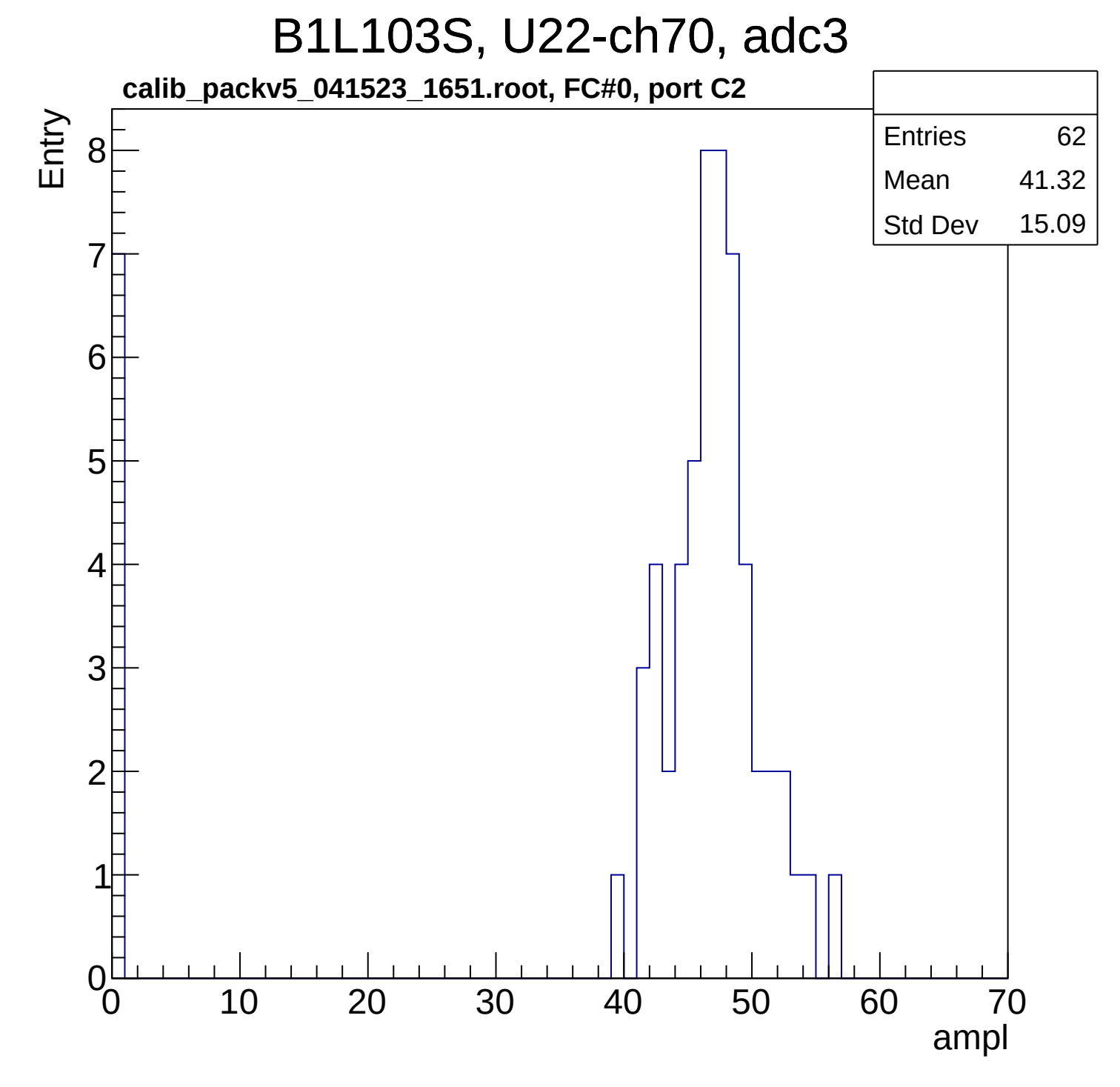
40
50
60
70


B1L103S, U22-ch70, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 41.32
Std Dev 15.09
Entry
ampl
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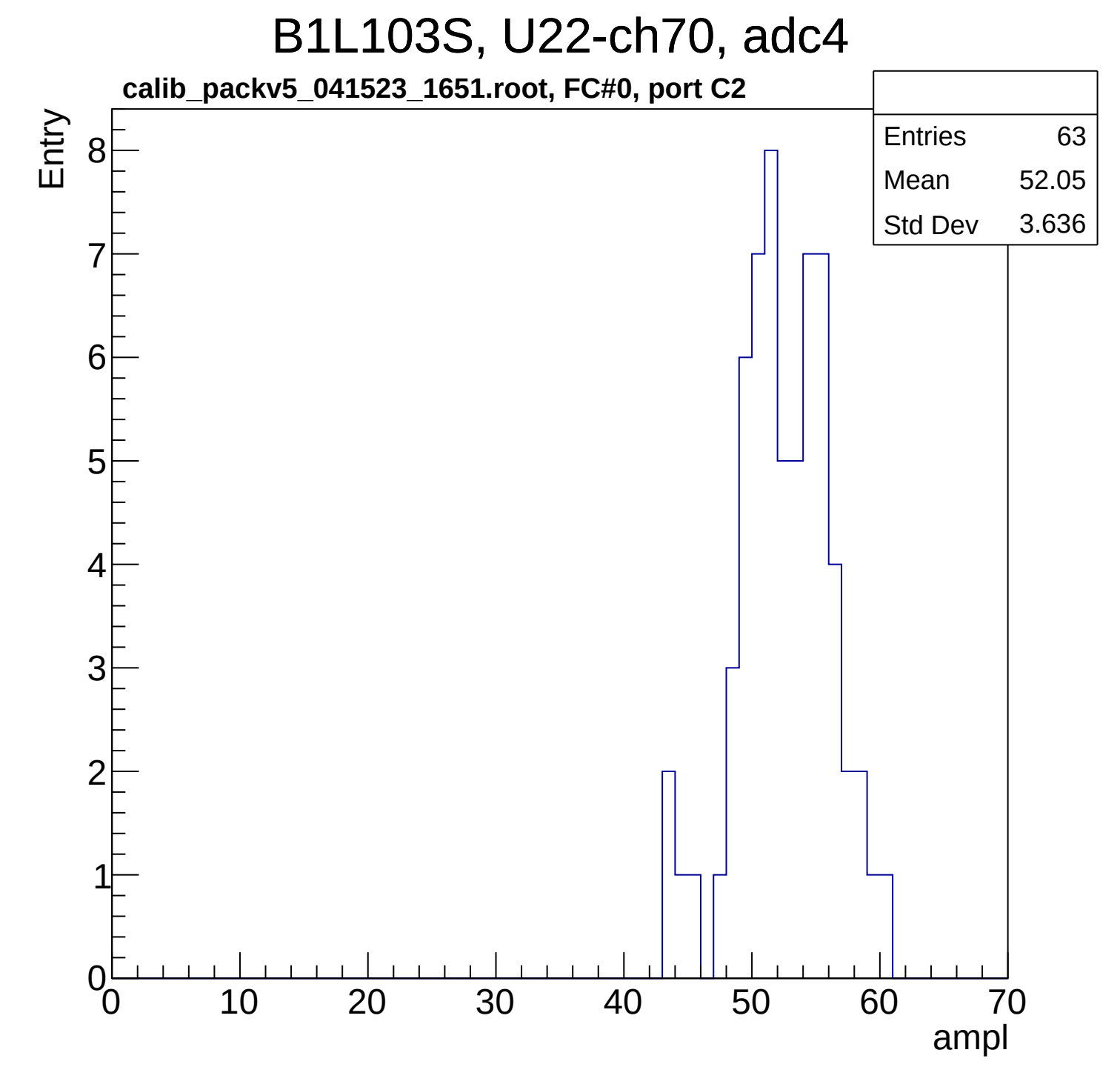
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch70, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 52.05
Std Dev 3.636
Entry
ampl
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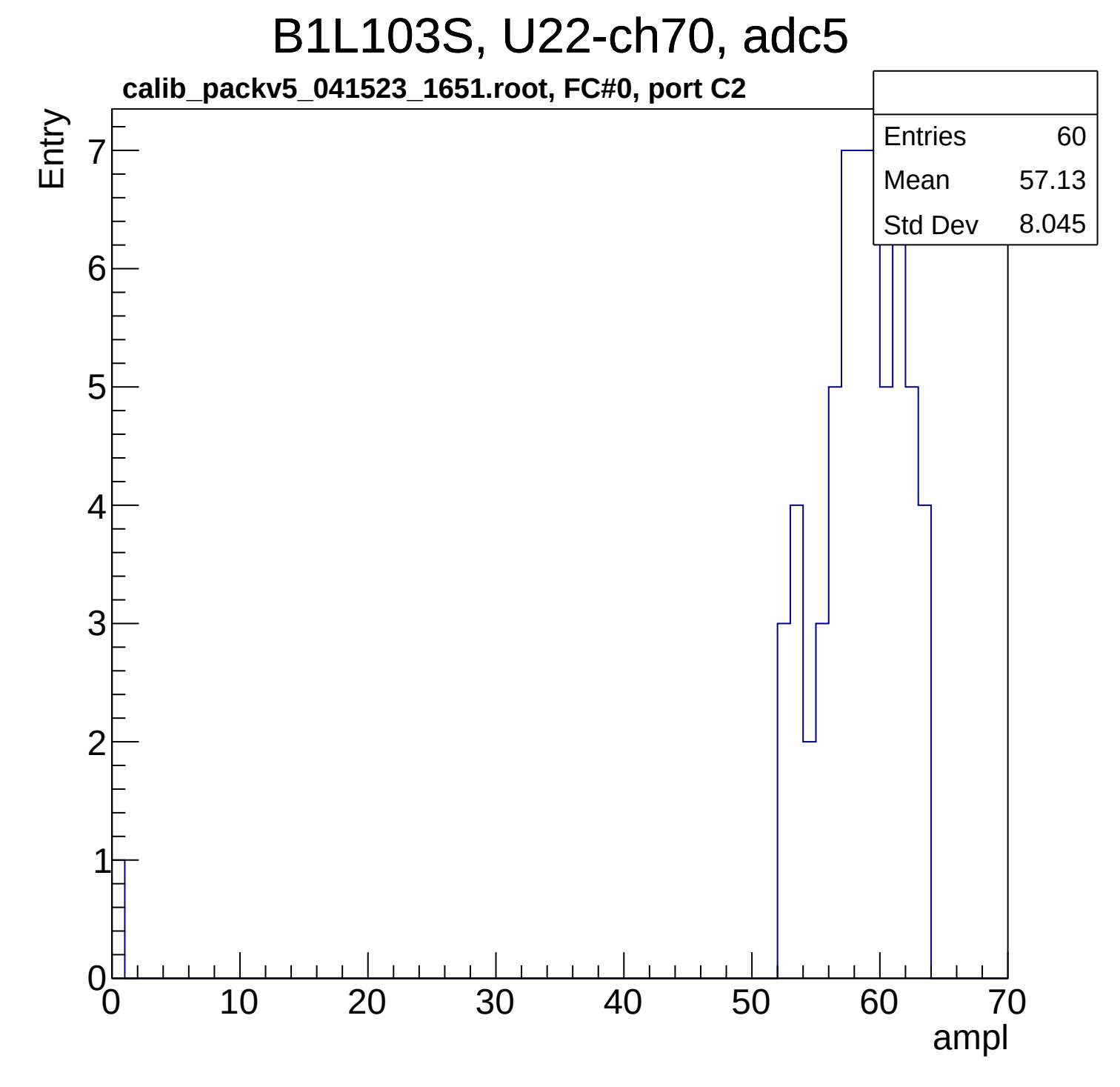
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch70, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 57.13
Std Dev 8.045
Entry
ampl
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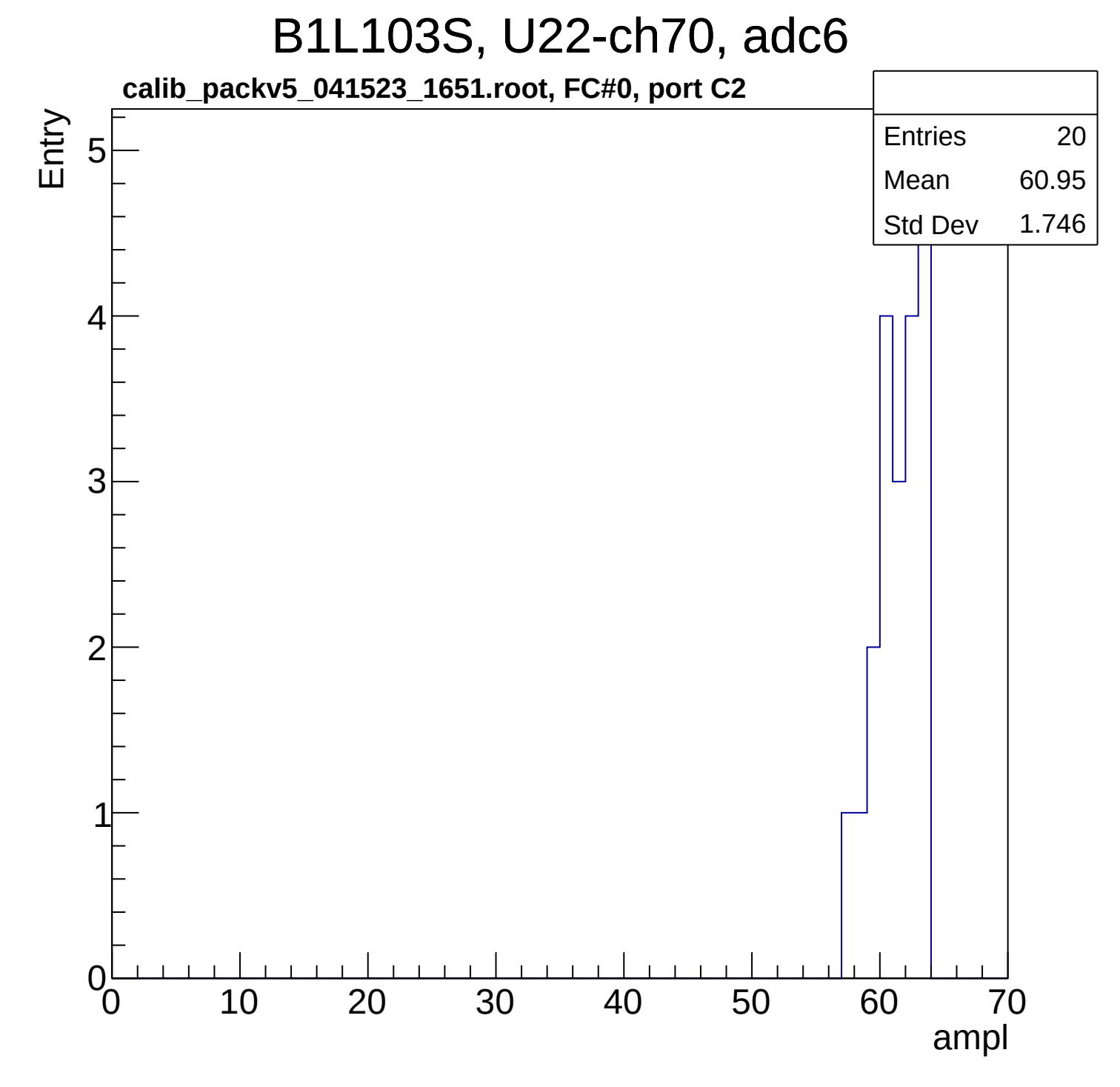
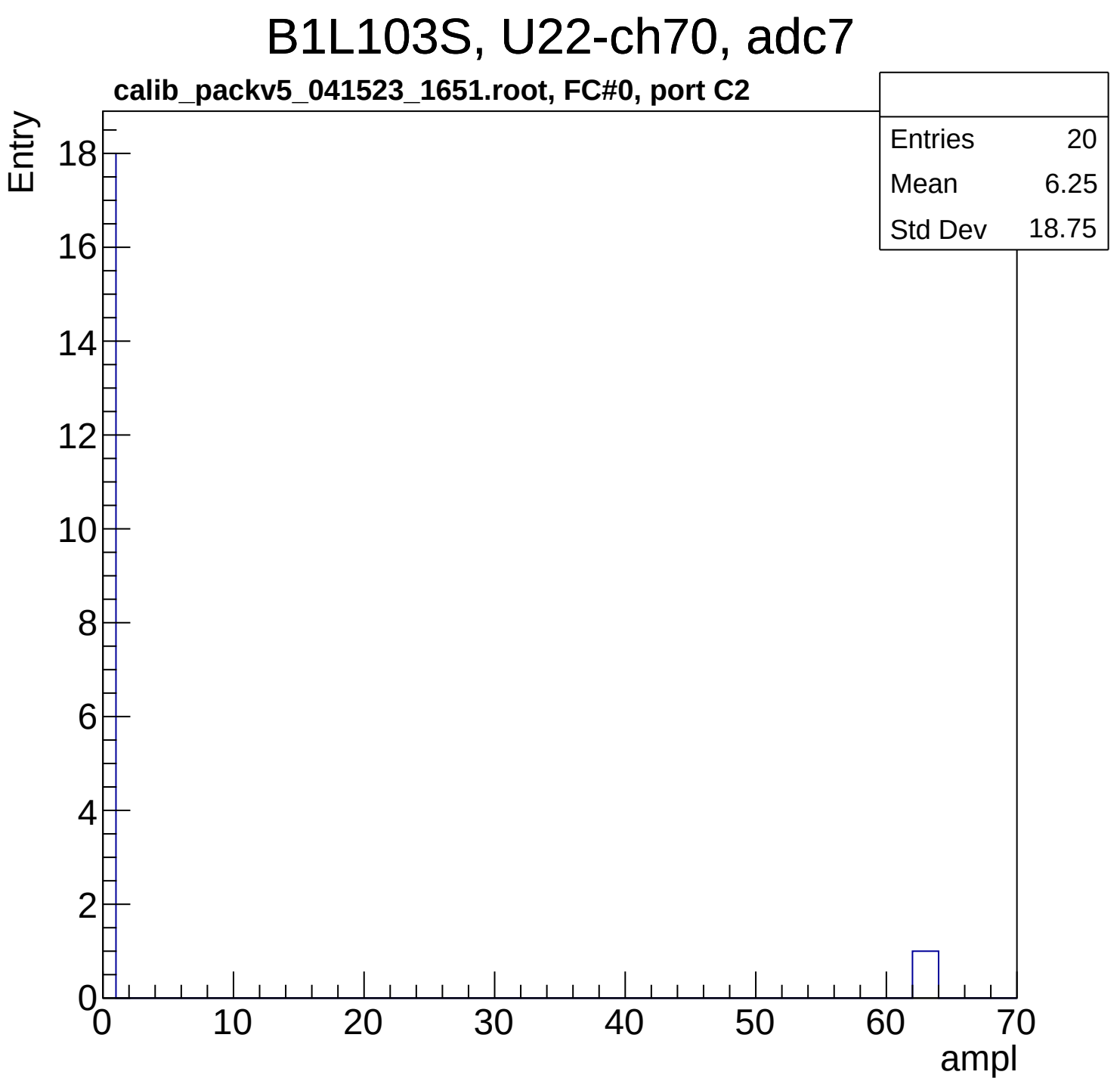
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U22-ch70, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 60.95
Std Dev 1.746
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U22-ch70, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 6.25
Std Dev 18.75
Entry
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6
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10
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14
16
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10
20
30
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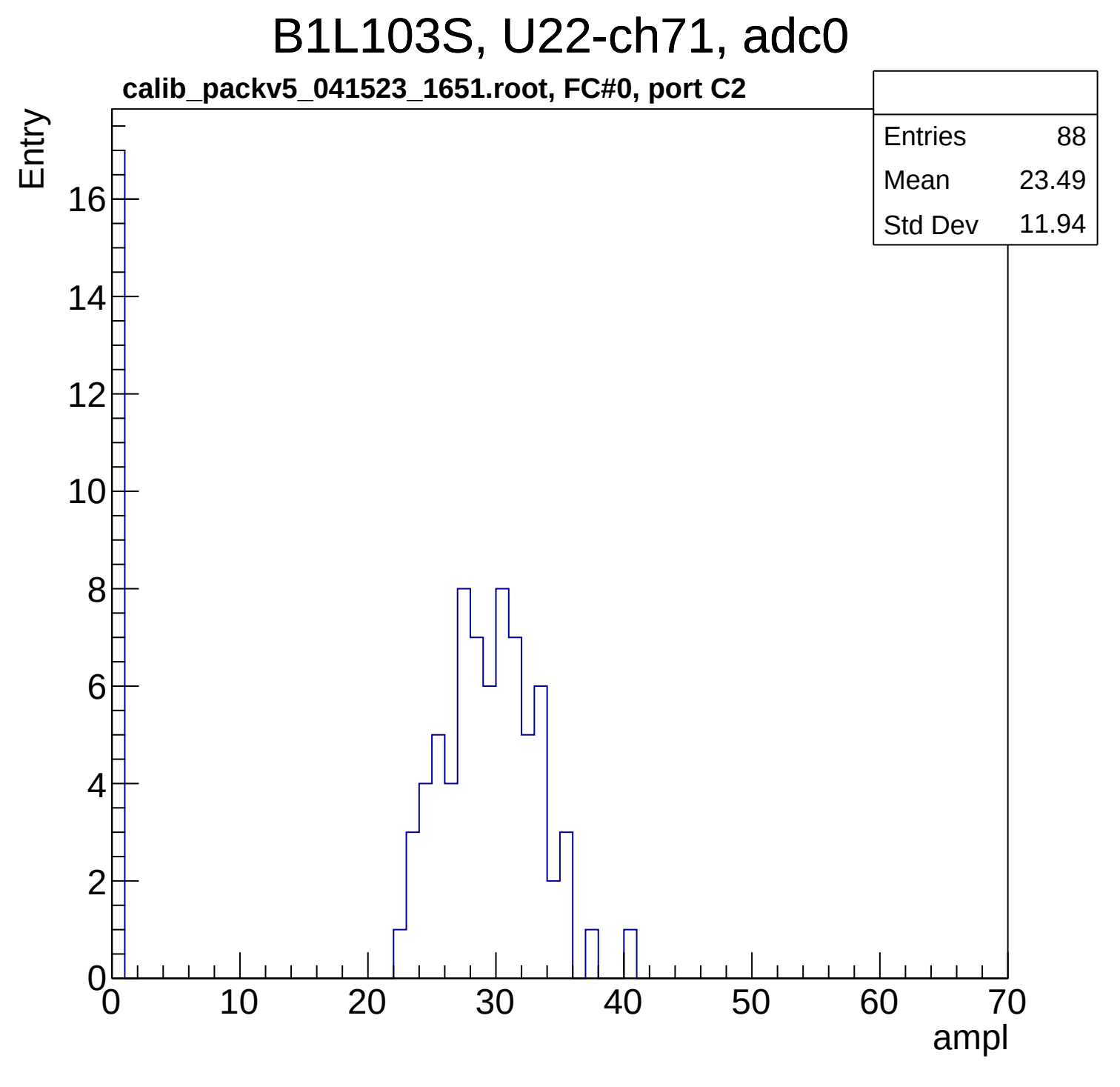
50
60
70
ampl


B1L103S, U22-ch71, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 23.49
Std Dev 11.94
Entry
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12
14
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20
30
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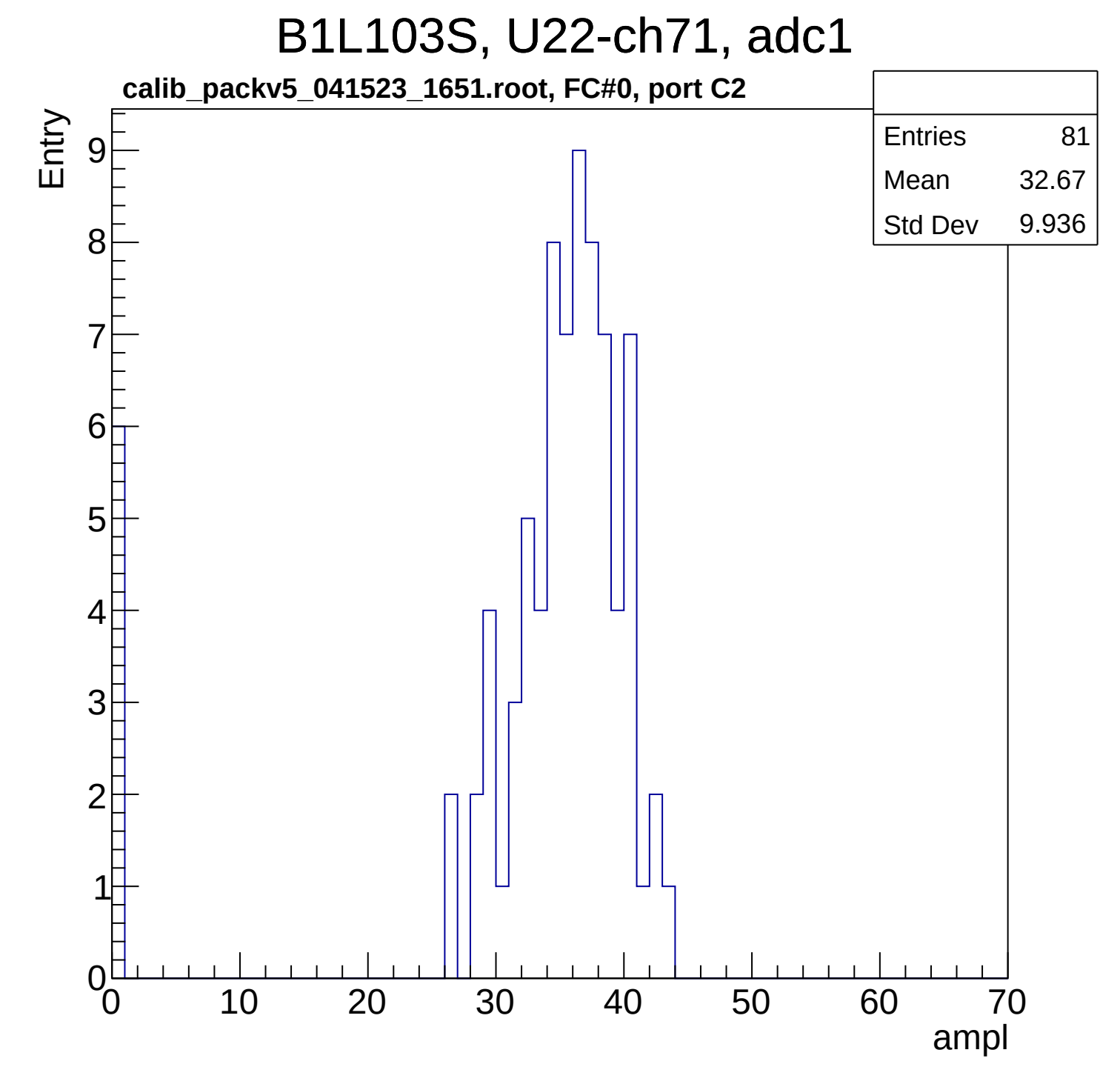
50
60
70
ampl


B1L103S, U22-ch71, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 32.67
Std Dev 9.936
Entry
ampl
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3
4
5
6
7
8
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0
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20
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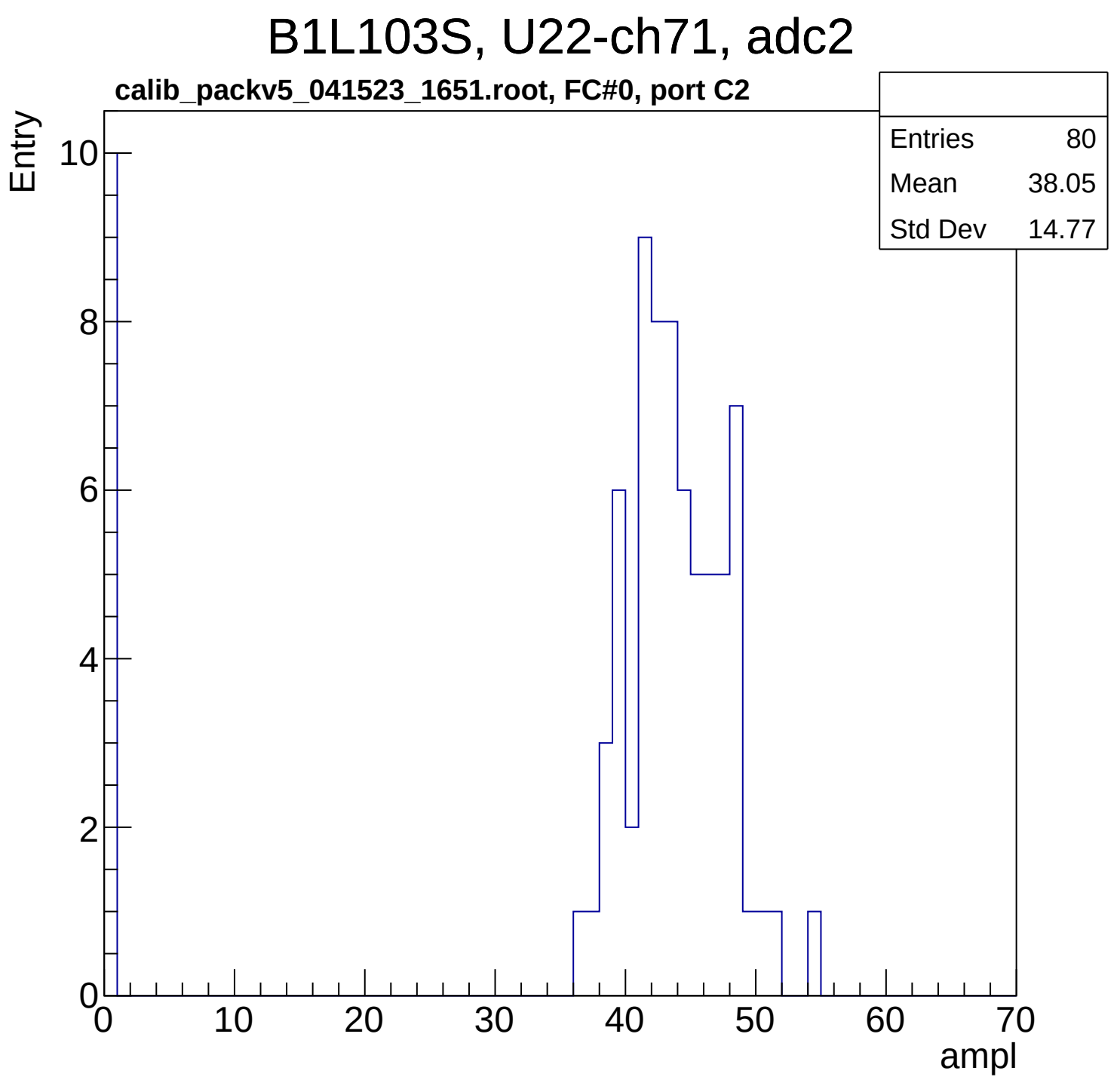
40
50
60
70


B1L103S, U22-ch71, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 38.05
Std Dev 14.77
Entry
0
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4
6
8
10
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10
20
30
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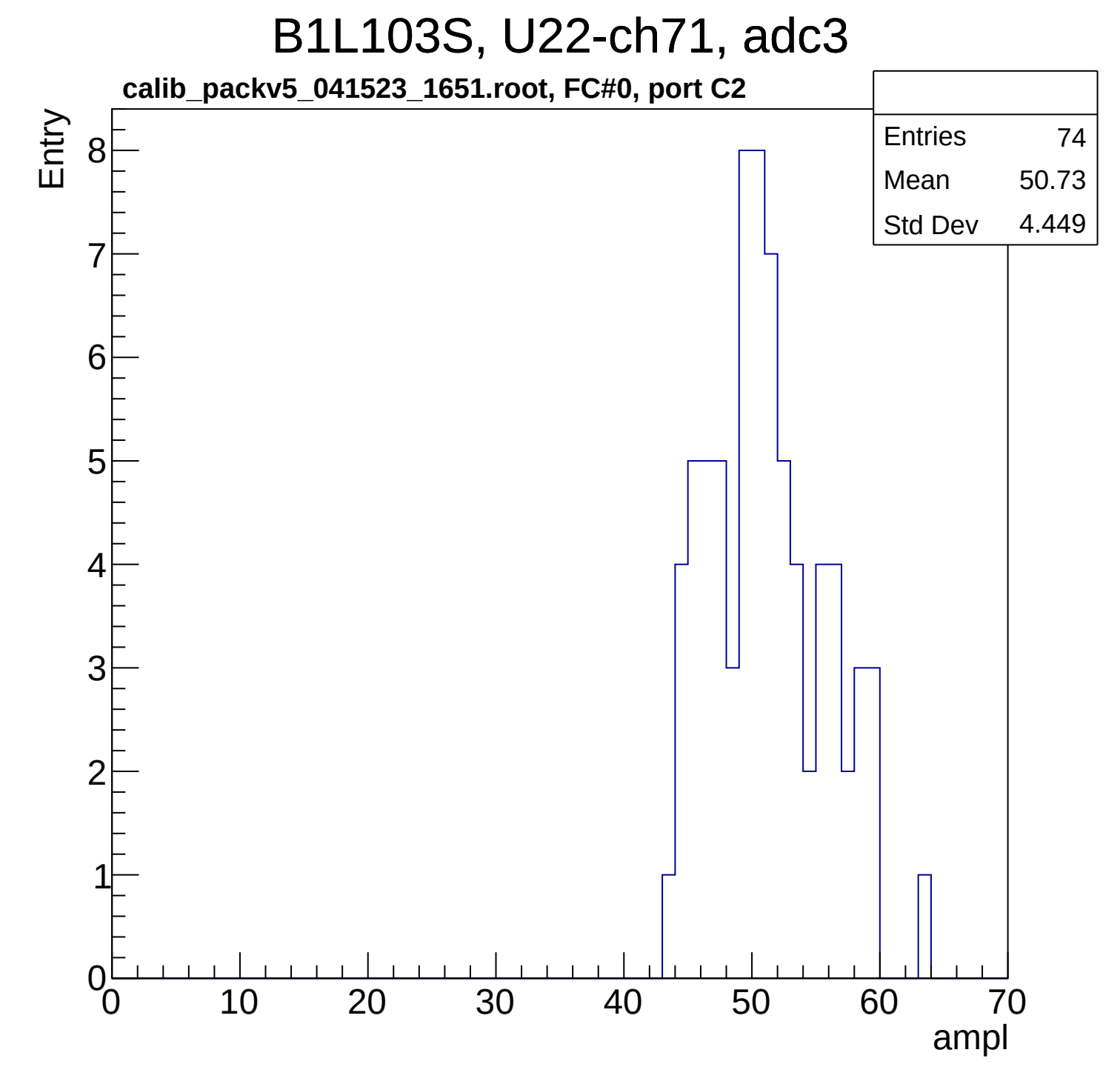
50
60
70
ampl


B1L103S, U22-ch71, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 50.73
Std Dev 4.449
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
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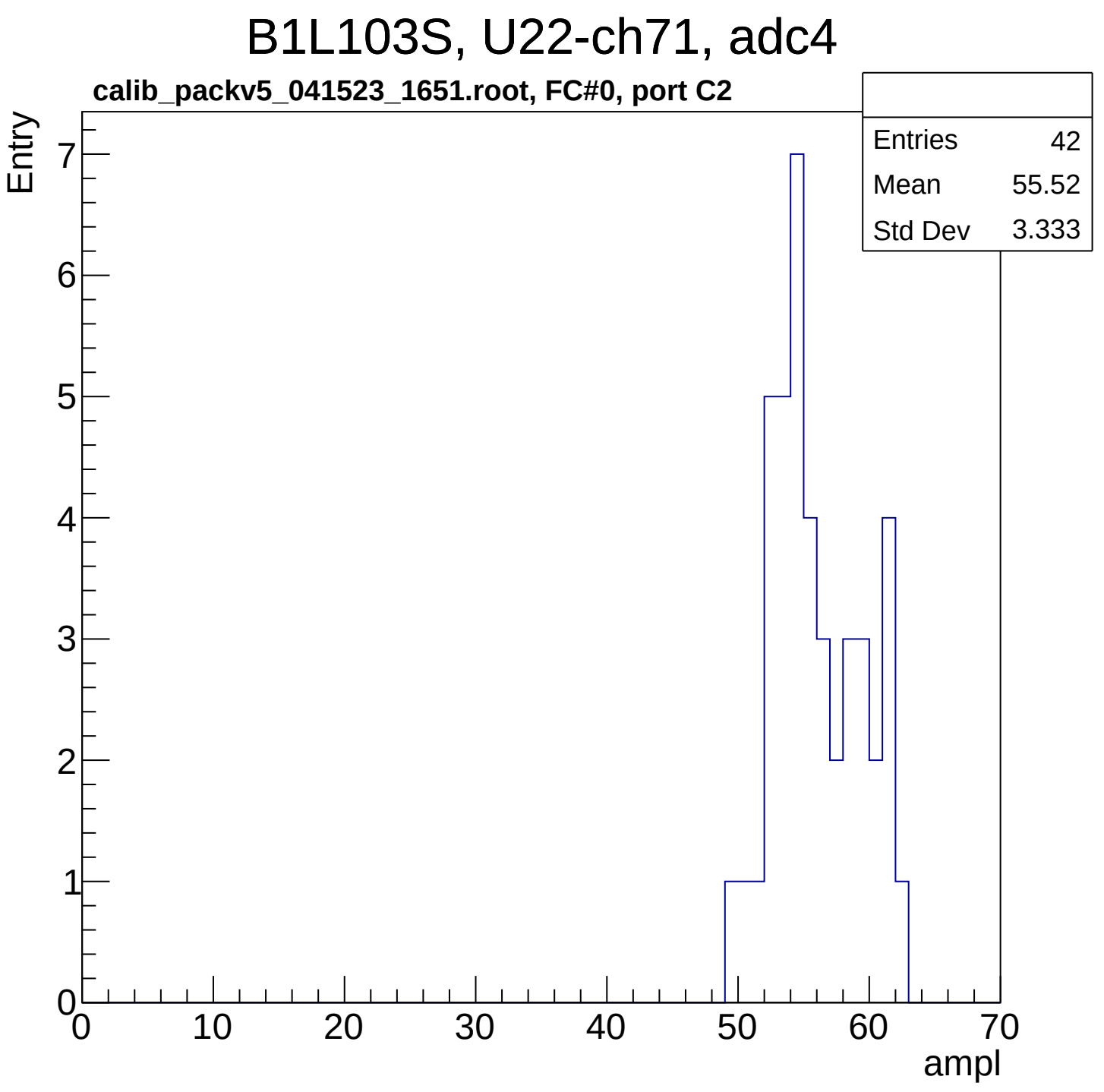
60
70


B1L103S, U22-ch71, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 55.52
Std Dev 3.333
Entry
ampl
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1
2
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4
5
6
7
0
10
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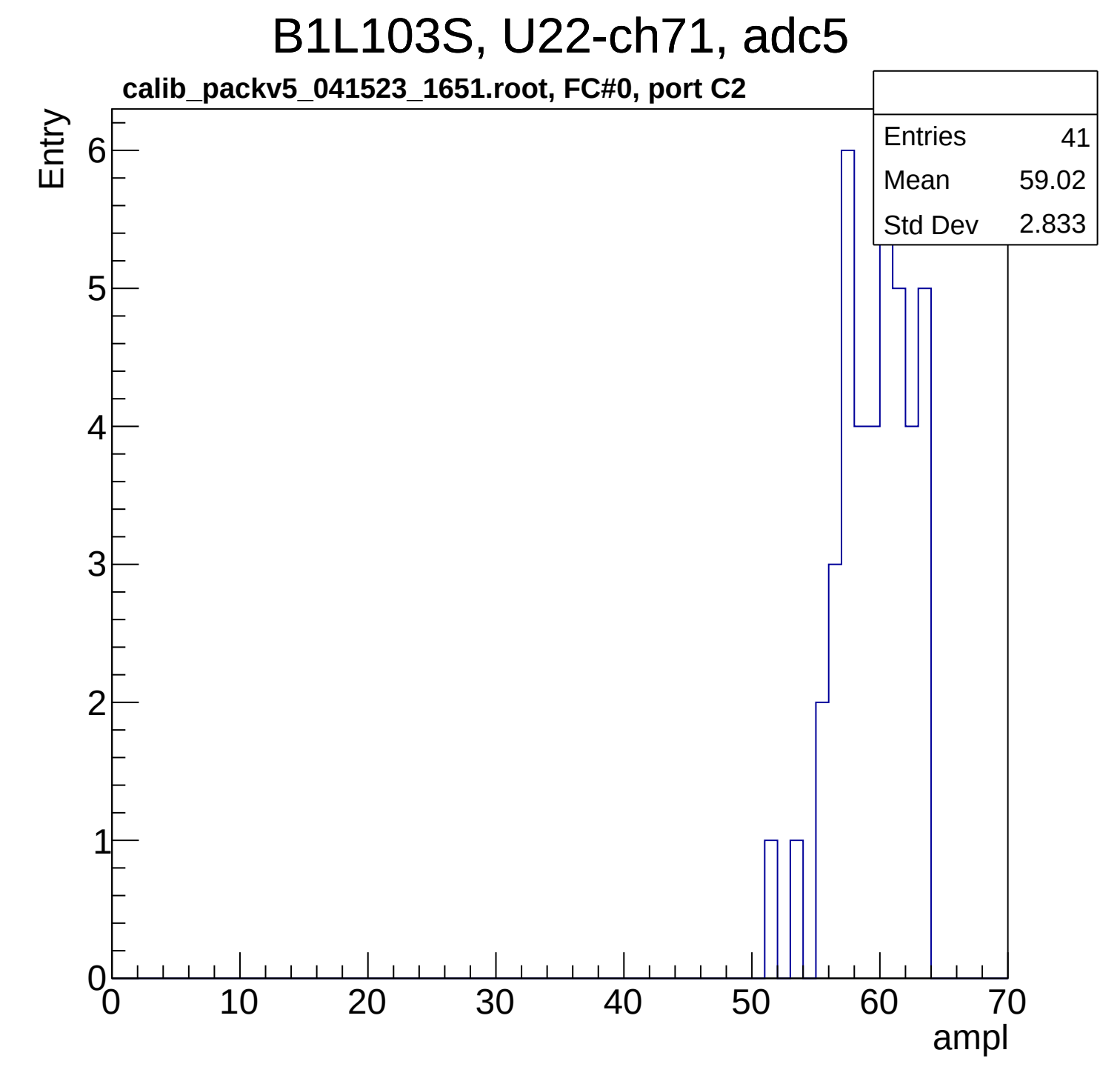
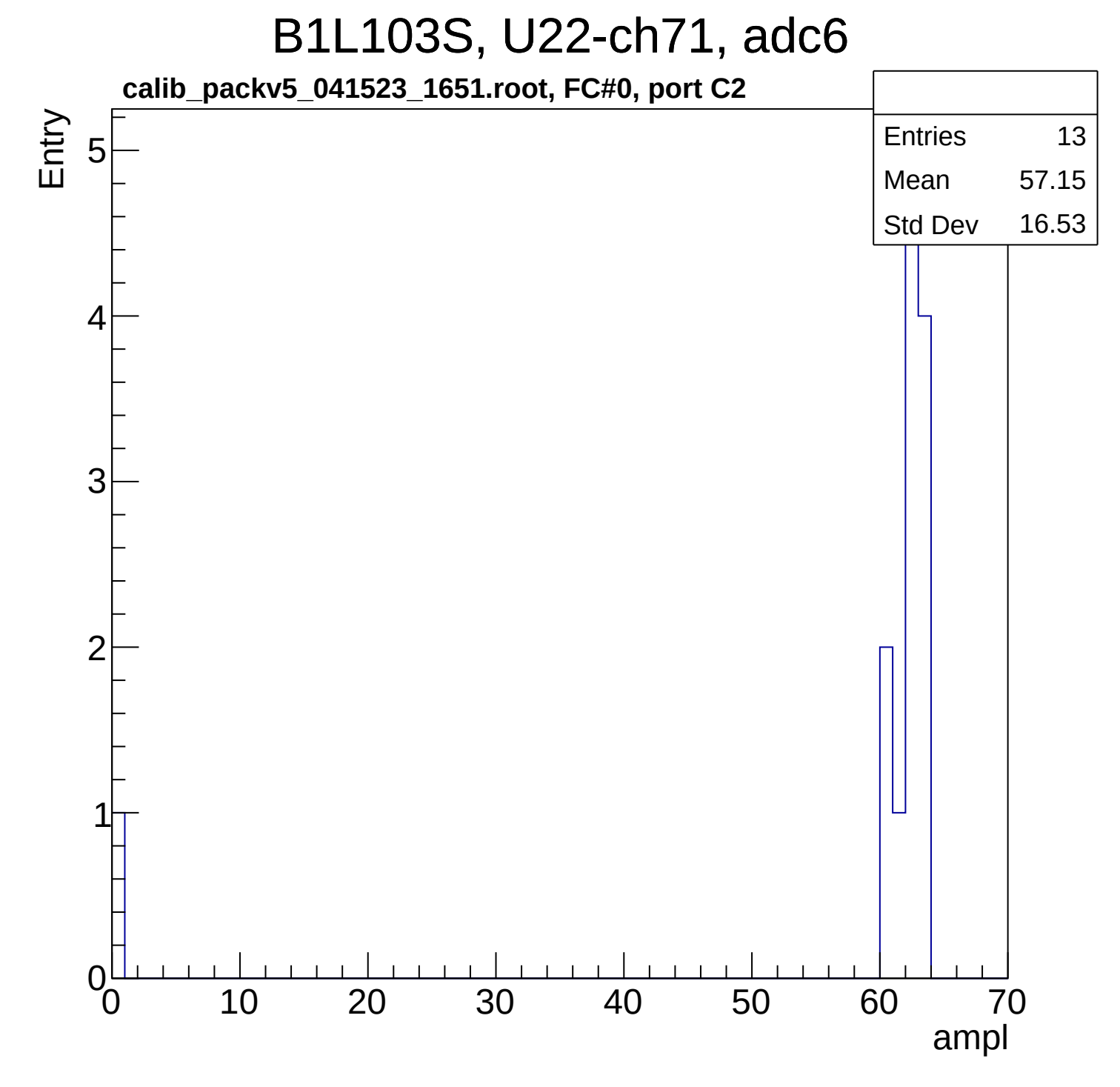
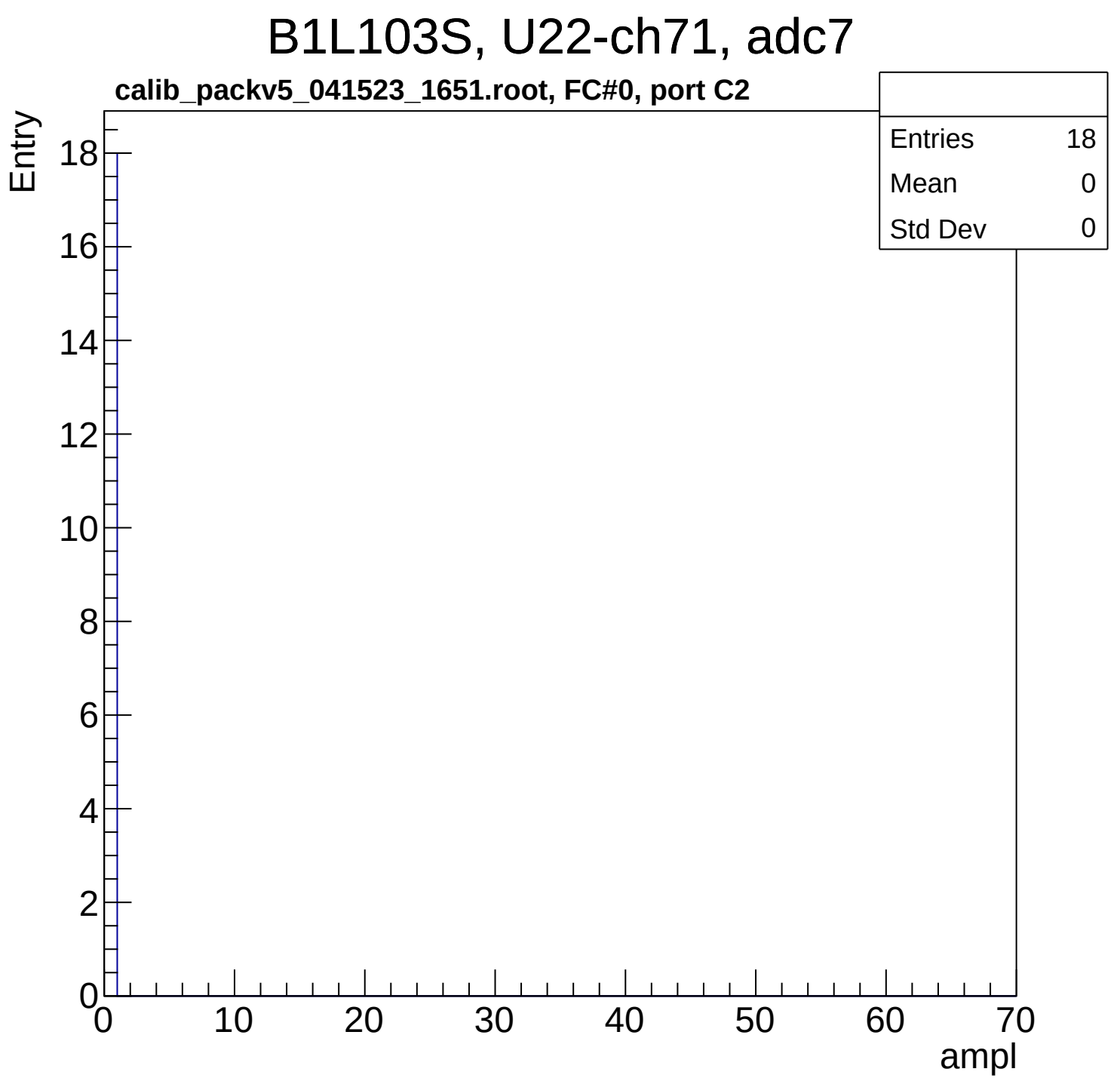
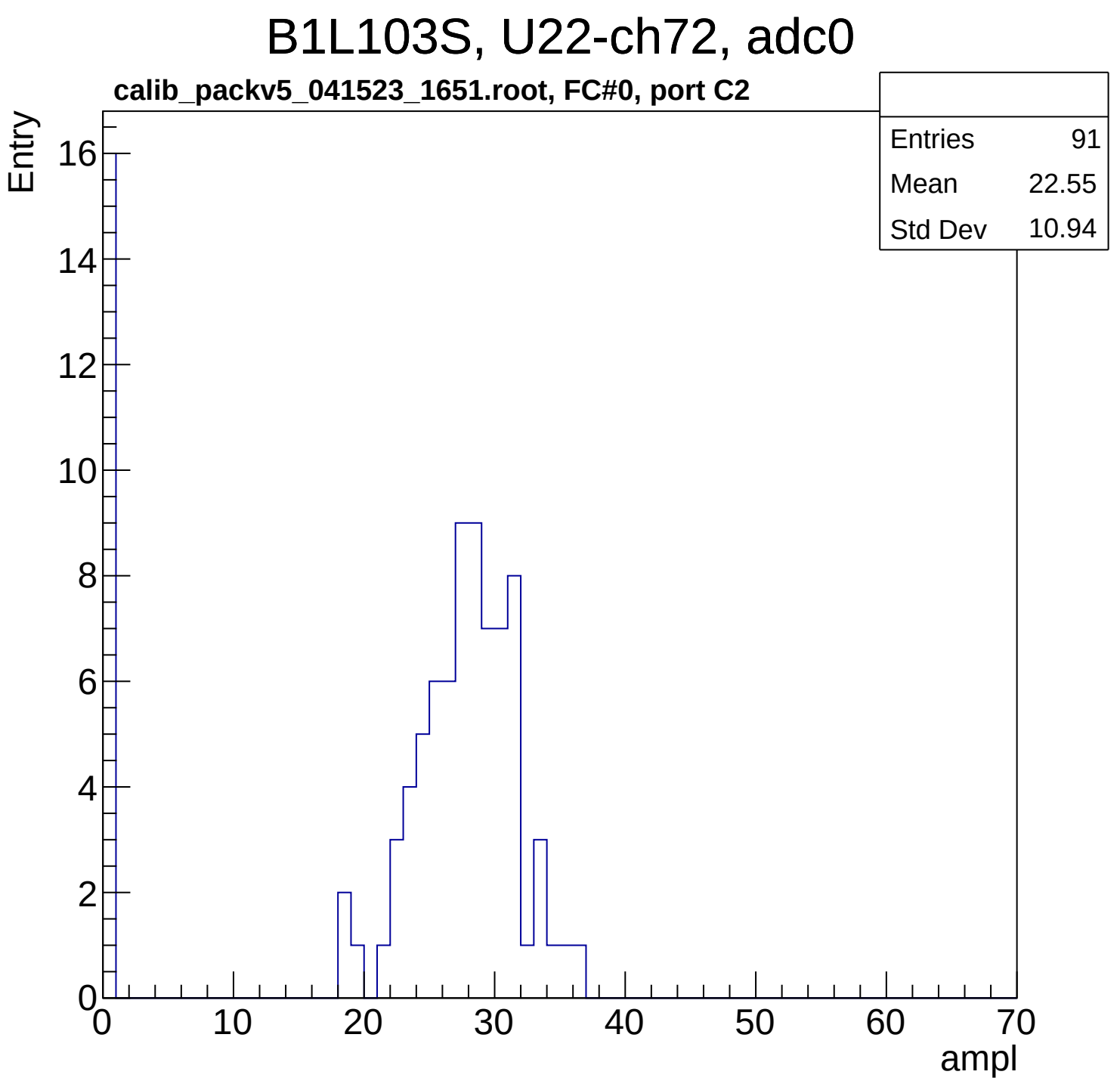
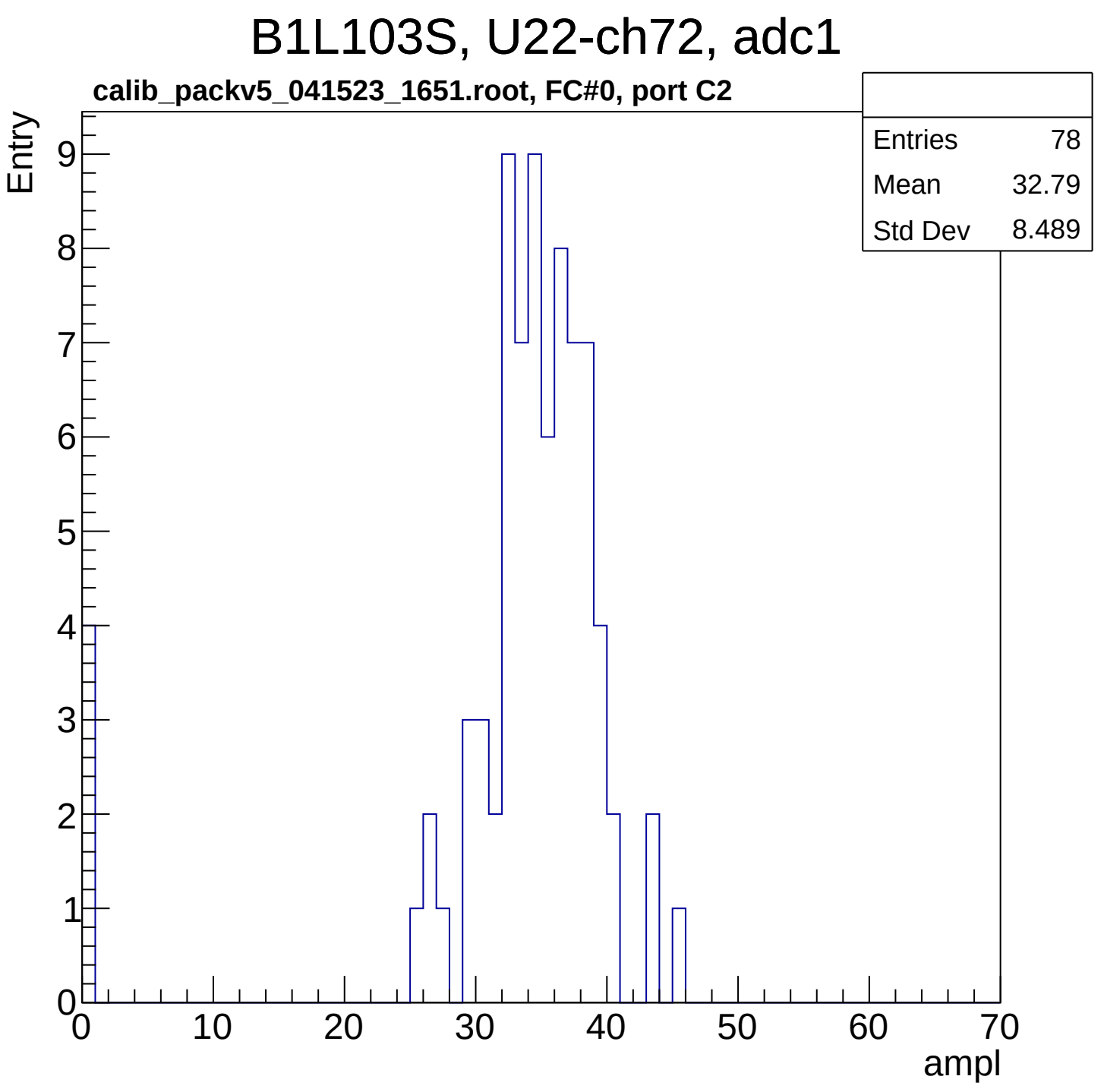
40
50
60
70

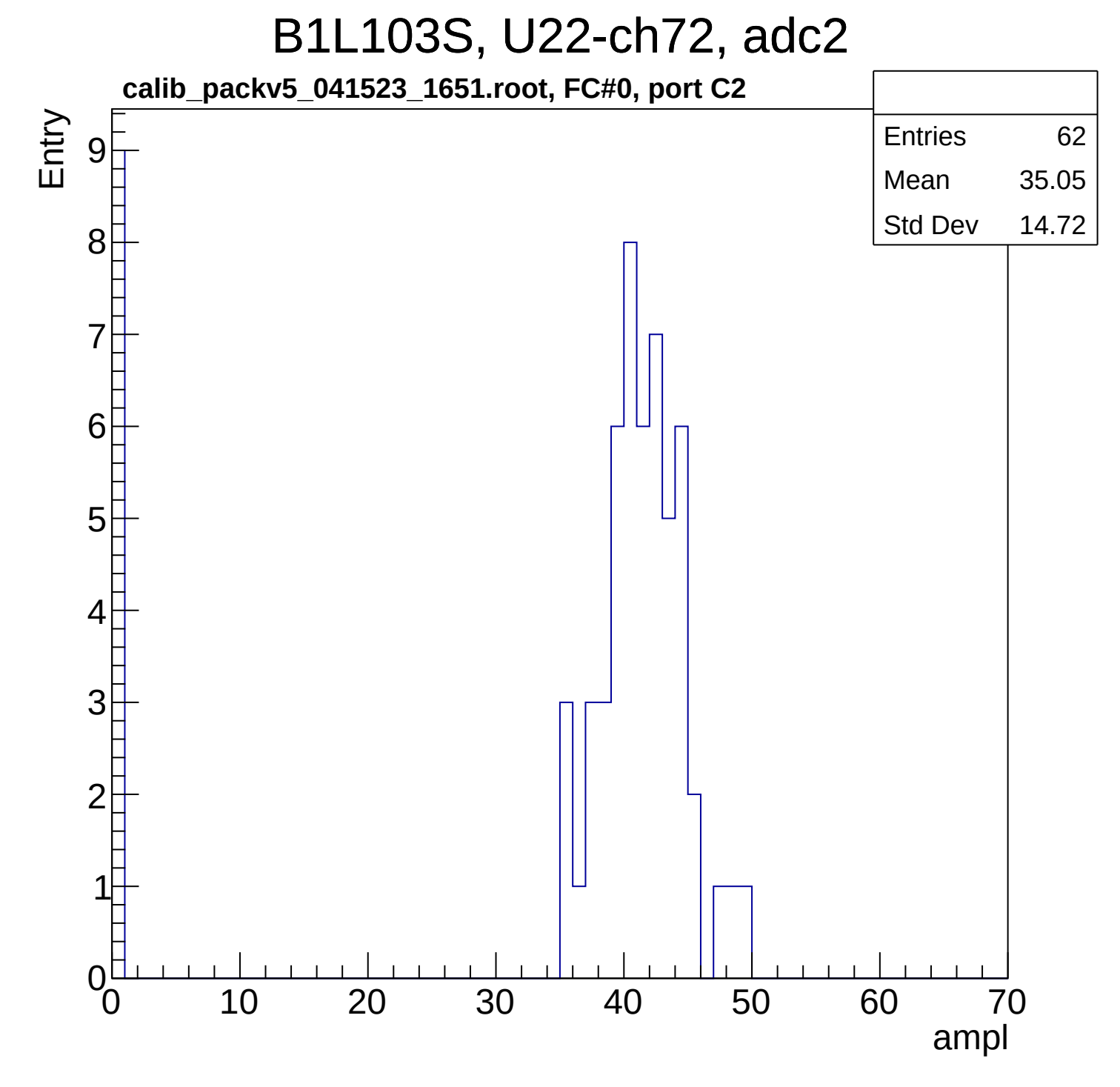

B1L103S, U22-ch71, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 59.02
Std Dev 2.833
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

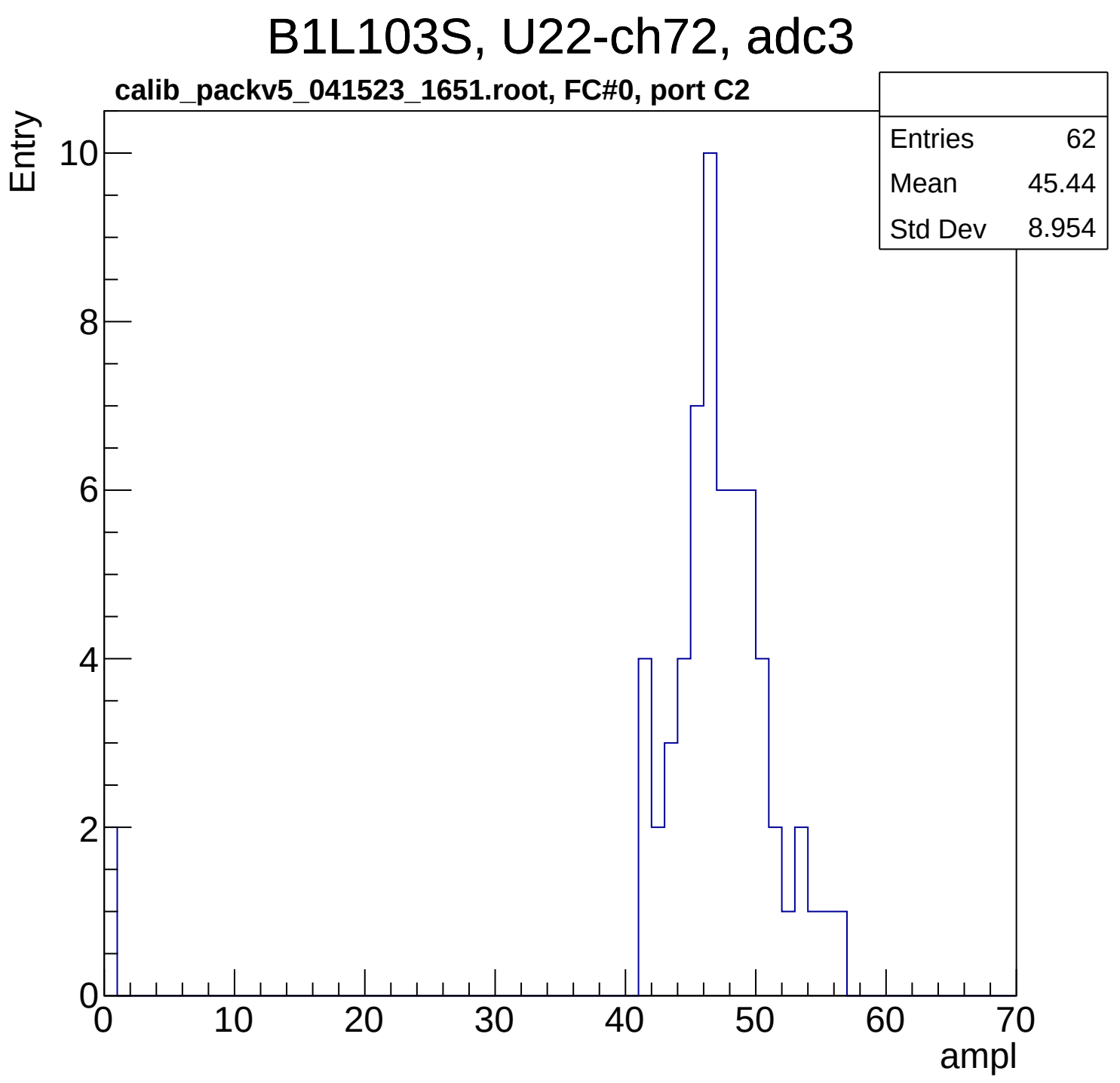

B1L103S, U22-ch71, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 57.15
Std Dev 16.53
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

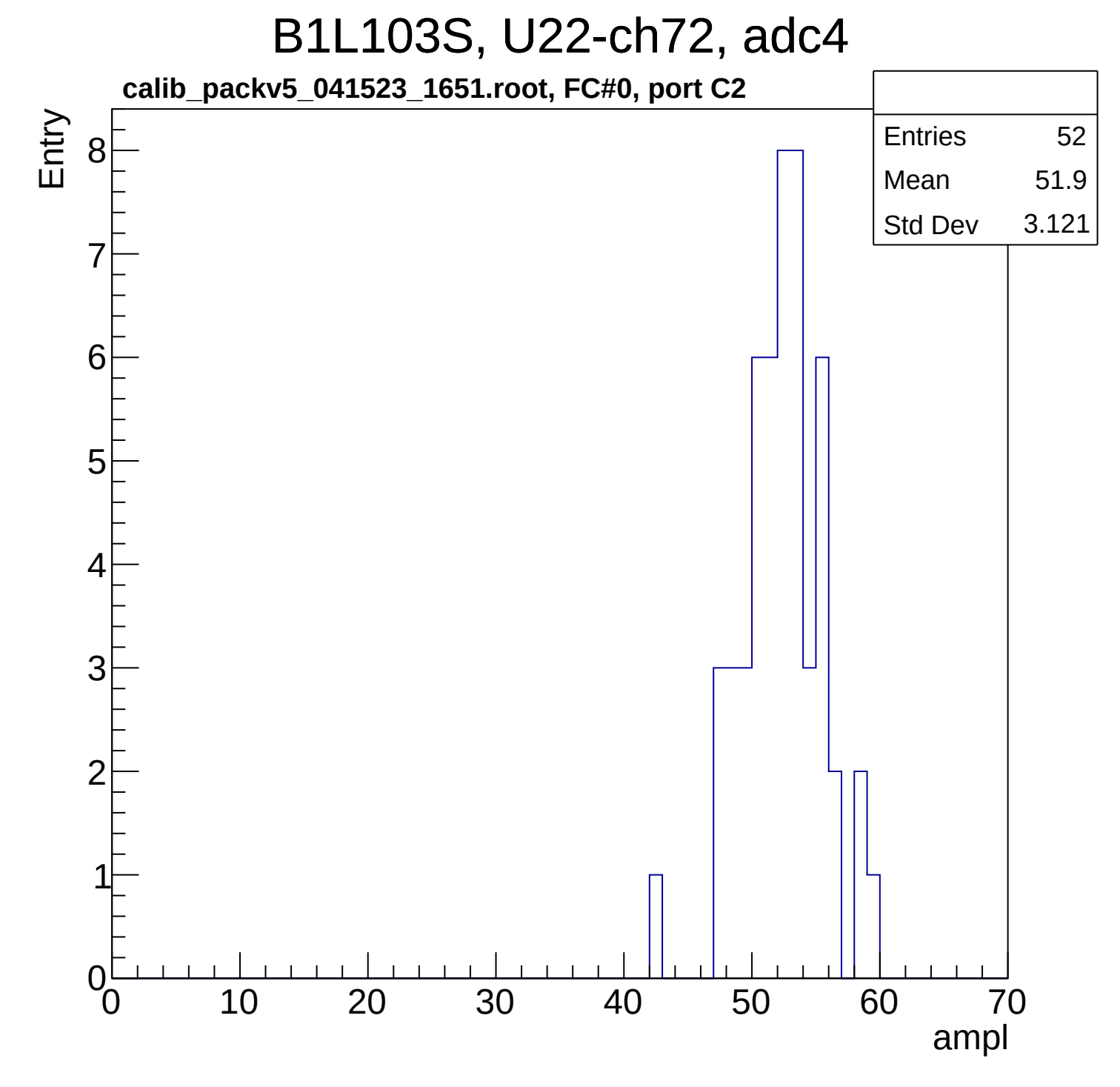

B1L103S, U22-ch71, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch72, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 22.55
Std Dev 10.94
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch72, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 32.79
Std Dev 8.489
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch72, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 35.05
Std Dev 14.72
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch72, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 45.44
Std Dev 8.954
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U22-ch72, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 51.9
Std Dev 3.121
Entry
ampl
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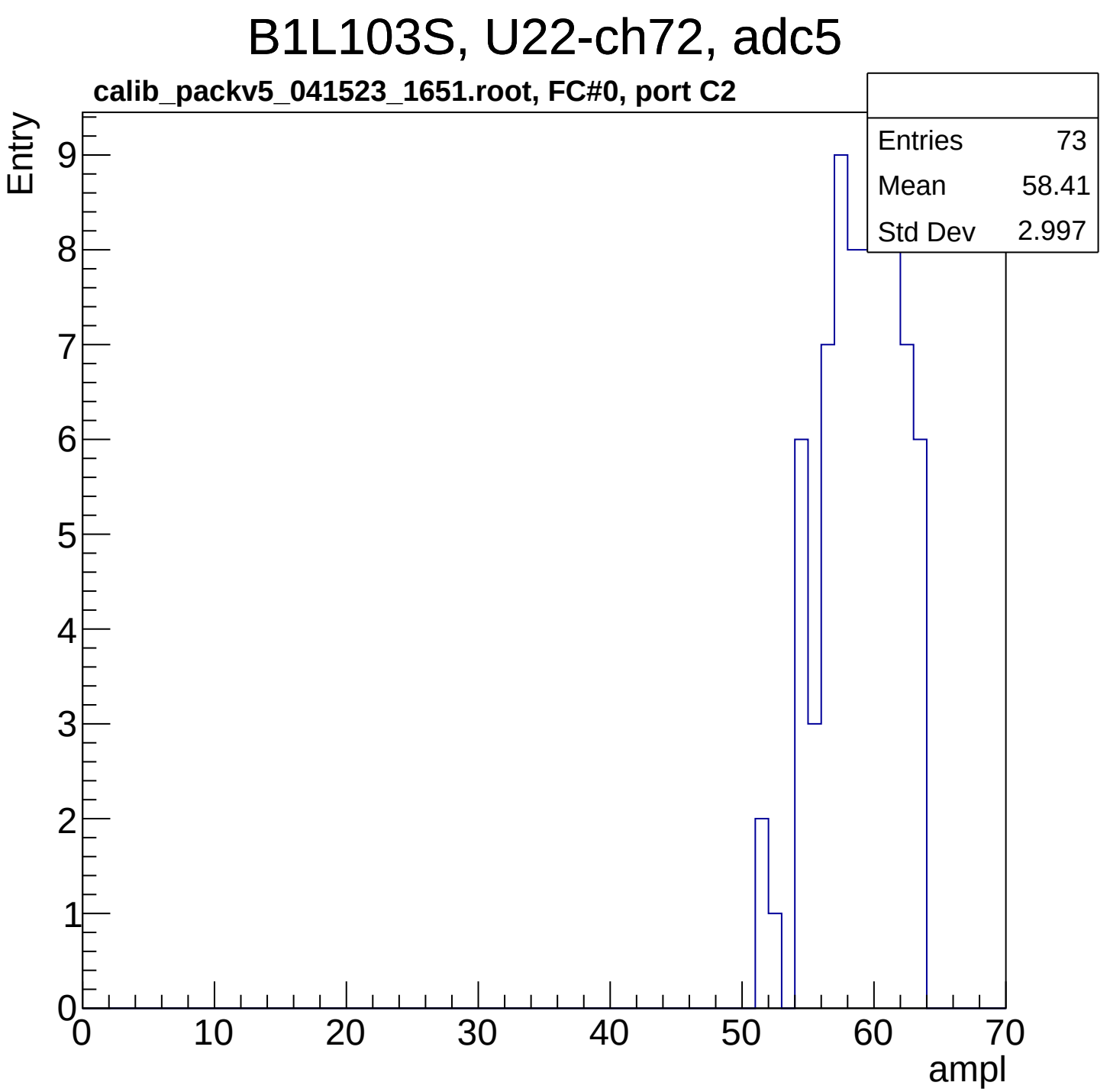
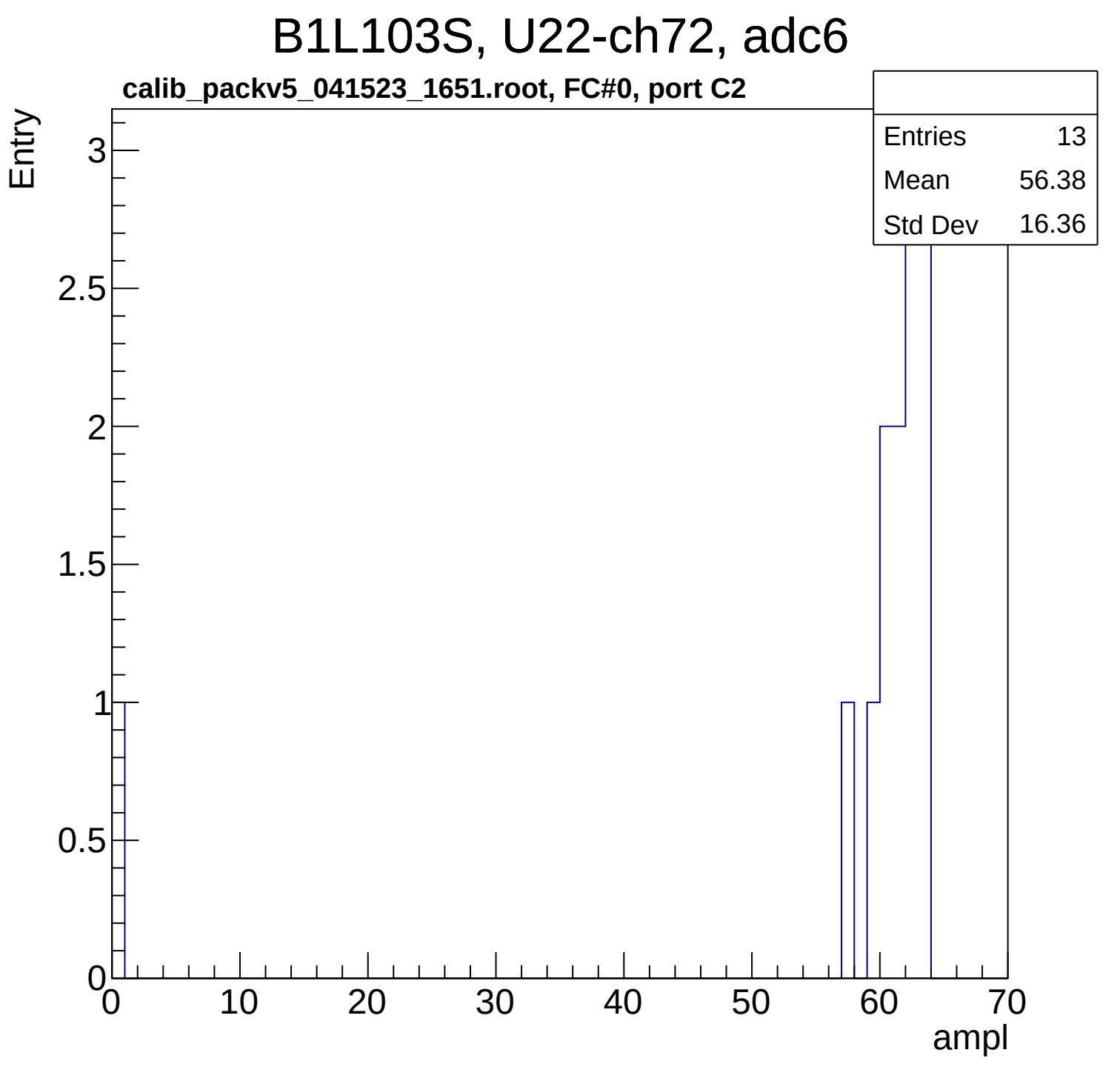
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch72, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 58.41
Std Dev 2.997
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch72, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 56.38
Std Dev 16.36
Entry
ampl
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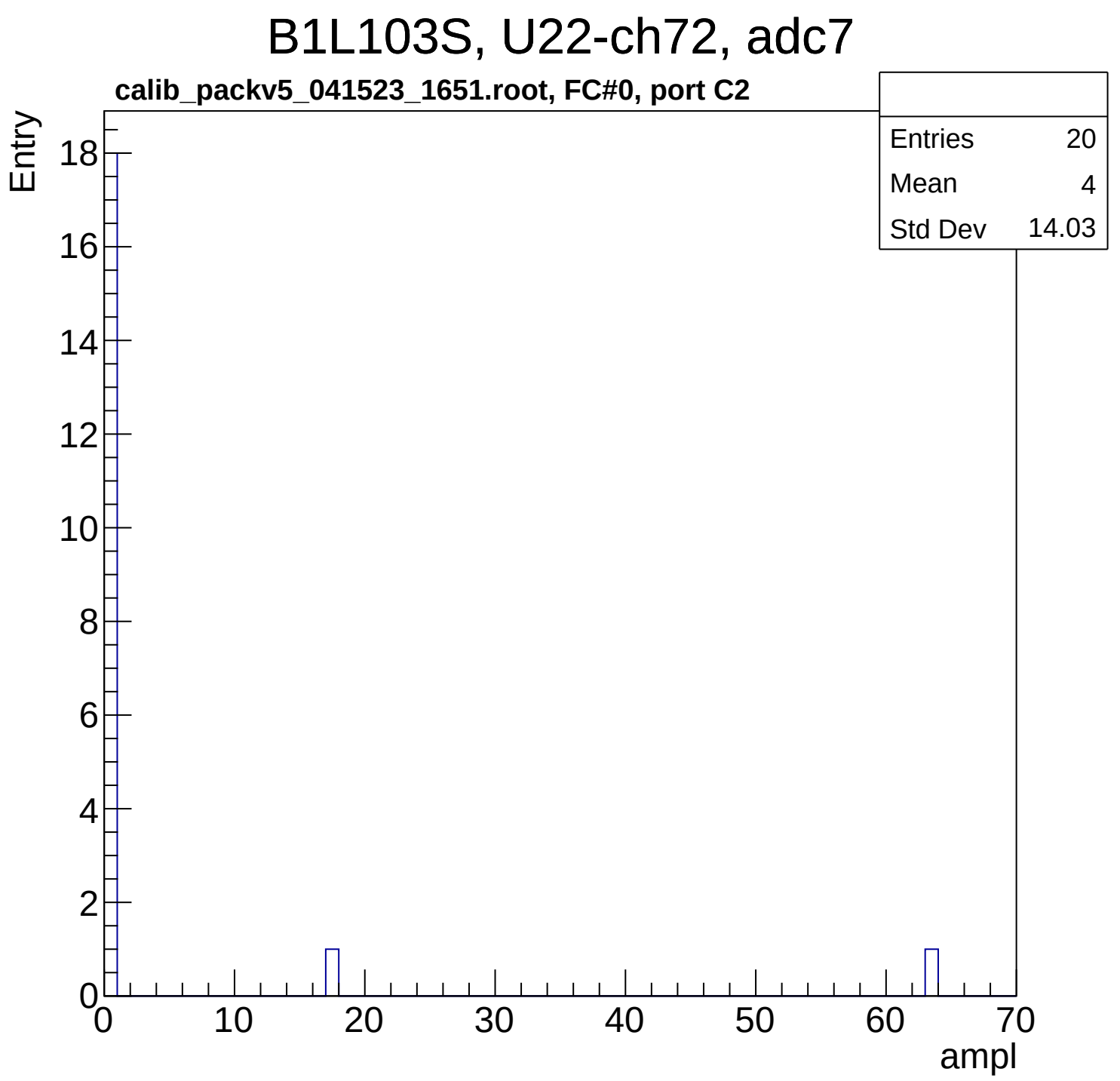
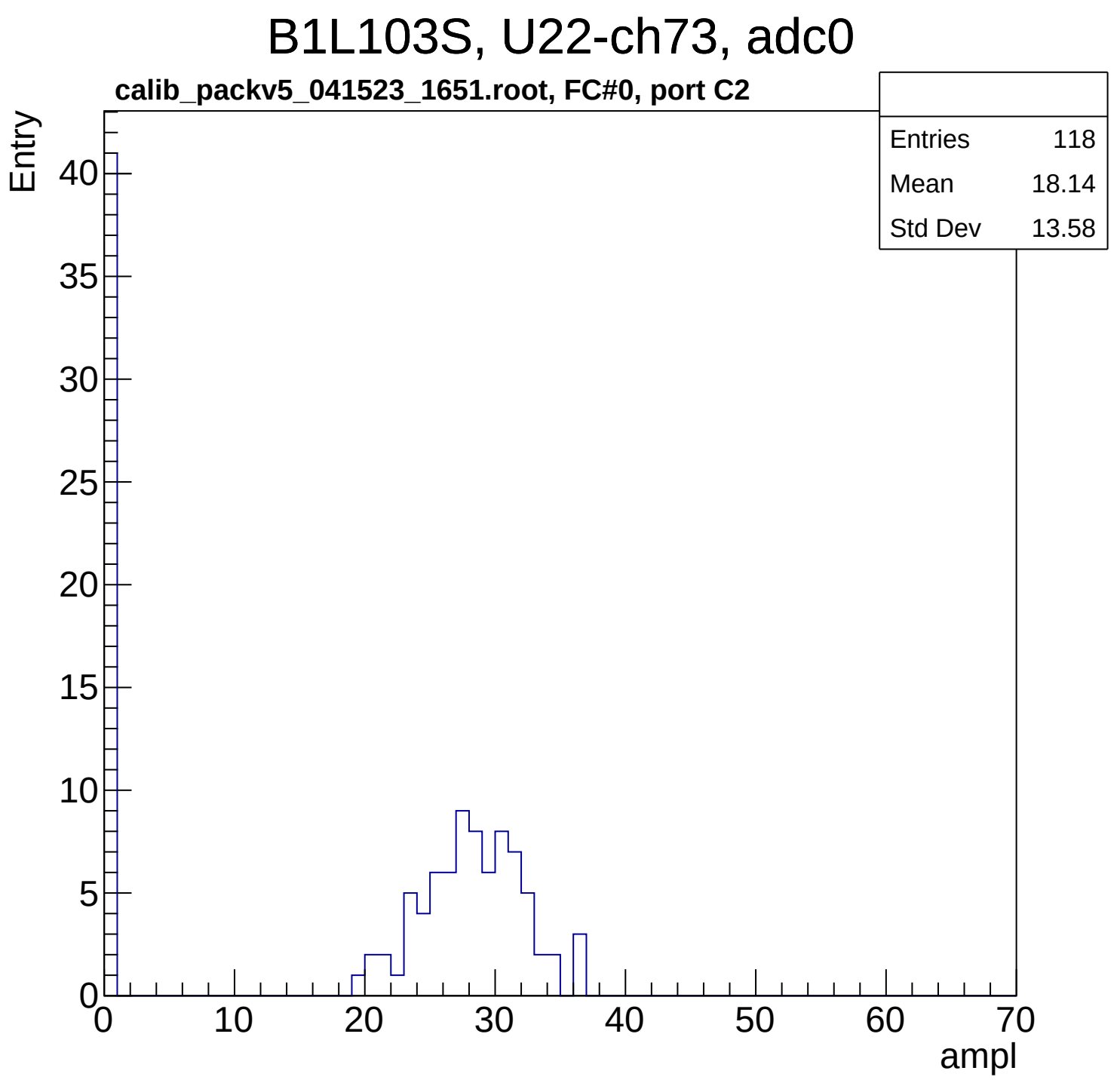
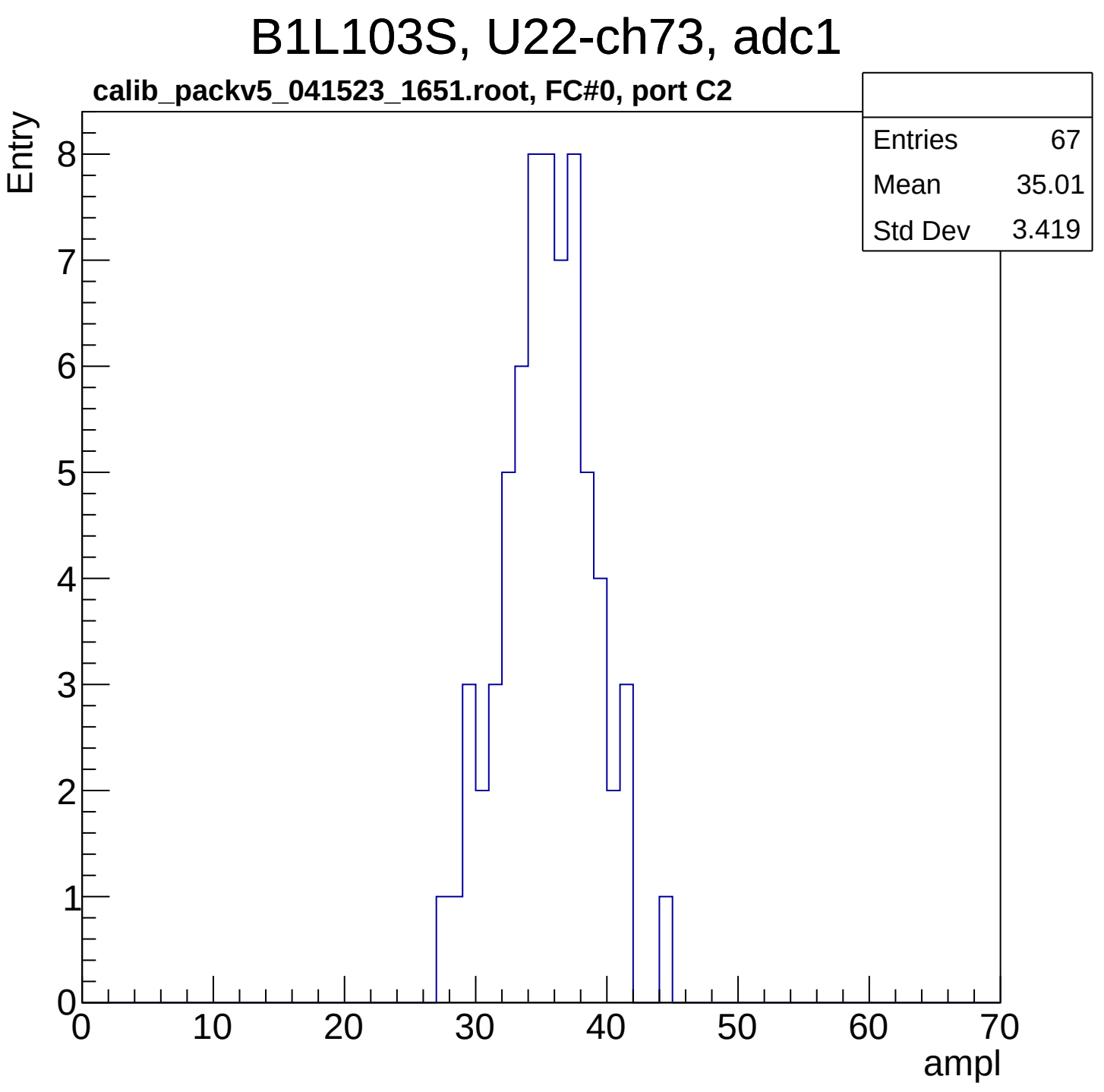
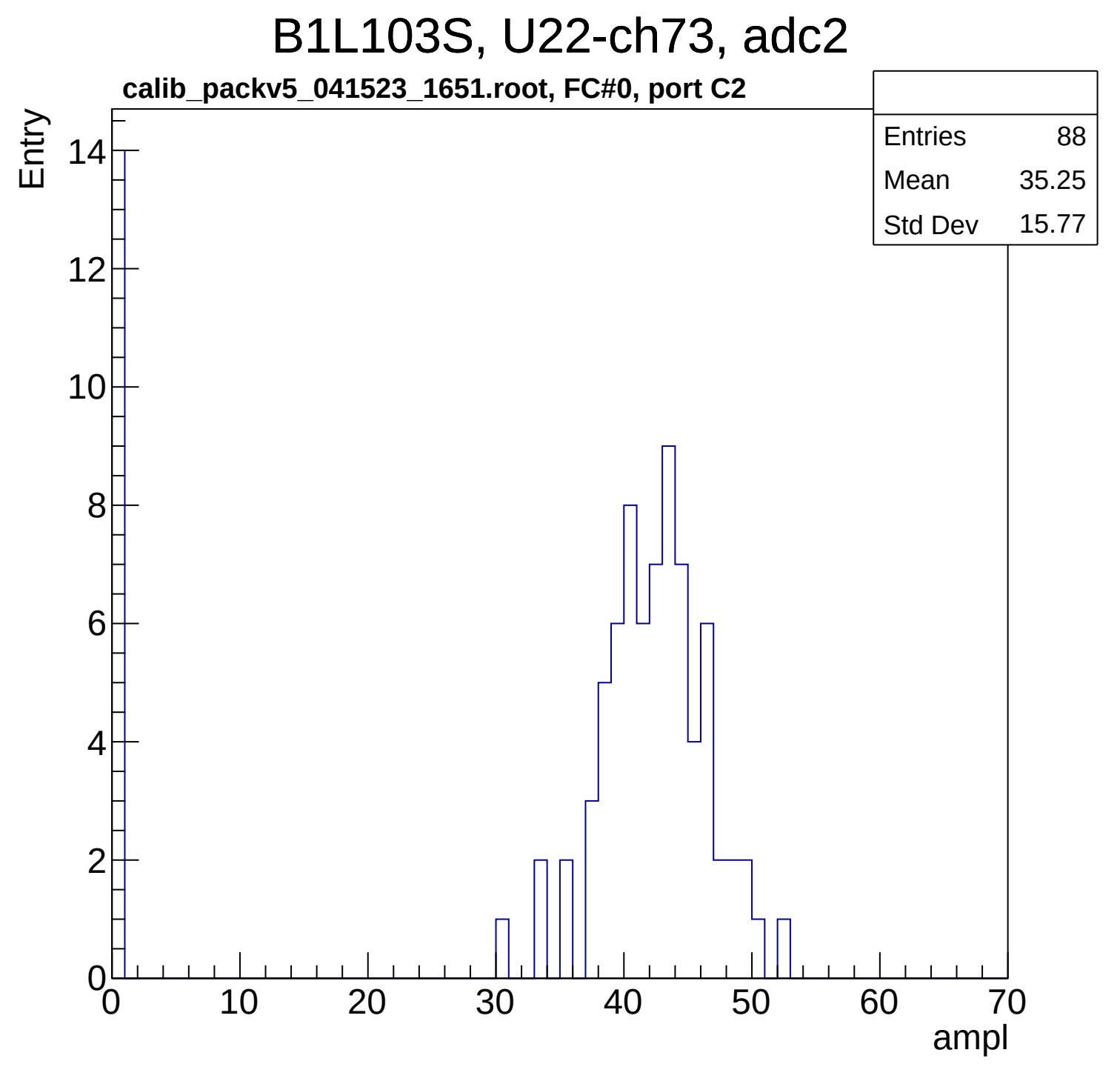
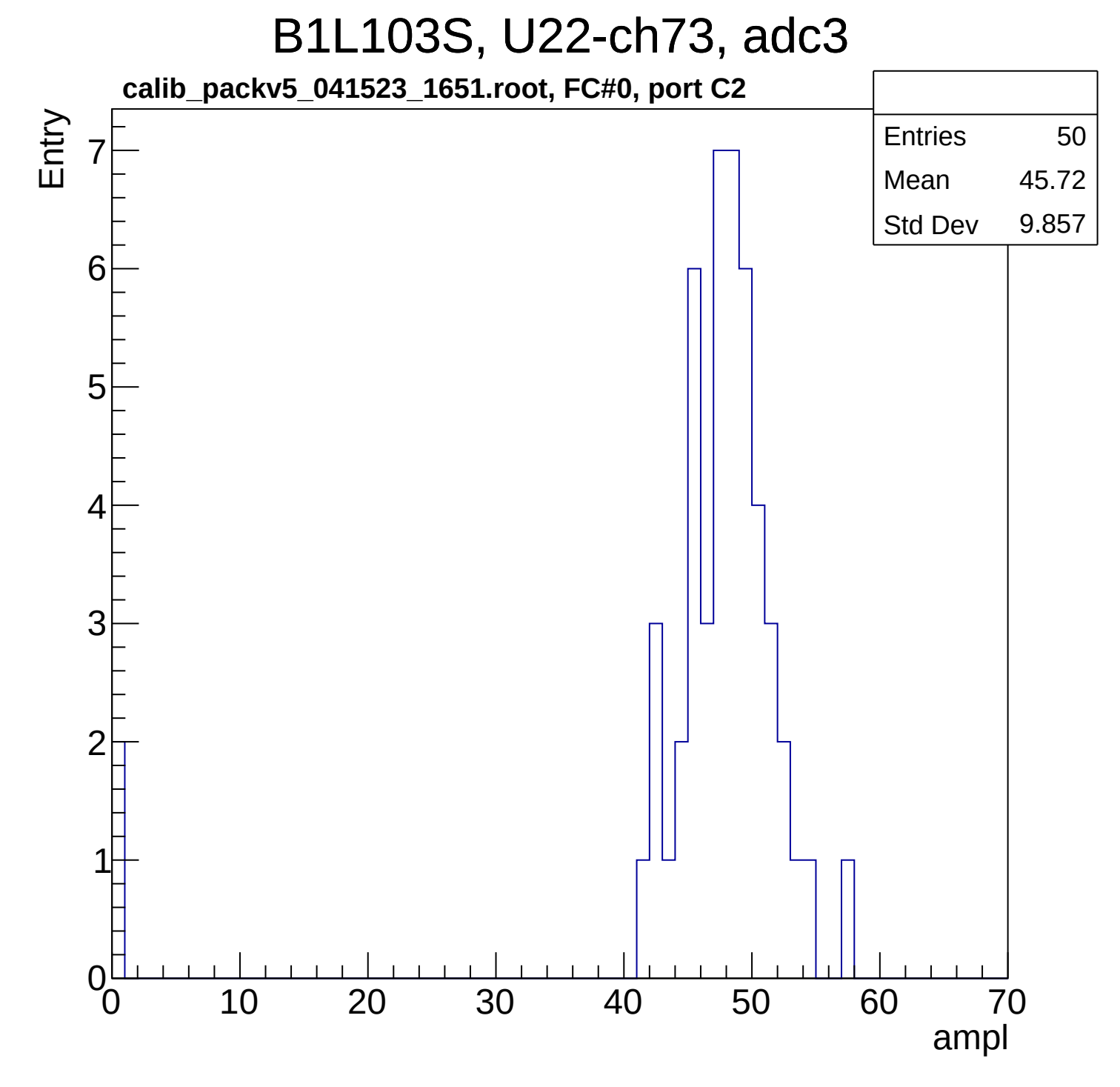
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

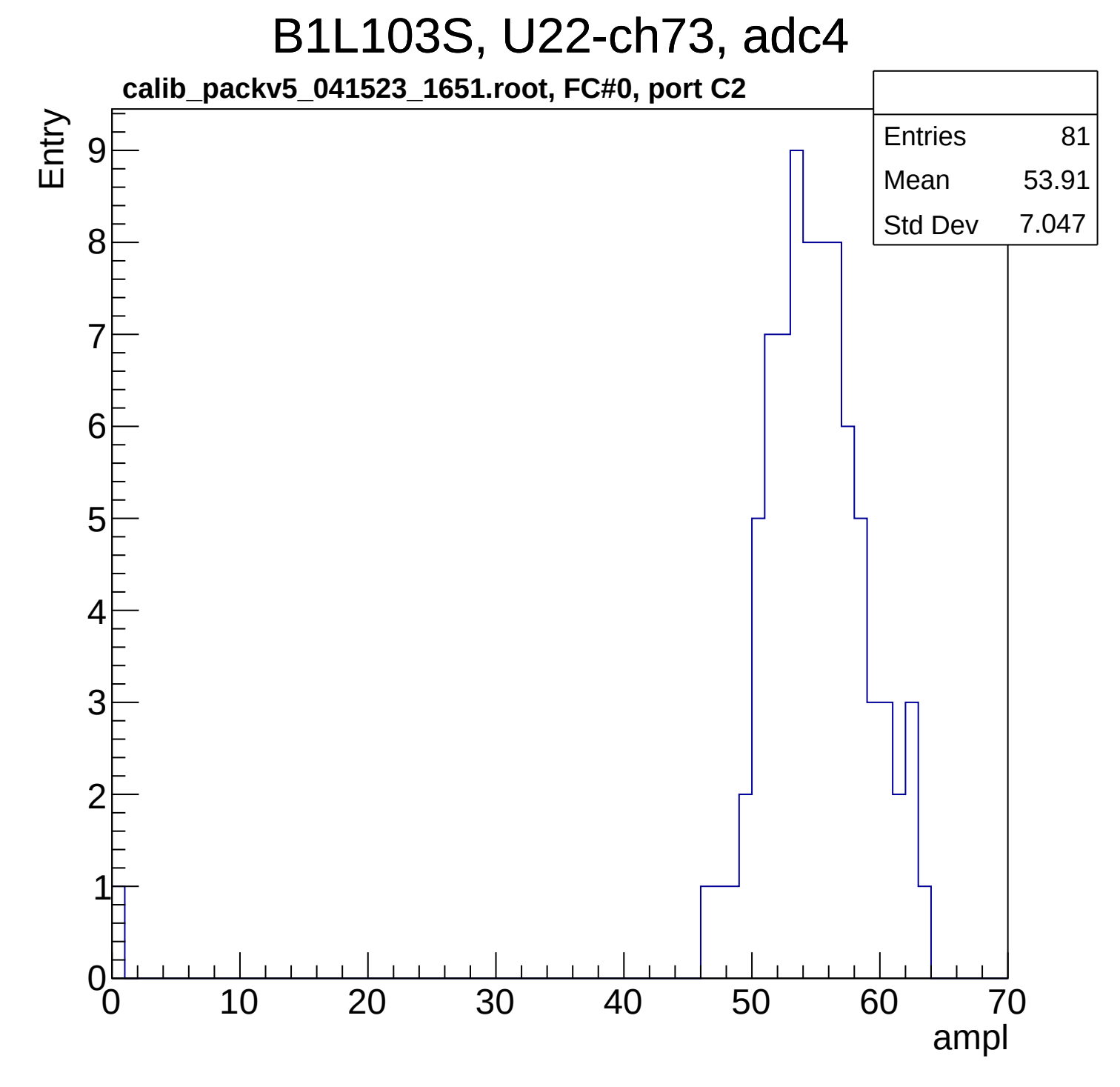

B1L103S, U22-ch72, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4
Std Dev 14.03
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

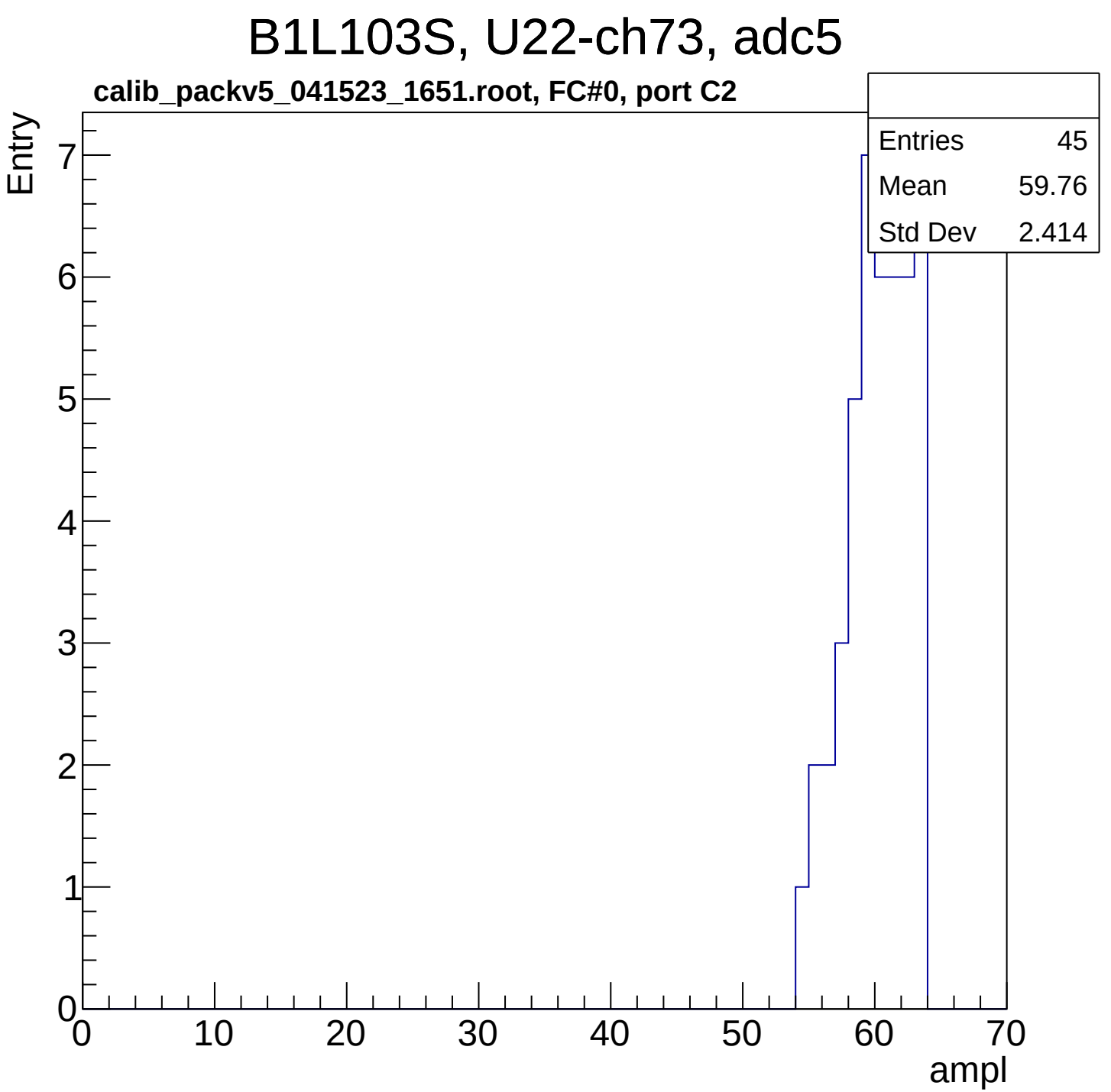

B1L103S, U22-ch73, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 118
Mean 18.14
Std Dev 13.58
Entry
ampl
0
5
10
15
20
25
30
35
40
0
10
20
30
40
50
60
70


B1L103S, U22-ch73, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 35.01
Std Dev 3.419
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch73, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 35.25
Std Dev 15.77
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch73, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 45.72
Std Dev 9.857
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U22-ch73, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 53.91
Std Dev 7.047
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch73, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 59.76
Std Dev 2.414
Entry
ampl
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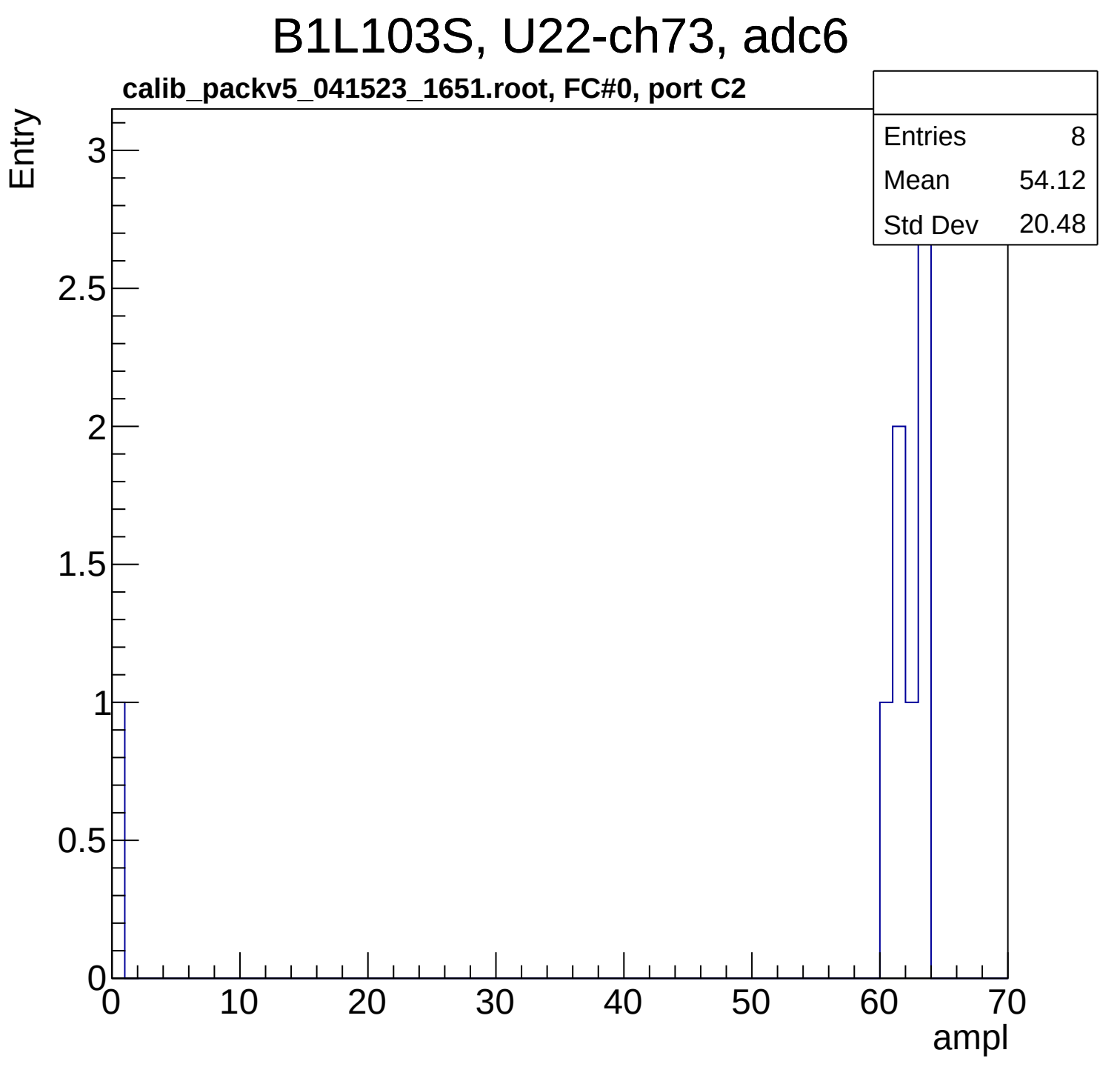
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U22-ch73, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 54.12
Std Dev 20.48
Entry
ampl
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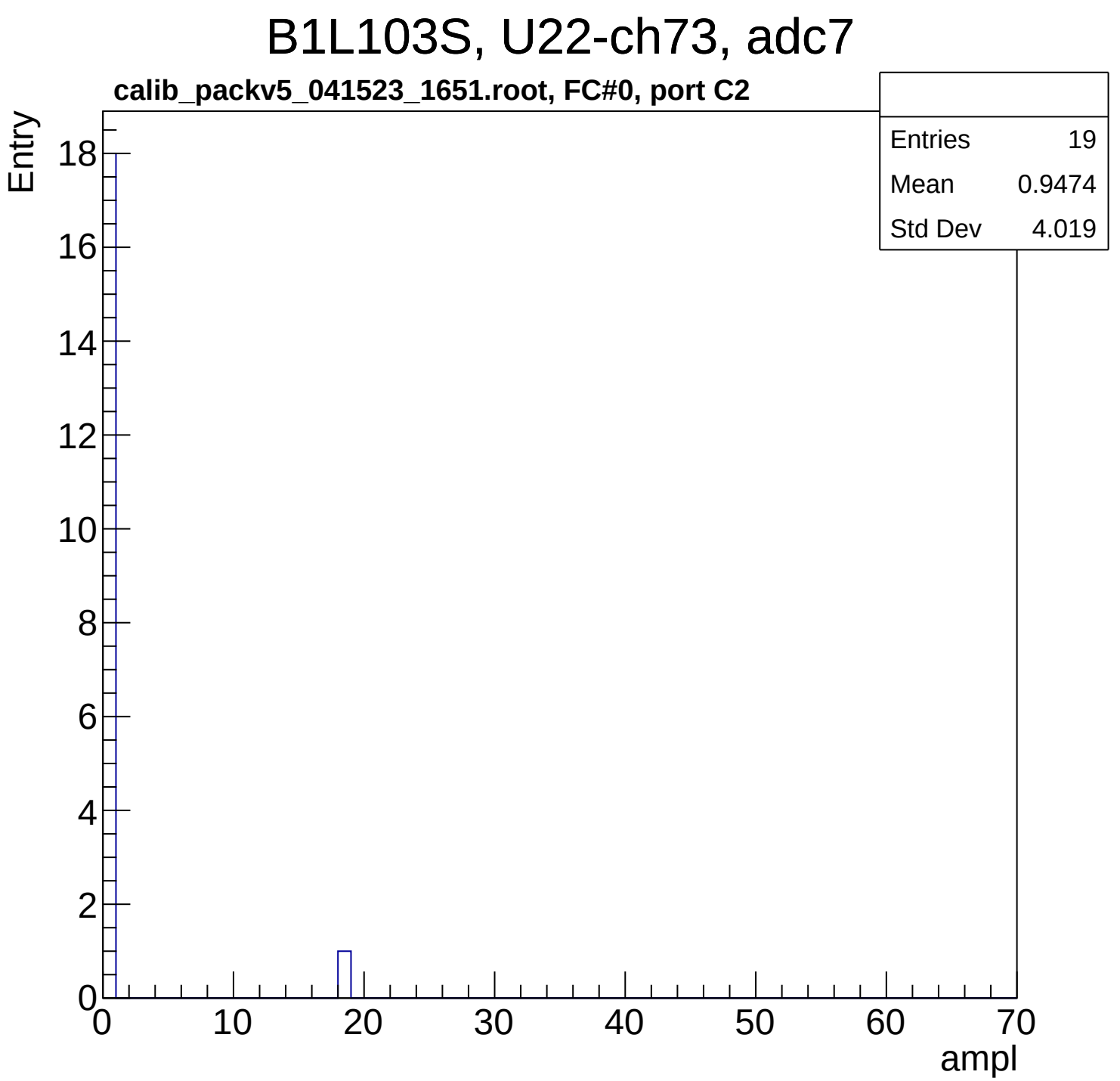
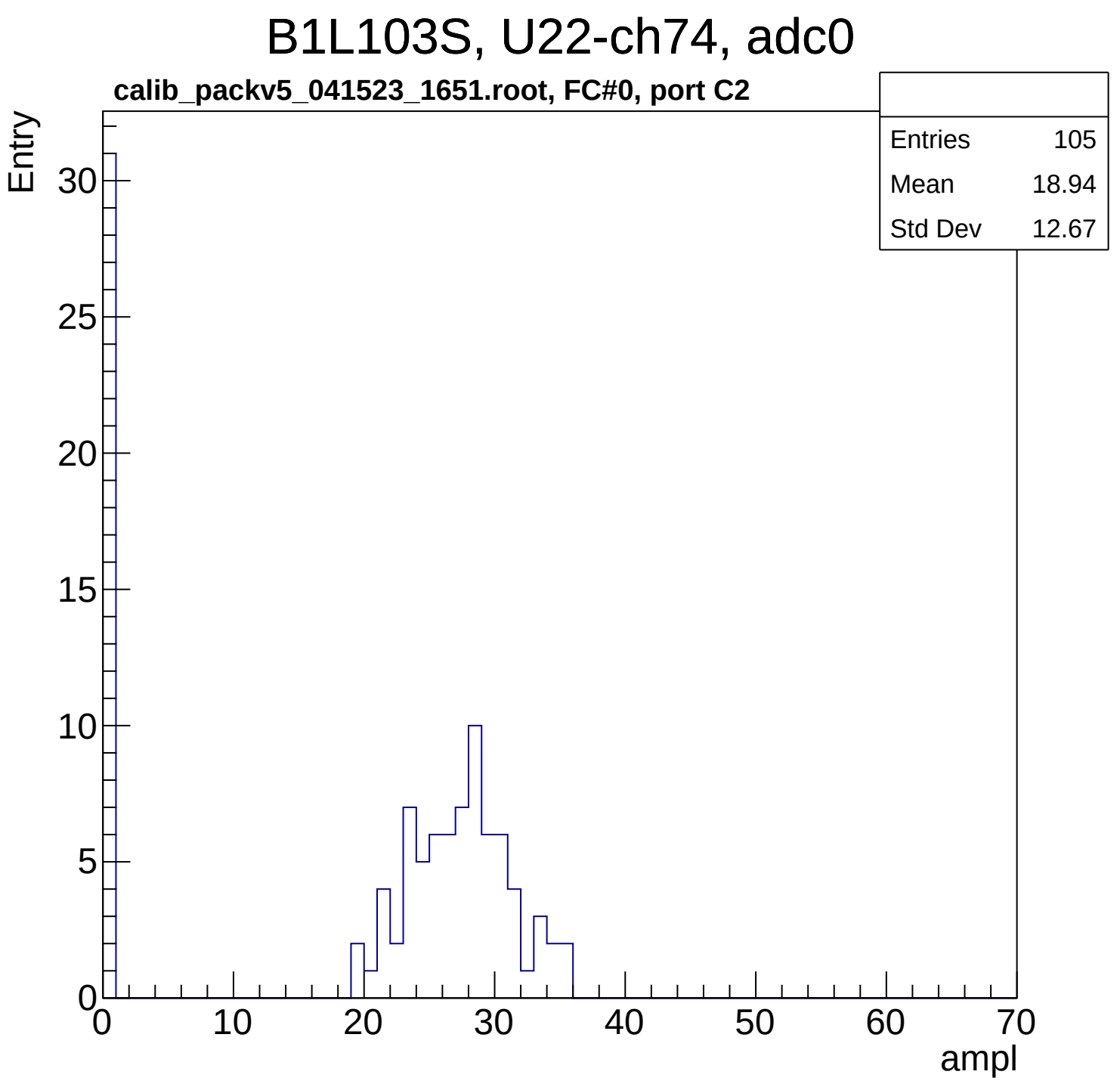
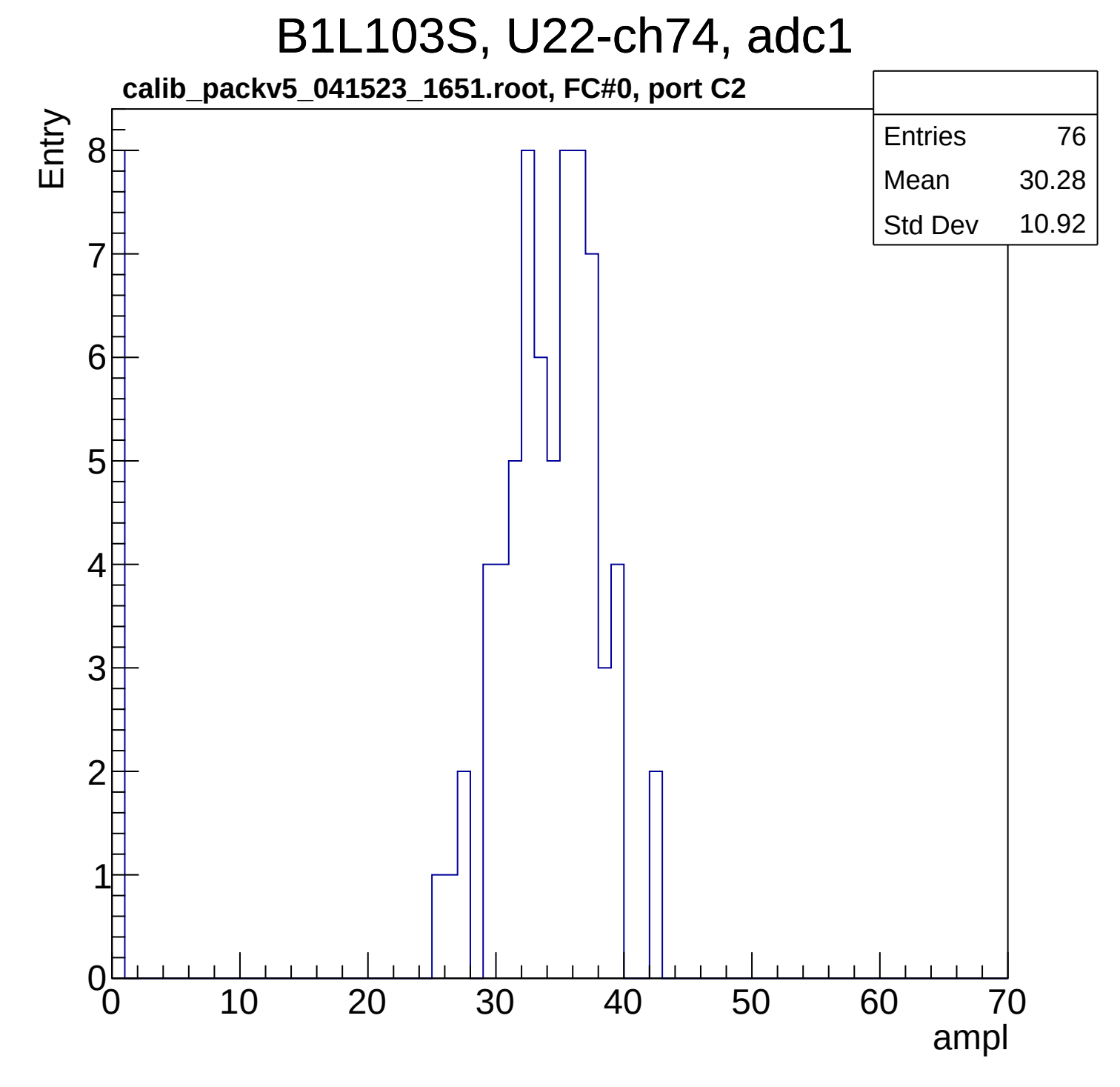
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U22-ch73, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0.9474
Std Dev 4.019
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch74, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 105
Mean 18.94
Std Dev 12.67
Entry
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch74, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 30.28
Std Dev 10.92
Entry
ampl
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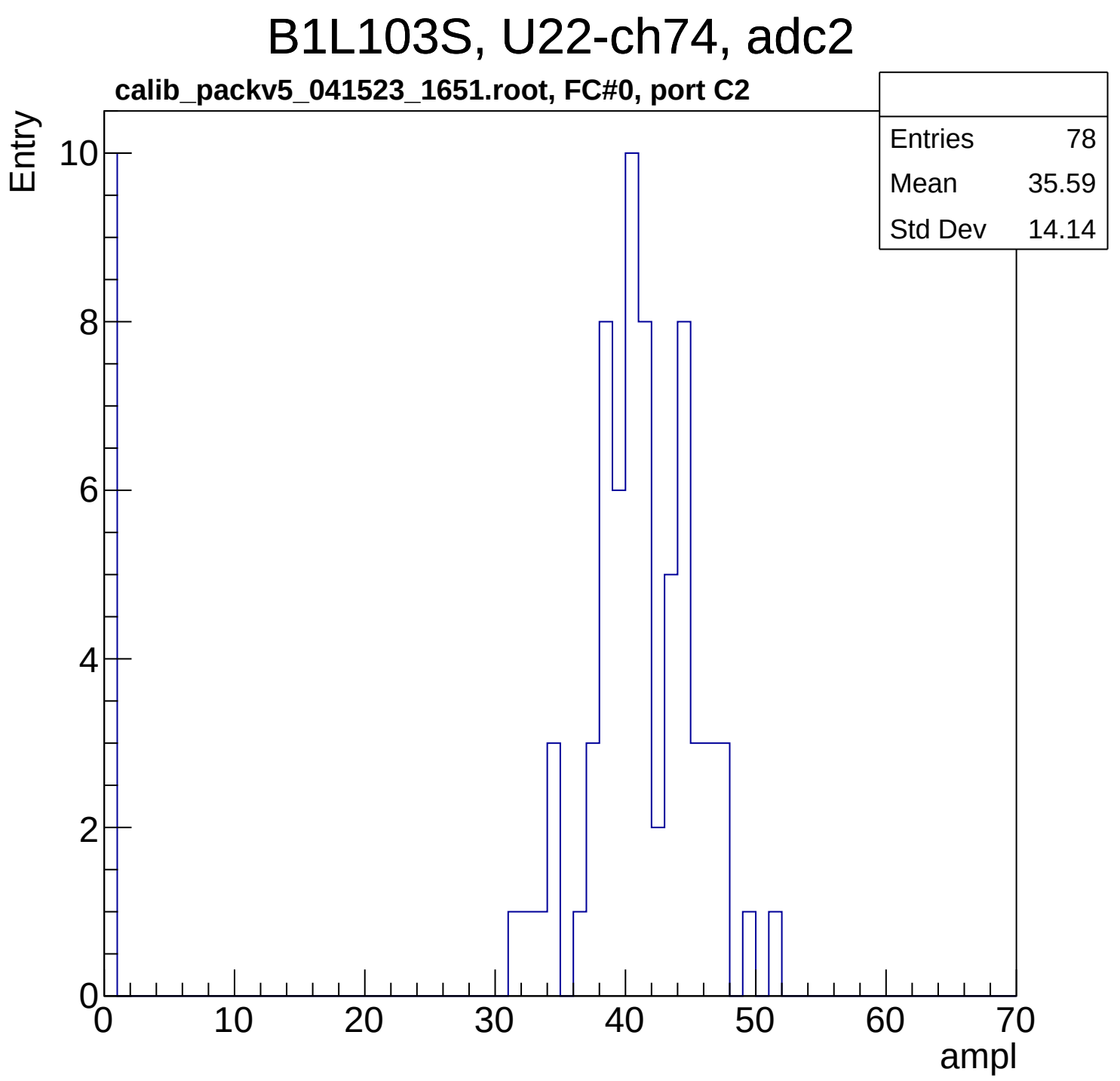
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch74, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 35.59
Std Dev 14.14
Entry
ampl
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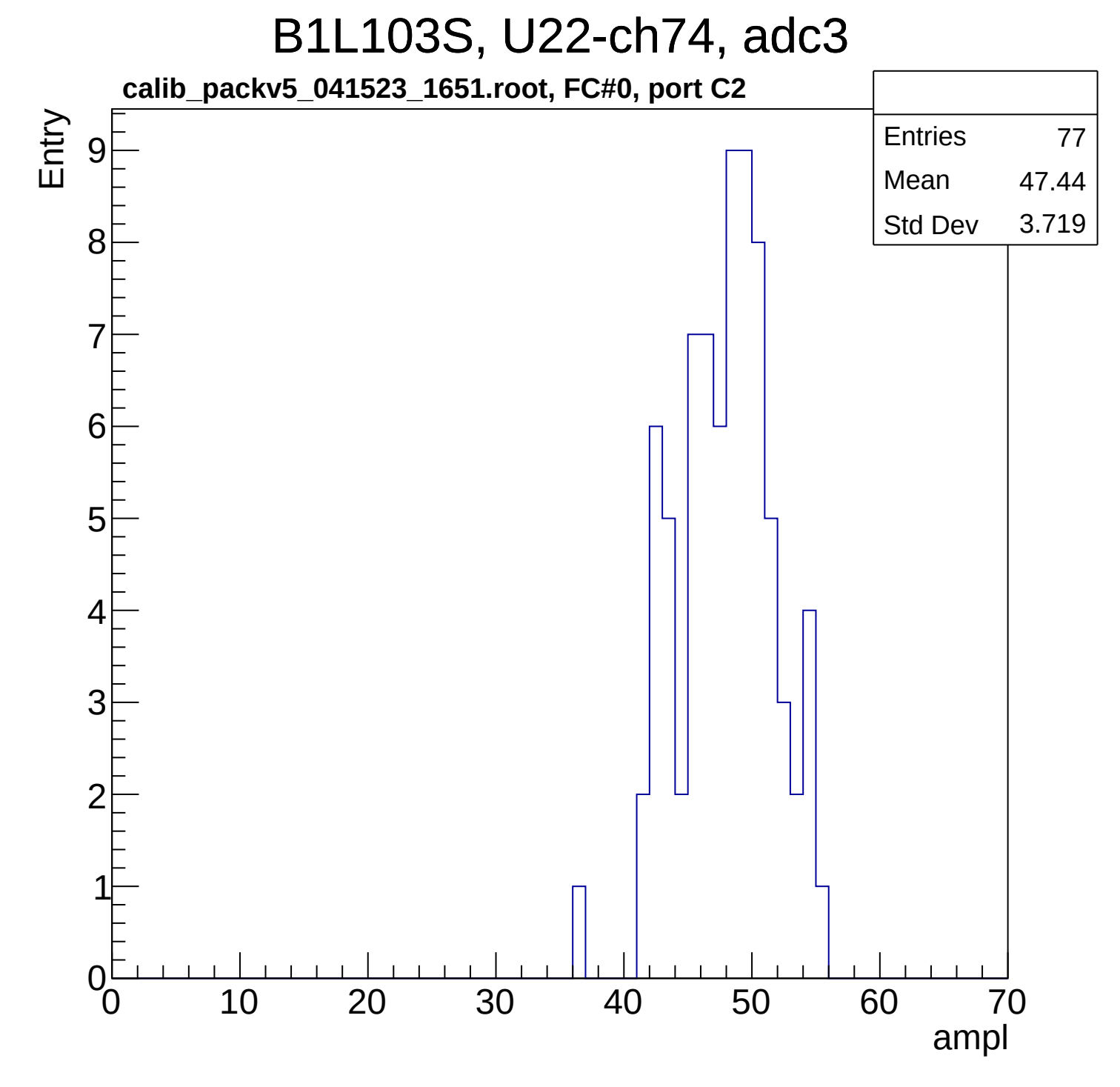
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U22-ch74, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 47.44
Std Dev 3.719
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
10
20
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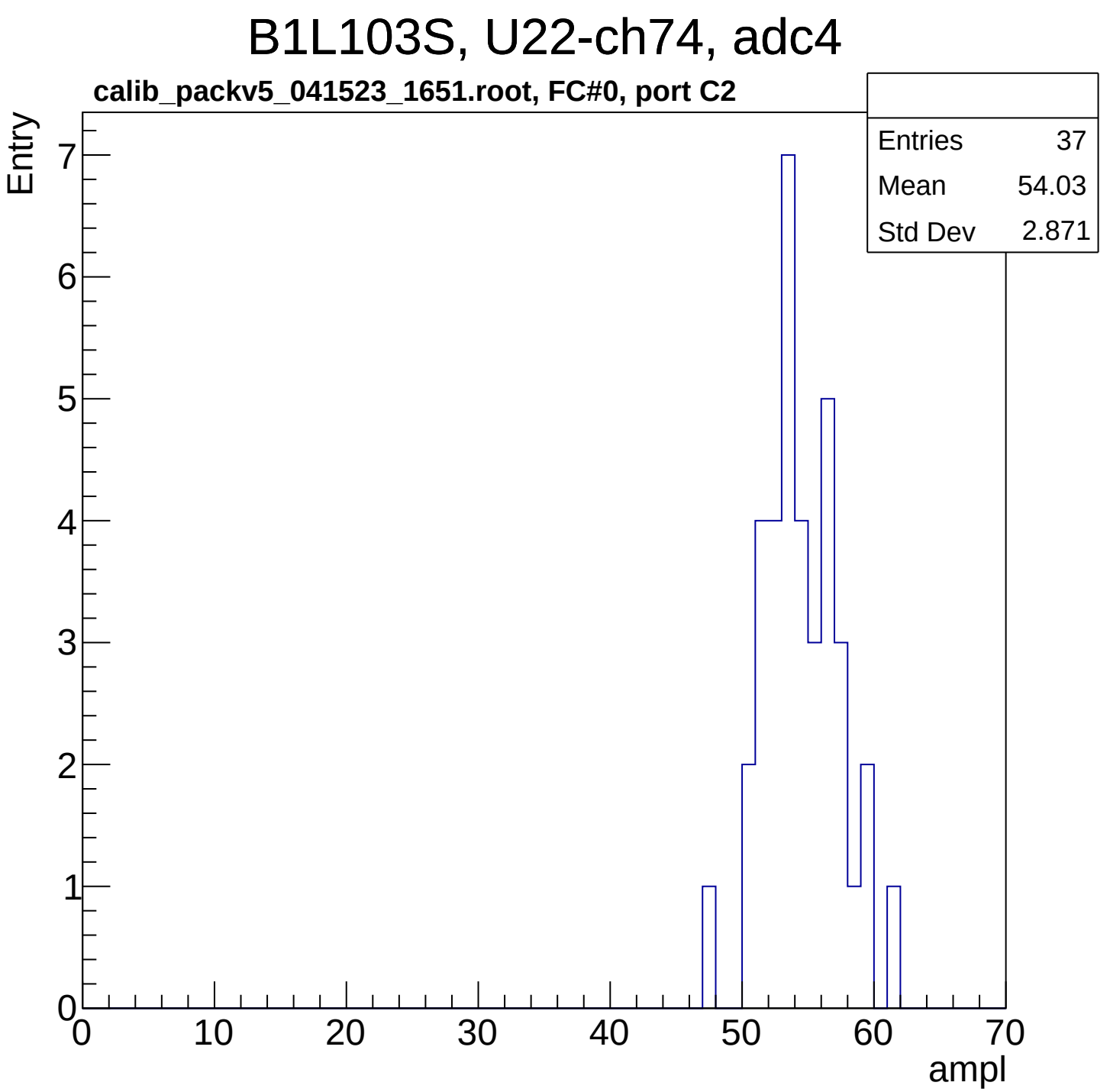
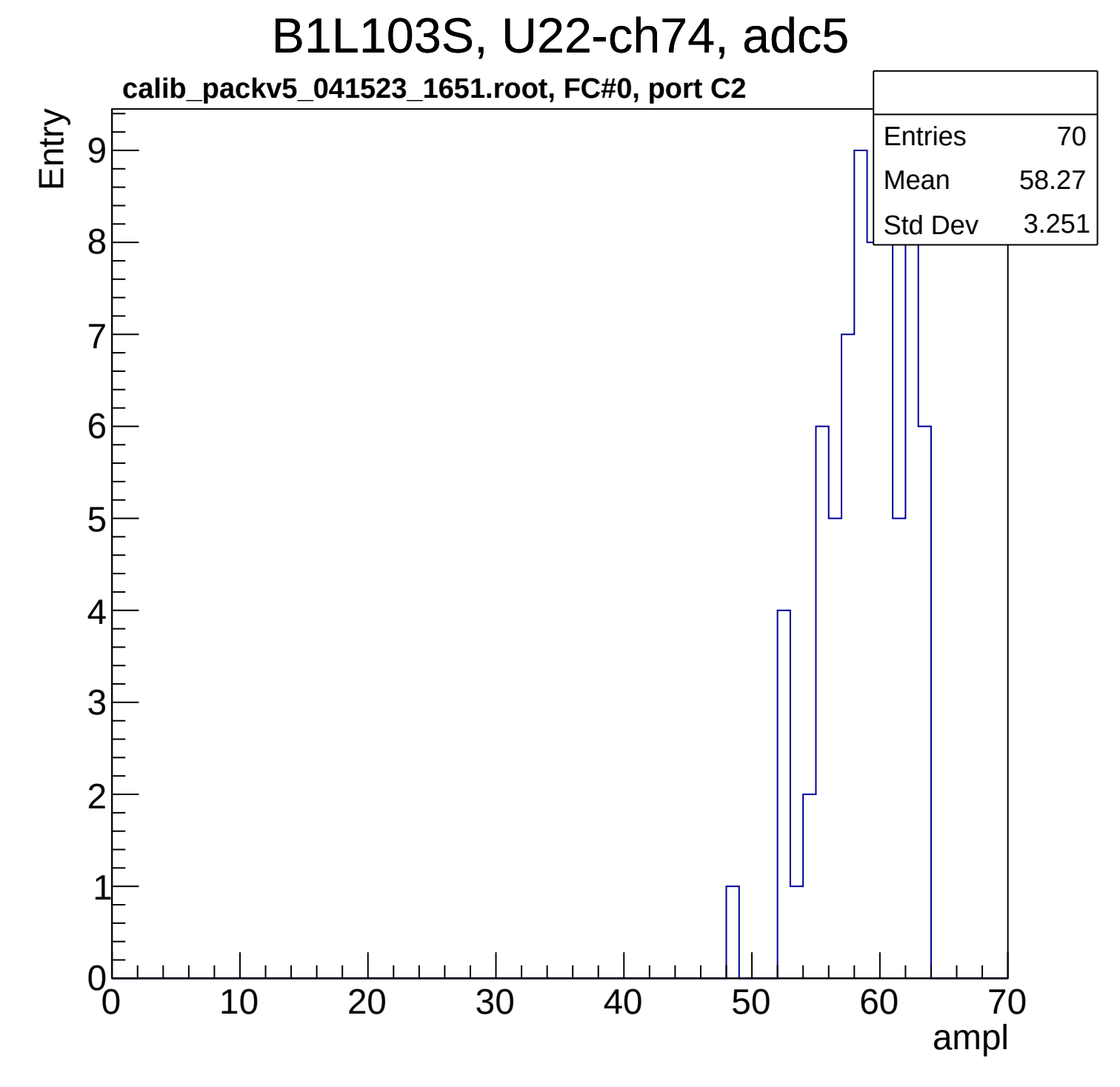
50
60
70


B1L103S, U22-ch74, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 54.03
Std Dev 2.871
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U22-ch74, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 58.27
Std Dev 3.251
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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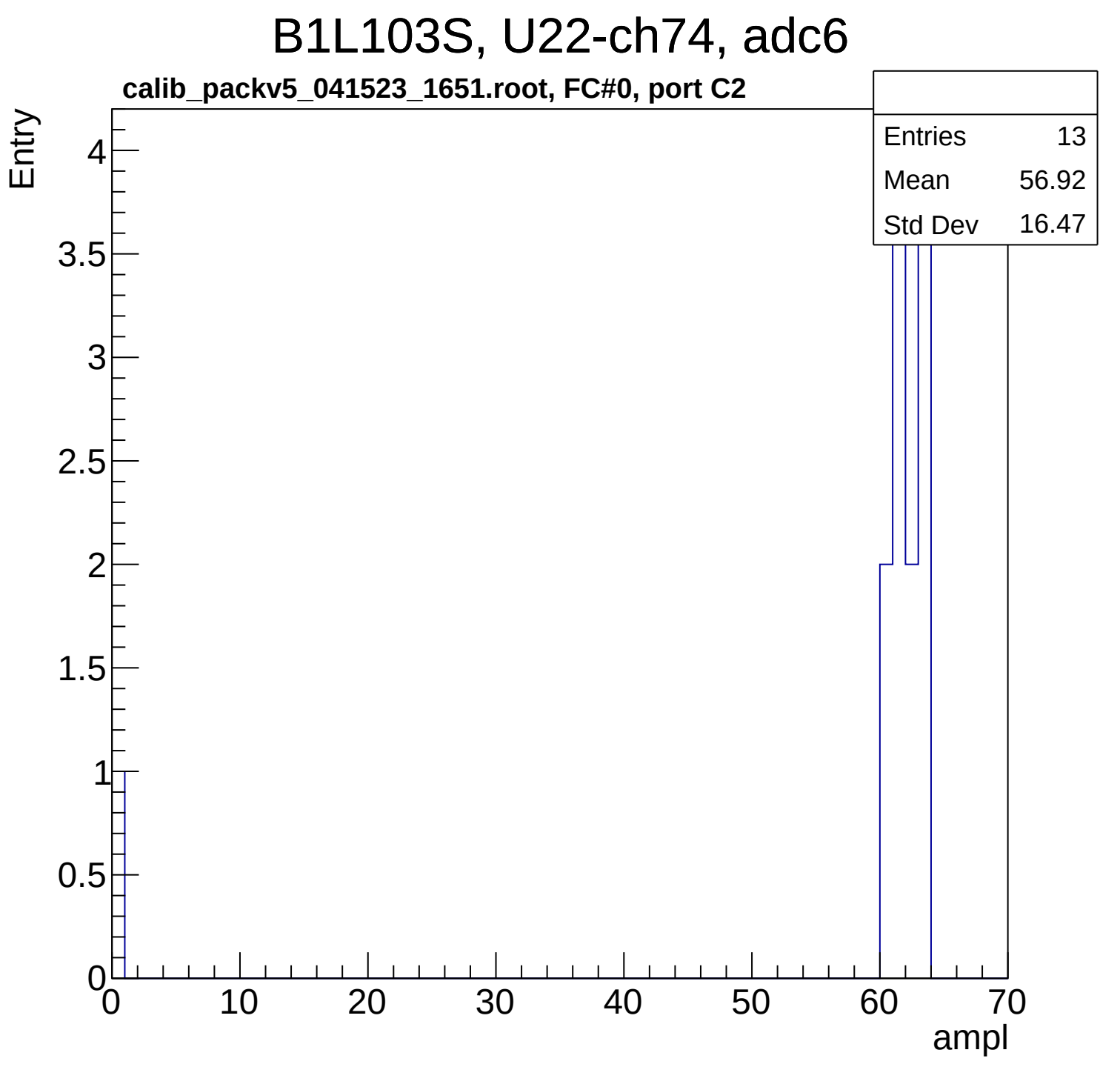
60
70


B1L103S, U22-ch74, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 56.92
Std Dev 16.47
Entry
ampl
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0.5
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1.5
2
2.5
3
3.5
4
0
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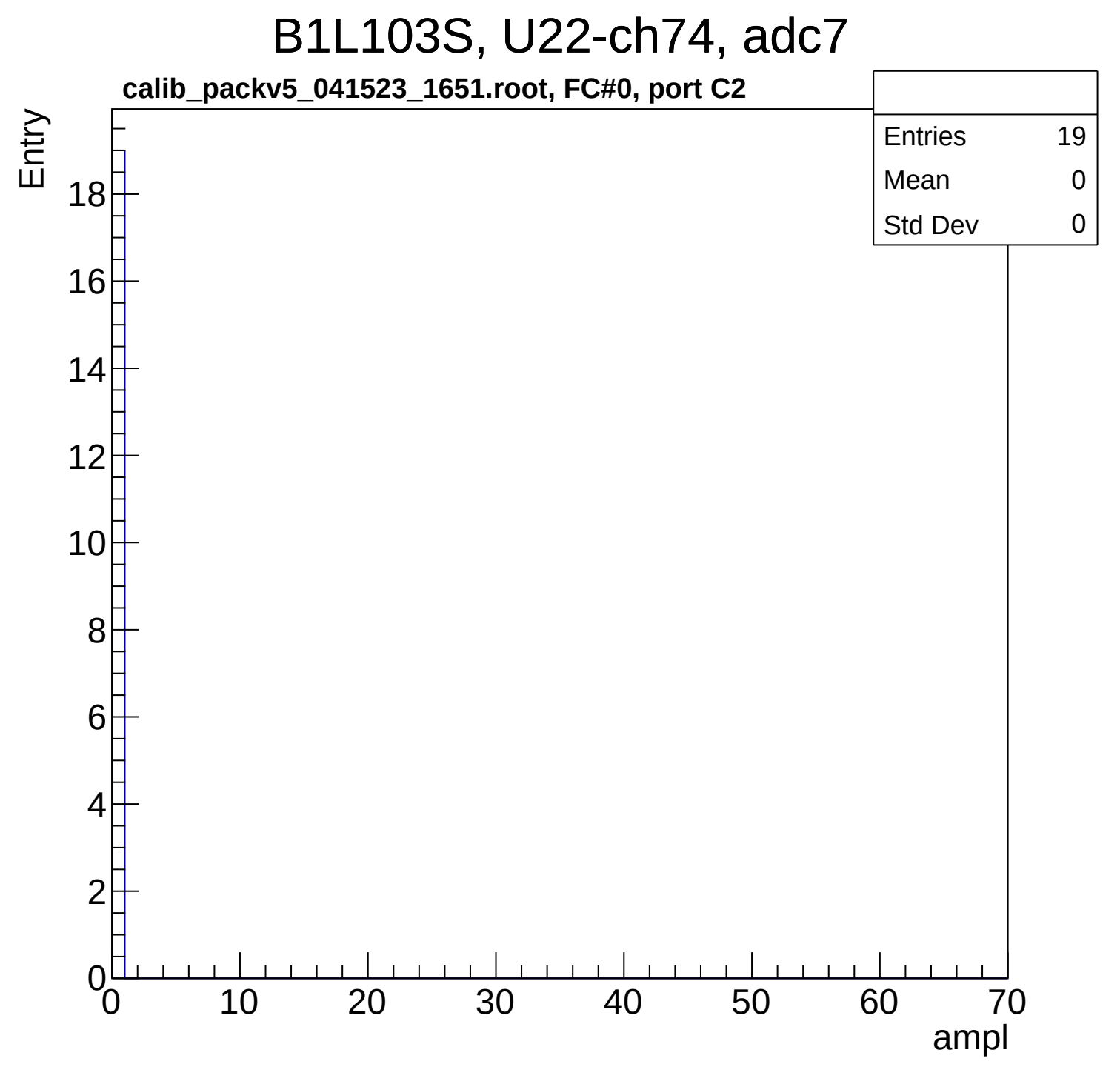
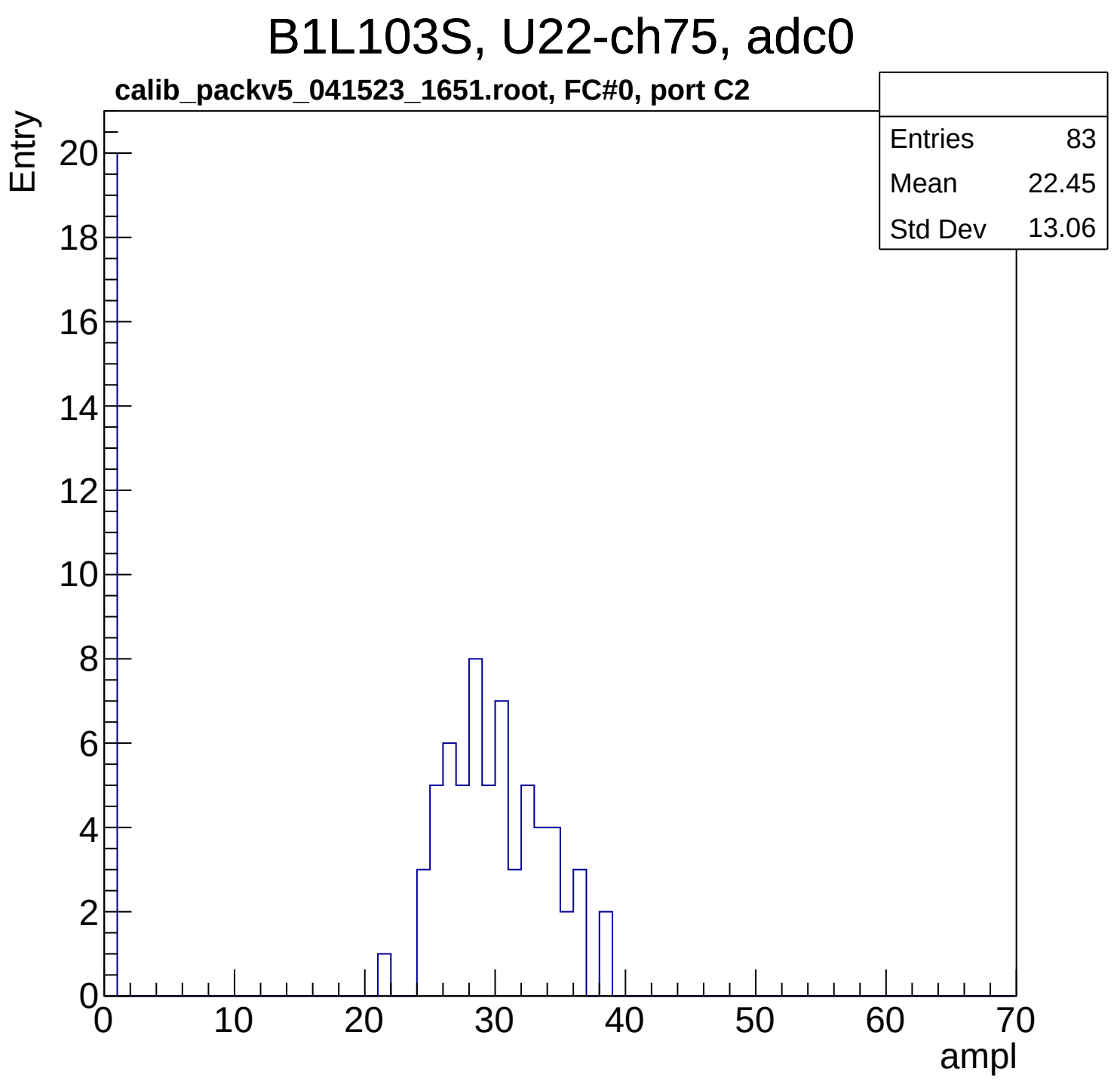
20
30
40
50
60
70


B1L103S, U22-ch74, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch75, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 22.45
Std Dev 13.06
Entry
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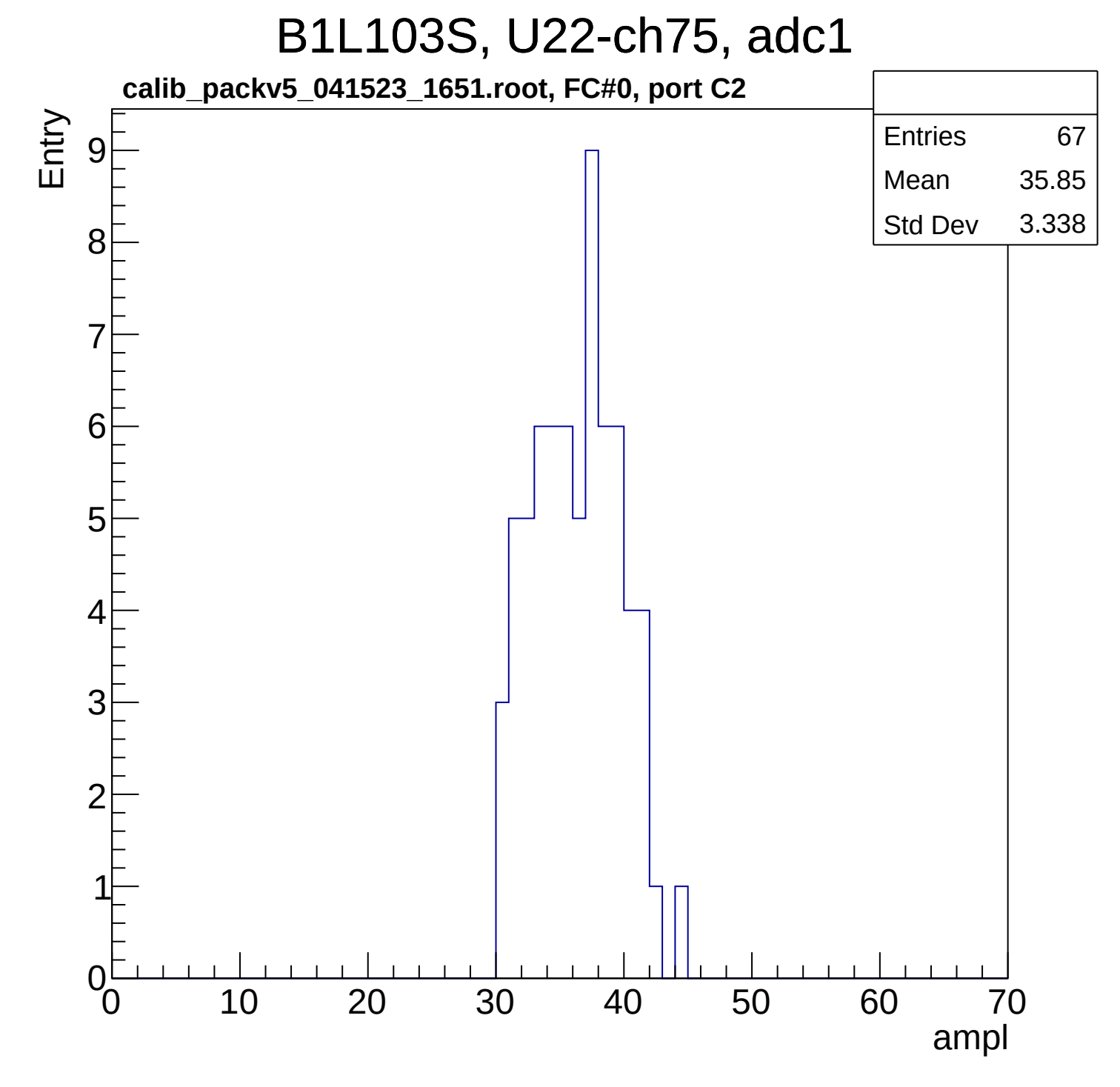
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch75, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 35.85
Std Dev 3.338
Entry
ampl
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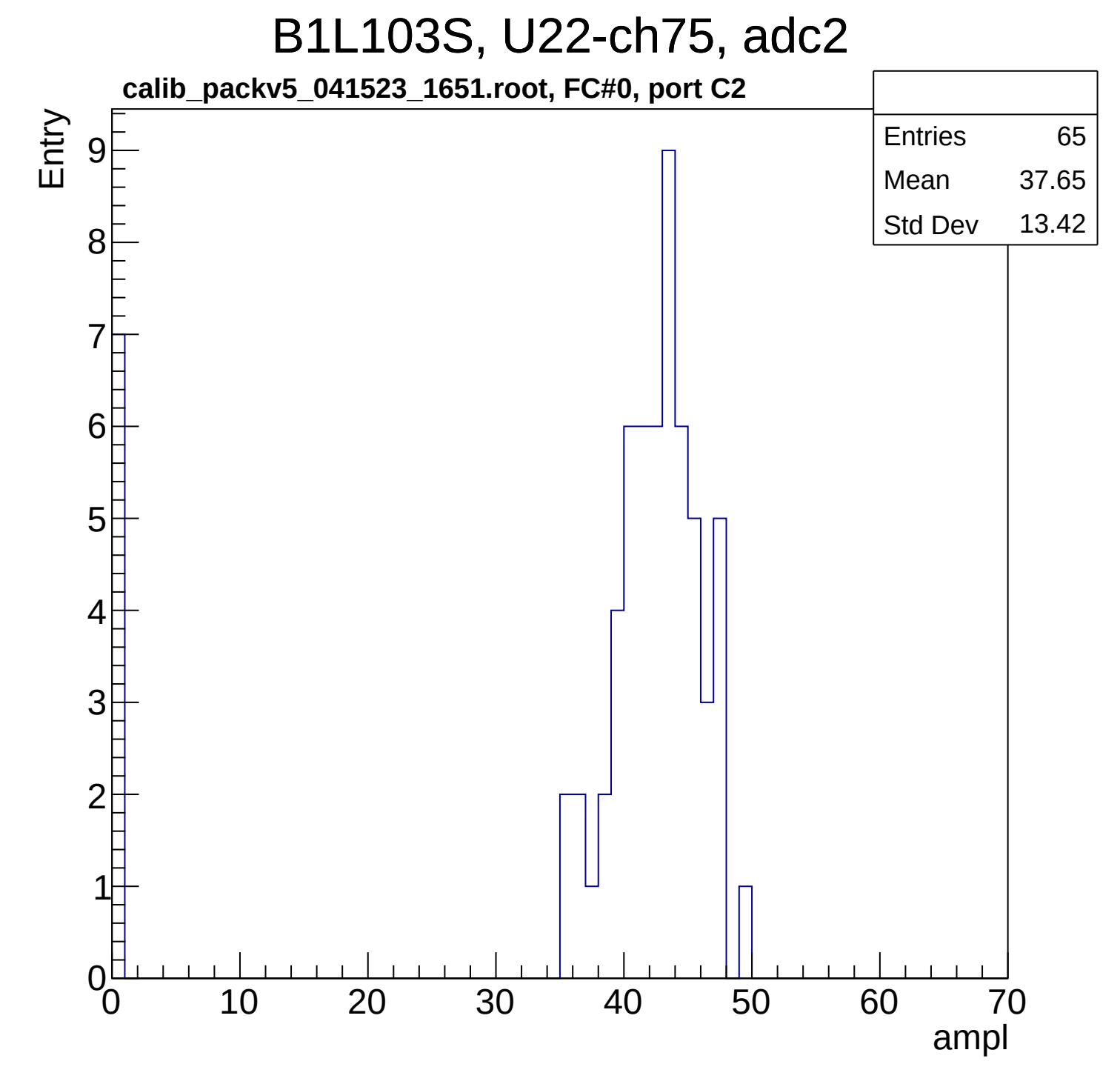
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch75, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 37.65
Std Dev 13.42
Entry
ampl
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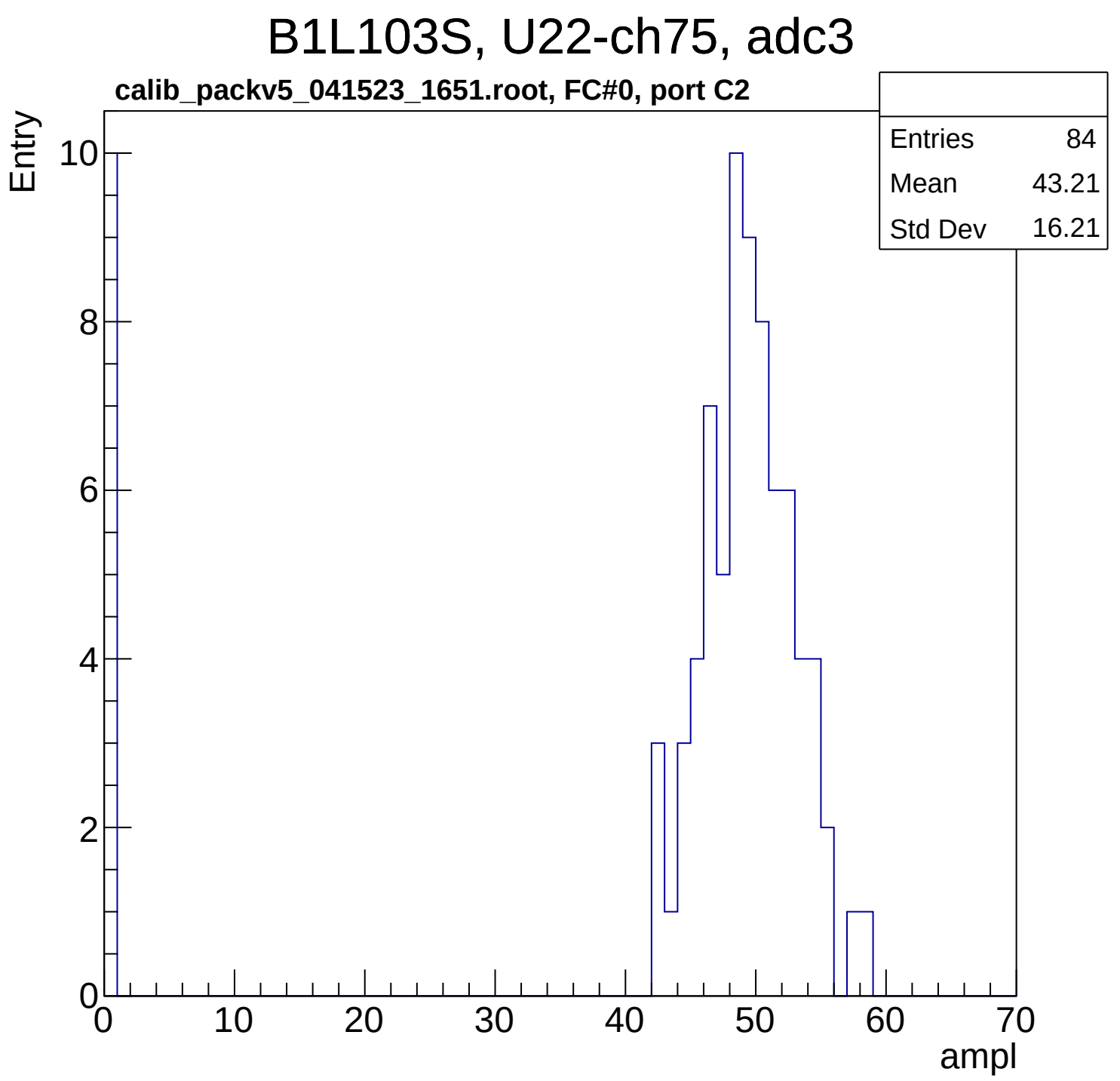
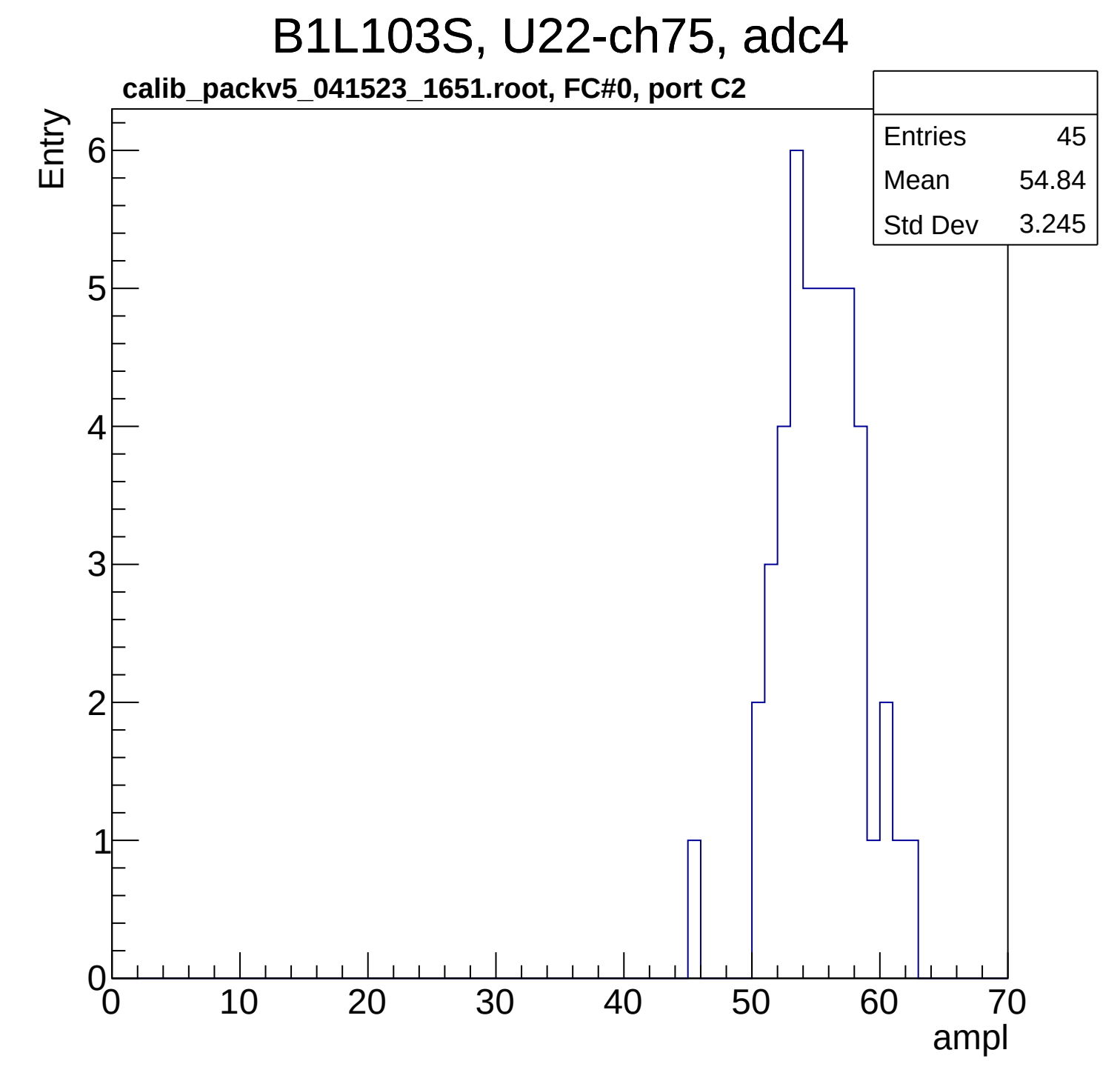
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch75, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 43.21
Std Dev 16.21
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U22-ch75, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 54.84
Std Dev 3.245
Entry
ampl
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2
3
4
5
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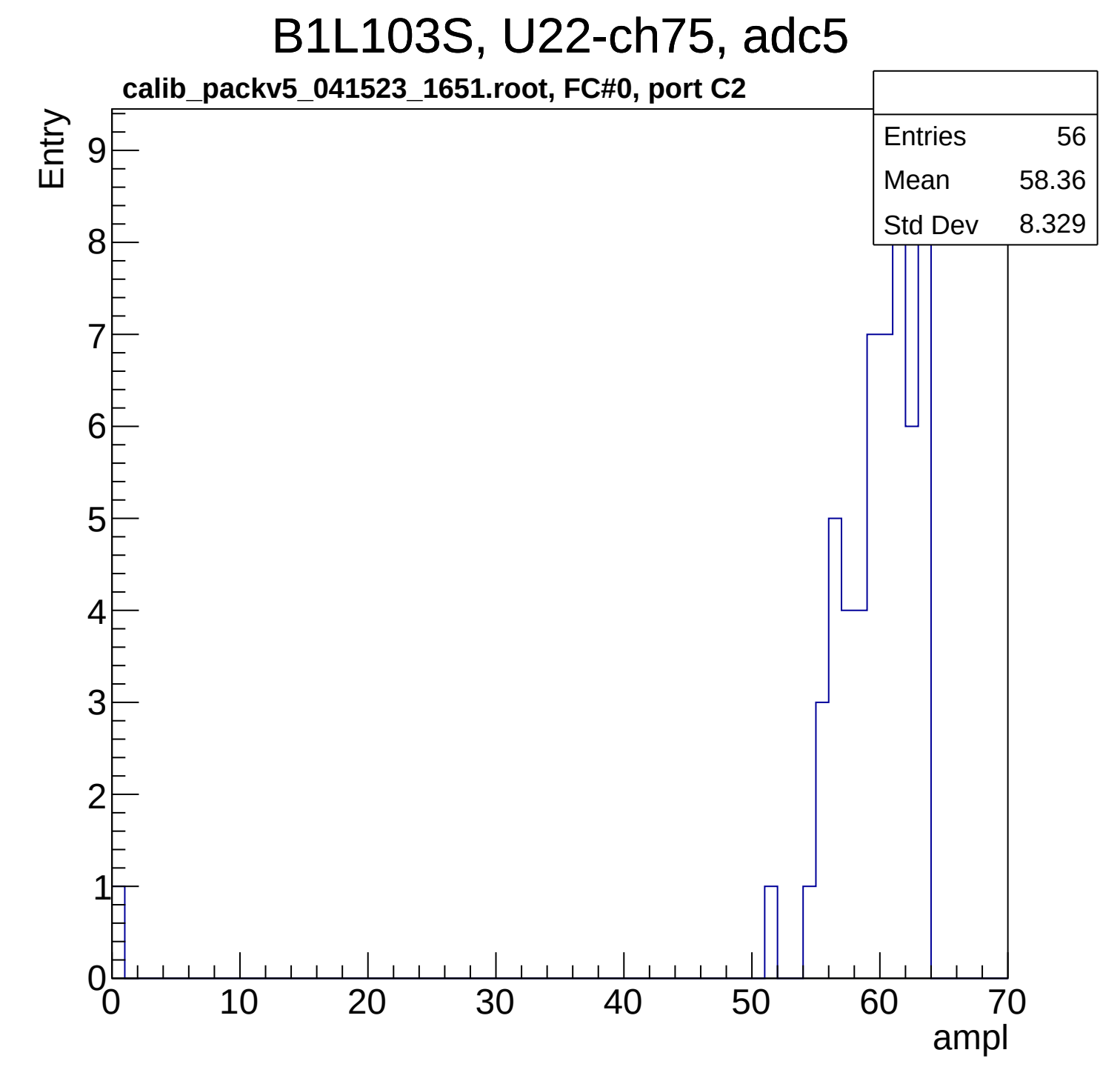
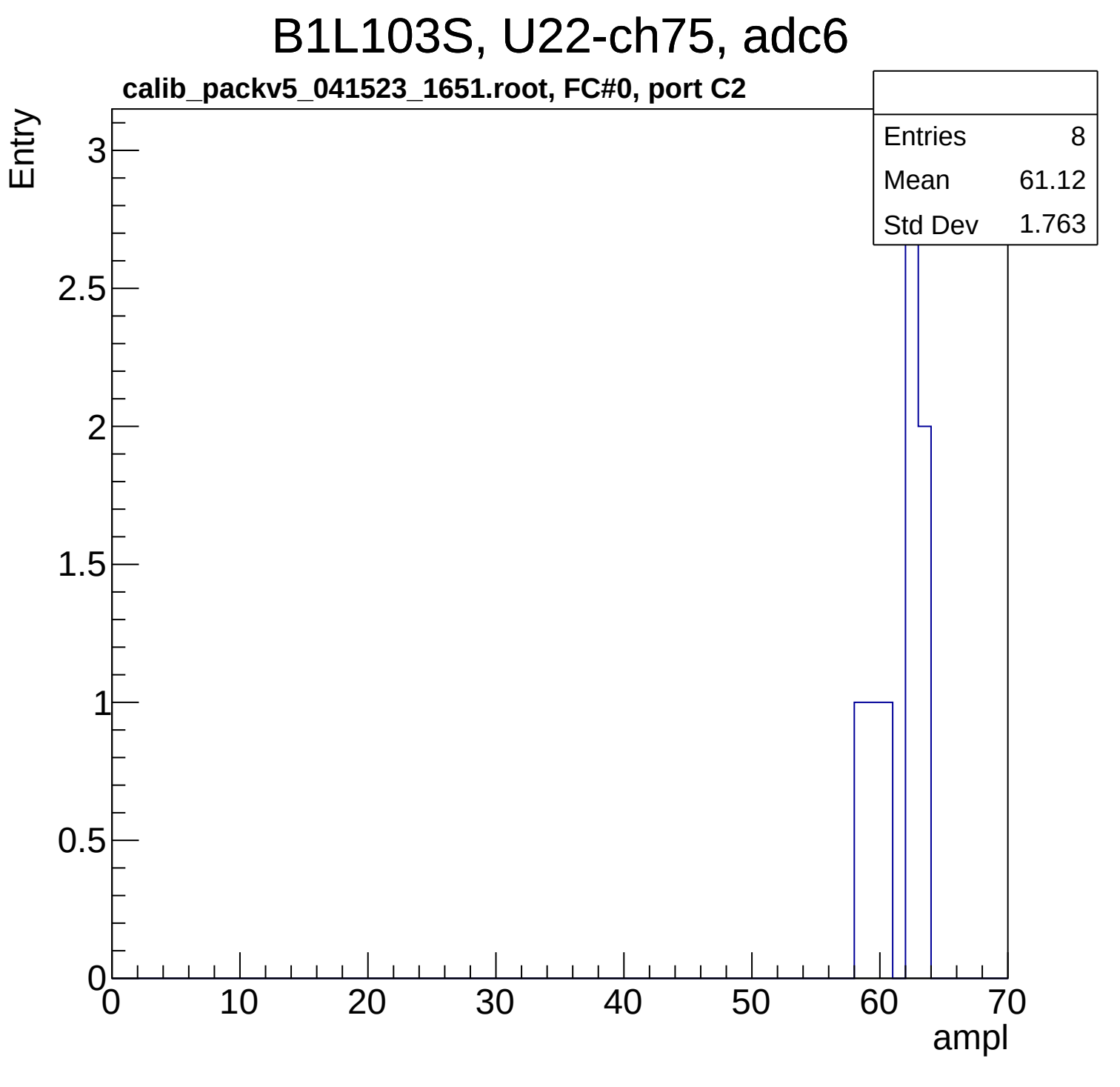
0
10
20
30
40
50
60
70


B1L103S, U22-ch75, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 58.36
Std Dev 8.329
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch75, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 61.12
Std Dev 1.763
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
30
40
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60
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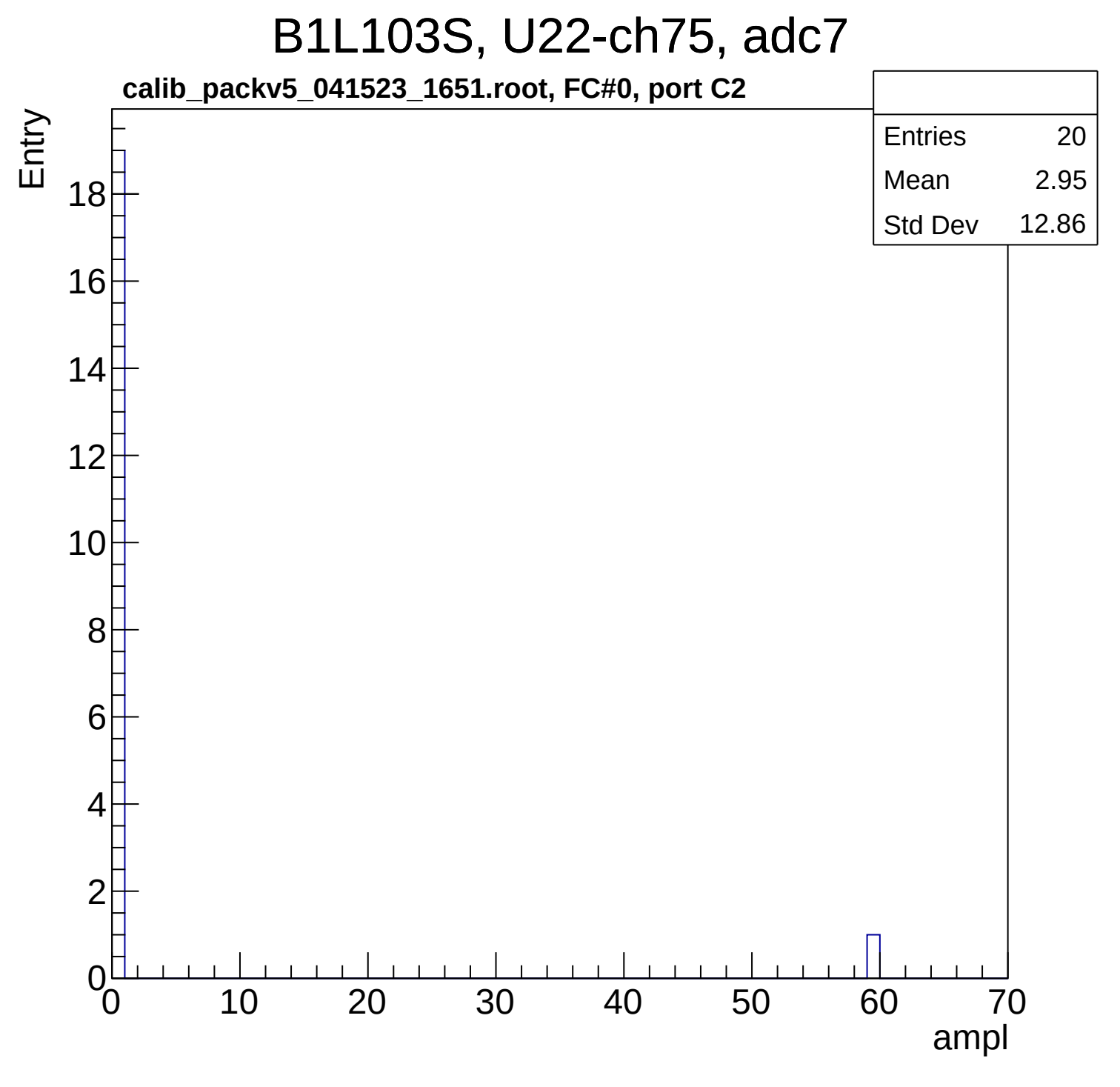
B1L103S, U22-ch75, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 2.95
Std Dev 12.86
Entry
0
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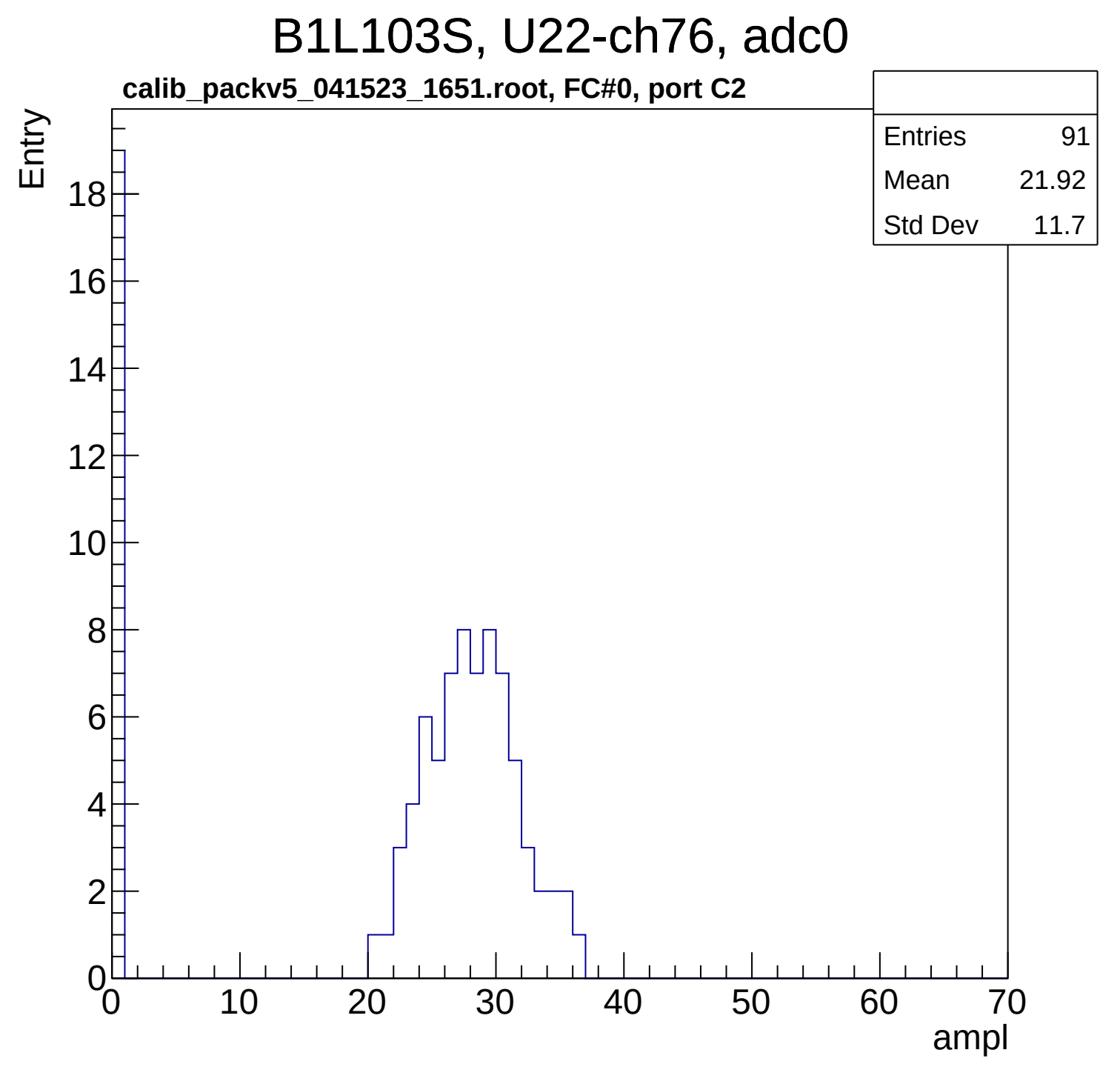
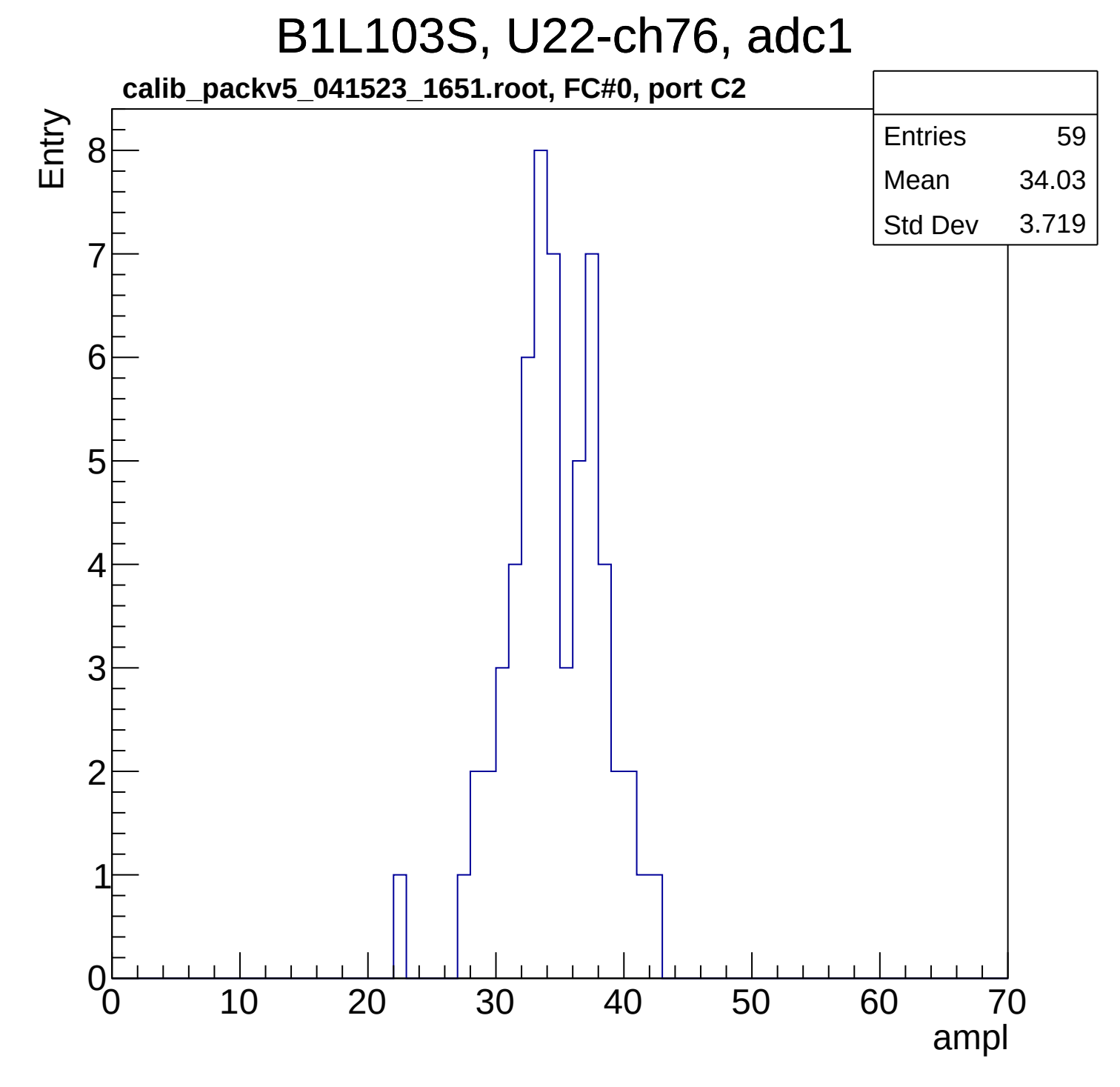
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch76, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 21.92
Std Dev 11.7
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch76, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 34.03
Std Dev 3.719
Entry
ampl
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2
3
4
5
6
7
8
0
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20
30
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60
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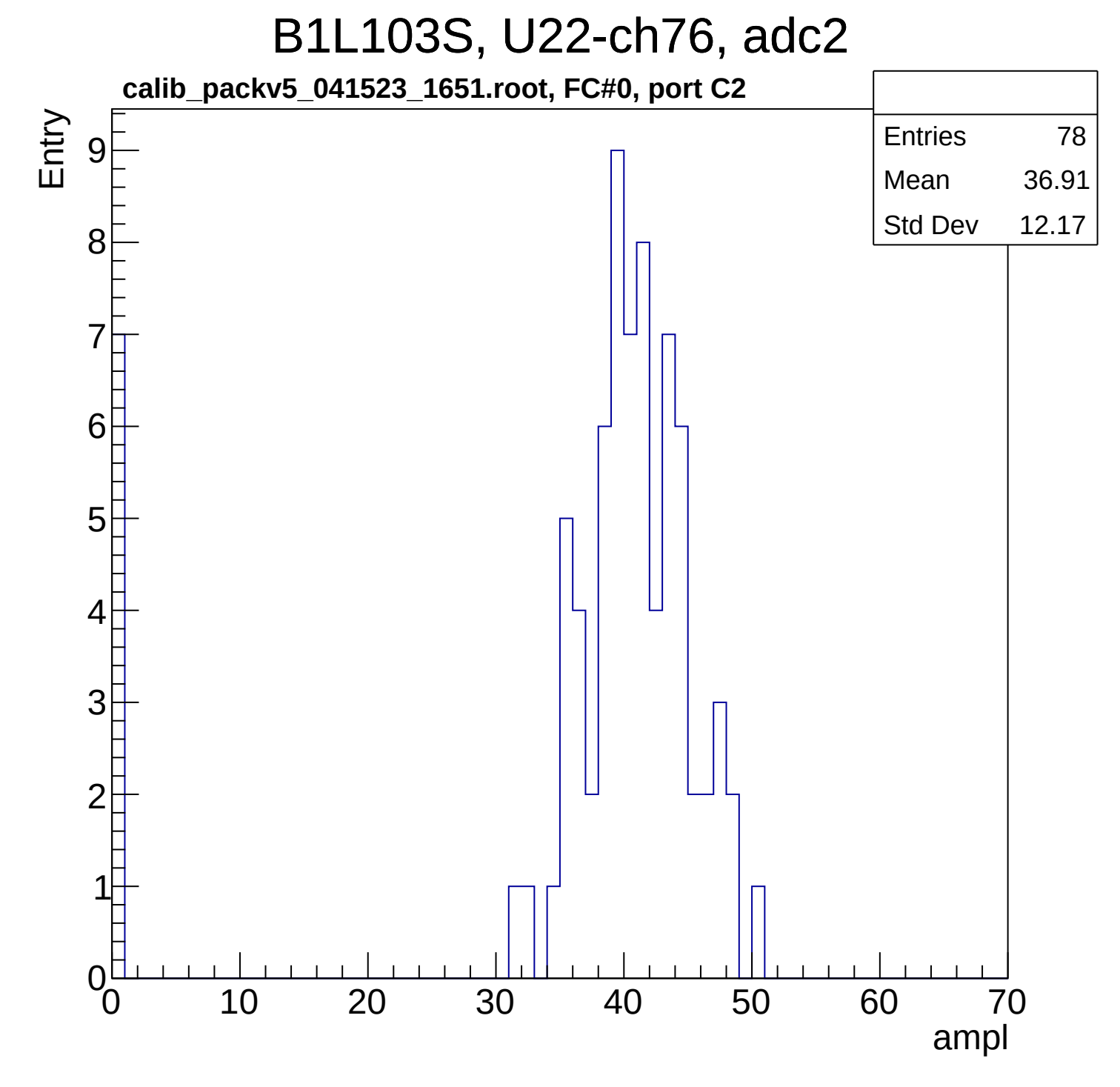
B1L103S, U22-ch76, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 36.91
Std Dev 12.17
Entry
ampl
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3
4
5
6
7
8
9
0
10
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40
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60
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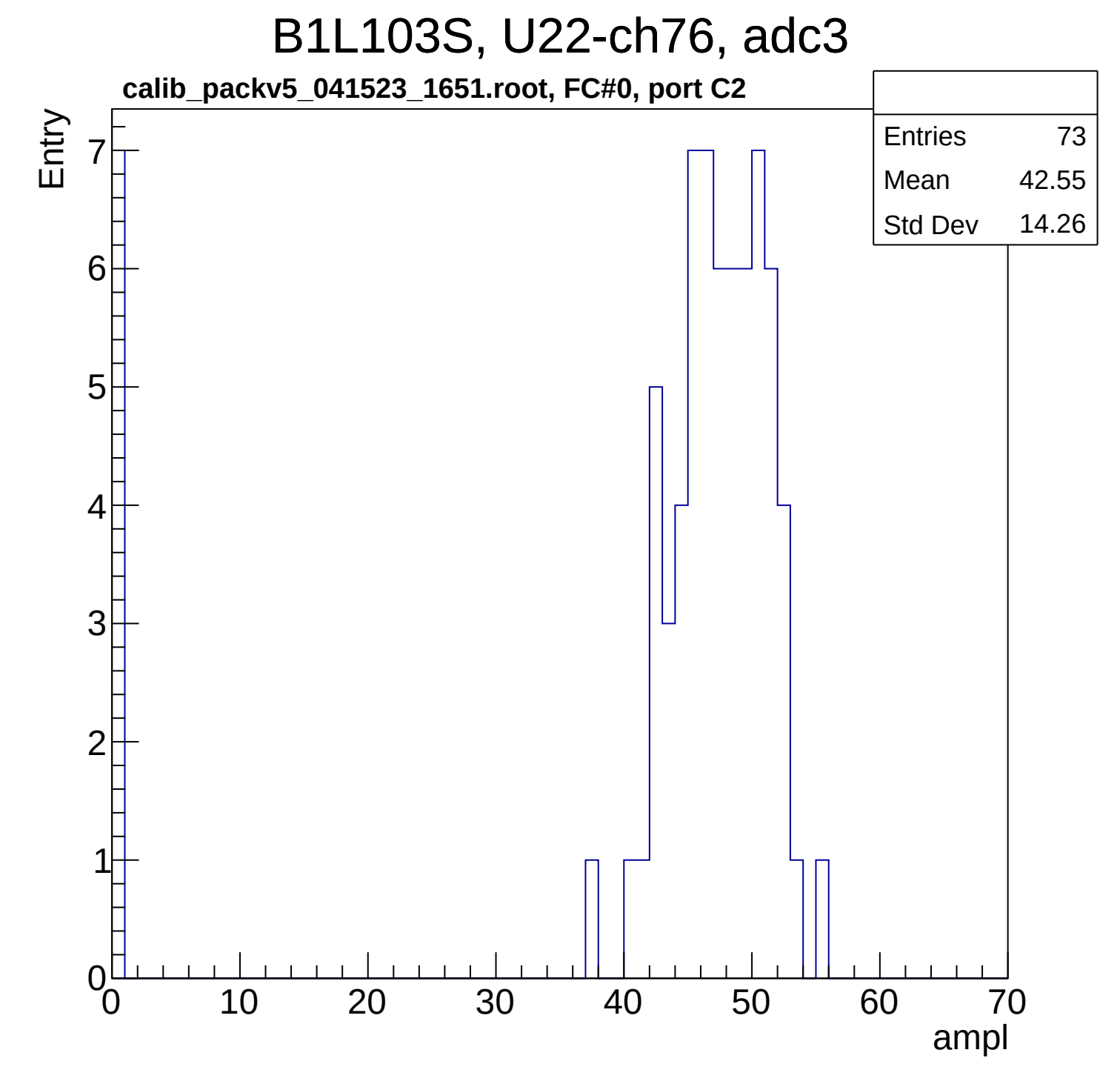
B1L103S, U22-ch76, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 42.55
Std Dev 14.26
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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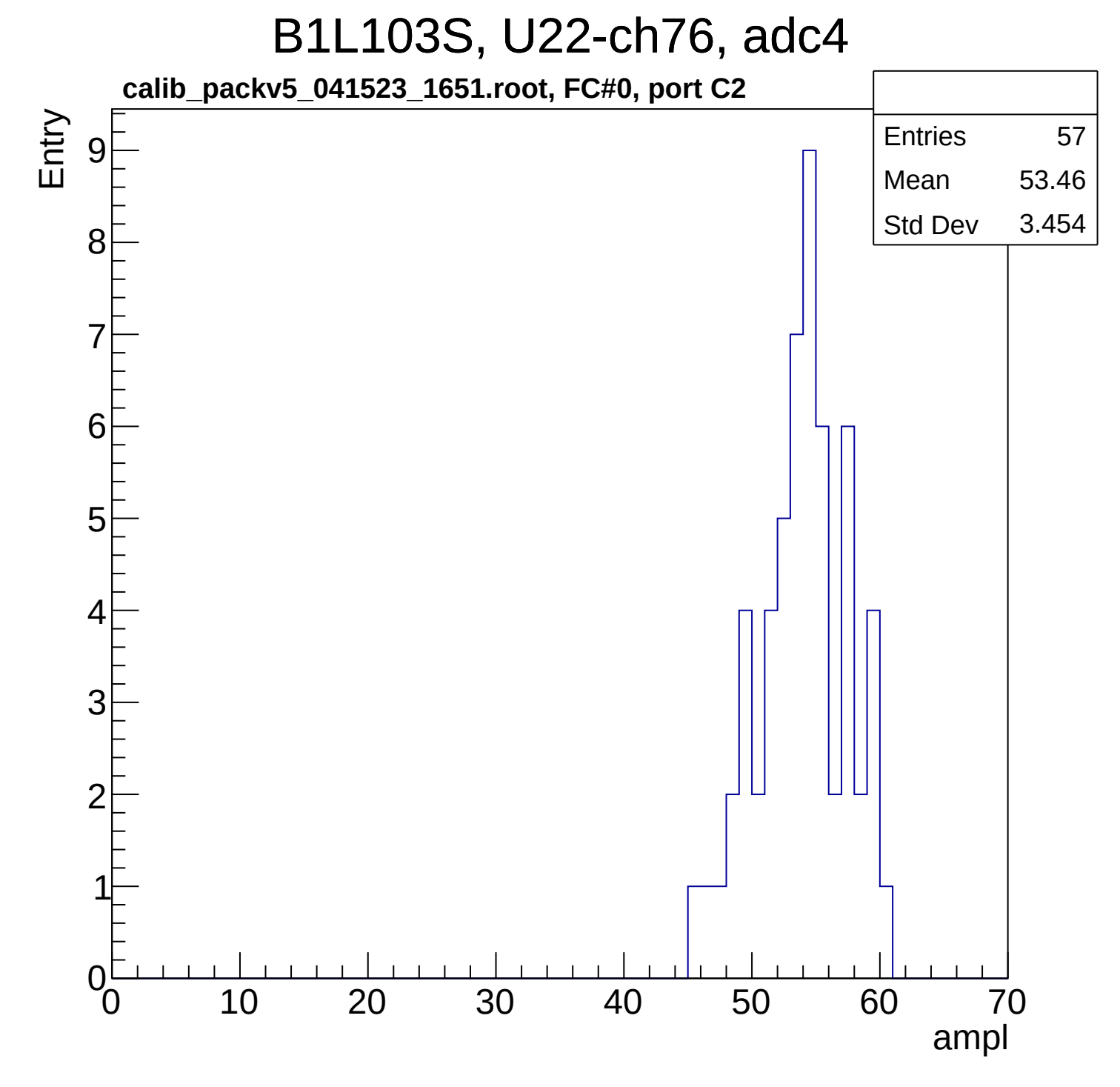
B1L103S, U22-ch76, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 53.46
Std Dev 3.454
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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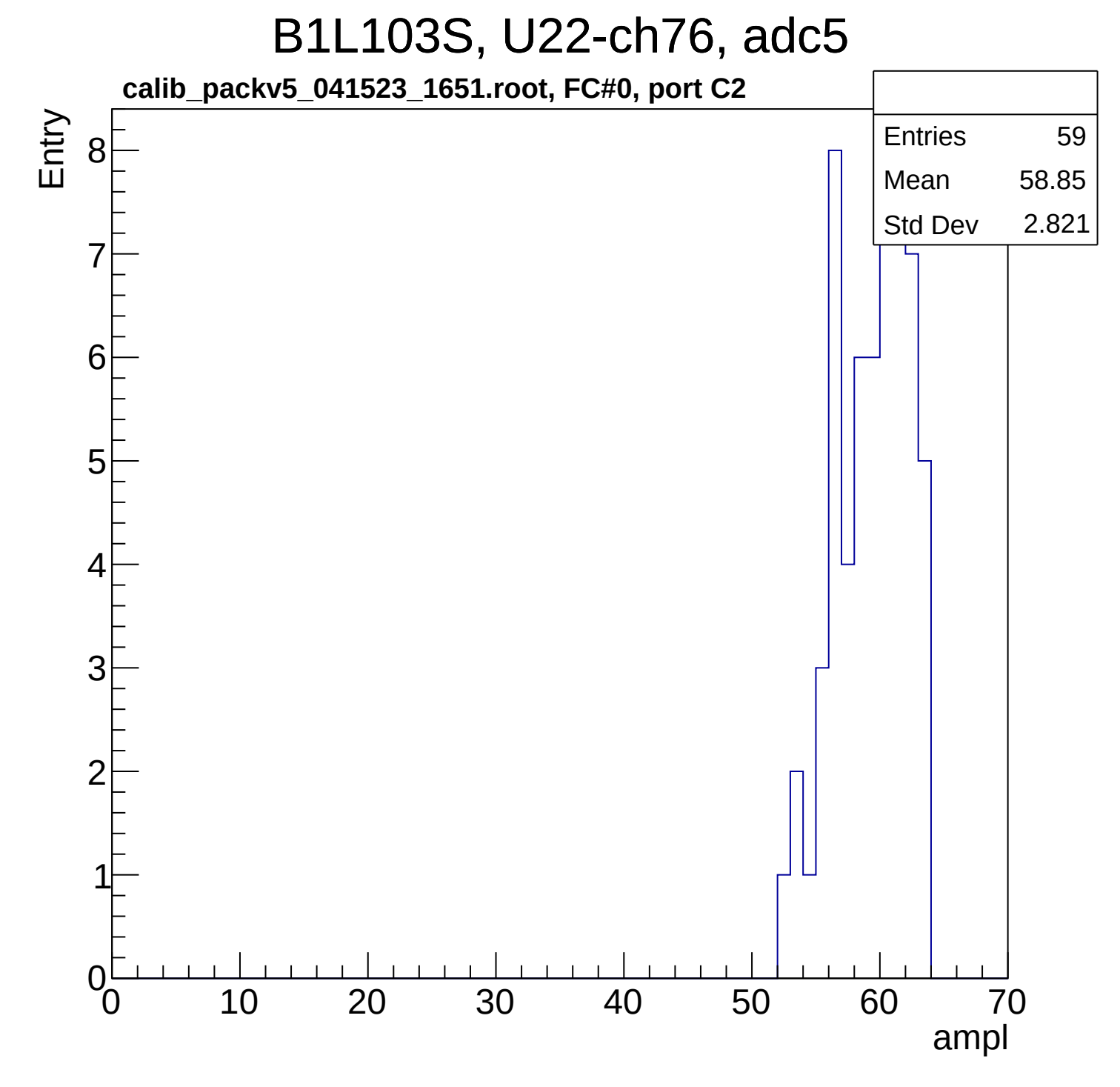
B1L103S, U22-ch76, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 58.85
Std Dev 2.821
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
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60
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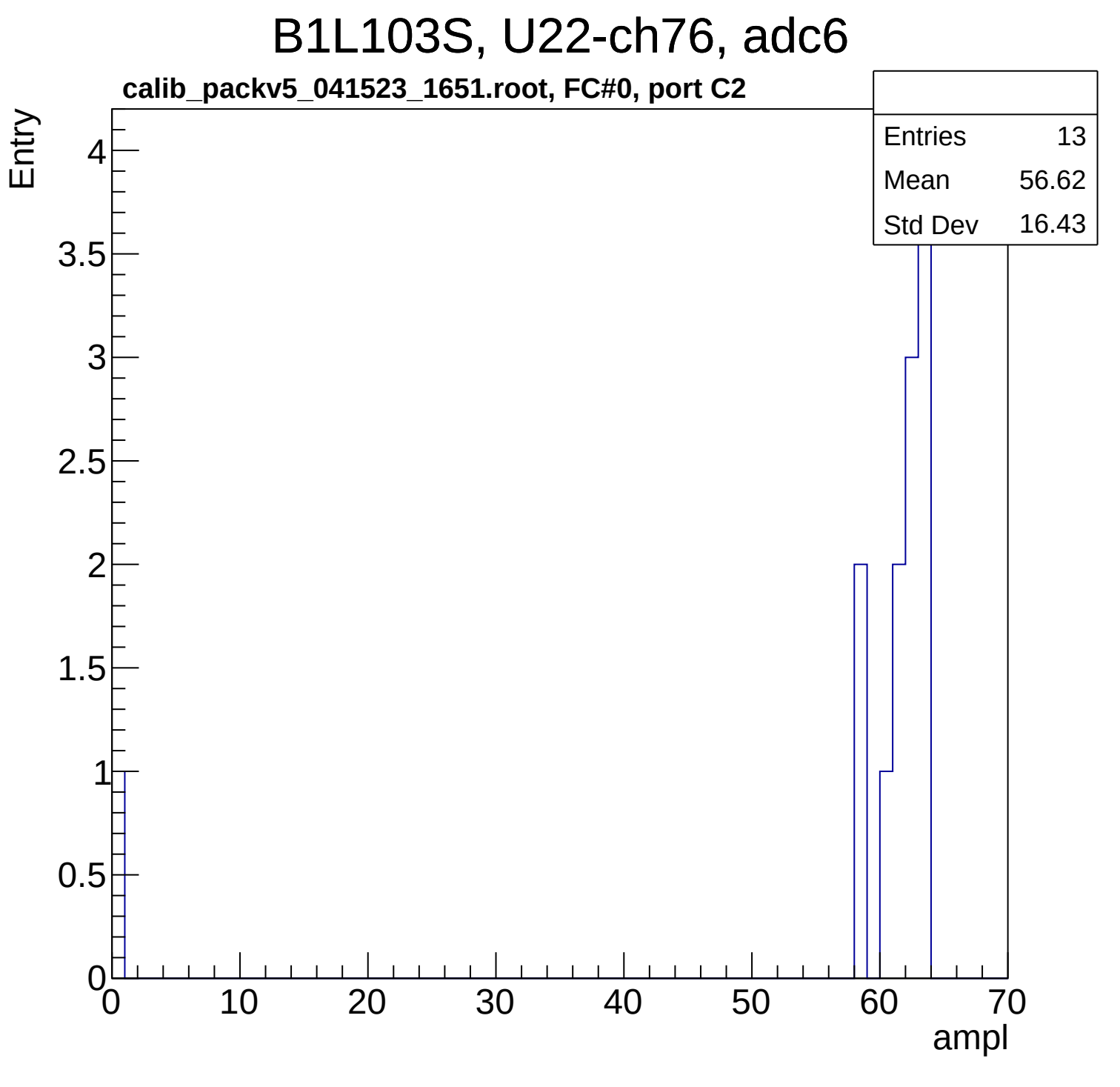
B1L103S, U22-ch76, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 56.62
Std Dev 16.43
Entry
ampl
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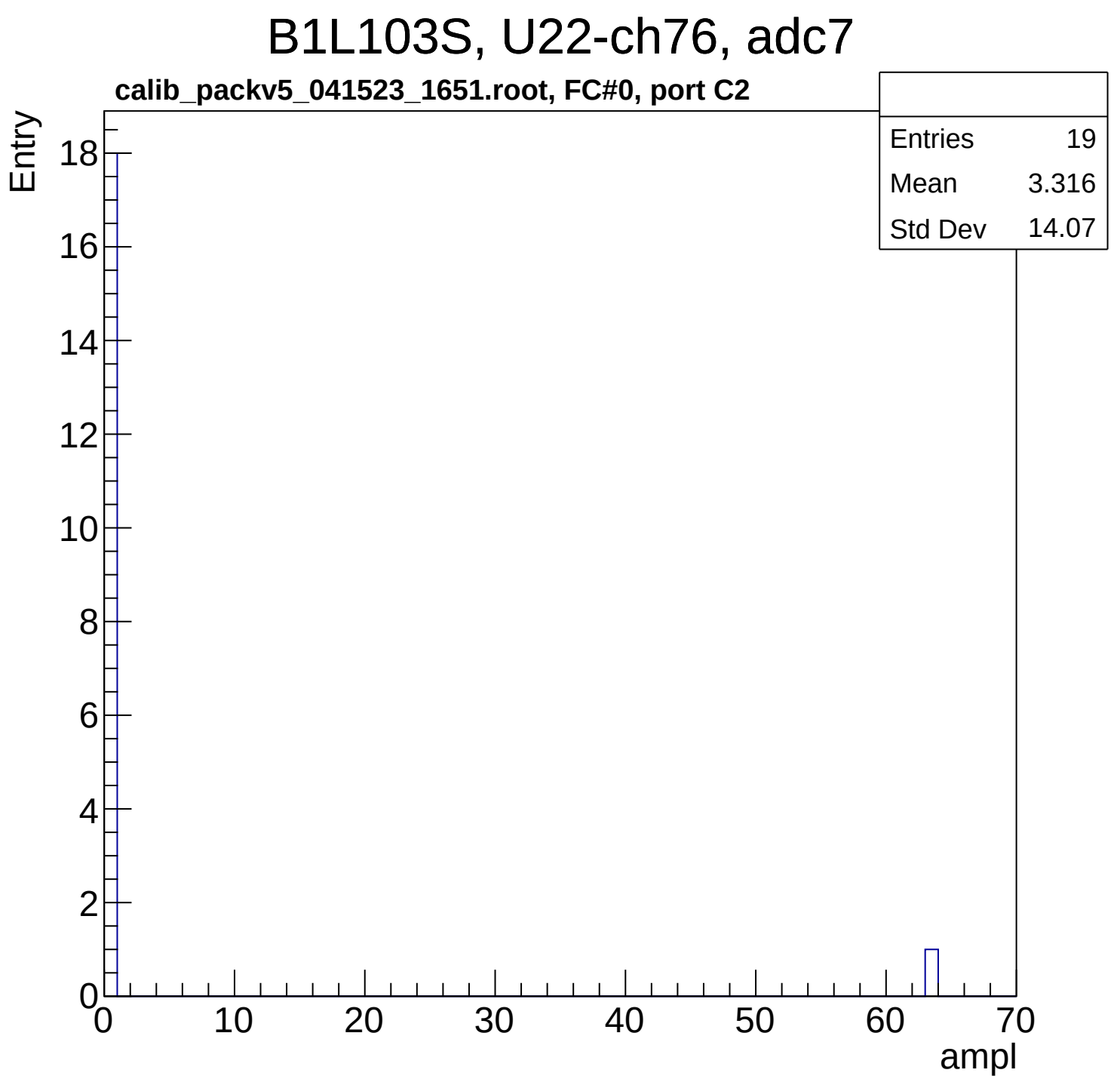
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U22-ch76, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.316
Std Dev 14.07
Entry
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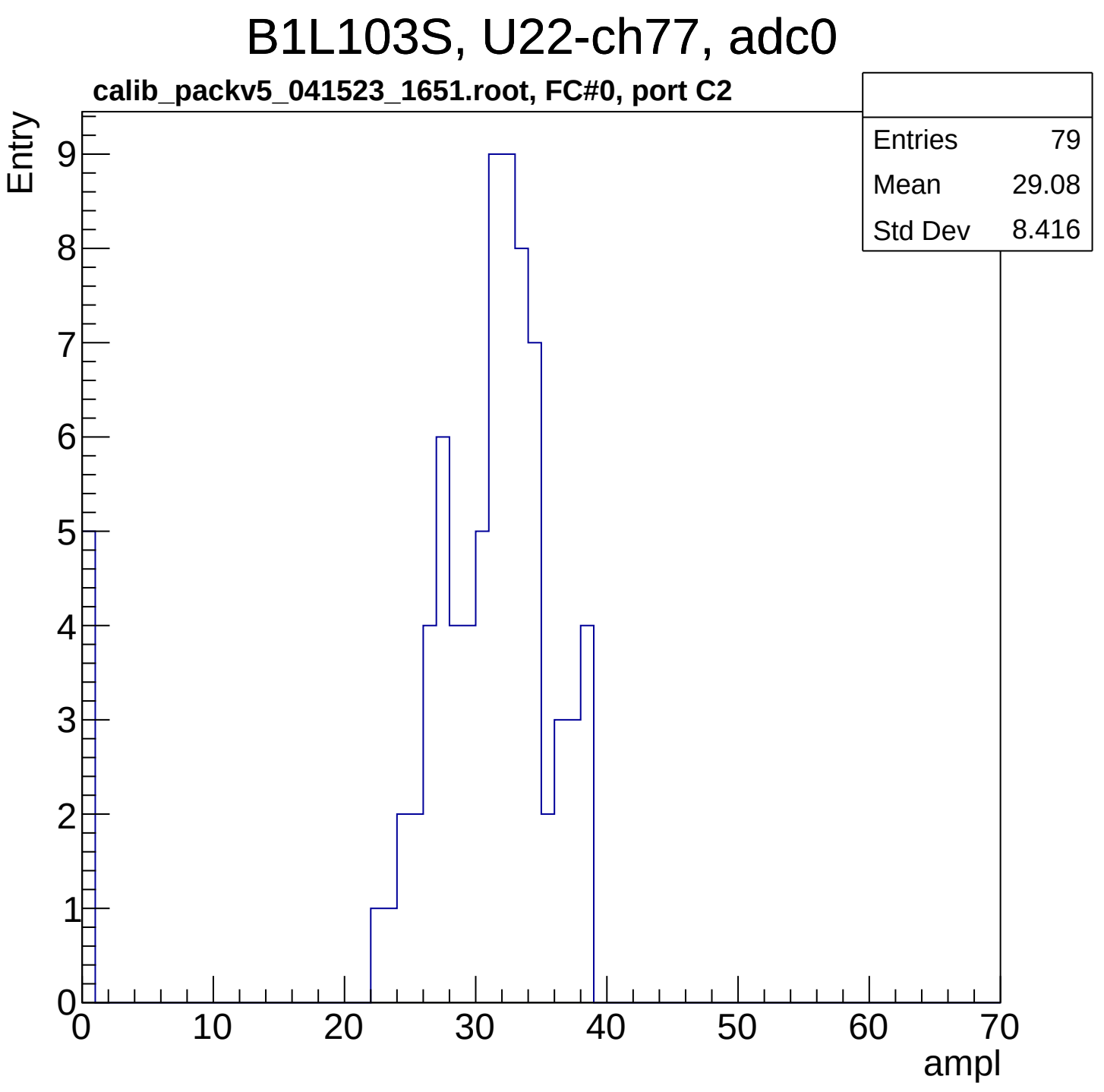
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch77, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 29.08
Std Dev 8.416
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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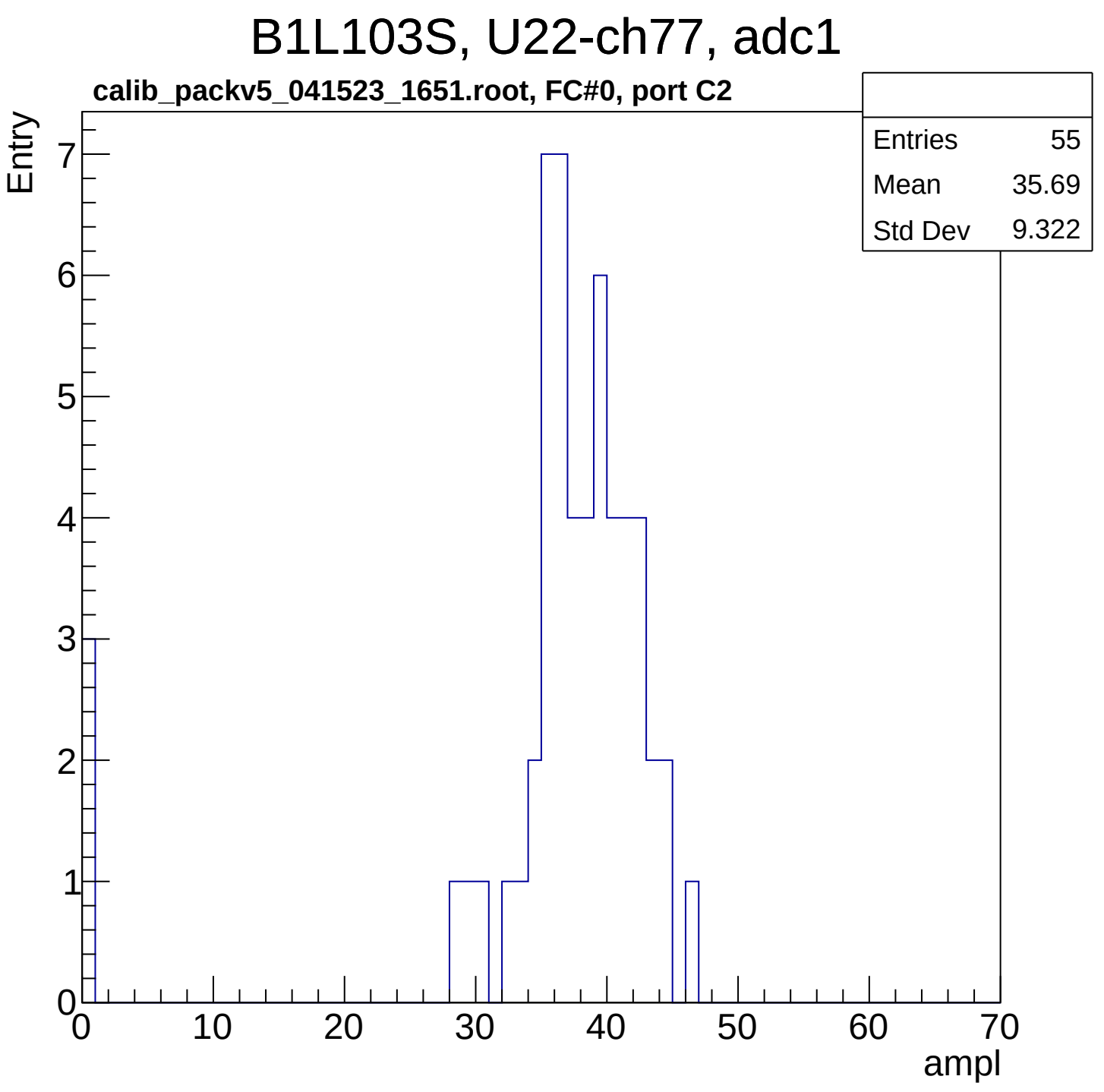
B1L103S, U22-ch77, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 35.69
Std Dev 9.322
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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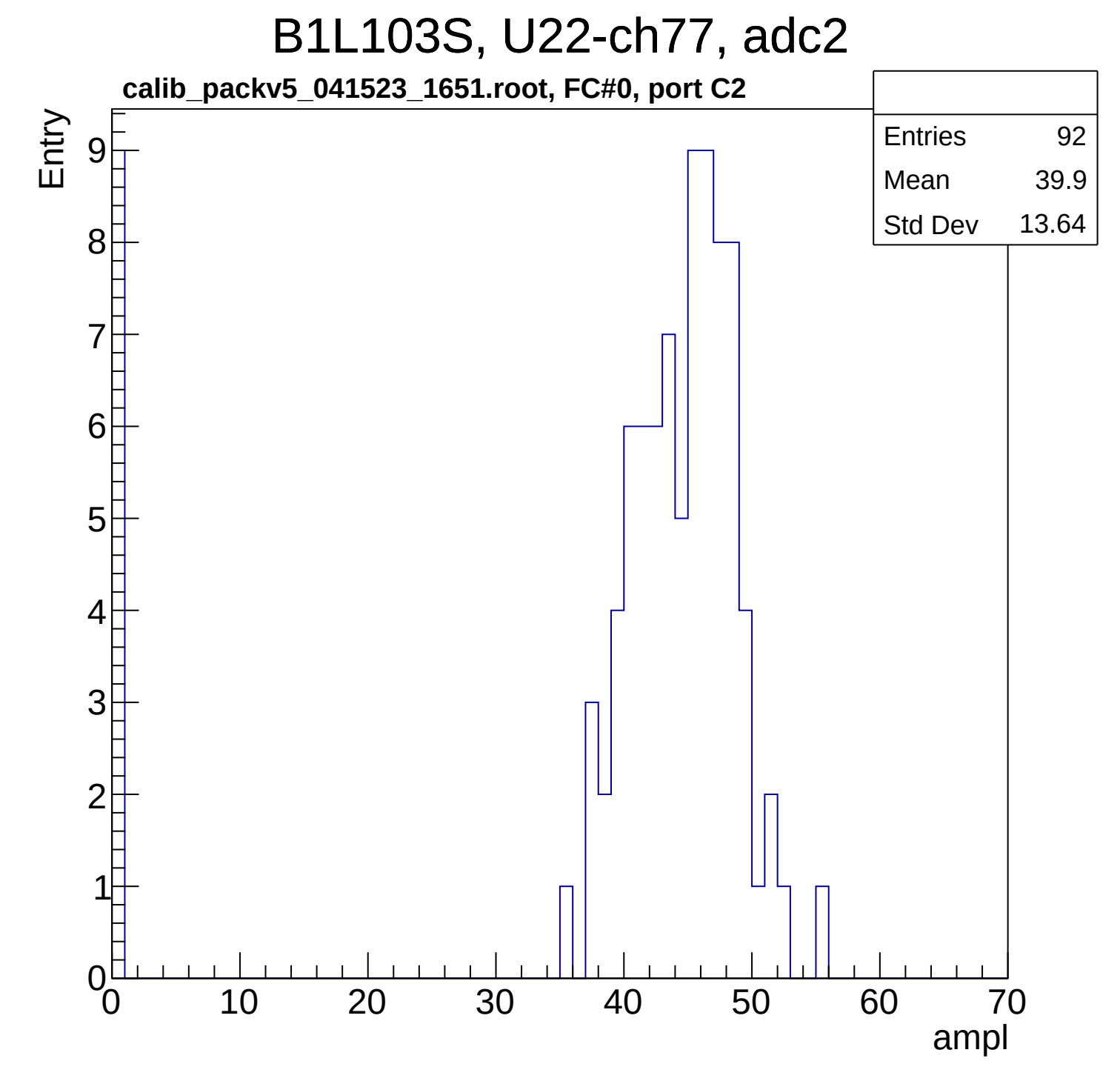
B1L103S, U22-ch77, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 39.9
Std Dev 13.64
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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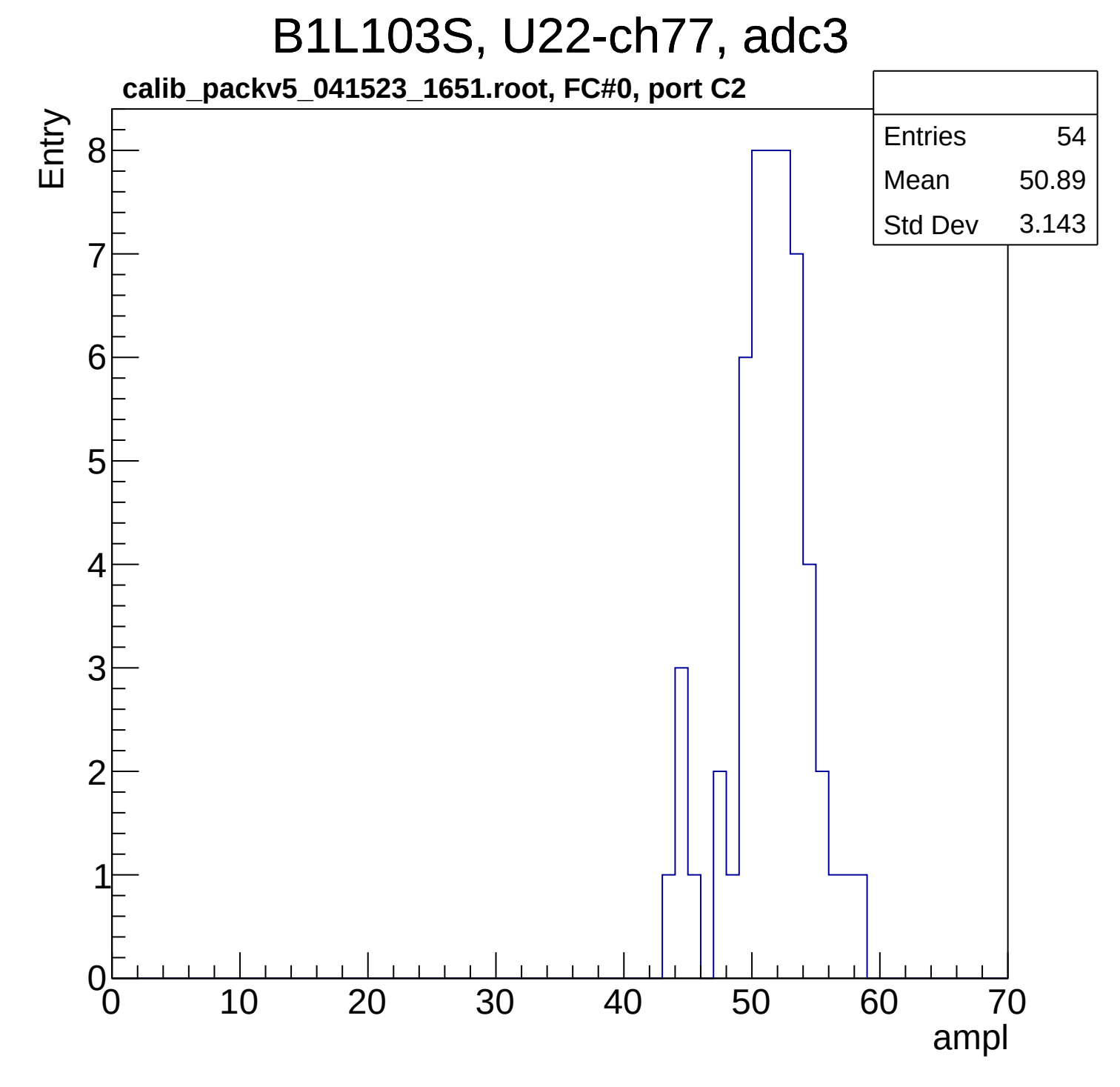
B1L103S, U22-ch77, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 50.89
Std Dev 3.143
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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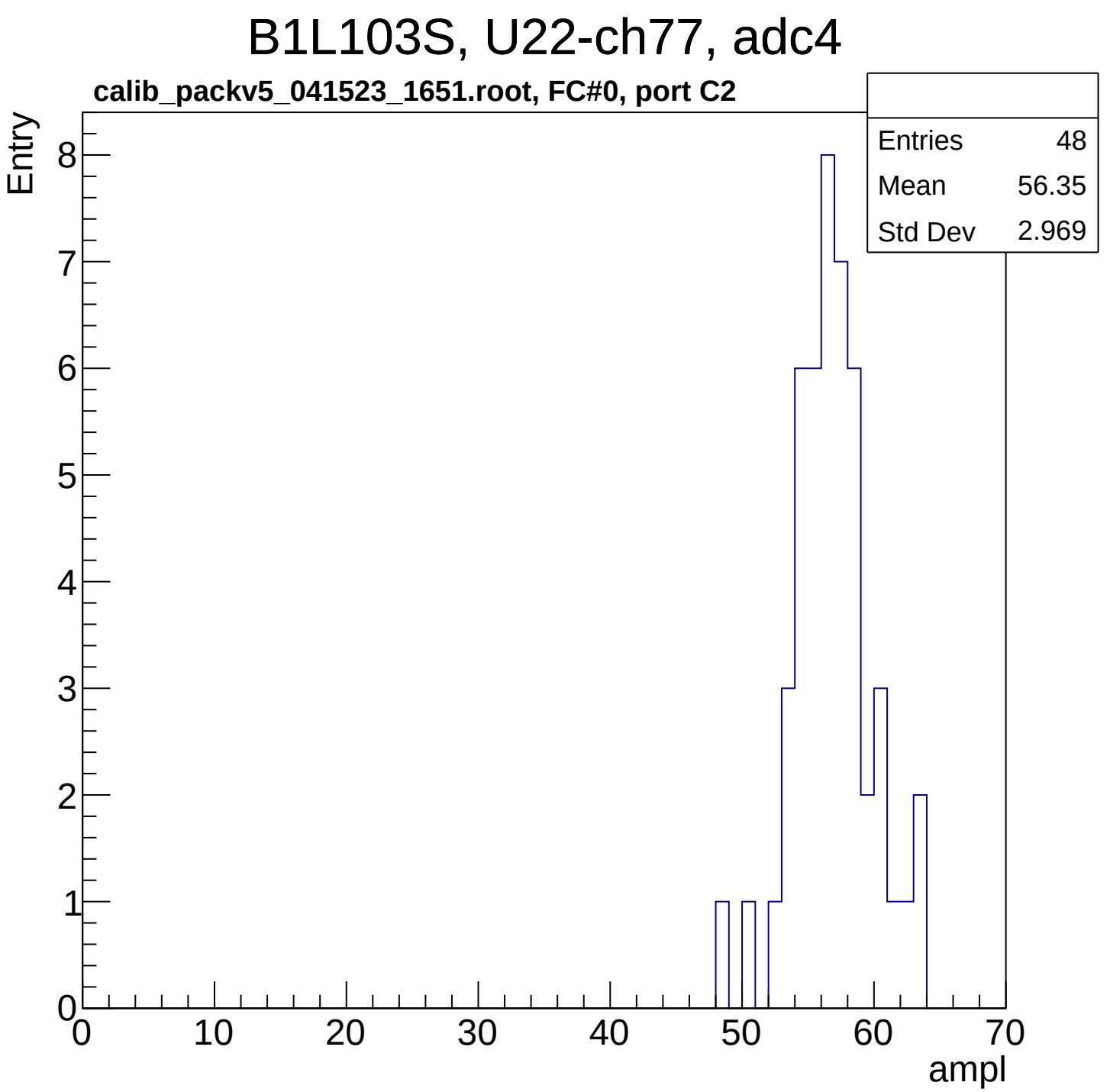
B1L103S, U22-ch77, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 56.35
Std Dev 2.969
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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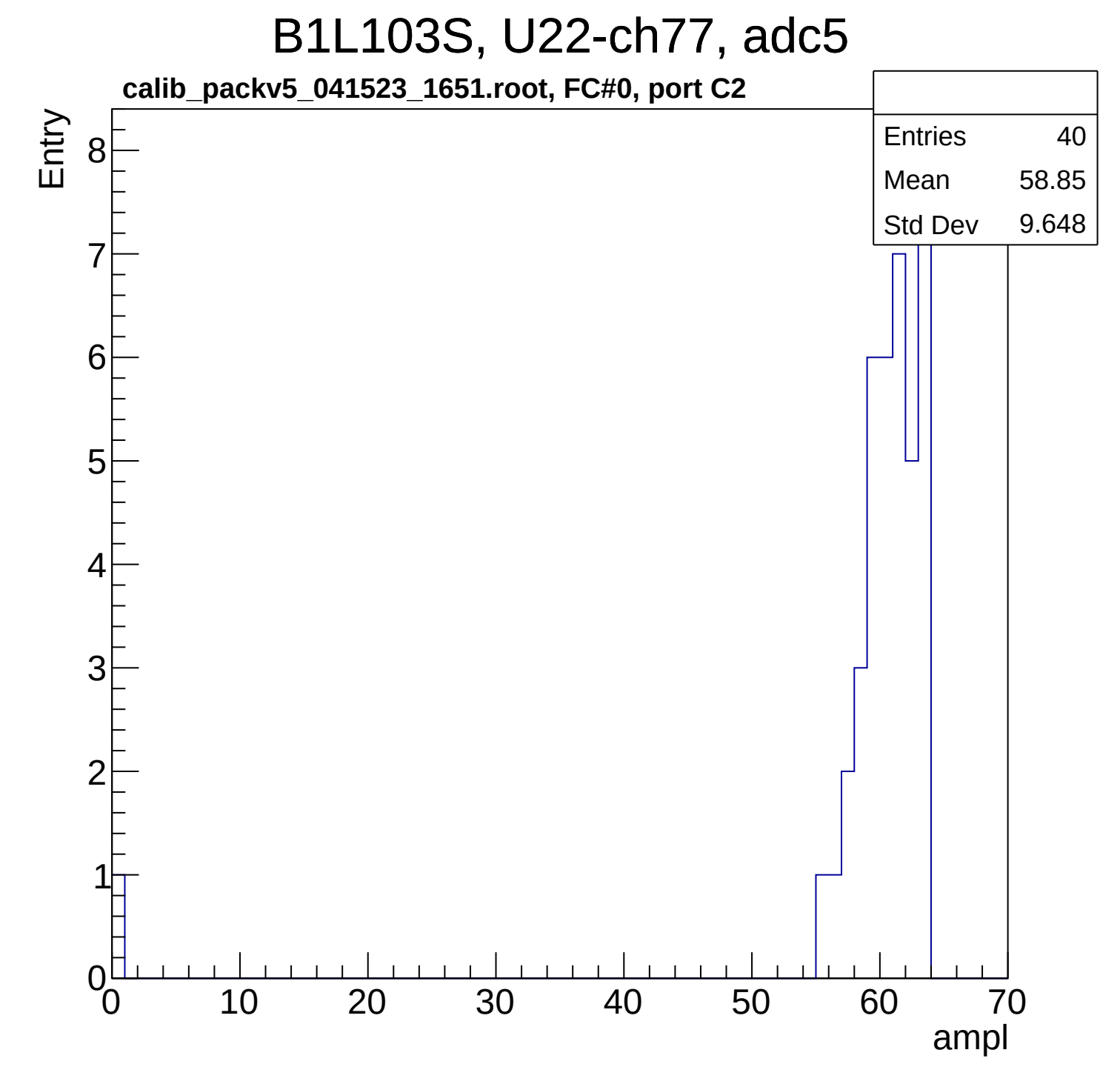
B1L103S, U22-ch77, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 58.85
Std Dev 9.648
Entry
ampl
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2
3
4
5
6
7
8
0
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20
30
40
50
60
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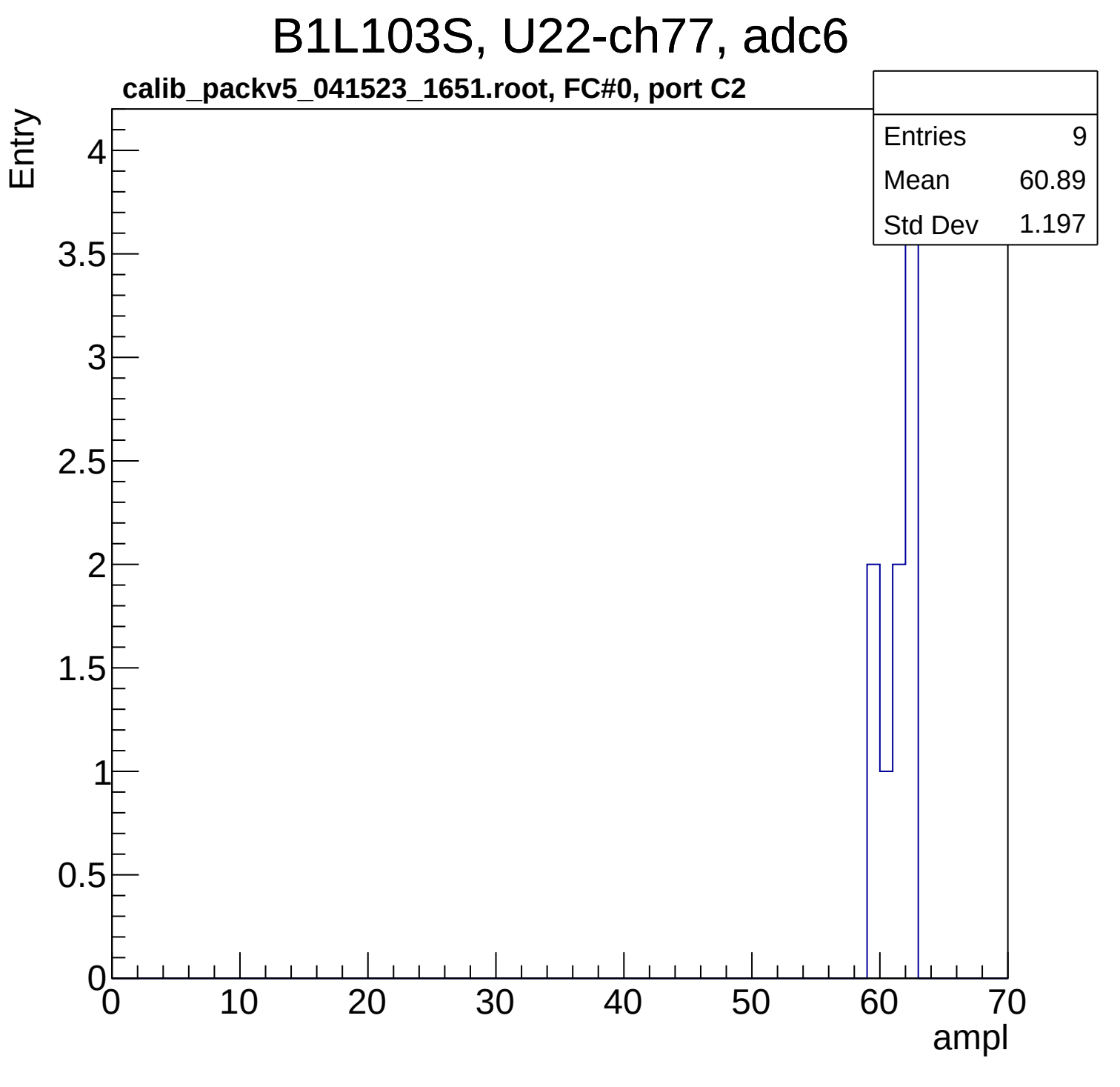
B1L103S, U22-ch77, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 60.89
Std Dev 1.197
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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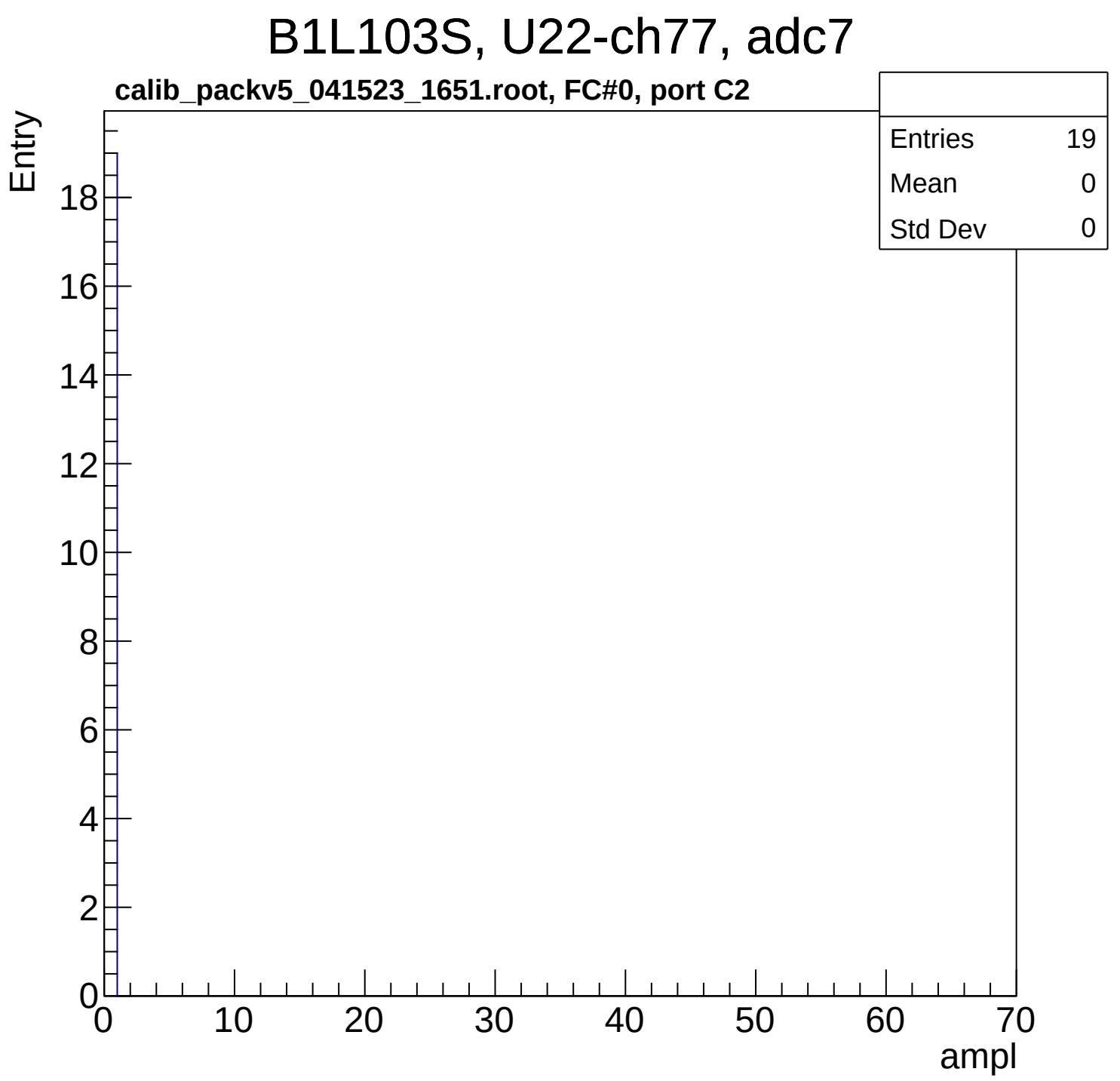
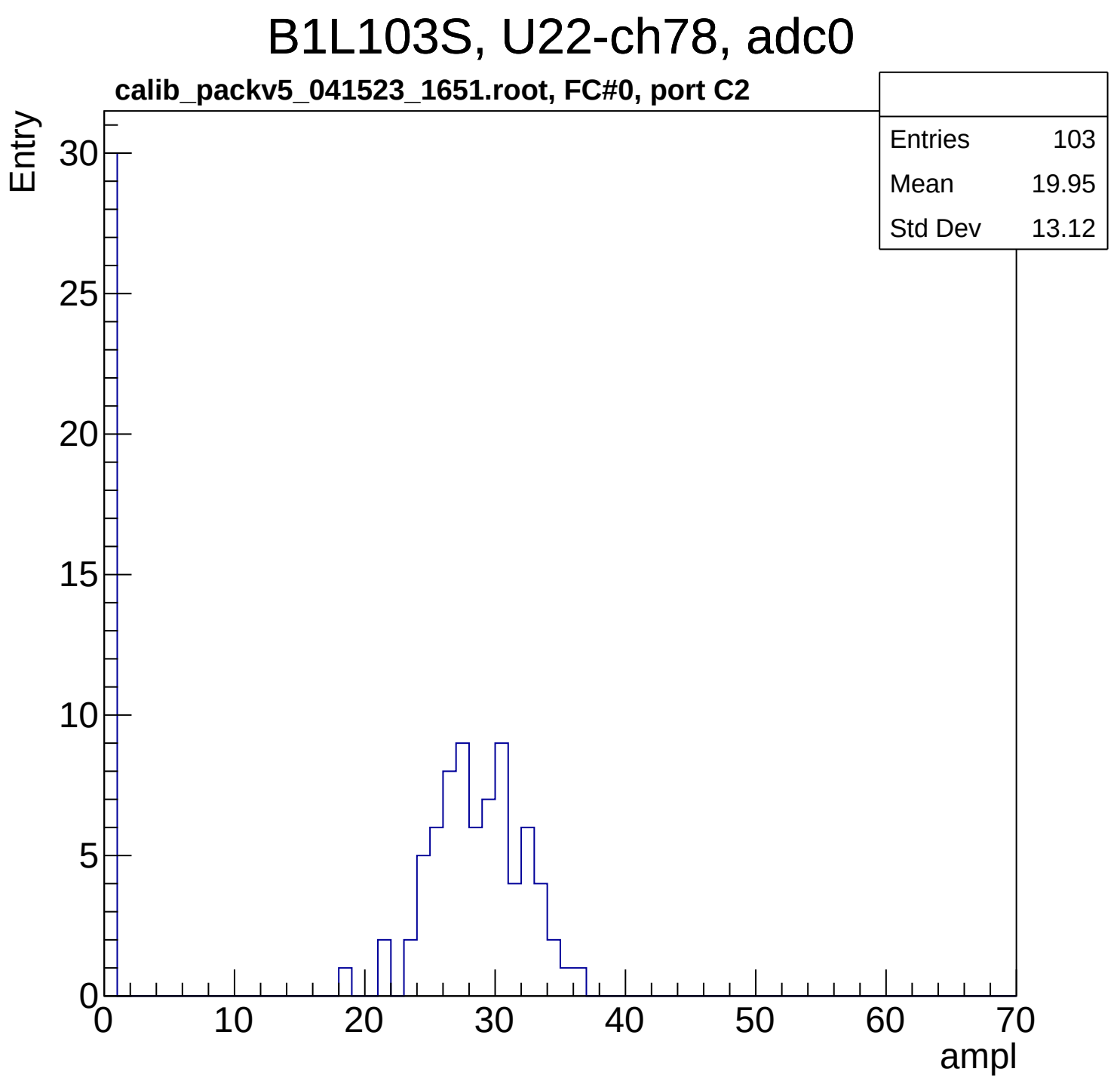
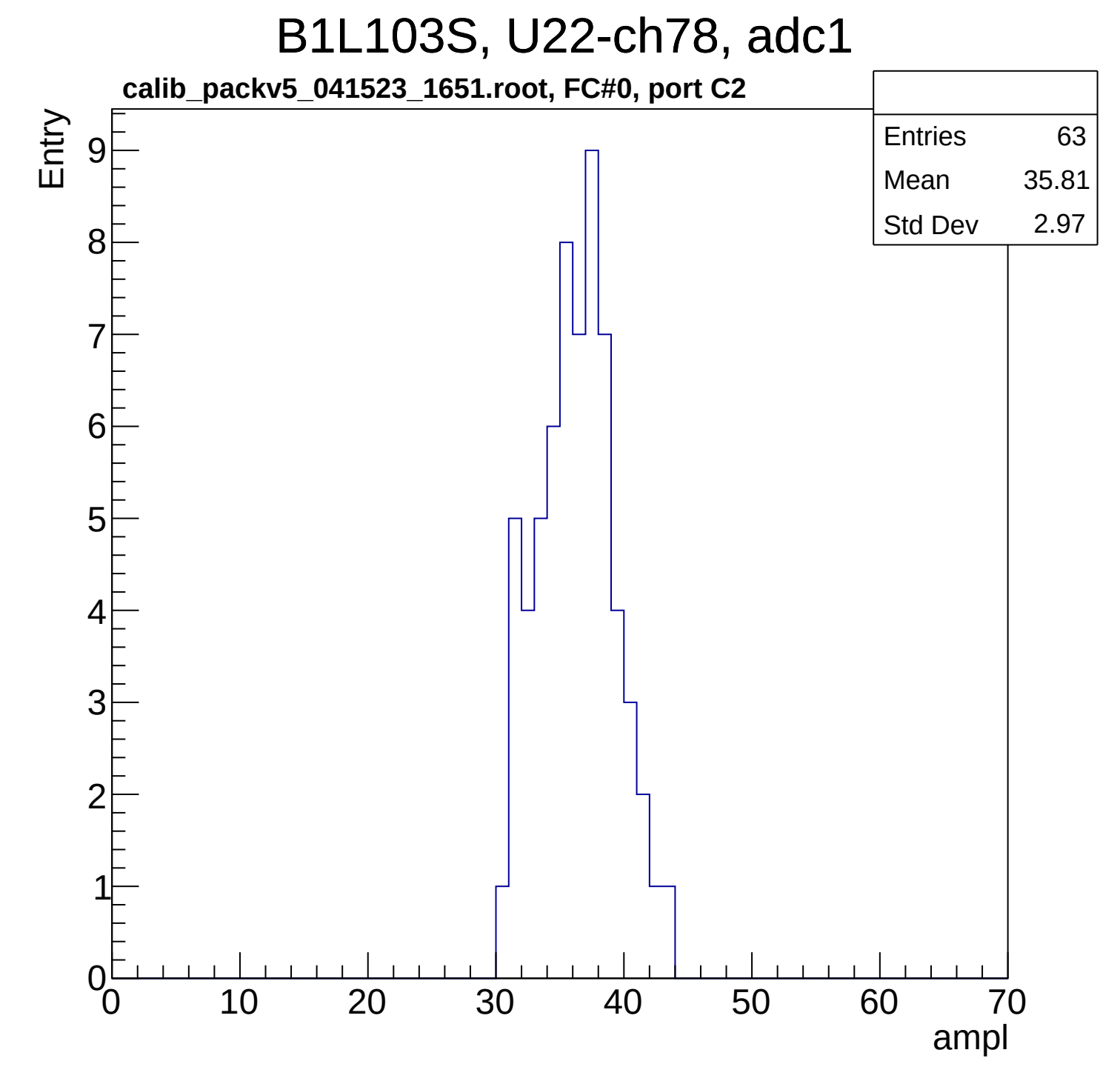

B1L103S, U22-ch77, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch78, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 103
Mean 19.95
Std Dev 13.12
Entry
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch78, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 35.81
Std Dev 2.97
Entry
ampl
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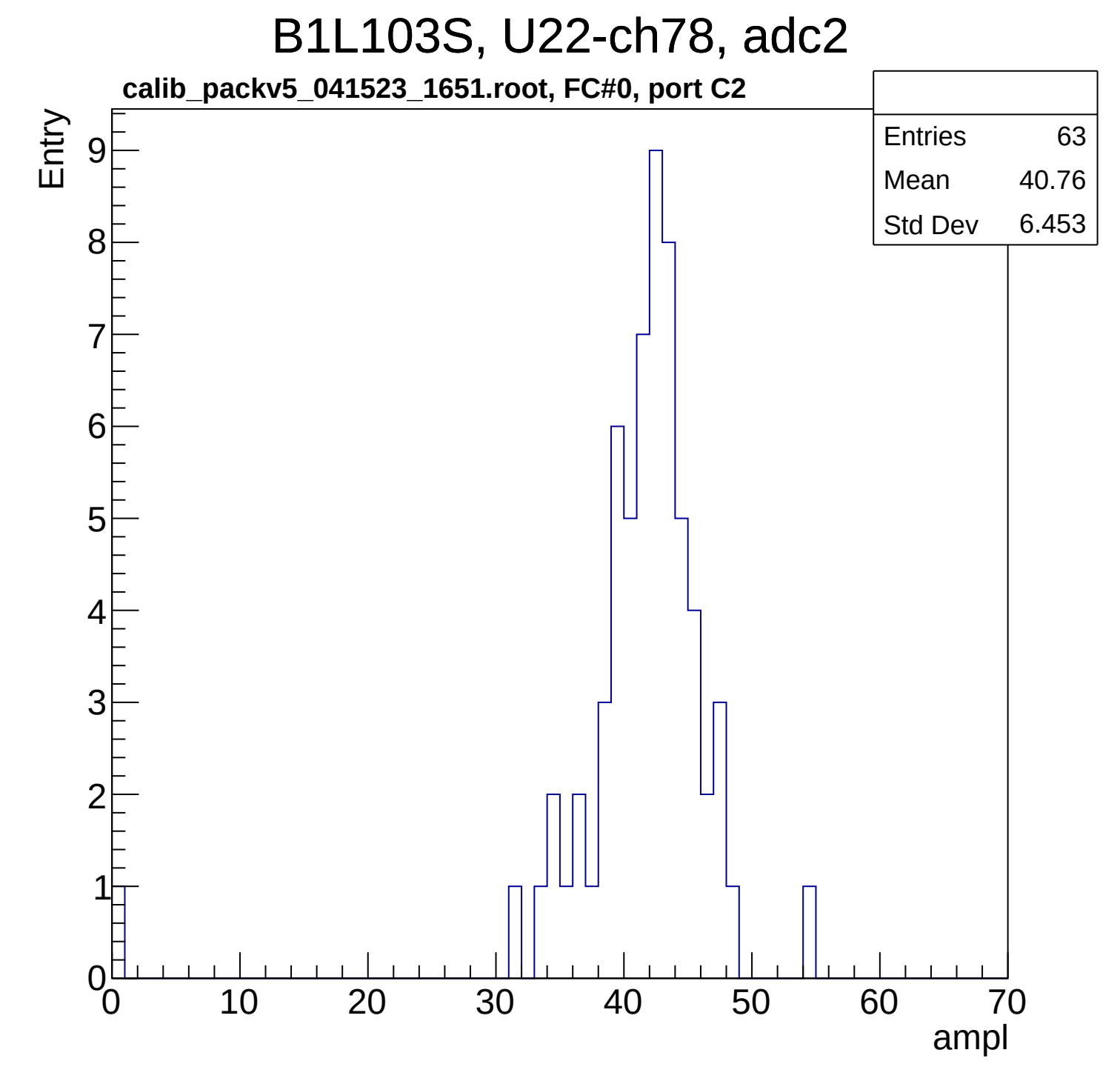
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch78, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 40.76
Std Dev 6.453
Entry
ampl
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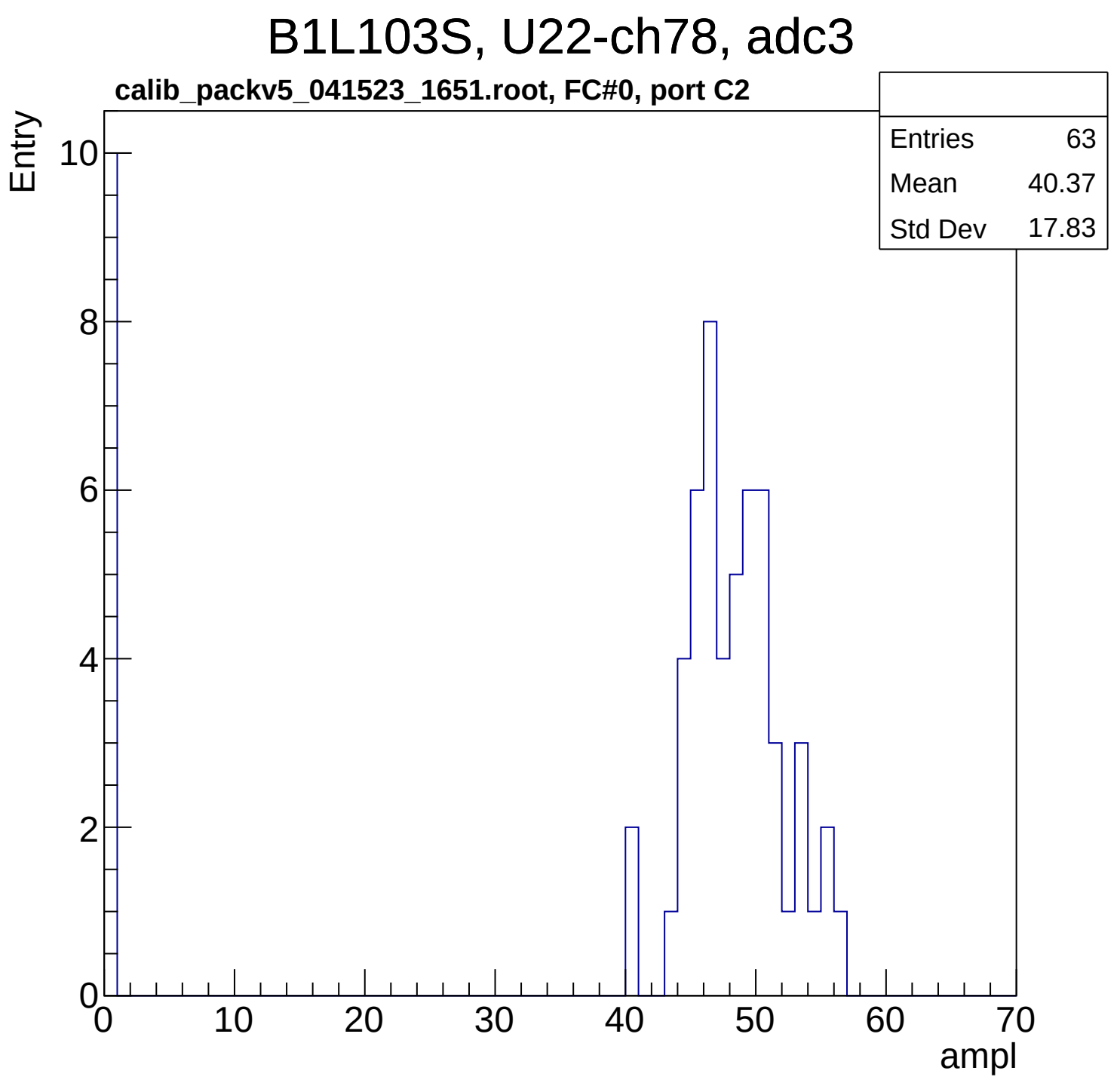
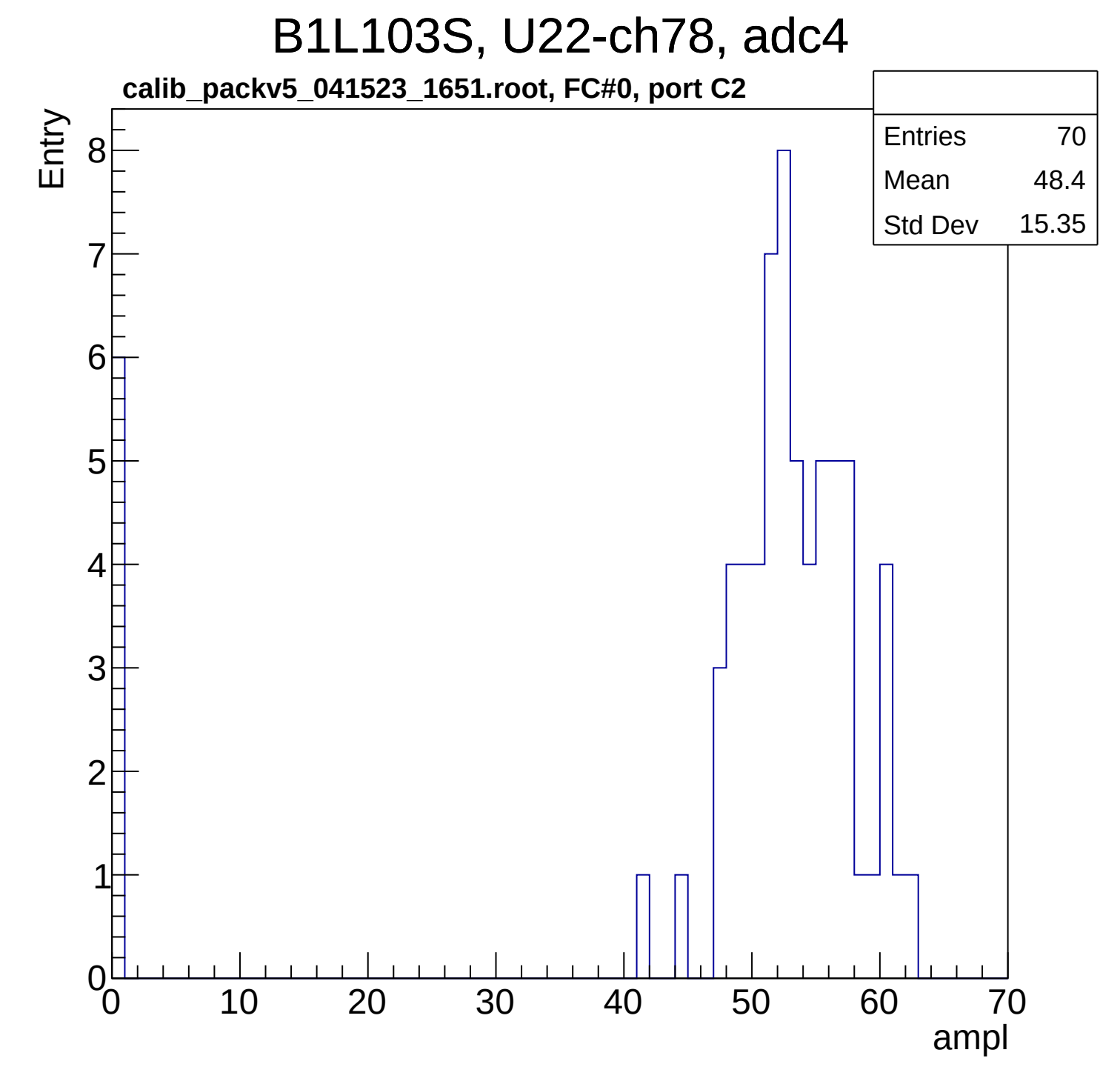
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch78, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 40.37
Std Dev 17.83
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch78, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 48.4
Std Dev 15.35
Entry
ampl
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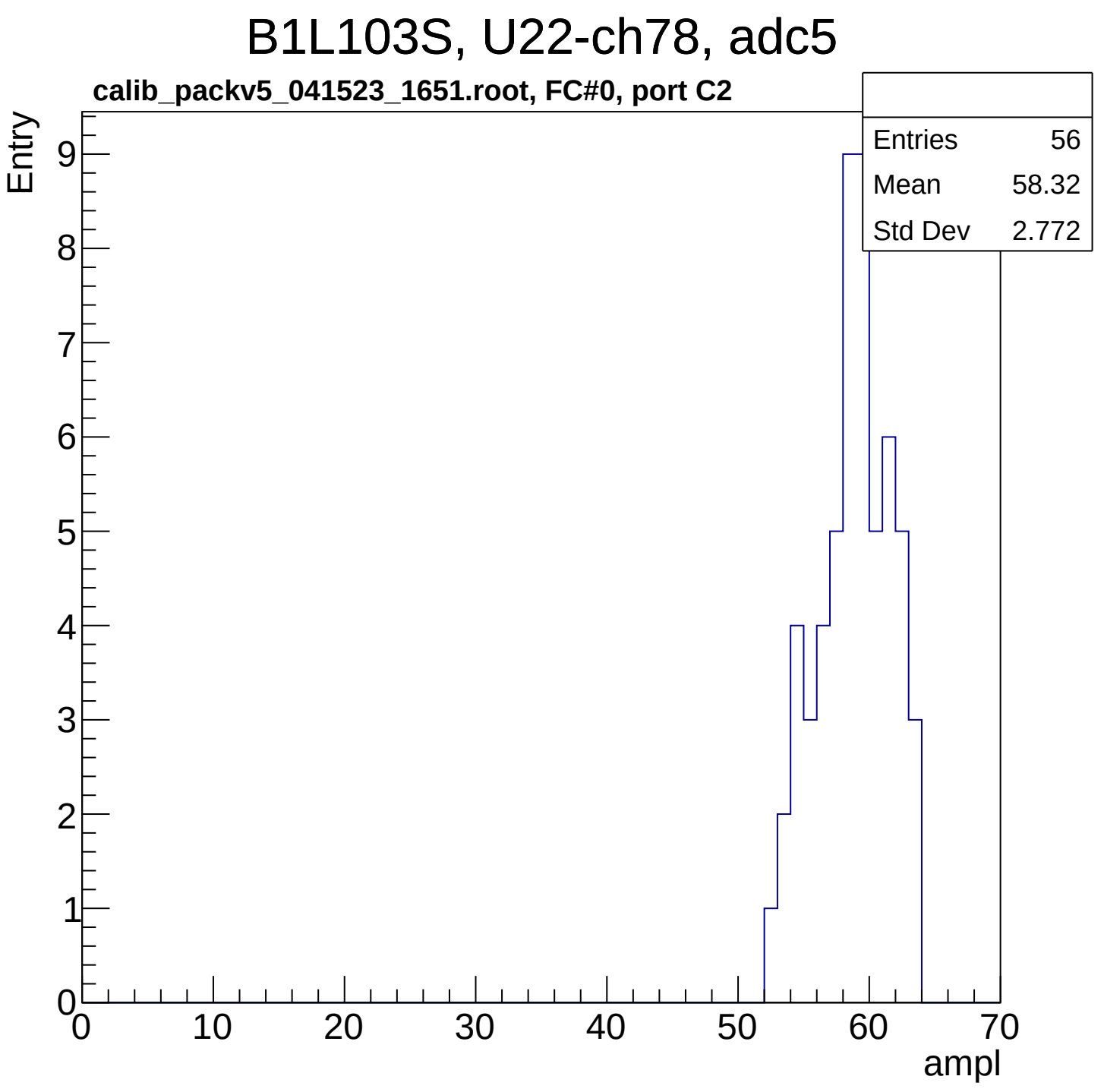
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch78, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 58.32
Std Dev 2.772
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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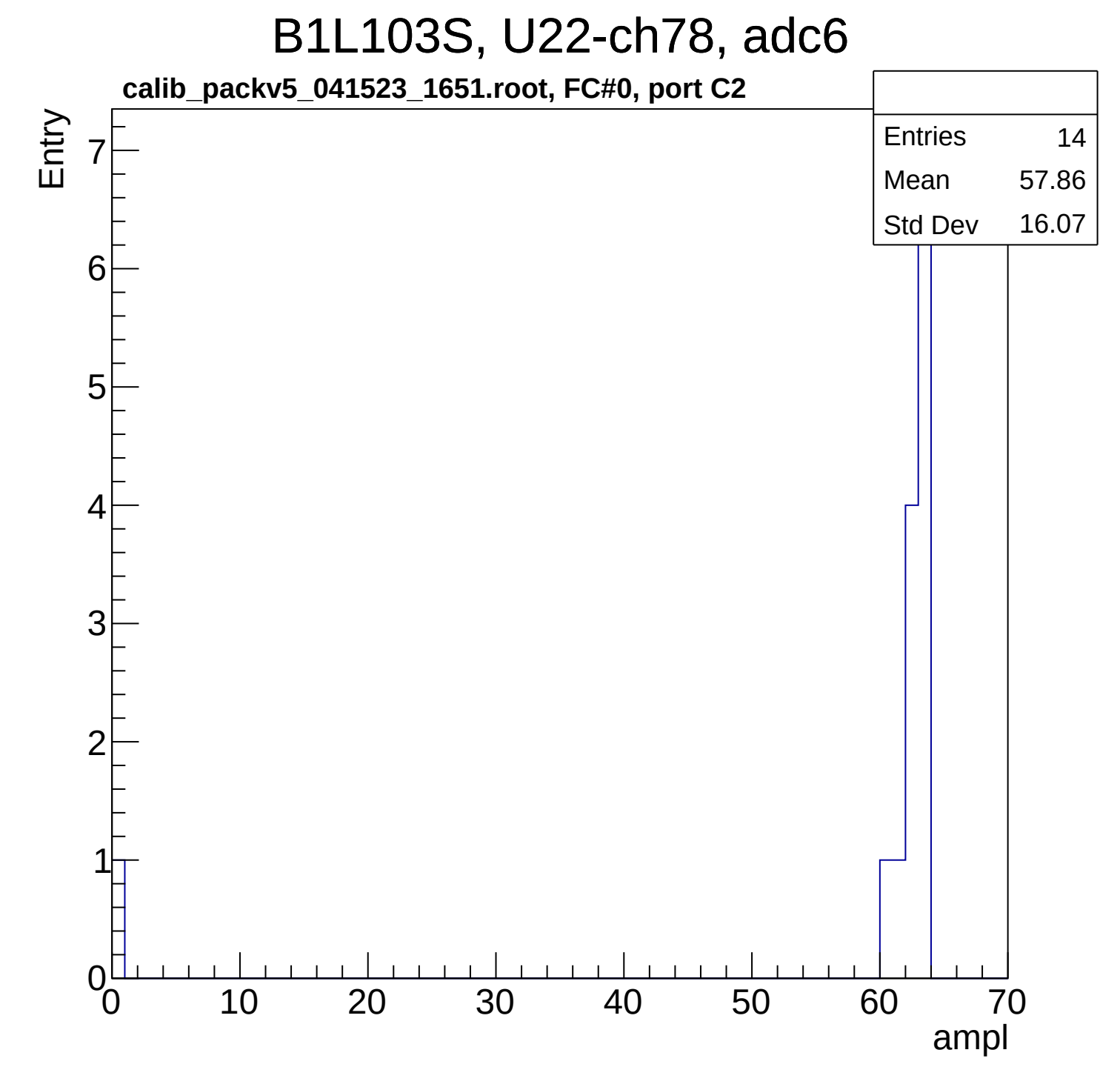
B1L103S, U22-ch78, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 57.86
Std Dev 16.07
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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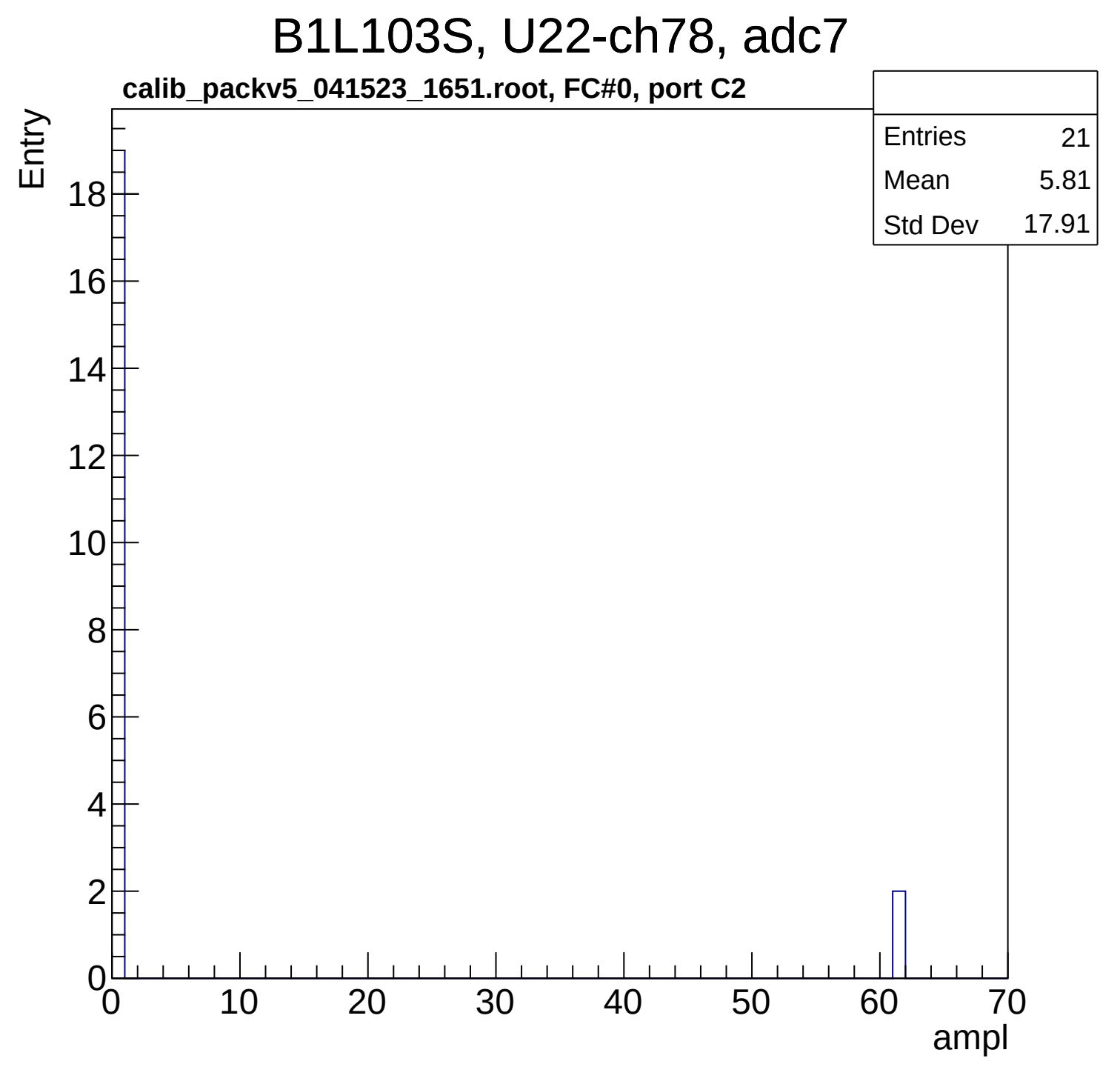
B1L103S, U22-ch78, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.81
Std Dev 17.91
Entry
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2
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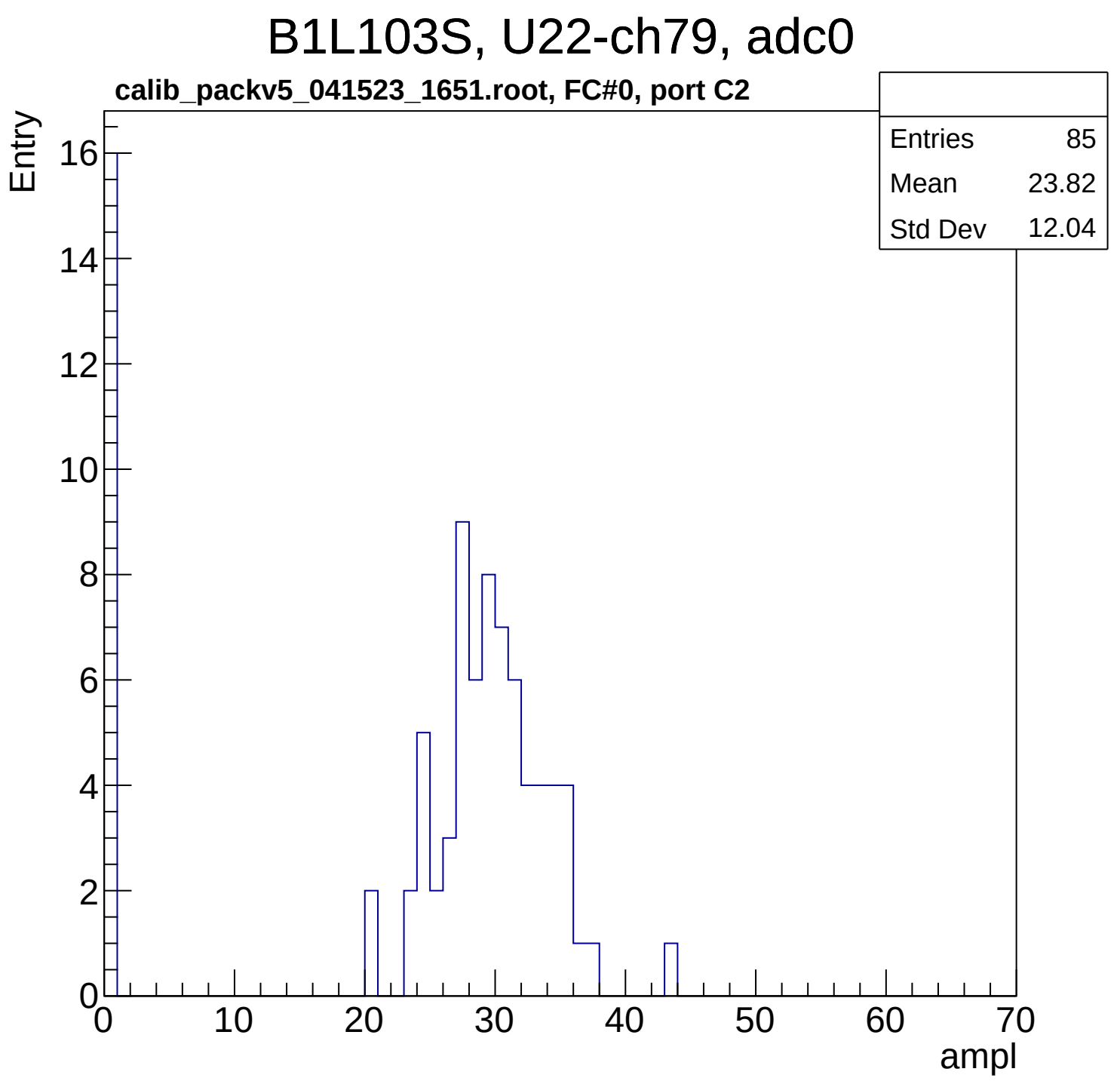
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch79, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 23.82
Std Dev 12.04
Entry
ampl
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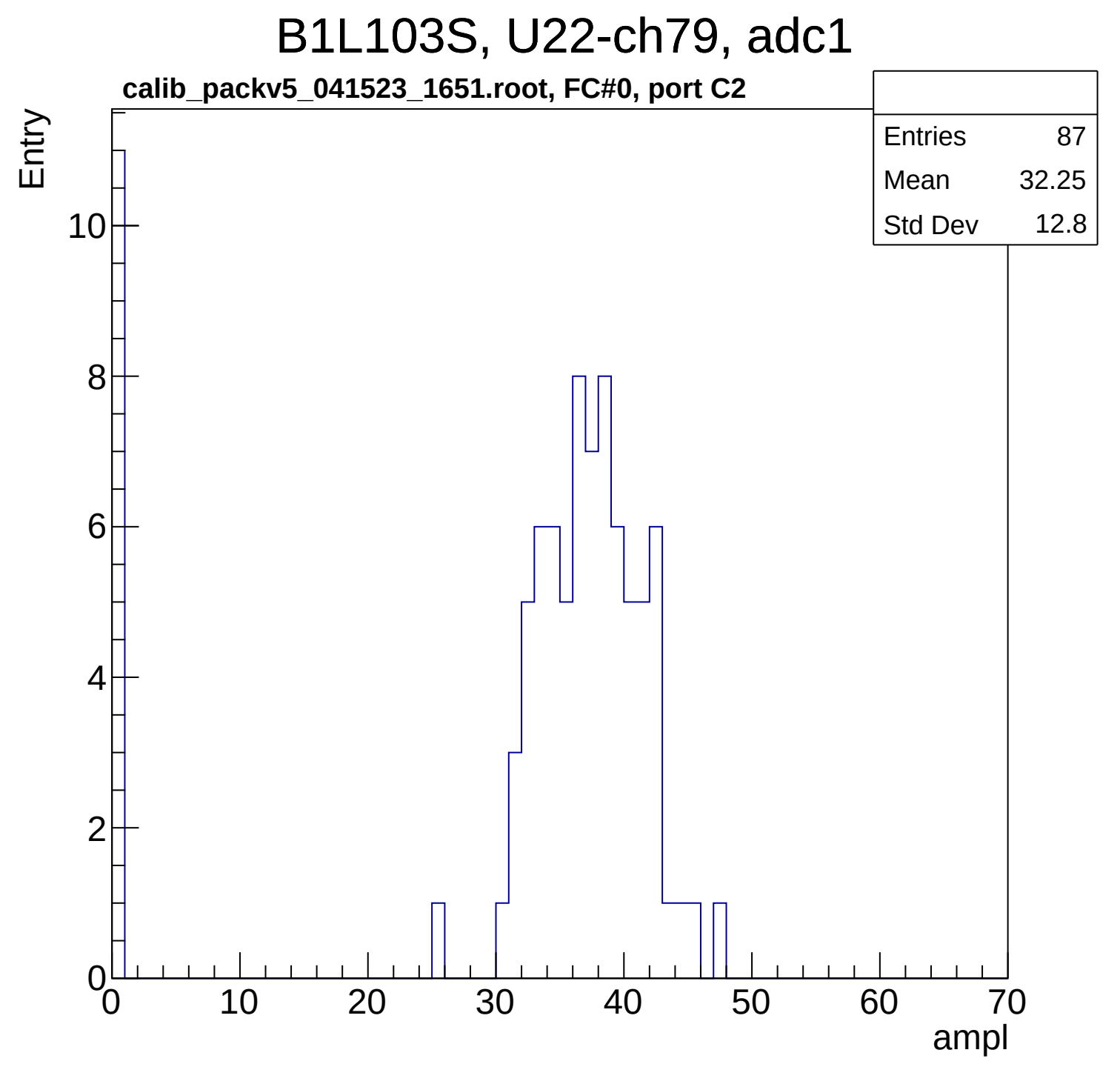
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L103S, U22-ch79, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 32.25
Std Dev 12.8
Entry
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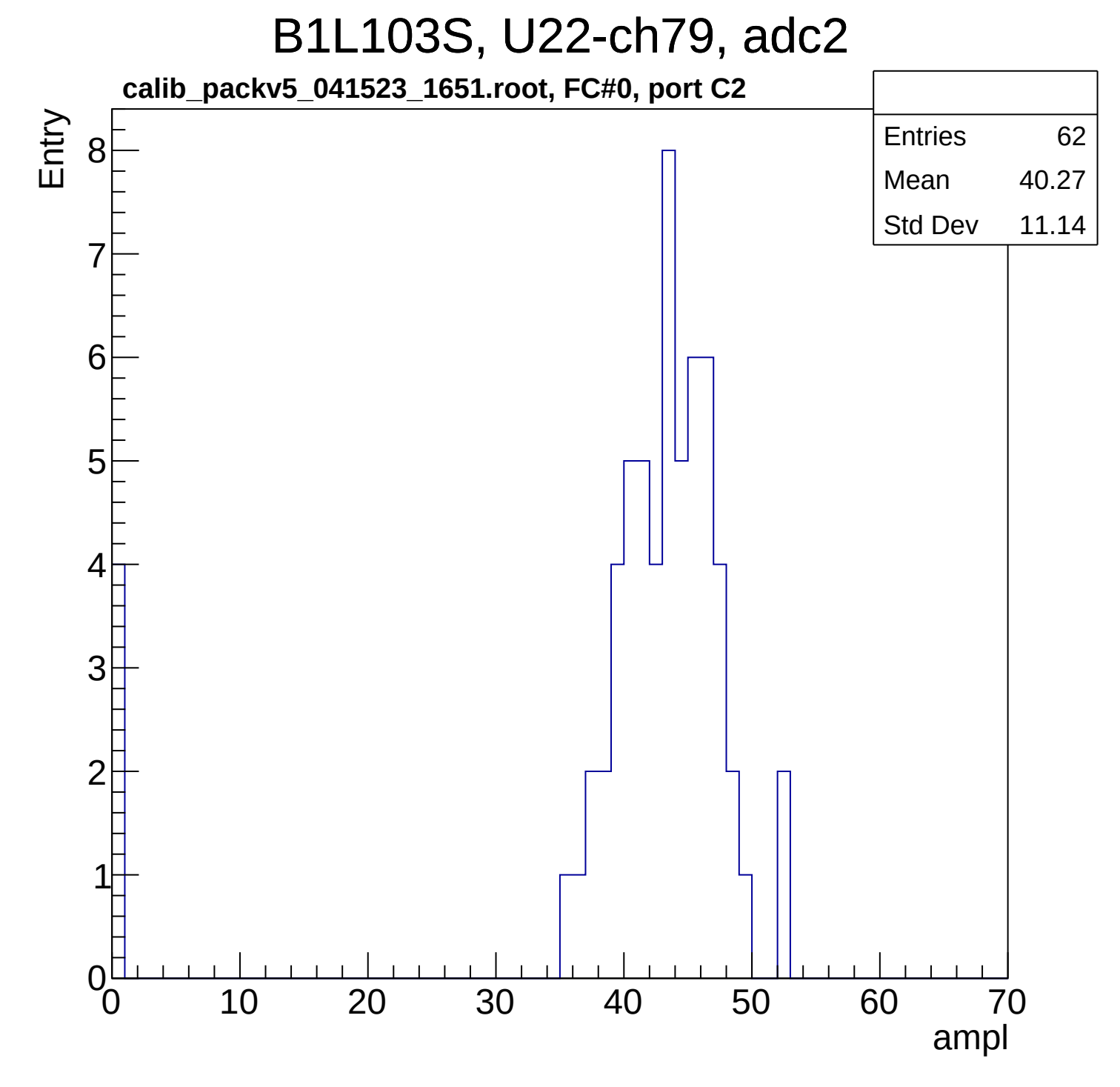
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch79, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 40.27
Std Dev 11.14
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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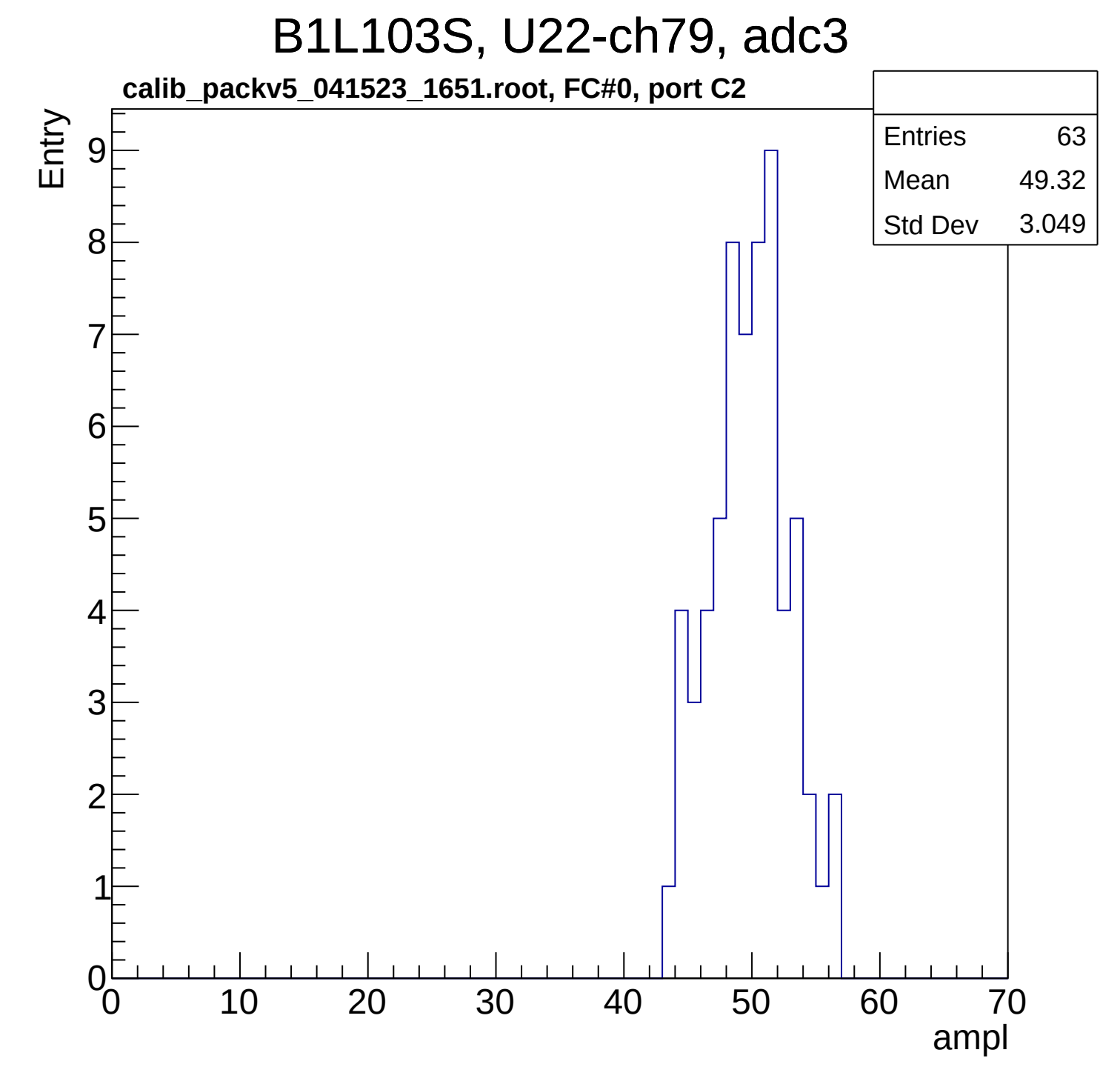
60
70


B1L103S, U22-ch79, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 49.32
Std Dev 3.049
Entry
ampl
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2
3
4
5
6
7
8
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0
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40
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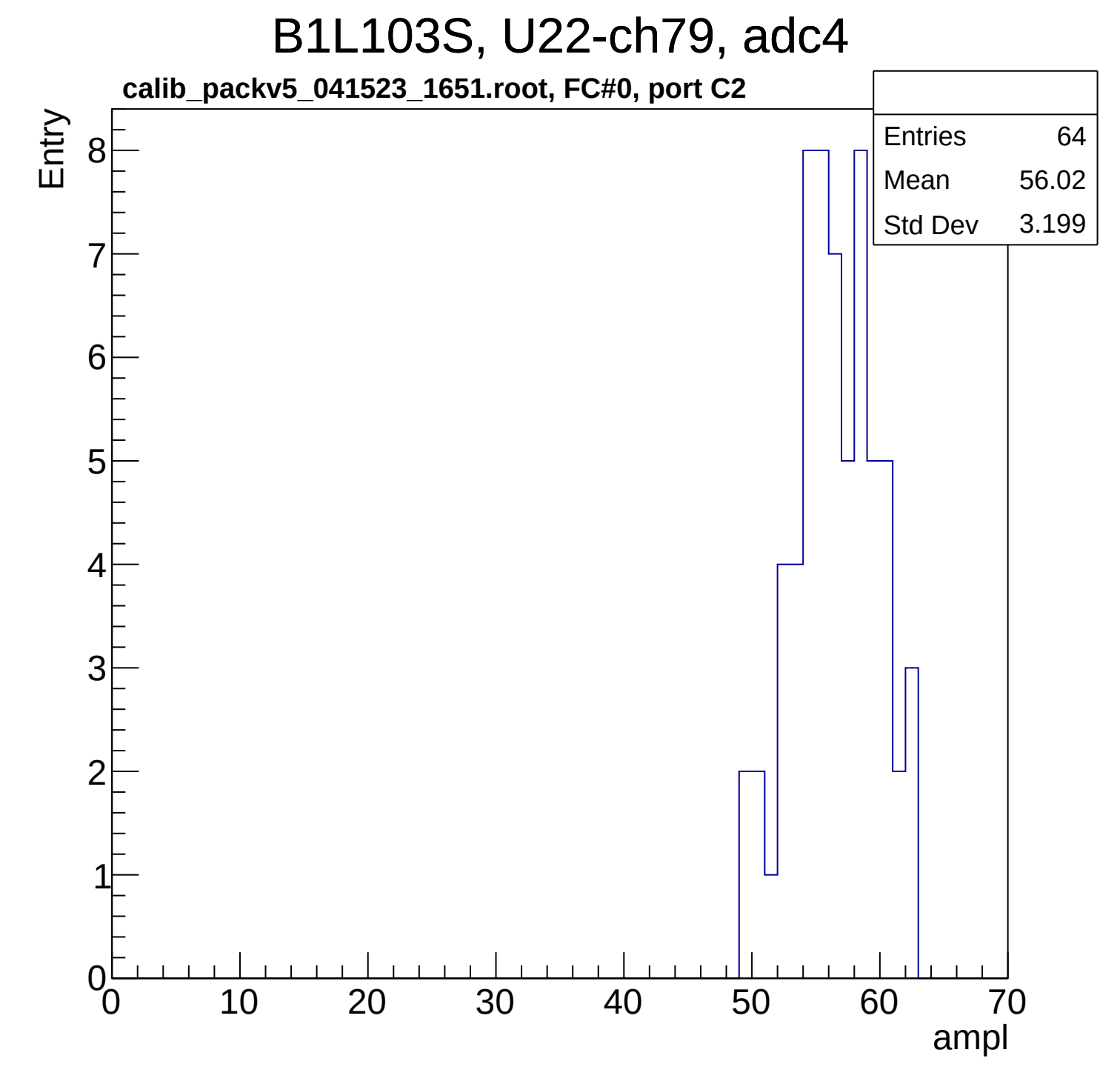
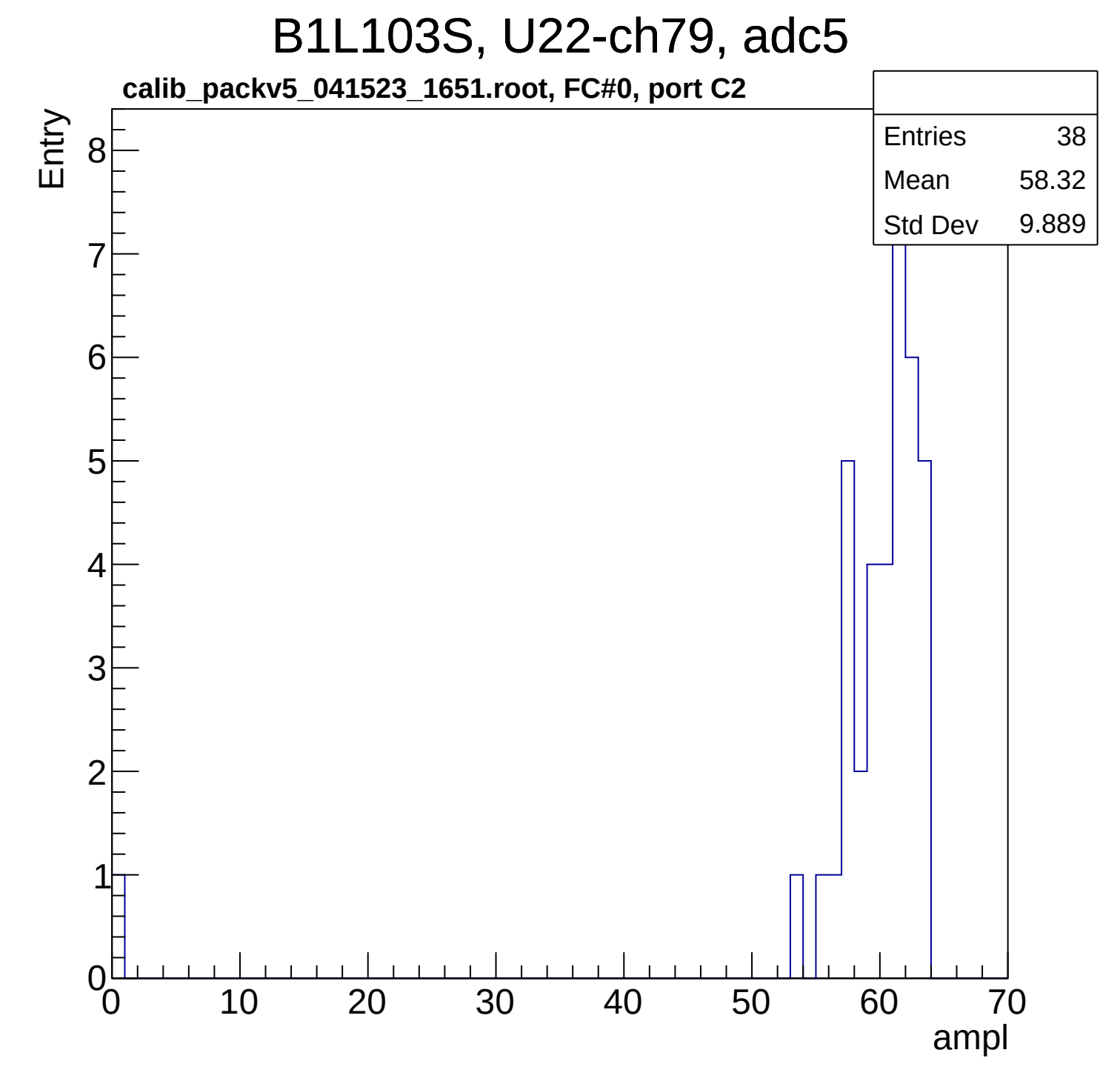
60
70


B1L103S, U22-ch79, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 56.02
Std Dev 3.199
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch79, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 58.32
Std Dev 9.889
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
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40
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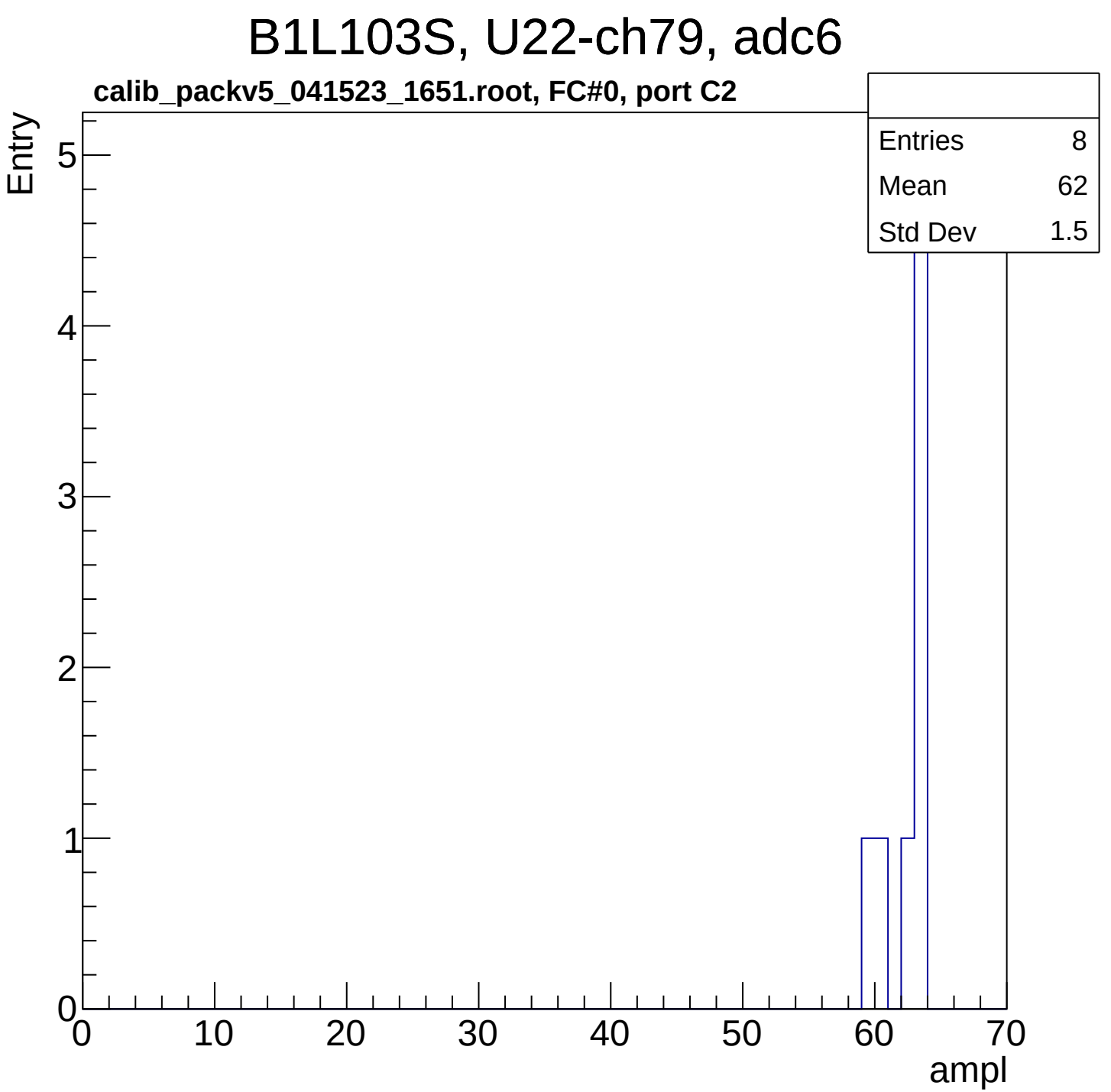
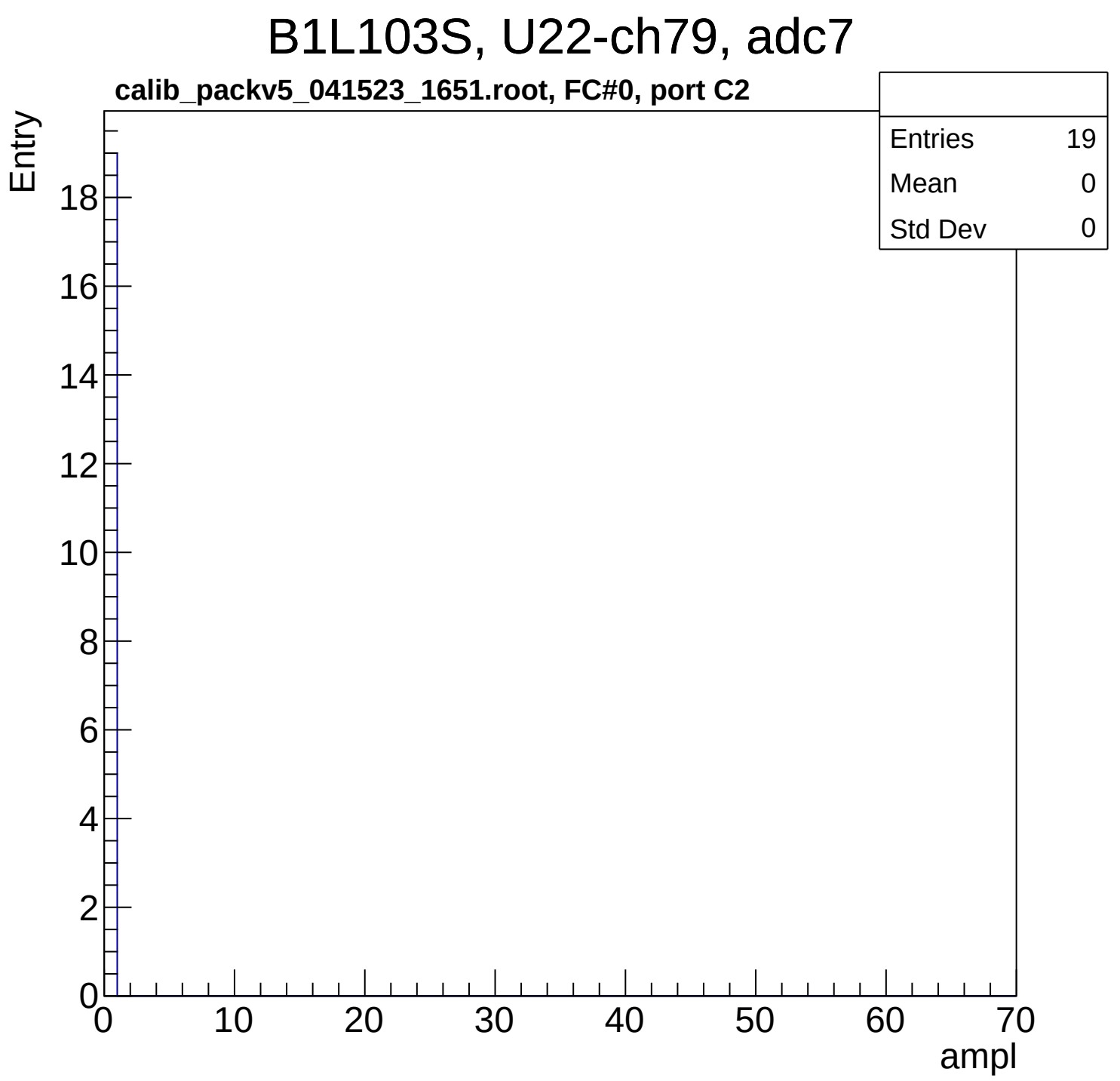
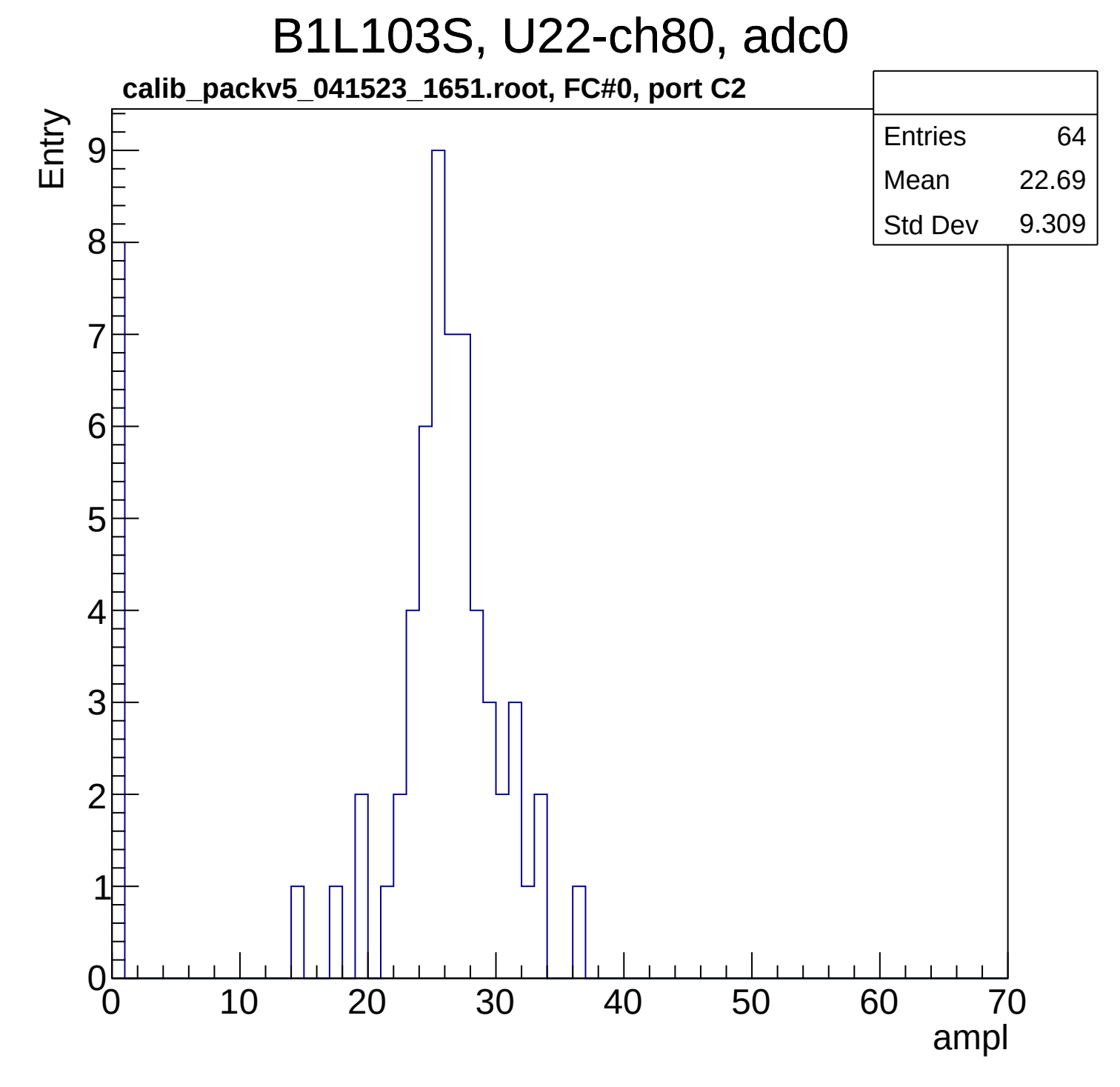
60
70


B1L103S, U22-ch79, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 62
Std Dev 1.5
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch79, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch80, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 22.69
Std Dev 9.309
Entry
ampl
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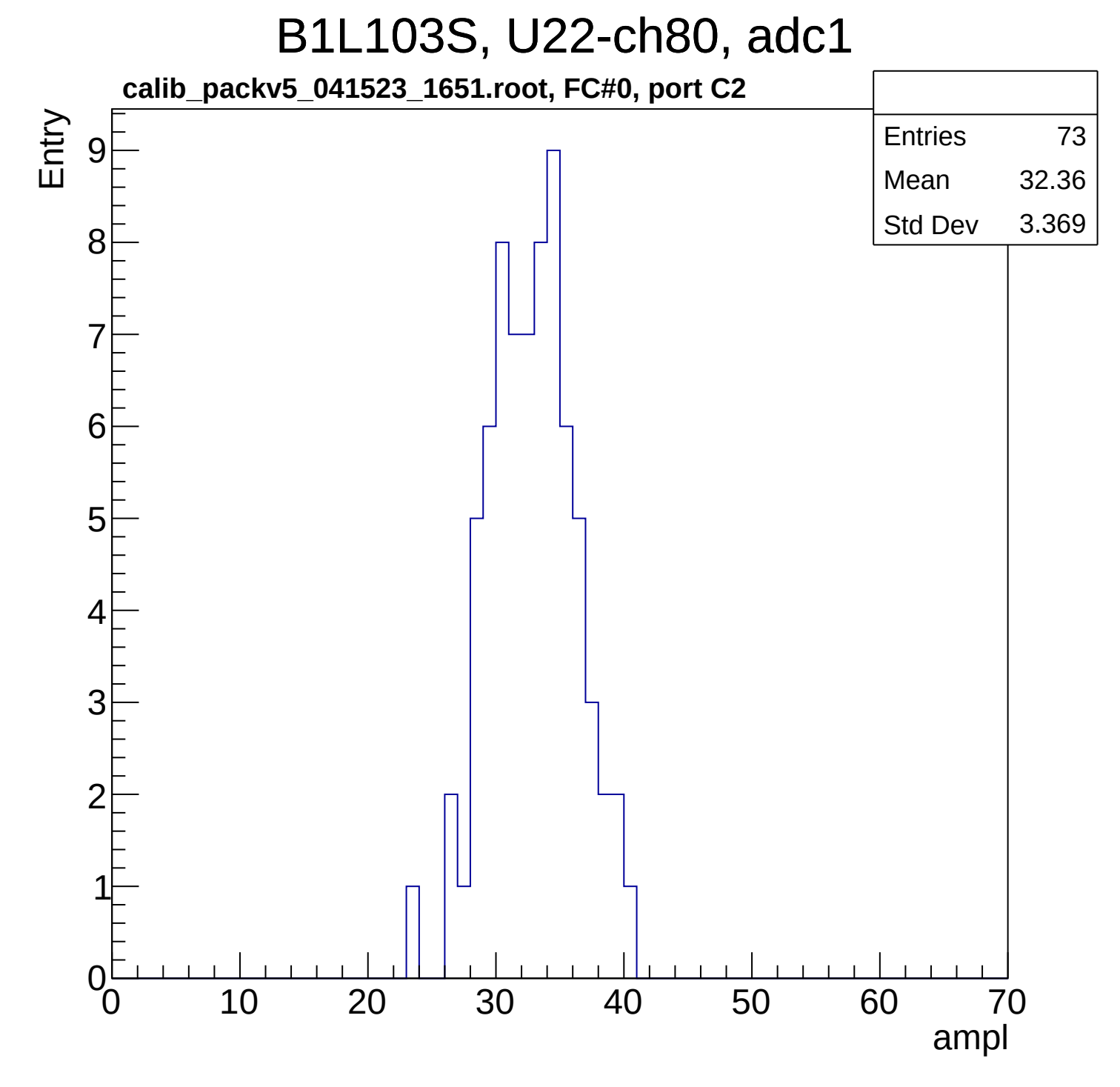
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch80, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 32.36
Std Dev 3.369
Entry
ampl
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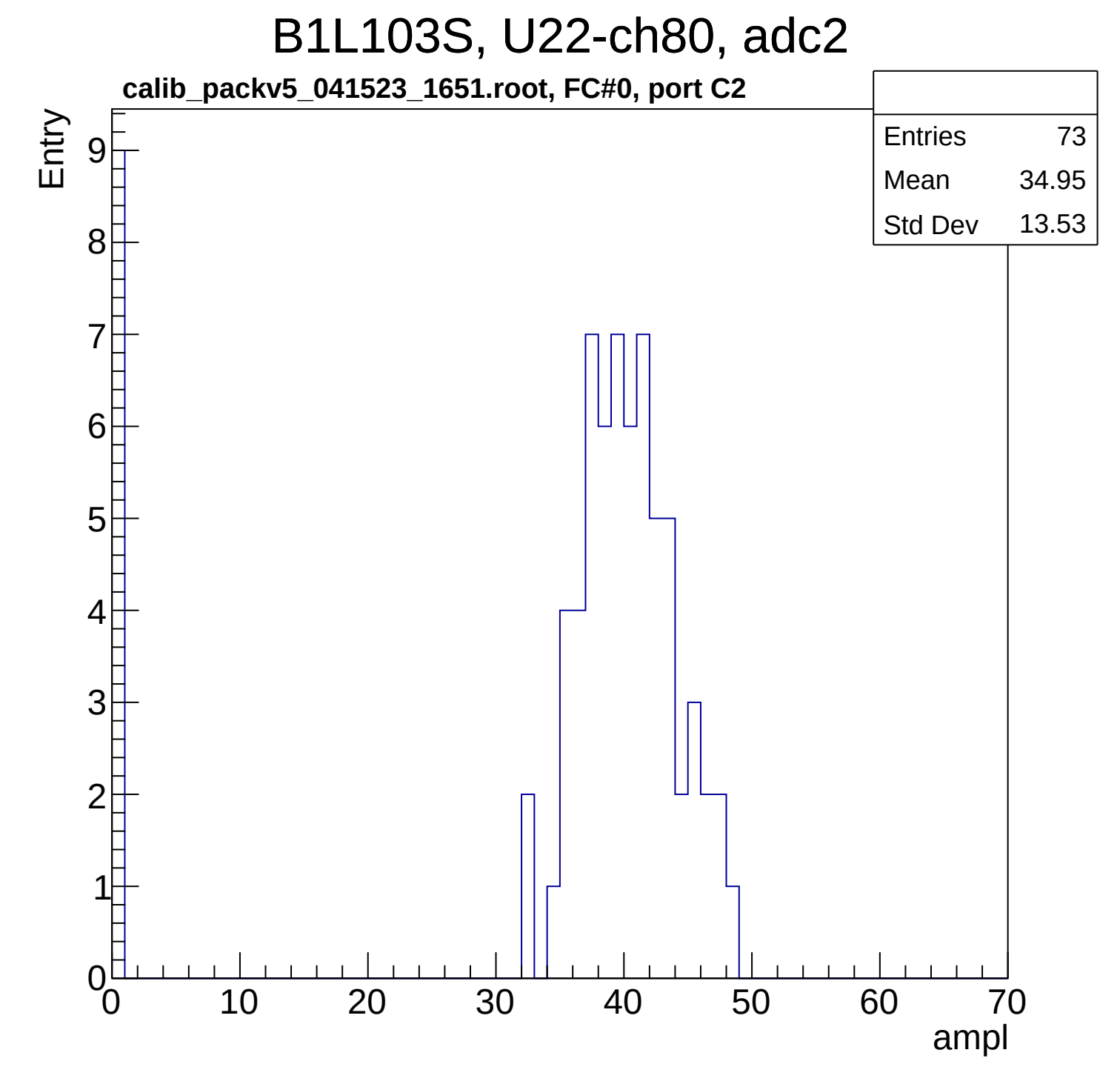
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch80, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 34.95
Std Dev 13.53
Entry
ampl
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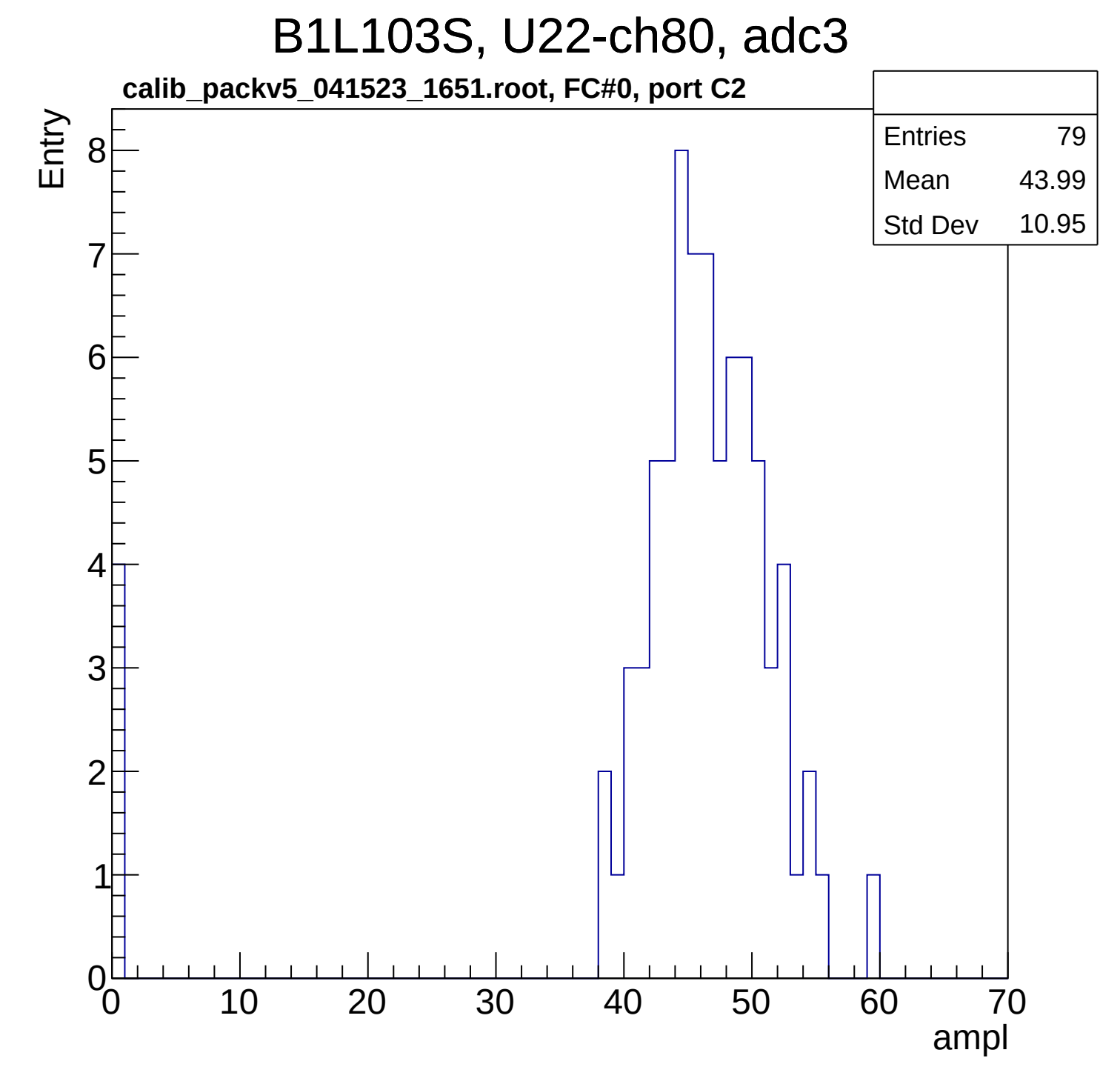
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch80, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 43.99
Std Dev 10.95
Entry
ampl
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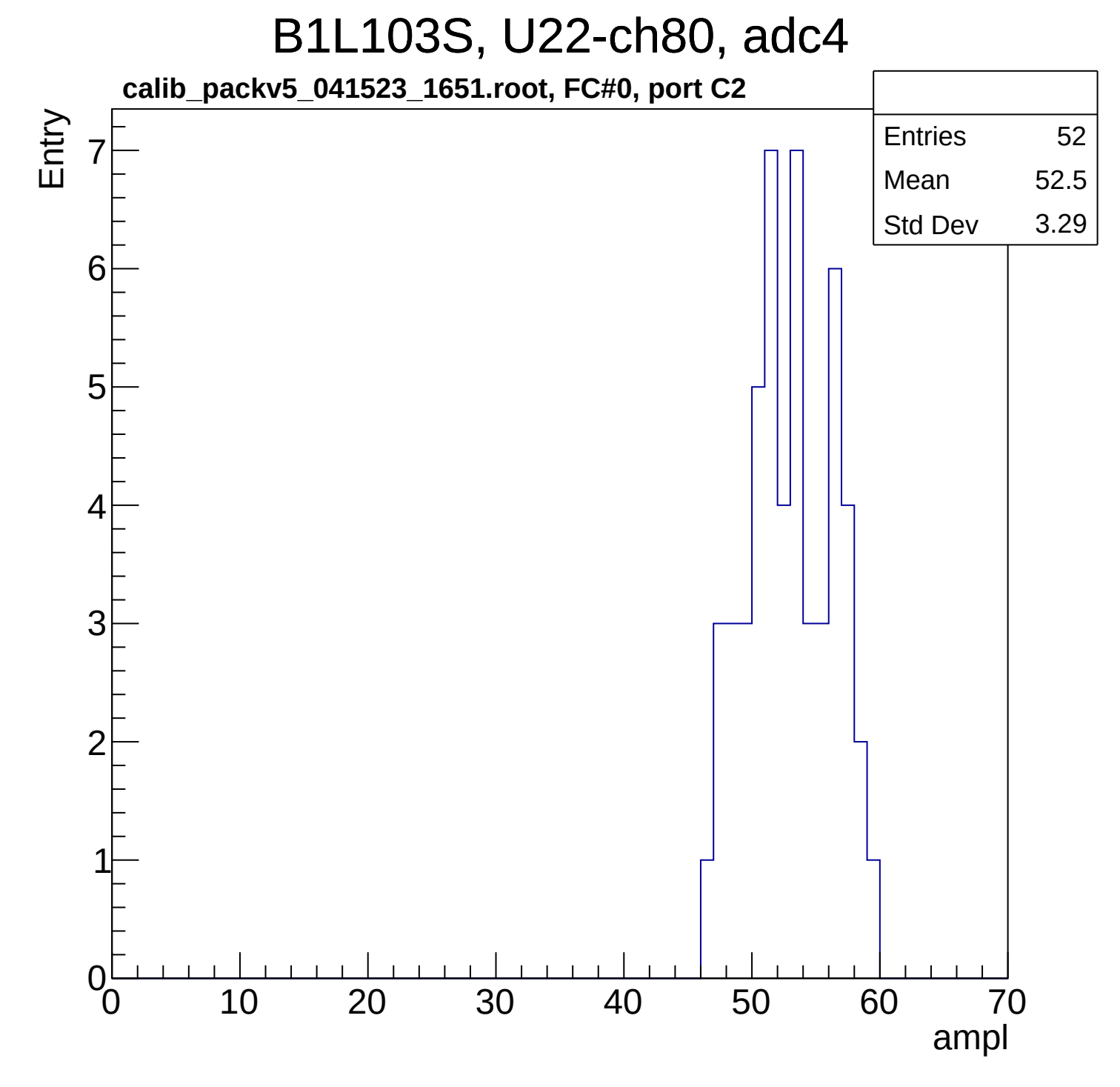
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch80, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 52.5
Std Dev 3.29
Entry
ampl
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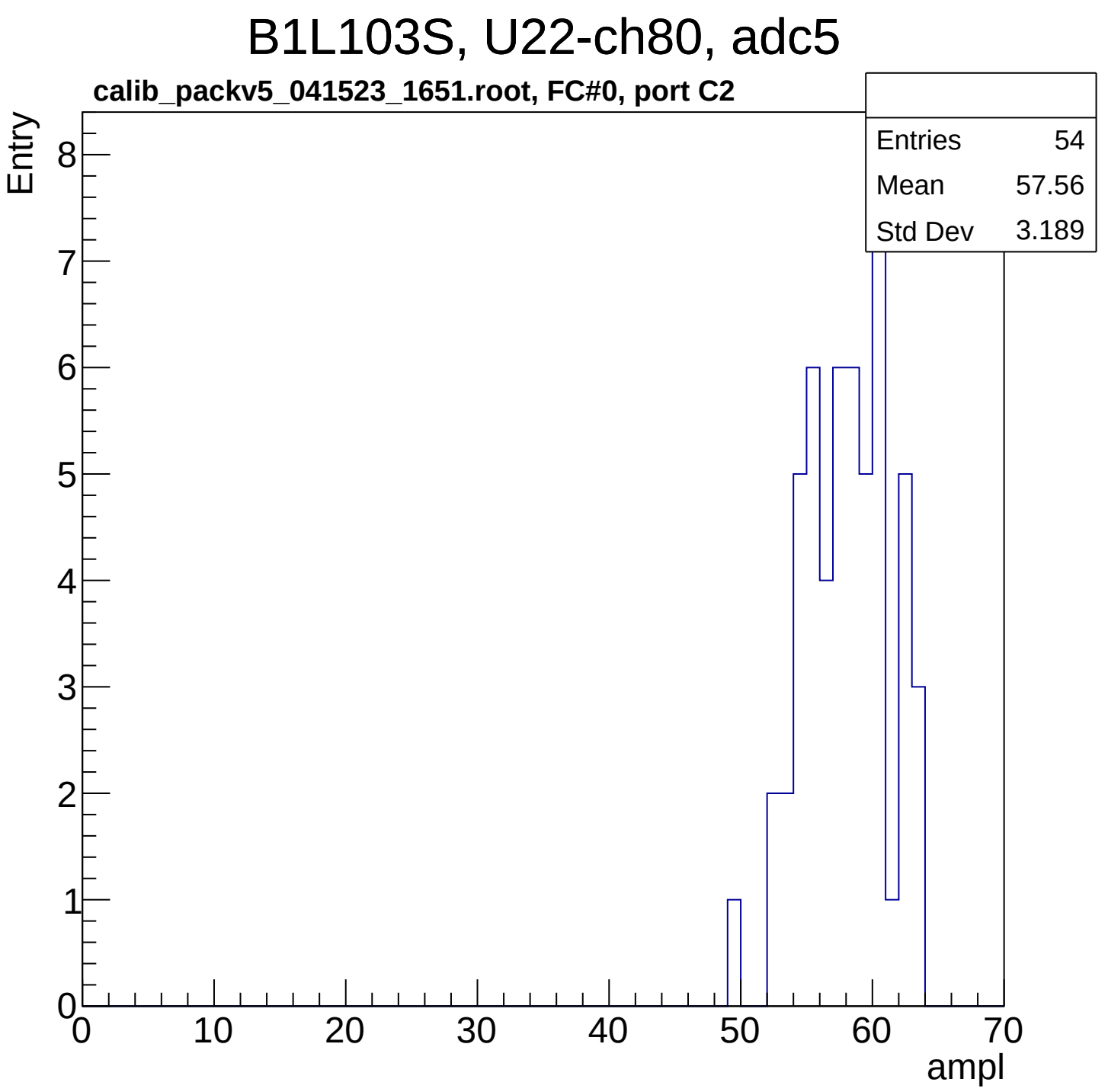
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U22-ch80, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 57.56
Std Dev 3.189
Entry
ampl
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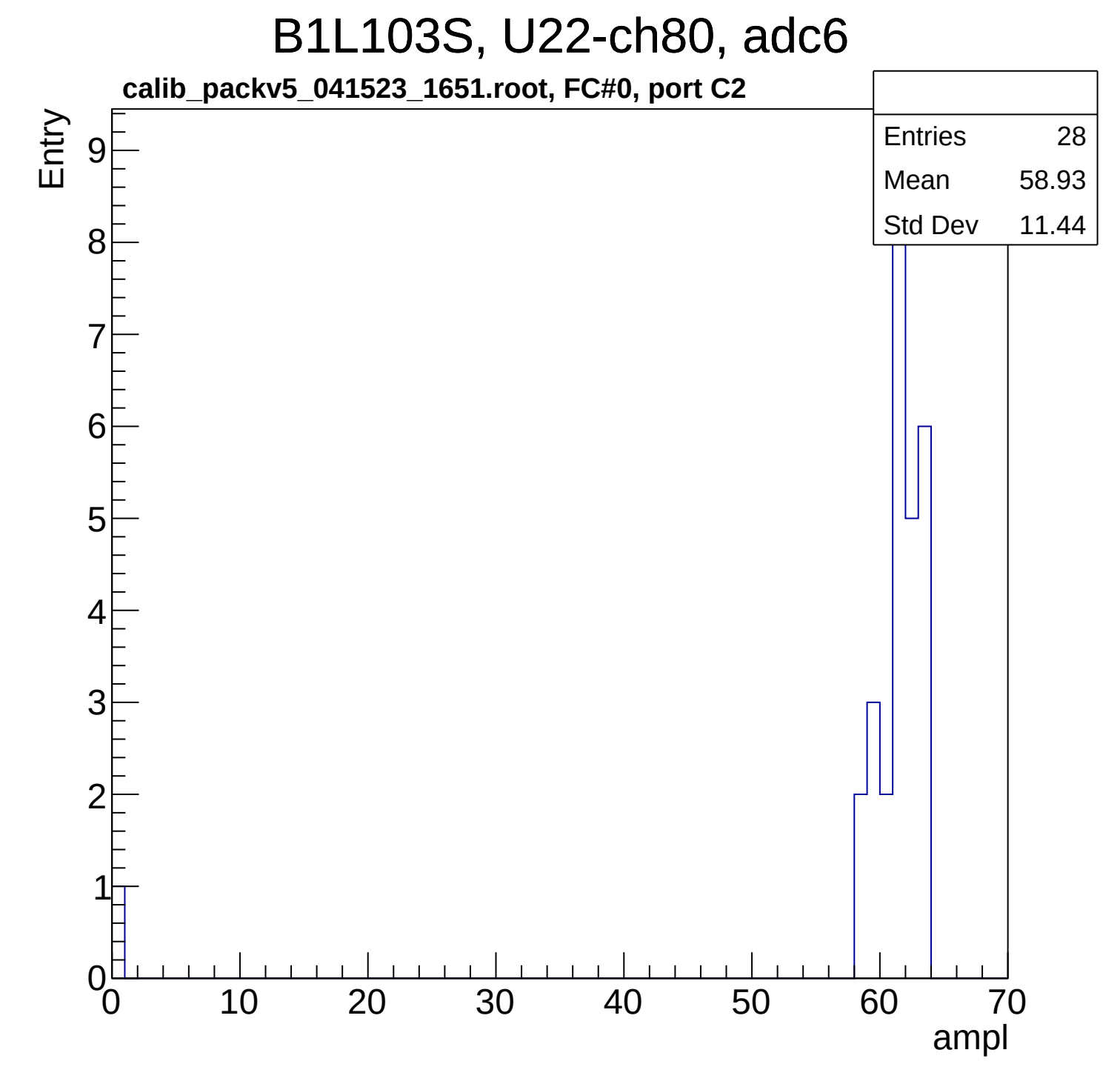
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch80, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 58.93
Std Dev 11.44
Entry
ampl
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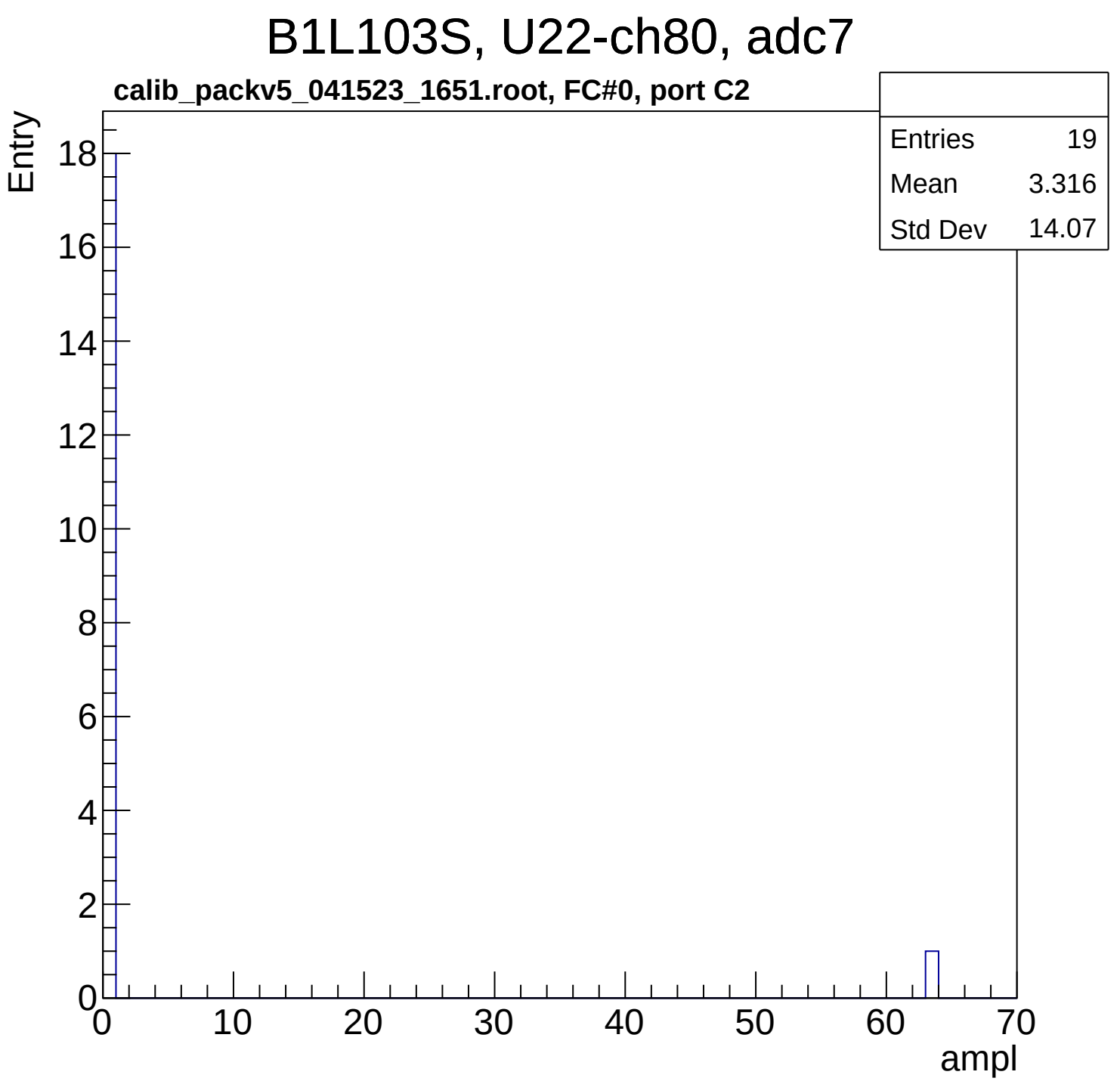
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch80, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.316
Std Dev 14.07
Entry
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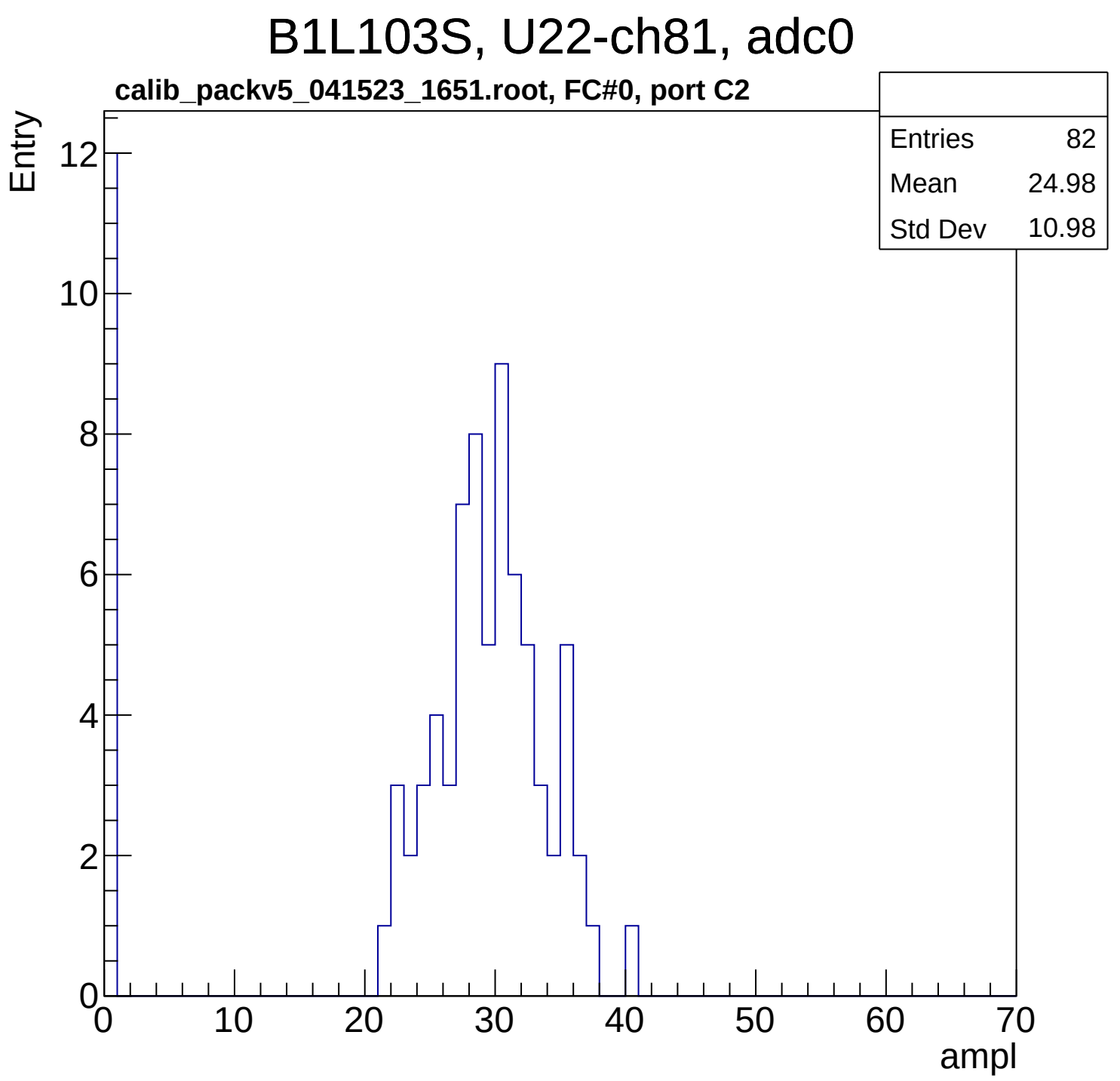
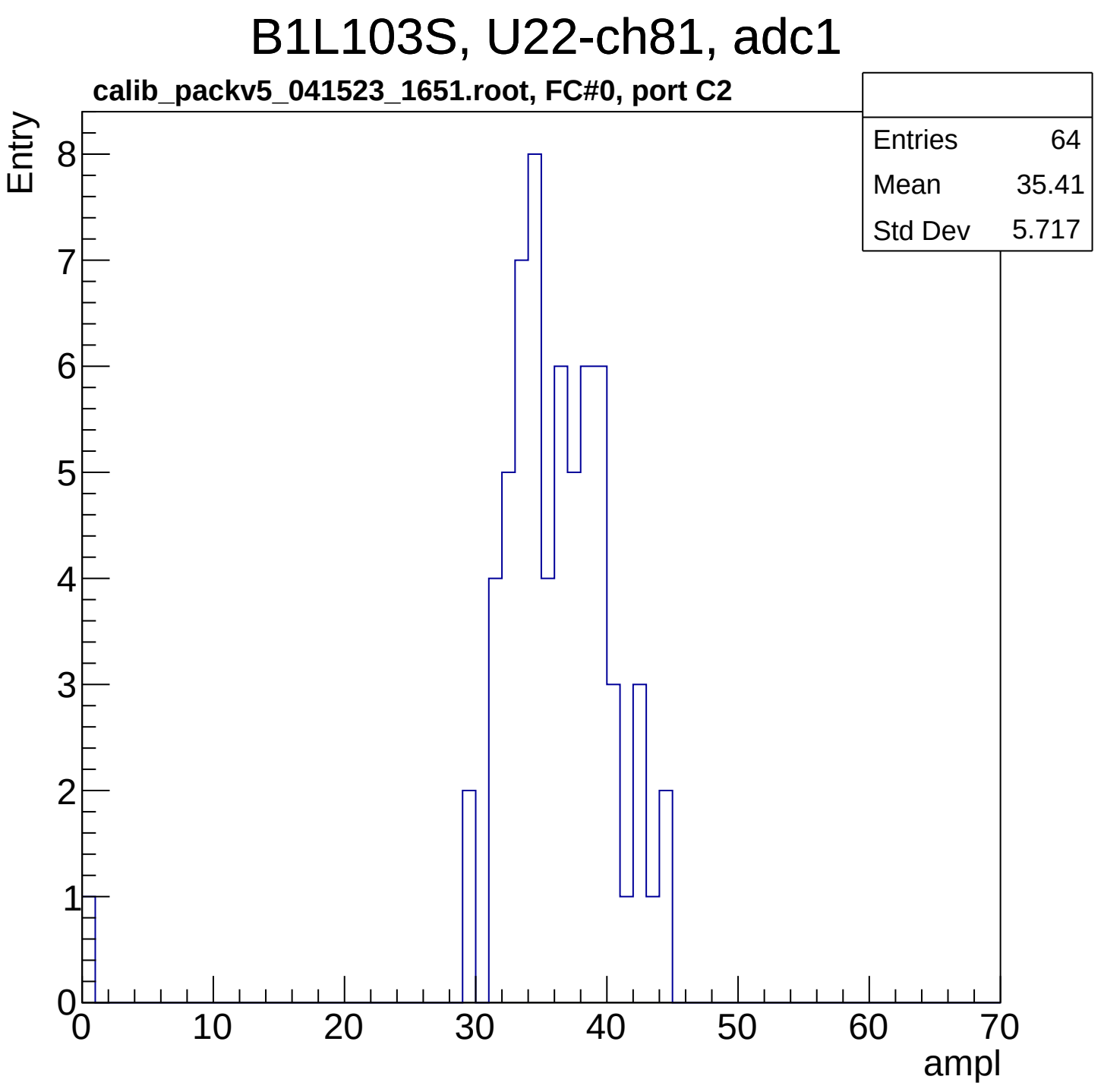
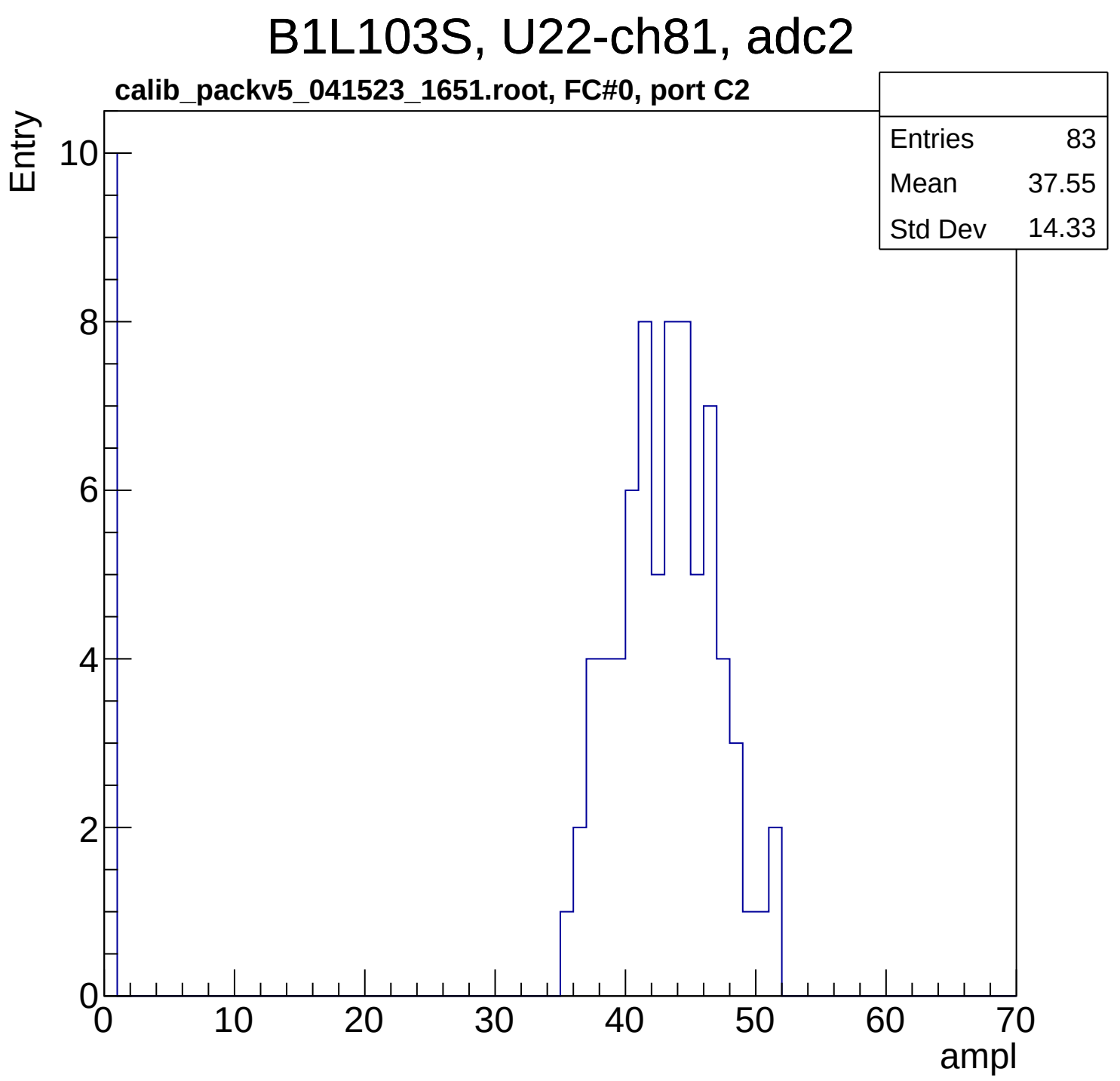
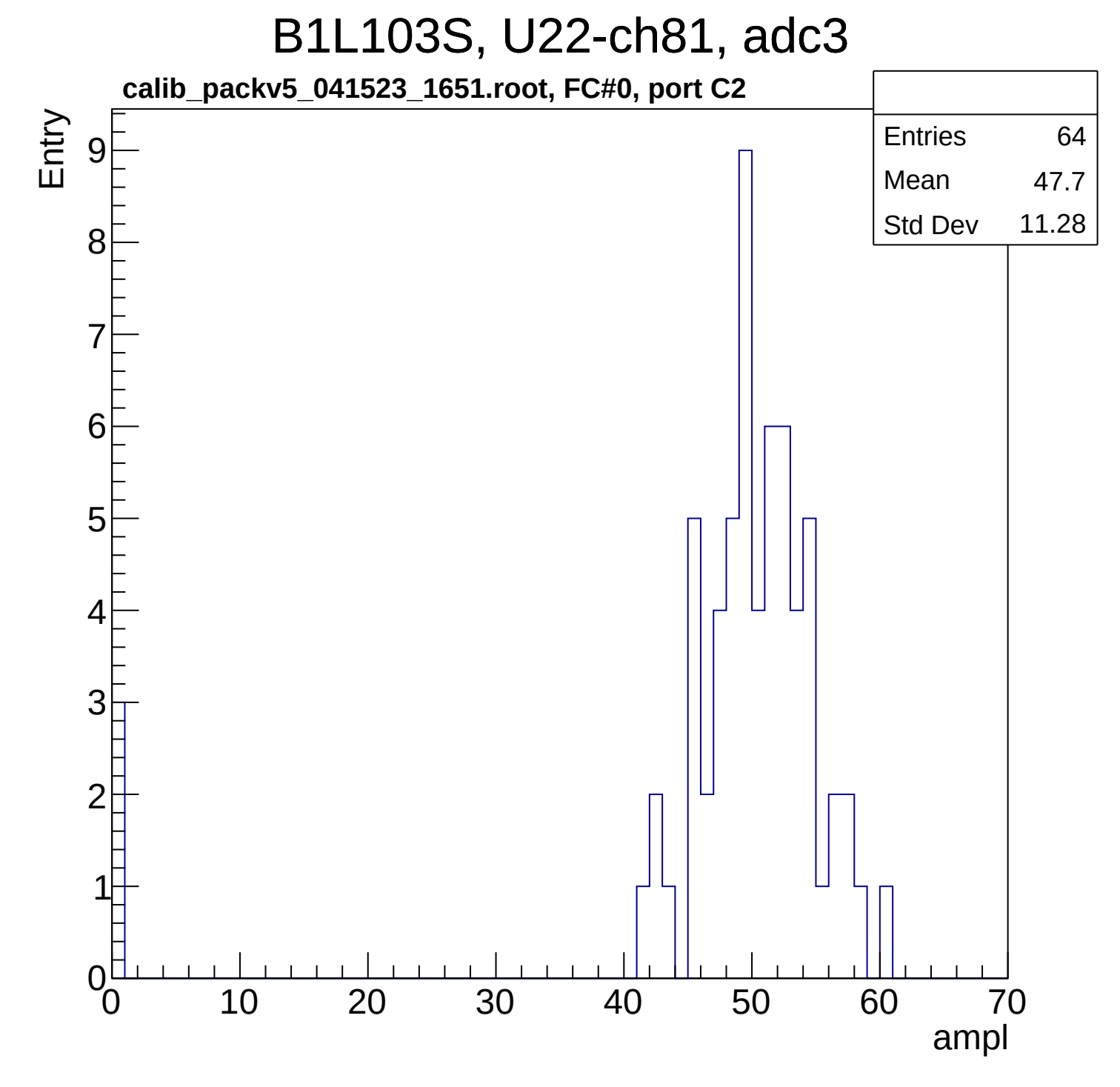
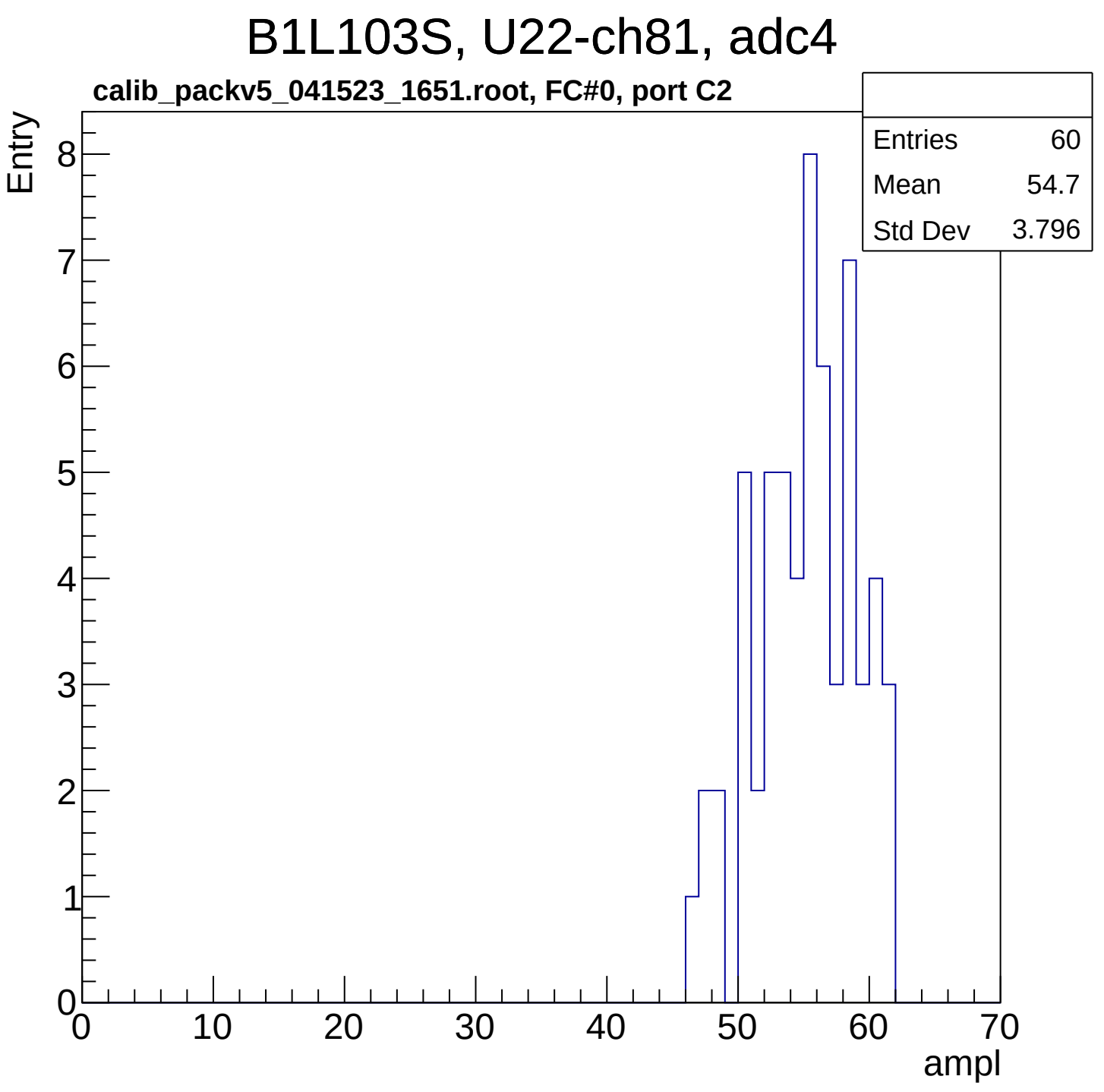
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch81, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 24.98
Std Dev 10.98
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch81, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 35.41
Std Dev 5.717
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch81, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 37.55
Std Dev 14.33
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch81, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 47.7
Std Dev 11.28
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L103S, U22-ch81, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 54.7
Std Dev 3.796
Entry
ampl
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1
2
3
4
5
6
7
8
0
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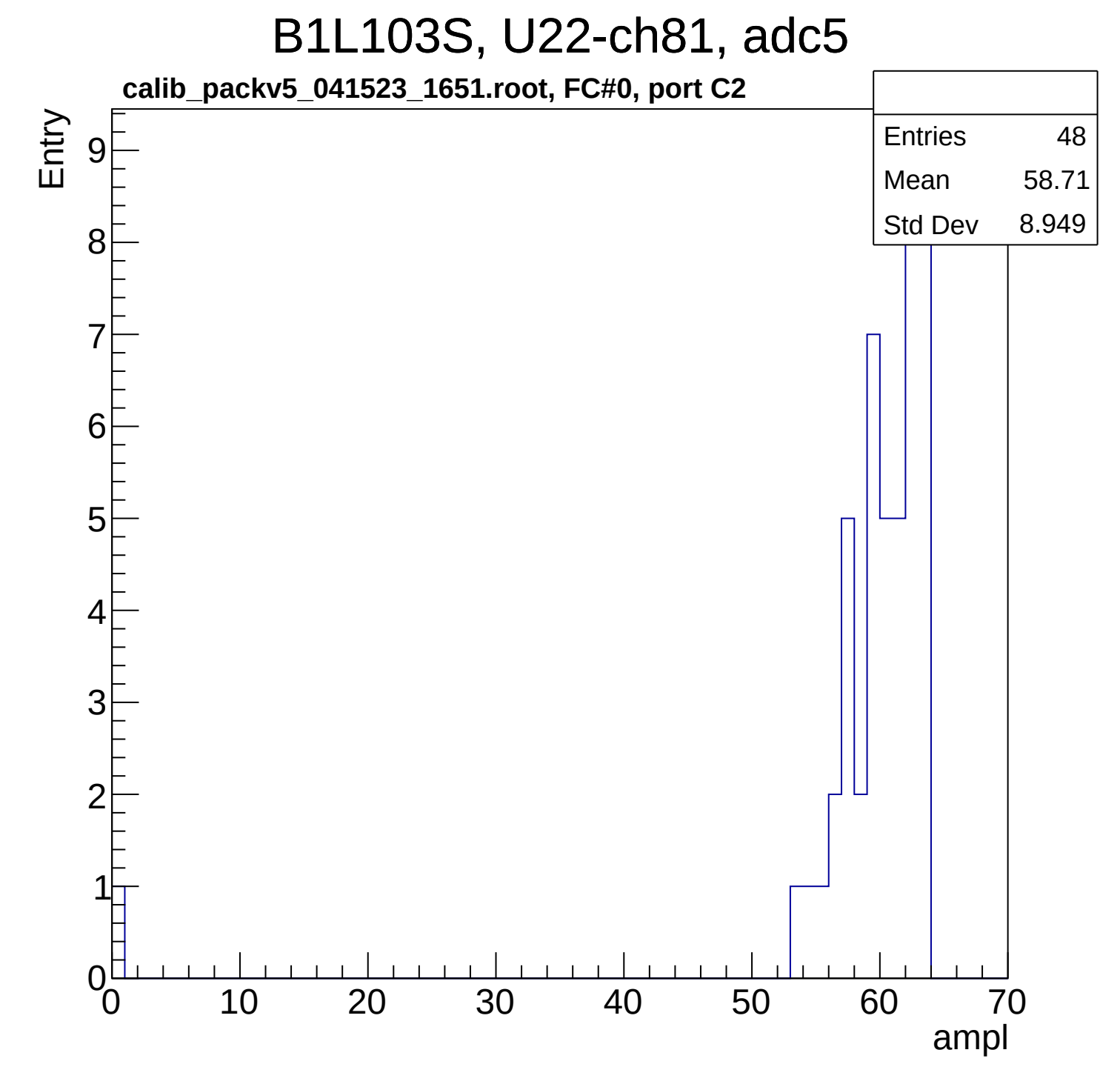
20
30
40
50
60
70


B1L103S, U22-ch81, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 58.71
Std Dev 8.949
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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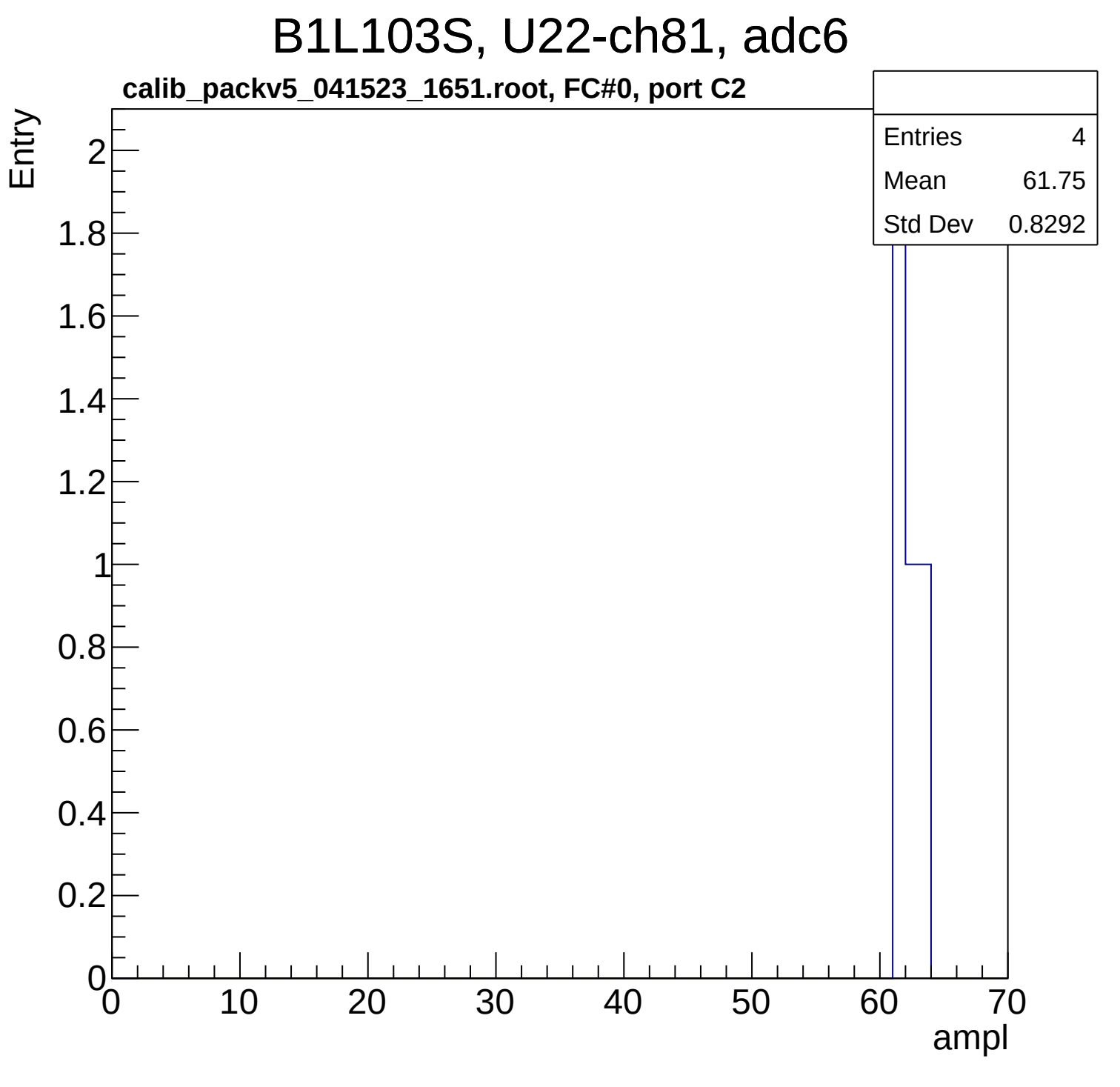
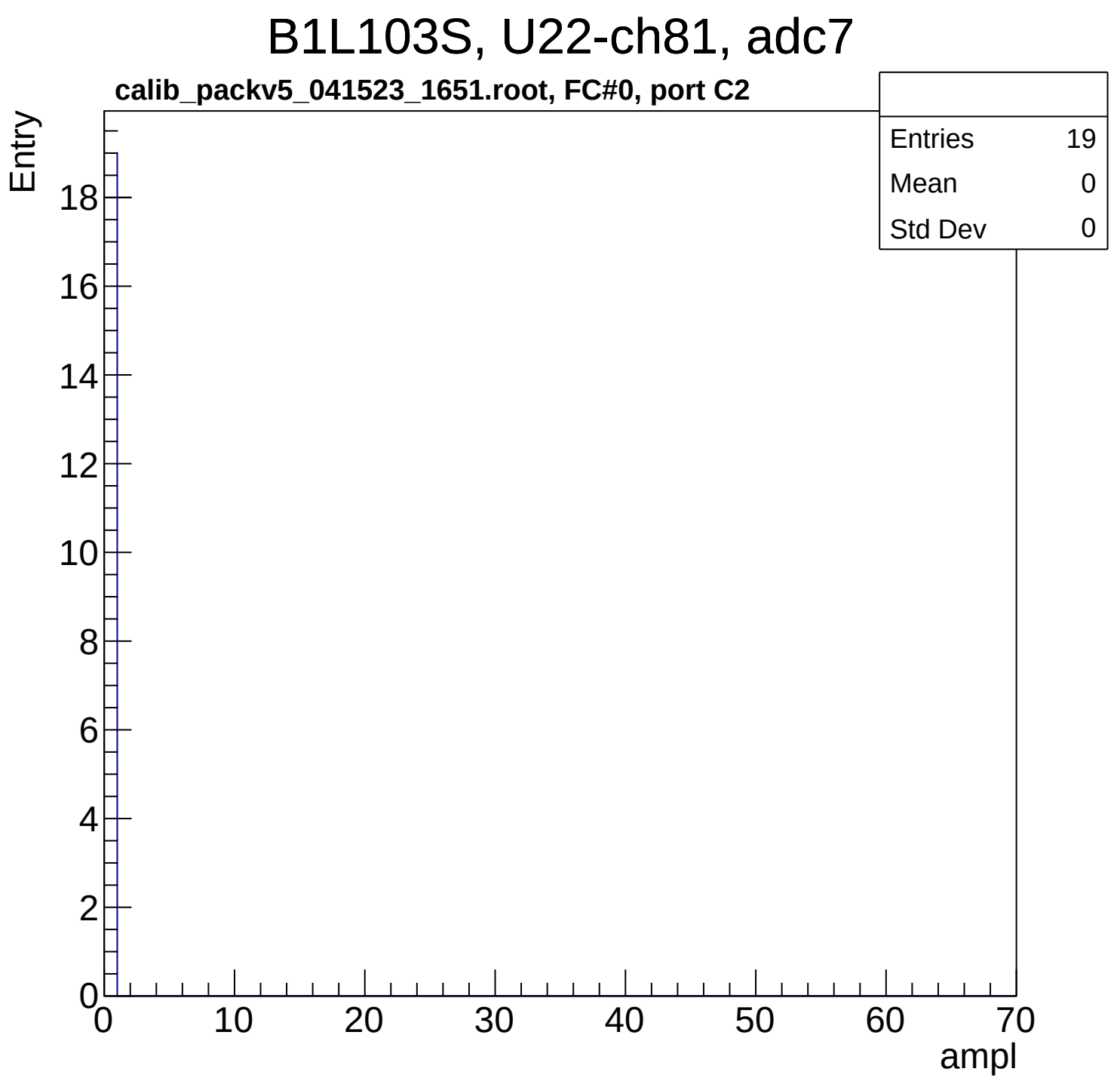
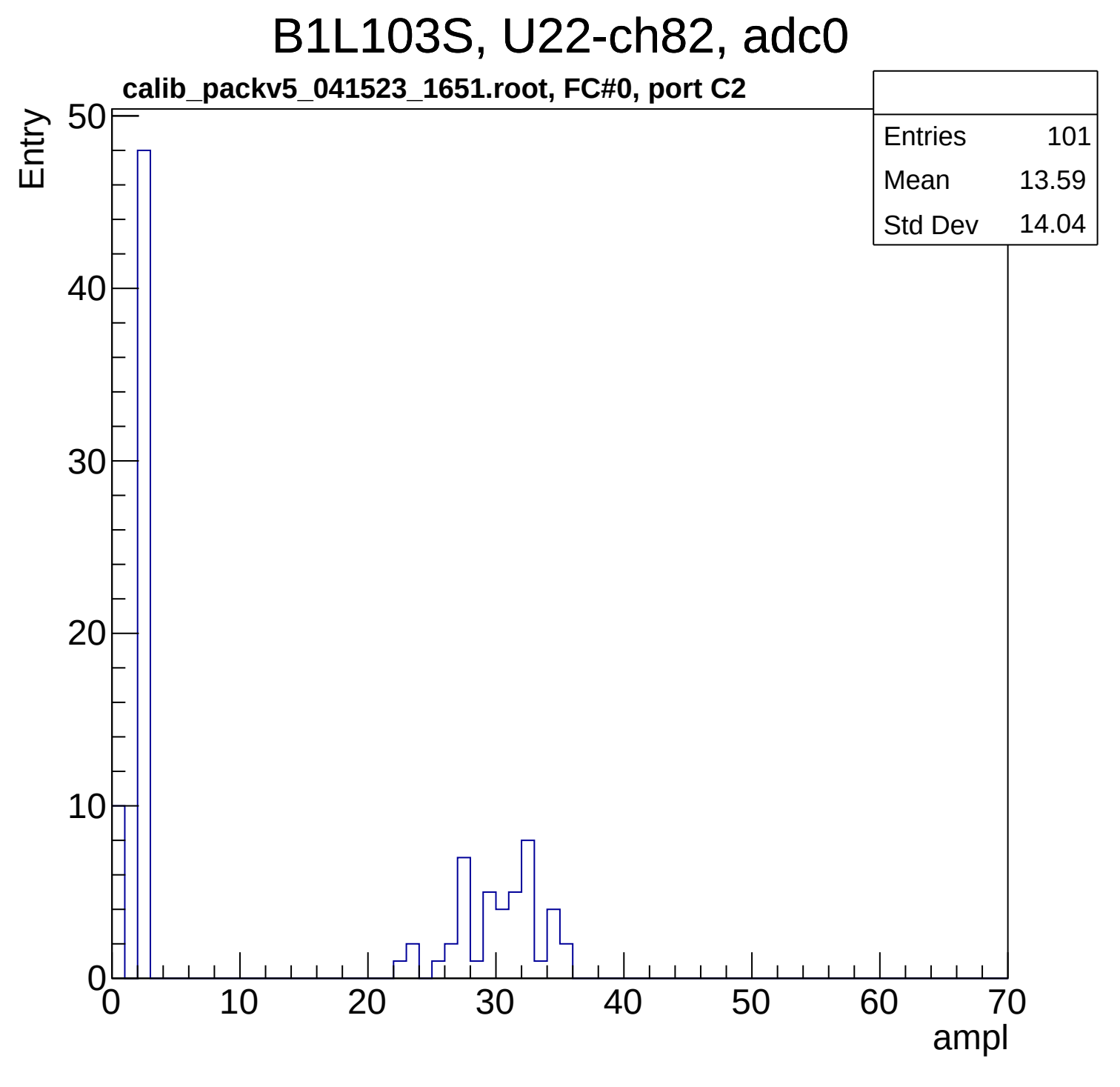
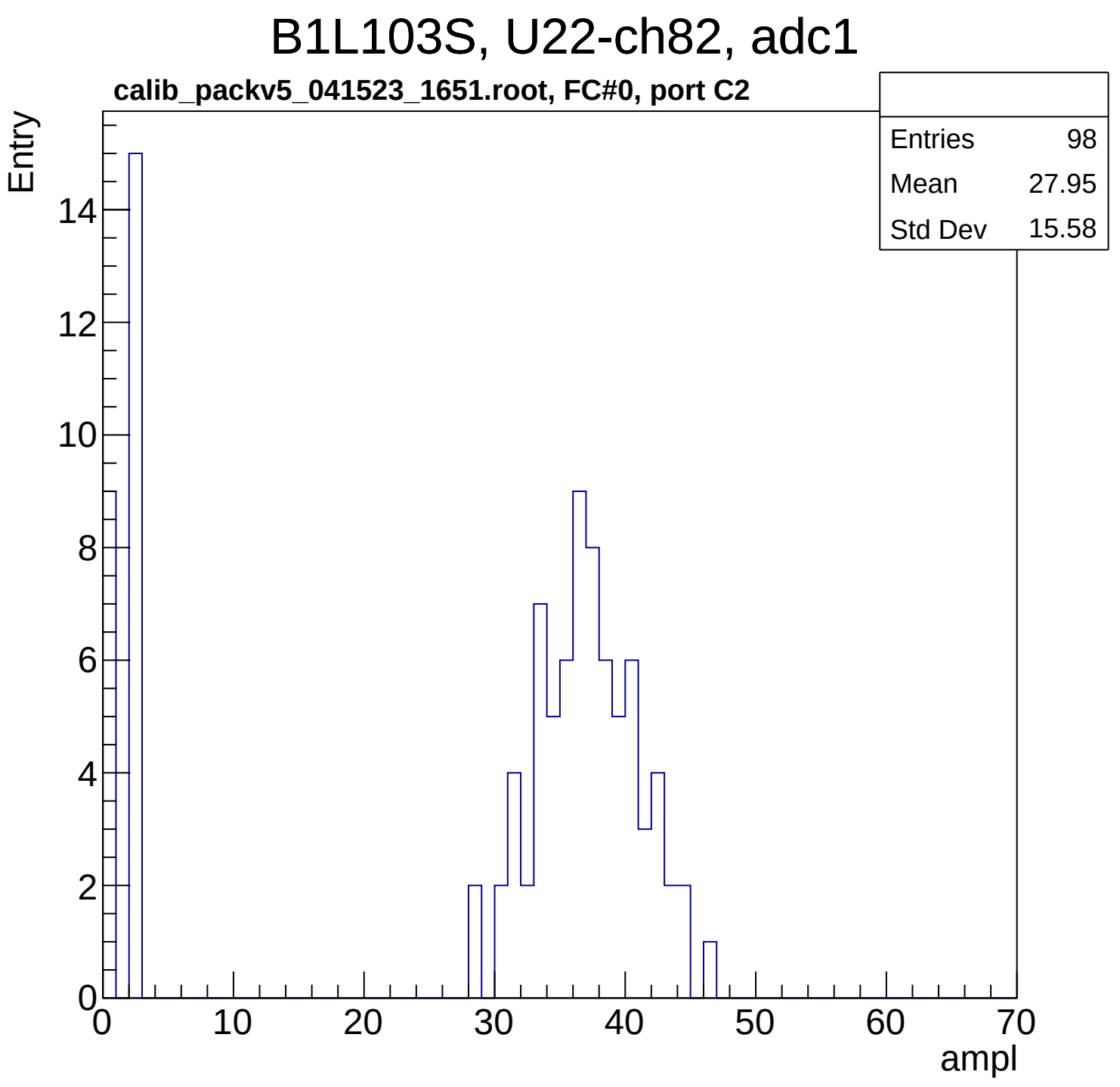
40
50
60
70


B1L103S, U22-ch81, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 61.75
Std Dev 0.8292
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U22-ch81, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch82, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 101
Mean 13.59
Std Dev 14.04
Entry
ampl
0
10
20
30
40
50
60
70


B1L103S, U22-ch82, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 98
Mean 27.95
Std Dev 15.58
Entry
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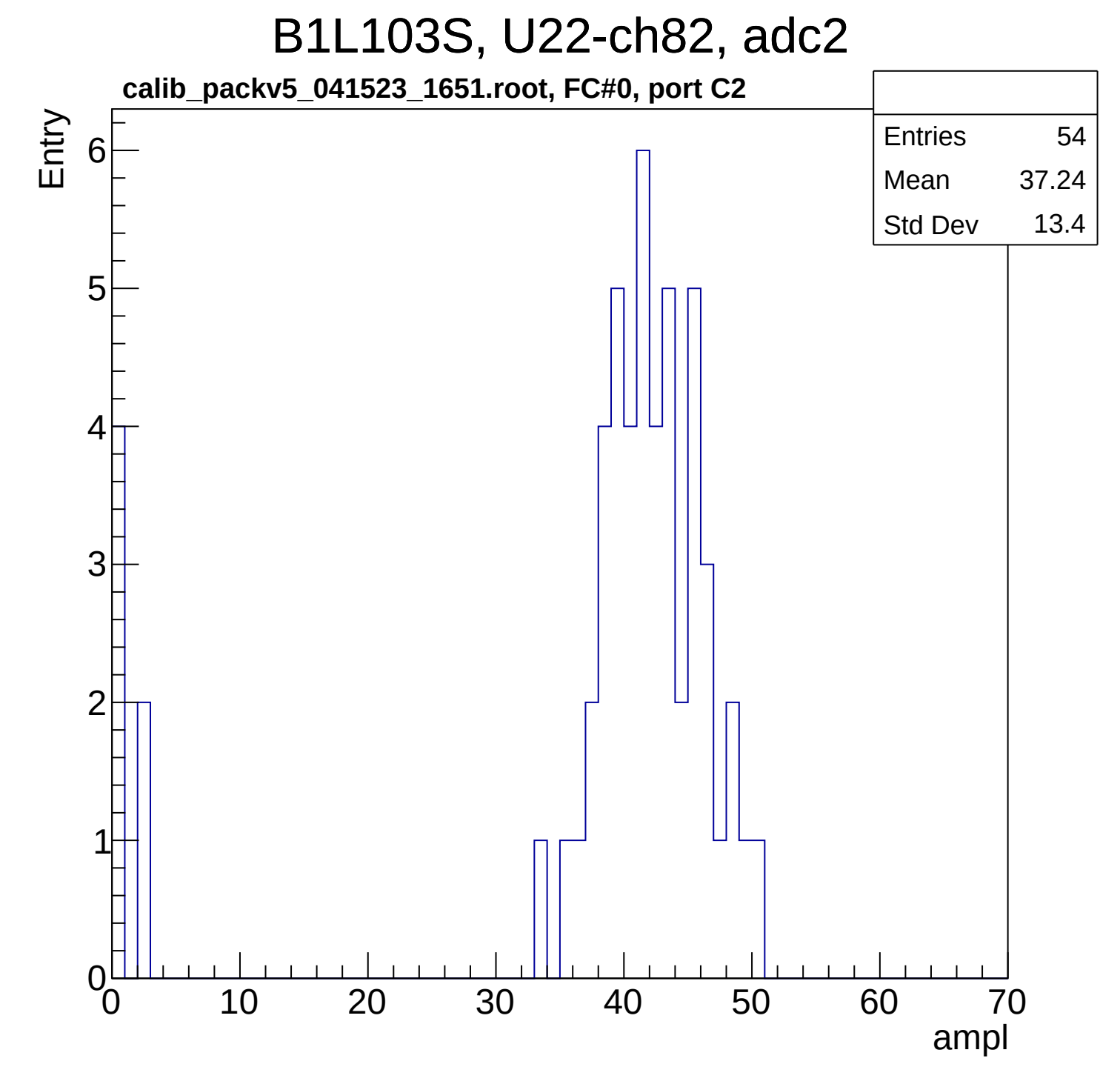
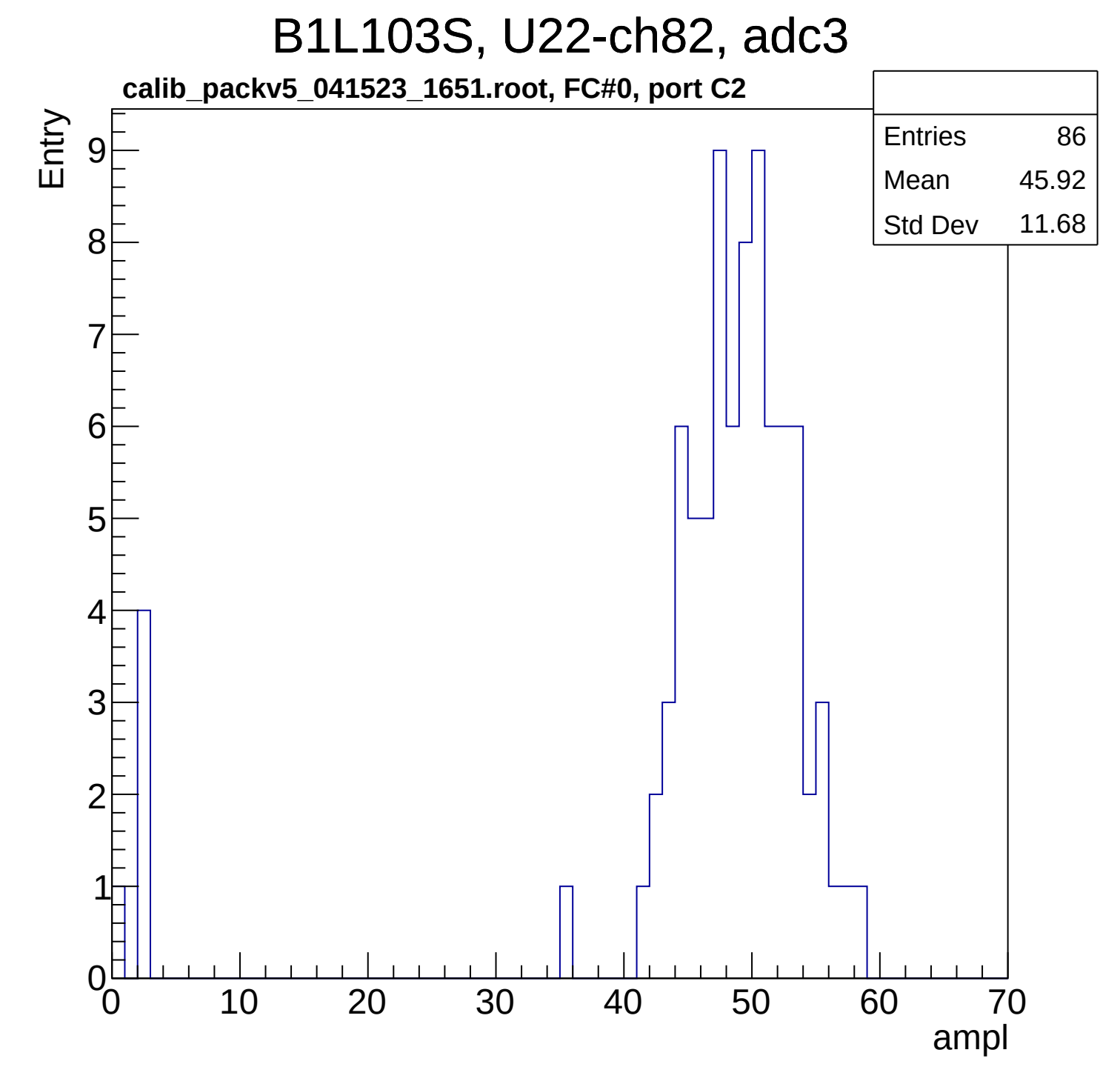
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch82, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 37.24
Std Dev 13.4
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch82, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 45.92
Std Dev 11.68
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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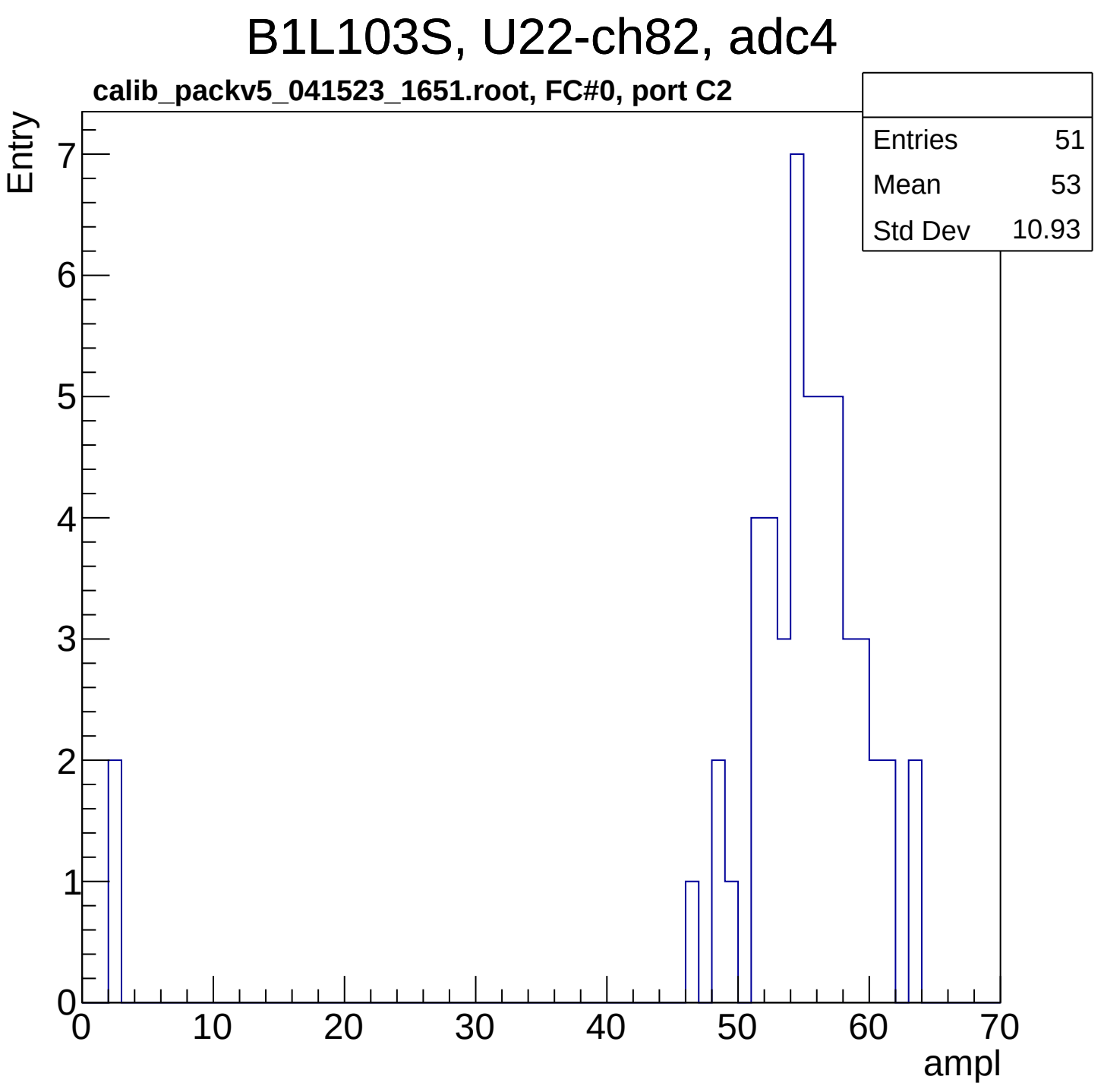
40
50
60
70


B1L103S, U22-ch82, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 53
Std Dev 10.93
Entry
ampl
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2
3
4
5
6
7
0
10
20
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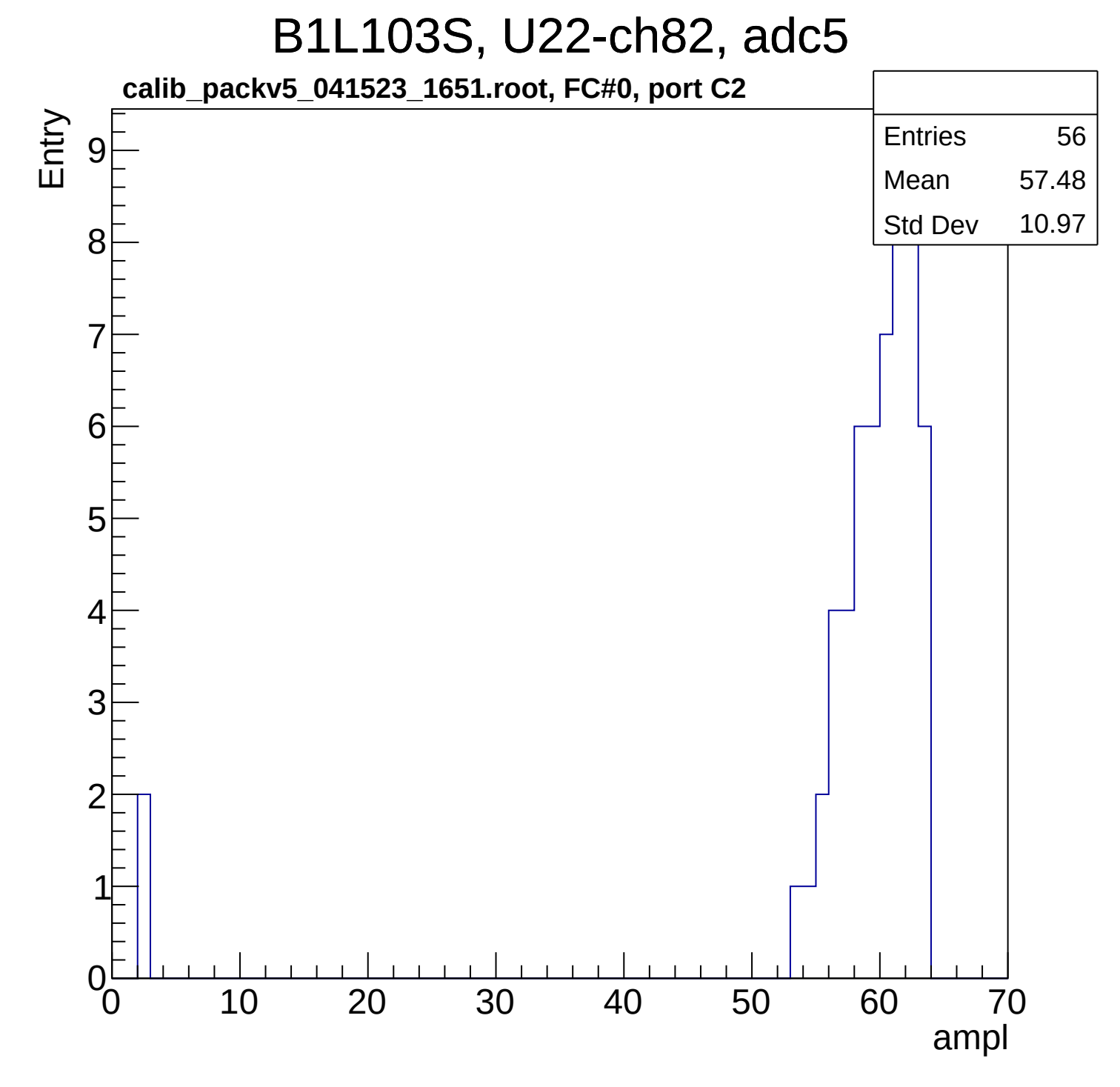
40
50
60
70


B1L103S, U22-ch82, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 57.48
Std Dev 10.97
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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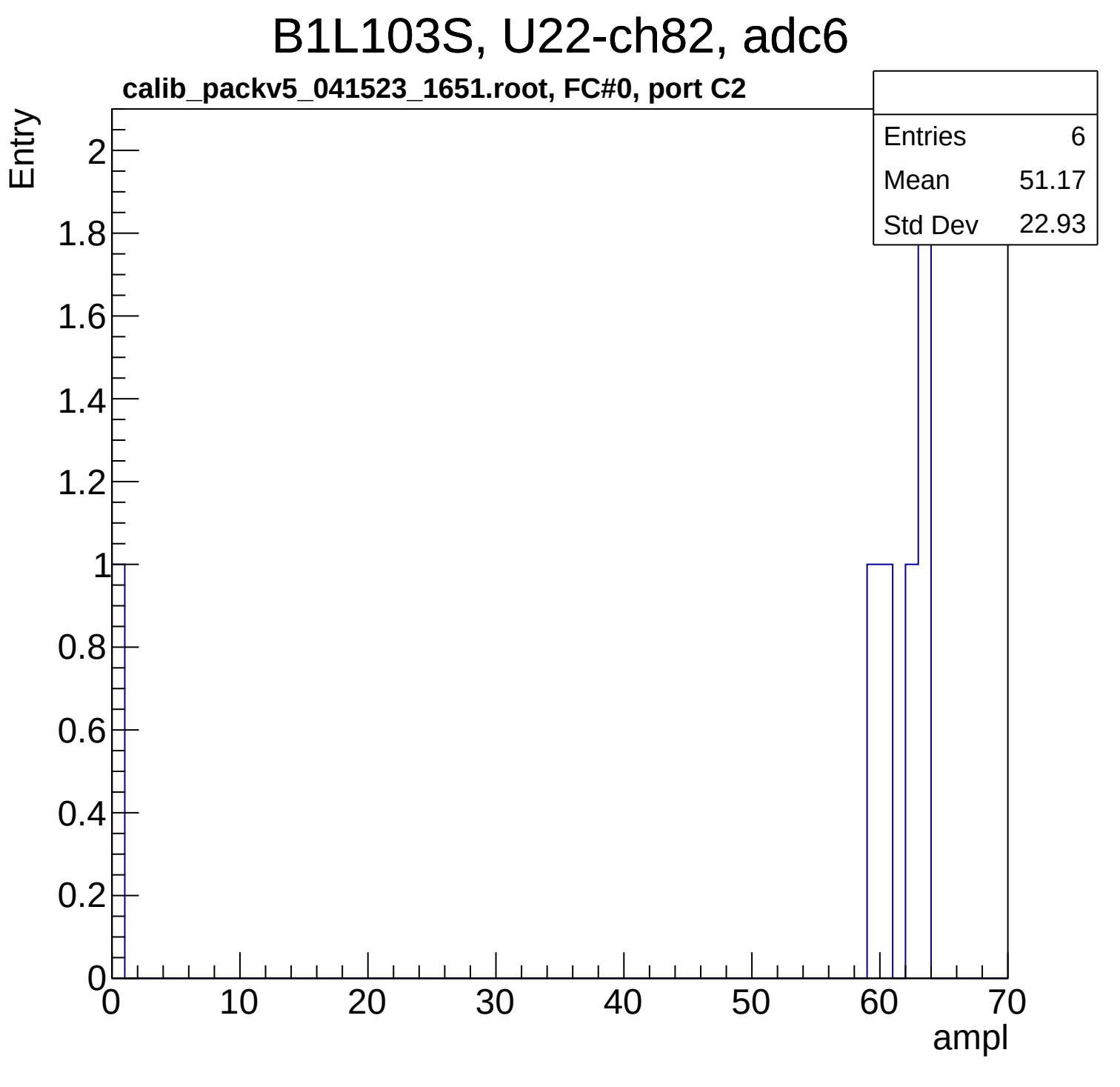
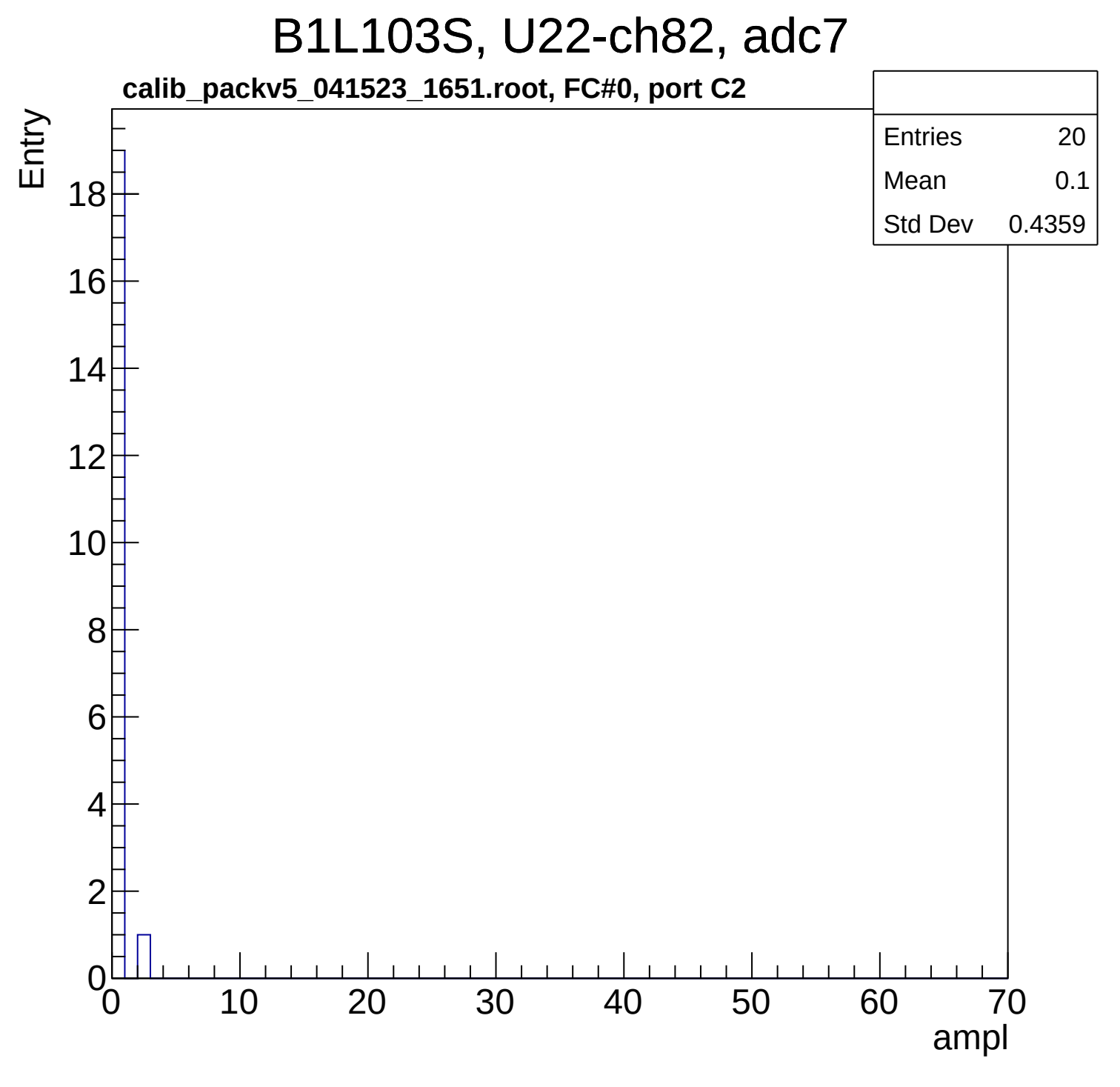
40
50
60
70


B1L103S, U22-ch82, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 51.17
Std Dev 22.93
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U22-ch82, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 0.1
Std Dev 0.4359
Entry
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6
8
10
12
14
16
18
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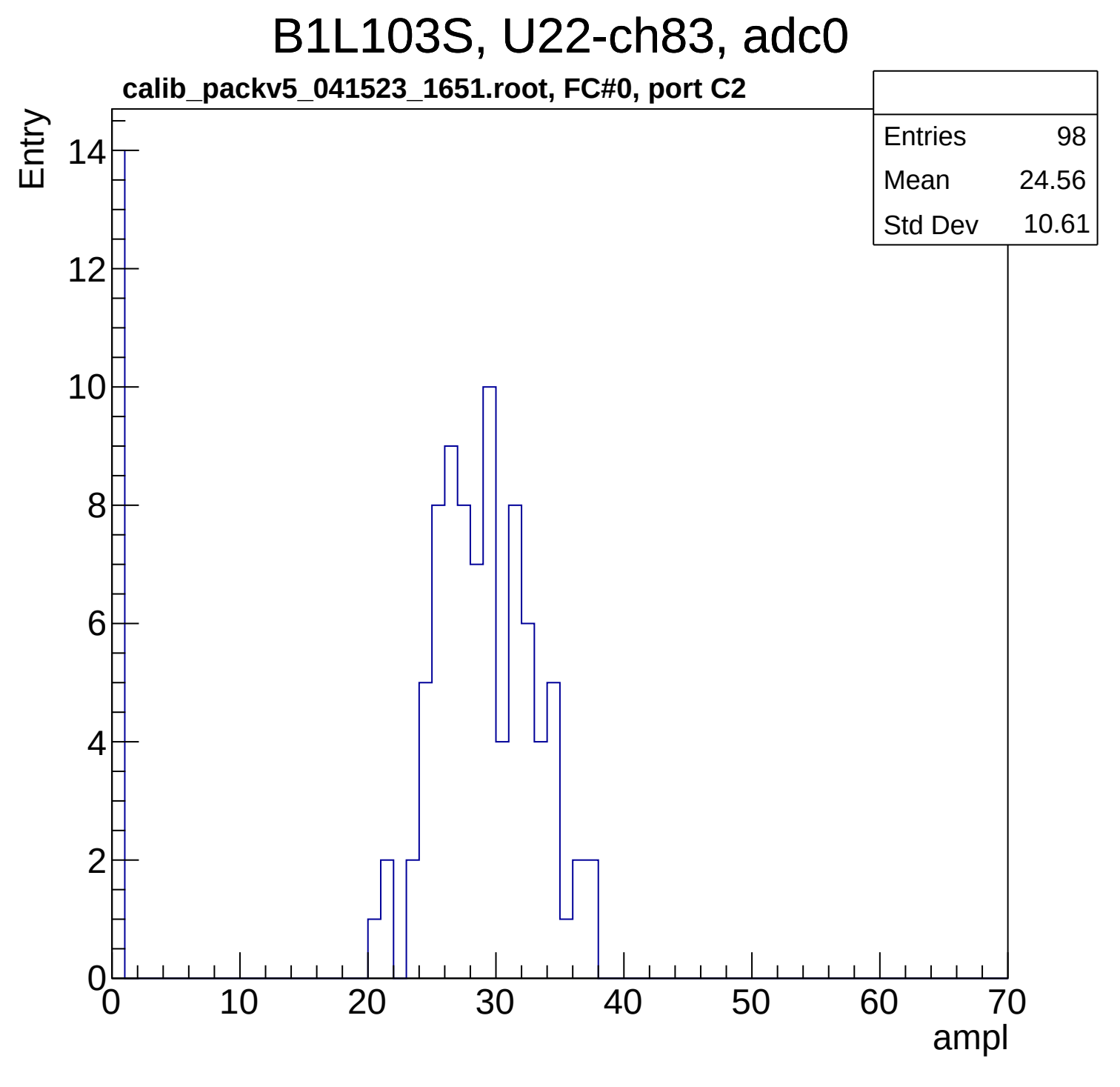
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch83, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 98
Mean 24.56
Std Dev 10.61
Entry
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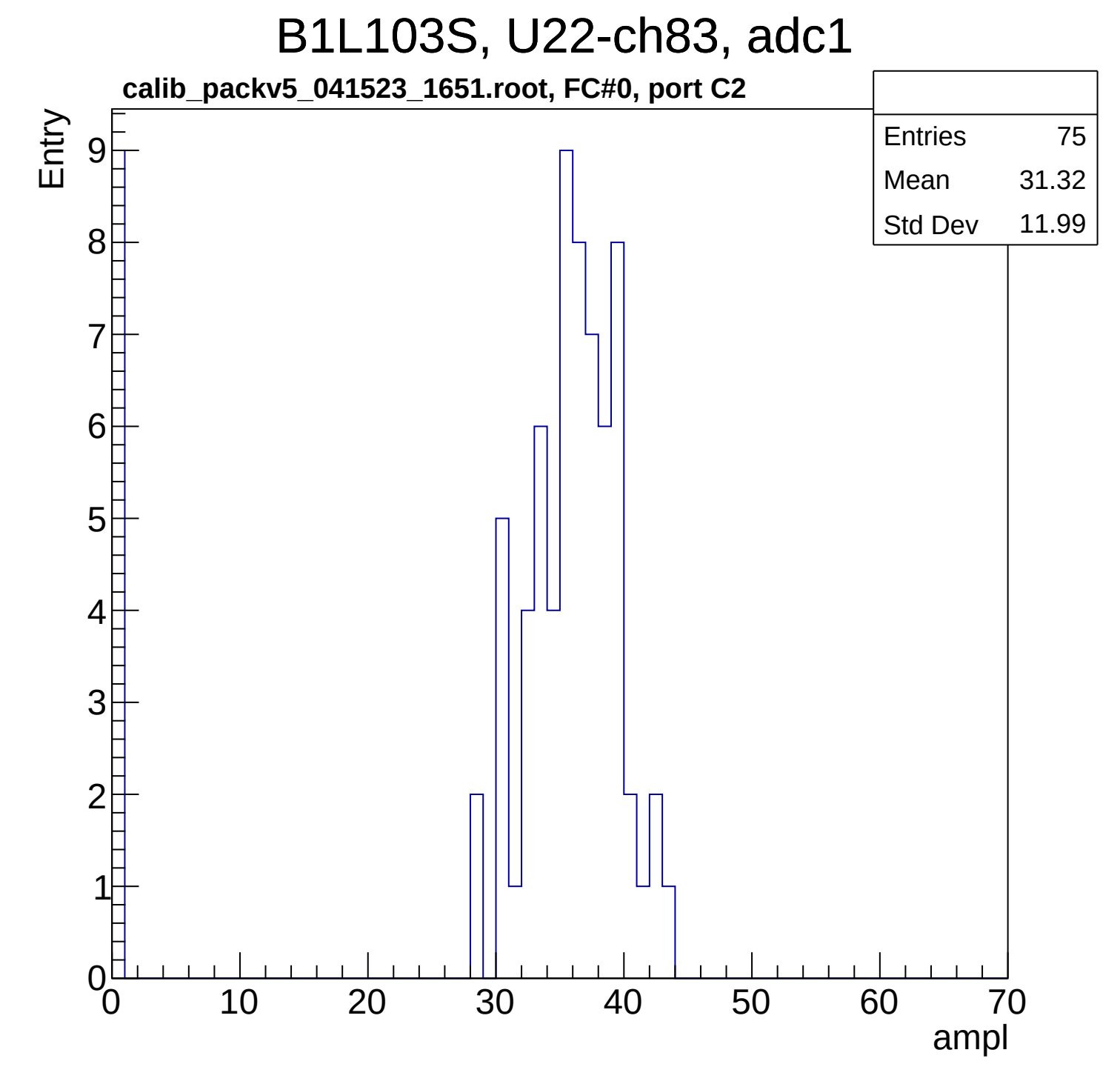
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch83, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 31.32
Std Dev 11.99
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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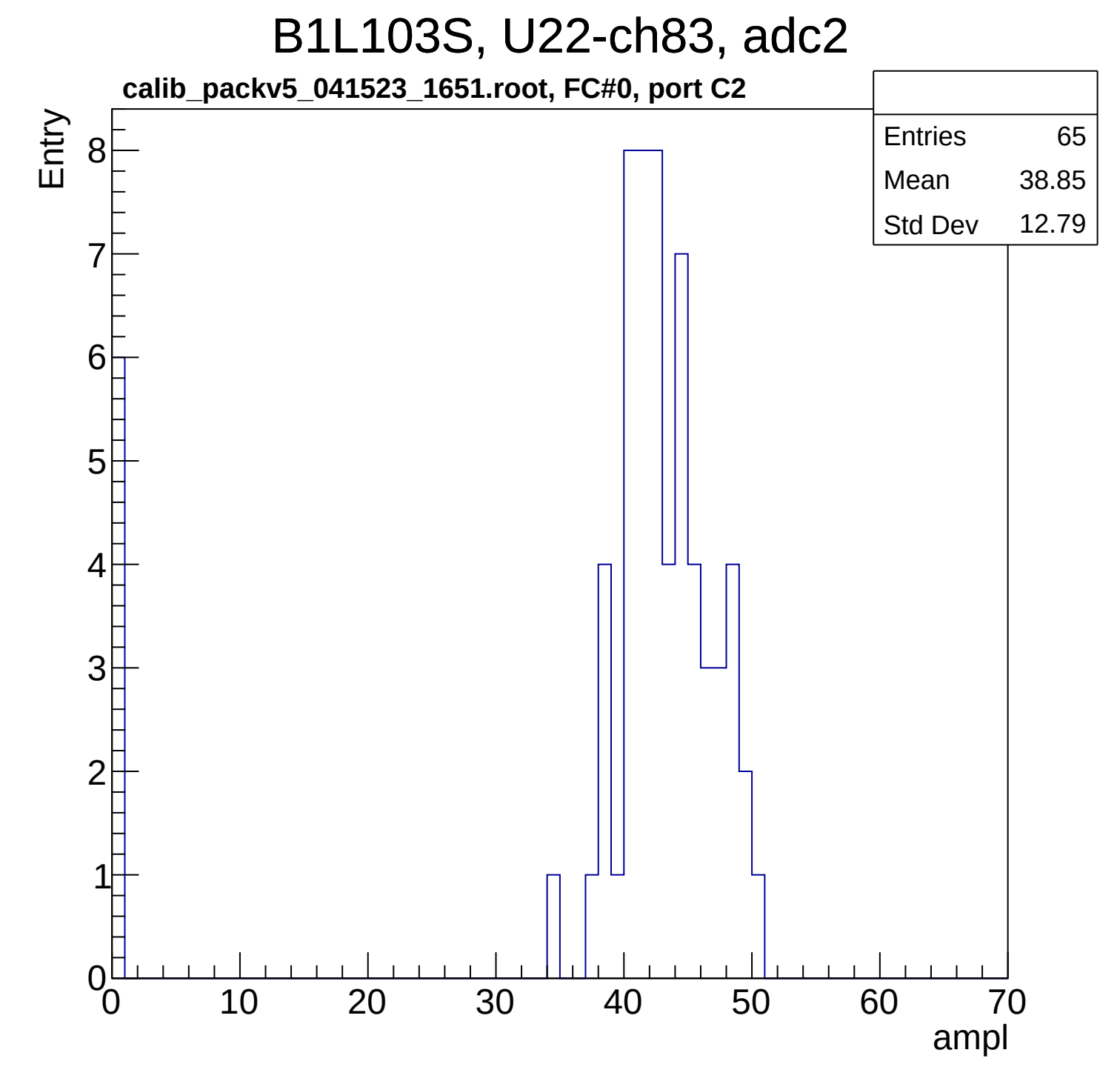
40
50
60
70


B1L103S, U22-ch83, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 38.85
Std Dev 12.79
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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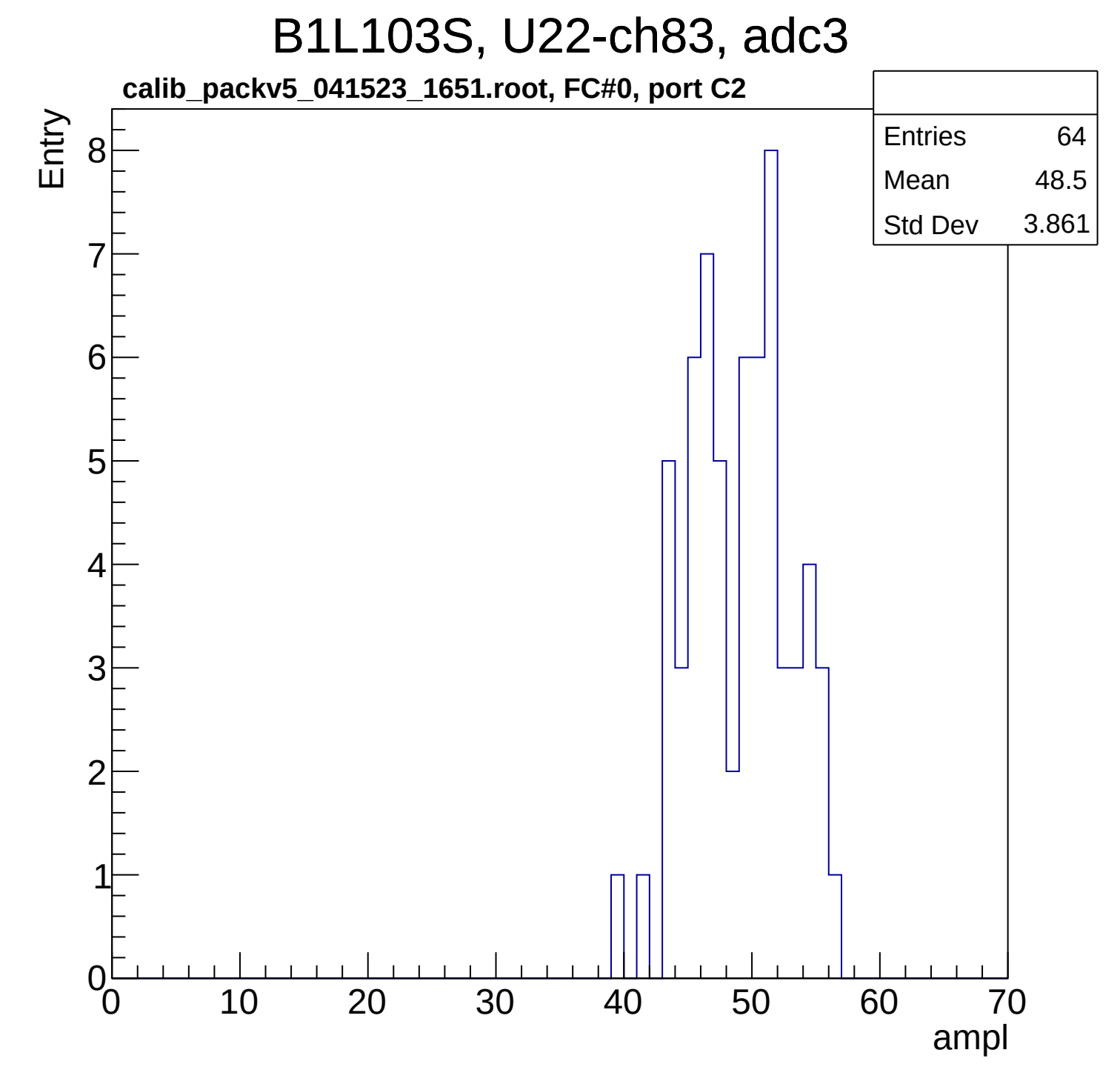
B1L103S, U22-ch83, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 48.5
Std Dev 3.861
Entry
ampl
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2
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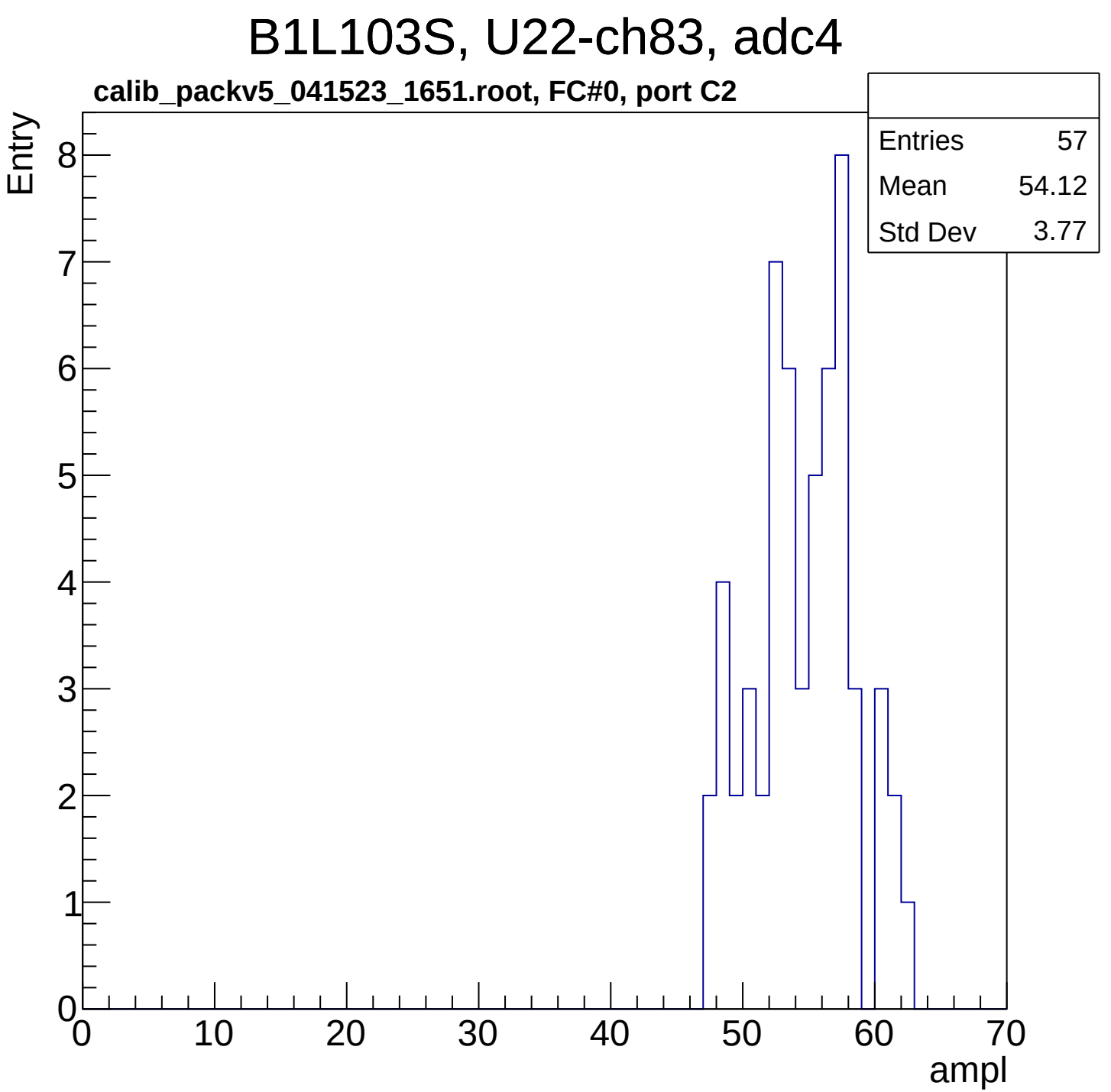
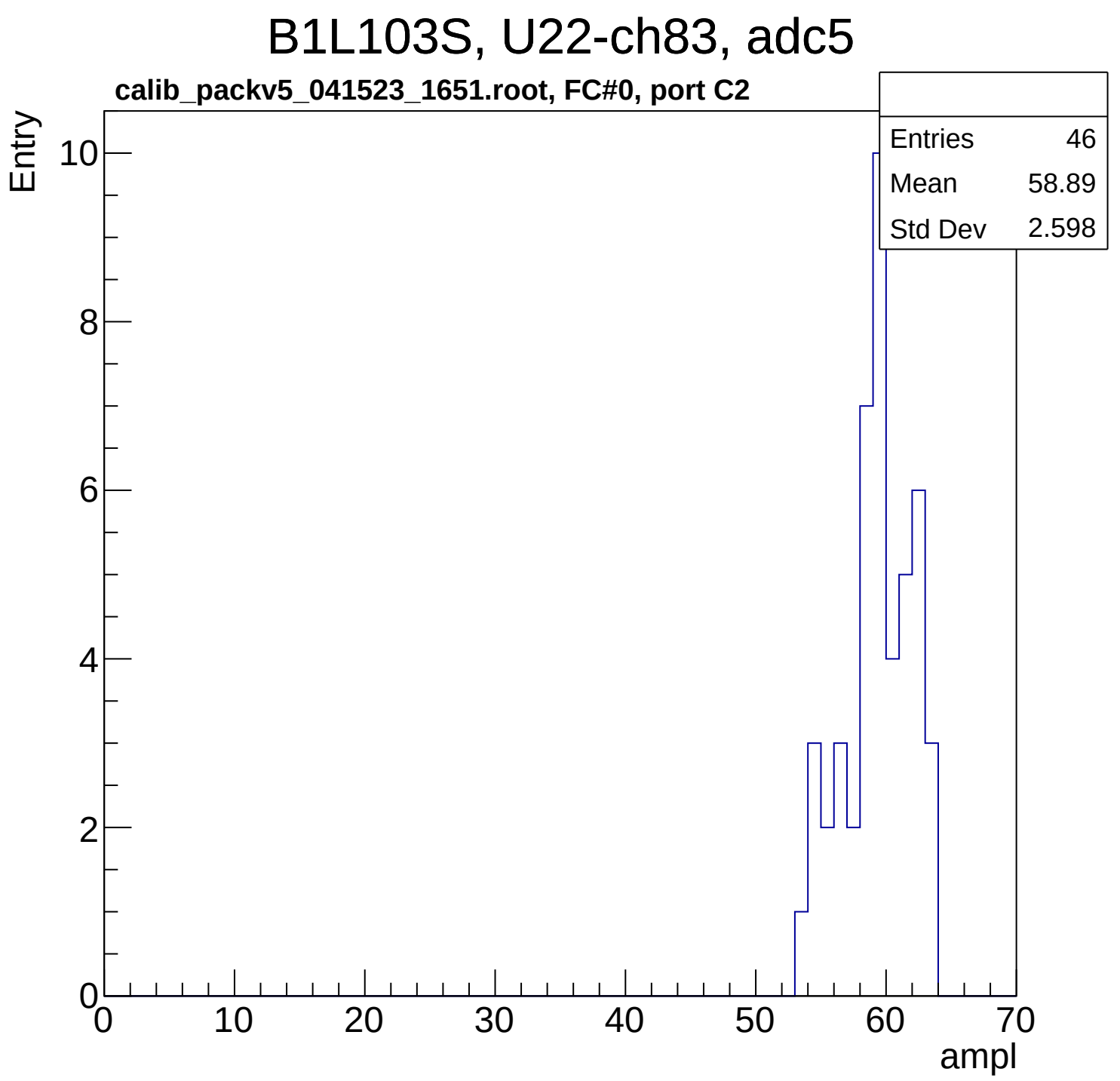
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch83, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 54.12
Std Dev 3.77
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch83, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 58.89
Std Dev 2.598
Entry
0
2
4
6
8
10
0
10
20
30
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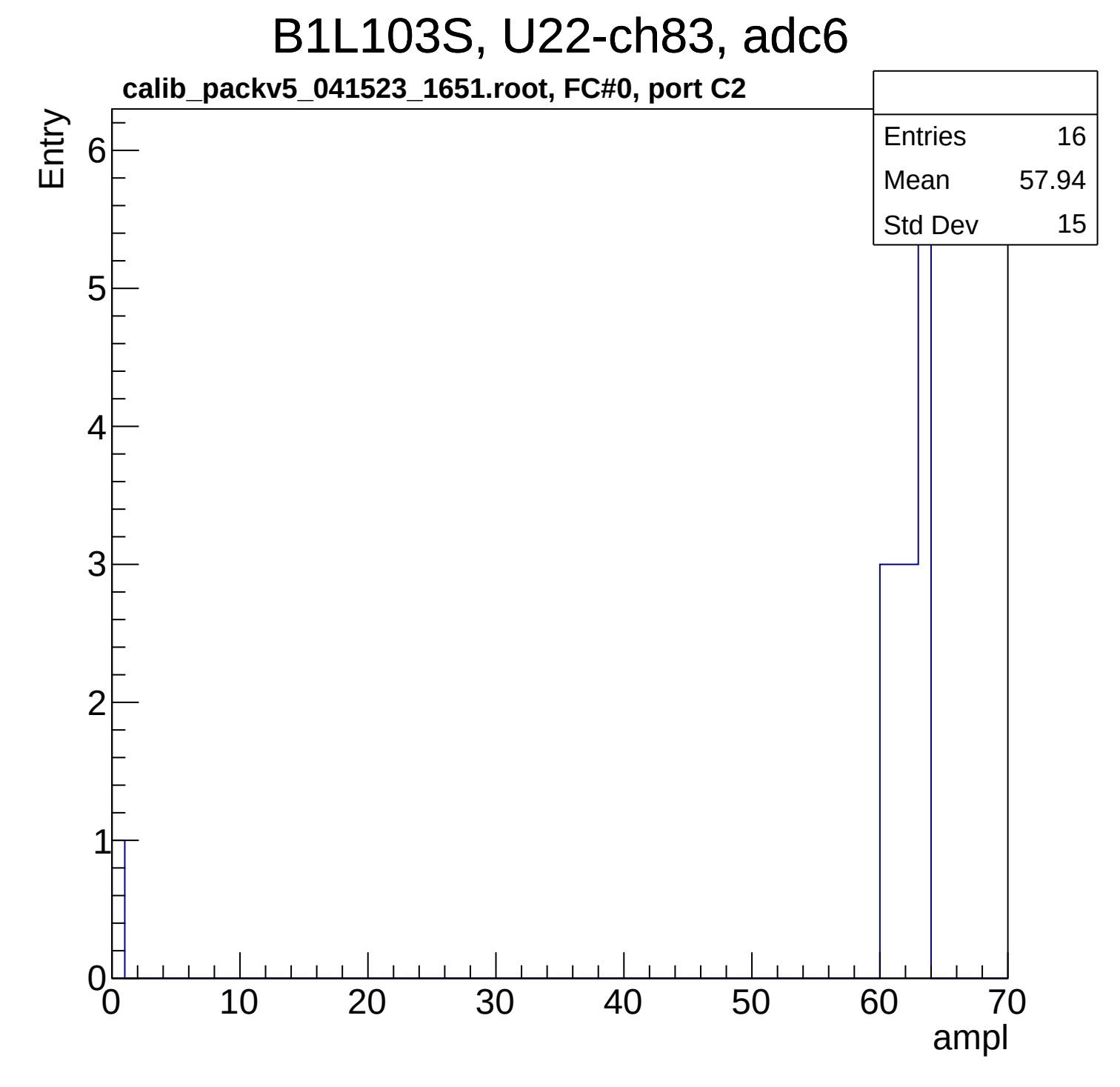
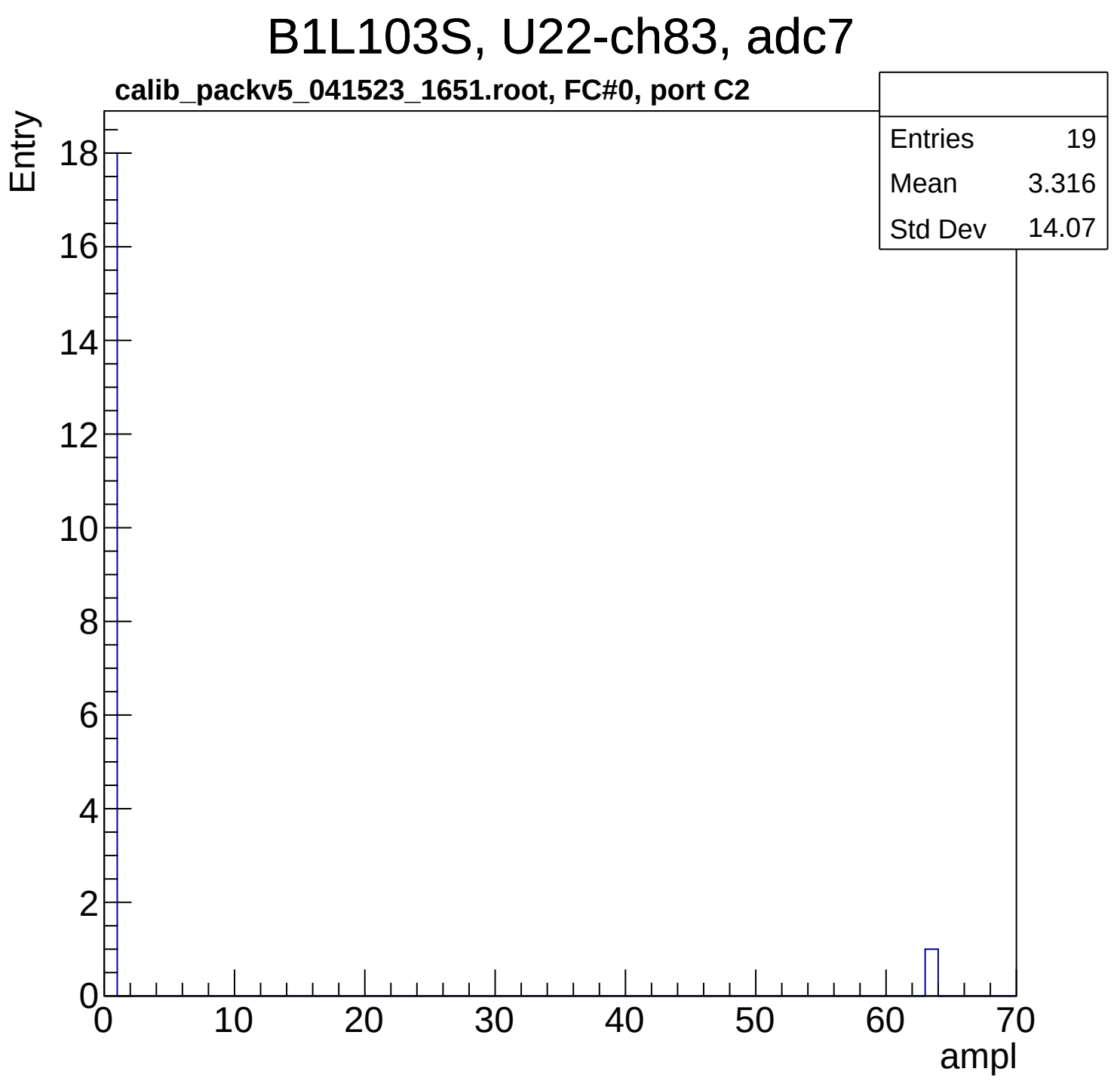
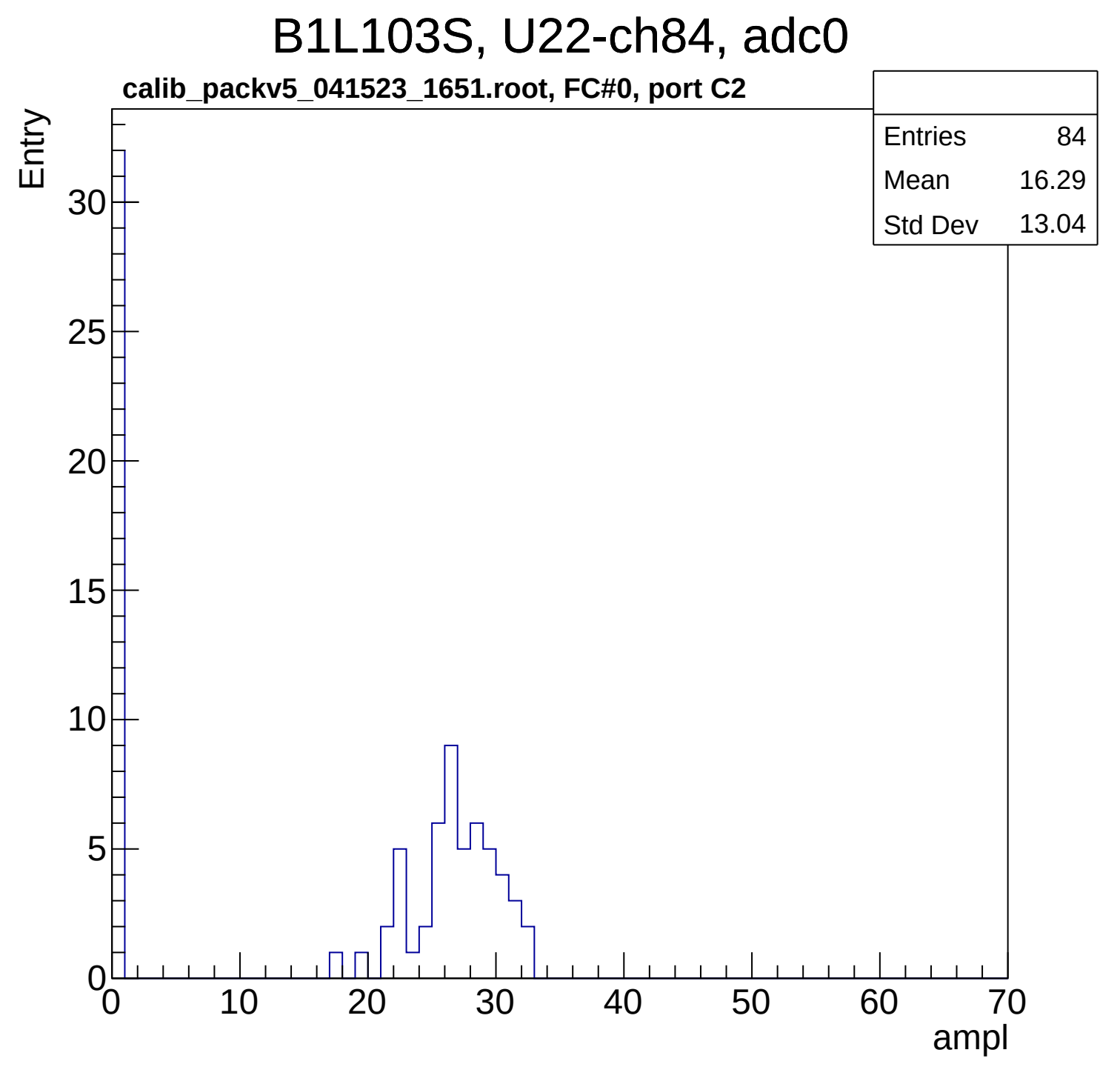
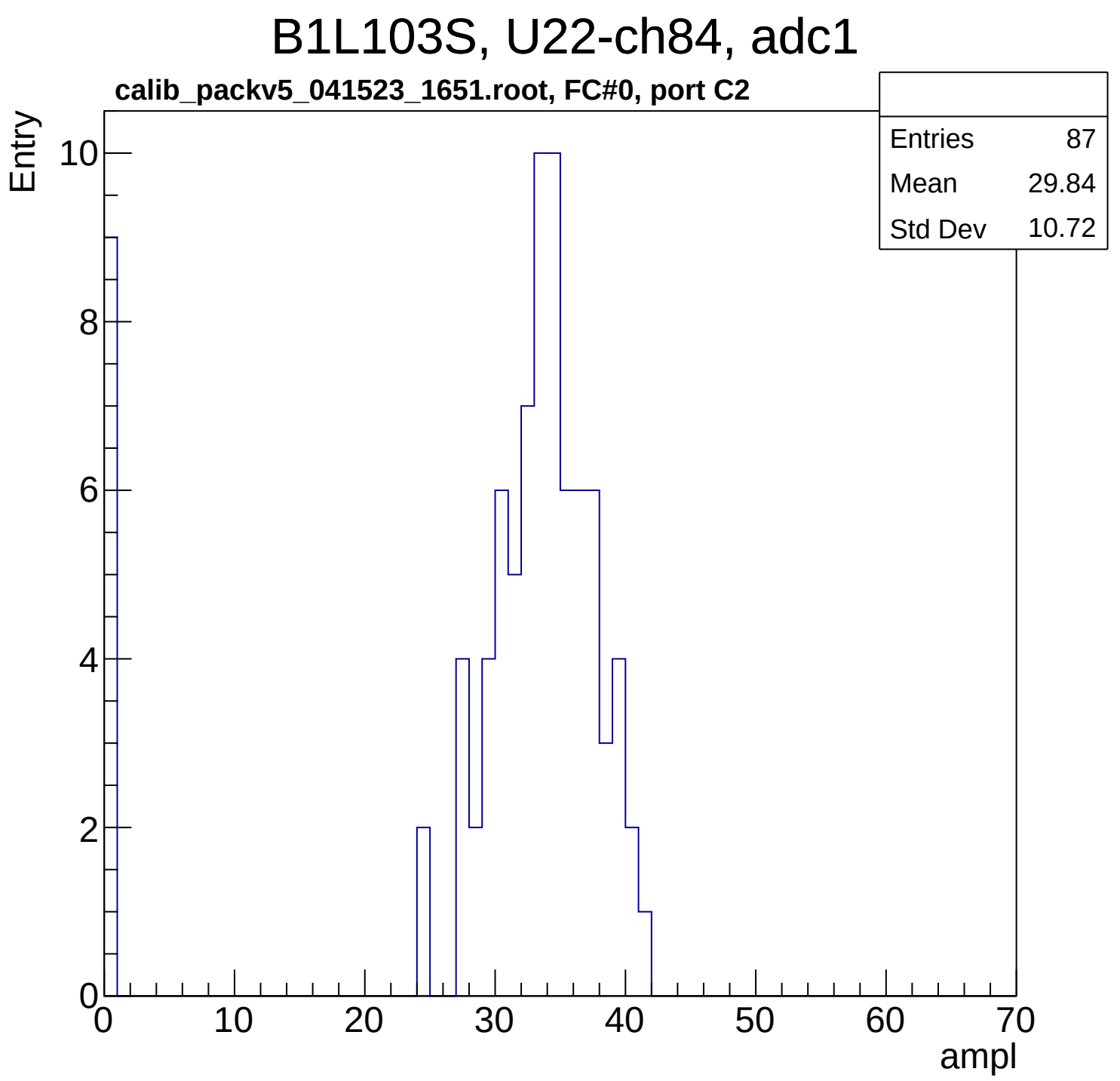
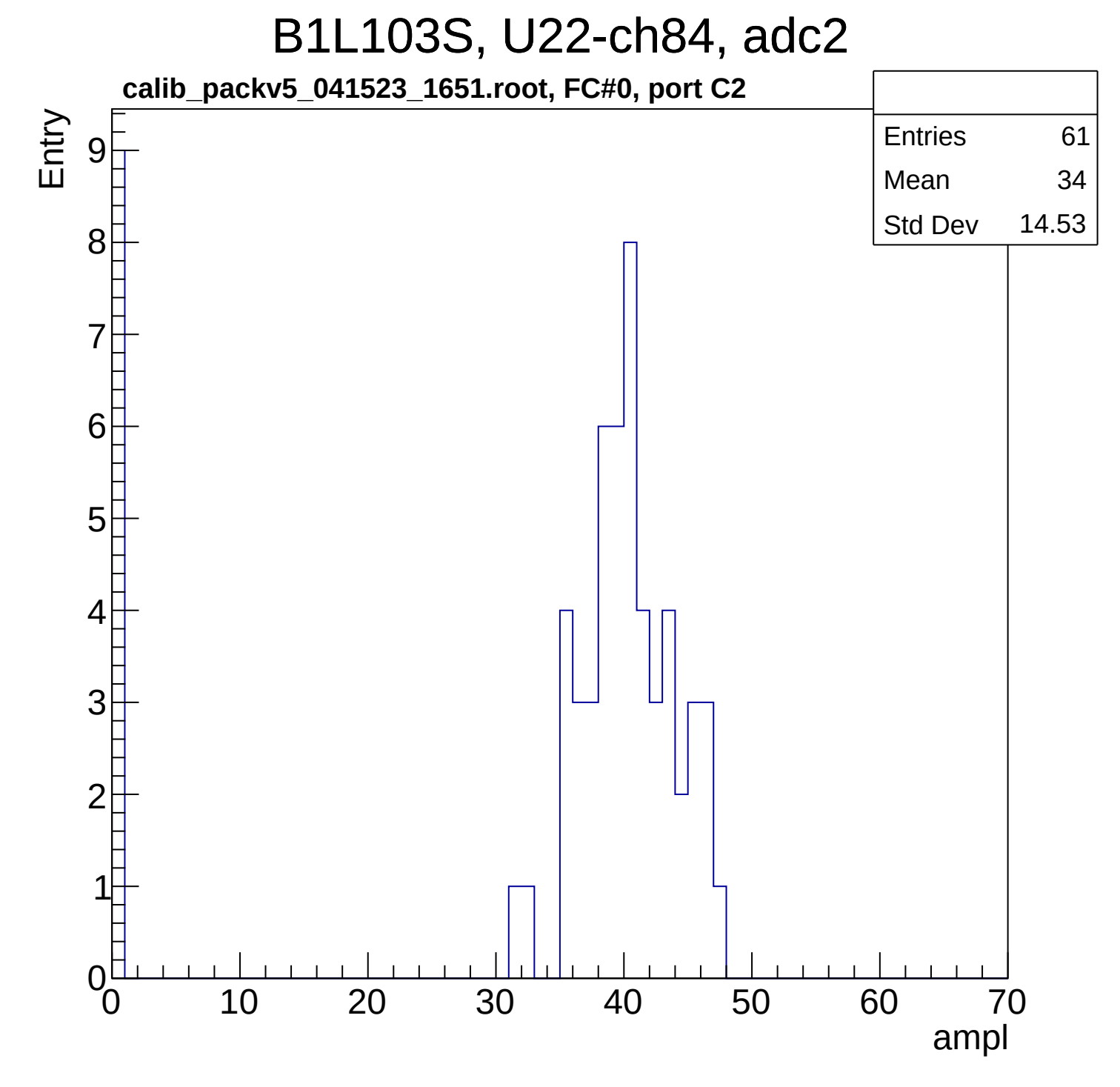
50
60
70
ampl

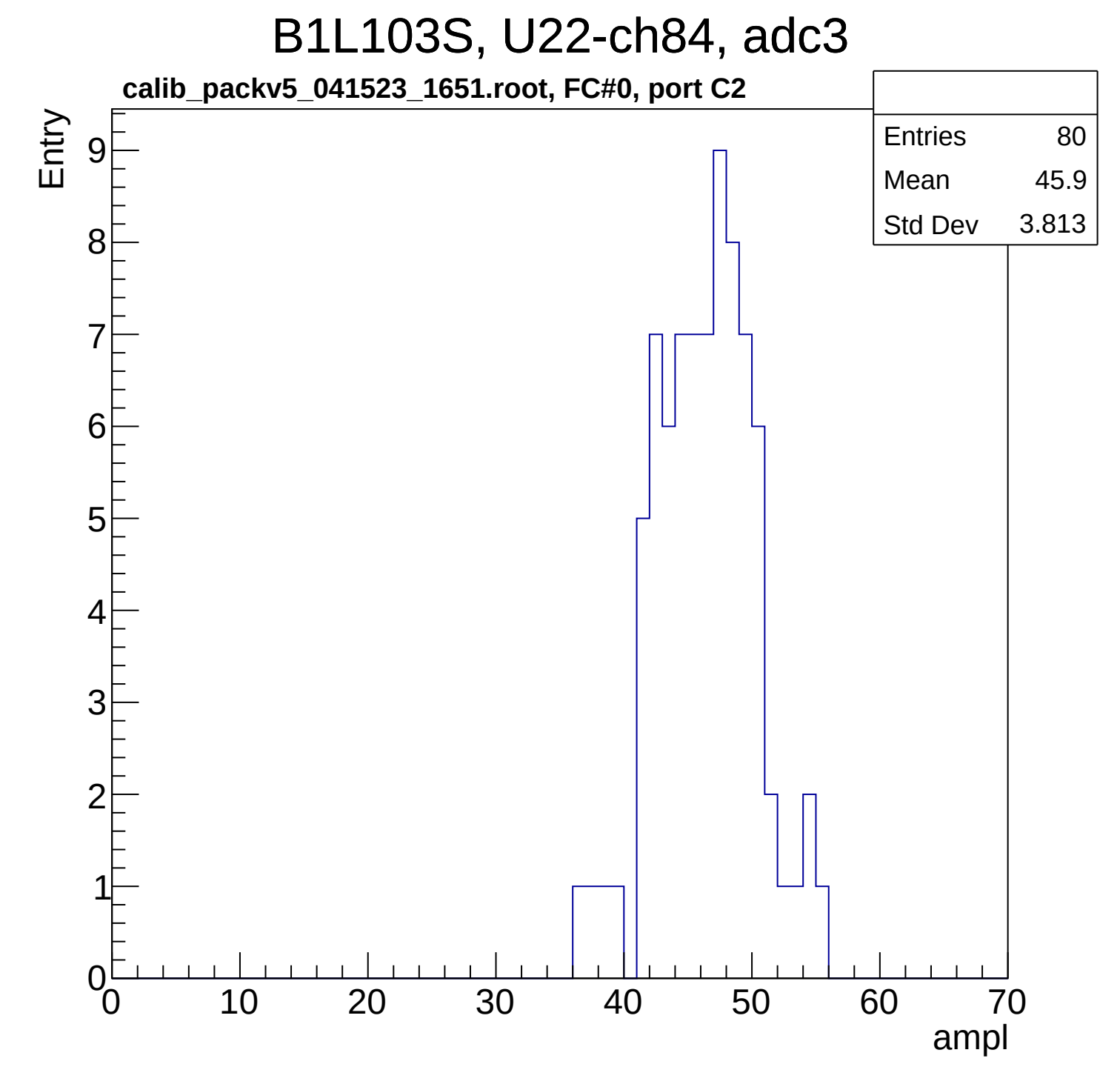

B1L103S, U22-ch83, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 57.94
Std Dev 15
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

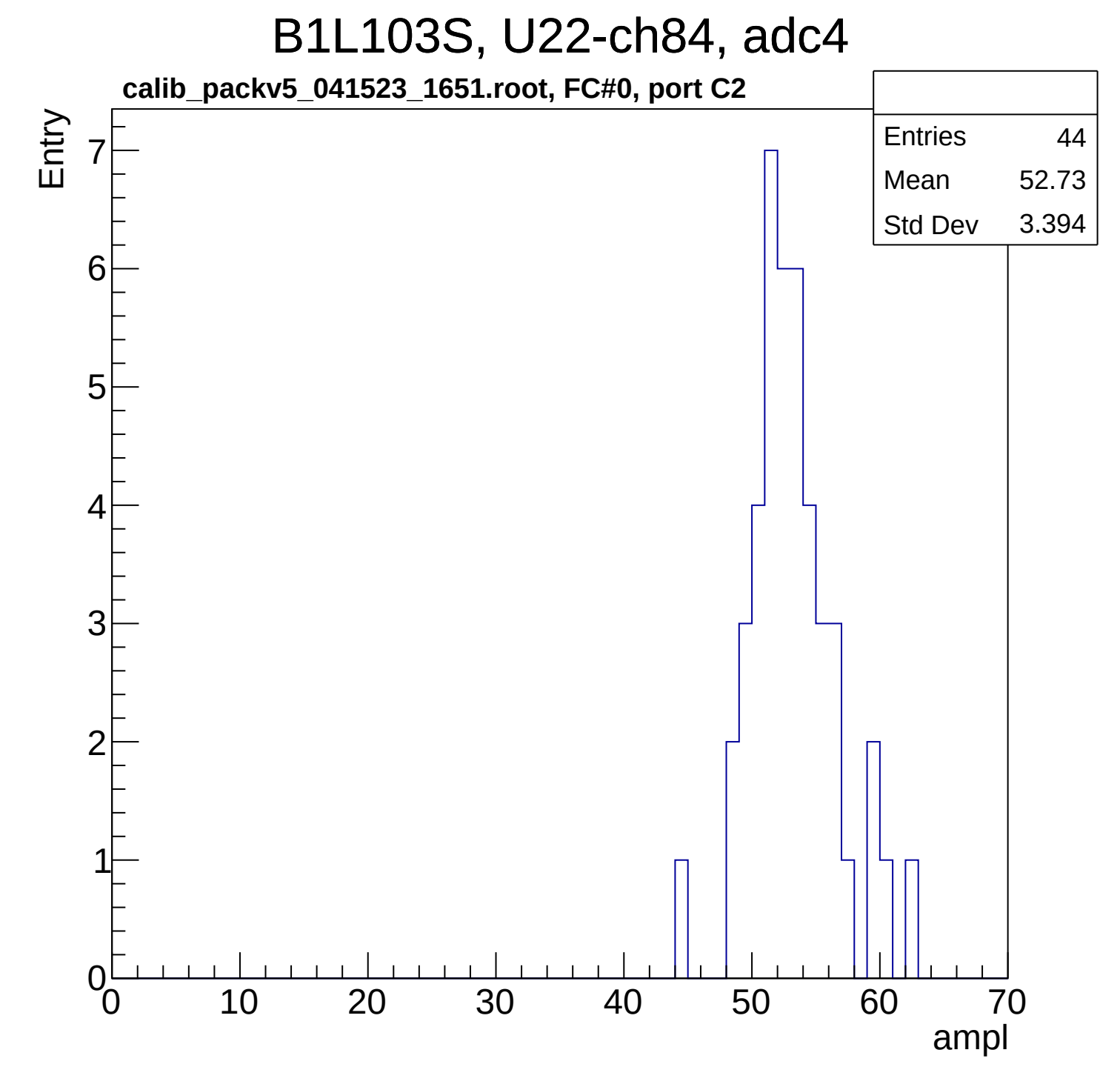

B1L103S, U22-ch83, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.316
Std Dev 14.07
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch84, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 16.29
Std Dev 13.04
Entry
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch84, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 29.84
Std Dev 10.72
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U22-ch84, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 34
Std Dev 14.53
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch84, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 45.9
Std Dev 3.813
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch84, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 52.73
Std Dev 3.394
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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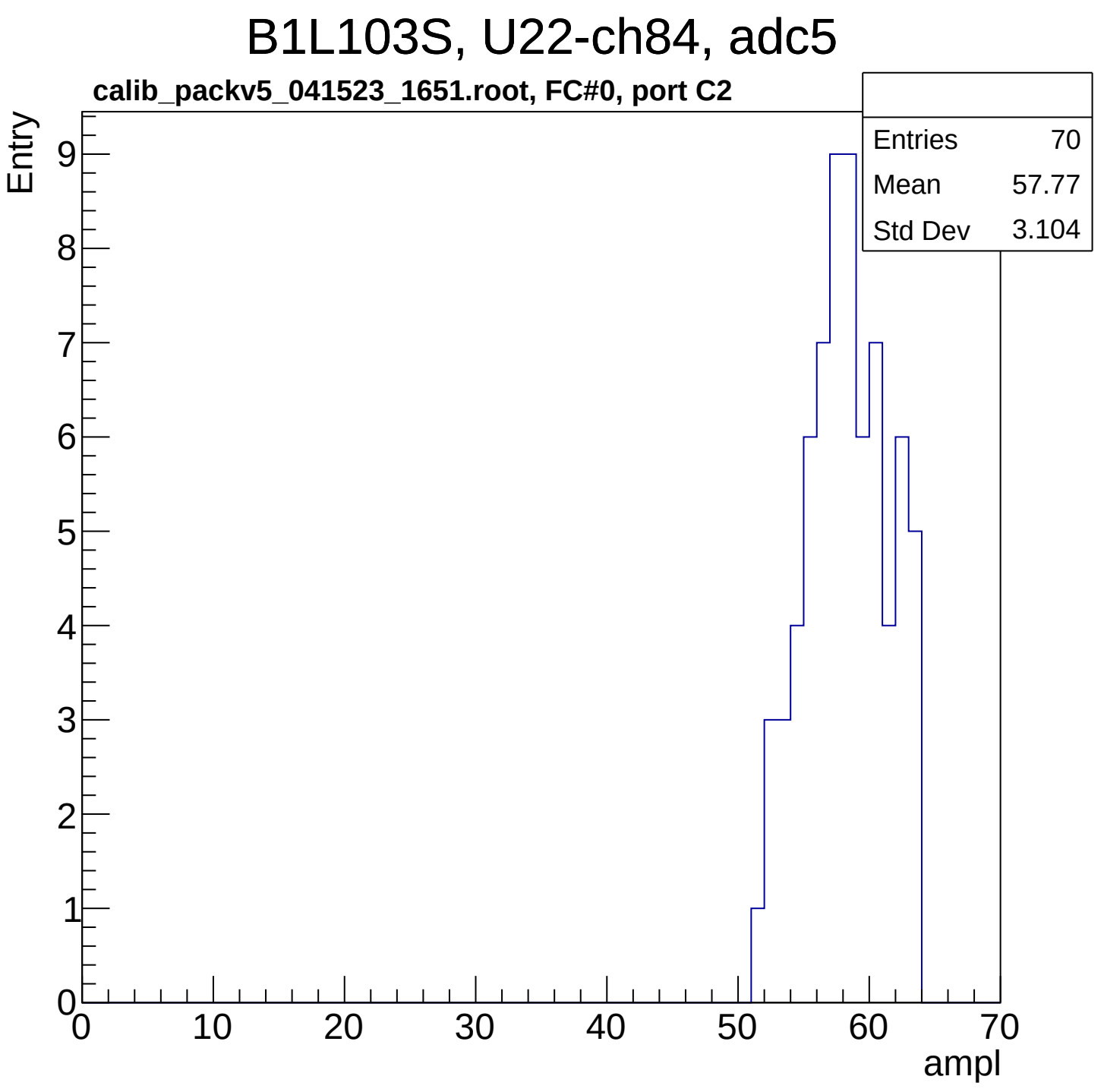
B1L103S, U22-ch84, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 57.77
Std Dev 3.104
Entry
ampl
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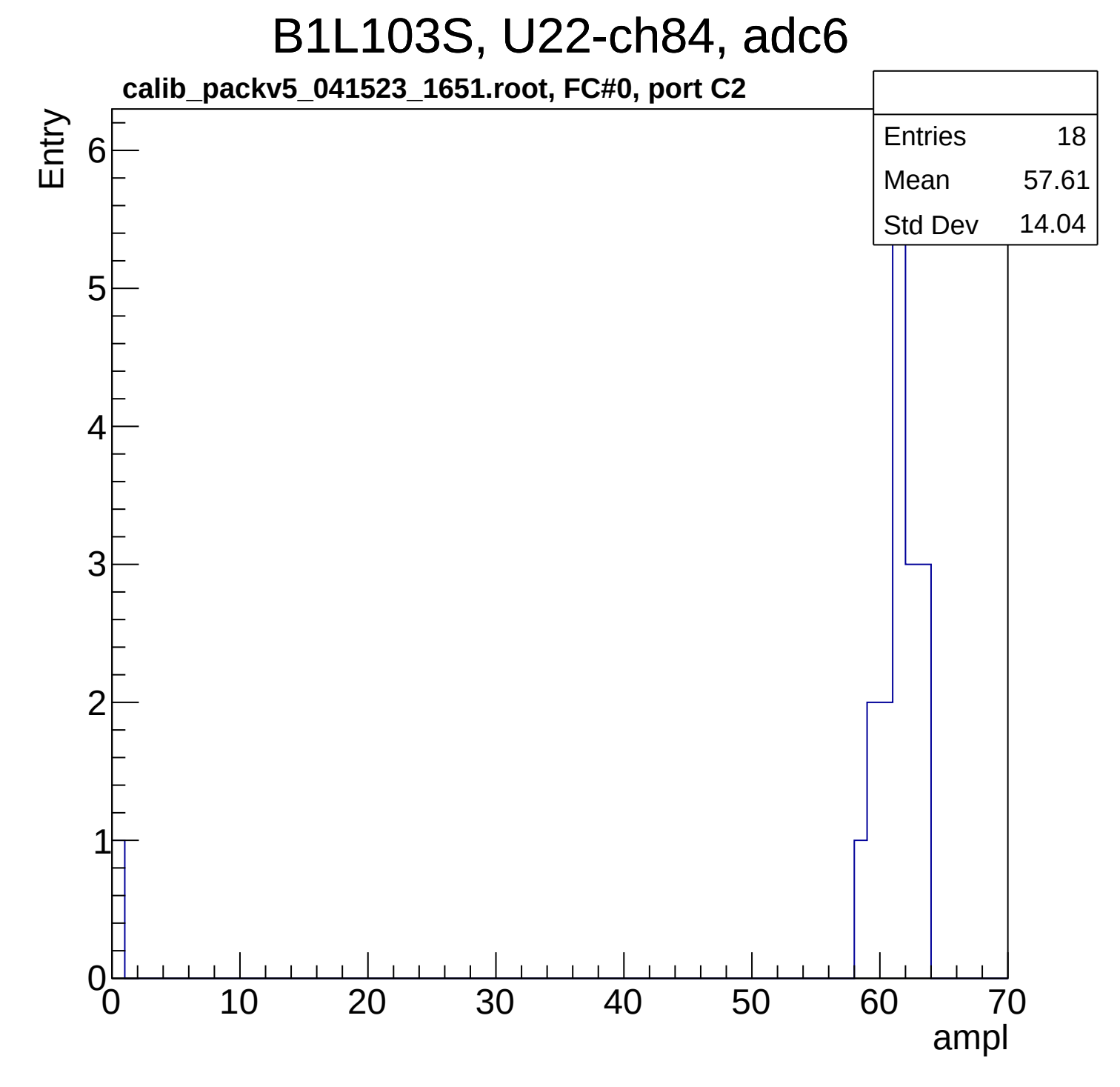
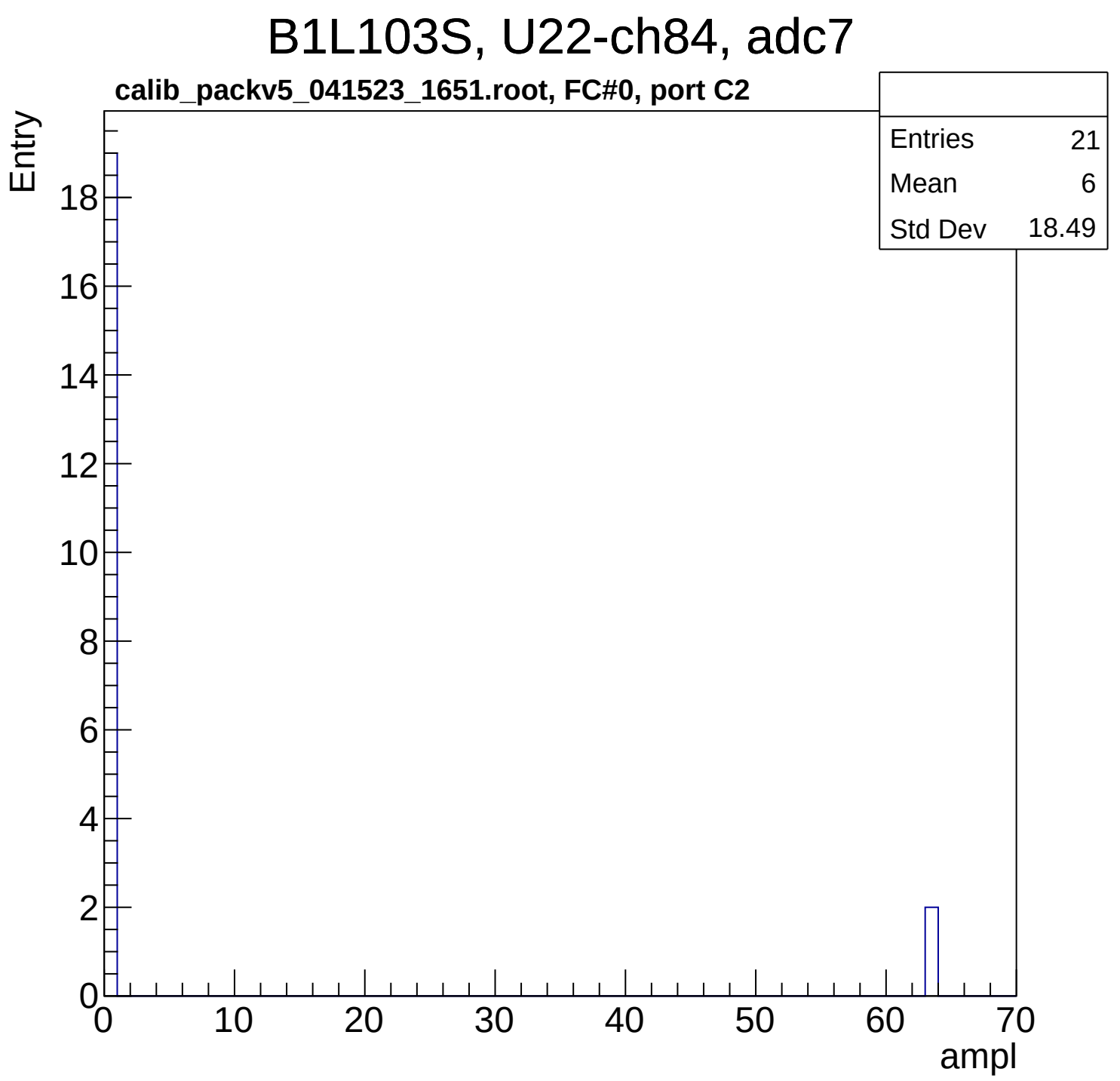
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch84, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 57.61
Std Dev 14.04
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U22-ch84, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 6
Std Dev 18.49
Entry
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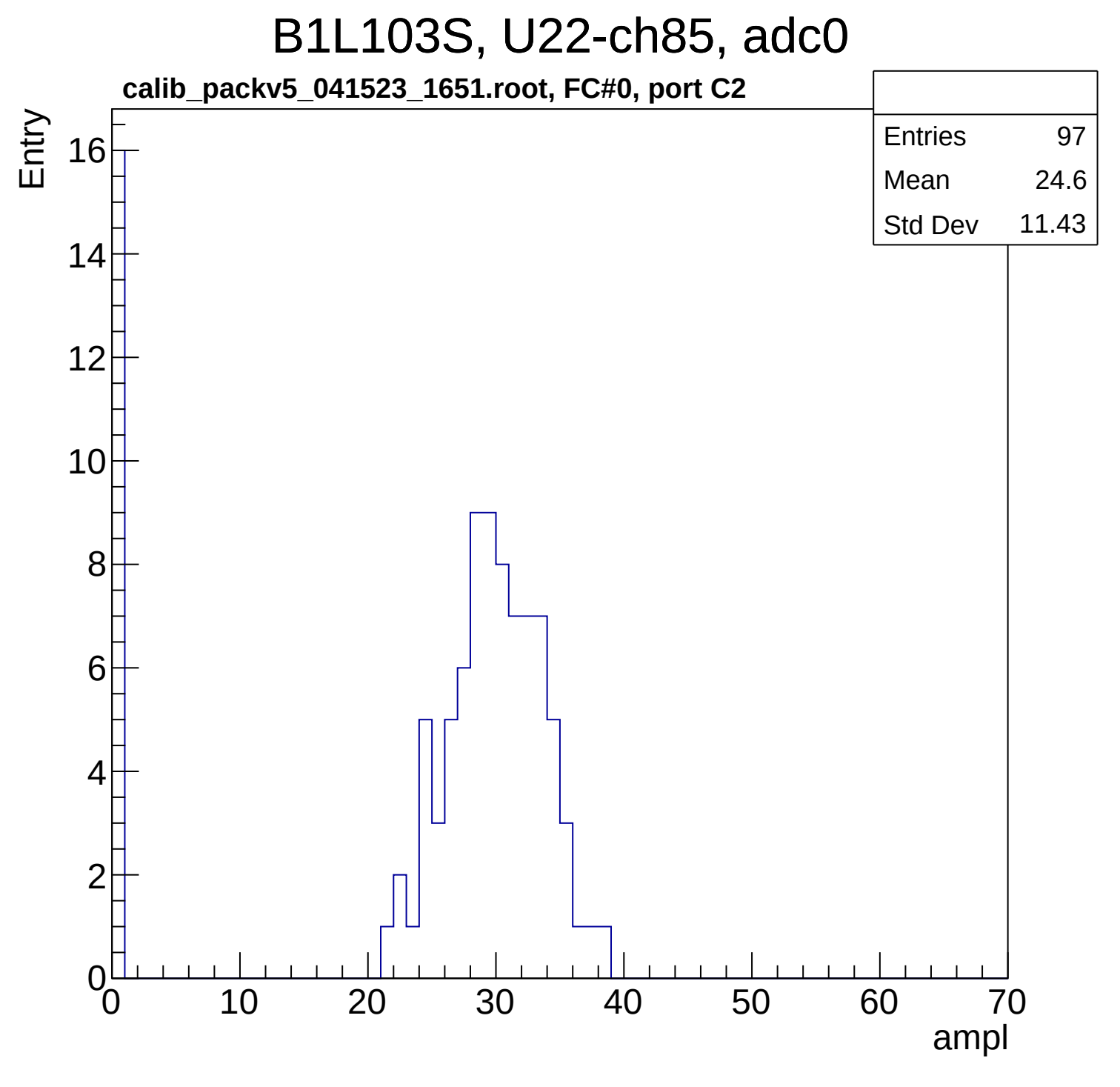
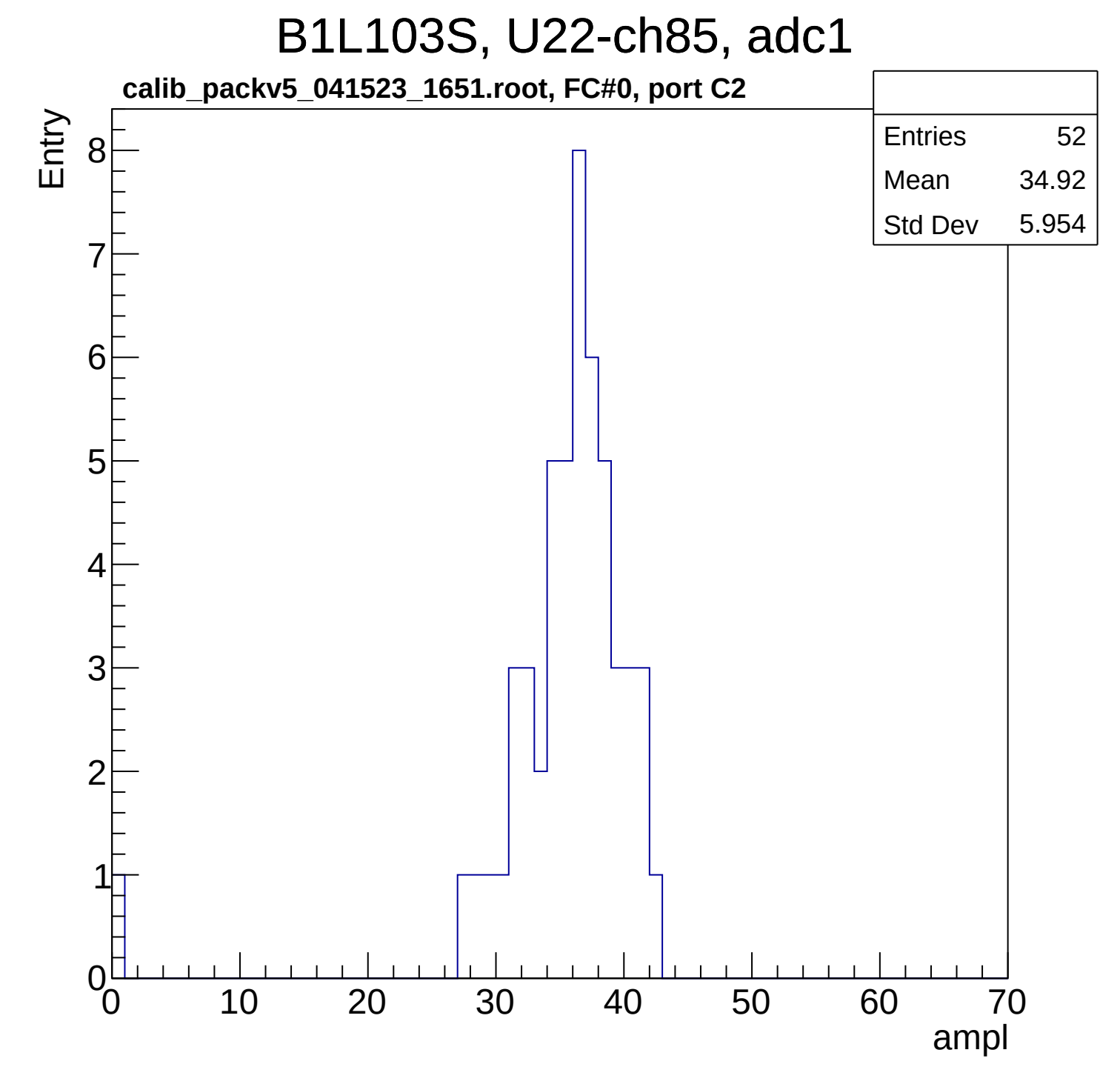
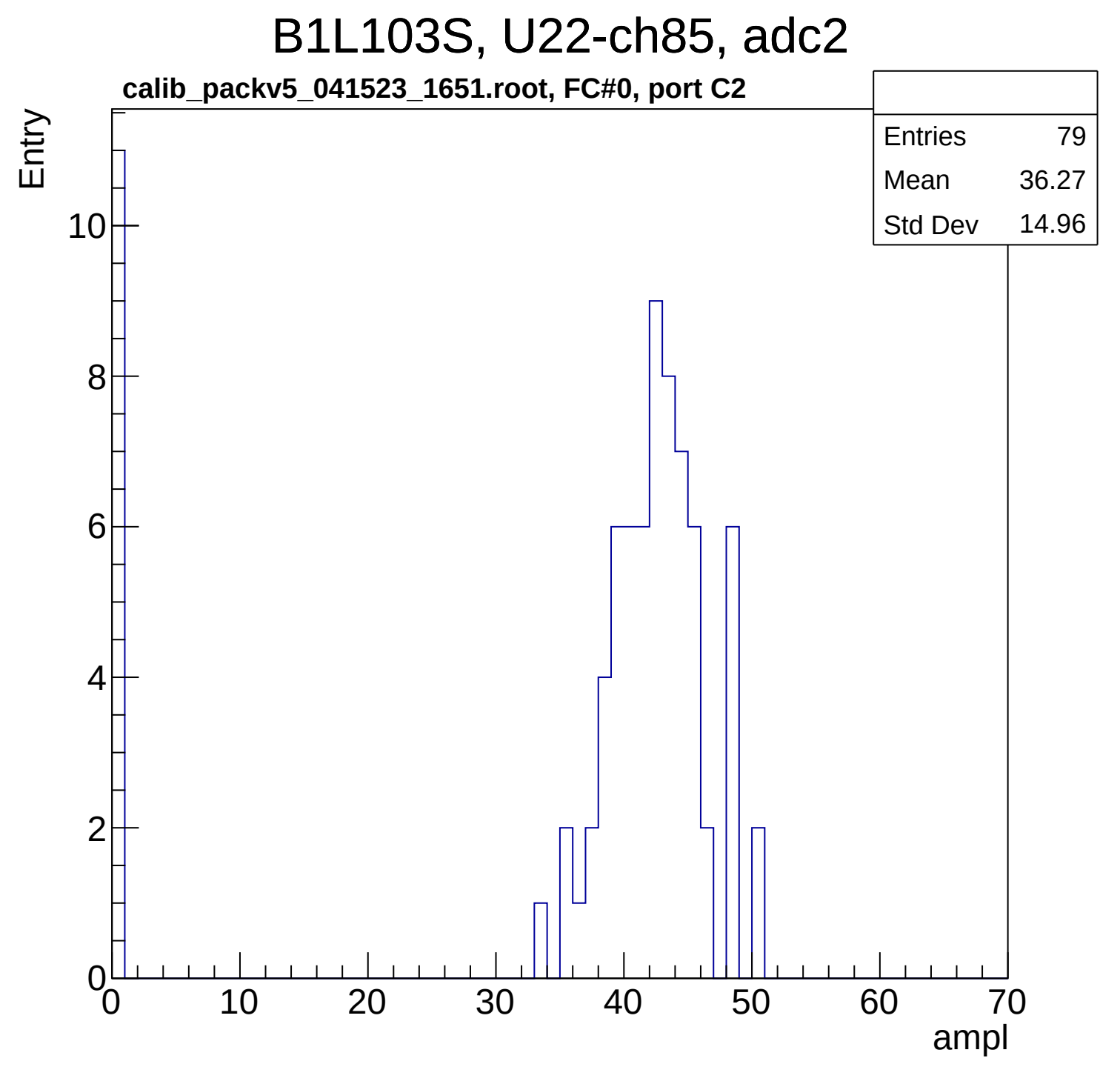
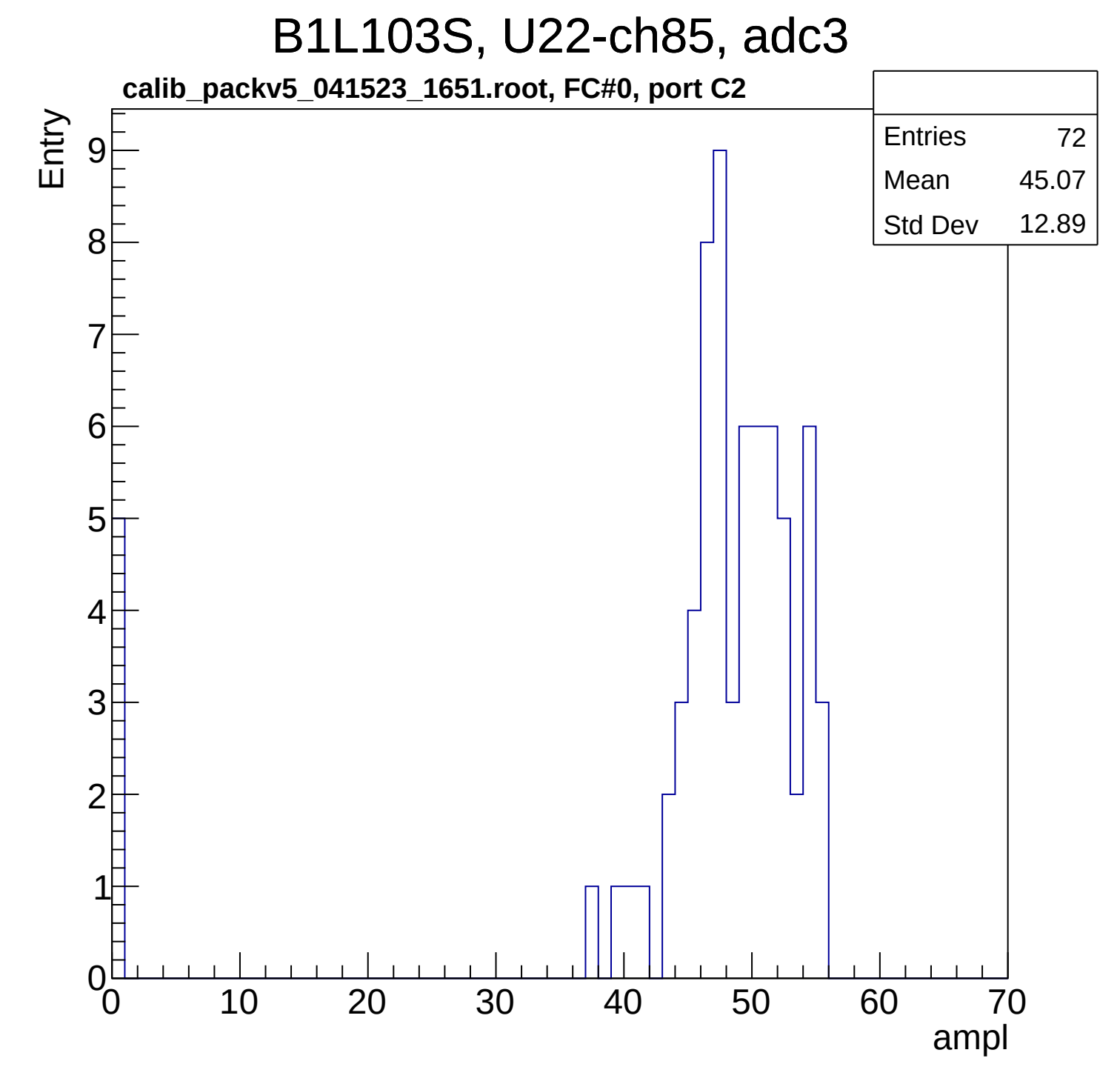
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch85, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 24.6
Std Dev 11.43
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch85, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 34.92
Std Dev 5.954
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch85, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 36.27
Std Dev 14.96
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch85, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 45.07
Std Dev 12.89
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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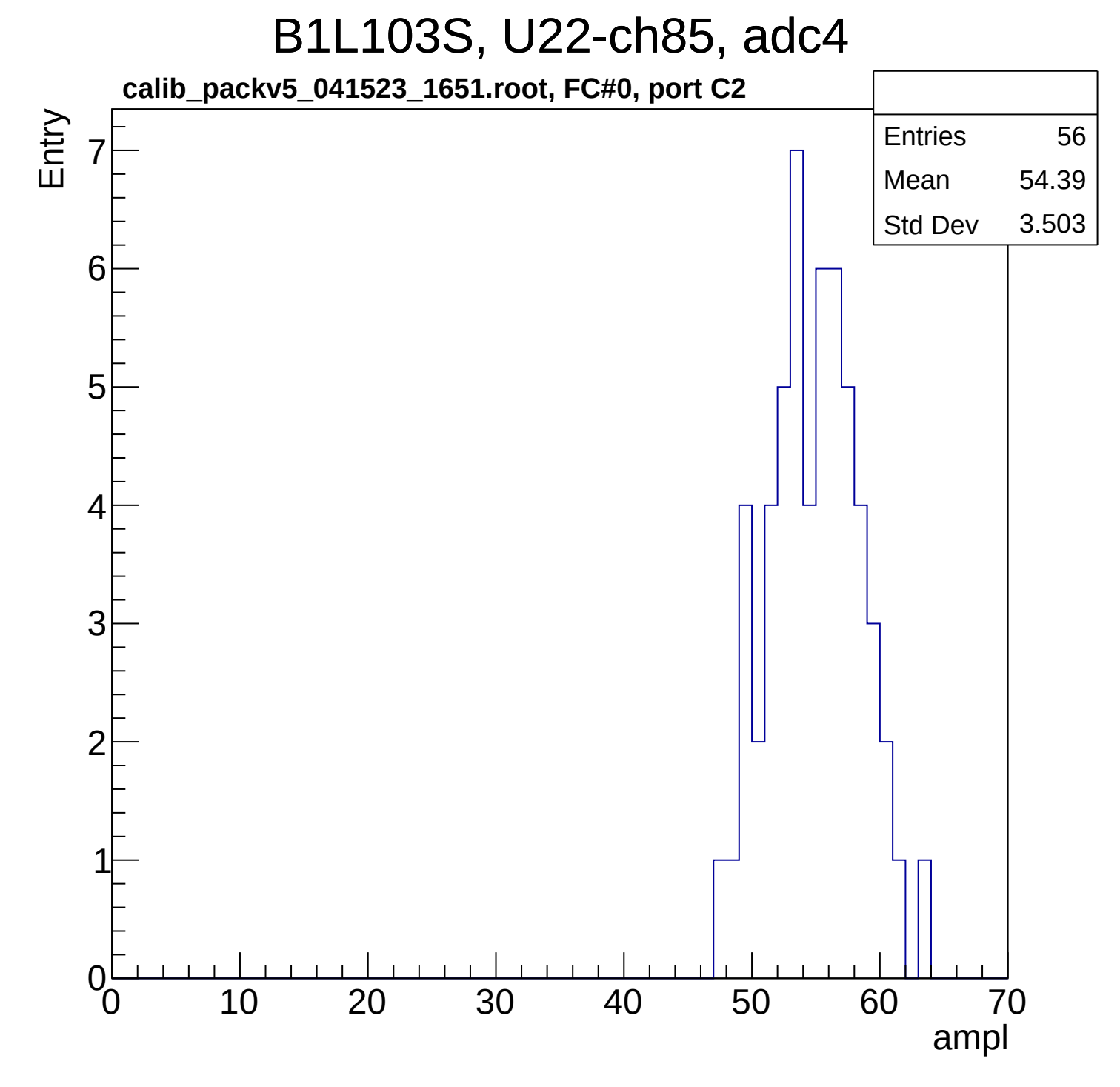
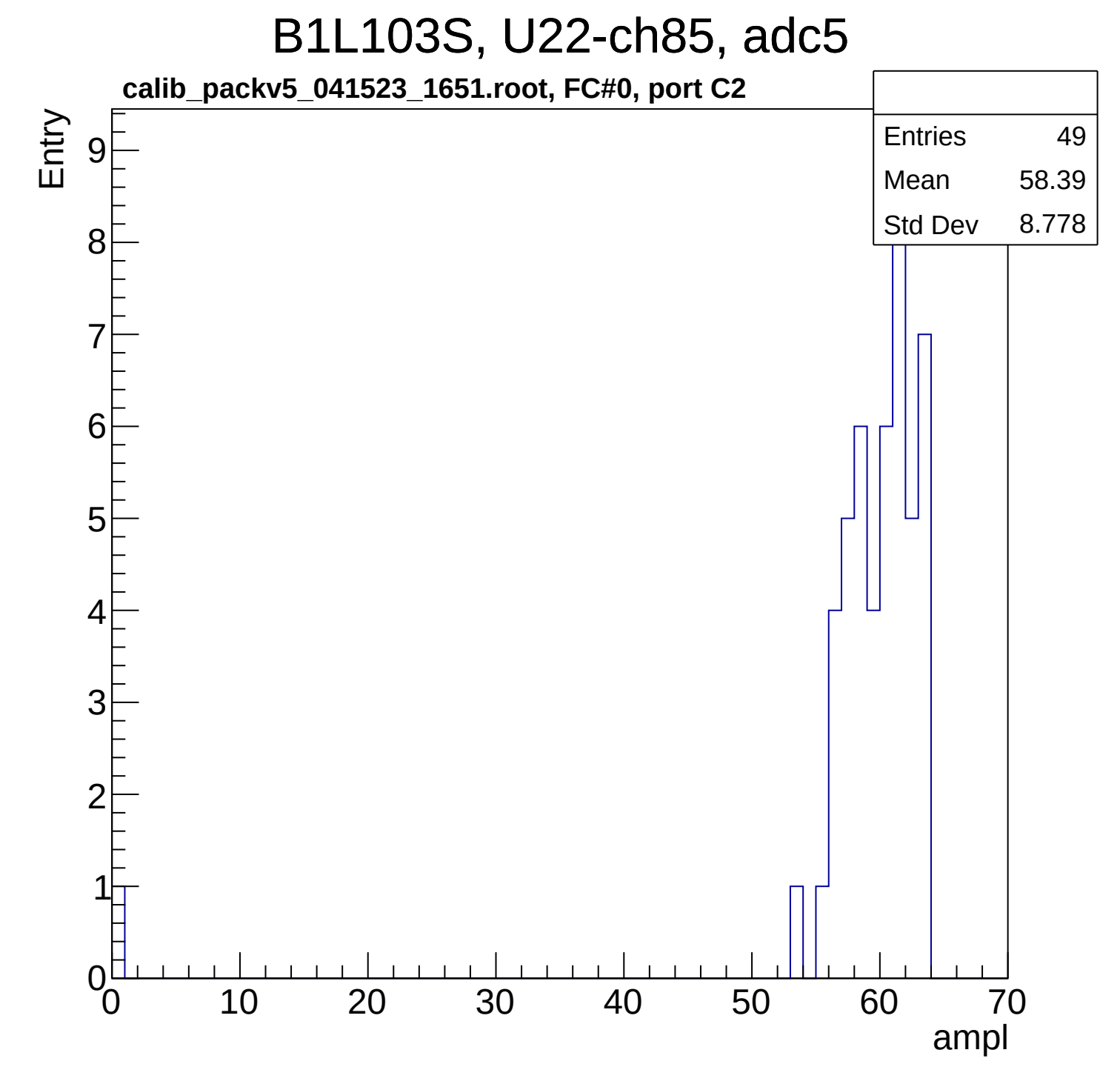
40
50
60
70


B1L103S, U22-ch85, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 54.39
Std Dev 3.503
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U22-ch85, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 58.39
Std Dev 8.778
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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60
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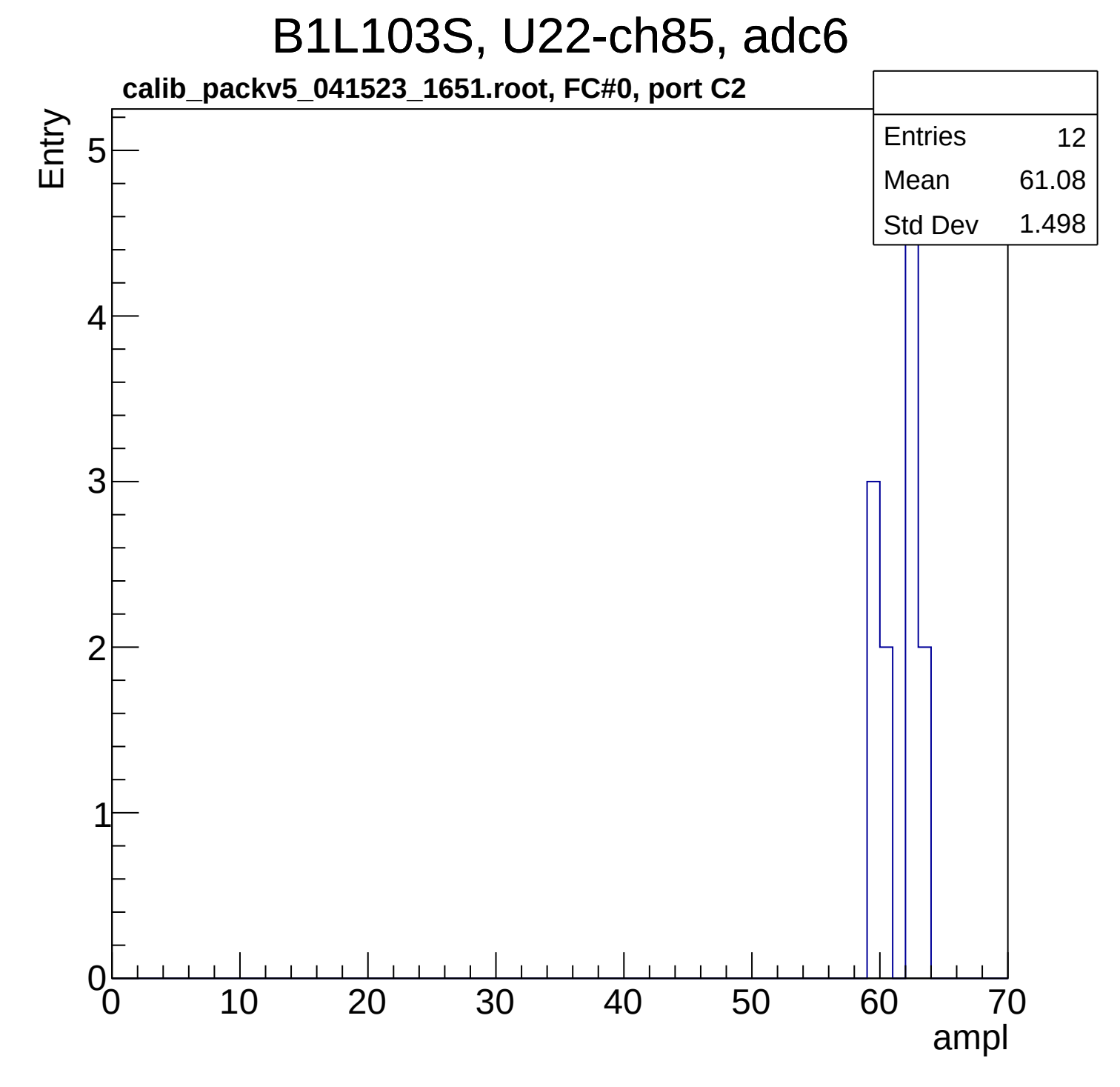
B1L103S, U22-ch85, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.08
Std Dev 1.498
Entry
ampl
0
1
2
3
4
5
0
10
20
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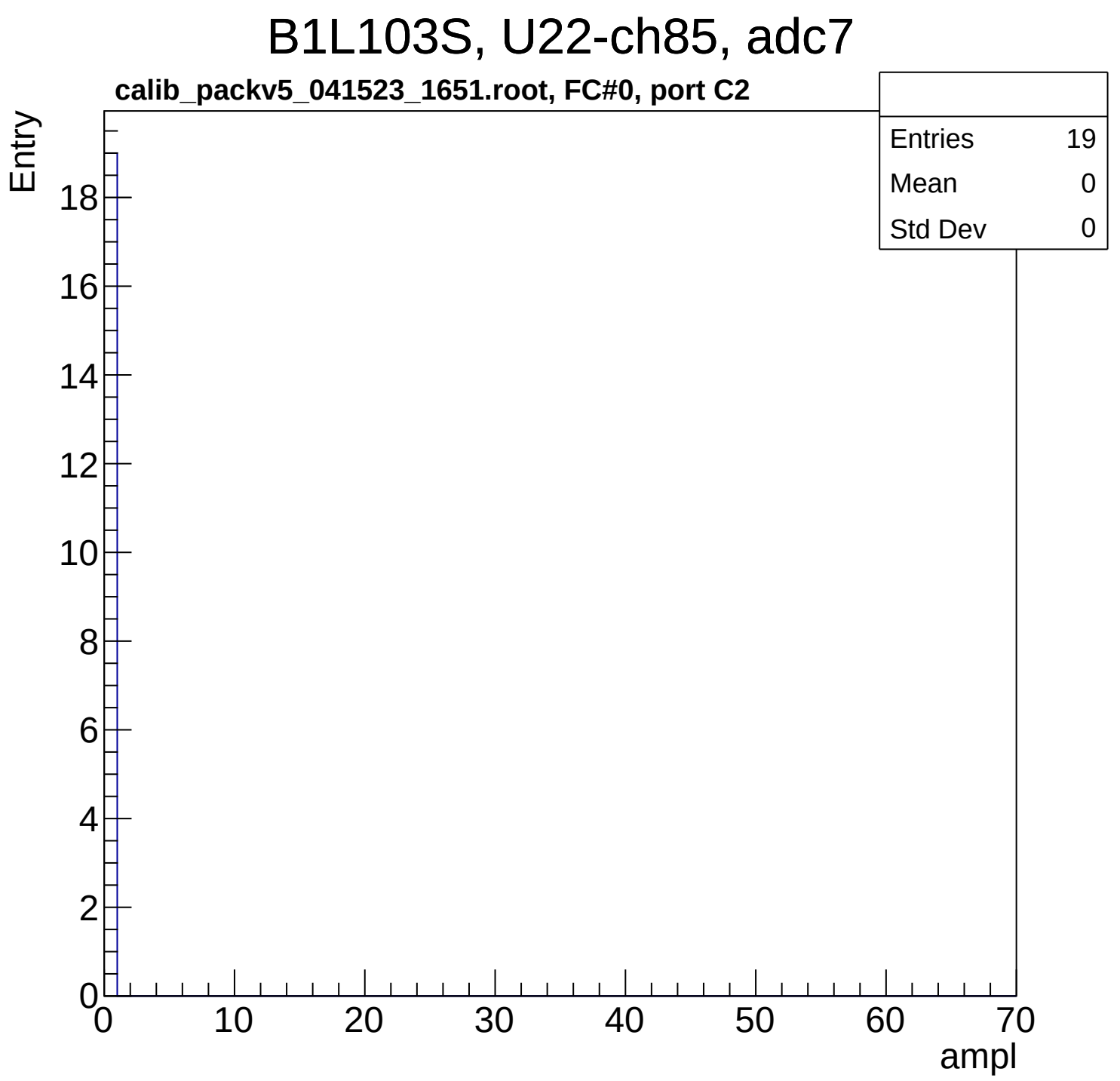
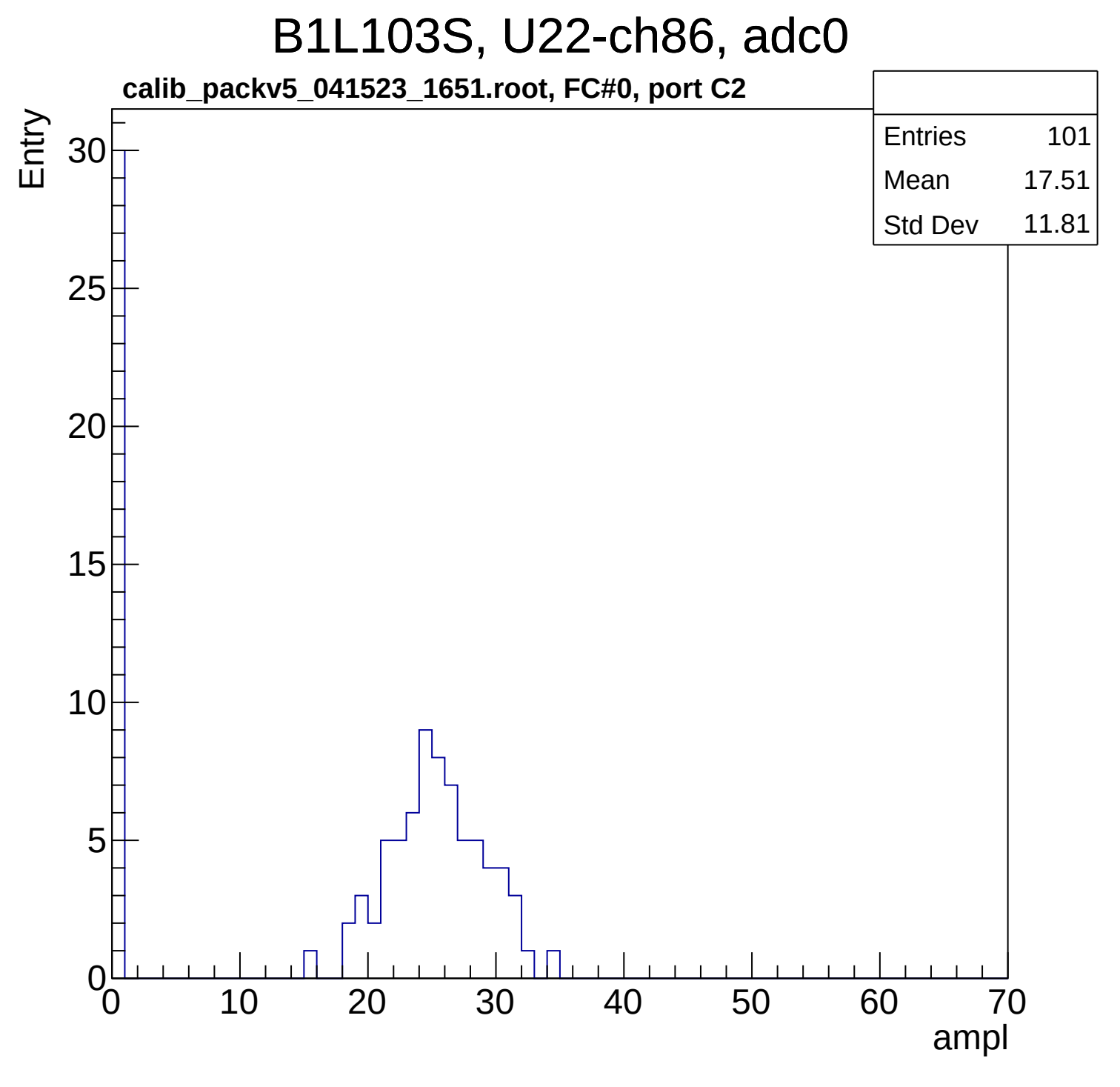
40
50
60
70


B1L103S, U22-ch85, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch86, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 101
Mean 17.51
Std Dev 11.81
Entry
ampl
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5
10
15
20
25
30
0
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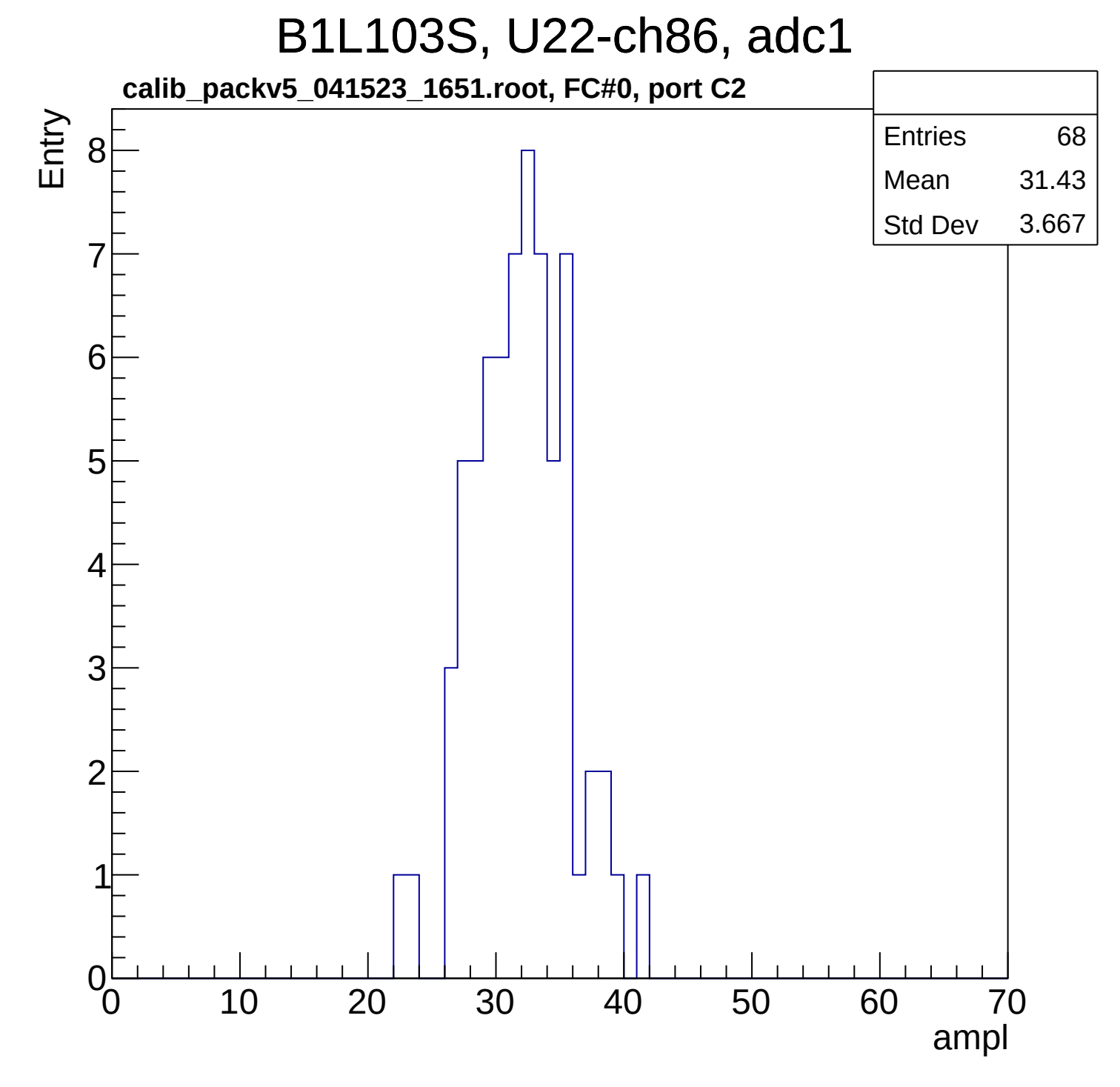
20
30
40
50
60
70


B1L103S, U22-ch86, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 31.43
Std Dev 3.667
Entry
ampl
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2
3
4
5
6
7
8
0
10
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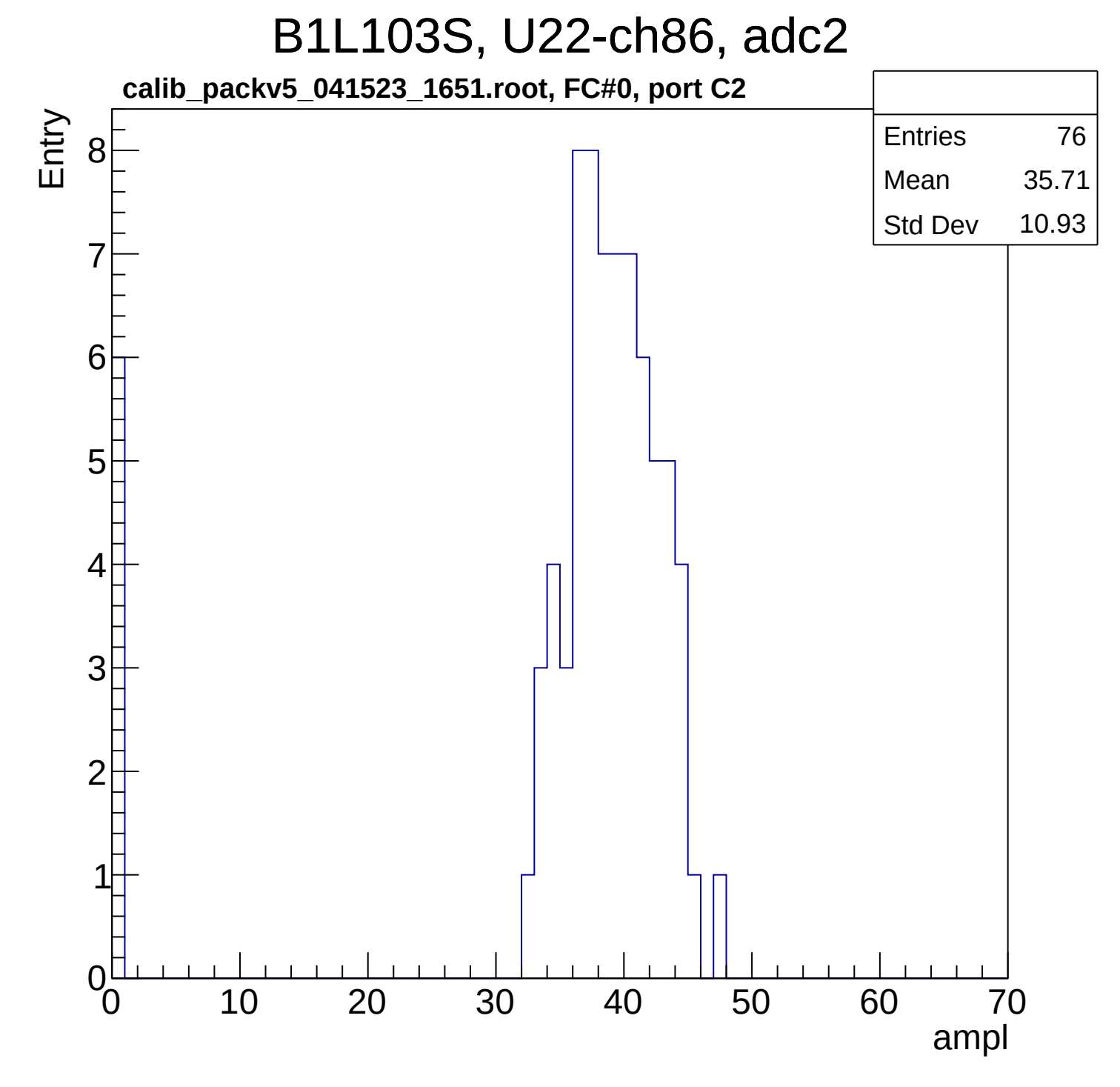
40
50
60
70


B1L103S, U22-ch86, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 35.71
Std Dev 10.93
Entry
ampl
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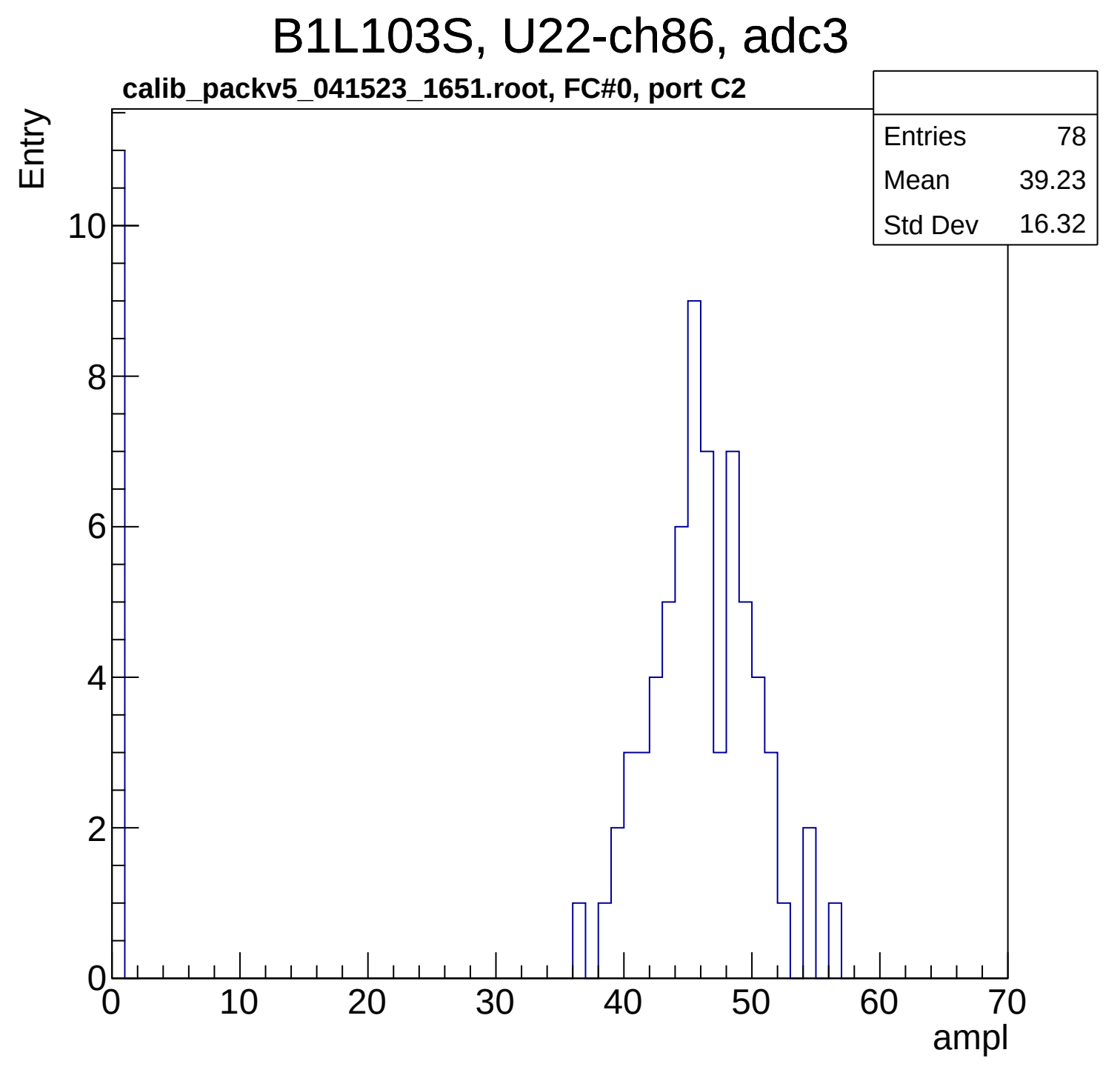
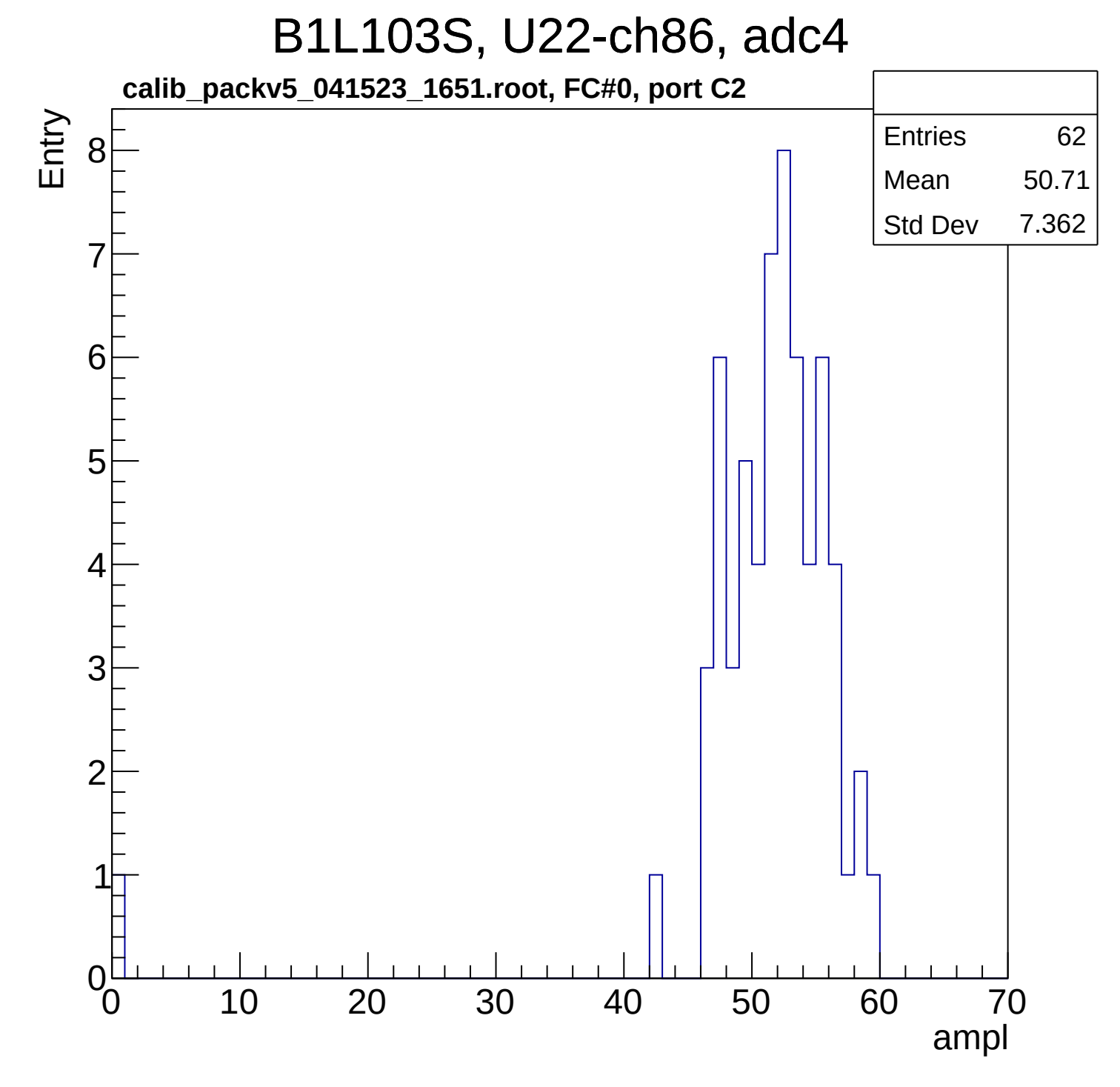
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch86, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 39.23
Std Dev 16.32
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U22-ch86, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 50.71
Std Dev 7.362
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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60
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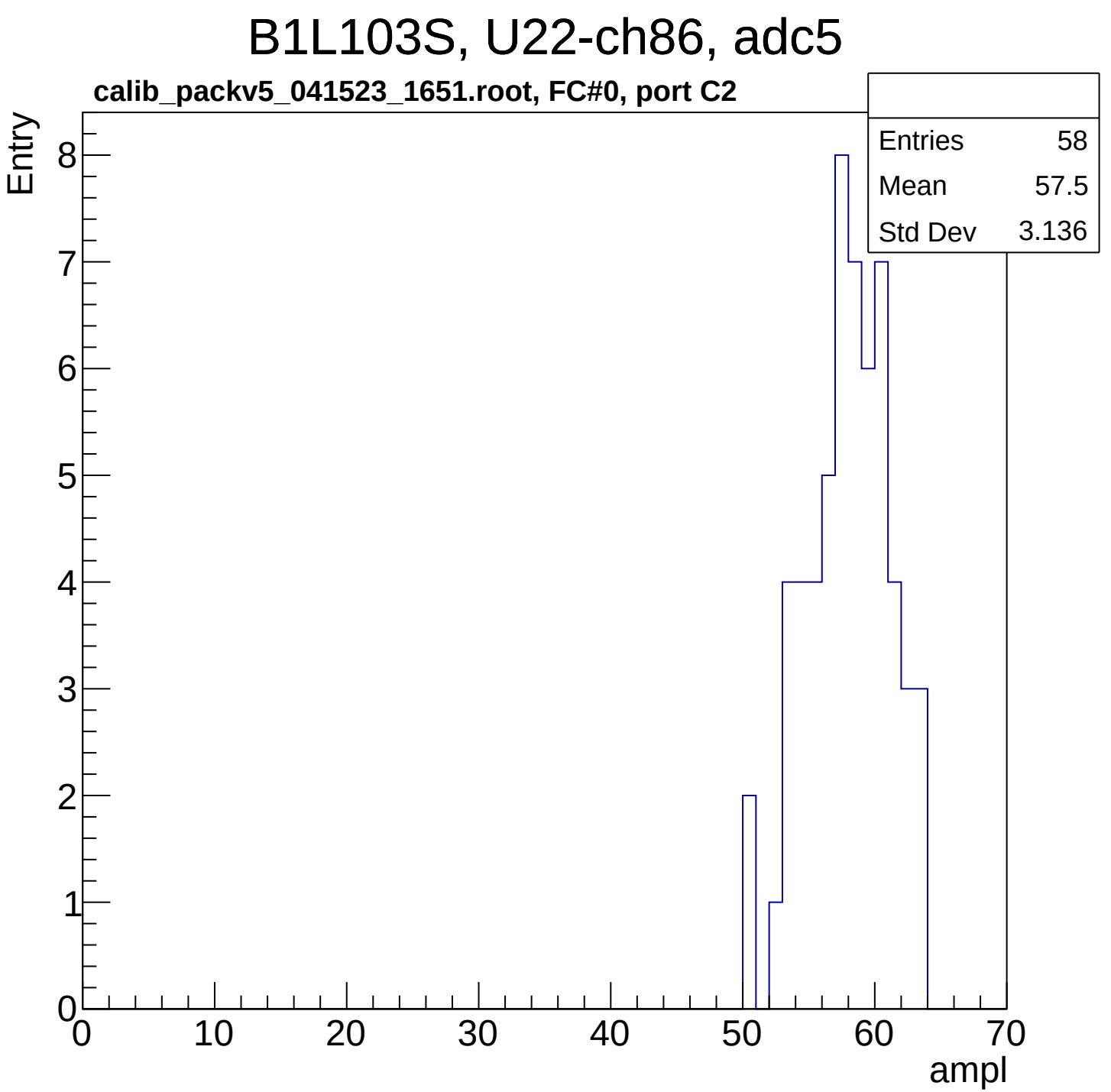
B1L103S, U22-ch86, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 57.5
Std Dev 3.136
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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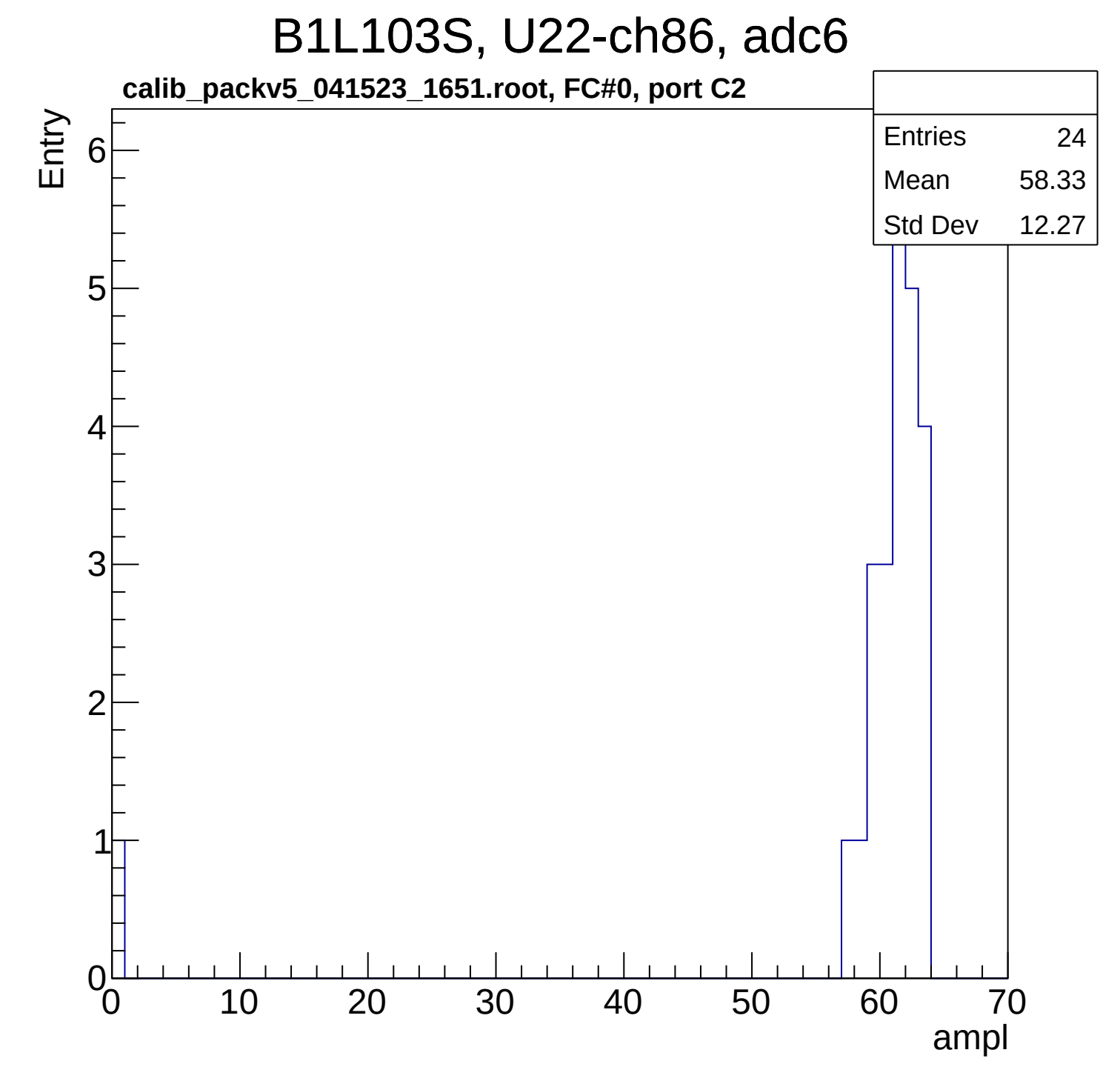
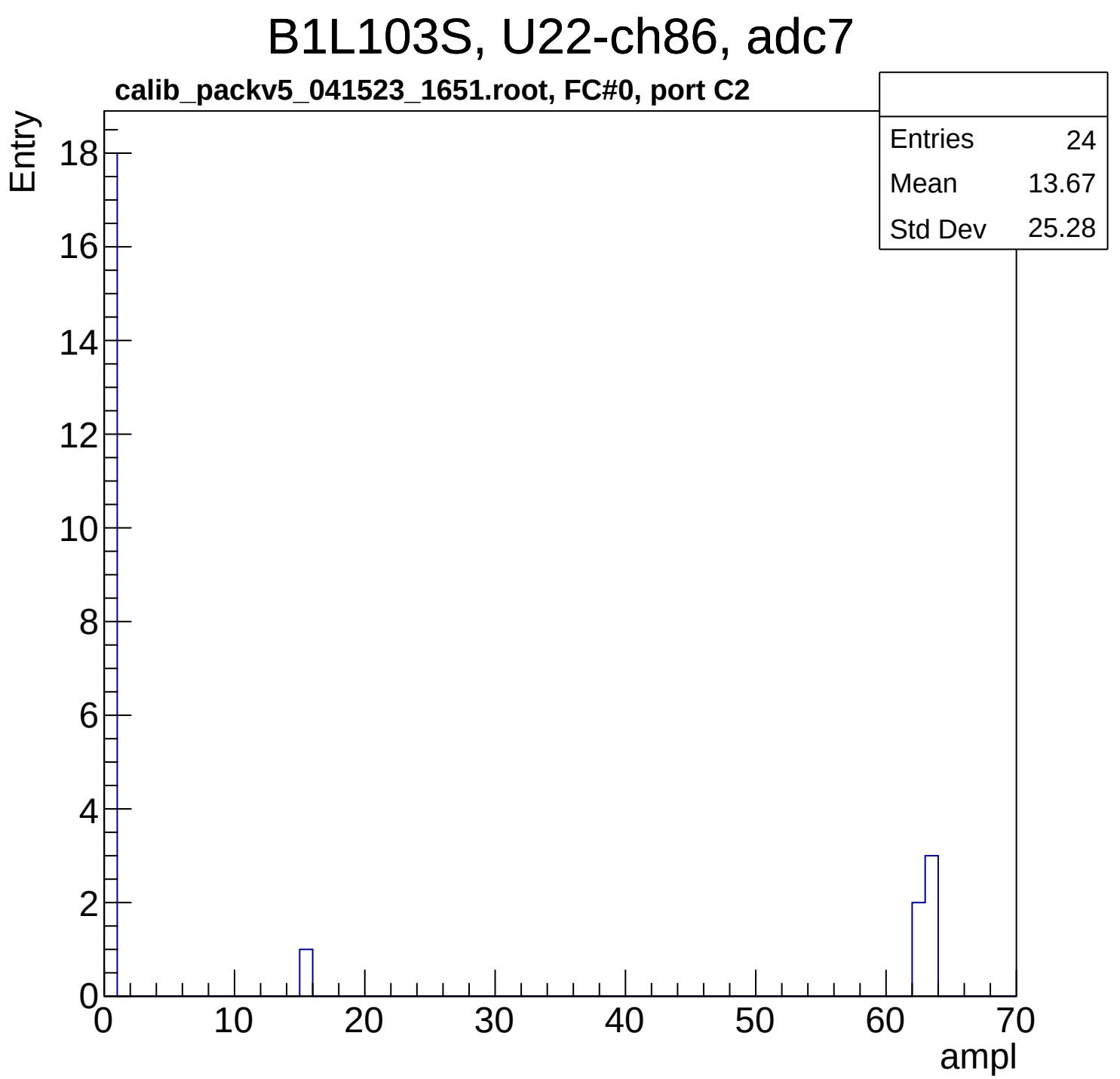
60
70


B1L103S, U22-ch86, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 58.33
Std Dev 12.27
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U22-ch86, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 13.67
Std Dev 25.28
Entry
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4
6
8
10
12
14
16
18
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10
20
30
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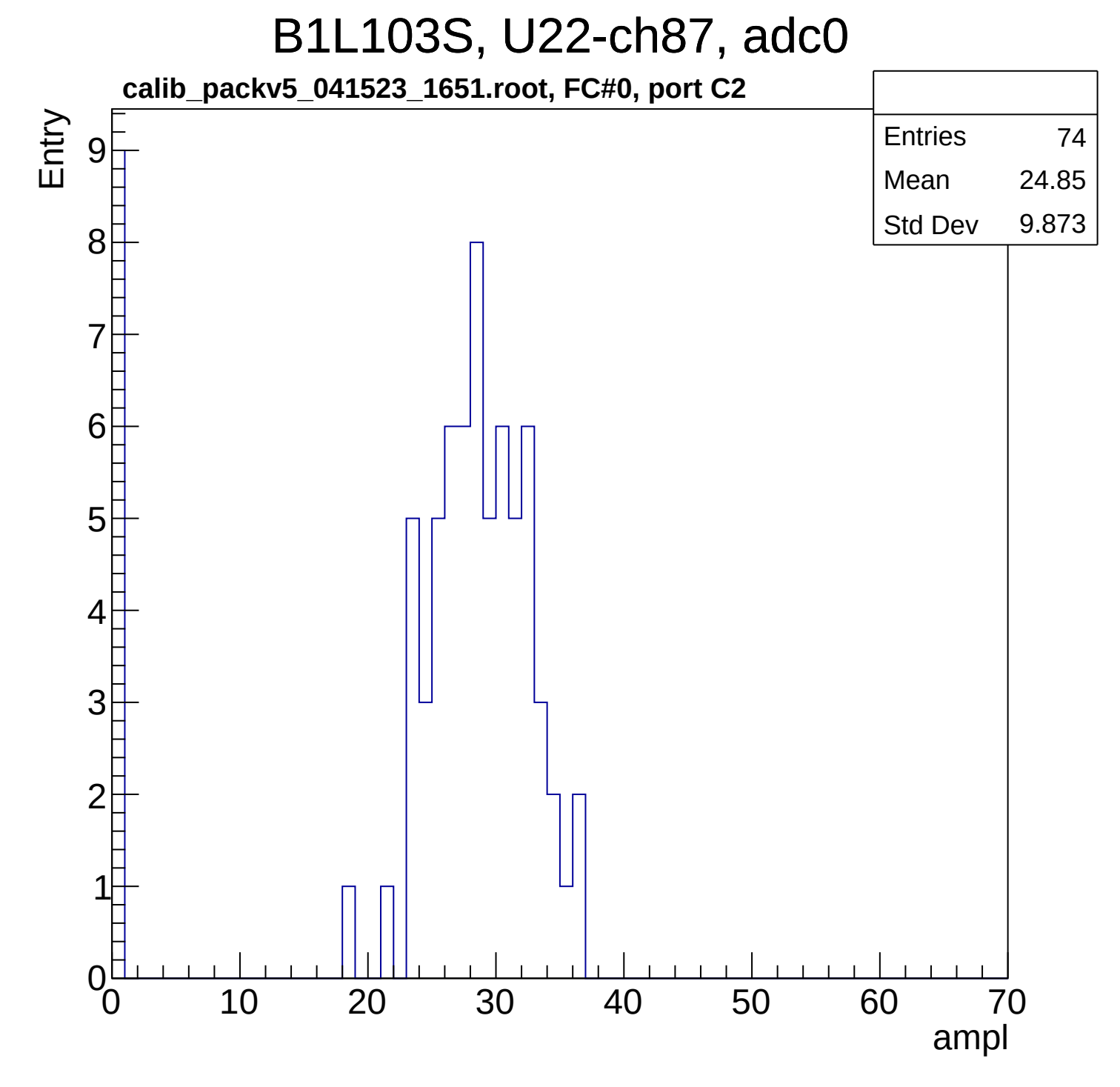
50
60
70
ampl


B1L103S, U22-ch87, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 24.85
Std Dev 9.873
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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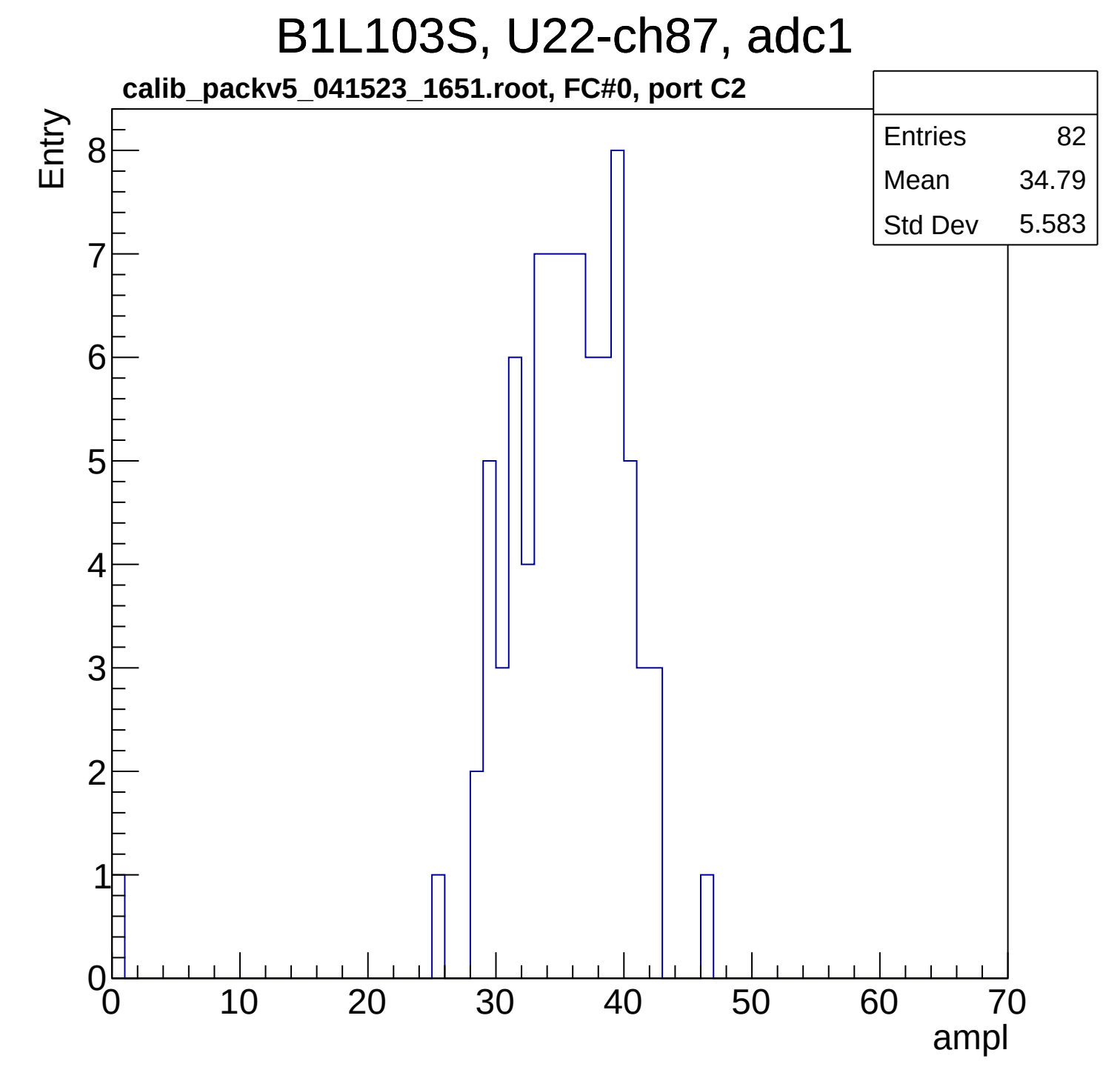
60
70


B1L103S, U22-ch87, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 34.79
Std Dev 5.583
Entry
ampl
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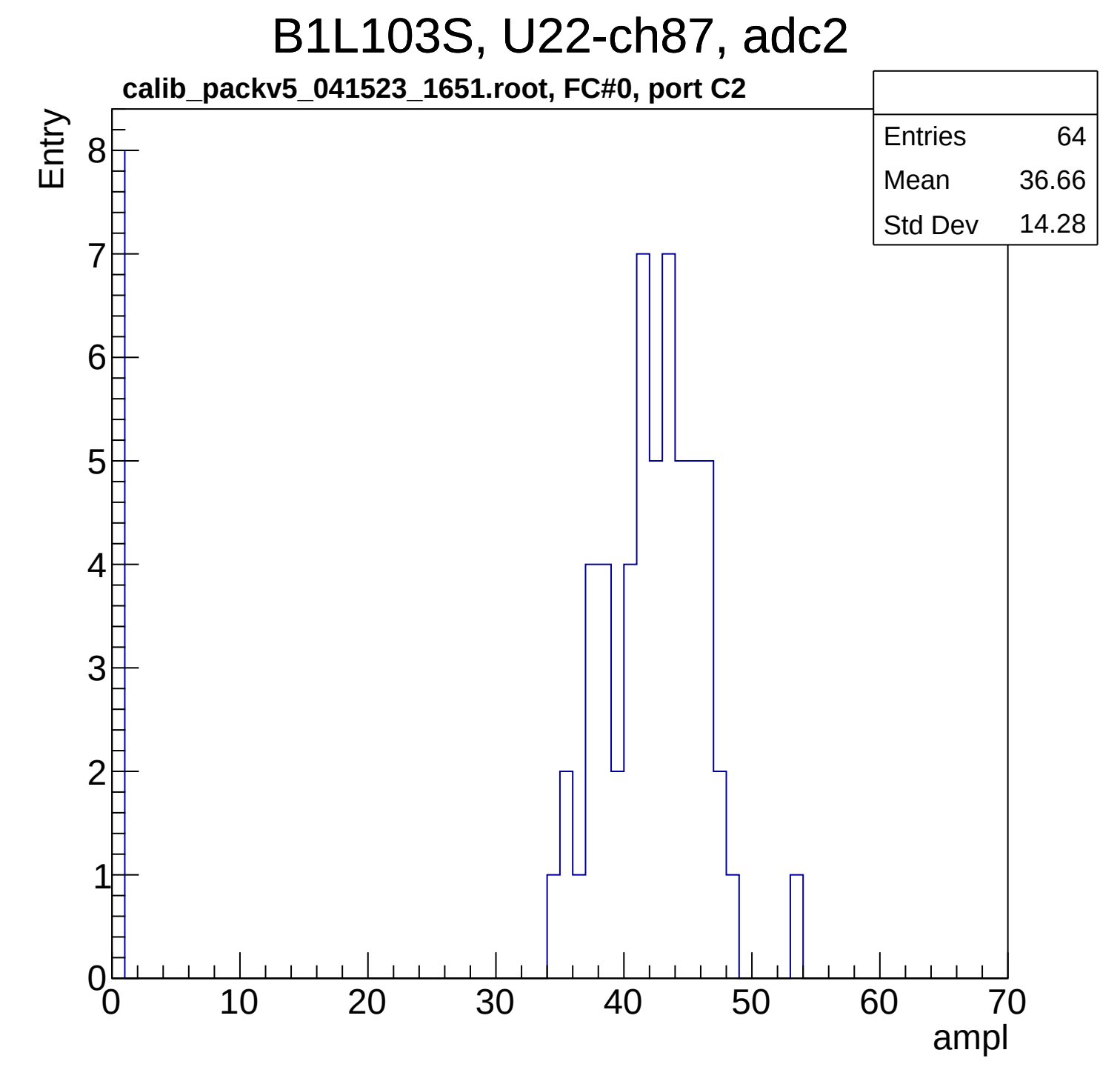
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch87, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 36.66
Std Dev 14.28
Entry
ampl
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1
2
3
4
5
6
7
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60
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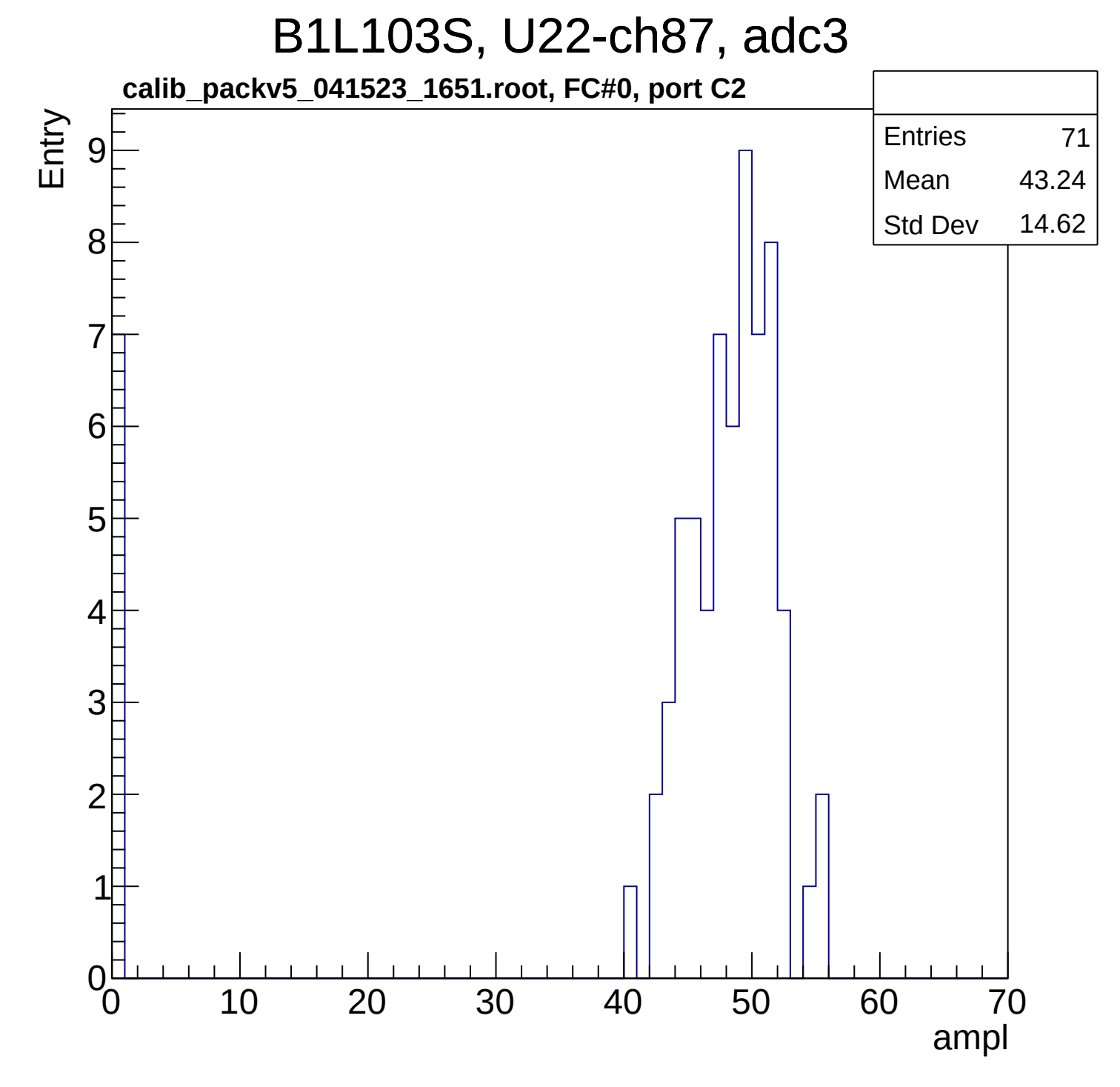
B1L103S, U22-ch87, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 43.24
Std Dev 14.62
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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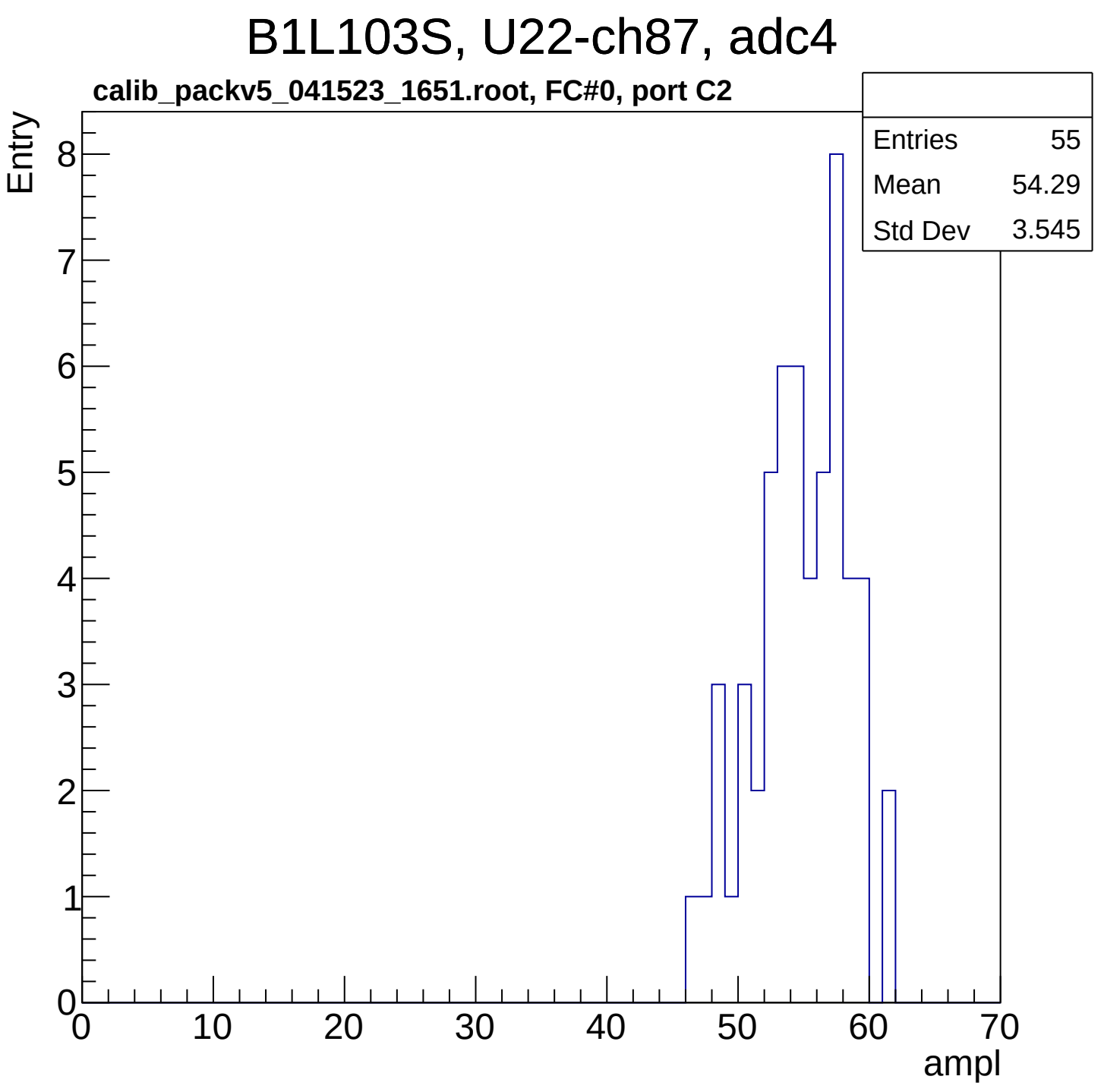
40
50
60
70


B1L103S, U22-ch87, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 54.29
Std Dev 3.545
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
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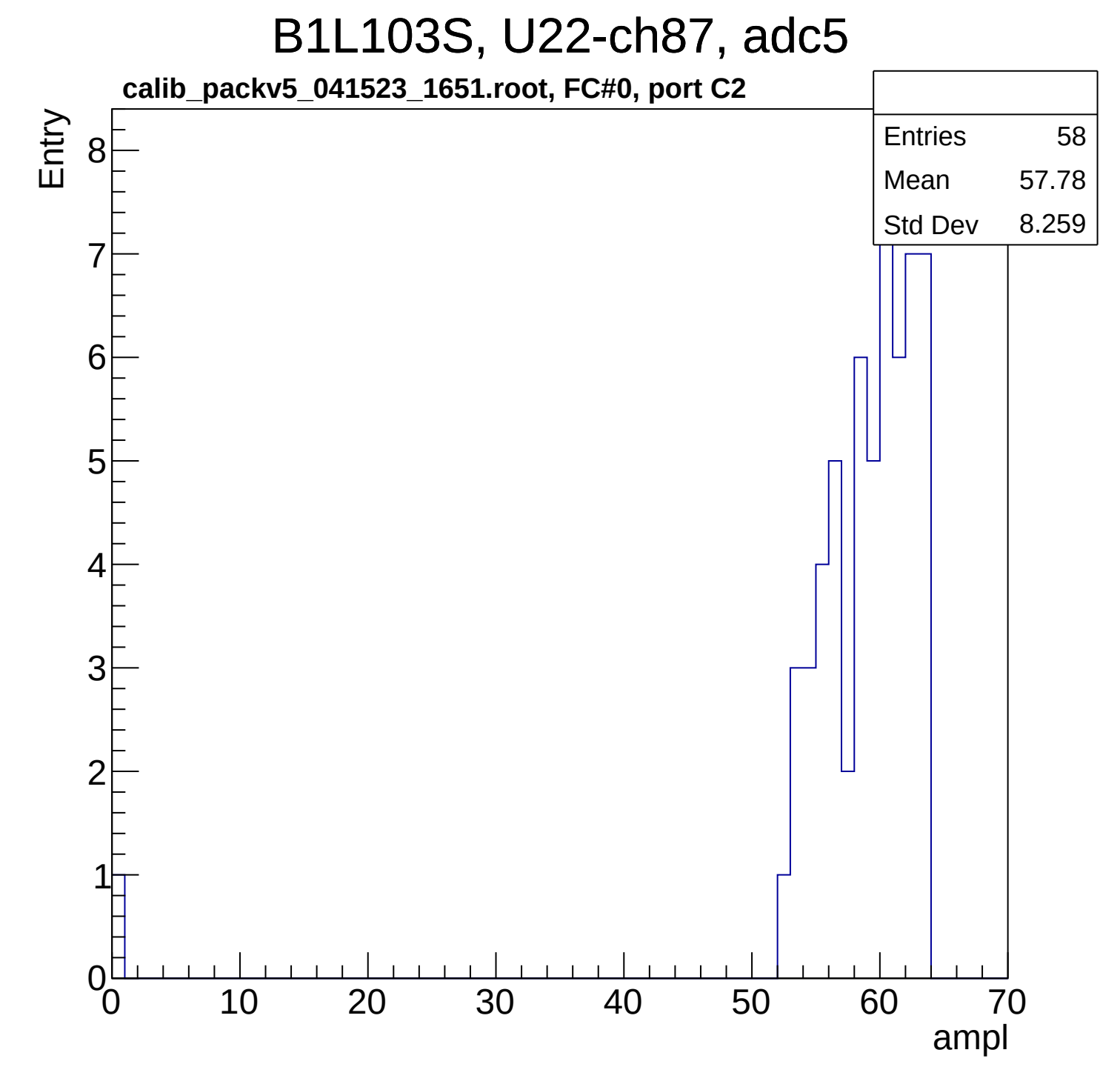
B1L103S, U22-ch87, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 57.78
Std Dev 8.259
Entry
ampl
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2
3
4
5
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7
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0
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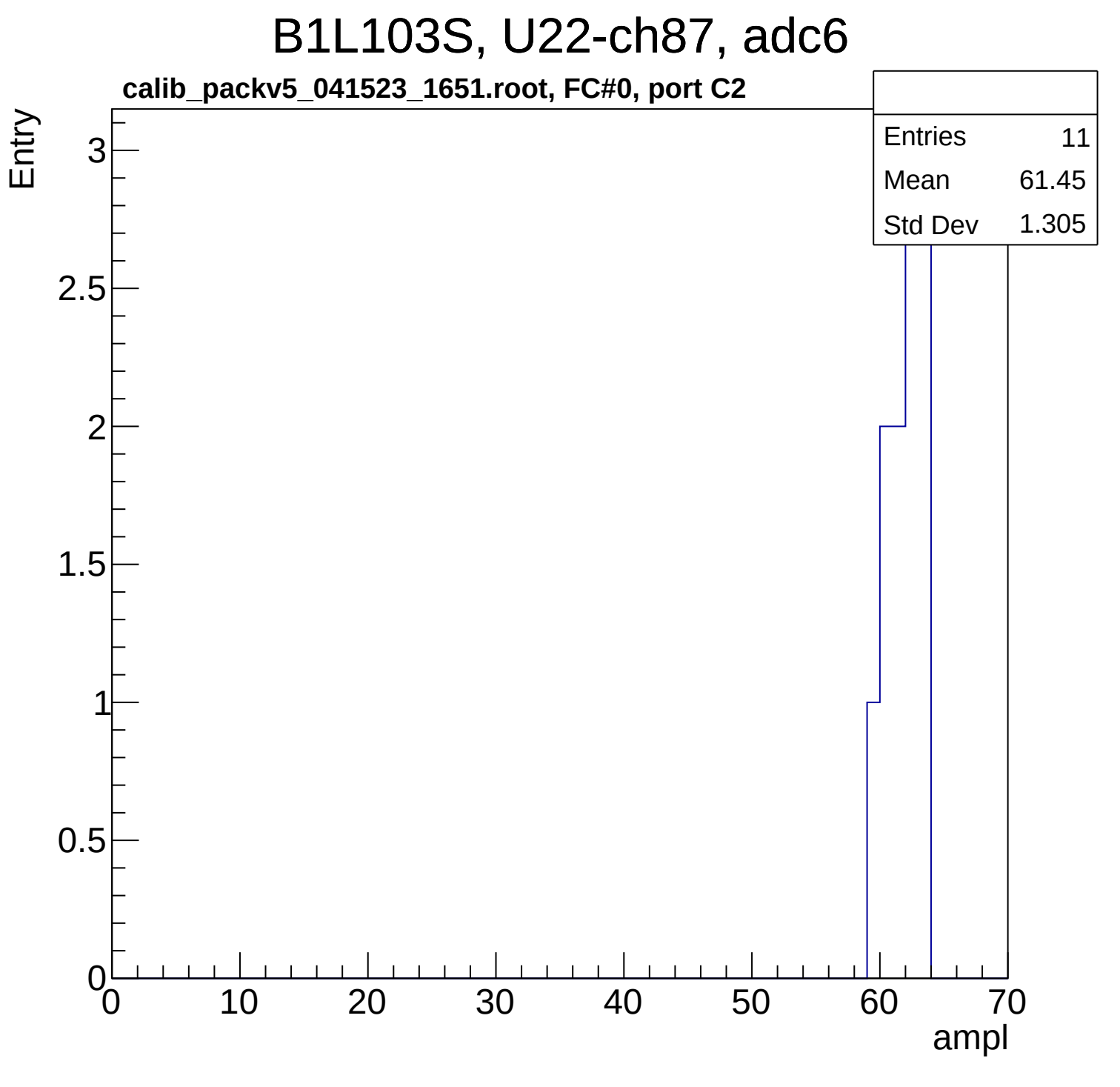
B1L103S, U22-ch87, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 61.45
Std Dev 1.305
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
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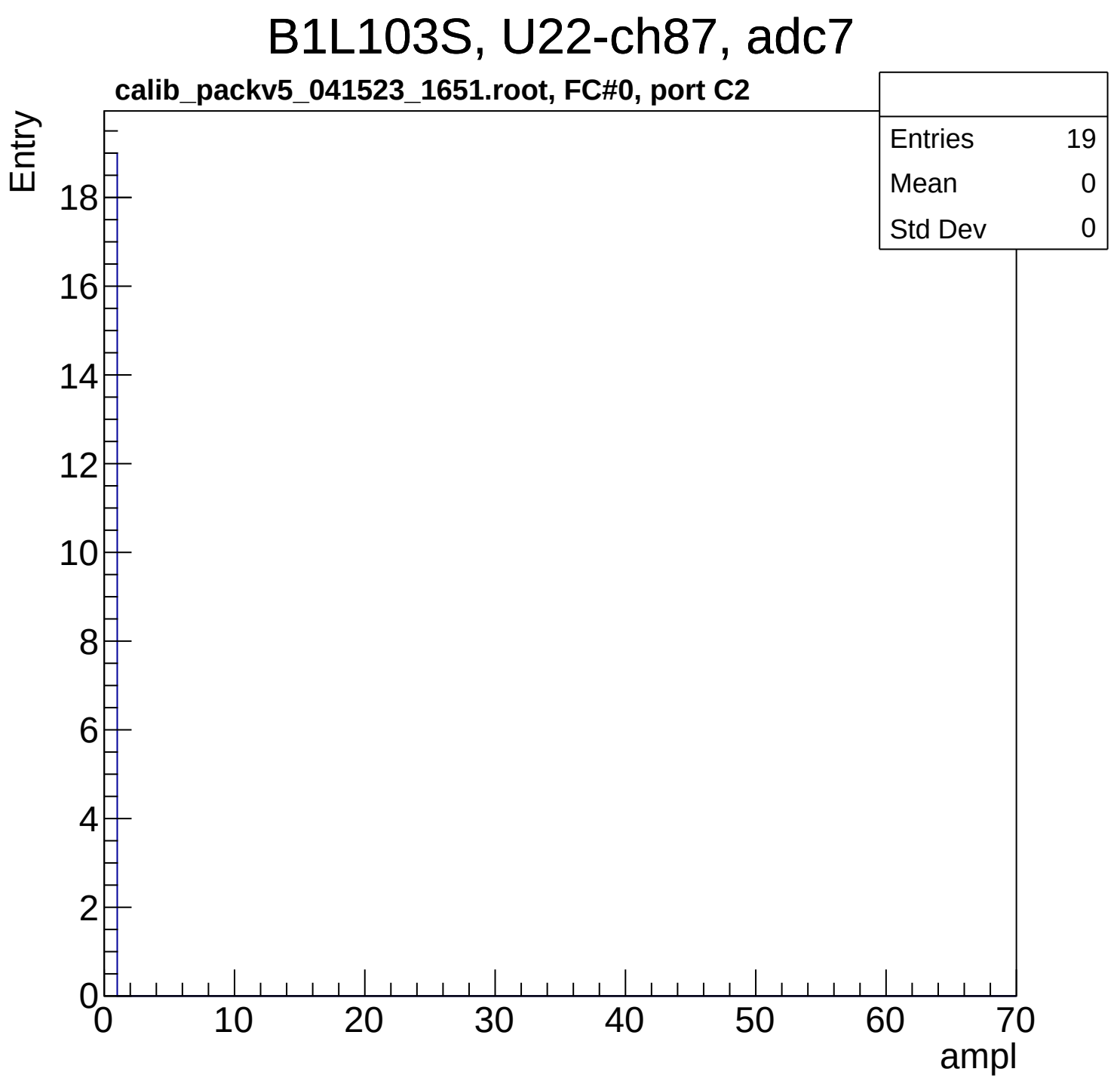
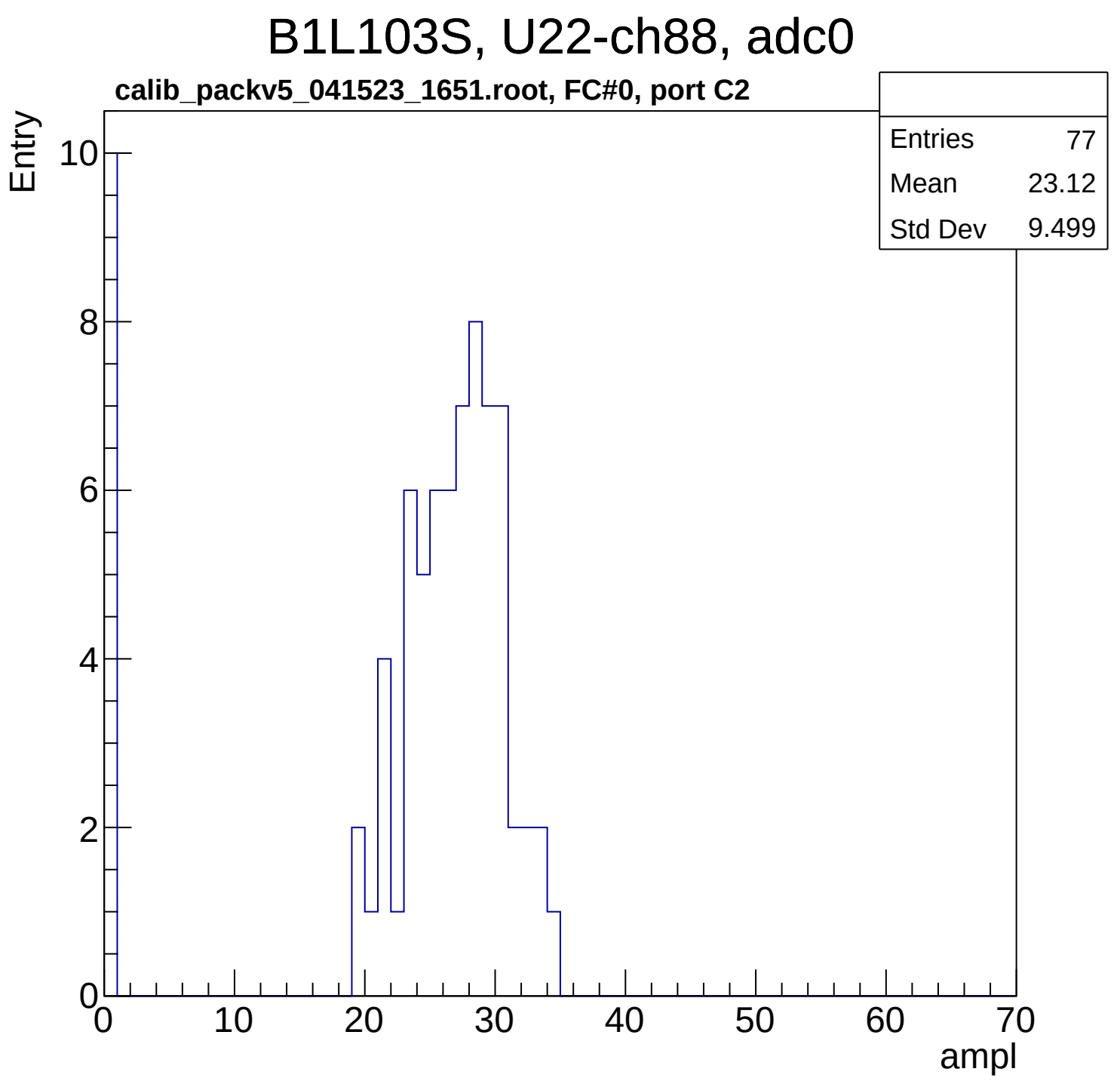

B1L103S, U22-ch87, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch88, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 23.12
Std Dev 9.499
Entry
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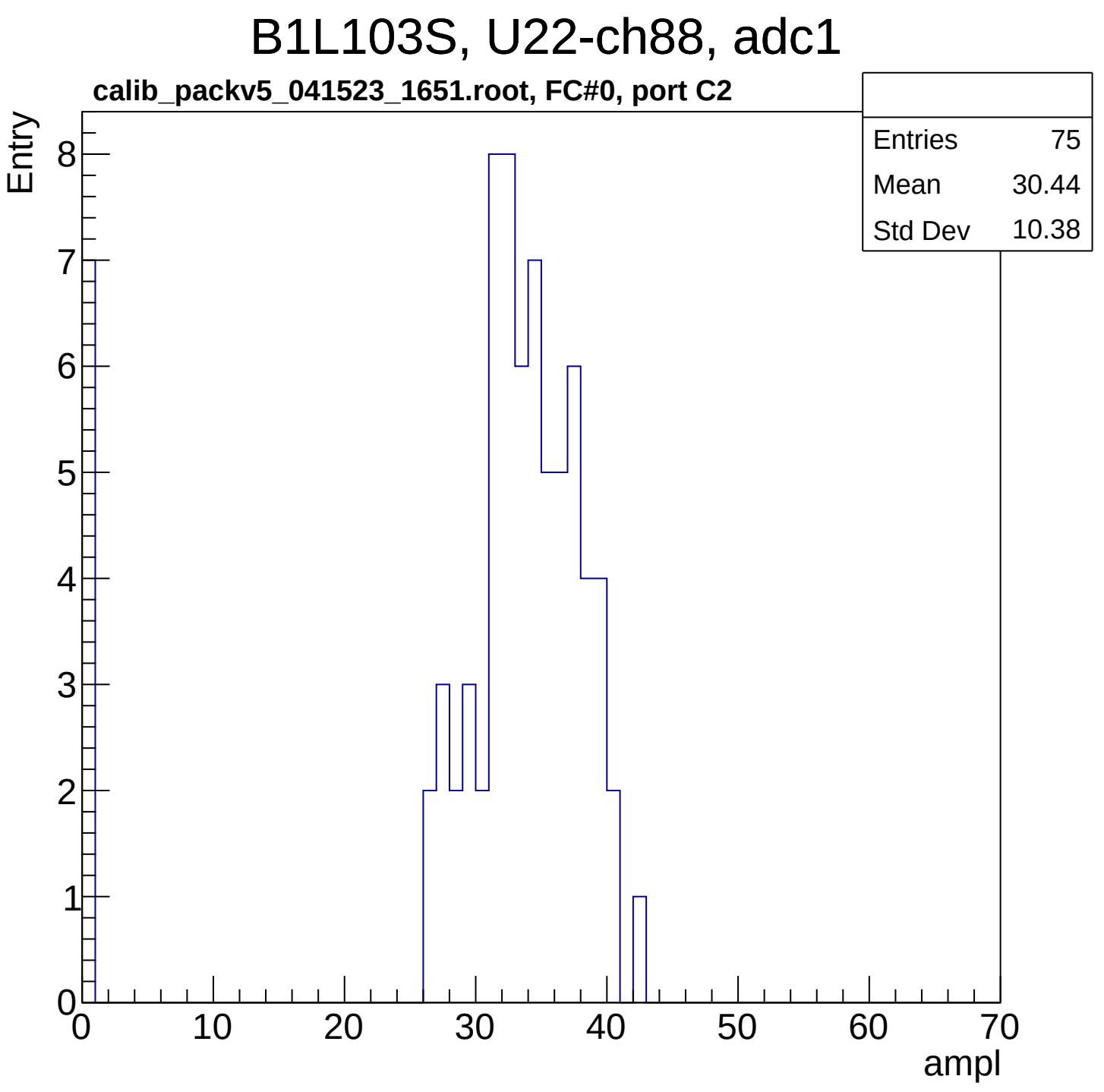
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch88, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 30.44
Std Dev 10.38
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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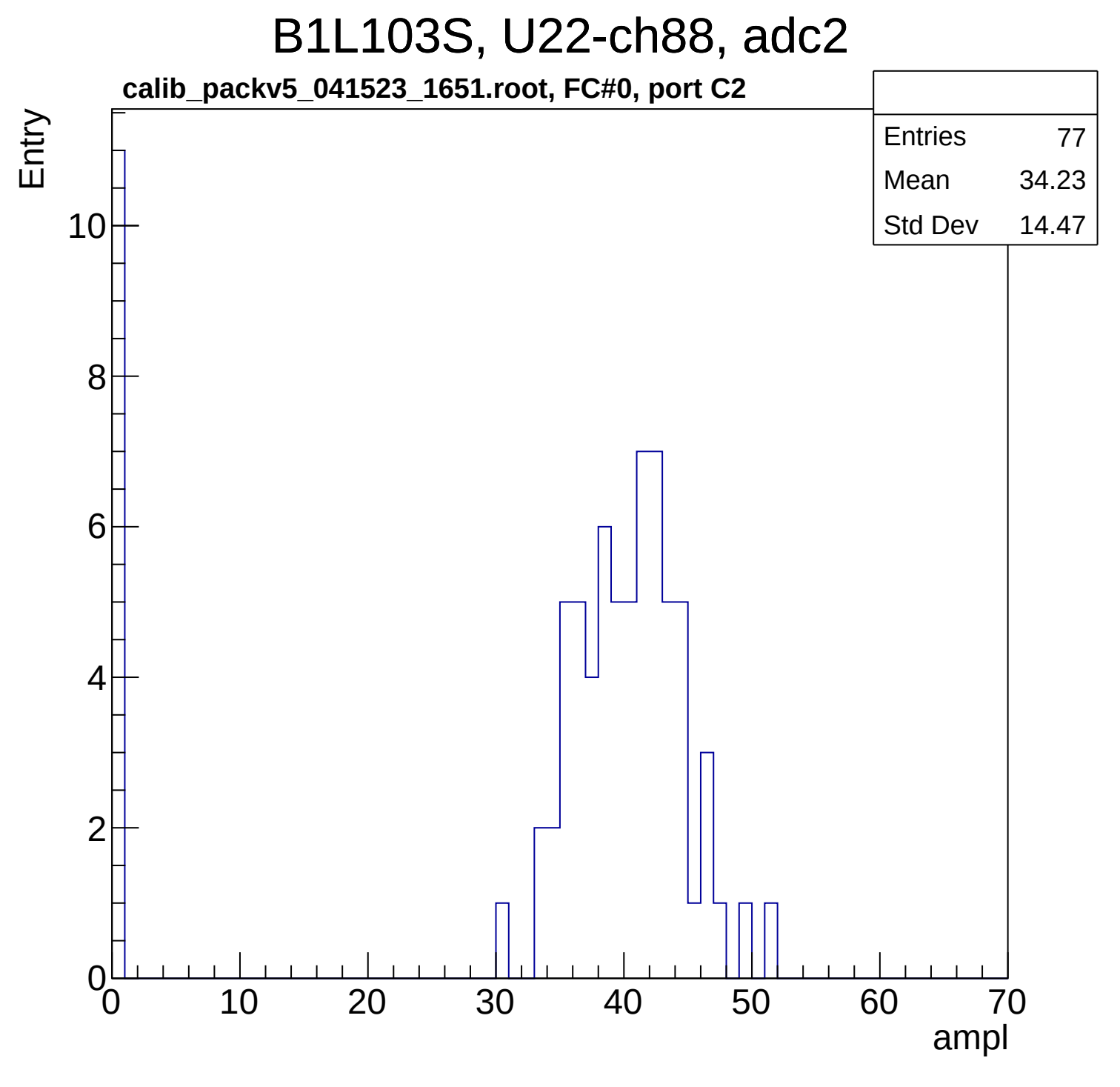
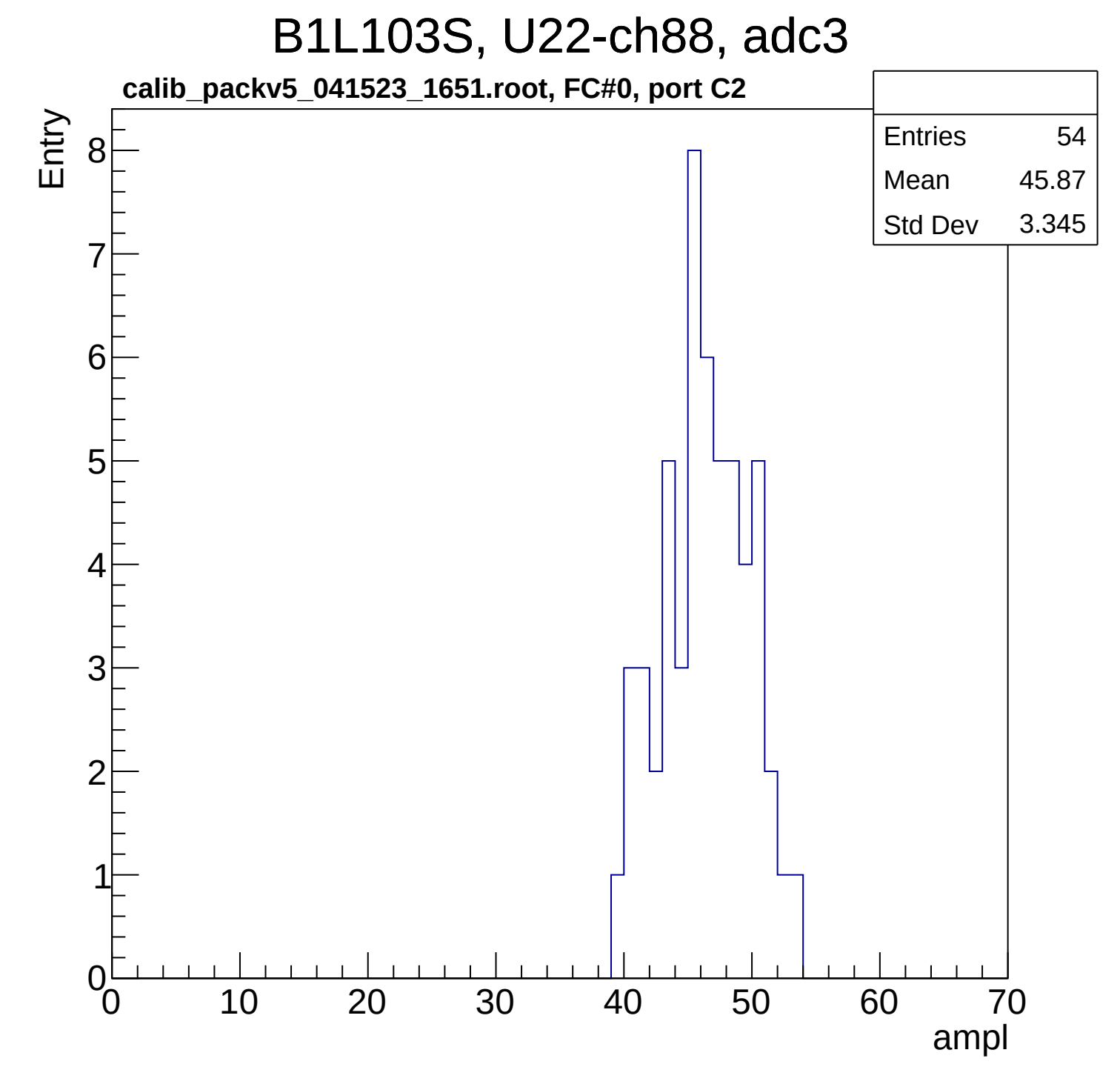

B1L103S, U22-ch88, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 34.23
Std Dev 14.47
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch88, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 45.87
Std Dev 3.345
Entry
ampl
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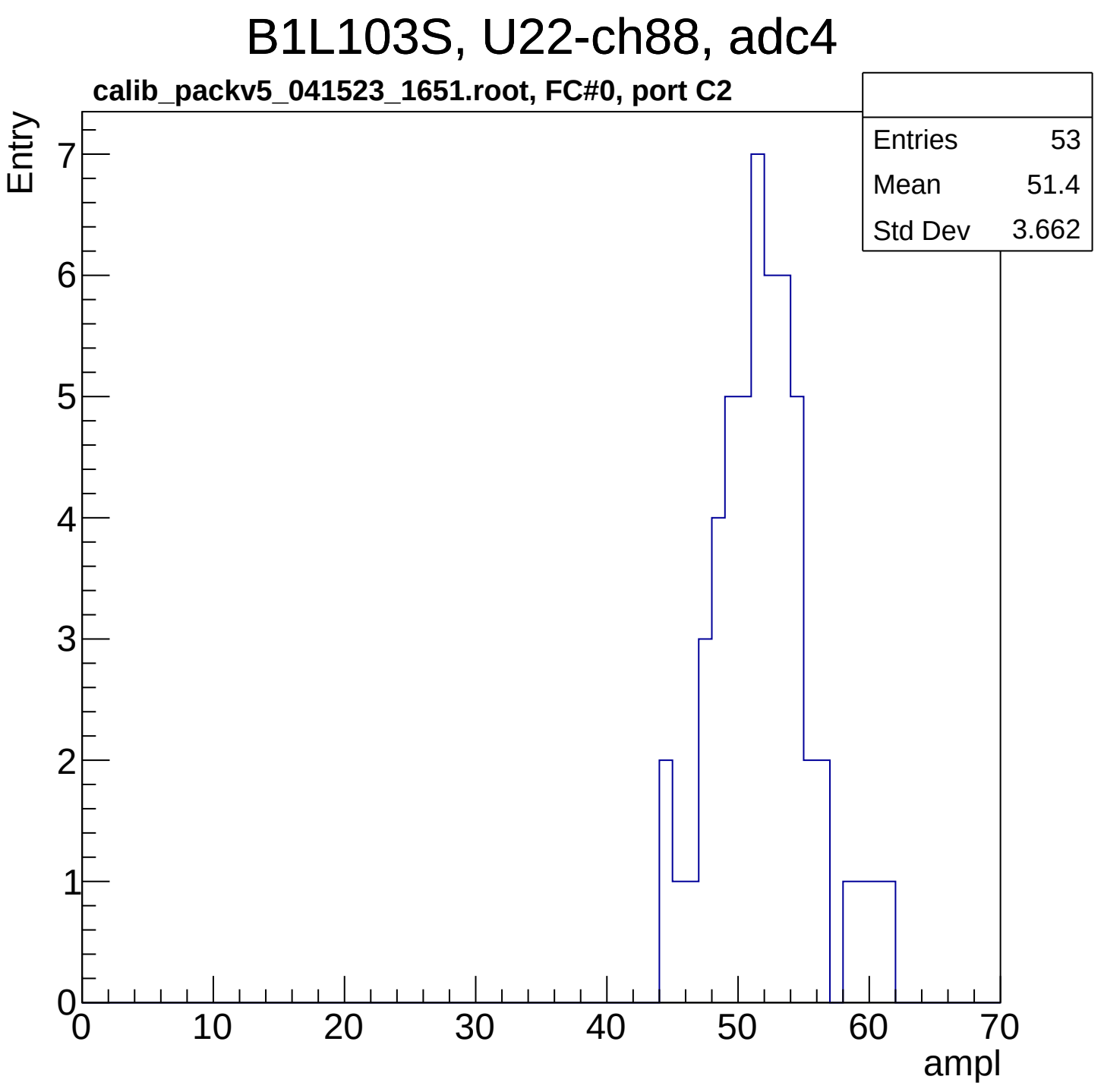
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch88, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 51.4
Std Dev 3.662
Entry
ampl
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2
3
4
5
6
7
0
10
20
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40
50
60
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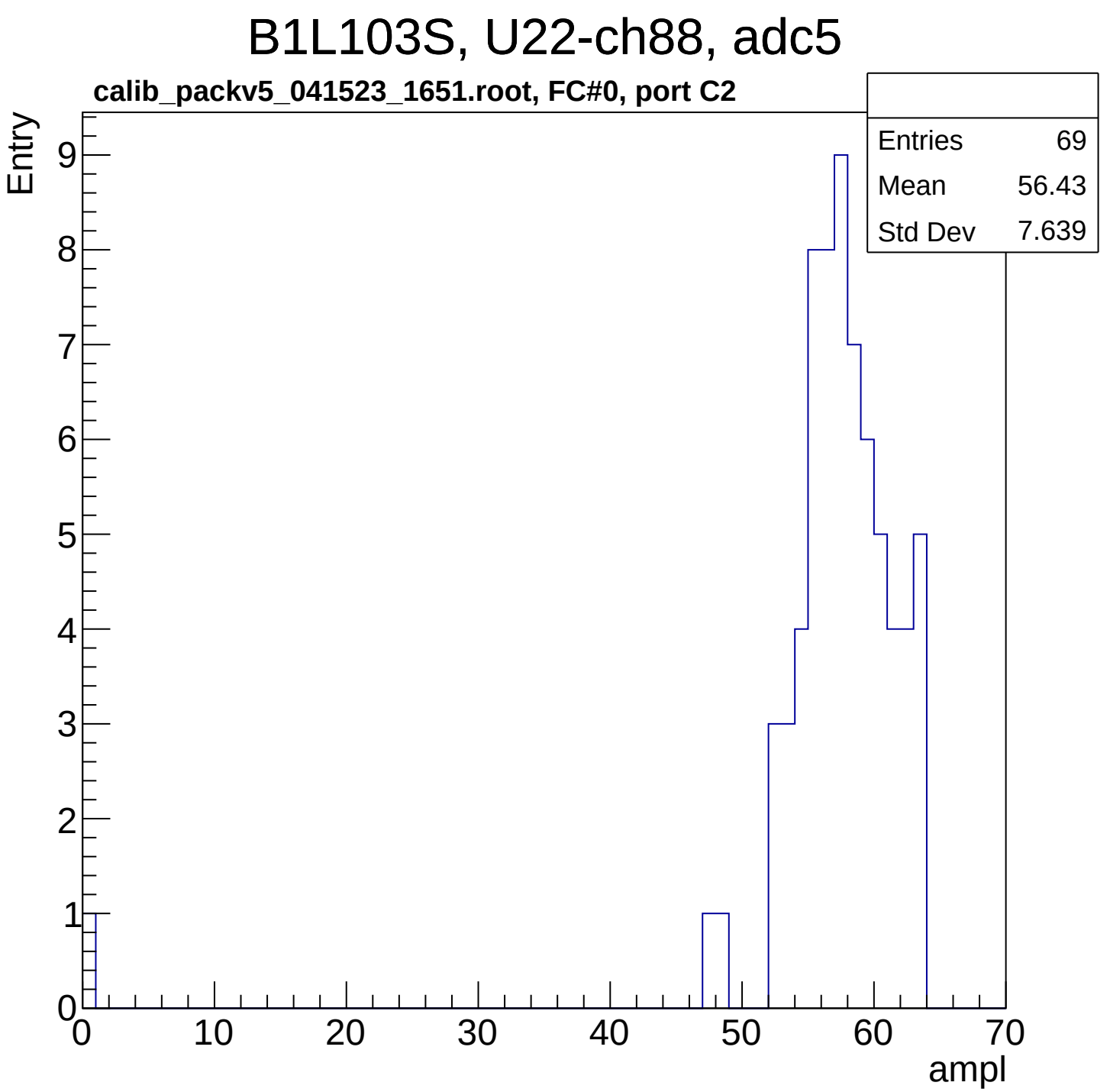
B1L103S, U22-ch88, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 56.43
Std Dev 7.639
Entry
ampl
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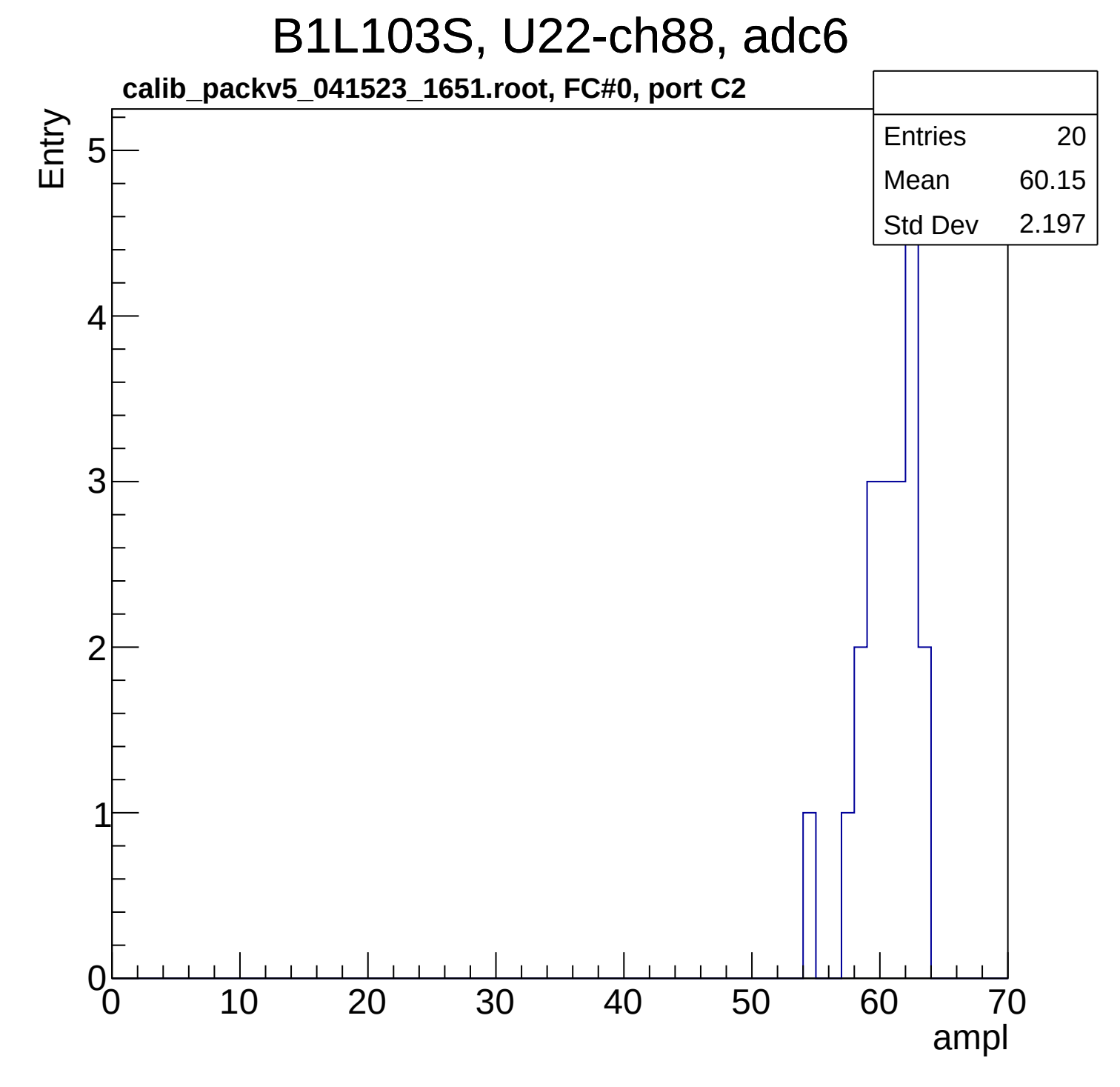
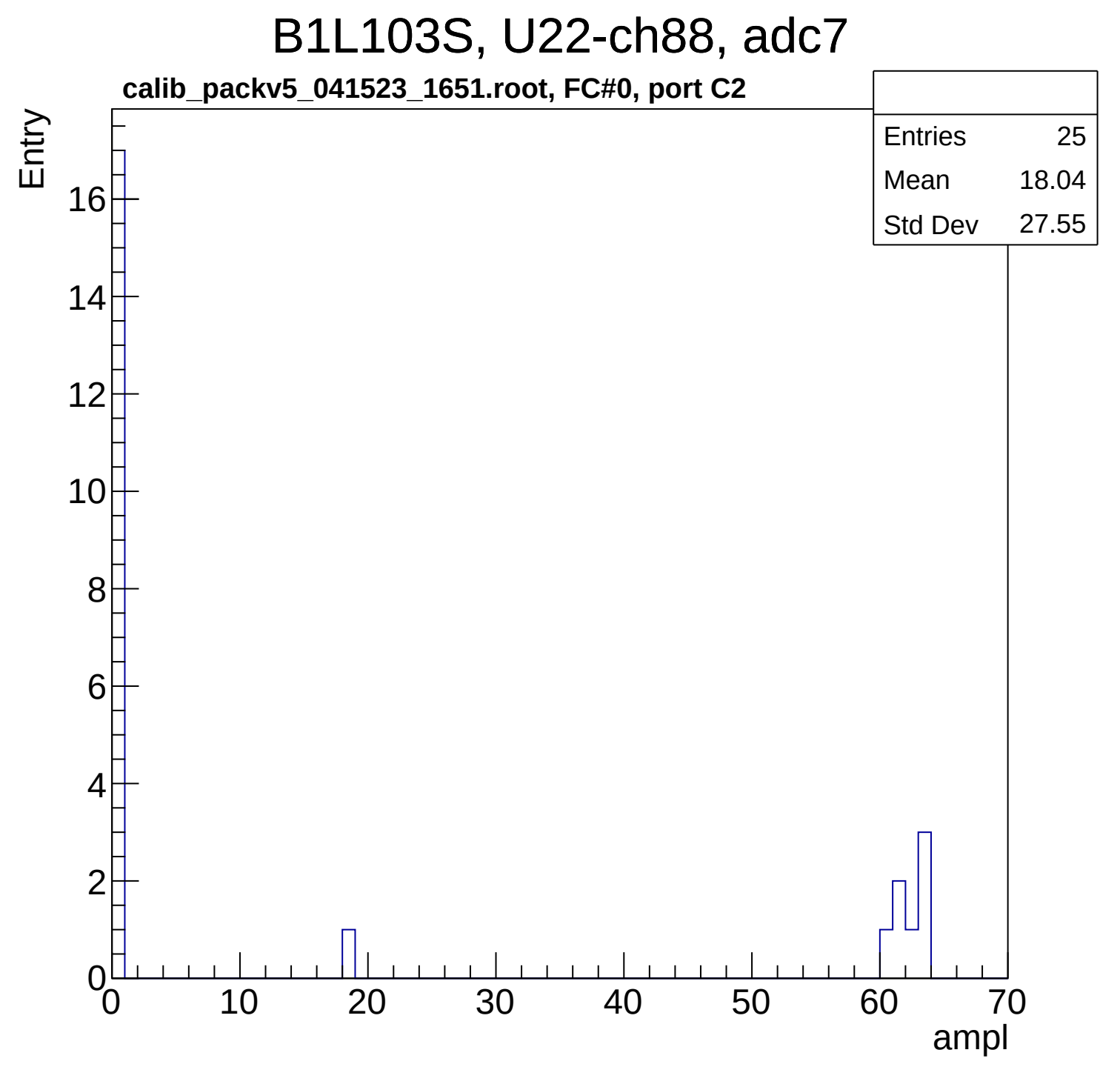
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch88, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 60.15
Std Dev 2.197
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U22-ch88, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 18.04
Std Dev 27.55
Entry
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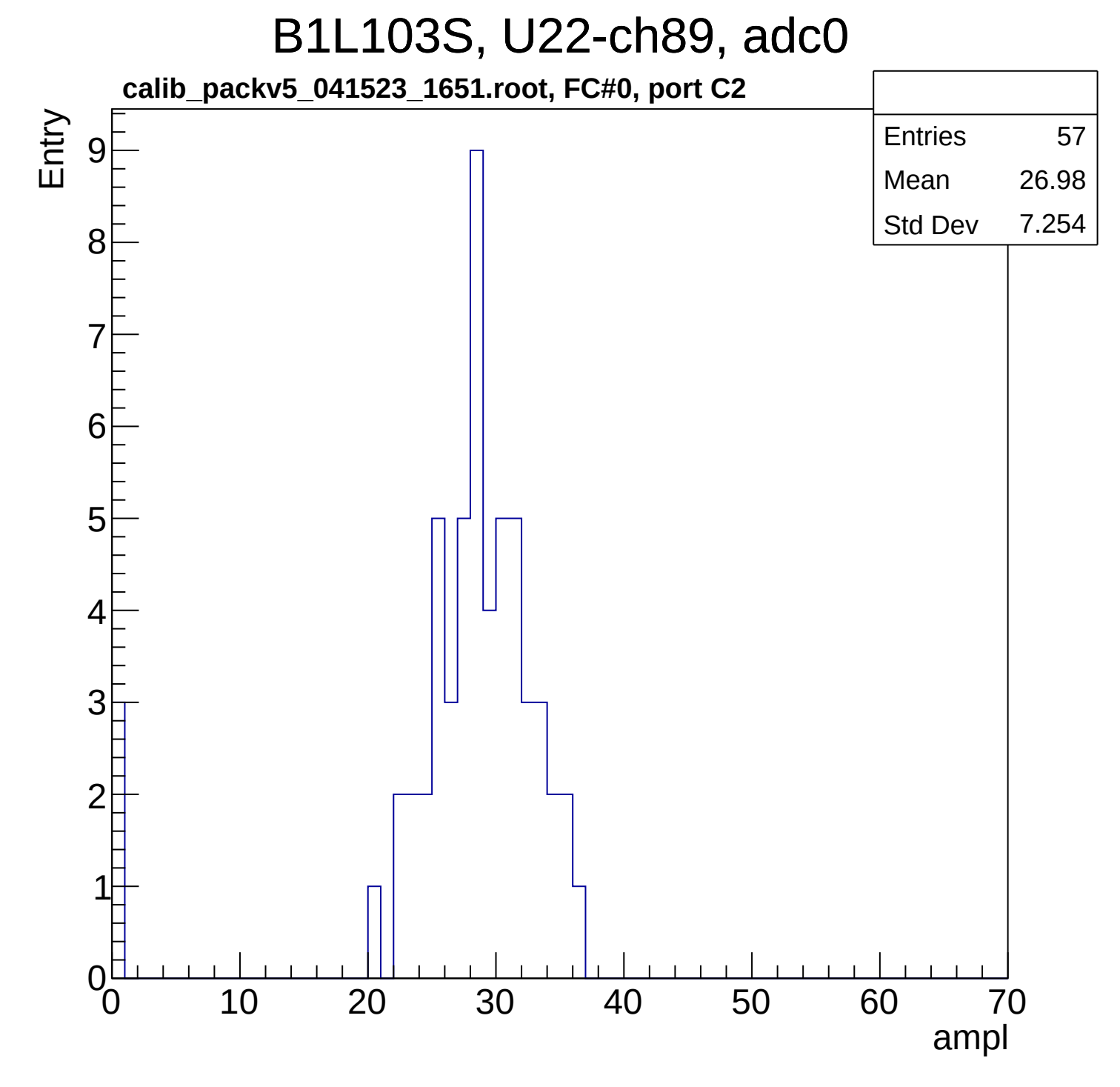
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch89, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 26.98
Std Dev 7.254
Entry
ampl
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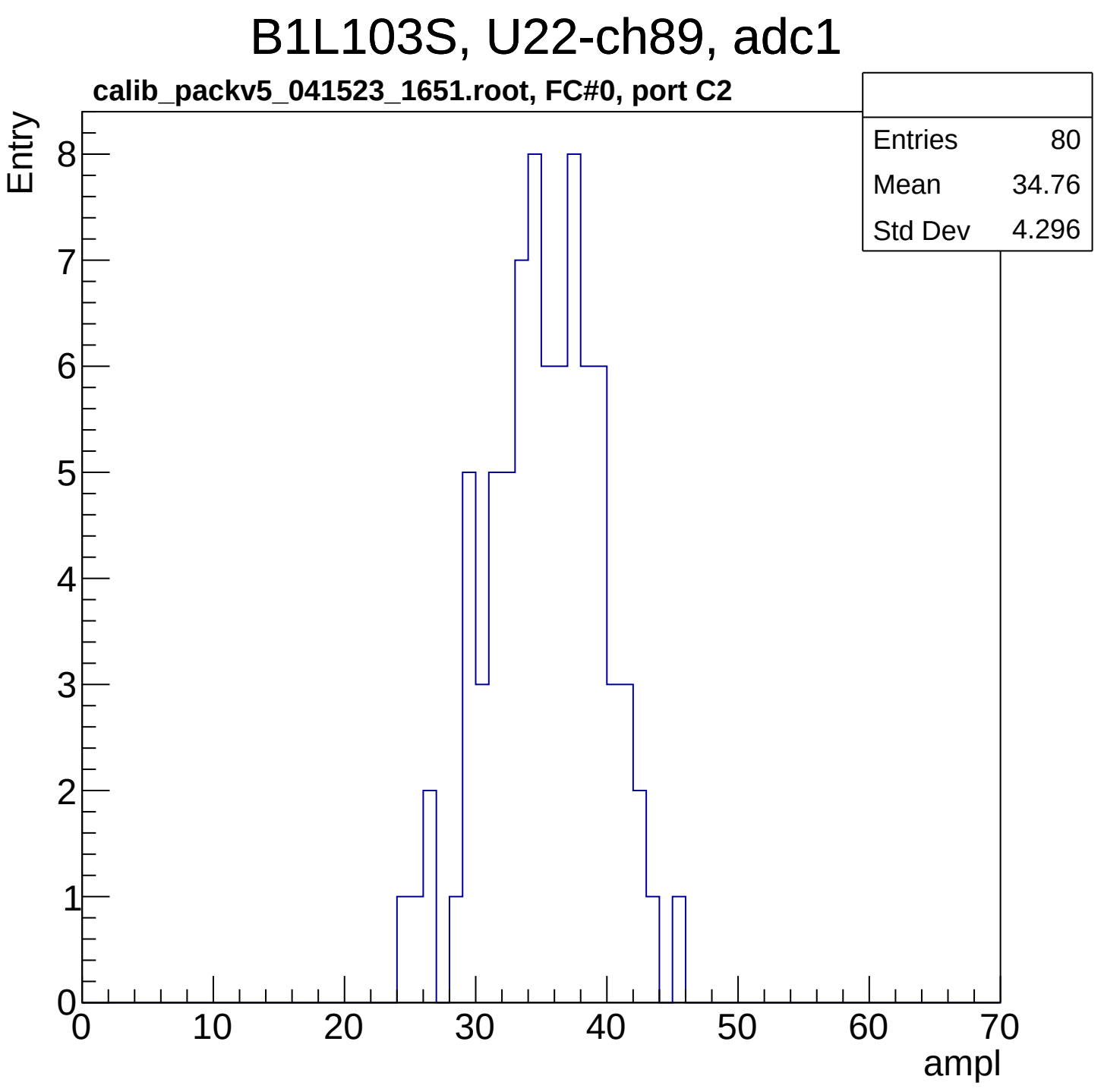
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch89, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 34.76
Std Dev 4.296
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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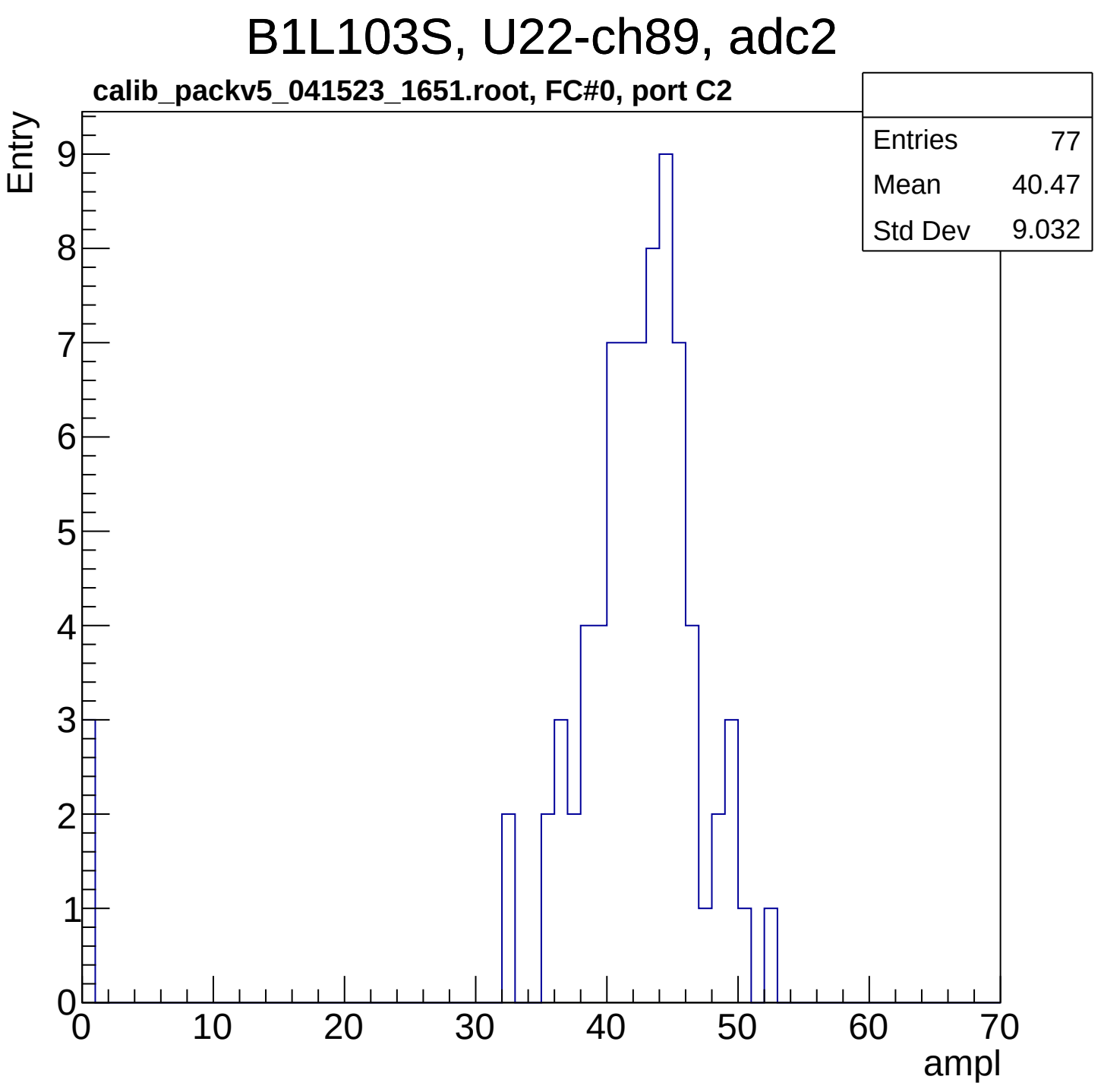
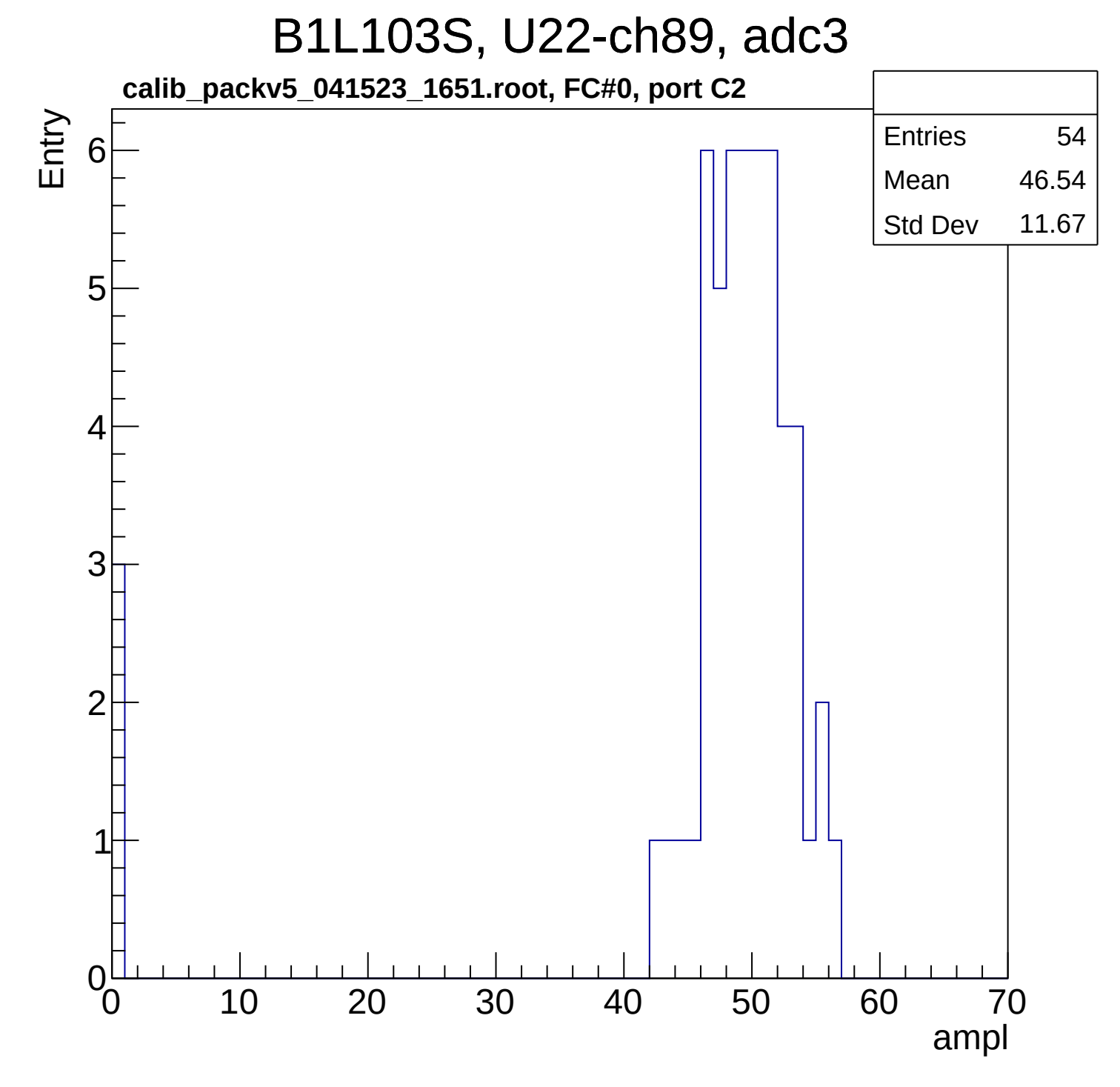
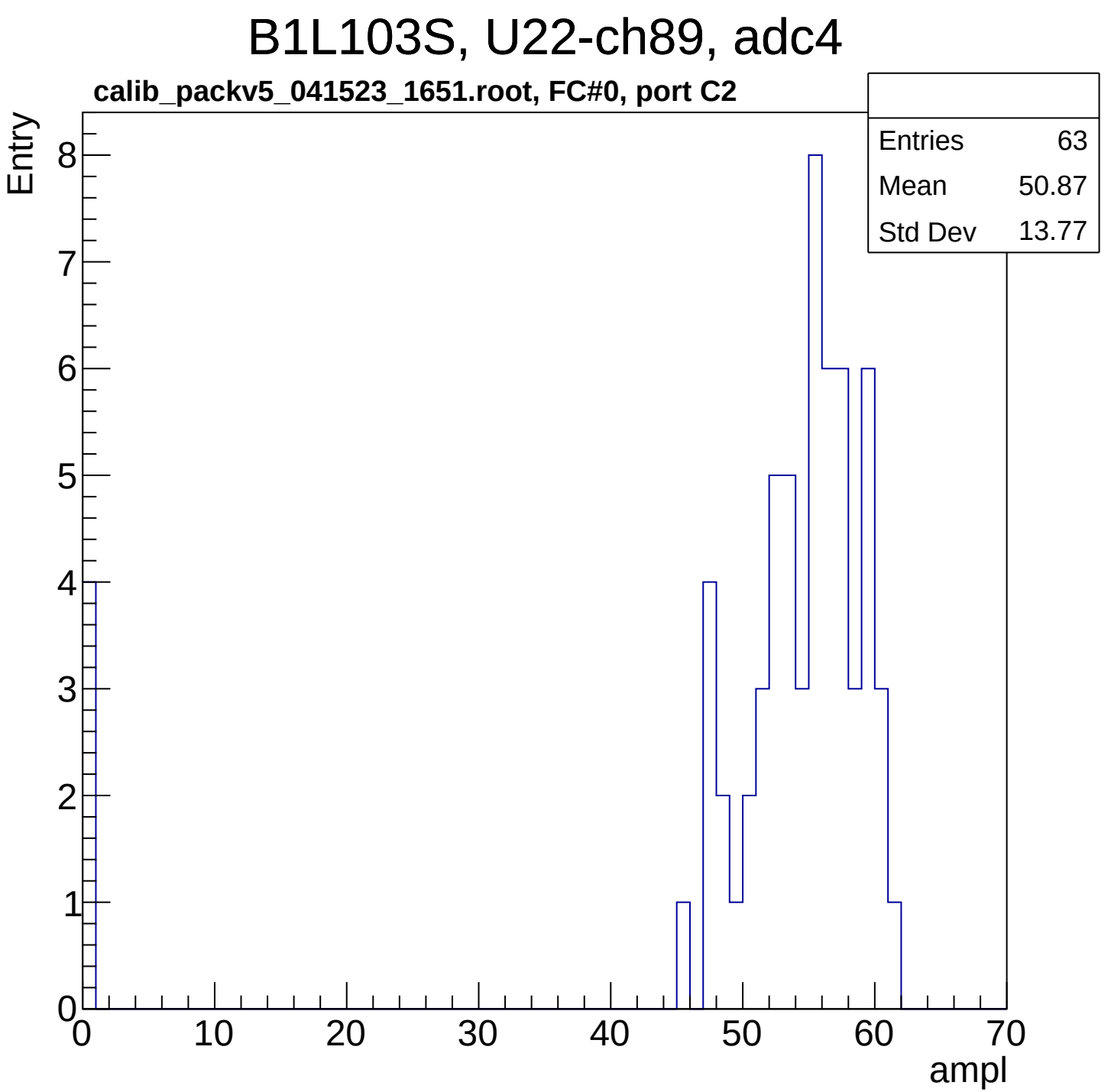

B1L103S, U22-ch89, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 40.47
Std Dev 9.032
Entry
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch89, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 46.54
Std Dev 11.67
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch89, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 50.87
Std Dev 13.77
Entry
ampl
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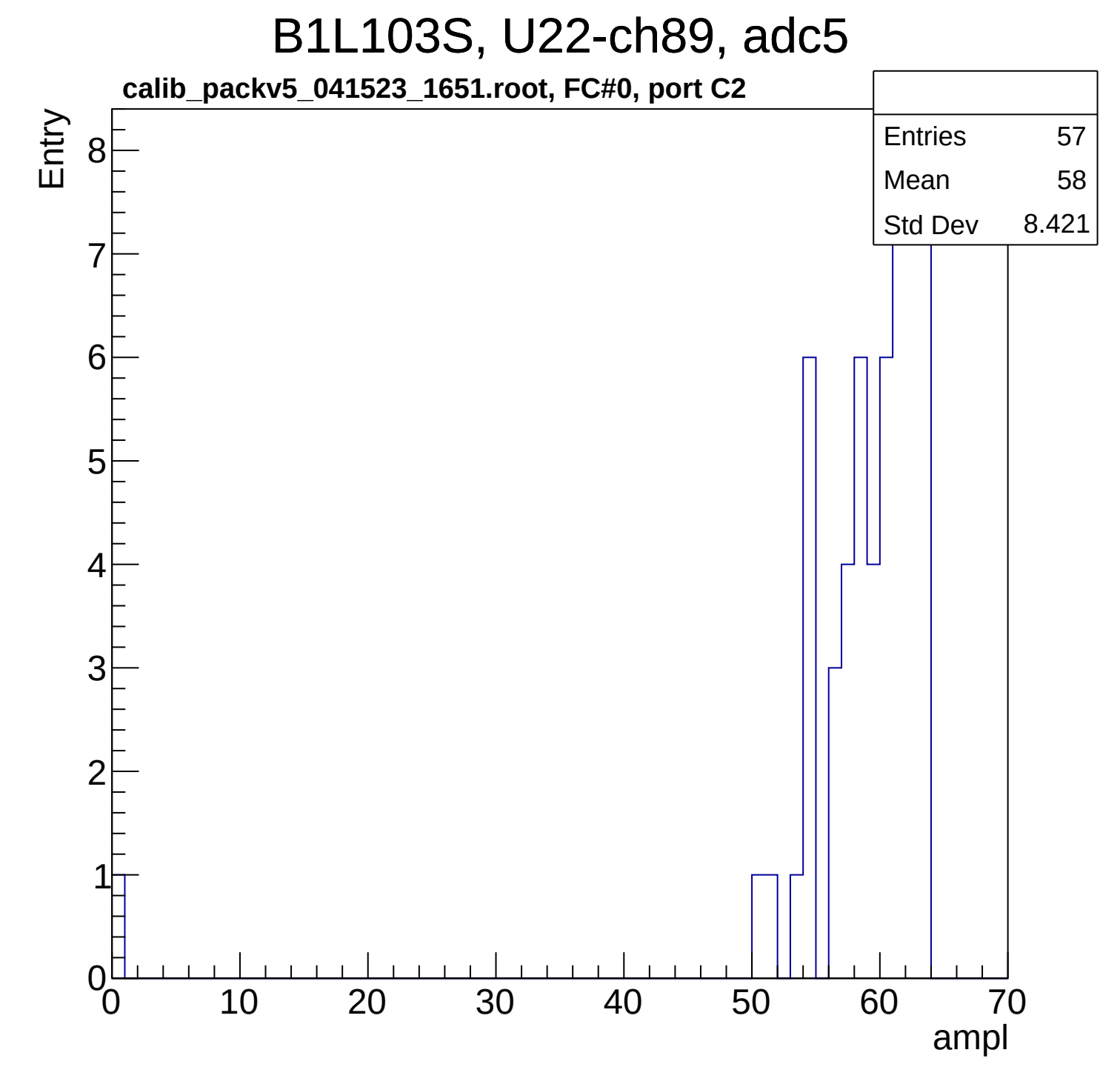
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch89, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 58
Std Dev 8.421
Entry
ampl
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1
2
3
4
5
6
7
8
0
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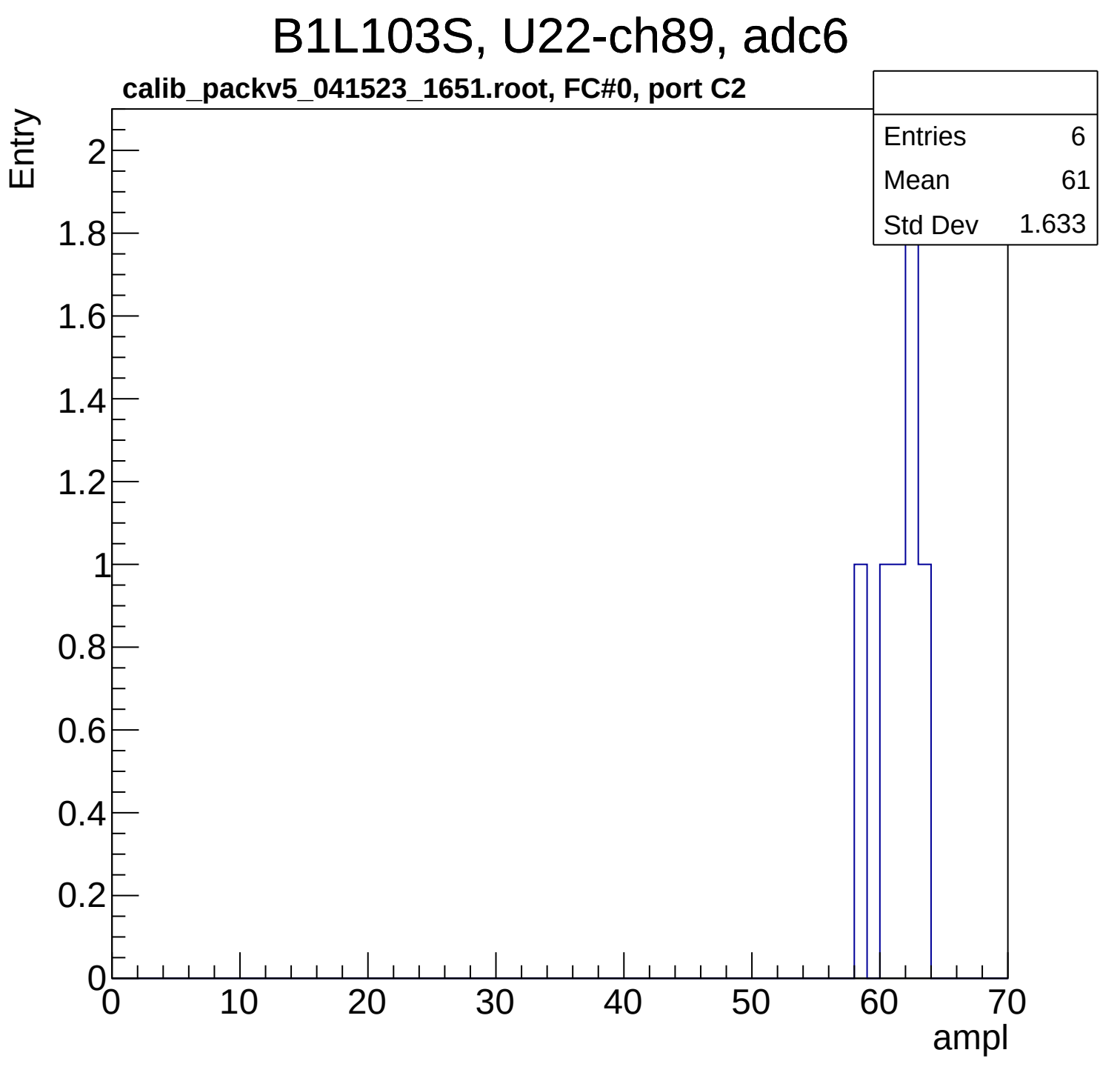
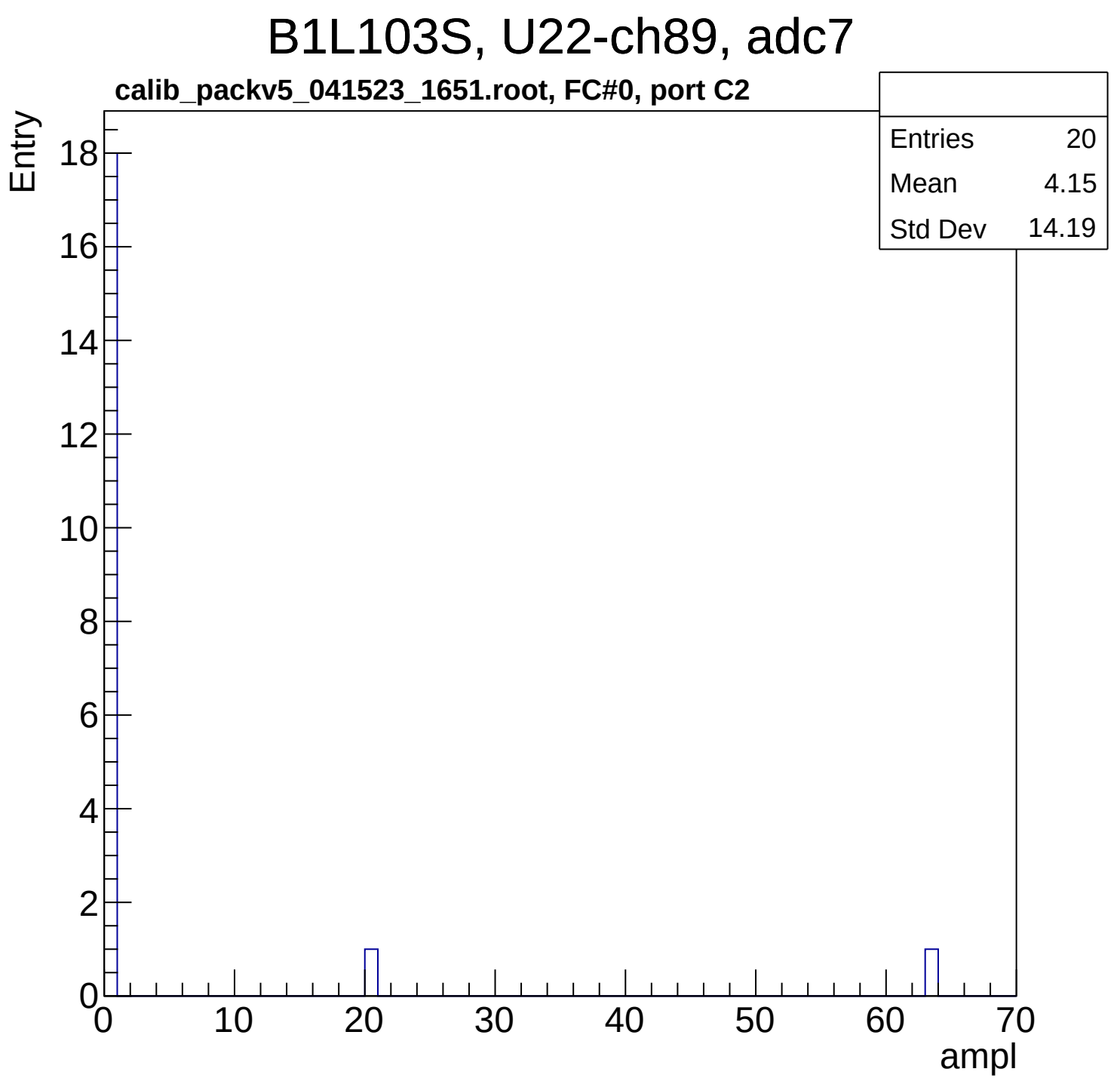
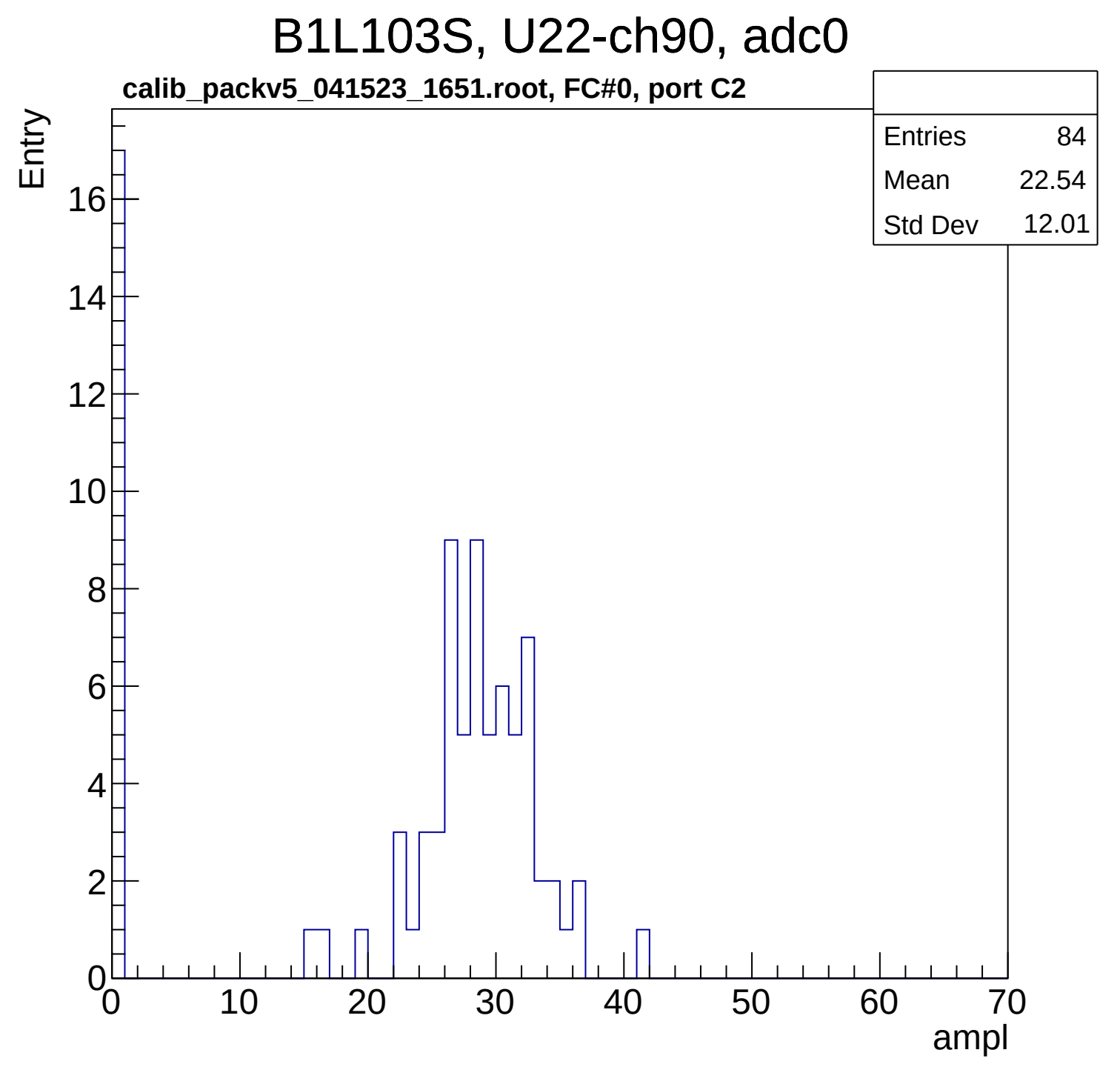
40
50
60
70


B1L103S, U22-ch89, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 61
Std Dev 1.633
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U22-ch89, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4.15
Std Dev 14.19
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch90, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 22.54
Std Dev 12.01
Entry
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4
6
8
10
12
14
16
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10
20
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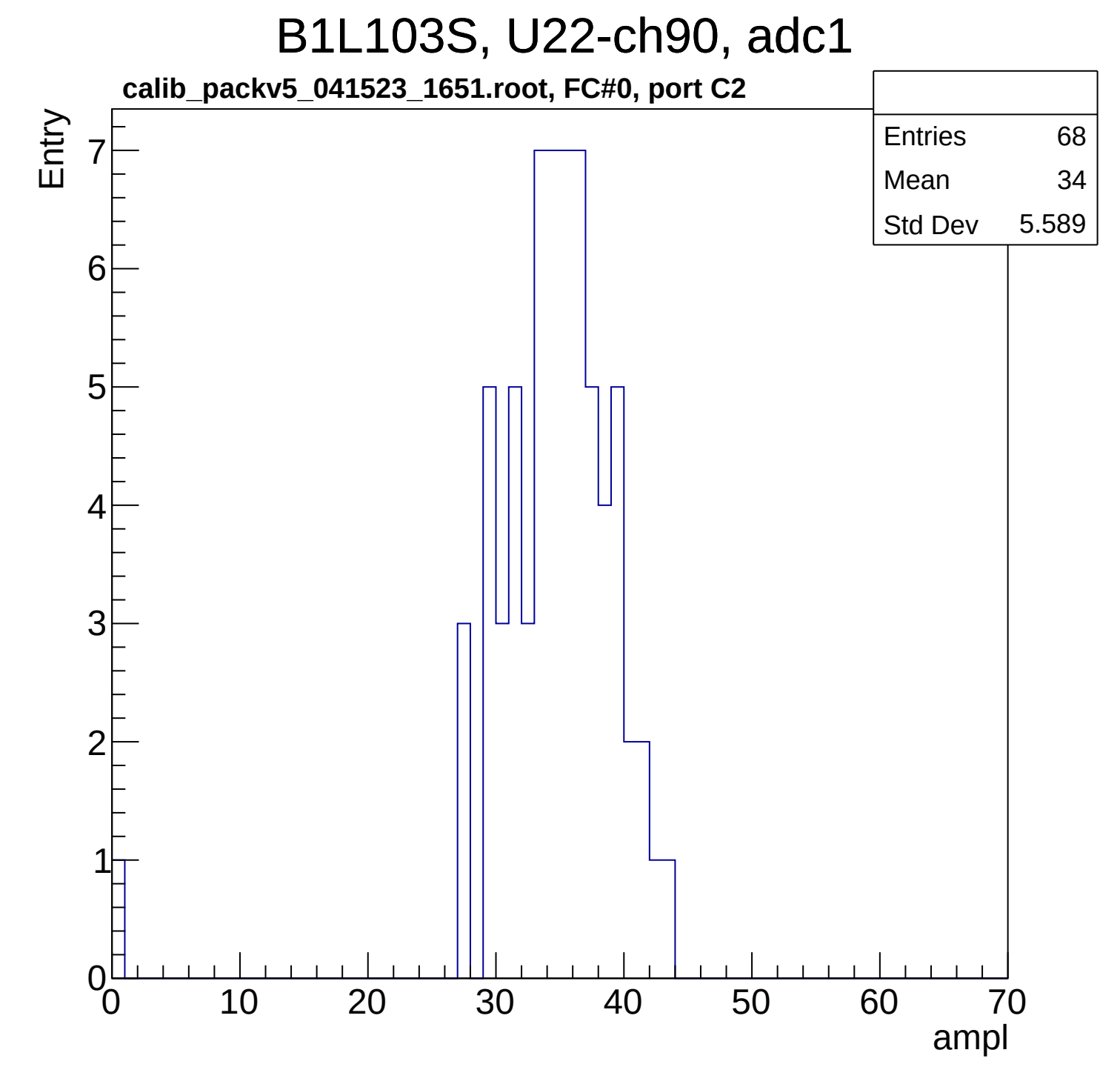
50
60
70
ampl


B1L103S, U22-ch90, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 34
Std Dev 5.589
Entry
ampl
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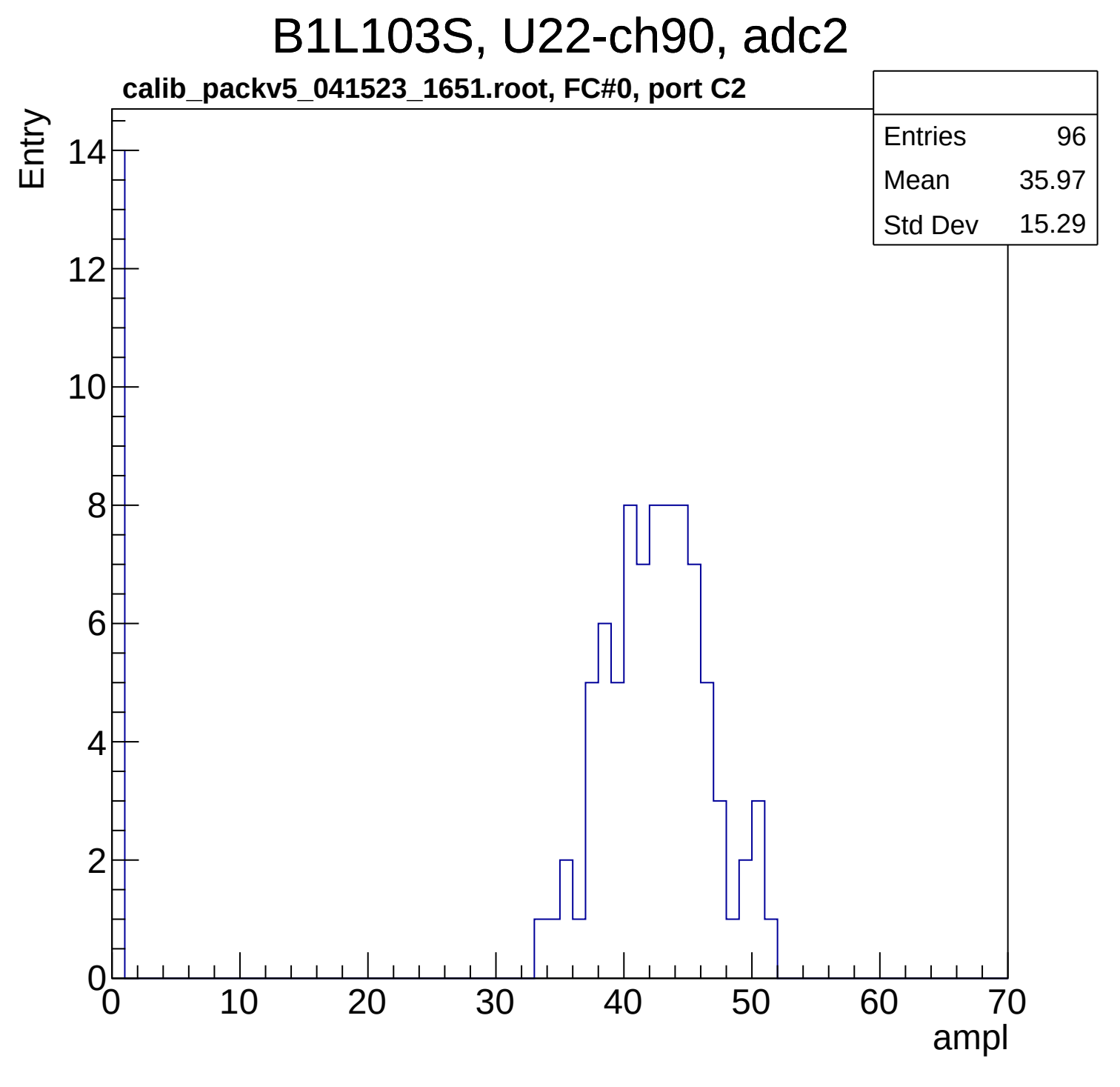
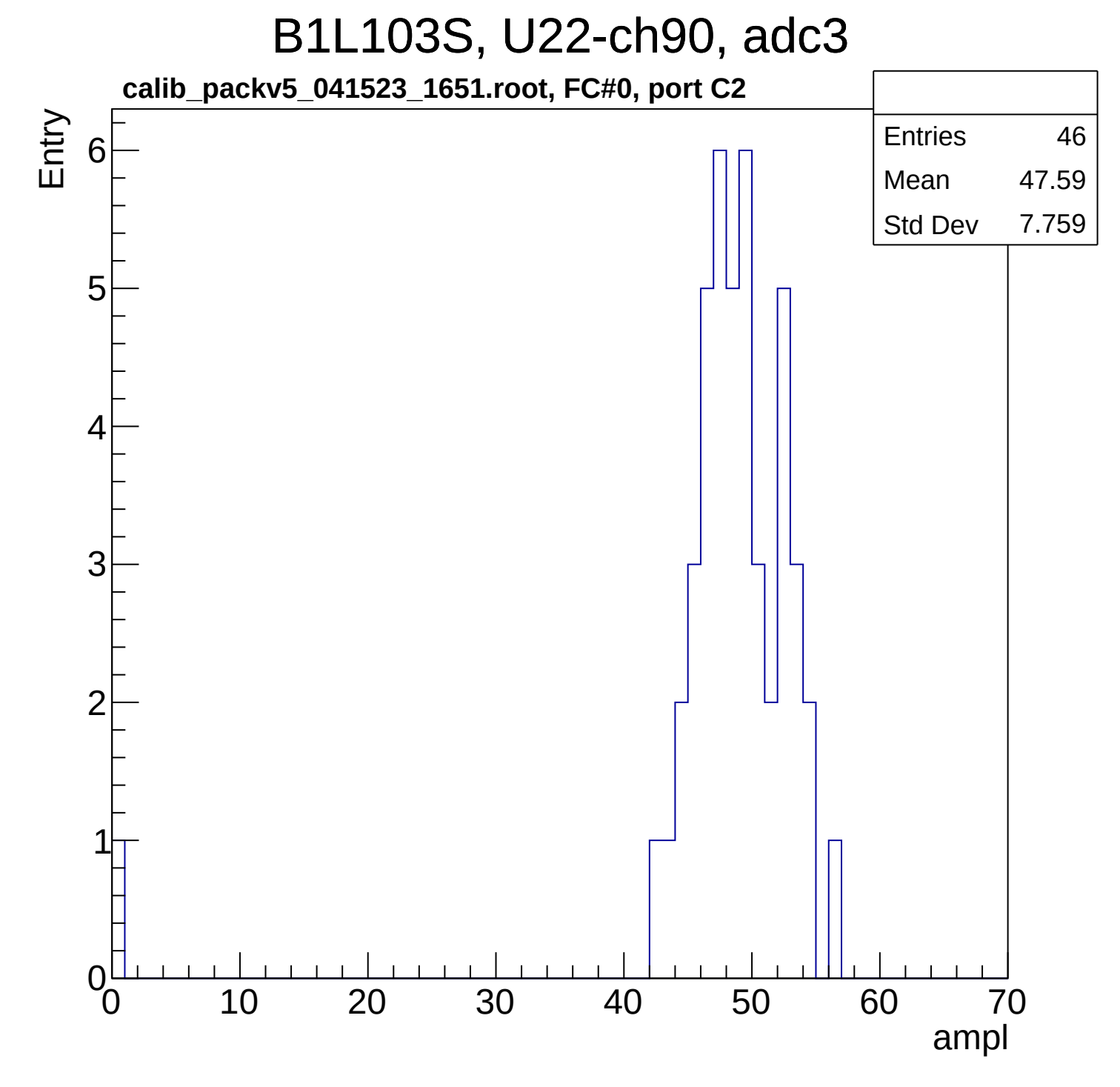
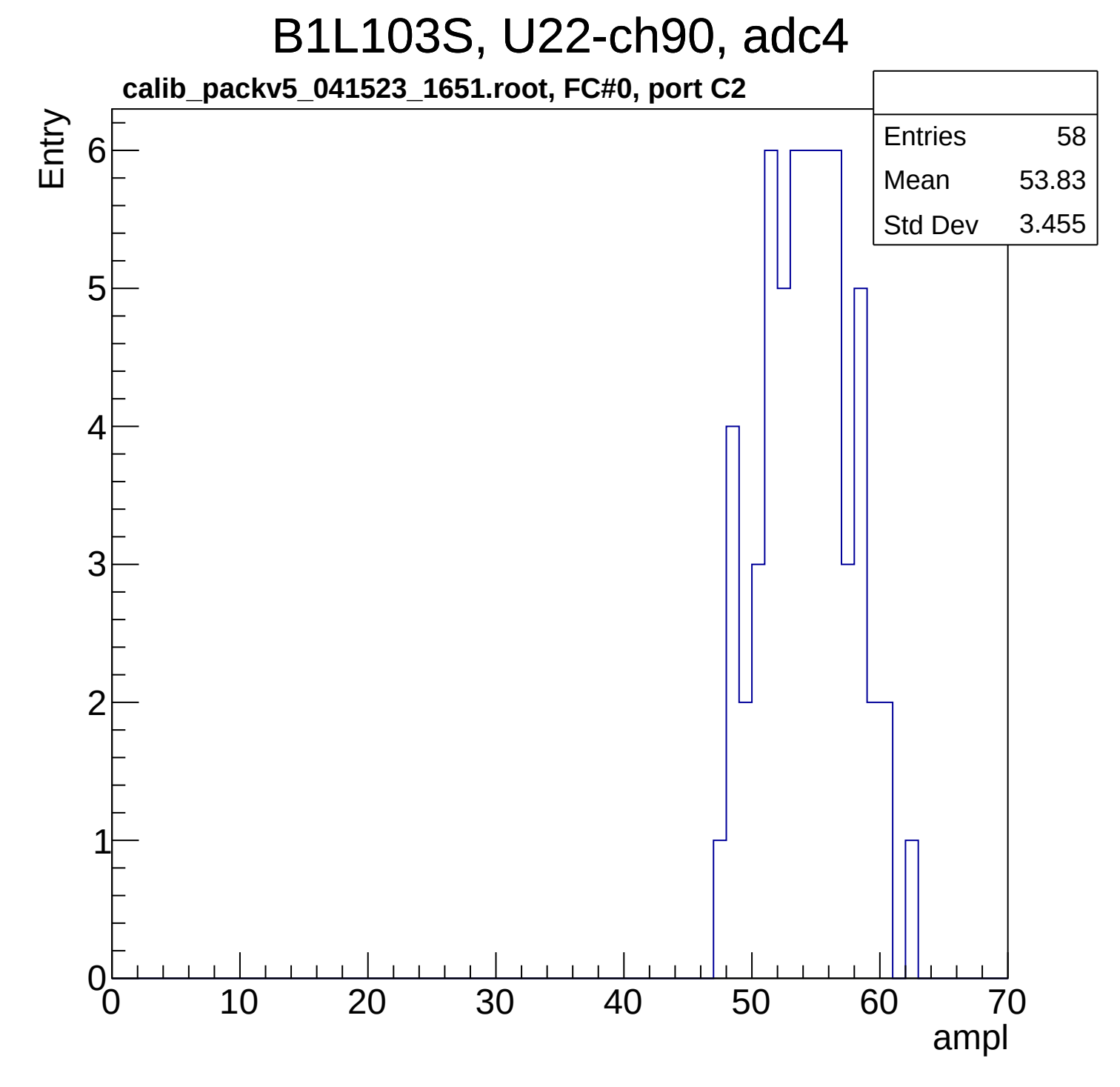
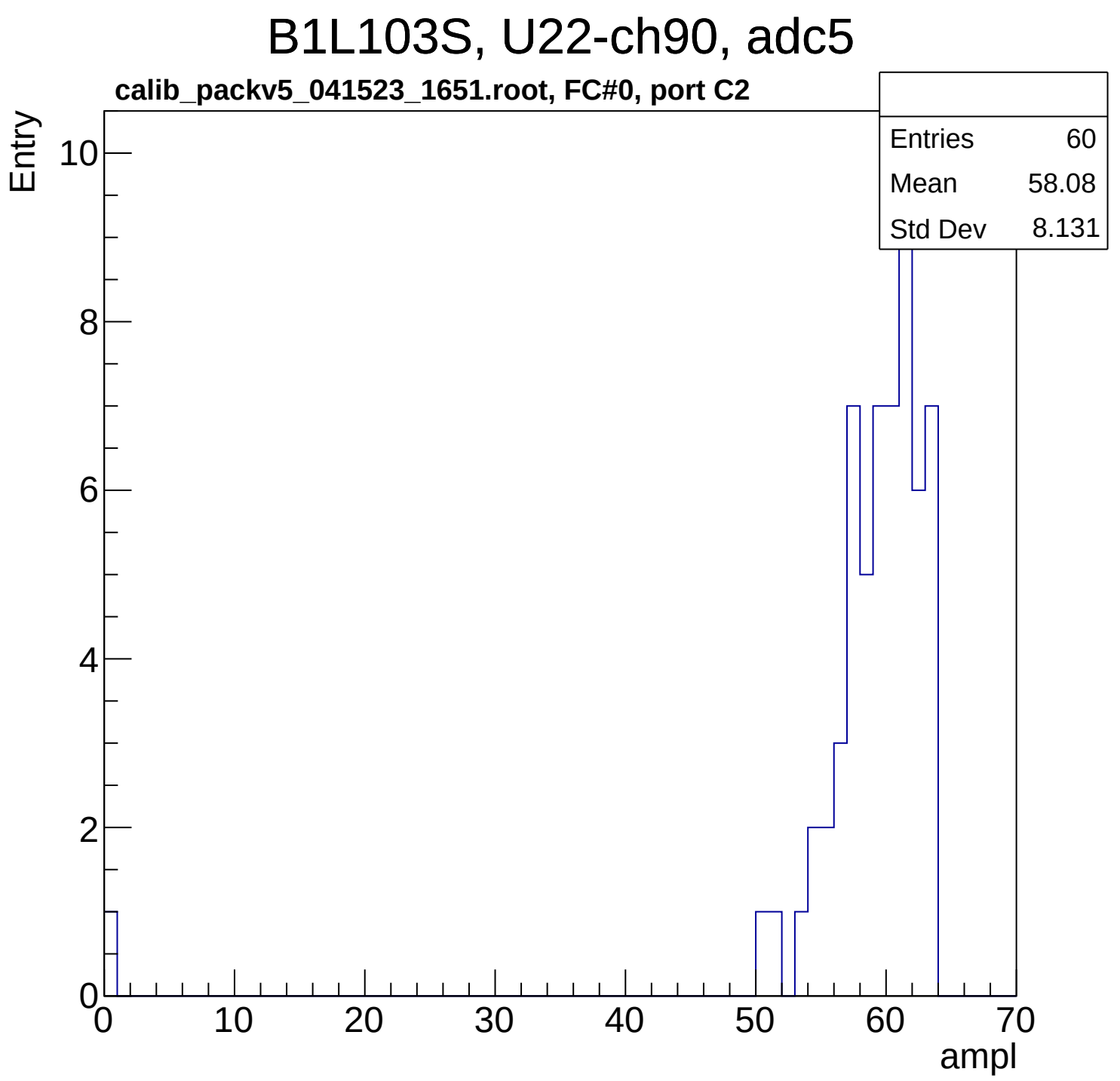
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U22-ch90, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 96
Mean 35.97
Std Dev 15.29
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch90, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 47.59
Std Dev 7.759
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U22-ch90, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 53.83
Std Dev 3.455
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch90, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 58.08
Std Dev 8.131
Entry
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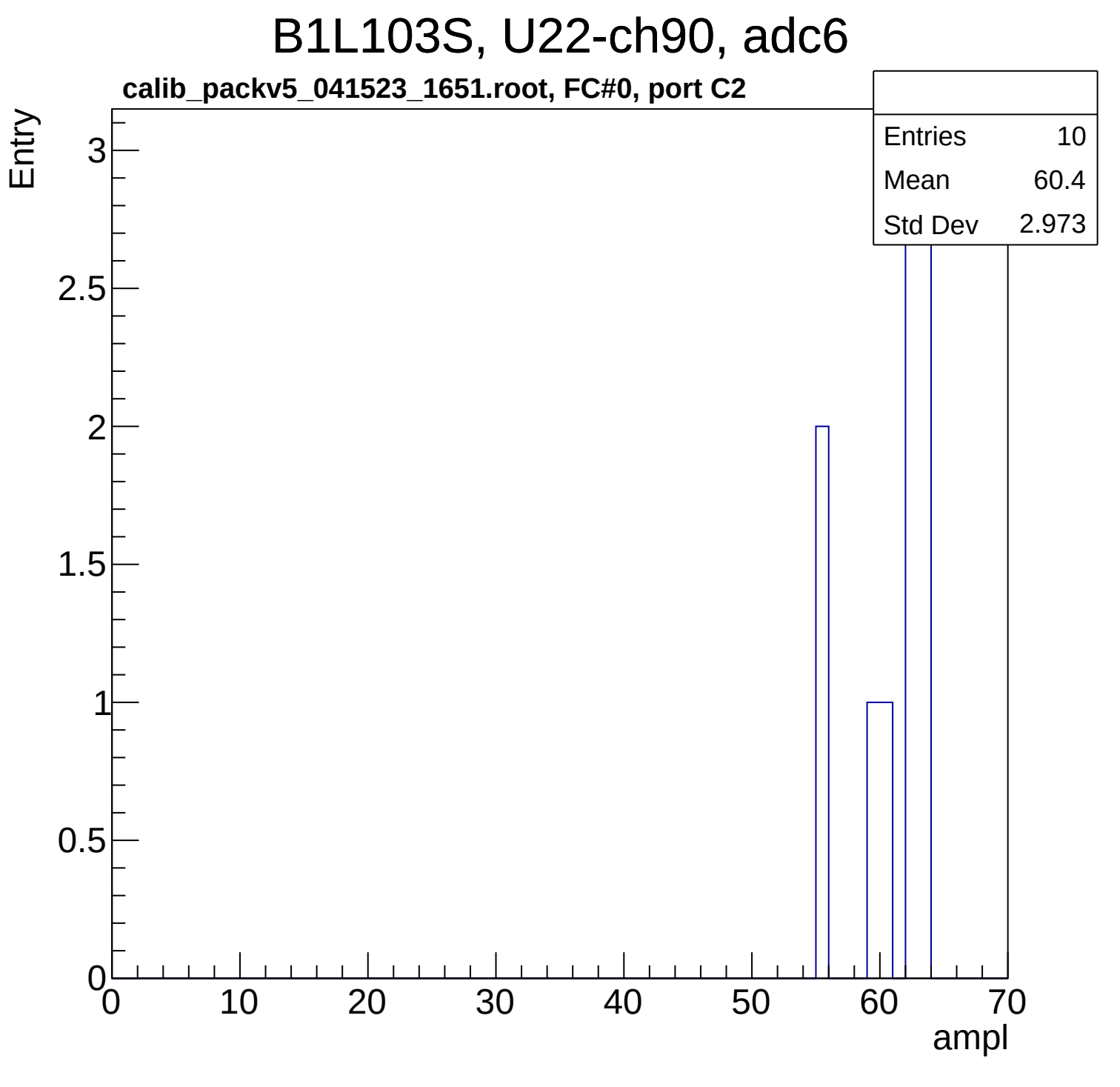
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch90, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 60.4
Std Dev 2.973
Entry
ampl
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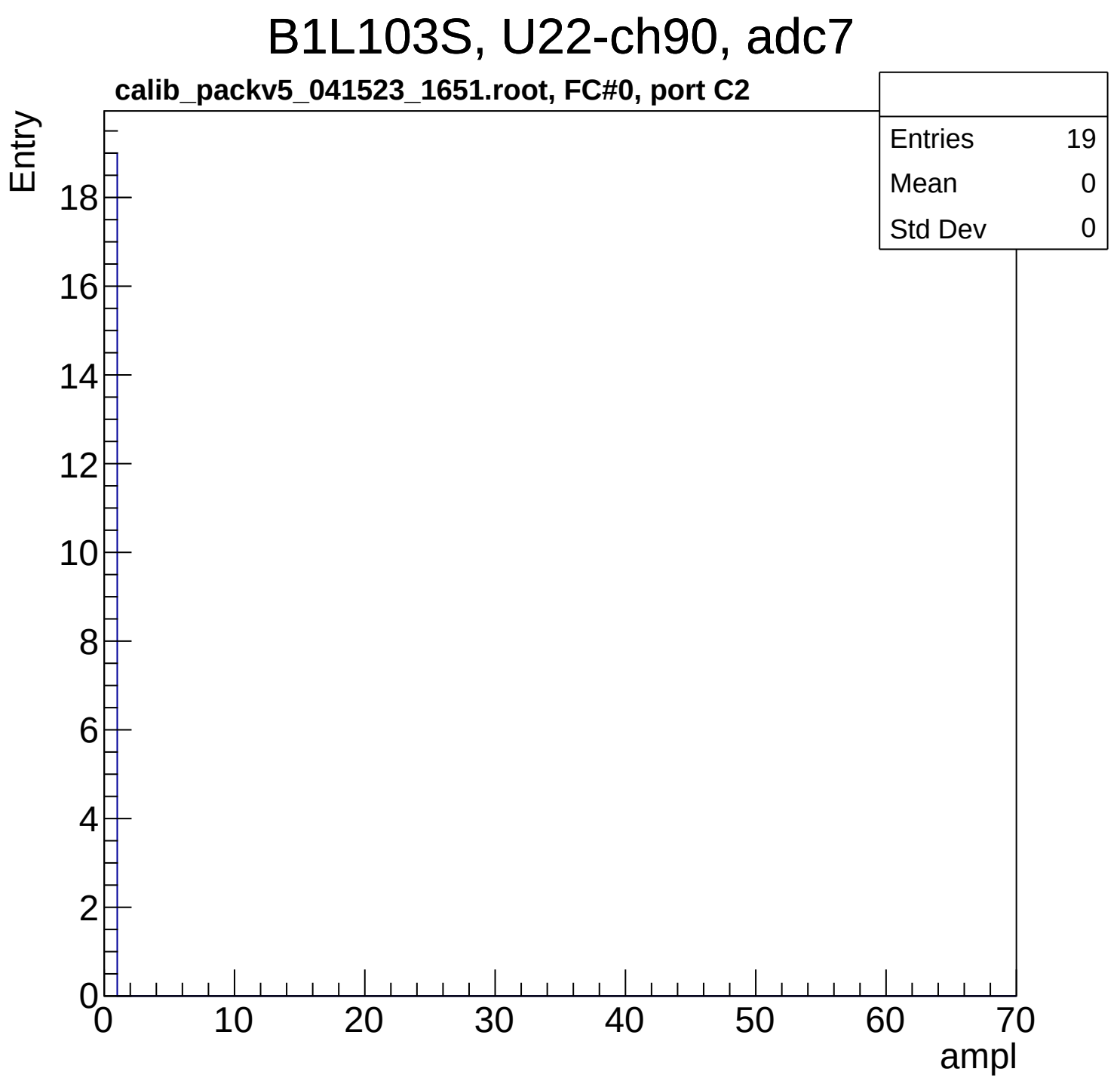
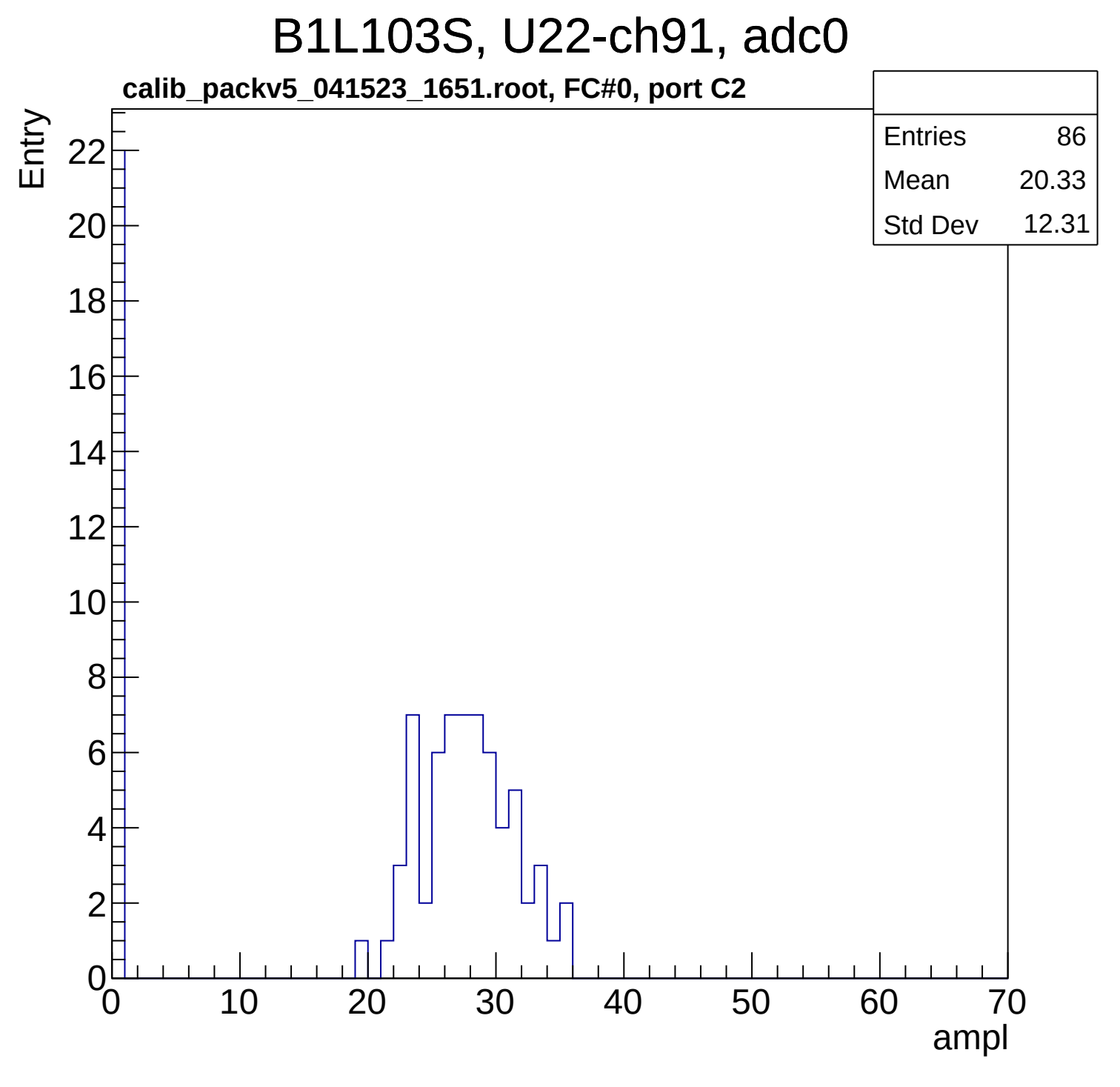
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U22-ch90, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch91, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 20.33
Std Dev 12.31
Entry
ampl
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6
8
10
12
14
16
18
20
22
0
10
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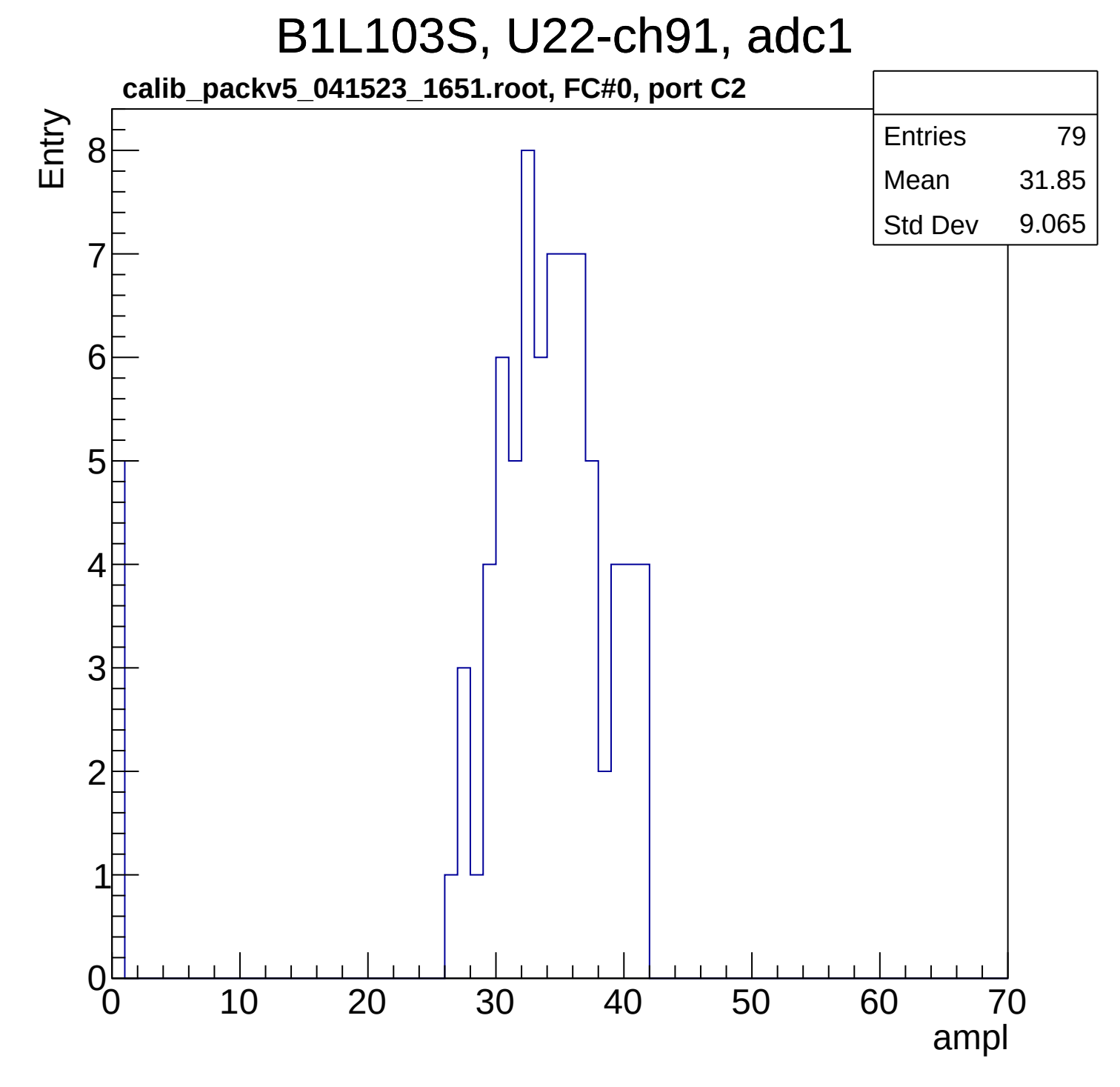
40
50
60
70


B1L103S, U22-ch91, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 31.85
Std Dev 9.065
Entry
ampl
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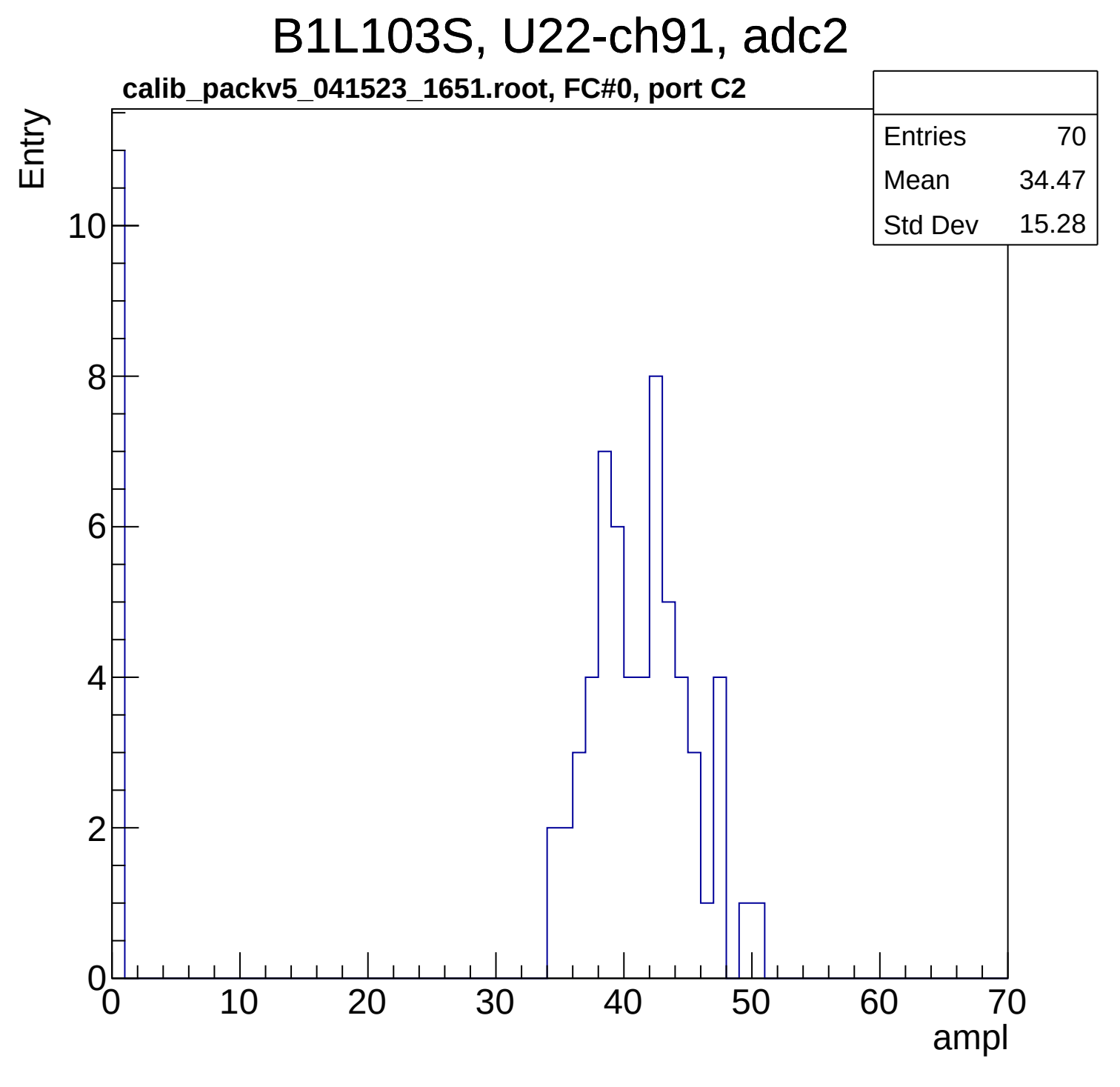
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch91, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 34.47
Std Dev 15.28
Entry
0
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4
6
8
10
0
10
20
30
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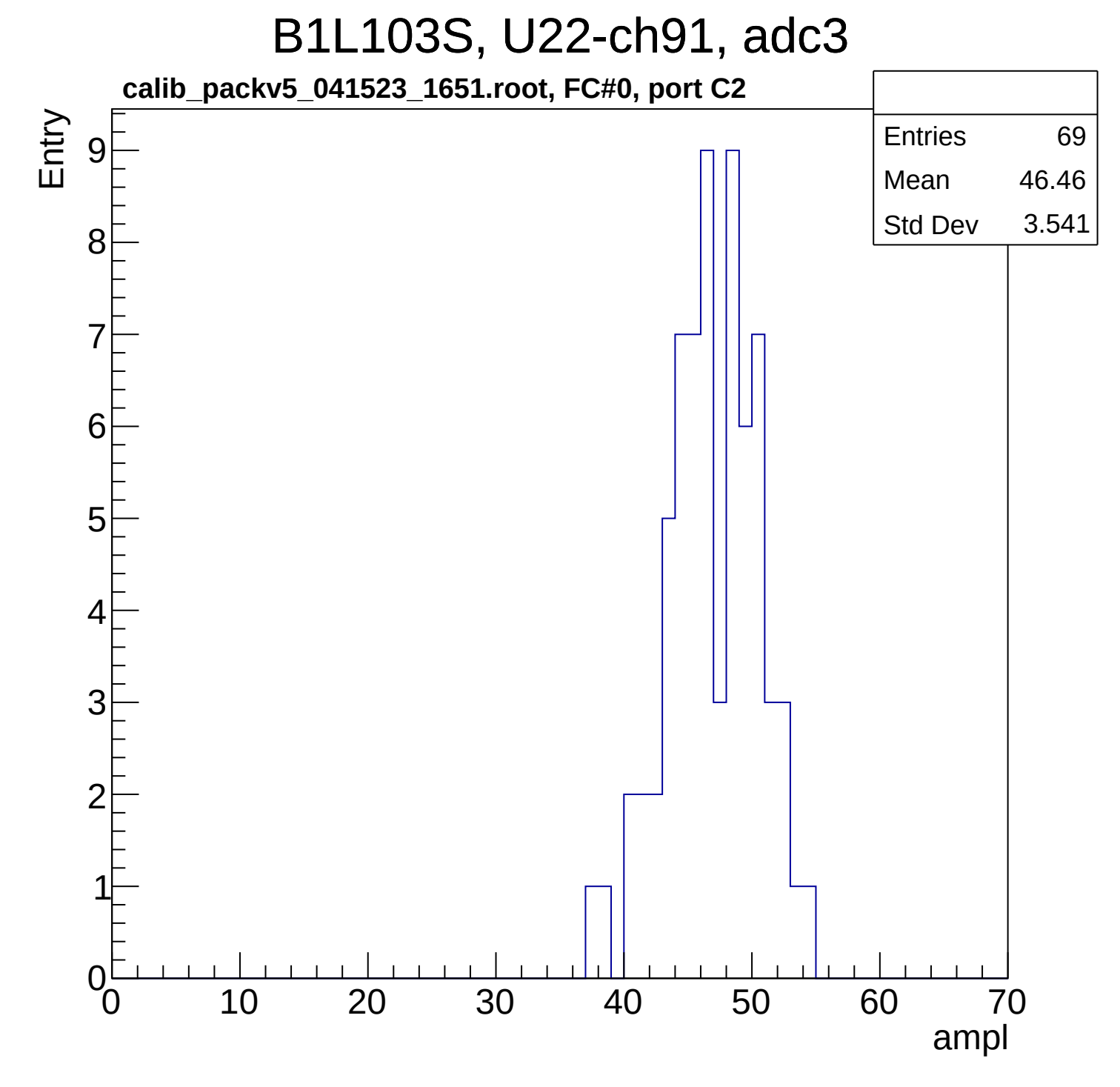
50
60
70
ampl


B1L103S, U22-ch91, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 46.46
Std Dev 3.541
Entry
ampl
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2
3
4
5
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7
8
9
0
10
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40
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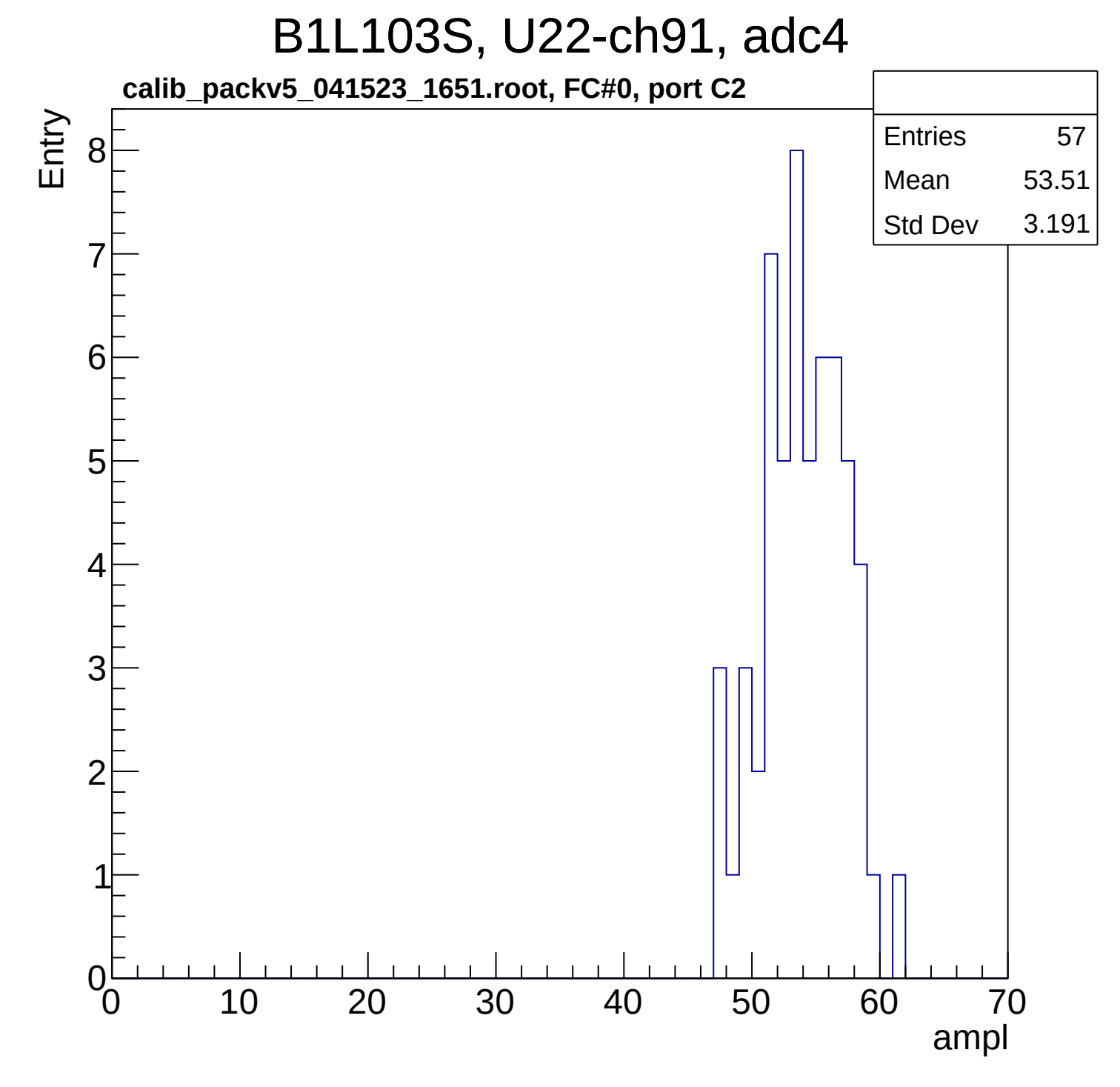
60
70


B1L103S, U22-ch91, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 53.51
Std Dev 3.191
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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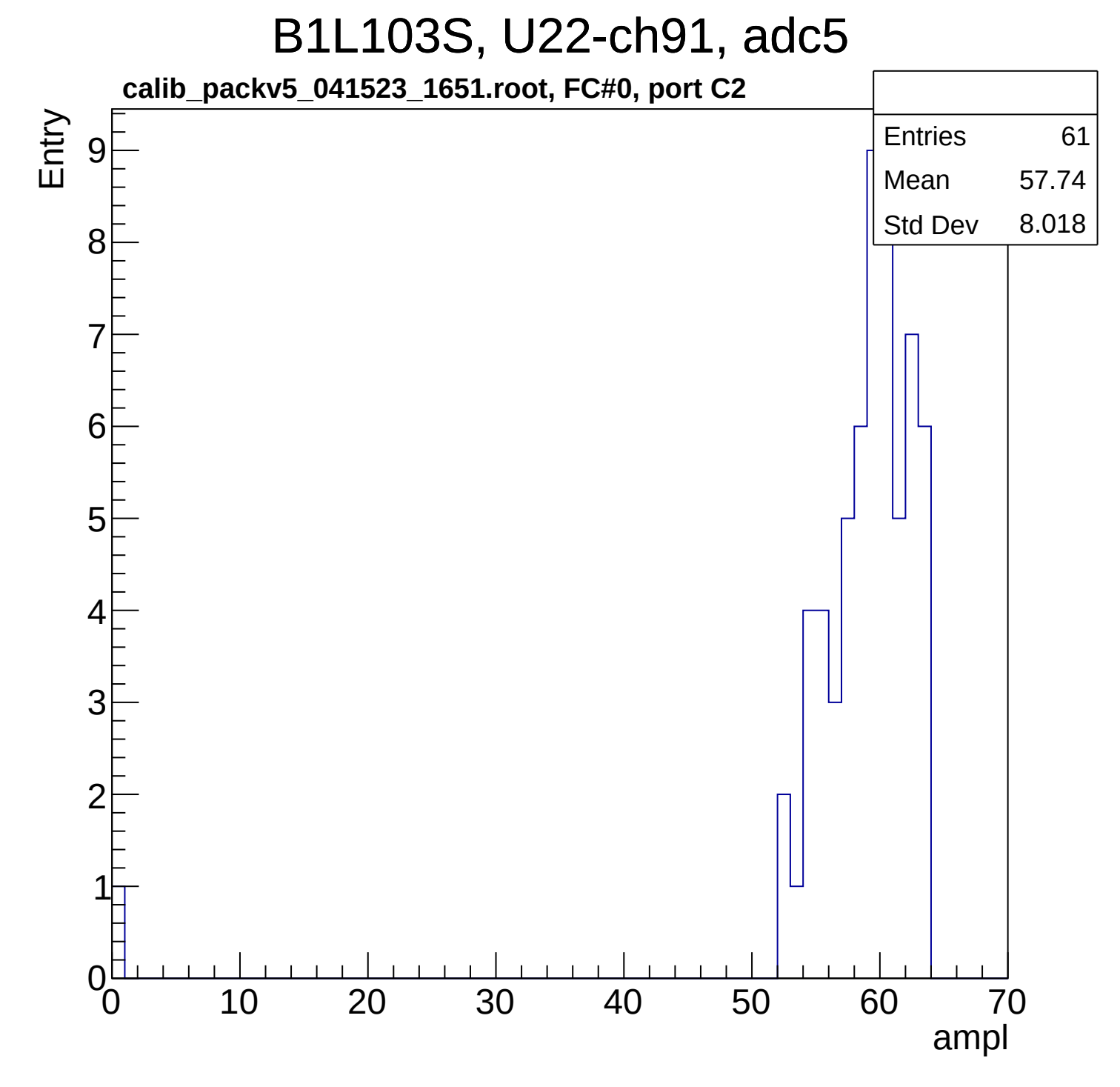
B1L103S, U22-ch91, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 57.74
Std Dev 8.018
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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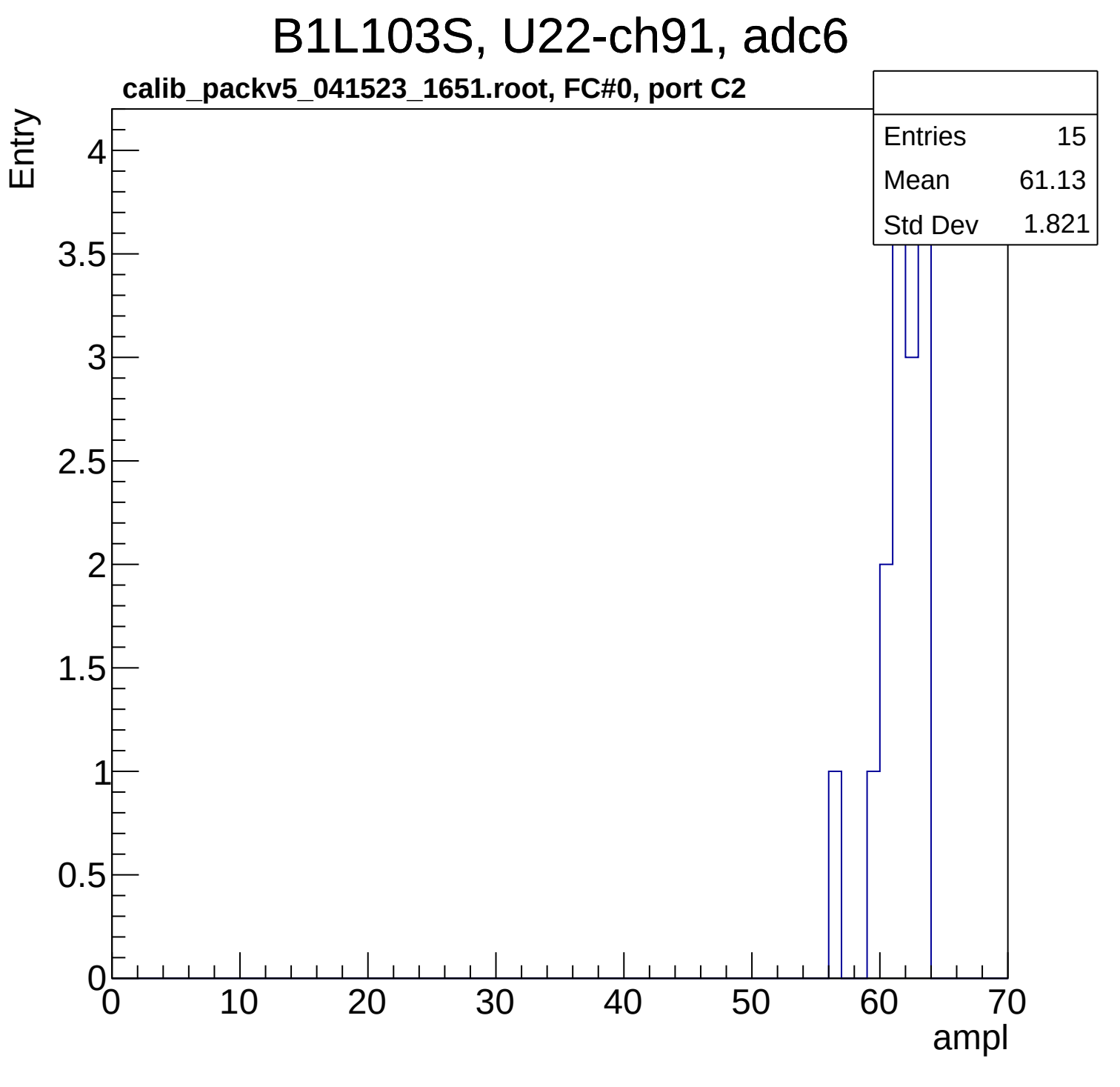
B1L103S, U22-ch91, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 61.13
Std Dev 1.821
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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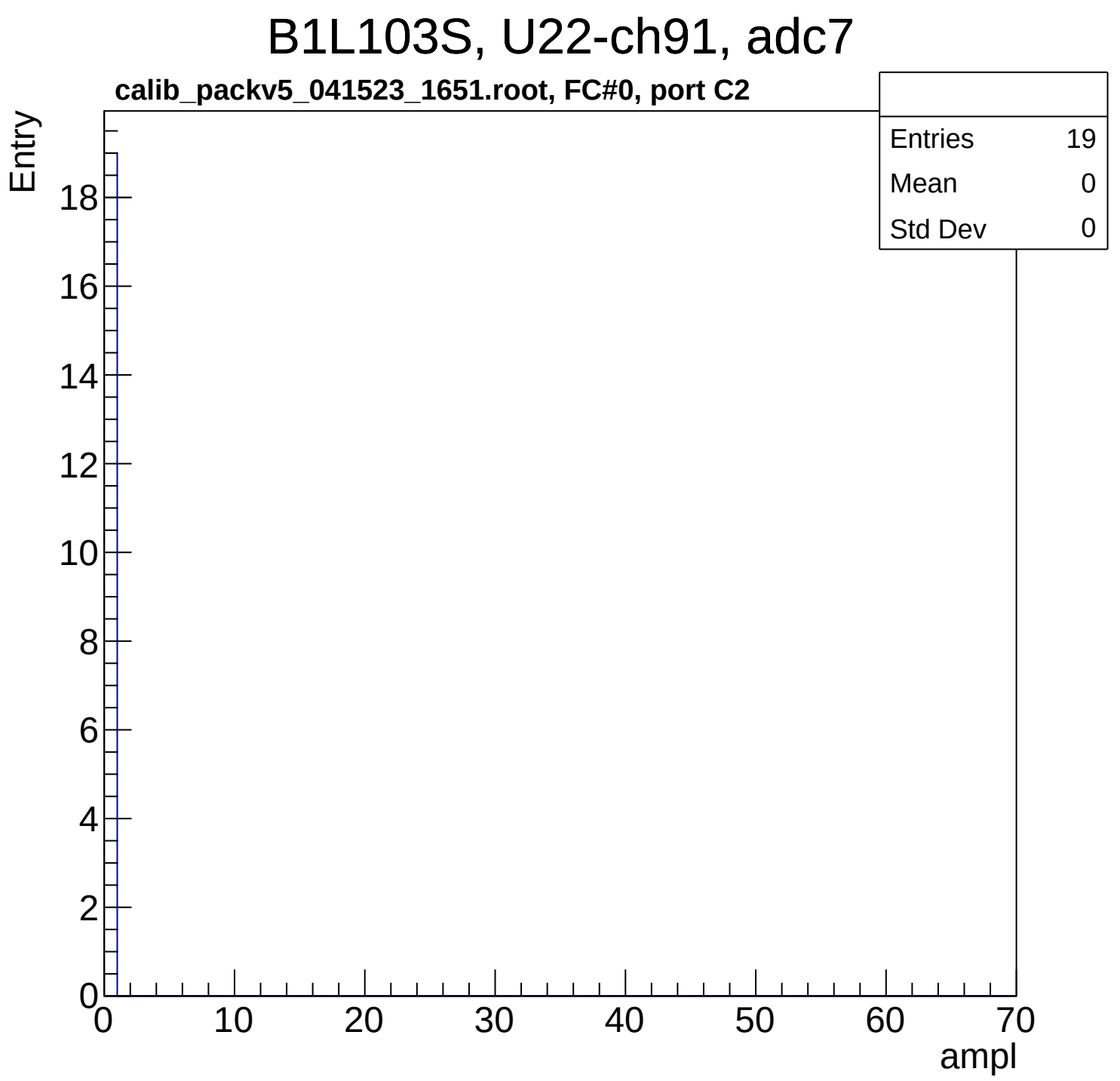
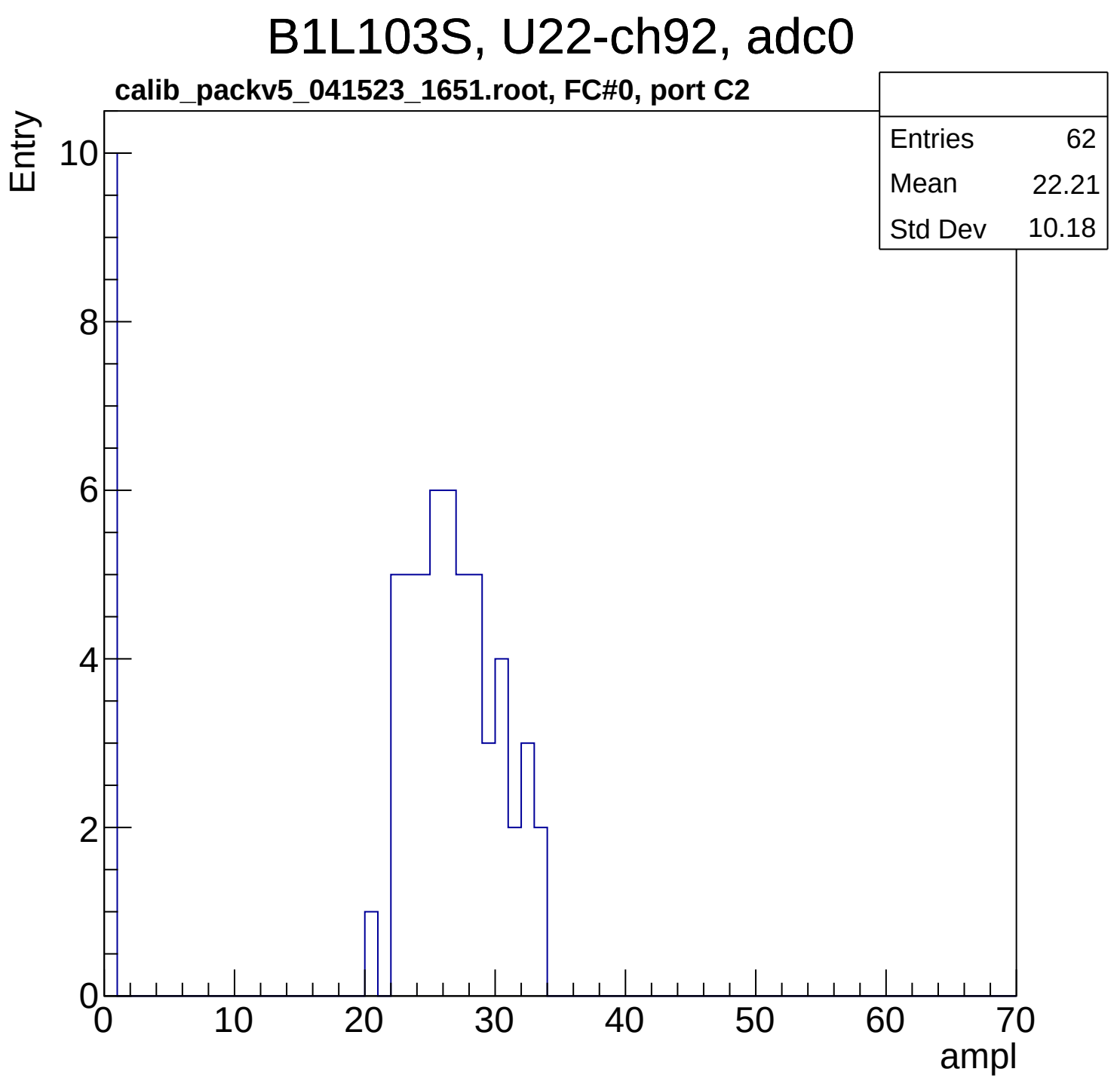
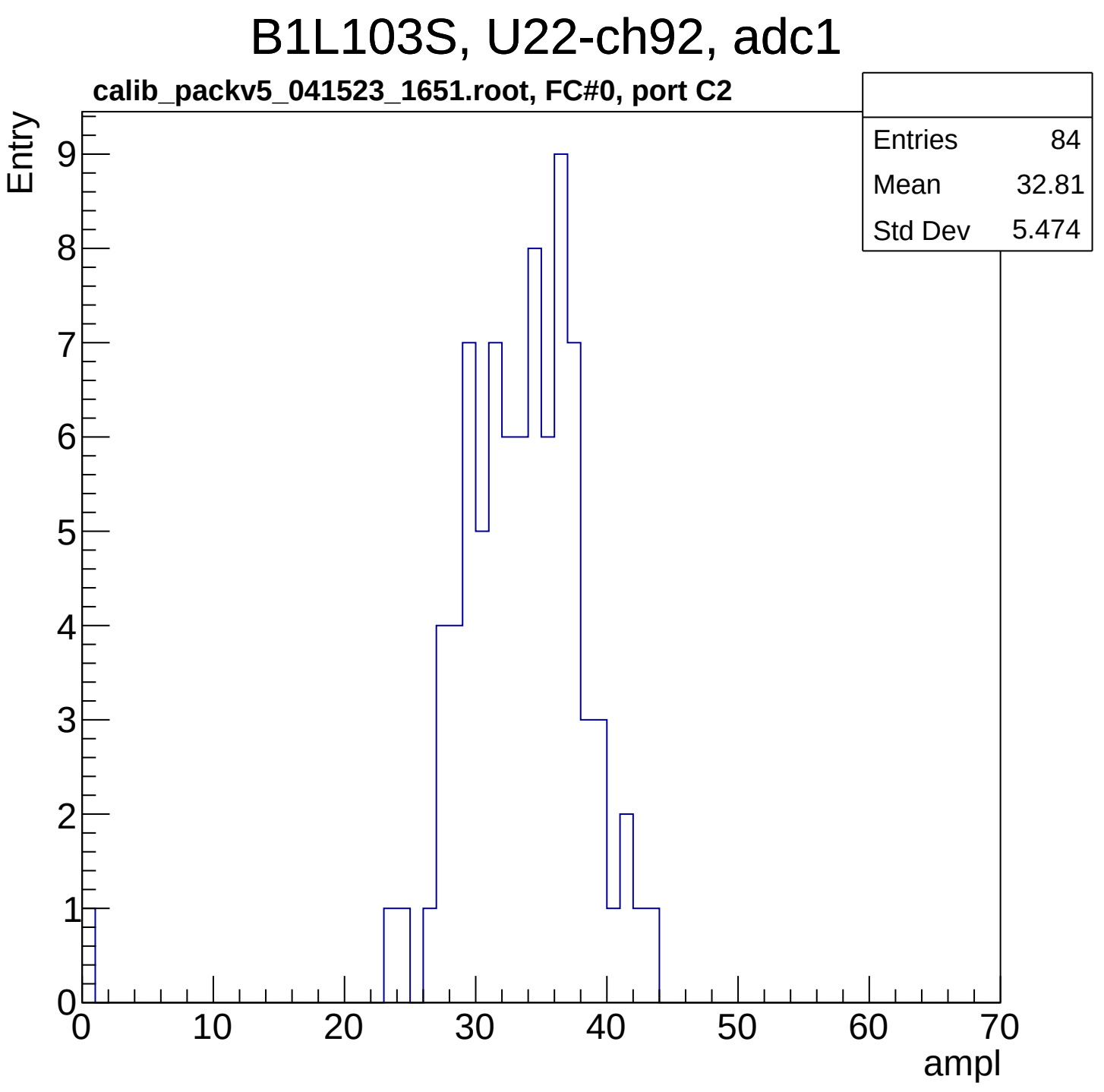
40
50
60
70


B1L103S, U22-ch91, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch92, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 22.21
Std Dev 10.18
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch92, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 32.81
Std Dev 5.474
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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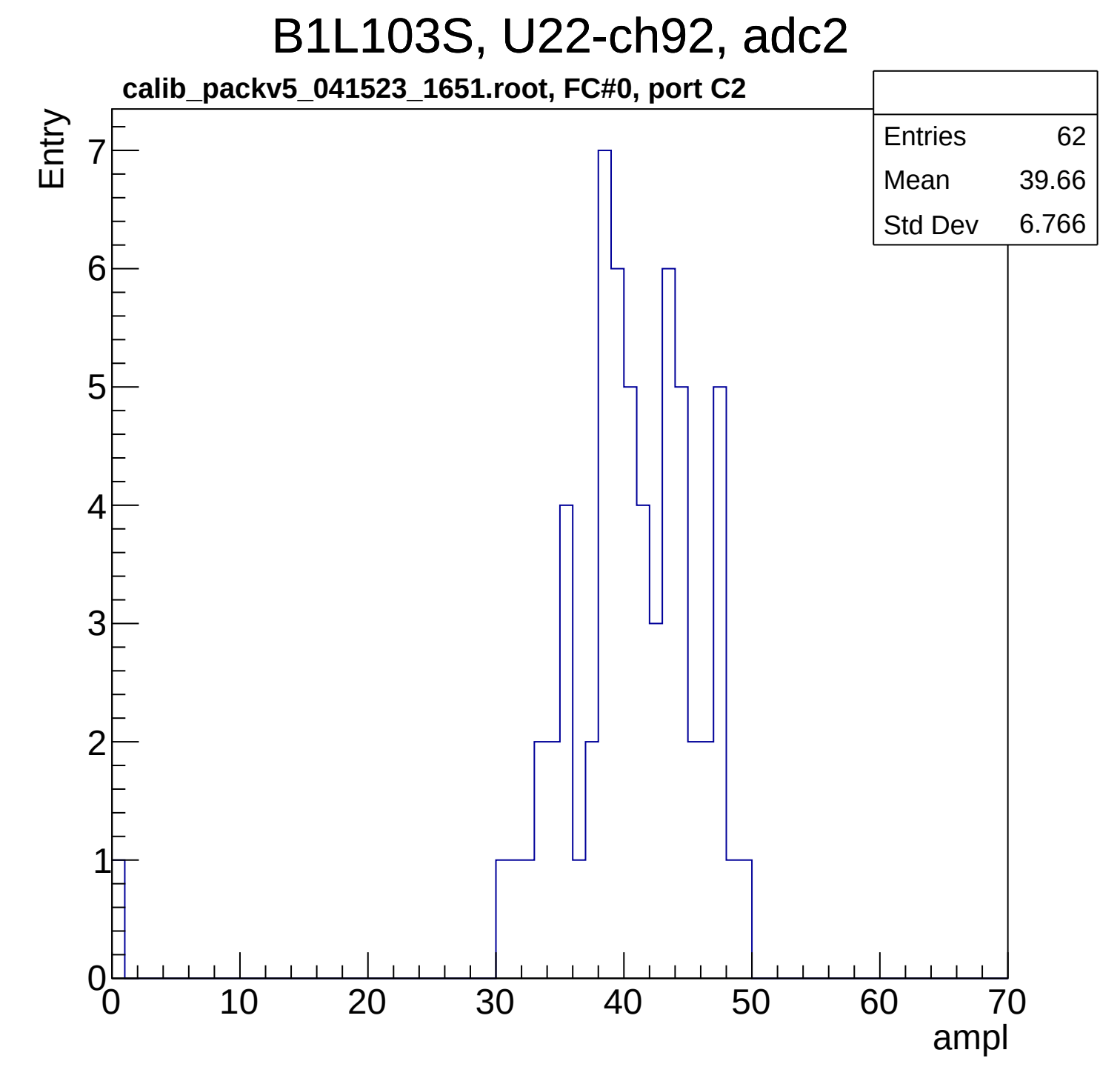
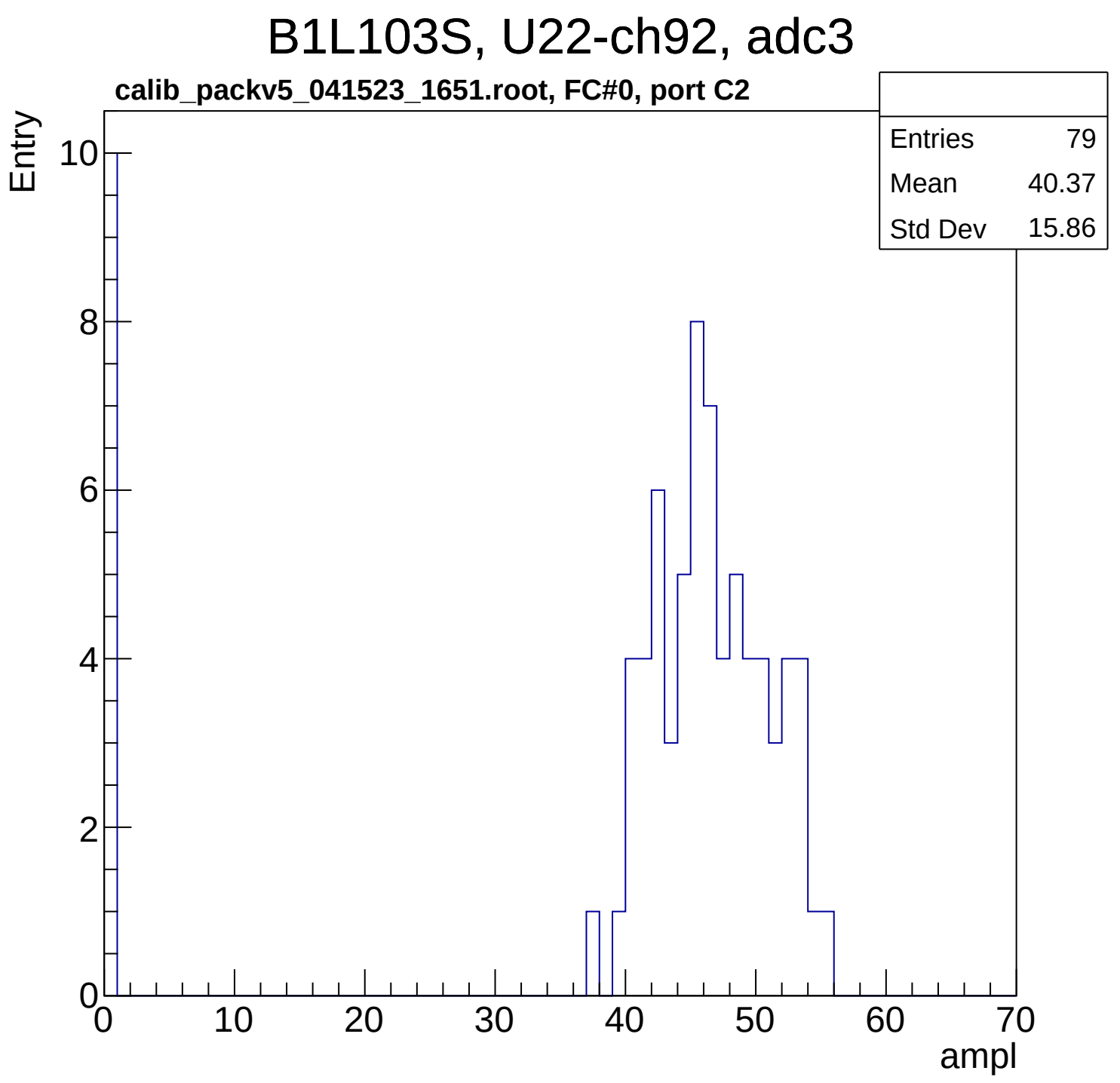
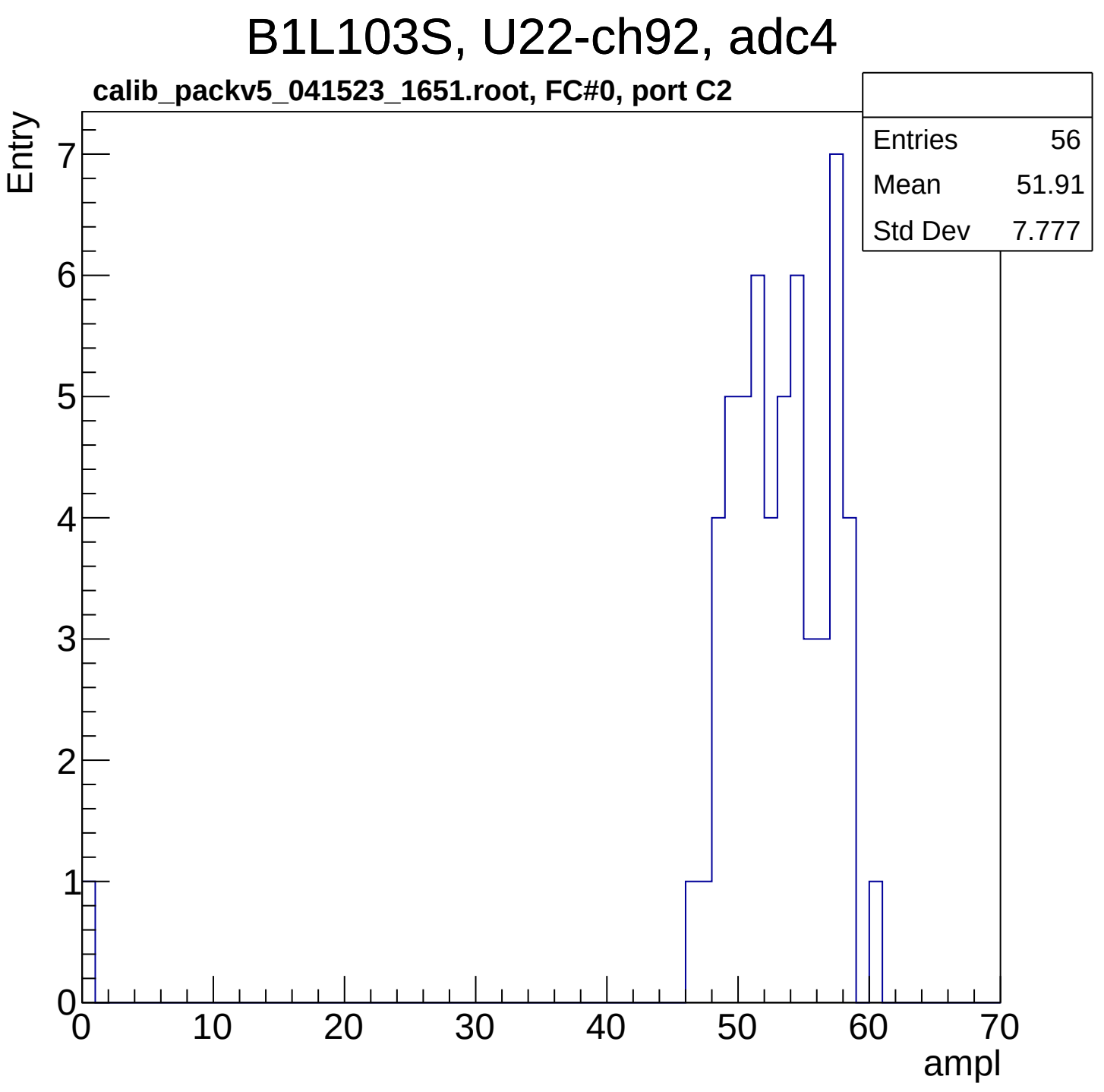

B1L103S, U22-ch92, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 39.66
Std Dev 6.766
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U22-ch92, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 40.37
Std Dev 15.86
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch92, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 51.91
Std Dev 7.777
Entry
ampl
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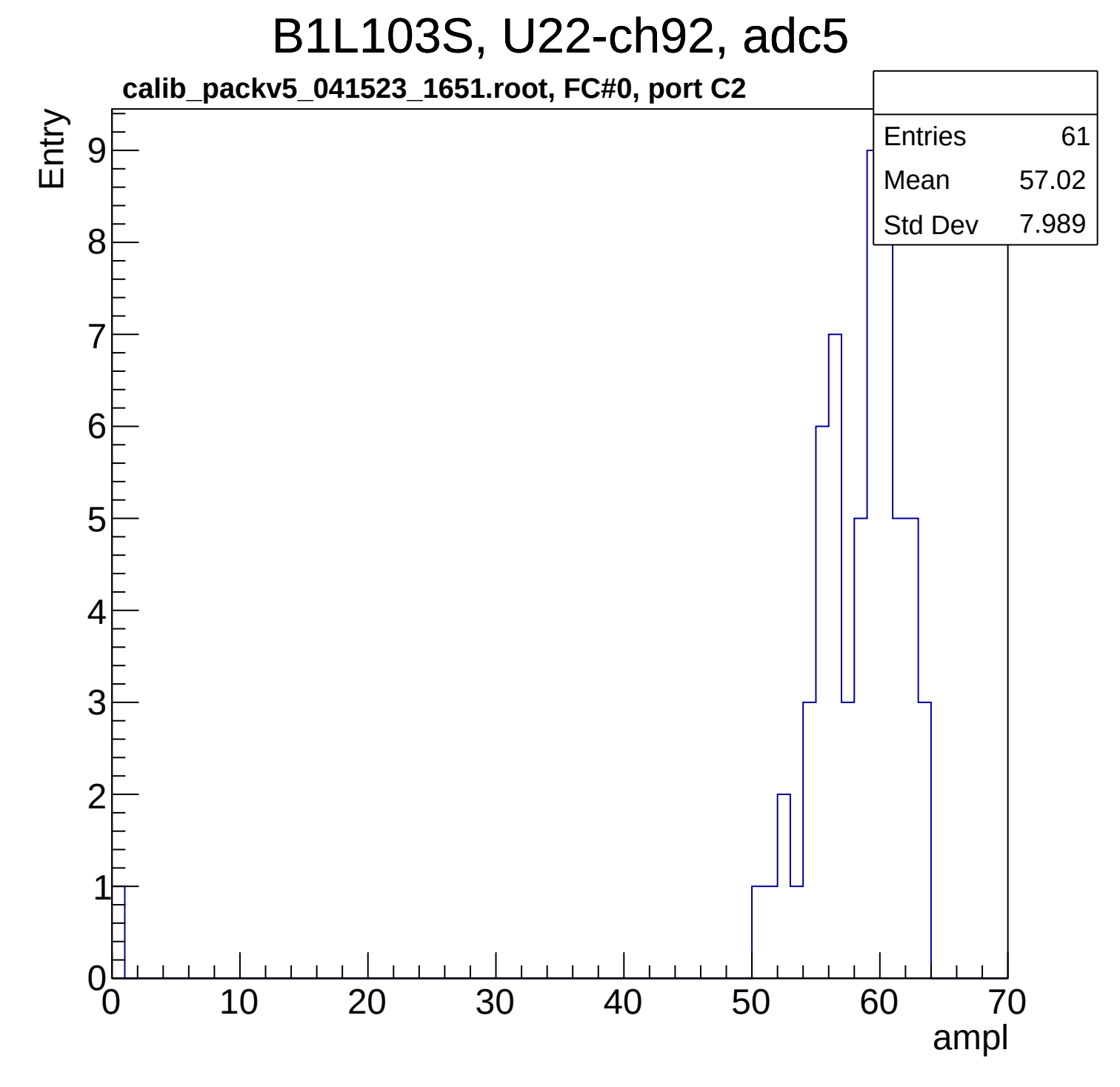
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U22-ch92, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 57.02
Std Dev 7.989
Entry
ampl
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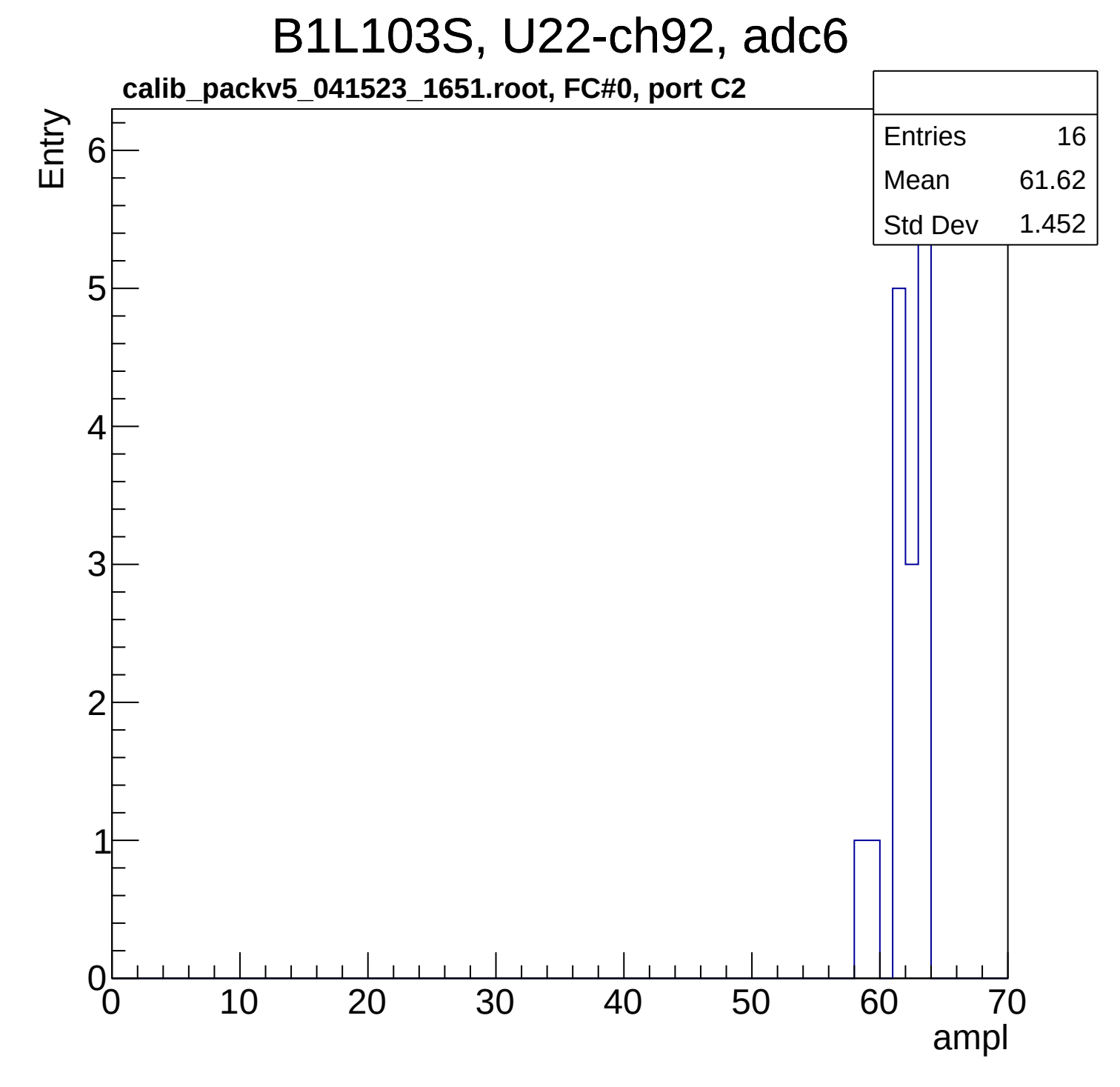
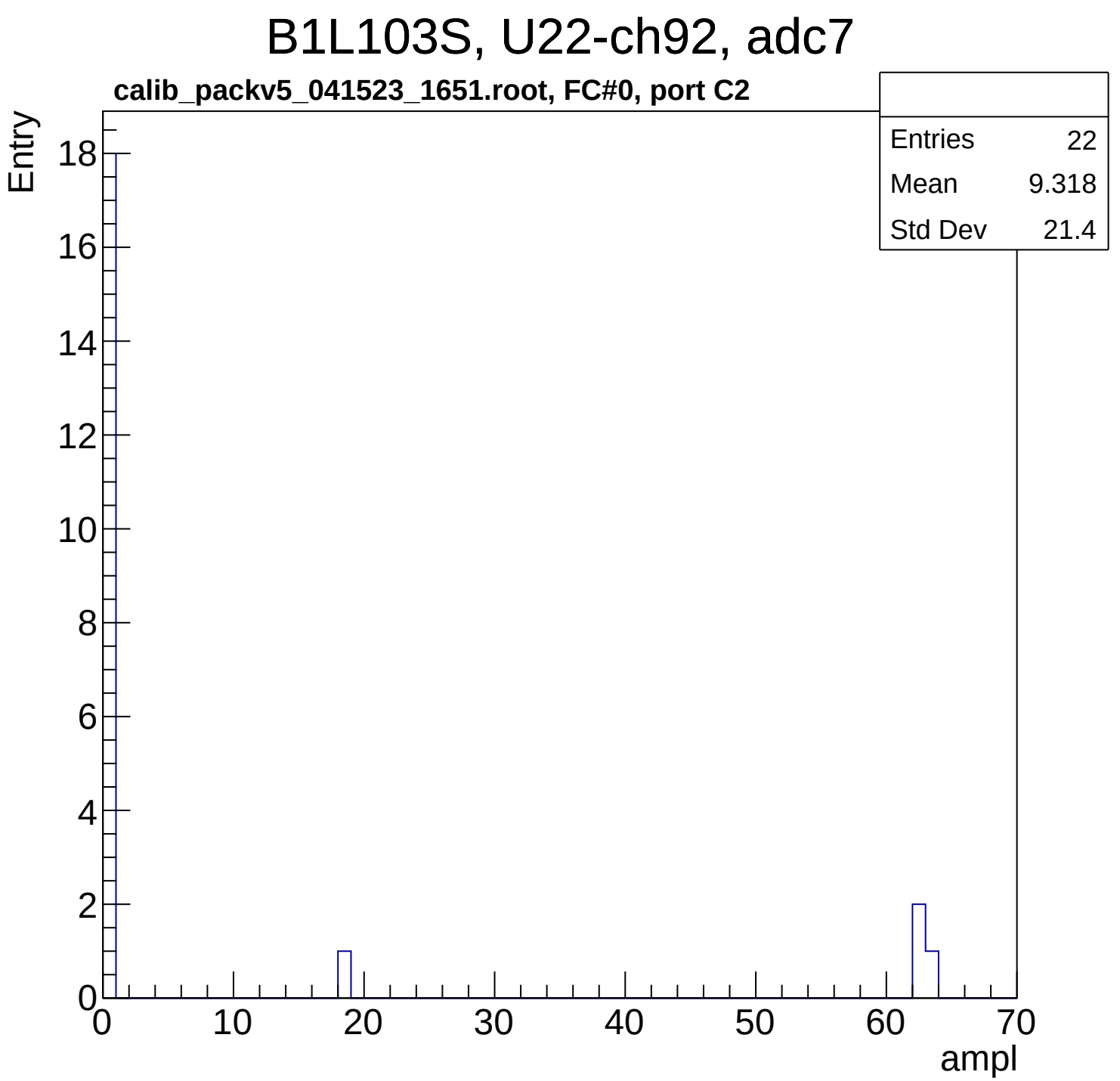
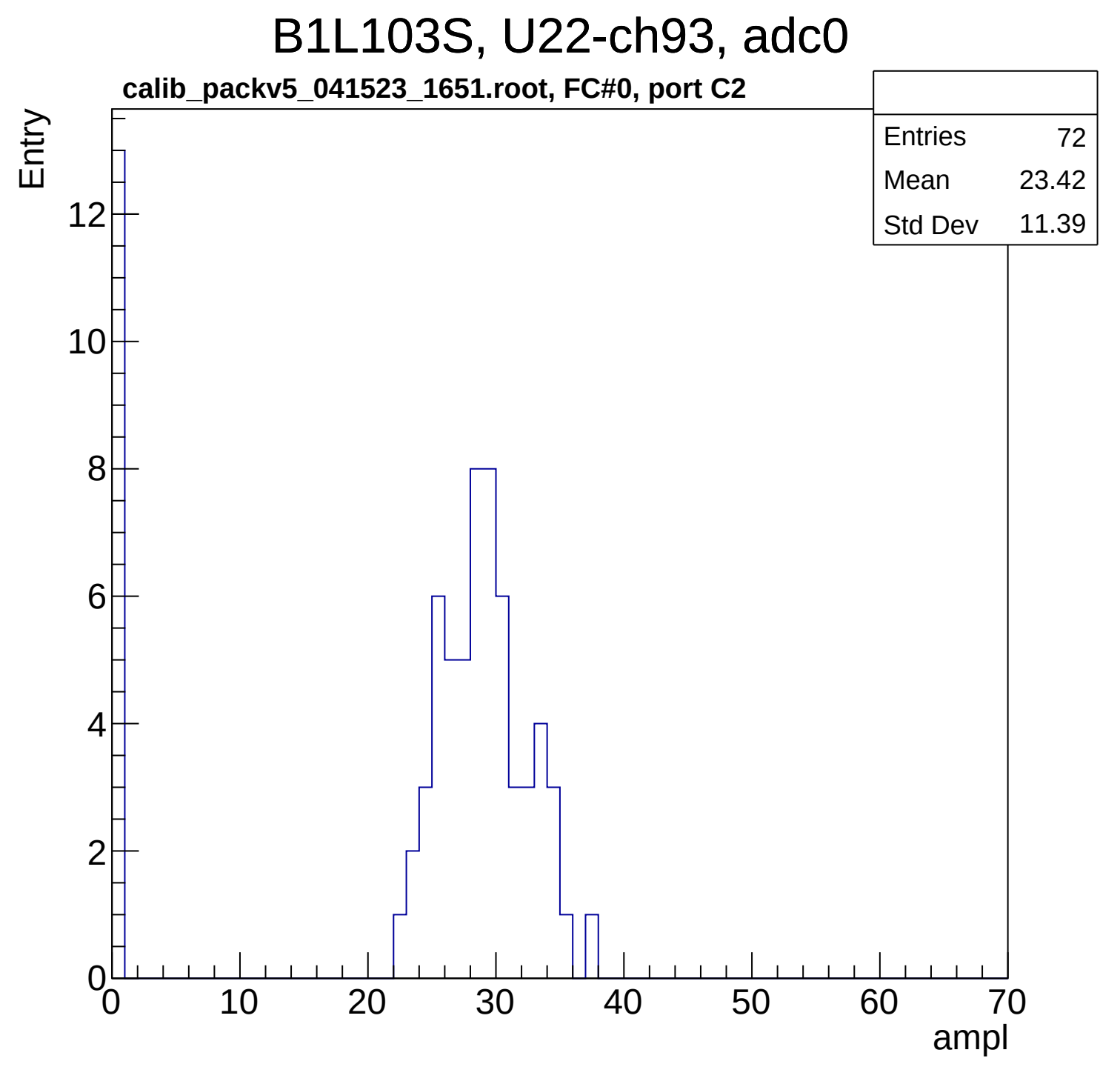
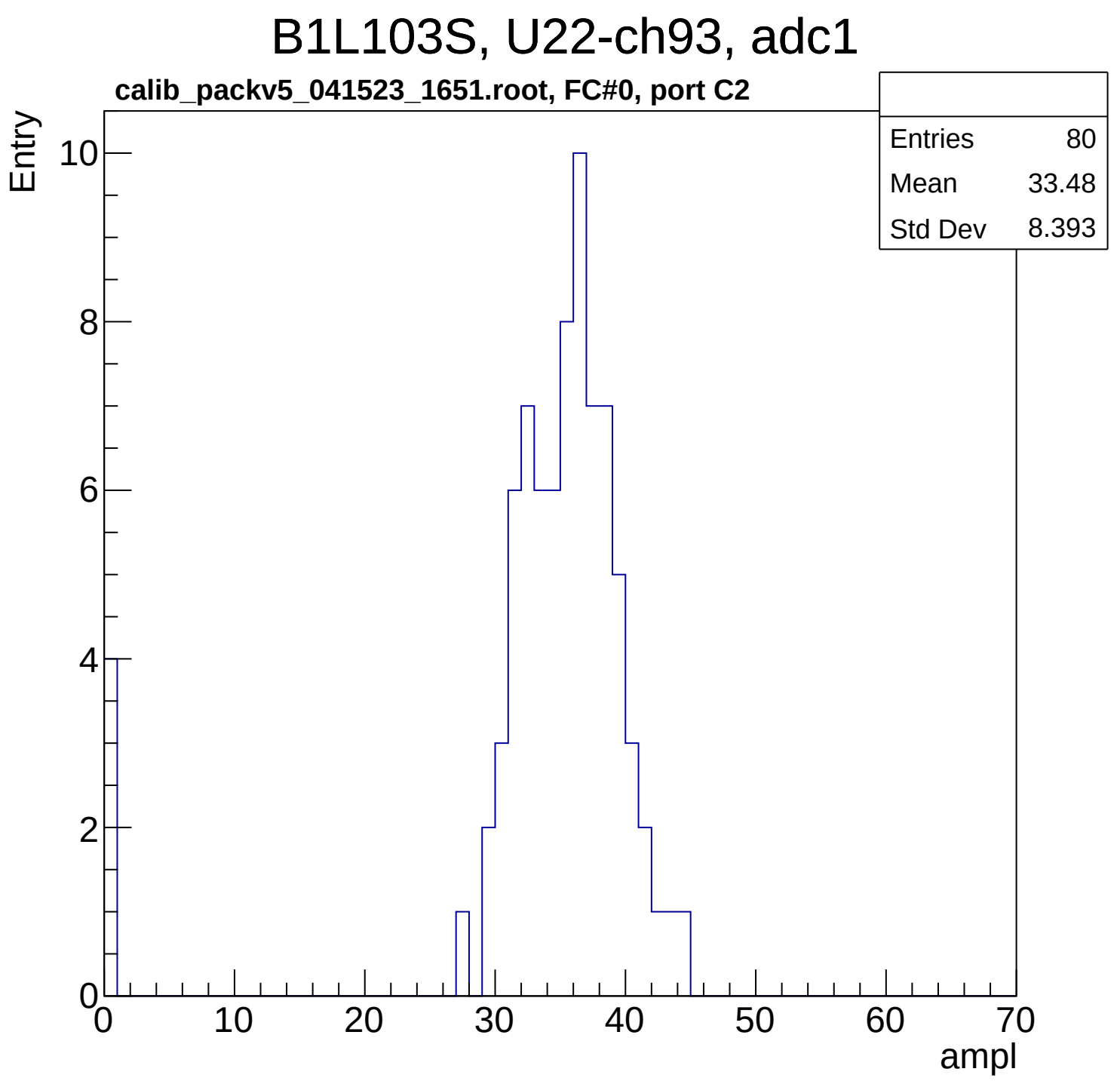
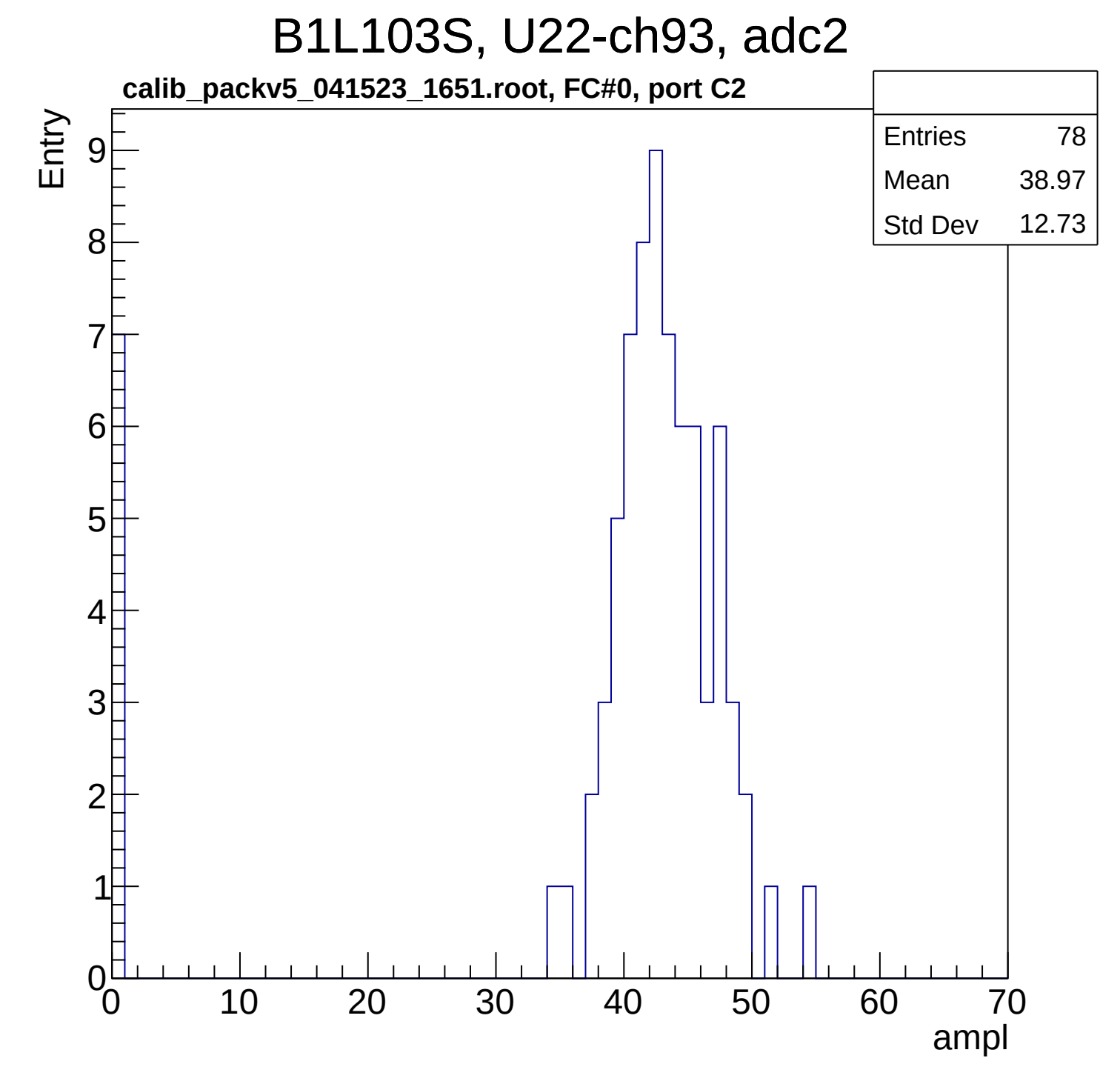
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

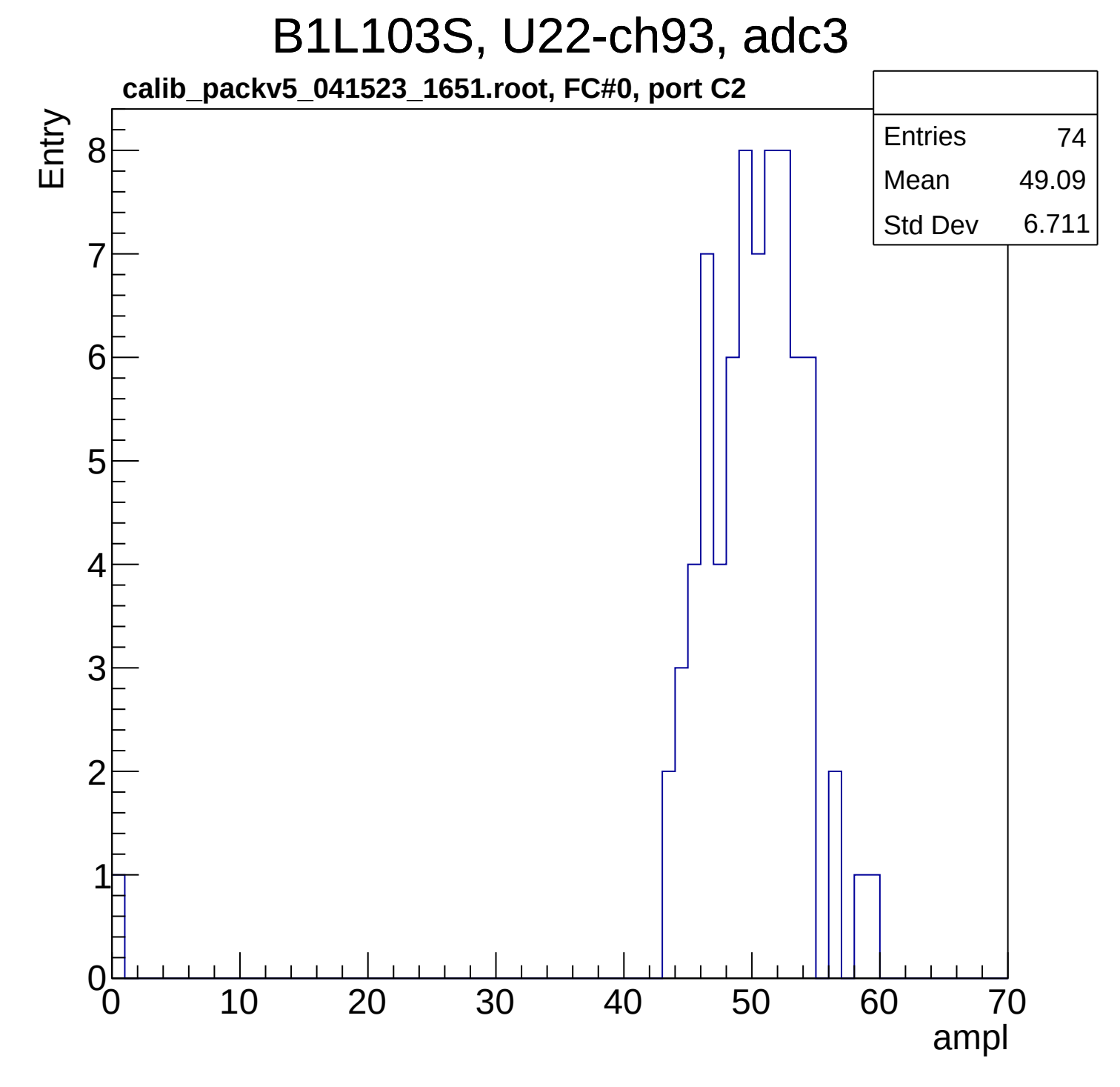

B1L103S, U22-ch92, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 61.62
Std Dev 1.452
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U22-ch92, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 9.318
Std Dev 21.4
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch93, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 23.42
Std Dev 11.39
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch93, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 33.48
Std Dev 8.393
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch93, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 38.97
Std Dev 12.73
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch93, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 49.09
Std Dev 6.711
Entry
ampl
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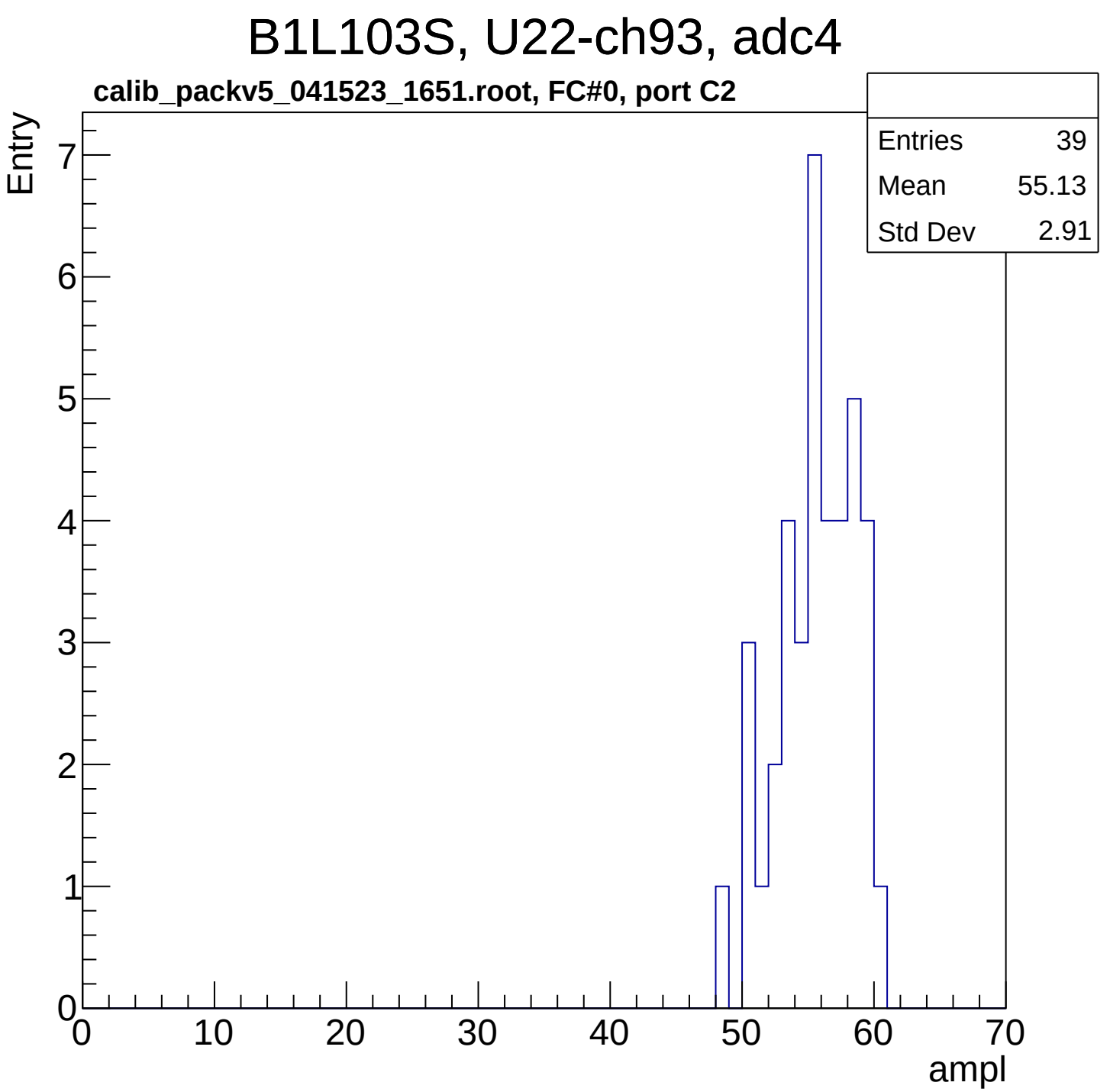
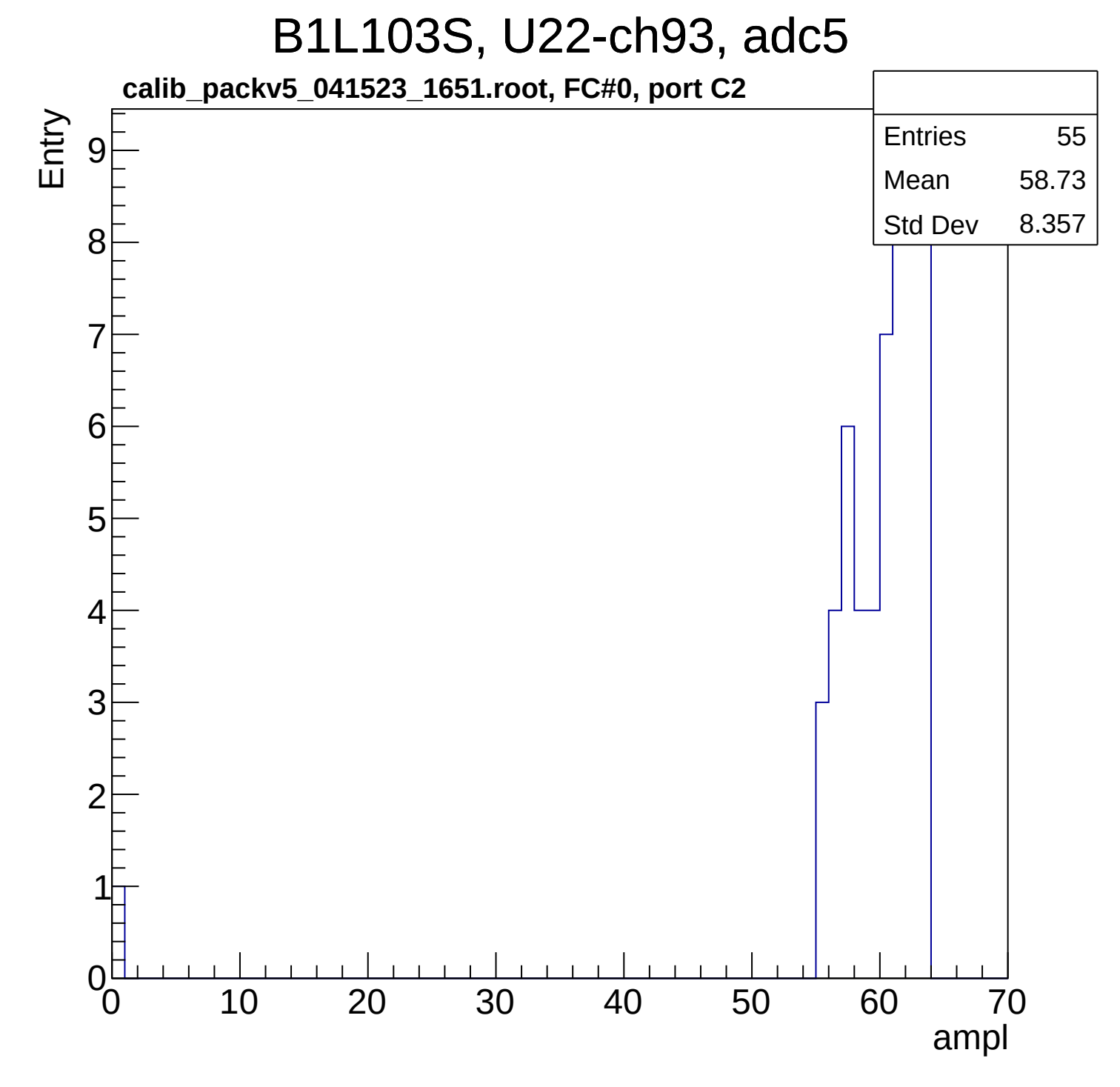
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch93, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 55.13
Std Dev 2.91
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U22-ch93, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 58.73
Std Dev 8.357
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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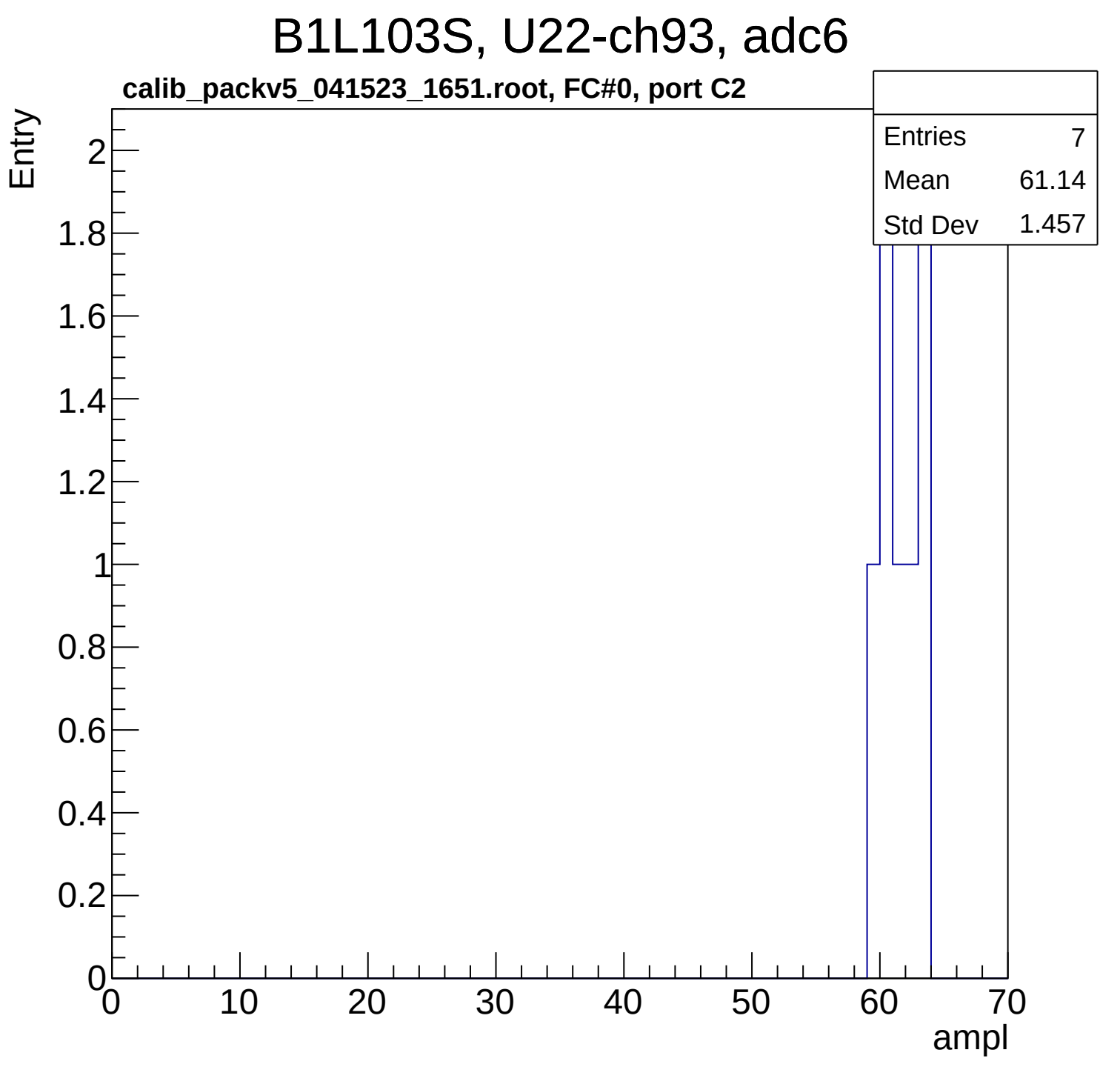
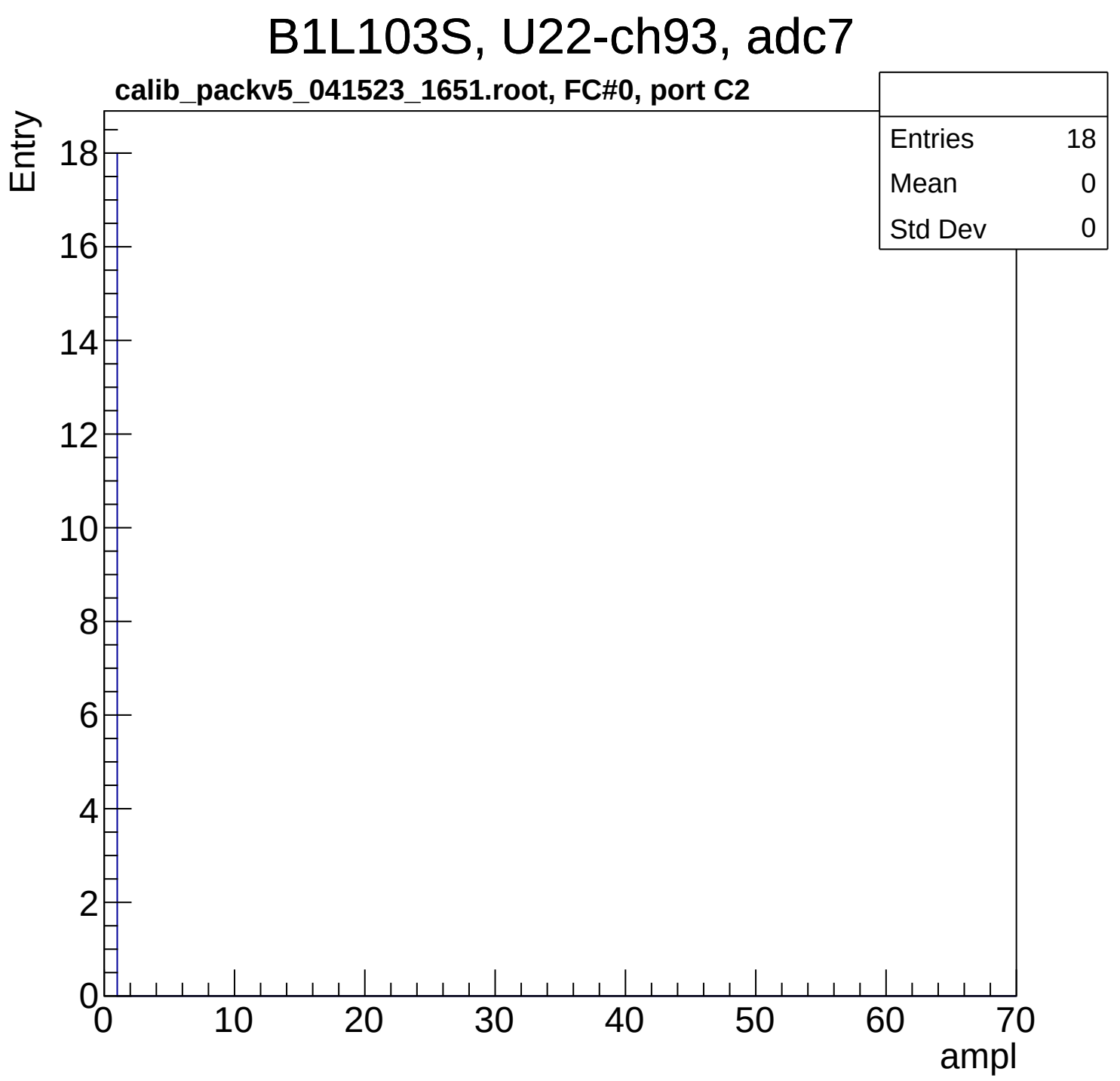
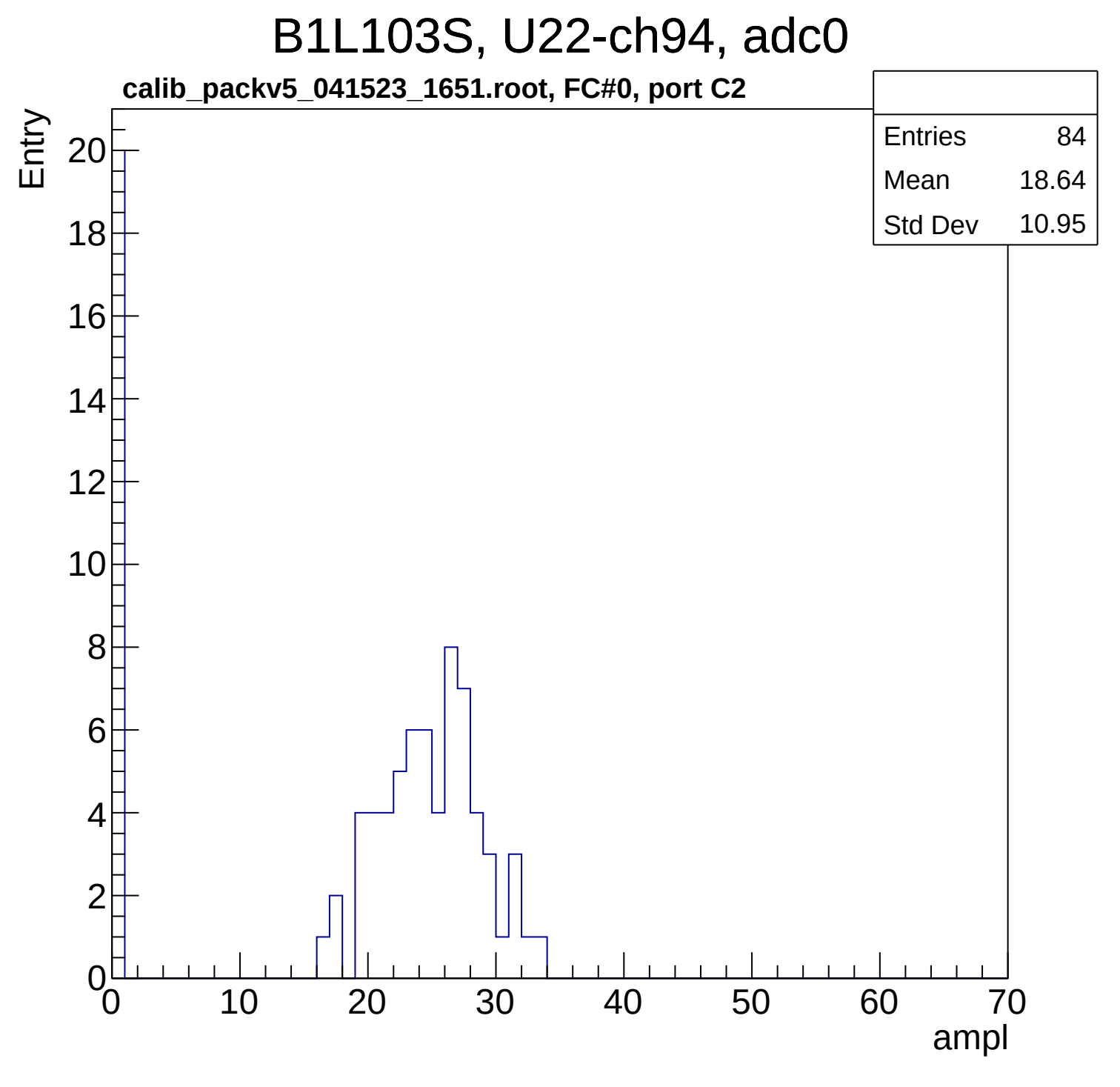
40
50
60
70


B1L103S, U22-ch93, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 61.14
Std Dev 1.457
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U22-ch93, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch94, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 18.64
Std Dev 10.95
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
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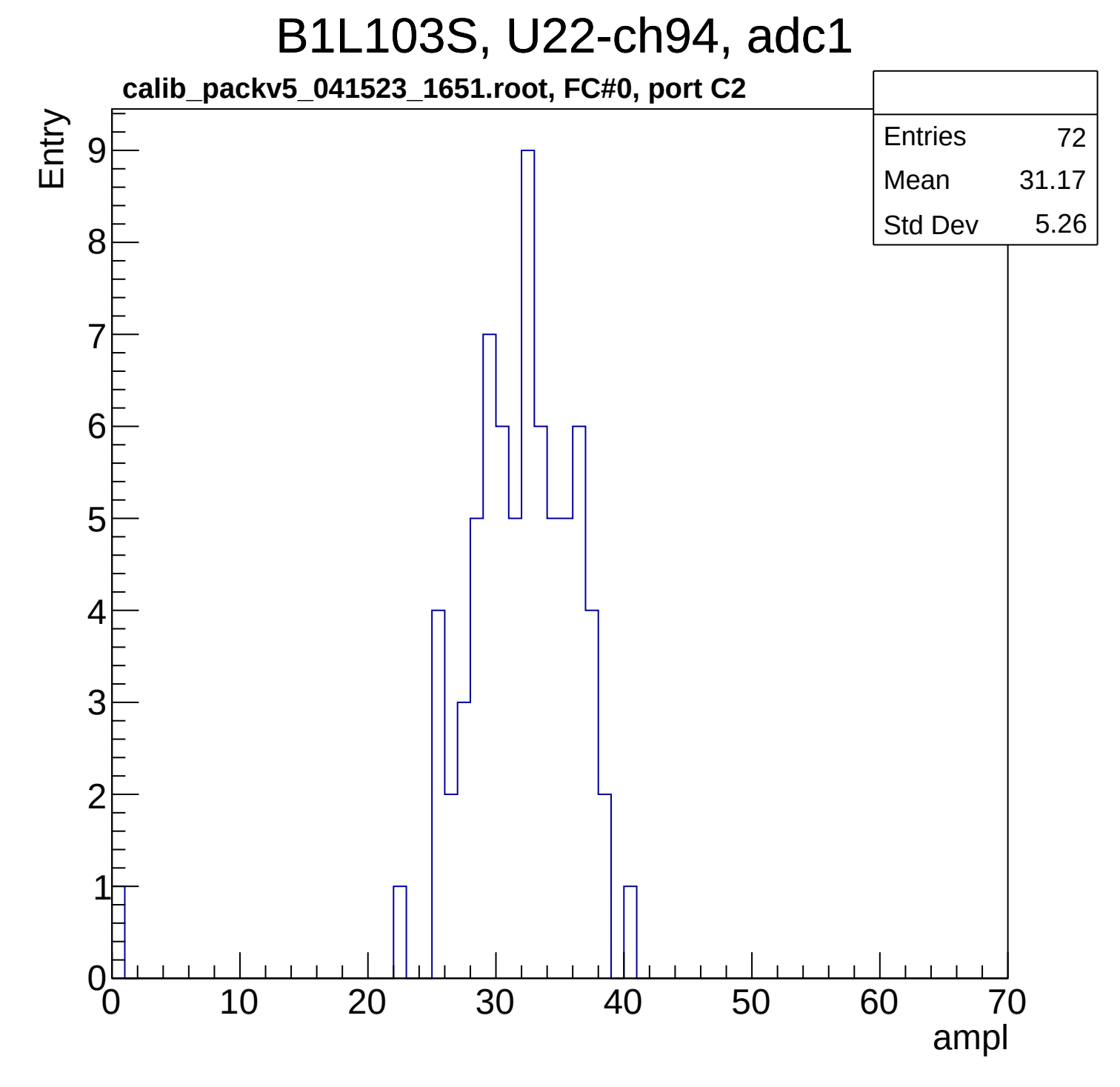
50
60
70


B1L103S, U22-ch94, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 31.17
Std Dev 5.26
Entry
ampl
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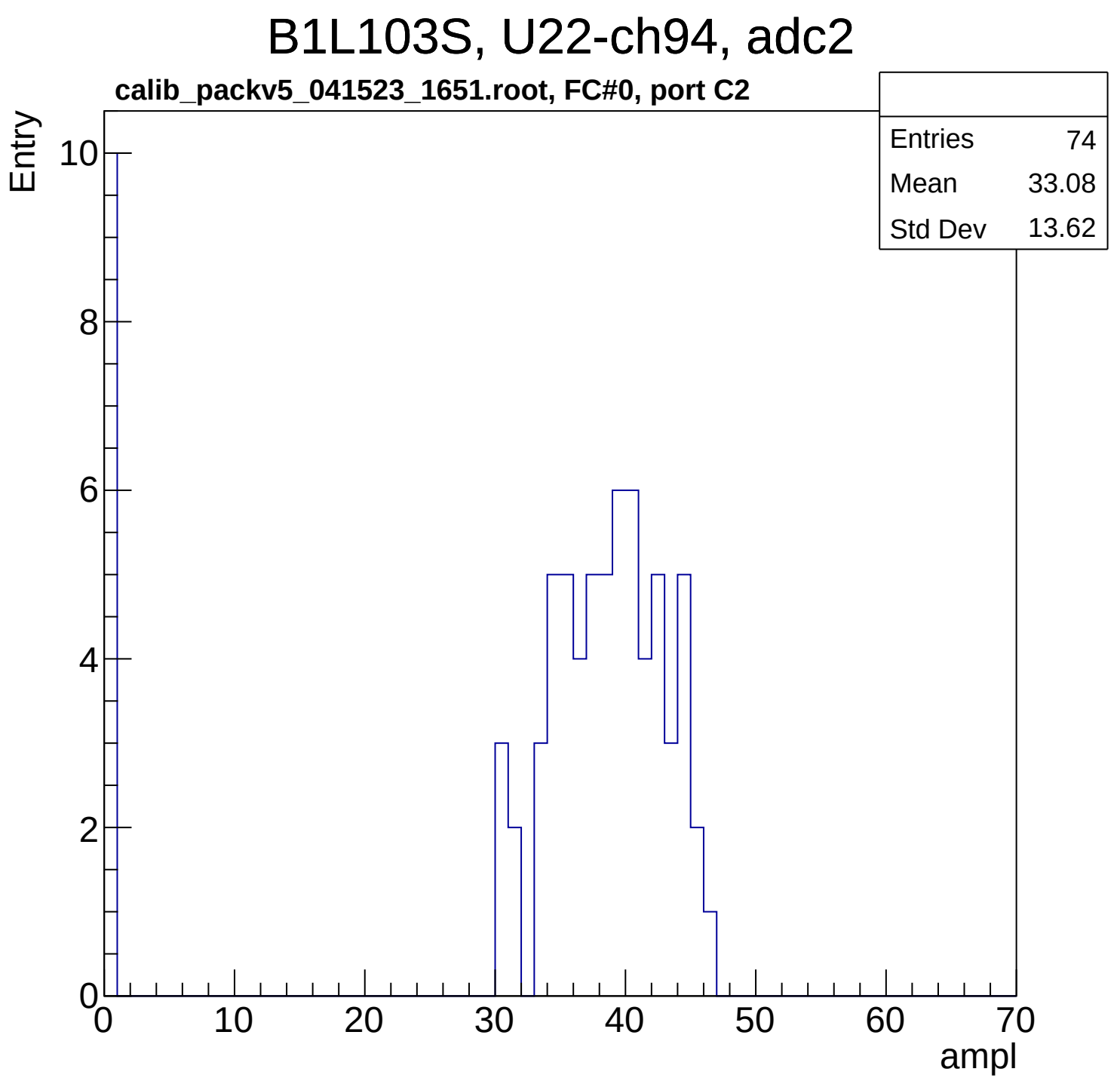
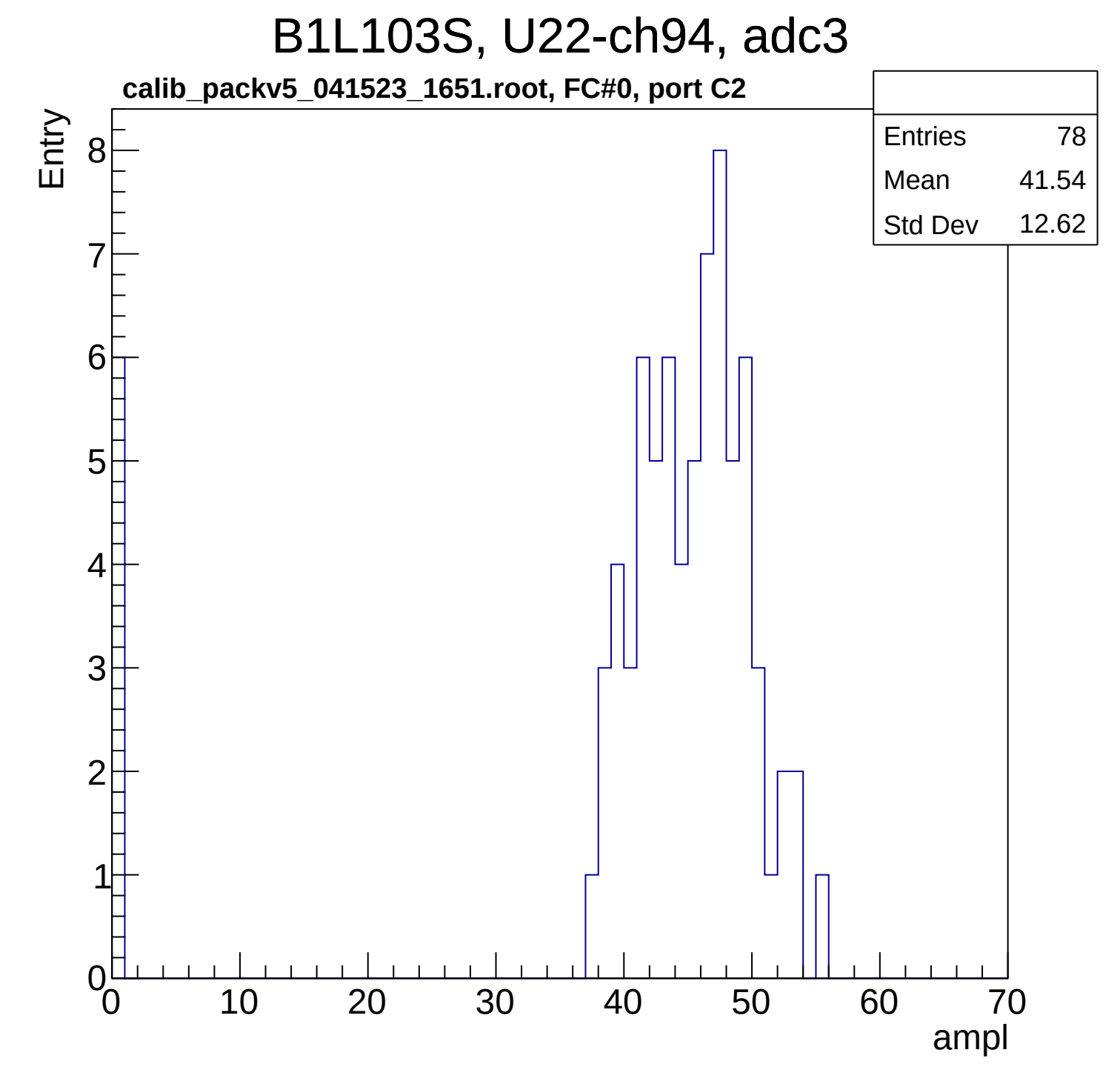
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch94, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 33.08
Std Dev 13.62
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch94, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 41.54
Std Dev 12.62
Entry
ampl
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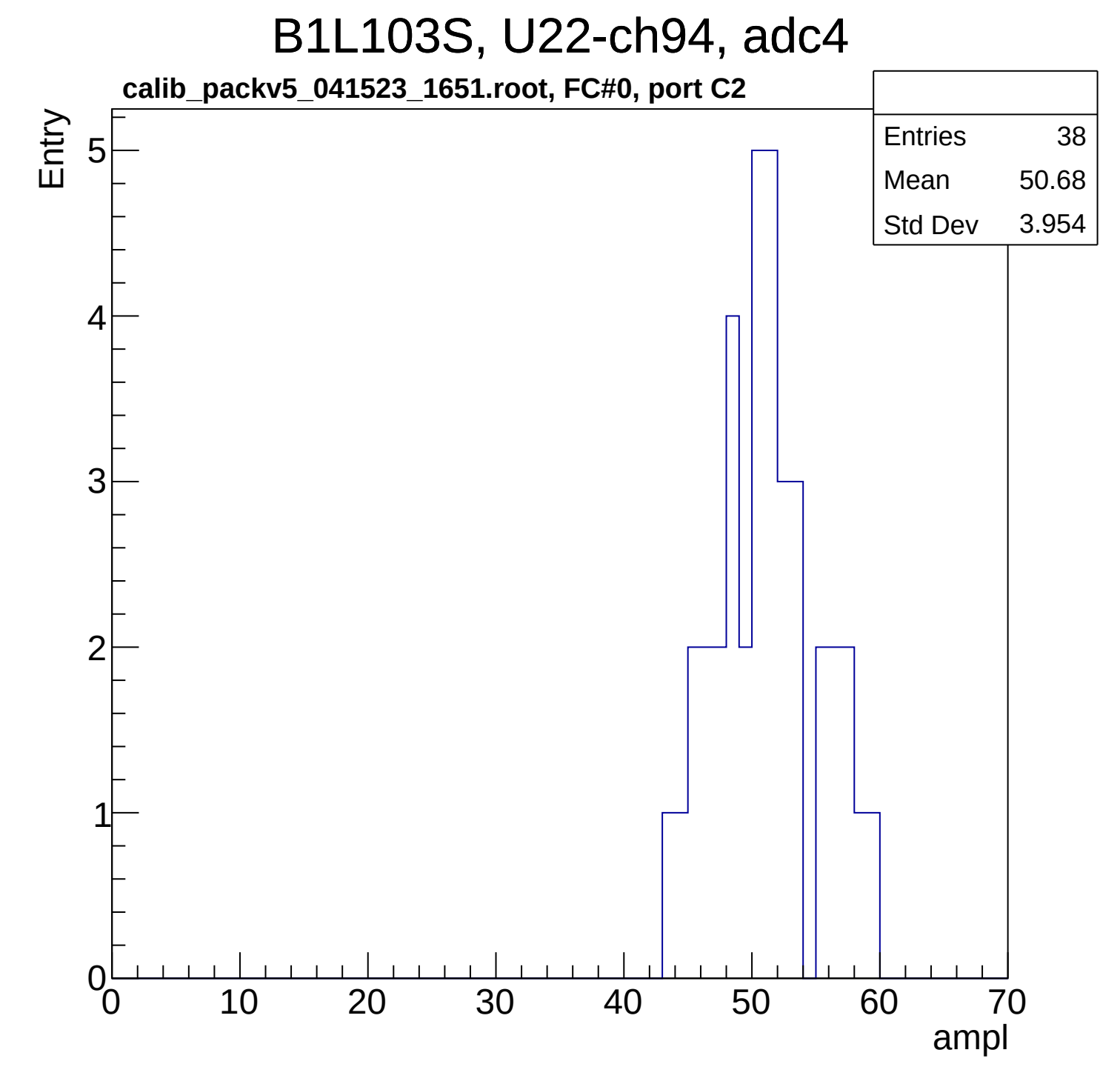
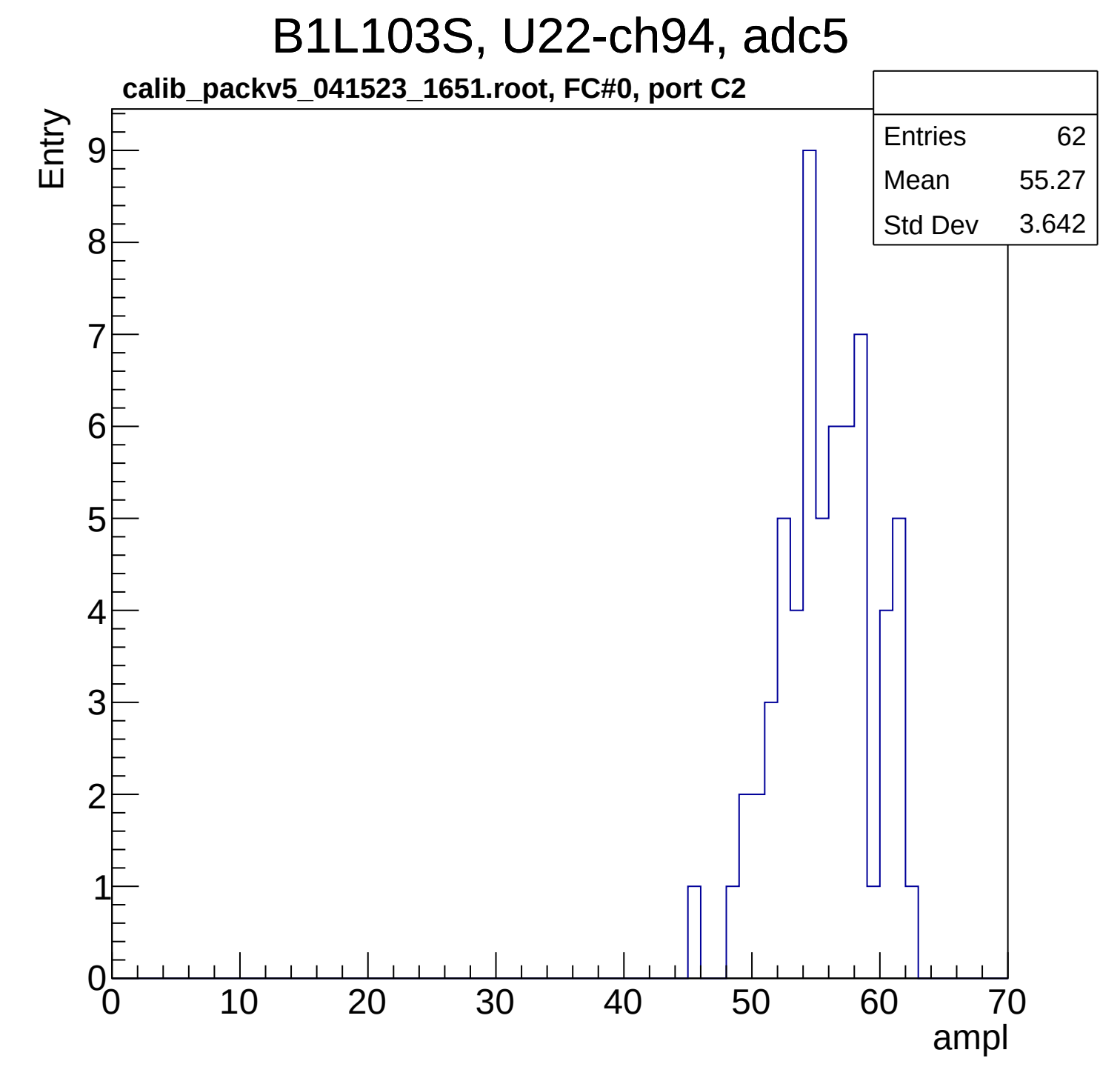
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch94, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 50.68
Std Dev 3.954
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch94, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 55.27
Std Dev 3.642
Entry
ampl
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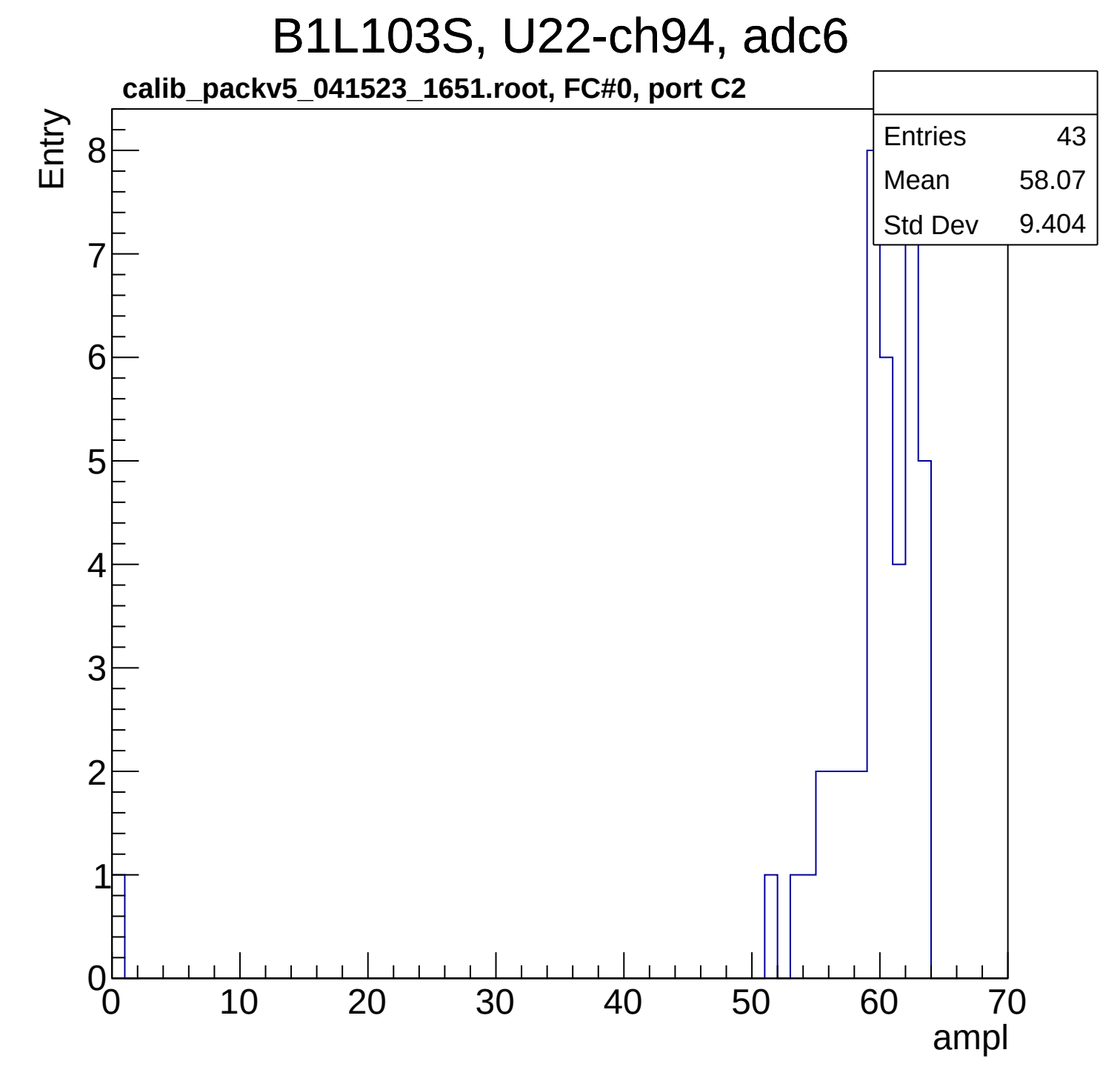
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch94, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 58.07
Std Dev 9.404
Entry
ampl
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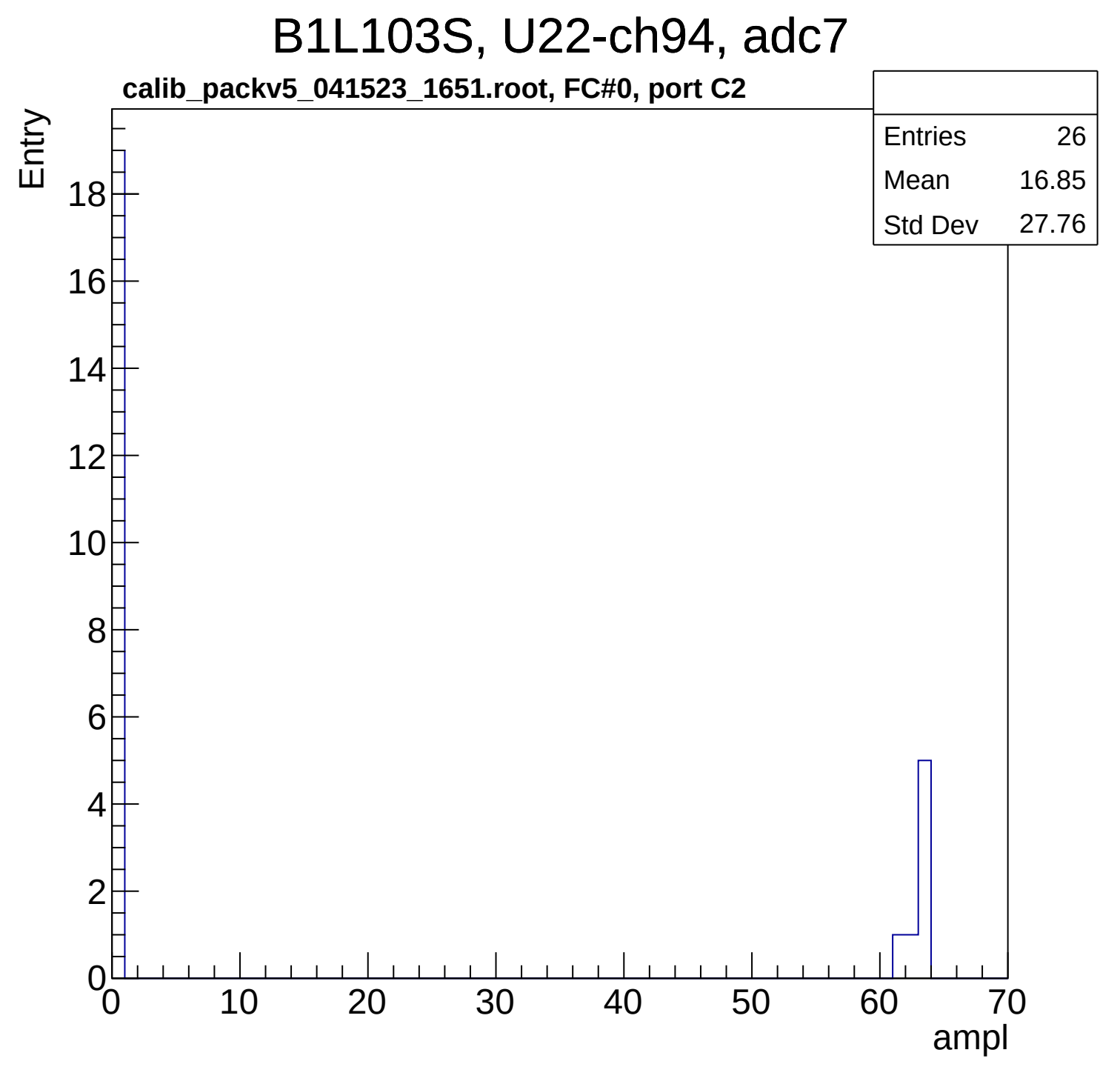
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch94, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 16.85
Std Dev 27.76
Entry
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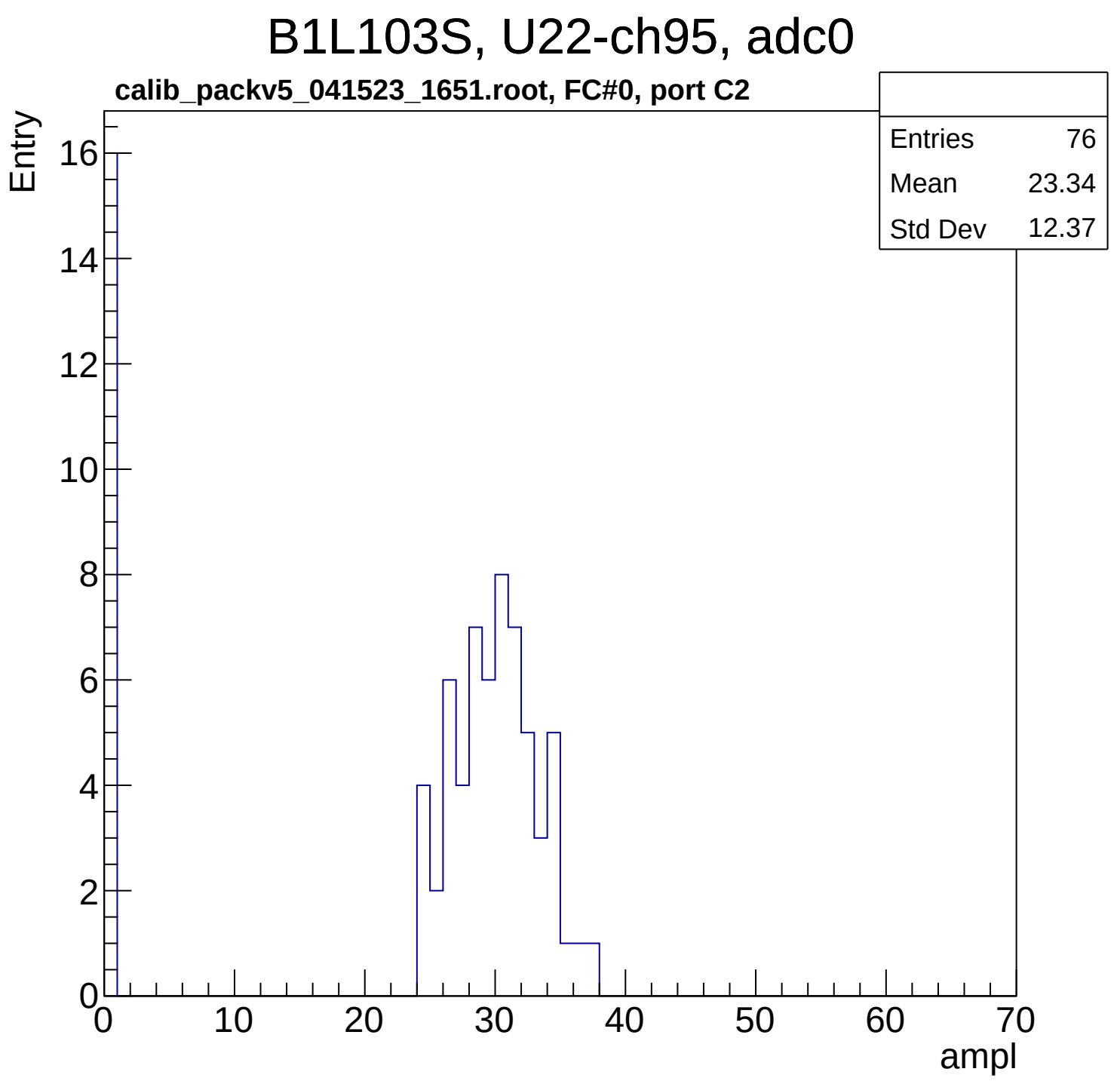
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch95, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 23.34
Std Dev 12.37
Entry
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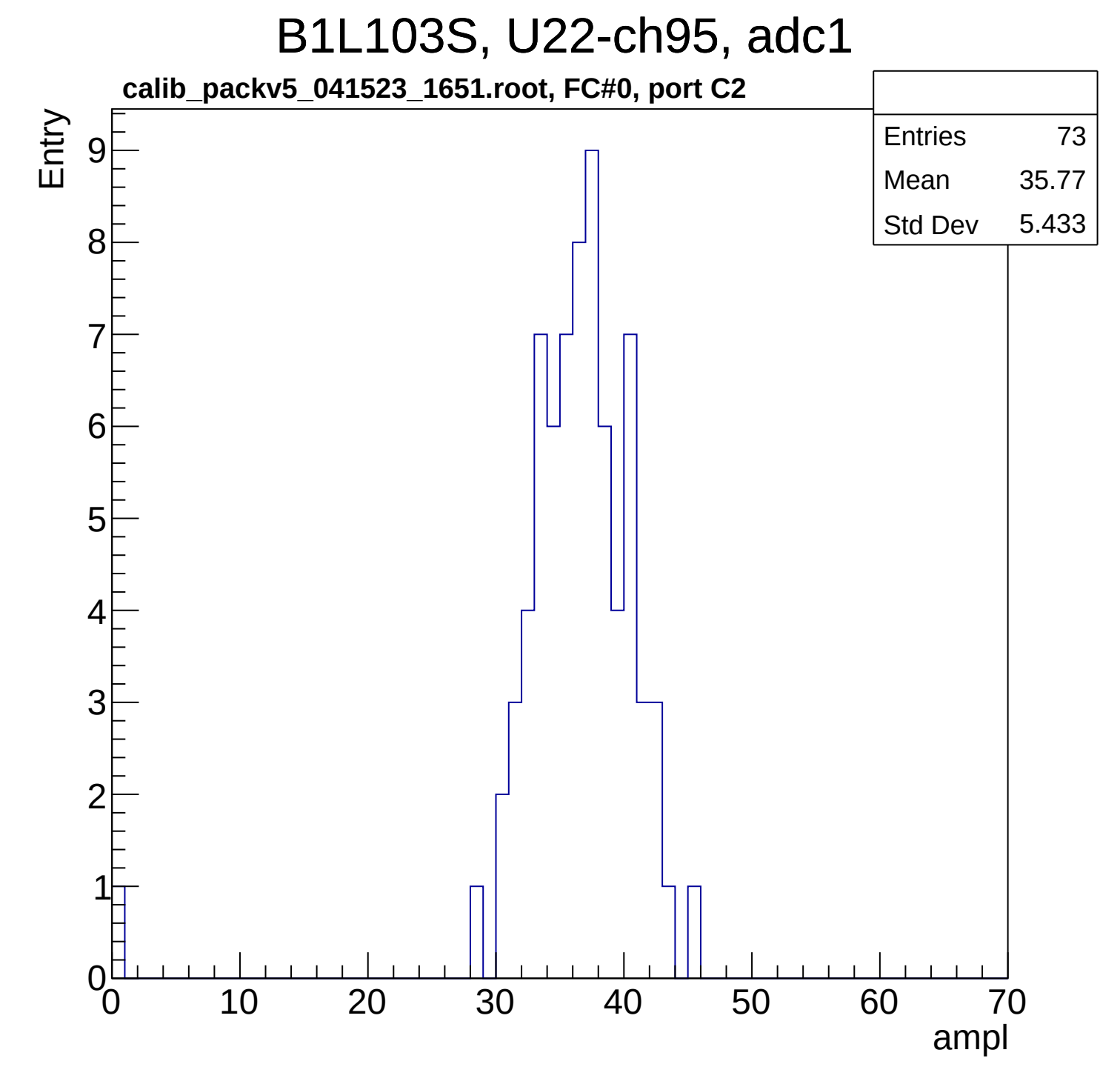
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch95, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 35.77
Std Dev 5.433
Entry
ampl
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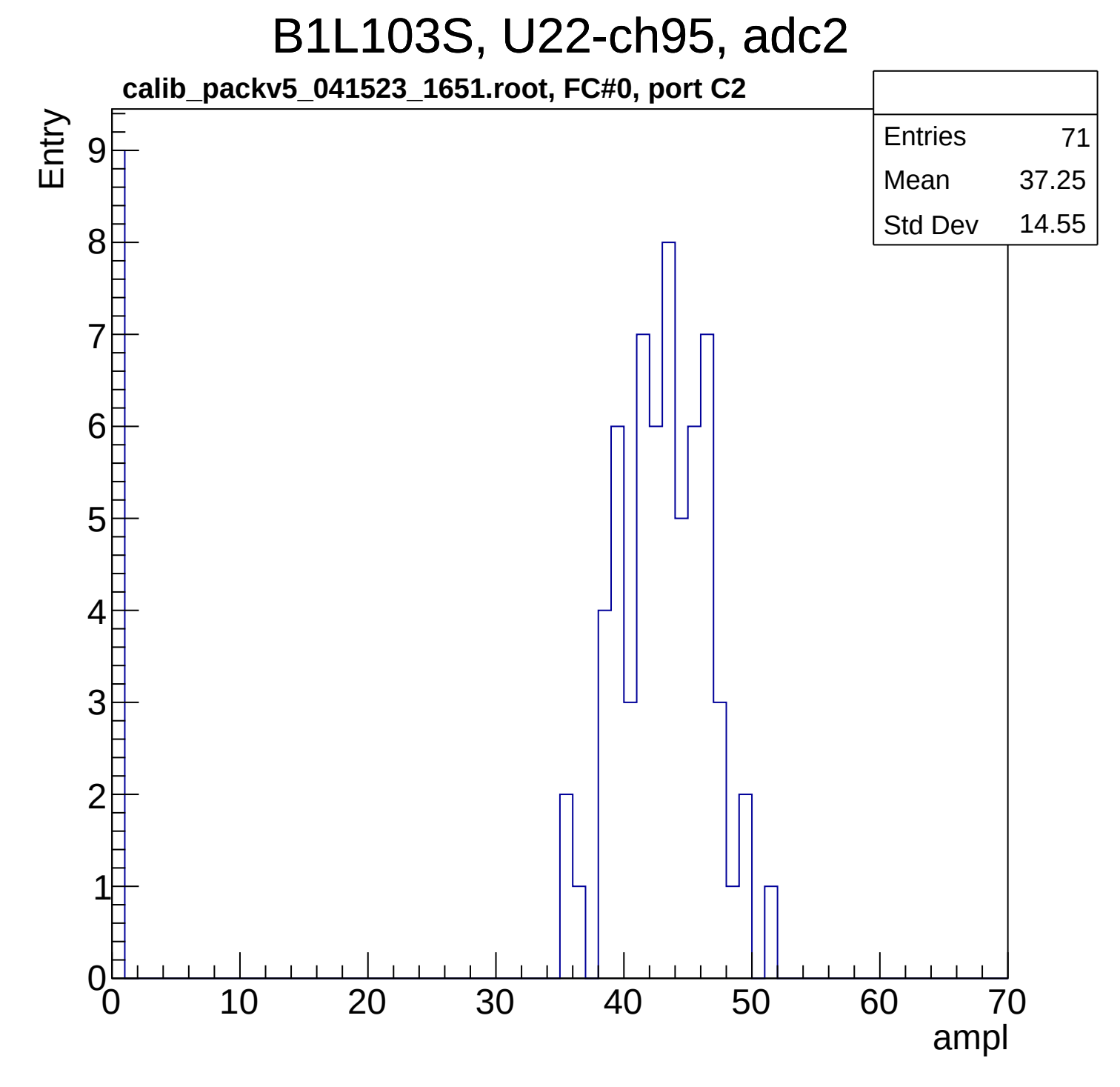
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch95, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 37.25
Std Dev 14.55
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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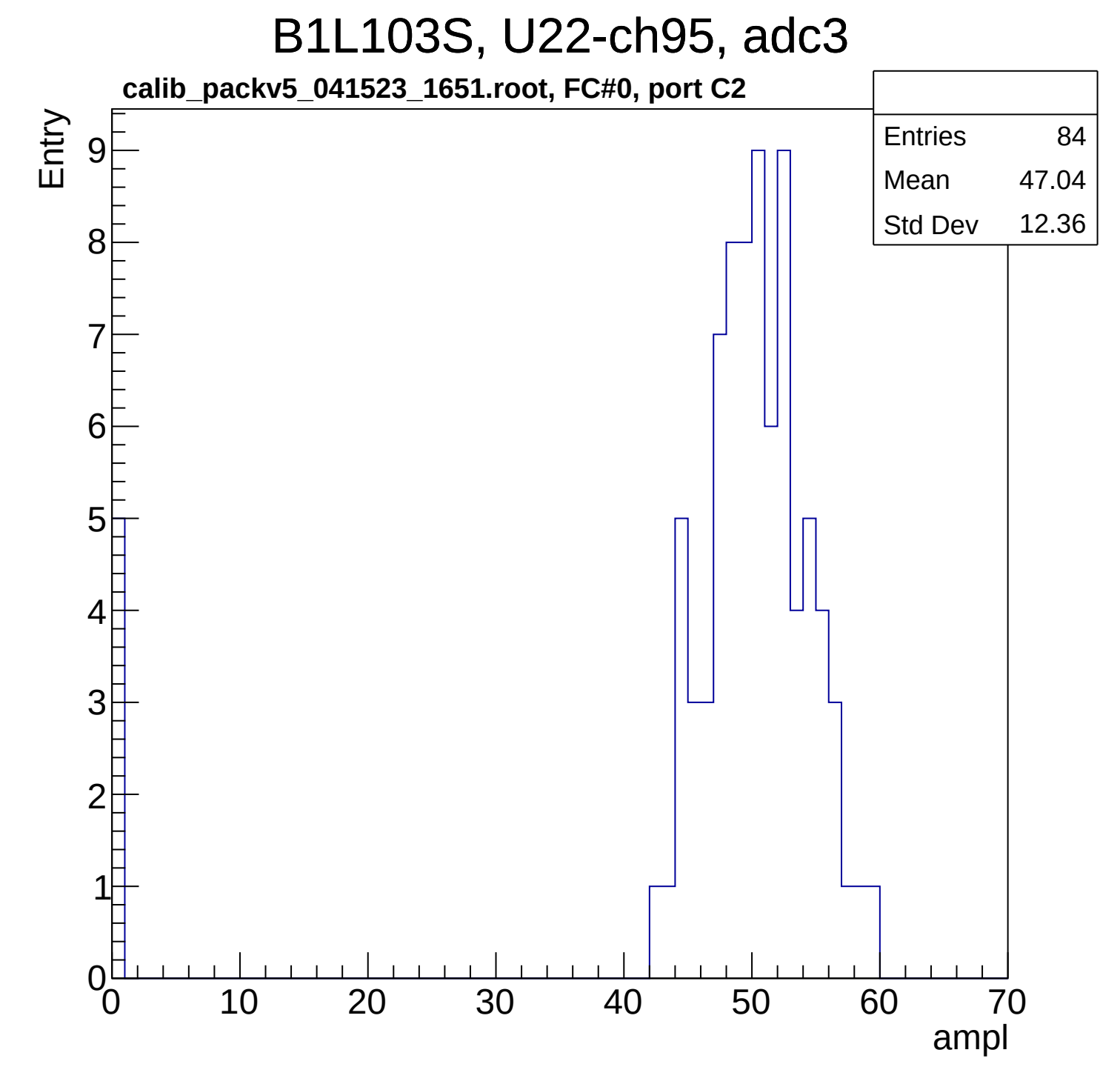
B1L103S, U22-ch95, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 47.04
Std Dev 12.36
Entry
ampl
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2
3
4
5
6
7
8
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0
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40
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60
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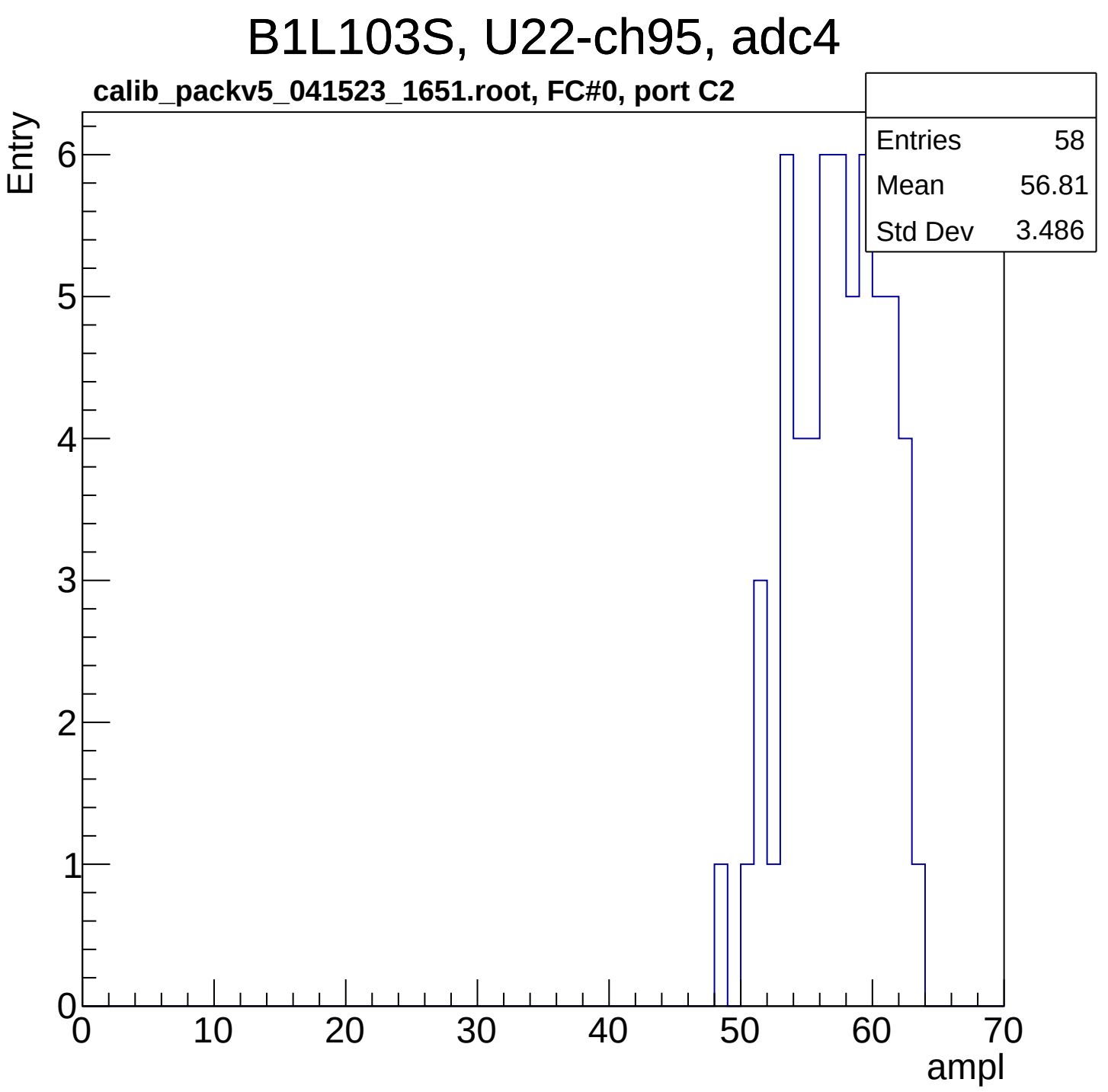
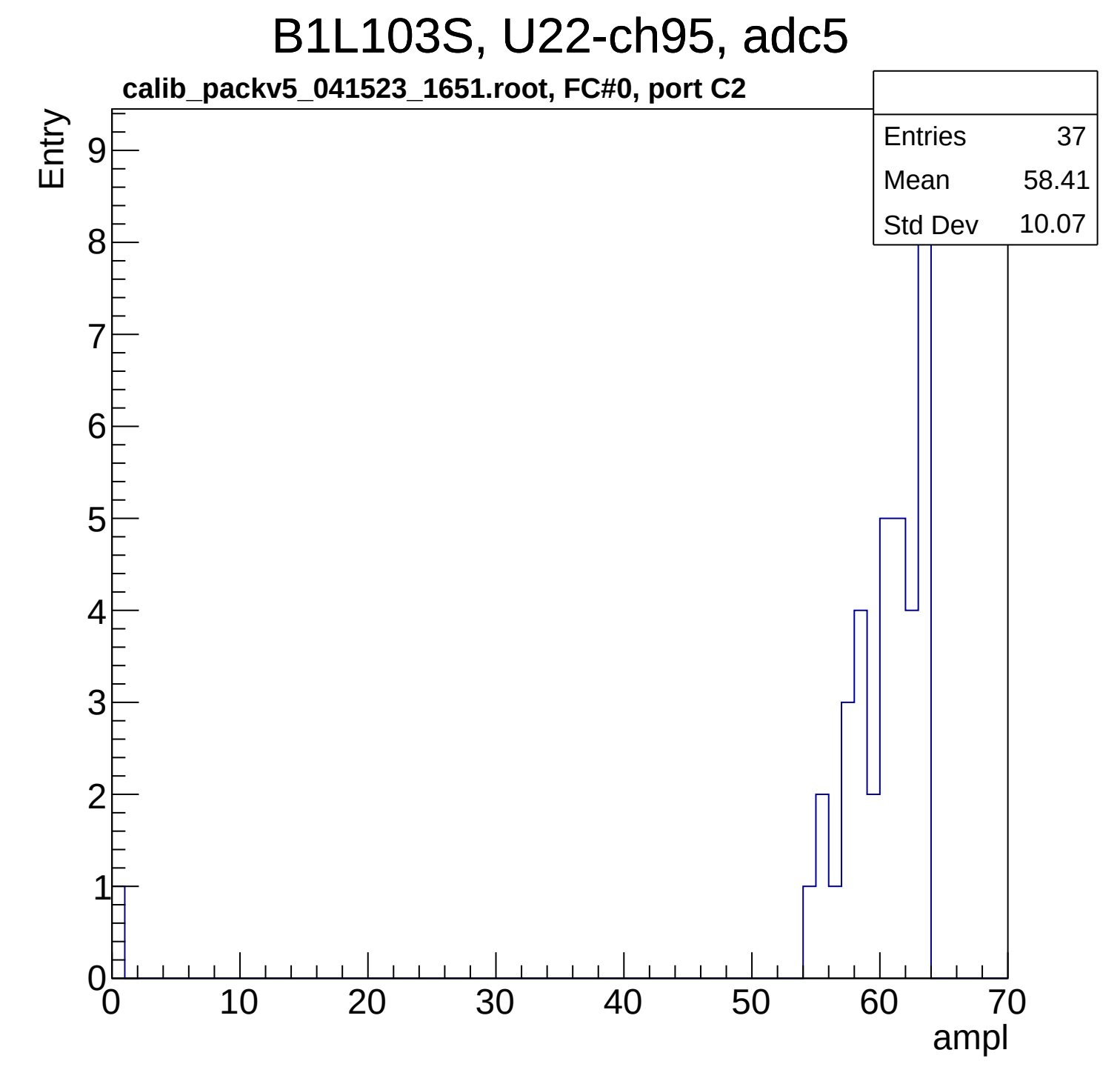

B1L103S, U22-ch95, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 56.81
Std Dev 3.486
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U22-ch95, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 58.41
Std Dev 10.07
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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20
30
40
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60
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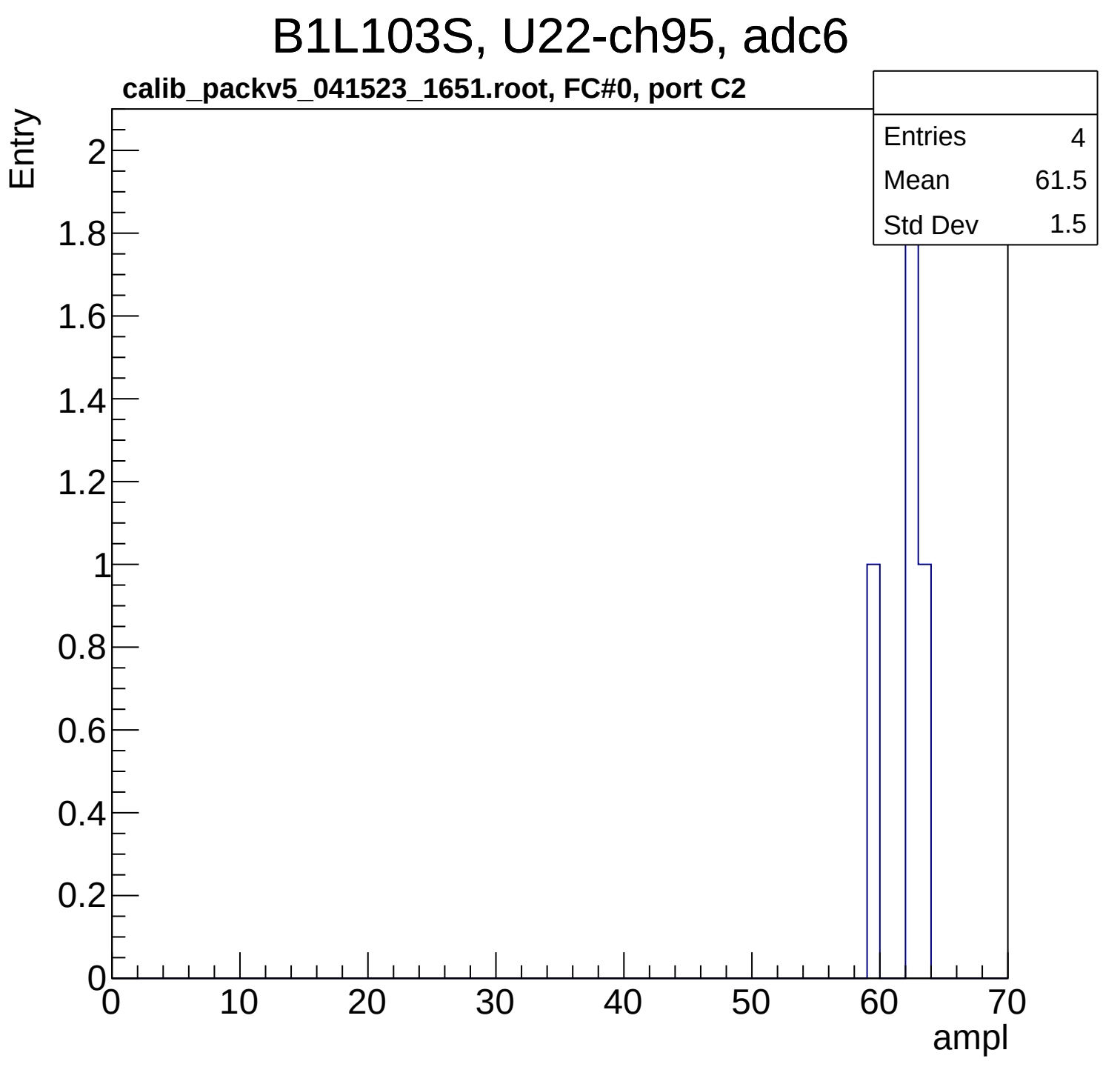
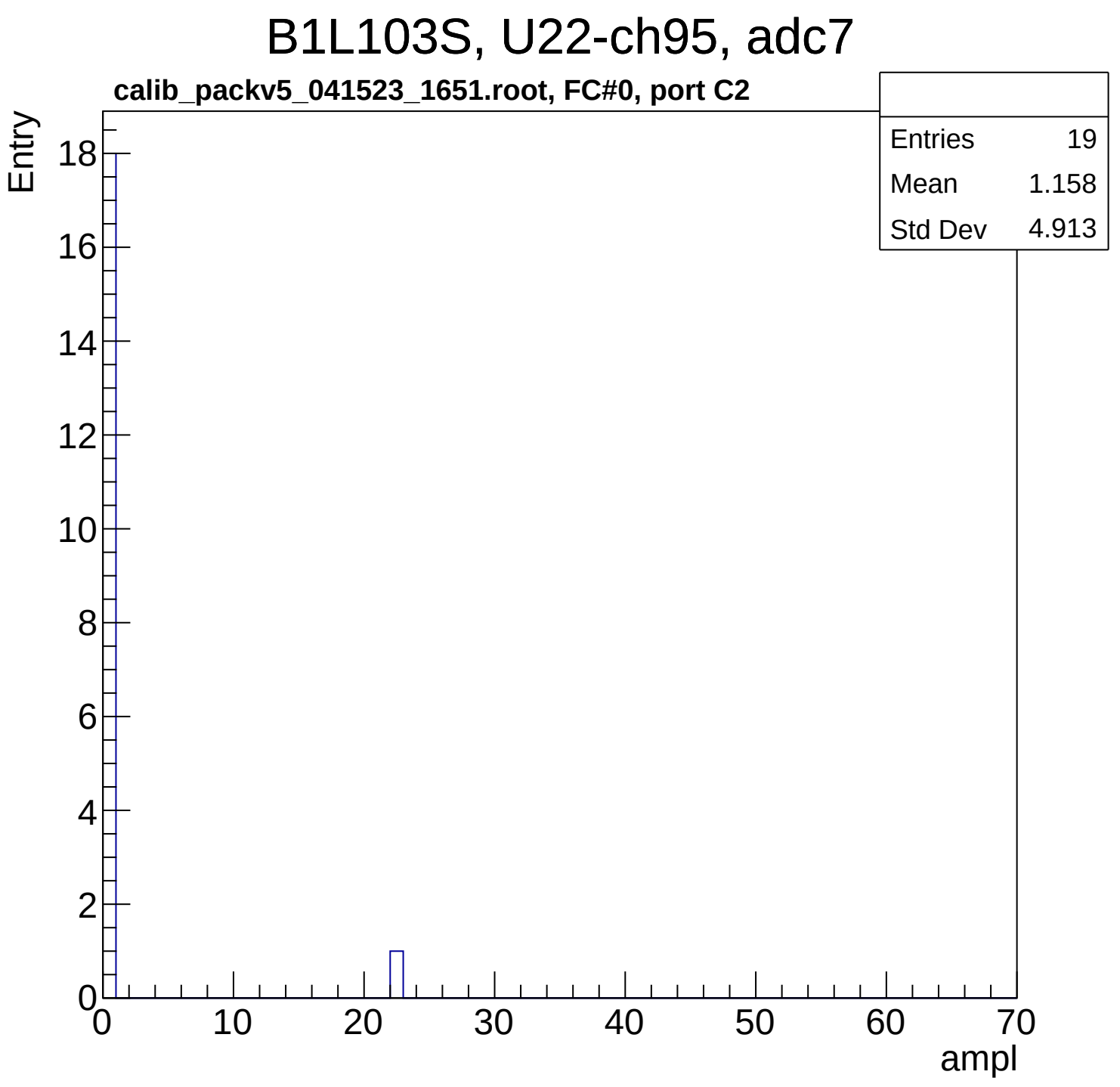
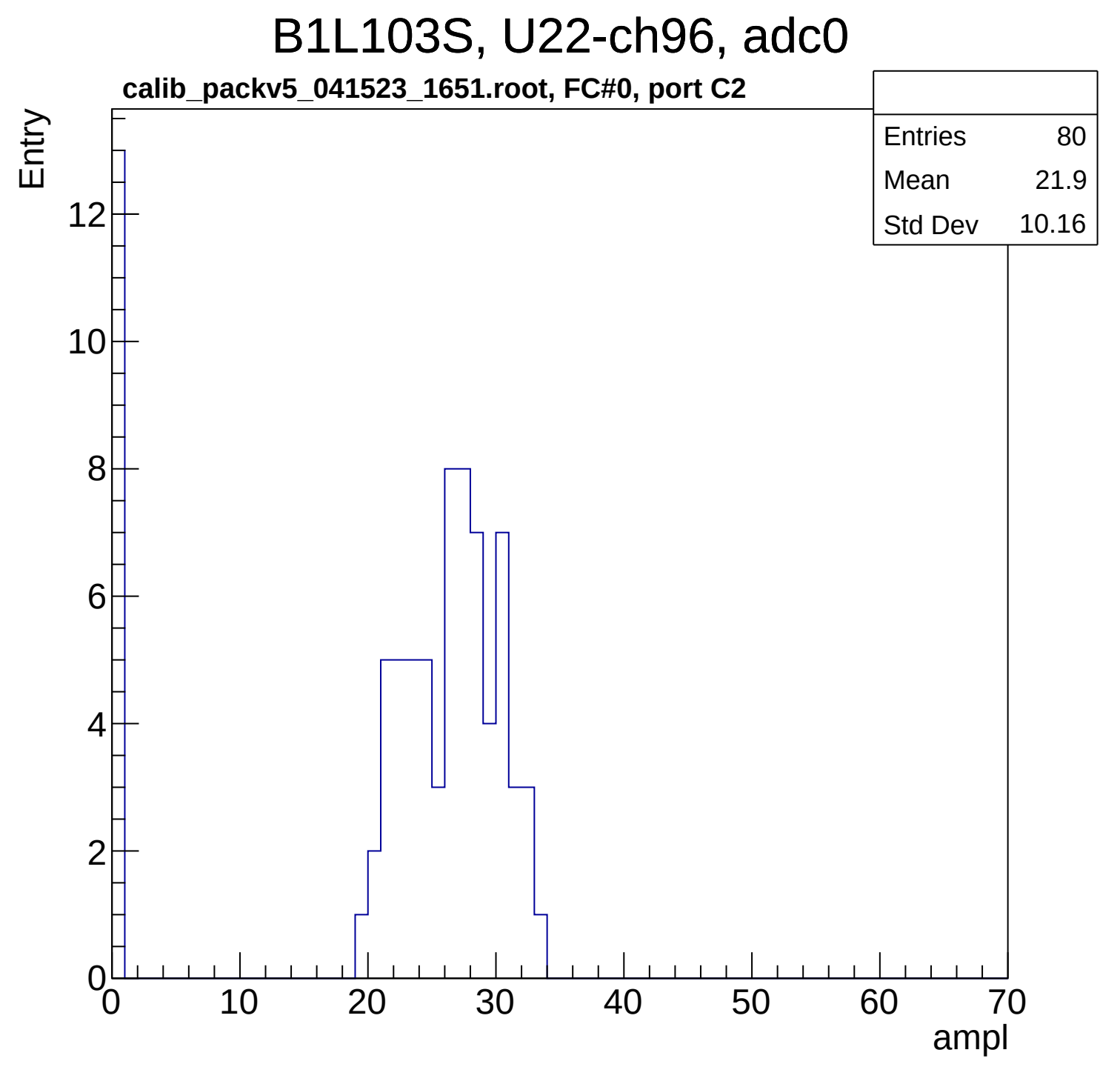
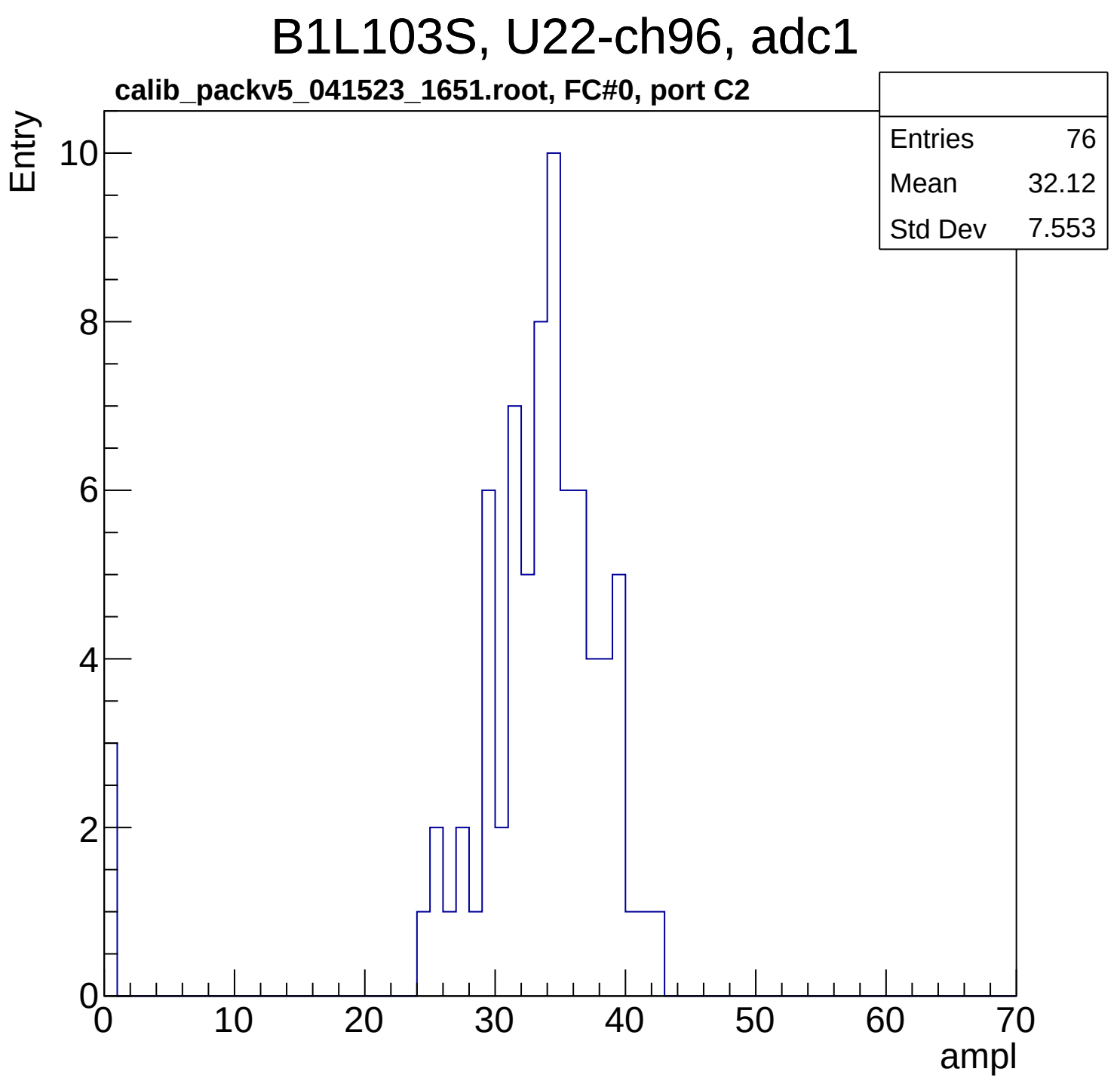
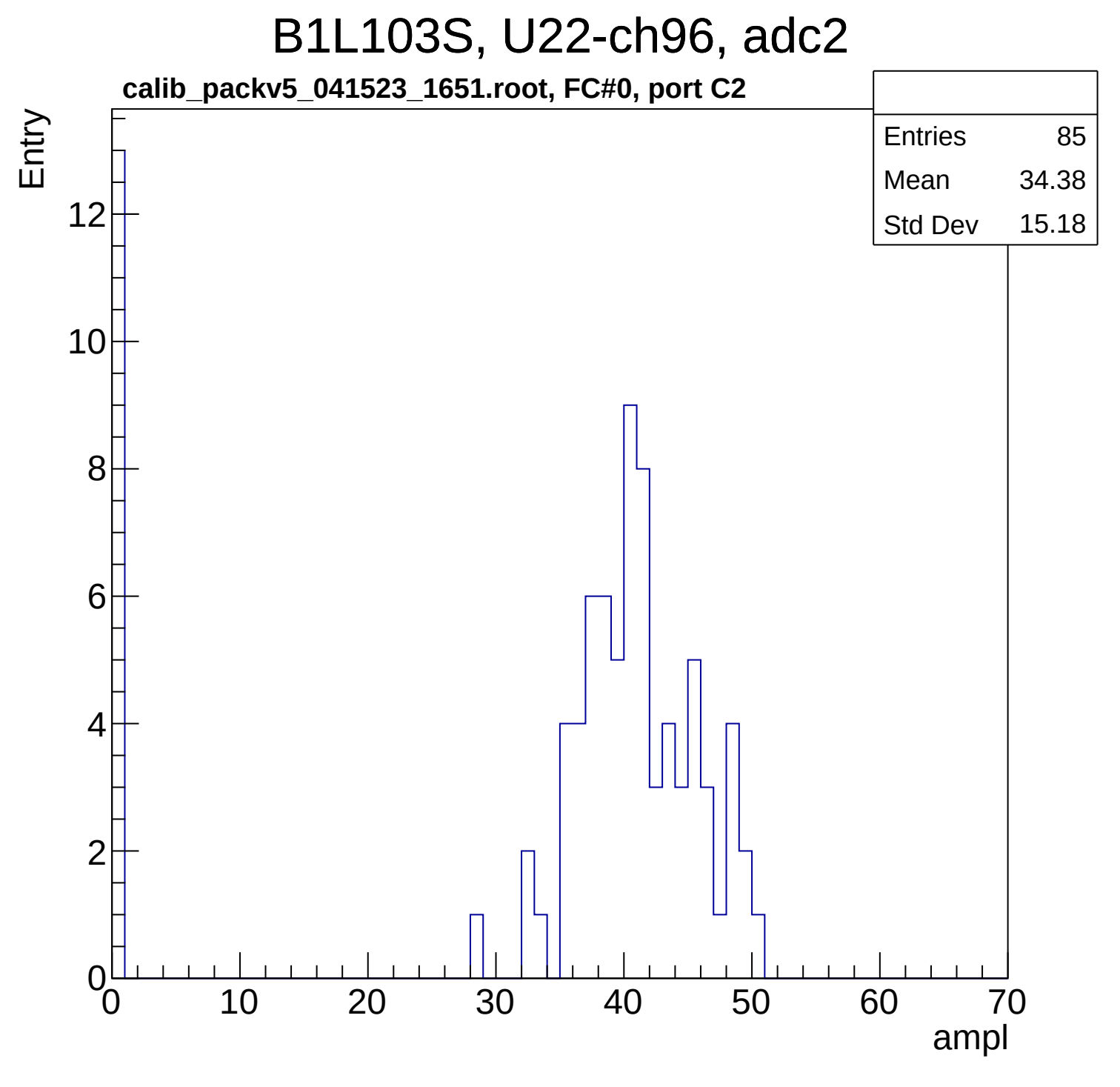
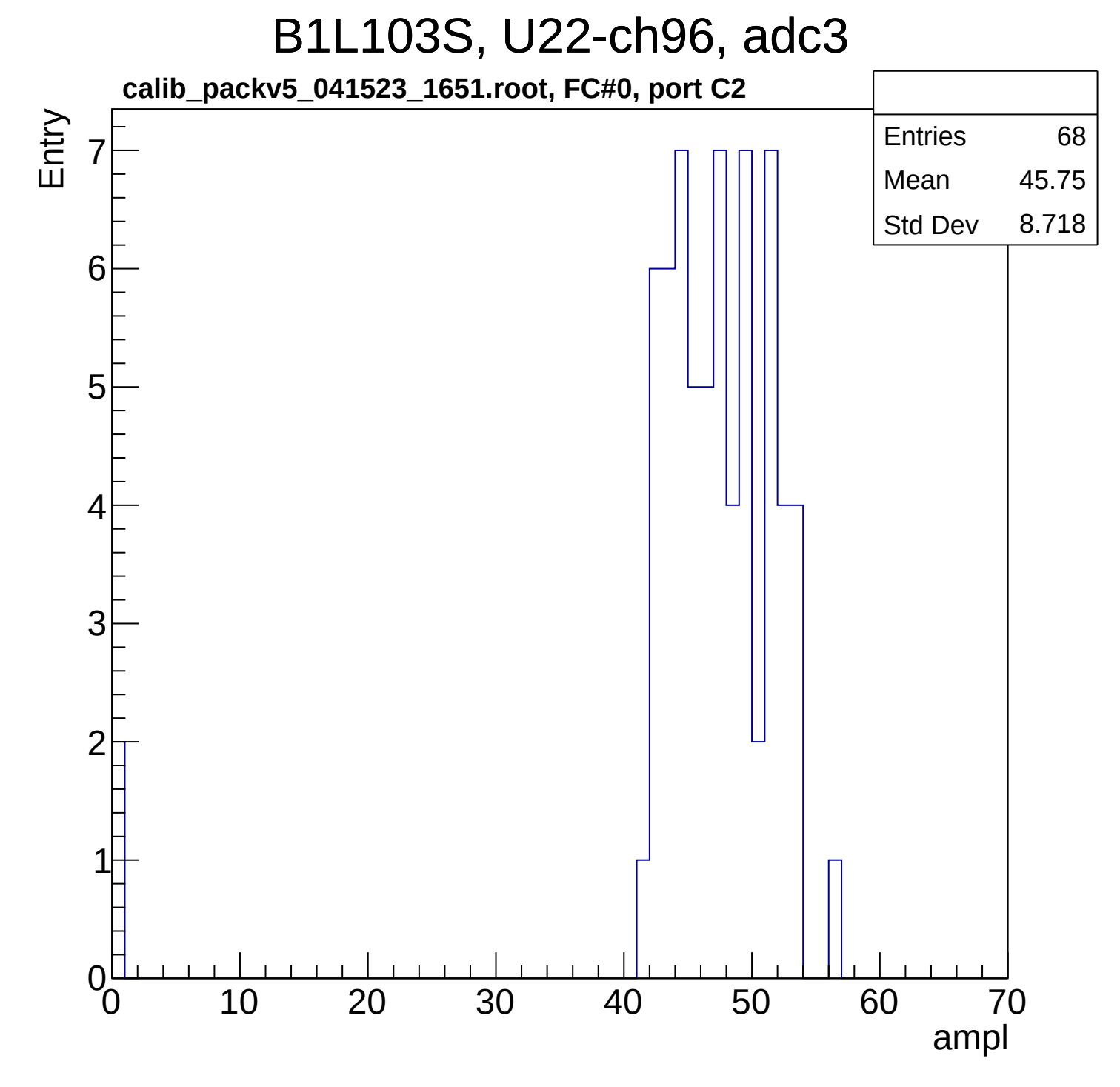

B1L103S, U22-ch95, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 61.5
Std Dev 1.5
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

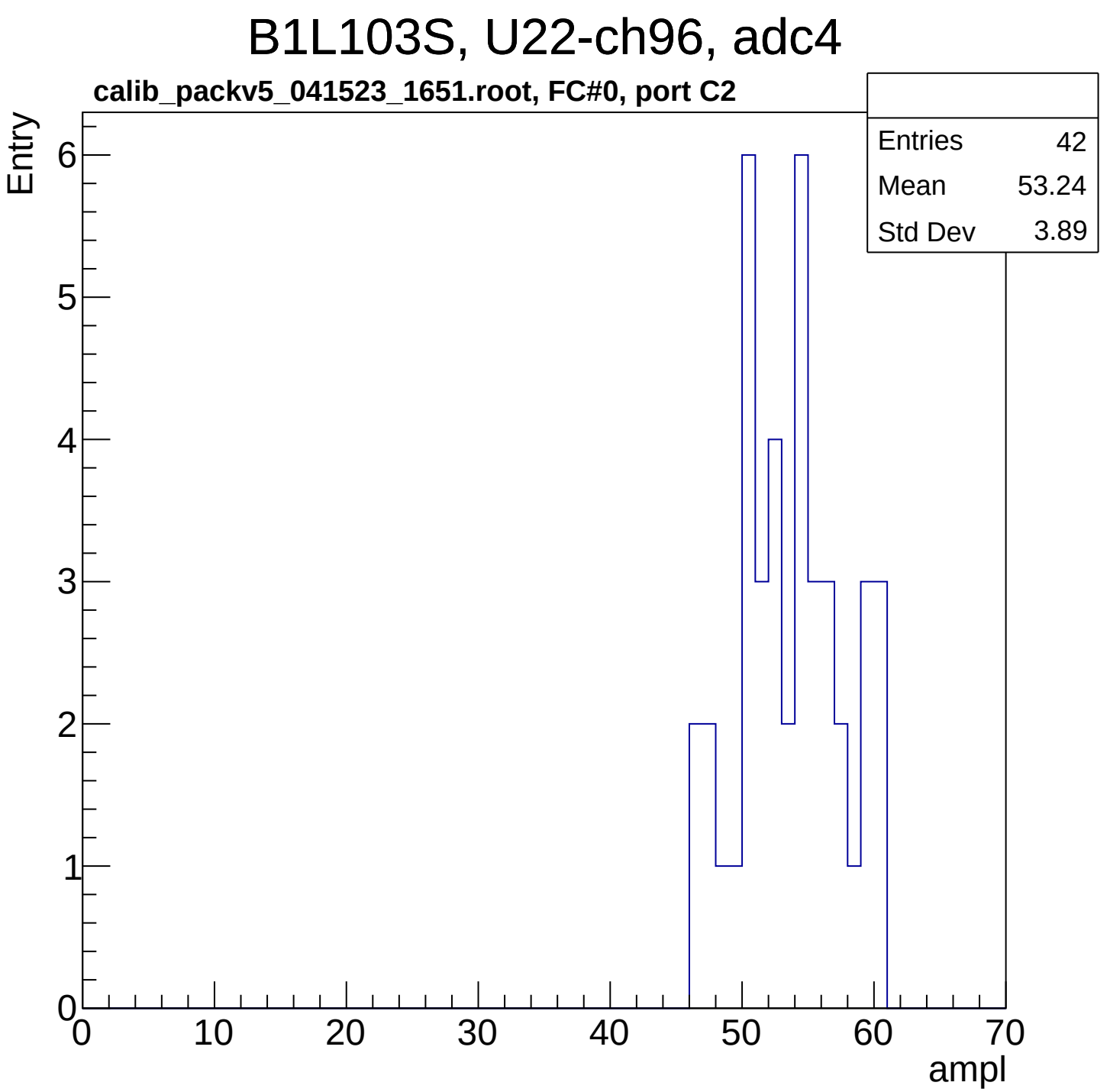

B1L103S, U22-ch95, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.158
Std Dev 4.913
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

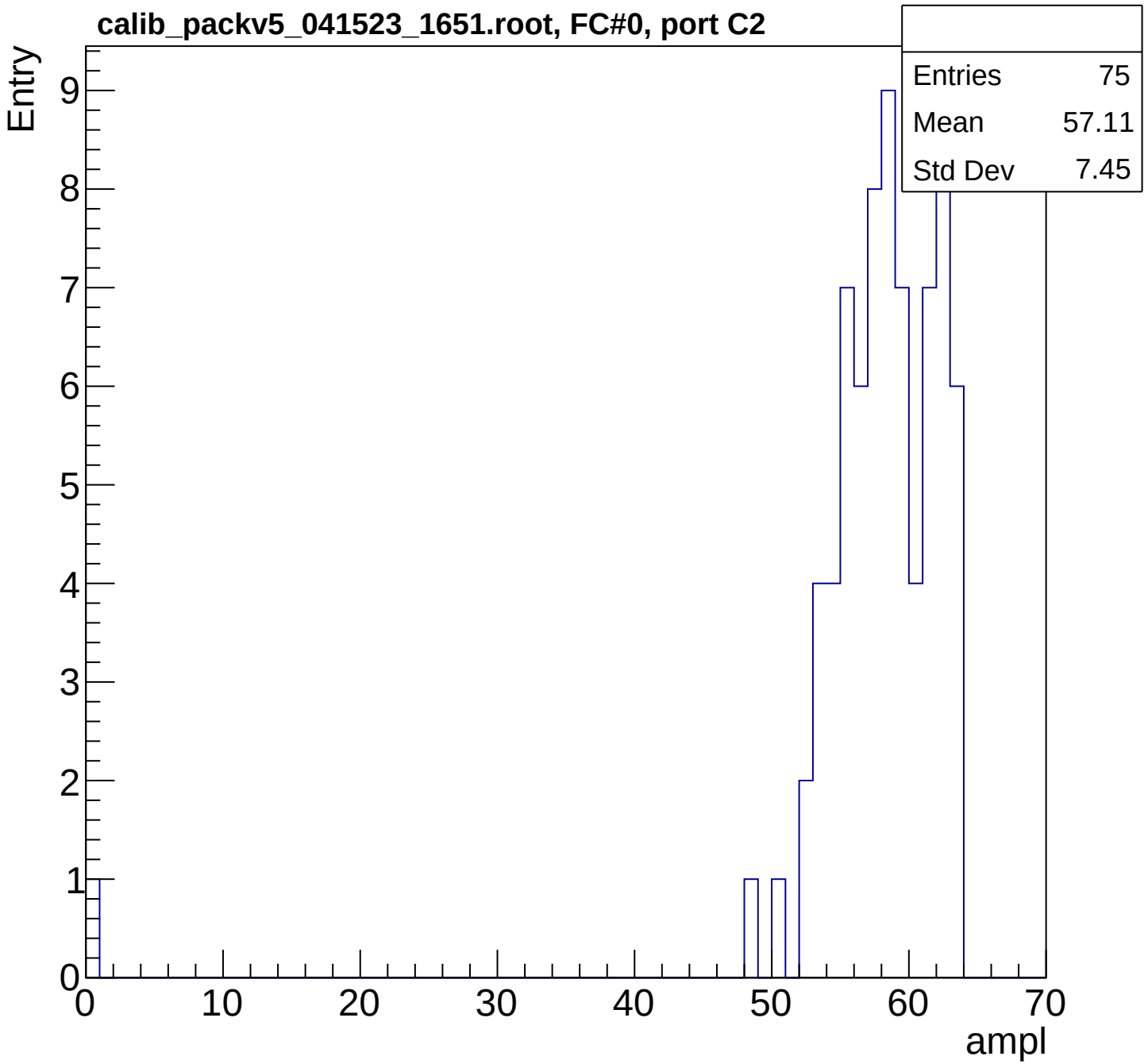

B1L103S, U22-ch96, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 21.9
Std Dev 10.16
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

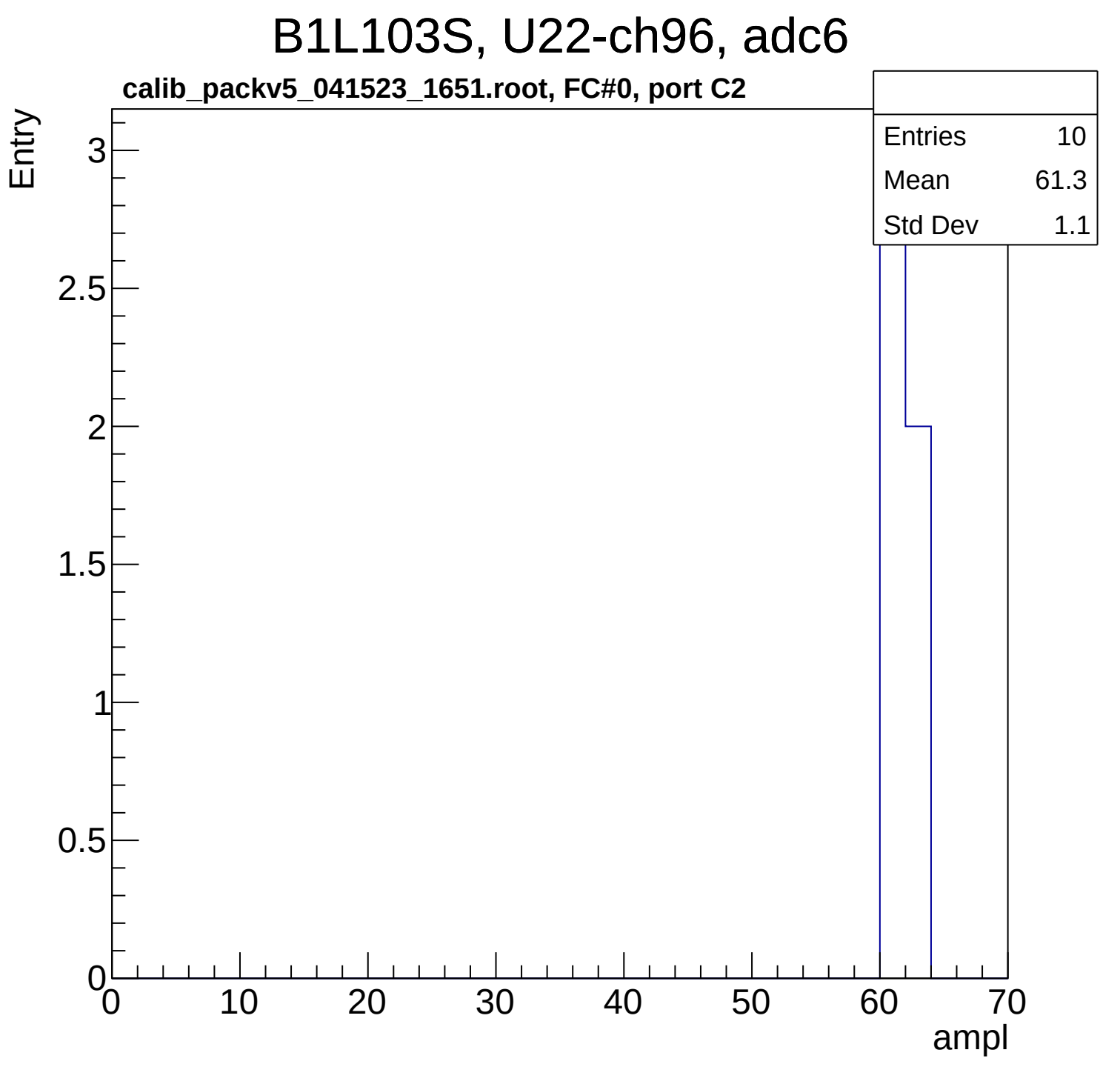

B1L103S, U22-ch96, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 32.12
Std Dev 7.553
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

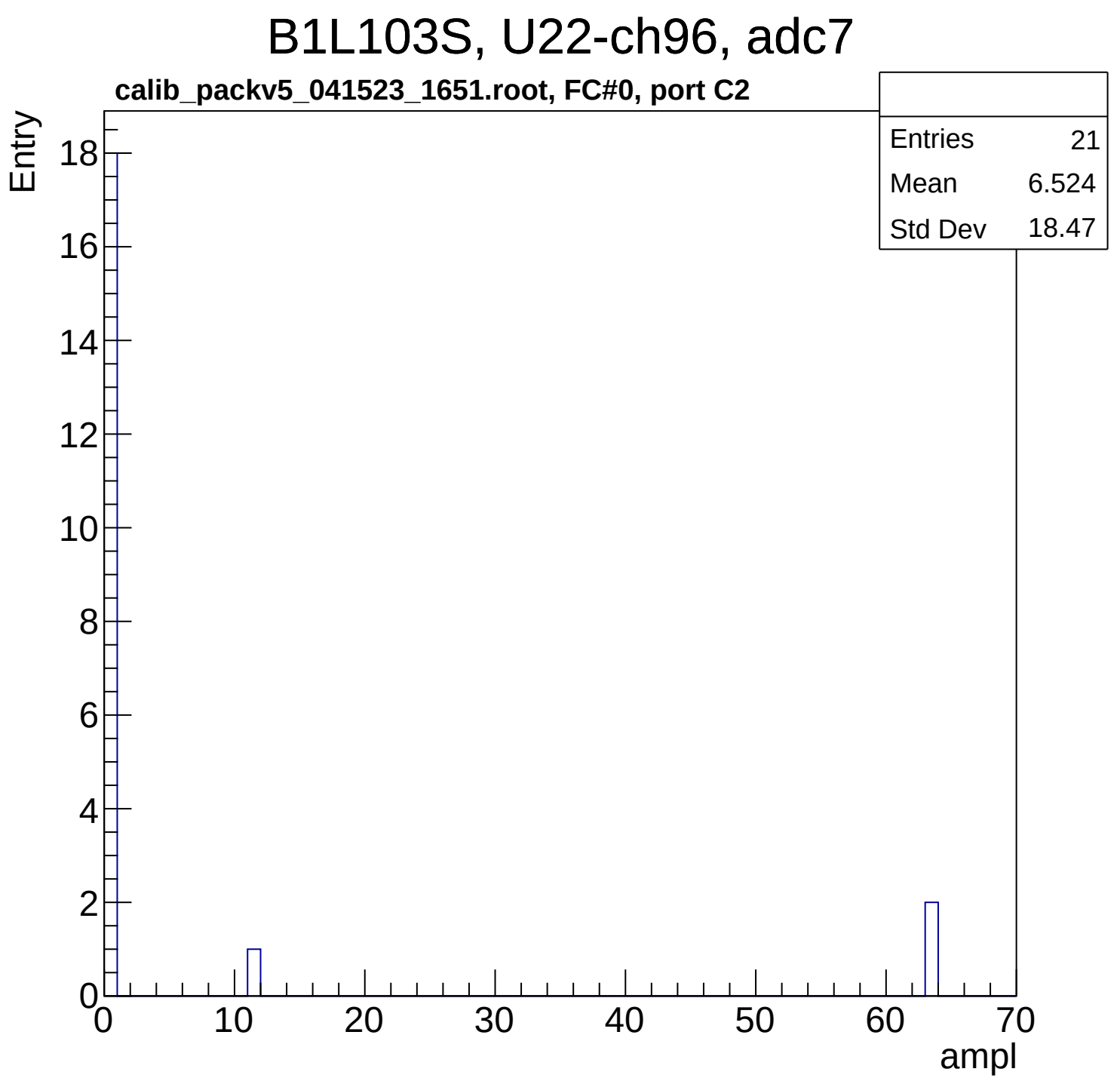

B1L103S, U22-ch96, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 34.38
Std Dev 15.18
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

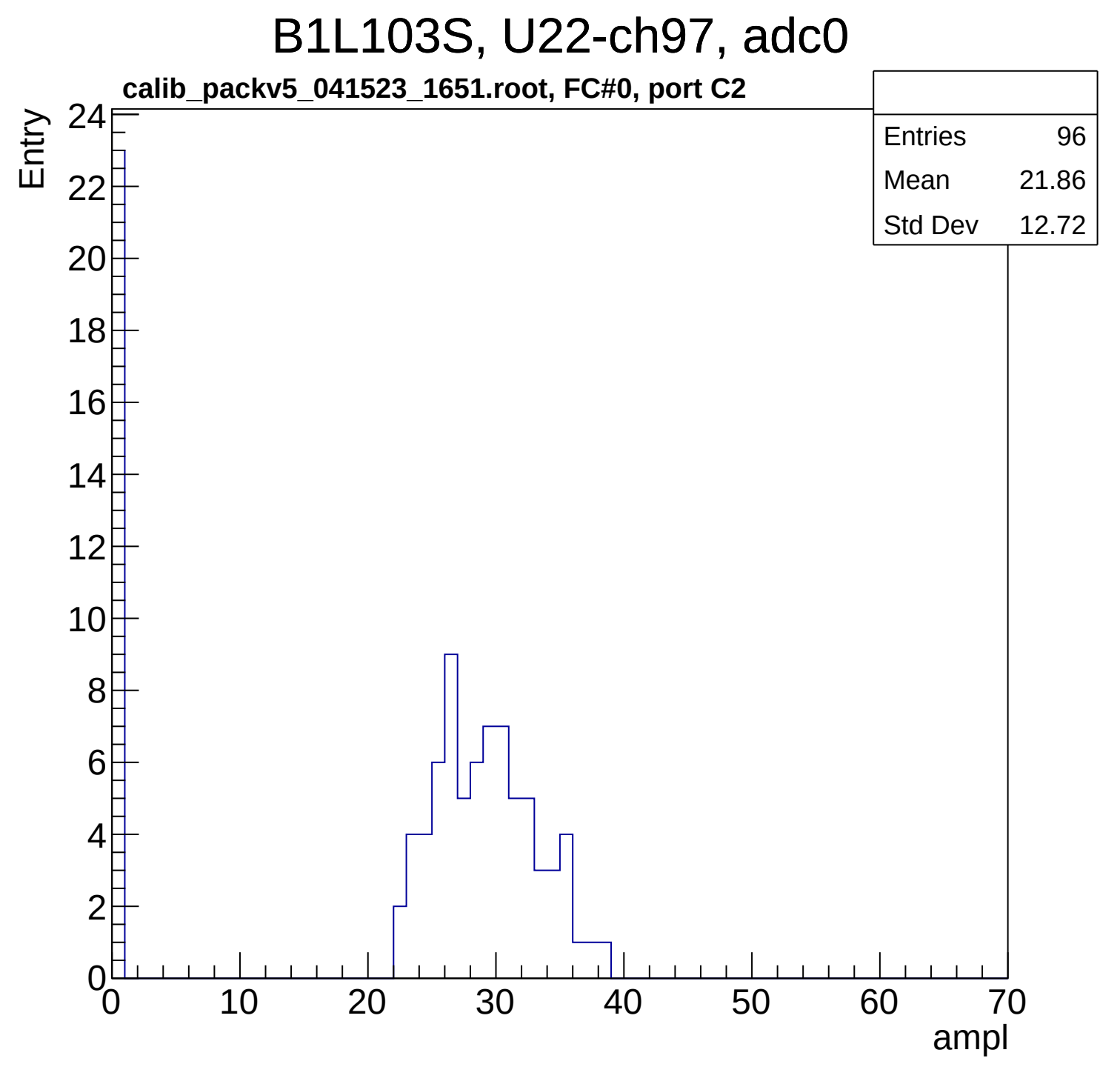

B1L103S, U22-ch96, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 45.75
Std Dev 8.718
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

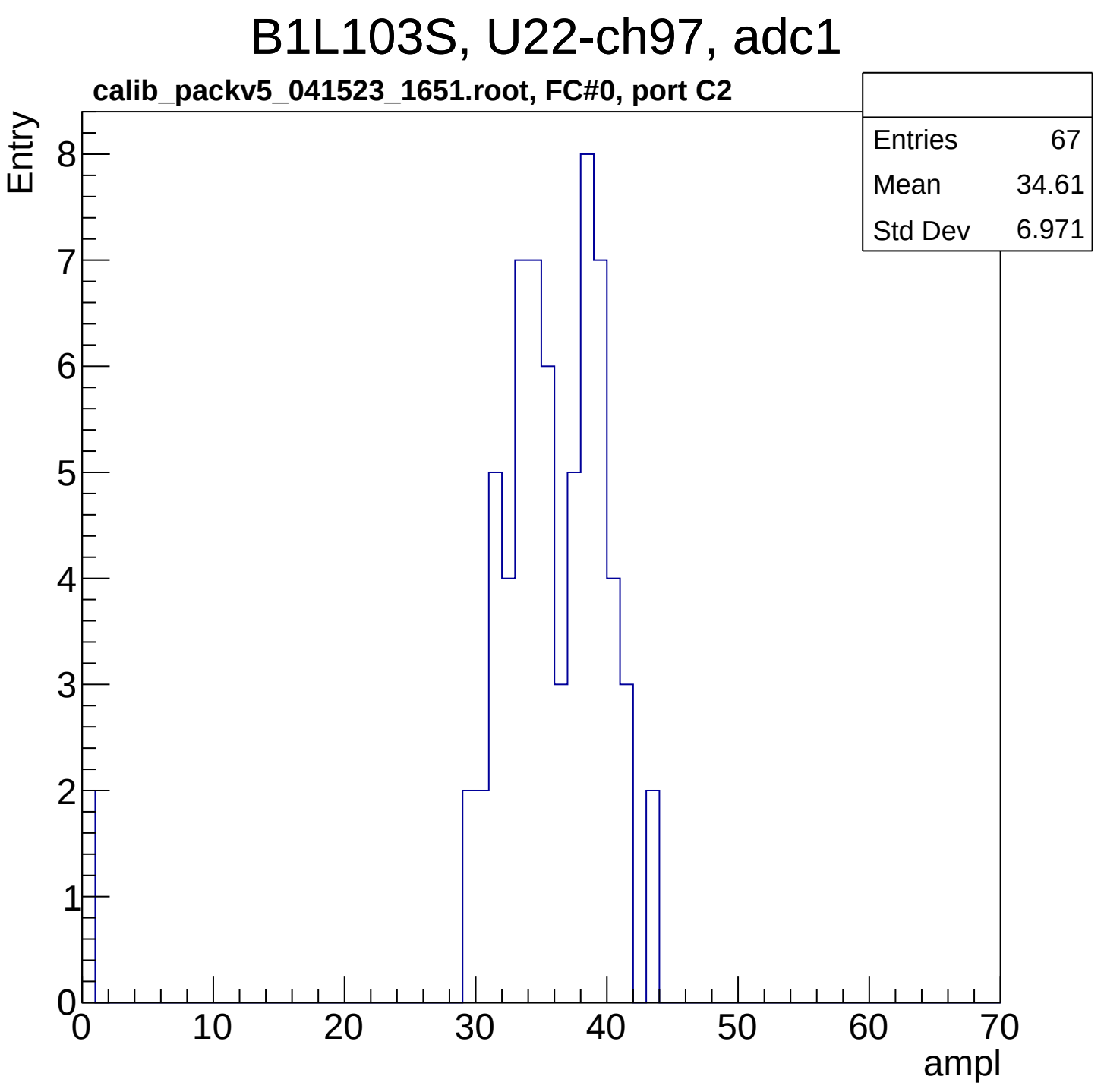

B1L103S, U22-ch96, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 53.24
Std Dev 3.89
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

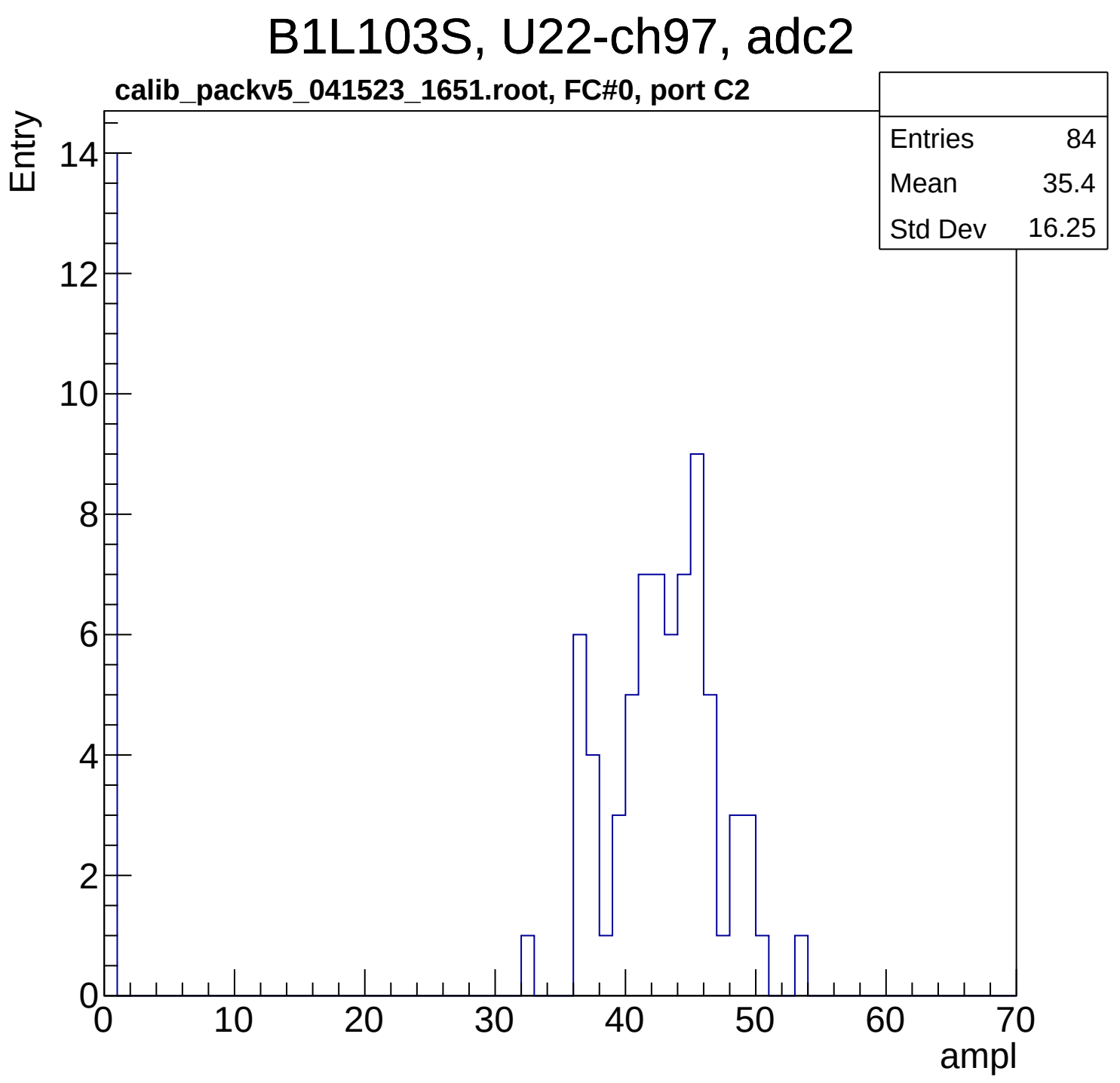

B1L103S, U22-ch96, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 57.11
Std Dev 7.45
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

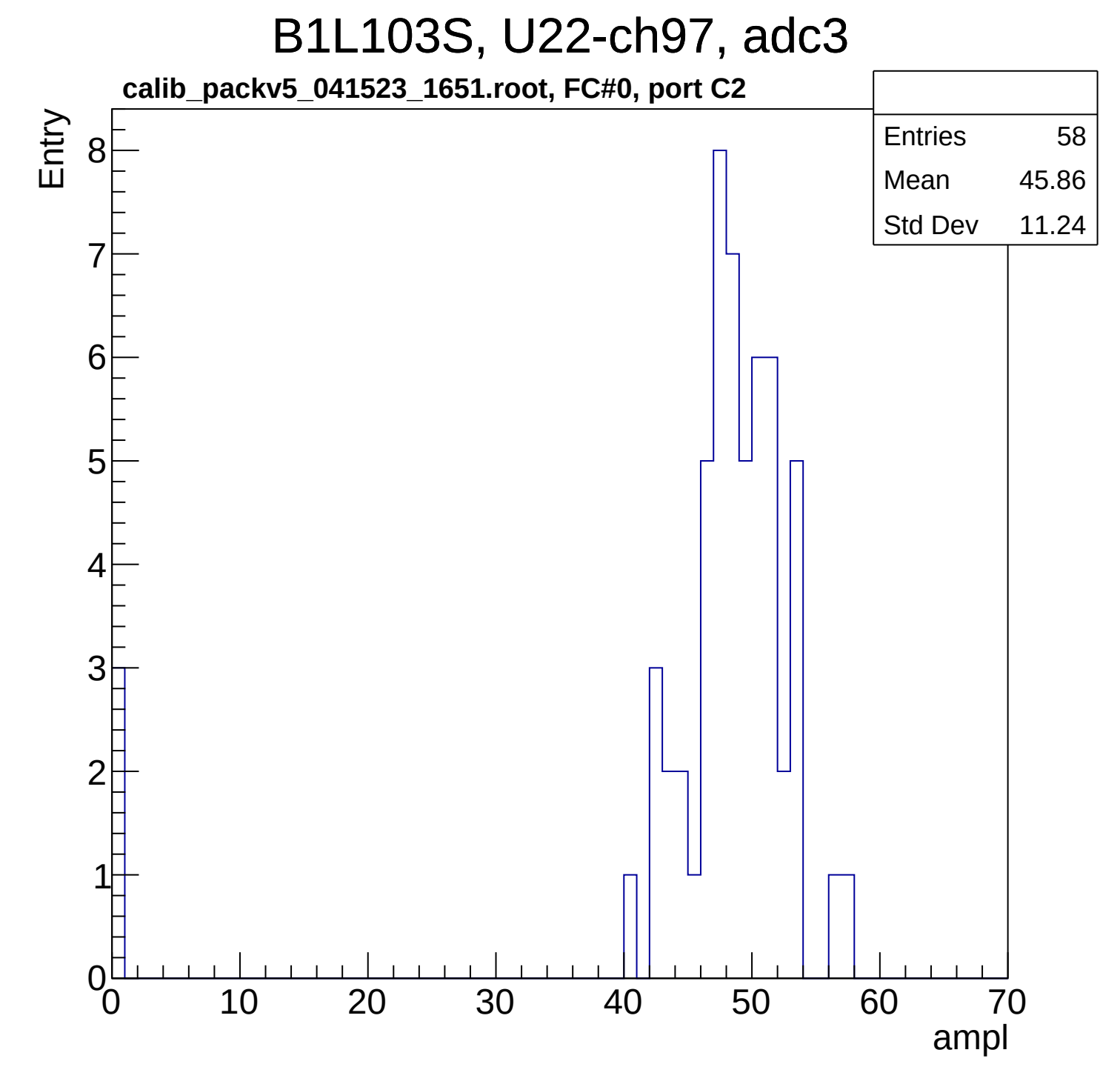

B1L103S, U22-ch96, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61.3
Std Dev 1.1
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

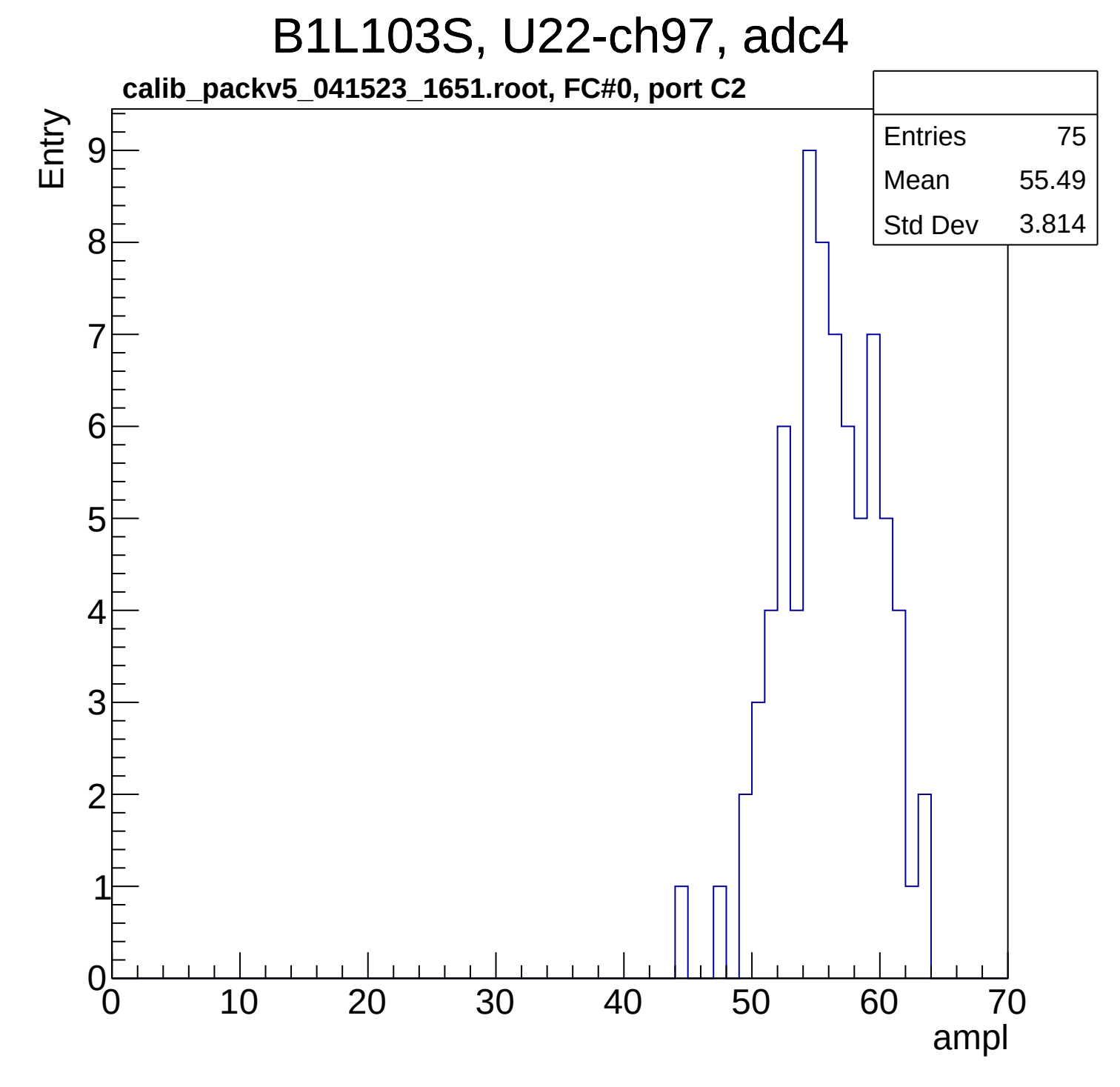

B1L103S, U22-ch96, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 6.524
Std Dev 18.47
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

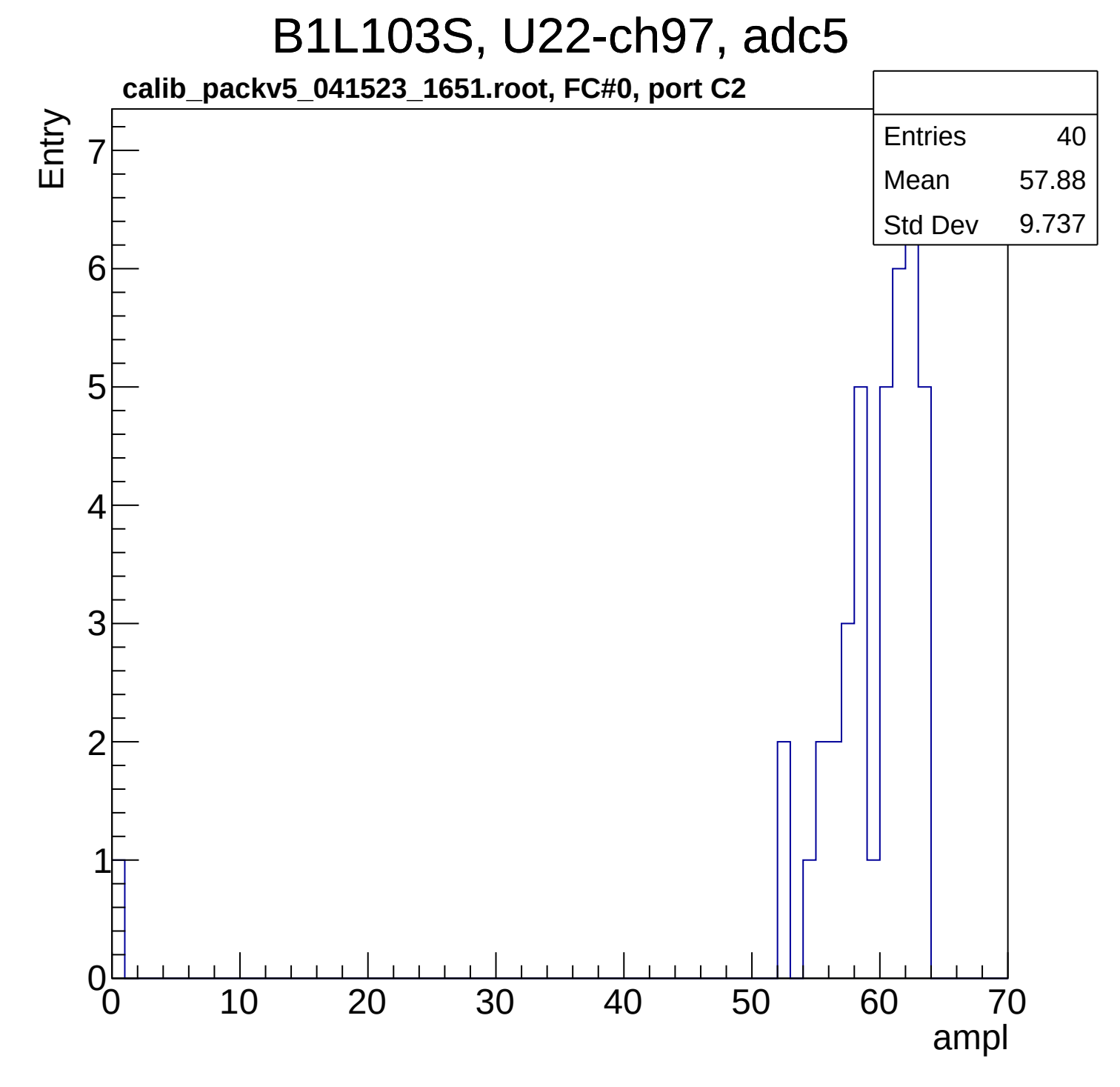

B1L103S, U22-ch97, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 96
Mean 21.86
Std Dev 12.72
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
24
0
10
20
30
40
50
60
70

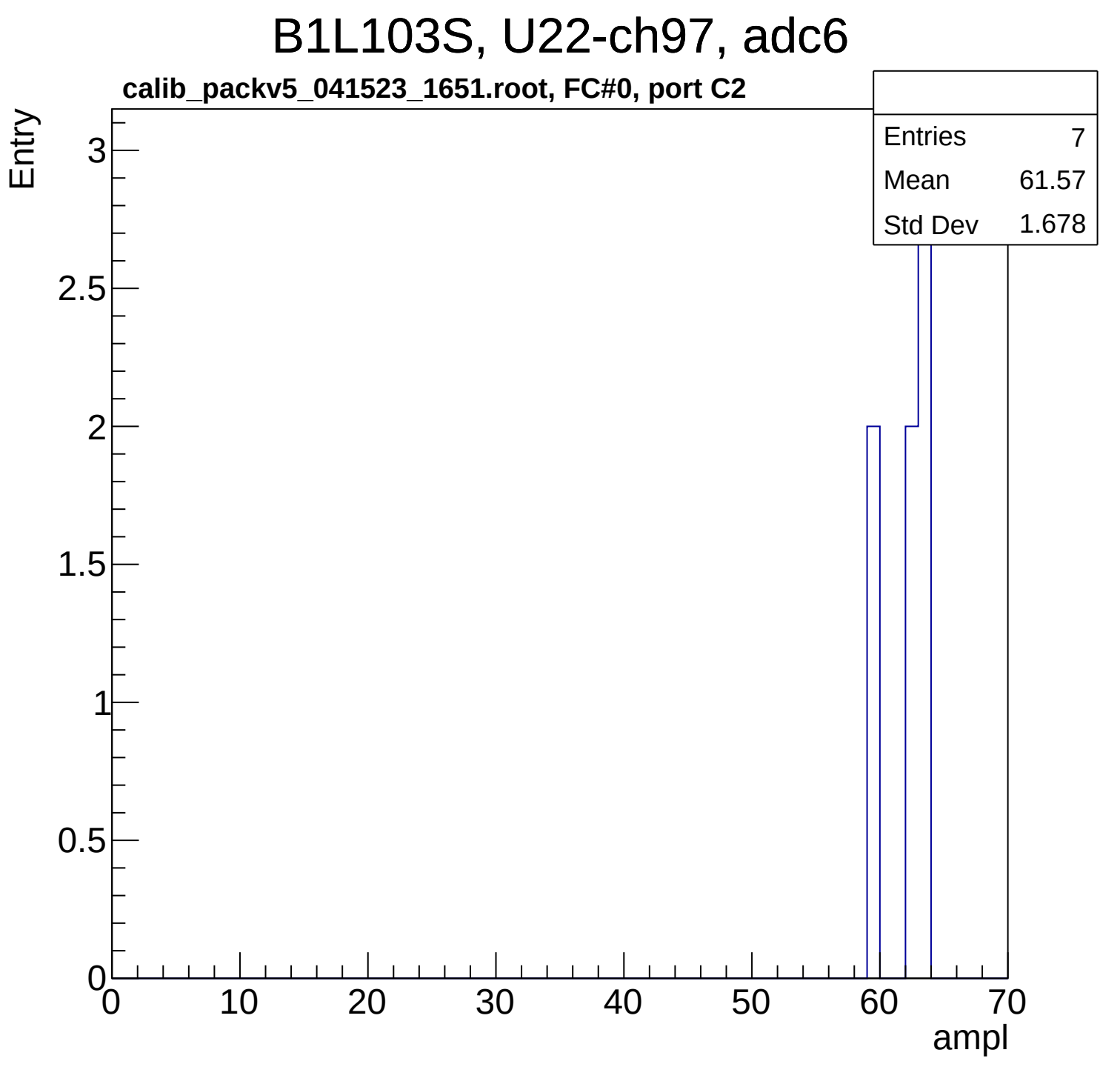

B1L103S, U22-ch97, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 34.61
Std Dev 6.971
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch97, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 35.4
Std Dev 16.25
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch97, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 45.86
Std Dev 11.24
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch97, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 55.49
Std Dev 3.814
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch97, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 57.88
Std Dev 9.737
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U22-ch97, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 61.57
Std Dev 1.678
Entry
ampl
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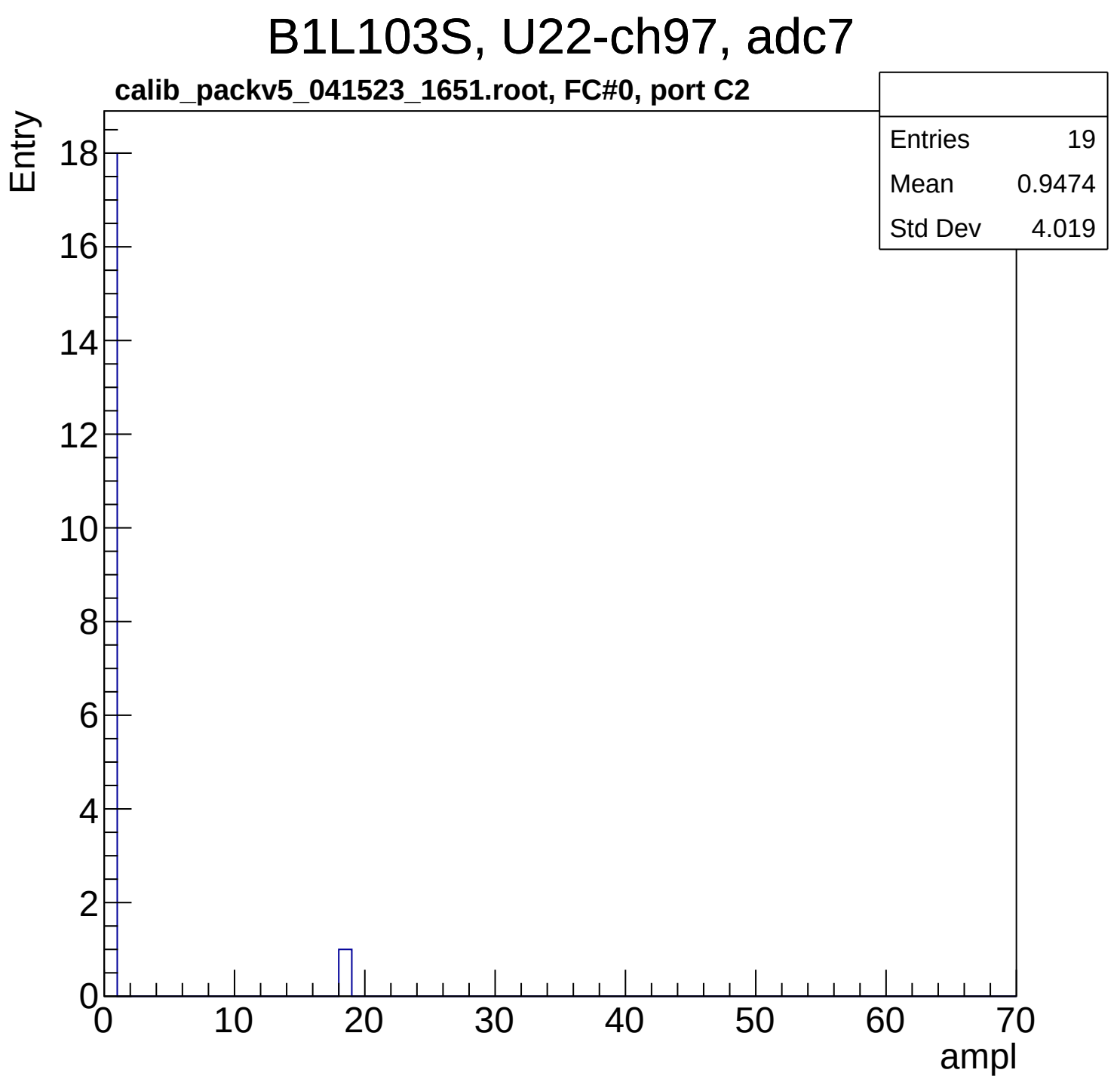
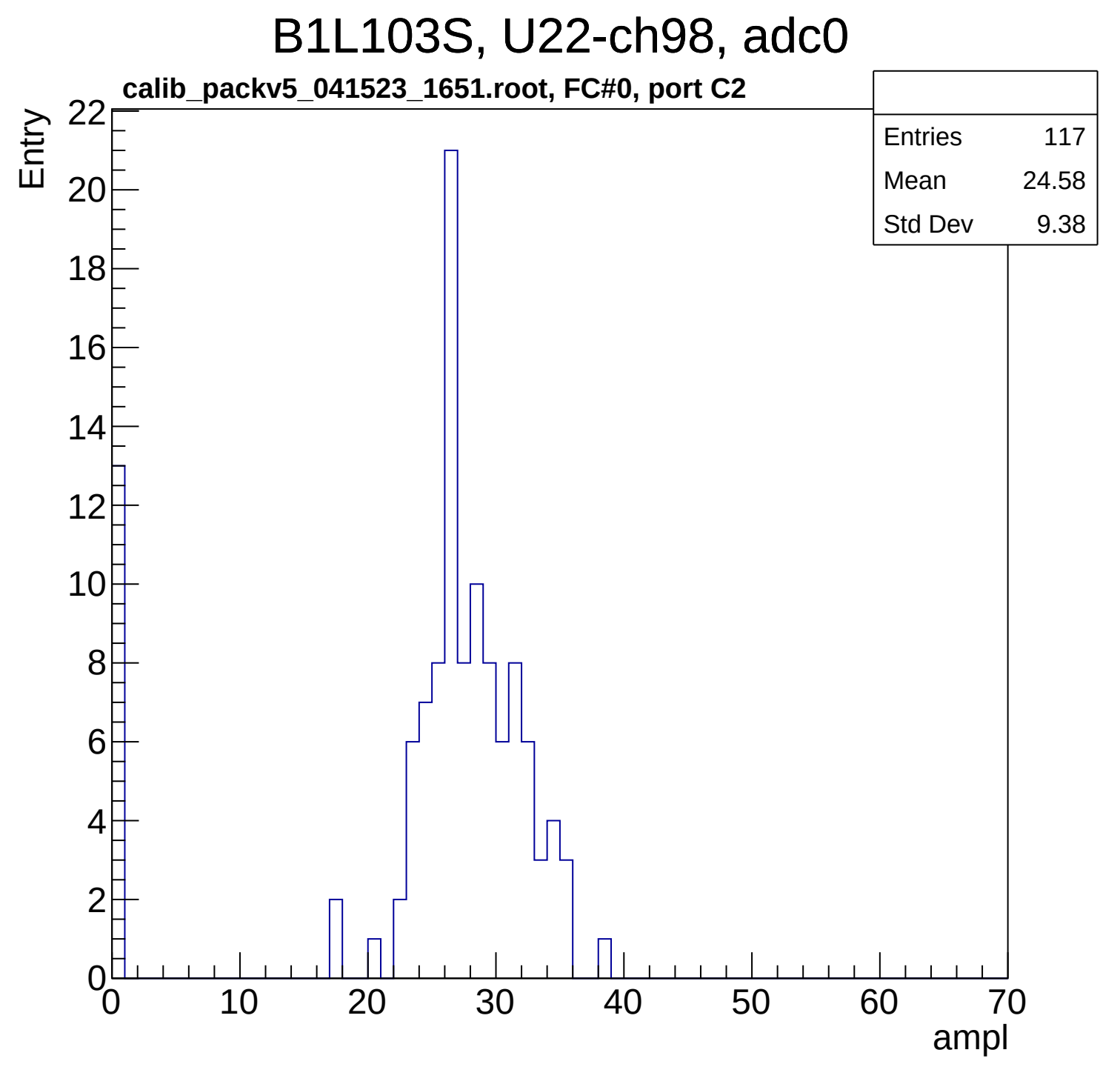
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U22-ch97, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0.9474
Std Dev 4.019
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch98, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 117
Mean 24.58
Std Dev 9.38
Entry
ampl
0
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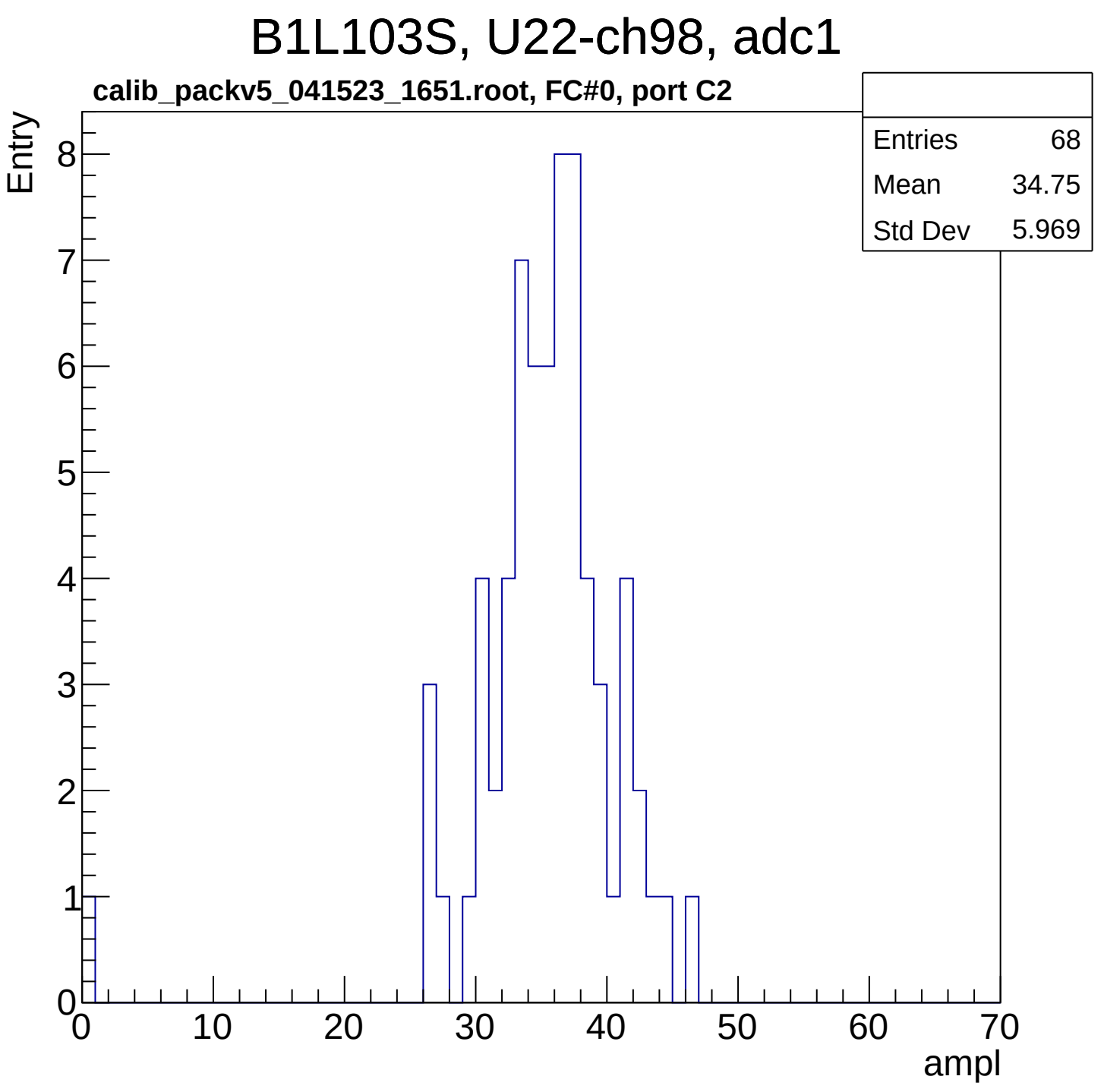
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70


B1L103S, U22-ch98, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 34.75
Std Dev 5.969
Entry
ampl
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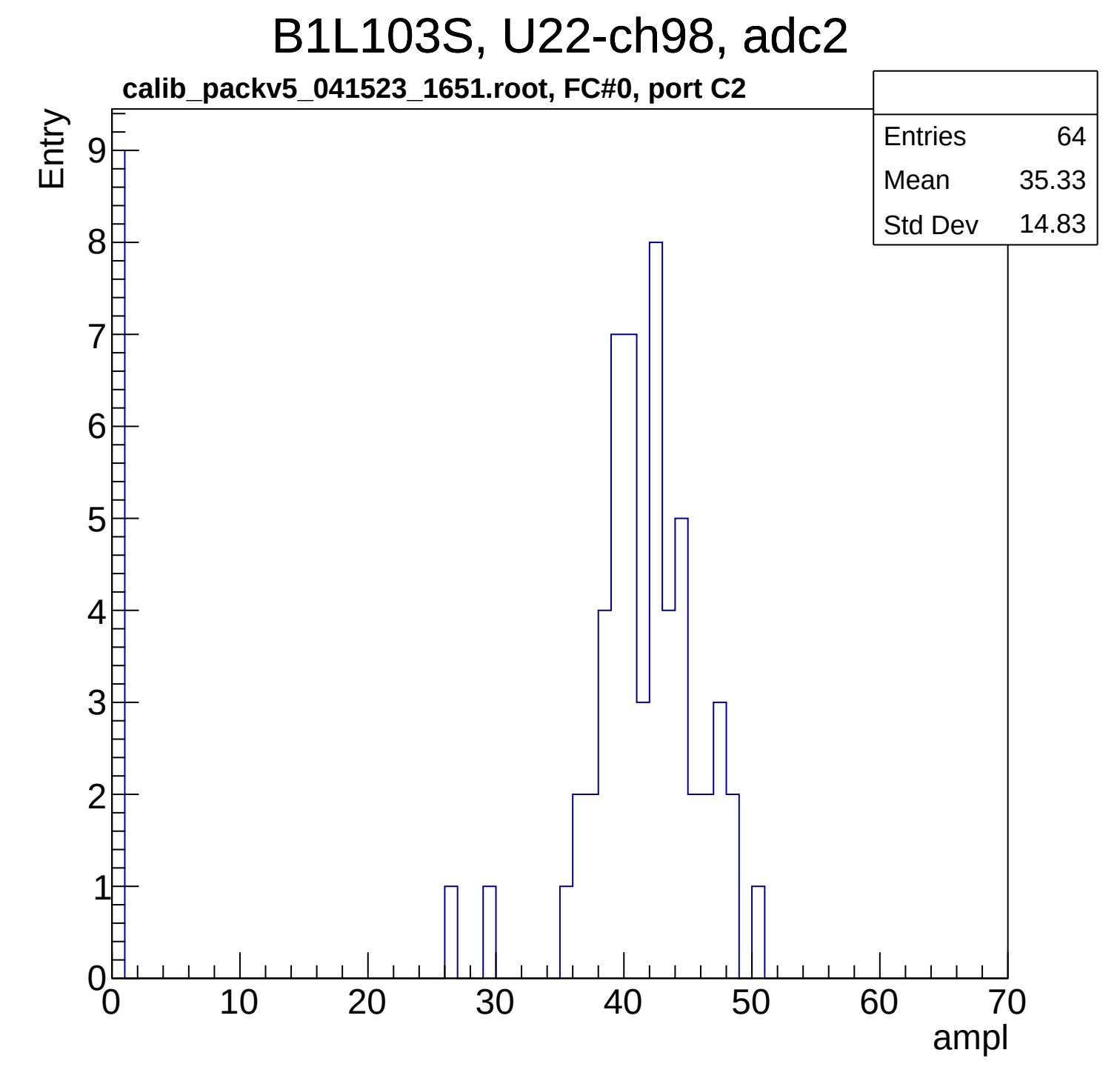
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch98, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 35.33
Std Dev 14.83
Entry
ampl
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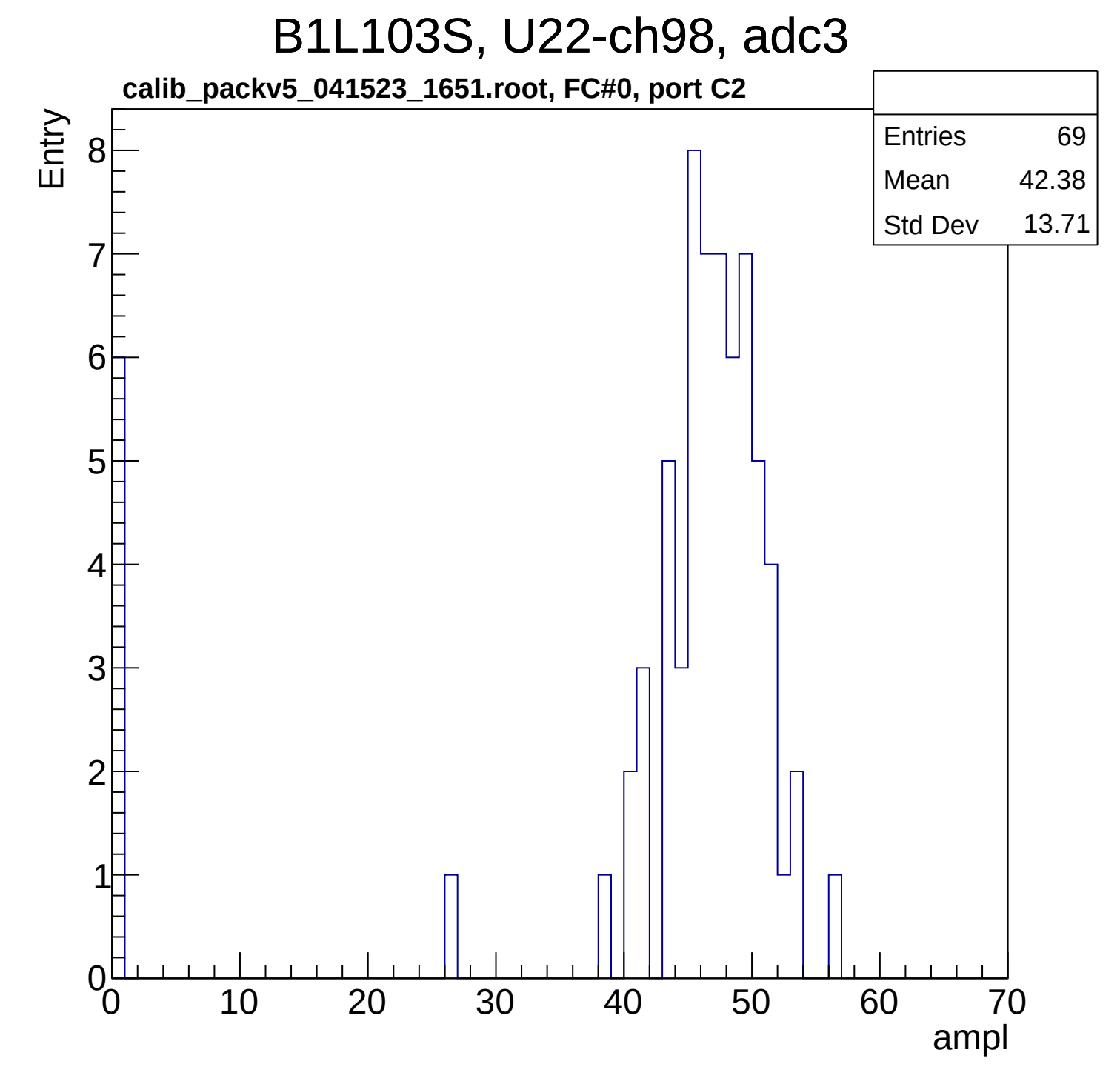
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch98, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 42.38
Std Dev 13.71
Entry
ampl
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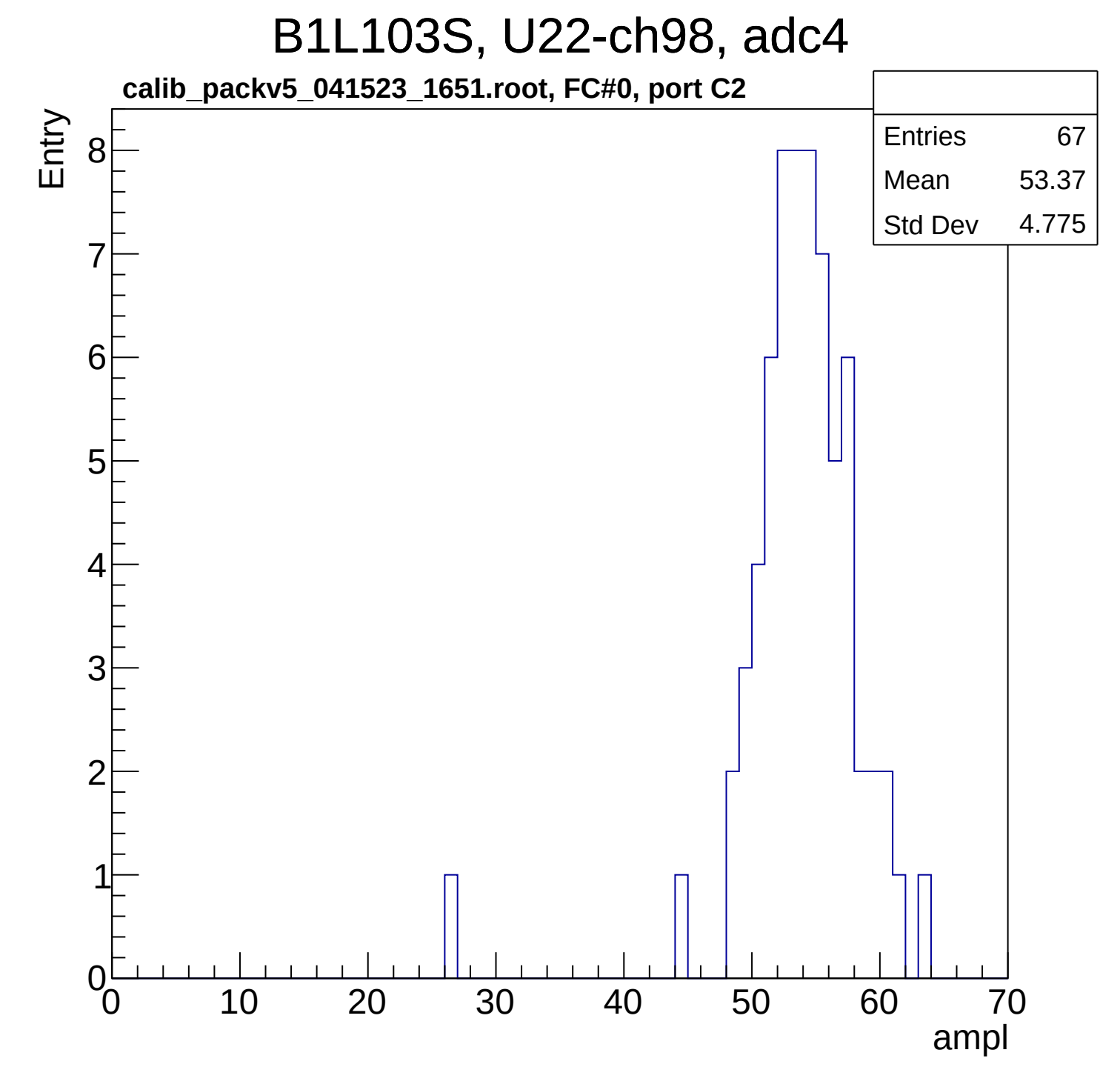
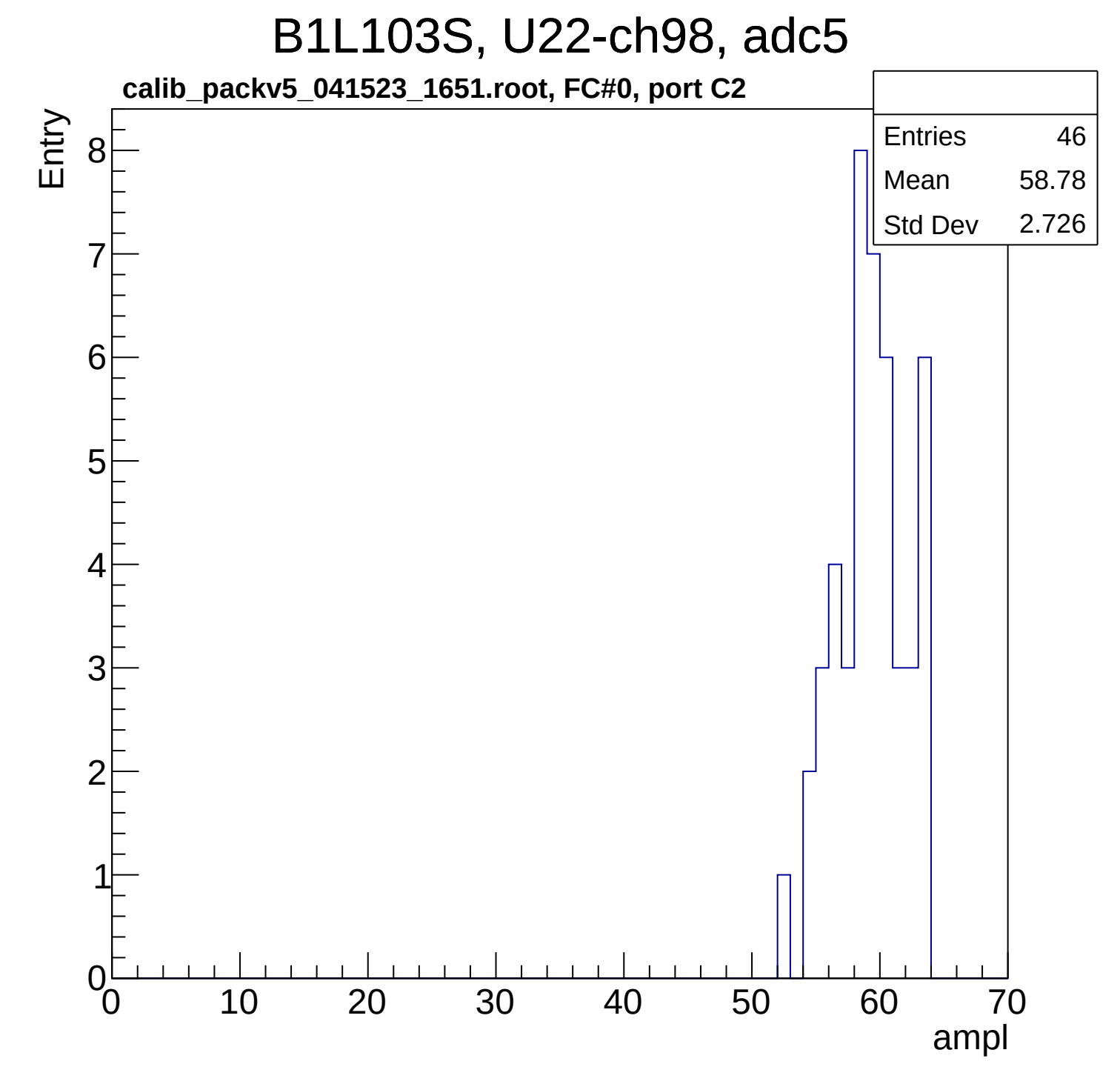
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch98, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 53.37
Std Dev 4.775
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch98, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 58.78
Std Dev 2.726
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
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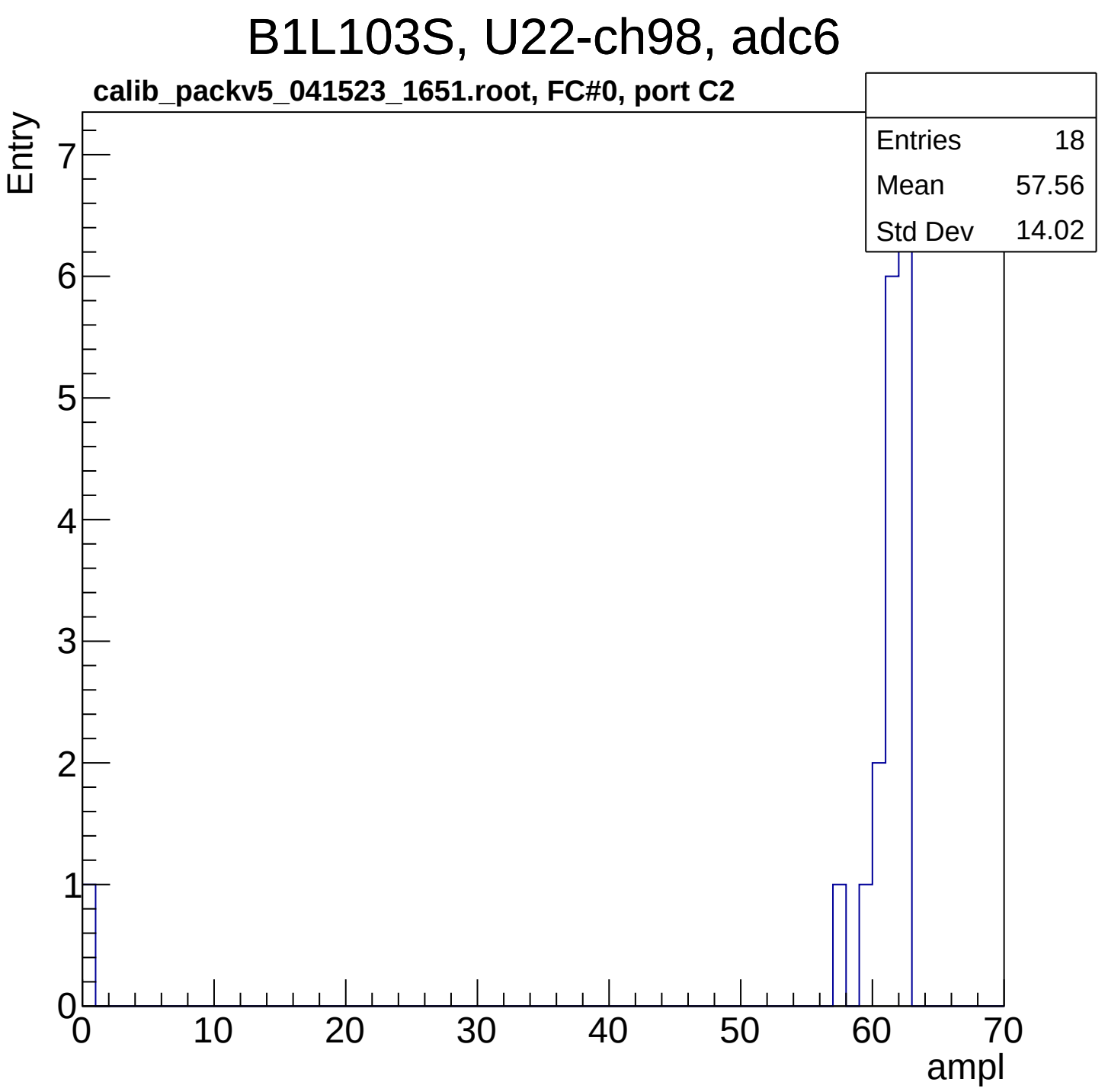
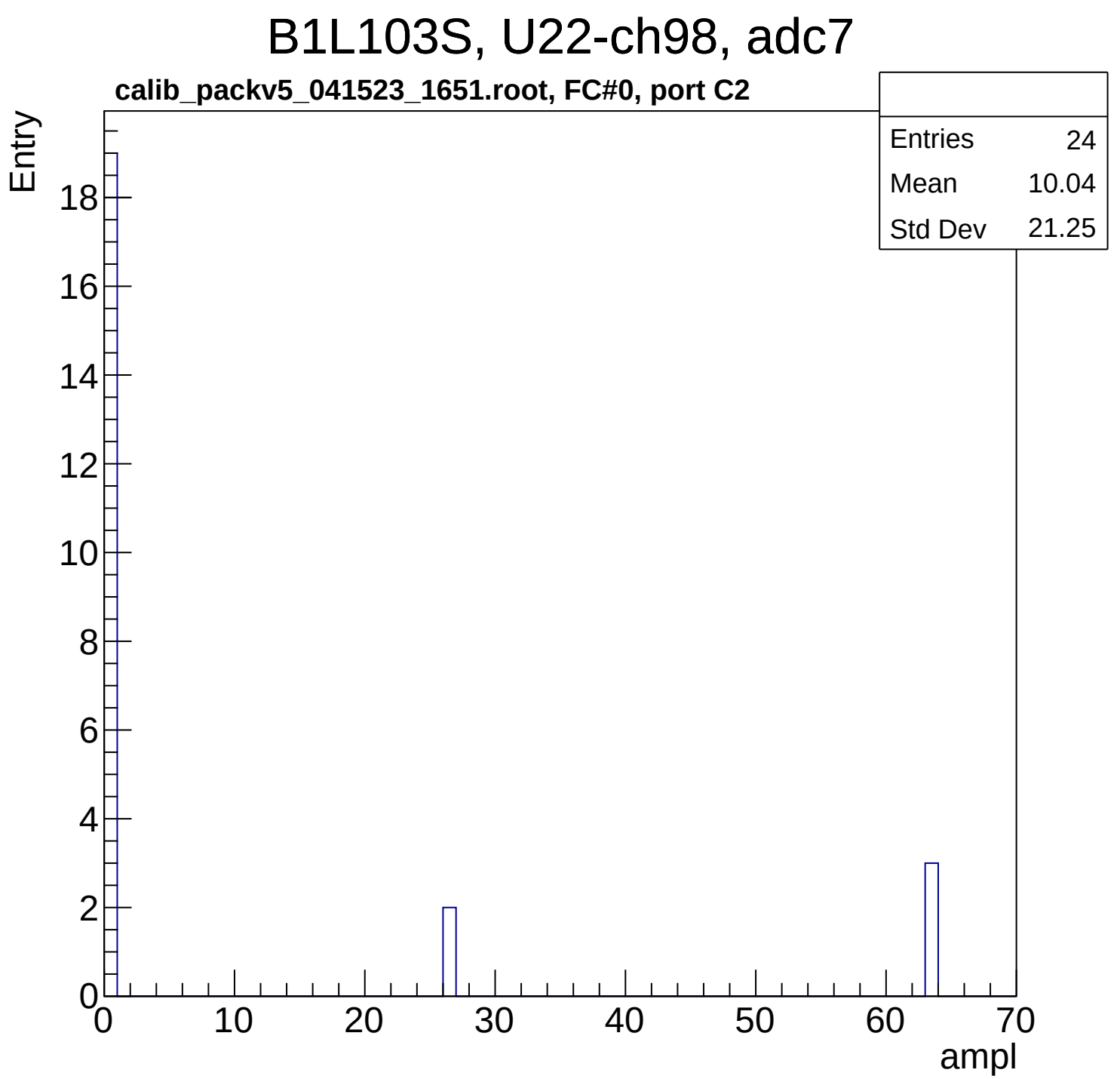
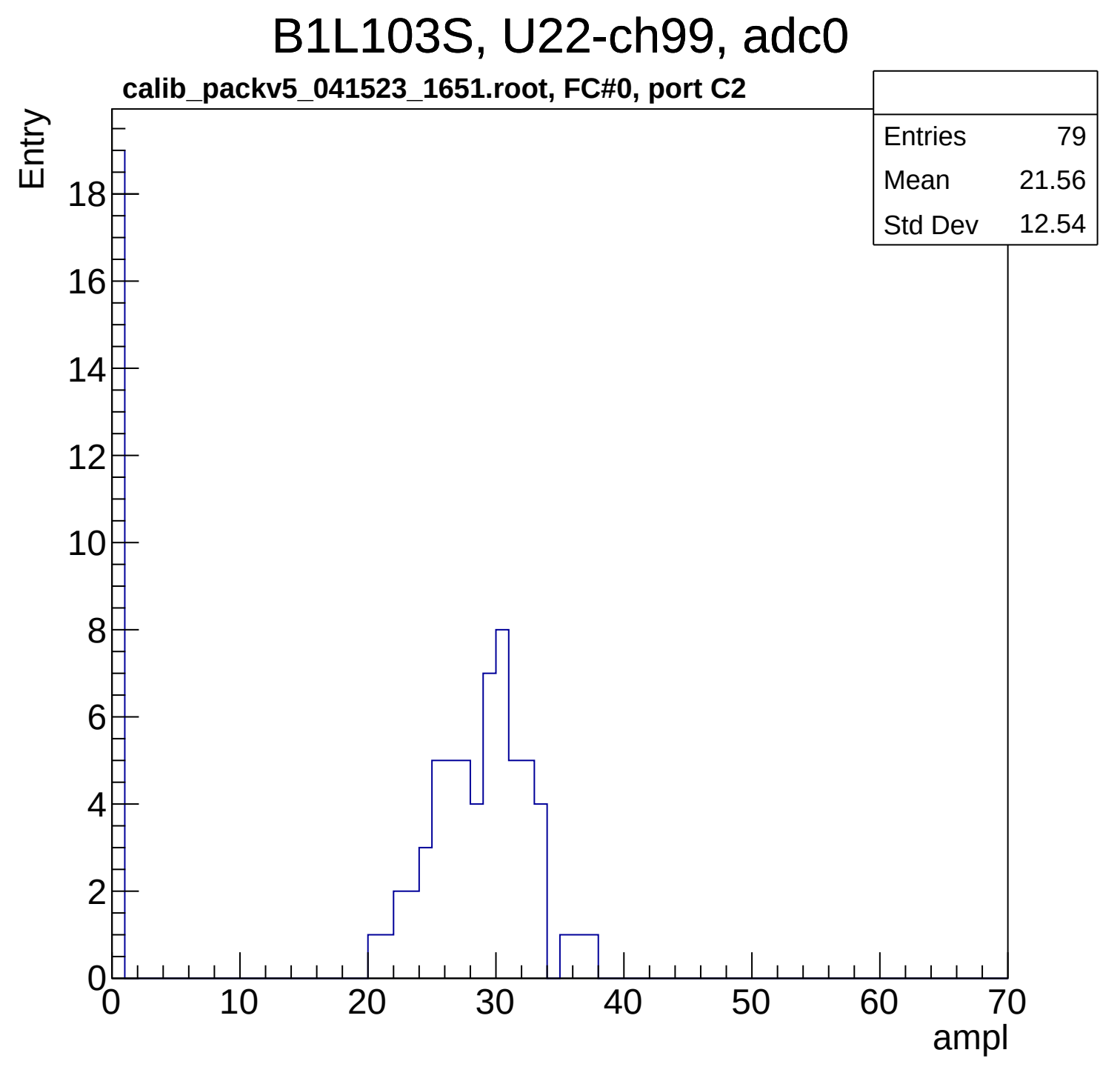
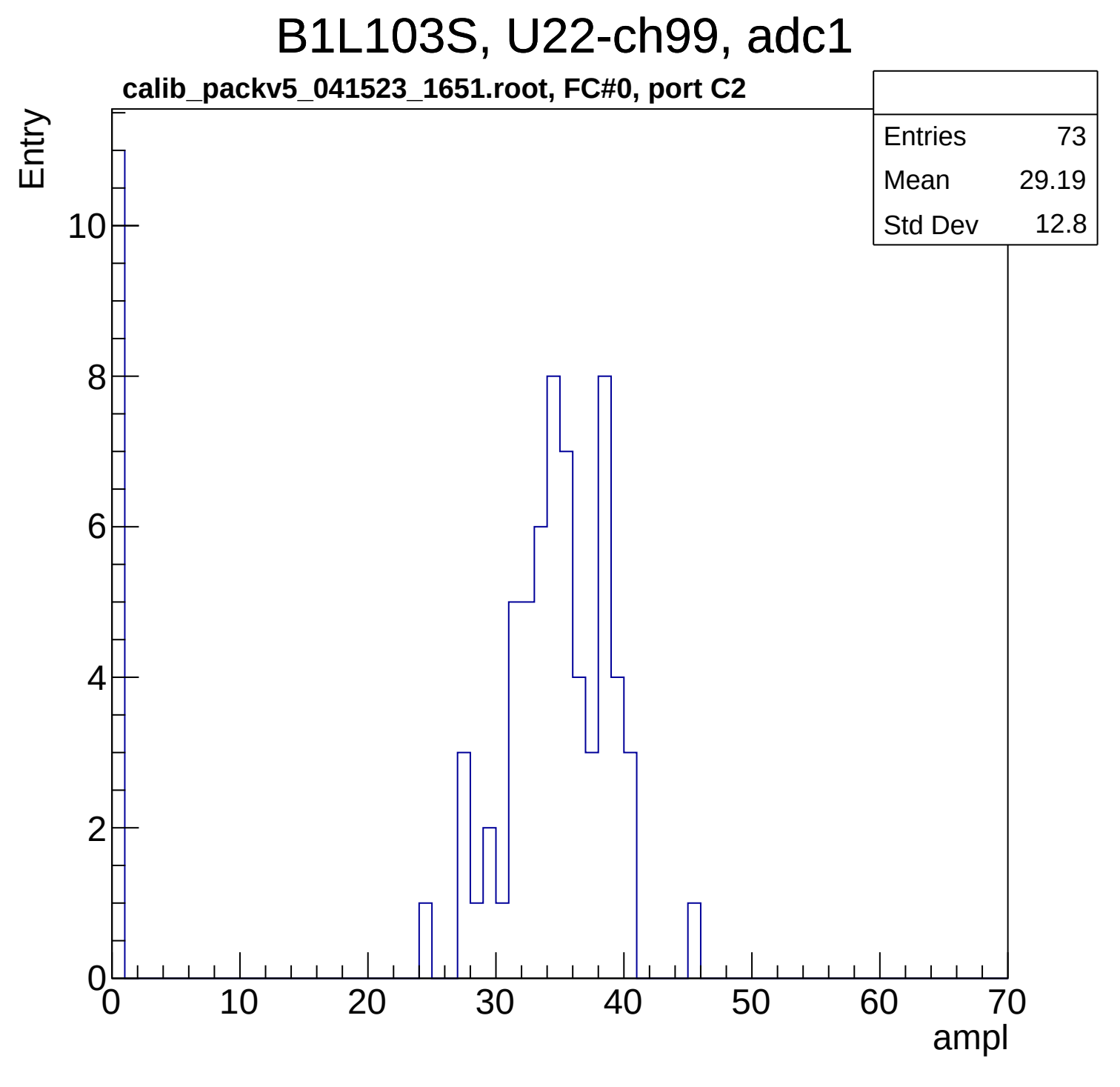
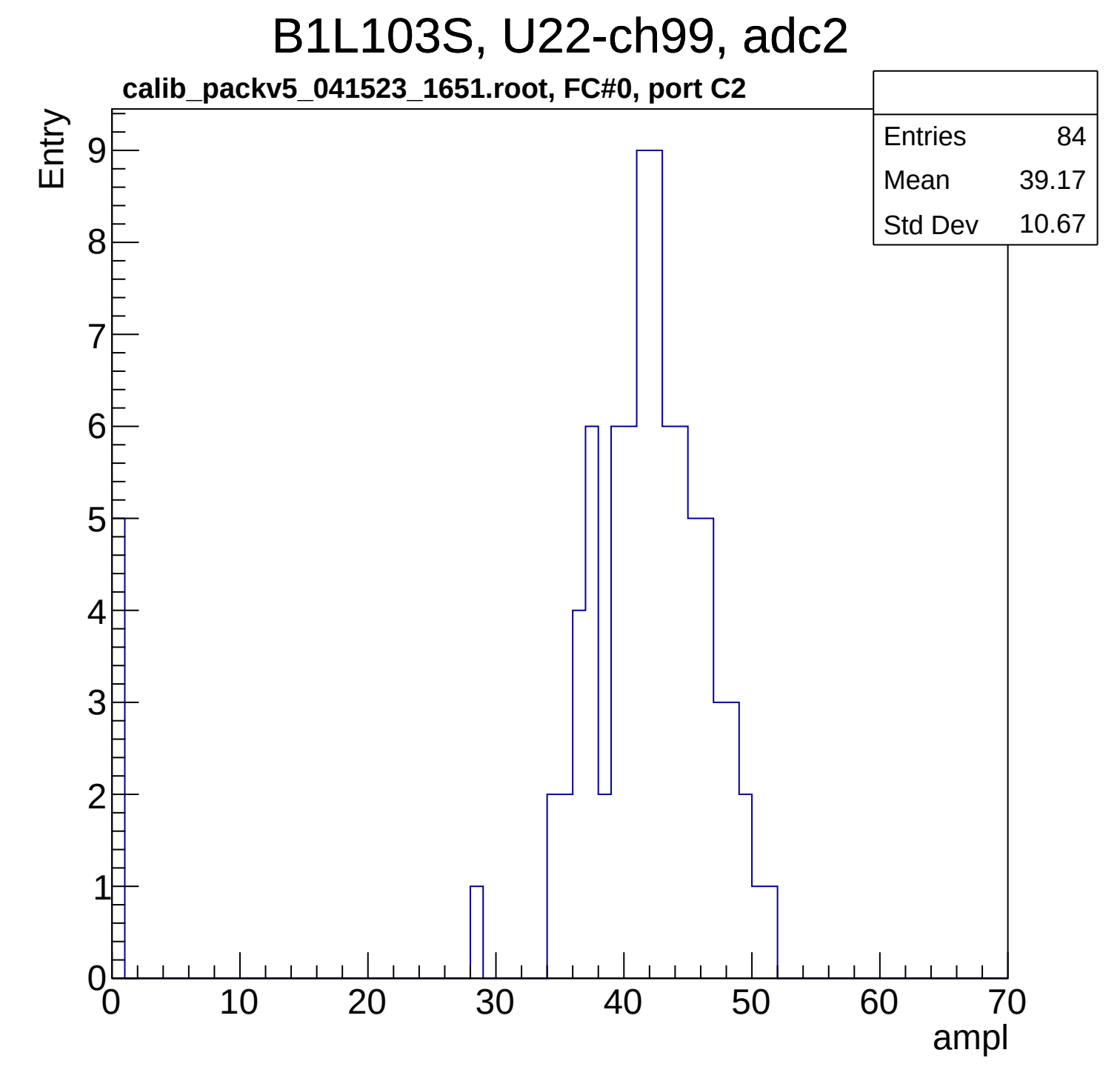
60
70


B1L103S, U22-ch98, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 57.56
Std Dev 14.02
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch98, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 10.04
Std Dev 21.25
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch99, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 21.56
Std Dev 12.54
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch99, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 29.19
Std Dev 12.8
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch99, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 39.17
Std Dev 10.67
Entry
ampl
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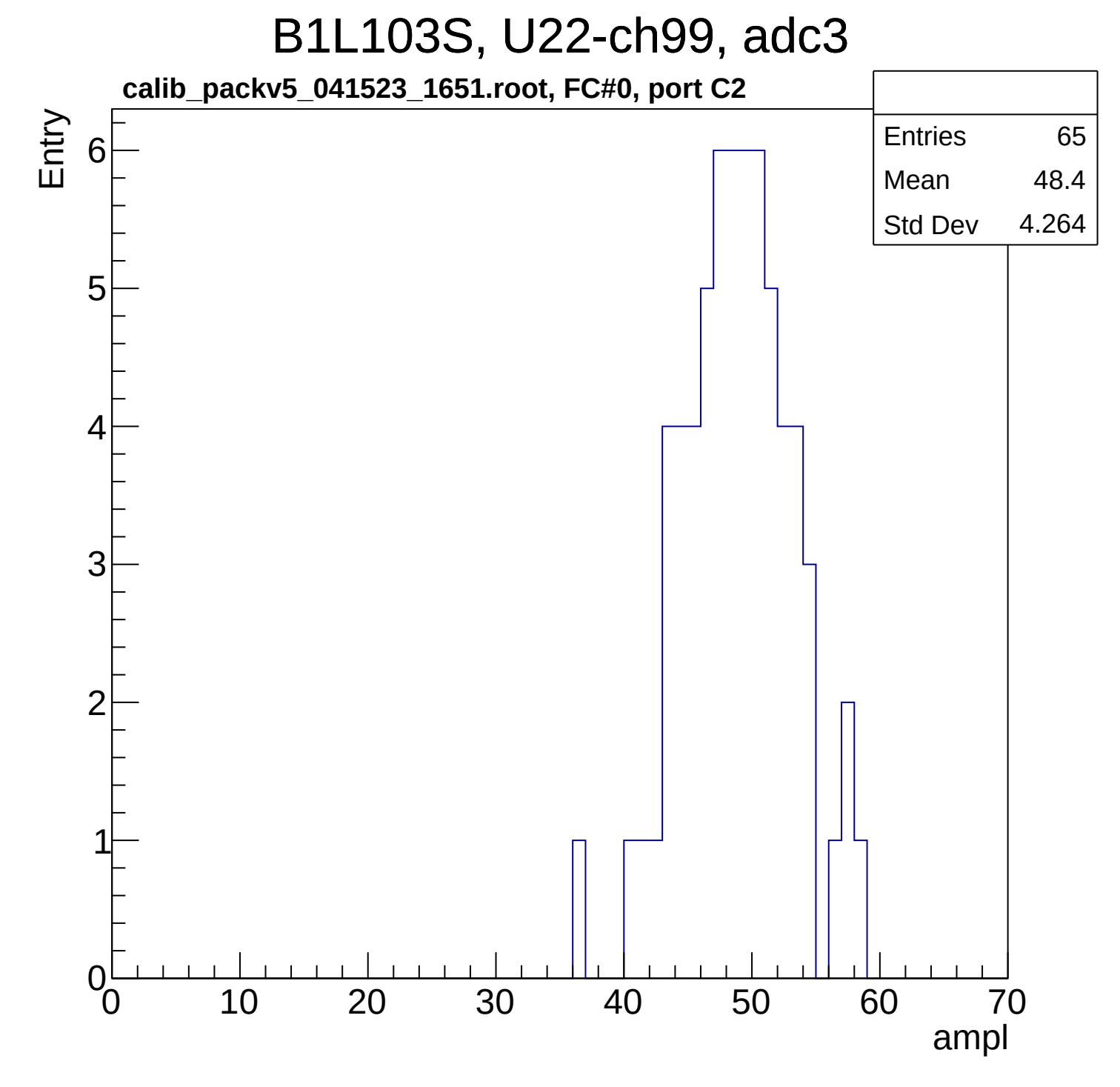
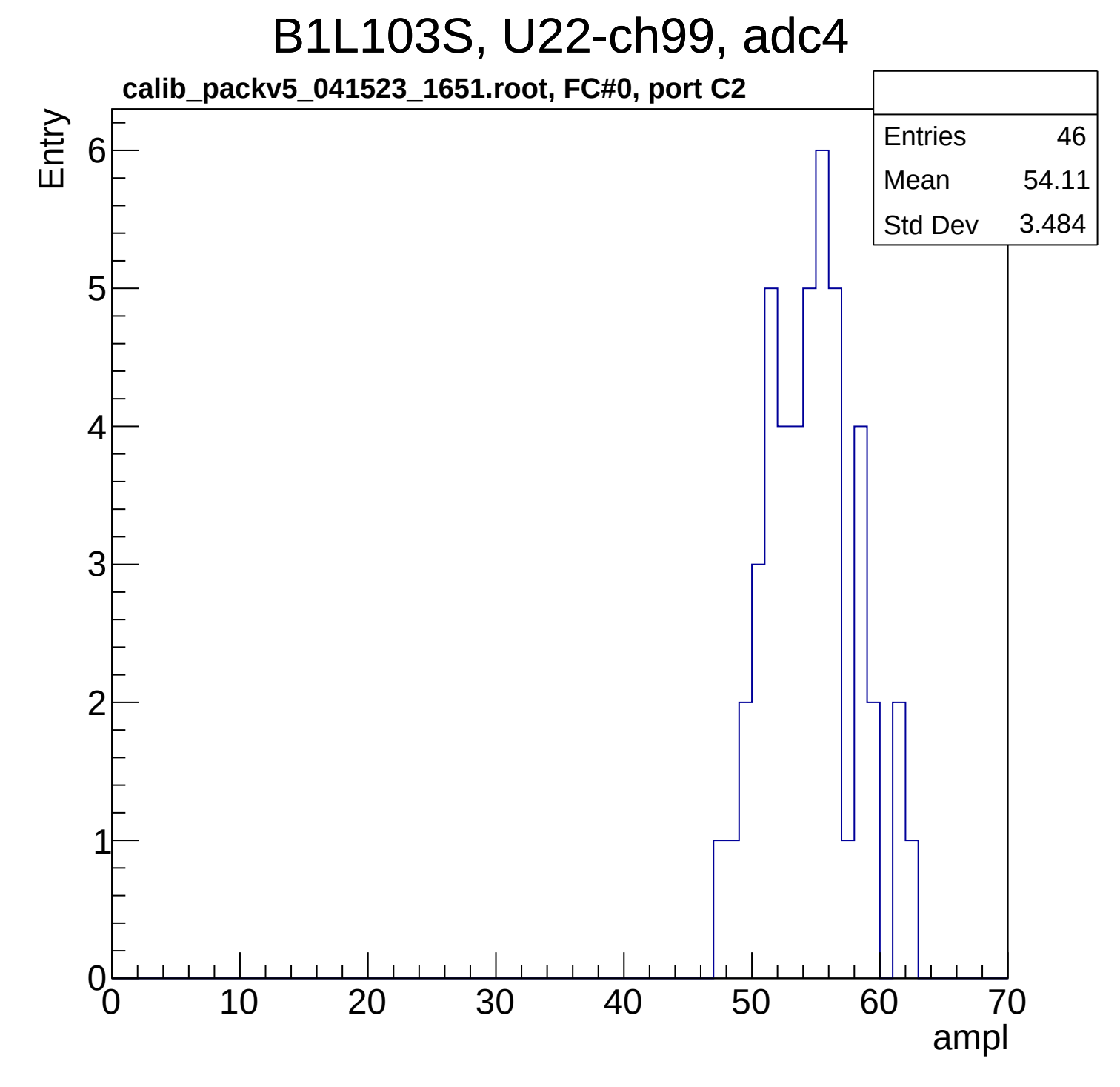
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch99, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 48.4
Std Dev 4.264
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U22-ch99, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 54.11
Std Dev 3.484
Entry
ampl
0
1
2
3
4
5
6
0
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20
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40
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60
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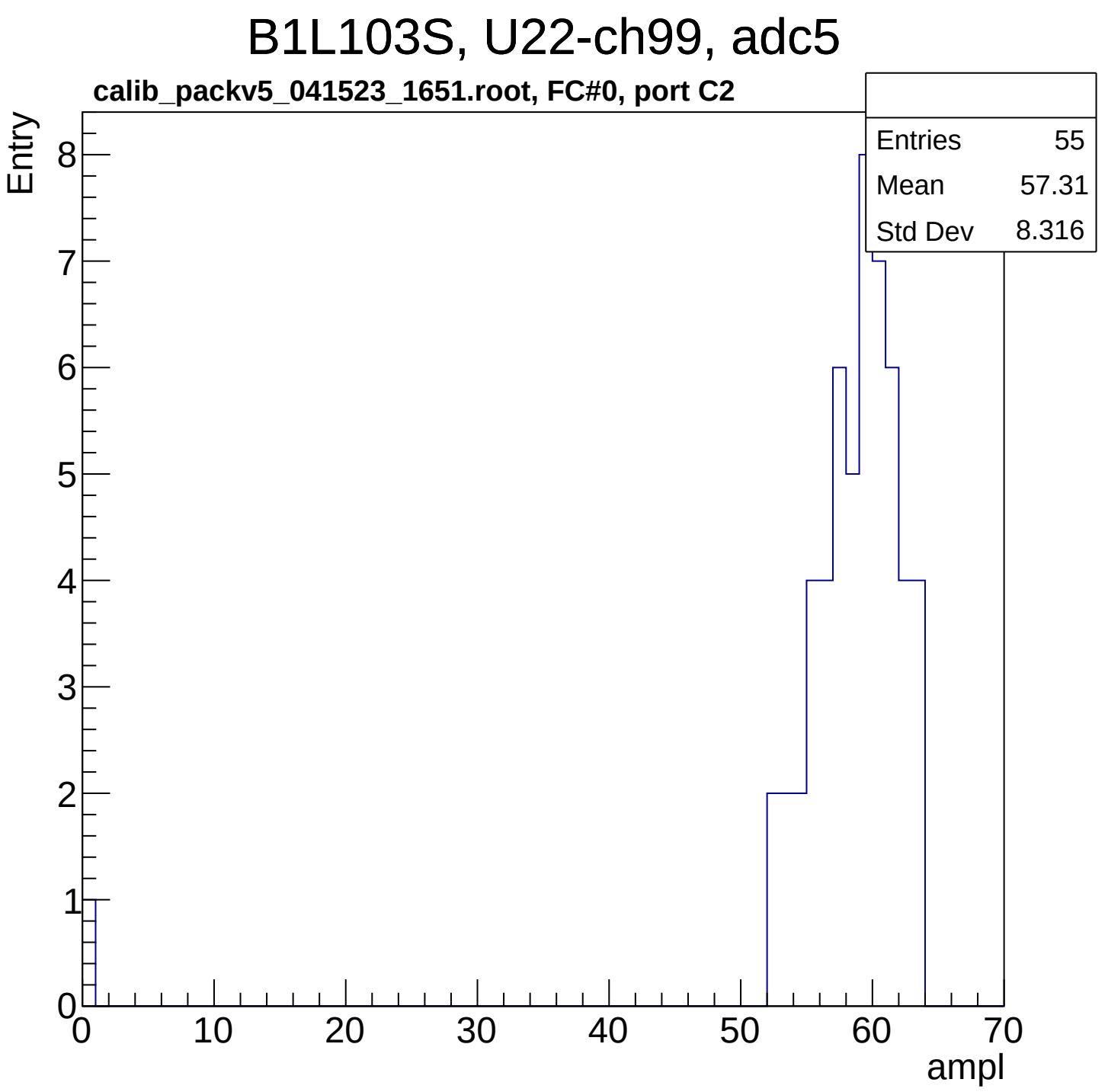
B1L103S, U22-ch99, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 57.31
Std Dev 8.316
Entry
0
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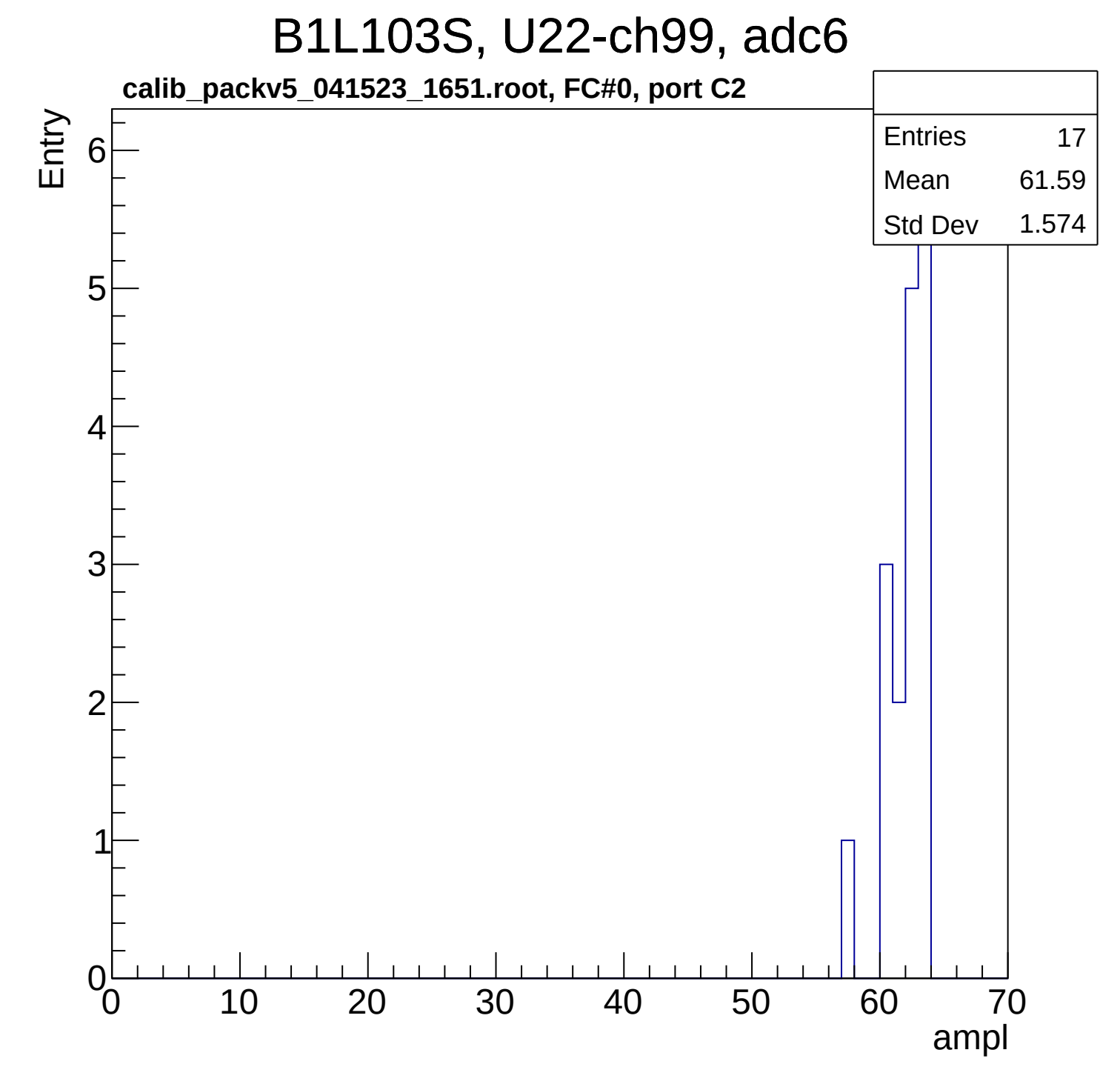
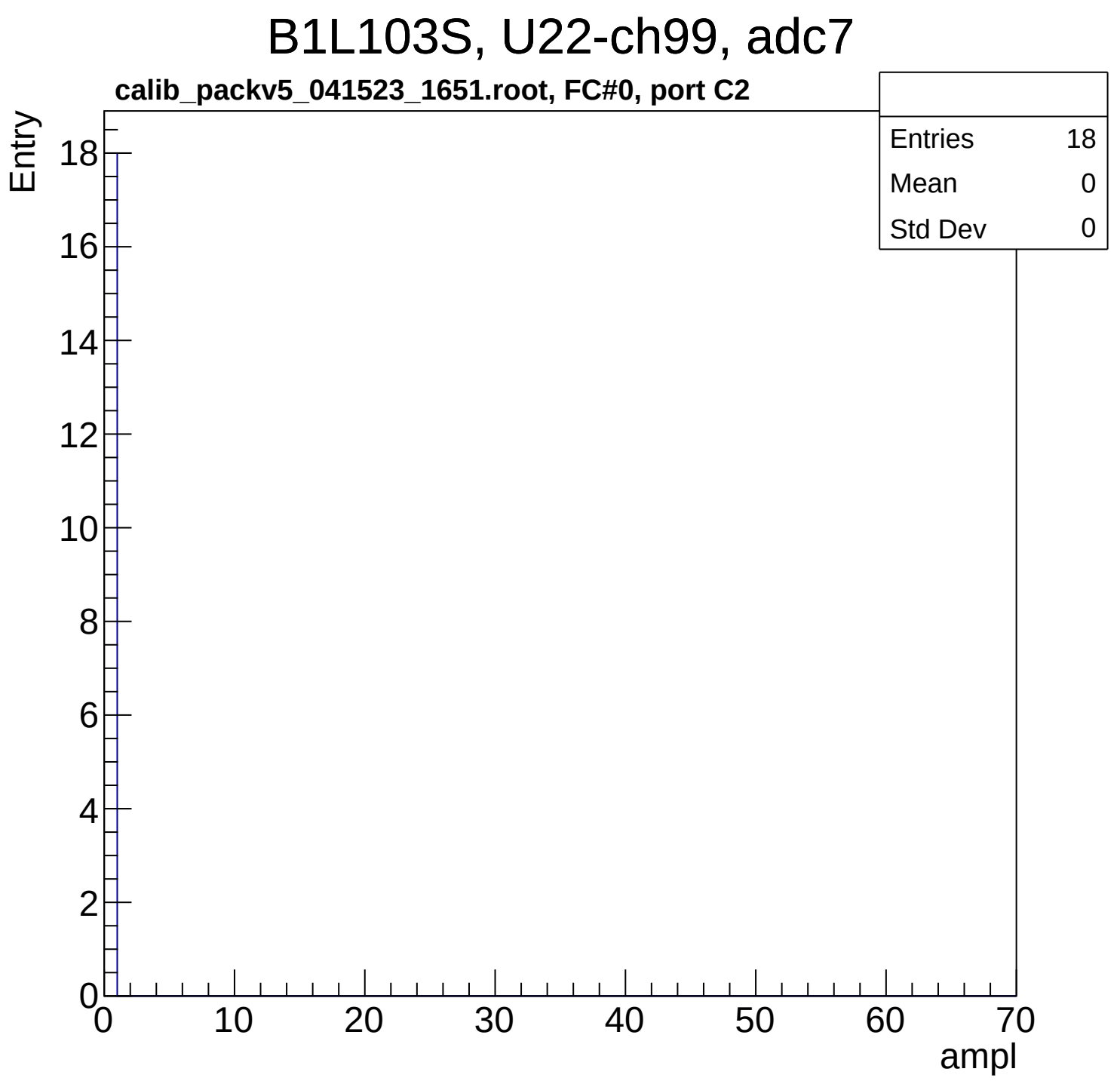
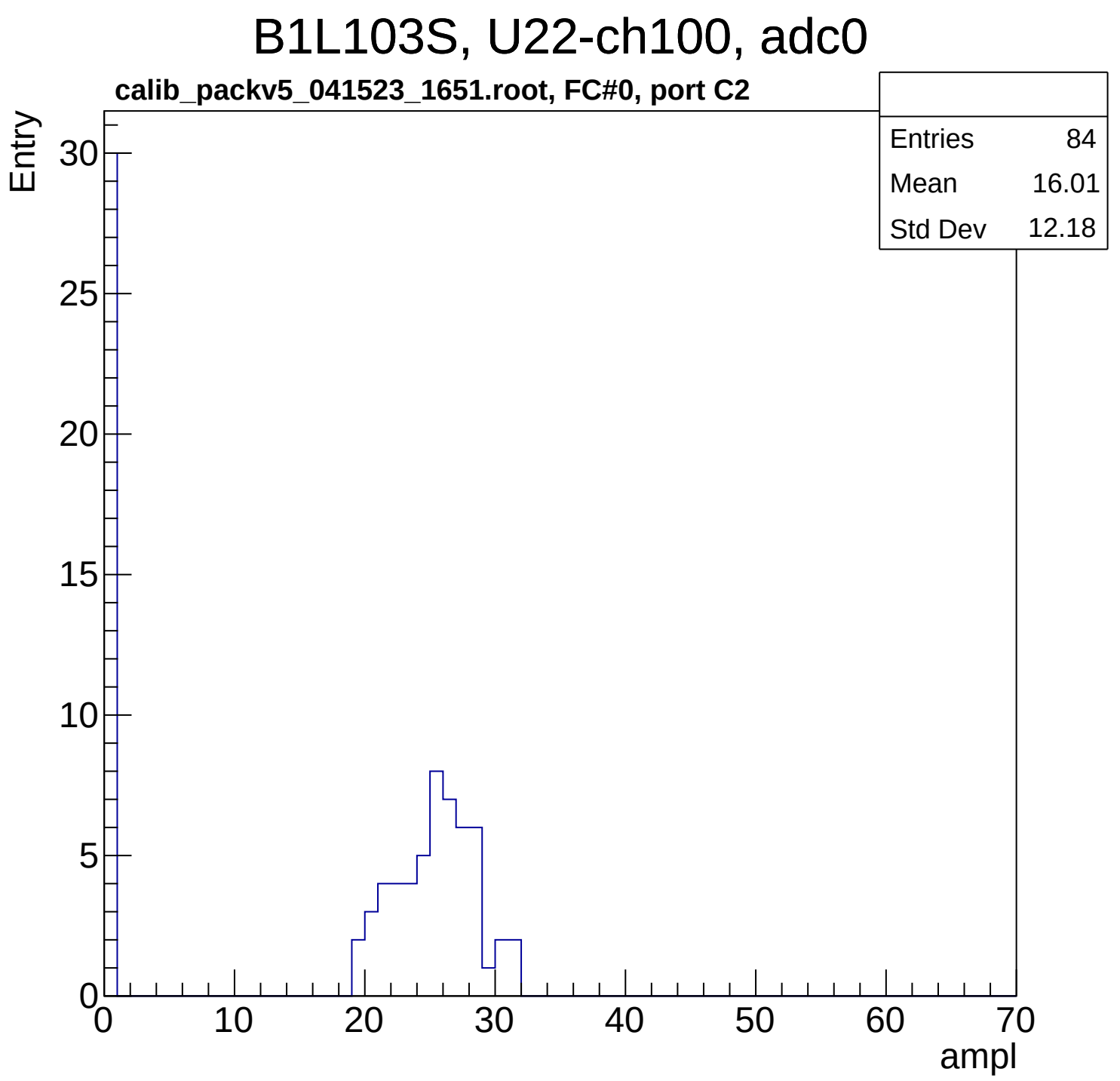
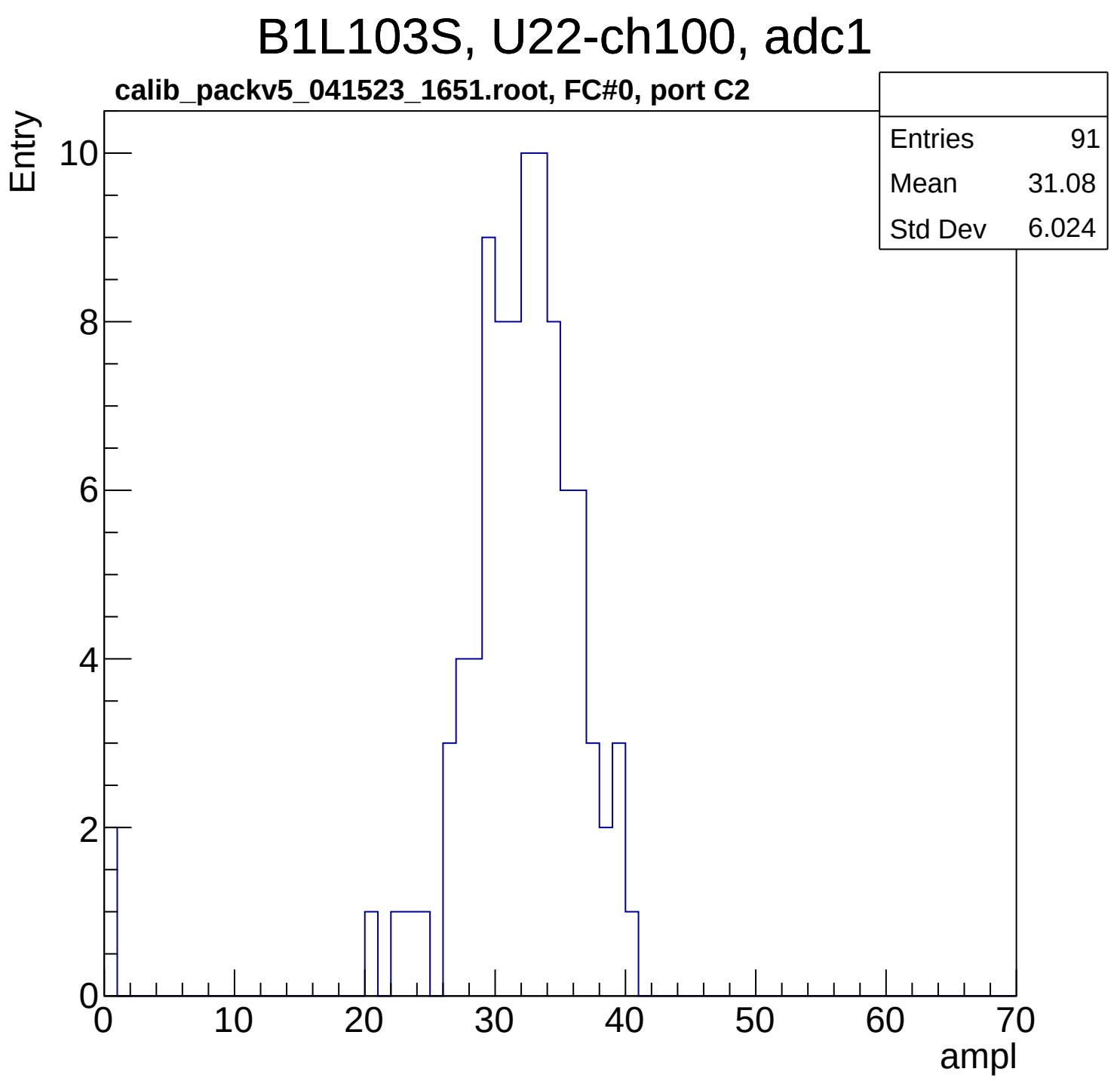
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch99, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 61.59
Std Dev 1.574
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U22-ch99, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch100, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 16.01
Std Dev 12.18
Entry
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch100, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 31.08
Std Dev 6.024
Entry
ampl
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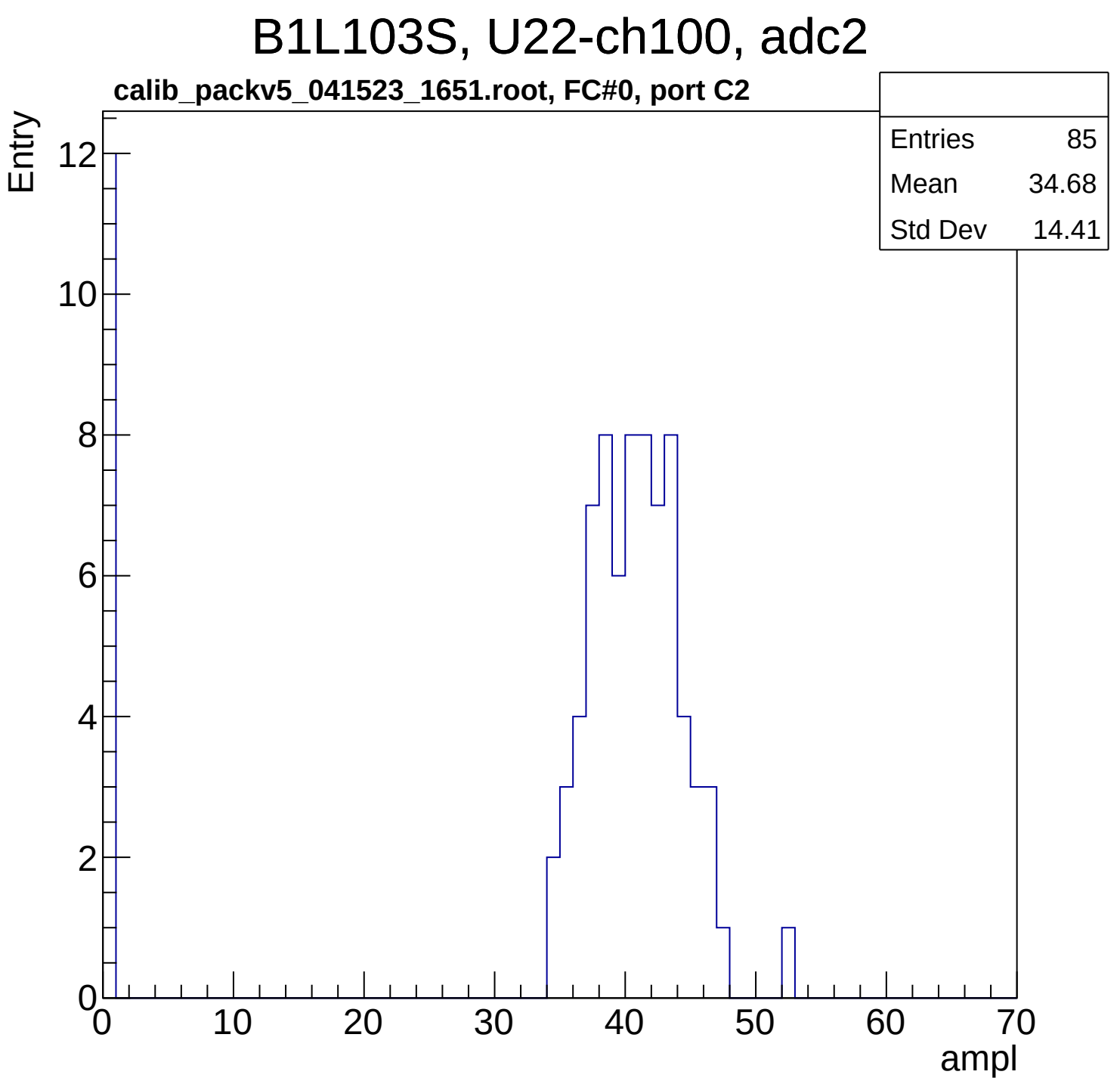
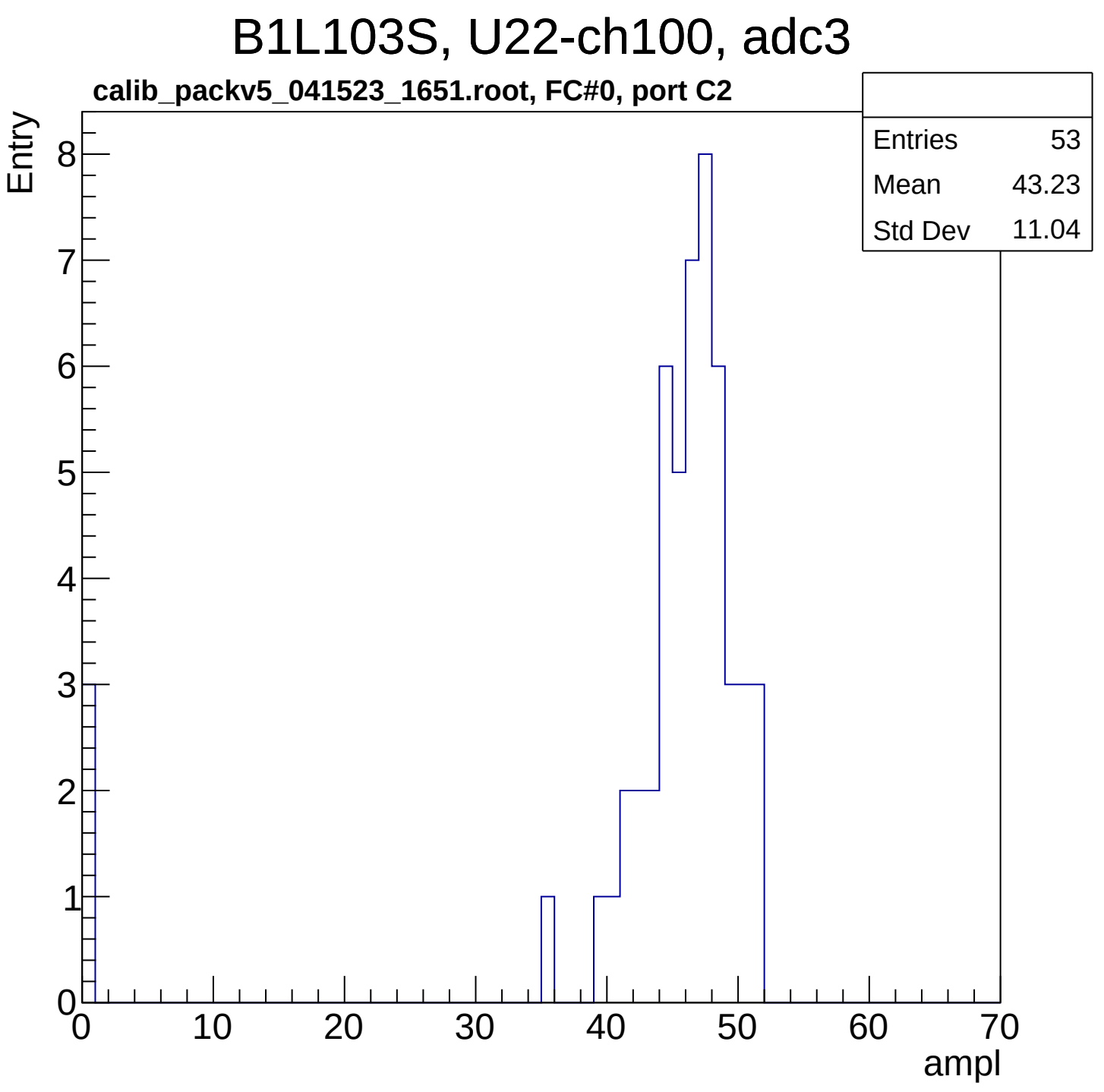
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U22-ch100, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 34.68
Std Dev 14.41
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch100, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 43.23
Std Dev 11.04
Entry
ampl
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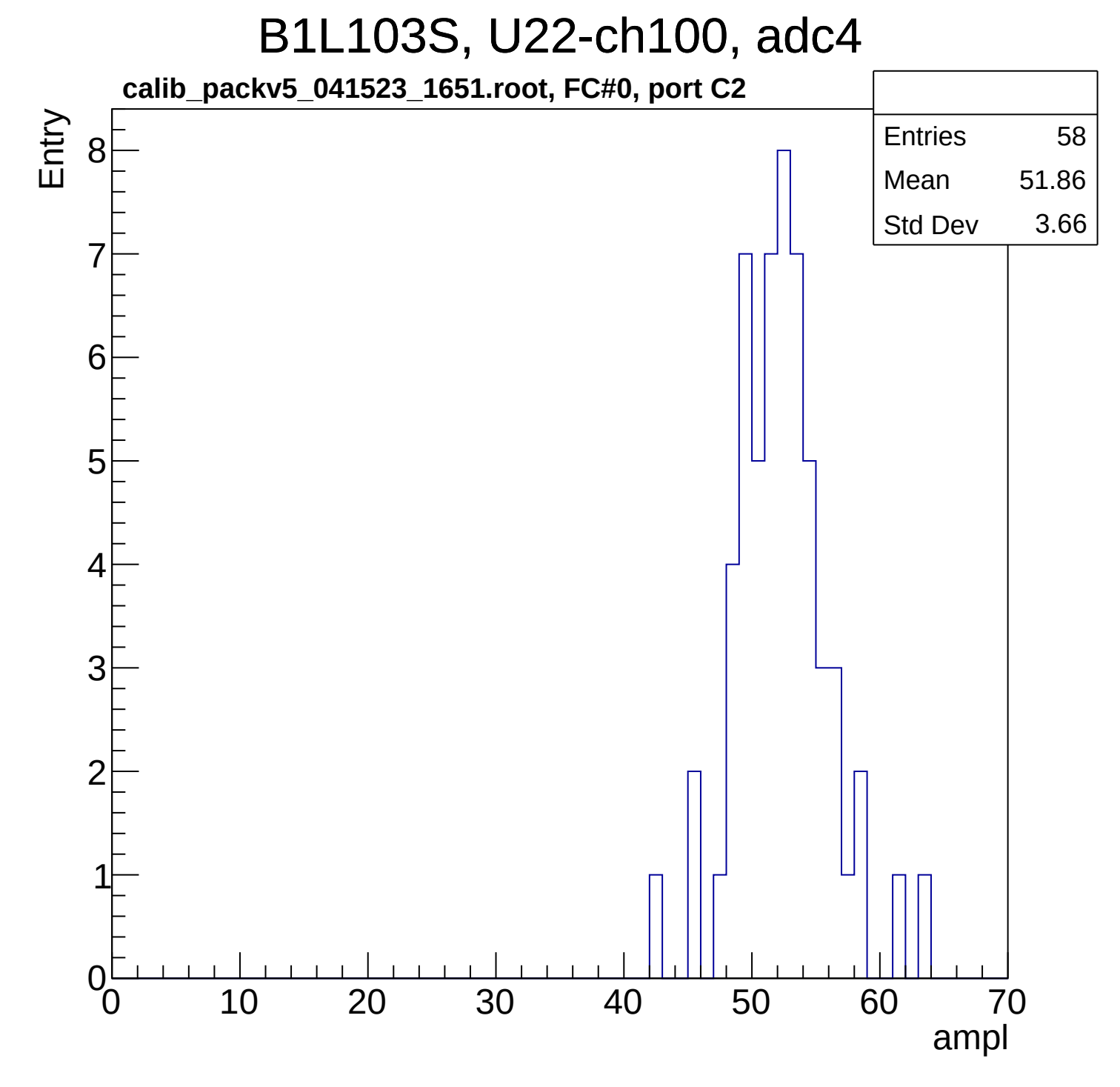
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch100, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 51.86
Std Dev 3.66
Entry
ampl
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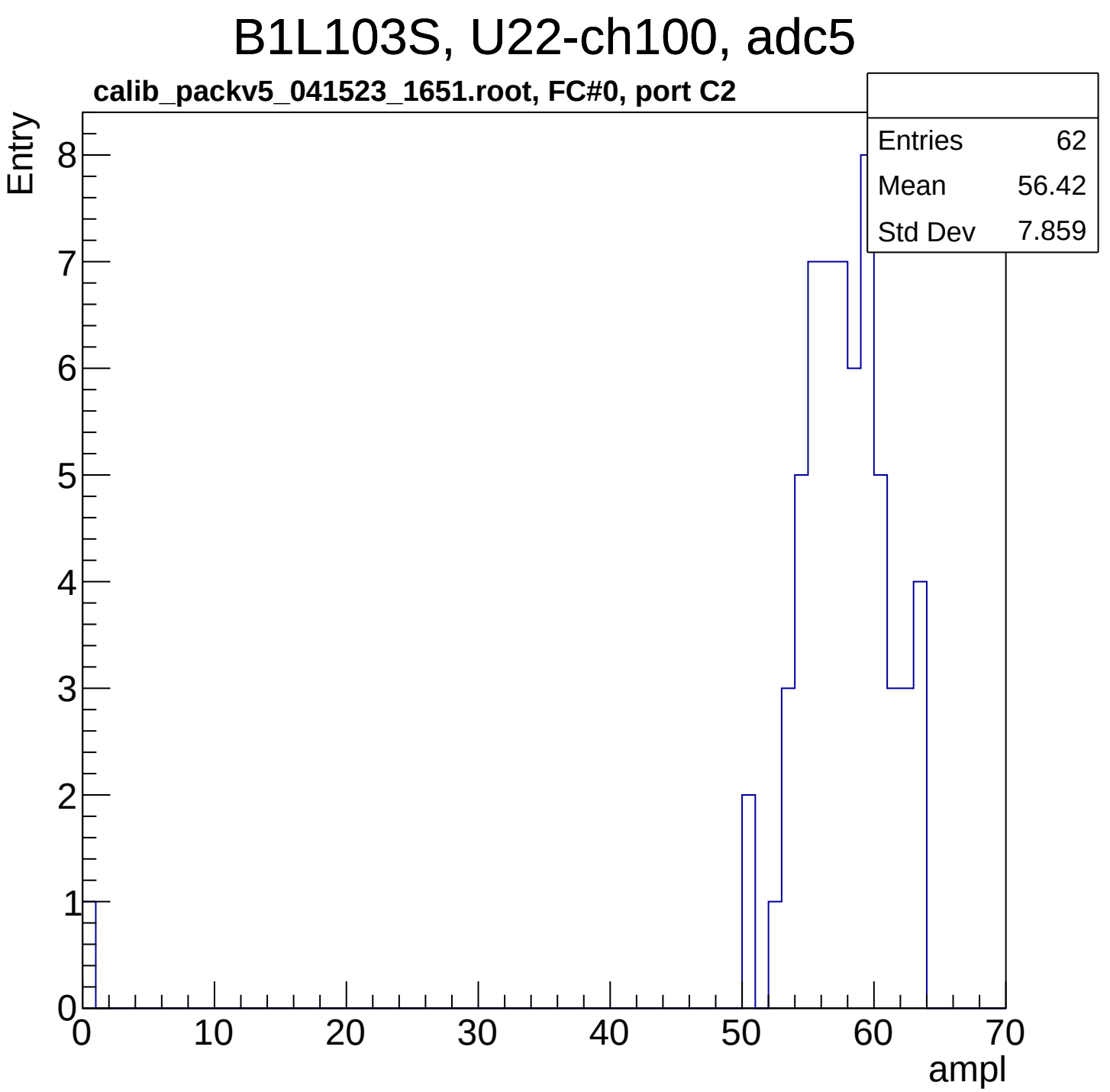
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch100, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 56.42
Std Dev 7.859
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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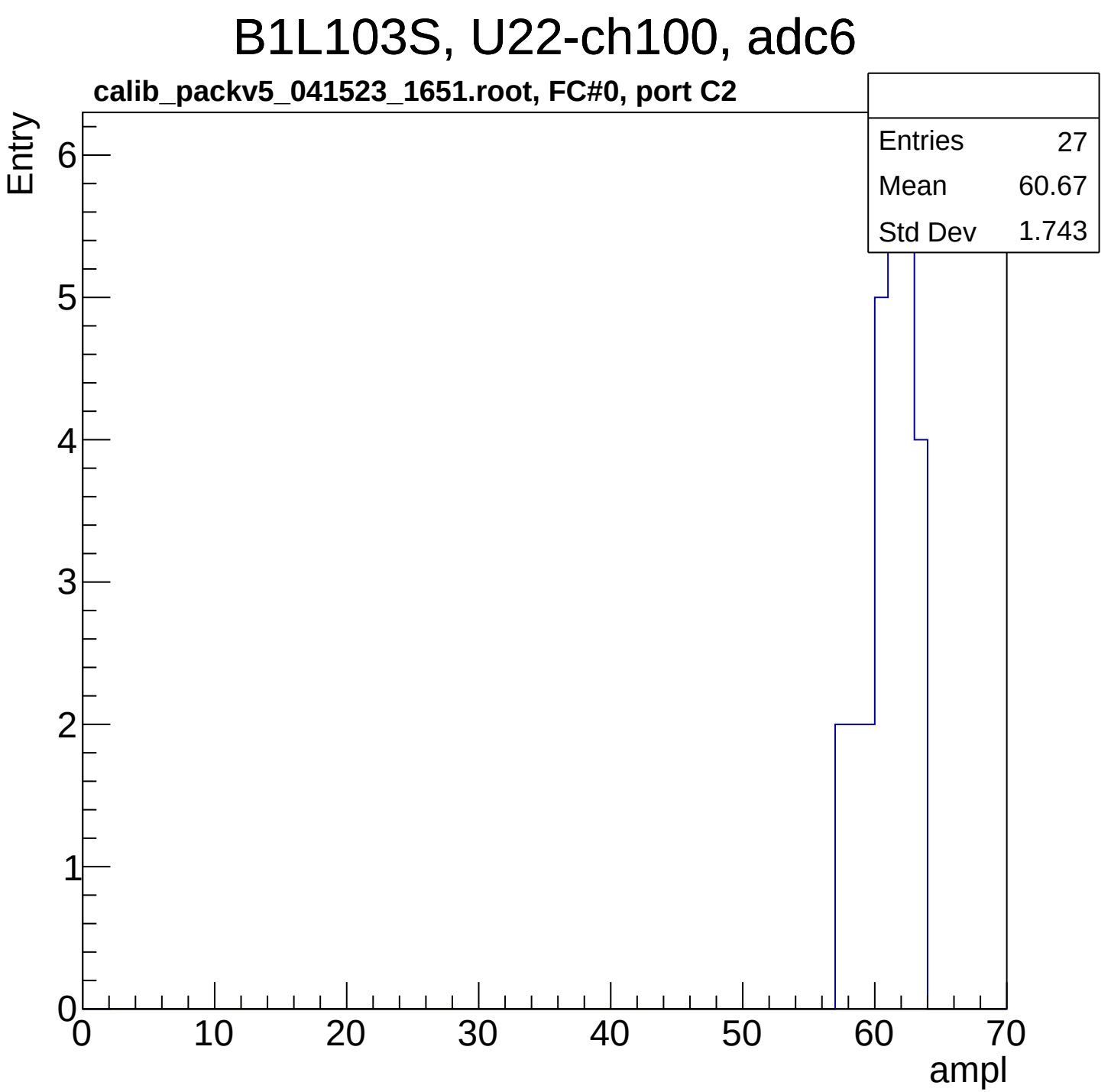
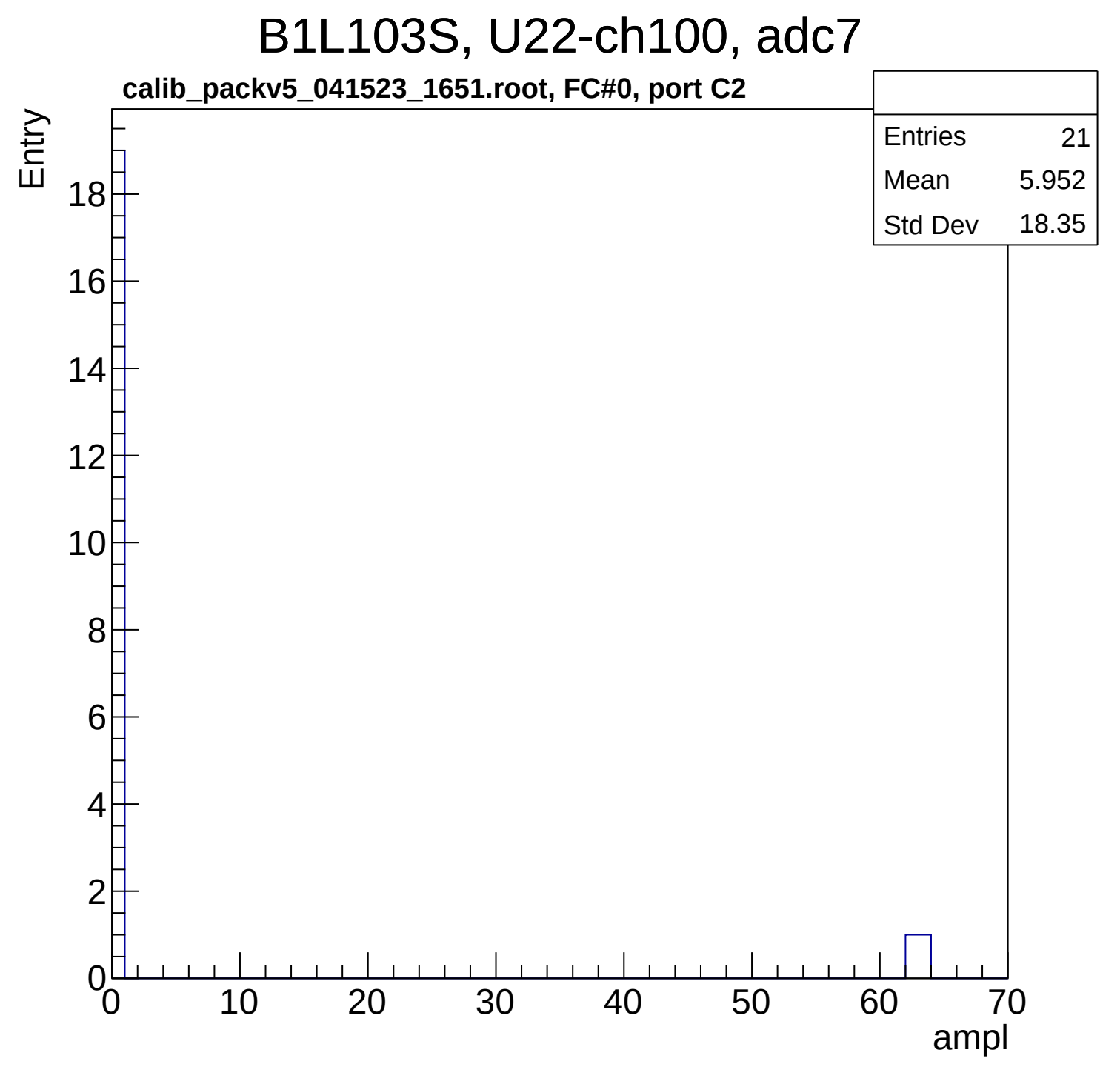

B1L103S, U22-ch100, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 60.67
Std Dev 1.743
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch100, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.952
Std Dev 18.35
Entry
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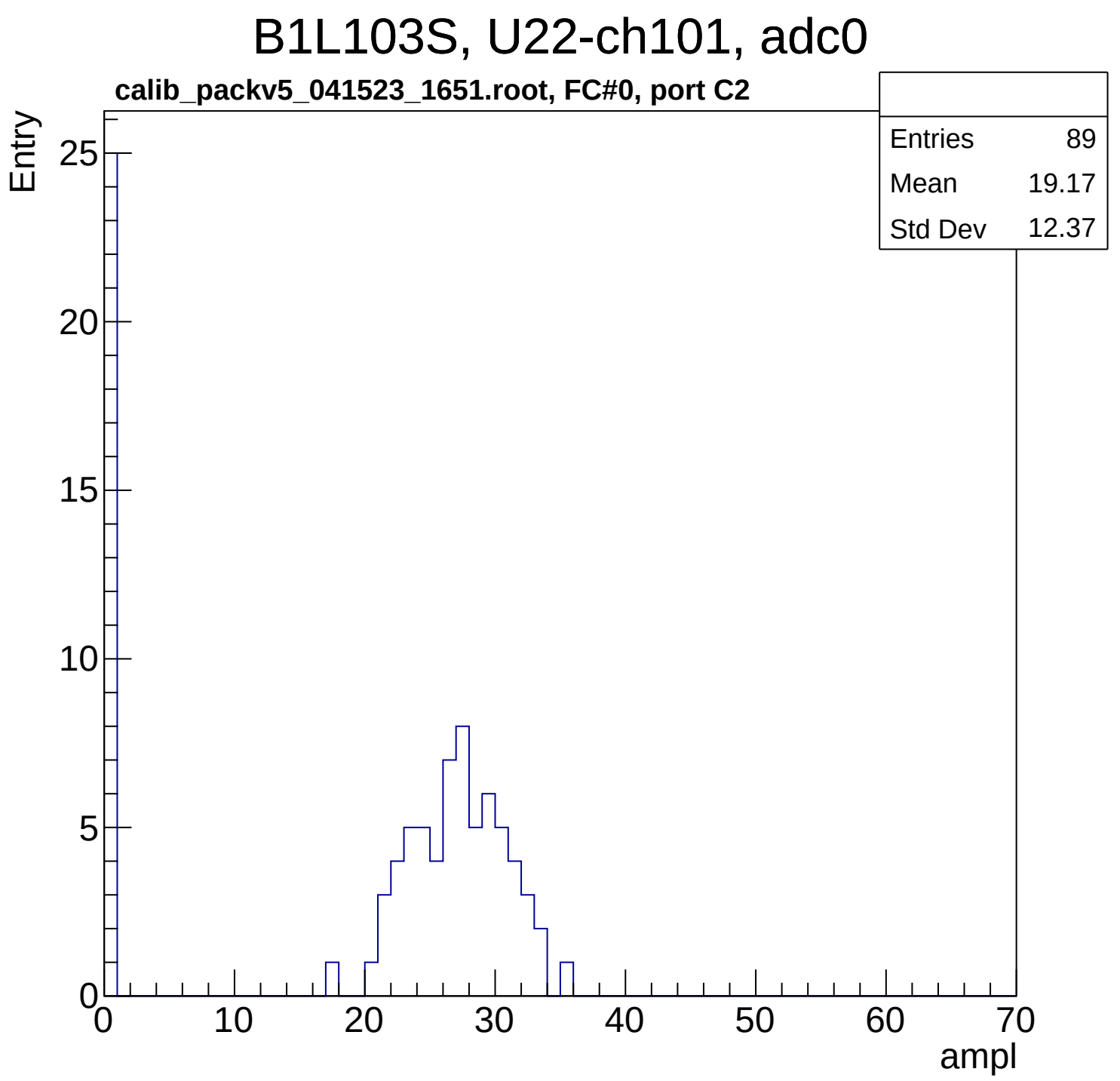
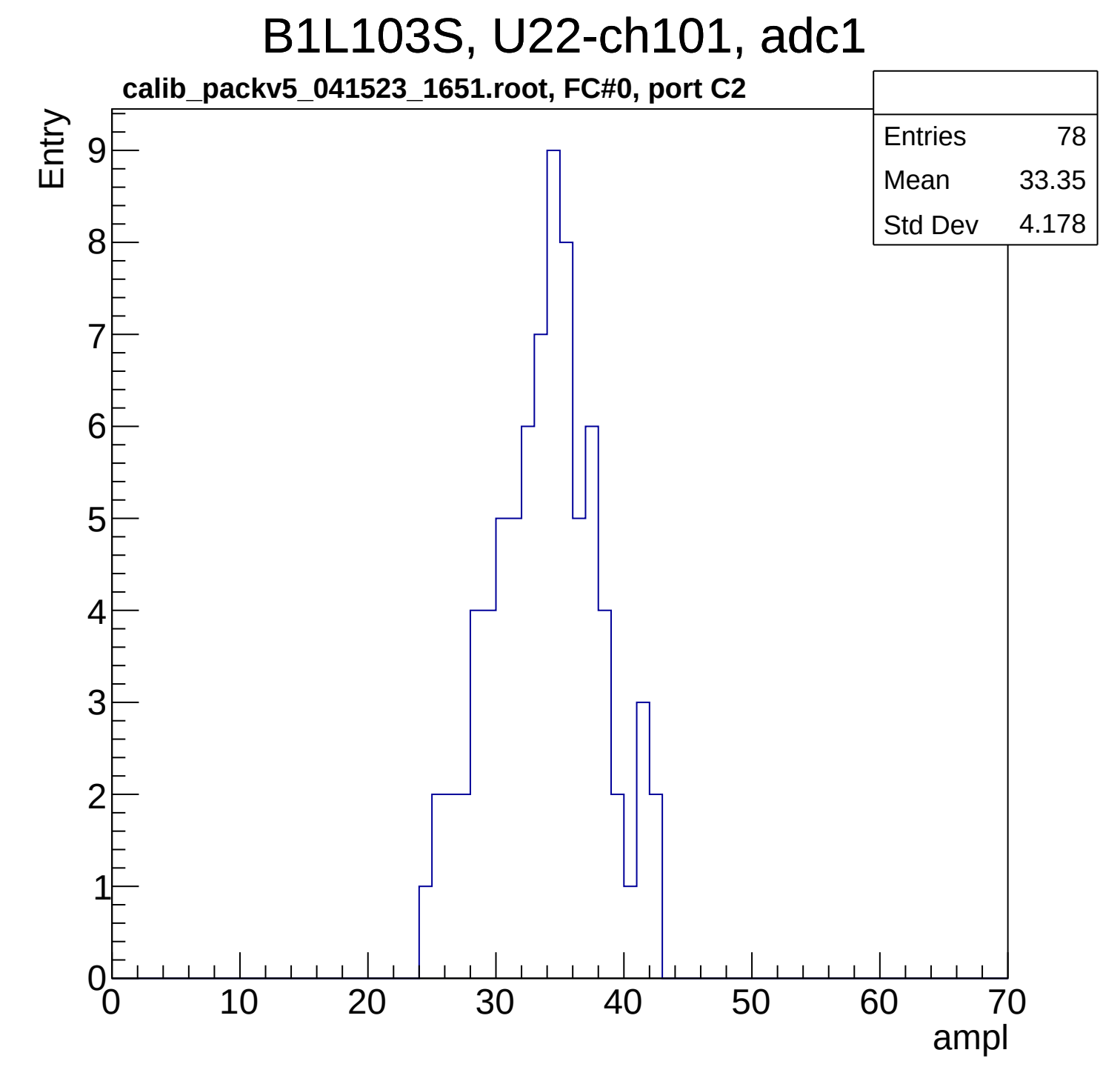
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch101, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 19.17
Std Dev 12.37
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch101, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 33.35
Std Dev 4.178
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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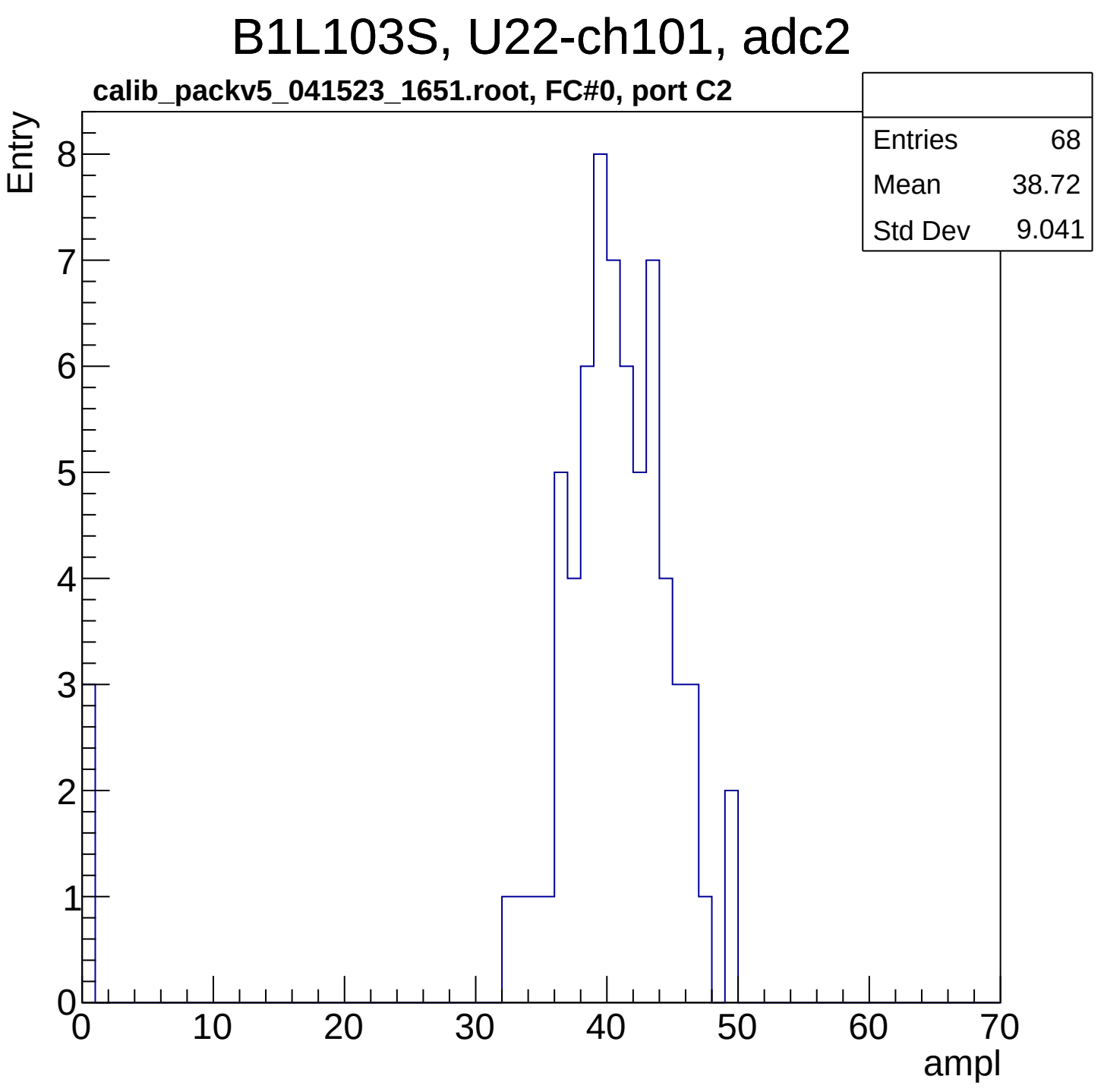
B1L103S, U22-ch101, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 38.72
Std Dev 9.041
Entry
ampl
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2
3
4
5
6
7
8
0
10
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30
40
50
60
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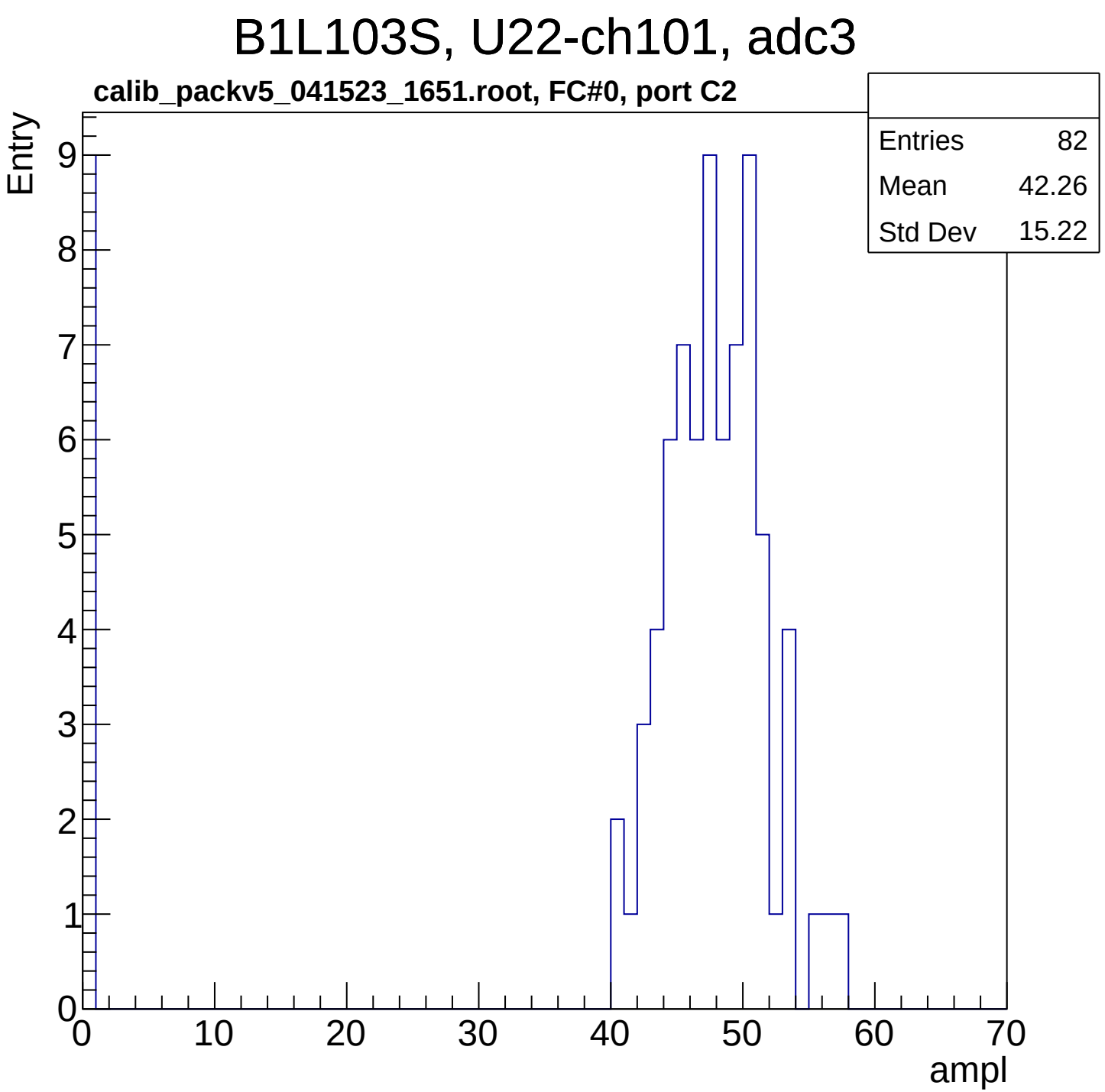
B1L103S, U22-ch101, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 42.26
Std Dev 15.22
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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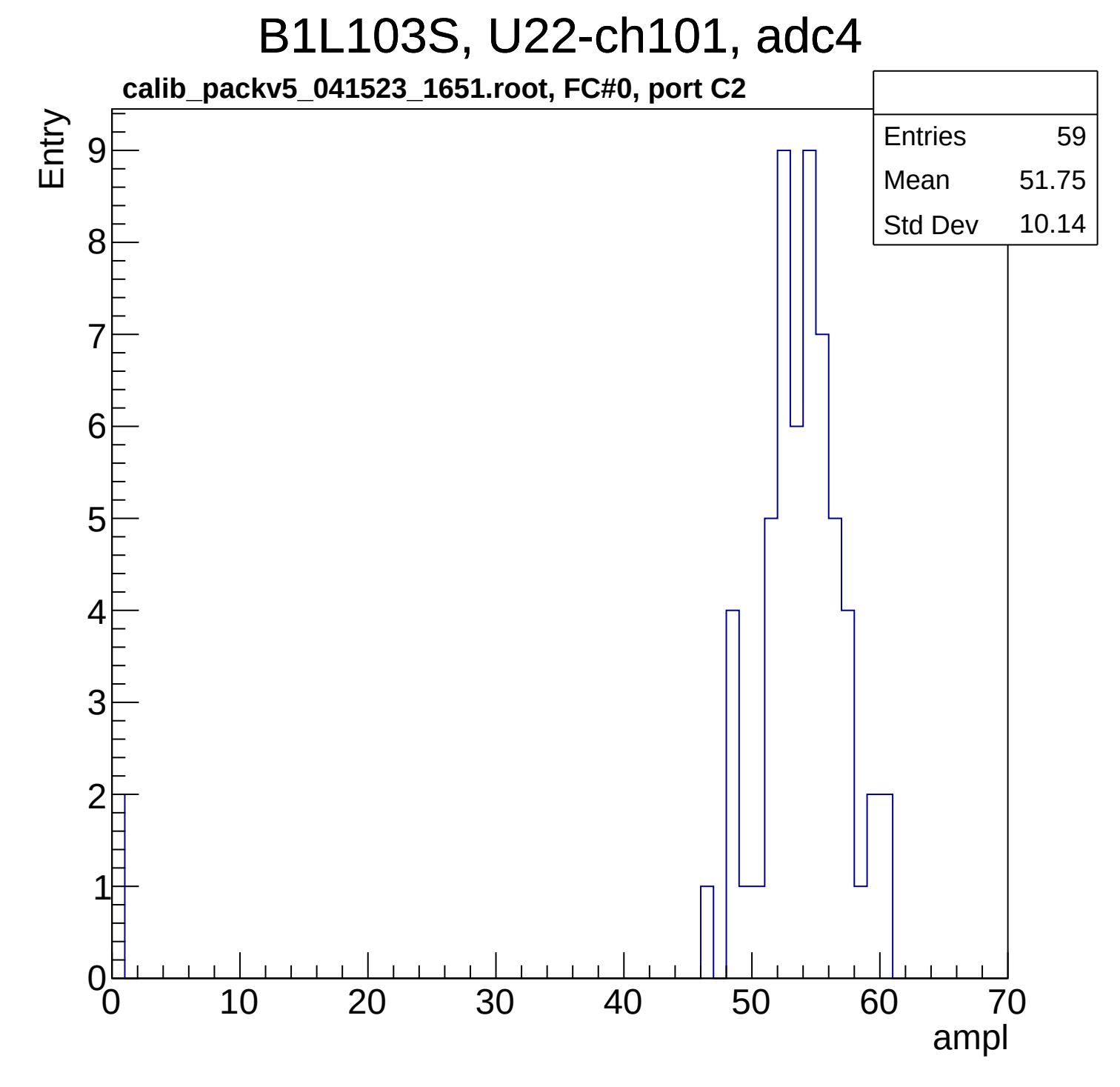
B1L103S, U22-ch101, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 51.75
Std Dev 10.14
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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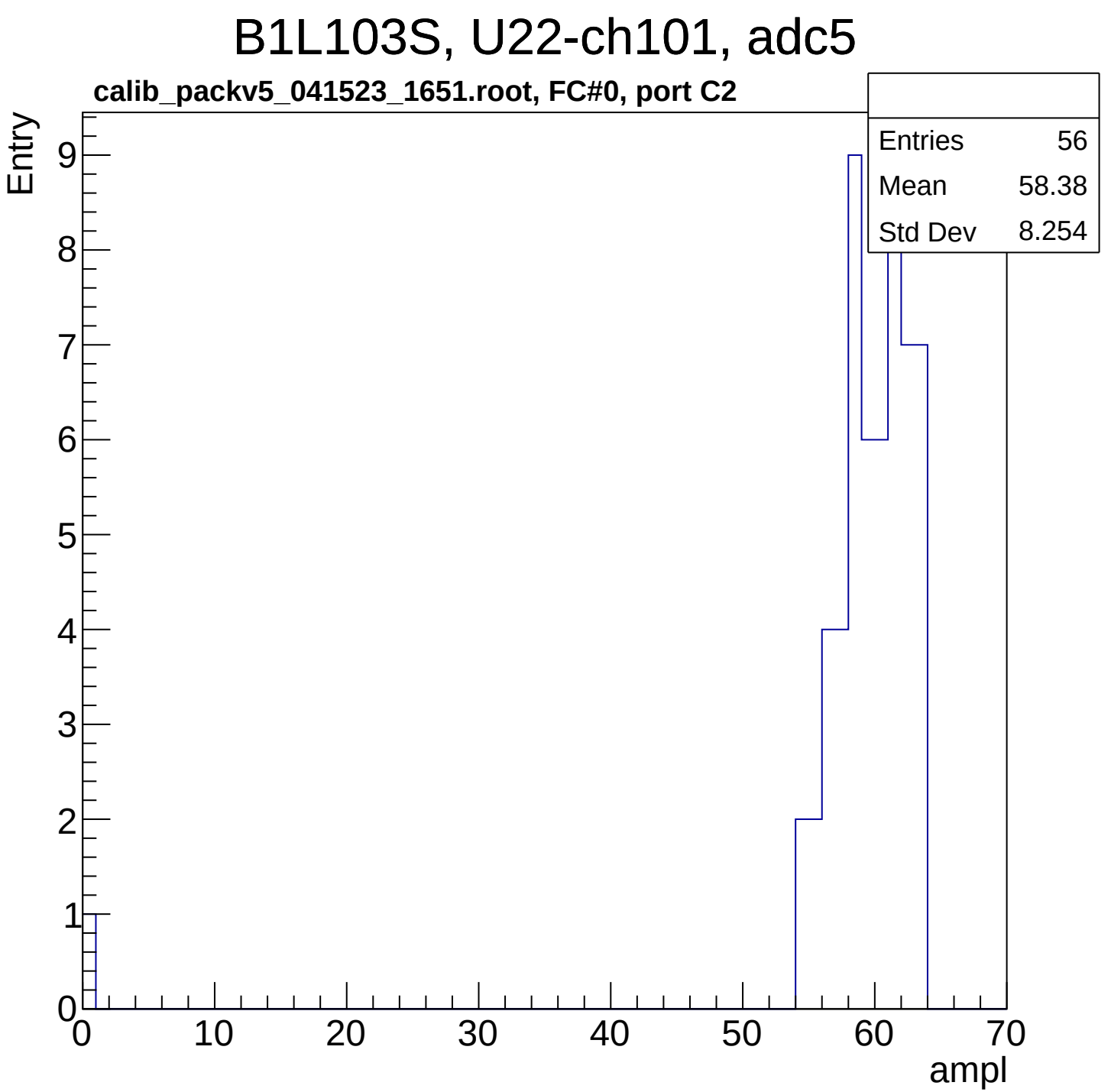
B1L103S, U22-ch101, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 58.38
Std Dev 8.254
Entry
ampl
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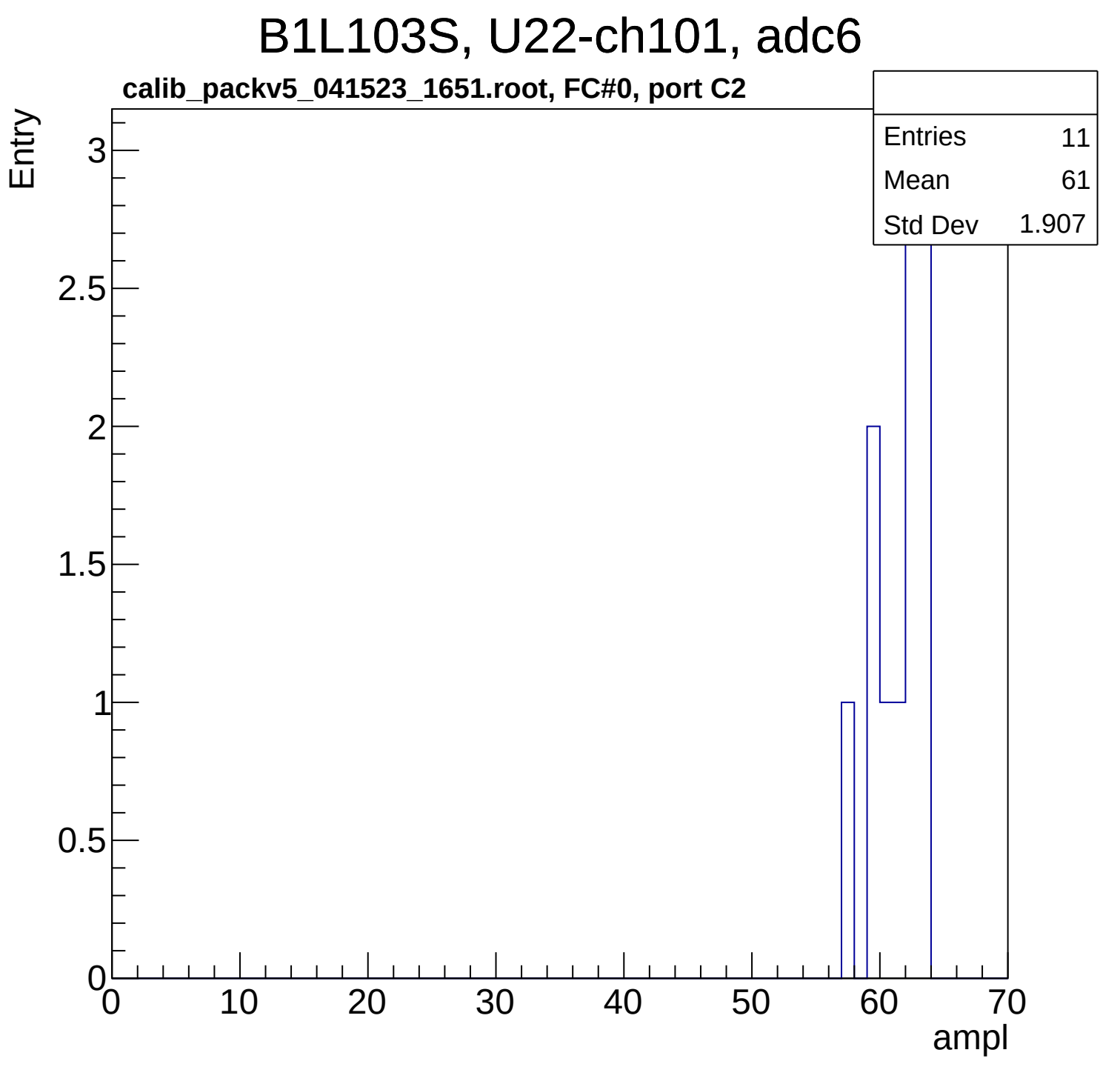
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch101, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 61
Std Dev 1.907
Entry
ampl
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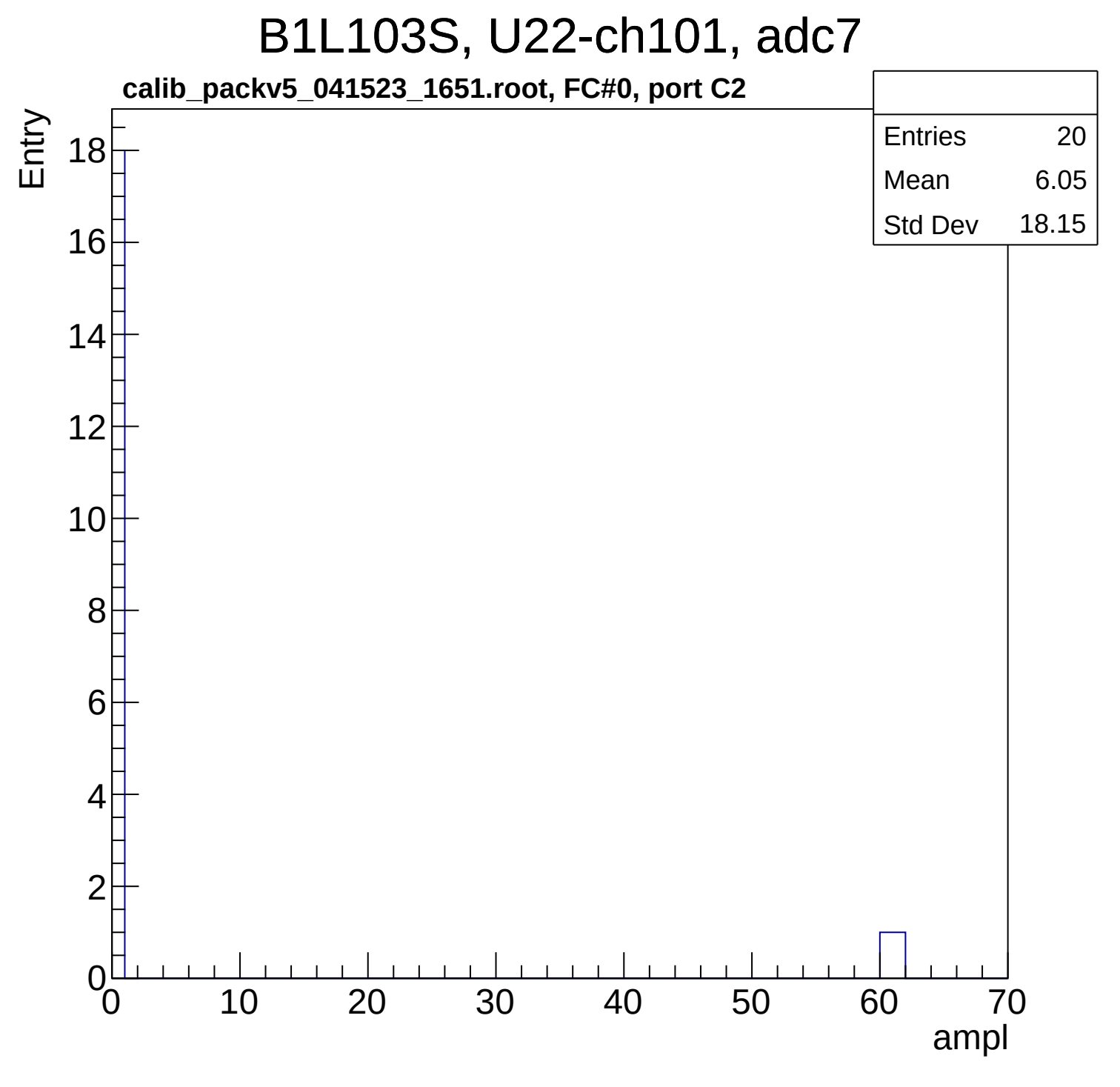
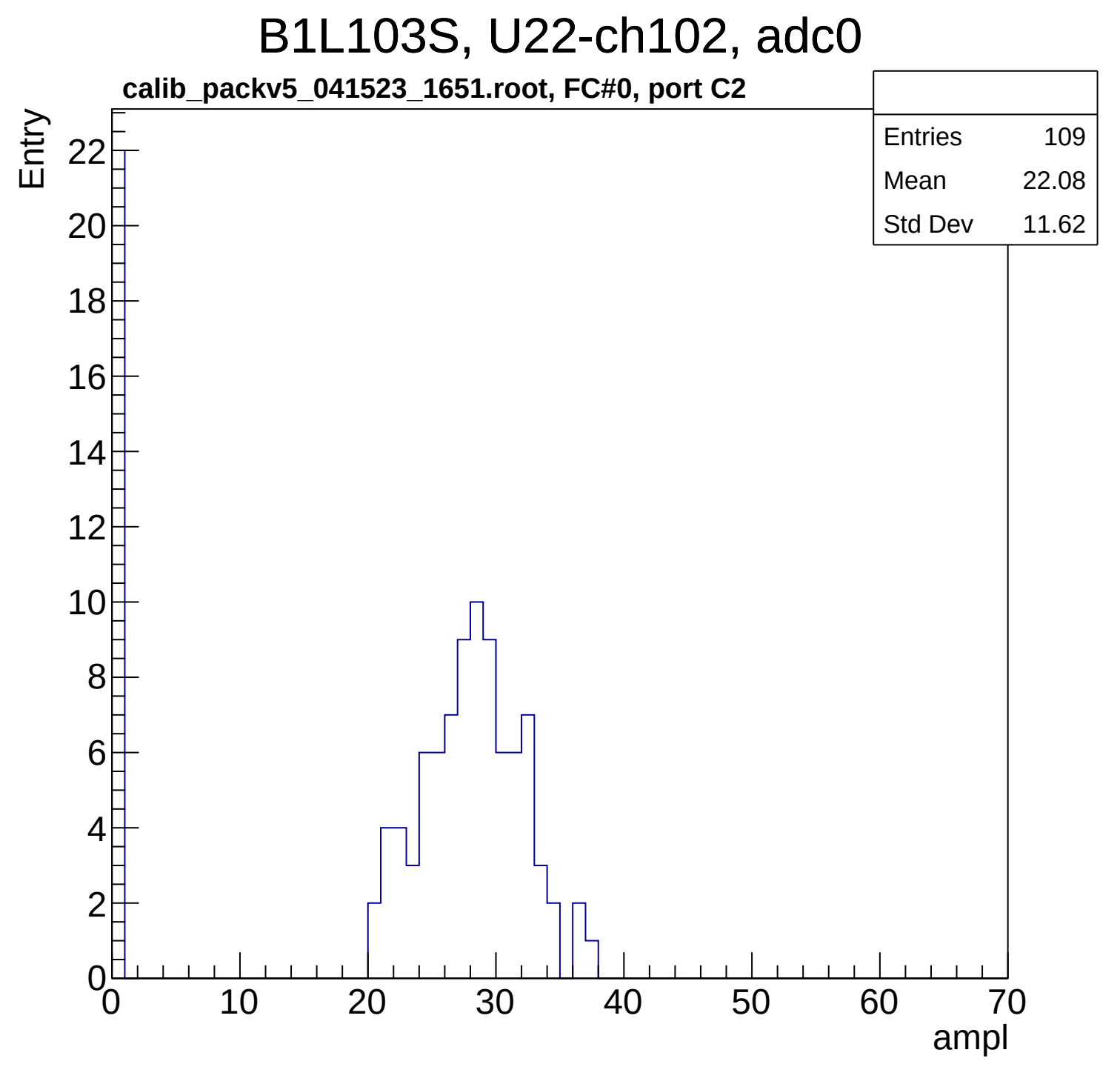
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U22-ch101, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 6.05
Std Dev 18.15
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch102, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 109
Mean 22.08
Std Dev 11.62
Entry
ampl
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2
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6
8
10
12
14
16
18
20
22
0
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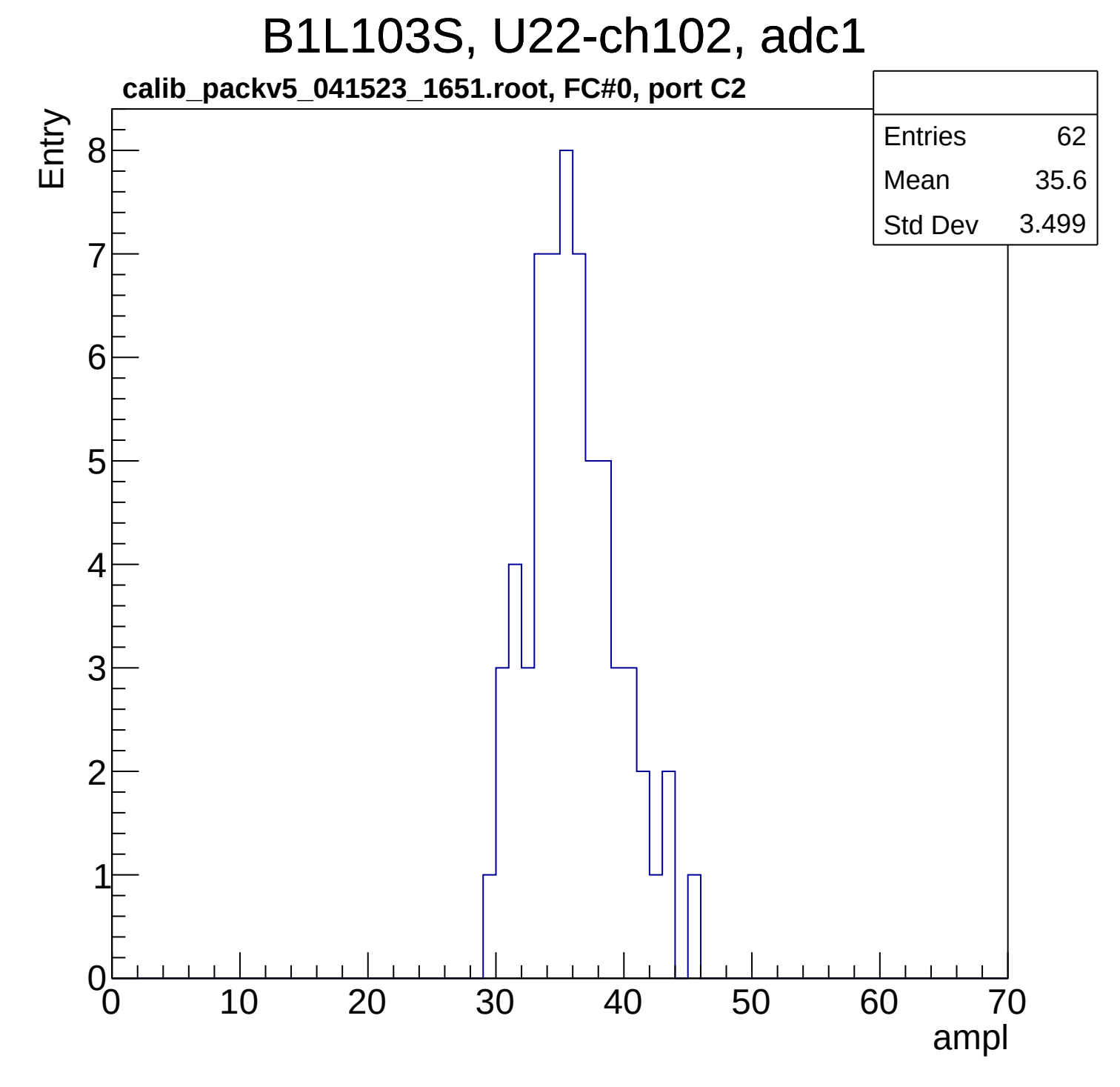
20
30
40
50
60
70


B1L103S, U22-ch102, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 35.6
Std Dev 3.499
Entry
ampl
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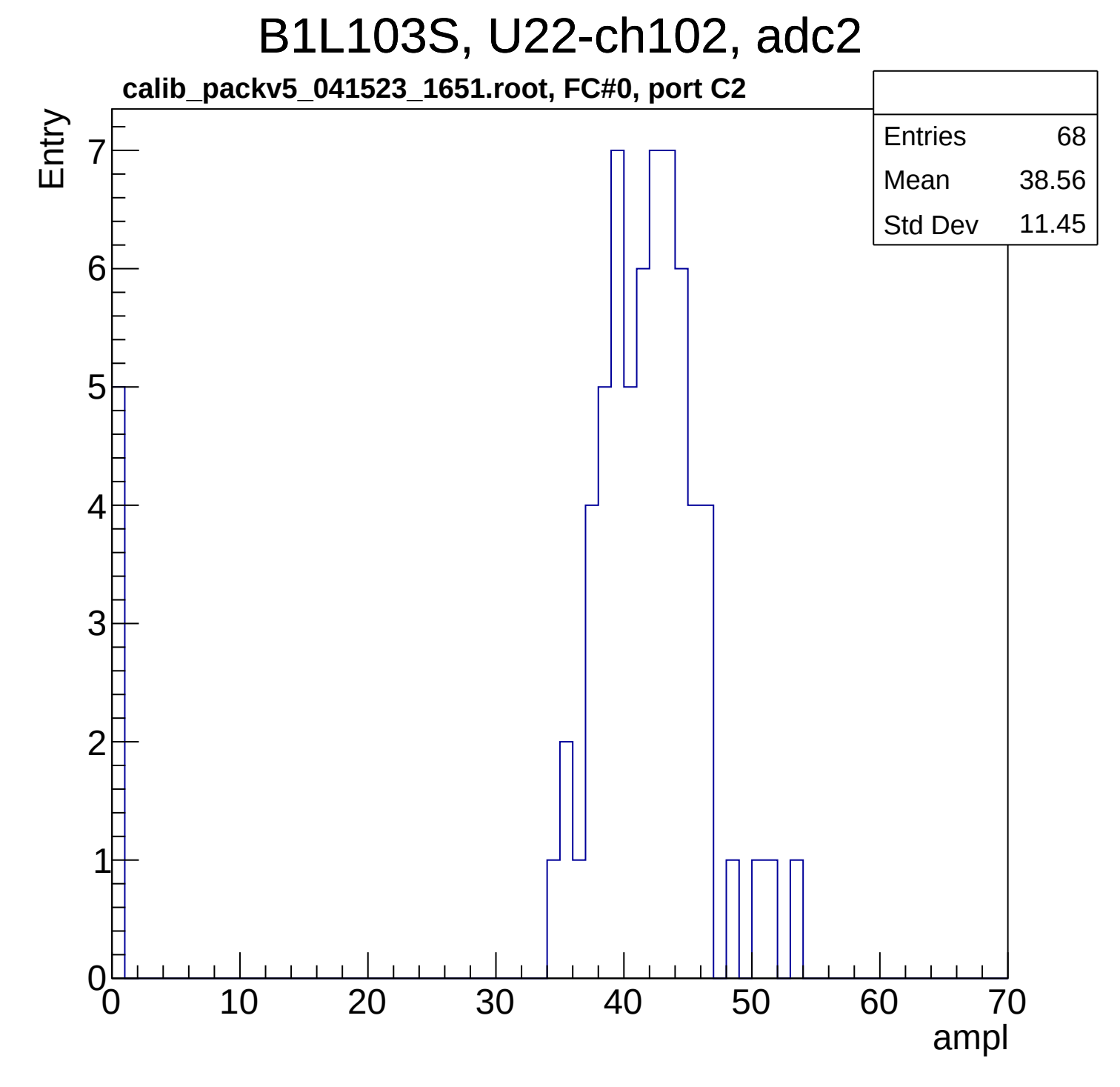
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch102, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 38.56
Std Dev 11.45
Entry
ampl
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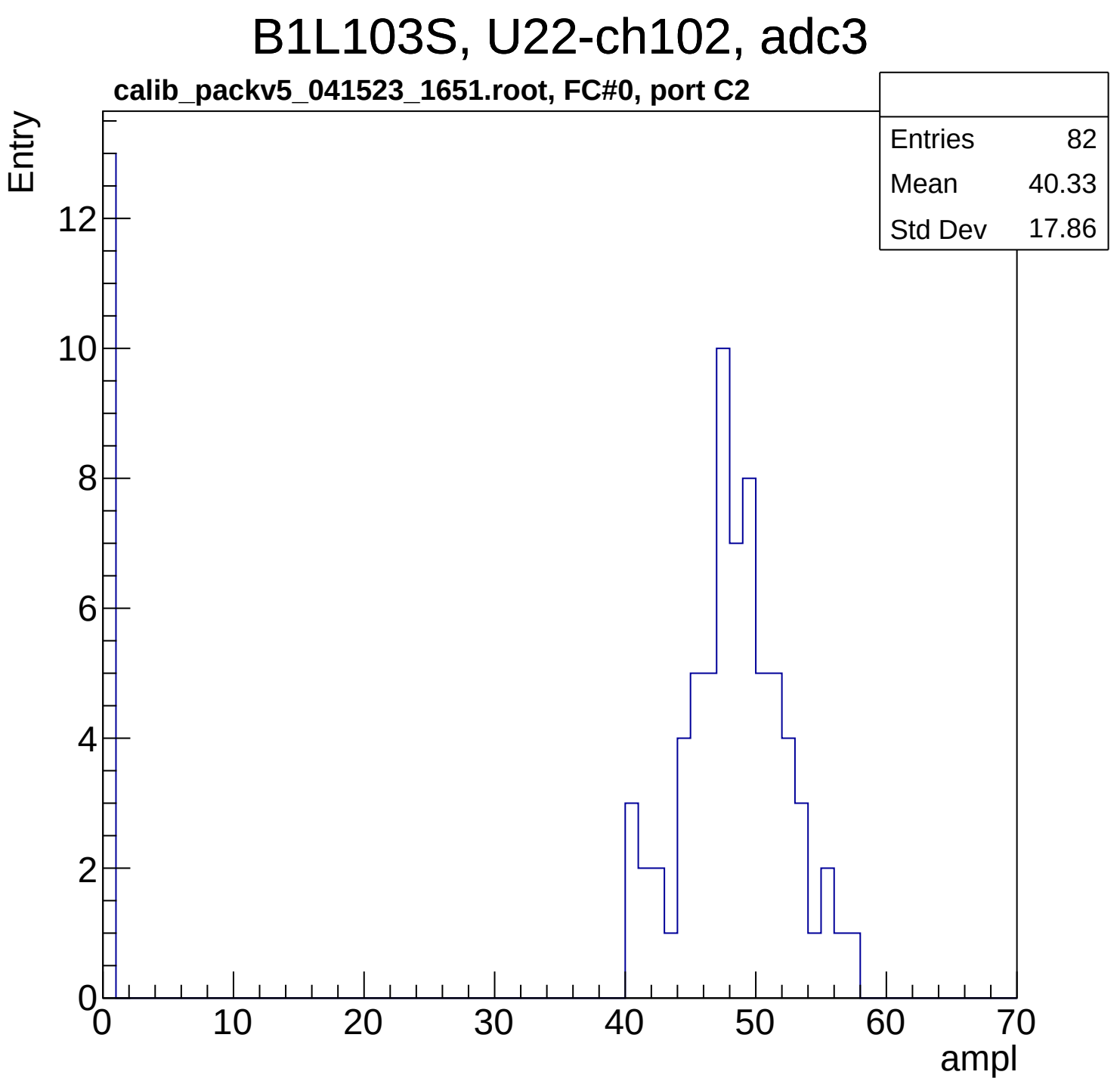
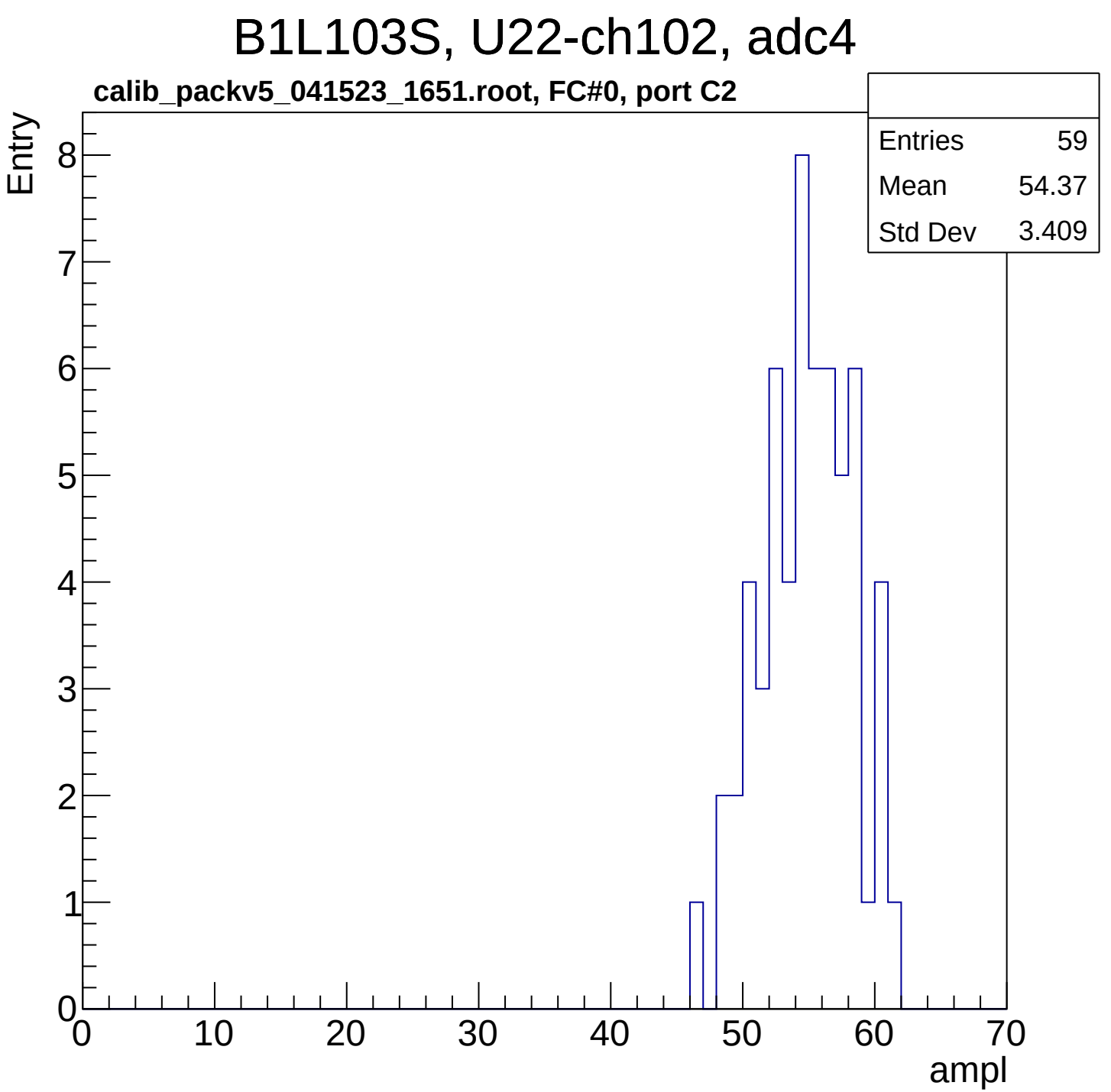
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U22-ch102, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 40.33
Std Dev 17.86
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U22-ch102, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 54.37
Std Dev 3.409
Entry
ampl
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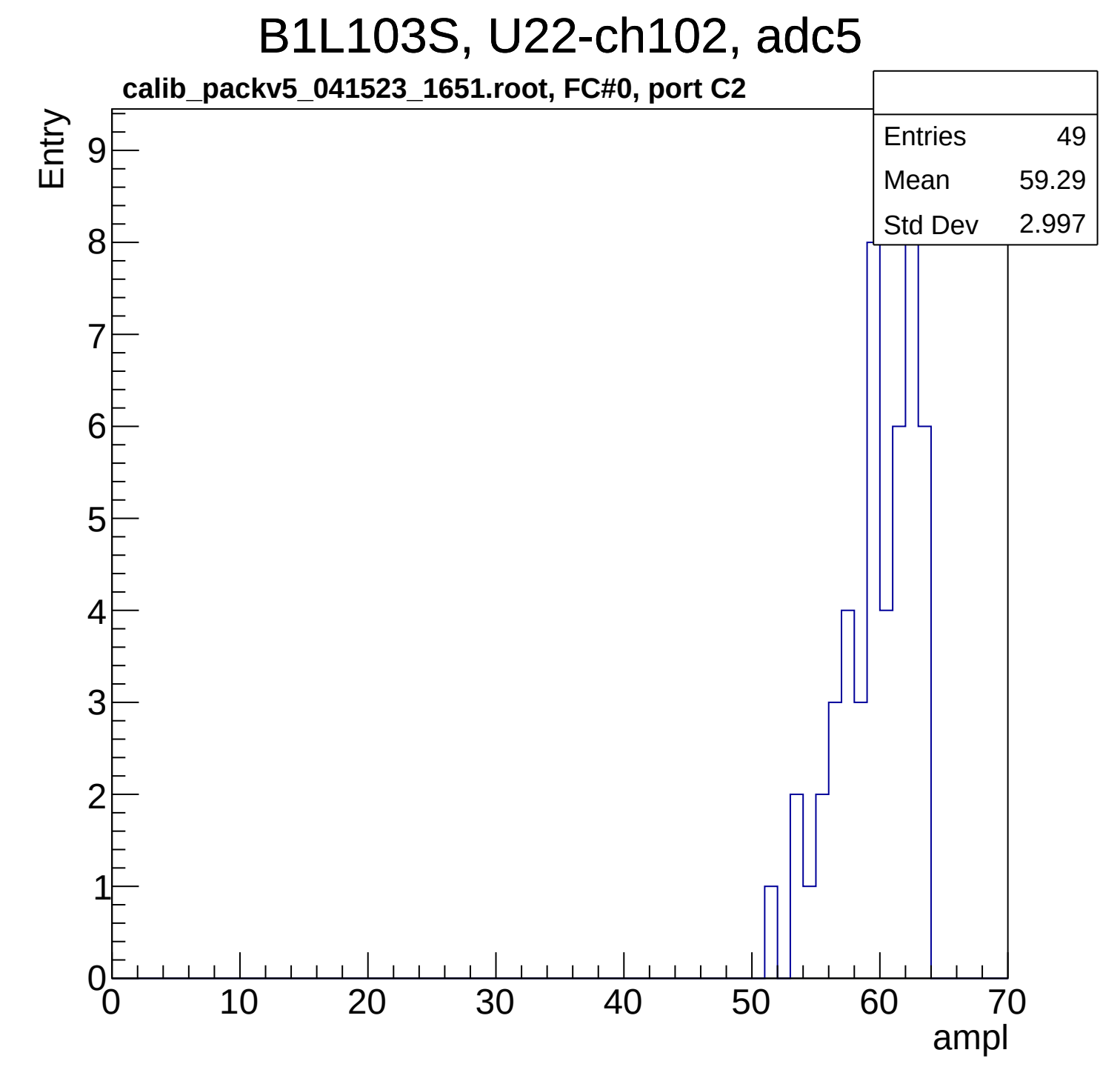
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch102, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 59.29
Std Dev 2.997
Entry
ampl
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2
3
4
5
6
7
8
9
0
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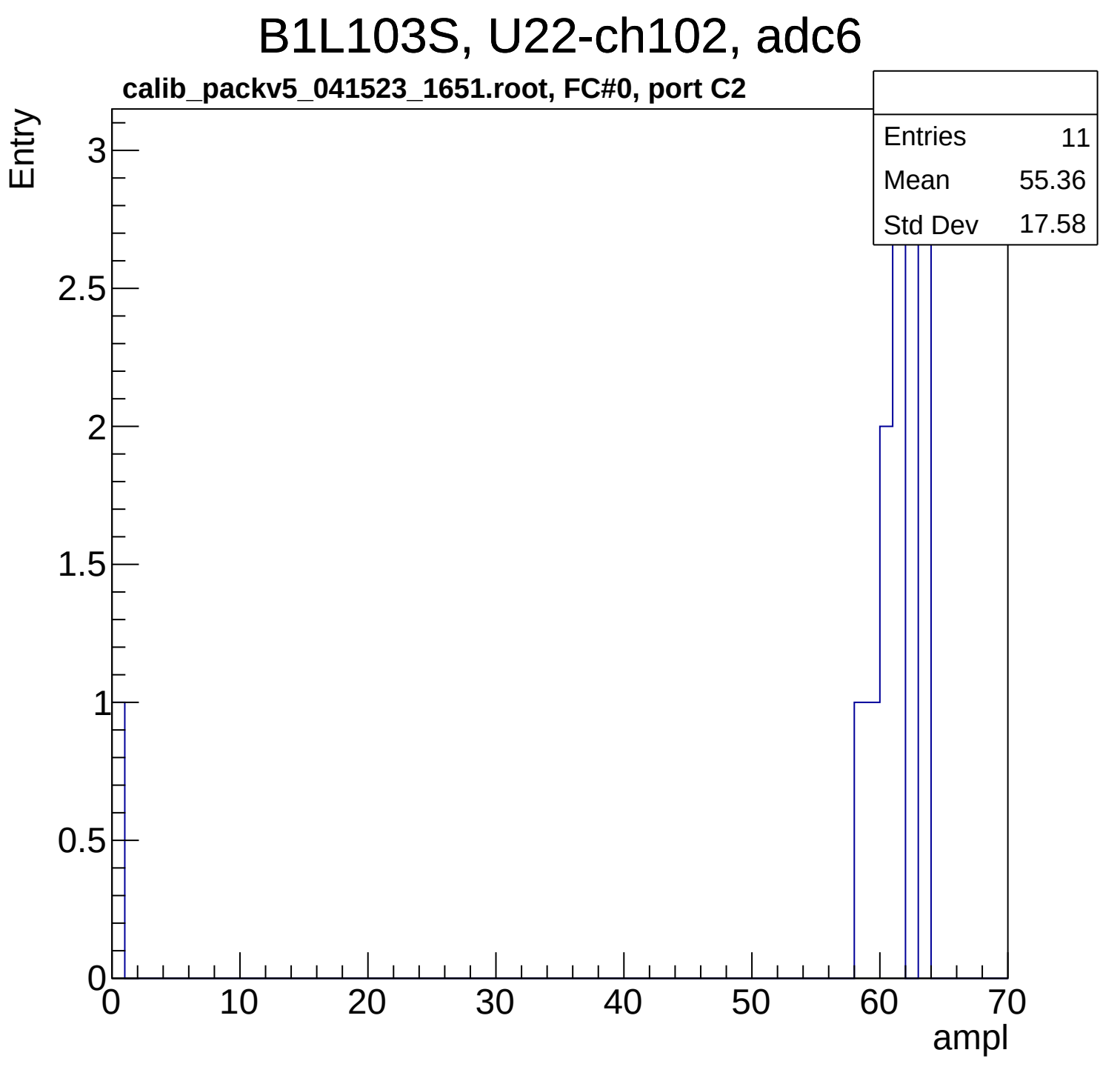
20
30
40
50
60
70


B1L103S, U22-ch102, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 55.36
Std Dev 17.58
Entry
ampl
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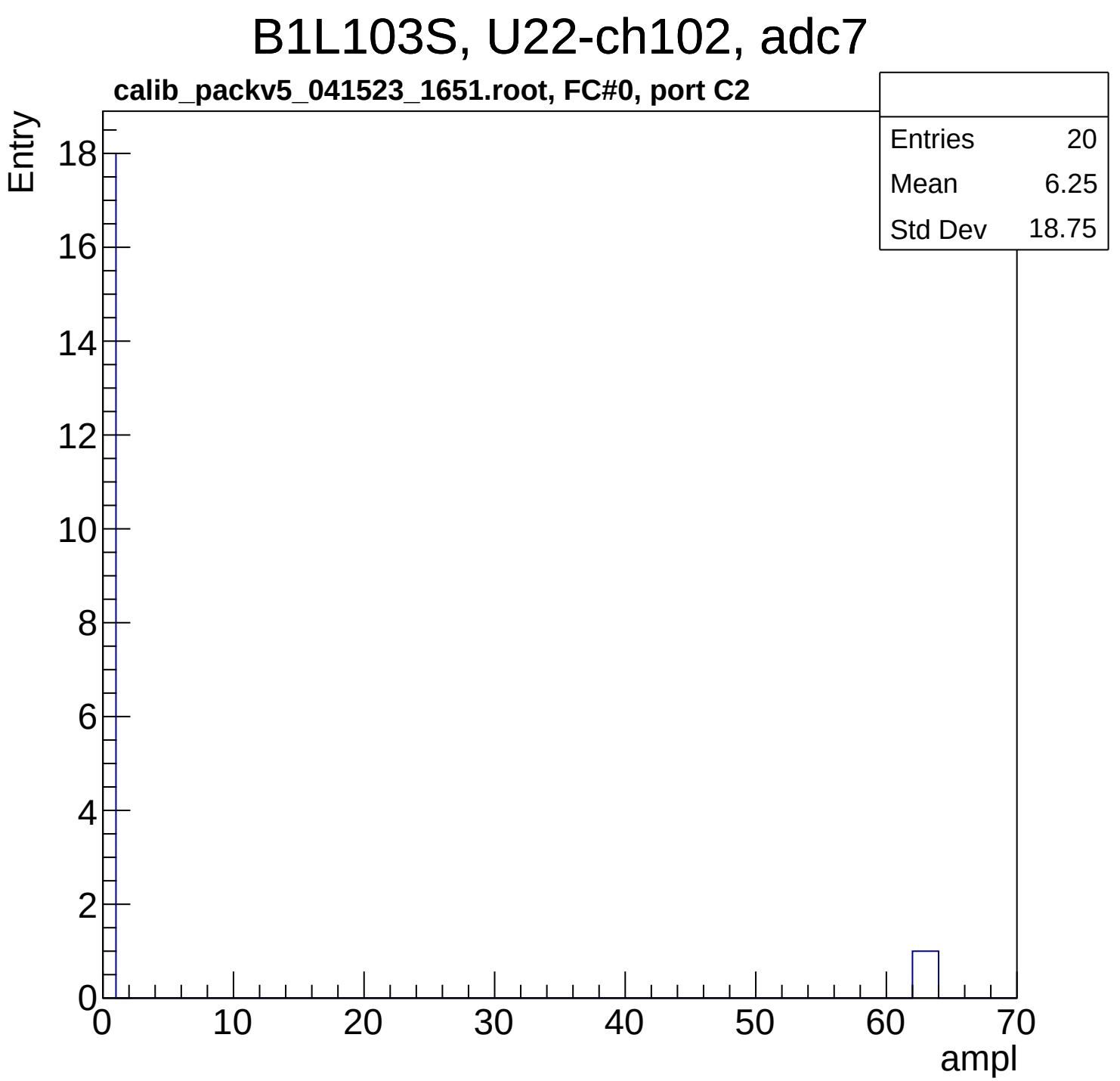
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U22-ch102, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 6.25
Std Dev 18.75
Entry
0
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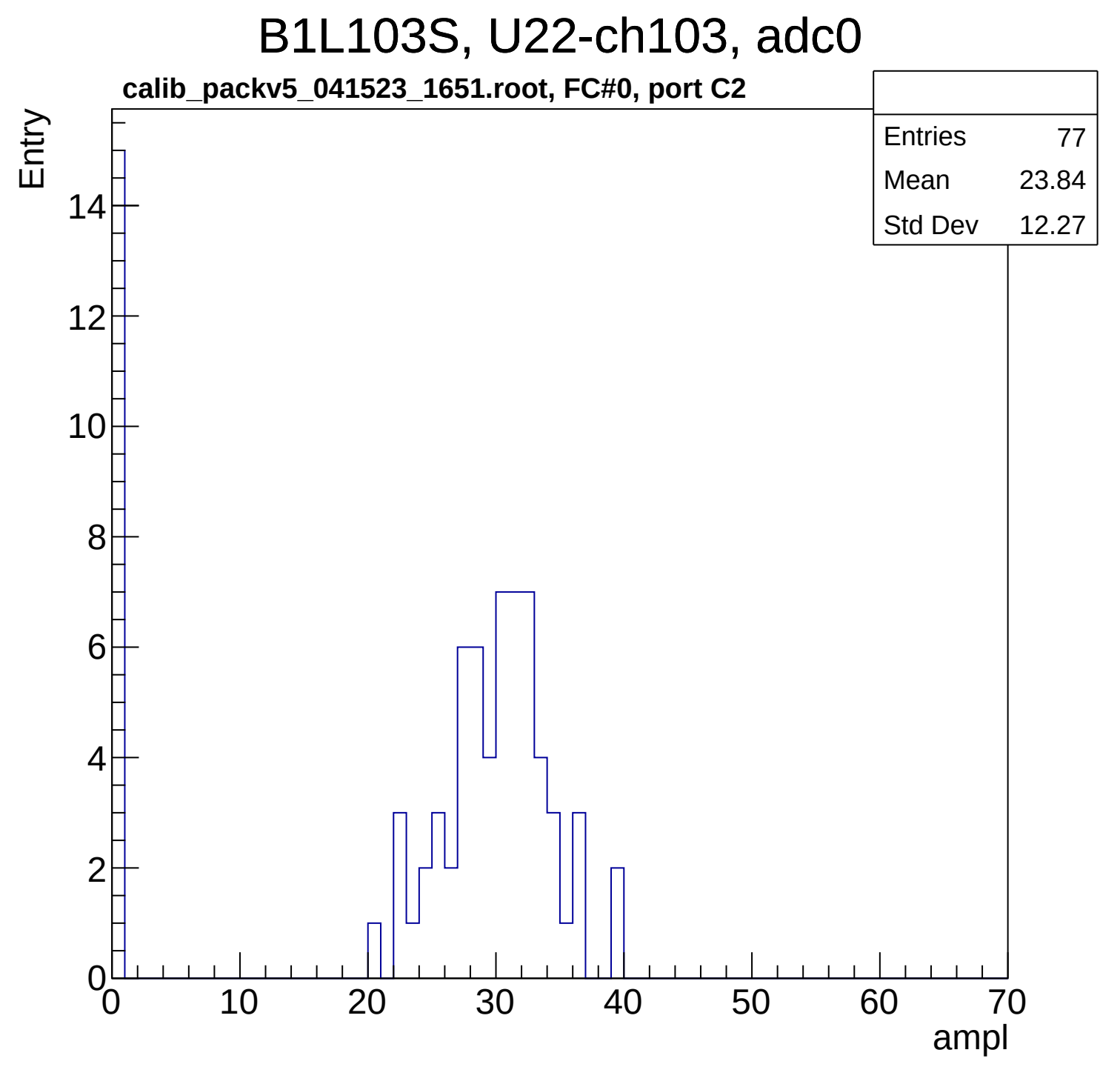
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch103, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 23.84
Std Dev 12.27
Entry
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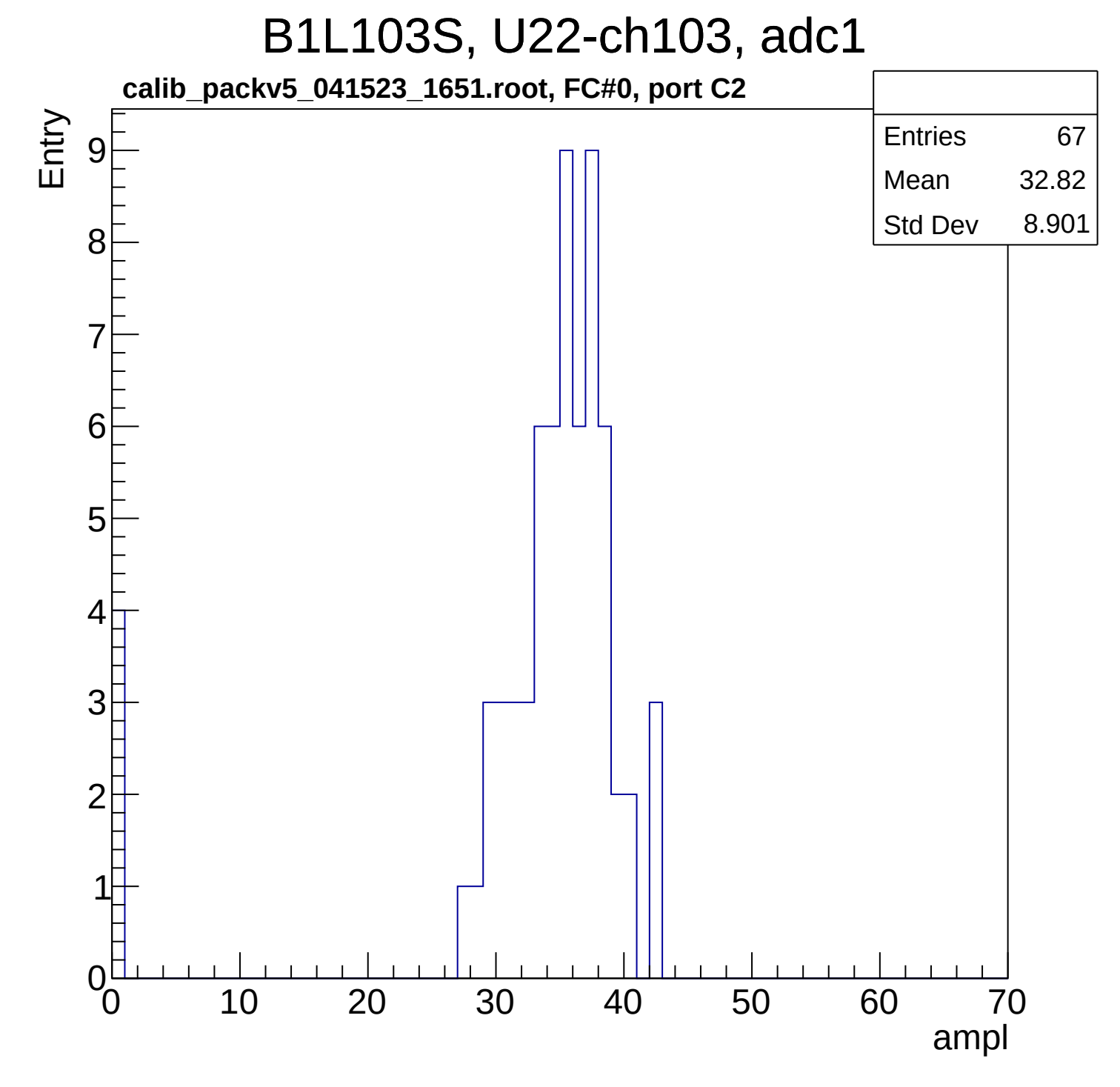
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch103, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 32.82
Std Dev 8.901
Entry
ampl
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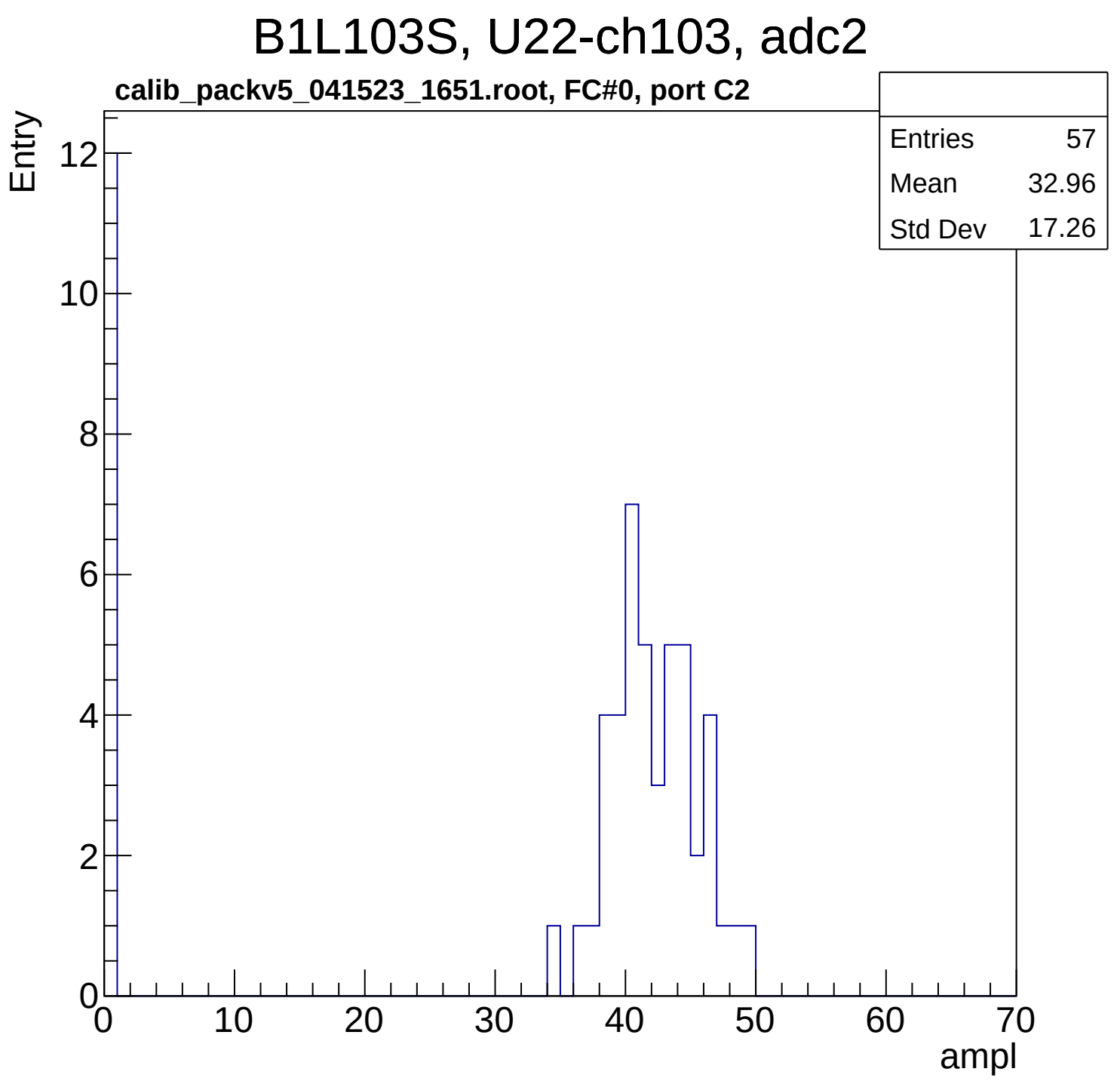
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch103, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 32.96
Std Dev 17.26
Entry
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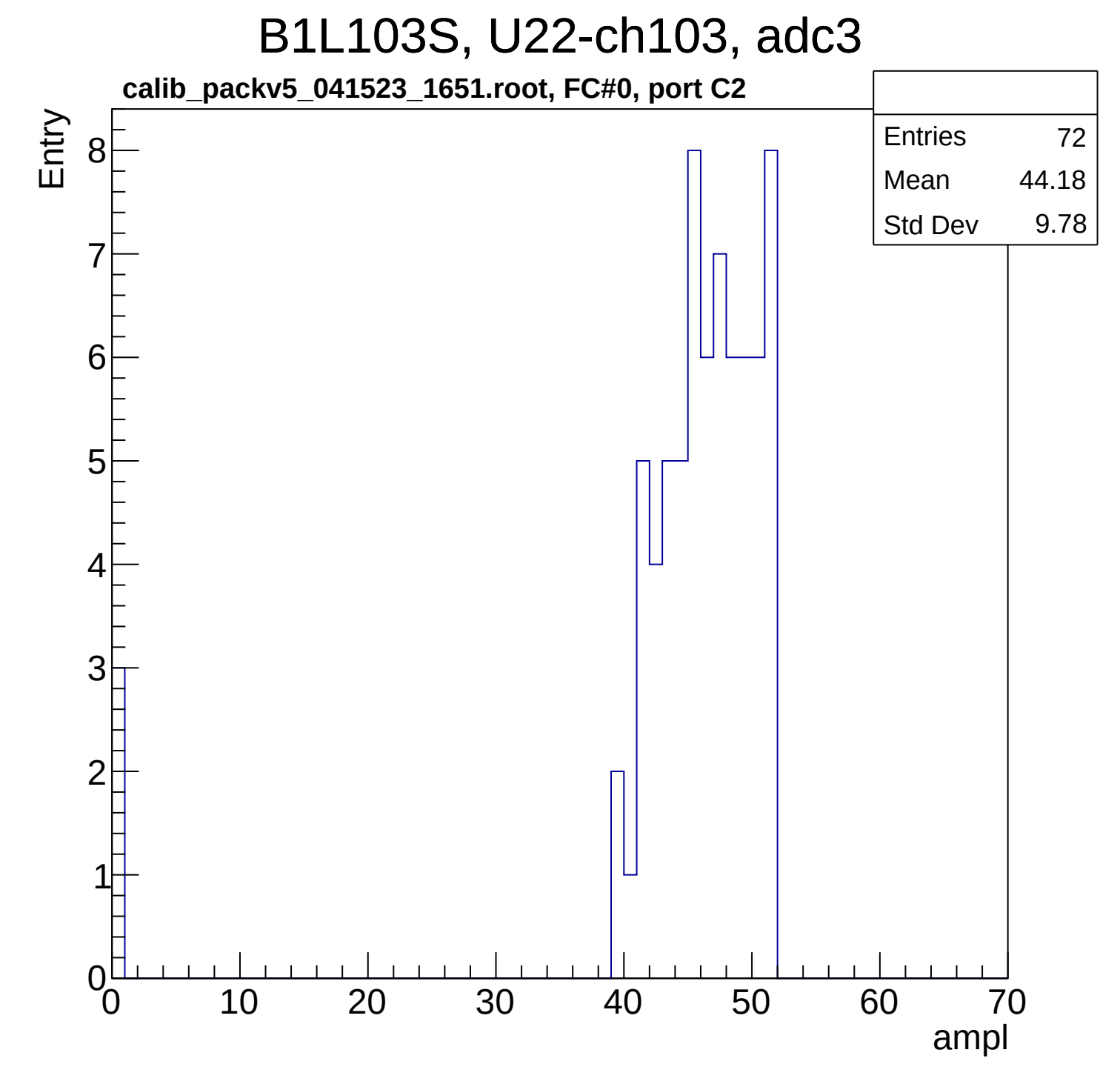
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch103, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 44.18
Std Dev 9.78
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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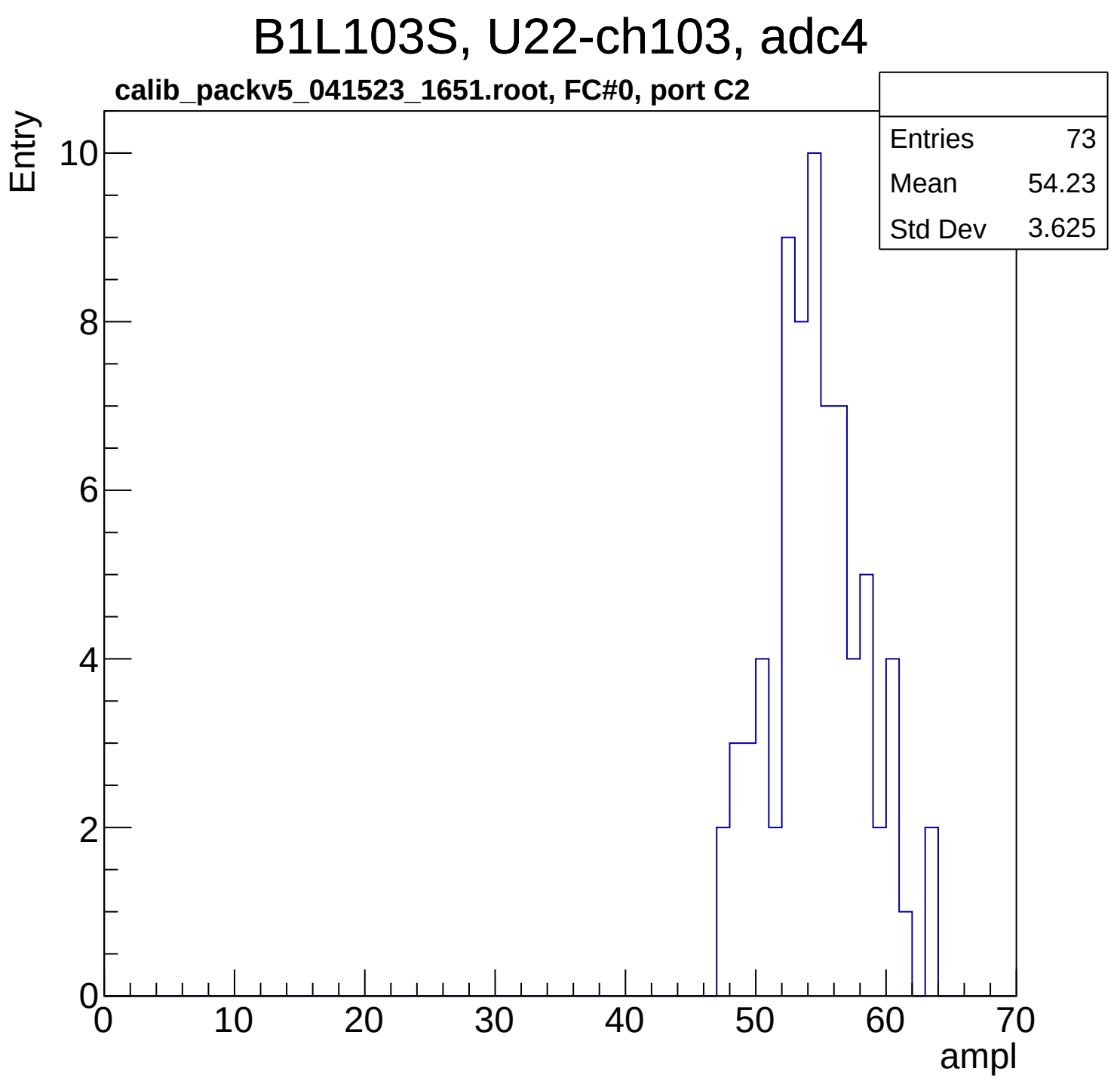
B1L103S, U22-ch103, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 54.23
Std Dev 3.625
Entry
ampl
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4
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40
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60
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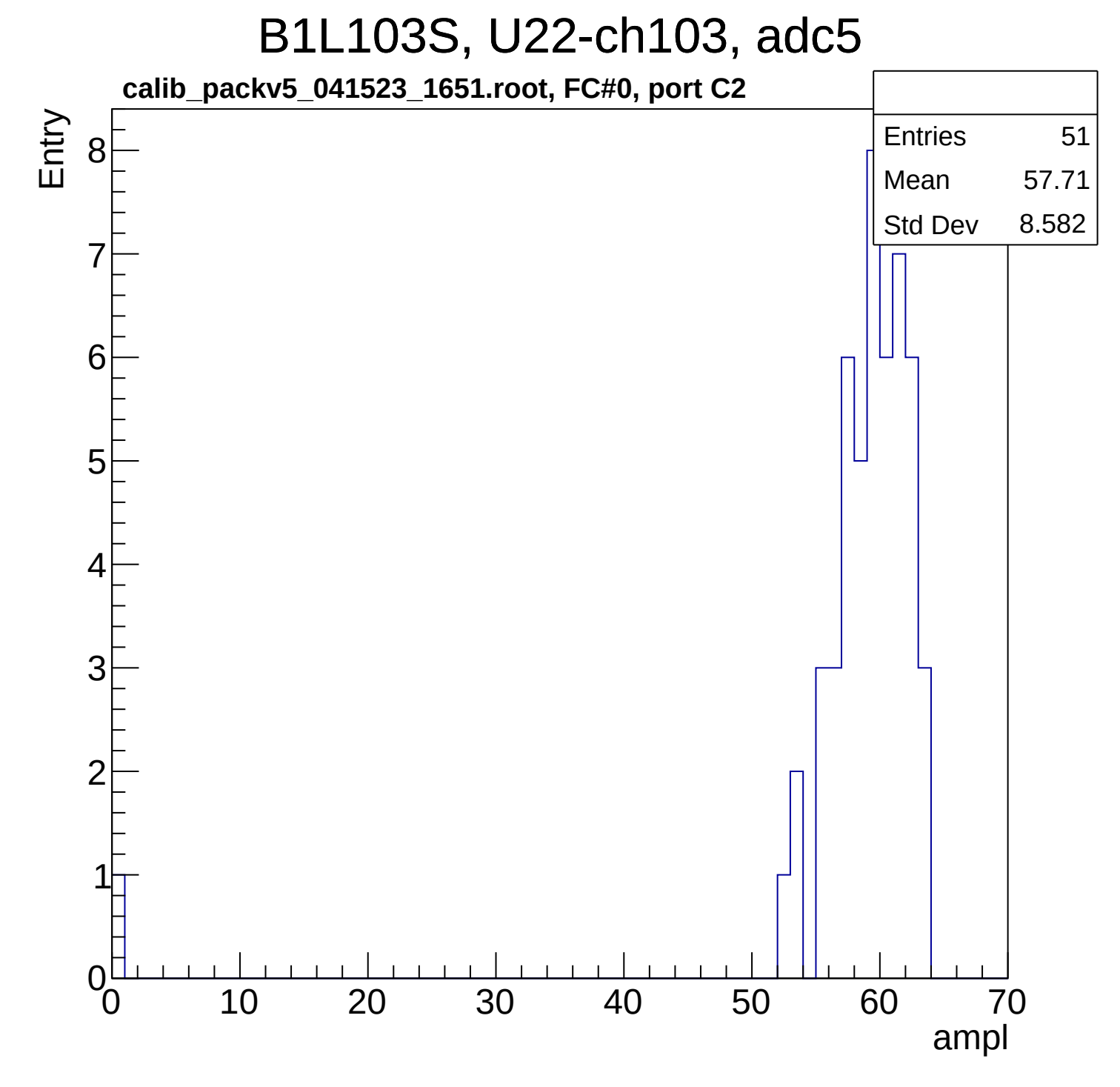
B1L103S, U22-ch103, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 57.71
Std Dev 8.582
Entry
ampl
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5
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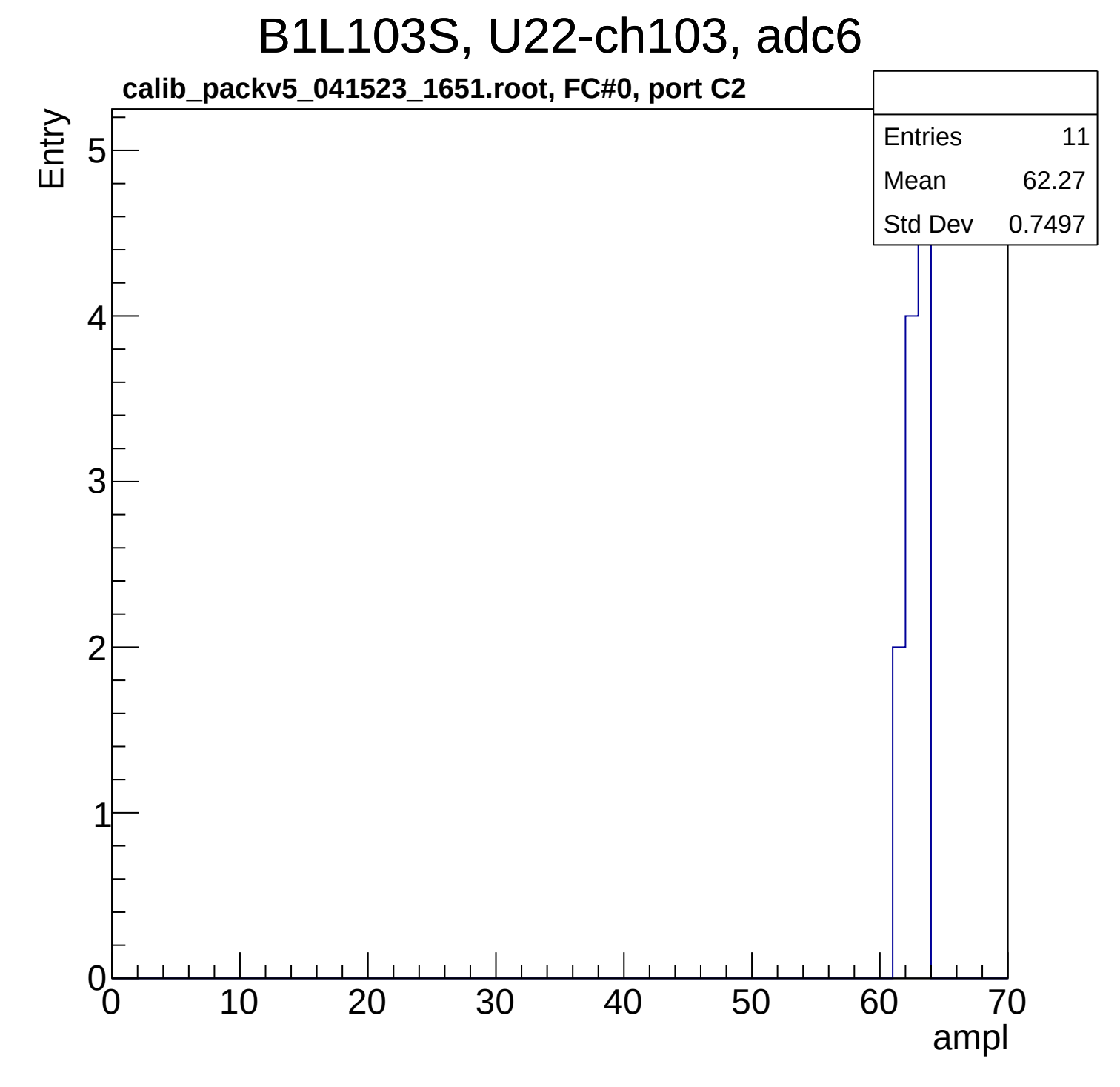
B1L103S, U22-ch103, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 62.27
Std Dev 0.7497
Entry
ampl
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2
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4
5
0
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20
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40
50
60
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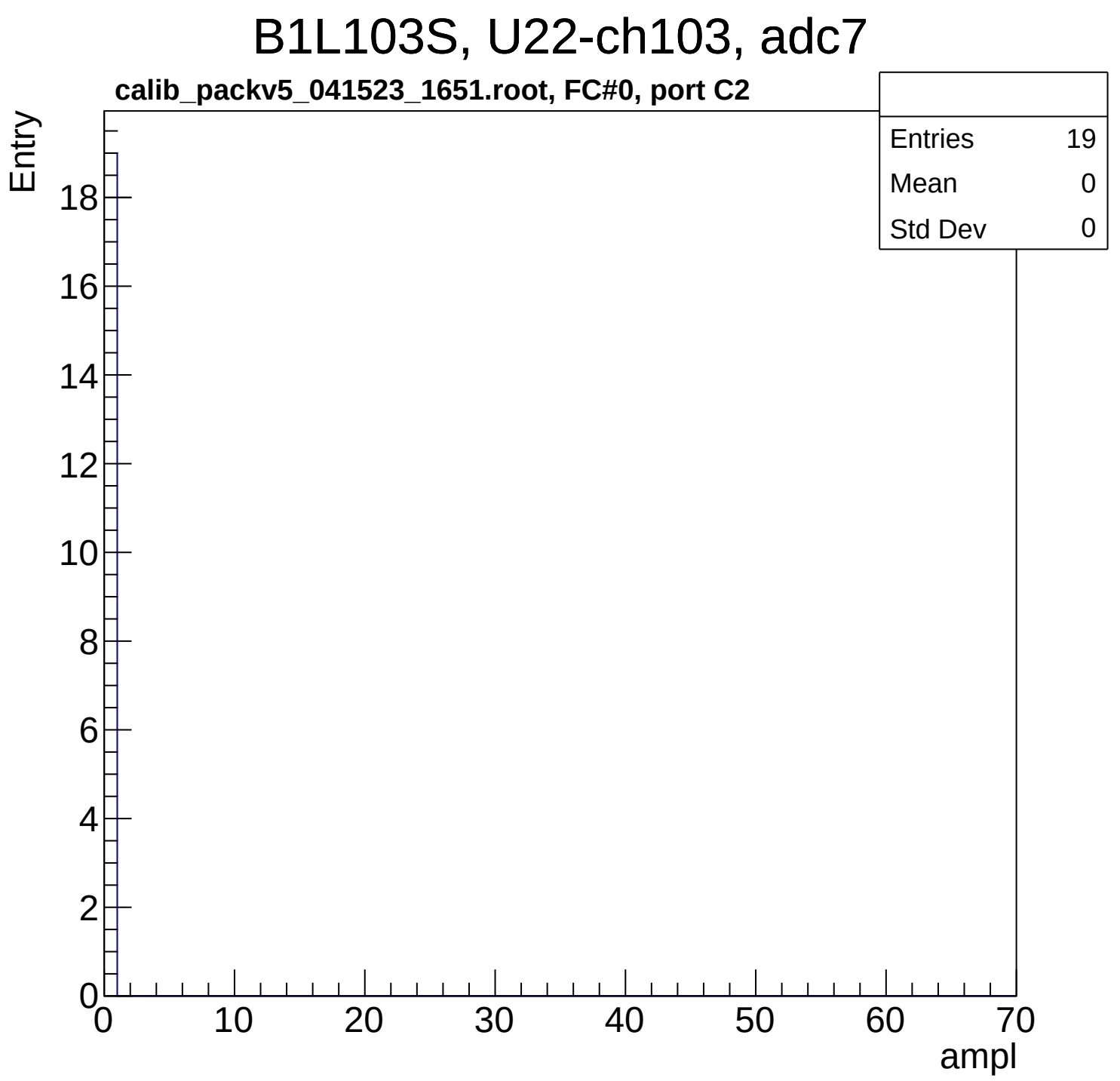
B1L103S, U22-ch103, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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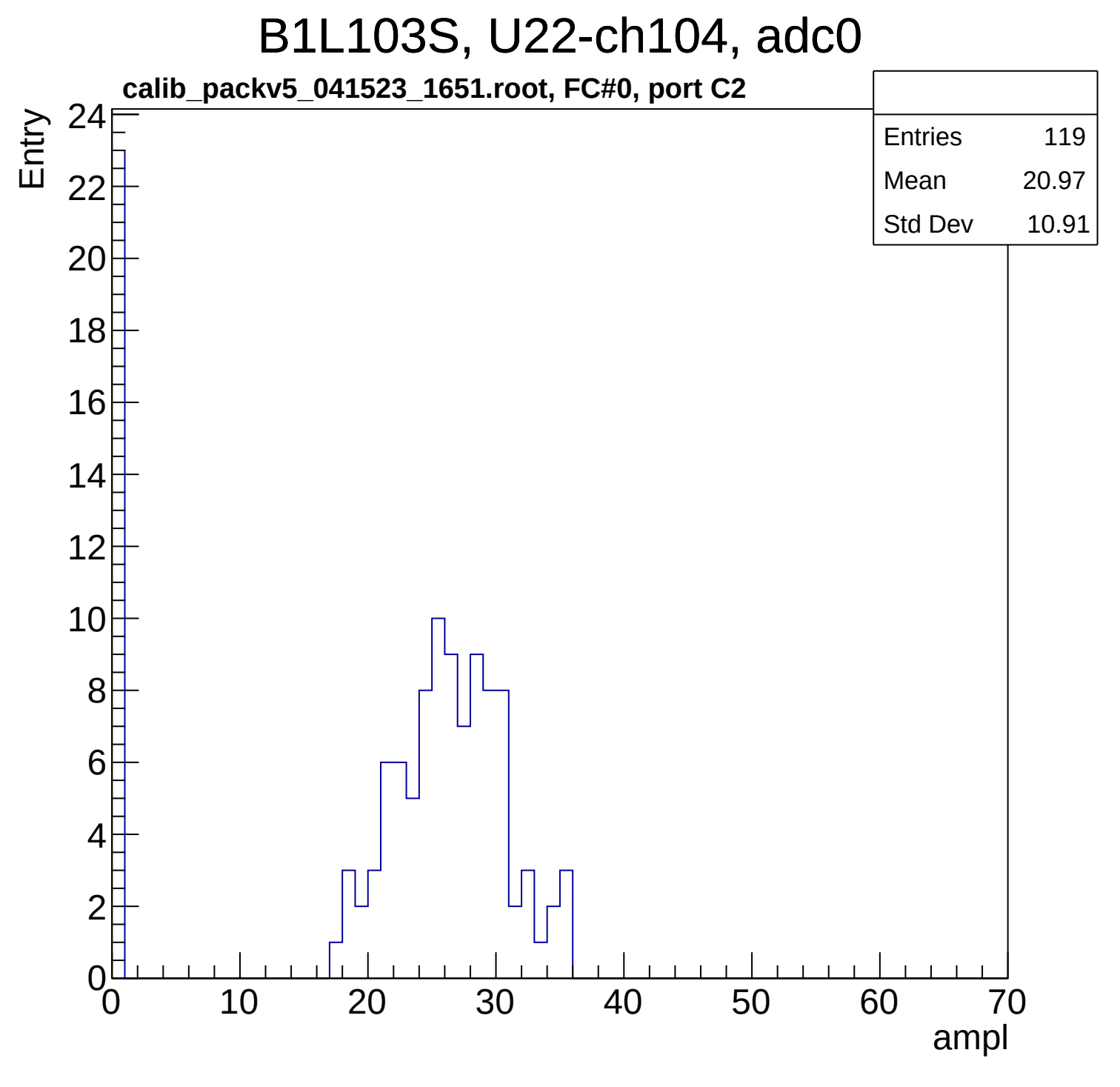
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch104, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 119
Mean 20.97
Std Dev 10.91
Entry
ampl
0
2
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6
8
10
12
14
16
18
20
22
24
0
10
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40
50
60
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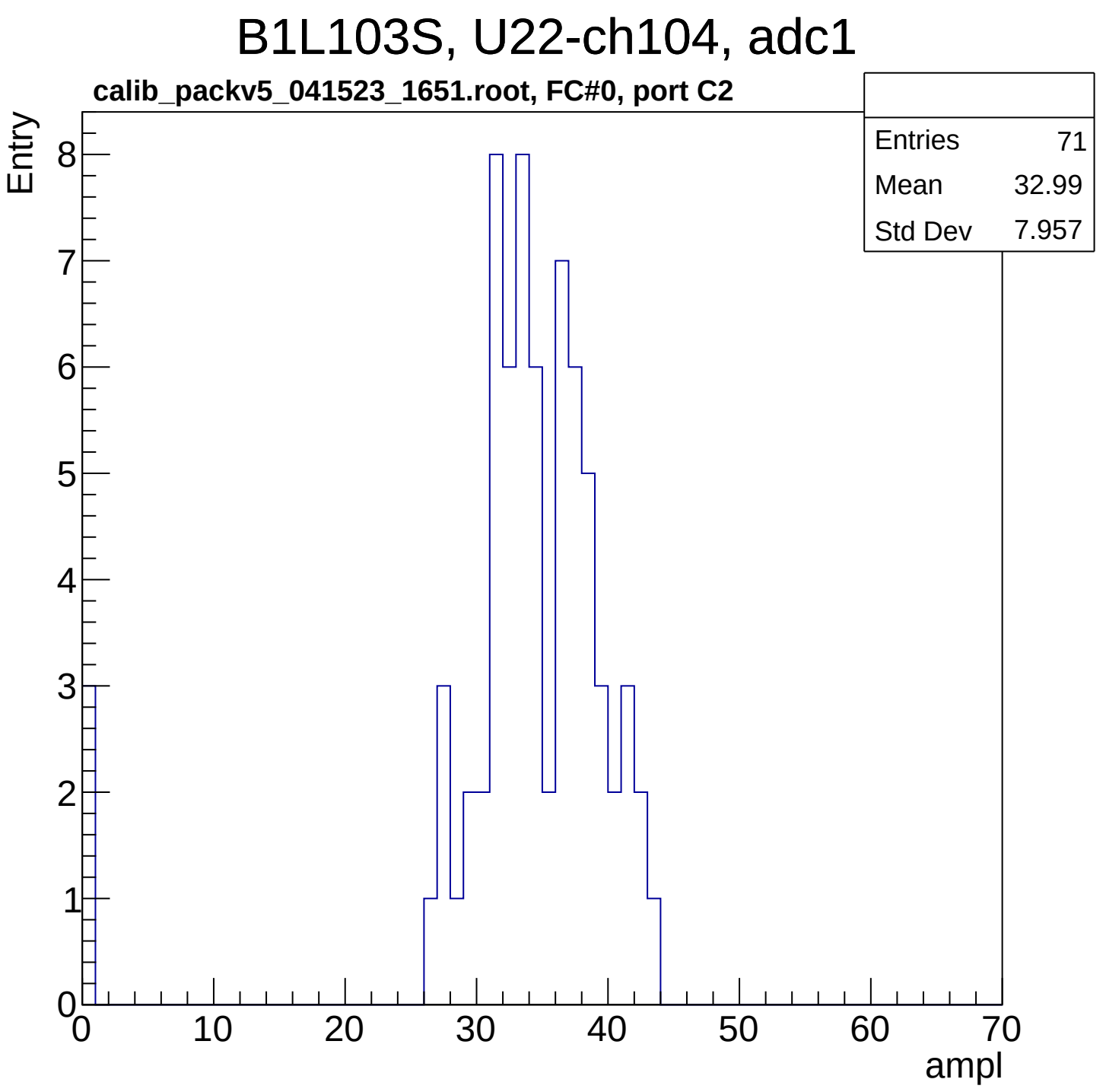
B1L103S, U22-ch104, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 32.99
Std Dev 7.957
Entry
ampl
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2
3
4
5
6
7
8
0
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40
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60
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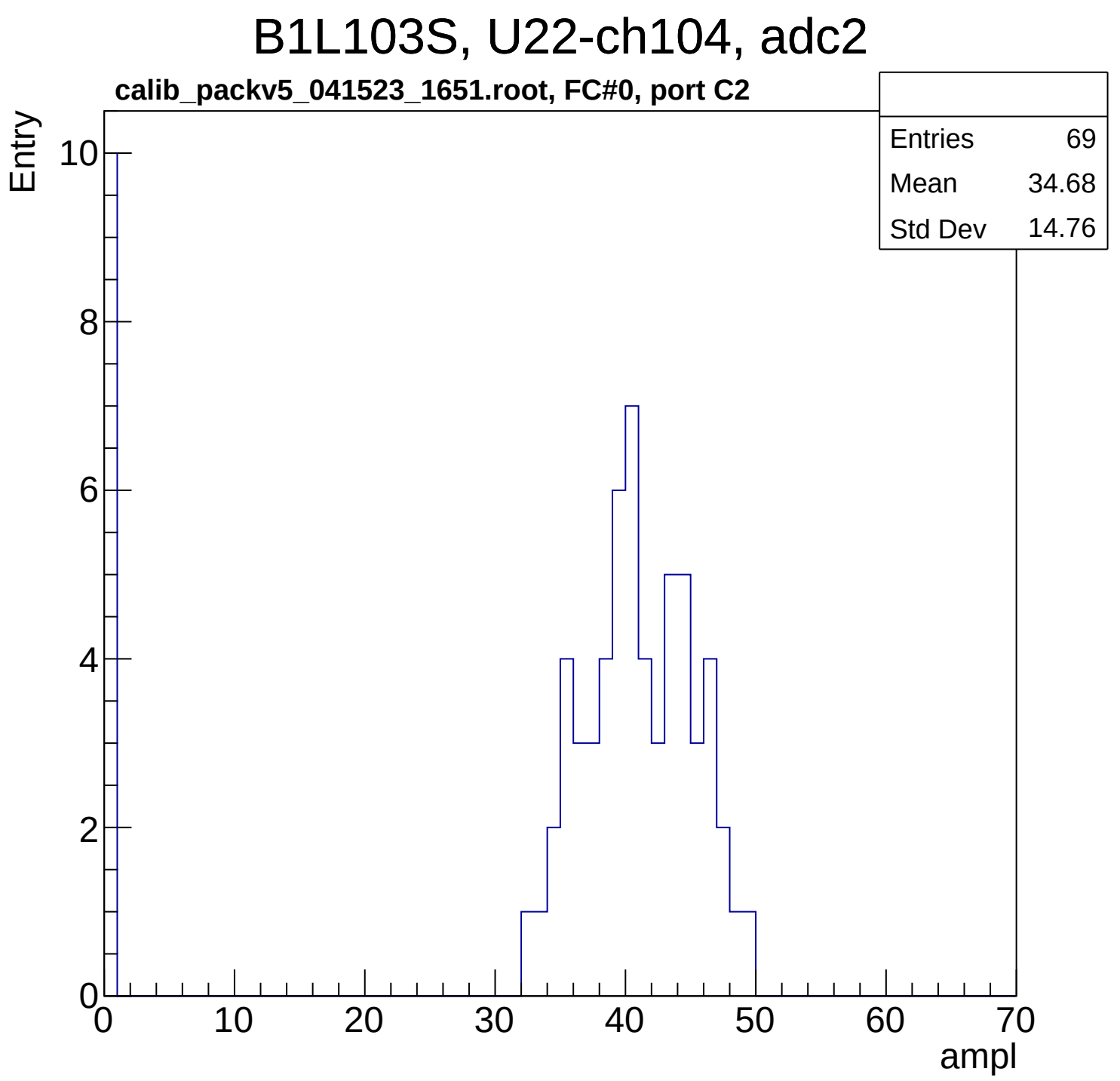
B1L103S, U22-ch104, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 34.68
Std Dev 14.76
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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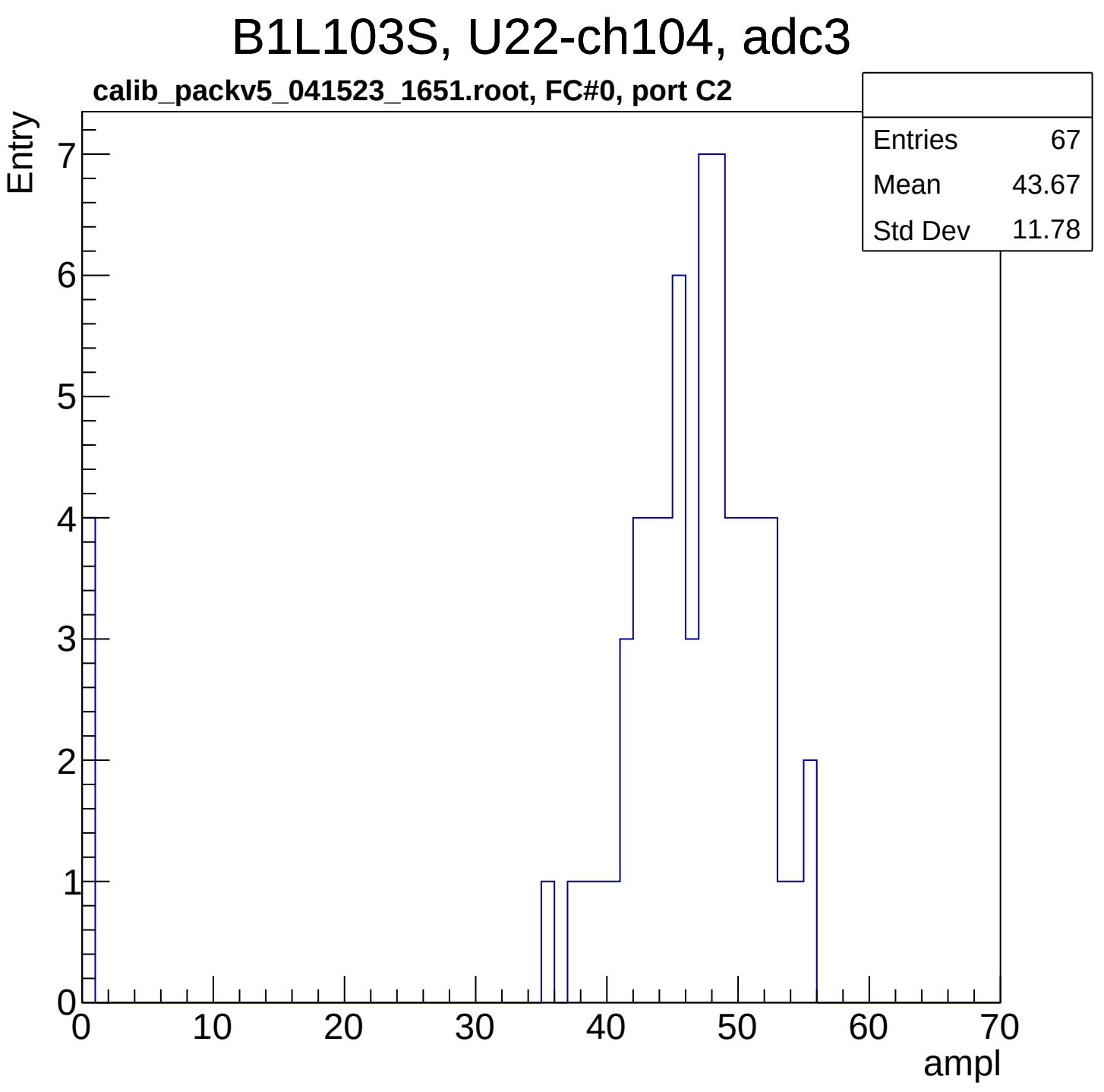
B1L103S, U22-ch104, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 43.67
Std Dev 11.78
Entry
ampl
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4
5
6
7
0
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20
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40
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60
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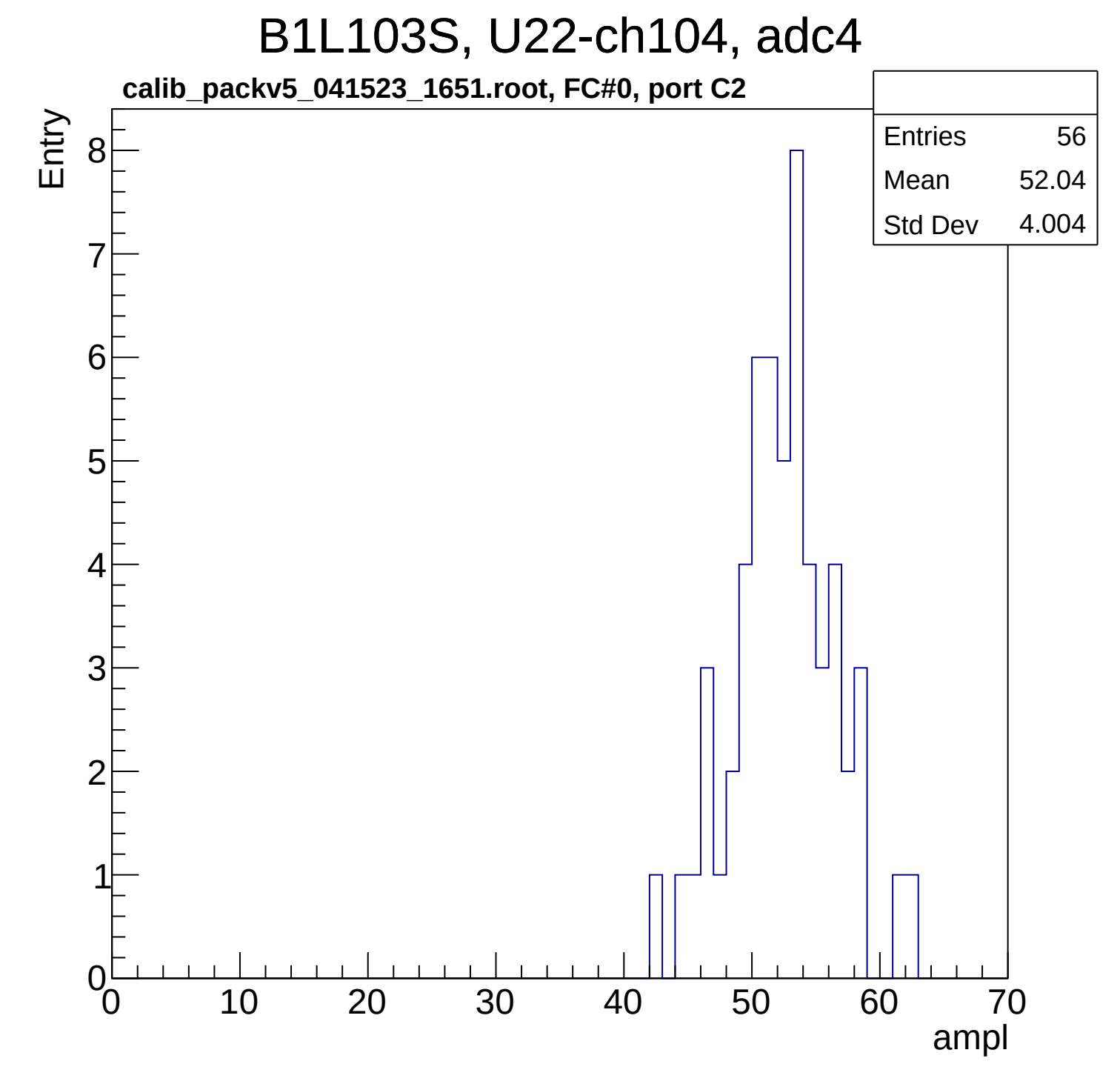
B1L103S, U22-ch104, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 52.04
Std Dev 4.004
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
50
60
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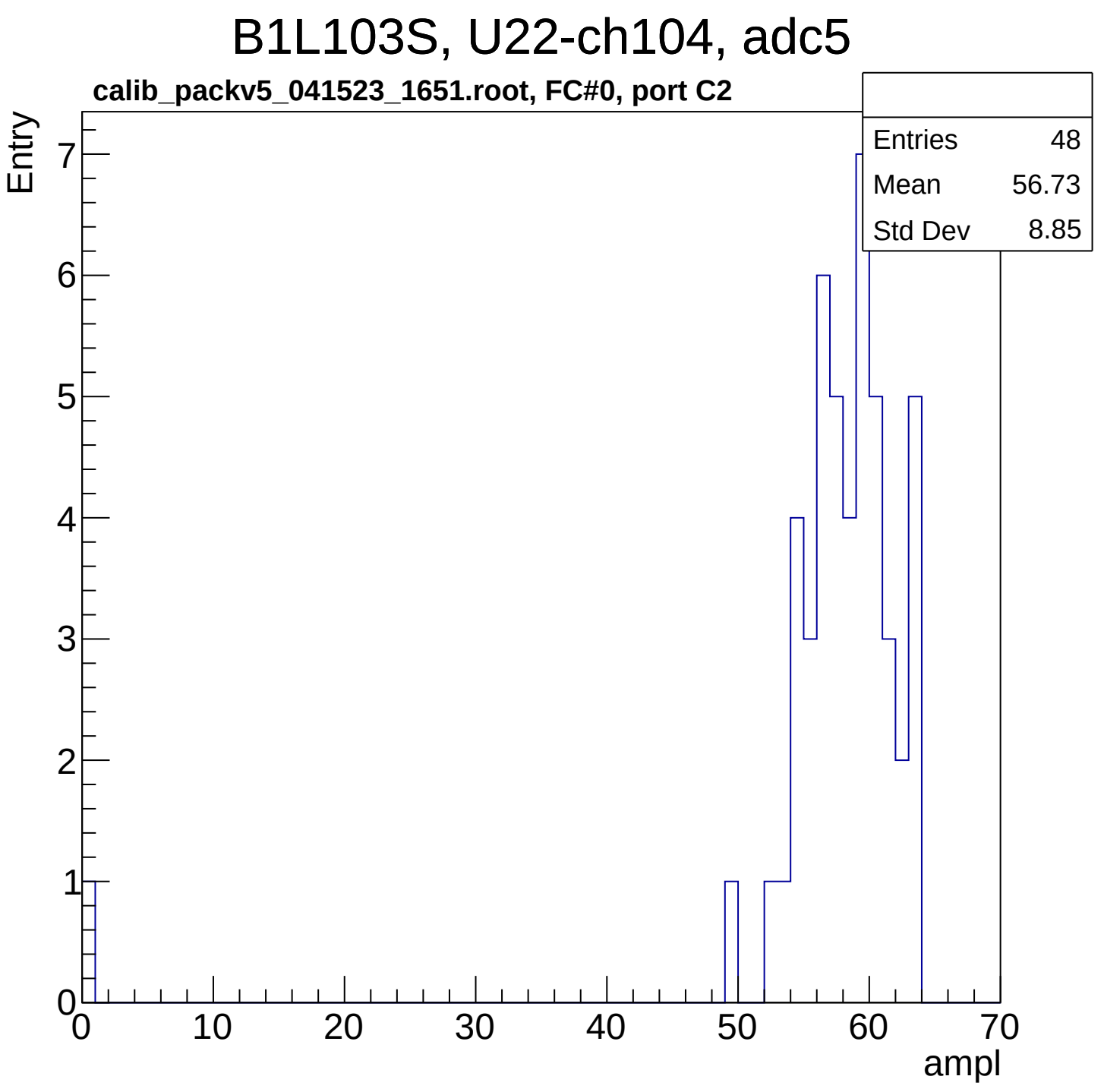
B1L103S, U22-ch104, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 56.73
Std Dev 8.85
Entry
ampl
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2
3
4
5
6
7
0
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20
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40
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60
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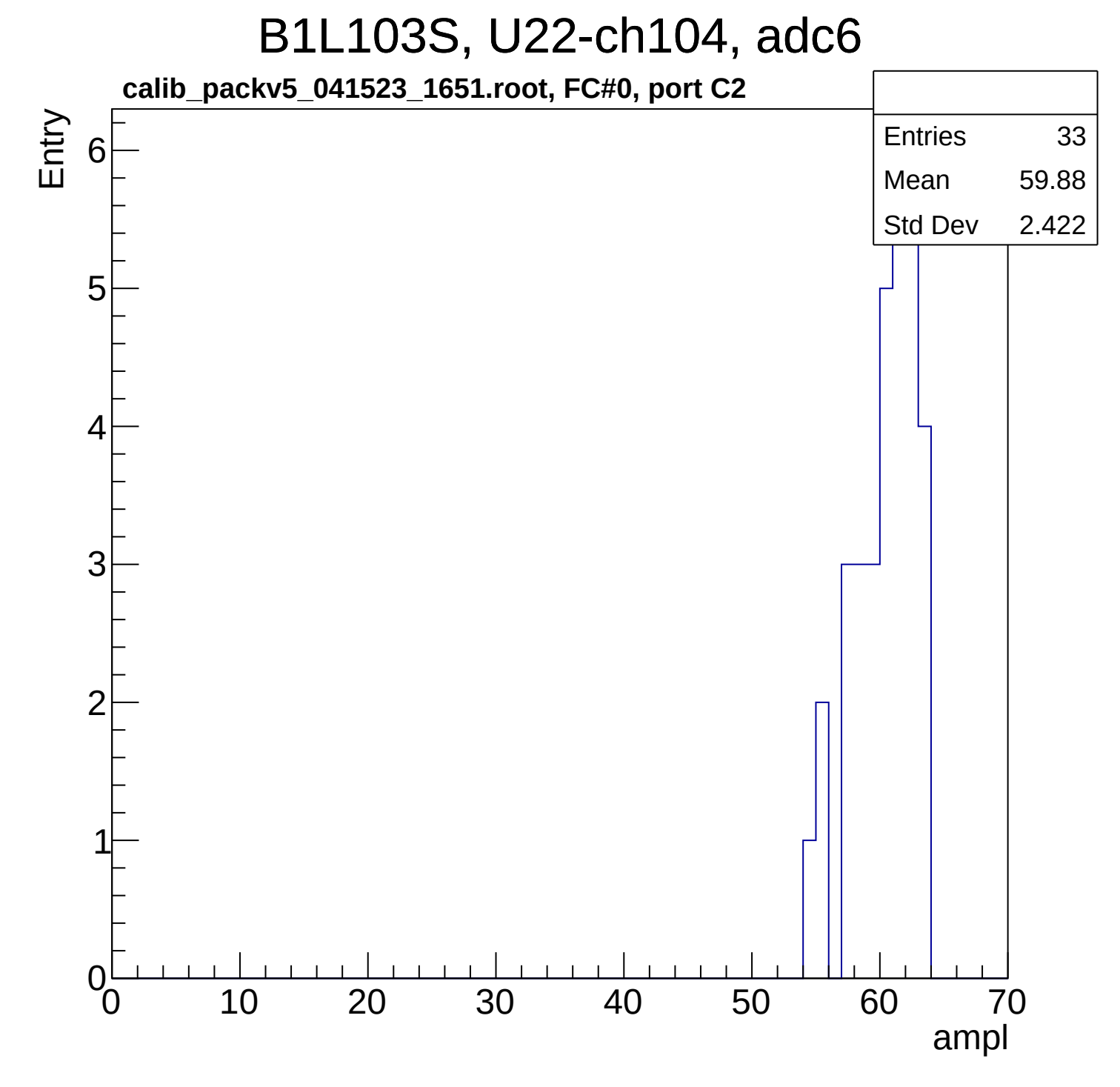
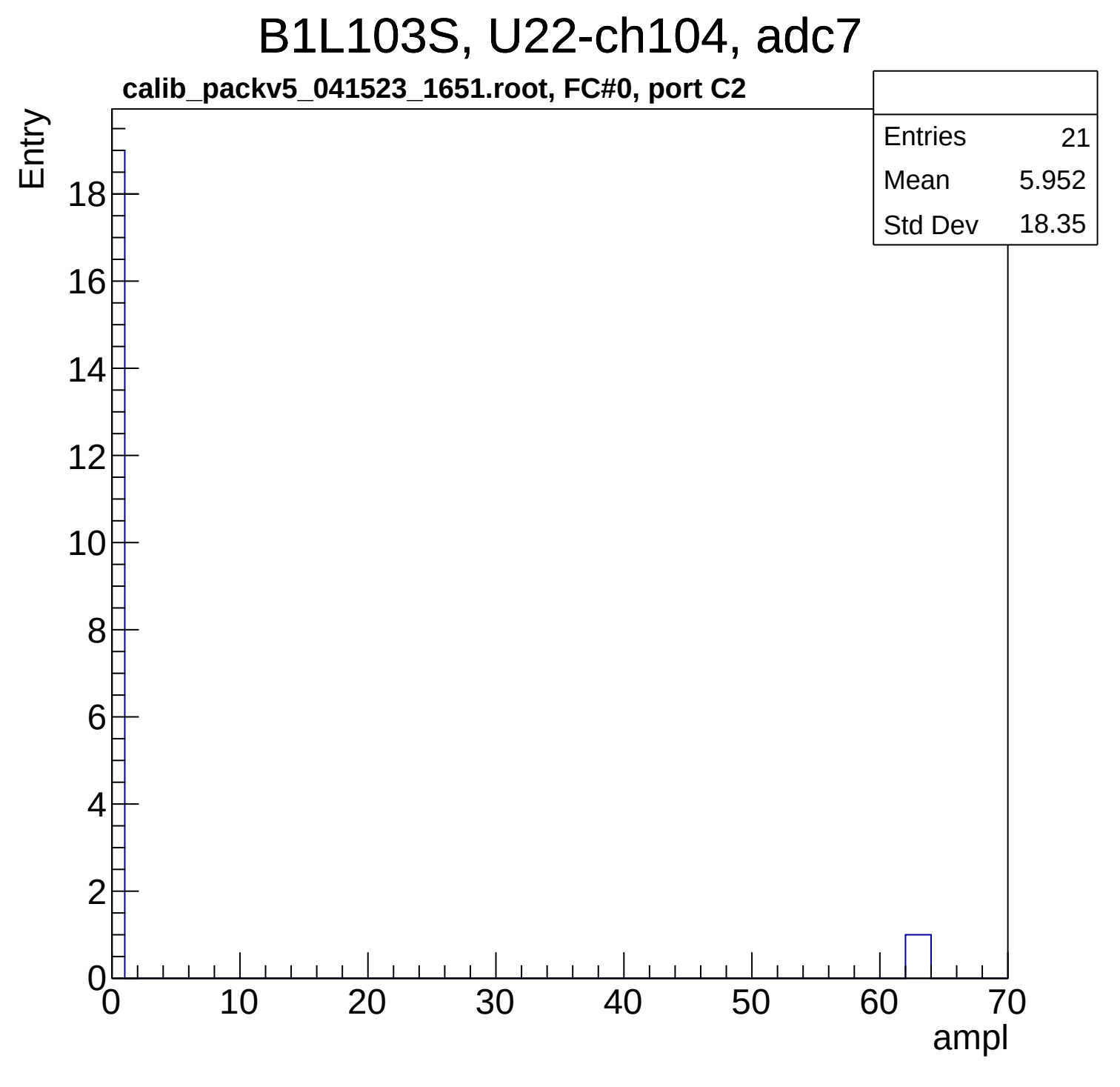

B1L103S, U22-ch104, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 59.88
Std Dev 2.422
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U22-ch104, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.952
Std Dev 18.35
Entry
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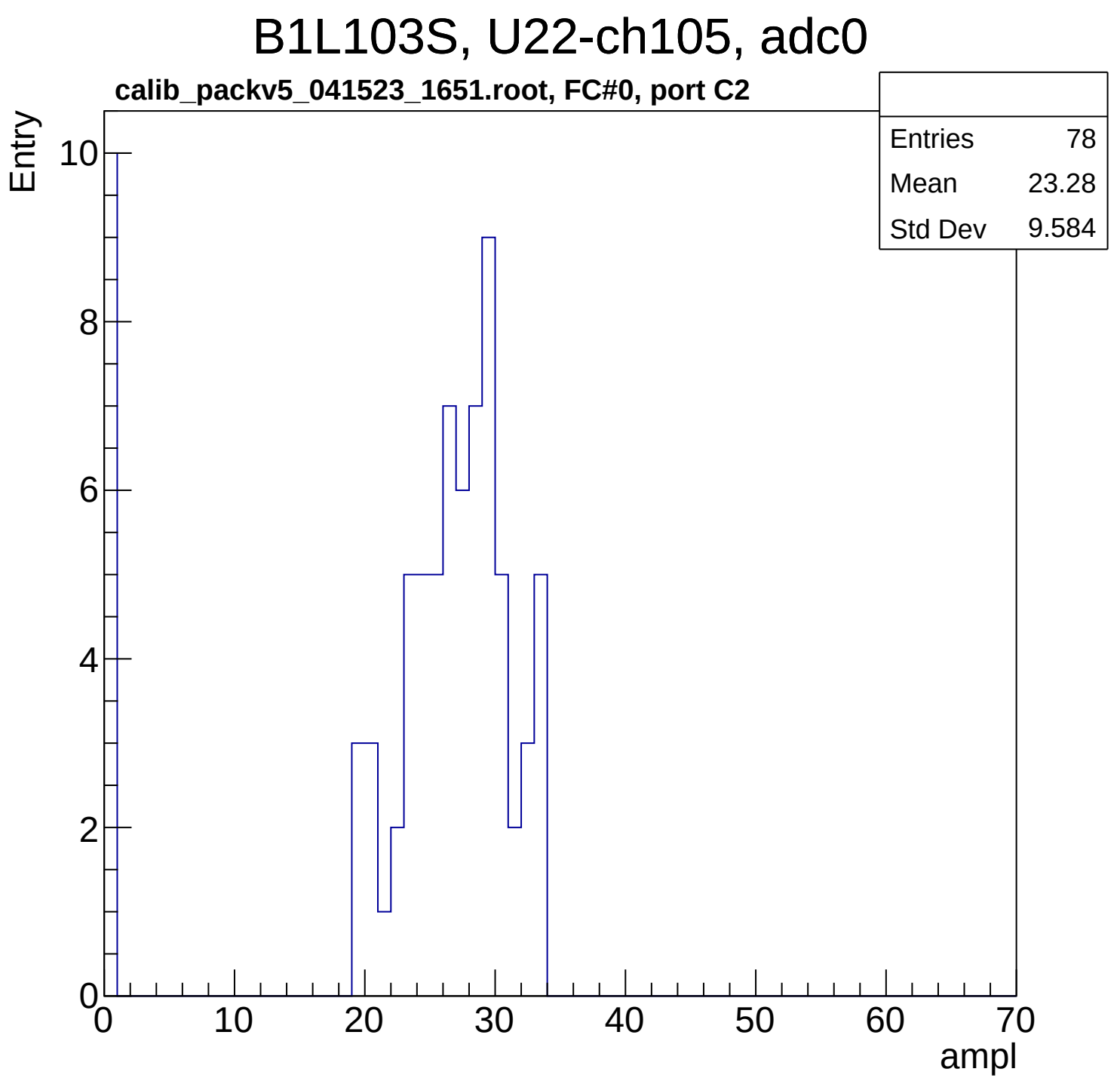
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch105, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 23.28
Std Dev 9.584
Entry
ampl
0
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4
6
8
10
0
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20
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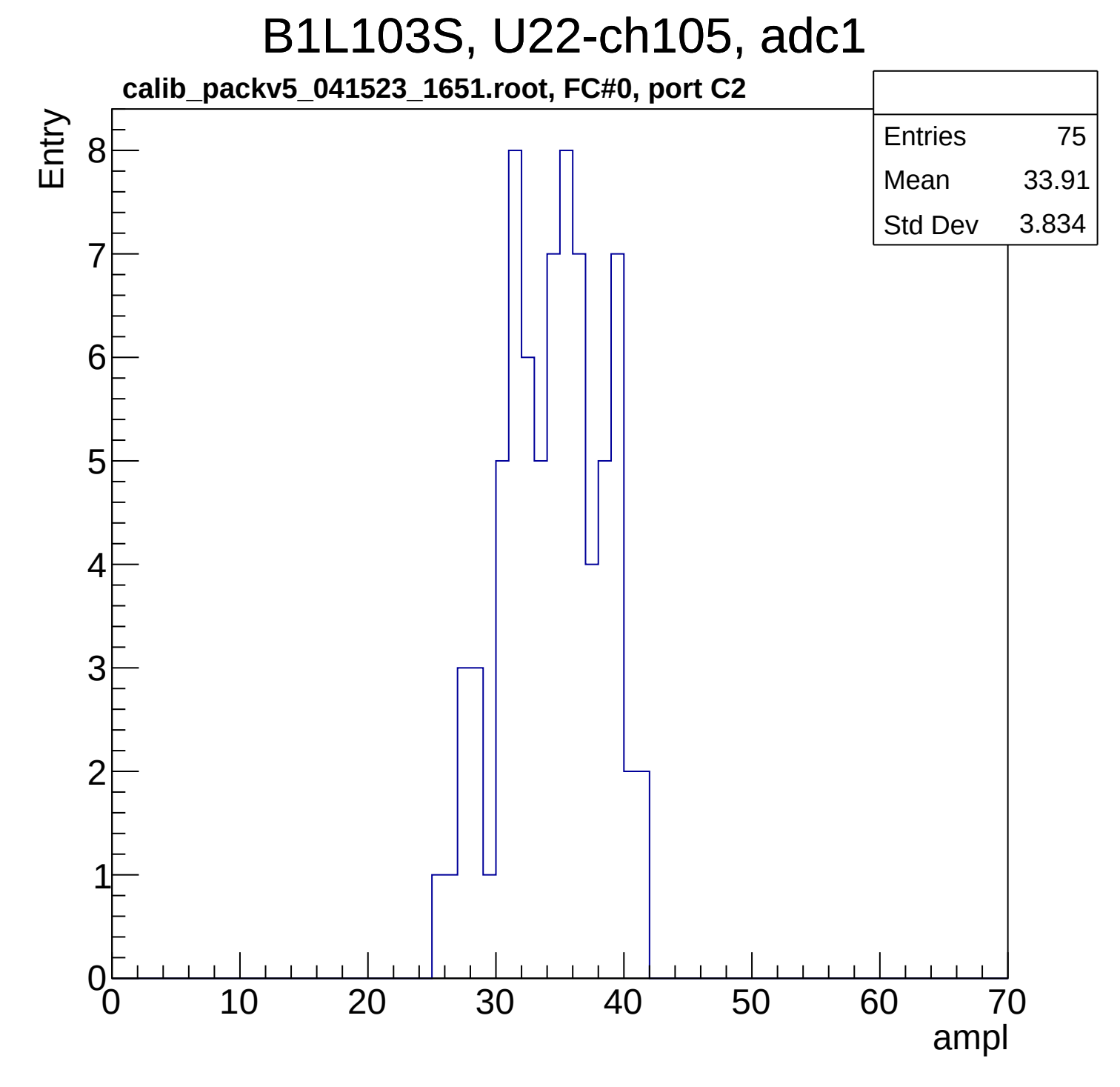
B1L103S, U22-ch105, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 33.91
Std Dev 3.834
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
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60
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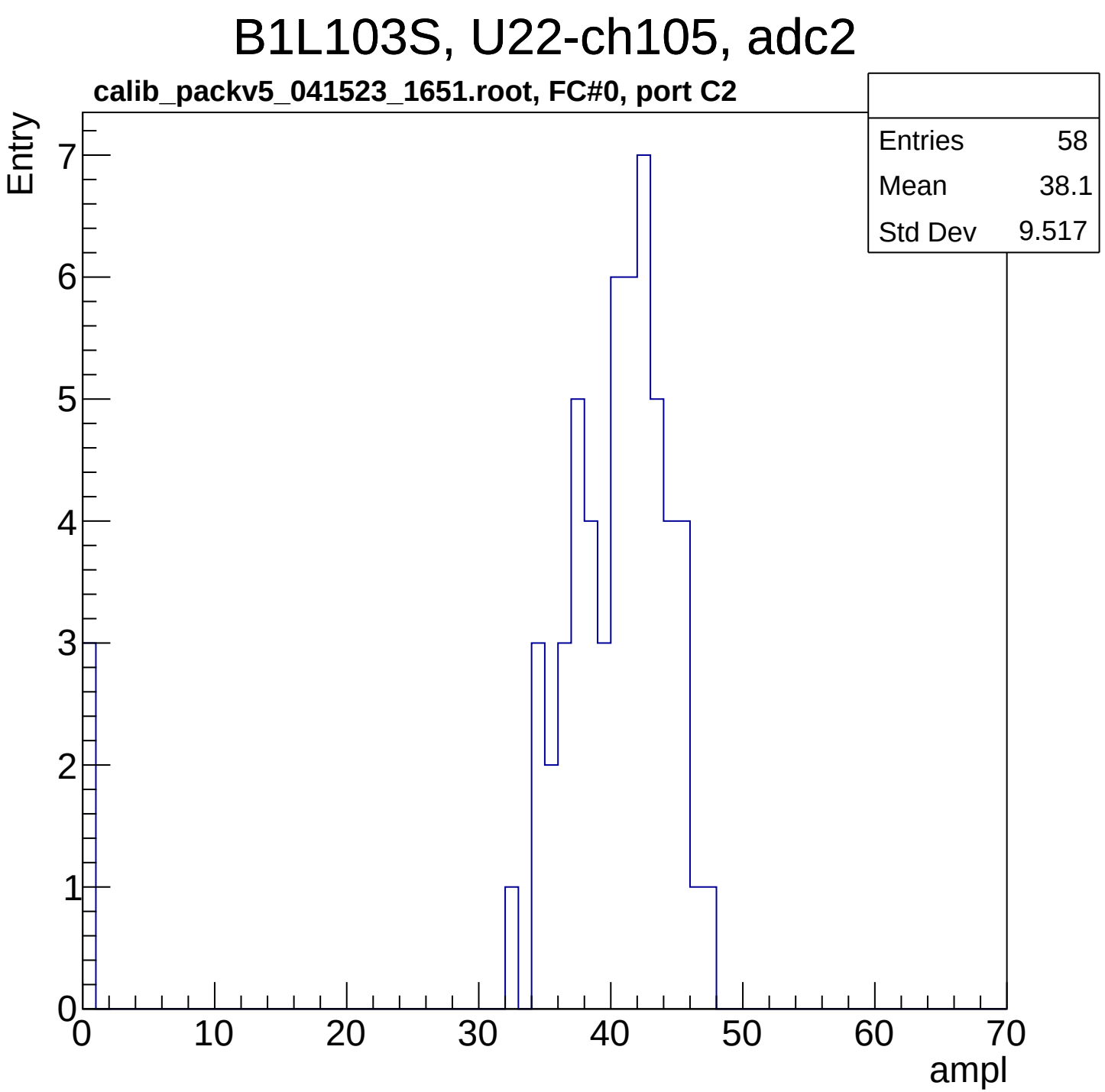
B1L103S, U22-ch105, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 38.1
Std Dev 9.517
Entry
ampl
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1
2
3
4
5
6
7
0
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60
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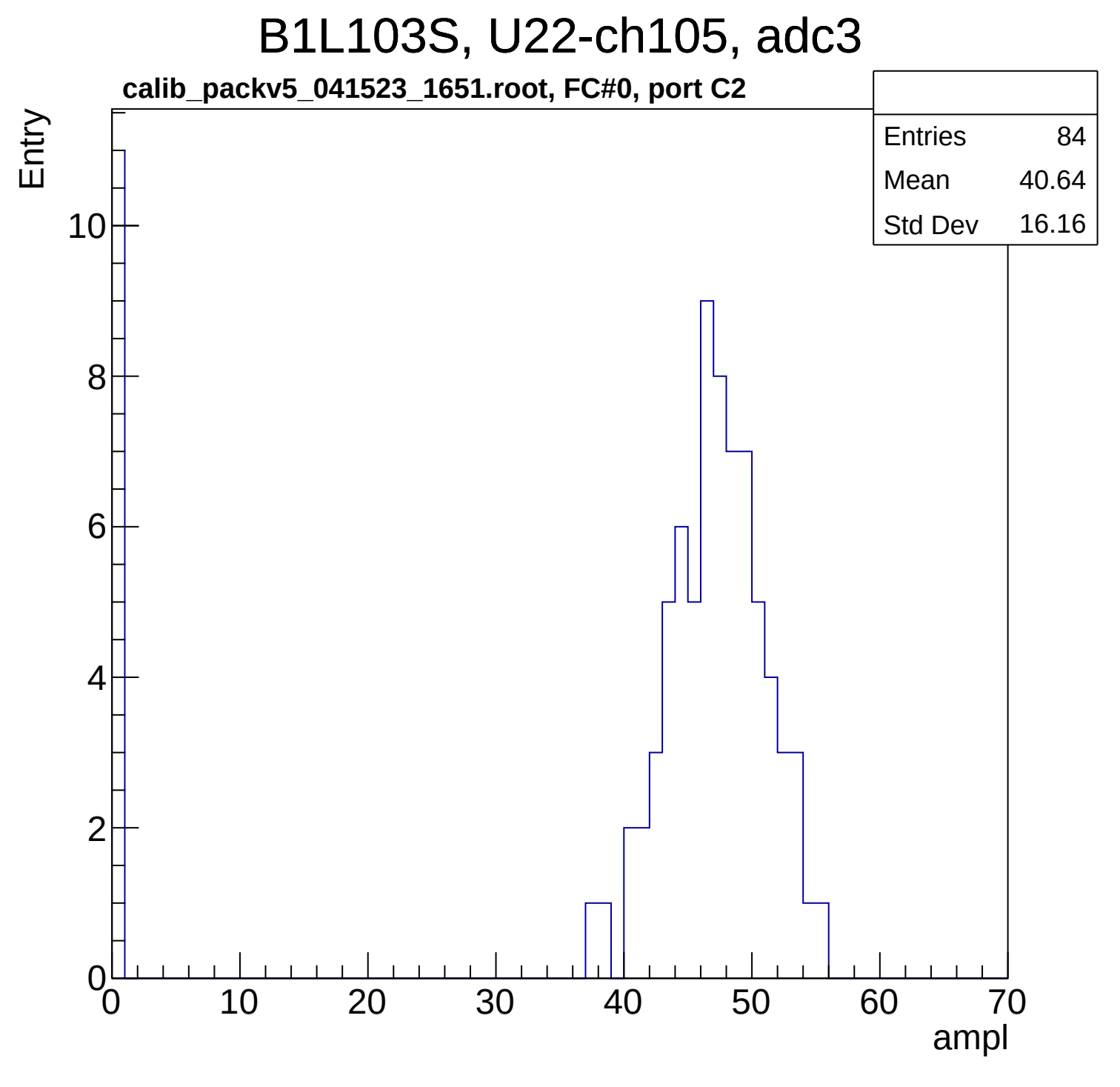
B1L103S, U22-ch105, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 40.64
Std Dev 16.16
Entry
ampl
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0
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40
50
60
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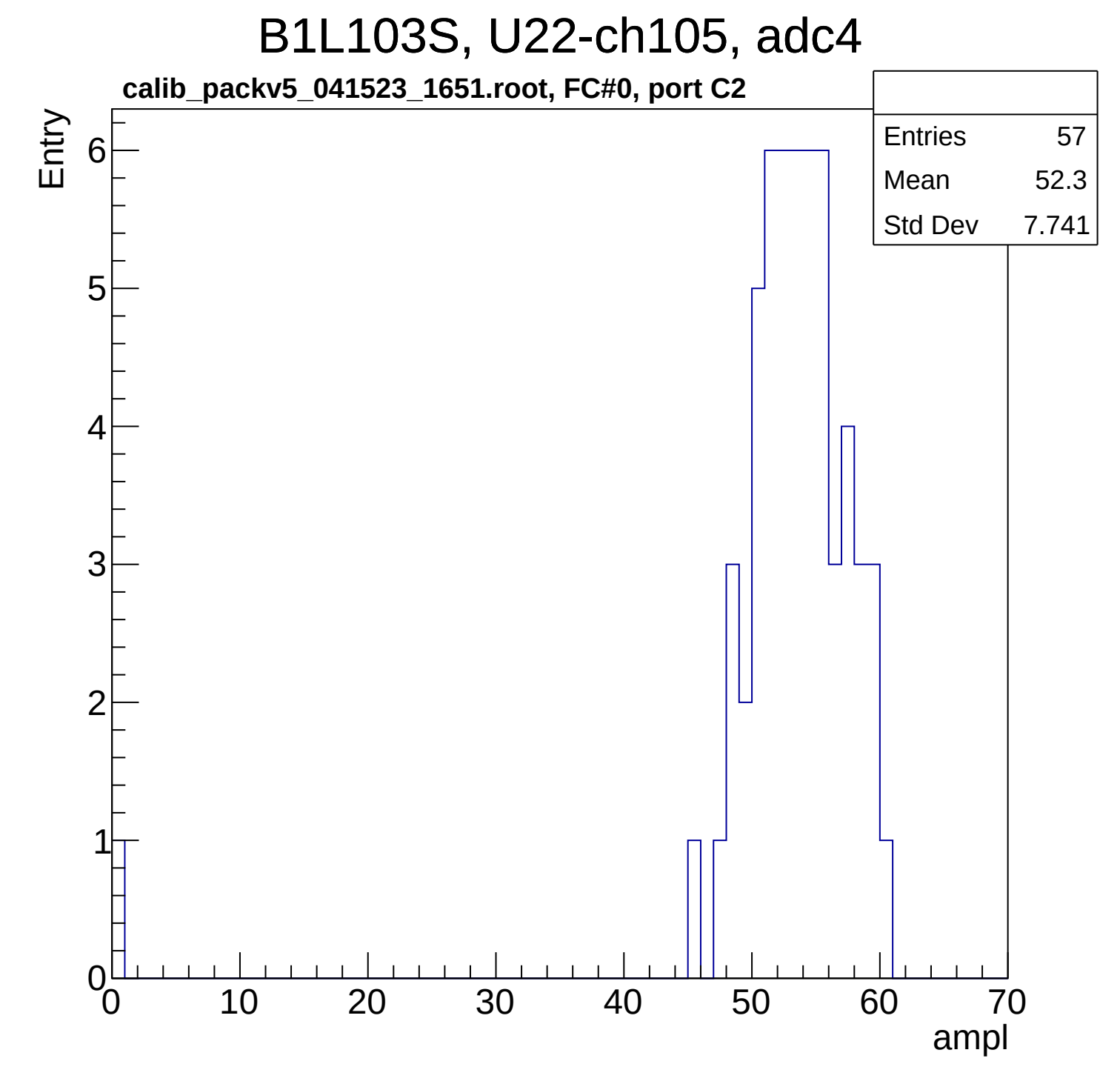
B1L103S, U22-ch105, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 52.3
Std Dev 7.741
Entry
ampl
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6
0
10
20
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40
50
60
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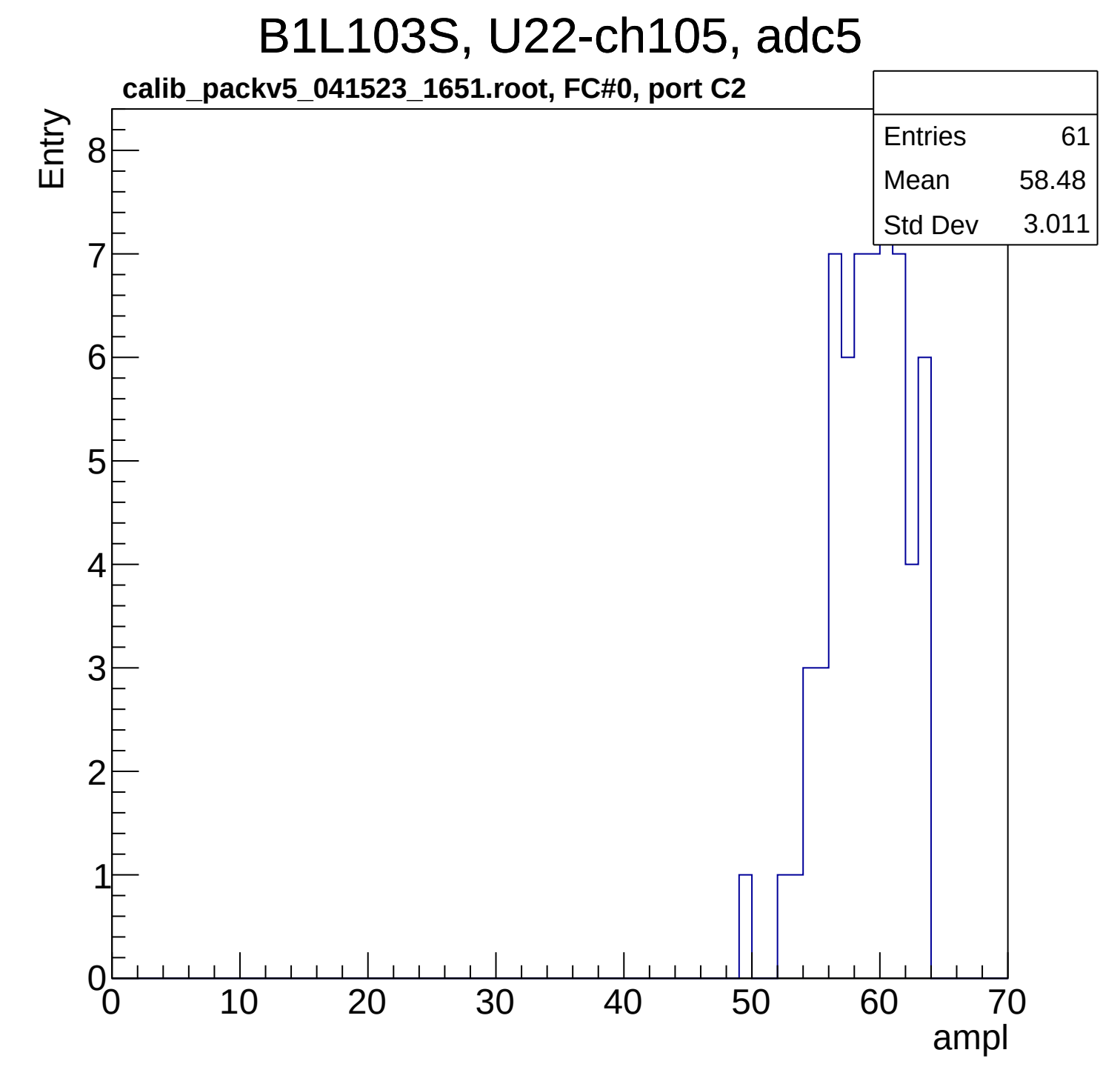
B1L103S, U22-ch105, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 58.48
Std Dev 3.011
Entry
ampl
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4
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6
7
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0
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40
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60
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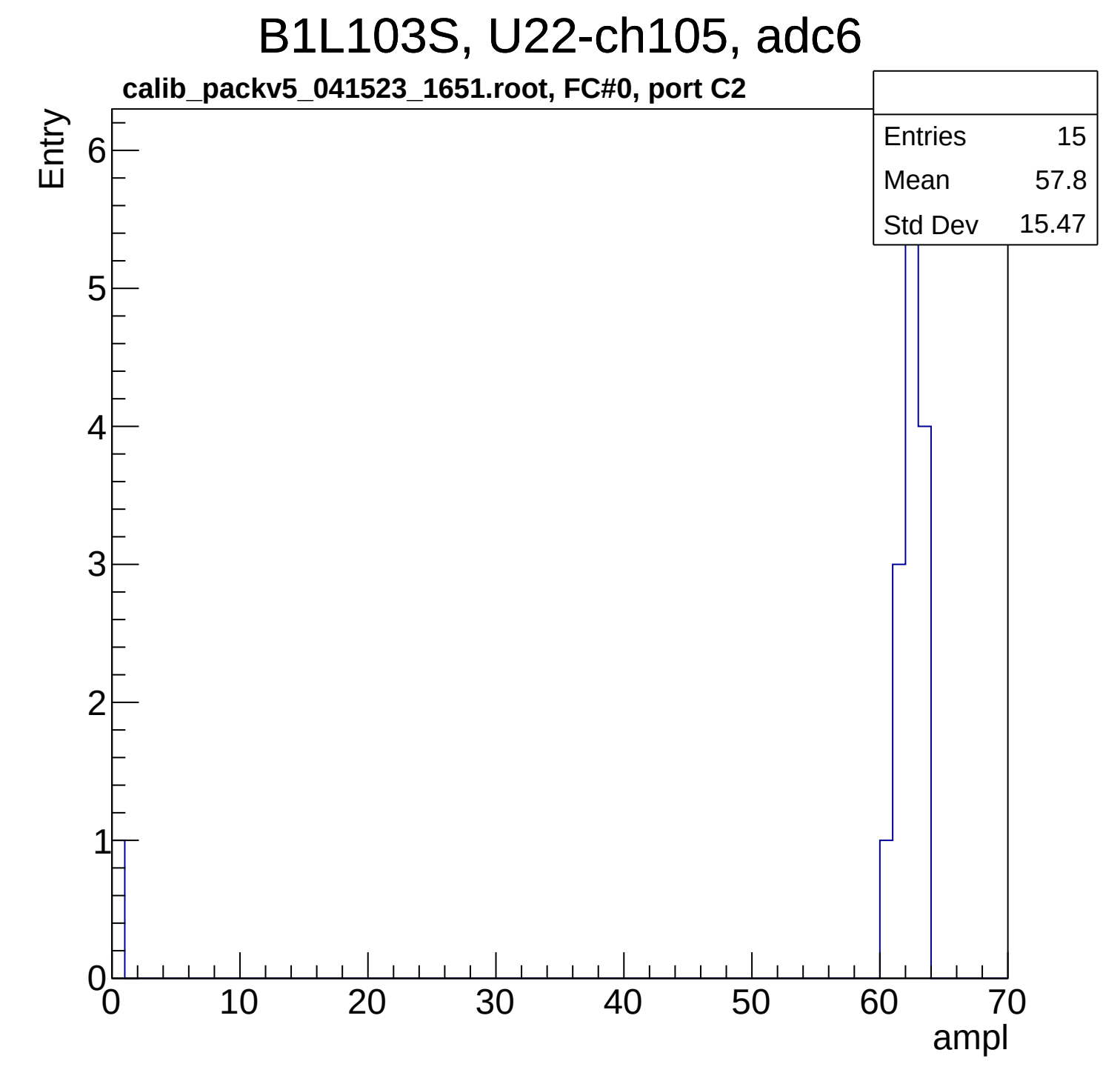
B1L103S, U22-ch105, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 57.8
Std Dev 15.47
Entry
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1
2
3
4
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0
10
20
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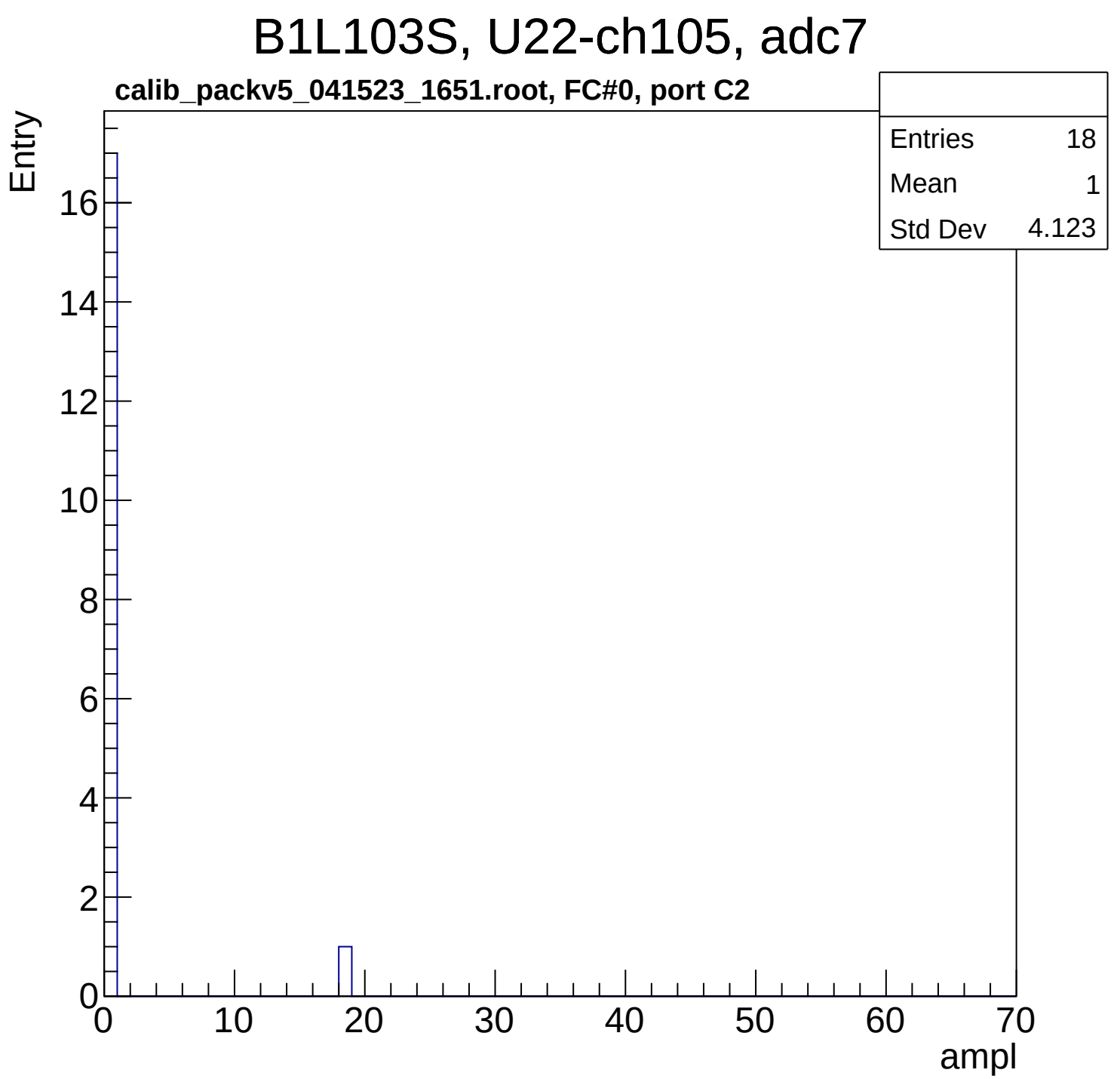
40
50
60
70
ampl


B1L103S, U22-ch105, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1
Std Dev 4.123
Entry
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8
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12
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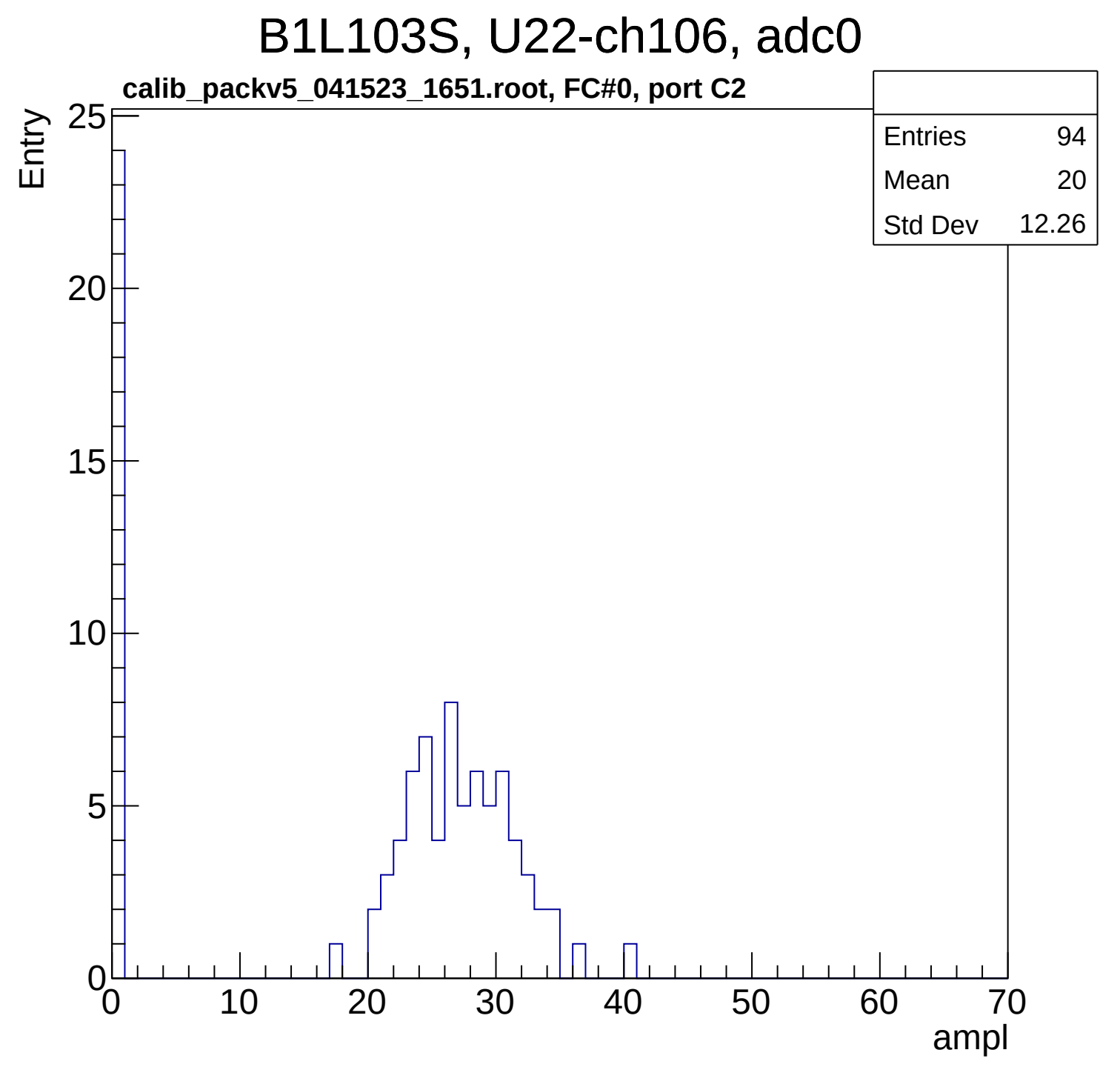
50
60
70
ampl


B1L103S, U22-ch106, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 20
Std Dev 12.26
Entry
ampl
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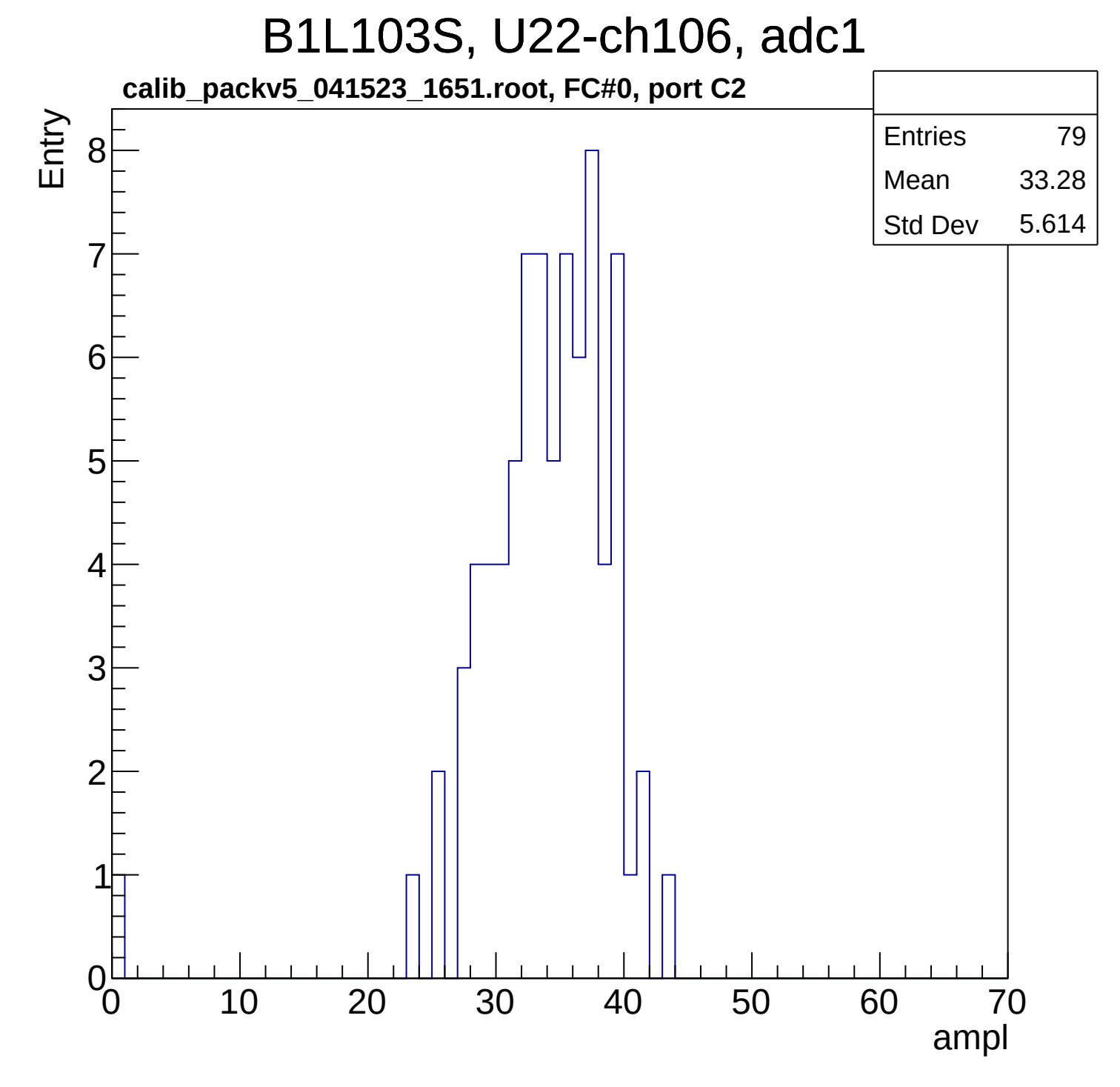
B1L103S, U22-ch106, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 33.28
Std Dev 5.614
Entry
ampl
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3
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5
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7
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0
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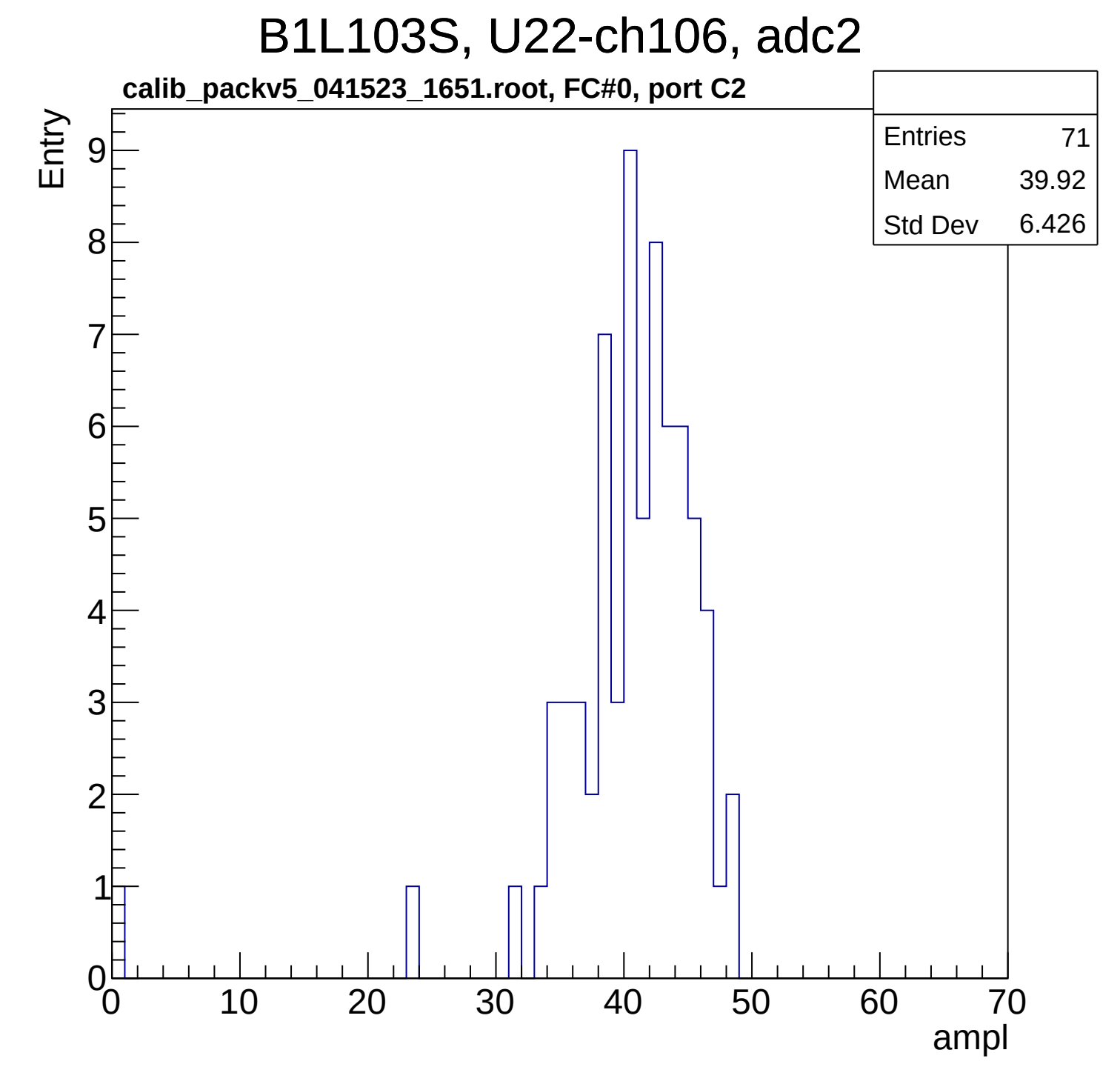
B1L103S, U22-ch106, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 39.92
Std Dev 6.426
Entry
ampl
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6
7
8
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0
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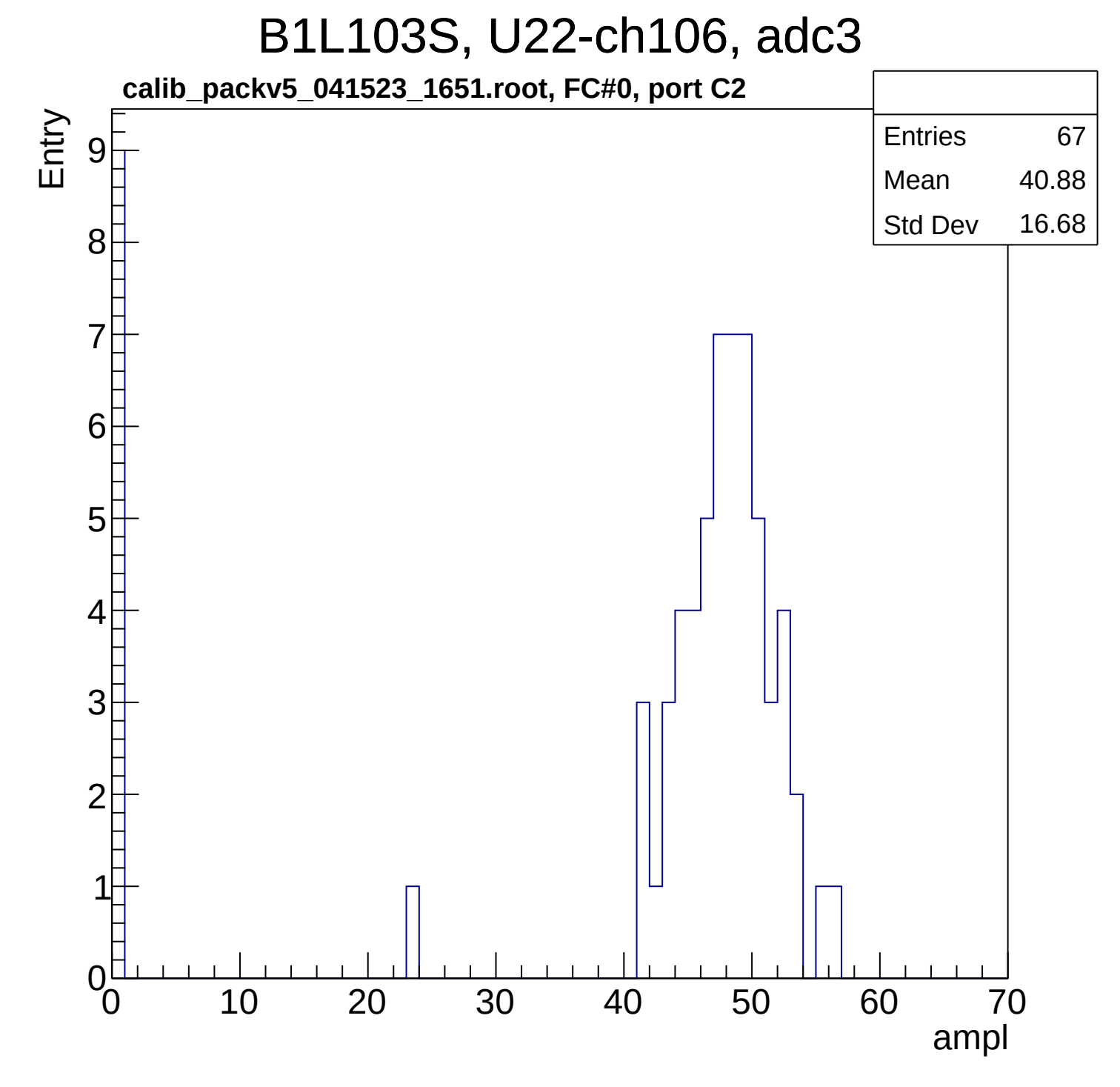
B1L103S, U22-ch106, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 40.88
Std Dev 16.68
Entry
ampl
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4
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6
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0
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60
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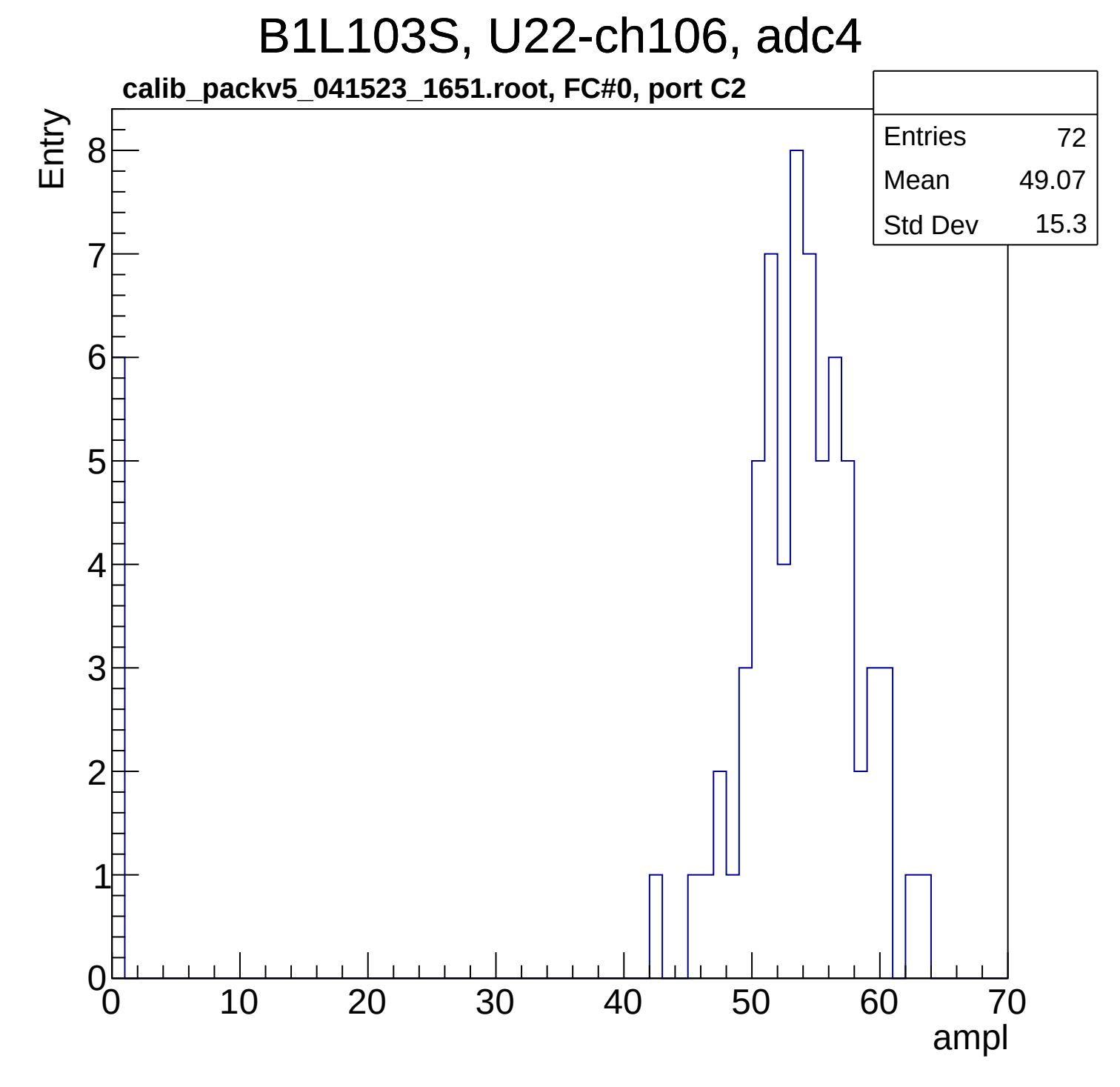
B1L103S, U22-ch106, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 49.07
Std Dev 15.3
Entry
ampl
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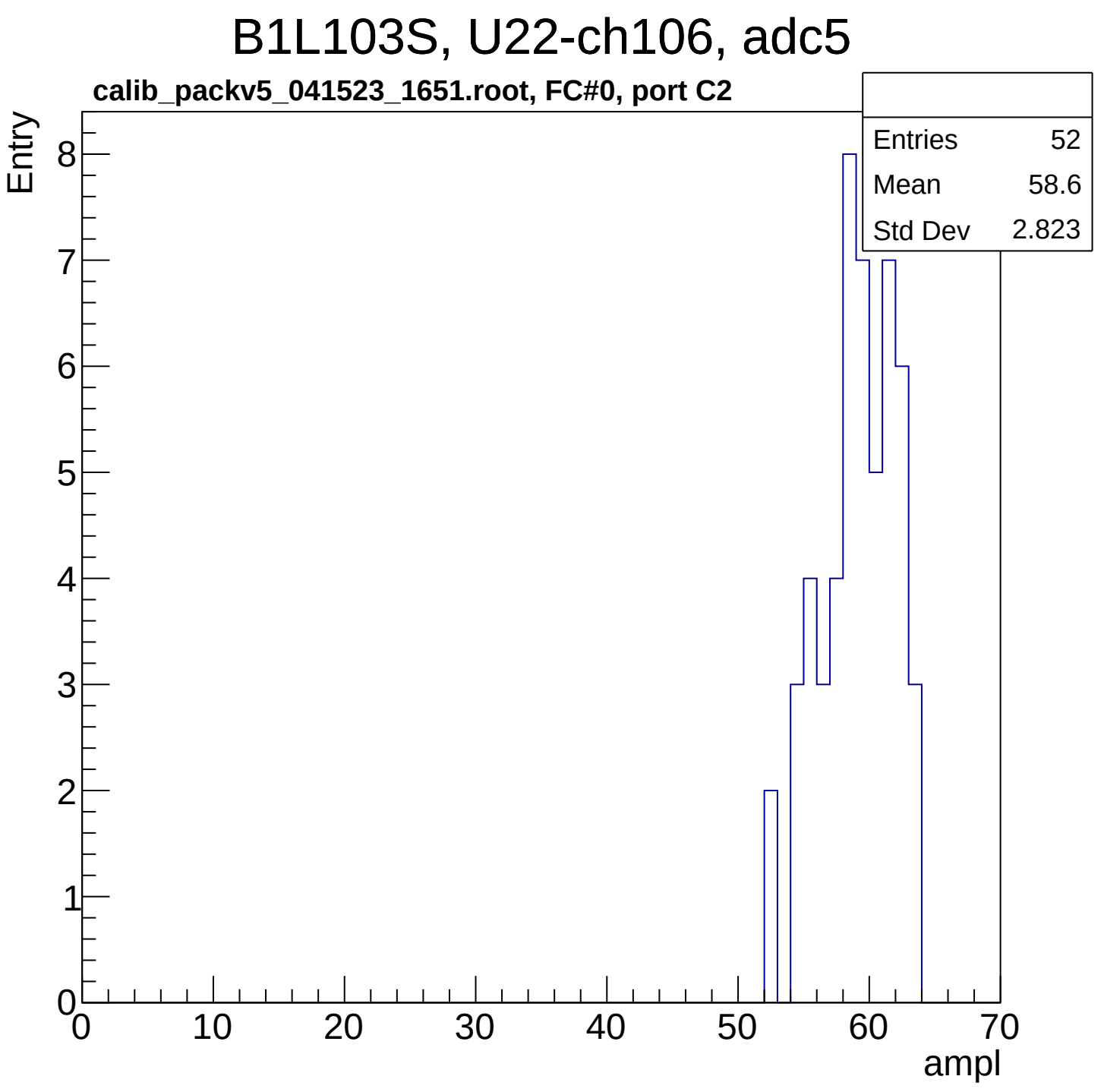
B1L103S, U22-ch106, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 58.6
Std Dev 2.823
Entry
ampl
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0
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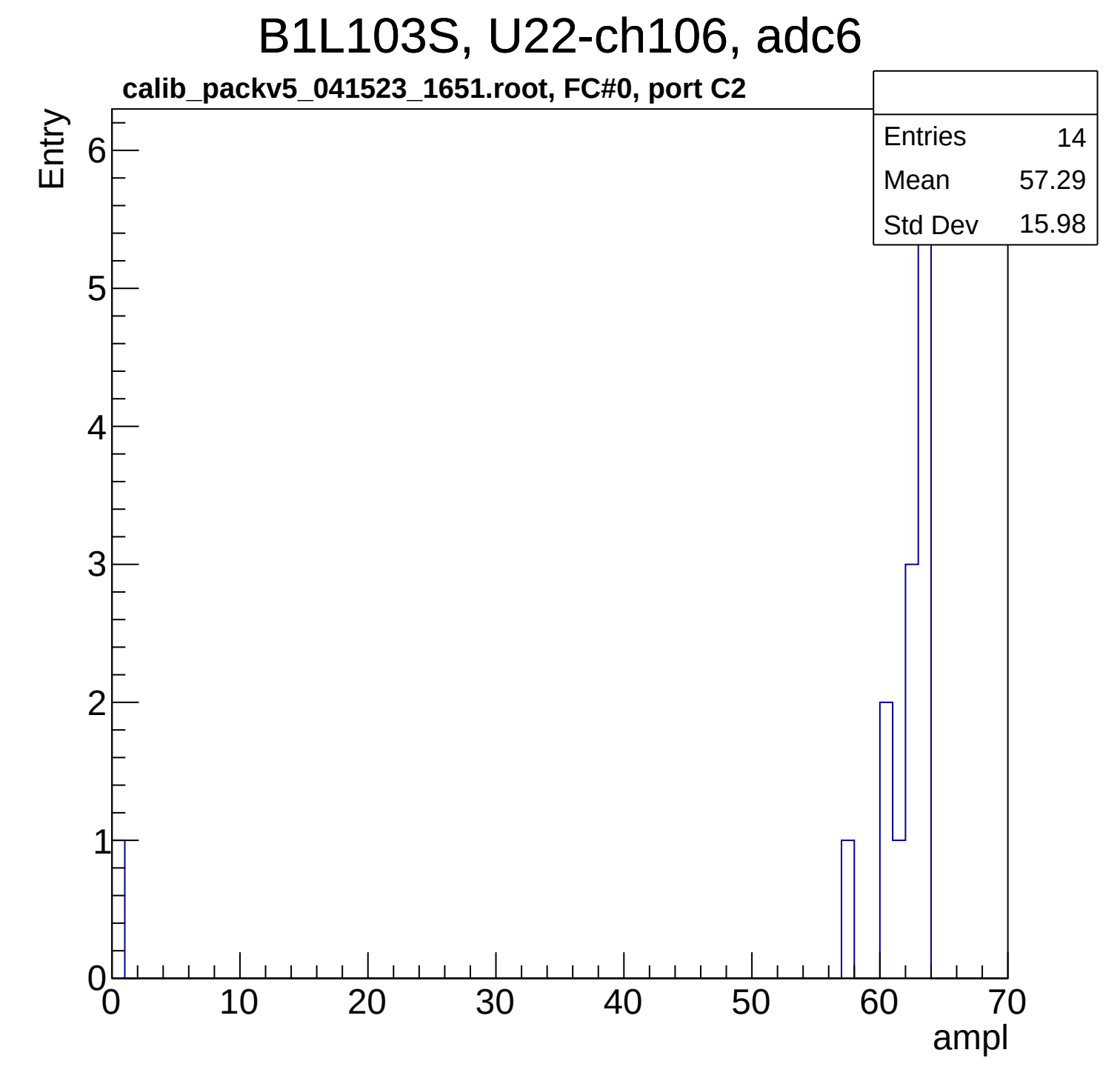
B1L103S, U22-ch106, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 57.29
Std Dev 15.98
Entry
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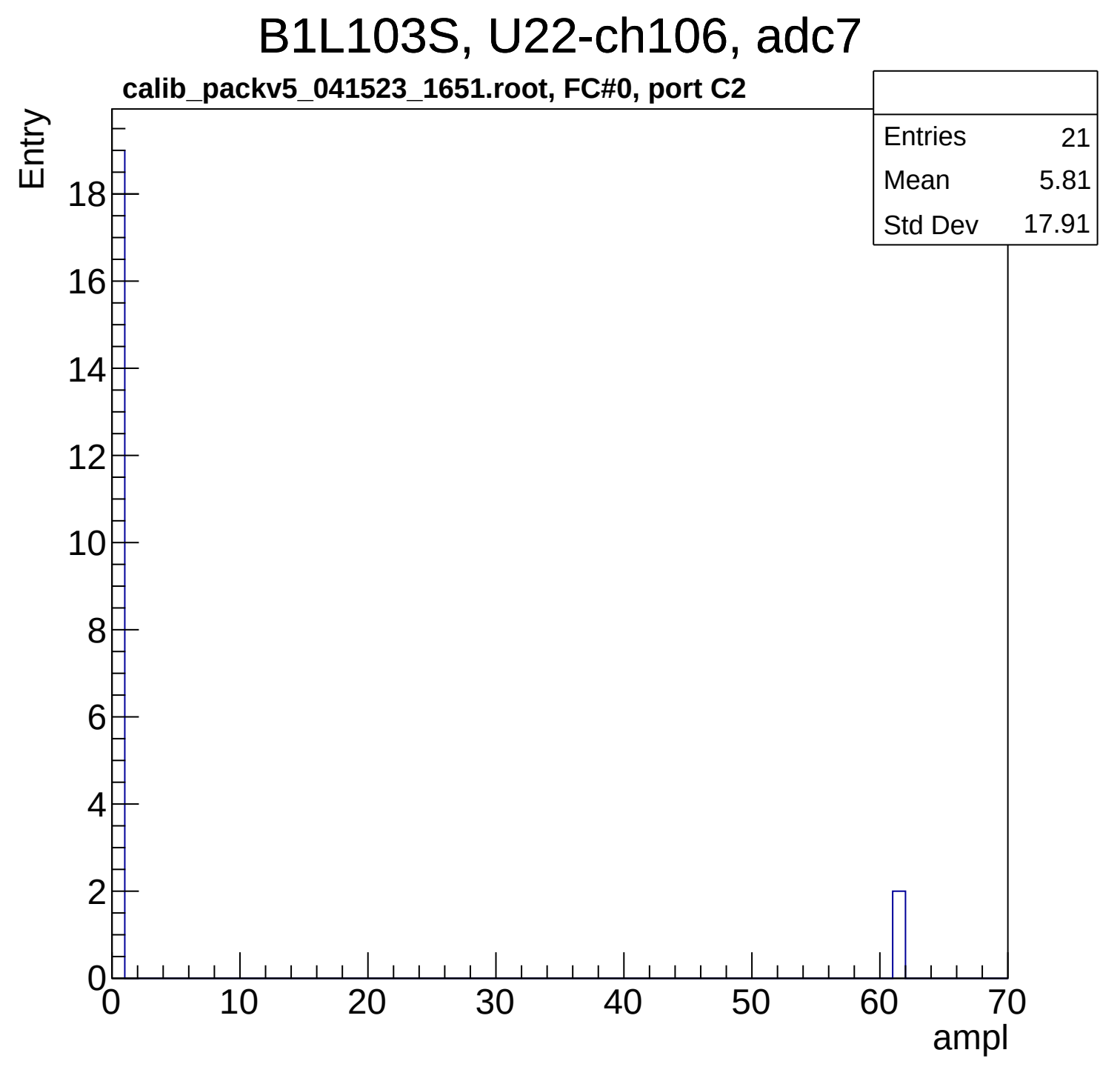
50
60
70
ampl


B1L103S, U22-ch106, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.81
Std Dev 17.91
Entry
0
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6
8
10
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14
16
18
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10
20
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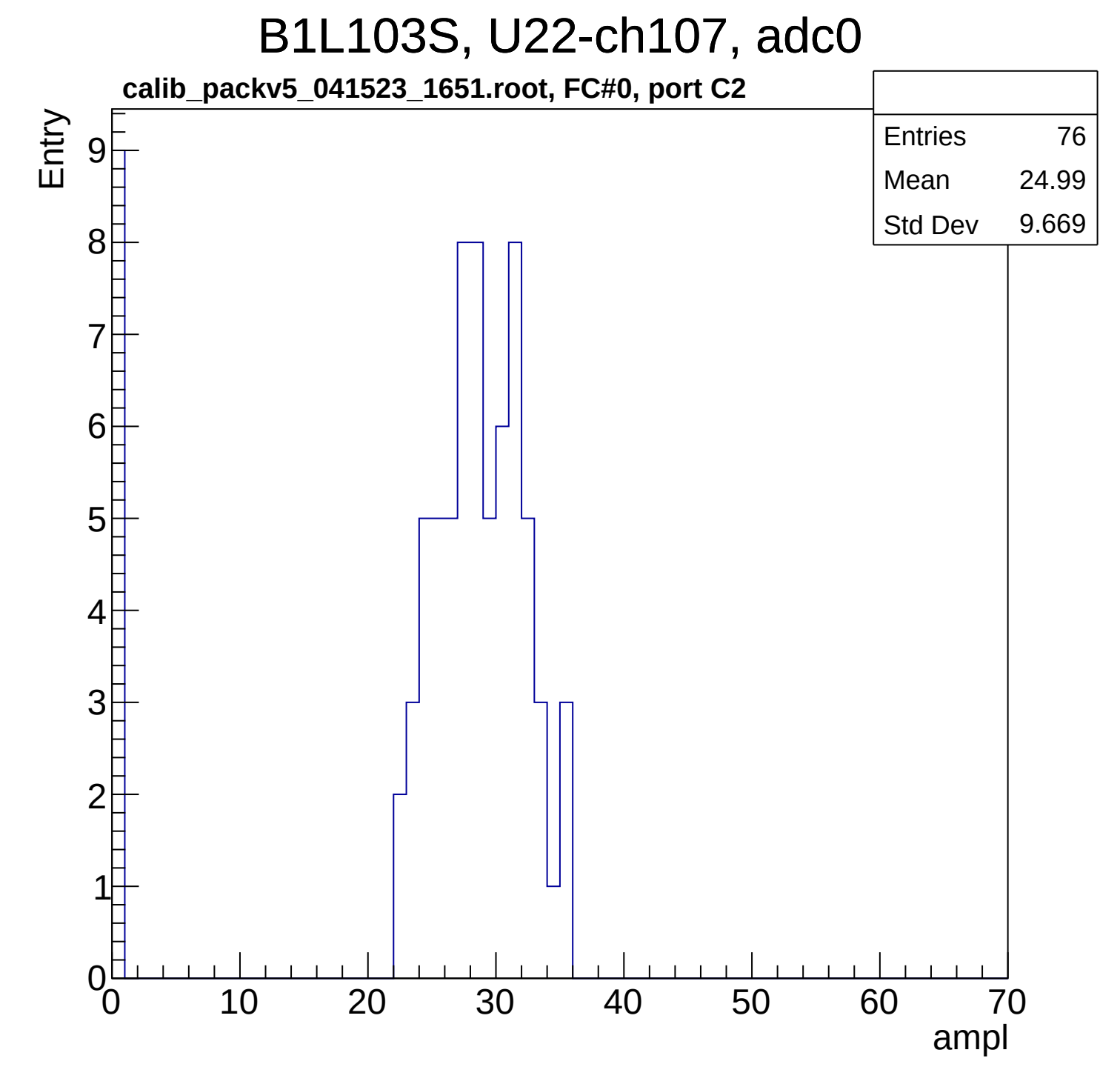
50
60
70
ampl


B1L103S, U22-ch107, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 24.99
Std Dev 9.669
Entry
ampl
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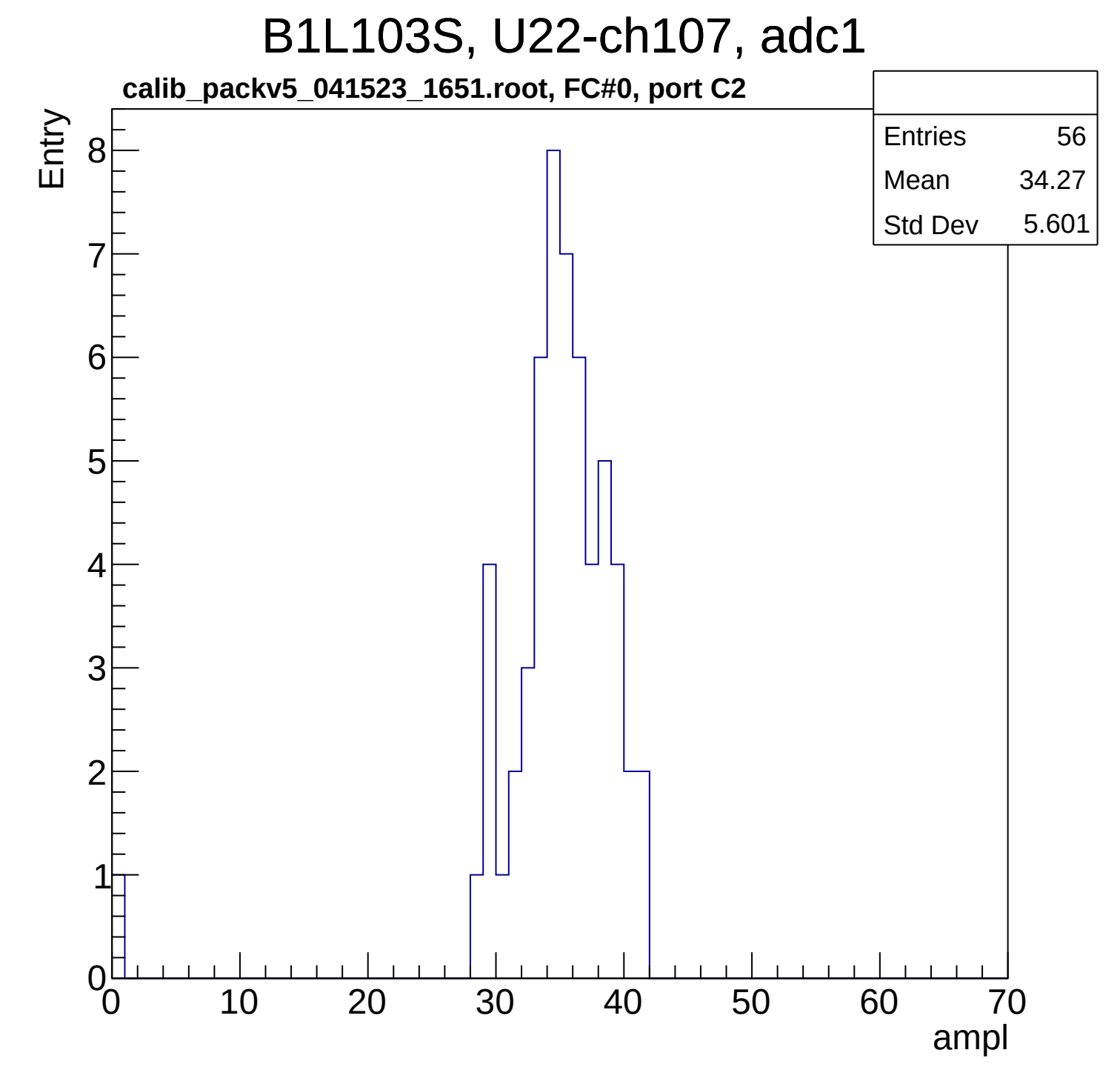
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch107, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 34.27
Std Dev 5.601
Entry
ampl
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2
3
4
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40
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60
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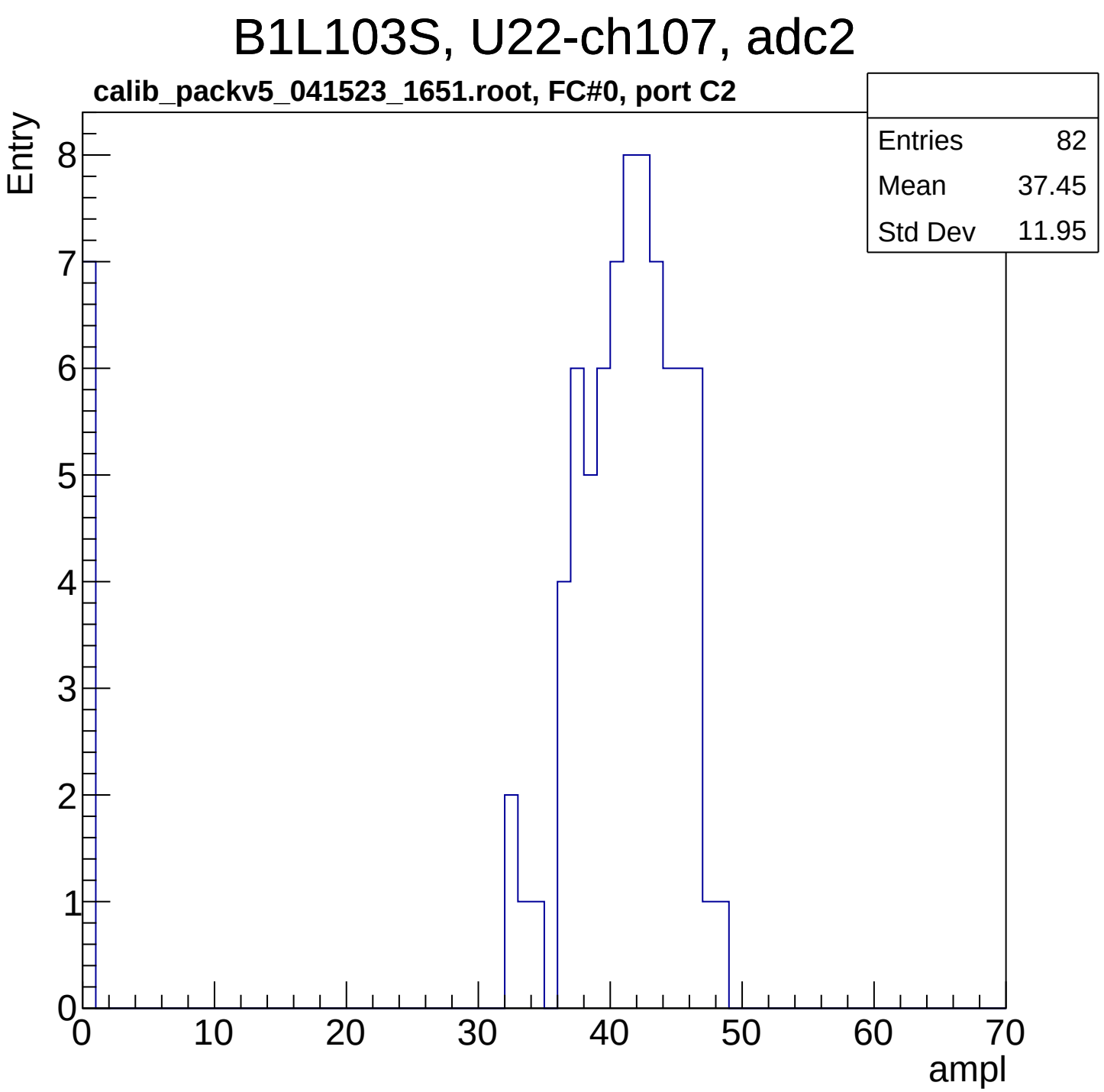
B1L103S, U22-ch107, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 37.45
Std Dev 11.95
Entry
ampl
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60
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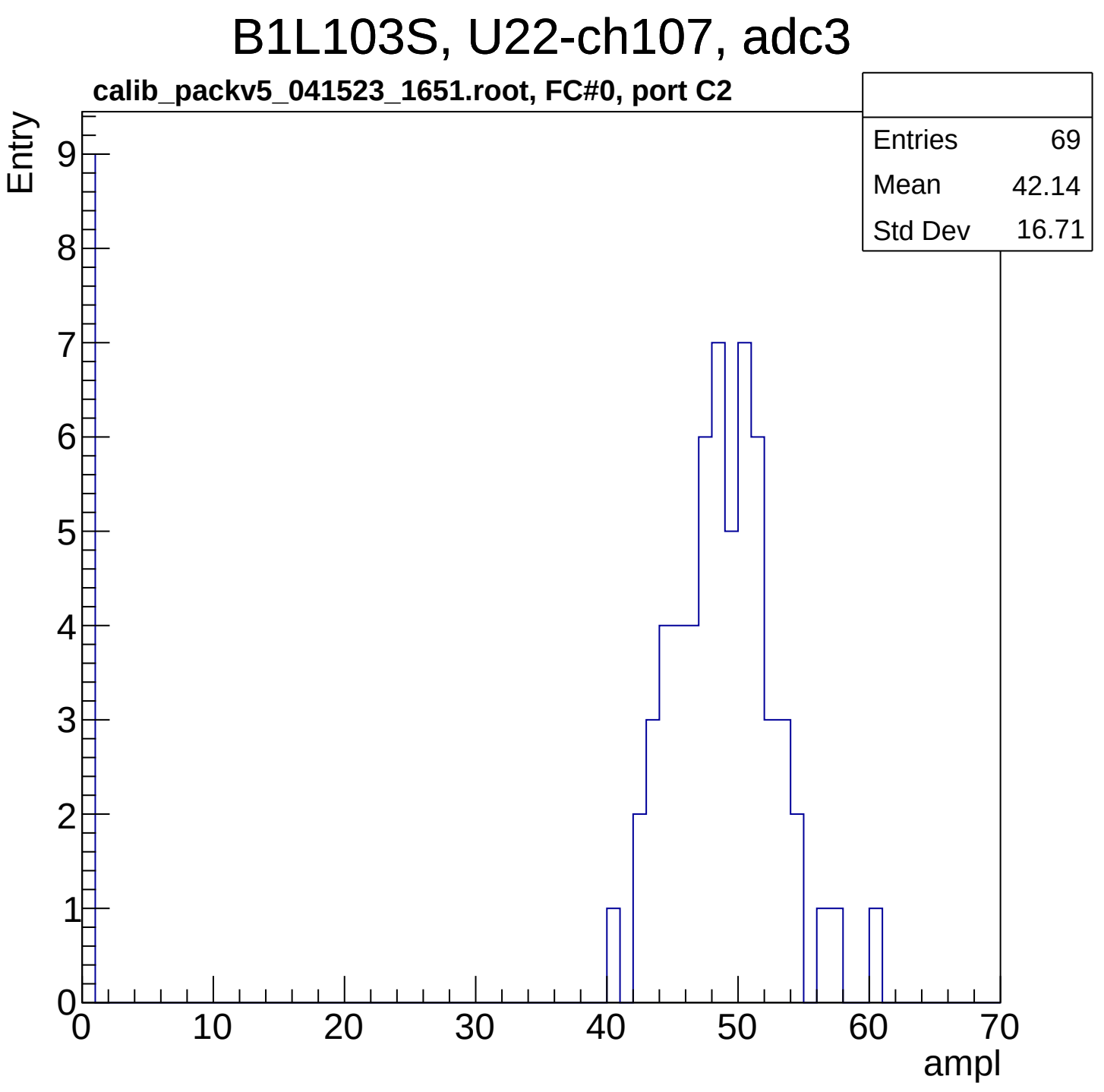
B1L103S, U22-ch107, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 42.14
Std Dev 16.71
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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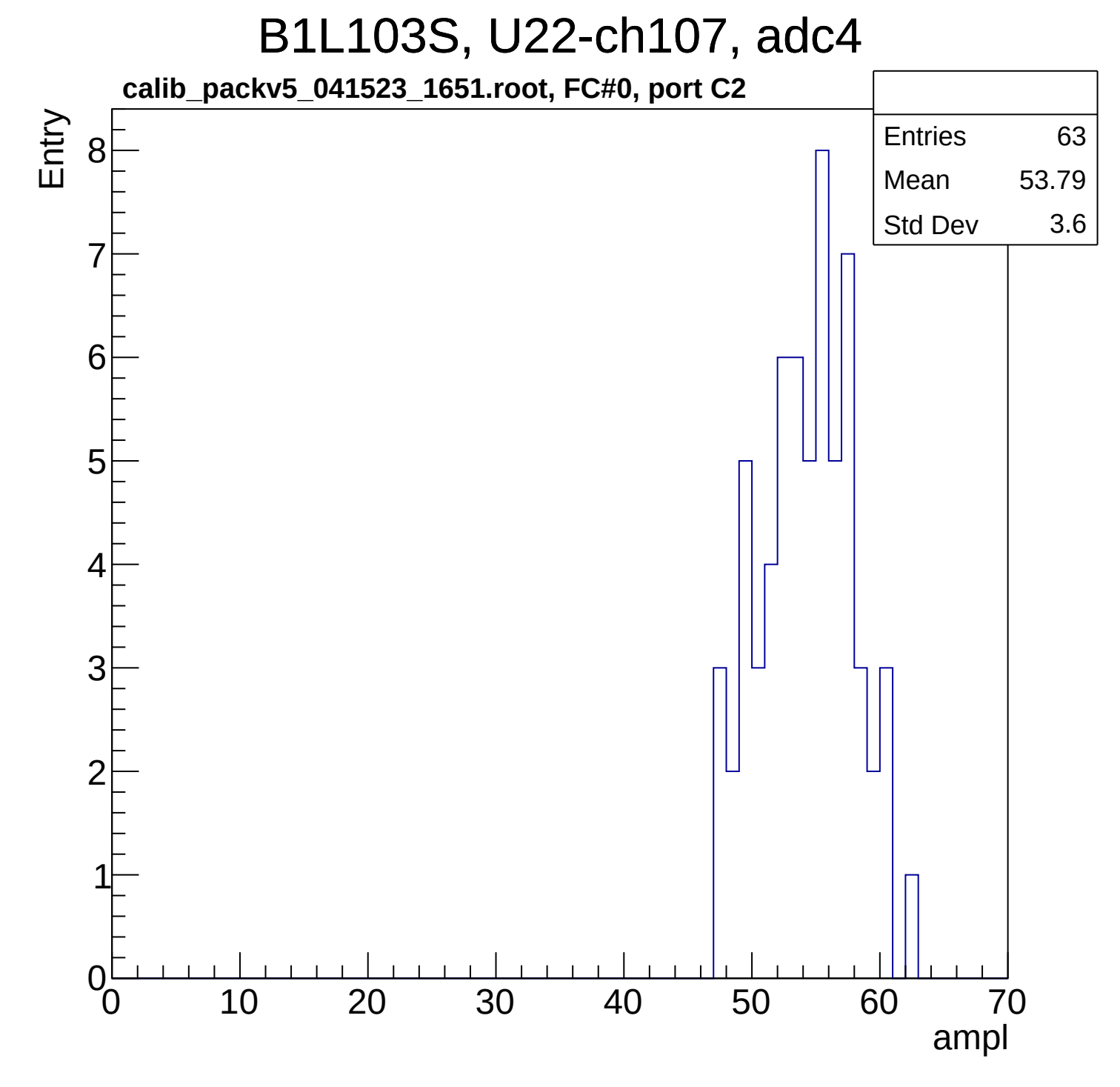
B1L103S, U22-ch107, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 53.79
Std Dev 3.6
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
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60
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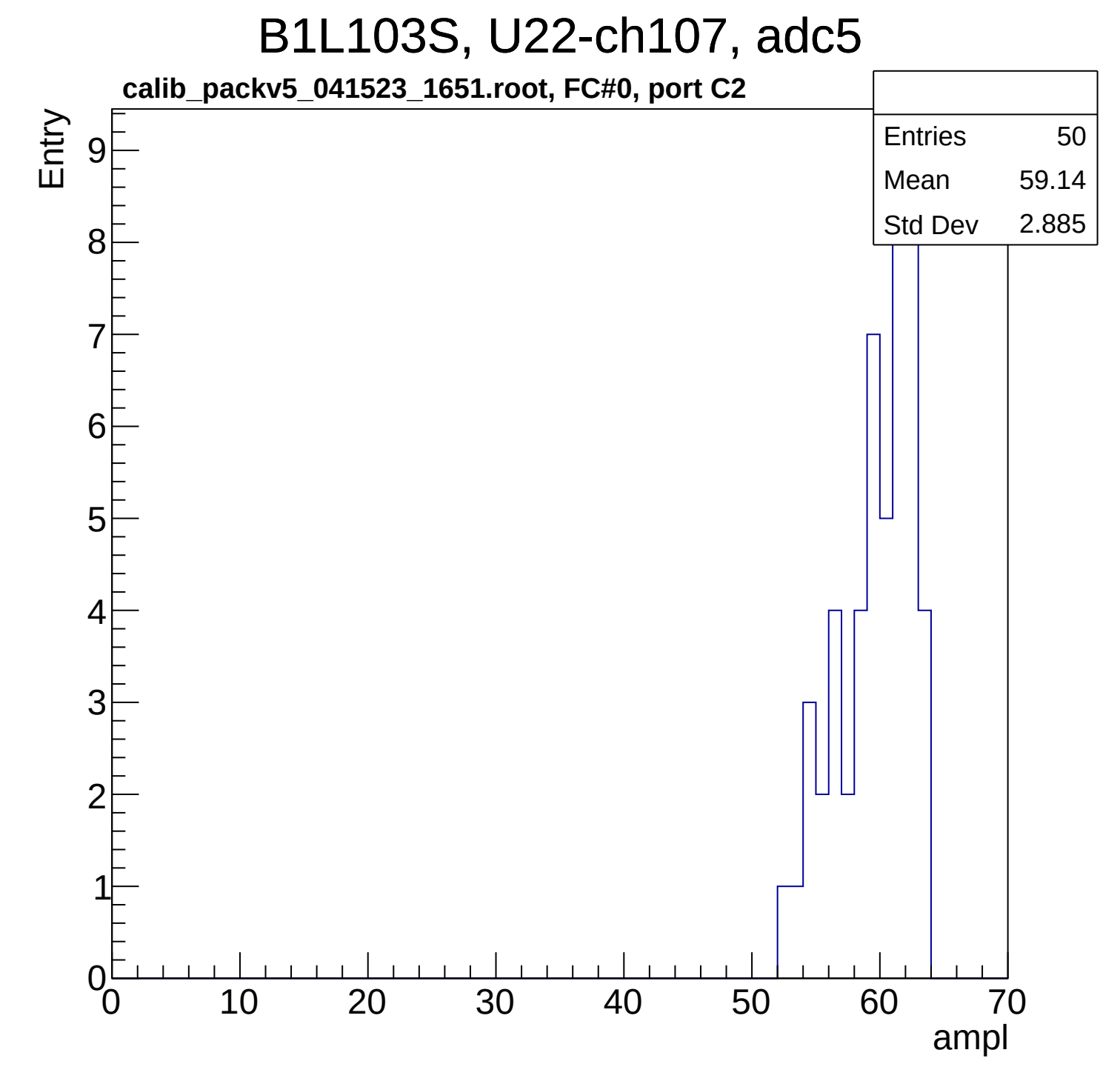
B1L103S, U22-ch107, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 59.14
Std Dev 2.885
Entry
ampl
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3
4
5
6
7
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0
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60
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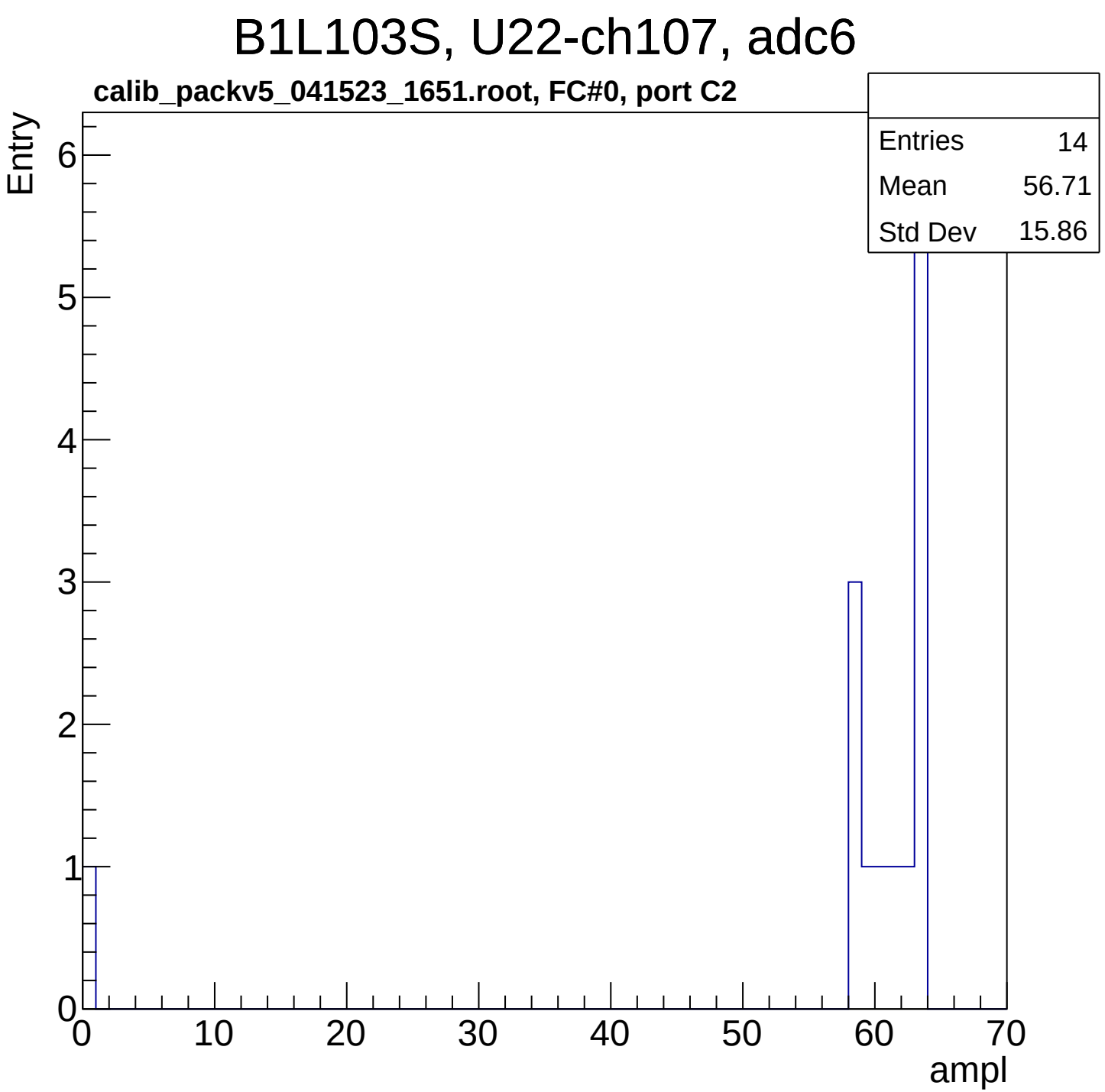
B1L103S, U22-ch107, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 56.71
Std Dev 15.86
Entry
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2
3
4
5
6
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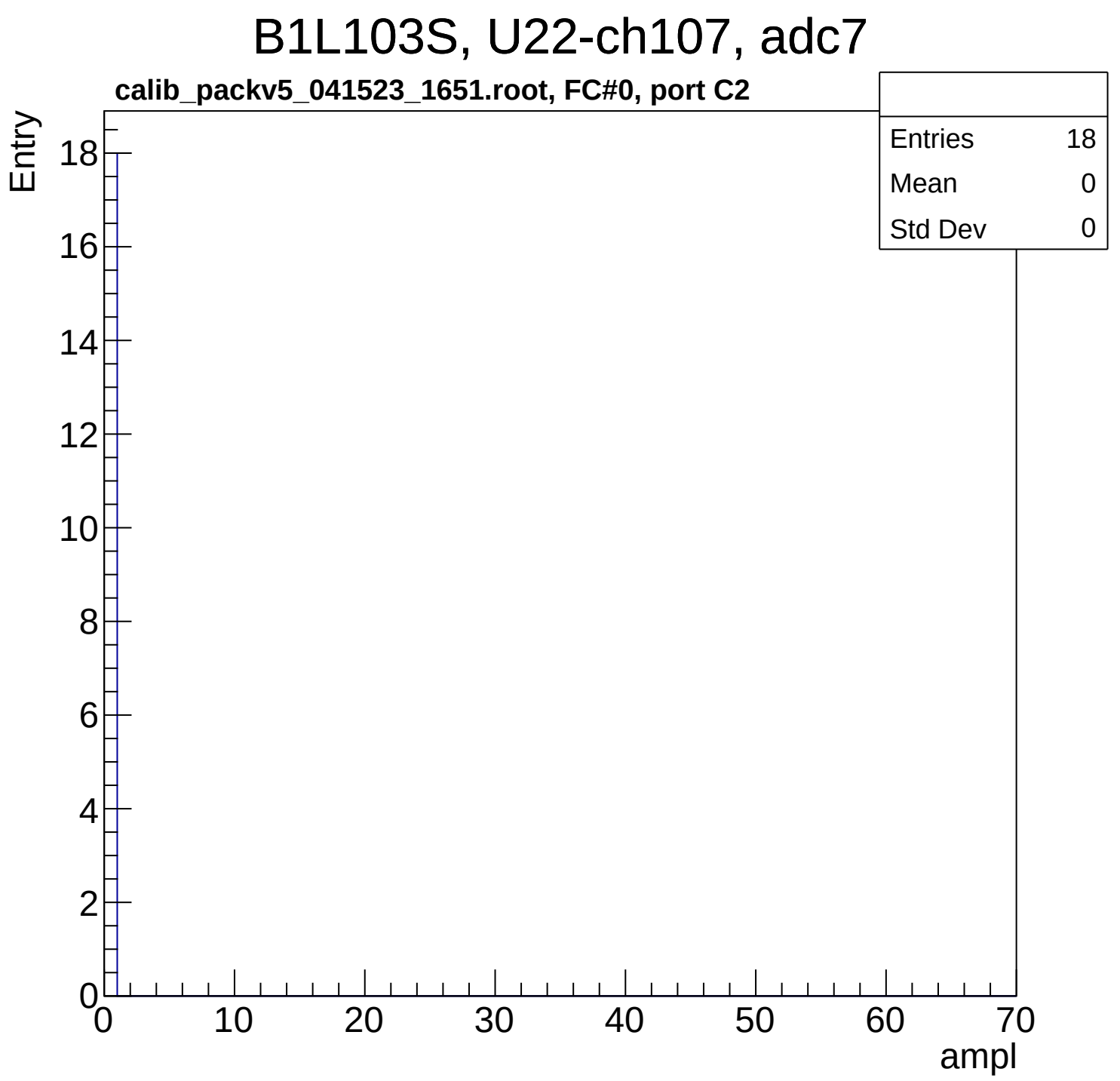
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch107, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
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6
8
10
12
14
16
18
0
10
20
30
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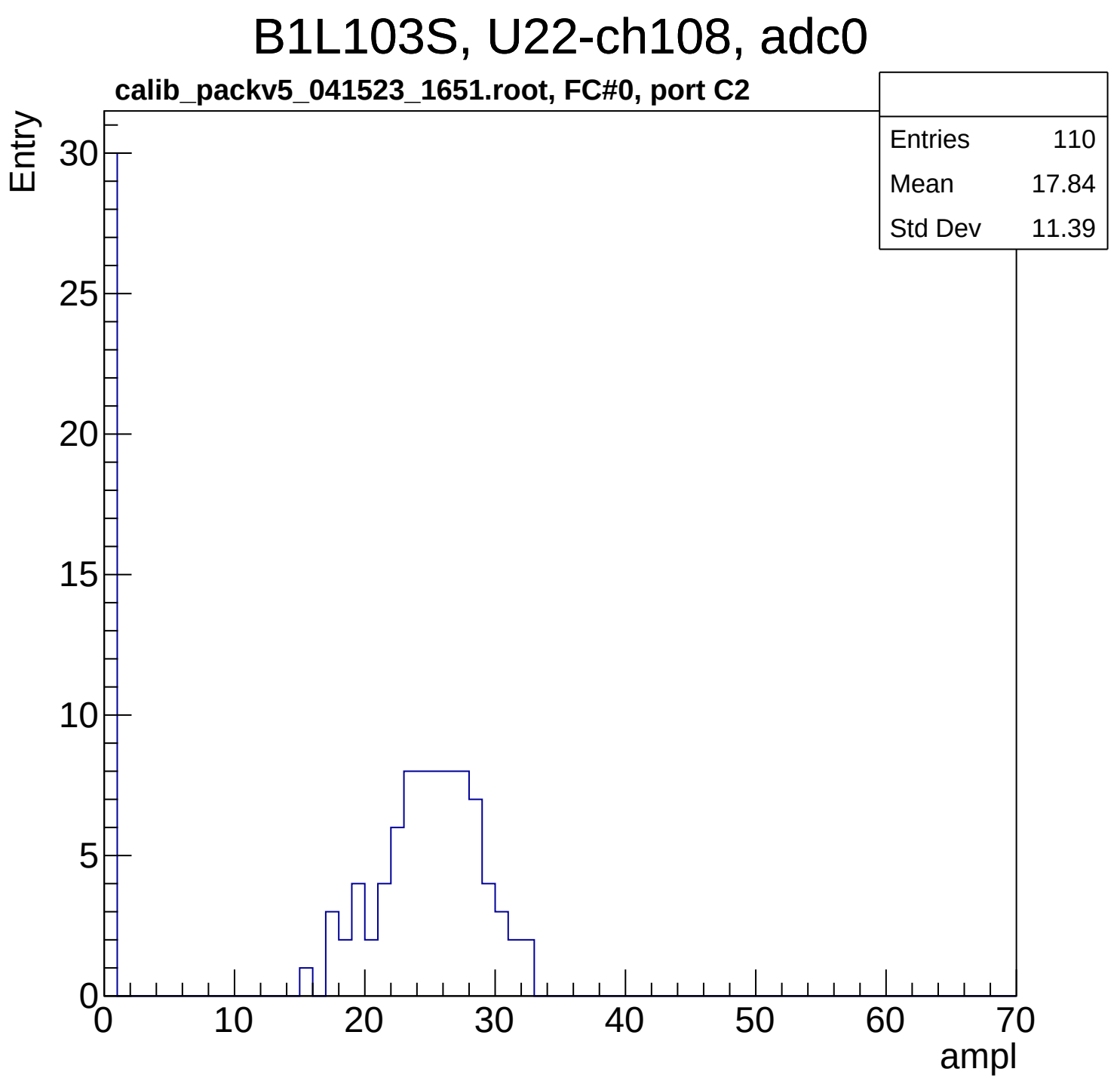
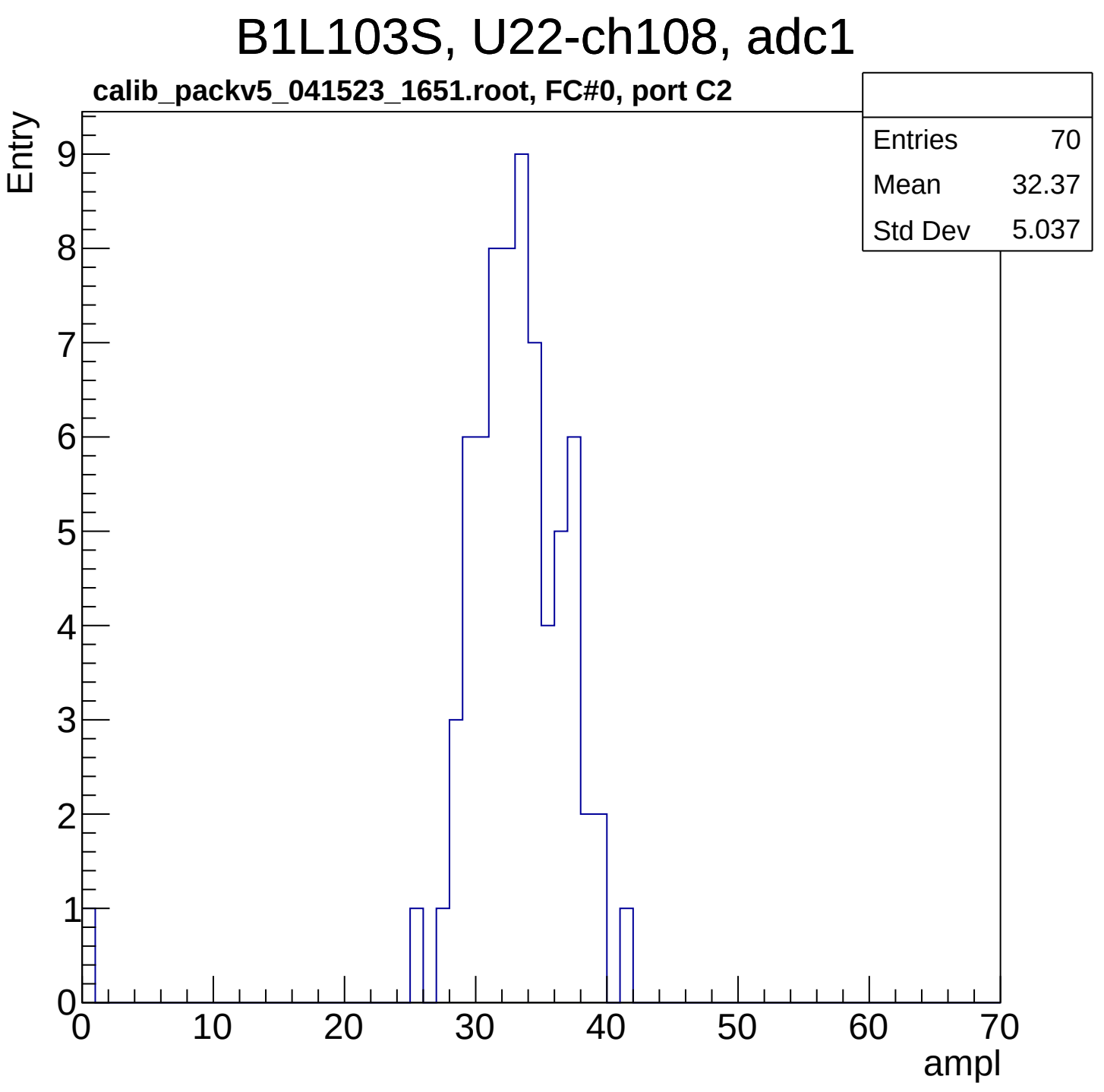
50
60
70
ampl


B1L103S, U22-ch108, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 110
Mean 17.84
Std Dev 11.39
Entry
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch108, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 32.37
Std Dev 5.037
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
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60
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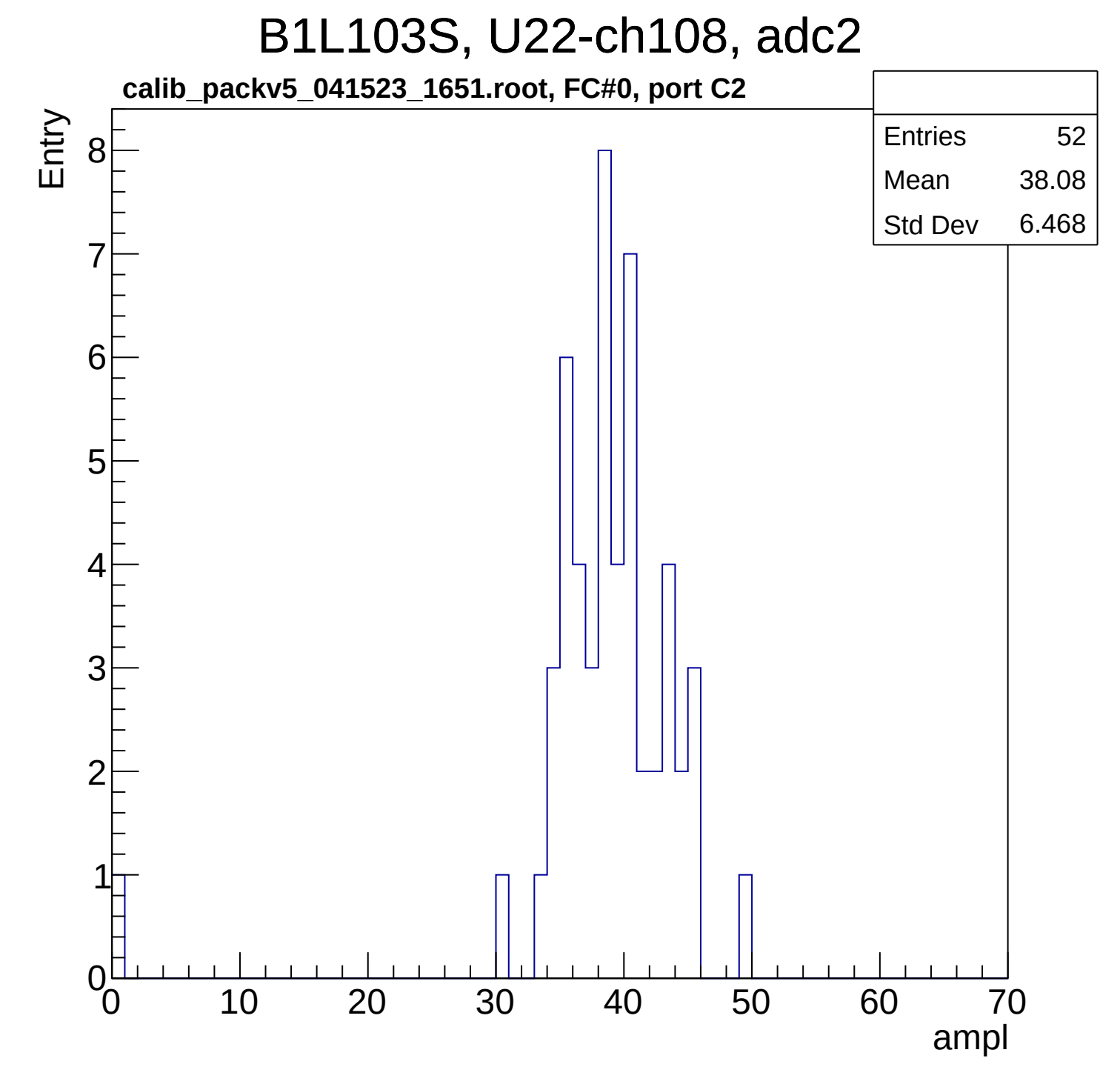
B1L103S, U22-ch108, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 38.08
Std Dev 6.468
Entry
ampl
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2
3
4
5
6
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0
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60
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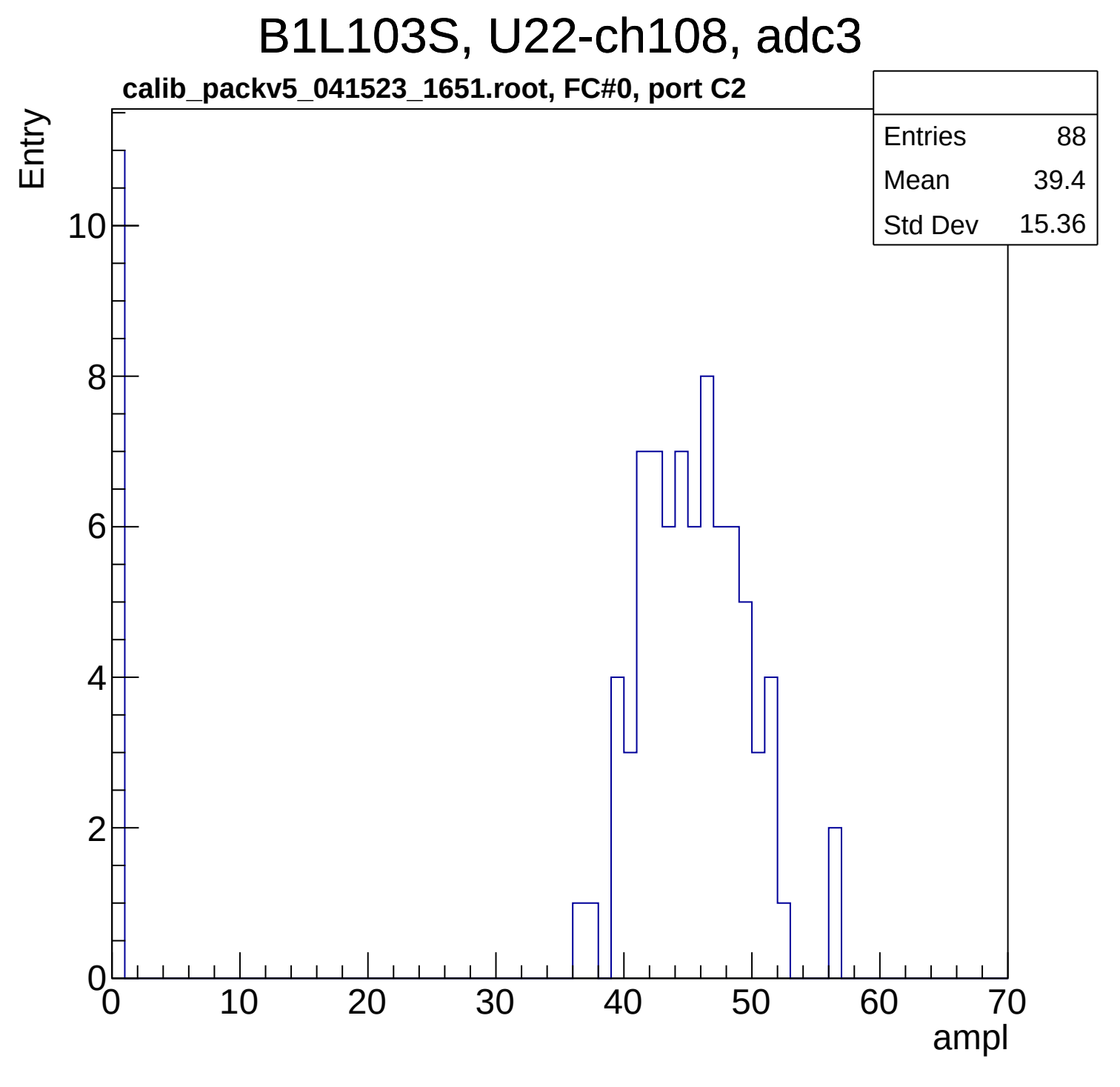
B1L103S, U22-ch108, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 39.4
Std Dev 15.36
Entry
ampl
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4
6
8
10
0
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20
30
40
50
60
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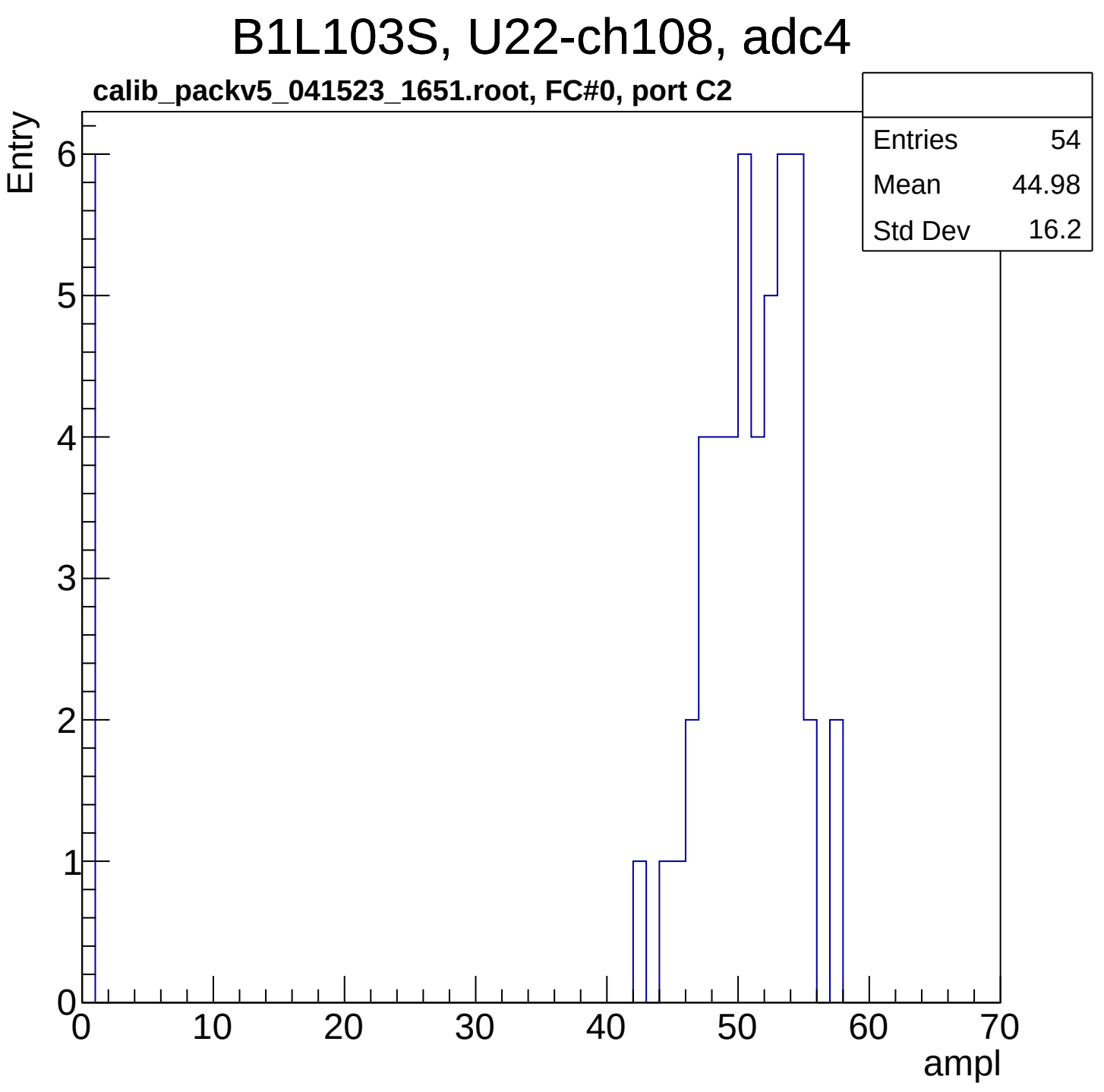
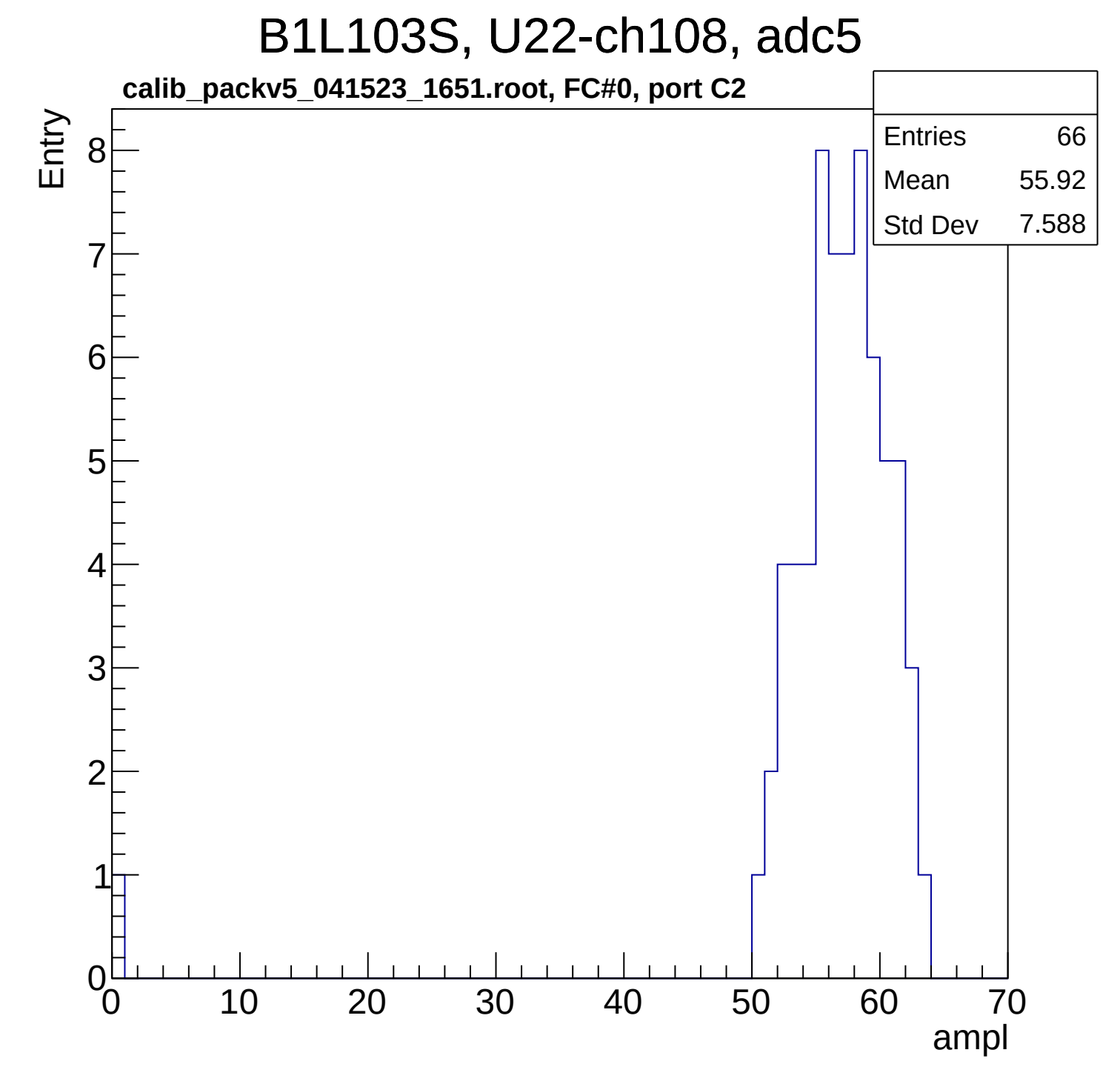

B1L103S, U22-ch108, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 44.98
Std Dev 16.2
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch108, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 55.92
Std Dev 7.588
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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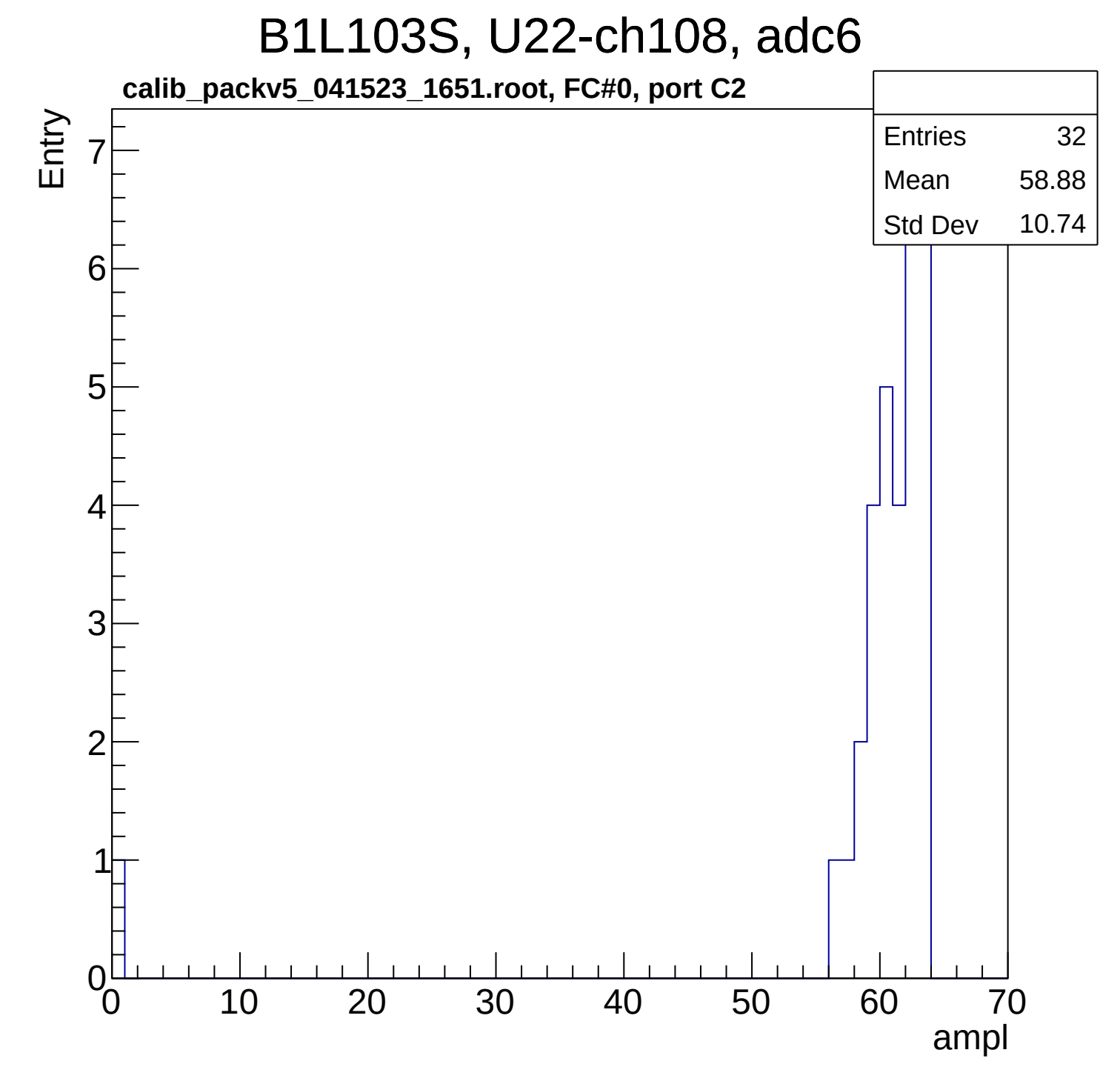
B1L103S, U22-ch108, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 58.88
Std Dev 10.74
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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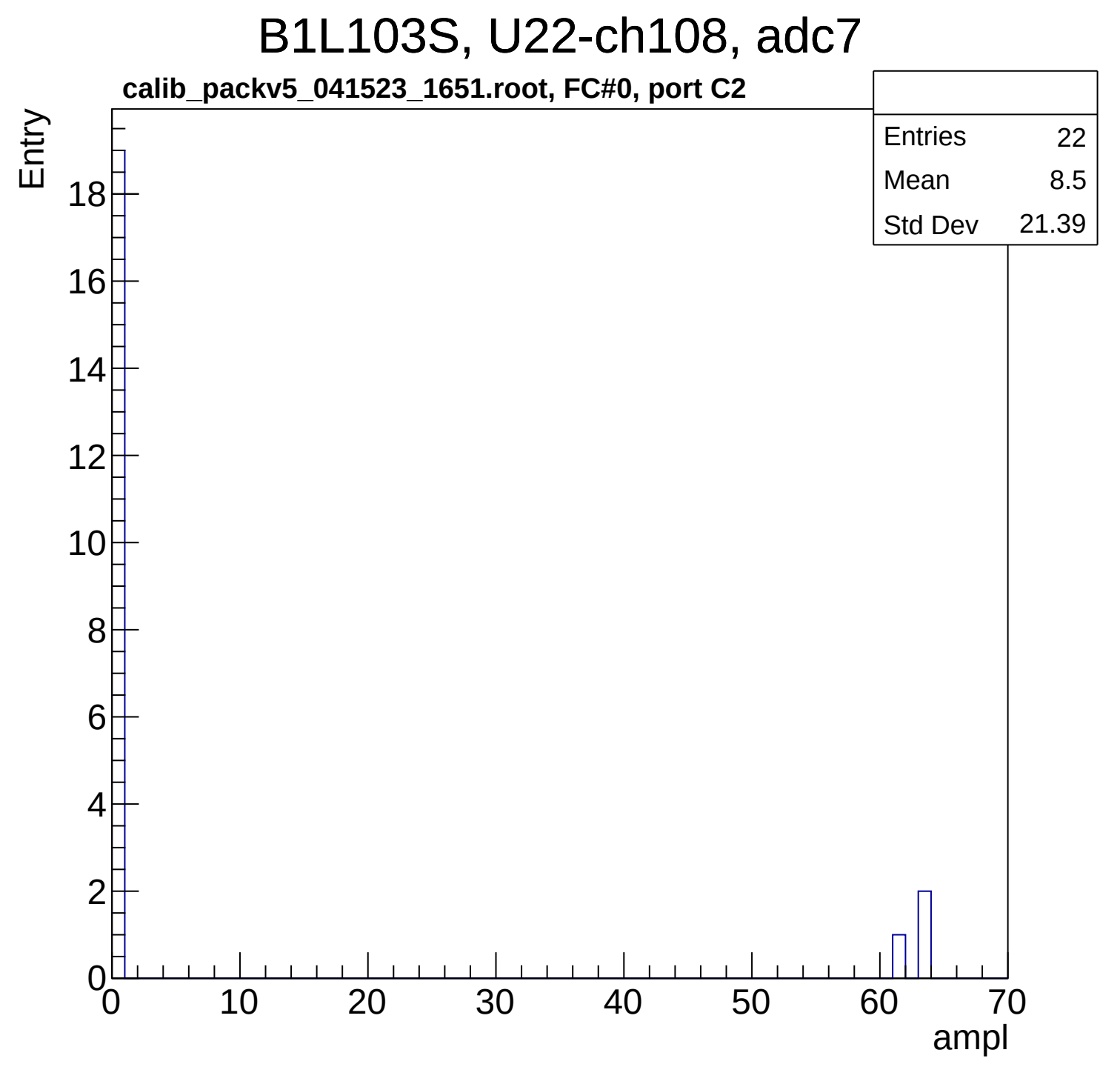
B1L103S, U22-ch108, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.5
Std Dev 21.39
Entry
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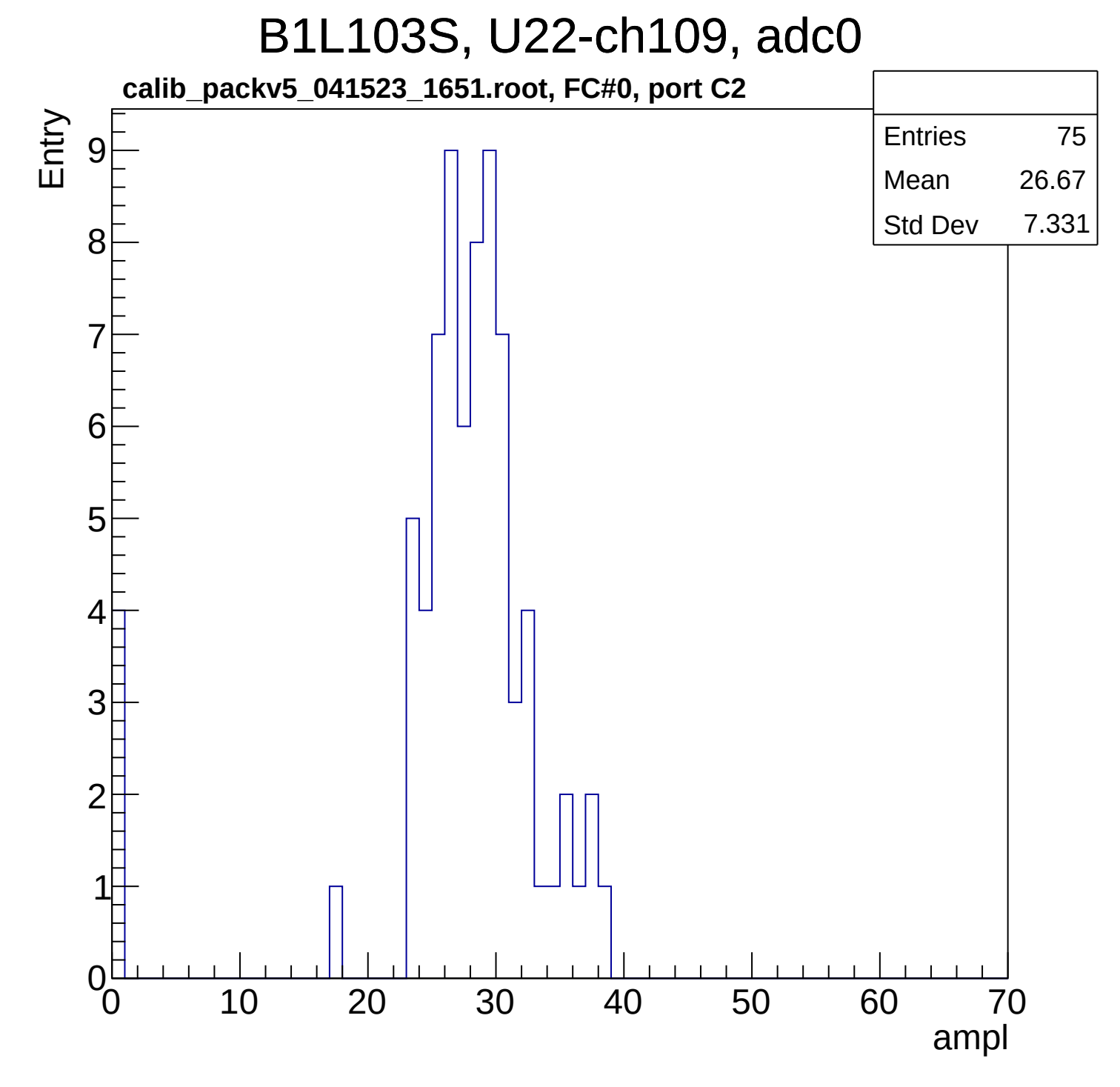
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch109, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 26.67
Std Dev 7.331
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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60
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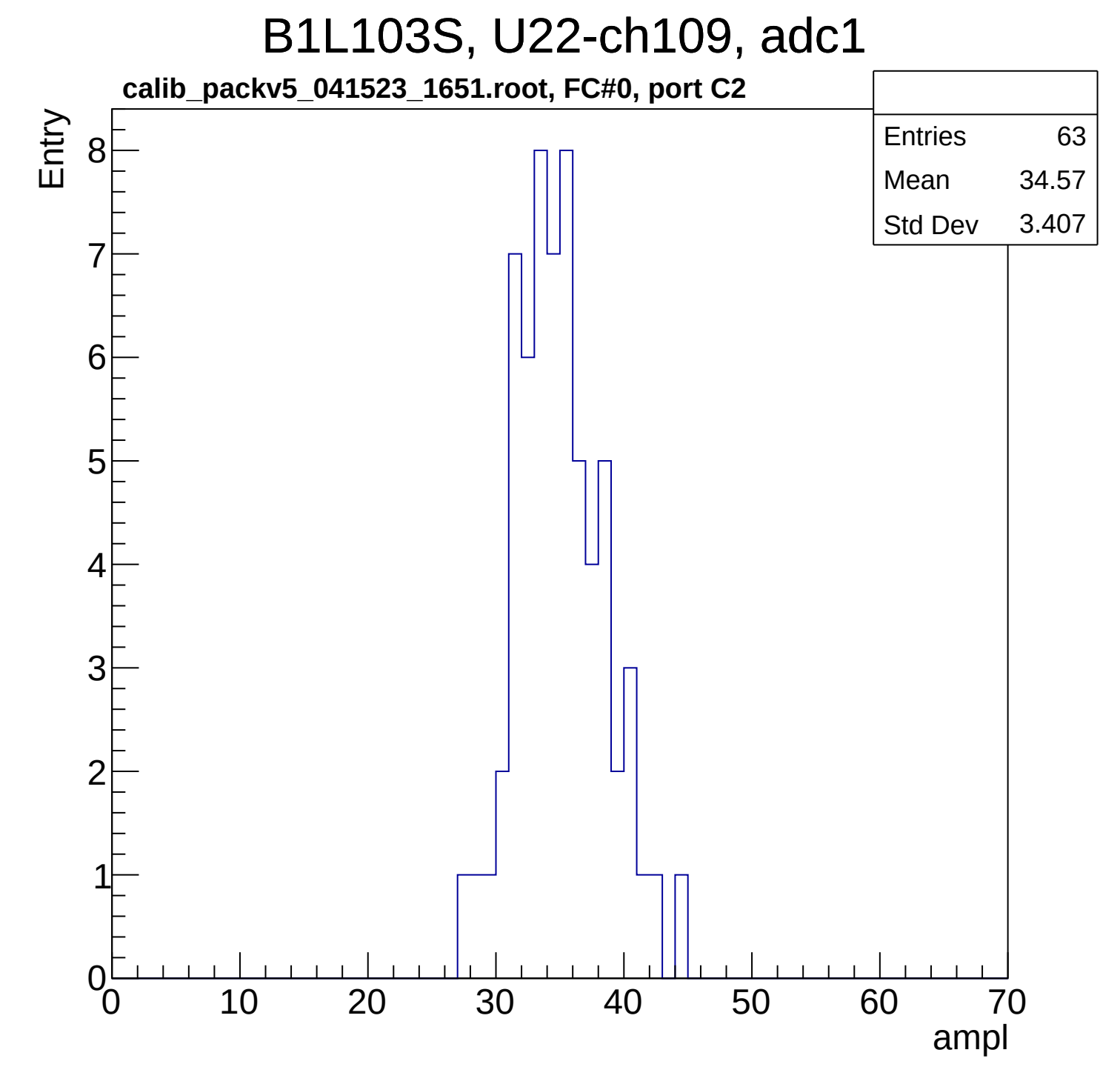
B1L103S, U22-ch109, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 34.57
Std Dev 3.407
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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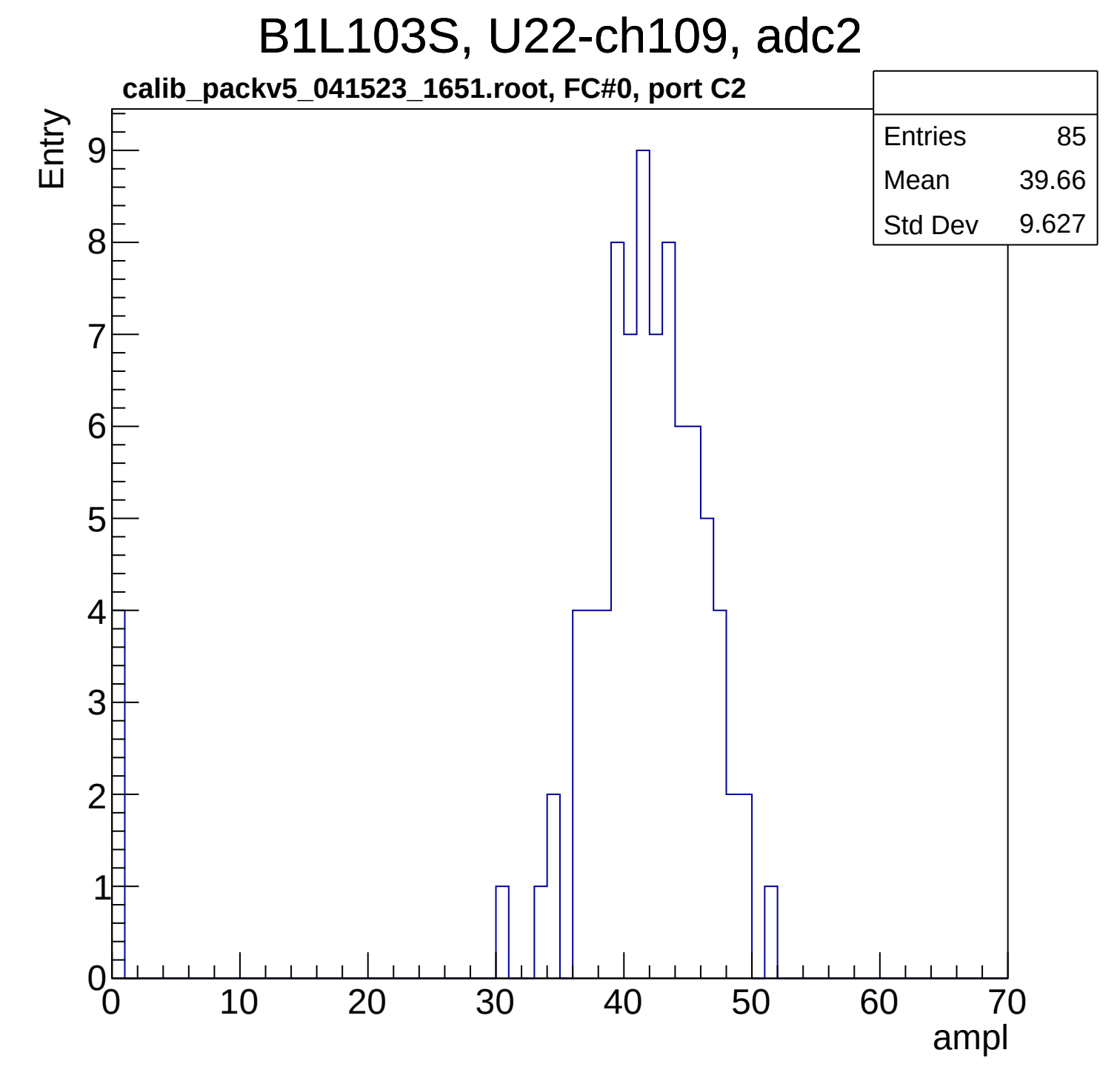
B1L103S, U22-ch109, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 39.66
Std Dev 9.627
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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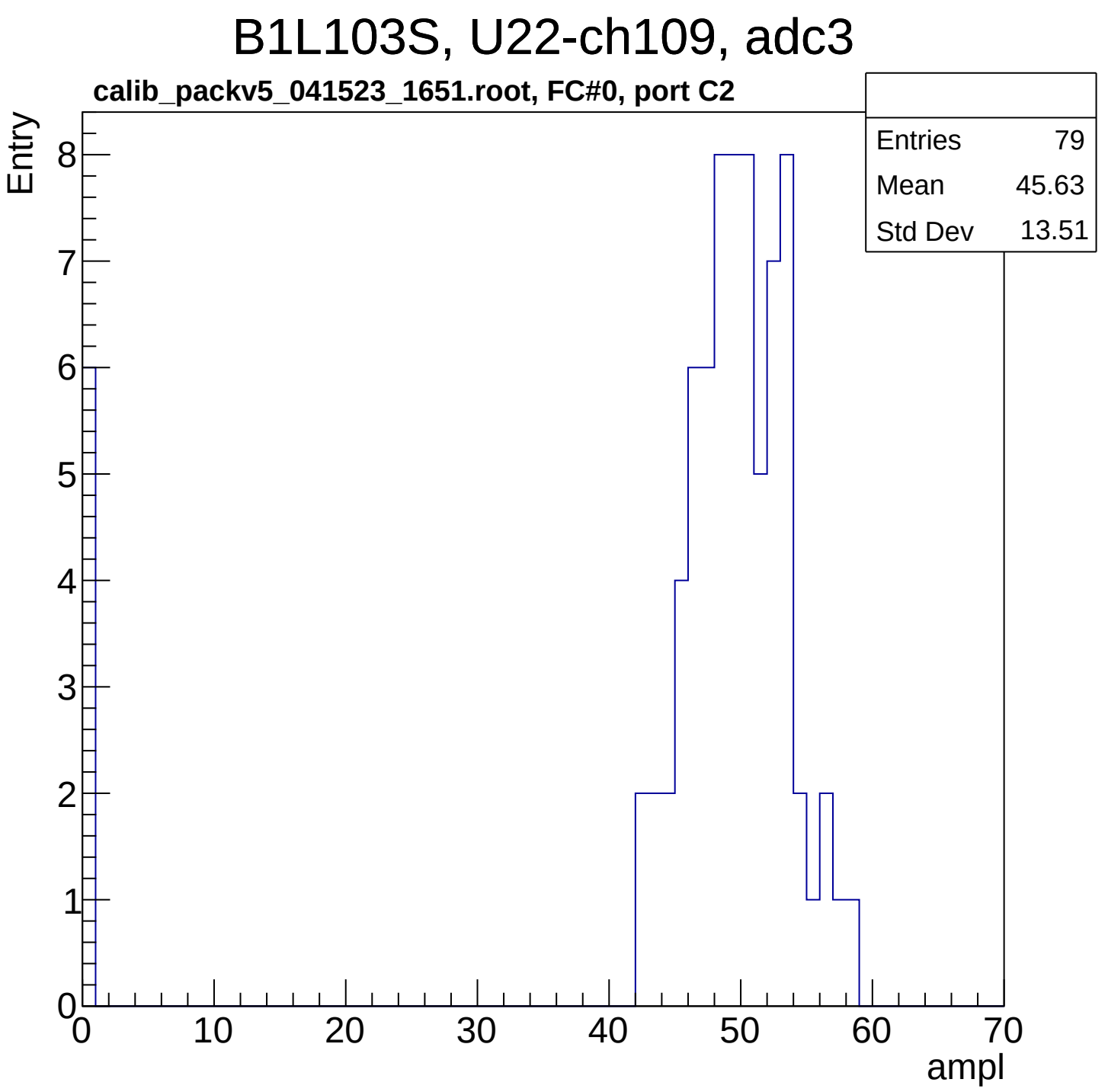
B1L103S, U22-ch109, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 45.63
Std Dev 13.51
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
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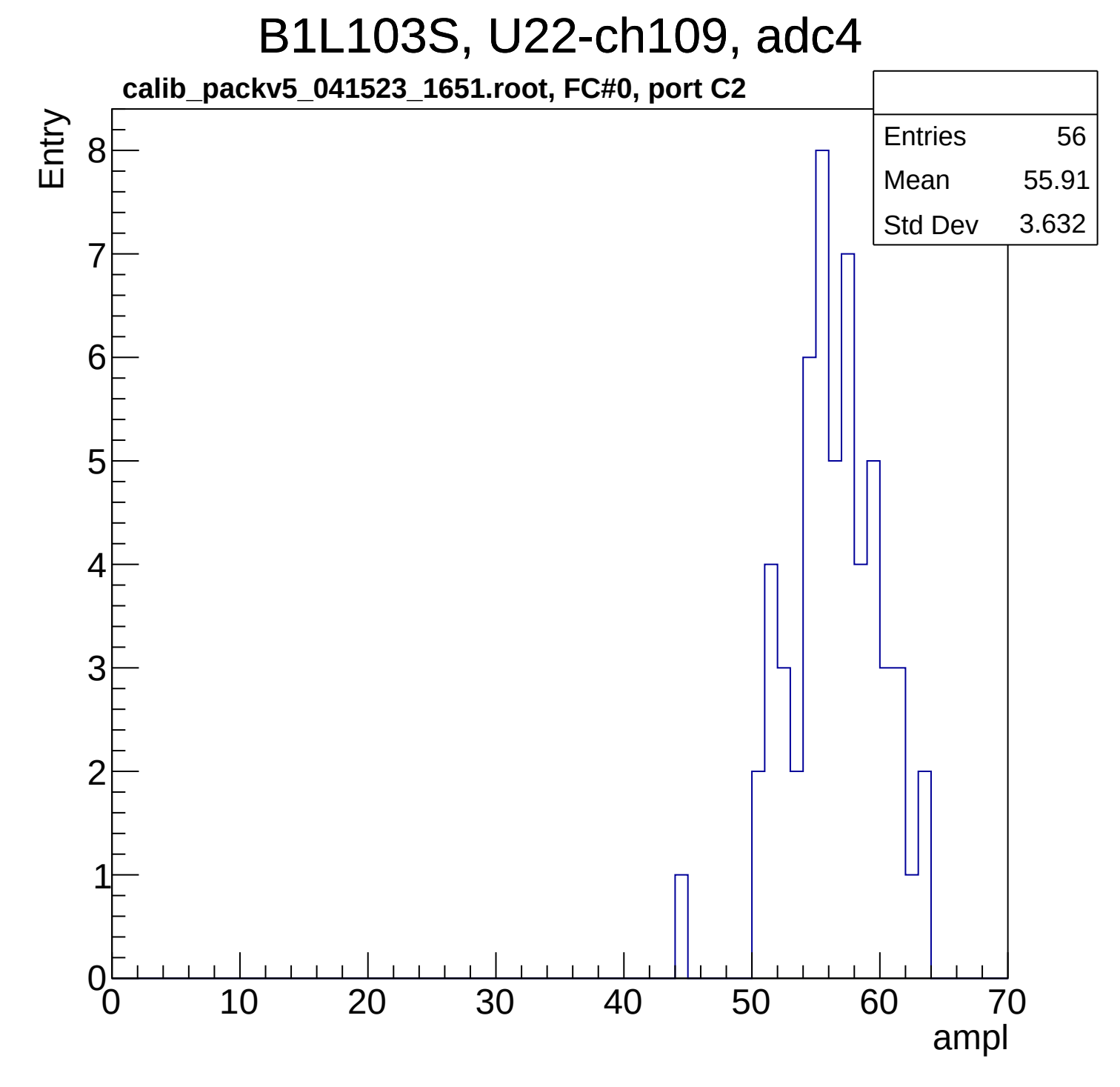
60
70


B1L103S, U22-ch109, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 55.91
Std Dev 3.632
Entry
ampl
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2
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4
5
6
7
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0
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40
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60
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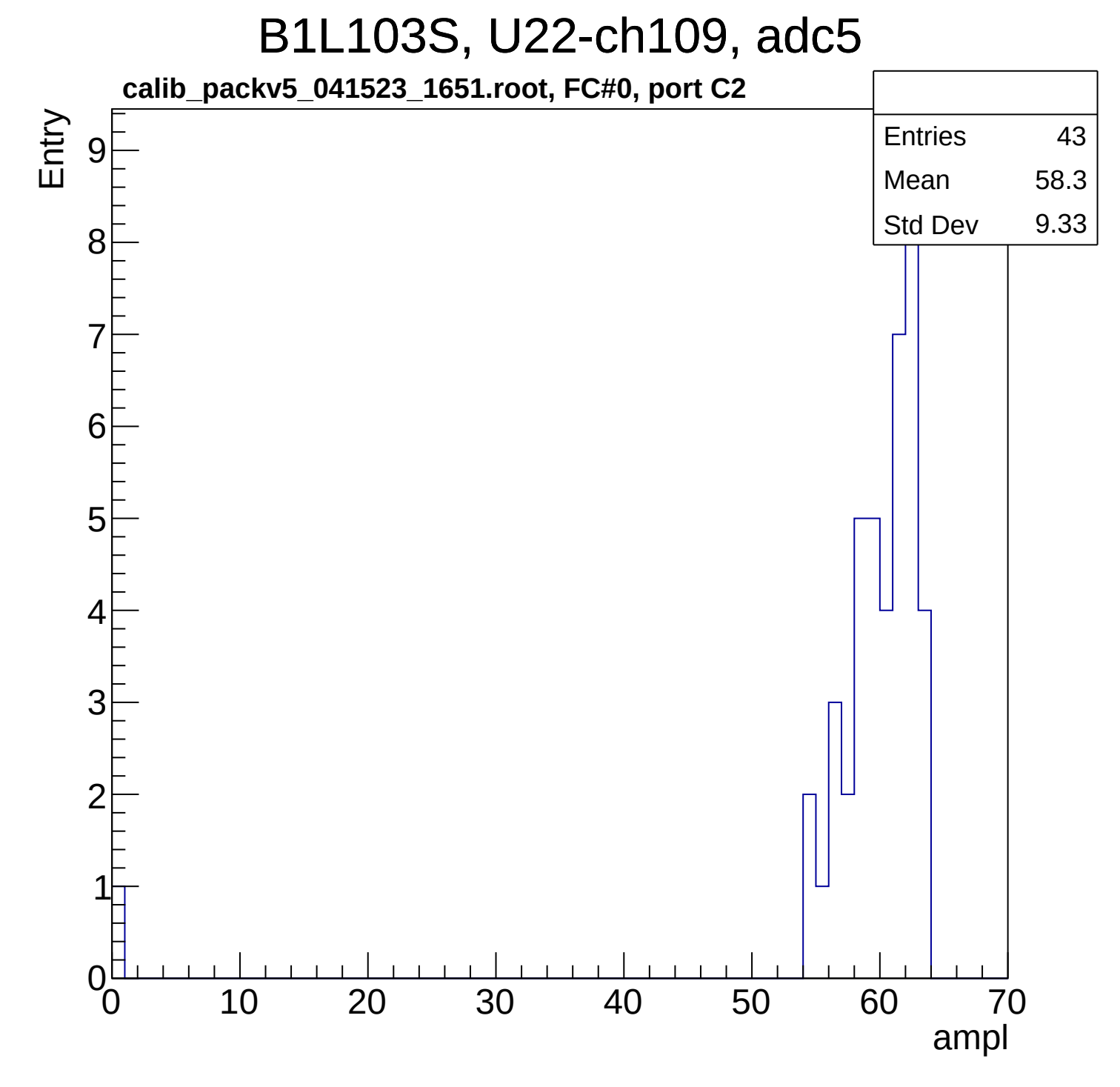
B1L103S, U22-ch109, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 58.3
Std Dev 9.33
Entry
ampl
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2
3
4
5
6
7
8
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0
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40
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60
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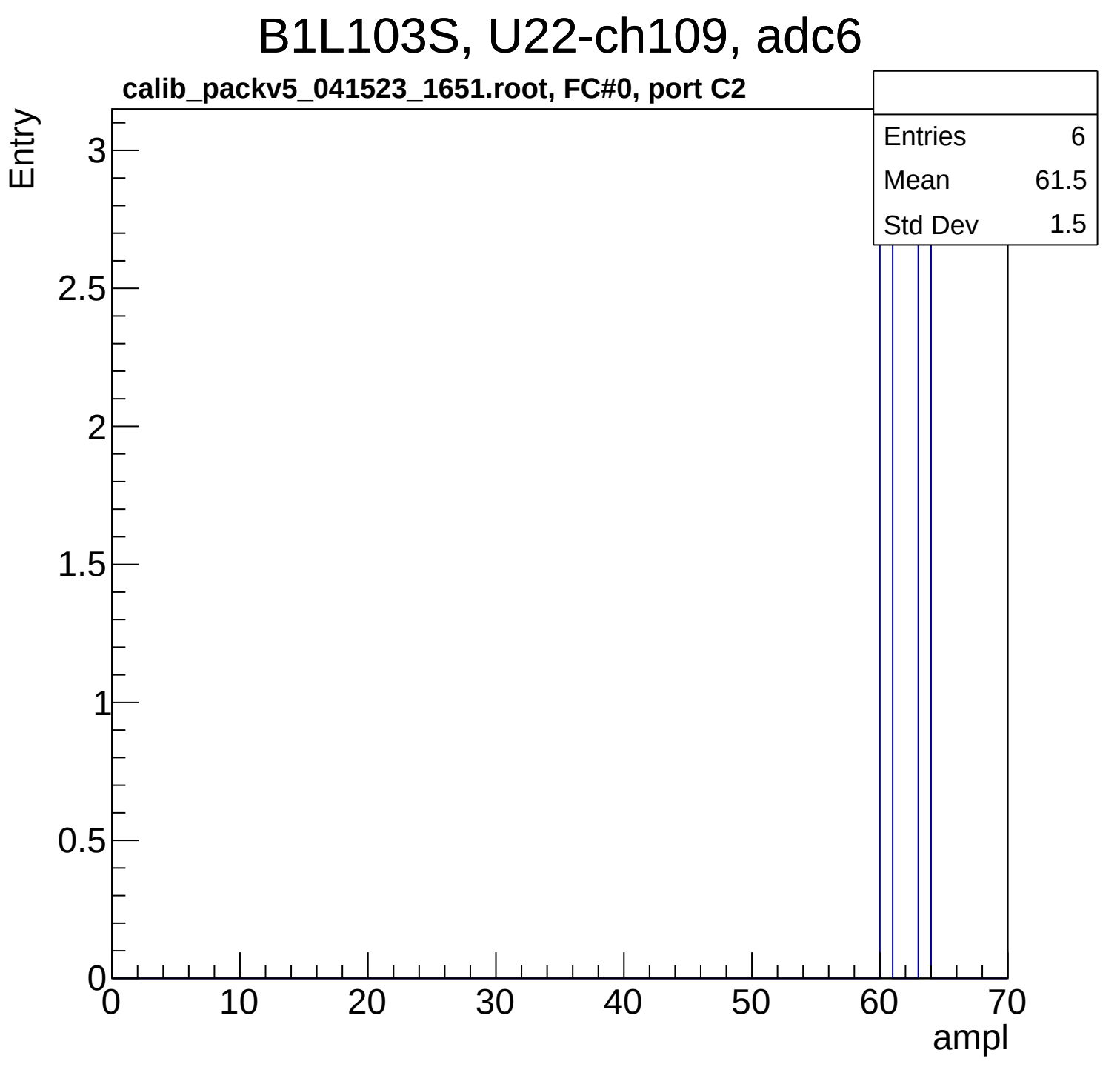
B1L103S, U22-ch109, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 61.5
Std Dev 1.5
Entry
ampl
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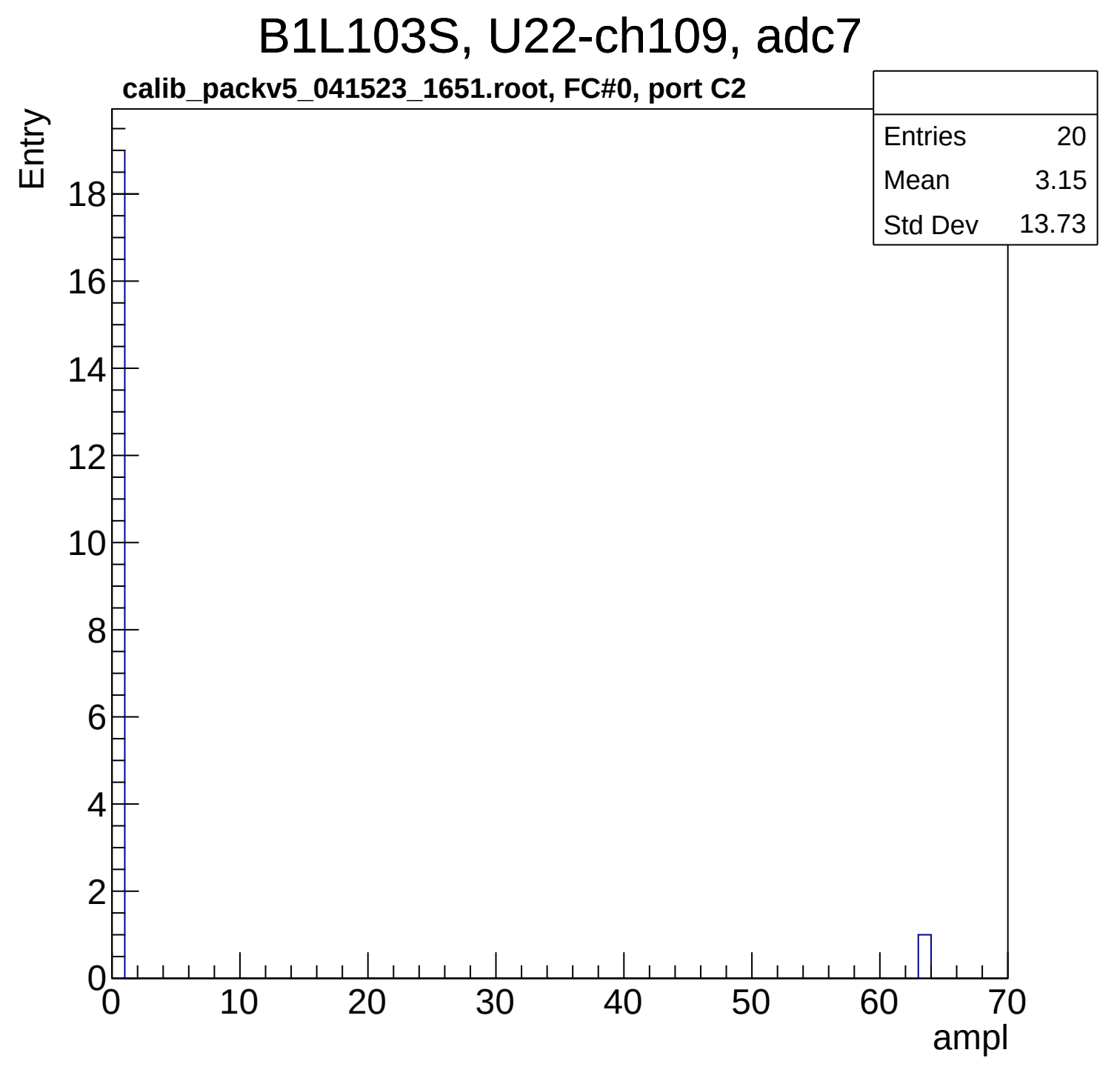
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U22-ch109, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
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6
8
10
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14
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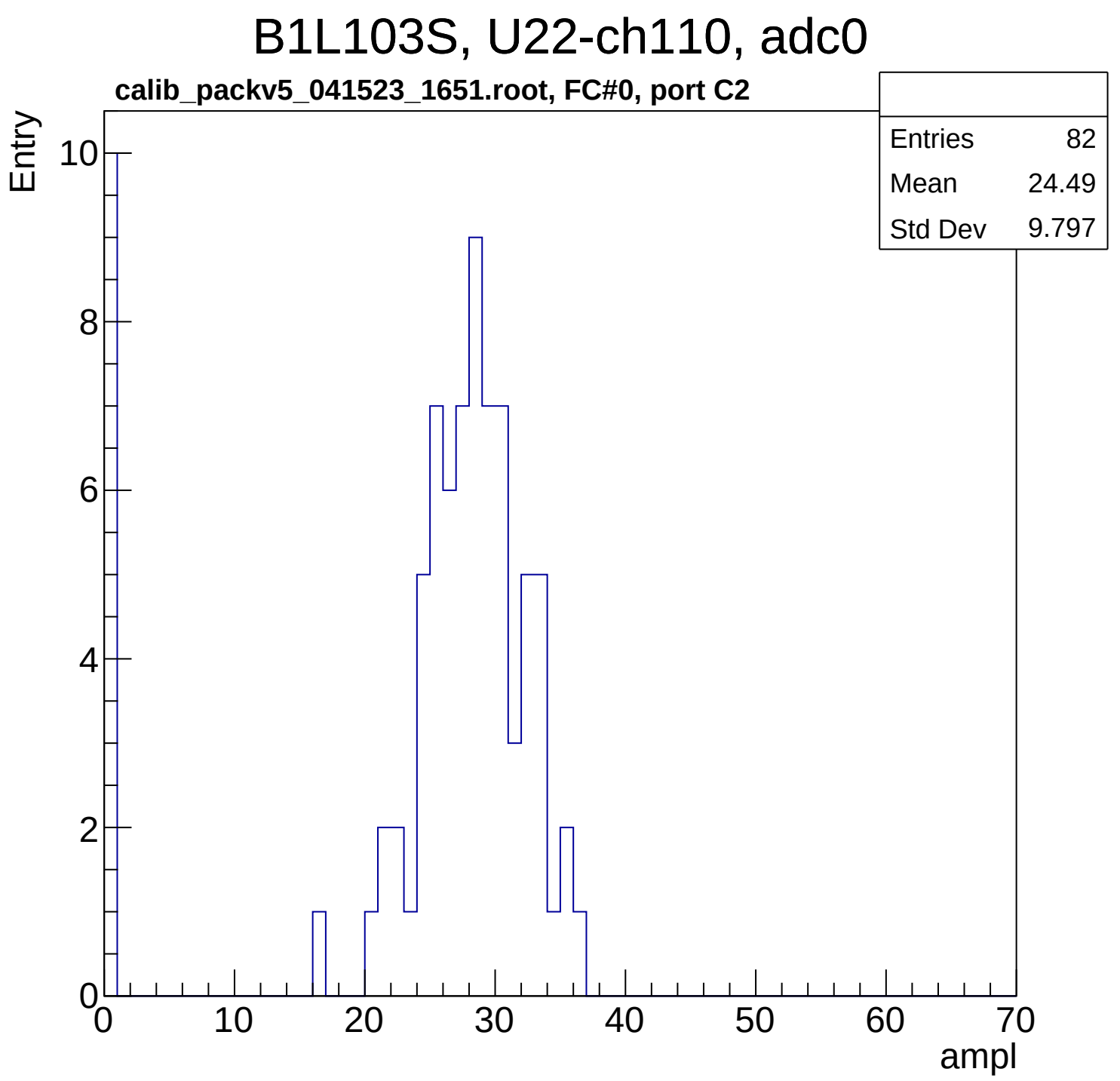
50
60
70
ampl


B1L103S, U22-ch110, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 24.49
Std Dev 9.797
Entry
ampl
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0
10
20
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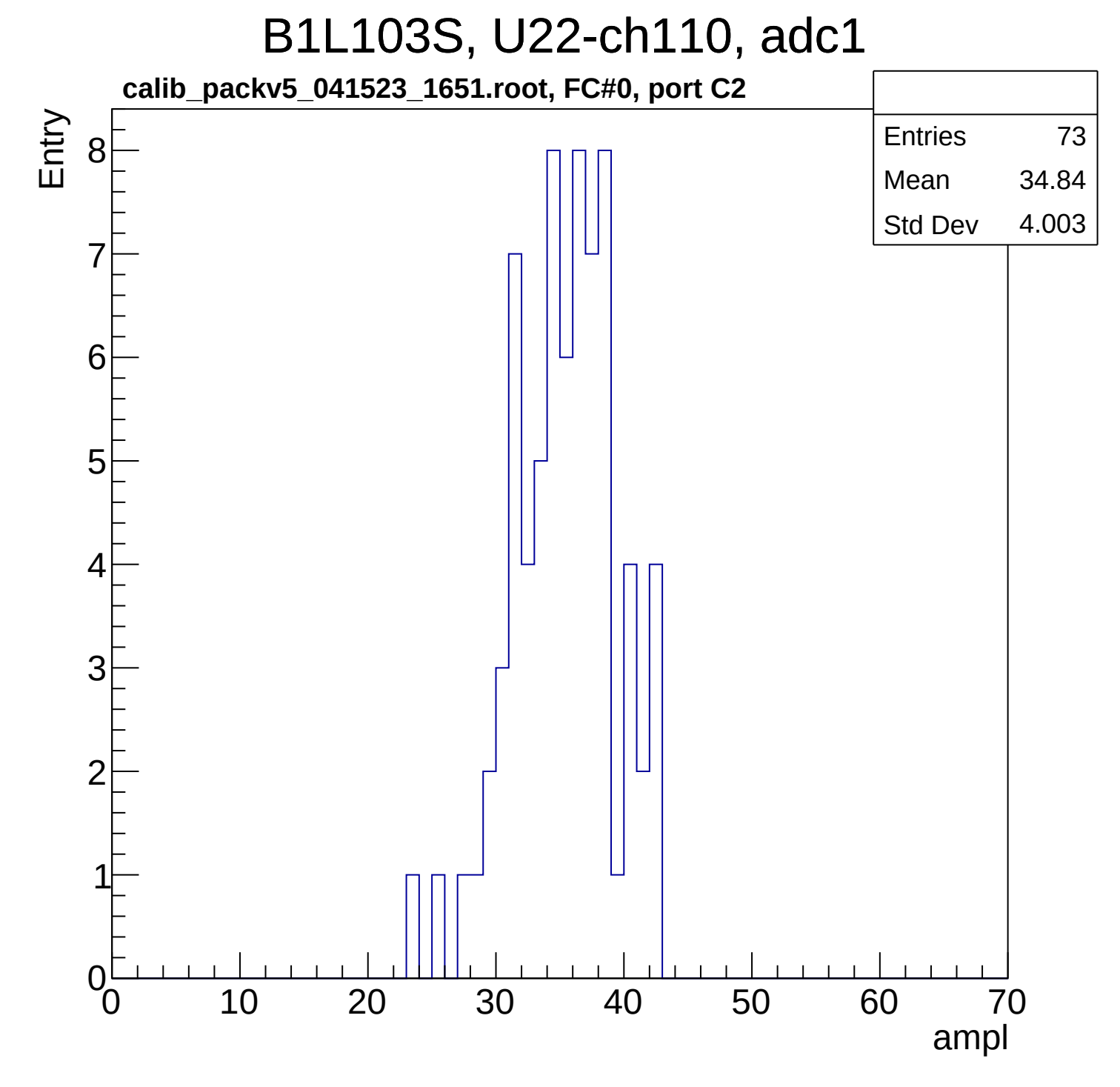
40
50
60
70


B1L103S, U22-ch110, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 34.84
Std Dev 4.003
Entry
ampl
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2
3
4
5
6
7
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0
10
20
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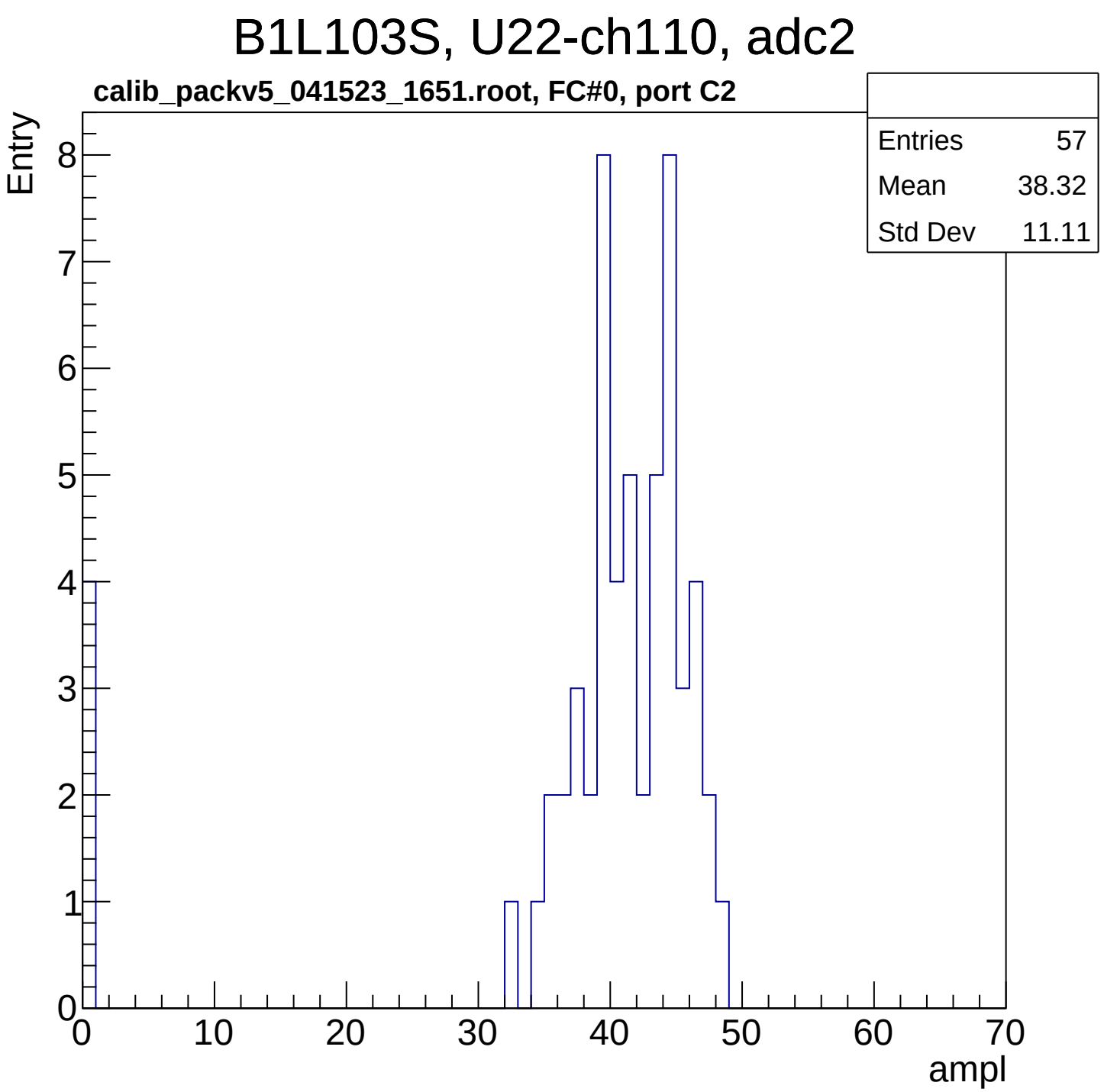
40
50
60
70


B1L103S, U22-ch110, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 38.32
Std Dev 11.11
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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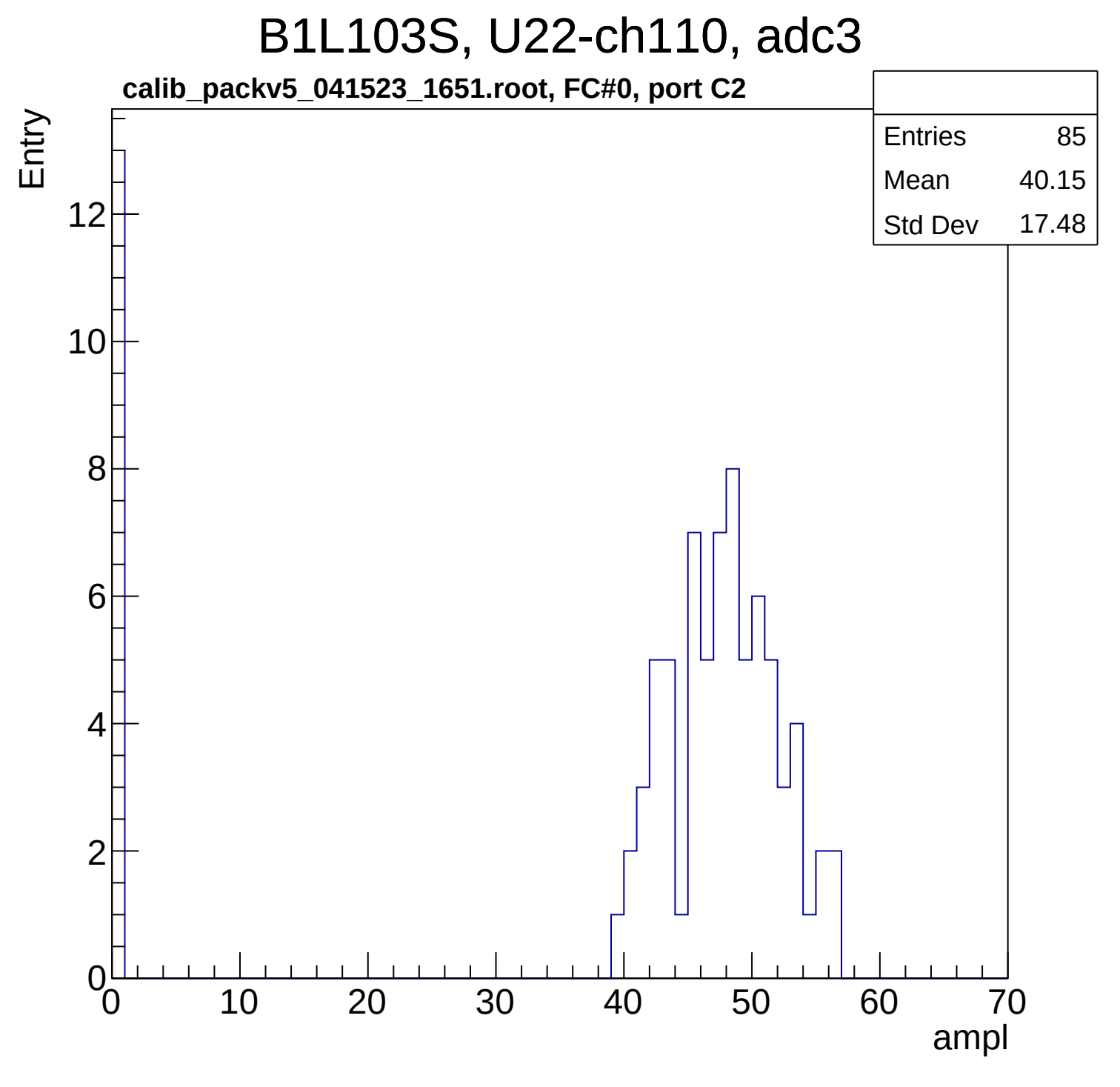
40
50
60
70


B1L103S, U22-ch110, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 40.15
Std Dev 17.48
Entry
0
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12
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30
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50
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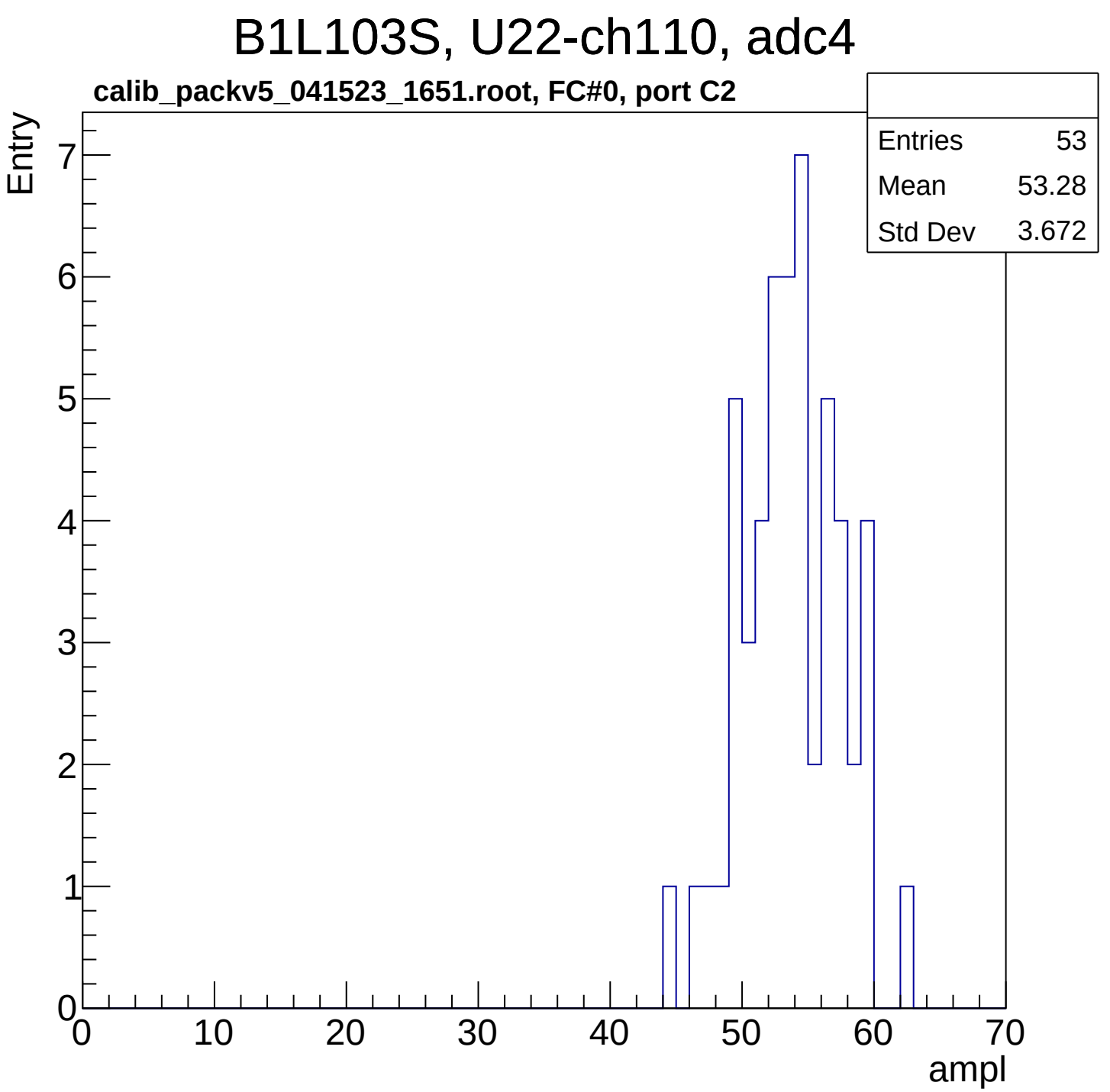
70
ampl


B1L103S, U22-ch110, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 53.28
Std Dev 3.672
Entry
ampl
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0
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40
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60
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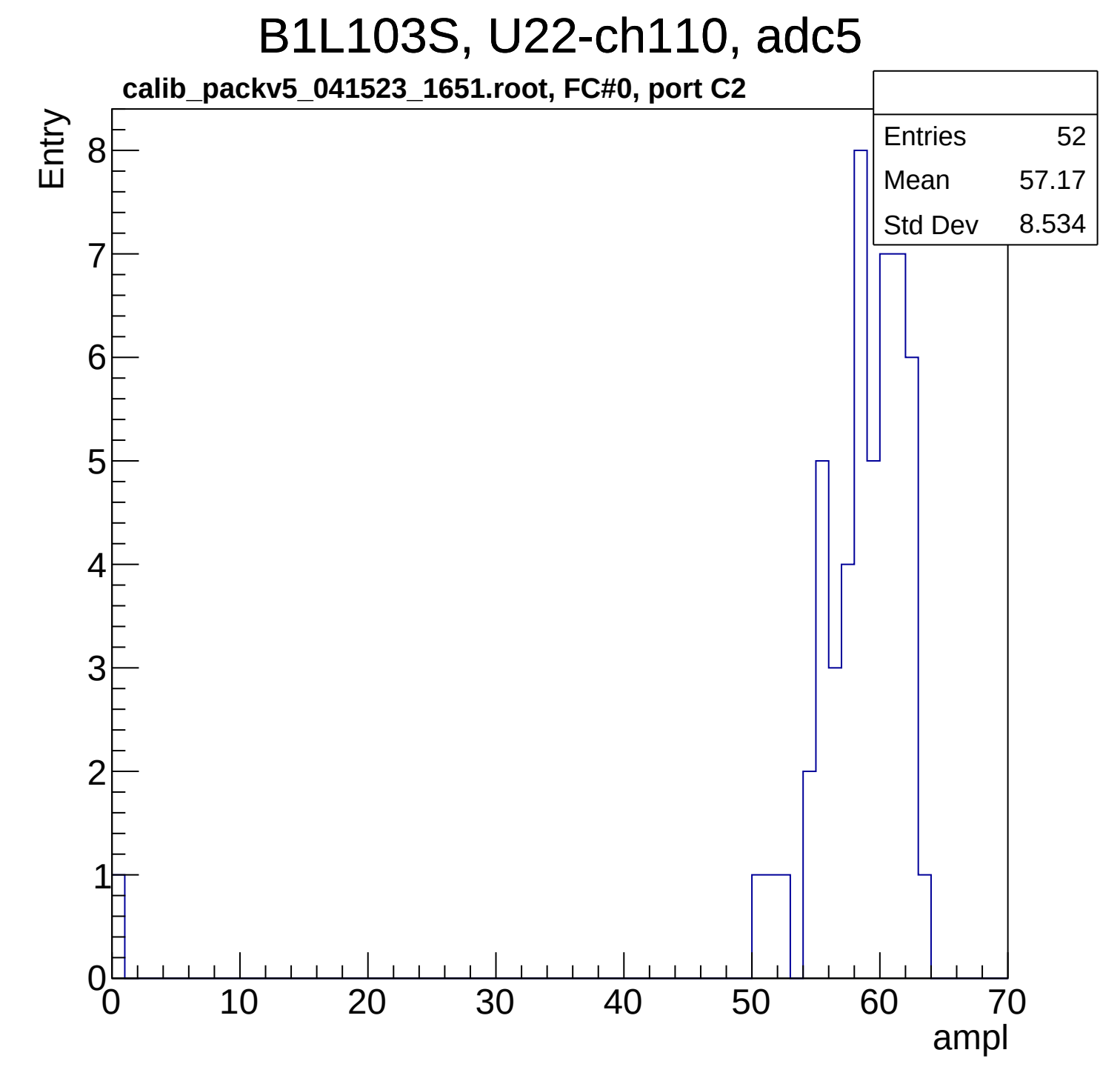
B1L103S, U22-ch110, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 57.17
Std Dev 8.534
Entry
ampl
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0
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60
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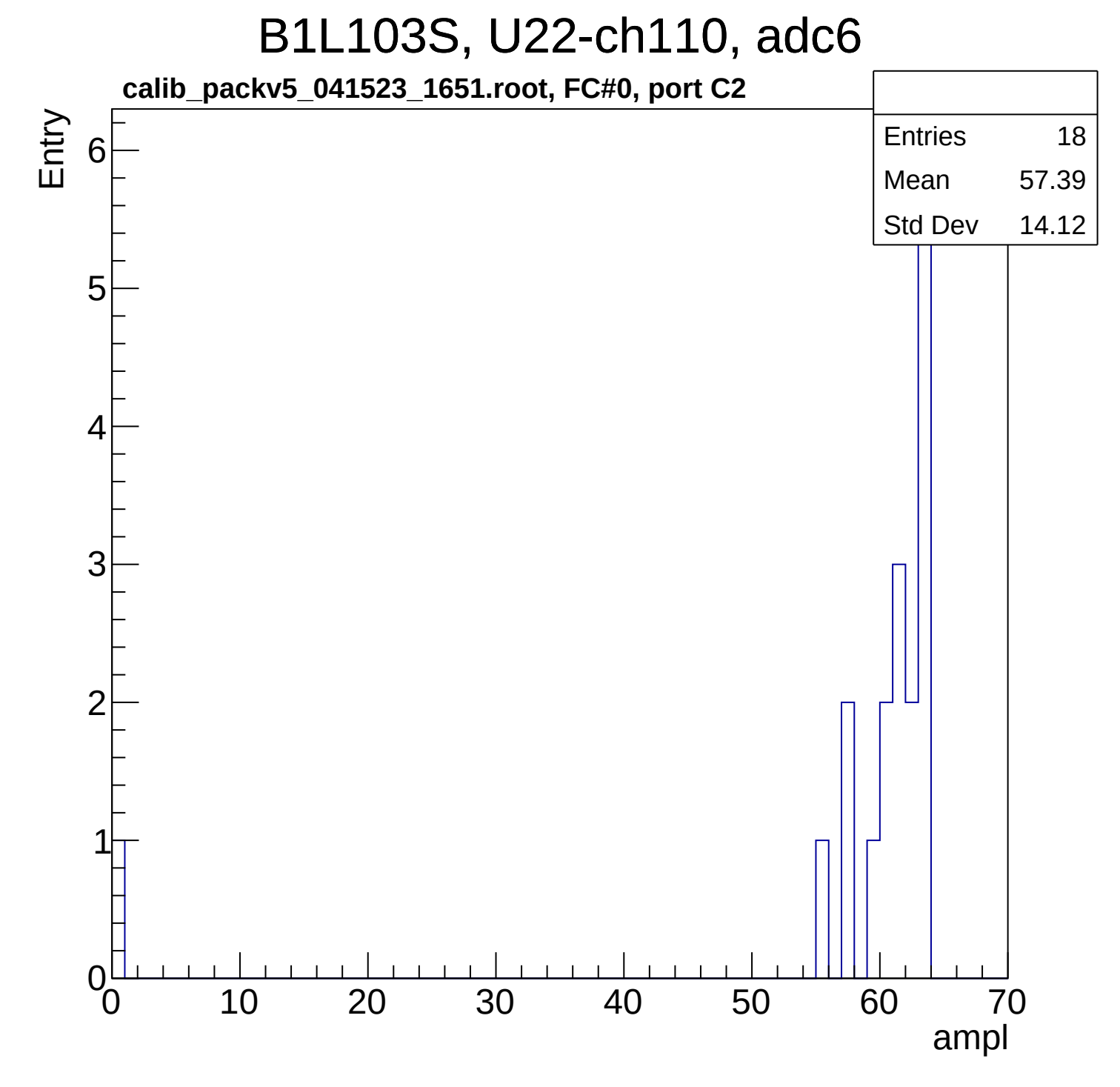
B1L103S, U22-ch110, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 57.39
Std Dev 14.12
Entry
ampl
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2
3
4
5
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0
10
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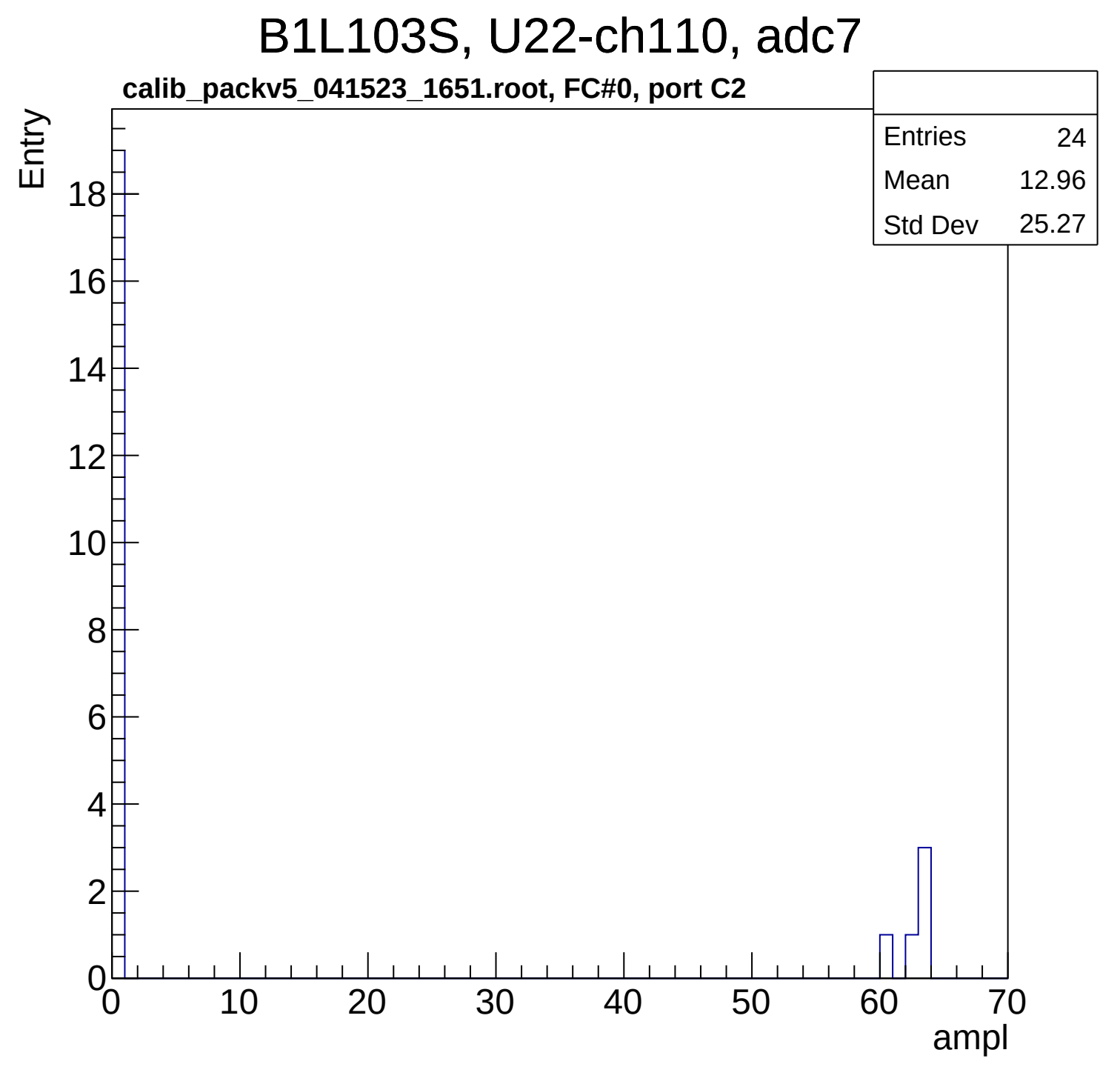
40
50
60
70


B1L103S, U22-ch110, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 12.96
Std Dev 25.27
Entry
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6
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10
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14
16
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10
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30
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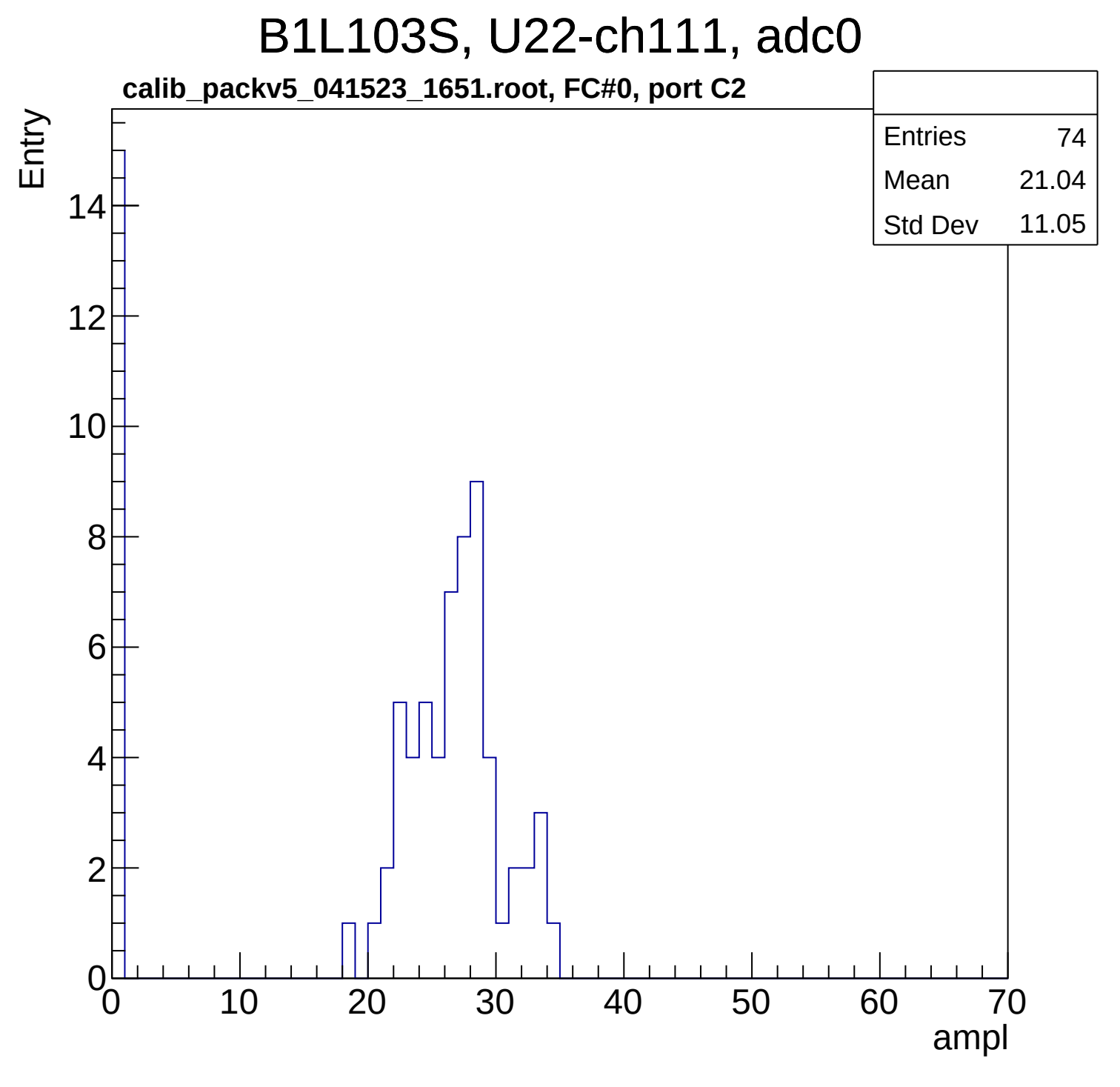
50
60
70
ampl


B1L103S, U22-ch111, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 21.04
Std Dev 11.05
Entry
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4
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10
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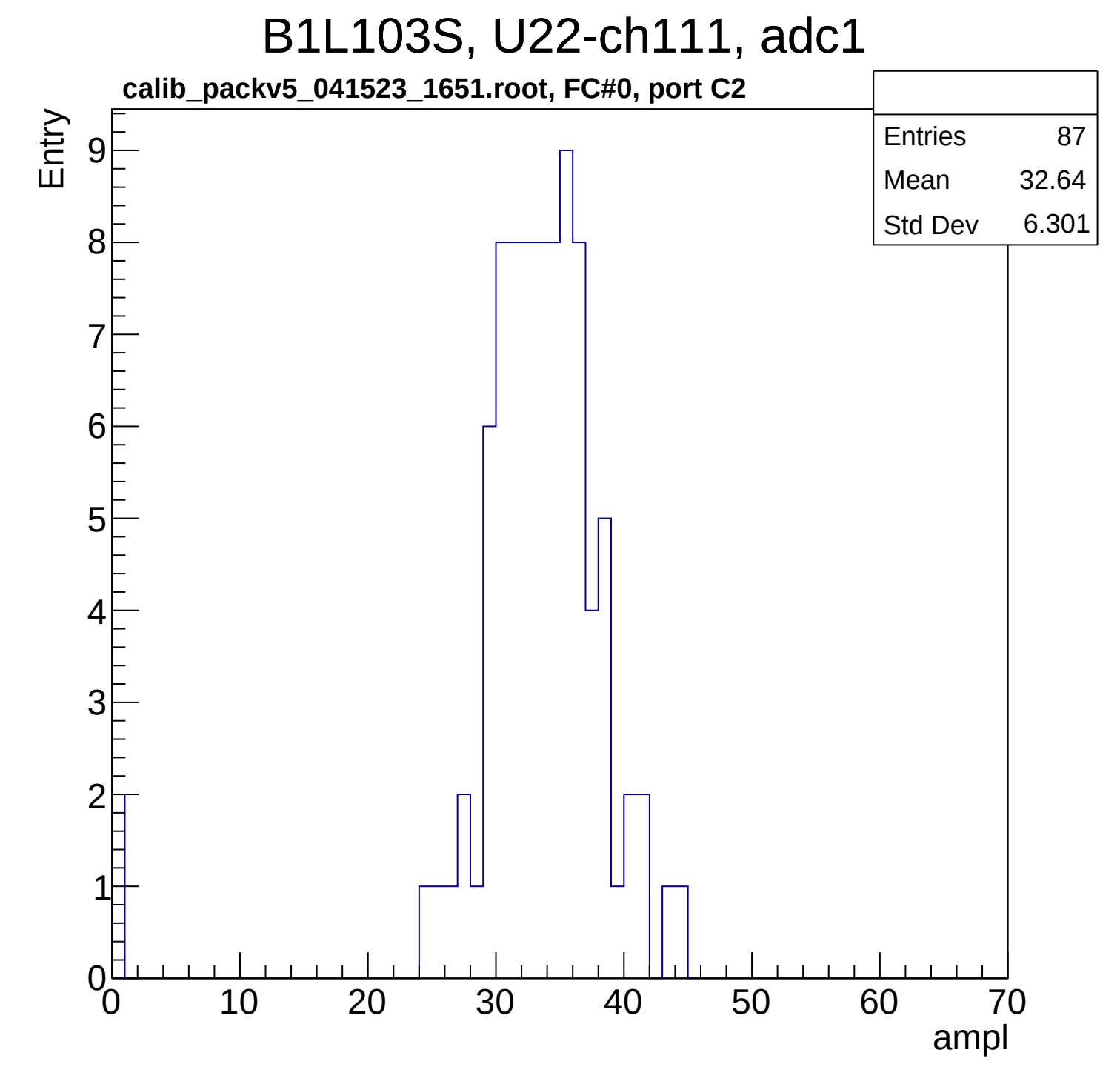
20
30
40
50
60
70
ampl


B1L103S, U22-ch111, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 32.64
Std Dev 6.301
Entry
ampl
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2
3
4
5
6
7
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0
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60
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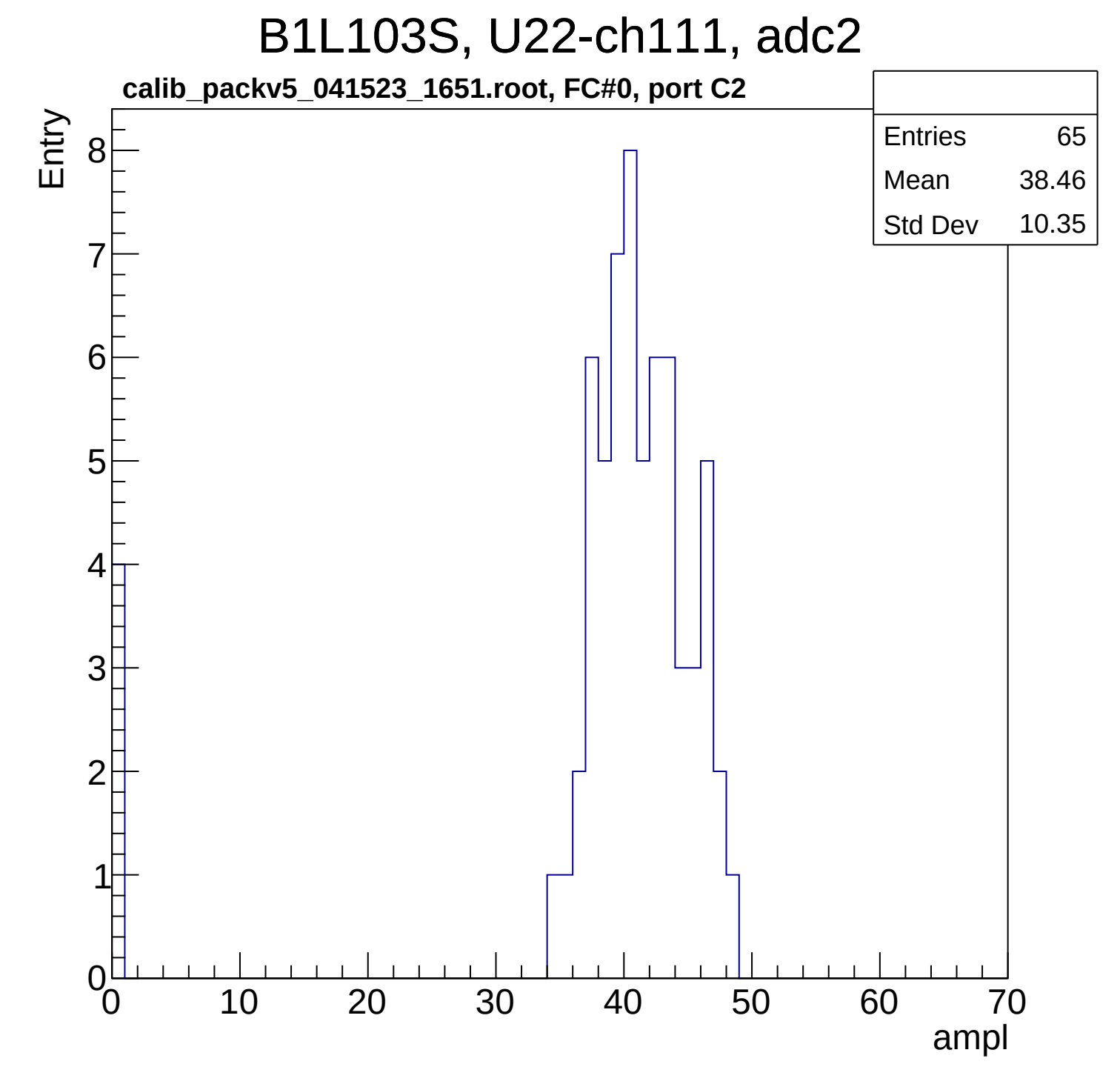
B1L103S, U22-ch111, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 38.46
Std Dev 10.35
Entry
ampl
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4
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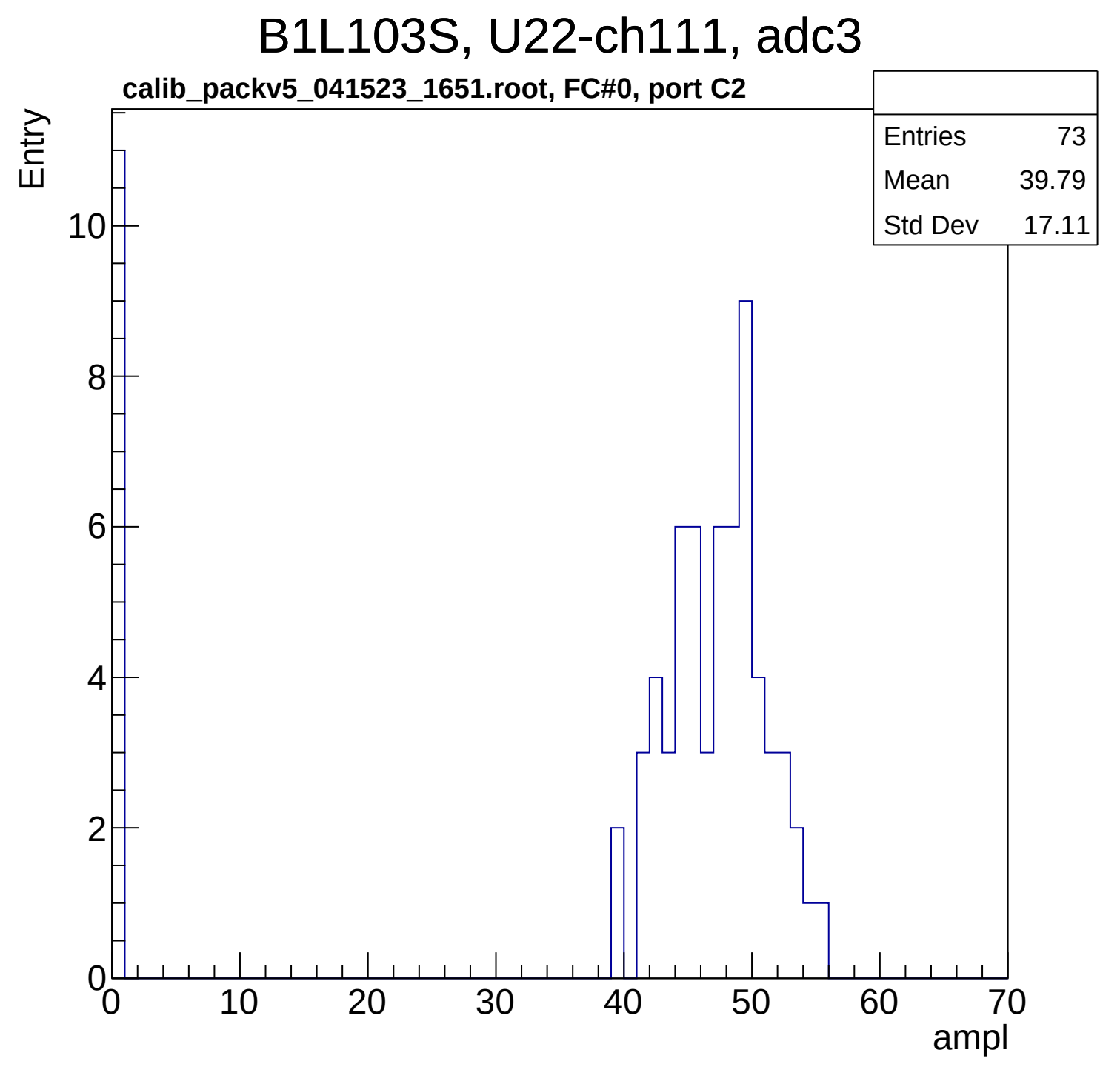
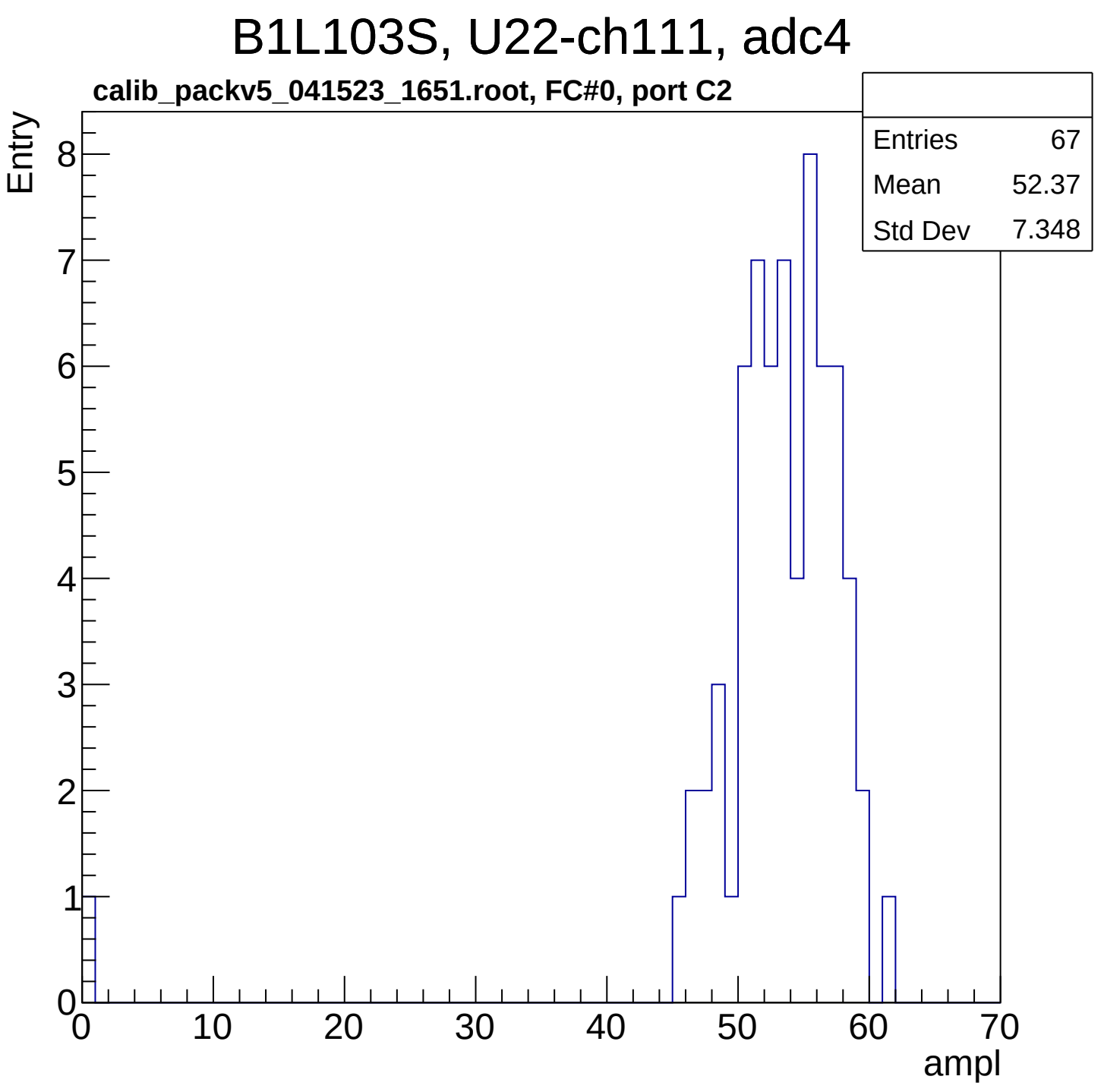

B1L103S, U22-ch111, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 39.79
Std Dev 17.11
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch111, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 52.37
Std Dev 7.348
Entry
ampl
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1
2
3
4
5
6
7
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0
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40
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60
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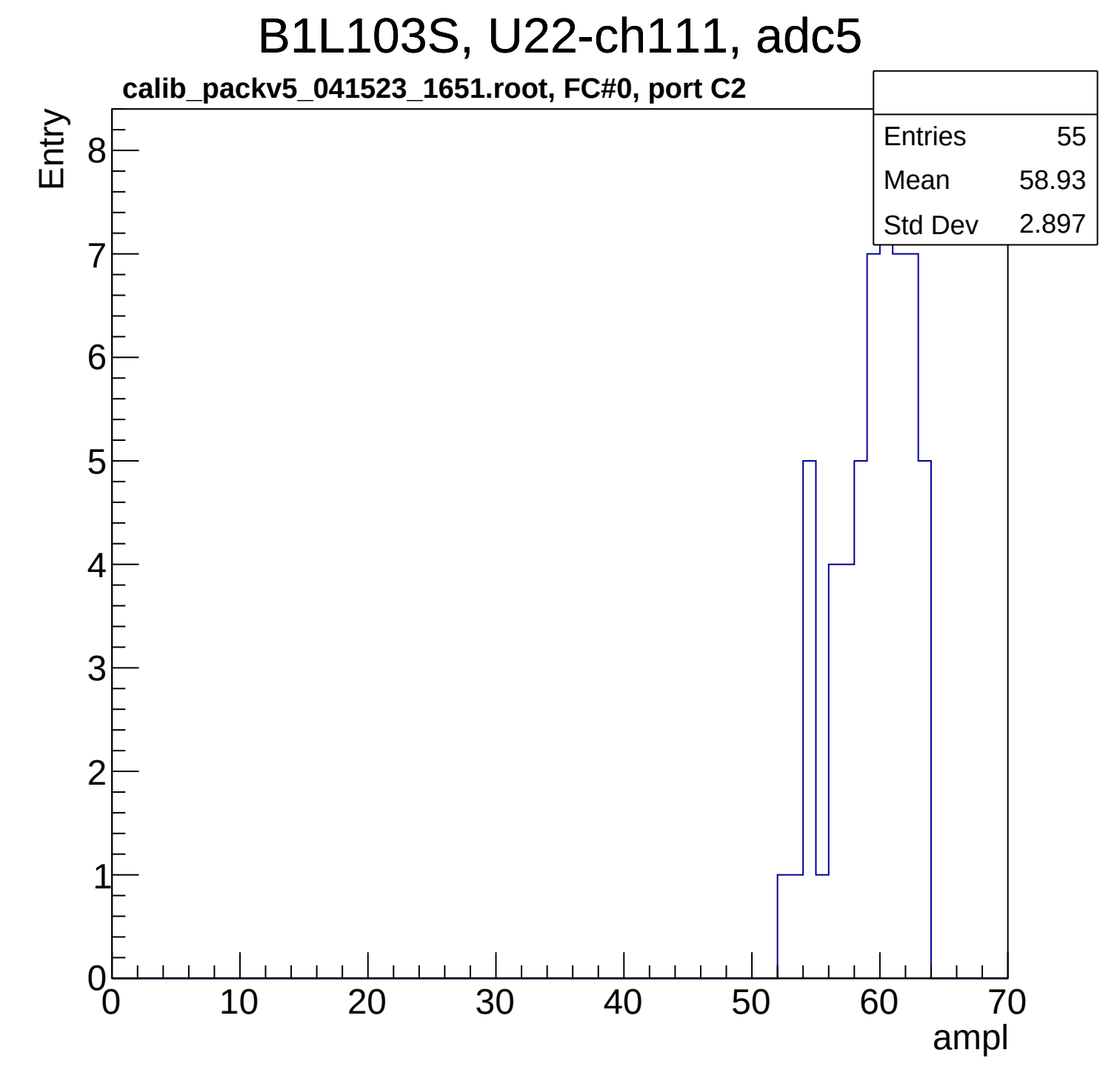
B1L103S, U22-ch111, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 58.93
Std Dev 2.897
Entry
ampl
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2
3
4
5
6
7
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0
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40
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60
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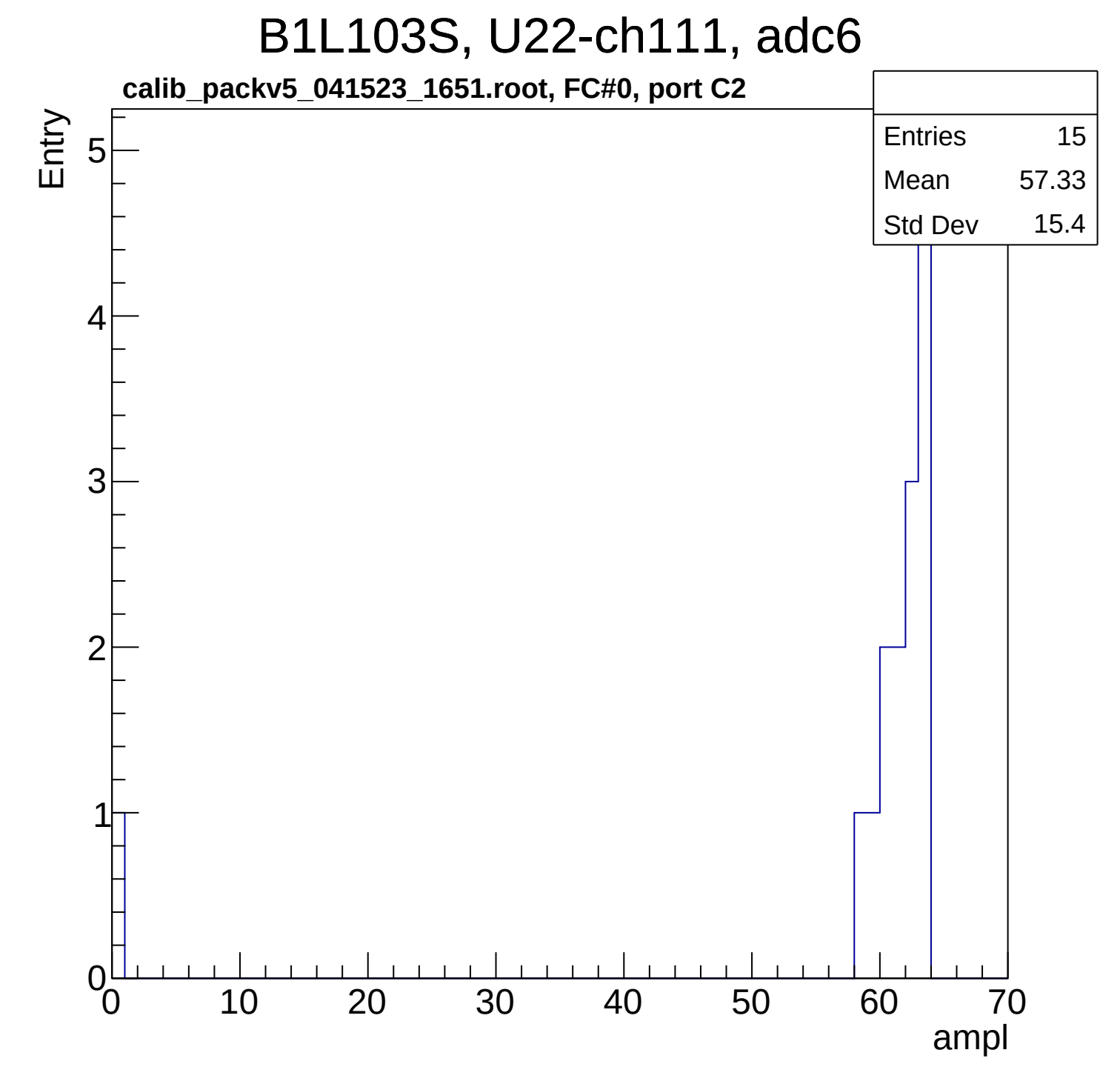
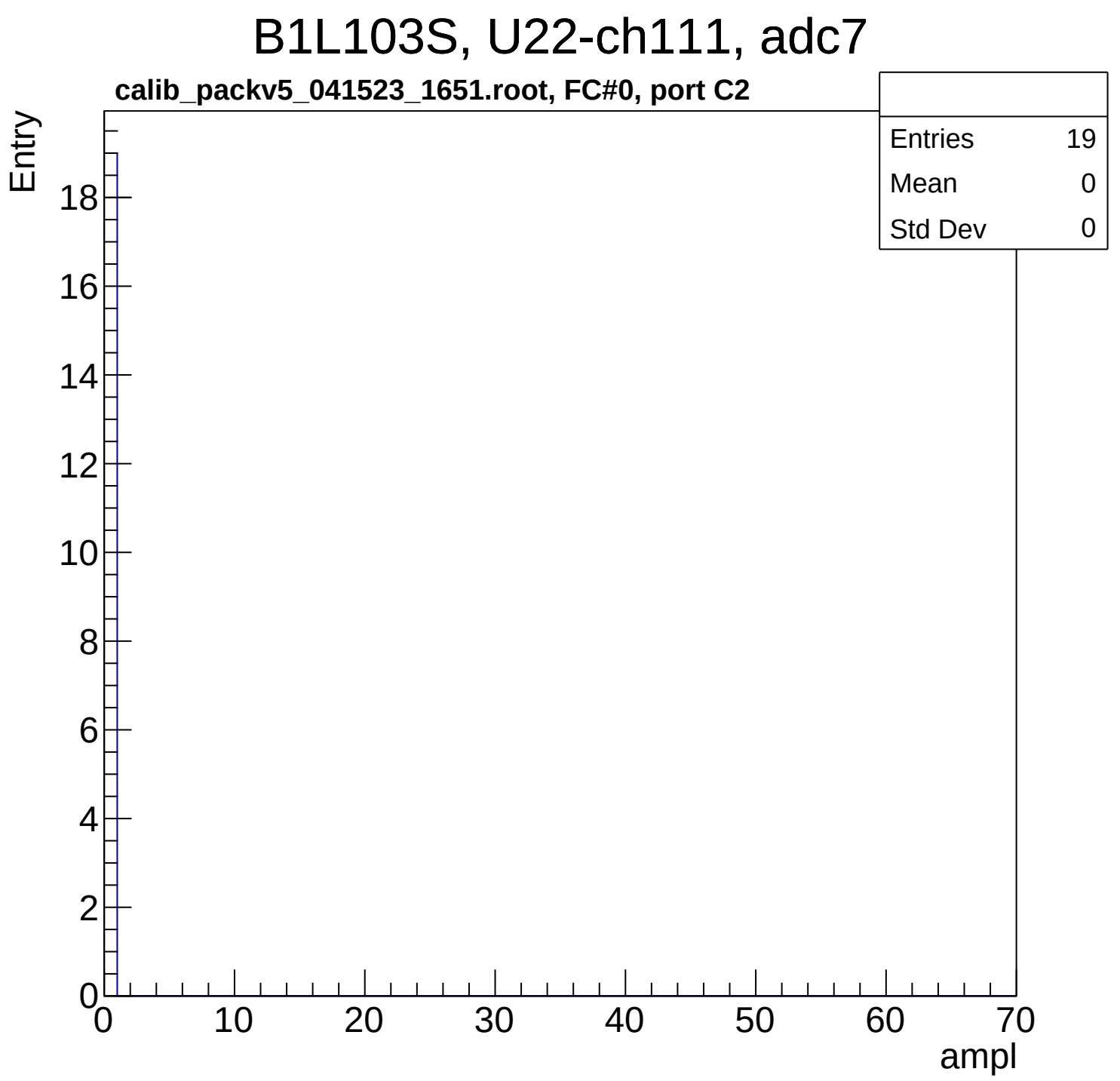

B1L103S, U22-ch111, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 57.33
Std Dev 15.4
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U22-ch111, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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2
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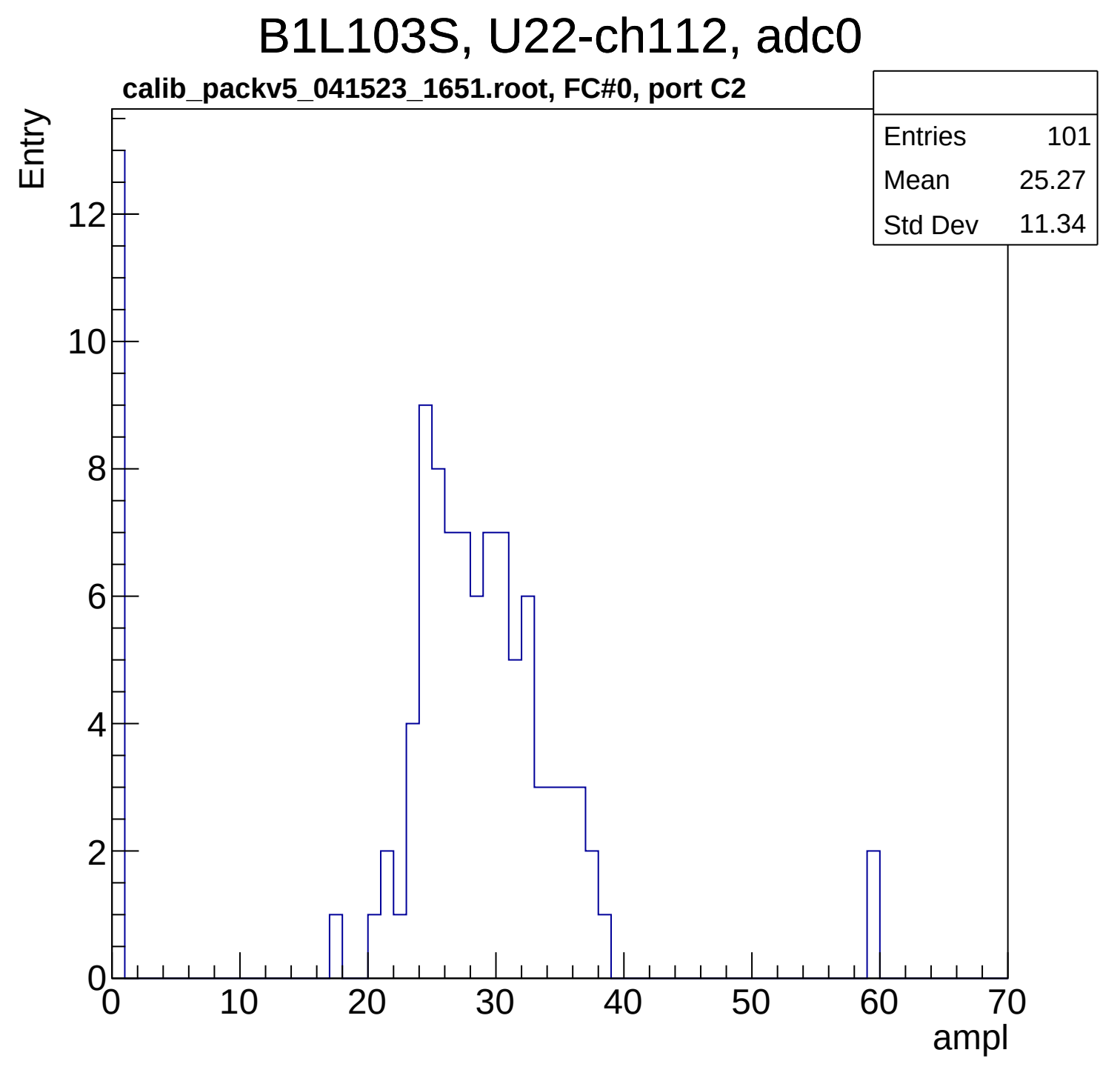
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch112, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 101
Mean 25.27
Std Dev 11.34
Entry
ampl
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2
4
6
8
10
12
0
10
20
30
40
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60
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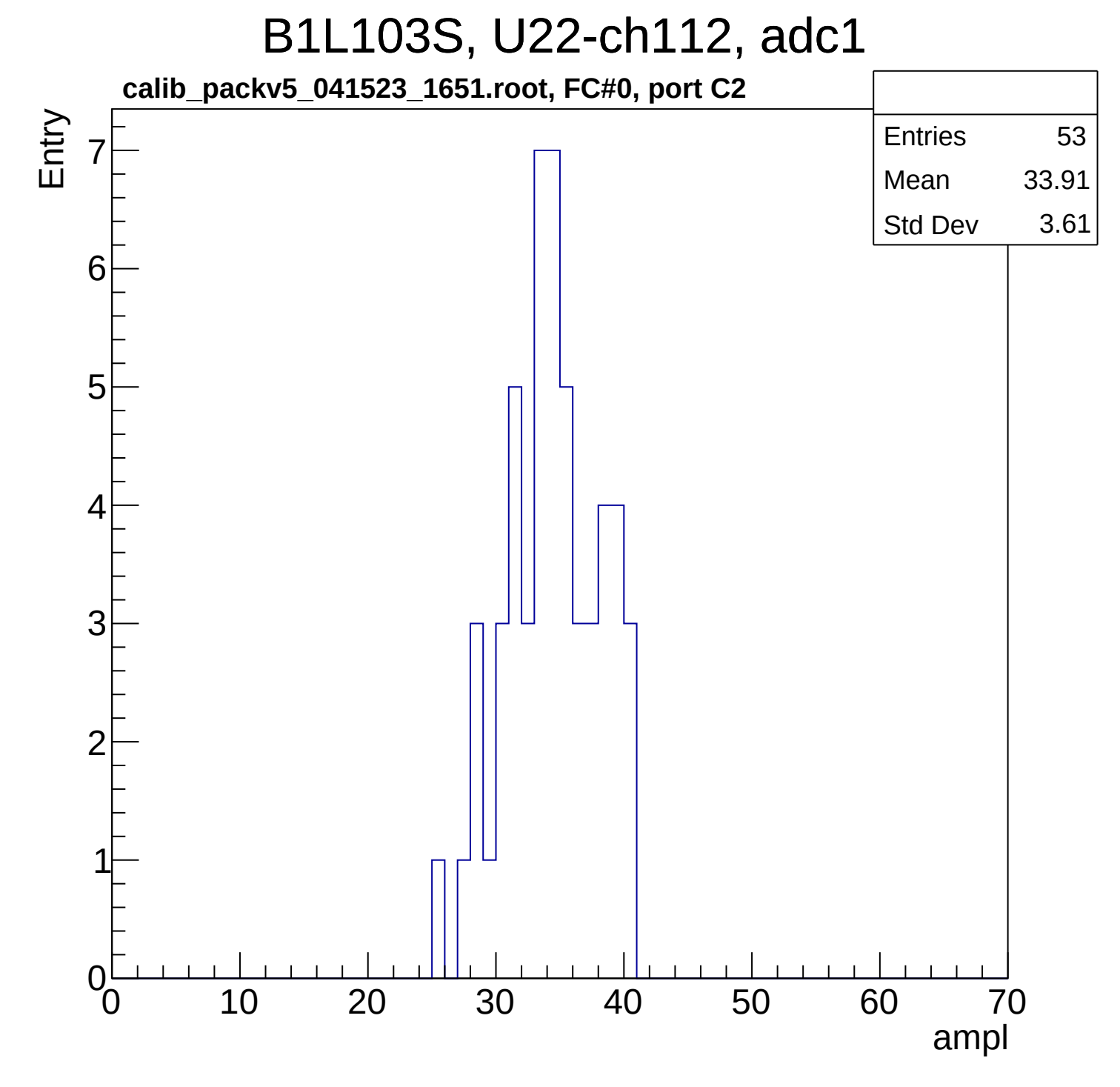
B1L103S, U22-ch112, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 33.91
Std Dev 3.61
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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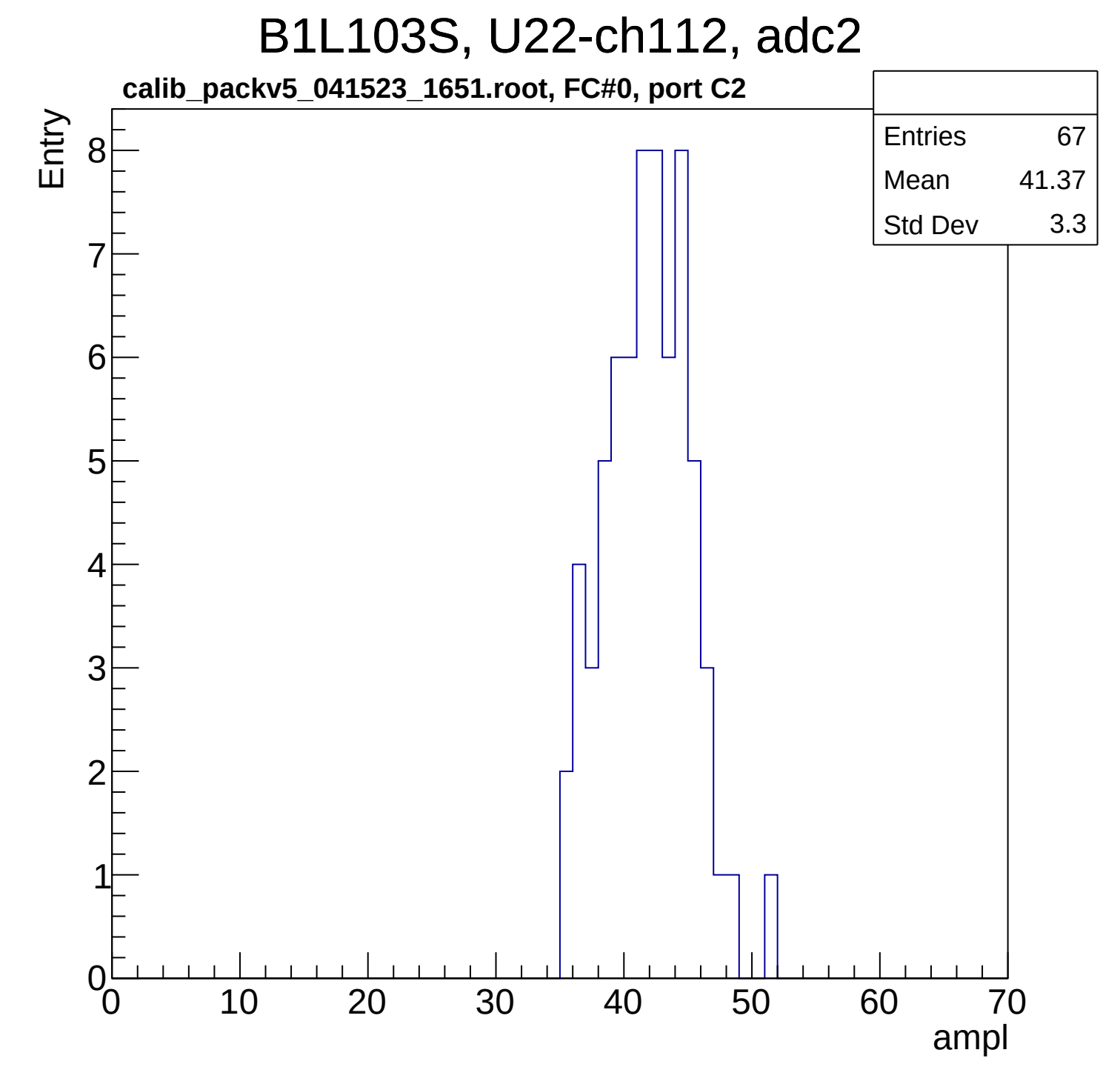
B1L103S, U22-ch112, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 41.37
Std Dev 3.3
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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40
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60
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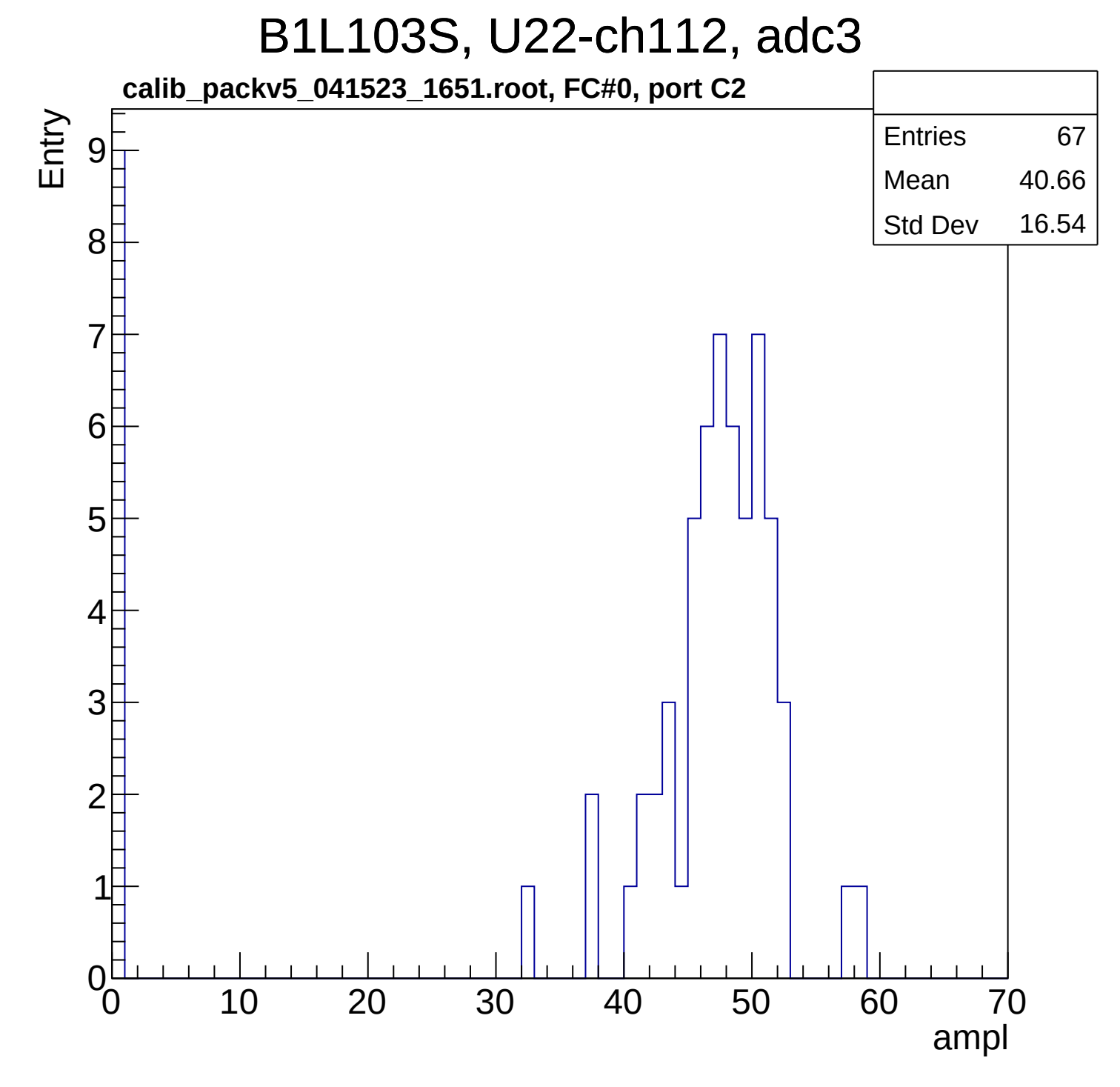
B1L103S, U22-ch112, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 40.66
Std Dev 16.54
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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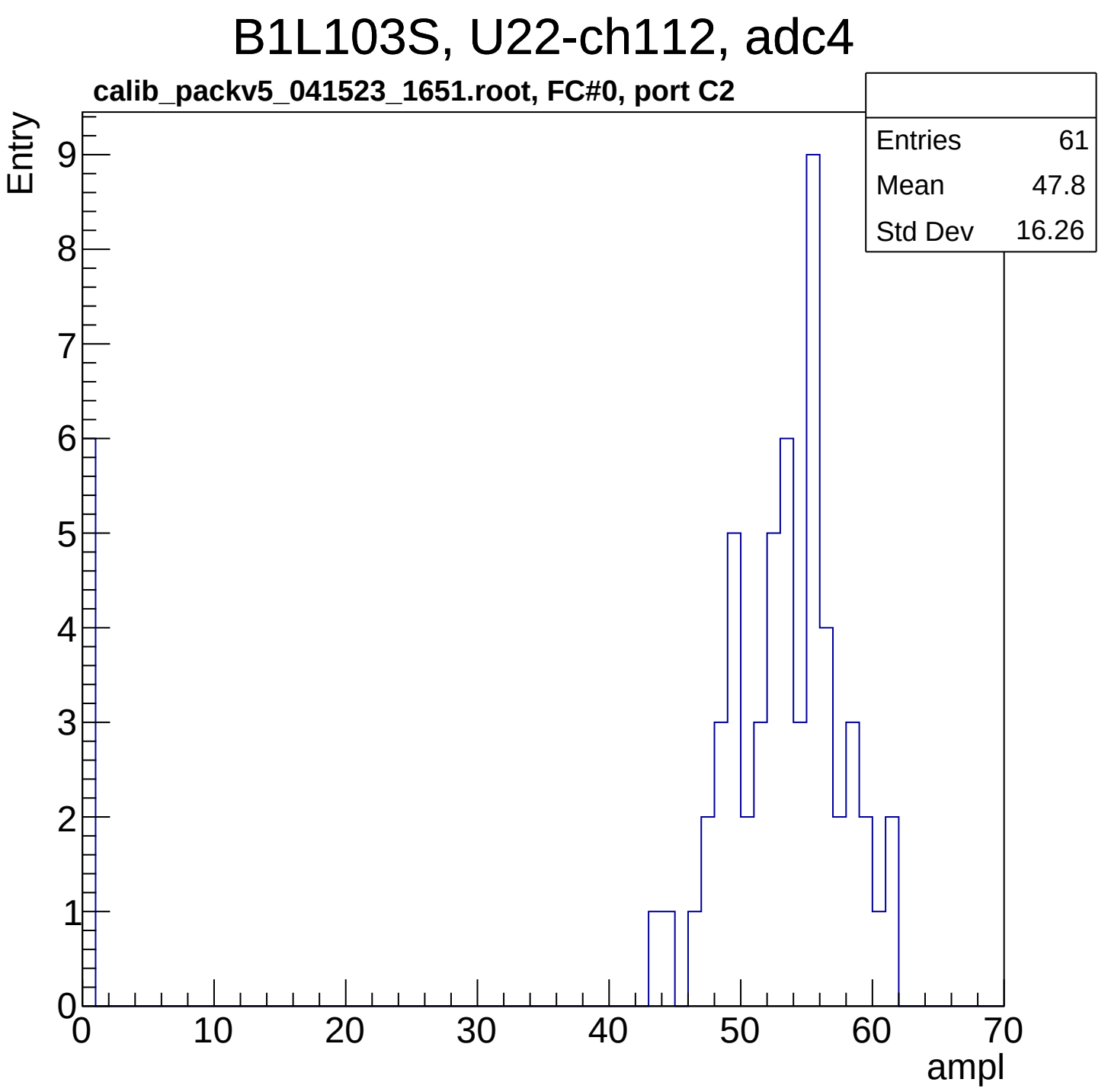
B1L103S, U22-ch112, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 47.8
Std Dev 16.26
Entry
ampl
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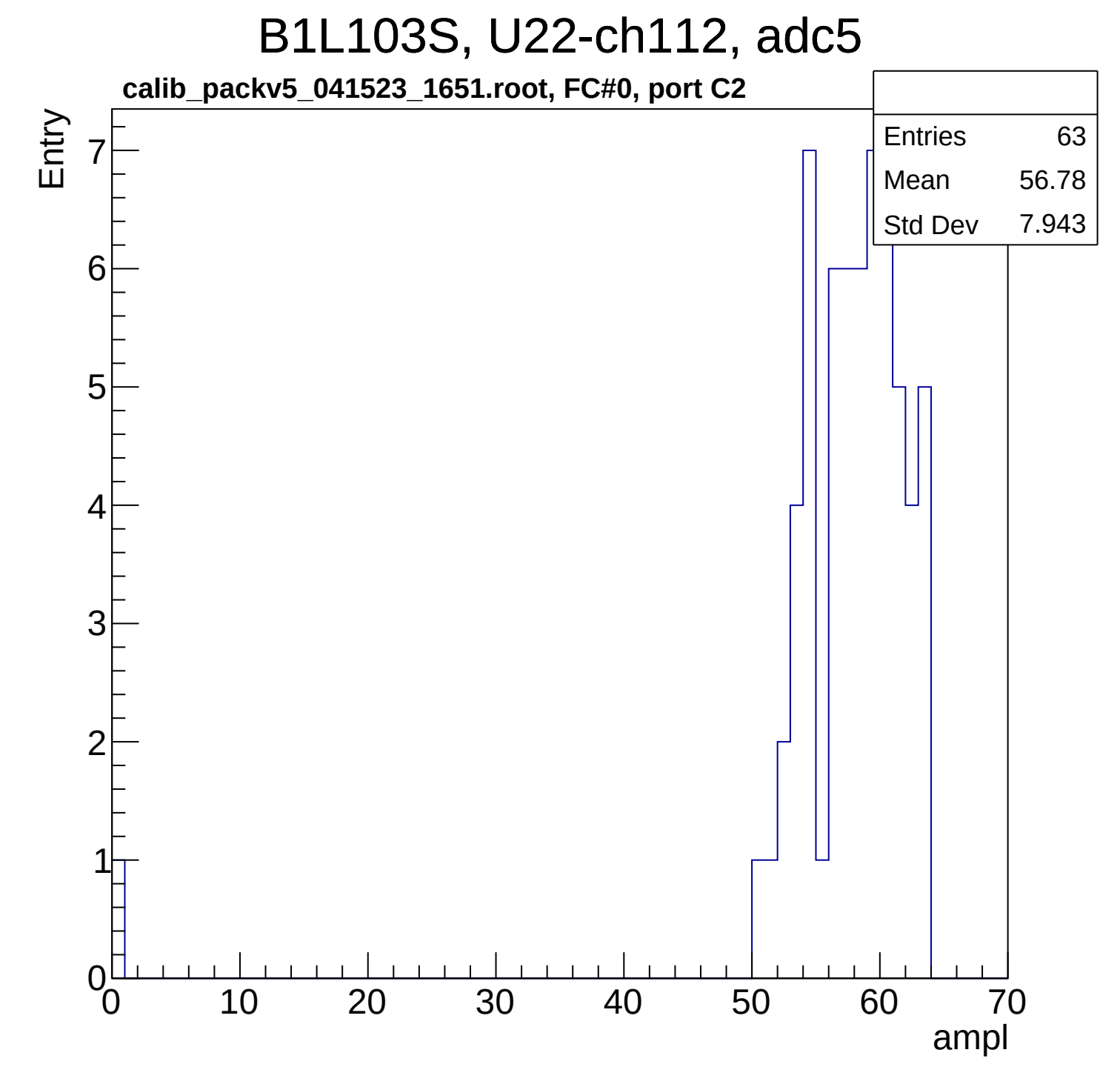
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch112, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 56.78
Std Dev 7.943
Entry
ampl
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1
2
3
4
5
6
7
0
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20
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40
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60
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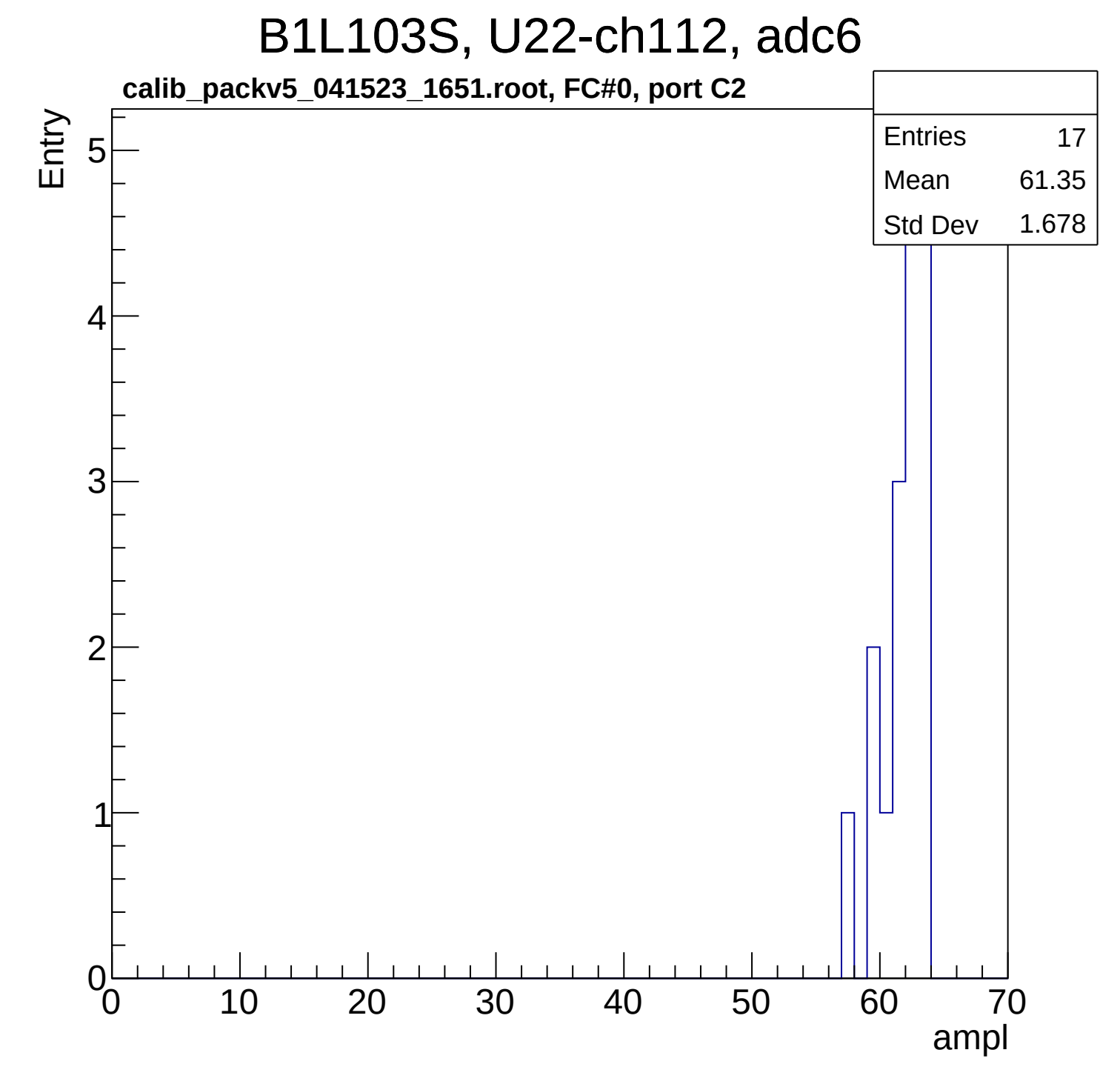
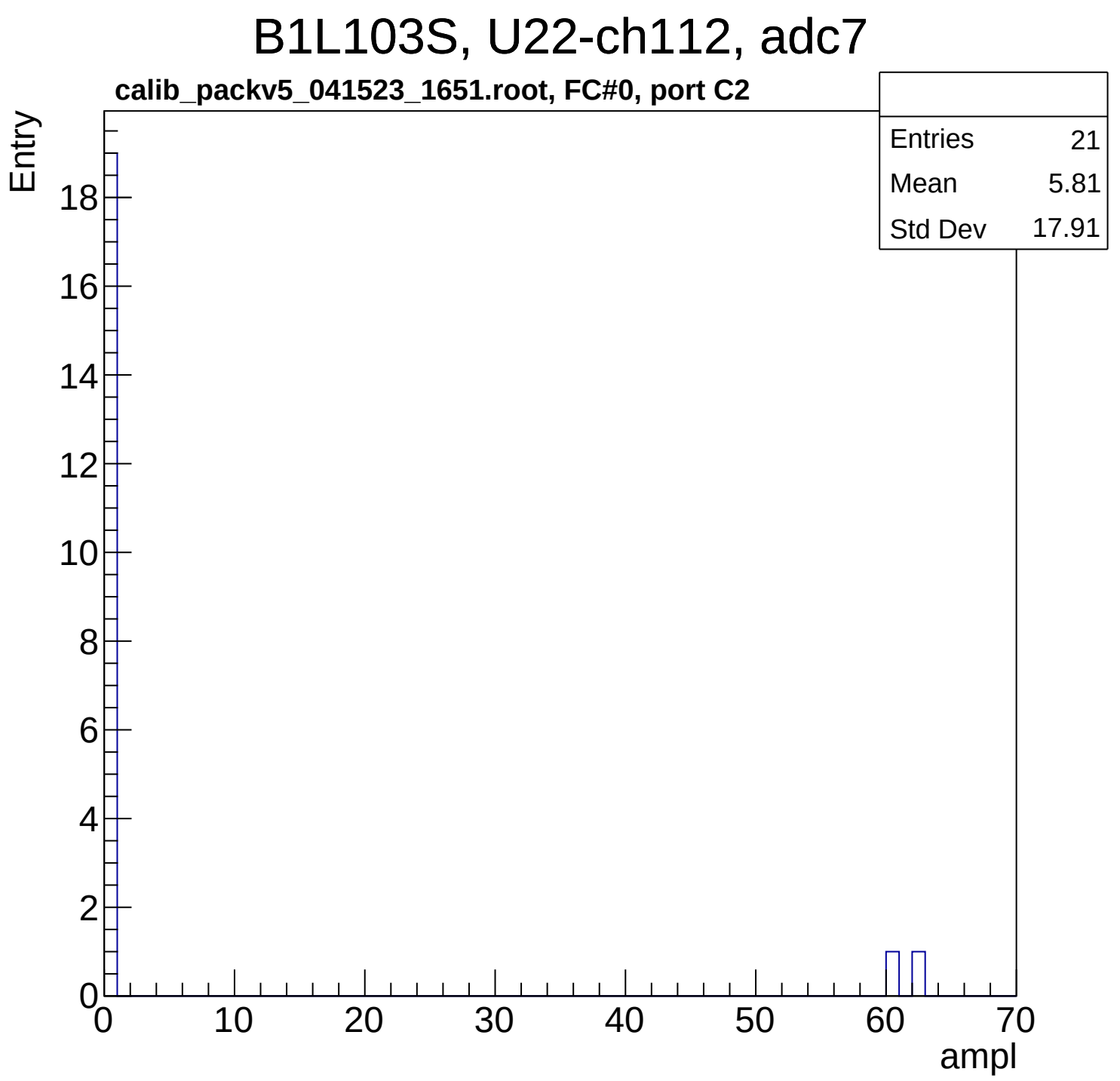

B1L103S, U22-ch112, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 61.35
Std Dev 1.678
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U22-ch112, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.81
Std Dev 17.91
Entry
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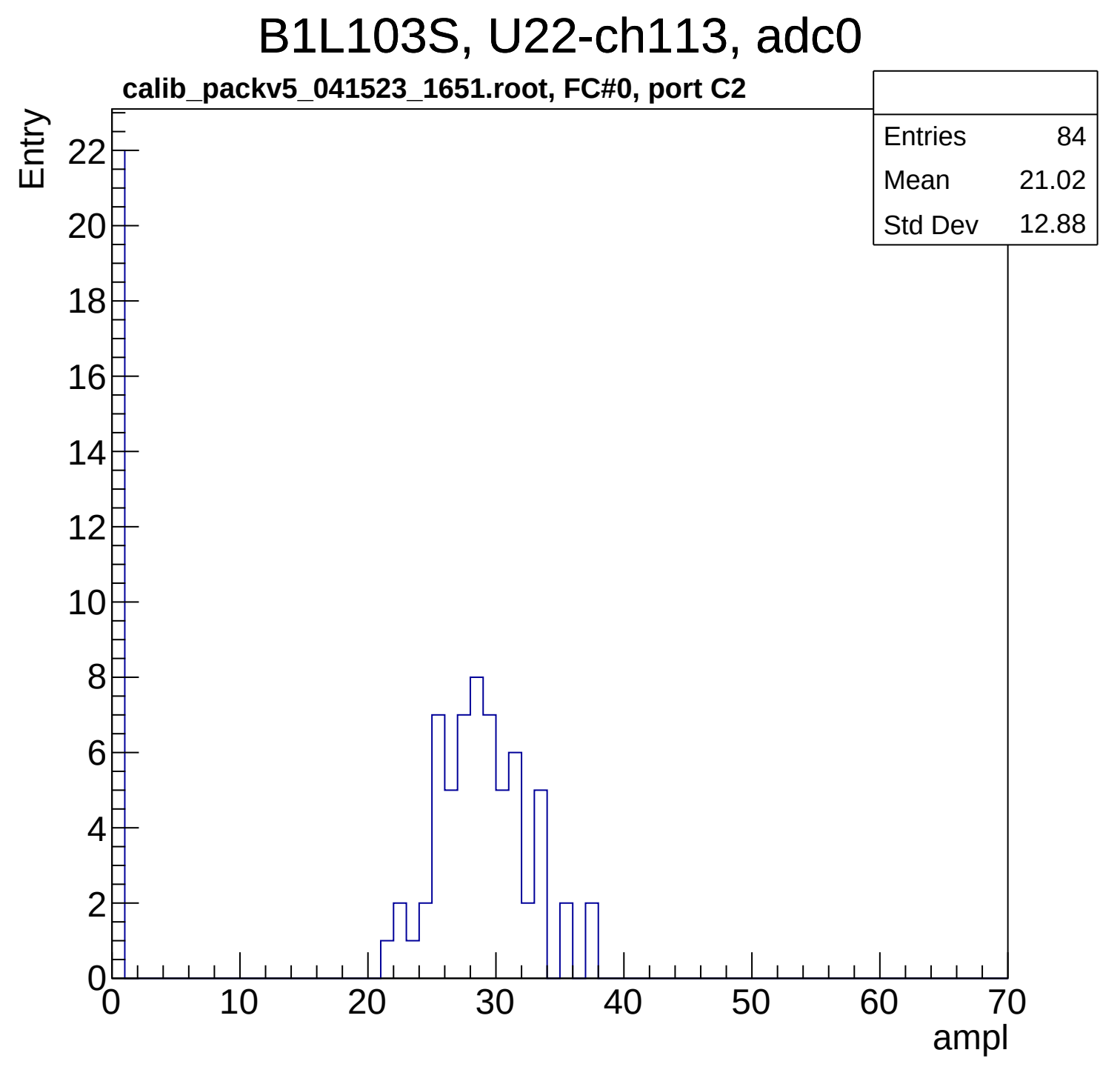
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch113, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 21.02
Std Dev 12.88
Entry
0
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4
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8
10
12
14
16
18
20
22
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10
20
30
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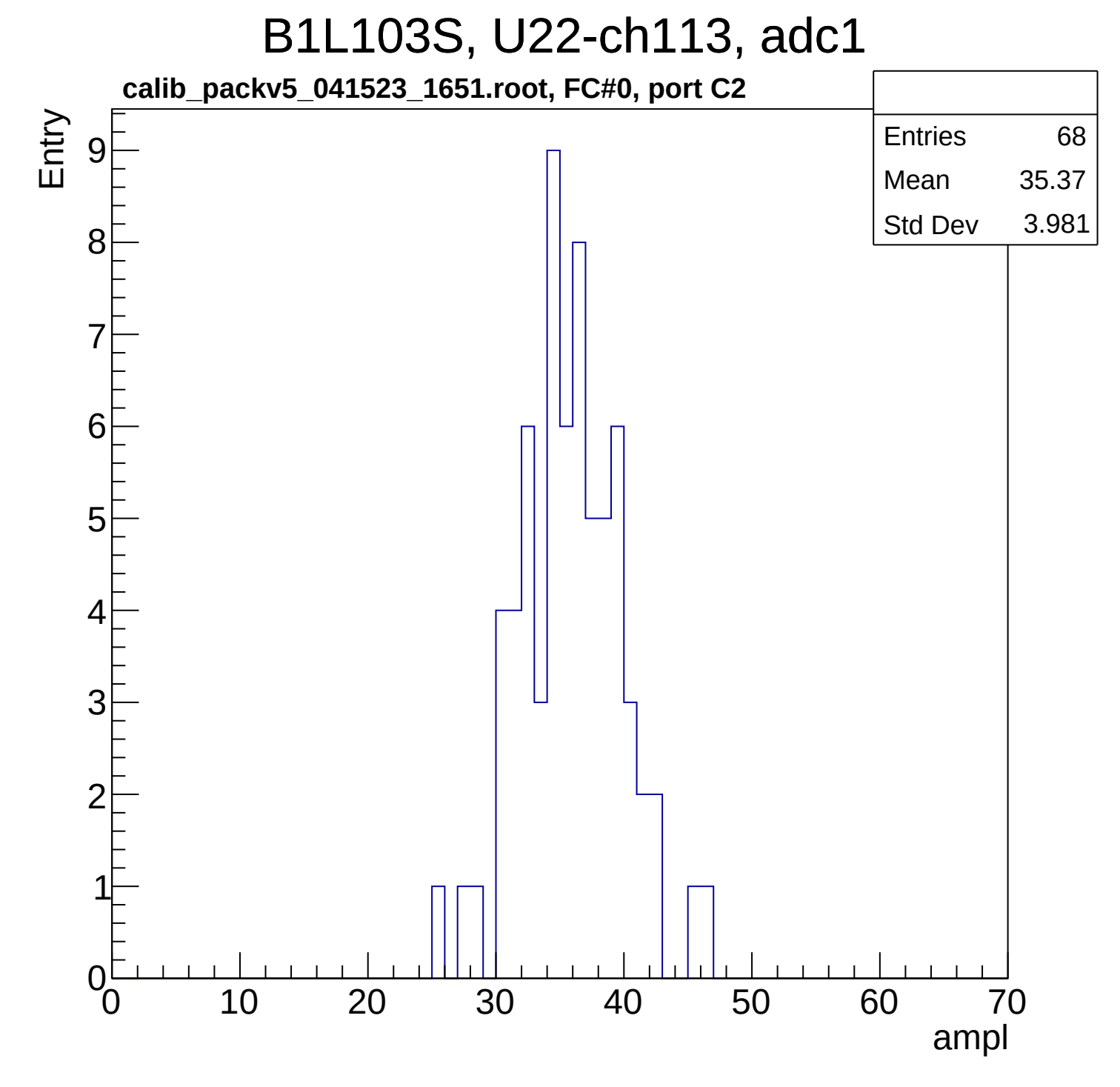
50
60
70
ampl


B1L103S, U22-ch113, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 35.37
Std Dev 3.981
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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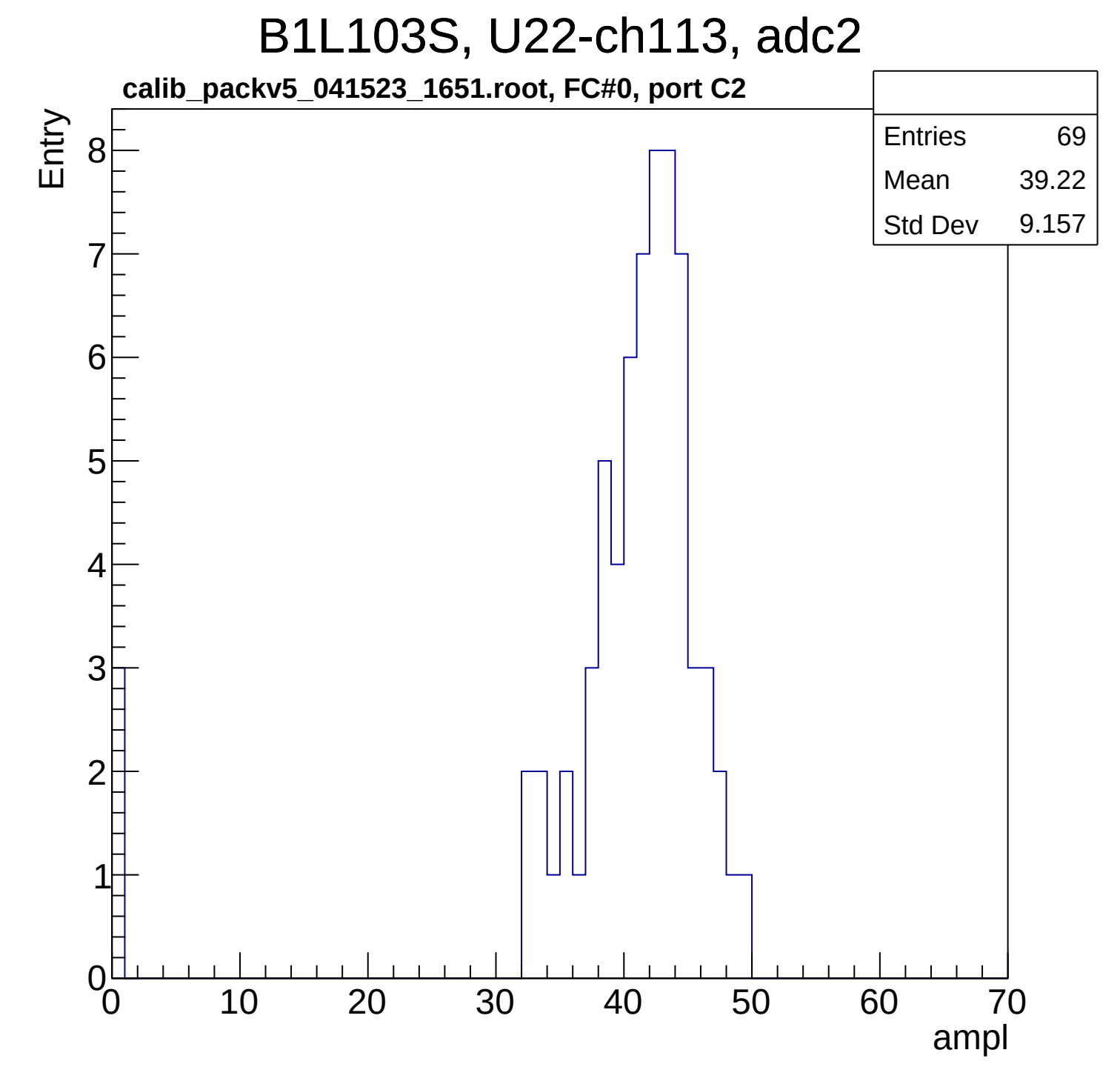
B1L103S, U22-ch113, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 39.22
Std Dev 9.157
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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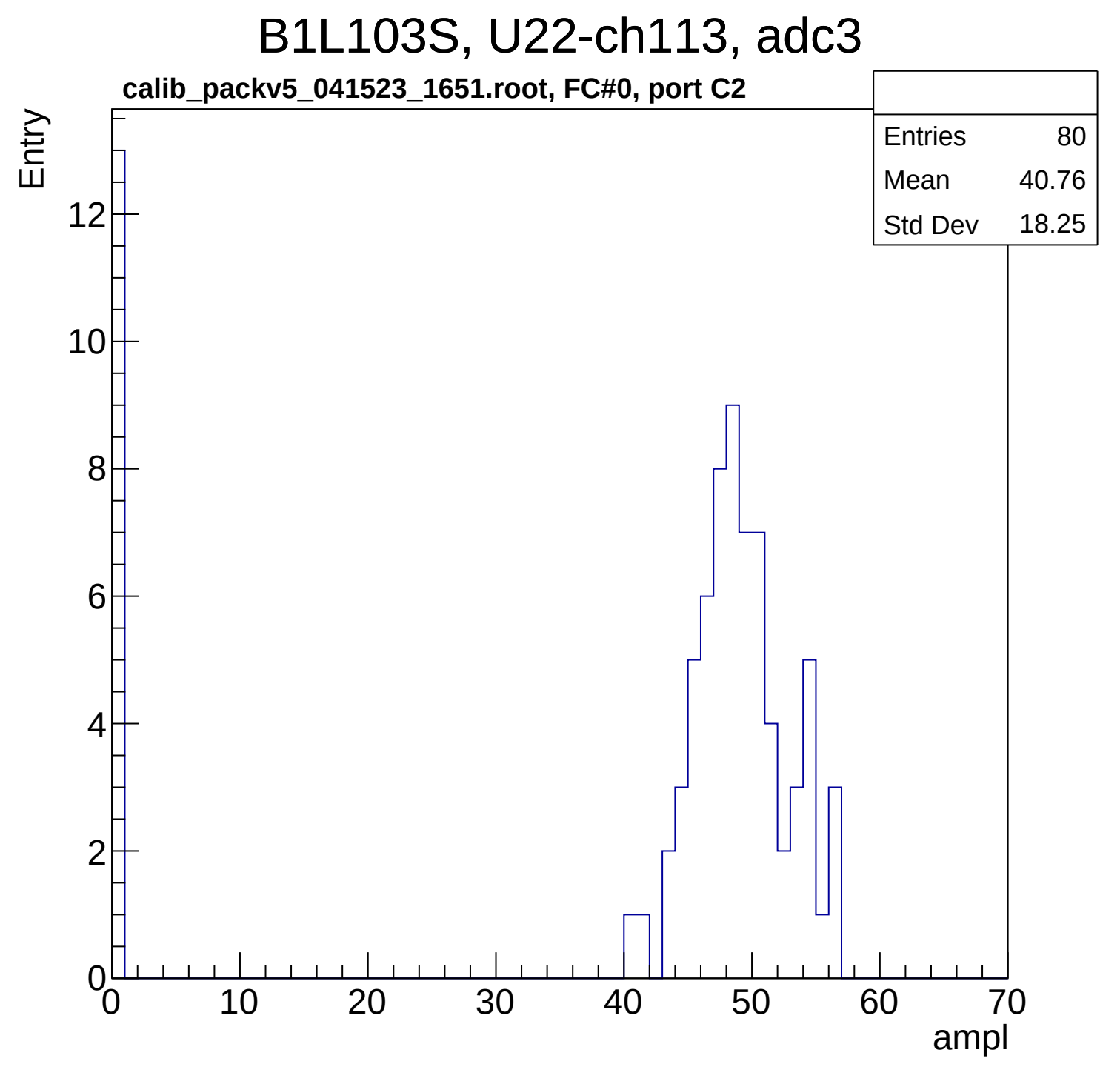
B1L103S, U22-ch113, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 40.76
Std Dev 18.25
Entry
ampl
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4
6
8
10
12
0
10
20
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40
50
60
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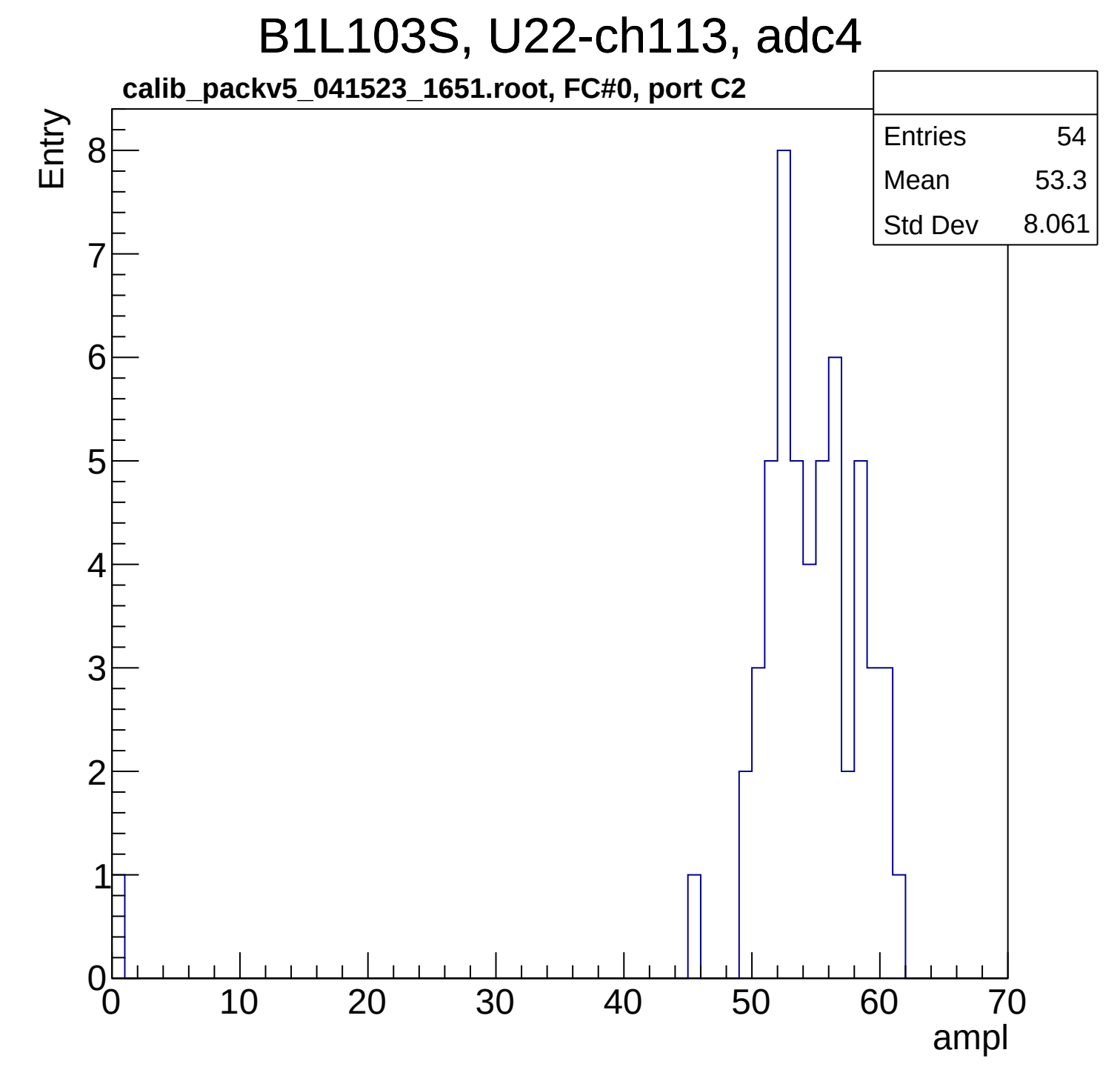
B1L103S, U22-ch113, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 53.3
Std Dev 8.061
Entry
ampl
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2
3
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5
6
7
8
0
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20
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40
50
60
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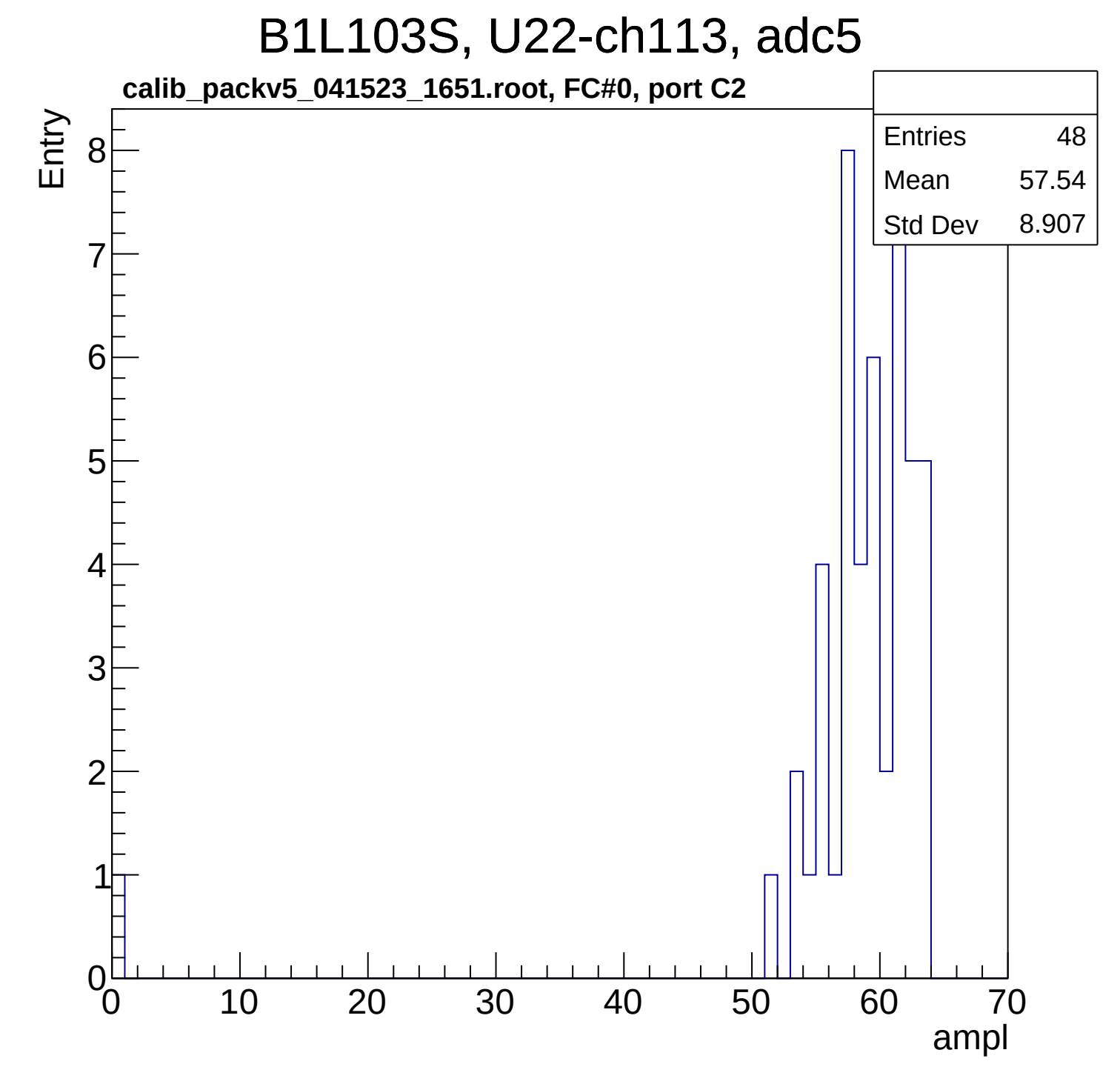
B1L103S, U22-ch113, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 57.54
Std Dev 8.907
Entry
ampl
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2
3
4
5
6
7
8
0
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40
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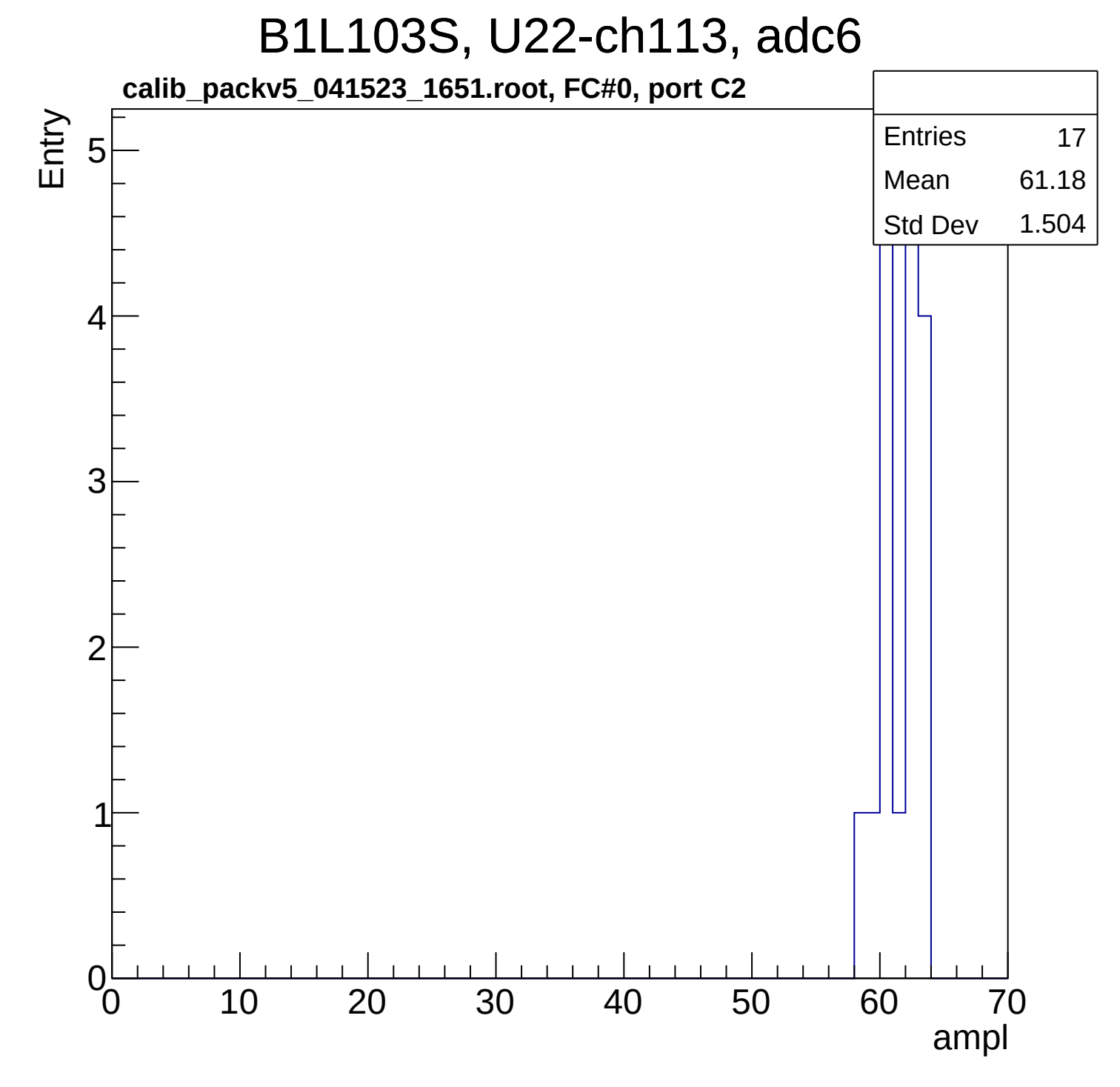
60
70


B1L103S, U22-ch113, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 61.18
Std Dev 1.504
Entry
ampl
0
1
2
3
4
5
0
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20
30
40
50
60
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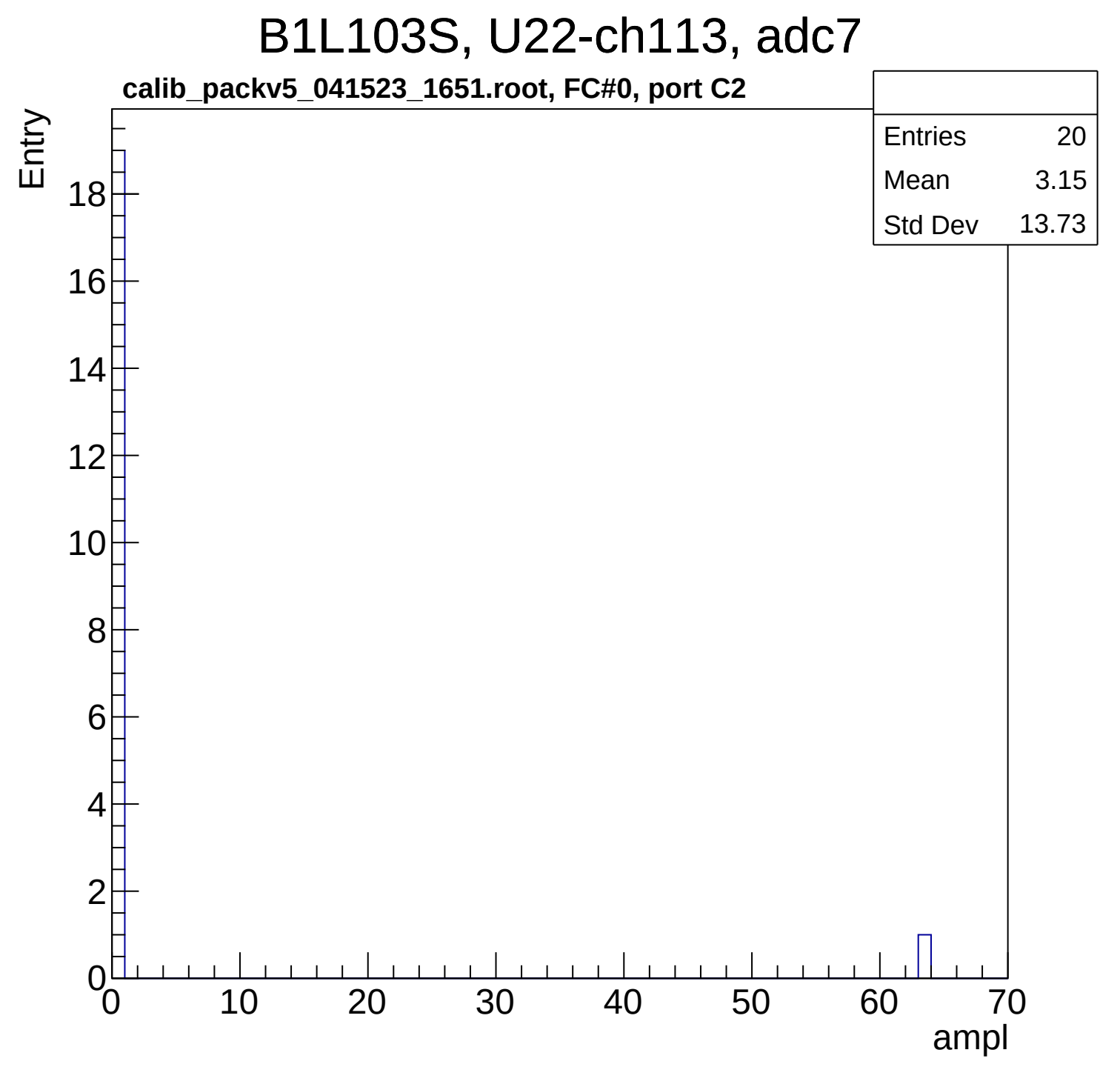
B1L103S, U22-ch113, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
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8
10
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14
16
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30
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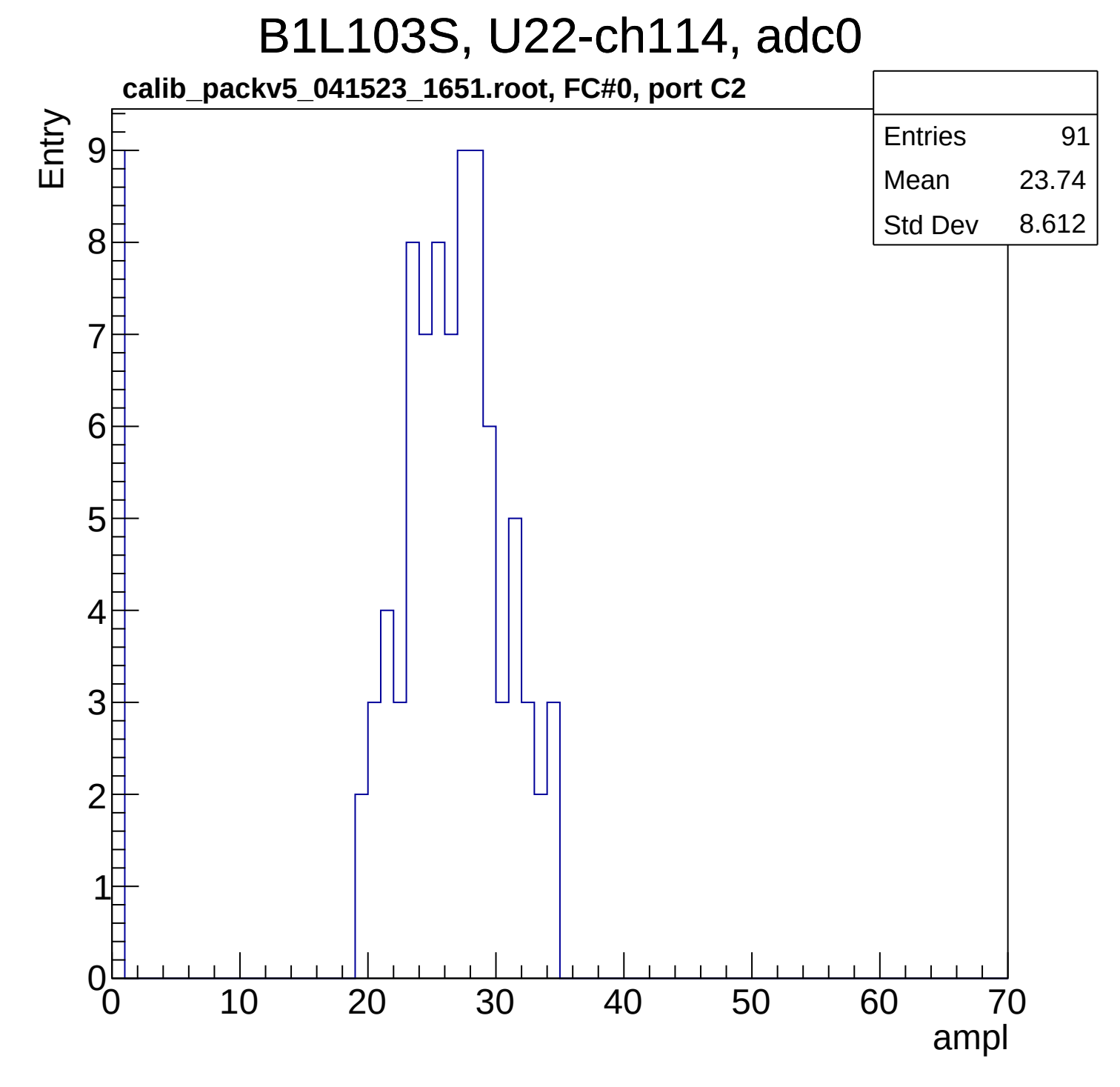
50
60
70
ampl


B1L103S, U22-ch114, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 23.74
Std Dev 8.612
Entry
ampl
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6
7
8
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0
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60
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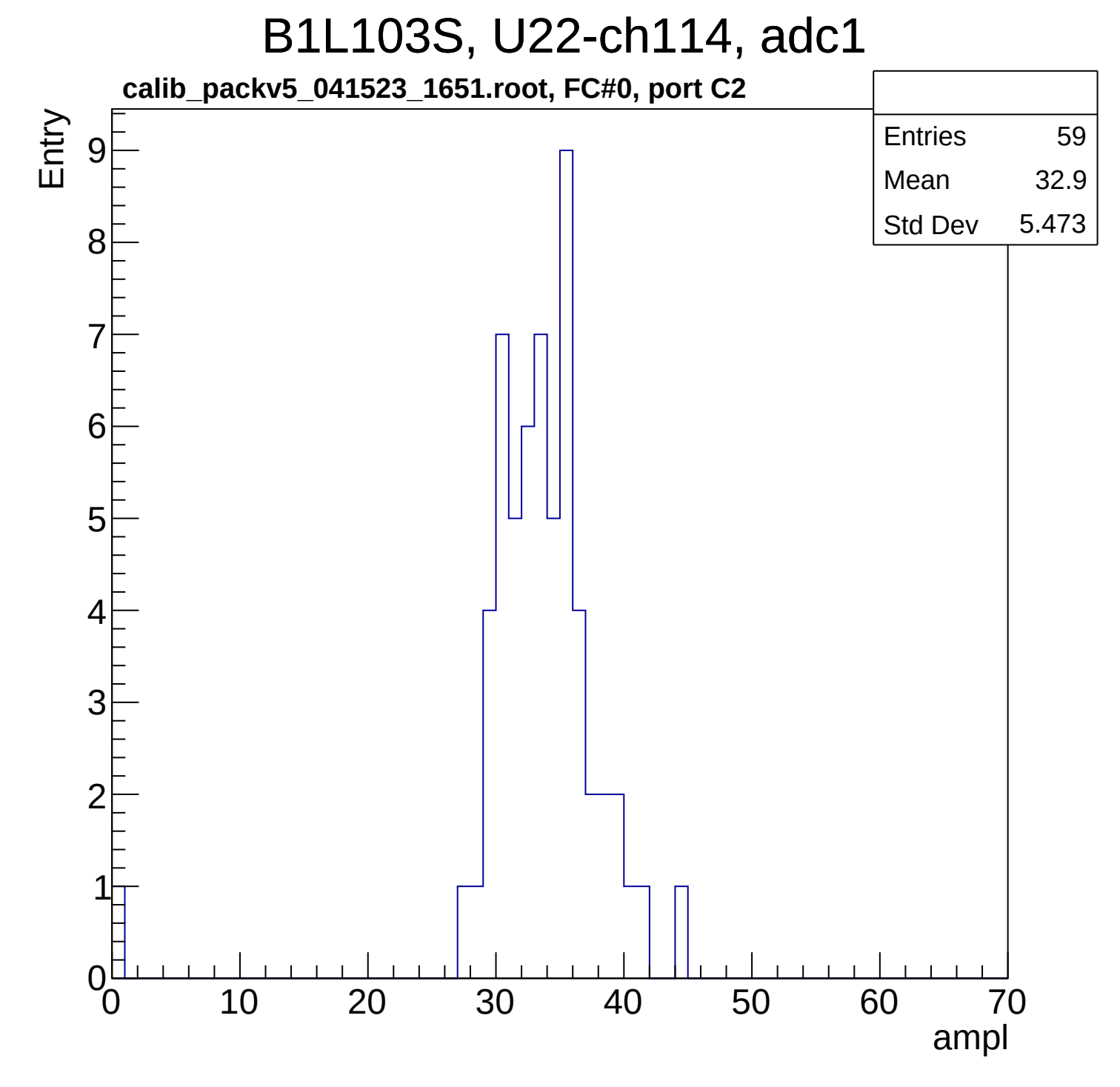
B1L103S, U22-ch114, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 32.9
Std Dev 5.473
Entry
ampl
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4
5
6
7
8
9
0
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20
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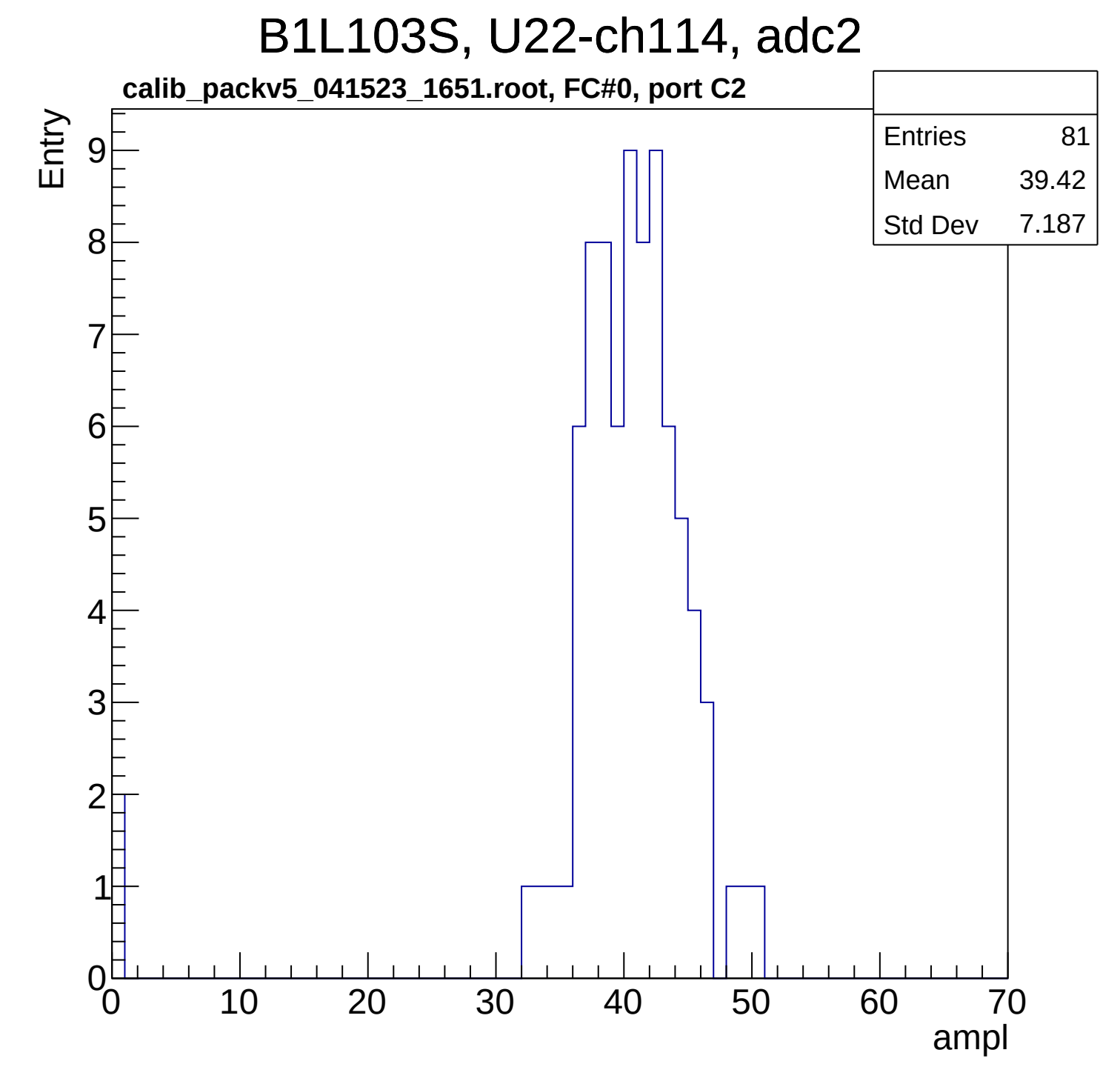
60
70


B1L103S, U22-ch114, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 39.42
Std Dev 7.187
Entry
ampl
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4
5
6
7
8
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0
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20
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40
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60
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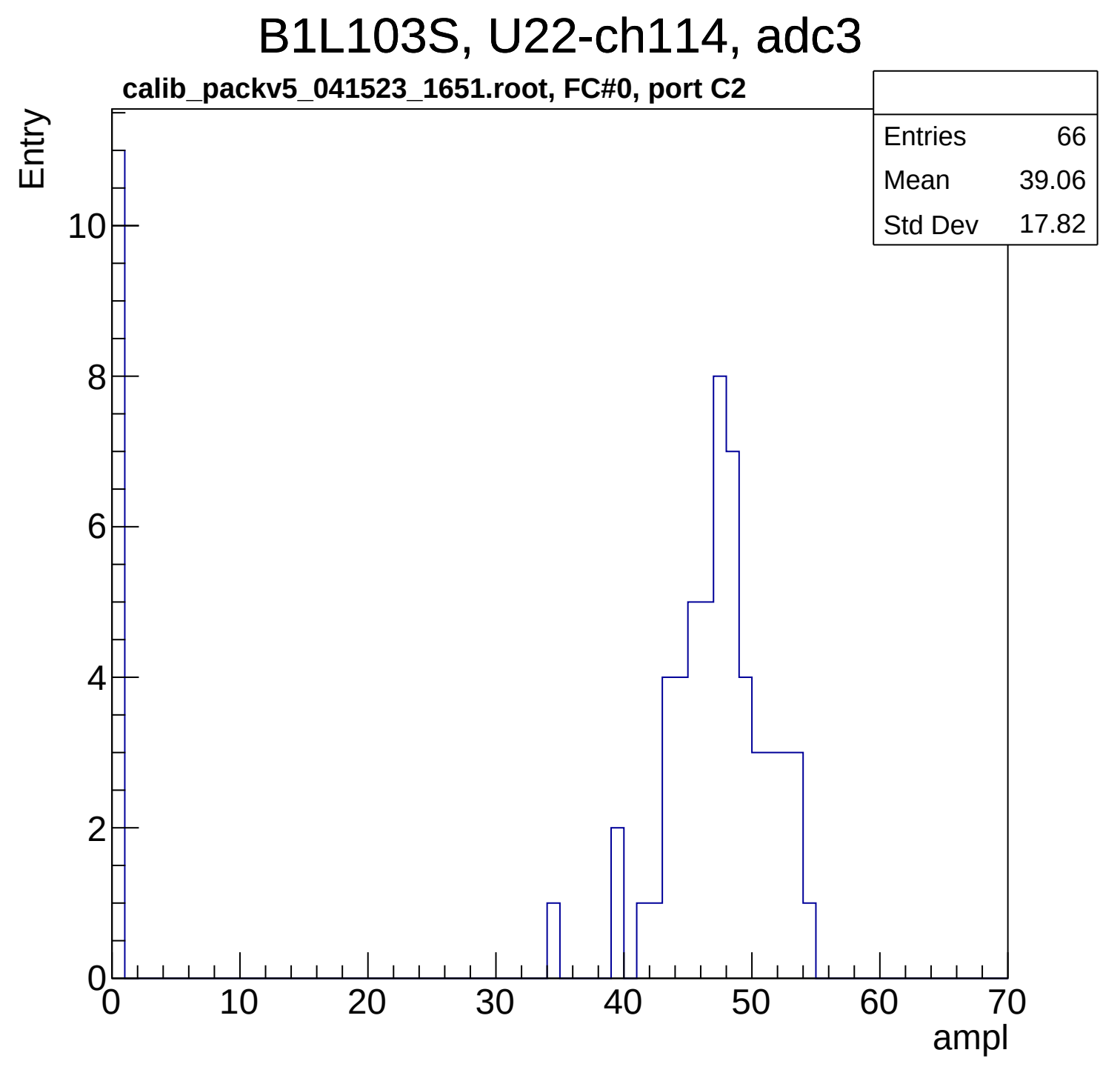
B1L103S, U22-ch114, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 39.06
Std Dev 17.82
Entry
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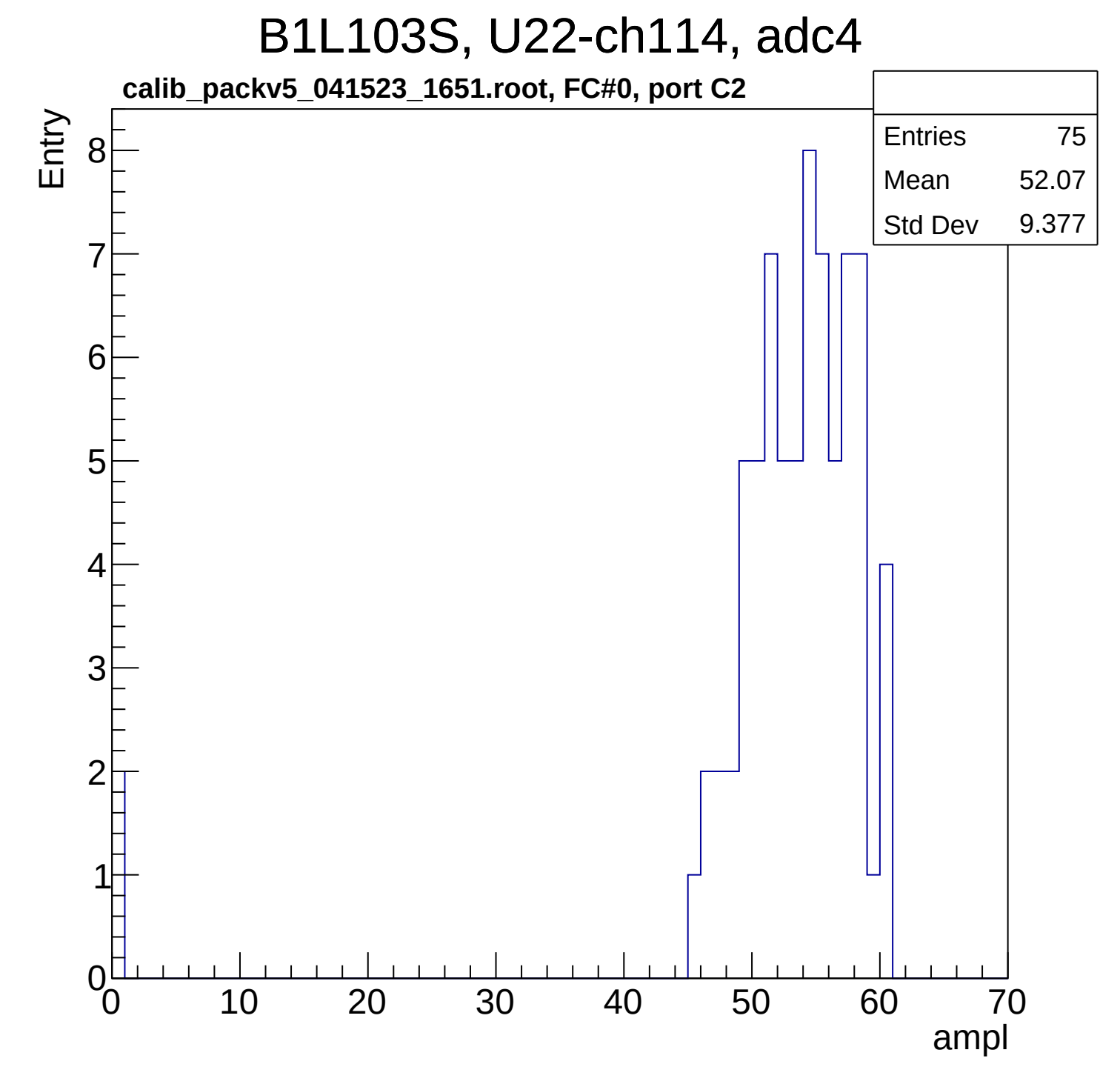
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch114, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 52.07
Std Dev 9.377
Entry
ampl
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2
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4
5
6
7
8
0
10
20
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40
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60
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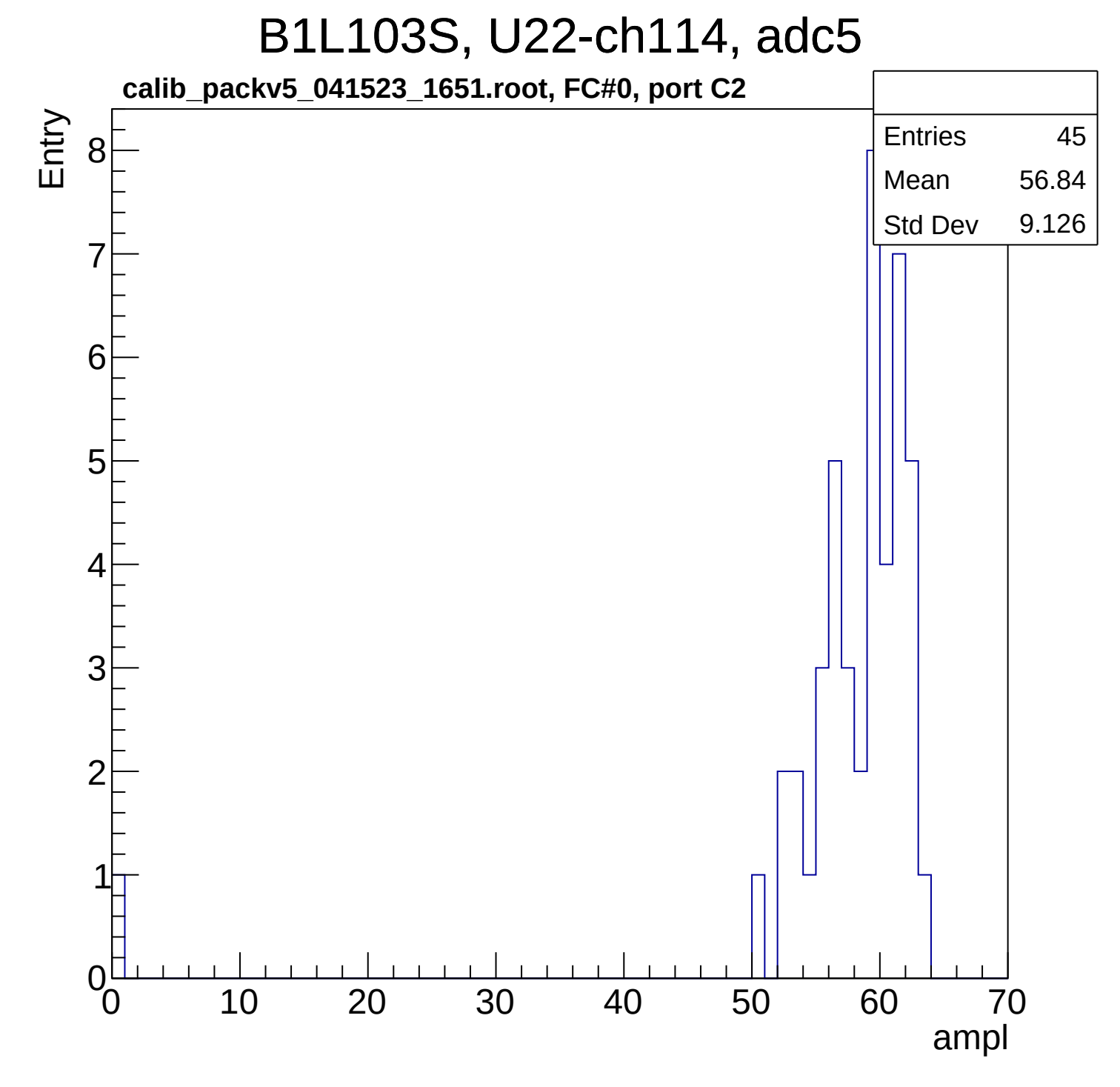
B1L103S, U22-ch114, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 56.84
Std Dev 9.126
Entry
ampl
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4
5
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7
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0
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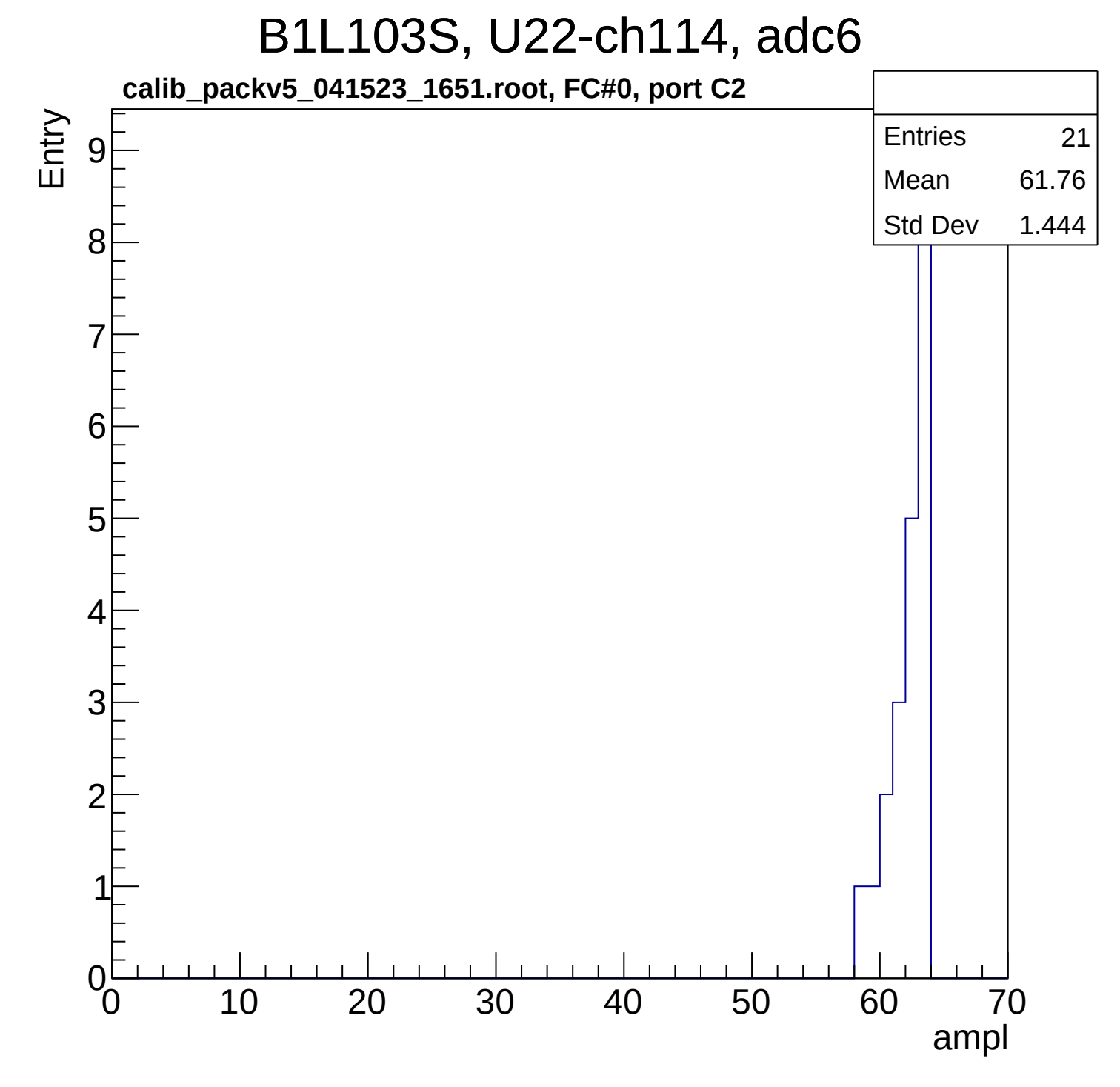
B1L103S, U22-ch114, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 61.76
Std Dev 1.444
Entry
ampl
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3
4
5
6
7
8
9
0
10
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40
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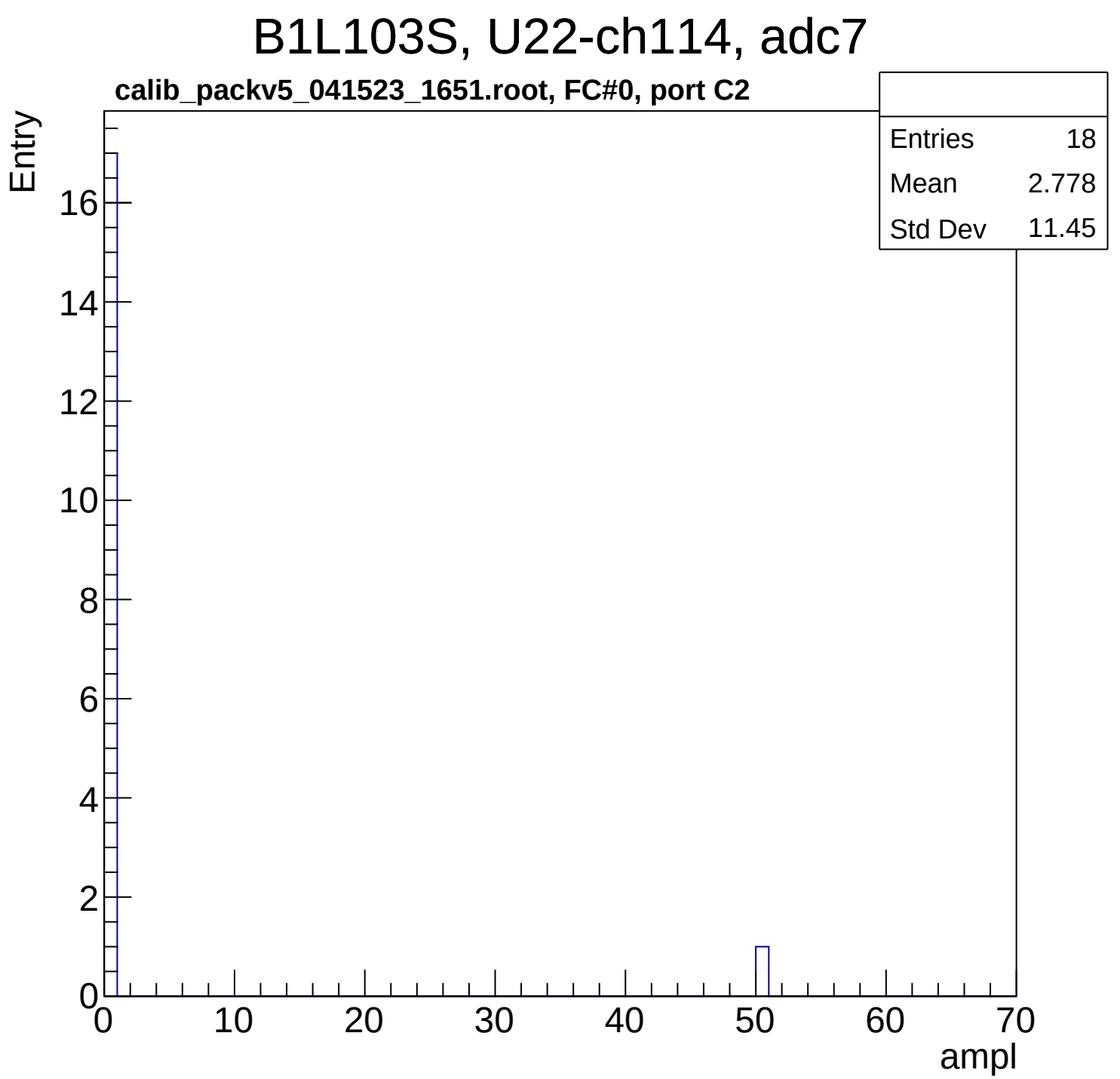
60
70


B1L103S, U22-ch114, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 2.778
Std Dev 11.45
Entry
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4
6
8
10
12
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16
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10
20
30
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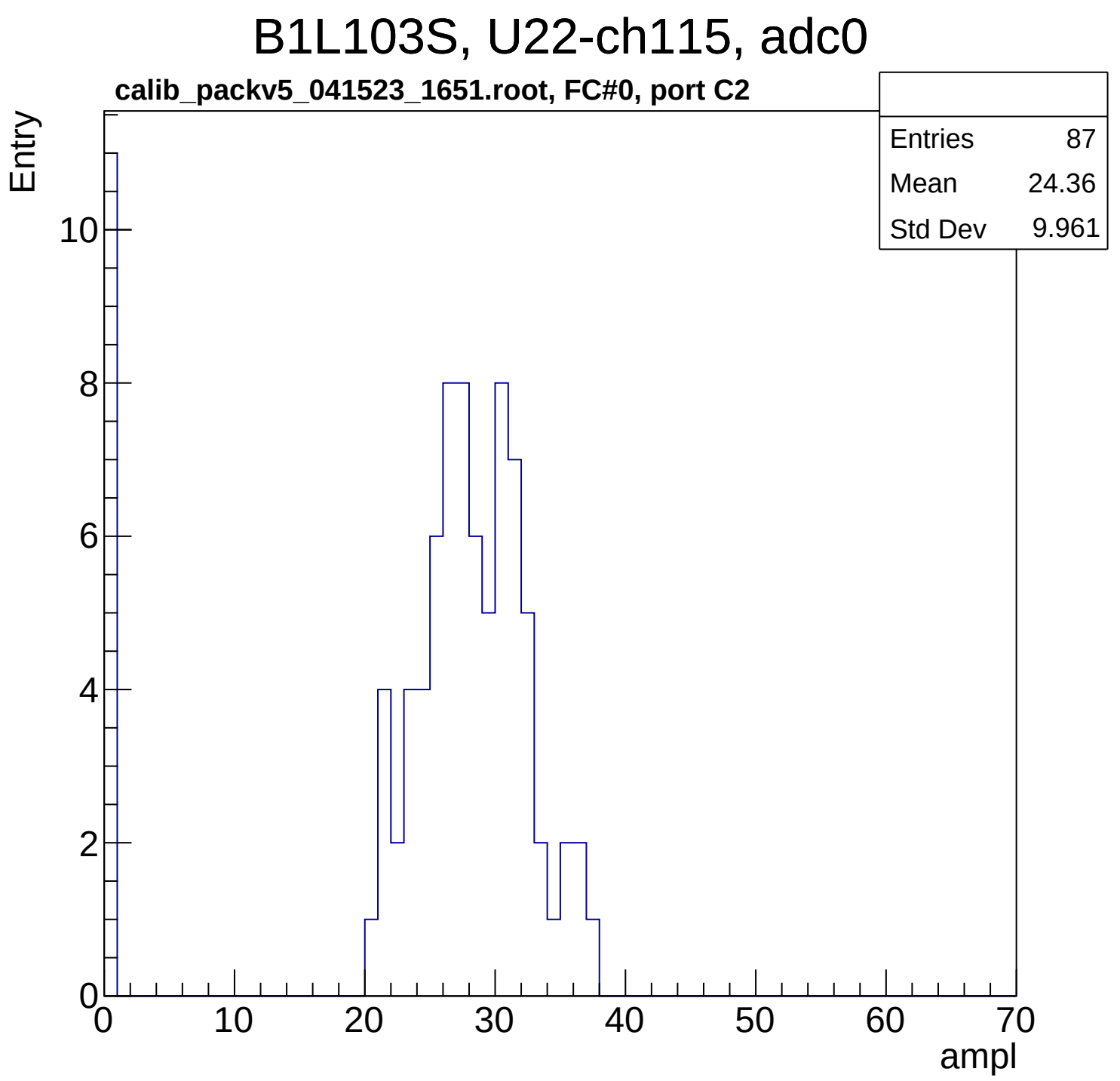
50
60
70
ampl


B1L103S, U22-ch115, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 24.36
Std Dev 9.961
Entry
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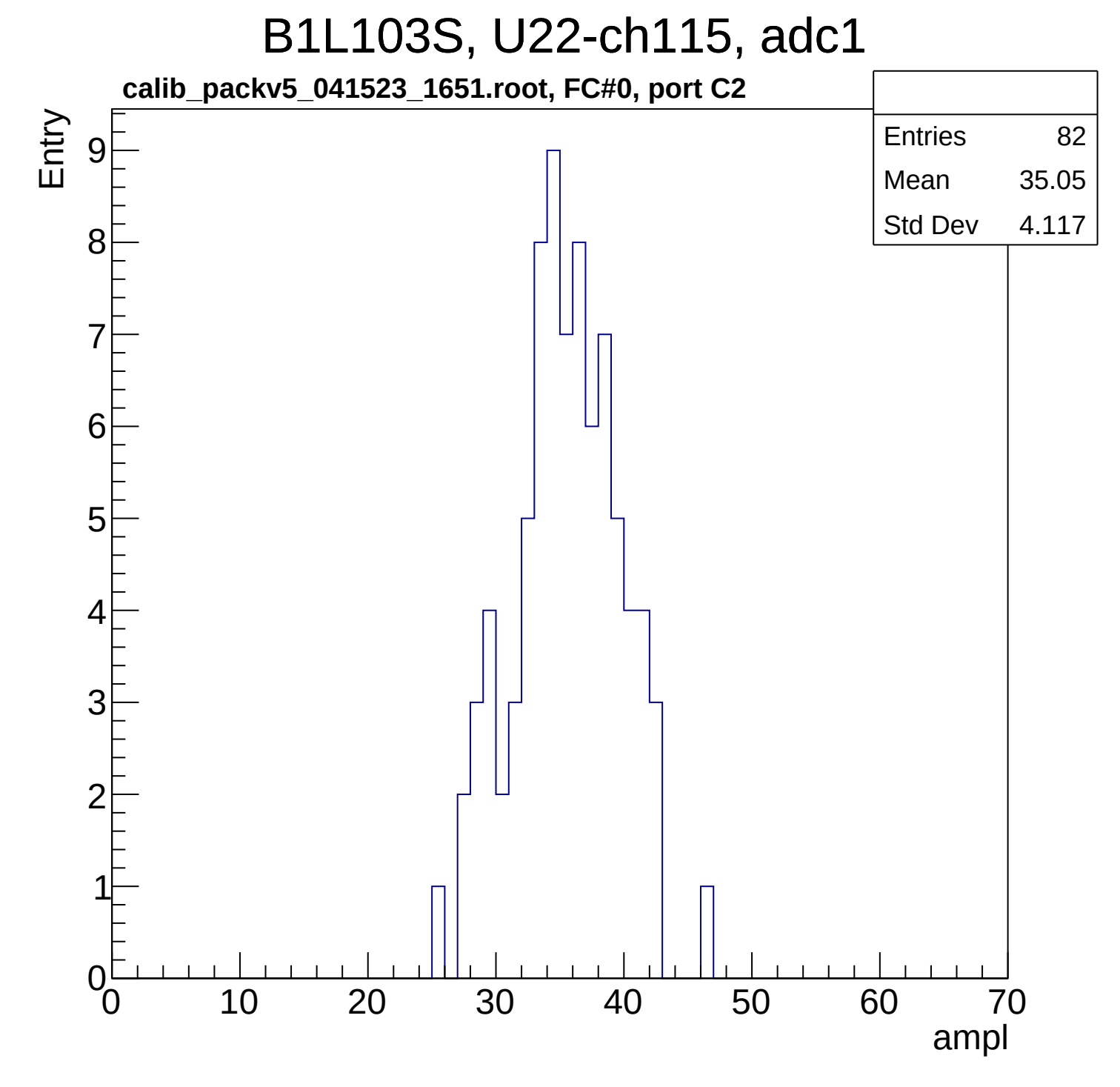
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch115, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 35.05
Std Dev 4.117
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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60
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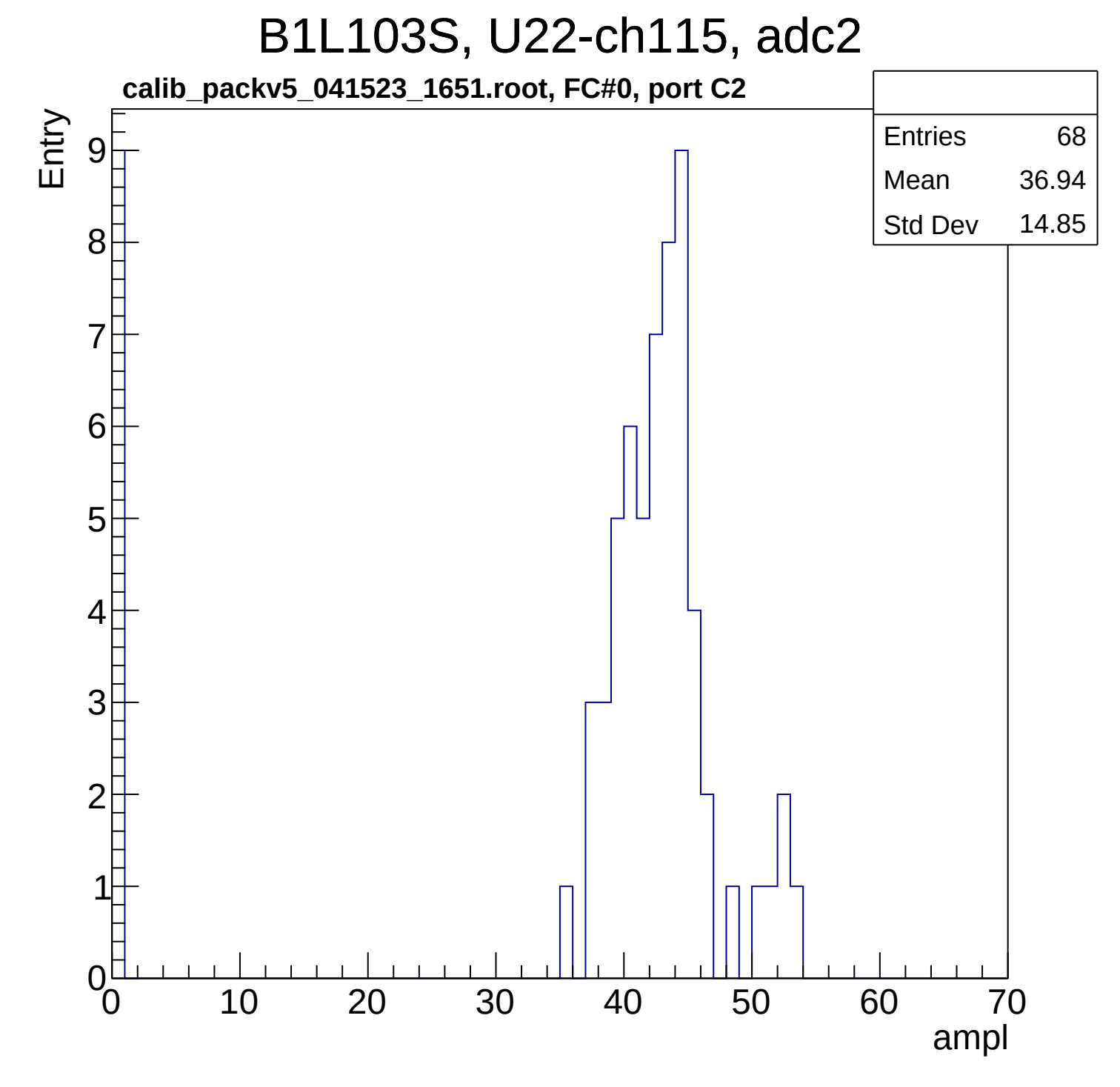
B1L103S, U22-ch115, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 36.94
Std Dev 14.85
Entry
ampl
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2
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4
5
6
7
8
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0
10
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40
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60
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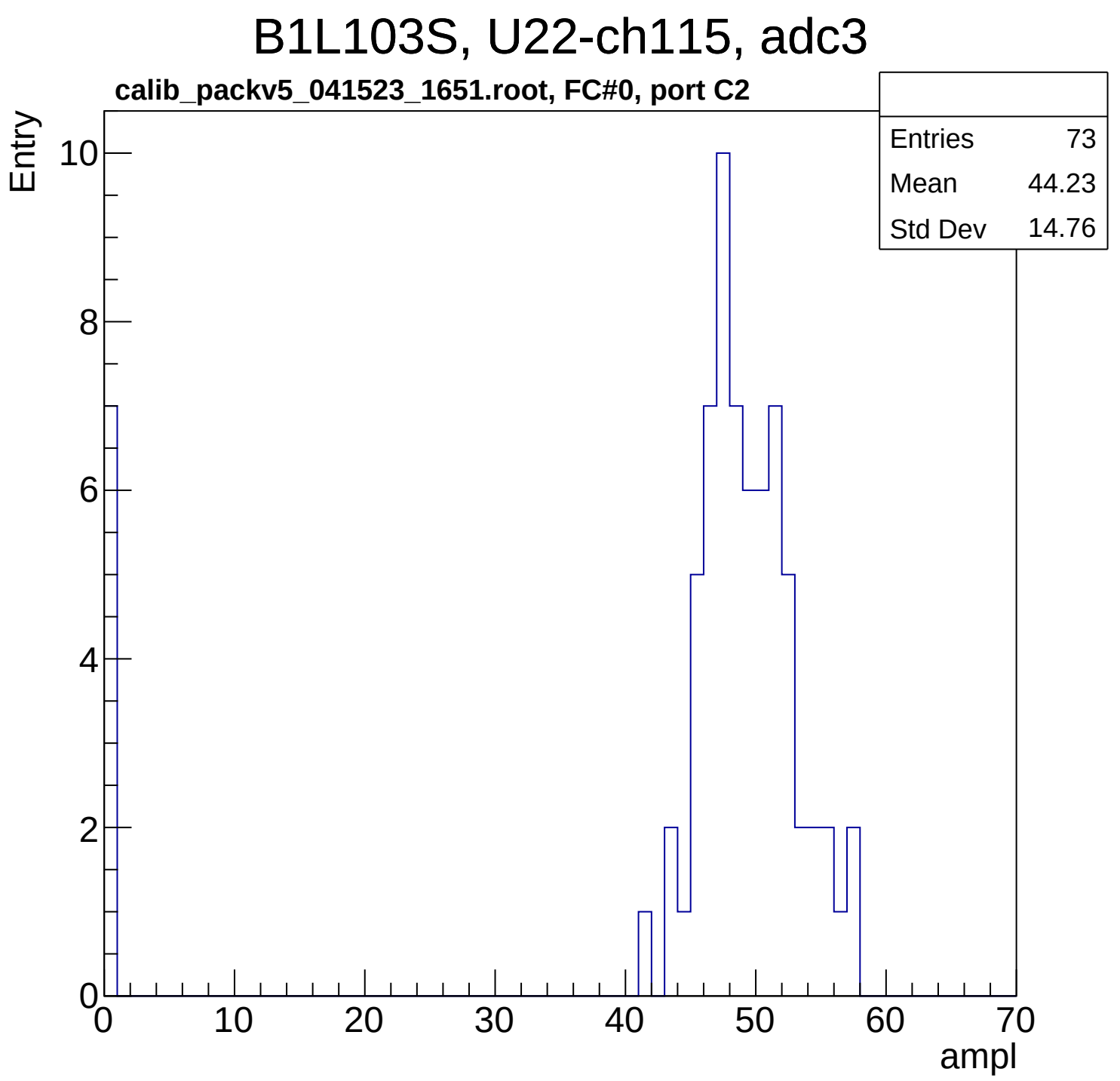
B1L103S, U22-ch115, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 44.23
Std Dev 14.76
Entry
ampl
0
2
4
6
8
10
0
10
20
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40
50
60
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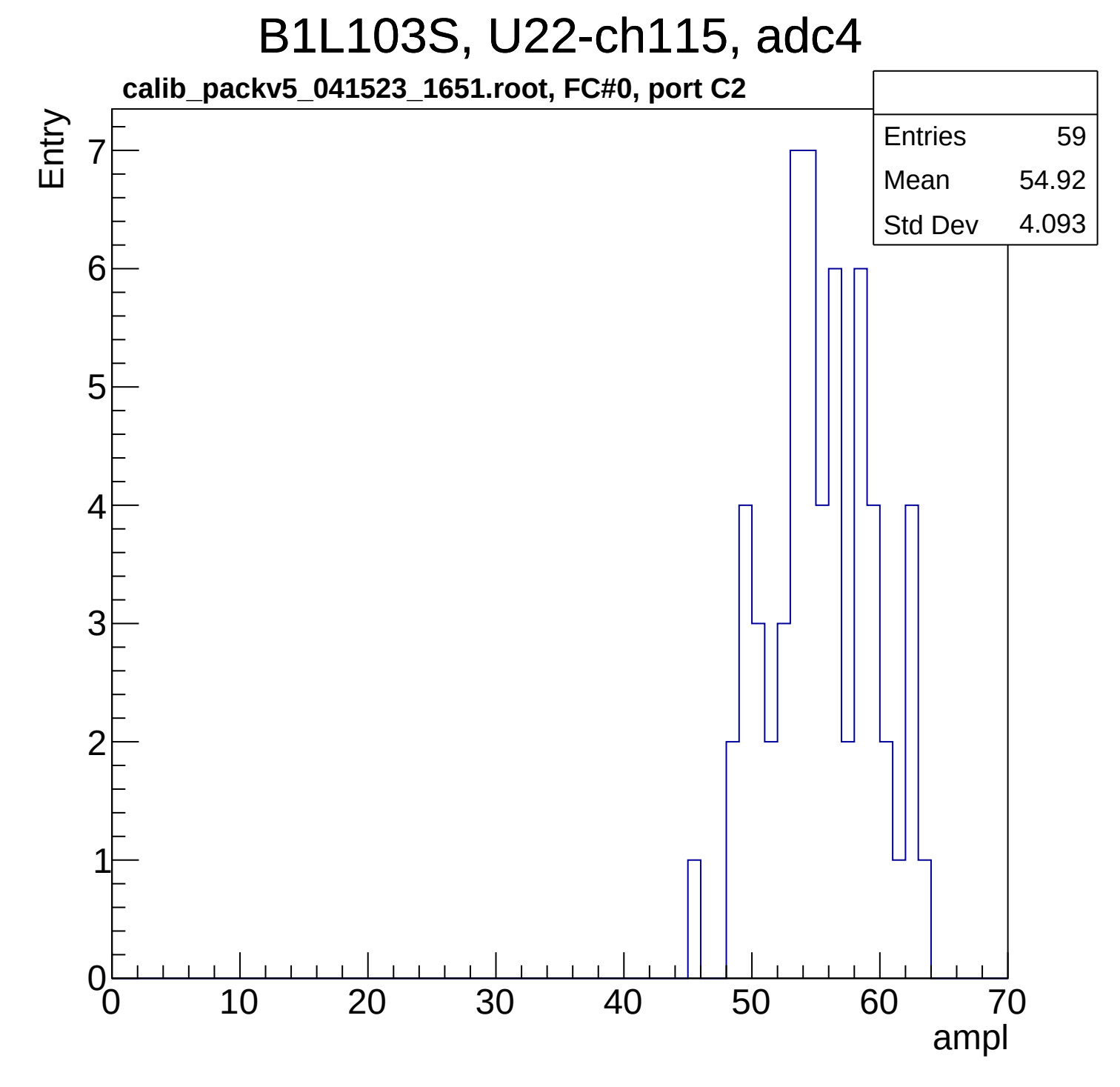
B1L103S, U22-ch115, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 54.92
Std Dev 4.093
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
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40
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60
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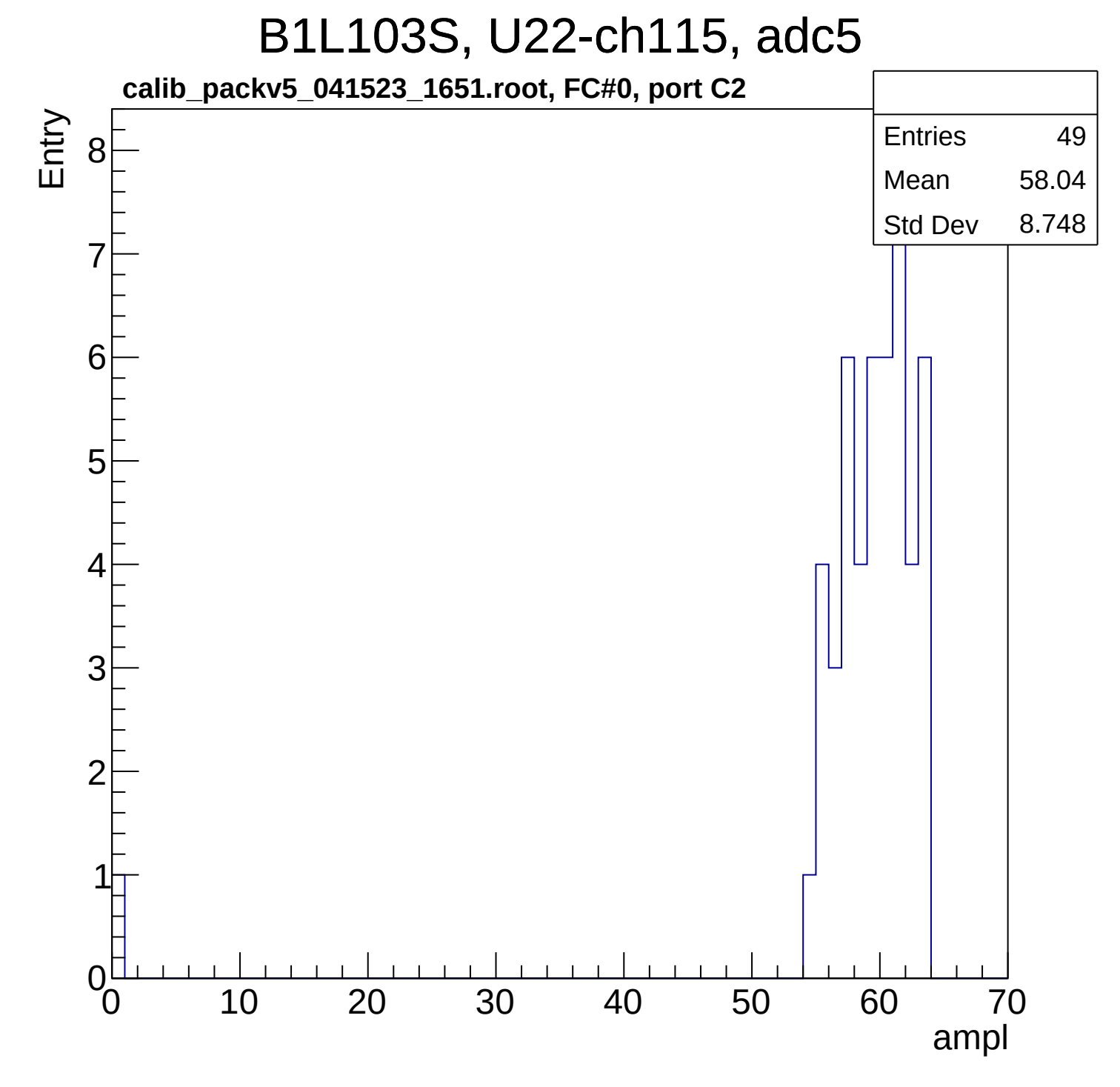
B1L103S, U22-ch115, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 58.04
Std Dev 8.748
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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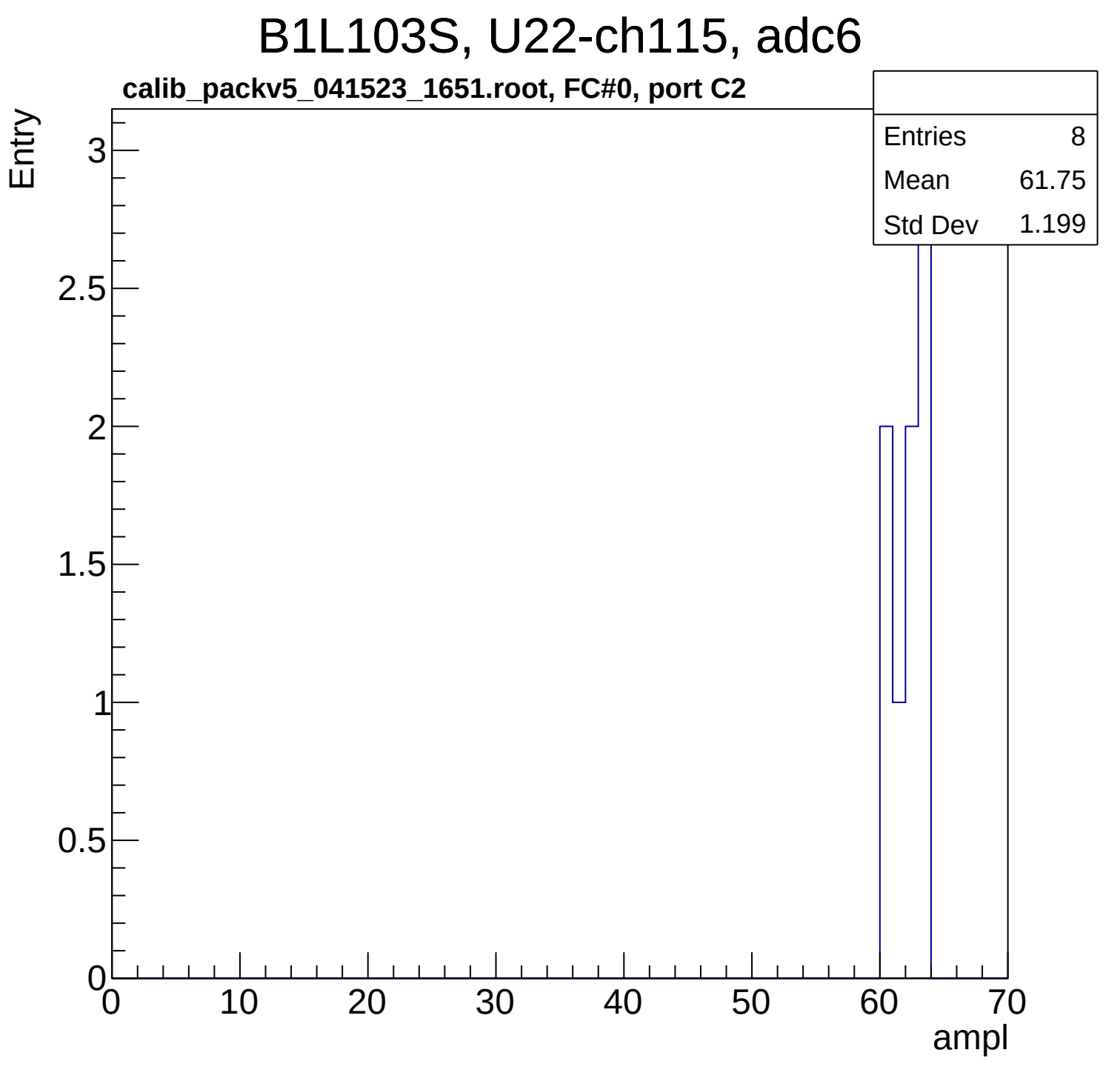
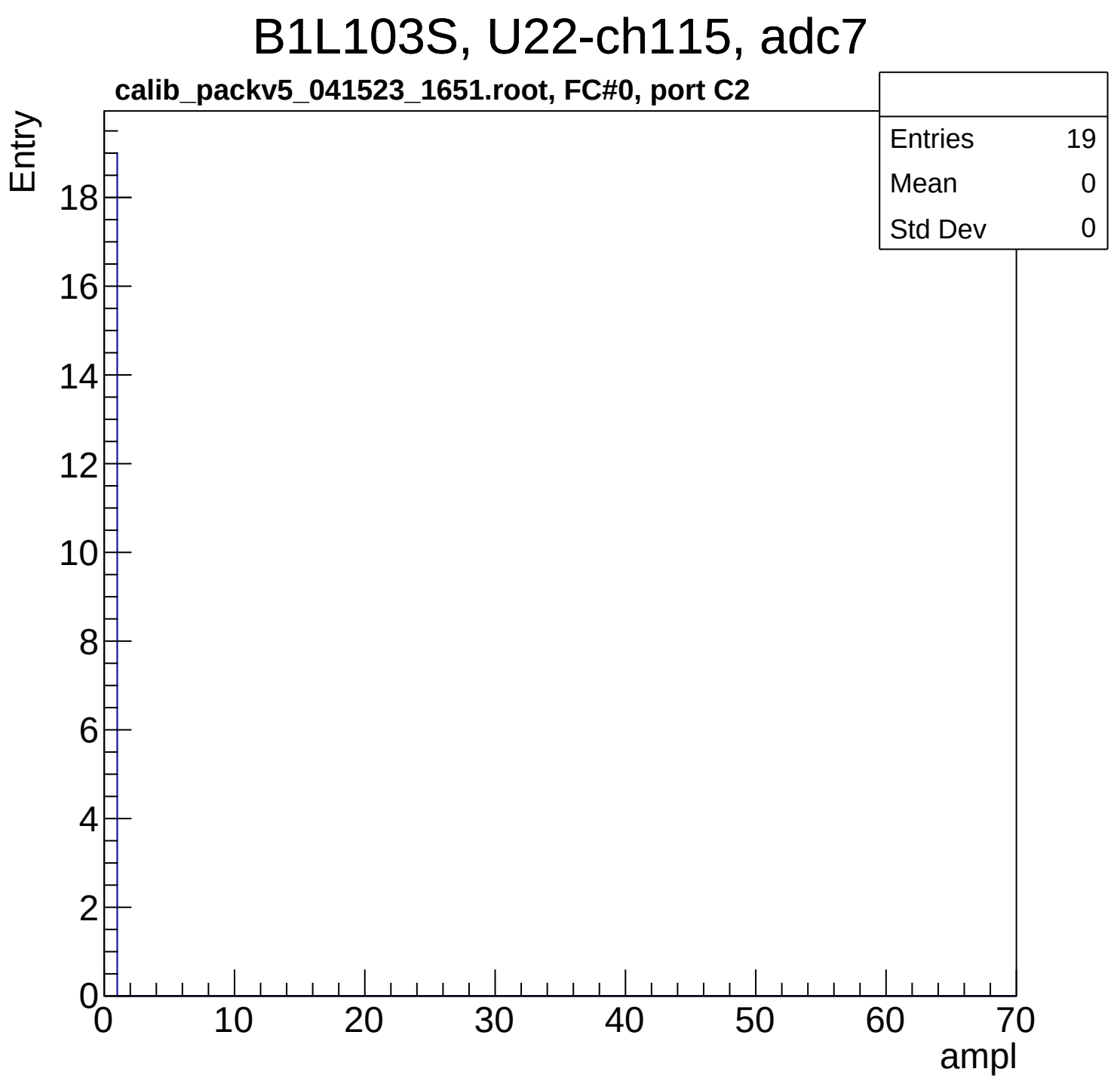
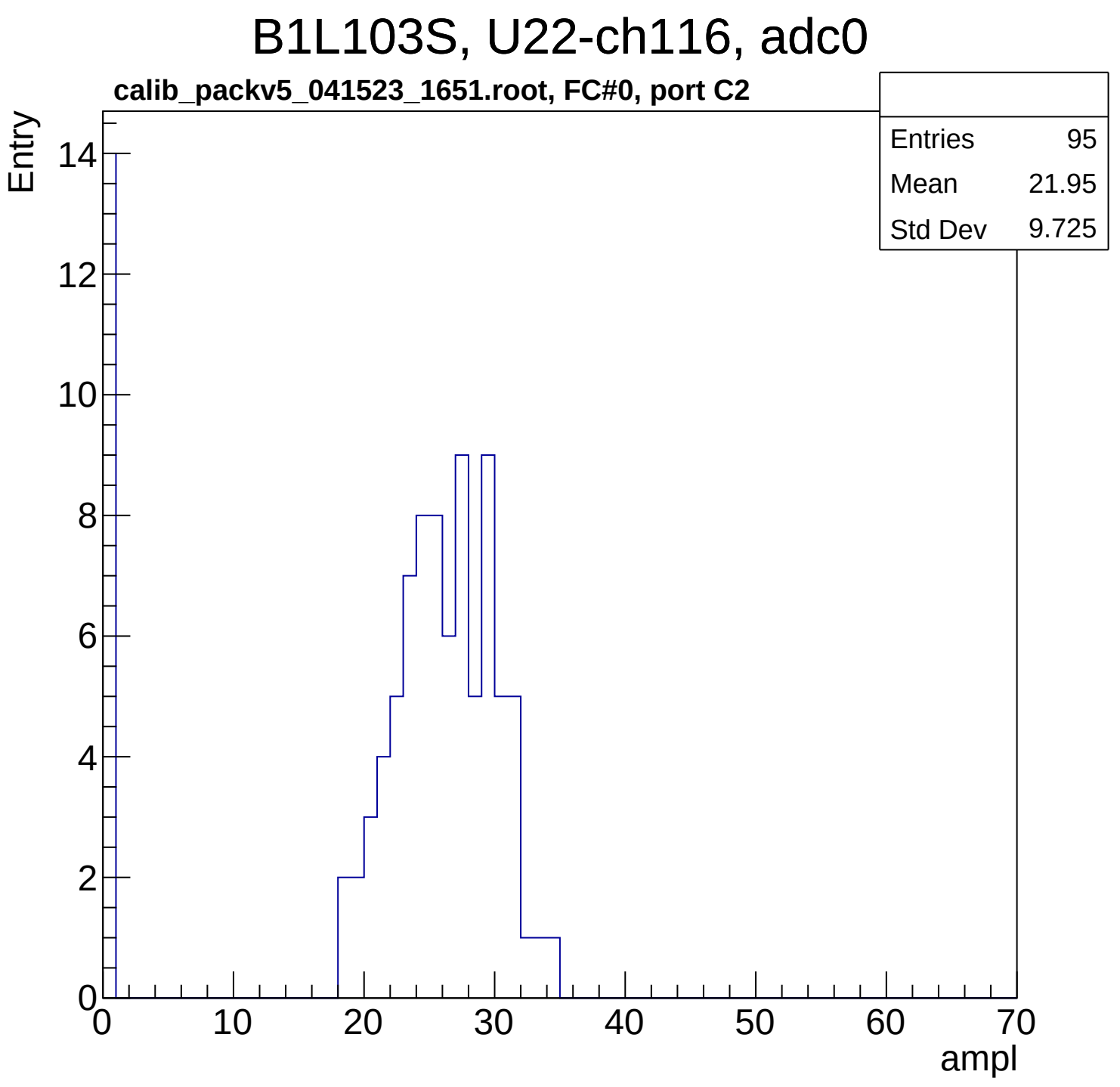
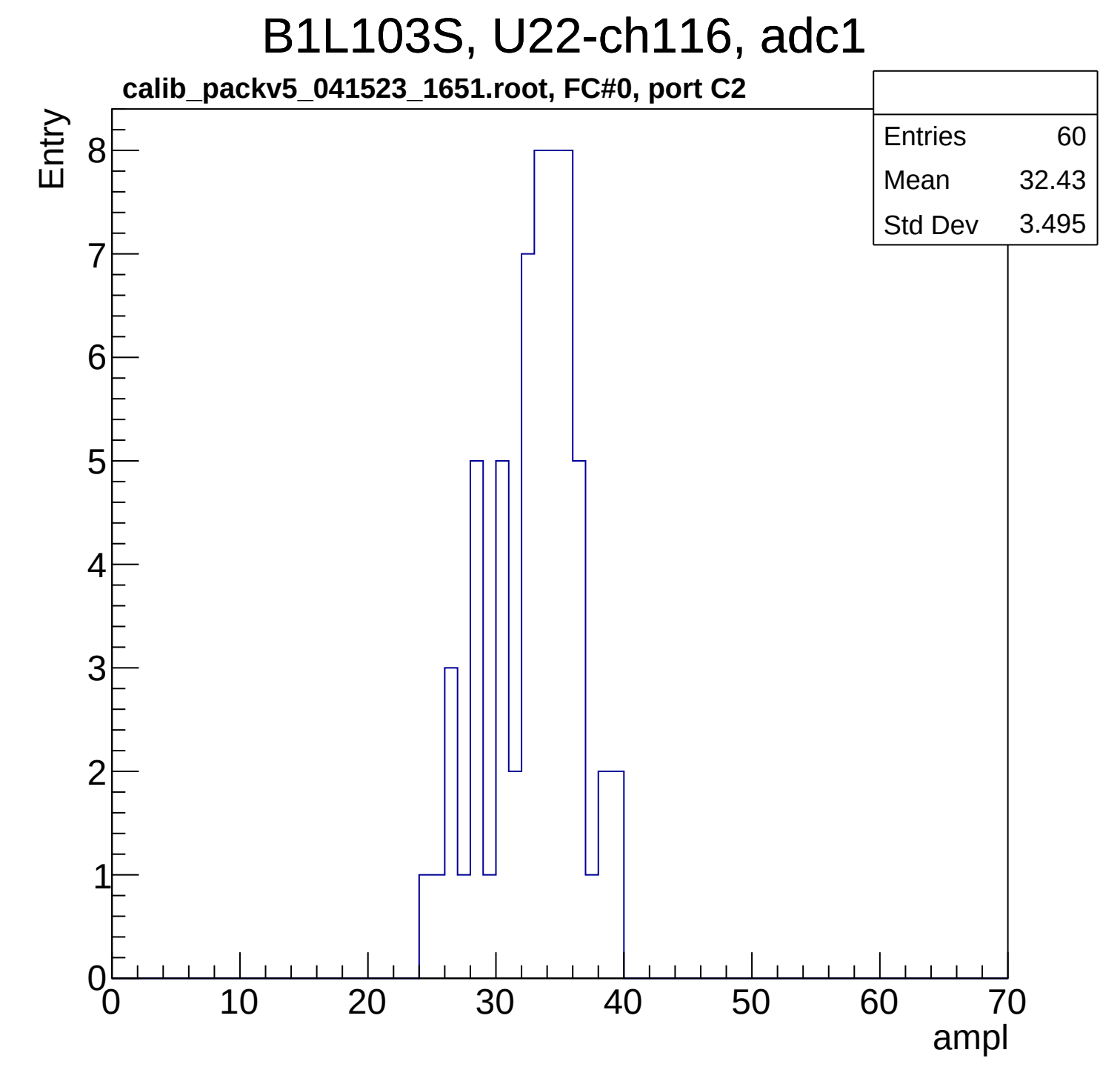
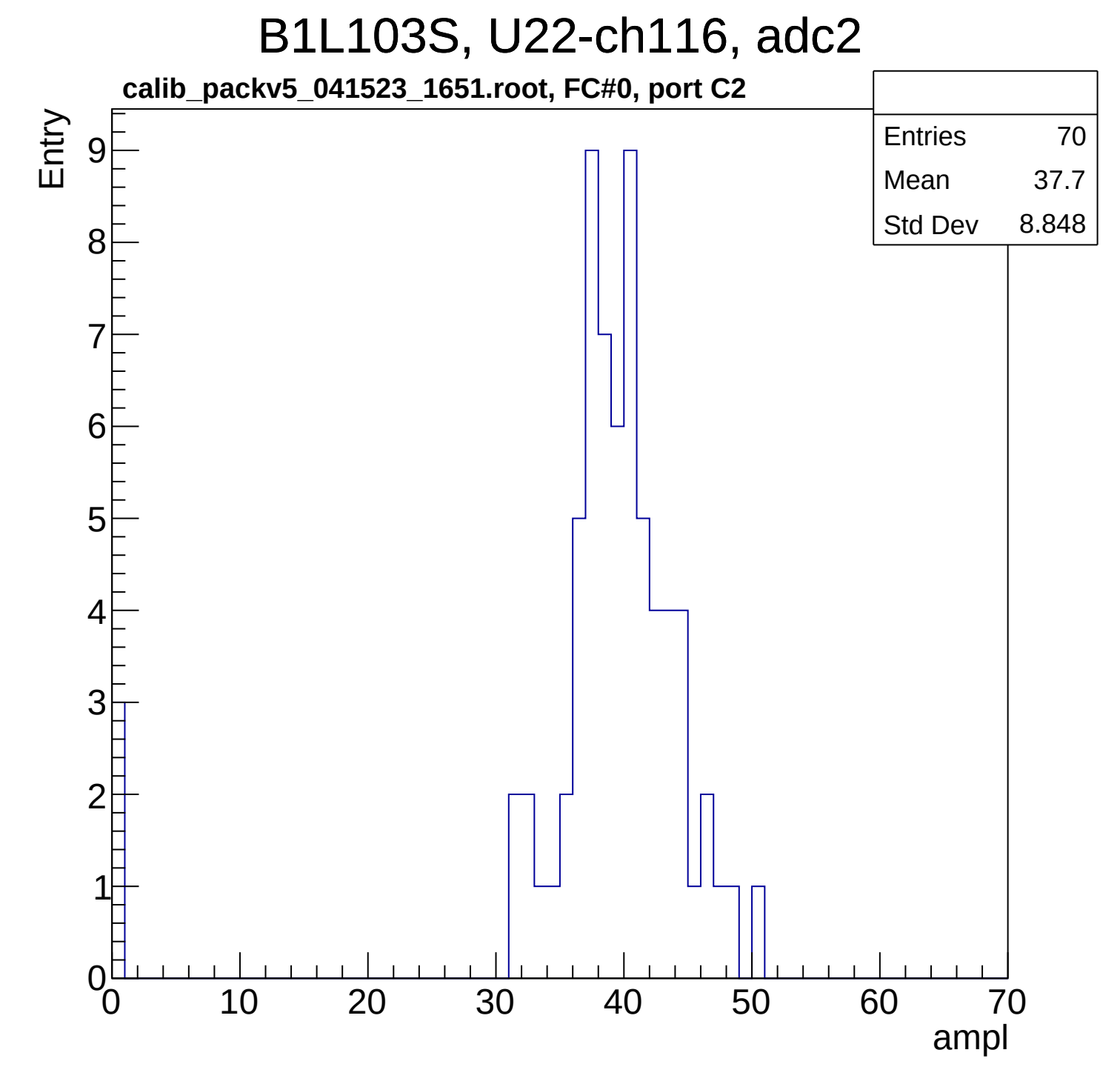

B1L103S, U22-ch115, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 61.75
Std Dev 1.199
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U22-ch115, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch116, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 21.95
Std Dev 9.725
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch116, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 32.43
Std Dev 3.495
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch116, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 37.7
Std Dev 8.848
Entry
ampl
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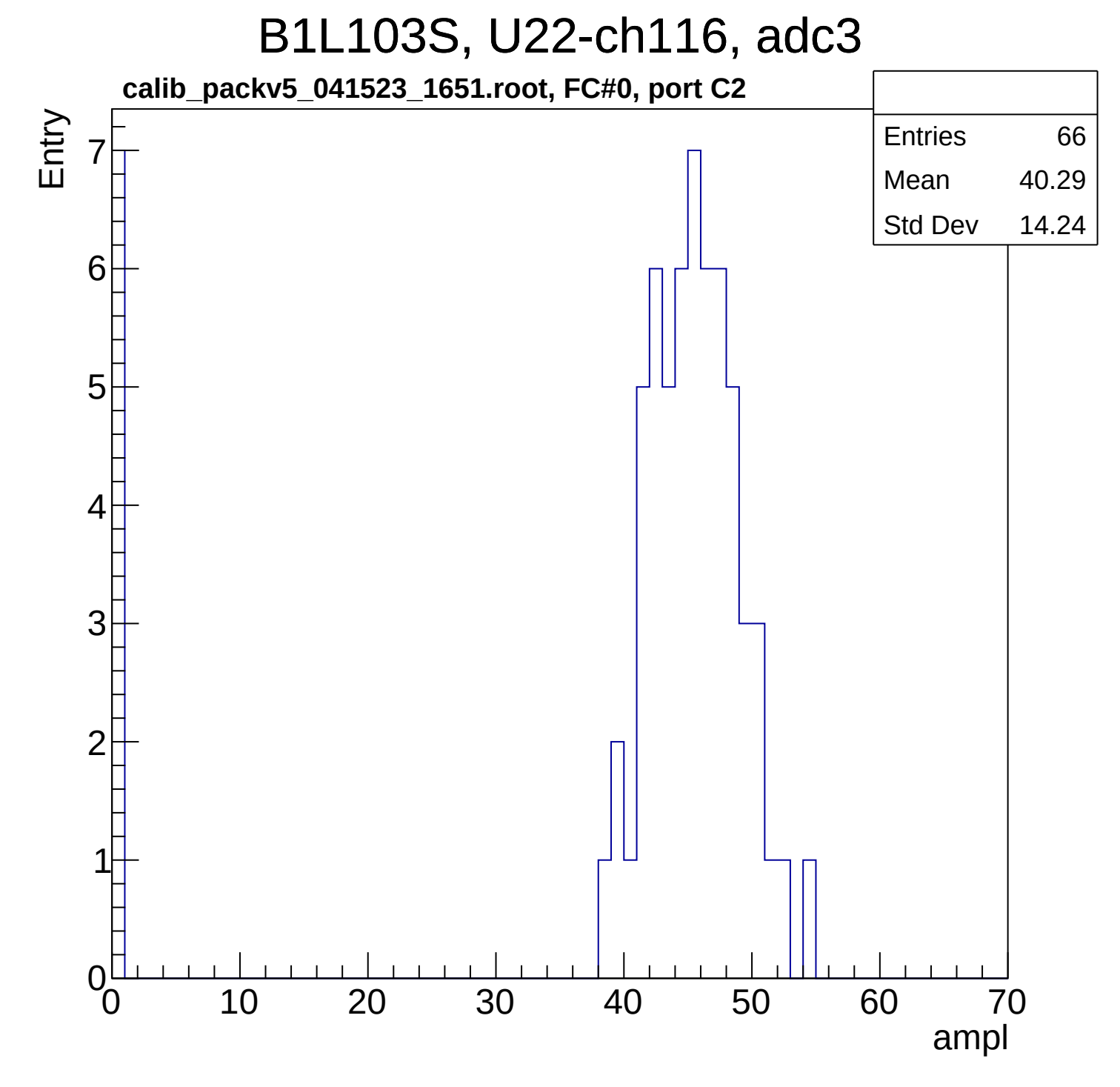
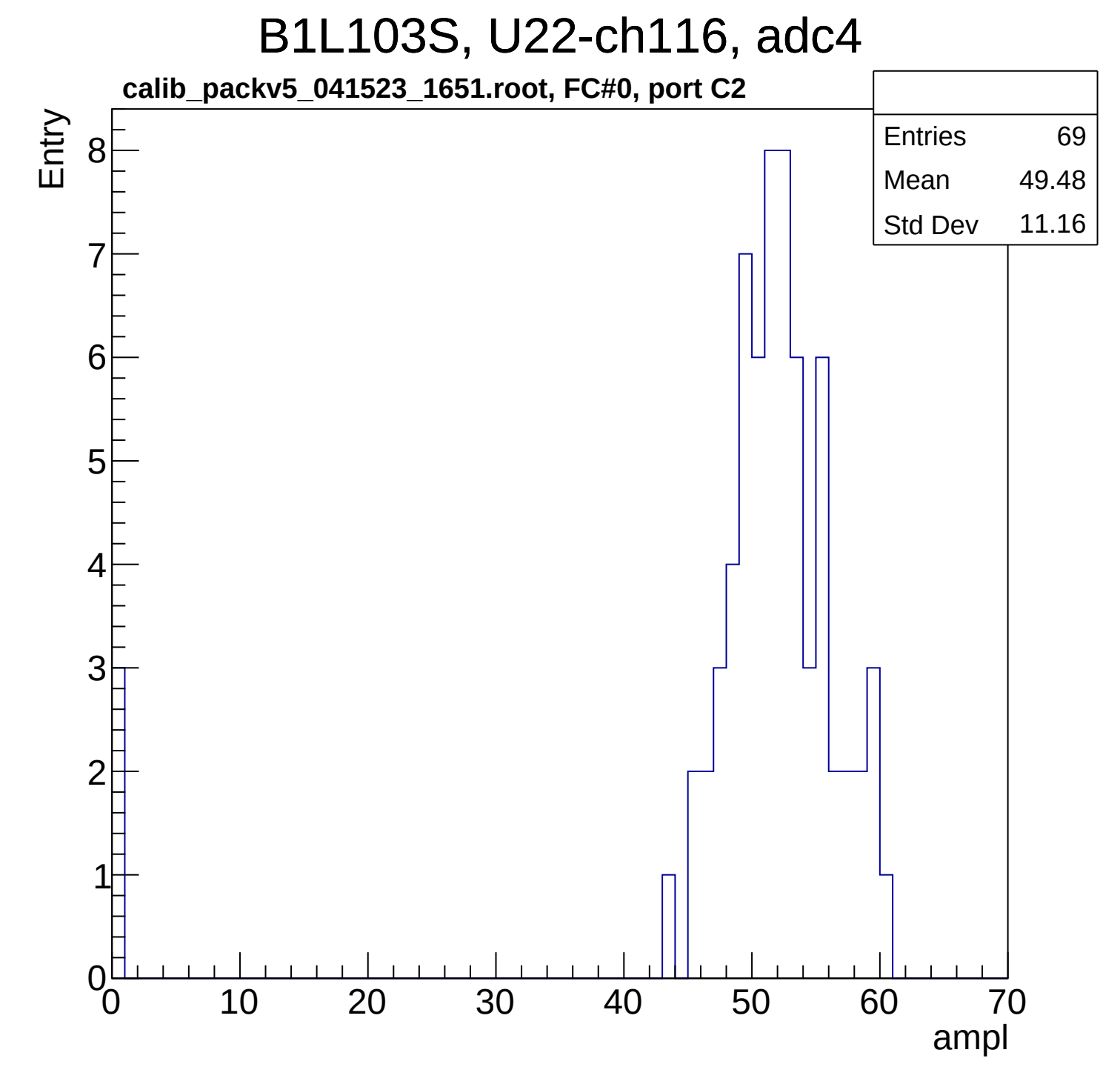
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch116, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 40.29
Std Dev 14.24
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U22-ch116, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 49.48
Std Dev 11.16
Entry
ampl
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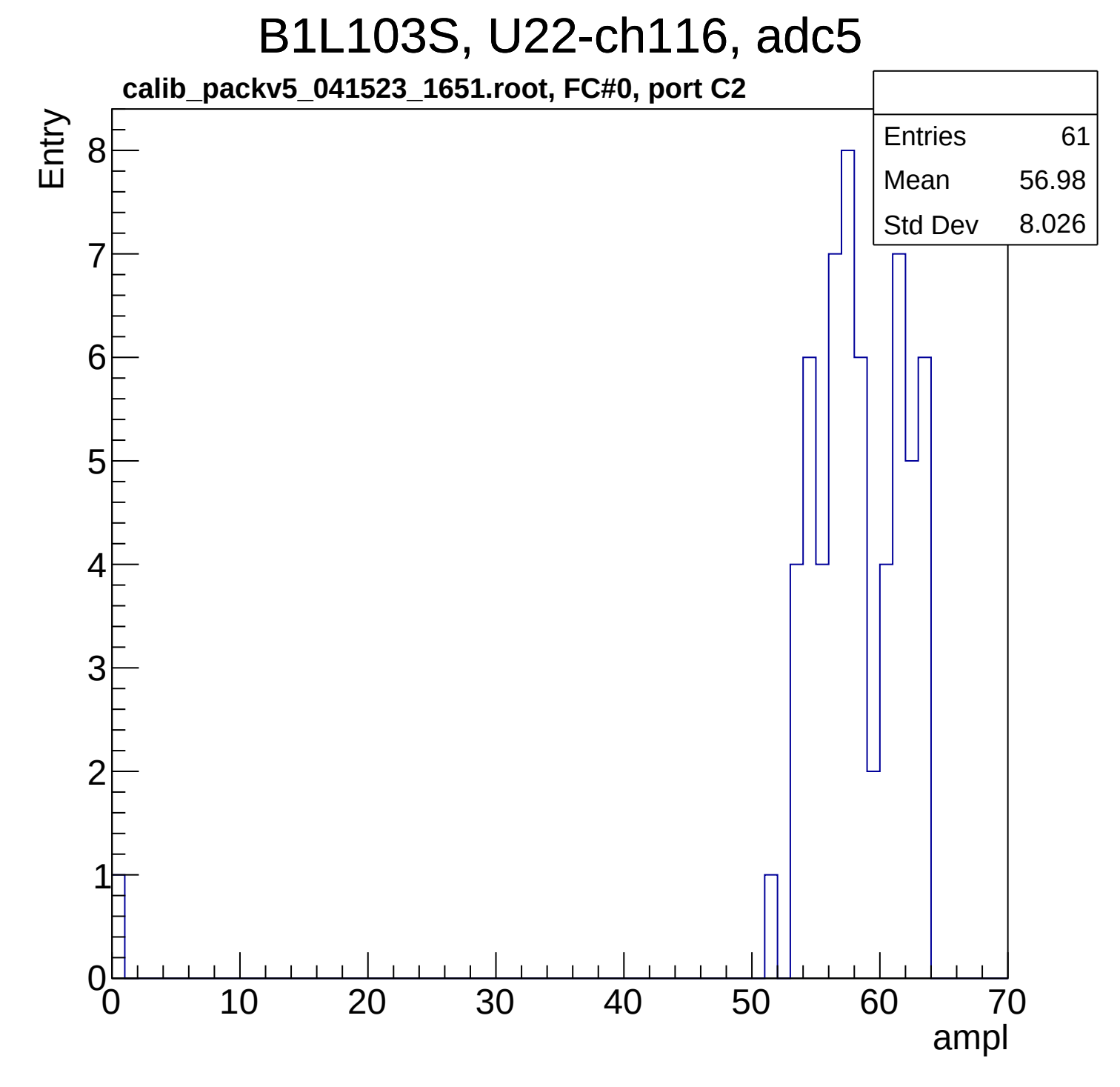
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch116, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 56.98
Std Dev 8.026
Entry
ampl
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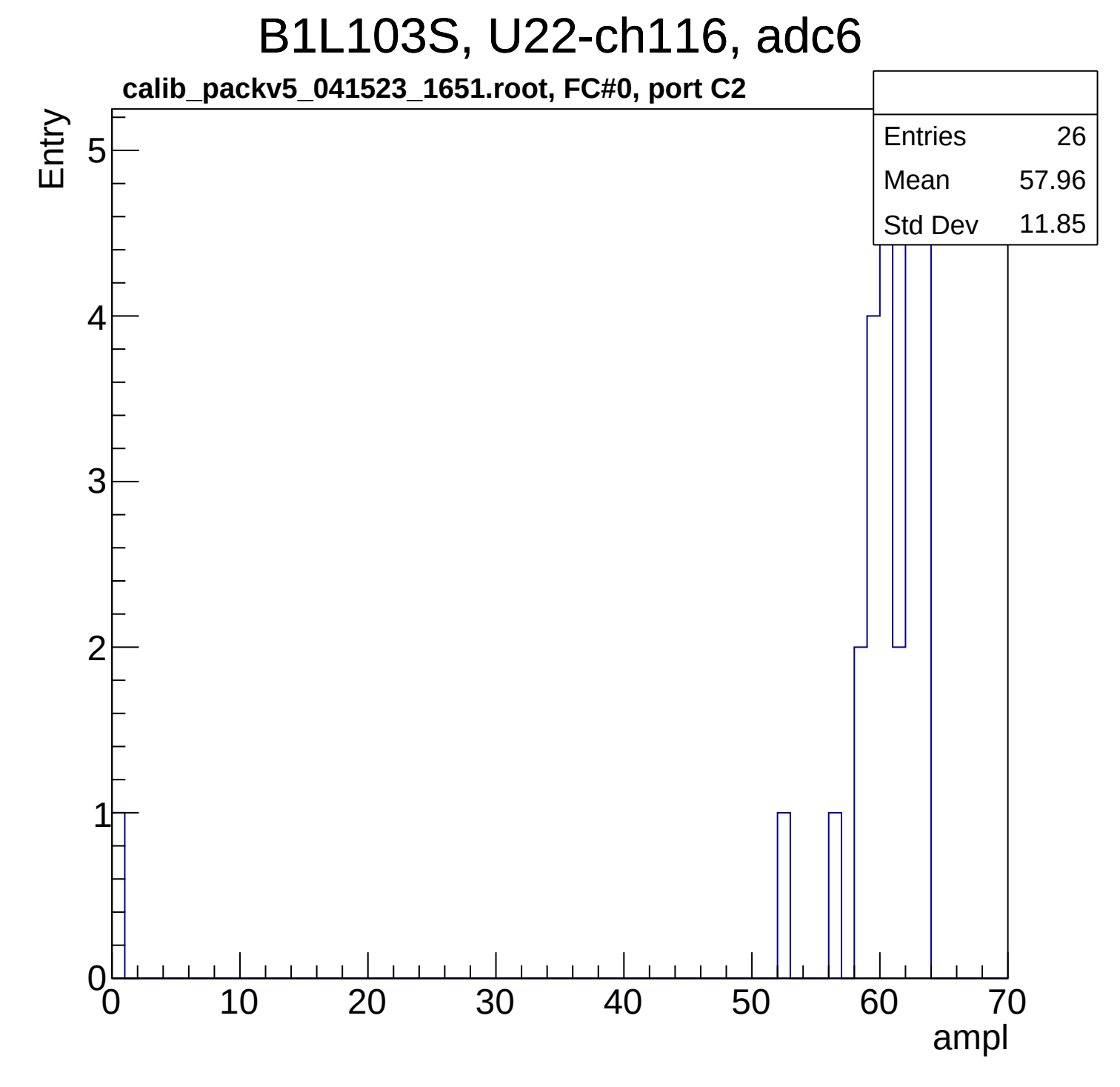
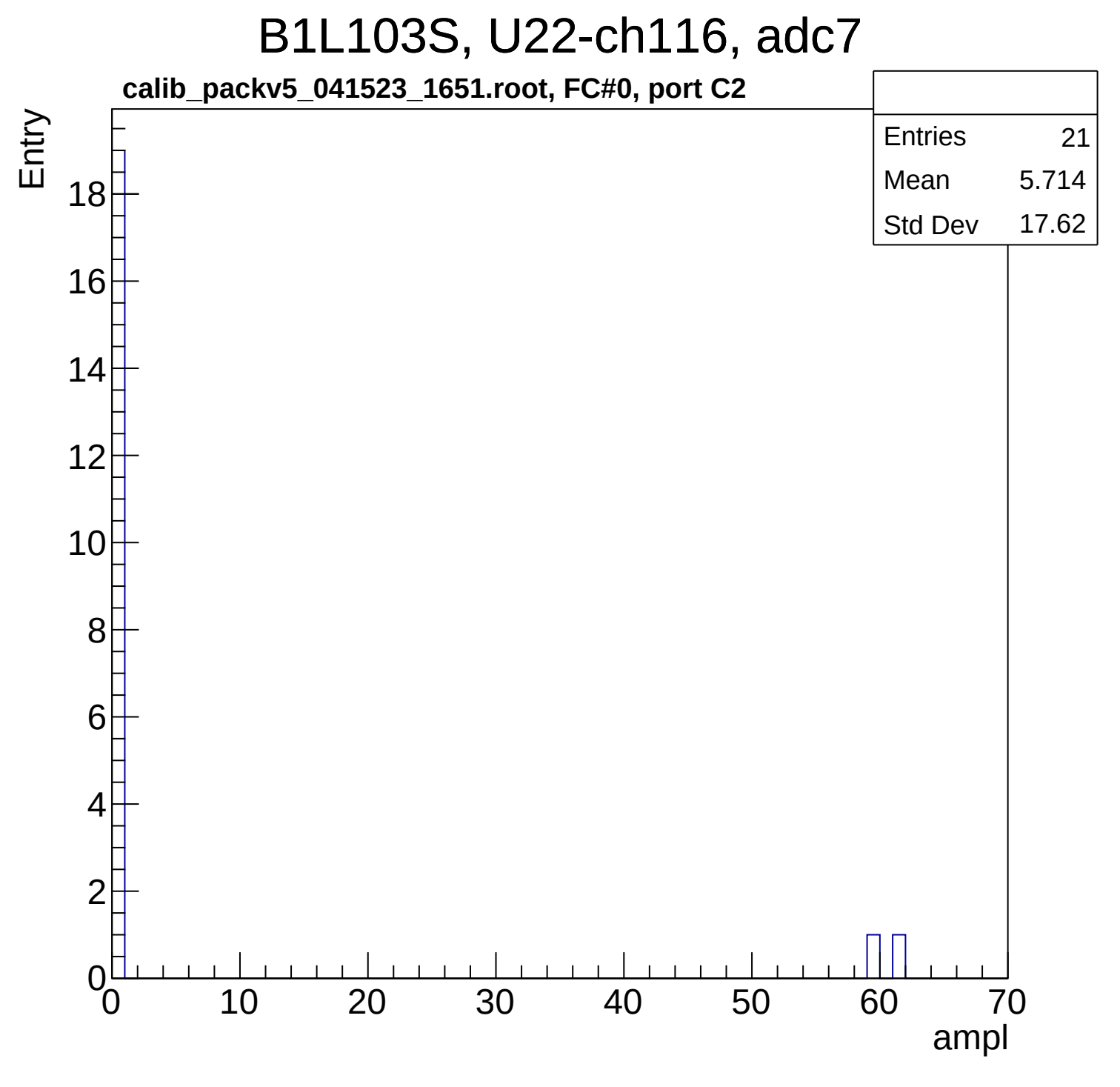
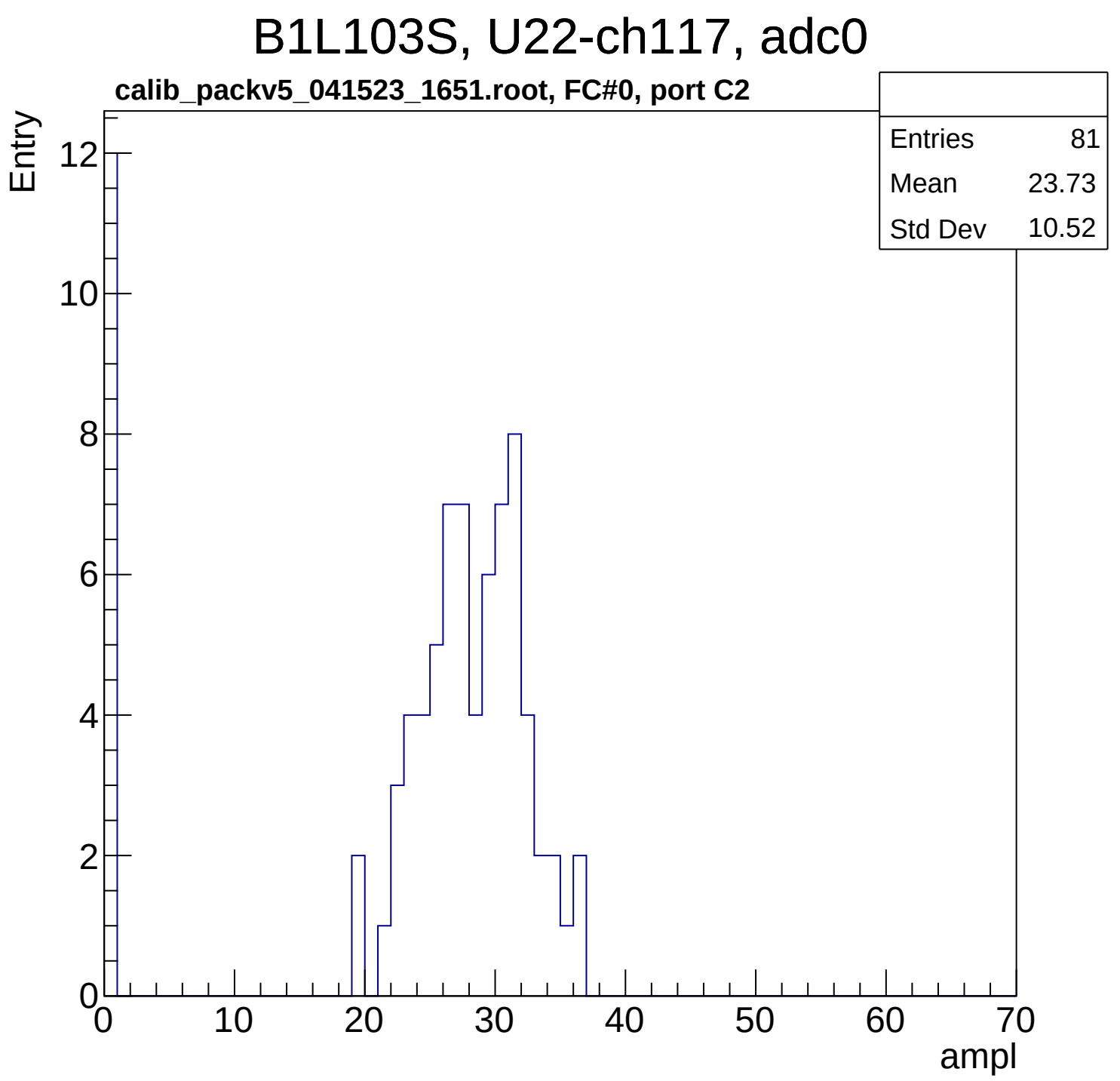
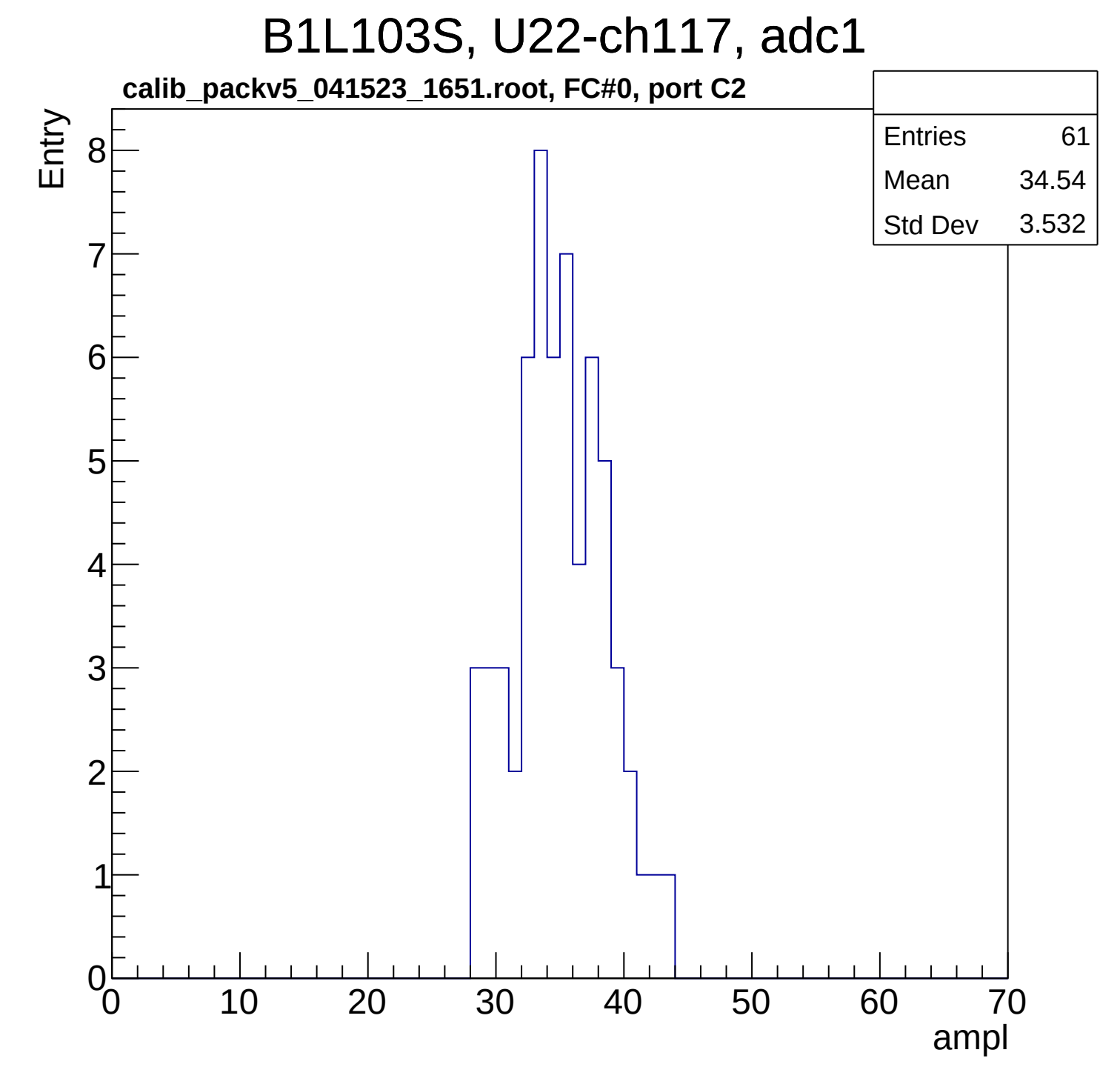
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch116, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 57.96
Std Dev 11.85
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U22-ch116, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.714
Std Dev 17.62
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch117, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 23.73
Std Dev 10.52
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U22-ch117, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 34.54
Std Dev 3.532
Entry
ampl
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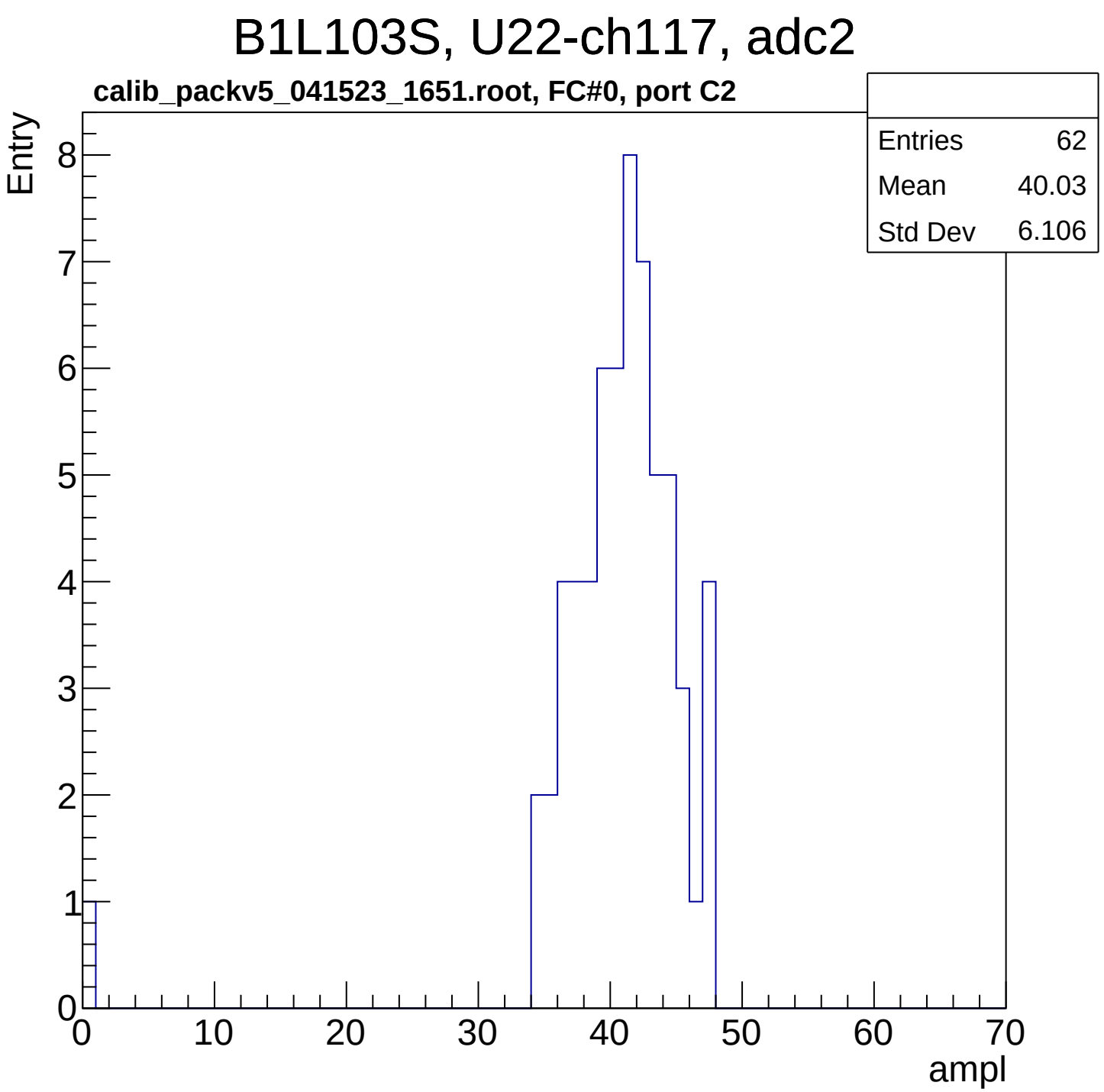
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch117, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 40.03
Std Dev 6.106
Entry
ampl
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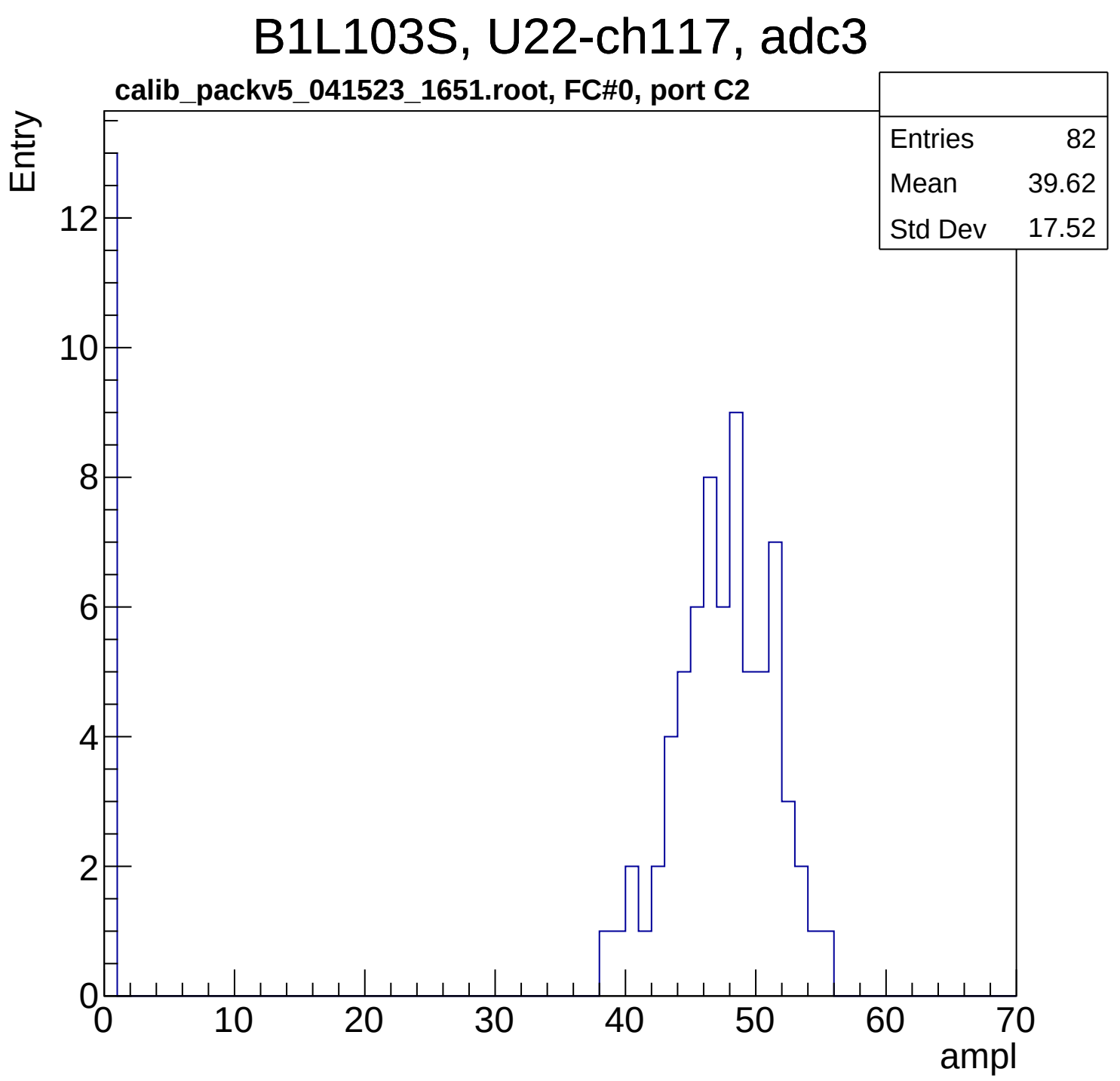
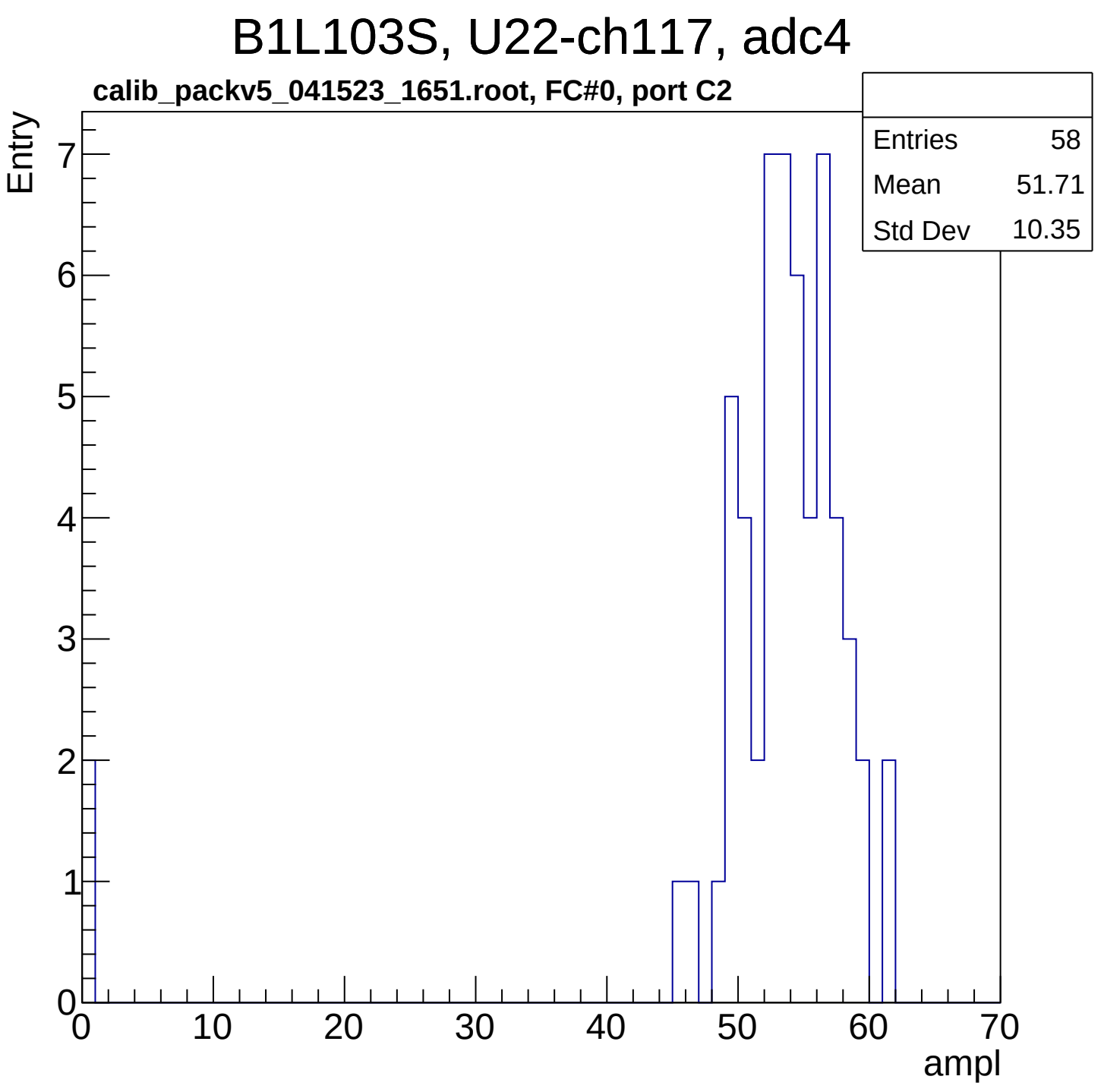
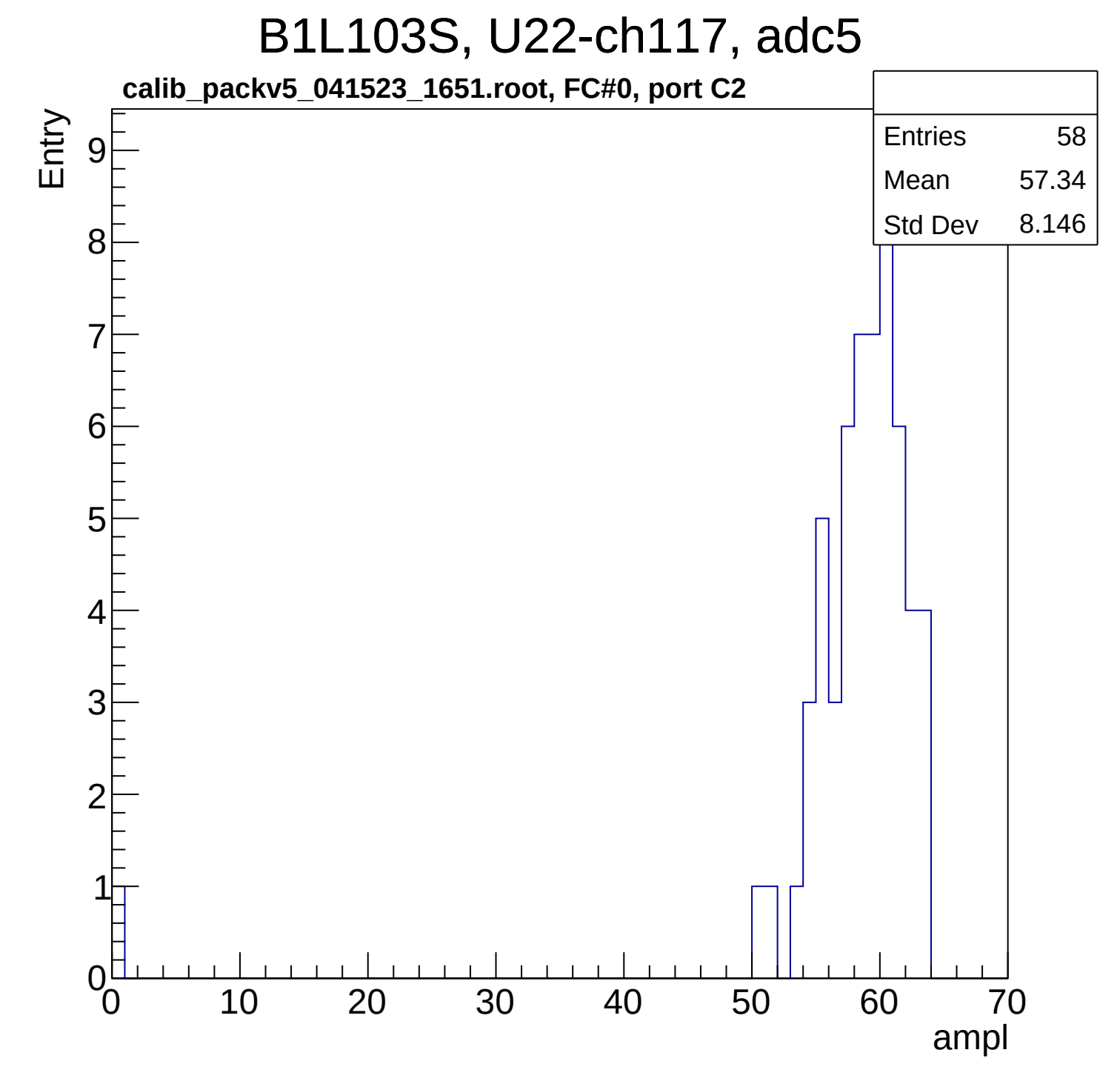
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch117, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 39.62
Std Dev 17.52
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch117, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 51.71
Std Dev 10.35
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U22-ch117, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 57.34
Std Dev 8.146
Entry
ampl
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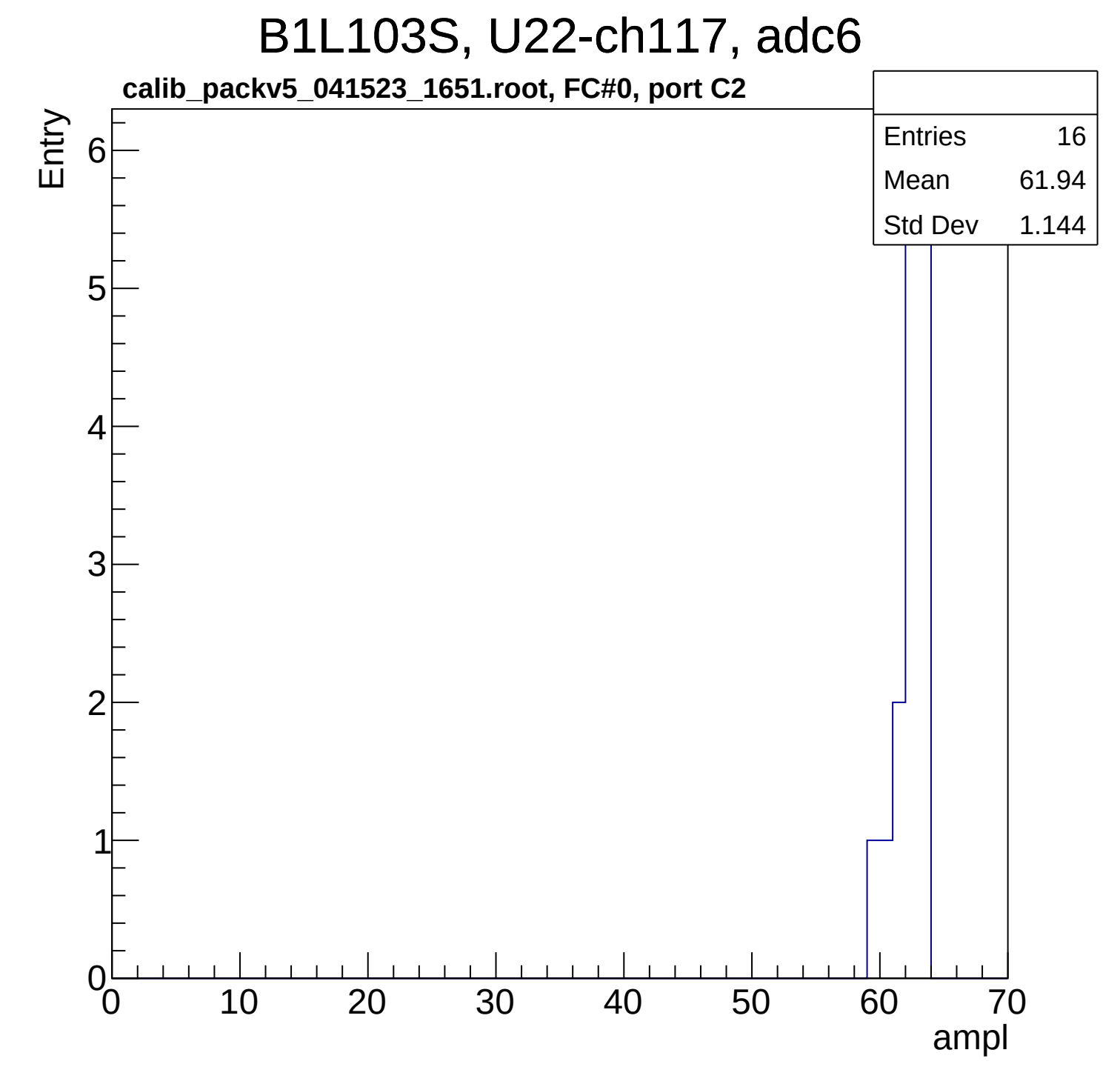
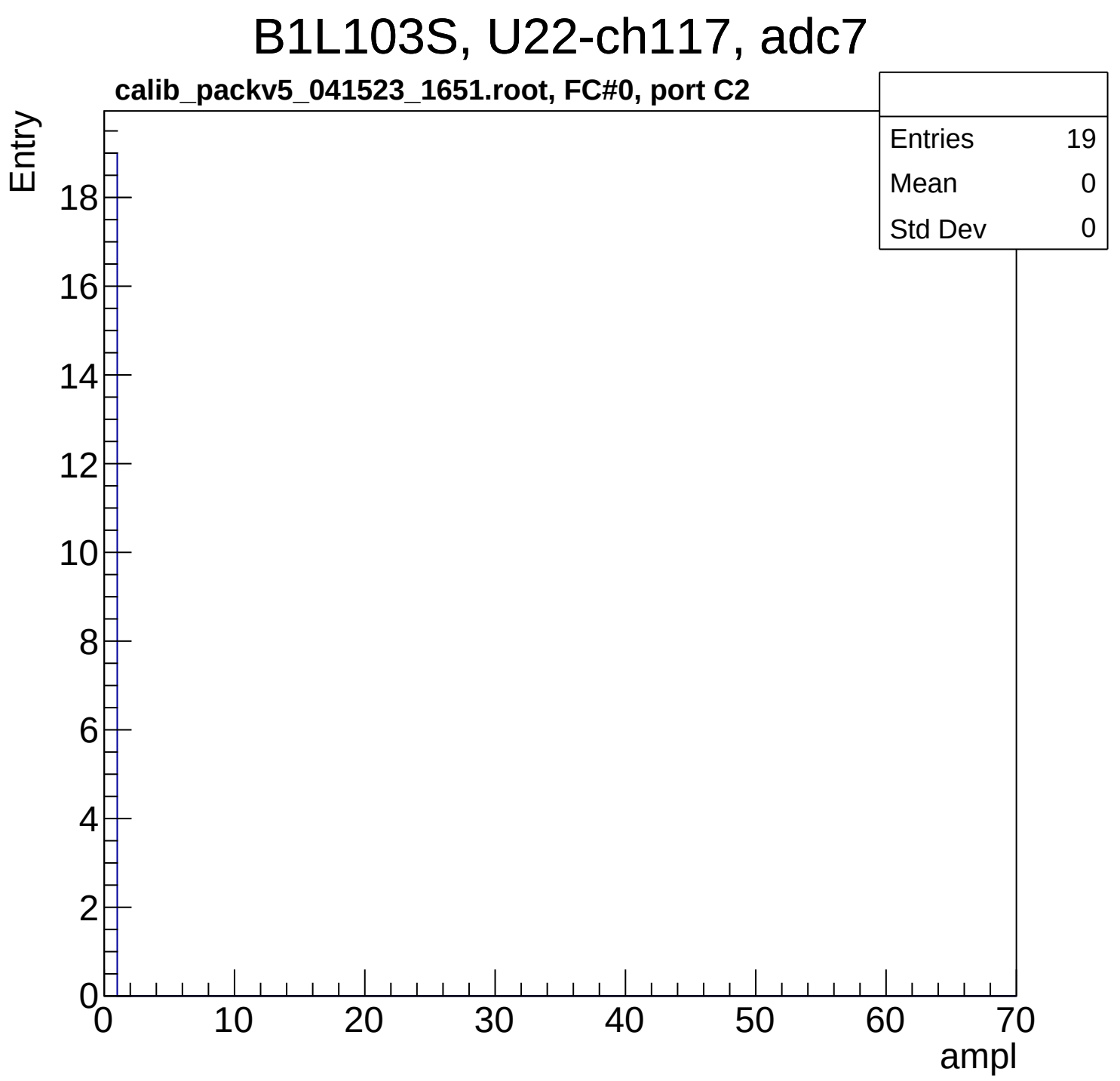
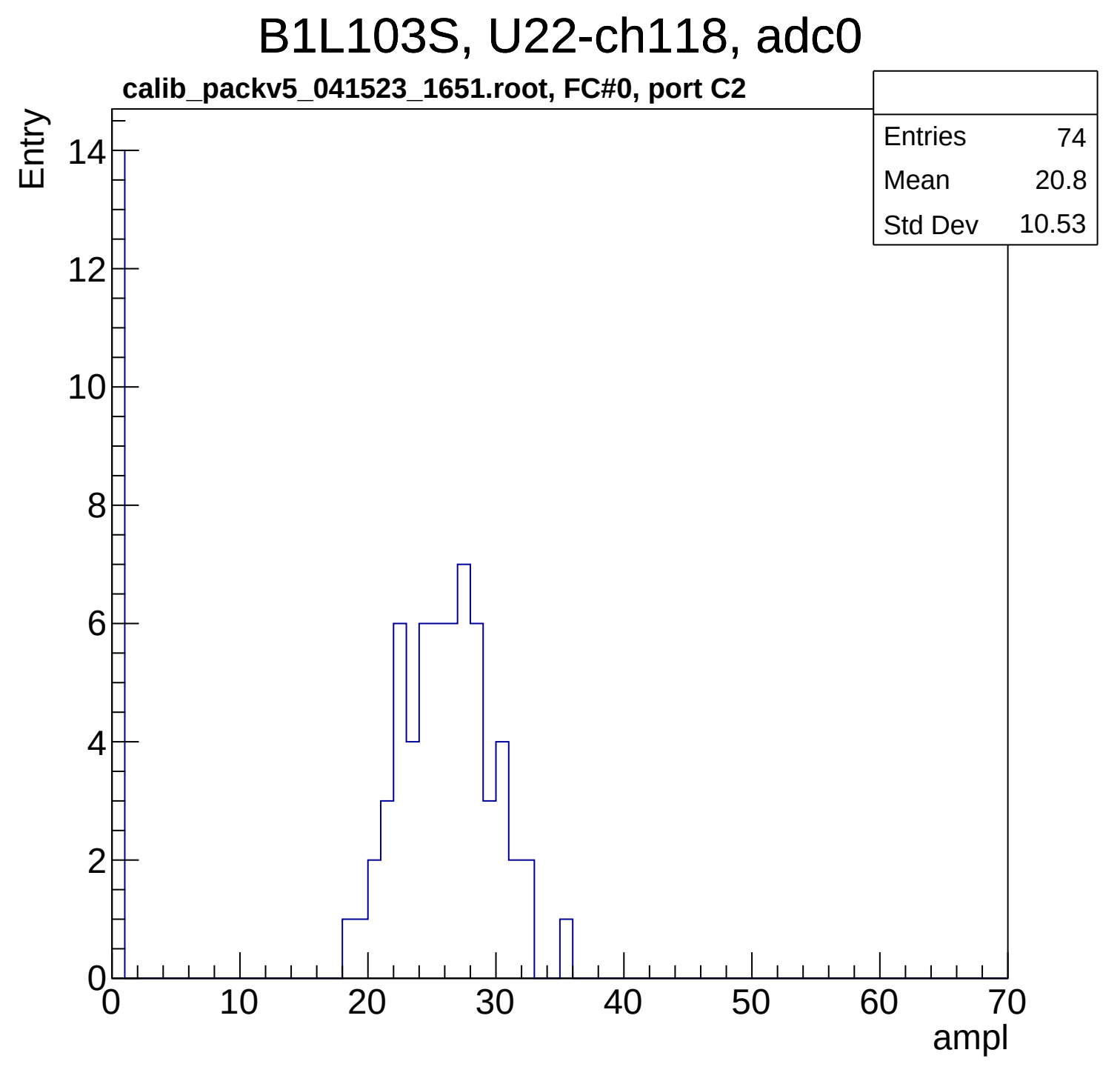
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch117, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 61.94
Std Dev 1.144
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U22-ch117, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch118, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 20.8
Std Dev 10.53
Entry
ampl
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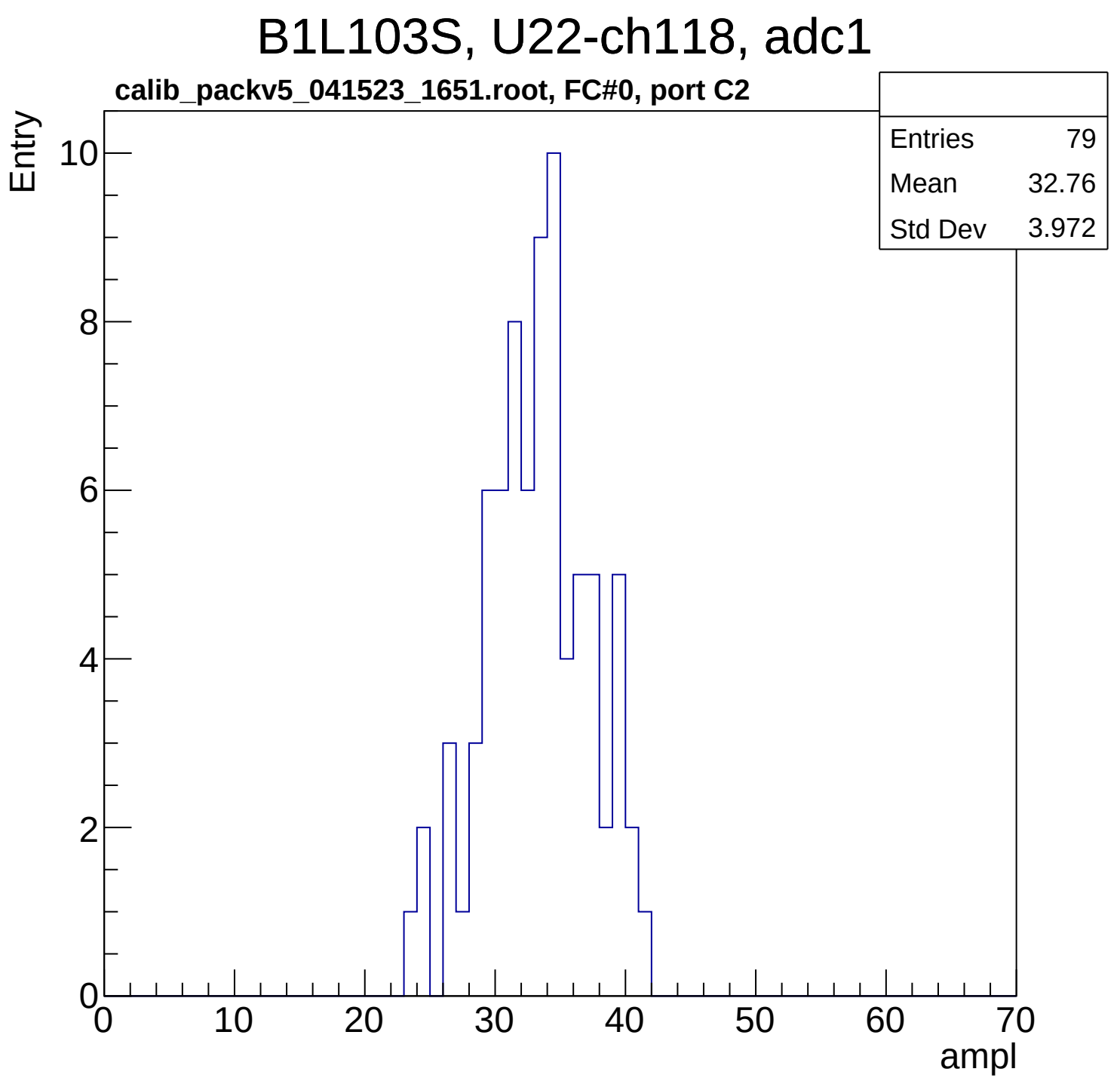
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U22-ch118, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 32.76
Std Dev 3.972
Entry
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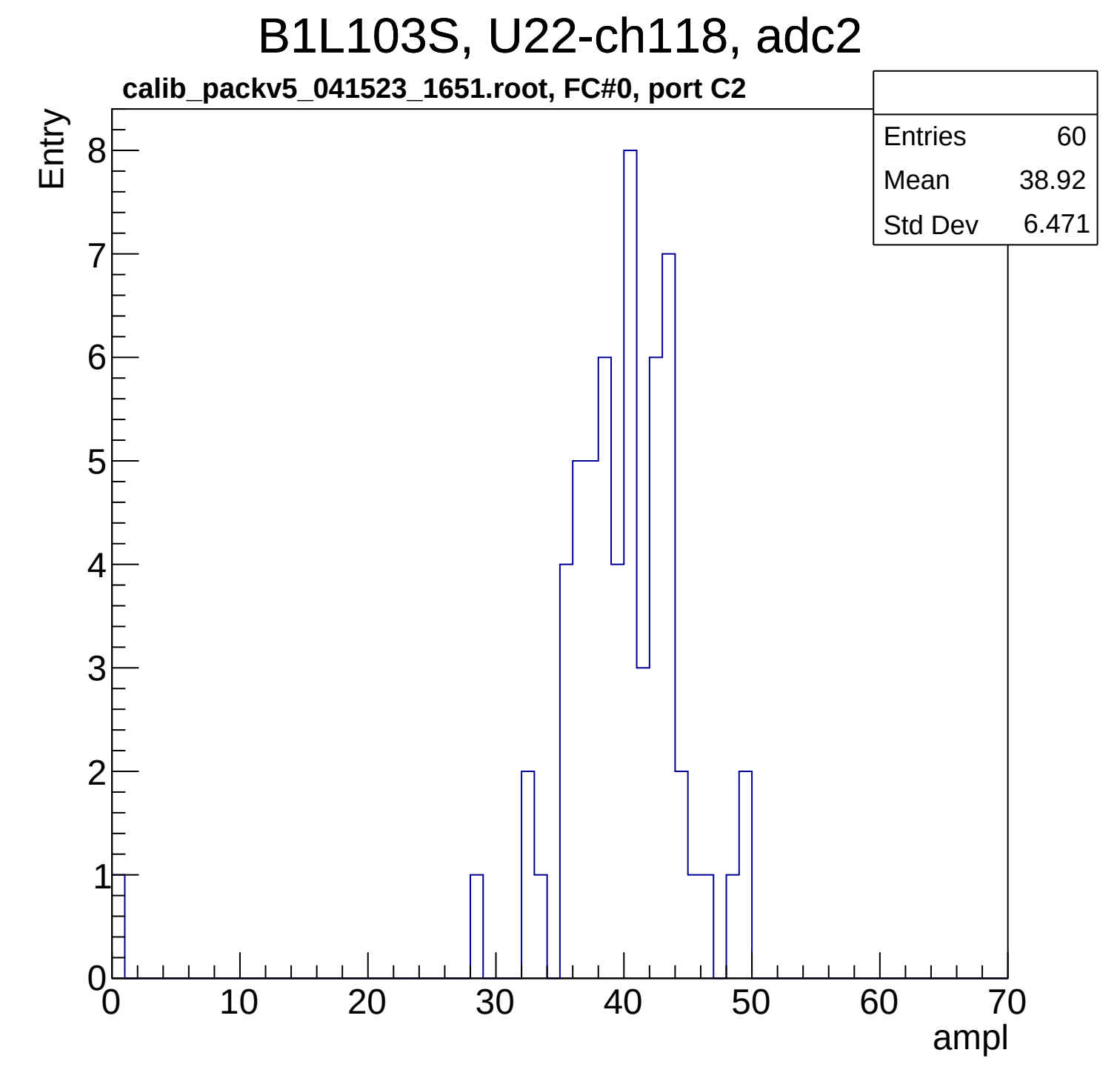
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch118, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 38.92
Std Dev 6.471
Entry
ampl
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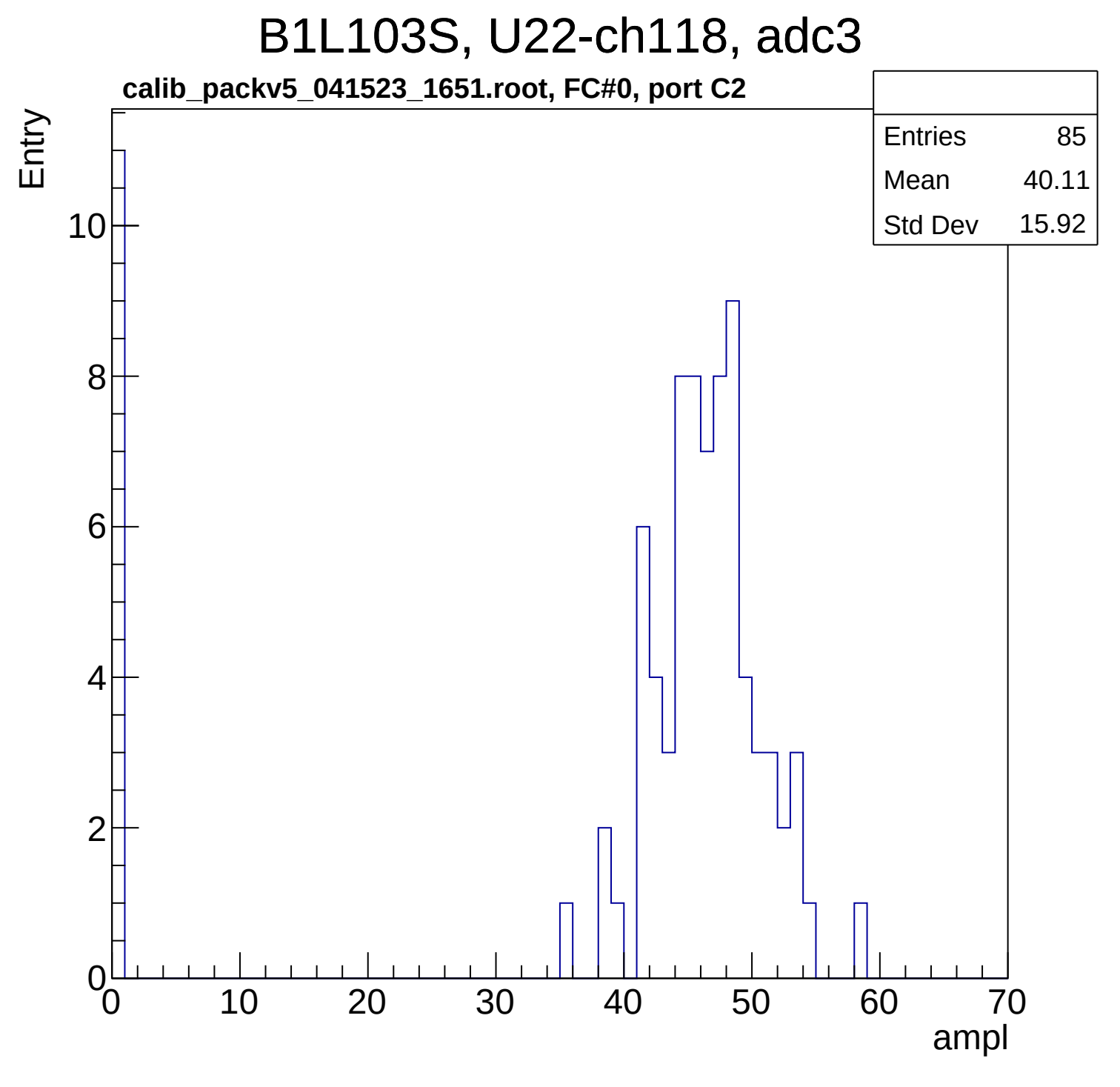
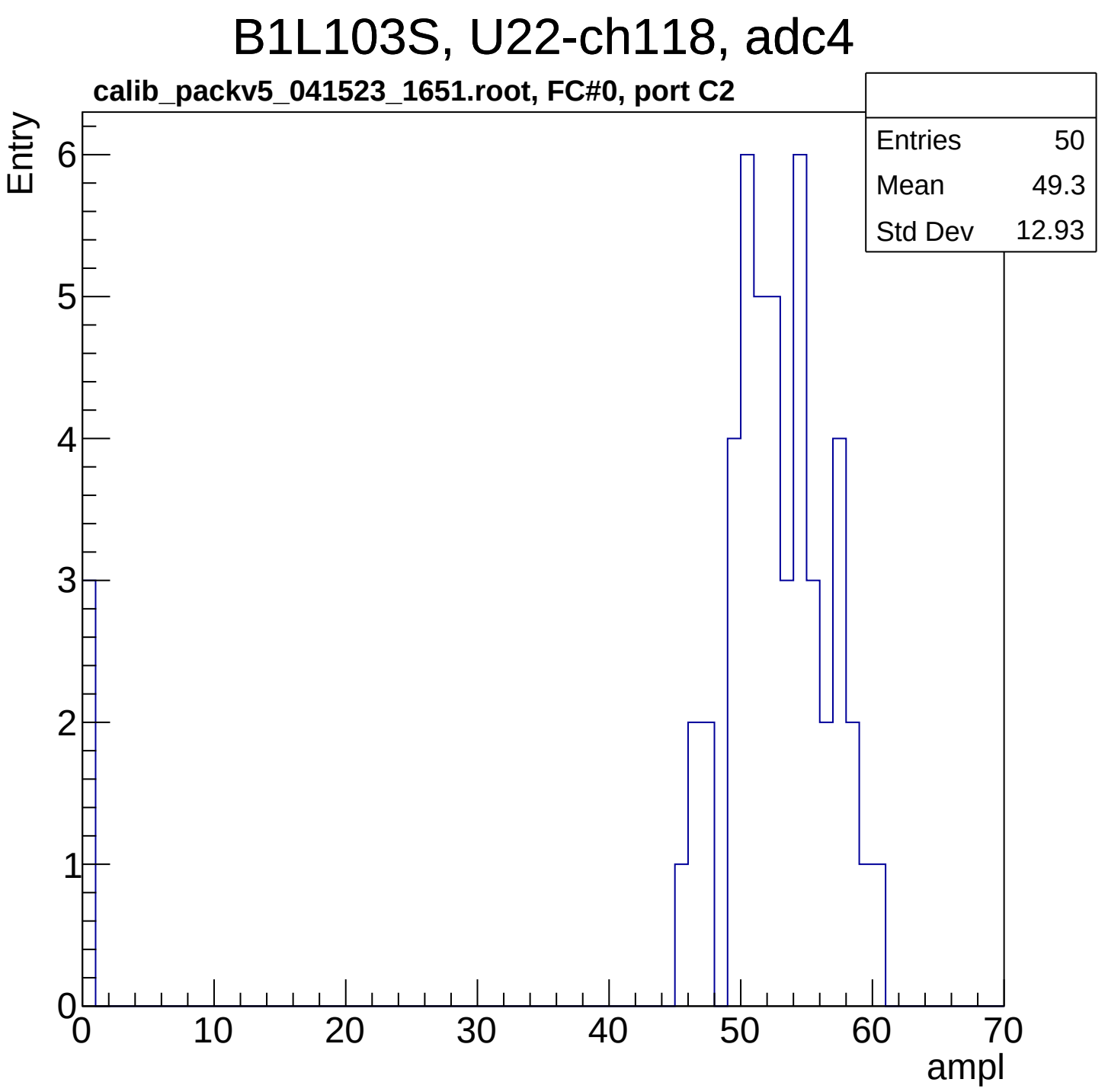
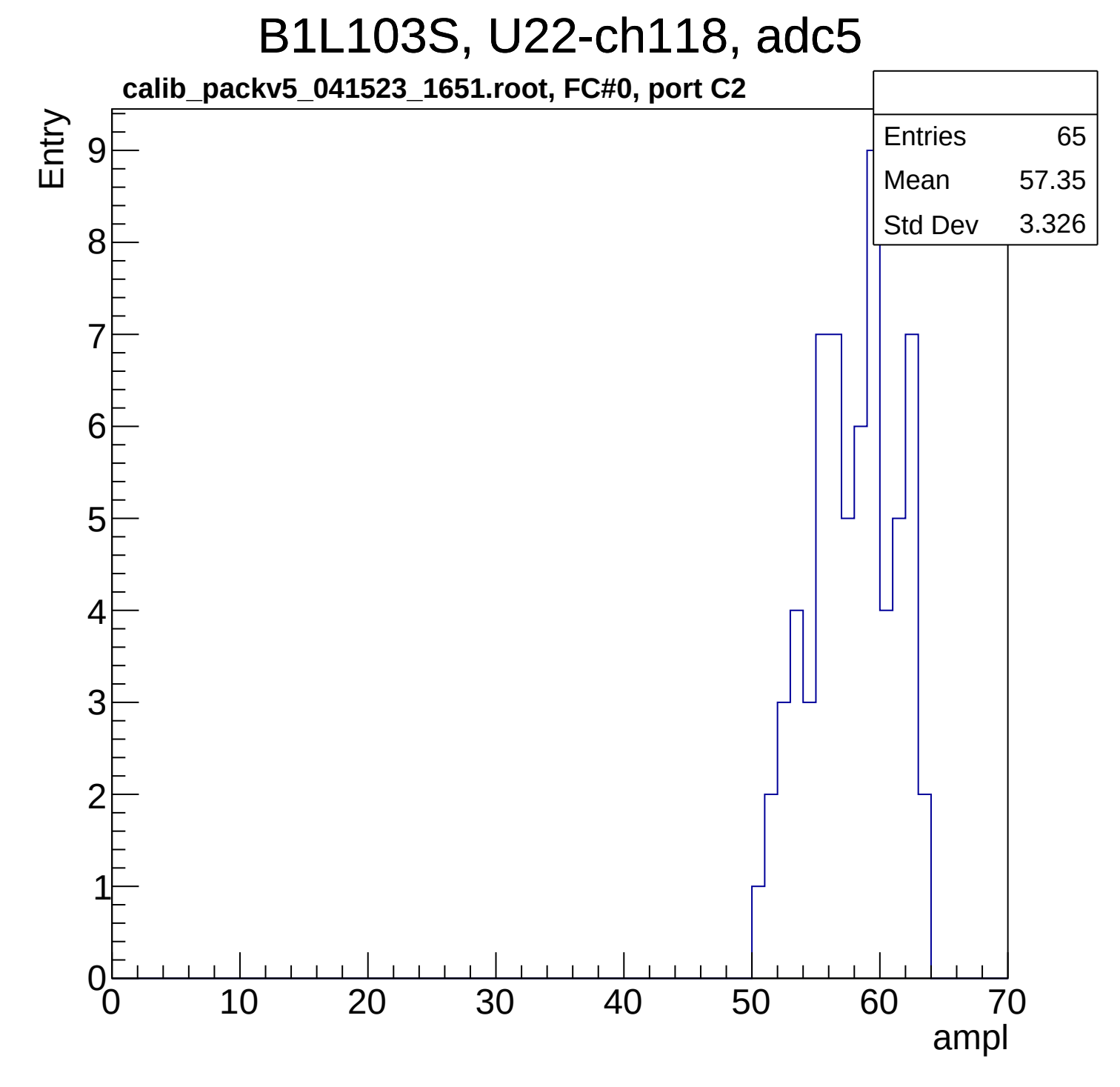
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch118, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 40.11
Std Dev 15.92
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch118, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 49.3
Std Dev 12.93
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch118, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 57.35
Std Dev 3.326
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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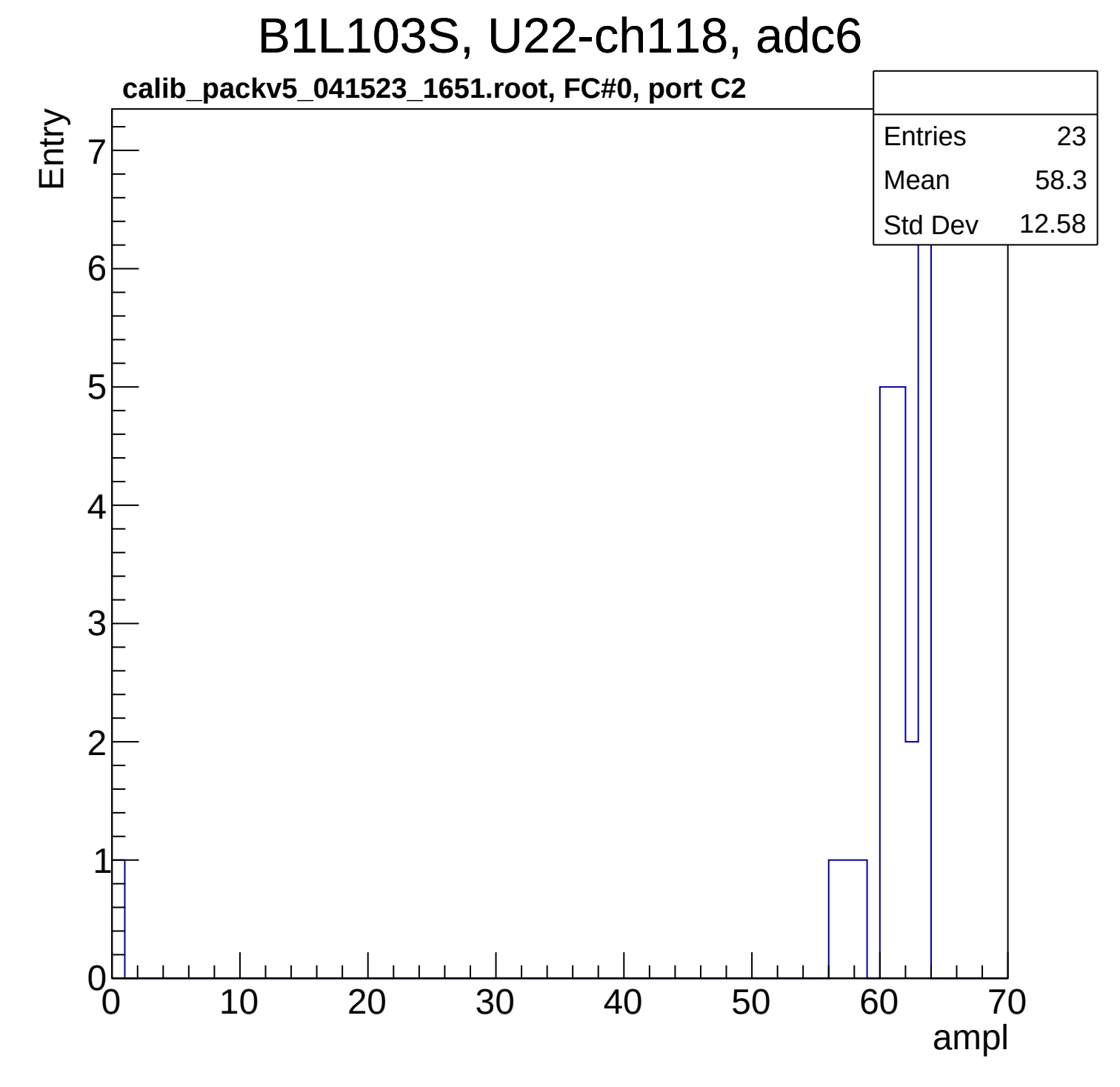
40
50
60
70


B1L103S, U22-ch118, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 58.3
Std Dev 12.58
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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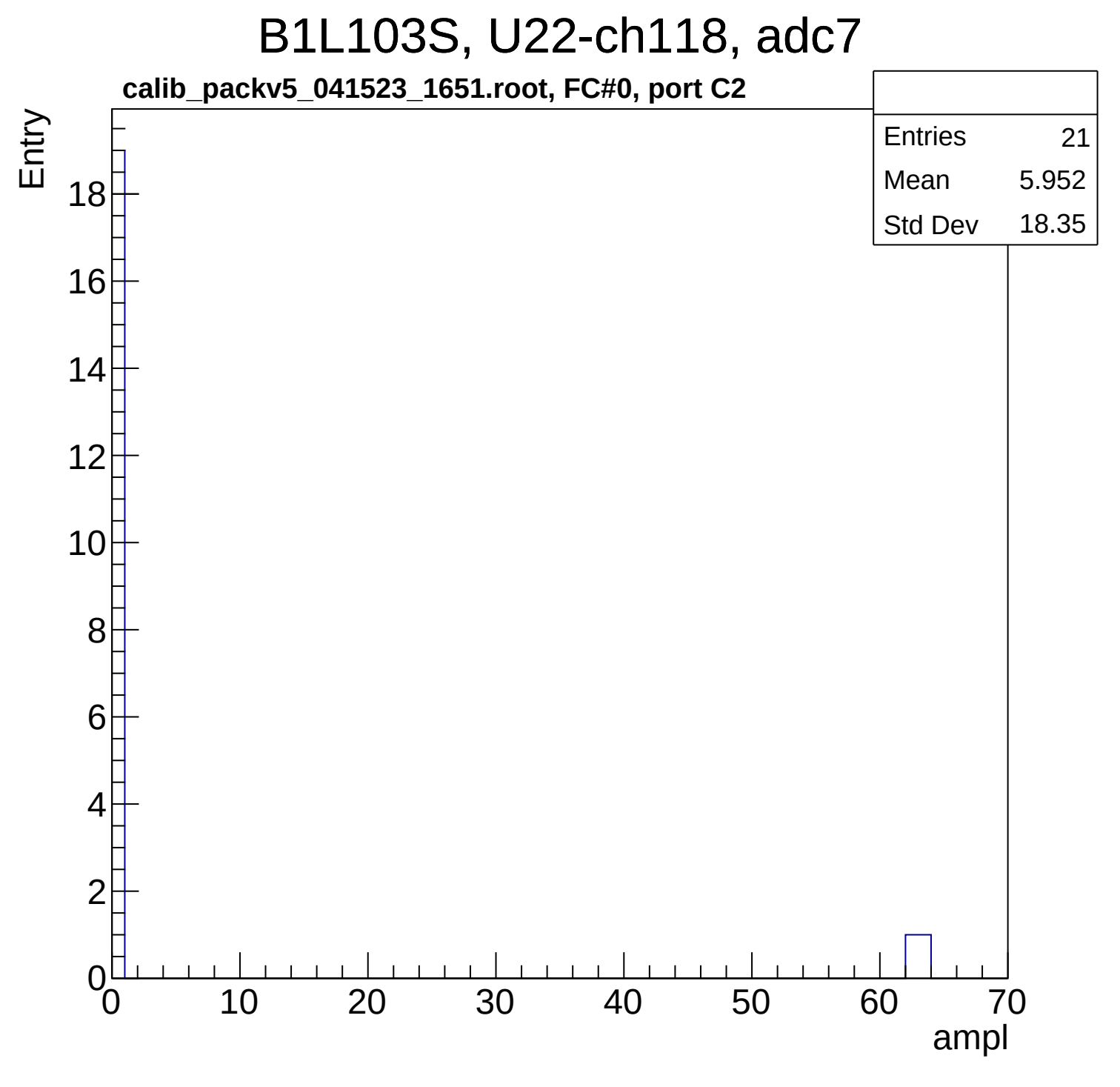
B1L103S, U22-ch118, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.952
Std Dev 18.35
Entry
0
2
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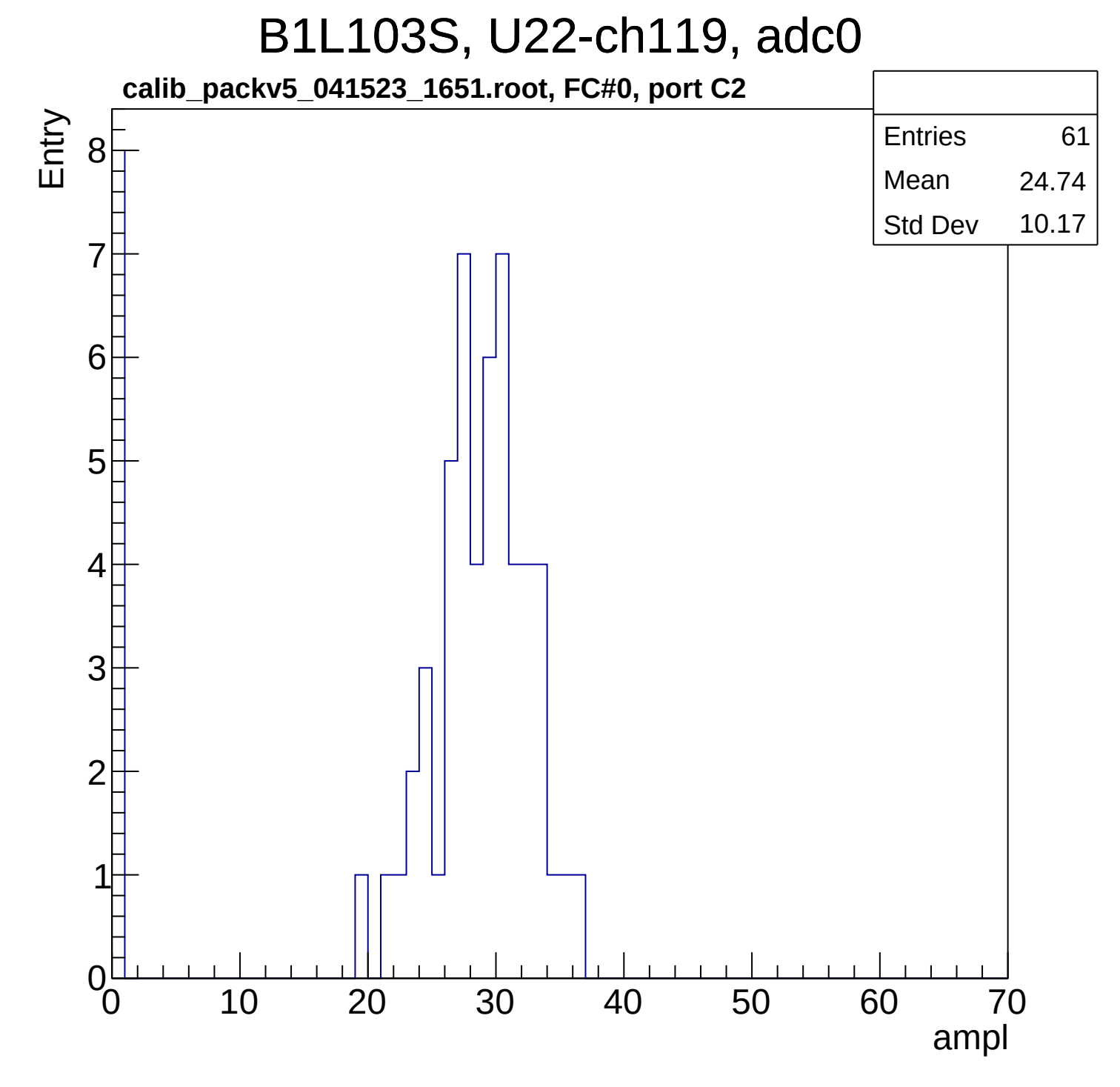
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch119, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 24.74
Std Dev 10.17
Entry
ampl
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1
2
3
4
5
6
7
8
0
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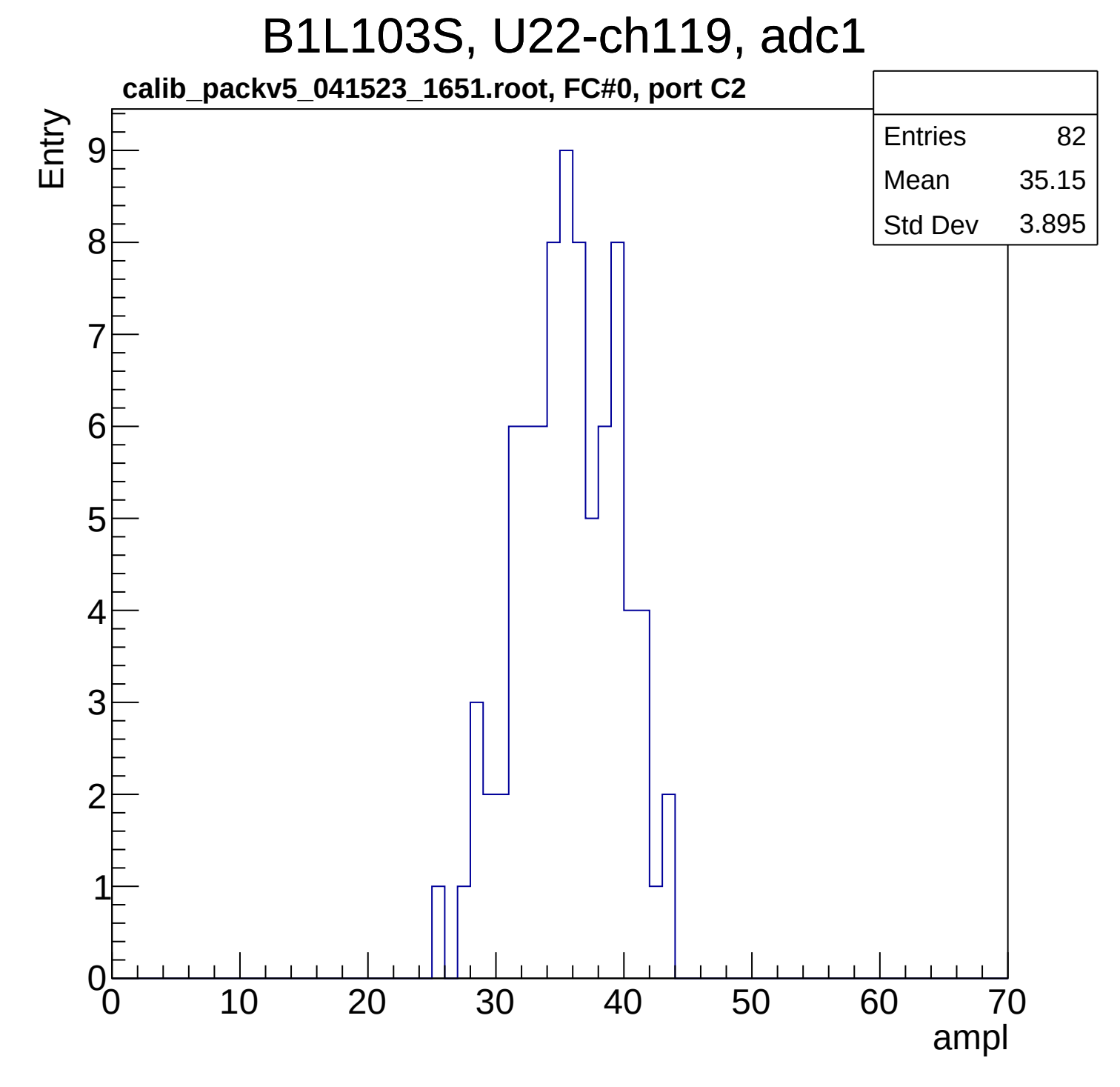
20
30
40
50
60
70


B1L103S, U22-ch119, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 35.15
Std Dev 3.895
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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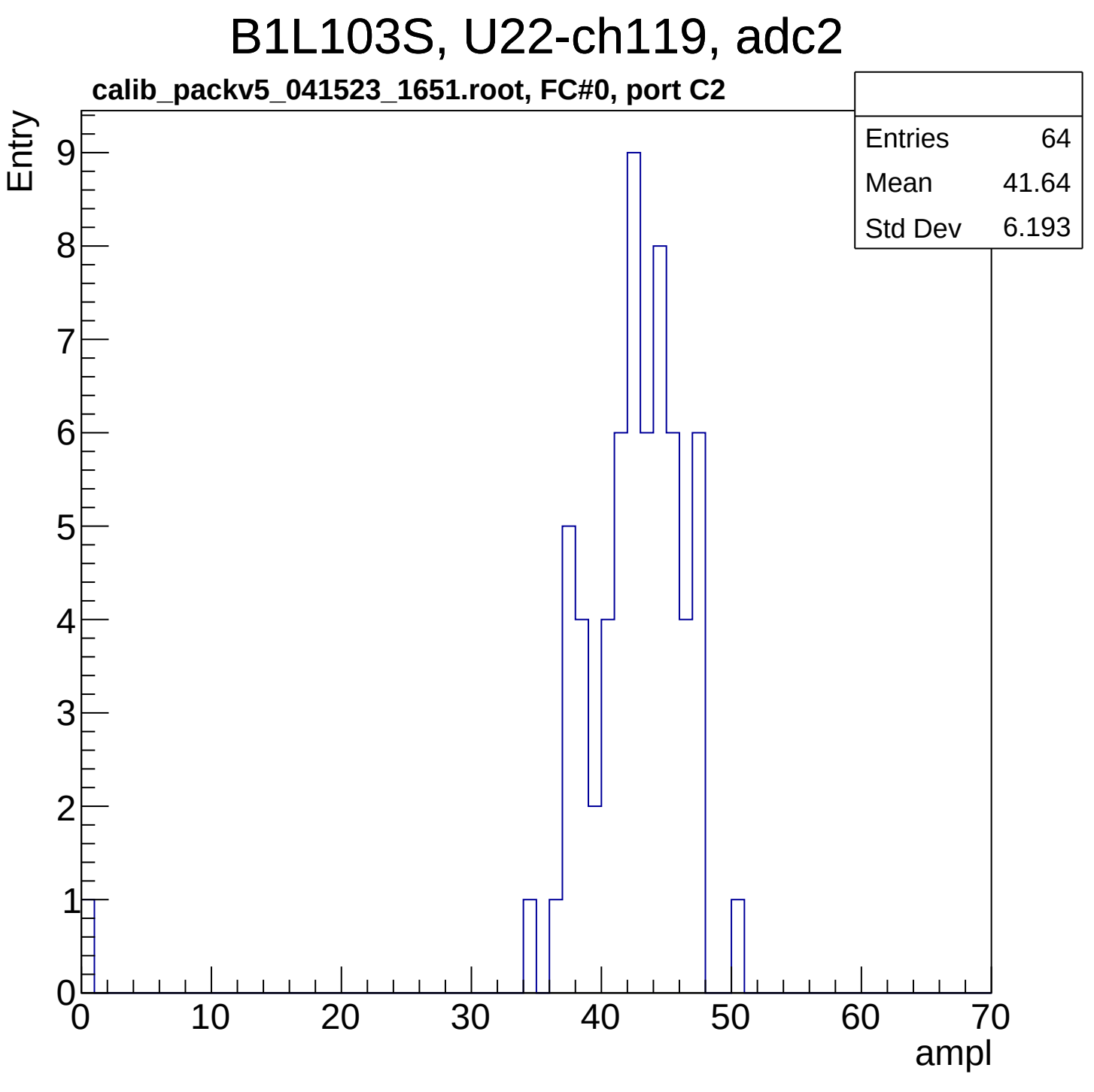
B1L103S, U22-ch119, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 41.64
Std Dev 6.193
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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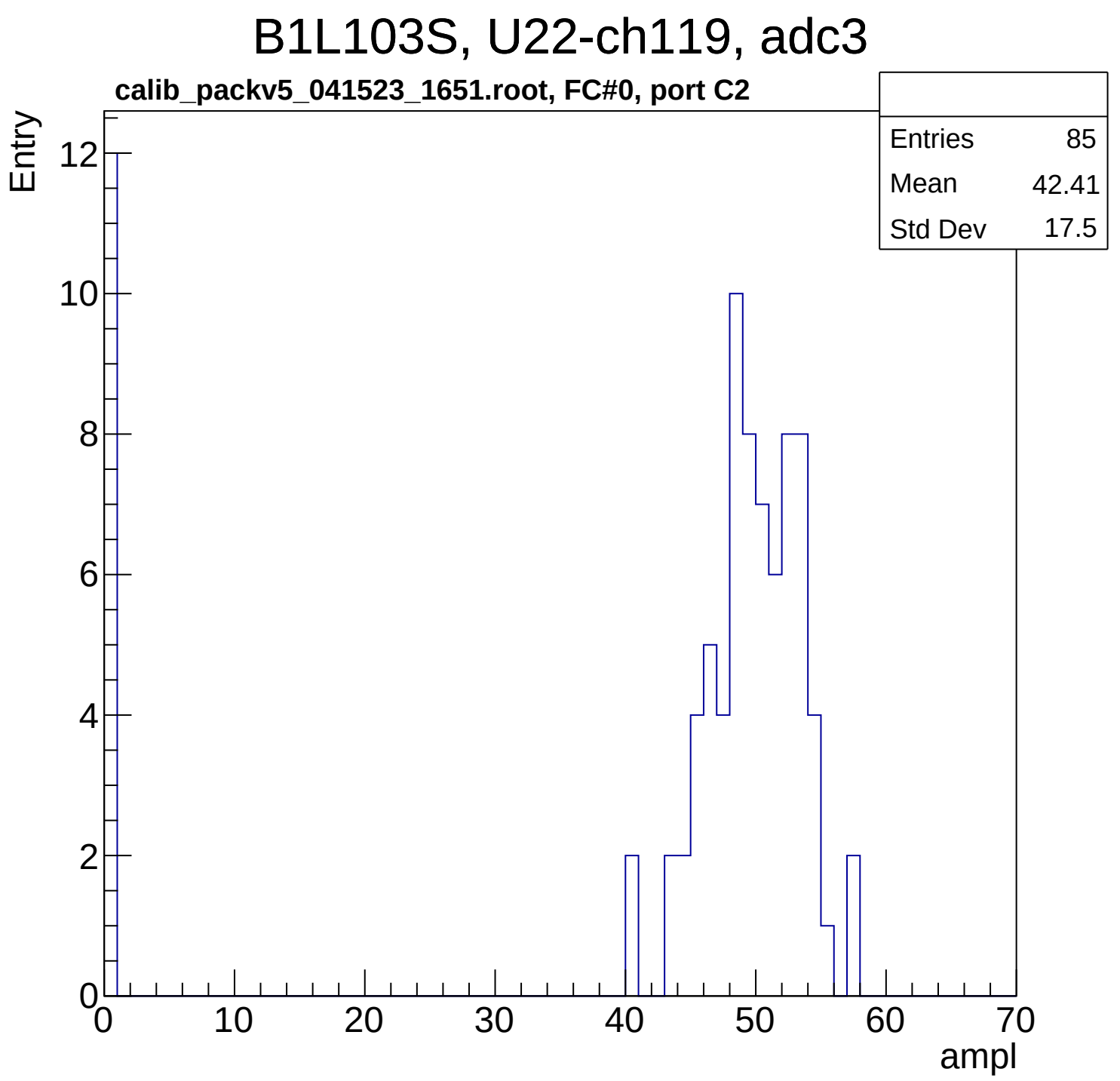
B1L103S, U22-ch119, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 42.41
Std Dev 17.5
Entry
ampl
0
2
4
6
8
10
12
0
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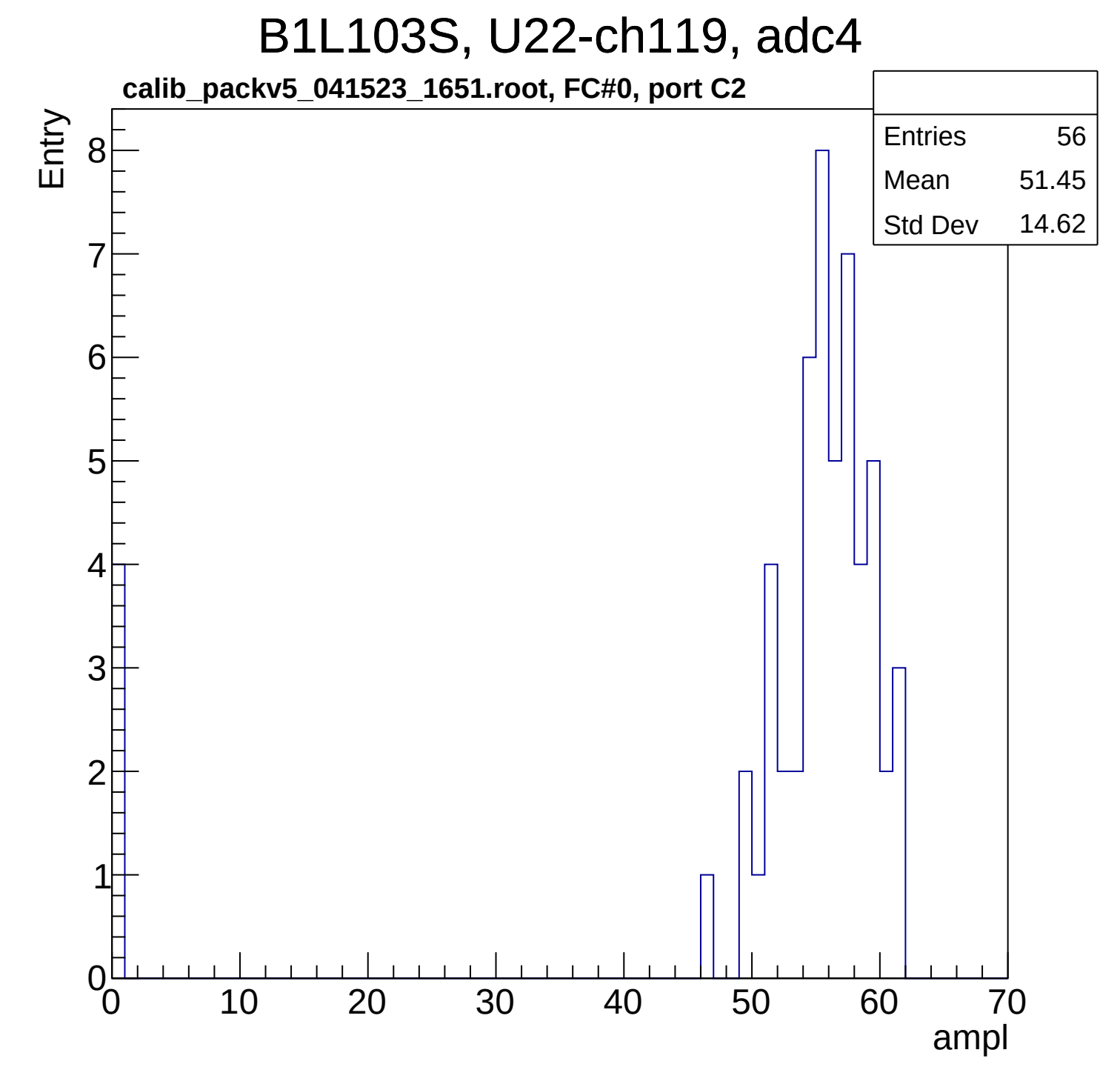
B1L103S, U22-ch119, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 51.45
Std Dev 14.62
Entry
ampl
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2
3
4
5
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7
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0
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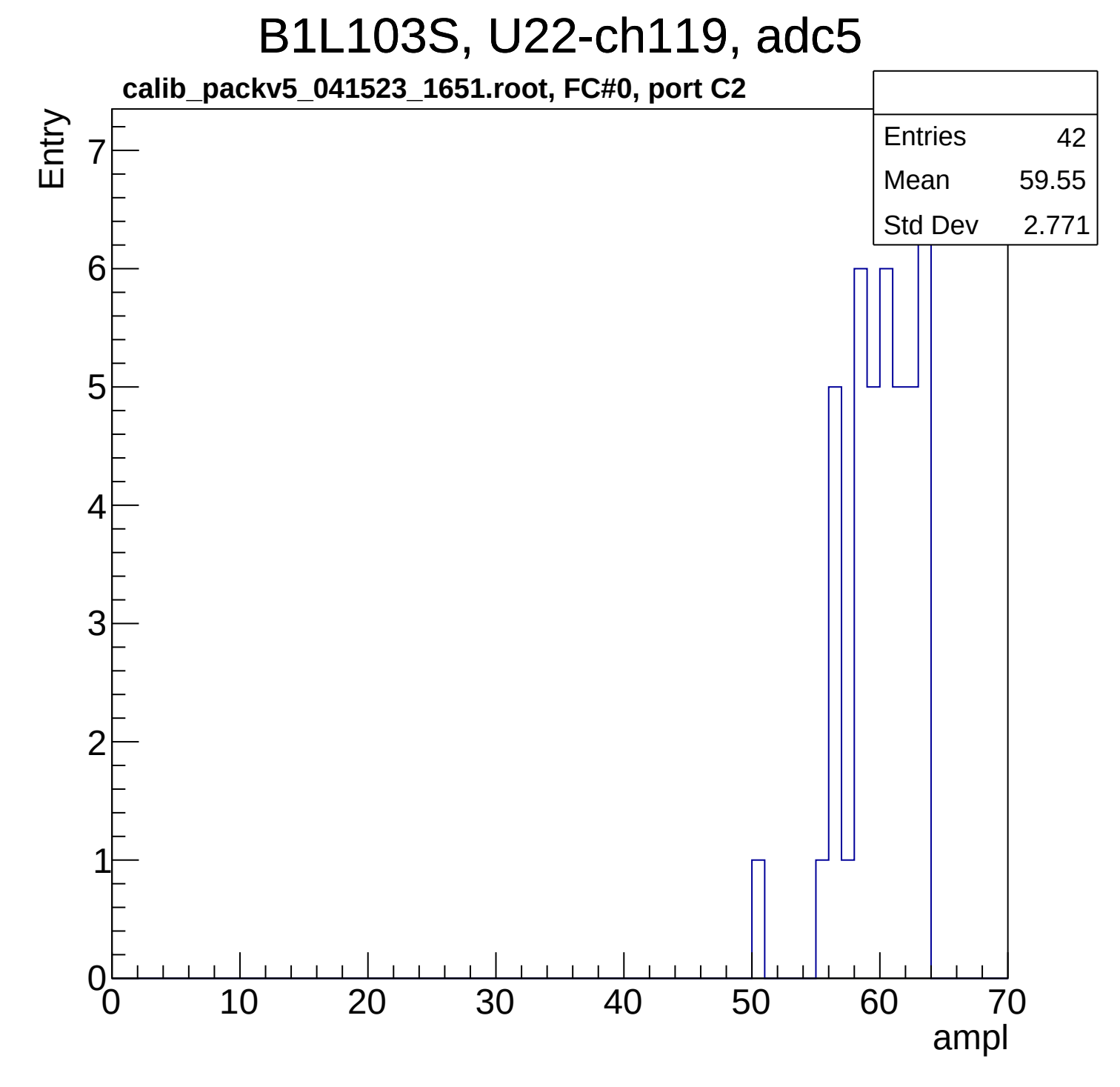
B1L103S, U22-ch119, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 59.55
Std Dev 2.771
Entry
ampl
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1
2
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0
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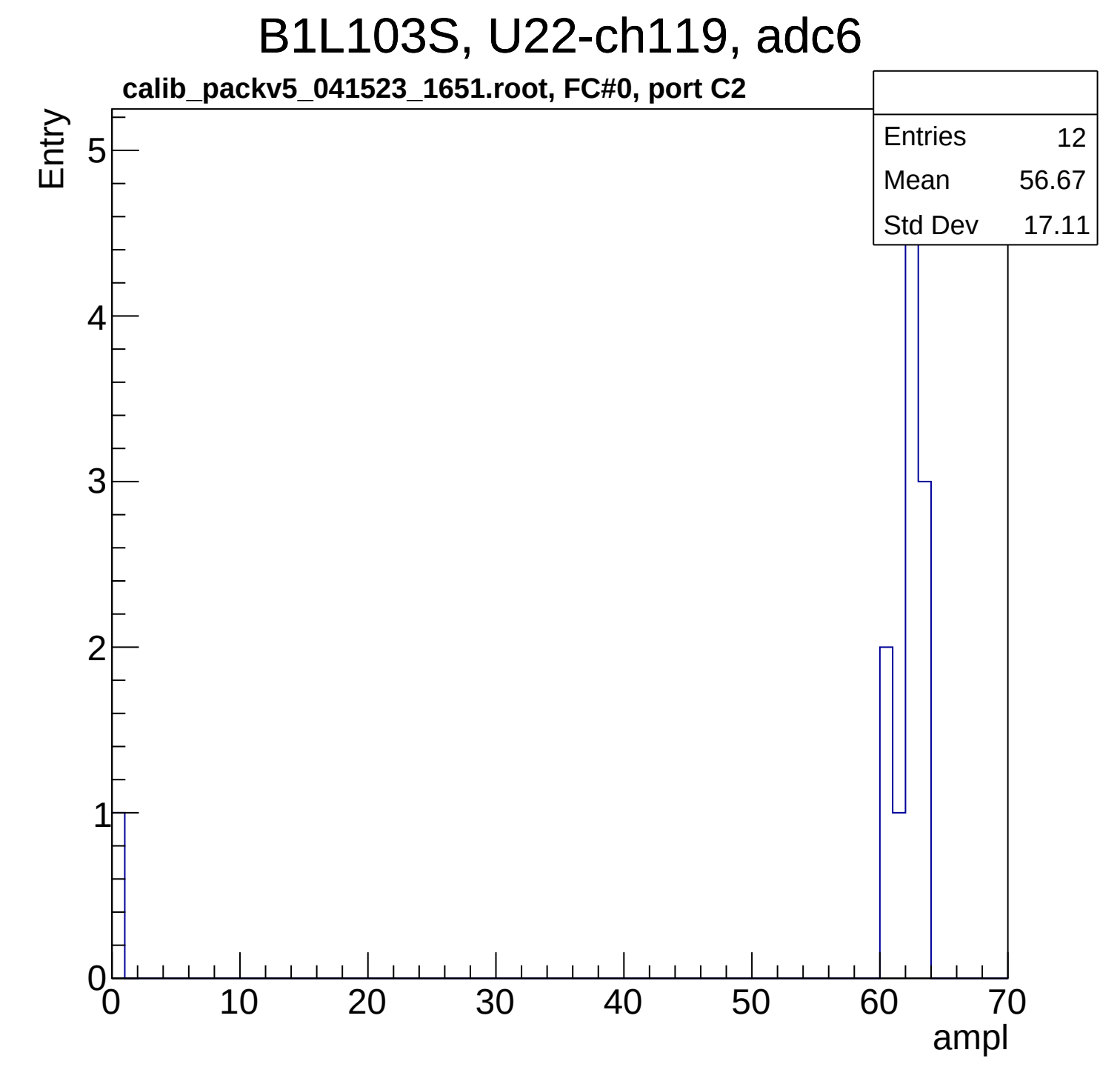
B1L103S, U22-ch119, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 56.67
Std Dev 17.11
Entry
ampl
0
1
2
3
4
5
0
10
20
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40
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60
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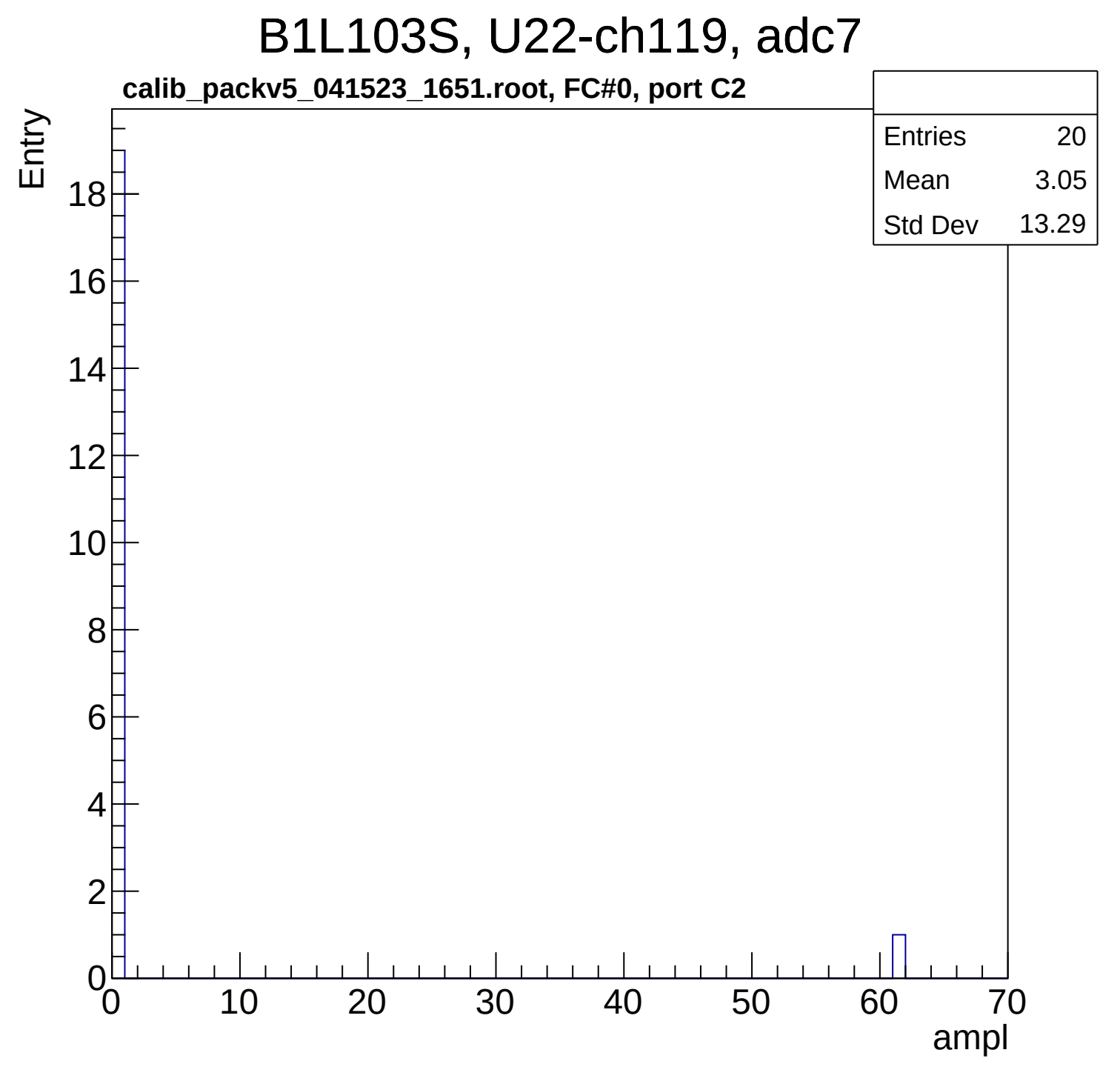
B1L103S, U22-ch119, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.05
Std Dev 13.29
Entry
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6
8
10
12
14
16
18
0
10
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30
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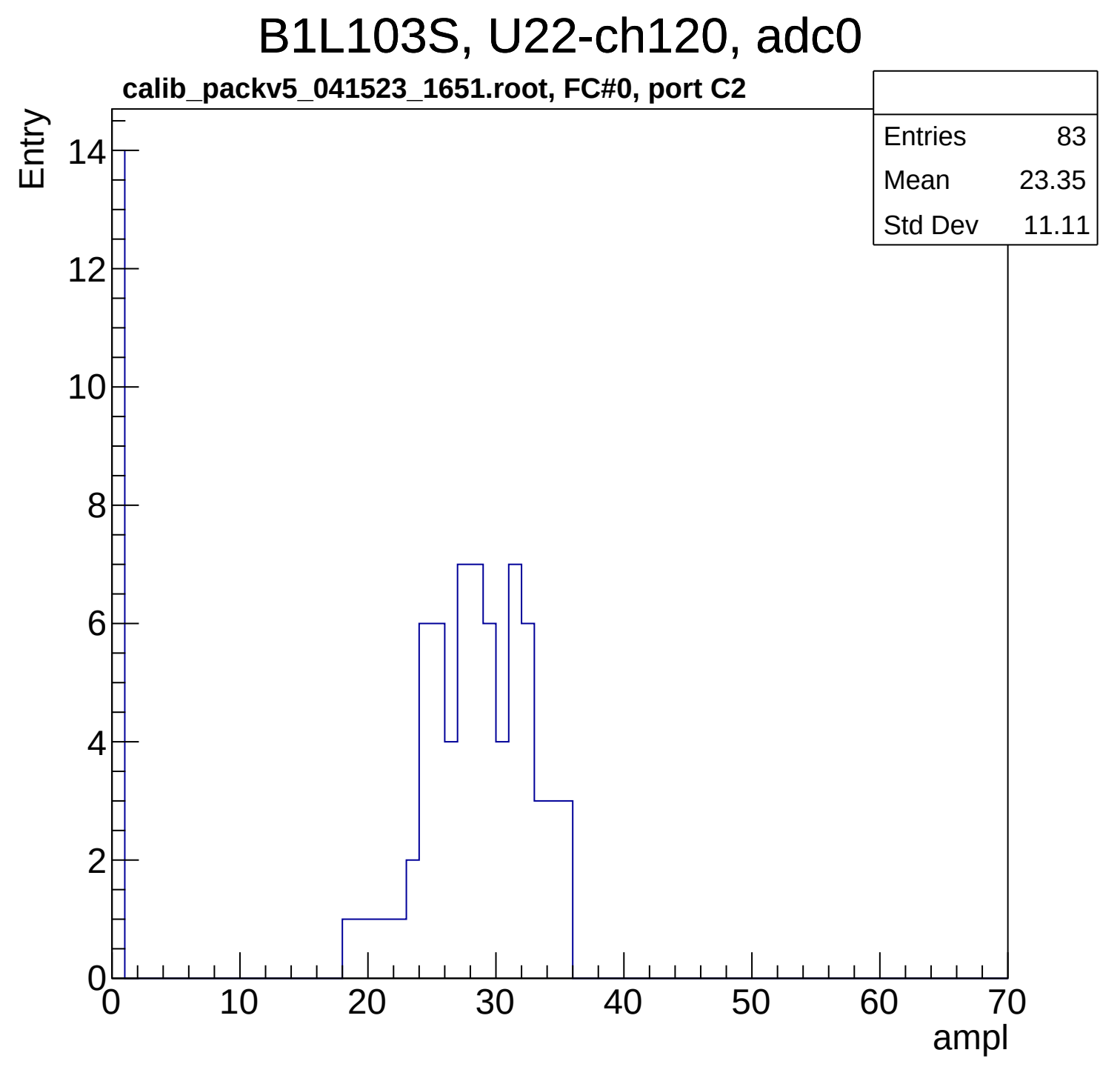
50
60
70
ampl


B1L103S, U22-ch120, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 23.35
Std Dev 11.11
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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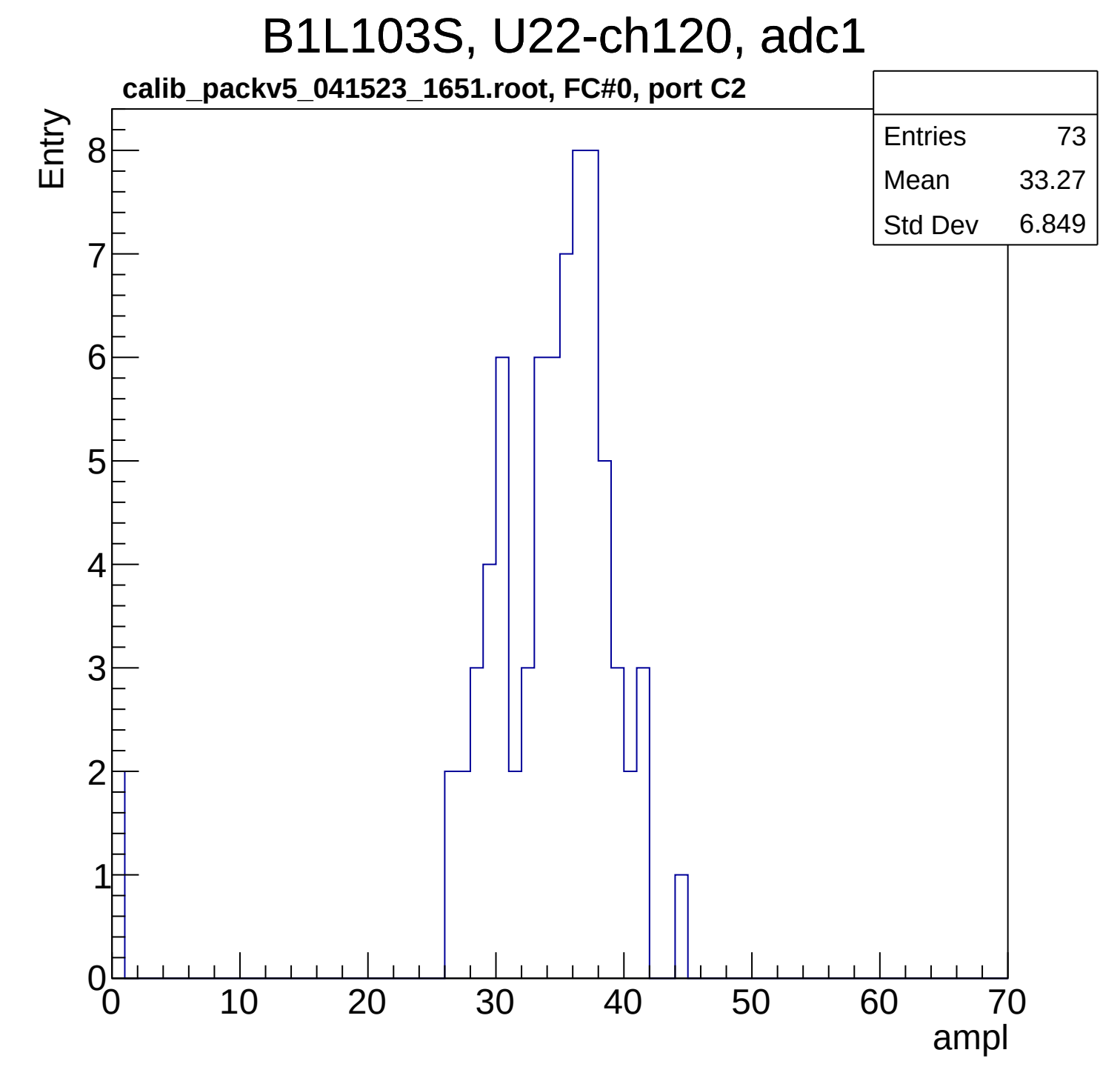
B1L103S, U22-ch120, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 33.27
Std Dev 6.849
Entry
ampl
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2
3
4
5
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7
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0
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60
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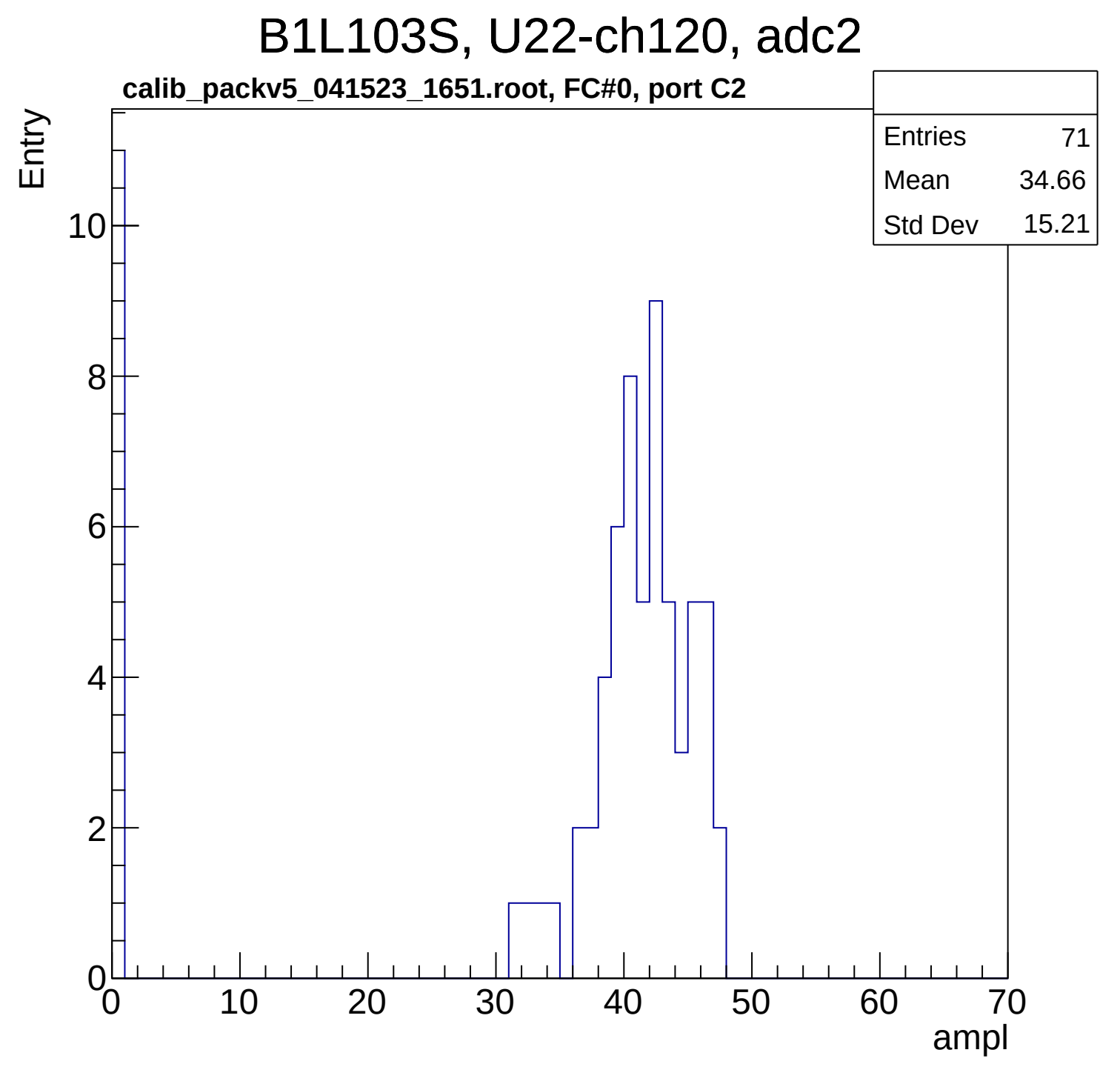
B1L103S, U22-ch120, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 34.66
Std Dev 15.21
Entry
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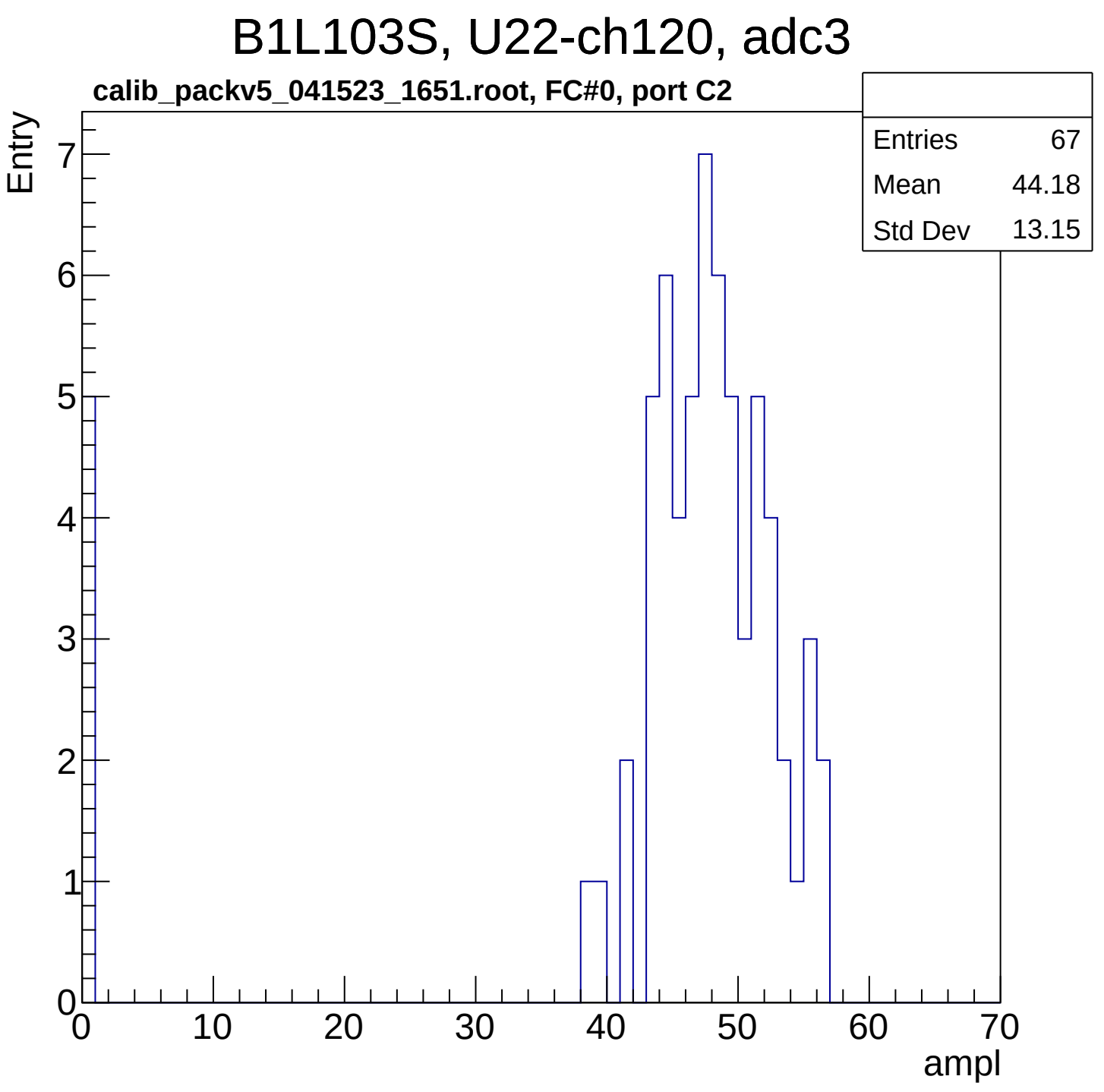
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch120, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 44.18
Std Dev 13.15
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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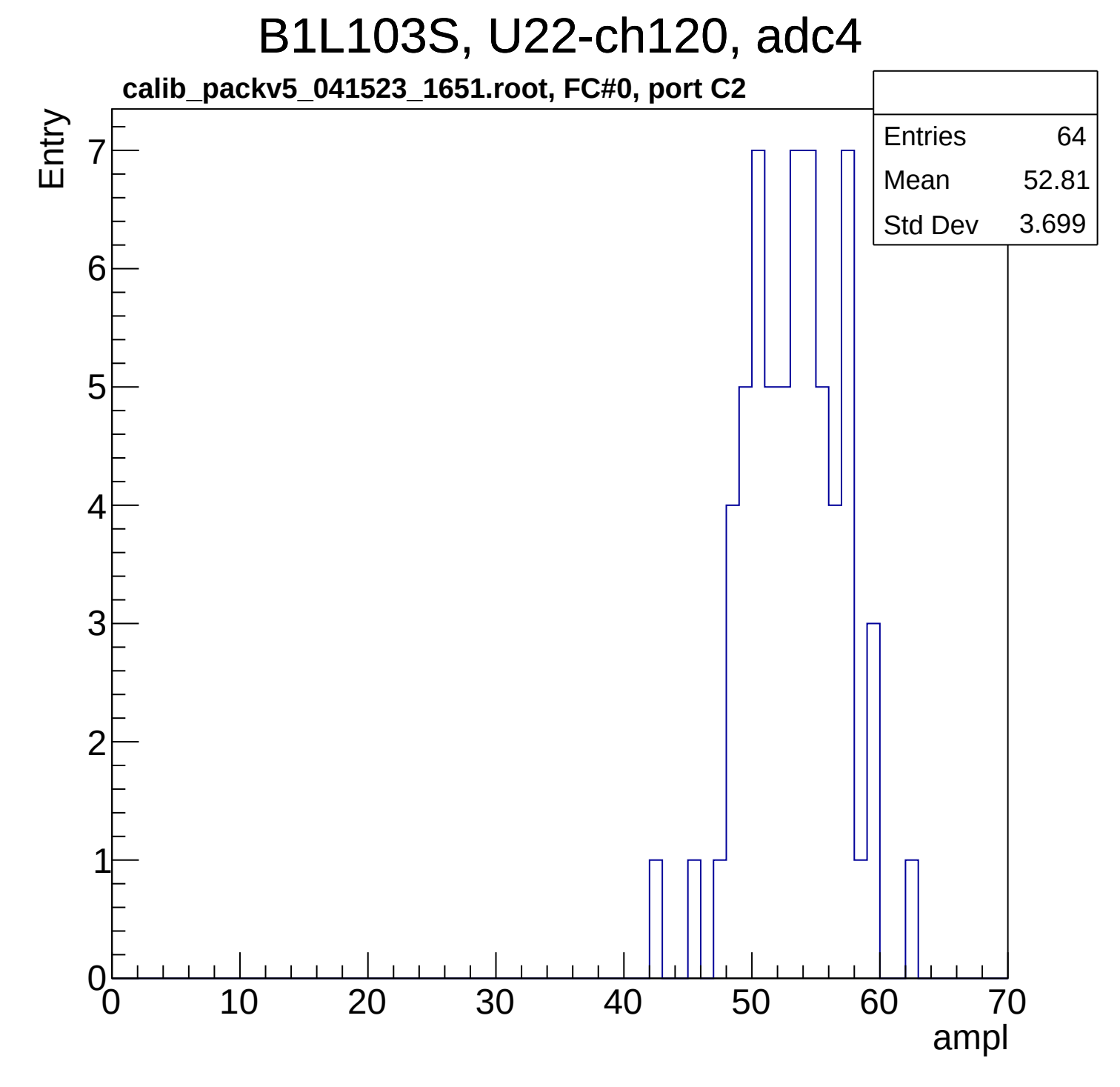
B1L103S, U22-ch120, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 52.81
Std Dev 3.699
Entry
ampl
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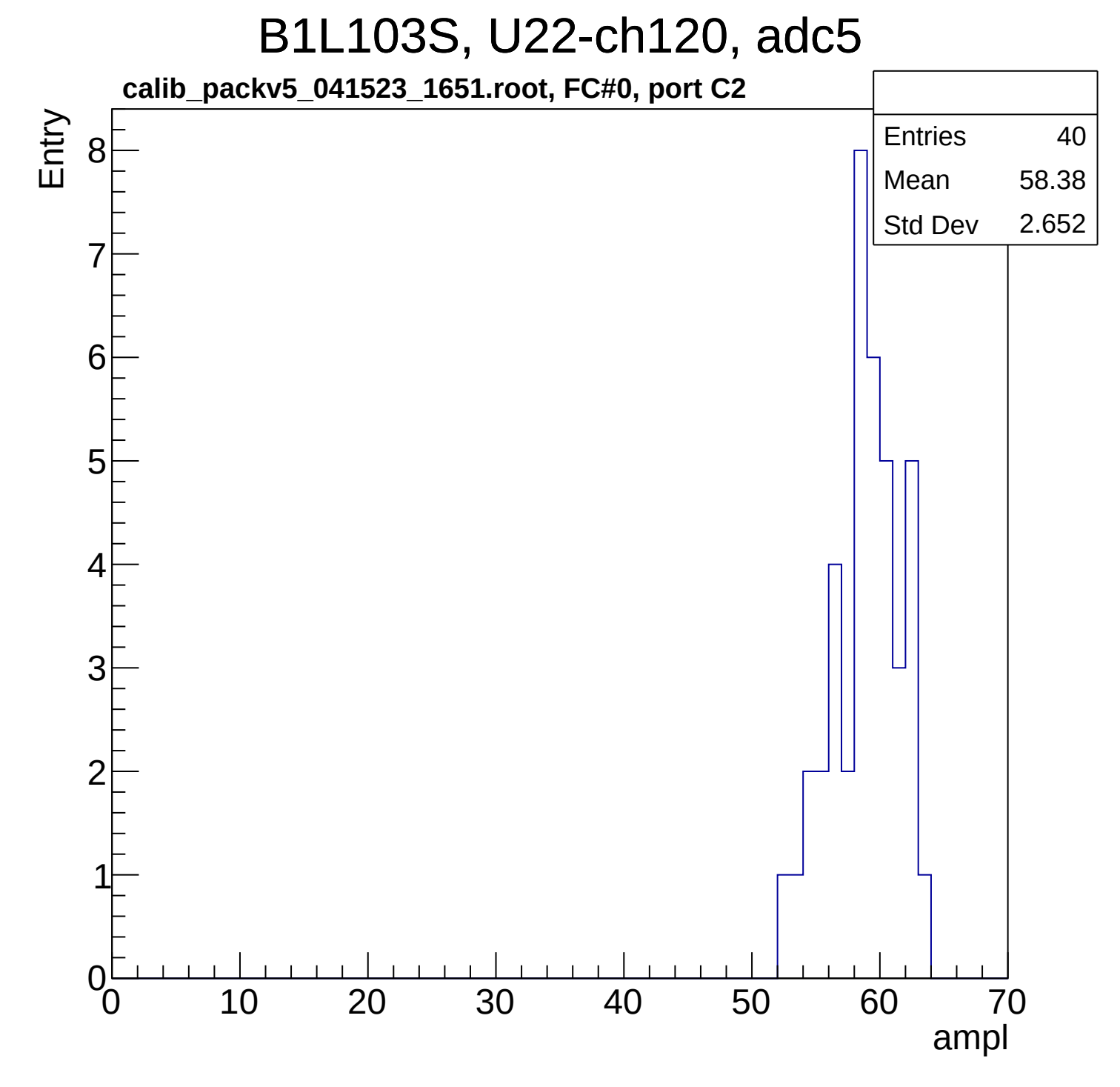
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U22-ch120, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 58.38
Std Dev 2.652
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
50
60
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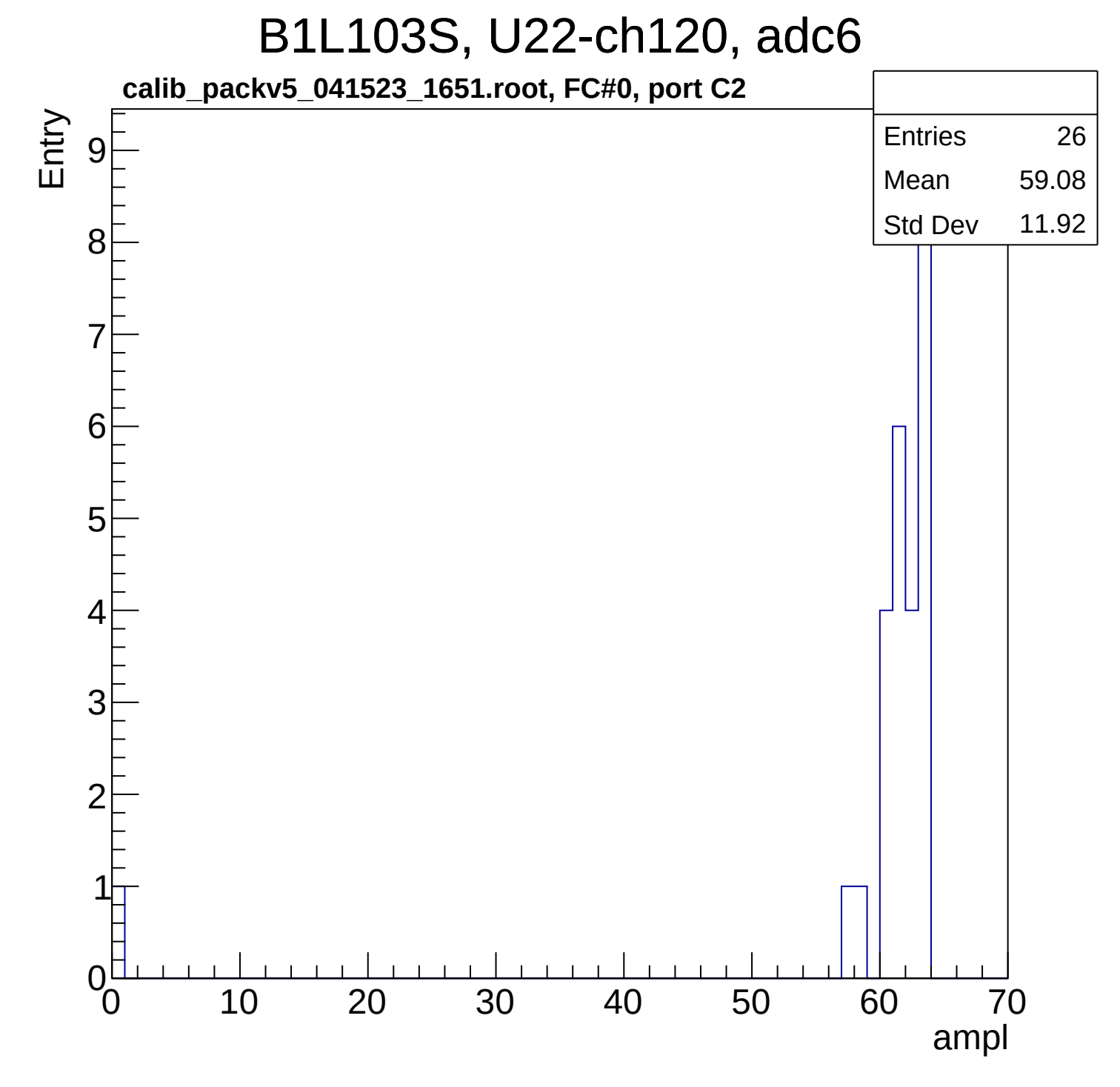
B1L103S, U22-ch120, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 59.08
Std Dev 11.92
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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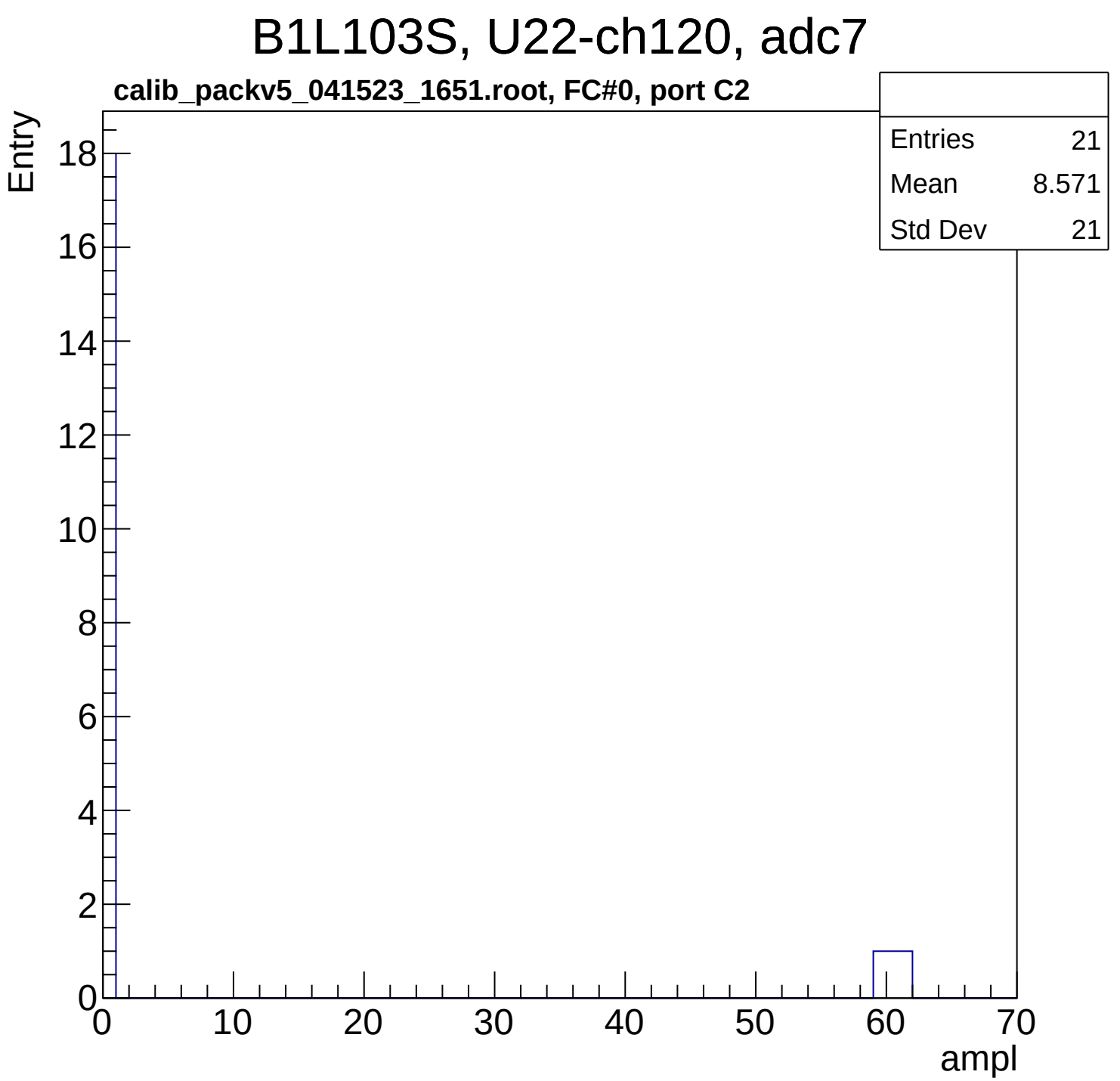
B1L103S, U22-ch120, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 8.571
Std Dev 21
Entry
ampl
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4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
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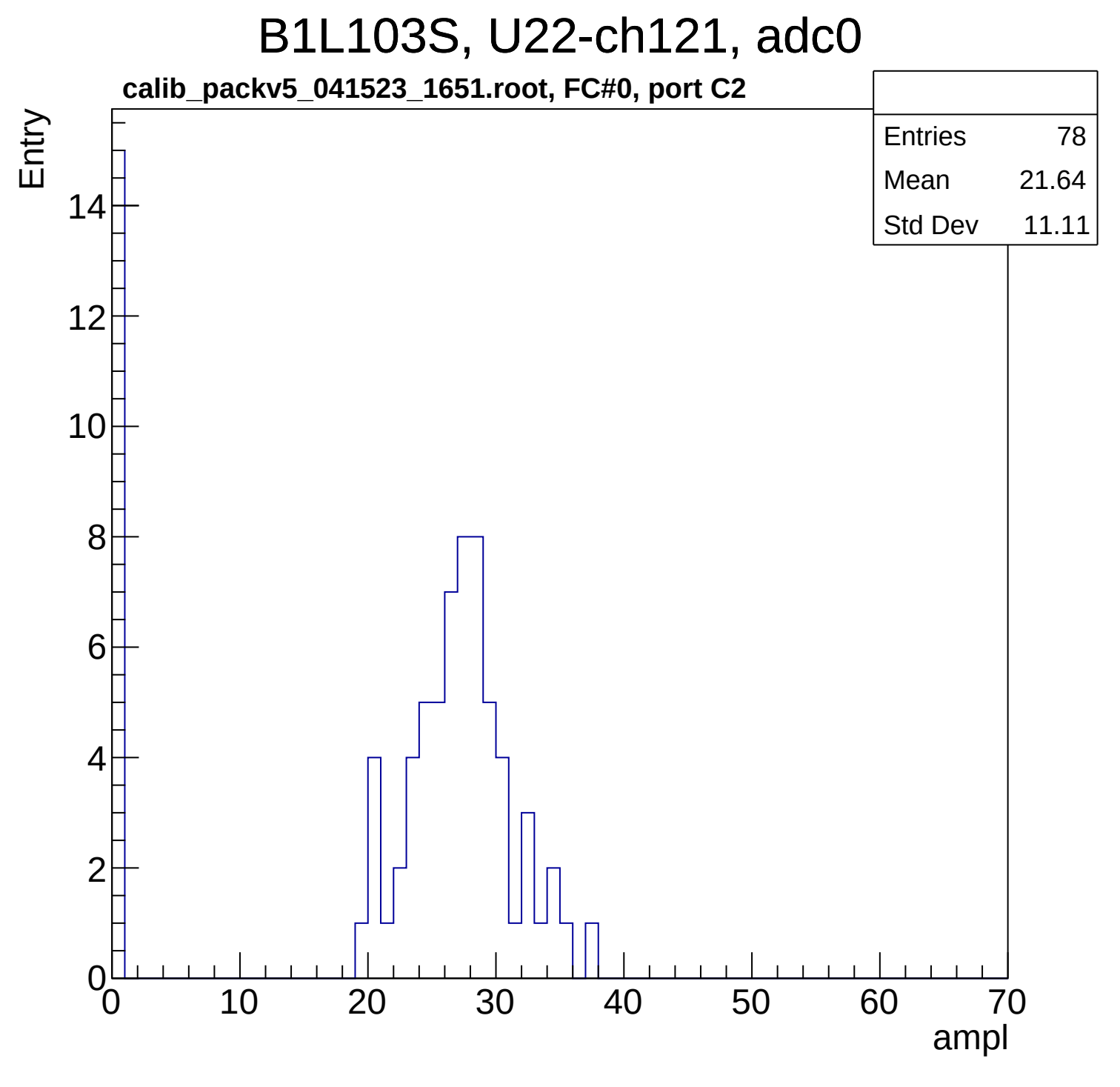
B1L103S, U22-ch121, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 21.64
Std Dev 11.11
Entry
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4
6
8
10
12
14
0
10
20
30
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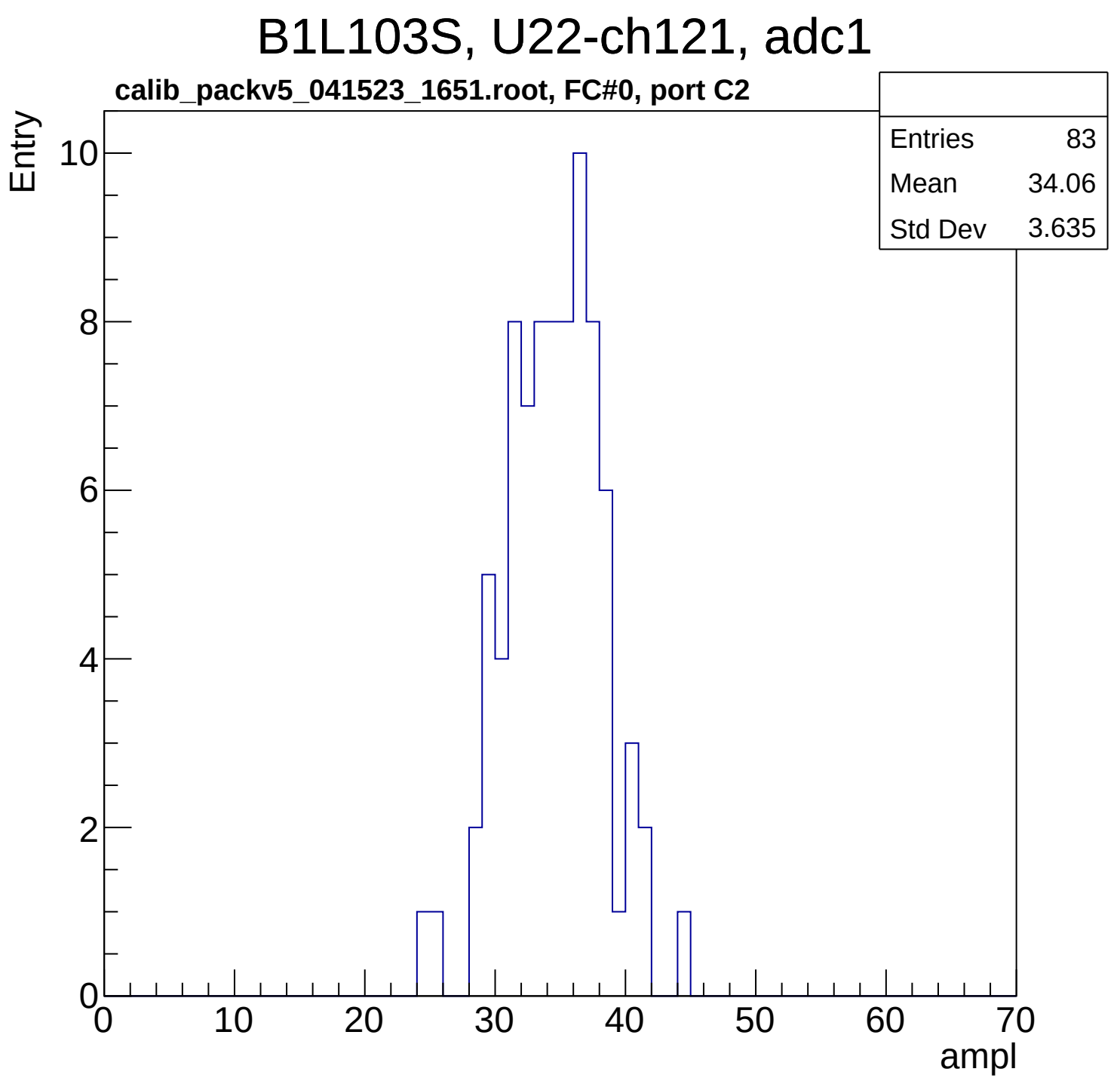
50
60
70
ampl


B1L103S, U22-ch121, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 34.06
Std Dev 3.635
Entry
ampl
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2
4
6
8
10
0
10
20
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40
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60
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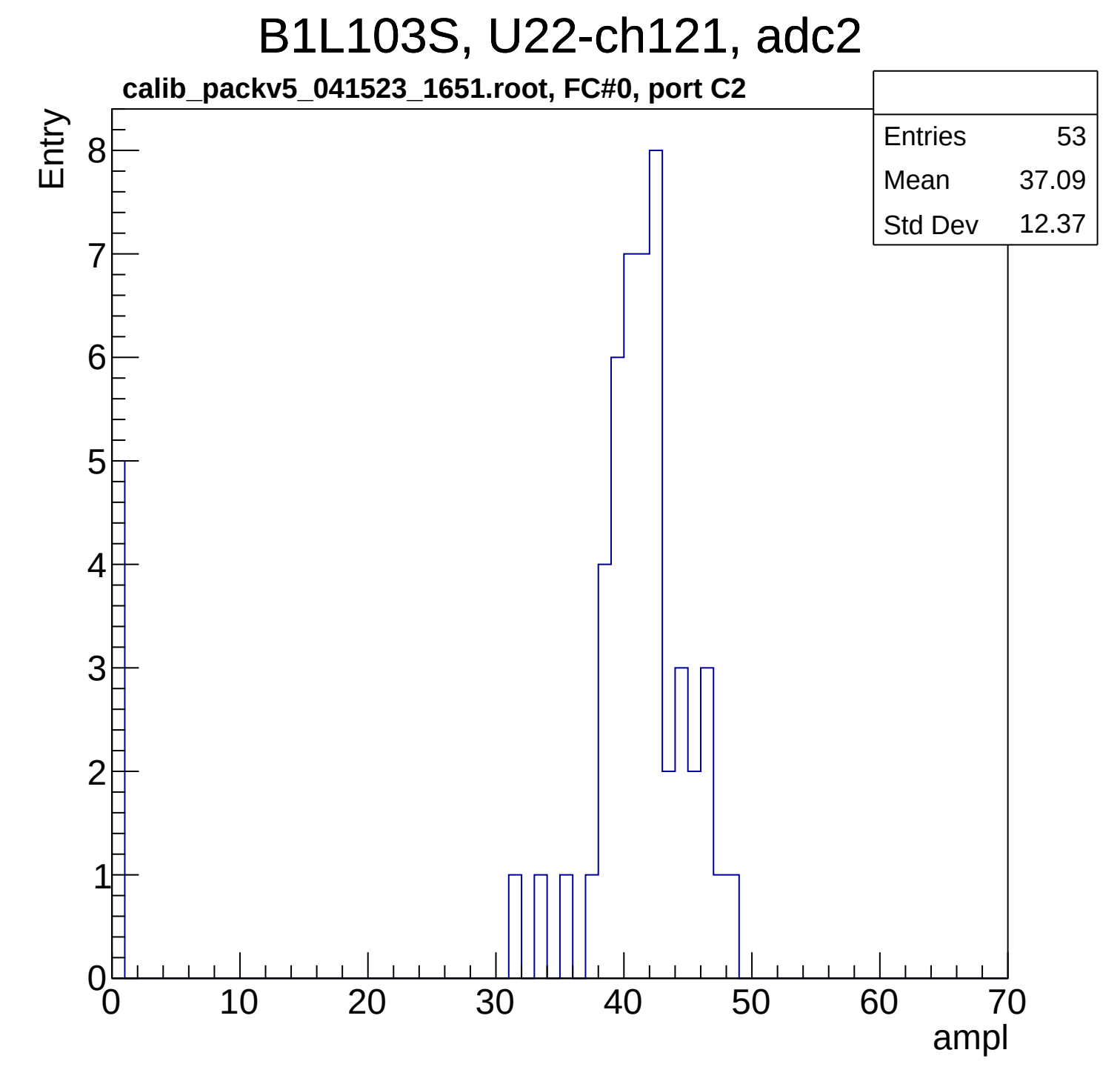
B1L103S, U22-ch121, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 37.09
Std Dev 12.37
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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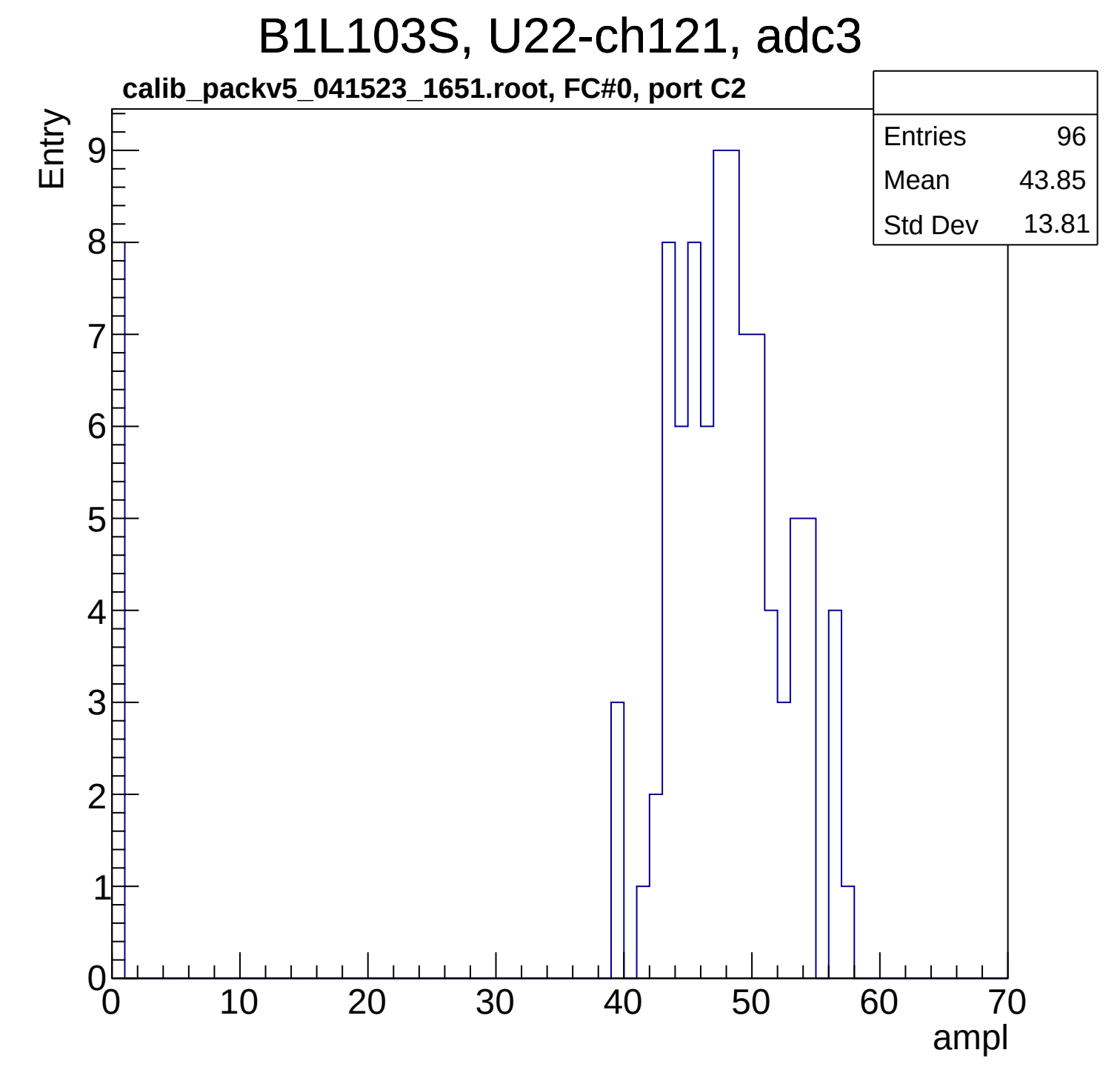
B1L103S, U22-ch121, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 96
Mean 43.85
Std Dev 13.81
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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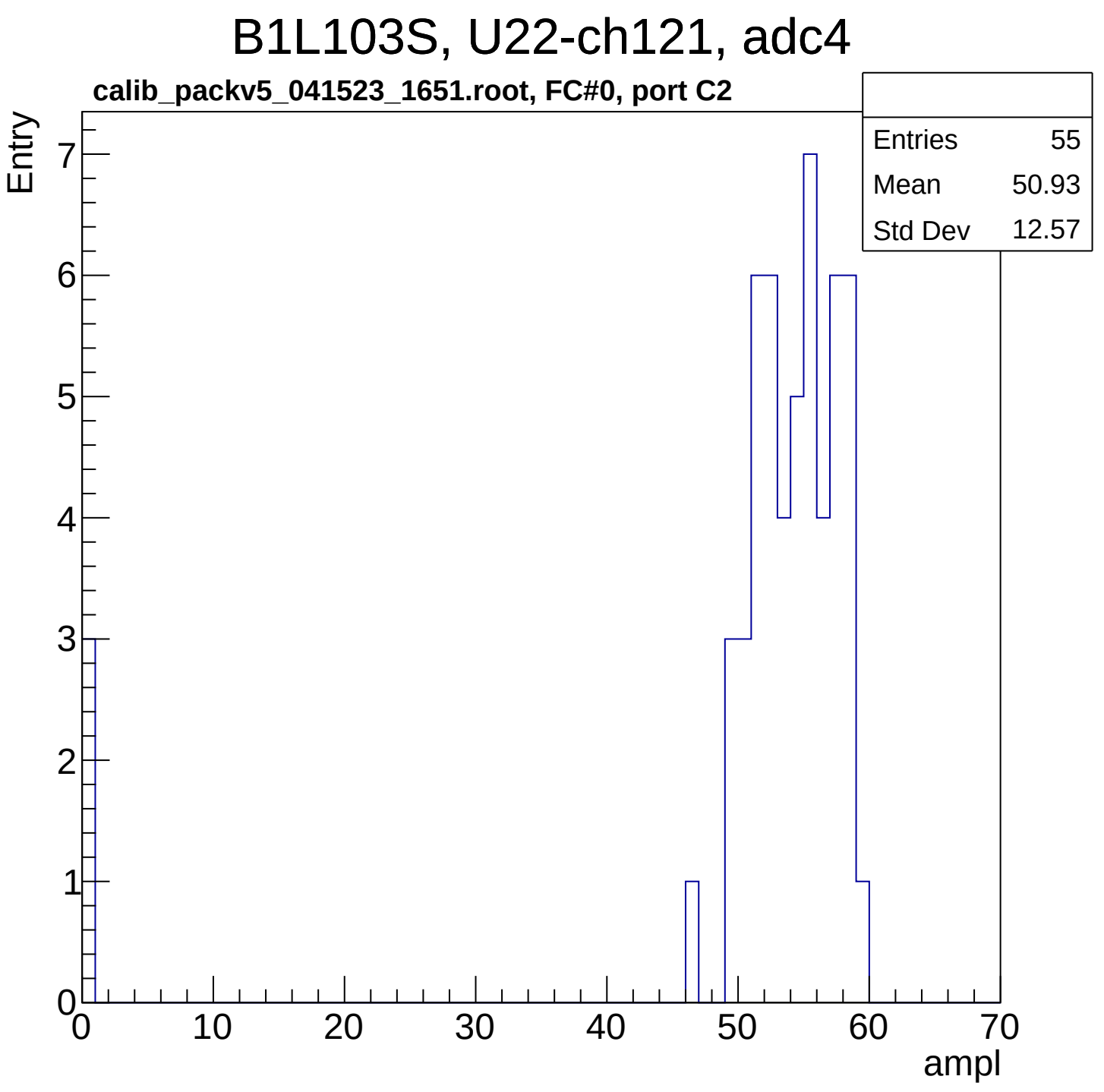
B1L103S, U22-ch121, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 50.93
Std Dev 12.57
Entry
ampl
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4
5
6
7
0
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20
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40
50
60
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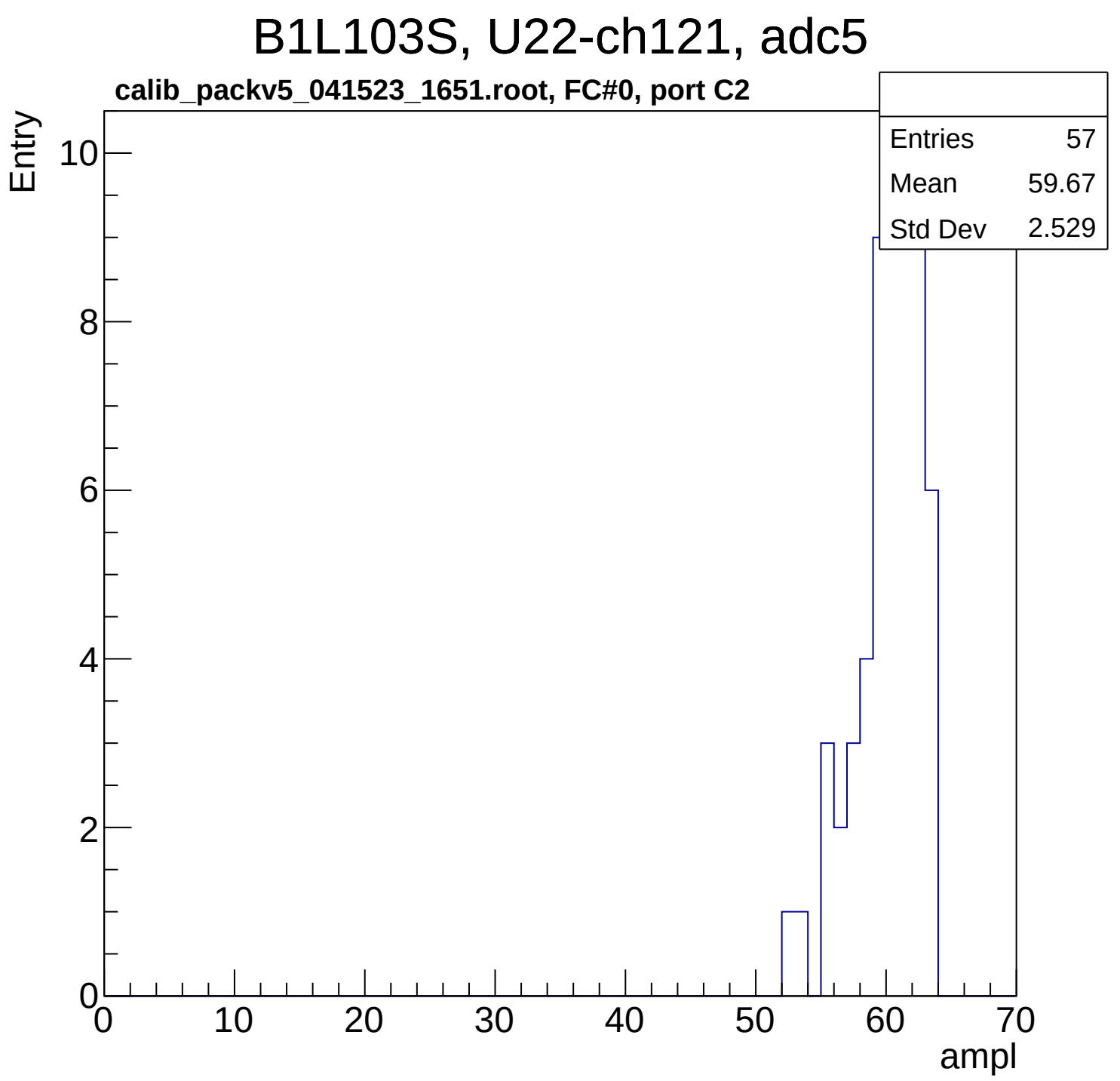
B1L103S, U22-ch121, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 59.67
Std Dev 2.529
Entry
0
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6
8
10
0
10
20
30
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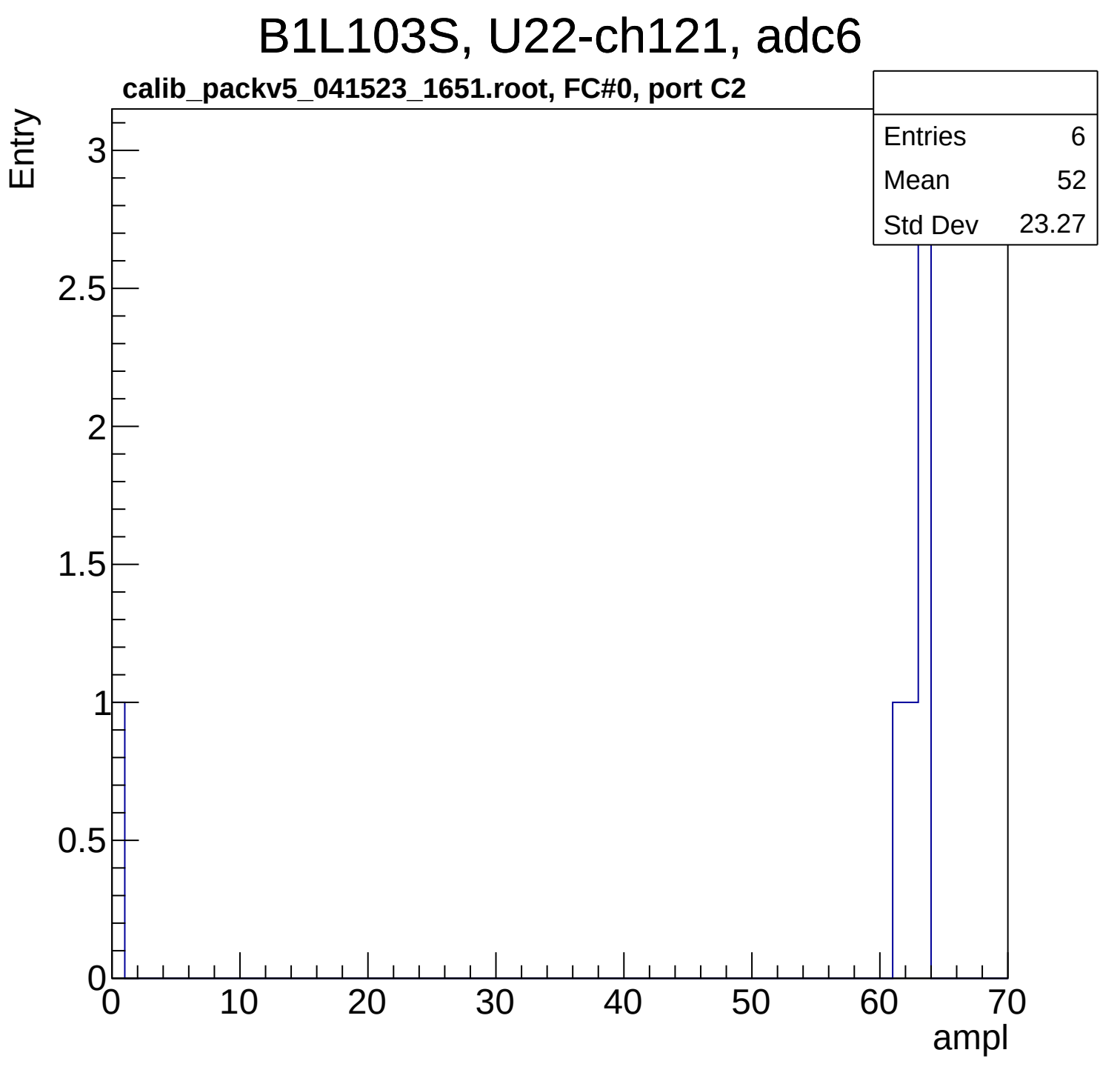
50
60
70
ampl


B1L103S, U22-ch121, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 52
Std Dev 23.27
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
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20
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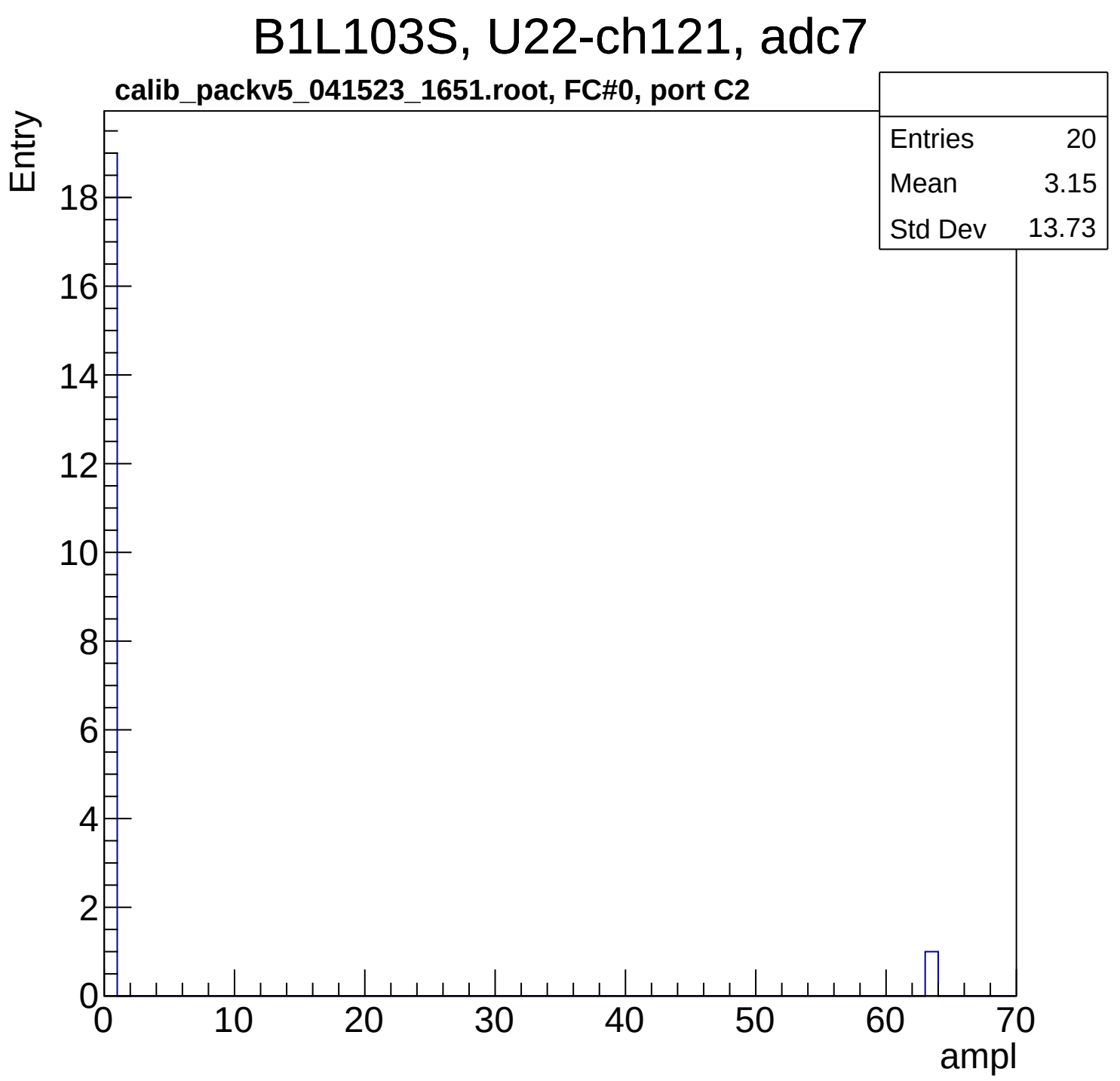
50
60
70


B1L103S, U22-ch121, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
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6
8
10
12
14
16
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10
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30
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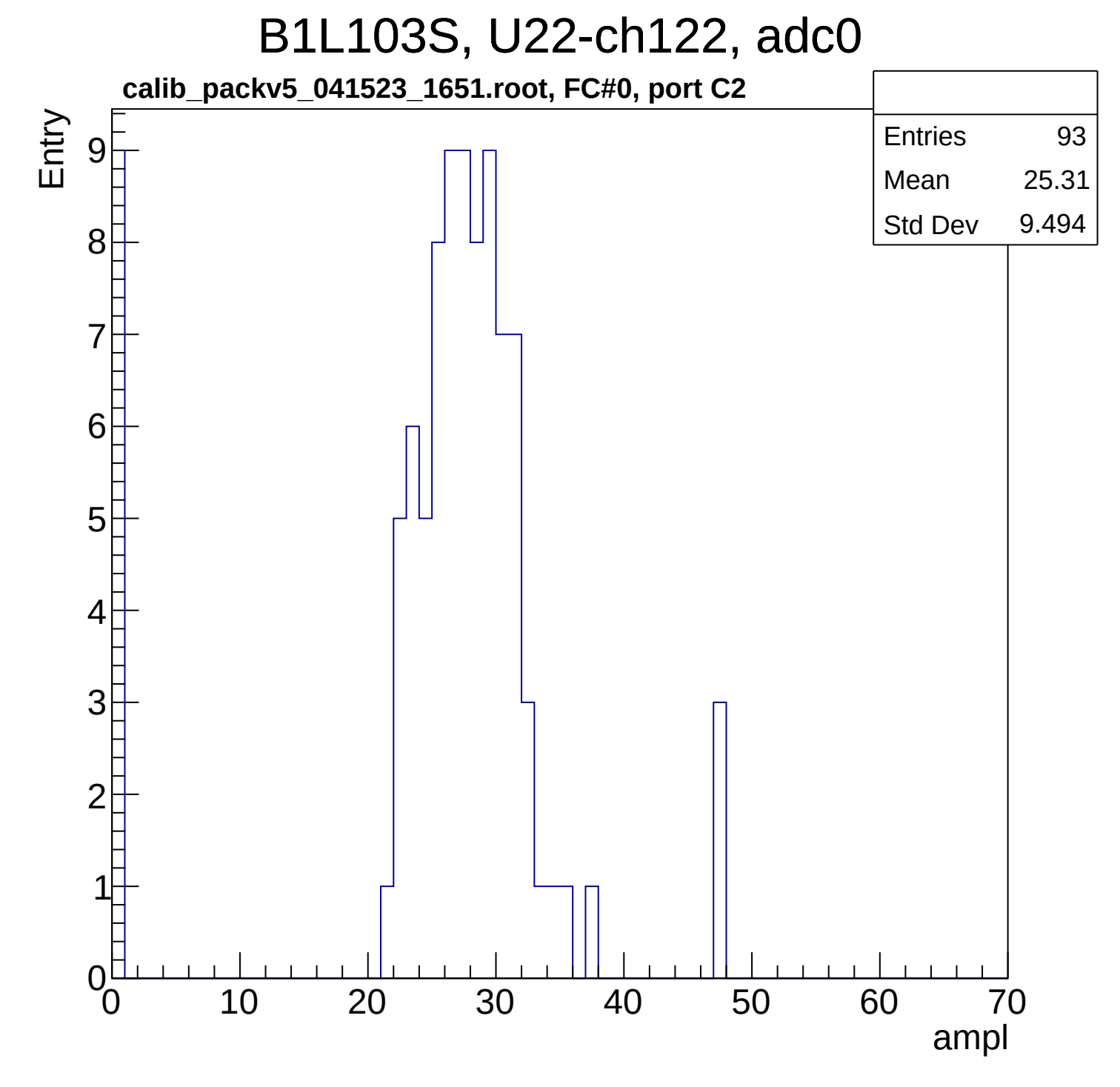
50
60
70
ampl


B1L103S, U22-ch122, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 25.31
Std Dev 9.494
Entry
ampl
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60
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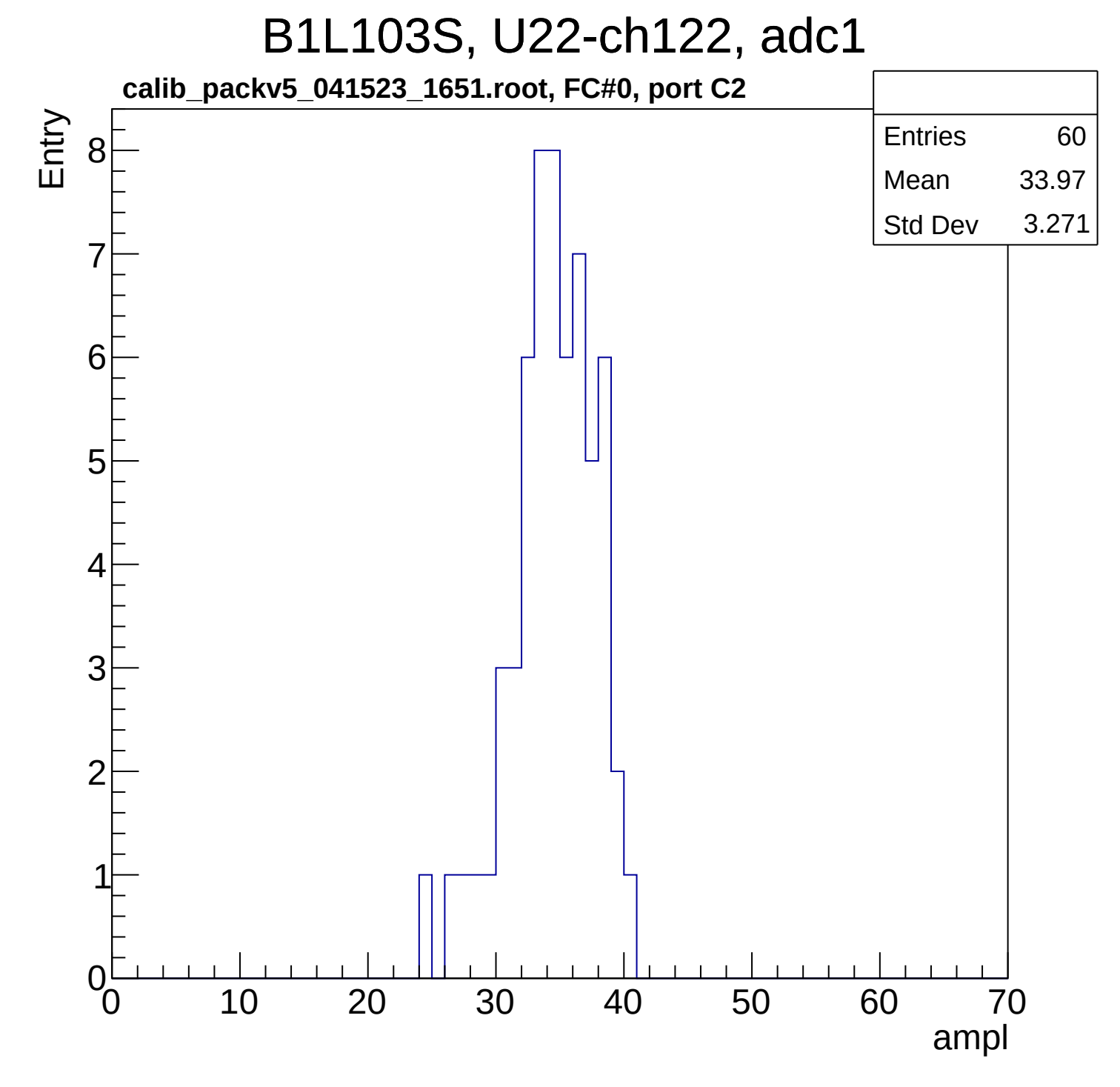
B1L103S, U22-ch122, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 33.97
Std Dev 3.271
Entry
ampl
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4
5
6
7
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0
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20
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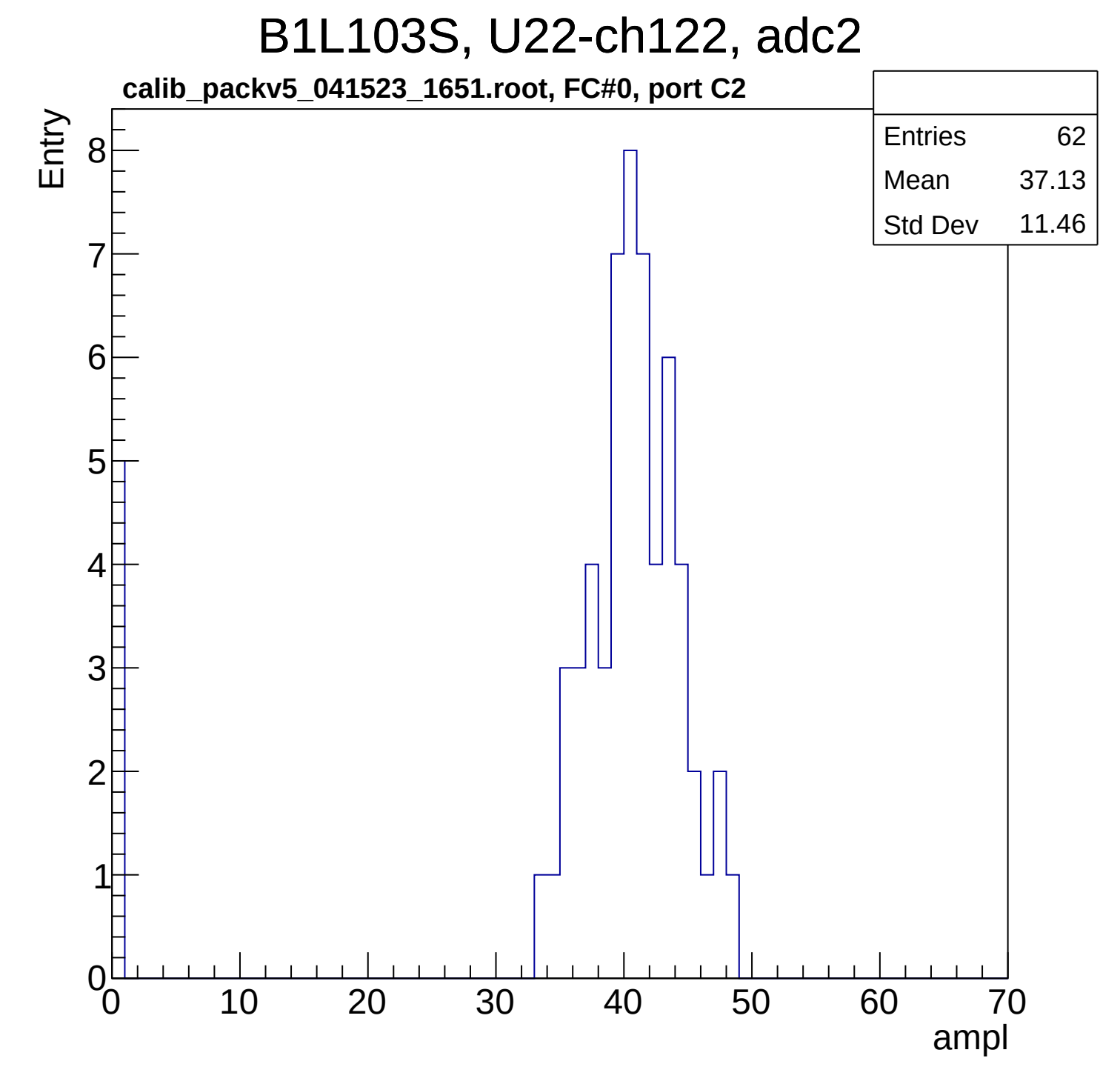
40
50
60
70


B1L103S, U22-ch122, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 37.13
Std Dev 11.46
Entry
ampl
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5
6
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0
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20
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40
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60
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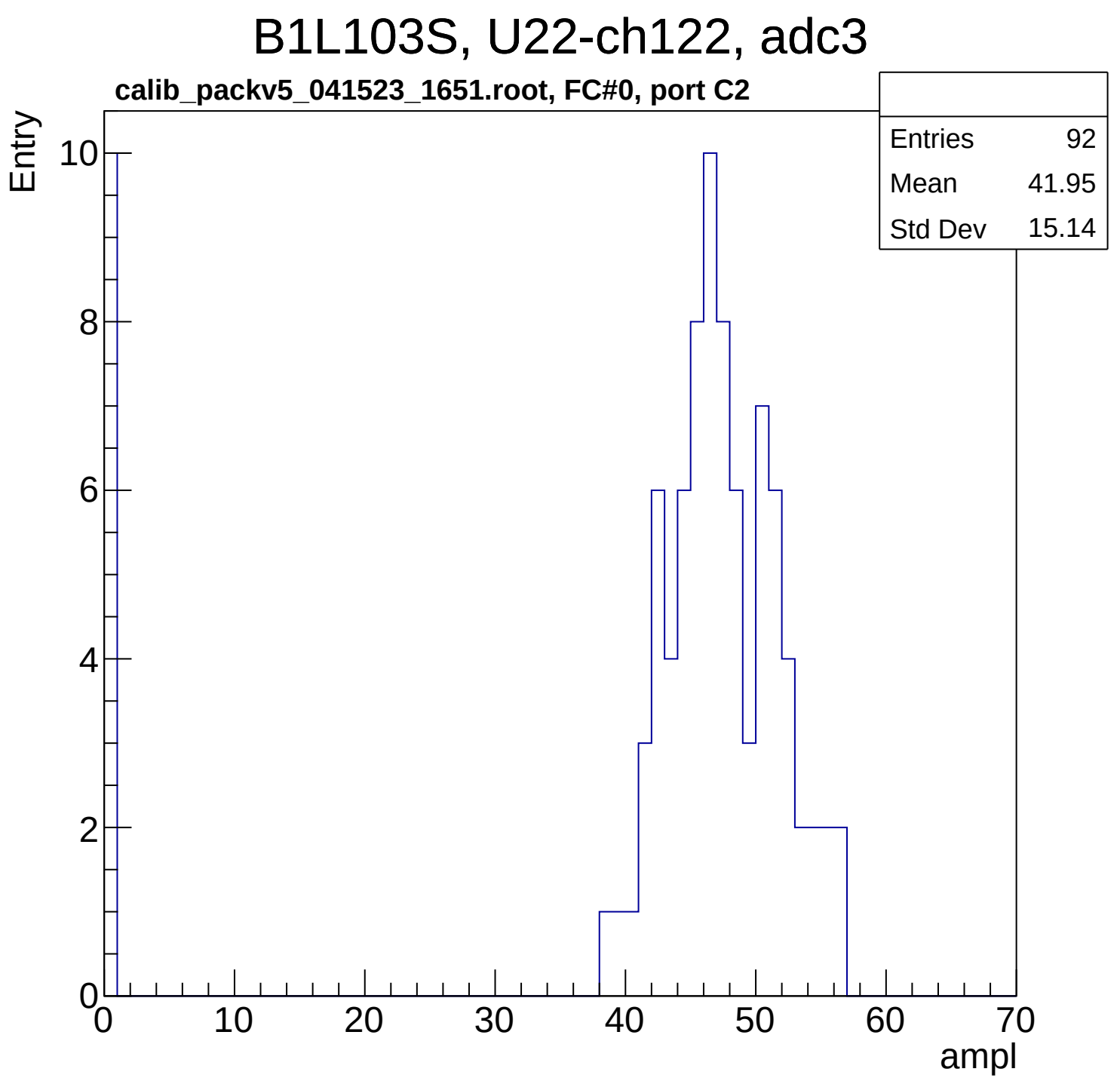
B1L103S, U22-ch122, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 41.95
Std Dev 15.14
Entry
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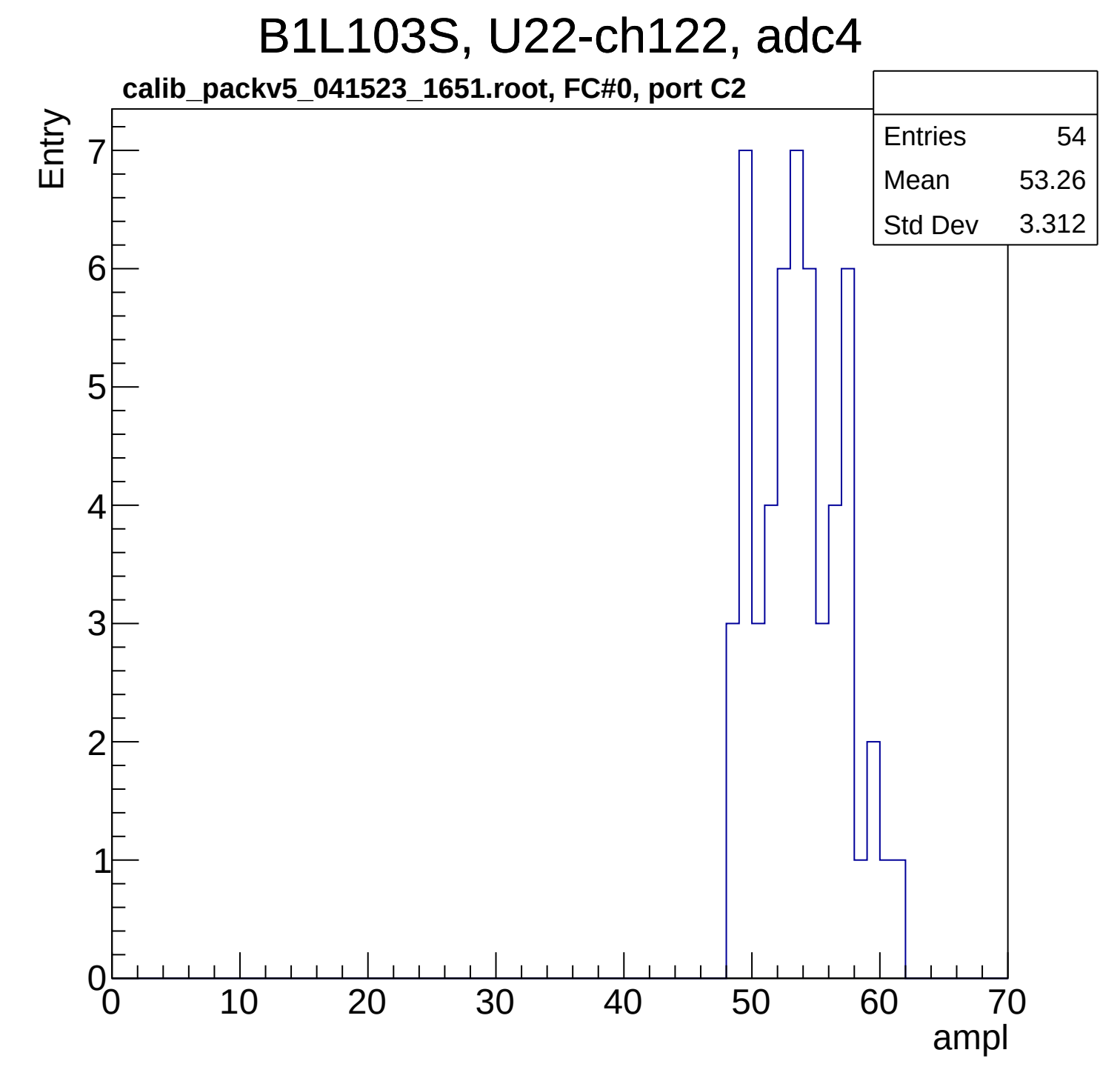
70
ampl


B1L103S, U22-ch122, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 53.26
Std Dev 3.312
Entry
ampl
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4
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0
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60
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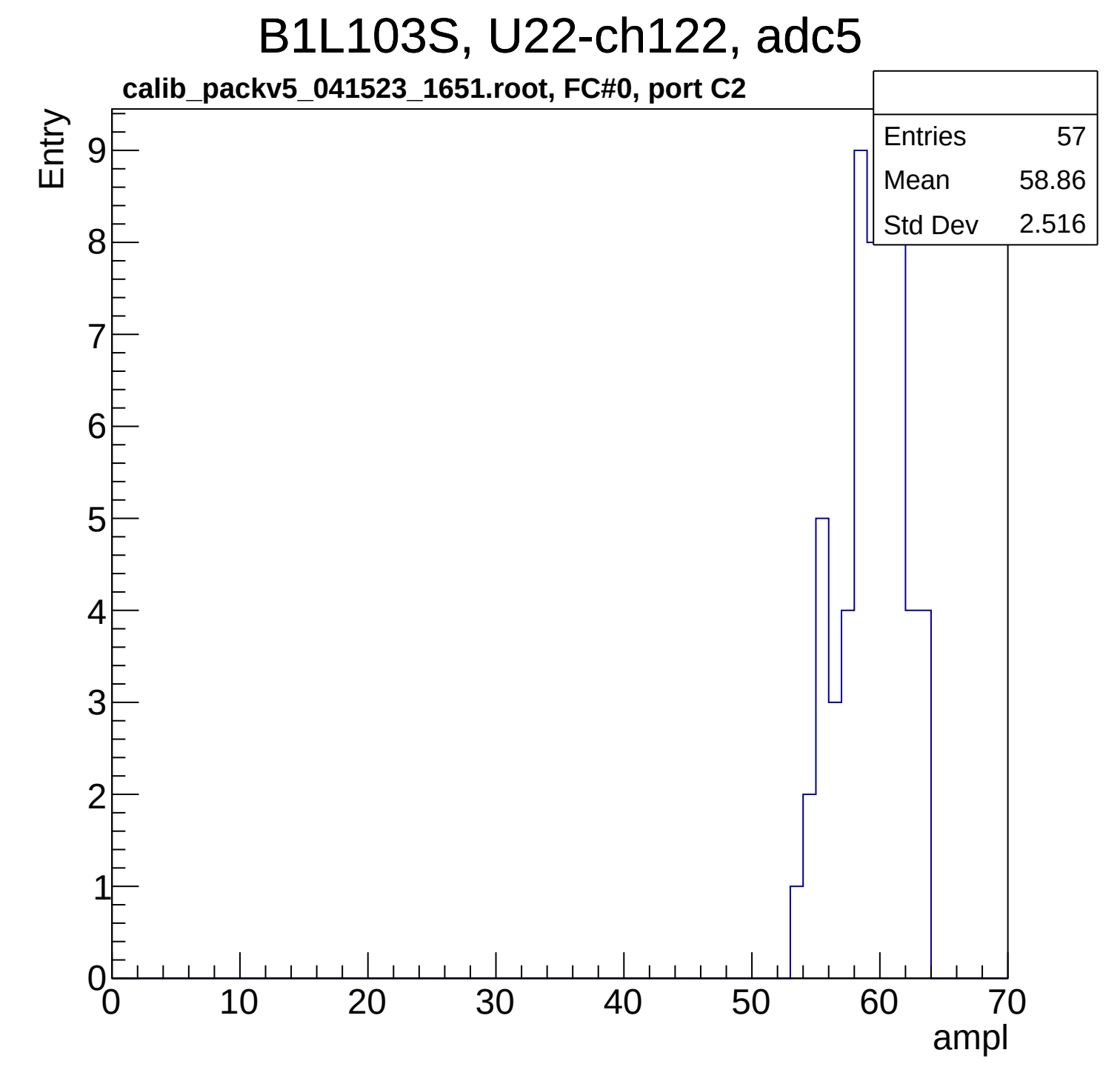
B1L103S, U22-ch122, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 58.86
Std Dev 2.516
Entry
ampl
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3
4
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6
7
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0
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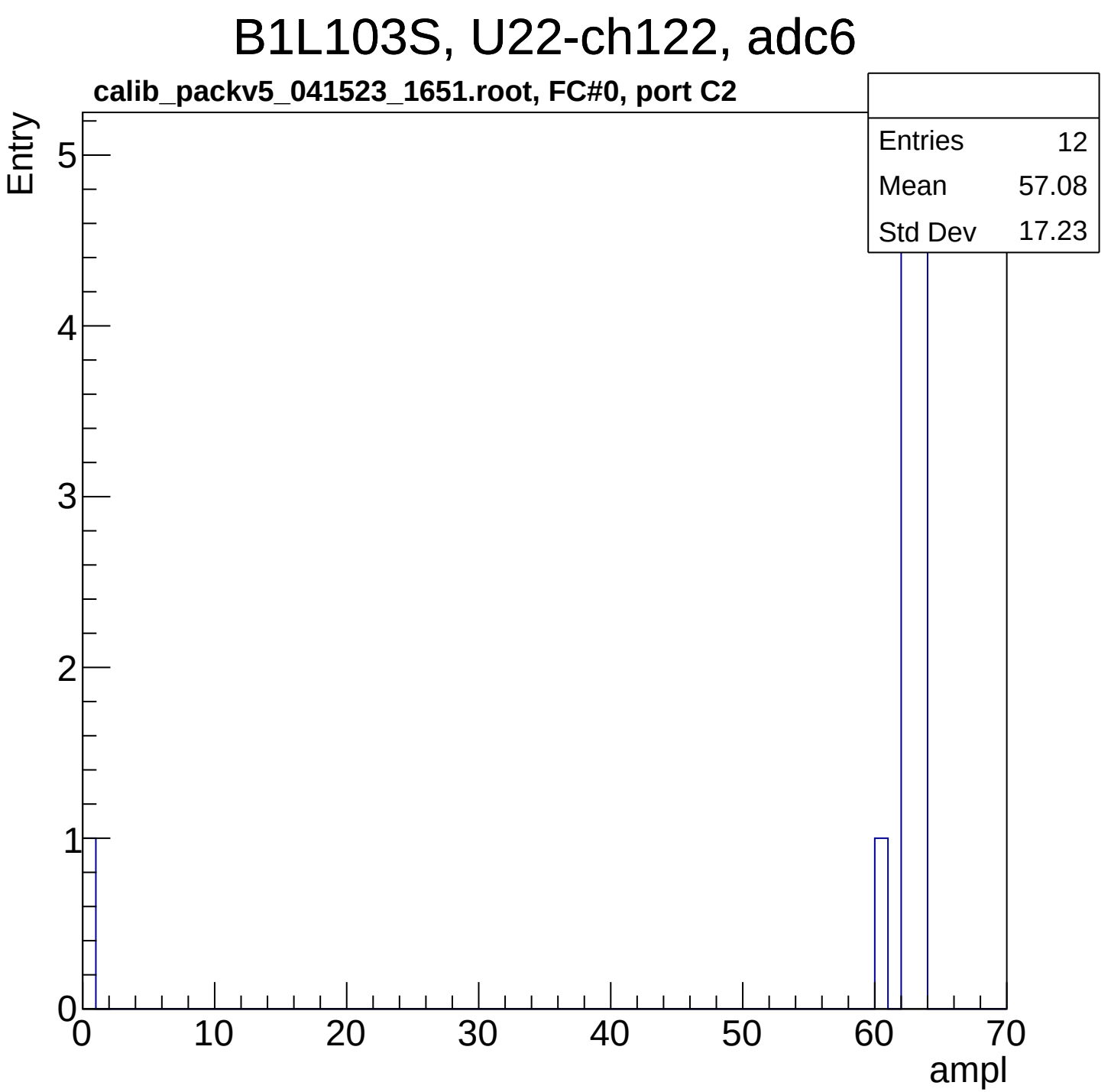
B1L103S, U22-ch122, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 57.08
Std Dev 17.23
Entry
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2
3
4
5
0
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50
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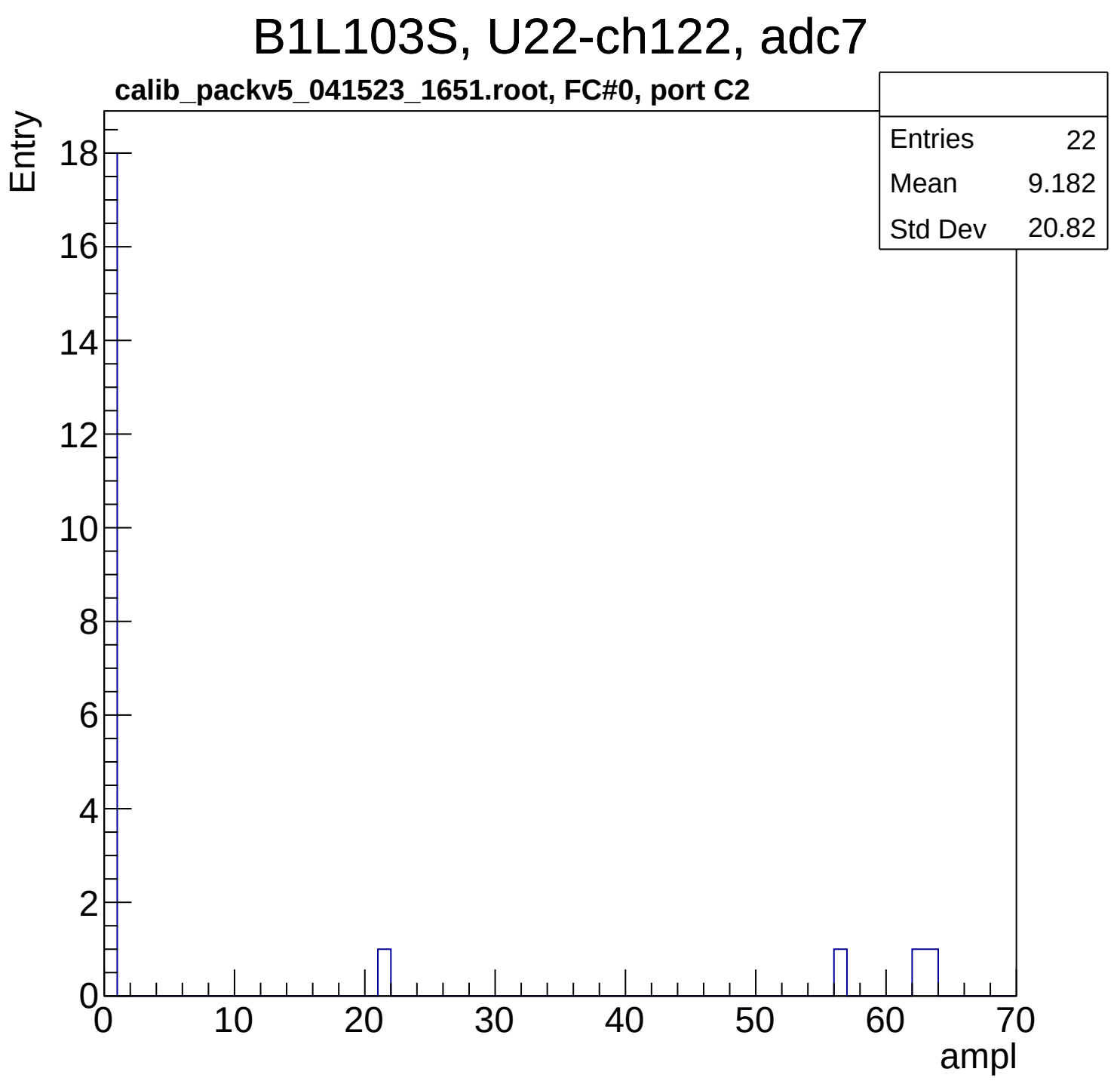
70
ampl


B1L103S, U22-ch122, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 9.182
Std Dev 20.82
Entry
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8
10
12
14
16
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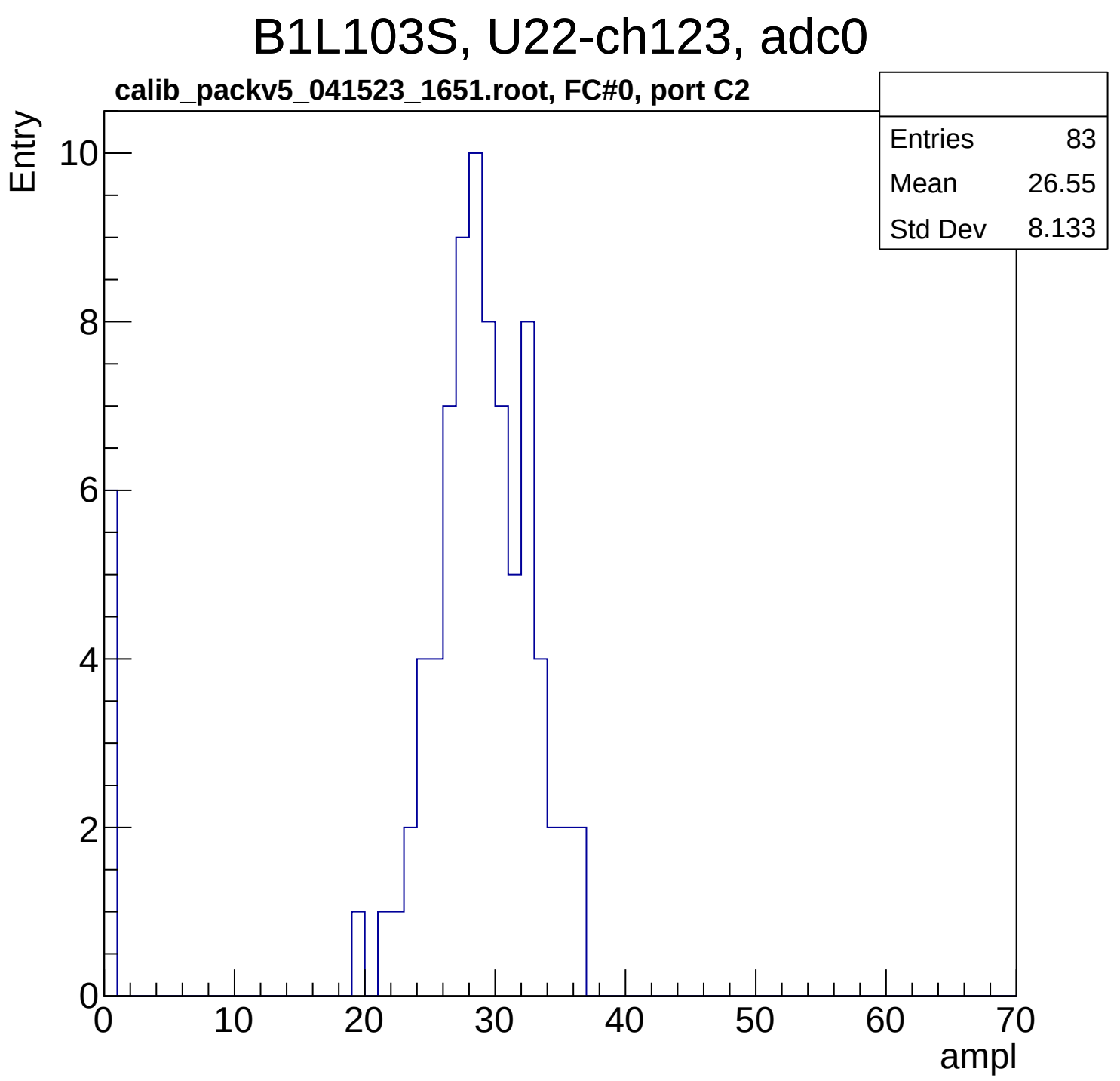
70
ampl


B1L103S, U22-ch123, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 26.55
Std Dev 8.133
Entry
0
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4
6
8
10
0
10
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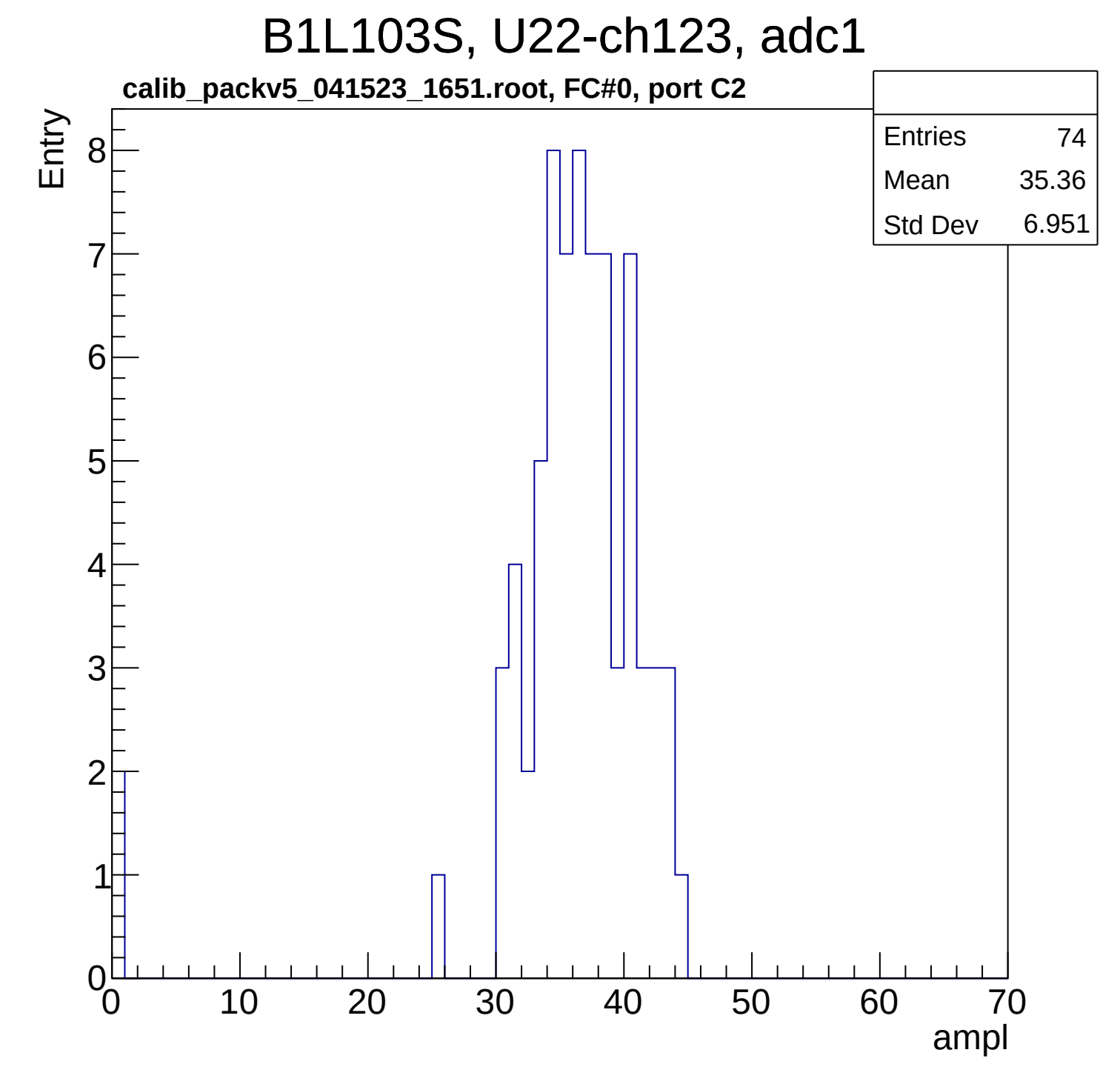
50
60
70
ampl


B1L103S, U22-ch123, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 35.36
Std Dev 6.951
Entry
ampl
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2
3
4
5
6
7
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0
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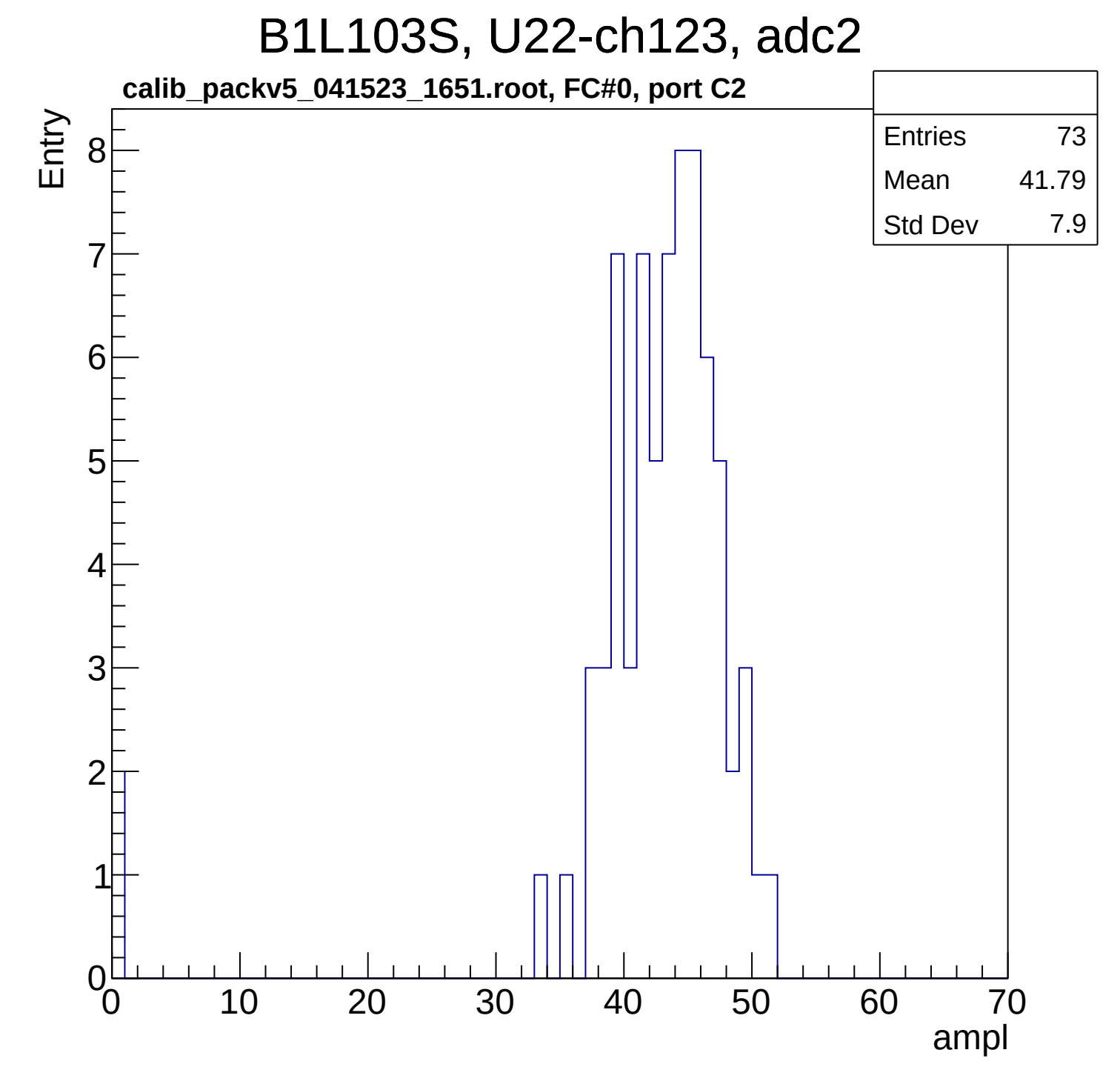
B1L103S, U22-ch123, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 41.79
Std Dev 7.9
Entry
ampl
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2
3
4
5
6
7
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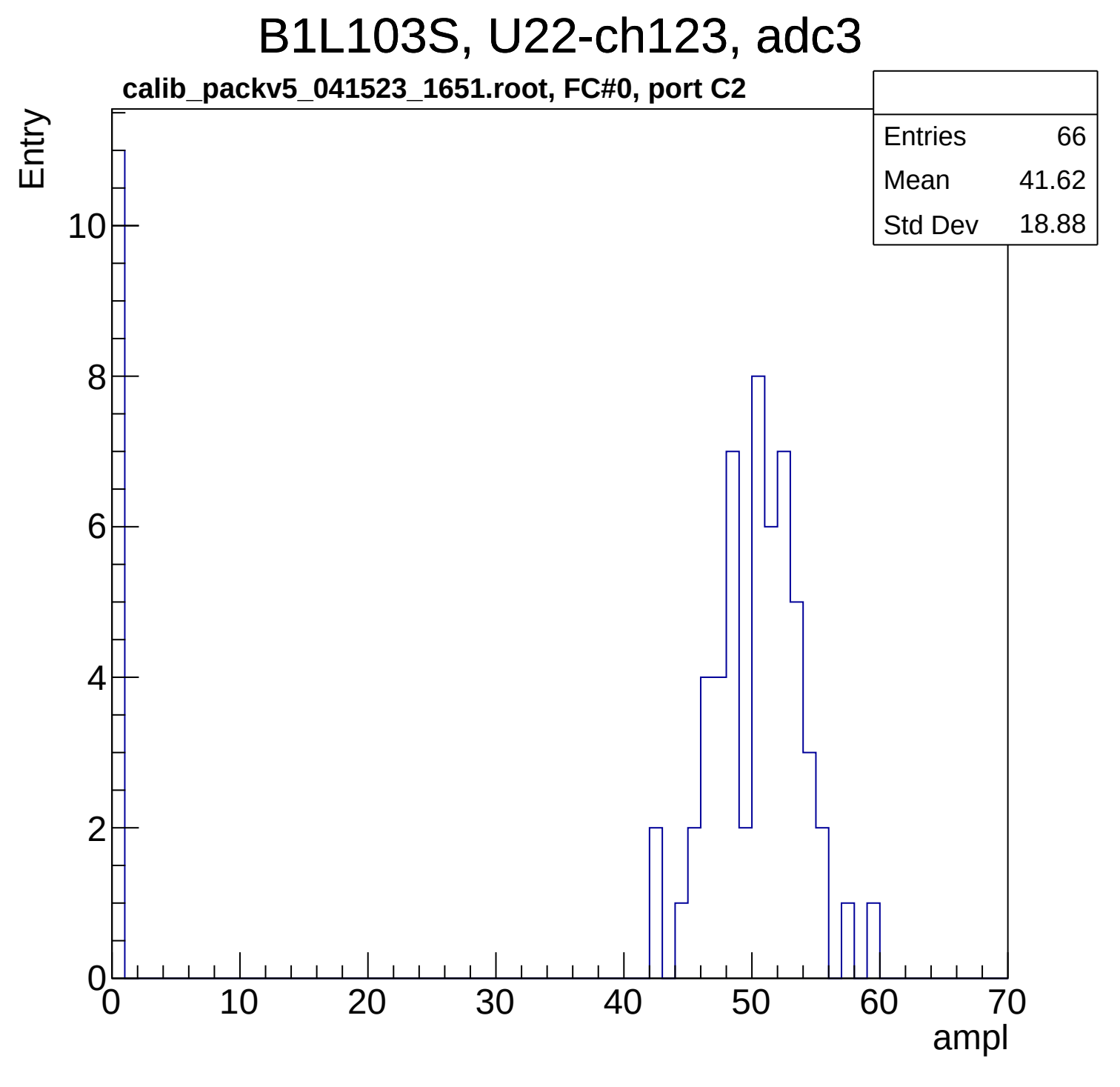
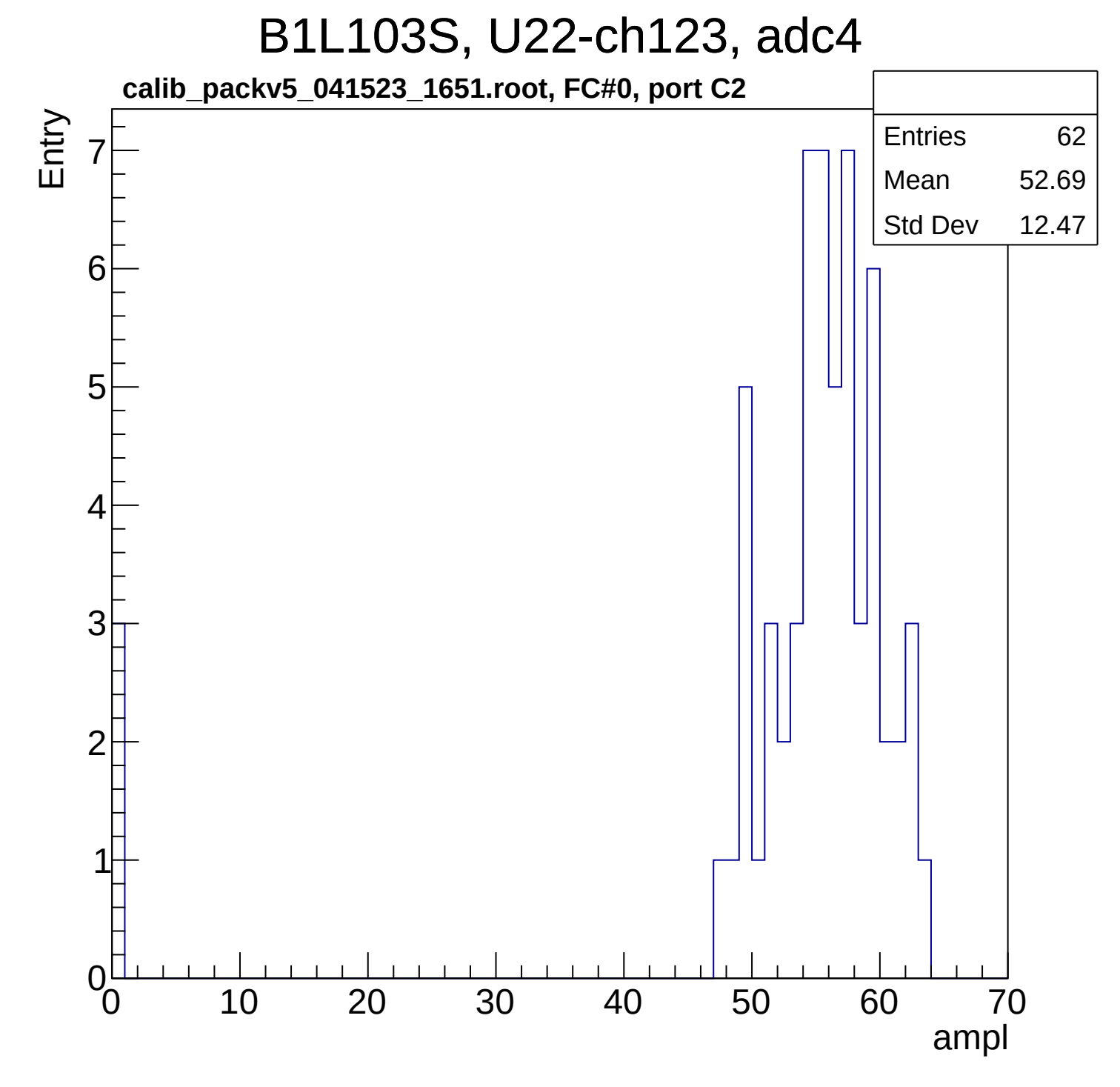
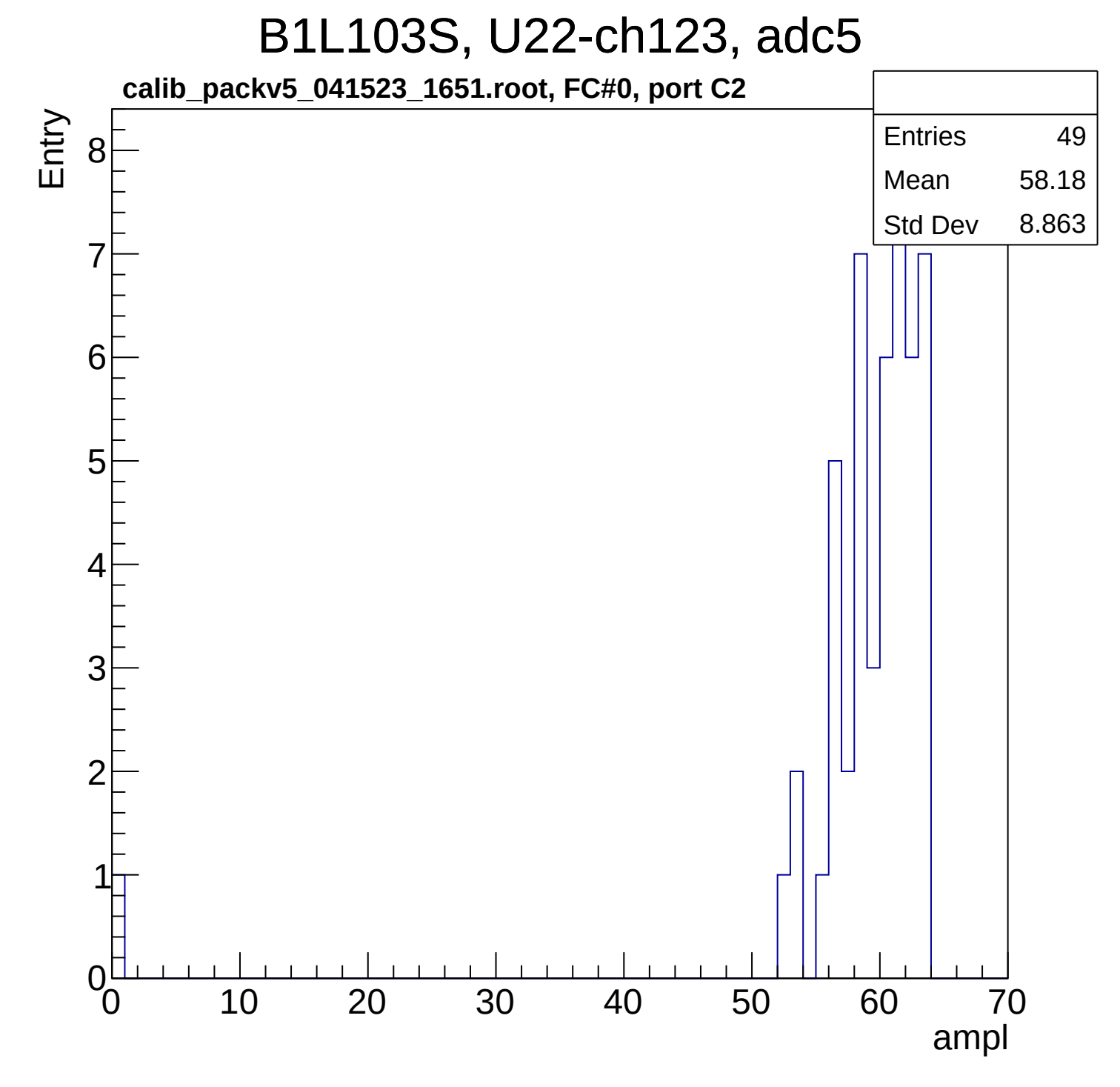

B1L103S, U22-ch123, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 41.62
Std Dev 18.88
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U22-ch123, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 52.69
Std Dev 12.47
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U22-ch123, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 58.18
Std Dev 8.863
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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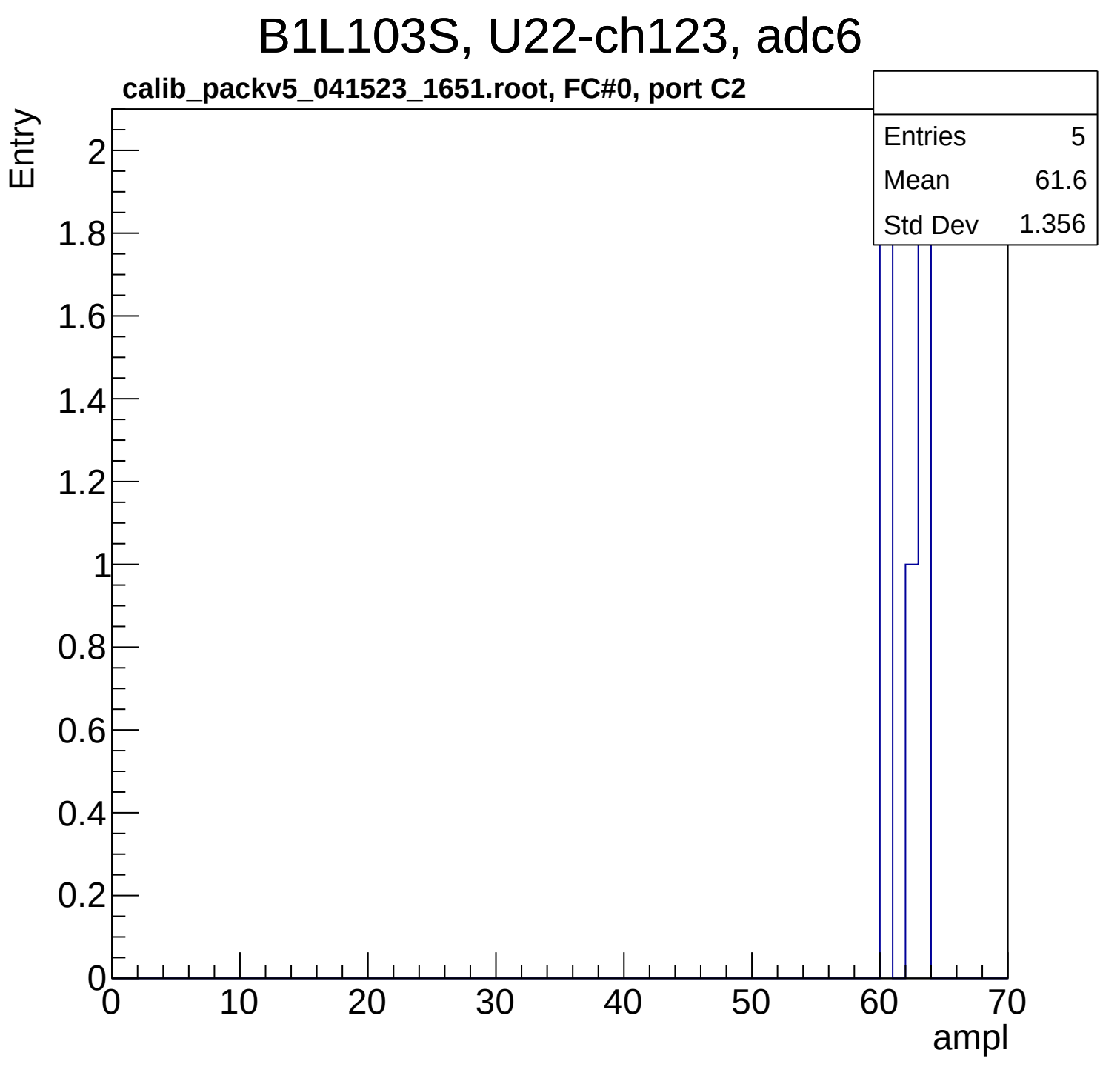
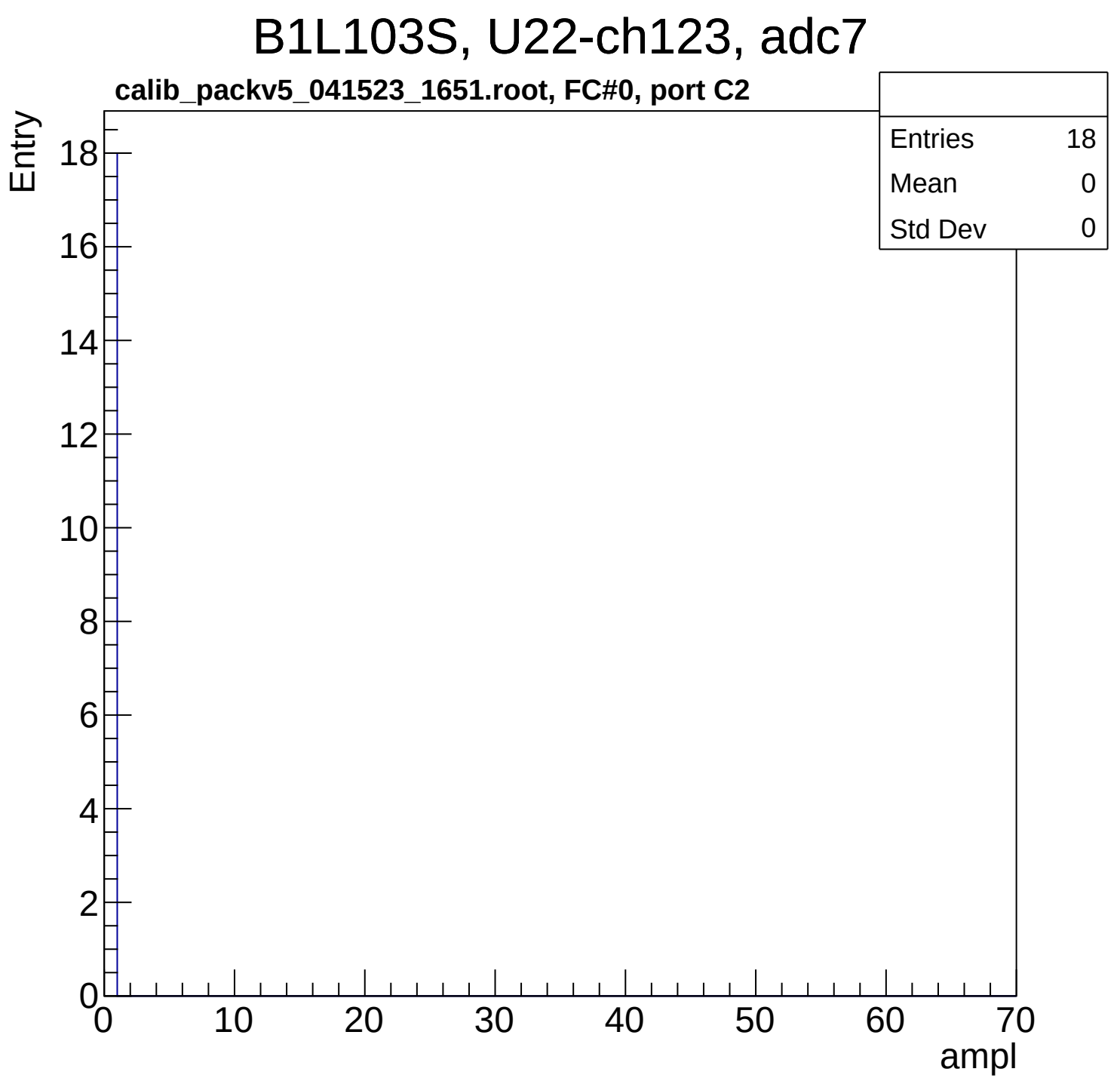
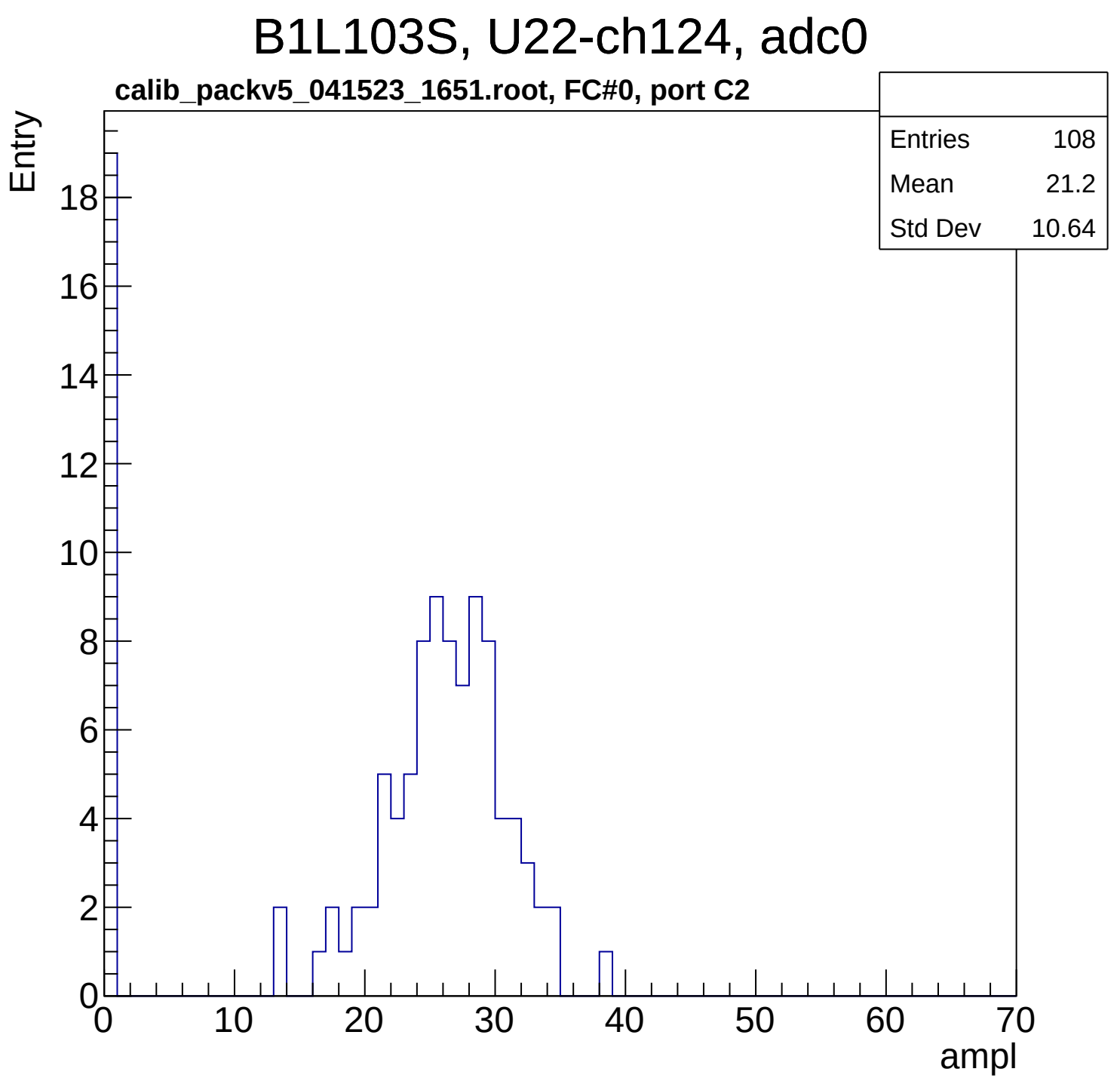

B1L103S, U22-ch123, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 61.6
Std Dev 1.356
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U22-ch123, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch124, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 108
Mean 21.2
Std Dev 10.64
Entry
0
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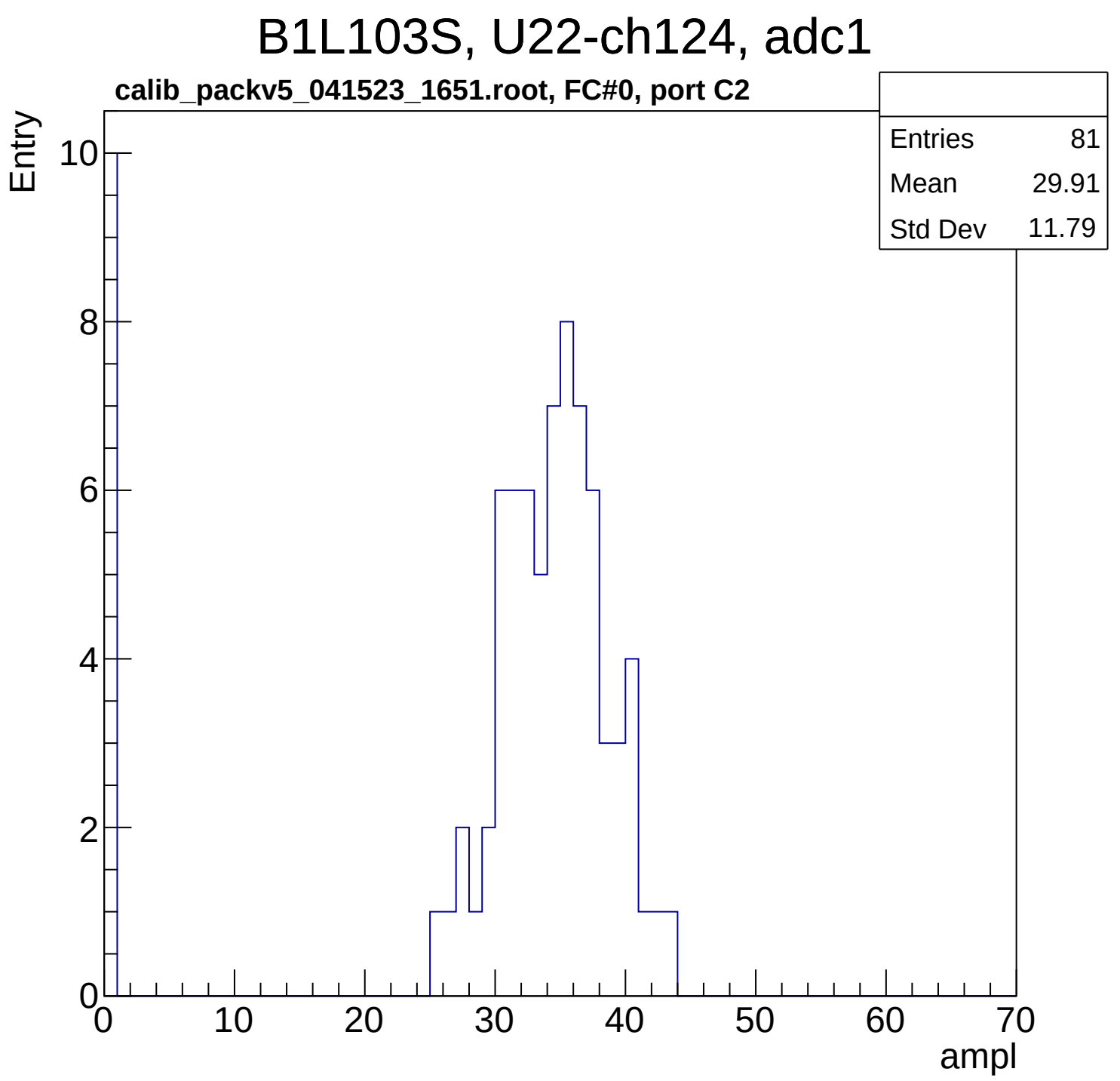
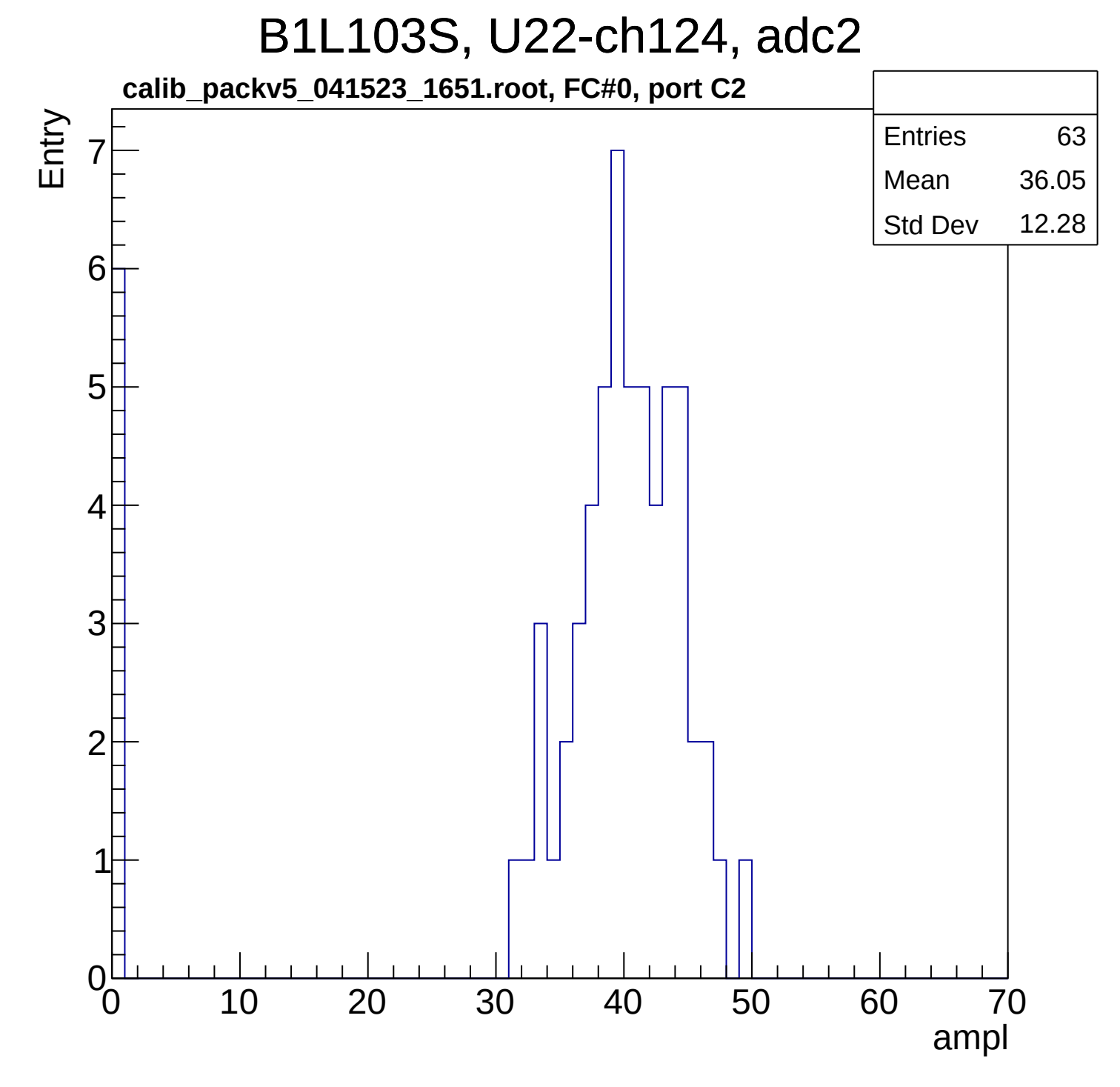
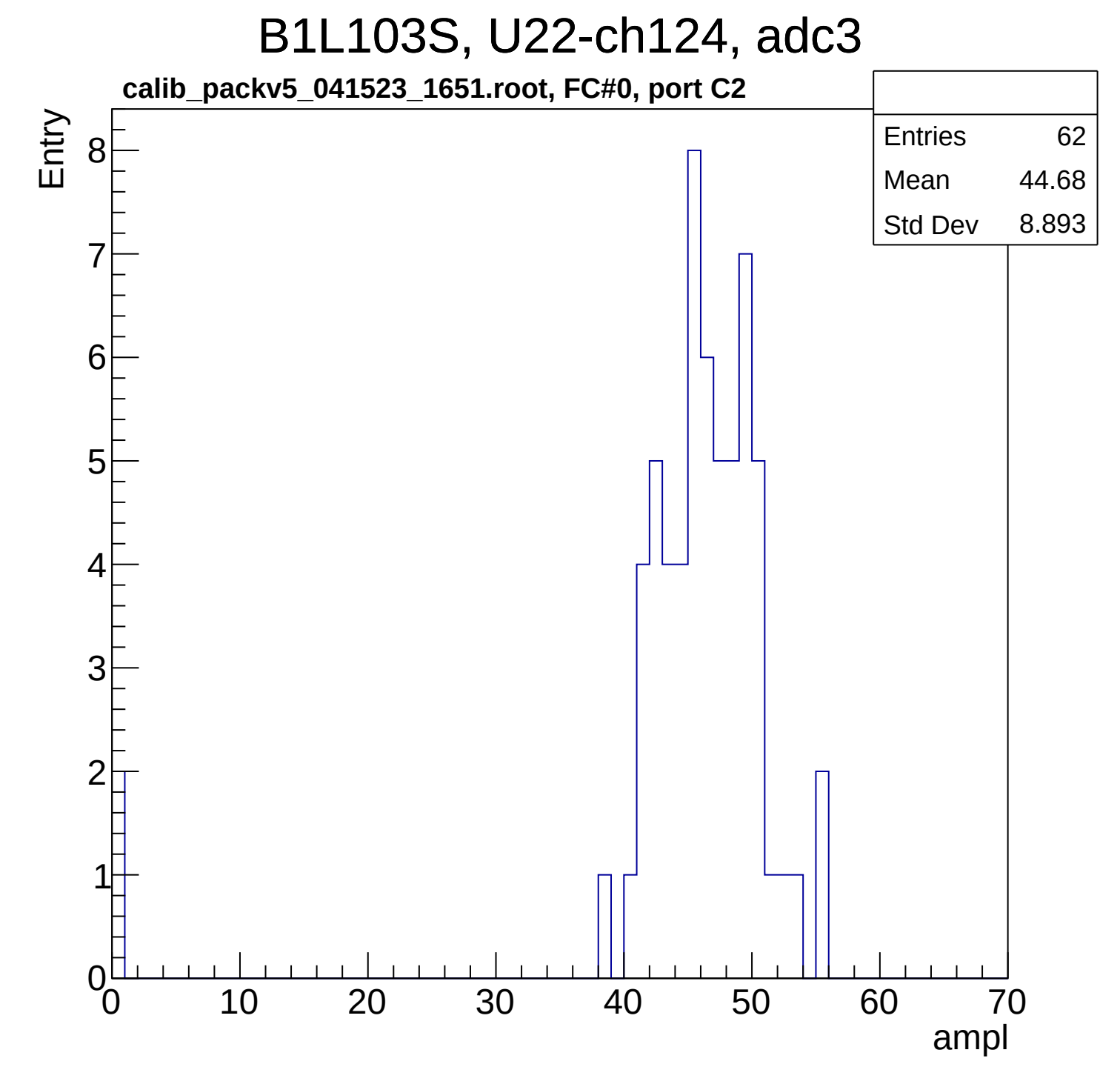
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch124, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 29.91
Std Dev 11.79
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch124, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 36.05
Std Dev 12.28
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U22-ch124, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 44.68
Std Dev 8.893
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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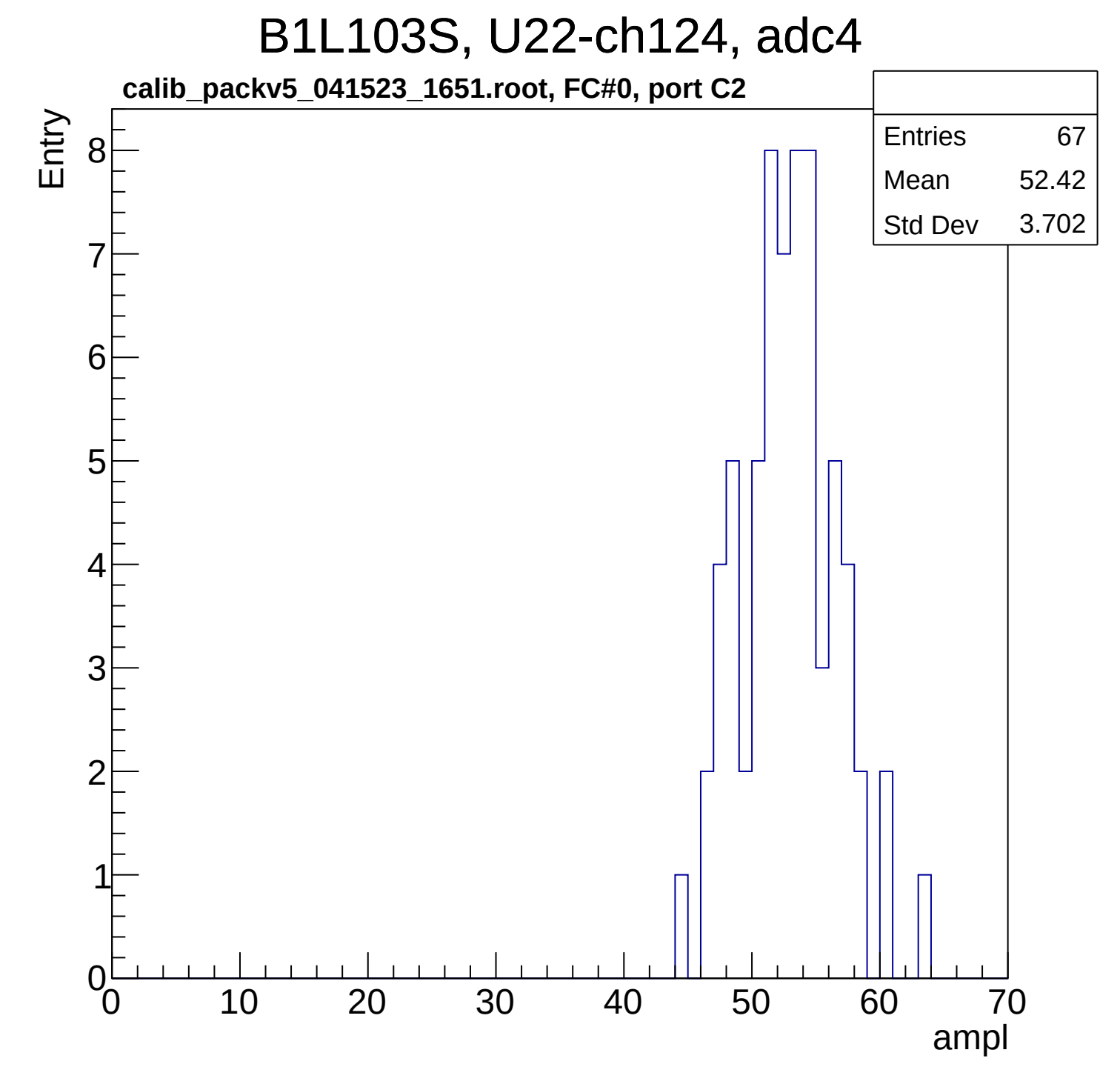
B1L103S, U22-ch124, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 52.42
Std Dev 3.702
Entry
ampl
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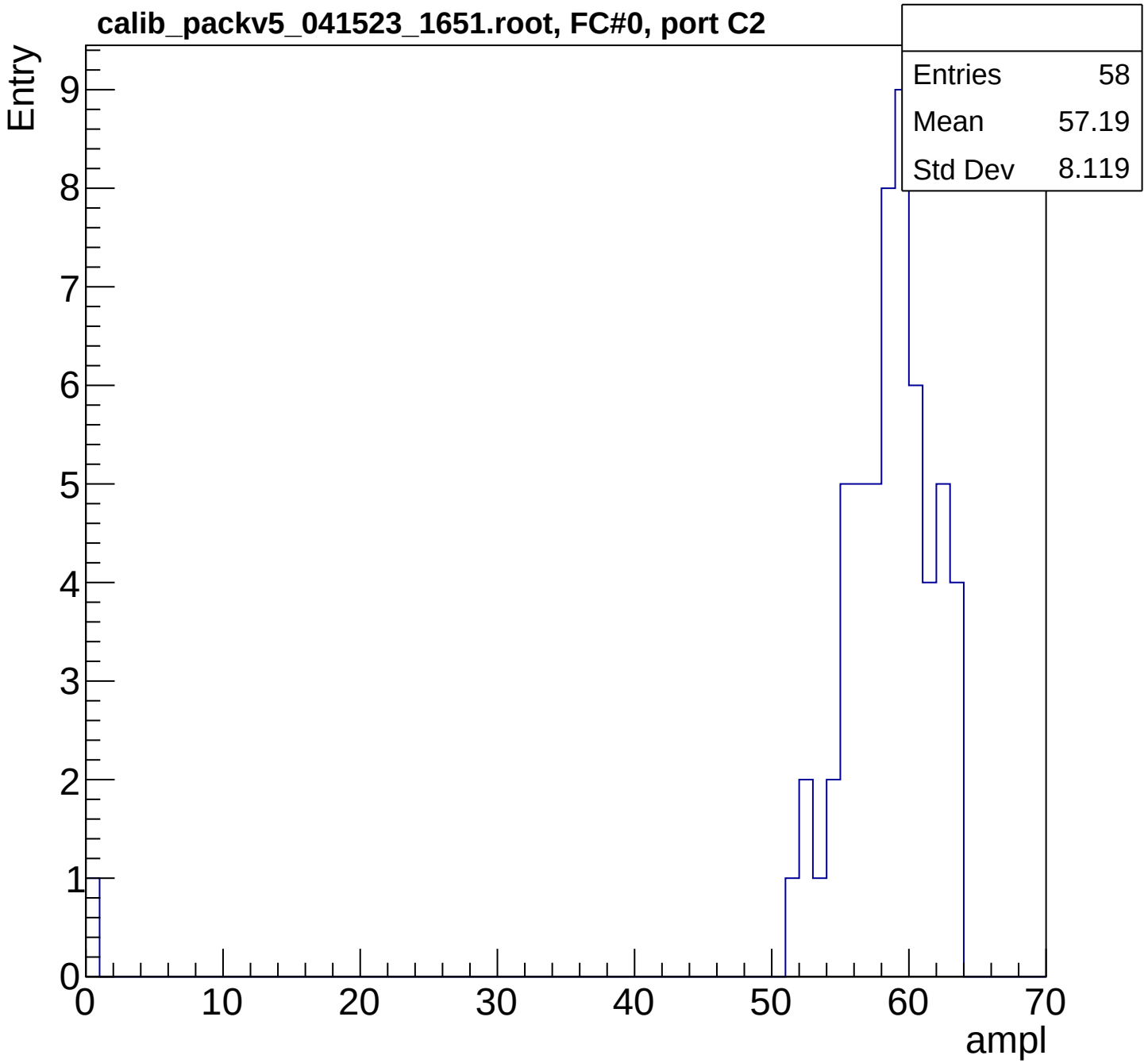
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch124, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 57.19
Std Dev 8.119
Entry
ampl
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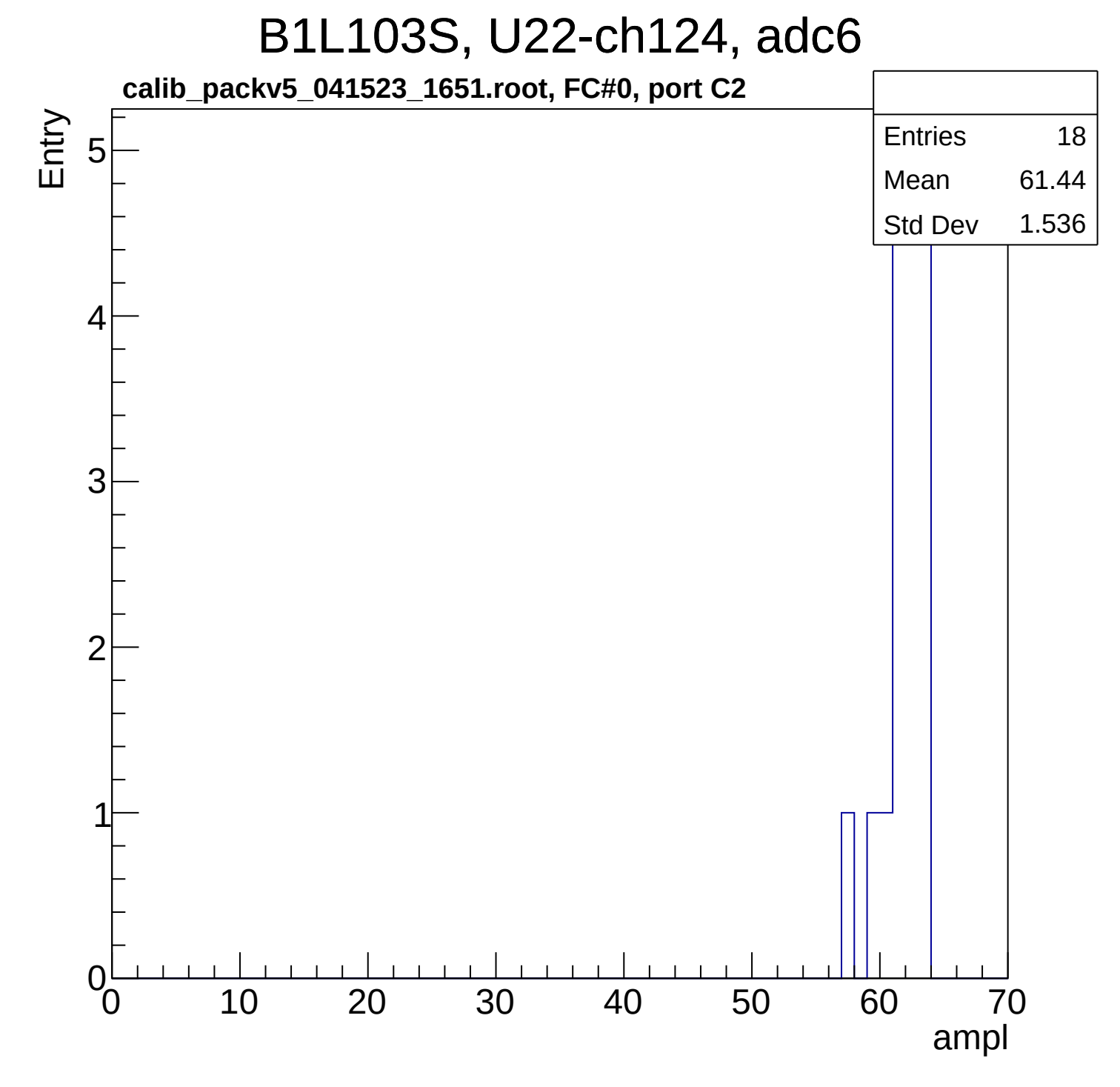
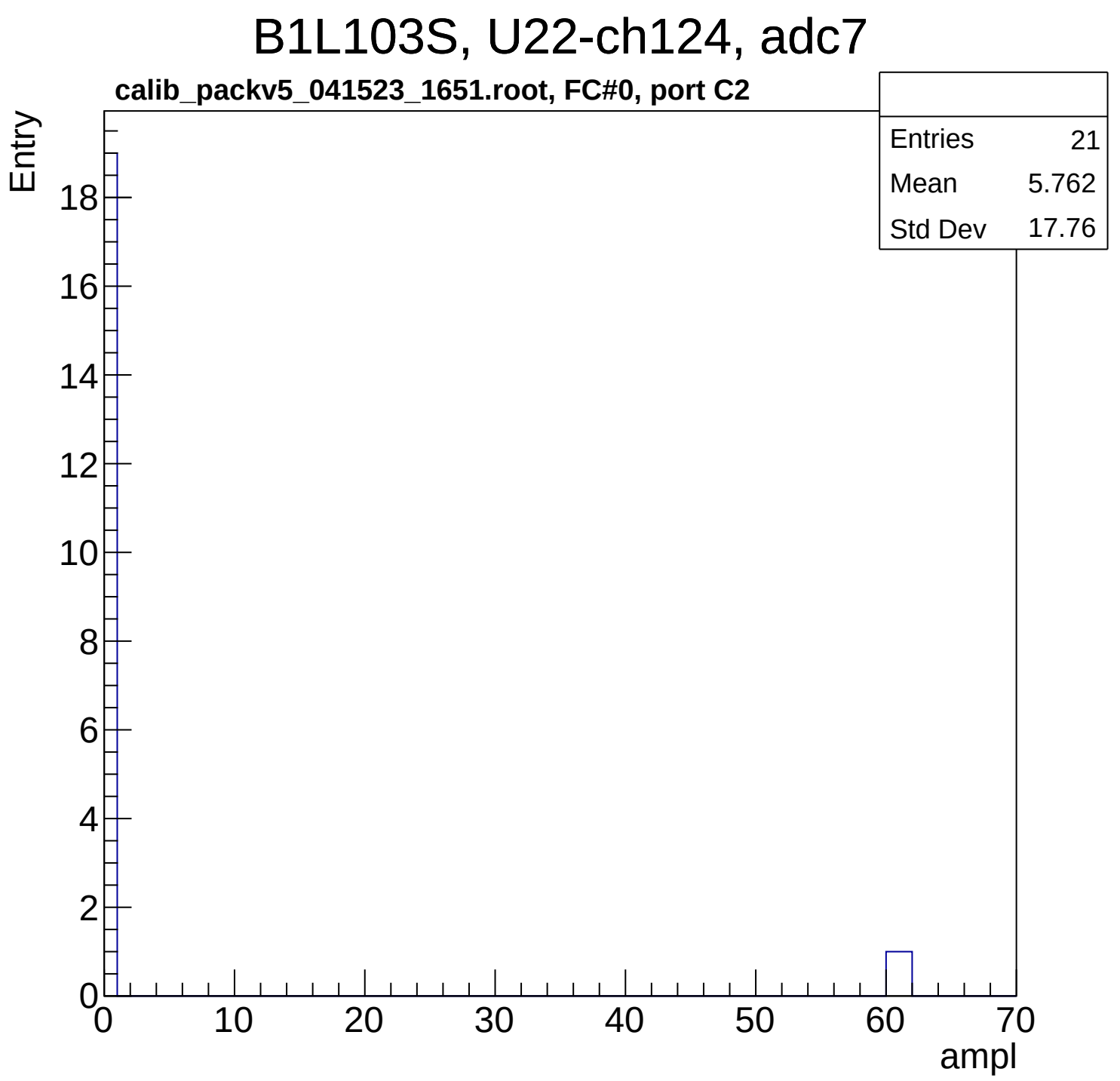
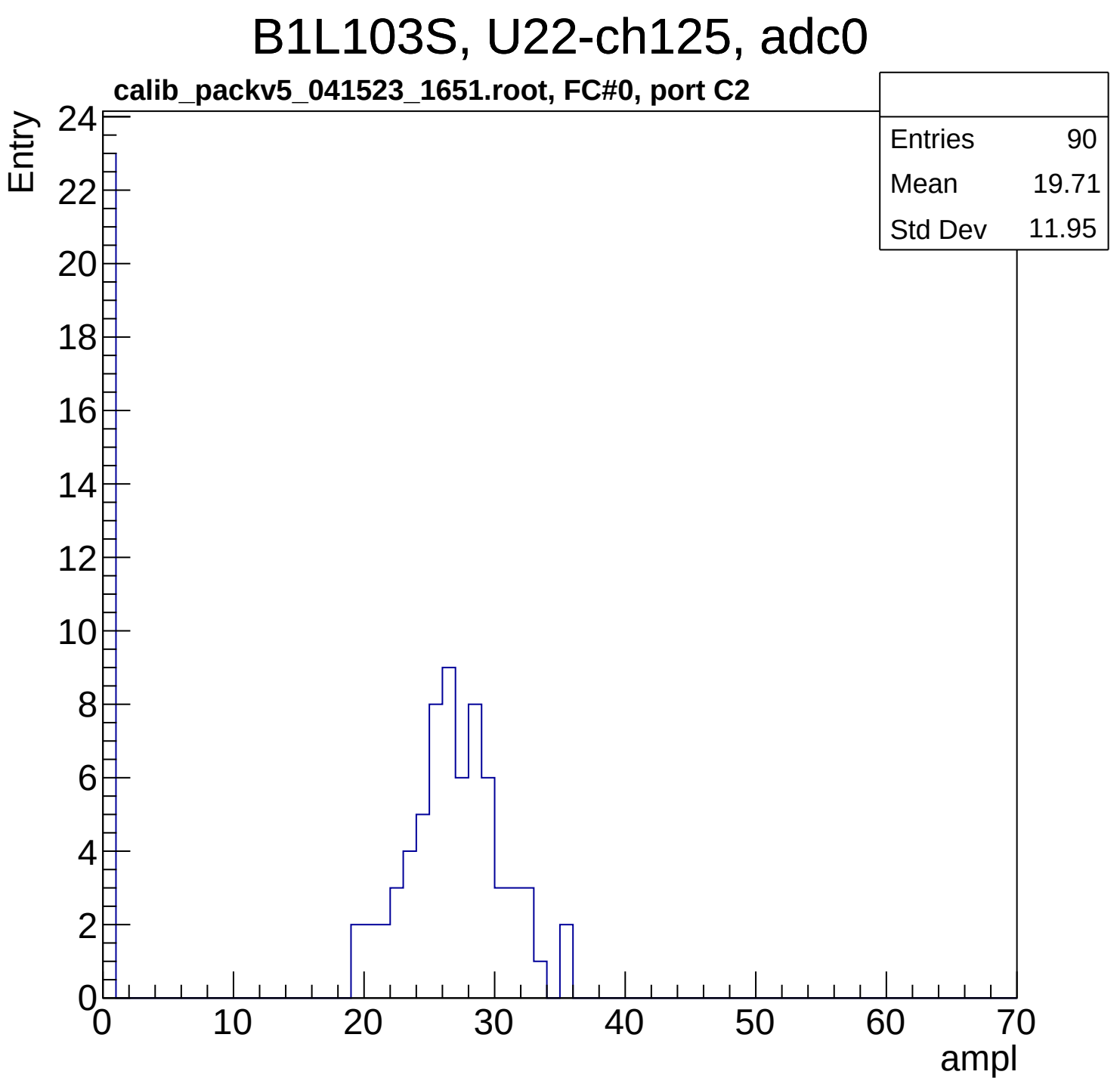
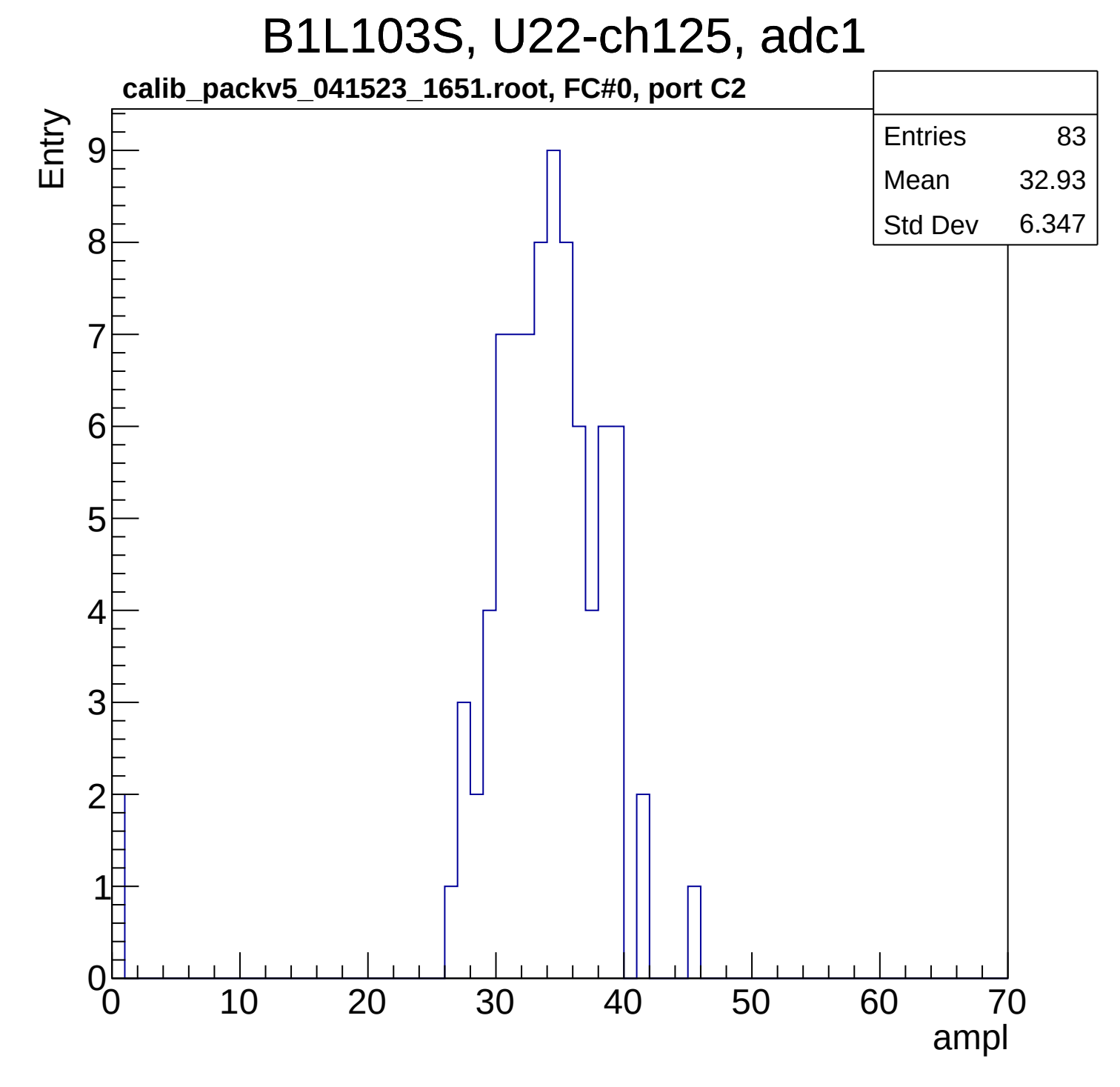
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch124, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 61.44
Std Dev 1.536
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U22-ch124, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.762
Std Dev 17.76
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch125, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 19.71
Std Dev 11.95
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
24
0
10
20
30
40
50
60
70


B1L103S, U22-ch125, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 32.93
Std Dev 6.347
Entry
ampl
0
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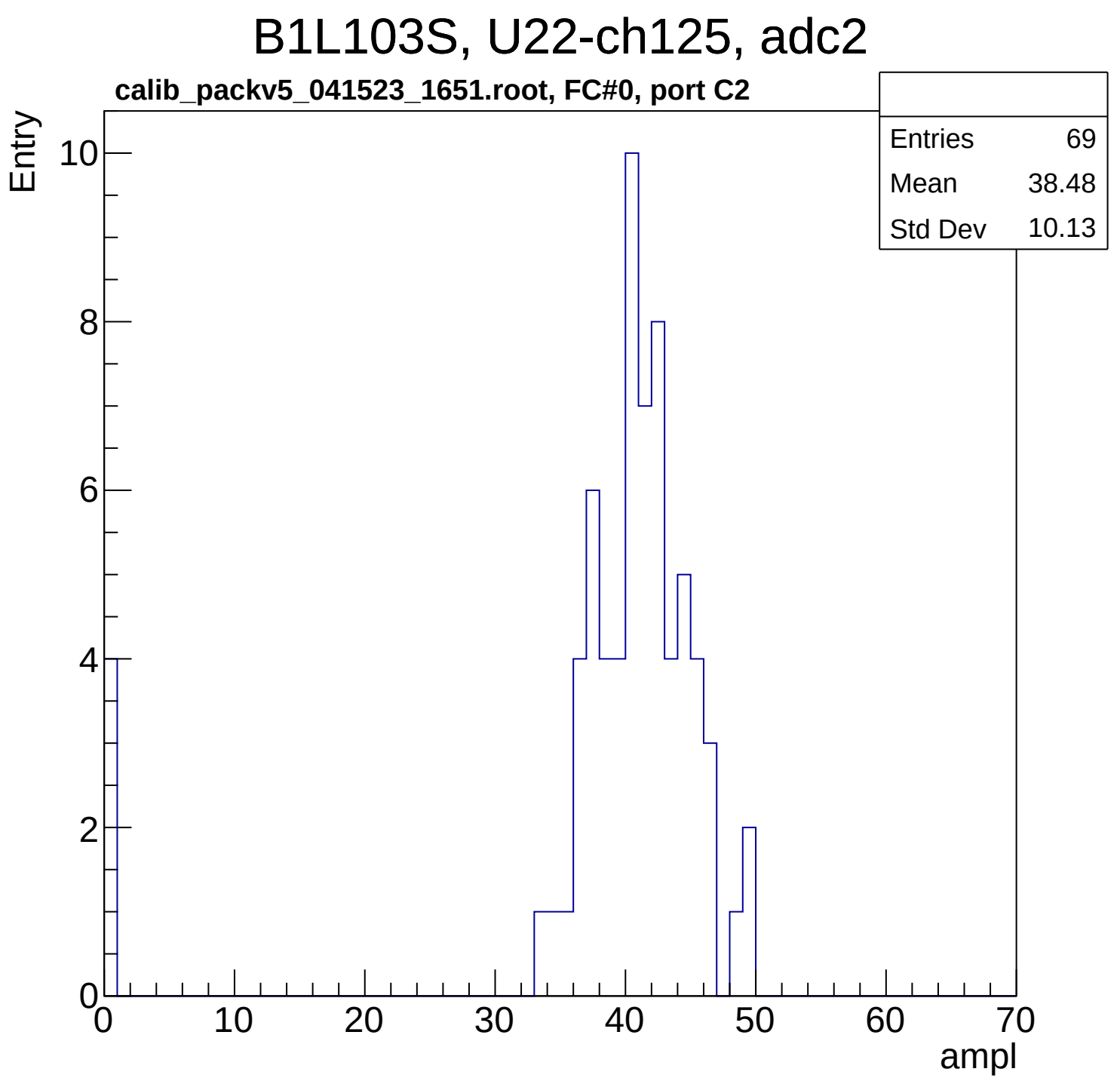
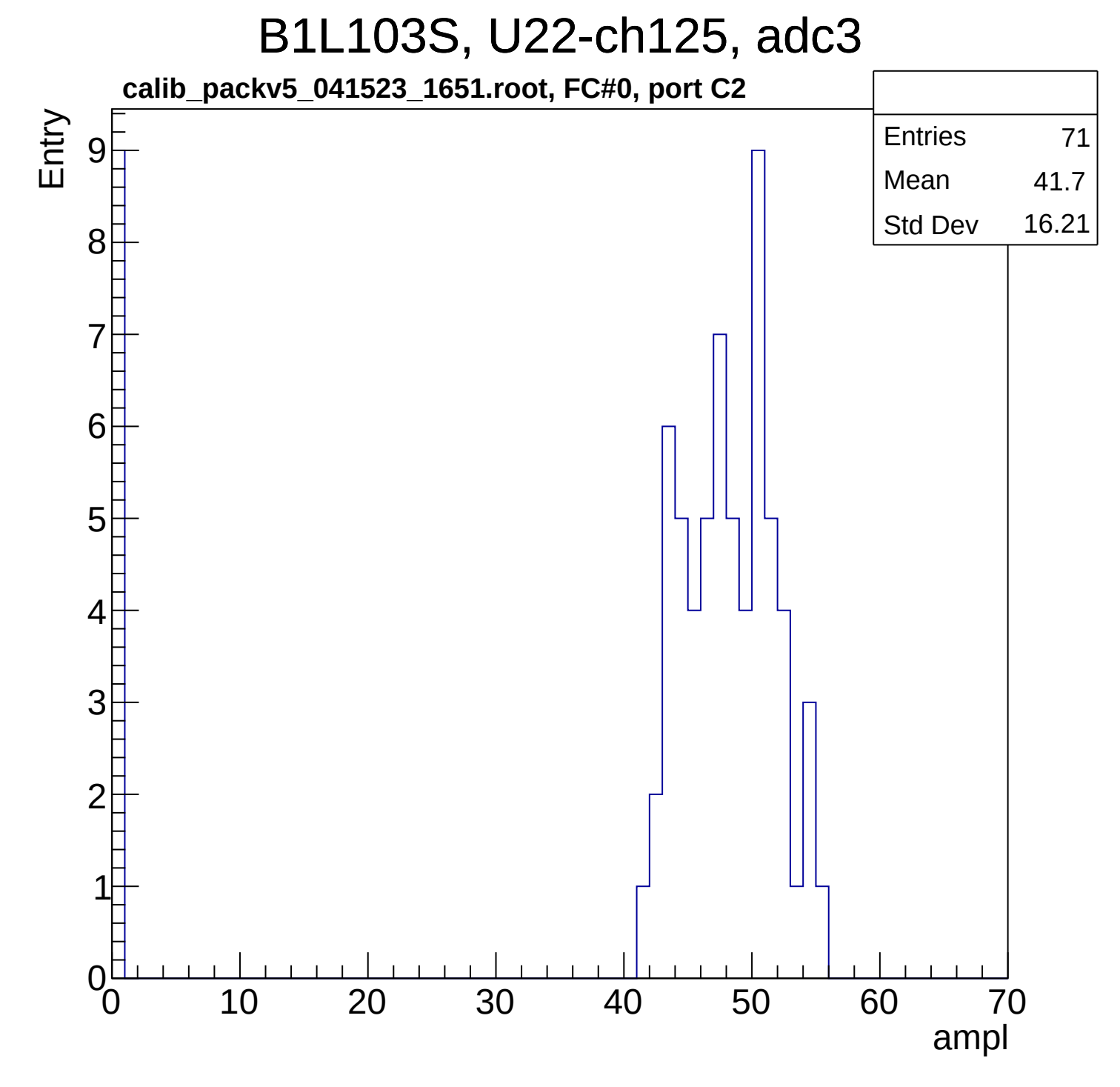
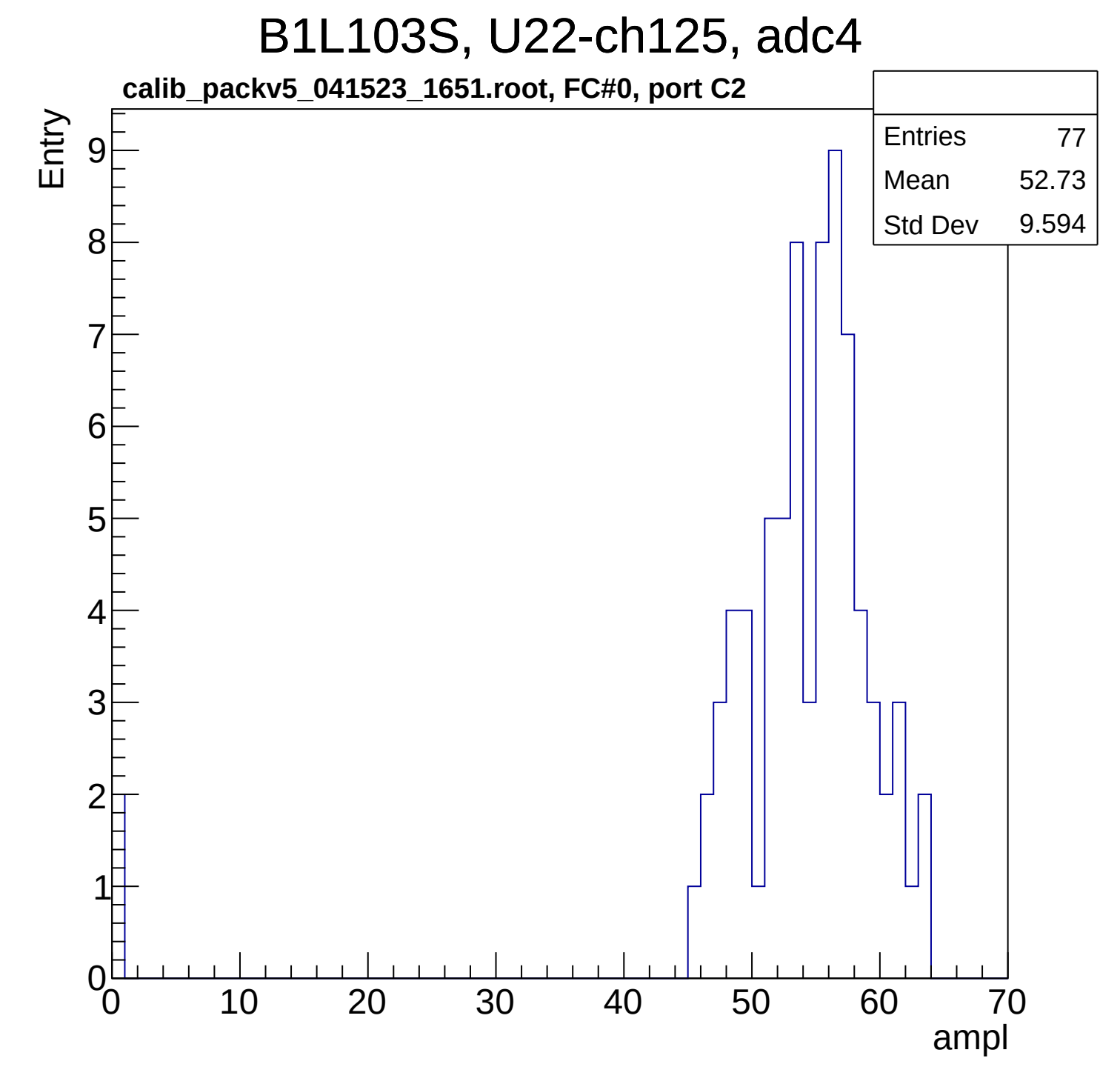
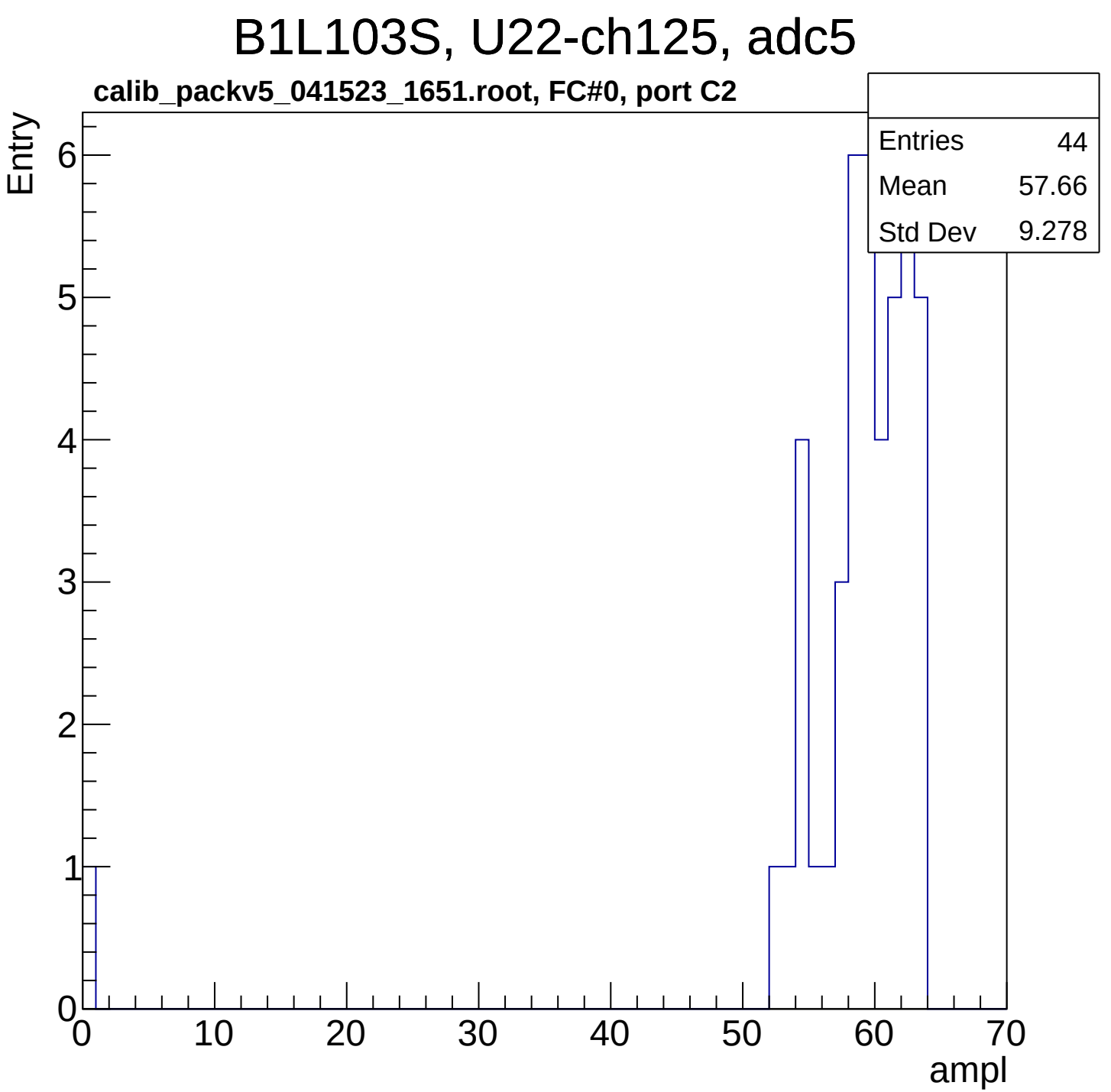
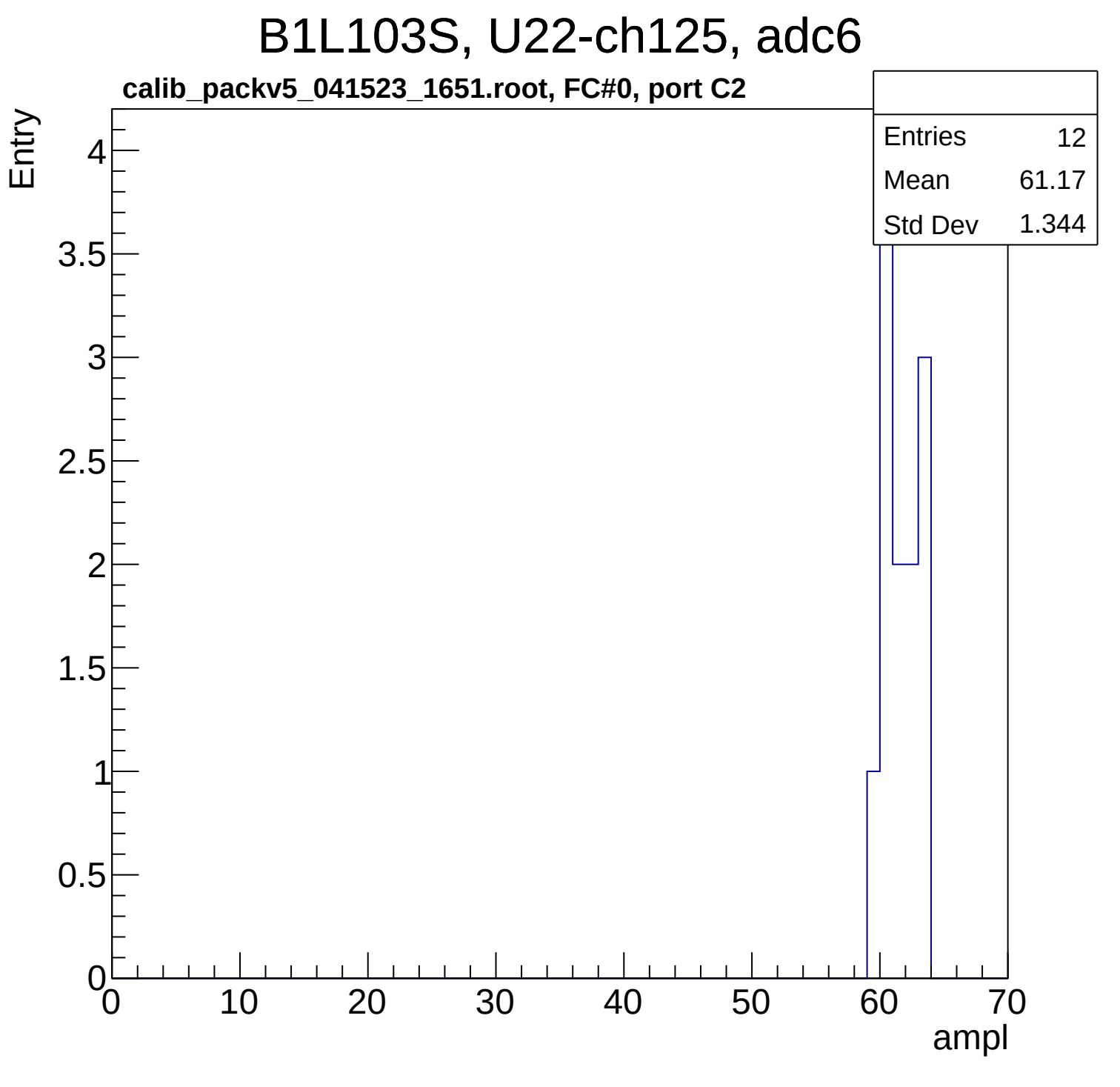
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

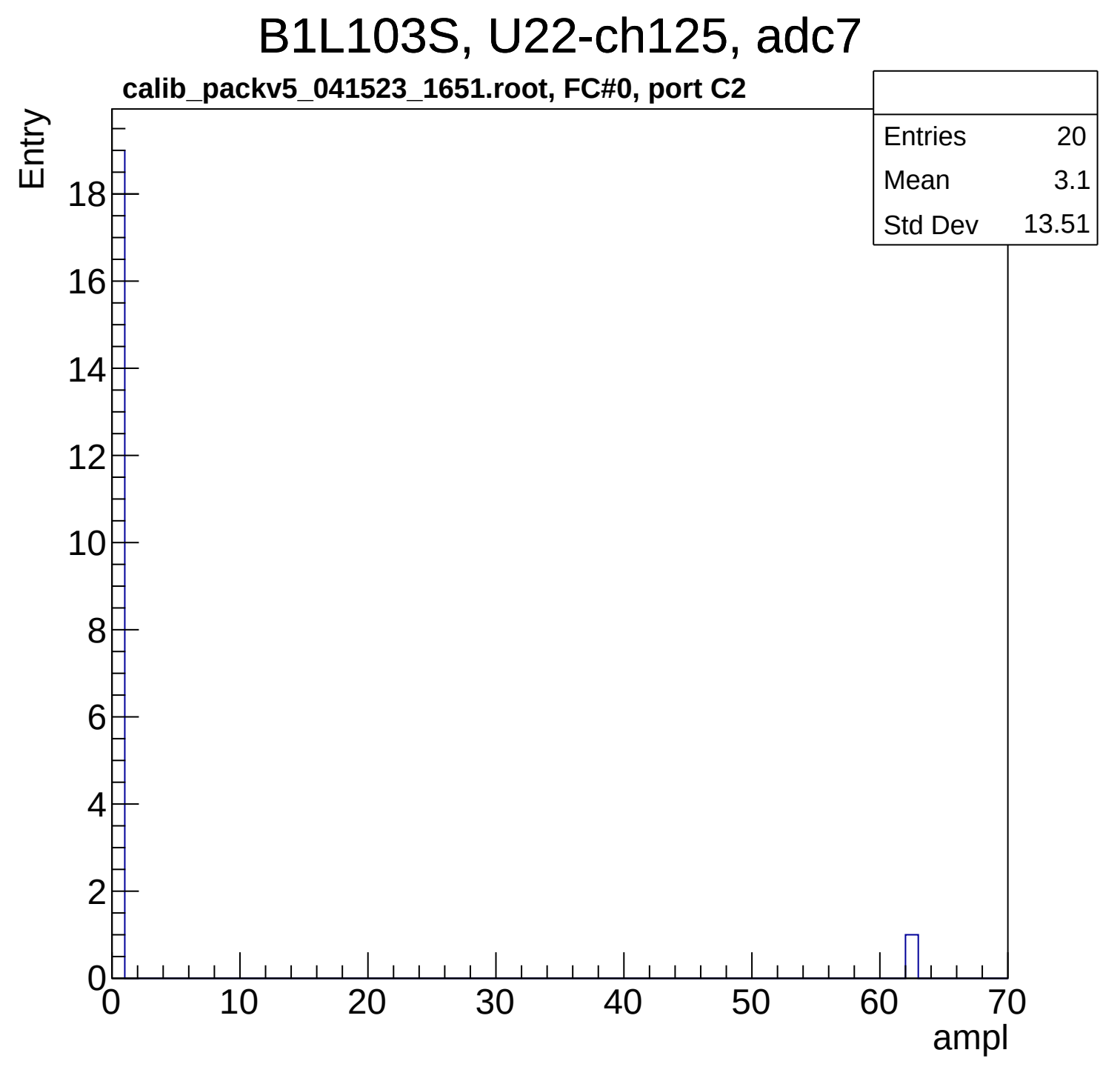

B1L103S, U22-ch125, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 38.48
Std Dev 10.13
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

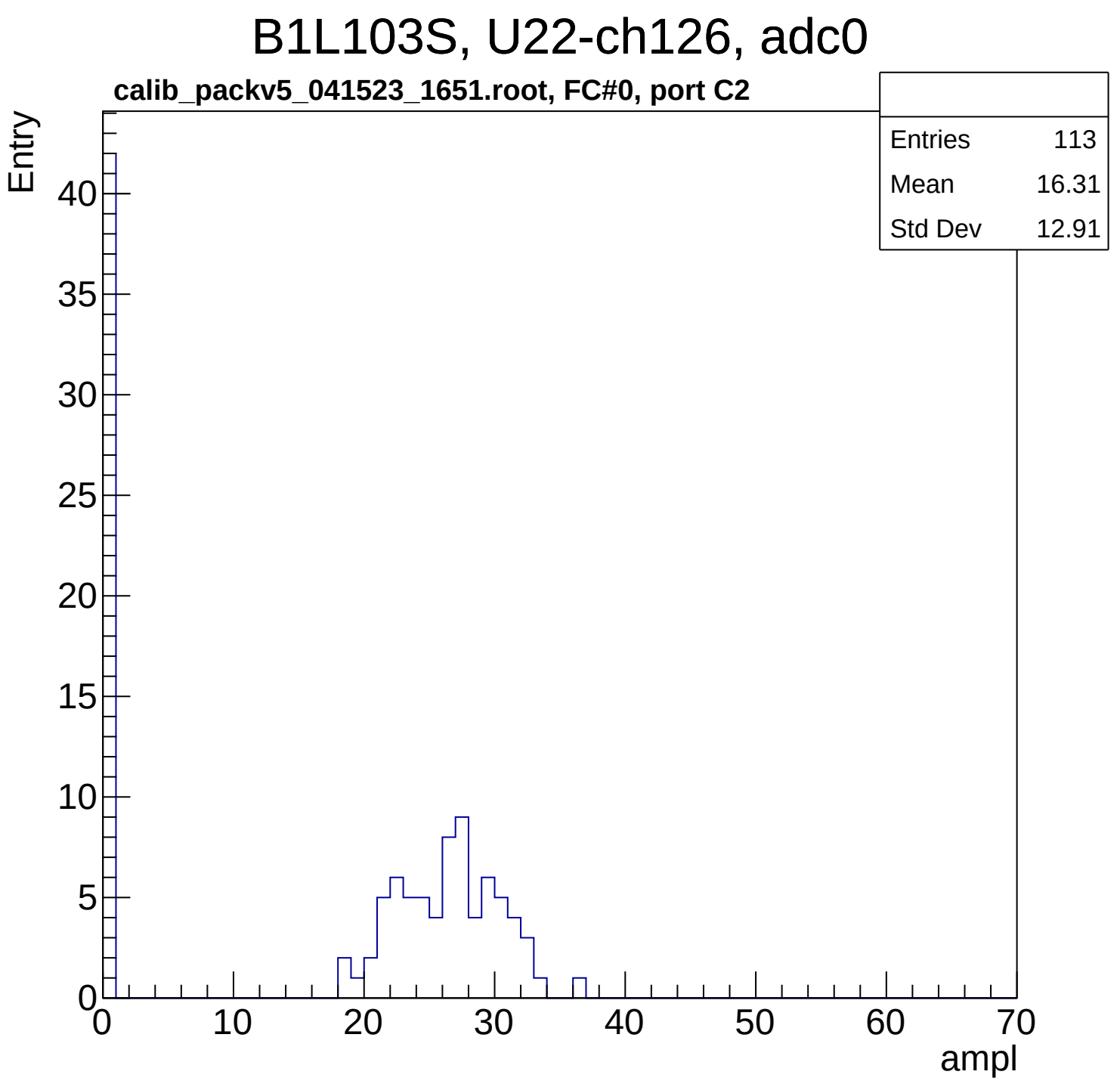

B1L103S, U22-ch125, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 41.7
Std Dev 16.21
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

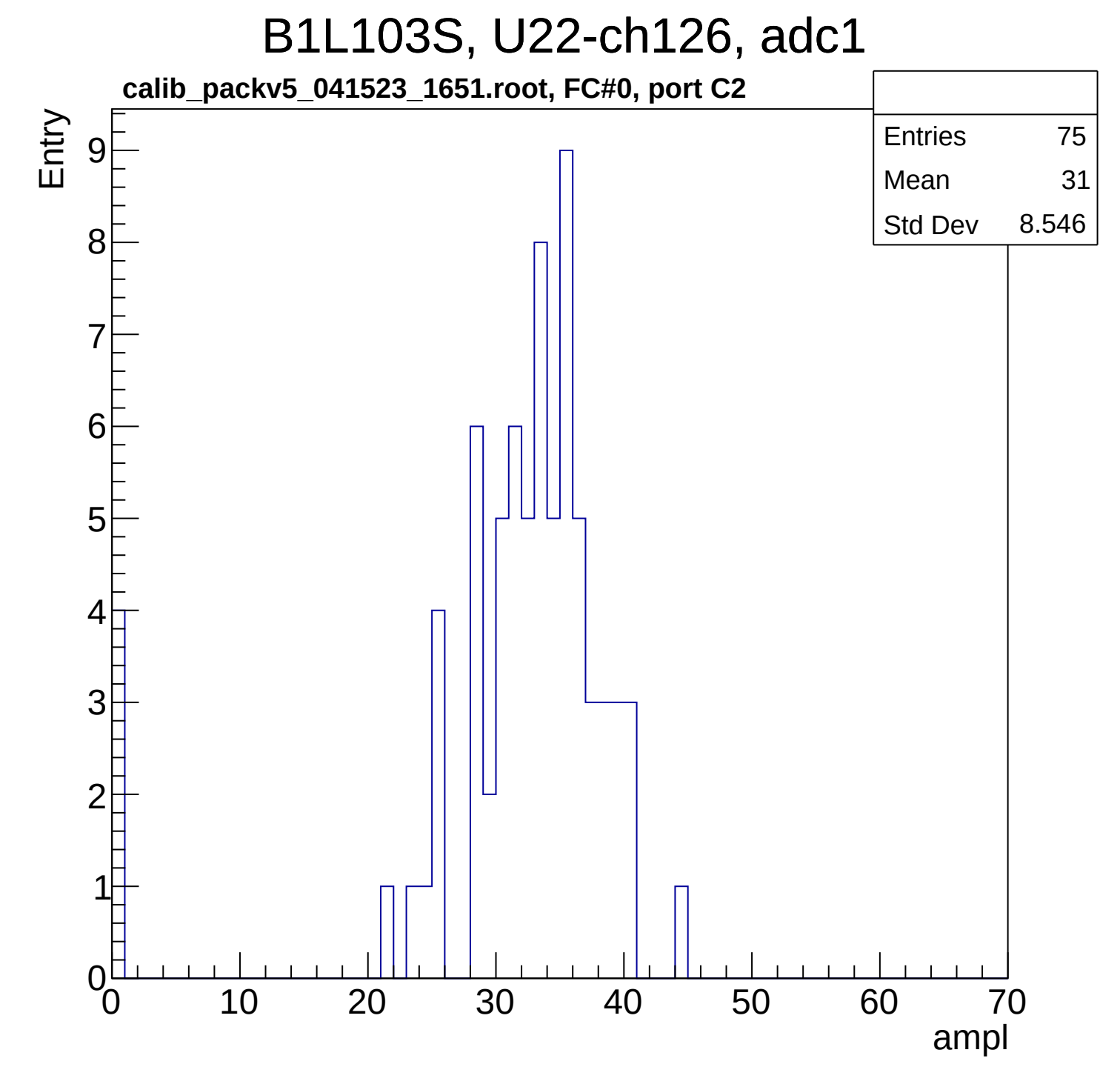

B1L103S, U22-ch125, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 52.73
Std Dev 9.594
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch125, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 57.66
Std Dev 9.278
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U22-ch125, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.17
Std Dev 1.344
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U22-ch125, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch126, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 113
Mean 16.31
Std Dev 12.91
Entry
0
5
10
15
20
25
30
35
40
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch126, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 31
Std Dev 8.546
Entry
ampl
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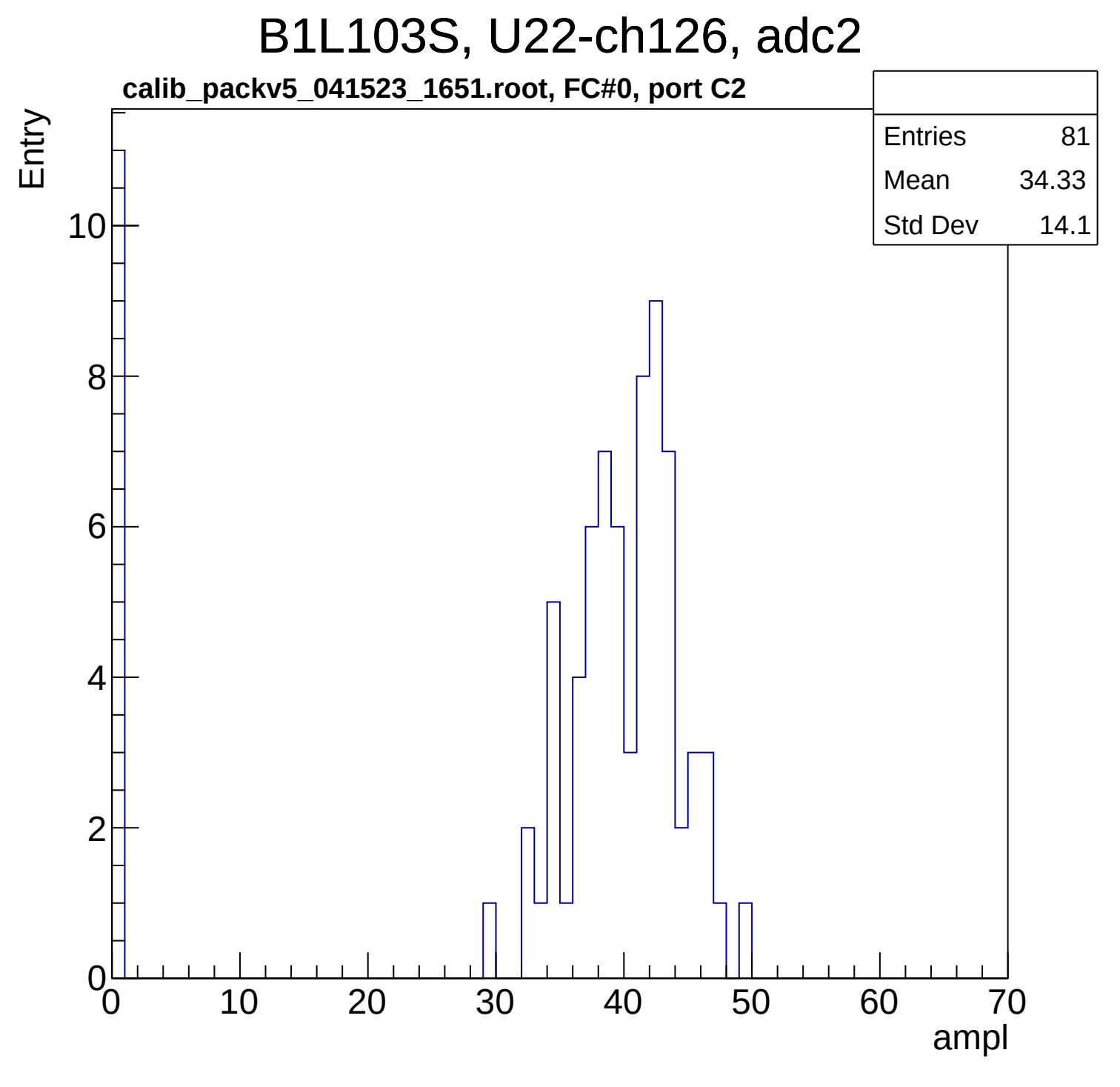
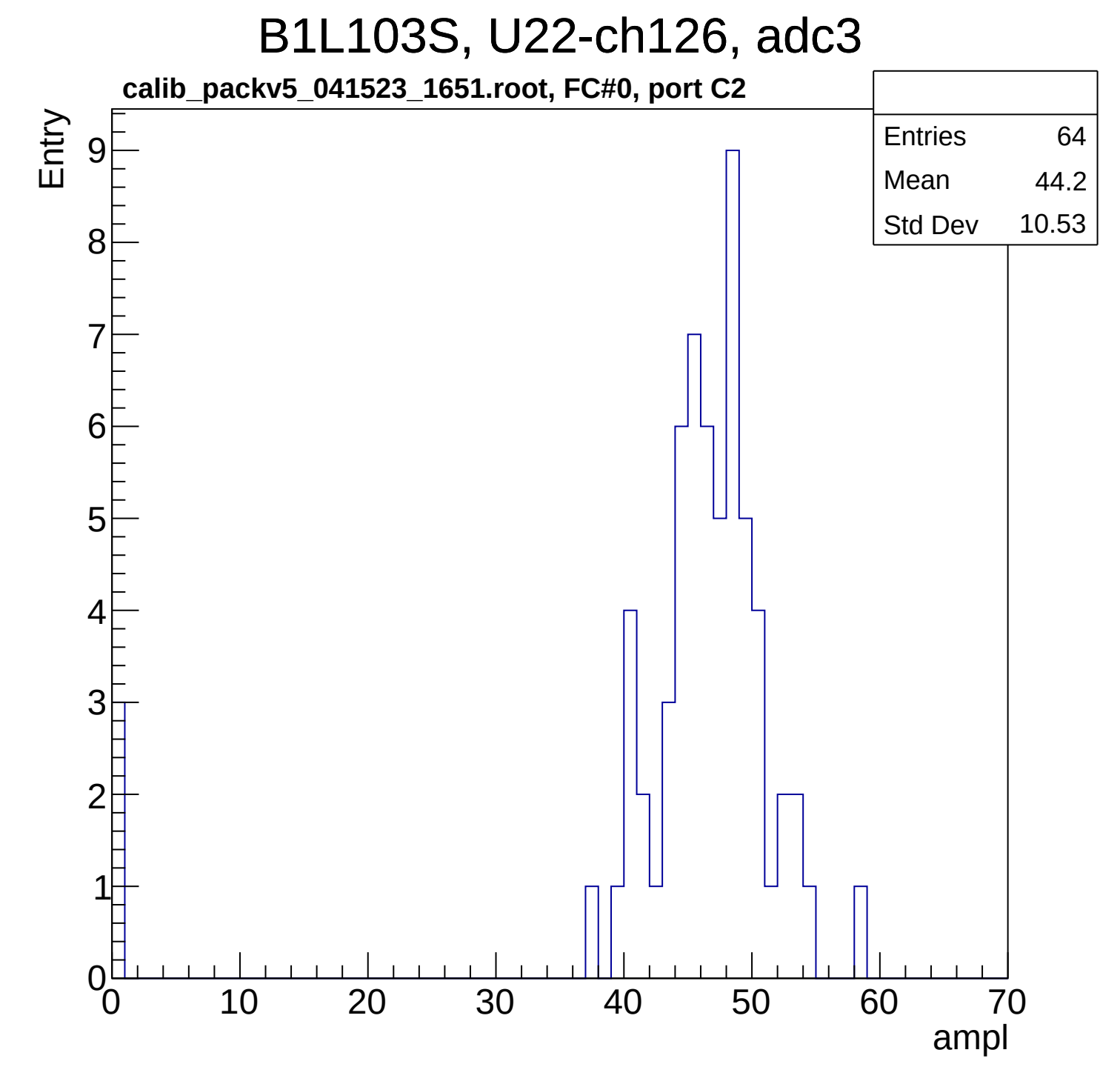
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch126, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 34.33
Std Dev 14.1
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch126, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 44.2
Std Dev 10.53
Entry
ampl
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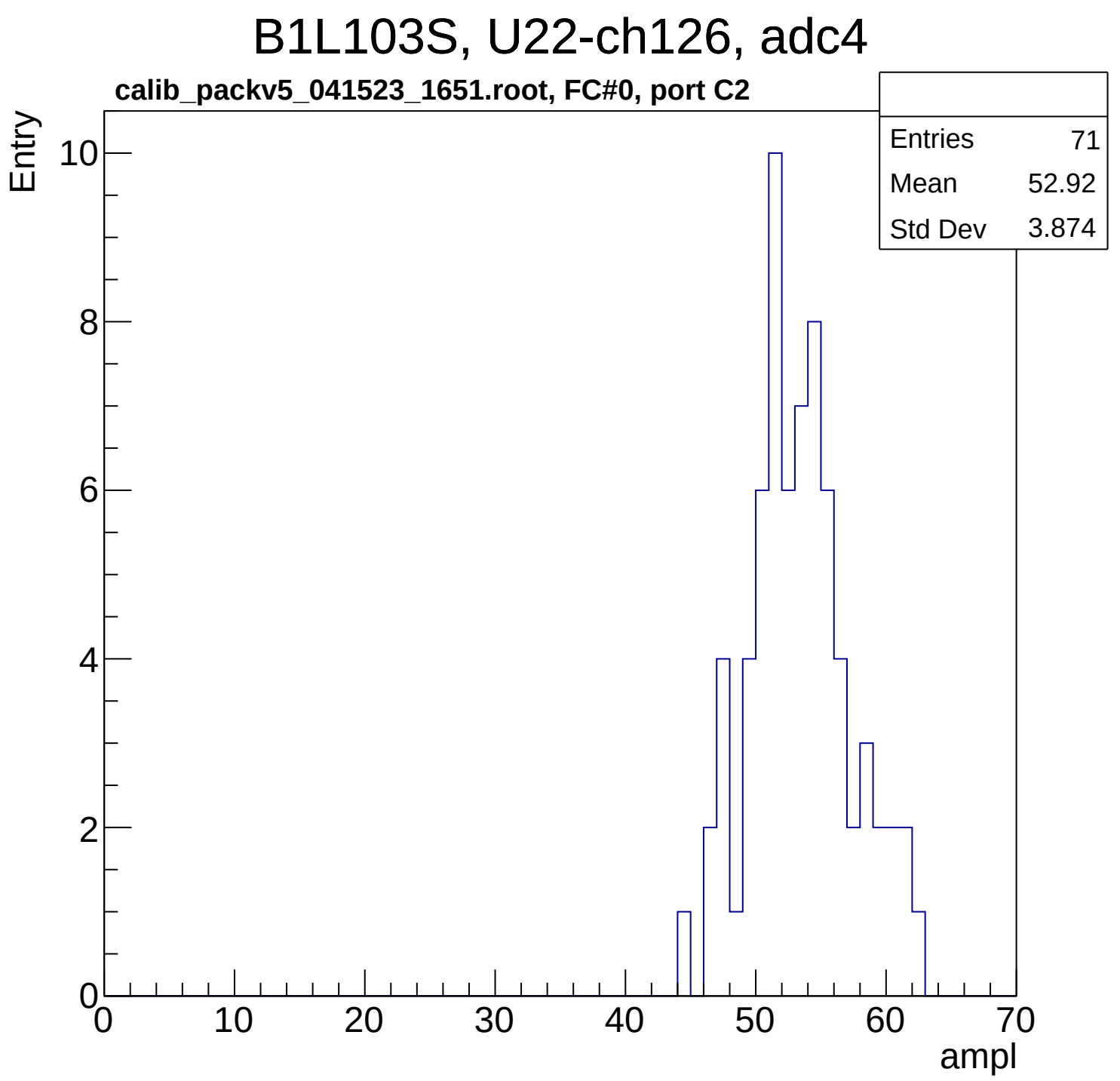
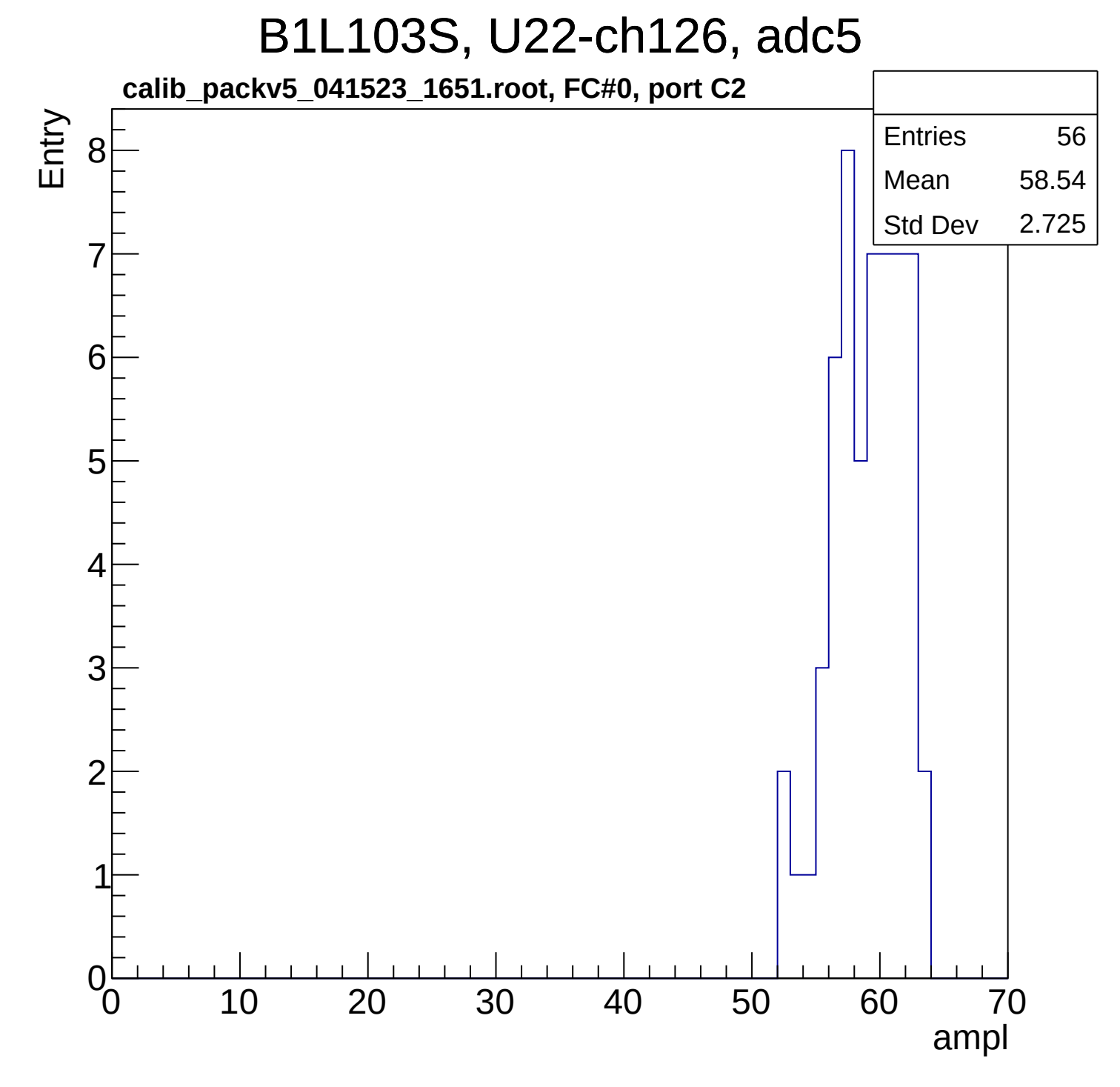
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch126, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 52.92
Std Dev 3.874
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch126, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 58.54
Std Dev 2.725
Entry
ampl
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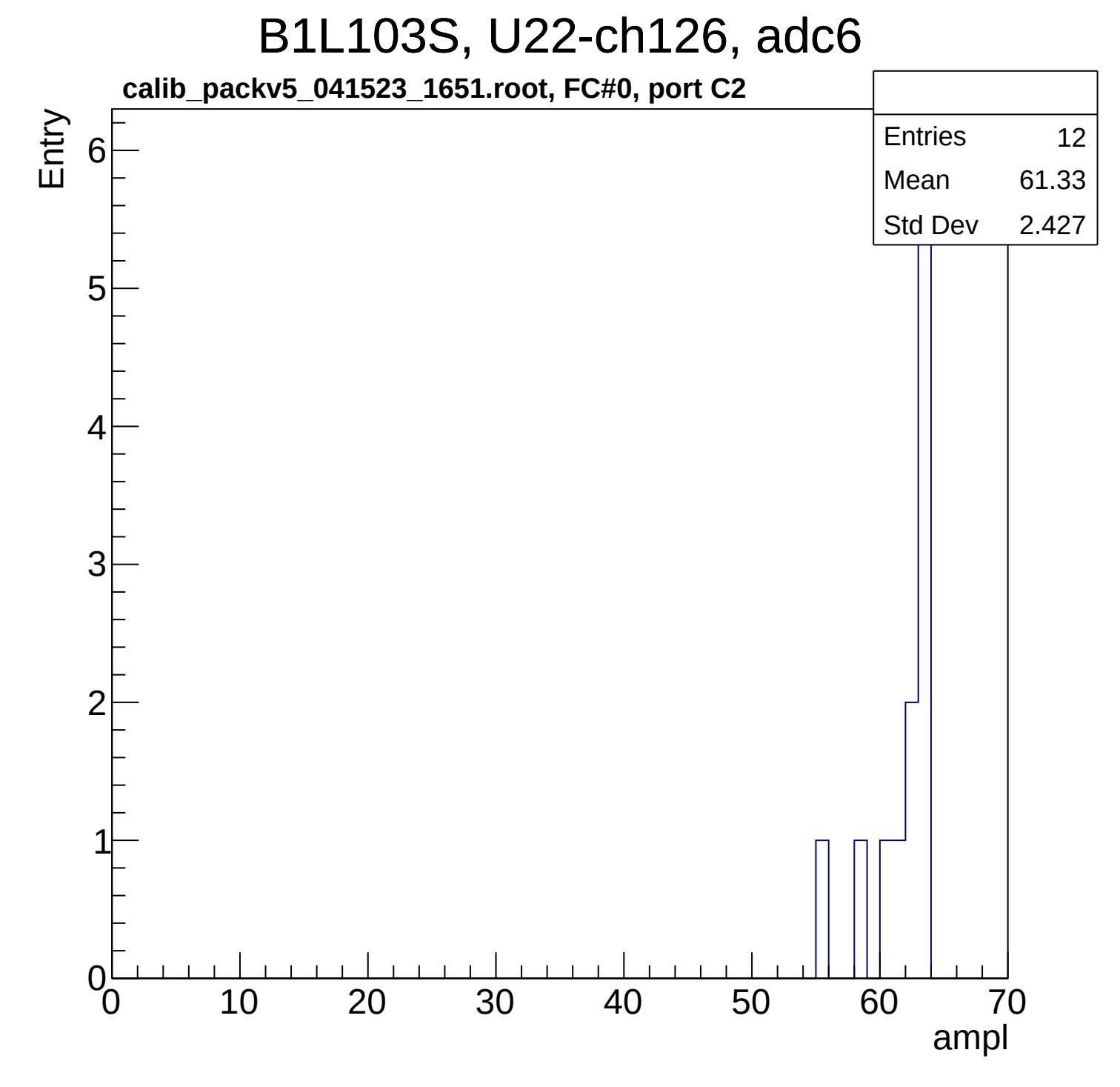
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch126, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.33
Std Dev 2.427
Entry
0
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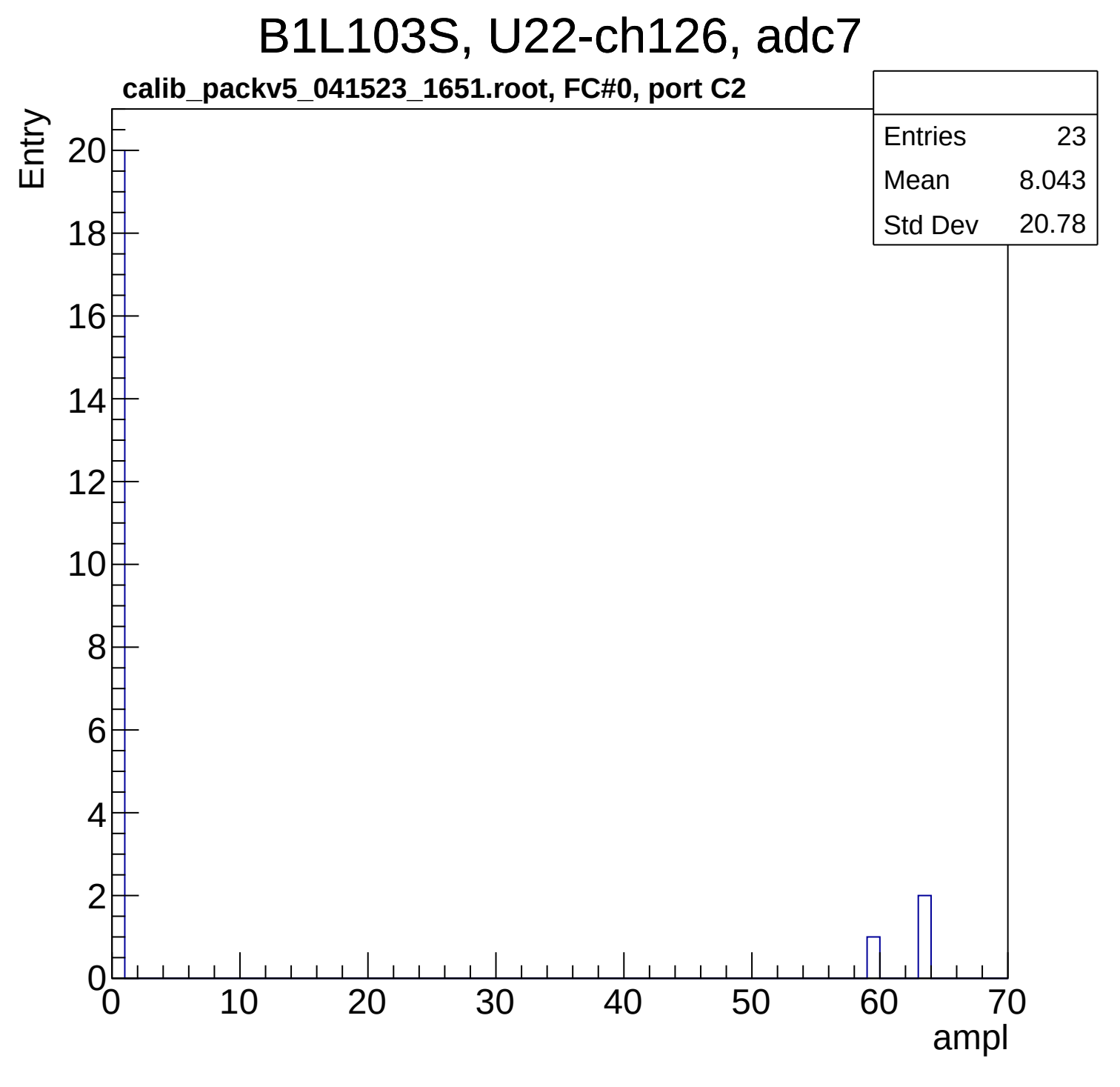
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch126, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 8.043
Std Dev 20.78
Entry
ampl
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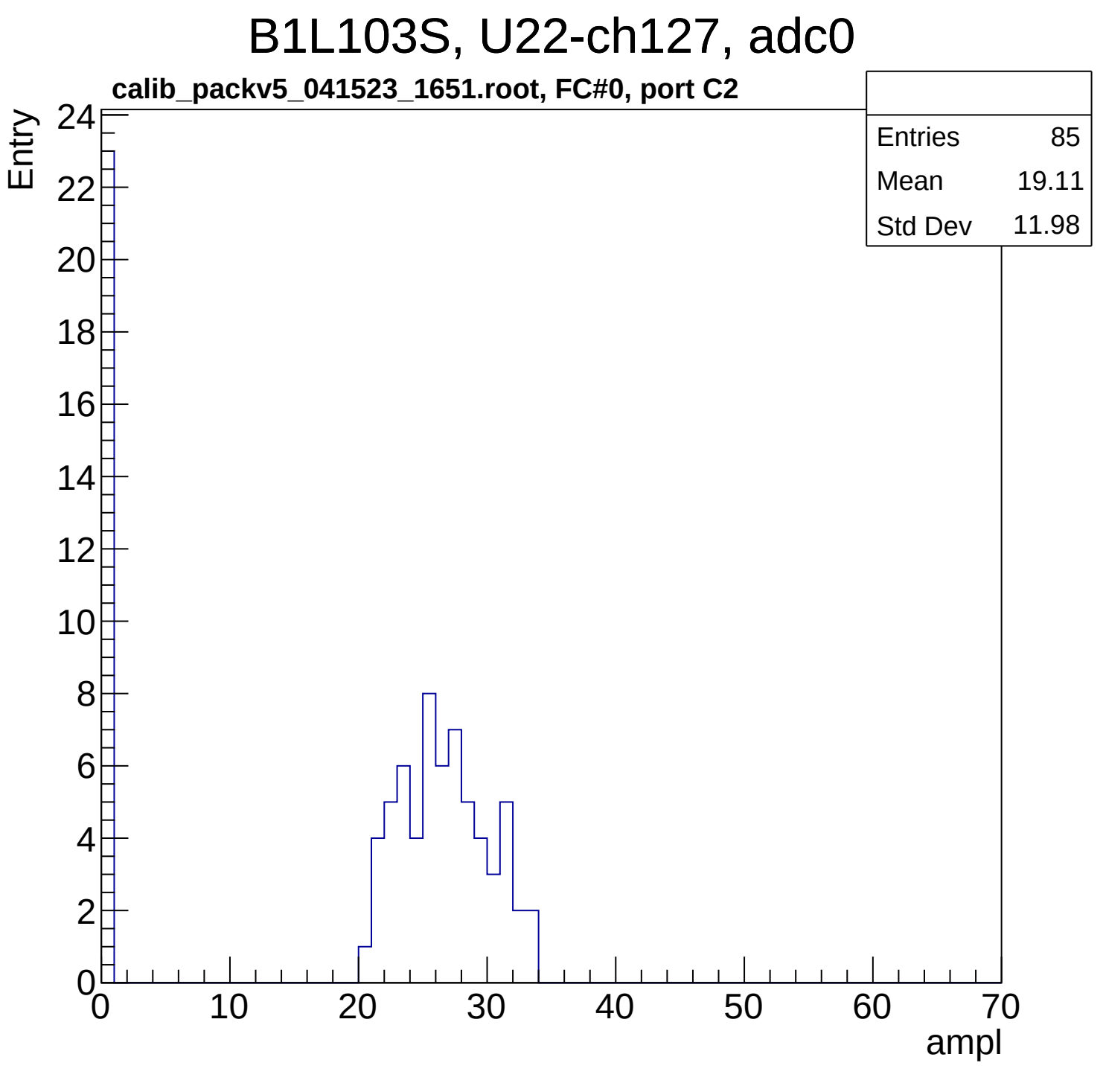
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70


B1L103S, U22-ch127, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 19.11
Std Dev 11.98
Entry
ampl
0
2
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10
12
14
16
18
20
22
24
0
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60
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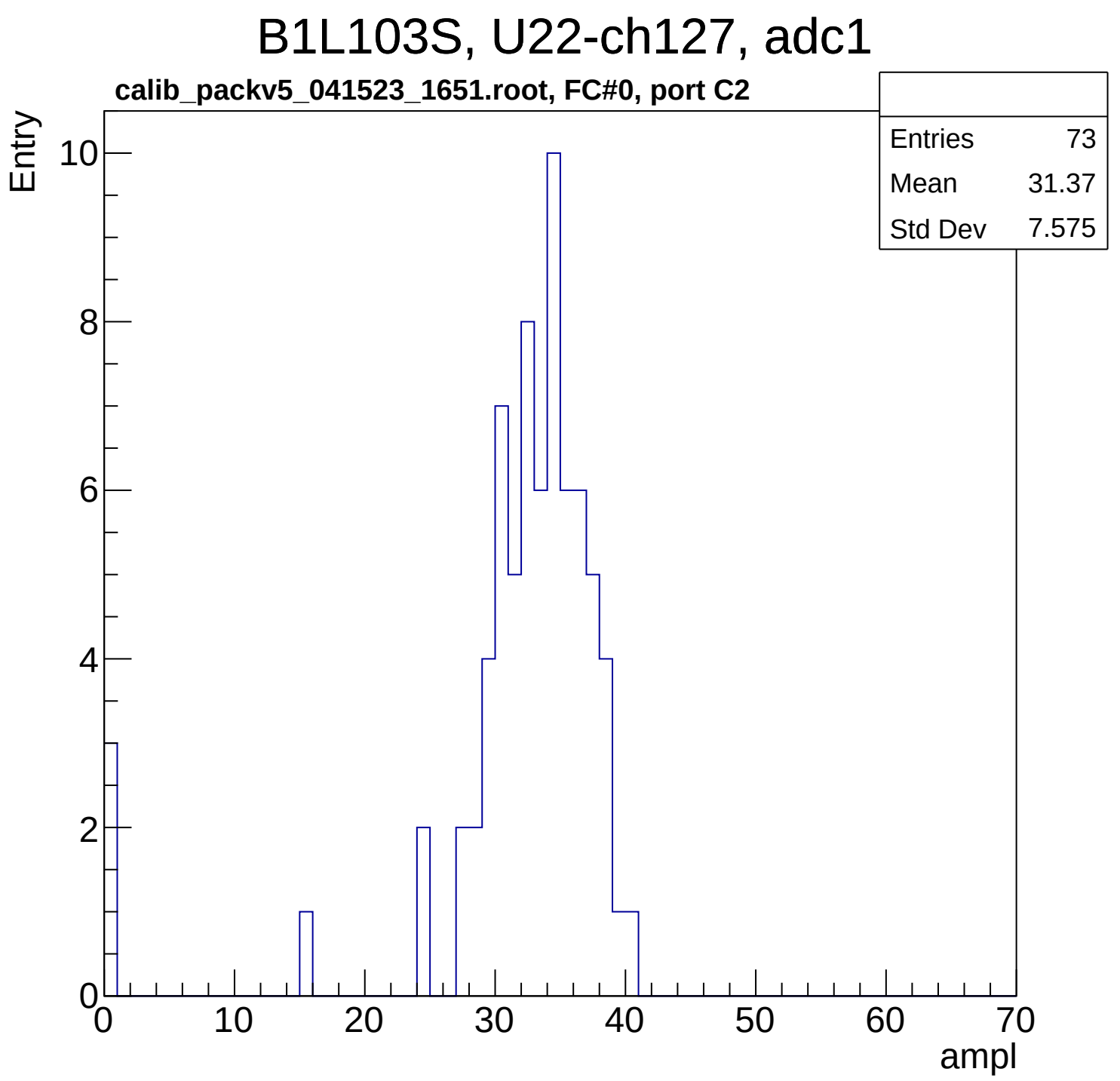
B1L103S, U22-ch127, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 31.37
Std Dev 7.575
Entry
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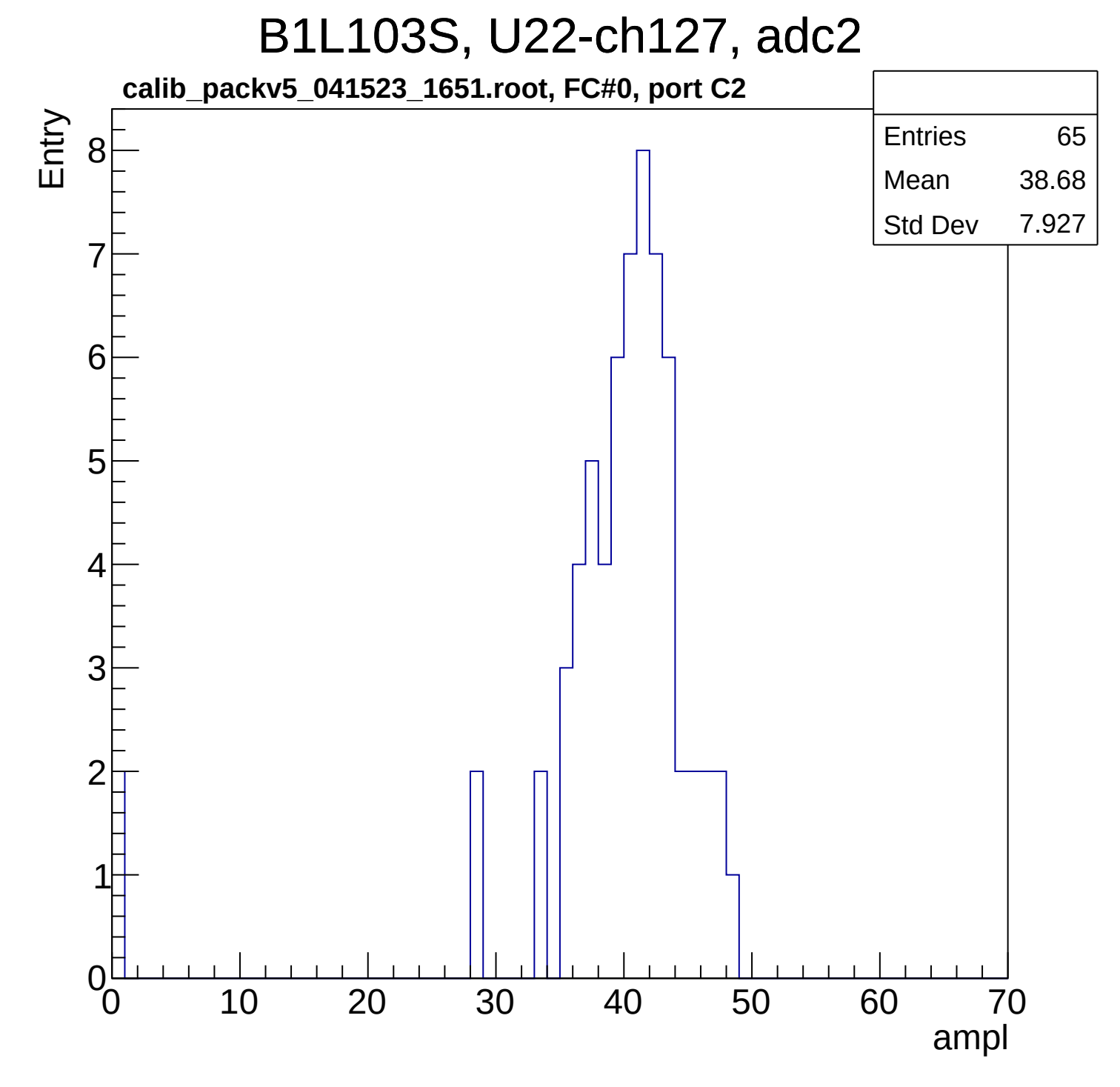
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U22-ch127, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 38.68
Std Dev 7.927
Entry
ampl
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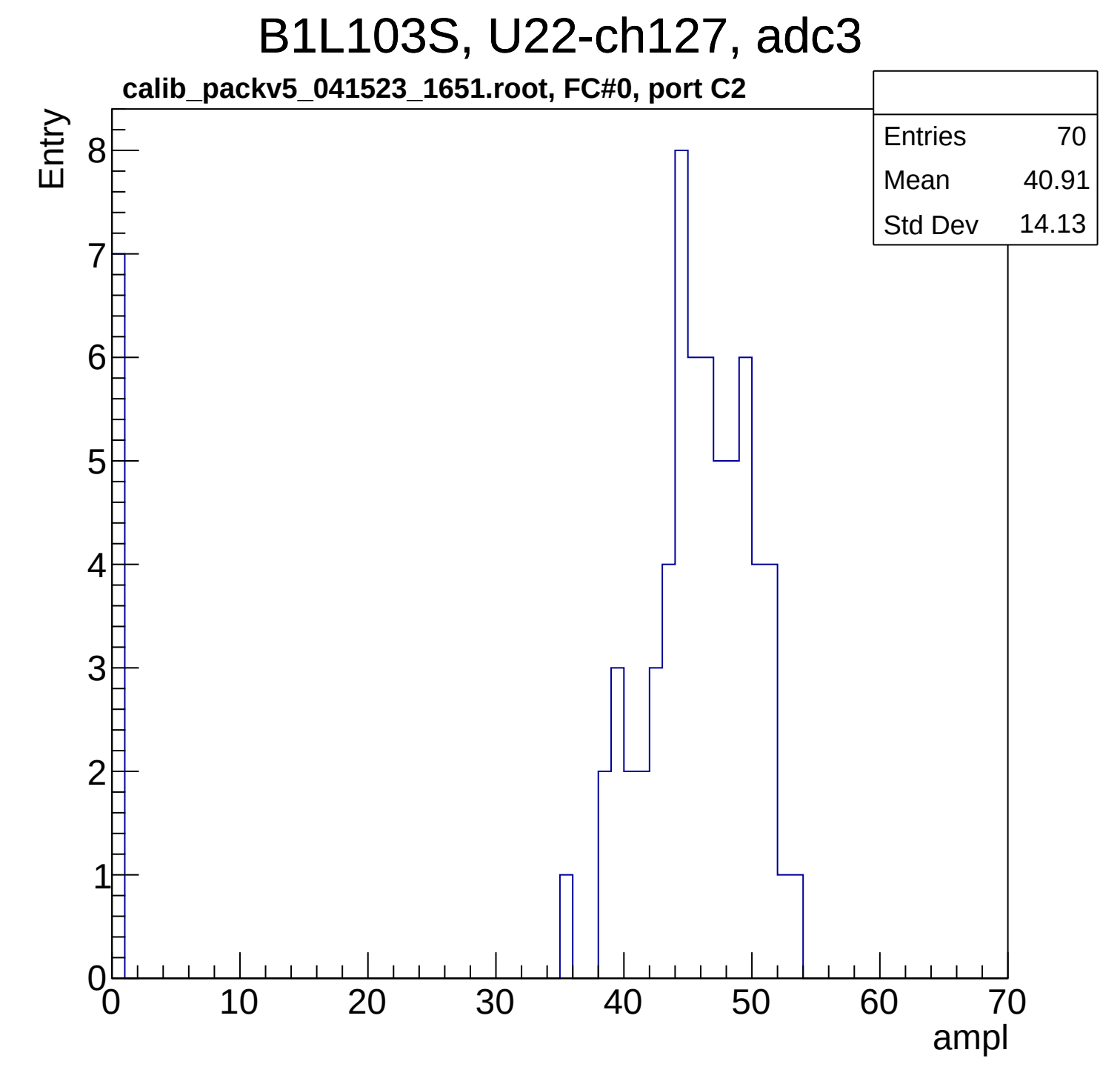
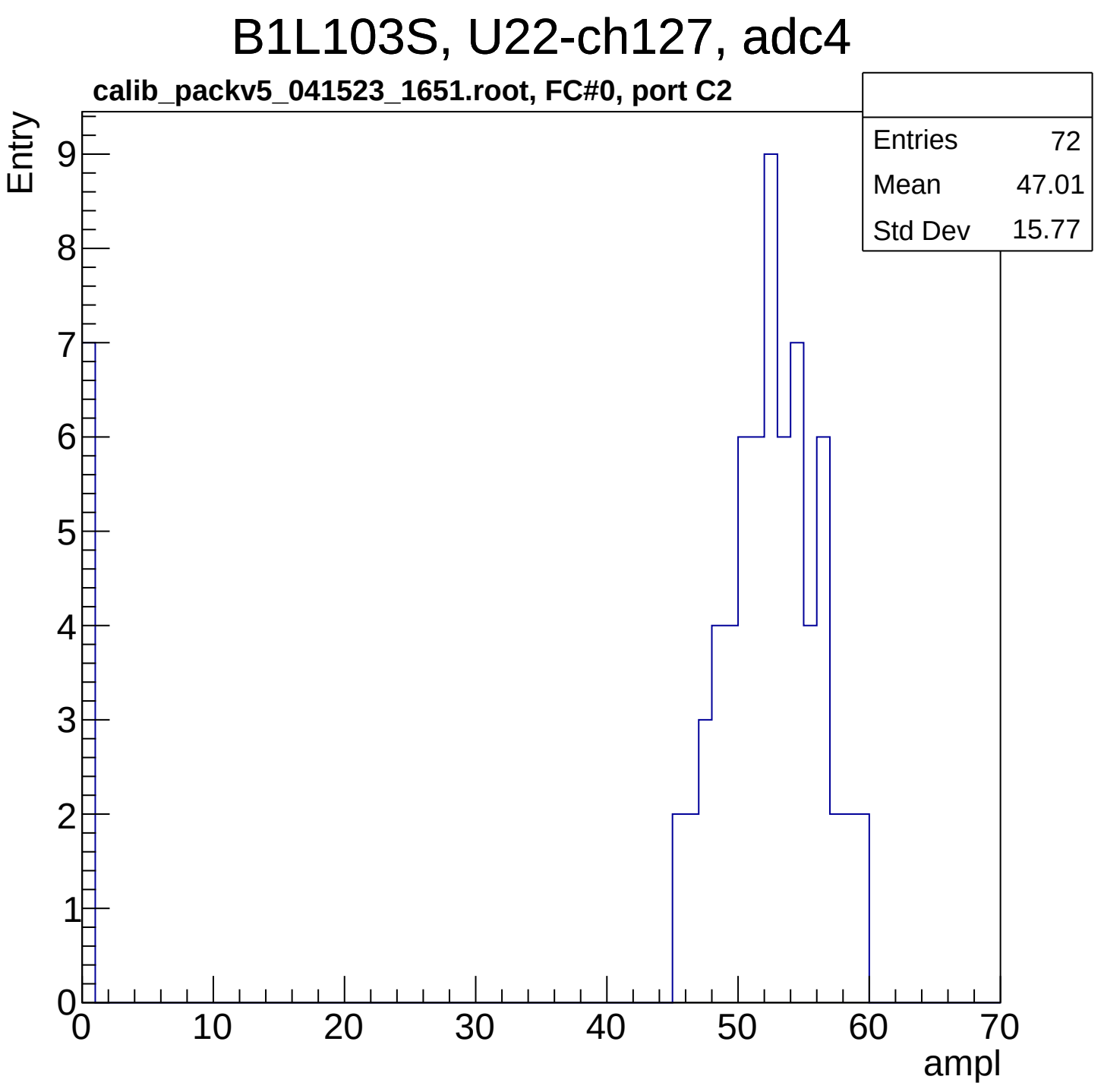
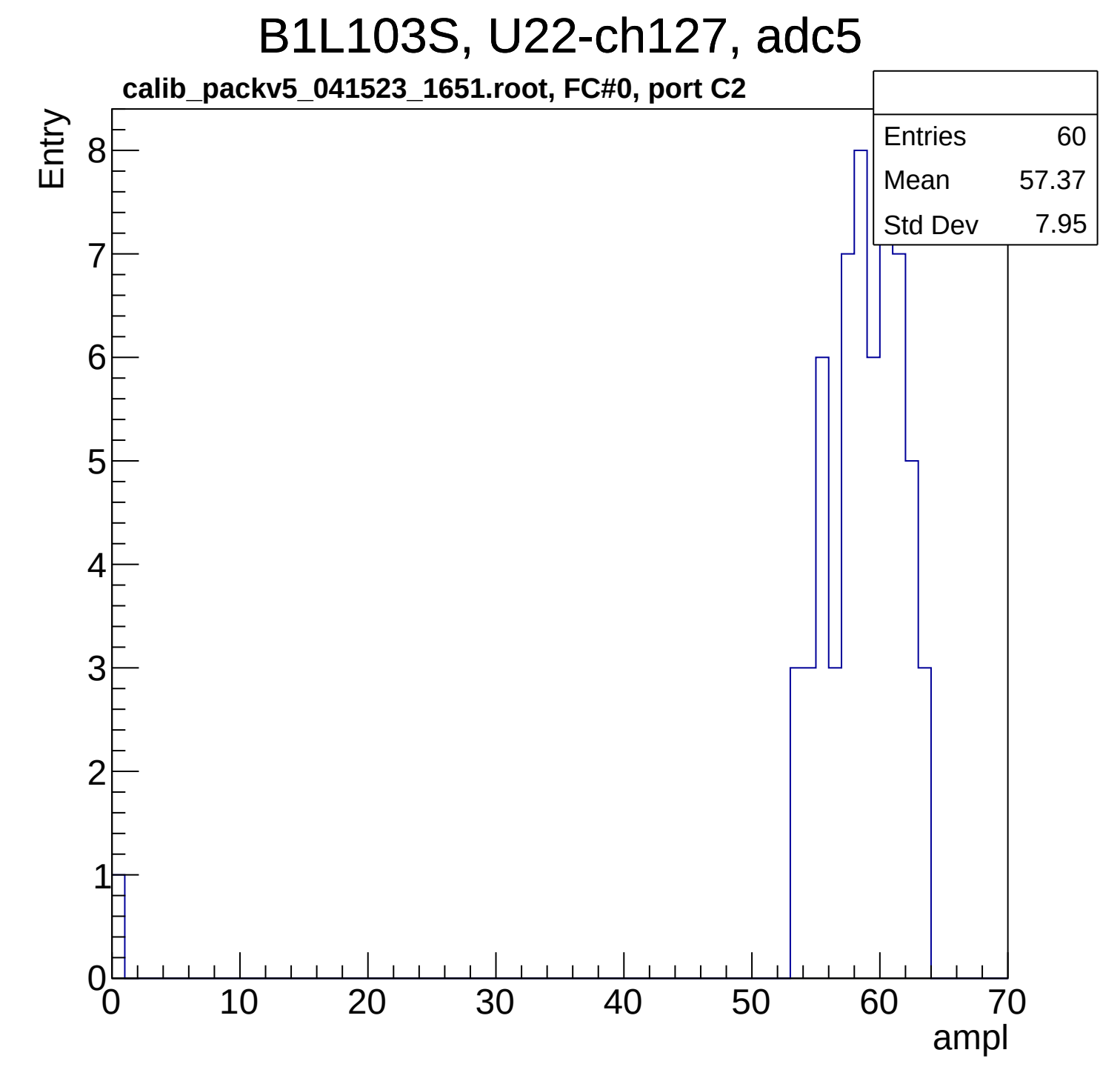
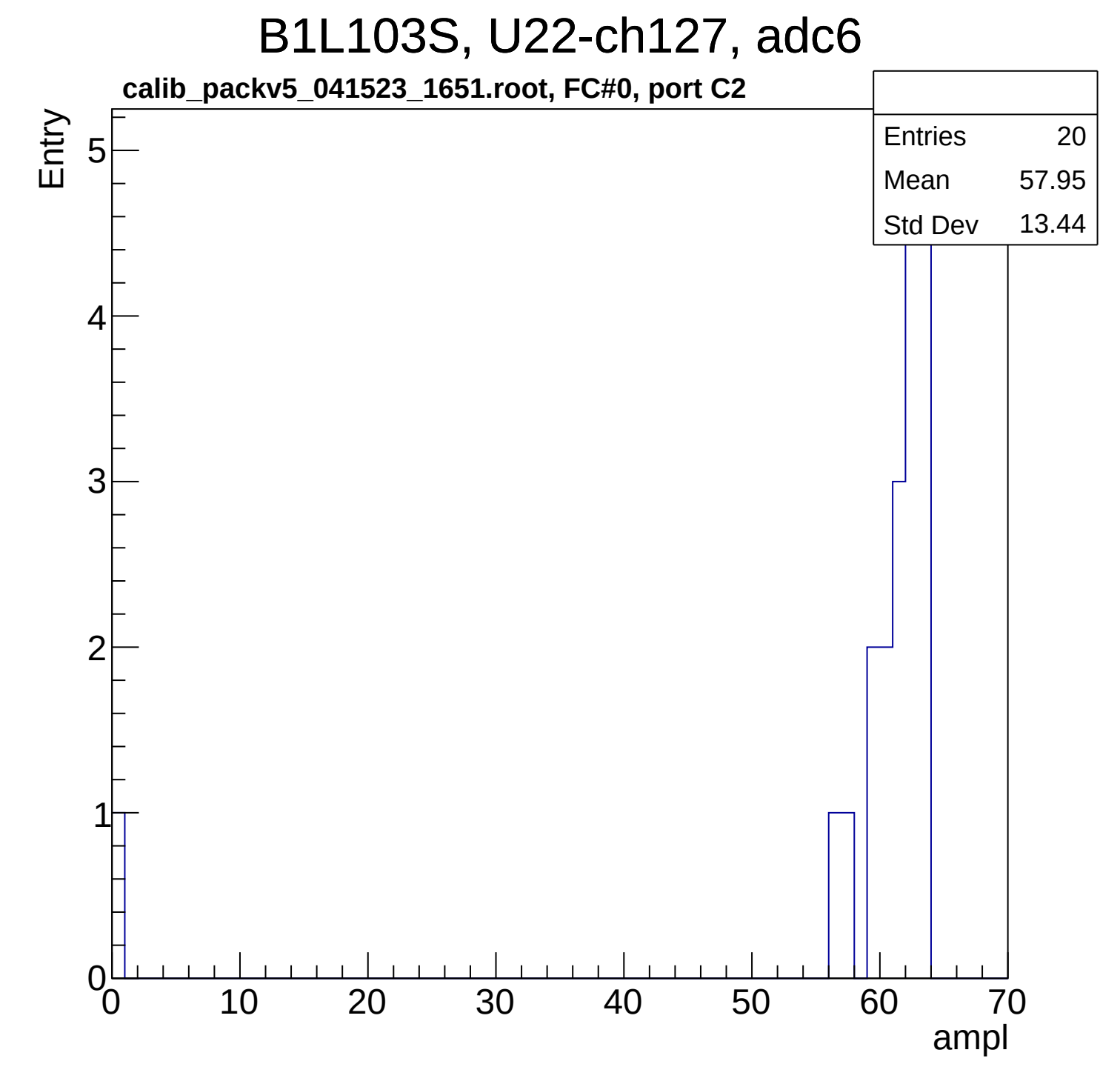
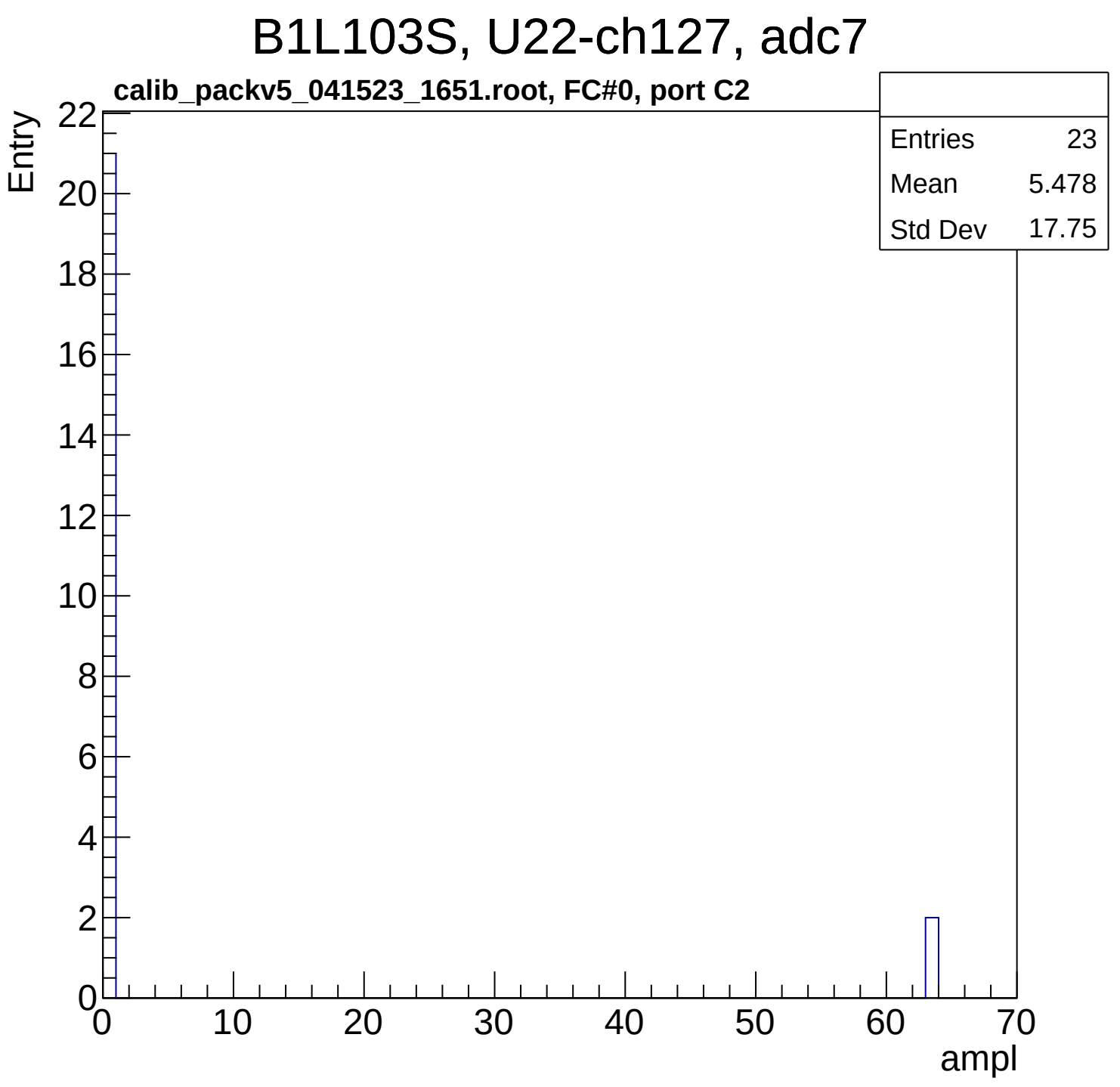
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

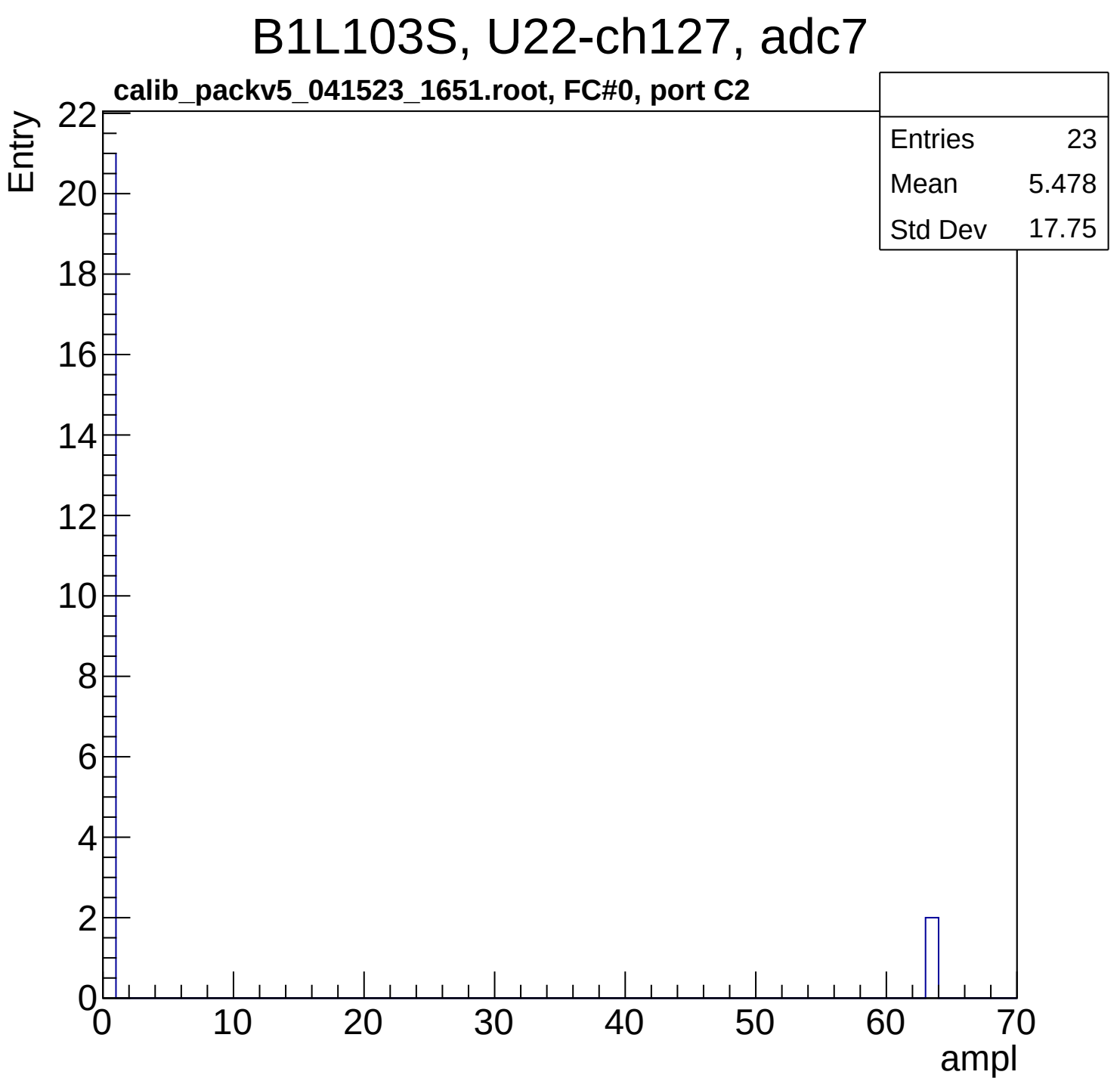

B1L103S, U22-ch127, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 40.91
Std Dev 14.13
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch127, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 47.01
Std Dev 15.77
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U22-ch127, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 57.37
Std Dev 7.95
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U22-ch127, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 57.95
Std Dev 13.44
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U22-ch127, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 5.478
Std Dev 17.75
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70


B1L103S, U22-ch127, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 5.478
Std Dev 17.75
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70