



# B1L100S, U16-ch0

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	390
Mean	43.56
Std Dev	12.28

Turn on : 25.2936

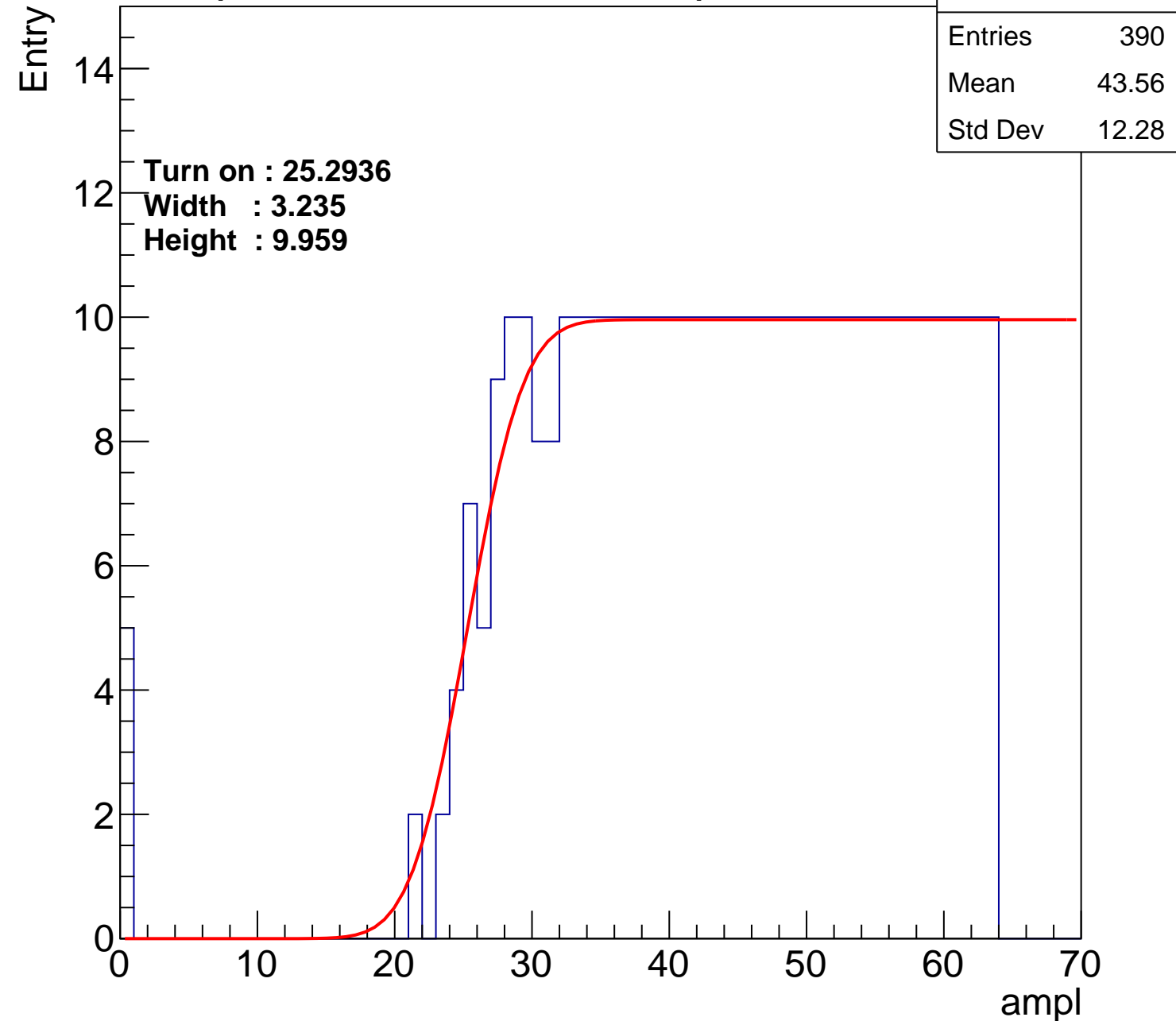
Width : 3.235

Height : 9.959

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch1

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	371
Mean	44.77
Std Dev	11.1

Turn on : 27.1052

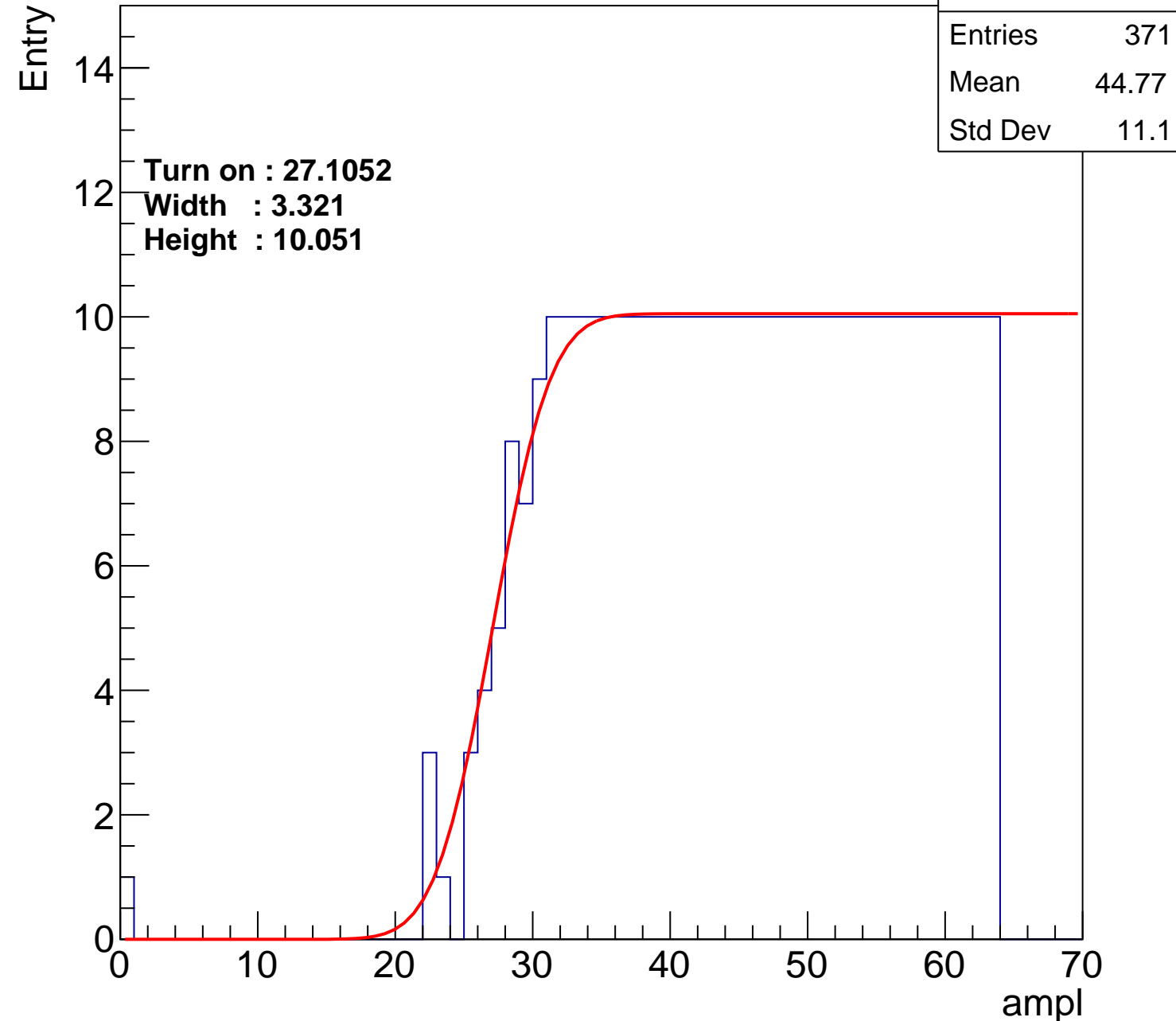
Width : 3.321

Height : 10.051

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch2

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	389
Mean	43.6
Std Dev	12.28

Turn on : 25.3009

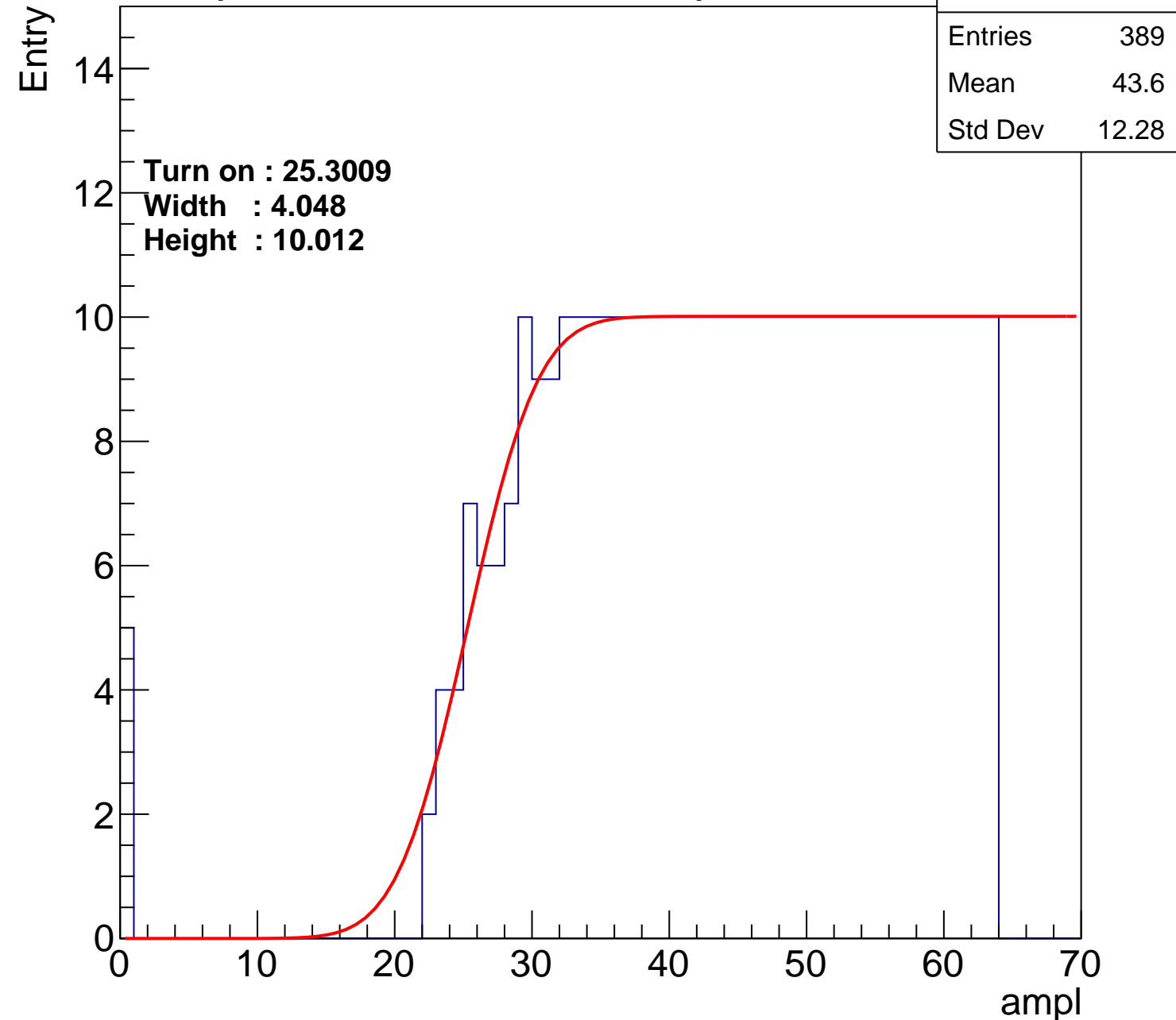
Width : 4.048

Height : 10.012

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	384
Mean	43.88
Std Dev	12.11

Turn on : 26.4118

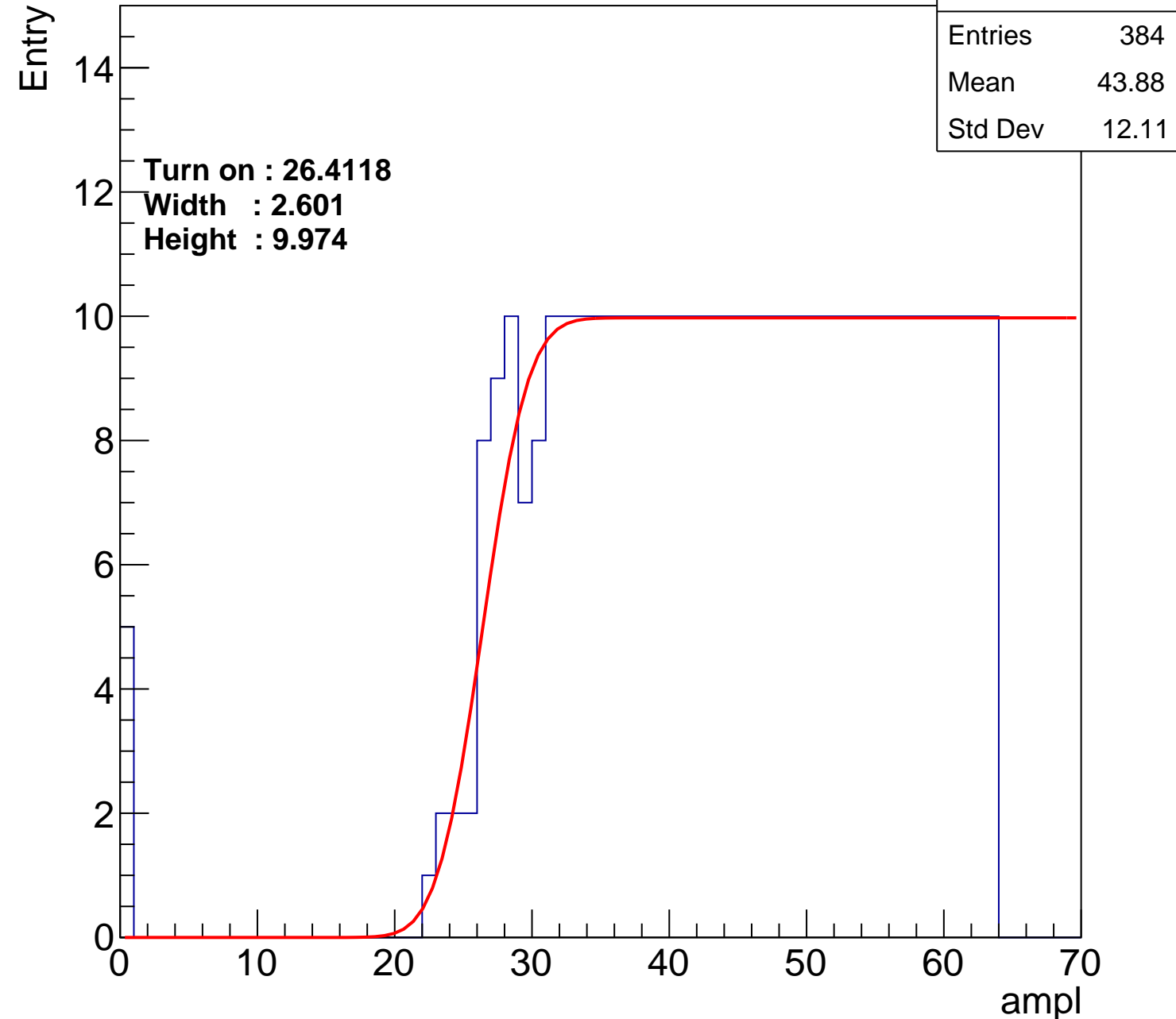
Width : 2.601

Height : 9.974

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	394
Mean	43.54
Std Dev	12

Turn on : 24.7163

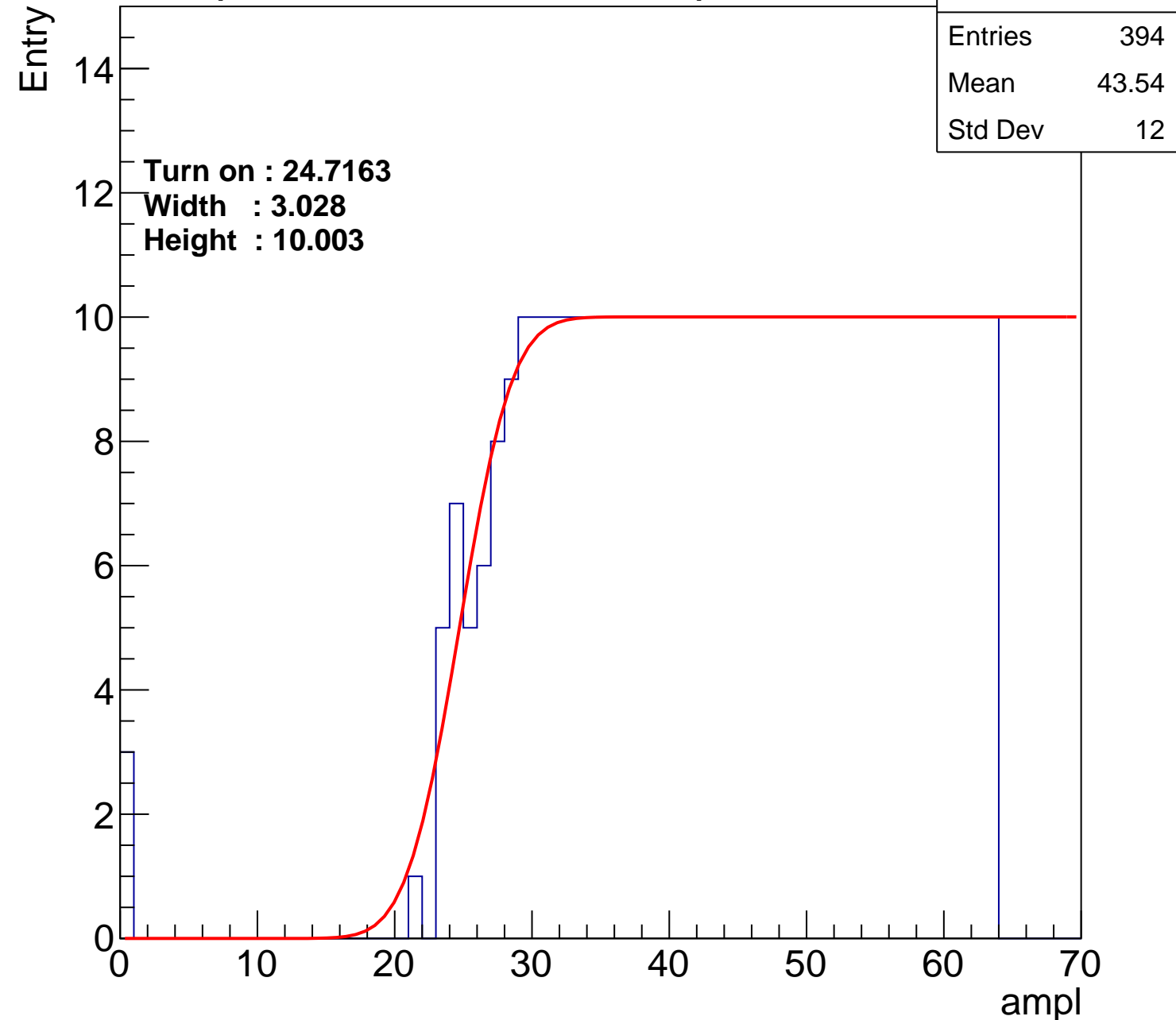
Width : 3.028

Height : 10.003

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	389
Mean	43.85
Std Dev	11.69

Turn on : 25.6098

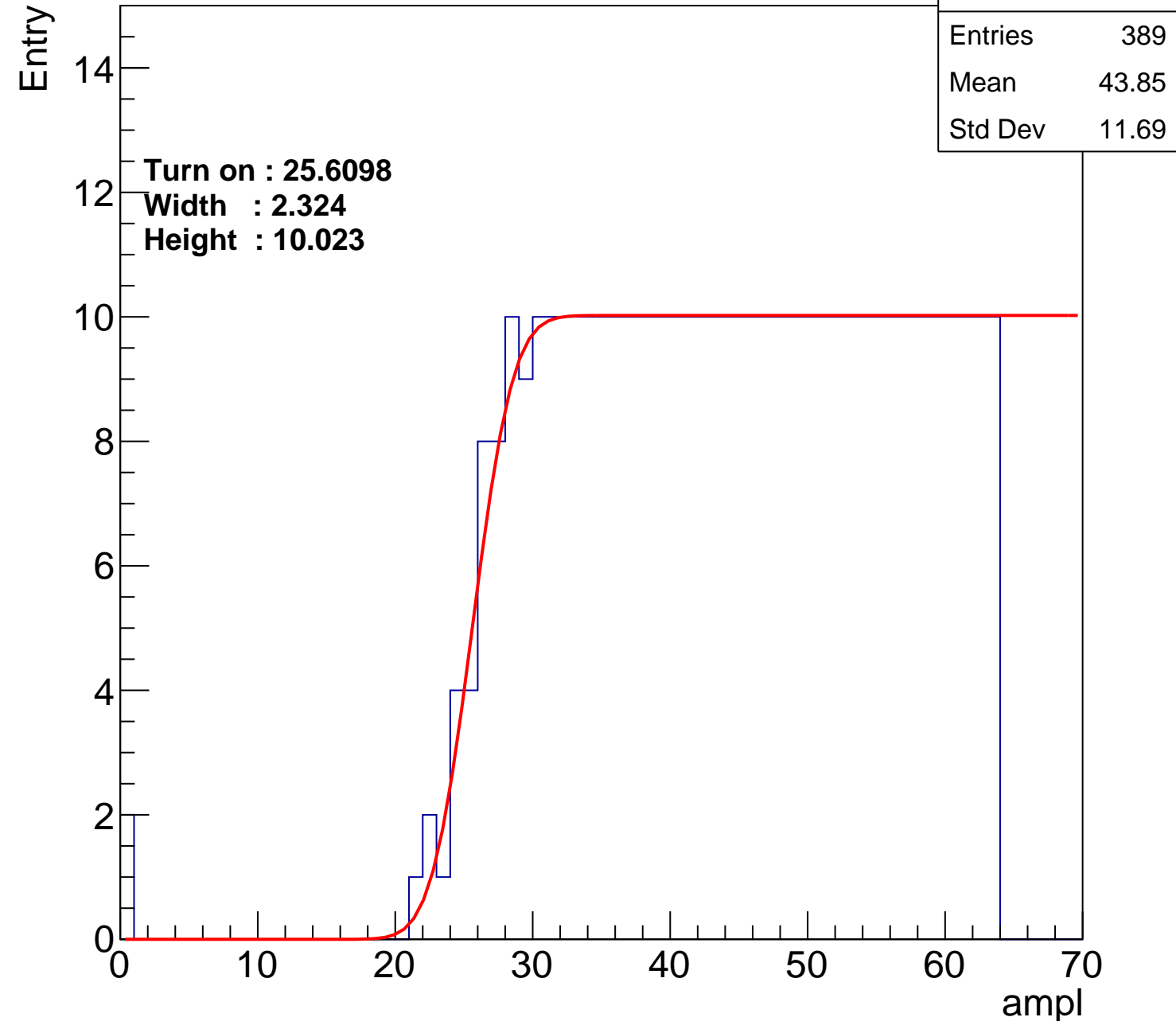
Width : 2.324

Height : 10.023

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	380
Mean	44.16
Std Dev	11.74

**Turn on : 25.8785**

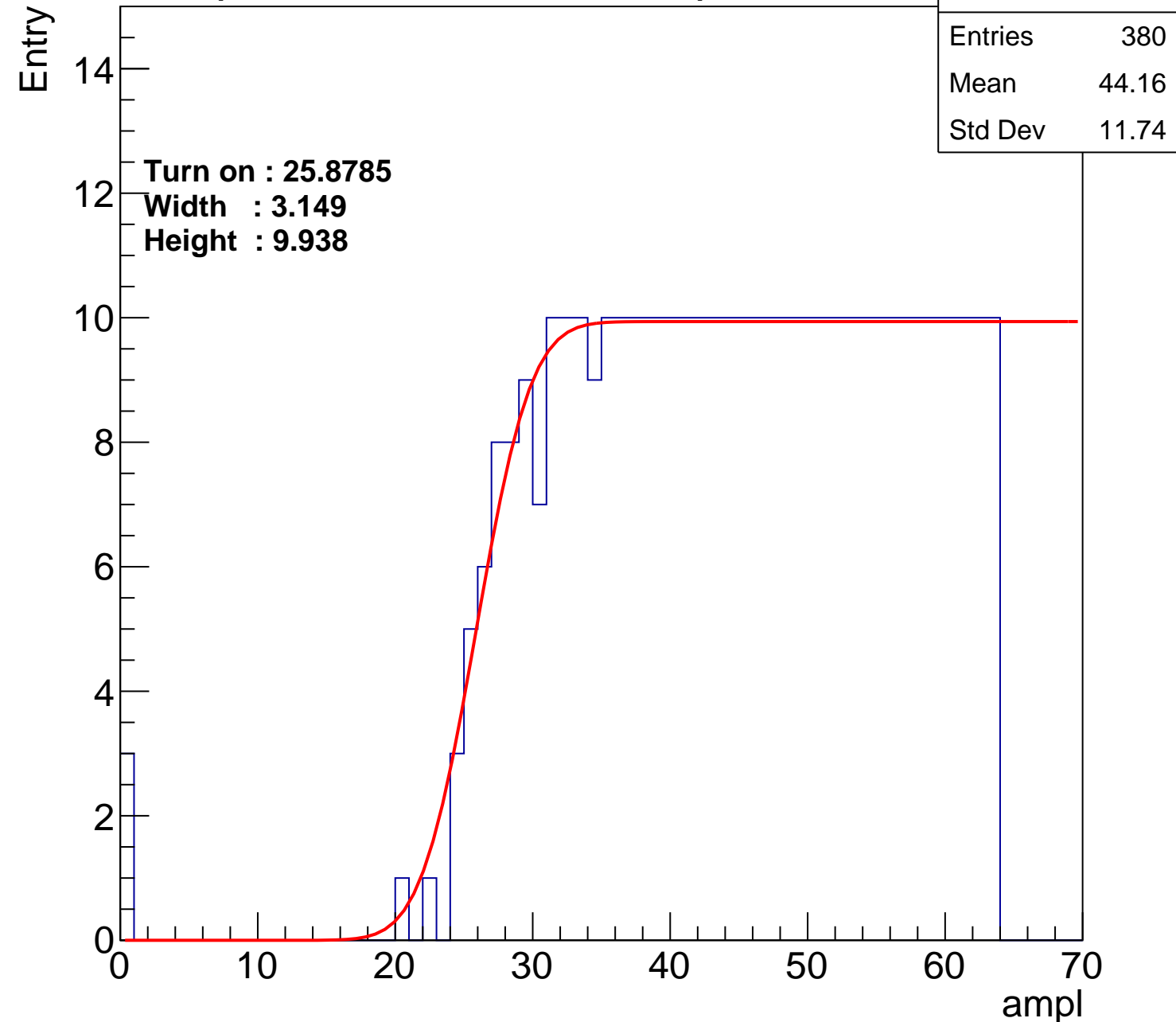
**Width : 3.149**

**Height : 9.938**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L100S, U16-ch7

**calib\_packv5\_042523\_0143.root, FC#4, port A2**

Entries	362
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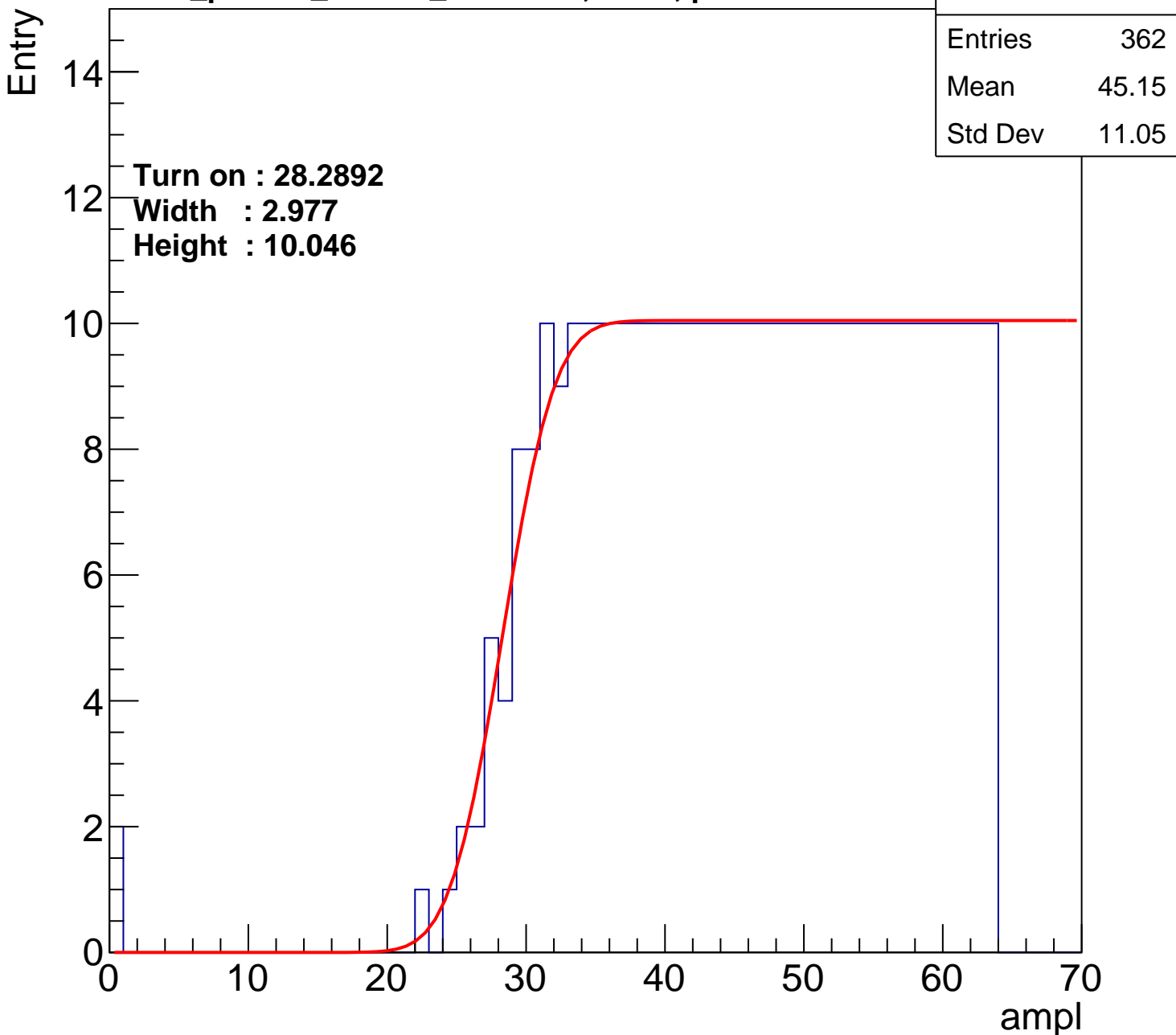
Mean	45.15
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Std Dev	11.05
---------	-------

**Turn on : 28.2892**

**Width : 2.977**

**Height : 10.046**



# B1L100S, U16-ch8

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	383
Mean	43.91
Std Dev	12.13

Turn on : 27.0274

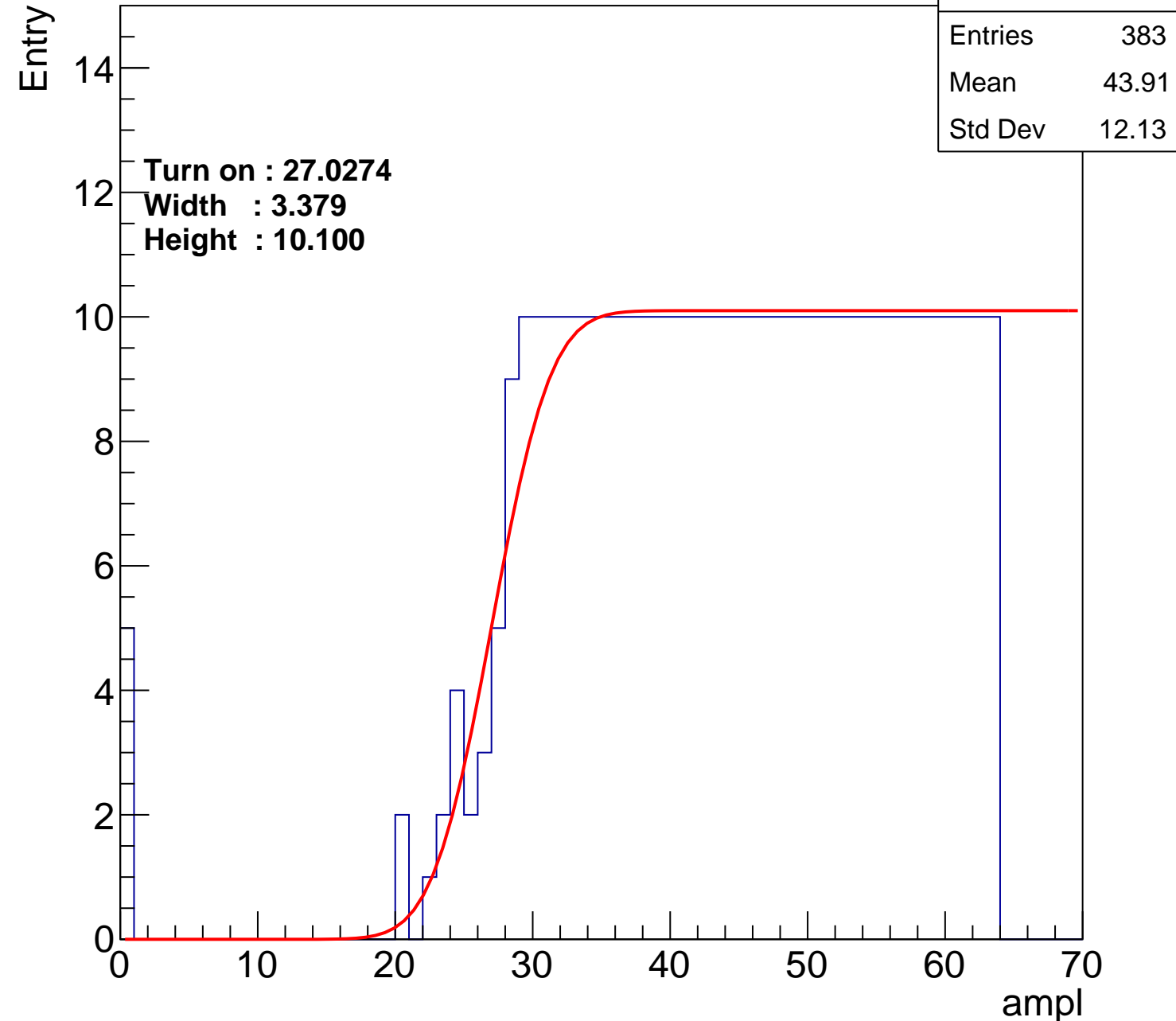
Width : 3.379

Height : 10.100

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch9

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	369
Mean	44.86
Std Dev	11.06

Turn on : 27.7268

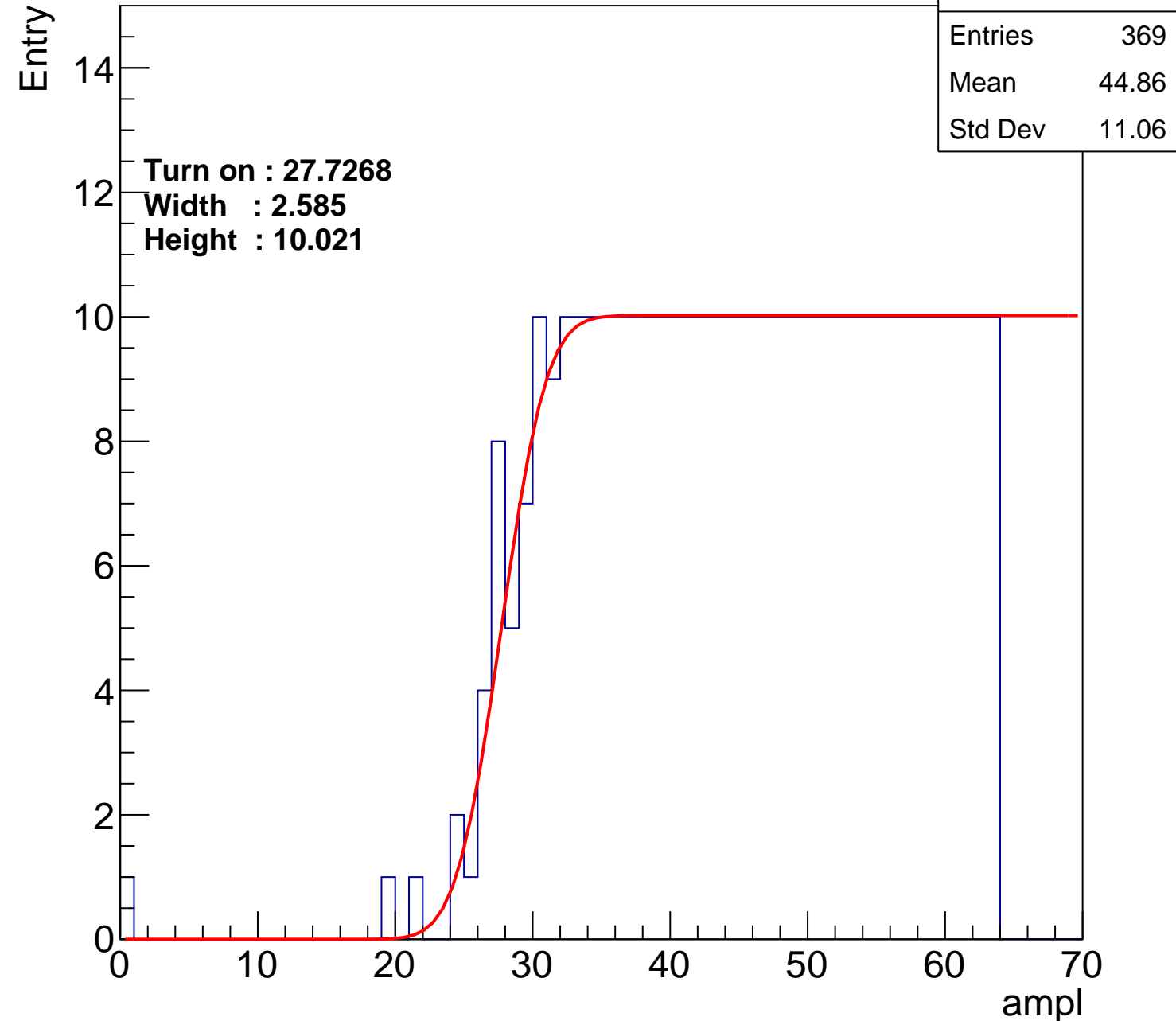
Width : 2.585

Height : 10.021

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch10

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	376
Mean	44.49
Std Dev	11.3

Turn on : 27.2366

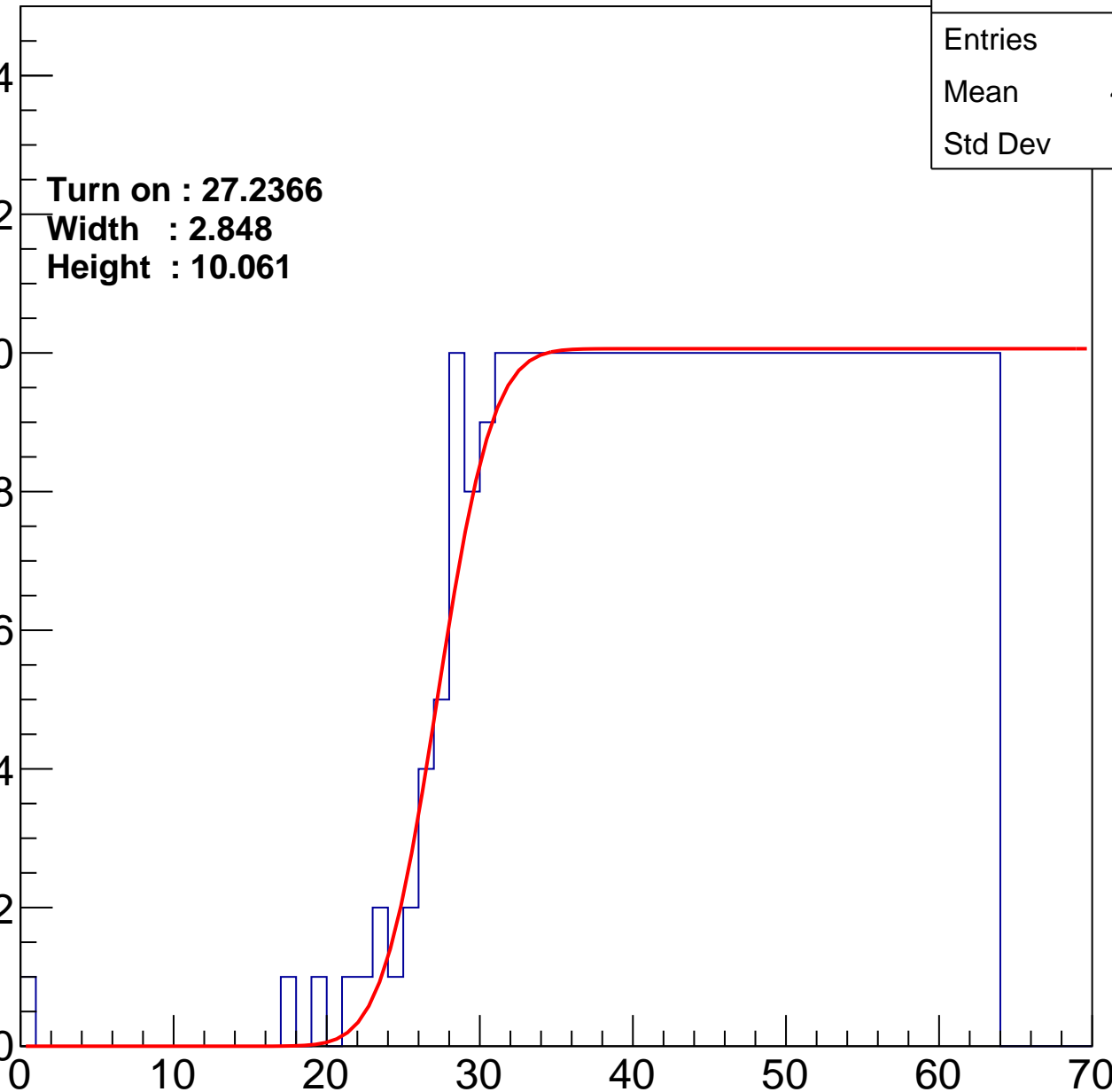
Width : 2.848

Height : 10.061

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch11

calib\_packv5\_042523\_0143.root, FC#4, port A2

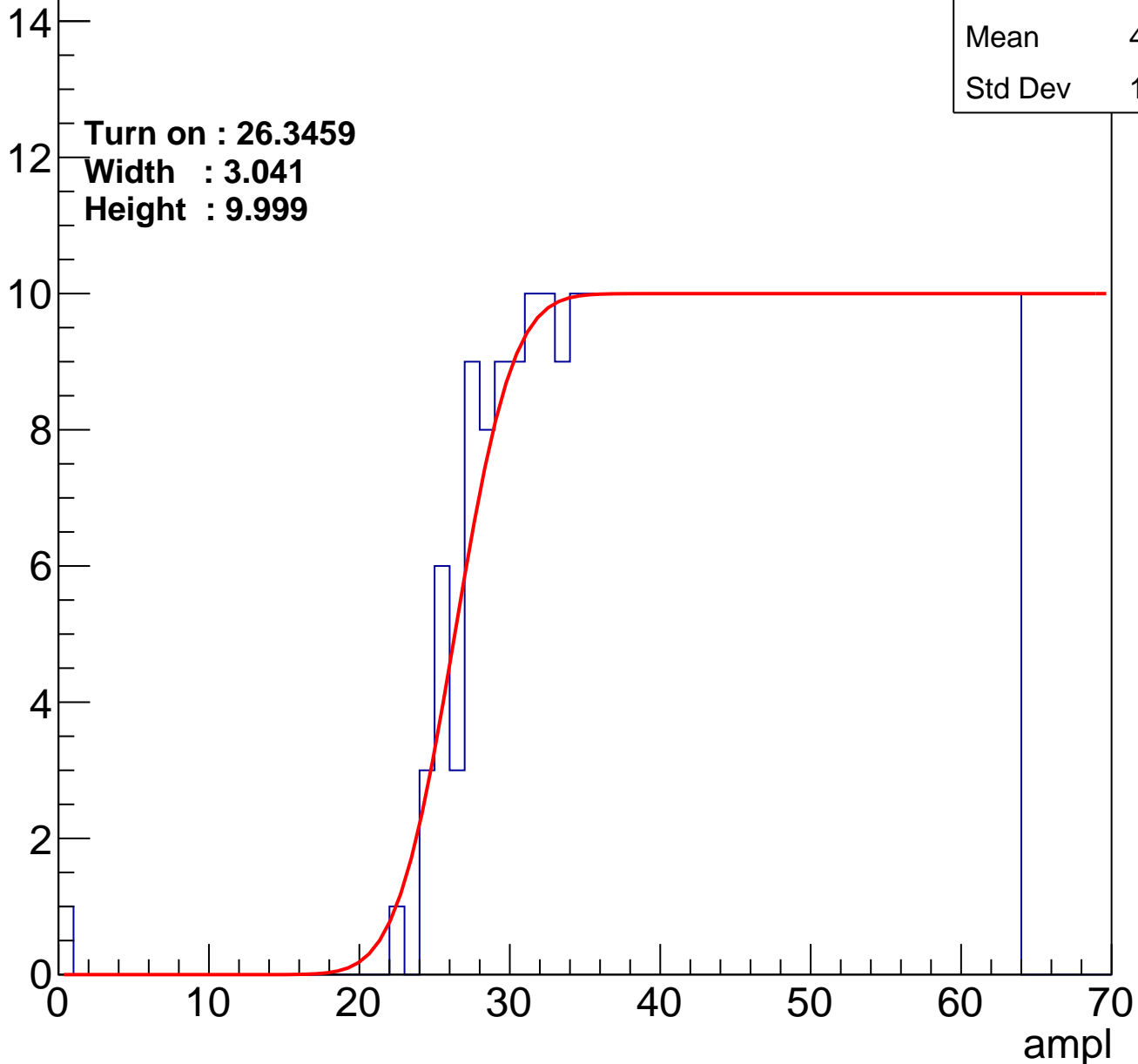
Entries	378
Mean	44.44
Std Dev	11.26

Turn on : 26.3459

Width : 3.041

Height : 9.999

Entry



# B1L100S, U16-ch12

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	397
Mean	43.36
Std Dev	12.12

Turn on : 24.7239

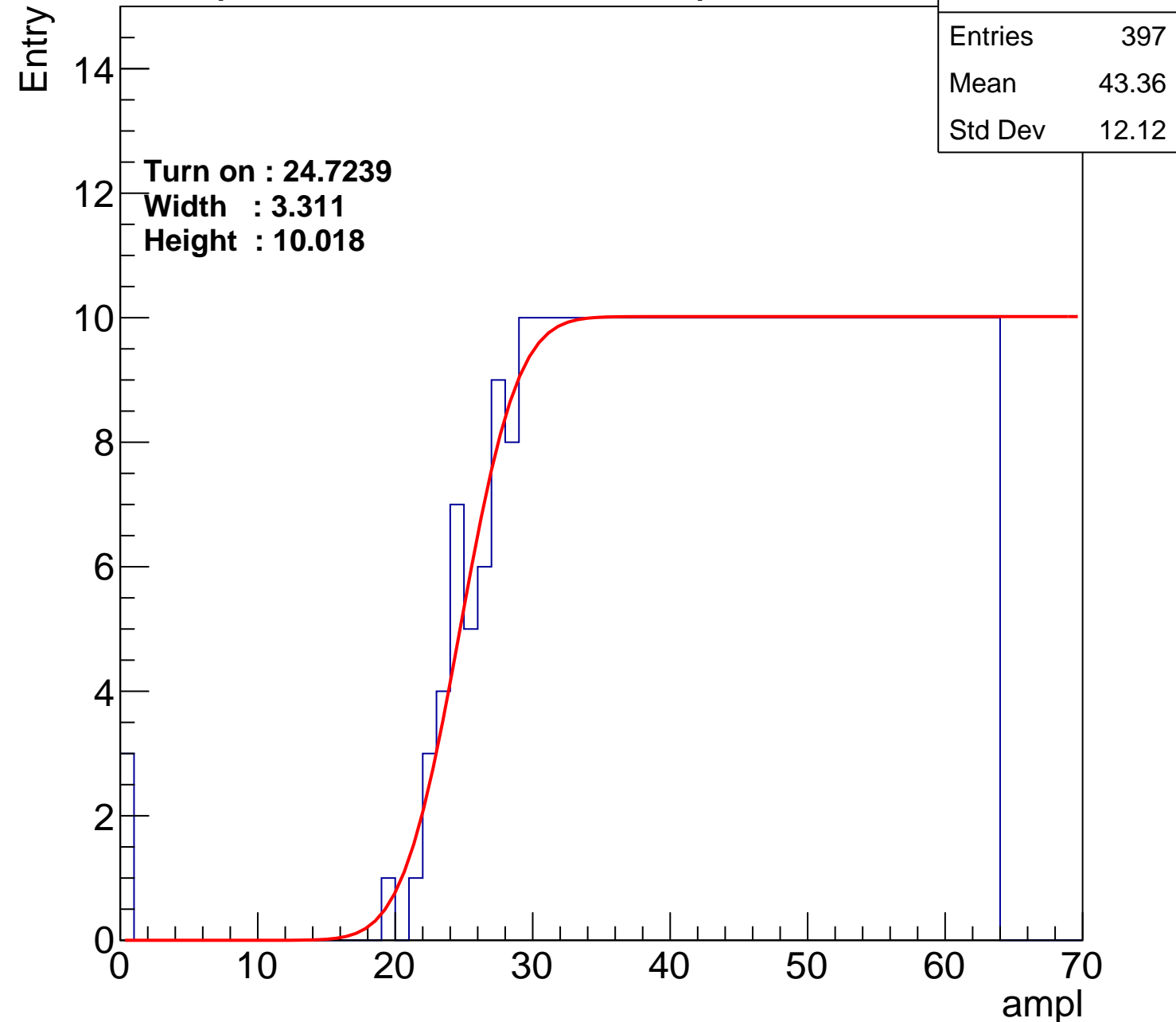
Width : 3.311

Height : 10.018

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch13

calib\_packv5\_042523\_0143.root, FC#4, port A2

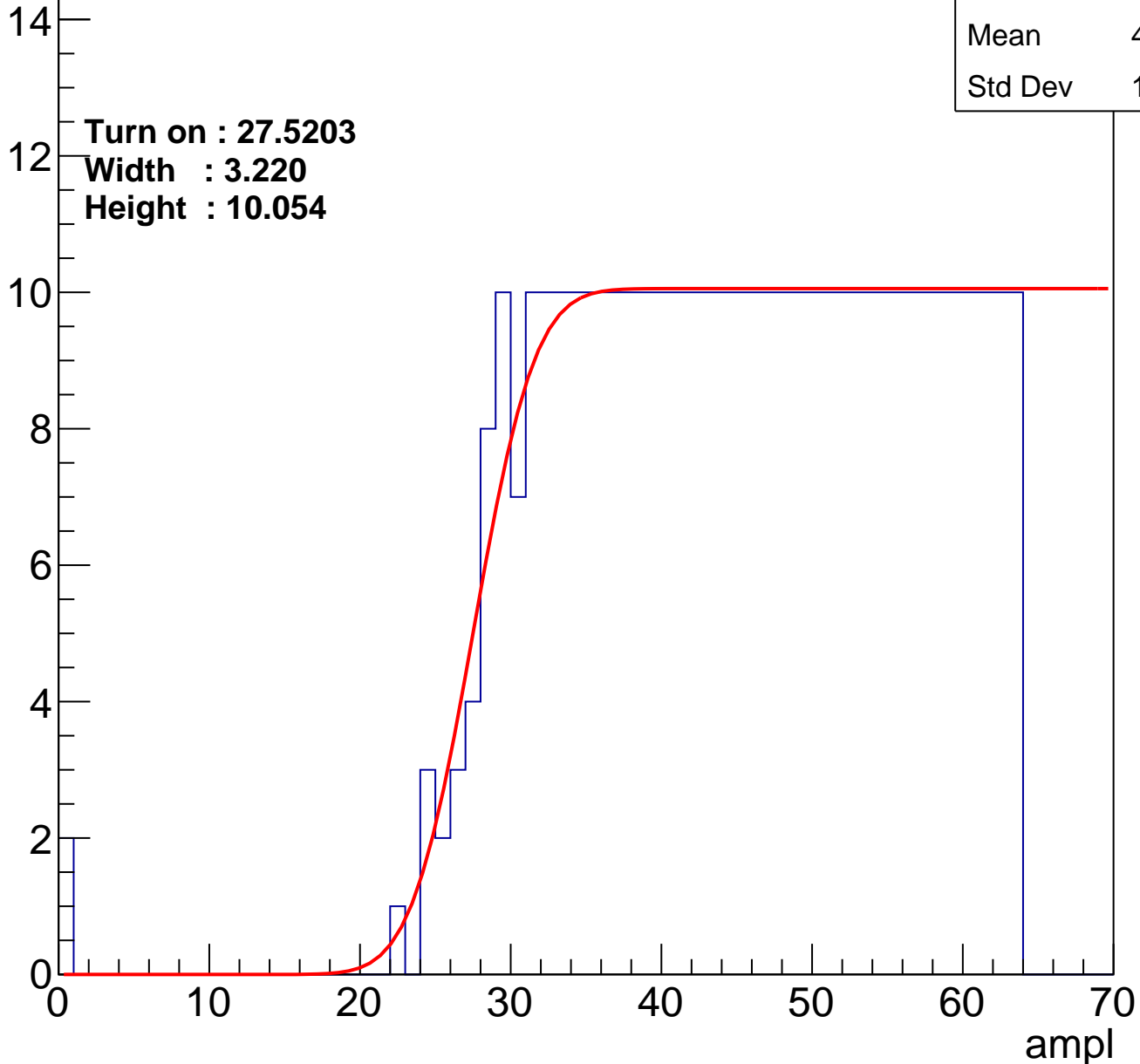
Entries	370
Mean	44.77
Std Dev	11.24

Turn on : 27.5203

Width : 3.220

Height : 10.054

Entry



# B1L100S, U16-ch14

calib\_packv5\_042523\_0143.root, FC#4, port A2

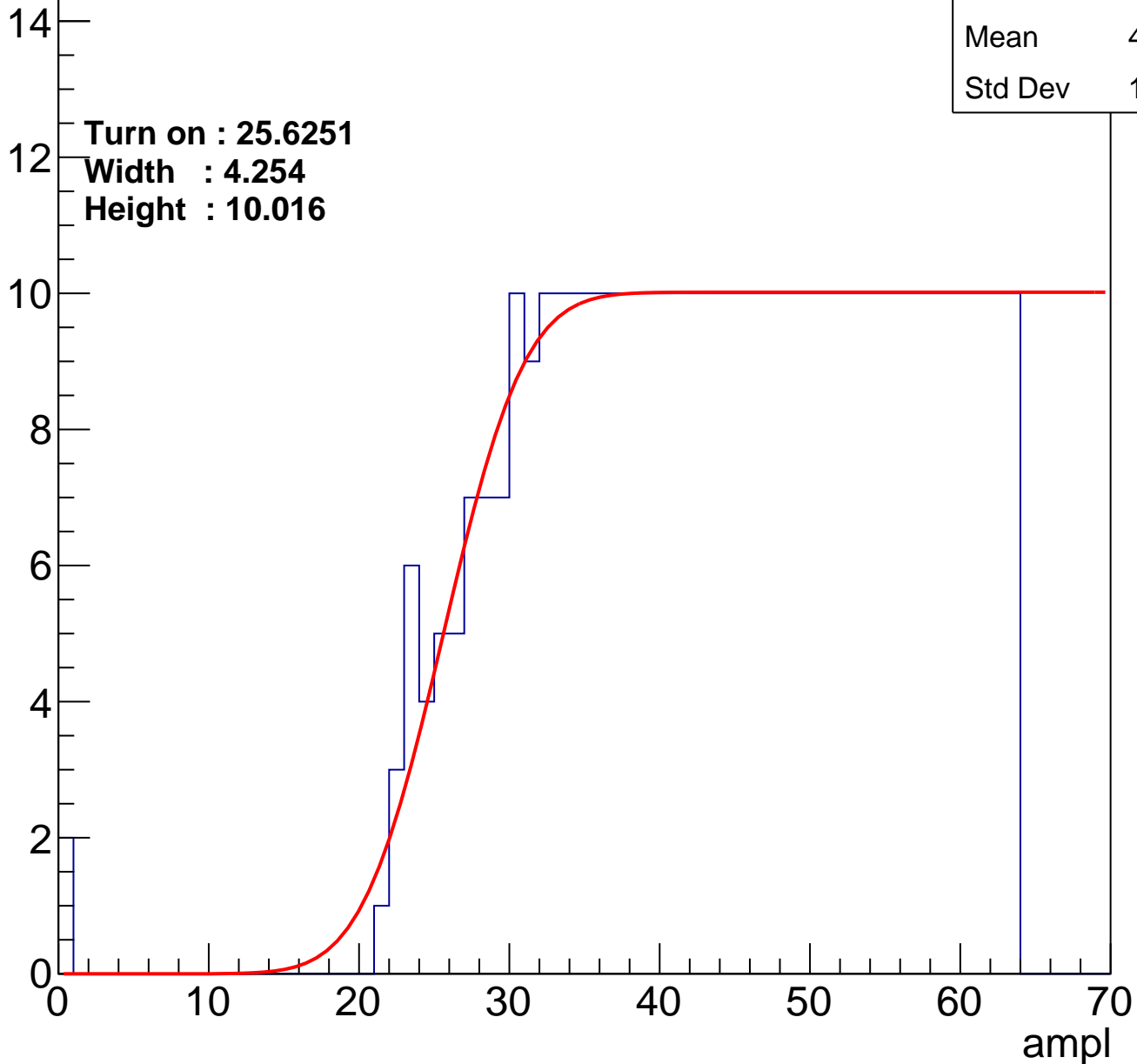
Entries	386
Mean	43.89
Std Dev	11.78

Turn on : 25.6251

Width : 4.254

Height : 10.016

Entry





# B1L100S, U16-ch15

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	370
Mean	44.61
Std Dev	11.65

Turn on : 27.3922

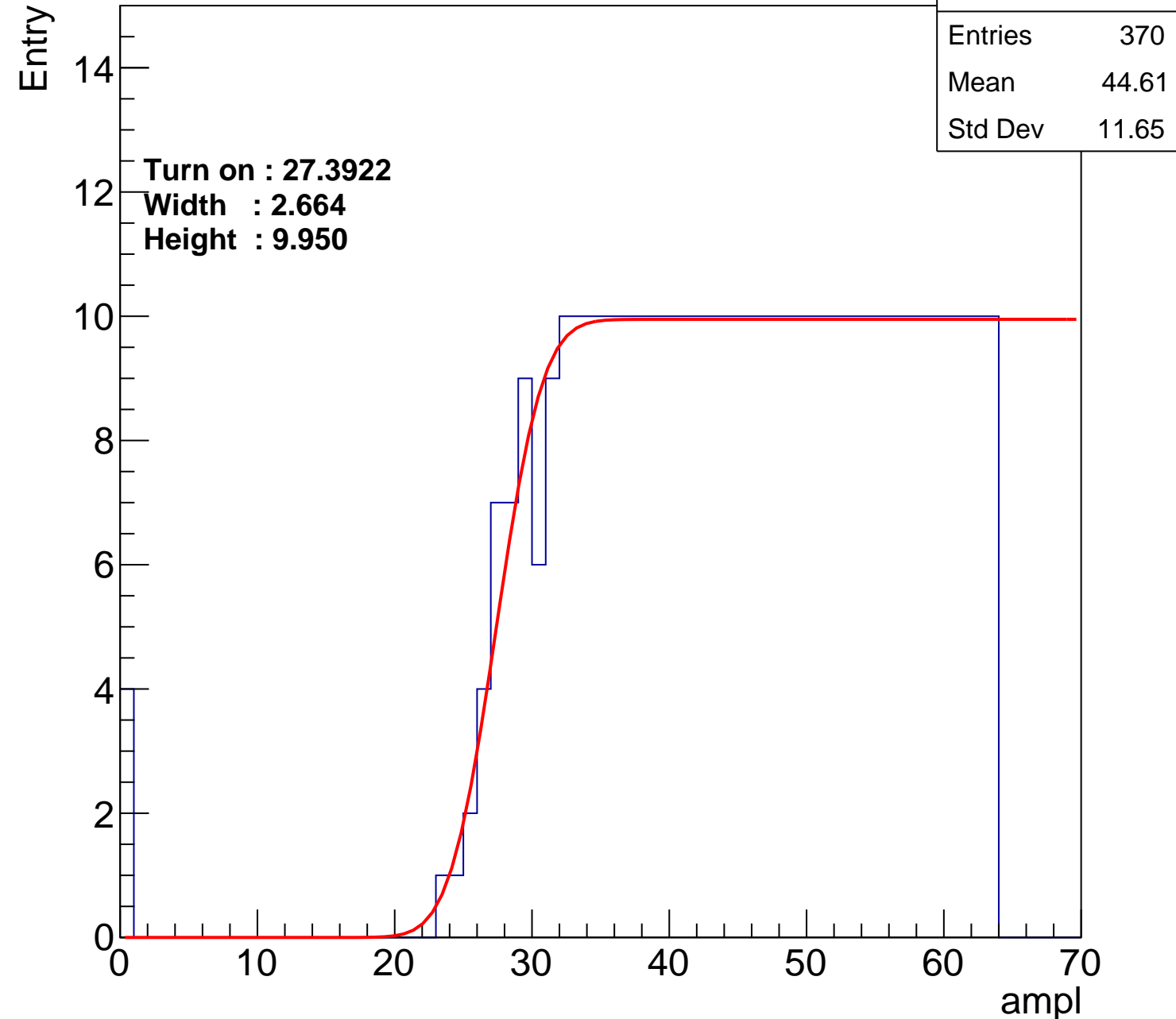
Width : 2.664

Height : 9.950

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch16

calib\_packv5\_042523\_0143.root, FC#4, port A2

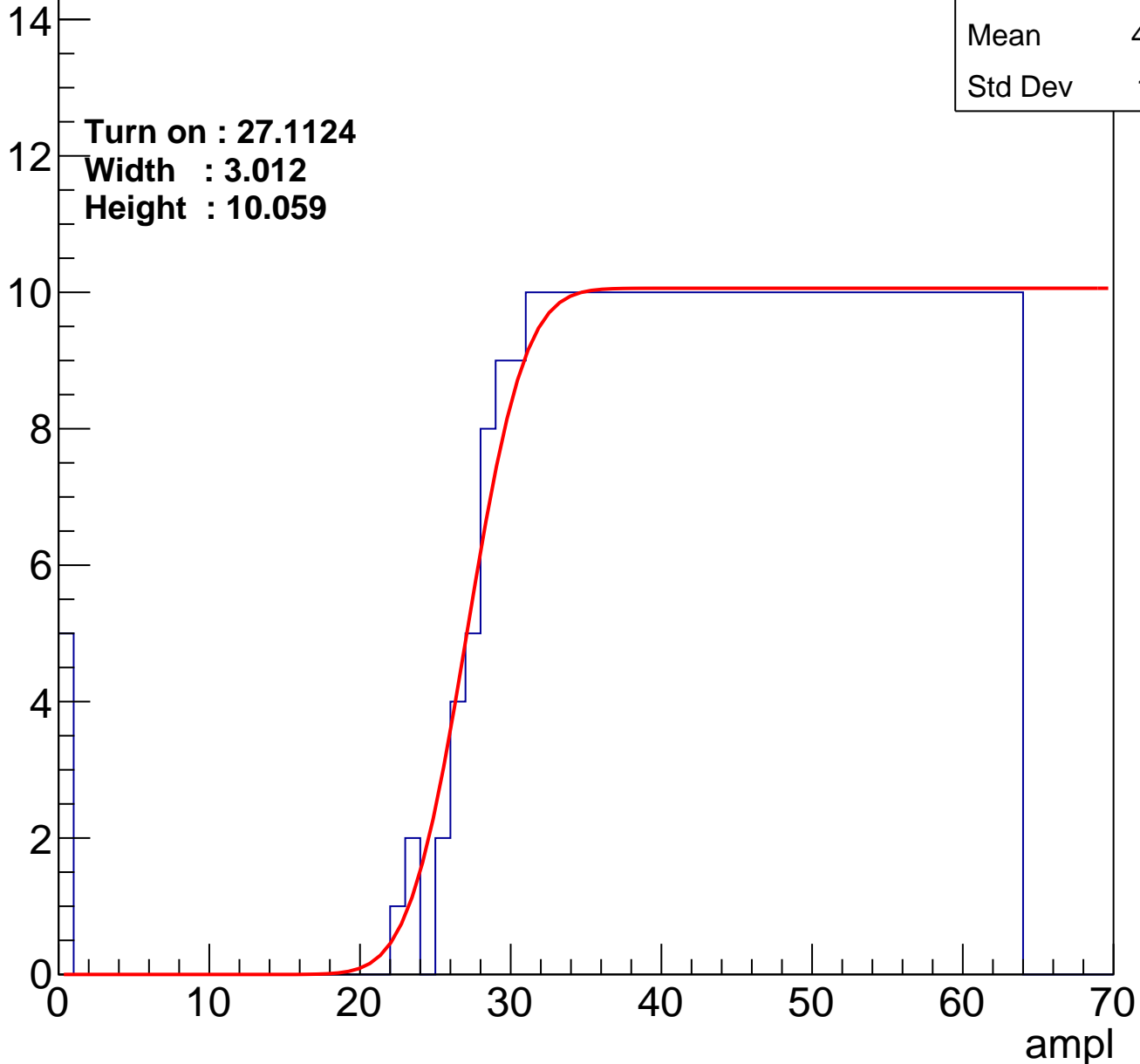
Entries	375
Mean	44.33
Std Dev	11.91

Turn on : 27.1124

Width : 3.012

Height : 10.059

Entry



# B1L100S, U16-ch17

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	384
Mean	44.1
Std Dev	11.5

Turn on : 25.8463

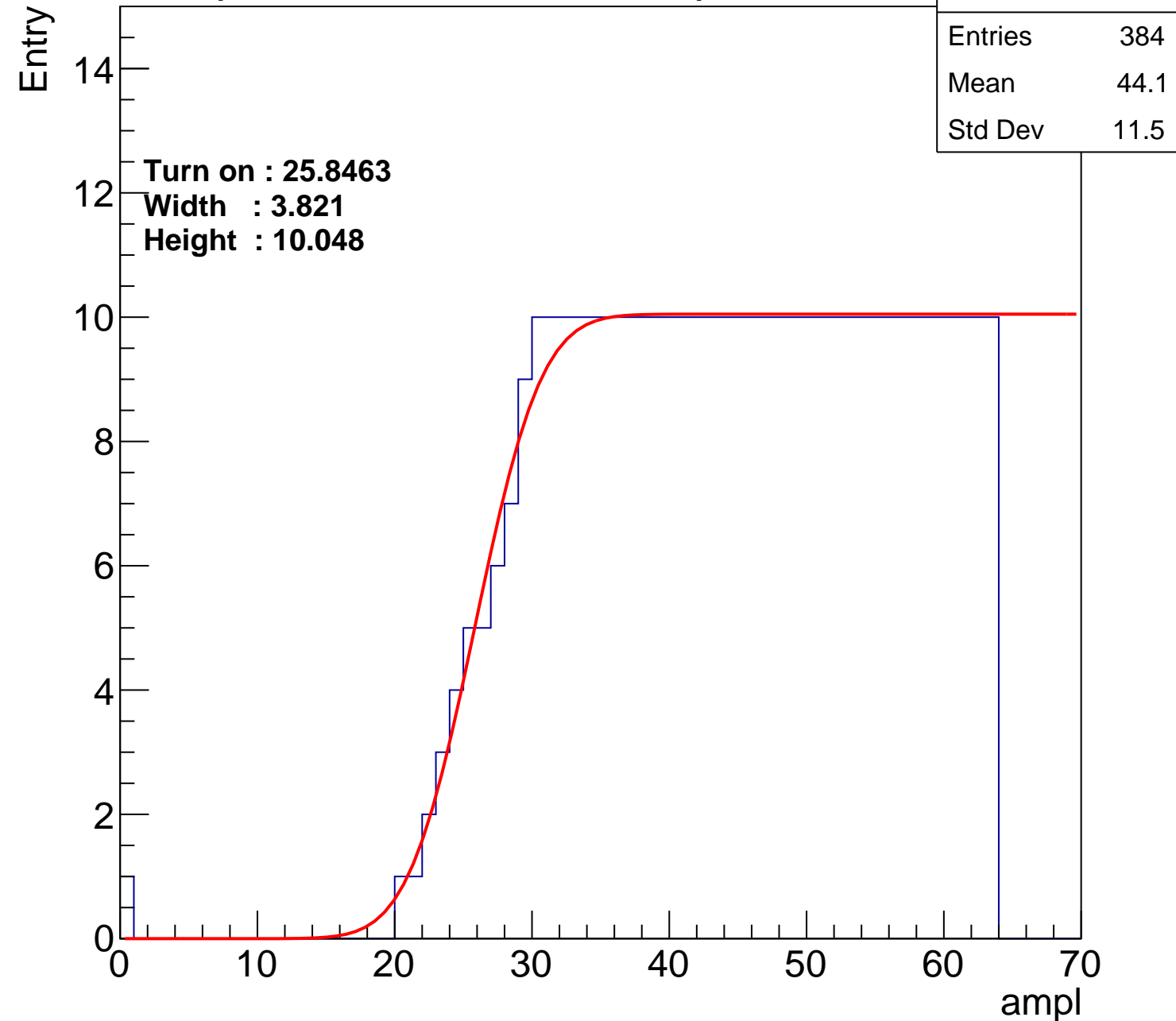
Width : 3.821

Height : 10.048

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch18

calib\_packv5\_042523\_0143.root, FC#4, port A2

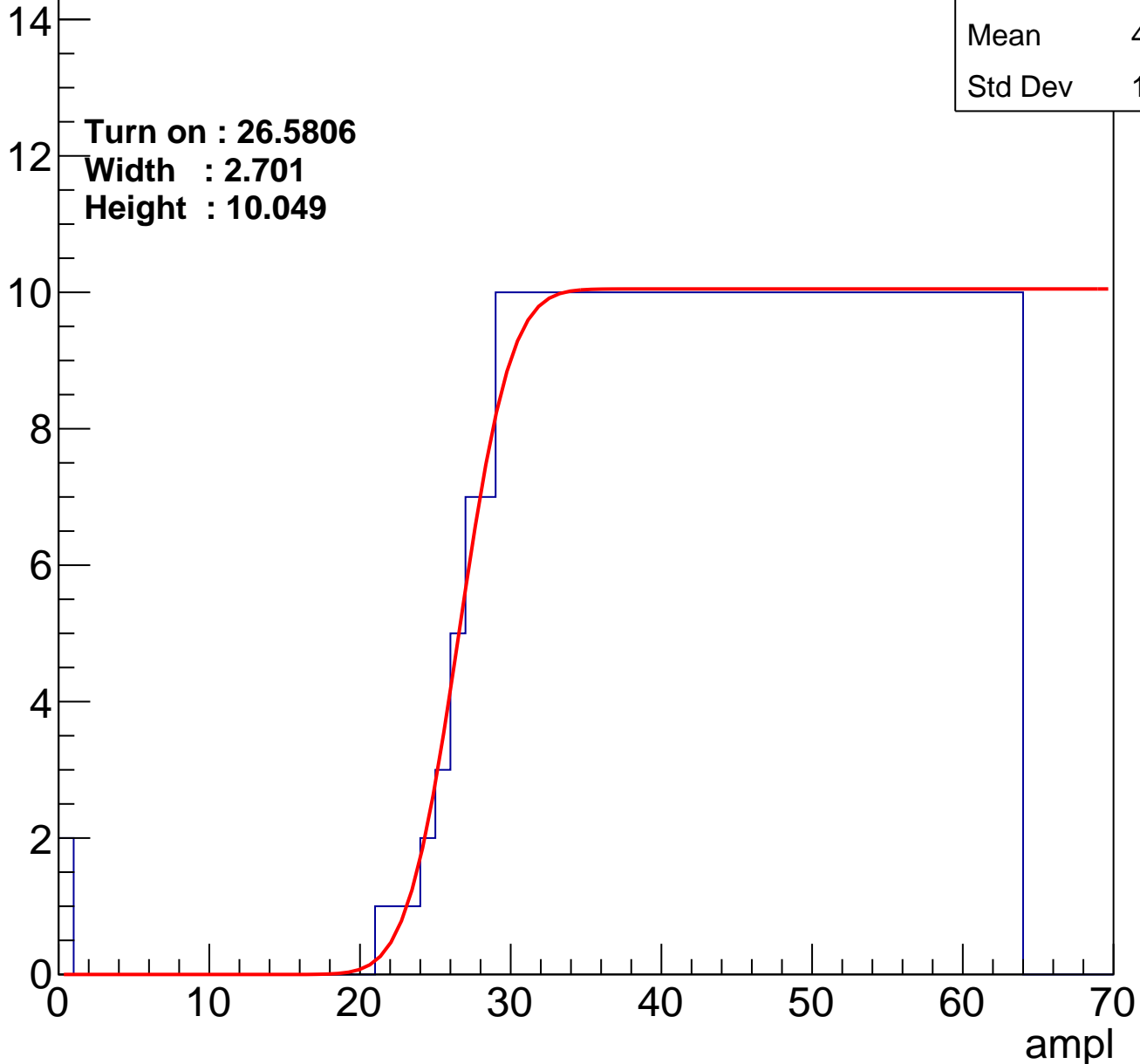
Entries	379
Mean	44.34
Std Dev	11.45

**Turn on : 26.5806**

**Width : 2.701**

**Height : 10.049**

Entry



# B1L100S, U16-ch19

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	384
Mean	44.03
Std Dev	11.67

Turn on : 26.8756

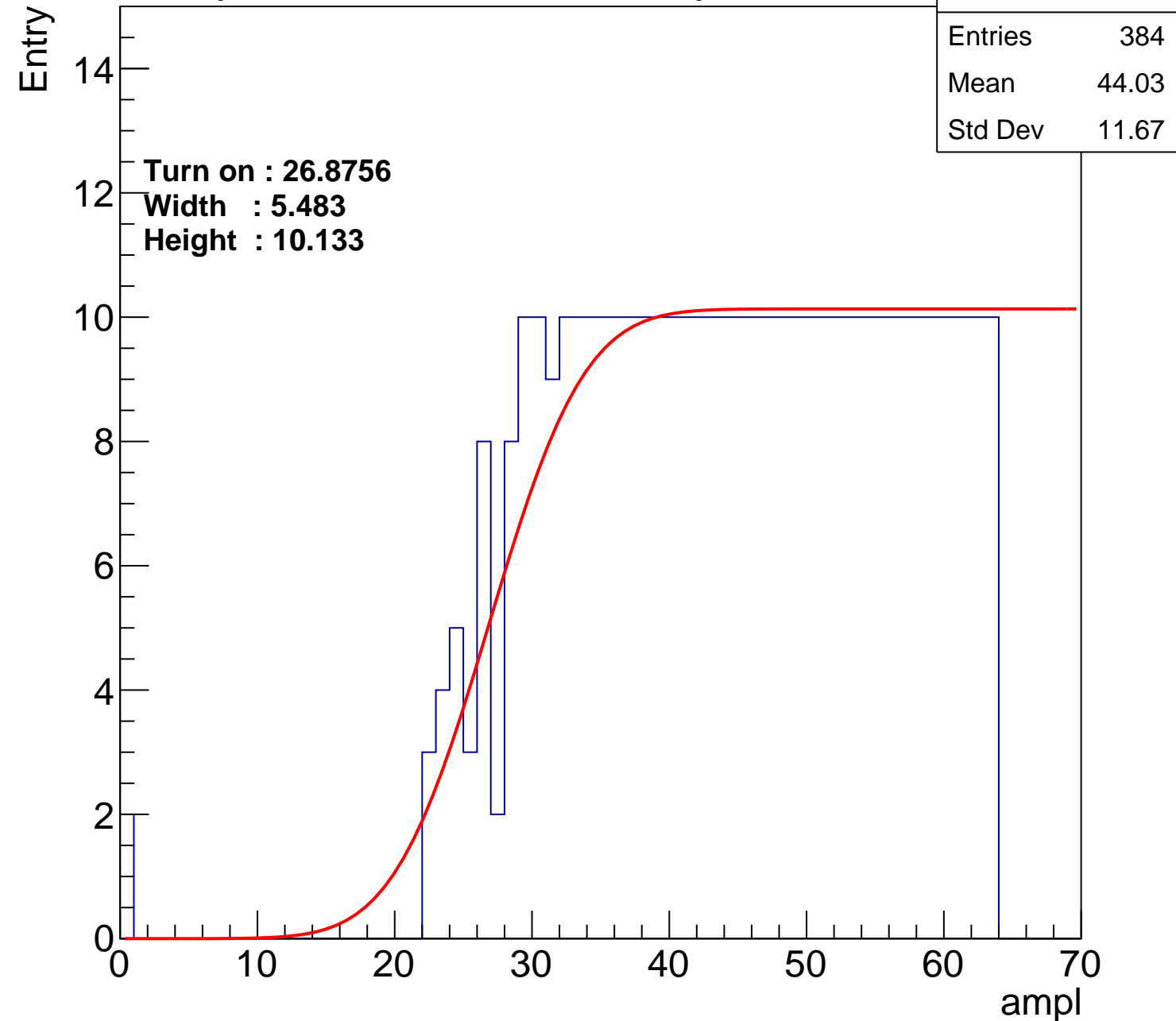
Width : 5.483

Height : 10.133

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch20

calib\_packv5\_042523\_0143.root, FC#4, port A2

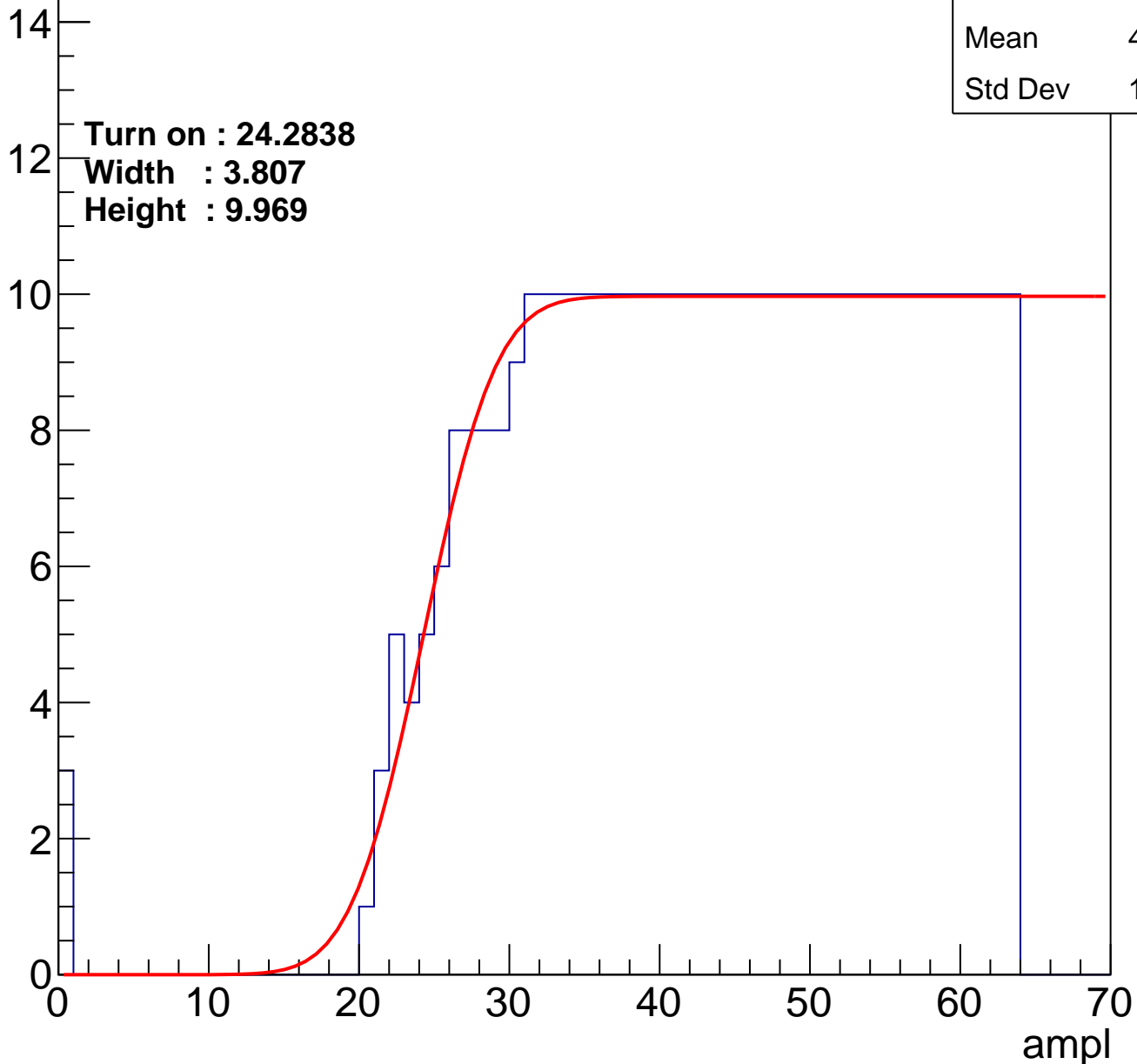
Entries	398
Mean	43.25
Std Dev	12.23

Turn on : 24.2838

Width : 3.807

Height : 9.969

Entry



# B1L100S, U16-ch21

calib\_packv5\_042523\_0143.root, FC#4, port A2

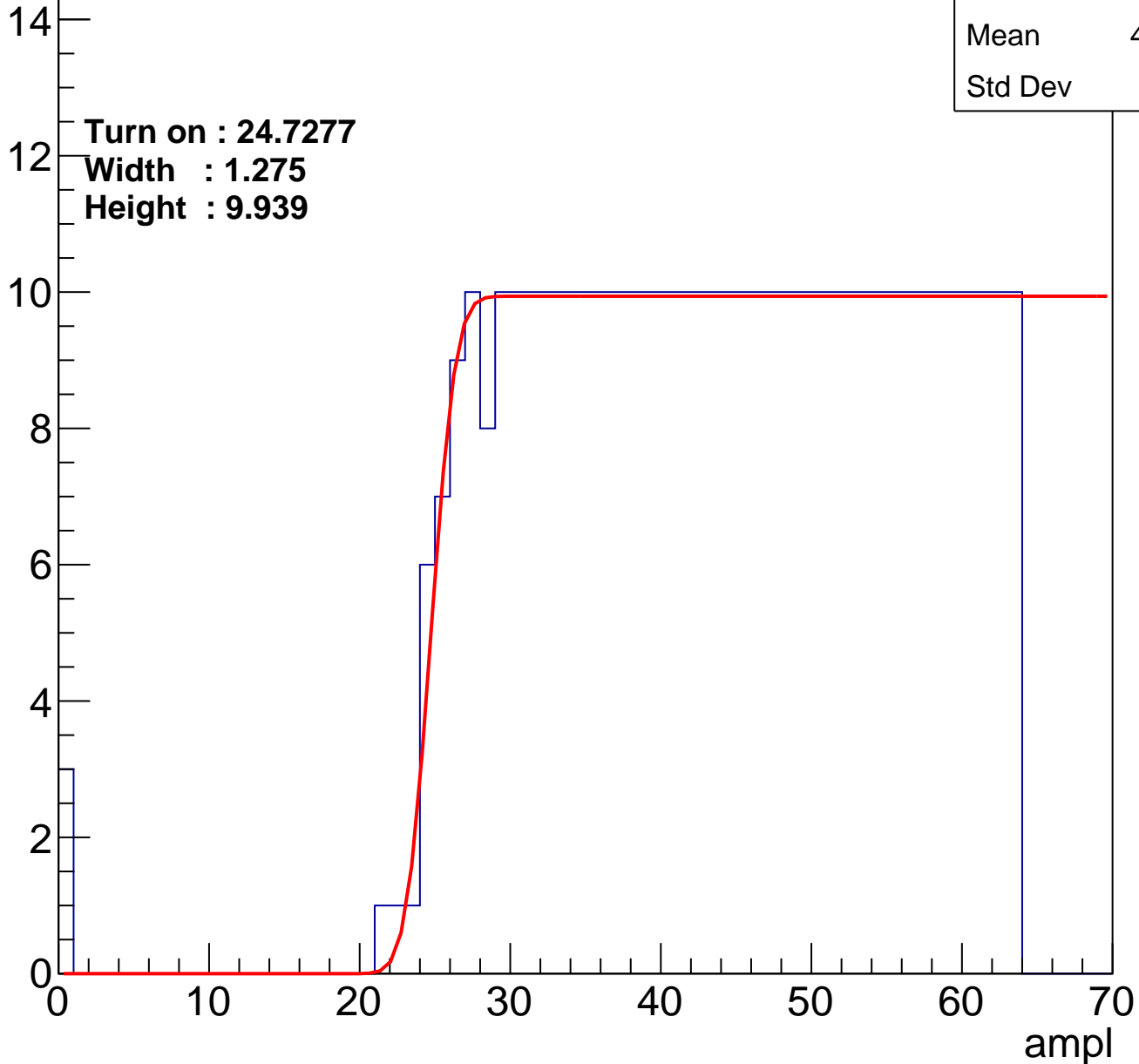
Entries	396
Mean	43.47
Std Dev	12

Turn on : 24.7277

Width : 1.275

Height : 9.939

Entry



# B1L100S, U16-ch22

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	394
Mean	43.45
Std Dev	12.2

Turn on : 25.3394

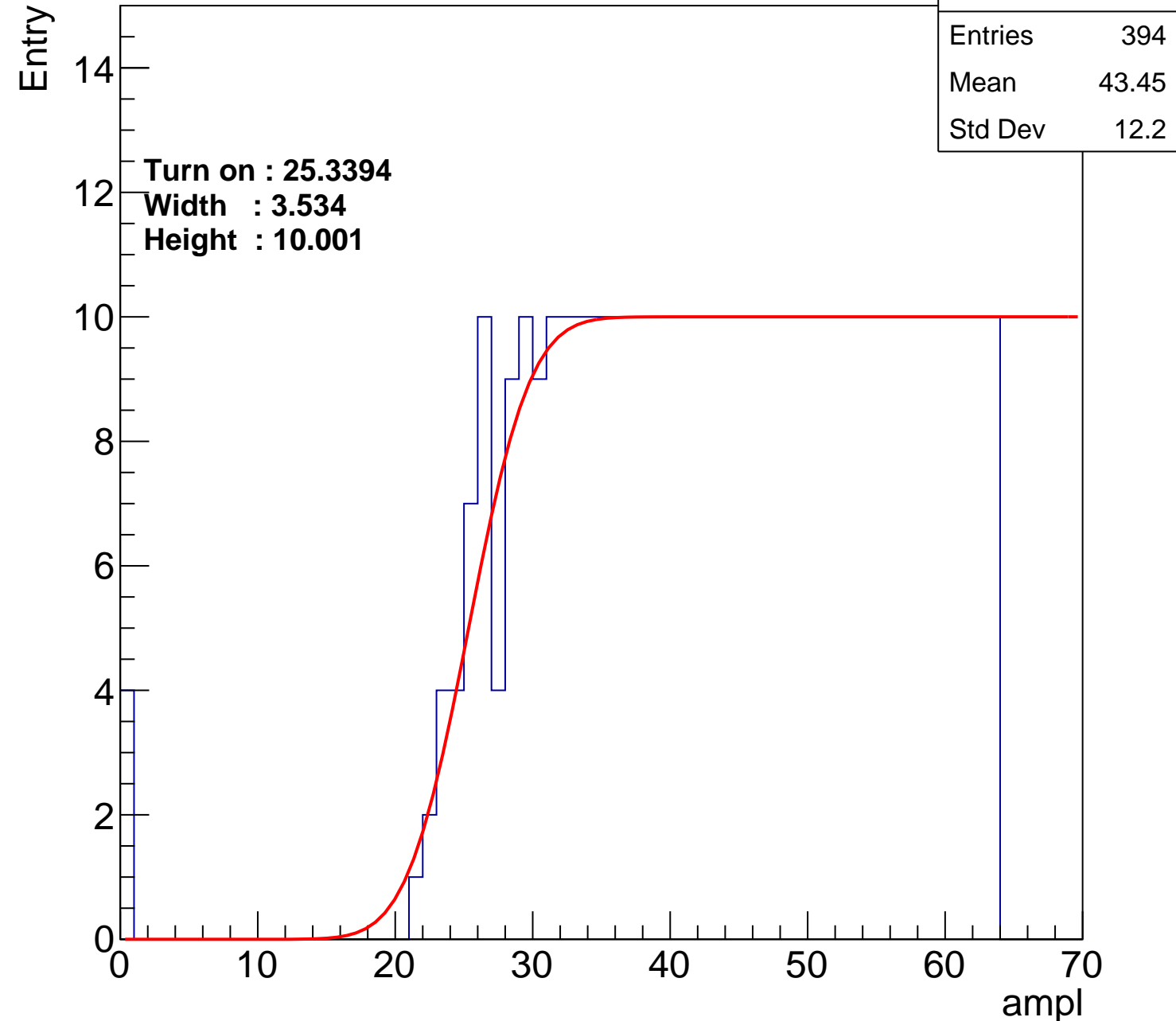
Width : 3.534

Height : 10.001

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L100S, U16-ch23

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	379
Mean	44.38
Std Dev	11.31

Turn on : 26.2903

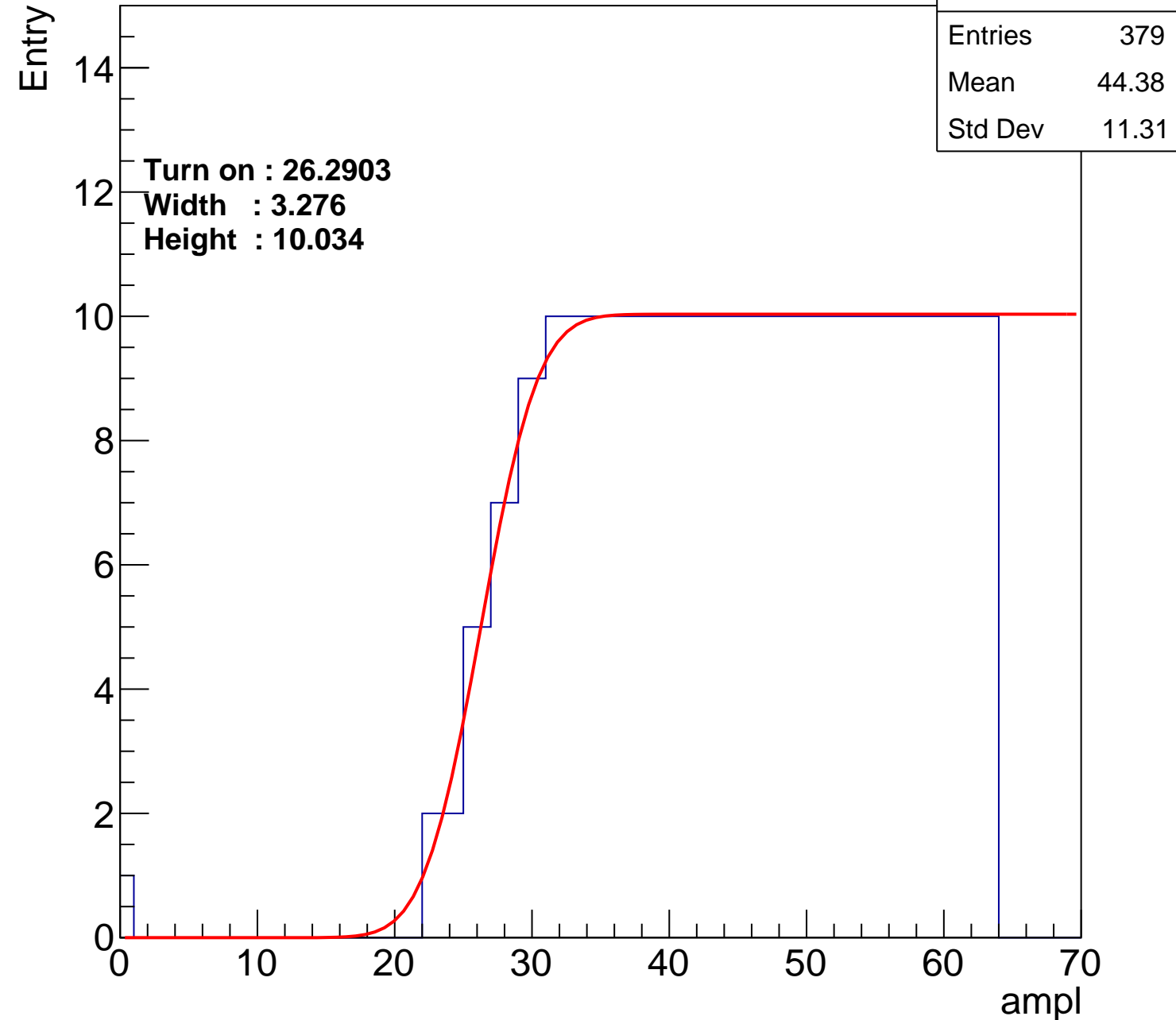
Width : 3.276

Height : 10.034

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch24

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	407
Mean	42.86
Std Dev	12.39

Turn on : 25.0723

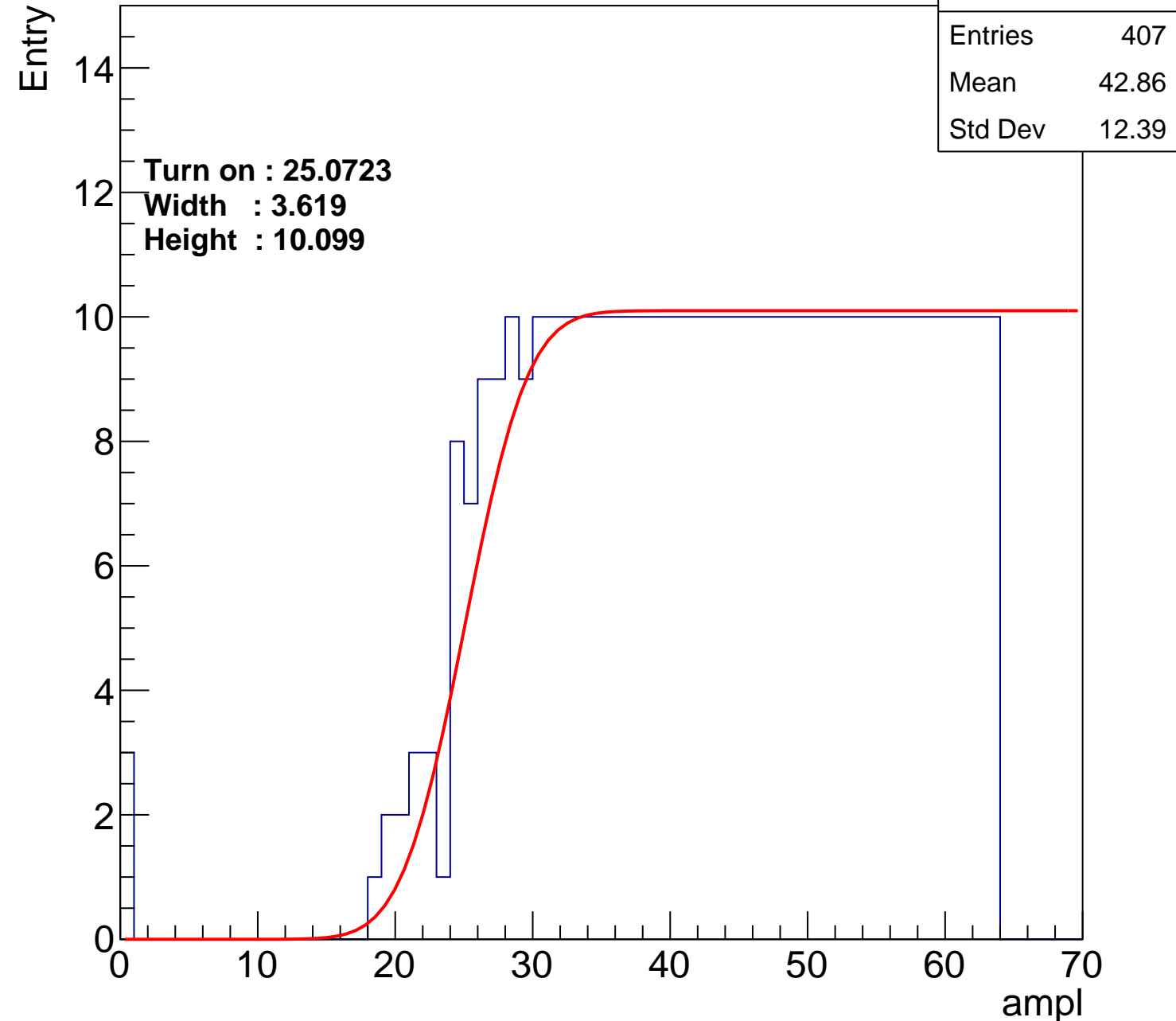
Width : 3.619

Height : 10.099

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch25

calib\_packv5\_042523\_0143.root, FC#4, port A2

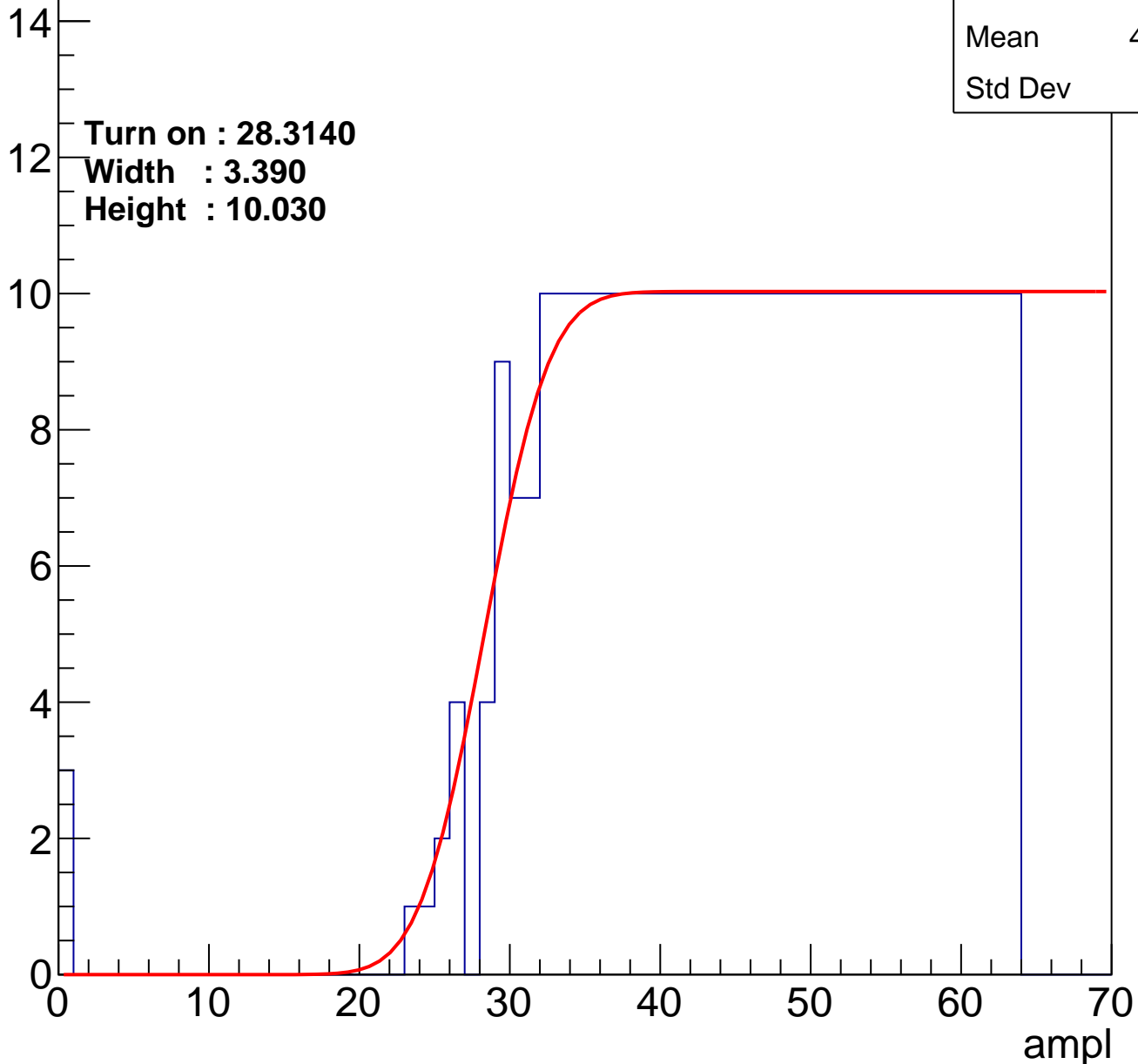
Entries	358
Mean	45.25
Std Dev	11.2

Turn on : 28.3140

Width : 3.390

Height : 10.030

Entry



# B1L100S, U16-ch26

calib\_packv5\_042523\_0143.root, FC#4, port A2

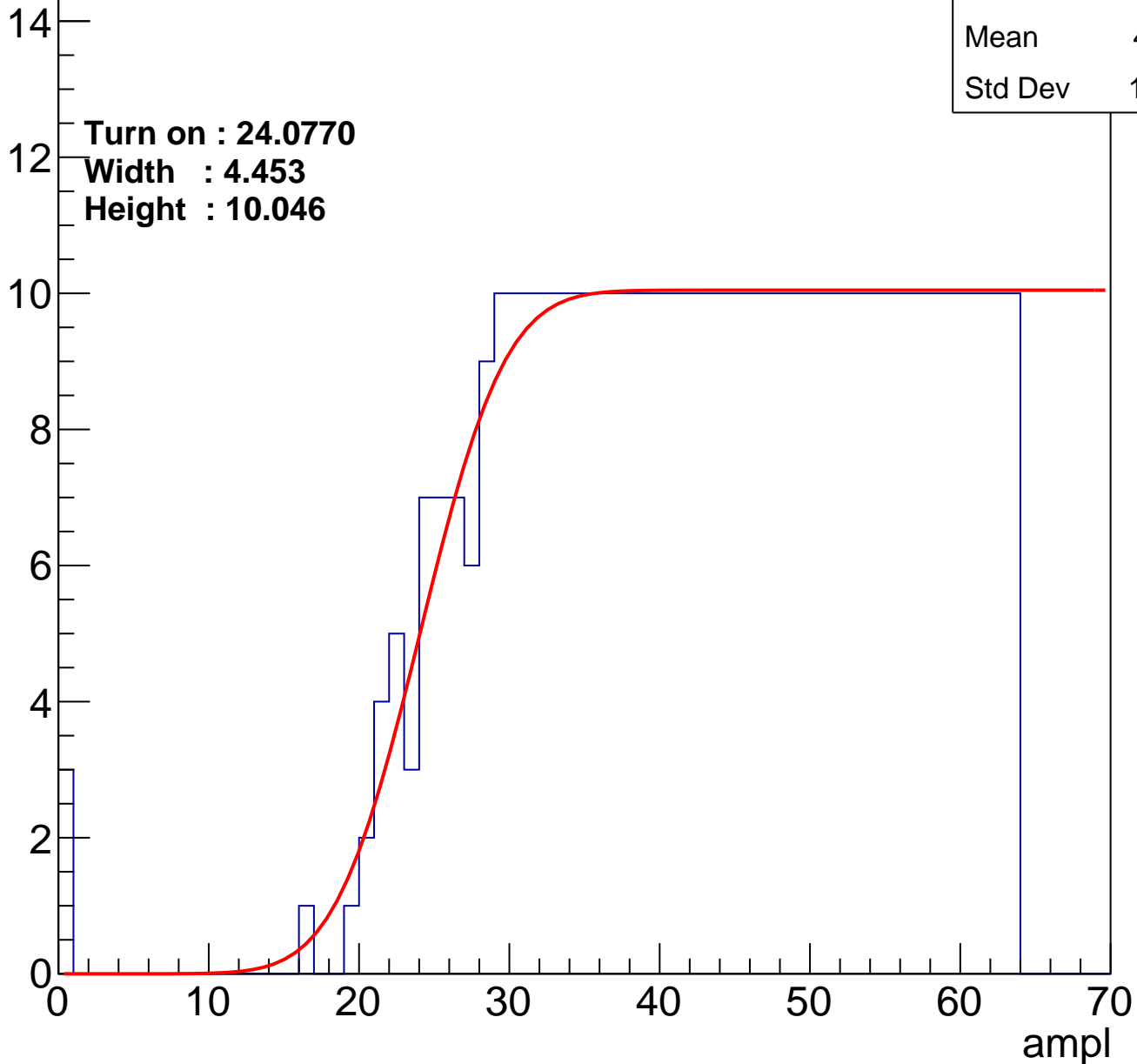
Entries	405
Mean	42.91
Std Dev	12.42

Turn on : 24.0770

Width : 4.453

Height : 10.046

Entry



# B1L100S, U16-ch27

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	379
Mean	44.22
Std Dev	11.71

Turn on : 26.5325

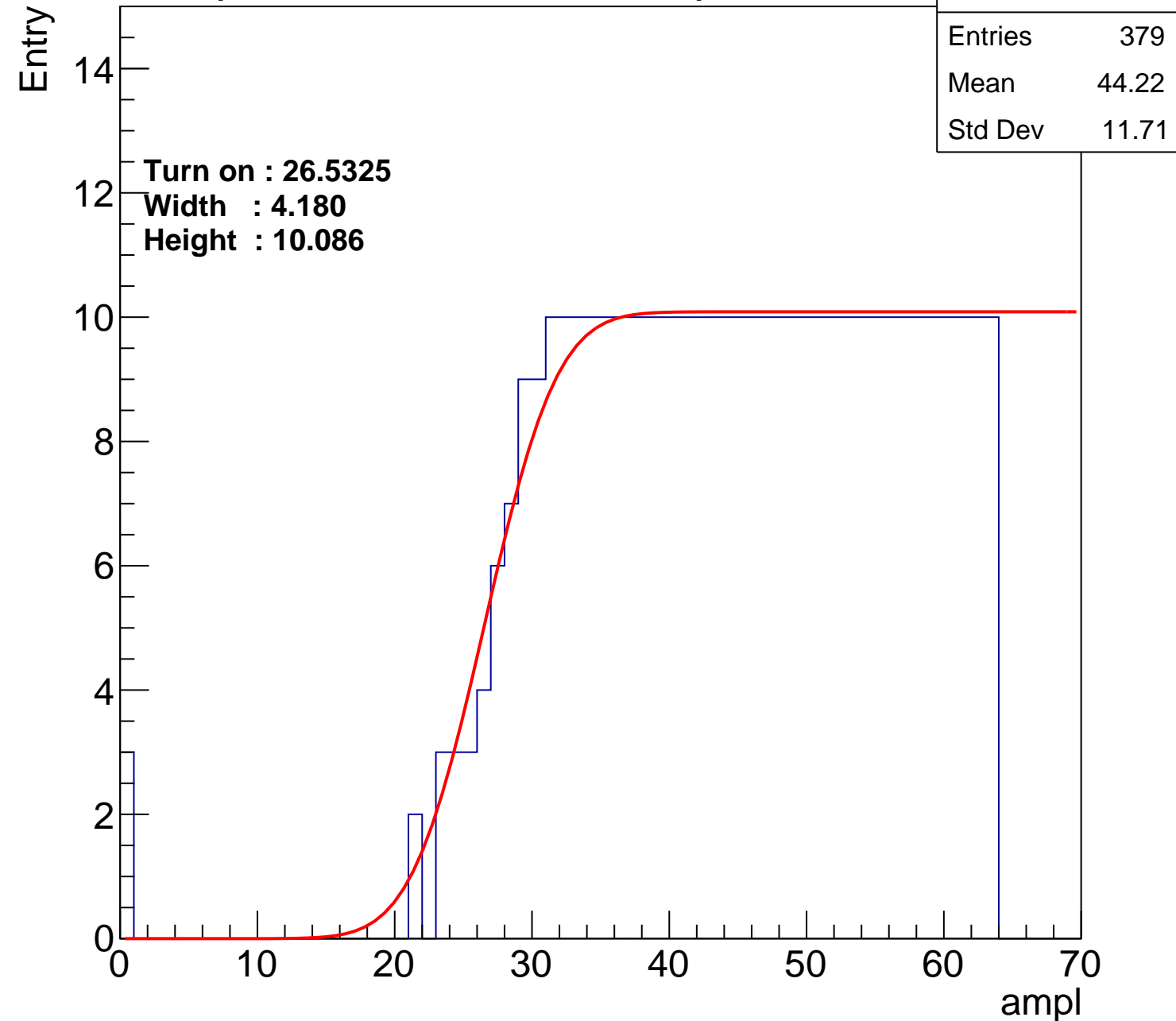
Width : 4.180

Height : 10.086

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch28

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	392
Mean	43.68
Std Dev	11.82

Turn on : 25.5074

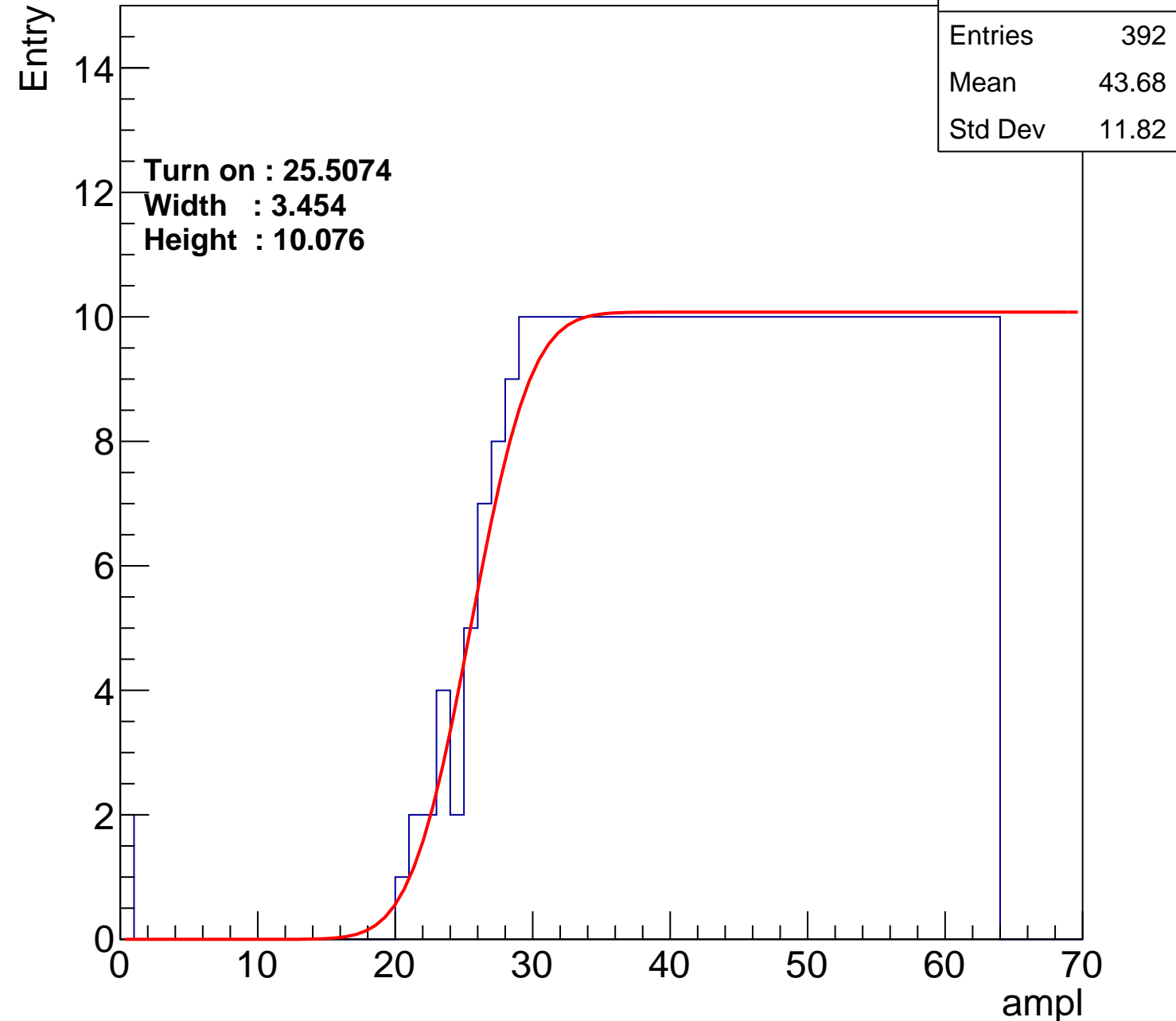
Width : 3.454

Height : 10.076

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch29

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	363
Mean	45.01
Std Dev	11.31

**Turn on : 28.1835**

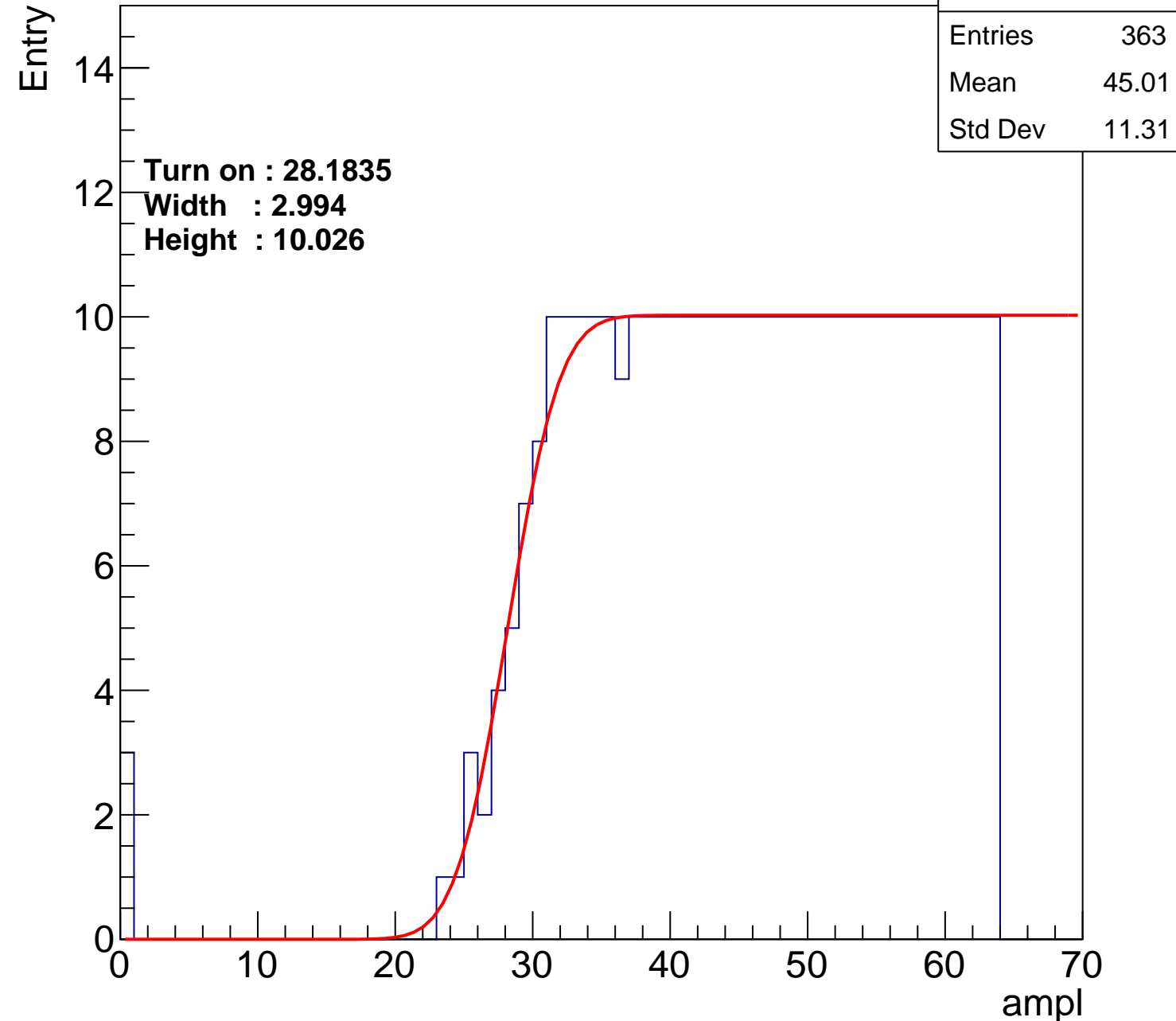
**Width : 2.994**

**Height : 10.026**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch30

calib\_packv5\_042523\_0143.root, FC#4, port A2

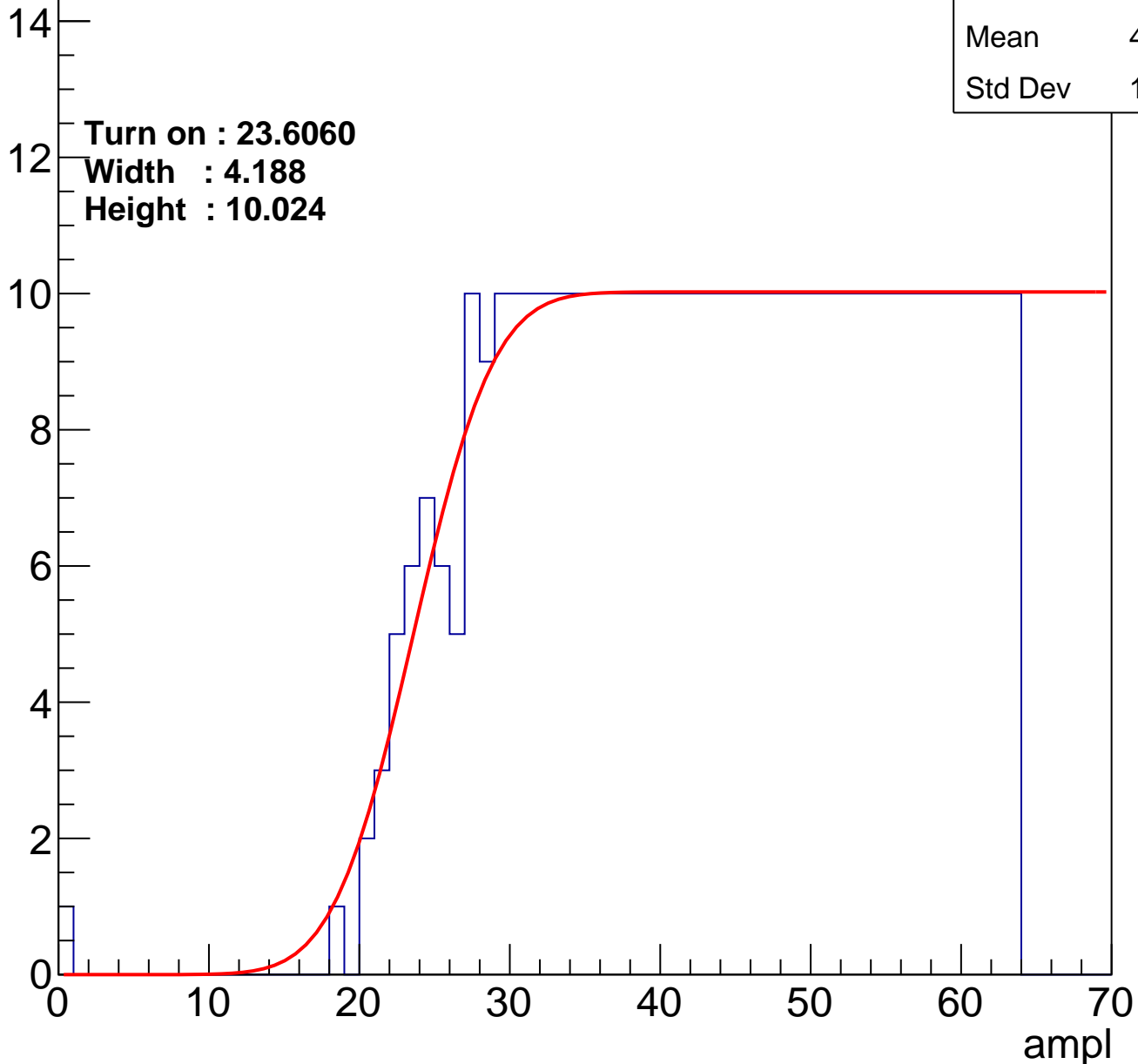
Entries	405
Mean	43.06
Std Dev	12.06

Turn on : 23.6060

Width : 4.188

Height : 10.024

Entry





# B1L100S, U16-ch31

calib\_packv5\_042523\_0143.root, FC#4, port A2

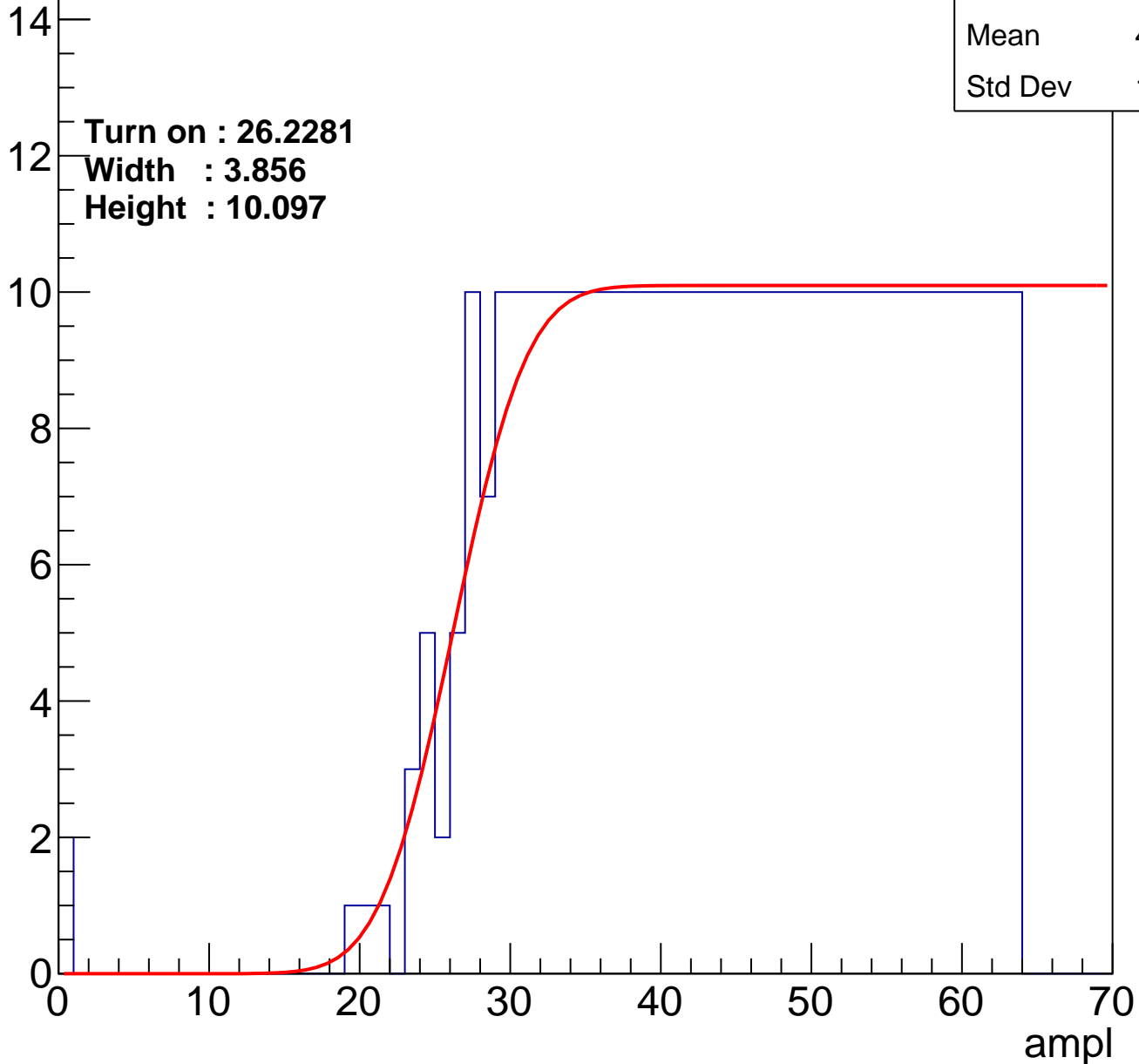
Entries	387
Mean	43.91
Std Dev	11.71

Turn on : 26.2281

Width : 3.856

Height : 10.097

Entry



# B1L100S, U16-ch32

calib\_packv5\_042523\_0143.root, FC#4, port A2

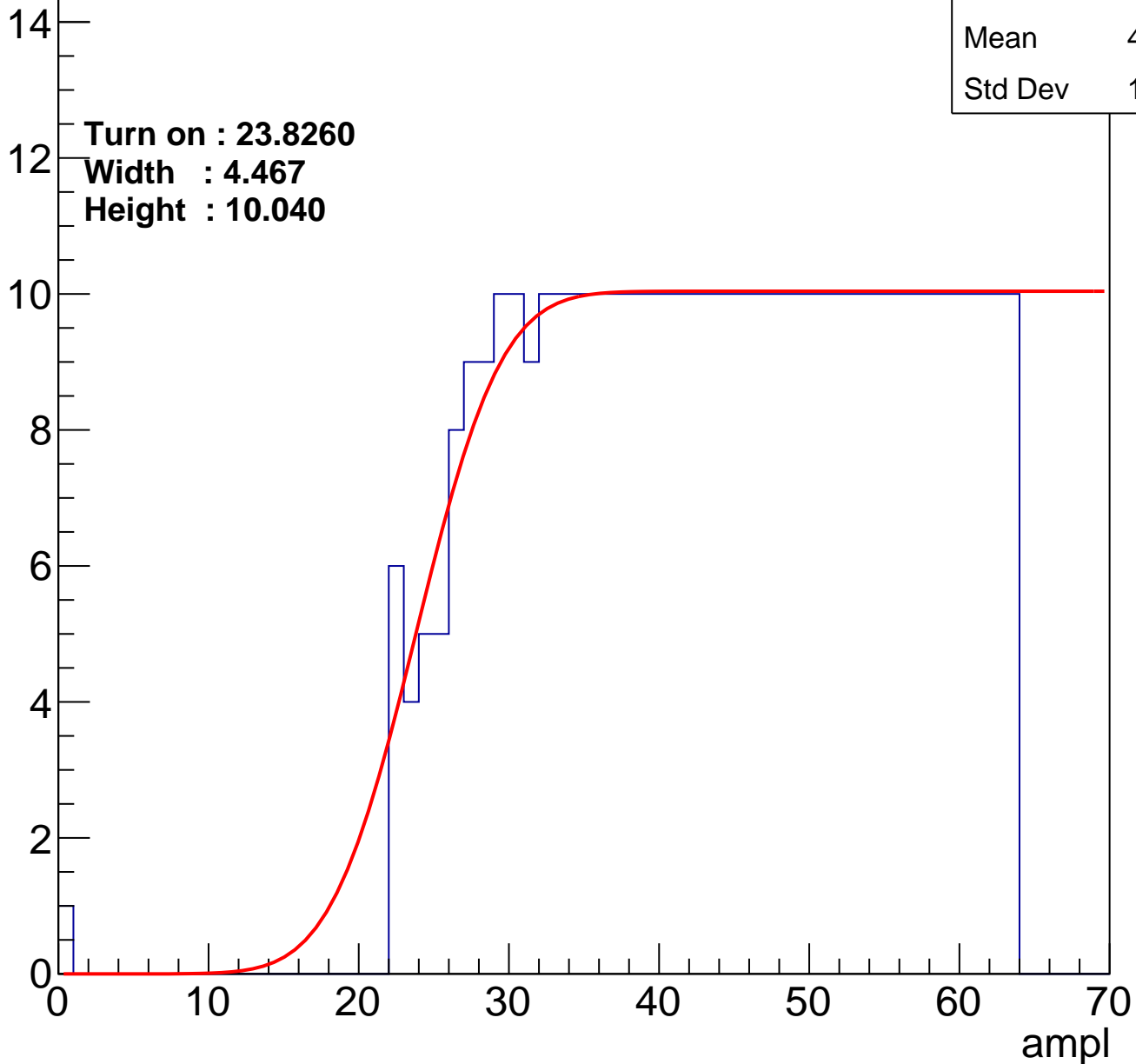
Entries	396
Mean	43.54
Std Dev	11.76

Turn on : 23.8260

Width : 4.467

Height : 10.040

Entry



# B1L100S, U16-ch33

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	376
Mean	44.14
Std Dev	12.2

Turn on : 26.7646

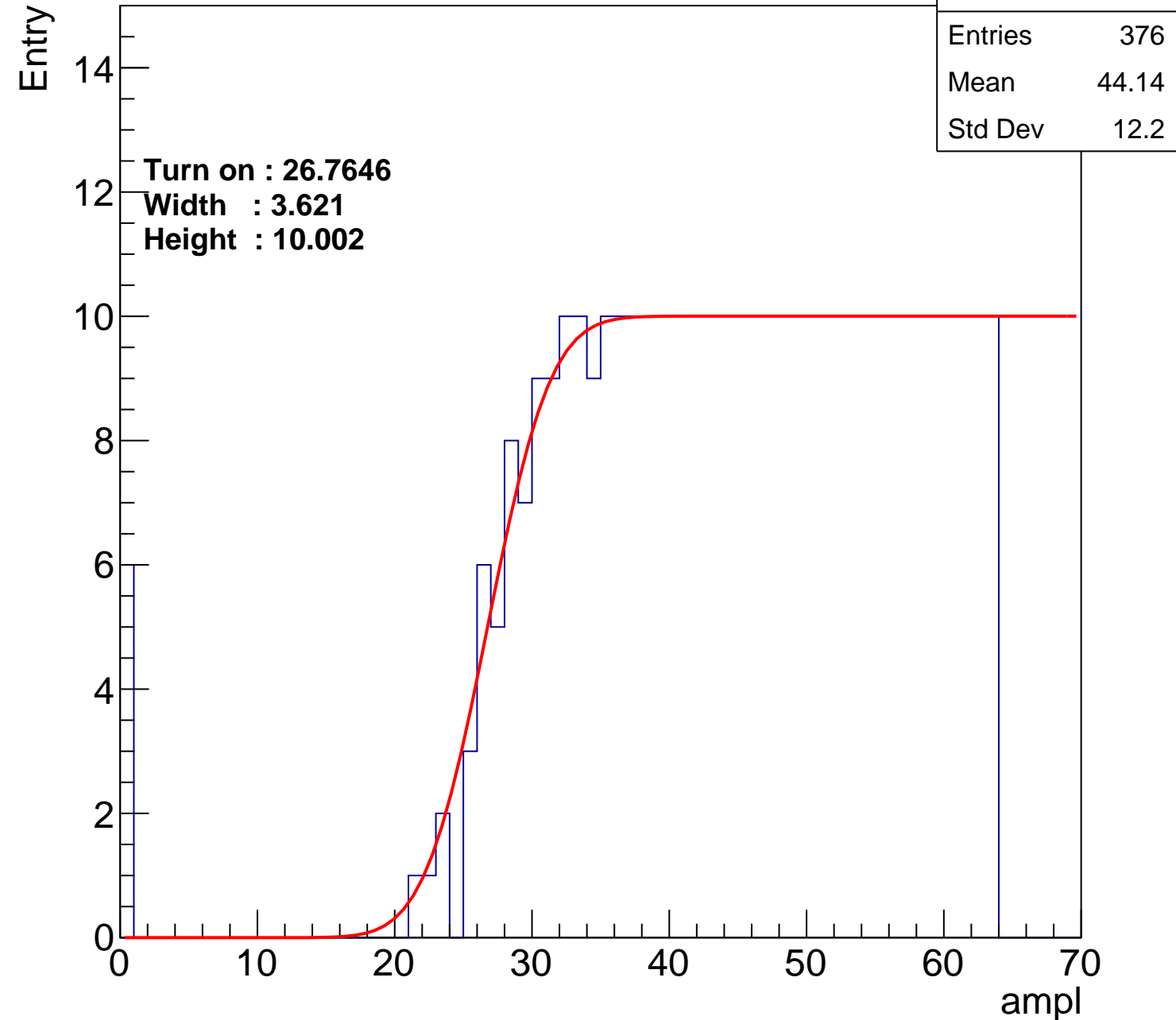
Width : 3.621

Height : 10.002

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch34

calib\_packv5\_042523\_0143.root, FC#4, port A2

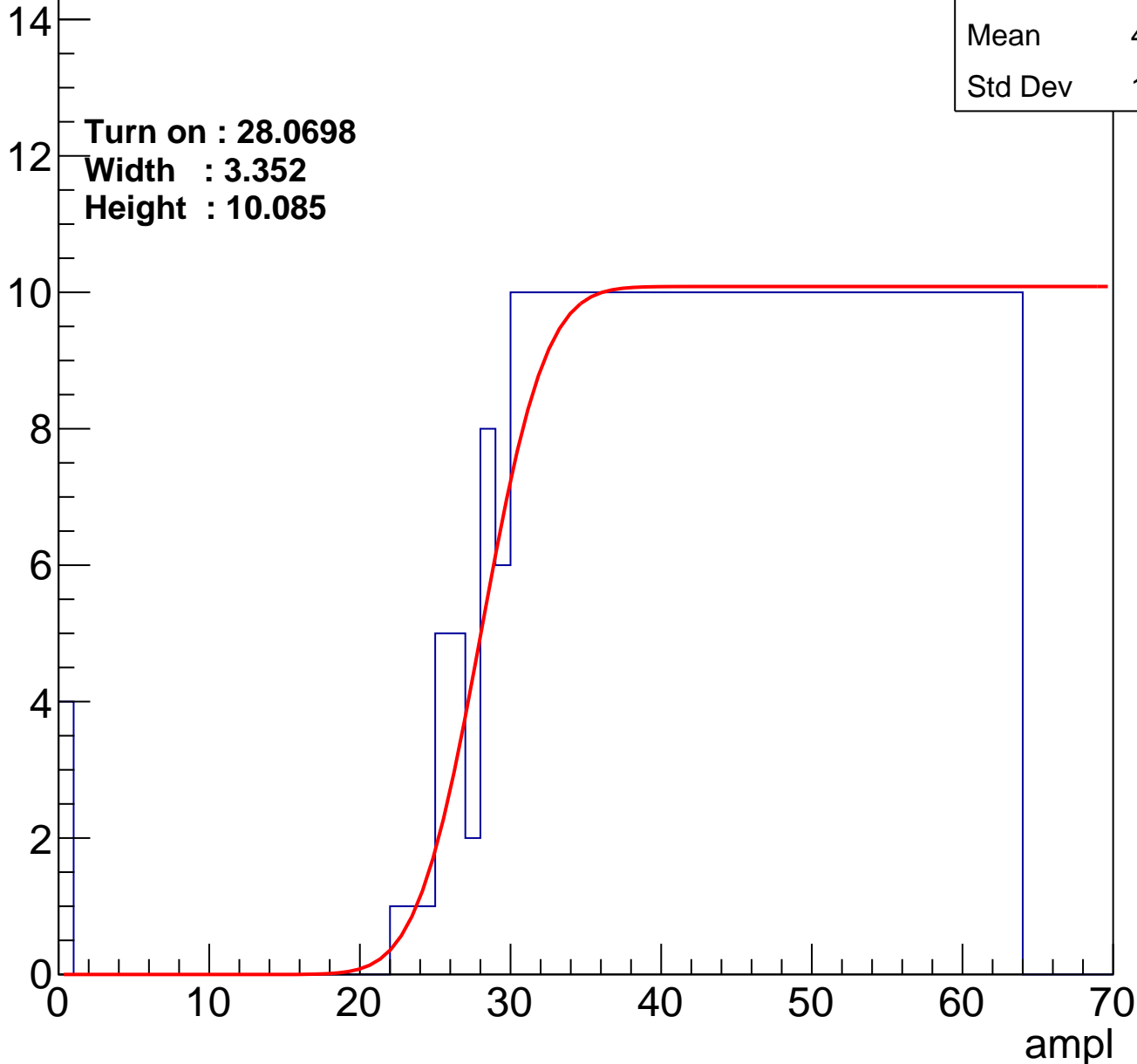
Entries	373
Mean	44.47
Std Dev	11.72

Turn on : 28.0698

Width : 3.352

Height : 10.085

Entry



# B1L100S, U16-ch35

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	384
Mean	43.83
Std Dev	12.19

Turn on : 26.3148

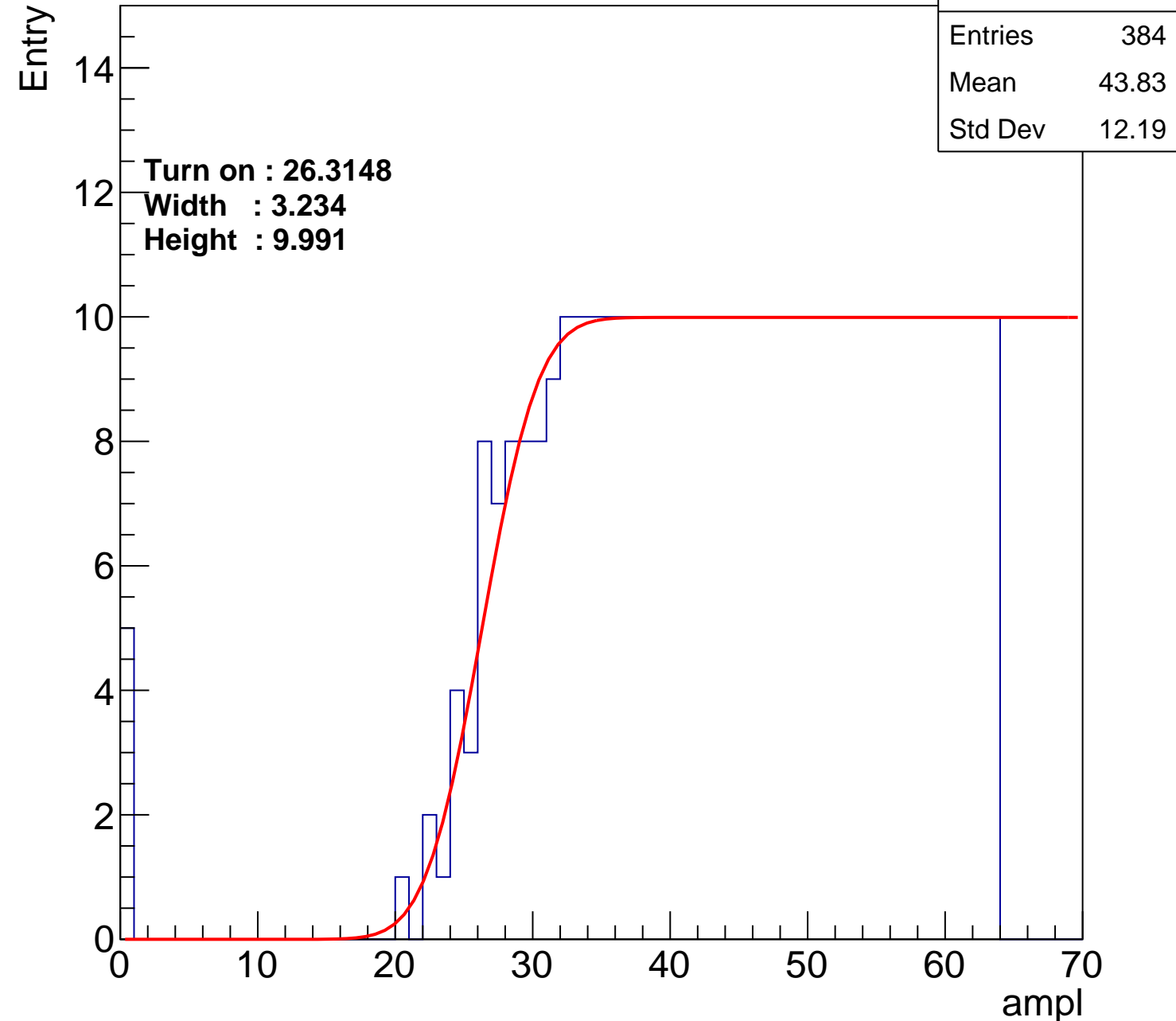
Width : 3.234

Height : 9.991

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch36

calib\_packv5\_042523\_0143.root, FC#4, port A2

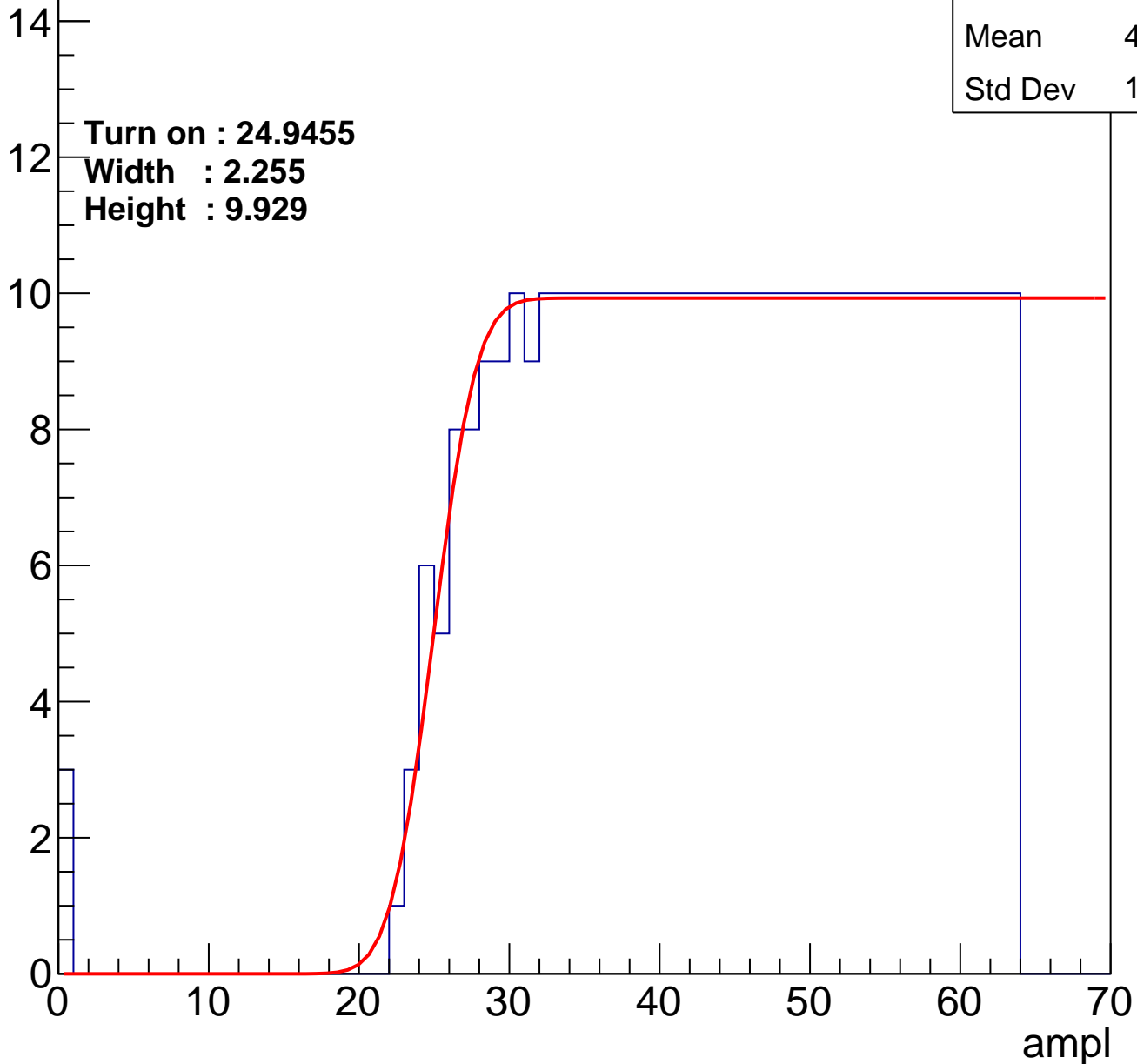
Entries	391
Mean	43.67
Std Dev	11.93

Turn on : 24.9455

Width : 2.255

Height : 9.929

Entry



# B1L100S, U16-ch37

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	376
Mean	44.49
Std Dev	11.36

Turn on : 26.3024

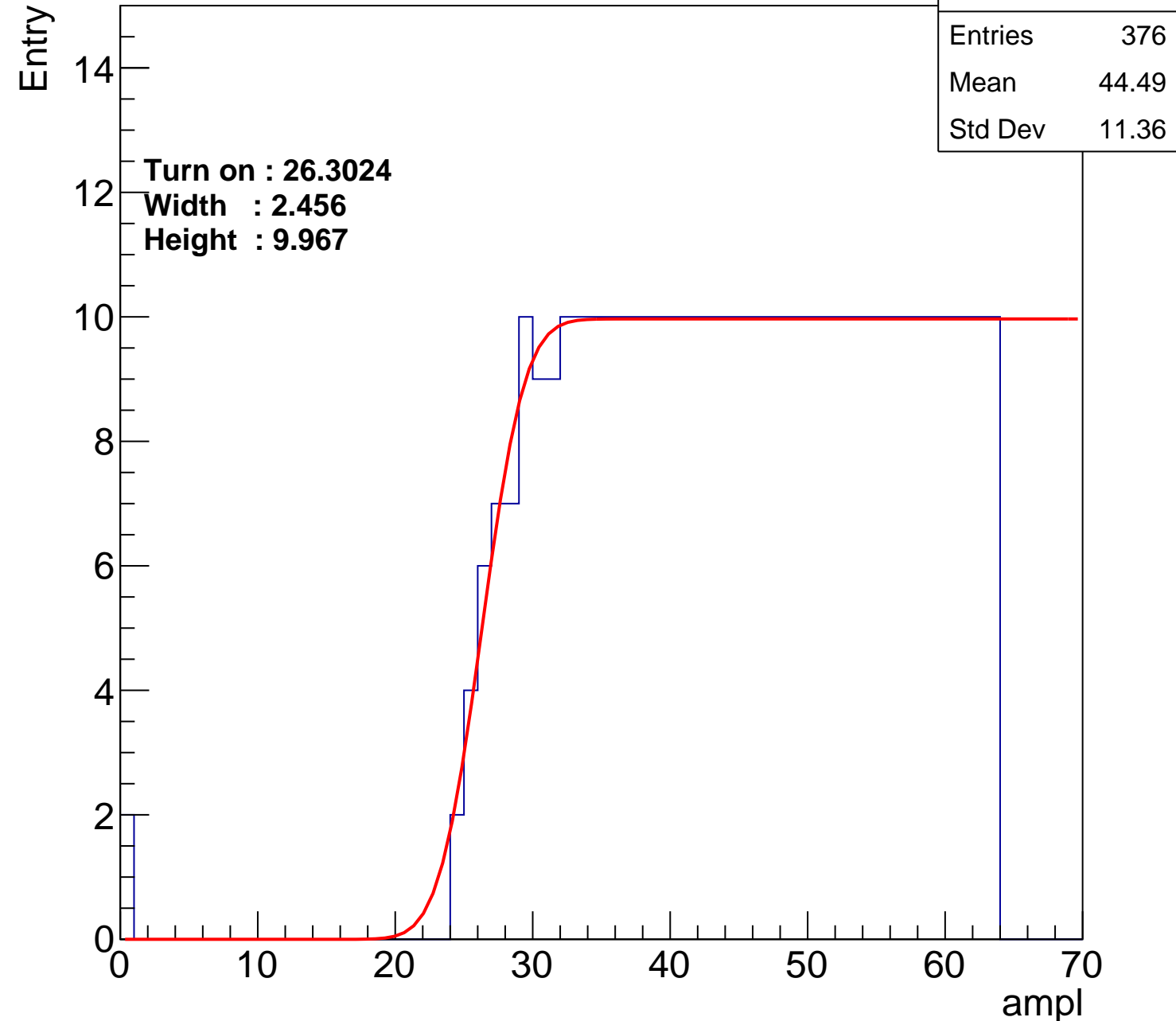
Width : 2.456

Height : 9.967

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch38

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	384
Mean	44.12
Std Dev	11.46

Turn on : 26.4191

Width : 2.880

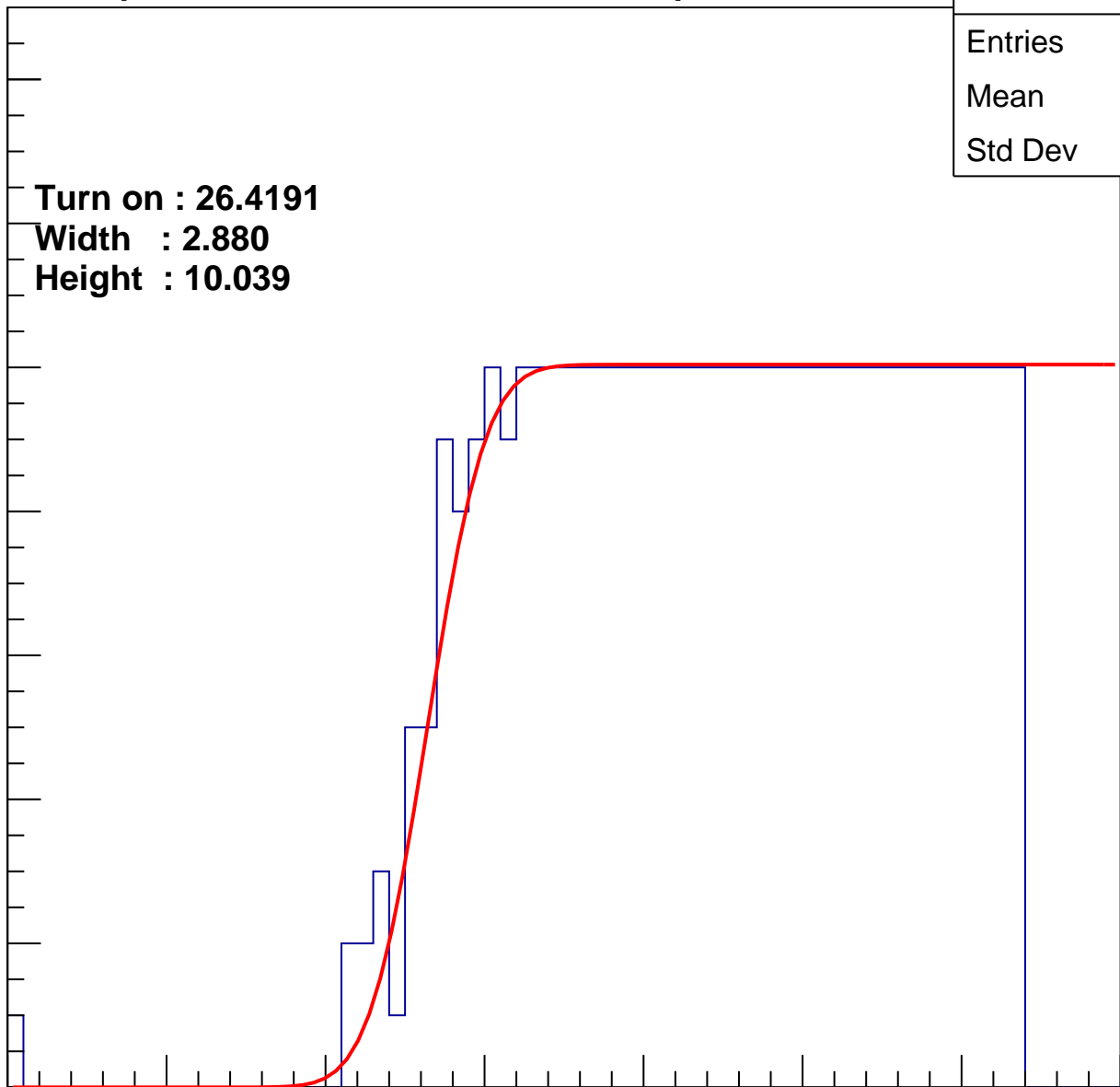
Height : 10.039

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70





# B1L100S, U16-ch39

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	372
Mean	44.65
Std Dev	11.32

Turn on : 27.4925

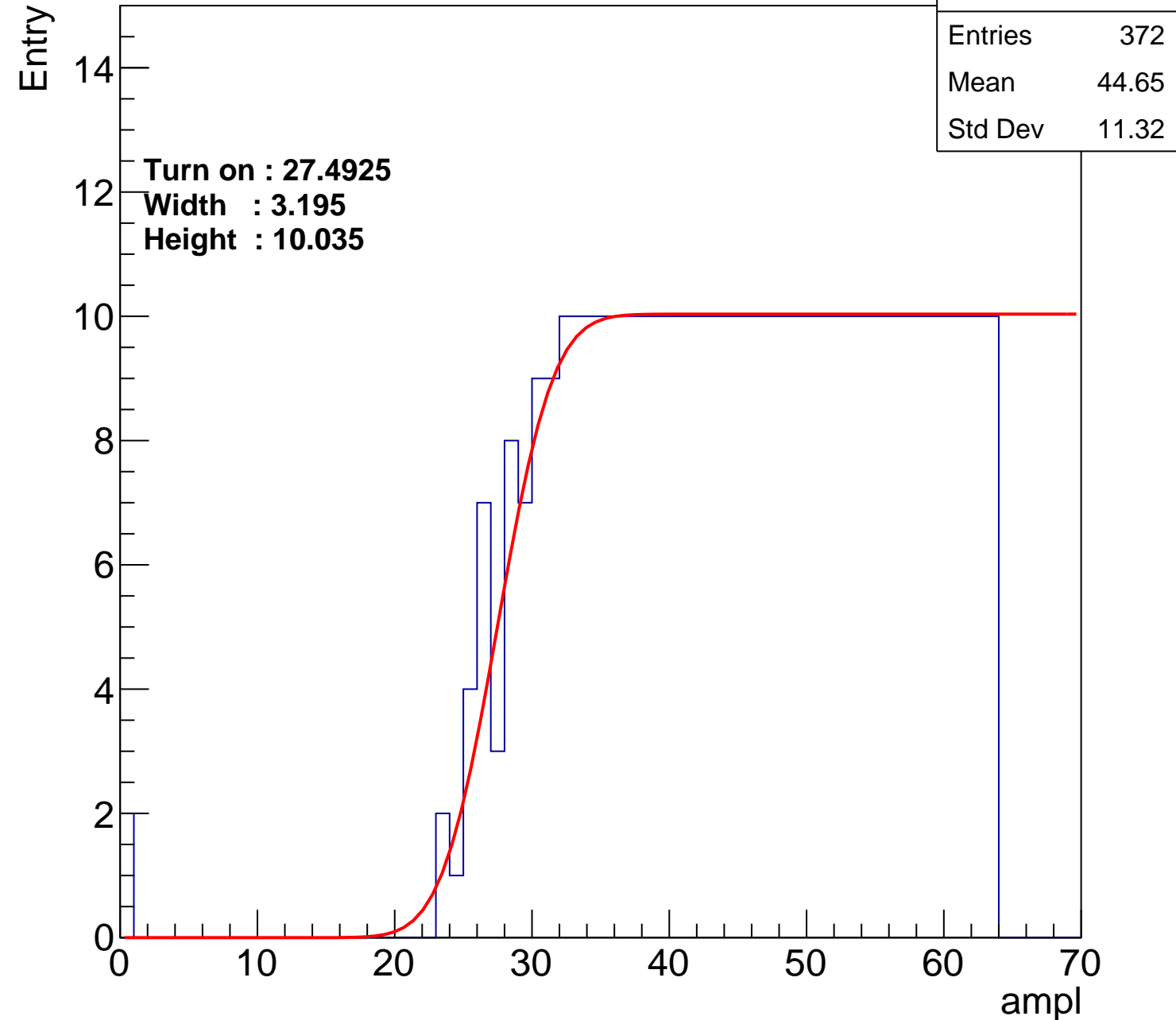
Width : 3.195

Height : 10.035

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch40

calib\_packv5\_042523\_0143.root, FC#4, port A2

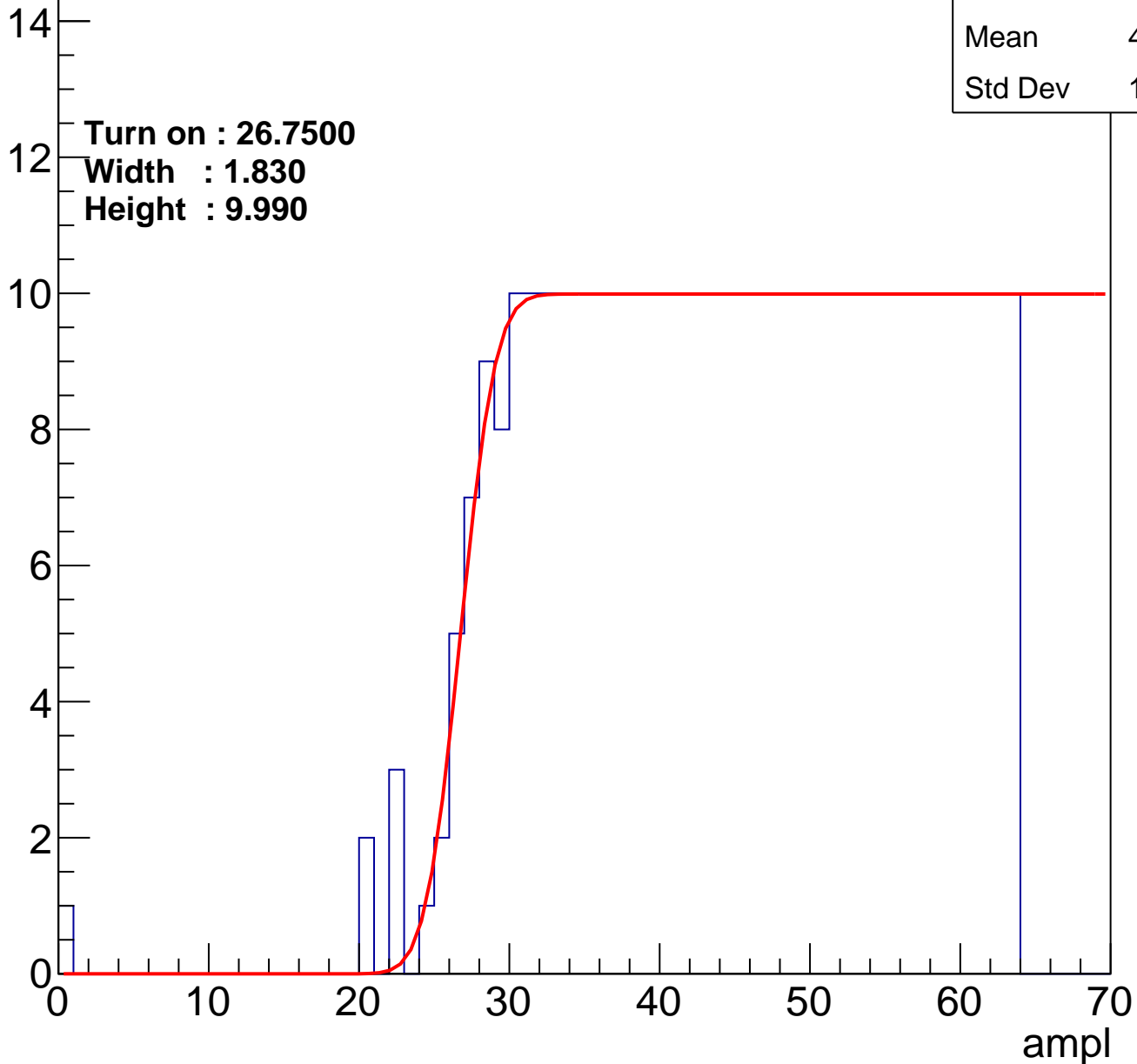
Entries	378
Mean	44.43
Std Dev	11.29

**Turn on : 26.7500**

**Width : 1.830**

**Height : 9.990**

Entry



# B1L100S, U16-ch41

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	378
Mean	44.23
Std Dev	11.82

**Turn on : 26.7562**

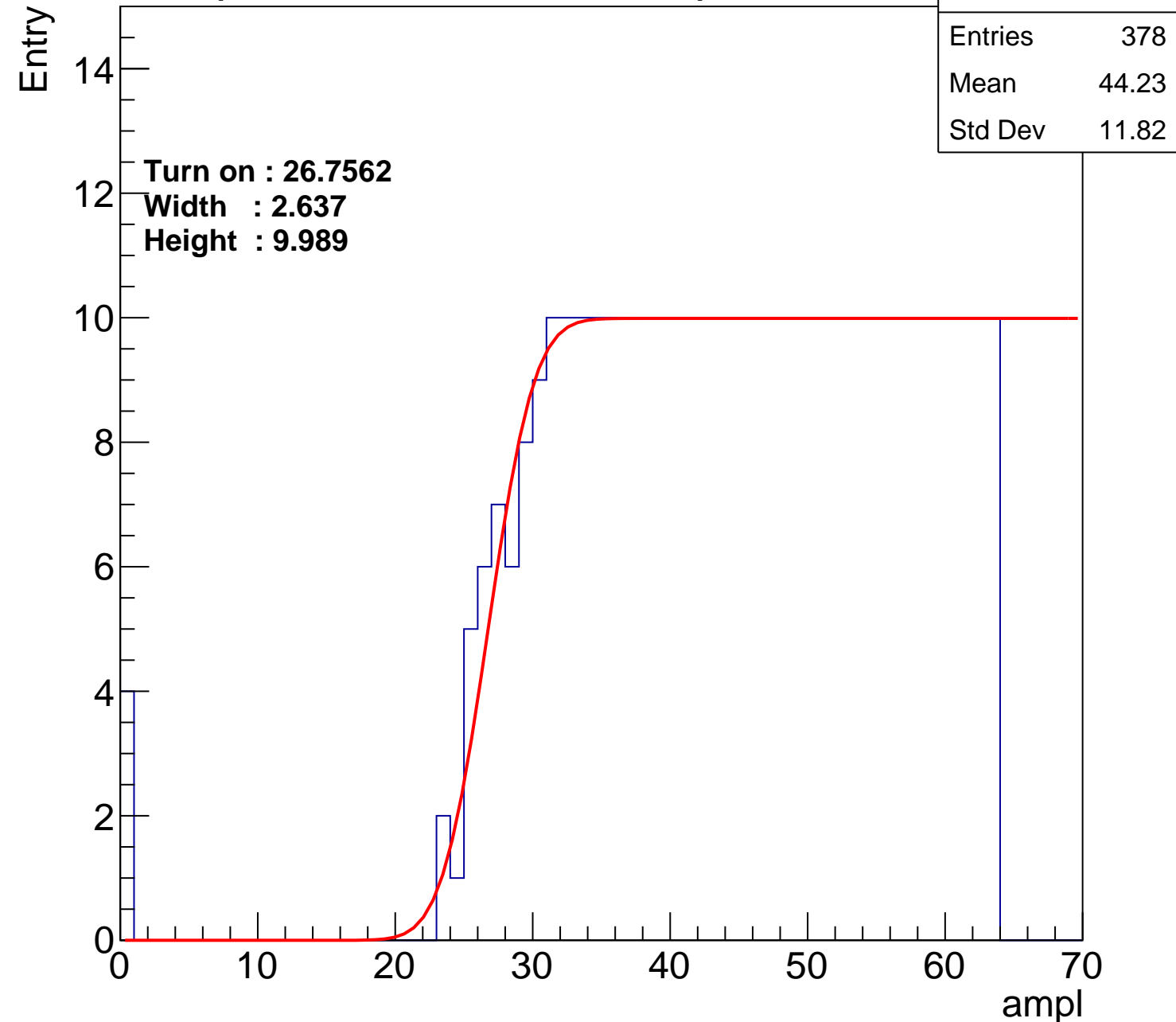
**Width : 2.637**

**Height : 9.989**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch42

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	375
Mean	44.45
Std Dev	11.49

Turn on : 27.1182

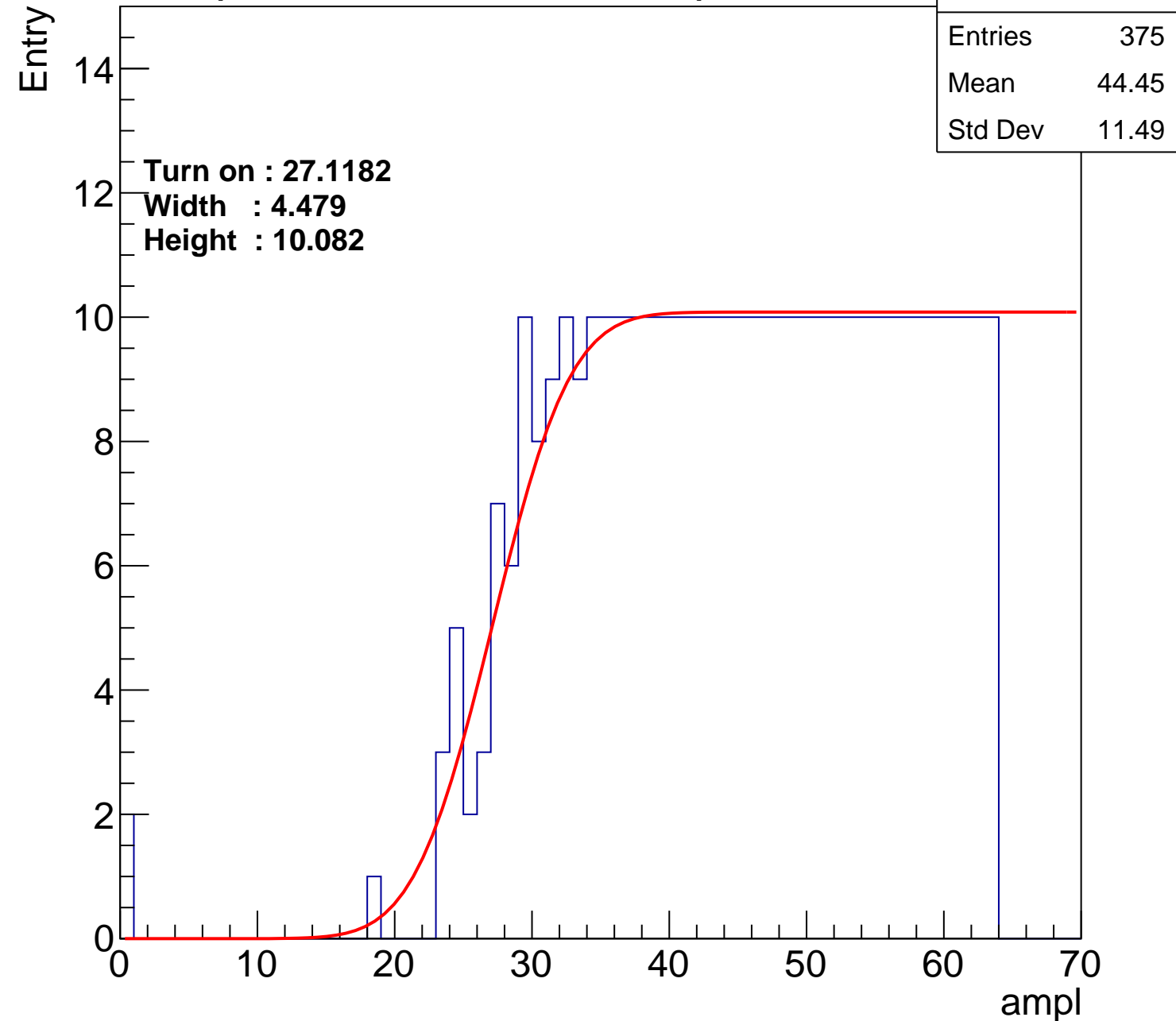
Width : 4.479

Height : 10.082

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch43

calib\_packv5\_042523\_0143.root, FC#4, port A2

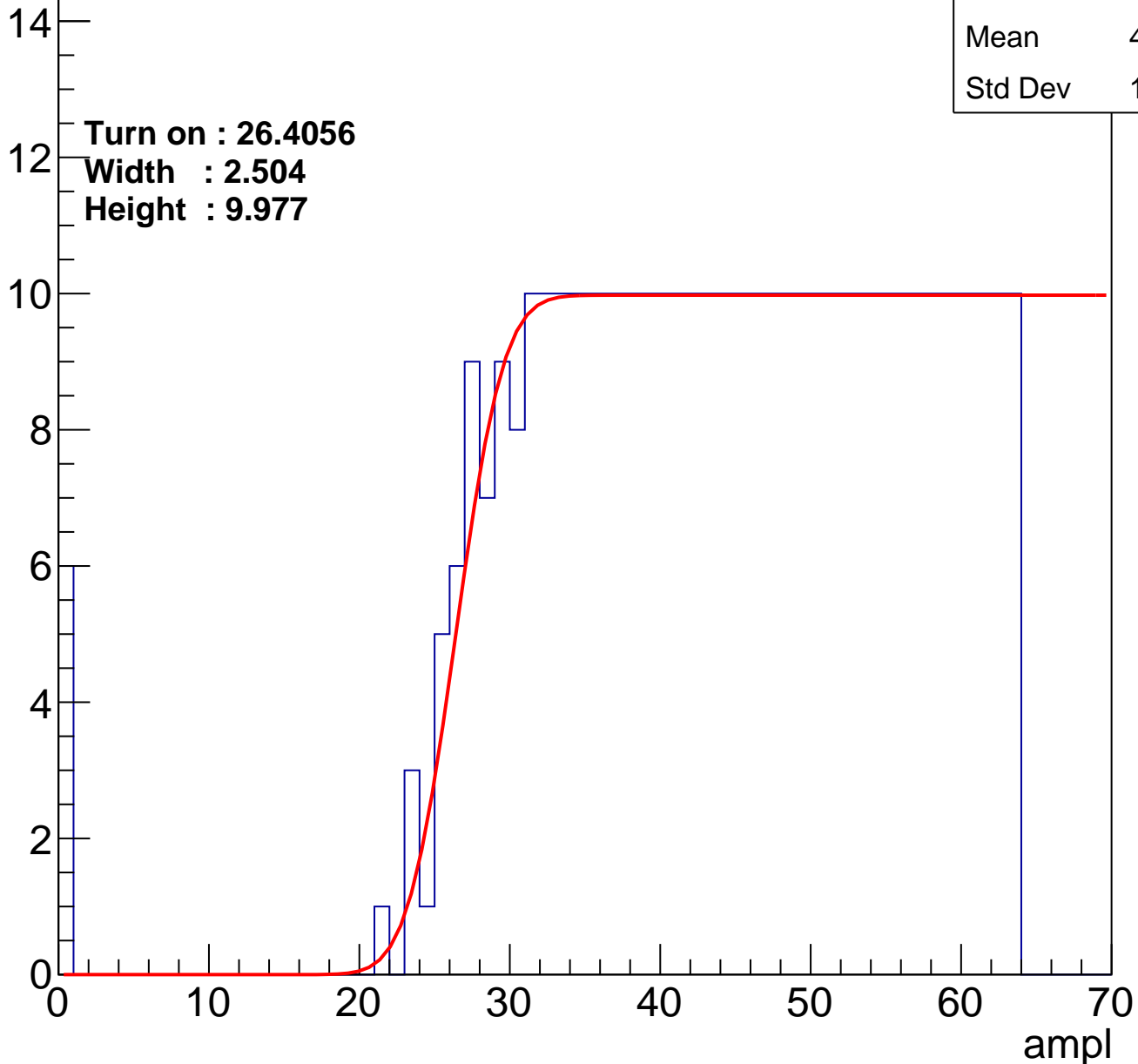
Entries	385
Mean	43.75
Std Dev	12.32

Turn on : 26.4056

Width : 2.504

Height : 9.977

Entry



# B1L100S, U16-ch44

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	377
Mean	44.37
Std Dev	11.59

Turn on : 26.6714

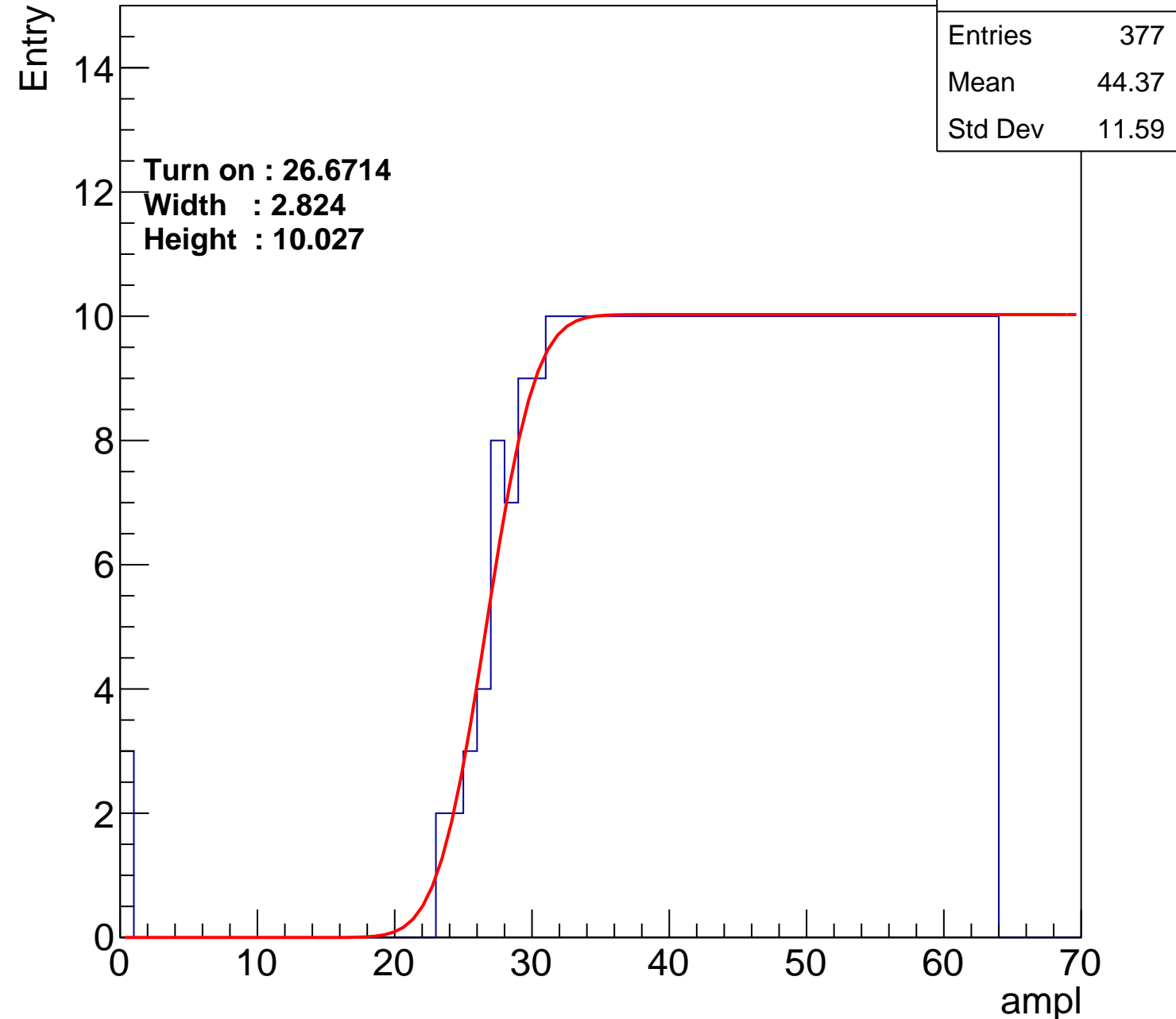
Width : 2.824

Height : 10.027

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch45

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	375
Mean	44.51
Std Dev	11.39

**Turn on : 26.9464**

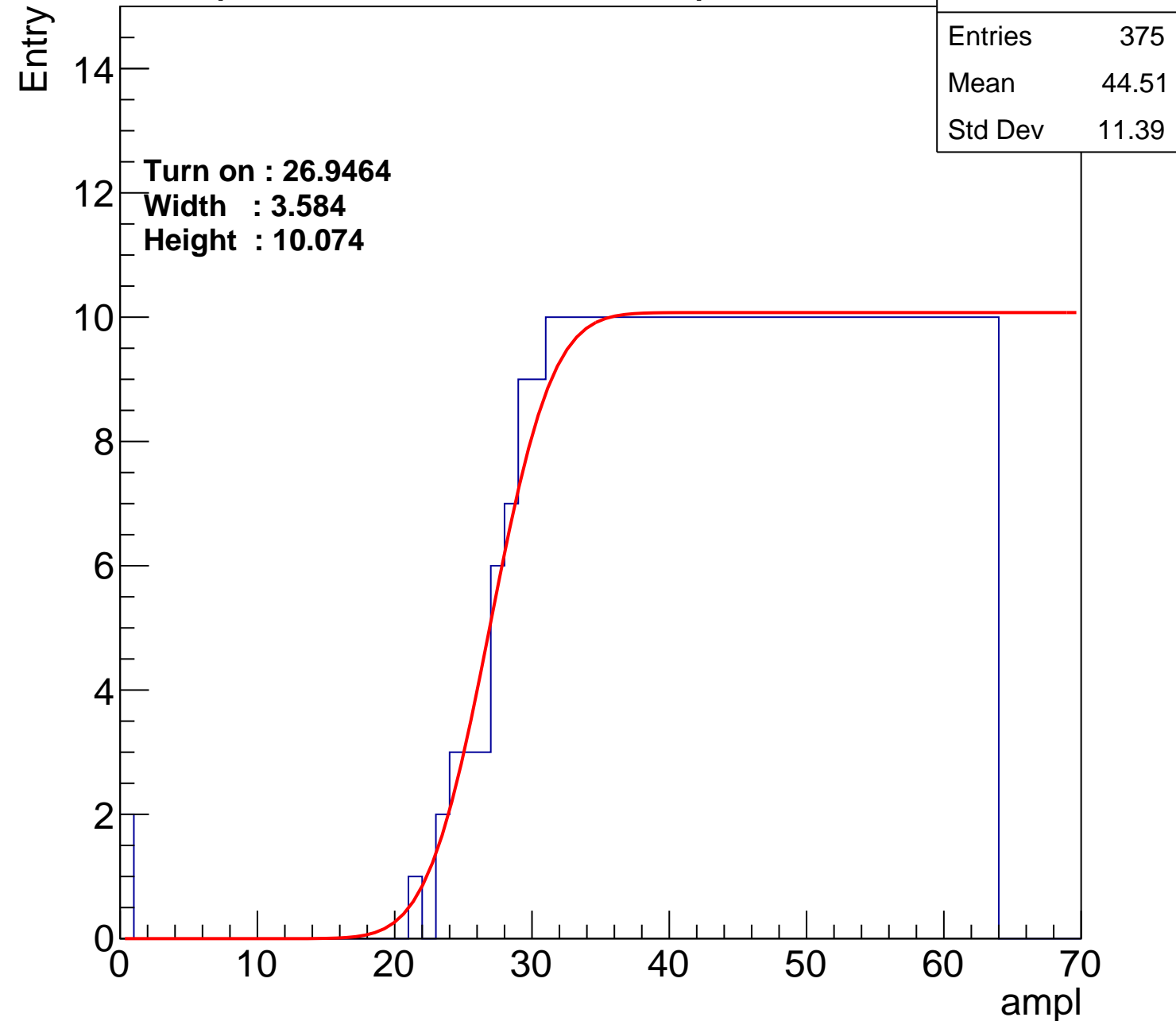
**Width : 3.584**

**Height : 10.074**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch46

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	418
Mean	42.41
Std Dev	12.47

Turn on : 22.5818

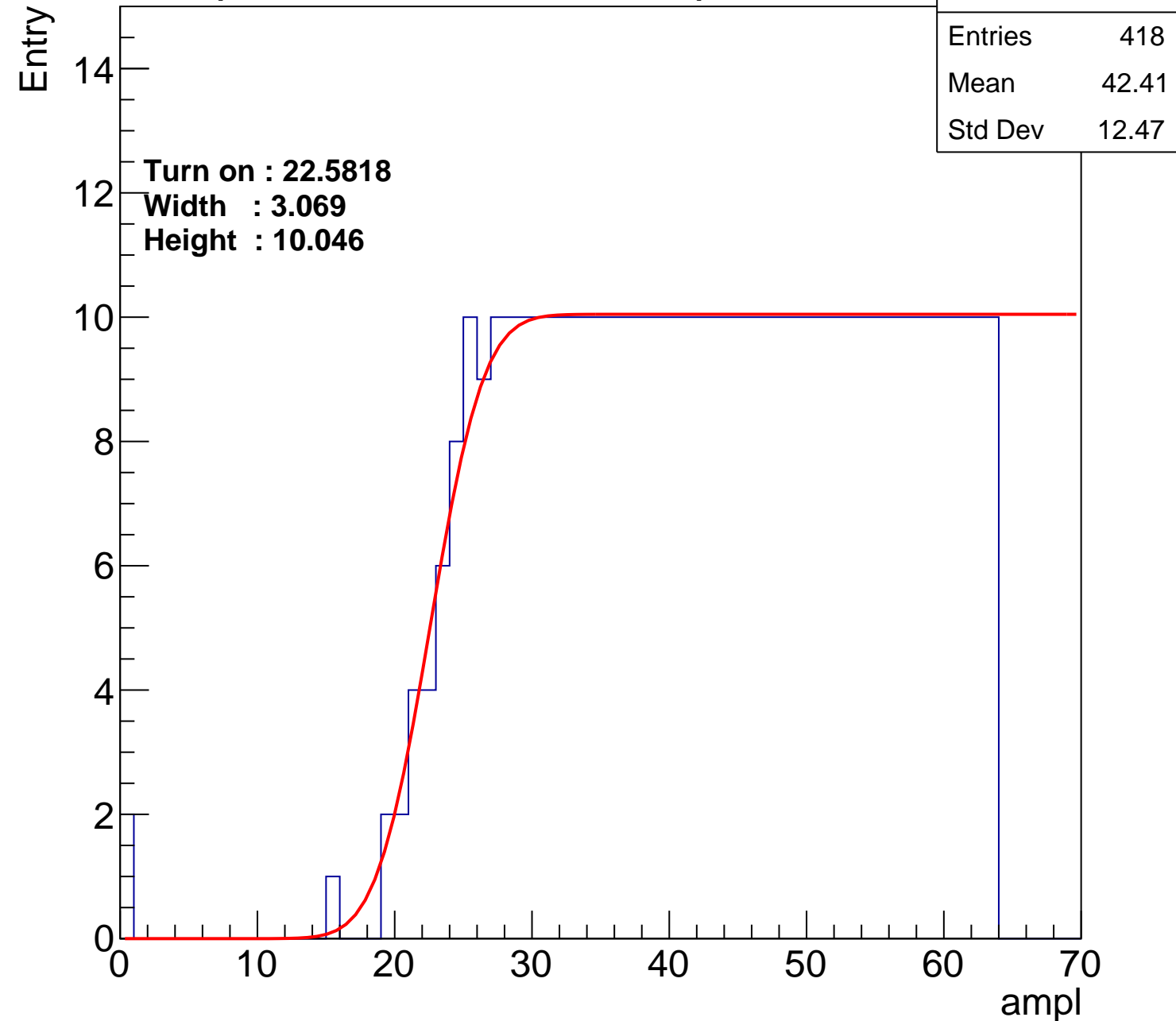
Width : 3.069

Height : 10.046

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L100S, U16-ch47

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	367
Mean	44.96
Std Dev	11

Turn on : 27.4569

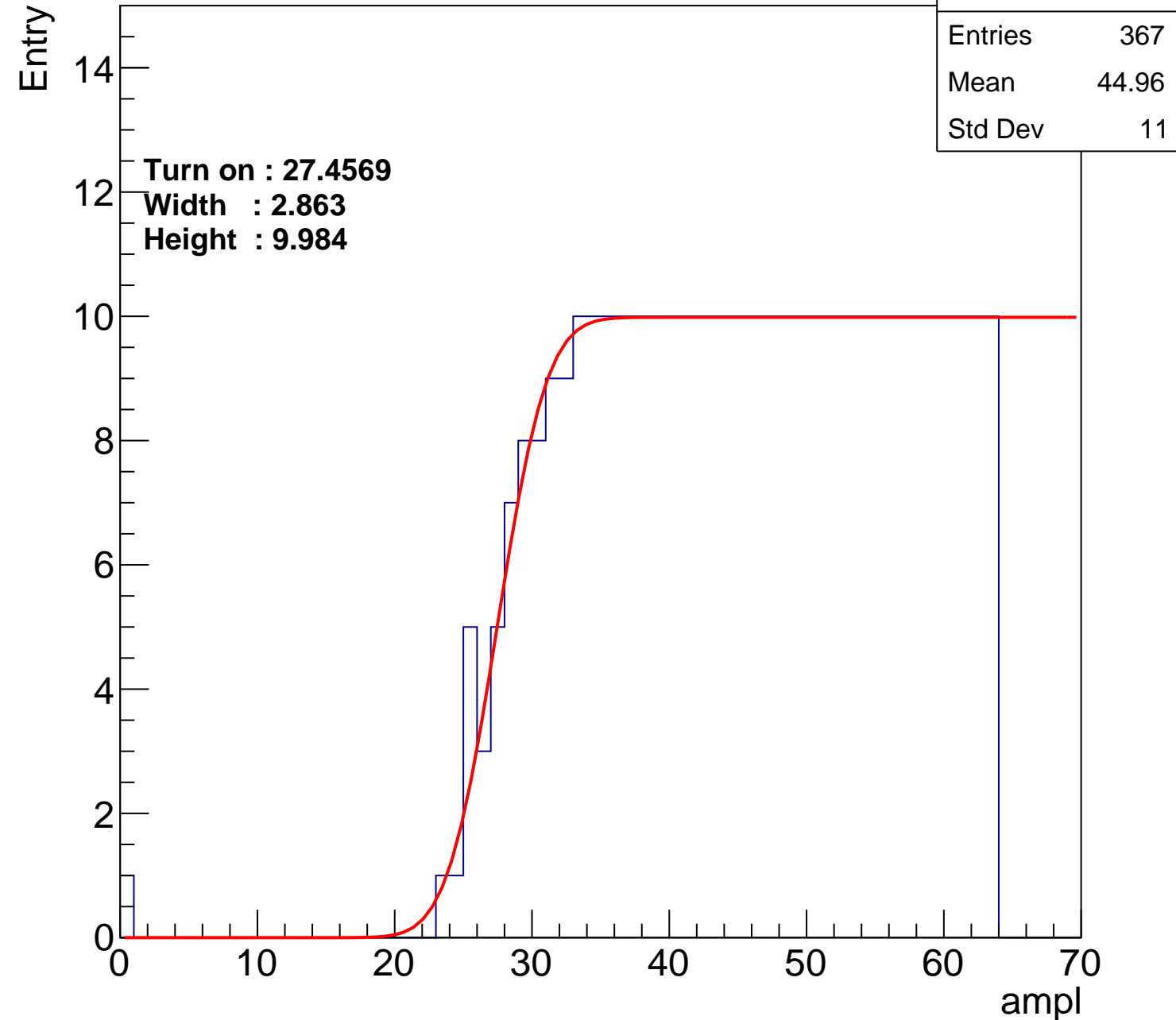
Width : 2.863

Height : 9.984

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch48

calib\_packv5\_042523\_0143.root, FC#4, port A2

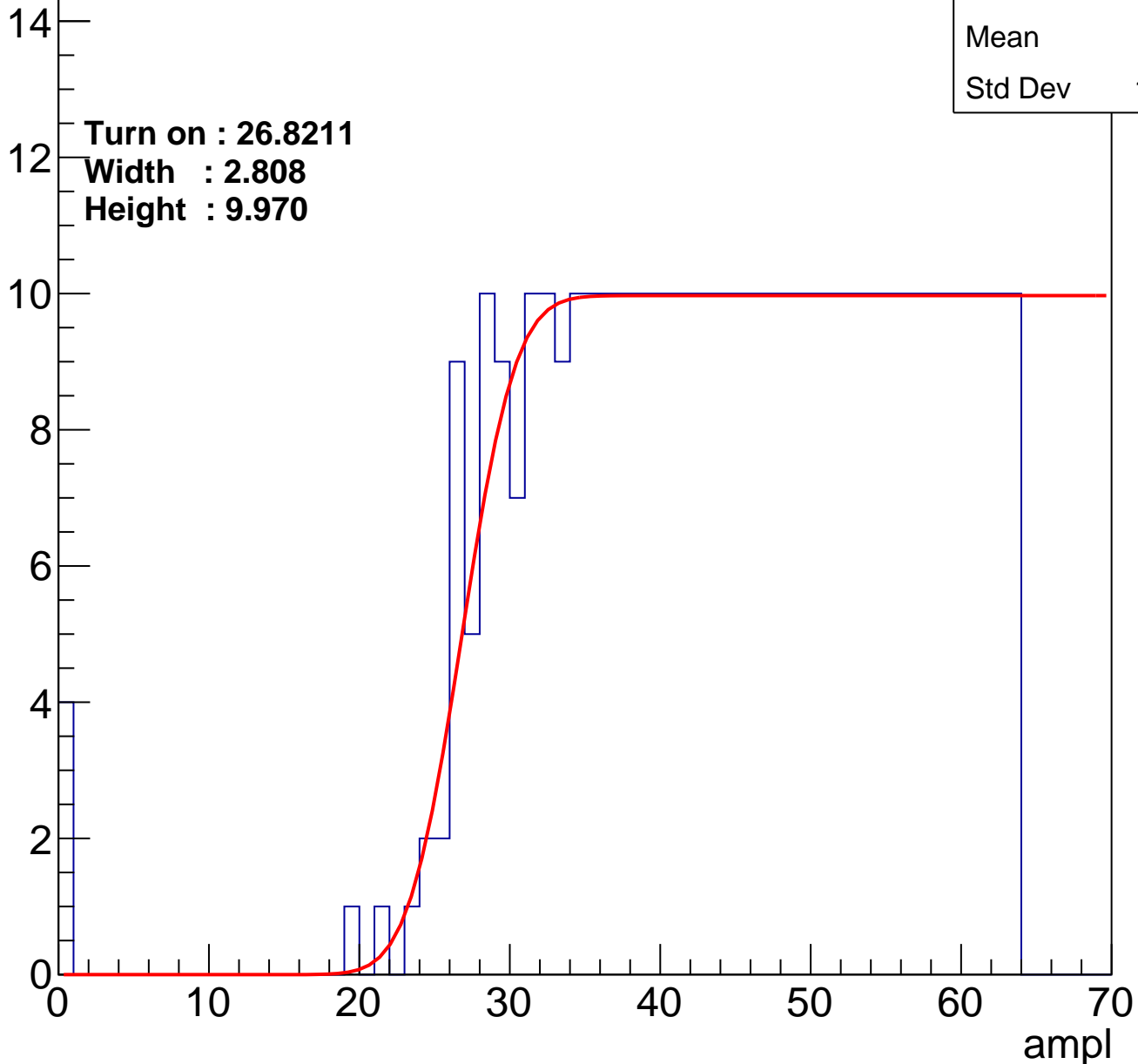
Entries	380
Mean	44.1
Std Dev	11.91

Turn on : 26.8211

Width : 2.808

Height : 9.970

Entry



# B1L100S, U16-ch49

calib\_packv5\_042523\_0143.root, FC#4, port A2

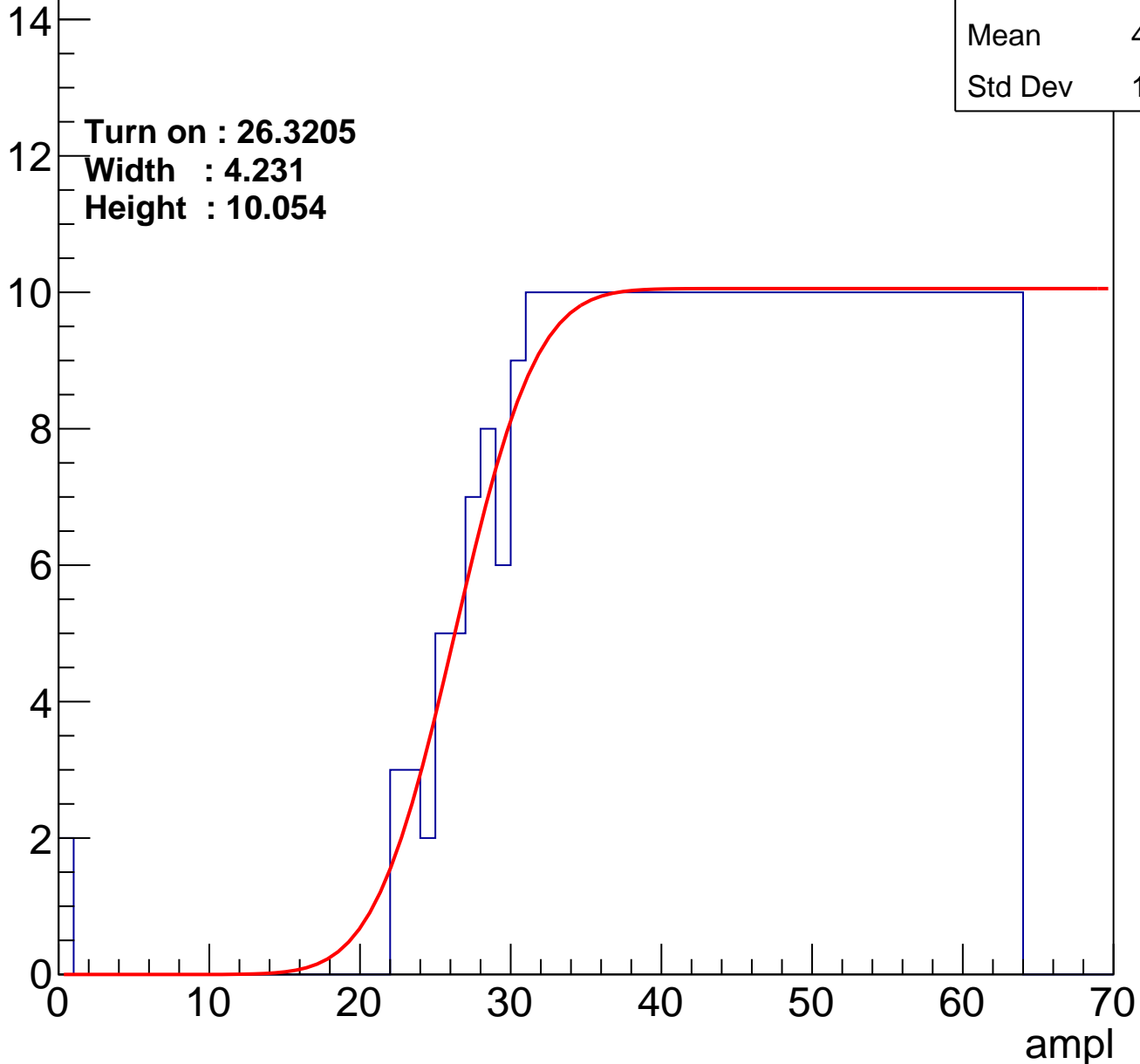
Entries	380
Mean	44.22
Std Dev	11.58

Turn on : 26.3205

Width : 4.231

Height : 10.054

Entry



# B1L100S, U16-ch50

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	397
Mean	43.32
Std Dev	12.18

Turn on : 24.7493

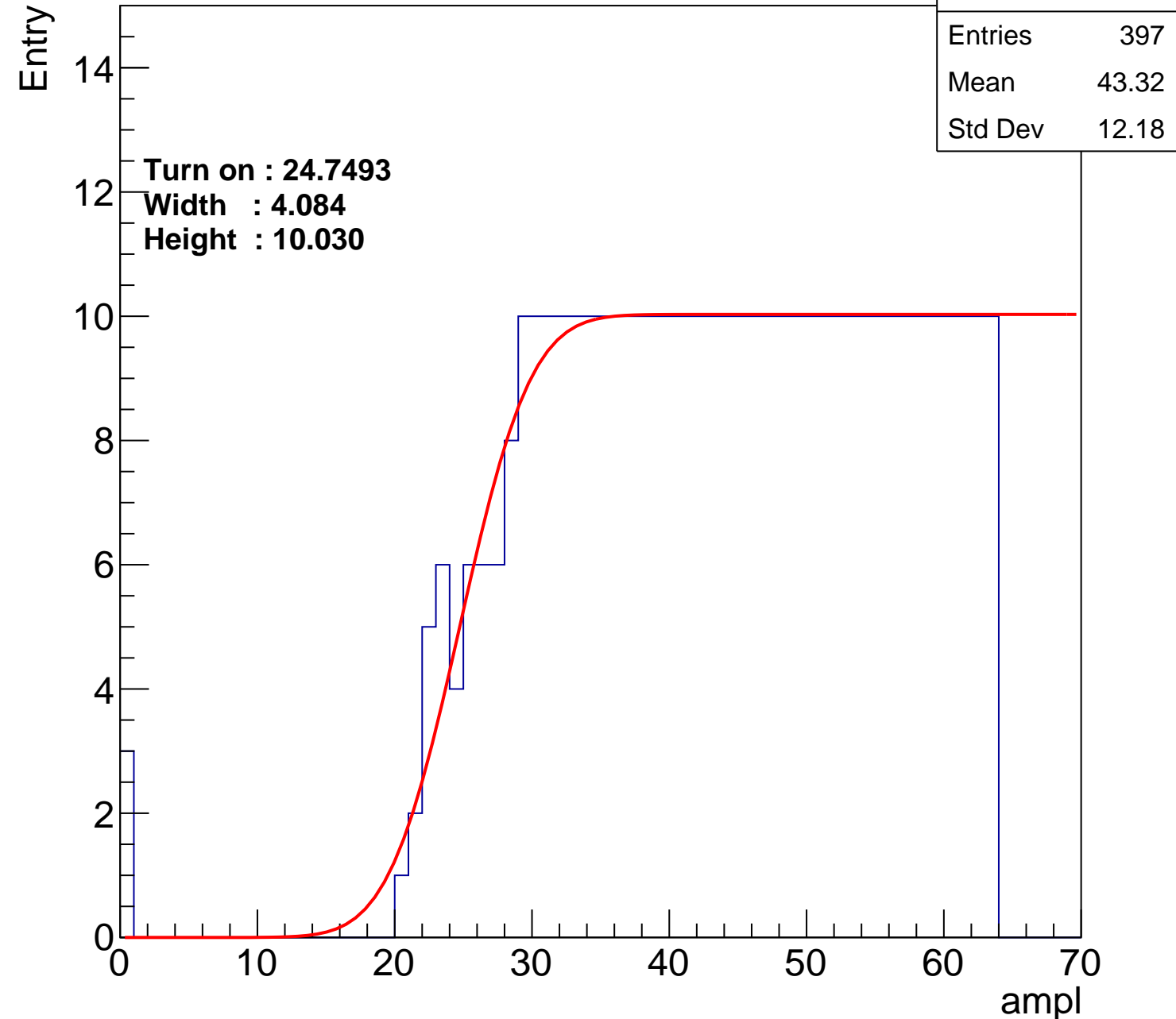
Width : 4.084

Height : 10.030

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch51

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	377
Mean	44.37
Std Dev	11.51

Turn on : 26.9491

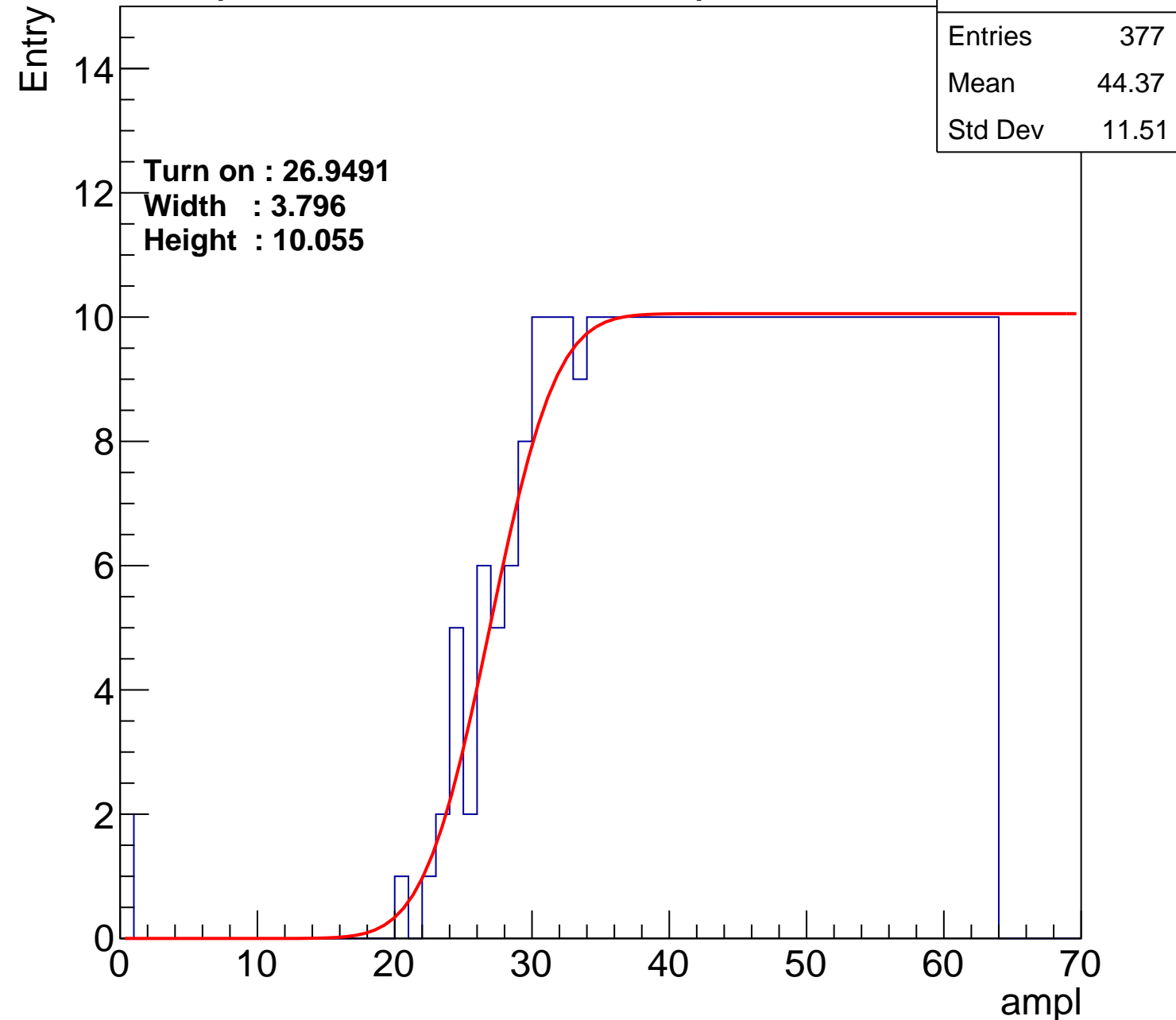
Width : 3.796

Height : 10.055

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch52

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	389
Mean	43.73
Std Dev	11.96

Turn on : 24.9659

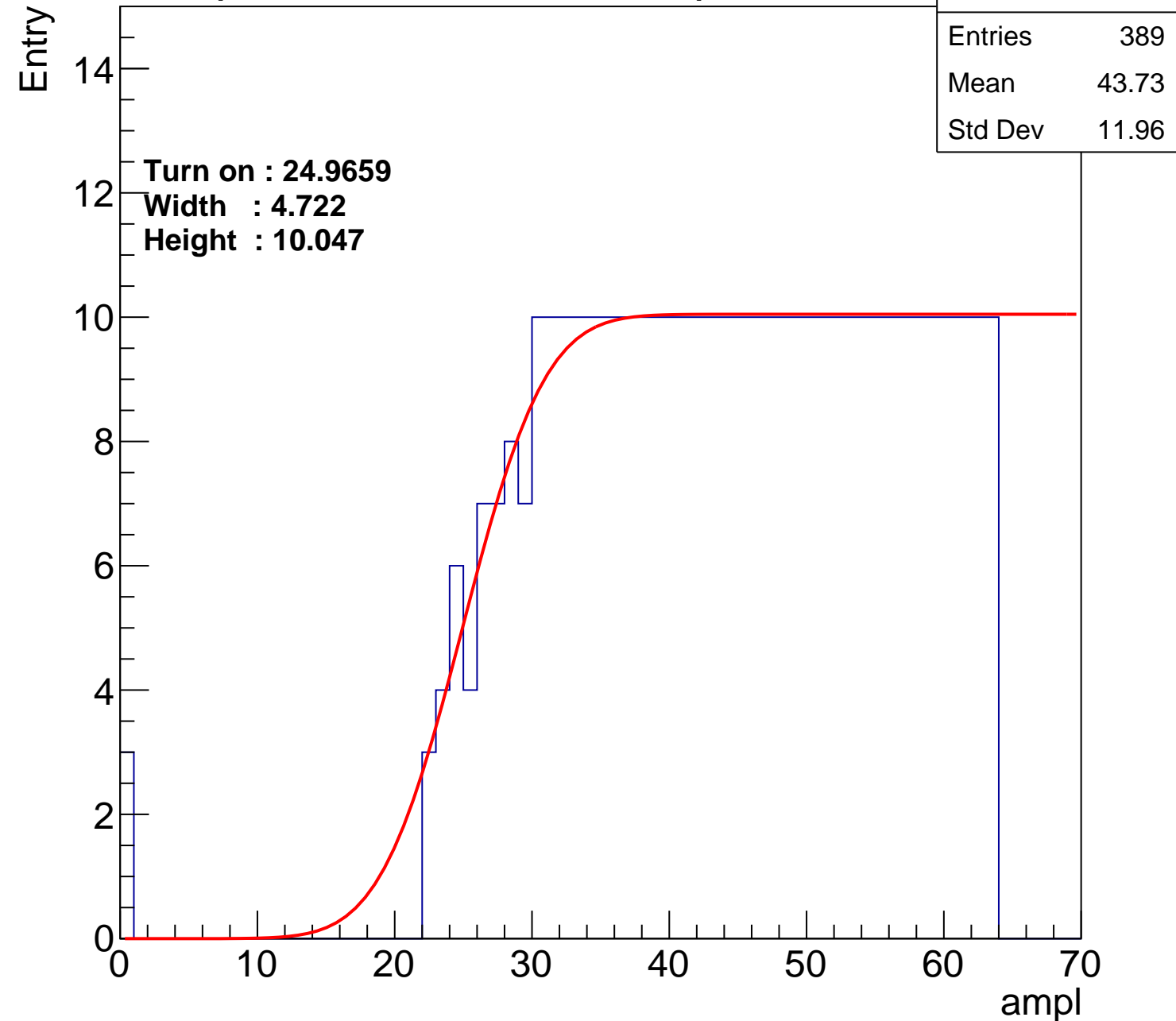
Width : 4.722

Height : 10.047

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch53

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	386
Mean	44.04
Std Dev	11.49

Turn on : 25.6523

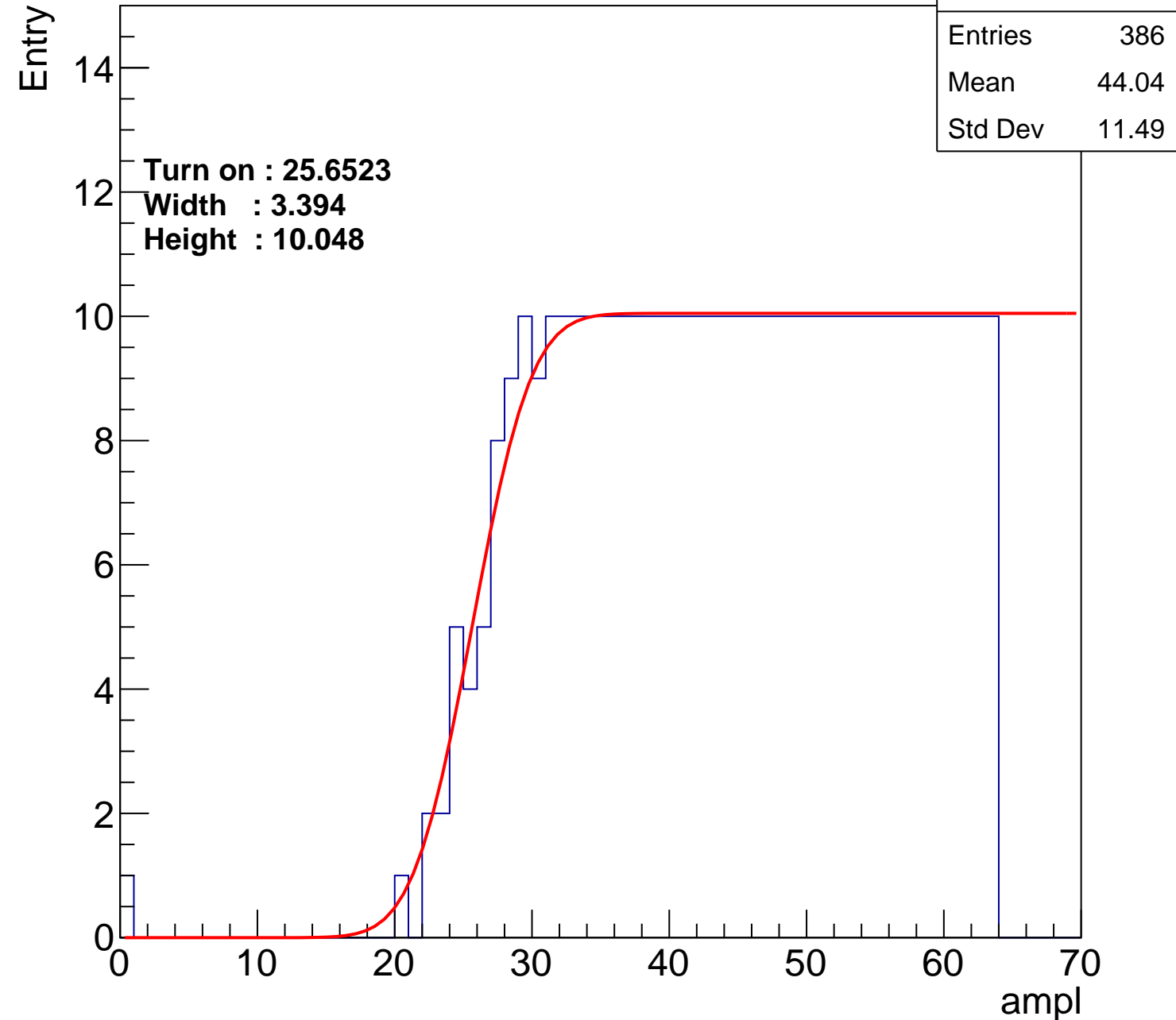
Width : 3.394

Height : 10.048

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch54

calib\_packv5\_042523\_0143.root, FC#4, port A2

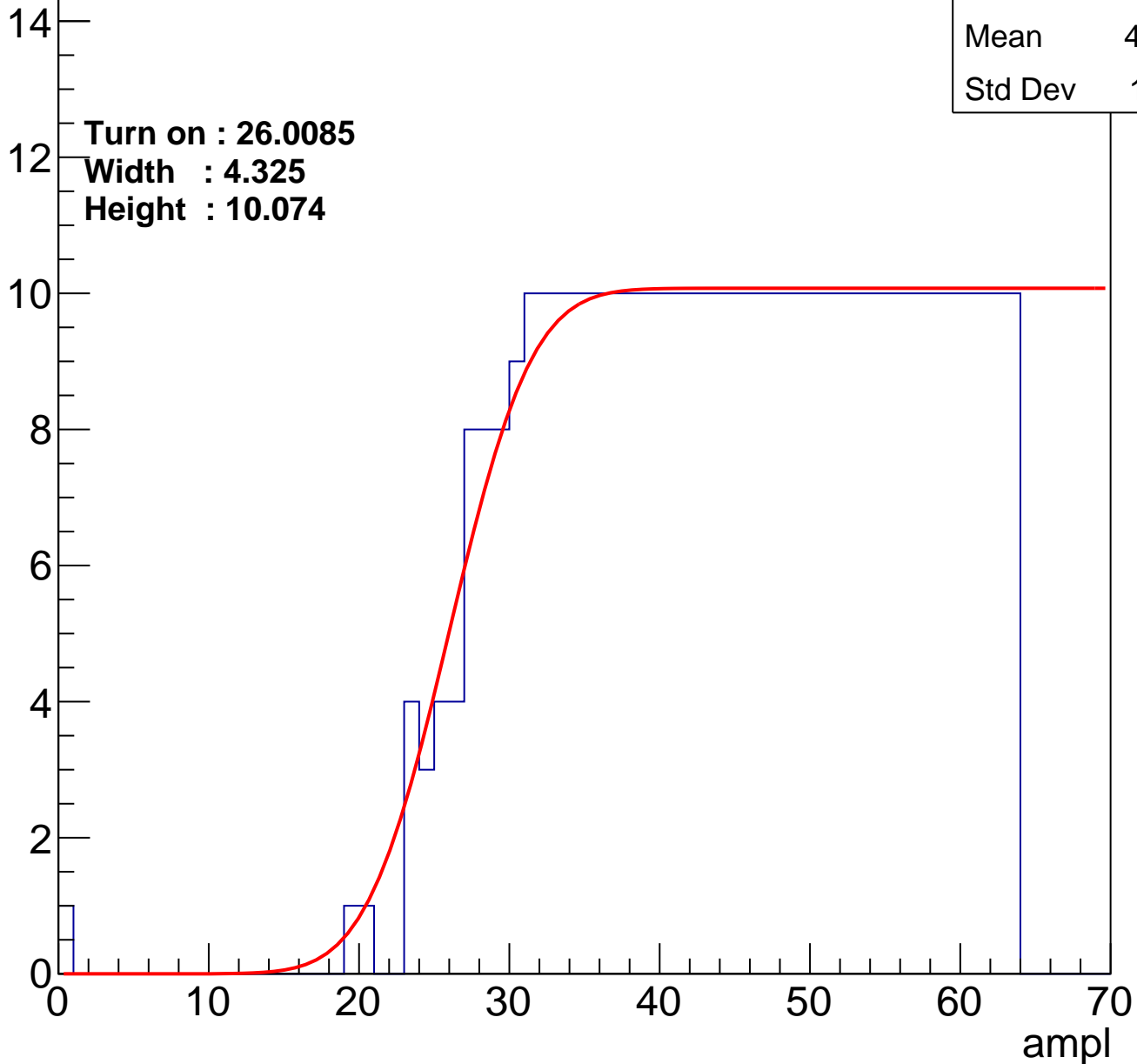
Entries	381
Mean	44.25
Std Dev	11.41

Turn on : 26.0085

Width : 4.325

Height : 10.074

Entry





# B1L100S, U16-ch55

calib\_packv5\_042523\_0143.root, FC#4, port A2

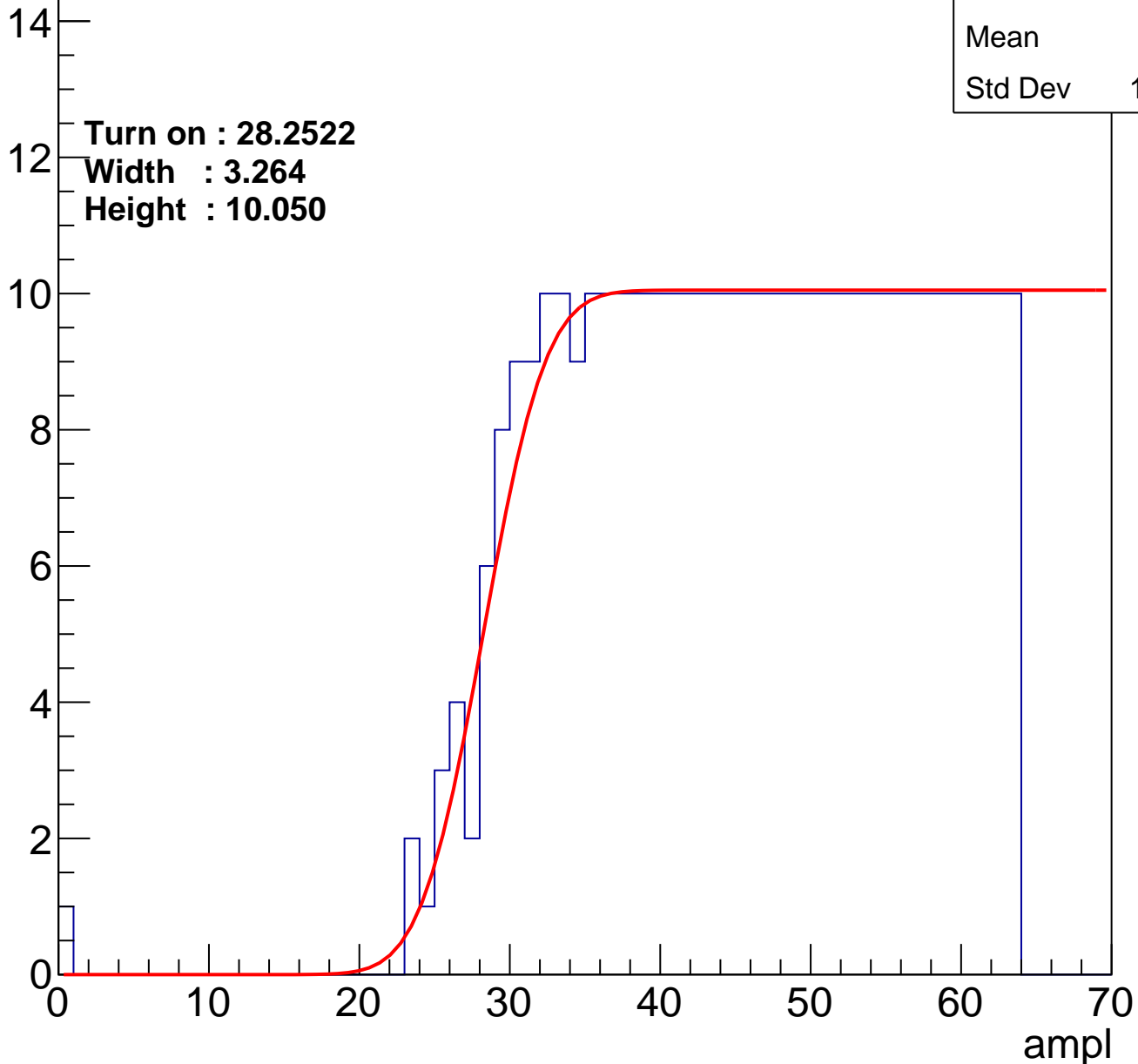
Entries	364
Mean	45.1
Std Dev	10.93

Turn on : 28.2522

Width : 3.264

Height : 10.050

Entry



# B1L100S, U16-ch56

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	377
Mean	44.46
Std Dev	11.28

Turn on : 26.4561

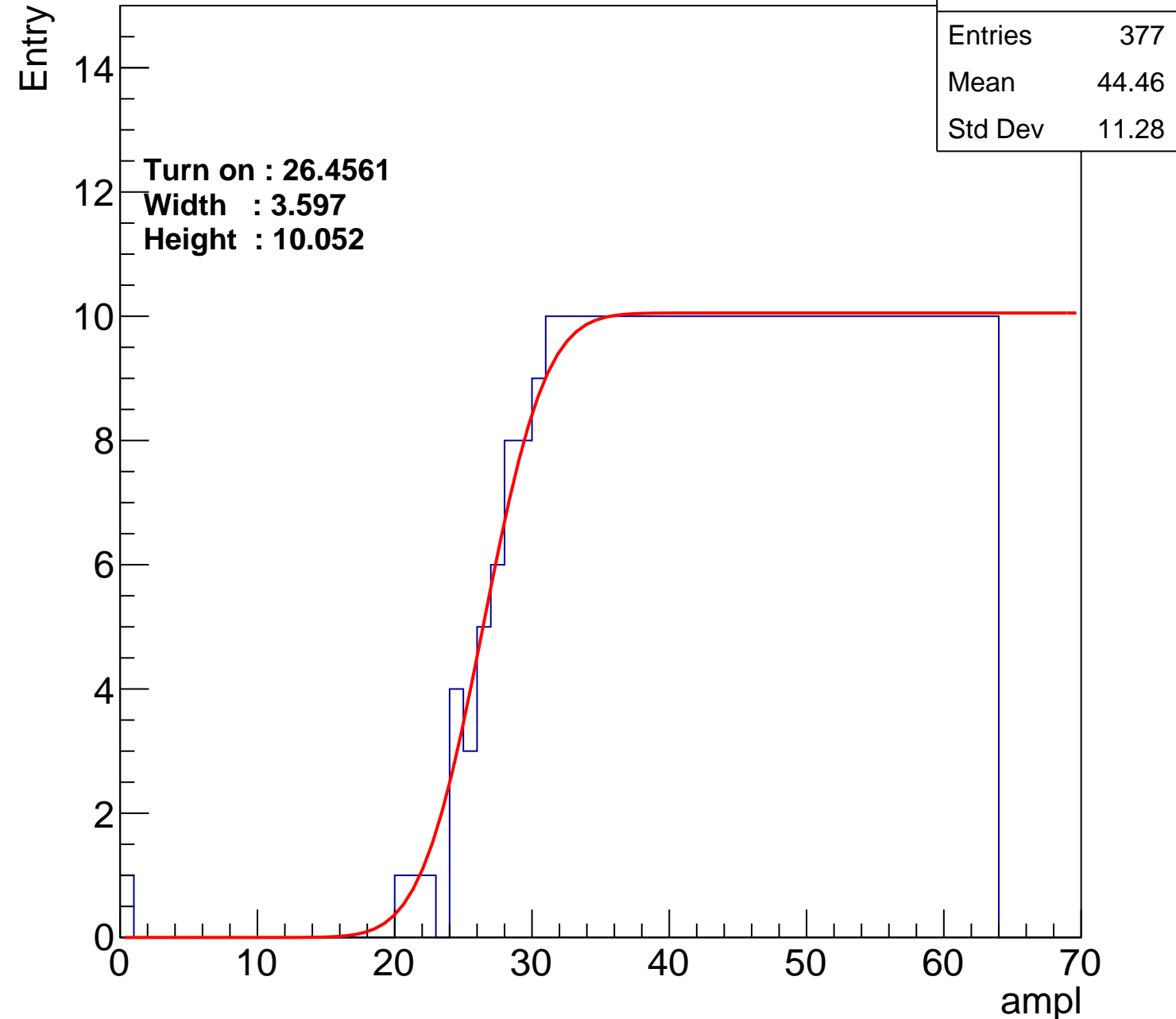
Width : 3.597

Height : 10.052

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch57

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	393
Mean	43.43
Std Dev	12.34

Turn on : 25.3705

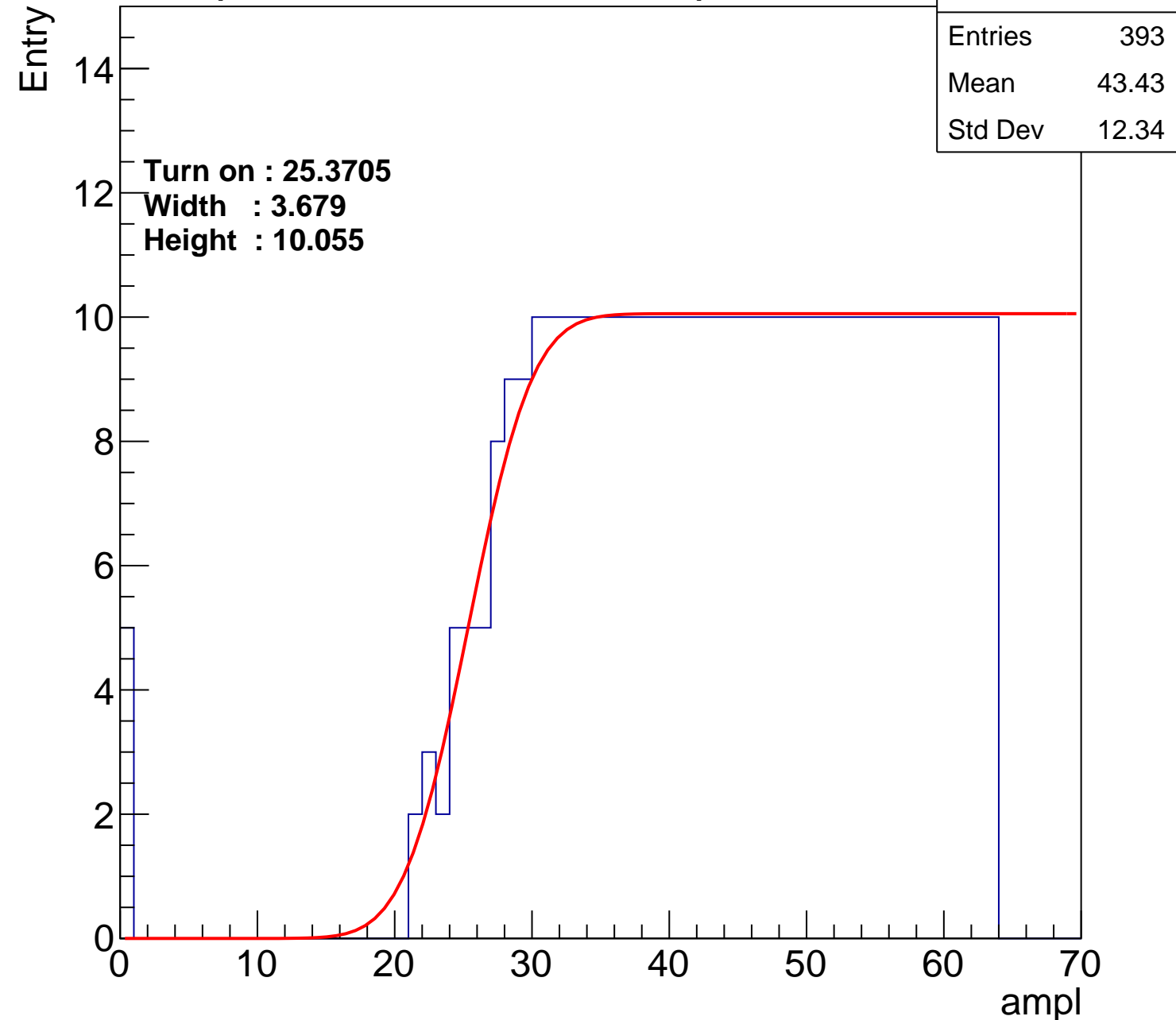
Width : 3.679

Height : 10.055

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch58

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	384
Mean	44.03
Std Dev	11.74

Turn on : 25.8631

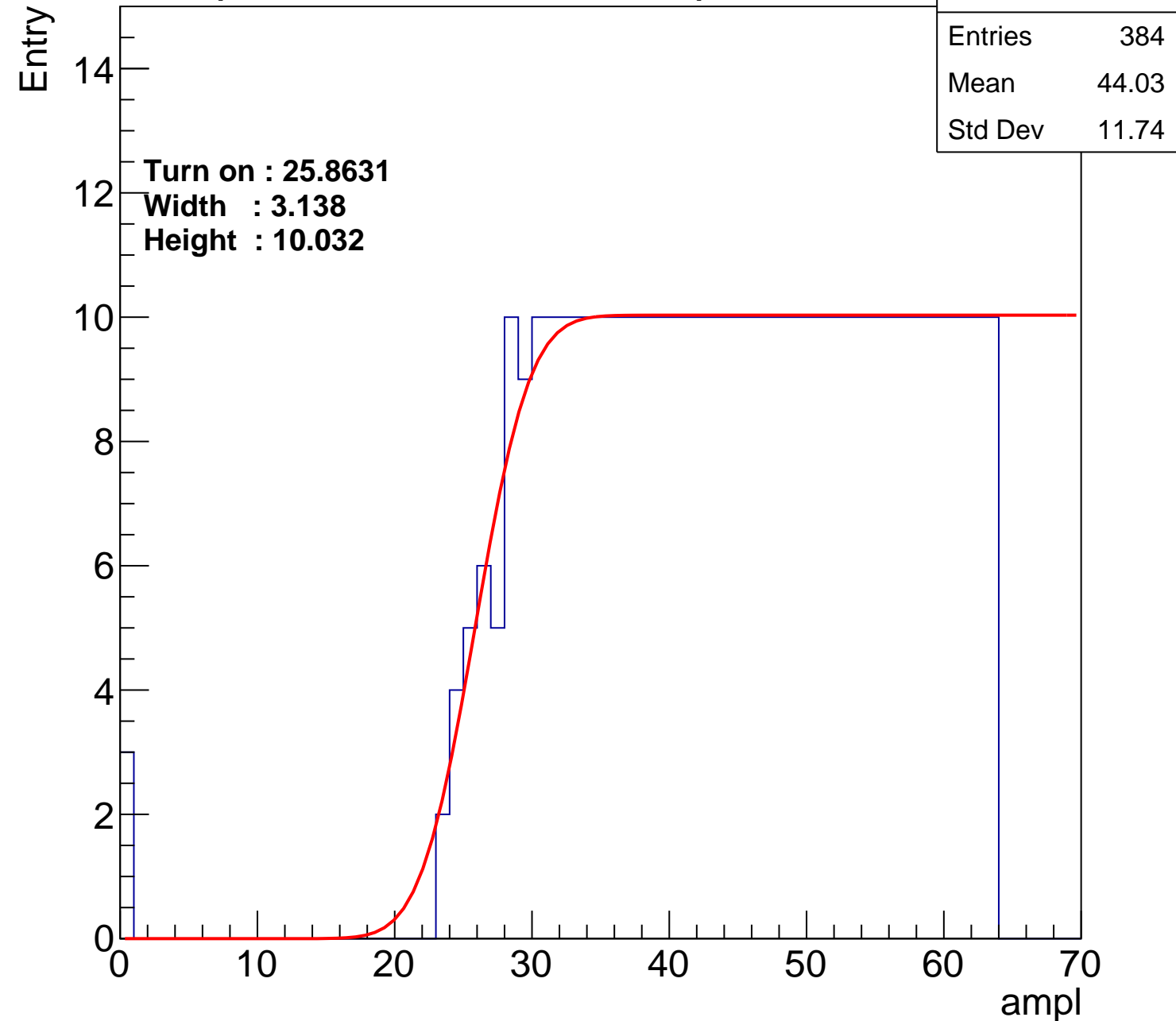
Width : 3.138

Height : 10.032

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch59

calib\_packv5\_042523\_0143.root, FC#4, port A2

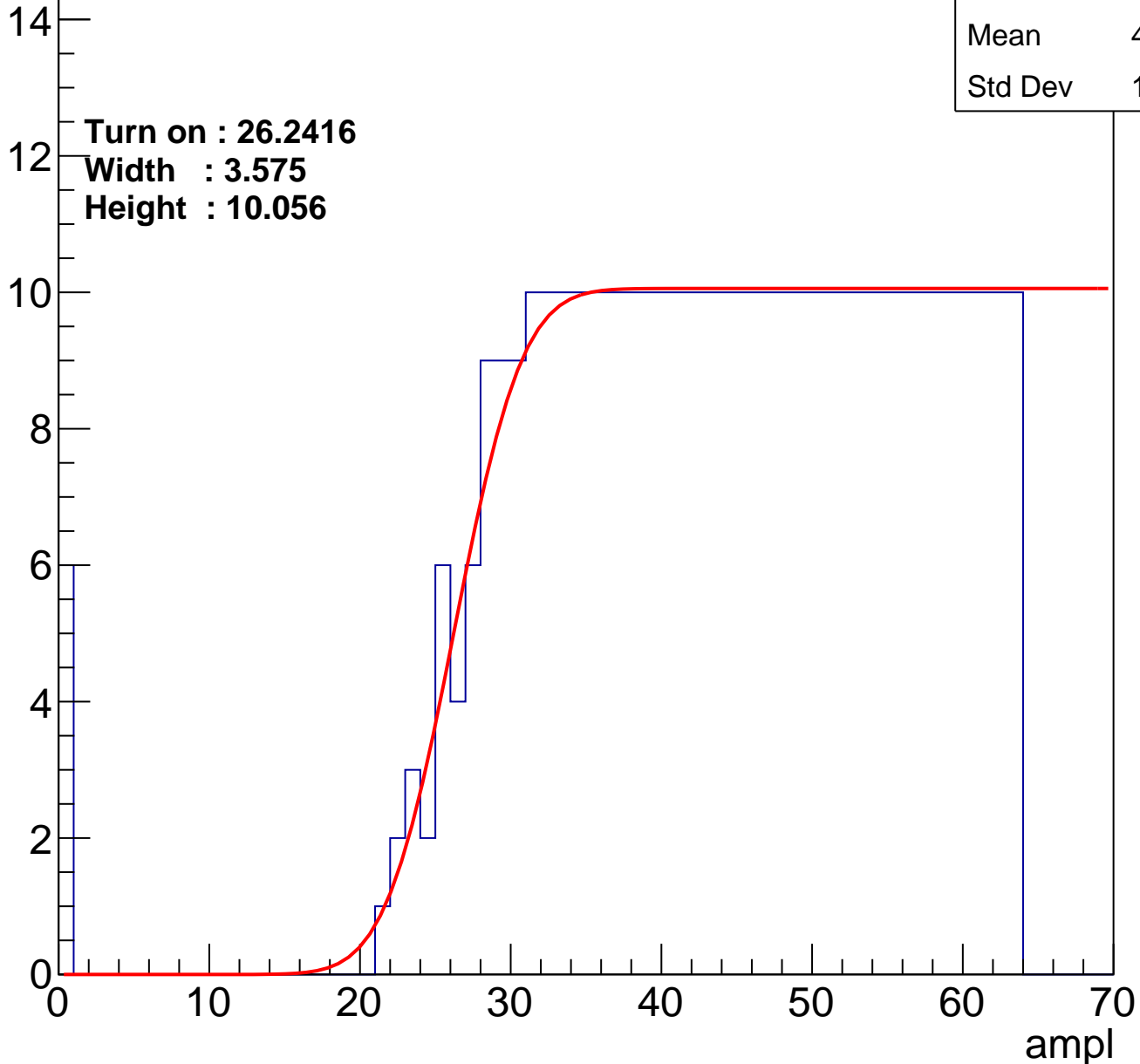
Entries	387
Mean	43.65
Std Dev	12.39

Turn on : 26.2416

Width : 3.575

Height : 10.056

Entry



# B1L100S, U16-ch60

calib\_packv5\_042523\_0143.root, FC#4, port A2

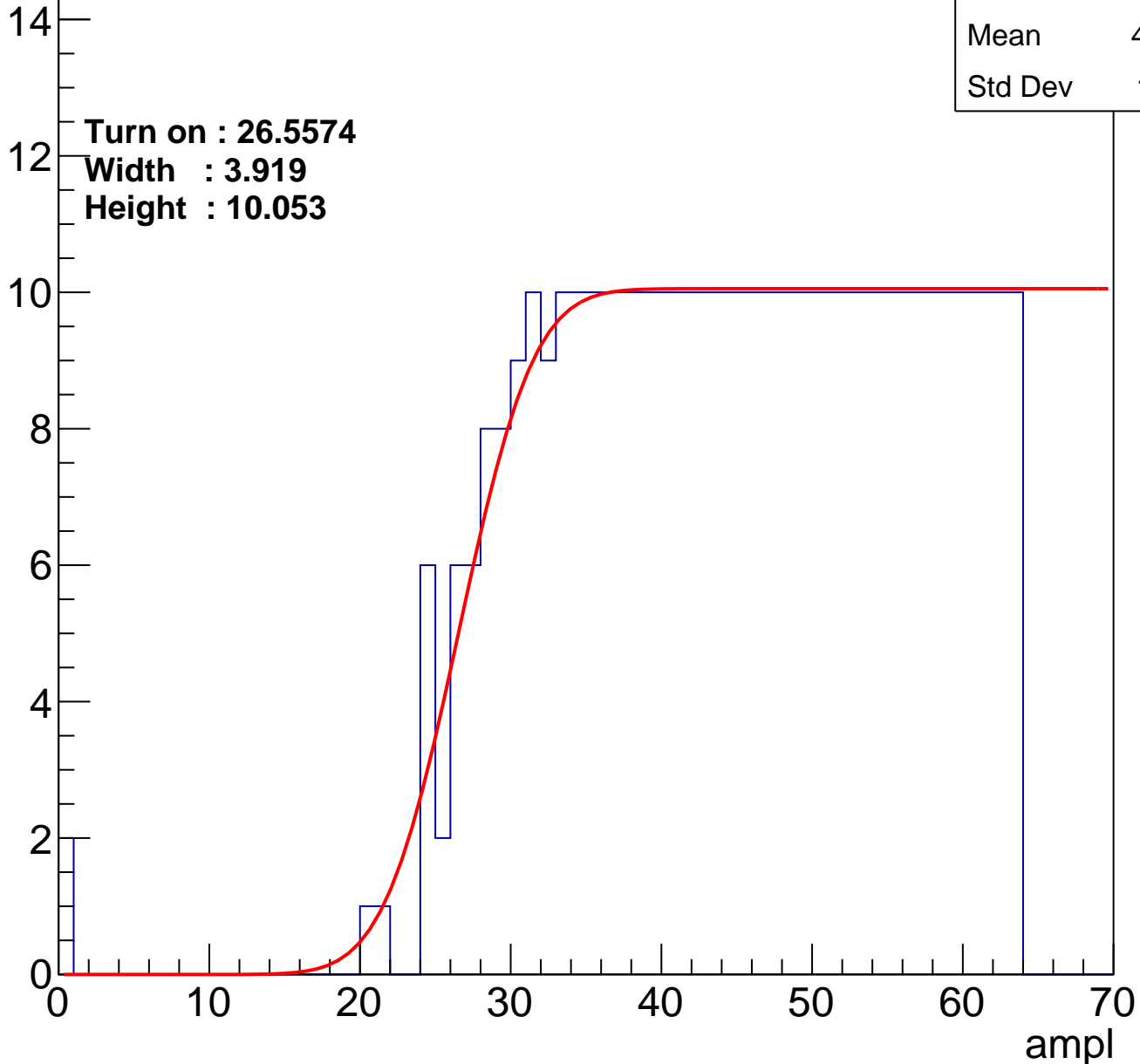
Entries	378
Mean	44.33
Std Dev	11.51

Turn on : 26.5574

Width : 3.919

Height : 10.053

Entry



# B1L100S, U16-ch61

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	398
Mean	43.45
Std Dev	11.8

Turn on : 24.4236

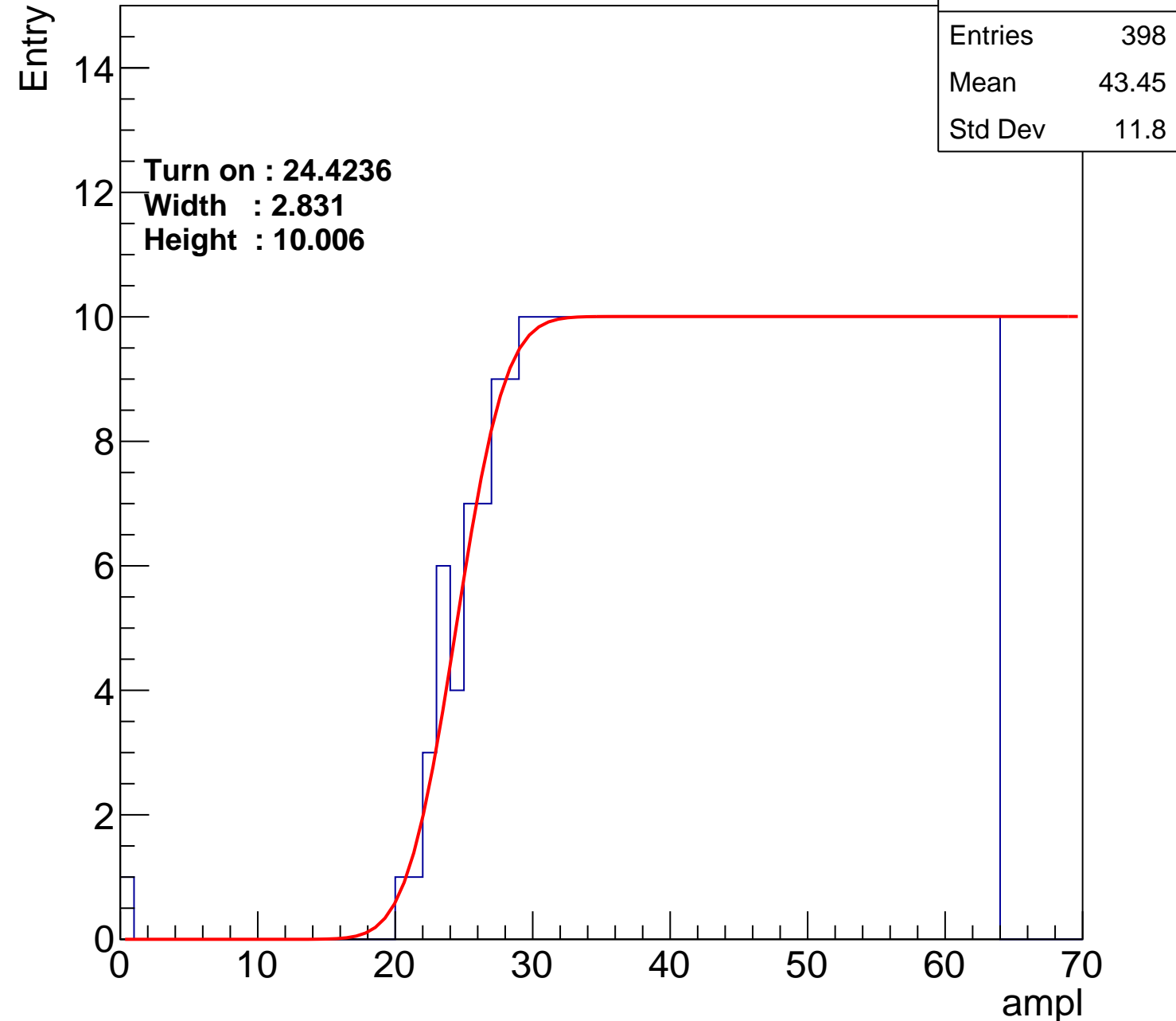
Width : 2.831

Height : 10.006

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch62

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	394
Mean	43.45
Std Dev	12.2

Turn on : 25.2108

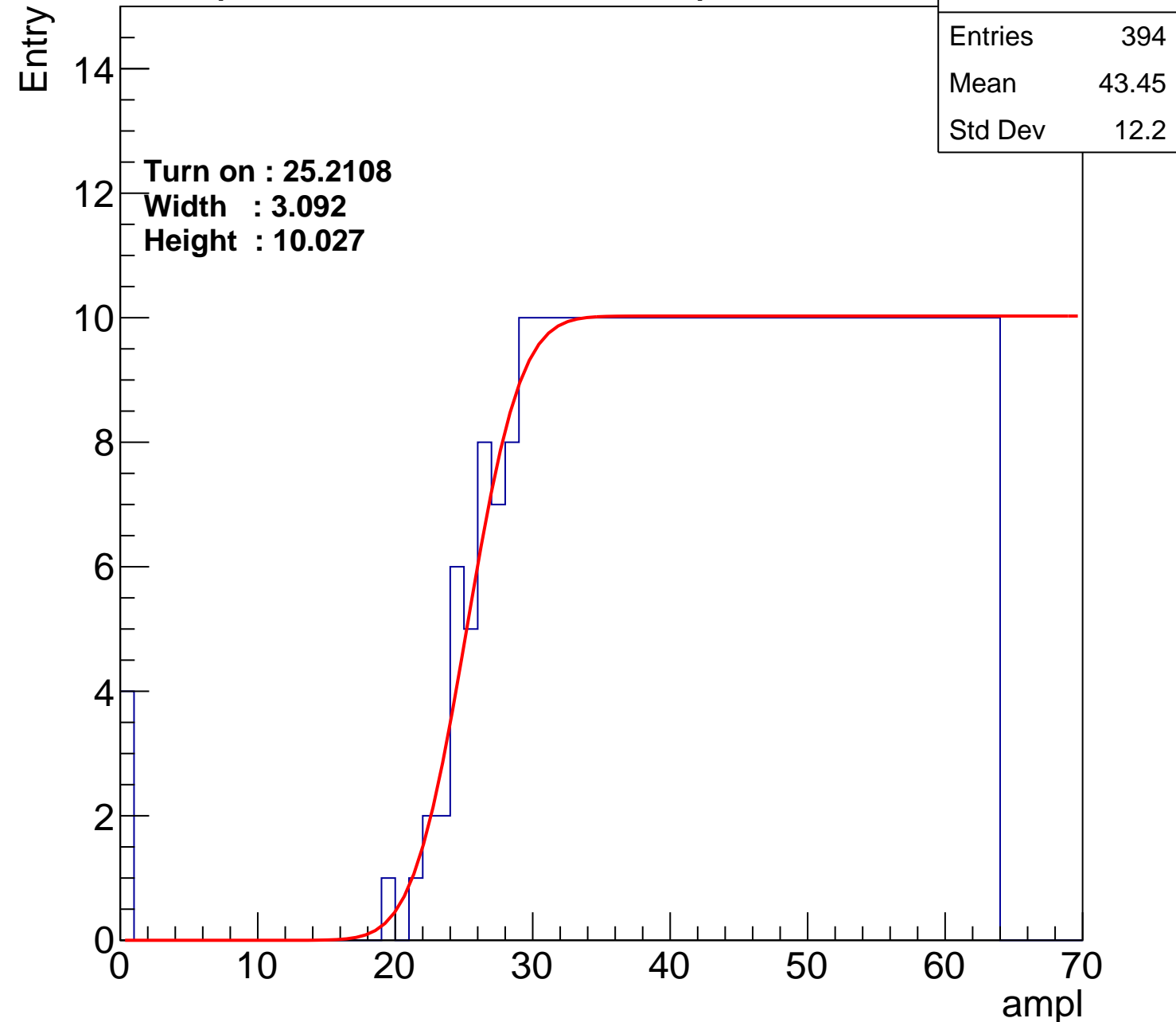
Width : 3.092

Height : 10.027

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L100S, U16-ch63

calib\_packv5\_042523\_0143.root, FC#4, port A2

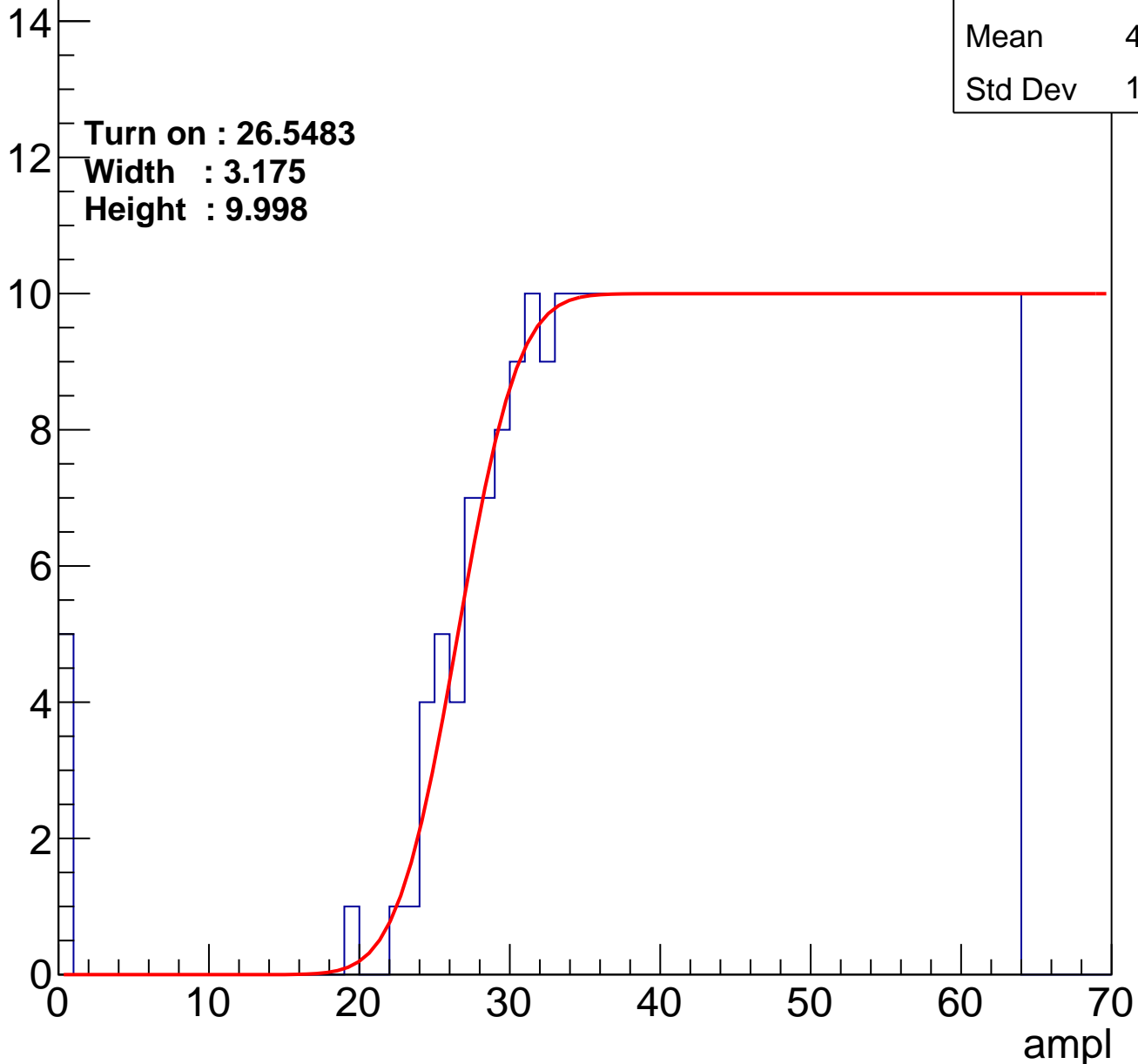
Entries	381
Mean	43.97
Std Dev	12.13

Turn on : 26.5483

Width : 3.175

Height : 9.998

Entry



# B1L100S, U16-ch64

calib\_packv5\_042523\_0143.root, FC#4, port A2

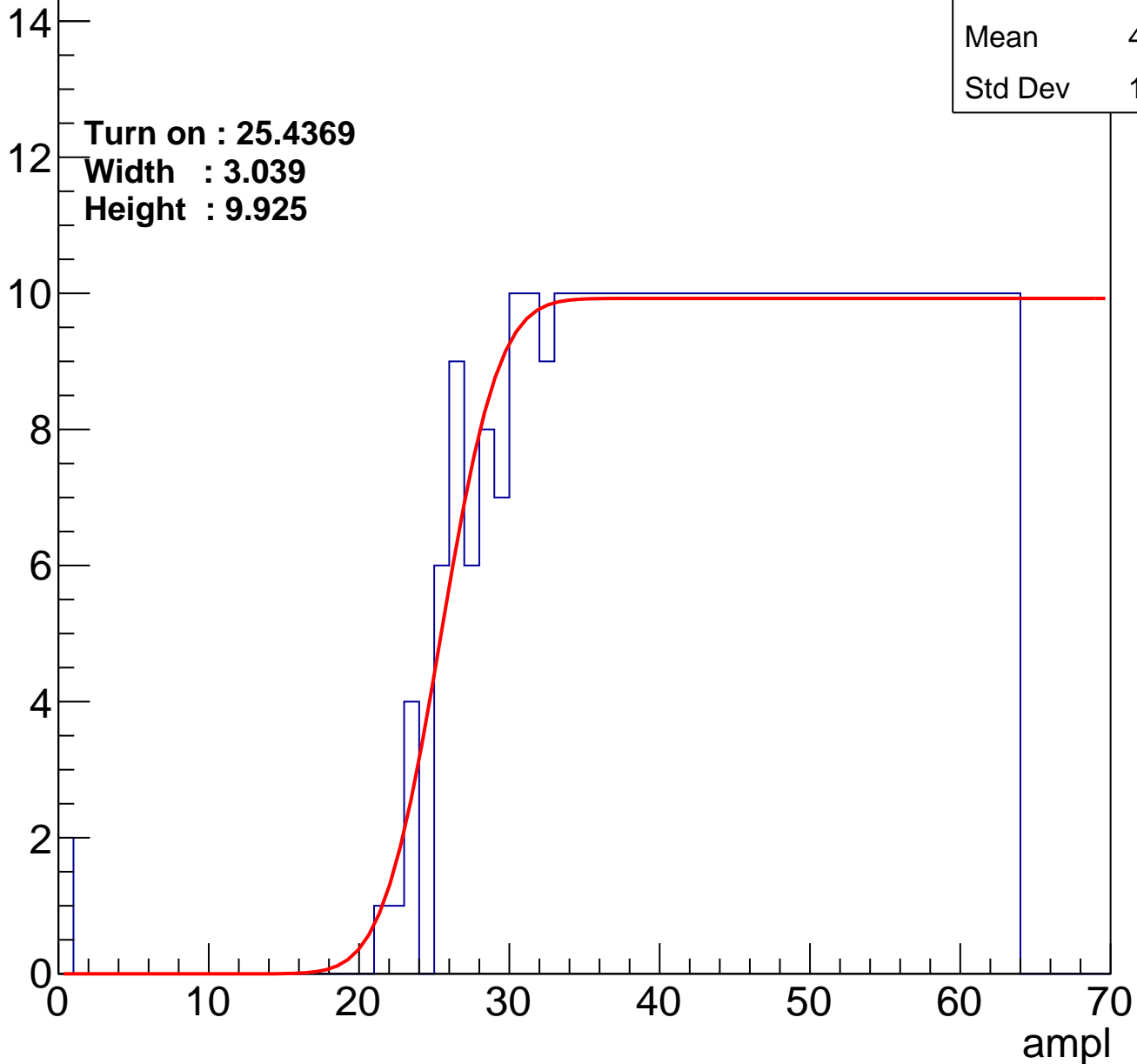
Entries	383
Mean	44.09
Std Dev	11.63

Turn on : 25.4369

Width : 3.039

Height : 9.925

Entry



# B1L100S, U16-ch65

calib\_packv5\_042523\_0143.root, FC#4, port A2

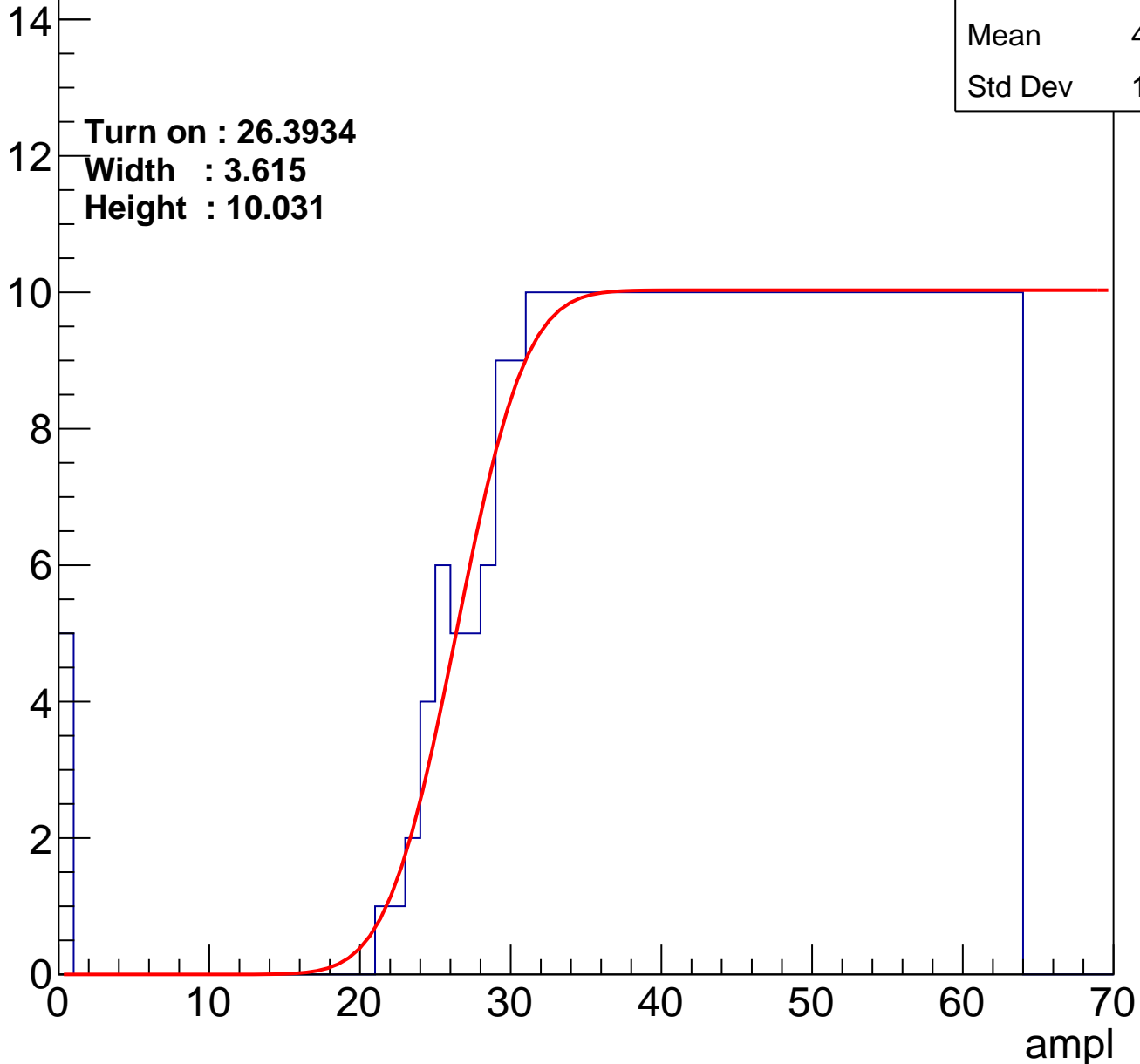
Entries	383
Mean	43.89
Std Dev	12.16

Turn on : 26.3934

Width : 3.615

Height : 10.031

Entry



# B1L100S, U16-ch66

calib\_packv5\_042523\_0143.root, FC#4, port A2

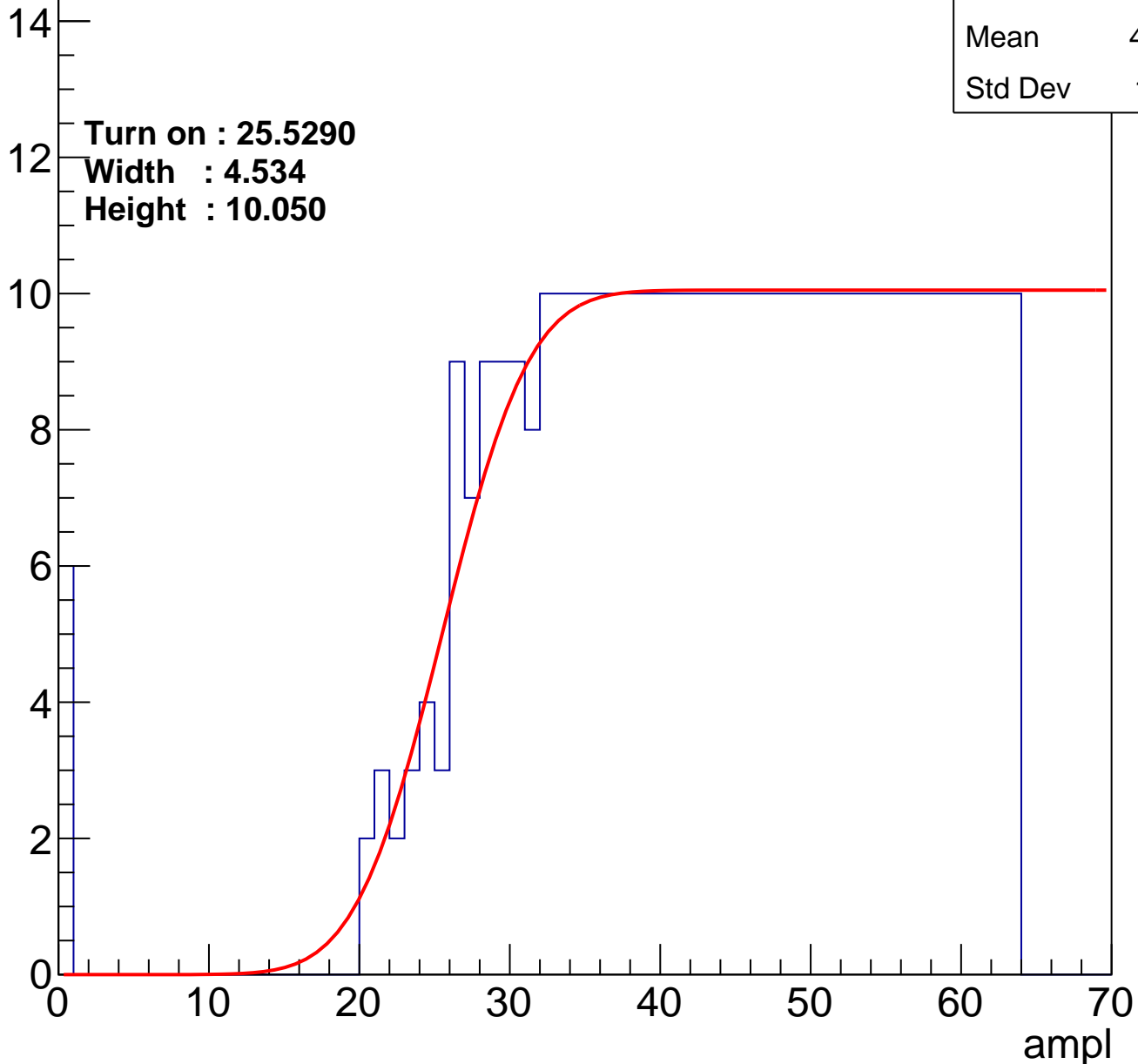
Entries	394
Mean	43.25
Std Dev	12.61

Turn on : 25.5290

Width : 4.534

Height : 10.050

Entry



# B1L100S, U16-ch67

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	387
Mean	43.72
Std Dev	12.2

Turn on : 26.0947

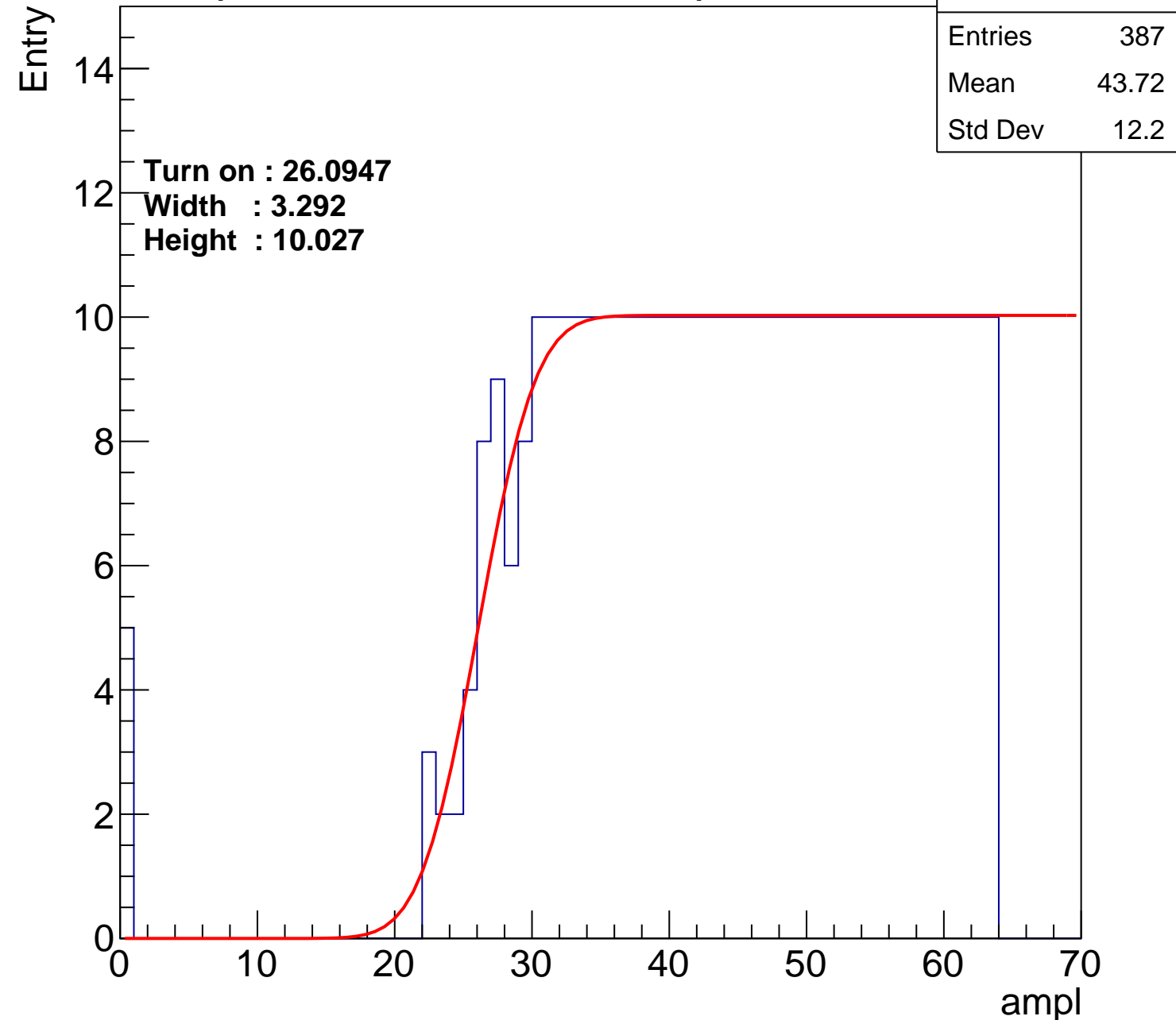
Width : 3.292

Height : 10.027

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch68

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	378
Mean	44.45
Std Dev	11.24

Turn on : 26.4583

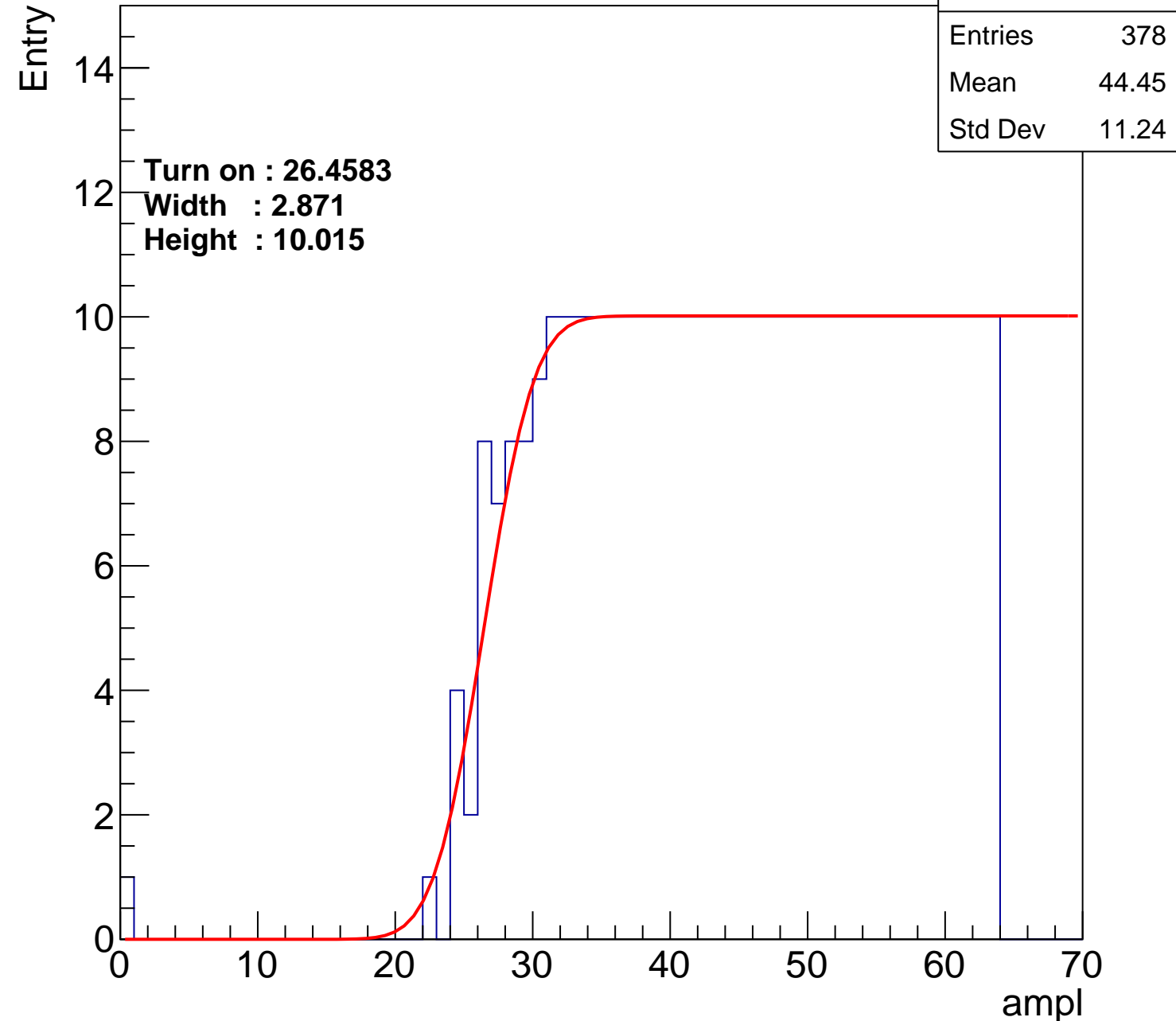
Width : 2.871

Height : 10.015

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch69

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	394
Mean	43.52
Std Dev	12.03

Turn on : 24.9295

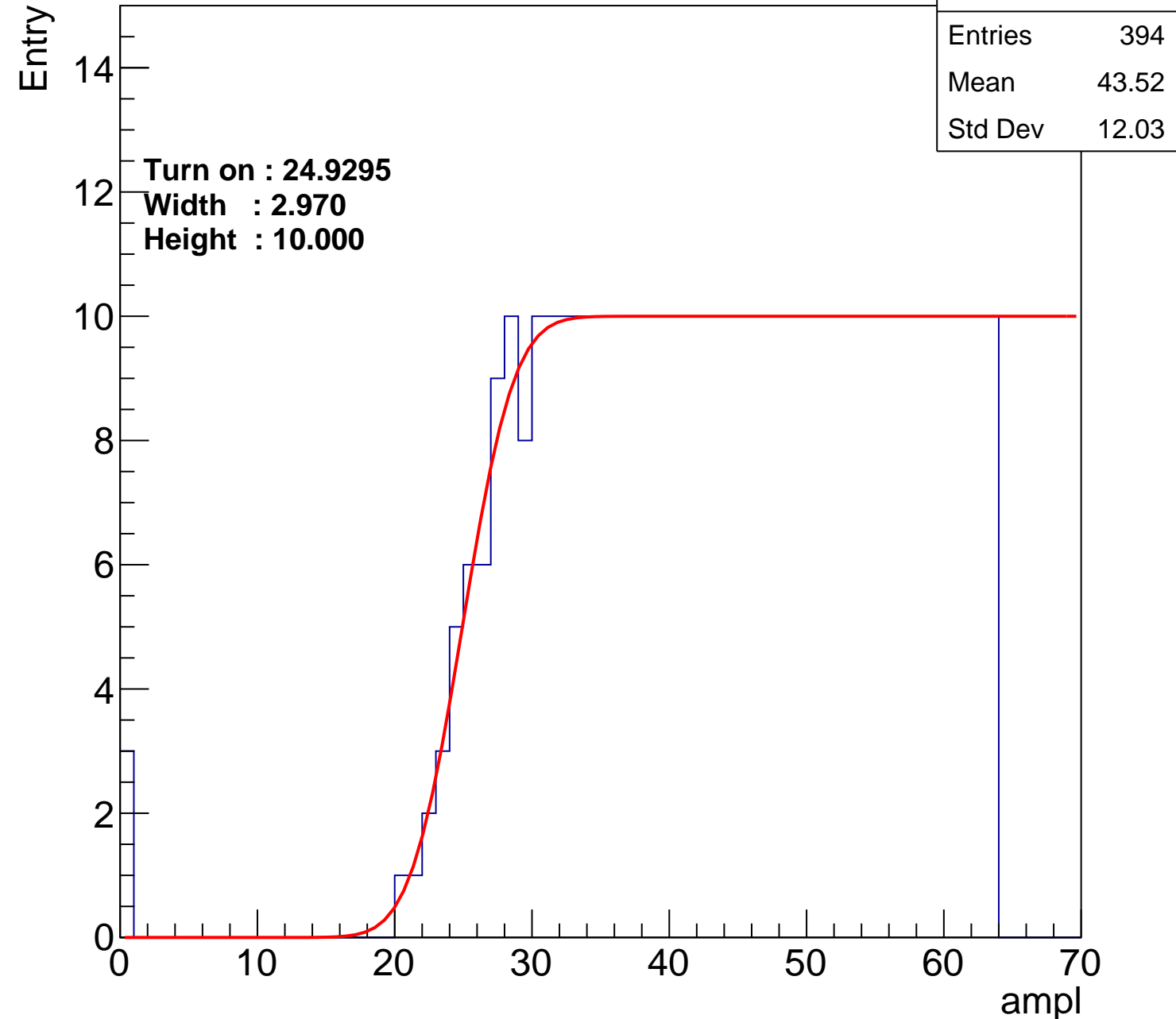
Width : 2.970

Height : 10.000

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch70

calib\_packv5\_042523\_0143.root, FC#4, port A2

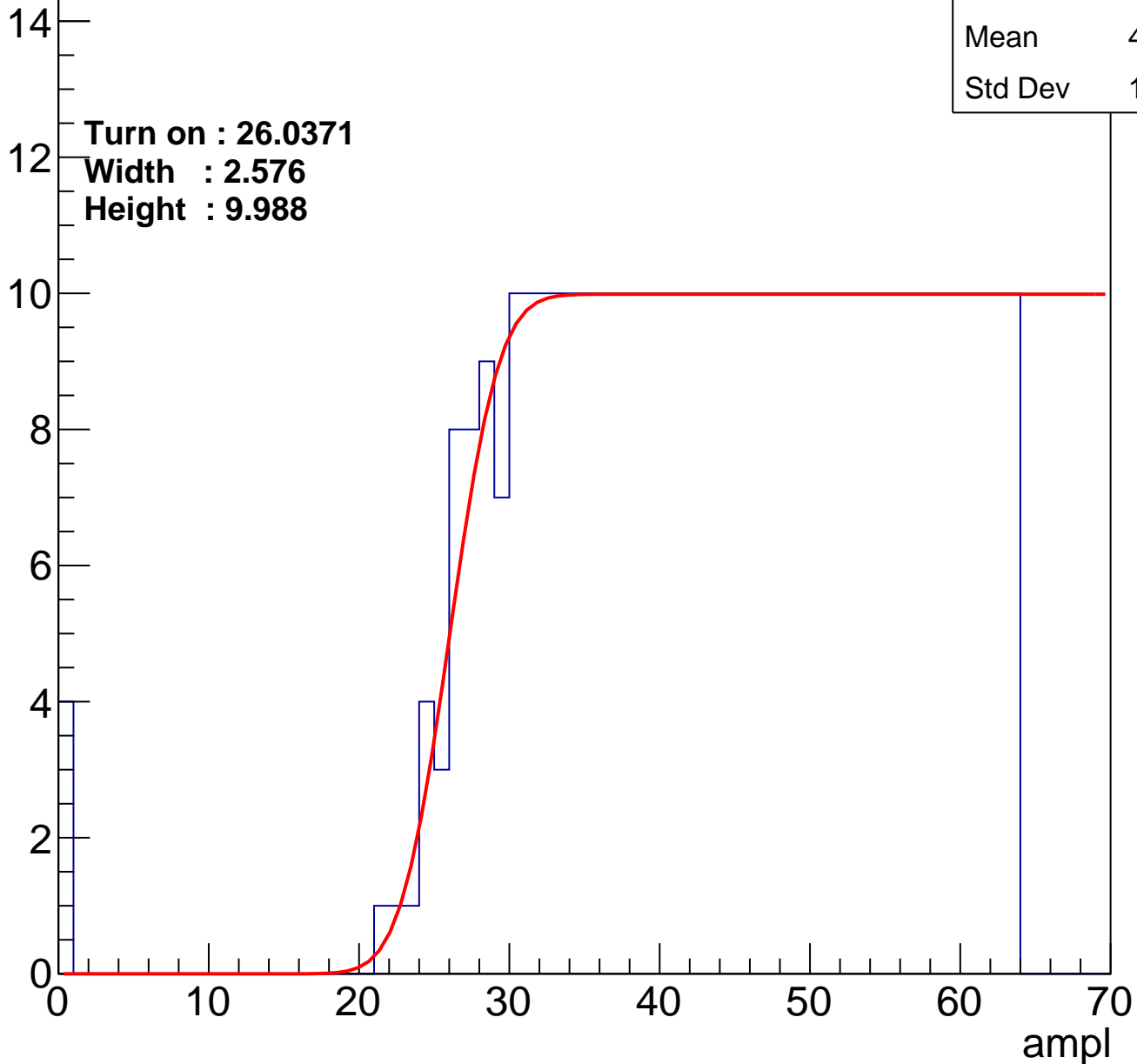
Entries	386
Mean	43.85
Std Dev	11.99

Turn on : 26.0371

Width : 2.576

Height : 9.988

Entry





# B1L100S, U16-ch71

calib\_packv5\_042523\_0143.root, FC#4, port A2

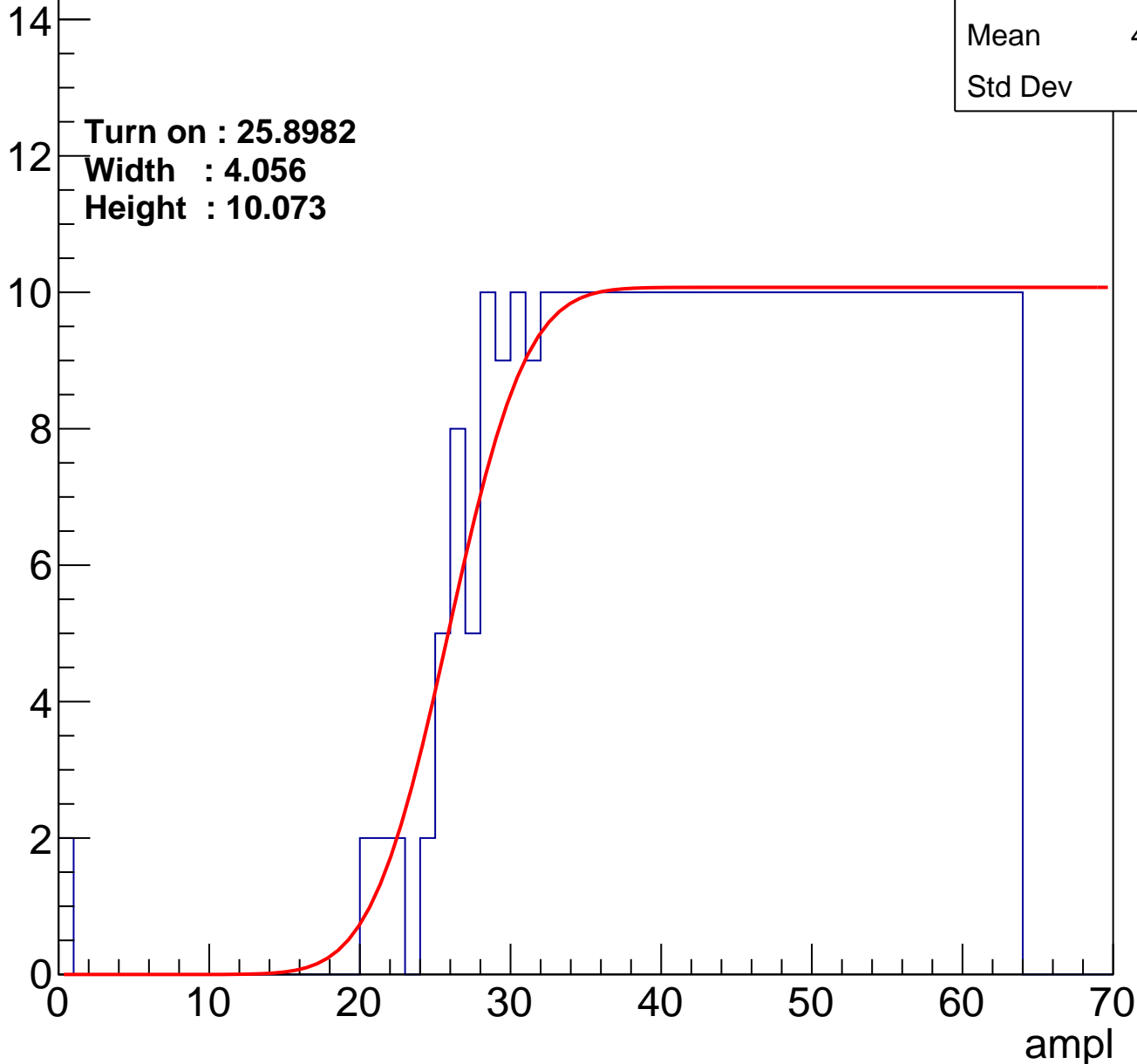
Entries	386
Mean	43.94
Std Dev	11.71

Turn on : 25.8982

Width : 4.056

Height : 10.073

Entry



# B1L100S, U16-ch72

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	375
Mean	44.47
Std Dev	11.46

Turn on : 26.9474

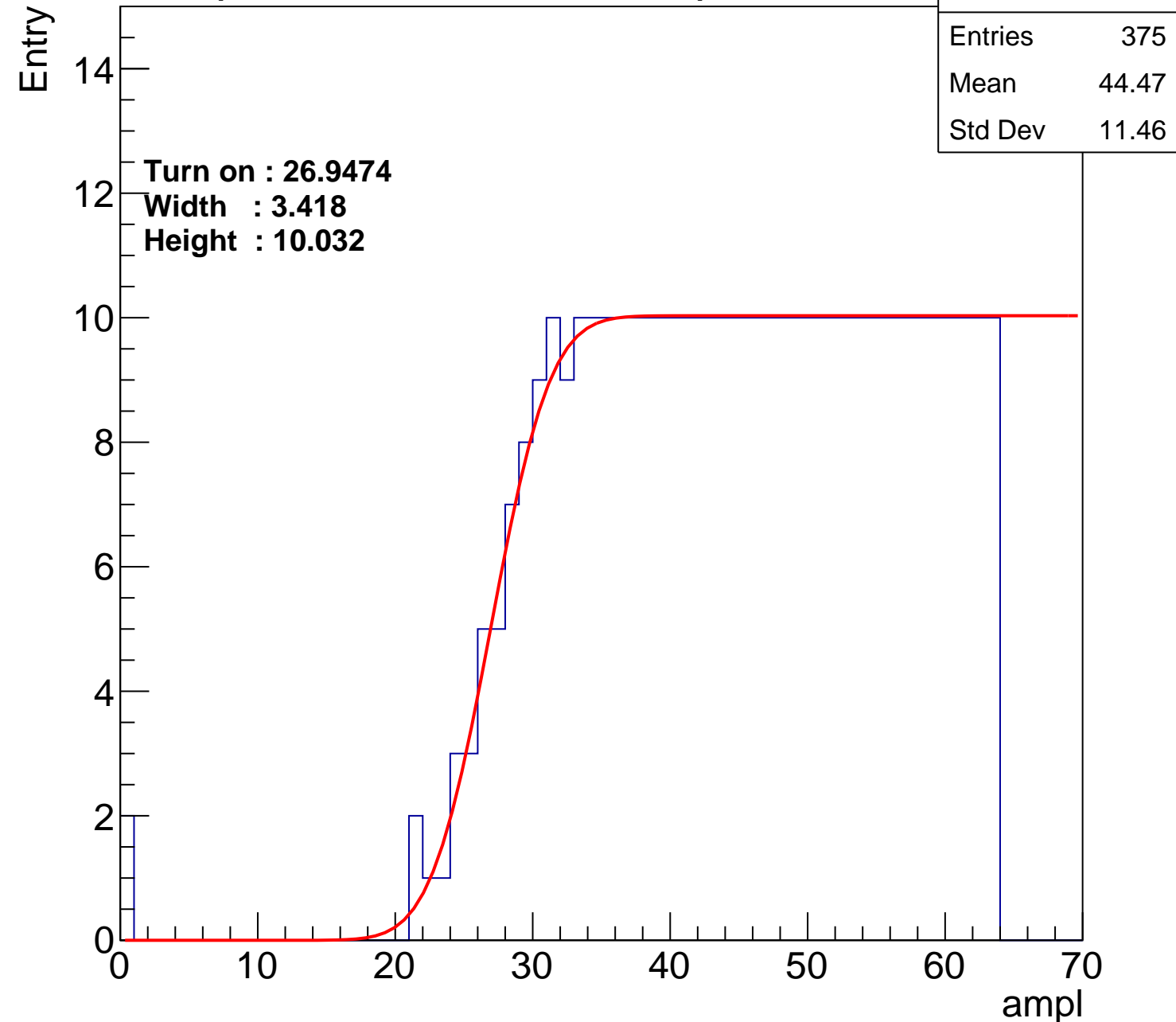
Width : 3.418

Height : 10.032

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch73

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	387
Mean	43.82
Std Dev	11.98

Turn on : 25.5324

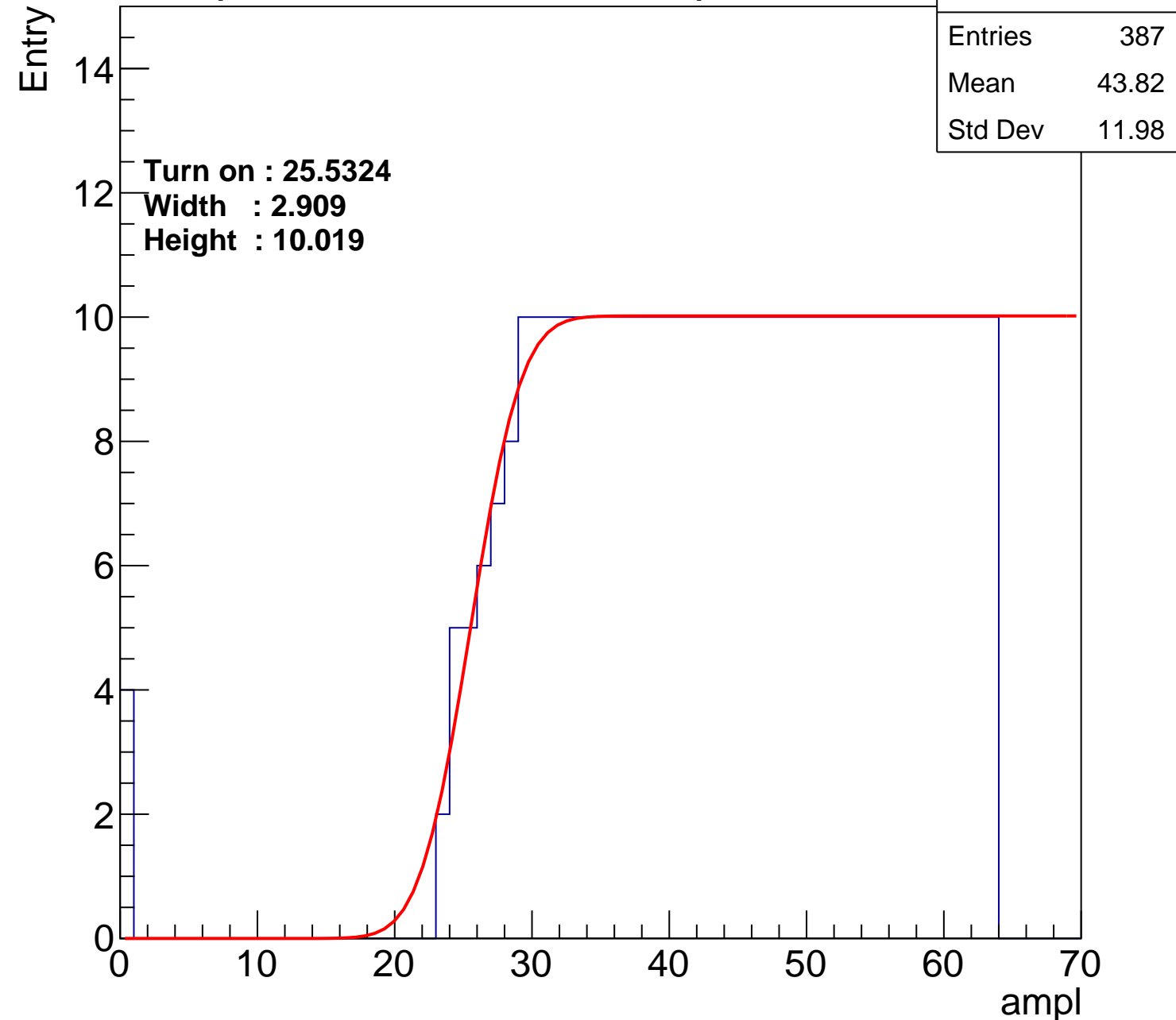
Width : 2.909

Height : 10.019

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch74

calib\_packv5\_042523\_0143.root, FC#4, port A2

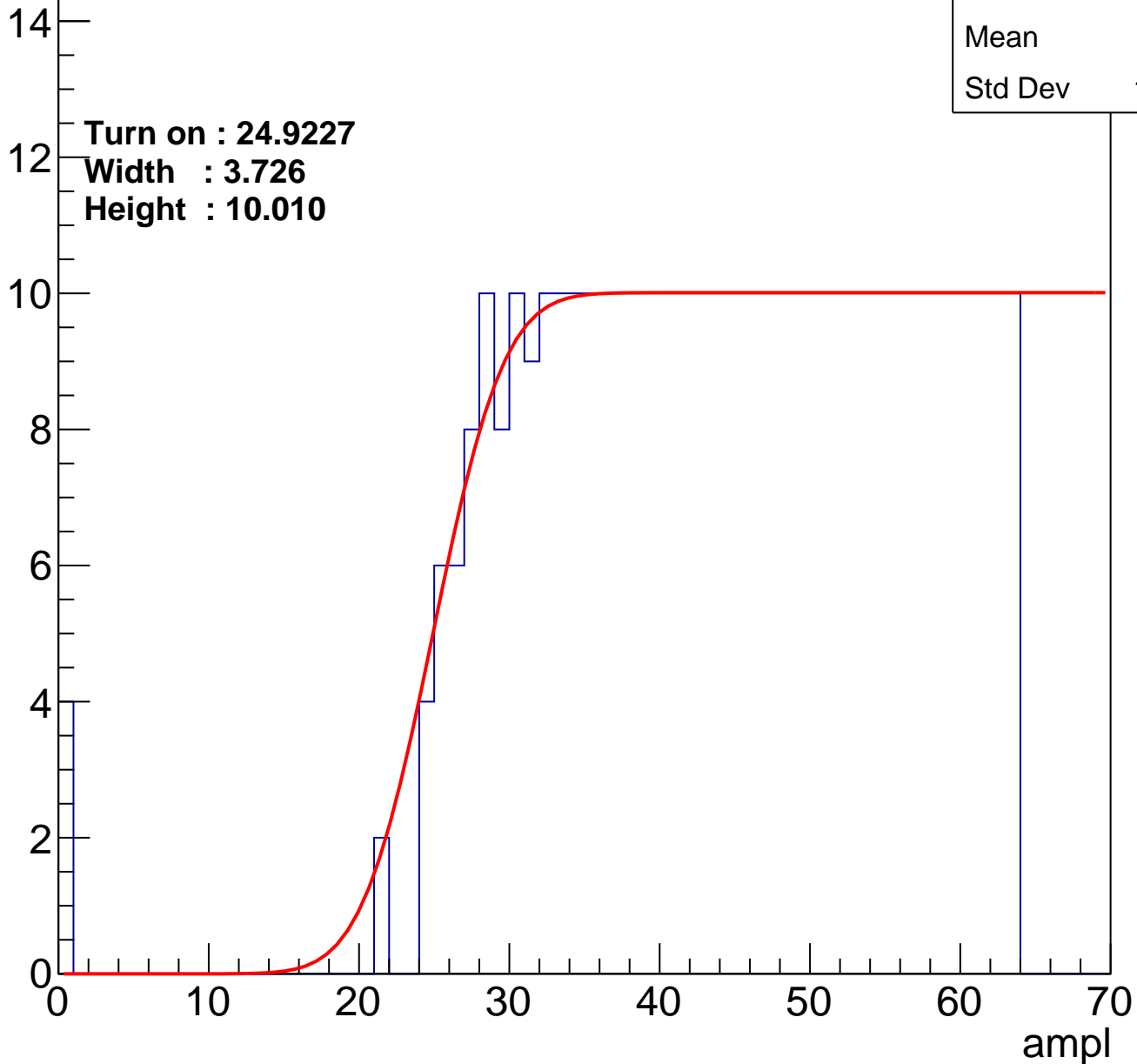
Entries	387
Mean	43.8
Std Dev	12.01

Turn on : 24.9227

Width : 3.726

Height : 10.010

Entry



# B1L100S, U16-ch75

calib\_packv5\_042523\_0143.root, FC#4, port A2

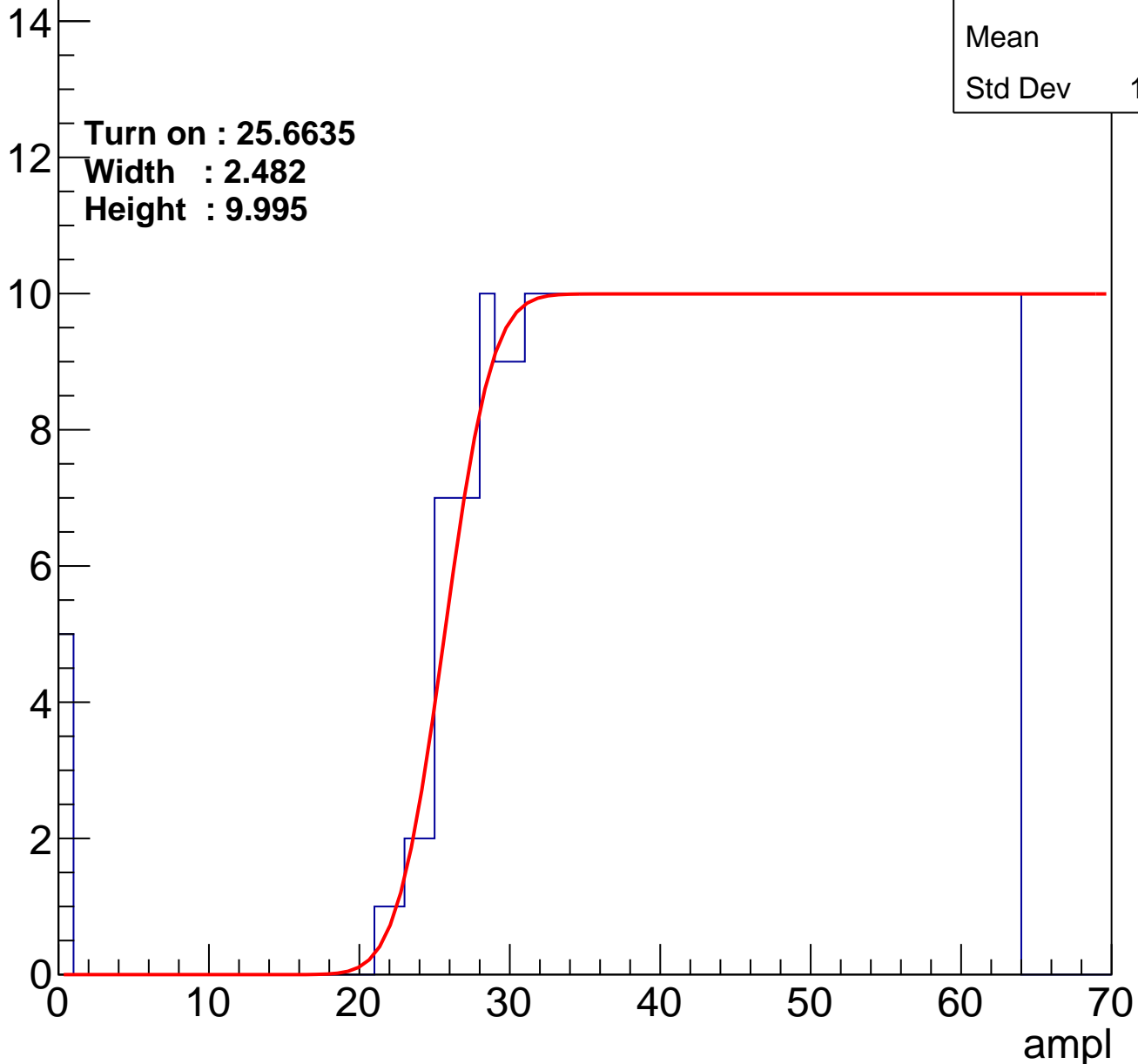
Entries	390
Mean	43.6
Std Dev	12.23

Turn on : 25.6635

Width : 2.482

Height : 9.995

Entry



# B1L100S, U16-ch76

calib\_packv5\_042523\_0143.root, FC#4, port A2

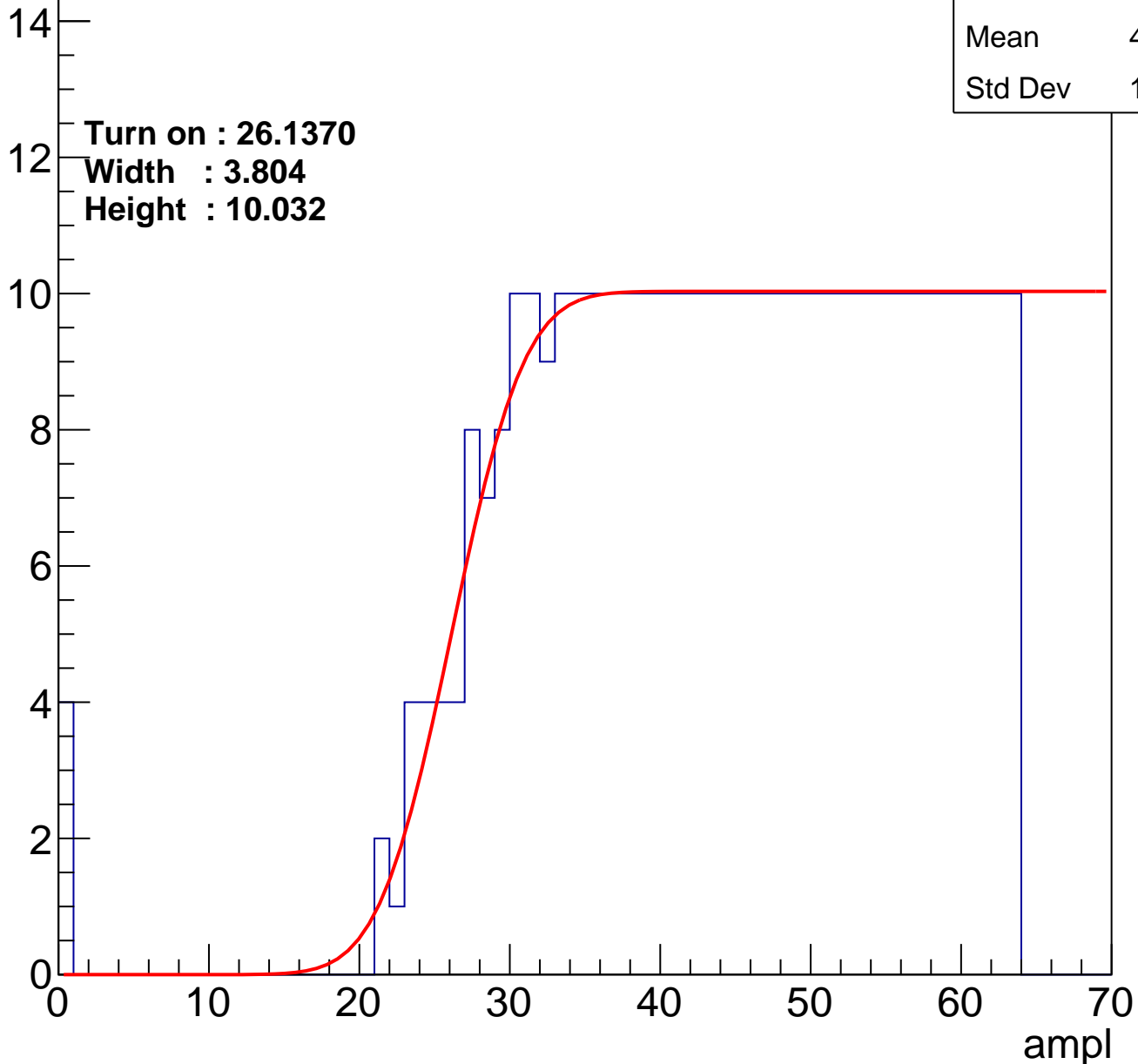
Entries	385
Mean	43.84
Std Dev	12.06

Turn on : 26.1370

Width : 3.804

Height : 10.032

Entry



# B1L100S, U16-ch77

calib\_packv5\_042523\_0143.root, FC#4, port A2

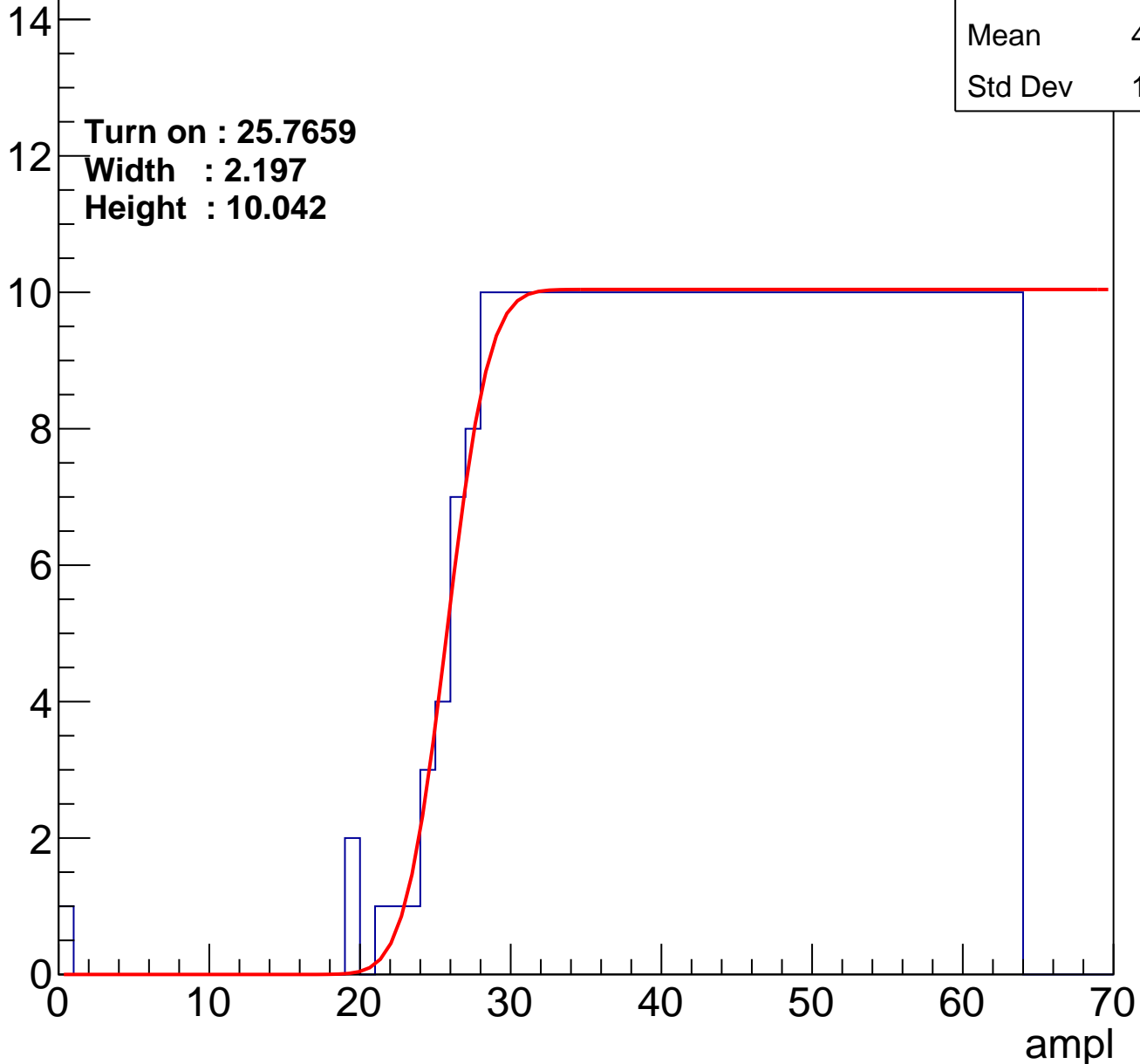
Entries	388
Mean	43.95
Std Dev	11.52

Turn on : 25.7659

Width : 2.197

Height : 10.042

Entry



# B1L100S, U16-ch78

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	385
Mean	43.94
Std Dev	11.84

Turn on : 26.0612

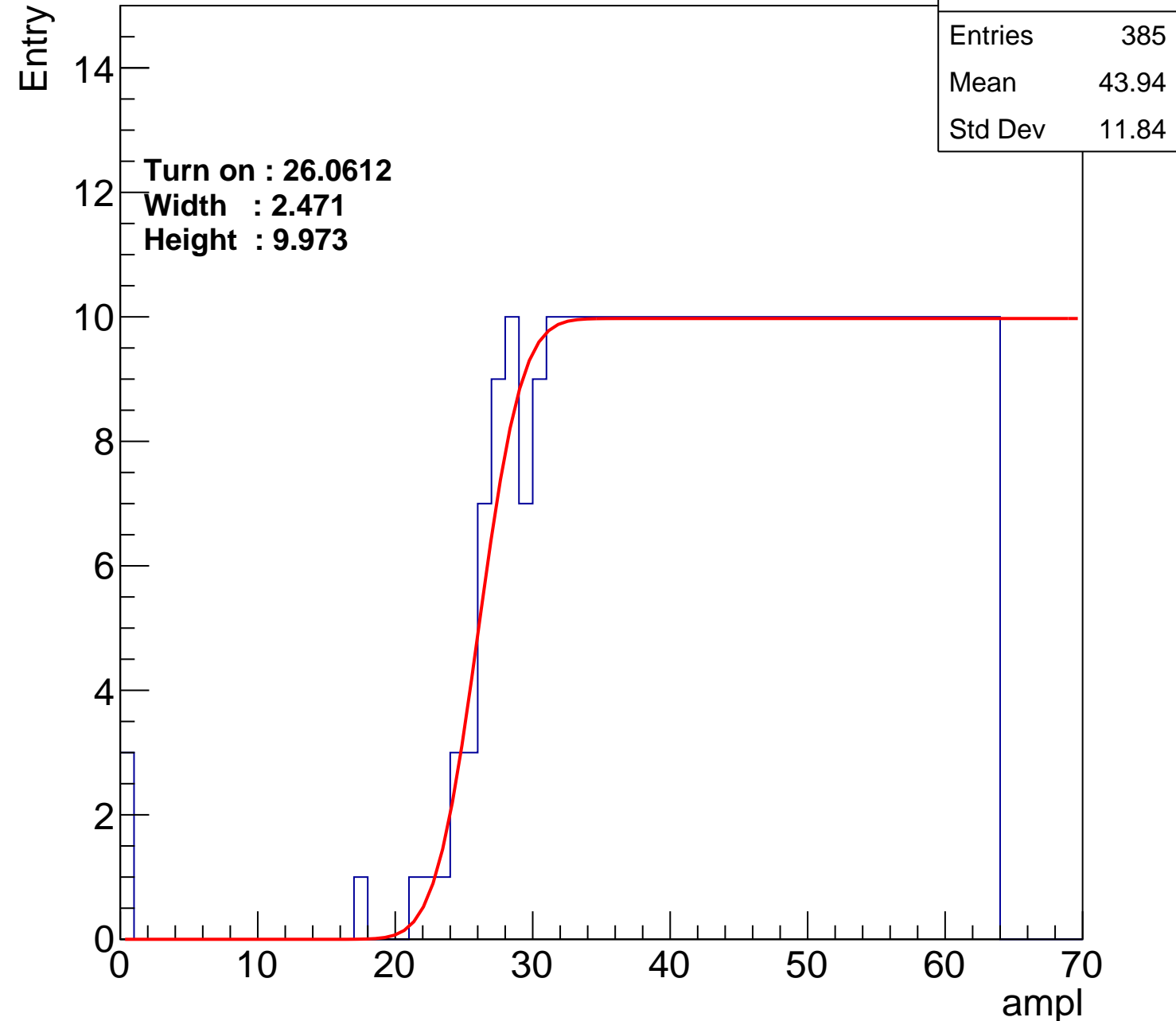
Width : 2.471

Height : 9.973

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L100S, U16-ch79

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	381
Mean	44.2
Std Dev	11.64

Turn on : 26.2213

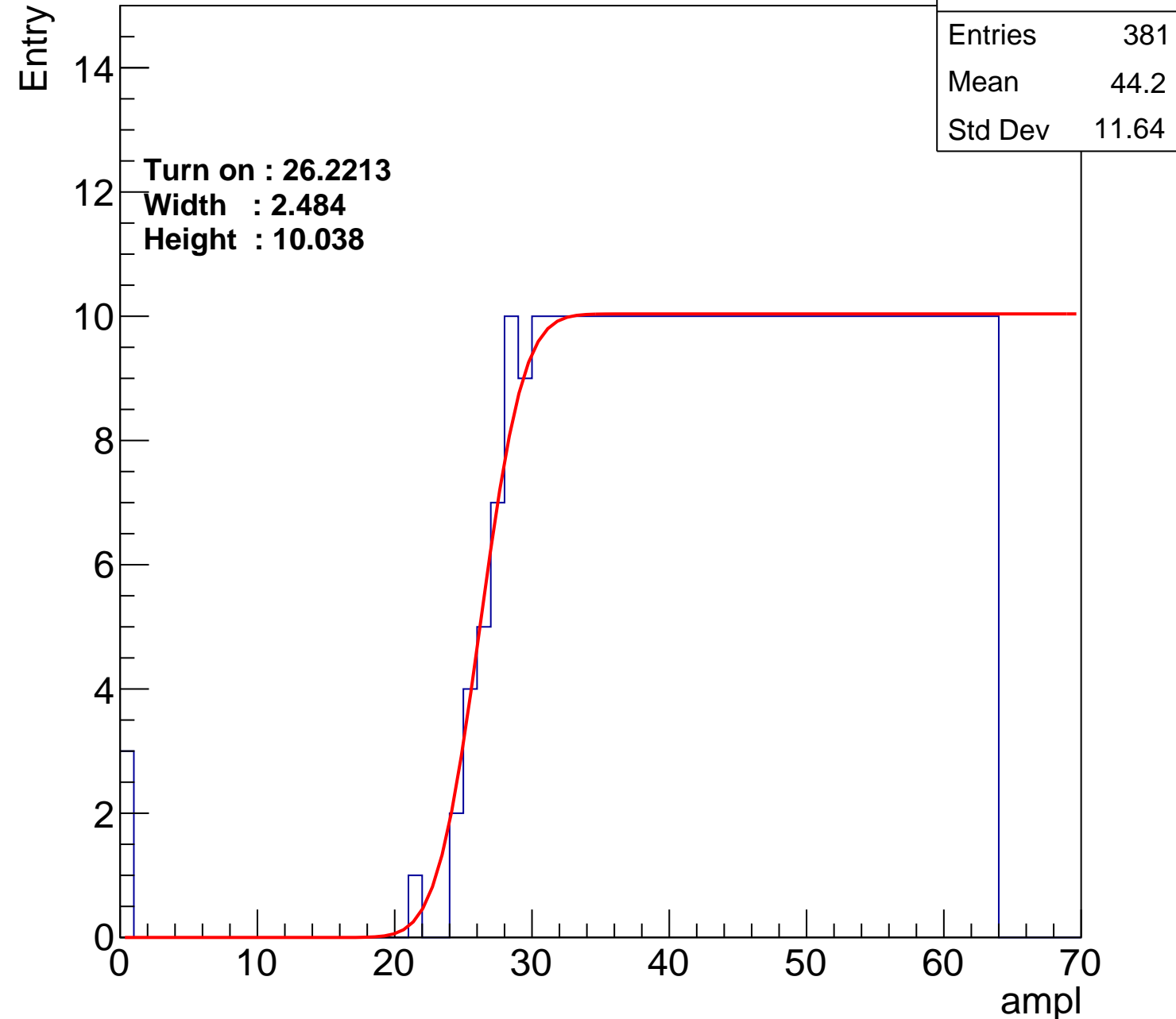
Width : 2.484

Height : 10.038

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch80

calib\_packv5\_042523\_0143.root, FC#4, port A2

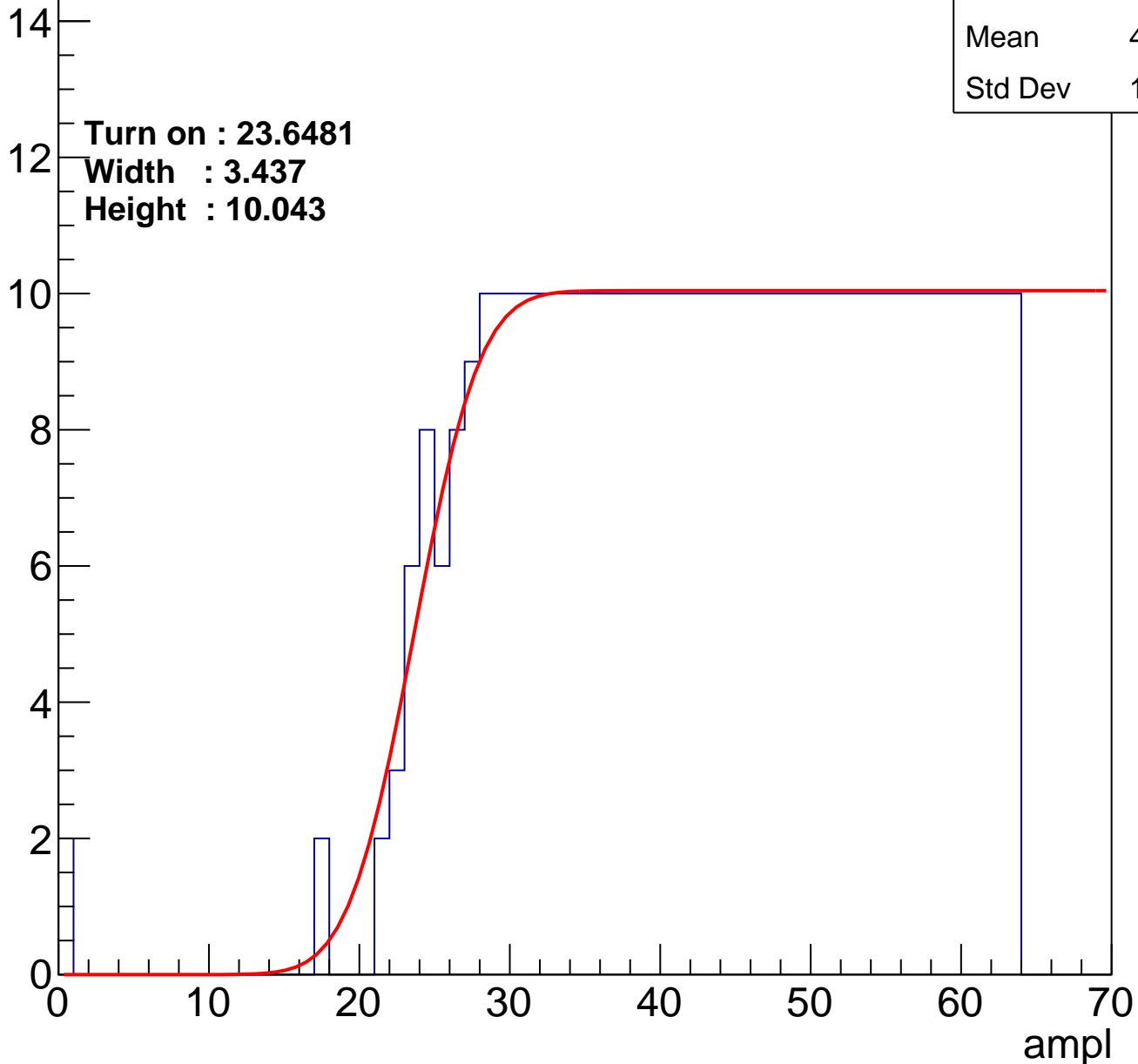
Entries	406
Mean	42.99
Std Dev	12.19

Turn on : 23.6481

Width : 3.437

Height : 10.043

Entry



# B1L100S, U16-ch81

calib\_packv5\_042523\_0143.root, FC#4, port A2

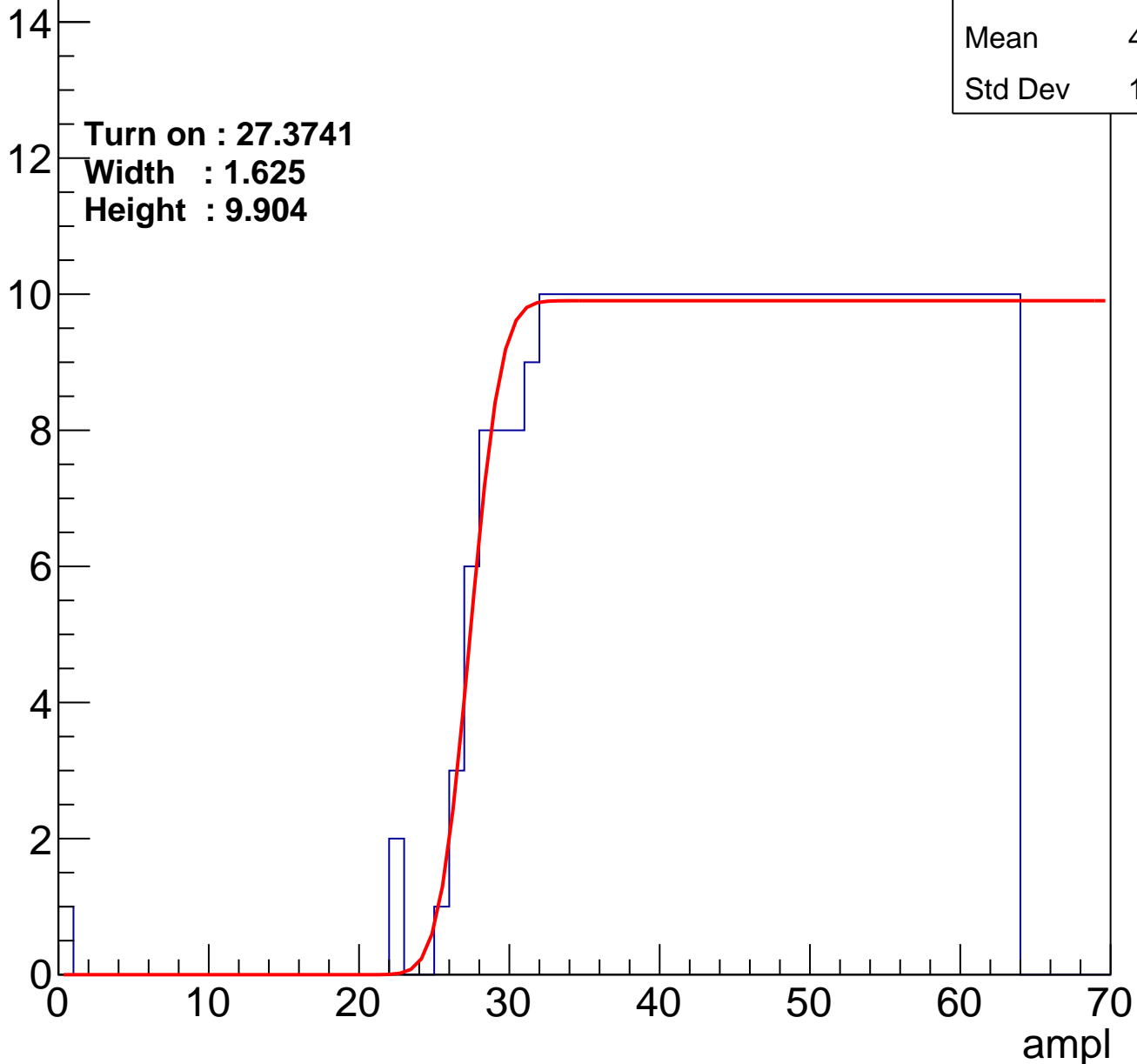
Entry

Entries	366
Mean	45.04
Std Dev	10.93

Turn on : 27.3741

Width : 1.625

Height : 9.904



# B1L100S, U16-ch82

calib\_packv5\_042523\_0143.root, FC#4, port A2

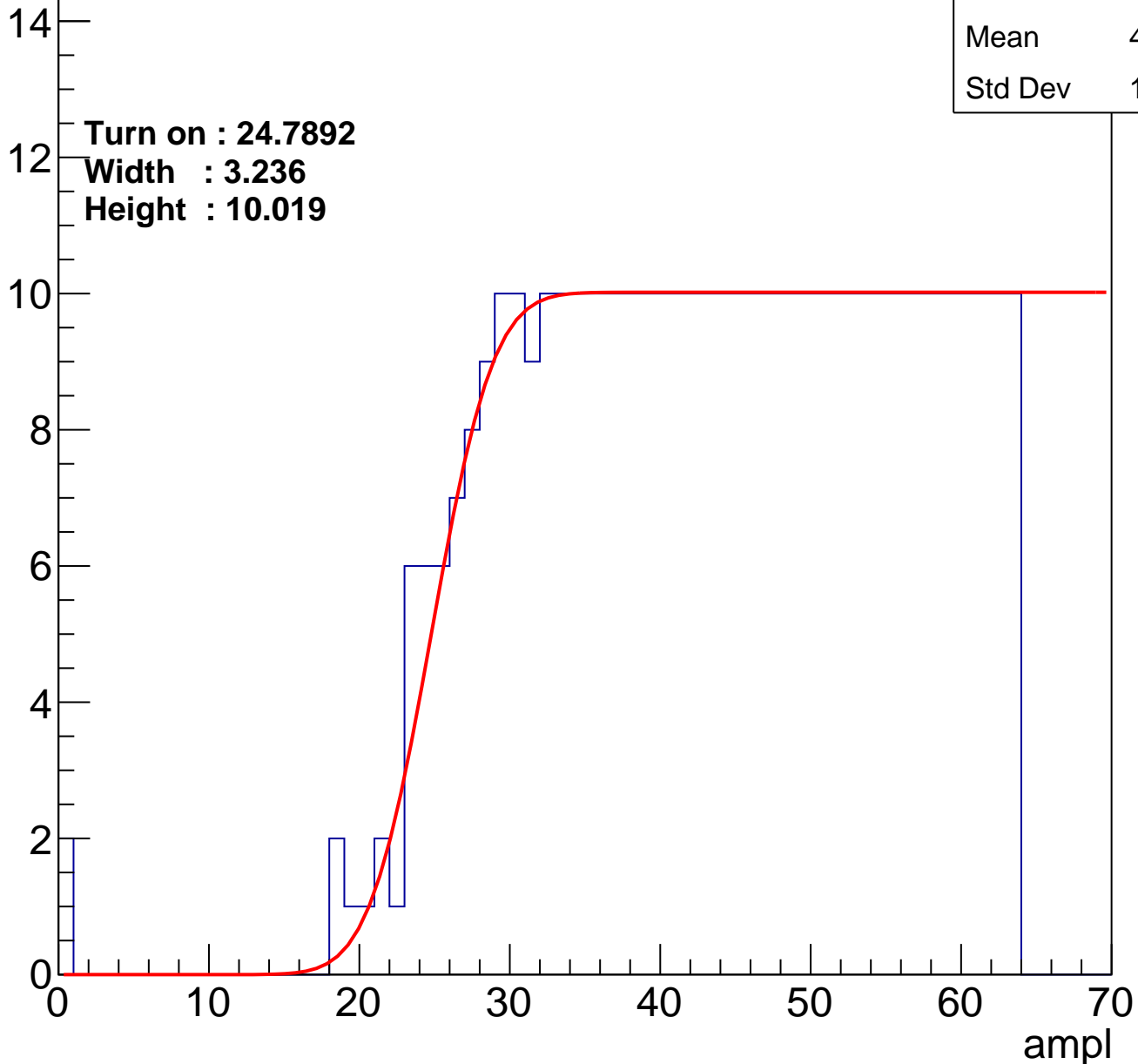
Entries	400
Mean	43.23
Std Dev	12.12

Turn on : 24.7892

Width : 3.236

Height : 10.019

Entry



# B1L100S, U16-ch83

calib\_packv5\_042523\_0143.root, FC#4, port A2

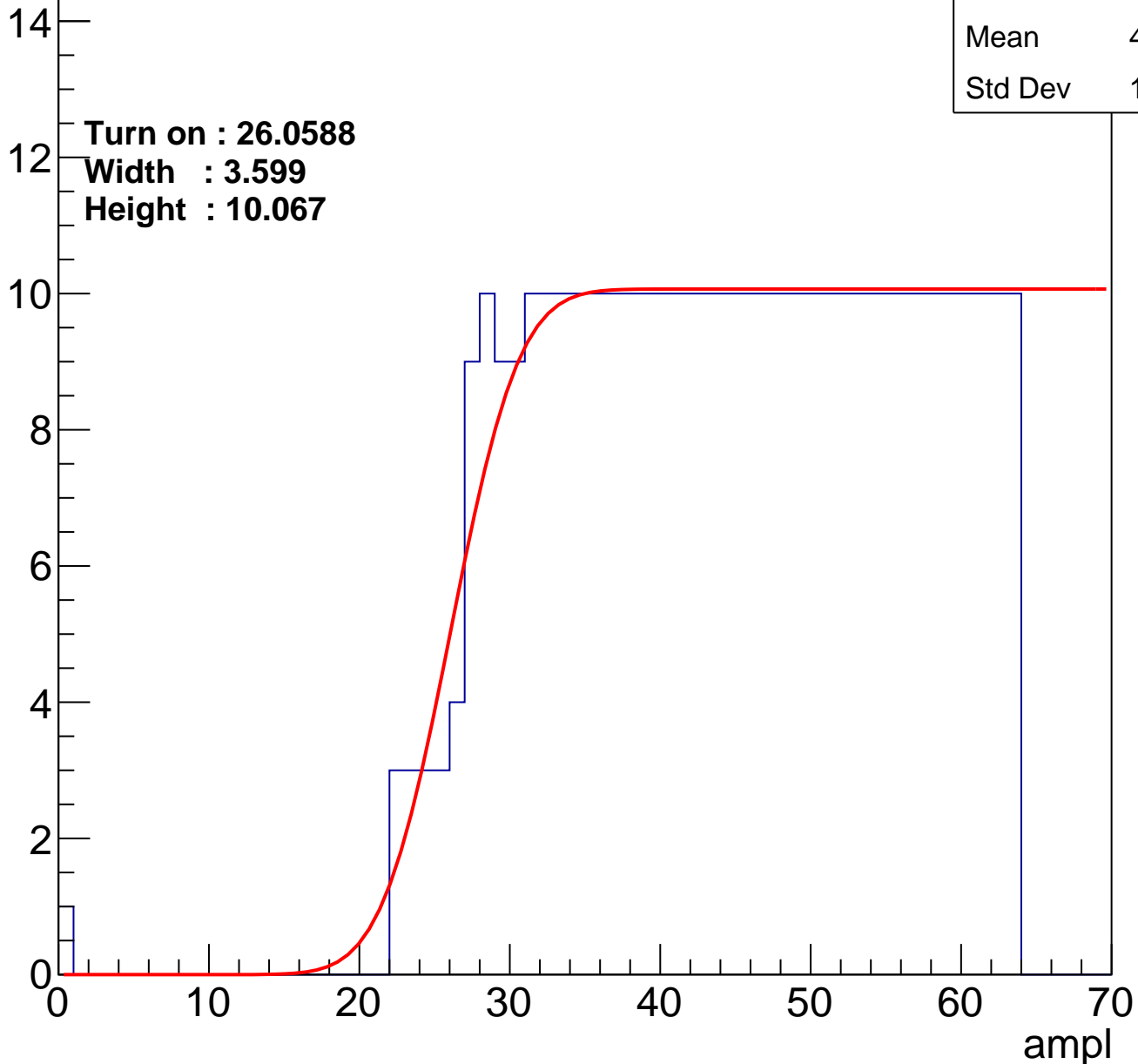
Entries	384
Mean	44.14
Std Dev	11.42

Turn on : 26.0588

Width : 3.599

Height : 10.067

Entry



# B1L100S, U16-ch84

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	383
Mean	44.17
Std Dev	11.43

Turn on : 26.5724

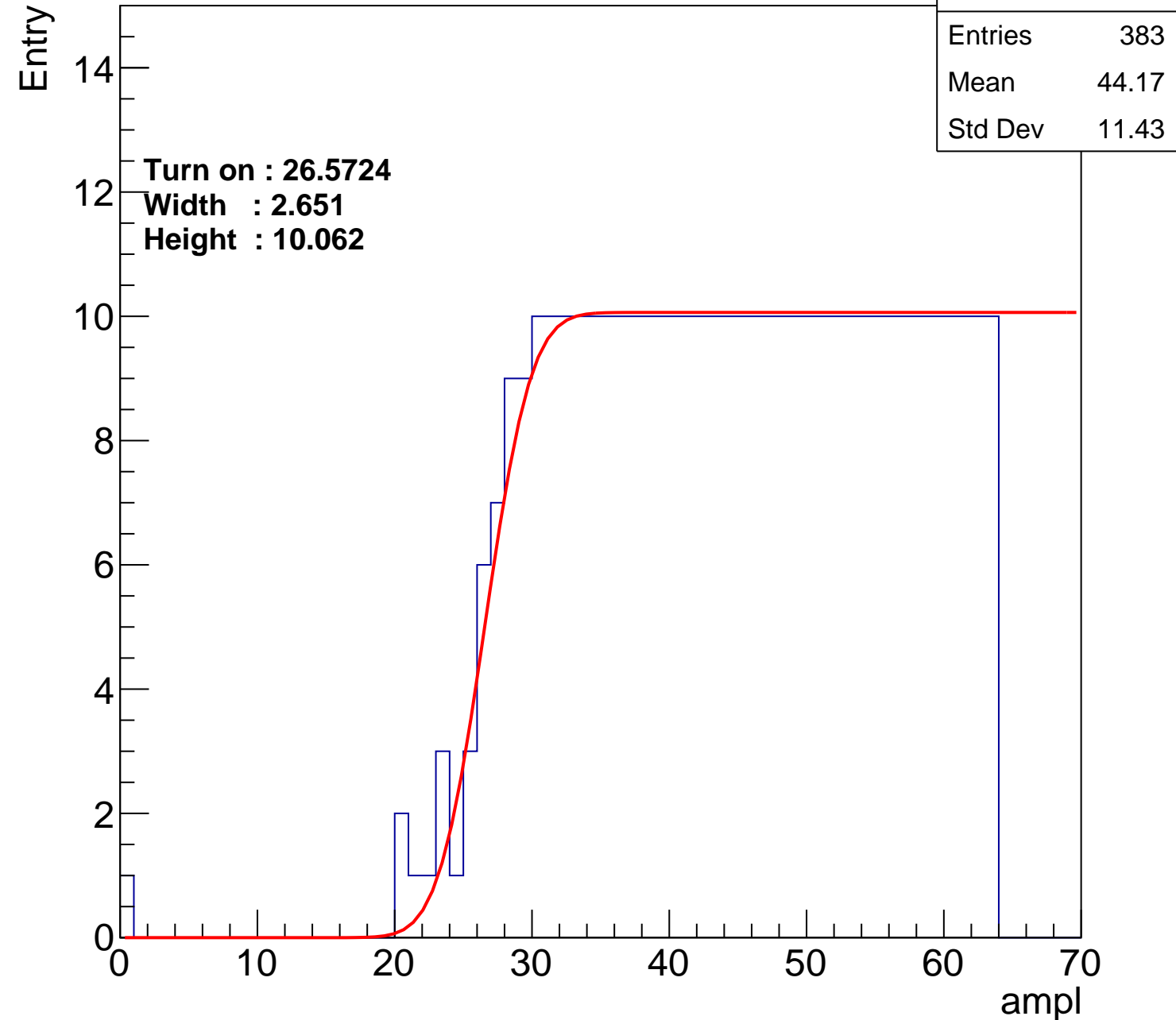
Width : 2.651

Height : 10.062

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch85

calib\_packv5\_042523\_0143.root, FC#4, port A2

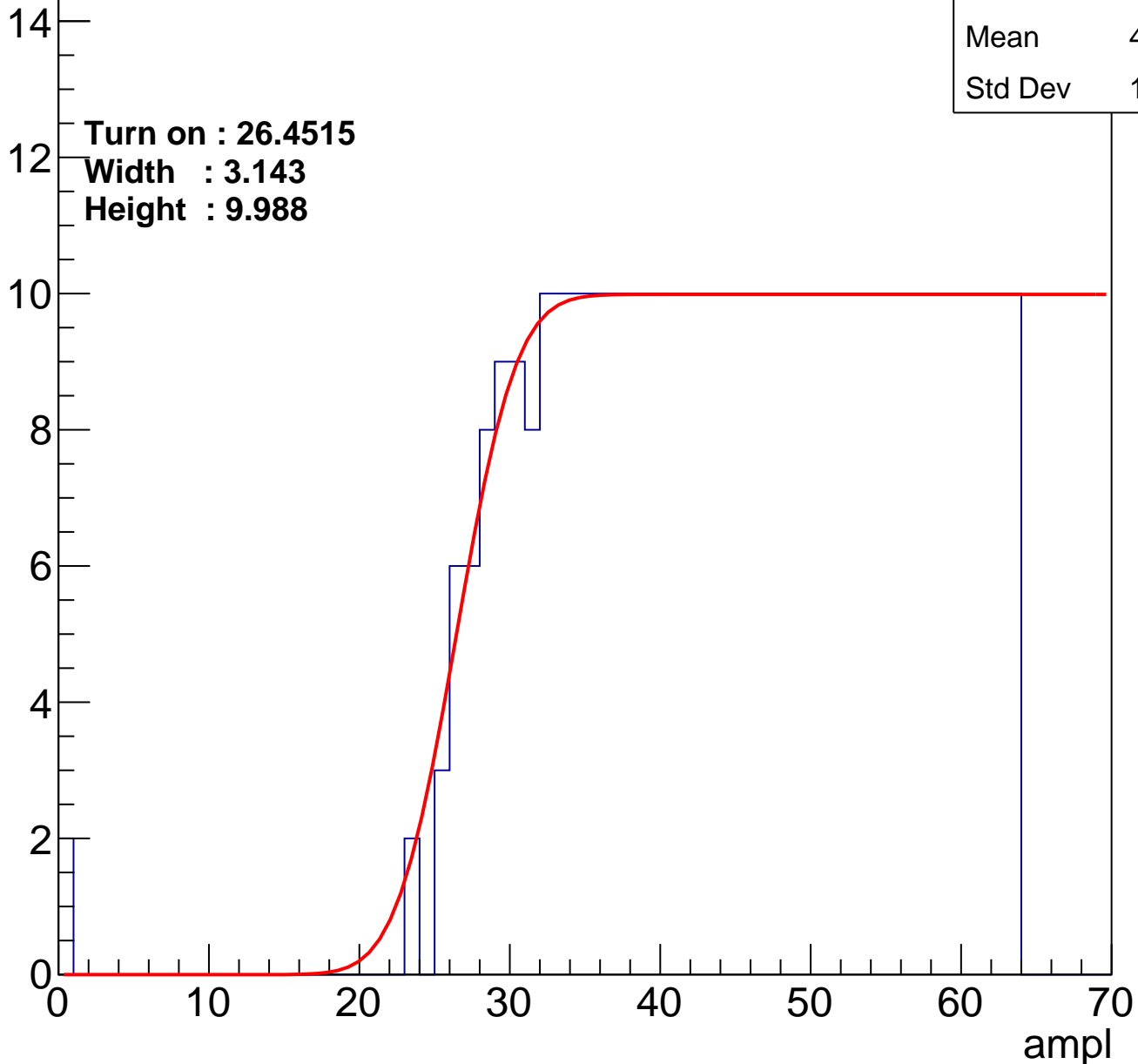
Entries	373
Mean	44.62
Std Dev	11.32

Turn on : 26.4515

Width : 3.143

Height : 9.988

Entry



# B1L100S, U16-ch86

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	386
Mean	43.7
Std Dev	12.36

Turn on : 26.6238

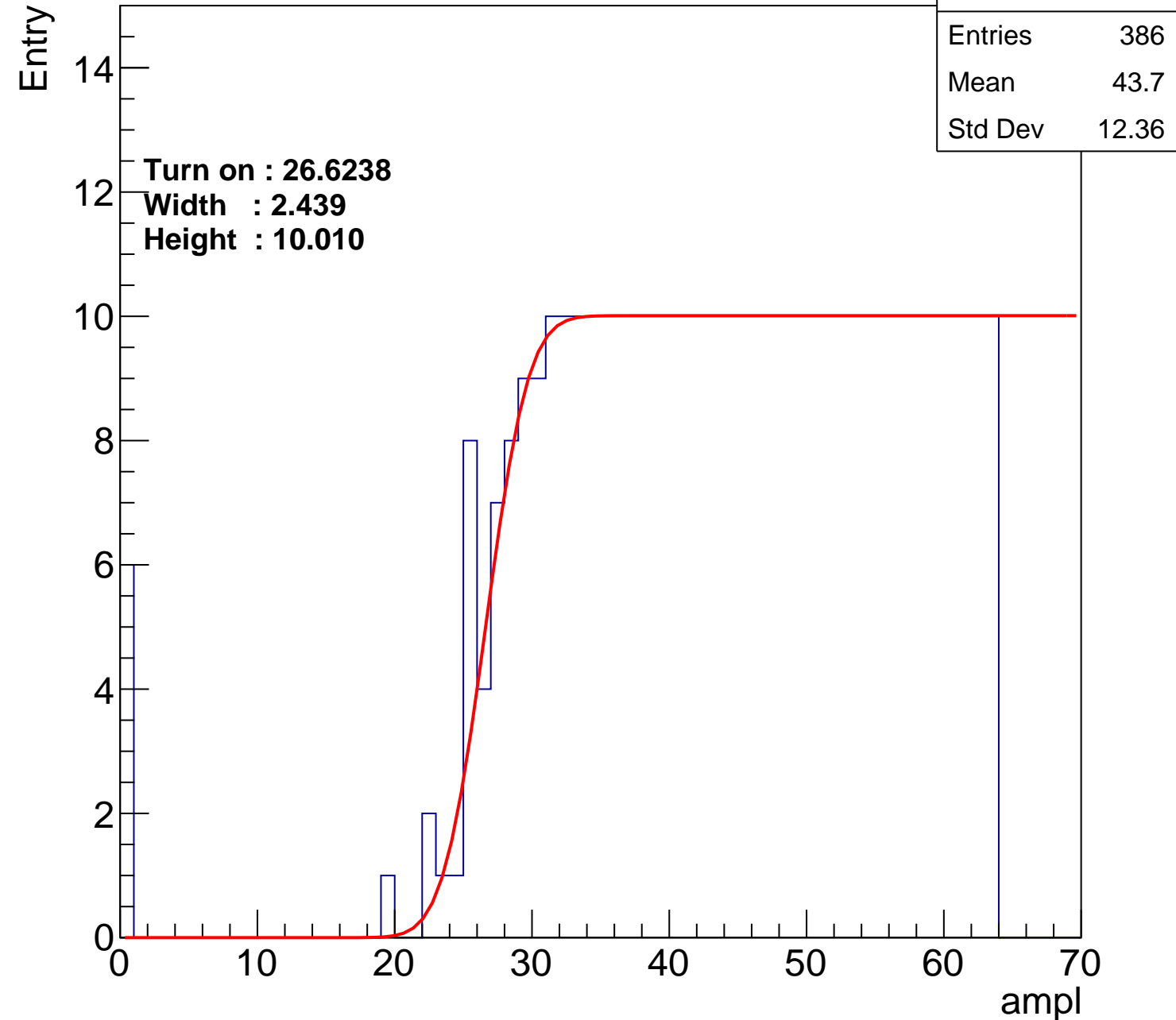
Width : 2.439

Height : 10.010

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L100S, U16-ch87

calib\_packv5\_042523\_0143.root, FC#4, port A2

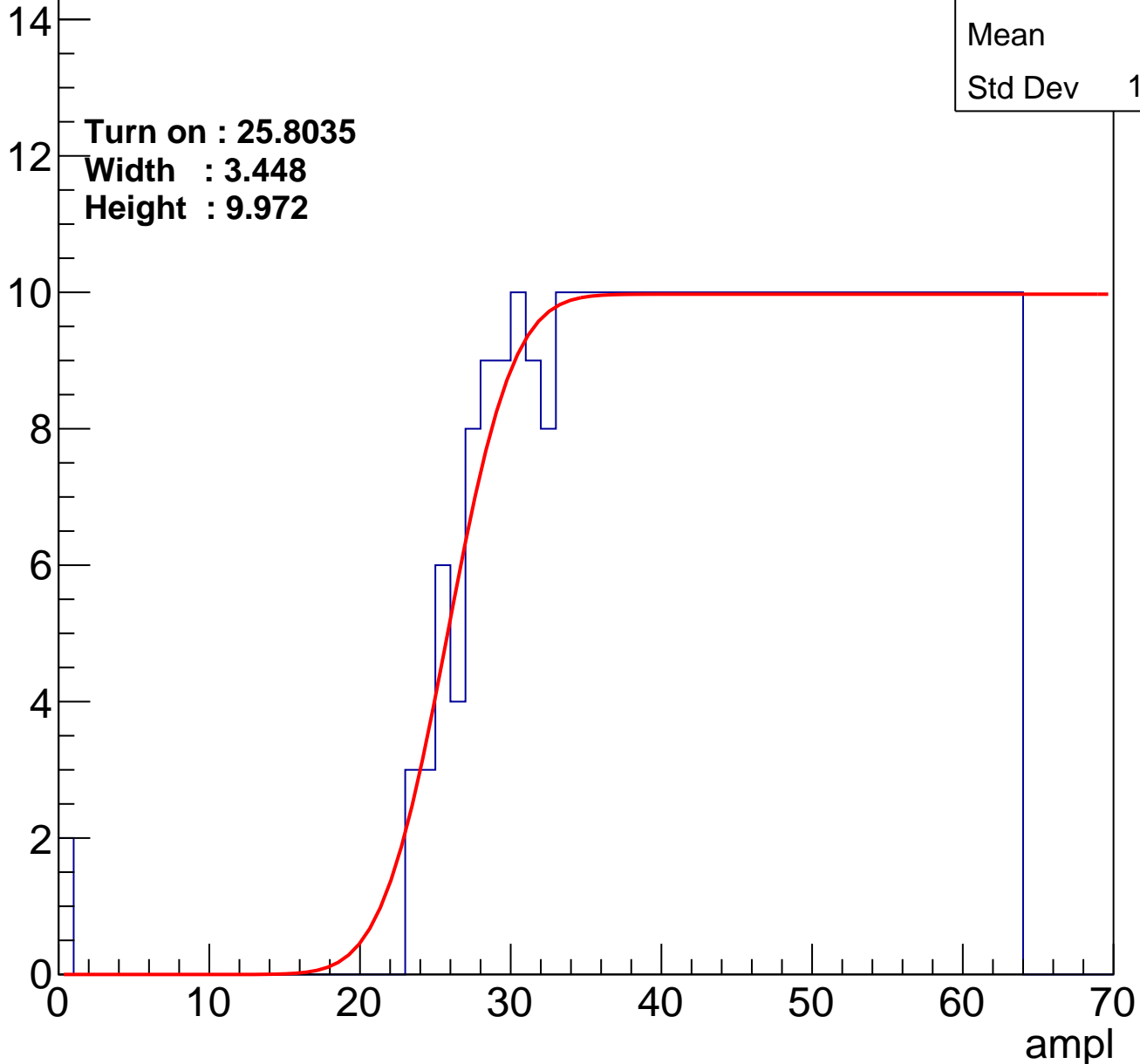
Entries	381
Mean	44.2
Std Dev	11.56

Turn on : 25.8035

Width : 3.448

Height : 9.972

Entry



# B1L100S, U16-ch88

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	389
Mean	43.74
Std Dev	11.95

**Turn on : 25.9098**

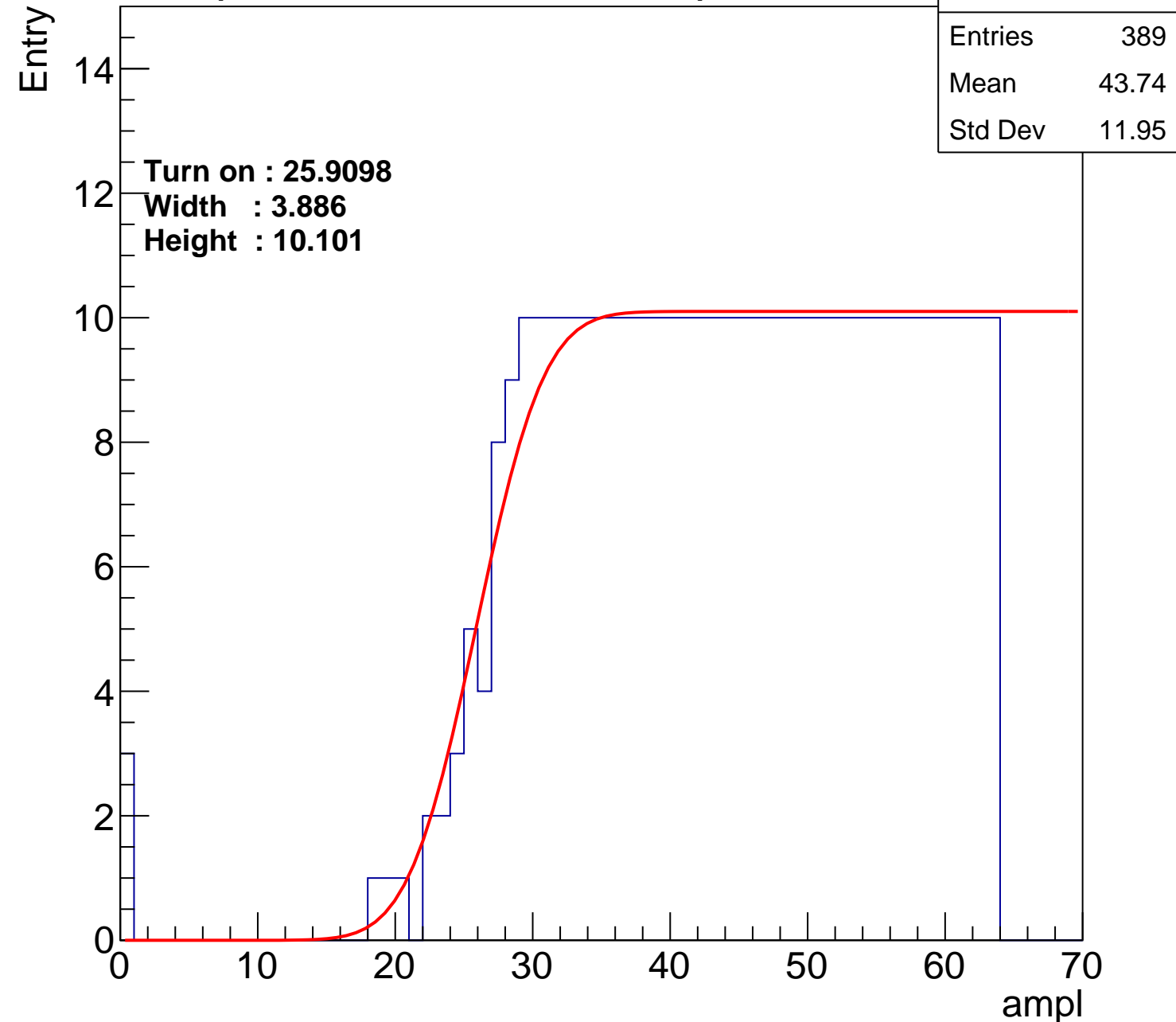
**Width : 3.886**

**Height : 10.101**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch89

calib\_packv5\_042523\_0143.root, FC#4, port A2

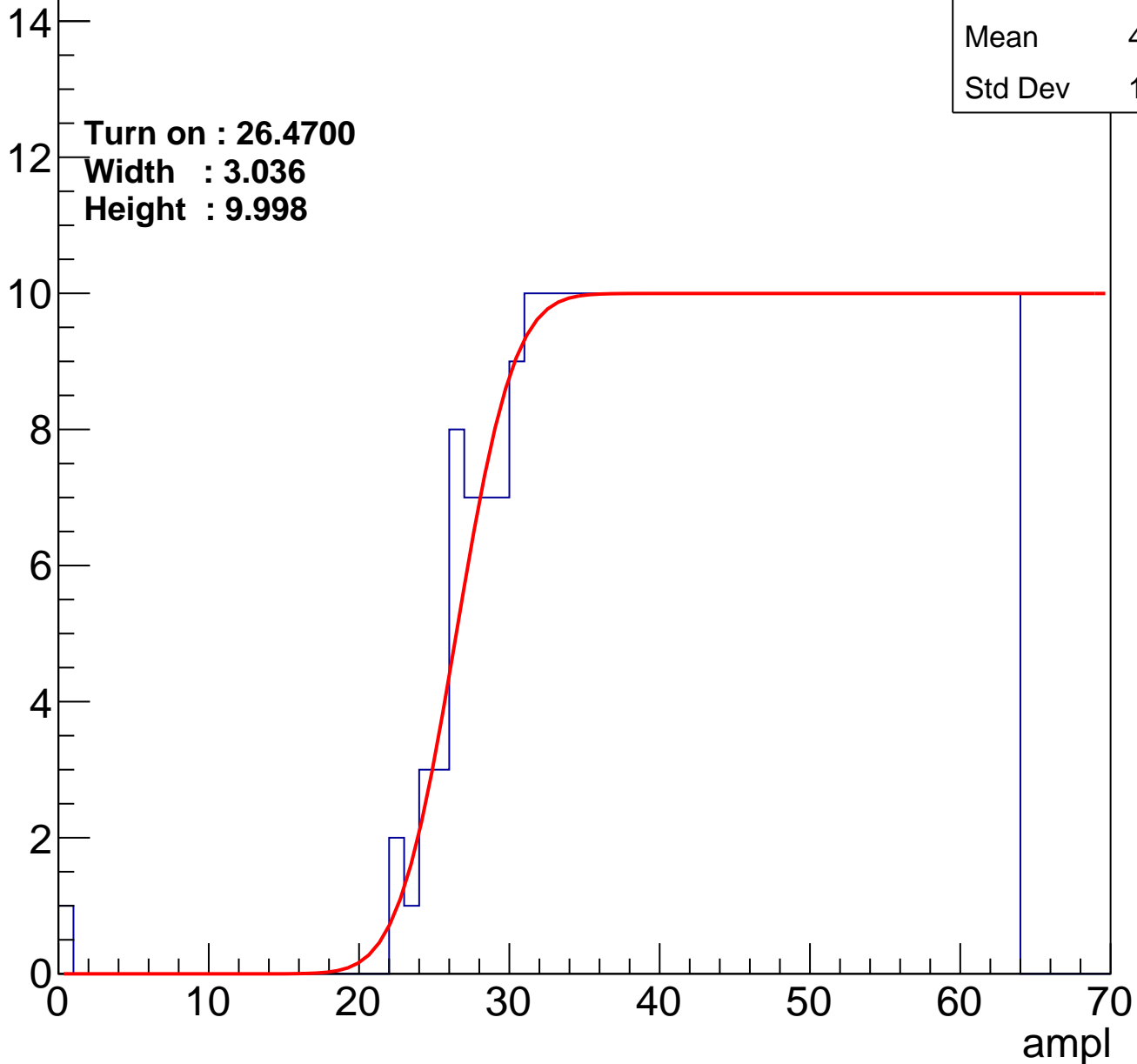
Entries	378
Mean	44.42
Std Dev	11.29

Turn on : 26.4700

Width : 3.036

Height : 9.998

Entry



# B1L100S, U16-ch90

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	384
Mean	44.07
Std Dev	11.62

**Turn on : 26.0183**

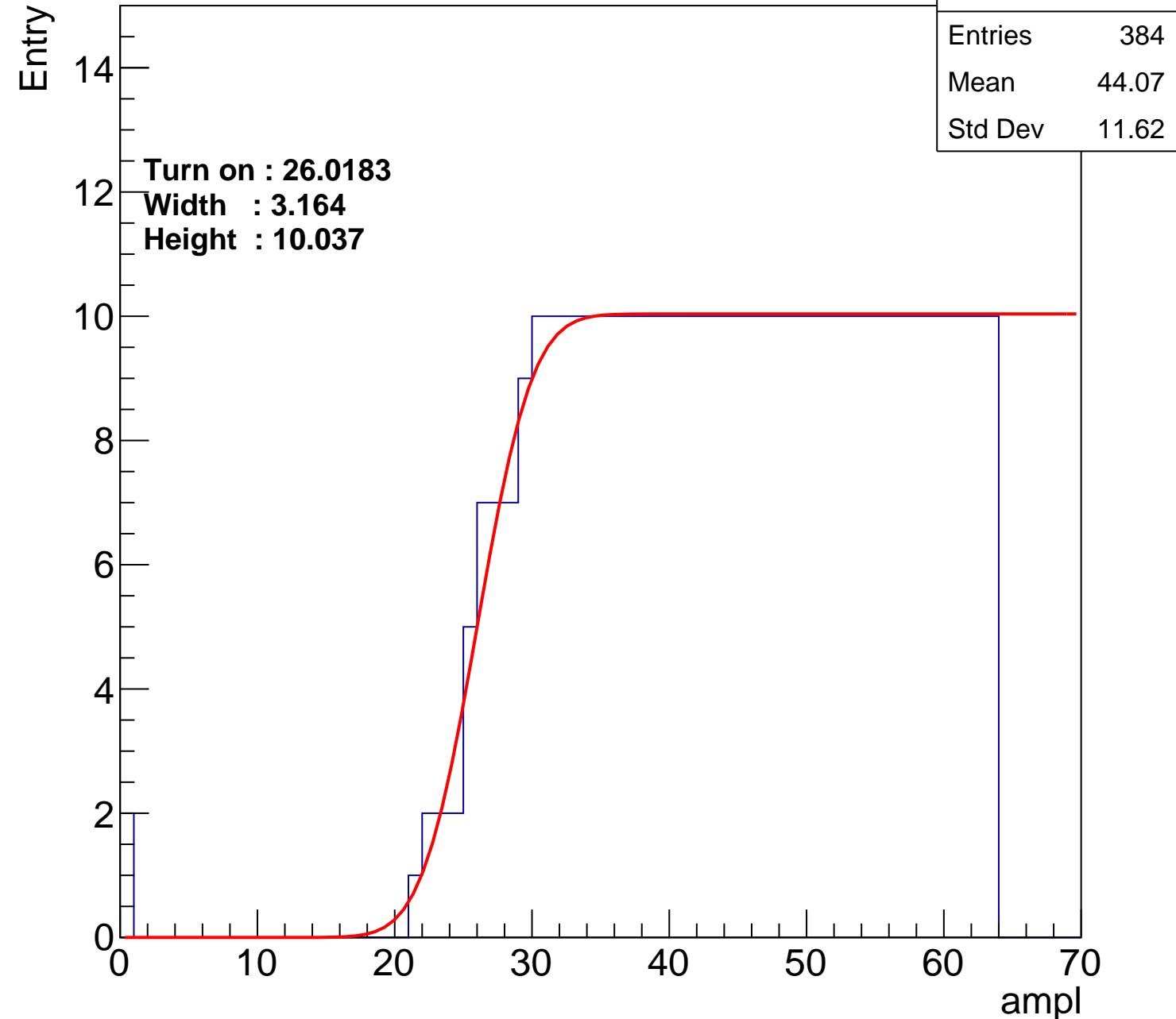
**Width : 3.164**

**Height : 10.037**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch91

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	360
Mean	45.25
Std Dev	11

**Turn on : 28.3970**

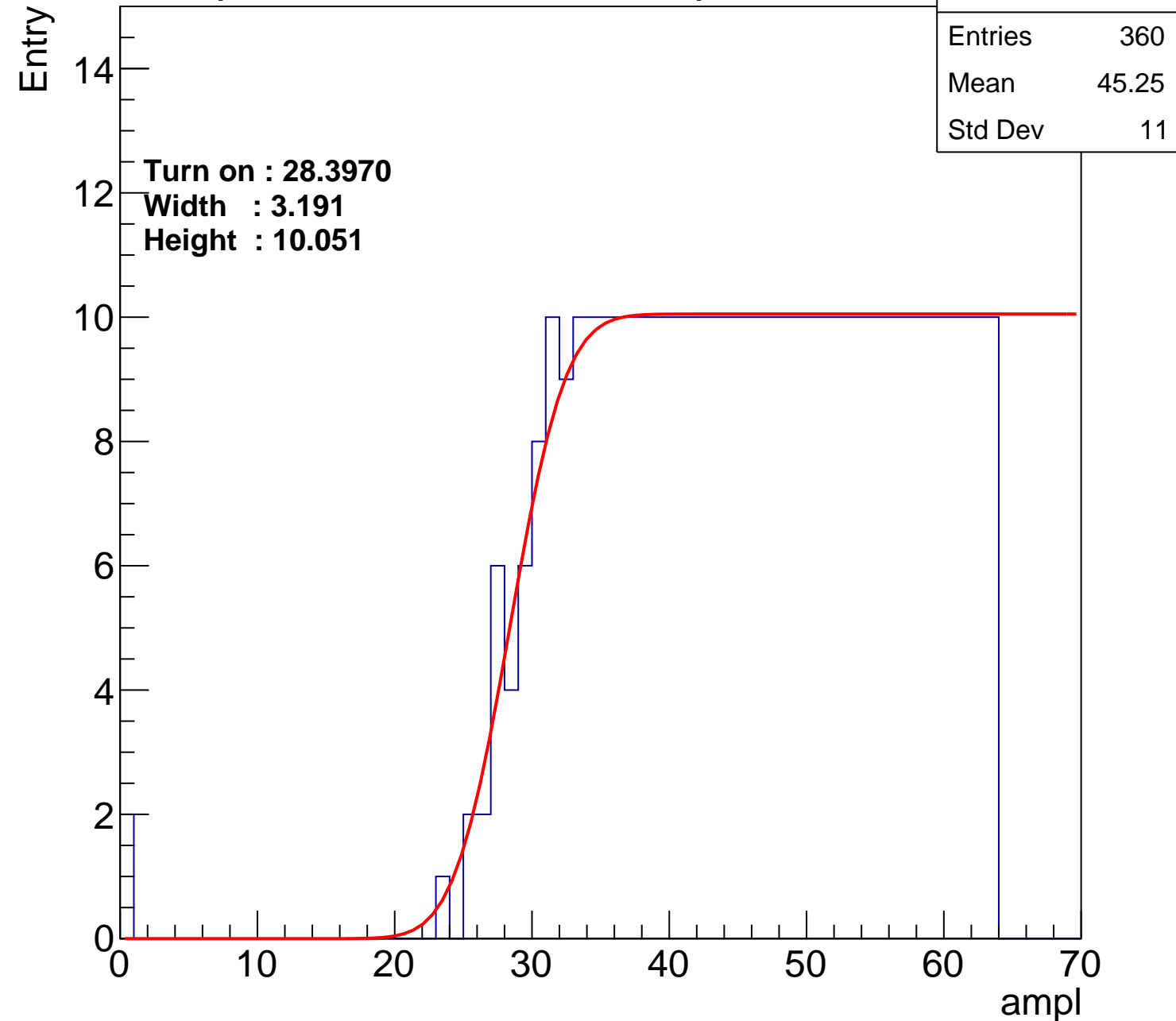
**Width : 3.191**

**Height : 10.051**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch92

calib\_packv5\_042523\_0143.root, FC#4, port A2

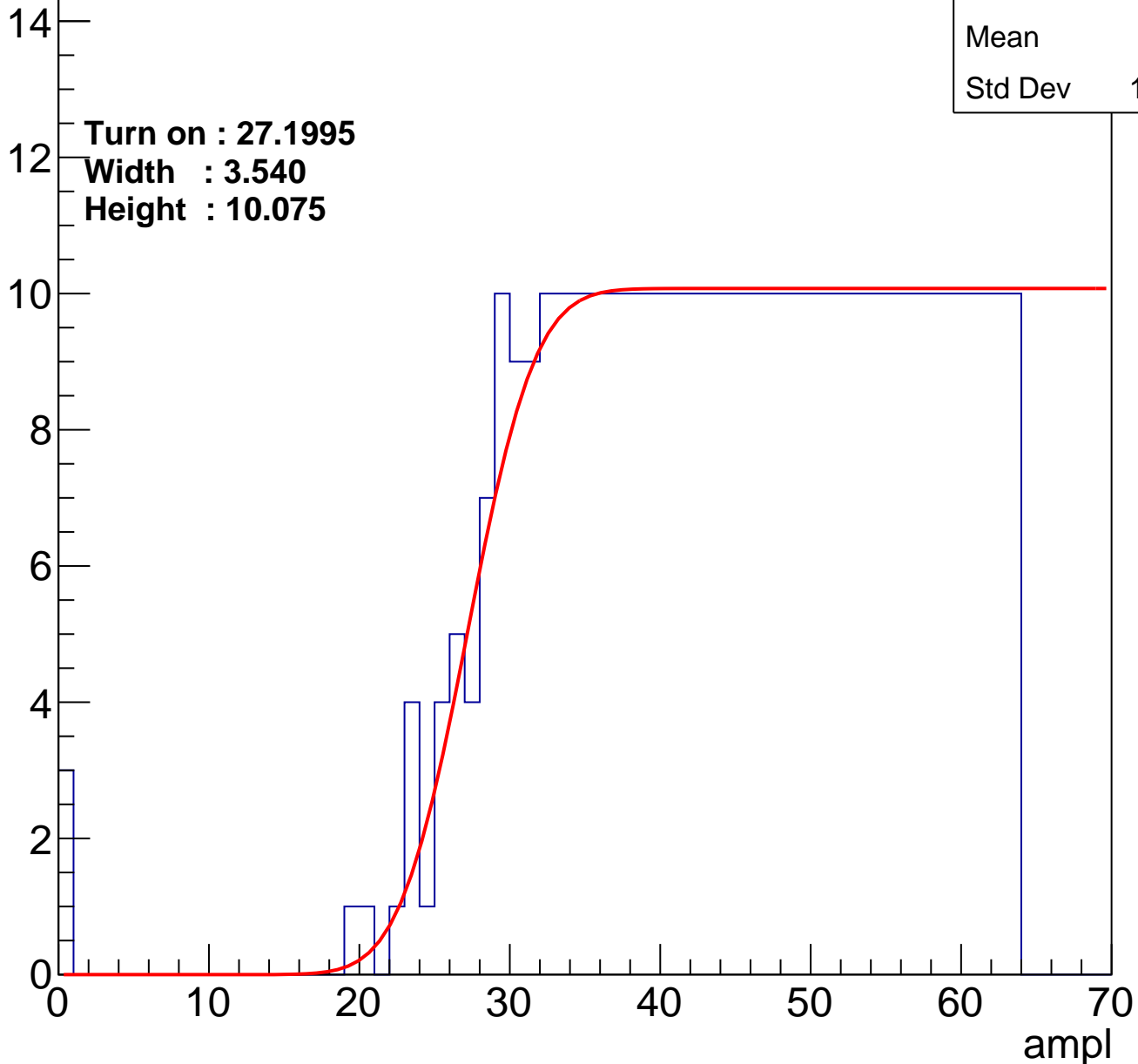
Entries	379
Mean	44.2
Std Dev	11.76

Turn on : 27.1995

Width : 3.540

Height : 10.075

Entry



# B1L100S, U16-ch93

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	373
Mean	44.7
Std Dev	11.1

Turn on : 26.8453

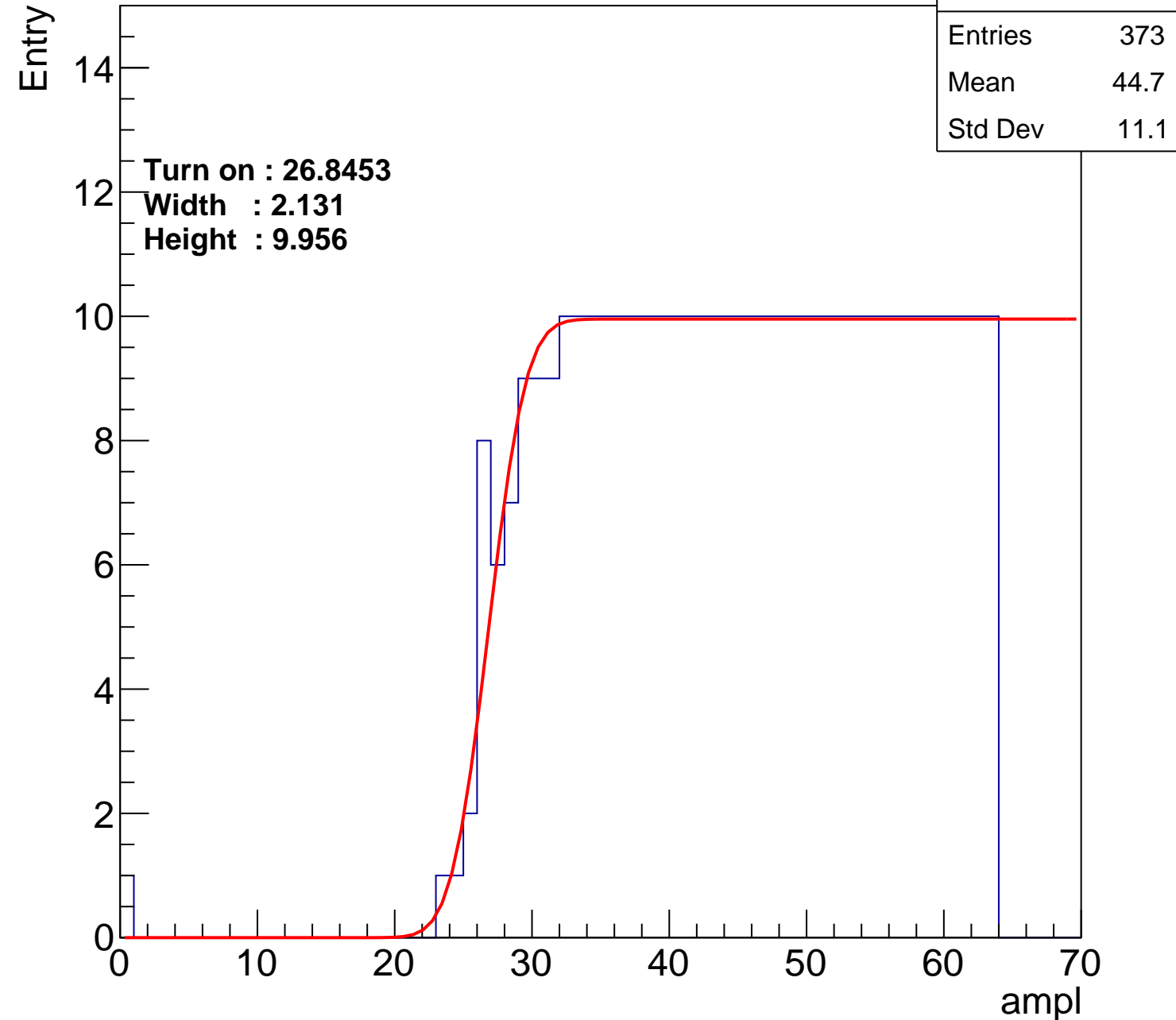
Width : 2.131

Height : 9.956

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch94

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	395
Mean	43.52
Std Dev	11.97

Turn on : 25.1295

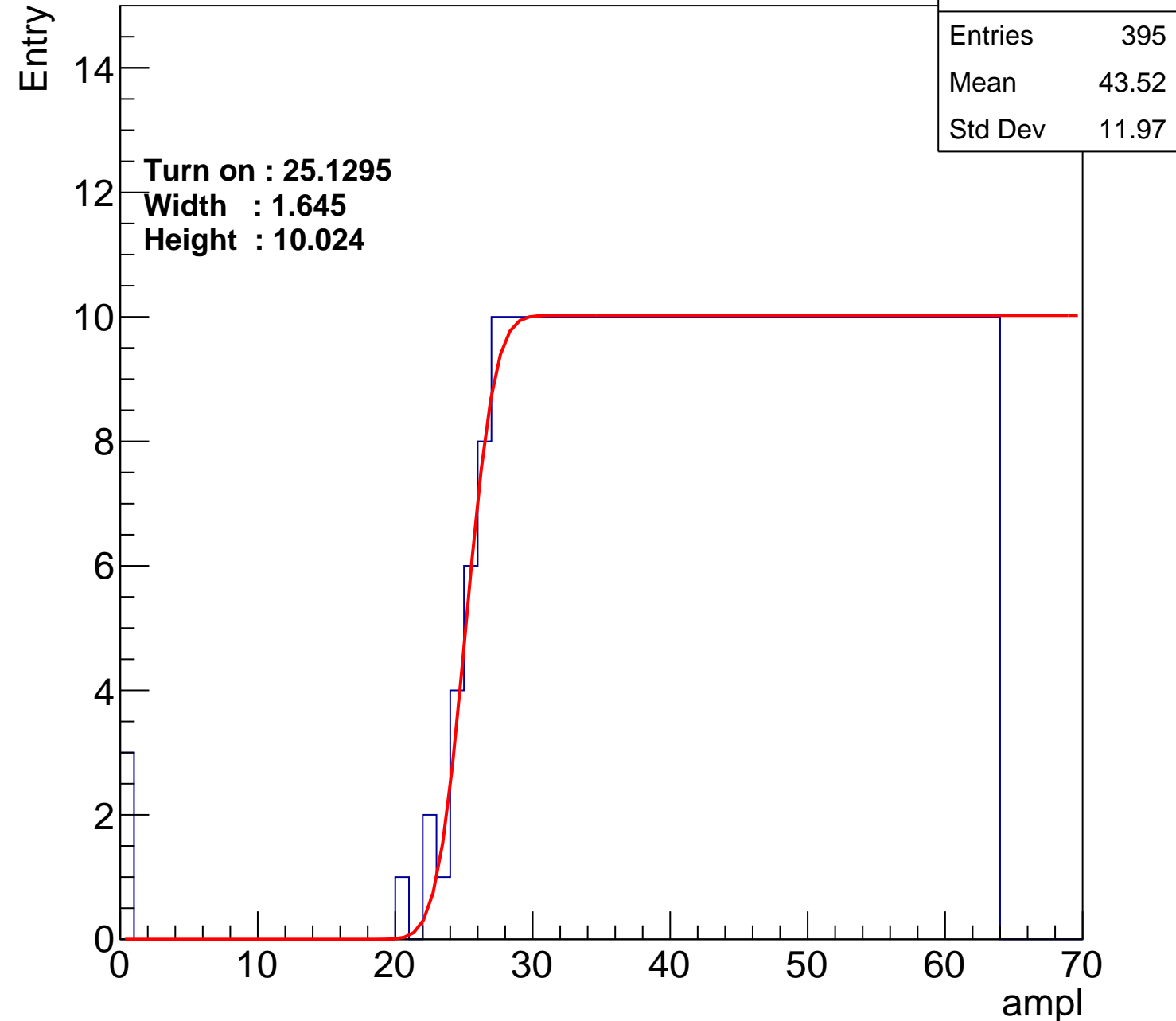
Width : 1.645

Height : 10.024

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L100S, U16-ch95

calib\_packv5\_042523\_0143.root, FC#4, port A2

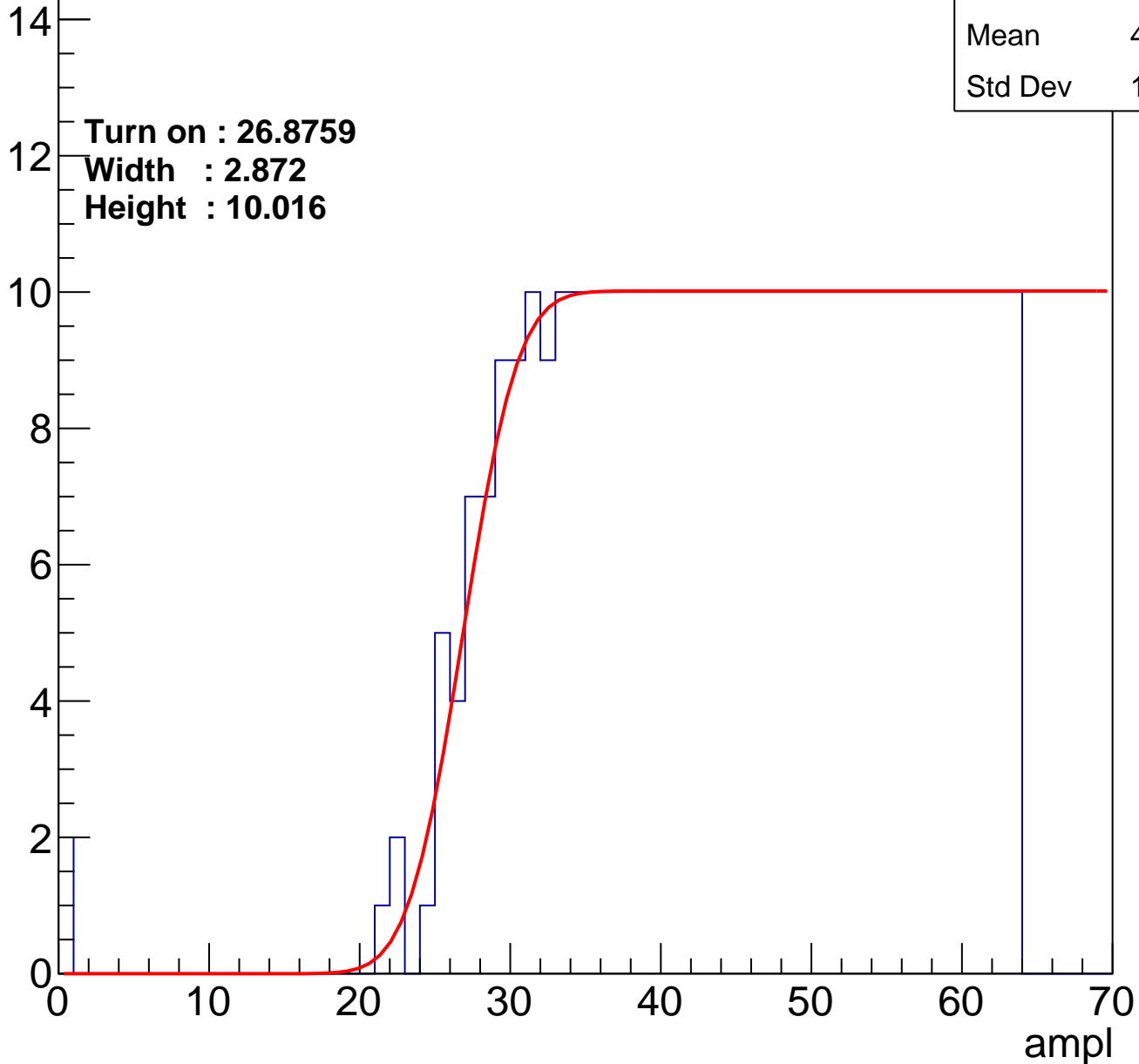
Entries	376
Mean	44.45
Std Dev	11.43

Turn on : 26.8759

Width : 2.872

Height : 10.016

Entry



# B1L100S, U16-ch96

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	398
Mean	43.42
Std Dev	12.05

Turn on : 24.8737

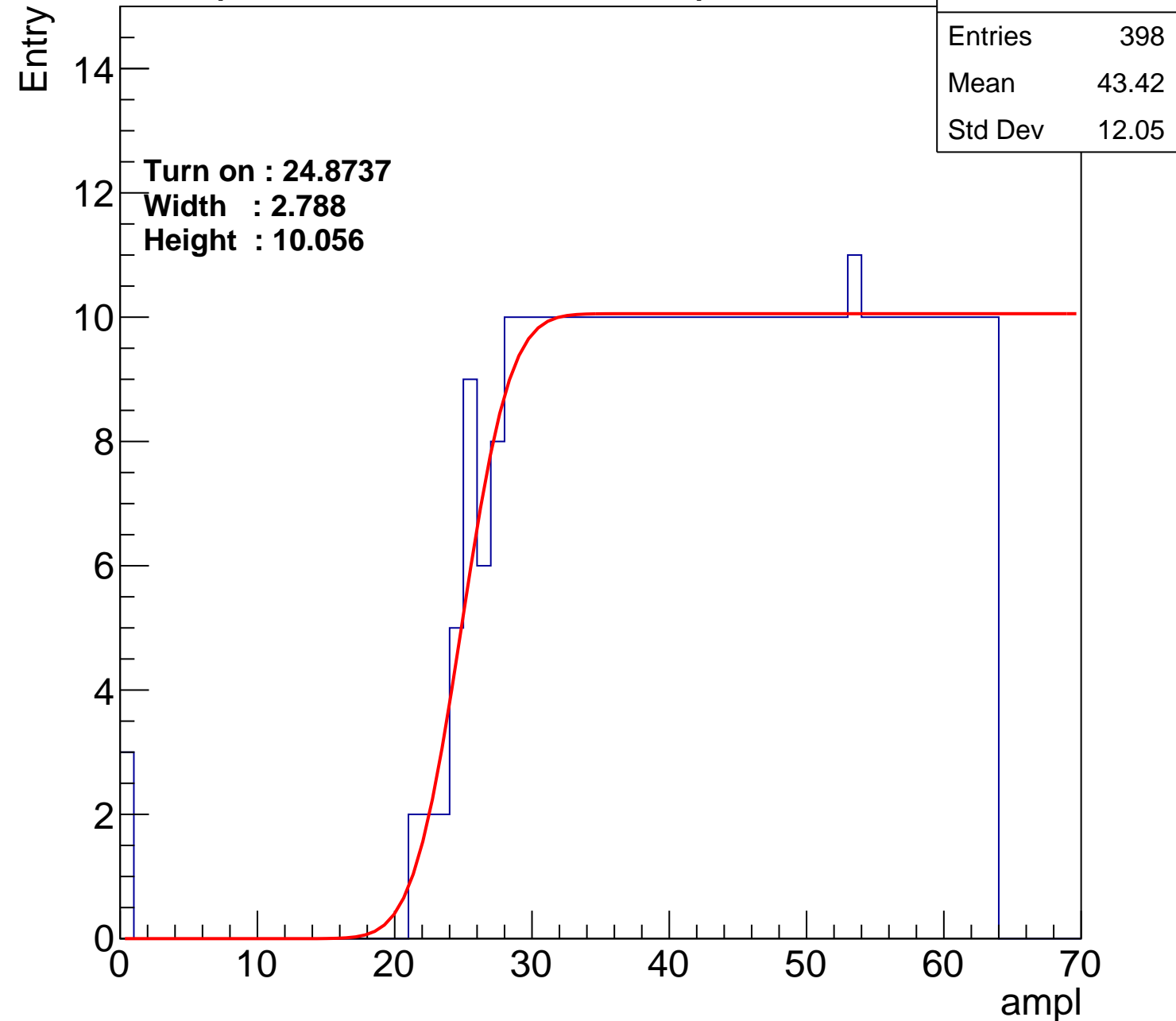
Width : 2.788

Height : 10.056

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch97

calib\_packv5\_042523\_0143.root, FC#4, port A2

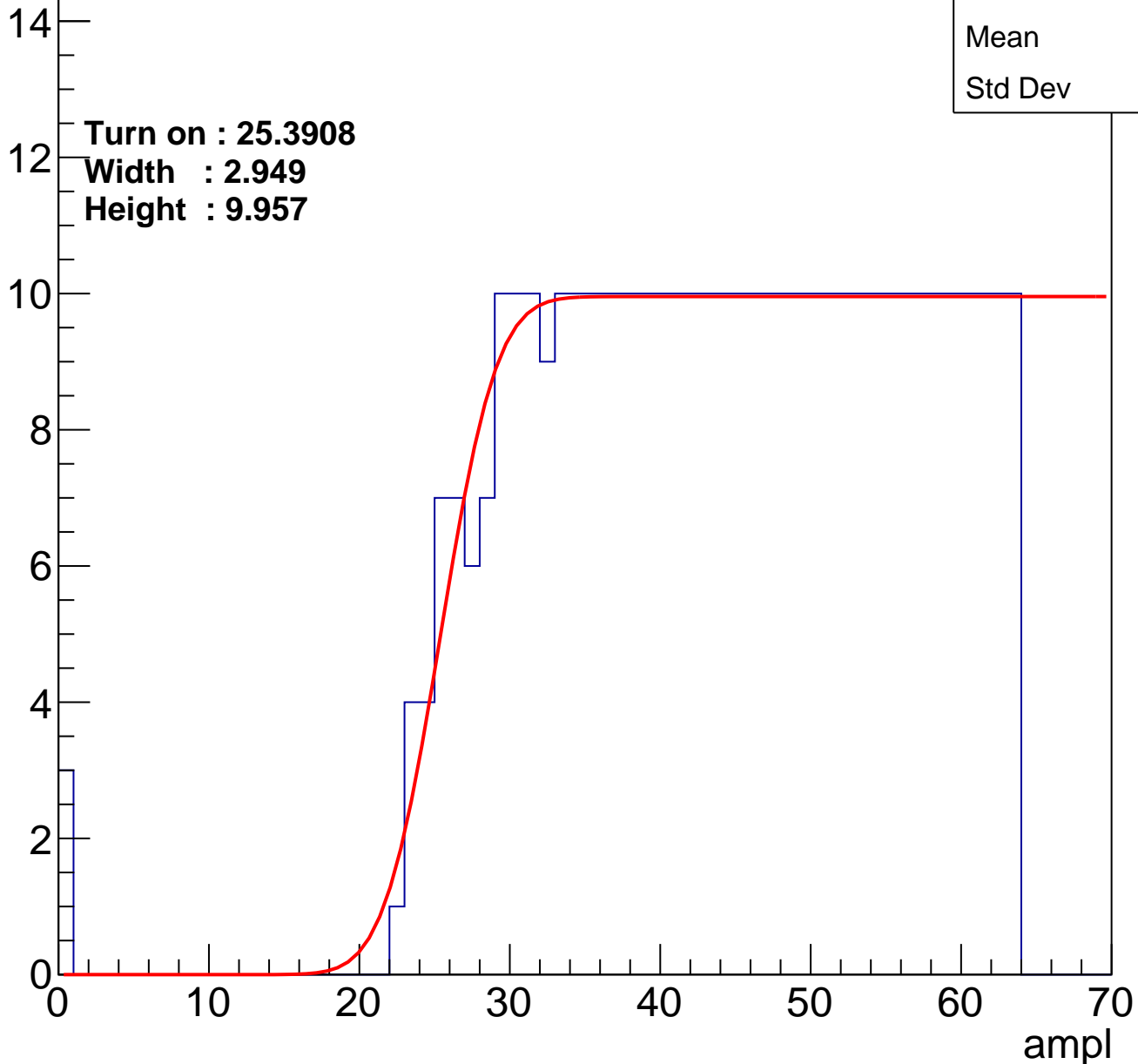
Entries	388
Mean	43.8
Std Dev	11.9

Turn on : 25.3908

Width : 2.949

Height : 9.957

Entry



**calib\_packv5\_042523\_0143.root, FC#4, port A2**

**calib\_packv5\_042523\_0143.root, FC#4, port A2**

Turn on : 25.8004  
Width : 1.405  
Height : 9.837



# B1L100S, U16-ch99

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	389
Mean	43.77
Std Dev	11.9

Turn on : 25.9606

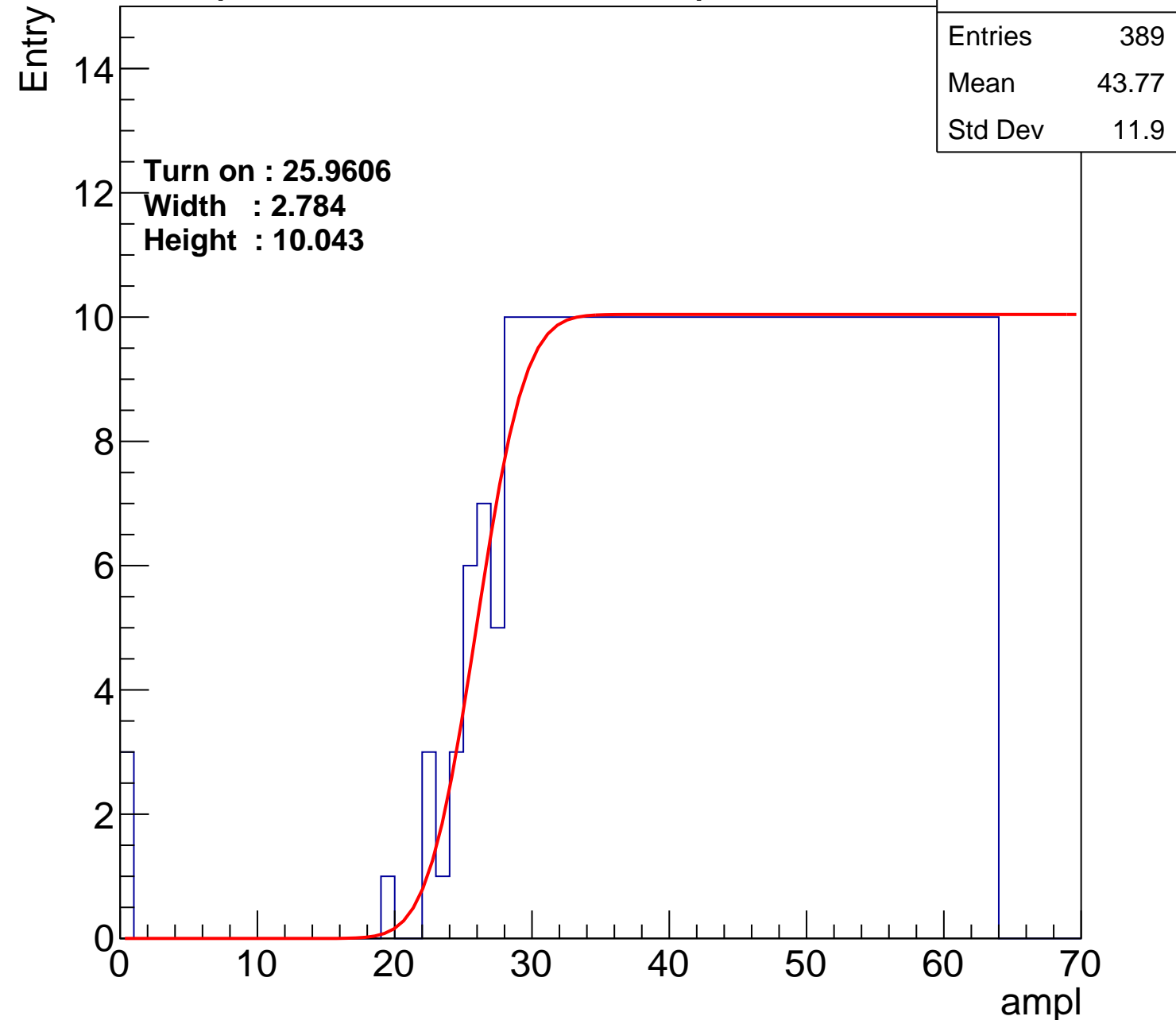
Width : 2.784

Height : 10.043

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch100

calib\_packv5\_042523\_0143.root, FC#4, port A2

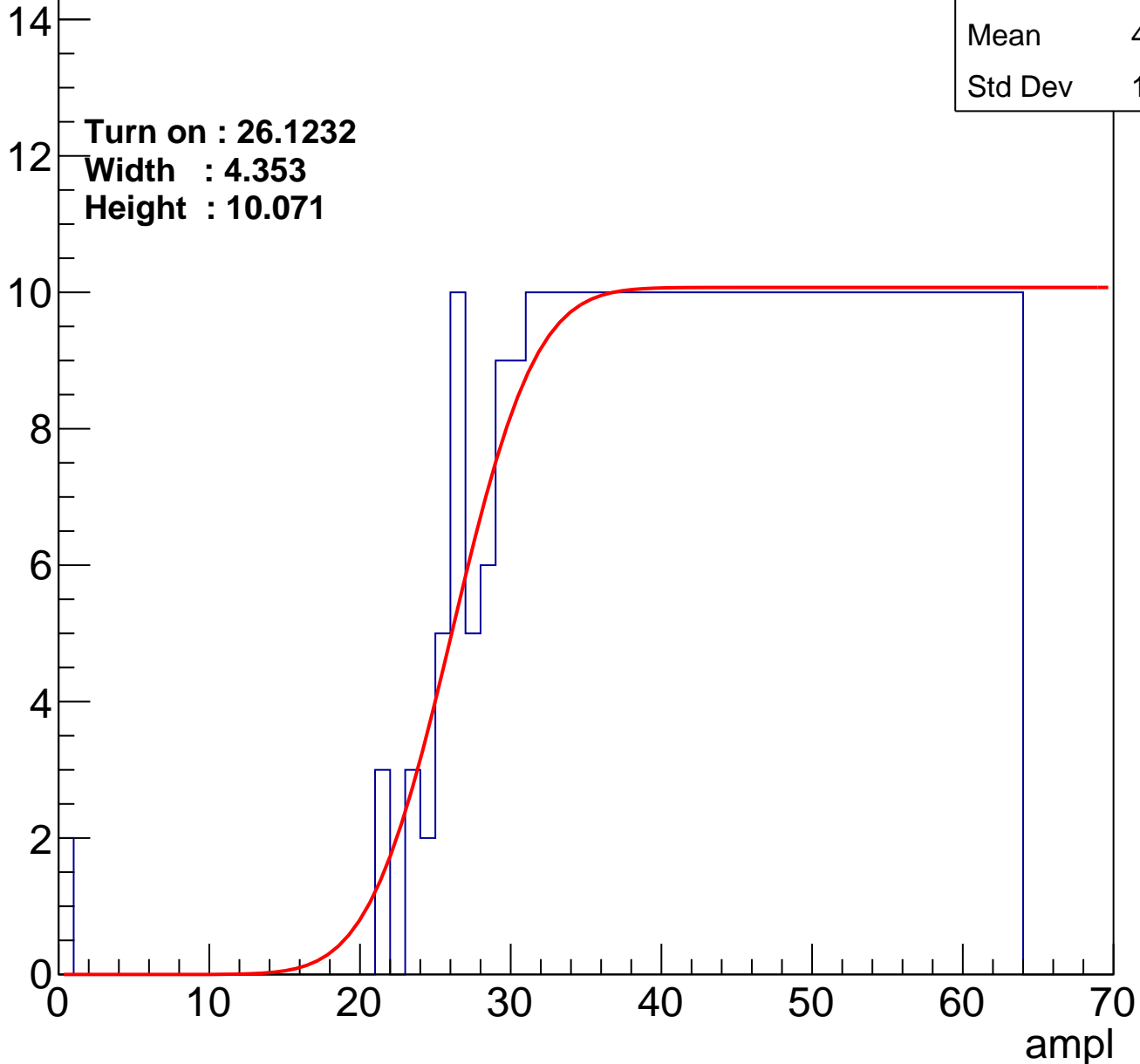
Entries	384
Mean	44.03
Std Dev	11.67

Turn on : 26.1232

Width : 4.353

Height : 10.071

Entry



# B1L100S, U16-ch101

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	391
Mean	43.69
Std Dev	11.85

Turn on : 25.9619

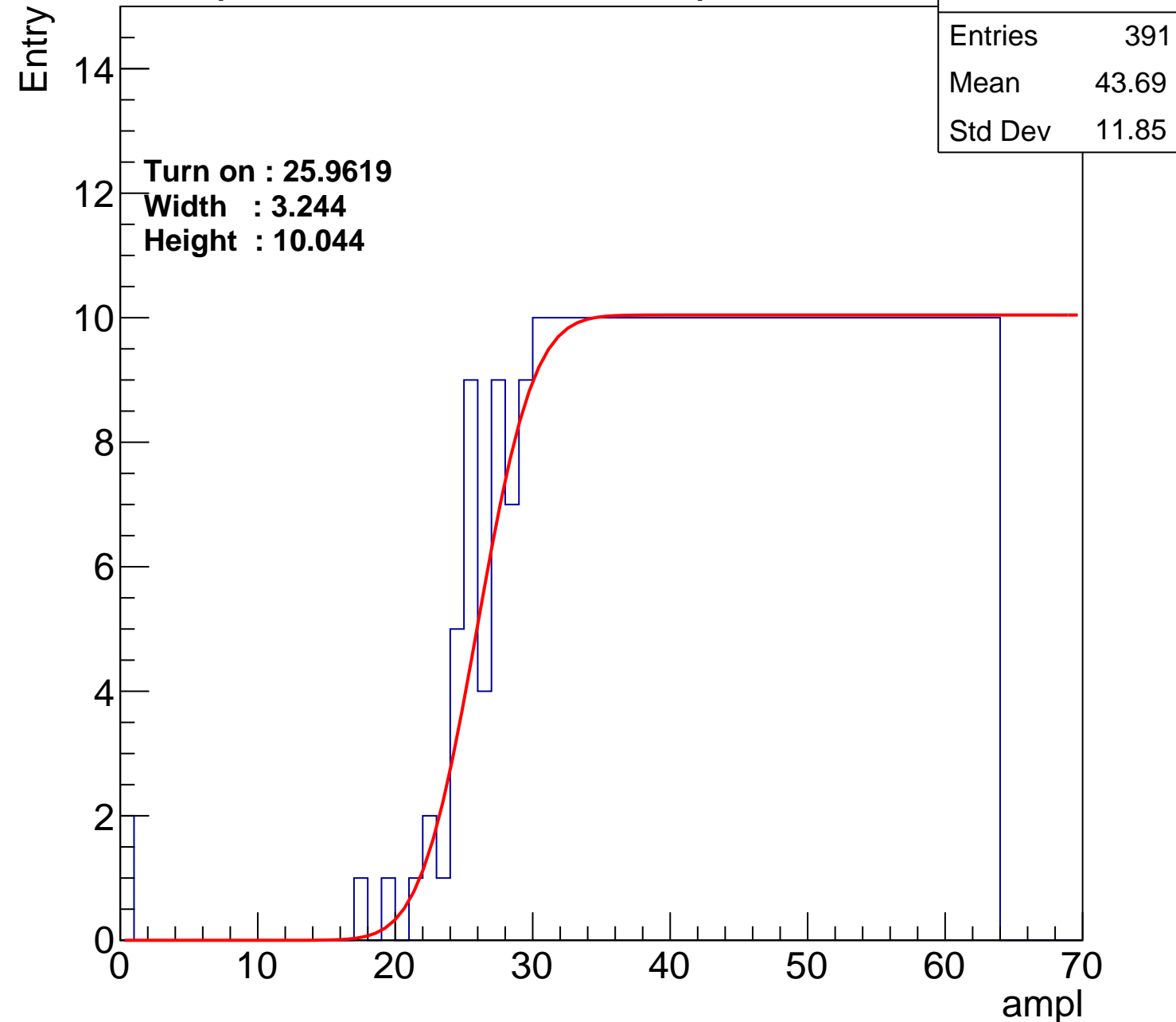
Width : 3.244

Height : 10.044

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch102

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	361
Mean	45.26
Std Dev	10.84

**Turn on : 28.3803**

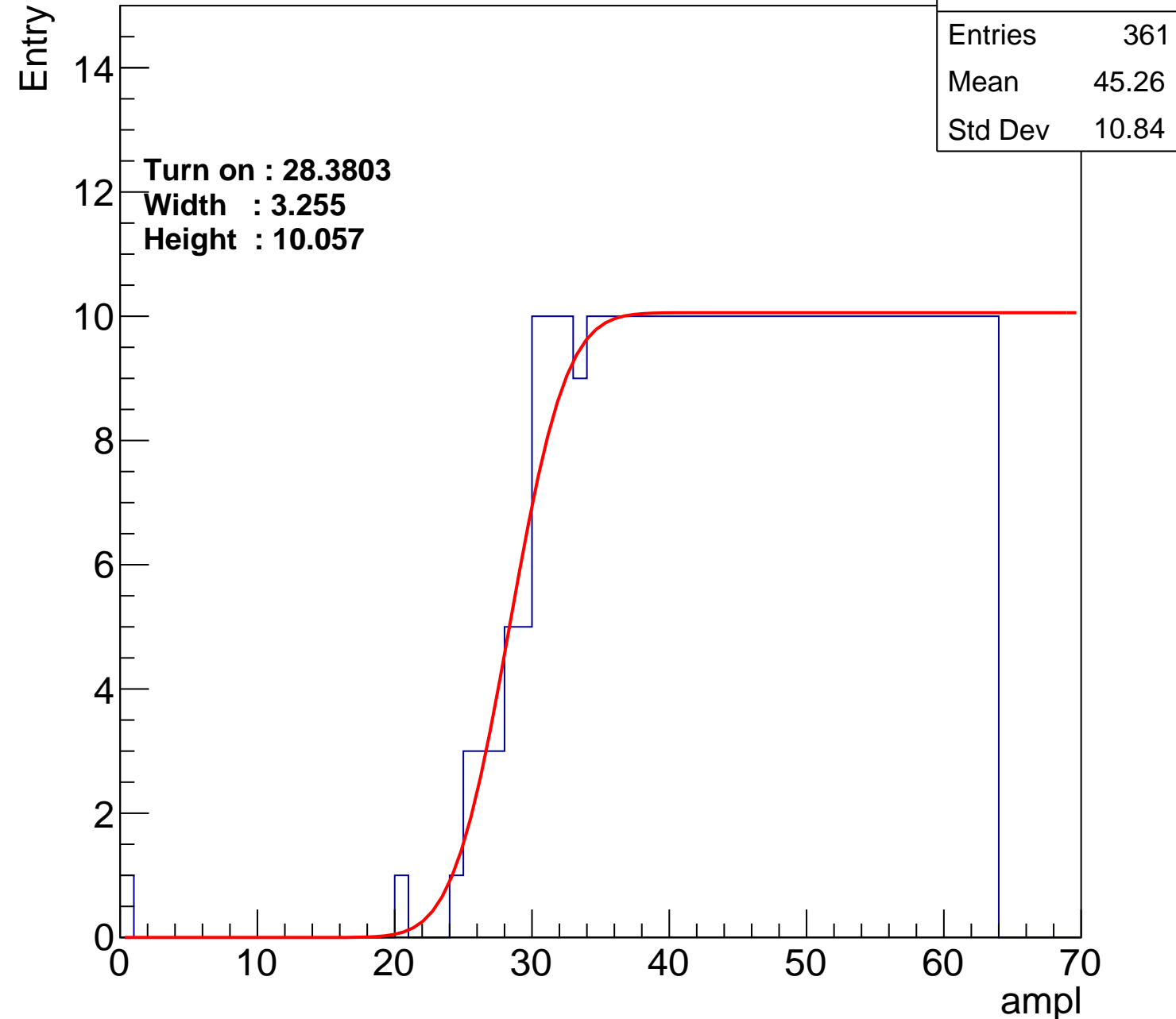
**Width : 3.255**

**Height : 10.057**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L100S, U16-ch103

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	389
Mean	43.84
Std Dev	11.71

Turn on : 25.1704

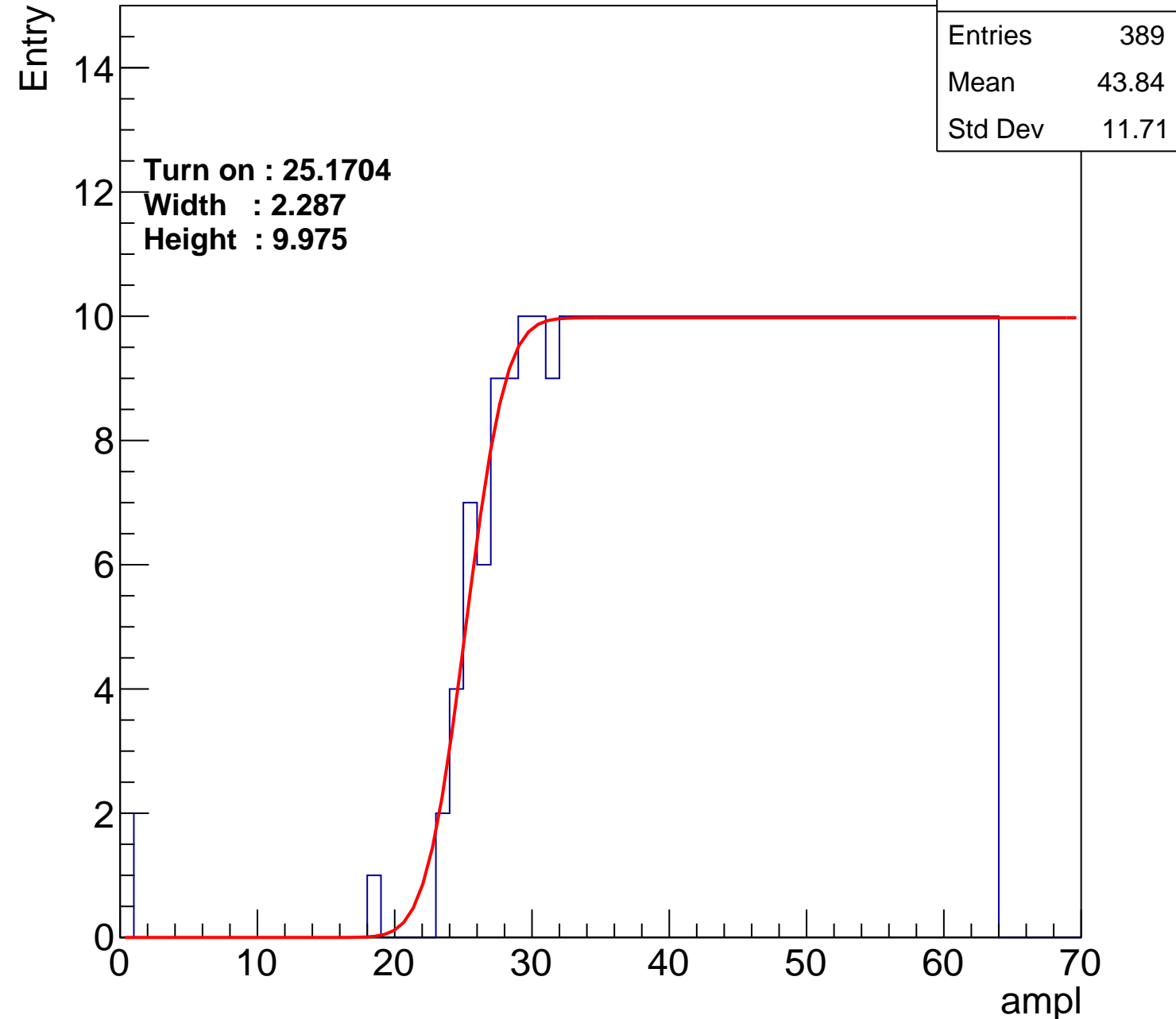
Width : 2.287

Height : 9.975

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch104

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	390
Mean	43.58
Std Dev	12.19

Turn on : 25.4090

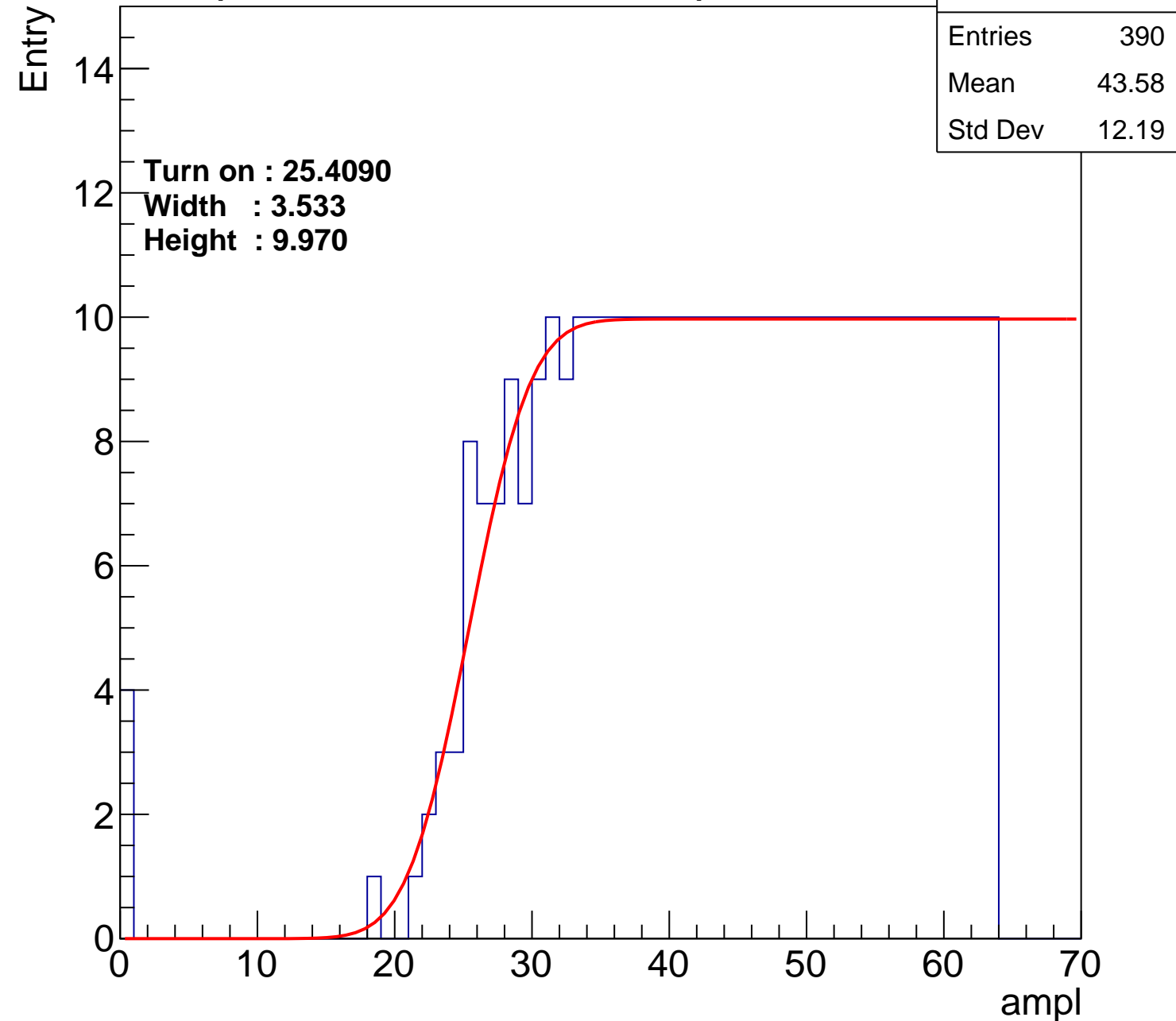
Width : 3.533

Height : 9.970

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch105

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	367
Mean	44.79
Std Dev	11.47

Turn on : 28.1293

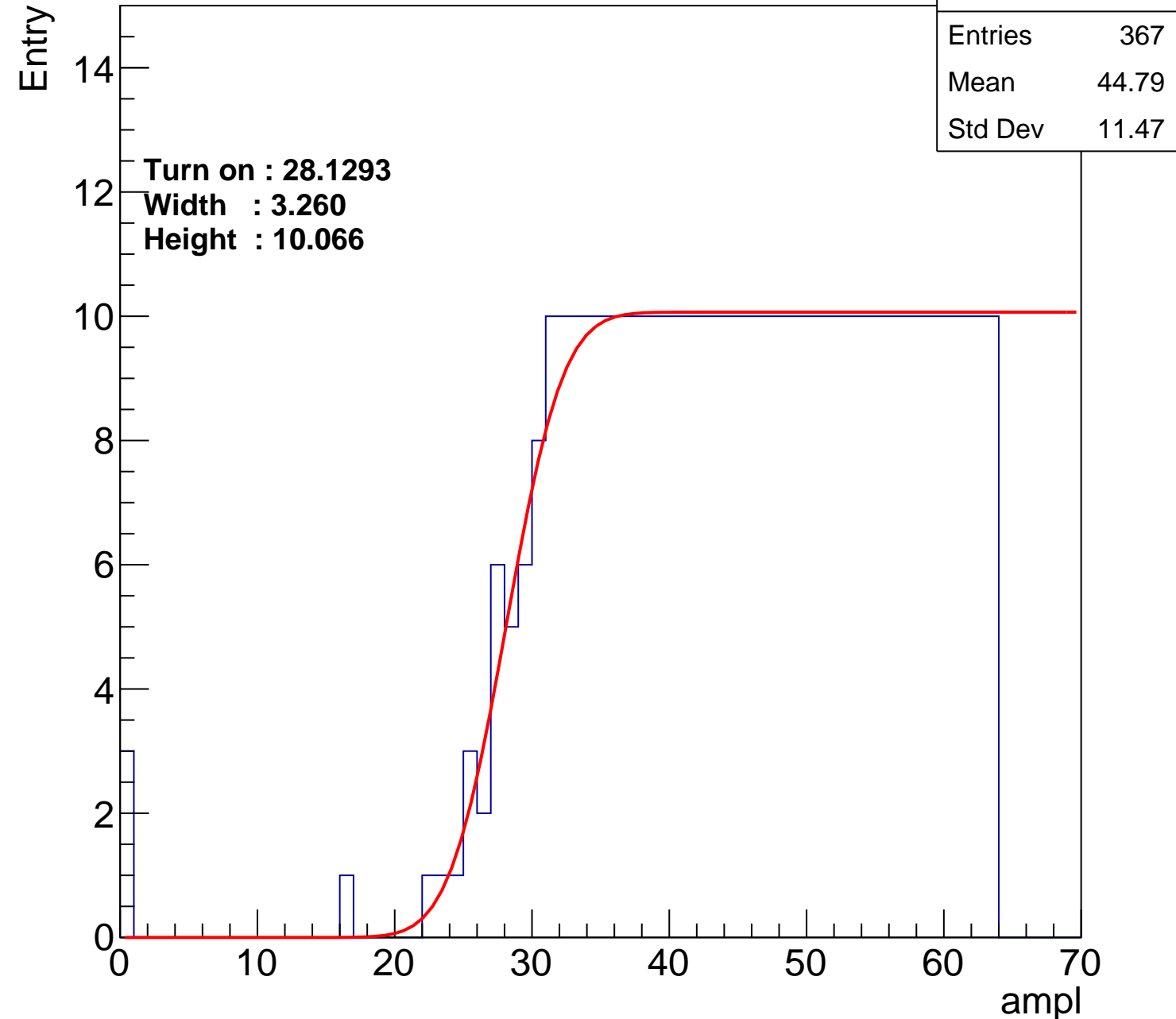
Width : 3.260

Height : 10.066

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch106

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	357
Mean	45.47
Std Dev	10.7

**Turn on : 28.6953**

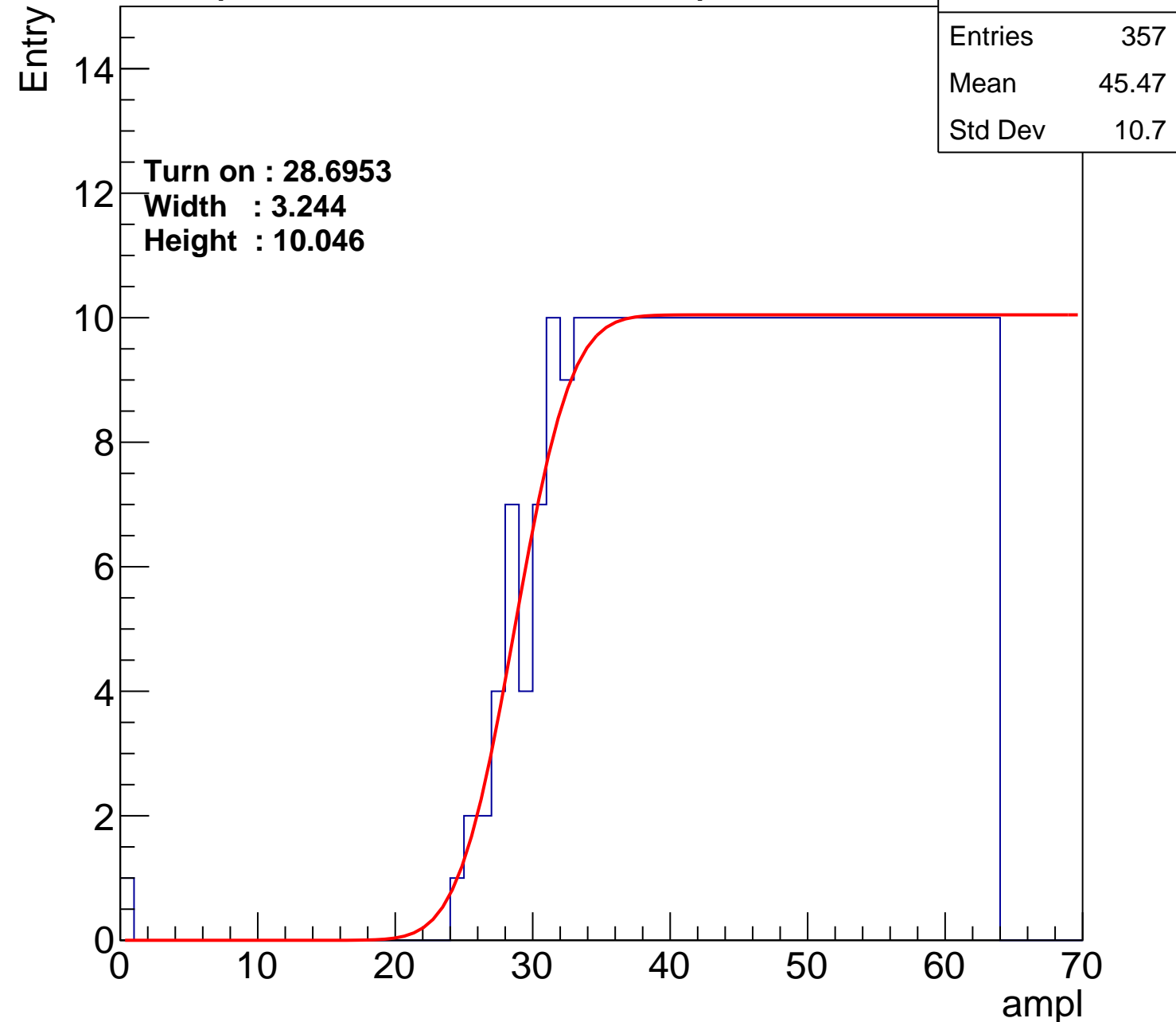
**Width : 3.244**

**Height : 10.046**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch107

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	377
Mean	44.41
Std Dev	11.45

**Turn on : 26.8062**

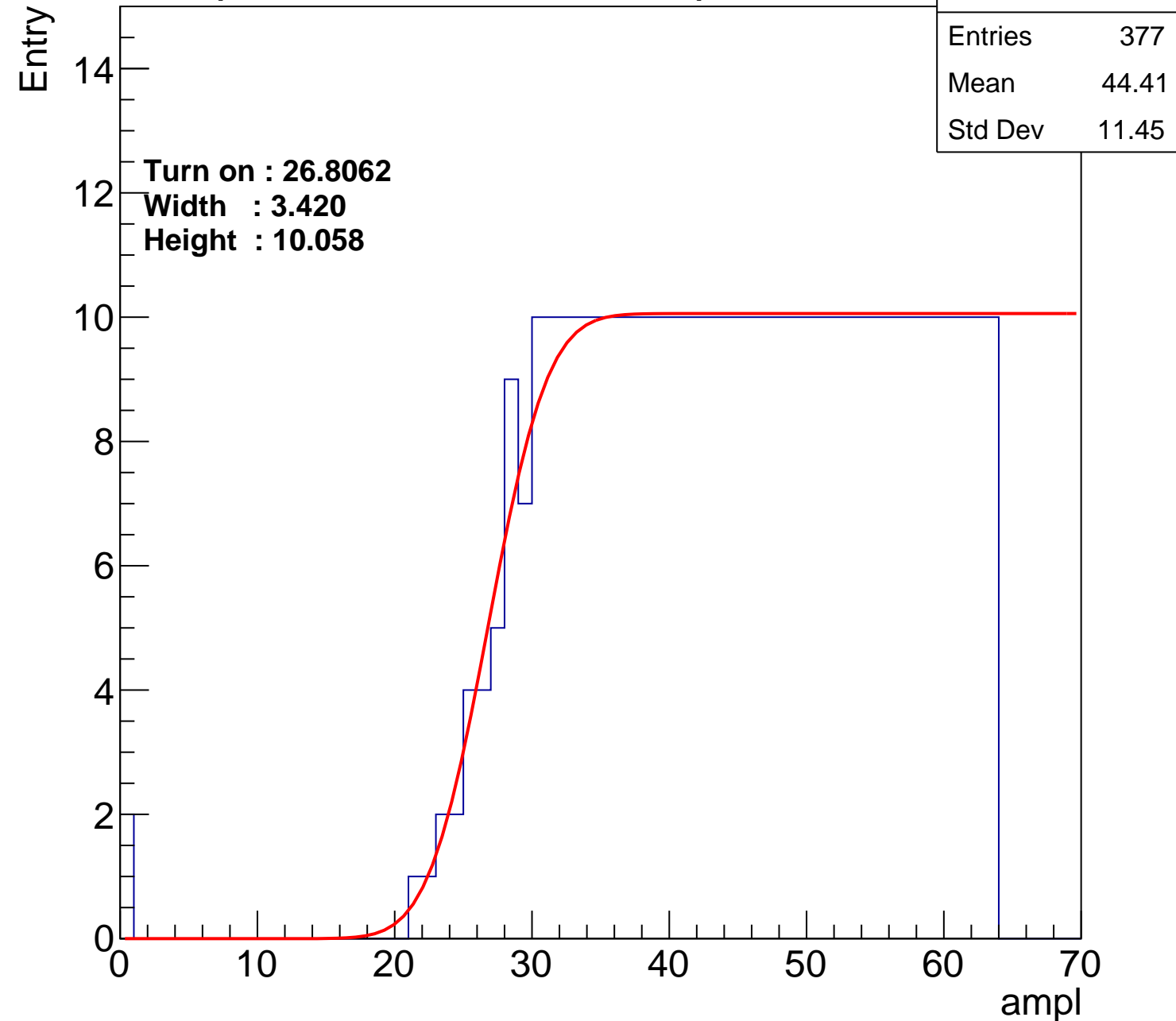
**Width : 3.420**

**Height : 10.058**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch108

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	396
Mean	43.45
Std Dev	12.03

Turn on : 24.8741

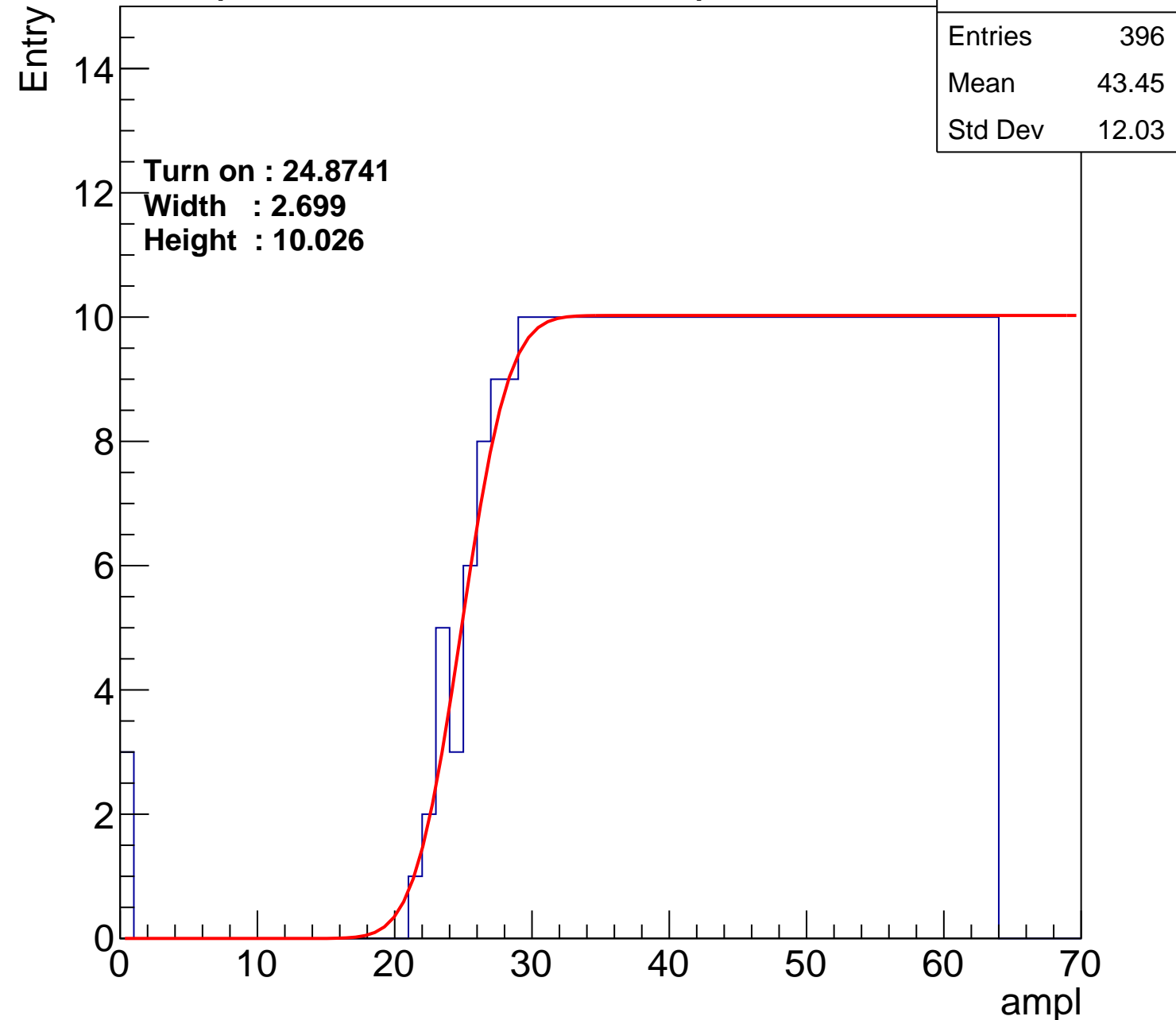
Width : 2.699

Height : 10.026

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch109

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	389
Mean	43.69
Std Dev	12.09

Turn on : 25.3841

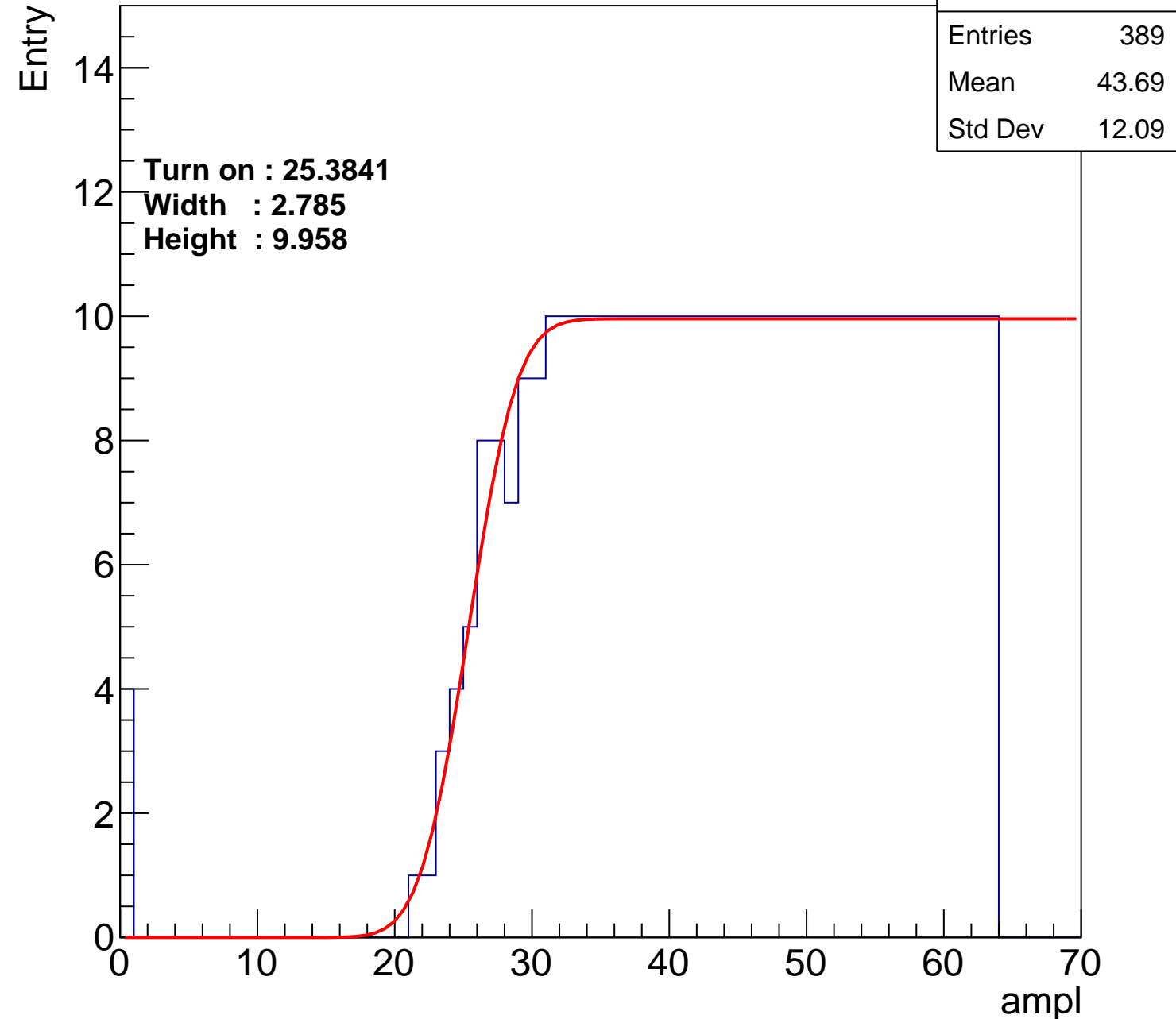
Width : 2.785

Height : 9.958

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch110

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	396
Mean	43.42
Std Dev	12.08

**Turn on : 24.5495**

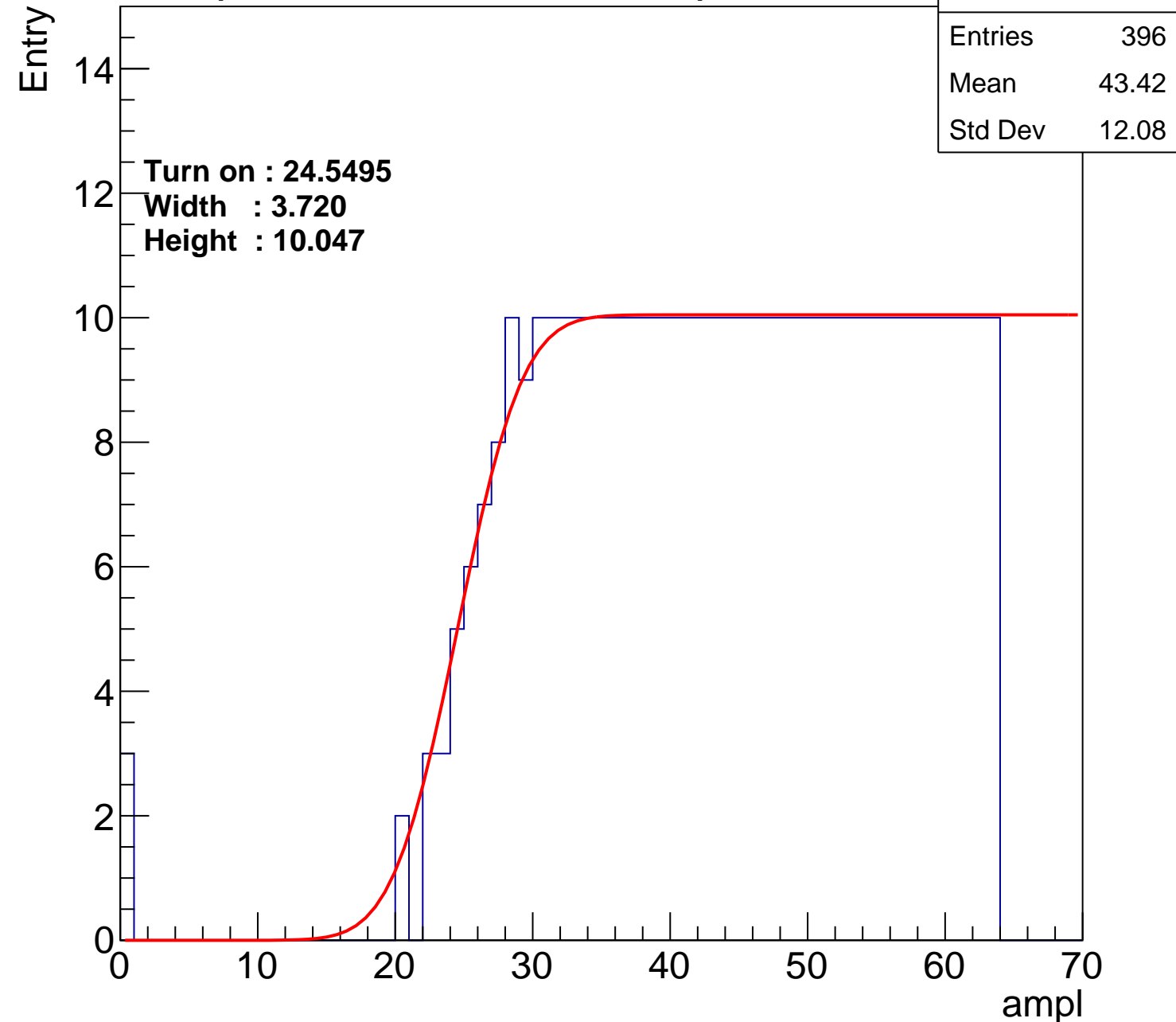
**Width : 3.720**

**Height : 10.047**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L100S, U16-ch111

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	377
Mean	44.42
Std Dev	11.35

Turn on : 27.1328

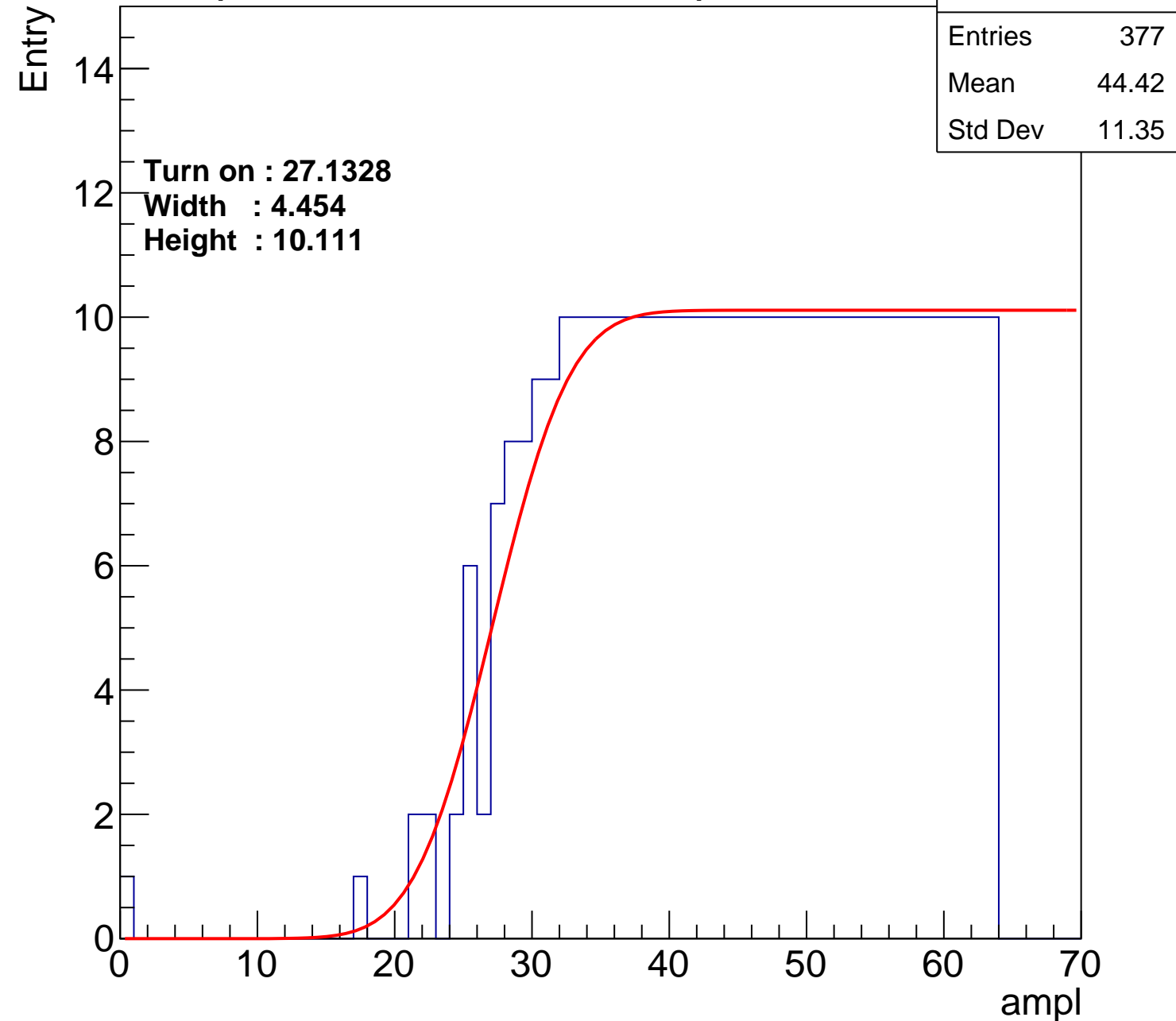
Width : 4.454

Height : 10.111

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch112

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	385
Mean	43.96
Std Dev	11.8

Turn on : 25.3532

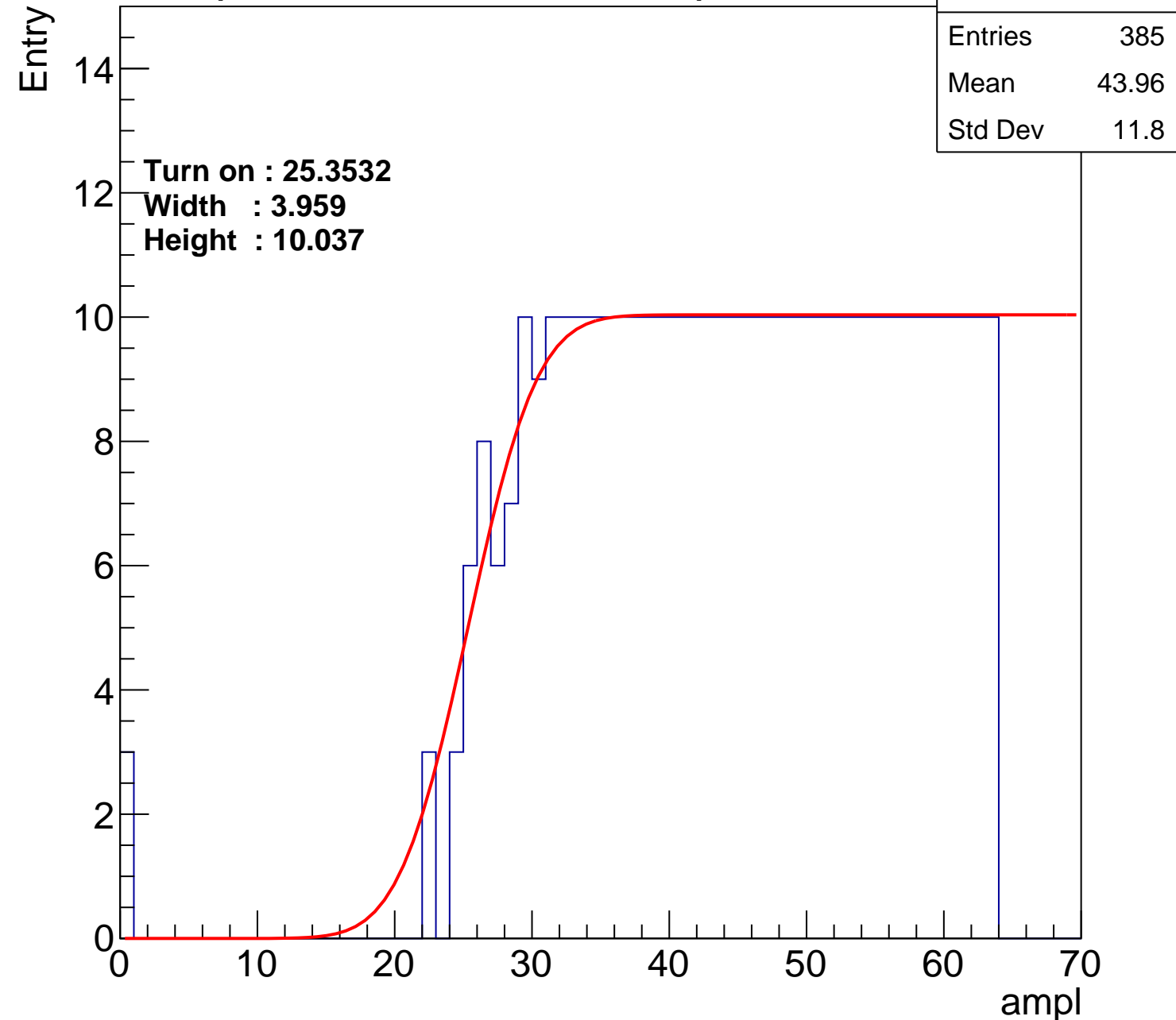
Width : 3.959

Height : 10.037

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch113

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	377
Mean	44.15
Std Dev	12.06

Turn on : 26.7425

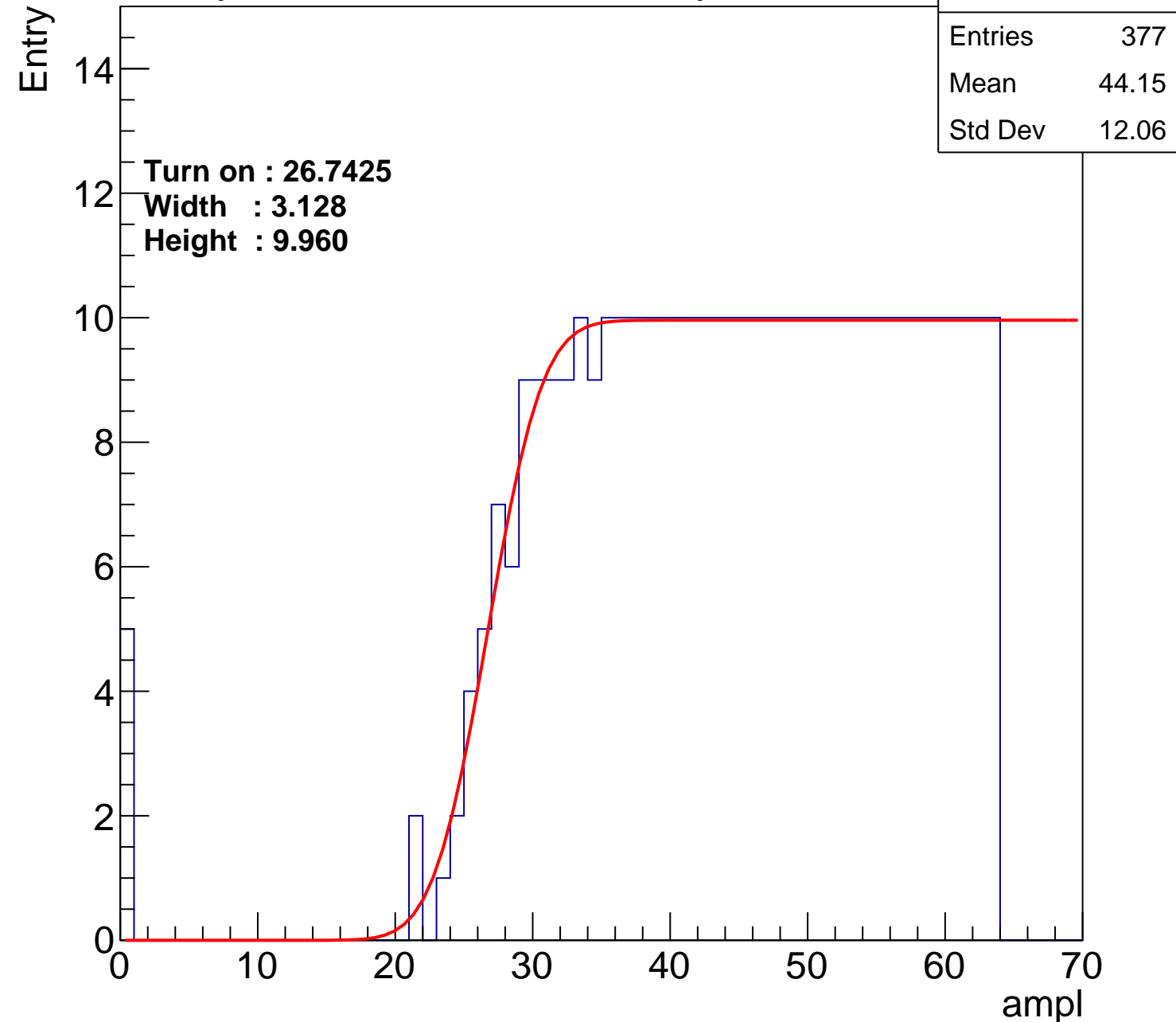
Width : 3.128

Height : 9.960

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch114

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	387
Mean	43.88
Std Dev	11.83

Turn on : 26.2258

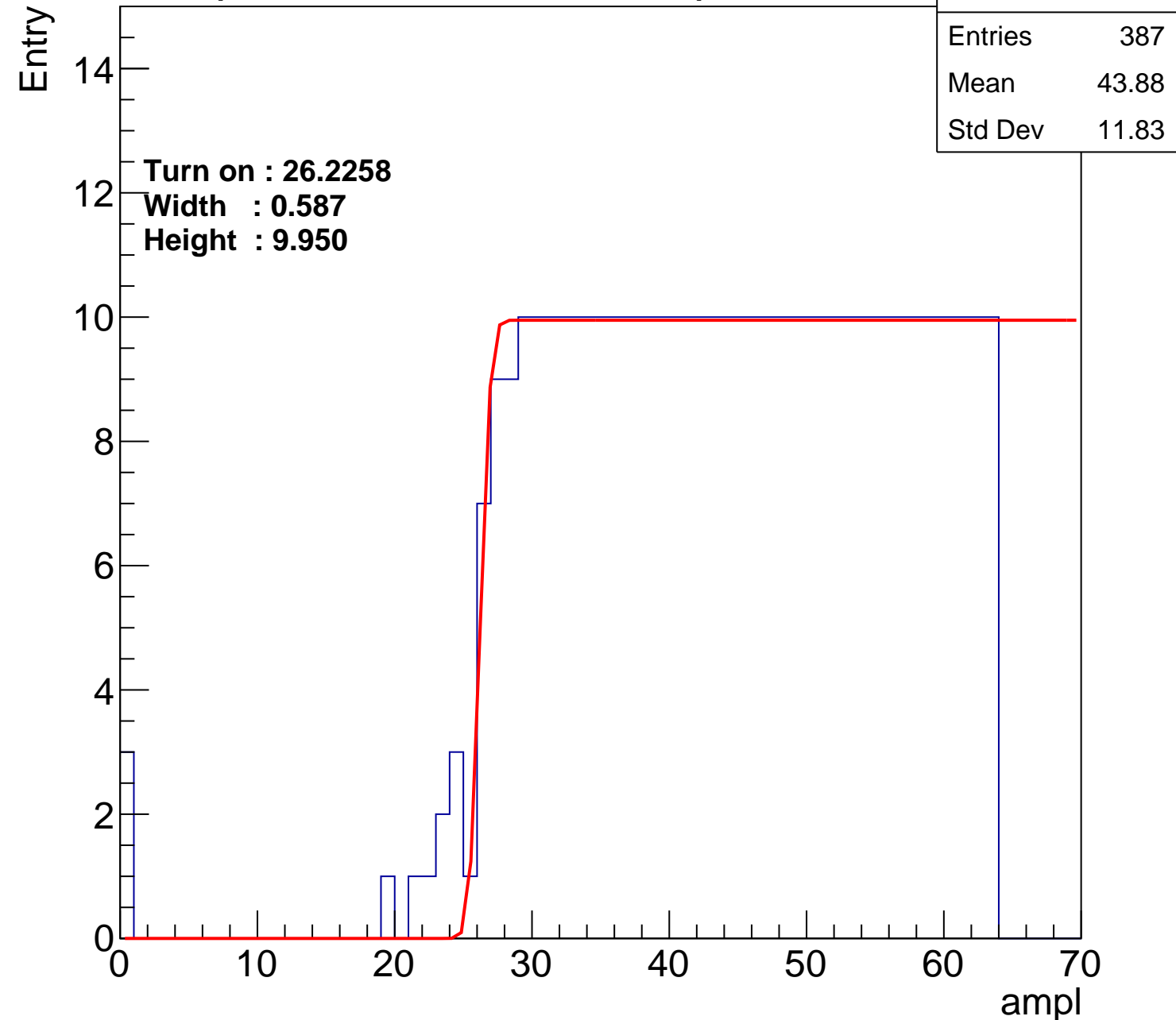
Width : 0.587

Height : 9.950

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch115

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	375
Mean	44.27
Std Dev	11.99

Turn on : 27.4679

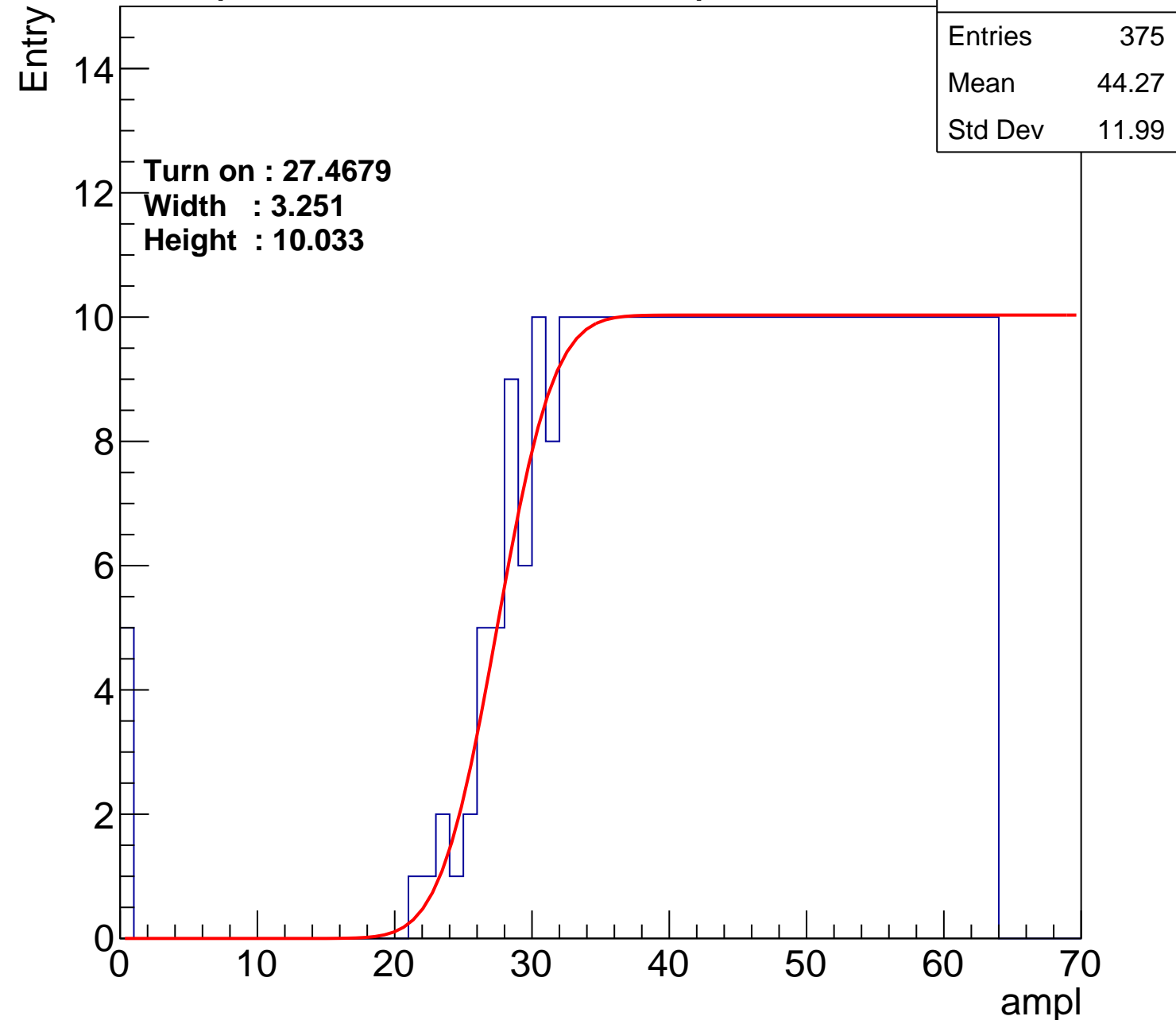
Width : 3.251

Height : 10.033

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch116

calib\_packv5\_042523\_0143.root, FC#4, port A2

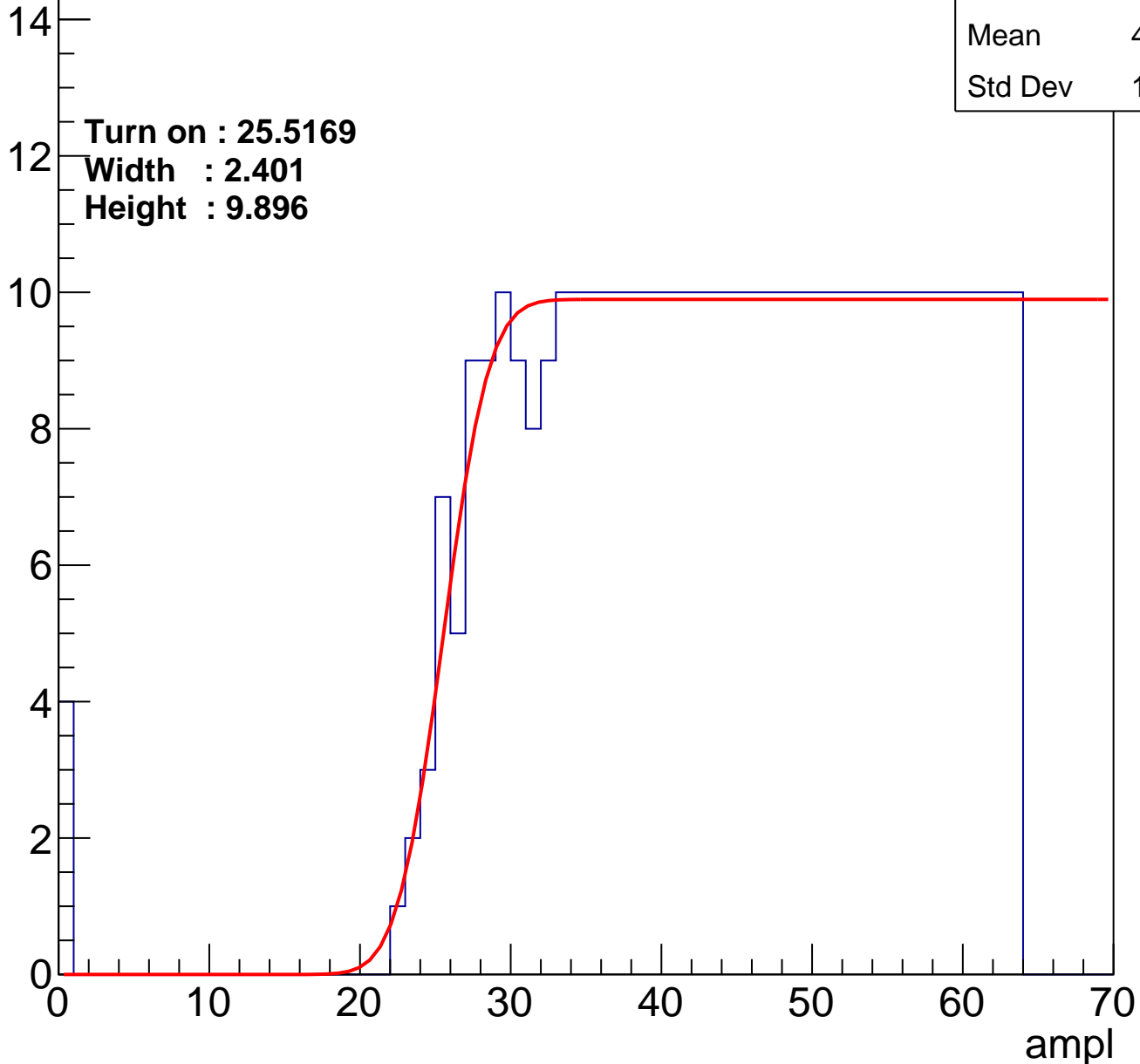
Entries	386
Mean	43.82
Std Dev	12.02

Turn on : 25.5169

Width : 2.401

Height : 9.896

Entry



# B1L100S, U16-ch117

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	367
Mean	44.93
Std Dev	11.14

Turn on : 27.2432

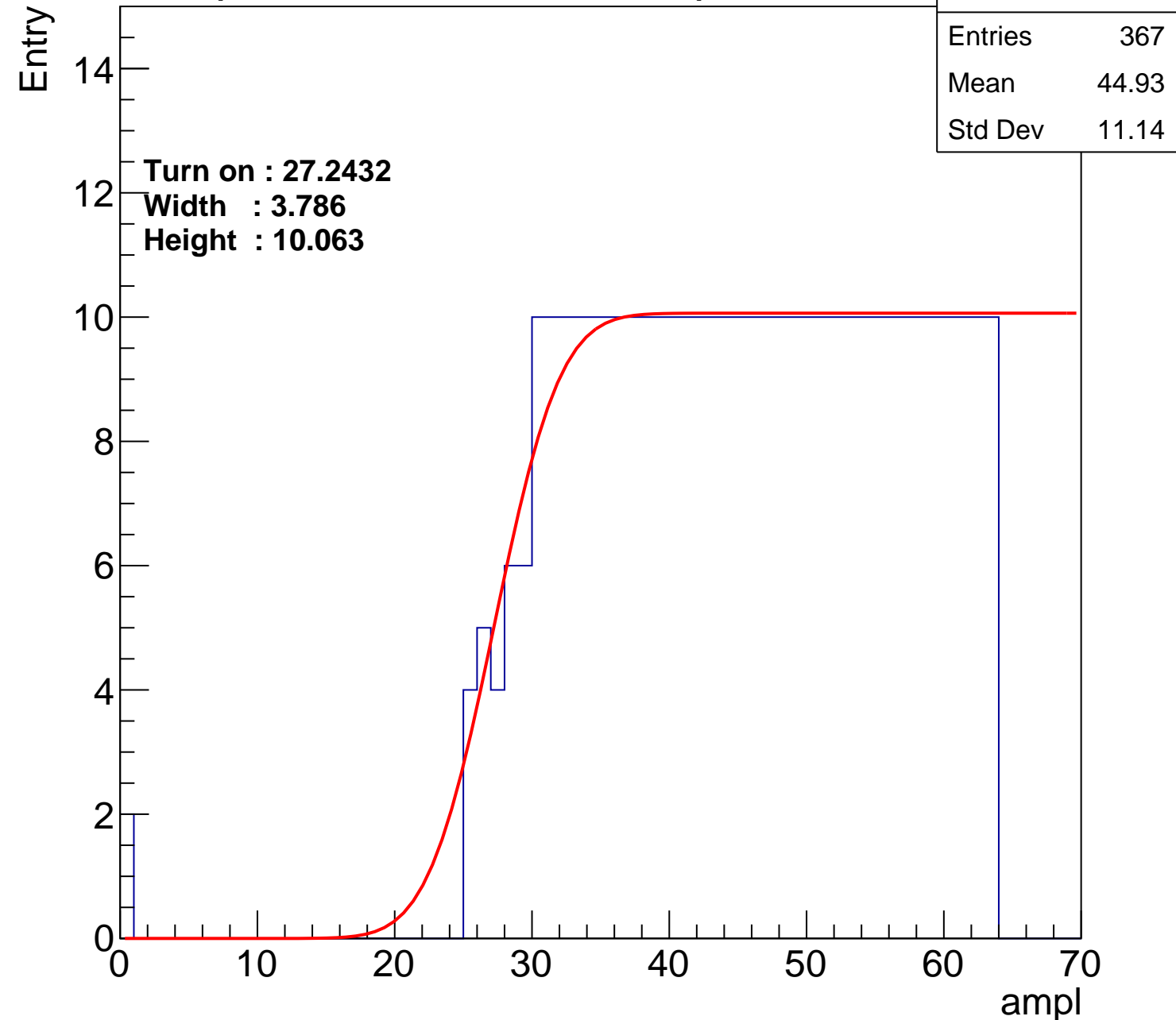
Width : 3.786

Height : 10.063

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch118

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	403
Mean	43.06
Std Dev	12.33

**Turn on : 23.9008**

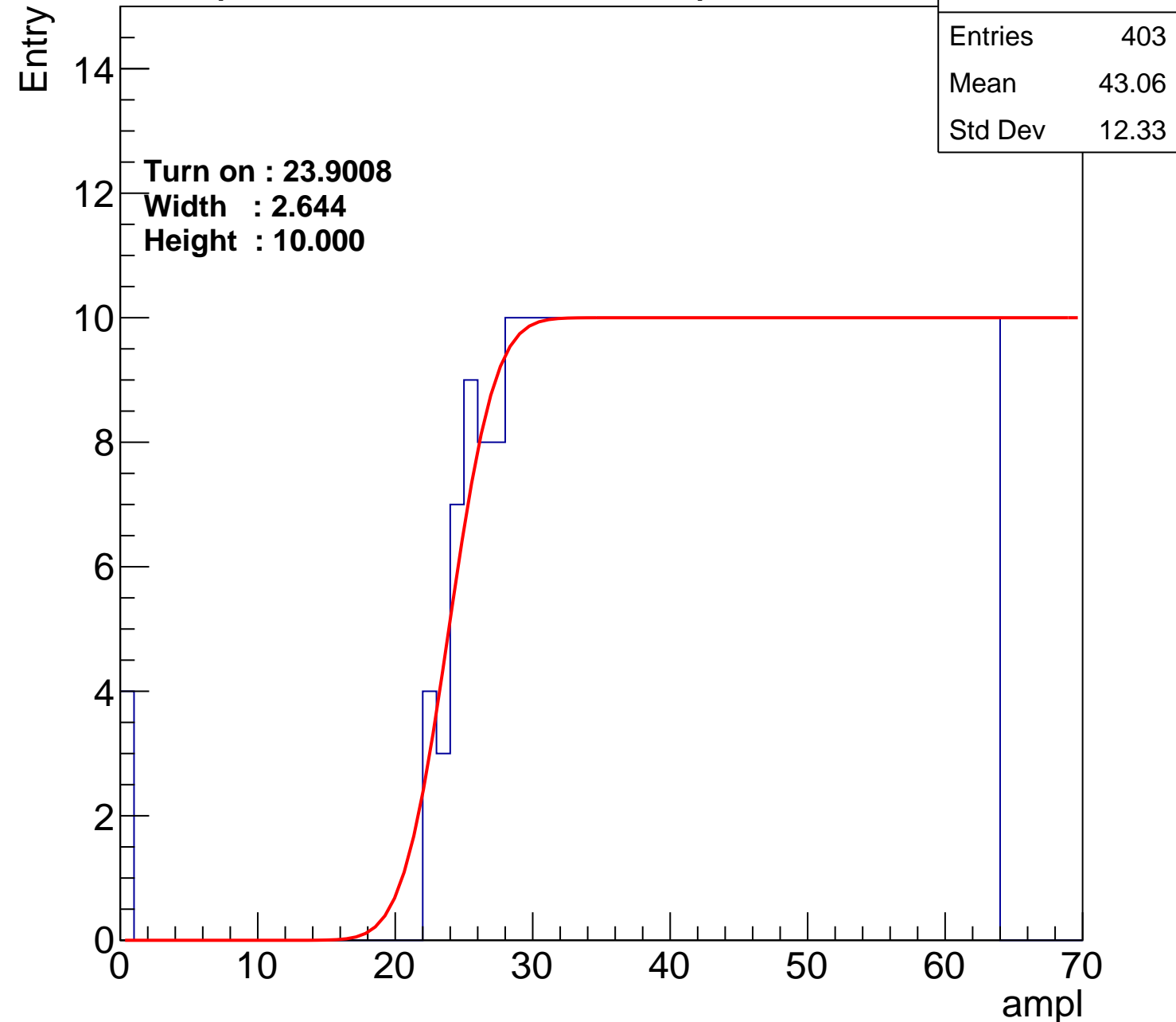
**Width : 2.644**

**Height : 10.000**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L100S, U16-ch119

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	369
Mean	44.7
Std Dev	11.48

**Turn on : 27.5763**

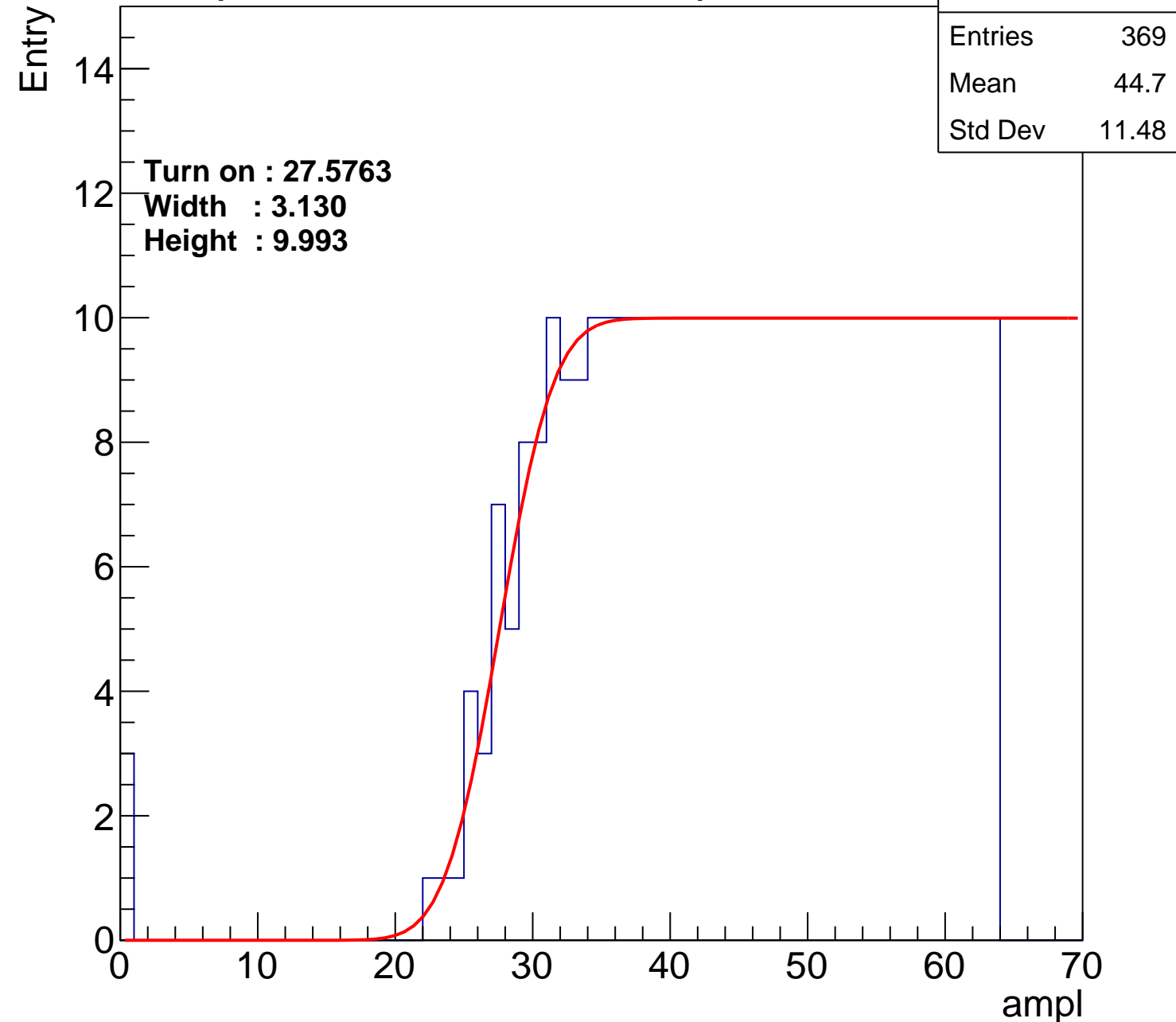
**Width : 3.130**

**Height : 9.993**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch120

calib\_packv5\_042523\_0143.root, FC#4, port A2

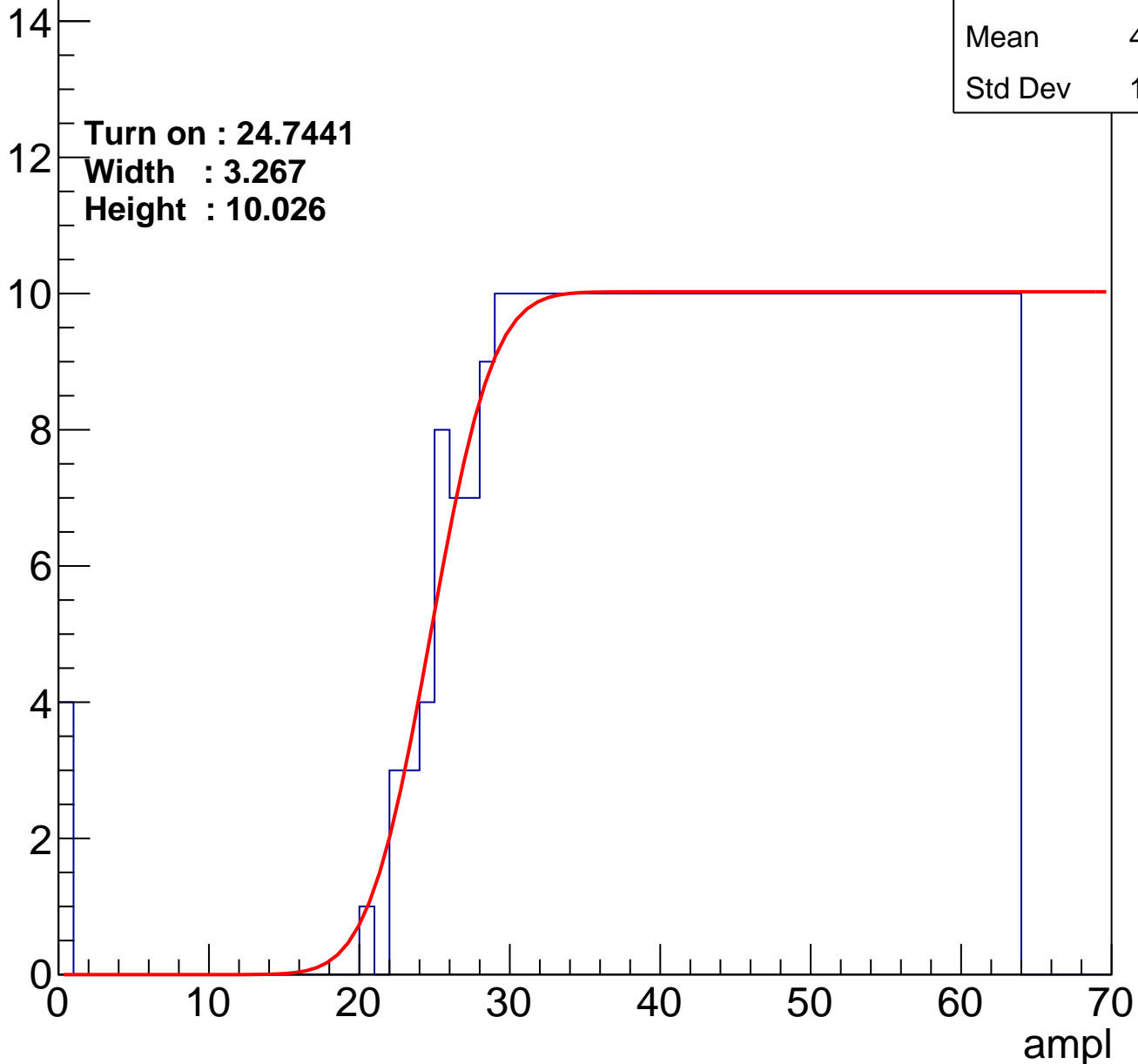
Entries	396
Mean	43.37
Std Dev	12.22

Turn on : 24.7441

Width : 3.267

Height : 10.026

Entry



# B1L100S, U16-ch121

calib\_packv5\_042523\_0143.root, FC#4, port A2

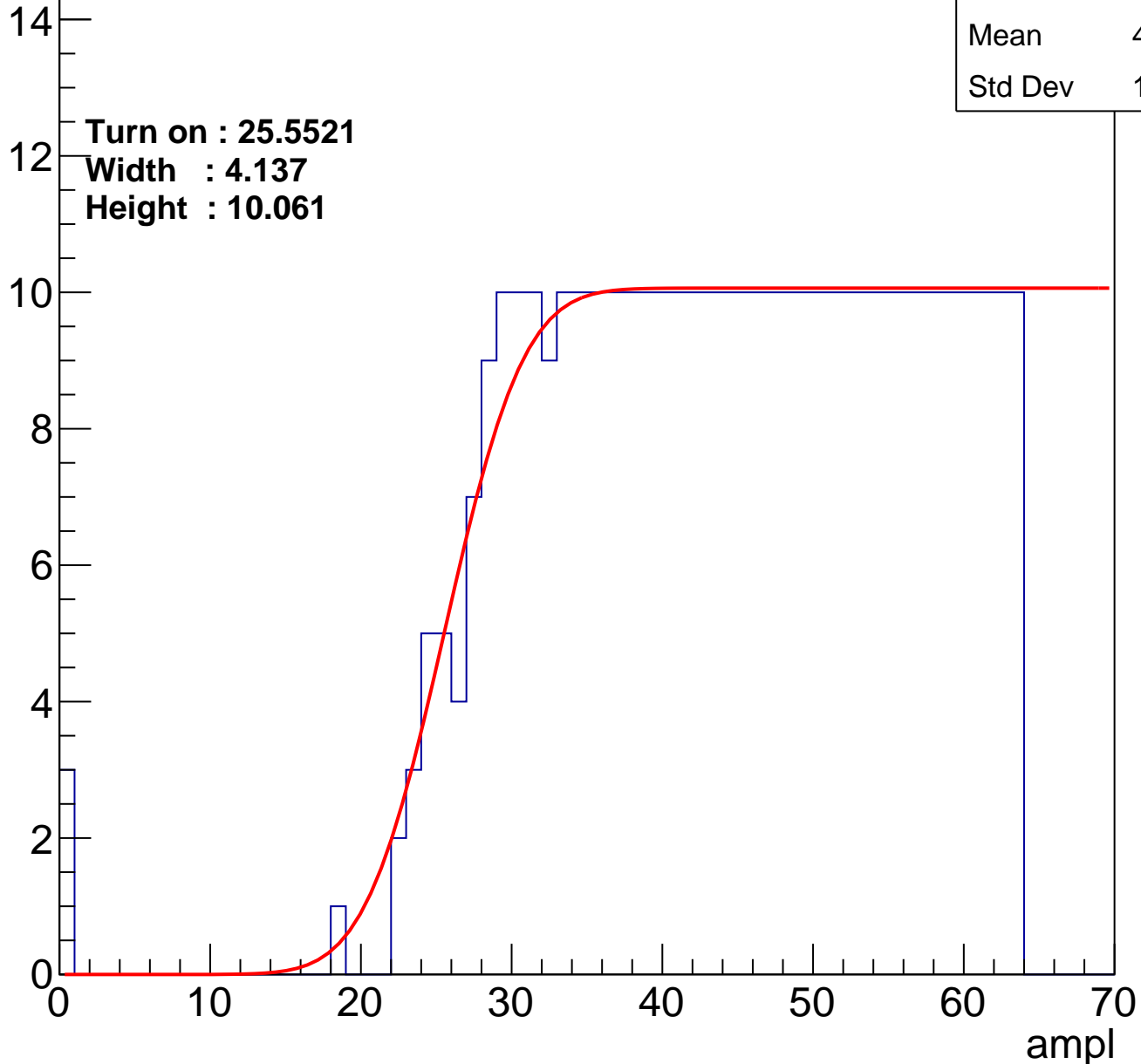
Entries	388
Mean	43.79
Std Dev	11.92

Turn on : 25.5521

Width : 4.137

Height : 10.061

Entry



# B1L100S, U16-ch122

calib\_packv5\_042523\_0143.root, FC#4, port A2

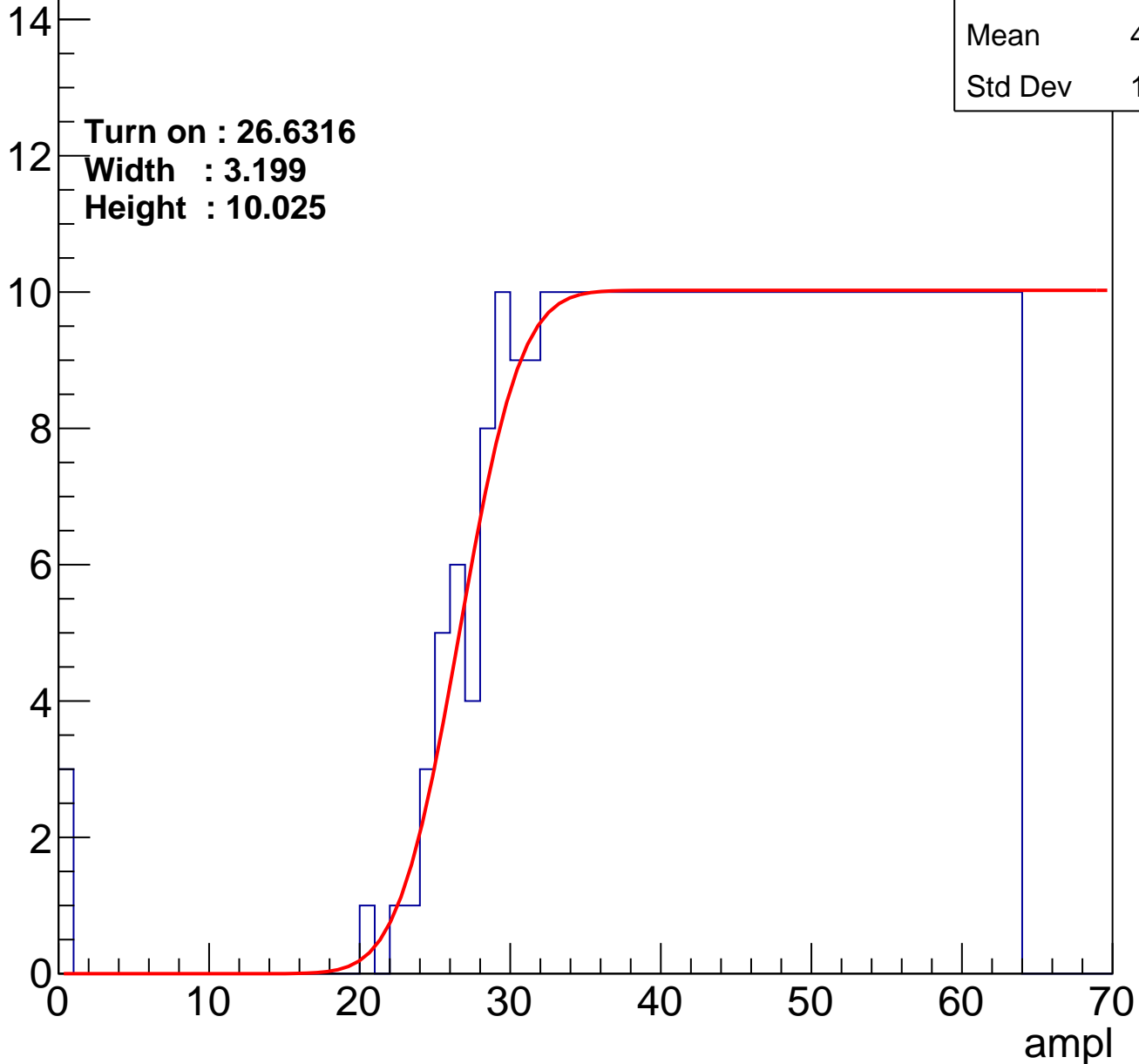
Entries	380
Mean	44.18
Std Dev	11.72

Turn on : 26.6316

Width : 3.199

Height : 10.025

Entry



# B1L100S, U16-ch123

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	370
Mean	44.7
Std Dev	11.34

**Turn on : 27.6569**

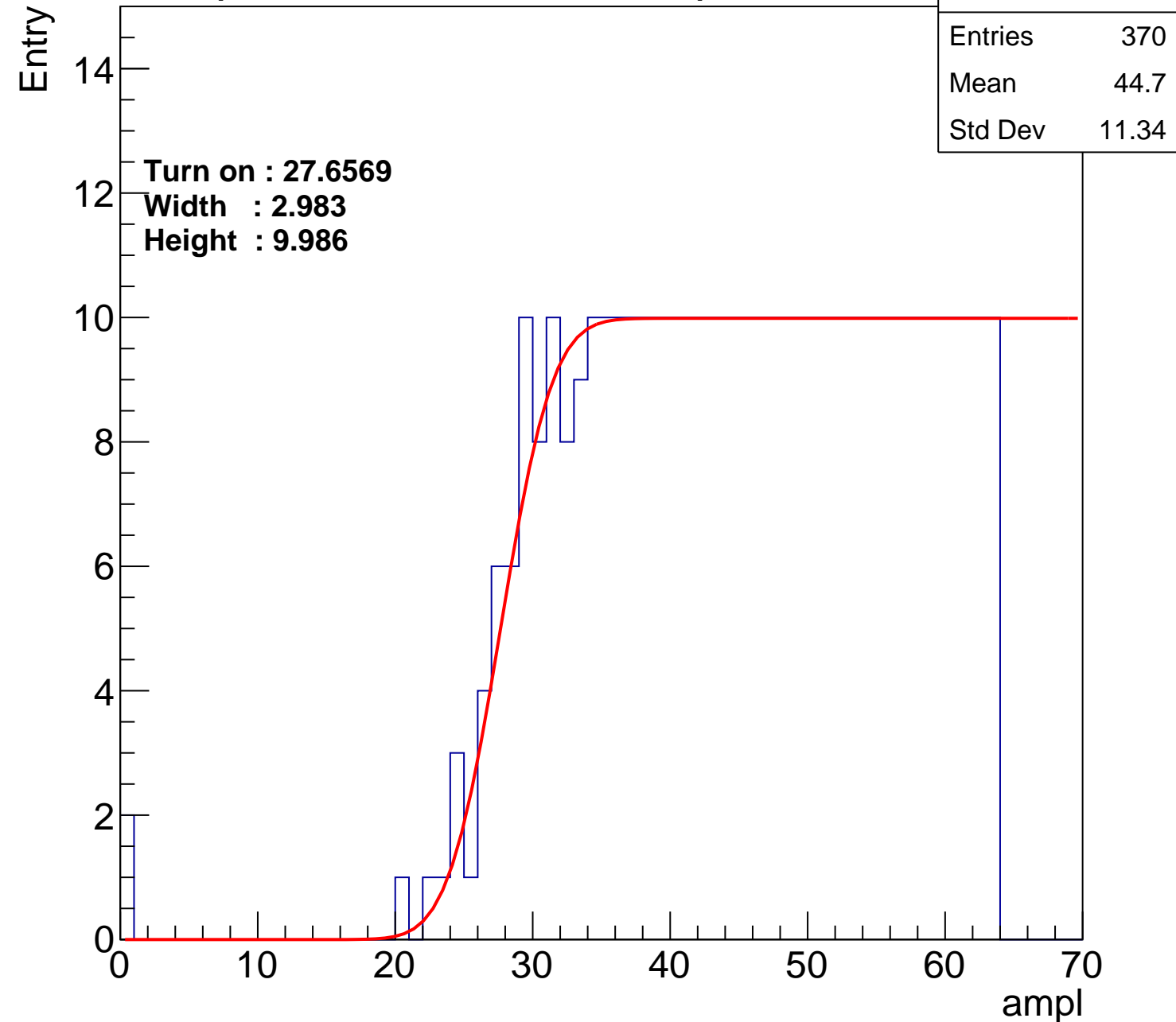
**Width : 2.983**

**Height : 9.986**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch124

calib\_packv5\_042523\_0143.root, FC#4, port A2

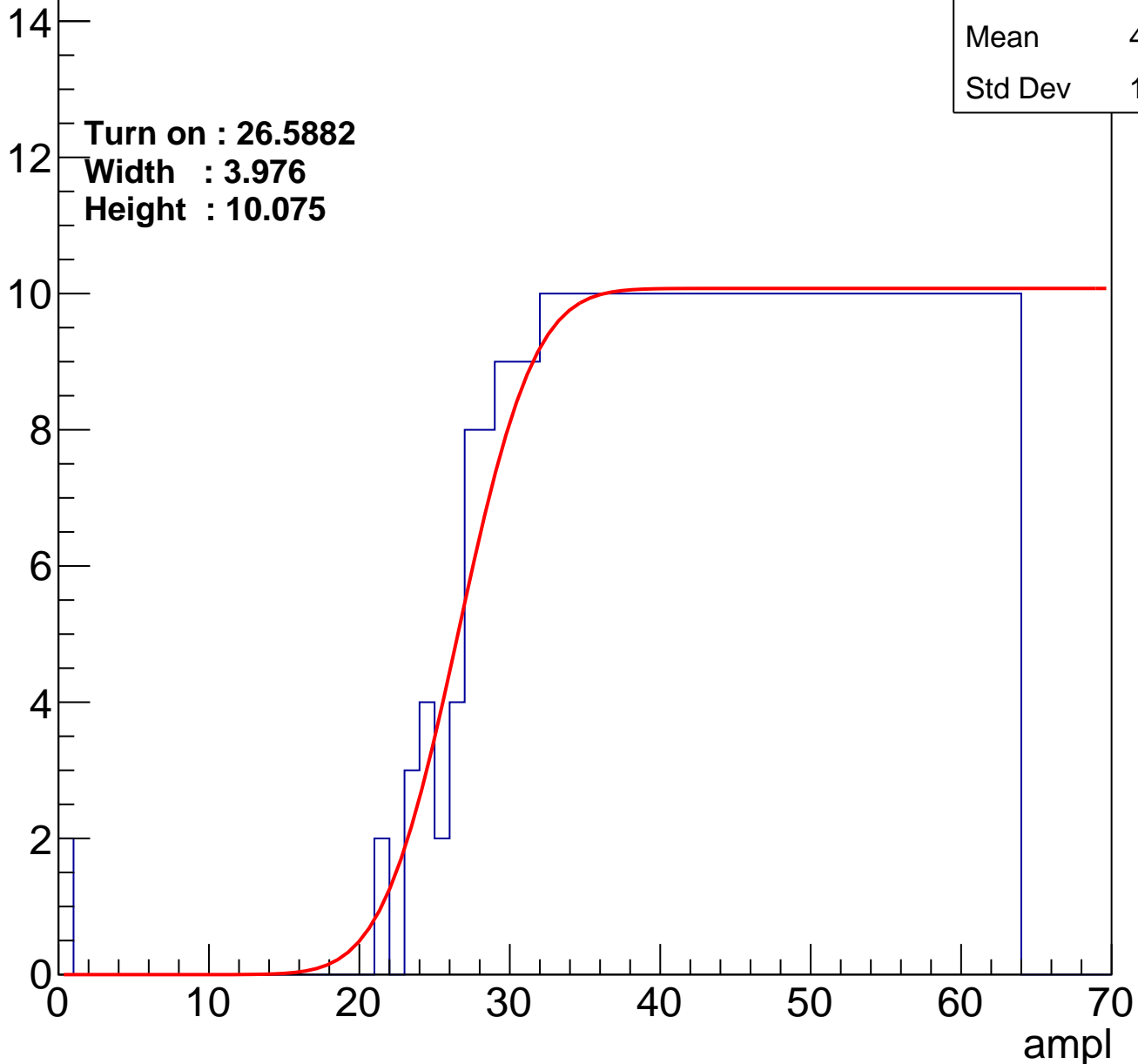
Entries	380
Mean	44.24
Std Dev	11.55

Turn on : 26.5882

Width : 3.976

Height : 10.075

Entry



# B1L100S, U16-ch125

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	382
Mean	44.1
Std Dev	11.67

Turn on : 26.5295

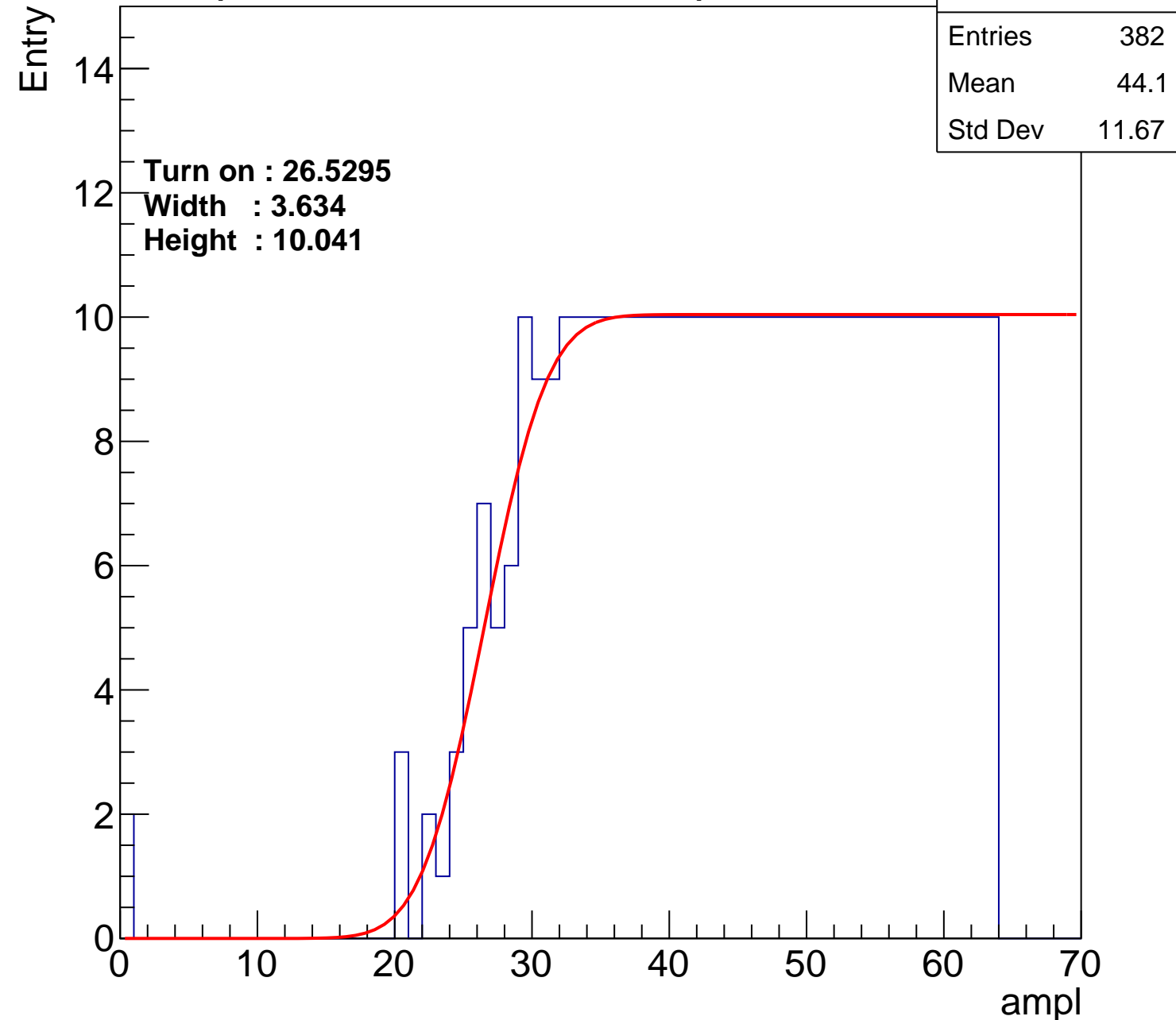
Width : 3.634

Height : 10.041

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U16-ch126

calib\_packv5\_042523\_0143.root, FC#4, port A2

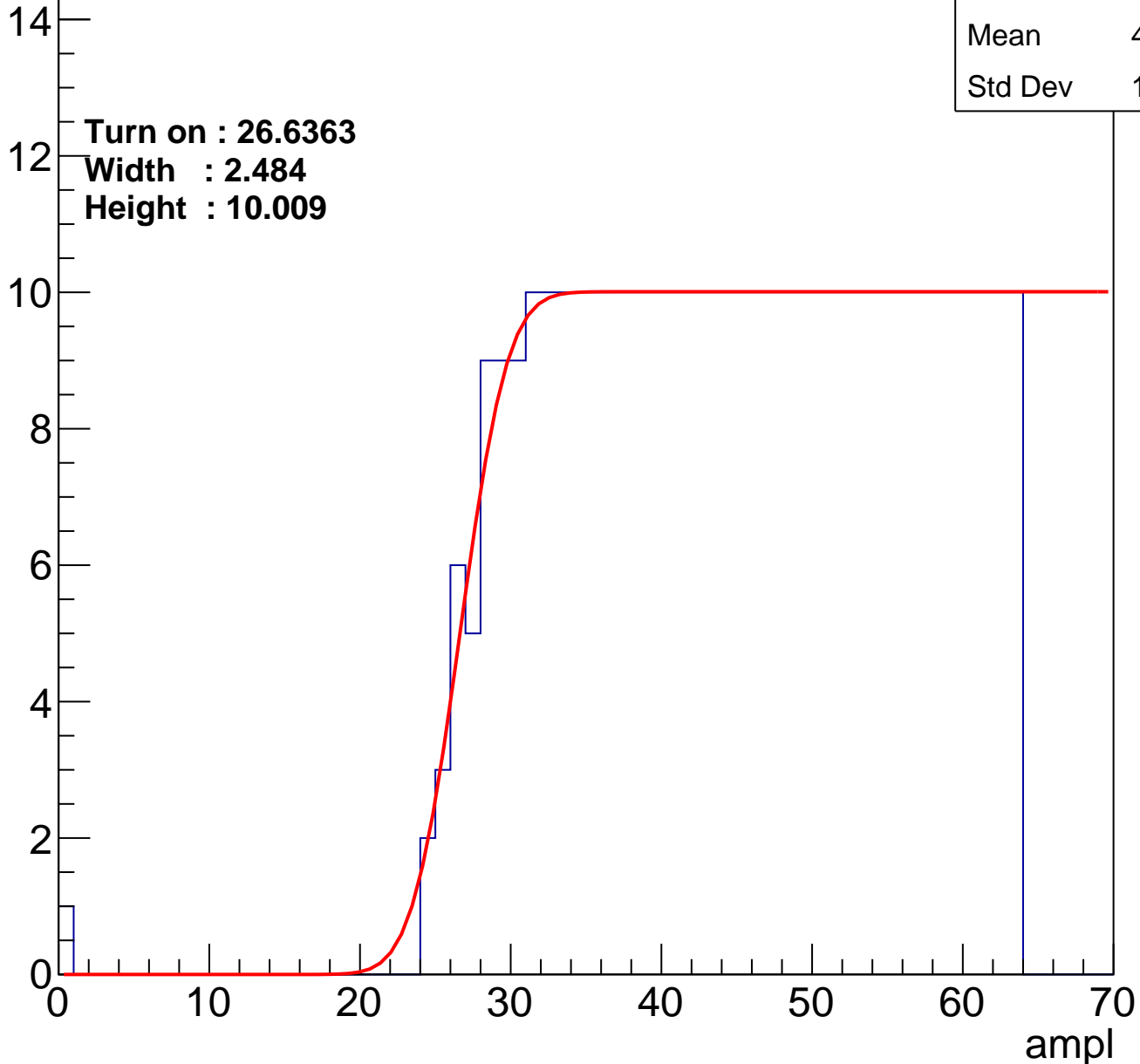
Entries	374
Mean	44.67
Std Dev	11.09

Turn on : 26.6363

Width : 2.484

Height : 10.009

Entry





# B1L100S, U16-ch127

calib\_packv5\_042523\_0143.root, FC#4, port A2

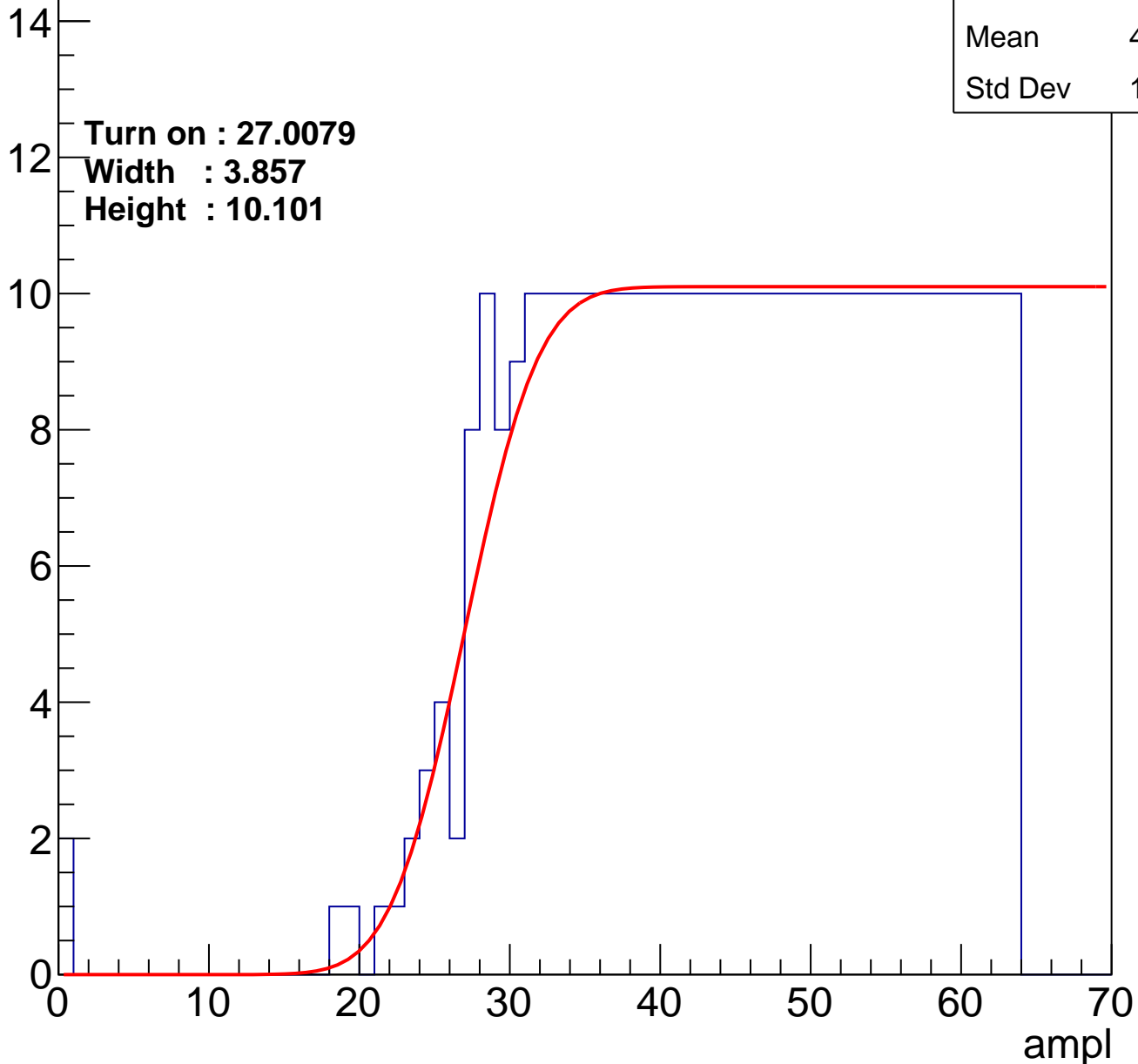
Entries	382
Mean	44.13
Std Dev	11.63

Turn on : 27.0079

Width : 3.857

Height : 10.101

Entry



# B1L100S, U16-ch127

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	382
Mean	44.13
Std Dev	11.63

Turn on : 27.0079

Width : 3.857

Height : 10.101

Entry

