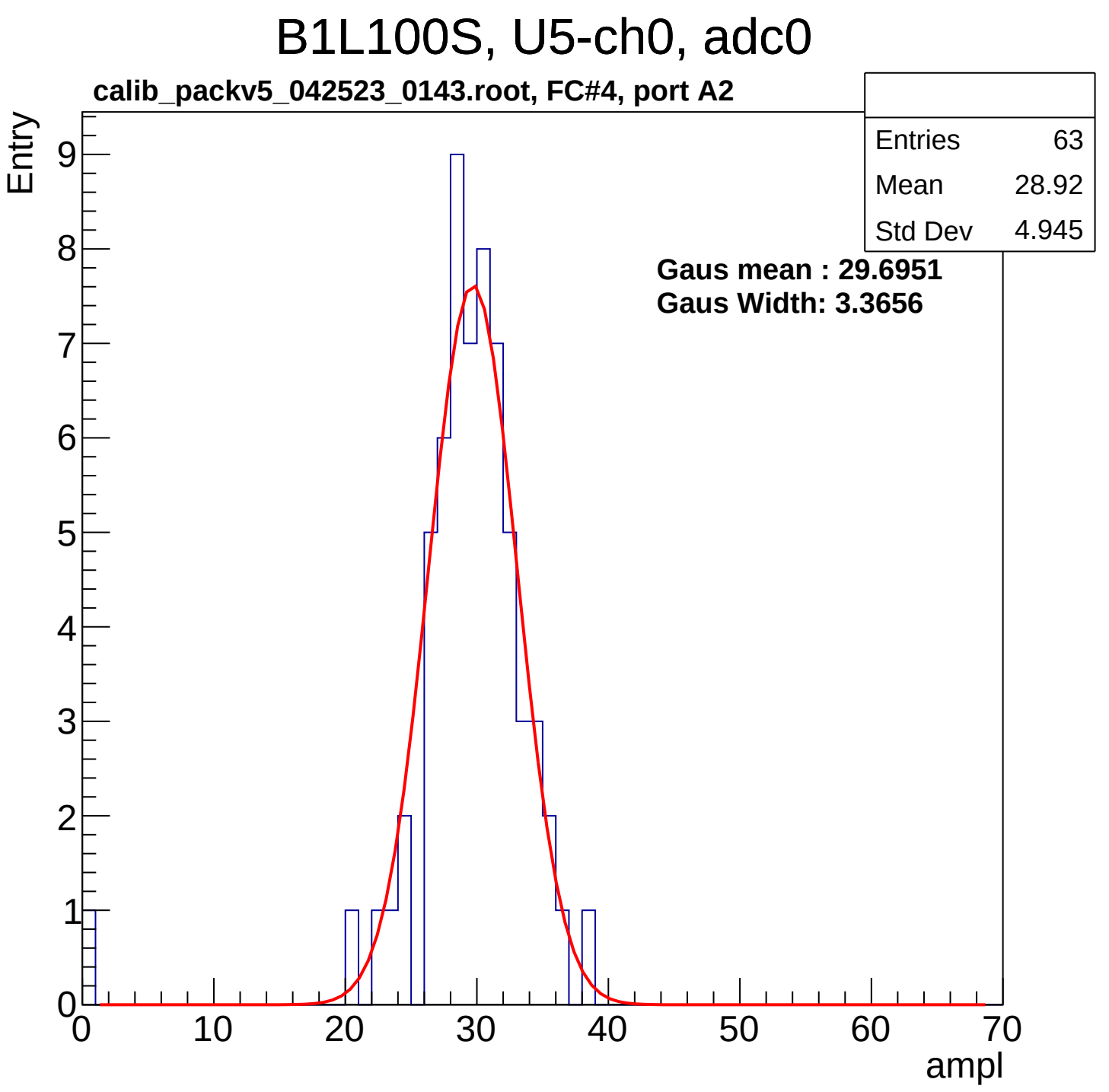
B1L100S, U5-ch0, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 28.92
Std Dev 4.945
Gaus mean : 29.6951
Gaus Width: 3.3656
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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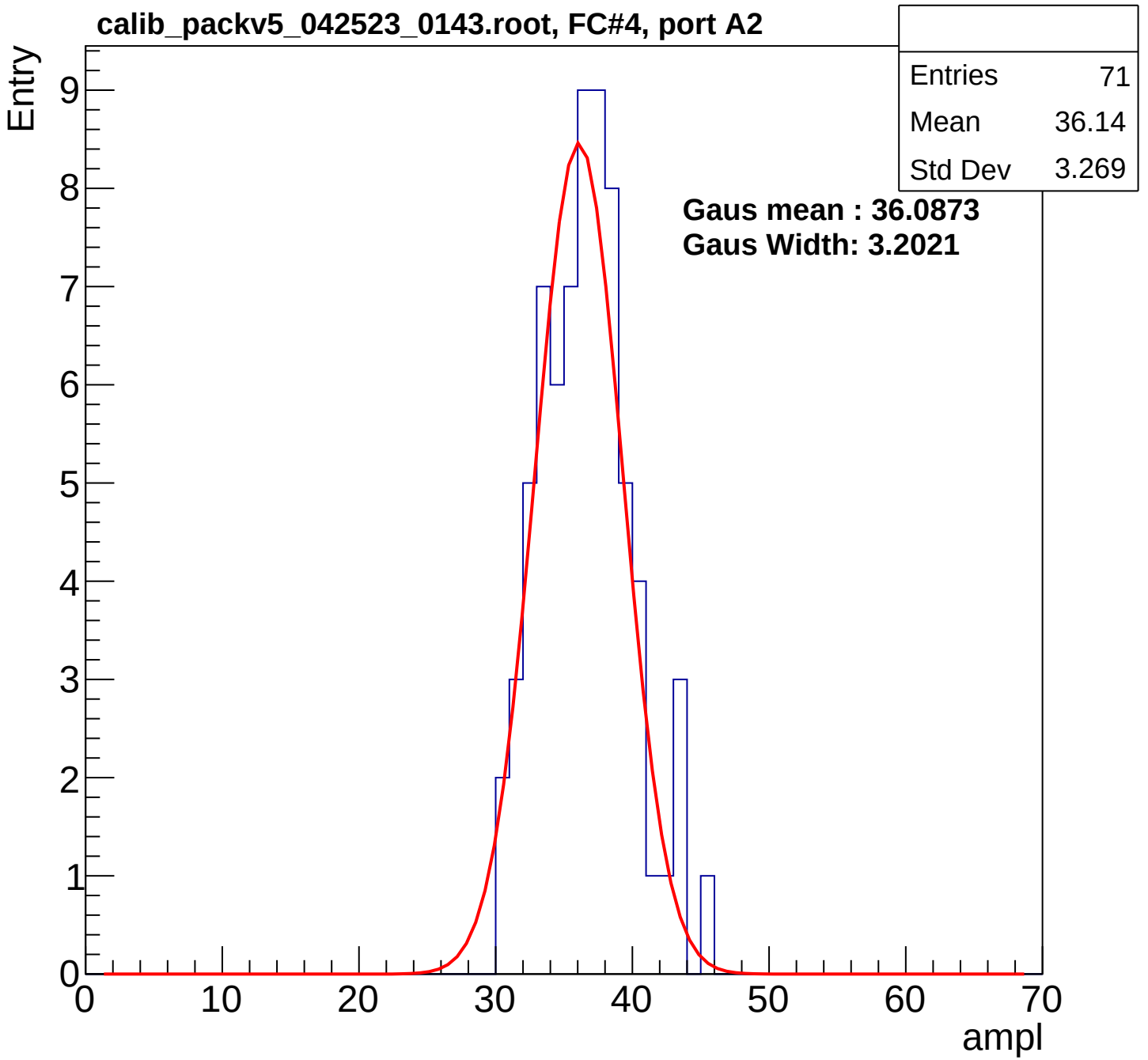
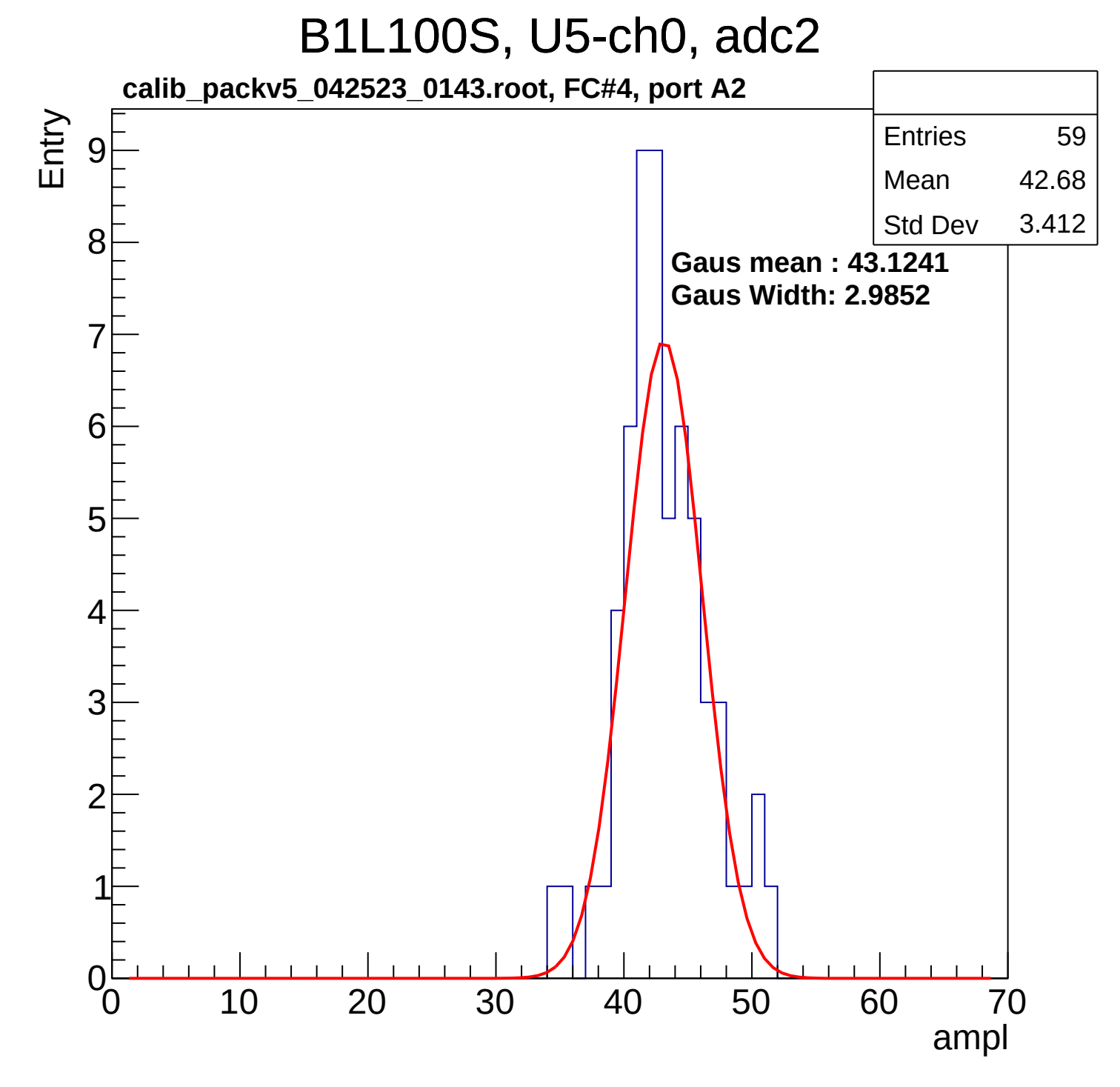
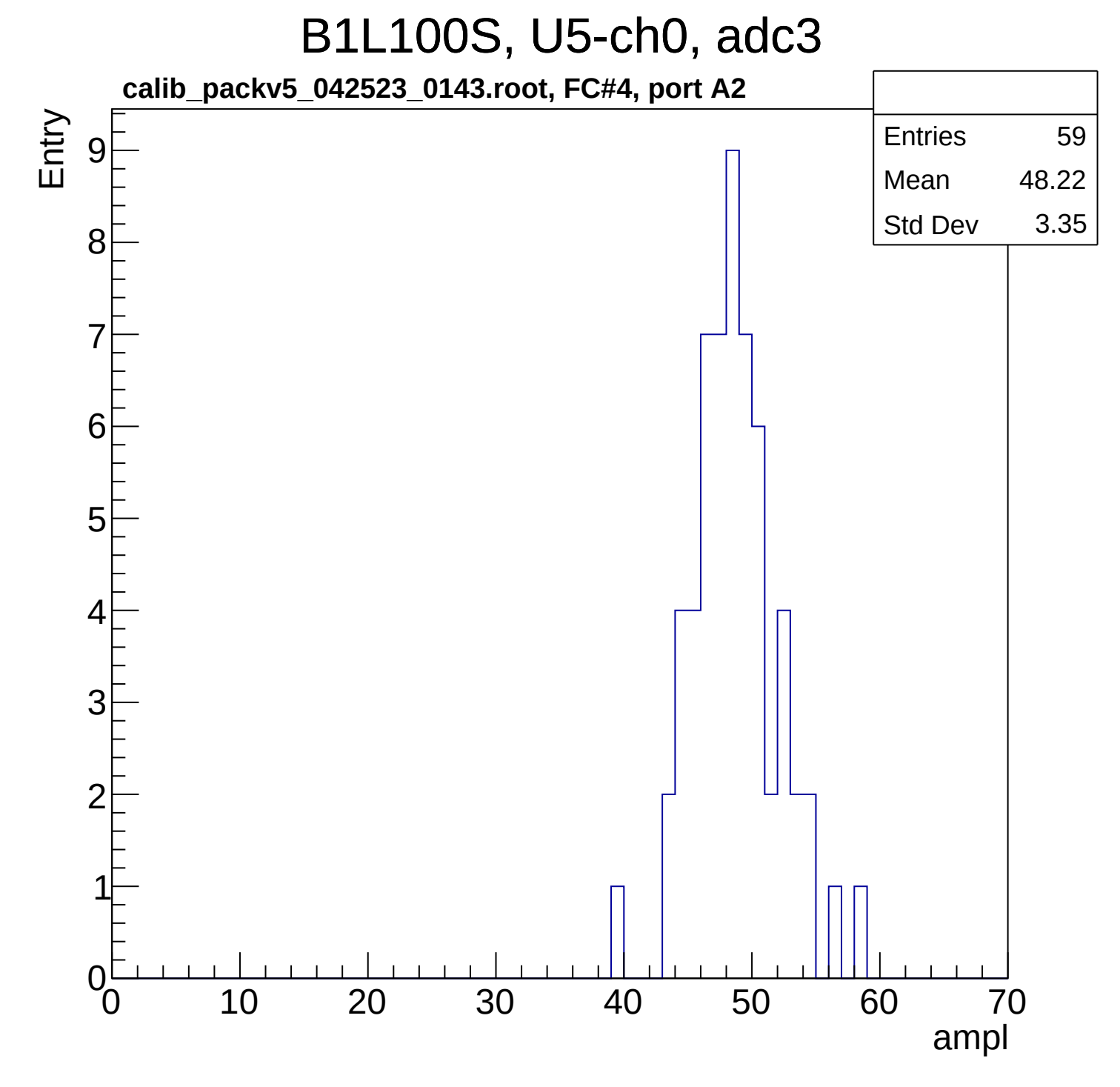
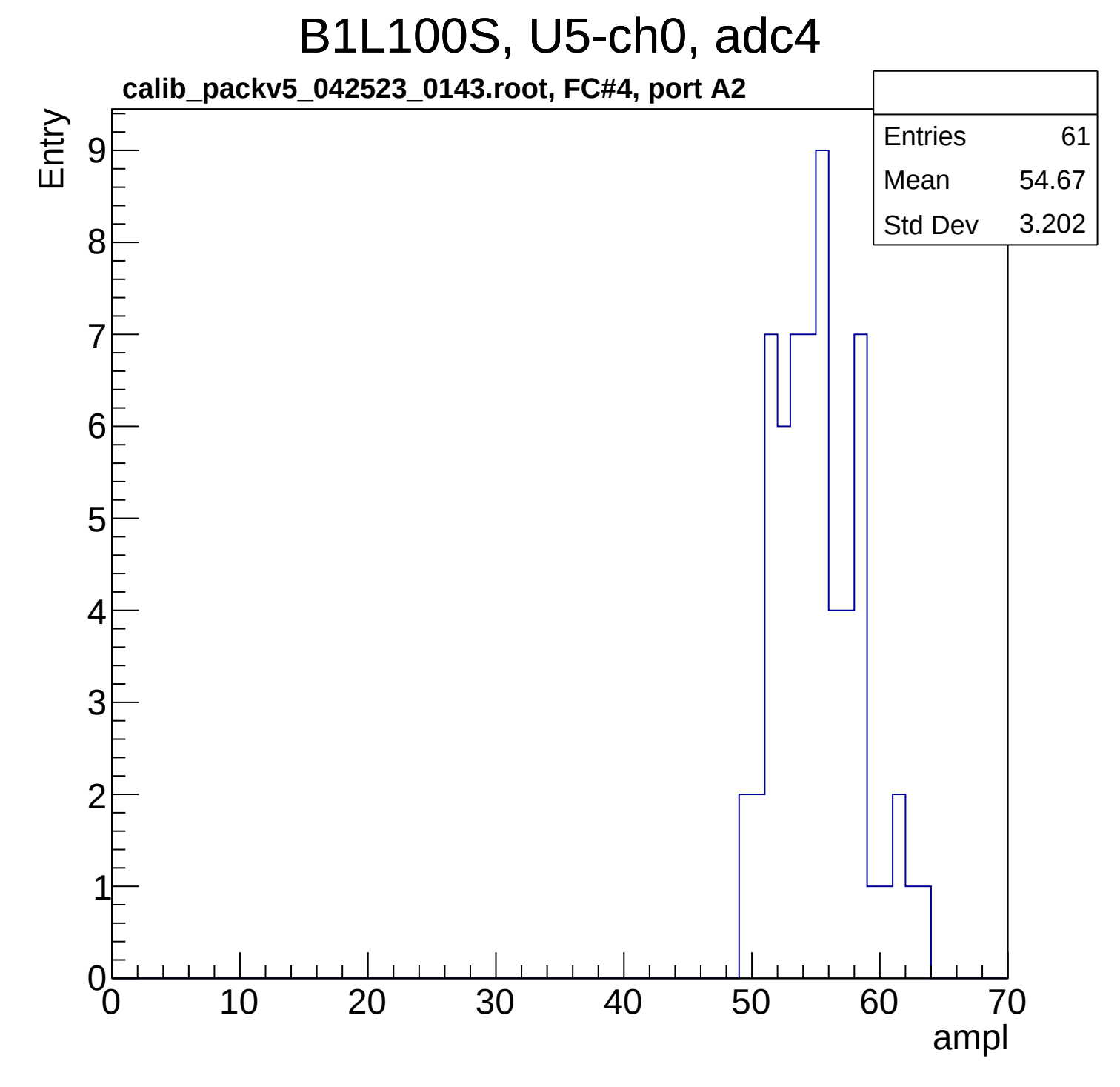
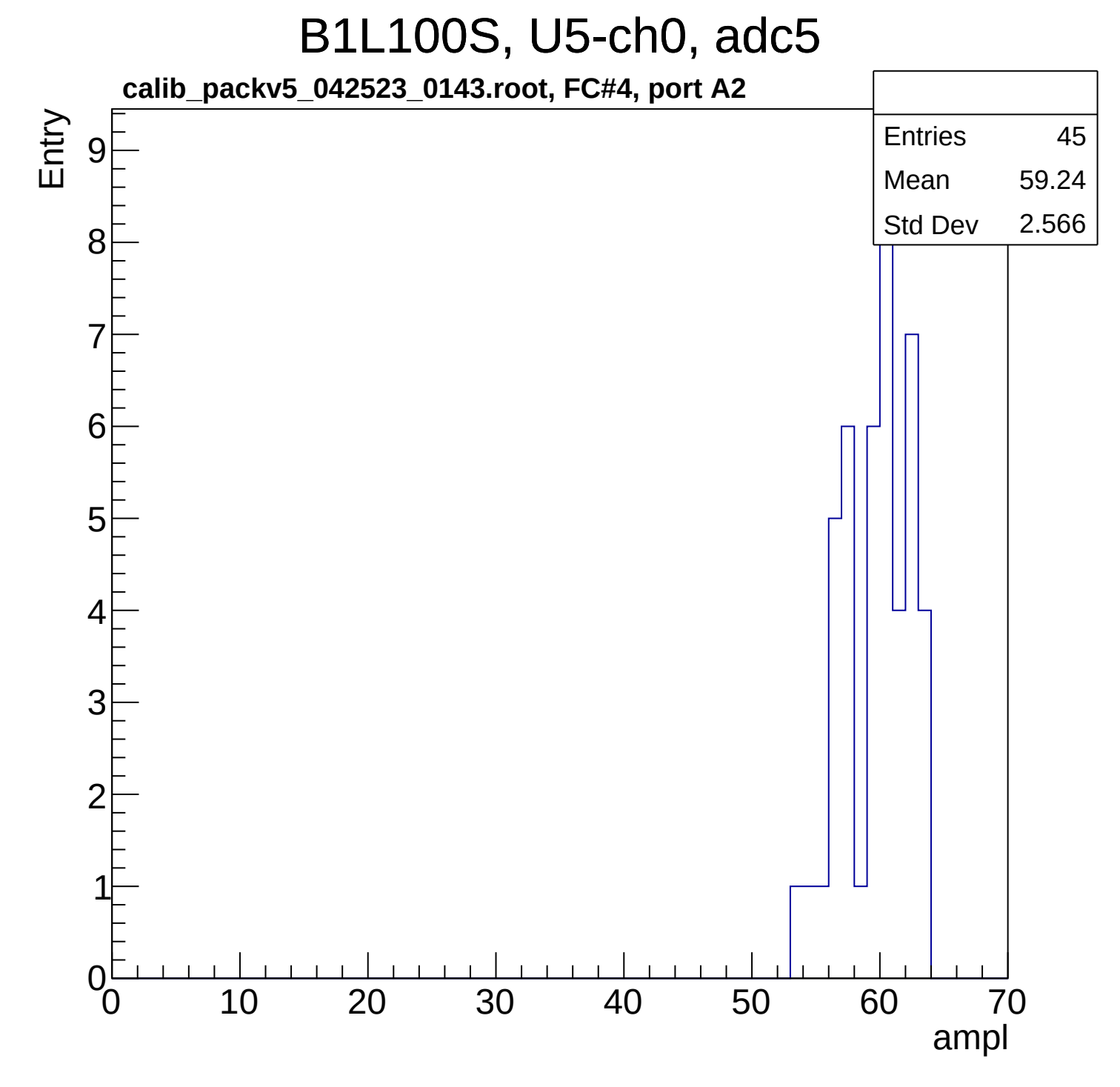
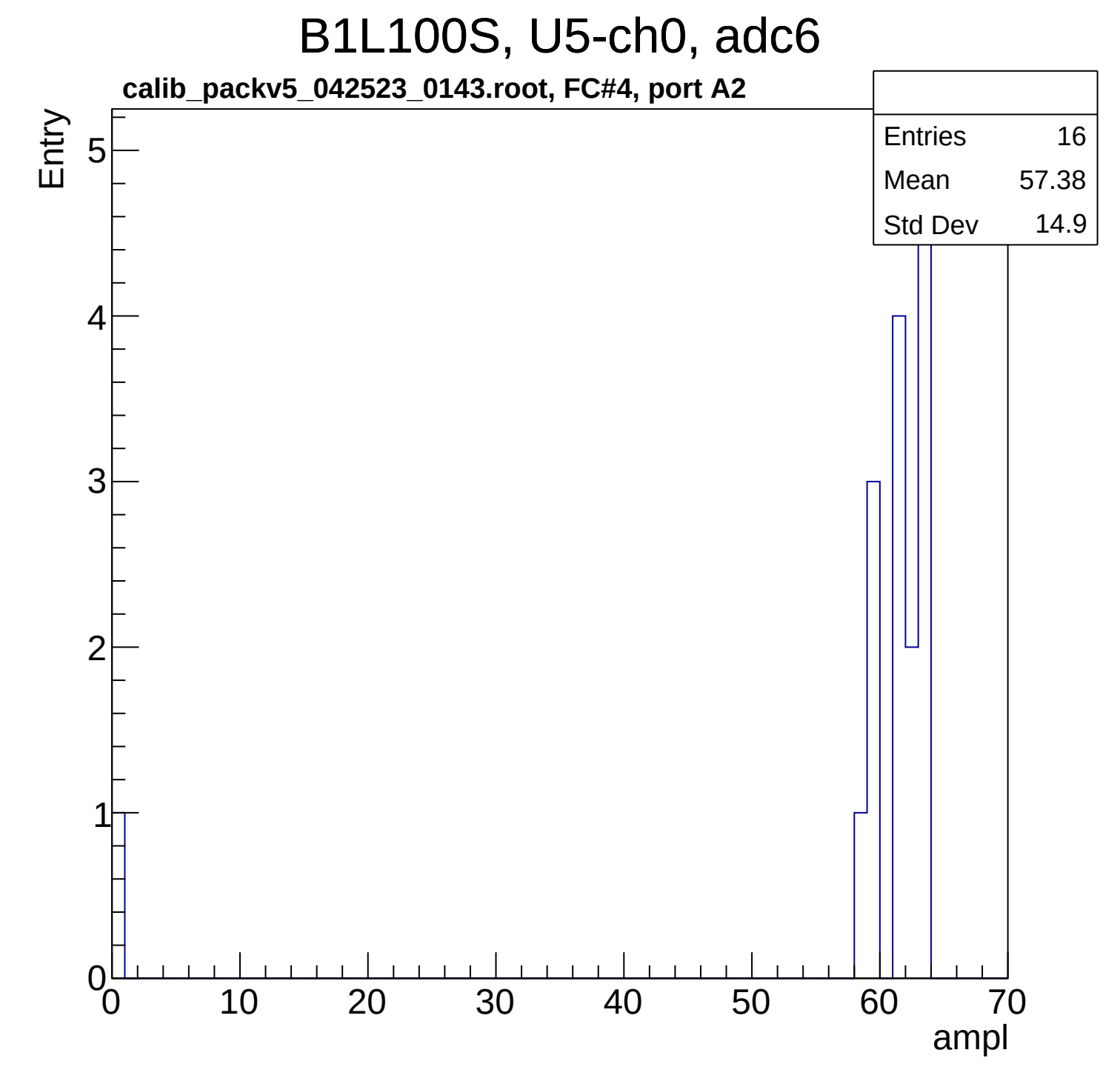

B1L100S, U5-ch0, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 36.14
Std Dev 3.269
Gaus mean : 36.0873
Gaus Width: 3.2021
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

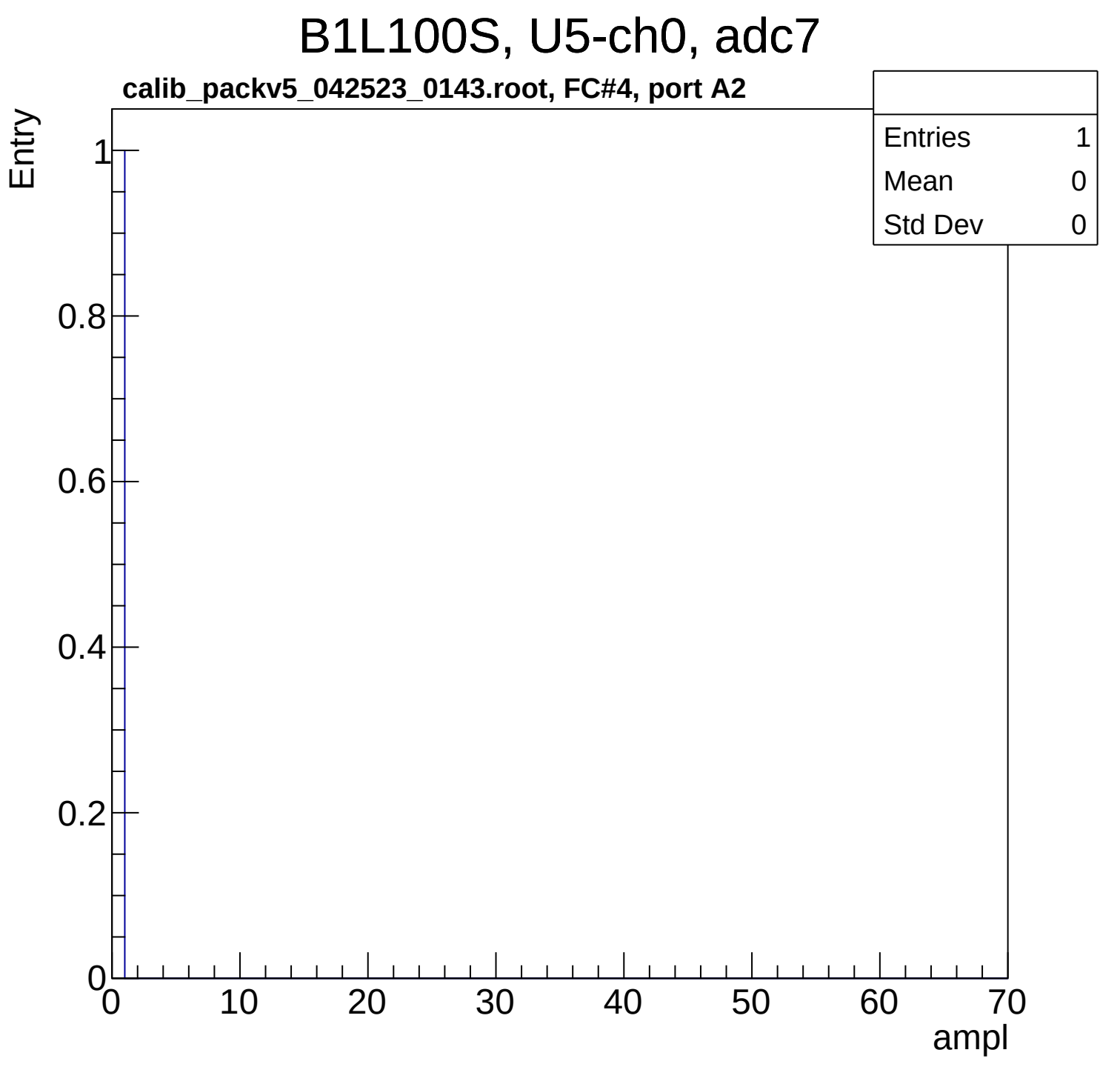

B1L100S, U5-ch0, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 42.68
Std Dev 3.412
Gaus mean : 43.1241
Gaus Width: 2.9852
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

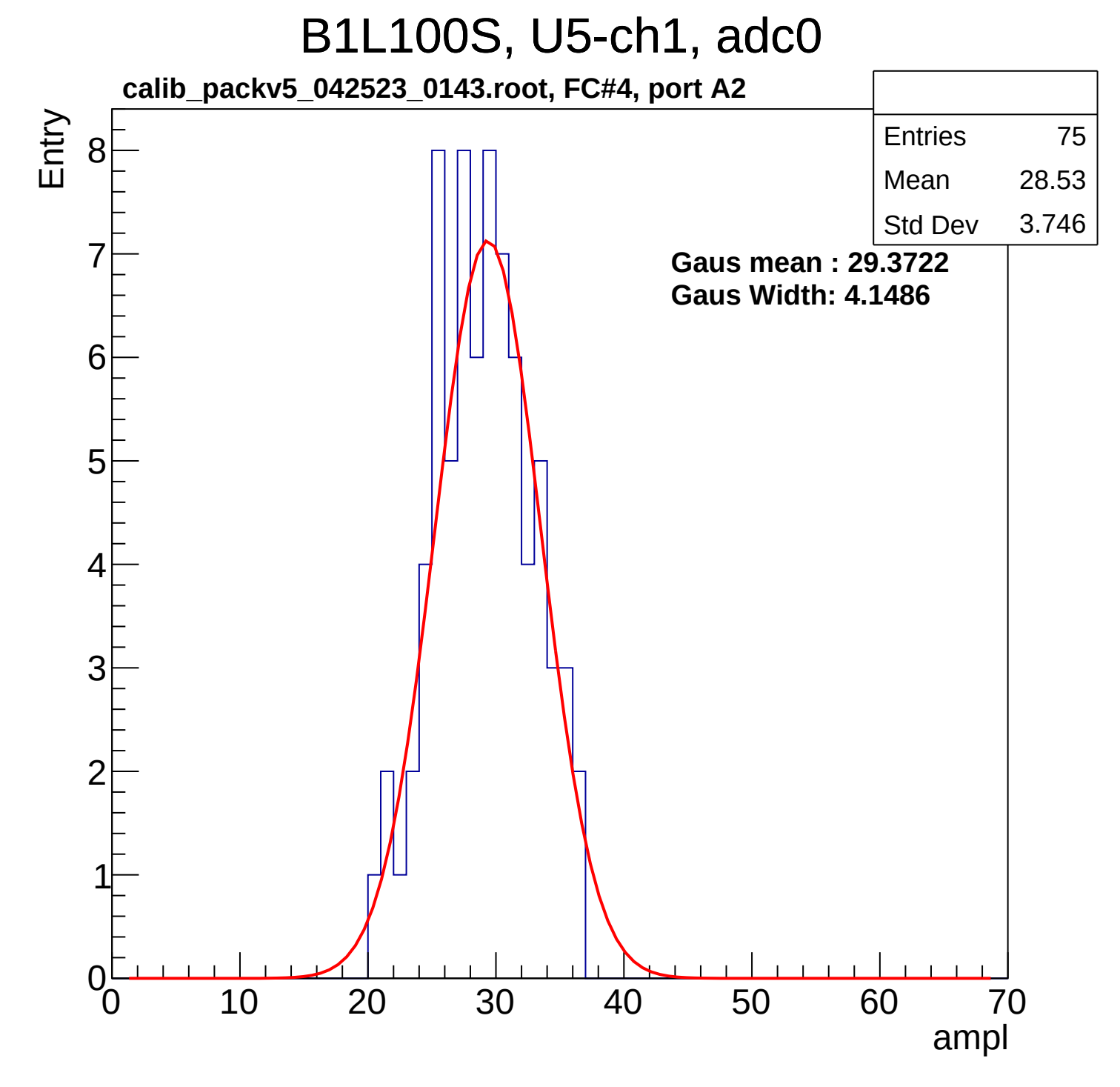

B1L100S, U5-ch0, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 48.22
Std Dev 3.35
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

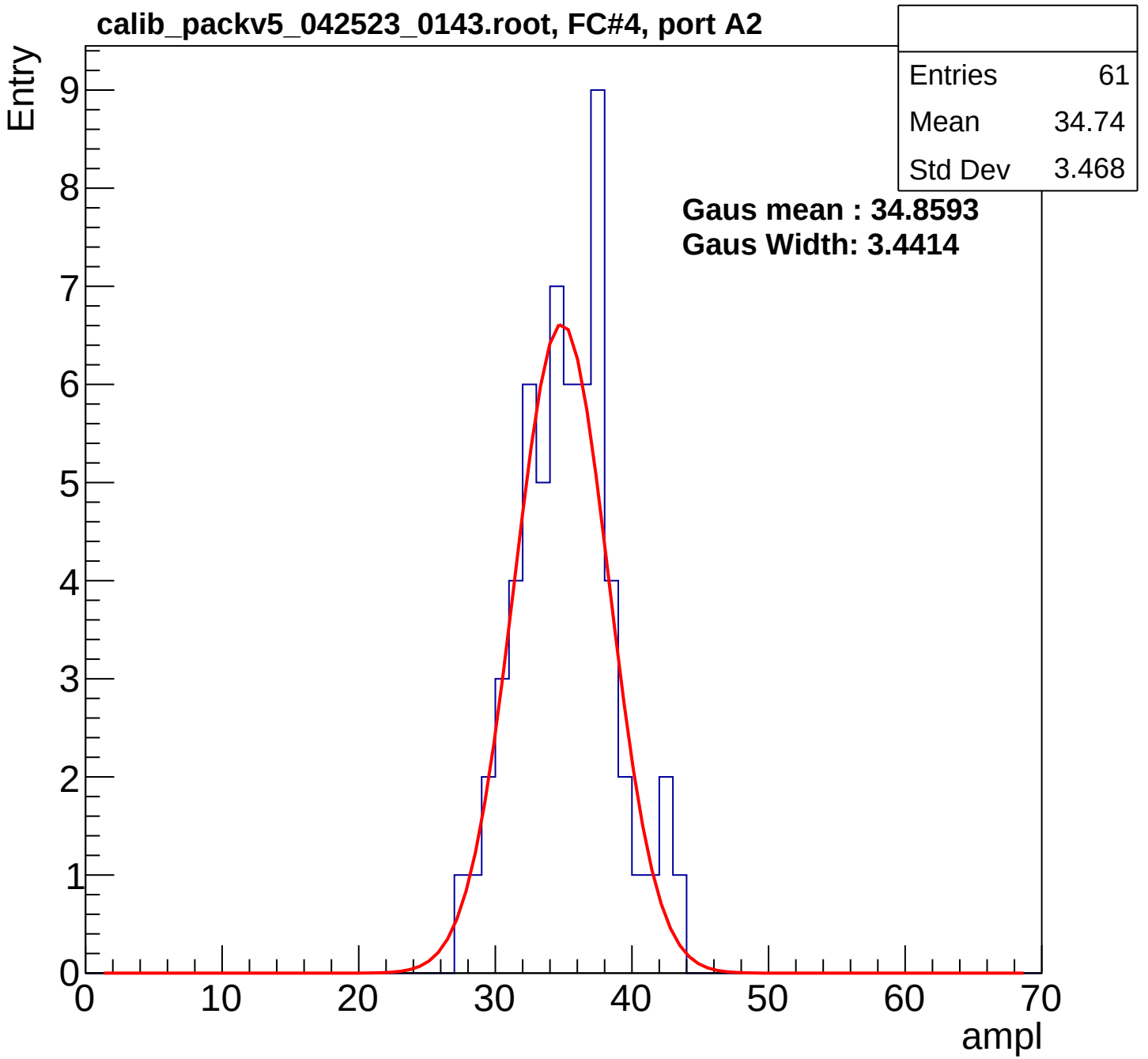

B1L100S, U5-ch0, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 54.67
Std Dev 3.202
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

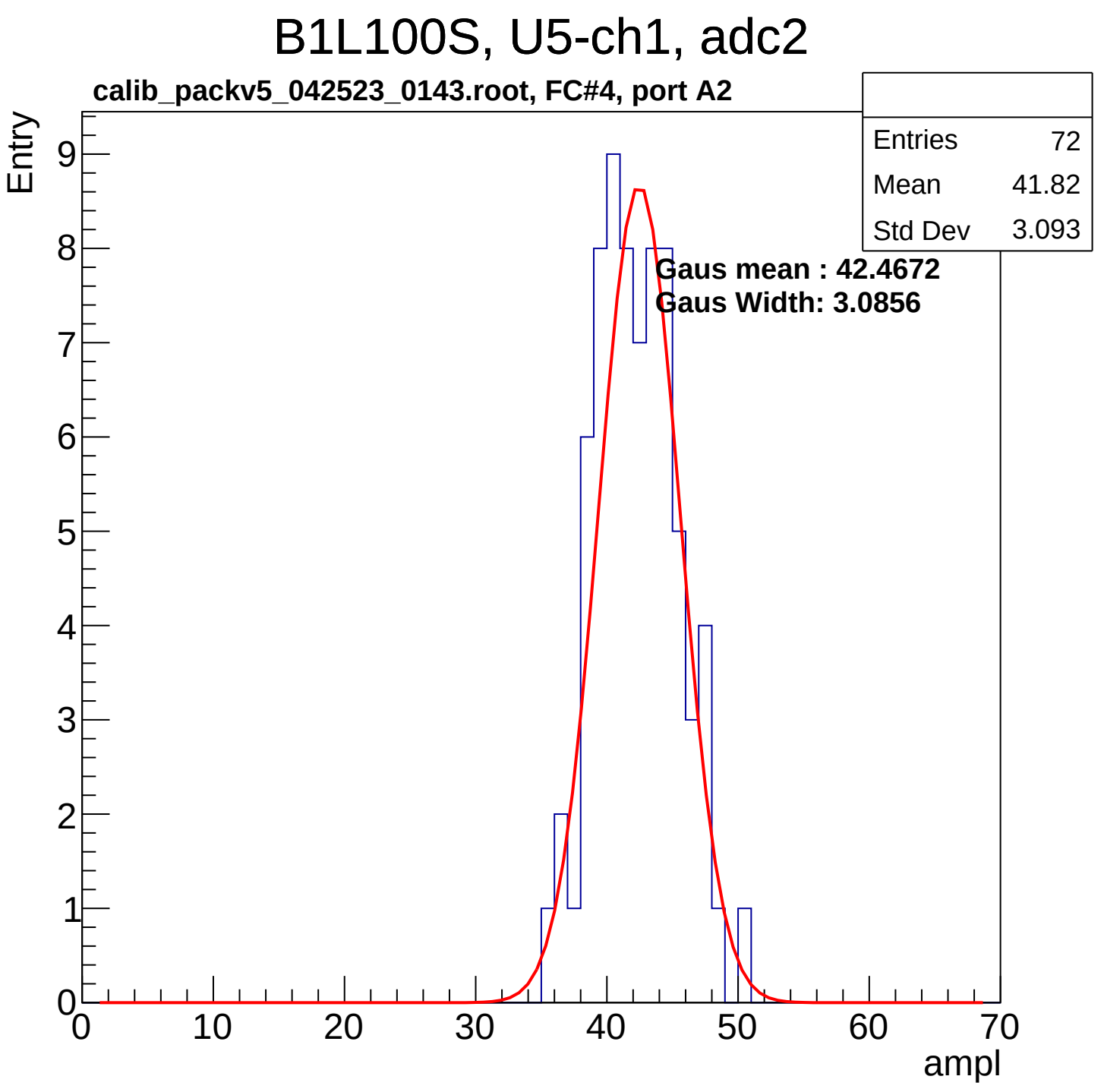

B1L100S, U5-ch0, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 45
Mean 59.24
Std Dev 2.566
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

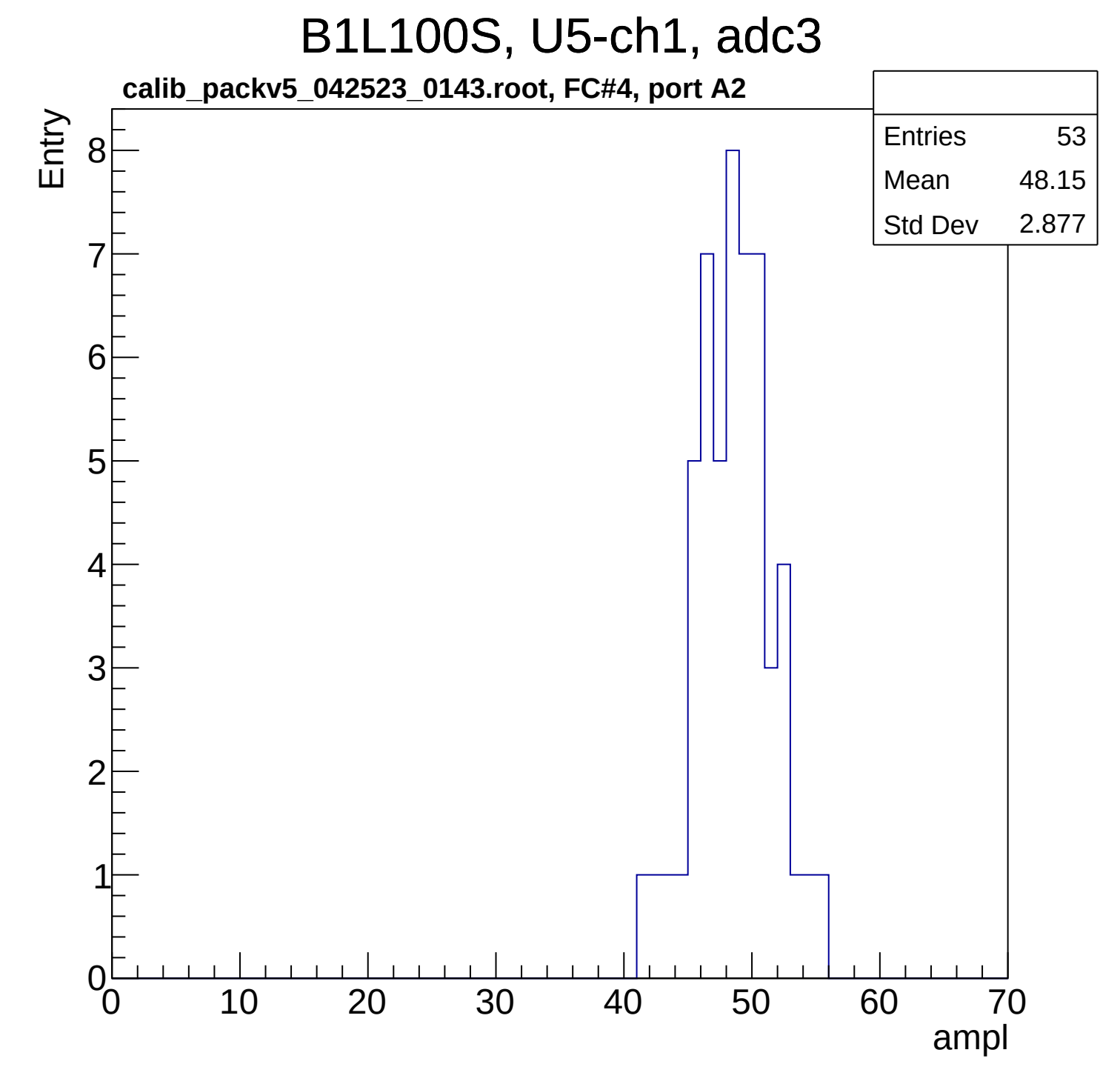

B1L100S, U5-ch0, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 16
Mean 57.38
Std Dev 14.9
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

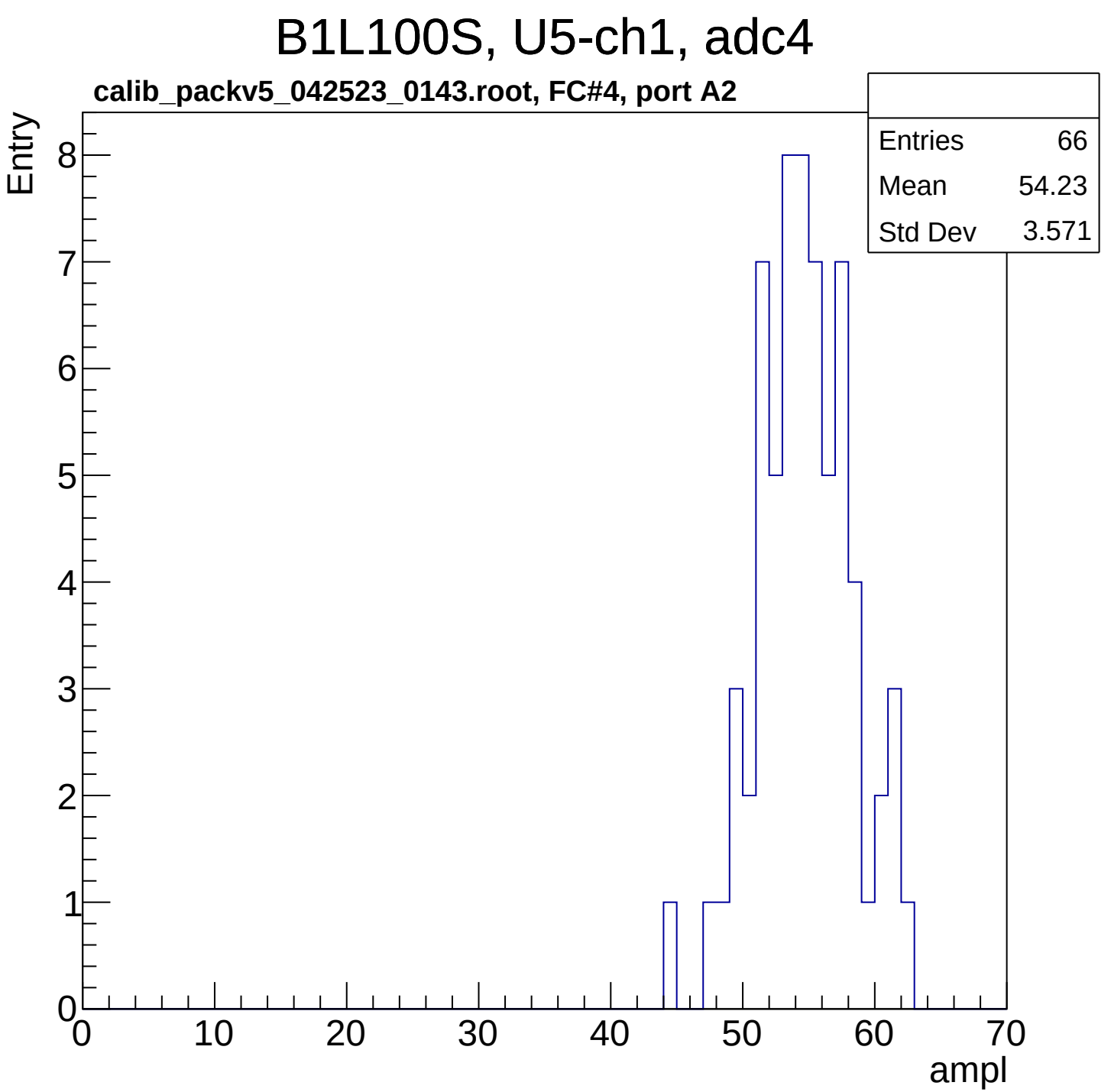

B1L100S, U5-ch0, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

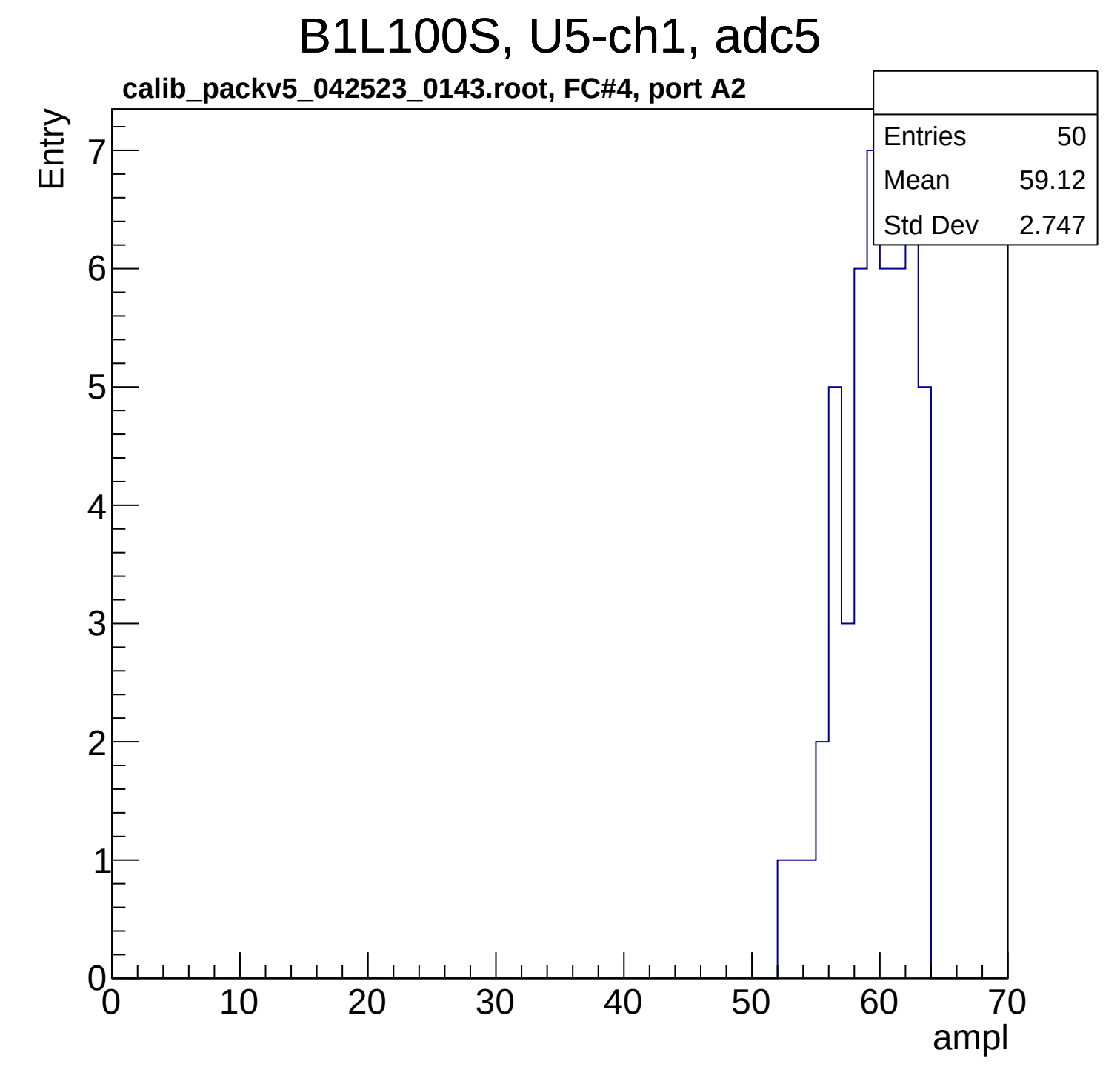

B1L100S, U5-ch1, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 75
Mean 28.53
Std Dev 3.746
Gaus mean : 29.3722
Gaus Width: 4.1486
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

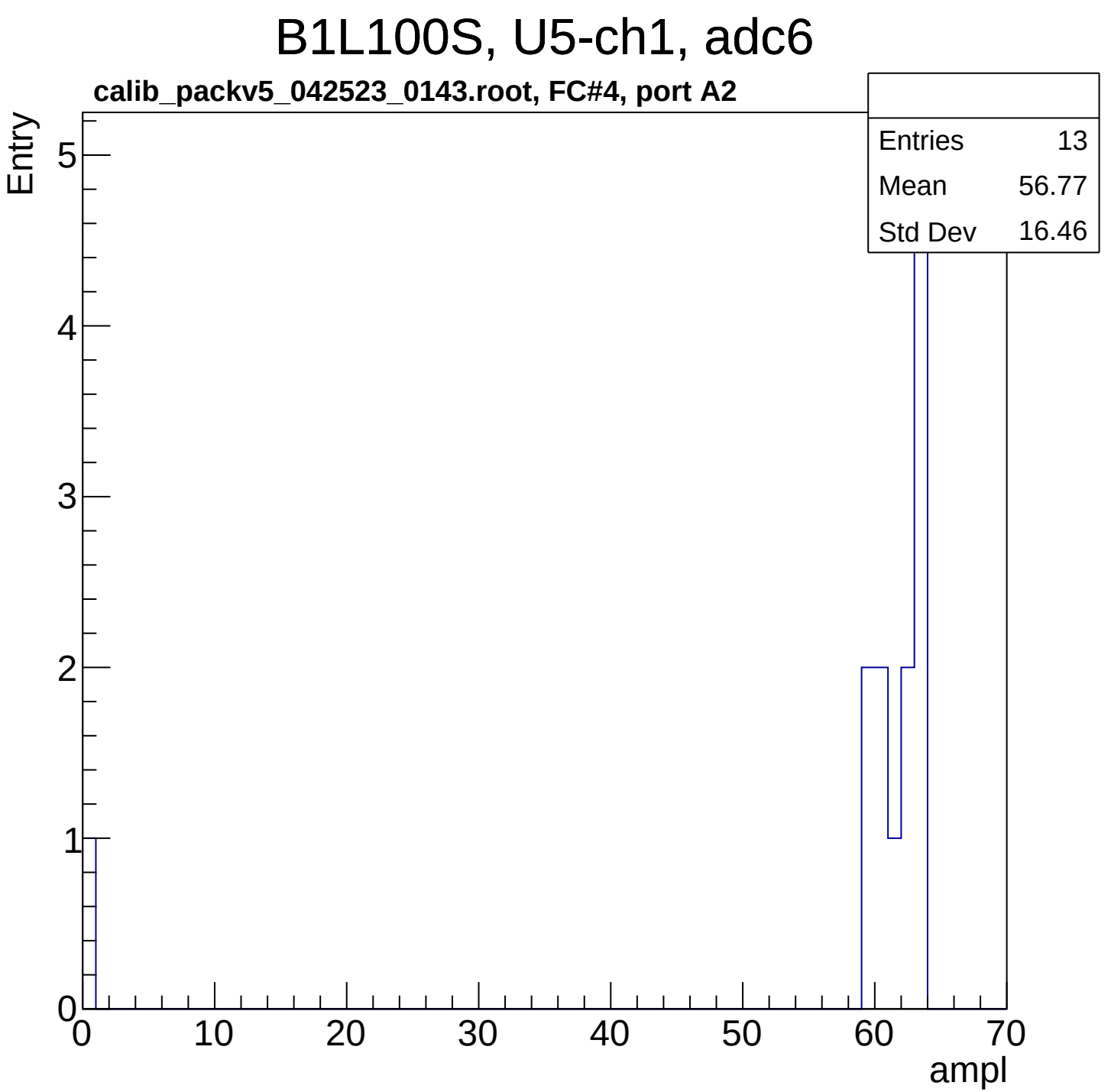

B1L100S, U5-ch1, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 34.74
Std Dev 3.468
Gaus mean : 34.8593
Gaus Width: 3.4414
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

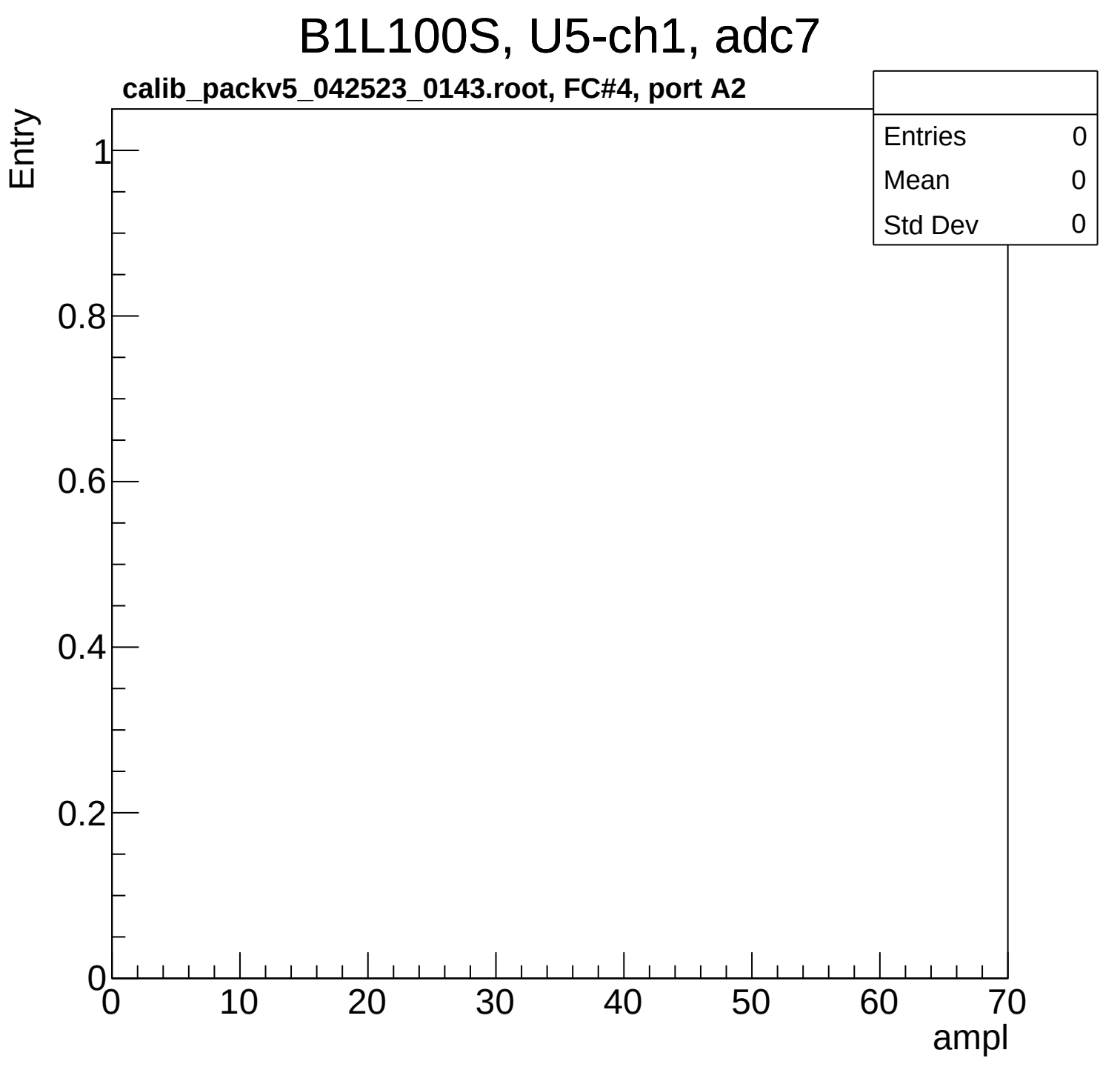

B1L100S, U5-ch1, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 41.82
Std Dev 3.093
Gaus mean : 42.4672
Gaus Width: 3.0856
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

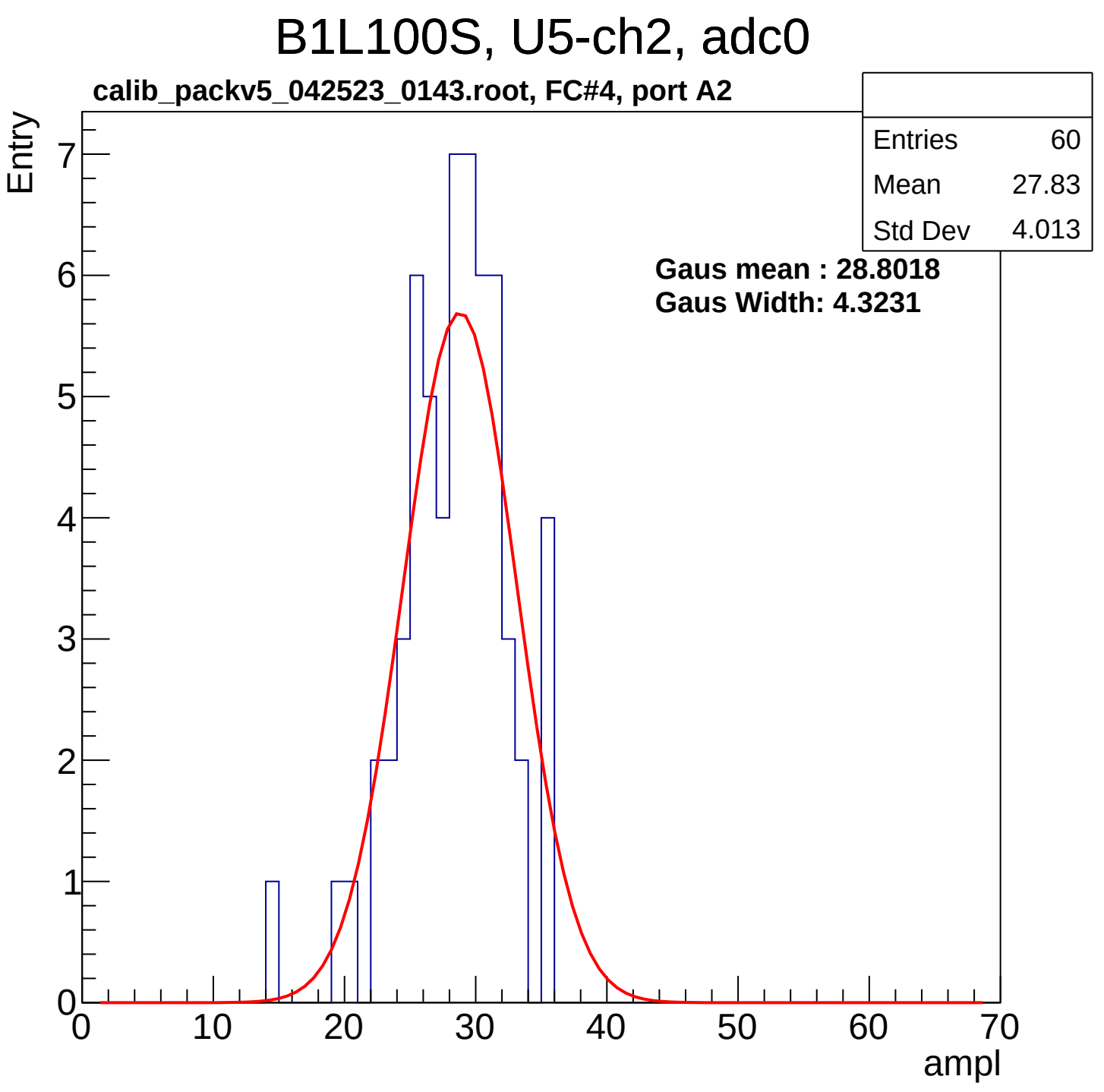

B1L100S, U5-ch1, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 48.15
Std Dev 2.877
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

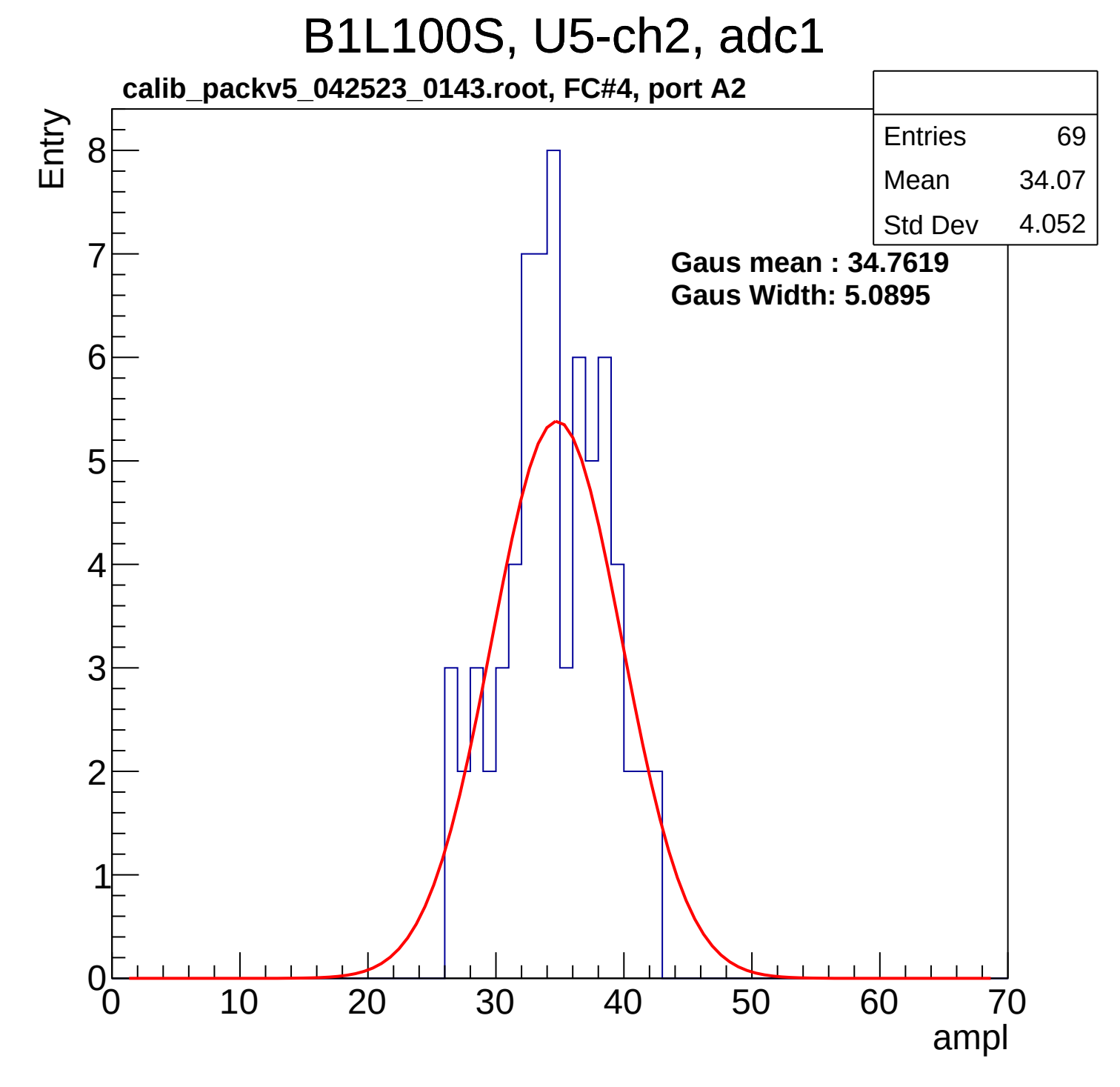

B1L100S, U5-ch1, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 54.23
Std Dev 3.571
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

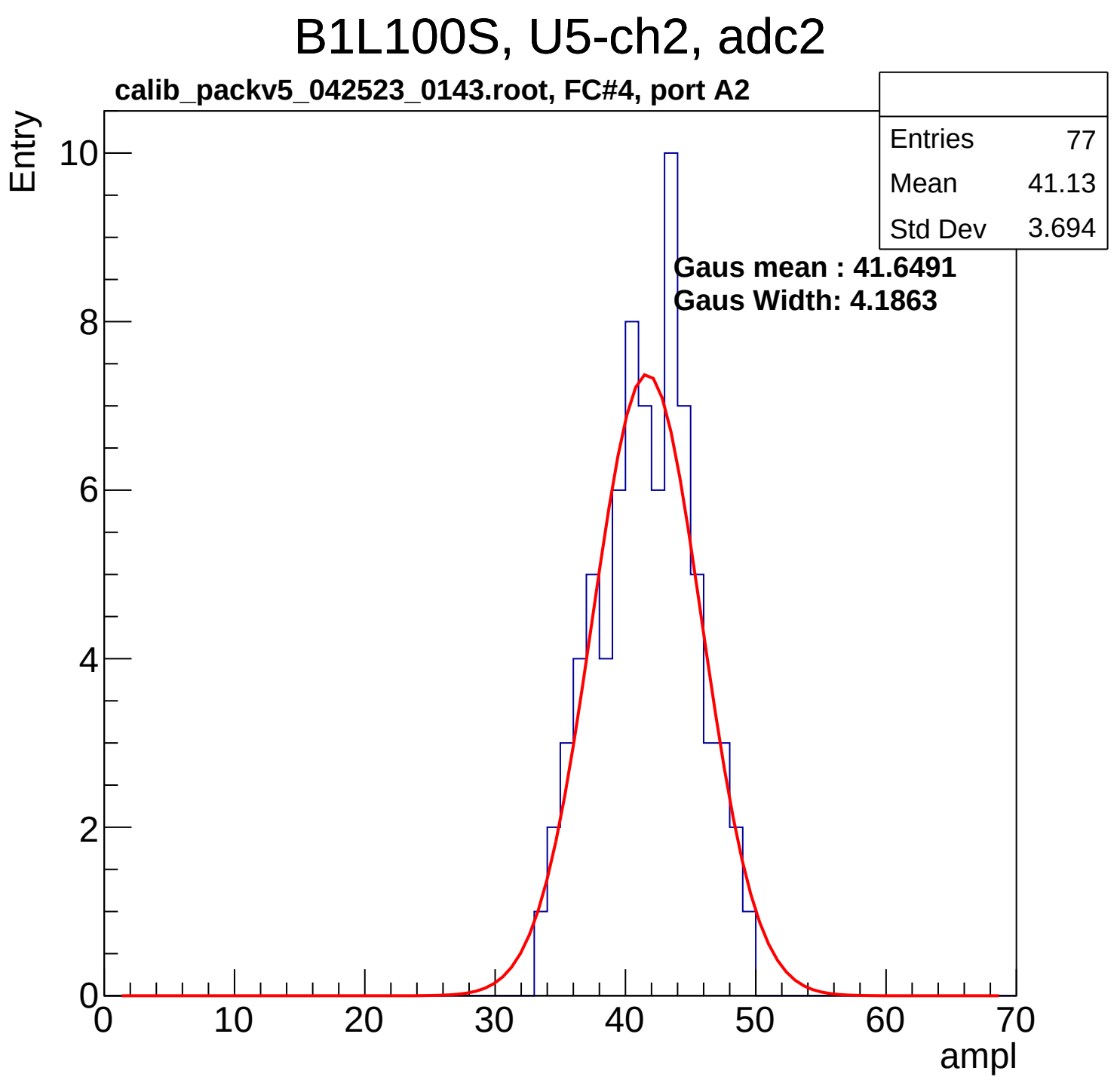

B1L100S, U5-ch1, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 59.12
Std Dev 2.747
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

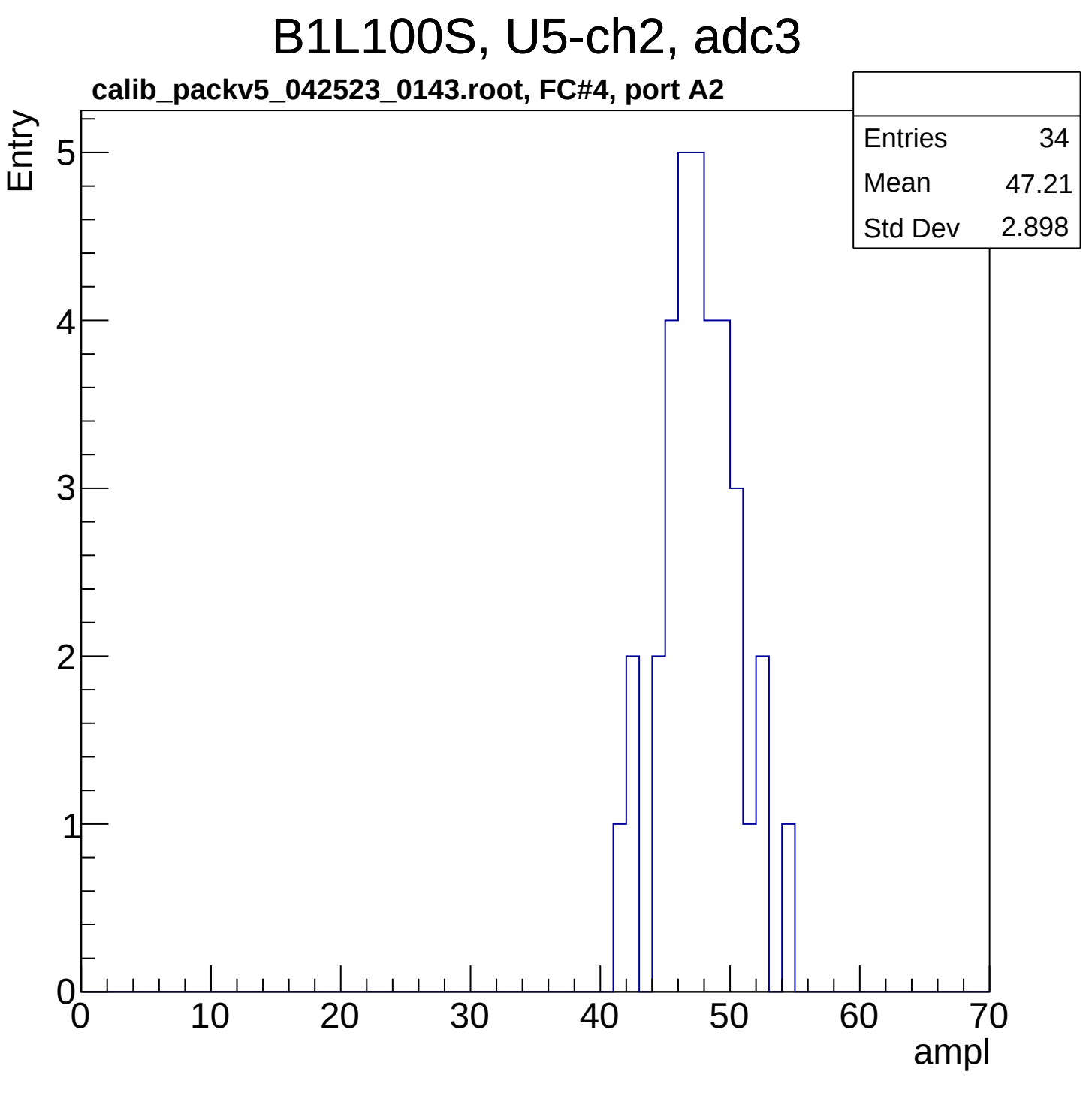

B1L100S, U5-ch1, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 13
Mean 56.77
Std Dev 16.46
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

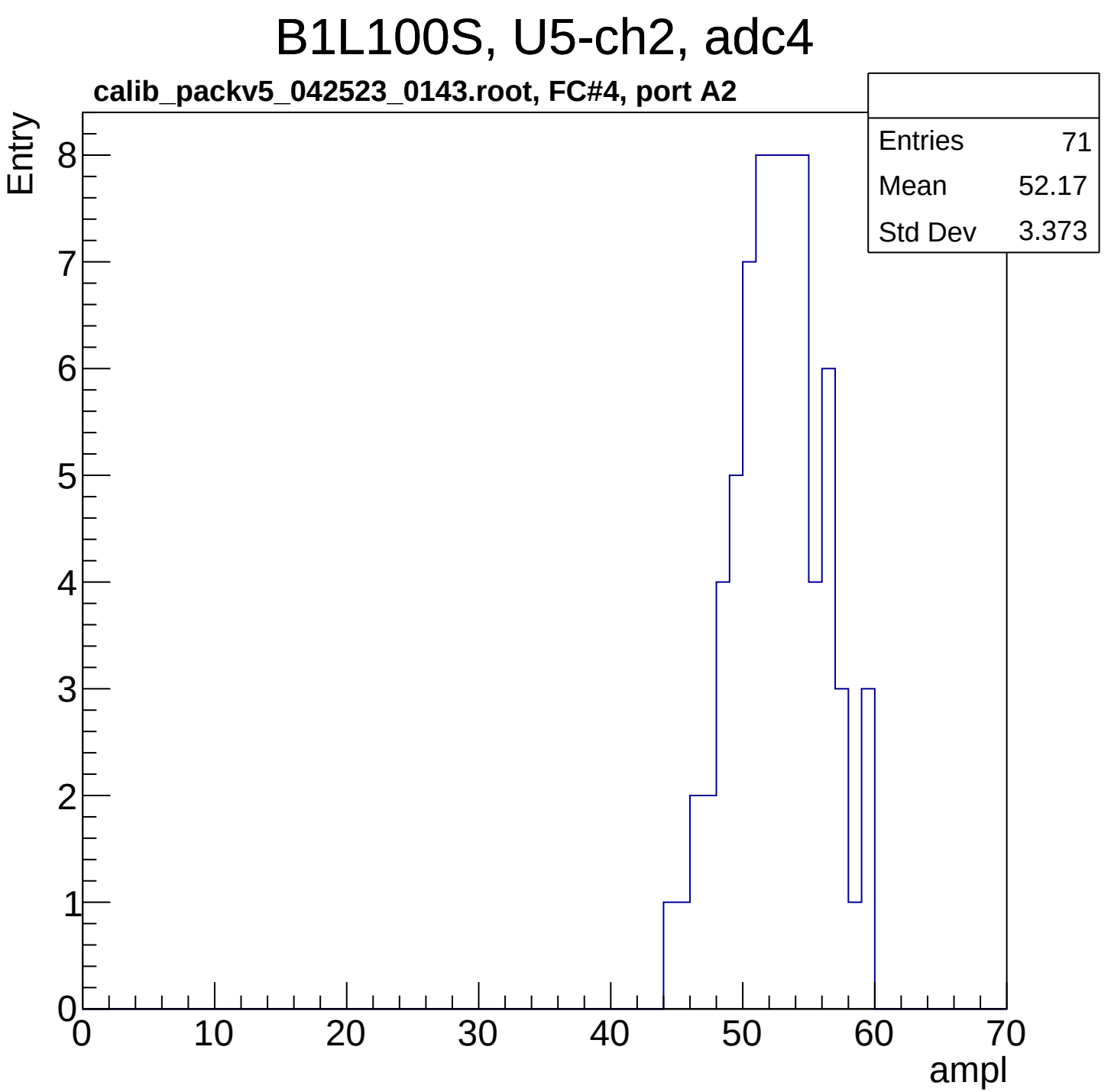

B1L100S, U5-ch1, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch2, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 27.83
Std Dev 4.013
Gaus mean : 28.8018
Gaus Width: 4.3231
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U5-ch2, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 34.07
Std Dev 4.052
Gaus mean : 34.7619
Gaus Width: 5.0895
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch2, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 77
Mean 41.13
Std Dev 3.694
Gaus mean : 41.6491
Gaus Width: 4.1863
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch2, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 34
Mean 47.21
Std Dev 2.898
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch2, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 52.17
Std Dev 3.373
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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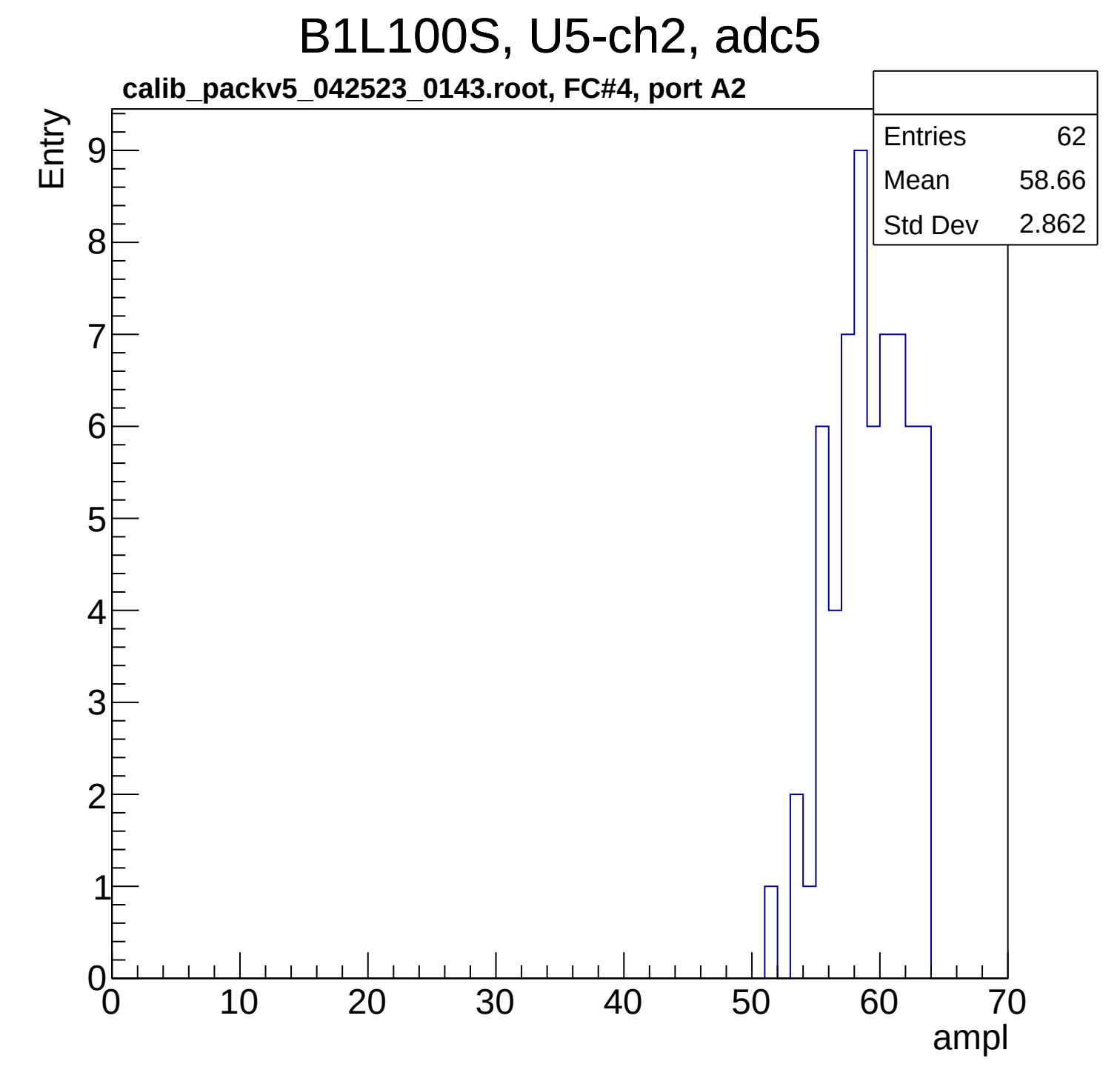
40
50
60
70


B1L100S, U5-ch2, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 58.66
Std Dev 2.862
Entry
ampl
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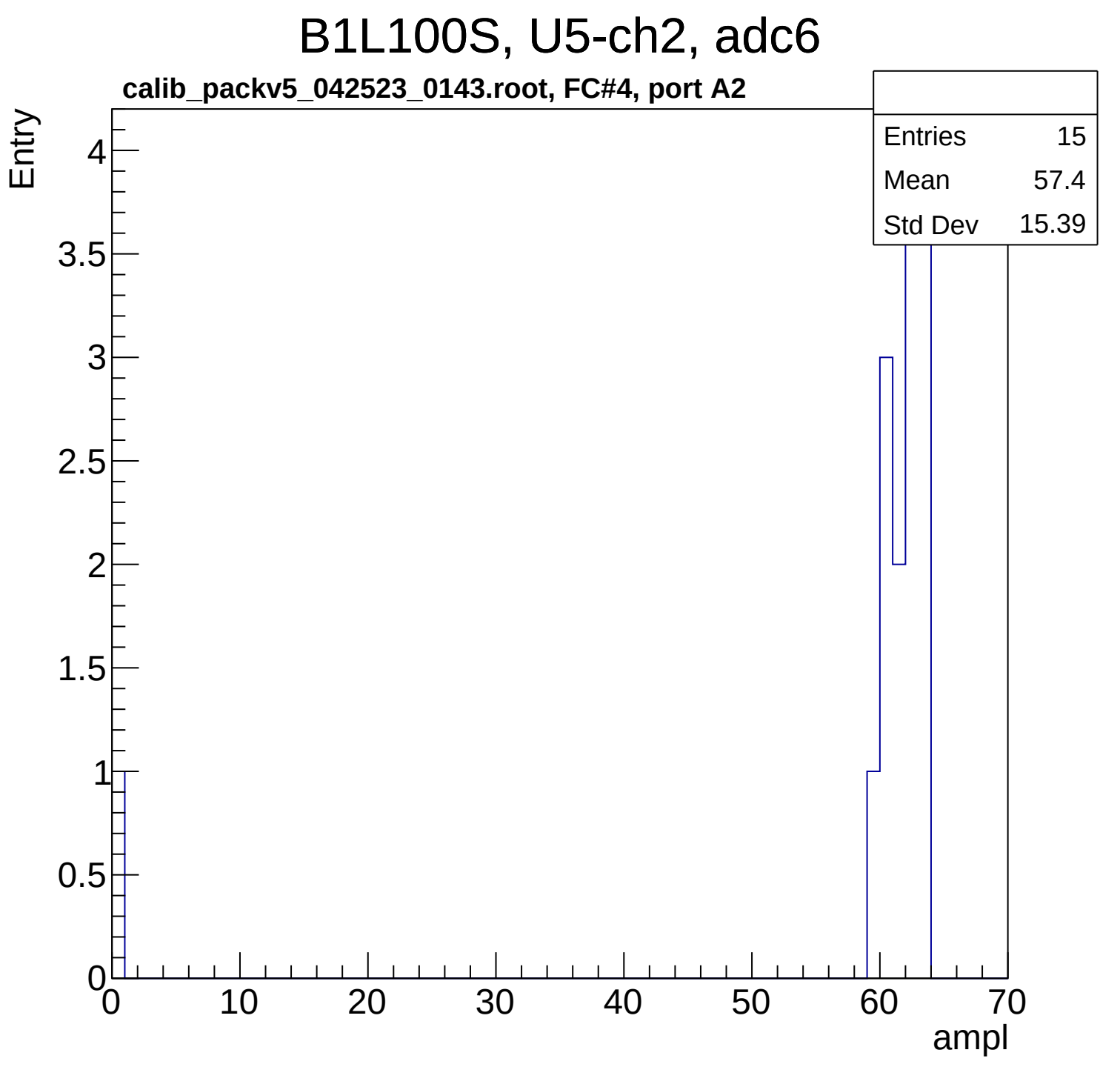
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch2, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 15
Mean 57.4
Std Dev 15.39
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
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20
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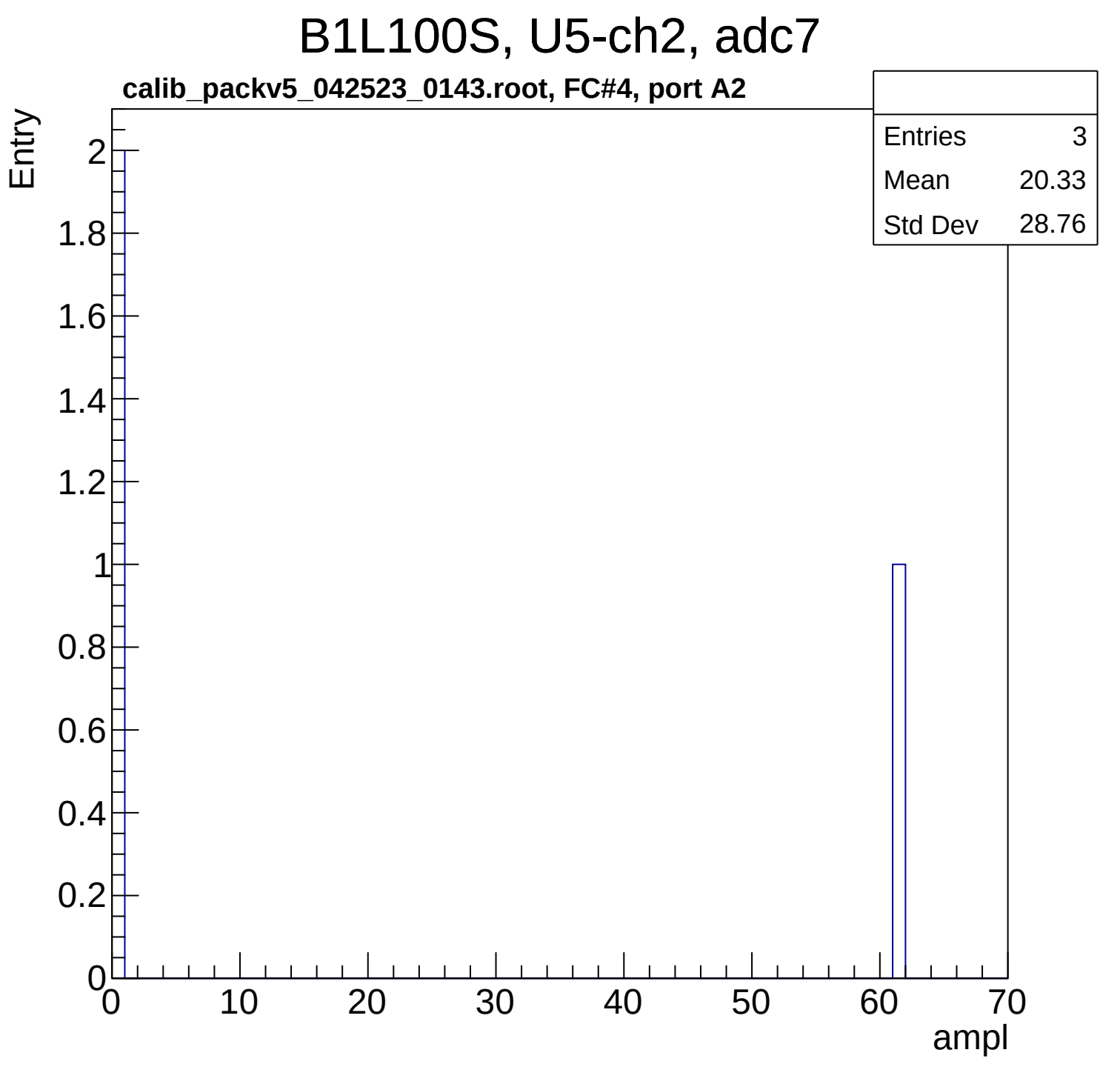
40
50
60
70


B1L100S, U5-ch2, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 20.33
Std Dev 28.76
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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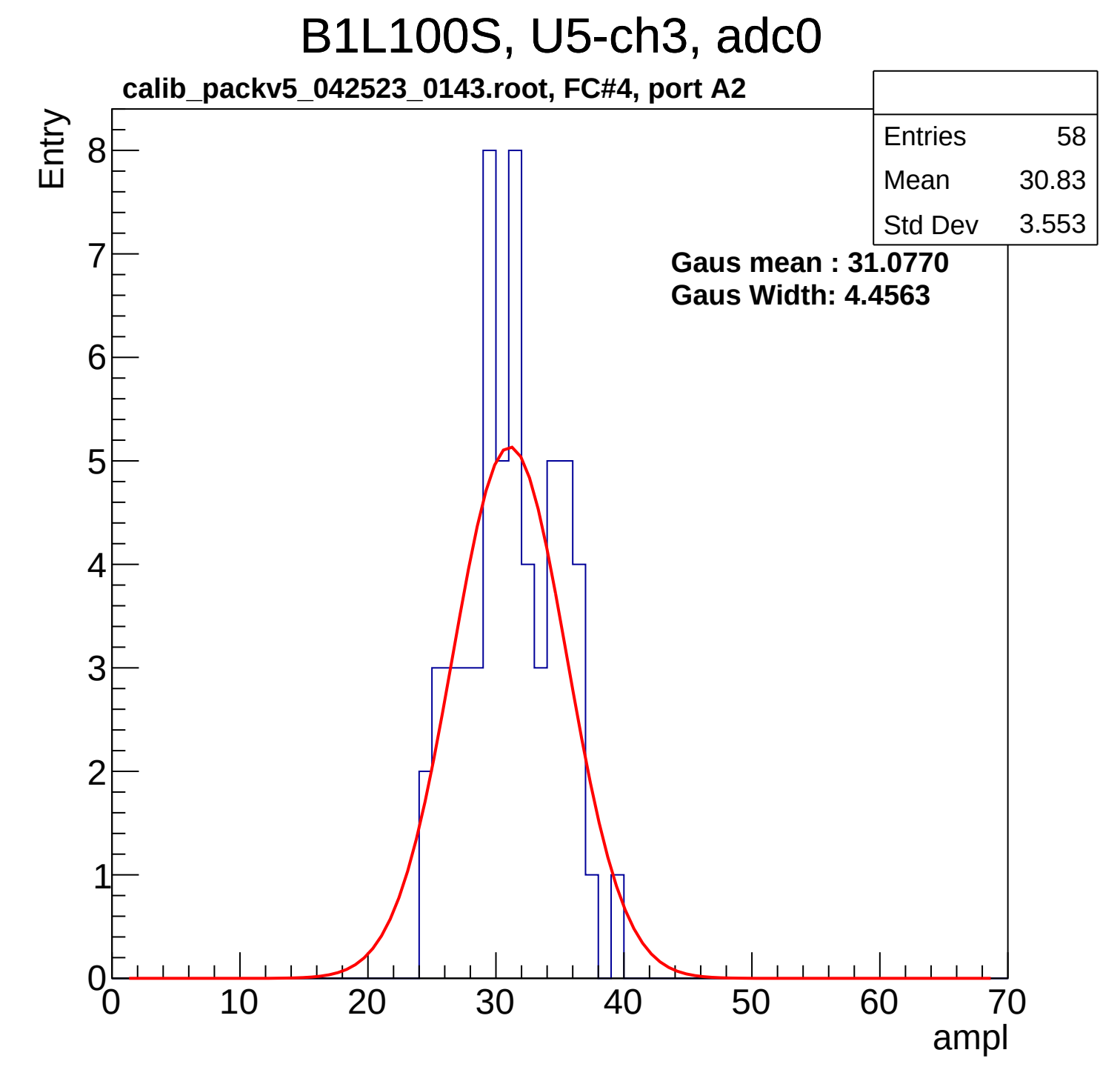
B1L100S, U5-ch3, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 30.83
Std Dev 3.553
Gaus mean : 31.0770
Gaus Width: 4.4563
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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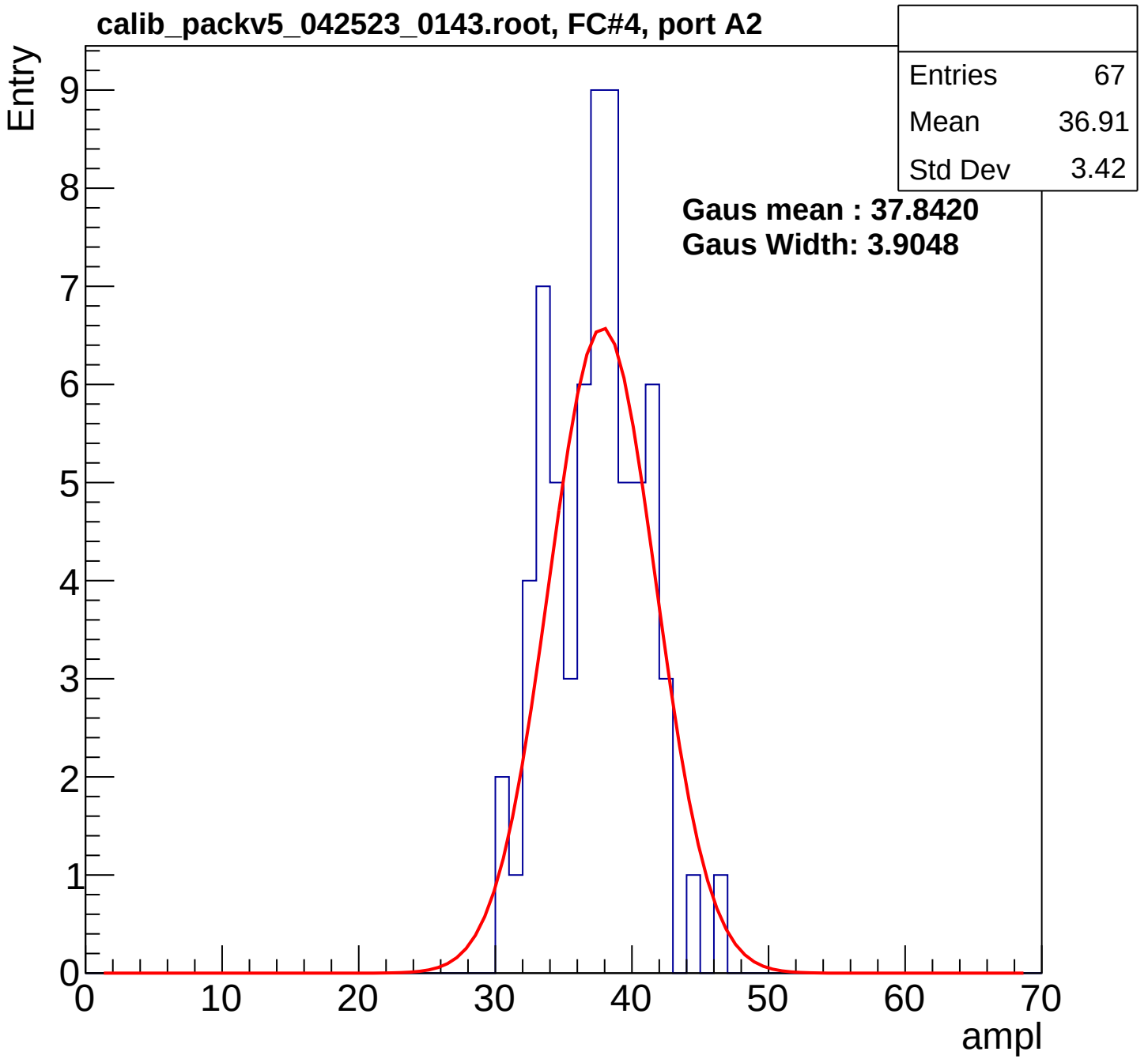
B1L100S, U5-ch3, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 36.91
Std Dev 3.42
Gaus mean : 37.8420
Gaus Width: 3.9048
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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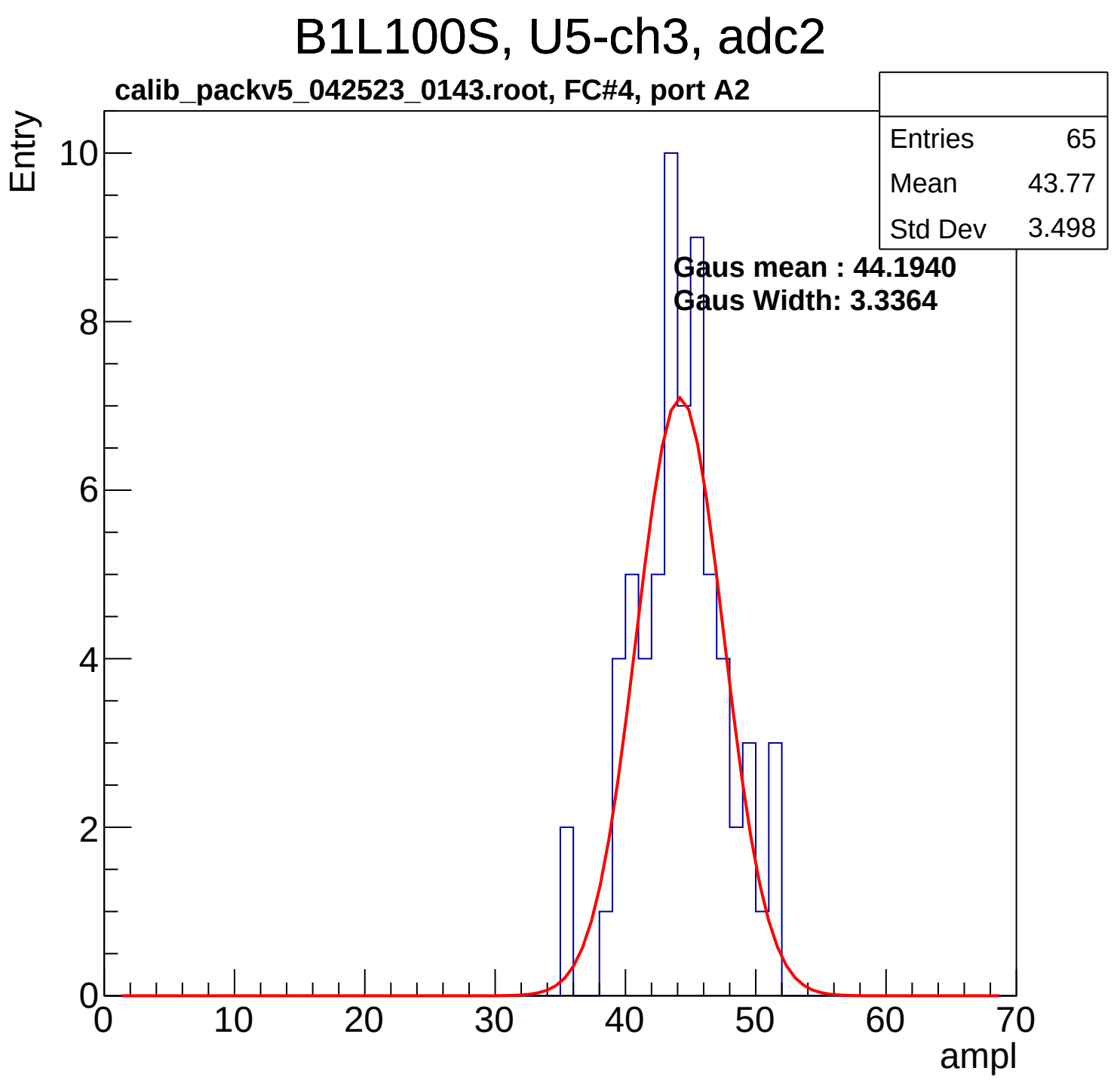
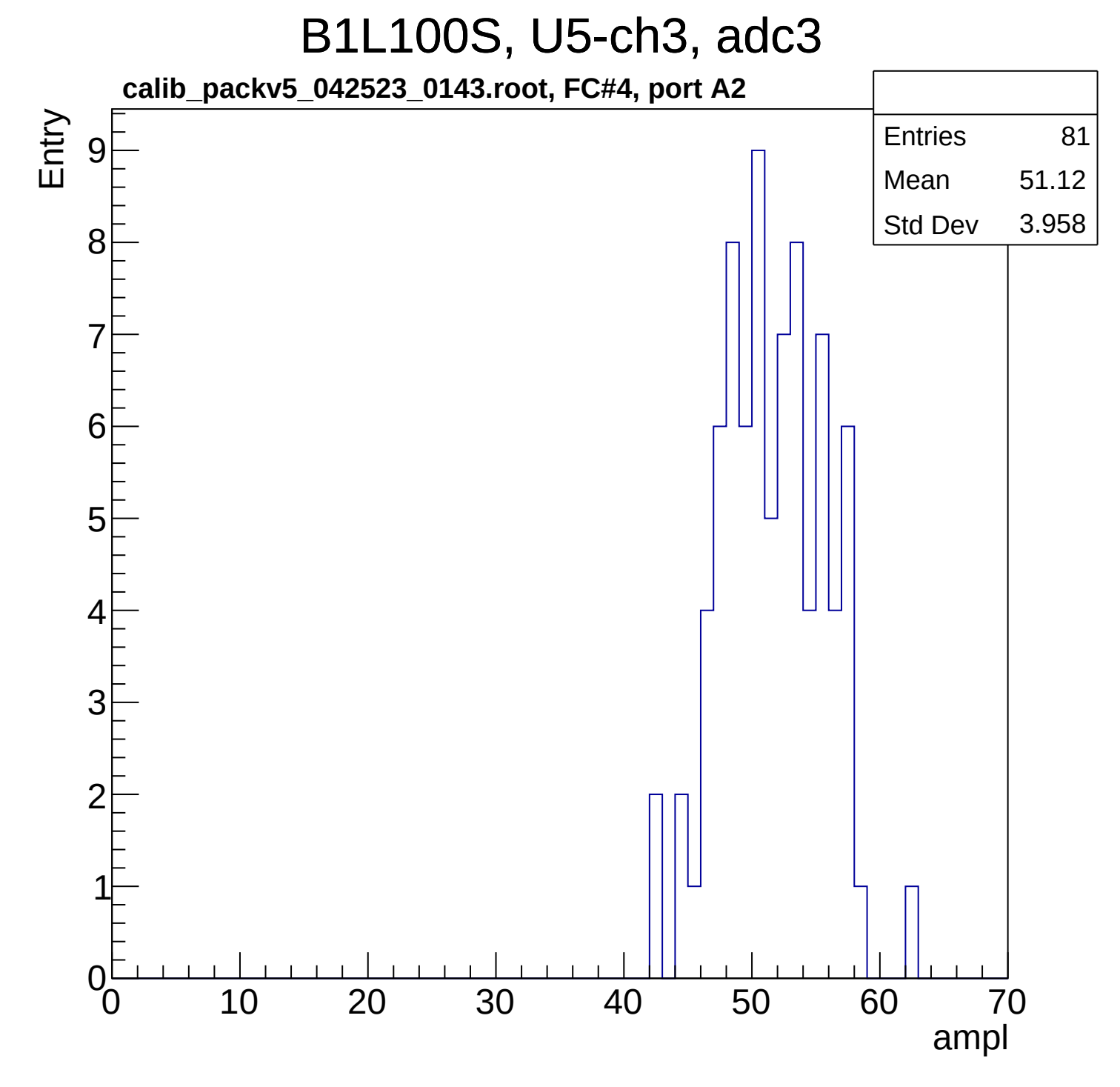
40
50
60
70


B1L100S, U5-ch3, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 43.77
Std Dev 3.498
Gaus mean : 44.1940
Gaus Width: 3.3364
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch3, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 81
Mean 51.12
Std Dev 3.958
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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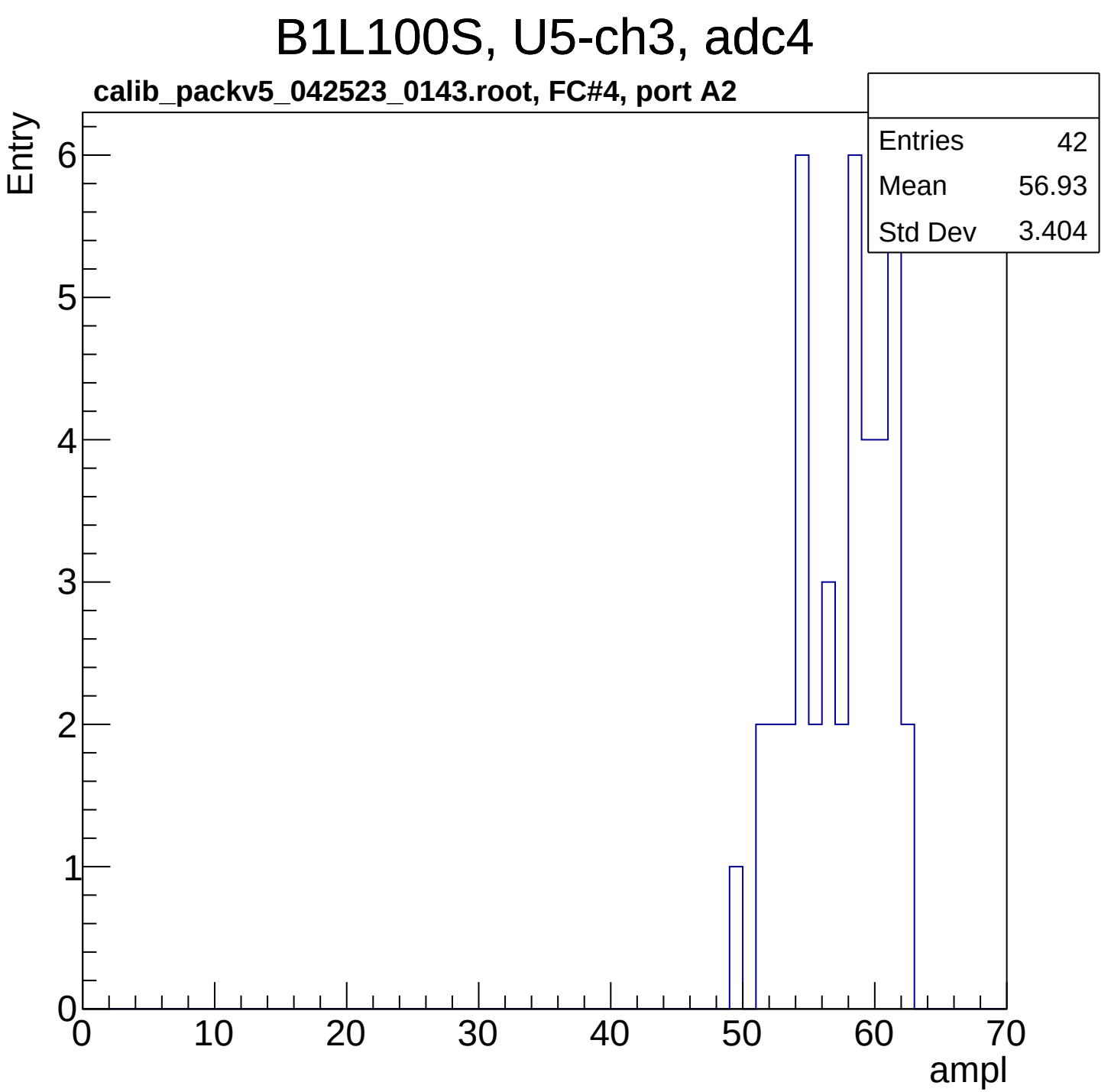
40
50
60
70


B1L100S, U5-ch3, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 42
Mean 56.93
Std Dev 3.404
Entry
ampl
0
1
2
3
4
5
6
0
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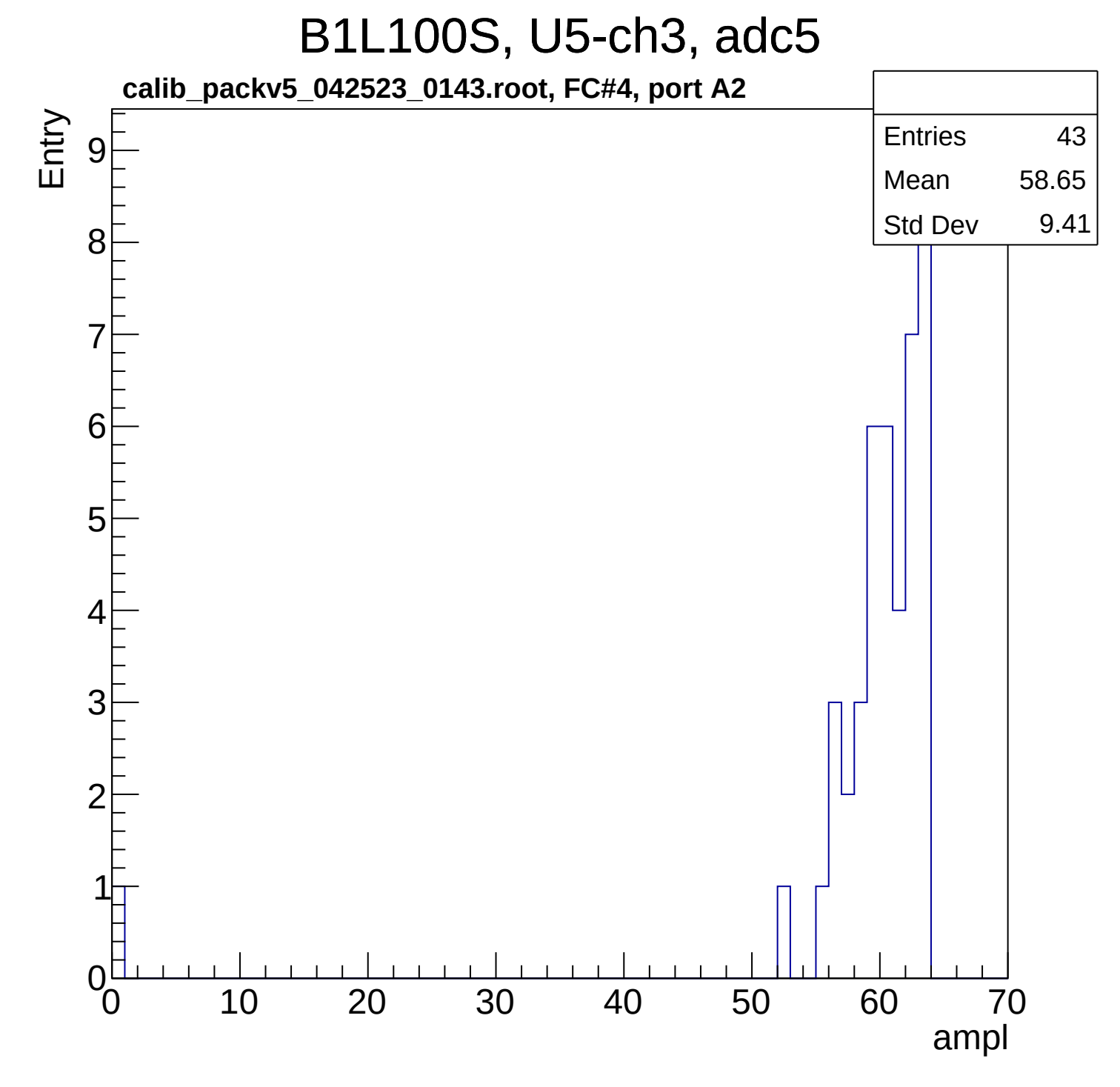
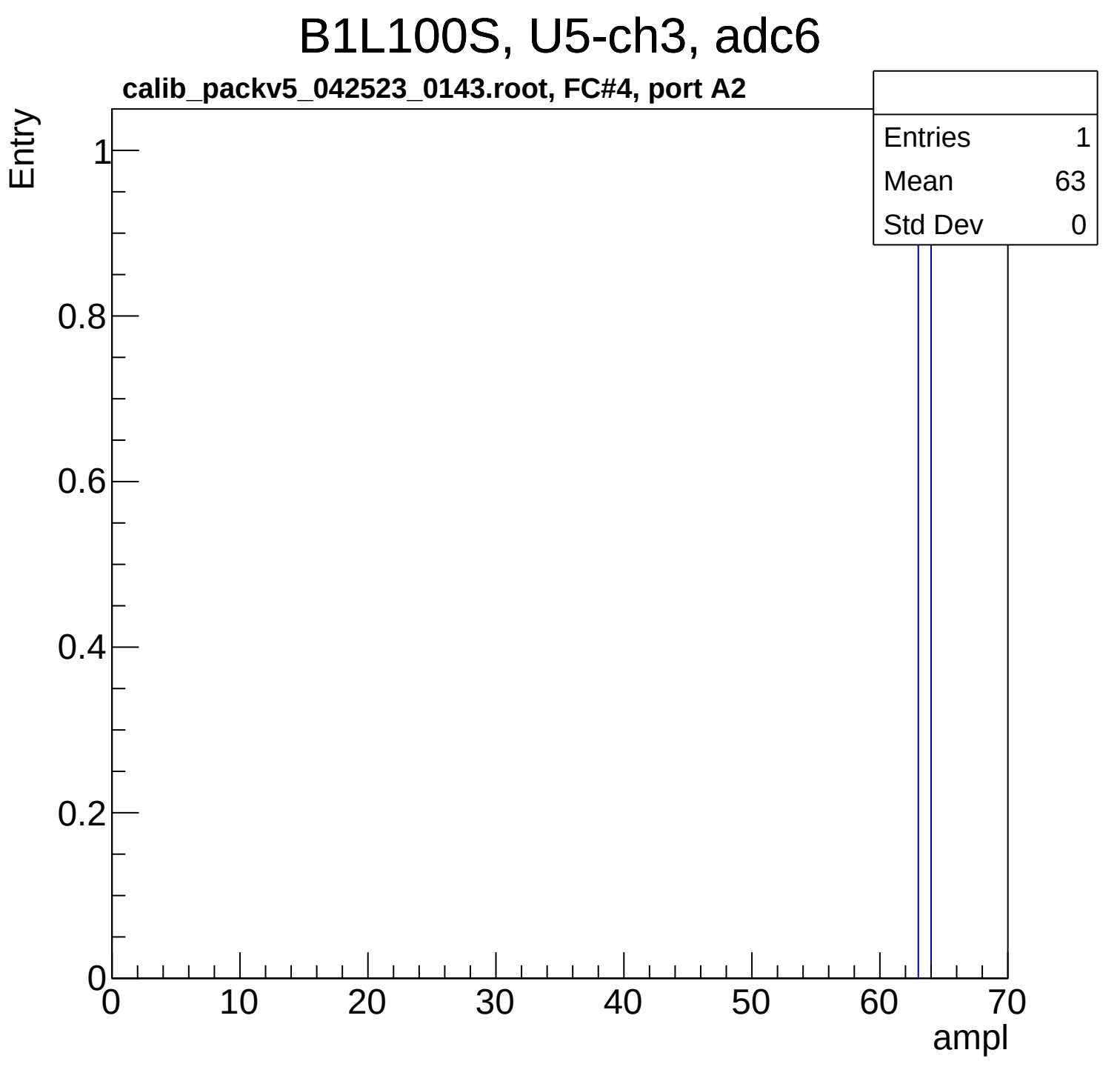
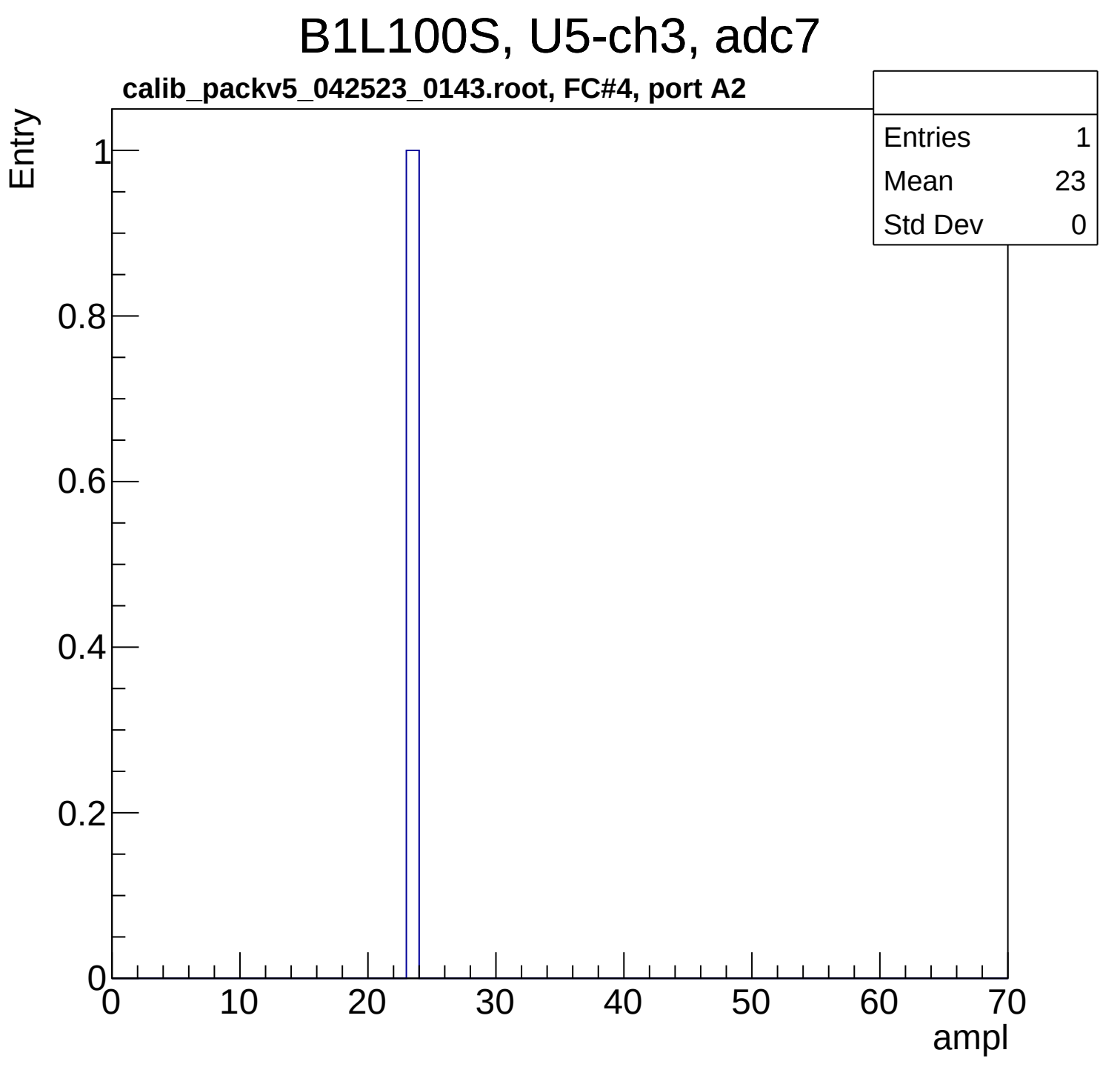
30
40
50
60
70


B1L100S, U5-ch3, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 43
Mean 58.65
Std Dev 9.41
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch3, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch3, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 23
Std Dev 0
Entry
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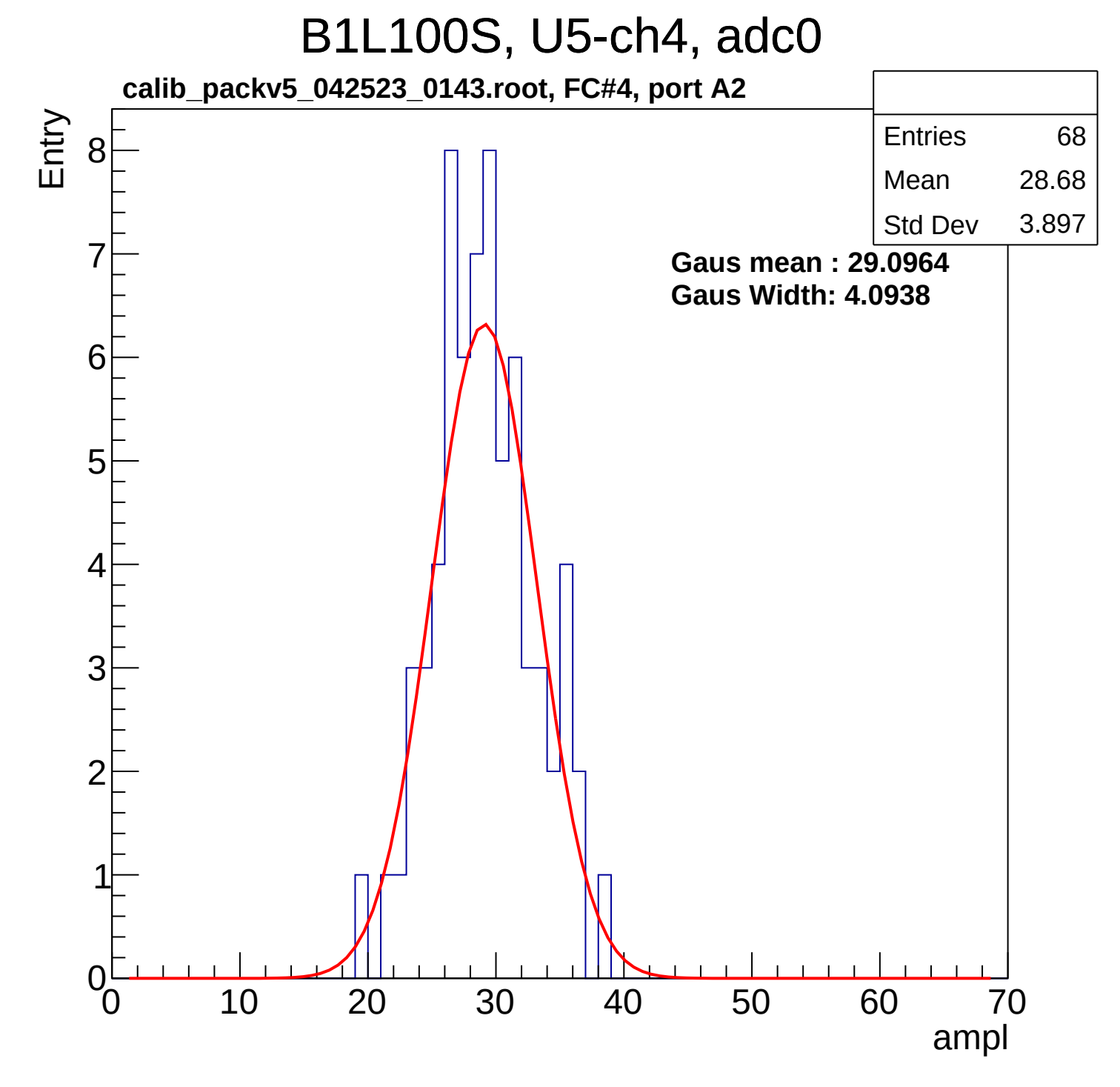
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch4, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 28.68
Std Dev 3.897
Gaus mean : 29.0964
Gaus Width: 4.0938
Entry
ampl
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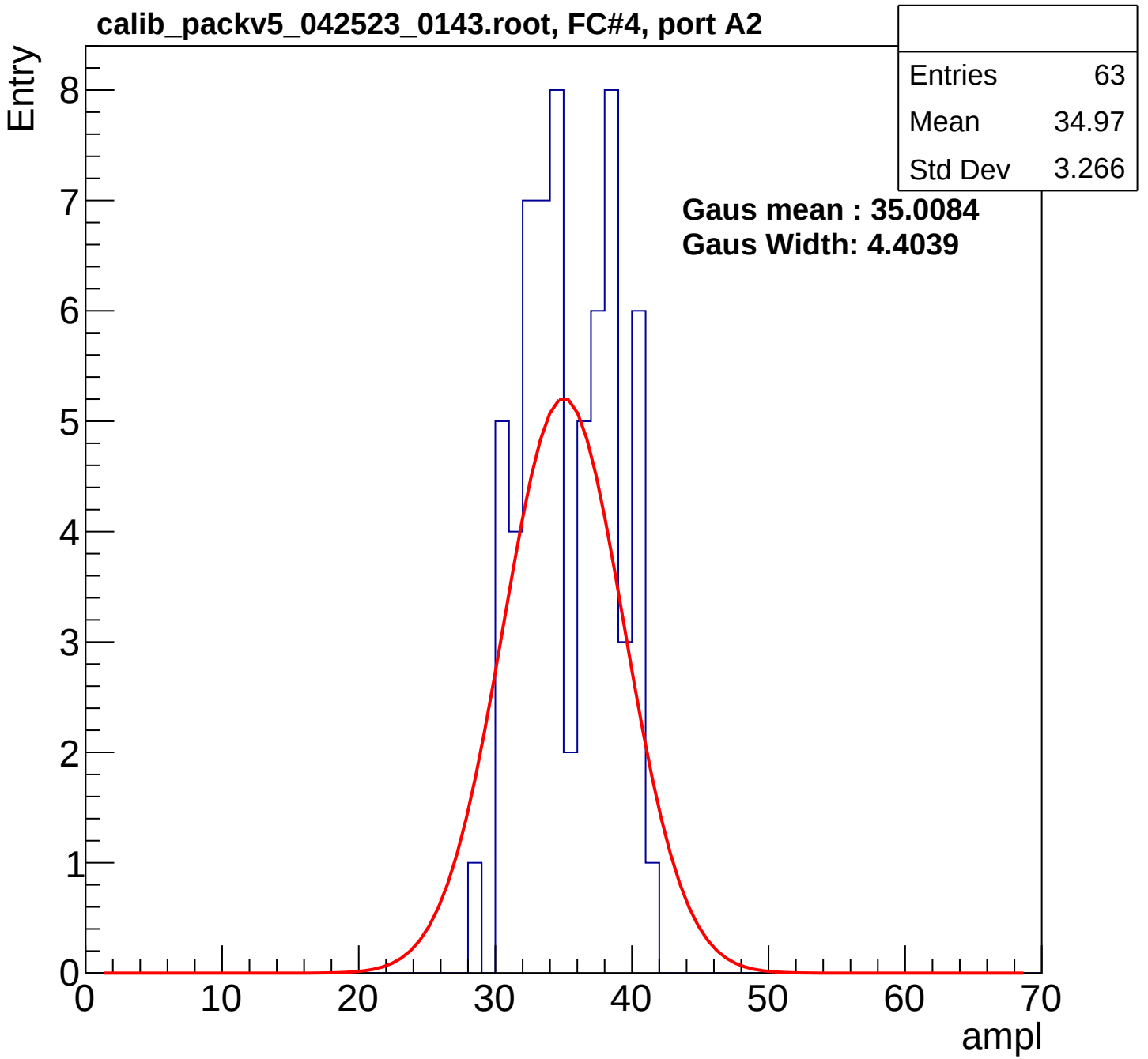
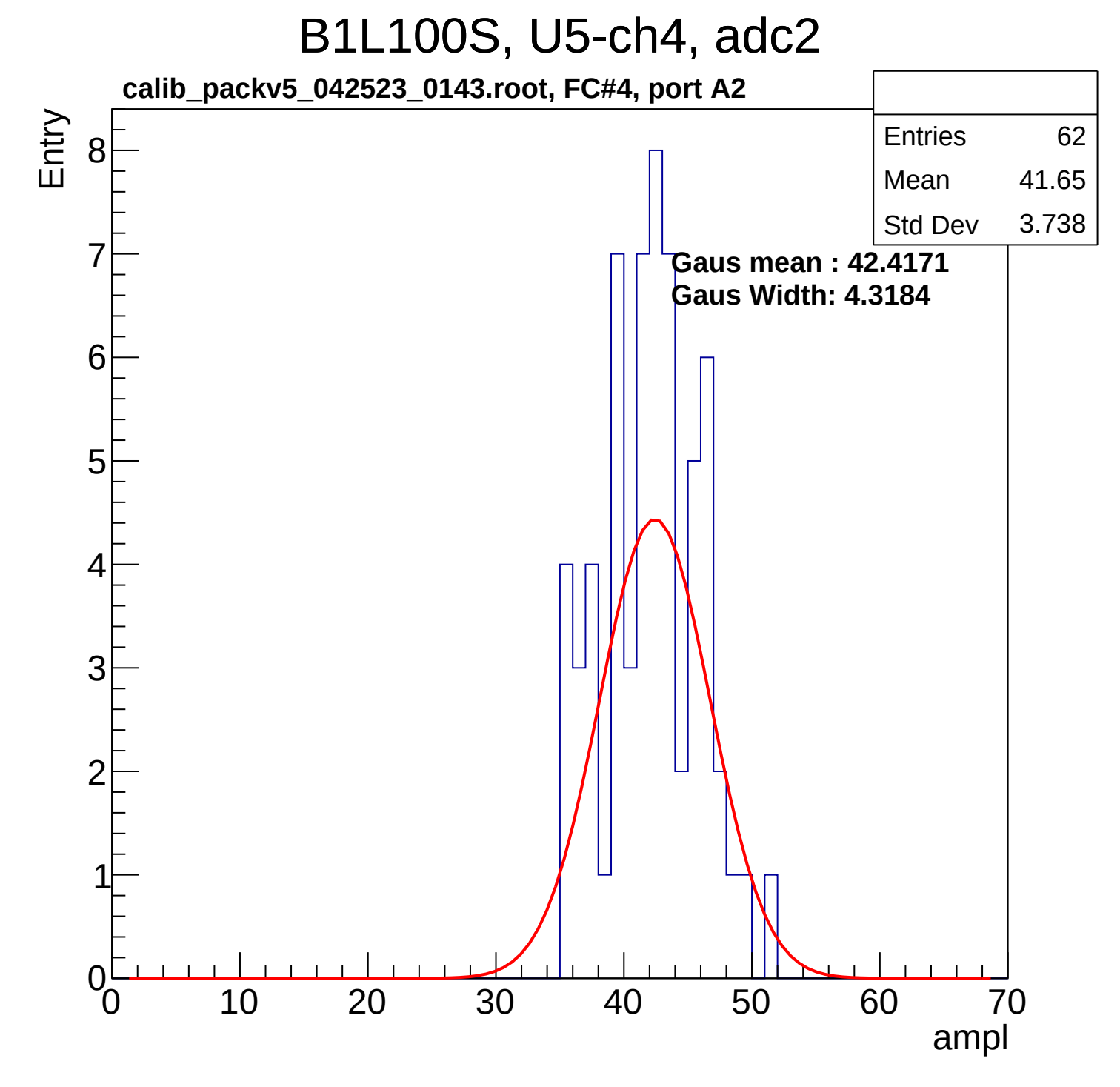
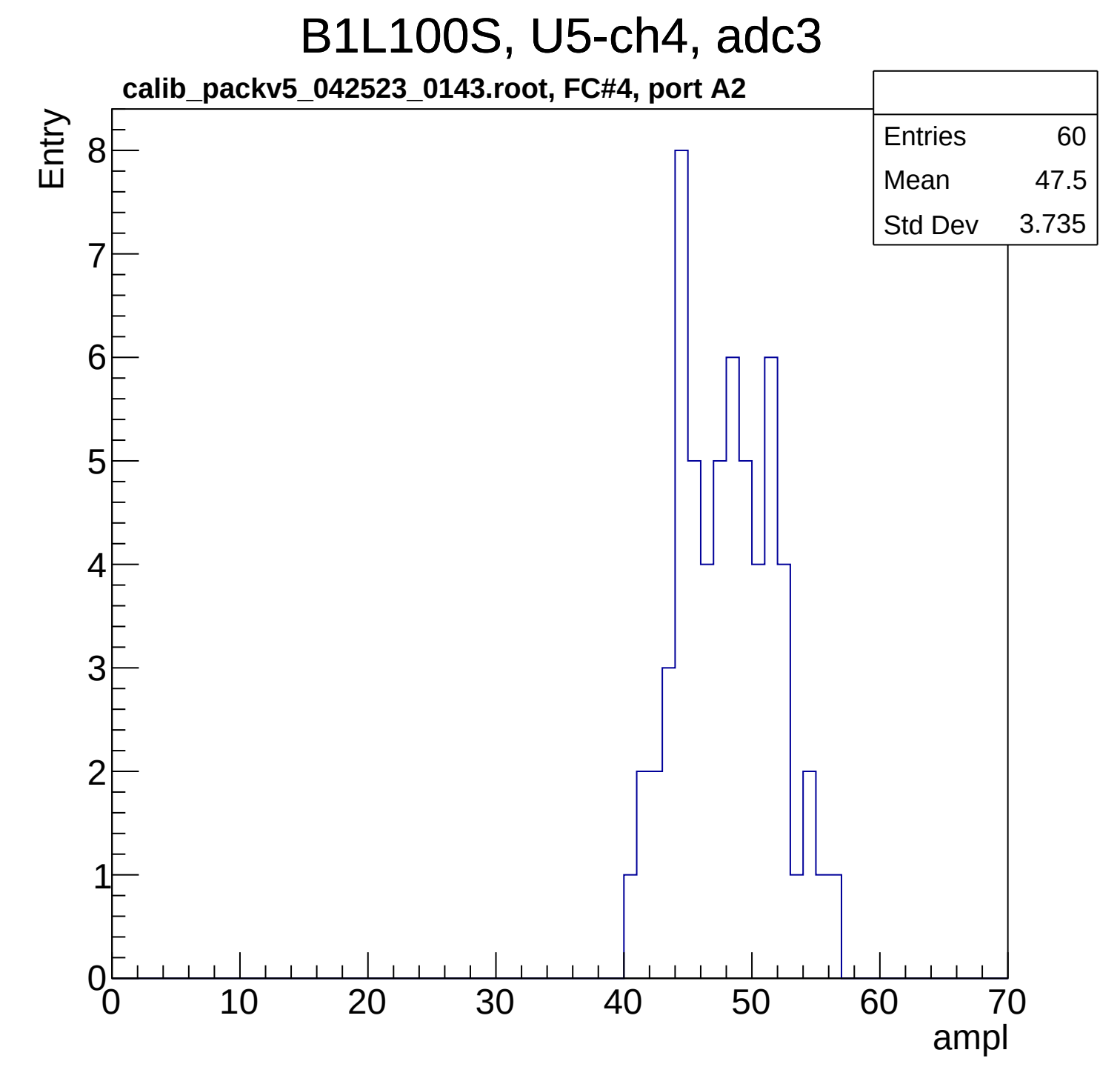
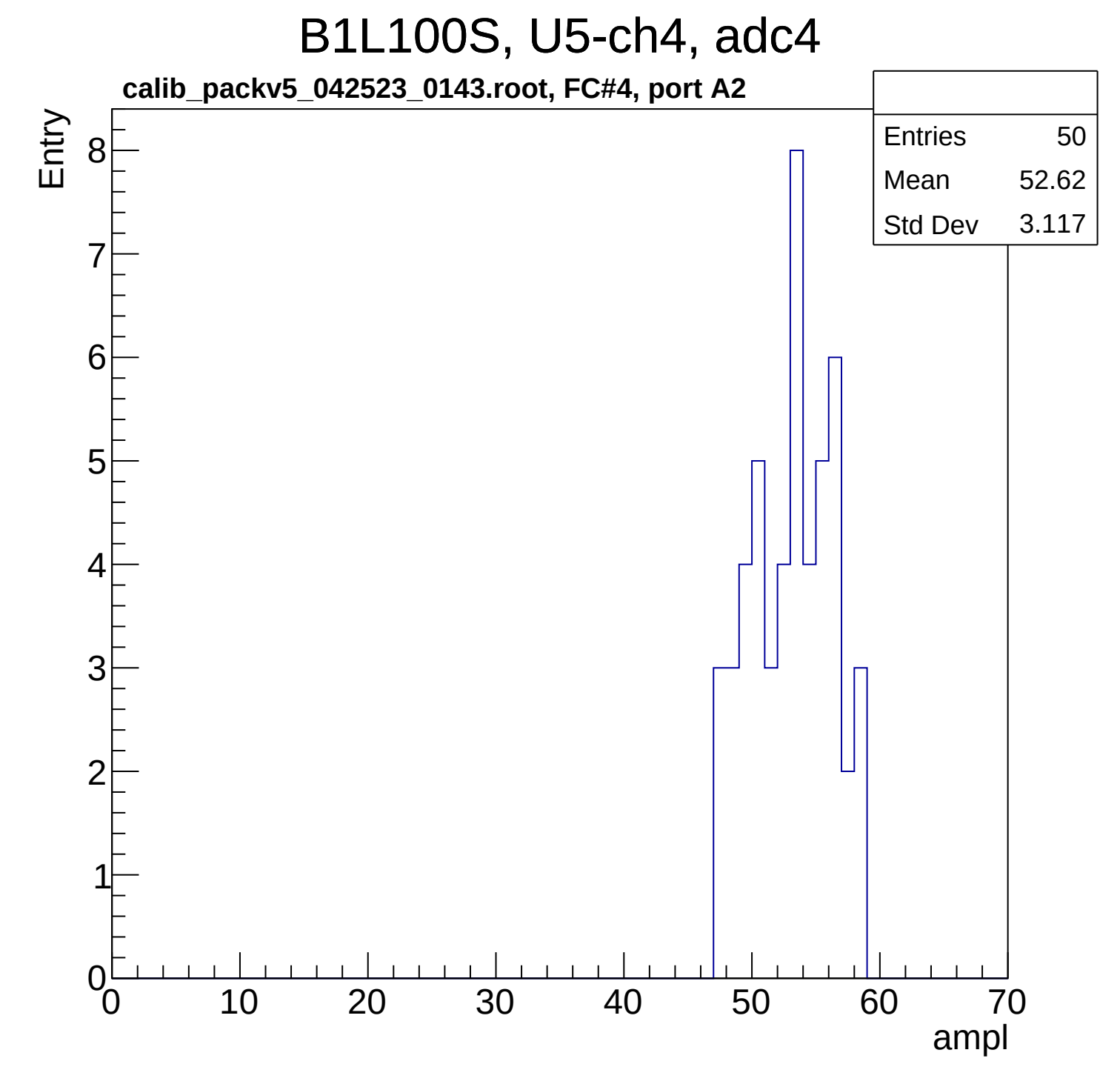
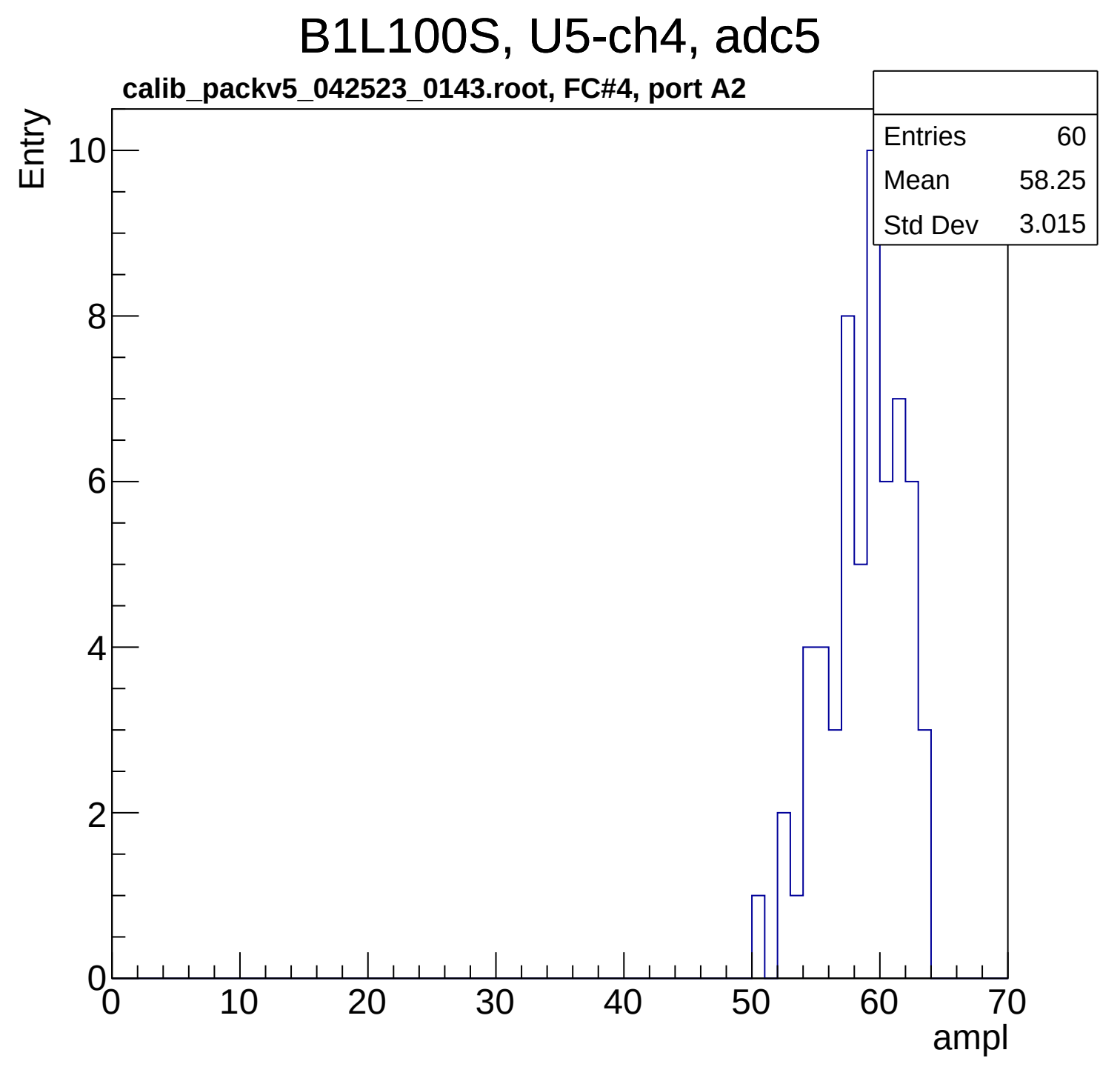
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

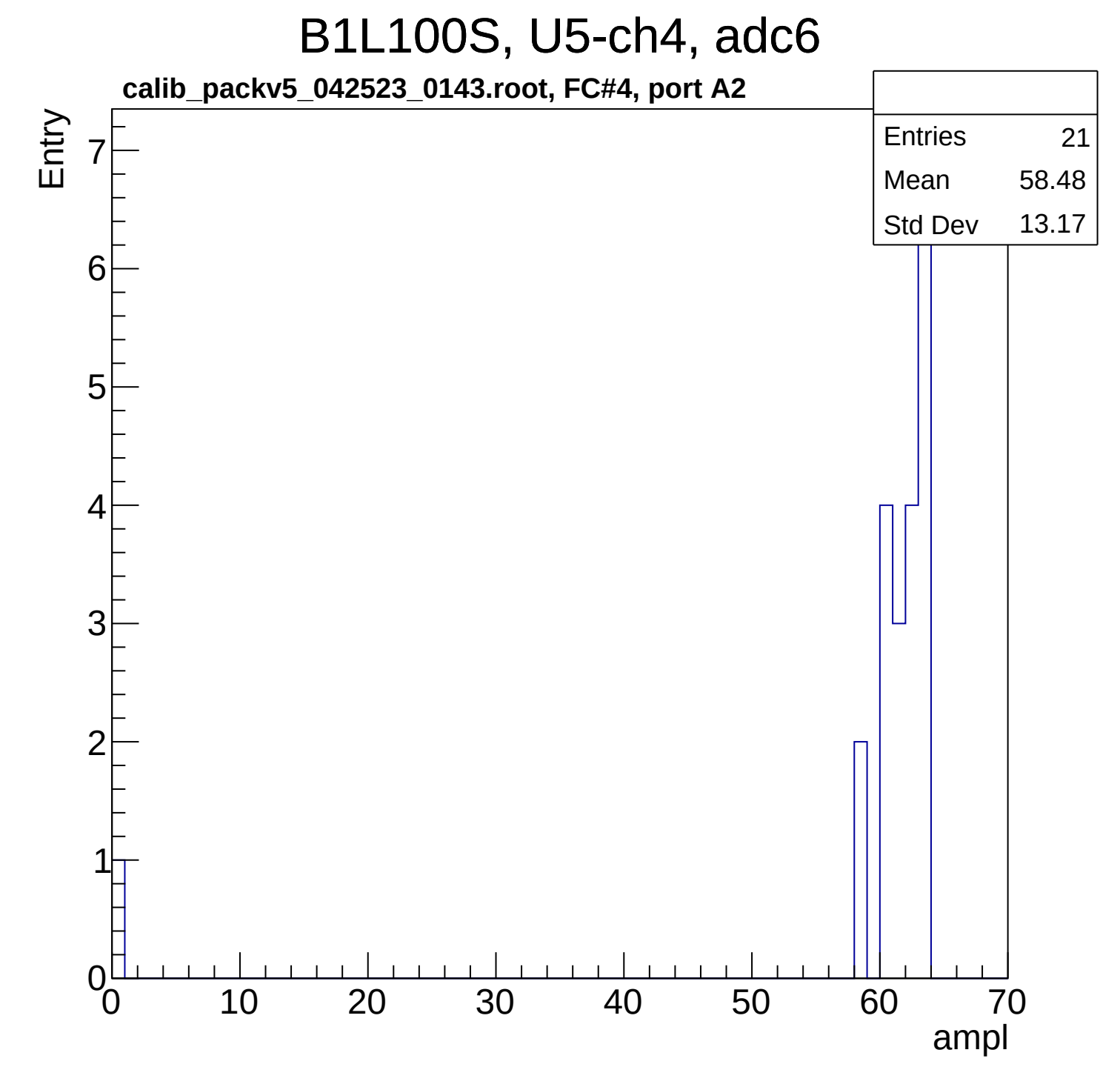

B1L100S, U5-ch4, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 34.97
Std Dev 3.266
Gaus mean : 35.0084
Gaus Width: 4.4039
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

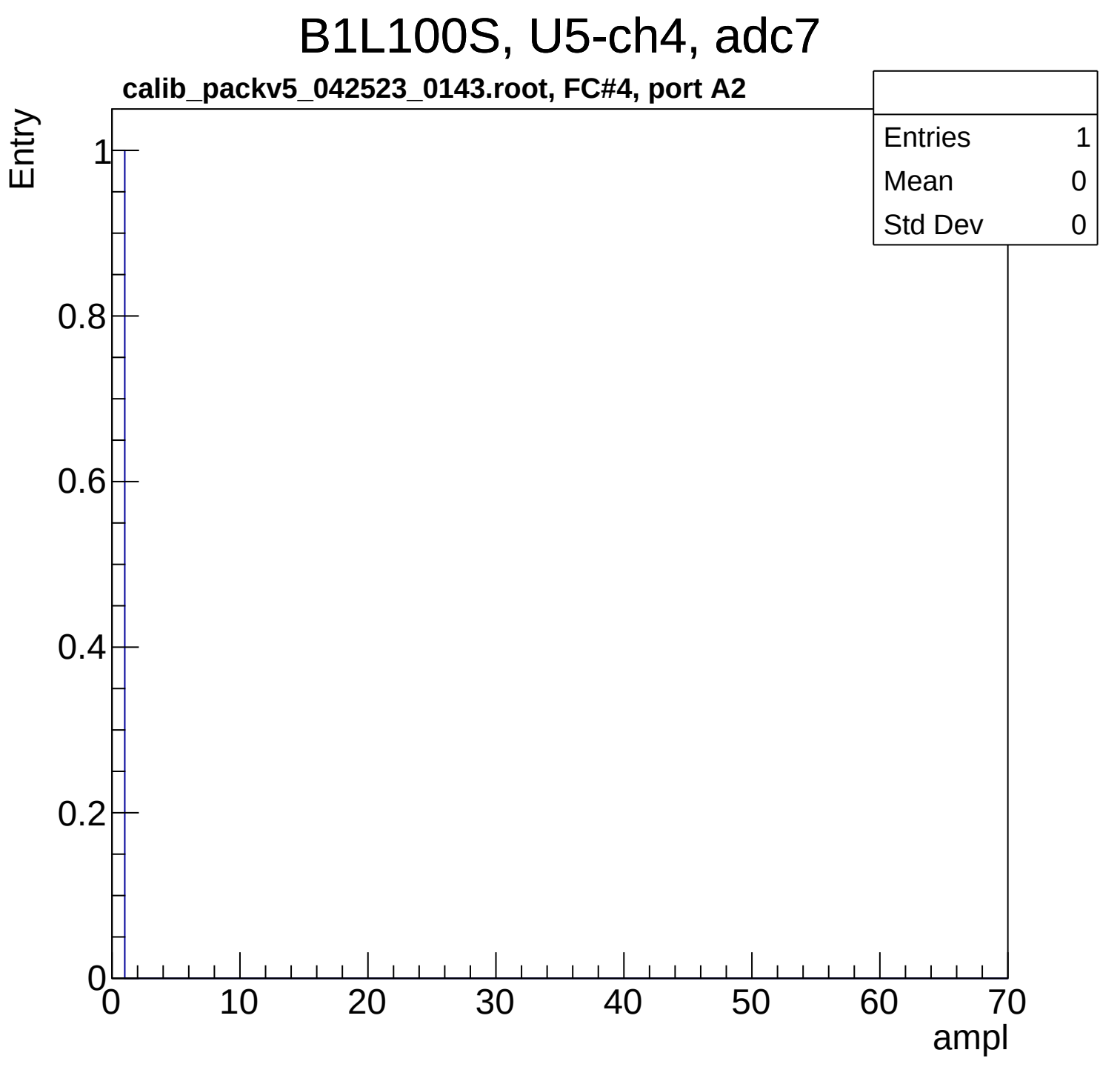

B1L100S, U5-ch4, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 41.65
Std Dev 3.738
Gaus mean : 42.4171
Gaus Width: 4.3184
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

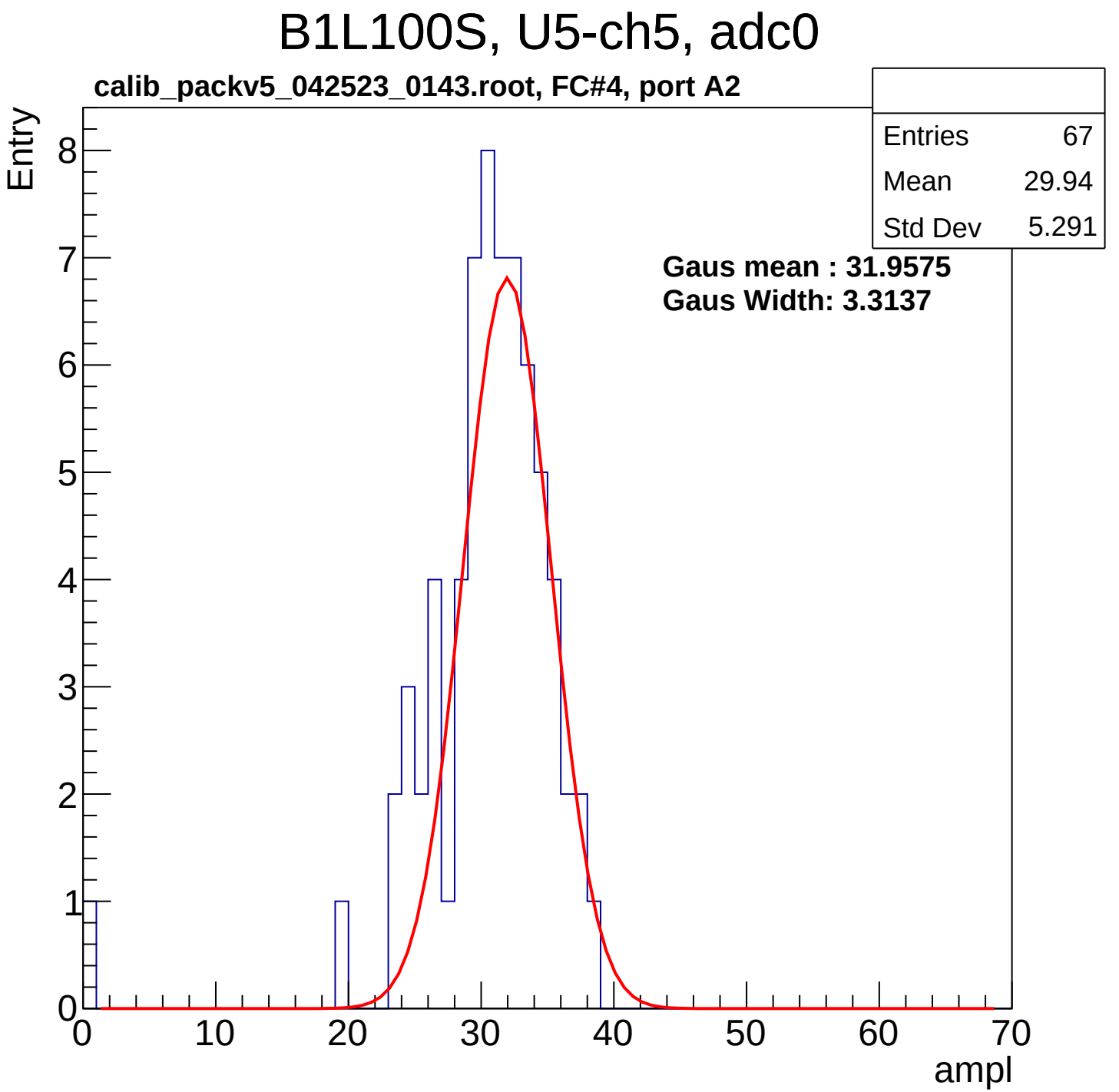

B1L100S, U5-ch4, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 47.5
Std Dev 3.735
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

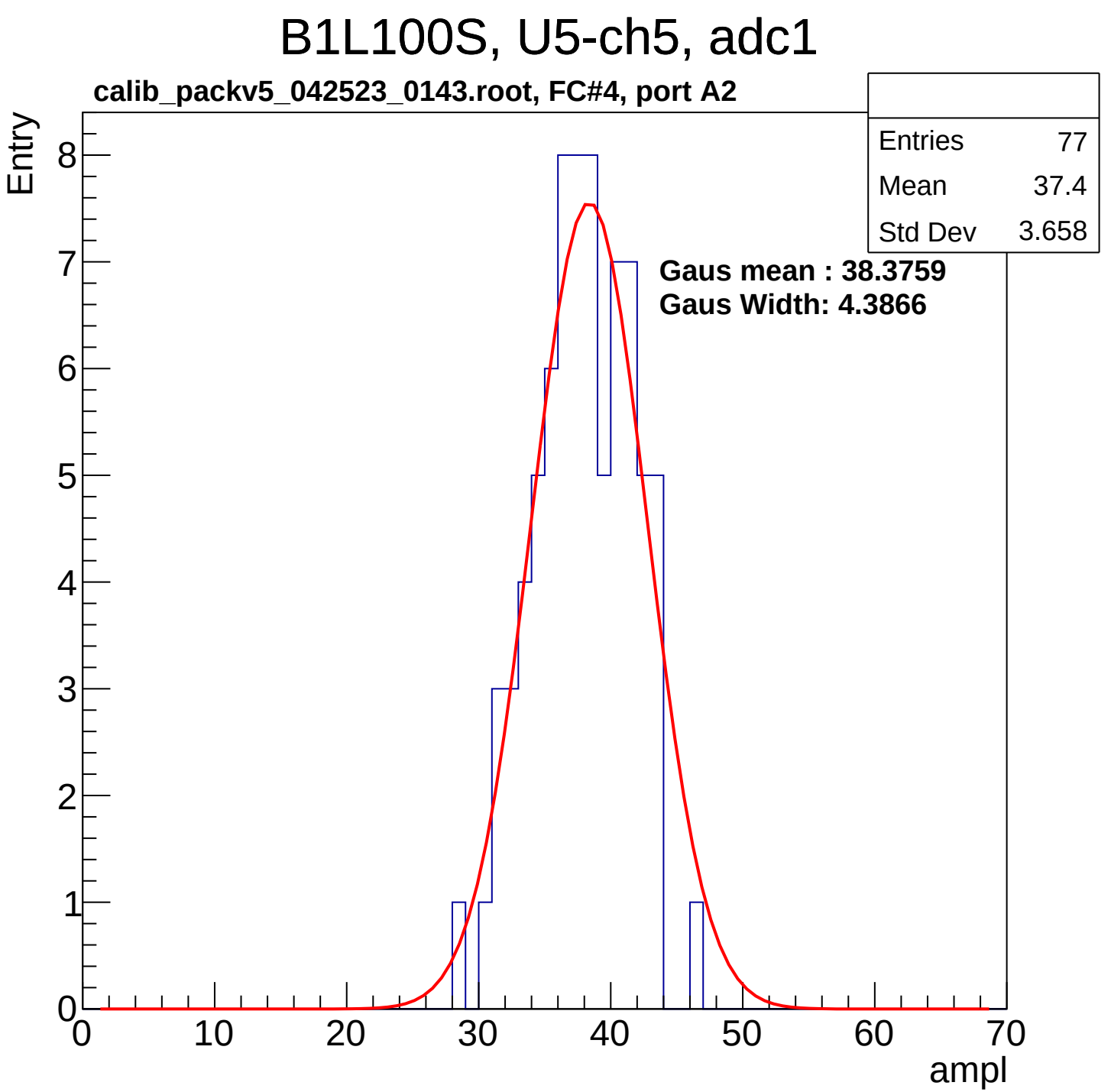

B1L100S, U5-ch4, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 52.62
Std Dev 3.117
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

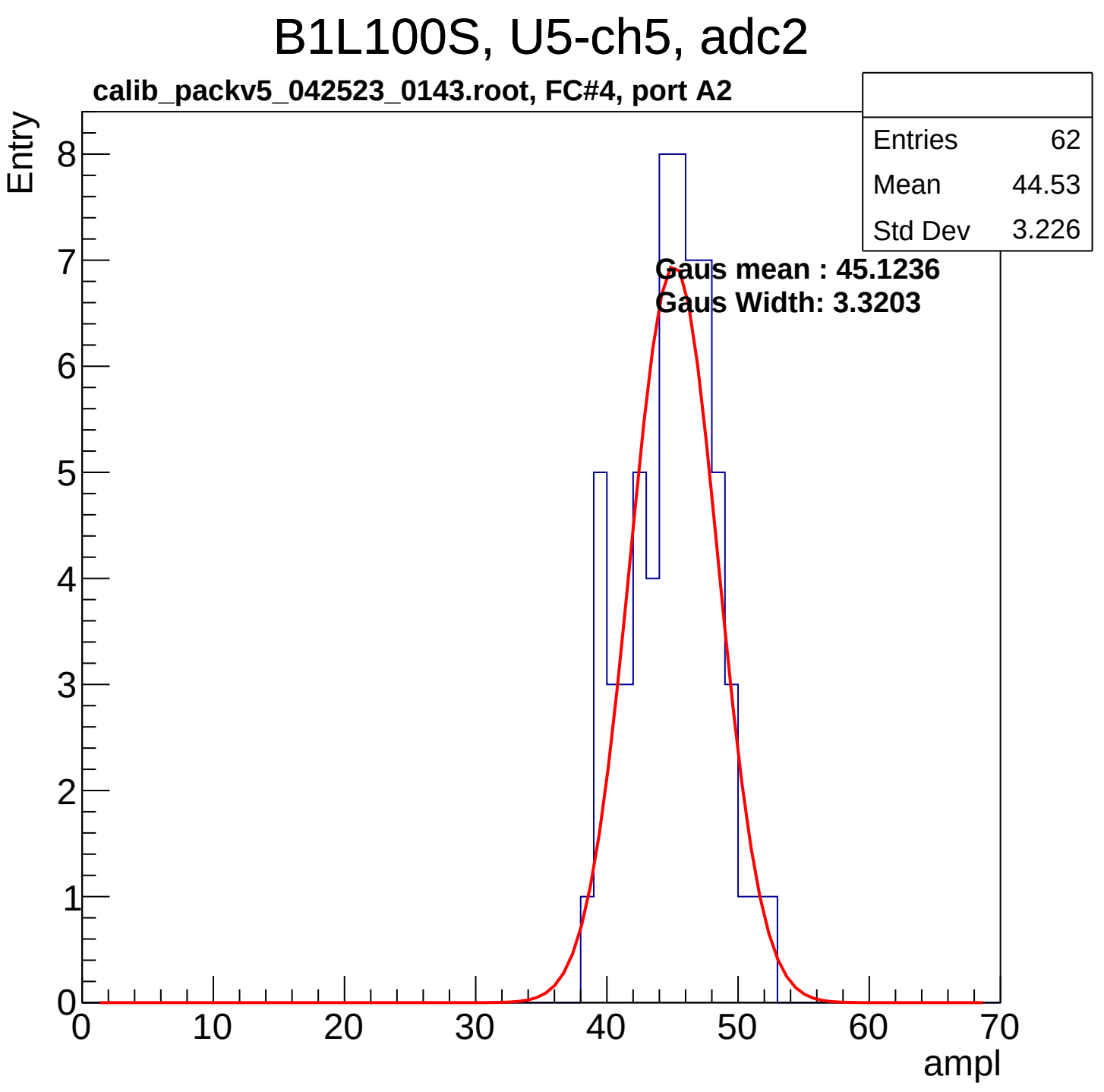

B1L100S, U5-ch4, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 58.25
Std Dev 3.015
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

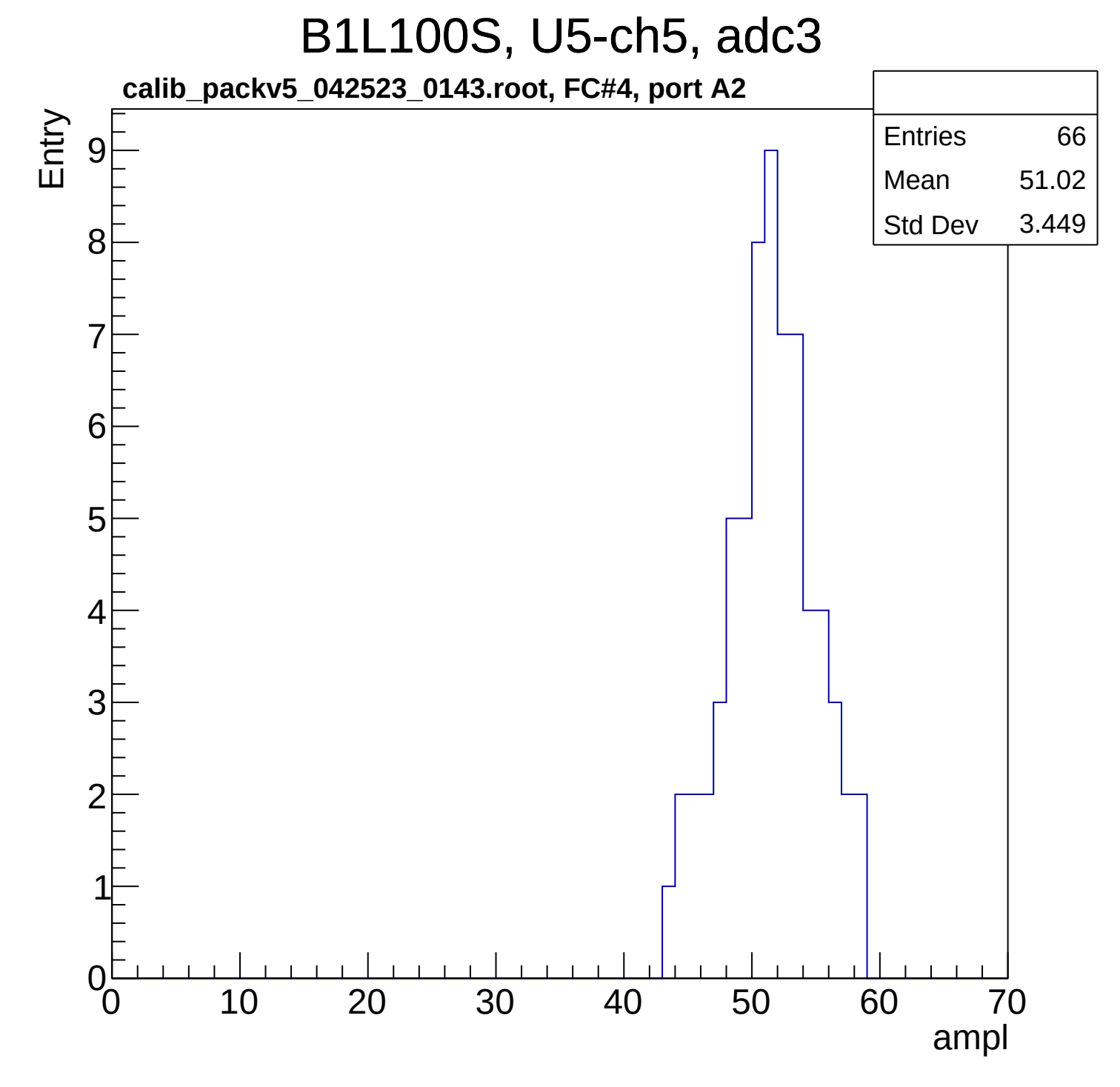

B1L100S, U5-ch4, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 21
Mean 58.48
Std Dev 13.17
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

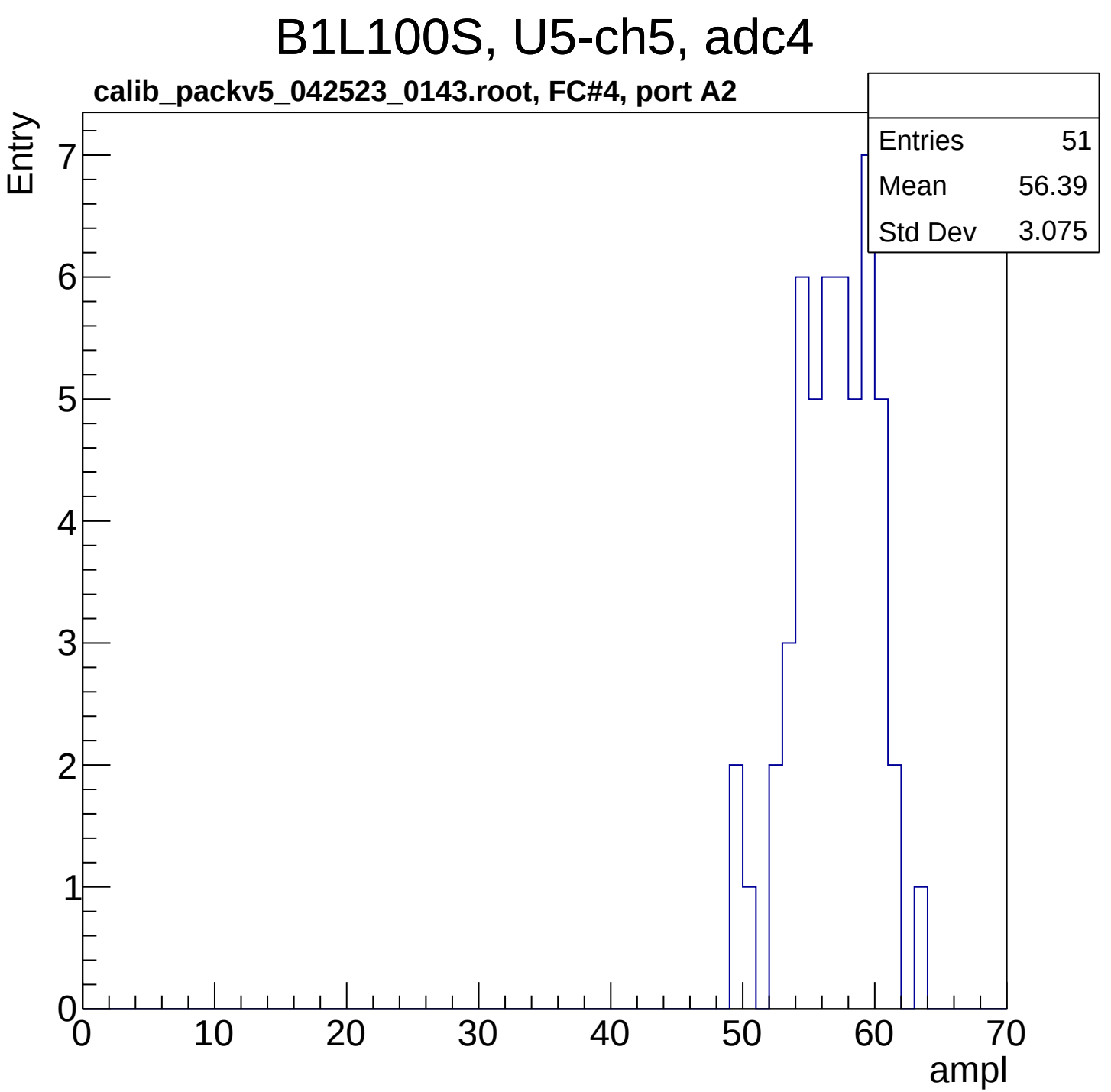

B1L100S, U5-ch4, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

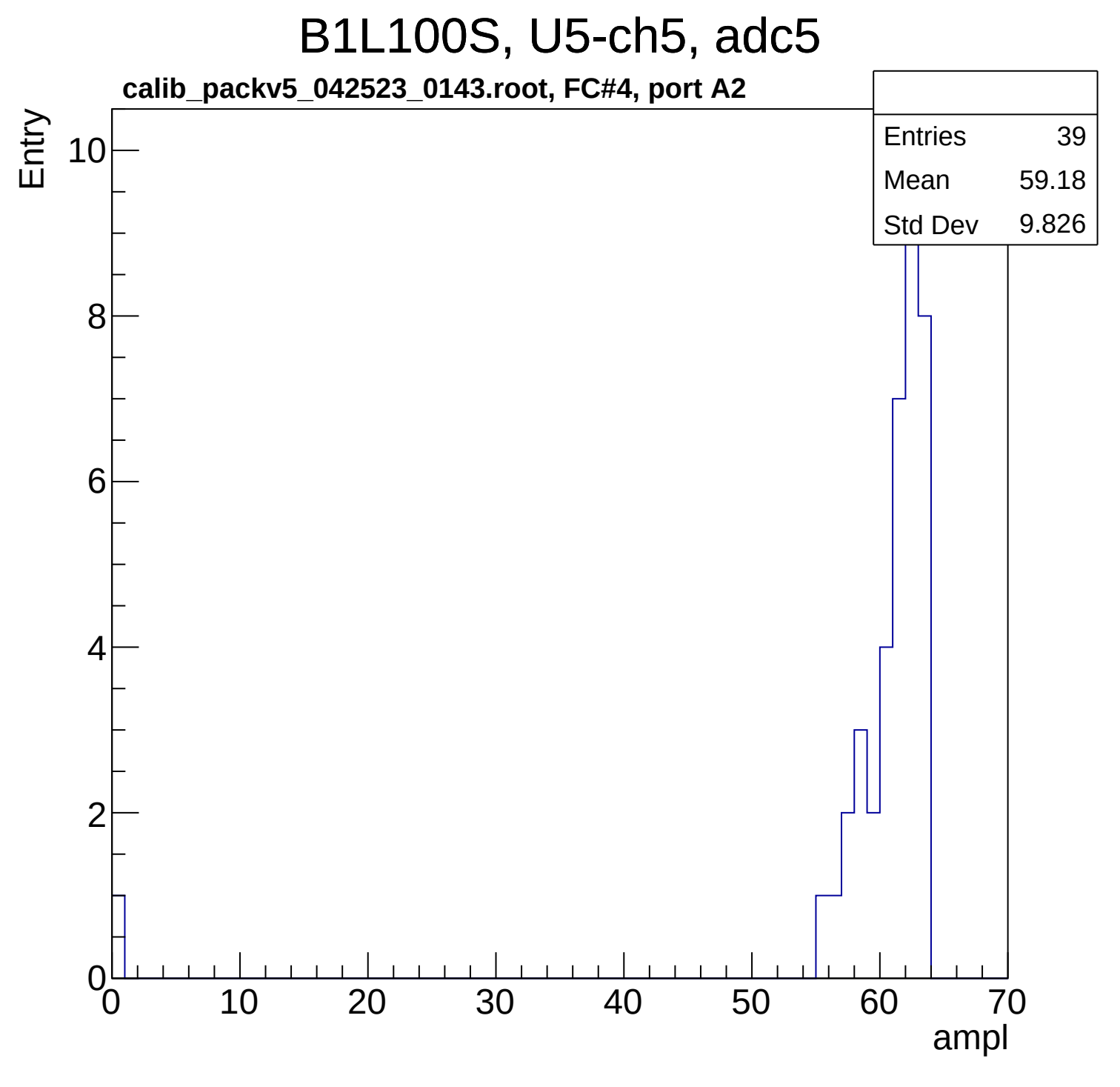

B1L100S, U5-ch5, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 29.94
Std Dev 5.291
Gaus mean : 31.9575
Gaus Width: 3.3137
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

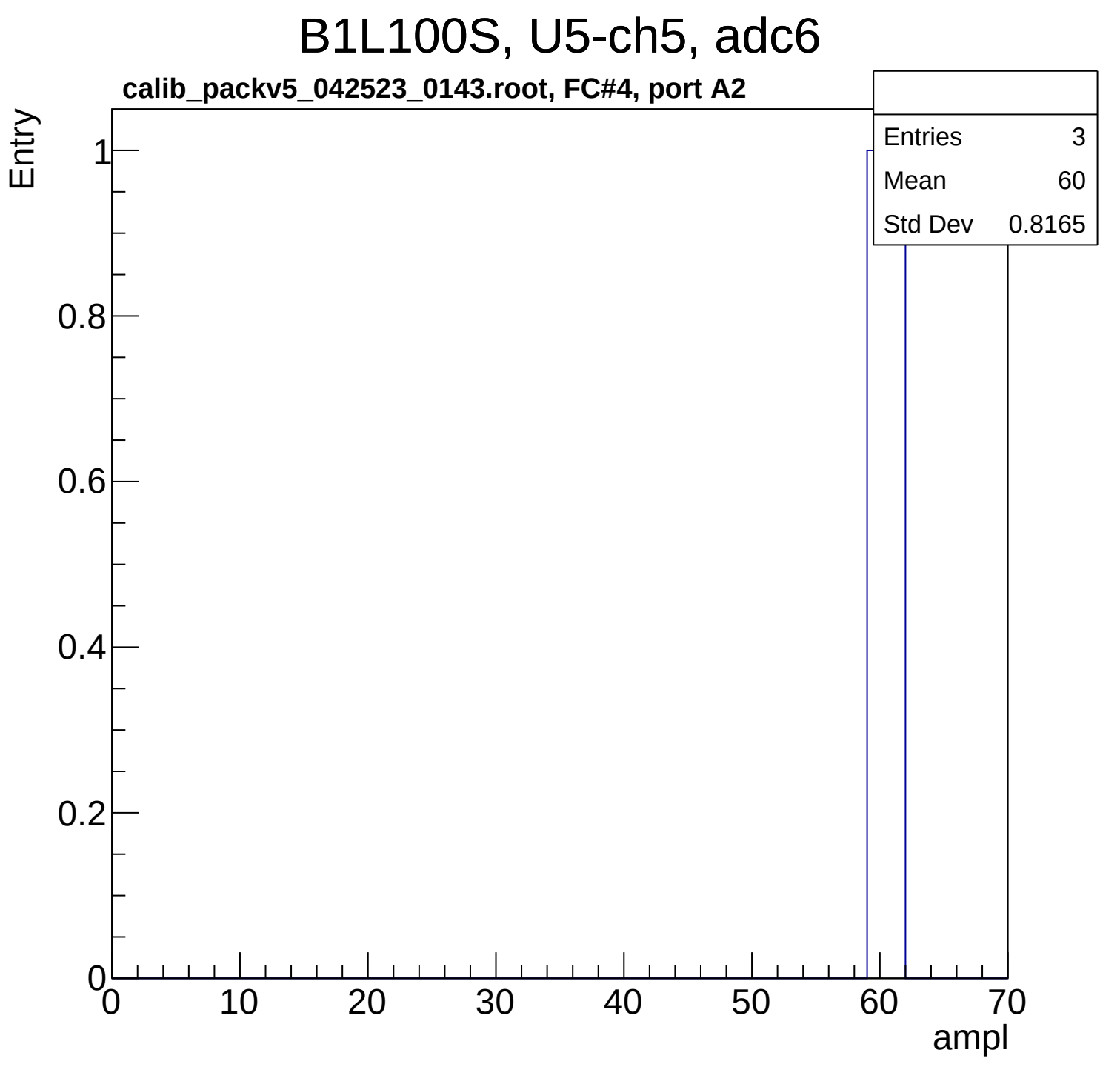

B1L100S, U5-ch5, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 77
Mean 37.4
Std Dev 3.658
Gaus mean : 38.3759
Gaus Width: 4.3866
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch5, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 44.53
Std Dev 3.226
Gaus mean : 45.1236
Gaus Width: 3.3203
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch5, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 51.02
Std Dev 3.449
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch5, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 56.39
Std Dev 3.075
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U5-ch5, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 39
Mean 59.18
Std Dev 9.826
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch5, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 60
Std Dev 0.8165
Entry
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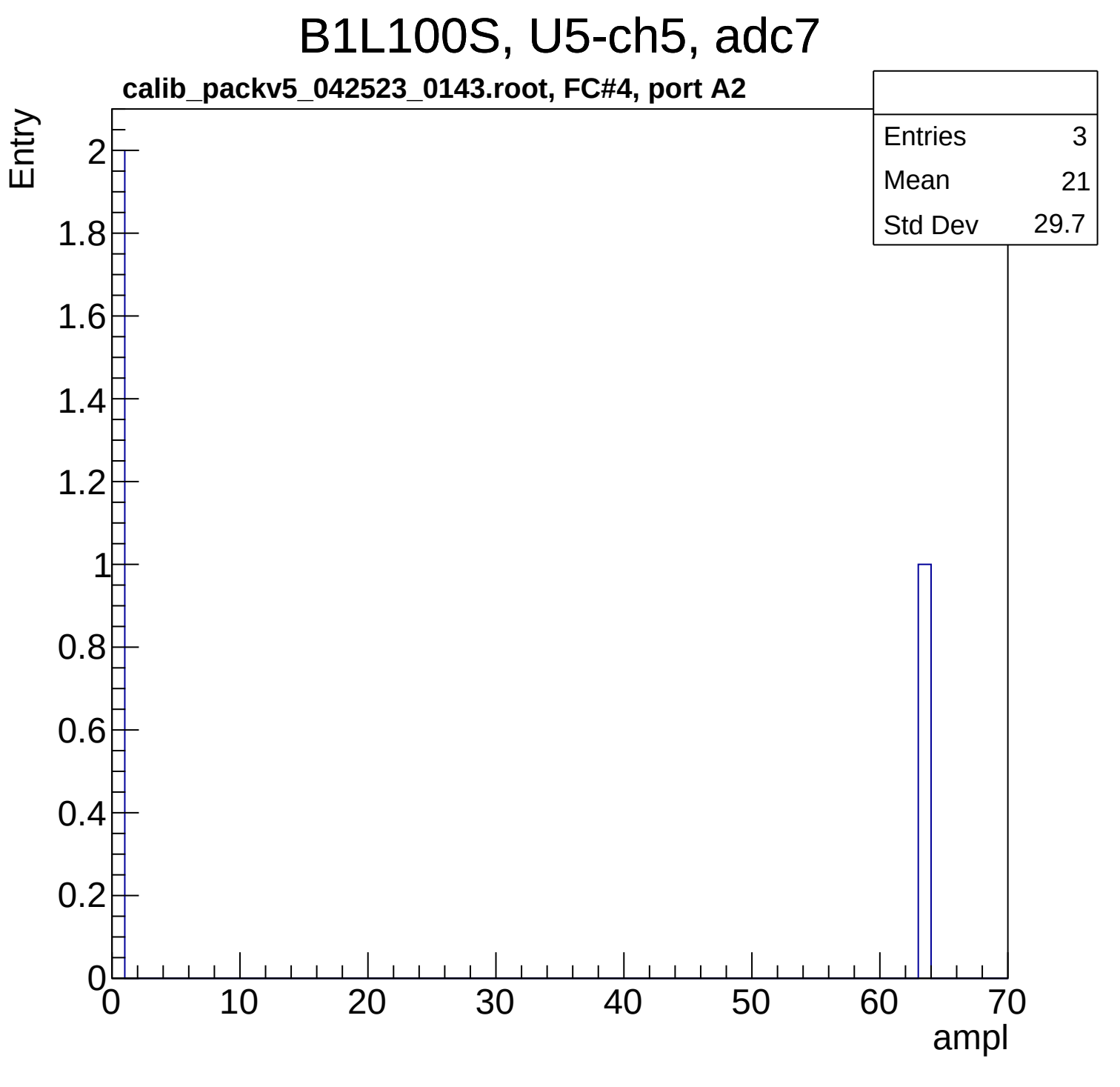
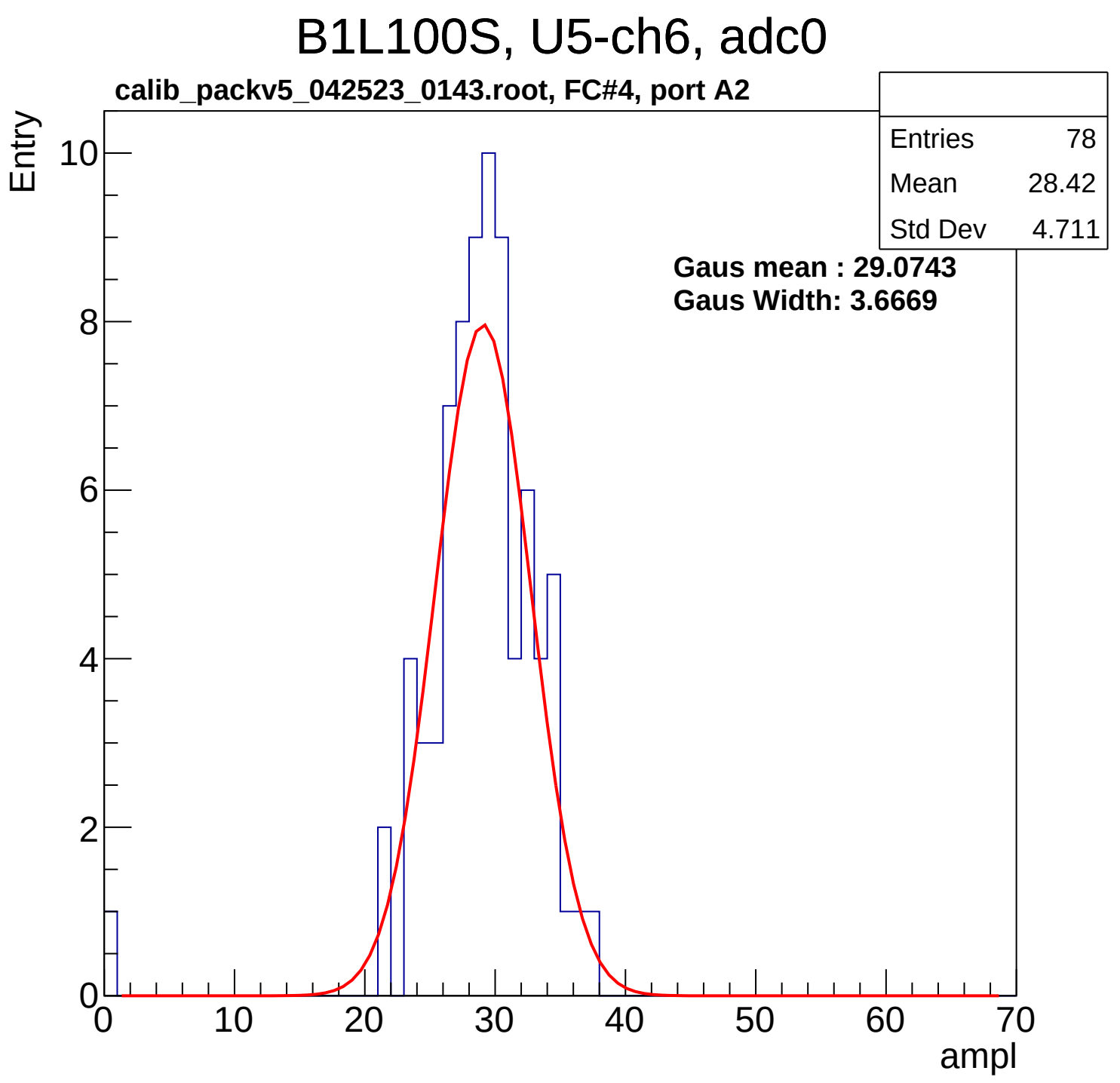
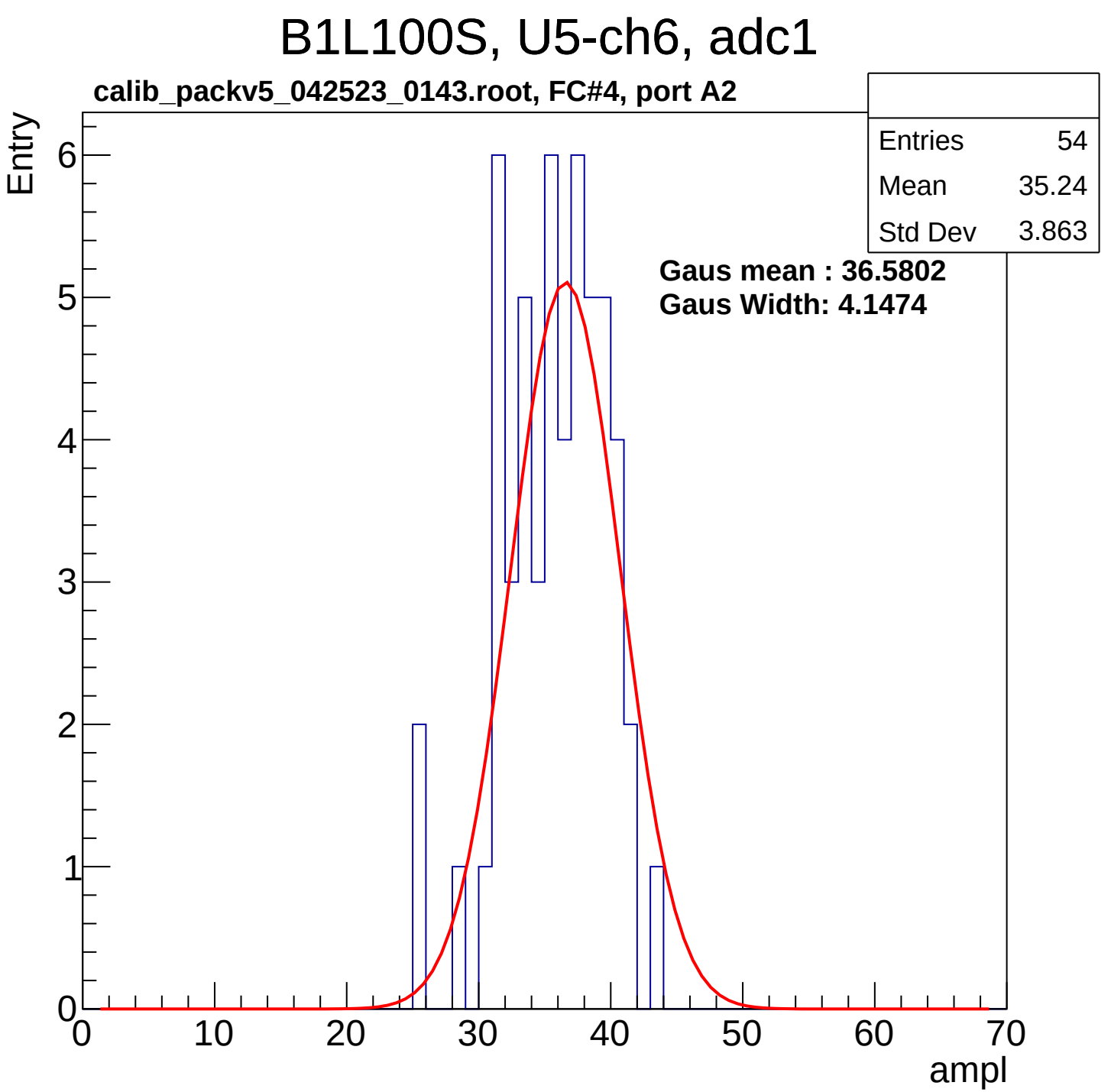
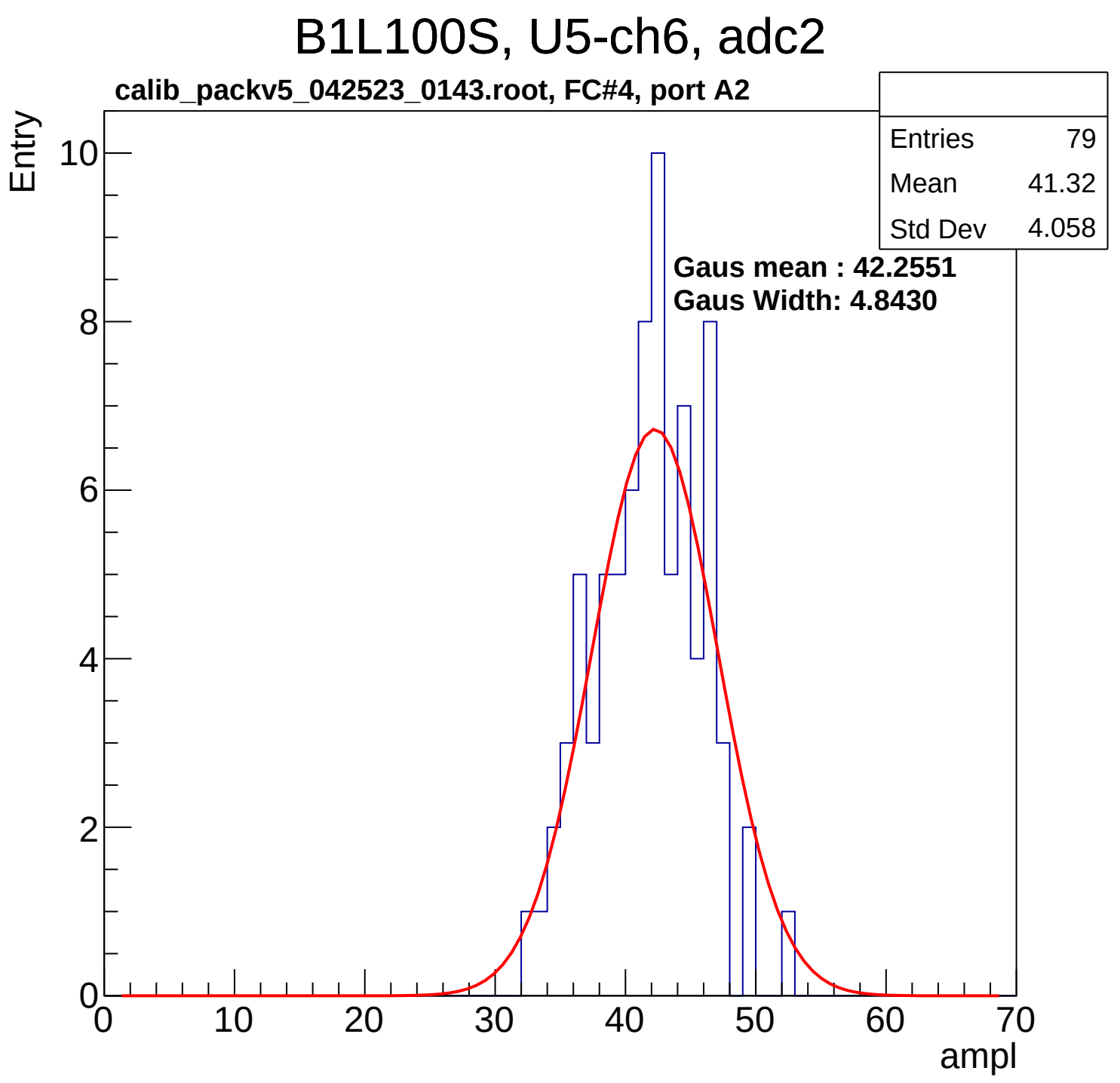
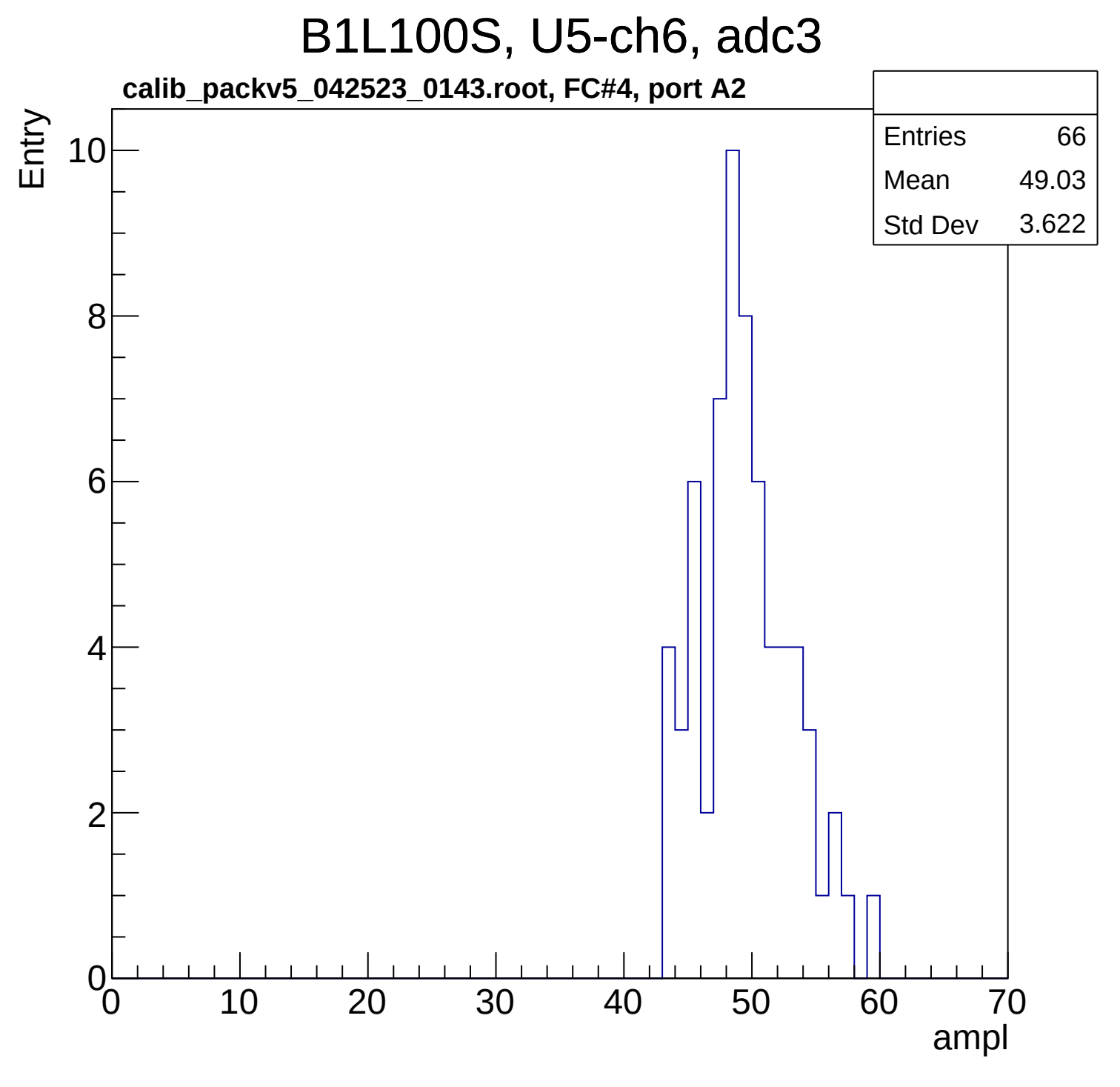
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch5, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 21
Std Dev 29.7
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L100S, U5-ch6, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 78
Mean 28.42
Std Dev 4.711
Gaus mean : 29.0743
Gaus Width: 3.6669
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch6, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 35.24
Std Dev 3.863
Gaus mean : 36.5802
Gaus Width: 4.1474
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L100S, U5-ch6, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 79
Mean 41.32
Std Dev 4.058
Gaus mean : 42.2551
Gaus Width: 4.8430
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch6, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 49.03
Std Dev 3.622
Entry
ampl
0
2
4
6
8
10
0
10
20
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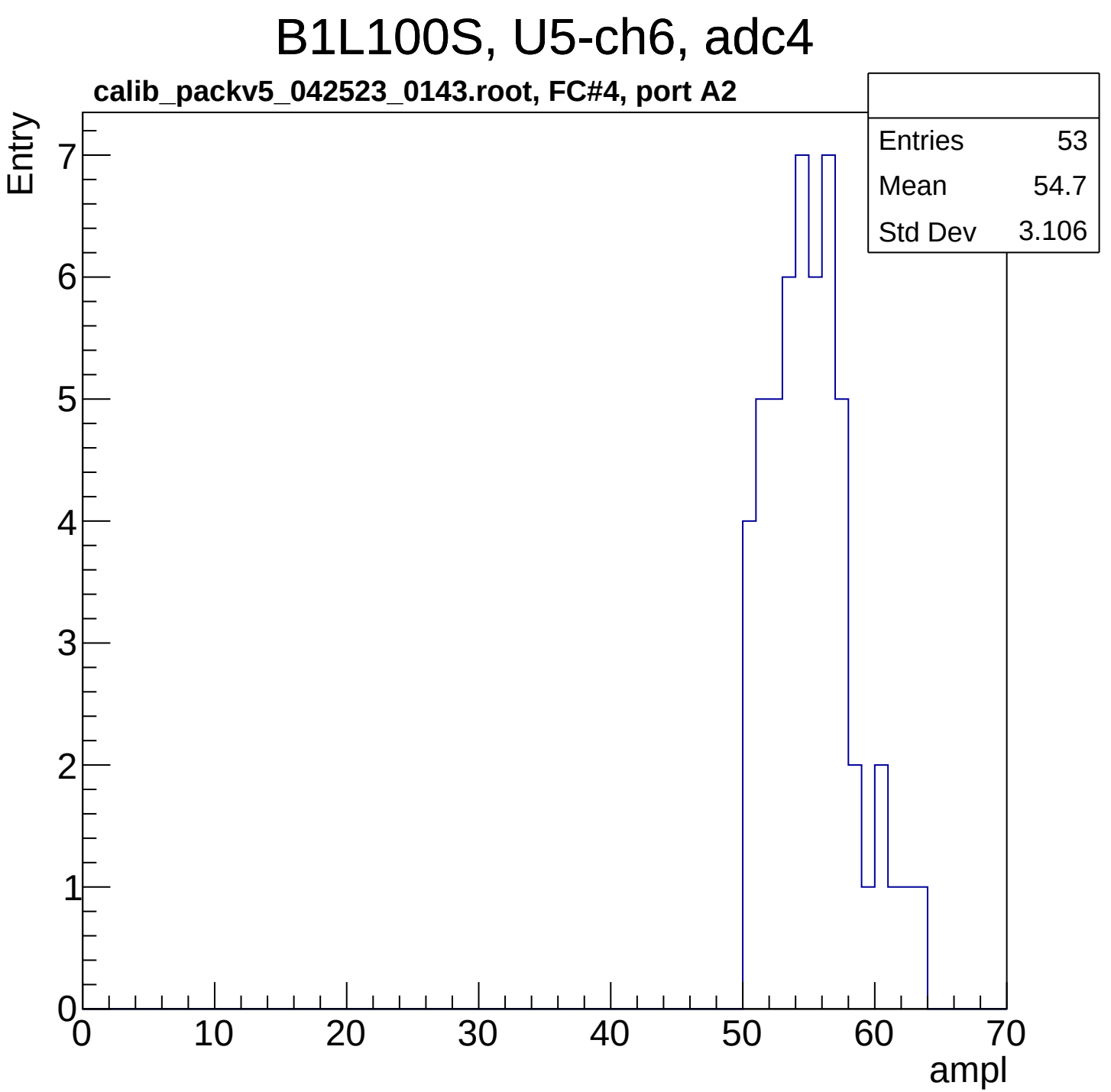
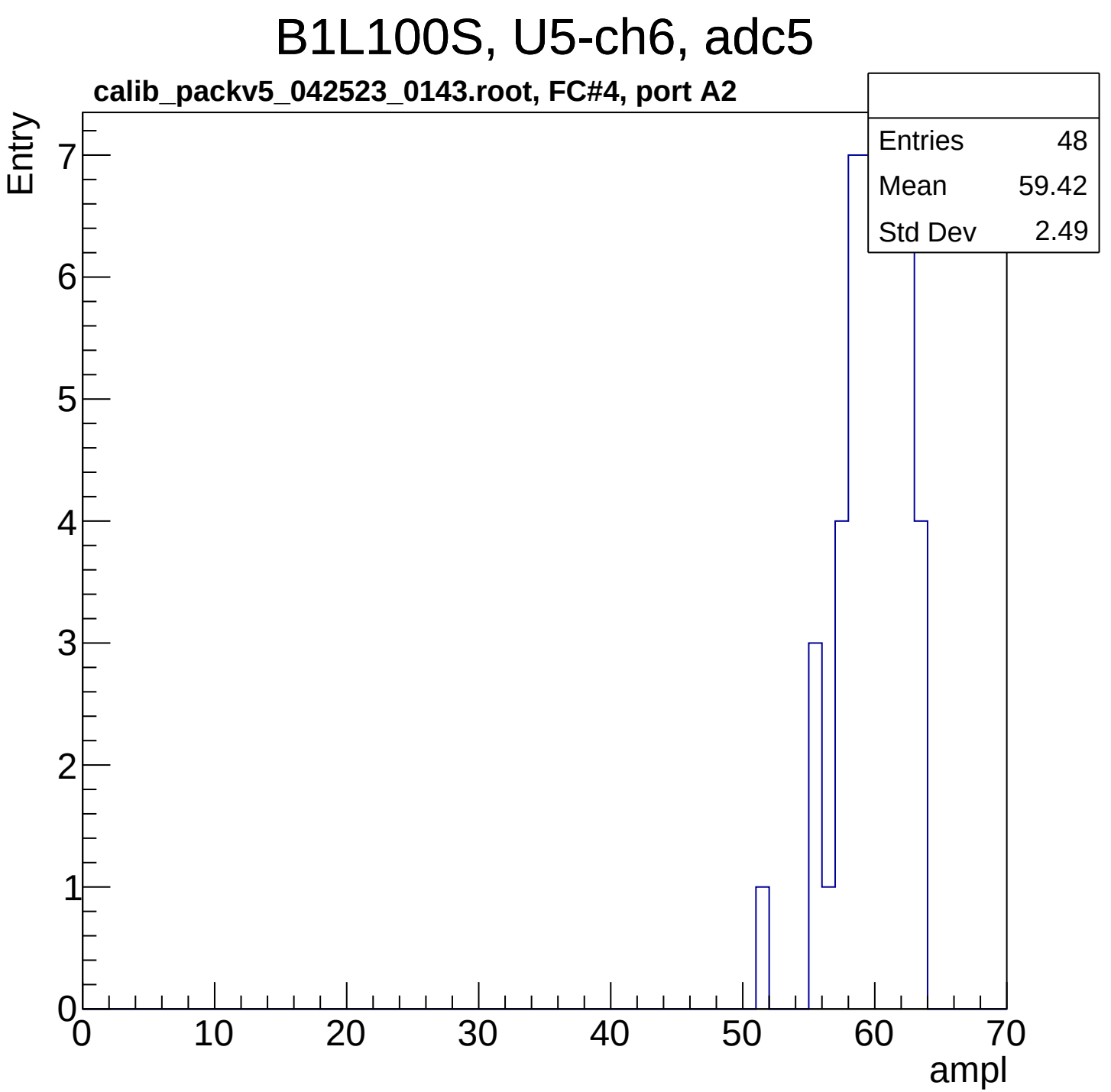
40
50
60
70


B1L100S, U5-ch6, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 54.7
Std Dev 3.106
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U5-ch6, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 48
Mean 59.42
Std Dev 2.49
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
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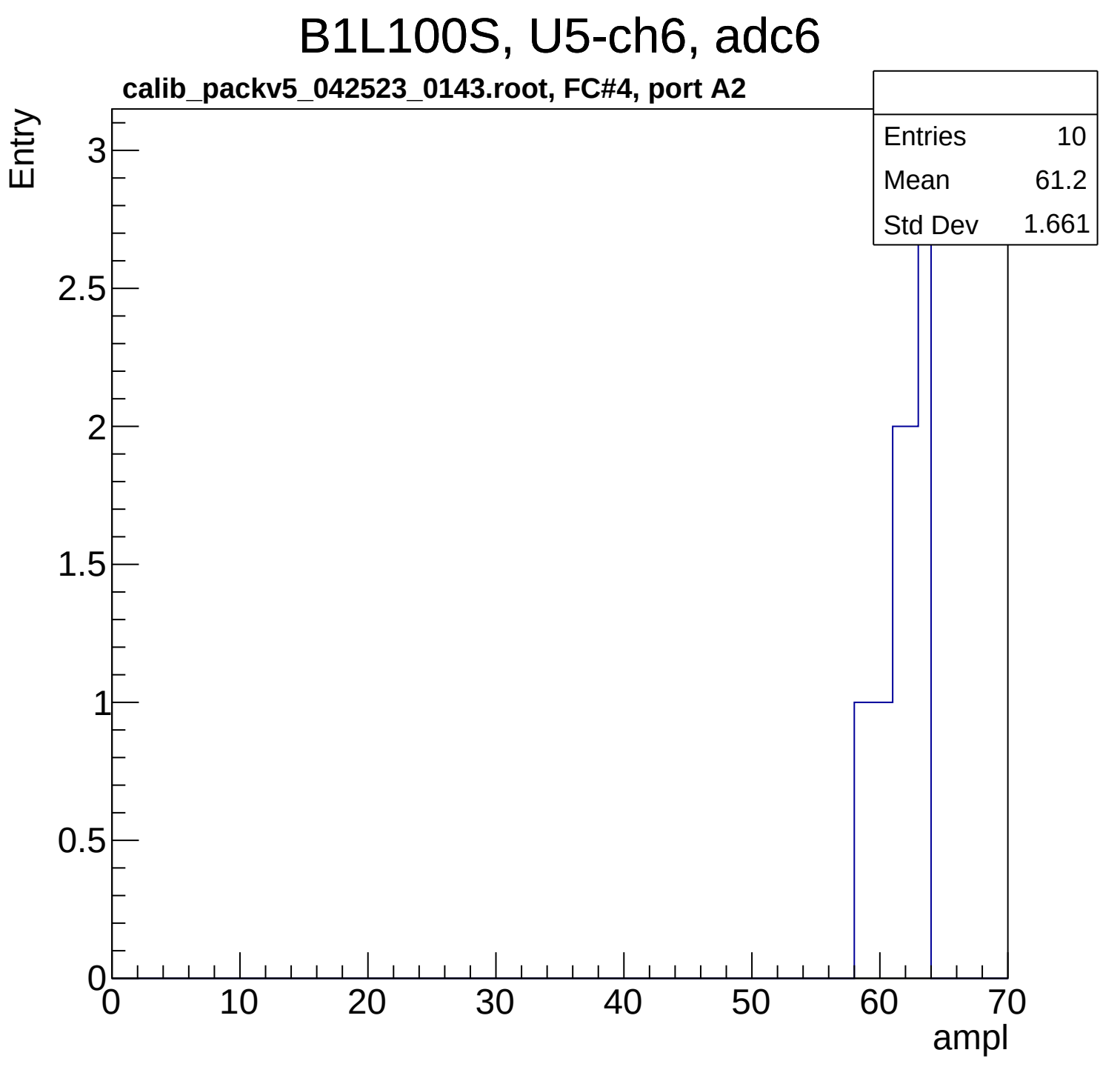
40
50
60
70


B1L100S, U5-ch6, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 10
Mean 61.2
Std Dev 1.661
Entry
ampl
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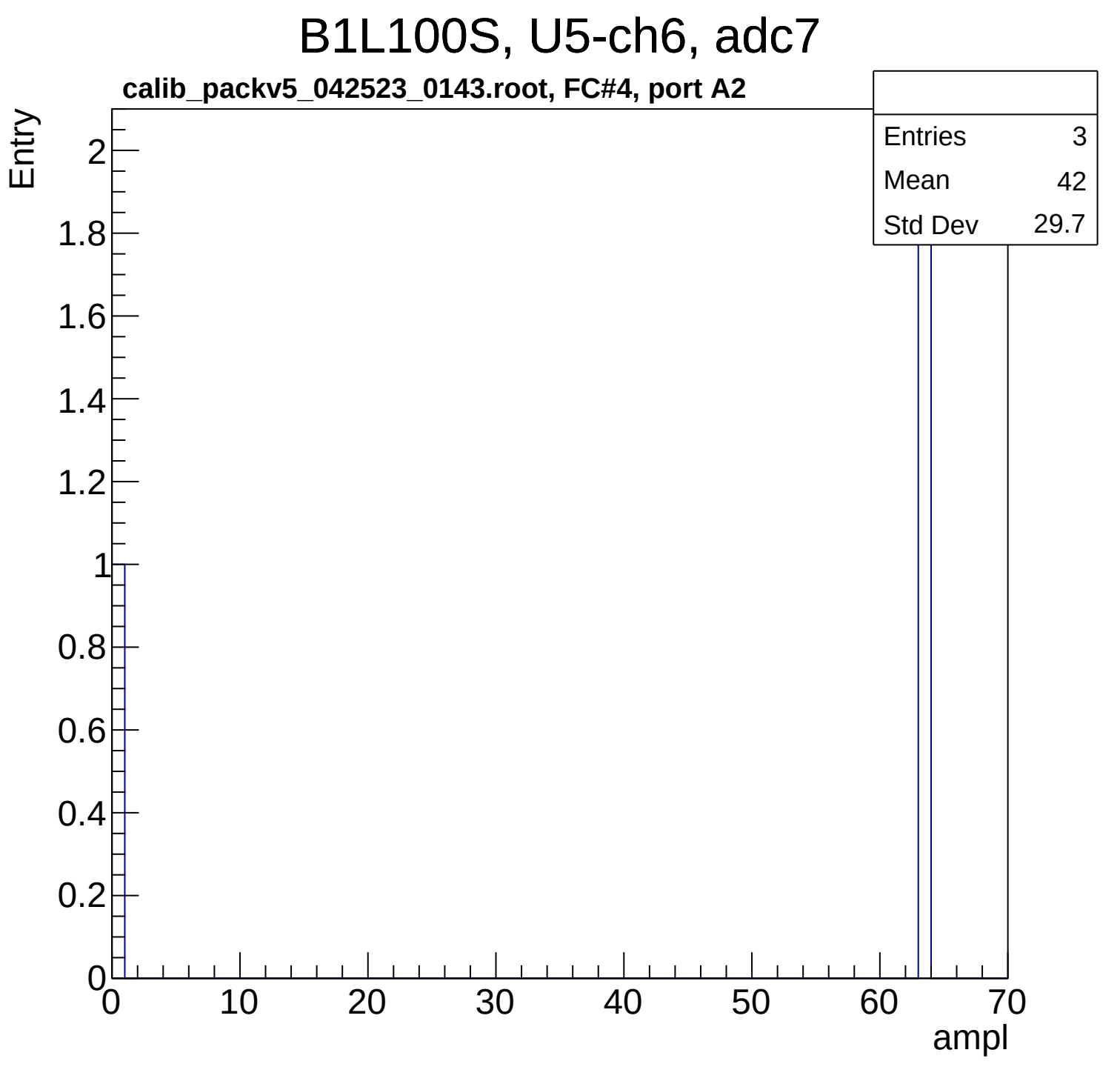
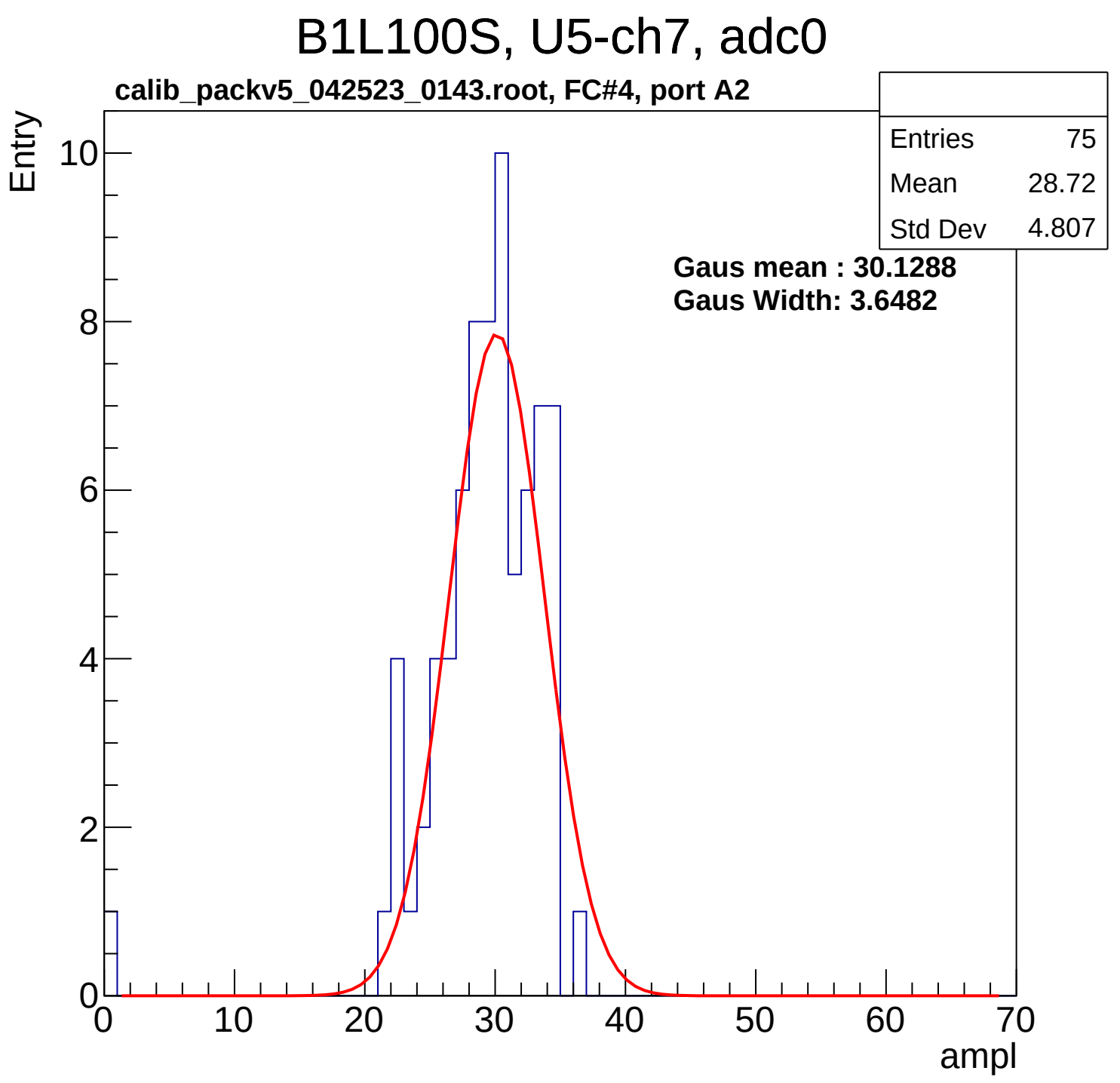
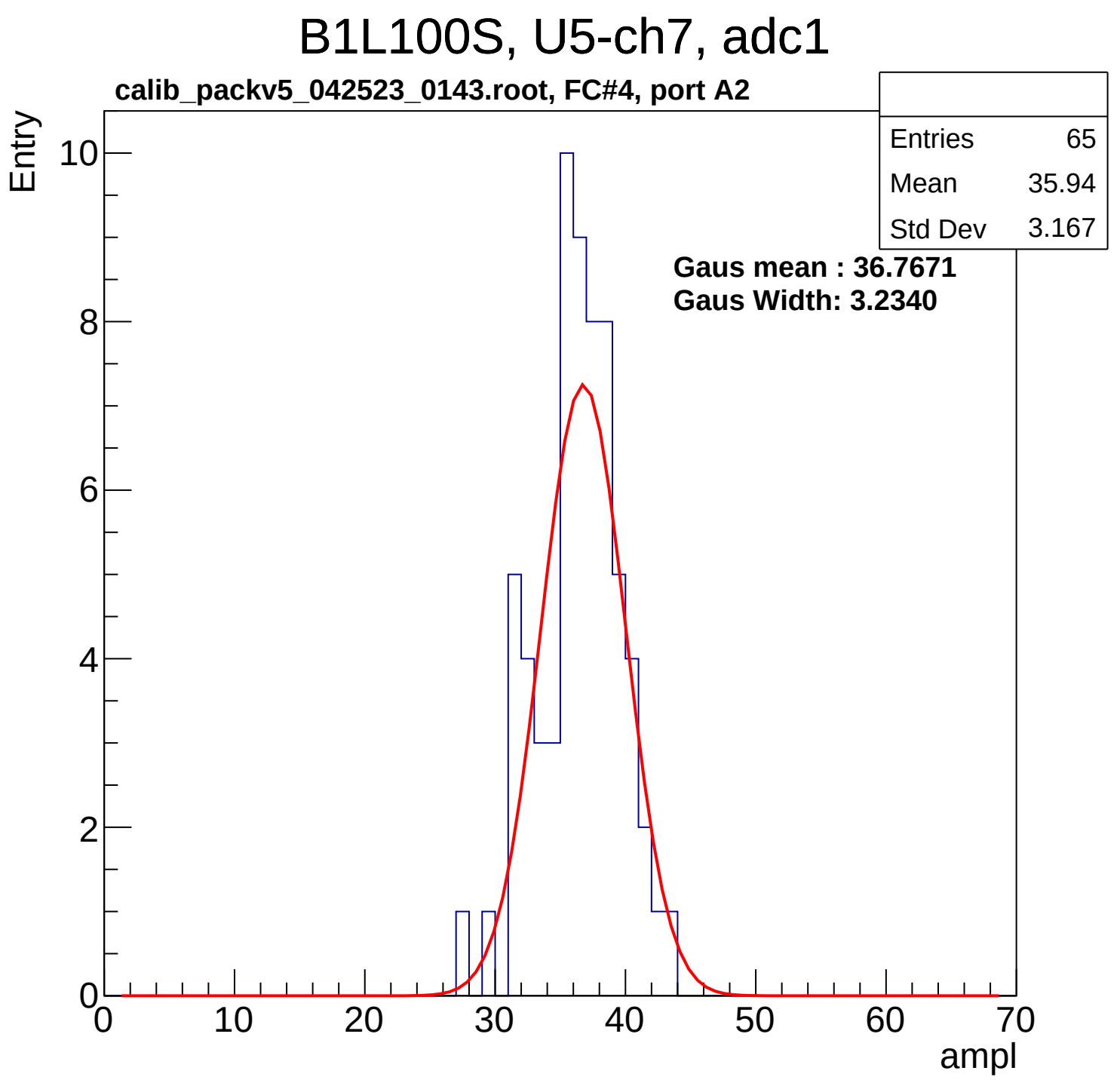
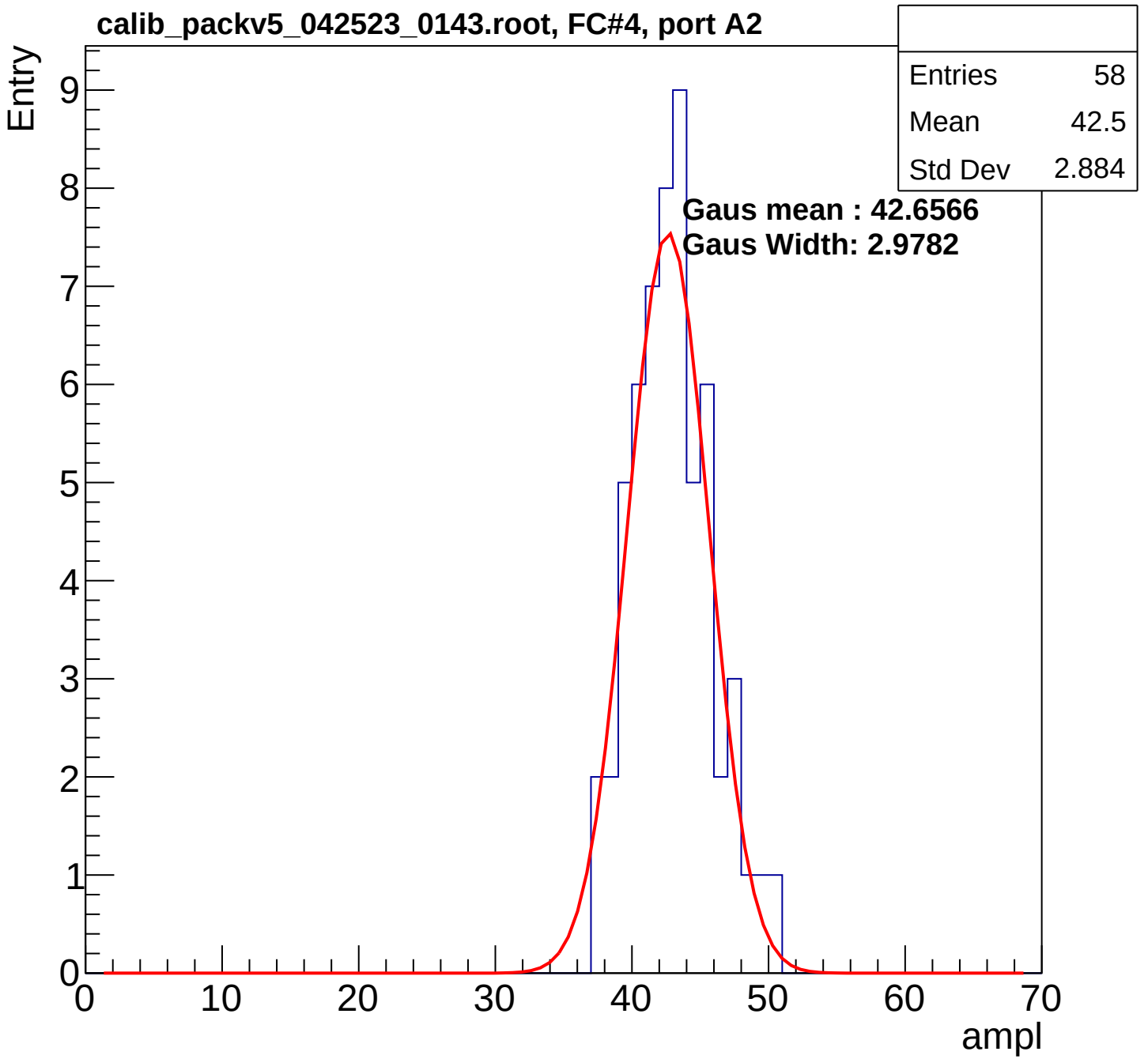
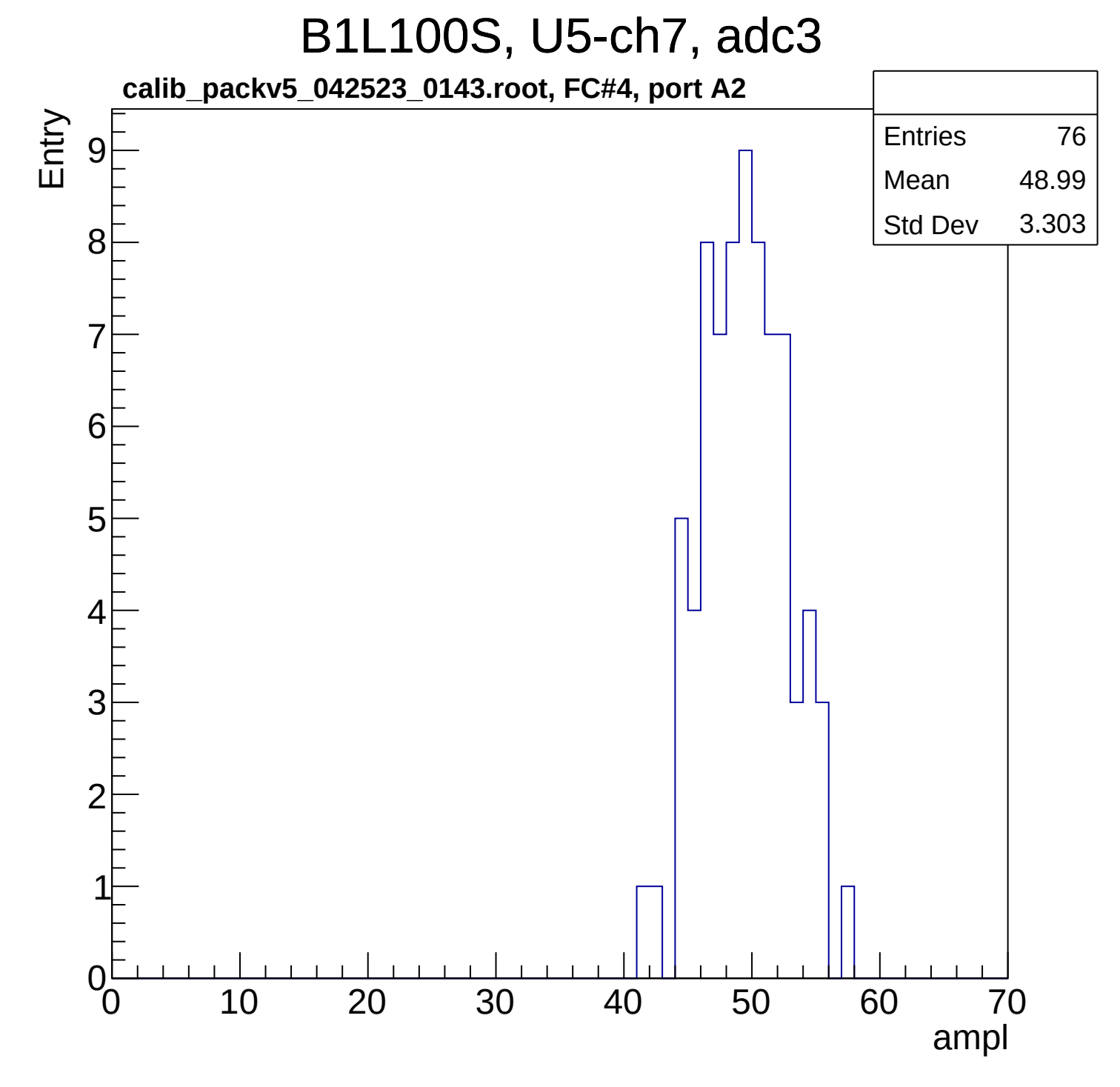
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L100S, U5-ch6, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 42
Std Dev 29.7
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L100S, U5-ch7, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 75
Mean 28.72
Std Dev 4.807
Gaus mean : 30.1288
Gaus Width: 3.6482
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch7, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 35.94
Std Dev 3.167
Gaus mean : 36.7671
Gaus Width: 3.2340
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch7, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 42.5
Std Dev 2.884
Gaus mean : 42.6566
Gaus Width: 2.9782
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch7, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 76
Mean 48.99
Std Dev 3.303
Entry
ampl
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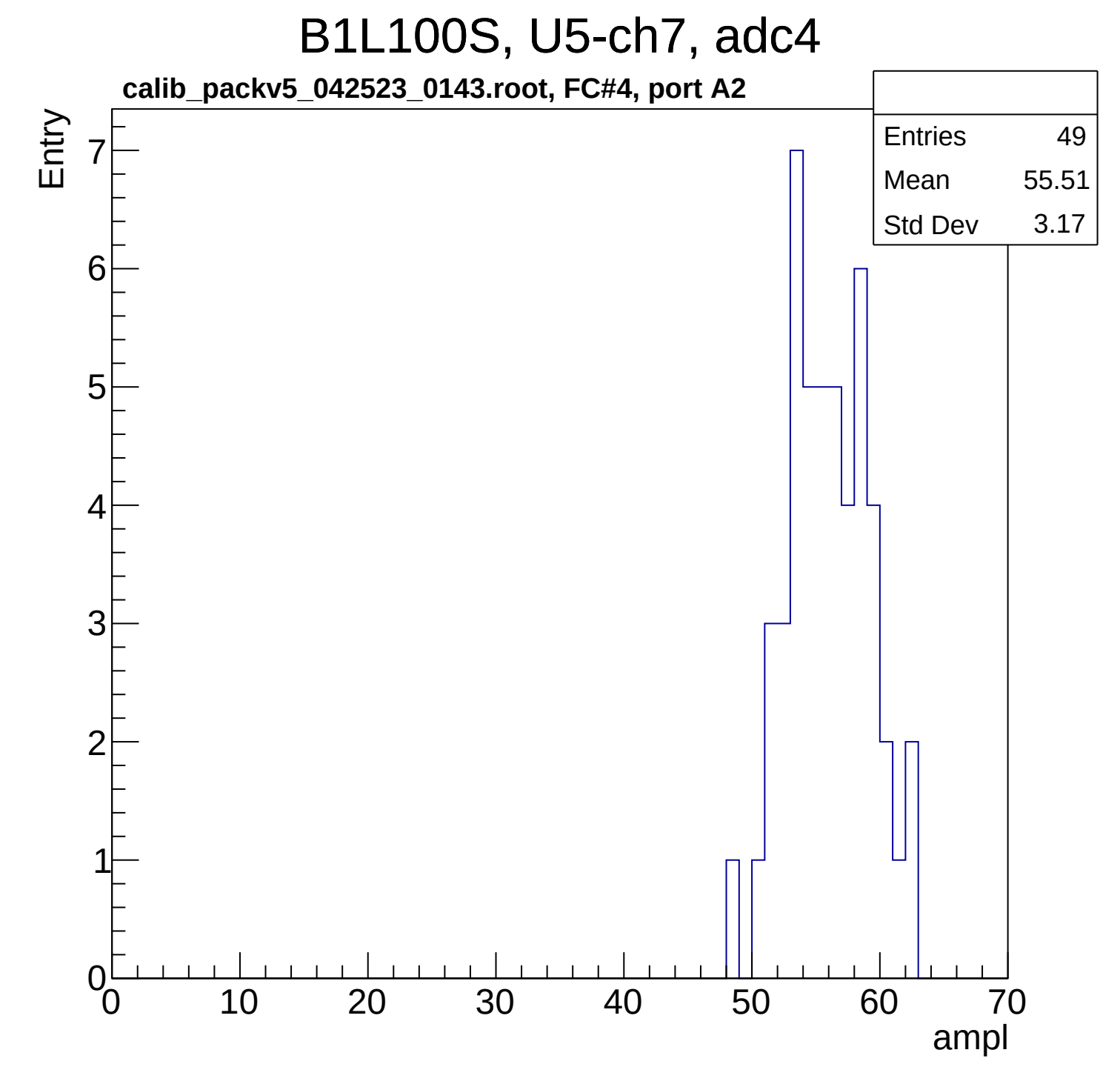
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch7, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 49
Mean 55.51
Std Dev 3.17
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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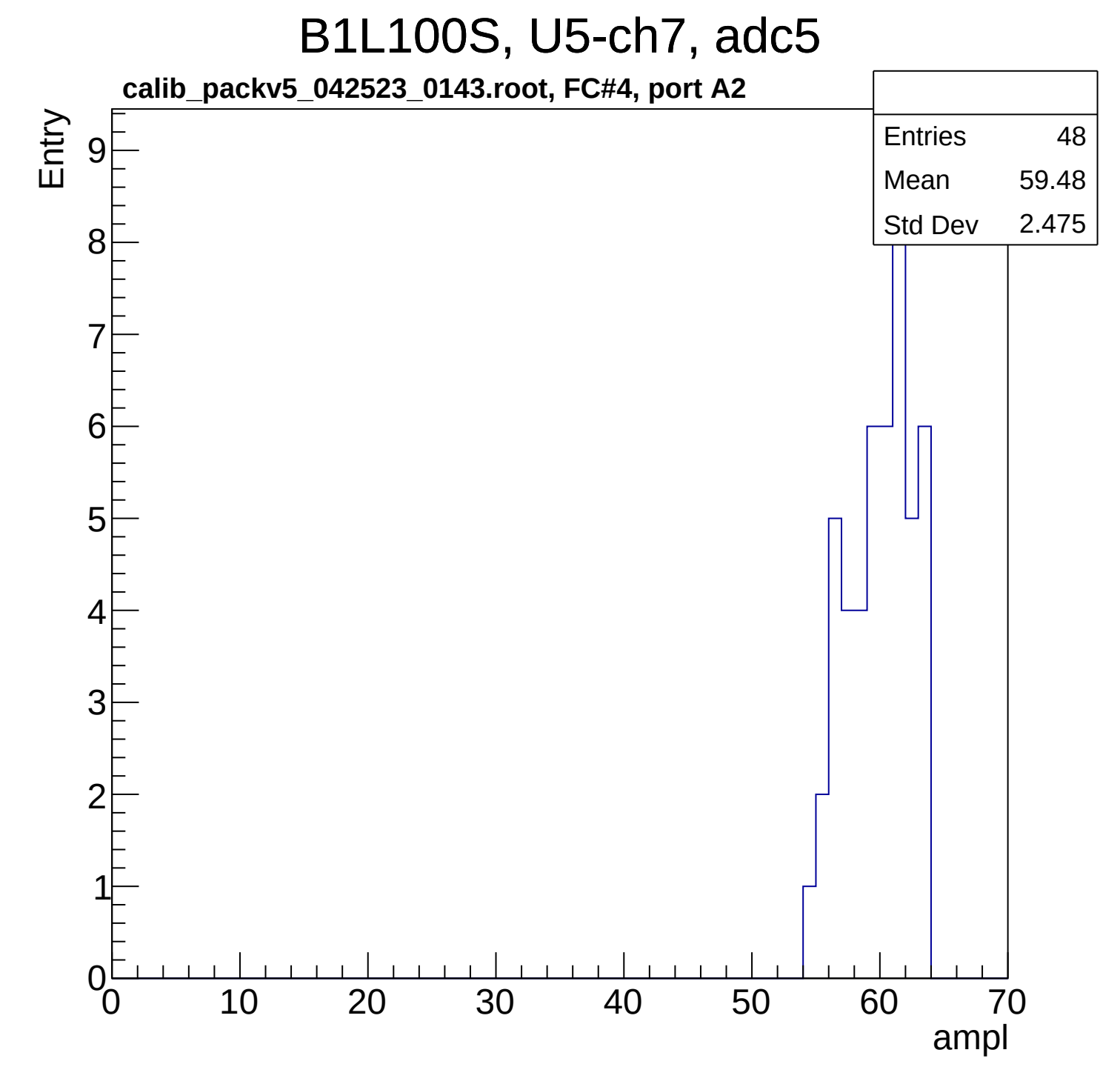
B1L100S, U5-ch7, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 48
Mean 59.48
Std Dev 2.475
Entry
ampl
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1
2
3
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6
7
8
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0
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40
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60
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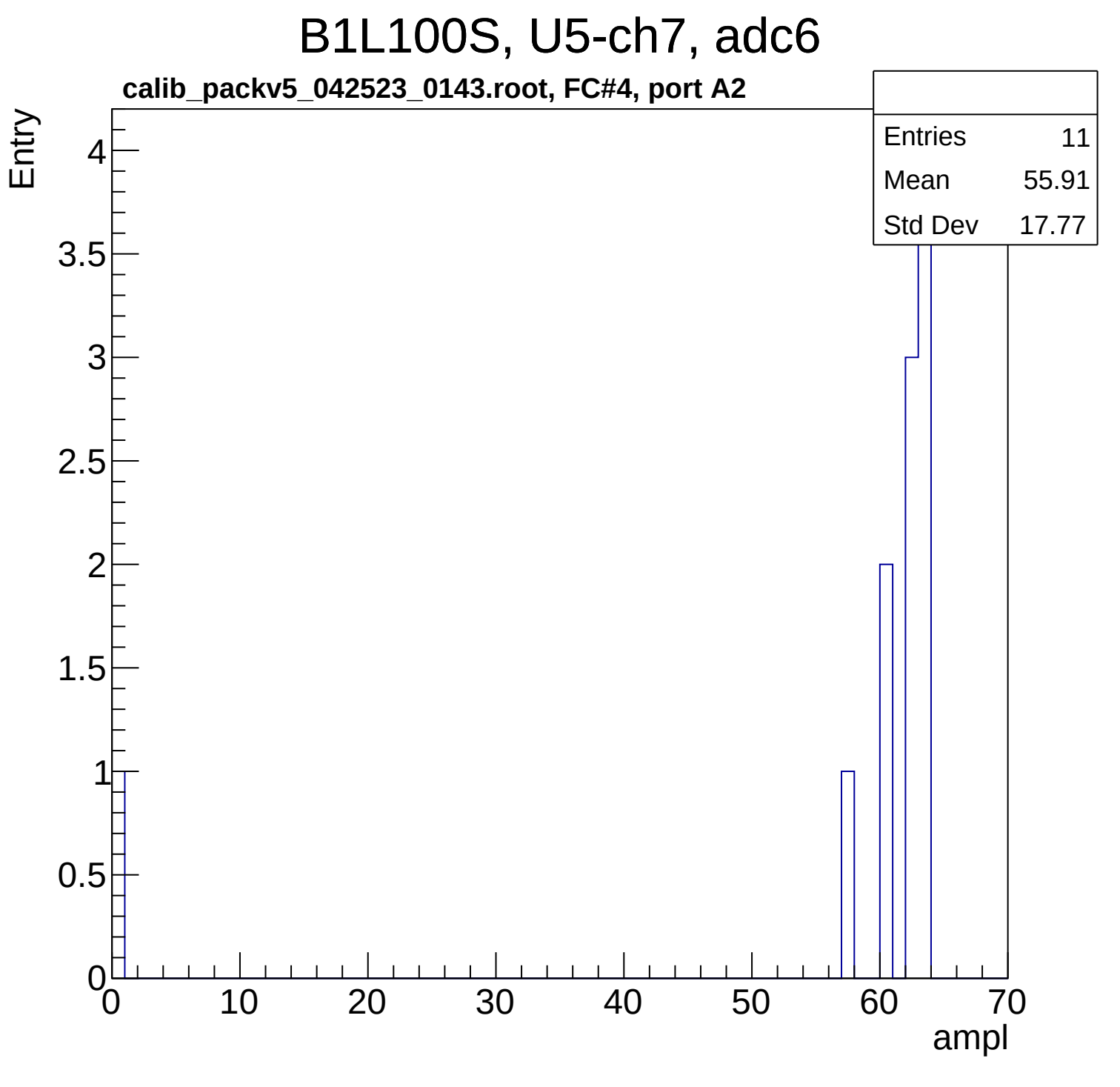
B1L100S, U5-ch7, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 11
Mean 55.91
Std Dev 17.77
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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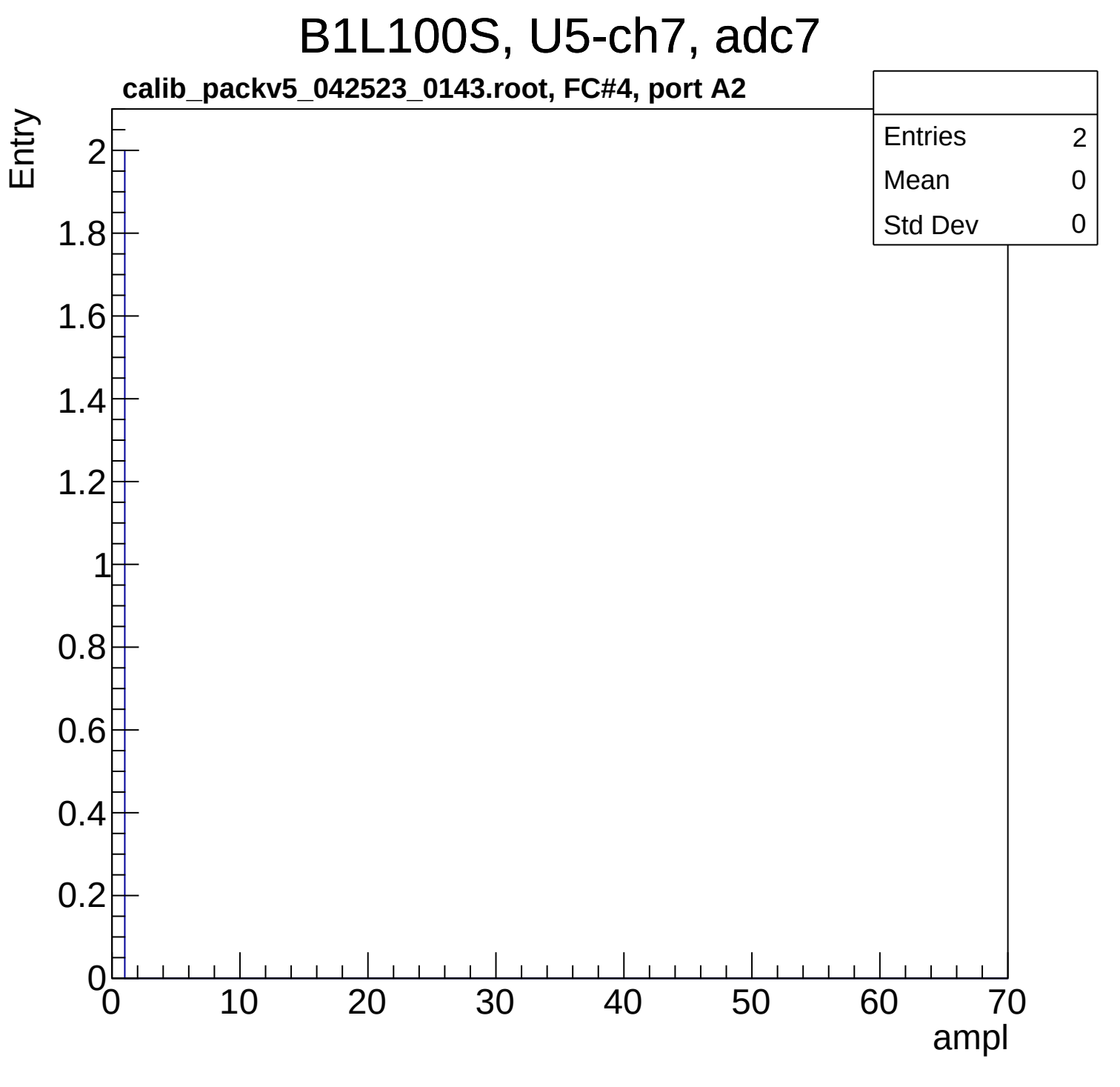
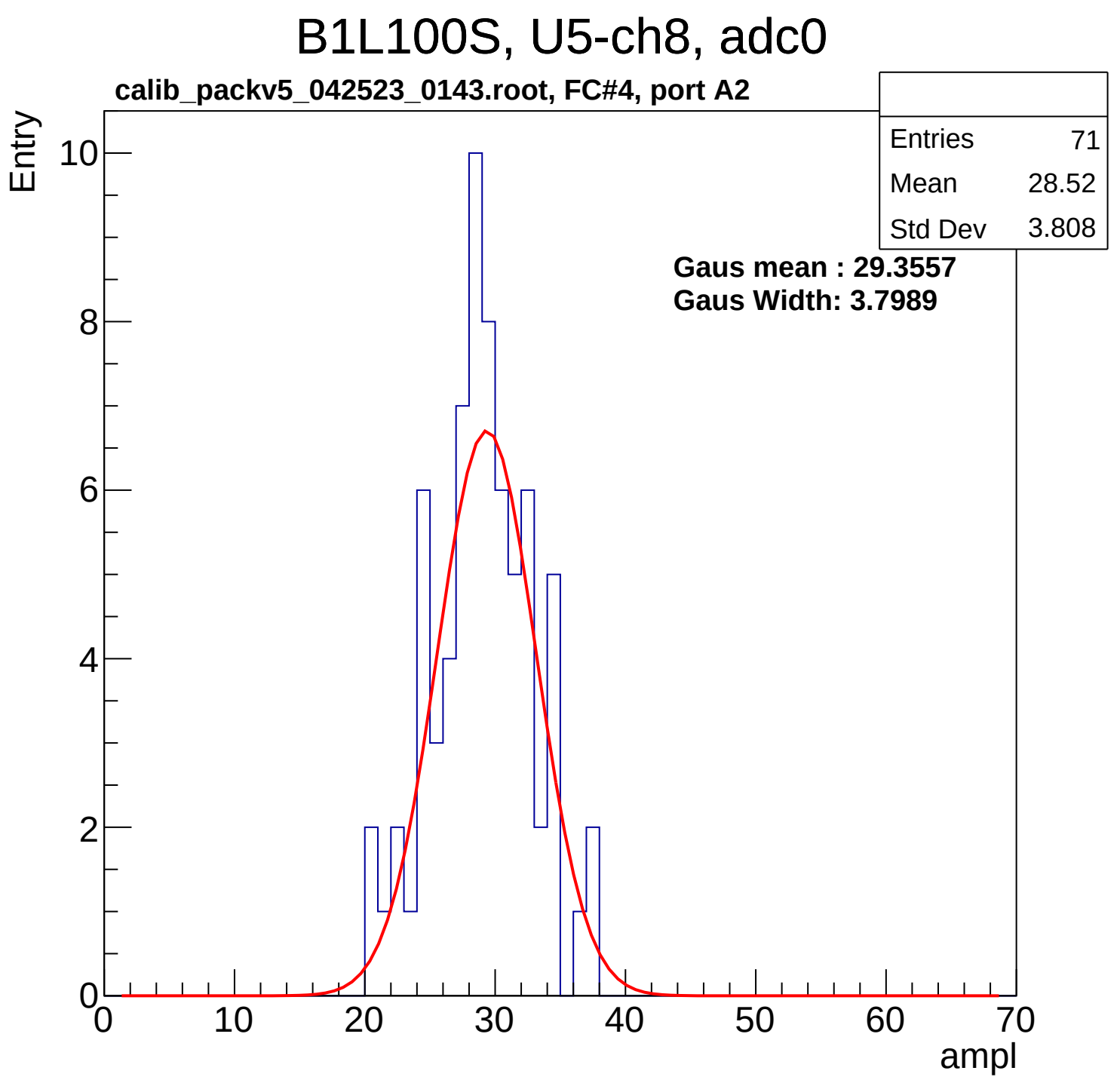
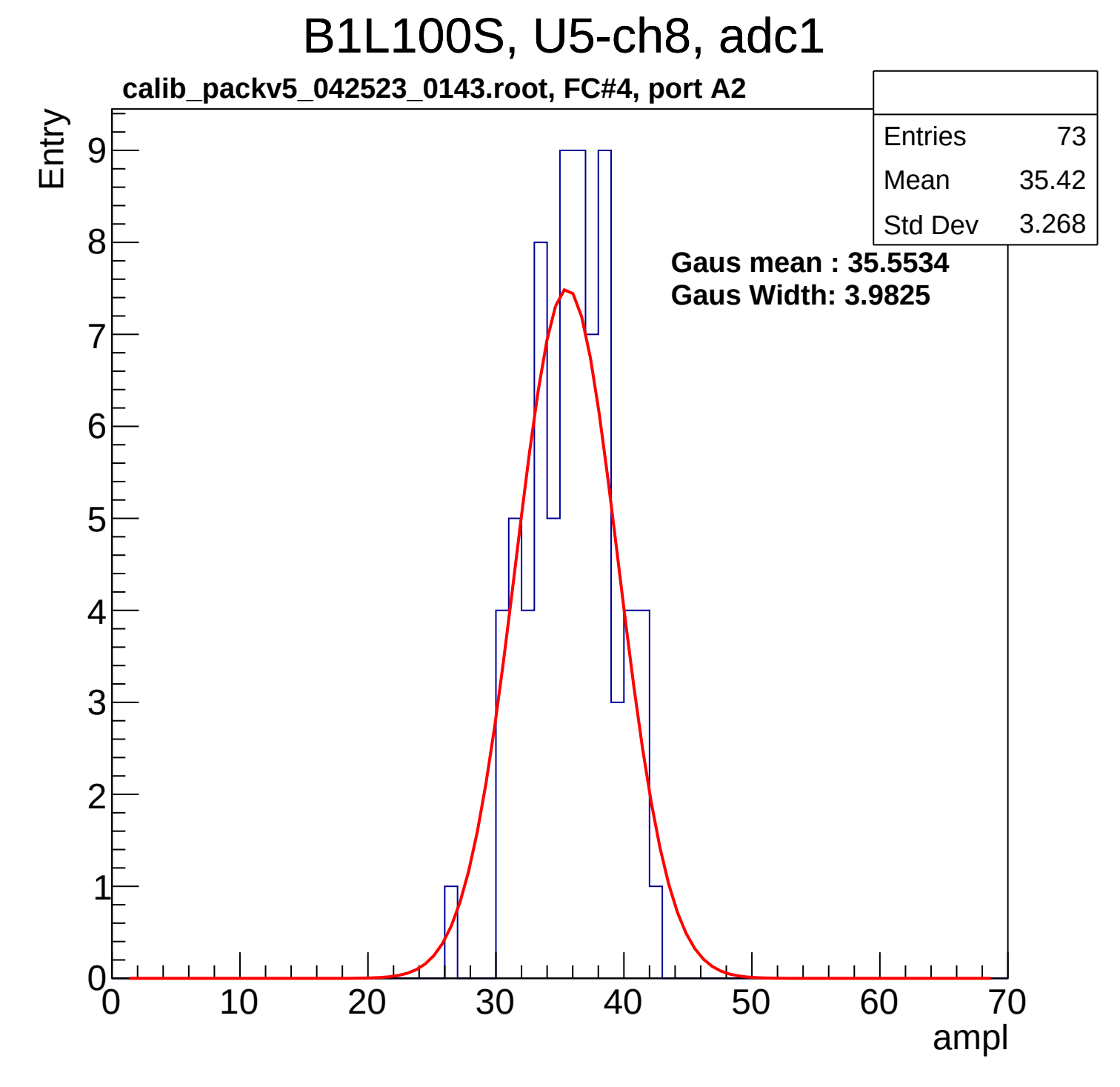

B1L100S, U5-ch7, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch8, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 28.52
Std Dev 3.808
Gaus mean : 29.3557
Gaus Width: 3.7989
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch8, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 35.42
Std Dev 3.268
Gaus mean : 35.5534
Gaus Width: 3.9825
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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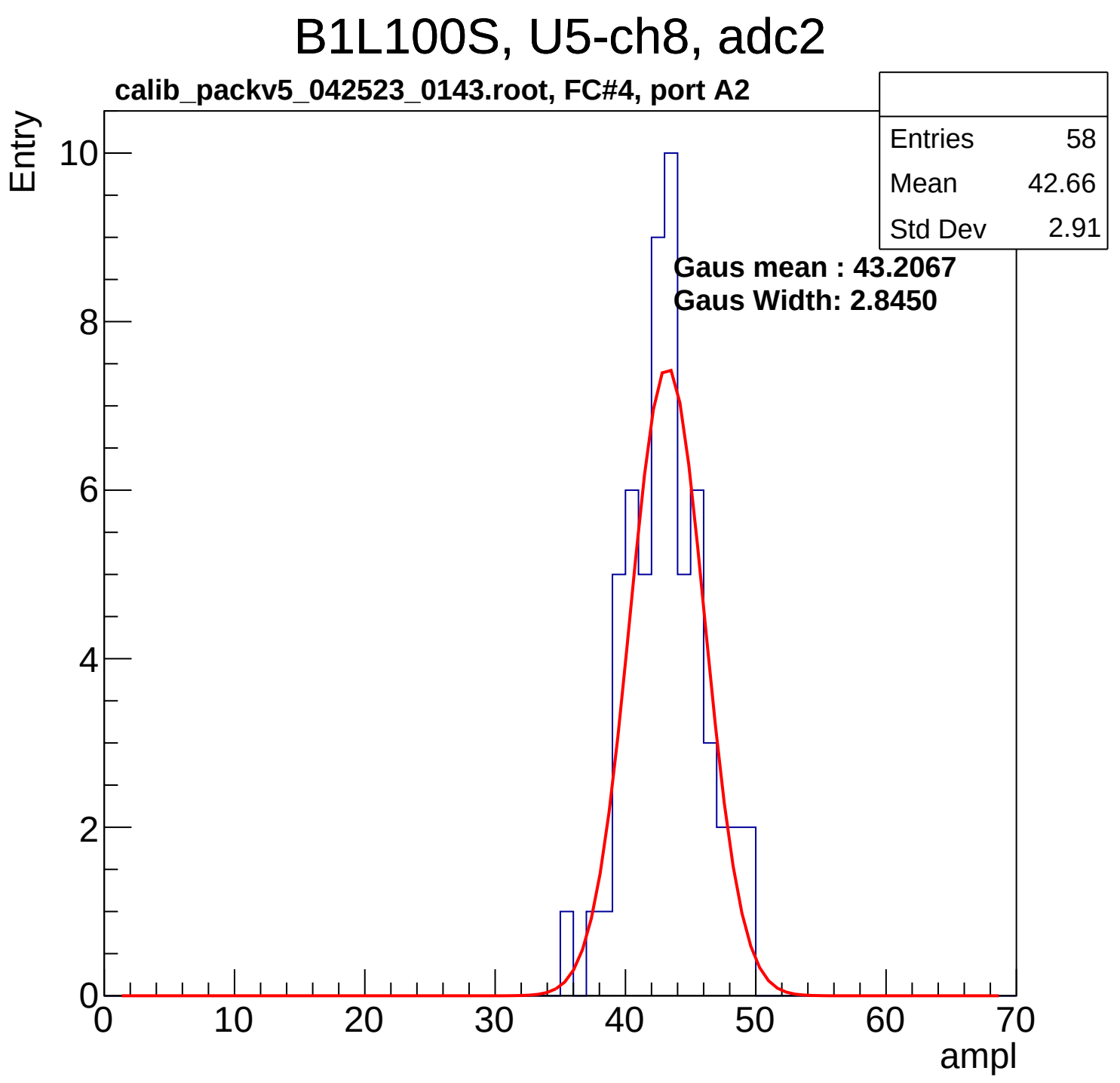
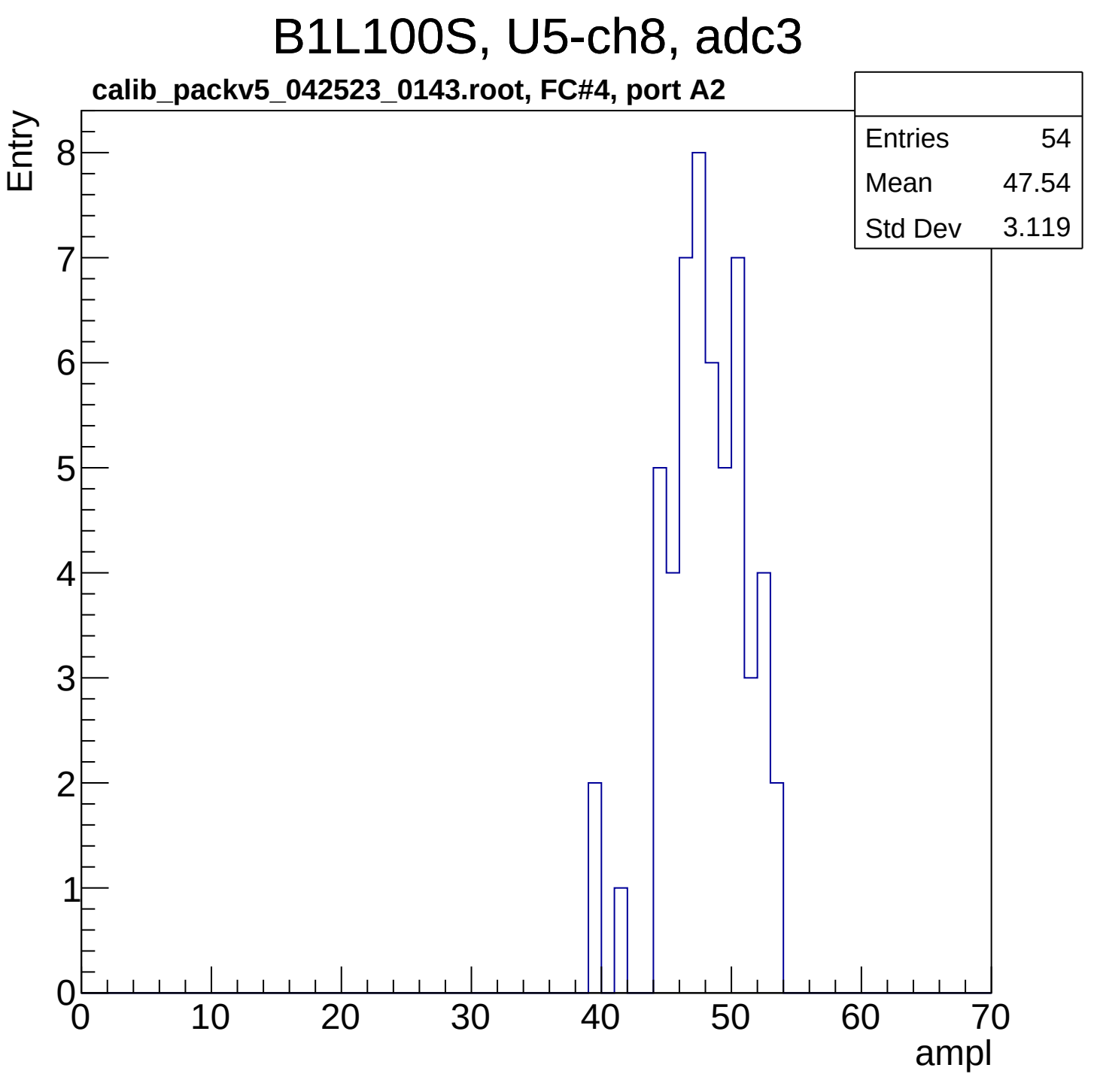
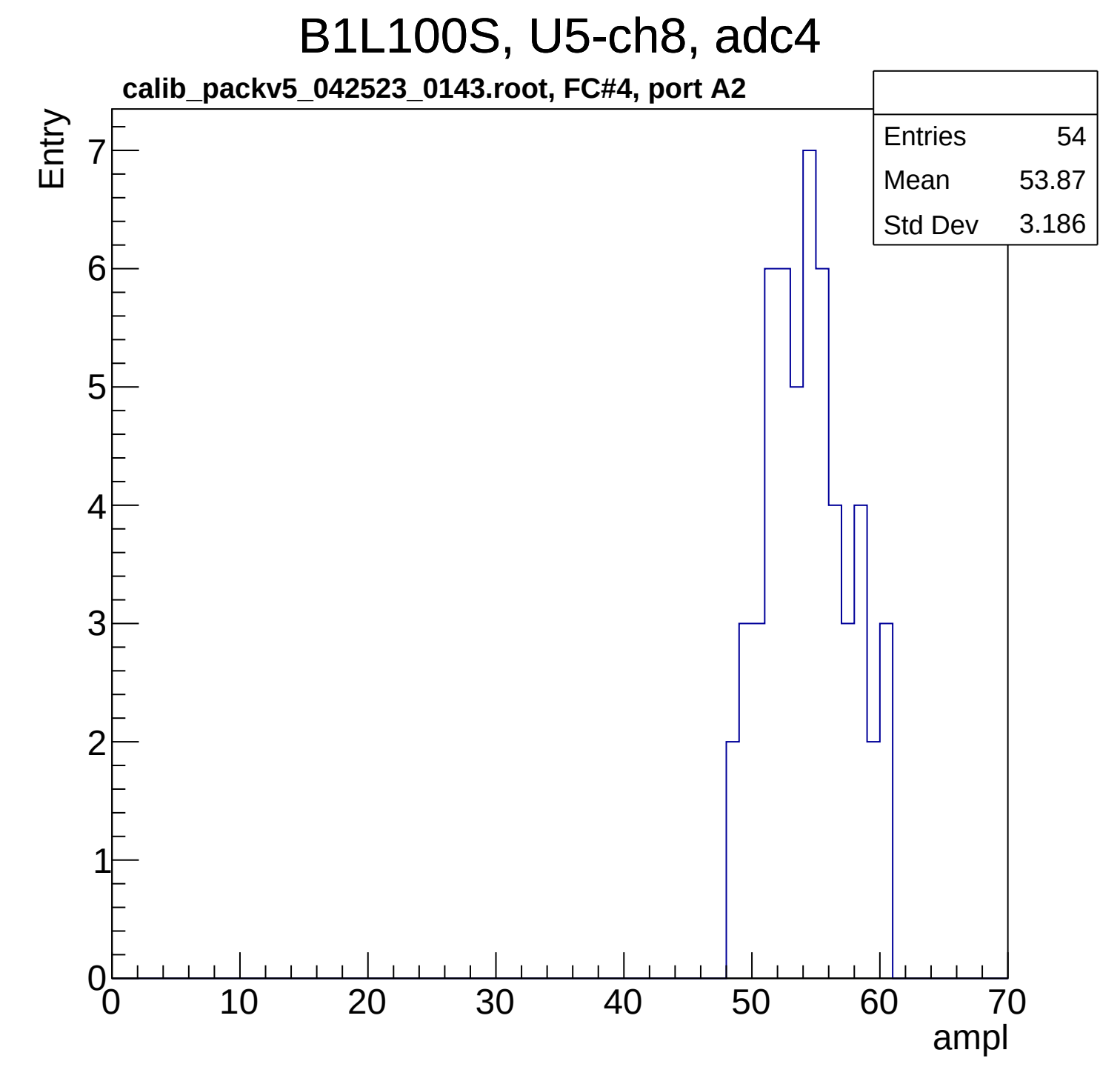
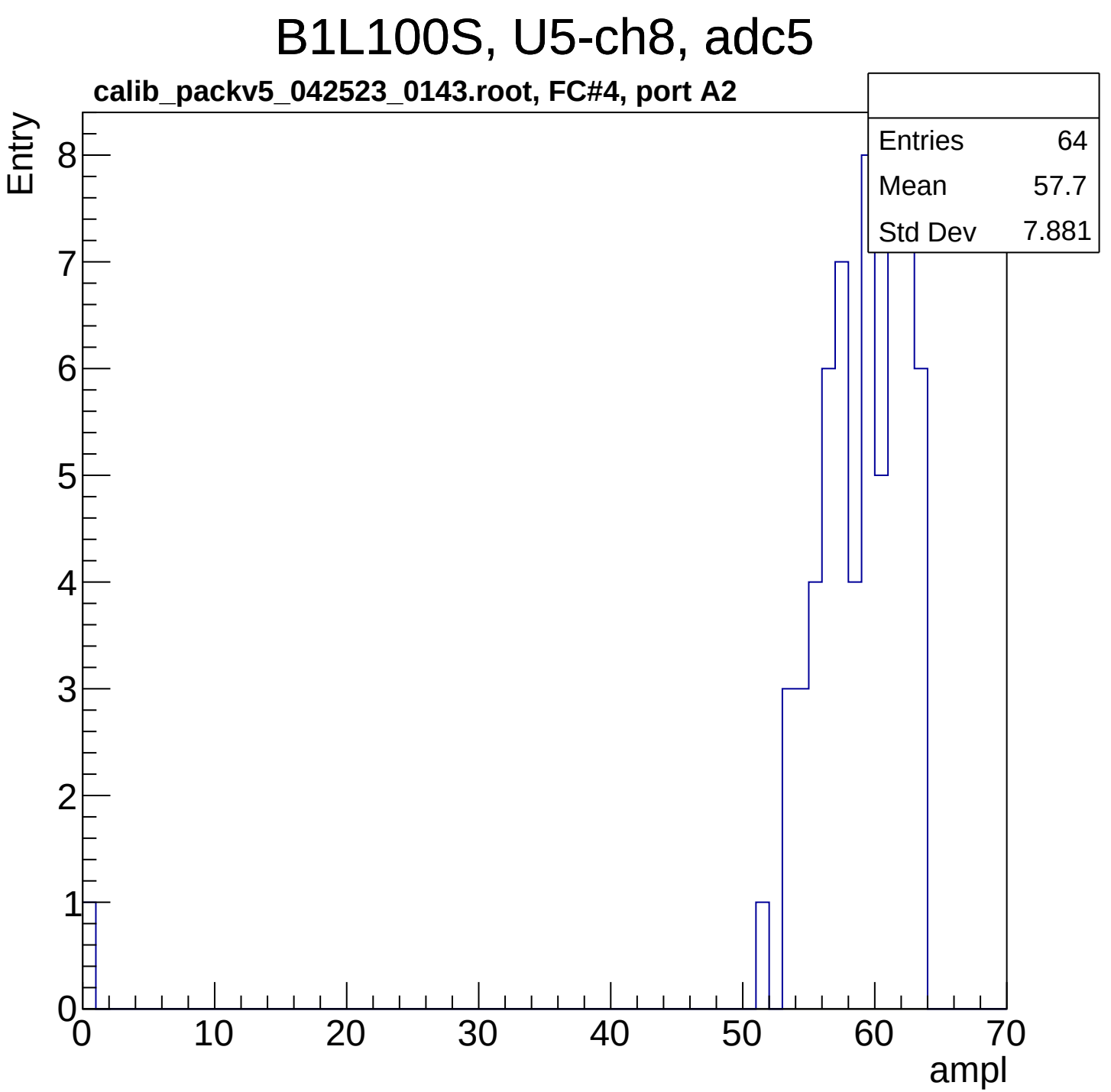

B1L100S, U5-ch8, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 42.66
Std Dev 2.91
Gaus mean : 43.2067
Gaus Width: 2.8450
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch8, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 47.54
Std Dev 3.119
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch8, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 53.87
Std Dev 3.186
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U5-ch8, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 57.7
Std Dev 7.881
Entry
ampl
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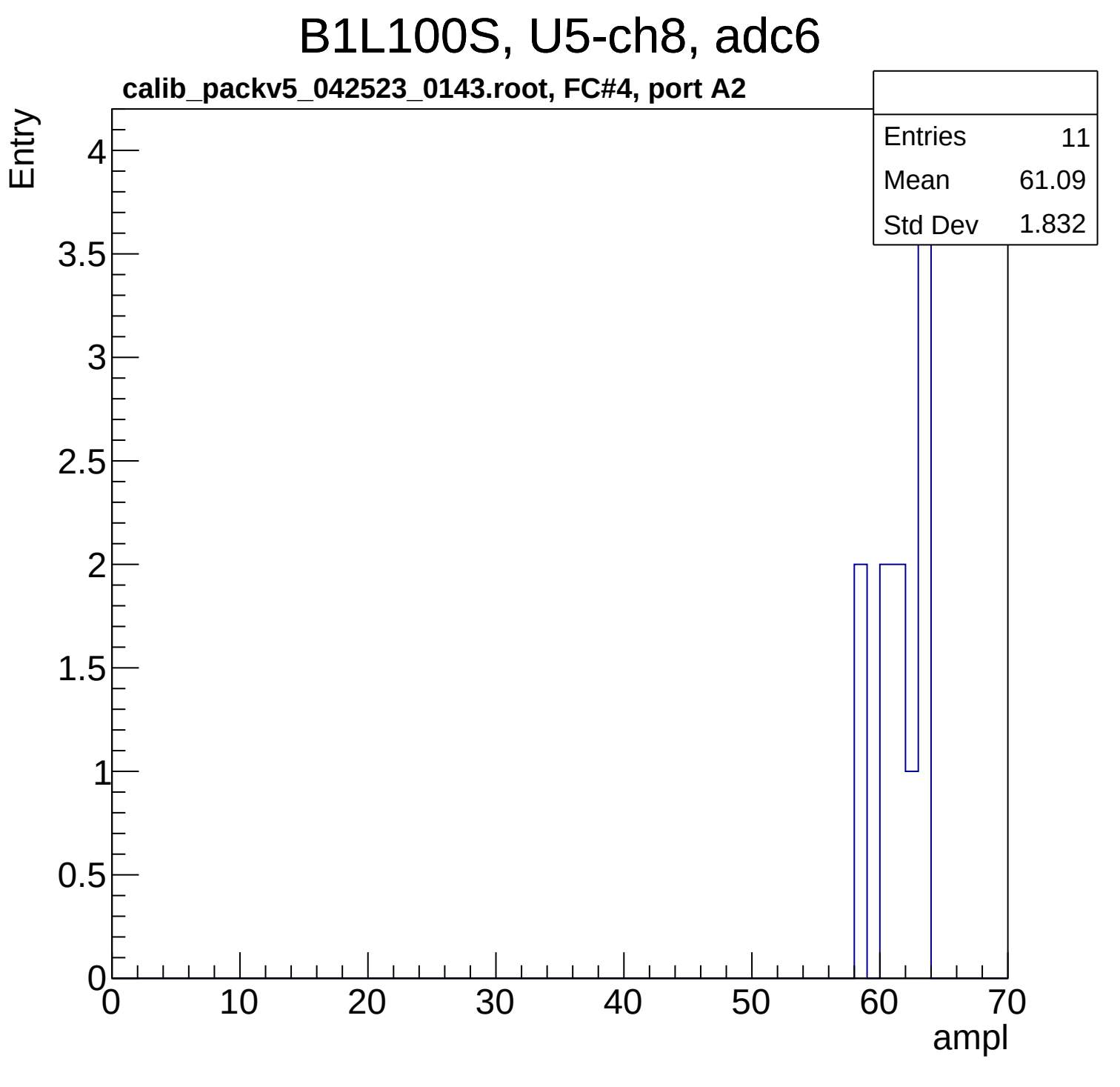
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch8, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 11
Mean 61.09
Std Dev 1.832
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
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30
40
50
60
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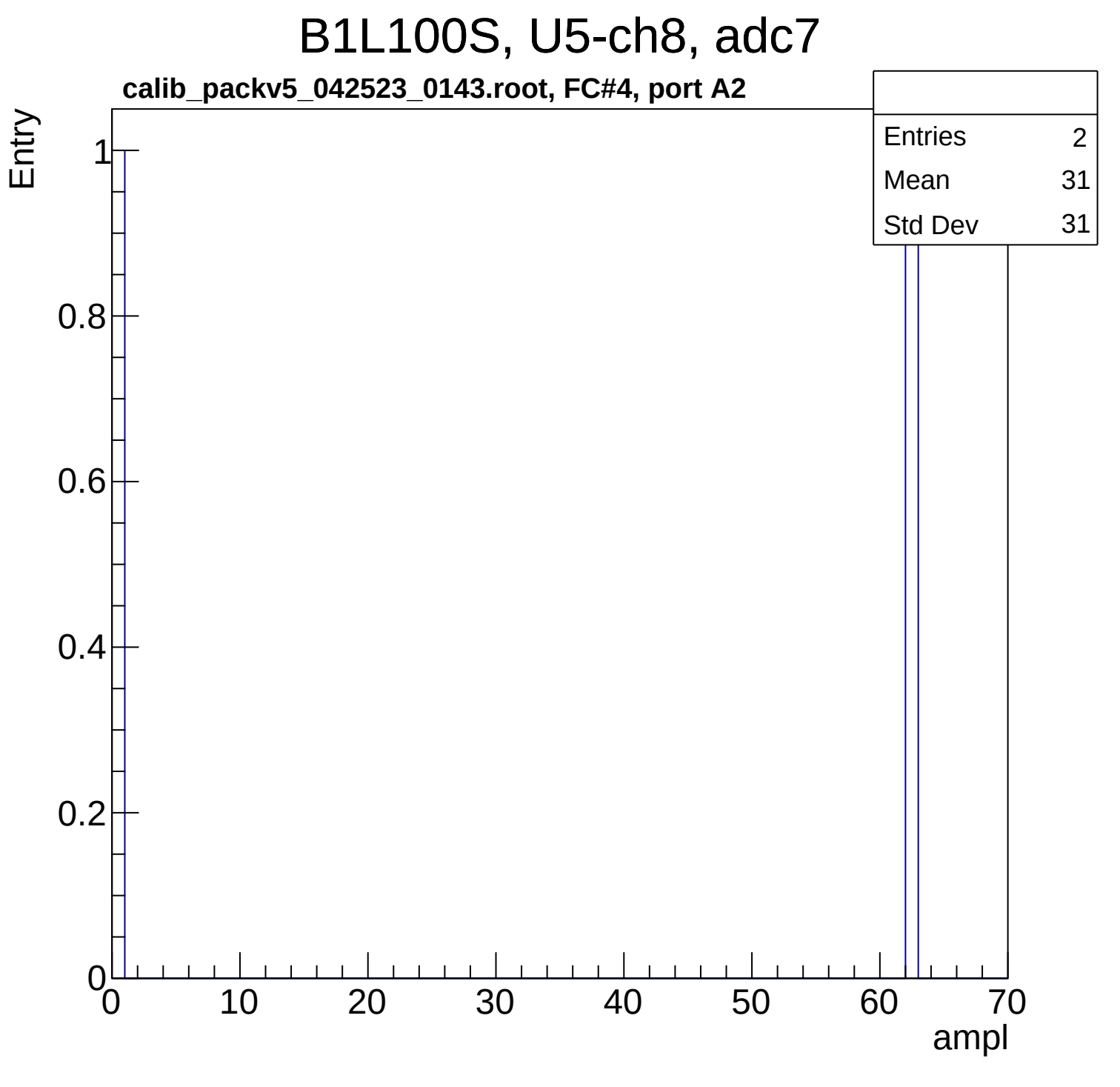
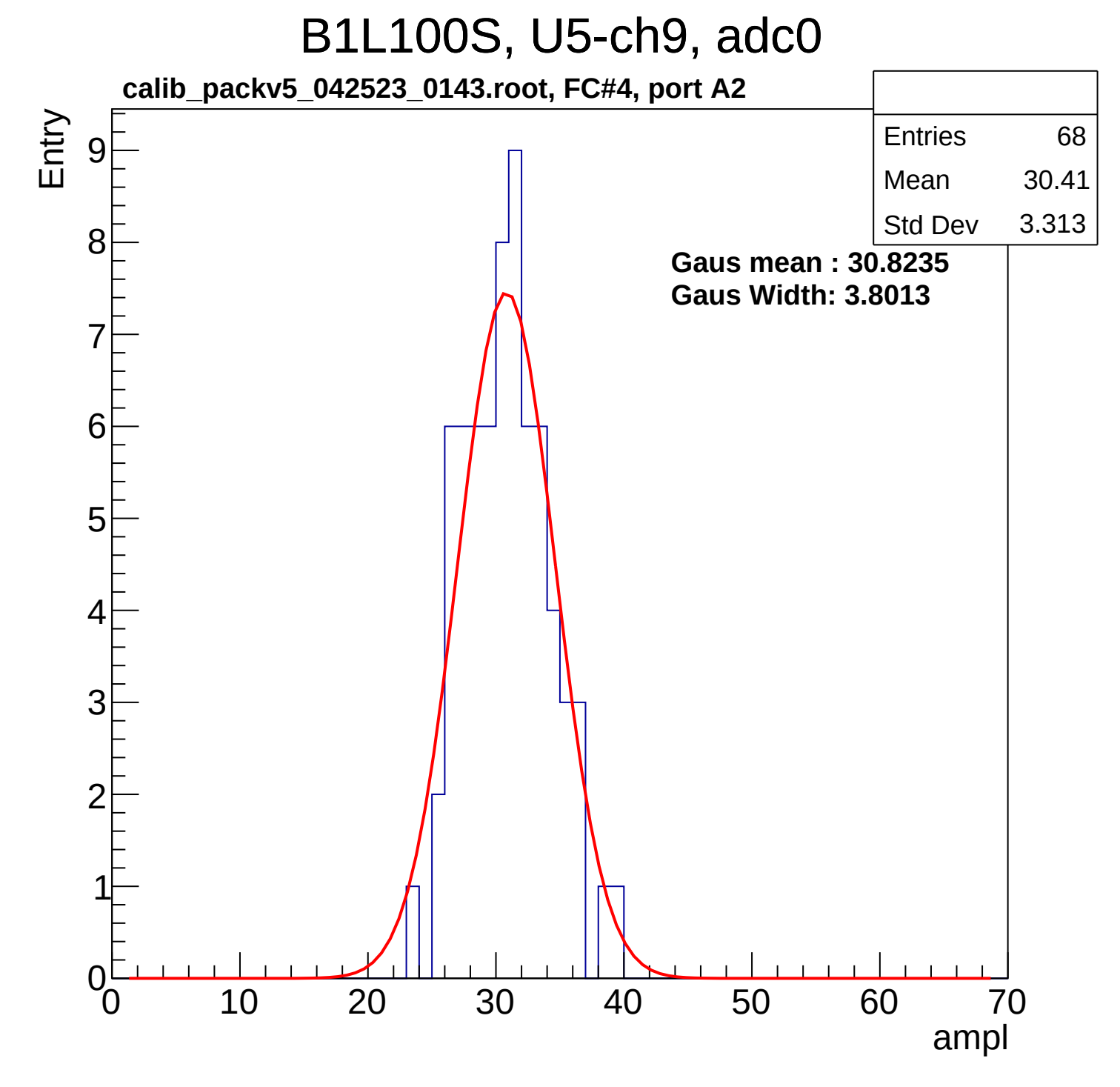
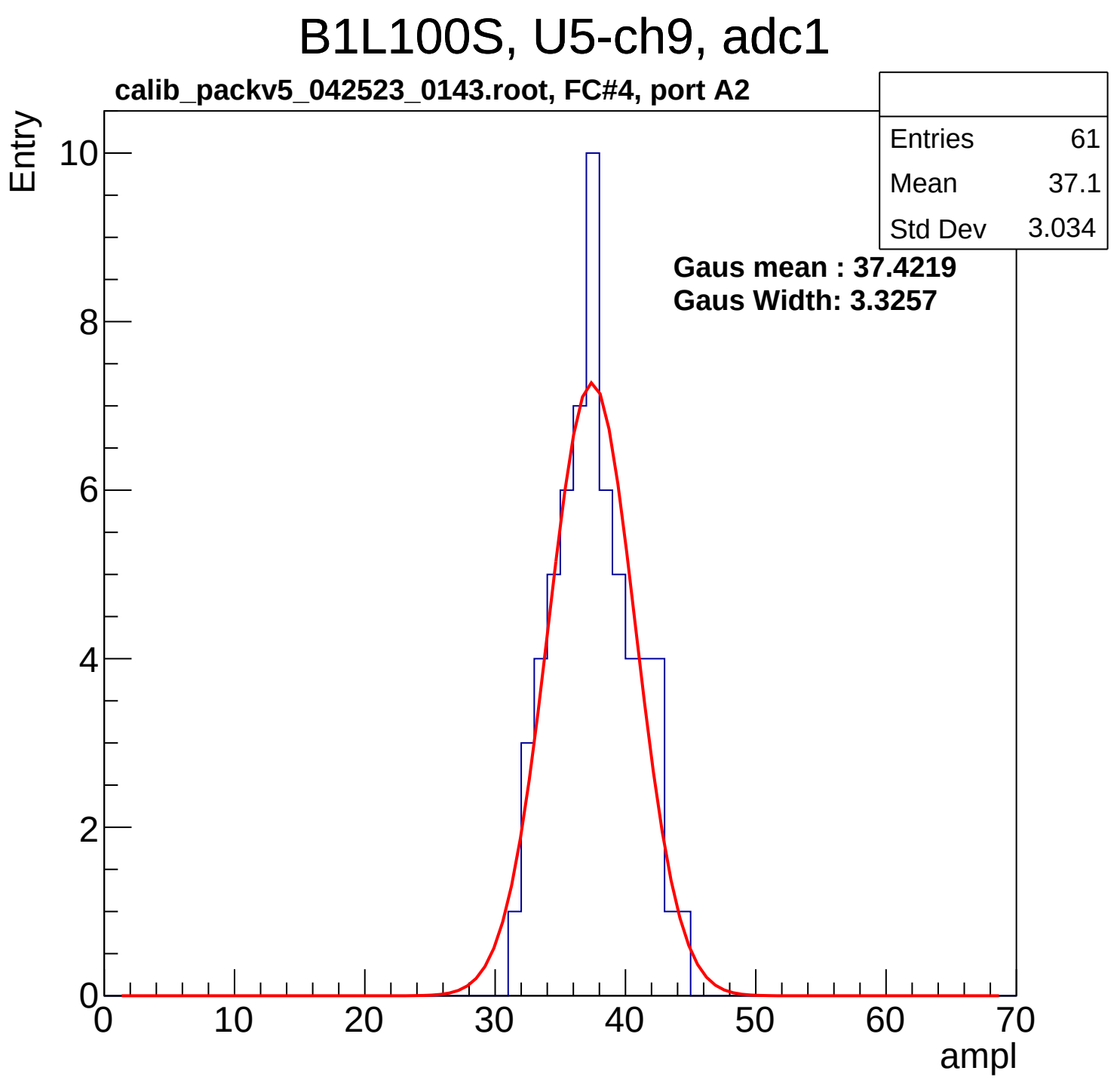
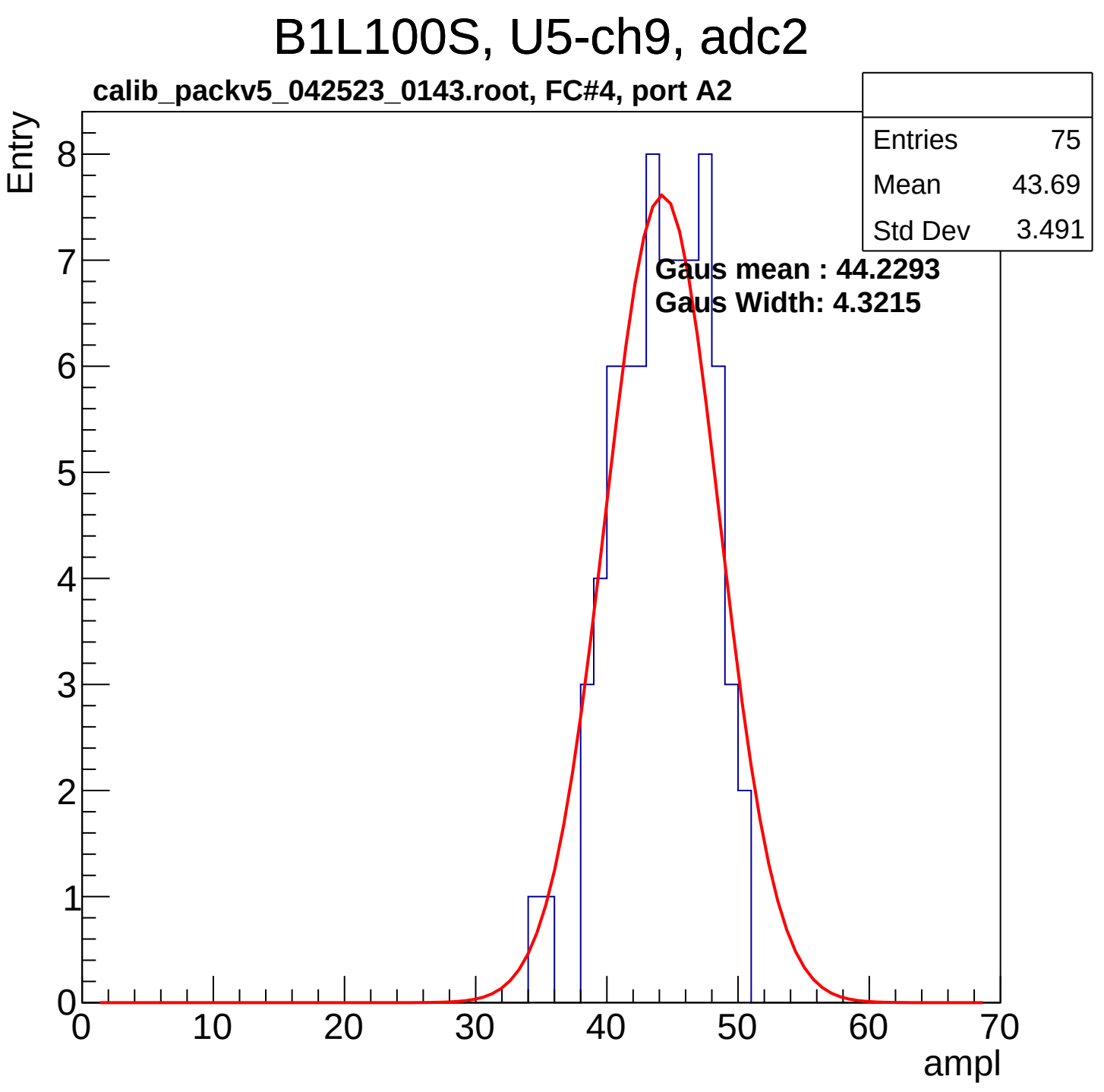

B1L100S, U5-ch8, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 31
Std Dev 31
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch9, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 30.41
Std Dev 3.313
Gaus mean : 30.8235
Gaus Width: 3.8013
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch9, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 37.1
Std Dev 3.034
Gaus mean : 37.4219
Gaus Width: 3.3257
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch9, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 75
Mean 43.69
Std Dev 3.491
Gaus mean : 44.2293
Gaus Width: 4.3215
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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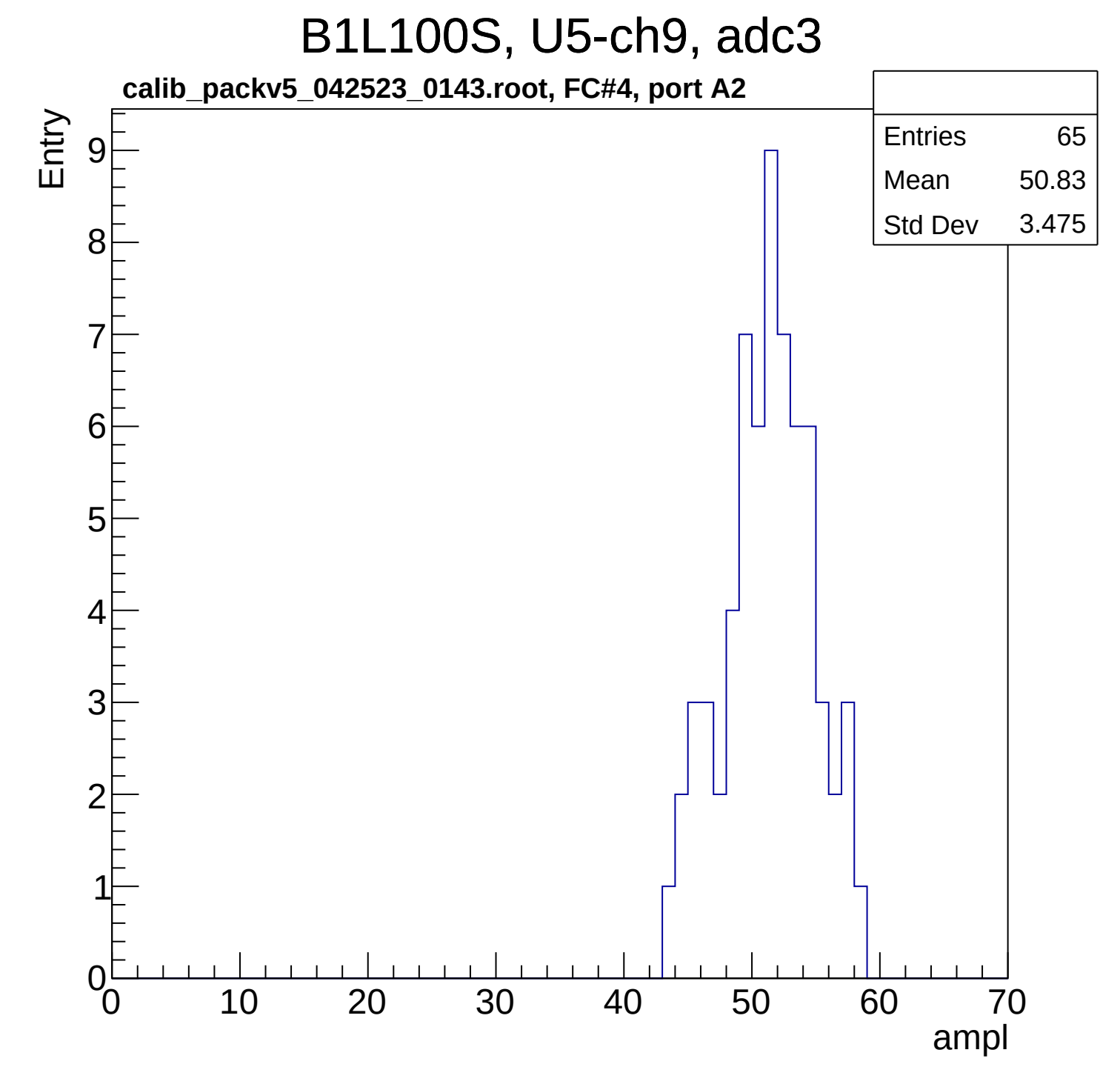
B1L100S, U5-ch9, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 50.83
Std Dev 3.475
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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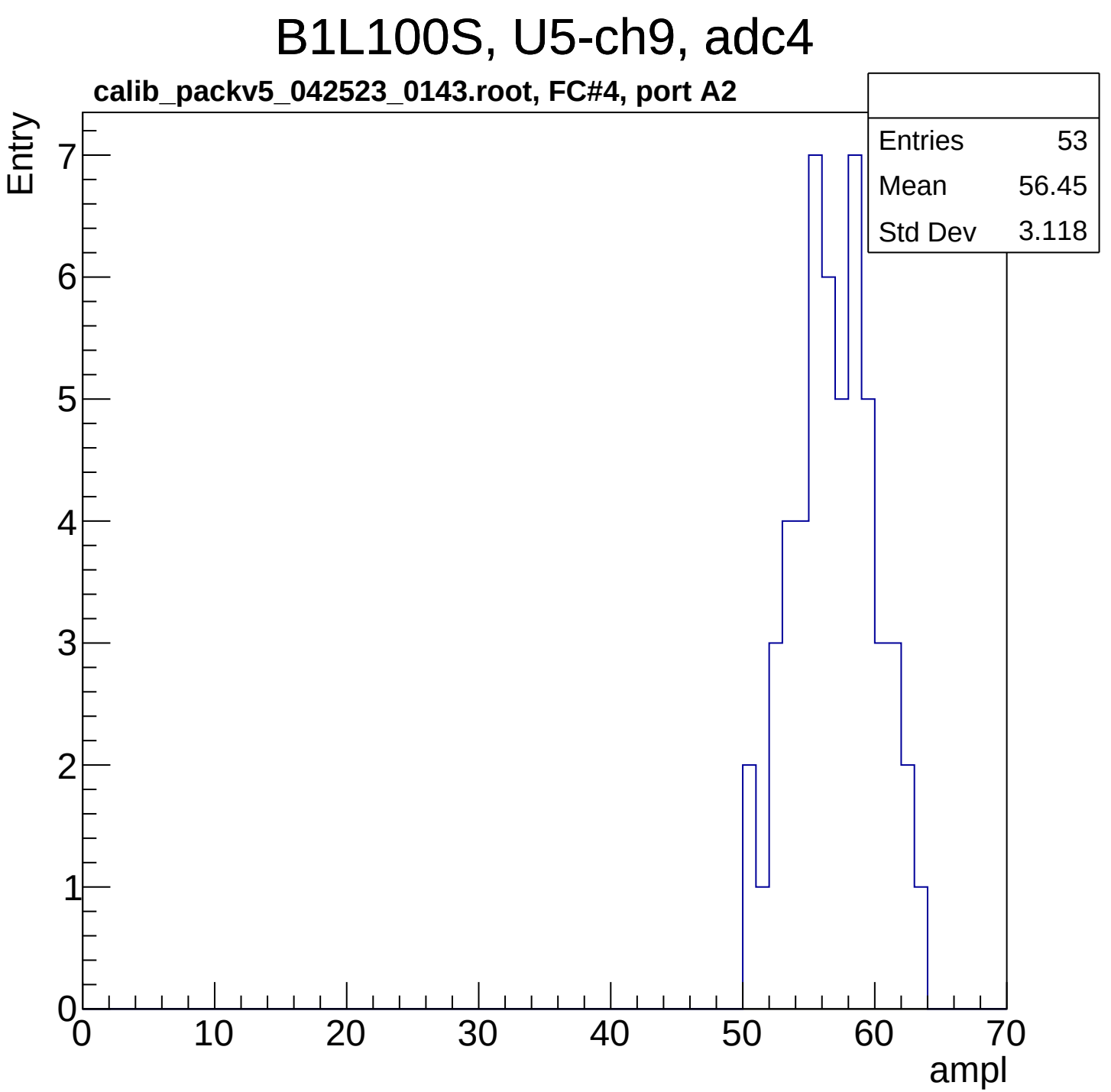
B1L100S, U5-ch9, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 56.45
Std Dev 3.118
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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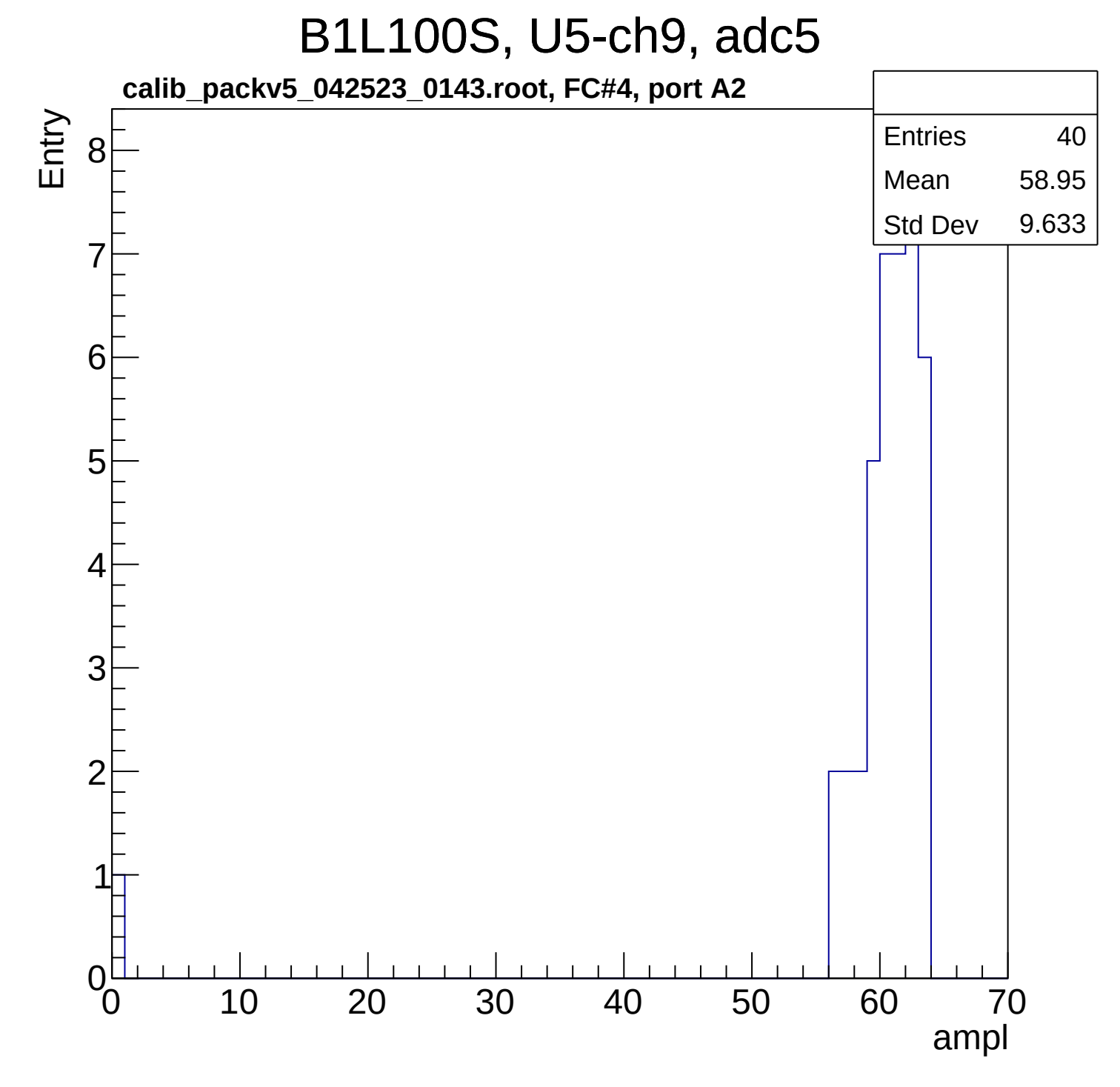
40
50
60
70


B1L100S, U5-ch9, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 40
Mean 58.95
Std Dev 9.633
Entry
ampl
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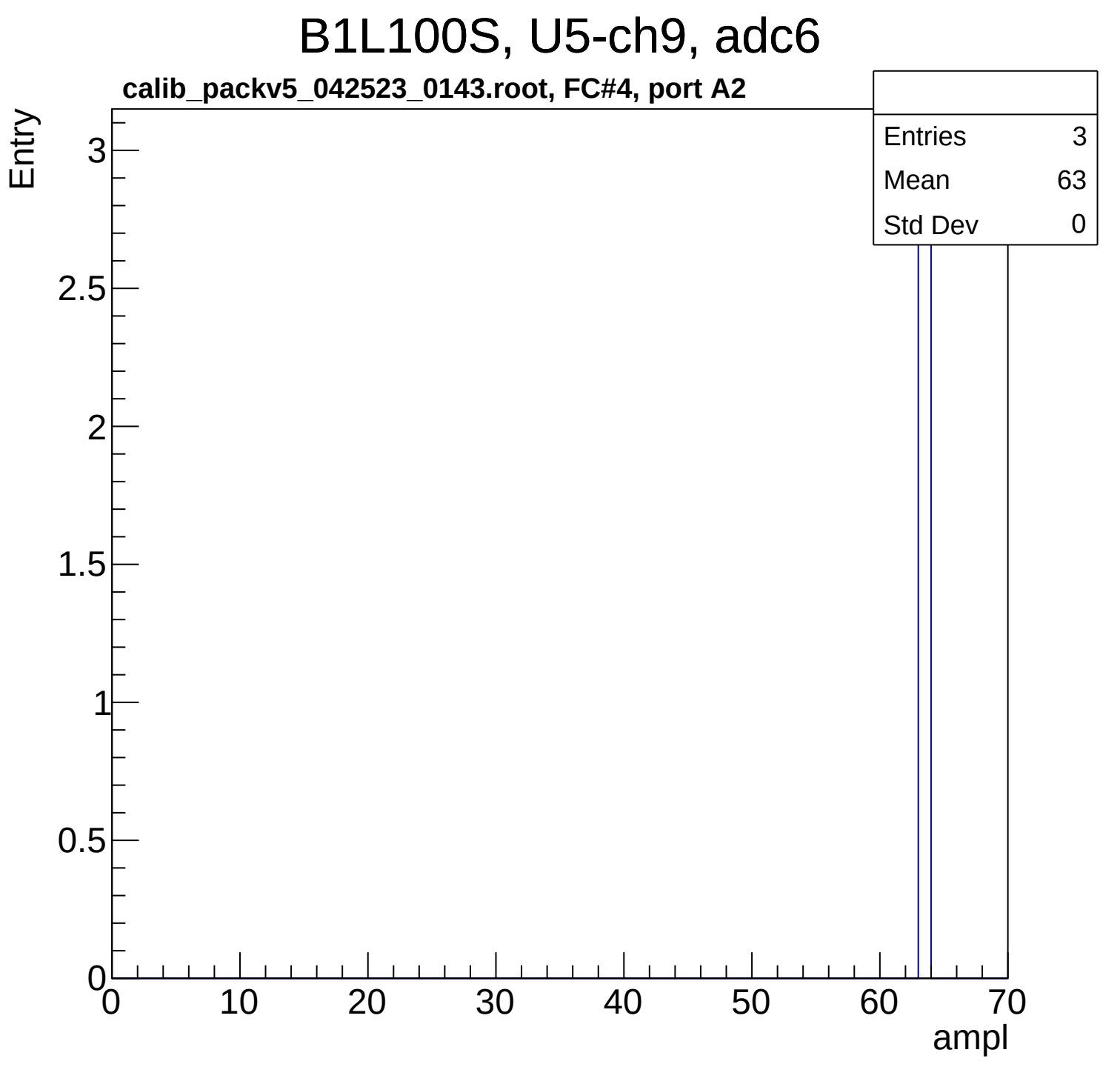
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch9, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 63
Std Dev 0
Entry
ampl
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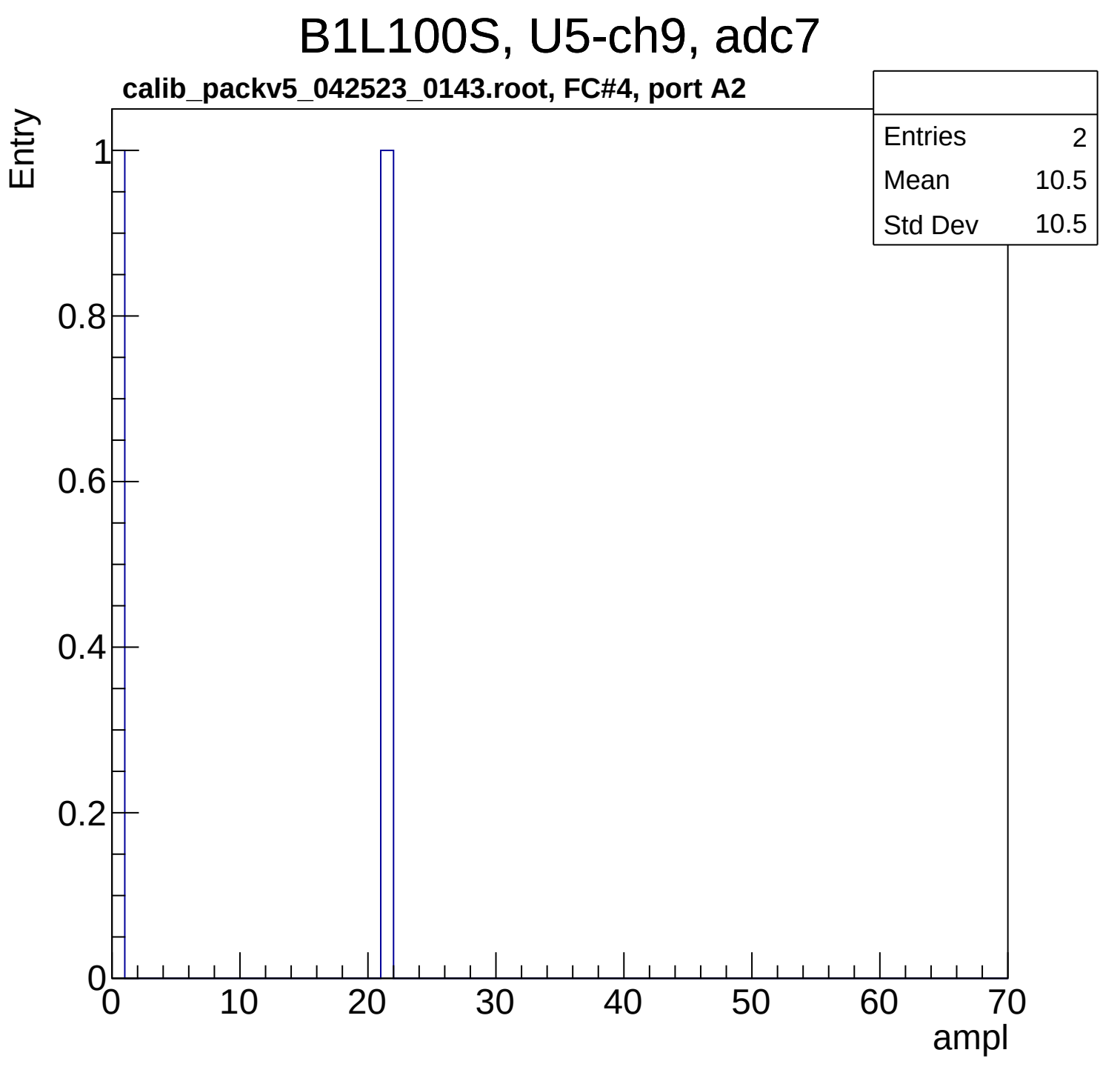
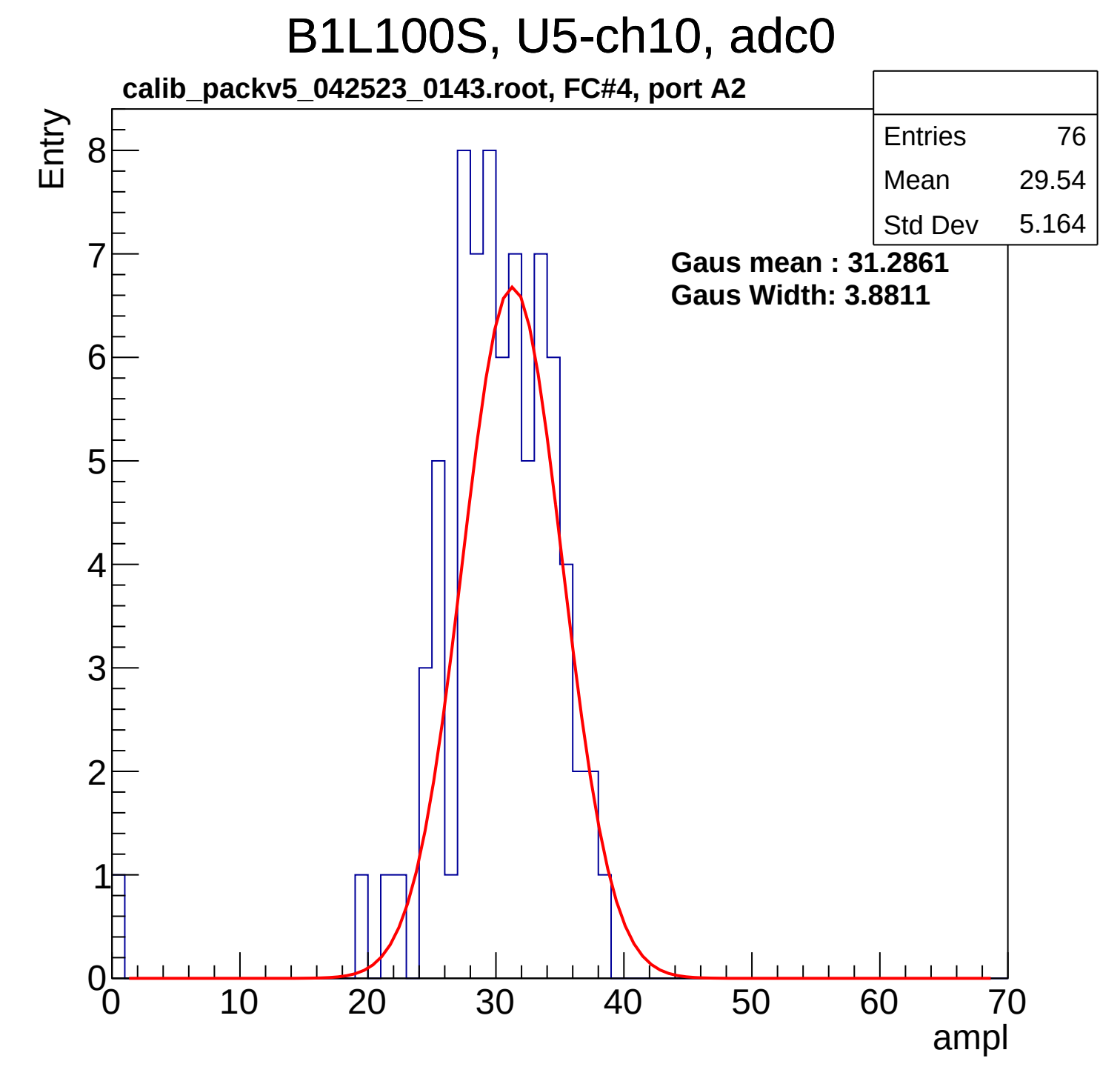
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L100S, U5-ch9, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 10.5
Std Dev 10.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch10, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 76
Mean 29.54
Std Dev 5.164
Gaus mean : 31.2861
Gaus Width: 3.8811
Entry
ampl
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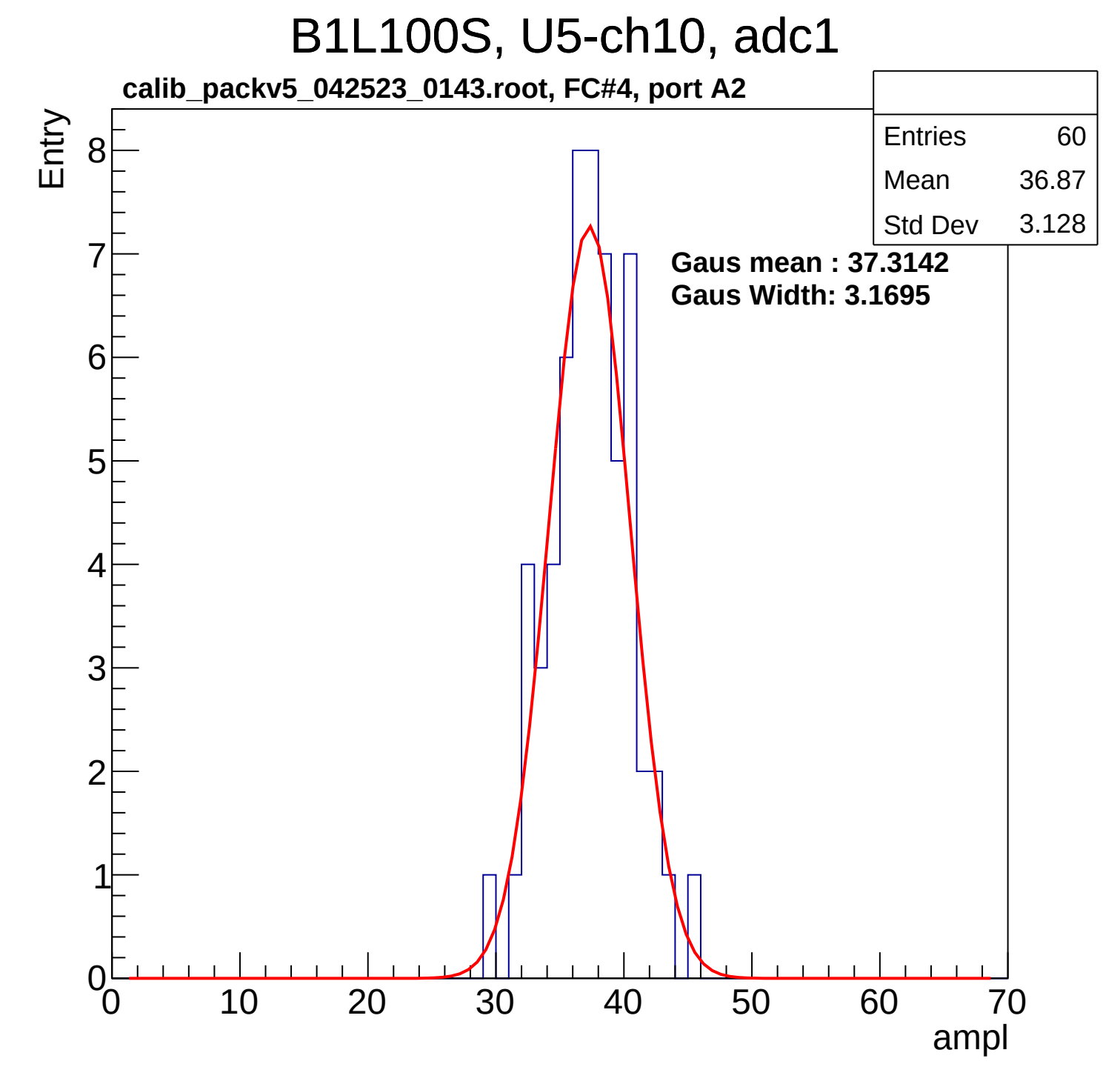
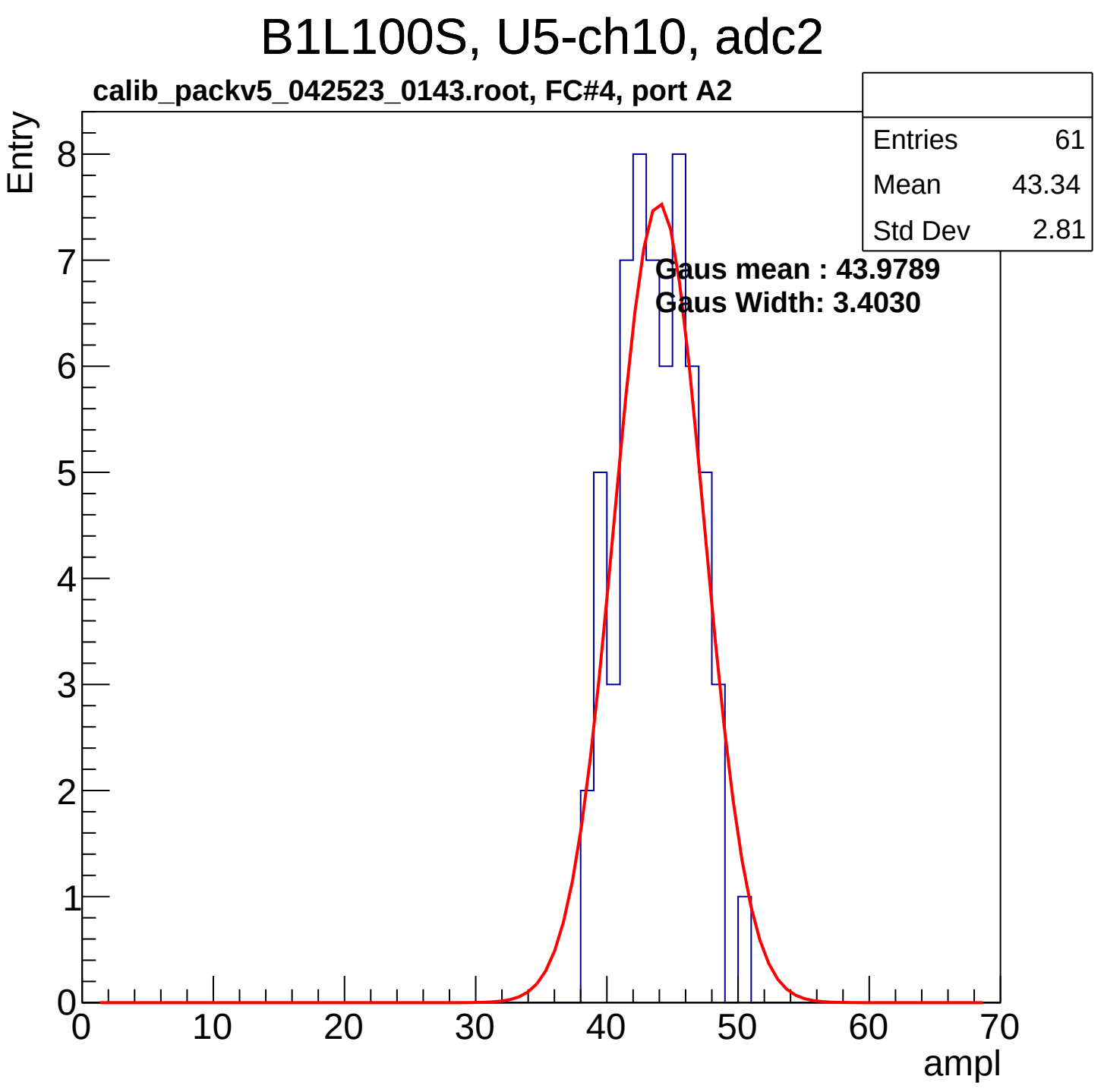
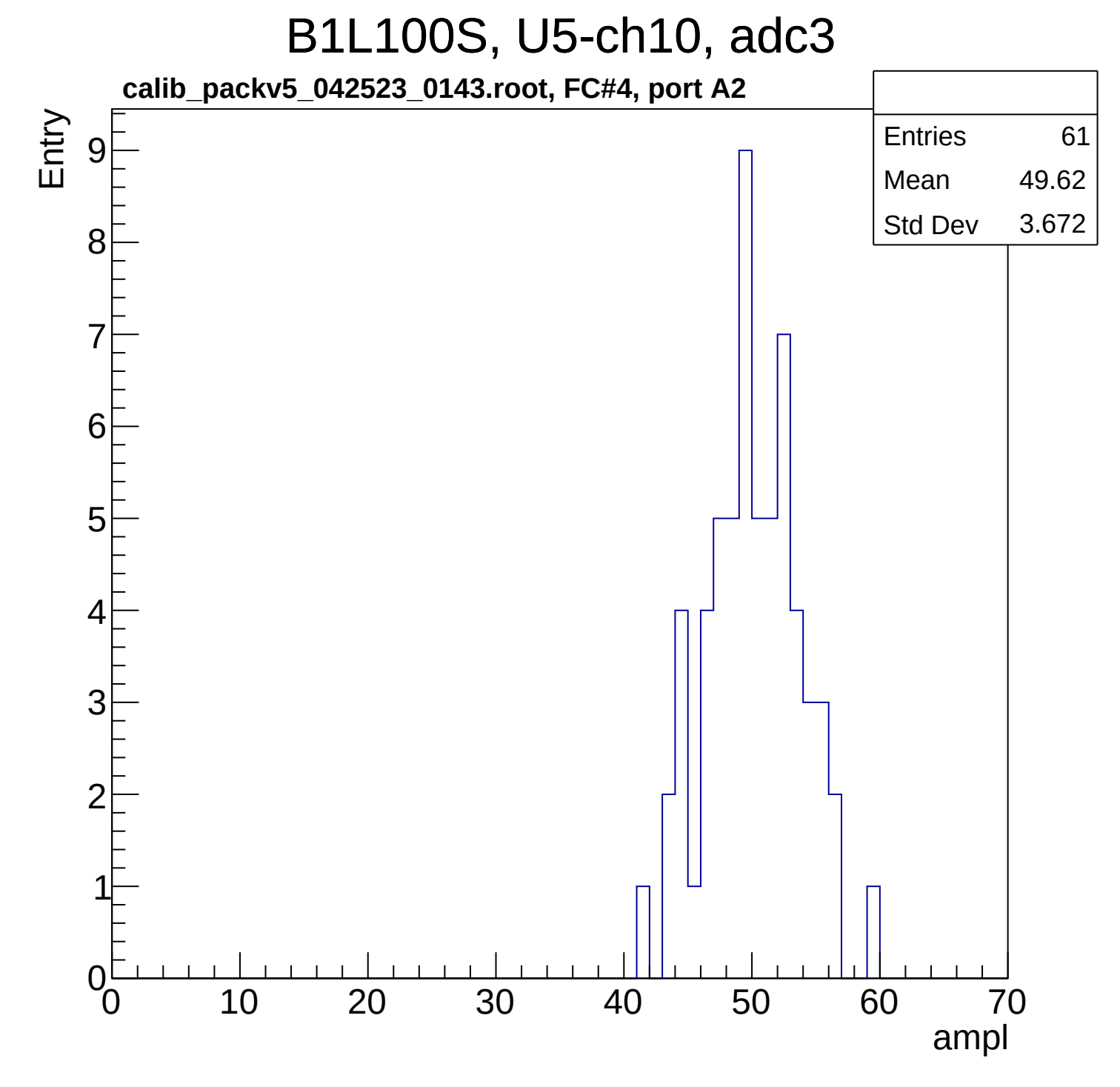
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch10, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 36.87
Std Dev 3.128
Gaus mean : 37.3142
Gaus Width: 3.1695
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch10, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 43.34
Std Dev 2.81
Gaus mean : 43.9789
Gaus Width: 3.4030
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch10, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 49.62
Std Dev 3.672
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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60
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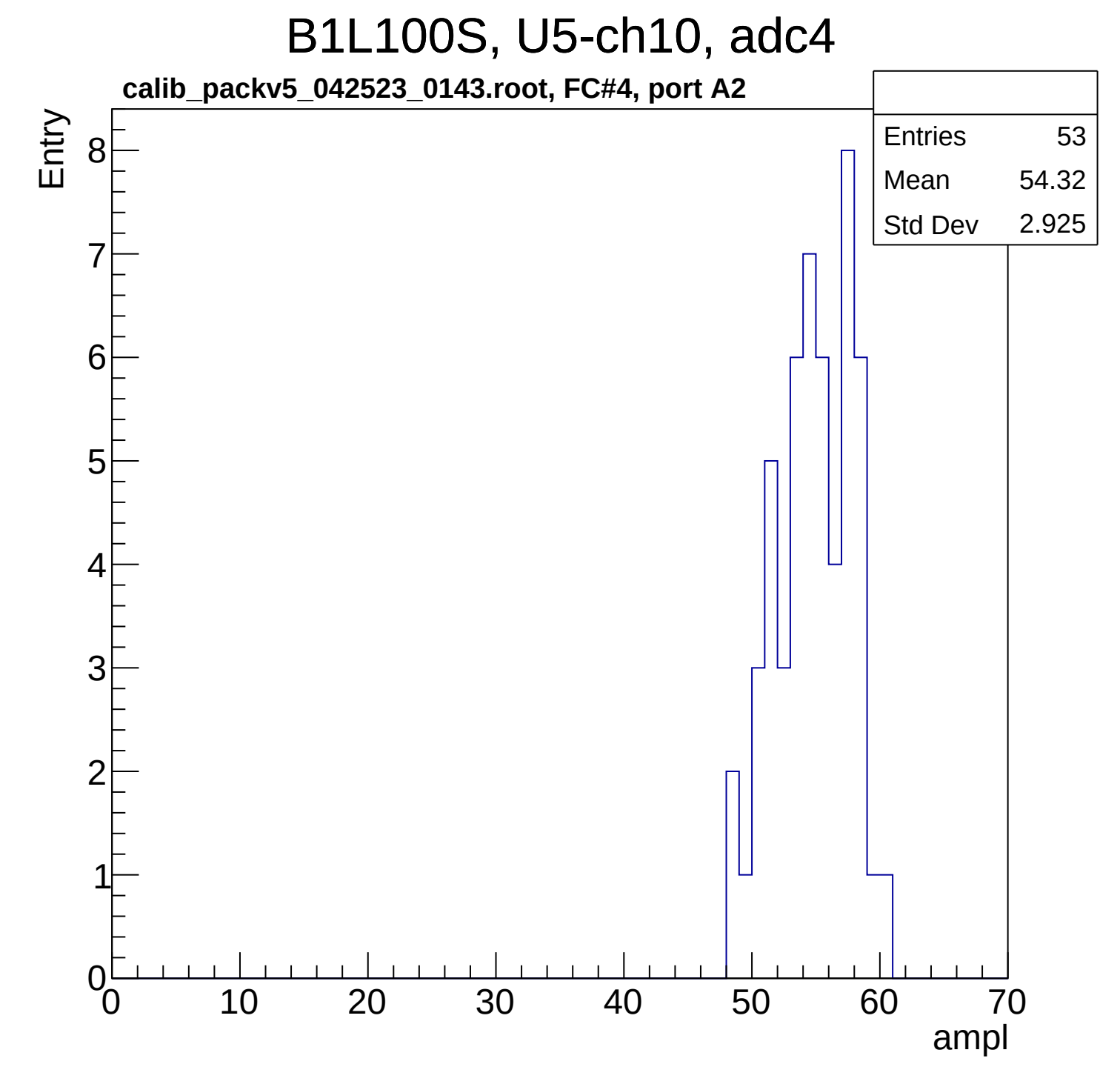
B1L100S, U5-ch10, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 54.32
Std Dev 2.925
Entry
ampl
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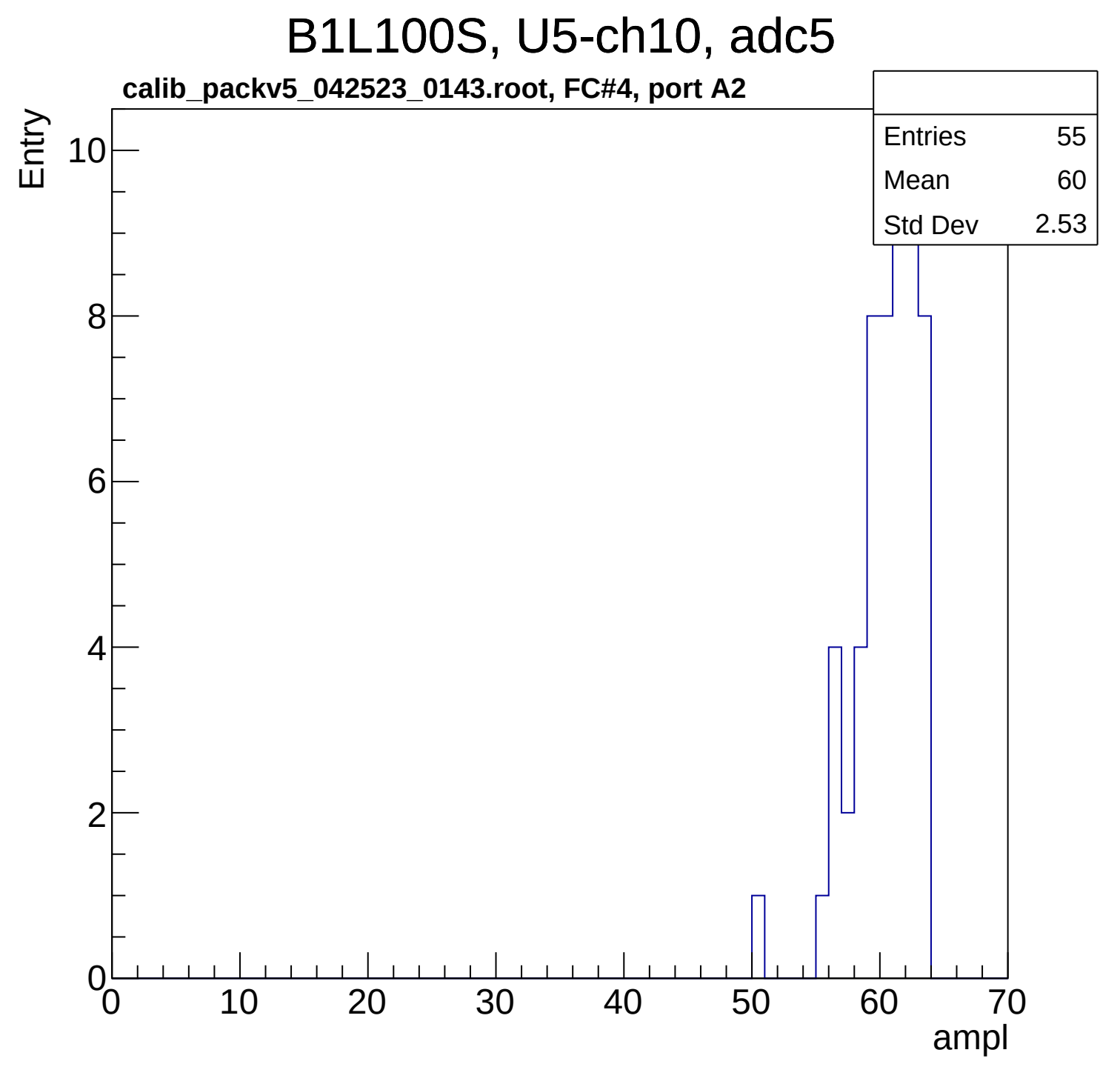
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch10, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 60
Std Dev 2.53
Entry
ampl
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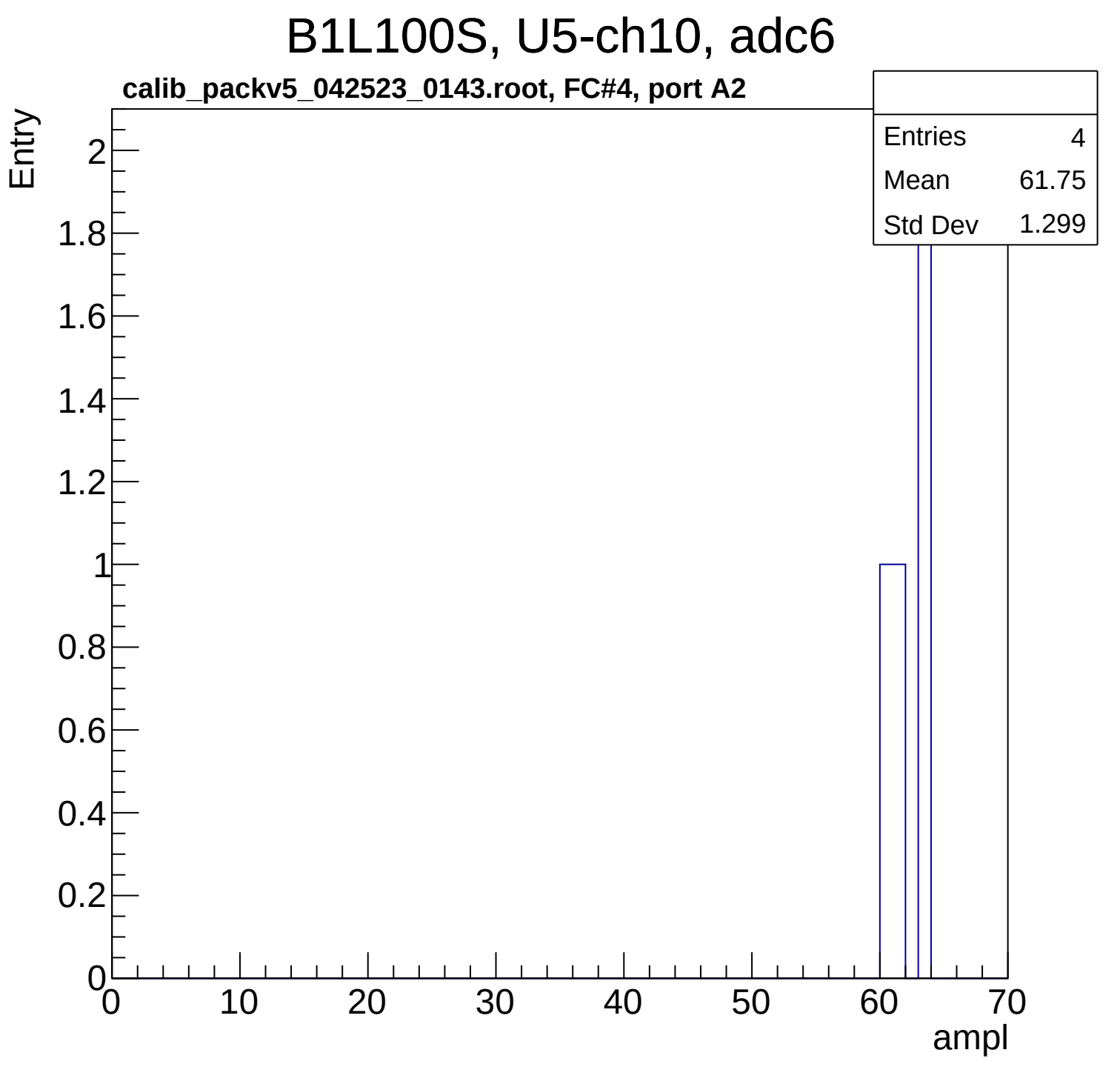
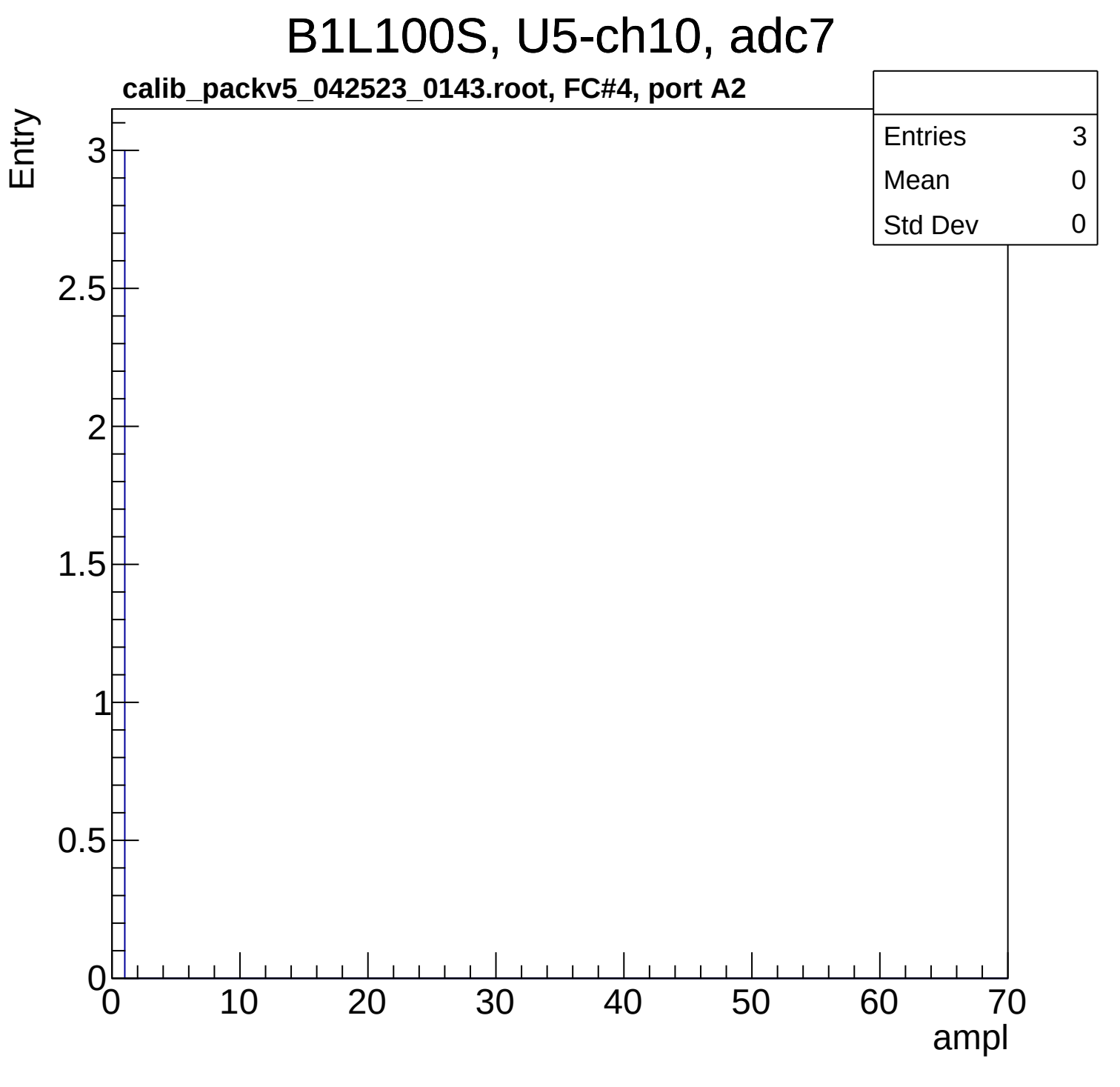
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch10, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 4
Mean 61.75
Std Dev 1.299
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L100S, U5-ch10, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 0
Std Dev 0
Entry
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2.5
2
1.5
1
0.5
0
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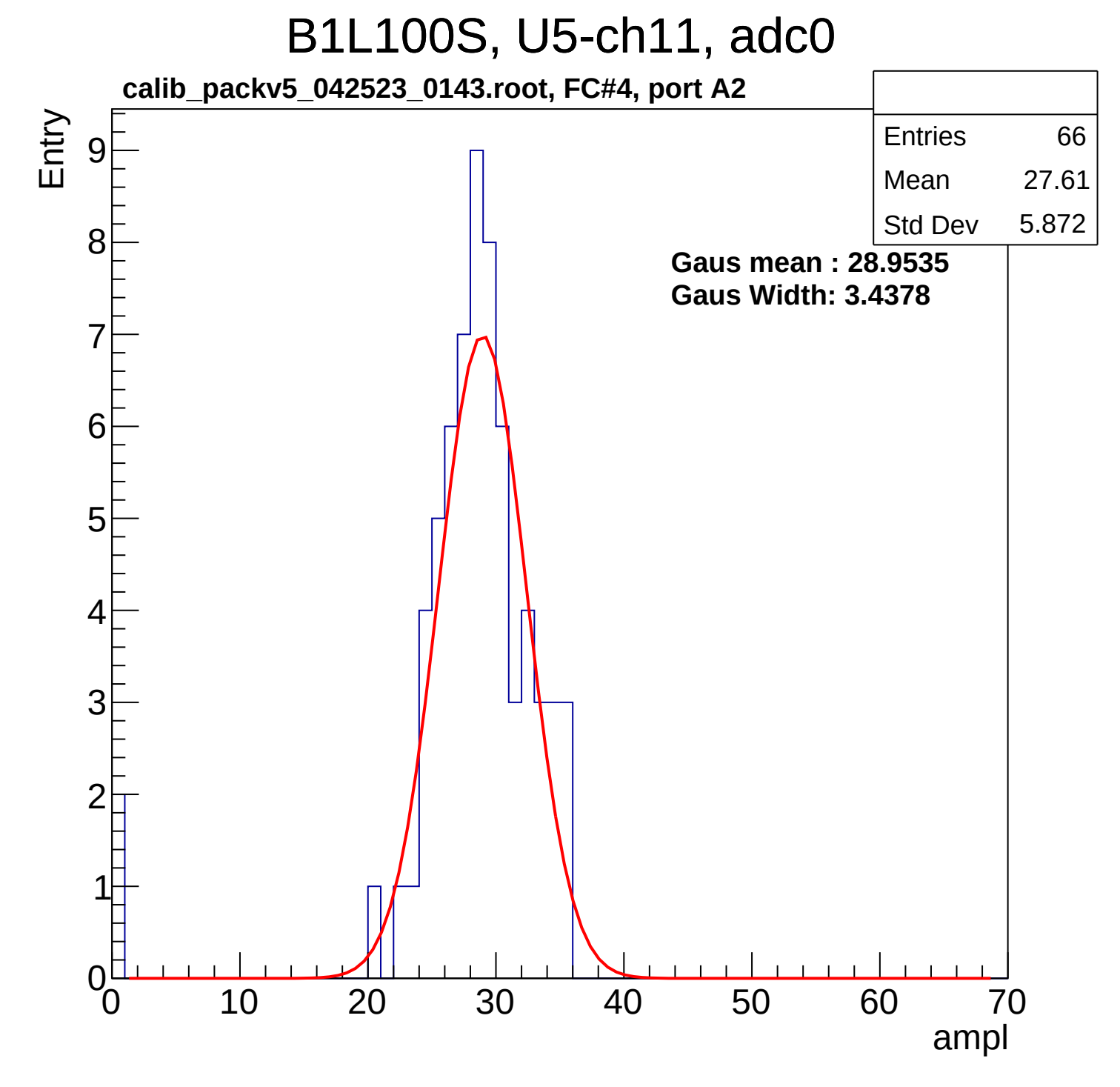
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch11, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 27.61
Std Dev 5.872
Gaus mean : 28.9535
Gaus Width: 3.4378
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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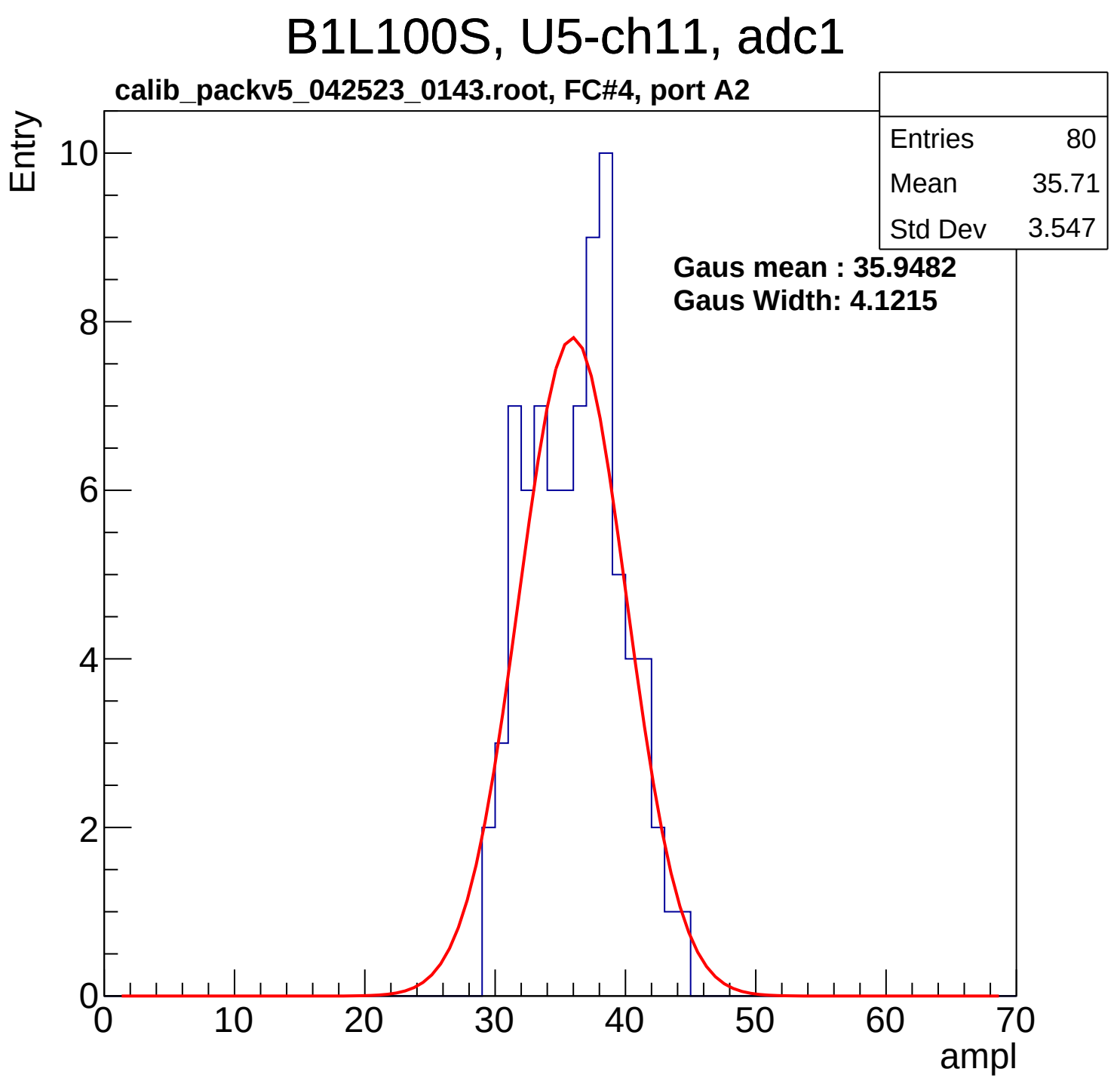
60
70


B1L100S, U5-ch11, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 80
Mean 35.71
Std Dev 3.547
Gaus mean : 35.9482
Gaus Width: 4.1215
Entry
ampl
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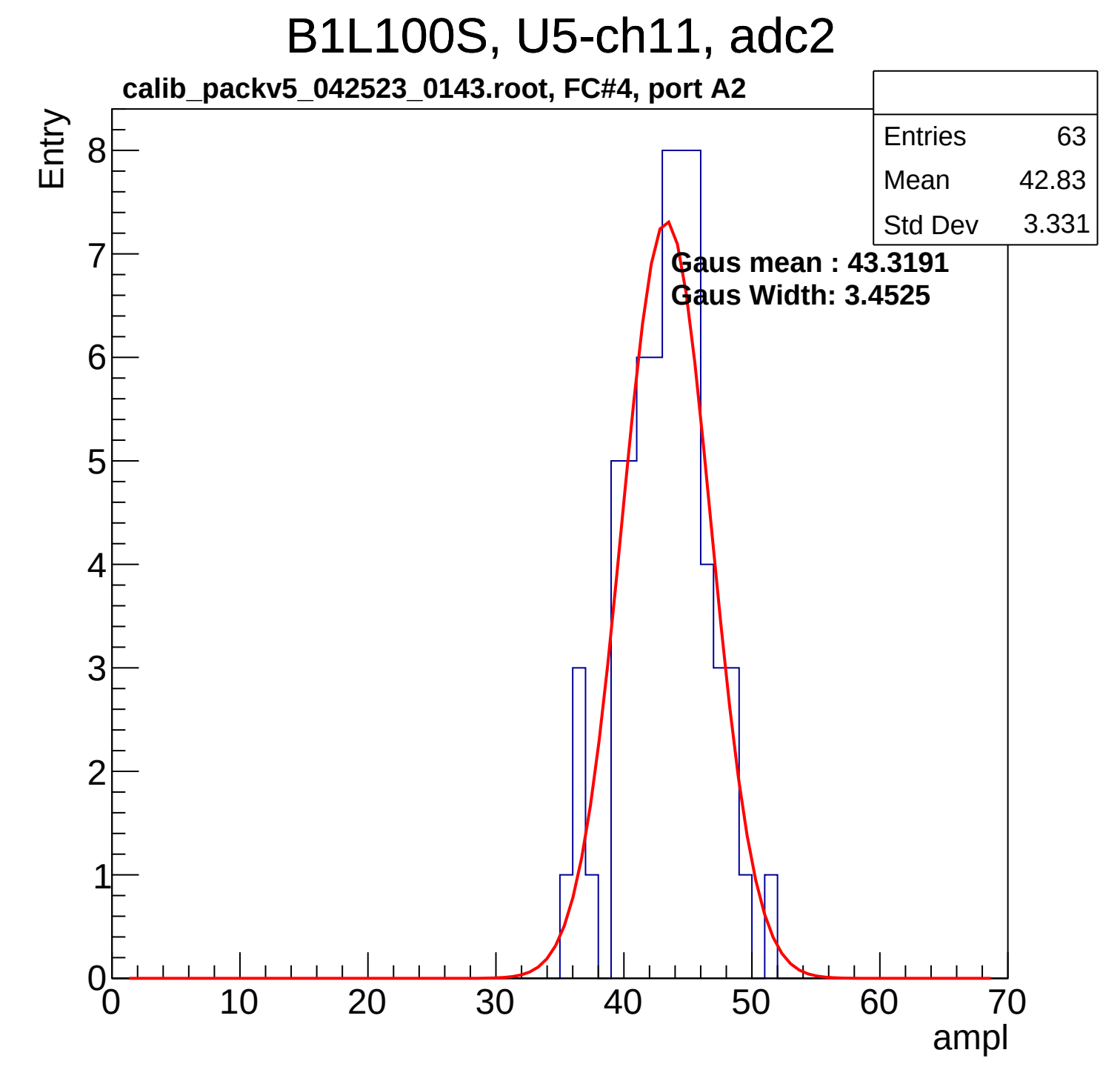
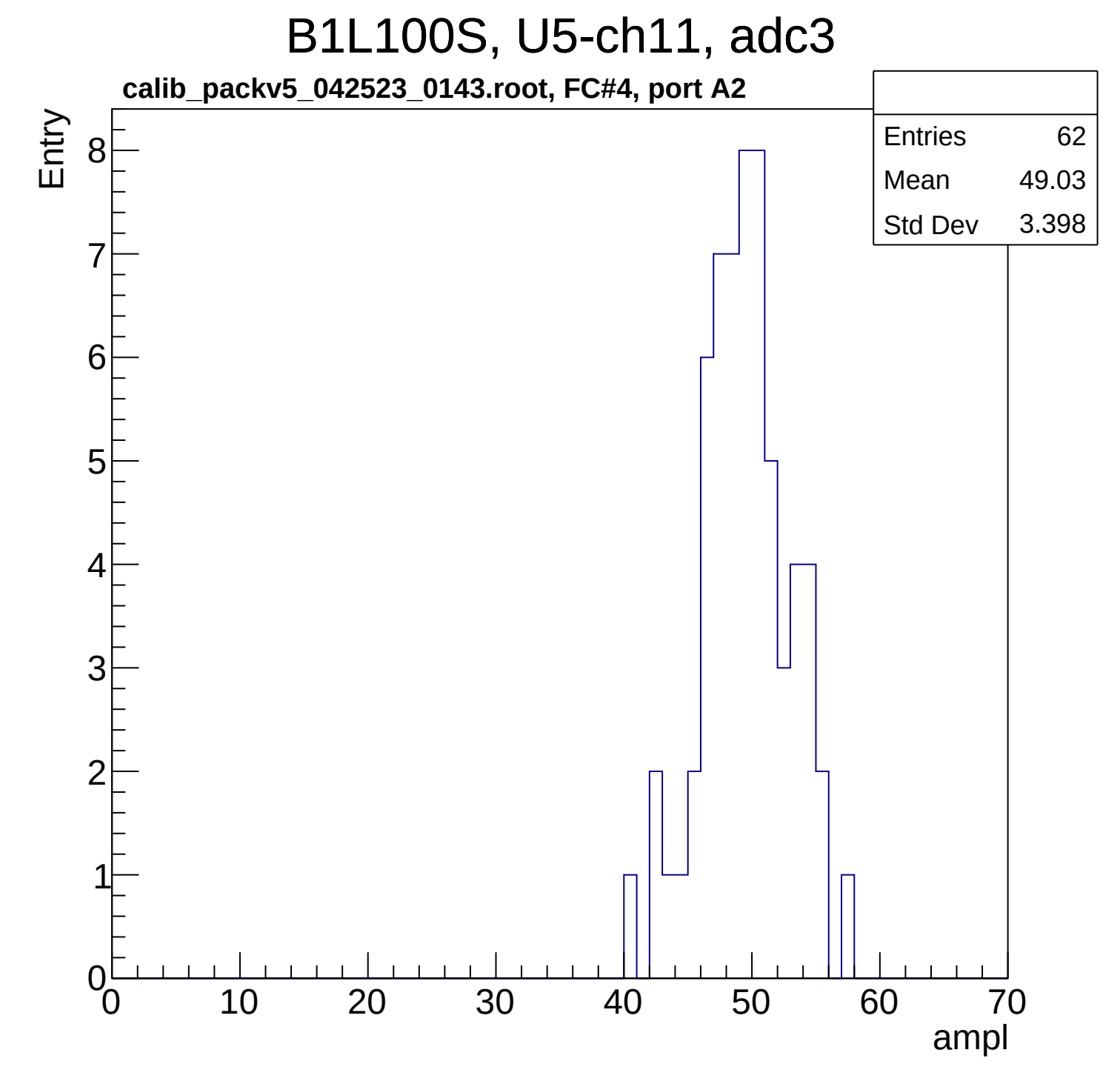
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch11, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 42.83
Std Dev 3.331
Gaus mean : 43.3191
Gaus Width: 3.4525
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch11, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 49.03
Std Dev 3.398
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
30
40
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60
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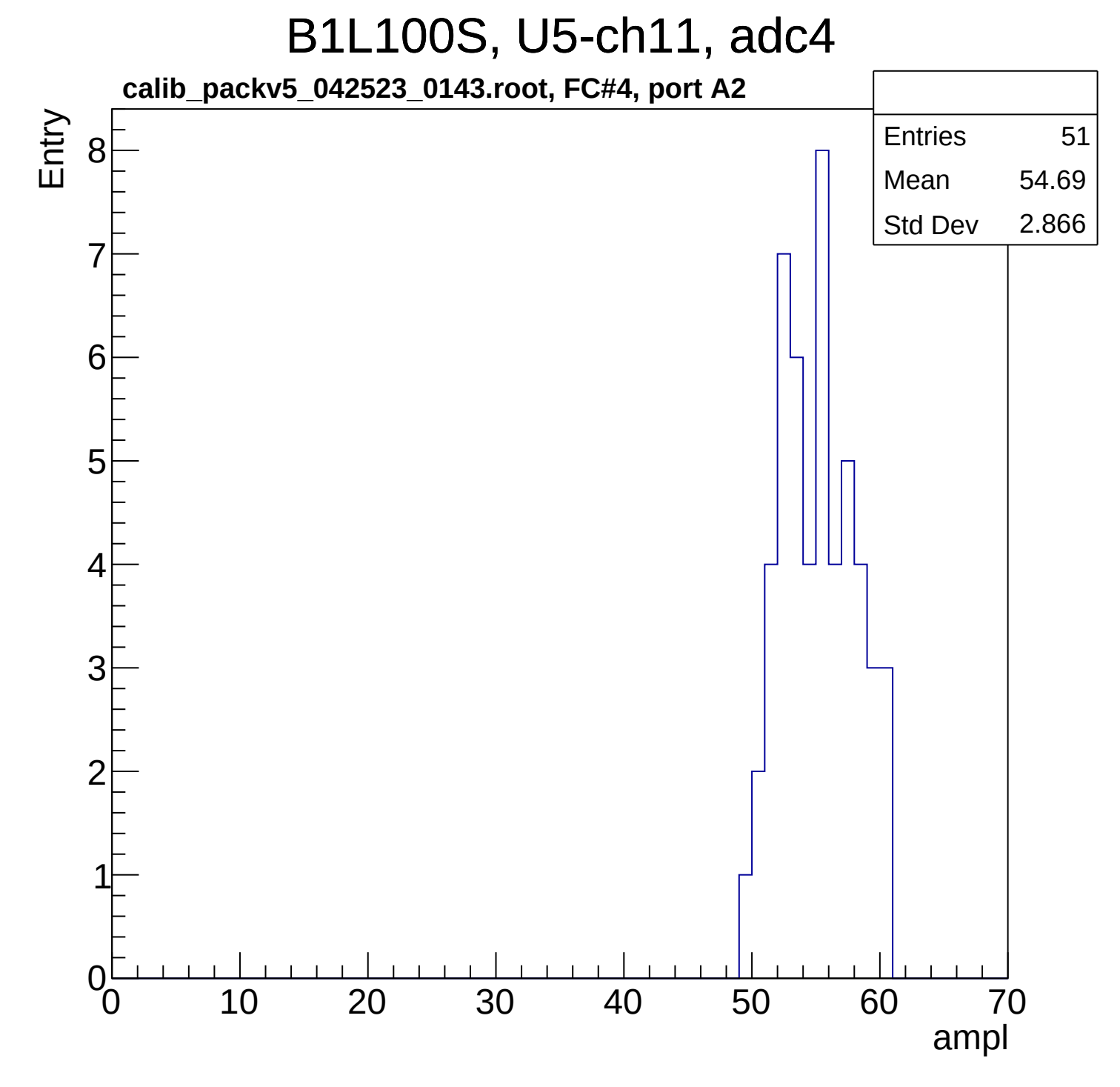
B1L100S, U5-ch11, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 54.69
Std Dev 2.866
Entry
ampl
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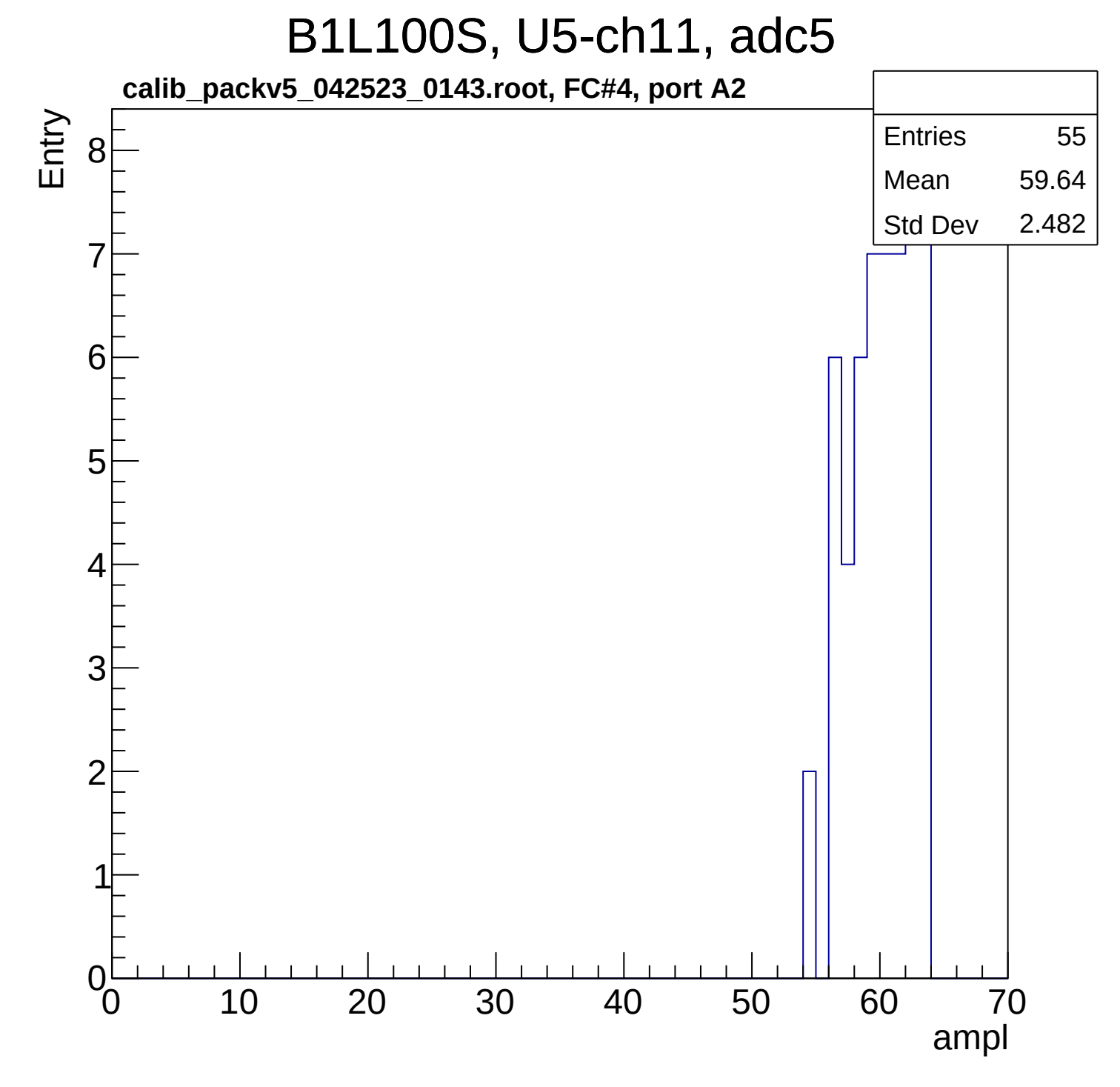
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch11, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 59.64
Std Dev 2.482
Entry
ampl
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1
2
3
4
5
6
7
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0
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40
50
60
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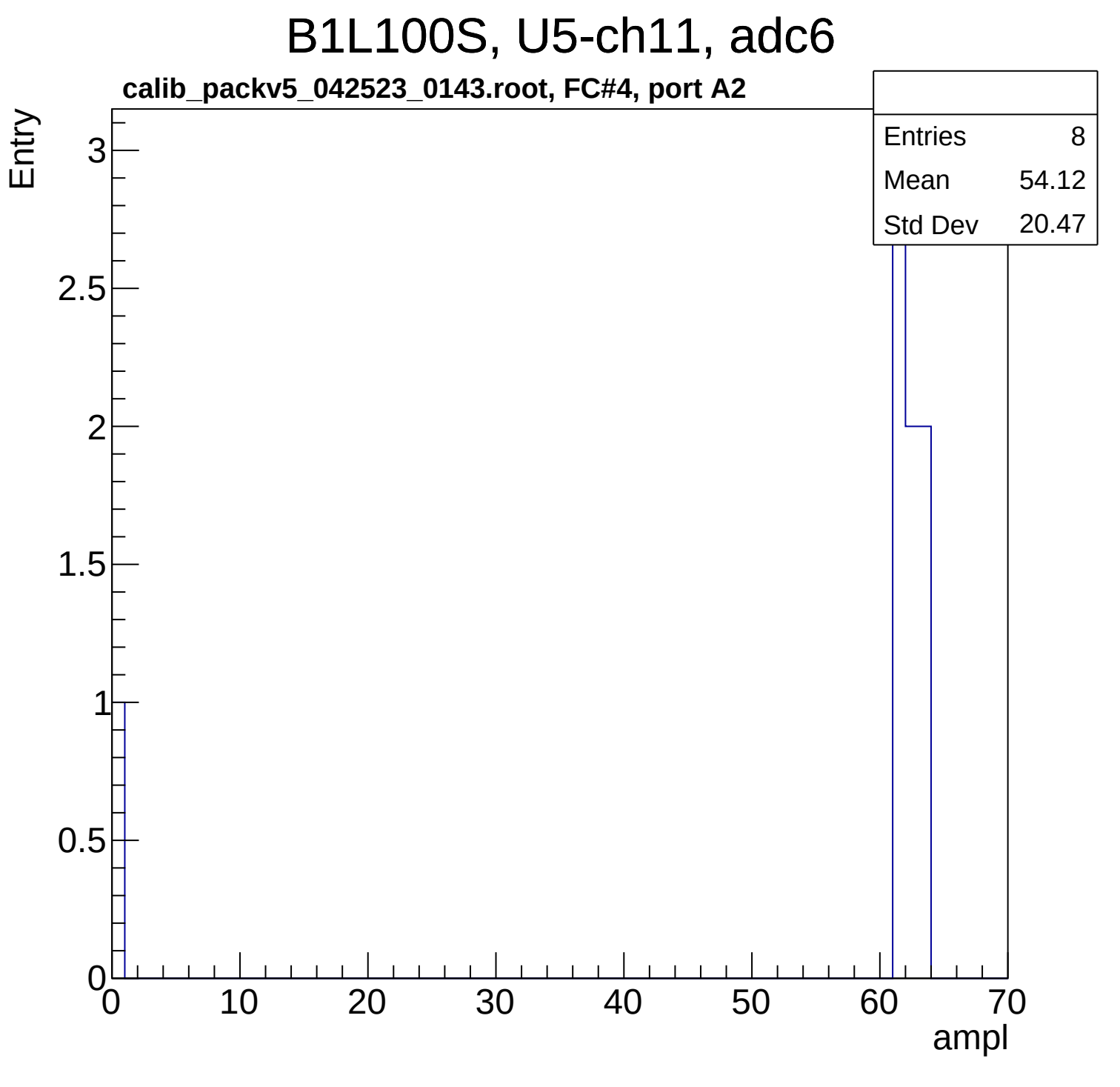
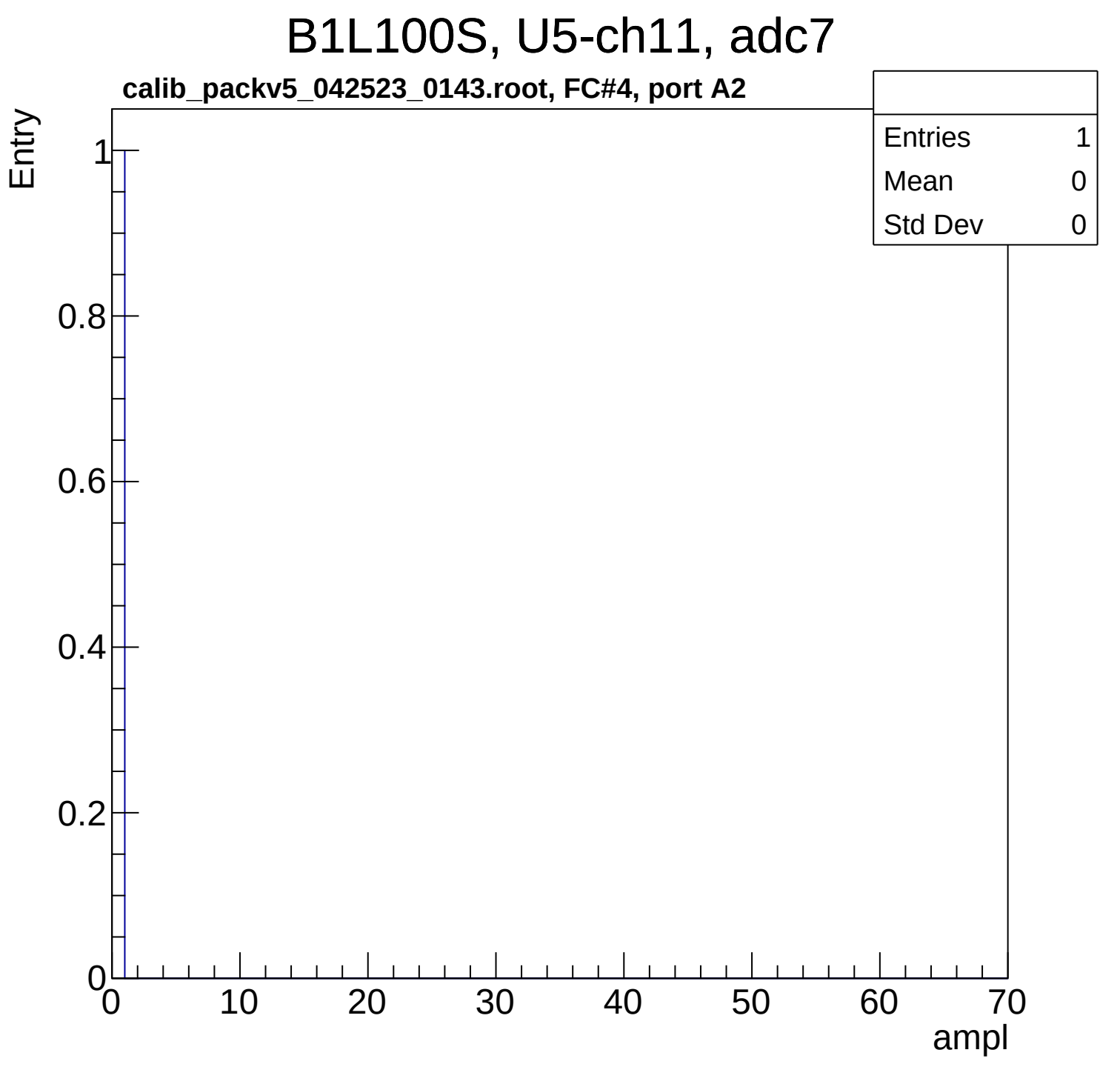
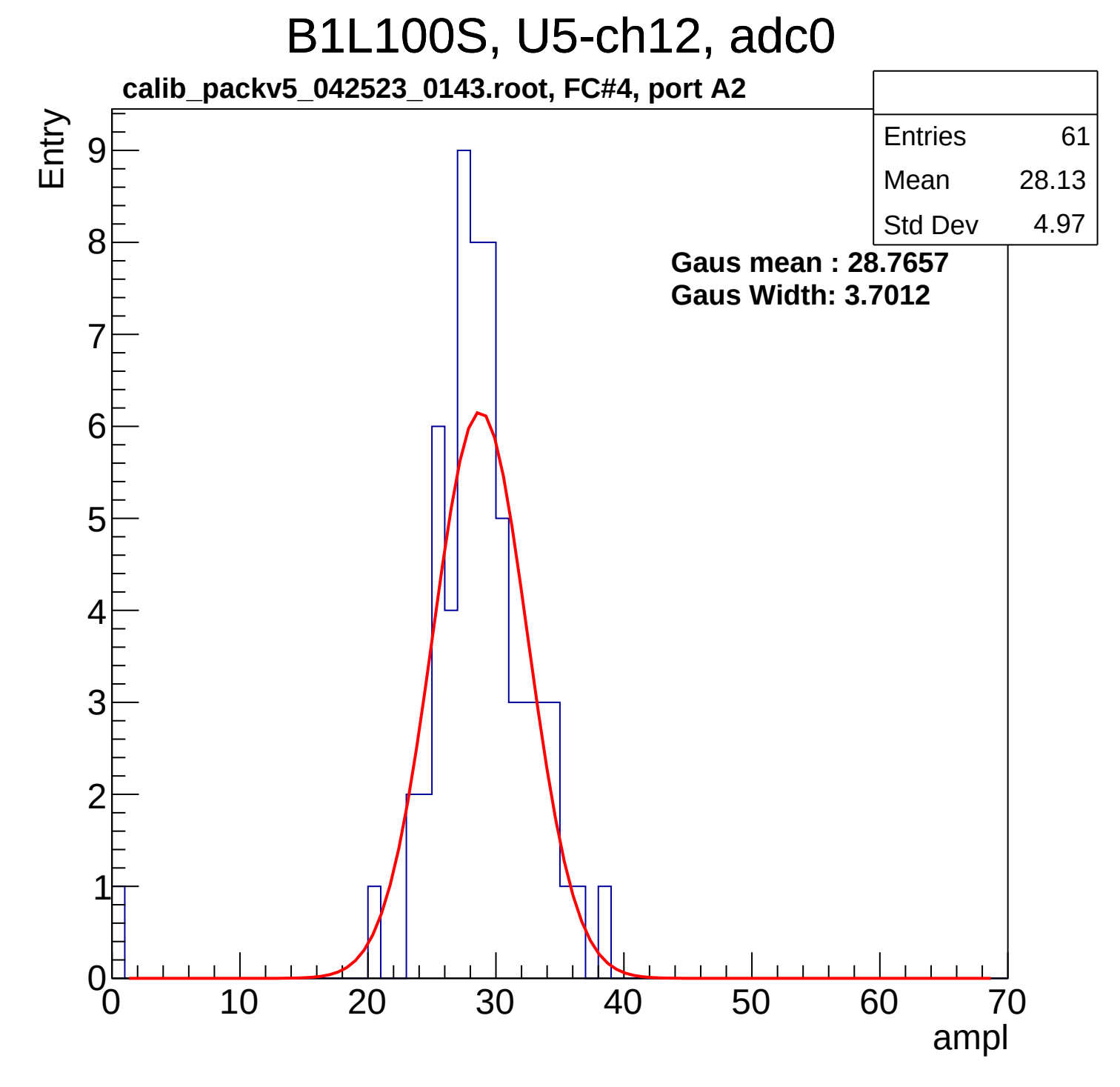
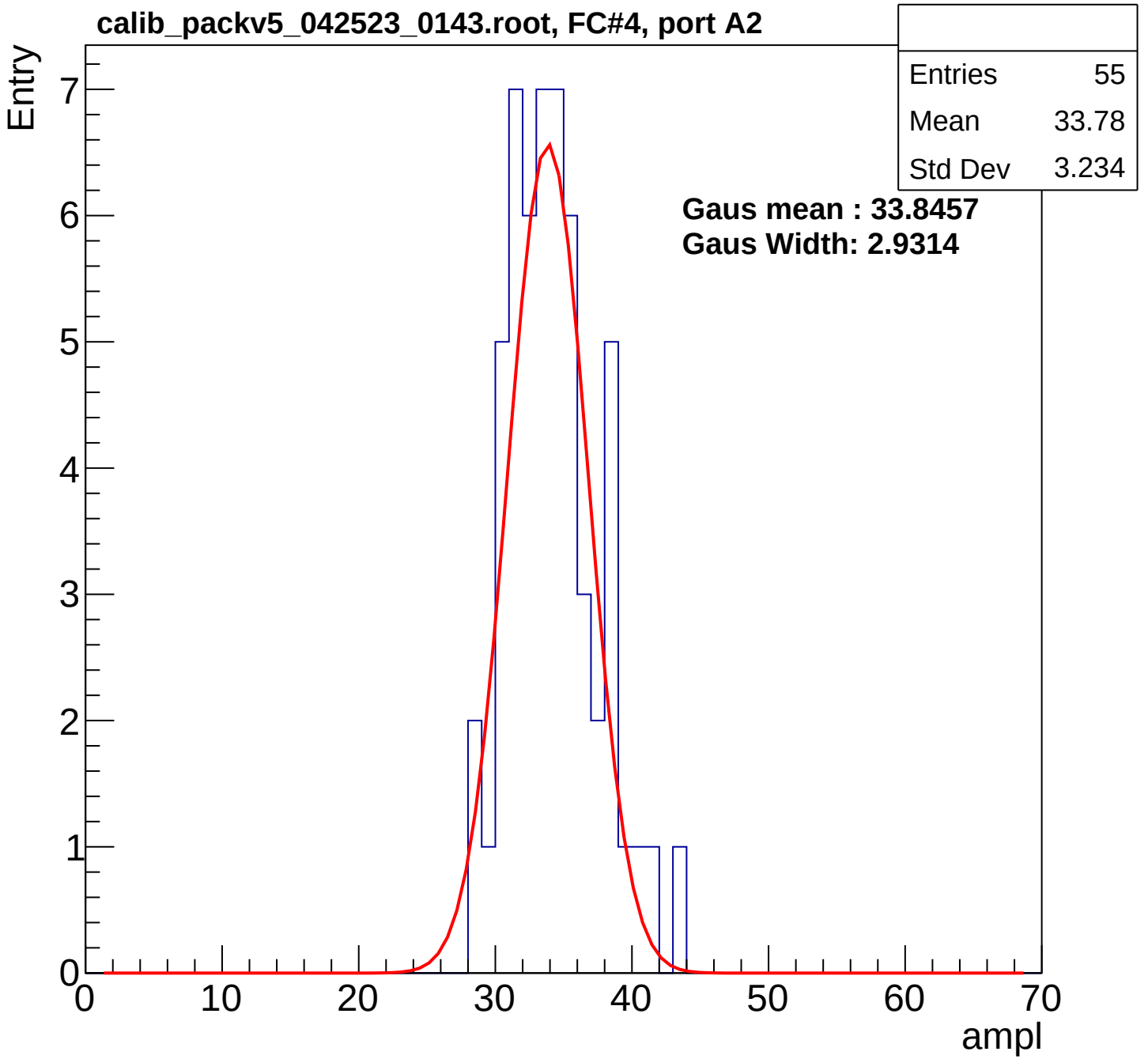
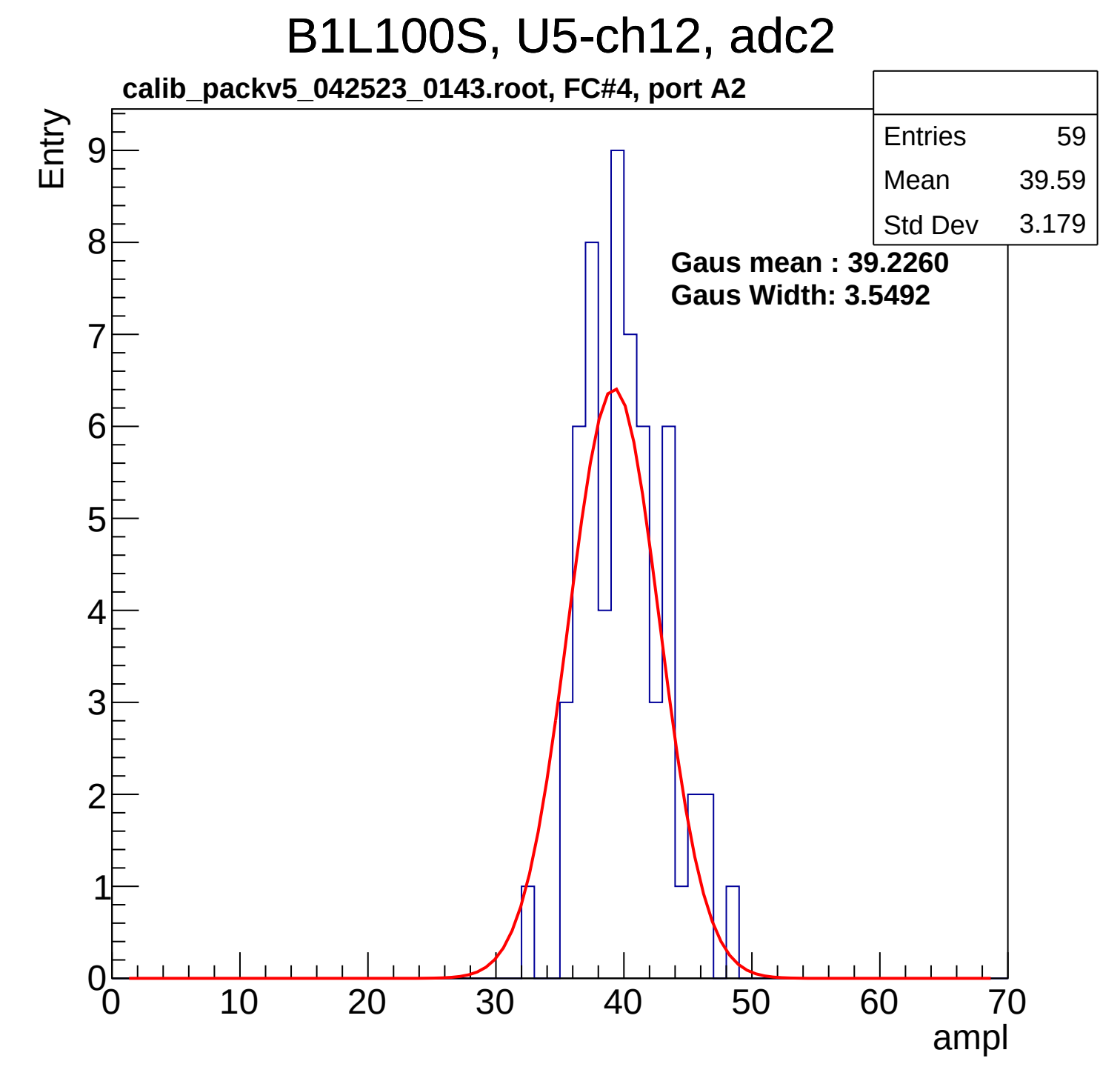
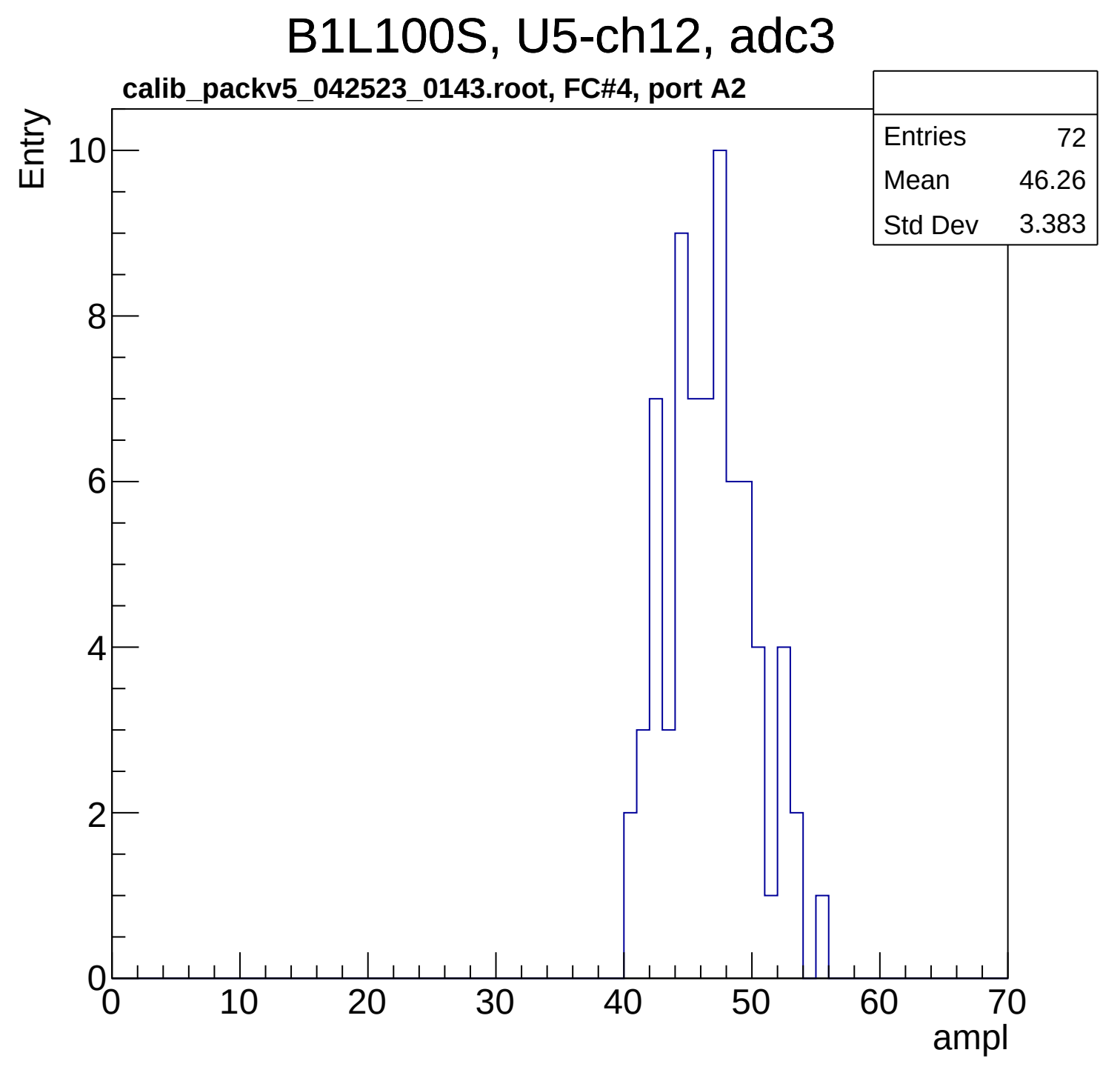

B1L100S, U5-ch11, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 8
Mean 54.12
Std Dev 20.47
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

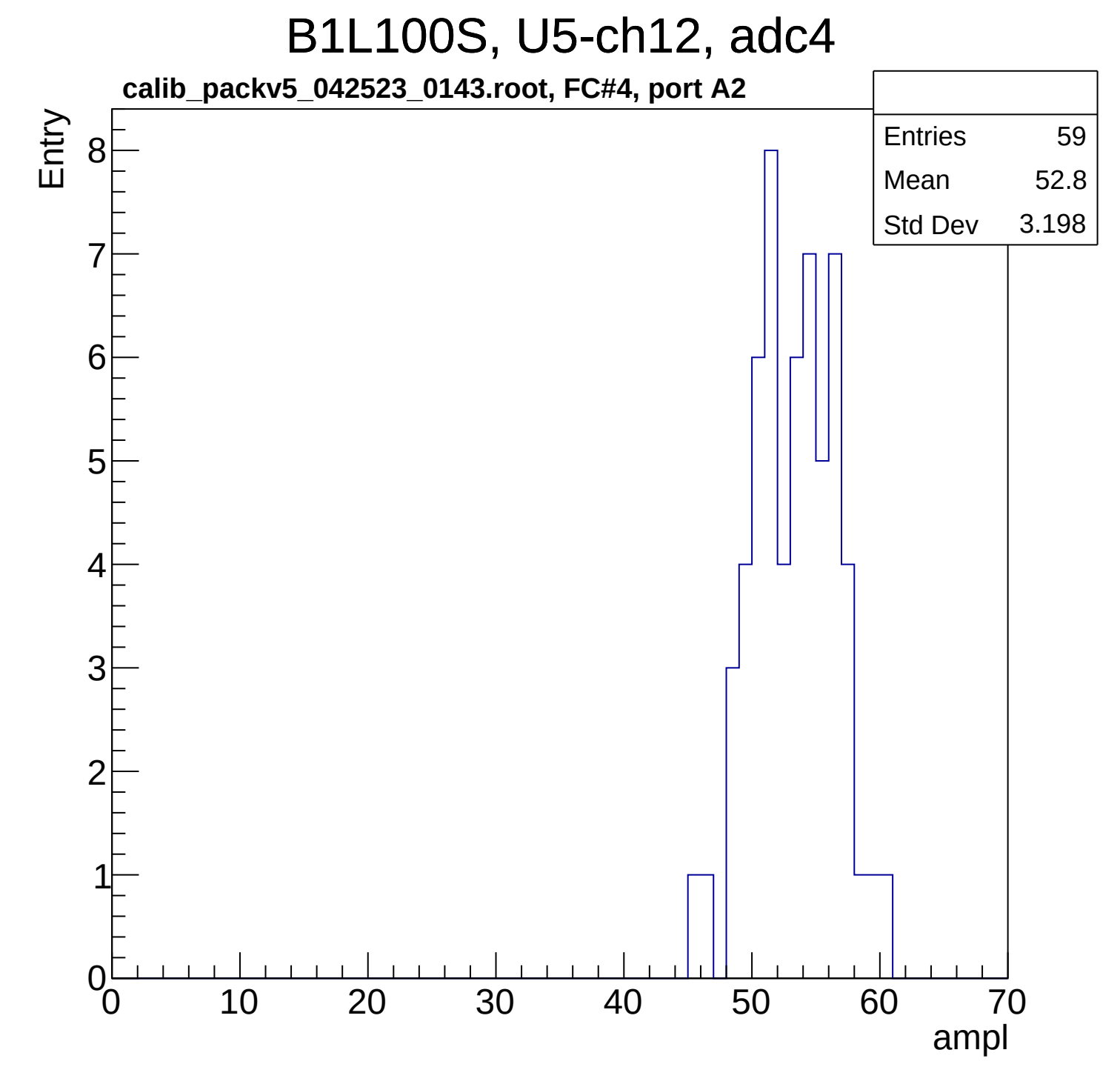

B1L100S, U5-ch11, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

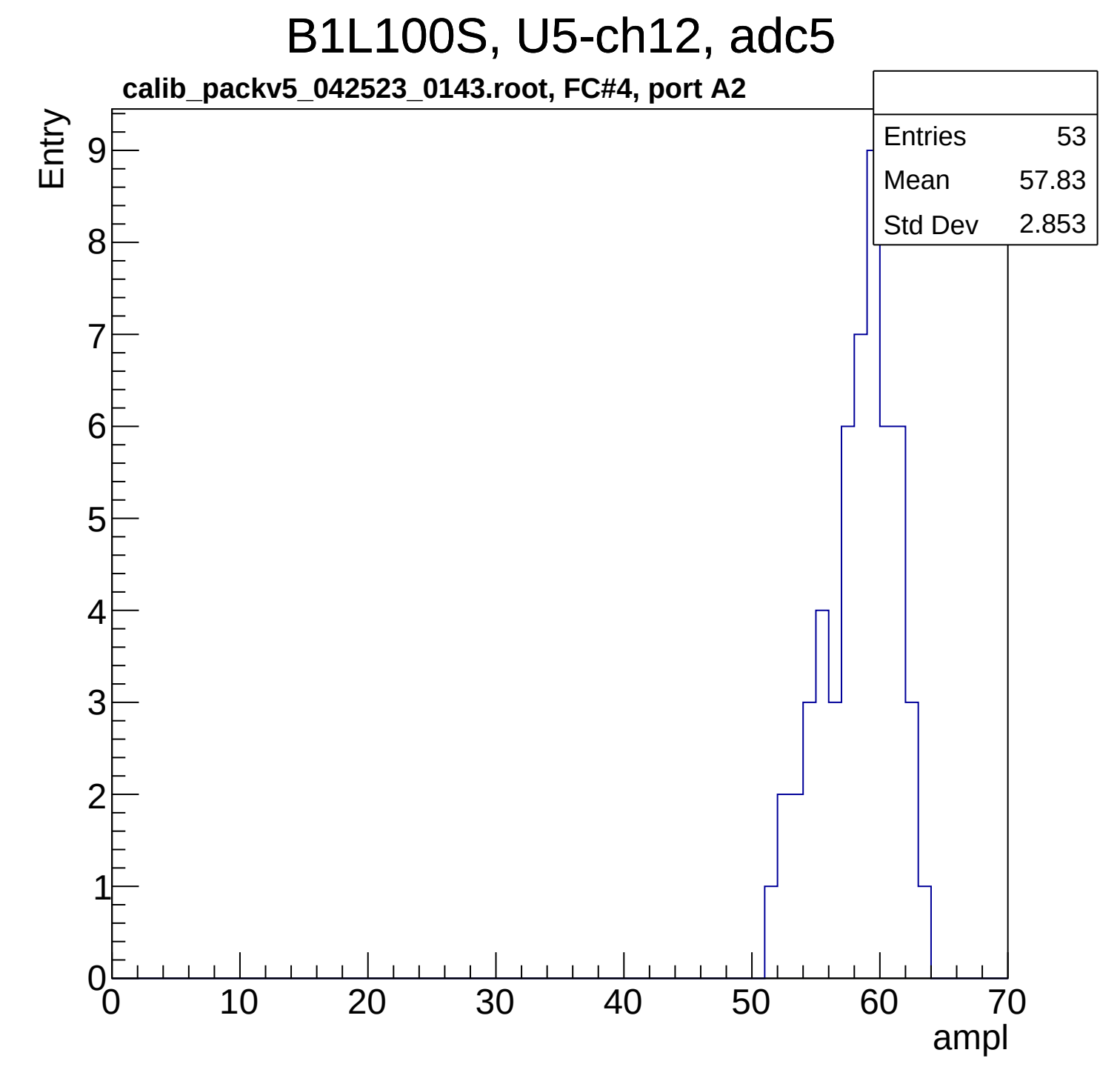

B1L100S, U5-ch12, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 28.13
Std Dev 4.97
Gaus mean : 28.7657
Gaus Width: 3.7012
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch12, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 33.78
Std Dev 3.234
Gaus mean : 33.8457
Gaus Width: 2.9314
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U5-ch12, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 39.59
Std Dev 3.179
Gaus mean : 39.2260
Gaus Width: 3.5492
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch12, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 46.26
Std Dev 3.383
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch12, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 52.8
Std Dev 3.198
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch12, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 57.83
Std Dev 2.853
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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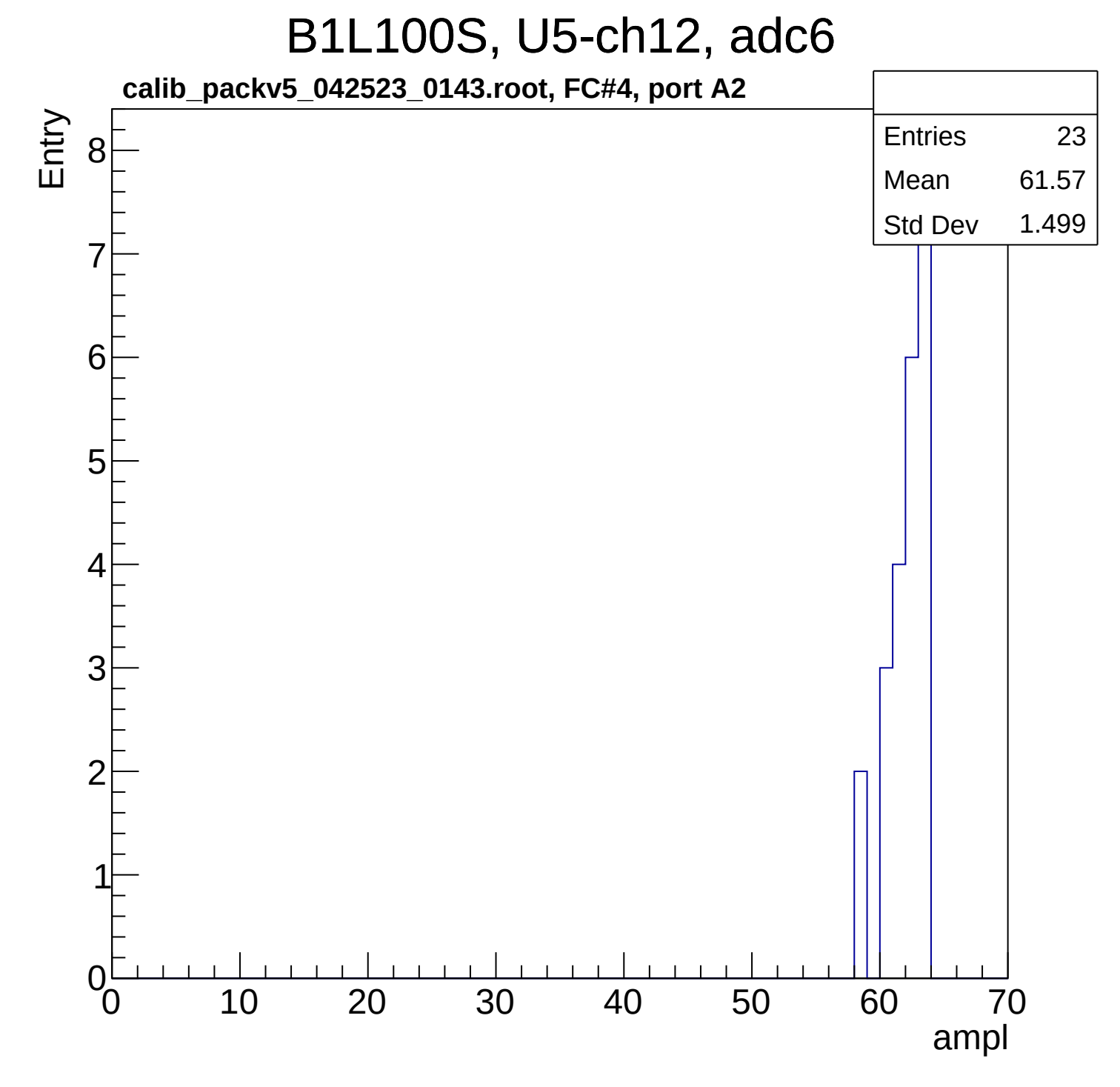
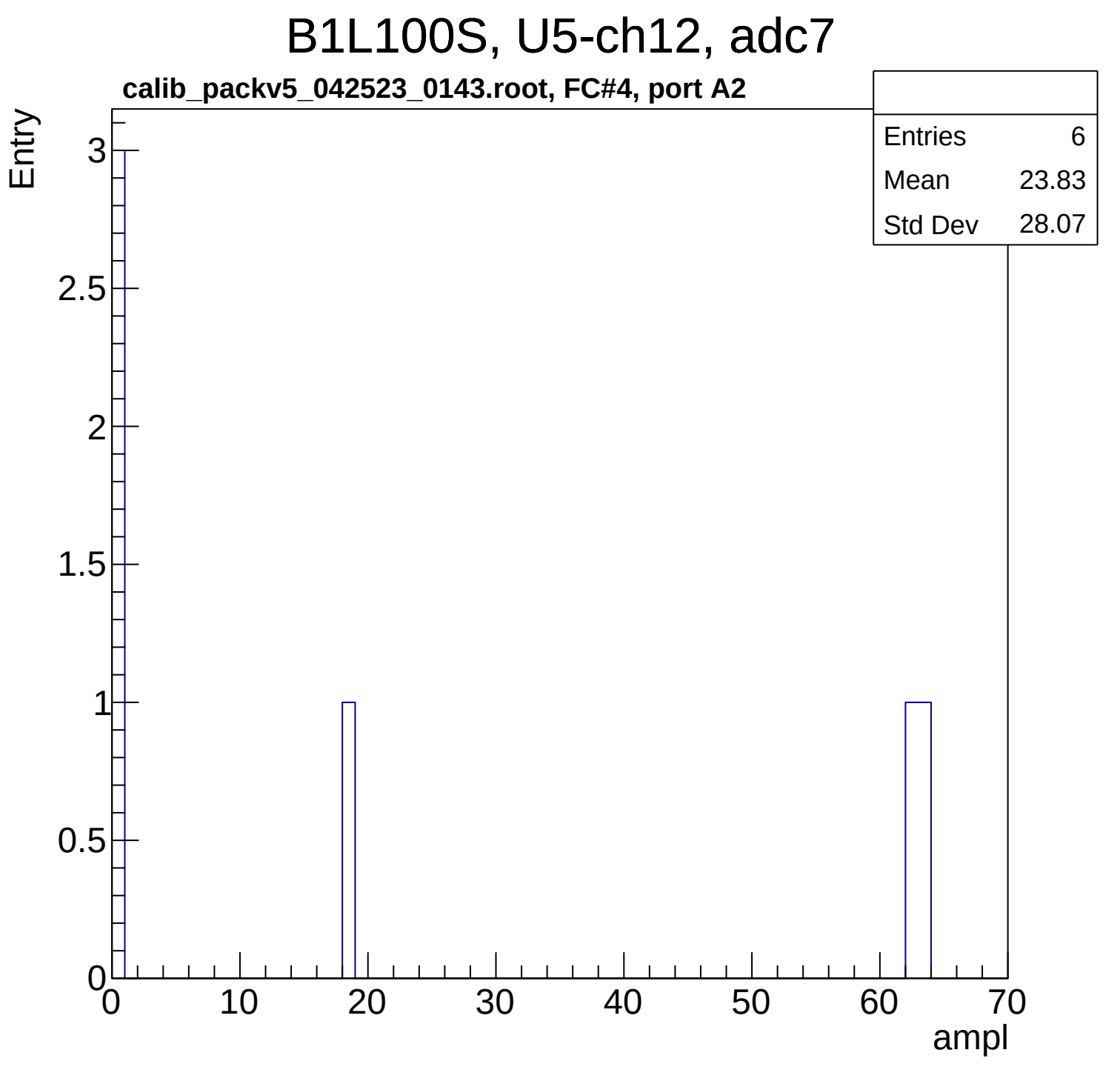
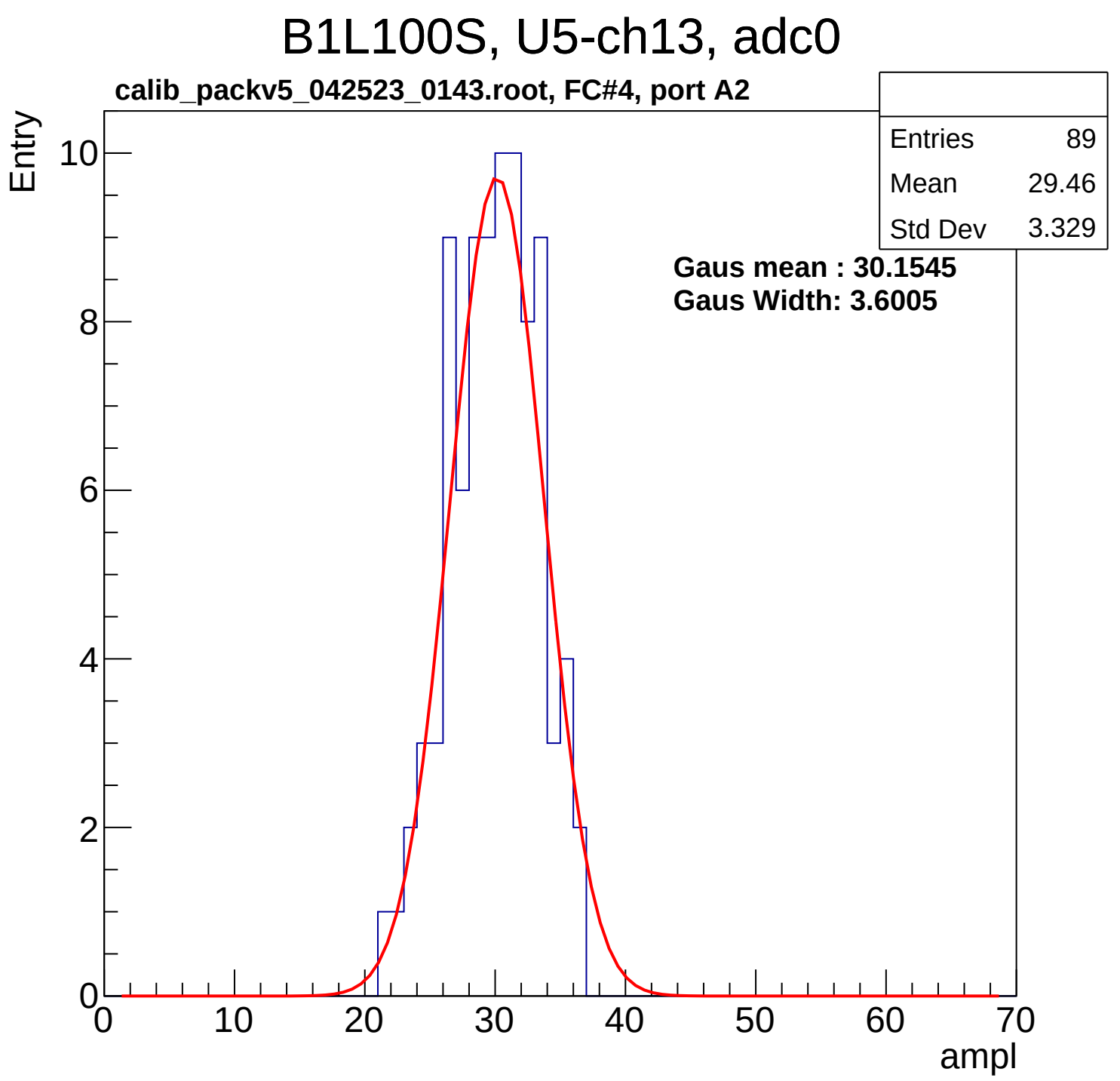
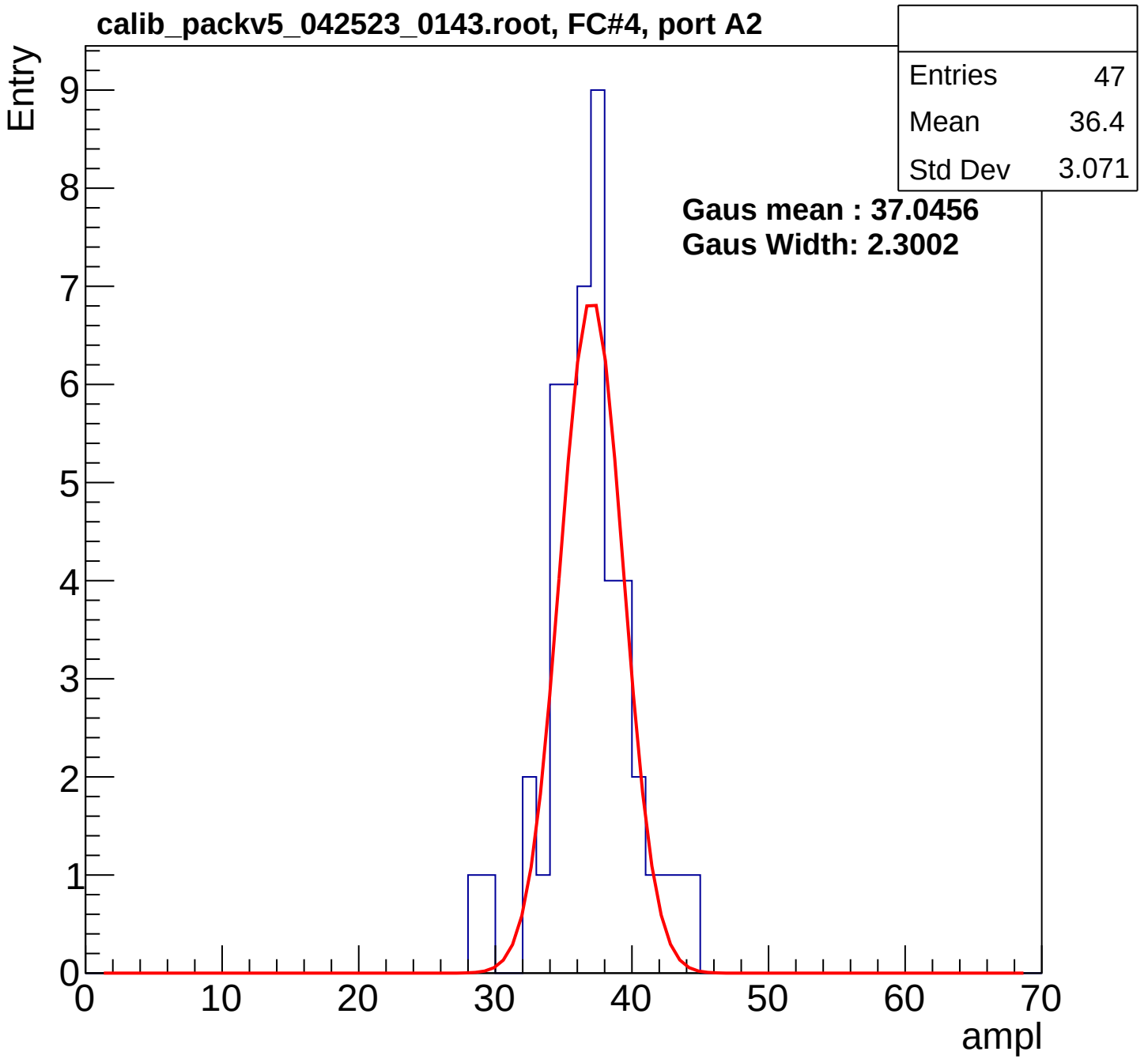
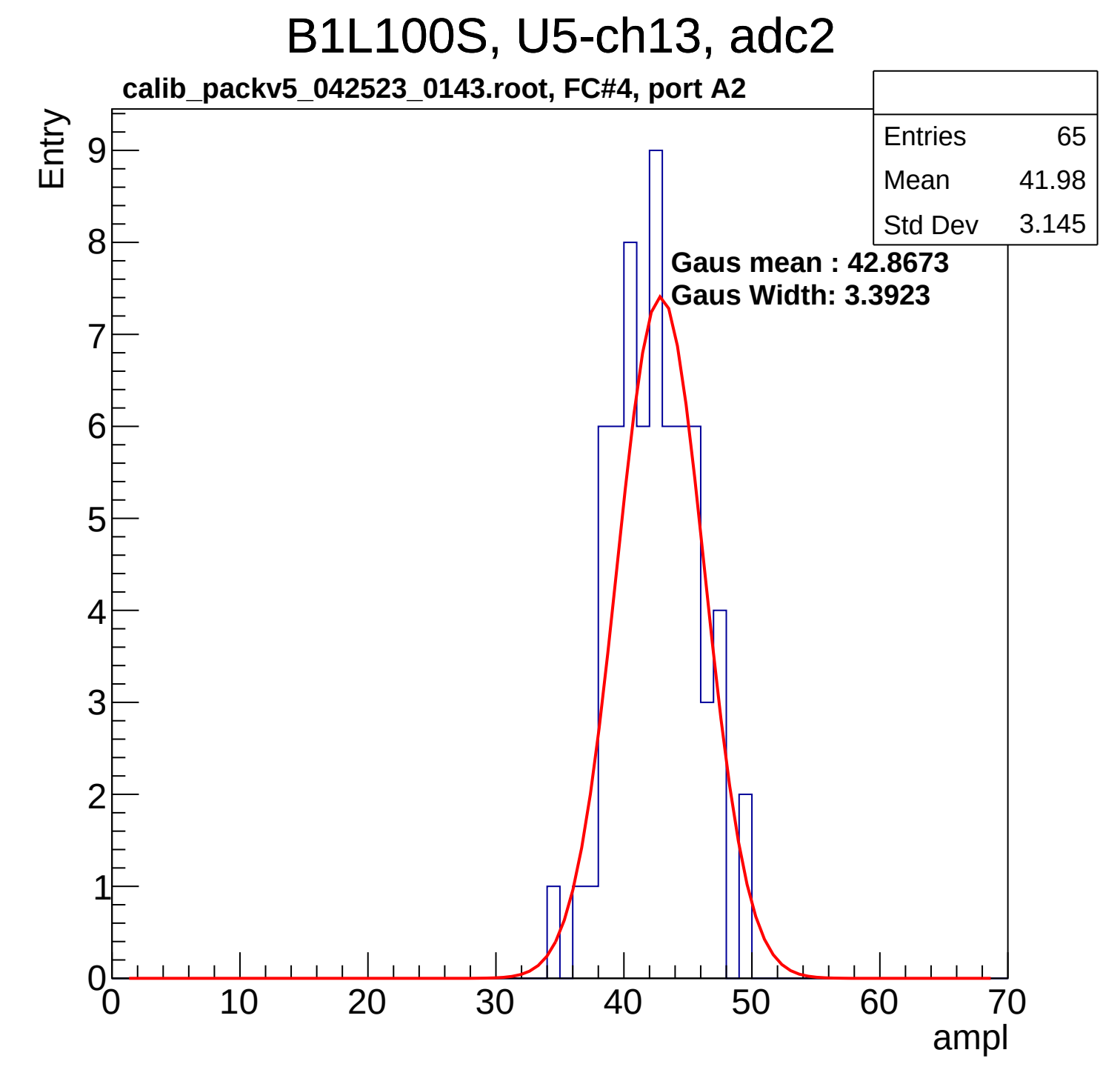
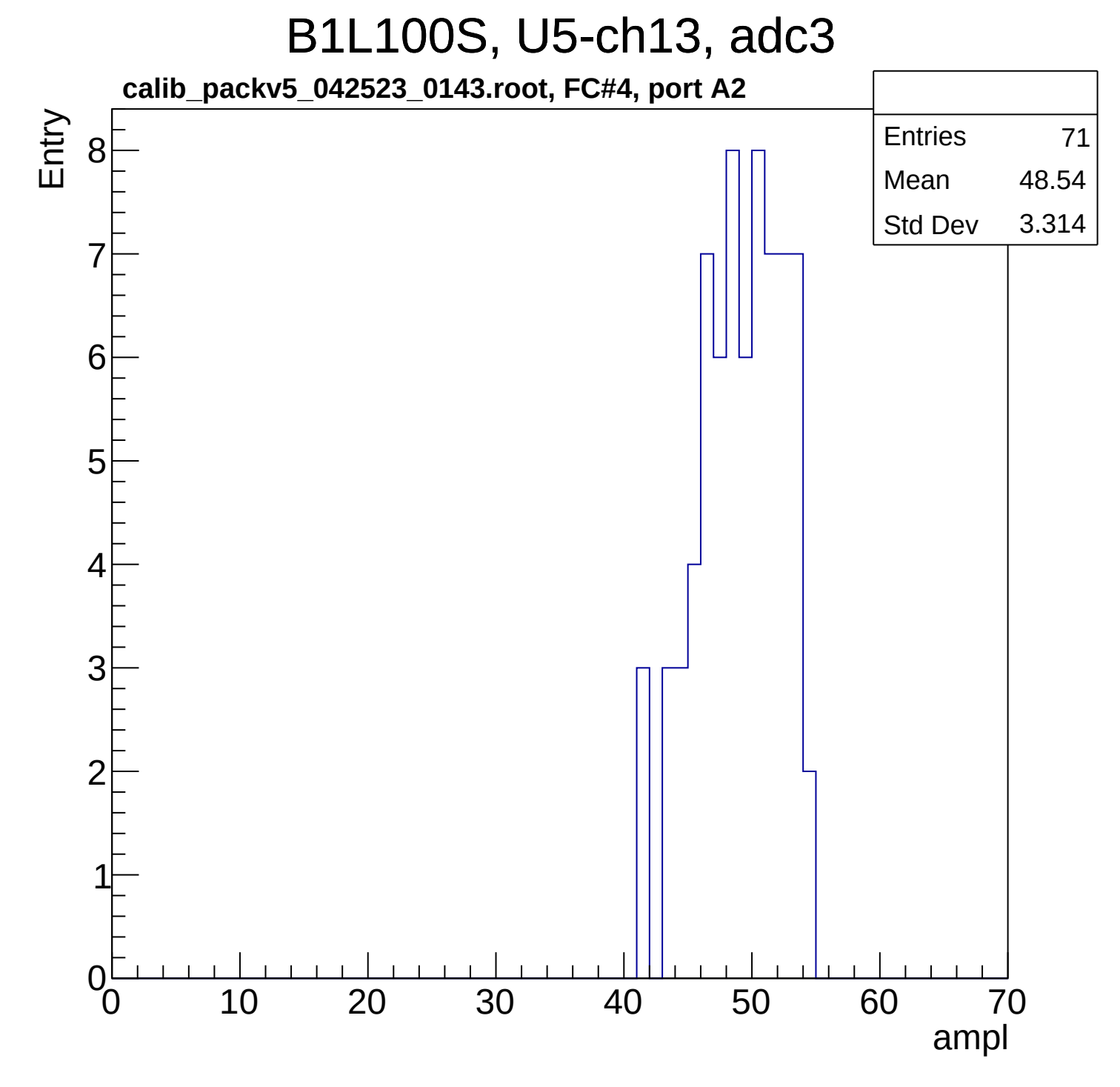

B1L100S, U5-ch12, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 23
Mean 61.57
Std Dev 1.499
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch12, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 6
Mean 23.83
Std Dev 28.07
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L100S, U5-ch13, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 89
Mean 29.46
Std Dev 3.329
Gaus mean : 30.1545
Gaus Width: 3.6005
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch13, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 47
Mean 36.4
Std Dev 3.071
Gaus mean : 37.0456
Gaus Width: 2.3002
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch13, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 41.98
Std Dev 3.145
Gaus mean : 42.8673
Gaus Width: 3.3923
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch13, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 48.54
Std Dev 3.314
Entry
ampl
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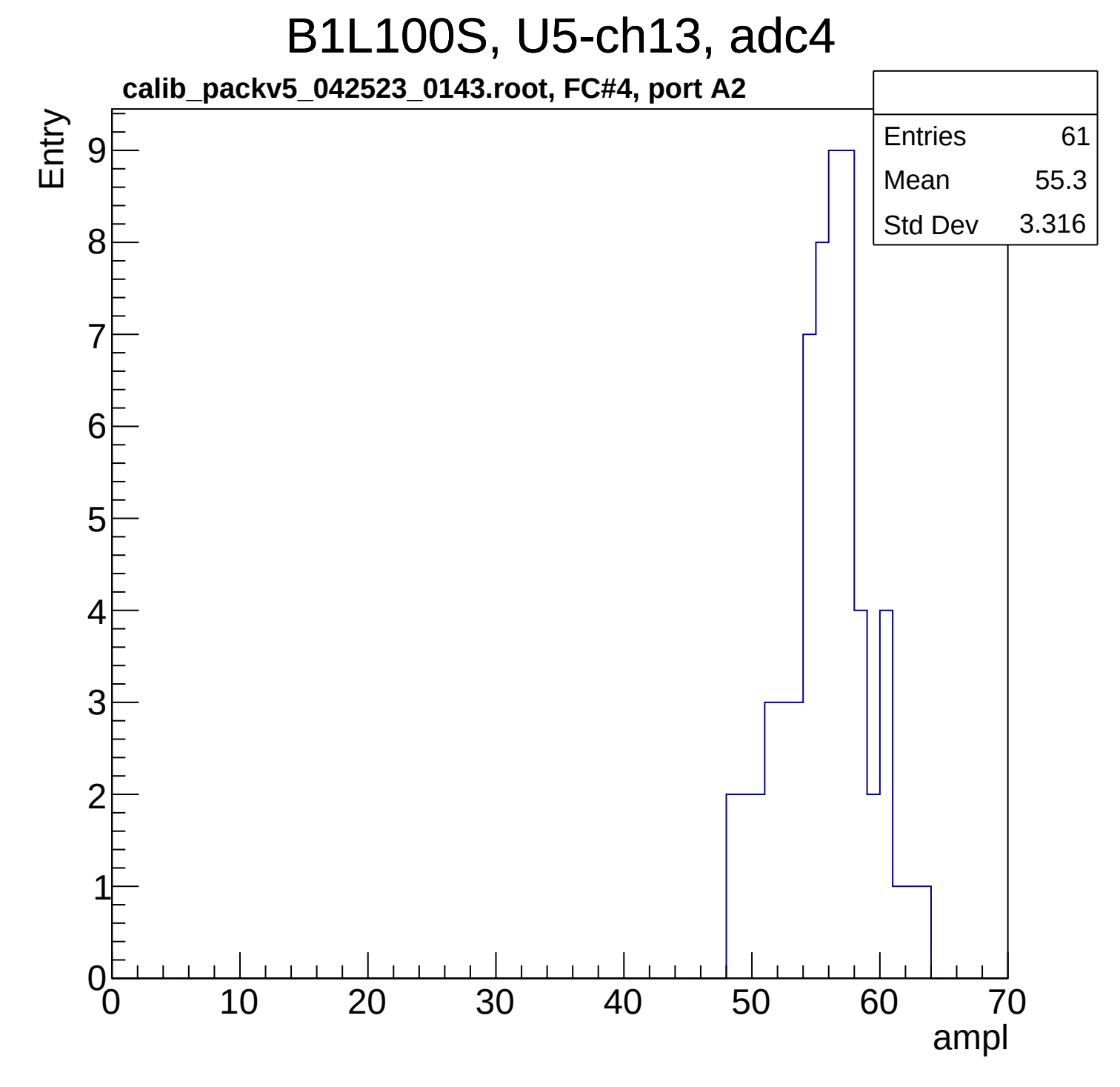
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch13, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 55.3
Std Dev 3.316
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
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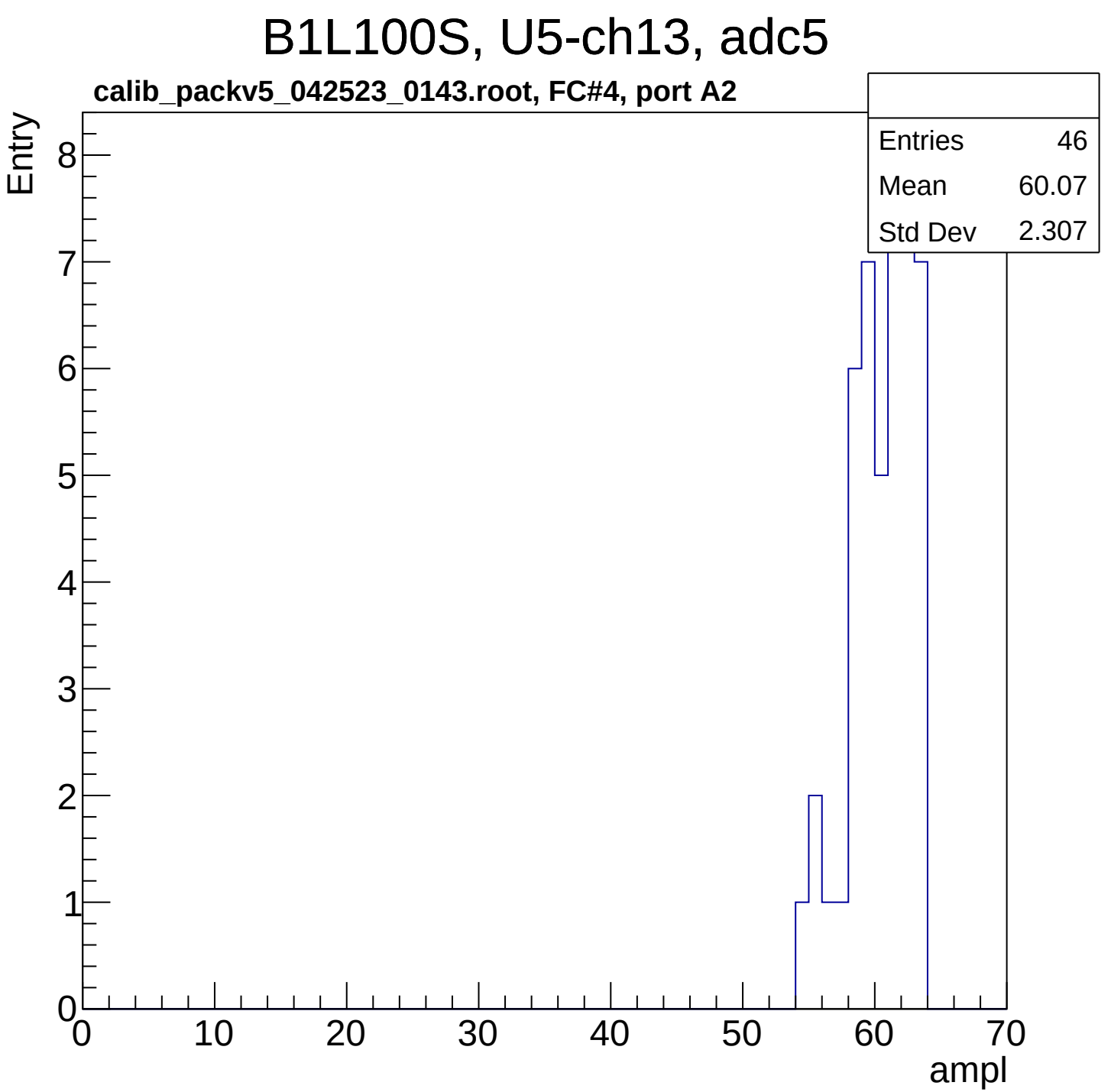
60
70


B1L100S, U5-ch13, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 46
Mean 60.07
Std Dev 2.307
Entry
ampl
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1
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3
4
5
6
7
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60
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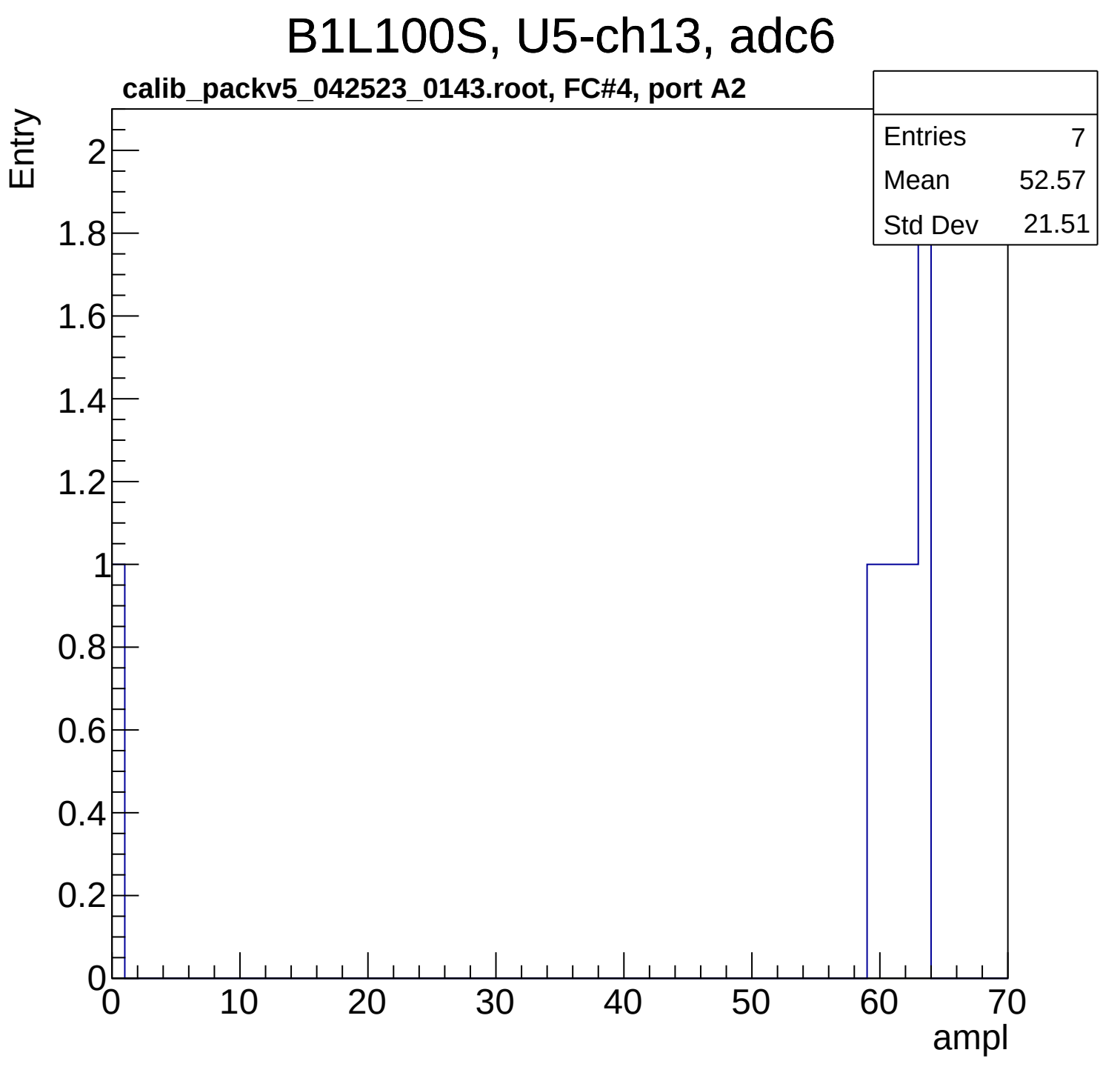
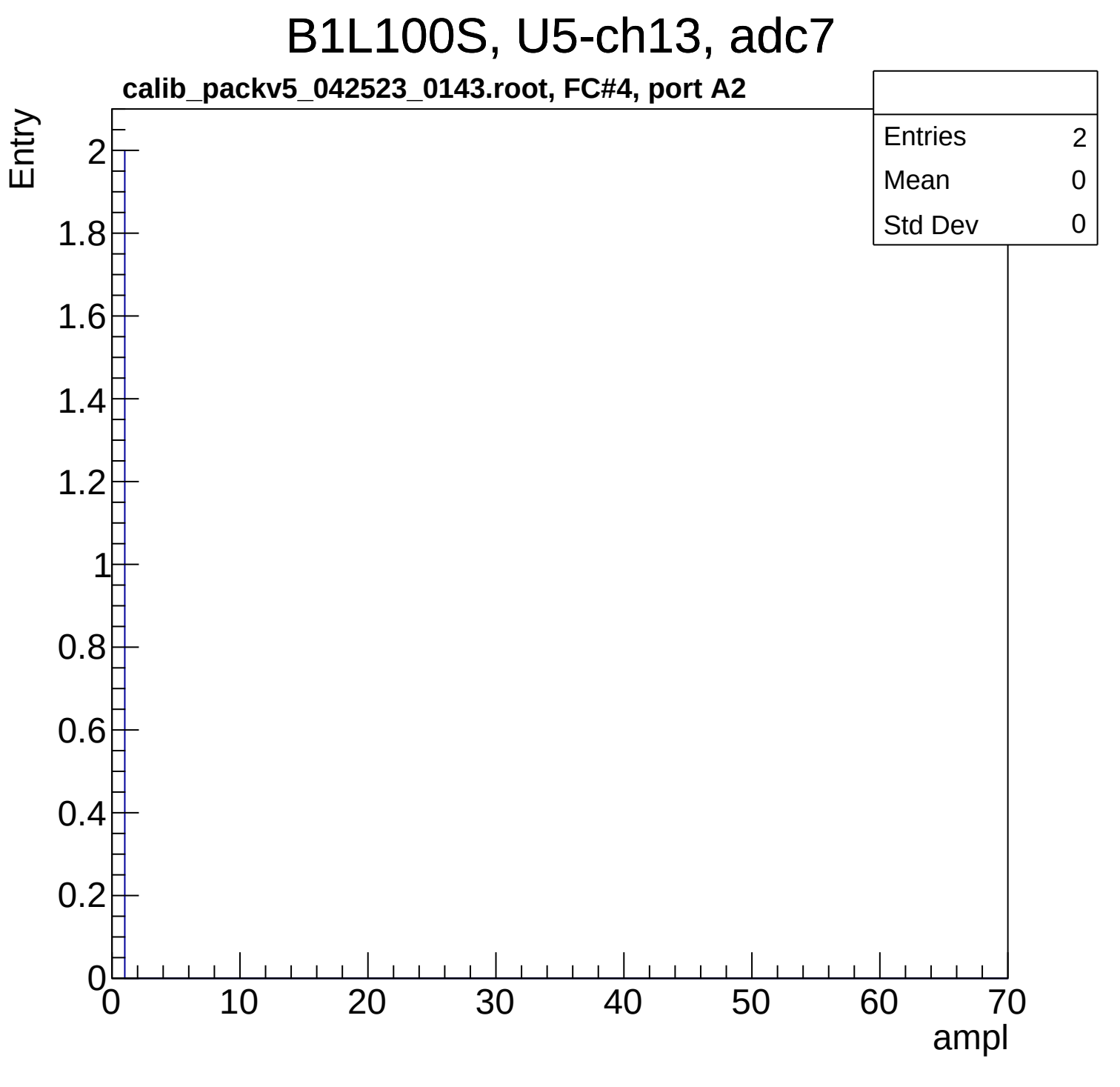
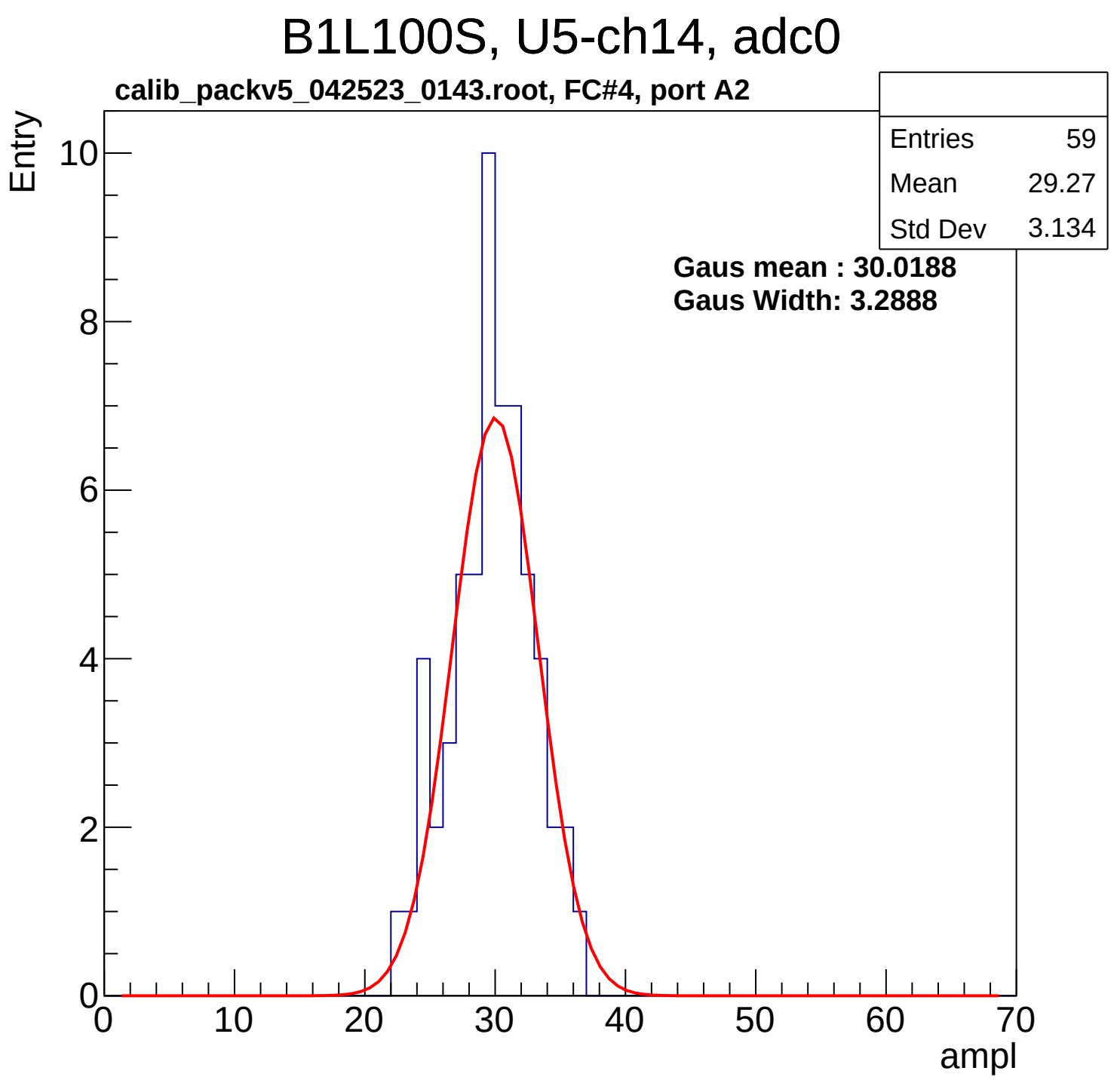
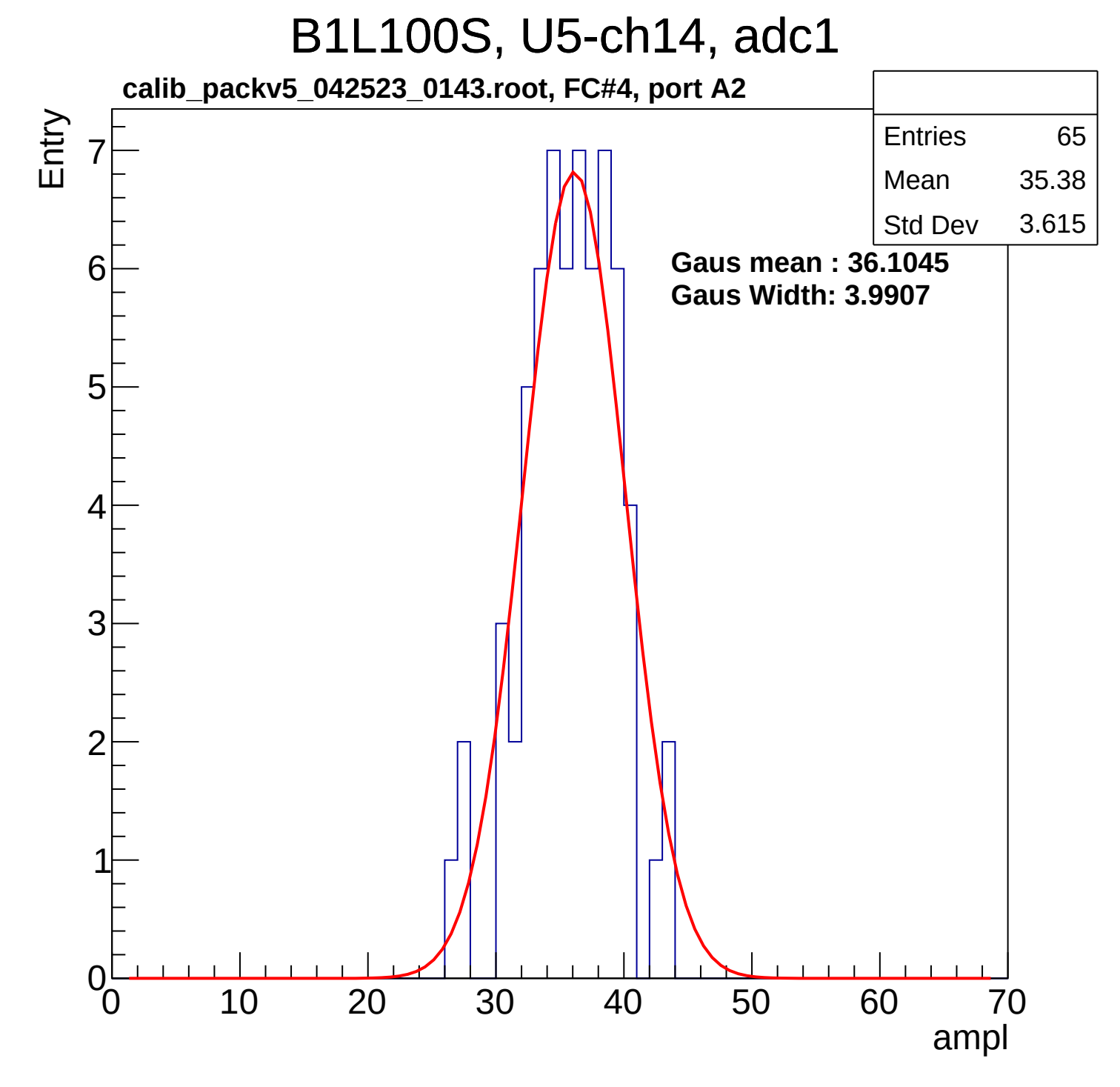
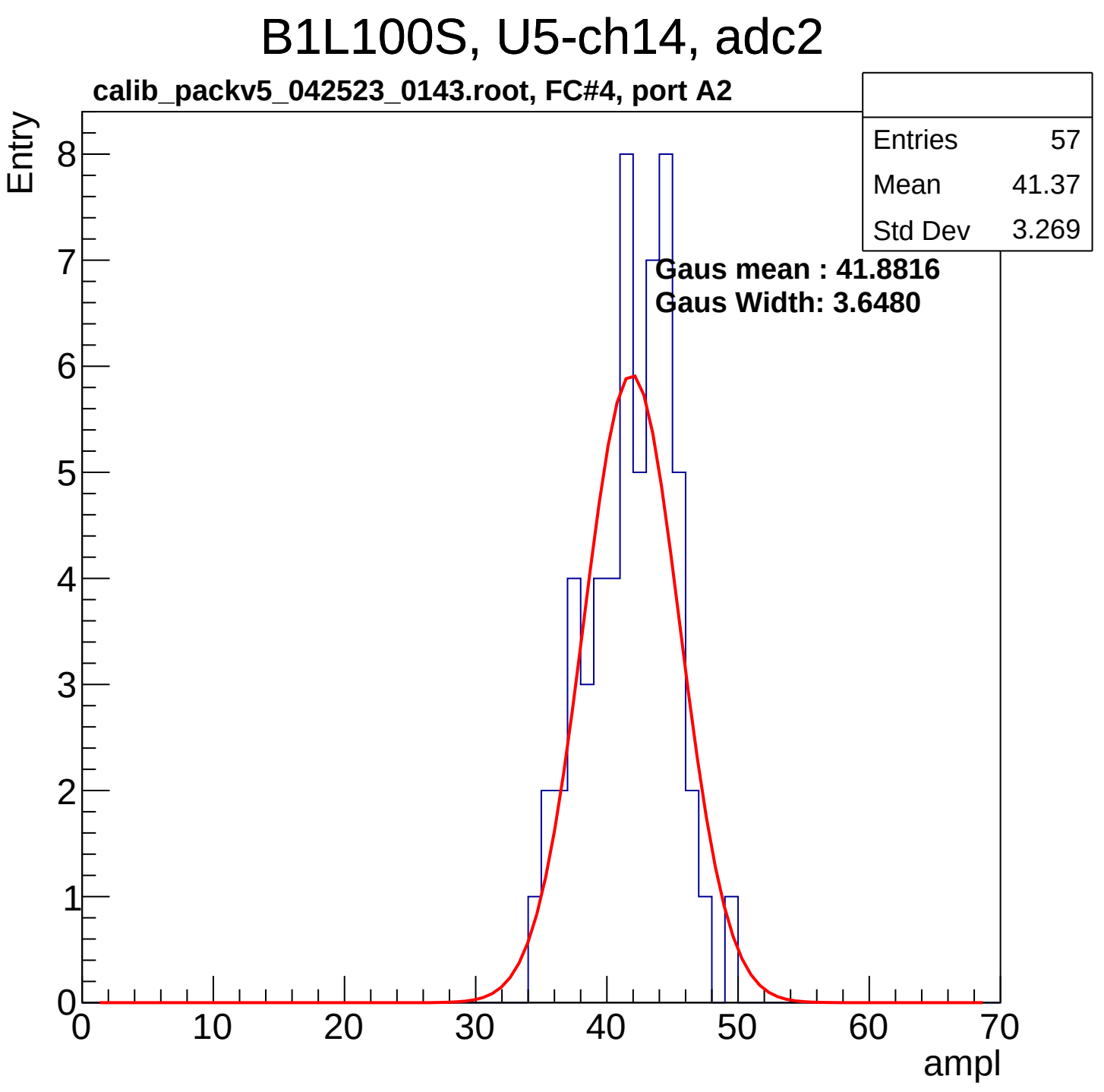

B1L100S, U5-ch13, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 7
Mean 52.57
Std Dev 21.51
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L100S, U5-ch13, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch14, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 29.27
Std Dev 3.134
Gaus mean : 30.0188
Gaus Width: 3.2888
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch14, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 35.38
Std Dev 3.615
Gaus mean : 36.1045
Gaus Width: 3.9907
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U5-ch14, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 41.37
Std Dev 3.269
Gaus mean : 41.8816
Gaus Width: 3.6480
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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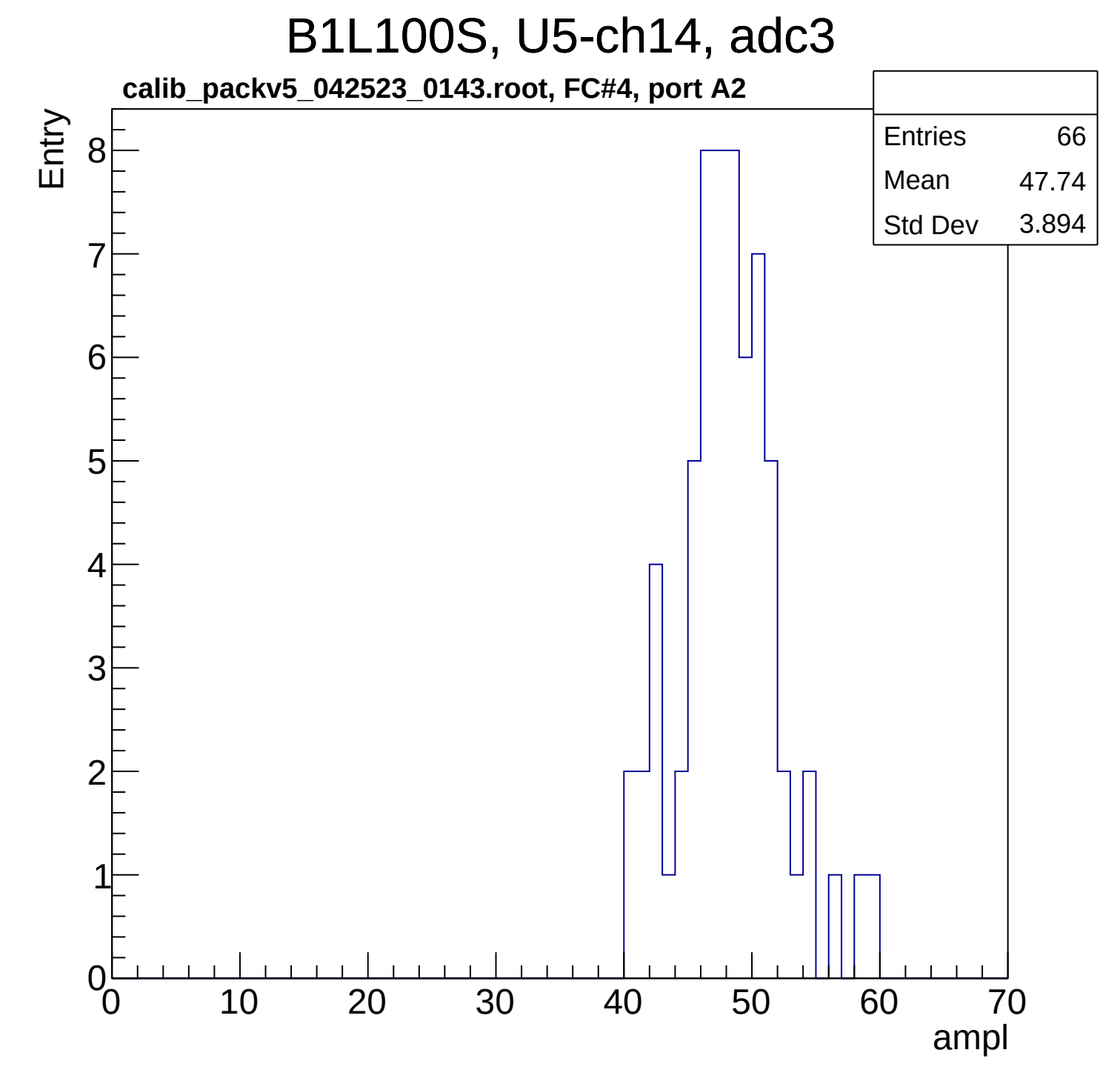
50
60
70


B1L100S, U5-ch14, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 47.74
Std Dev 3.894
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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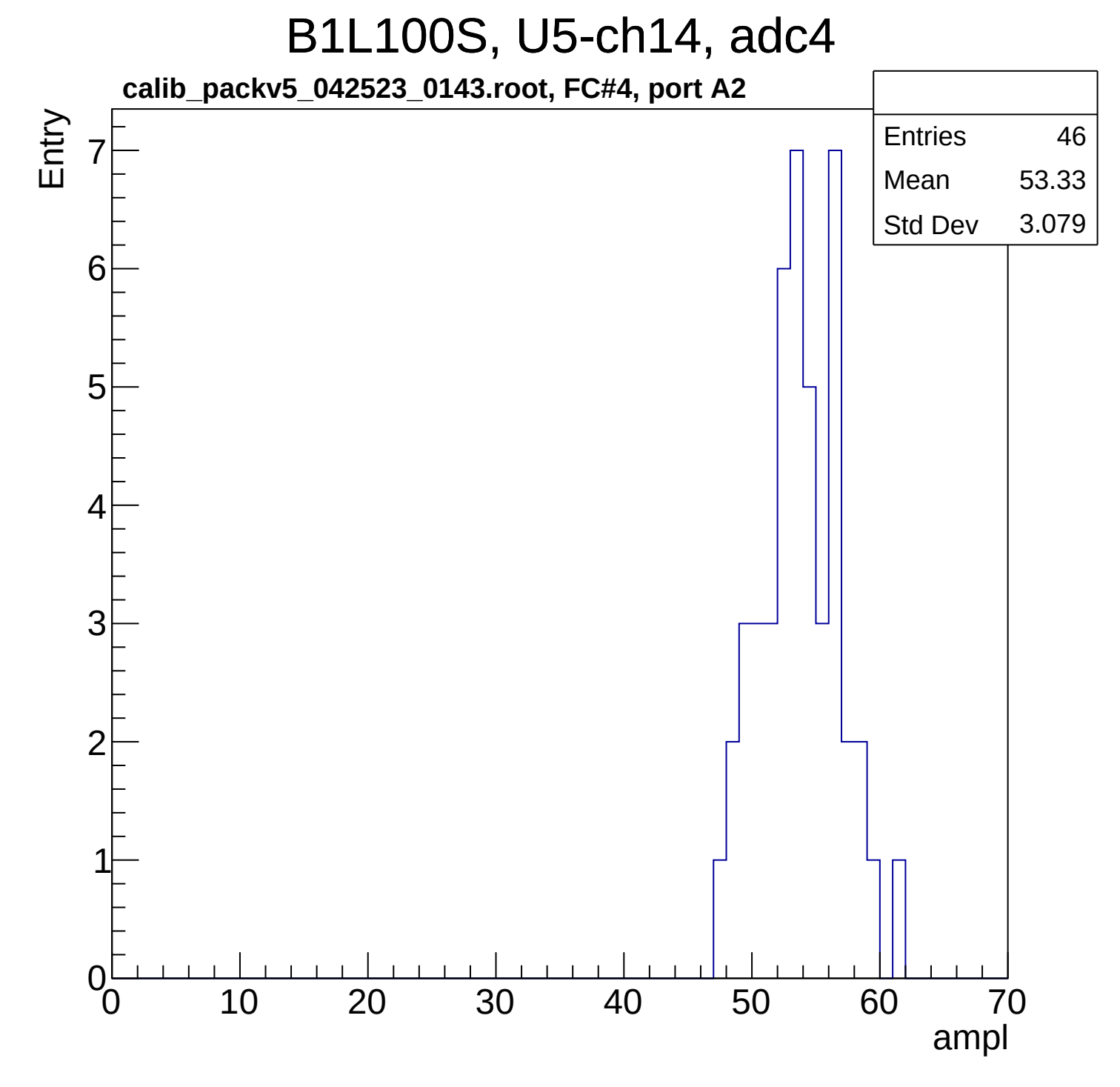
B1L100S, U5-ch14, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 46
Mean 53.33
Std Dev 3.079
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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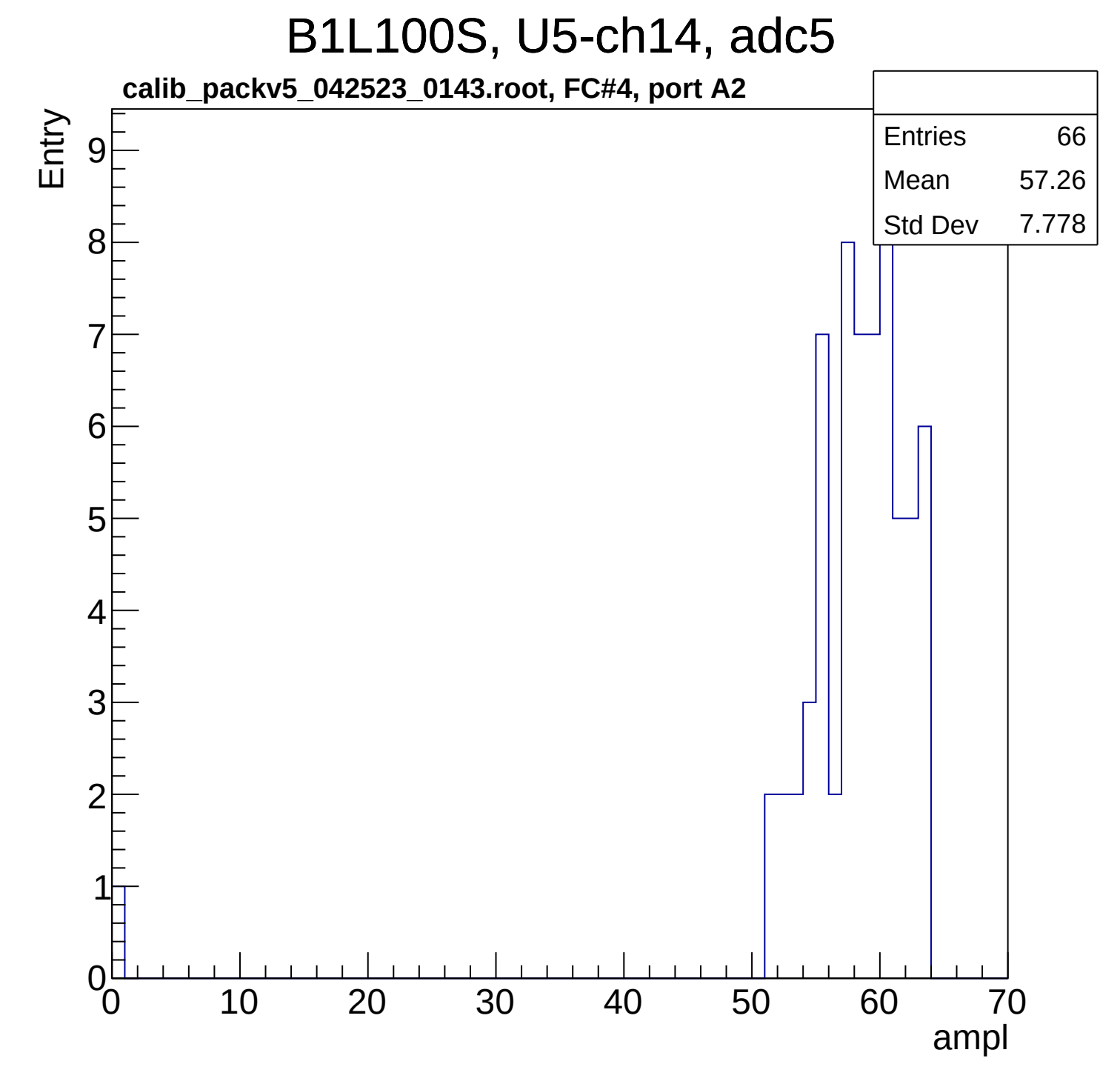
40
50
60
70


B1L100S, U5-ch14, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 57.26
Std Dev 7.778
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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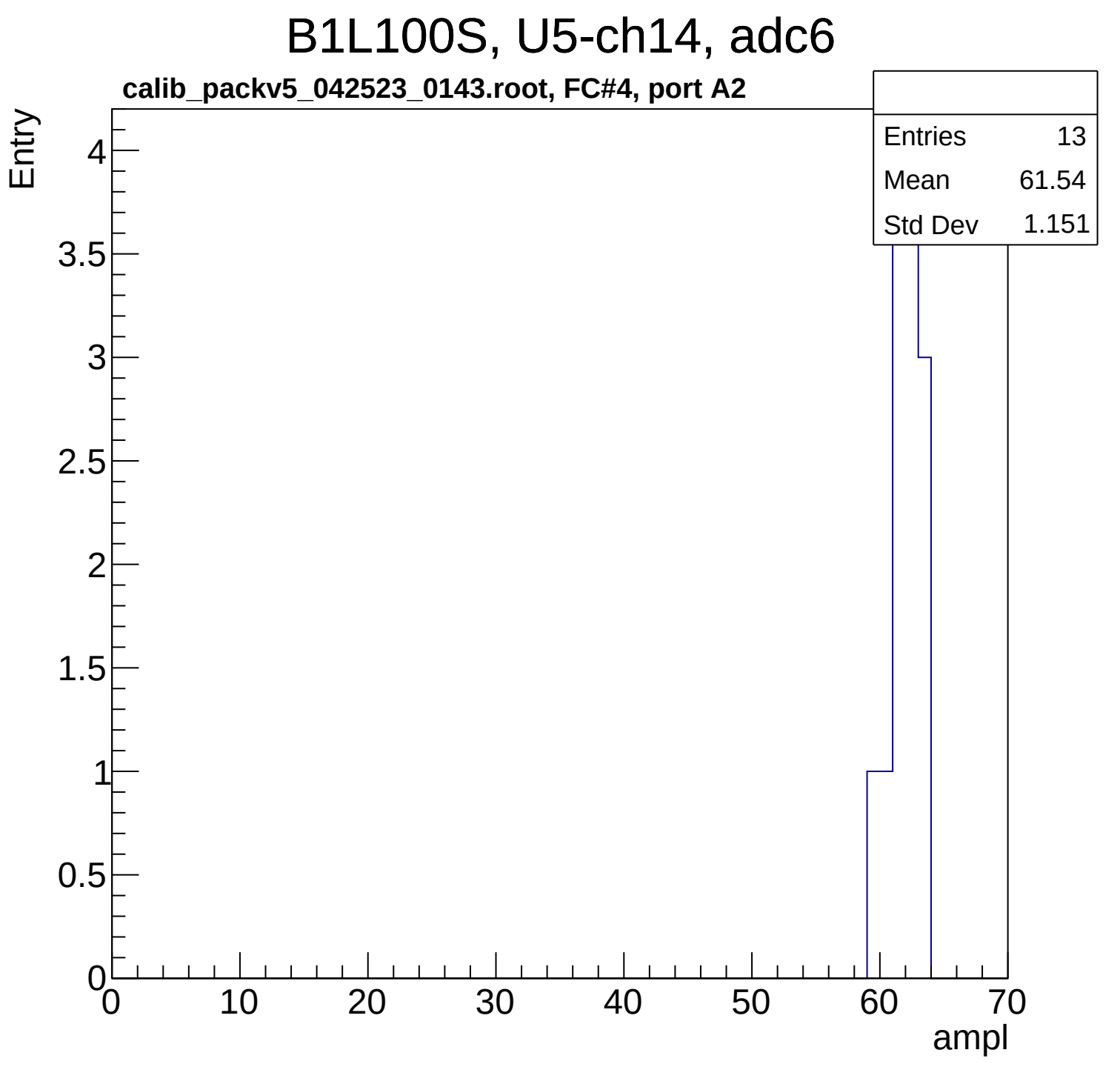
B1L100S, U5-ch14, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 13
Mean 61.54
Std Dev 1.151
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
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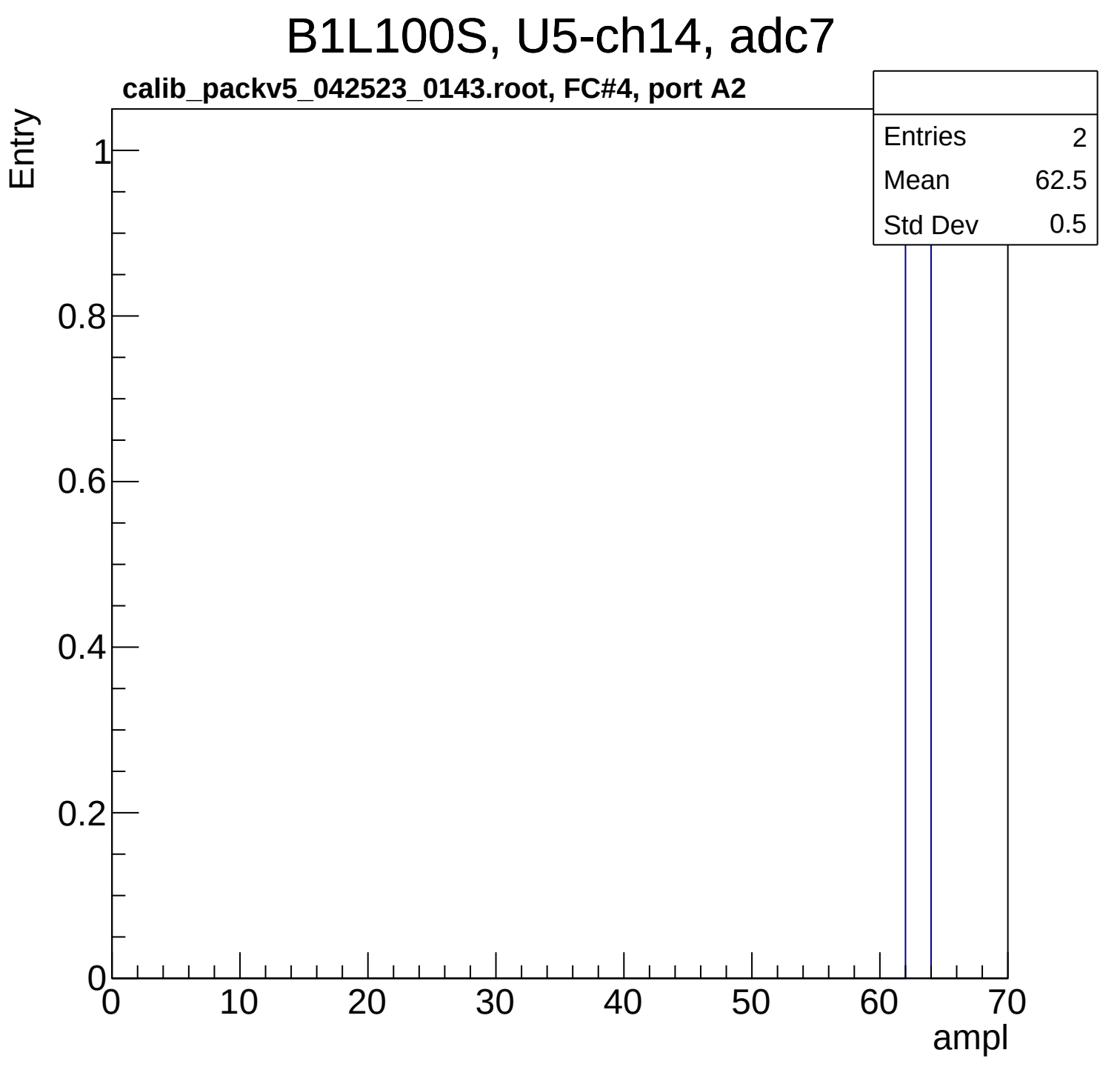
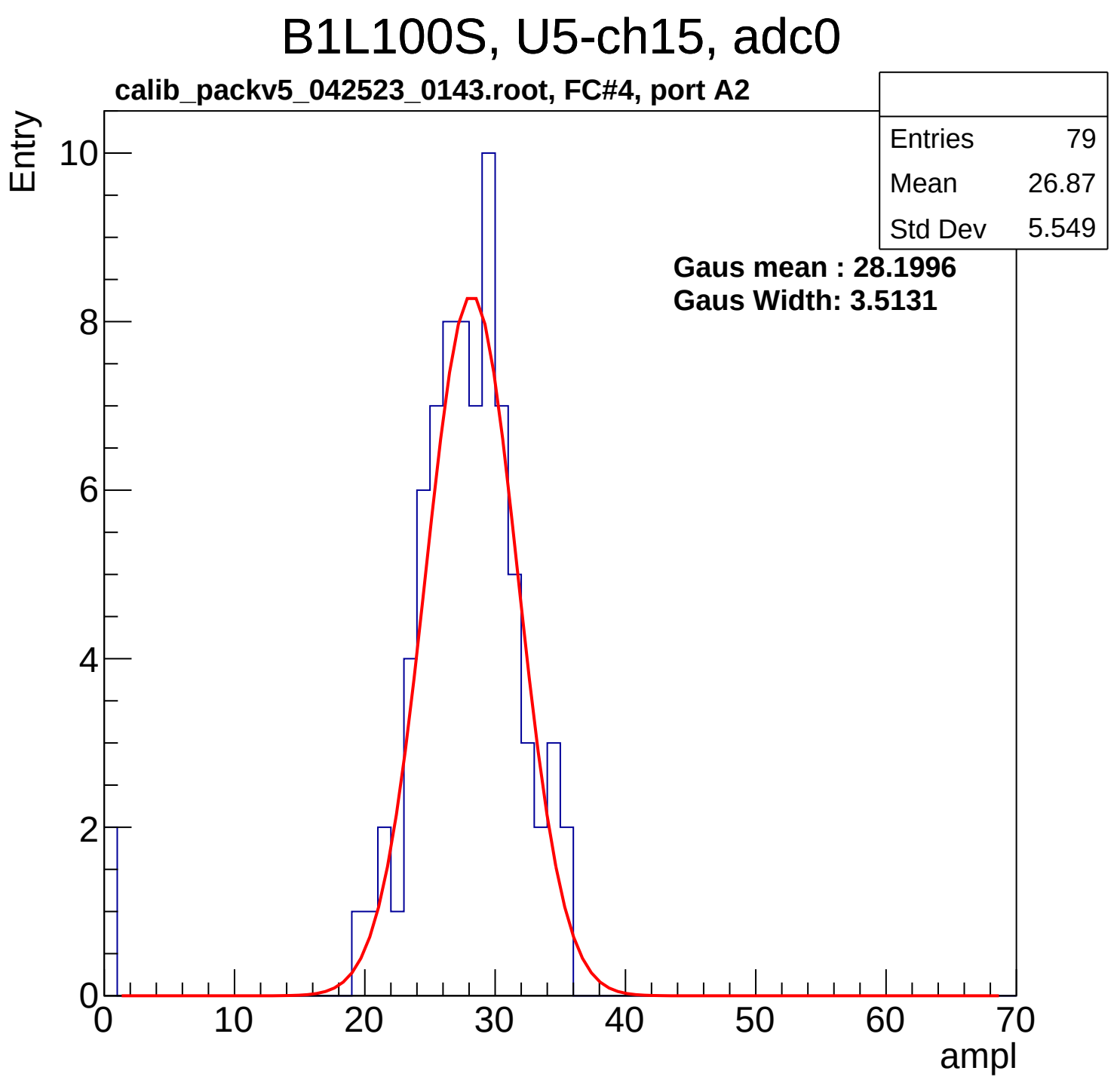
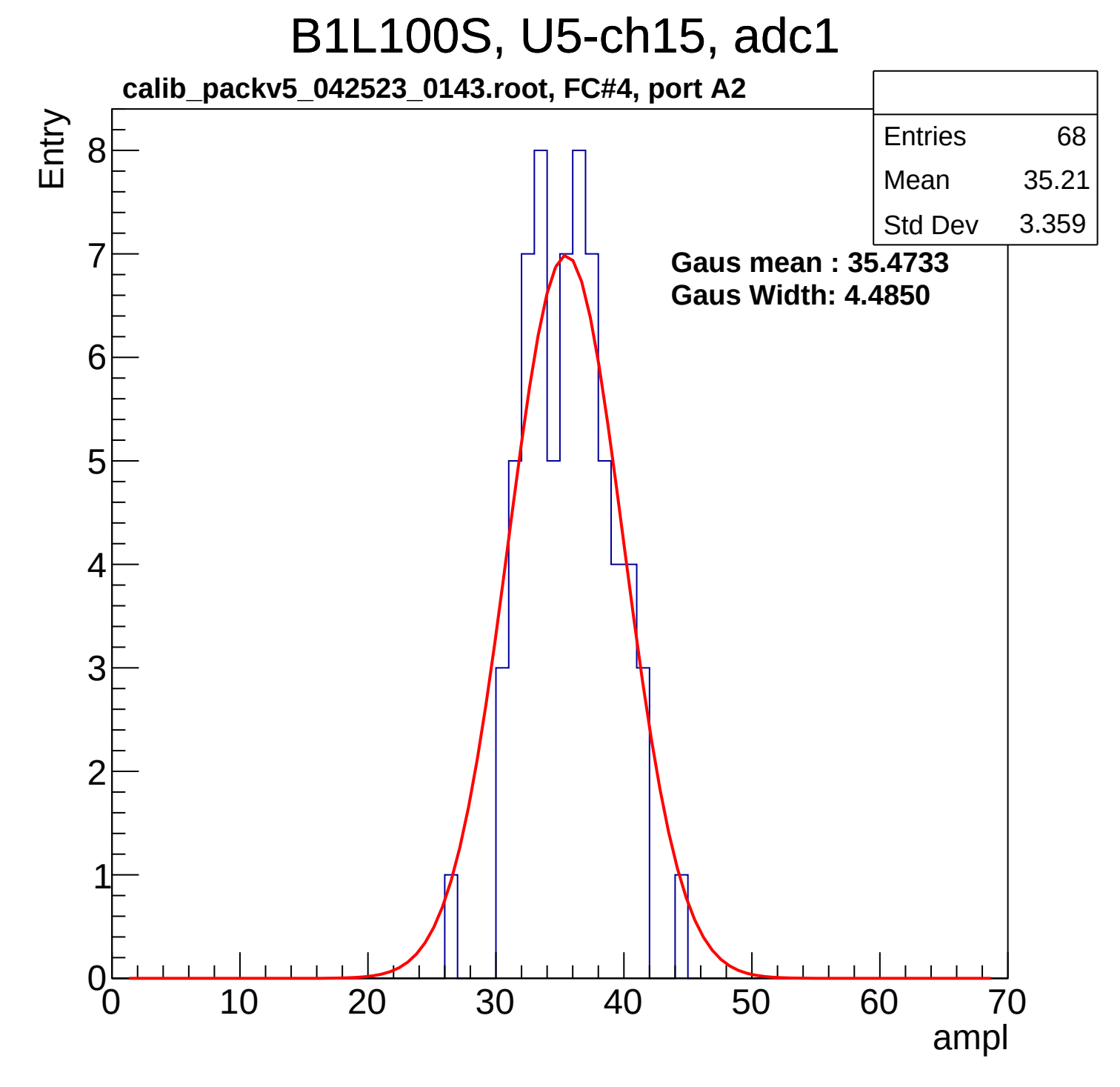
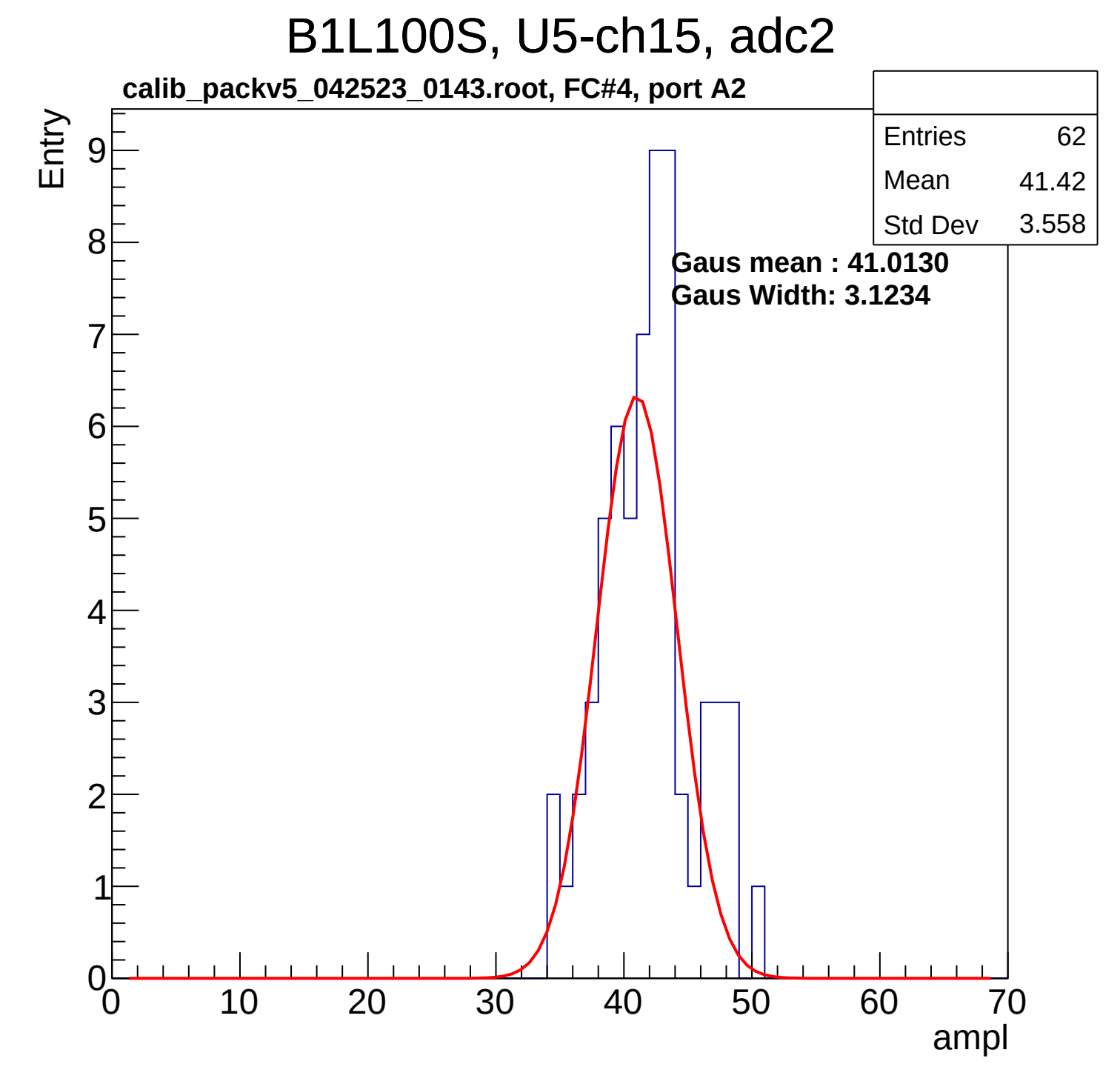
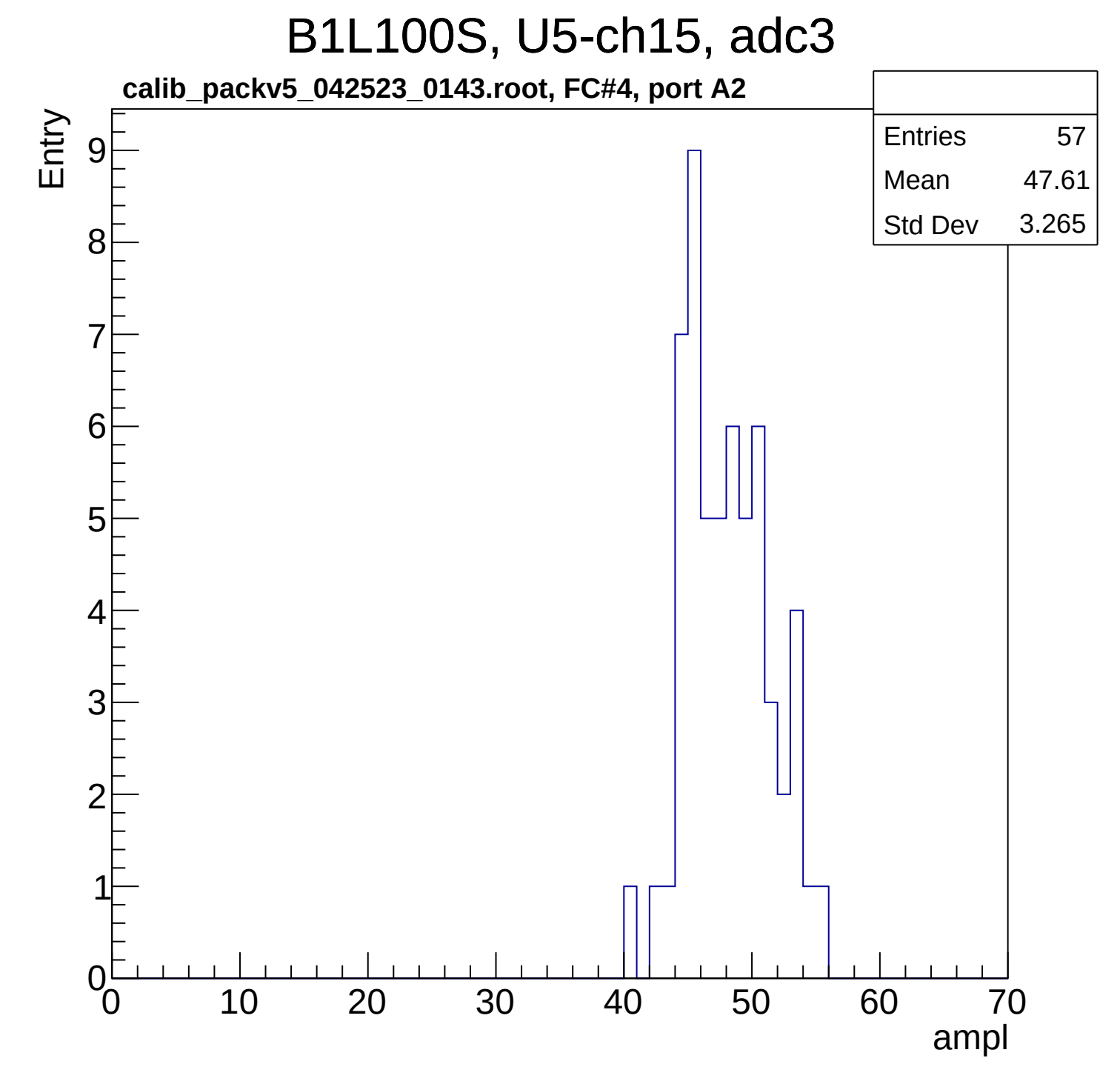
60
70


B1L100S, U5-ch14, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch15, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 79
Mean 26.87
Std Dev 5.549
Gaus mean : 28.1996
Gaus Width: 3.5131
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch15, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 35.21
Std Dev 3.359
Gaus mean : 35.4733
Gaus Width: 4.4850
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch15, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 41.42
Std Dev 3.558
Gaus mean : 41.0130
Gaus Width: 3.1234
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch15, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 47.61
Std Dev 3.265
Entry
ampl
0
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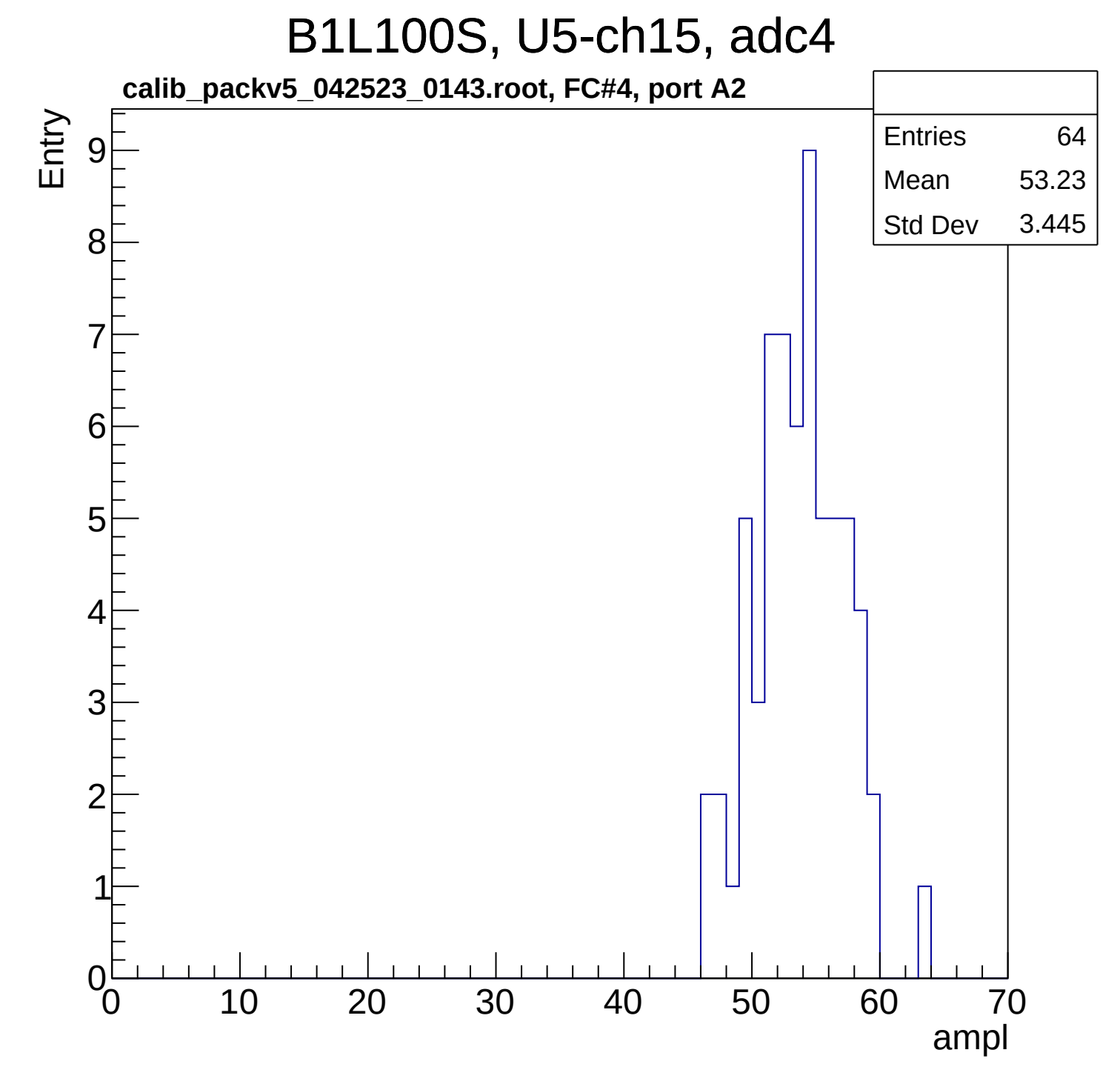
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch15, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 53.23
Std Dev 3.445
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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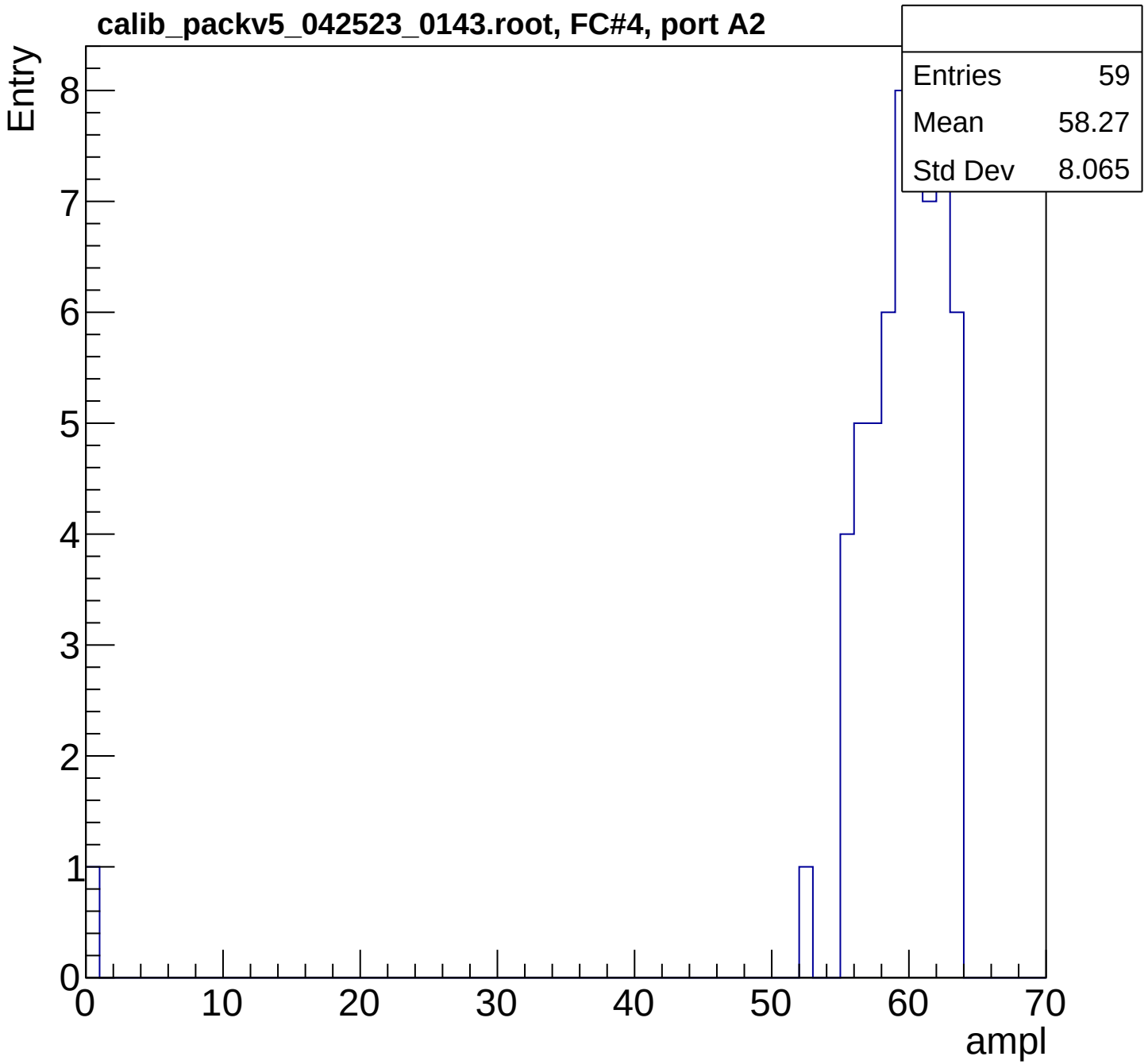
40
50
60
70


B1L100S, U5-ch15, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 58.27
Std Dev 8.065
Entry
ampl
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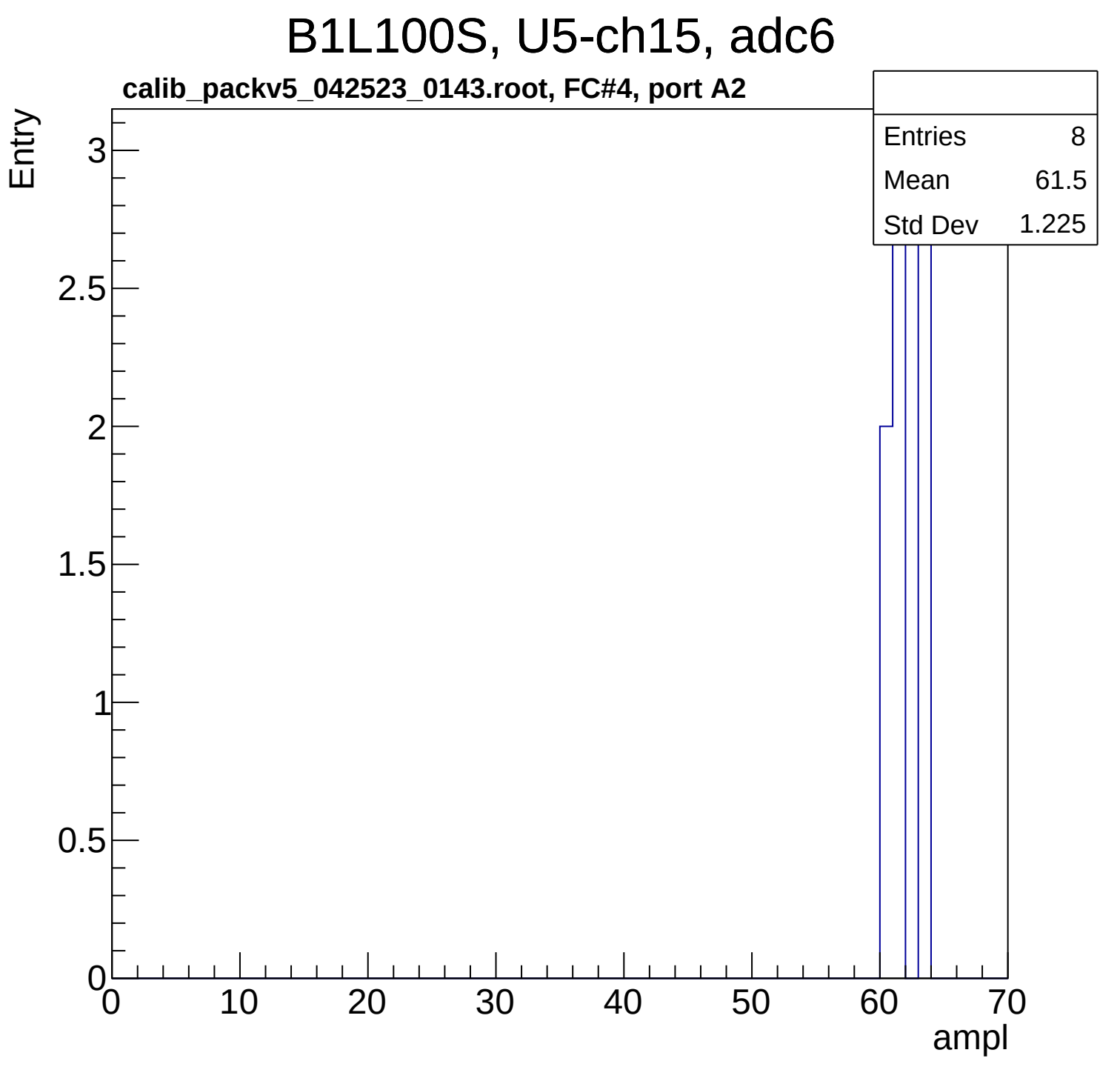
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch15, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 8
Mean 61.5
Std Dev 1.225
Entry
ampl
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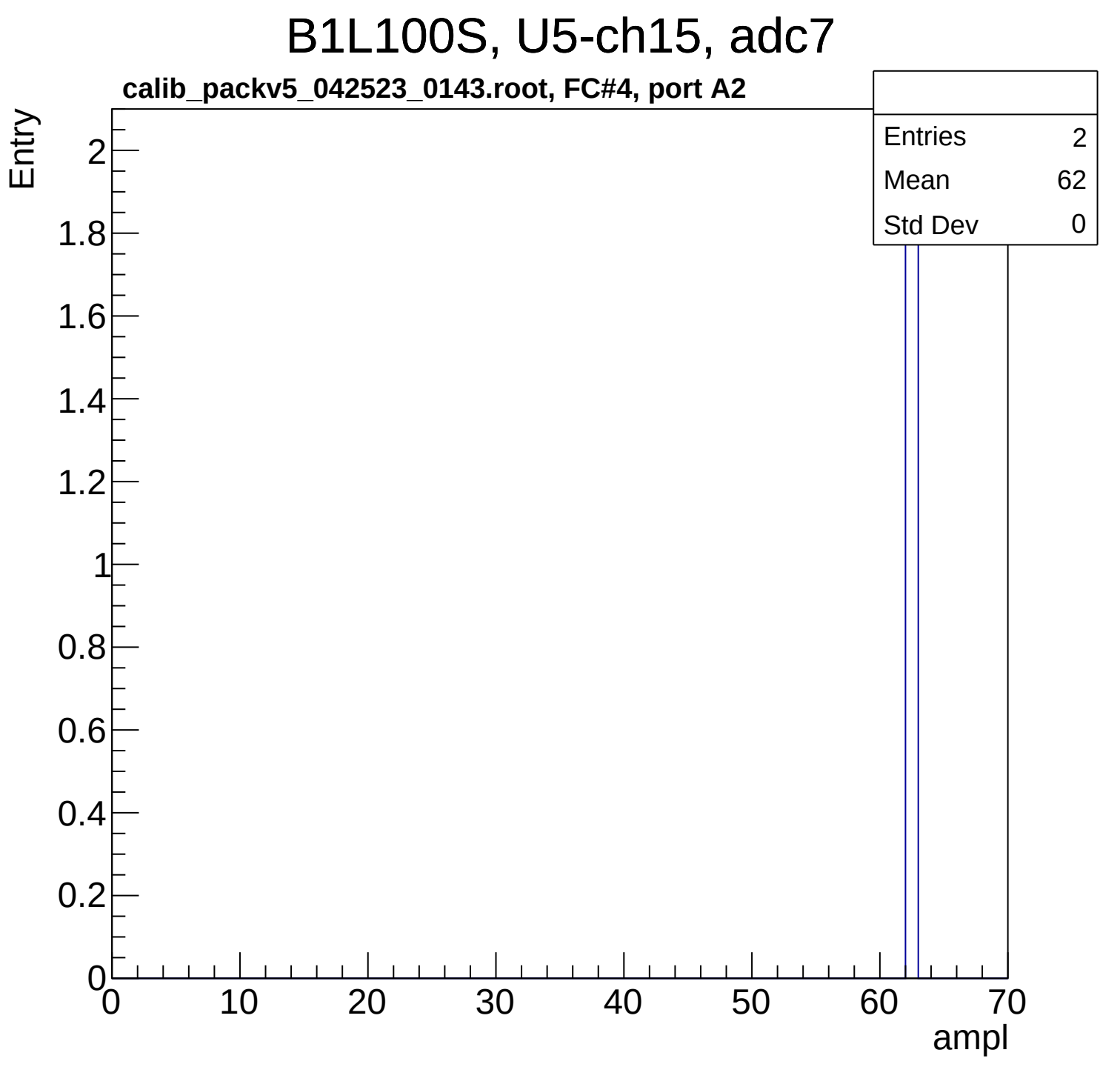
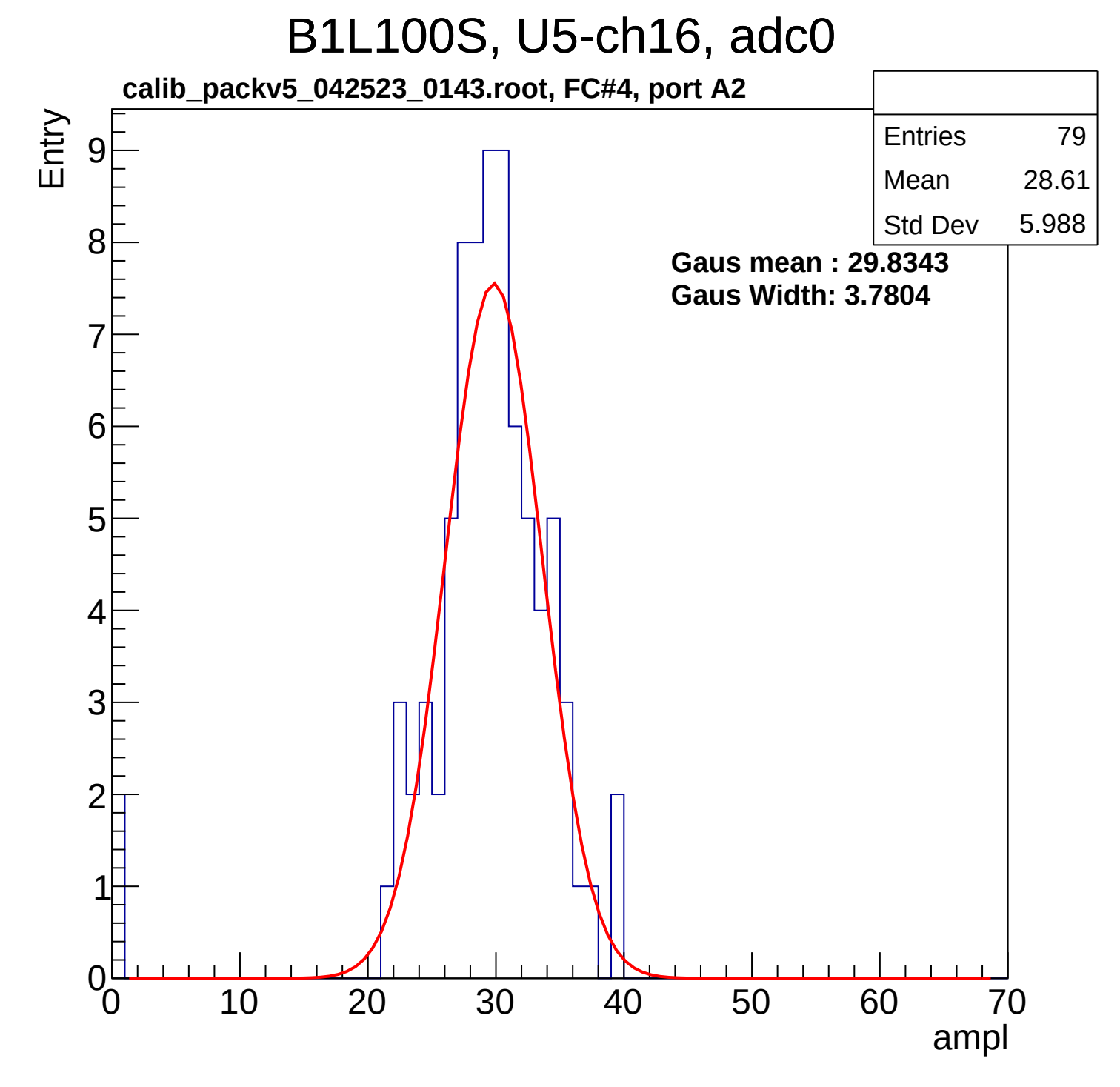
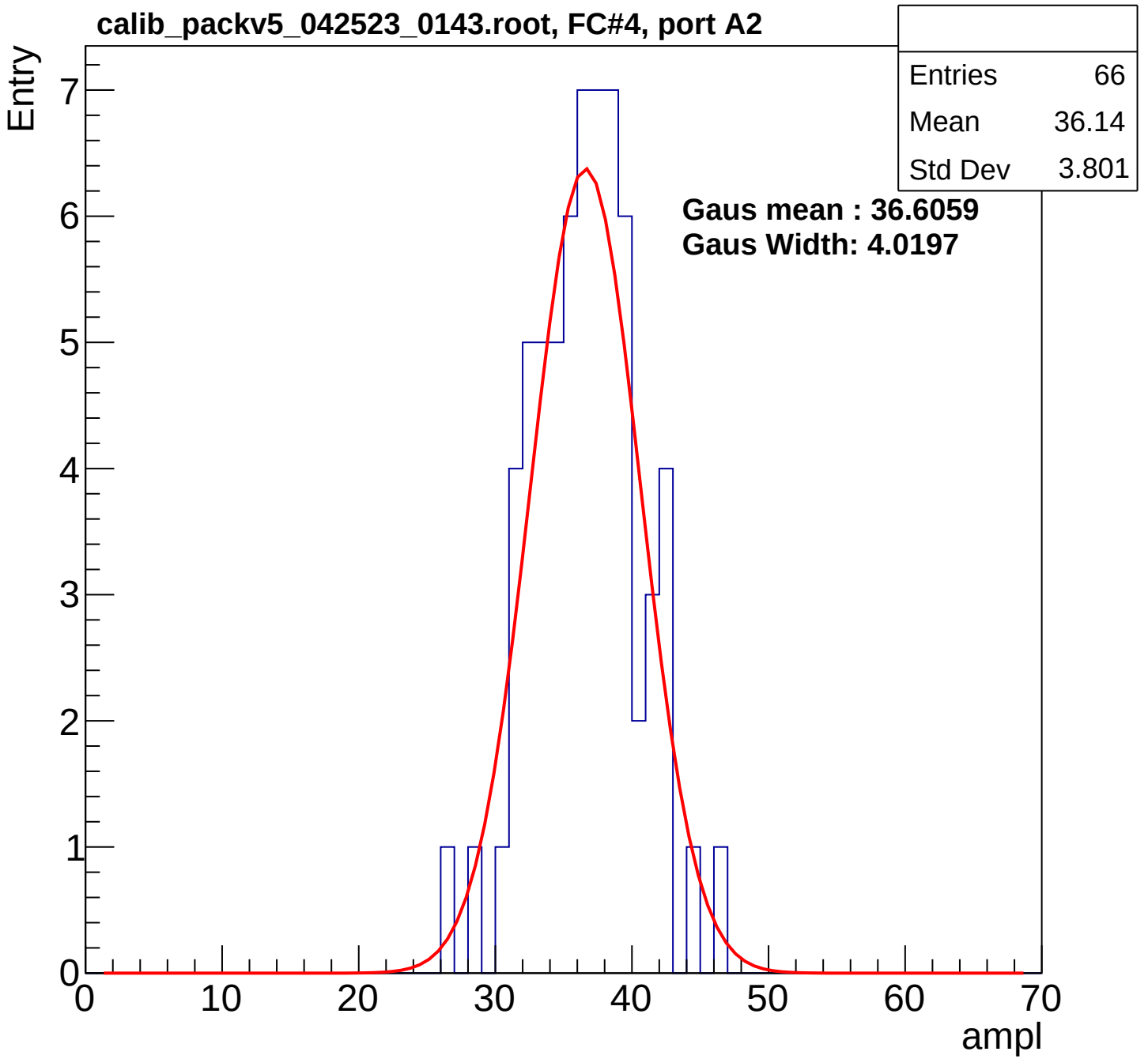
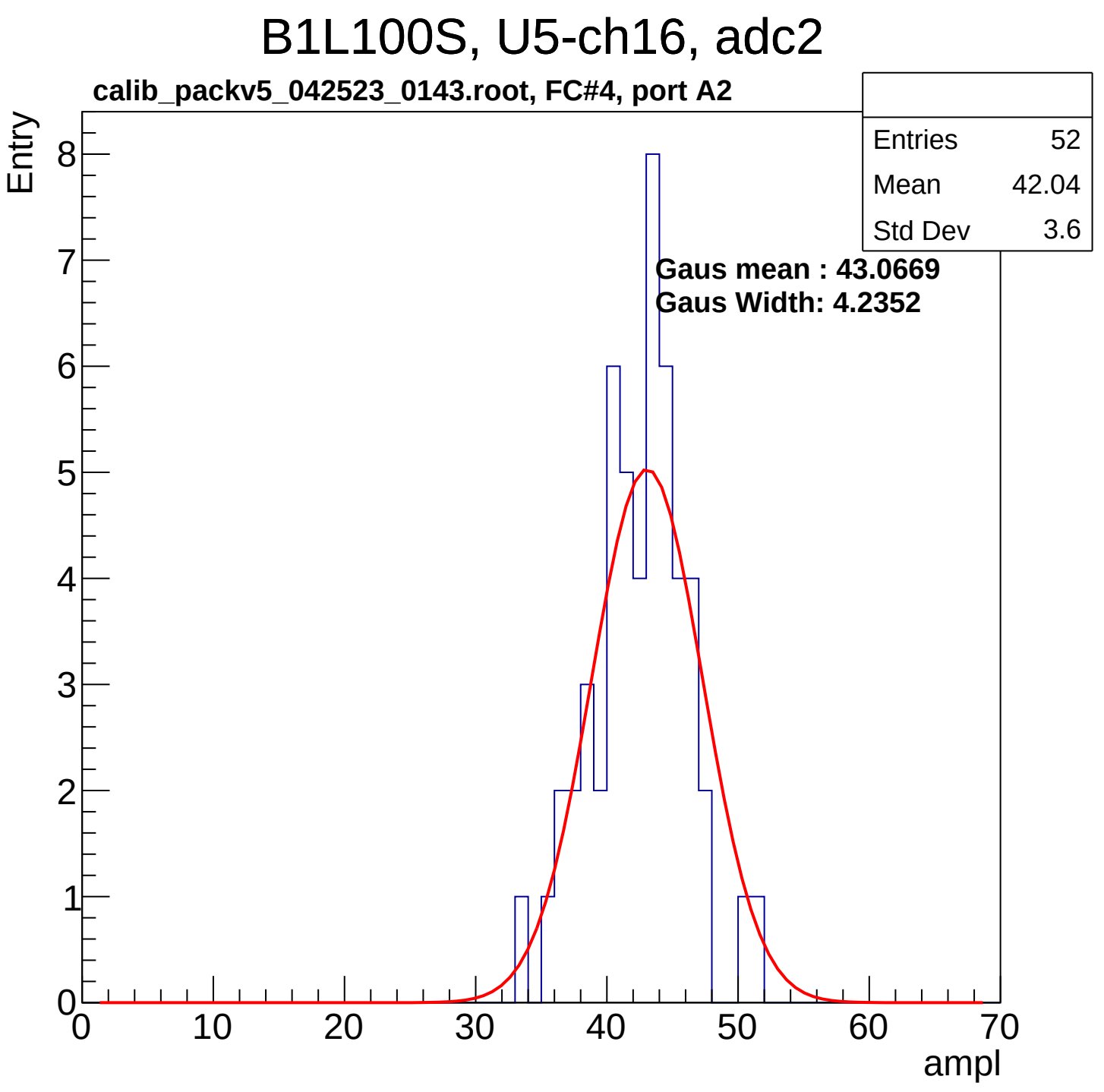
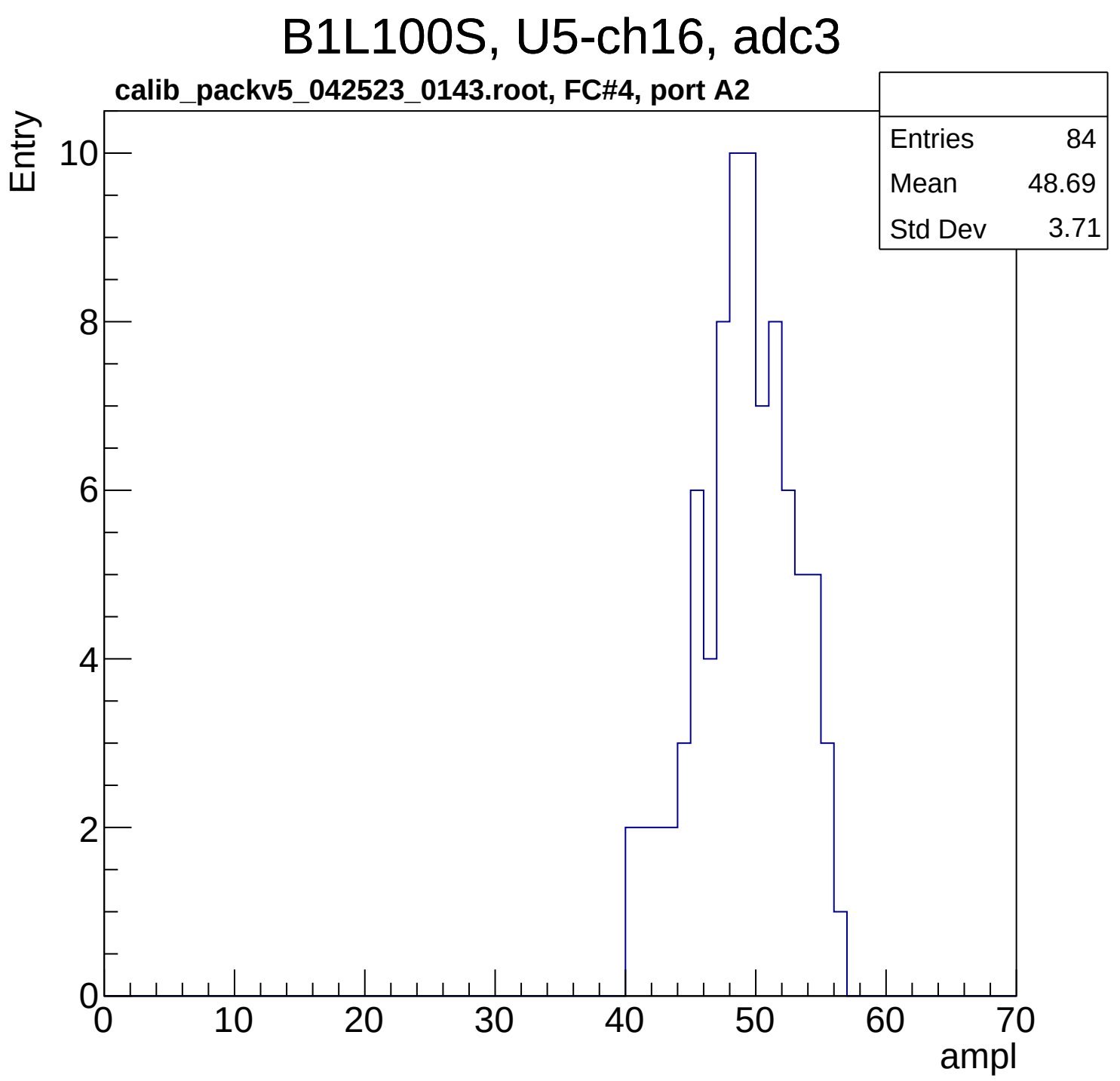
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

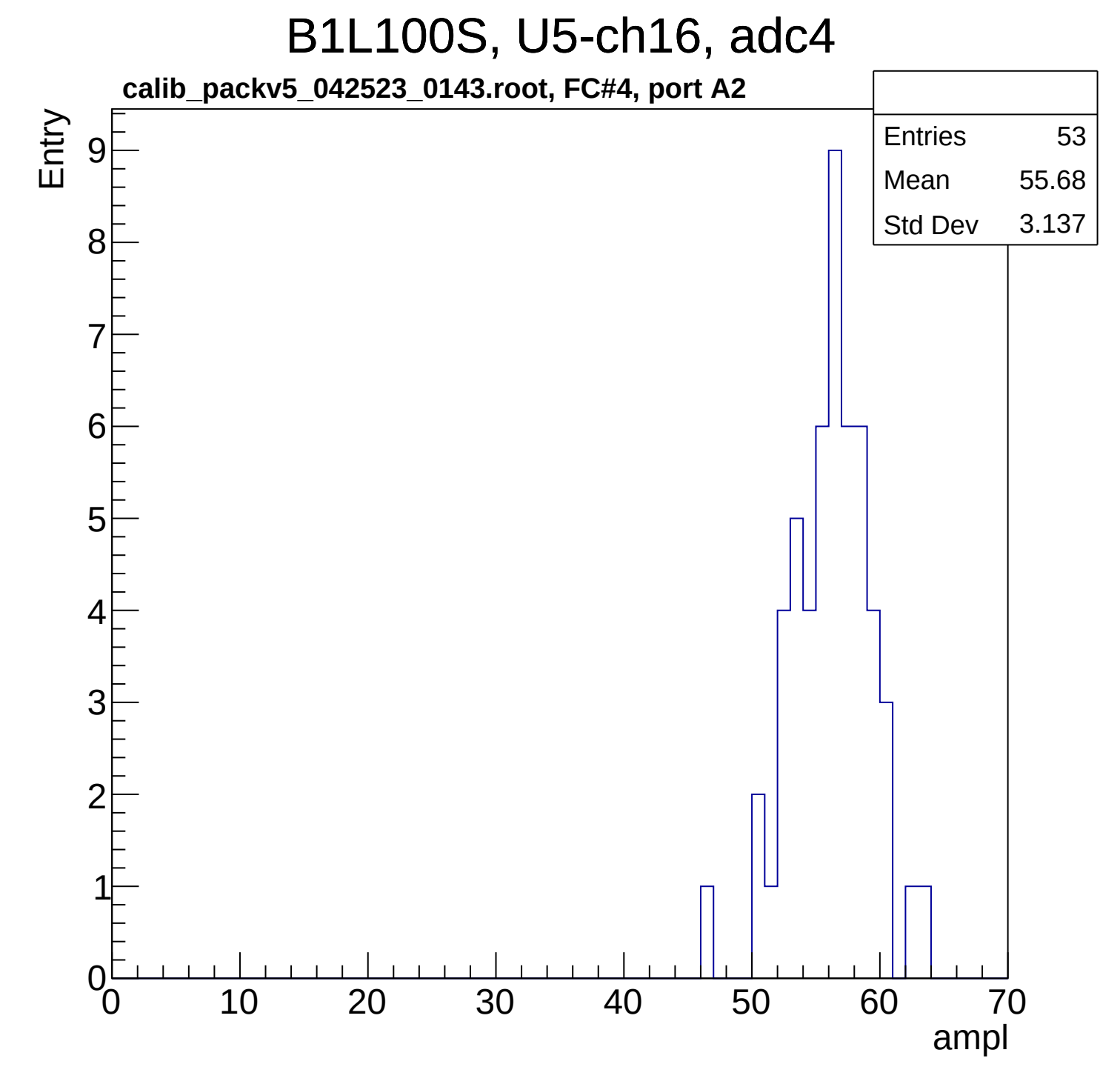

B1L100S, U5-ch15, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 62
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L100S, U5-ch16, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 79
Mean 28.61
Std Dev 5.988
Gaus mean : 29.8343
Gaus Width: 3.7804
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch16, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 36.14
Std Dev 3.801
Gaus mean : 36.6059
Gaus Width: 4.0197
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U5-ch16, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 52
Mean 42.04
Std Dev 3.6
Gaus mean : 43.0669
Gaus Width: 4.2352
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch16, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 84
Mean 48.69
Std Dev 3.71
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch16, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 55.68
Std Dev 3.137
Entry
ampl
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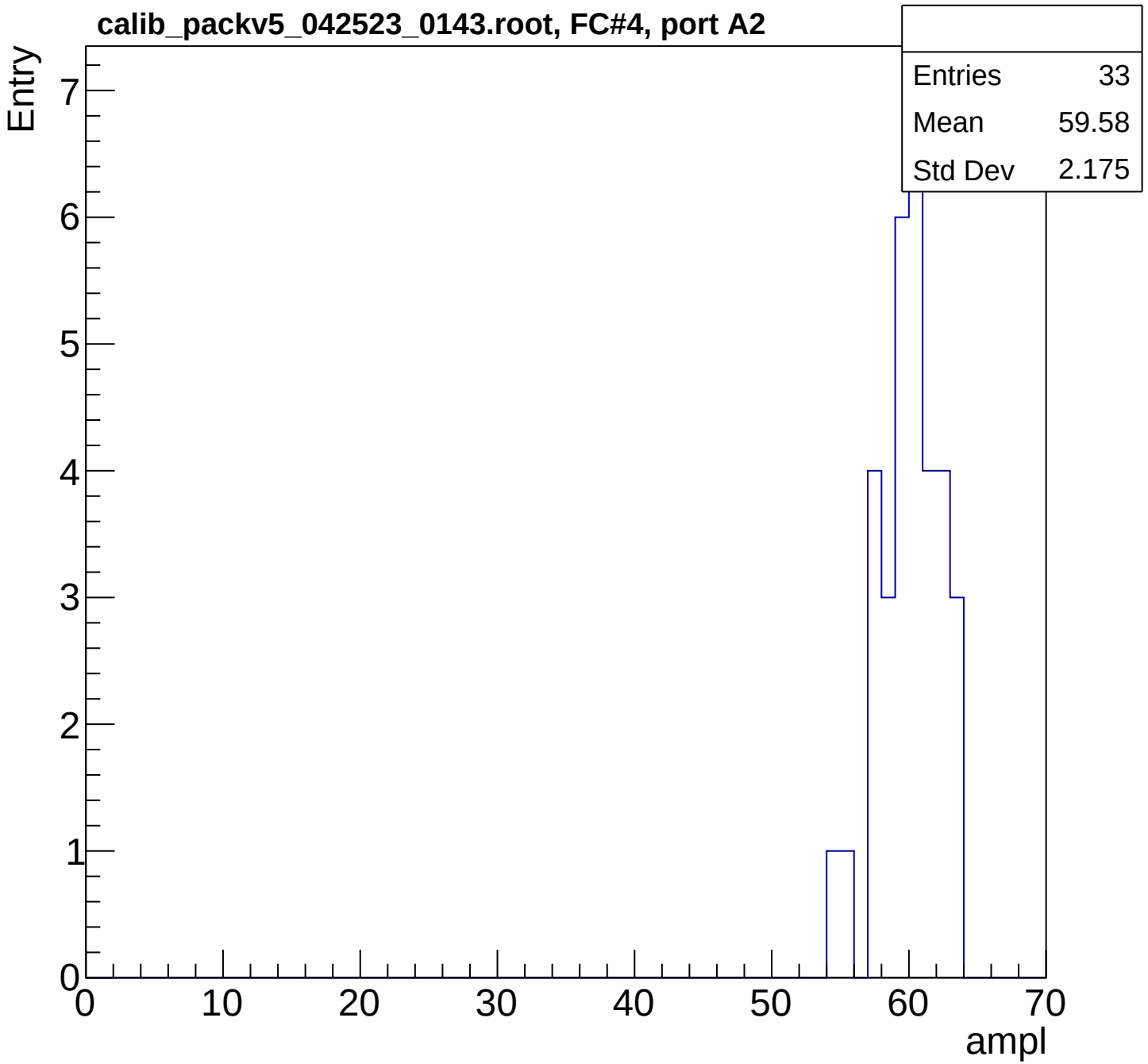
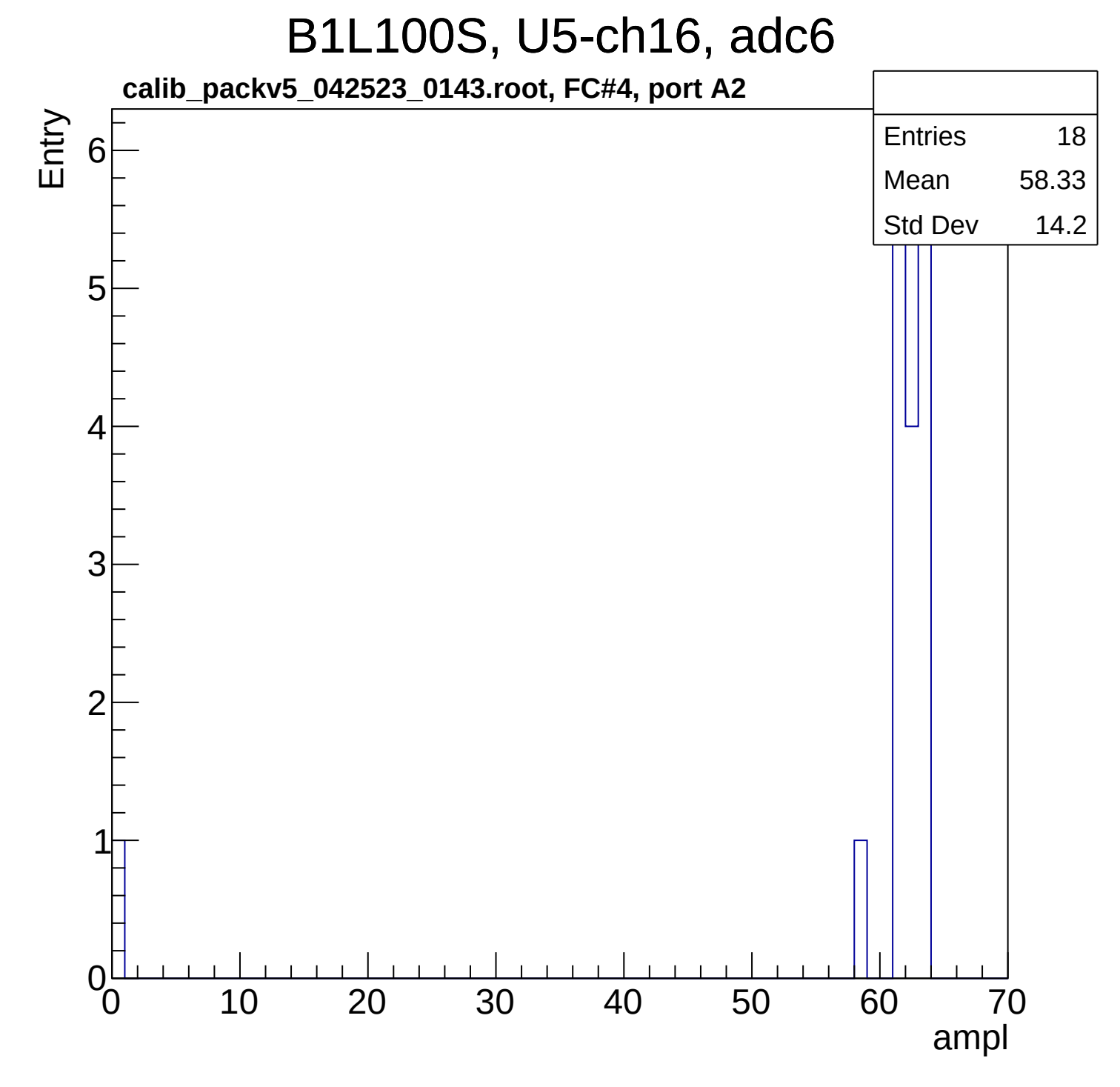
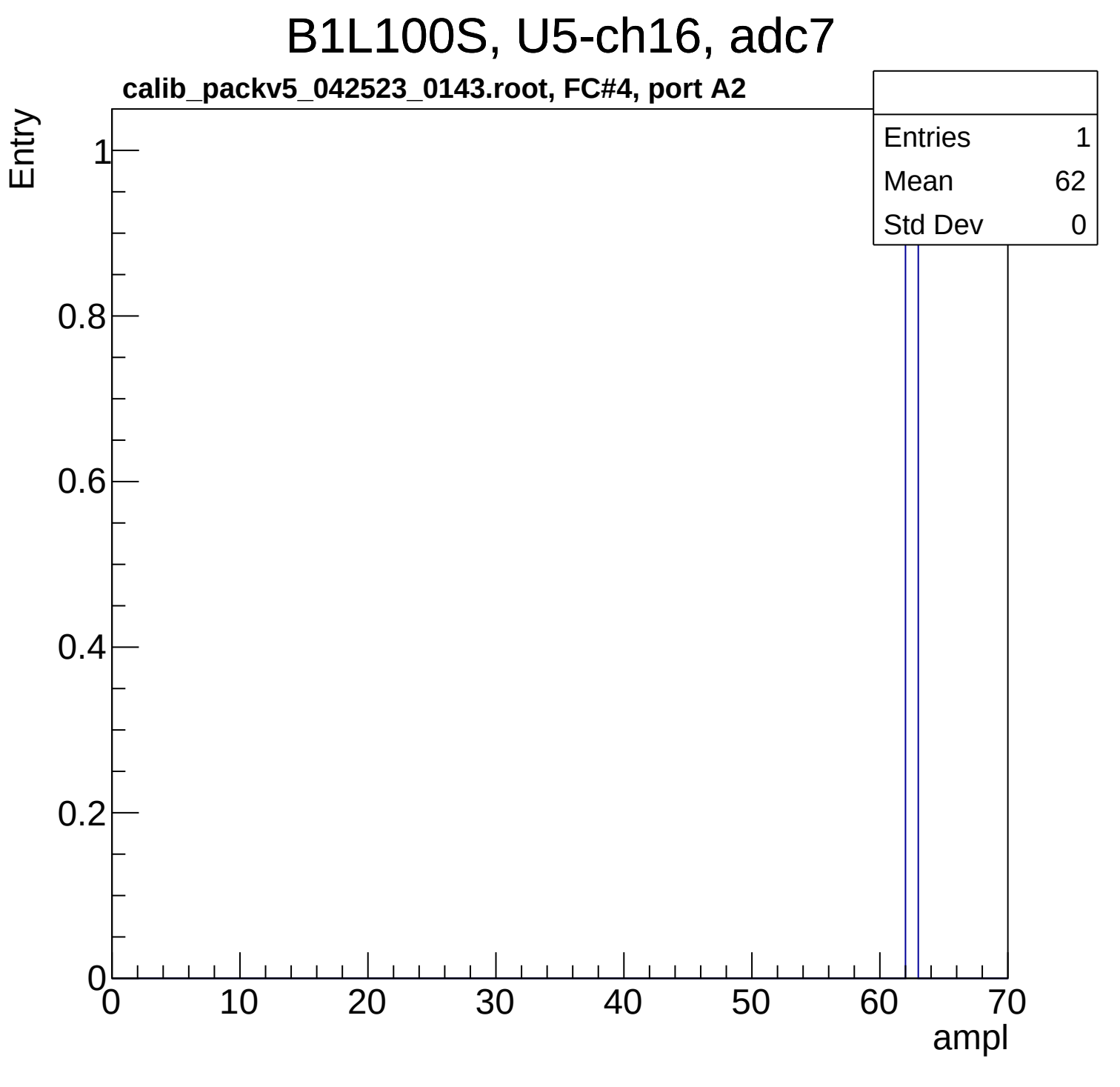
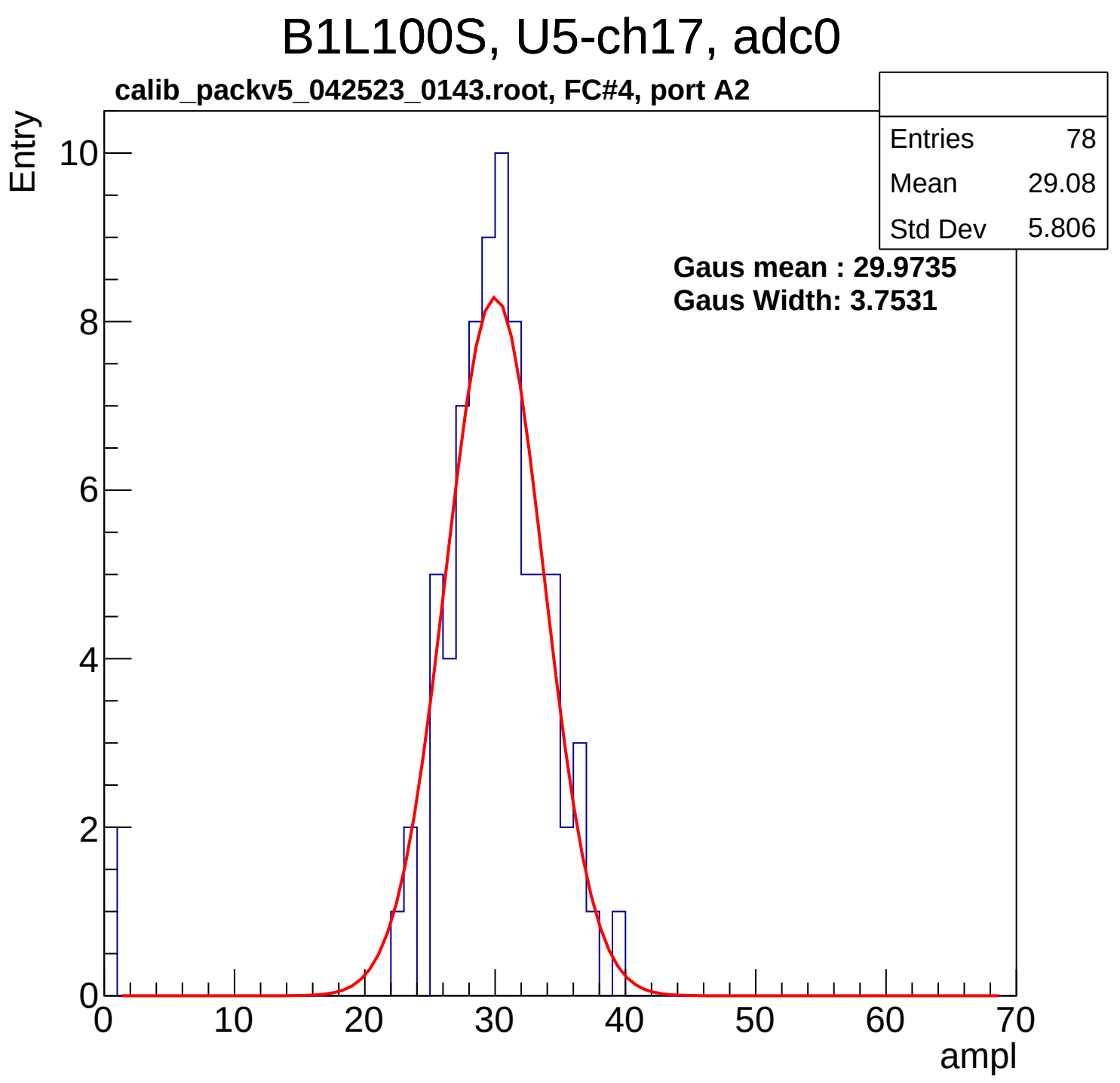
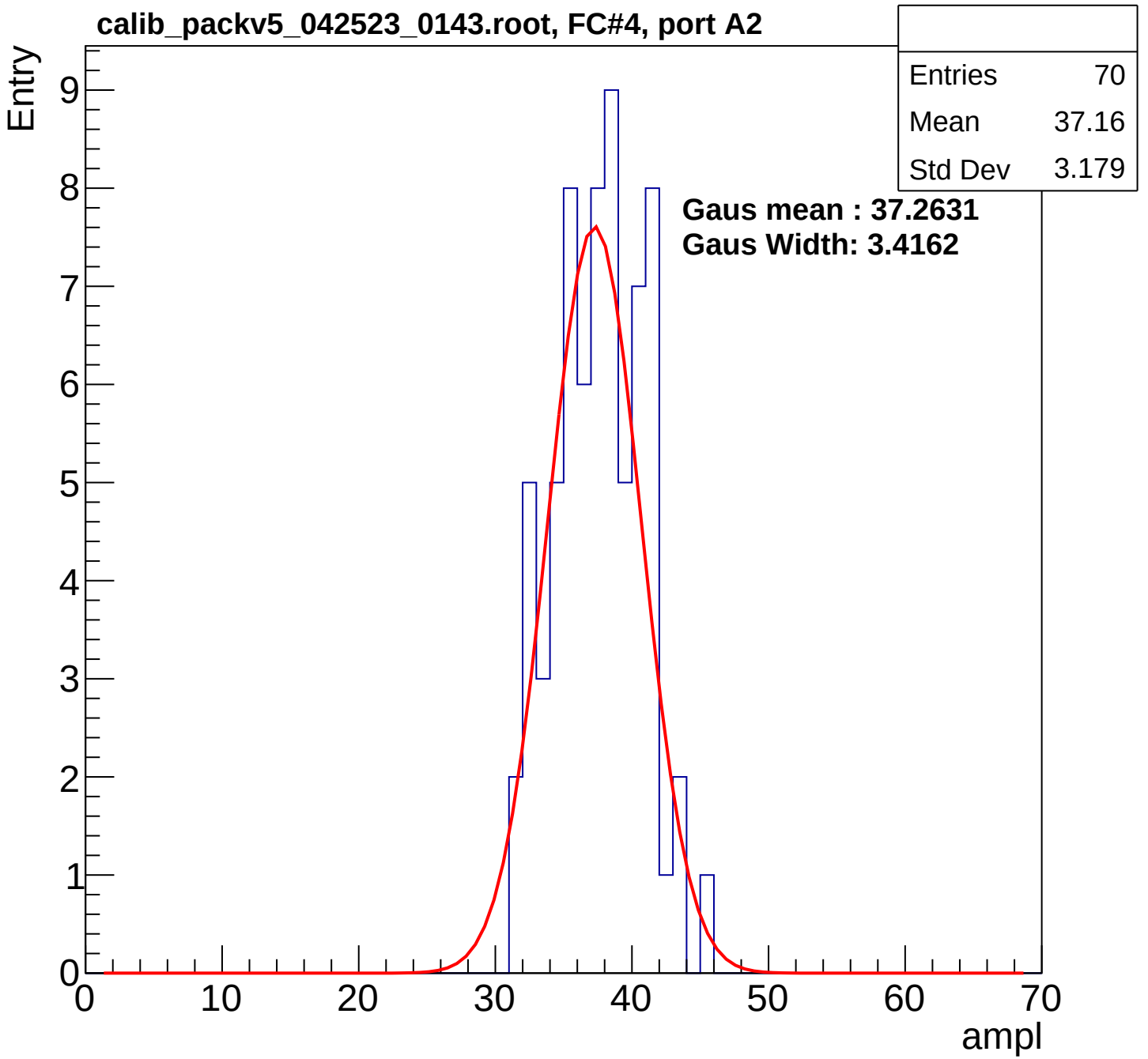
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

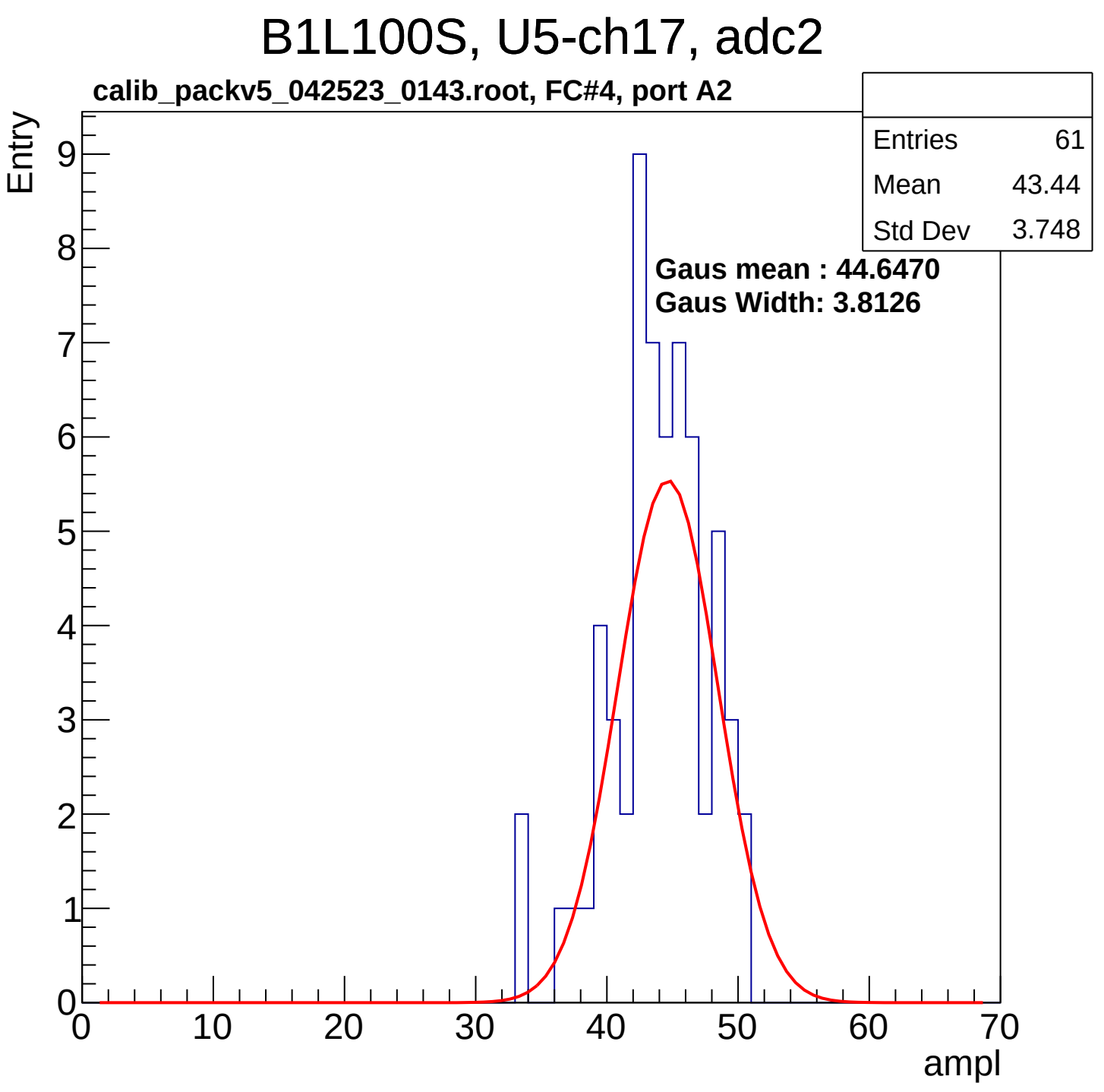

B1L100S, U5-ch16, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 33
Mean 59.58
Std Dev 2.175
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U5-ch16, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 18
Mean 58.33
Std Dev 14.2
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch16, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 62
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch17, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 78
Mean 29.08
Std Dev 5.806
Gaus mean : 29.9735
Gaus Width: 3.7531
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch17, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 37.16
Std Dev 3.179
Gaus mean : 37.2631
Gaus Width: 3.4162
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch17, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 43.44
Std Dev 3.748
Gaus mean : 44.6470
Gaus Width: 3.8126
Entry
ampl
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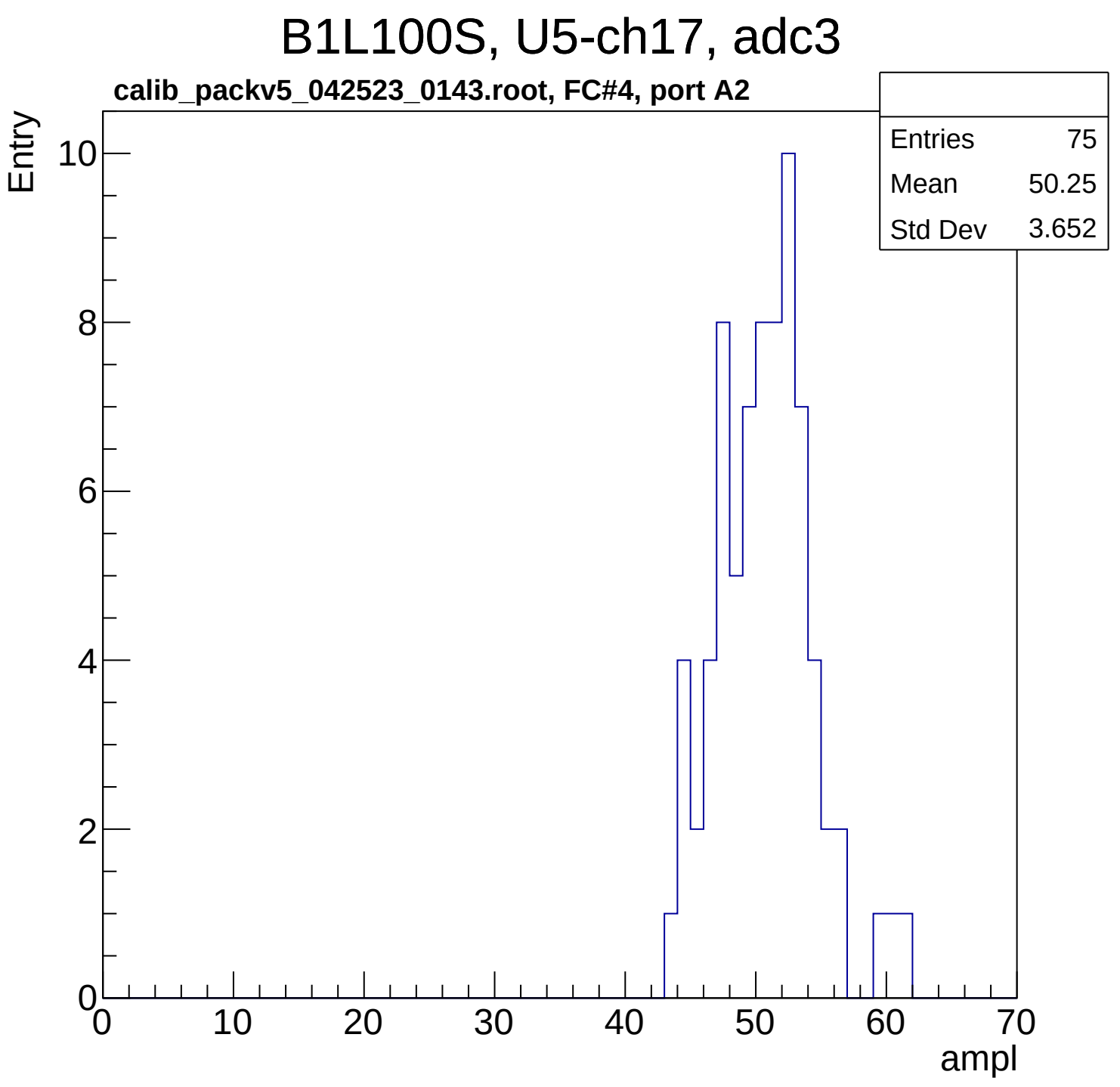
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch17, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 75
Mean 50.25
Std Dev 3.652
Entry
ampl
0
2
4
6
8
10
0
10
20
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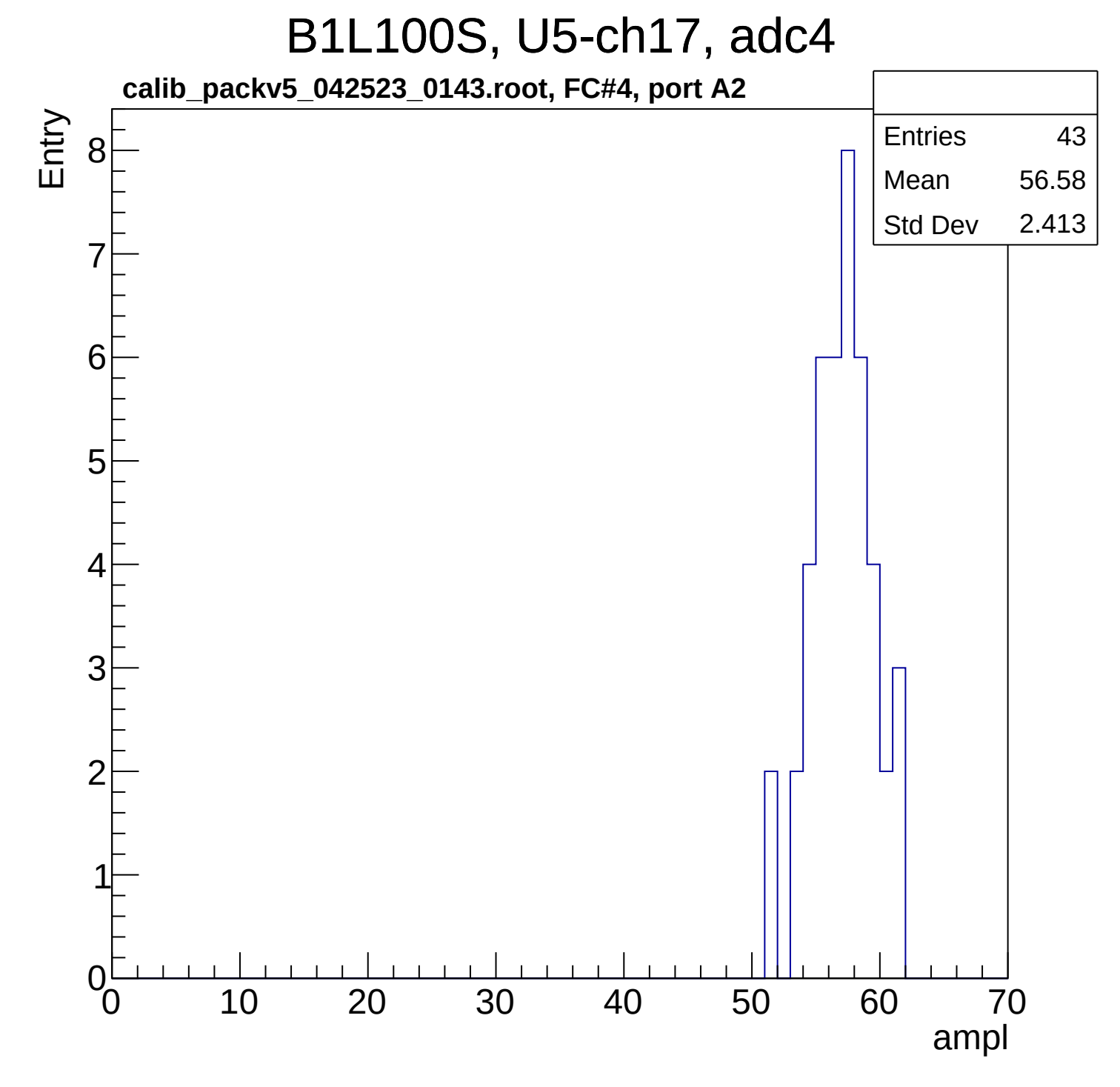
40
50
60
70


B1L100S, U5-ch17, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 43
Mean 56.58
Std Dev 2.413
Entry
ampl
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1
2
3
4
5
6
7
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0
10
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60
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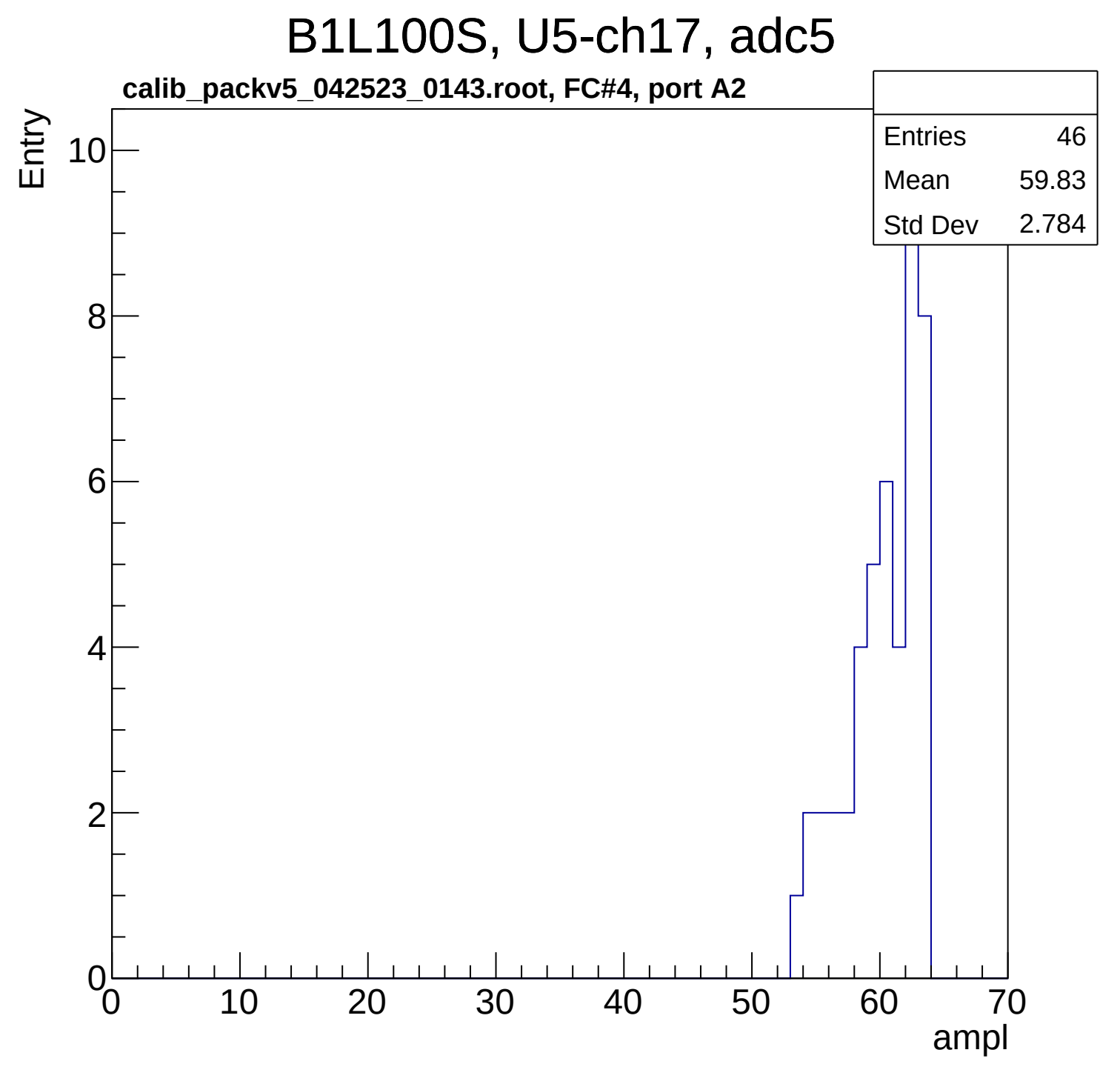
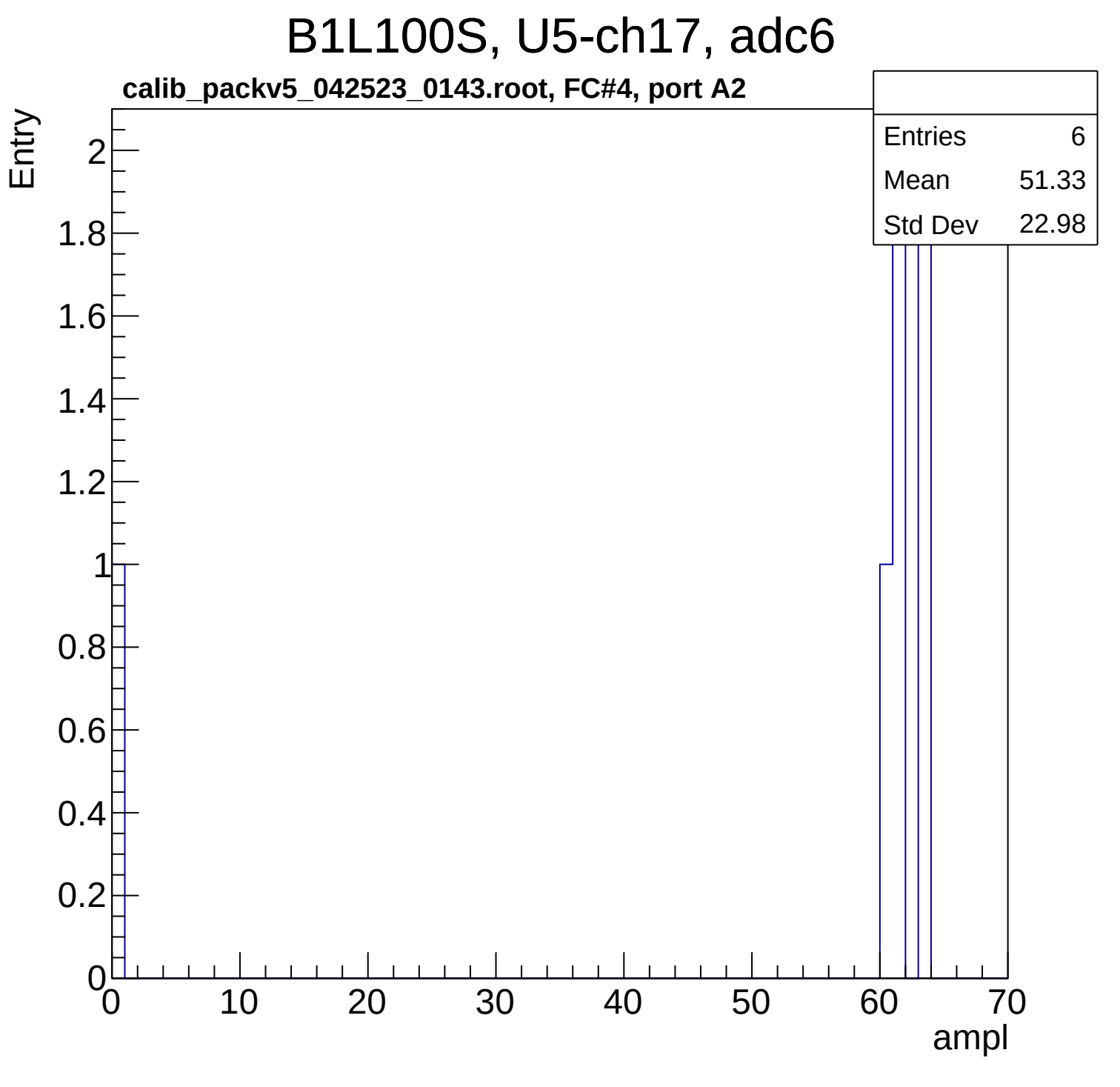
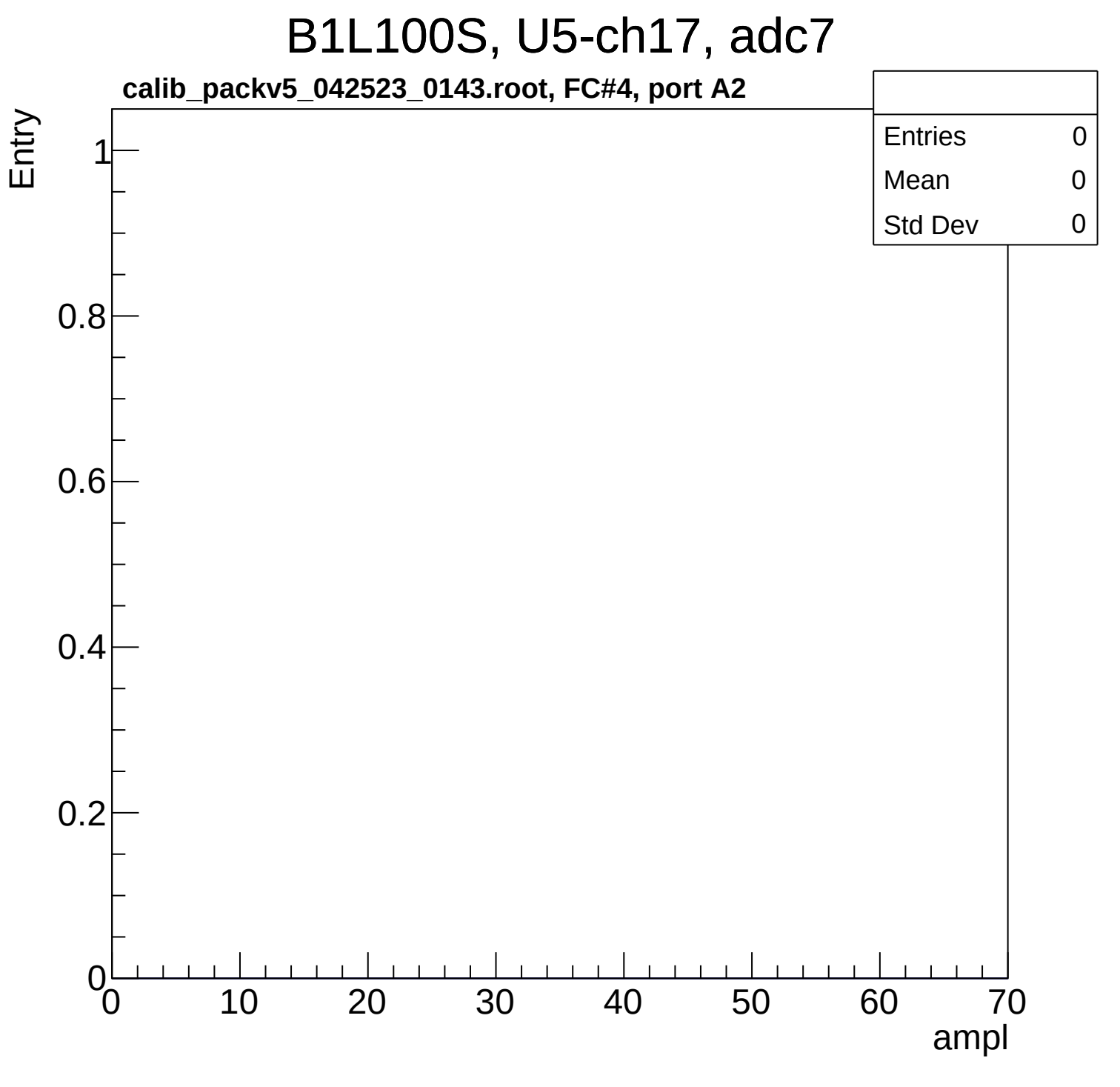

B1L100S, U5-ch17, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 46
Mean 59.83
Std Dev 2.784
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch17, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 6
Mean 51.33
Std Dev 22.98
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L100S, U5-ch17, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
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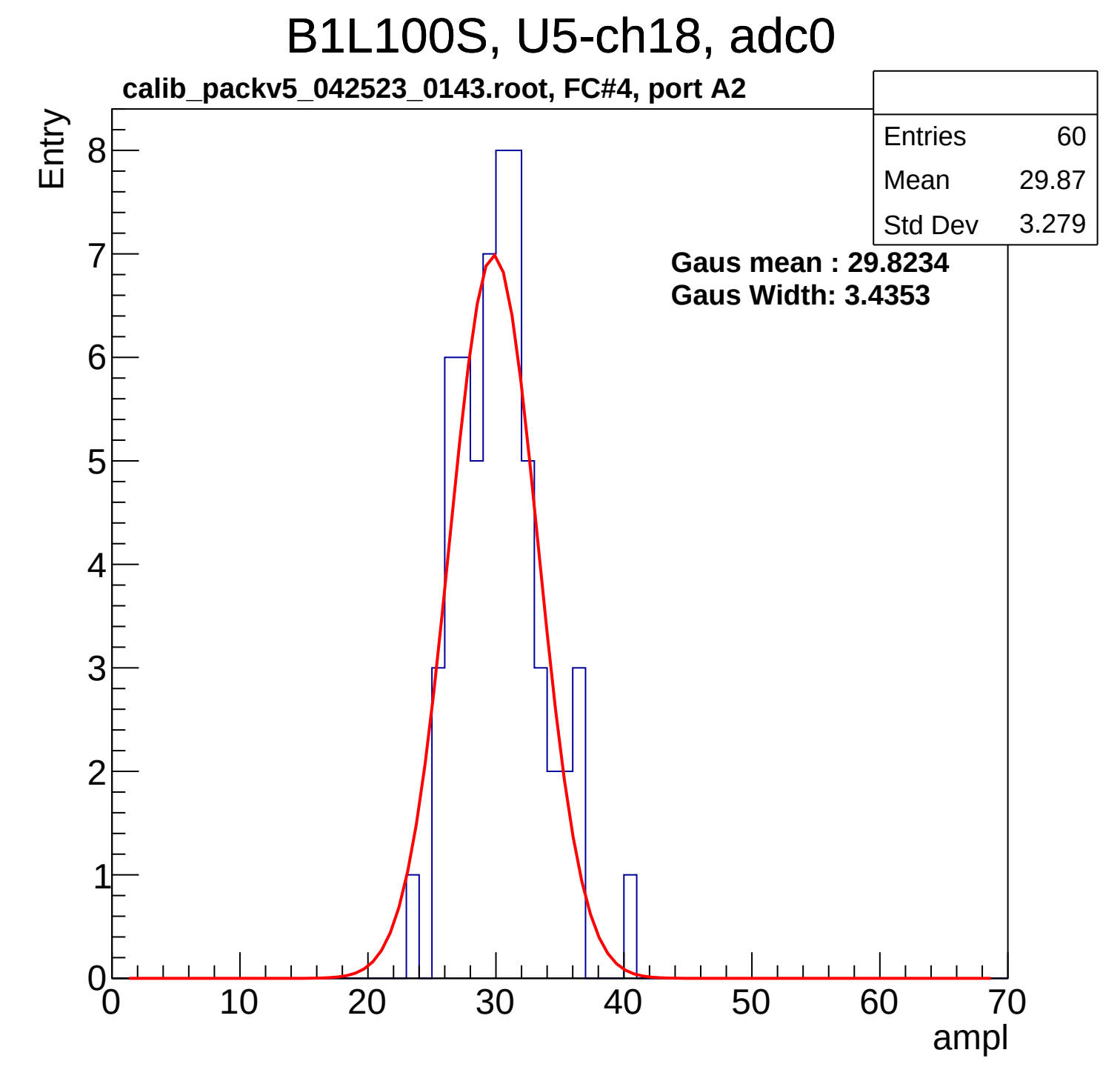
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch18, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 29.87
Std Dev 3.279
Gaus mean : 29.8234
Gaus Width: 3.4353
Entry
ampl
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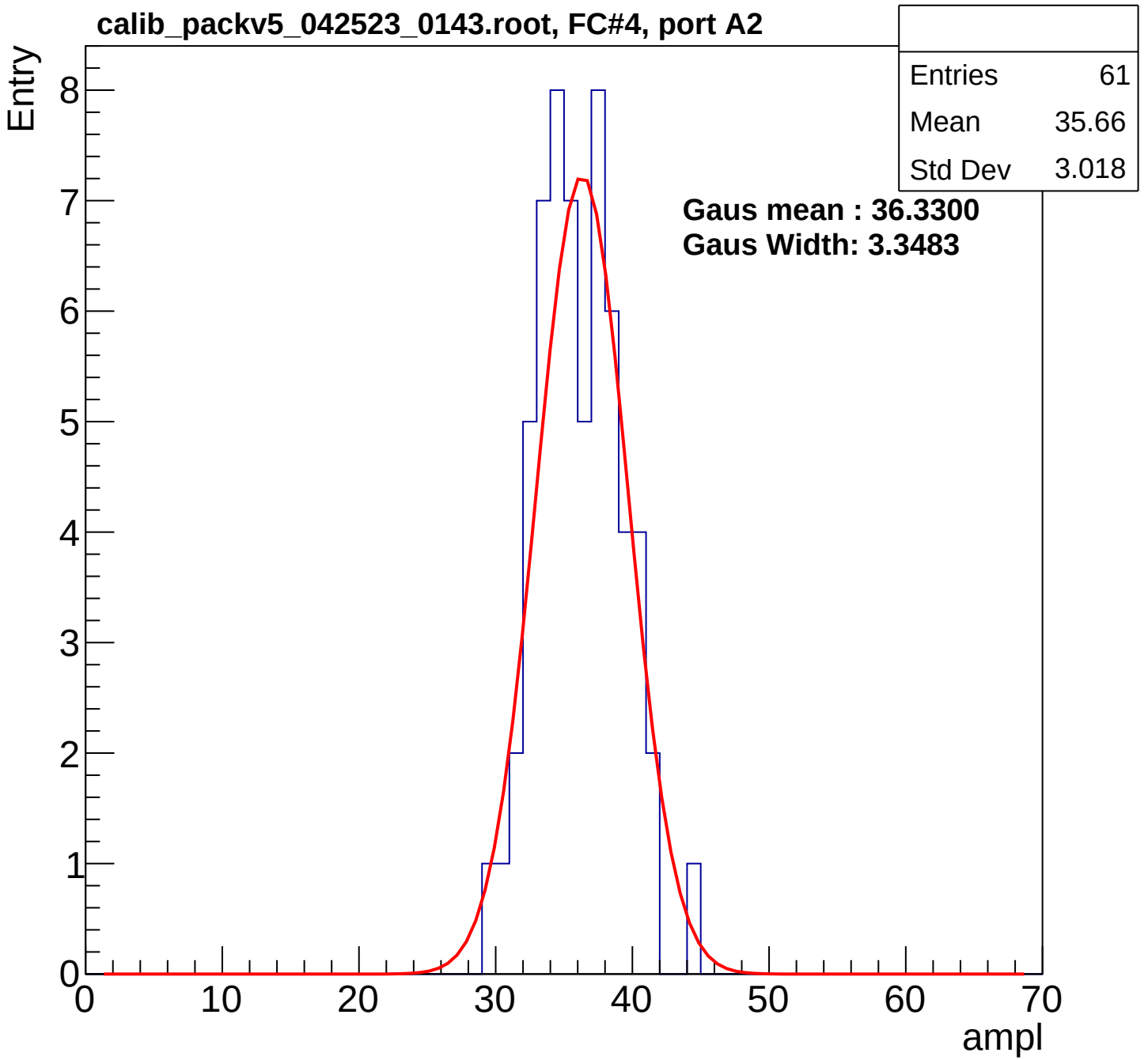
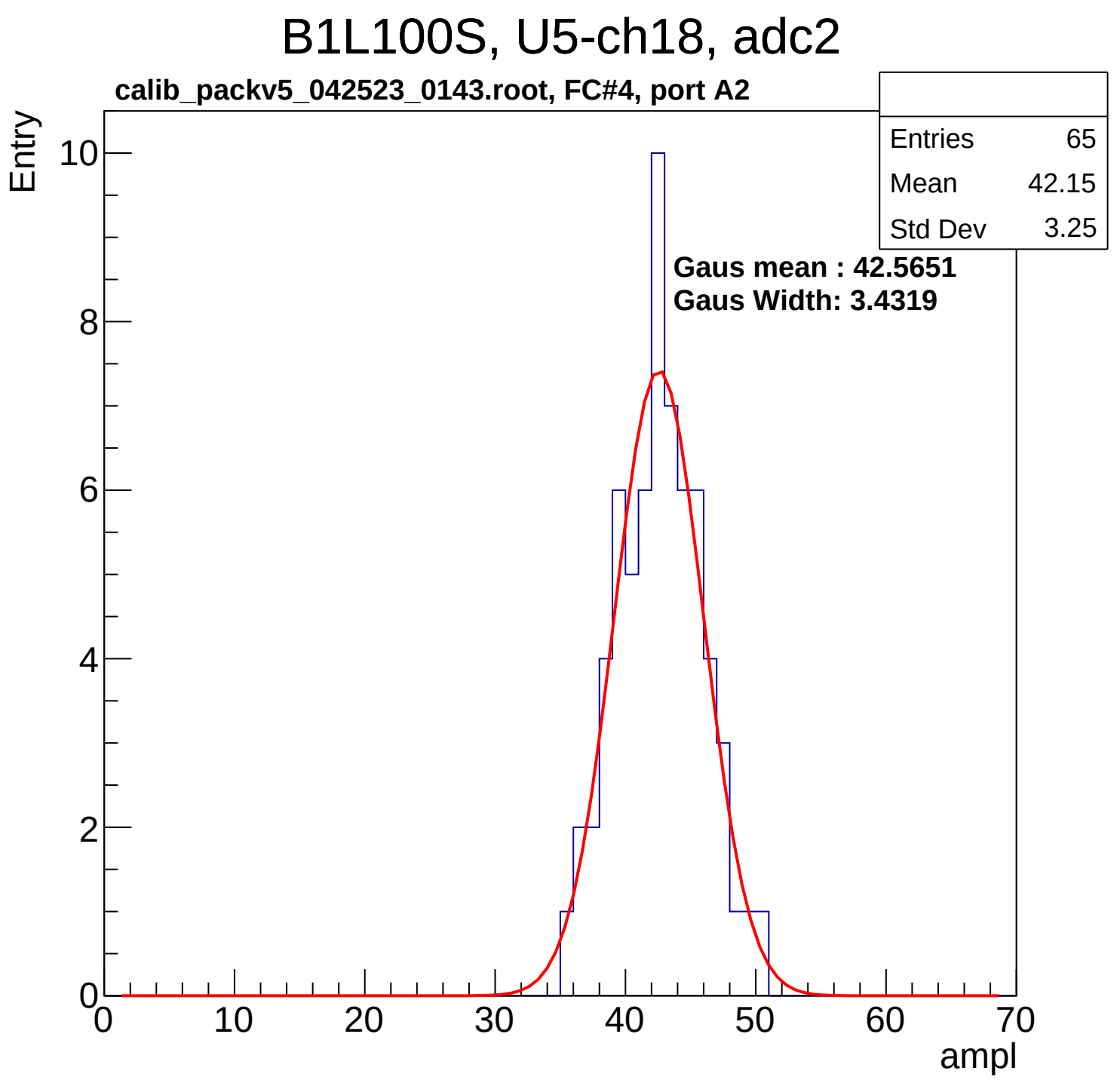
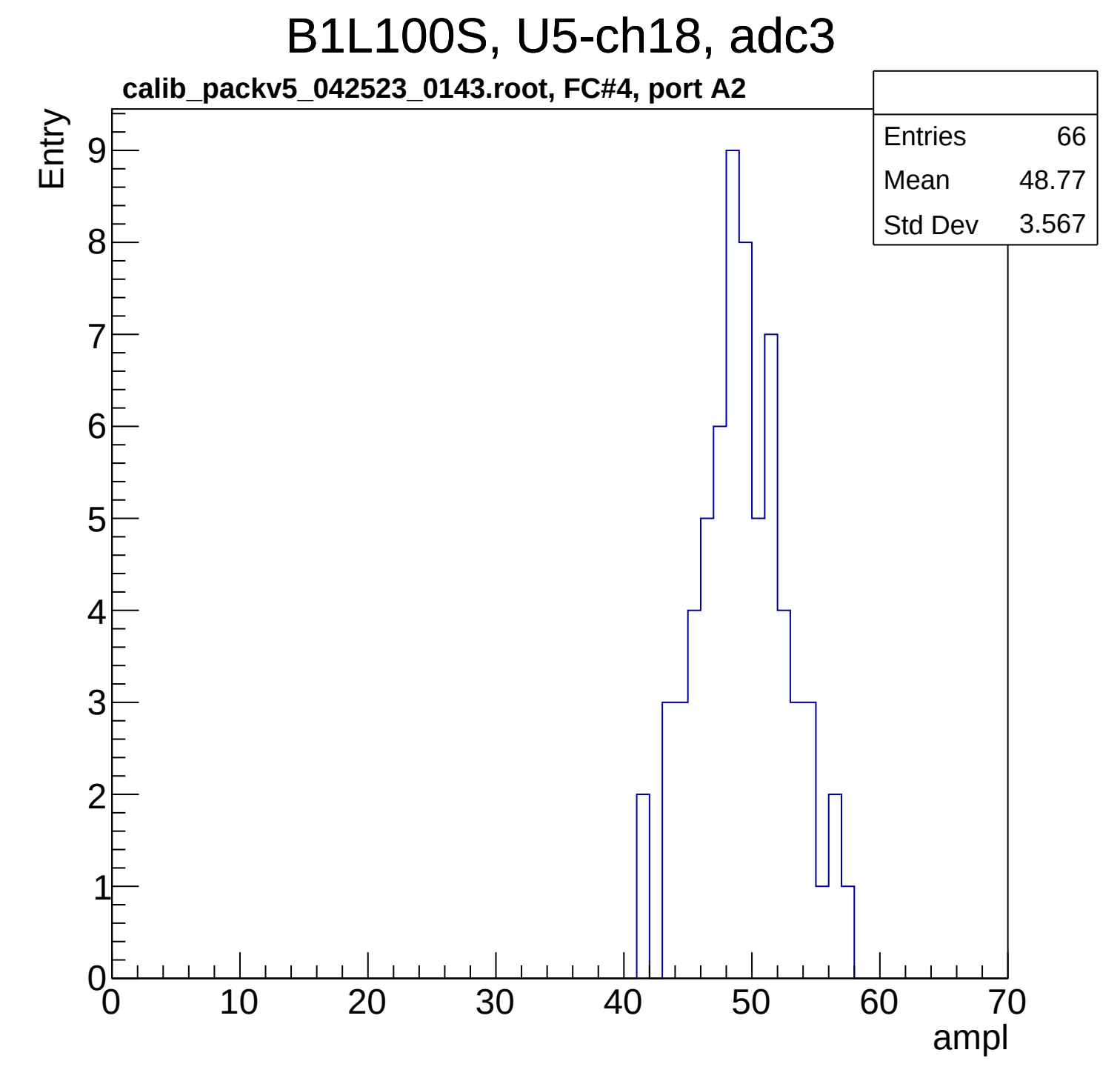
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch18, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 35.66
Std Dev 3.018
Gaus mean : 36.3300
Gaus Width: 3.3483
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch18, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 42.15
Std Dev 3.25
Gaus mean : 42.5651
Gaus Width: 3.4319
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch18, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 48.77
Std Dev 3.567
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
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60
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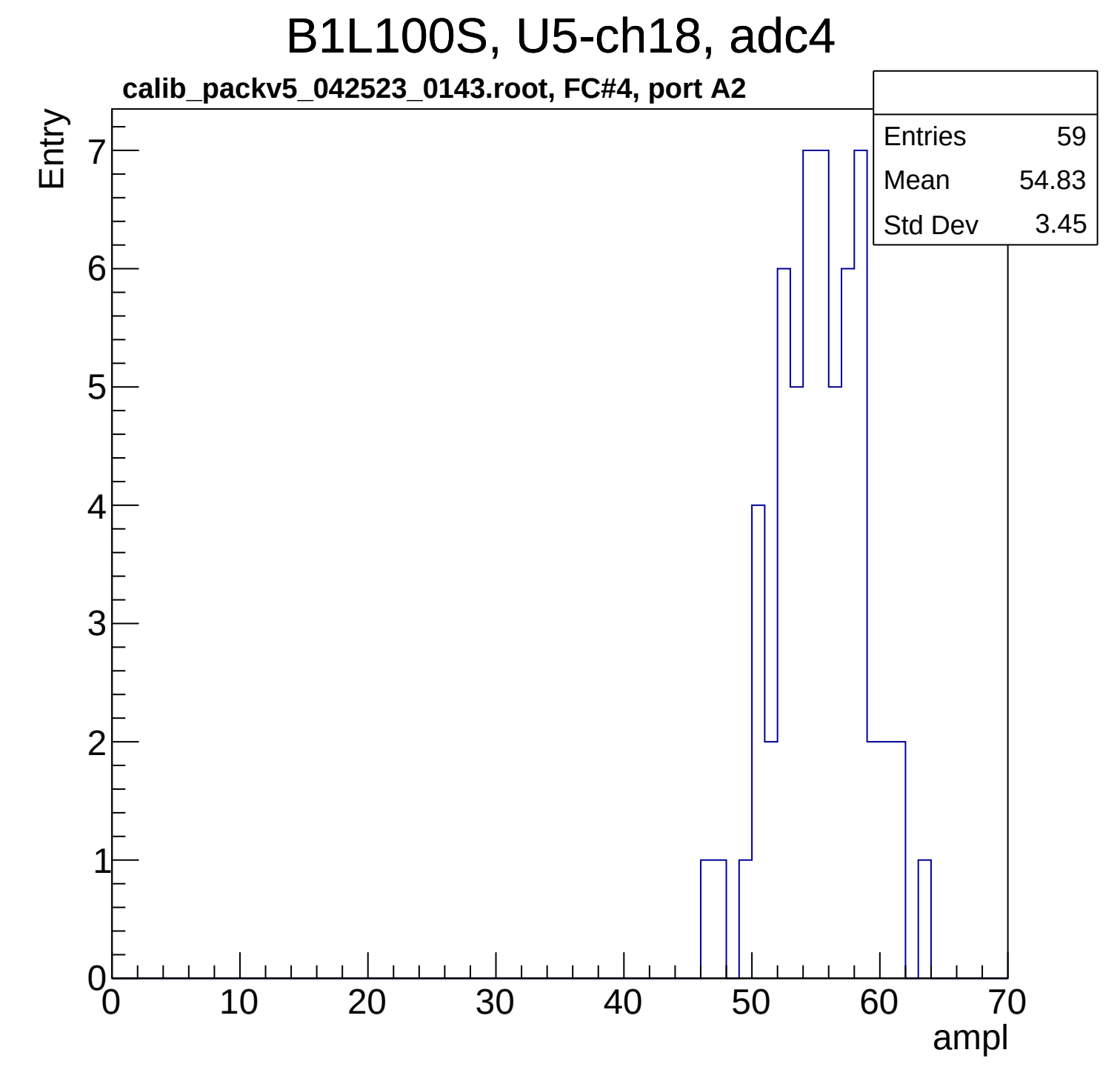
B1L100S, U5-ch18, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 54.83
Std Dev 3.45
Entry
ampl
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1
2
3
4
5
6
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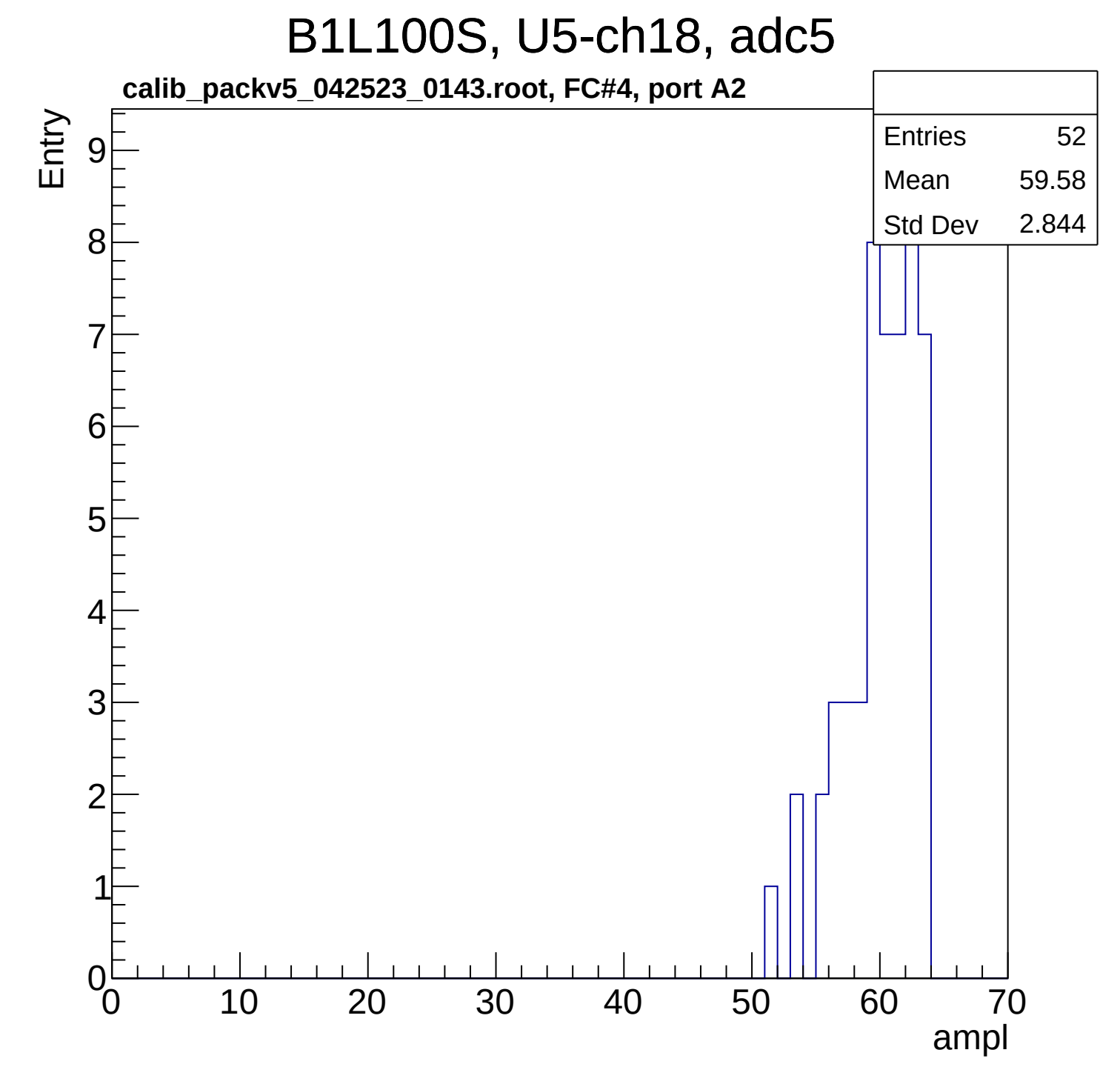
0
10
20
30
40
50
60
70


B1L100S, U5-ch18, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 52
Mean 59.58
Std Dev 2.844
Entry
ampl
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2
3
4
5
6
7
8
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0
10
20
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40
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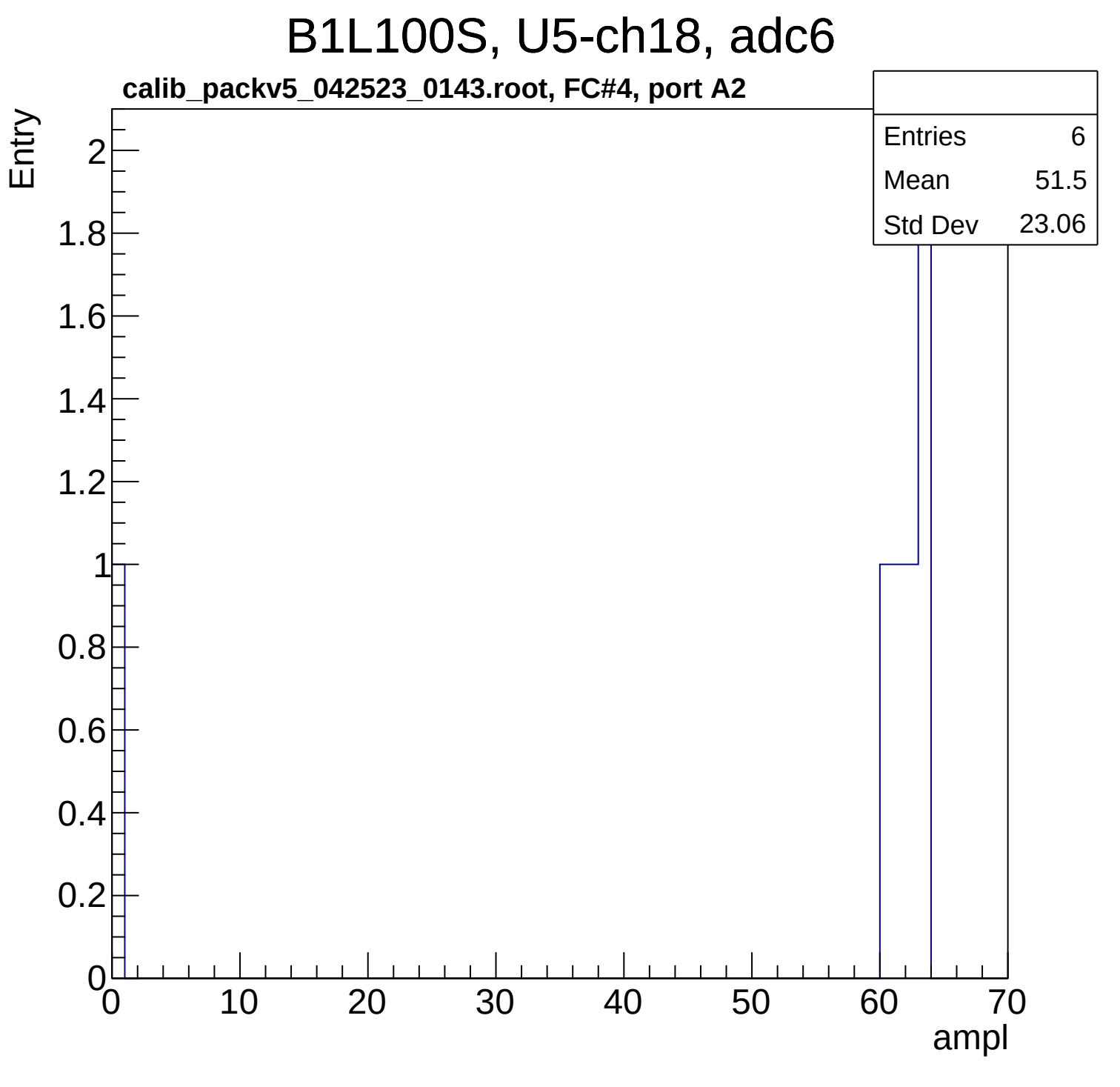
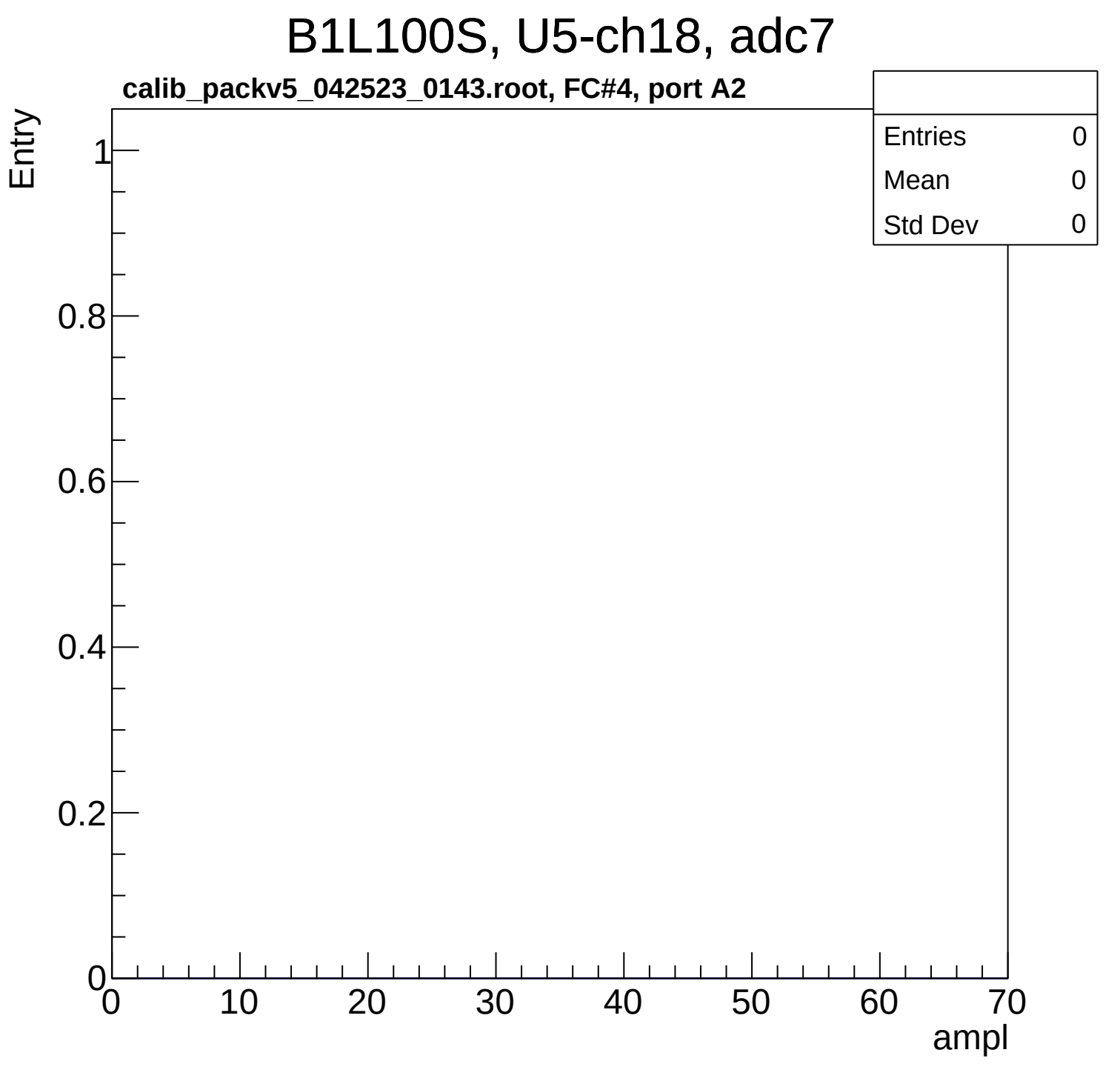
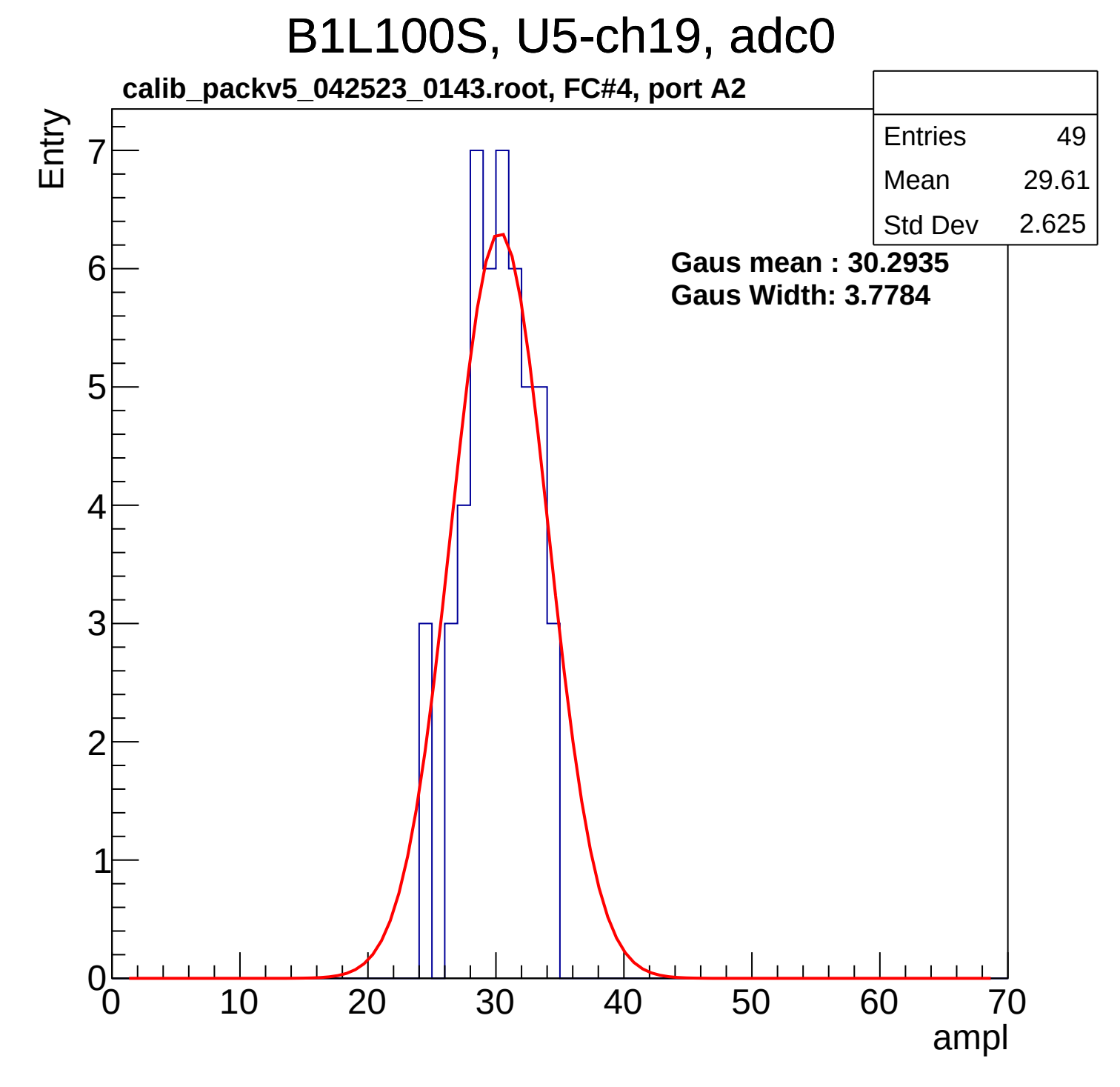
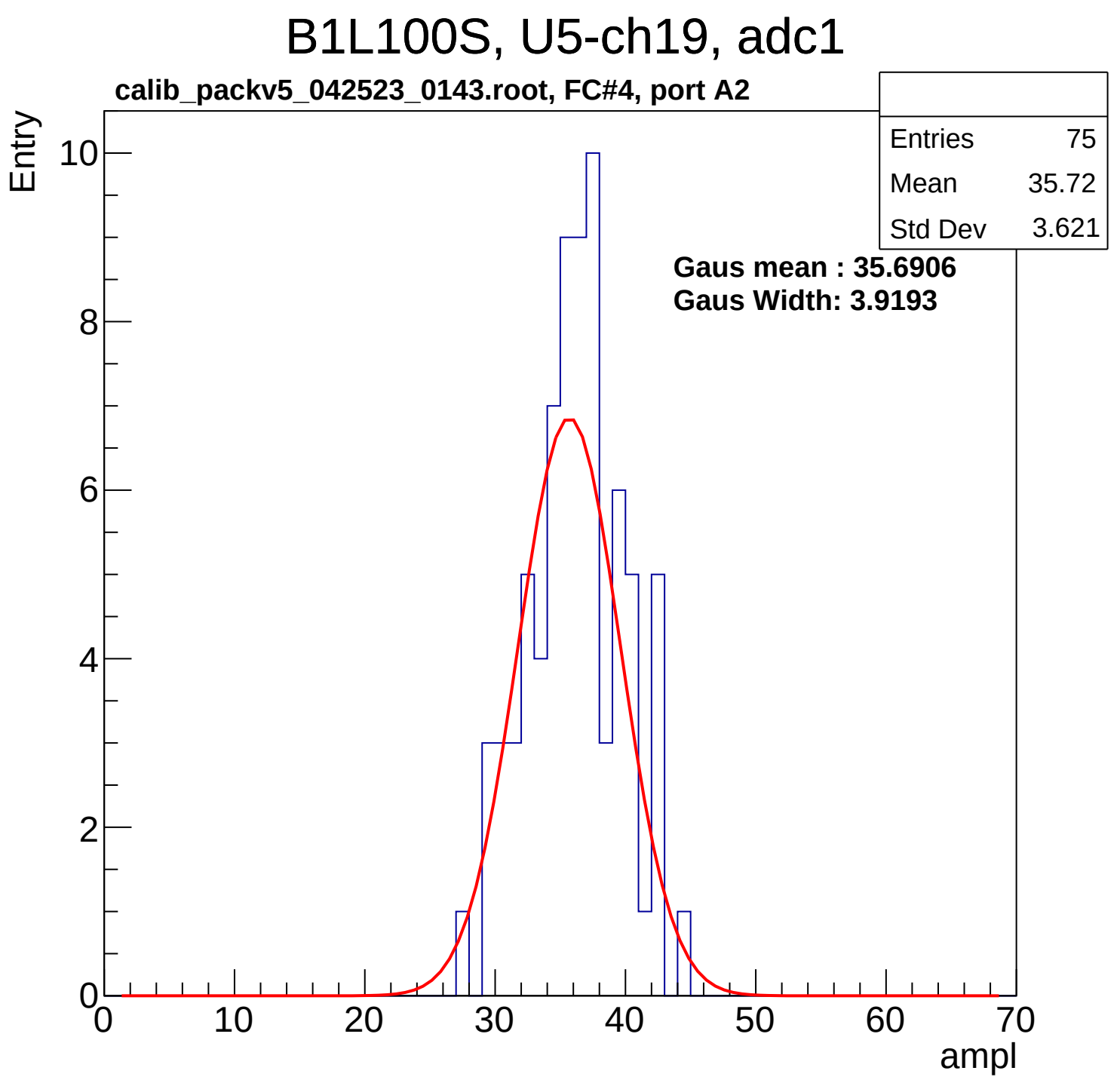
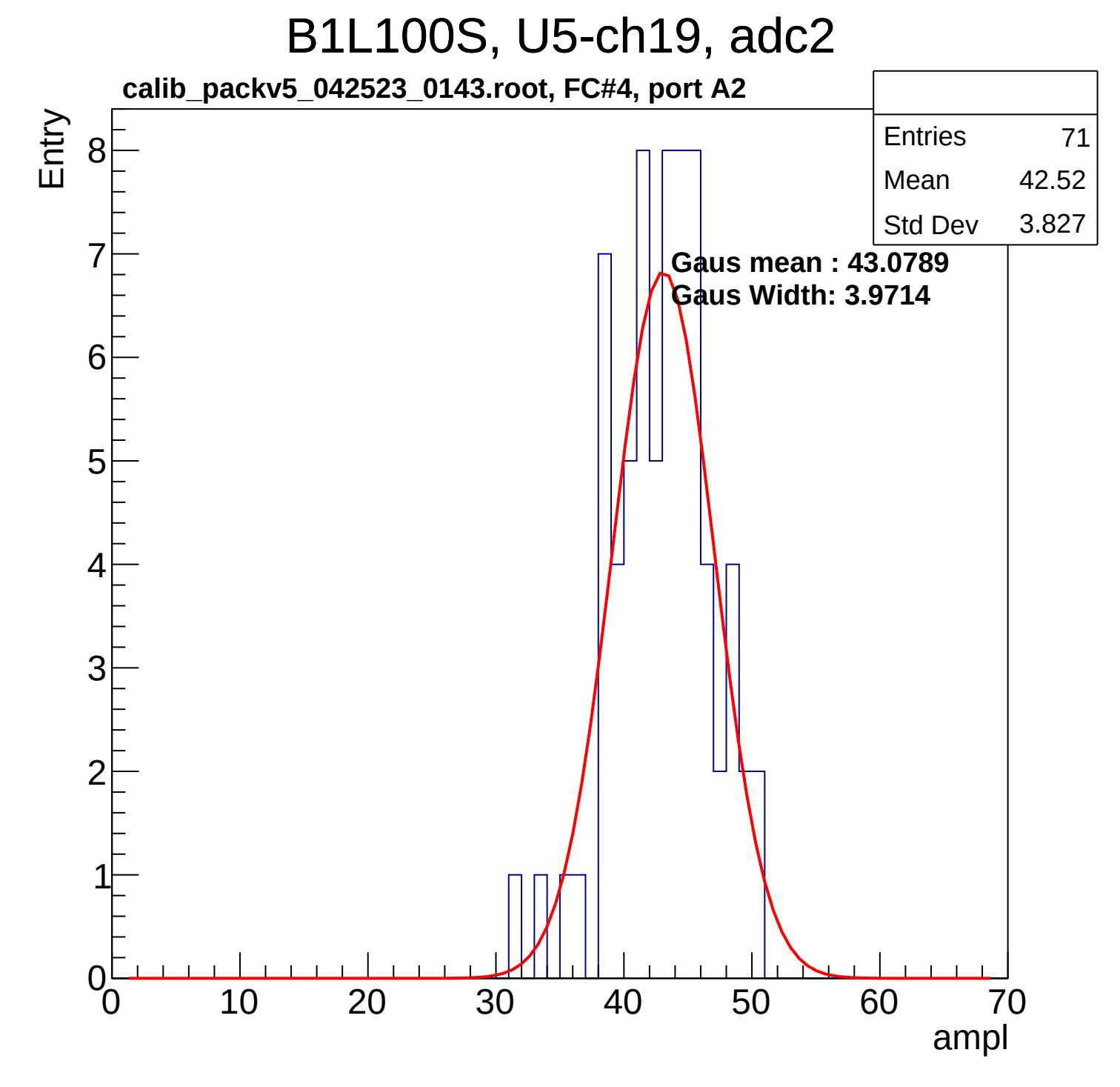
70

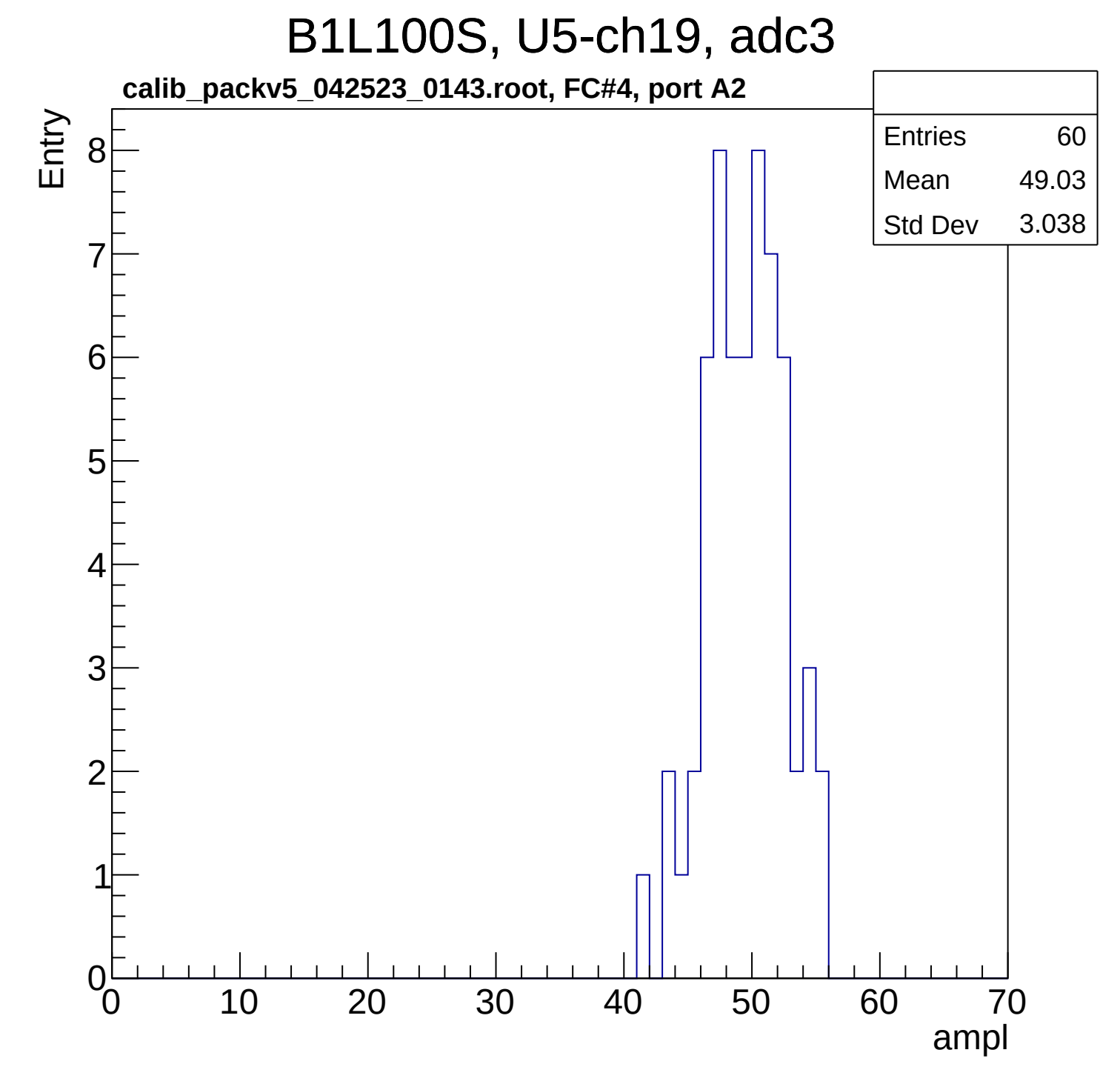

B1L100S, U5-ch18, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 6
Mean 51.5
Std Dev 23.06
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

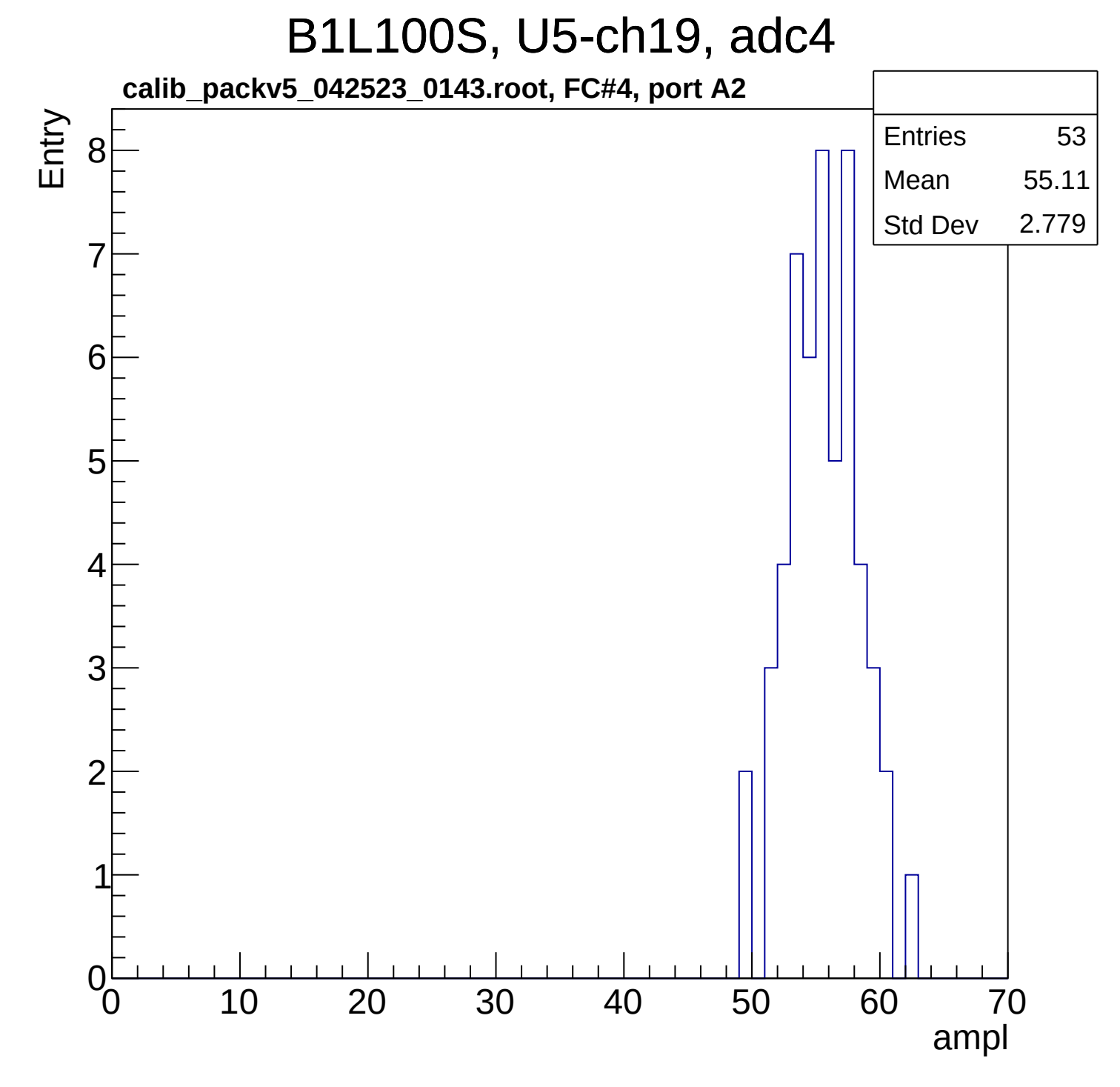

B1L100S, U5-ch18, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

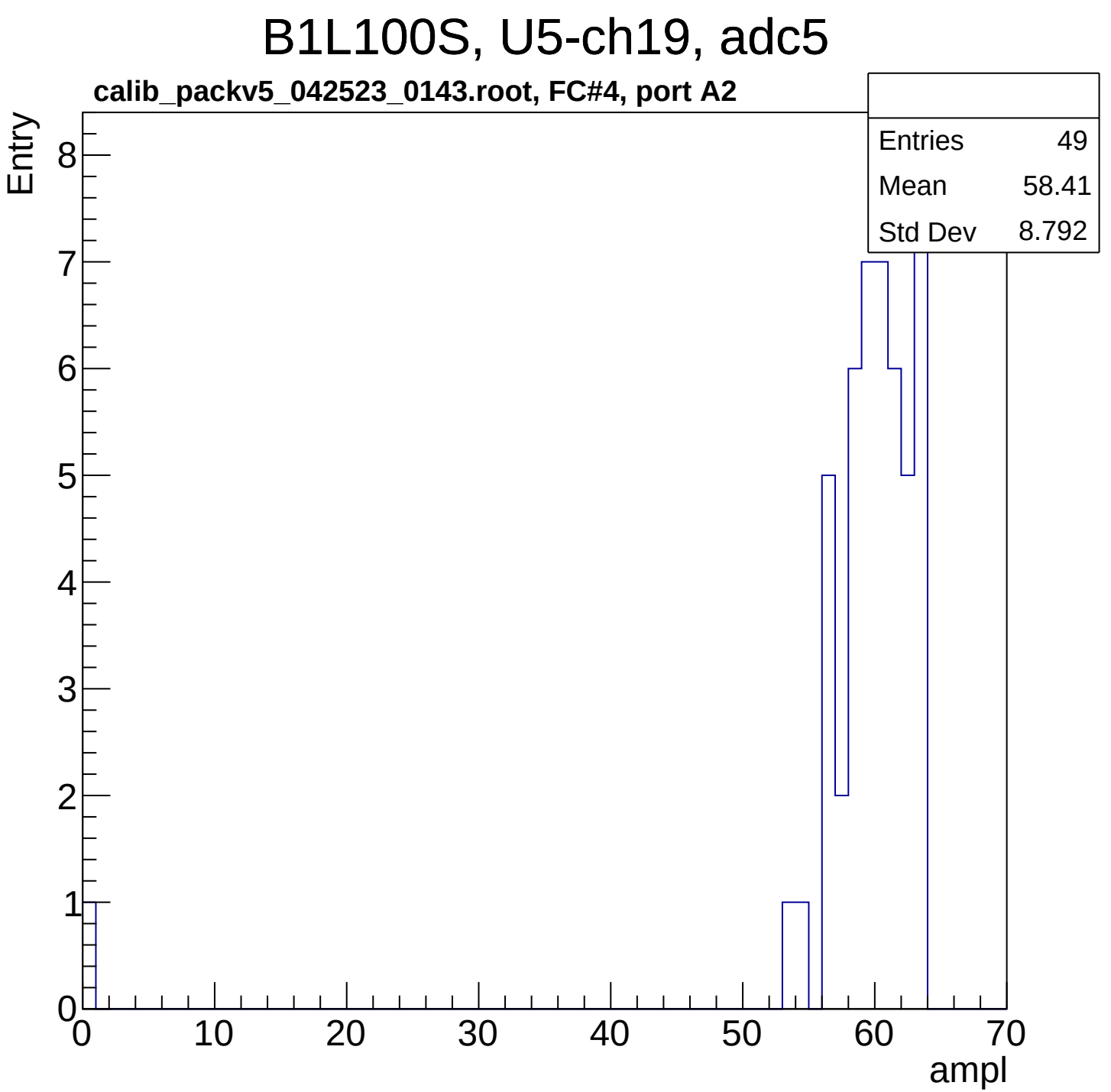

B1L100S, U5-ch19, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 49
Mean 29.61
Std Dev 2.625
Gaus mean : 30.2935
Gaus Width: 3.7784
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

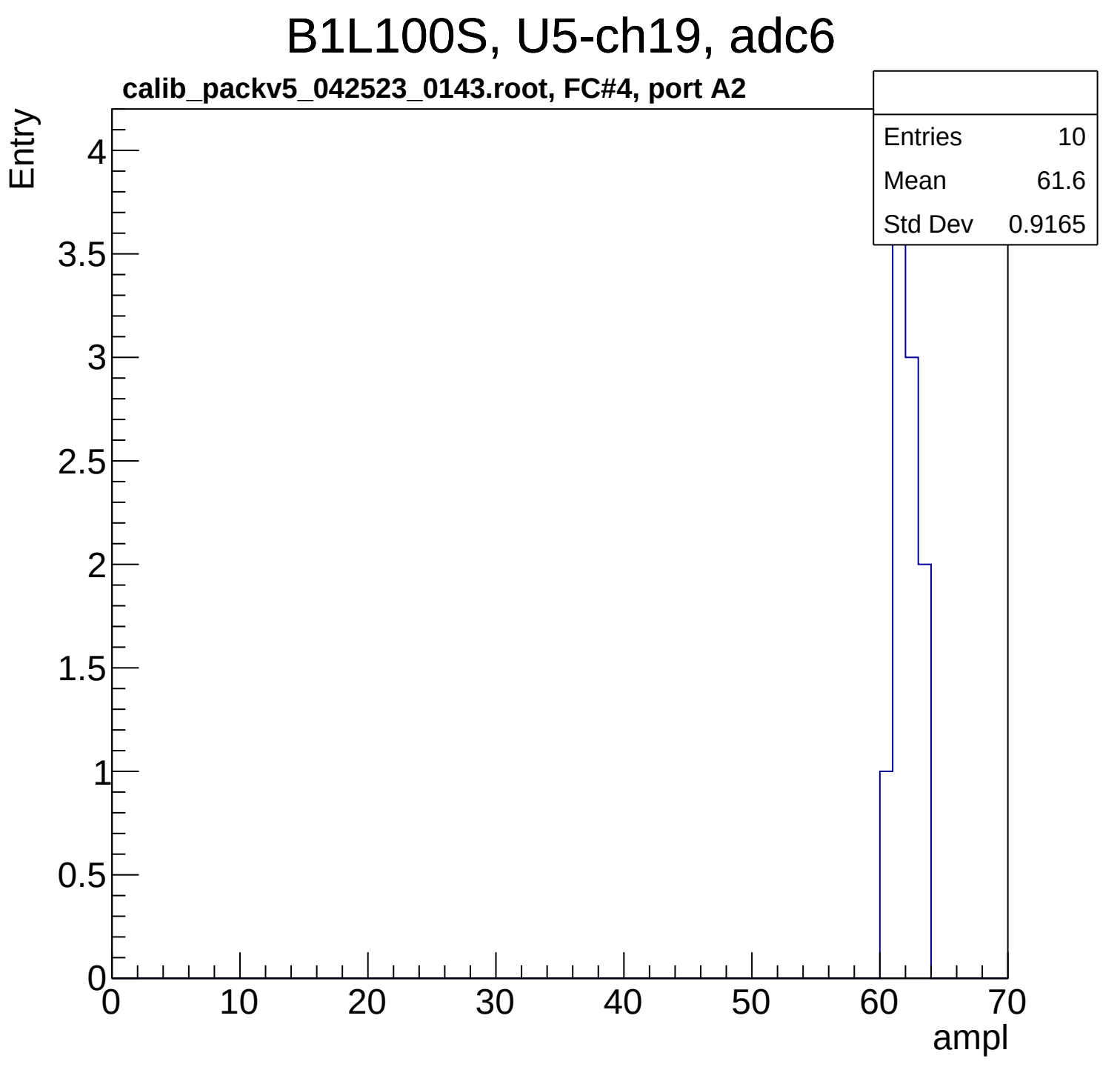

B1L100S, U5-ch19, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 75
Mean 35.72
Std Dev 3.621
Gaus mean : 35.6906
Gaus Width: 3.9193
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

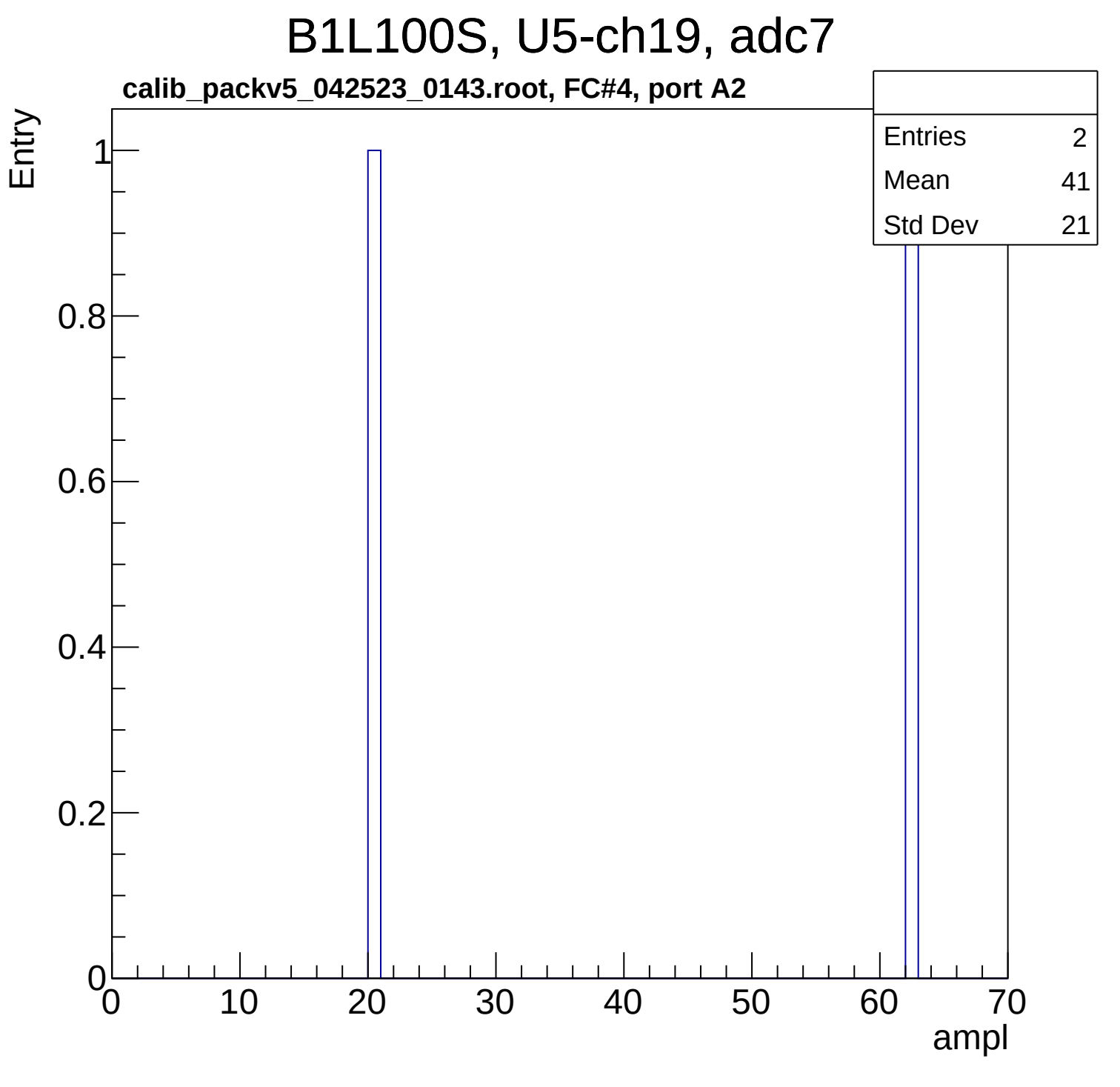

B1L100S, U5-ch19, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 42.52
Std Dev 3.827
Gaus mean : 43.0789
Gaus Width: 3.9714
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

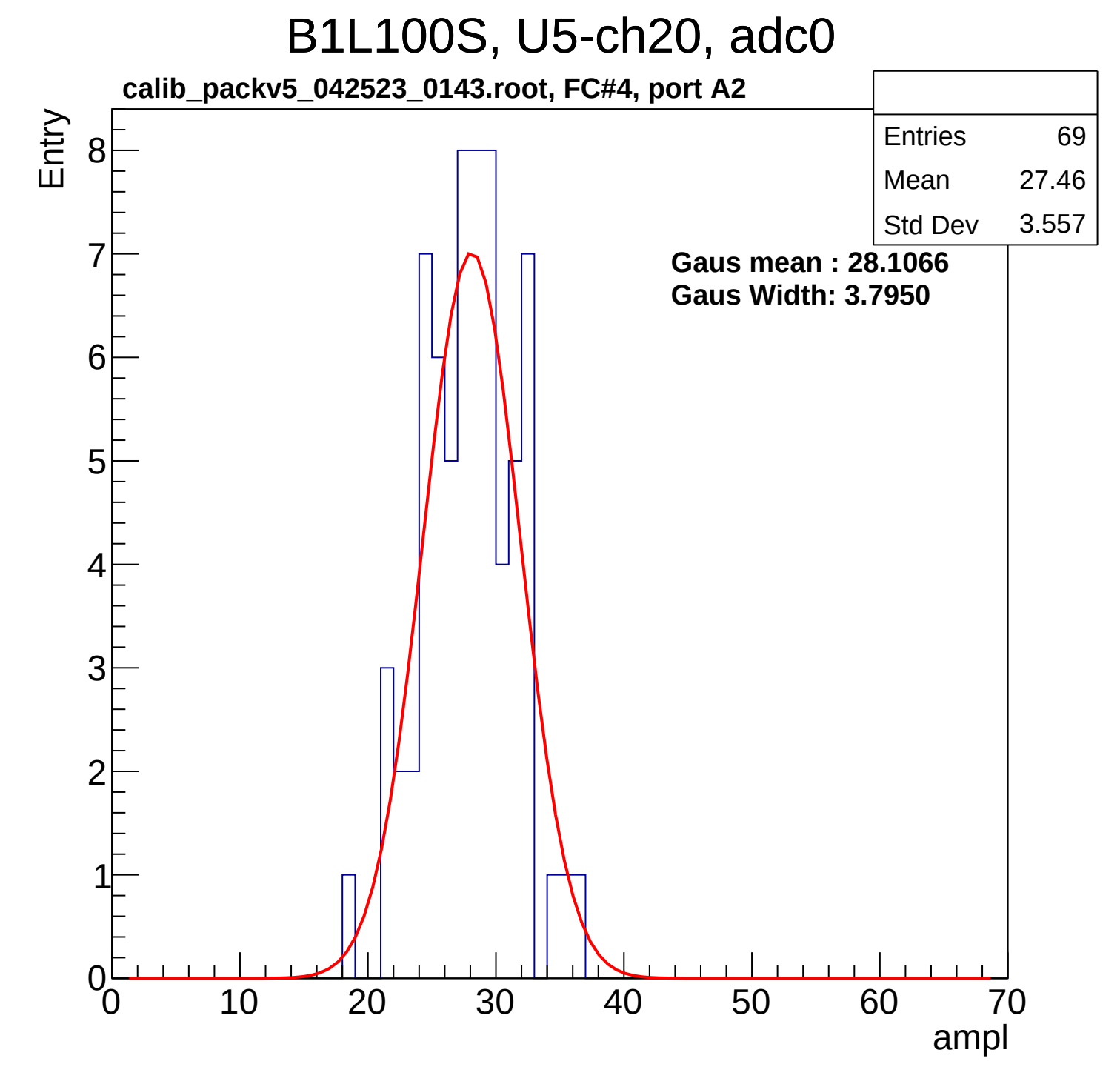

B1L100S, U5-ch19, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 49.03
Std Dev 3.038
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

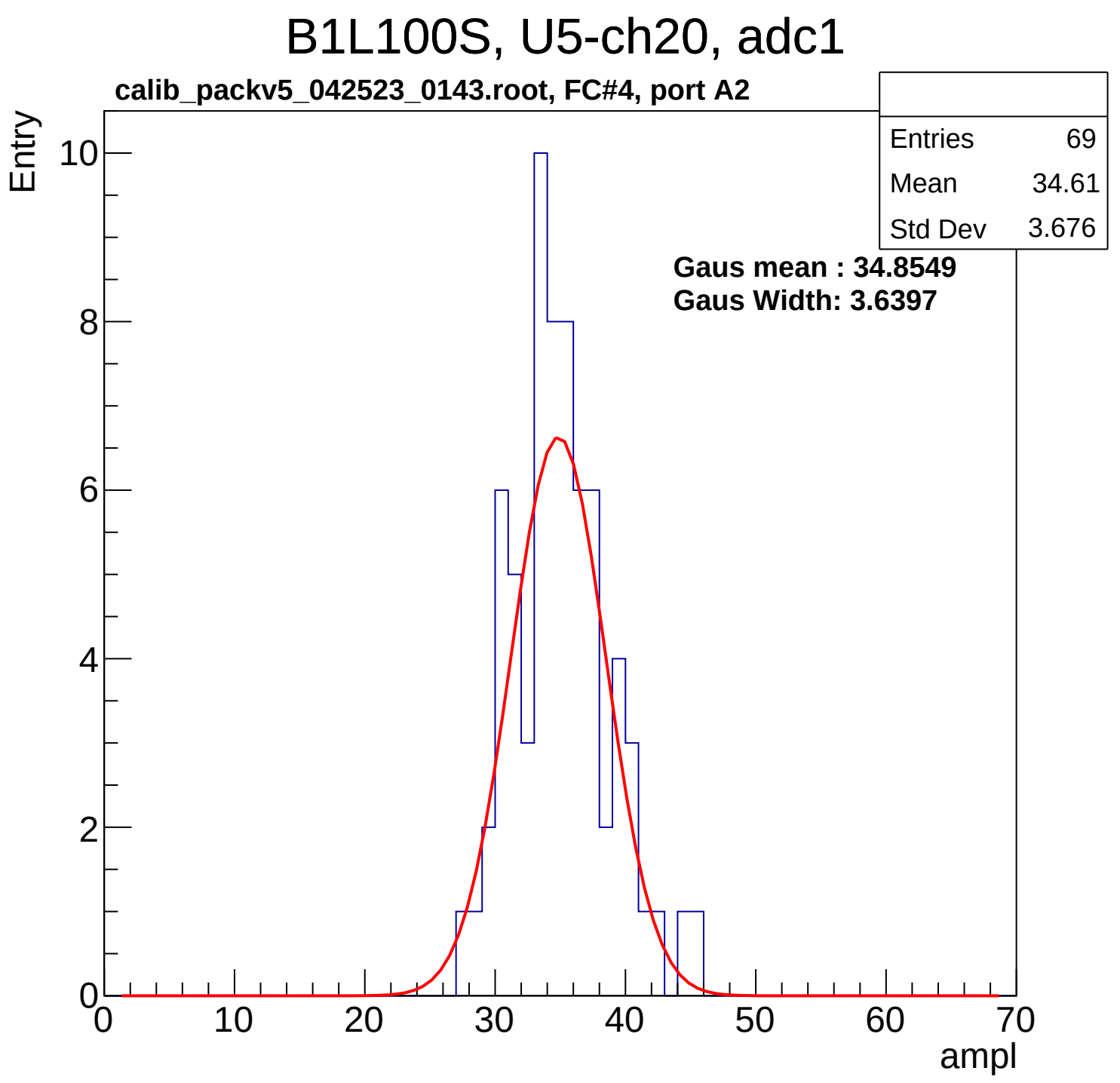

B1L100S, U5-ch19, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 55.11
Std Dev 2.779
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

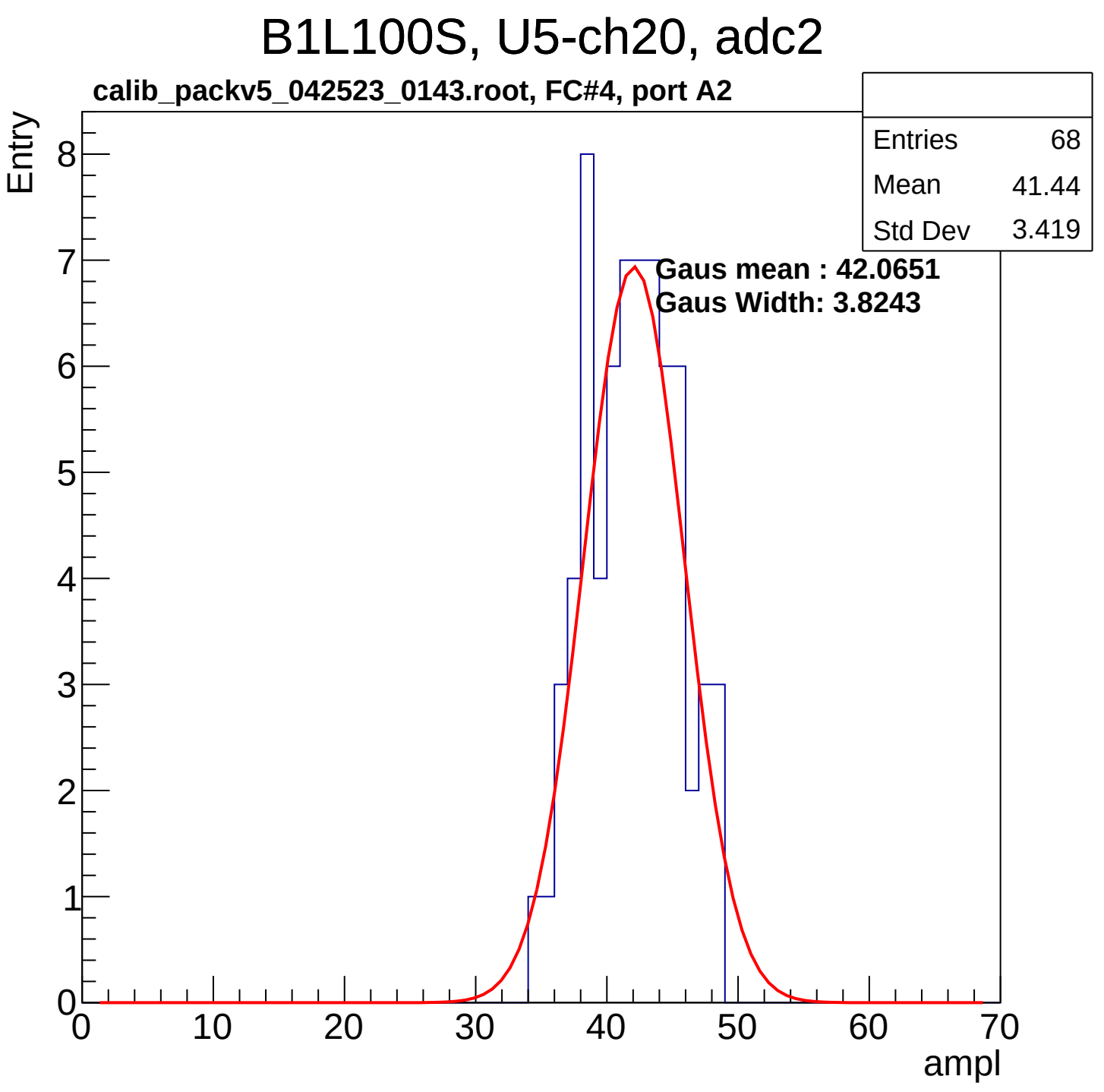

B1L100S, U5-ch19, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 49
Mean 58.41
Std Dev 8.792
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

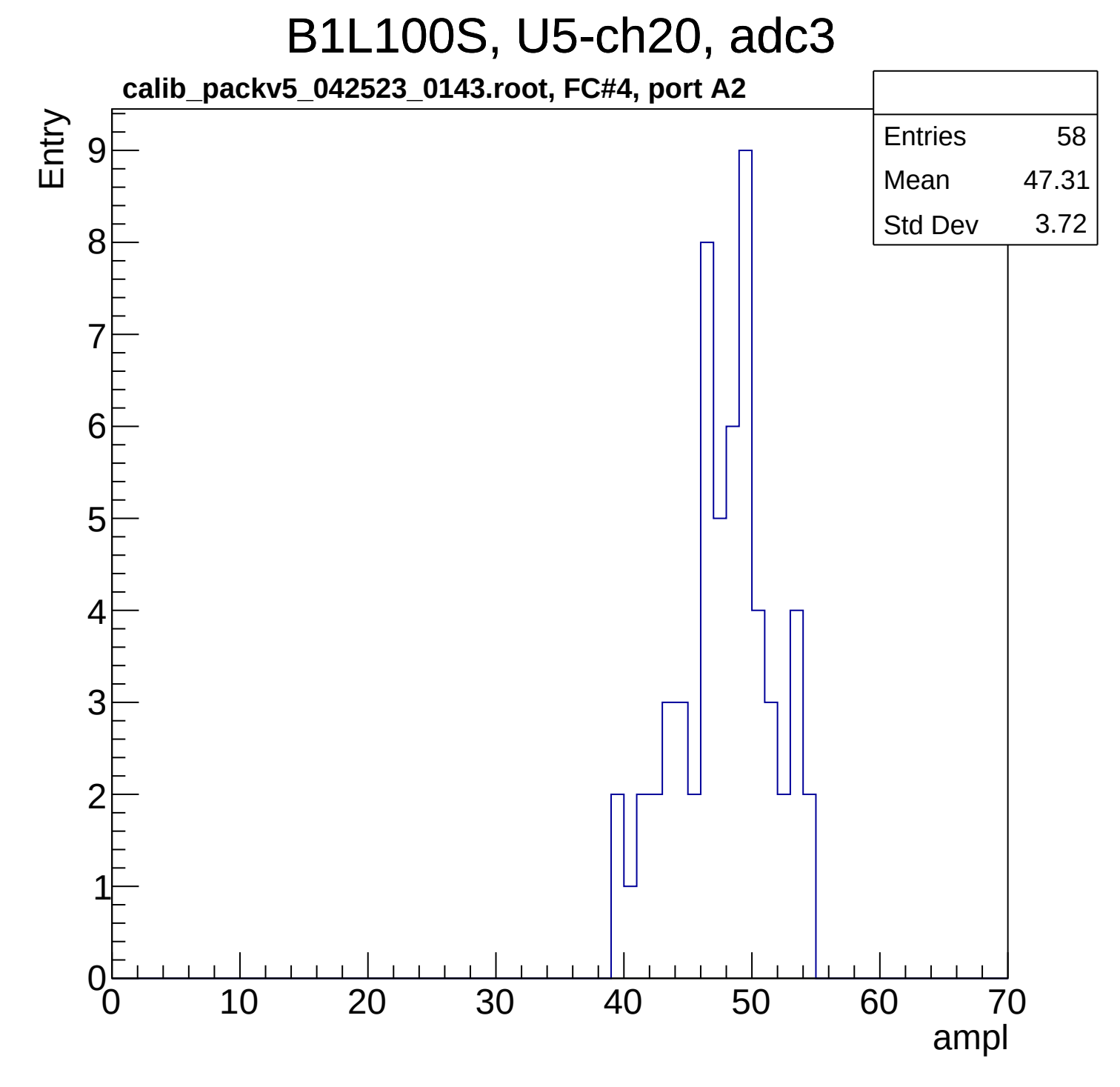

B1L100S, U5-ch19, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 10
Mean 61.6
Std Dev 0.9165
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

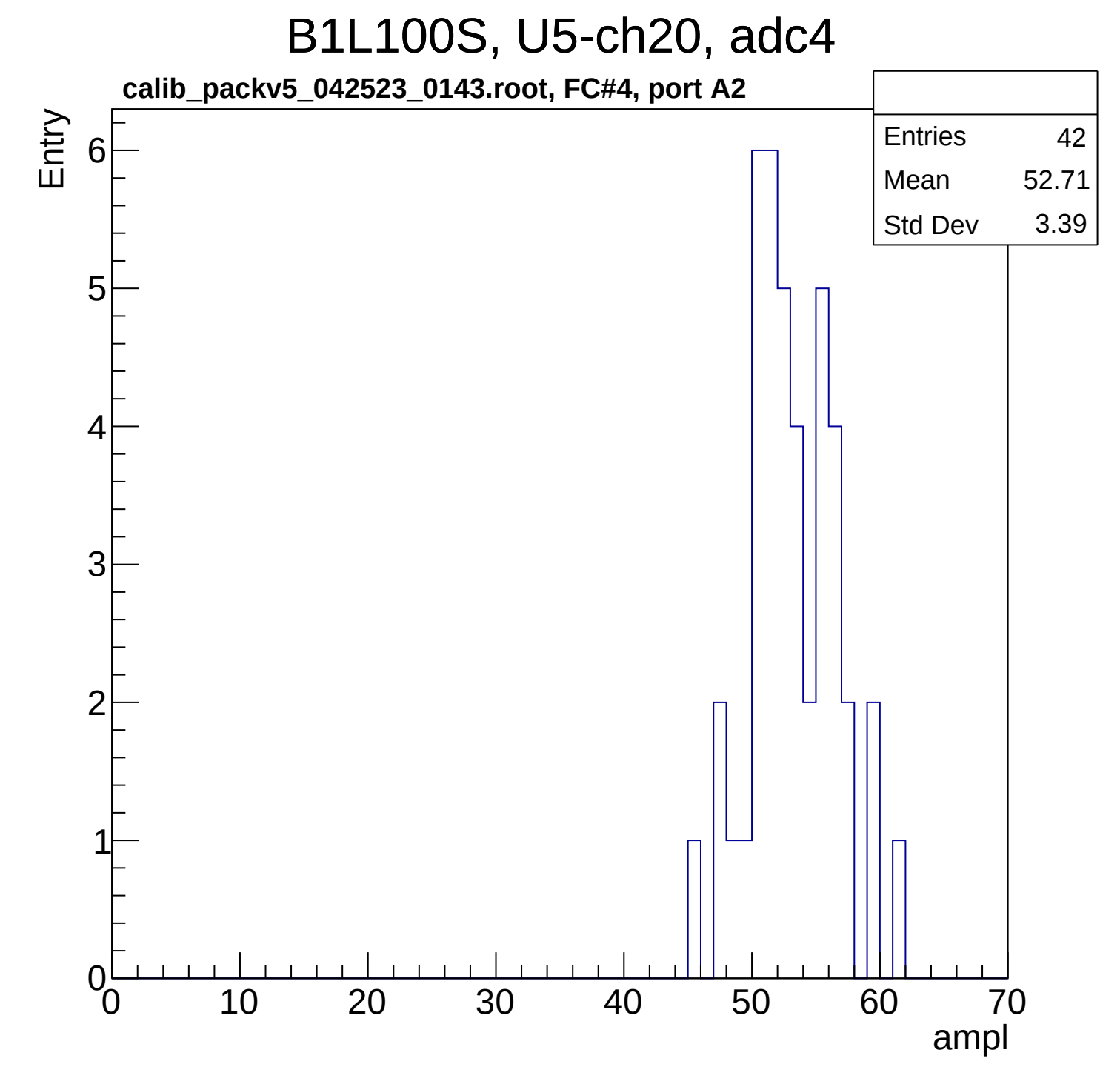

B1L100S, U5-ch19, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 41
Std Dev 21
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

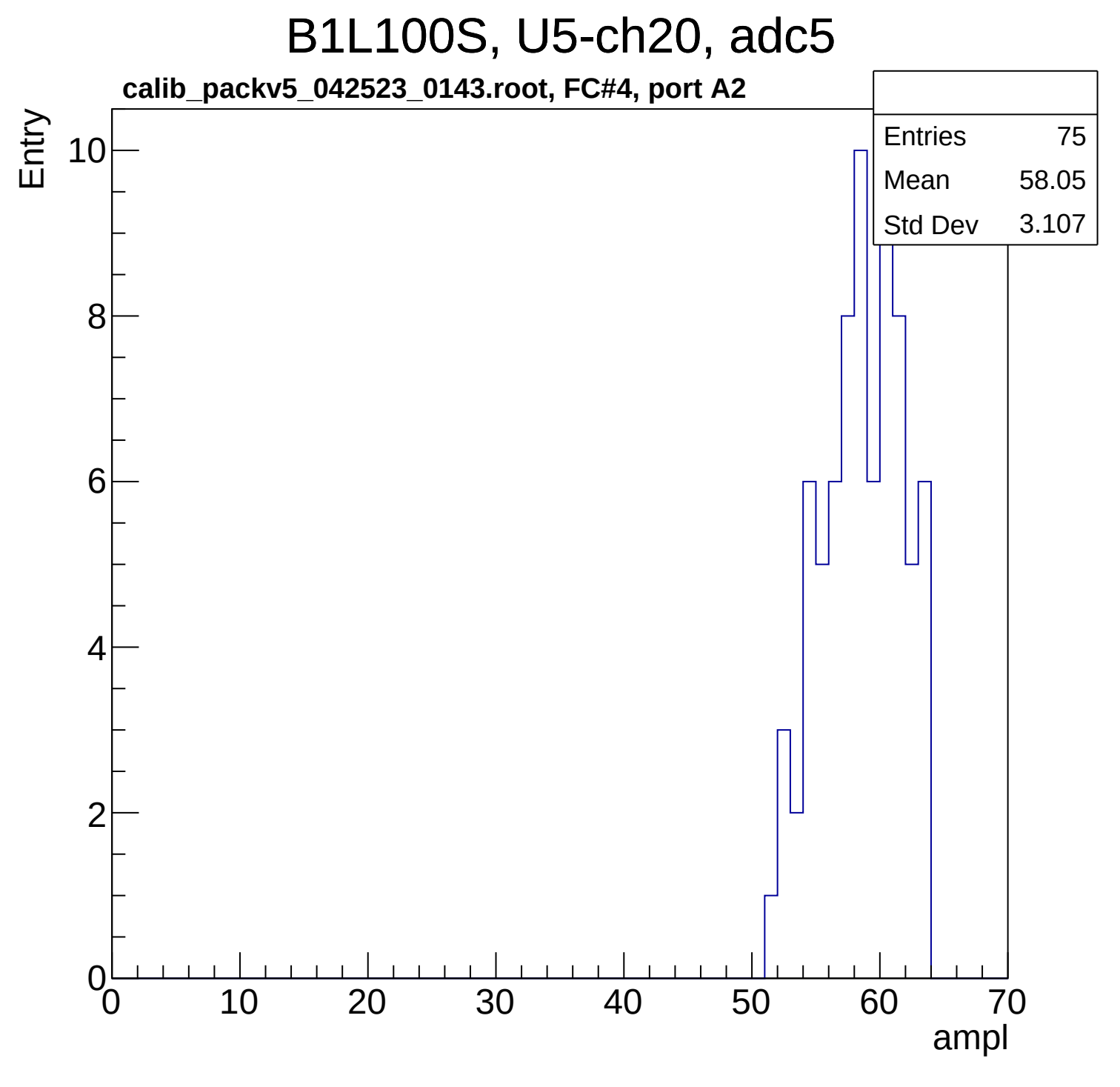

B1L100S, U5-ch20, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 27.46
Std Dev 3.557
Gaus mean : 28.1066
Gaus Width: 3.7950
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

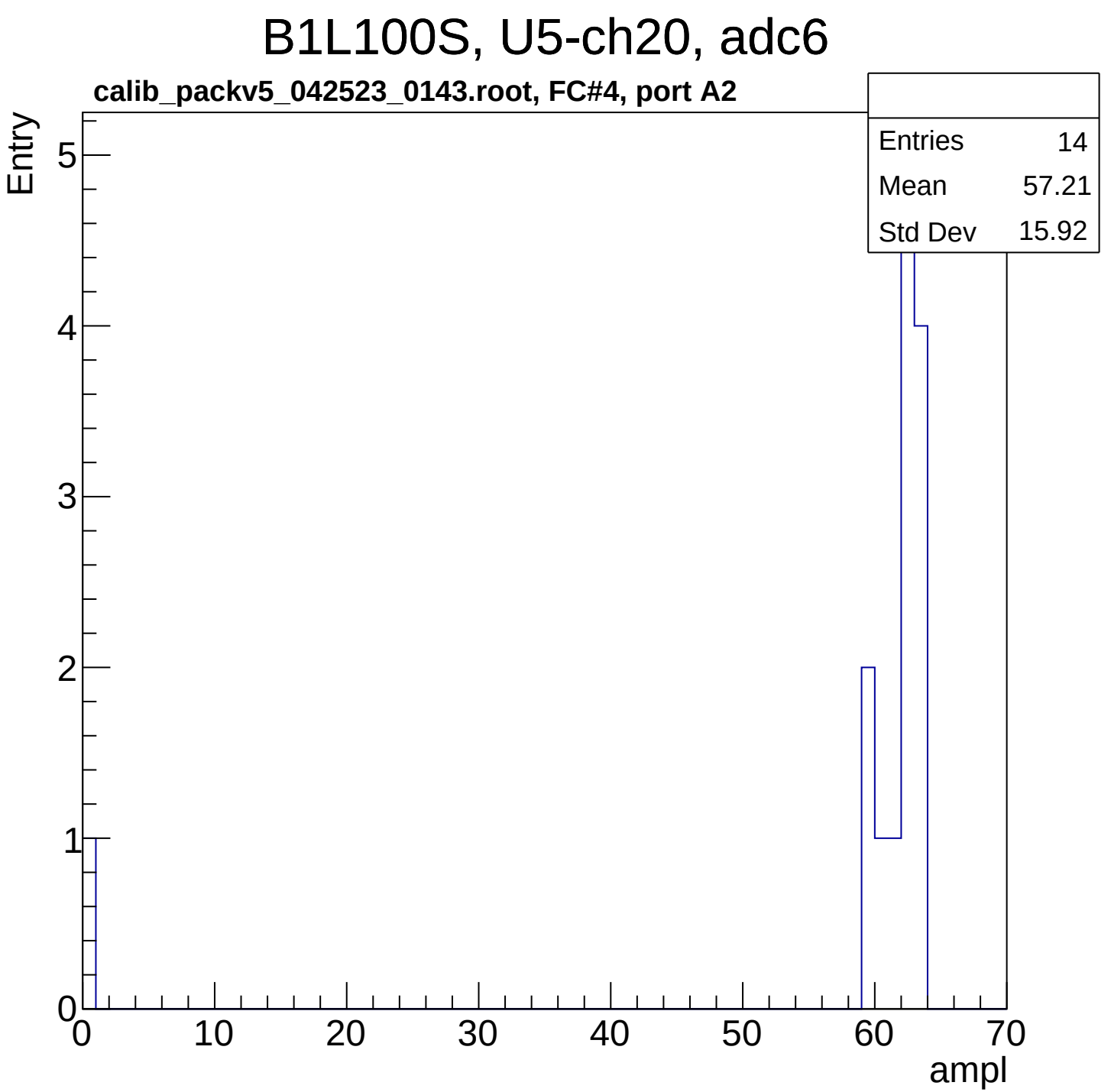

B1L100S, U5-ch20, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 34.61
Std Dev 3.676
Gaus mean : 34.8549
Gaus Width: 3.6397
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

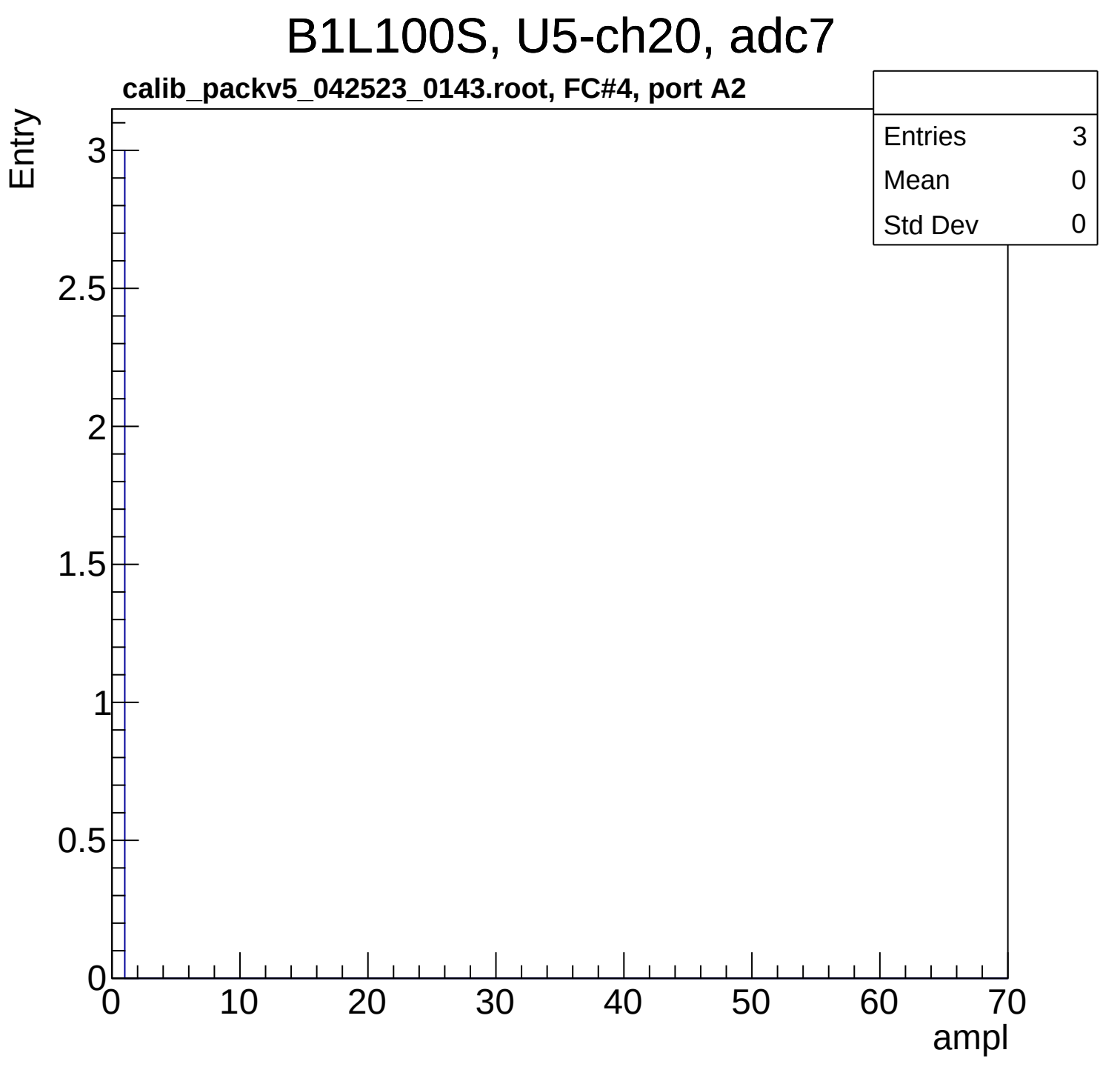

B1L100S, U5-ch20, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 41.44
Std Dev 3.419
Gaus mean : 42.0651
Gaus Width: 3.8243
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

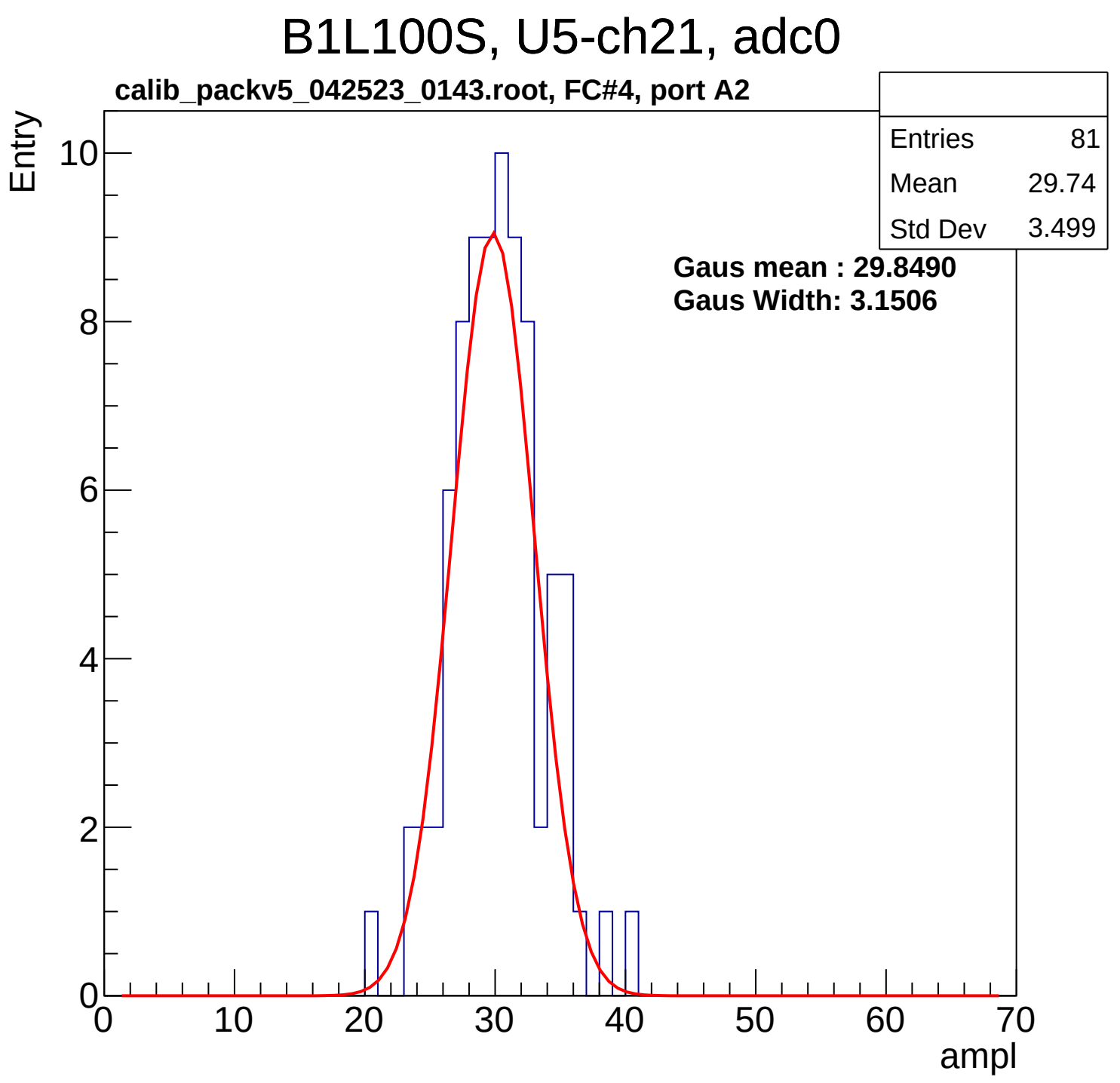

B1L100S, U5-ch20, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 47.31
Std Dev 3.72
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

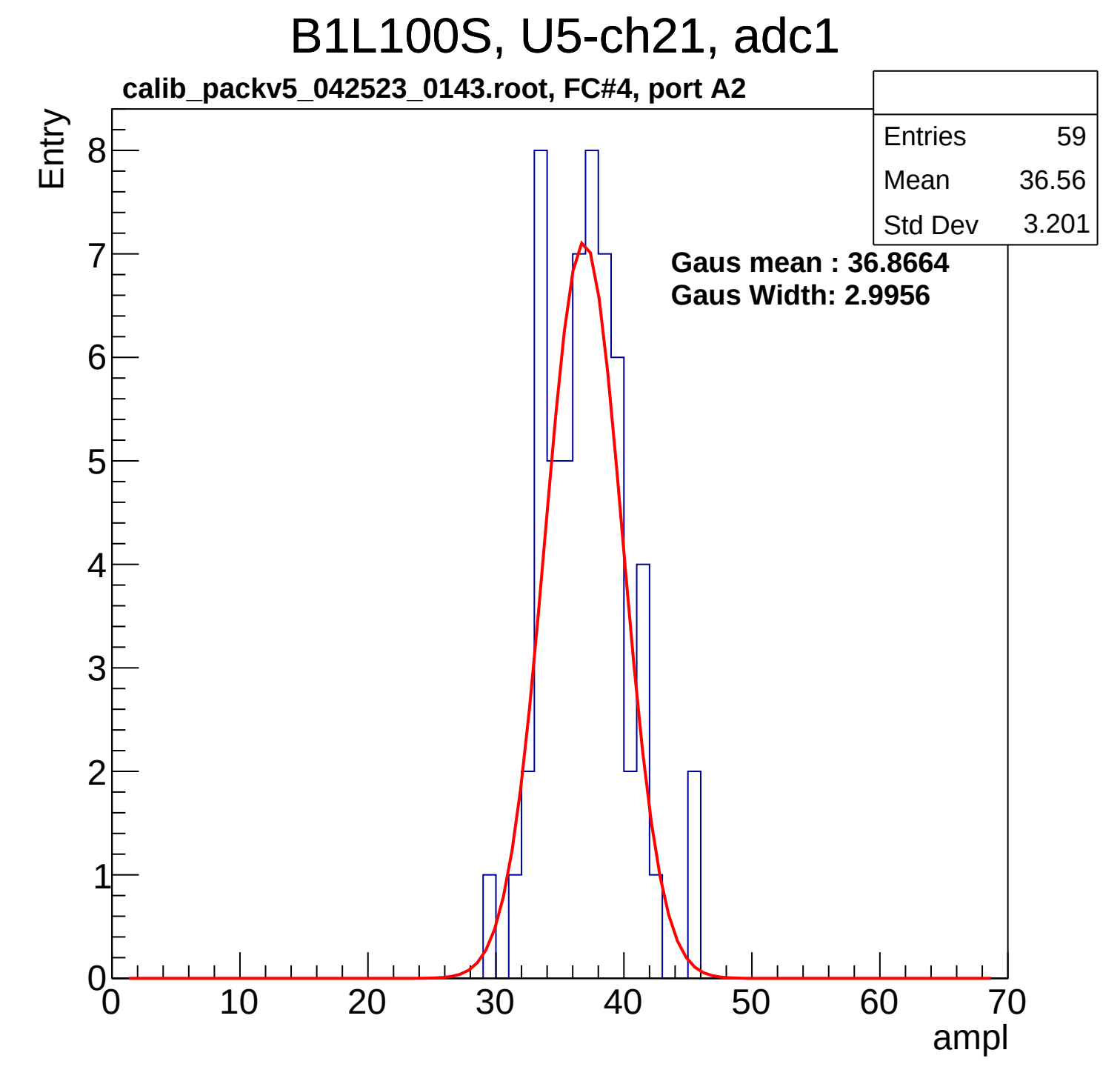

B1L100S, U5-ch20, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 42
Mean 52.71
Std Dev 3.39
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

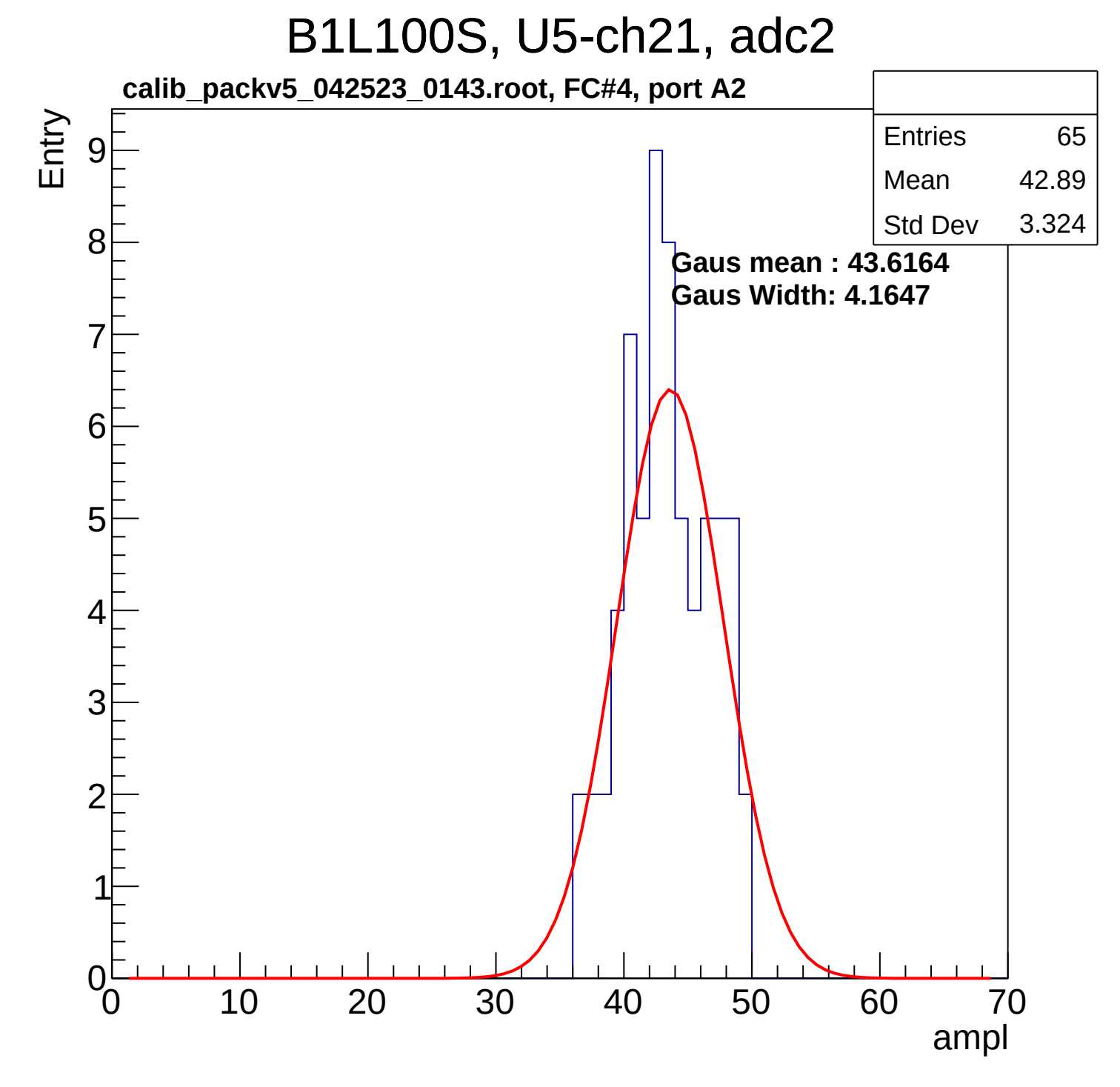

B1L100S, U5-ch20, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 75
Mean 58.05
Std Dev 3.107
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

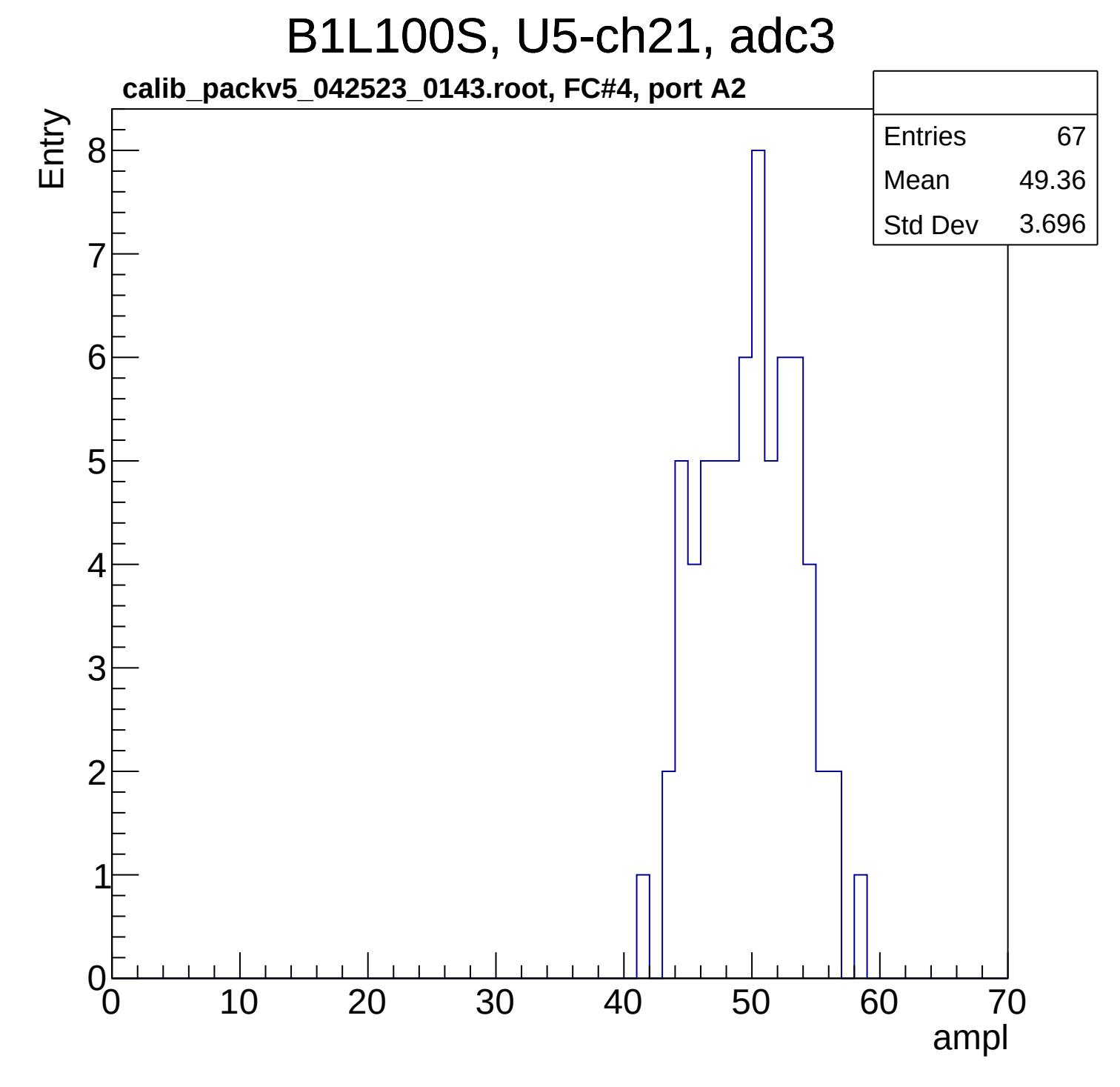

B1L100S, U5-ch20, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 14
Mean 57.21
Std Dev 15.92
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch20, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 0
Std Dev 0
Entry
3
2.5
2
1.5
1
0.5
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch21, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 81
Mean 29.74
Std Dev 3.499
Gaus mean : 29.8490
Gaus Width: 3.1506
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch21, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 36.56
Std Dev 3.201
Gaus mean : 36.8664
Gaus Width: 2.9956
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch21, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 42.89
Std Dev 3.324
Gaus mean : 43.6164
Gaus Width: 4.1647
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch21, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 49.36
Std Dev 3.696
Entry
ampl
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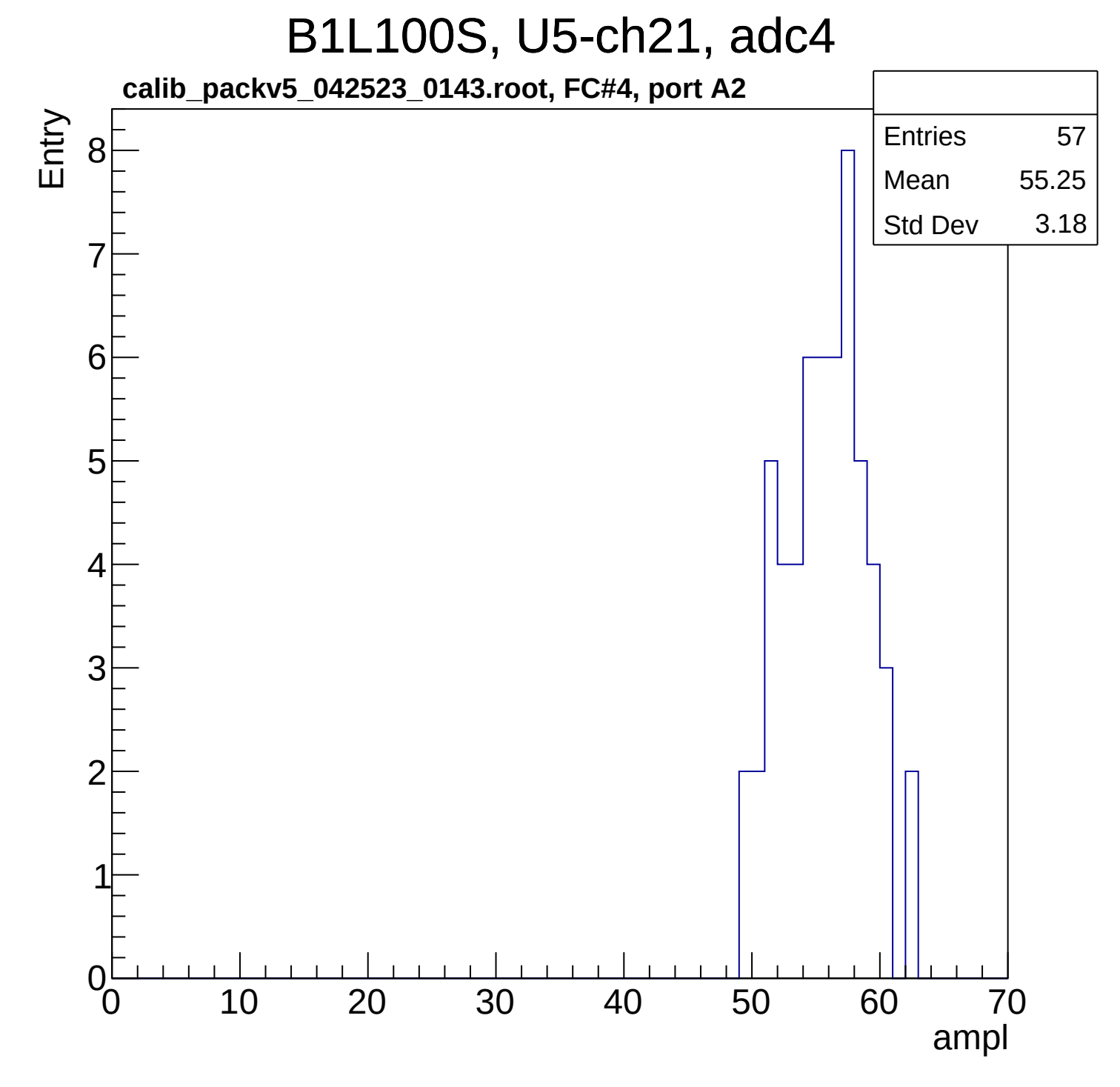
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch21, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 55.25
Std Dev 3.18
Entry
ampl
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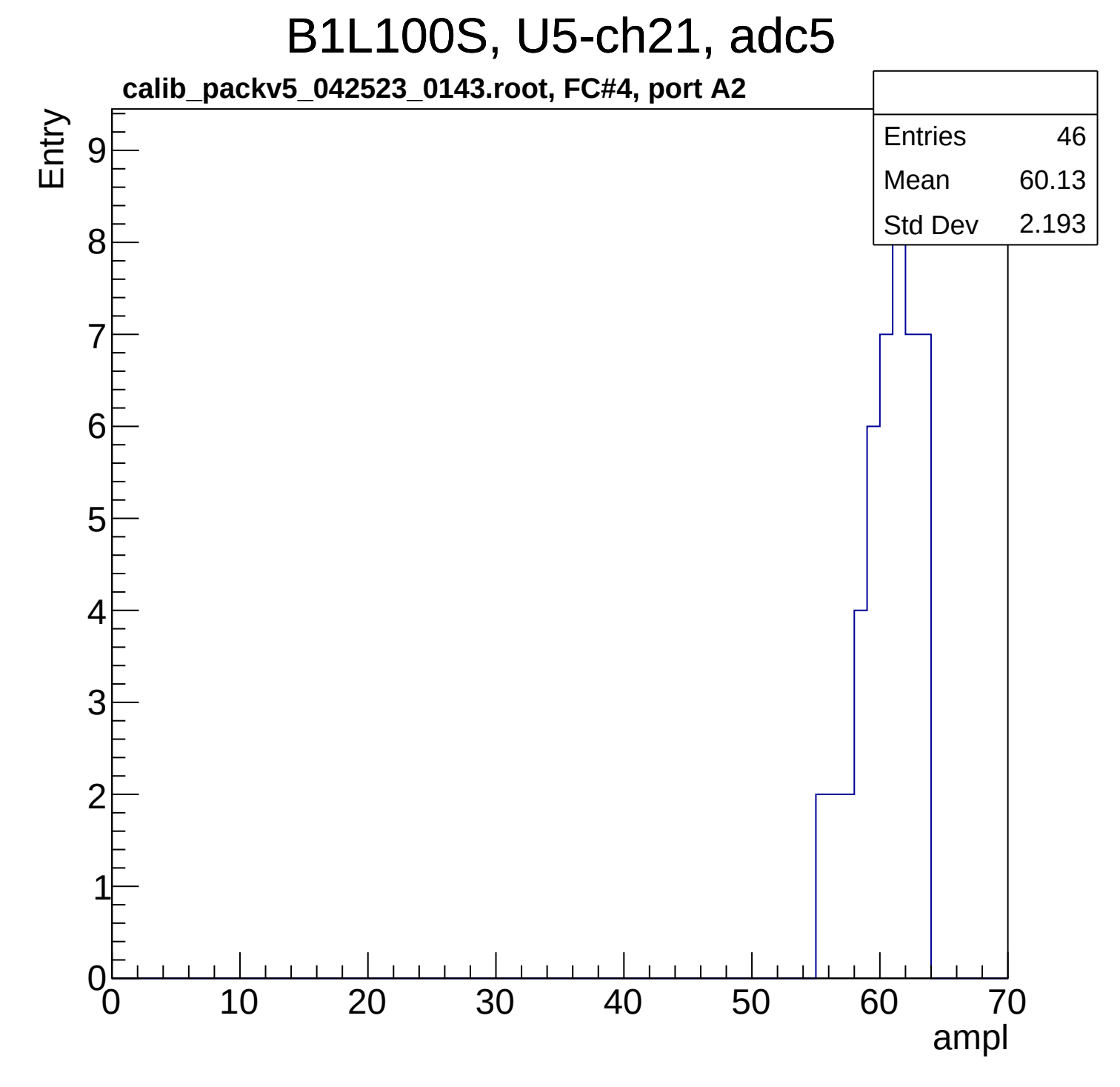
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch21, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 46
Mean 60.13
Std Dev 2.193
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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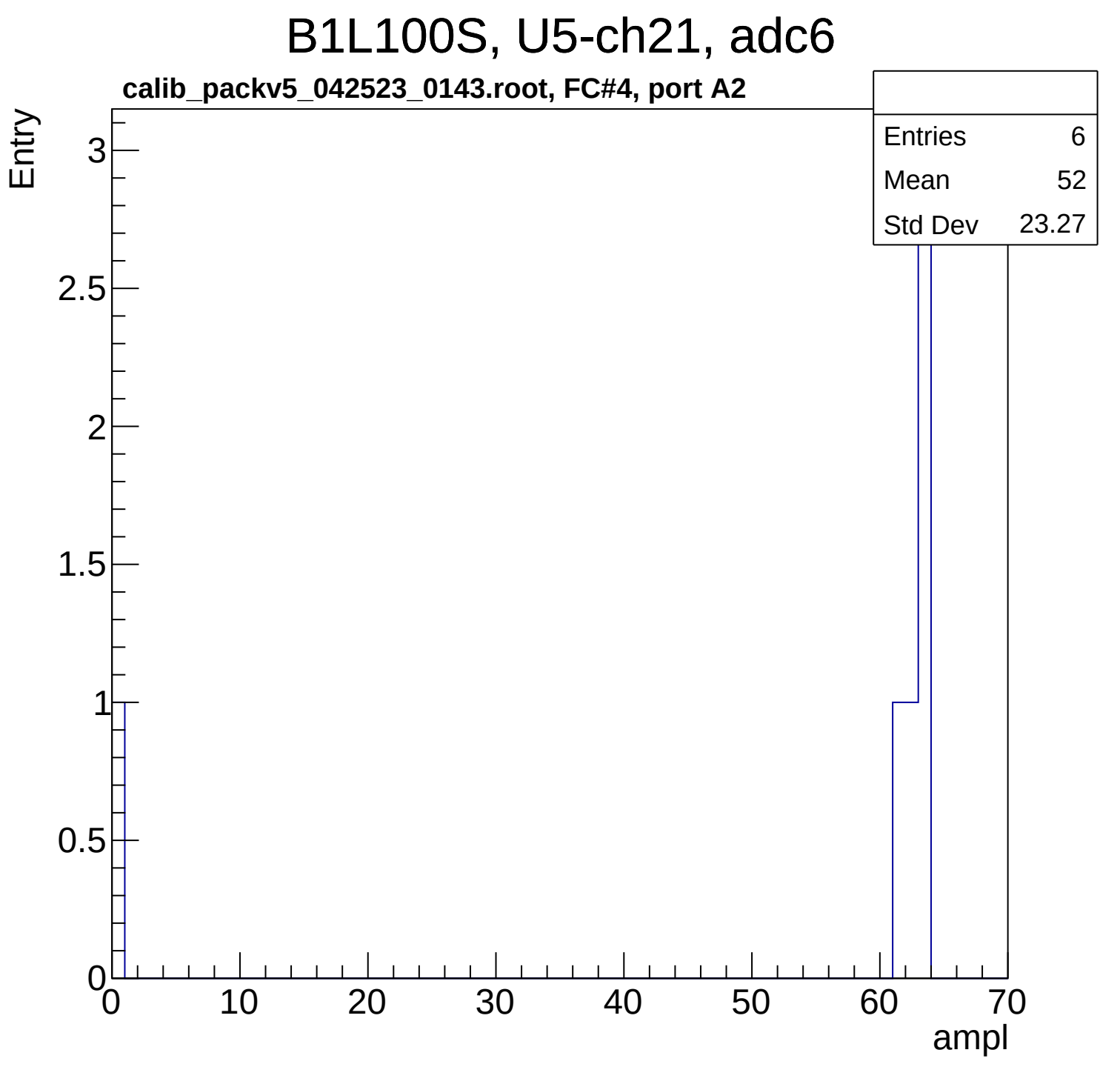
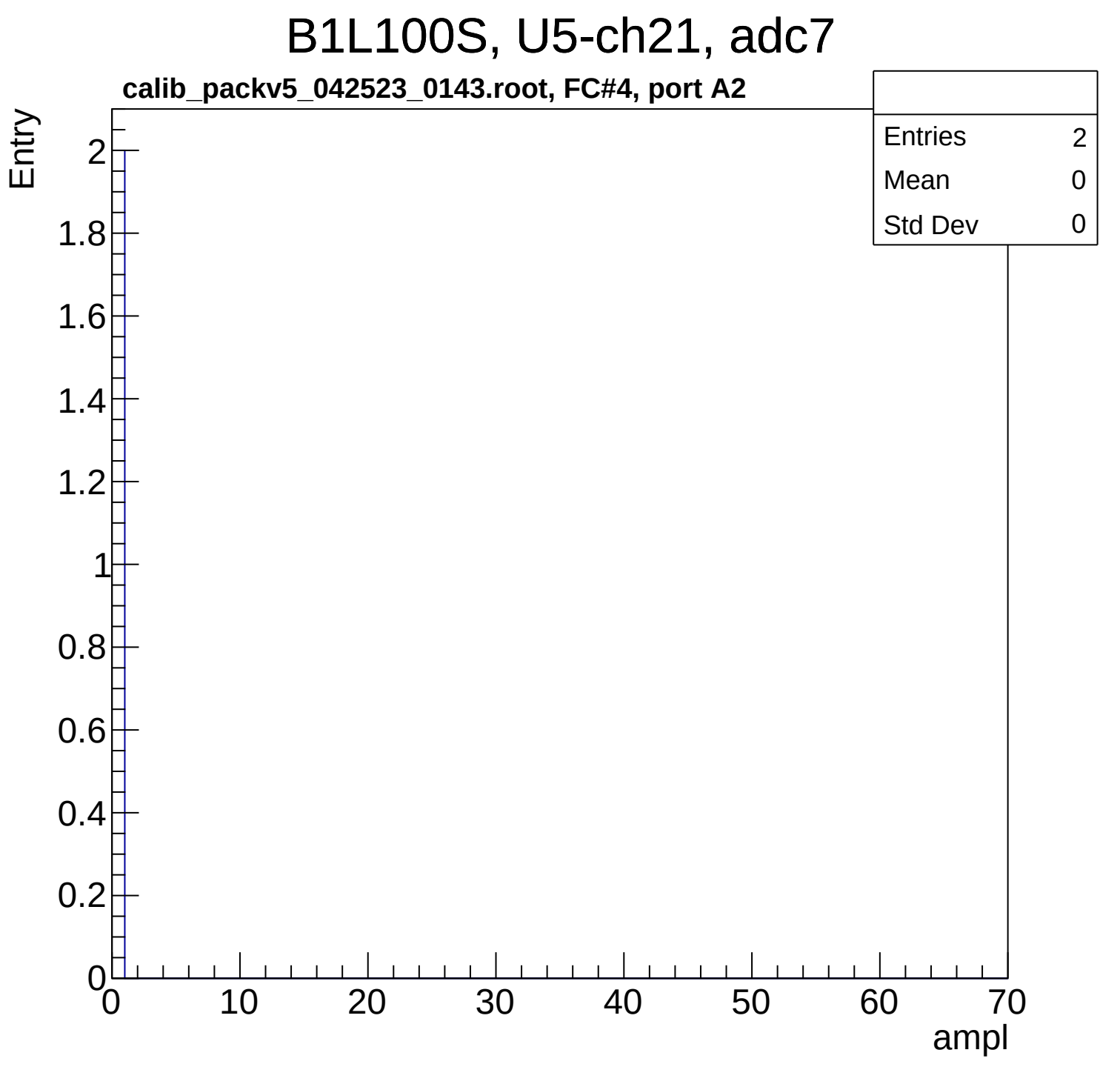
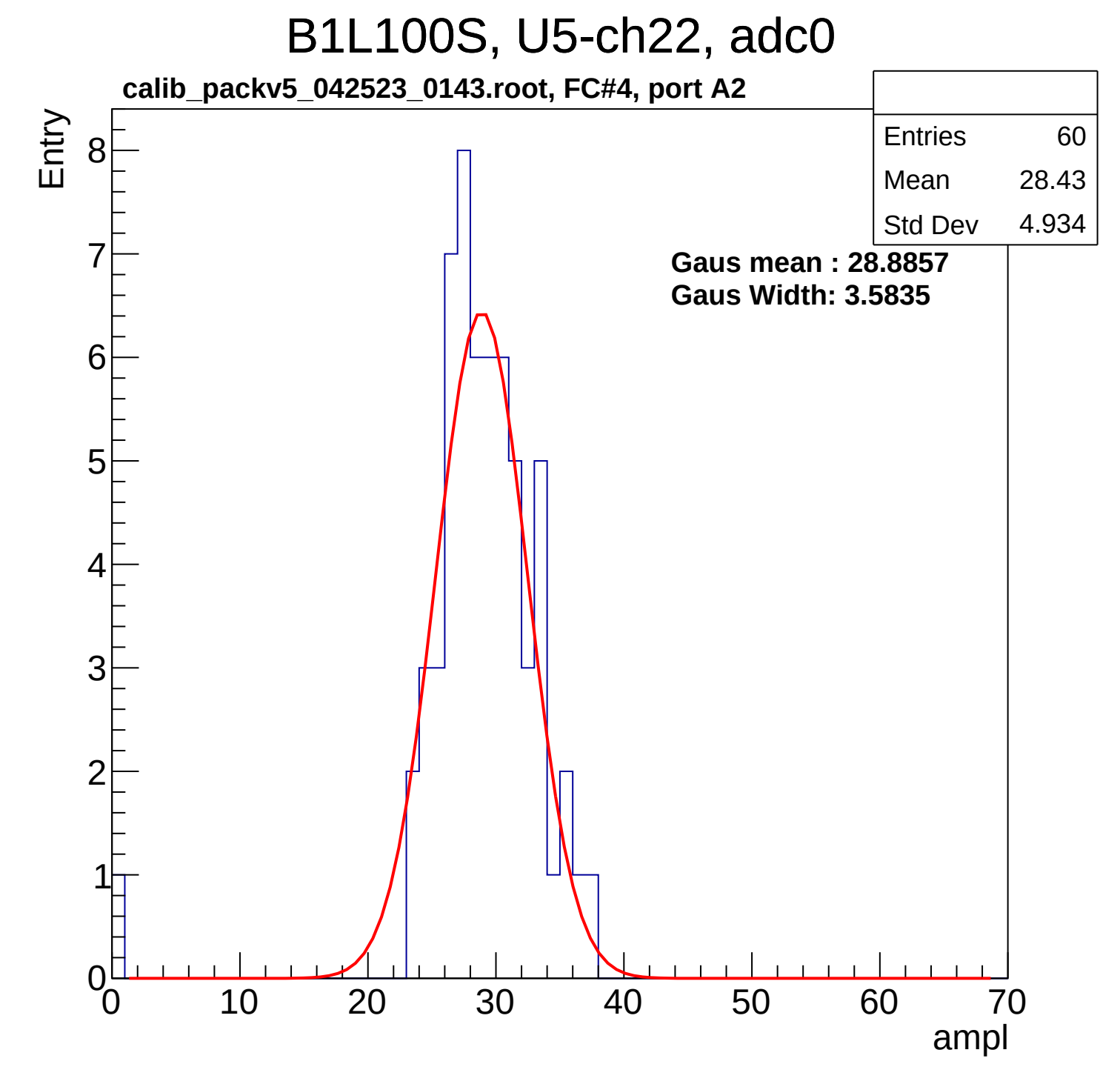
40
50
60
70


B1L100S, U5-ch21, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 6
Mean 52
Std Dev 23.27
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L100S, U5-ch21, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch22, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 28.43
Std Dev 4.934
Gaus mean : 28.8857
Gaus Width: 3.5835
Entry
ampl
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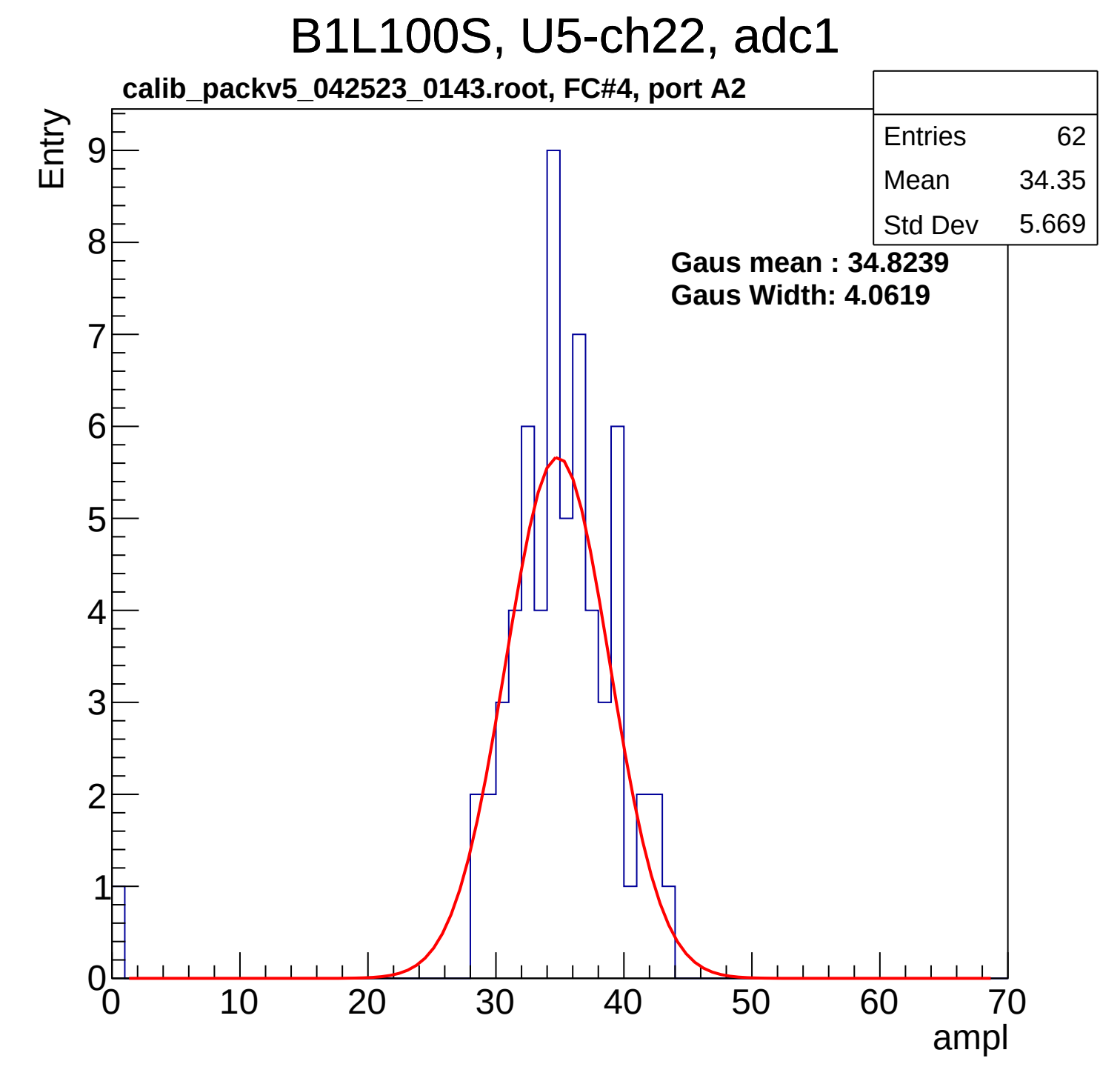
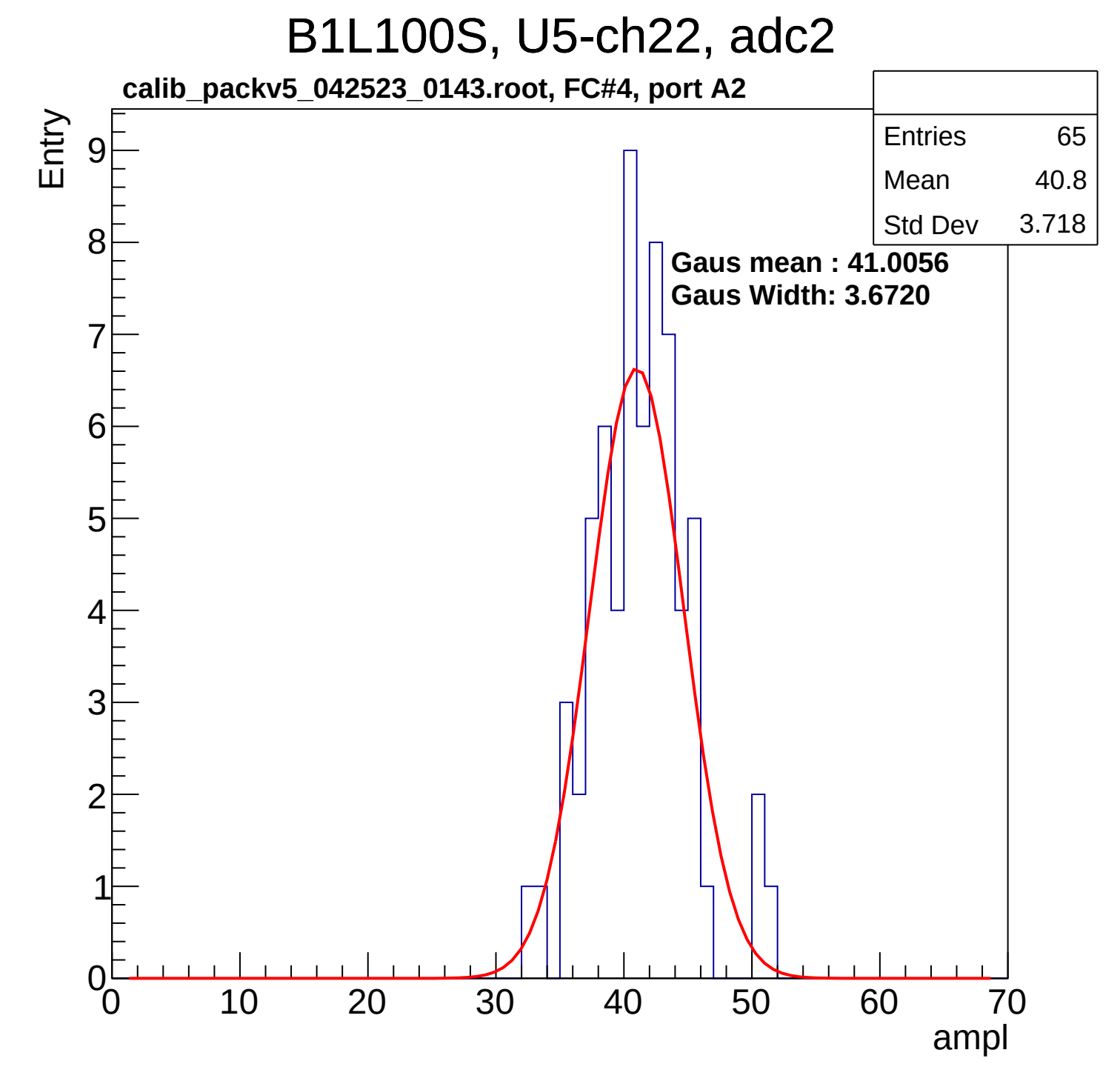
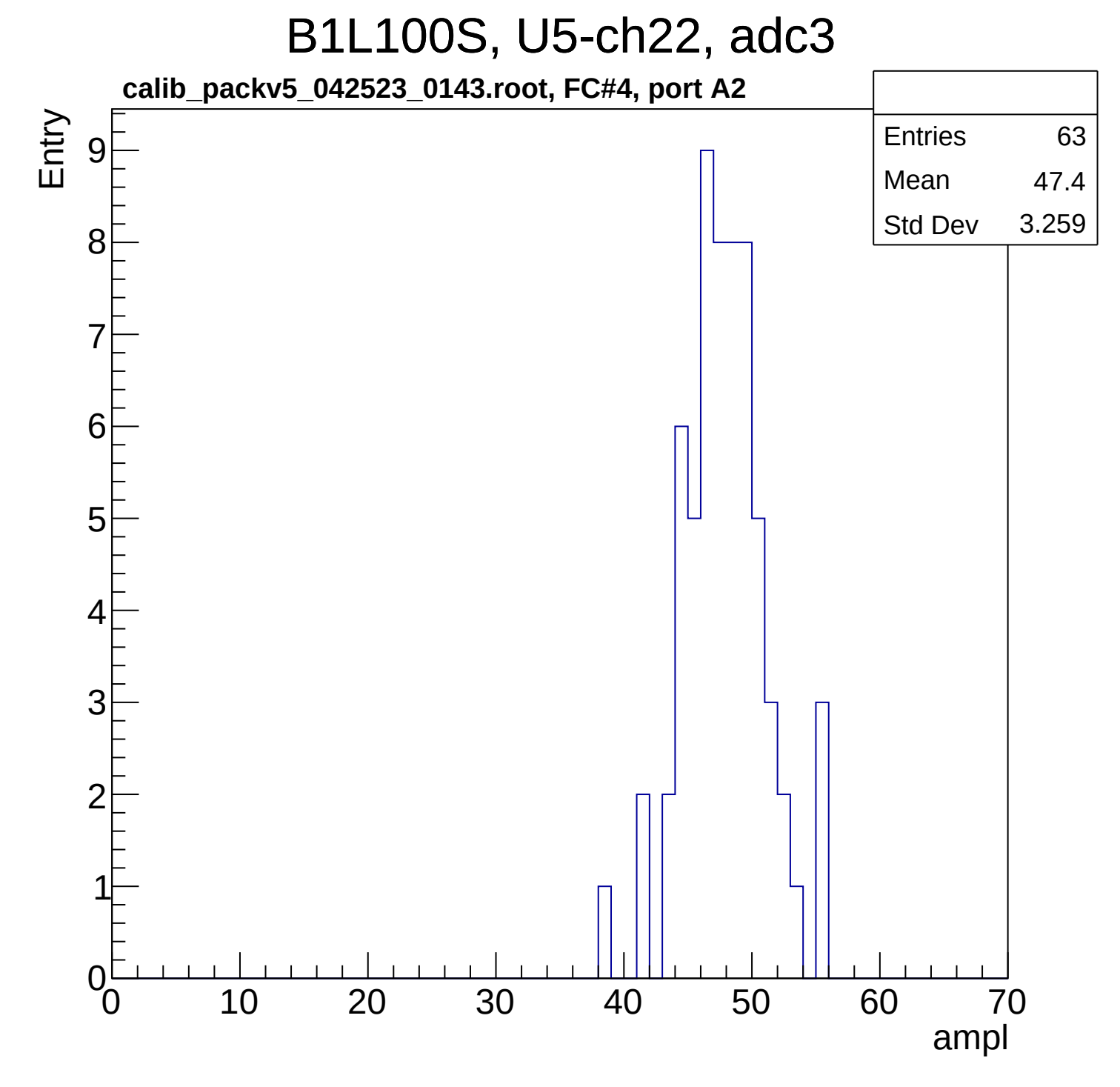
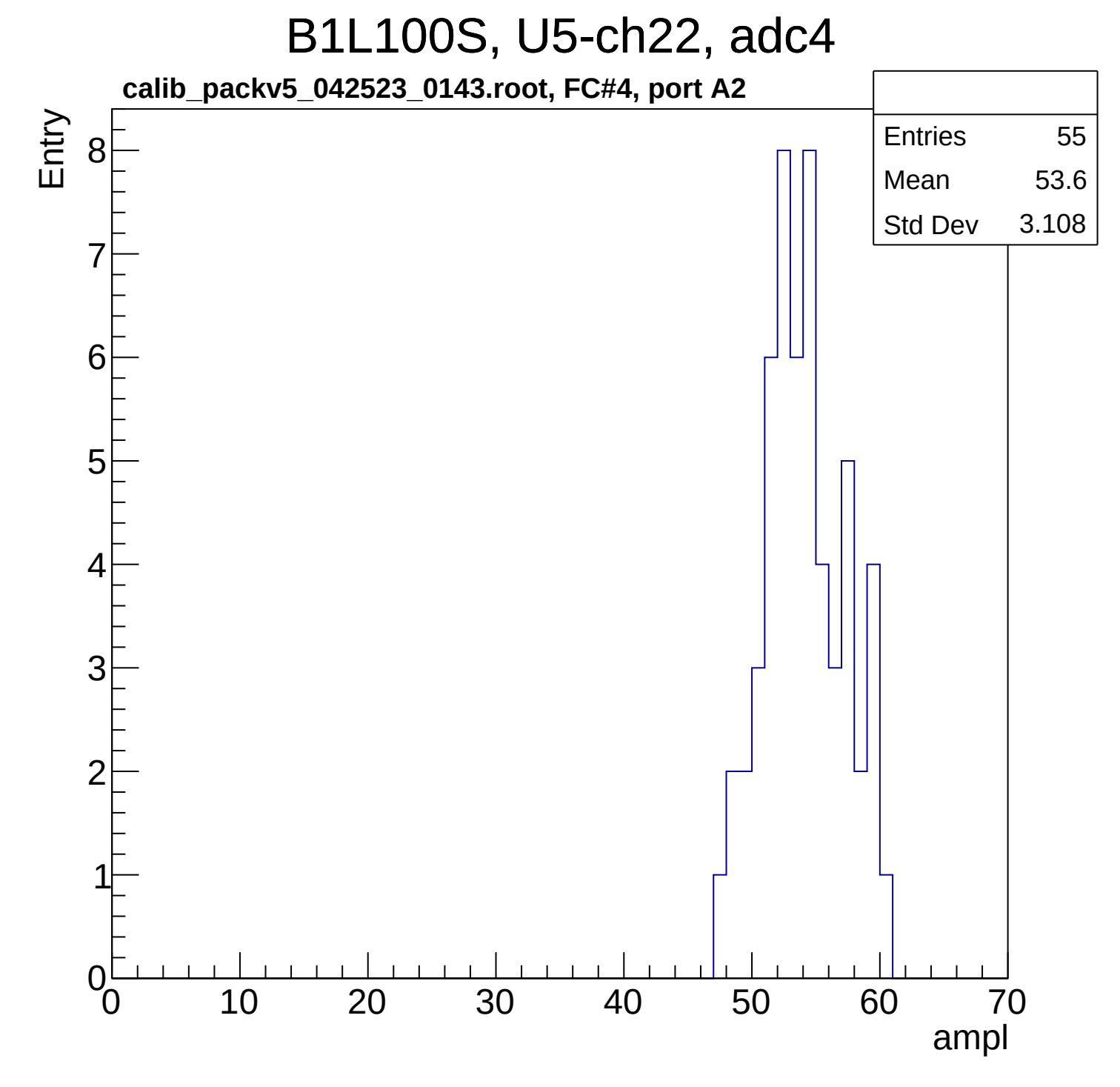
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch22, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 34.35
Std Dev 5.669
Gaus mean : 34.8239
Gaus Width: 4.0619
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch22, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 40.8
Std Dev 3.718
Gaus mean : 41.0056
Gaus Width: 3.6720
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch22, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 47.4
Std Dev 3.259
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch22, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 53.6
Std Dev 3.108
Entry
ampl
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1
2
3
4
5
6
7
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0
10
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40
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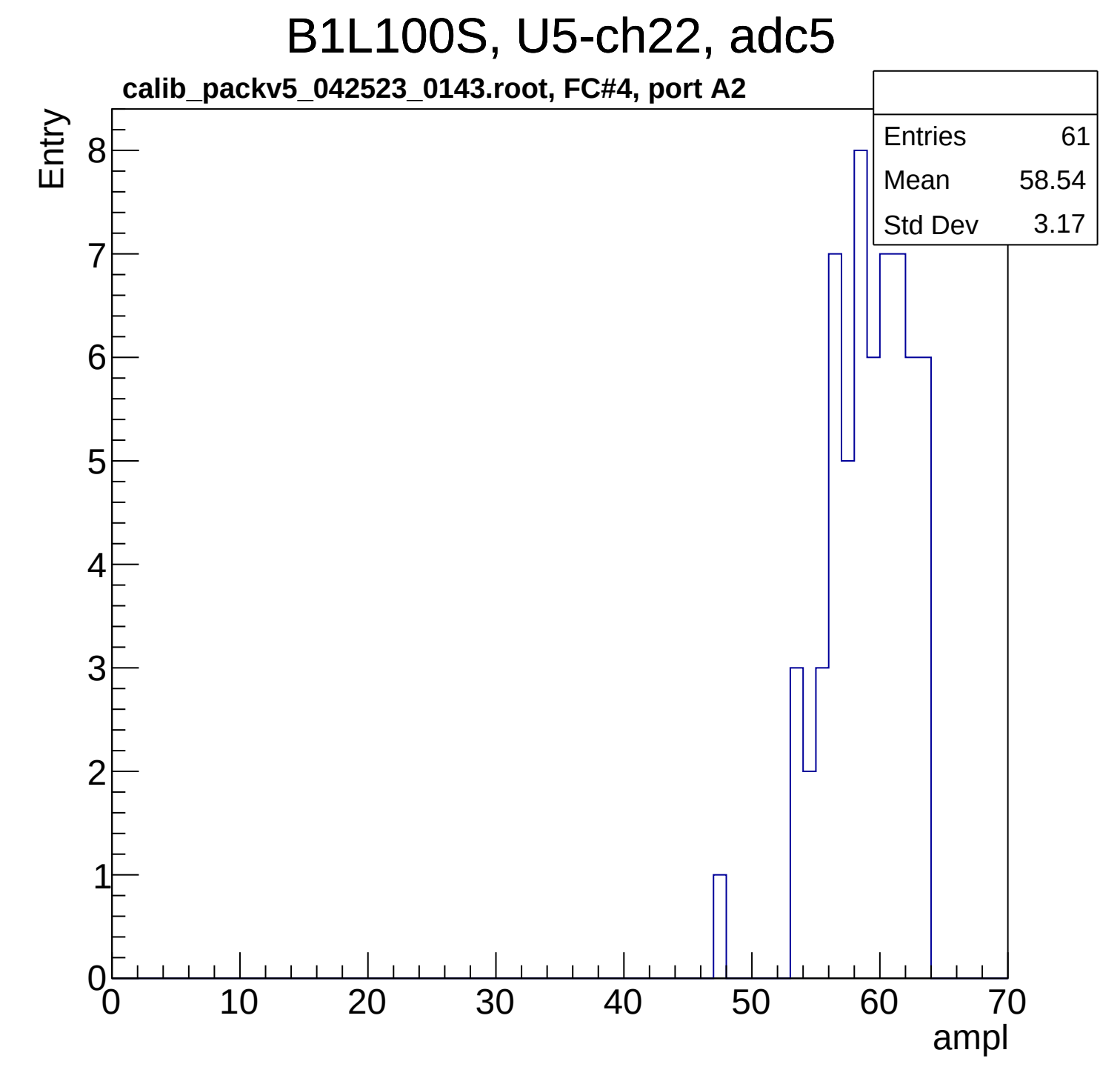
B1L100S, U5-ch22, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 58.54
Std Dev 3.17
Entry
ampl
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1
2
3
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5
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7
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0
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40
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60
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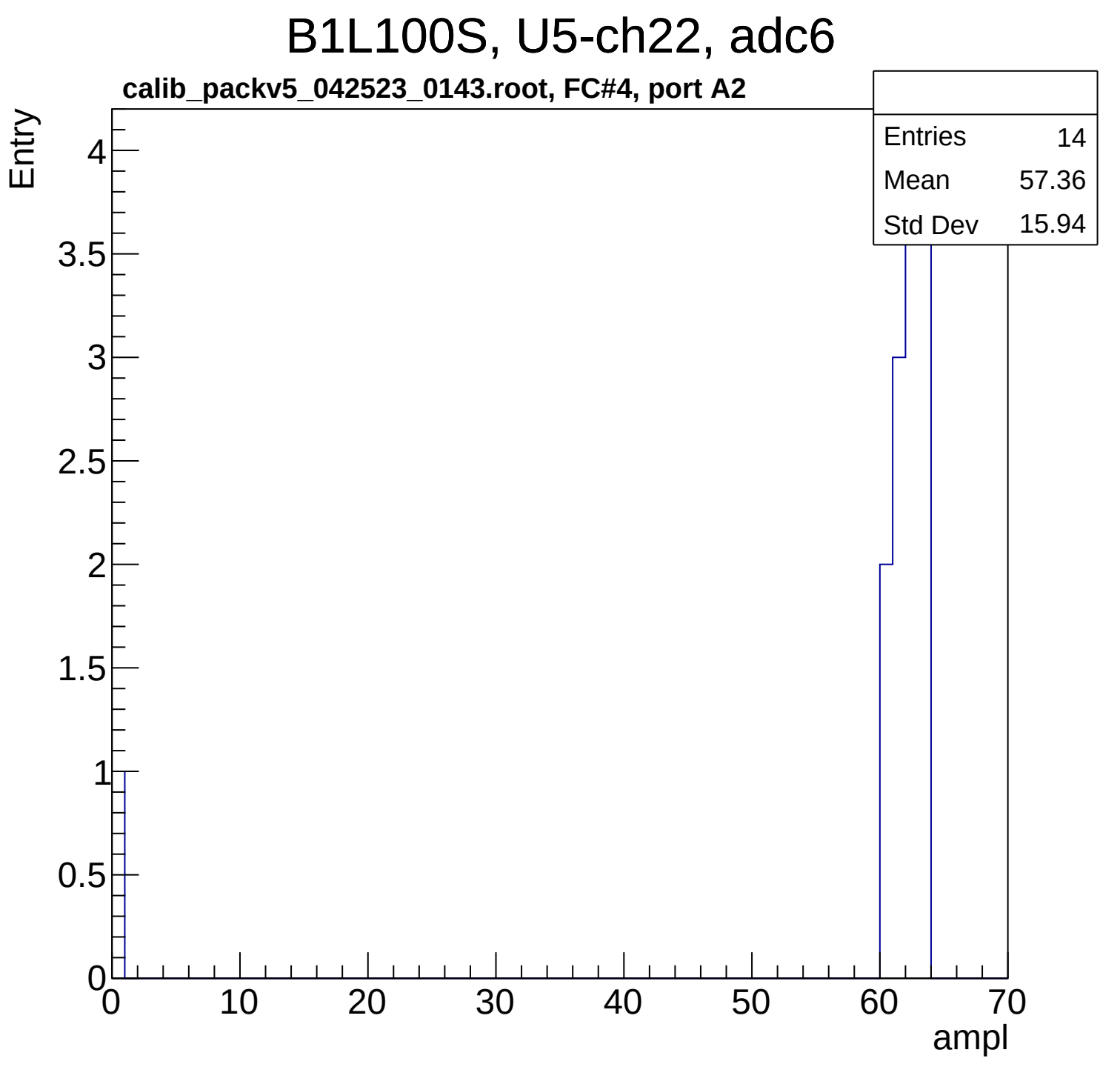
B1L100S, U5-ch22, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 14
Mean 57.36
Std Dev 15.94
Entry
ampl
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0.5
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1.5
2
2.5
3
3.5
4
0
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20
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40
50
60
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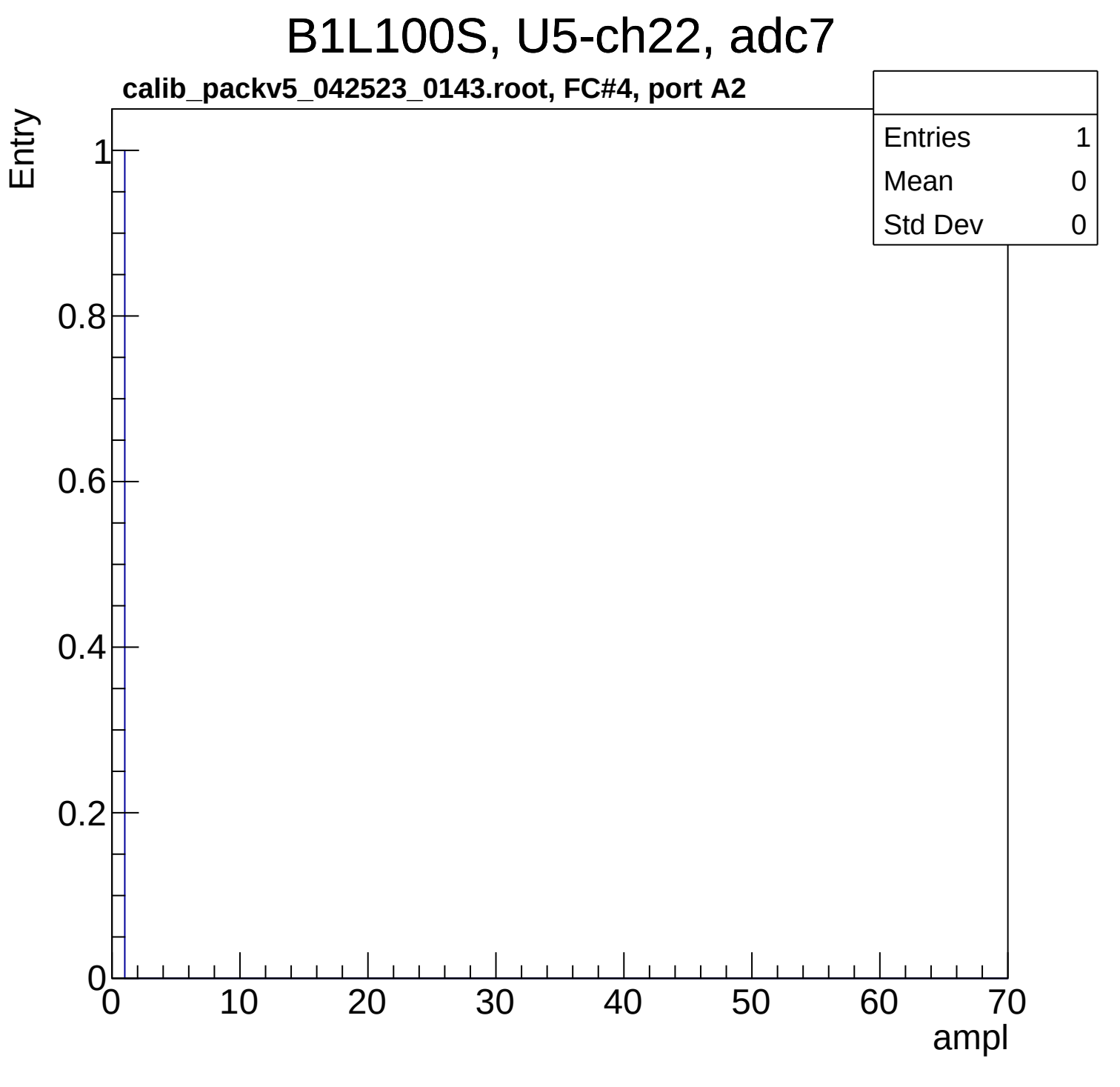
B1L100S, U5-ch22, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
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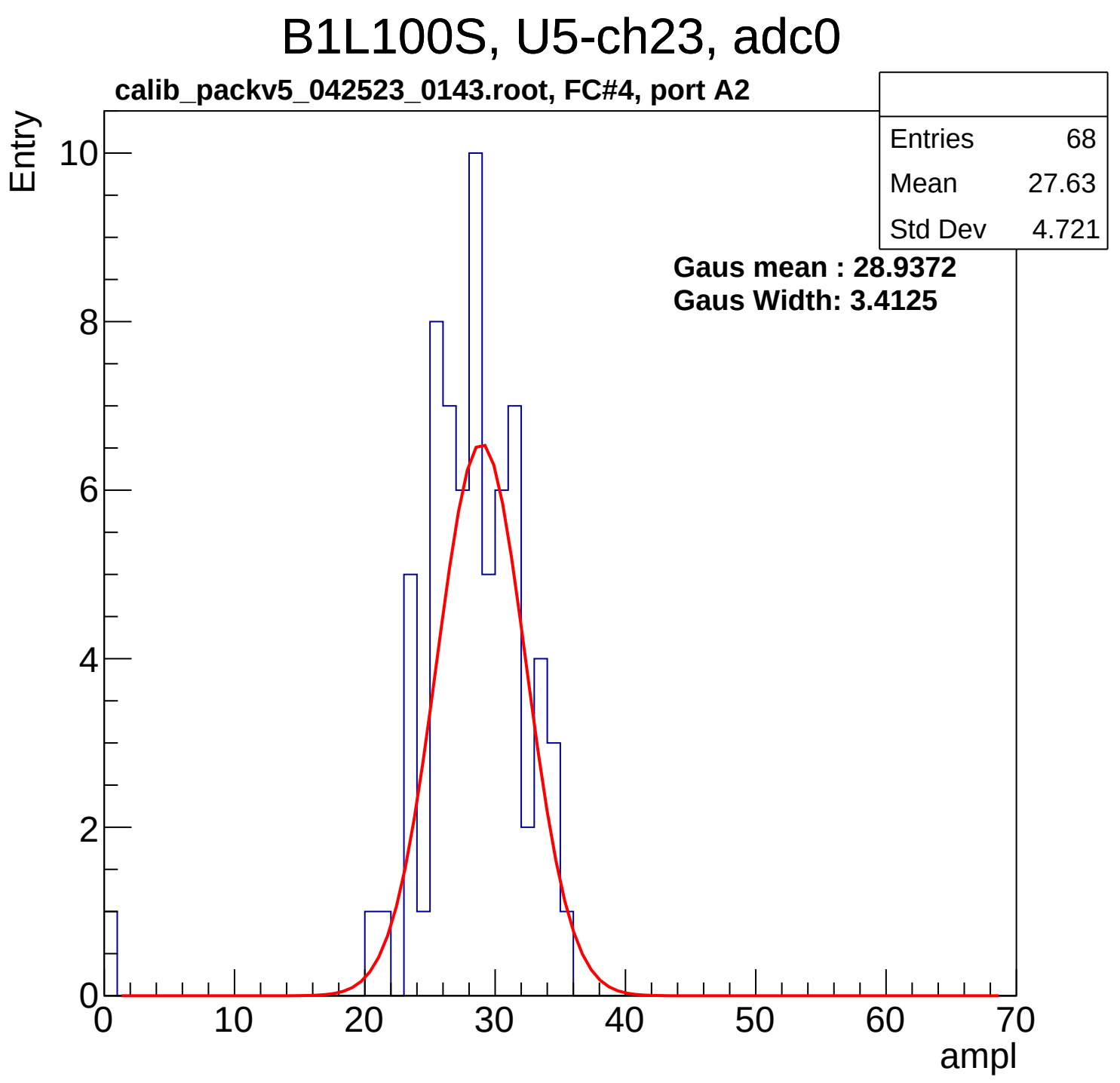
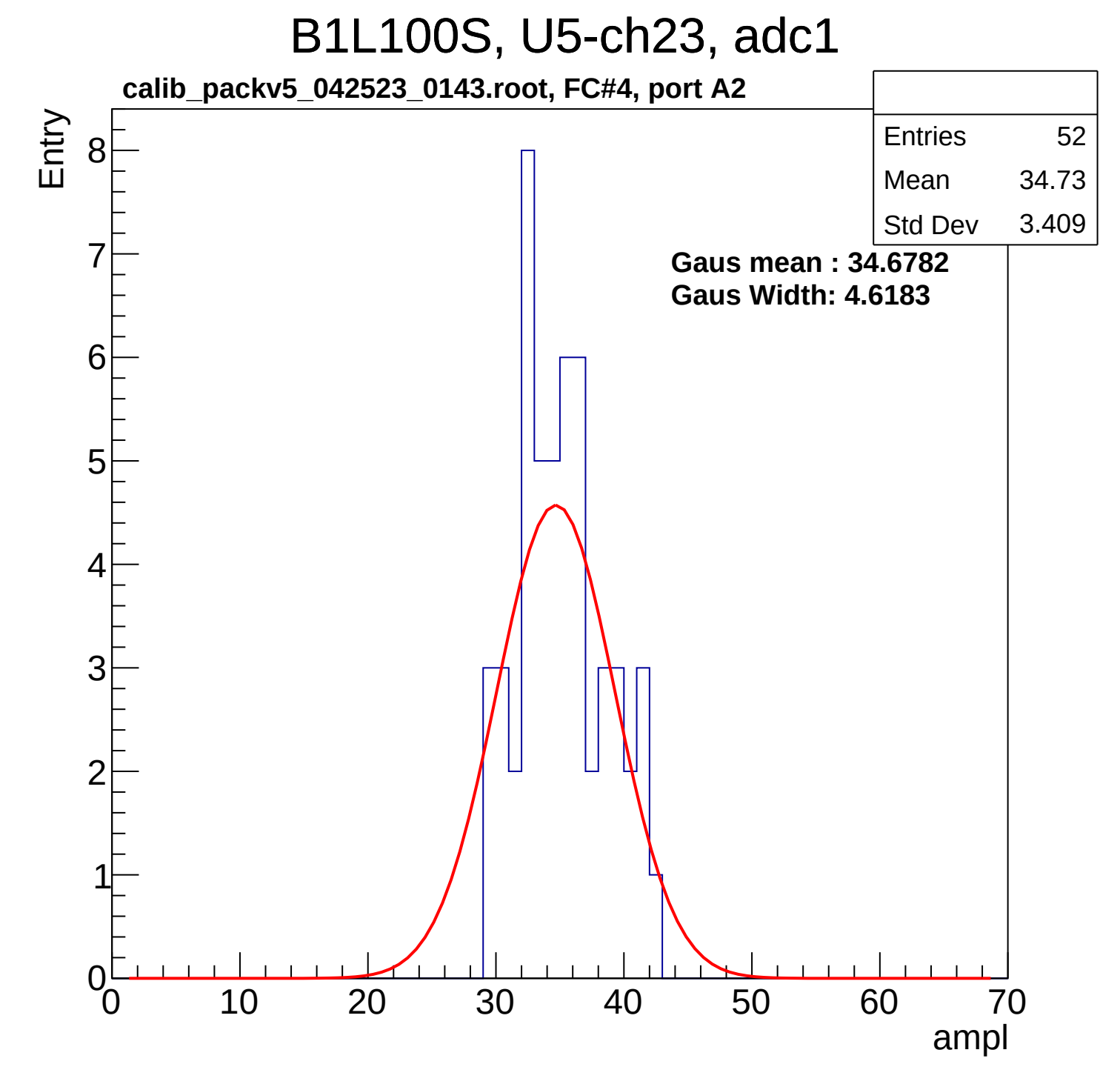
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch23, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 27.63
Std Dev 4.721
Gaus mean : 28.9372
Gaus Width: 3.4125
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch23, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 52
Mean 34.73
Std Dev 3.409
Gaus mean : 34.6782
Gaus Width: 4.6183
Entry
ampl
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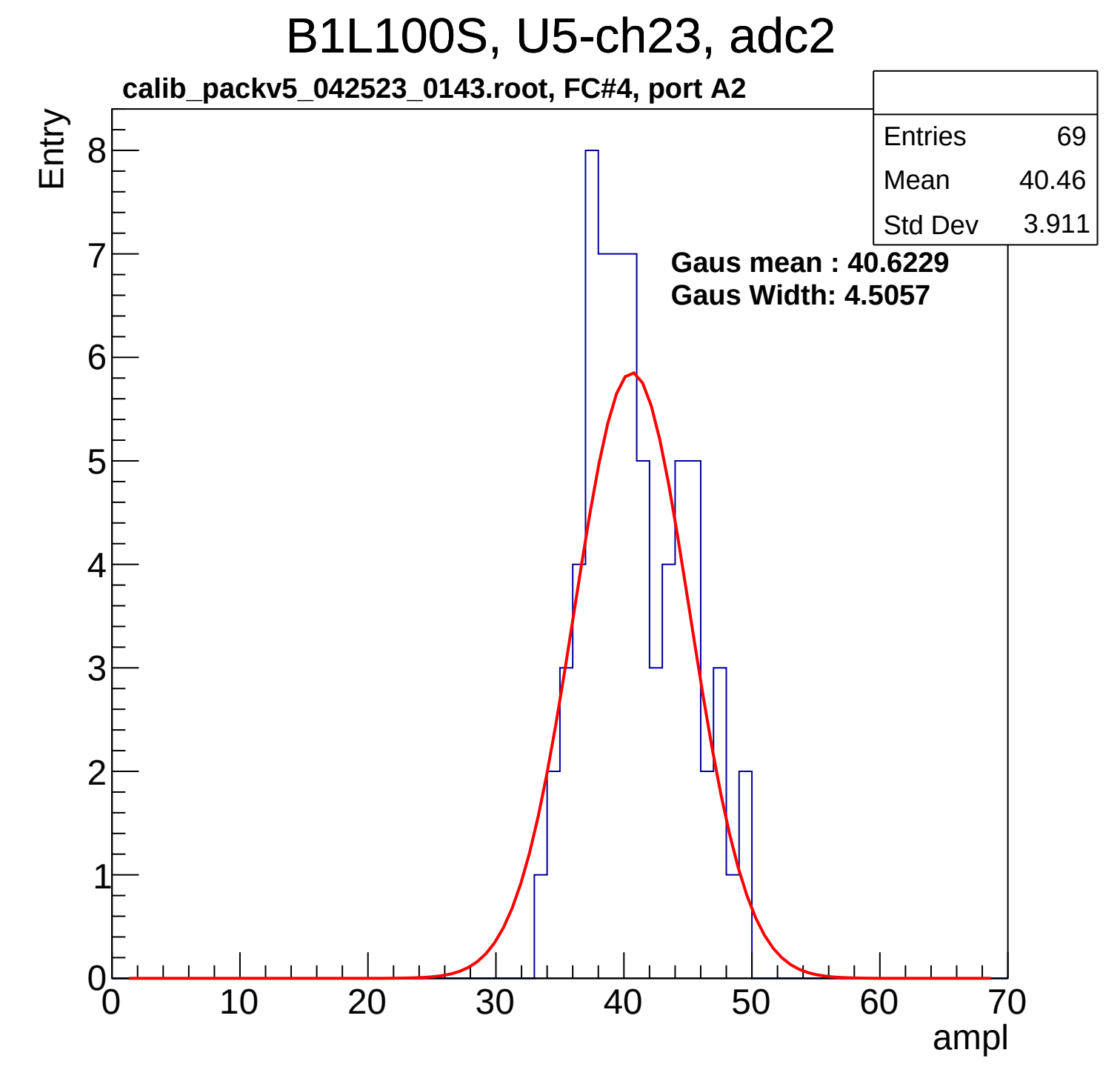
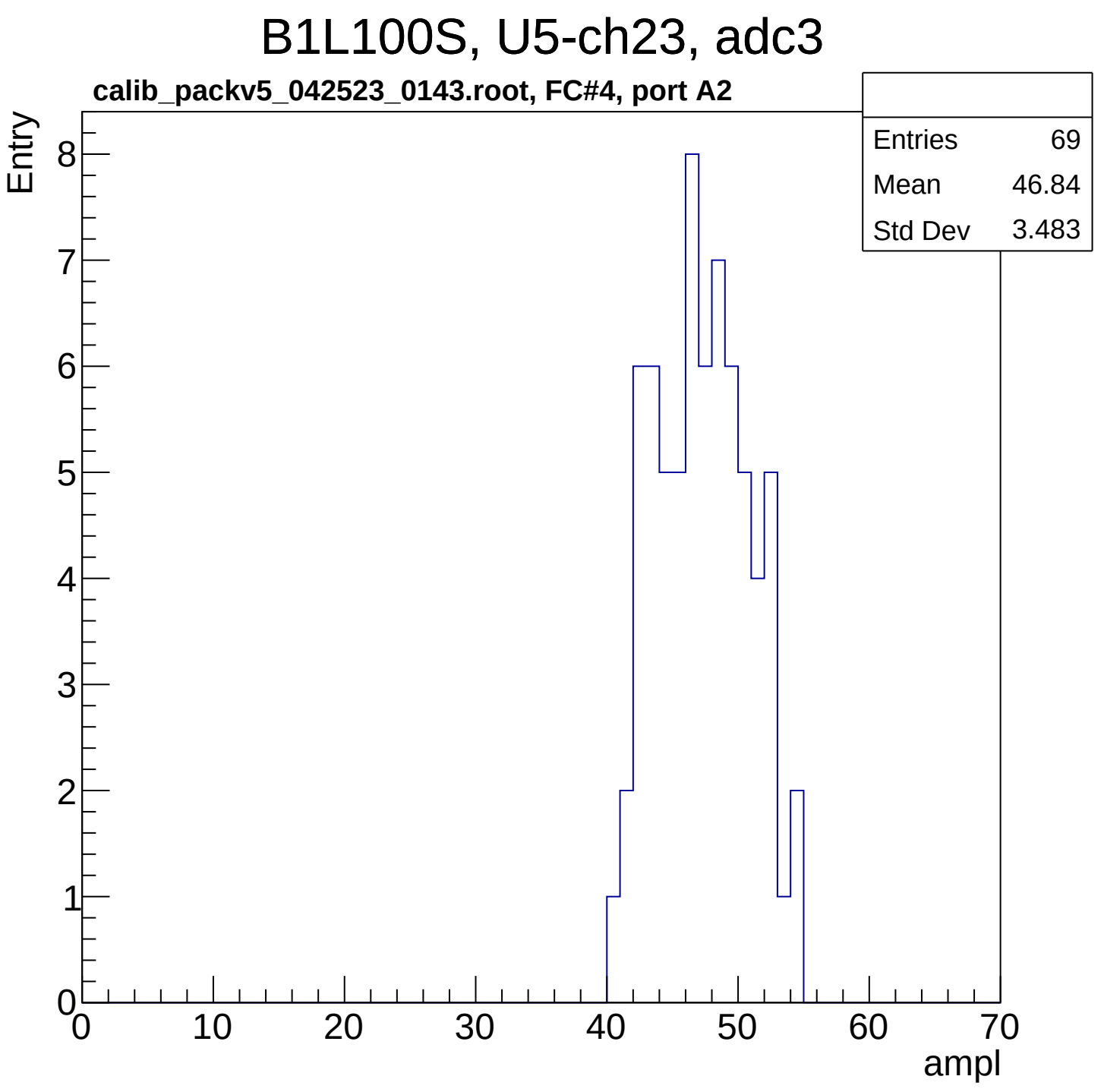
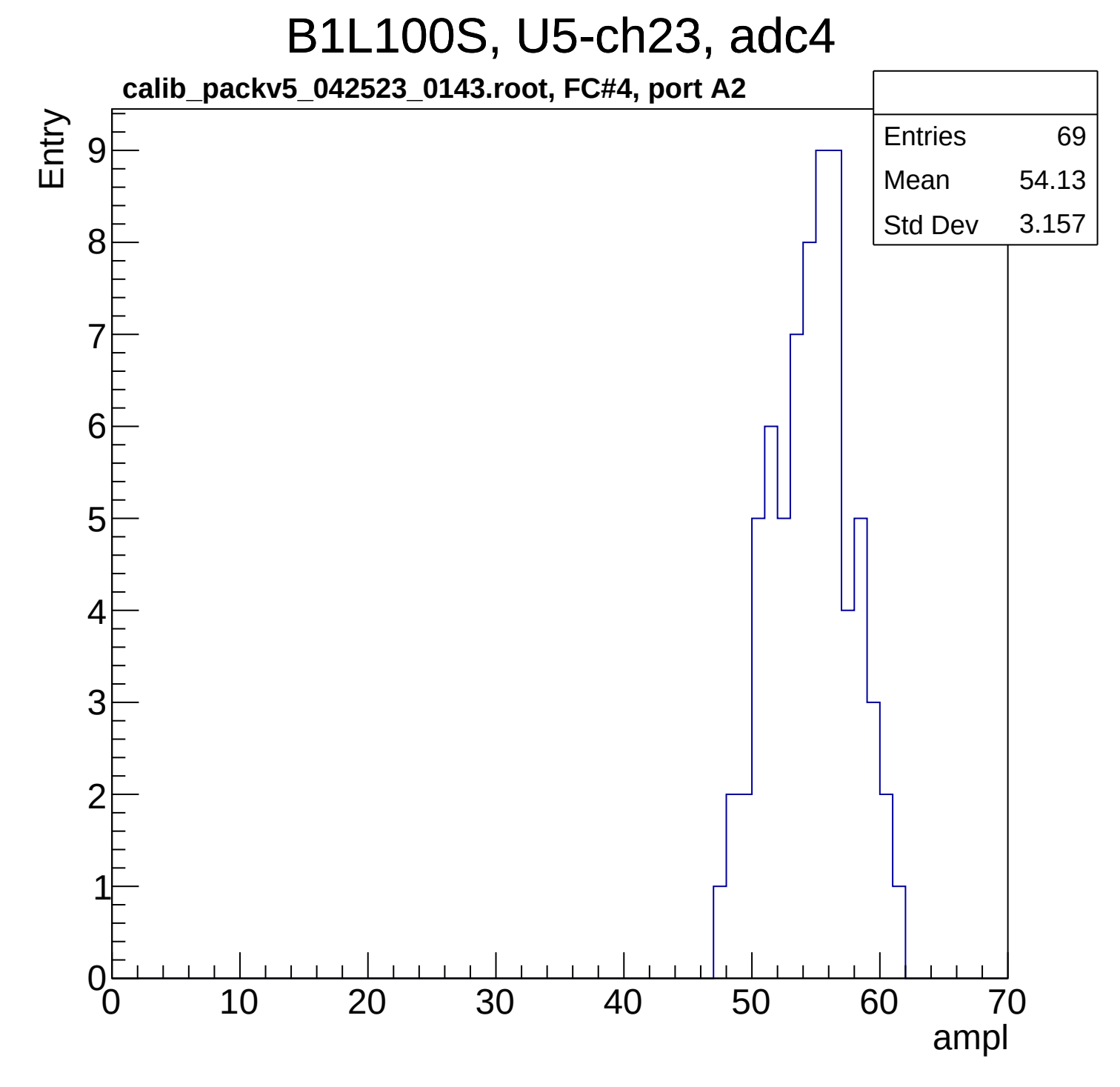
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch23, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 40.46
Std Dev 3.911
Gaus mean : 40.6229
Gaus Width: 4.5057
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch23, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 46.84
Std Dev 3.483
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch23, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 54.13
Std Dev 3.157
Entry
ampl
0
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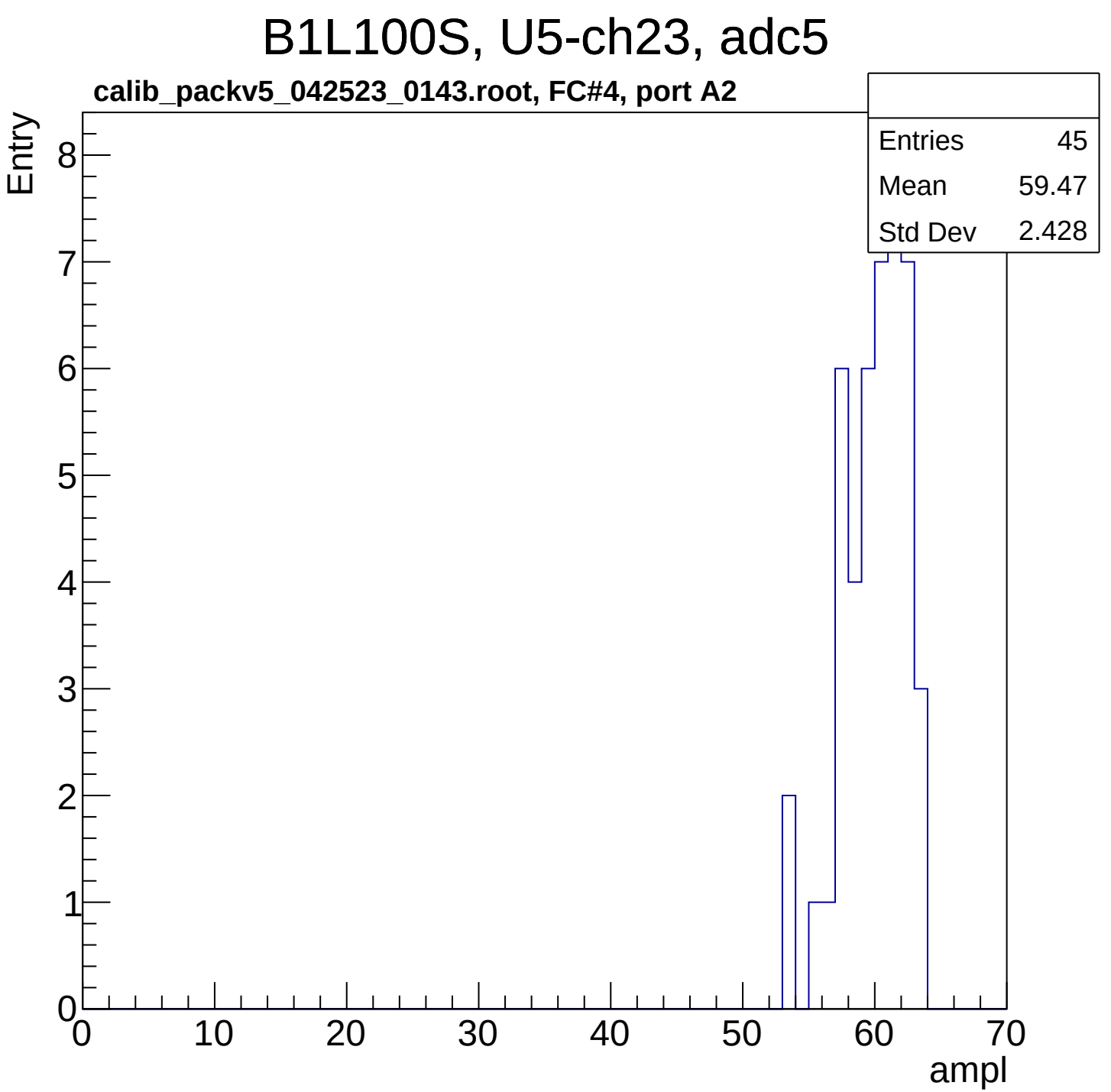
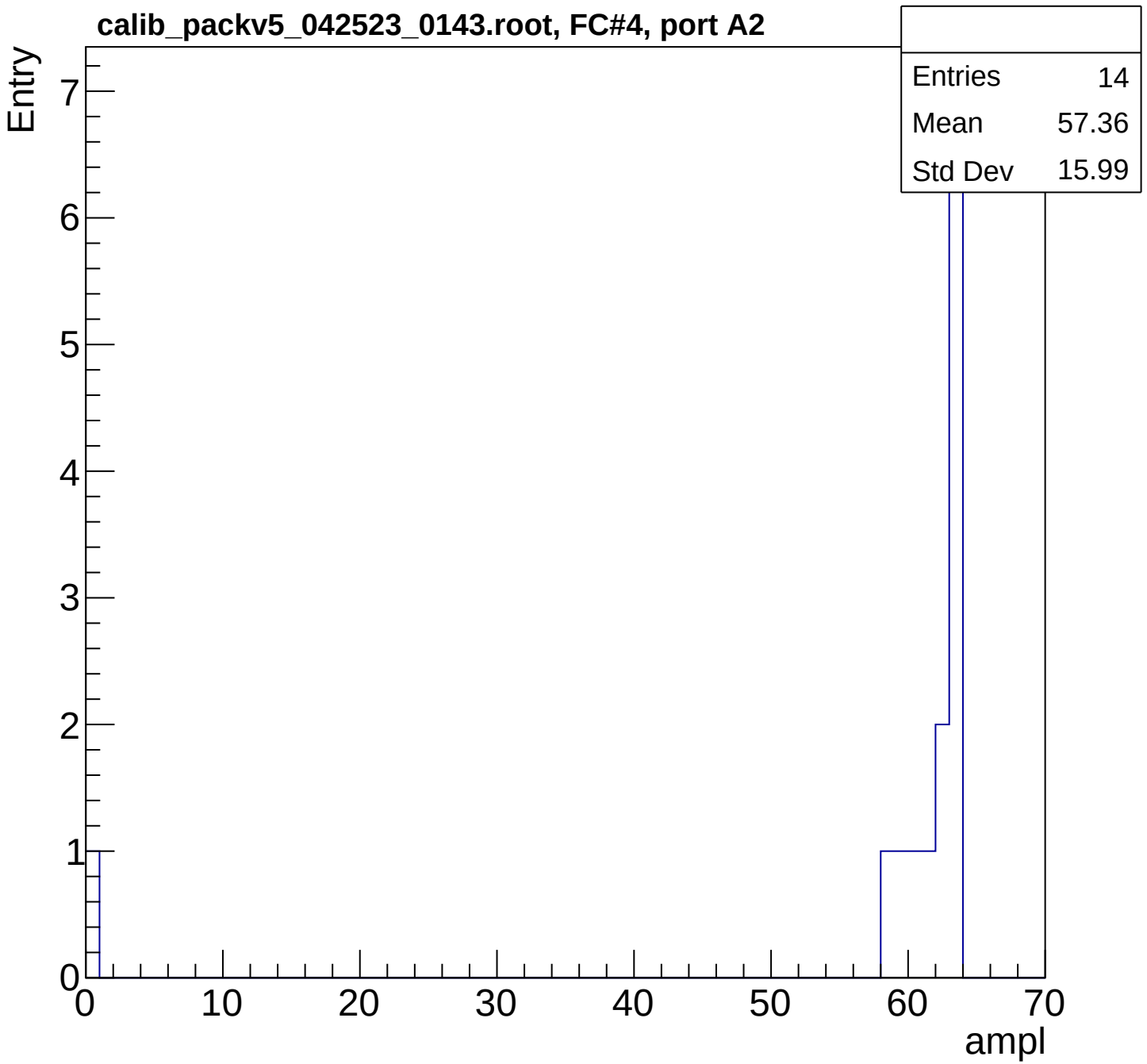
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch23, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 45
Mean 59.47
Std Dev 2.428
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch23, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 14
Mean 57.36
Std Dev 15.99
Entry
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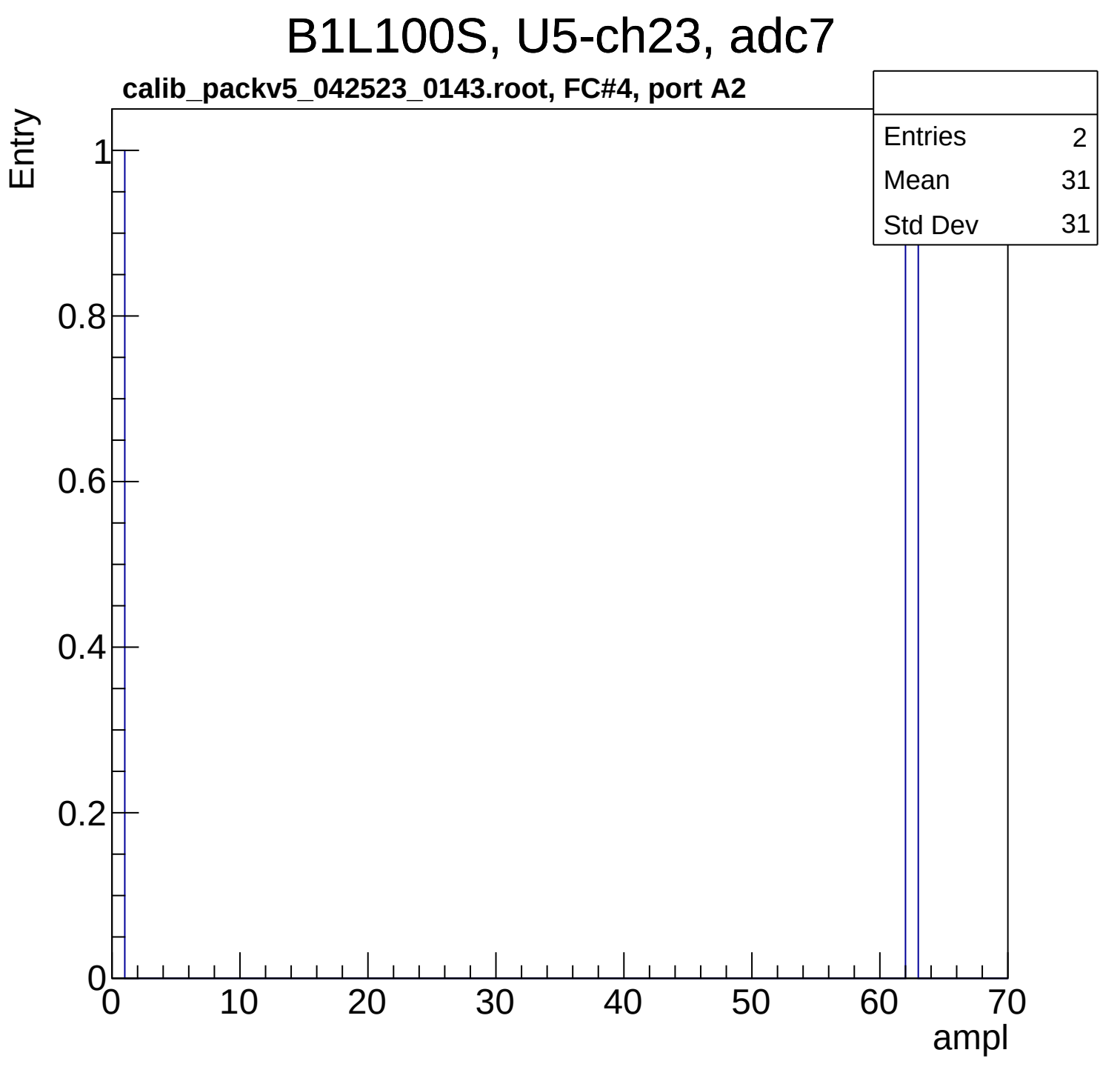
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch23, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 31
Std Dev 31
Entry
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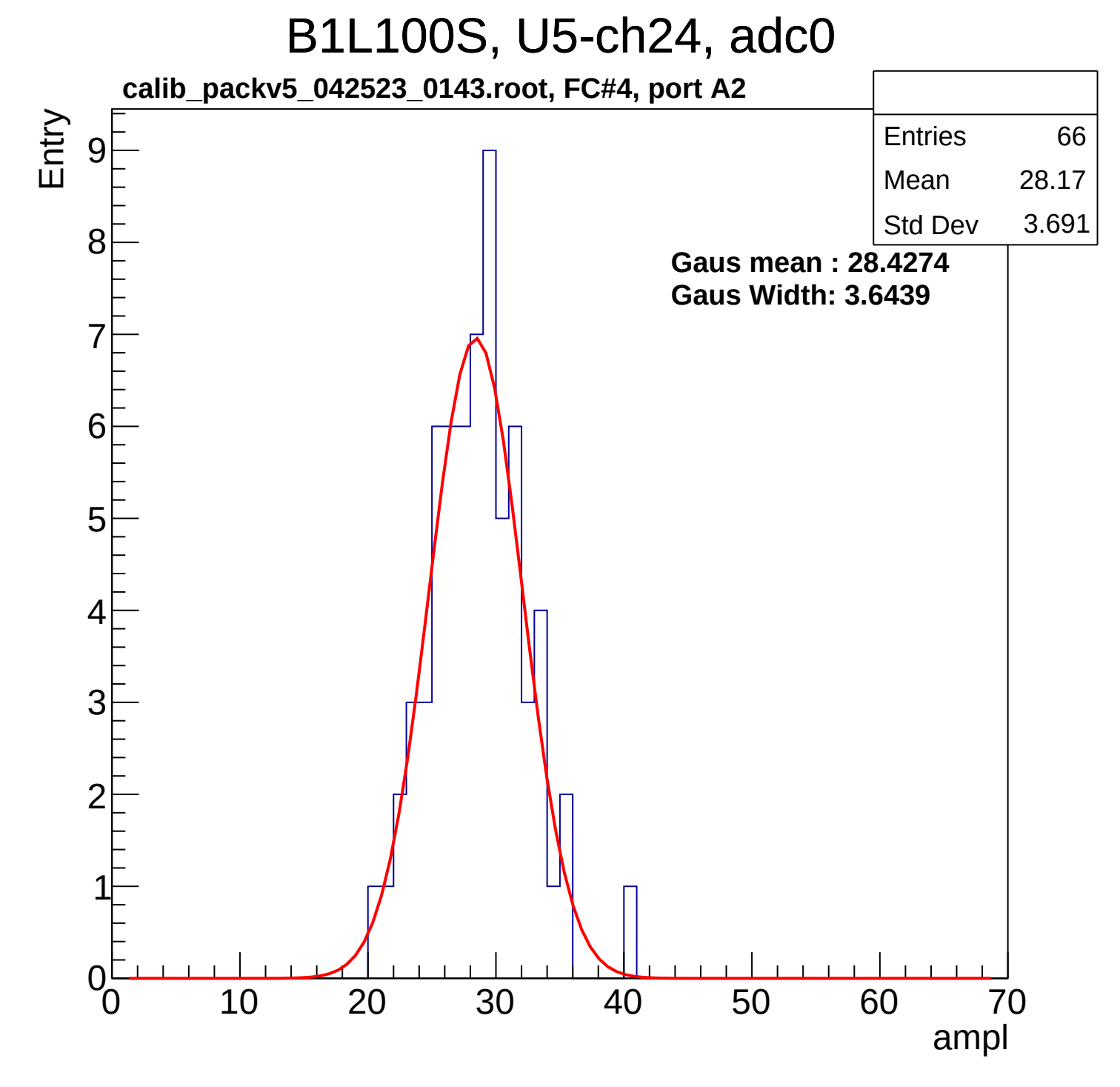
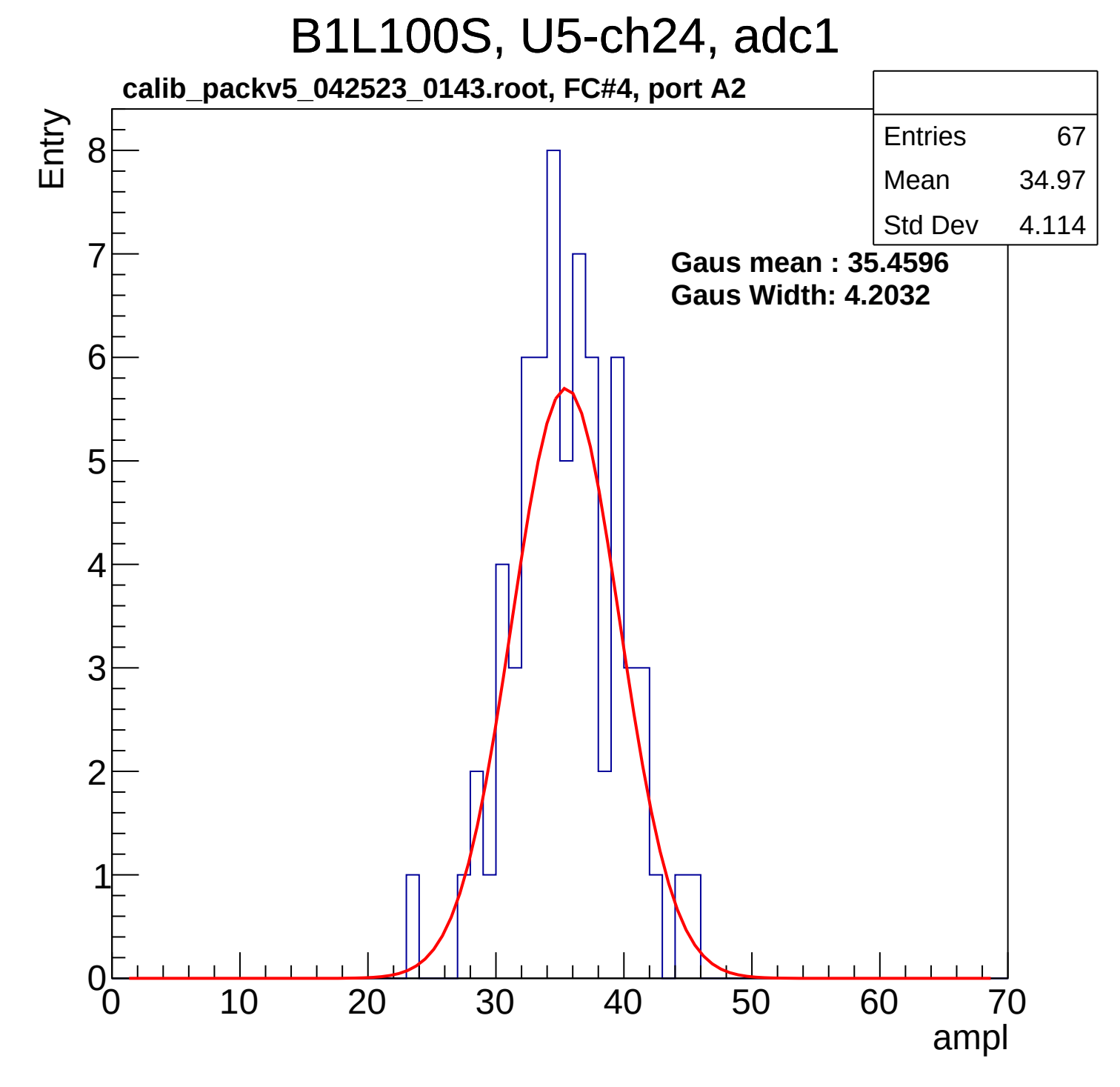
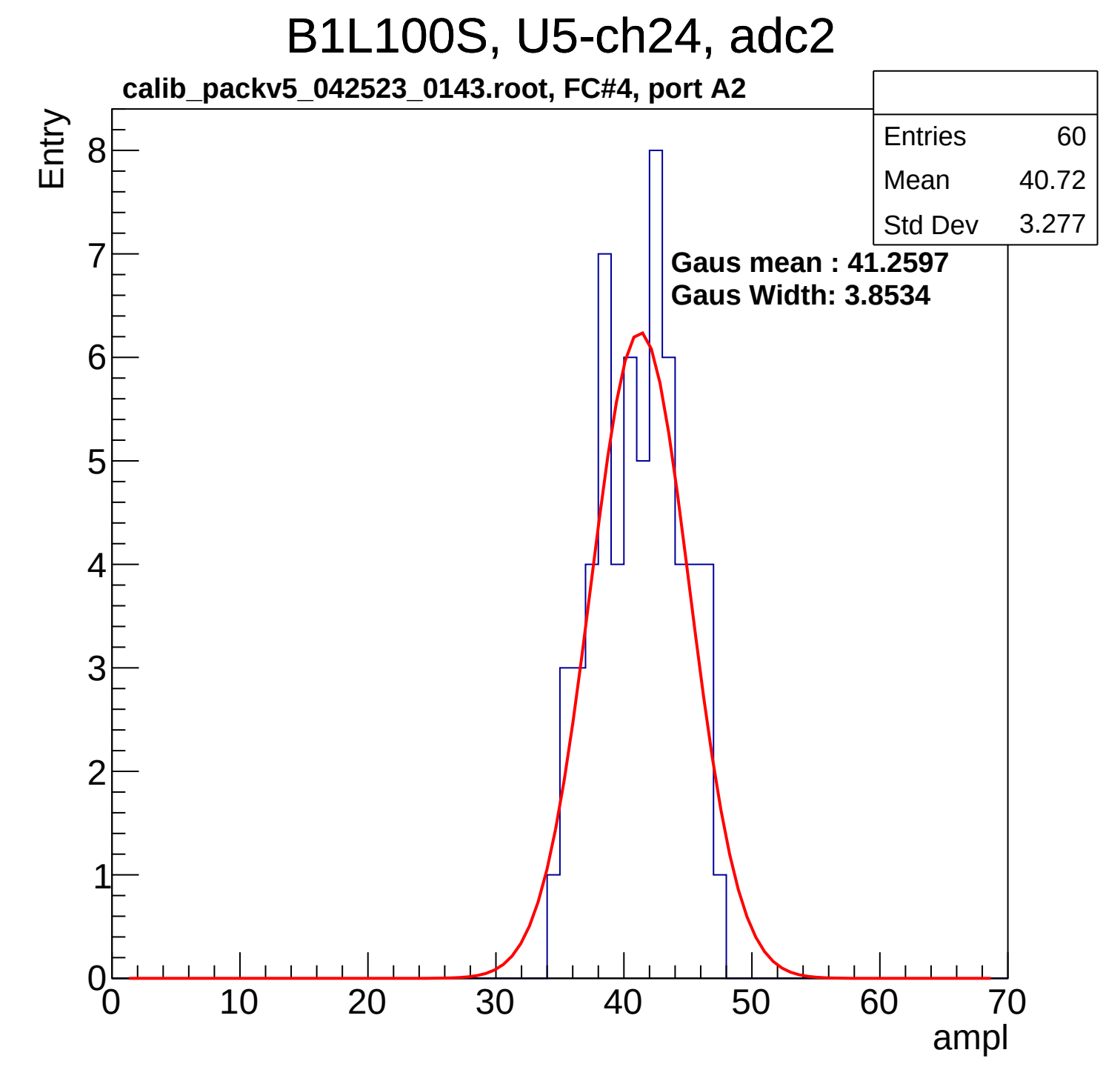
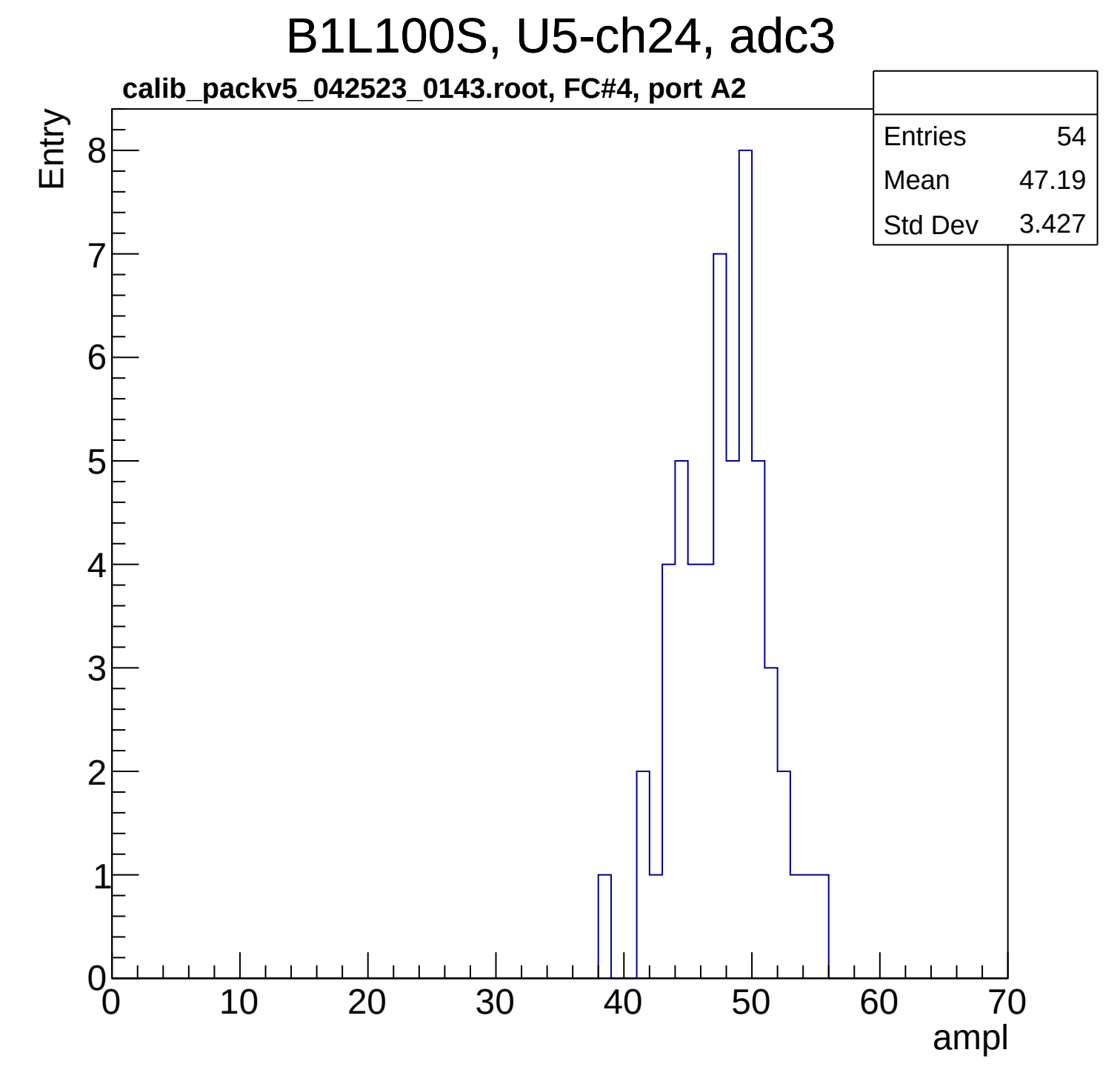
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch24, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 28.17
Std Dev 3.691
Gaus mean : 28.4274
Gaus Width: 3.6439
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch24, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 34.97
Std Dev 4.114
Gaus mean : 35.4596
Gaus Width: 4.2032
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch24, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 40.72
Std Dev 3.277
Gaus mean : 41.2597
Gaus Width: 3.8534
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch24, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 47.19
Std Dev 3.427
Entry
ampl
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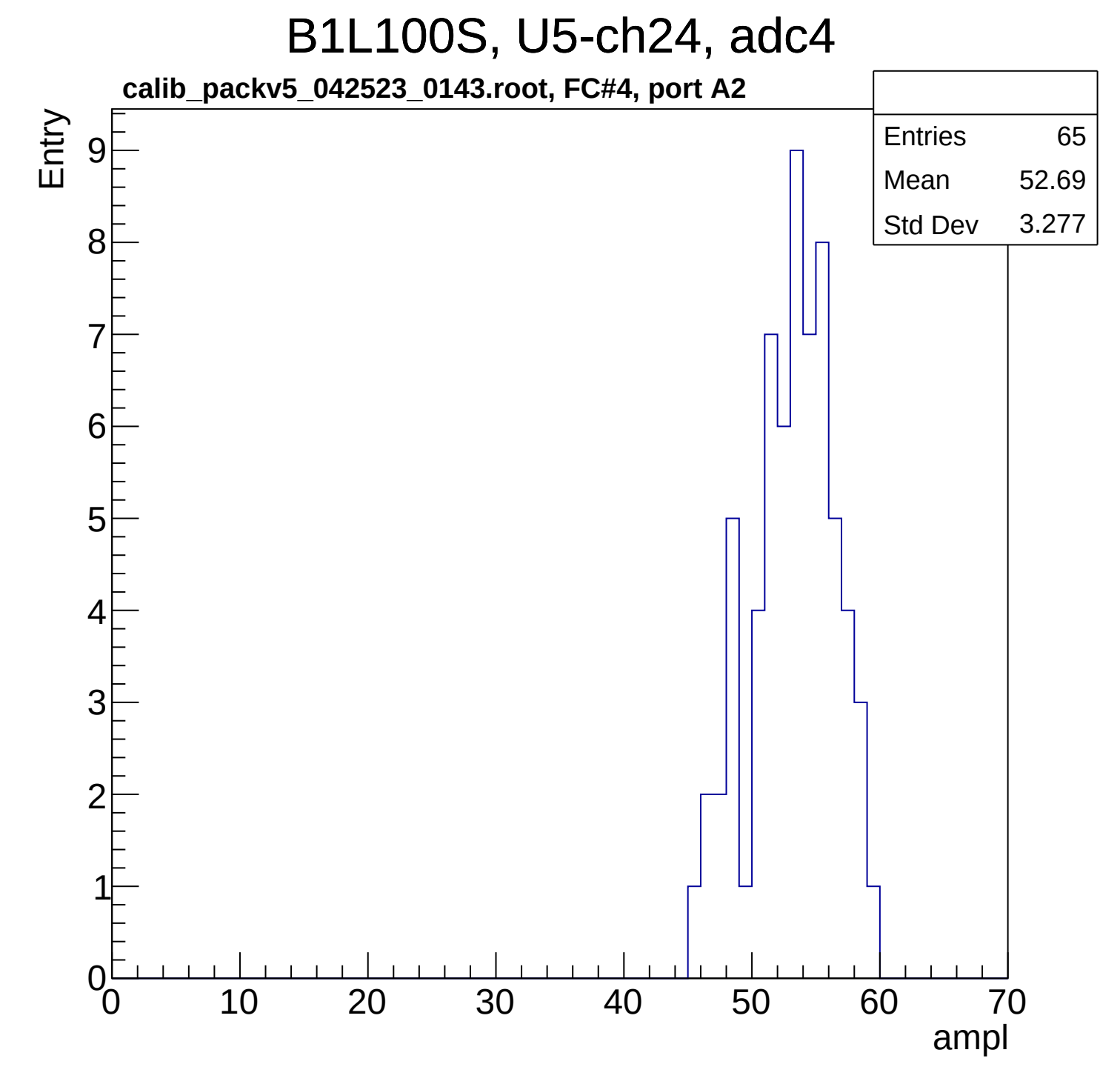
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch24, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 52.69
Std Dev 3.277
Entry
ampl
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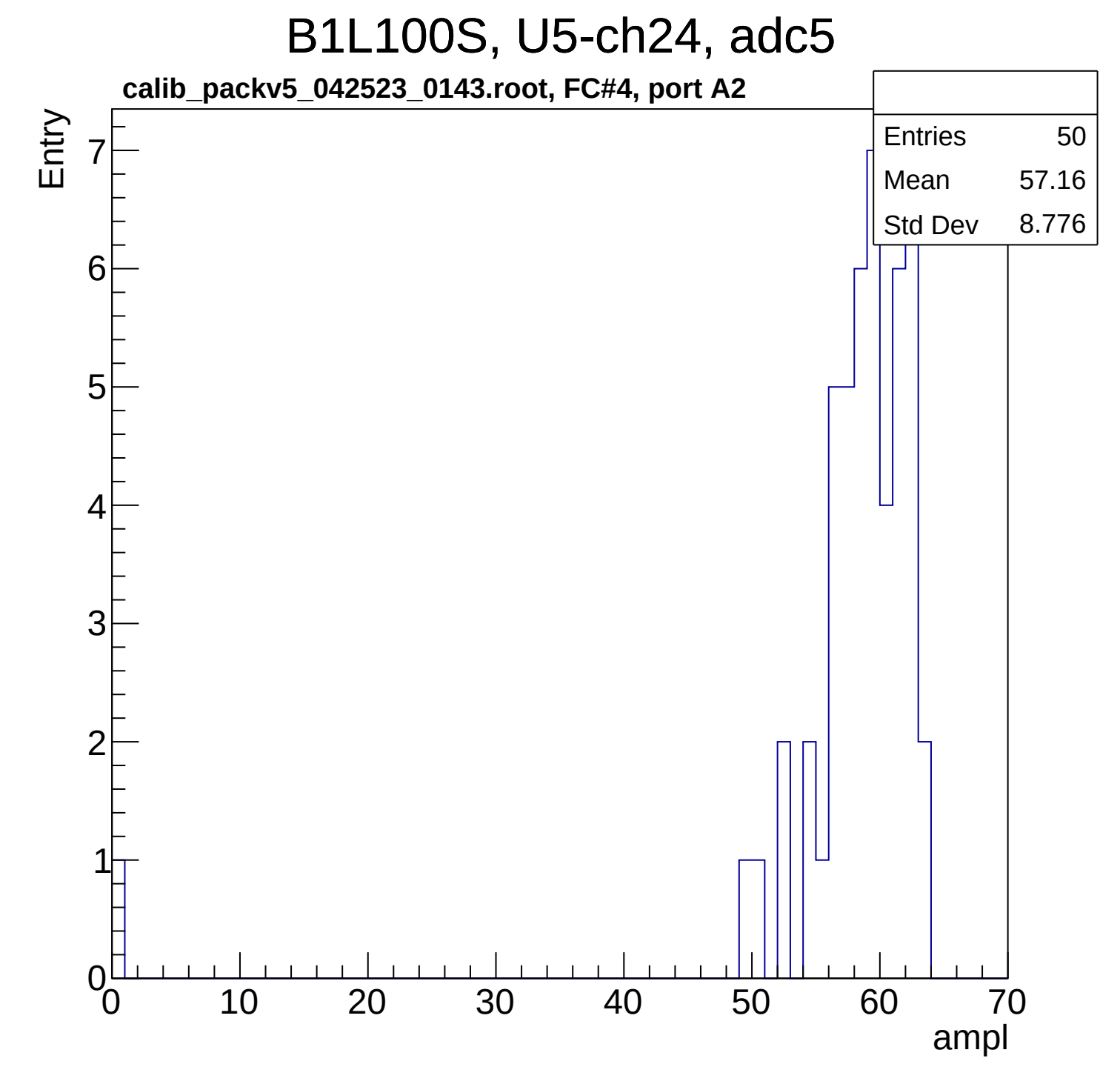
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch24, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 57.16
Std Dev 8.776
Entry
ampl
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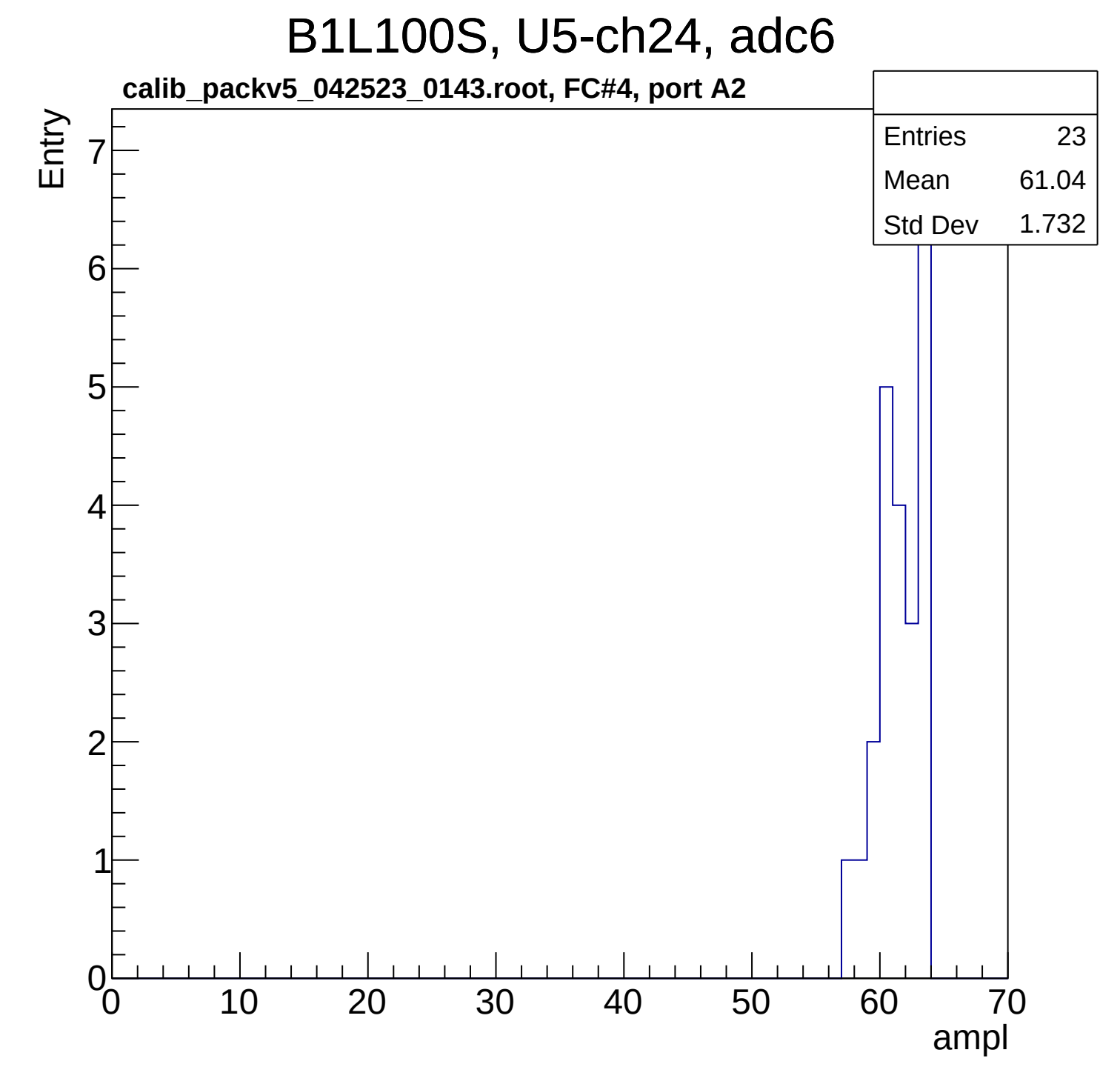
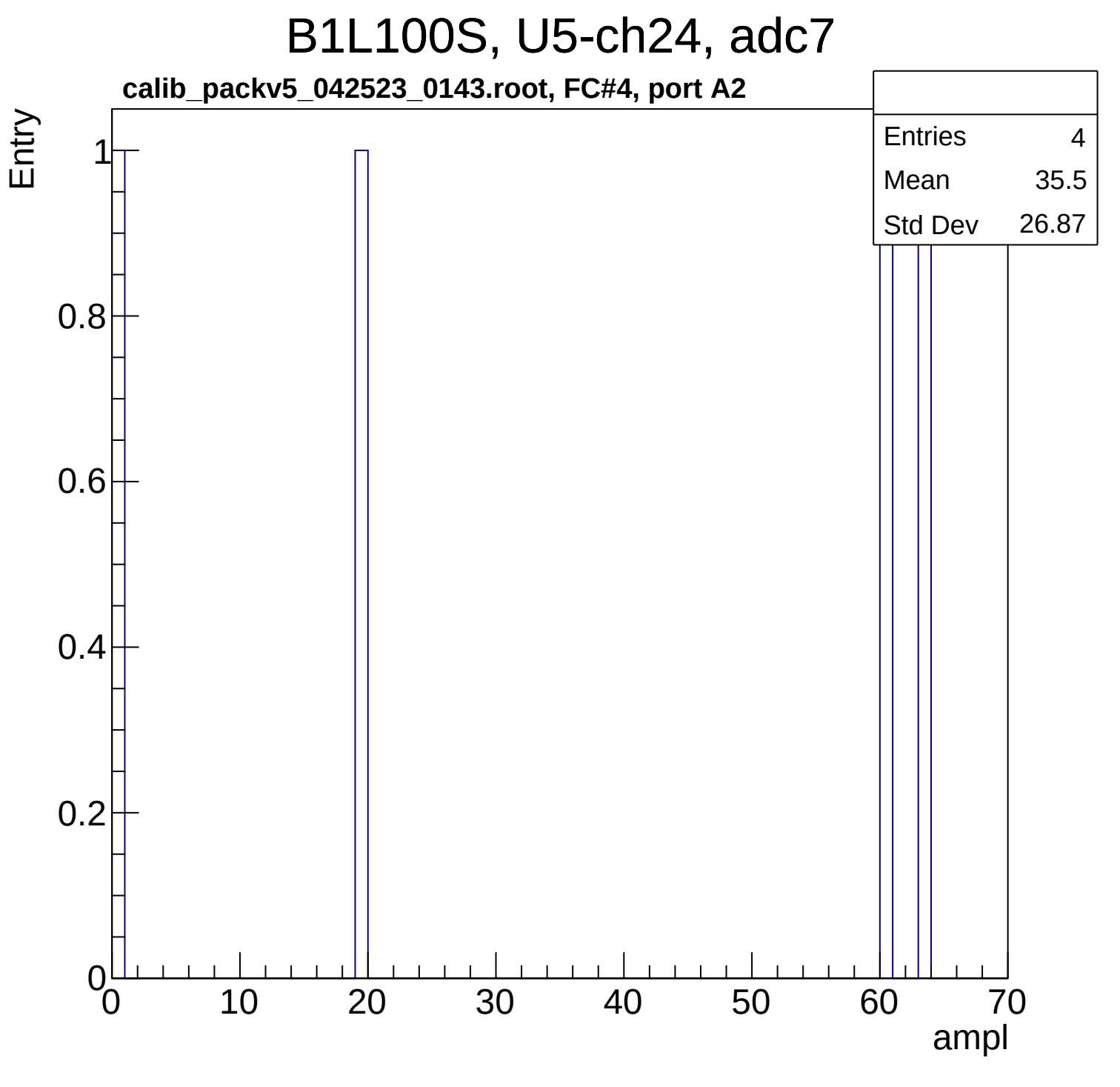
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U5-ch24, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 23
Mean 61.04
Std Dev 1.732
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U5-ch24, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 4
Mean 35.5
Std Dev 26.87
Entry
ampl
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0.2
0.4
0.6
0.8
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0
10
20
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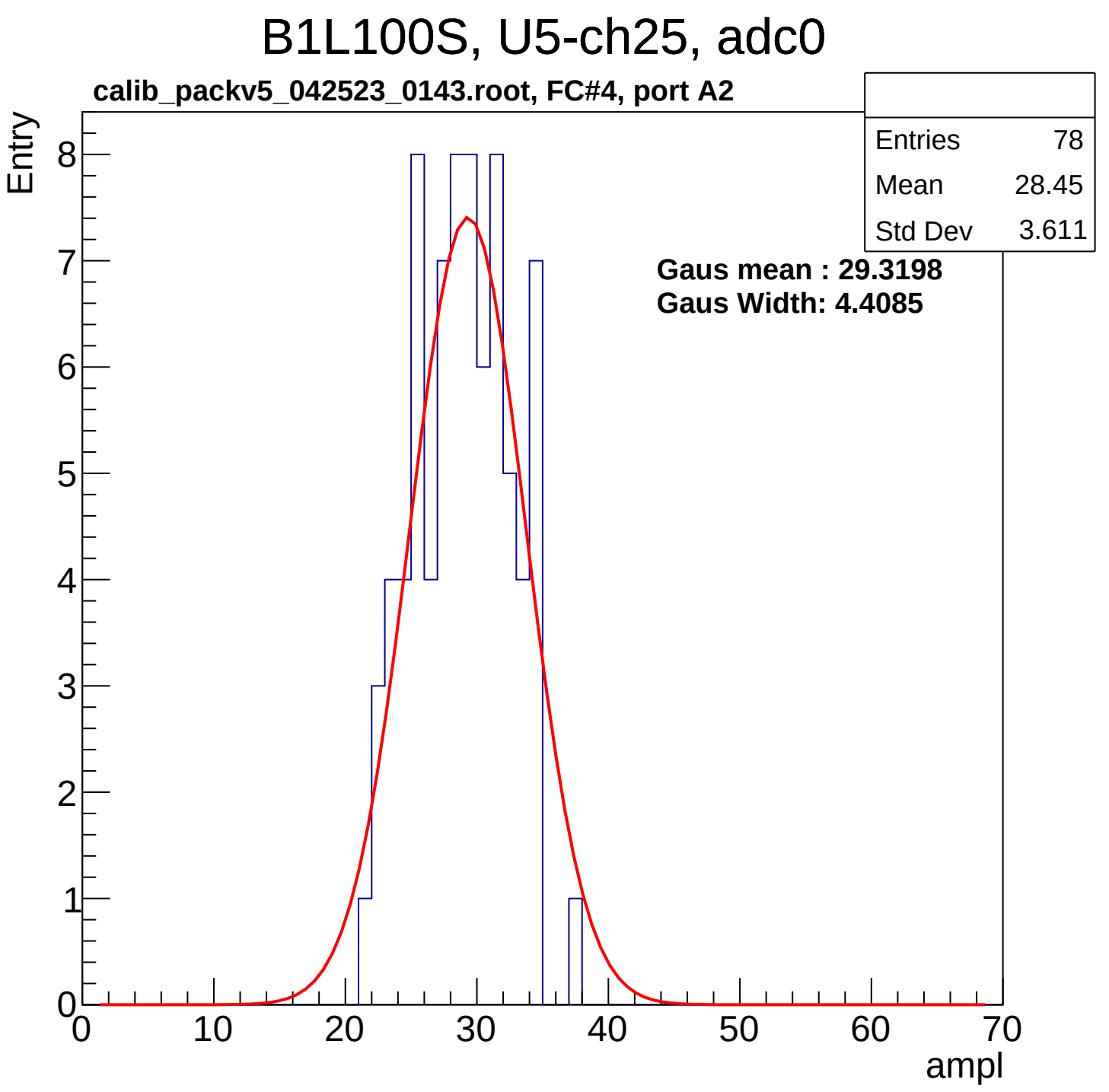
40
50
60
70


B1L100S, U5-ch25, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 78
Mean 28.45
Std Dev 3.611
Gaus mean : 29.3198
Gaus Width: 4.4085
Entry
ampl
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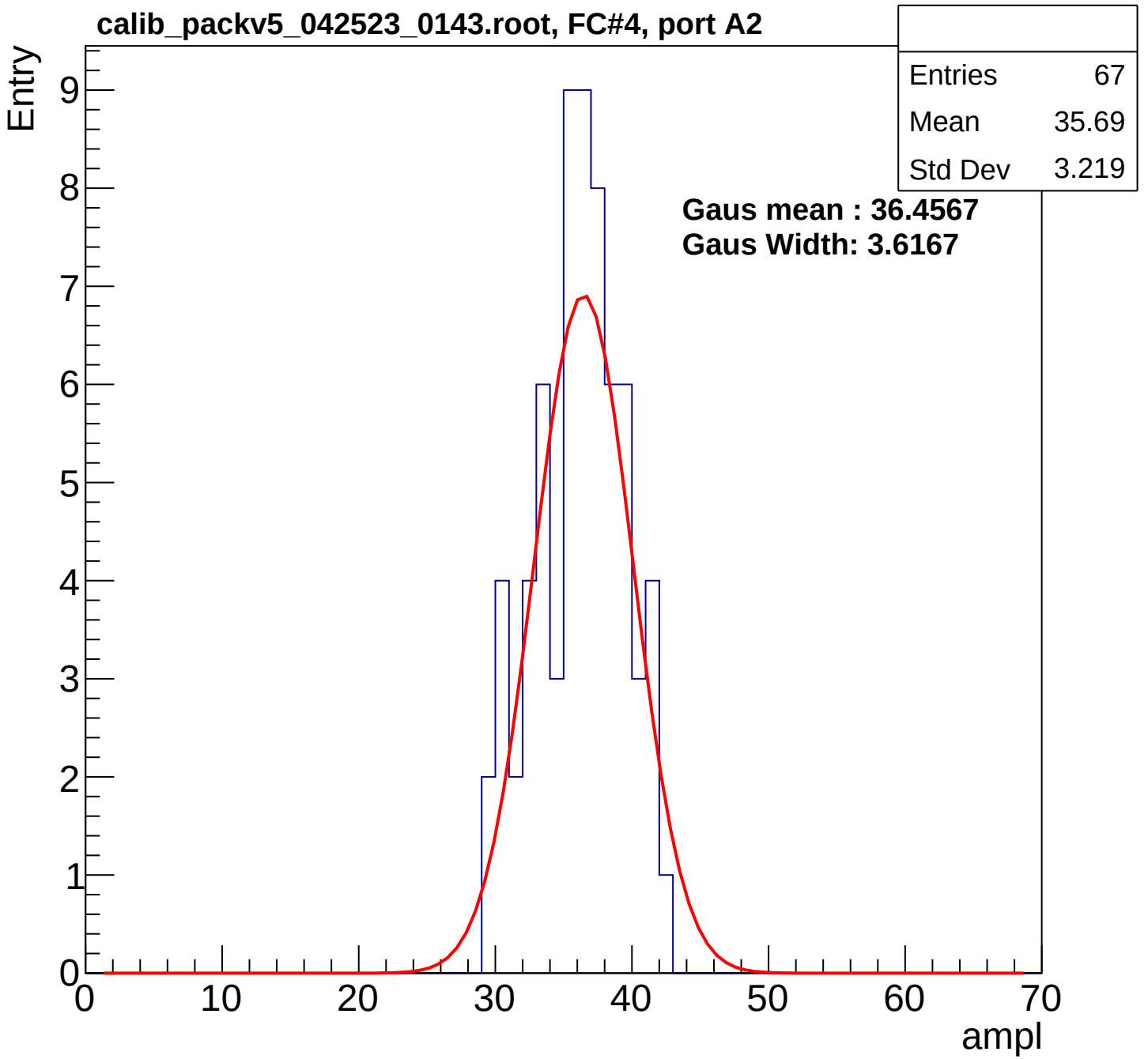
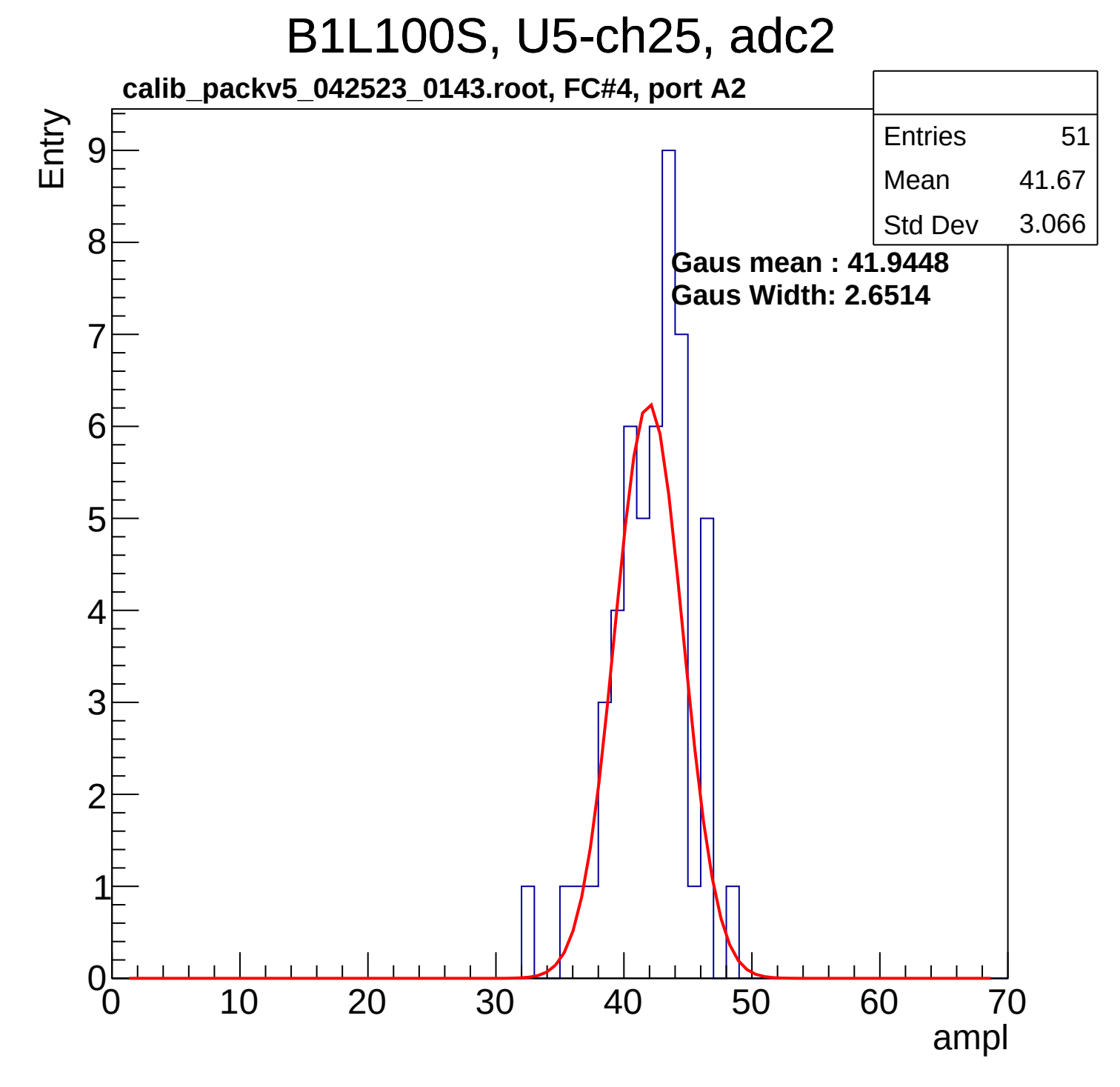
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch25, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 35.69
Std Dev 3.219
Gaus mean : 36.4567
Gaus Width: 3.6167
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch25, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 41.67
Std Dev 3.066
Gaus mean : 41.9448
Gaus Width: 2.6514
Entry
ampl
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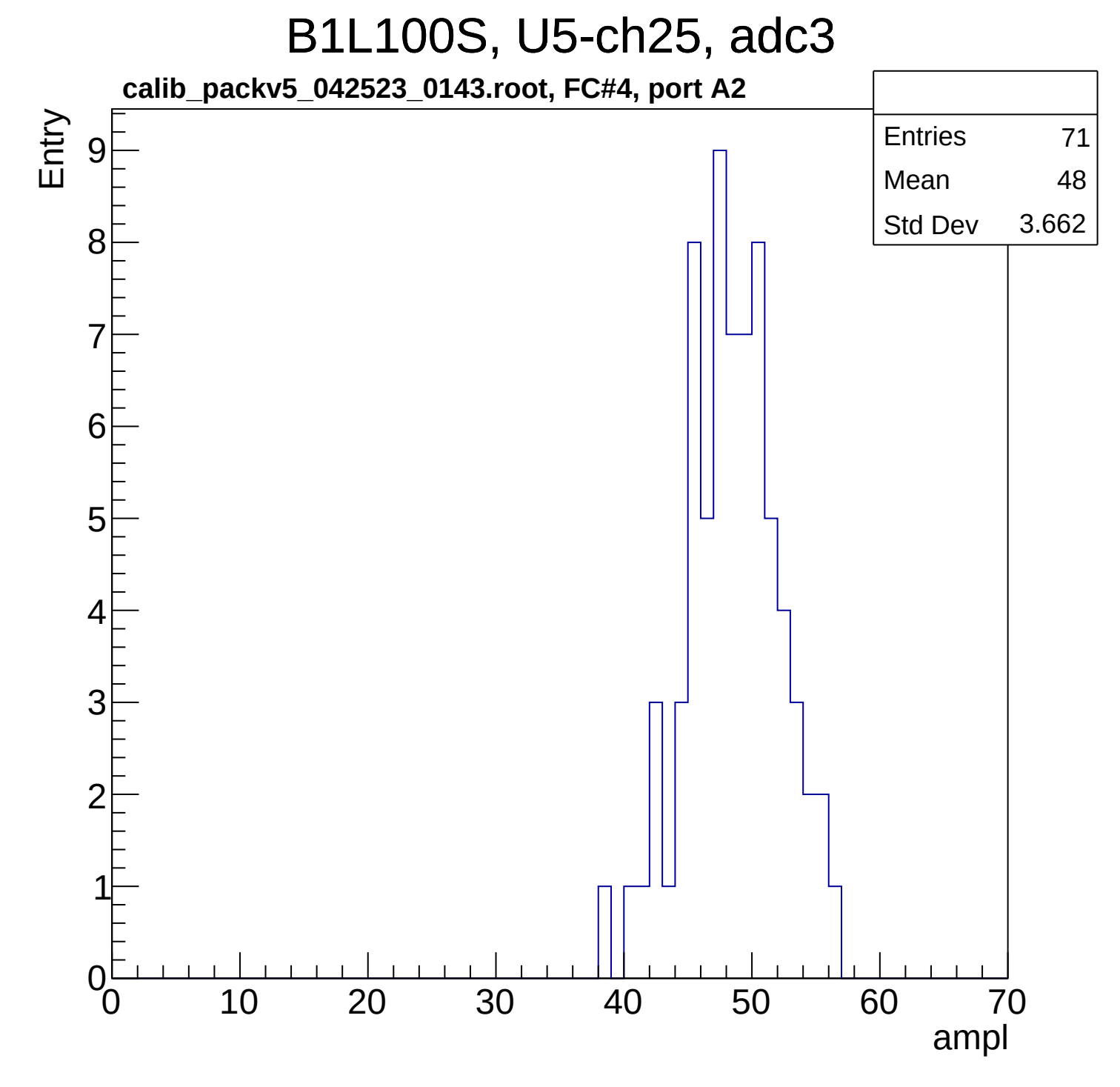
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch25, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 48
Std Dev 3.662
Entry
ampl
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2
3
4
5
6
7
8
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0
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60
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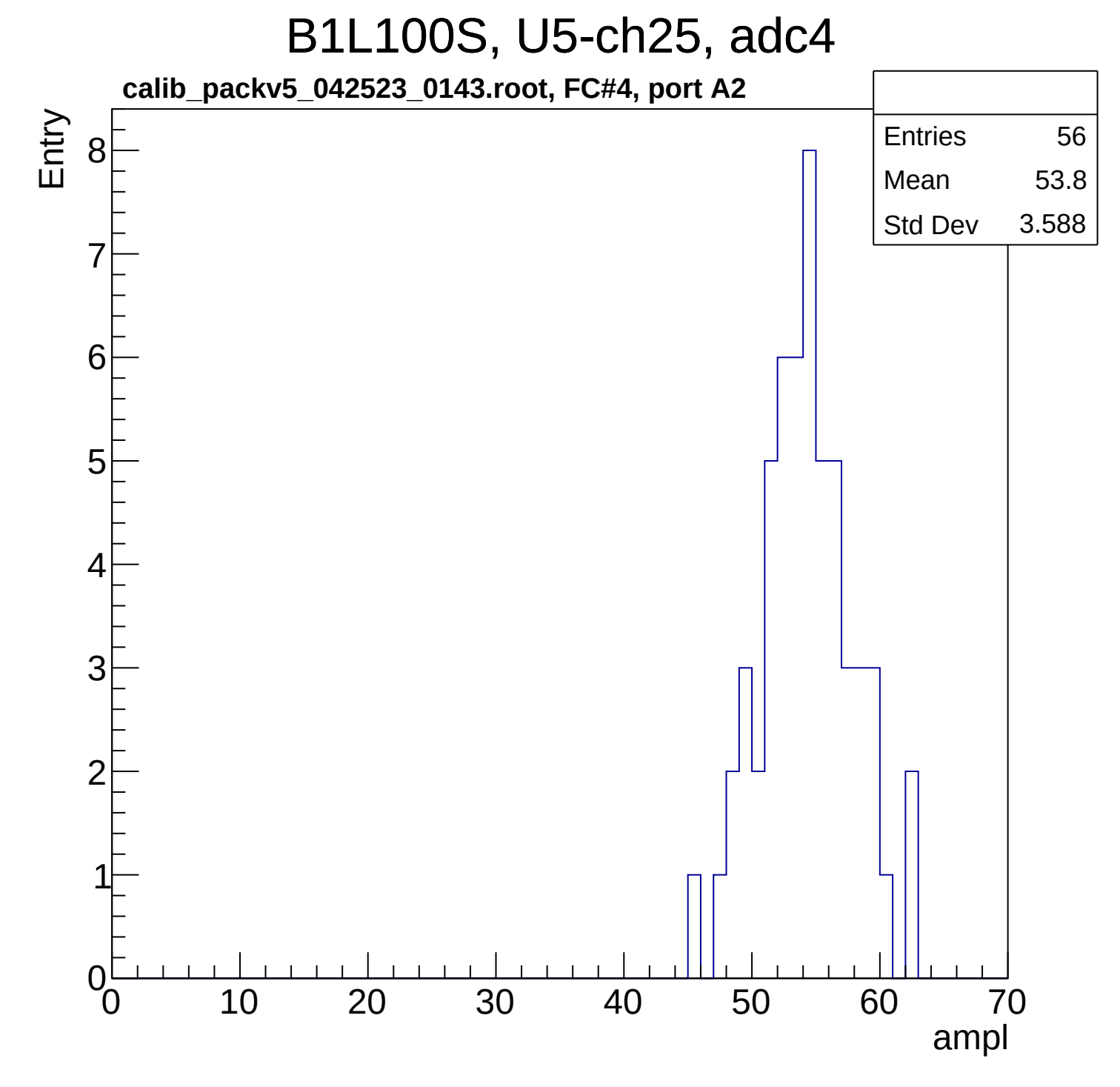
B1L100S, U5-ch25, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 53.8
Std Dev 3.588
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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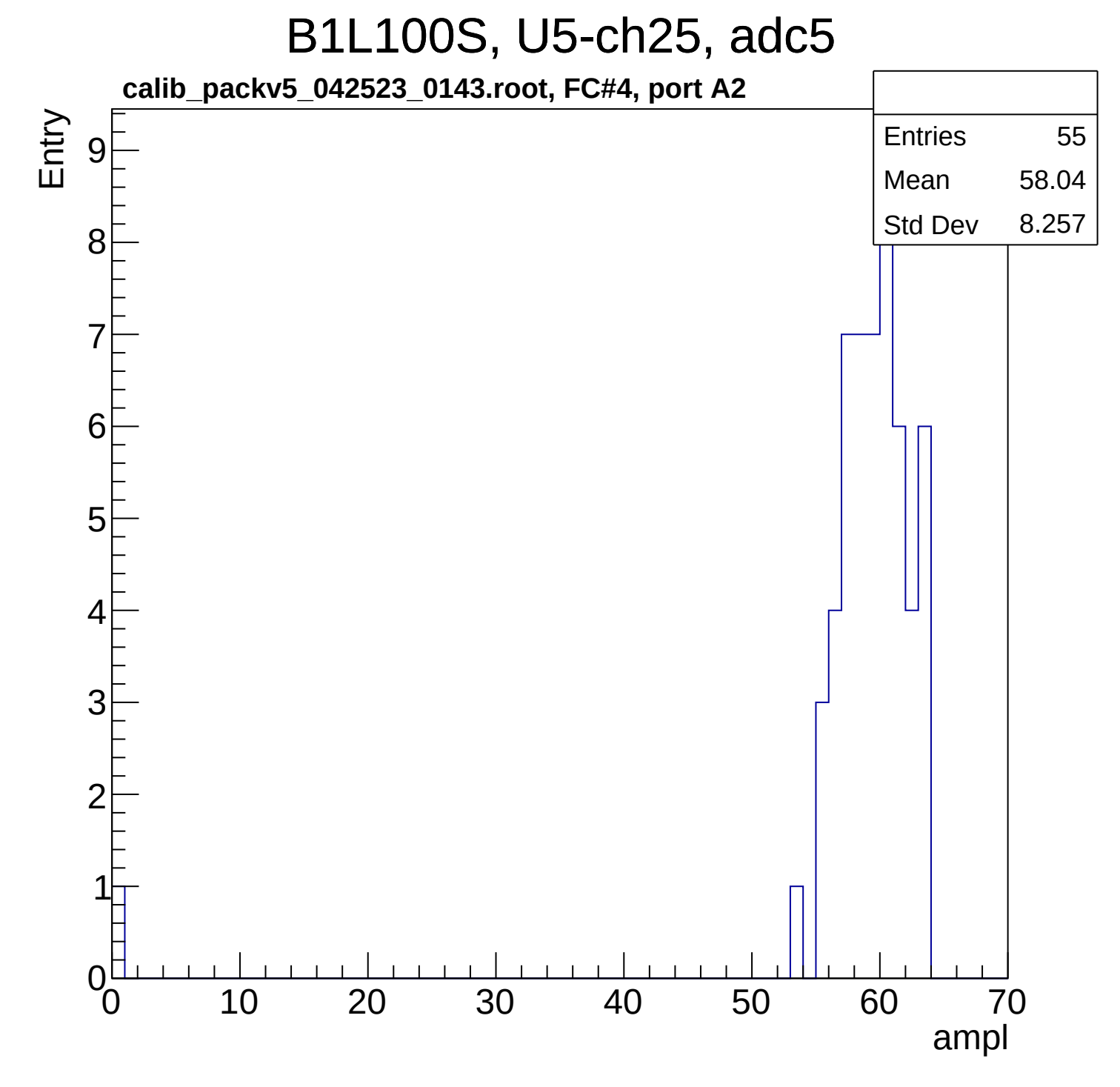
B1L100S, U5-ch25, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 58.04
Std Dev 8.257
Entry
ampl
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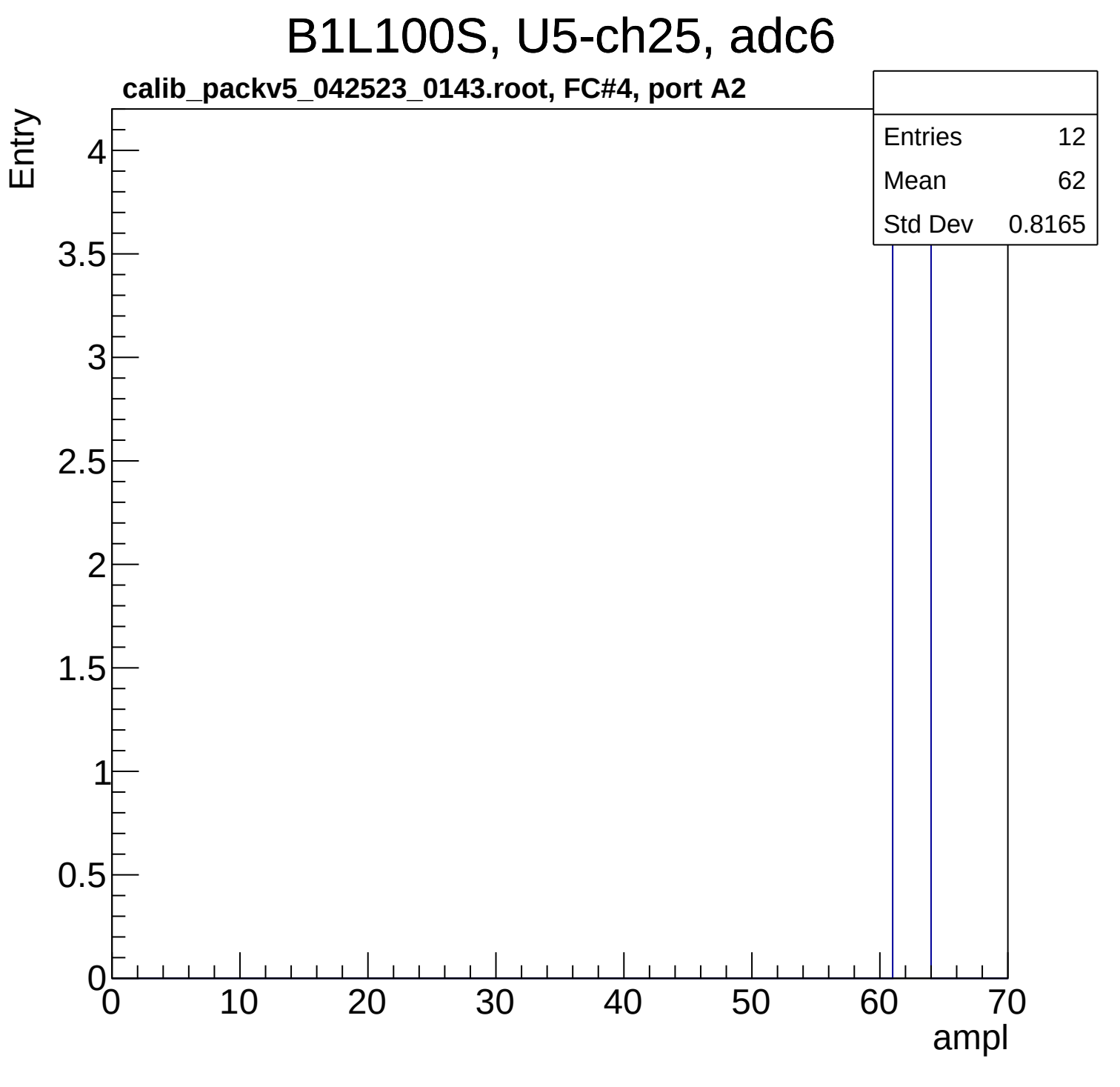
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch25, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 12
Mean 62
Std Dev 0.8165
Entry
ampl
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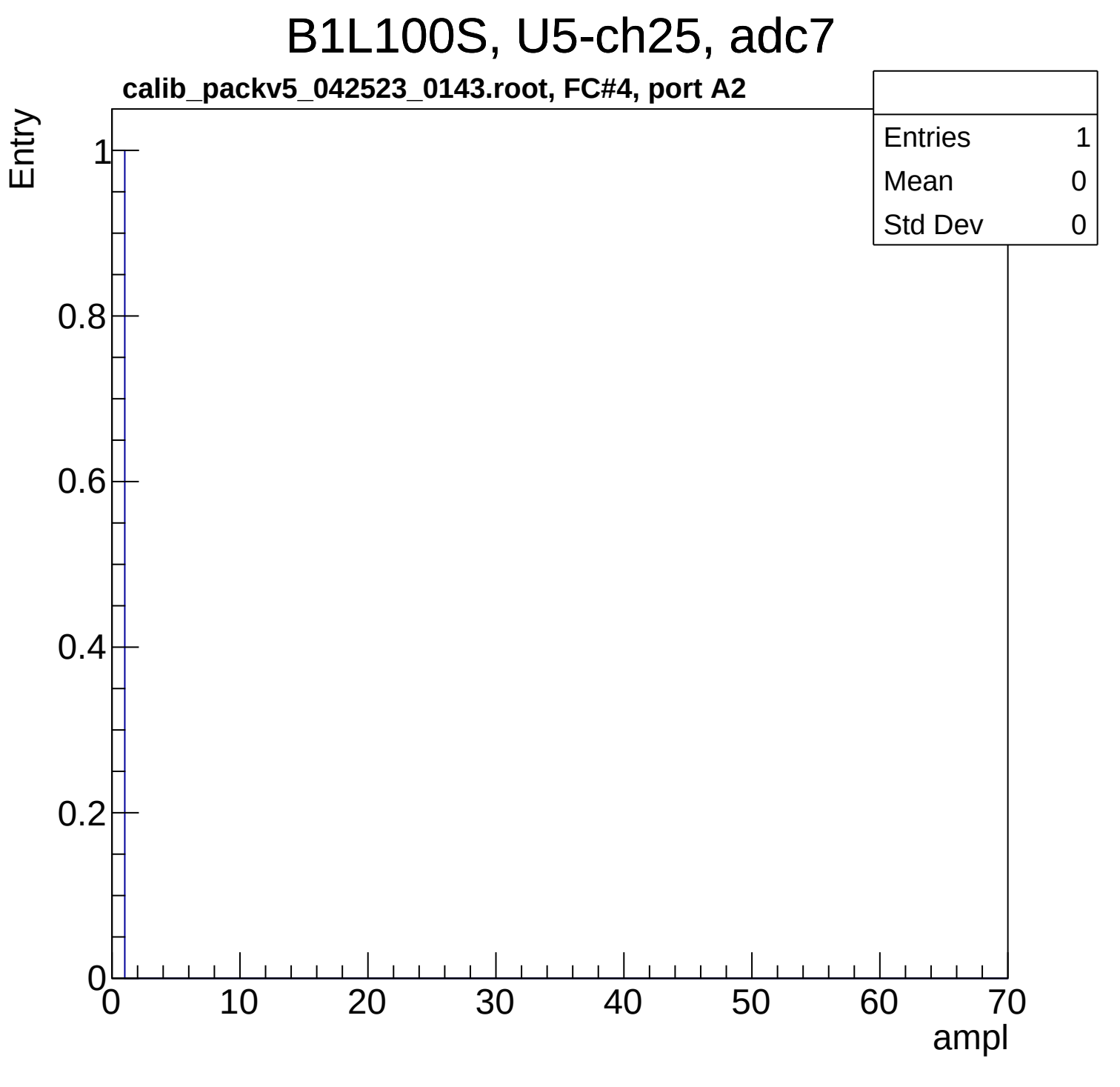
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L100S, U5-ch25, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
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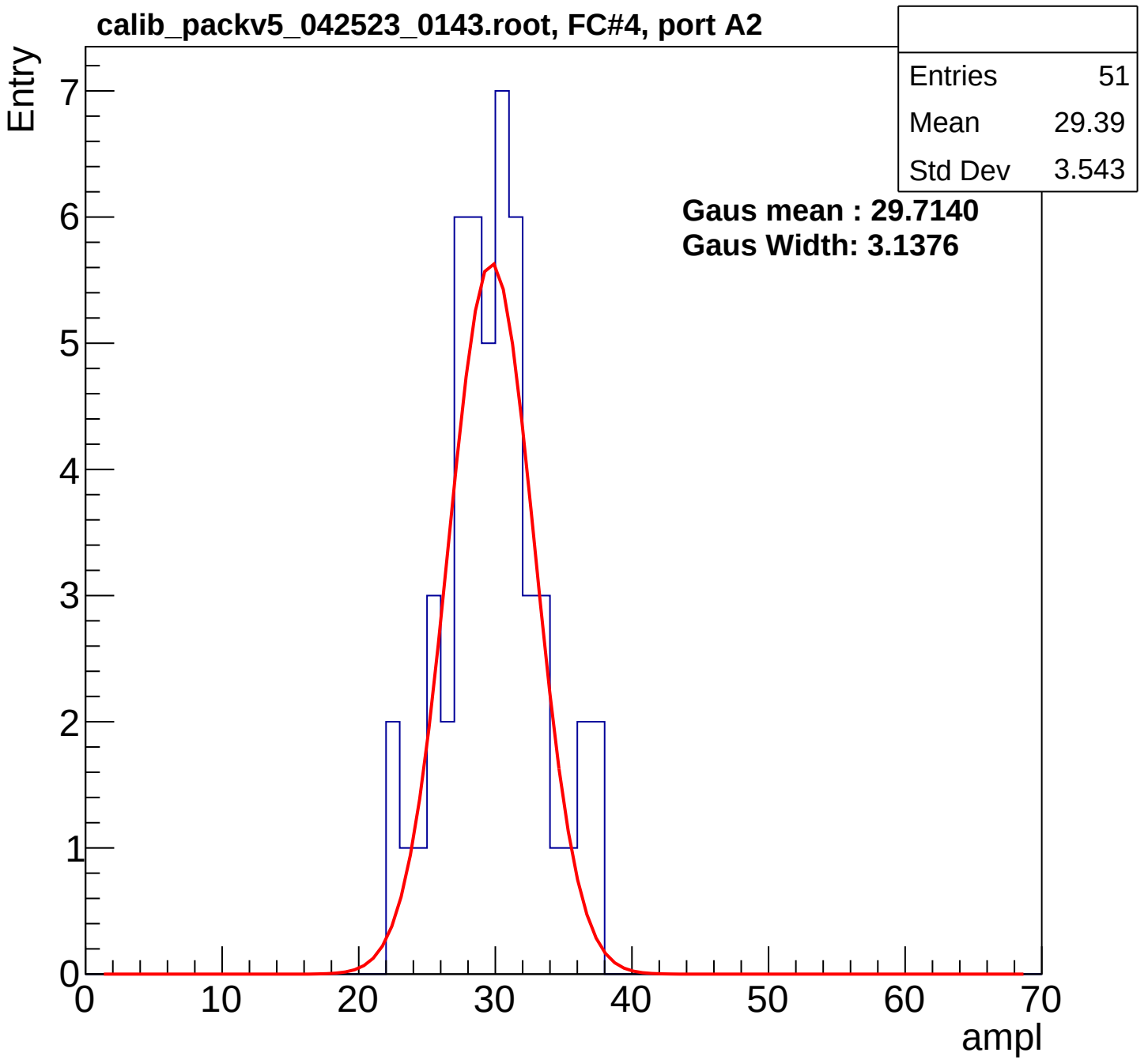
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch26, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 29.39
Std Dev 3.543
Gaus mean : 29.7140
Gaus Width: 3.1376
Entry
ampl
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1
2
3
4
5
6
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10
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50
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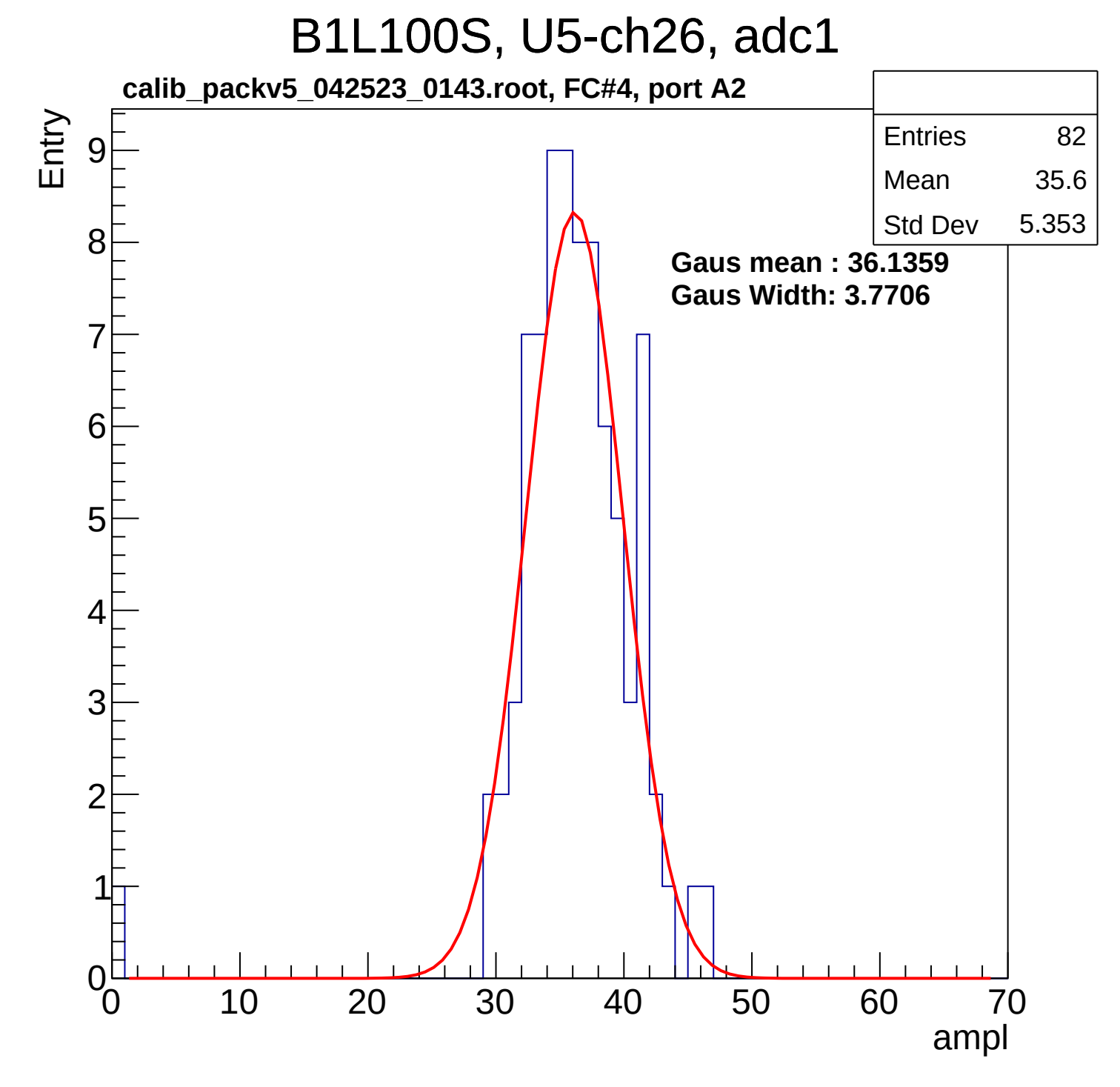
B1L100S, U5-ch26, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 82
Mean 35.6
Std Dev 5.353
Gaus mean : 36.1359
Gaus Width: 3.7706
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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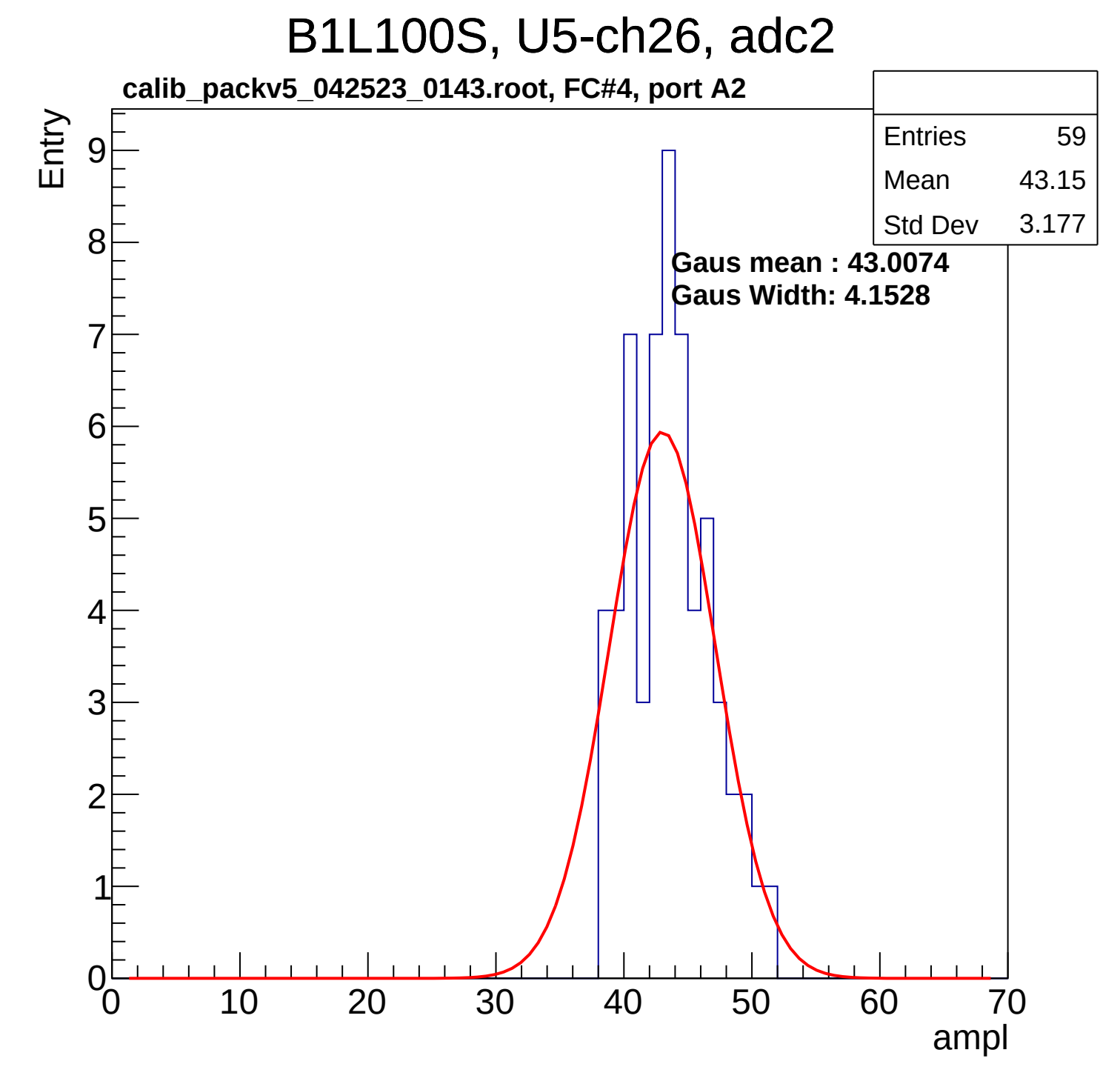
60
70


B1L100S, U5-ch26, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 43.15
Std Dev 3.177
Gaus mean : 43.0074
Gaus Width: 4.1528
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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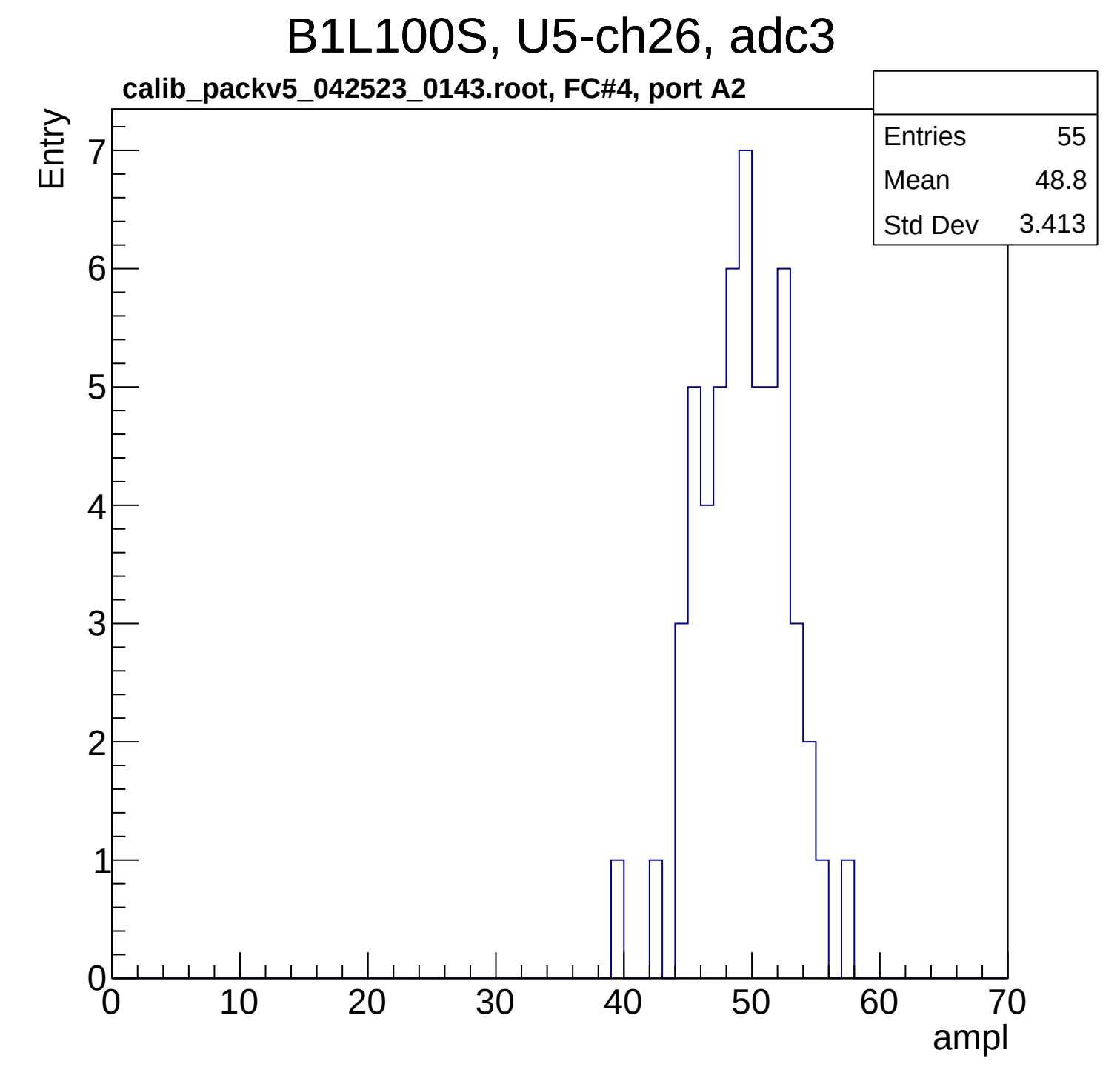
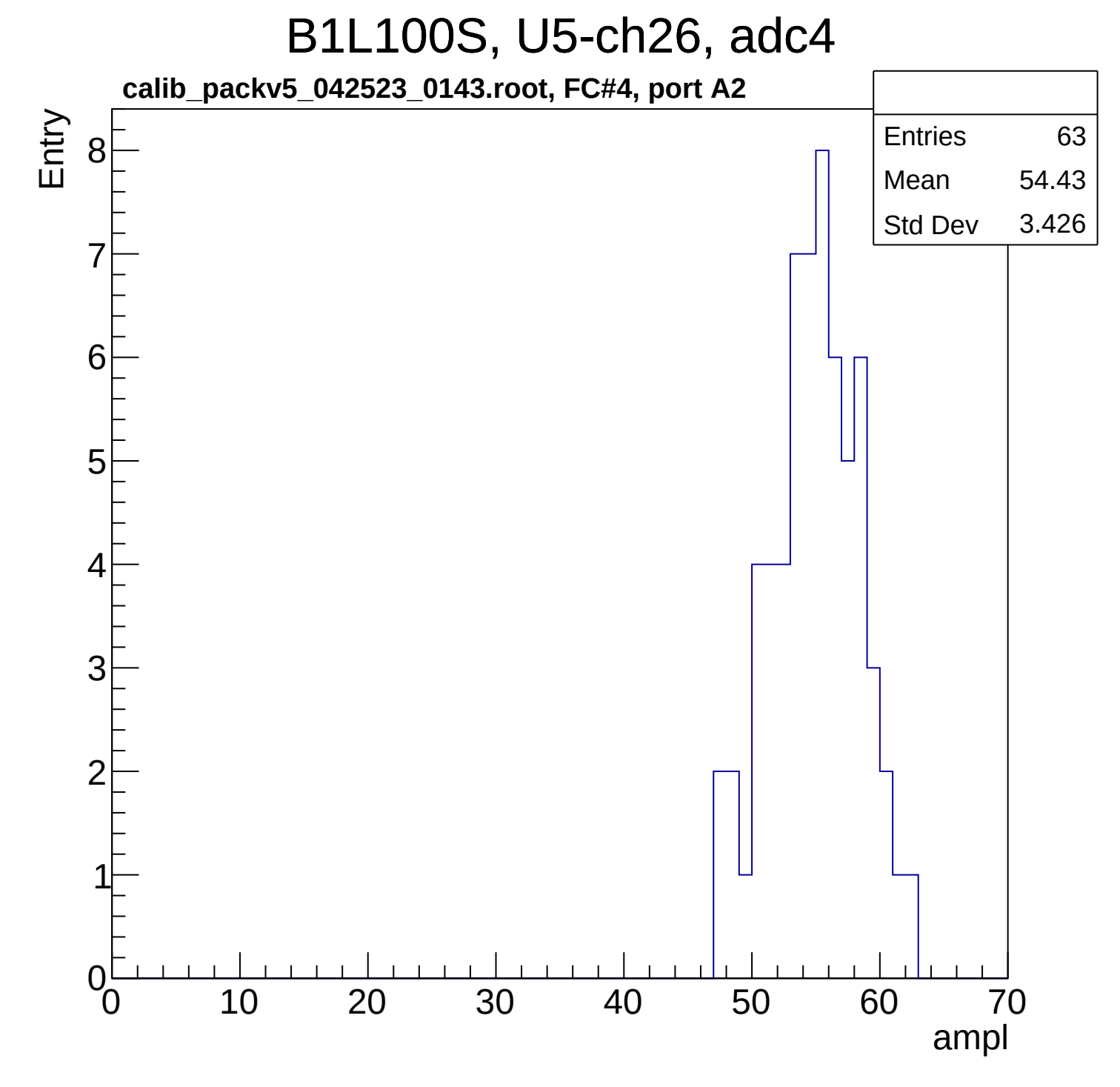
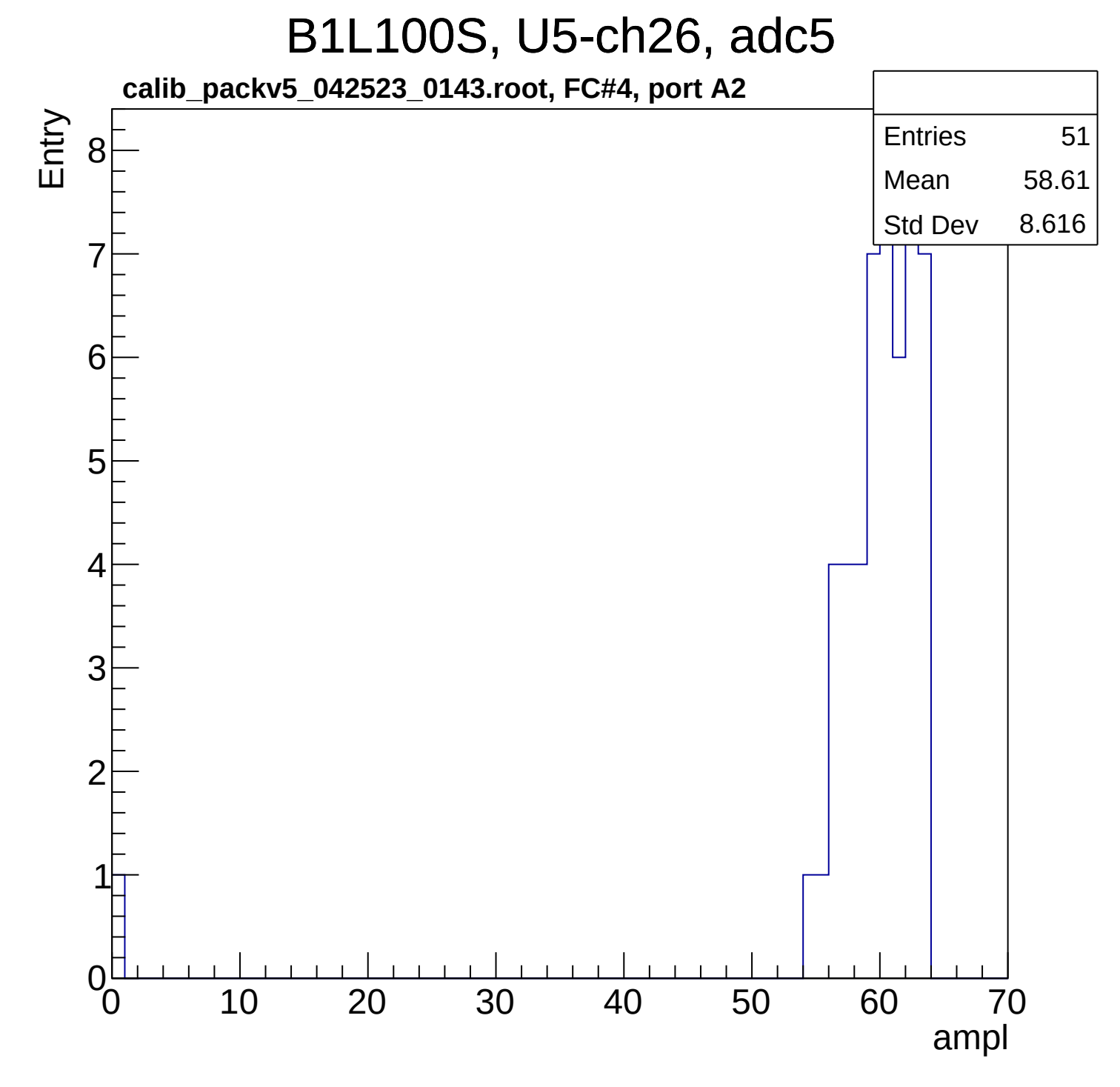

B1L100S, U5-ch26, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 48.8
Std Dev 3.413
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U5-ch26, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 54.43
Std Dev 3.426
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch26, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 58.61
Std Dev 8.616
Entry
ampl
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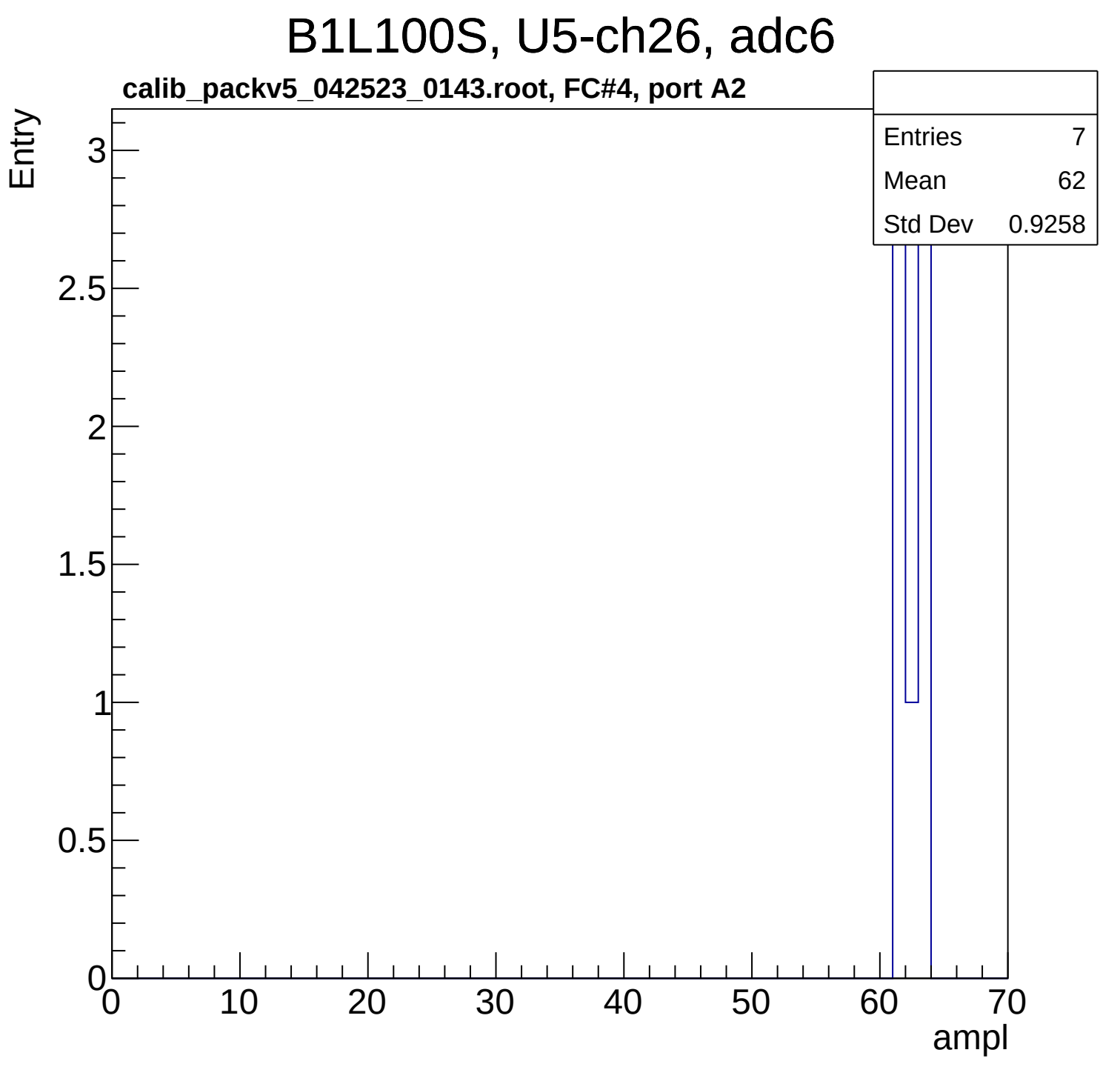
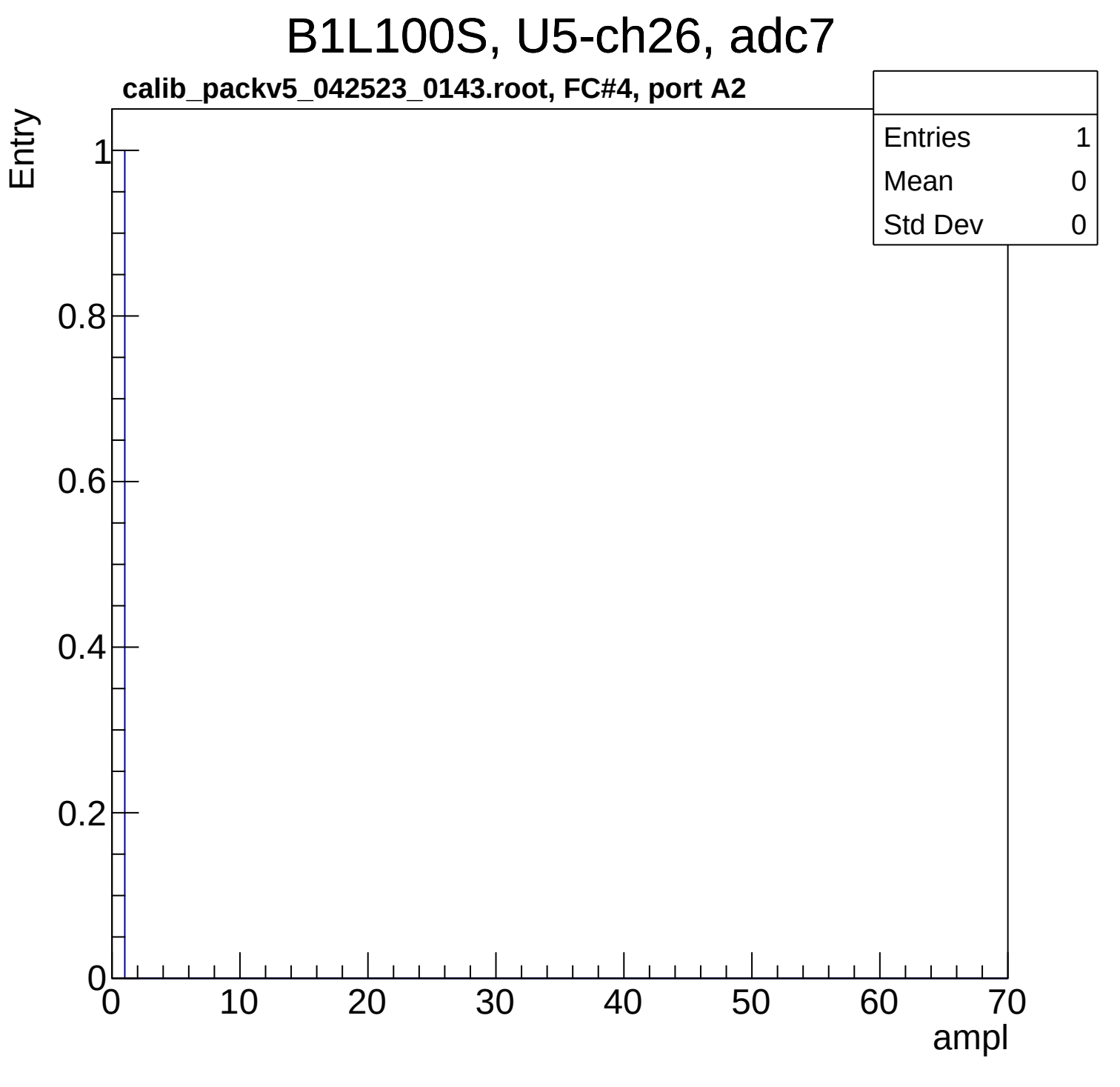
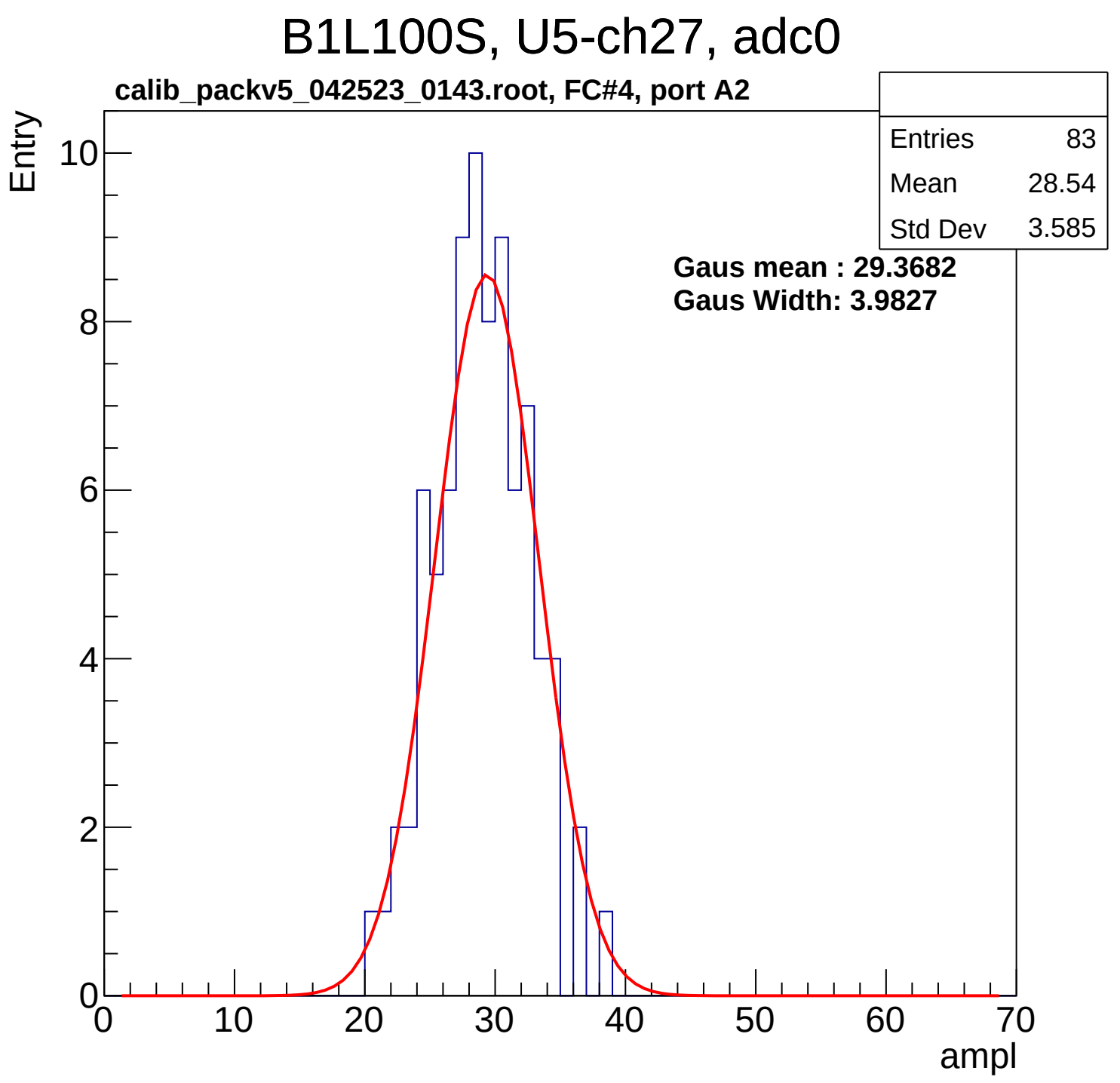
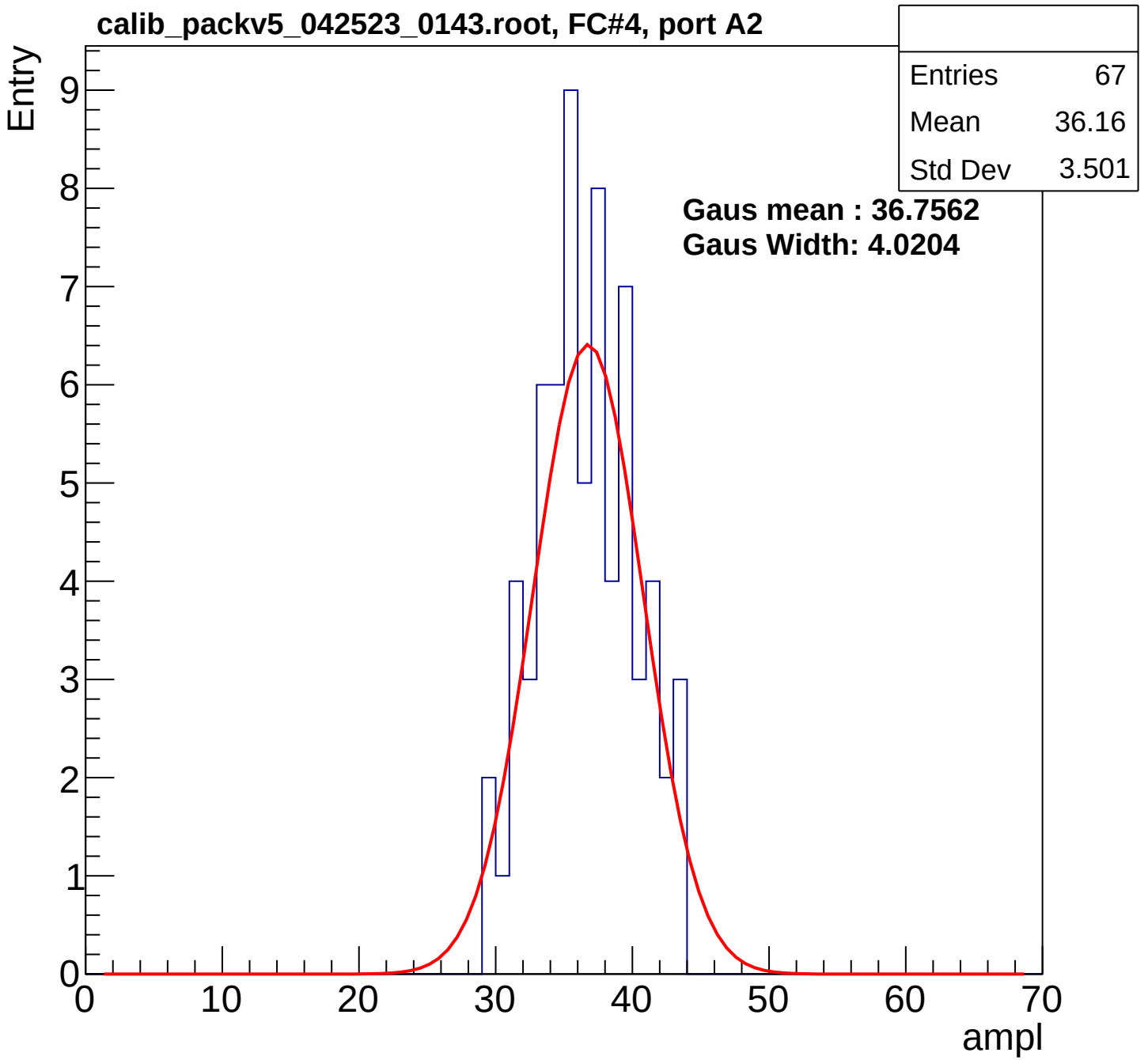
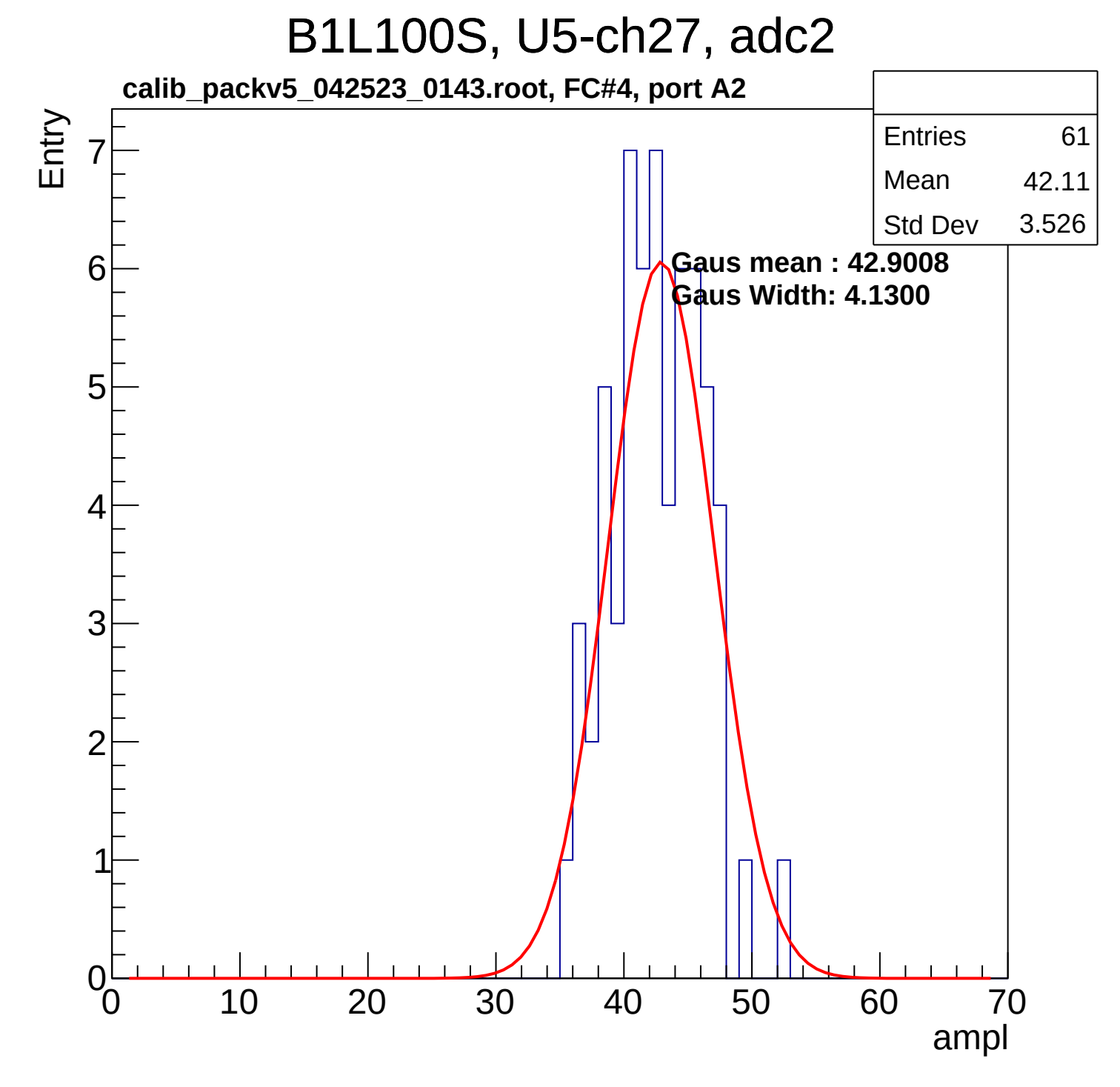
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

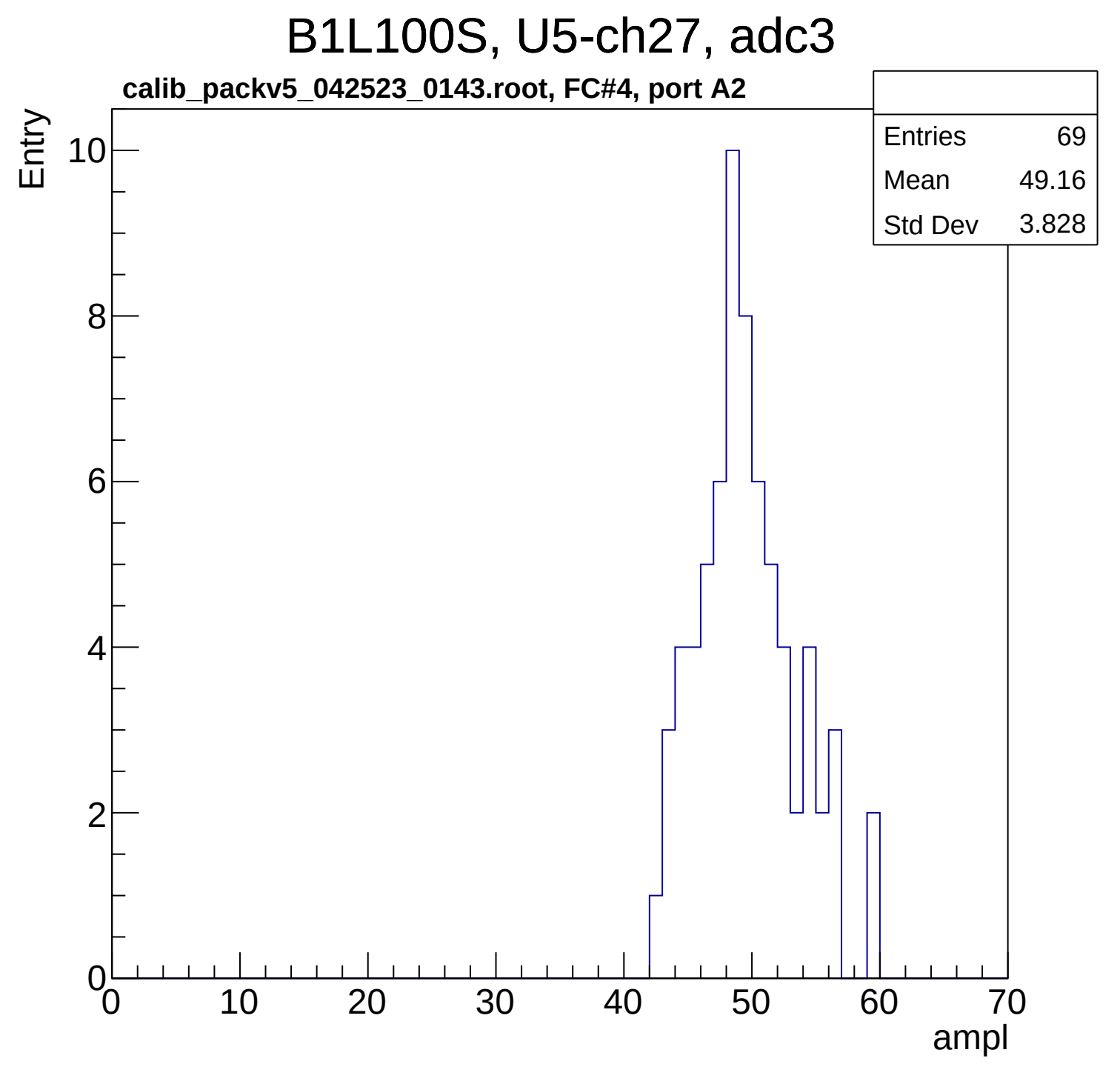

B1L100S, U5-ch26, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 7
Mean 62
Std Dev 0.9258
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

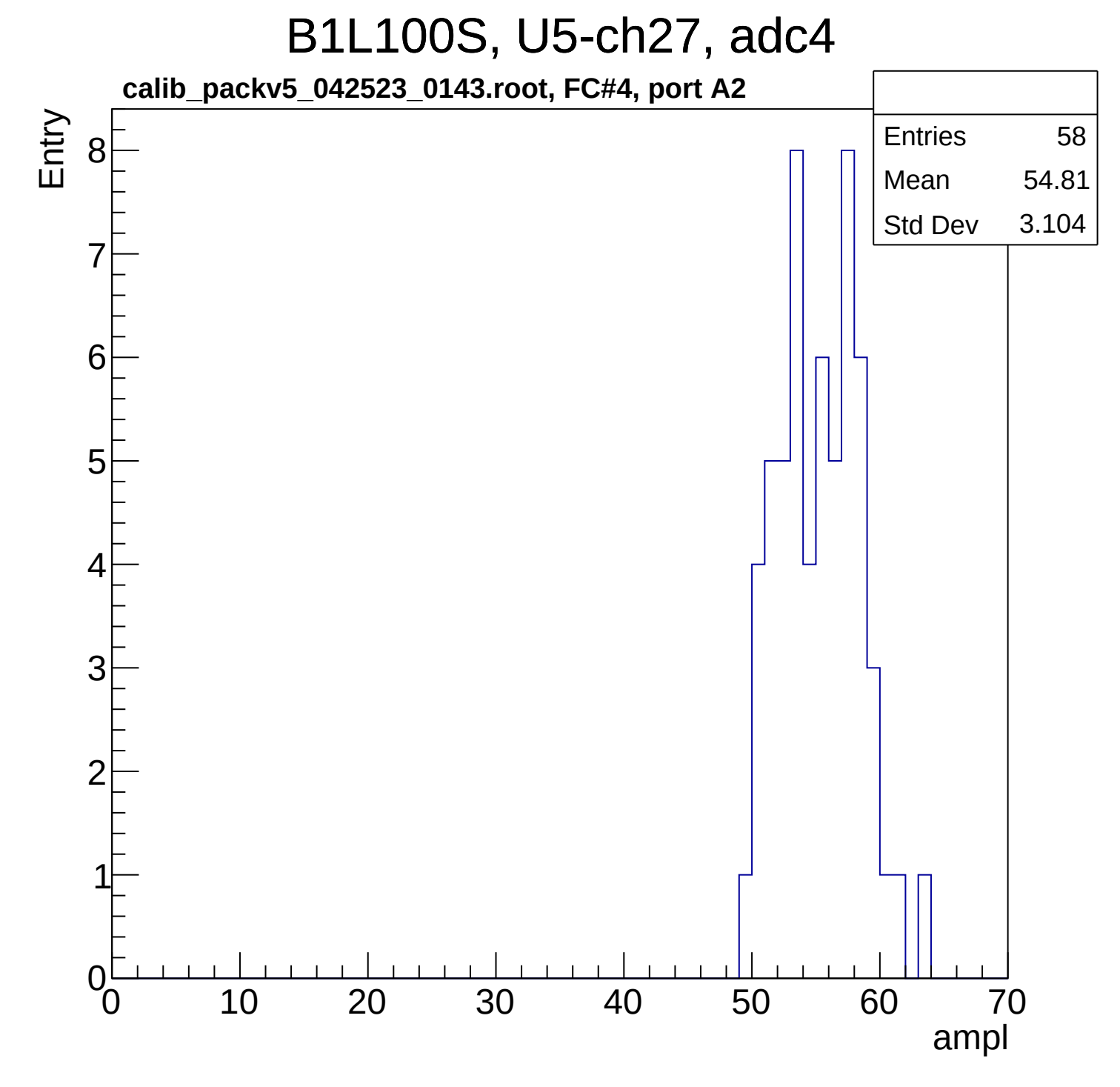

B1L100S, U5-ch26, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

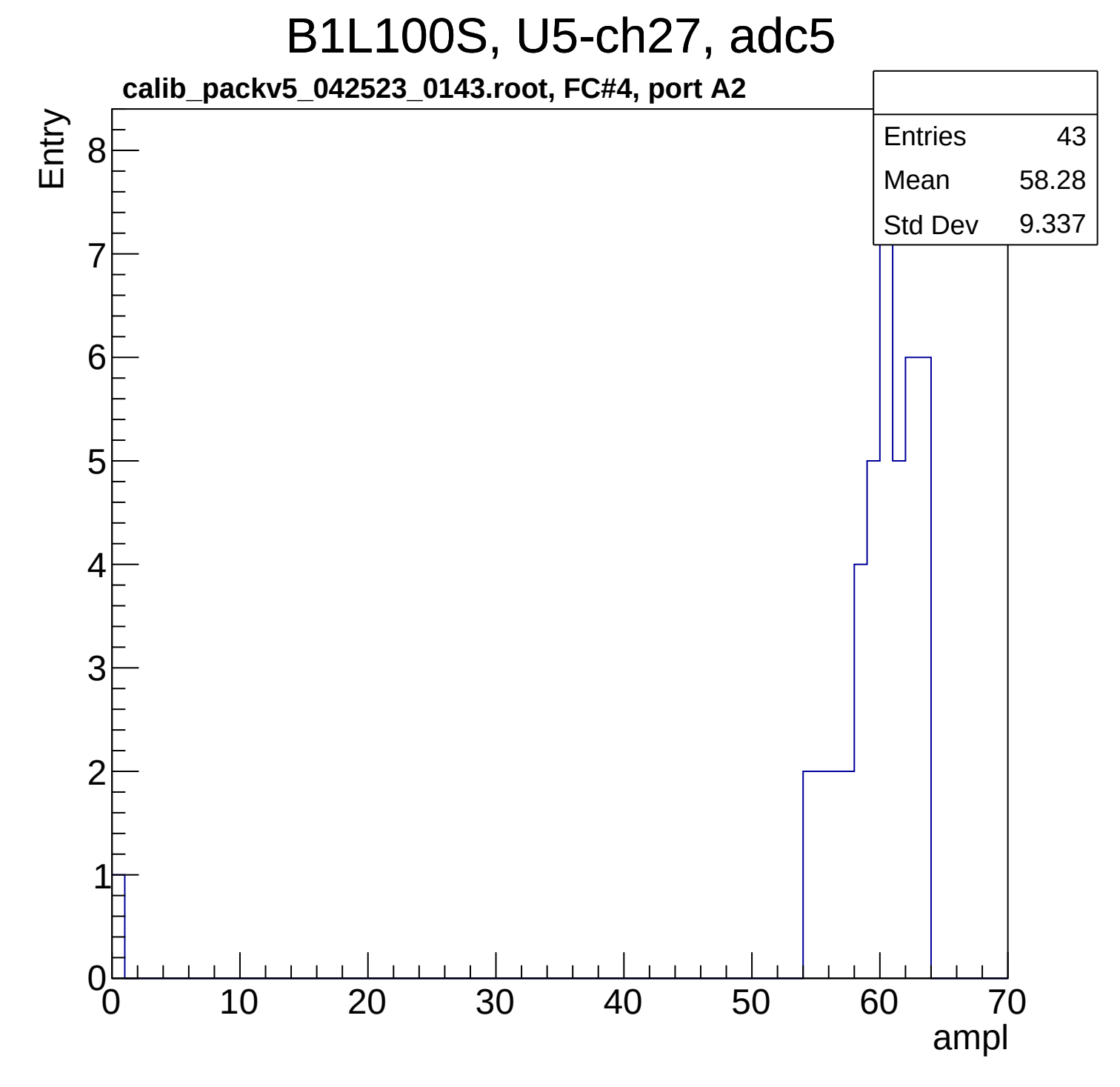

B1L100S, U5-ch27, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 83
Mean 28.54
Std Dev 3.585
Gaus mean : 29.3682
Gaus Width: 3.9827
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch27, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 36.16
Std Dev 3.501
Gaus mean : 36.7562
Gaus Width: 4.0204
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch27, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 42.11
Std Dev 3.526
Gaus mean : 42.9008
Gaus Width: 4.1300
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U5-ch27, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 49.16
Std Dev 3.828
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch27, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 54.81
Std Dev 3.104
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch27, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 43
Mean 58.28
Std Dev 9.337
Entry
ampl
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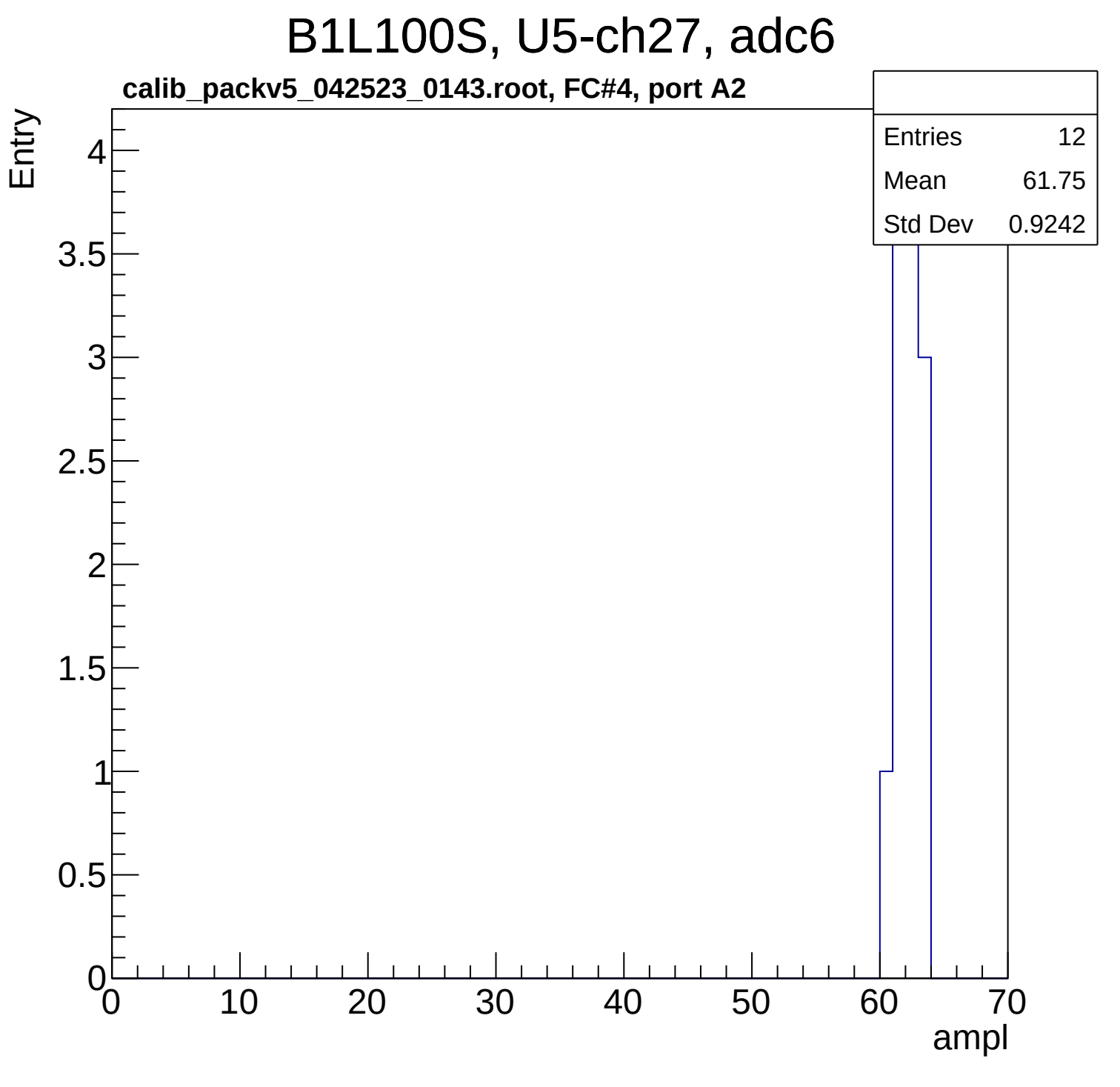
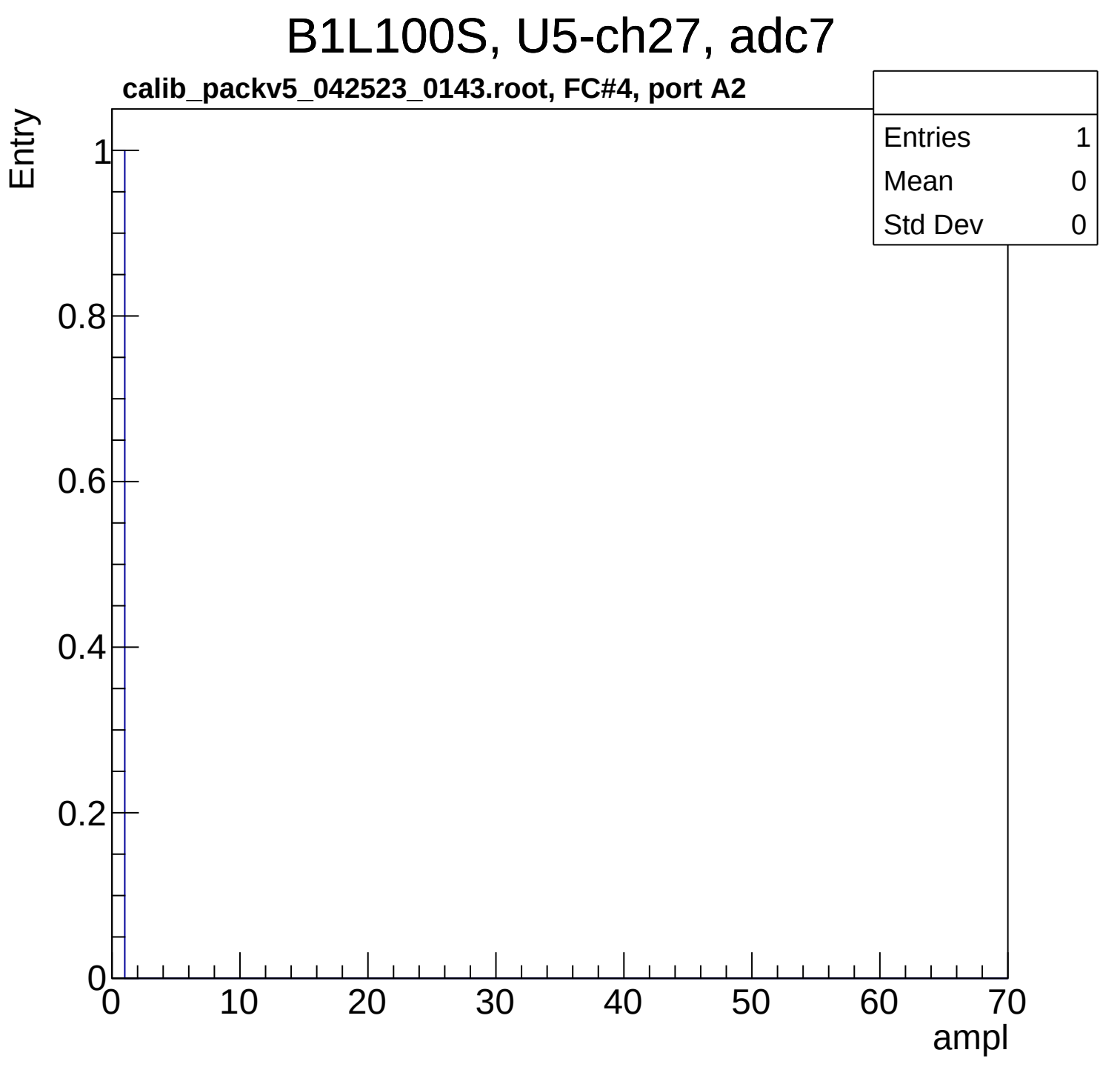
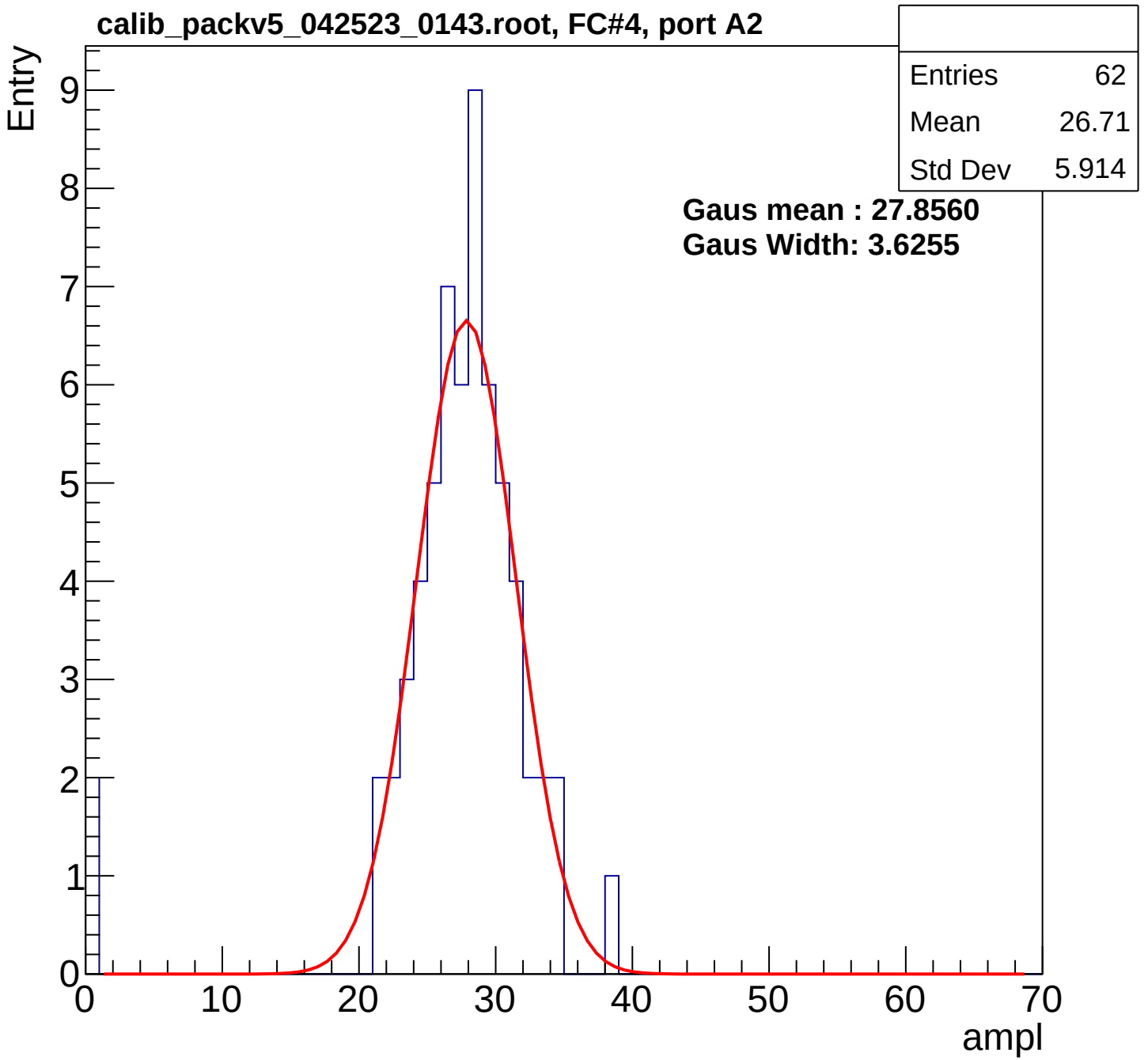
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch27, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 12
Mean 61.75
Std Dev 0.9242
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L100S, U5-ch27, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch28, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 26.71
Std Dev 5.914
Gaus mean : 27.8560
Gaus Width: 3.6255
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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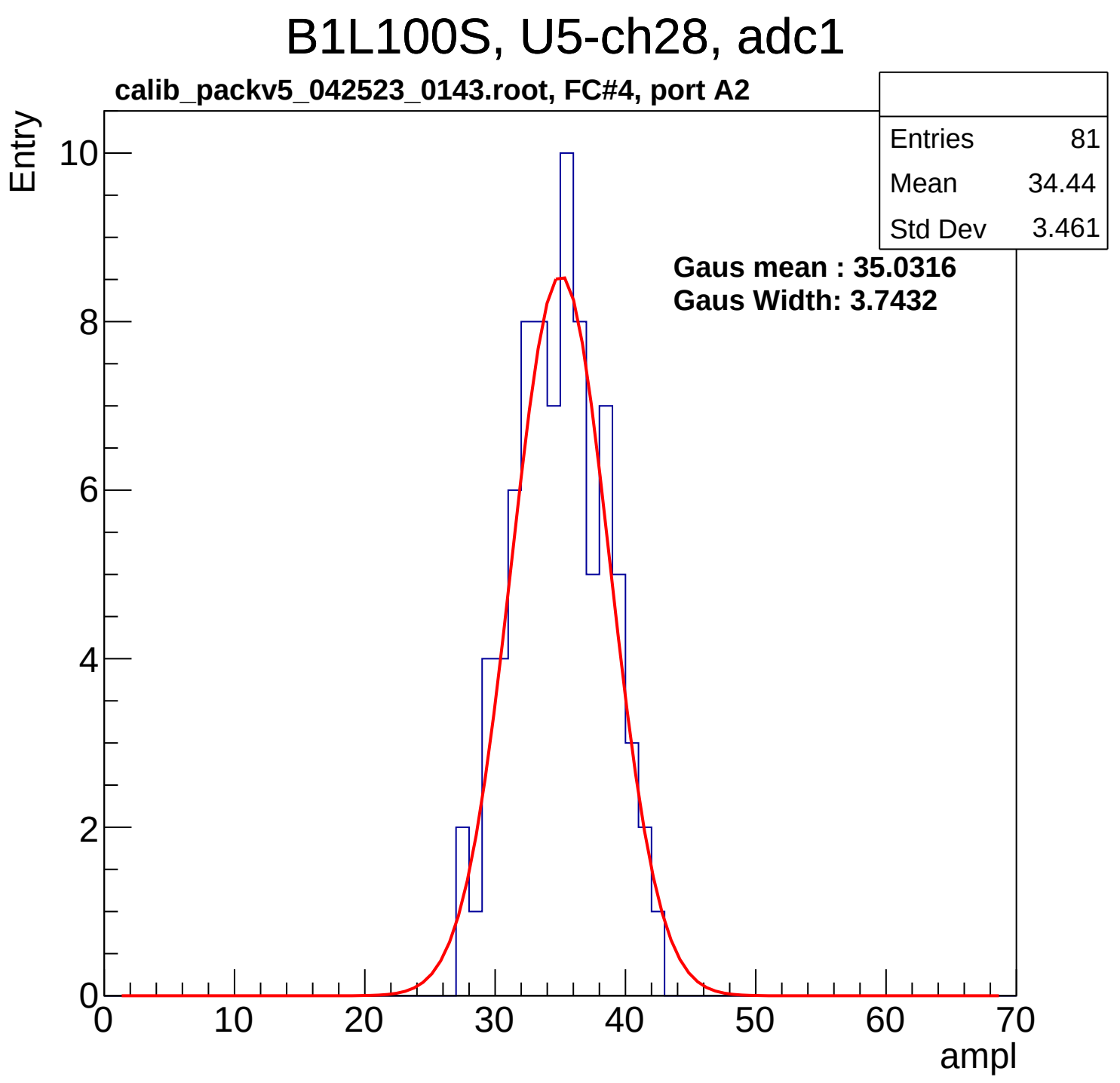
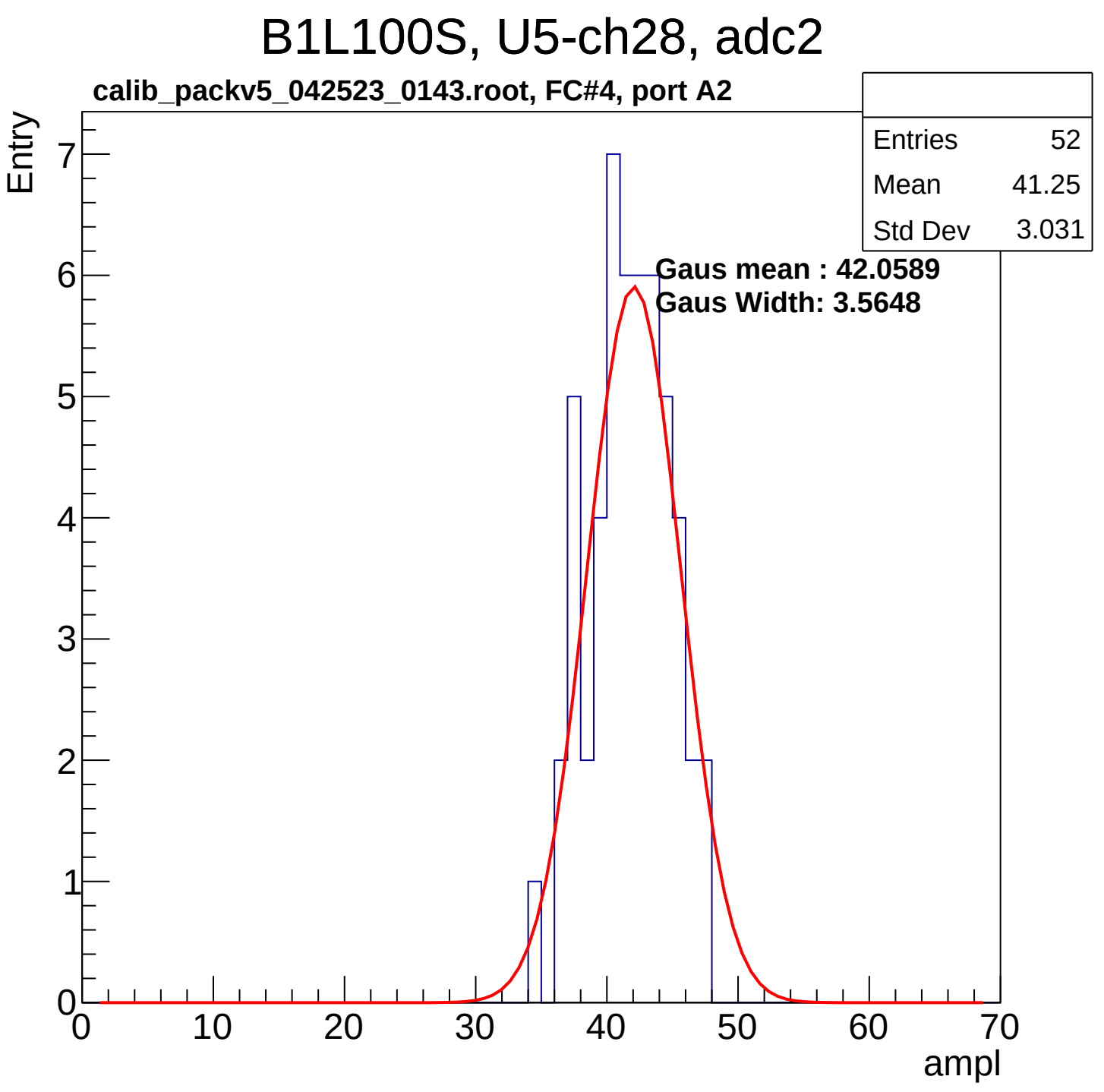
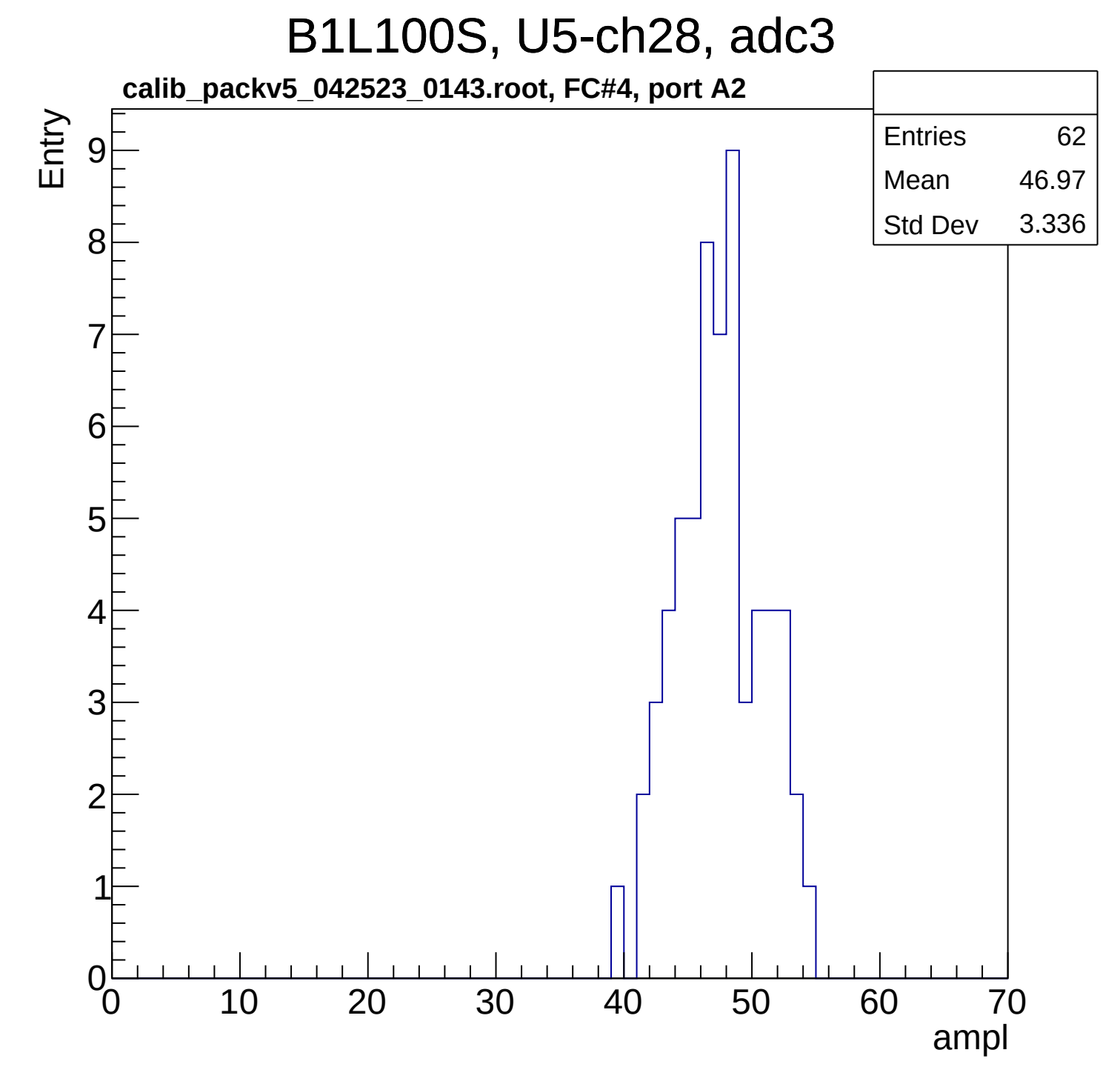
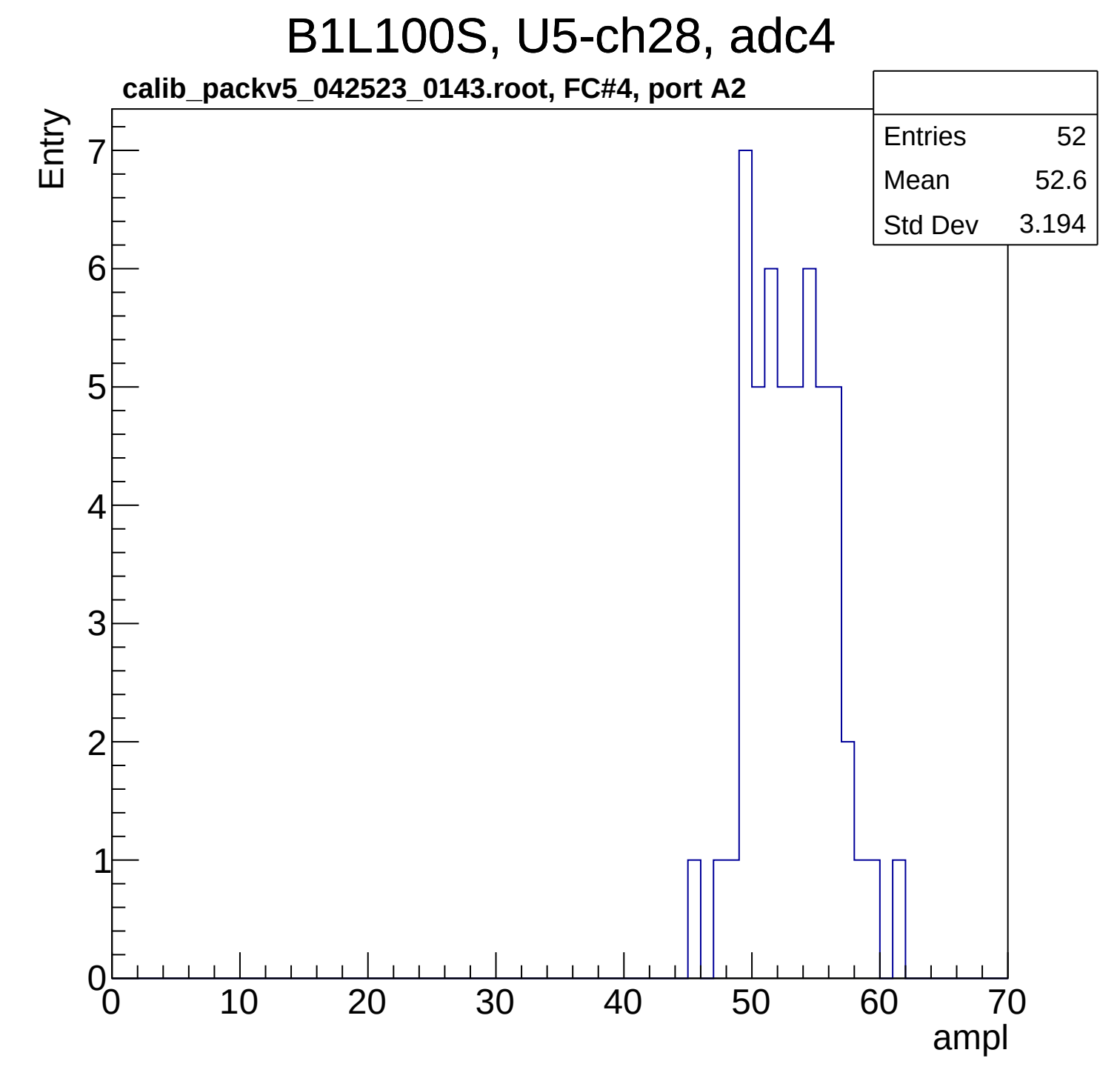
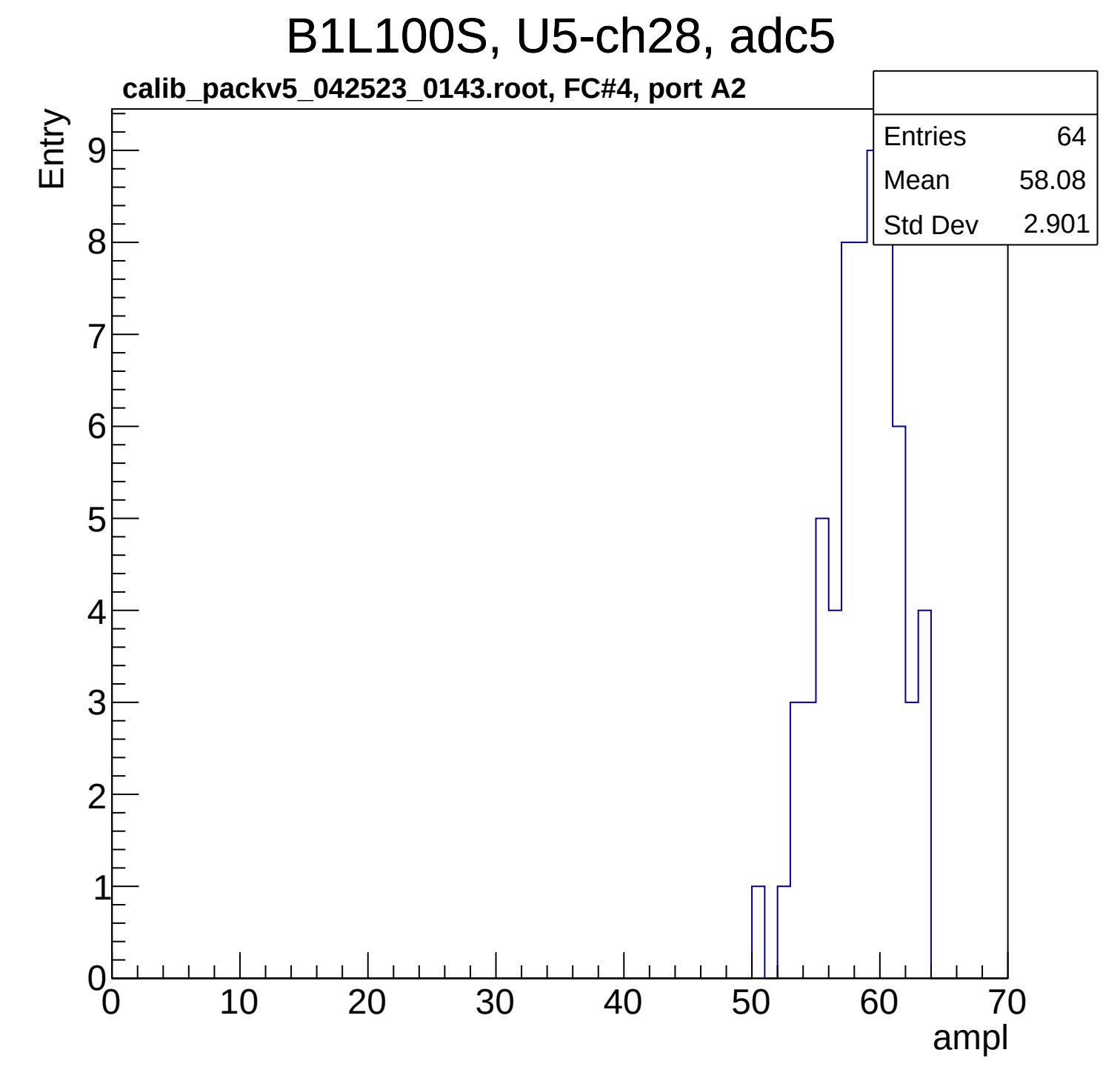

B1L100S, U5-ch28, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 81
Mean 34.44
Std Dev 3.461
Gaus mean : 35.0316
Gaus Width: 3.7432
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch28, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 52
Mean 41.25
Std Dev 3.031
Gaus mean : 42.0589
Gaus Width: 3.5648
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U5-ch28, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 46.97
Std Dev 3.336
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch28, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 52
Mean 52.6
Std Dev 3.194
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U5-ch28, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 58.08
Std Dev 2.901
Entry
ampl
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2
3
4
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6
7
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0
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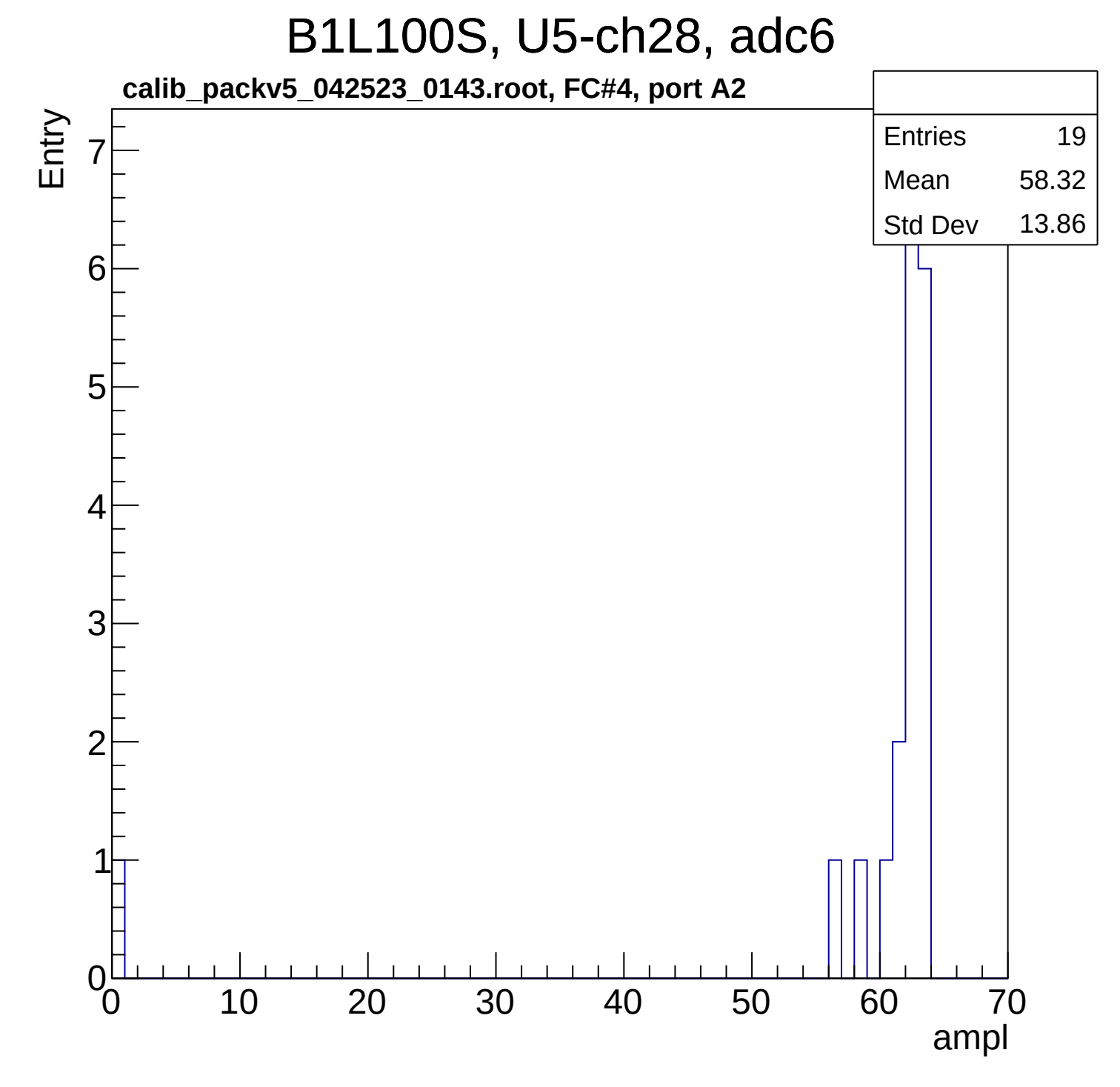
60
70


B1L100S, U5-ch28, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 19
Mean 58.32
Std Dev 13.86
Entry
ampl
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1
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4
5
6
7
0
10
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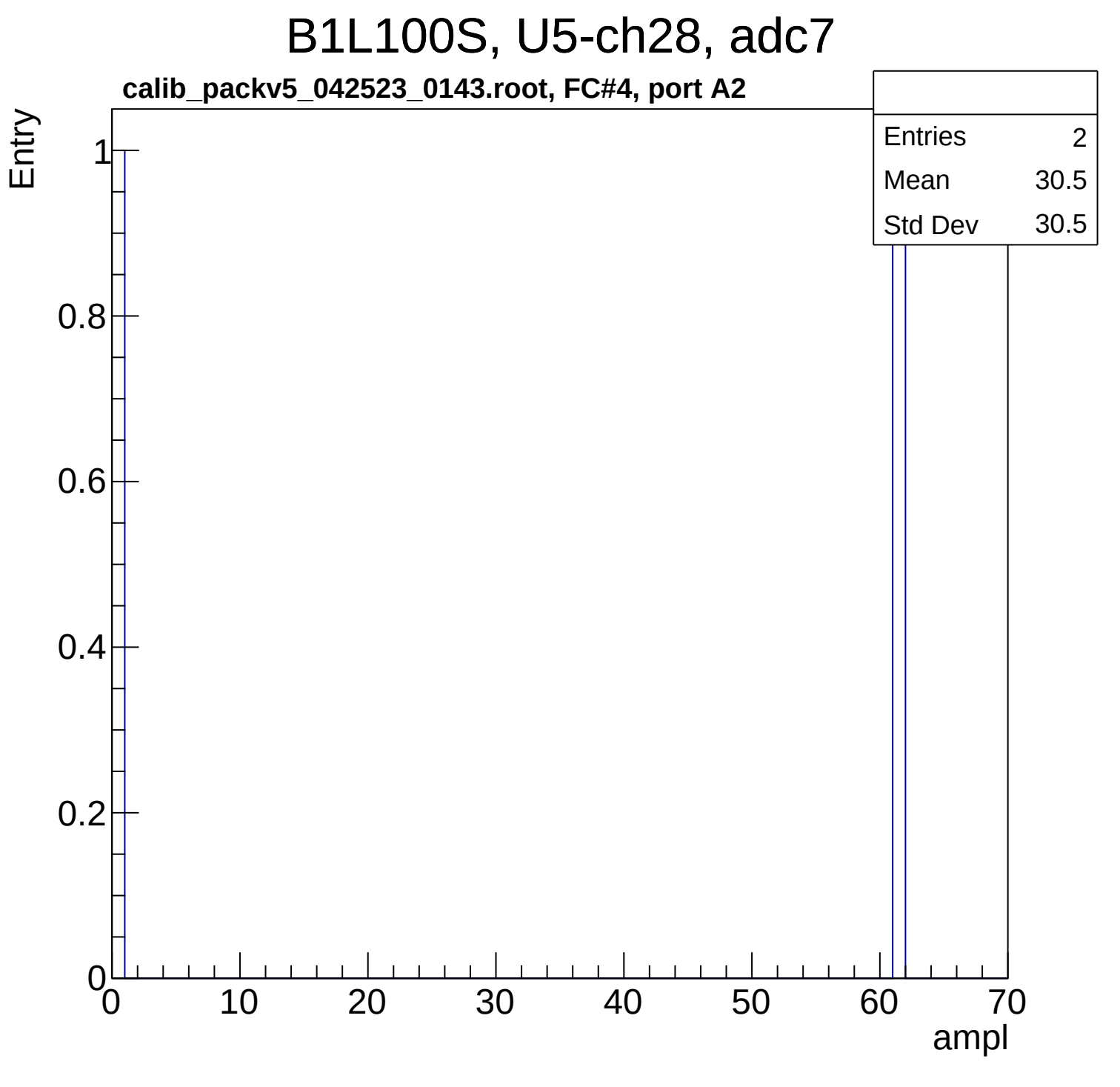
40
50
60
70


B1L100S, U5-ch28, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 30.5
Std Dev 30.5
Entry
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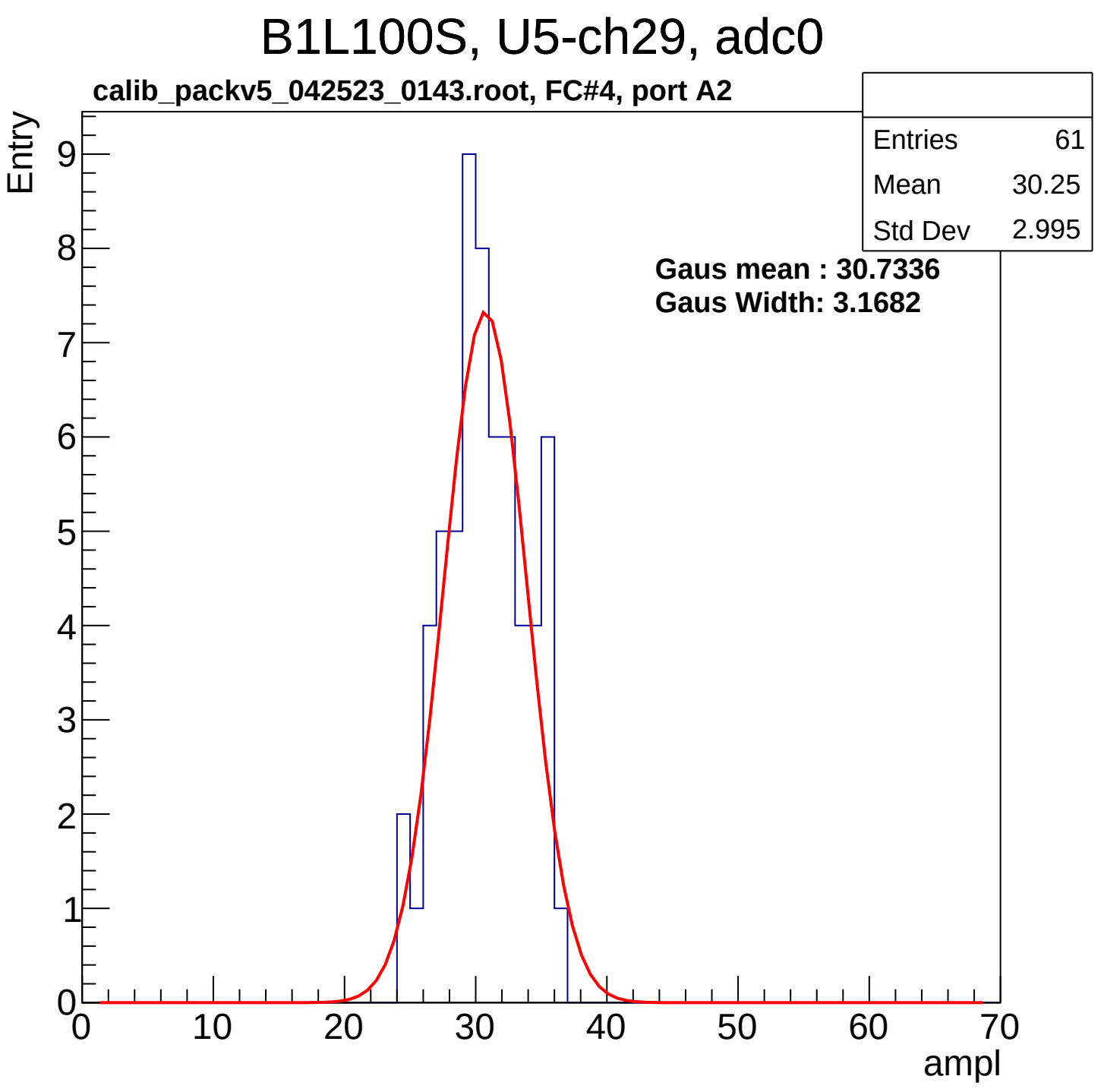
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch29, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 30.25
Std Dev 2.995
Gaus mean : 30.7336
Gaus Width: 3.1682
Entry
ampl
0
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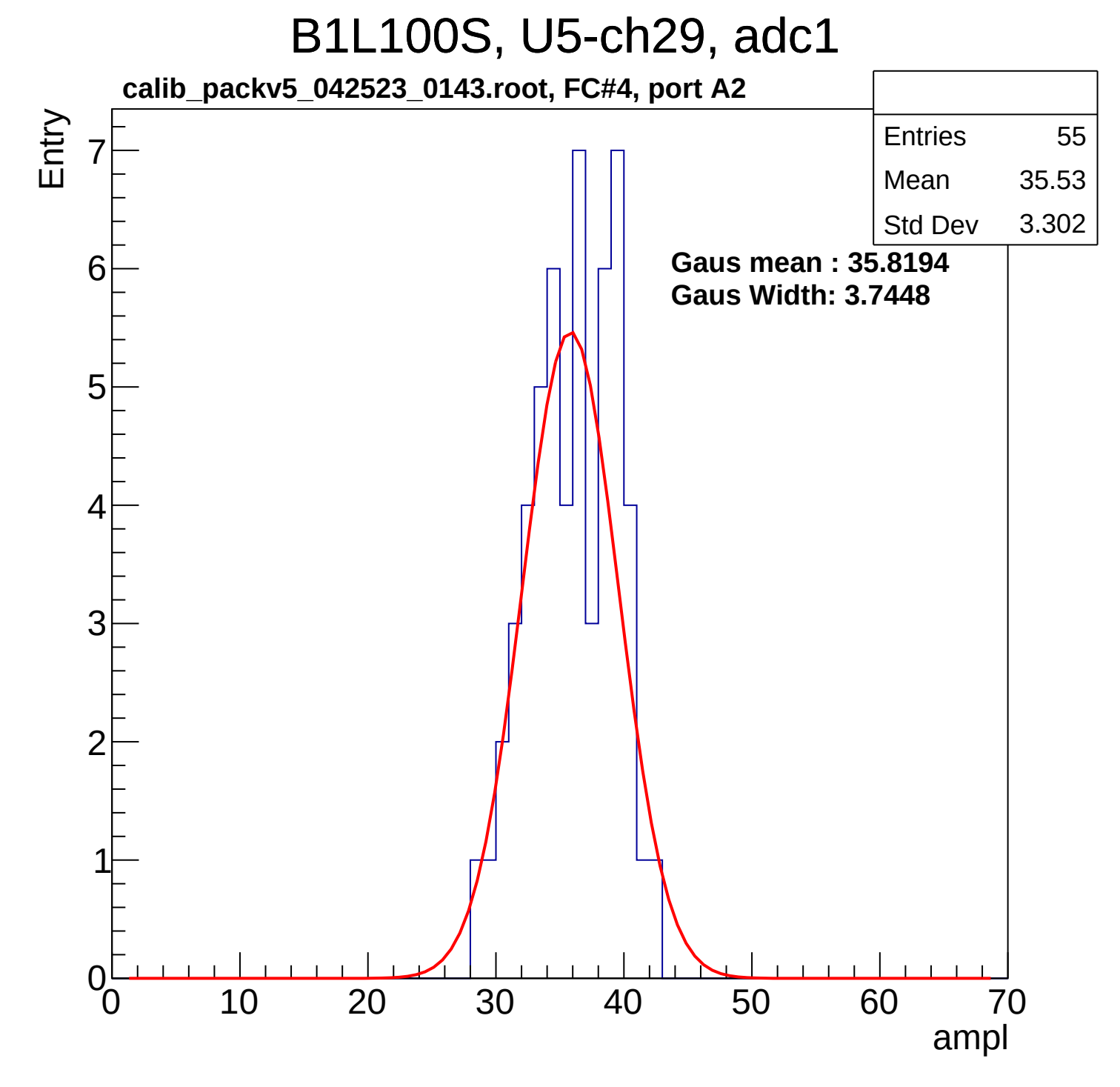
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch29, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 35.53
Std Dev 3.302
Gaus mean : 35.8194
Gaus Width: 3.7448
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
30
40
50
60
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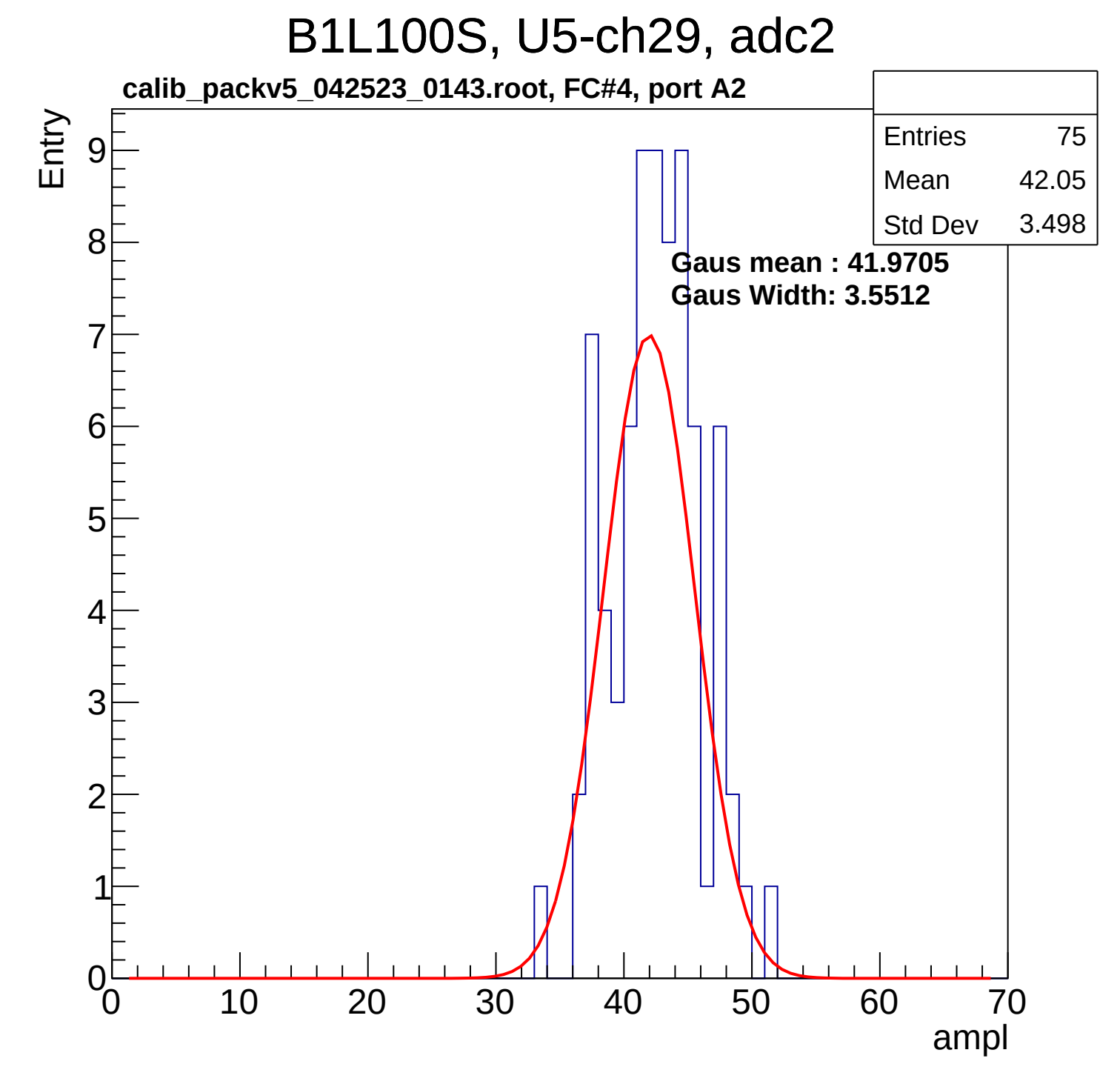
B1L100S, U5-ch29, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 75
Mean 42.05
Std Dev 3.498
Gaus mean : 41.9705
Gaus Width: 3.5512
Entry
ampl
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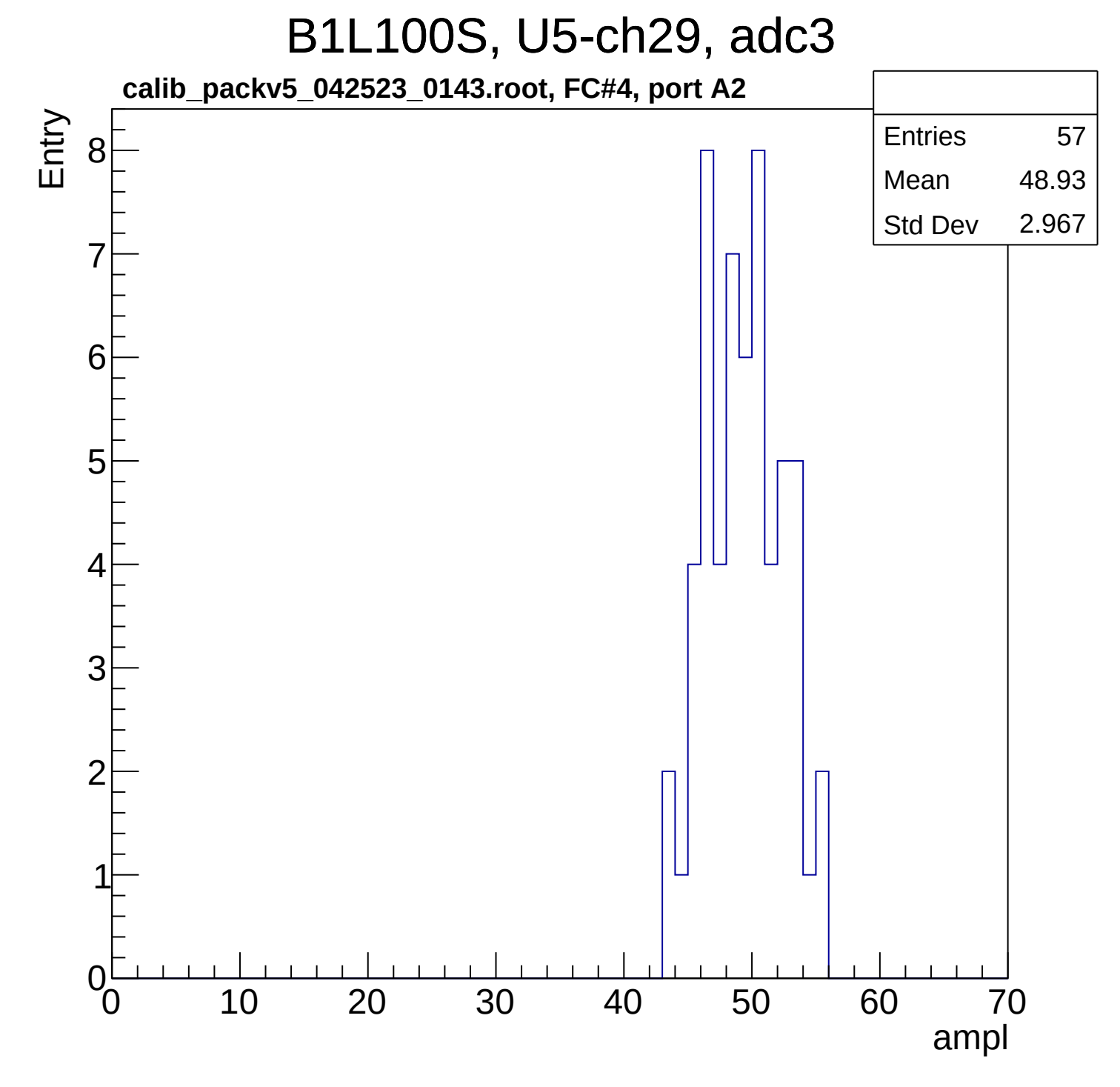
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch29, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 48.93
Std Dev 2.967
Entry
ampl
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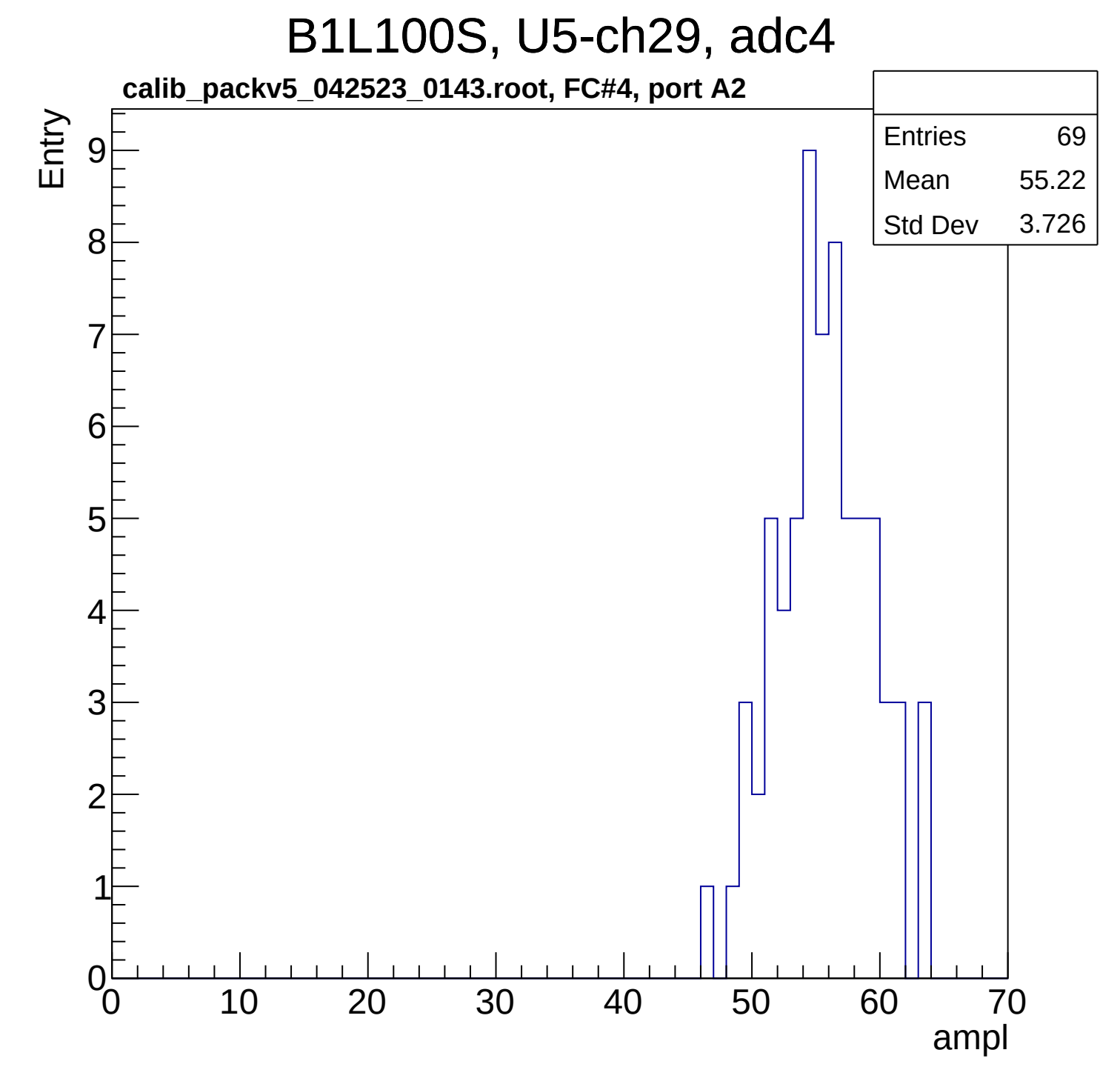
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch29, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 55.22
Std Dev 3.726
Entry
ampl
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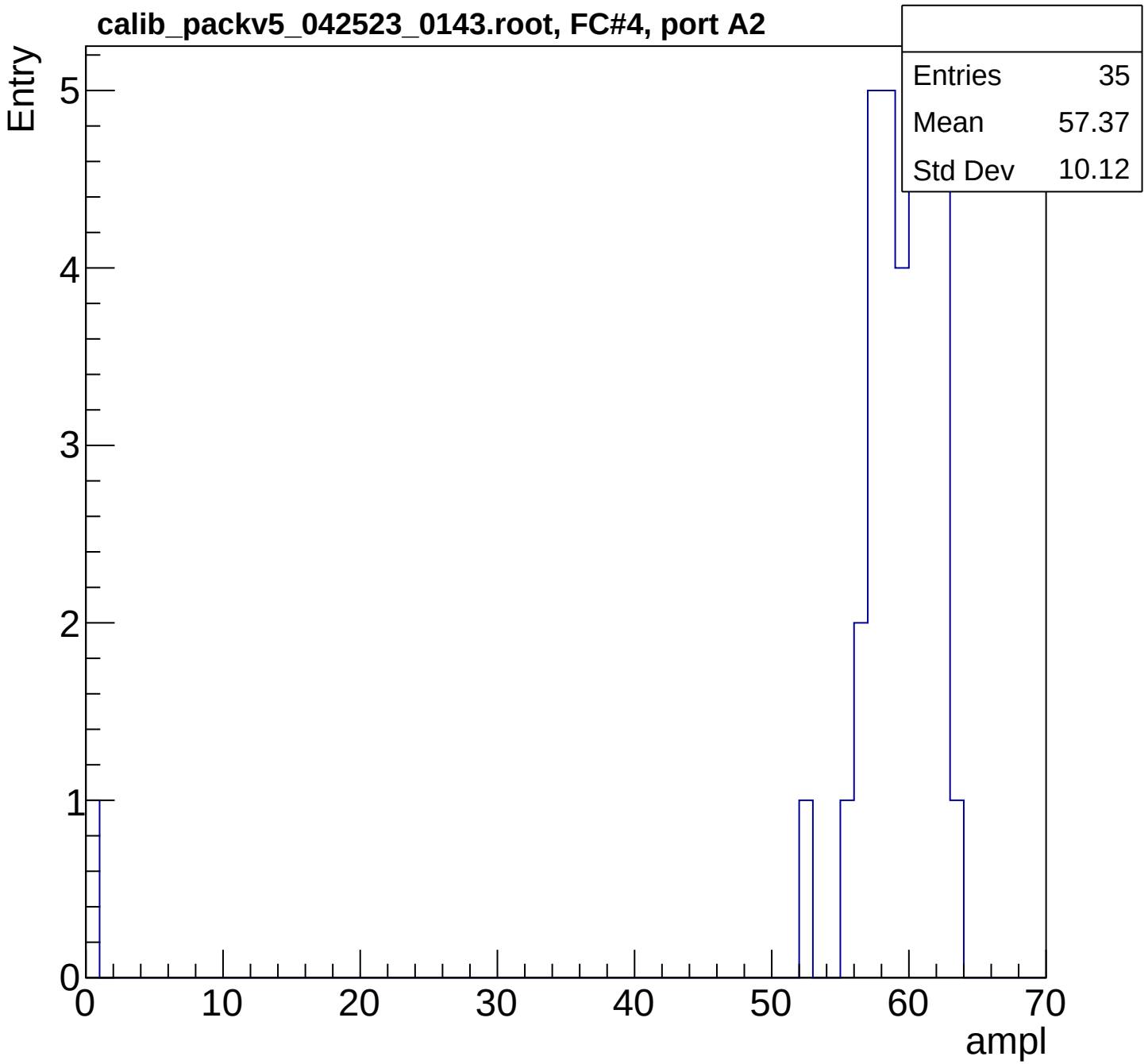
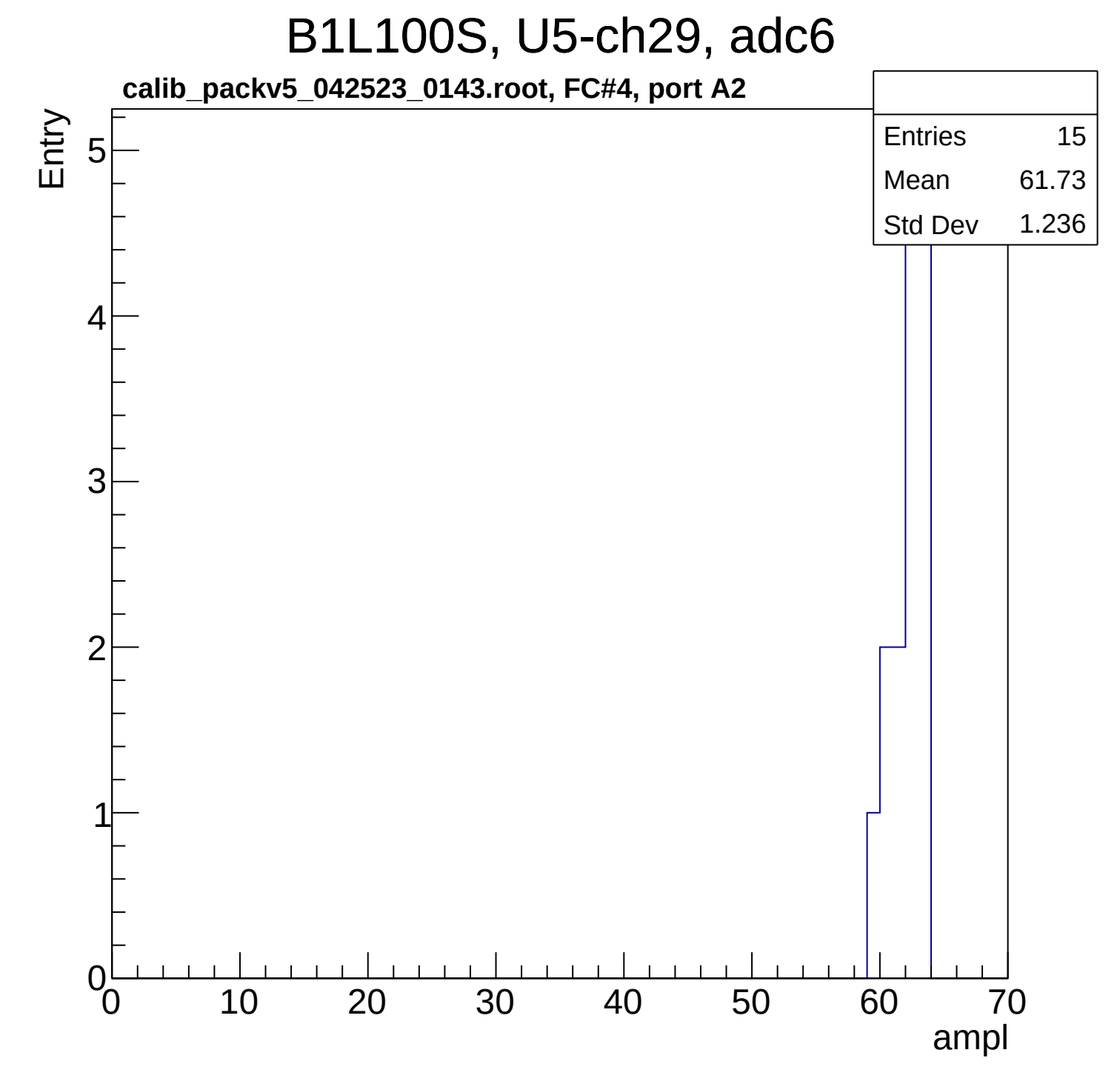
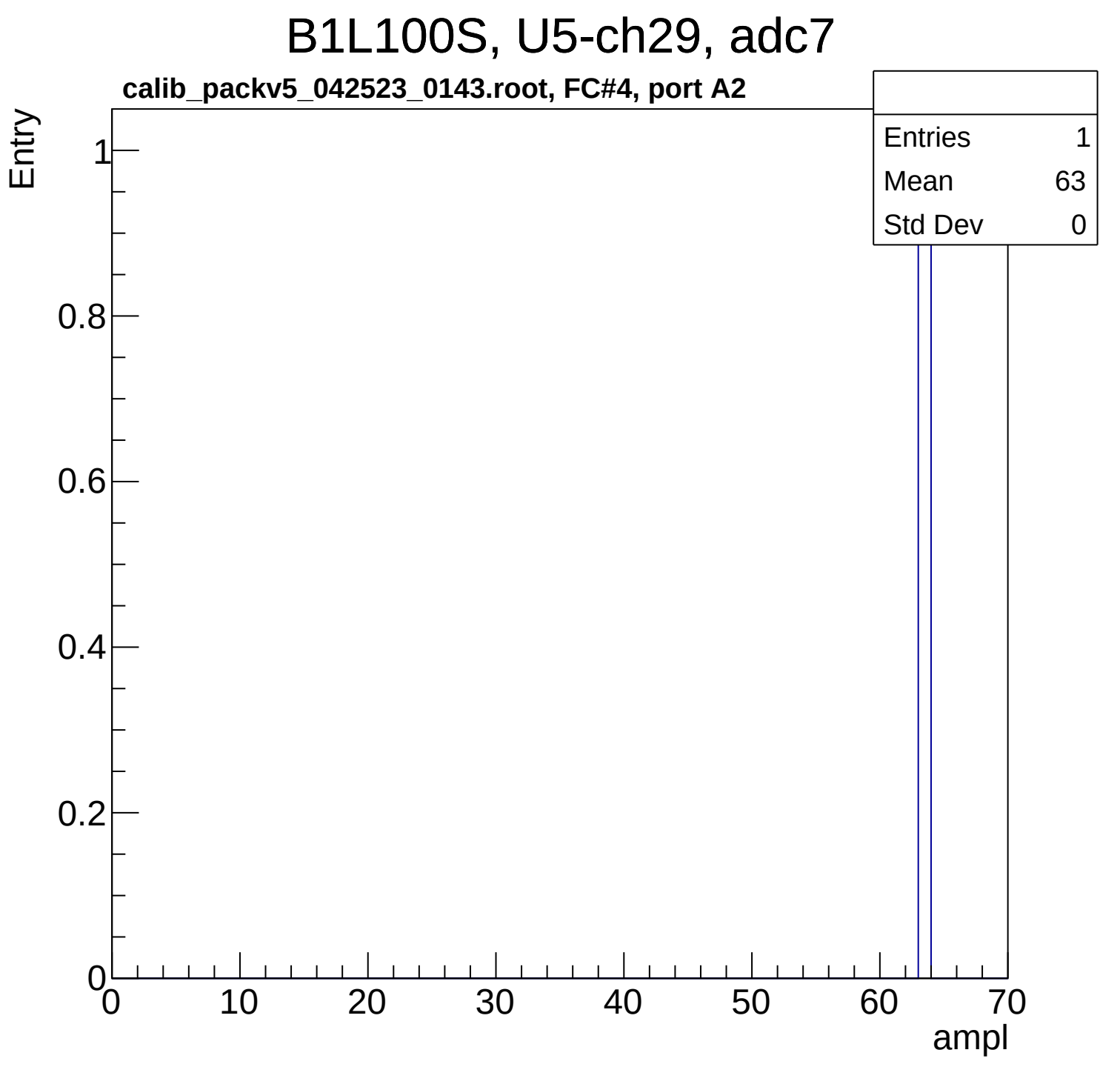
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch29, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 35
Mean 57.37
Std Dev 10.12
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch29, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 15
Mean 61.73
Std Dev 1.236
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch29, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 63
Std Dev 0
Entry
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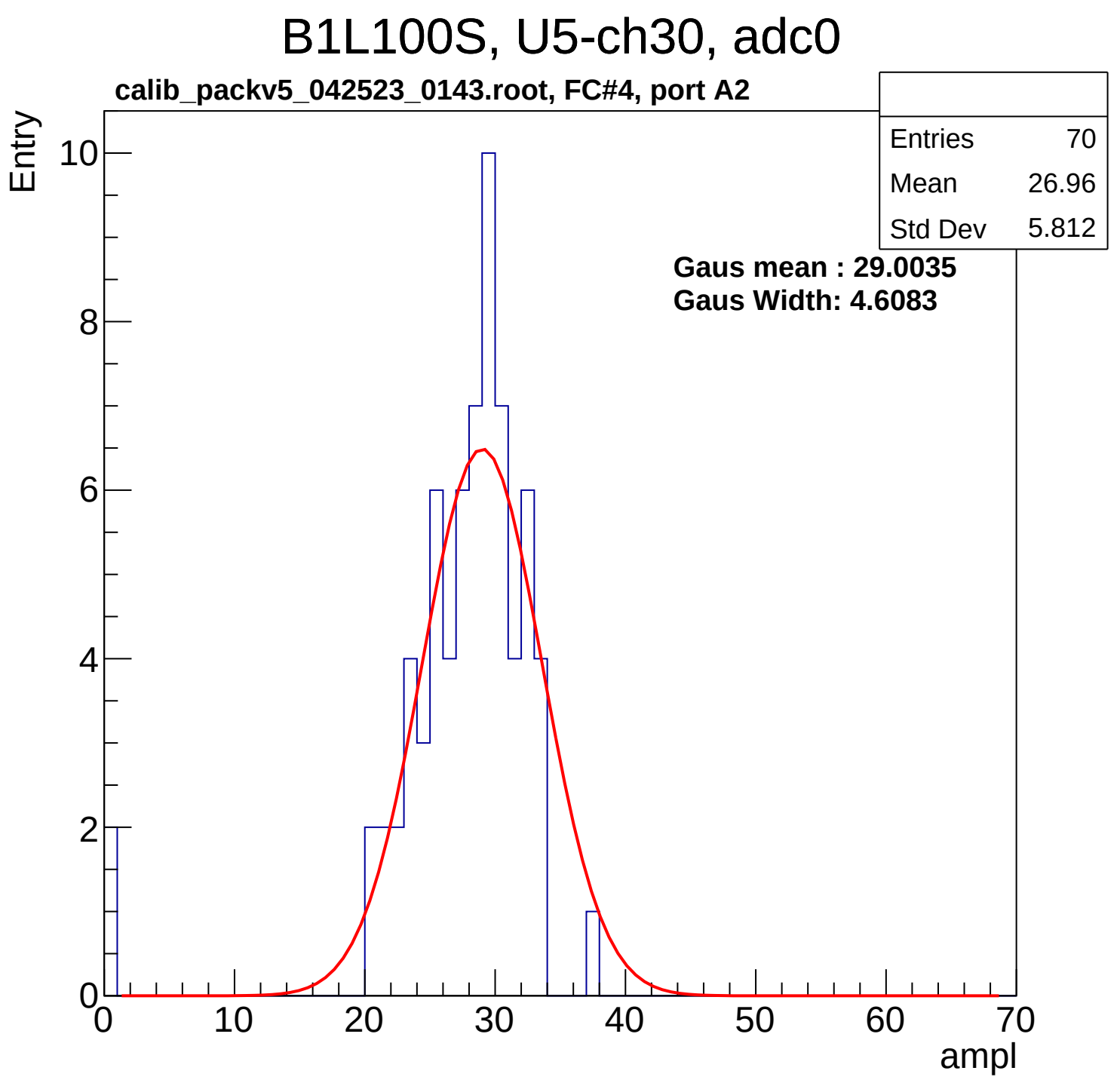
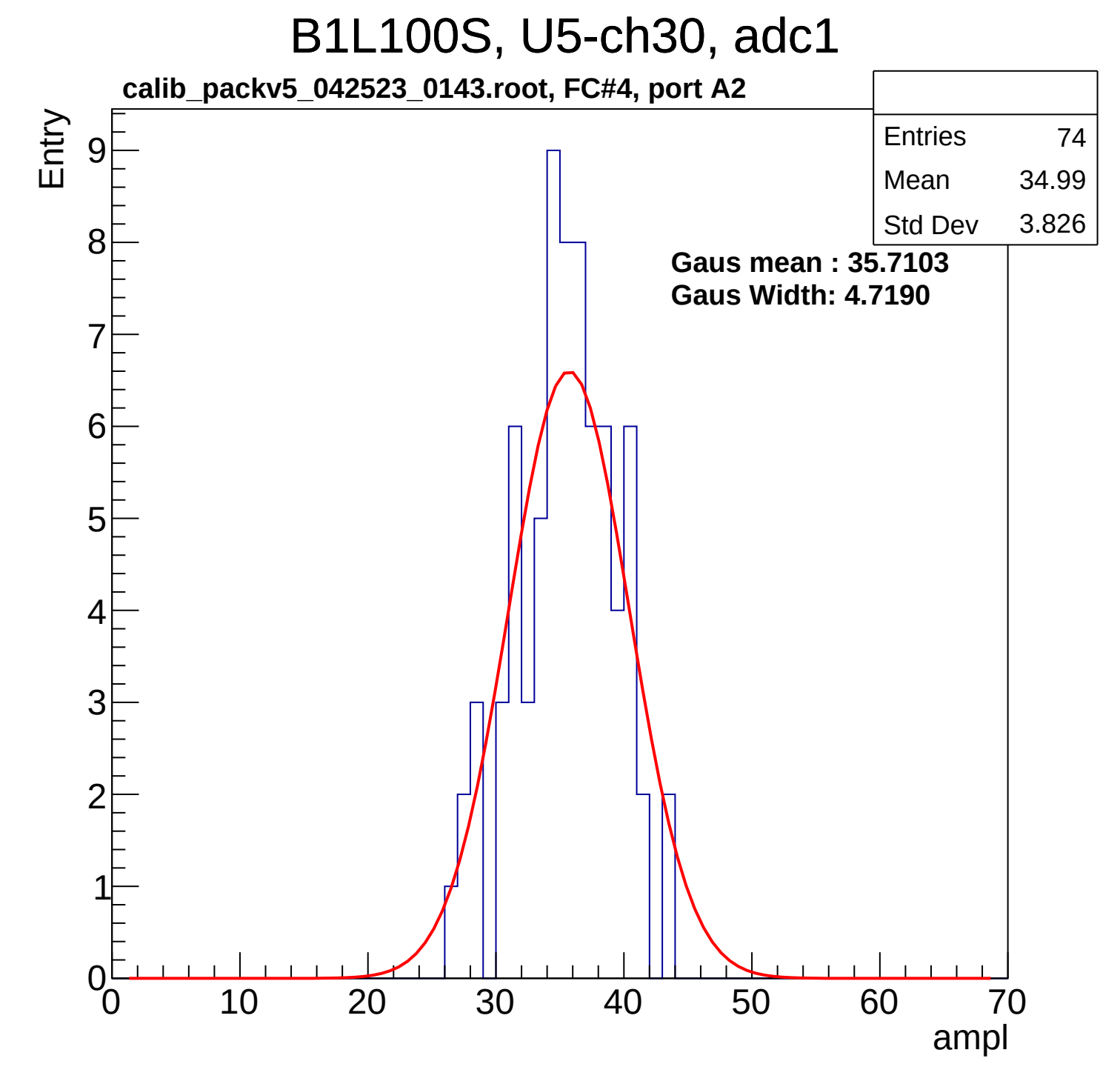
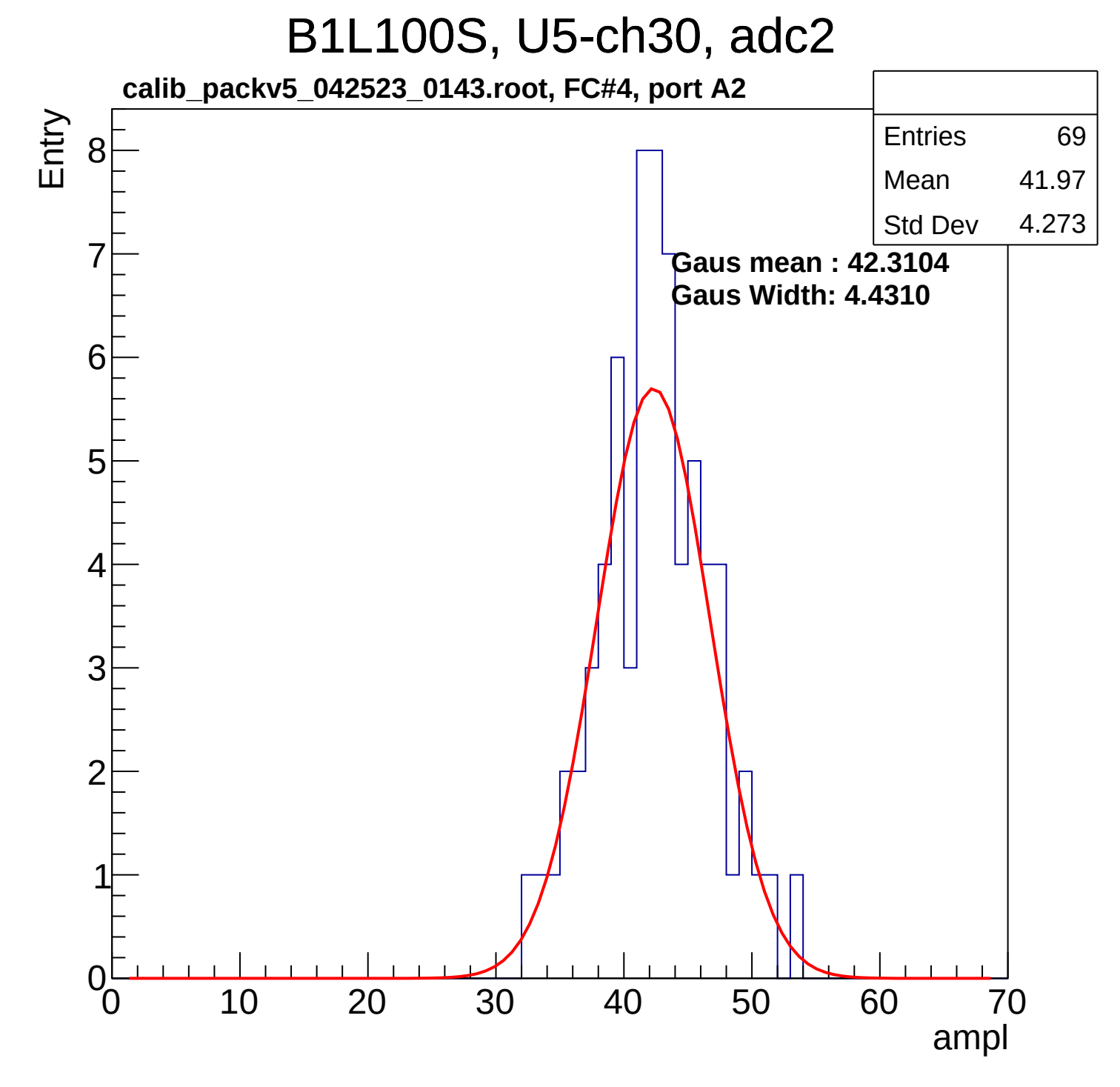
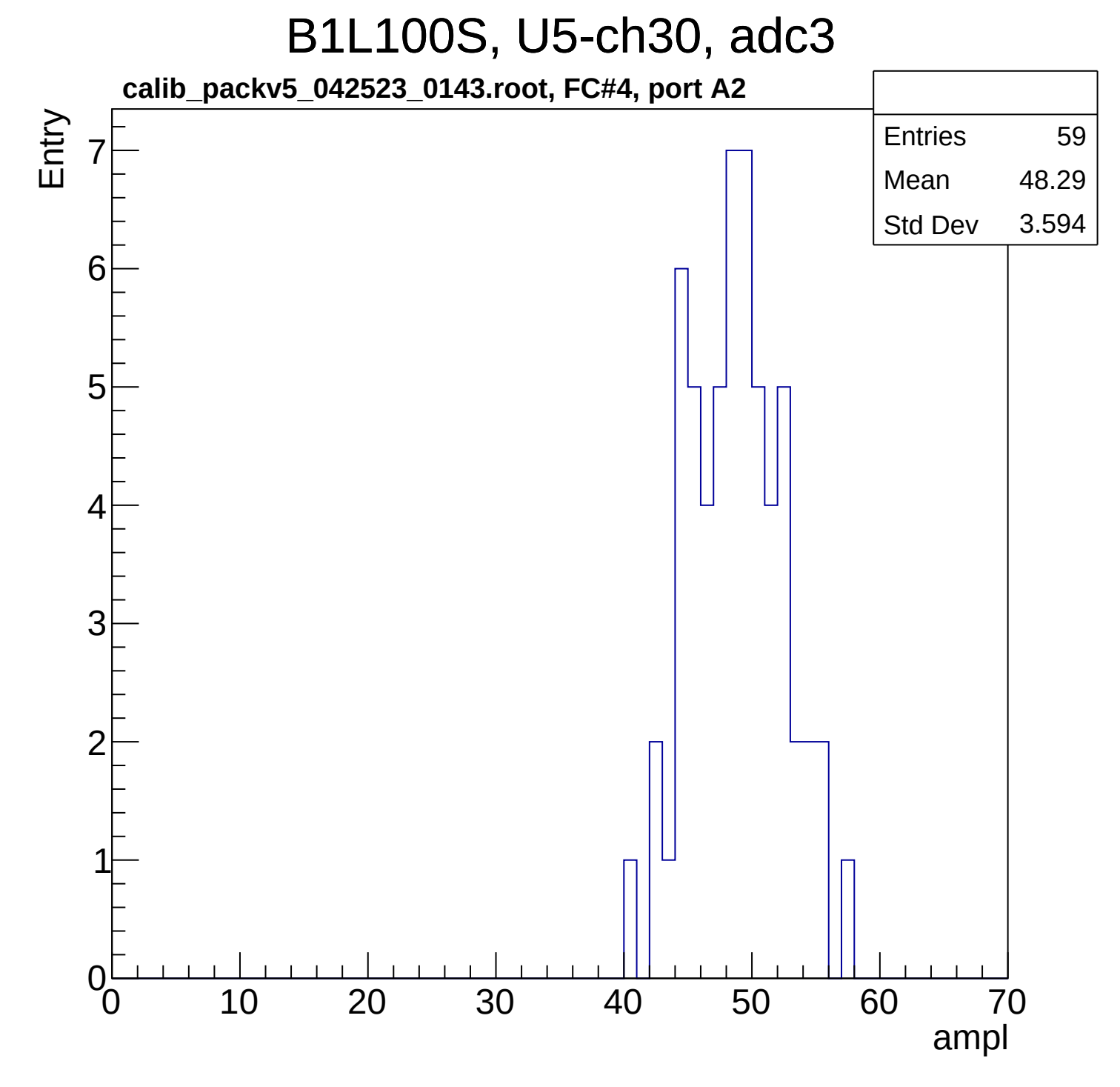
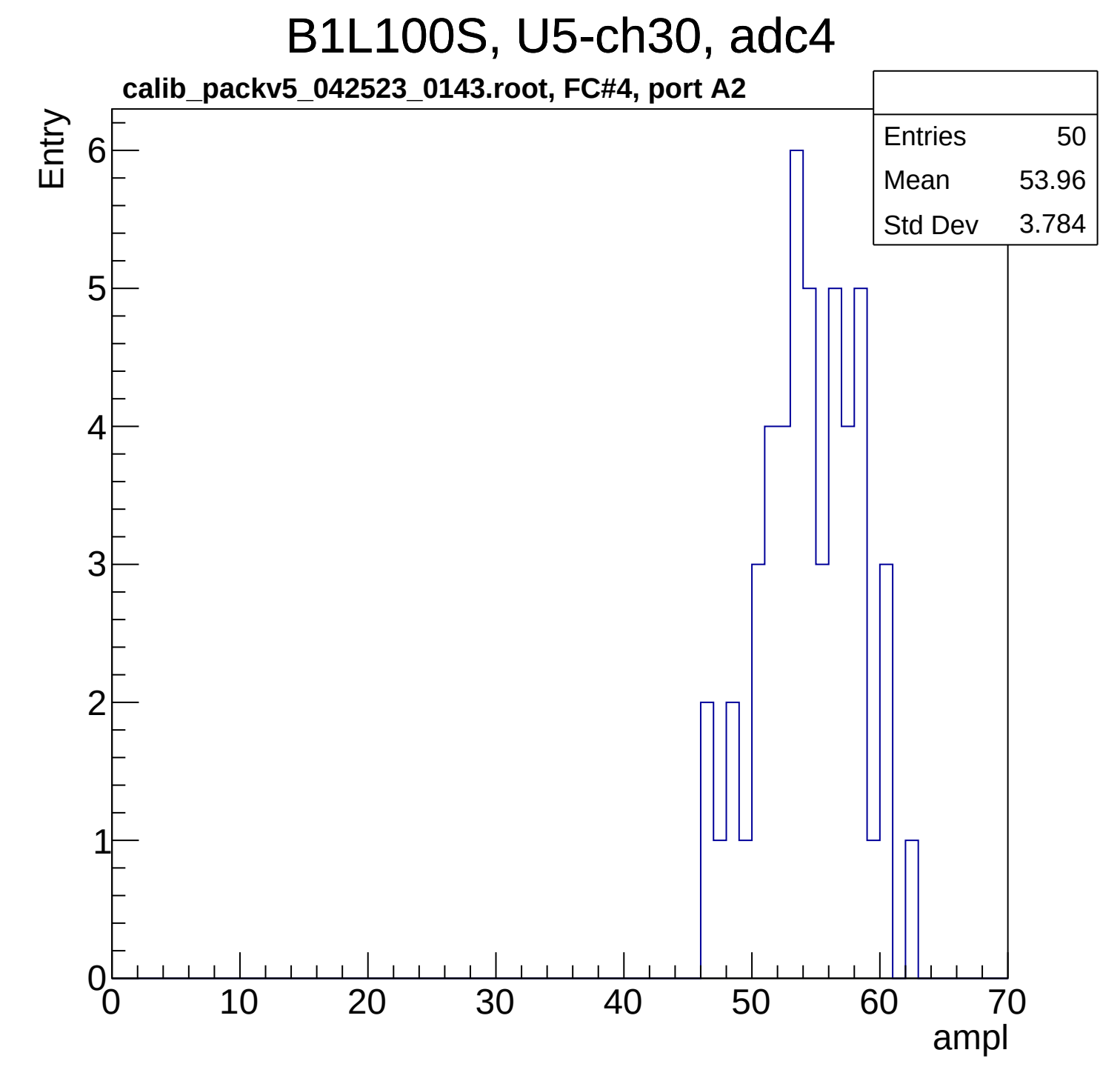
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

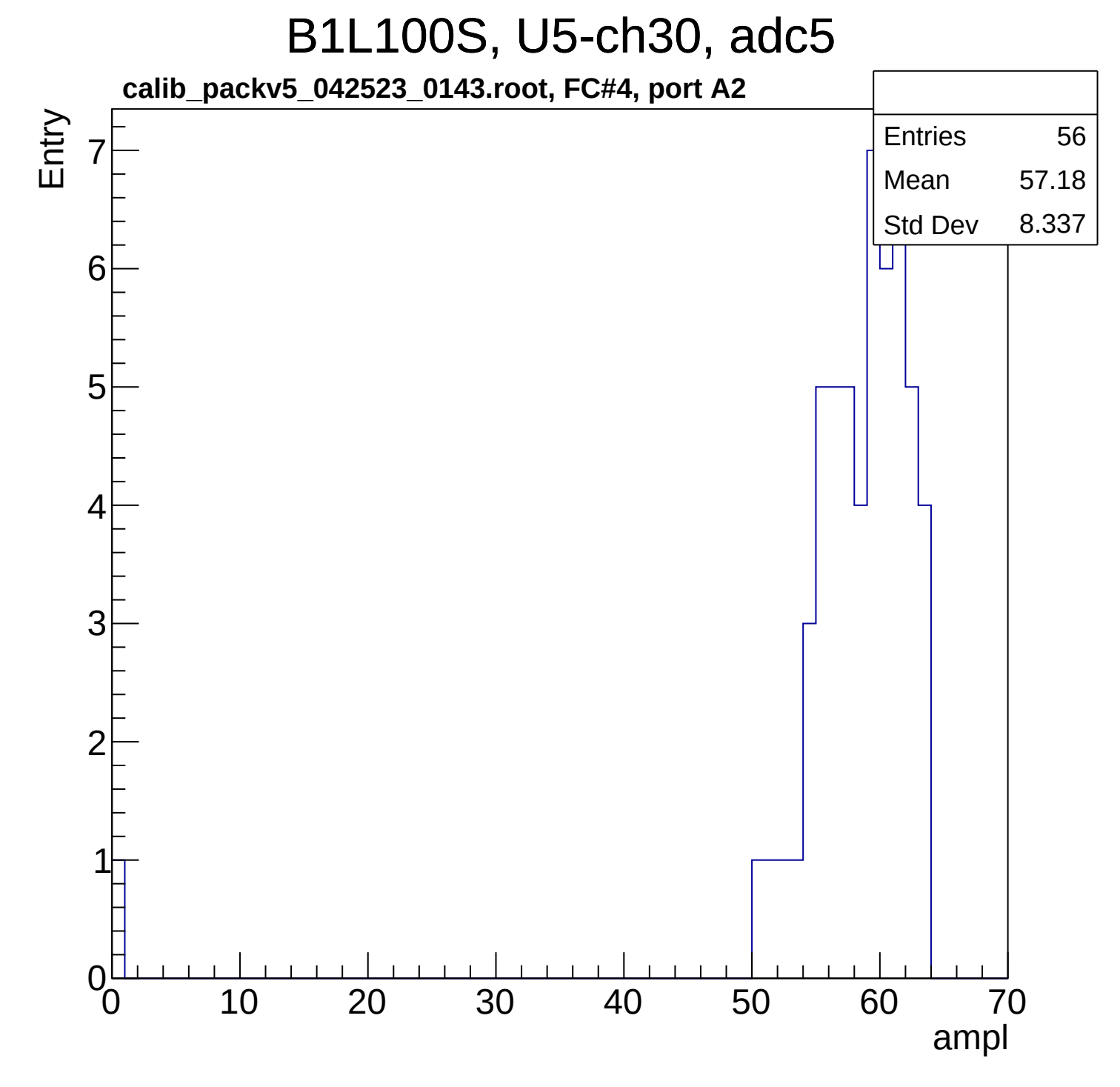

B1L100S, U5-ch30, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 26.96
Std Dev 5.812
Gaus mean : 29.0035
Gaus Width: 4.6083
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

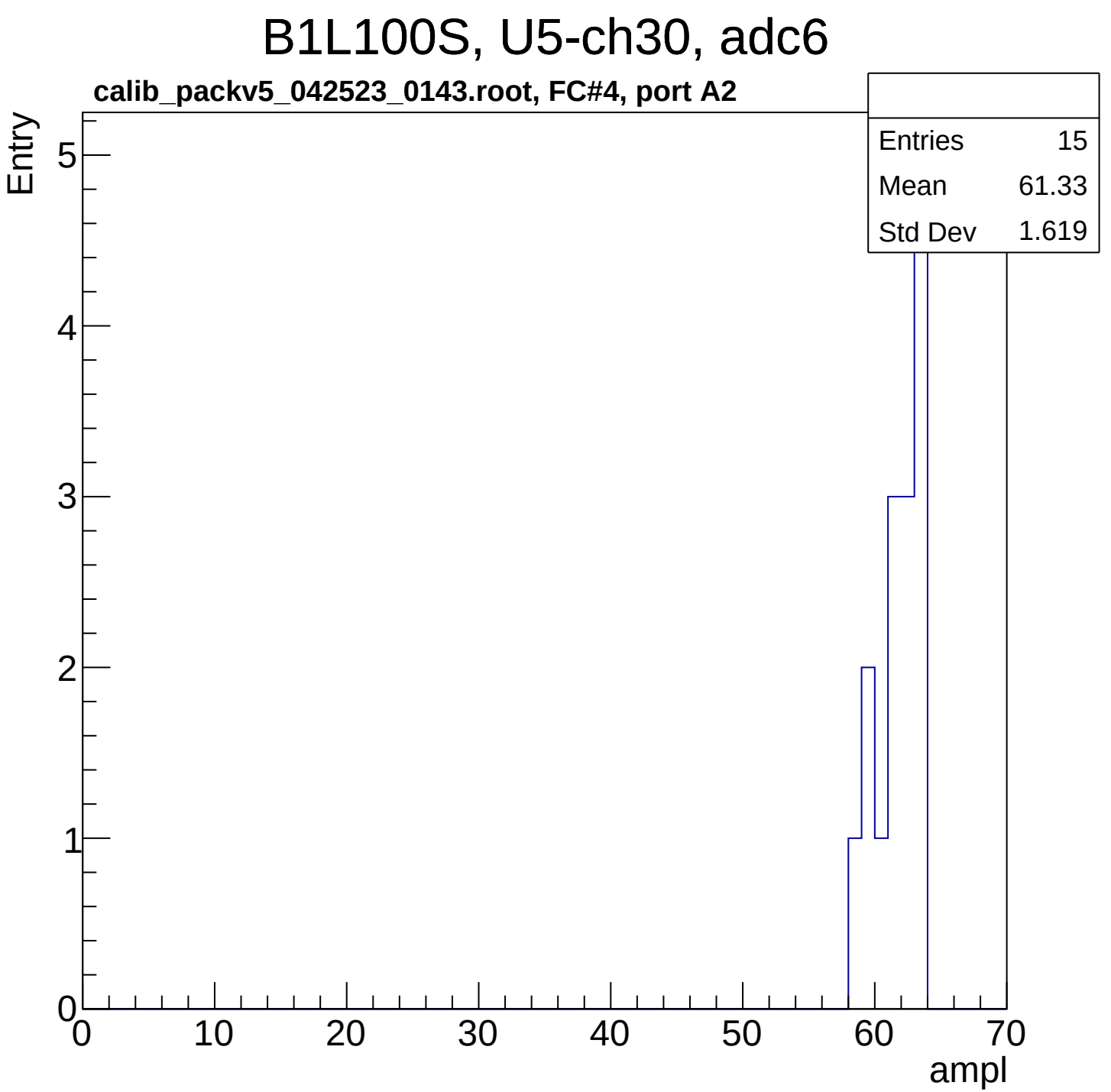

B1L100S, U5-ch30, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 74
Mean 34.99
Std Dev 3.826
Gaus mean : 35.7103
Gaus Width: 4.7190
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

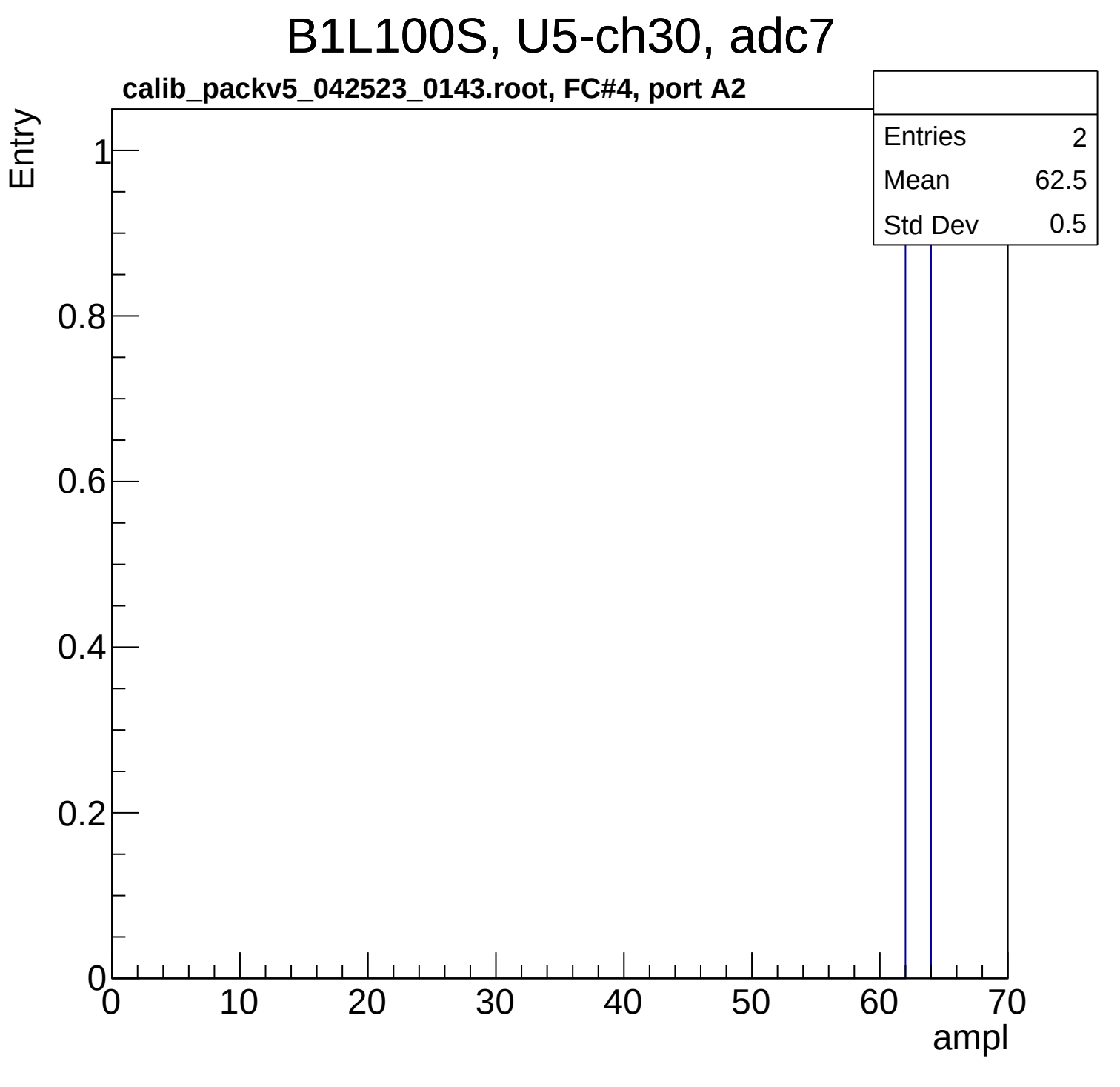

B1L100S, U5-ch30, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 41.97
Std Dev 4.273
Gaus mean : 42.3104
Gaus Width: 4.4310
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

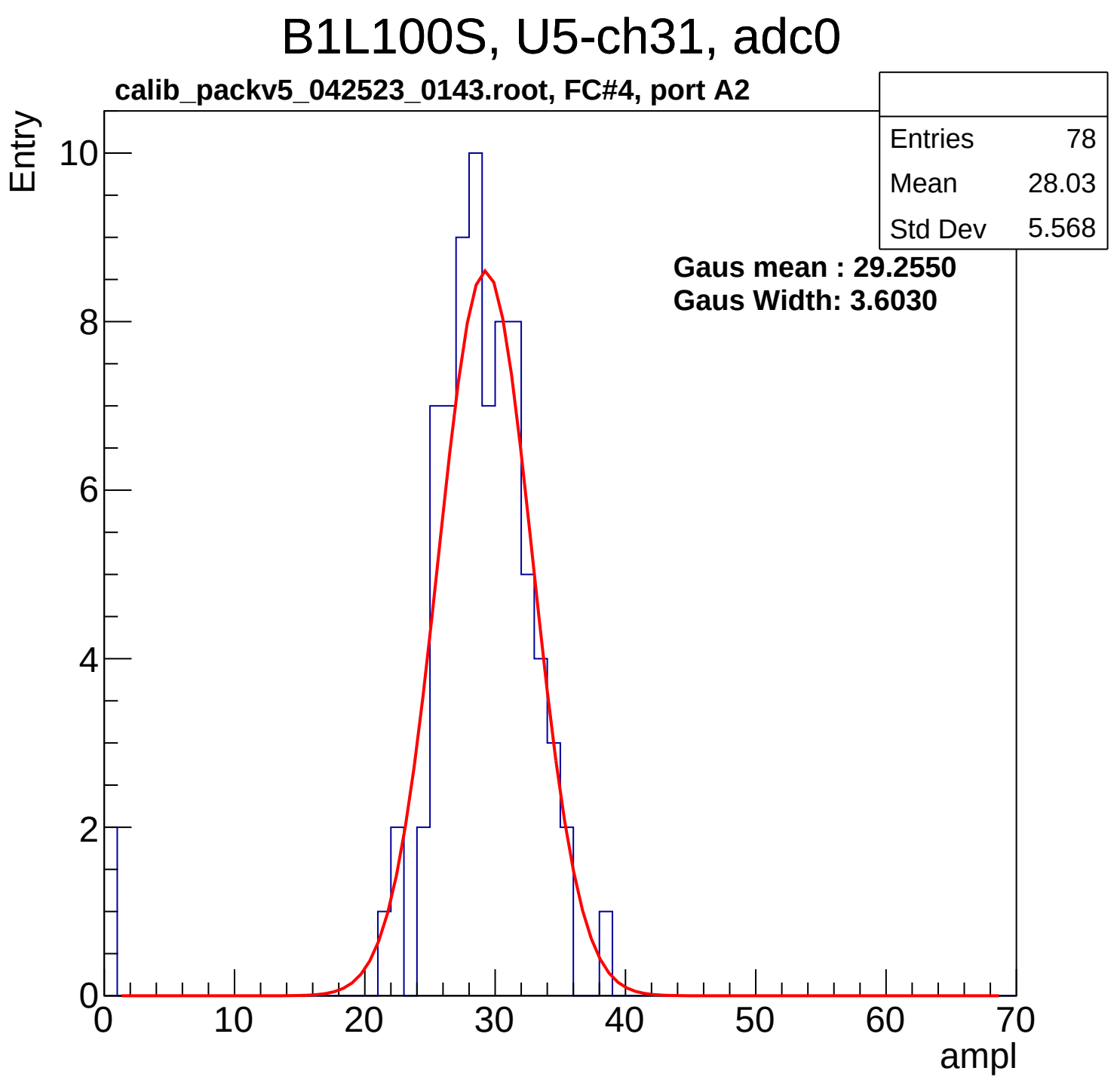

B1L100S, U5-ch30, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 48.29
Std Dev 3.594
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

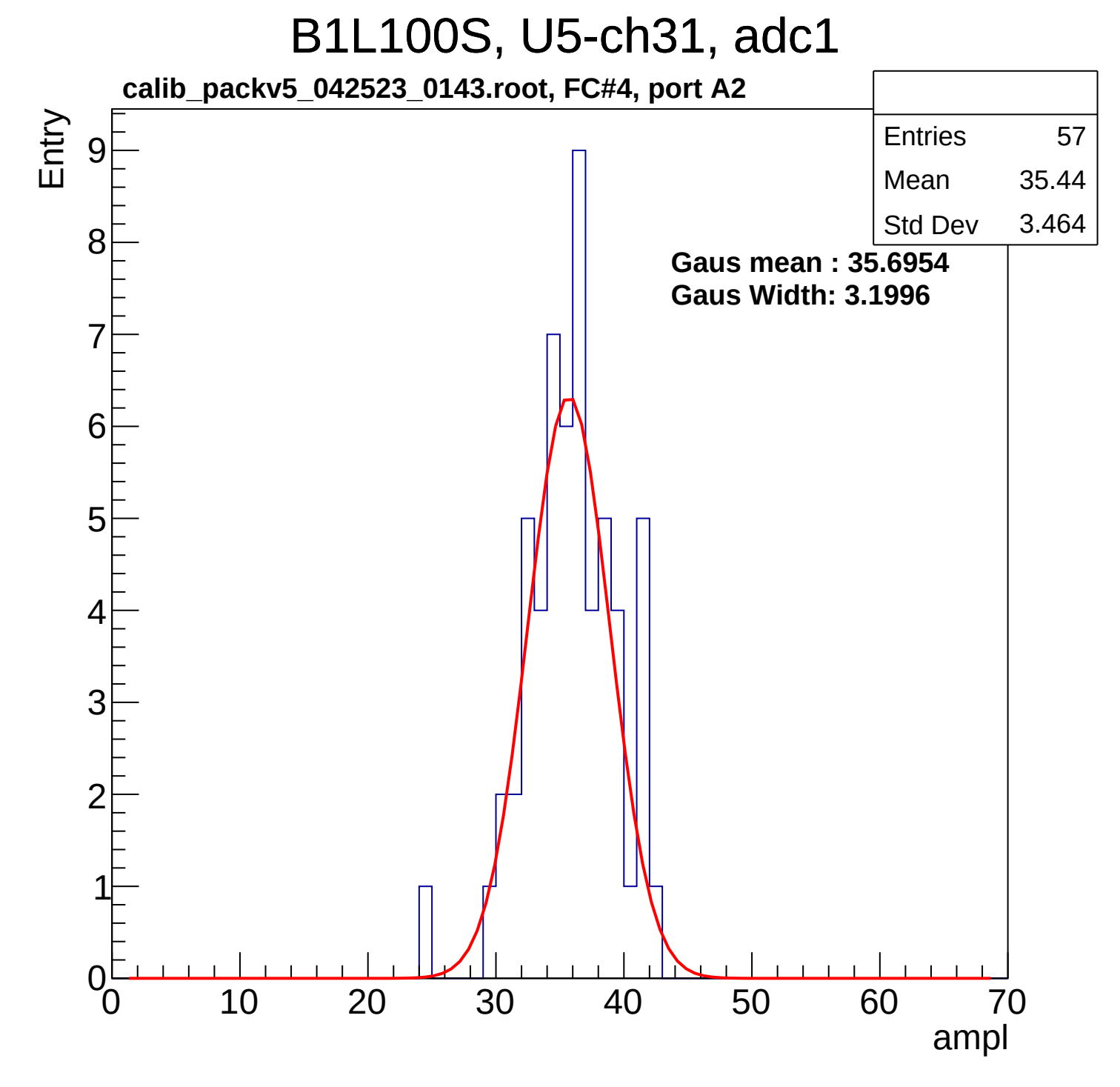

B1L100S, U5-ch30, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 53.96
Std Dev 3.784
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

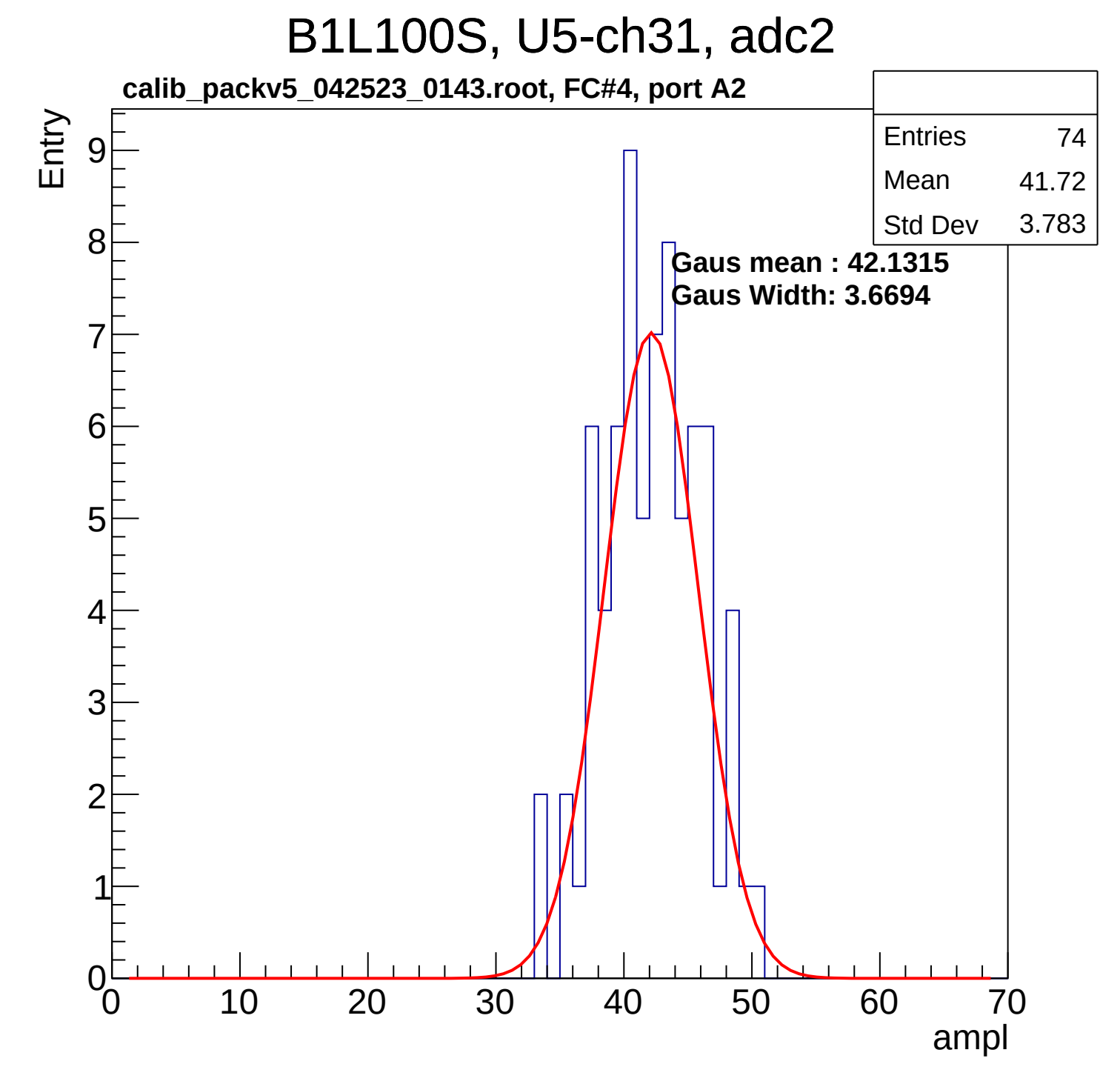

B1L100S, U5-ch30, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 57.18
Std Dev 8.337
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

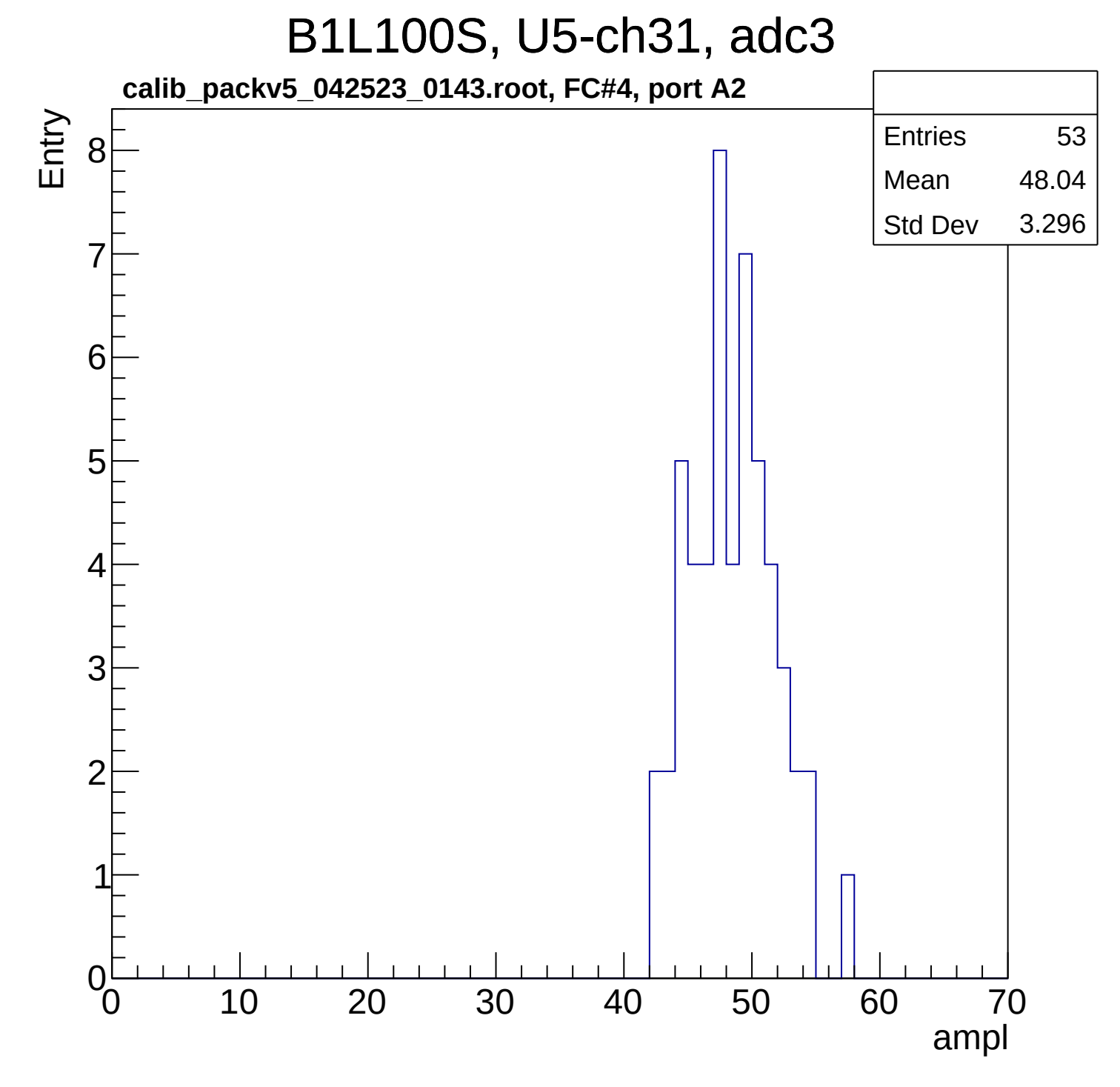

B1L100S, U5-ch30, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 15
Mean 61.33
Std Dev 1.619
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

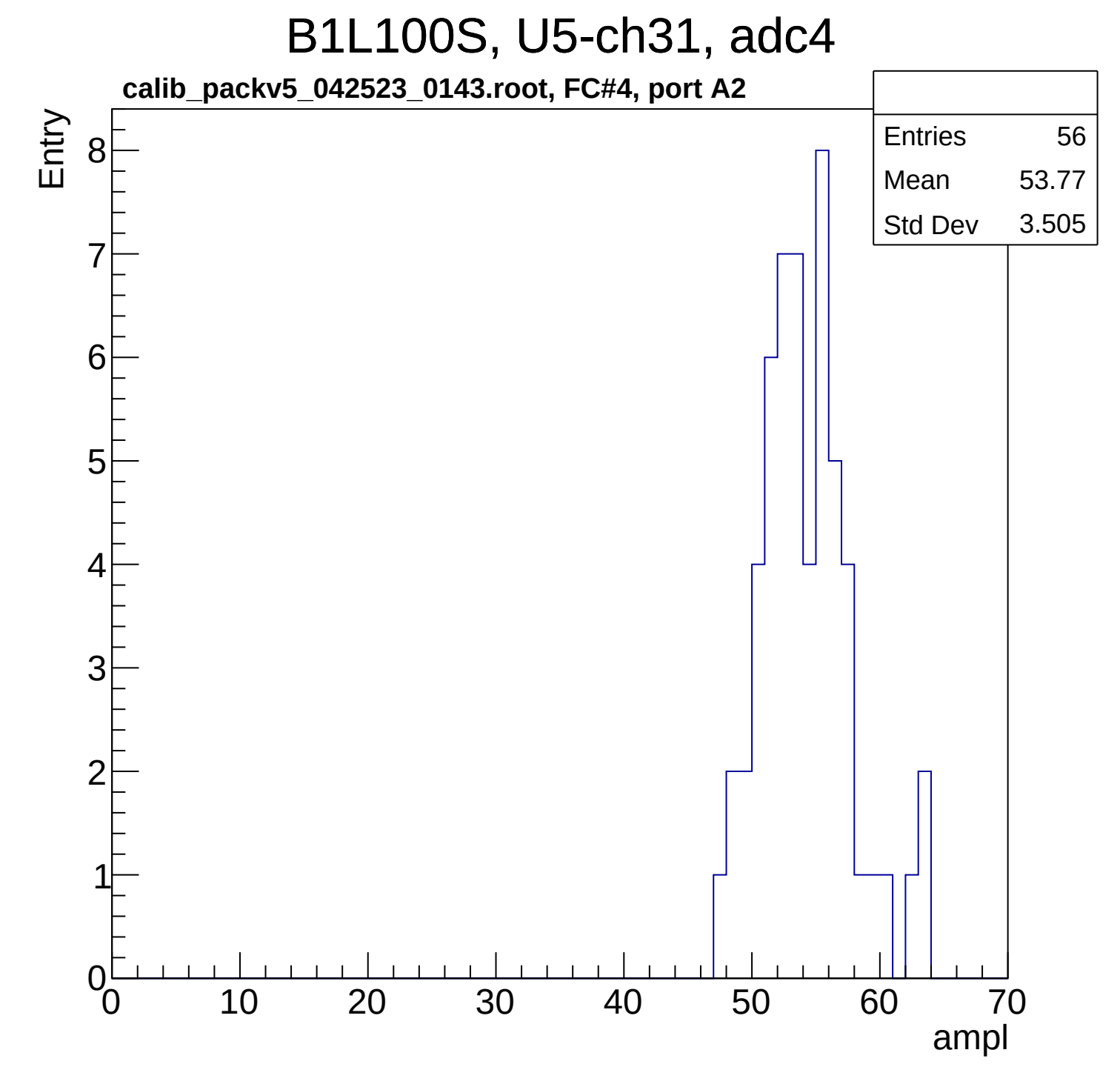

B1L100S, U5-ch30, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

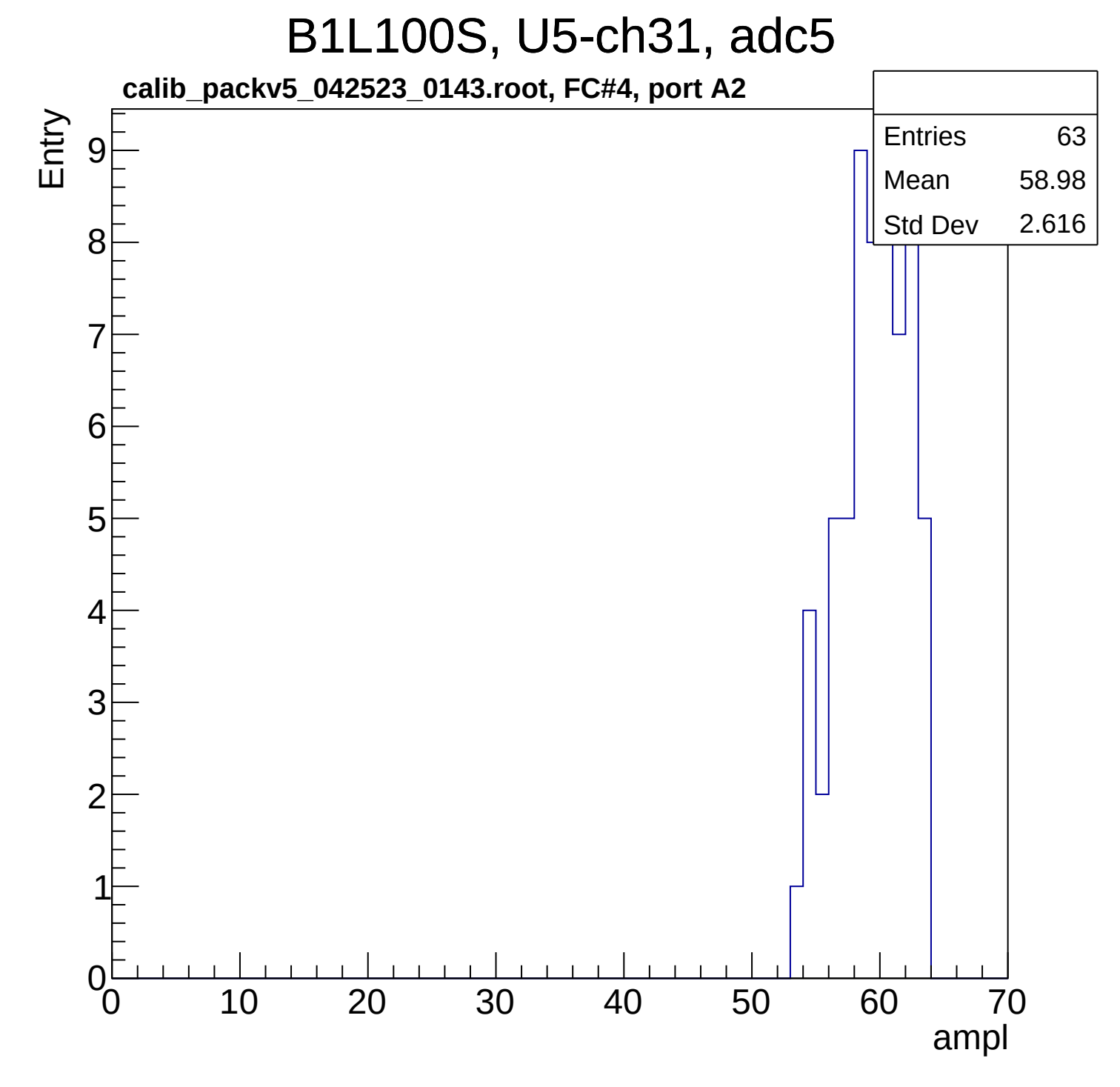

B1L100S, U5-ch31, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 78
Mean 28.03
Std Dev 5.568
Gaus mean : 29.2550
Gaus Width: 3.6030
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

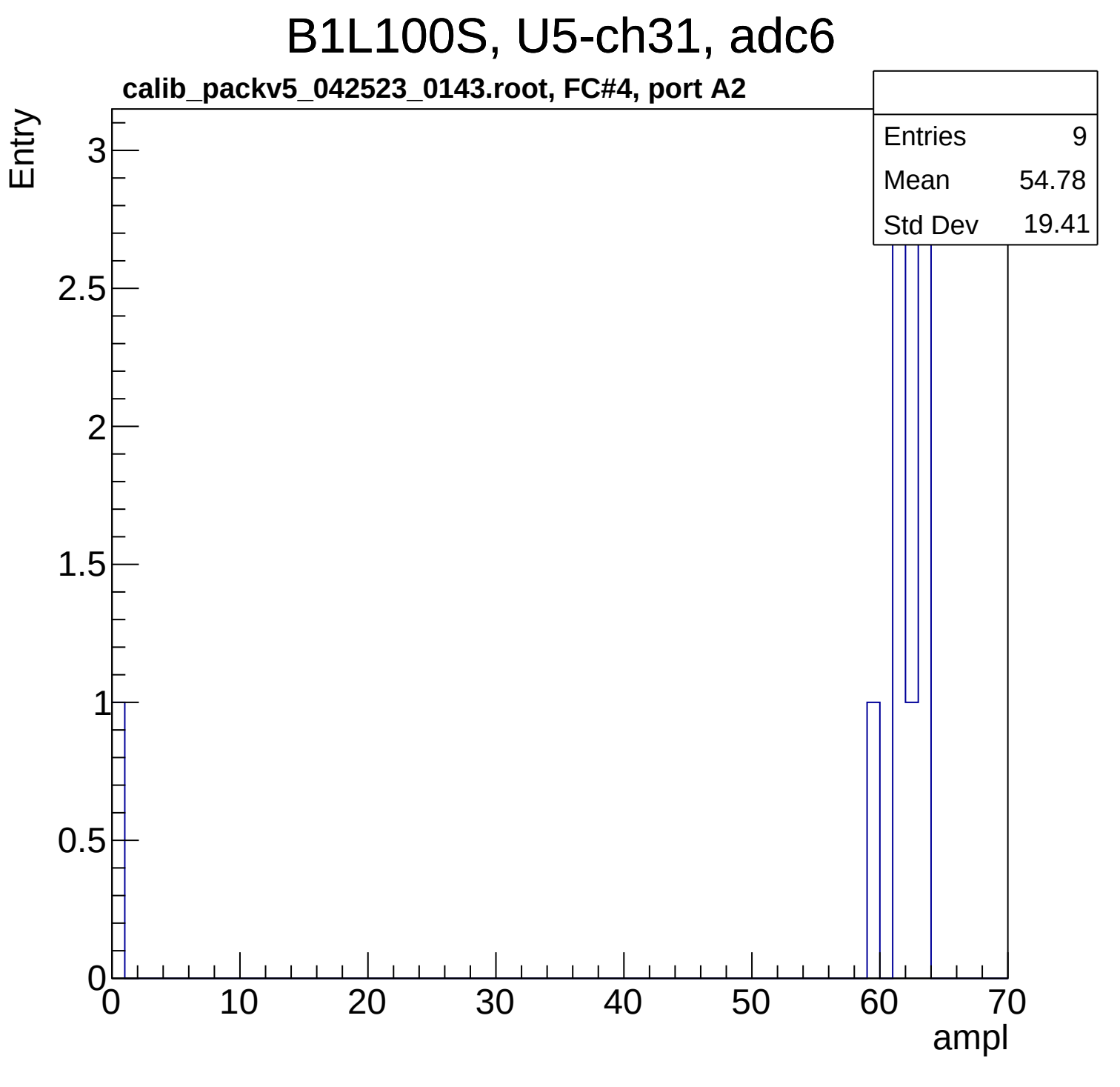

B1L100S, U5-ch31, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 35.44
Std Dev 3.464
Gaus mean : 35.6954
Gaus Width: 3.1996
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9

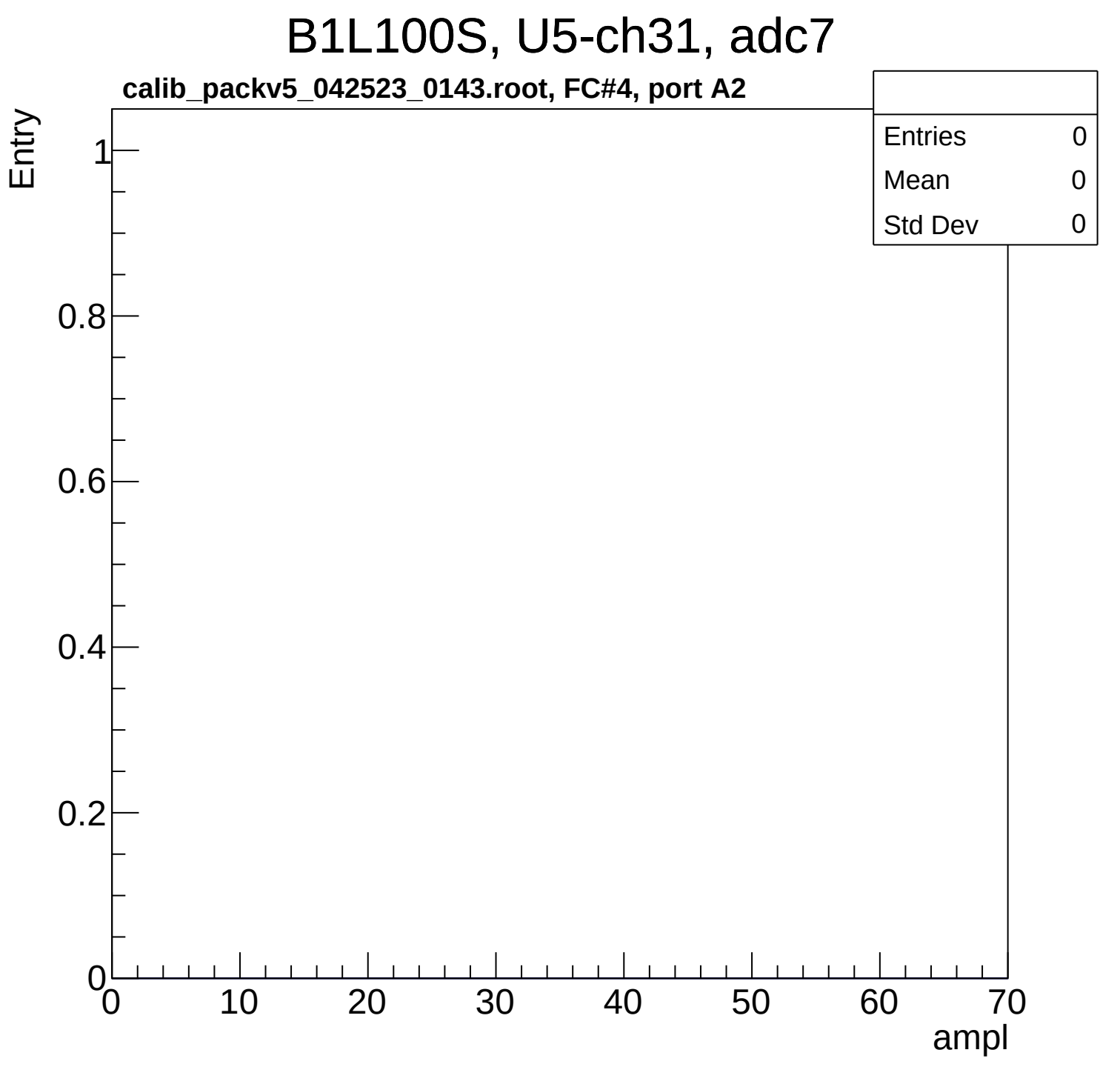

B1L100S, U5-ch31, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 74
Mean 41.72
Std Dev 3.783
Gaus mean : 42.1315
Gaus Width: 3.6694
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

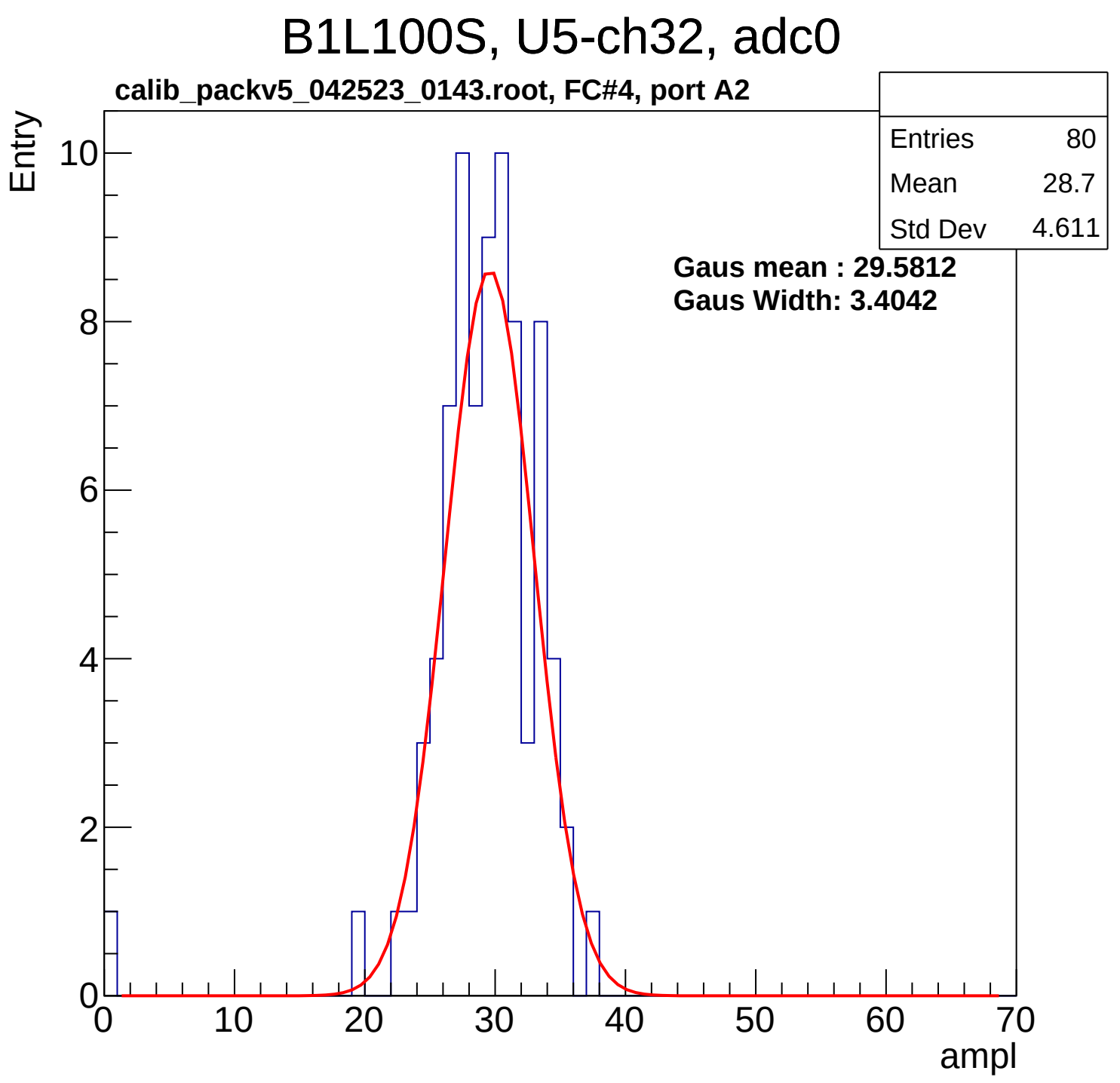

B1L100S, U5-ch31, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 48.04
Std Dev 3.296
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

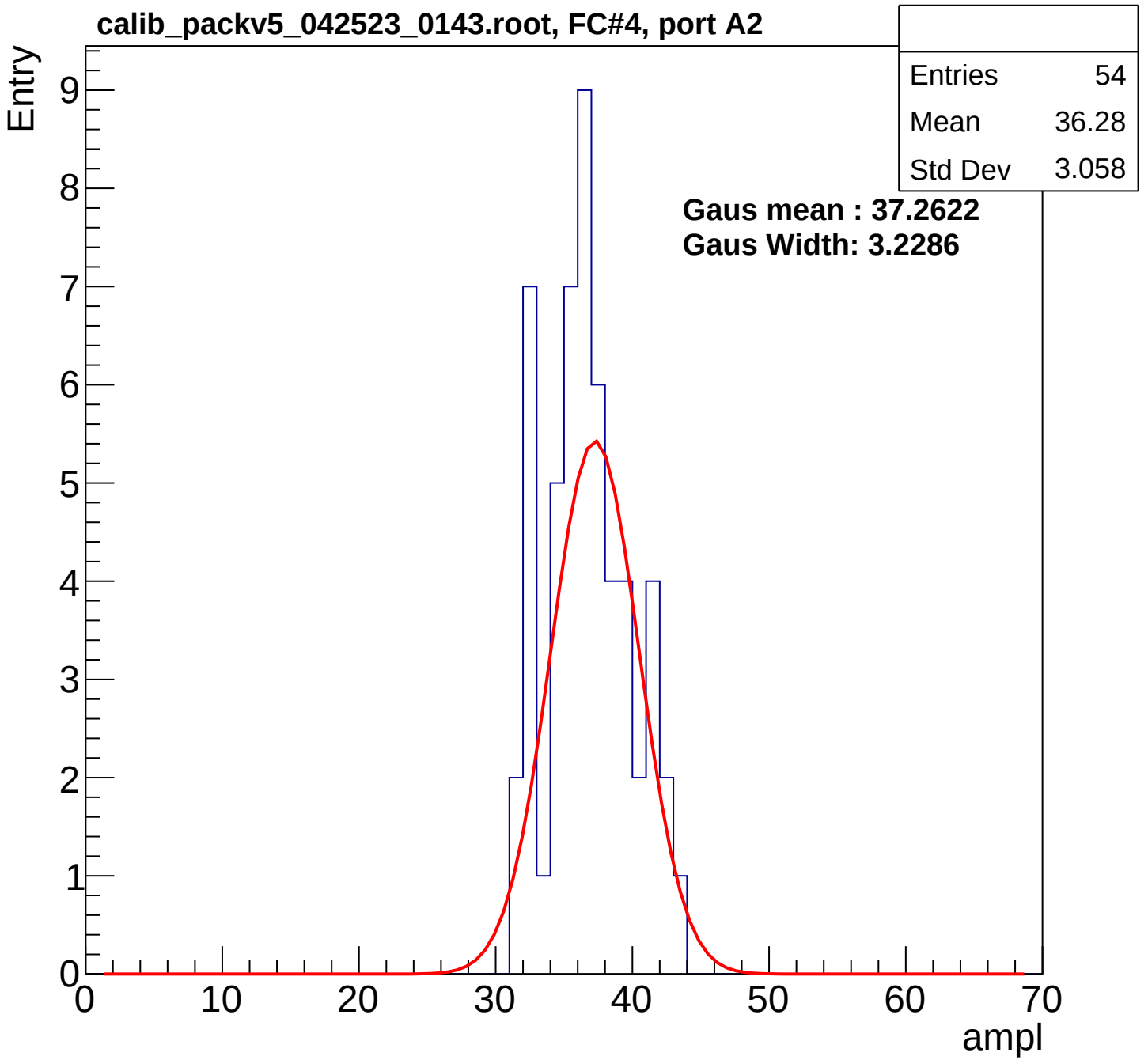

B1L100S, U5-ch31, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 53.77
Std Dev 3.505
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

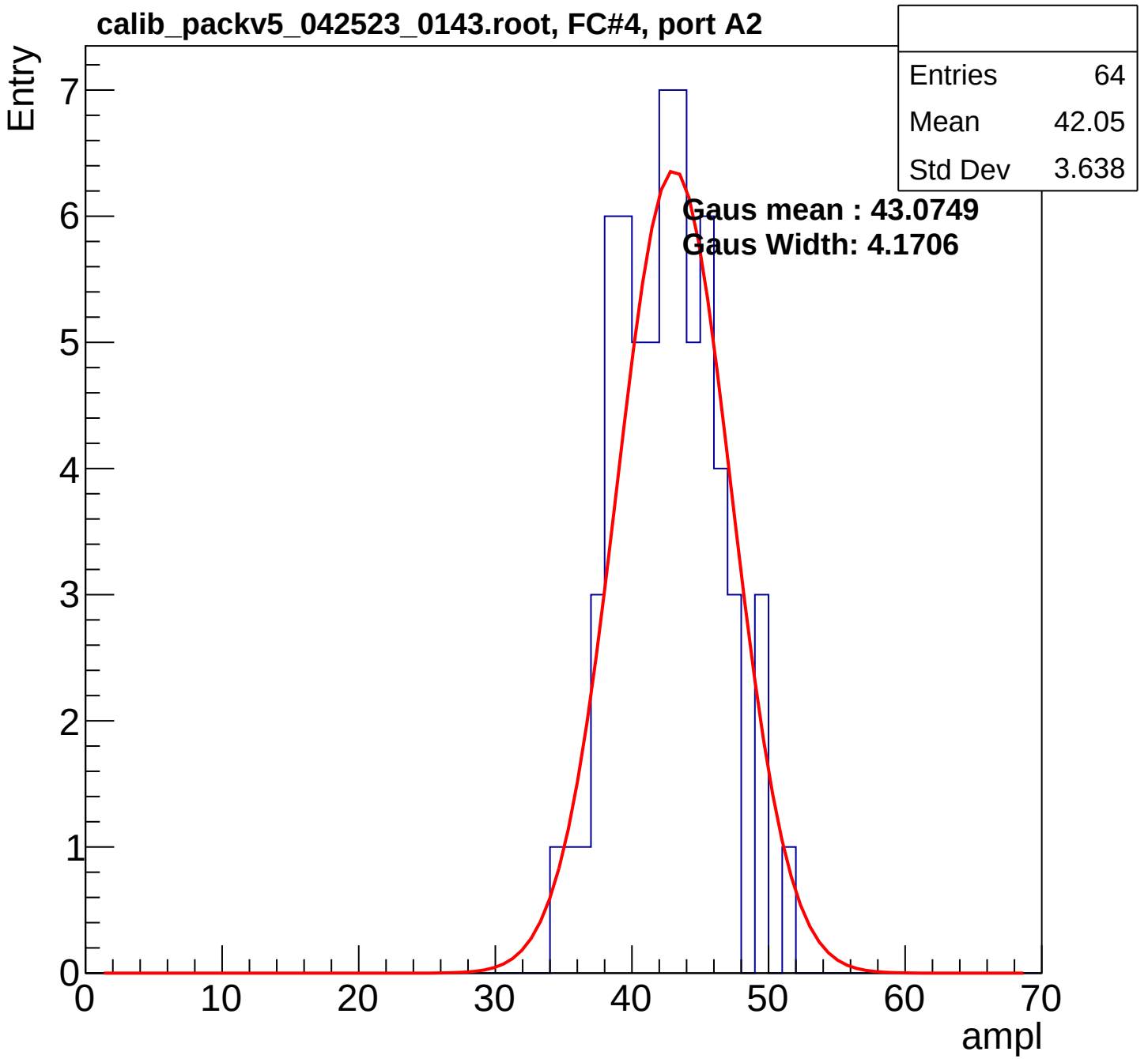

B1L100S, U5-ch31, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 58.98
Std Dev 2.616
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

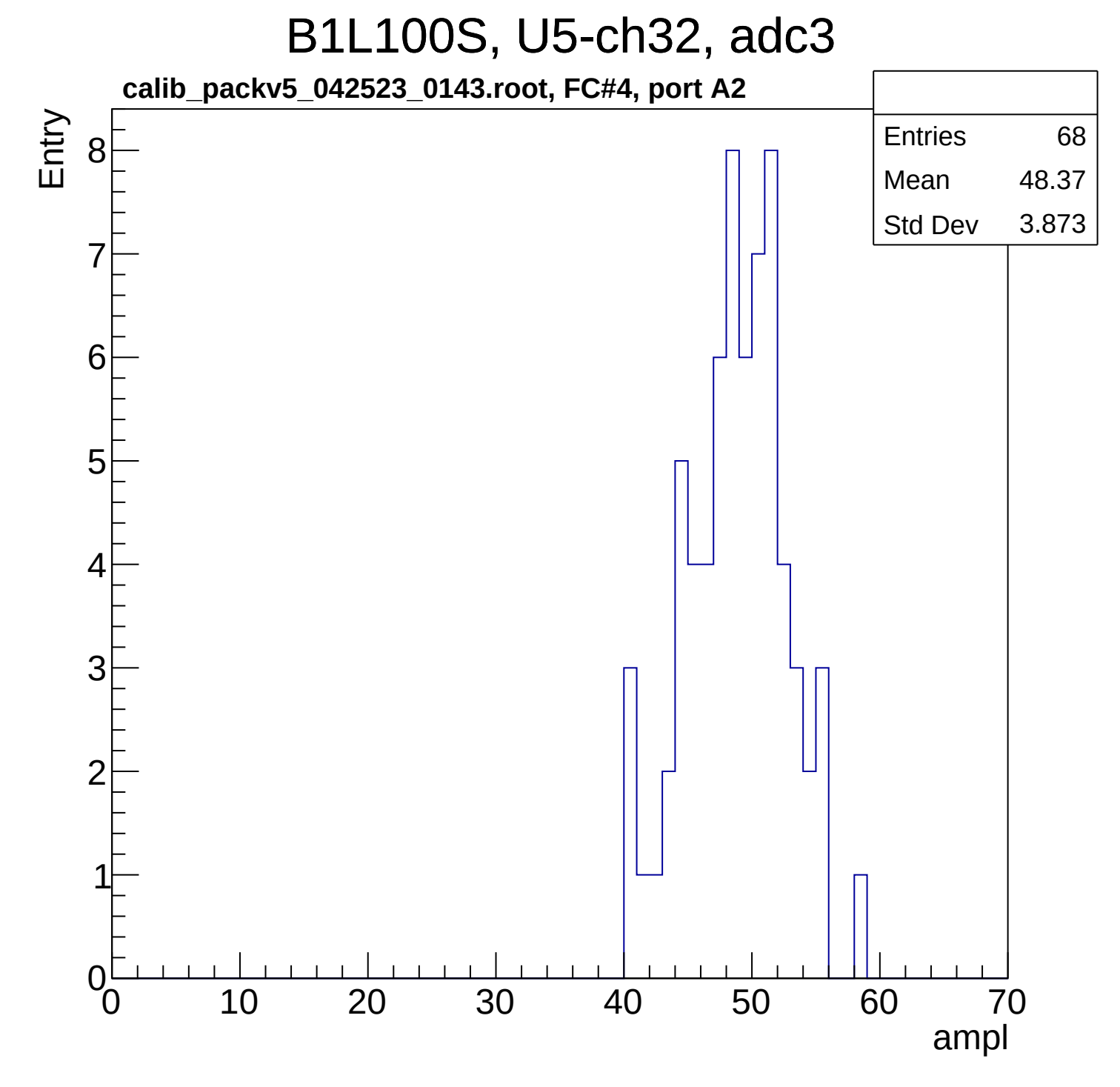

B1L100S, U5-ch31, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 9
Mean 54.78
Std Dev 19.41
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L100S, U5-ch31, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch32, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 80
Mean 28.7
Std Dev 4.611
Gaus mean : 29.5812
Gaus Width: 3.4042
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch32, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 36.28
Std Dev 3.058
Gaus mean : 37.2622
Gaus Width: 3.2286
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch32, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 42.05
Std Dev 3.638
Gaus mean : 43.0749
Gaus Width: 4.1706
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U5-ch32, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 48.37
Std Dev 3.873
Entry
ampl
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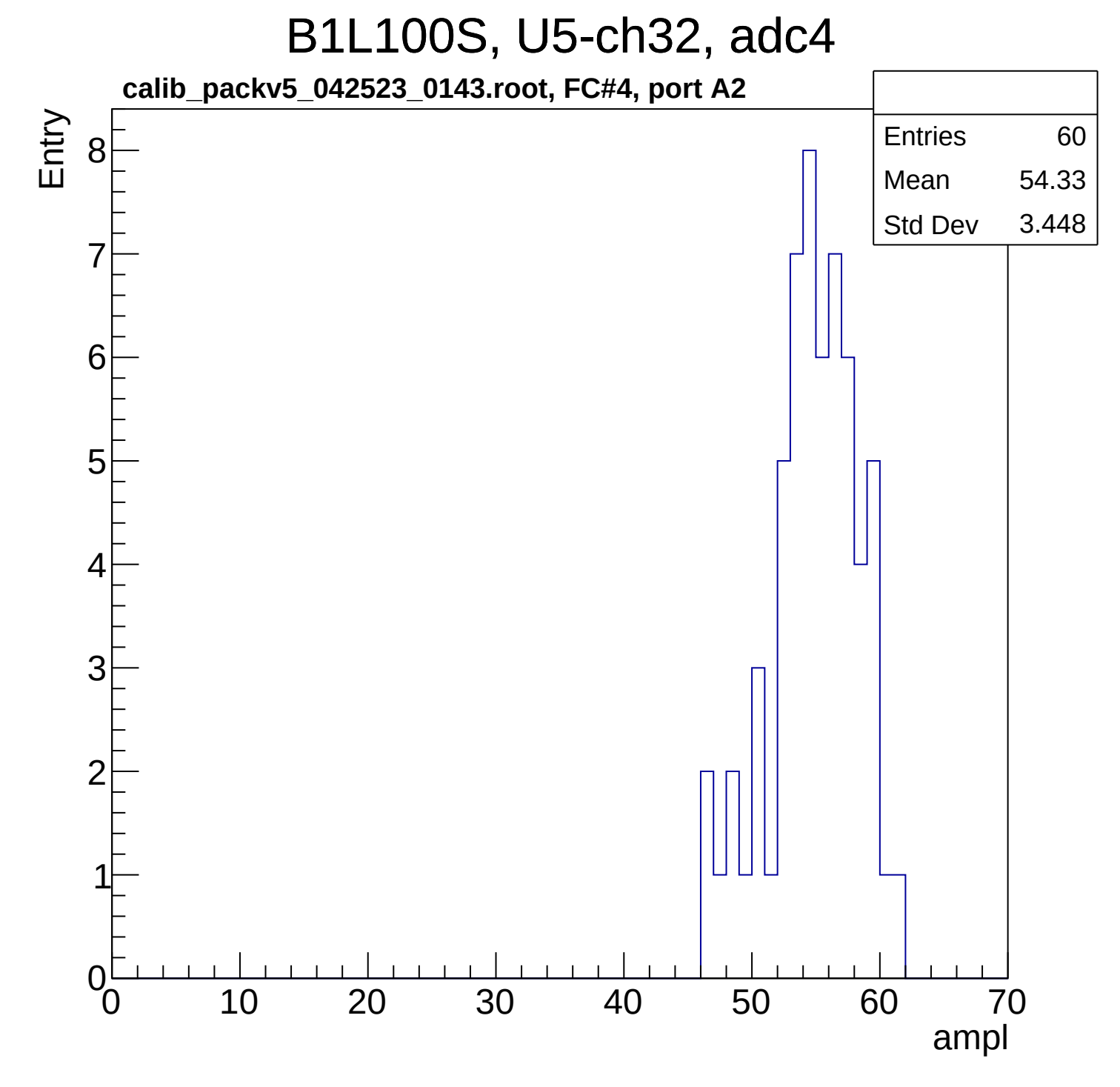
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch32, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 54.33
Std Dev 3.448
Entry
ampl
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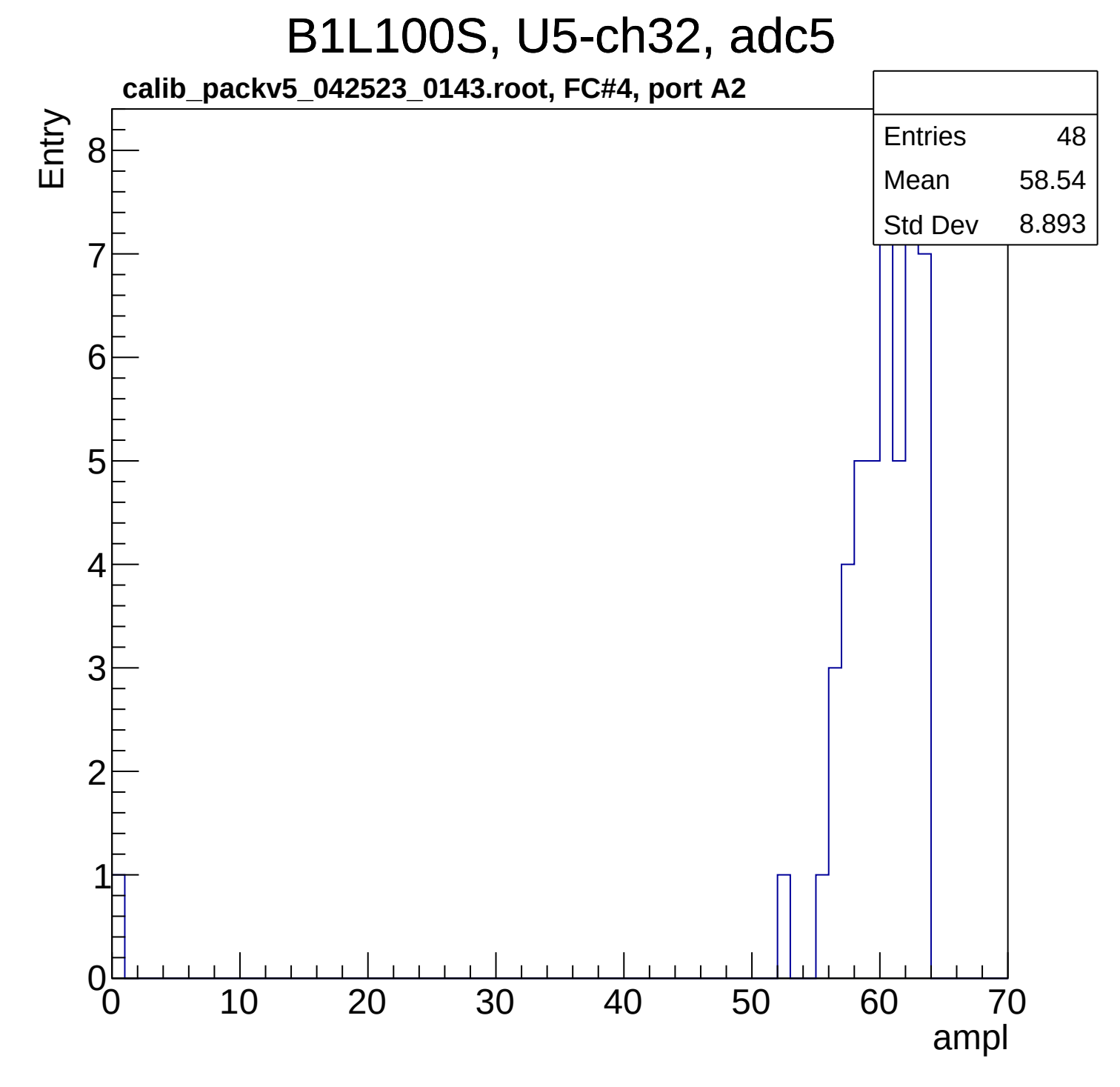
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch32, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 48
Mean 58.54
Std Dev 8.893
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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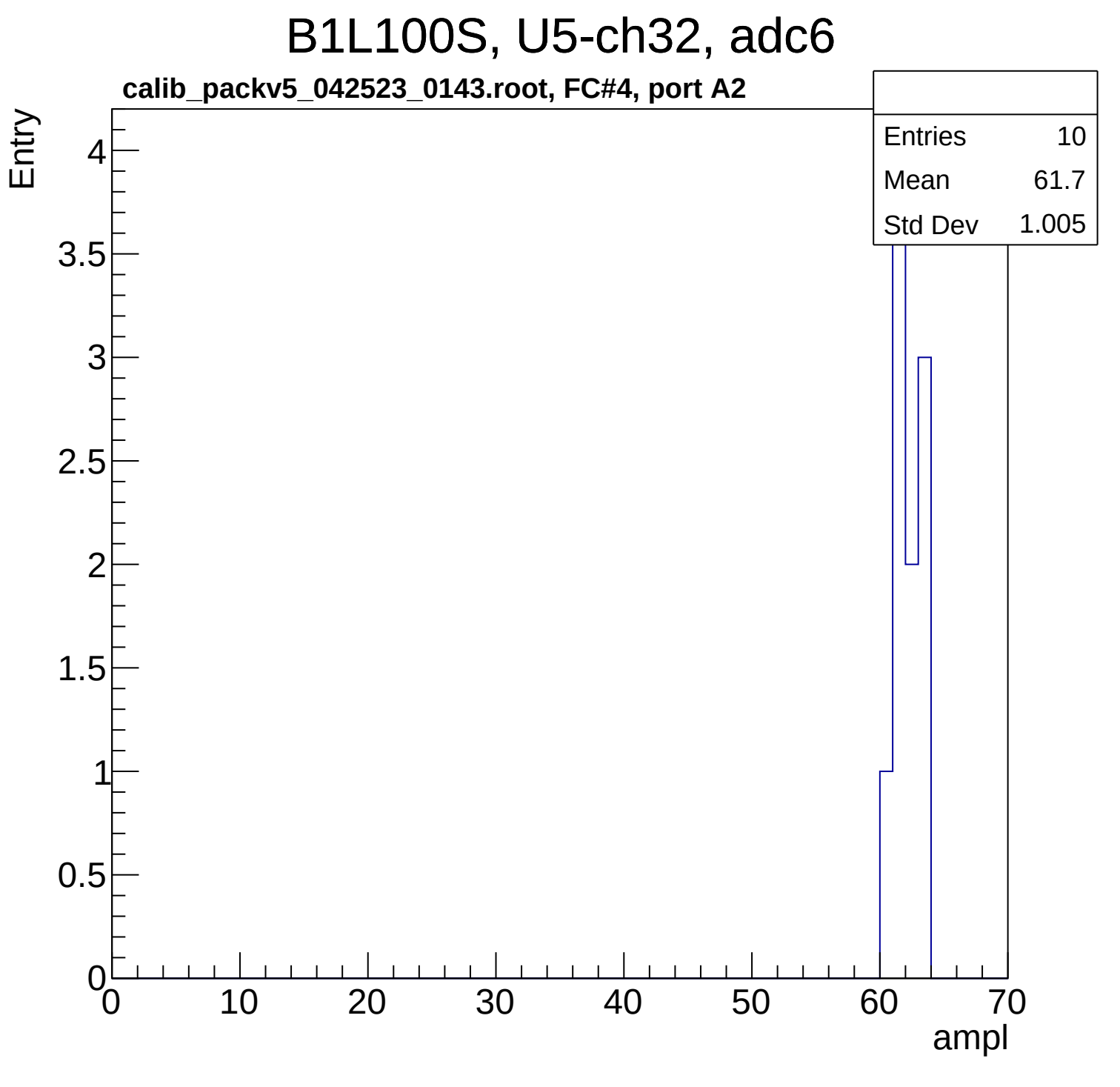
B1L100S, U5-ch32, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 10
Mean 61.7
Std Dev 1.005
Entry
ampl
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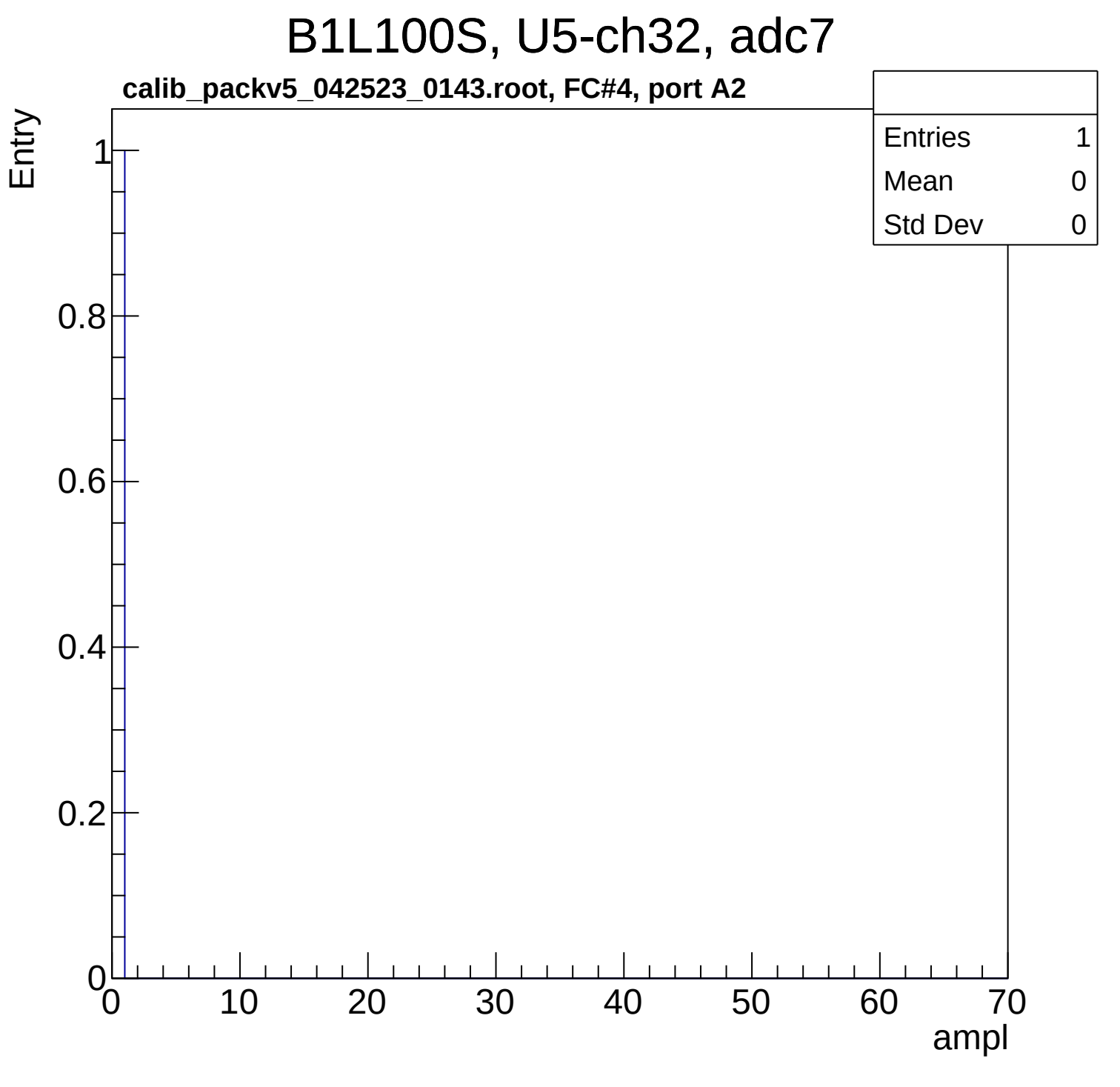
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L100S, U5-ch32, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
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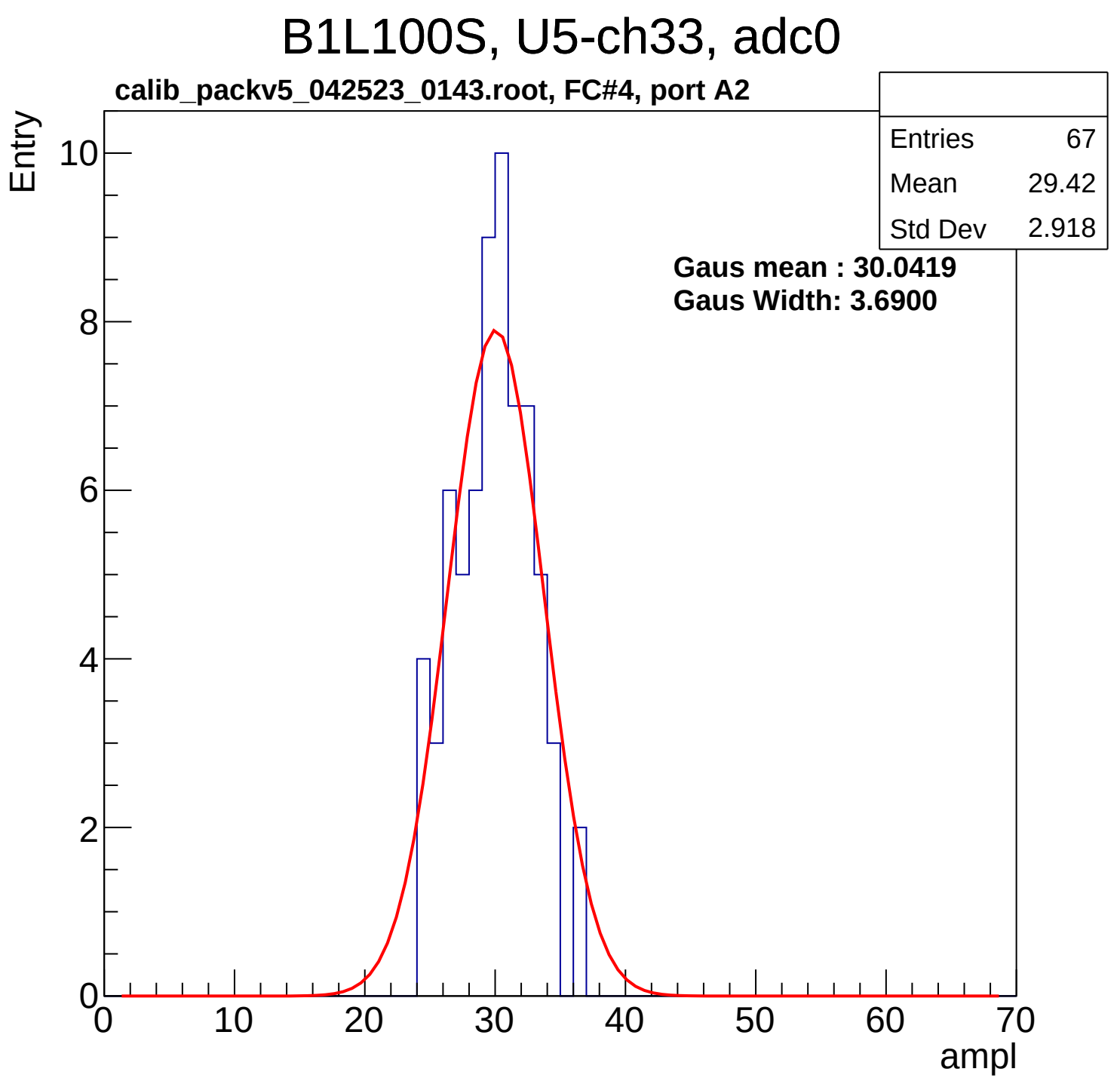
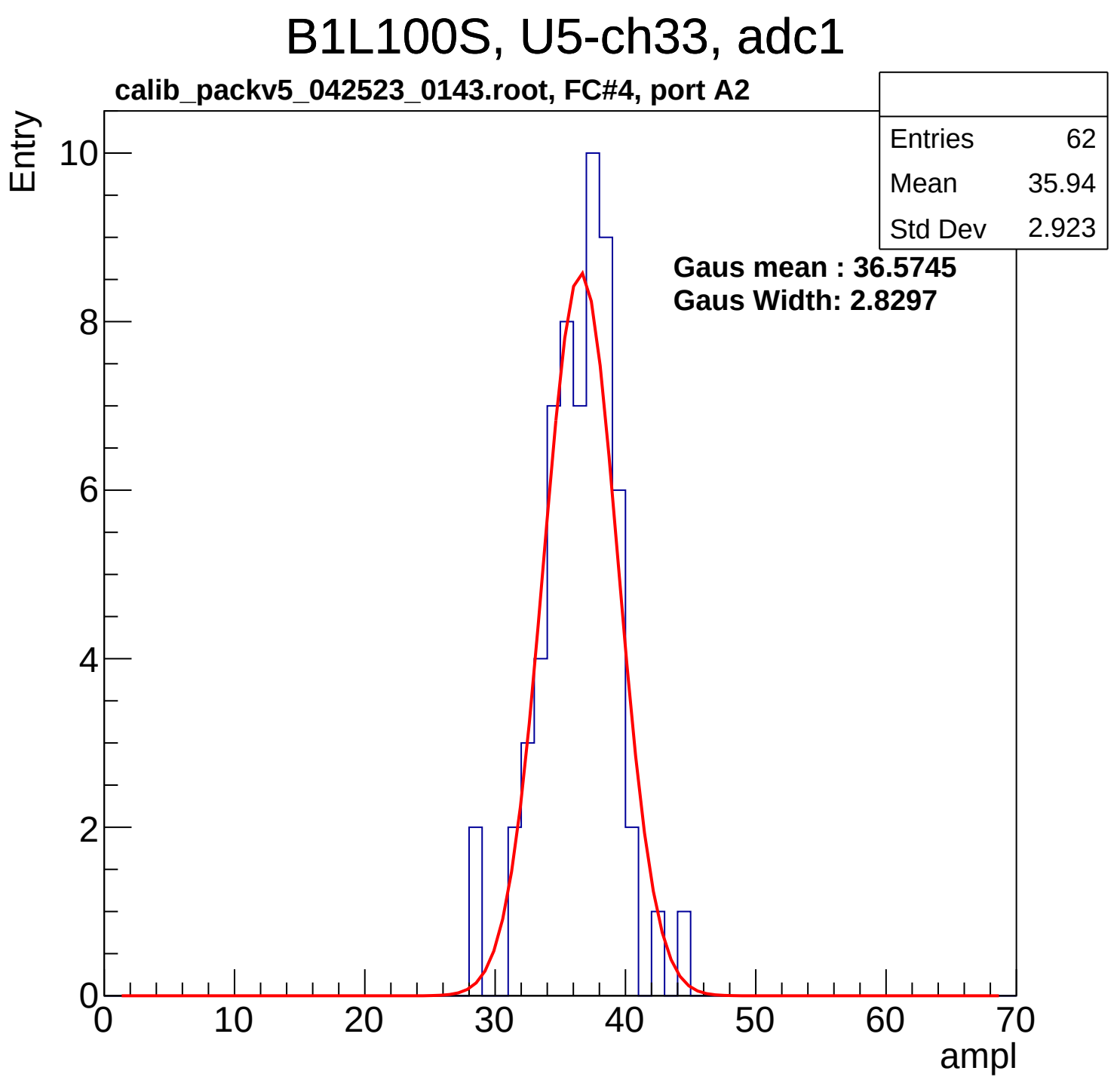
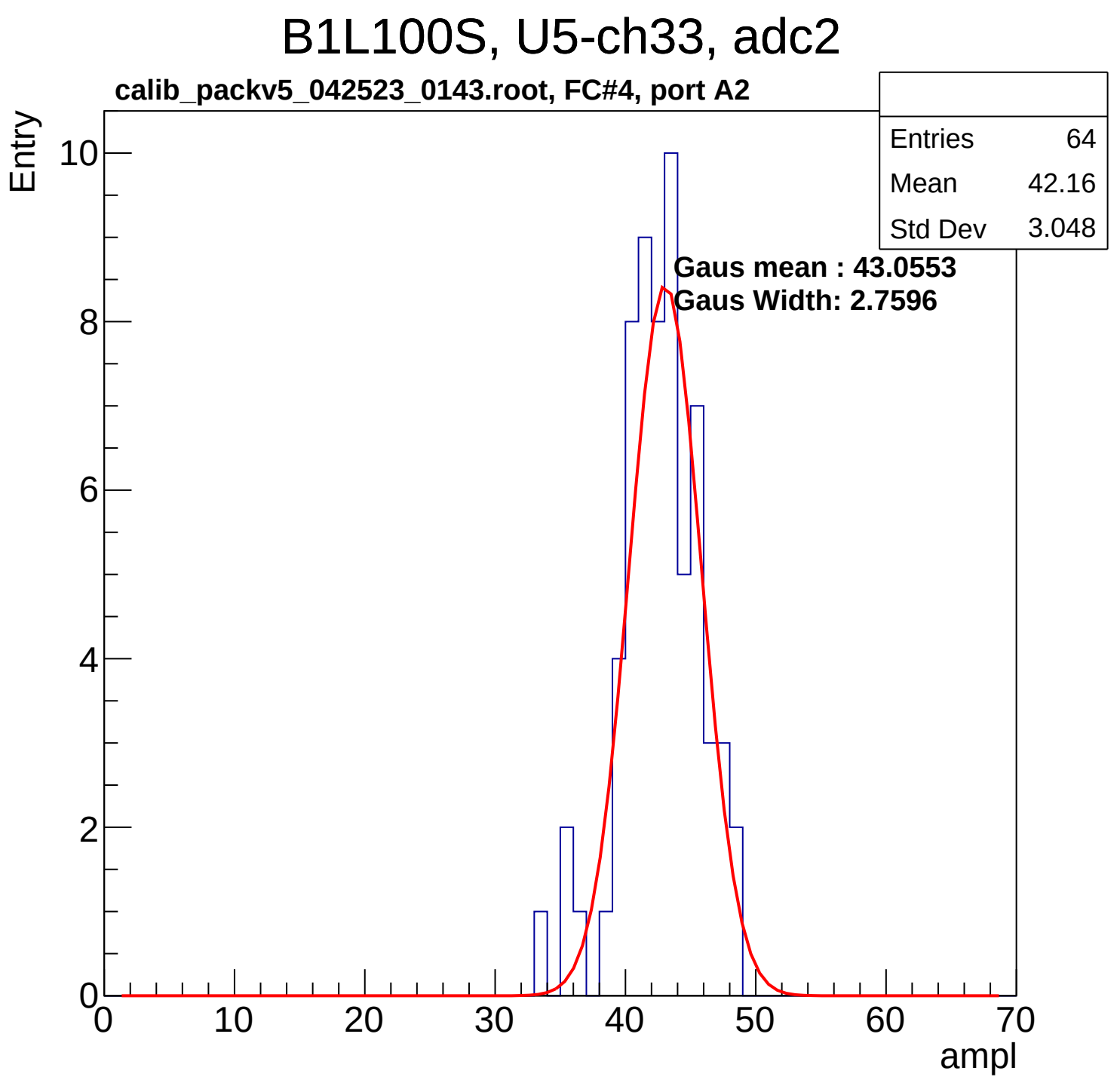
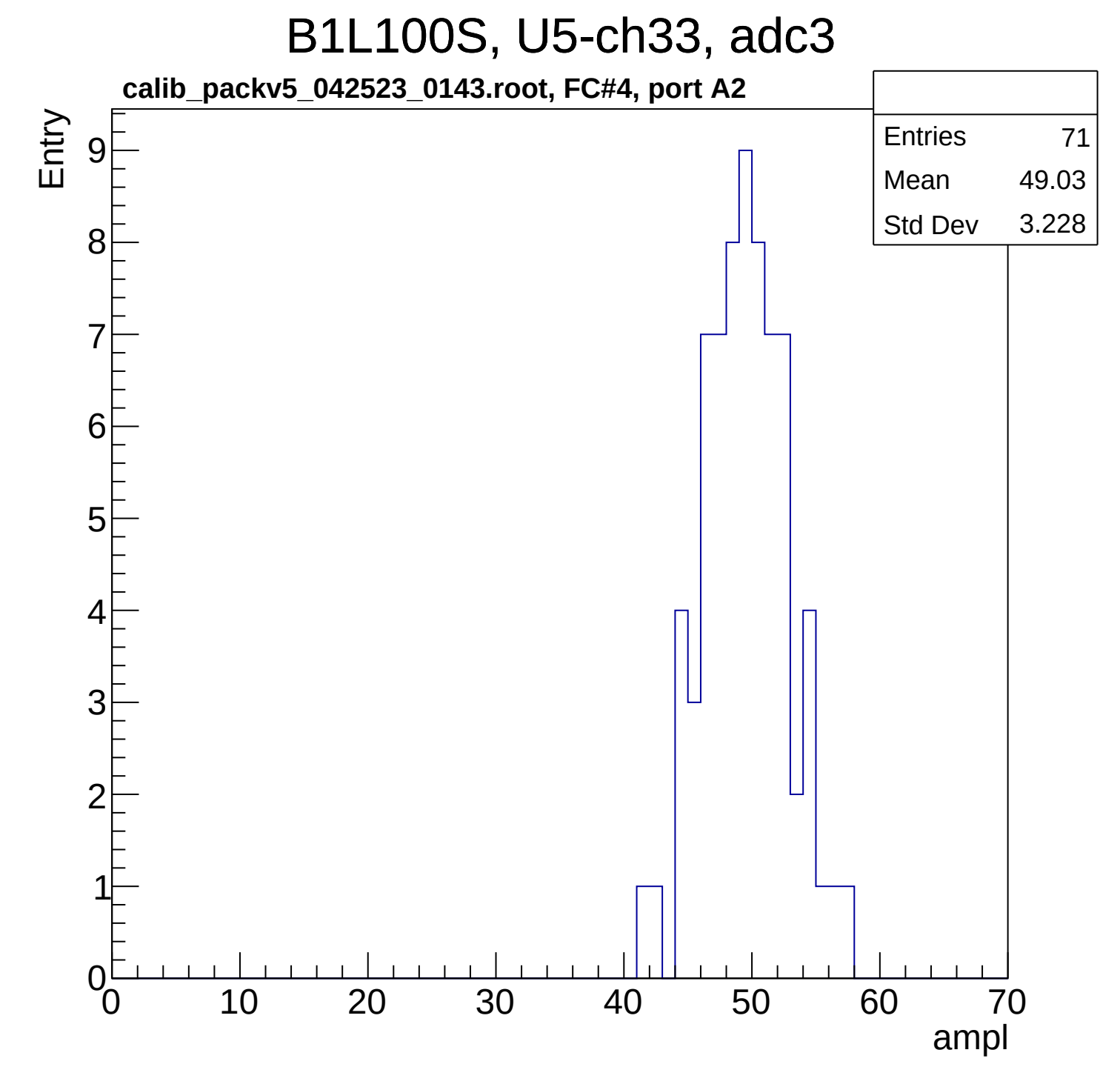
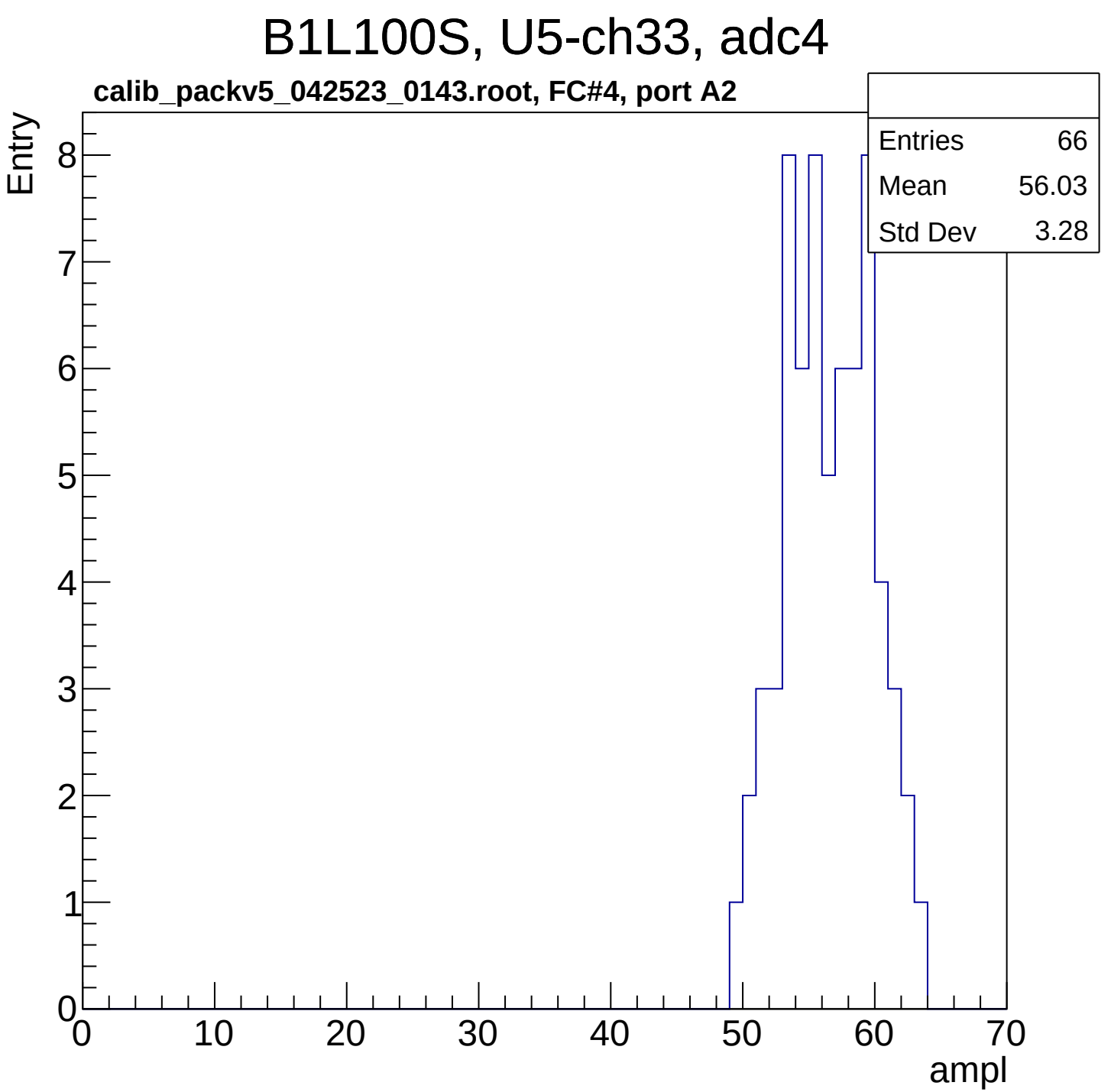
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch33, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 29.42
Std Dev 2.918
Gaus mean : 30.0419
Gaus Width: 3.6900
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch33, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 35.94
Std Dev 2.923
Gaus mean : 36.5745
Gaus Width: 2.8297
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch33, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 42.16
Std Dev 3.048
Gaus mean : 43.0553
Gaus Width: 2.7596
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch33, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 49.03
Std Dev 3.228
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch33, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 56.03
Std Dev 3.28
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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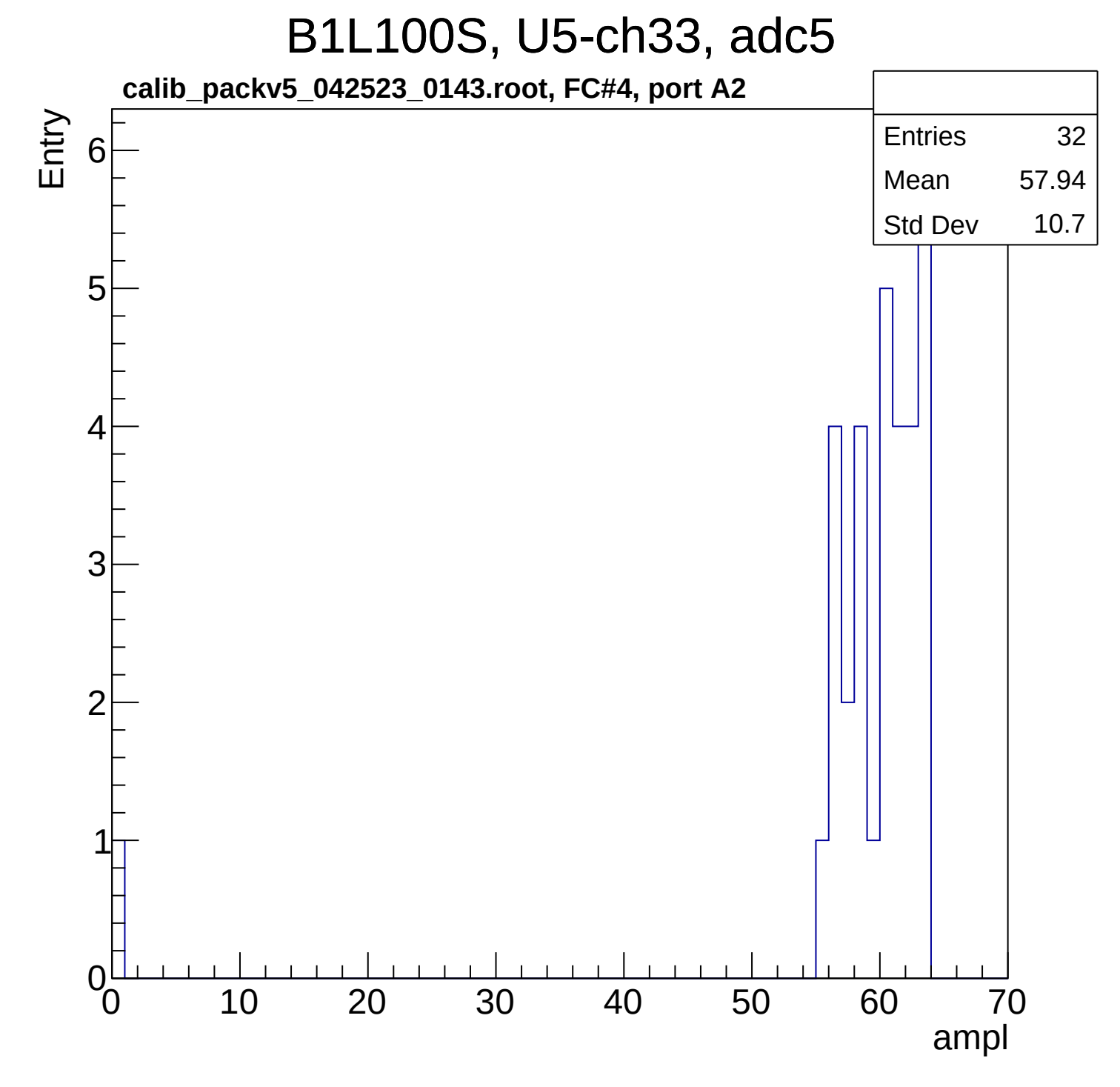
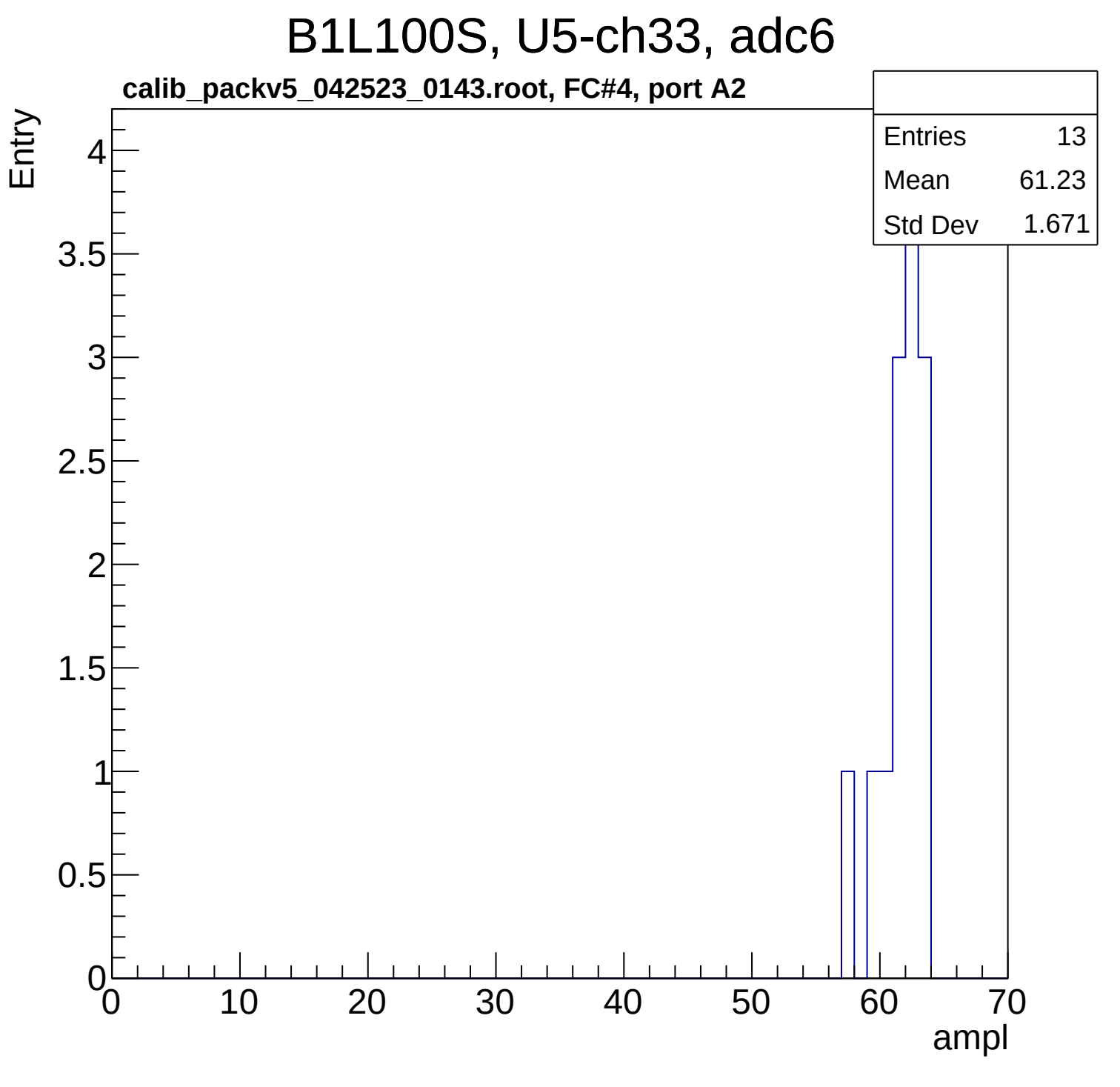
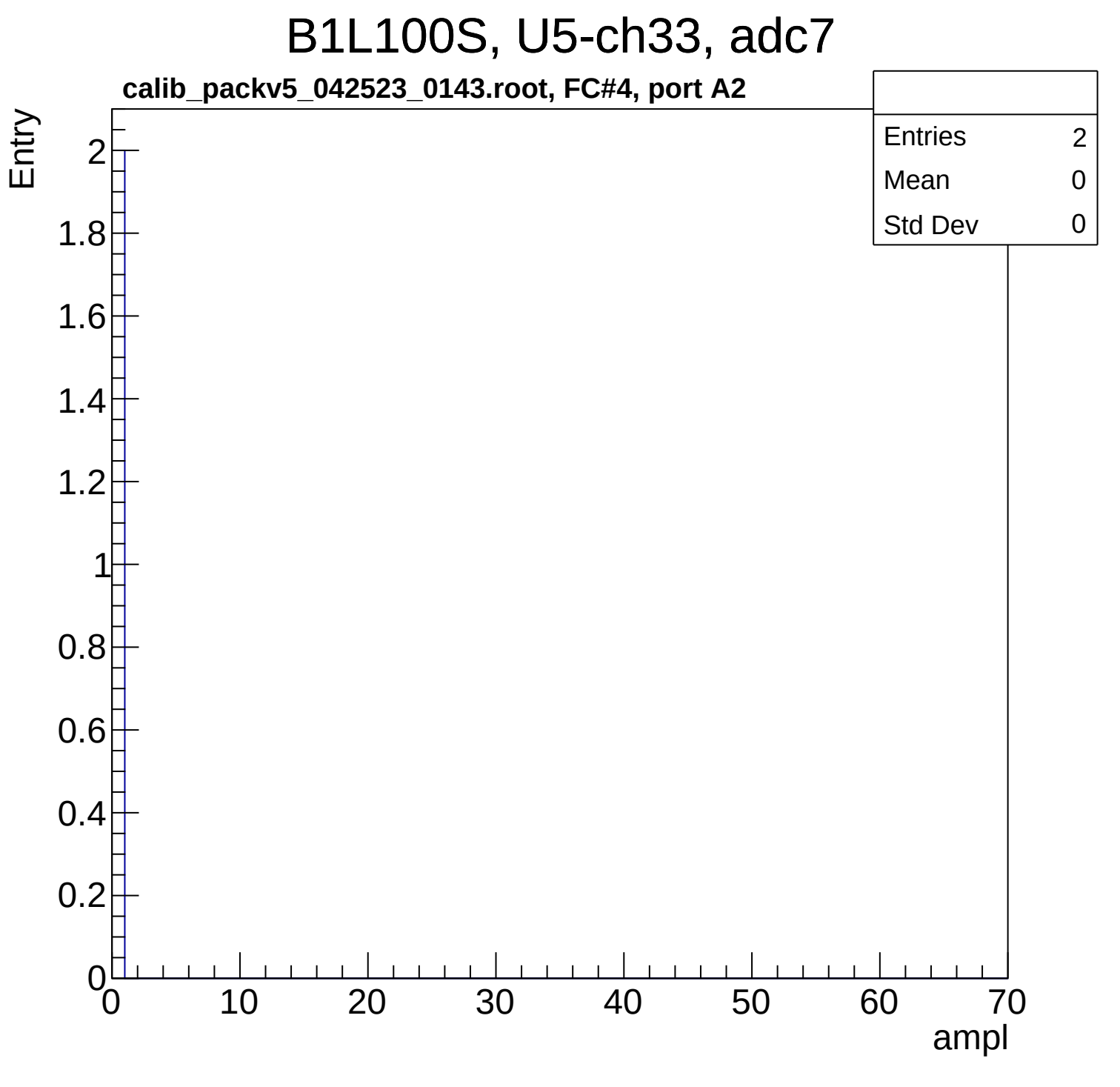

B1L100S, U5-ch33, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 32
Mean 57.94
Std Dev 10.7
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L100S, U5-ch33, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 13
Mean 61.23
Std Dev 1.671
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L100S, U5-ch33, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
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0.6
0.4
0.2
0
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10
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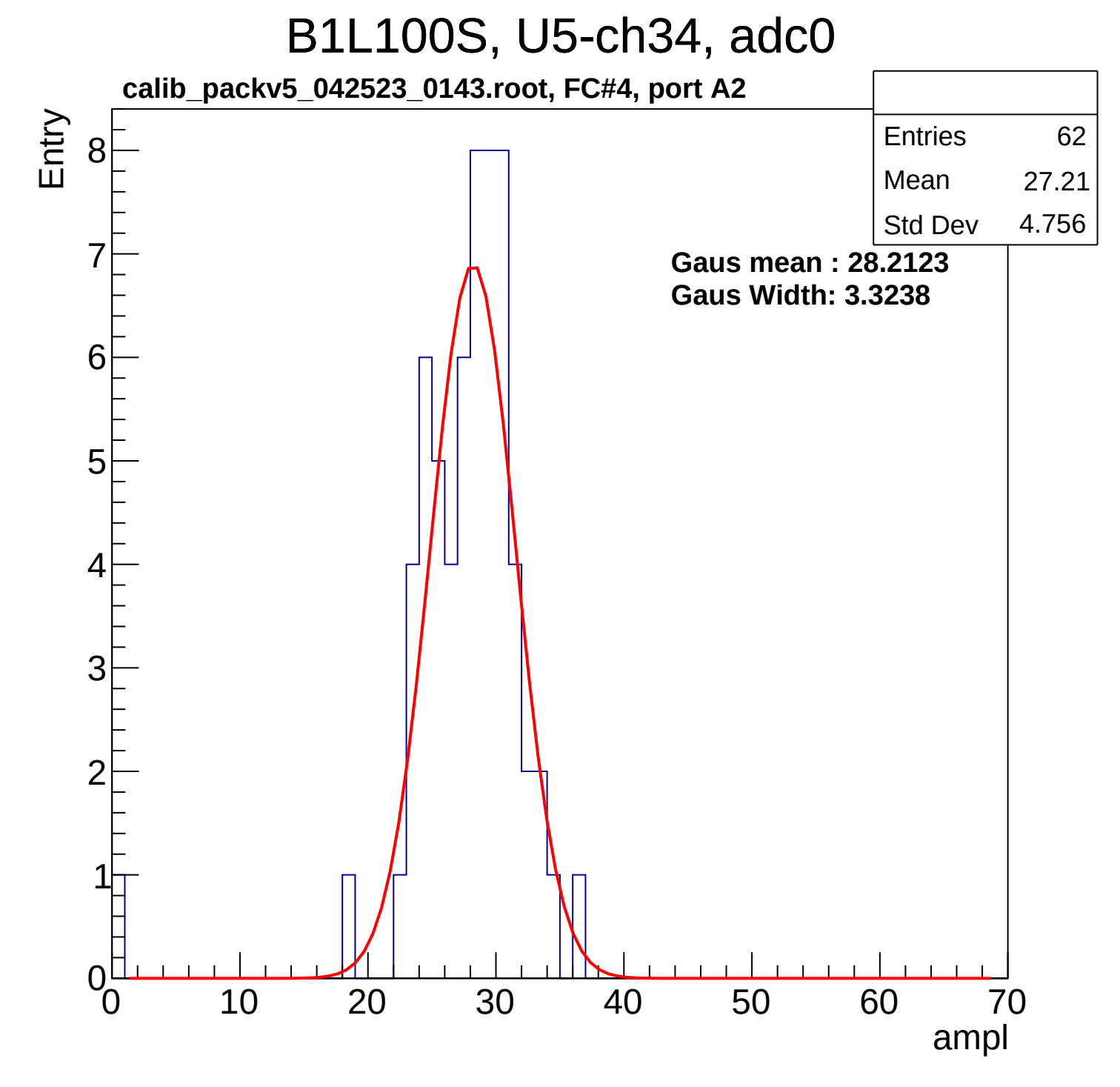
70
ampl


B1L100S, U5-ch34, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 27.21
Std Dev 4.756
Gaus mean : 28.2123
Gaus Width: 3.3238
Entry
ampl
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1
2
3
4
5
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7
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0
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40
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60
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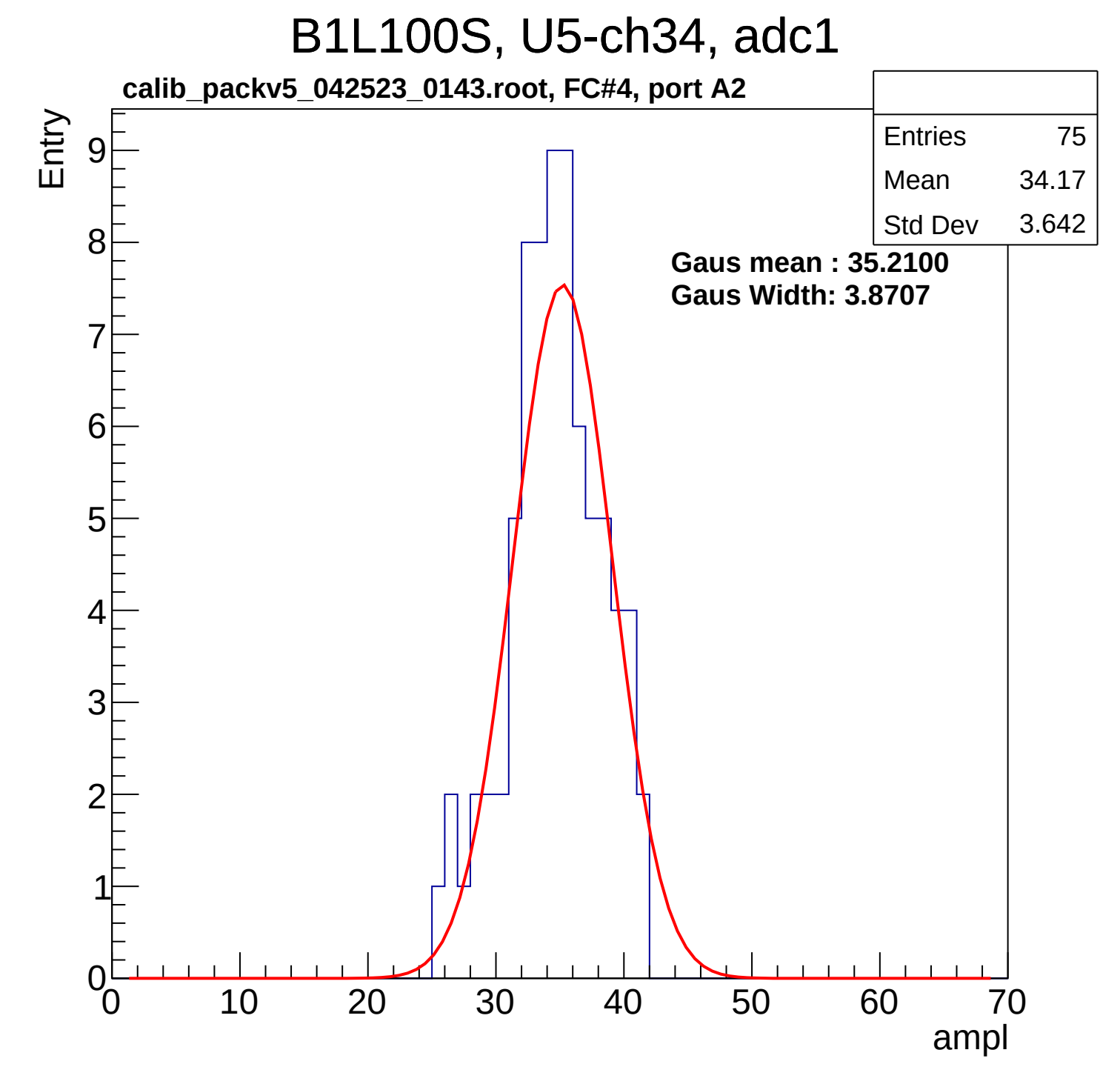
B1L100S, U5-ch34, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 75
Mean 34.17
Std Dev 3.642
Gaus mean : 35.2100
Gaus Width: 3.8707
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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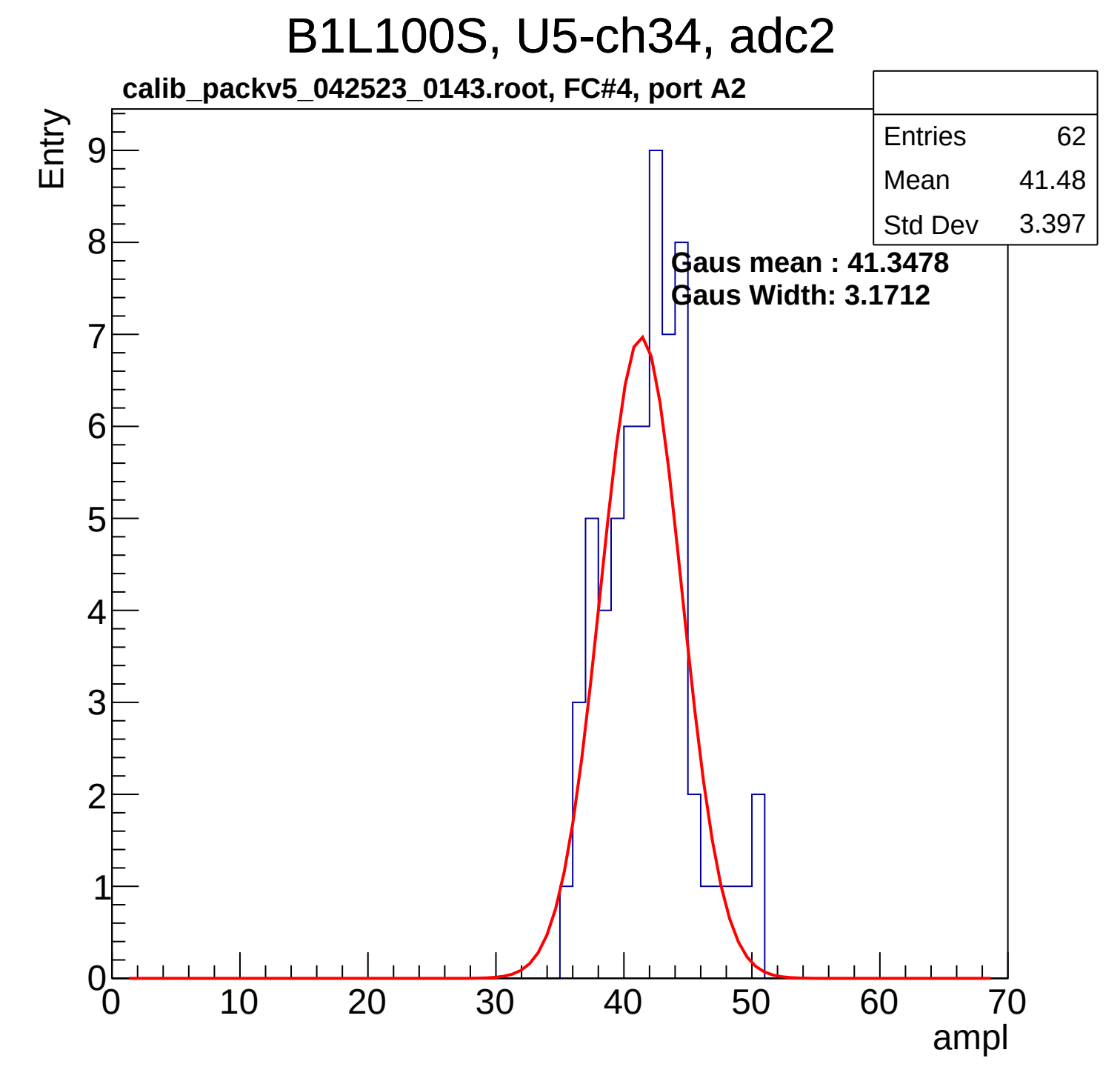
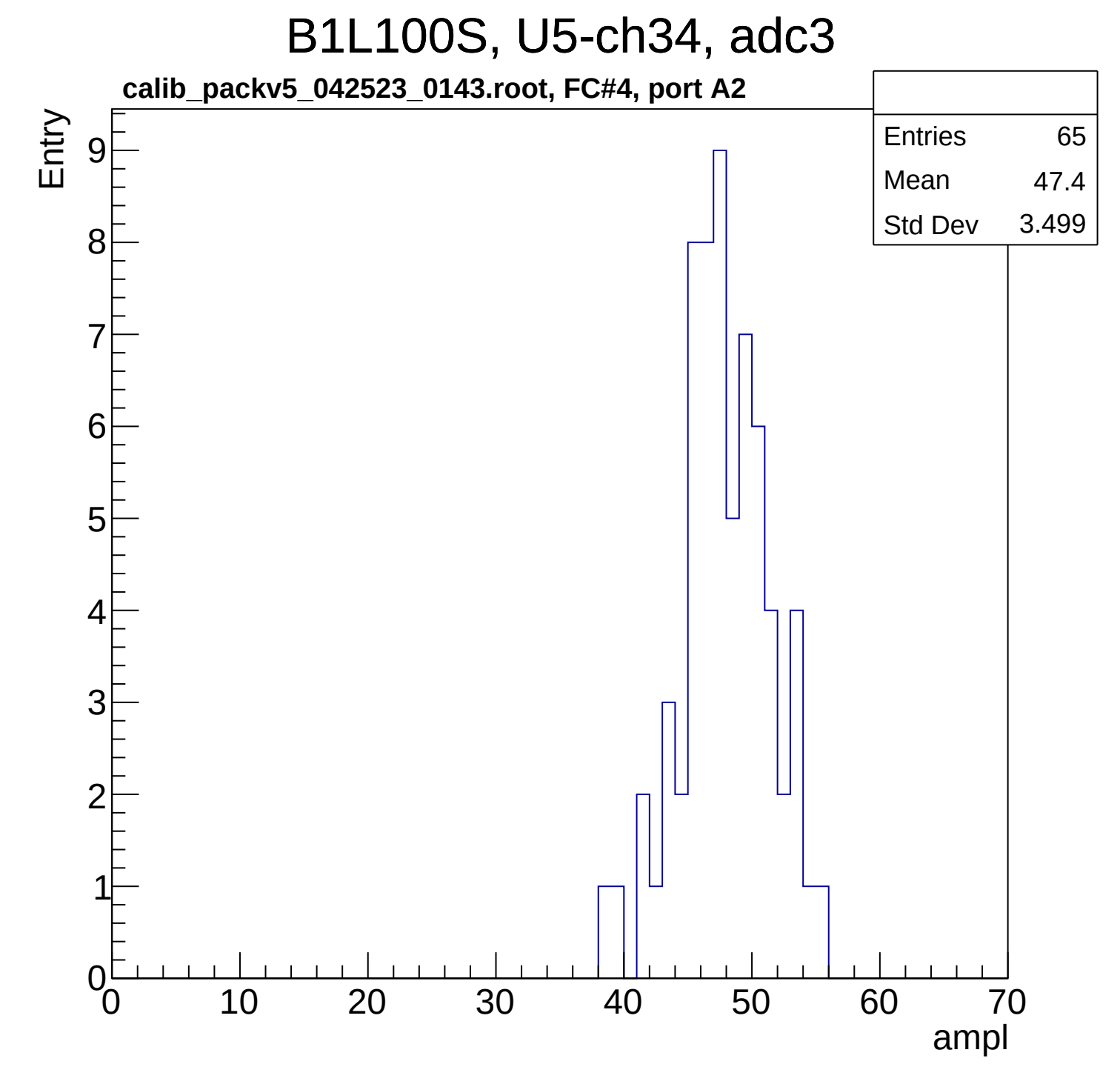

B1L100S, U5-ch34, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 41.48
Std Dev 3.397
Gaus mean : 41.3478
Gaus Width: 3.1712
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L100S, U5-ch34, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 47.4
Std Dev 3.499
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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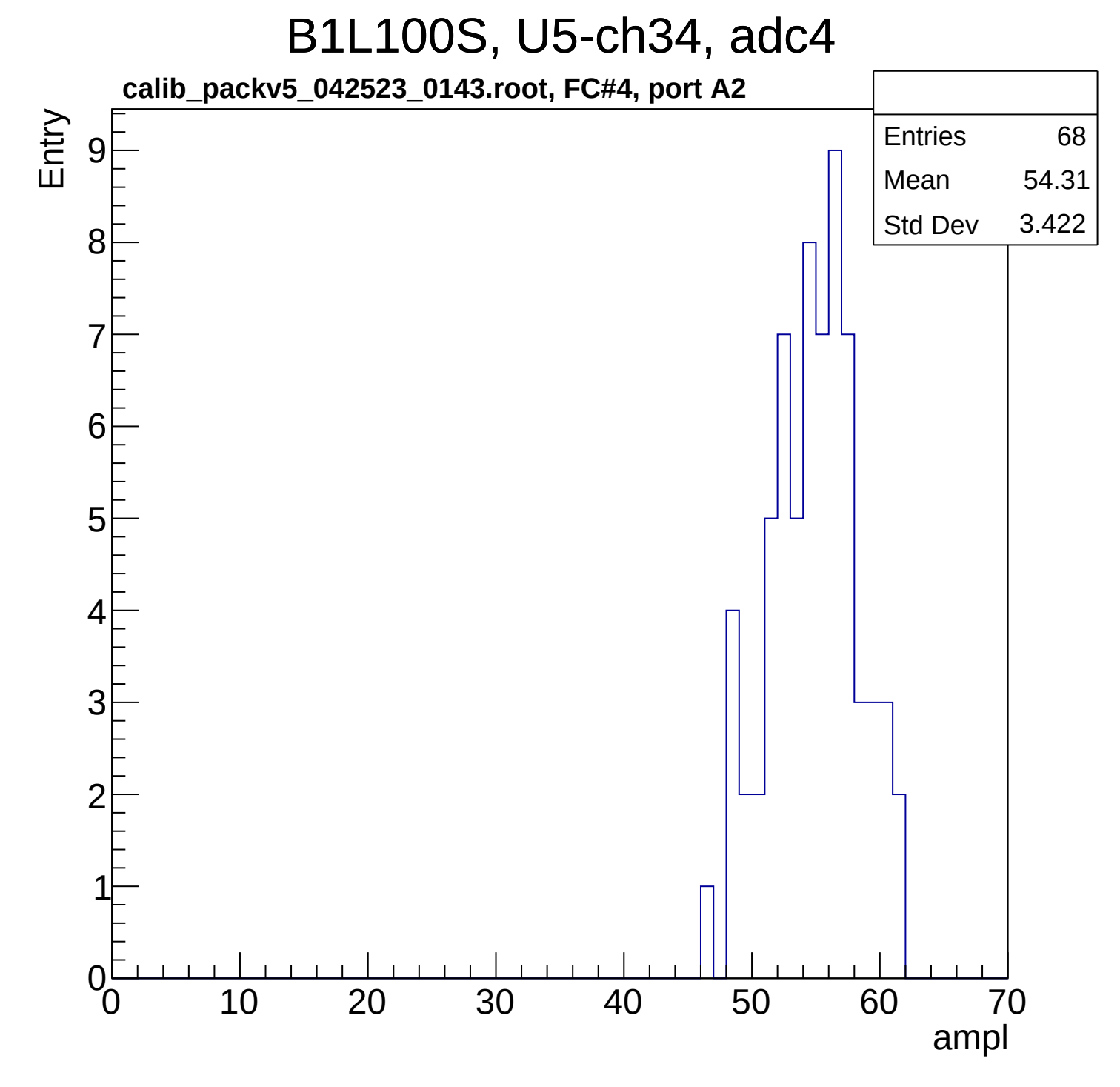
40
50
60
70


B1L100S, U5-ch34, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 54.31
Std Dev 3.422
Entry
ampl
0
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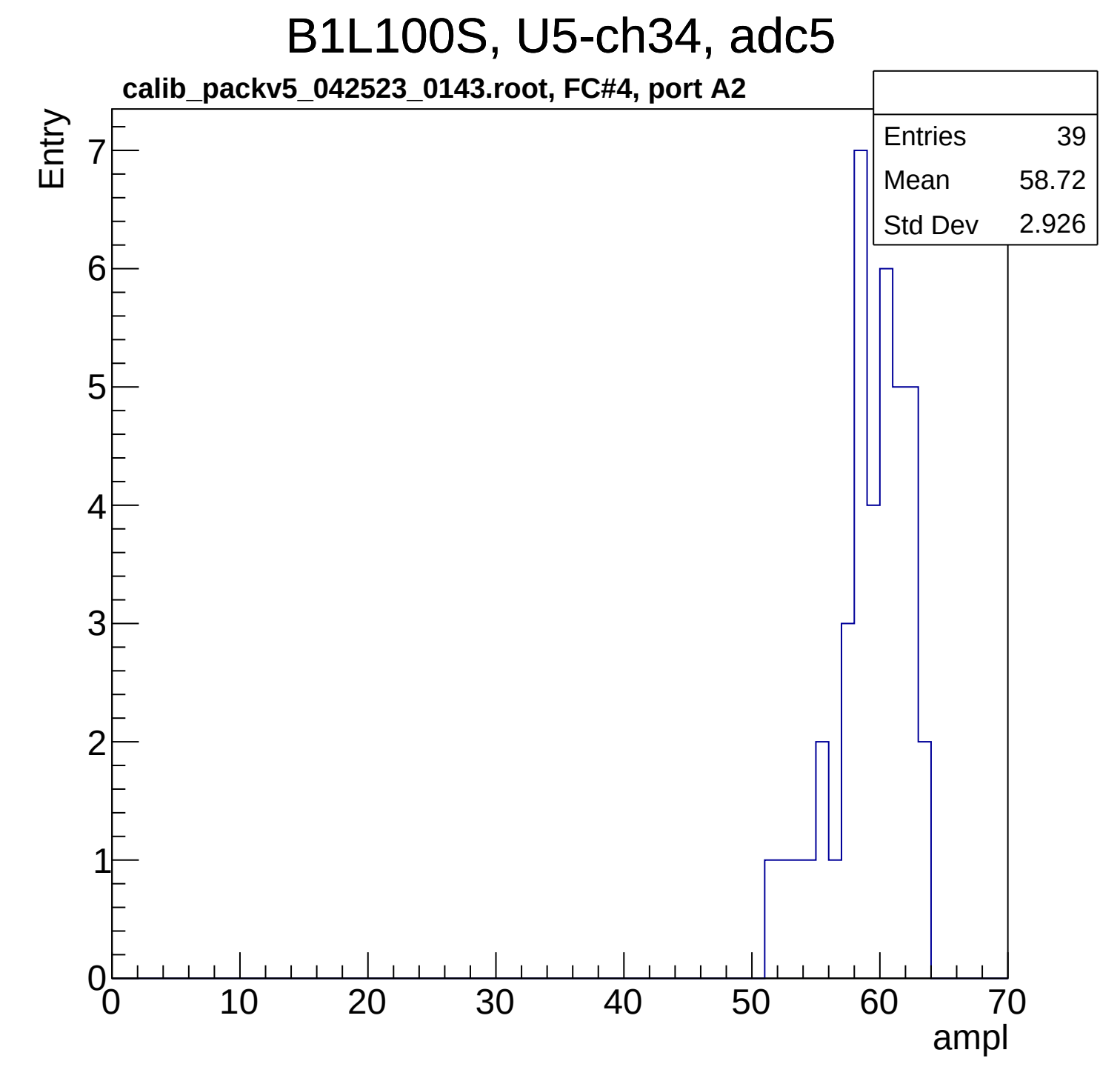
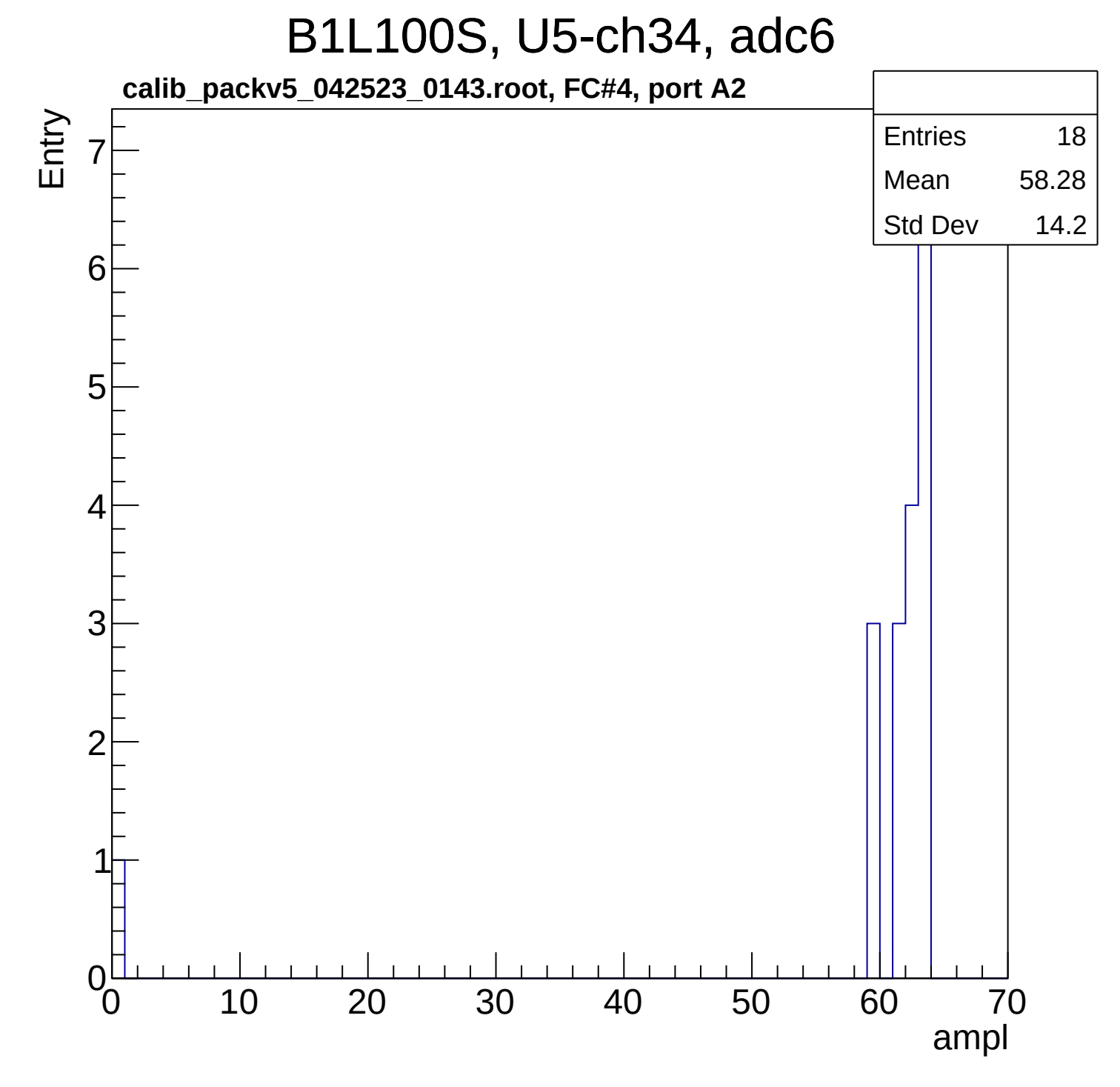
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch34, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 39
Mean 58.72
Std Dev 2.926
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U5-ch34, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 18
Mean 58.28
Std Dev 14.2
Entry
ampl
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3
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0
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40
50
60
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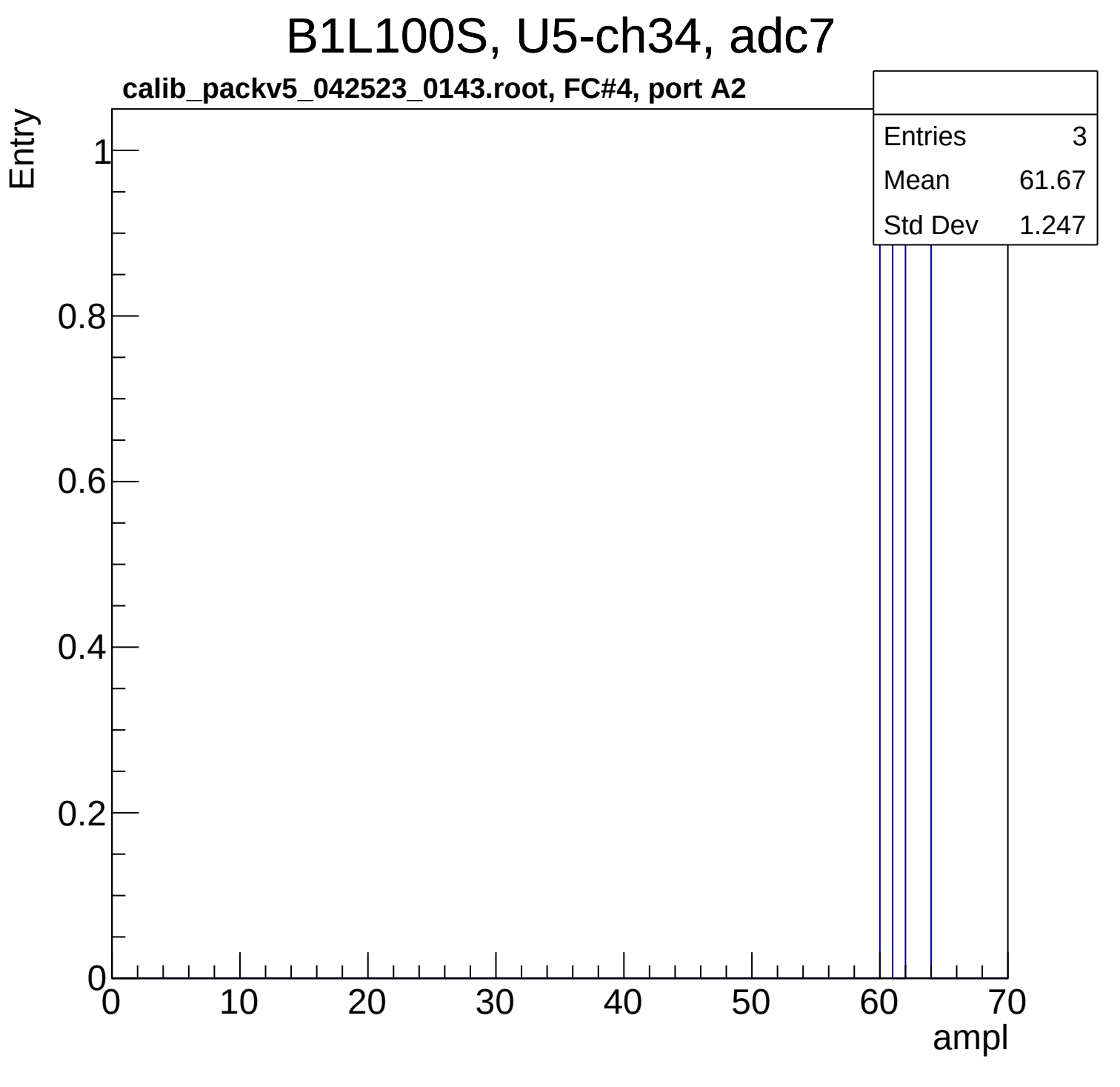
B1L100S, U5-ch34, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 61.67
Std Dev 1.247
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
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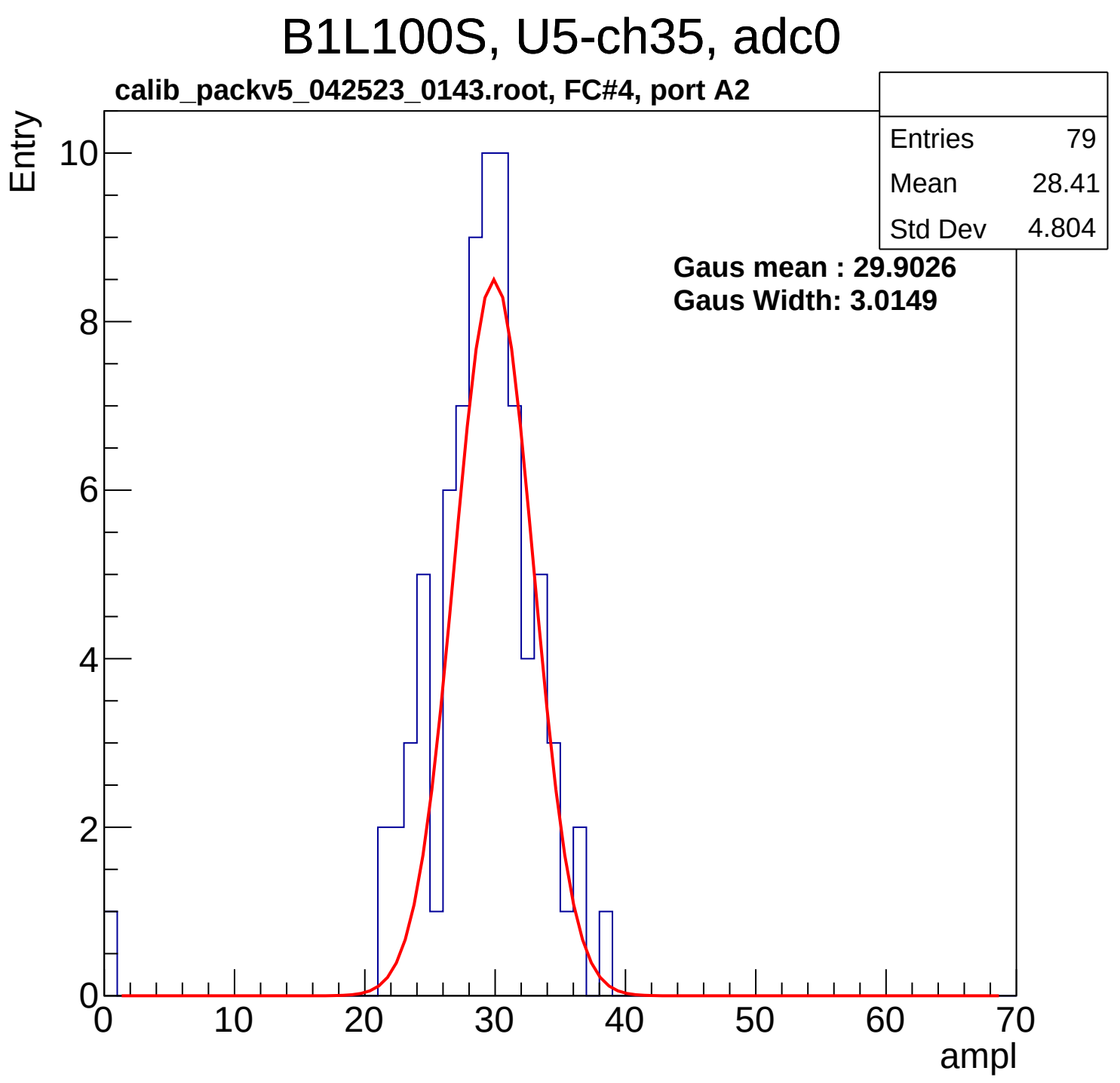
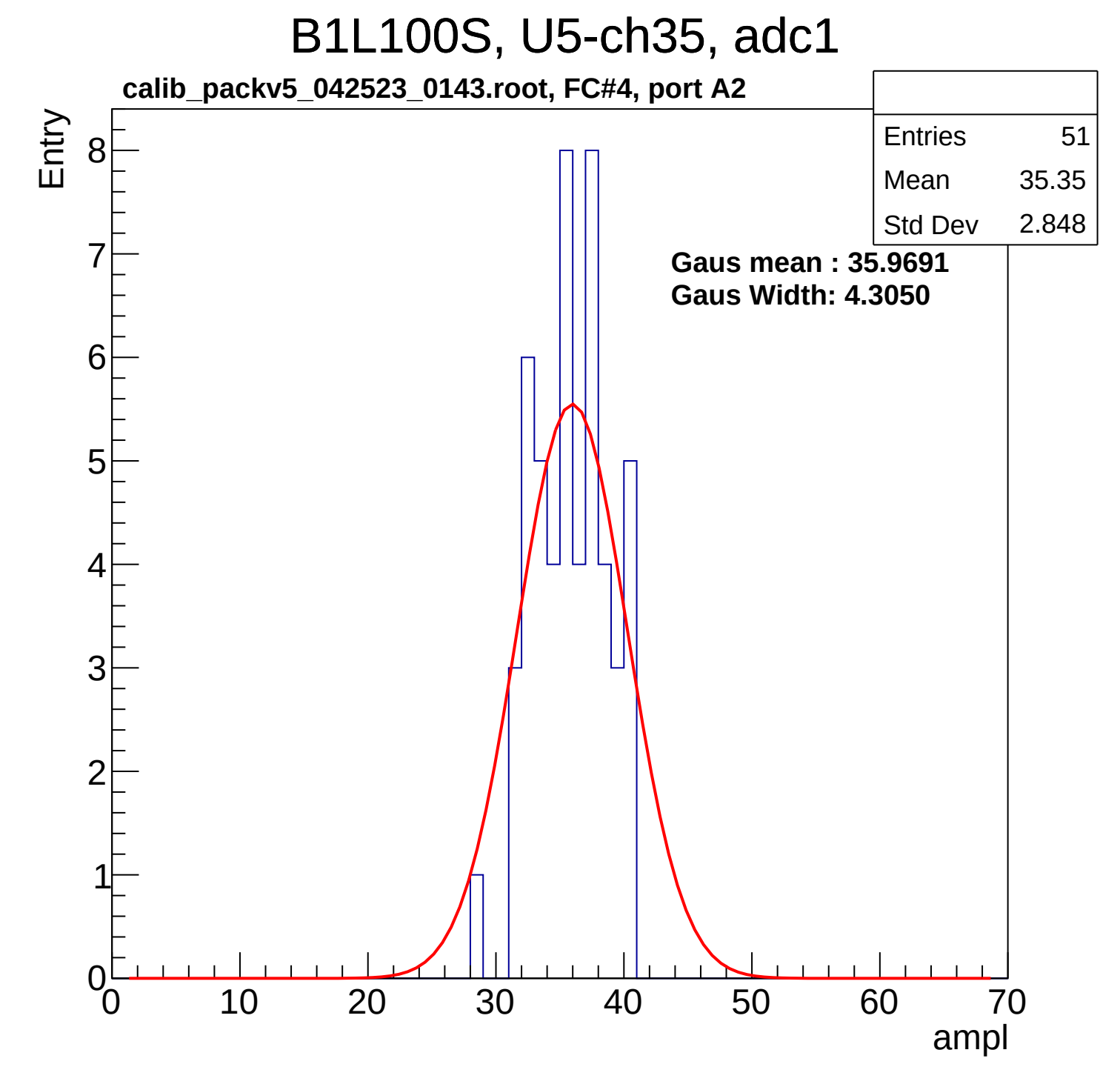
40
50
60
70


B1L100S, U5-ch35, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 79
Mean 28.41
Std Dev 4.804
Gaus mean : 29.9026
Gaus Width: 3.0149
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch35, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 35.35
Std Dev 2.848
Gaus mean : 35.9691
Gaus Width: 4.3050
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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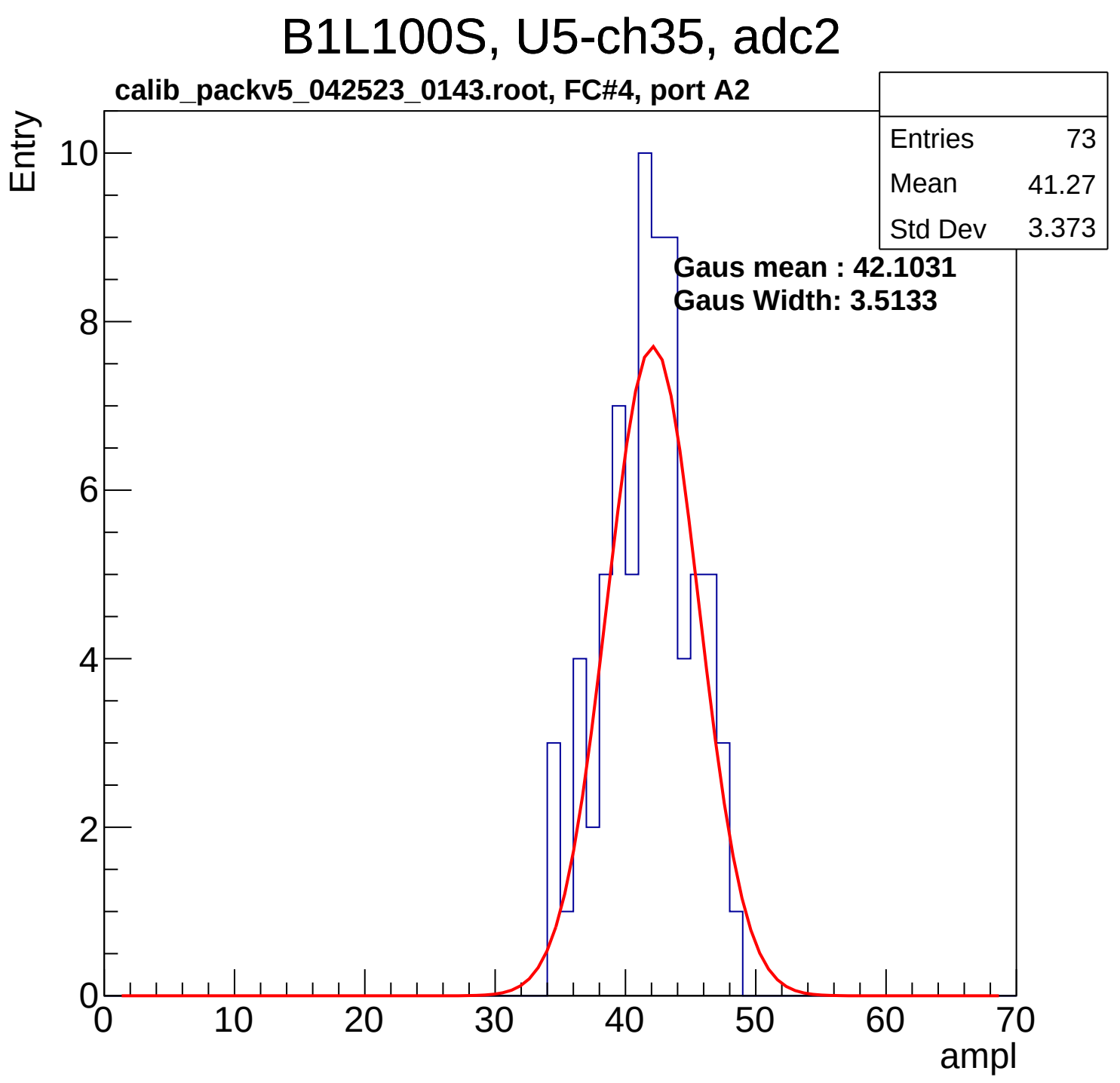
B1L100S, U5-ch35, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 41.27
Std Dev 3.373
Gaus mean : 42.1031
Gaus Width: 3.5133
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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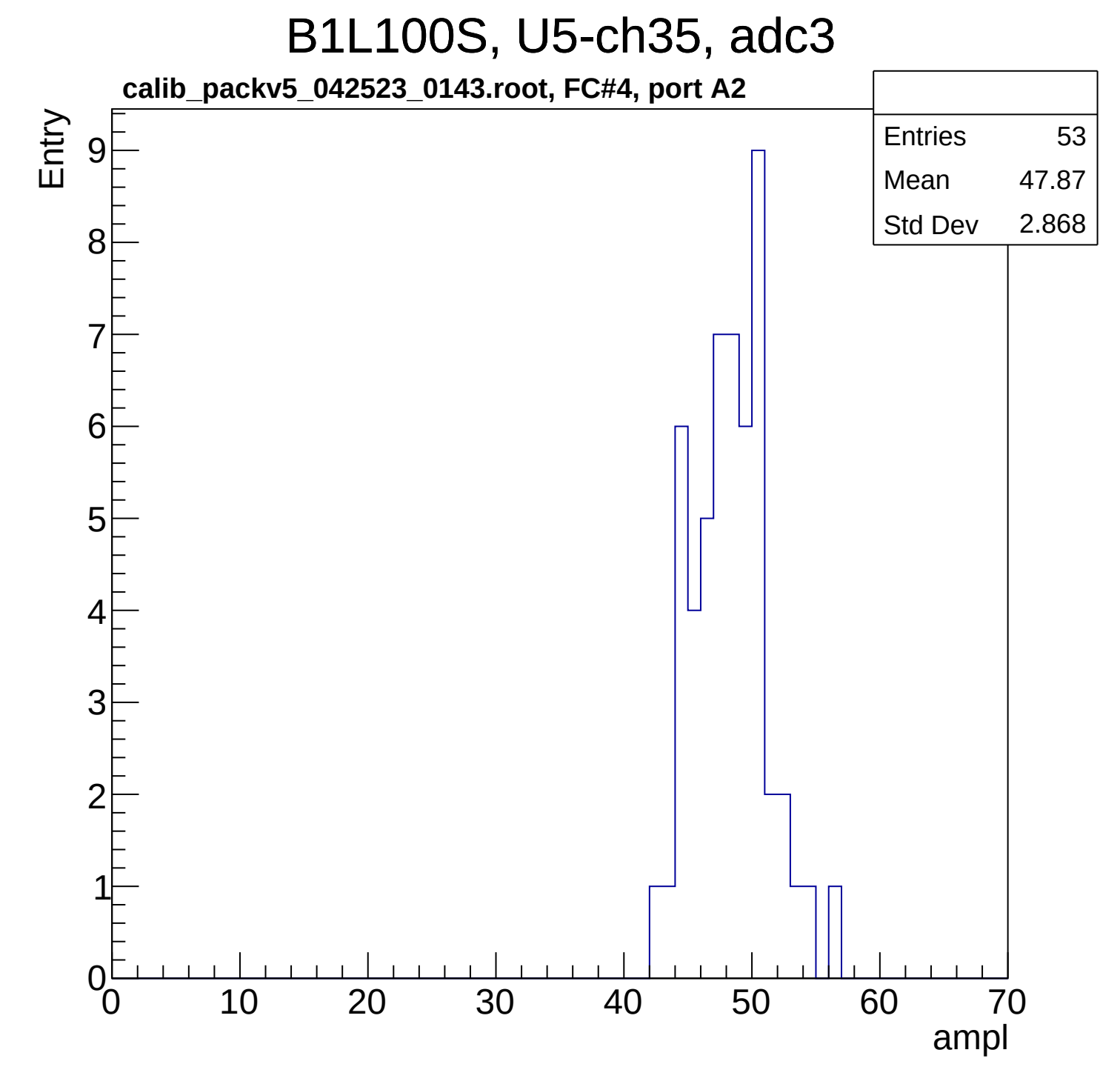
B1L100S, U5-ch35, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 47.87
Std Dev 2.868
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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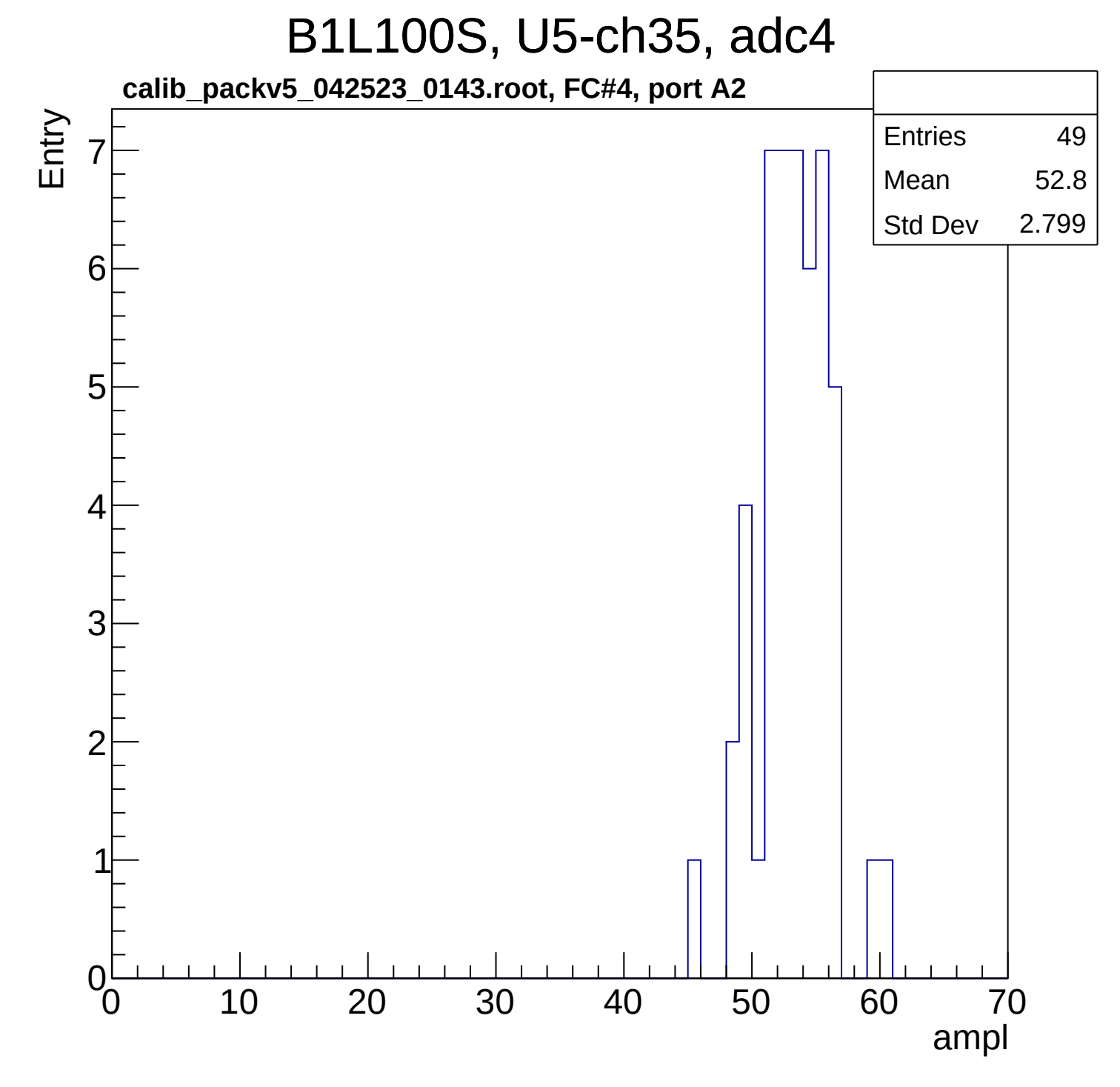
B1L100S, U5-ch35, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 49
Mean 52.8
Std Dev 2.799
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
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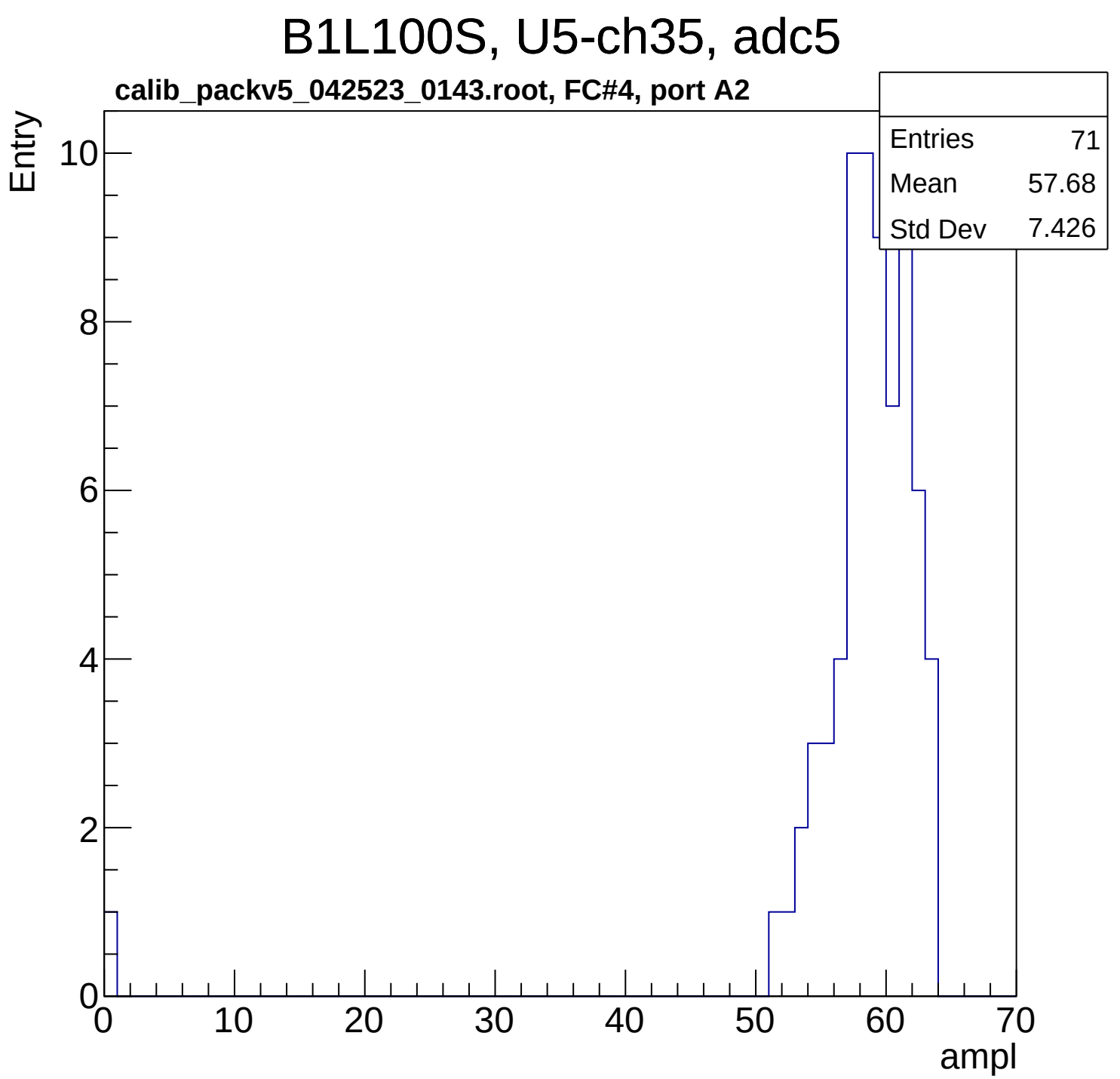
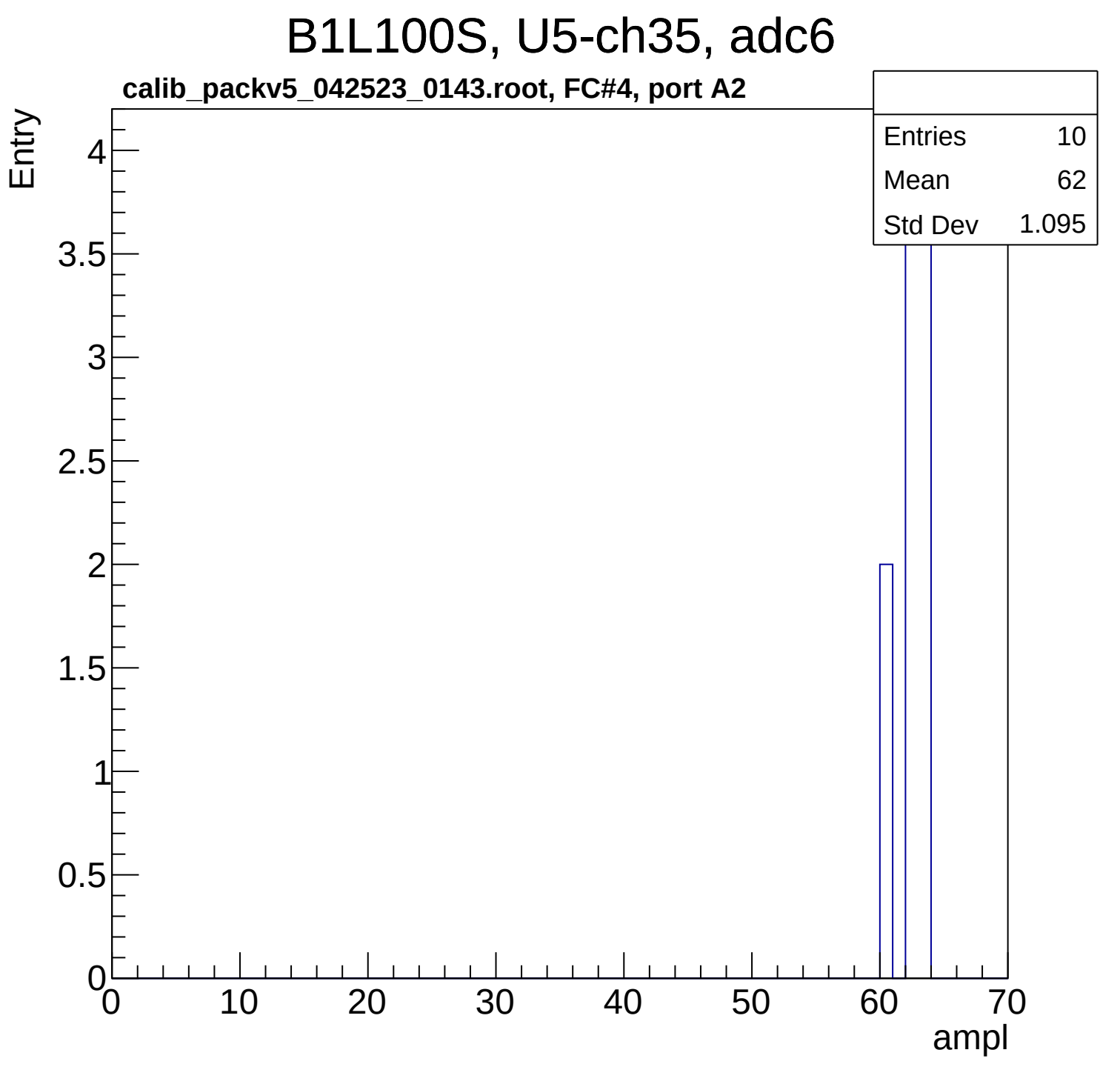
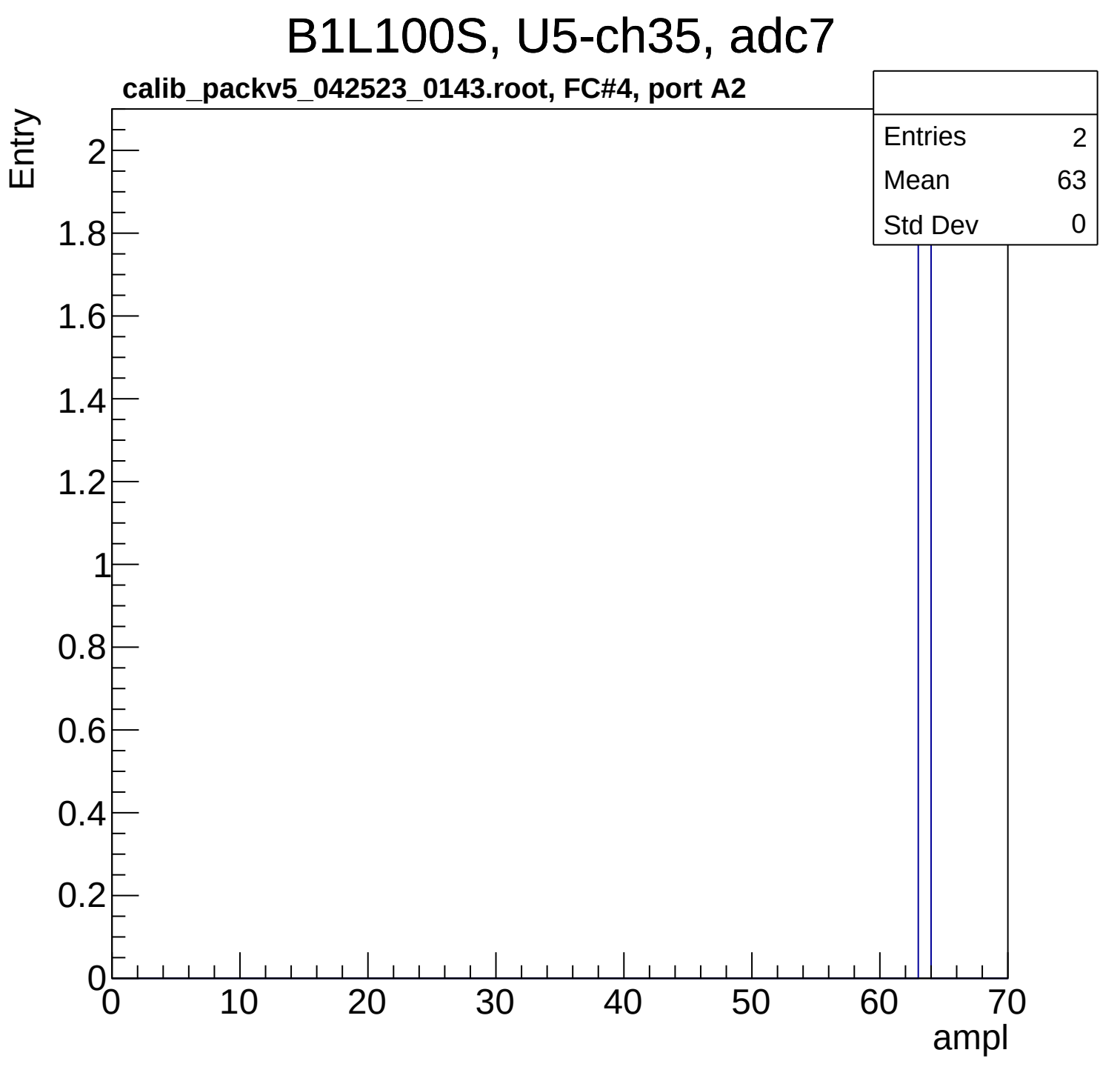
60
70


B1L100S, U5-ch35, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 57.68
Std Dev 7.426
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch35, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 10
Mean 62
Std Dev 1.095
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L100S, U5-ch35, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 63
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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20
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40
50
60
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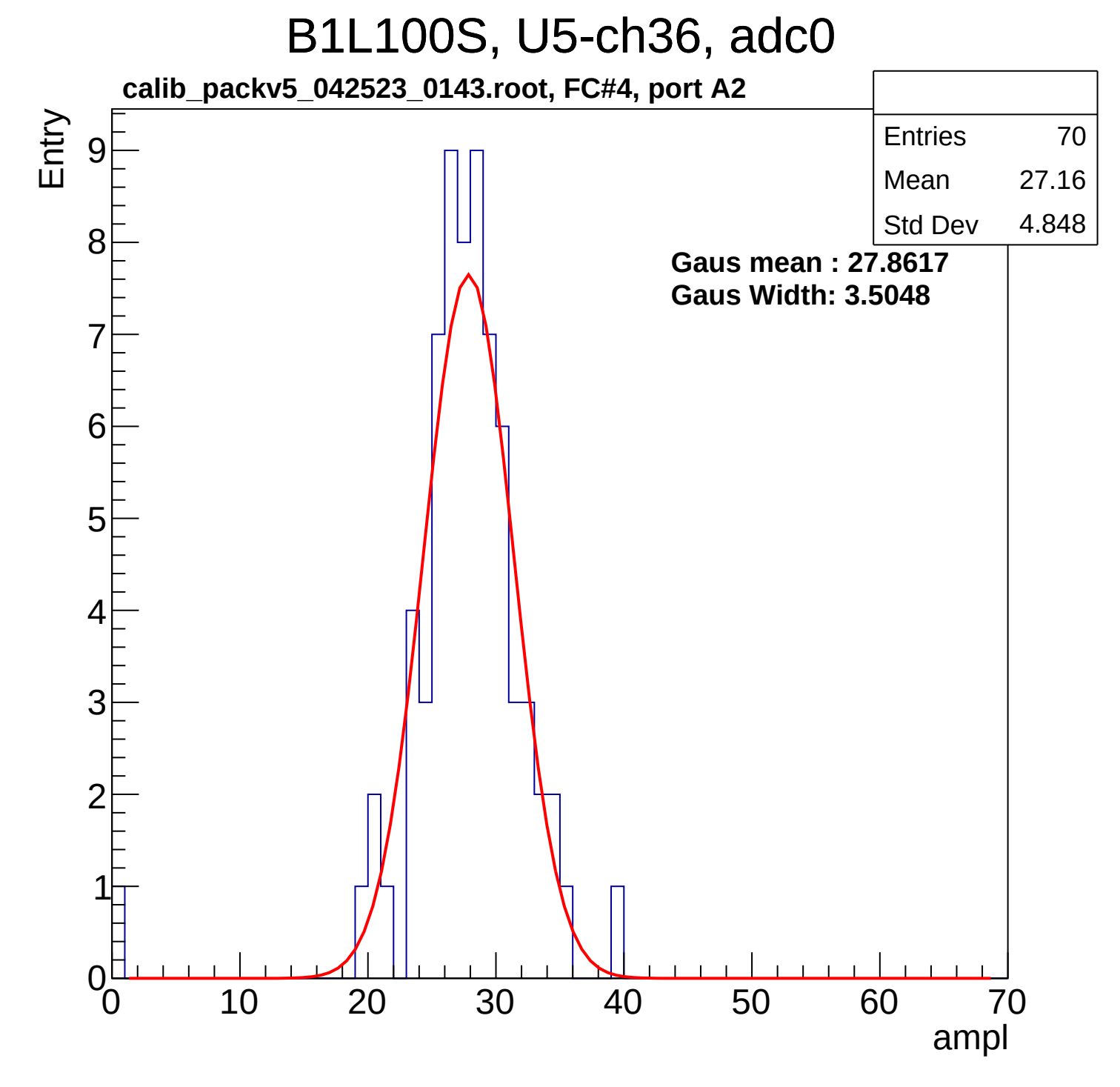
B1L100S, U5-ch36, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 27.16
Std Dev 4.848
Gaus mean : 27.8617
Gaus Width: 3.5048
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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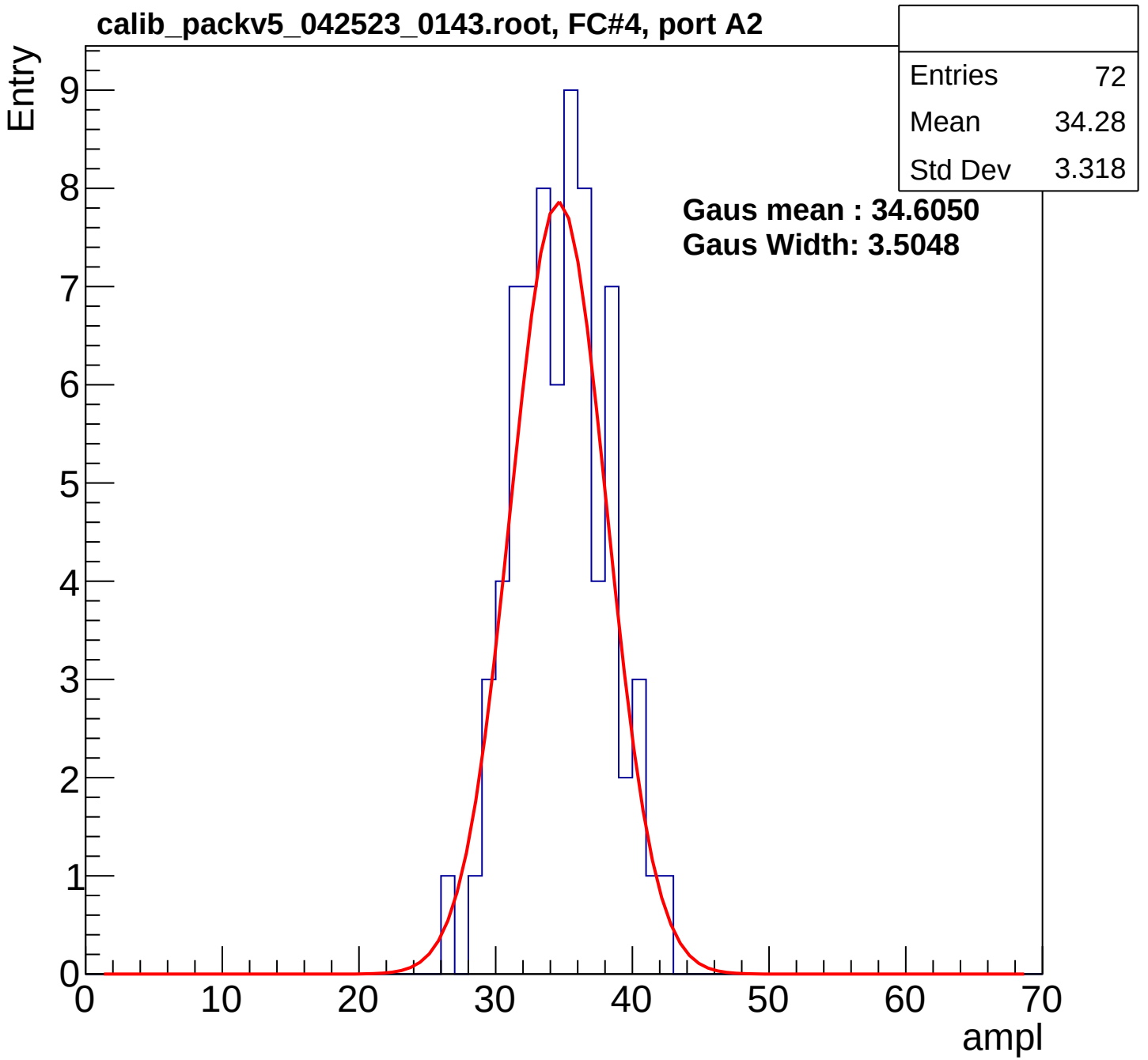
40
50
60
70


B1L100S, U5-ch36, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 34.28
Std Dev 3.318
Gaus mean : 34.6050
Gaus Width: 3.5048
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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20
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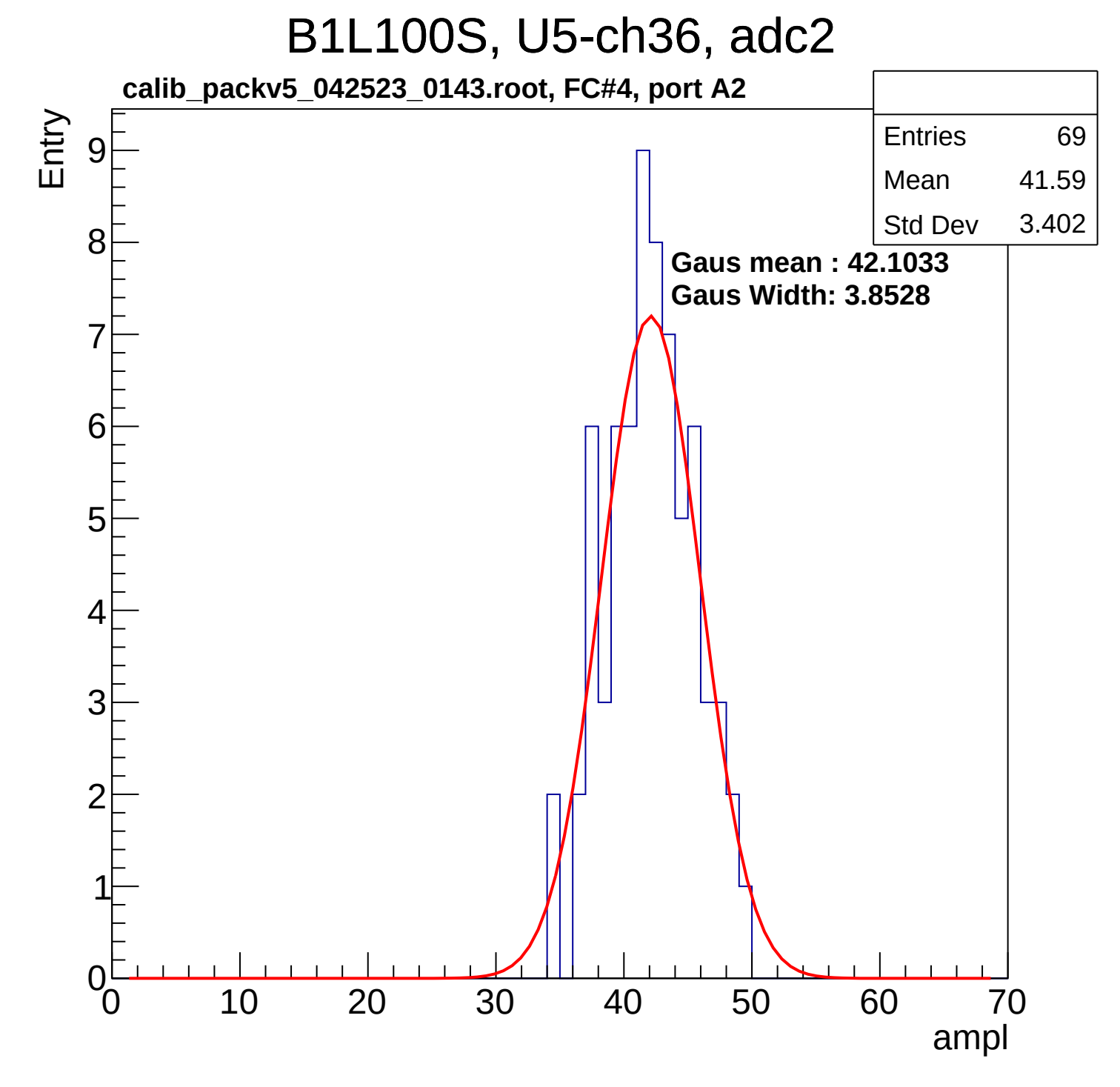
40
50
60
70


B1L100S, U5-ch36, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 41.59
Std Dev 3.402
Gaus mean : 42.1033
Gaus Width: 3.8528
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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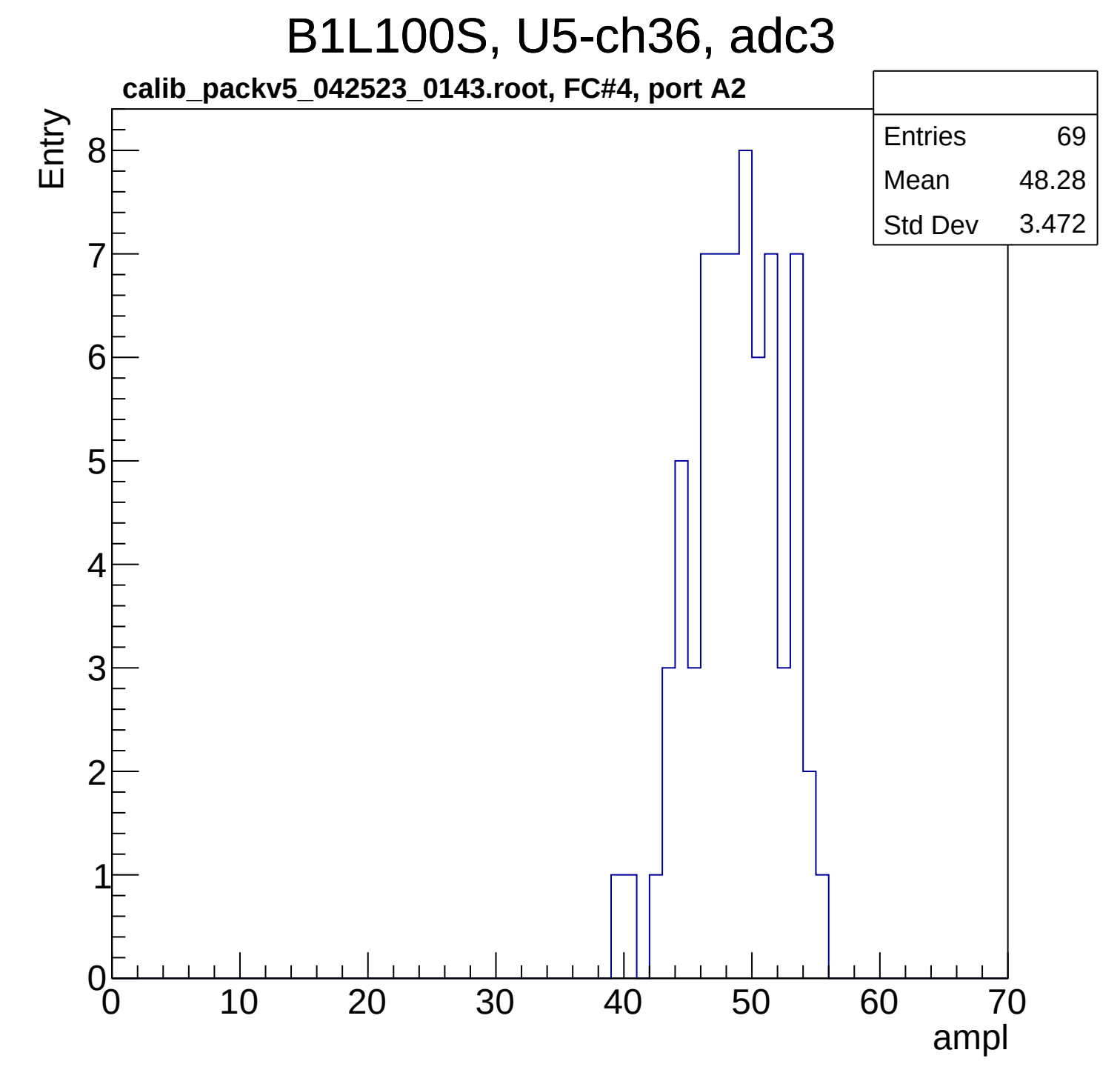
B1L100S, U5-ch36, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 48.28
Std Dev 3.472
Entry
ampl
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5
6
7
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0
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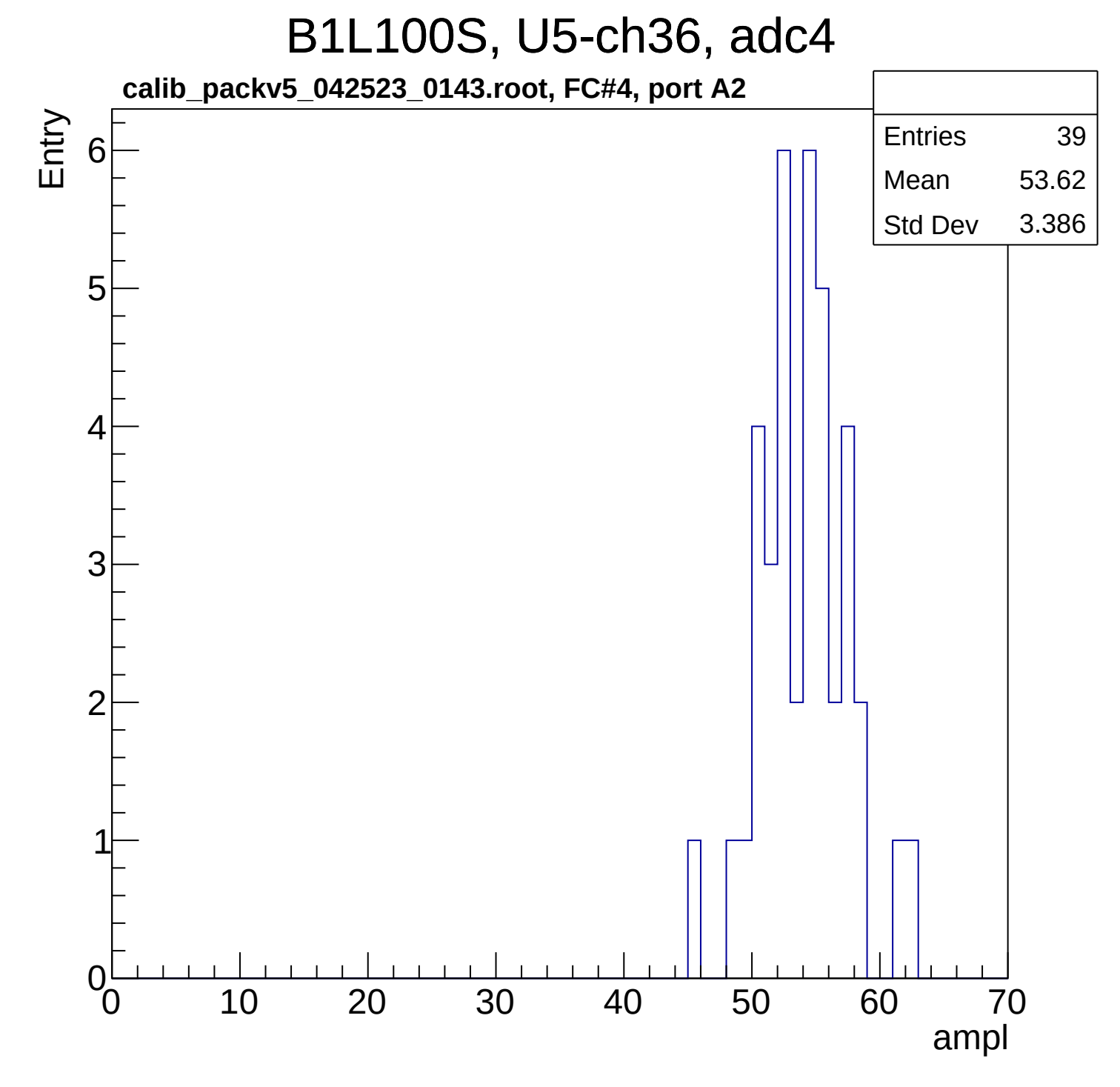
B1L100S, U5-ch36, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 39
Mean 53.62
Std Dev 3.386
Entry
ampl
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3
4
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0
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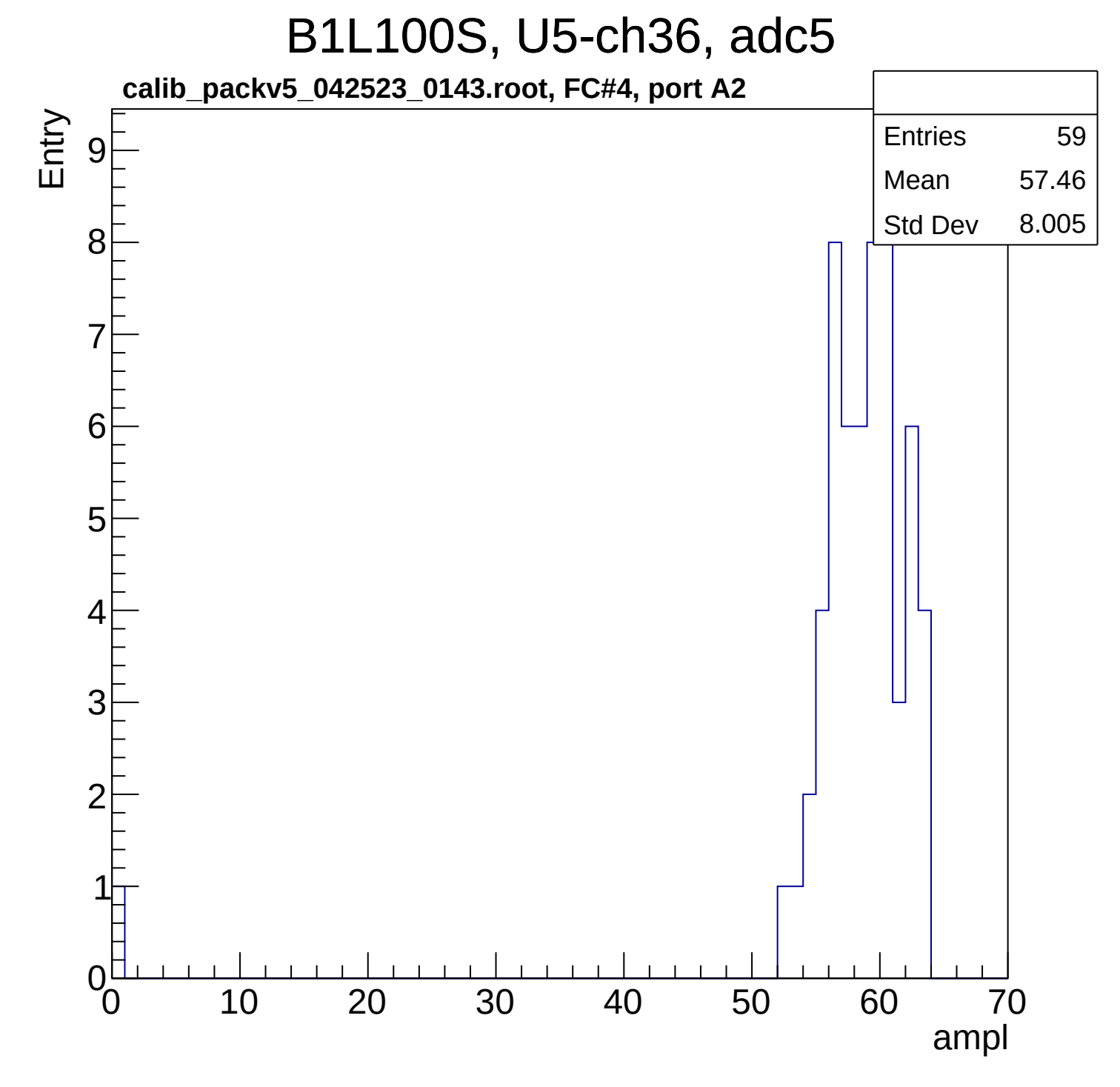
B1L100S, U5-ch36, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 57.46
Std Dev 8.005
Entry
ampl
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2
3
4
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6
7
8
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0
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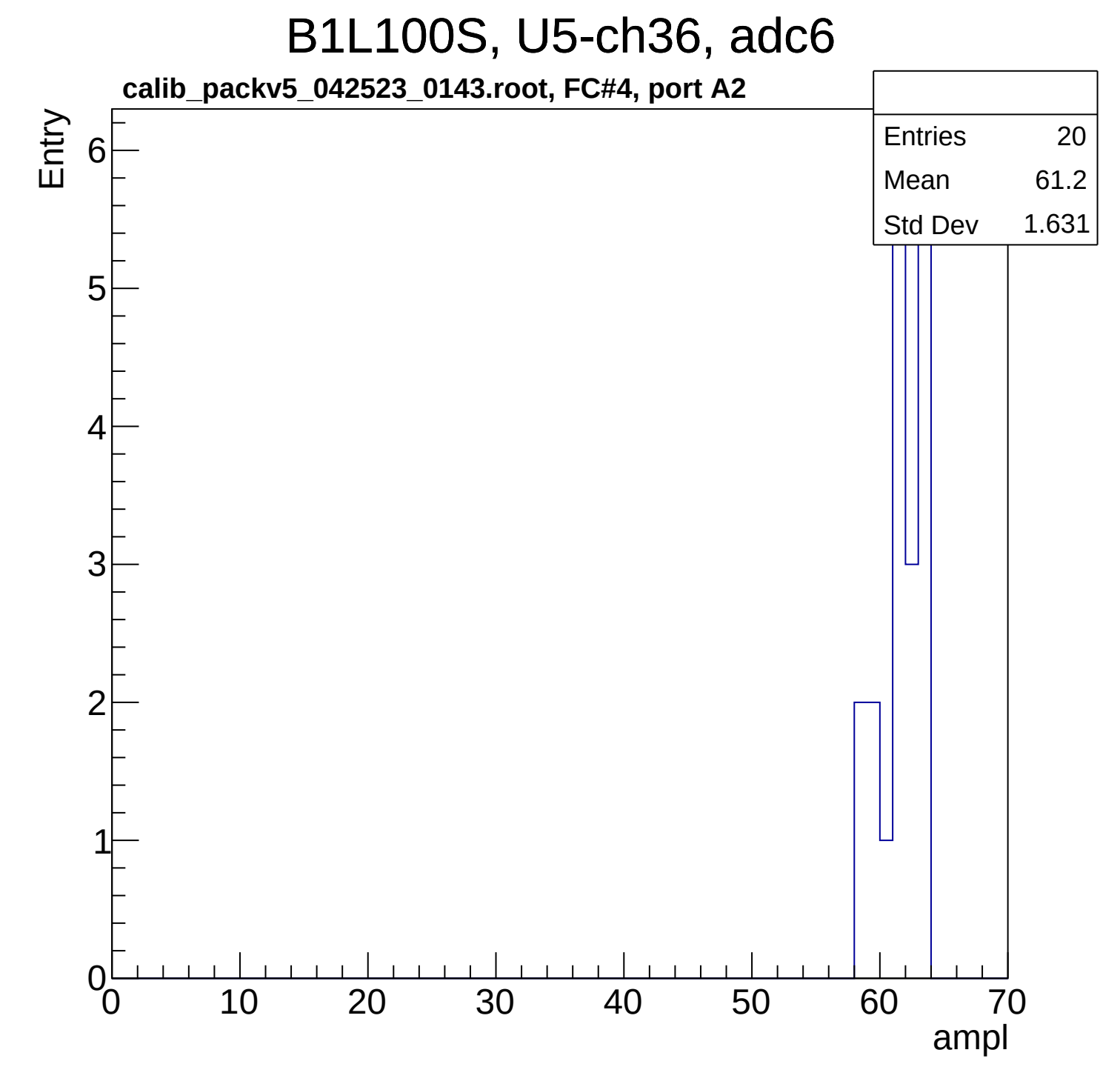
B1L100S, U5-ch36, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 20
Mean 61.2
Std Dev 1.631
Entry
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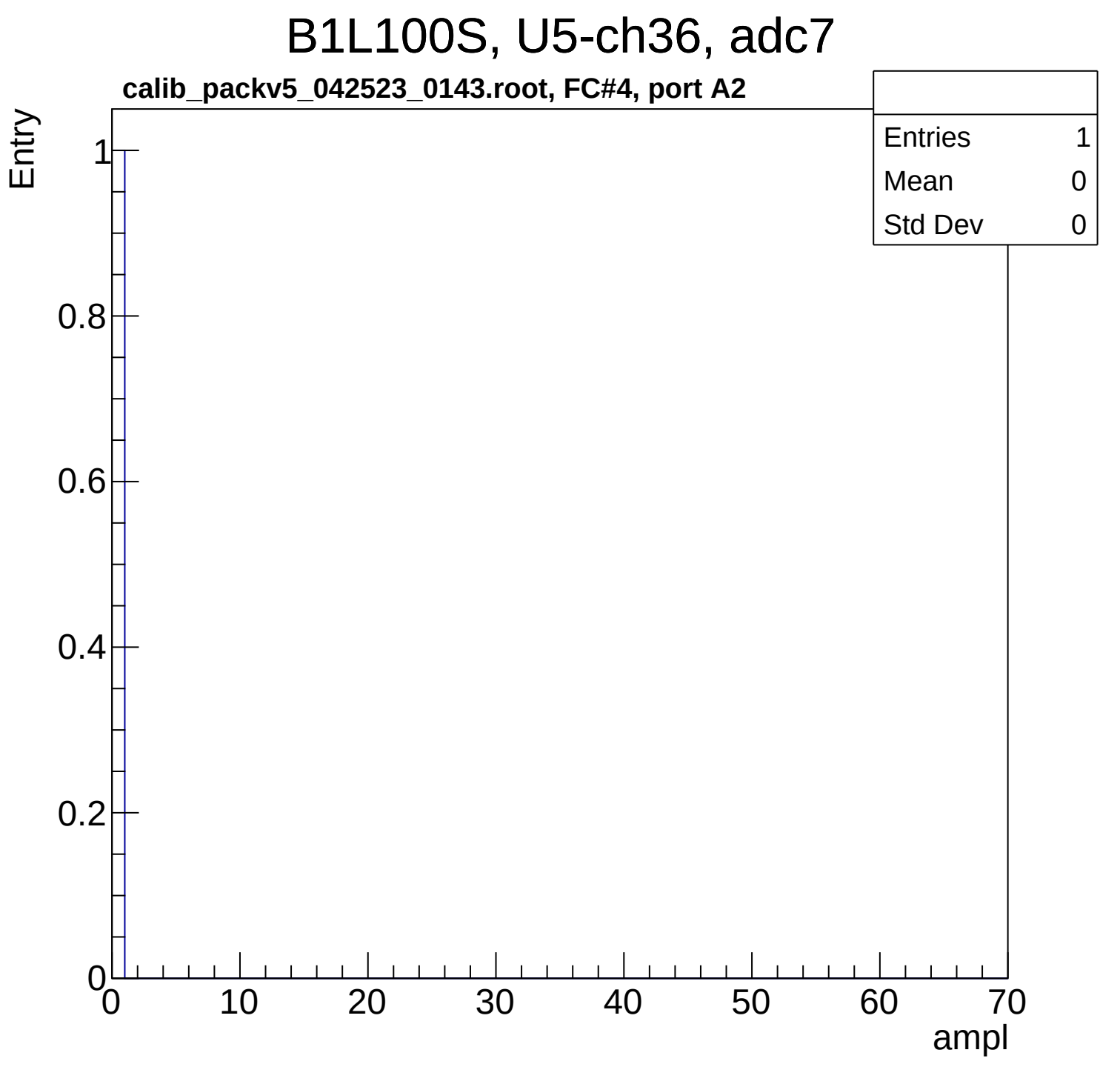
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch36, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
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0.6
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10
20
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50
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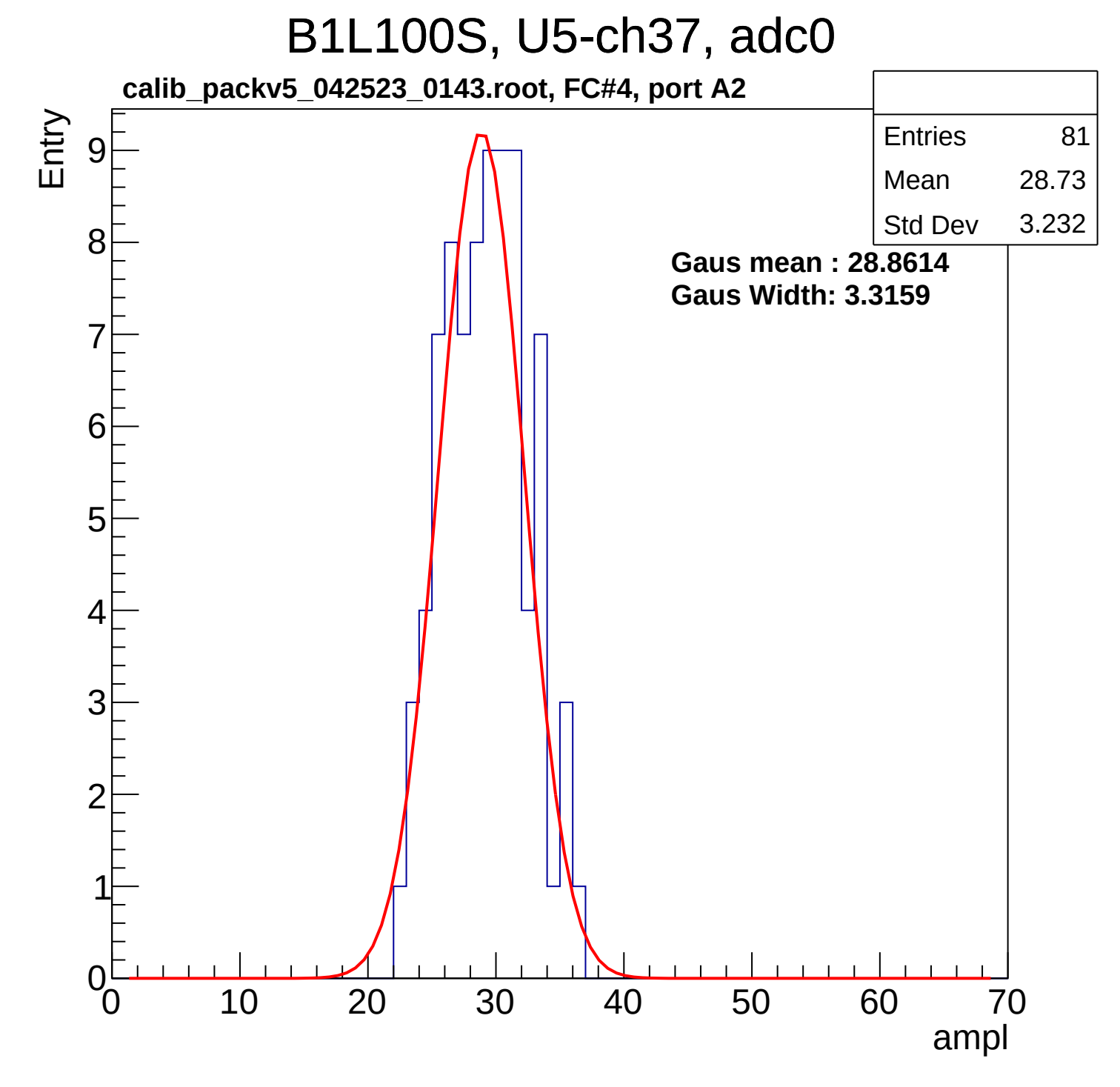
70
ampl


B1L100S, U5-ch37, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 81
Mean 28.73
Std Dev 3.232
Gaus mean : 28.8614
Gaus Width: 3.3159
Entry
ampl
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2
3
4
5
6
7
8
9
0
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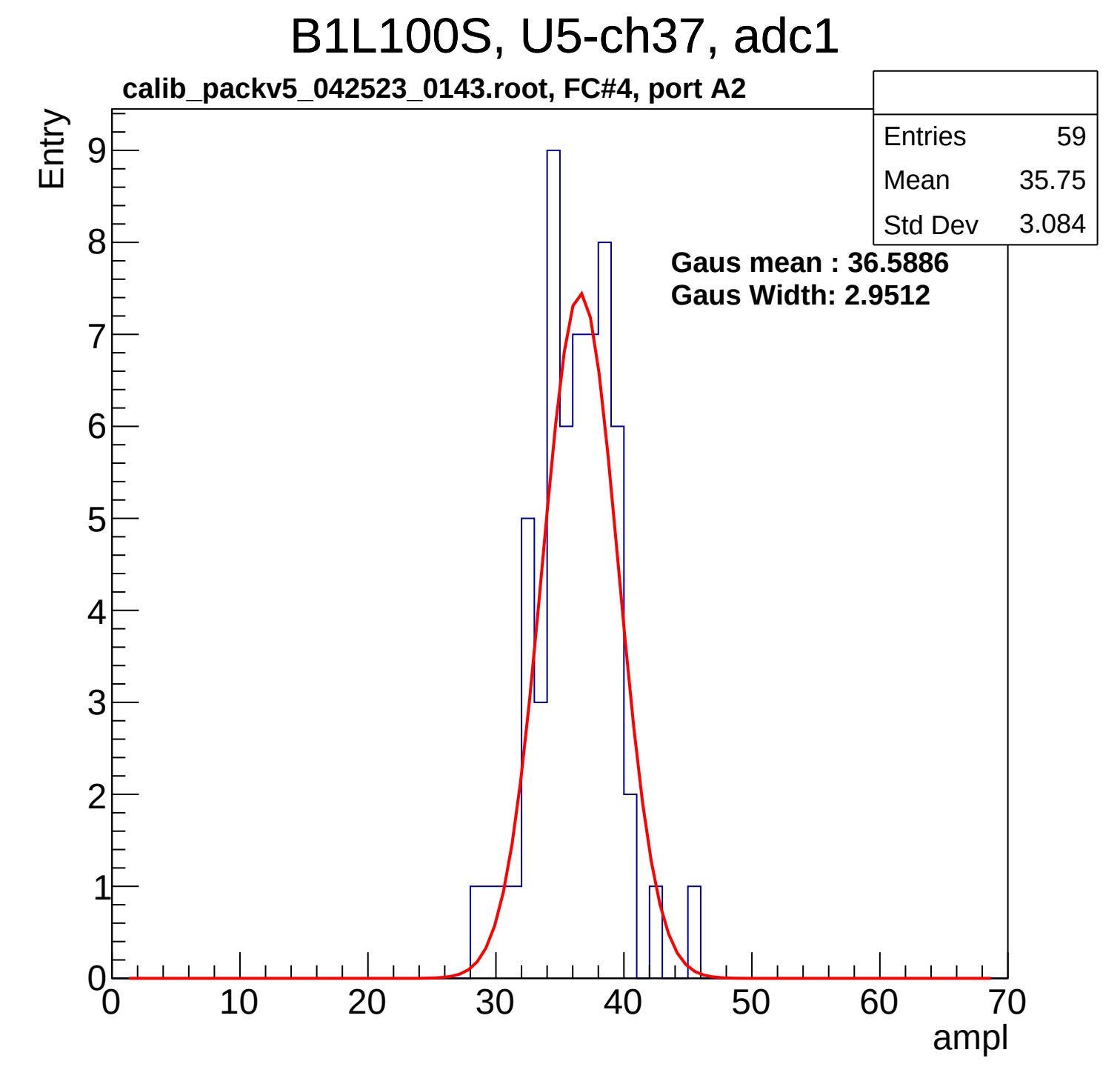
B1L100S, U5-ch37, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 35.75
Std Dev 3.084
Gaus mean : 36.5886
Gaus Width: 2.9512
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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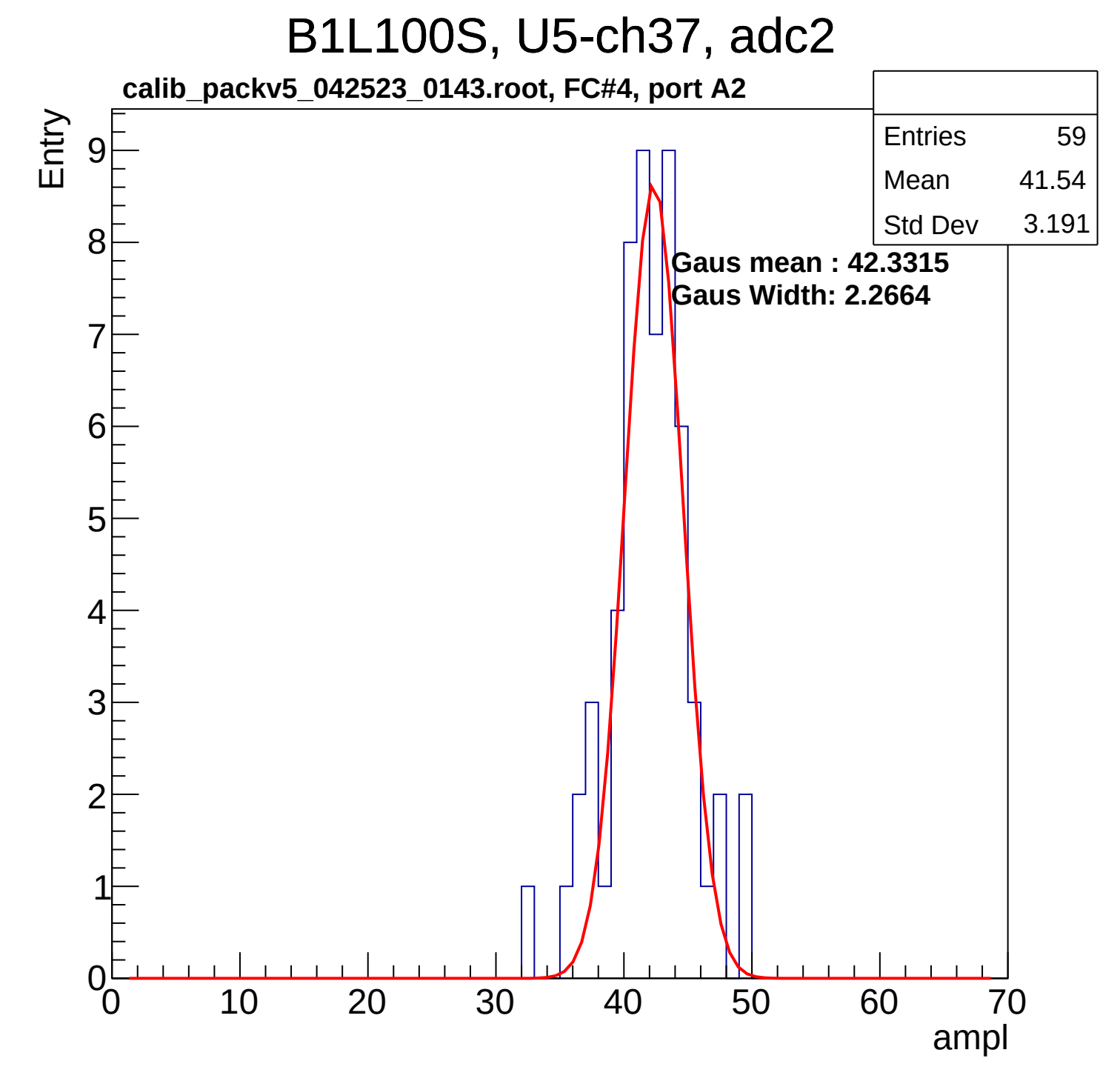
30
40
50
60
70


B1L100S, U5-ch37, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 41.54
Std Dev 3.191
Gaus mean : 42.3315
Gaus Width: 2.2664
Entry
ampl
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10
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30
40
50
60
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1
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3
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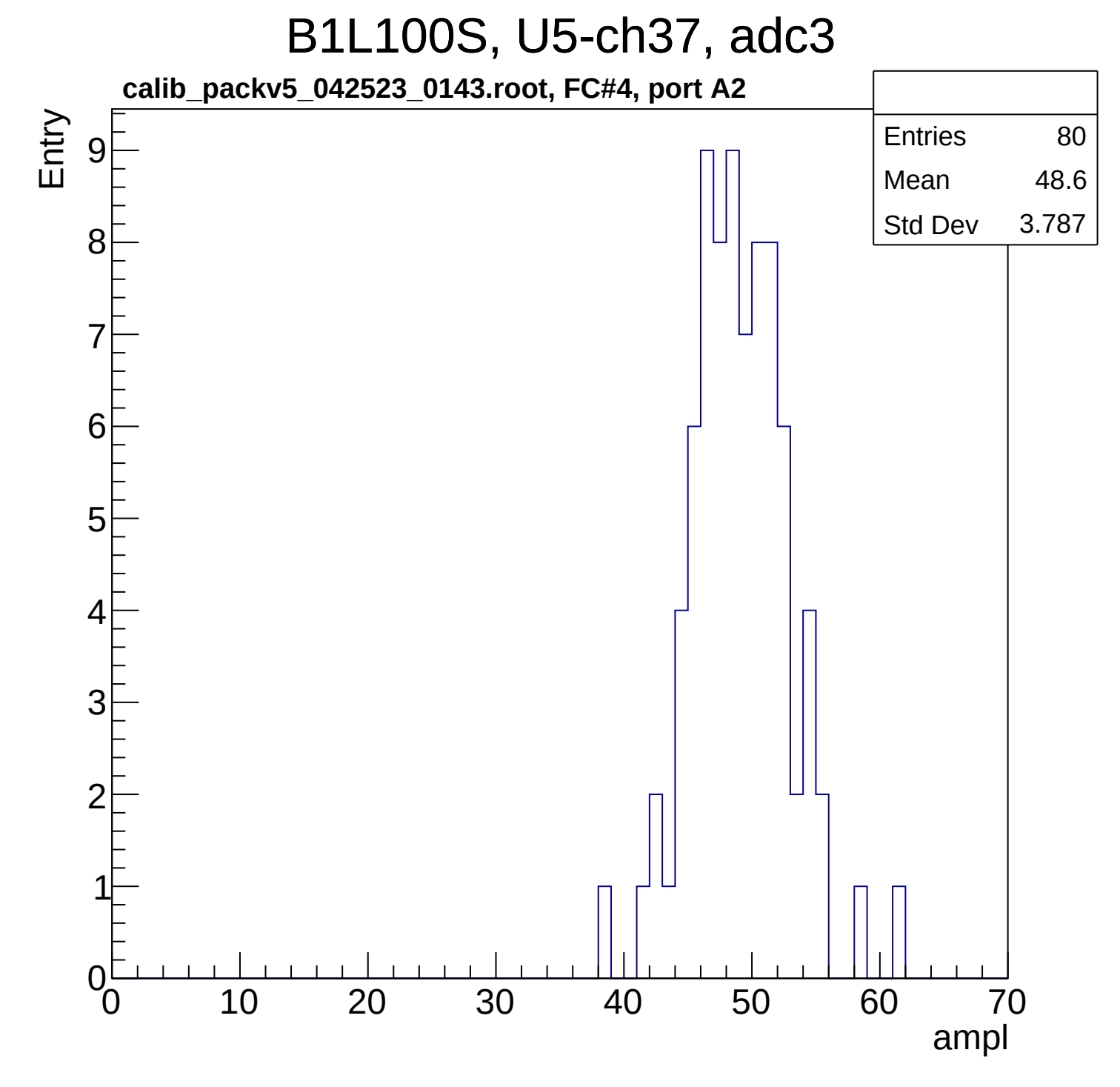
6
7
8
9


B1L100S, U5-ch37, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 80
Mean 48.6
Std Dev 3.787
Entry
ampl
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3
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5
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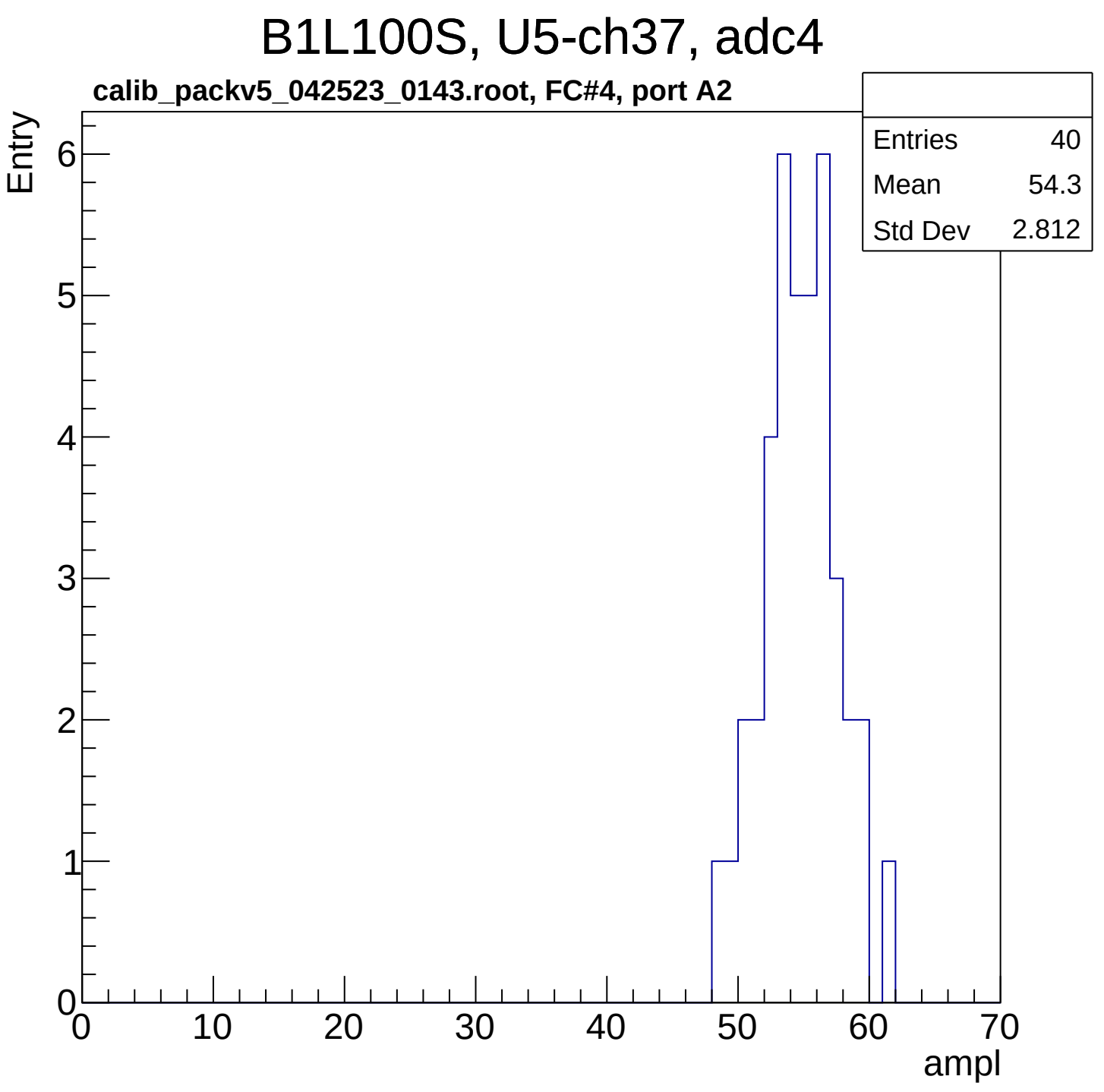
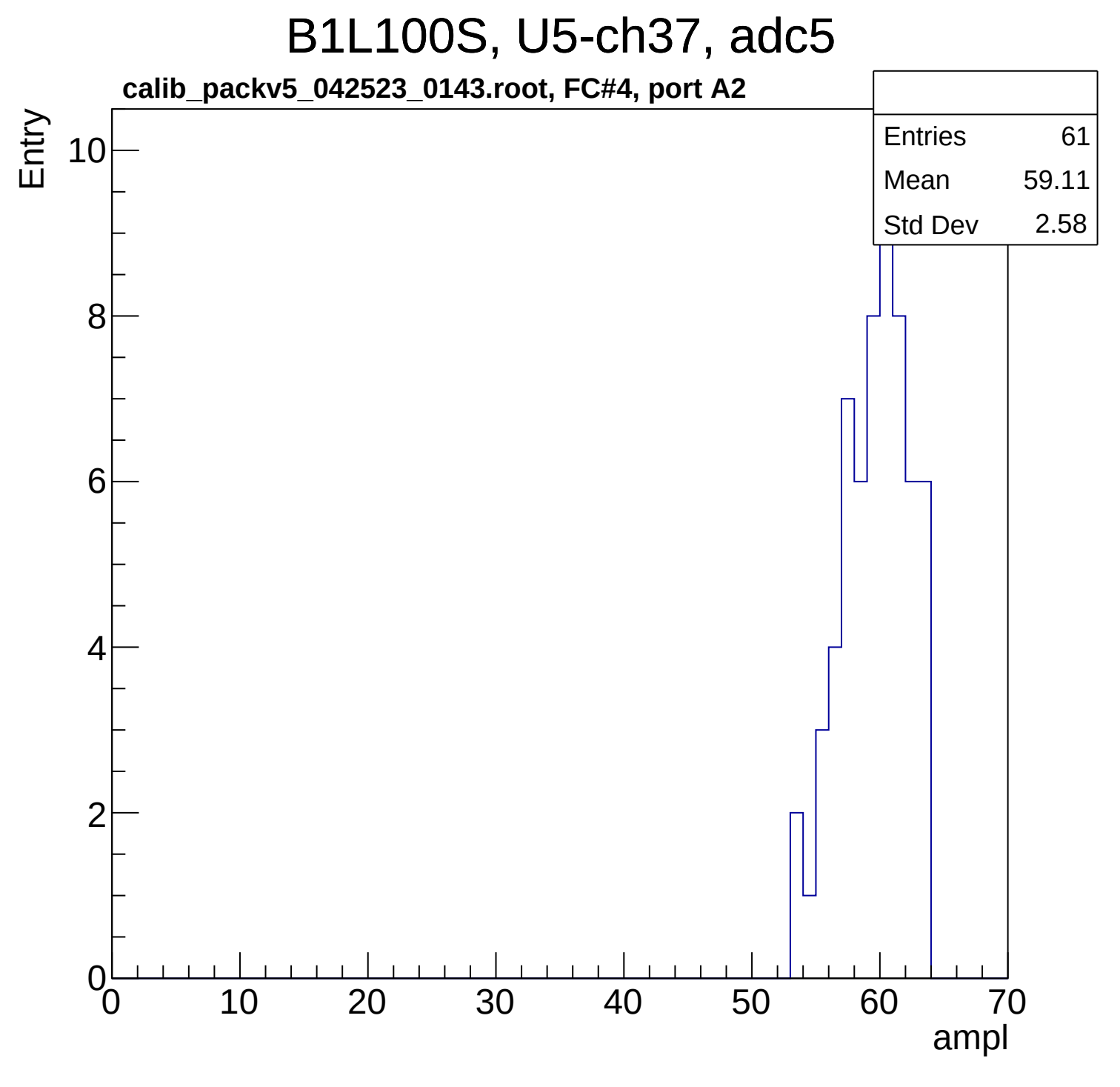
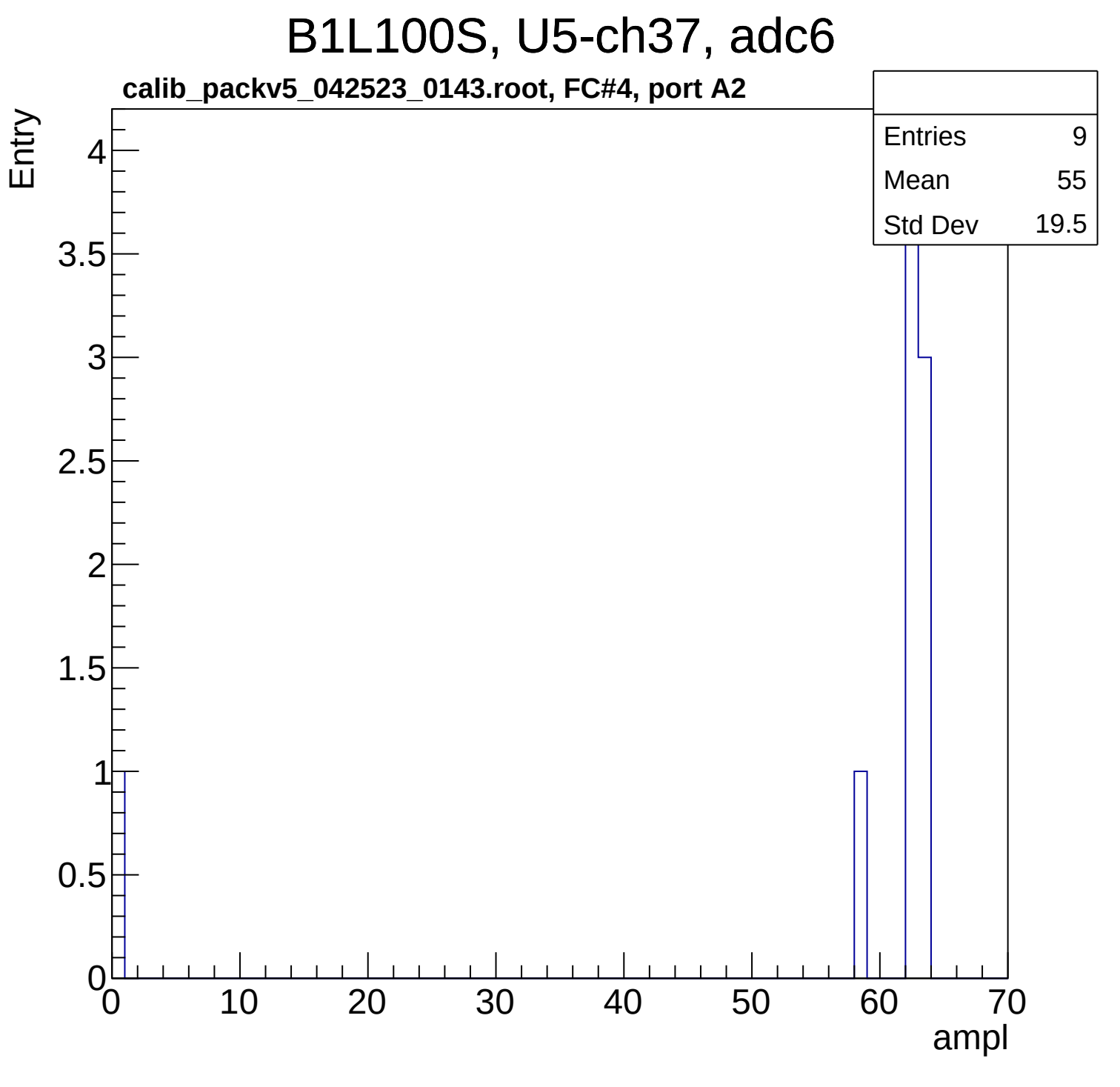
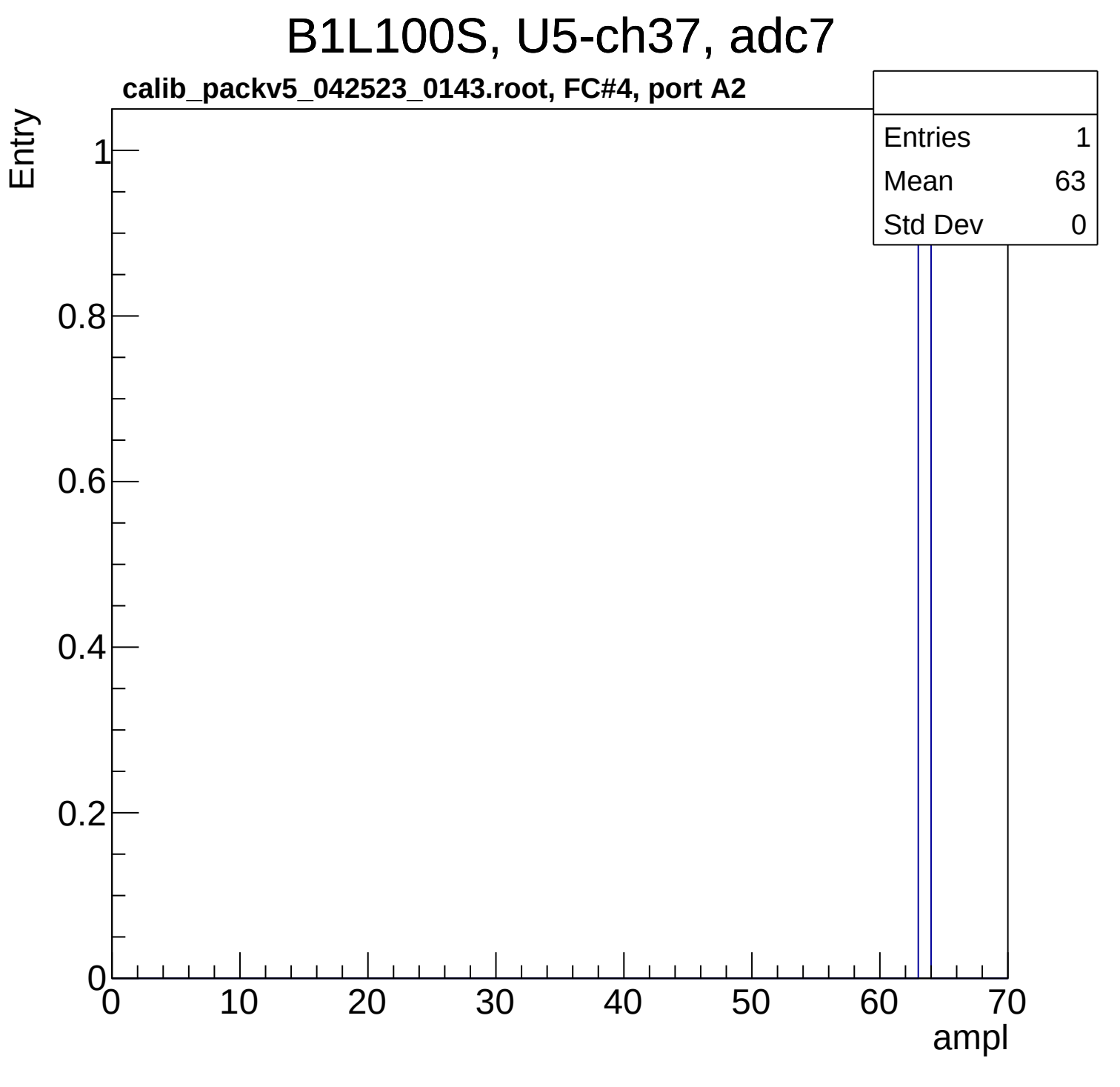
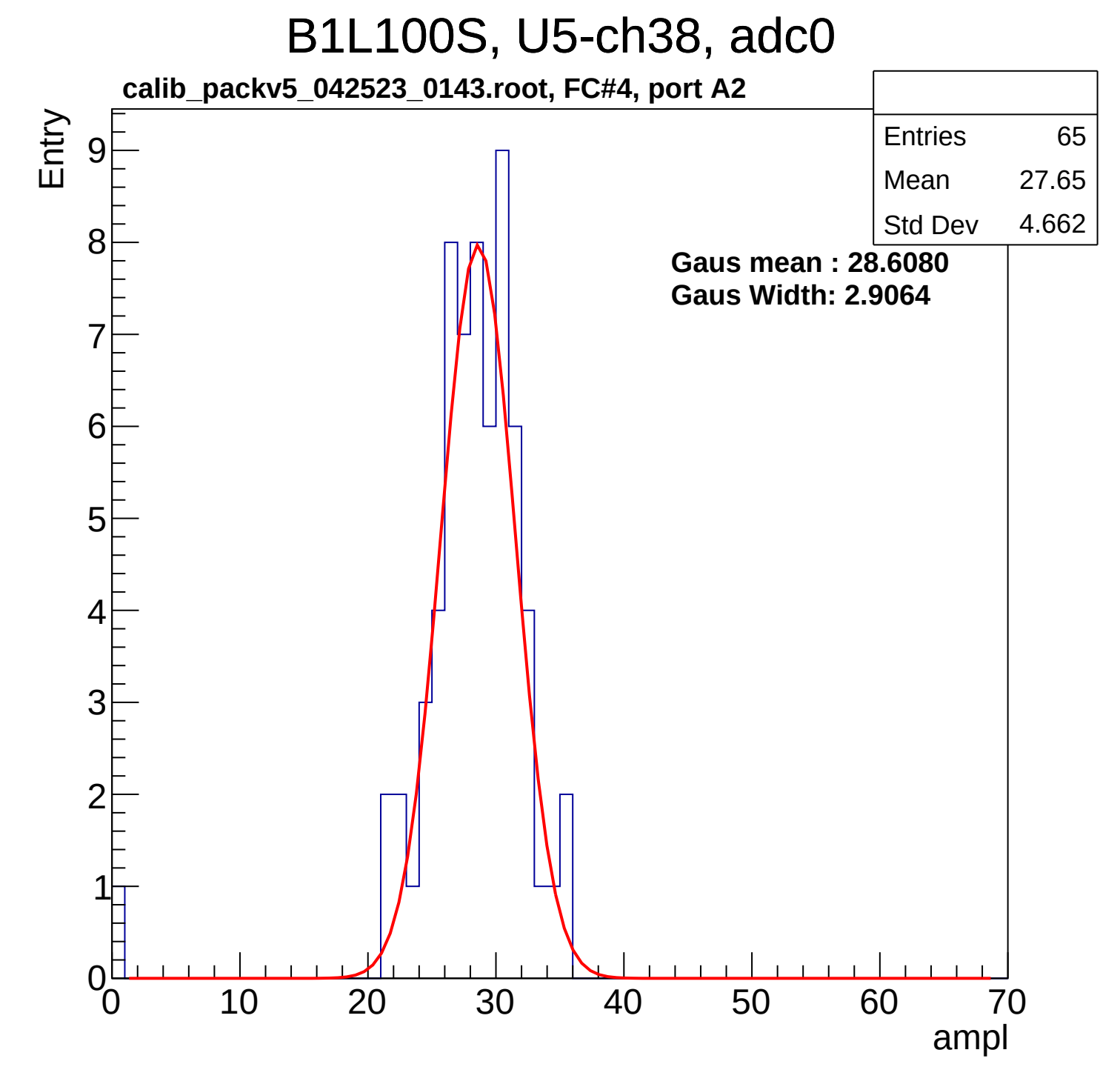
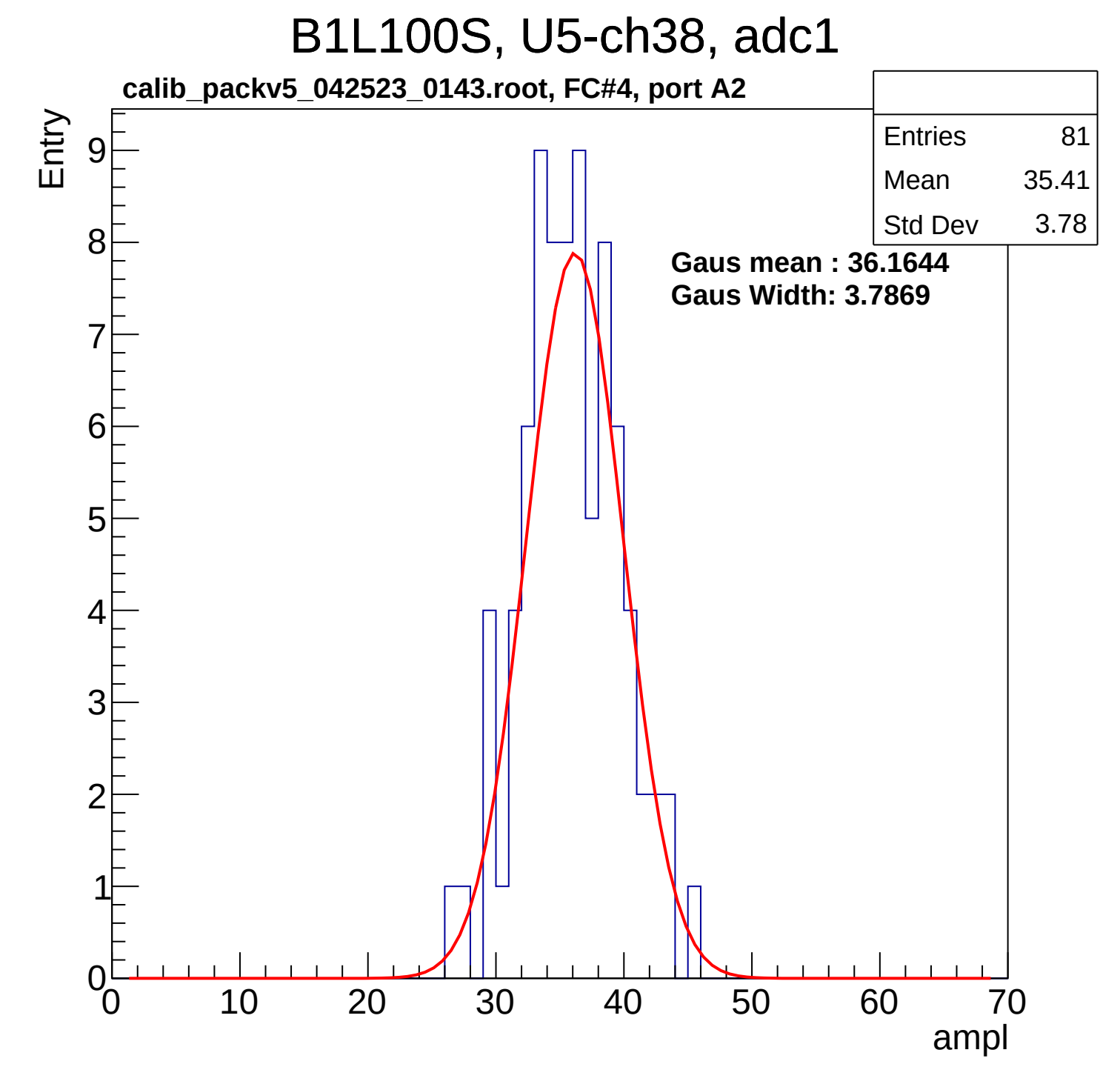

B1L100S, U5-ch37, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 40
Mean 54.3
Std Dev 2.812
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch37, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 59.11
Std Dev 2.58
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch37, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 9
Mean 55
Std Dev 19.5
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L100S, U5-ch37, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch38, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 27.65
Std Dev 4.662
Gaus mean : 28.6080
Gaus Width: 2.9064
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch38, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 81
Mean 35.41
Std Dev 3.78
Gaus mean : 36.1644
Gaus Width: 3.7869
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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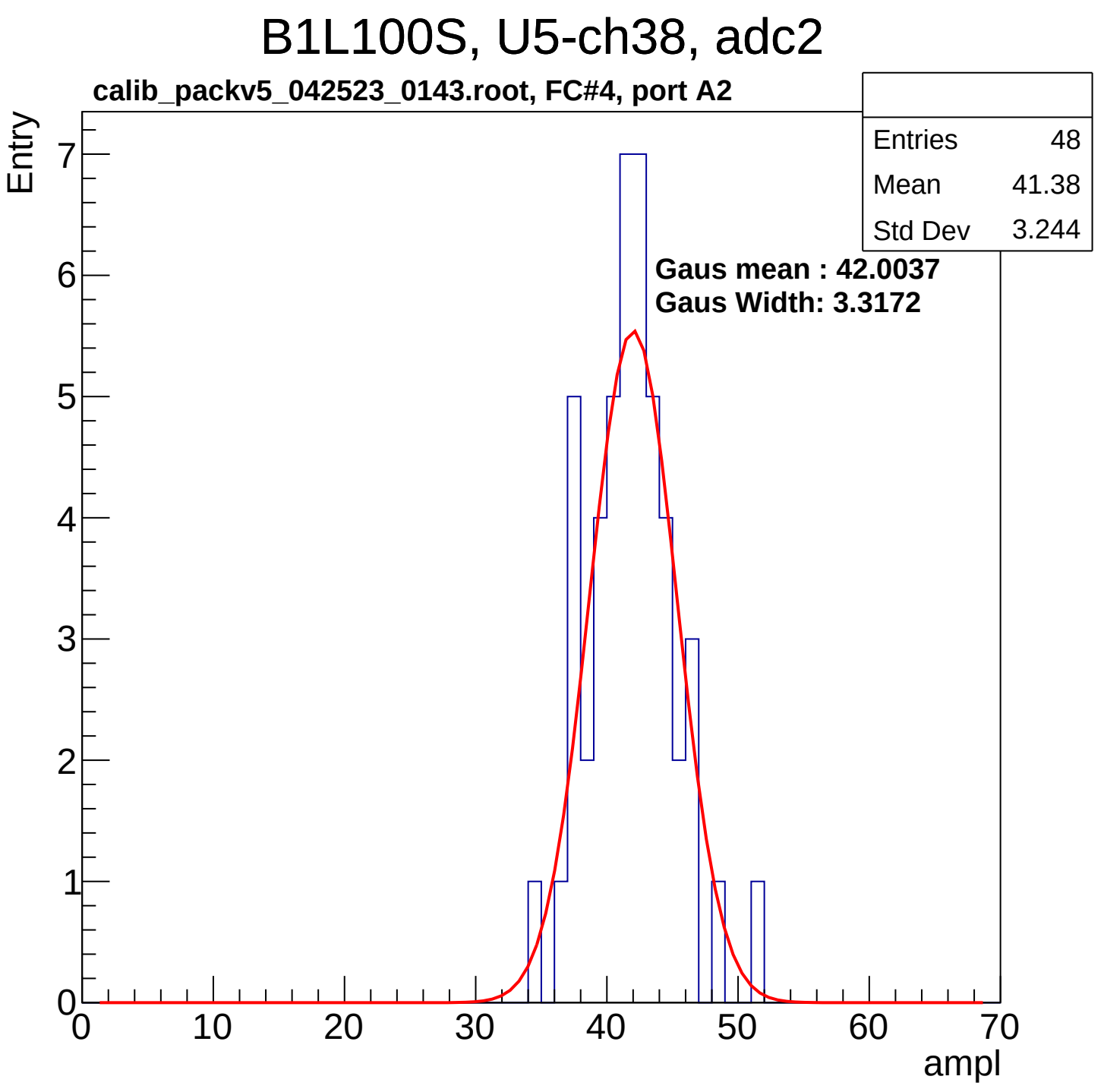
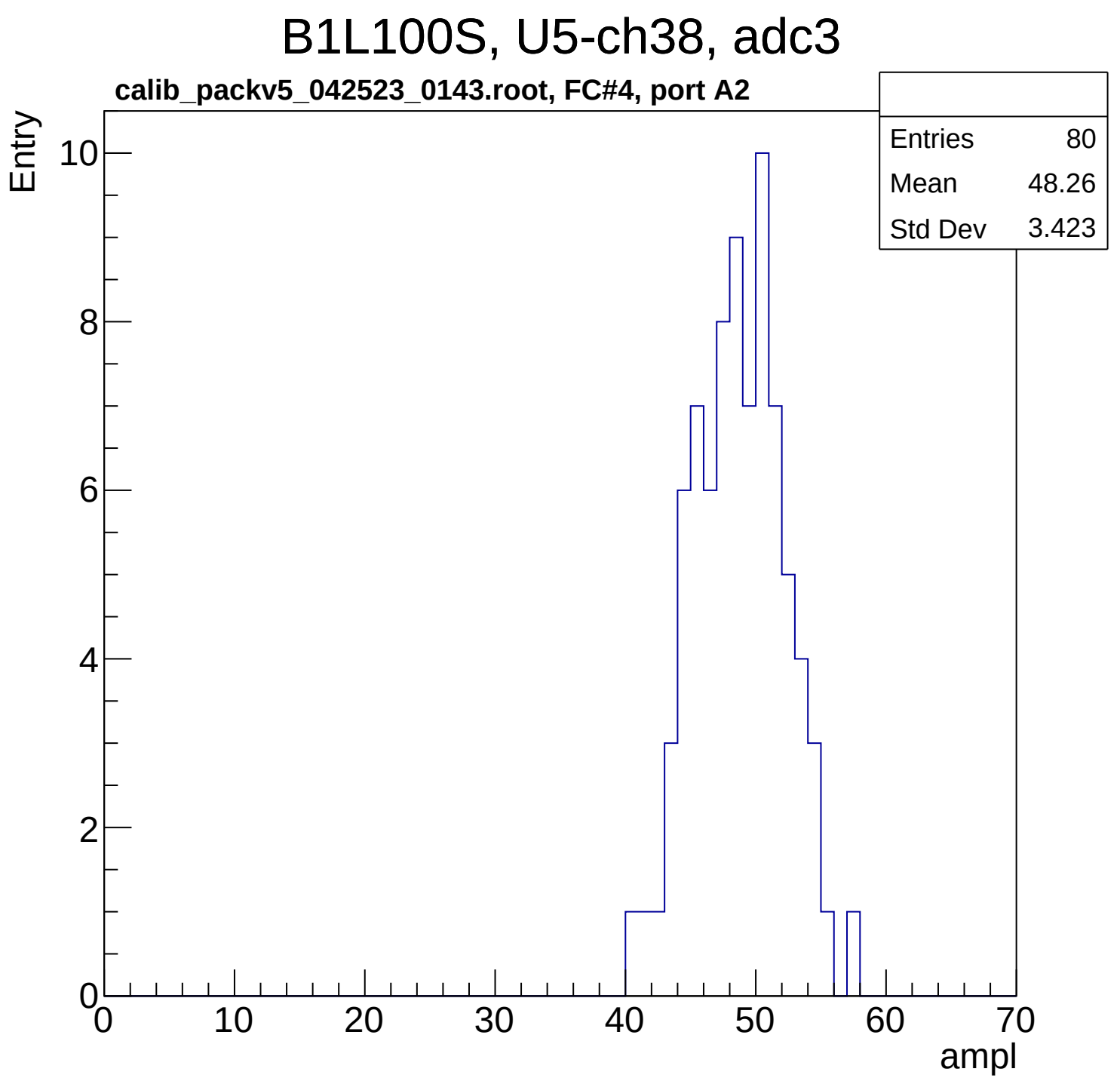
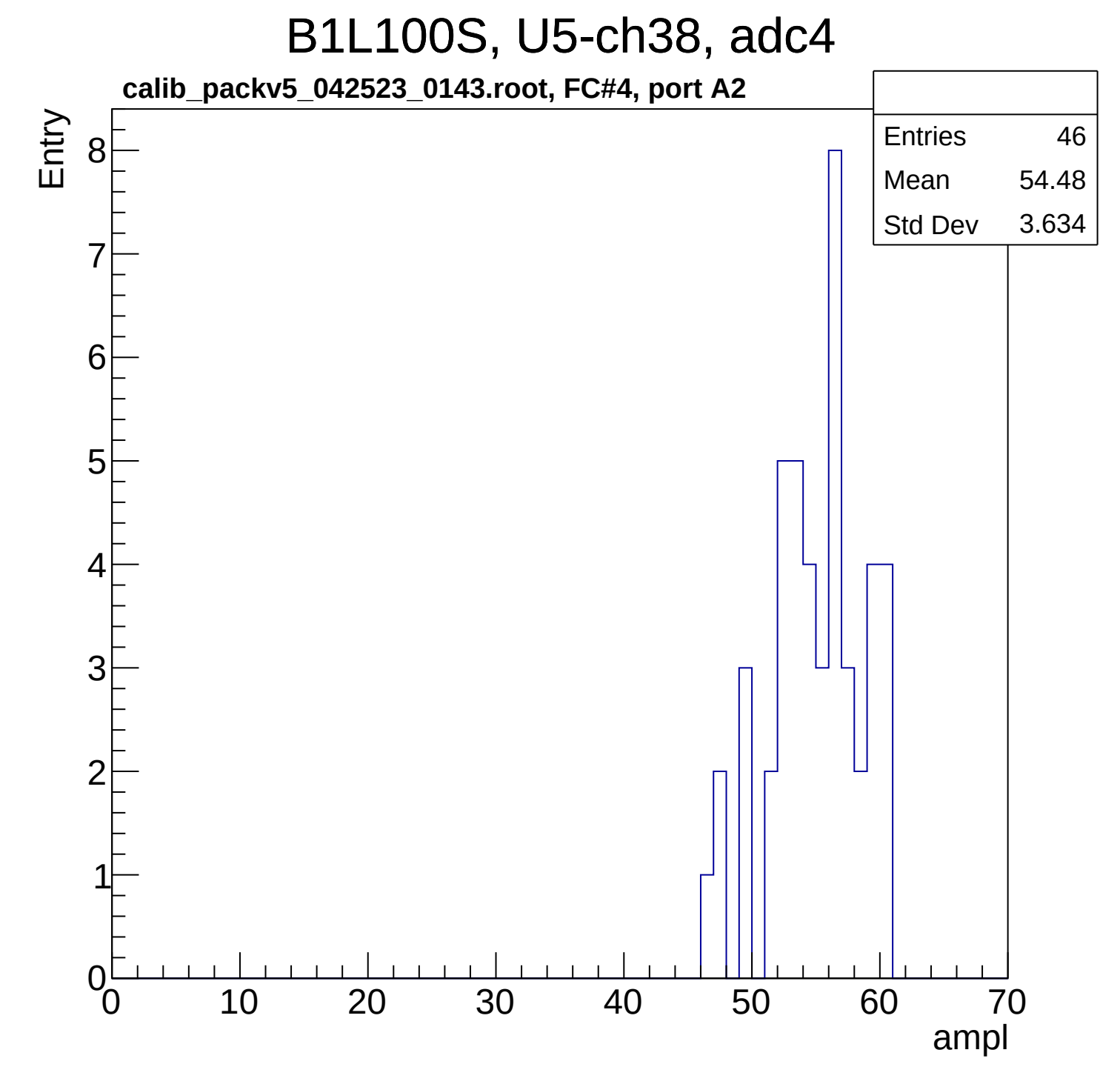
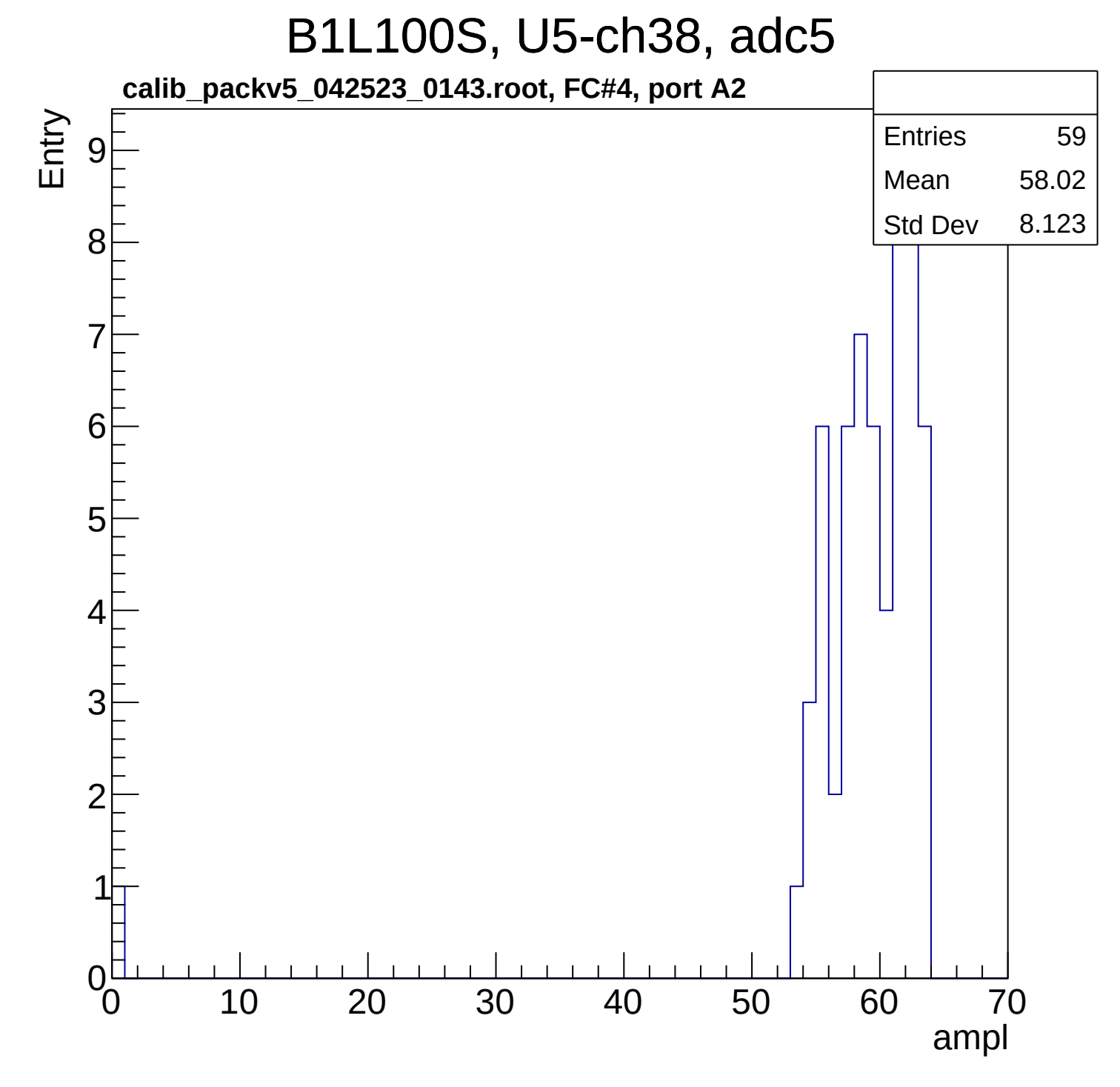
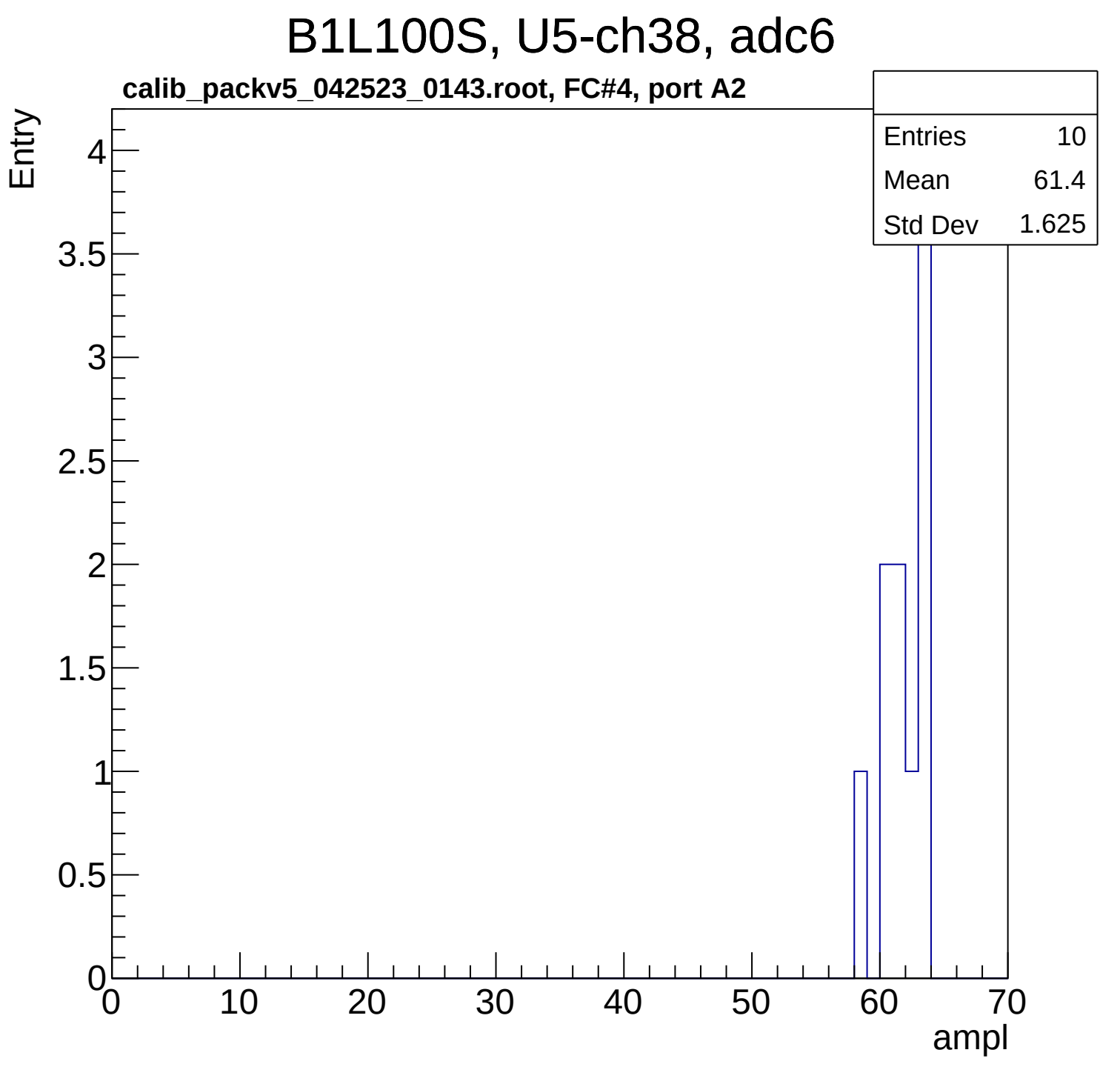
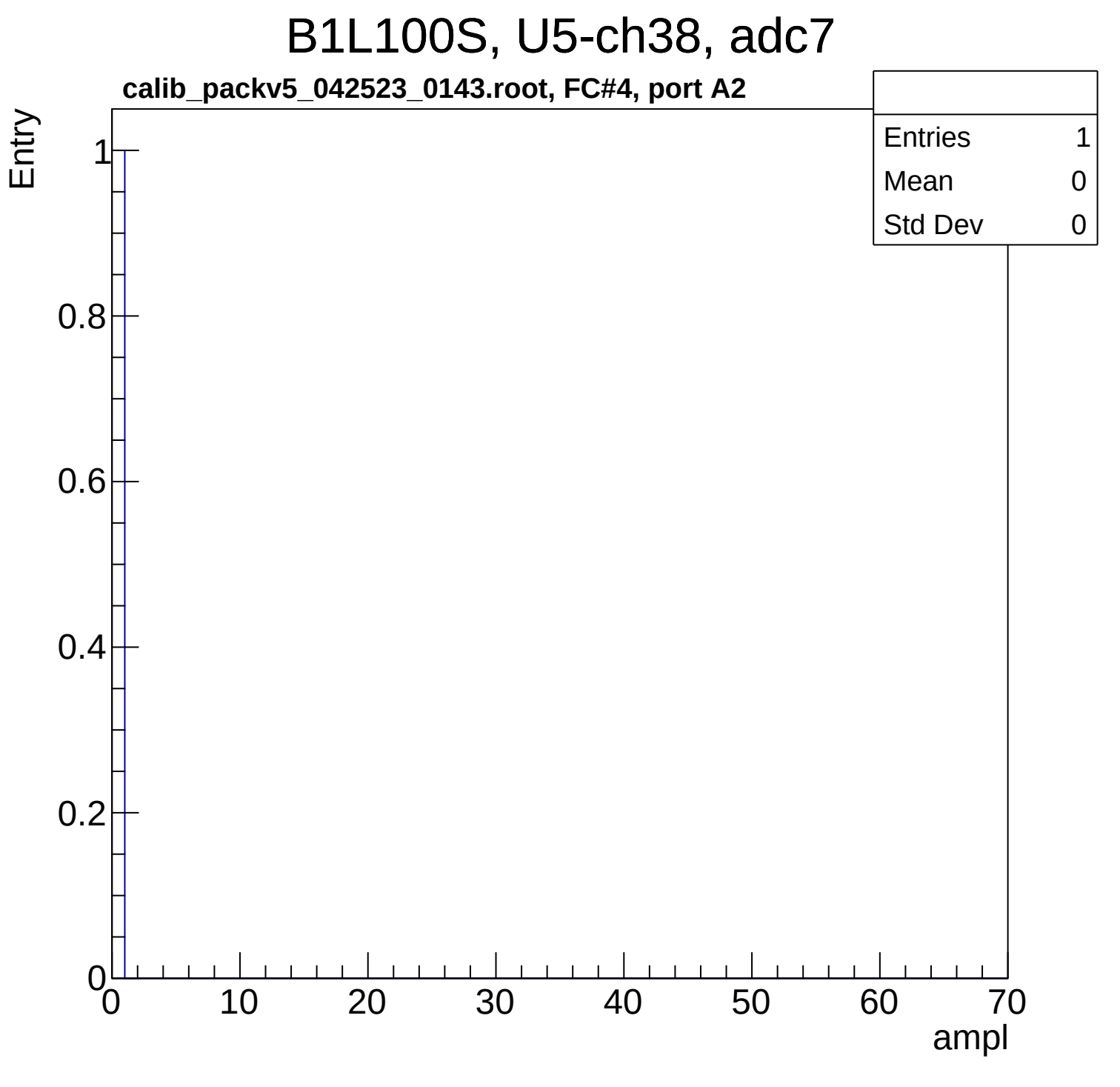

B1L100S, U5-ch38, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 48
Mean 41.38
Std Dev 3.244
Gaus mean : 42.0037
Gaus Width: 3.3172
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

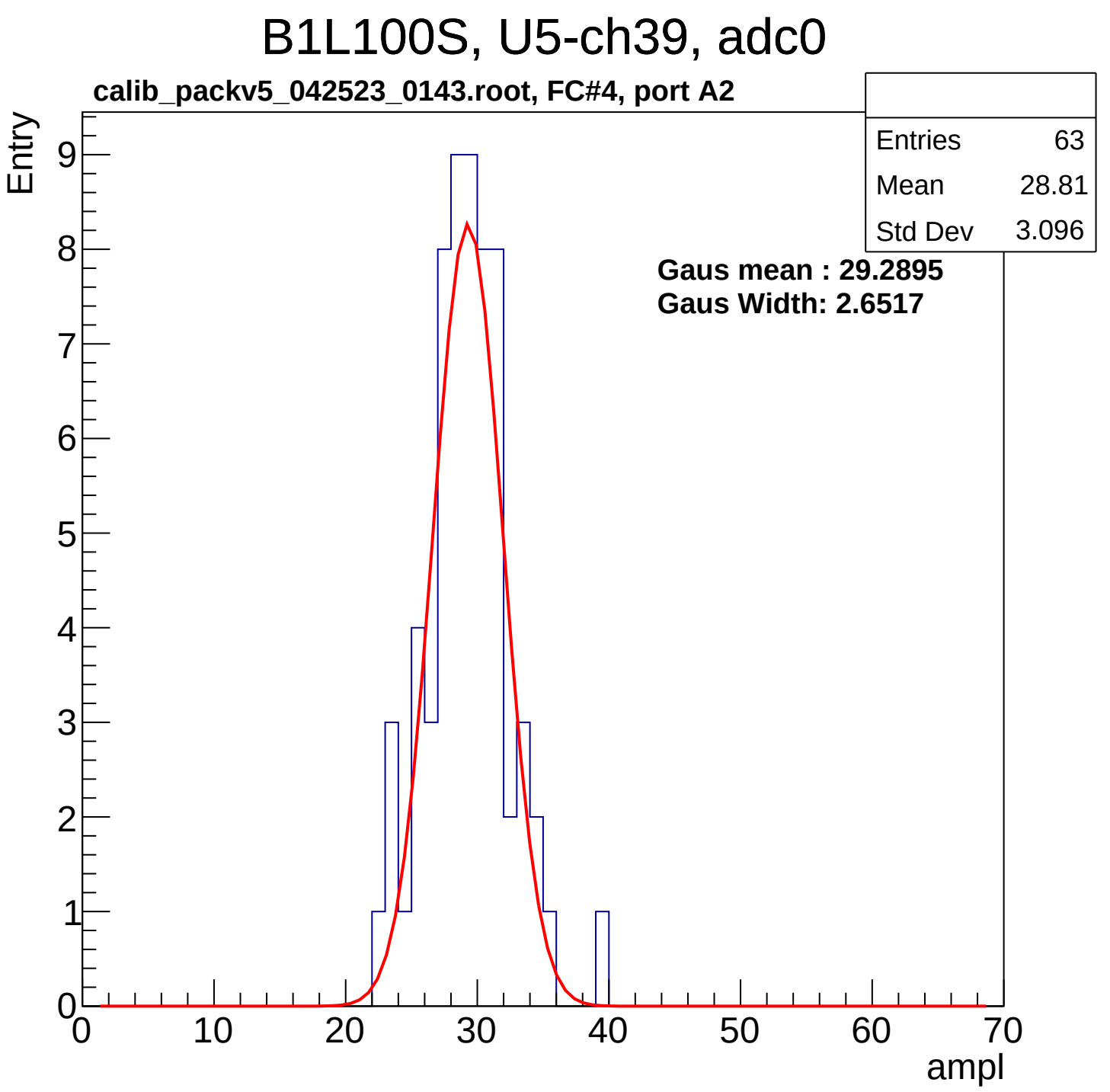

B1L100S, U5-ch38, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 80
Mean 48.26
Std Dev 3.423
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

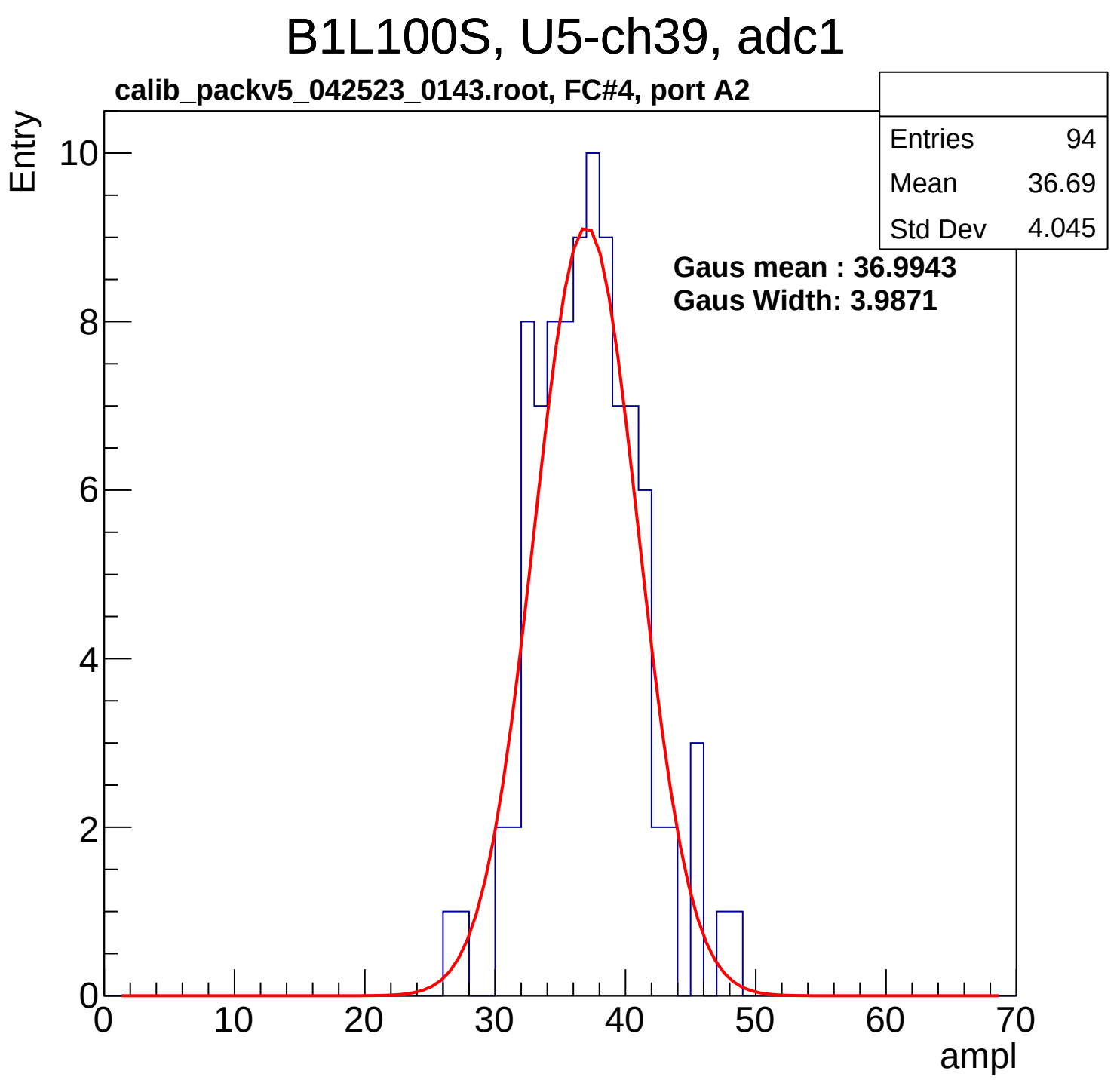

B1L100S, U5-ch38, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 46
Mean 54.48
Std Dev 3.634
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

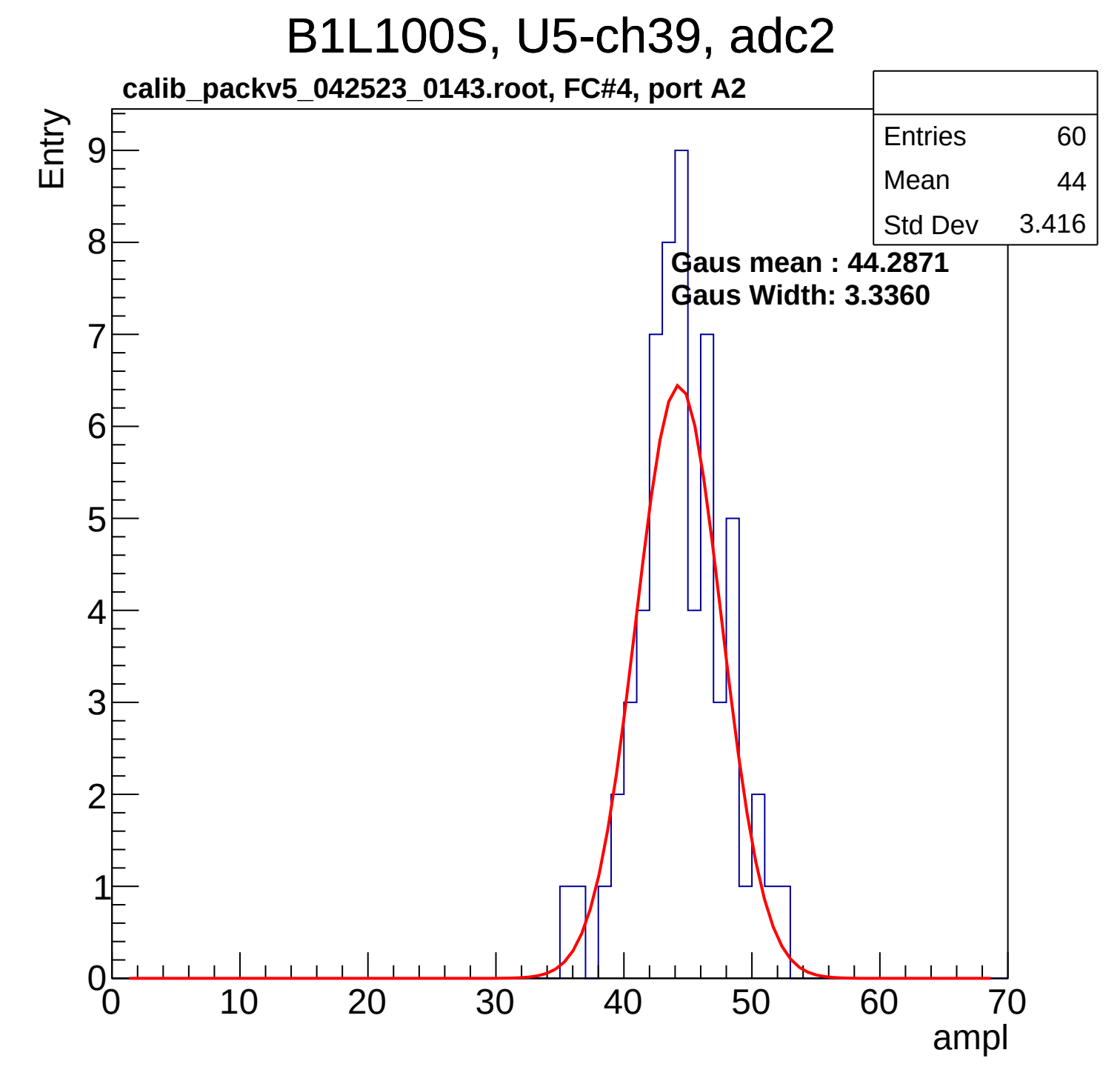

B1L100S, U5-ch38, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 58.02
Std Dev 8.123
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

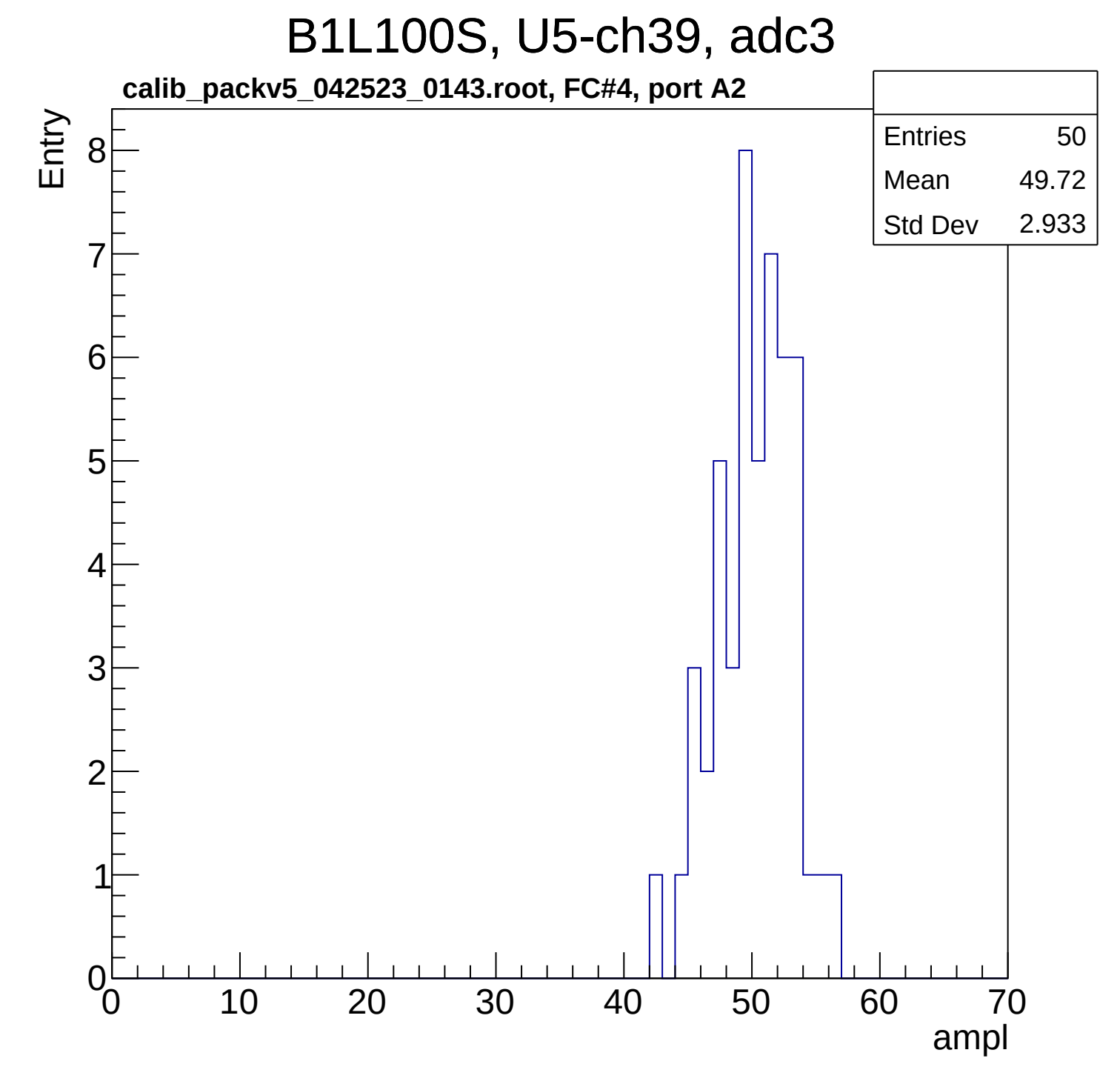

B1L100S, U5-ch38, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 10
Mean 61.4
Std Dev 1.625
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

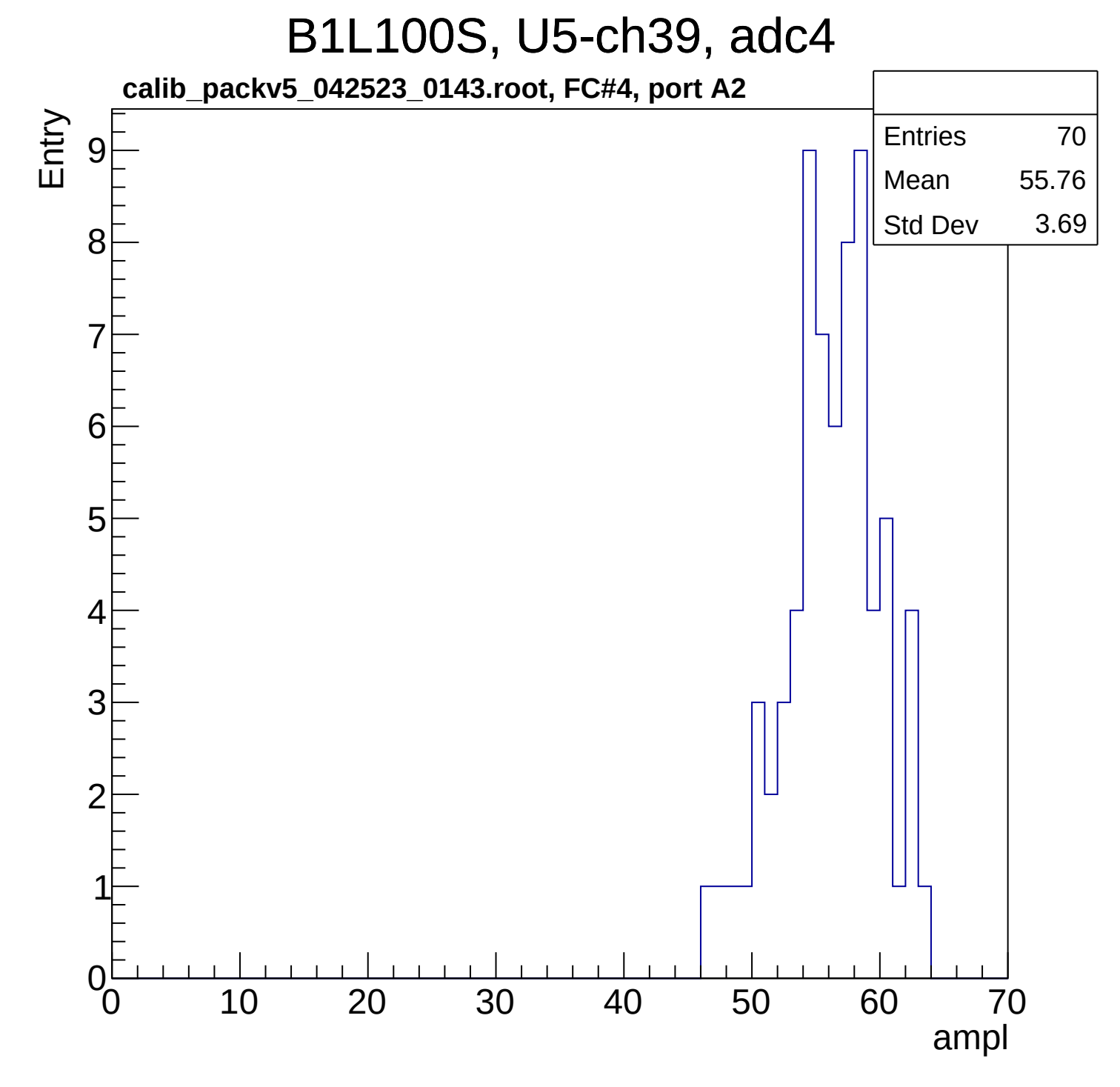

B1L100S, U5-ch38, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch39, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 28.81
Std Dev 3.096
Gaus mean : 29.2895
Gaus Width: 2.6517
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch39, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 94
Mean 36.69
Std Dev 4.045
Gaus mean : 36.9943
Gaus Width: 3.9871
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch39, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 44
Std Dev 3.416
Gaus mean : 44.2871
Gaus Width: 3.3360
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch39, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 49.72
Std Dev 2.933
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch39, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 55.76
Std Dev 3.69
Entry
ampl
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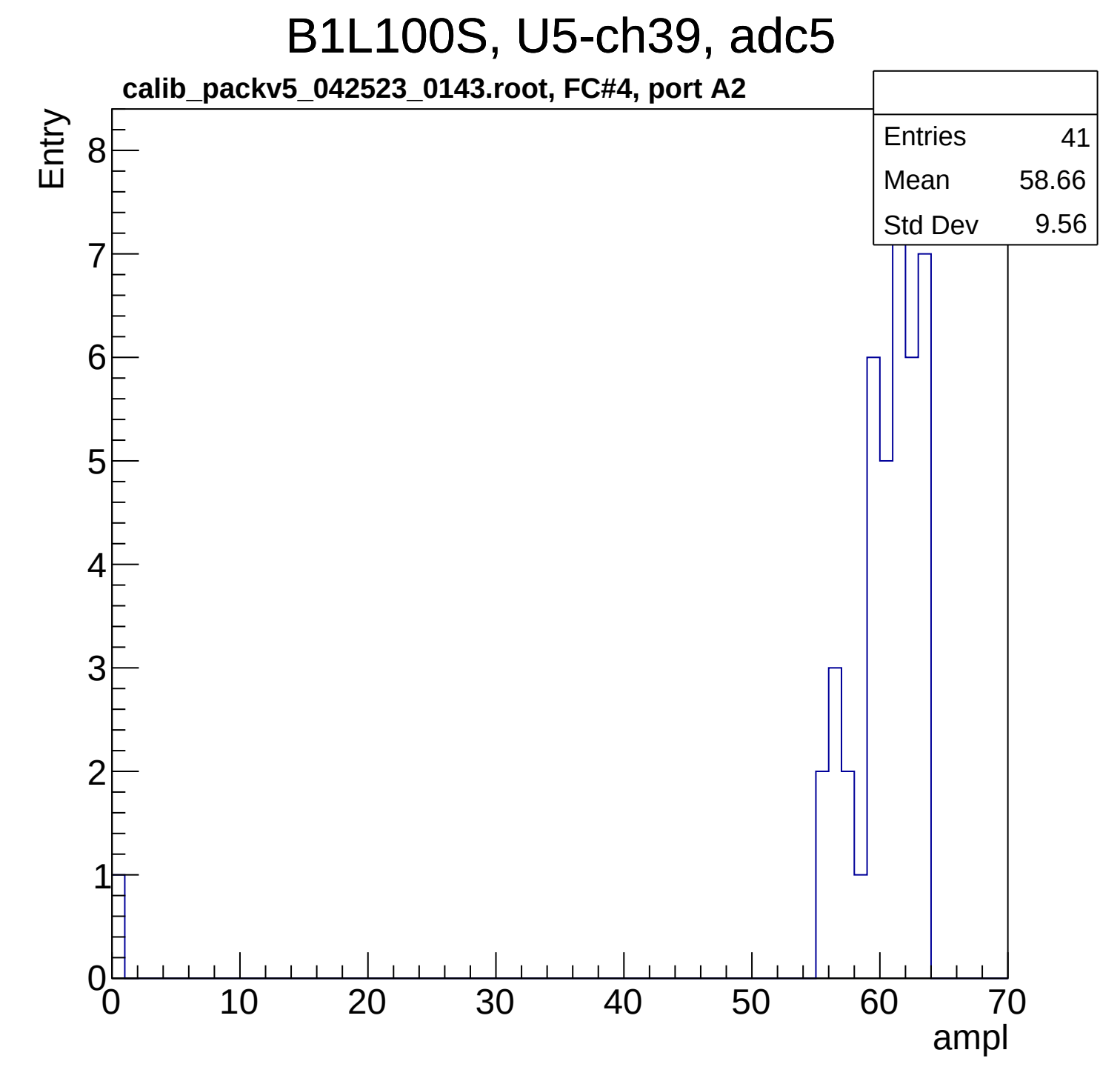
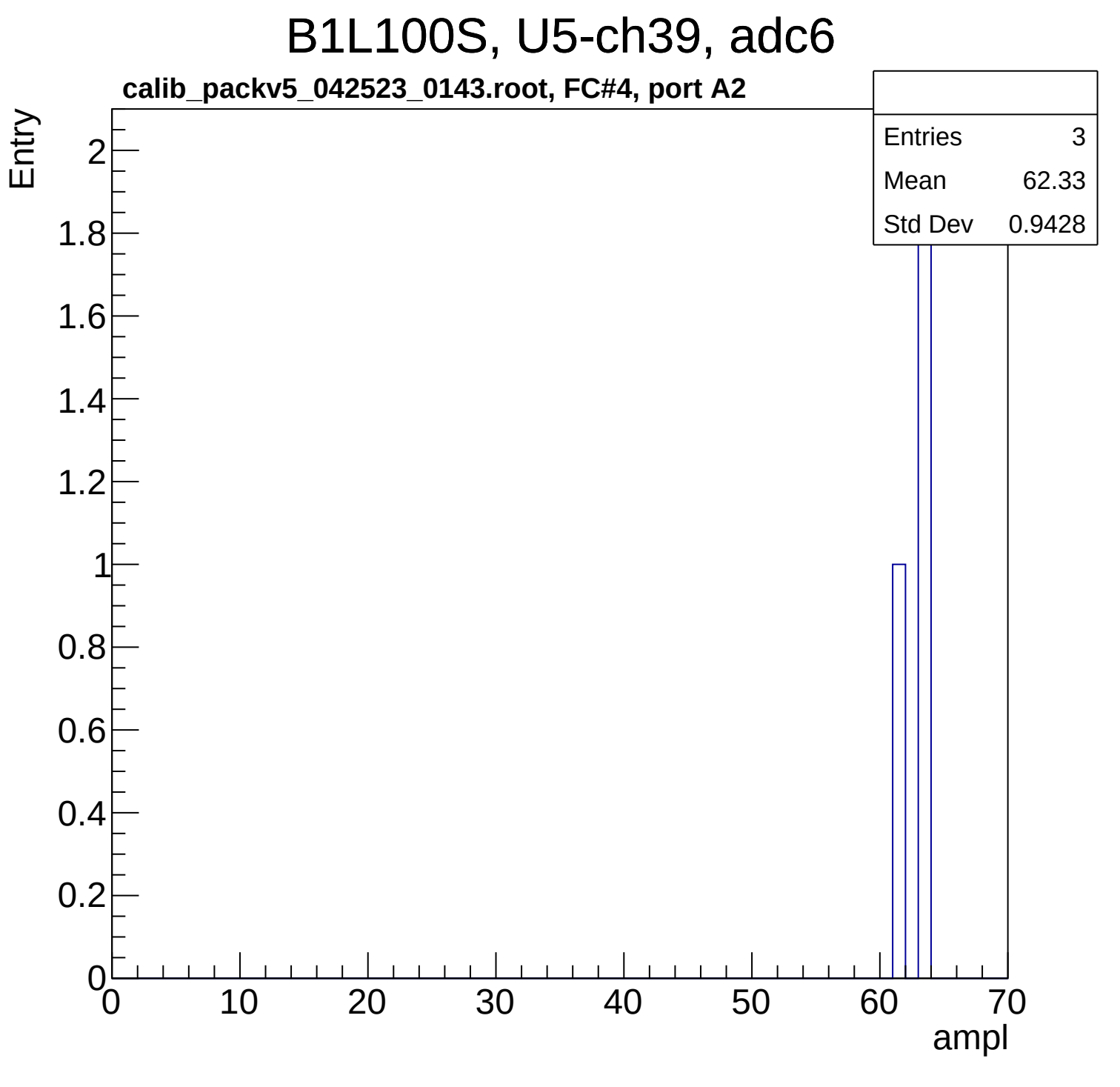
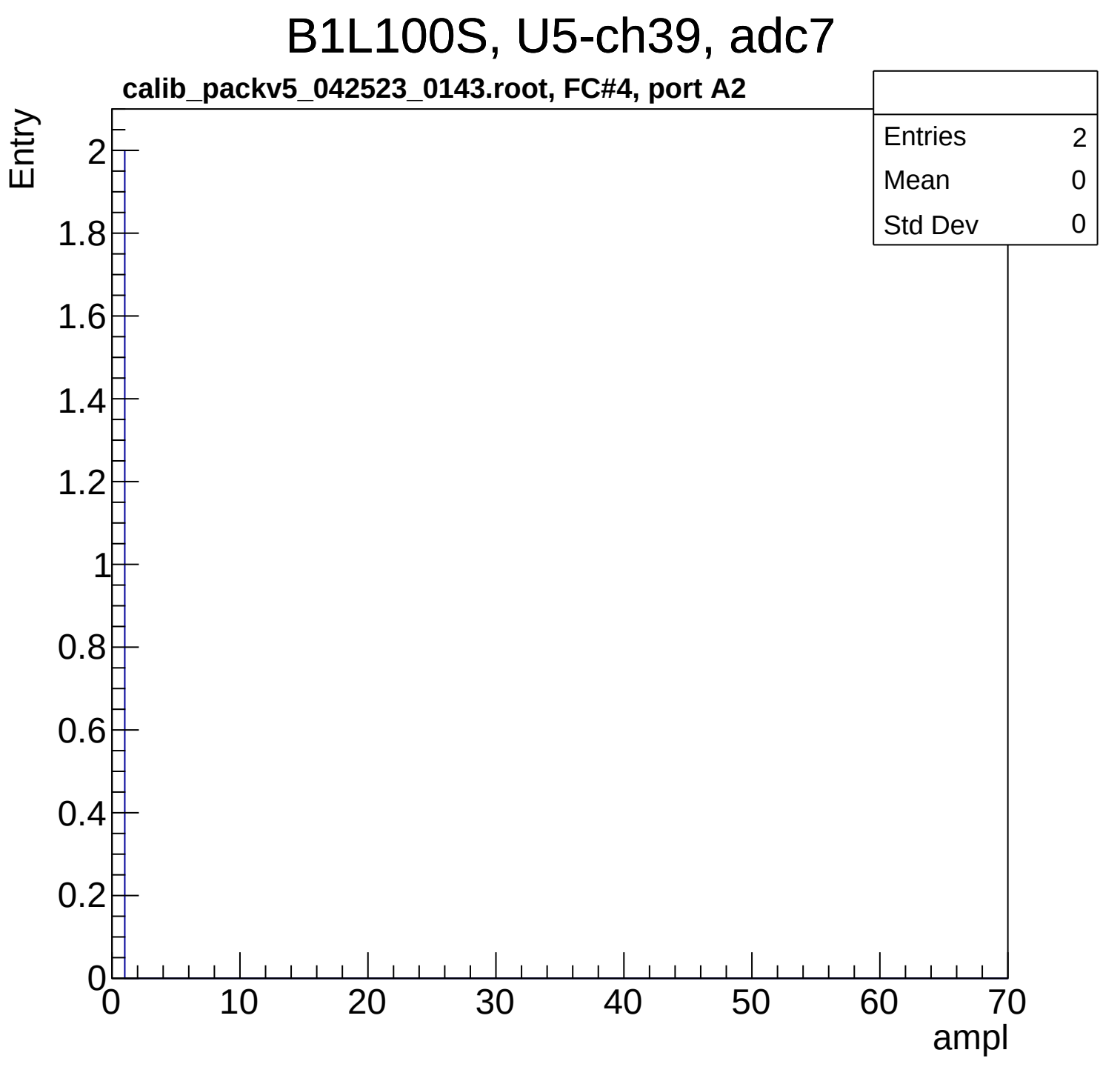
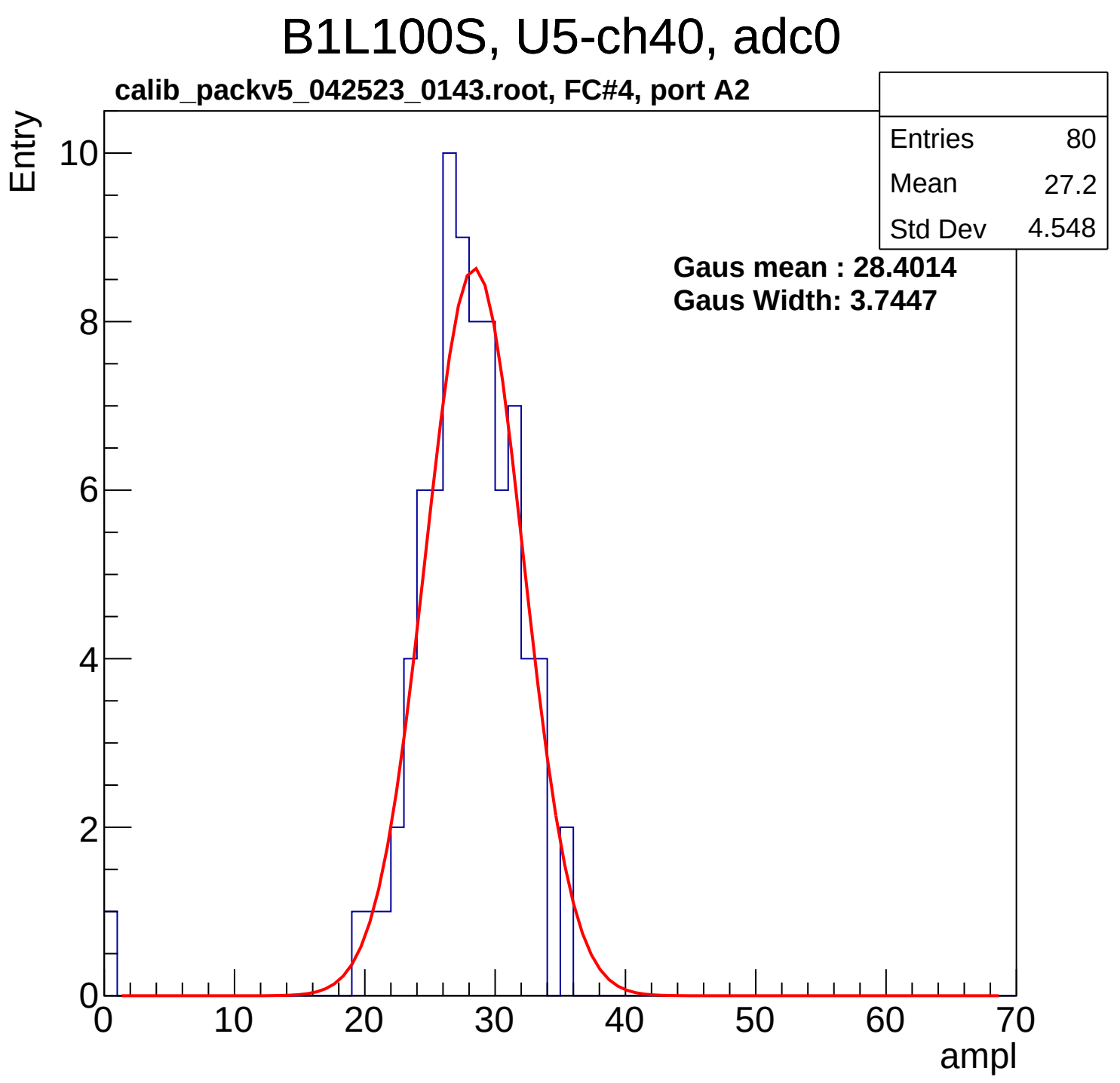
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch39, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 41
Mean 58.66
Std Dev 9.56
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch39, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 62.33
Std Dev 0.9428
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L100S, U5-ch39, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch40, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 80
Mean 27.2
Std Dev 4.548
Gaus mean : 28.4014
Gaus Width: 3.7447
Entry
ampl
0
2
4
6
8
10
0
10
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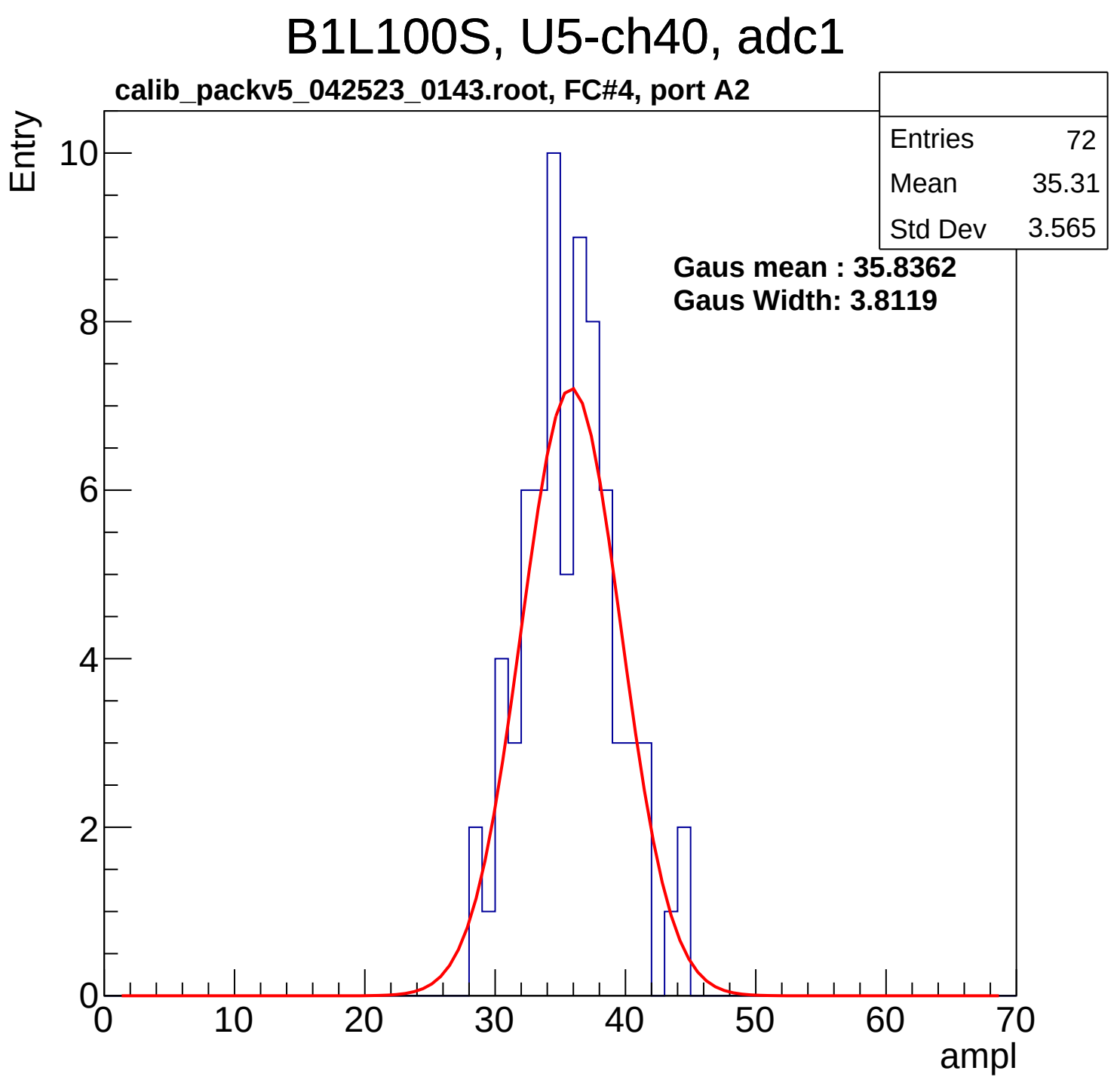
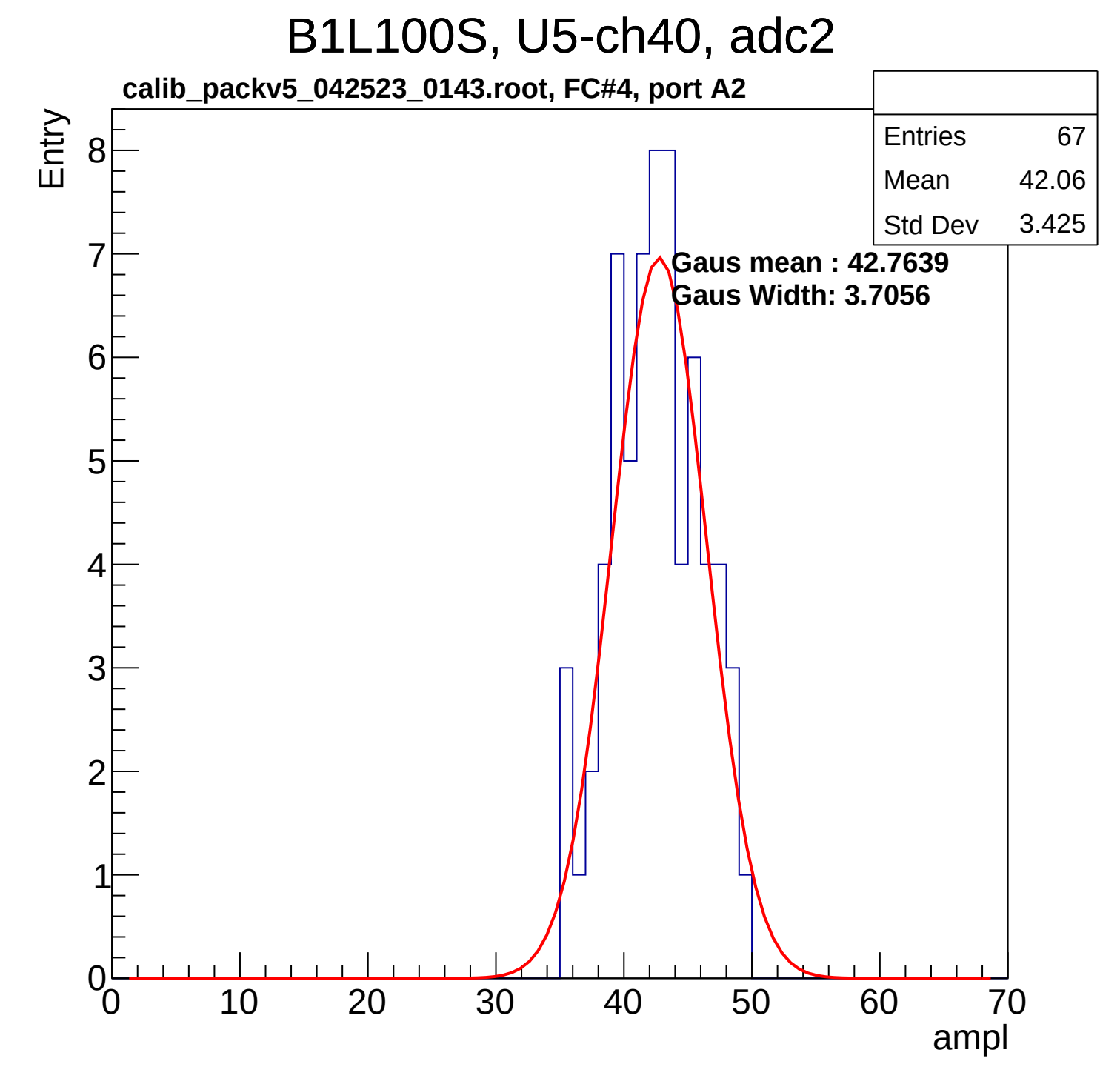
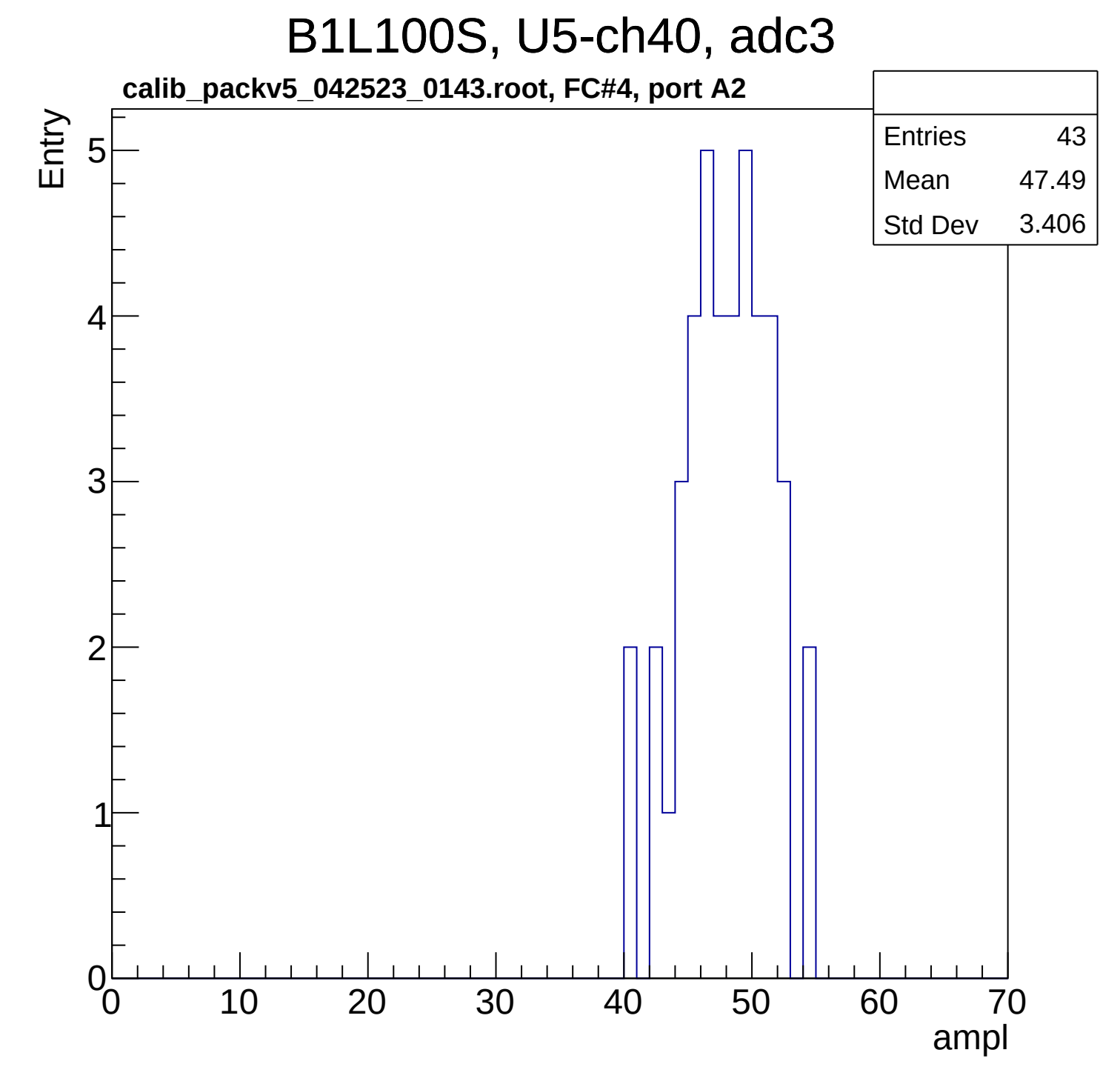
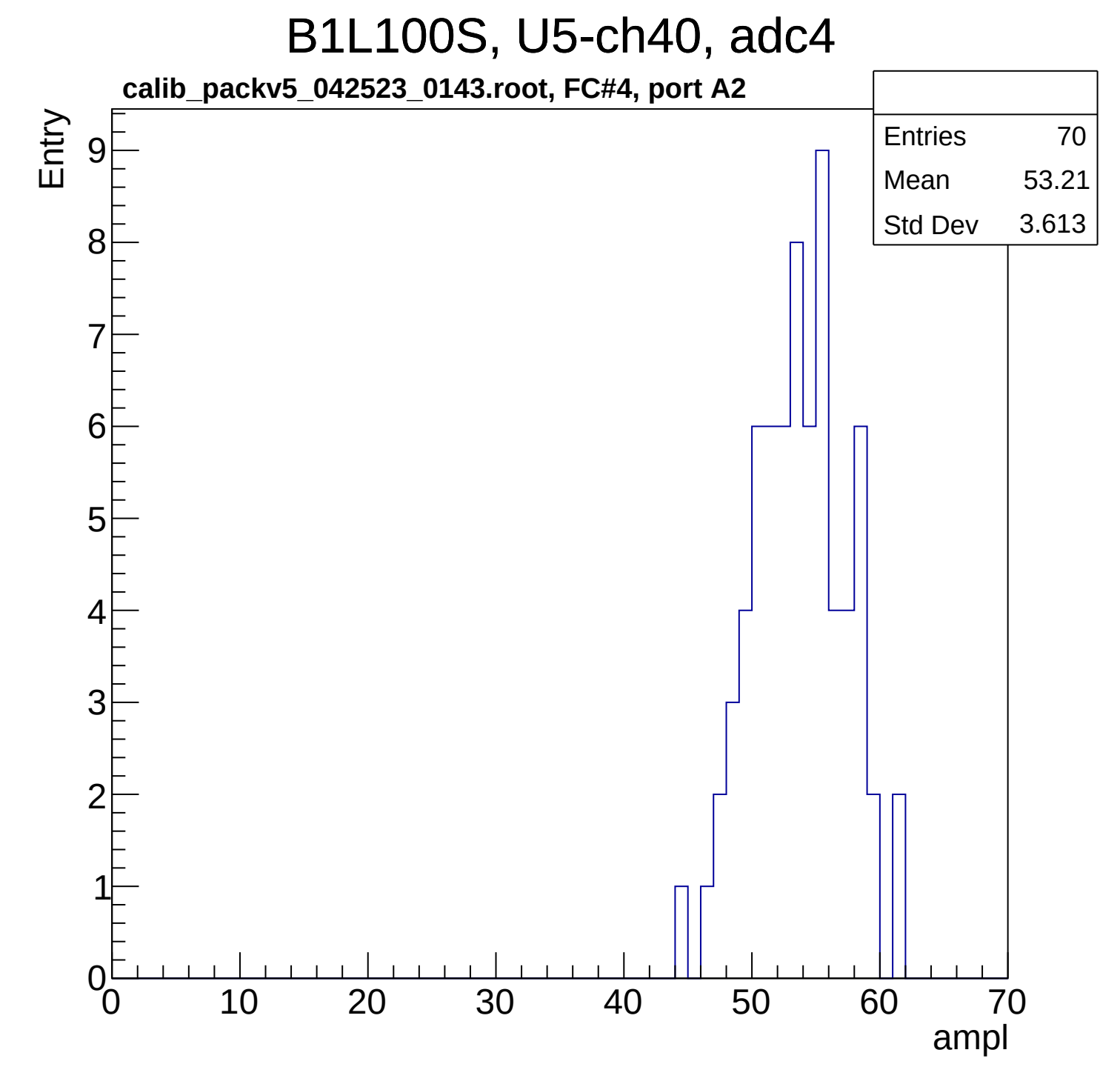
60
70


B1L100S, U5-ch40, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 35.31
Std Dev 3.565
Gaus mean : 35.8362
Gaus Width: 3.8119
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch40, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 42.06
Std Dev 3.425
Gaus mean : 42.7639
Gaus Width: 3.7056
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch40, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 43
Mean 47.49
Std Dev 3.406
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch40, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 53.21
Std Dev 3.613
Entry
ampl
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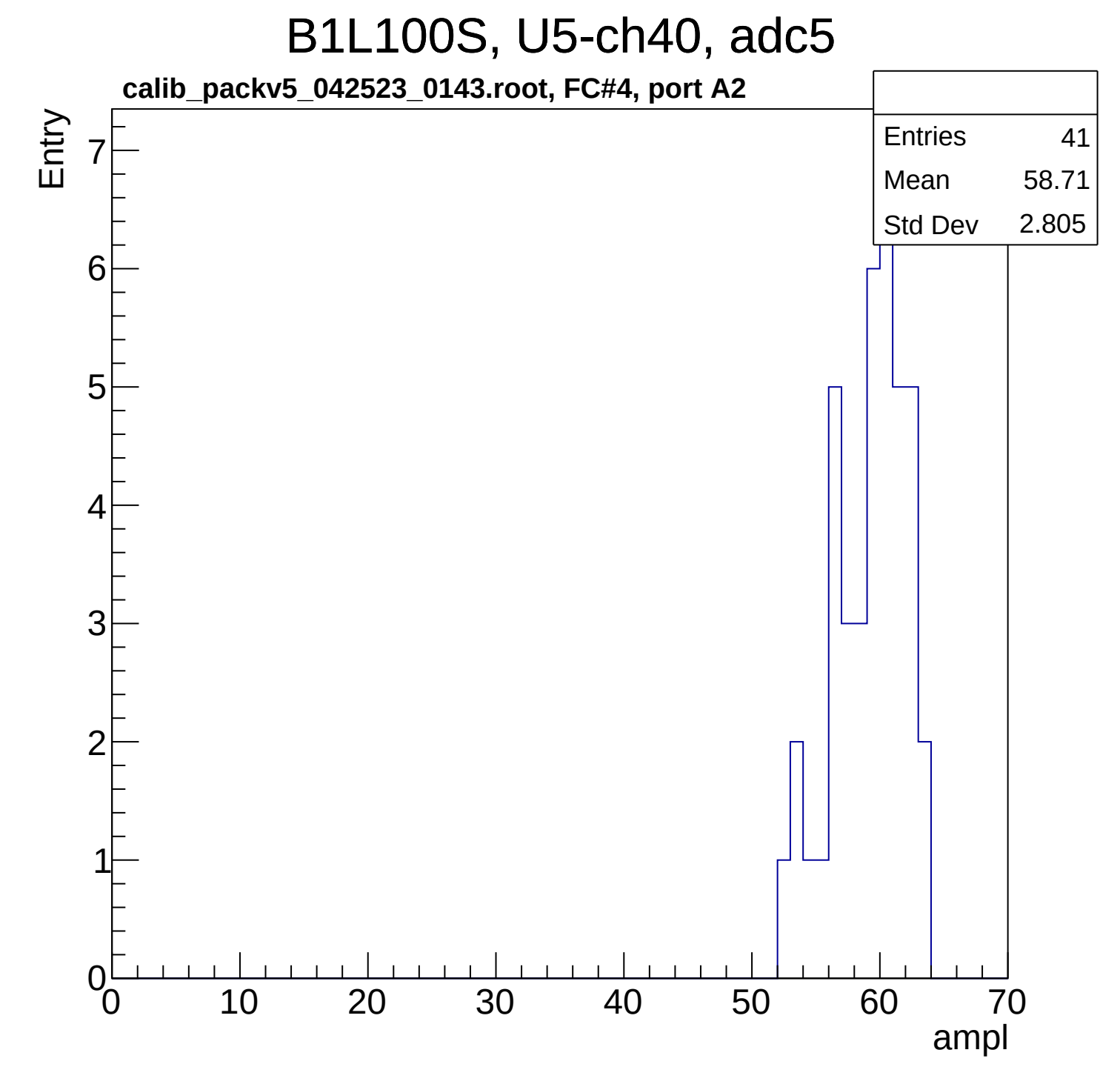
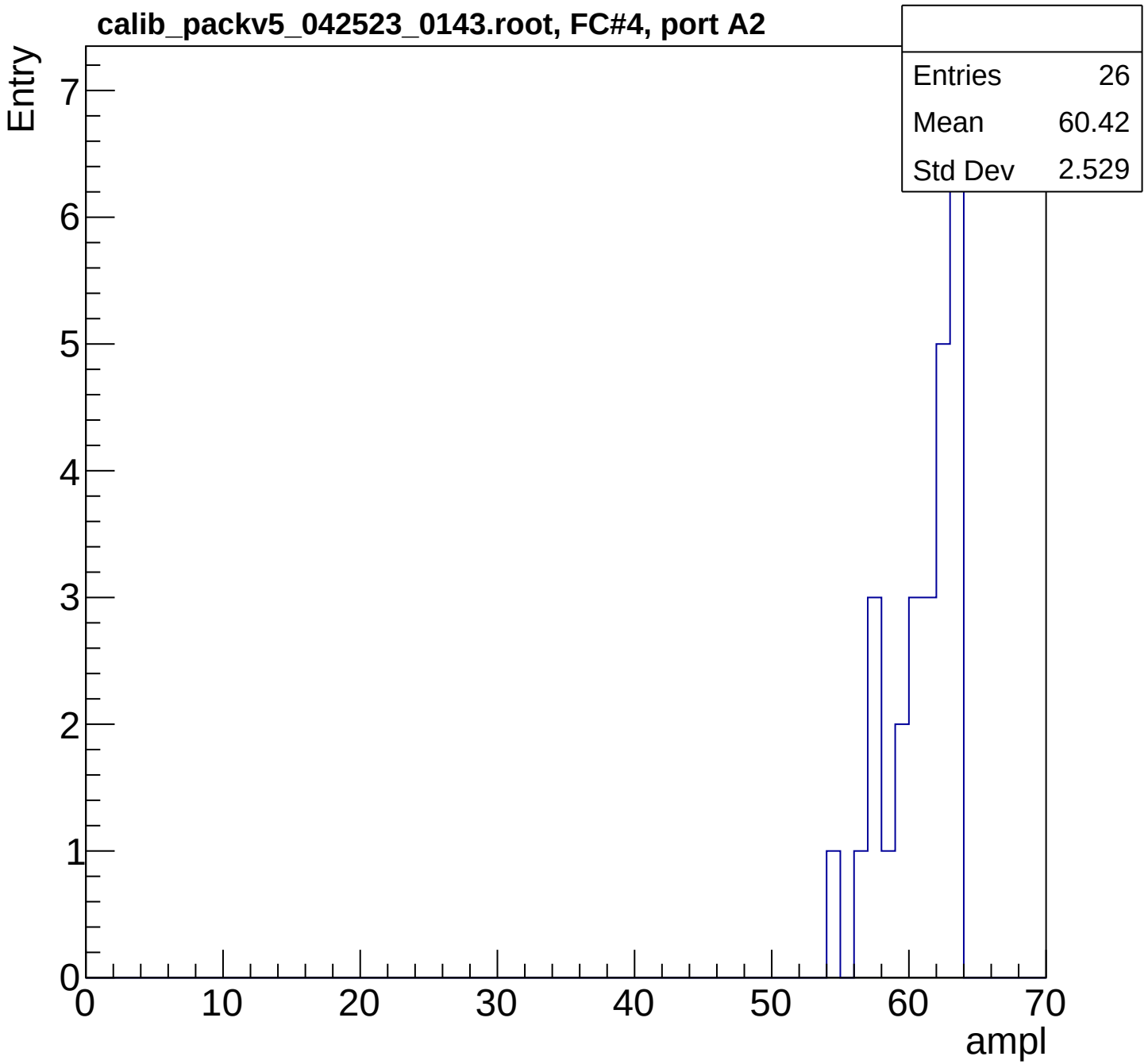
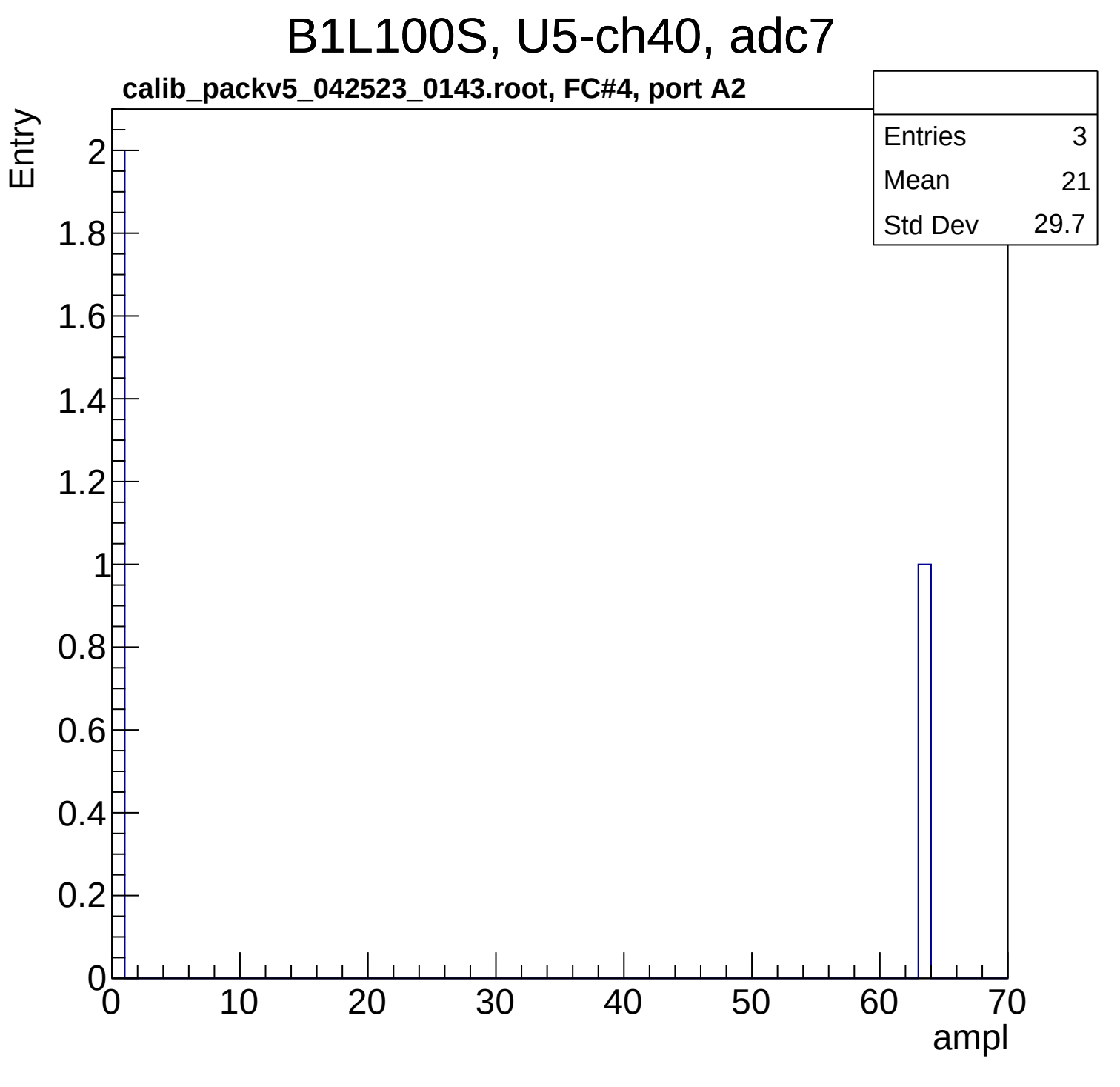
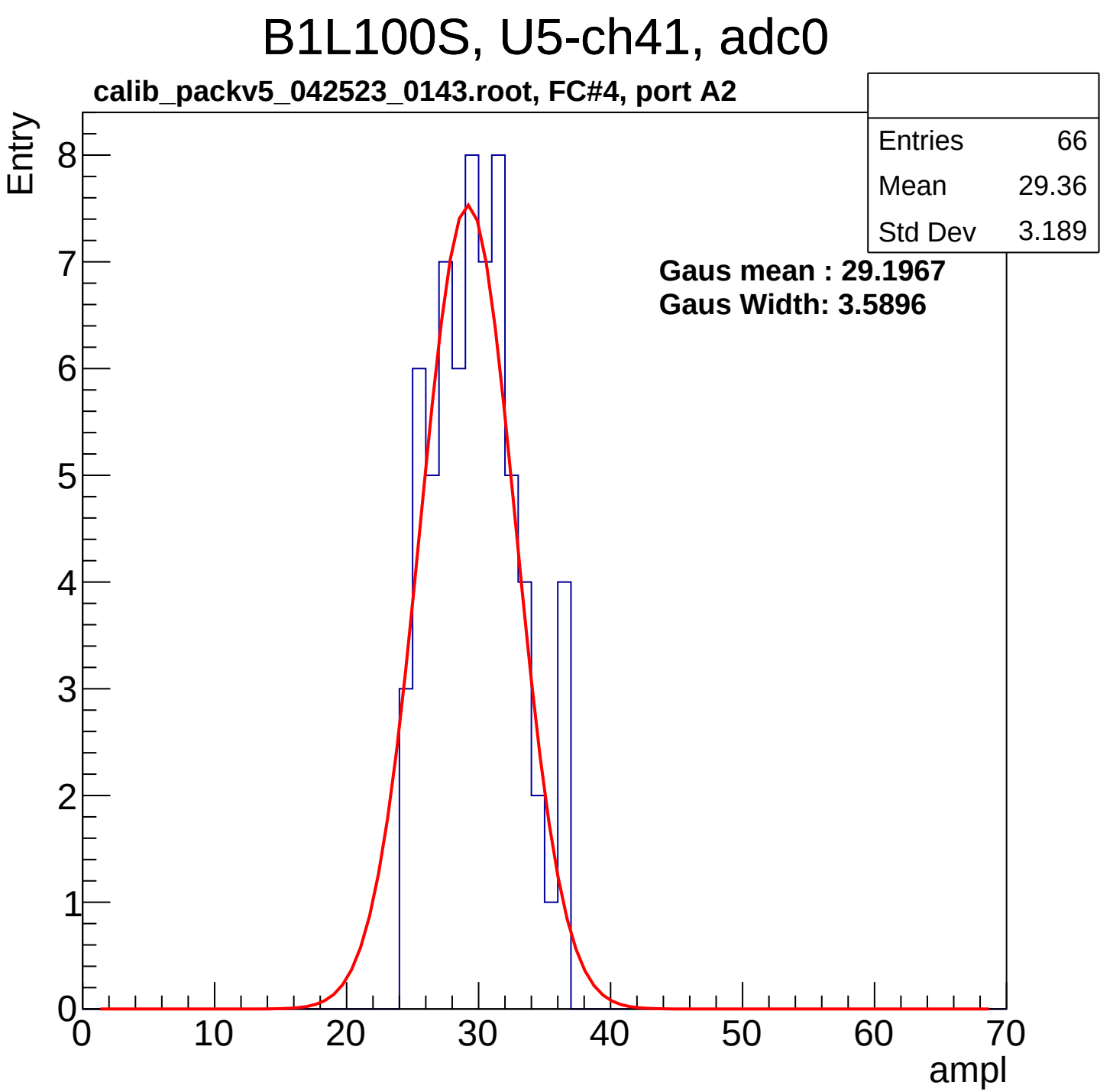
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch40, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 41
Mean 58.71
Std Dev 2.805
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U5-ch40, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 26
Mean 60.42
Std Dev 2.529
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U5-ch40, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 21
Std Dev 29.7
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L100S, U5-ch41, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 29.36
Std Dev 3.189
Gaus mean : 29.1967
Gaus Width: 3.5896
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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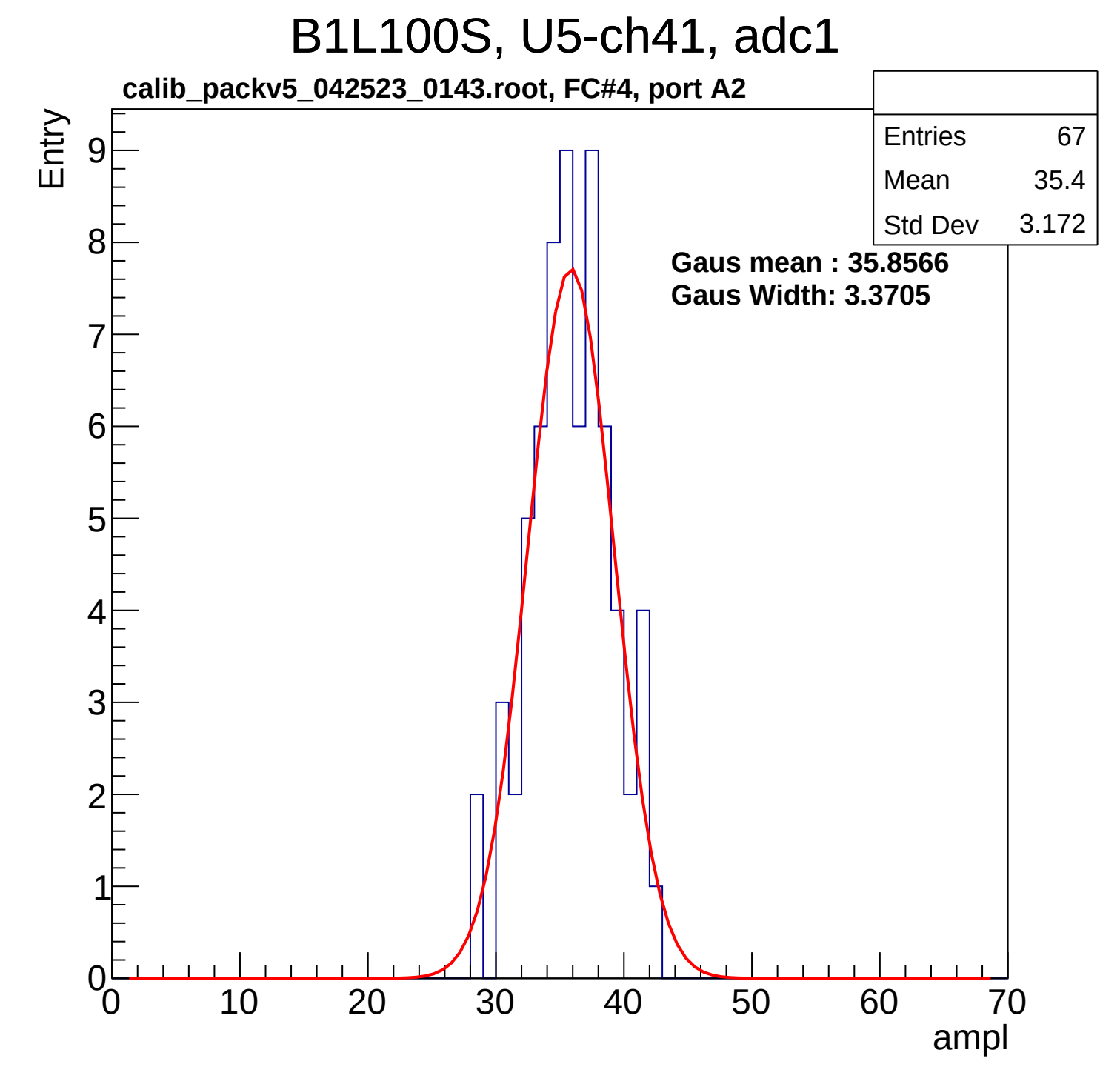
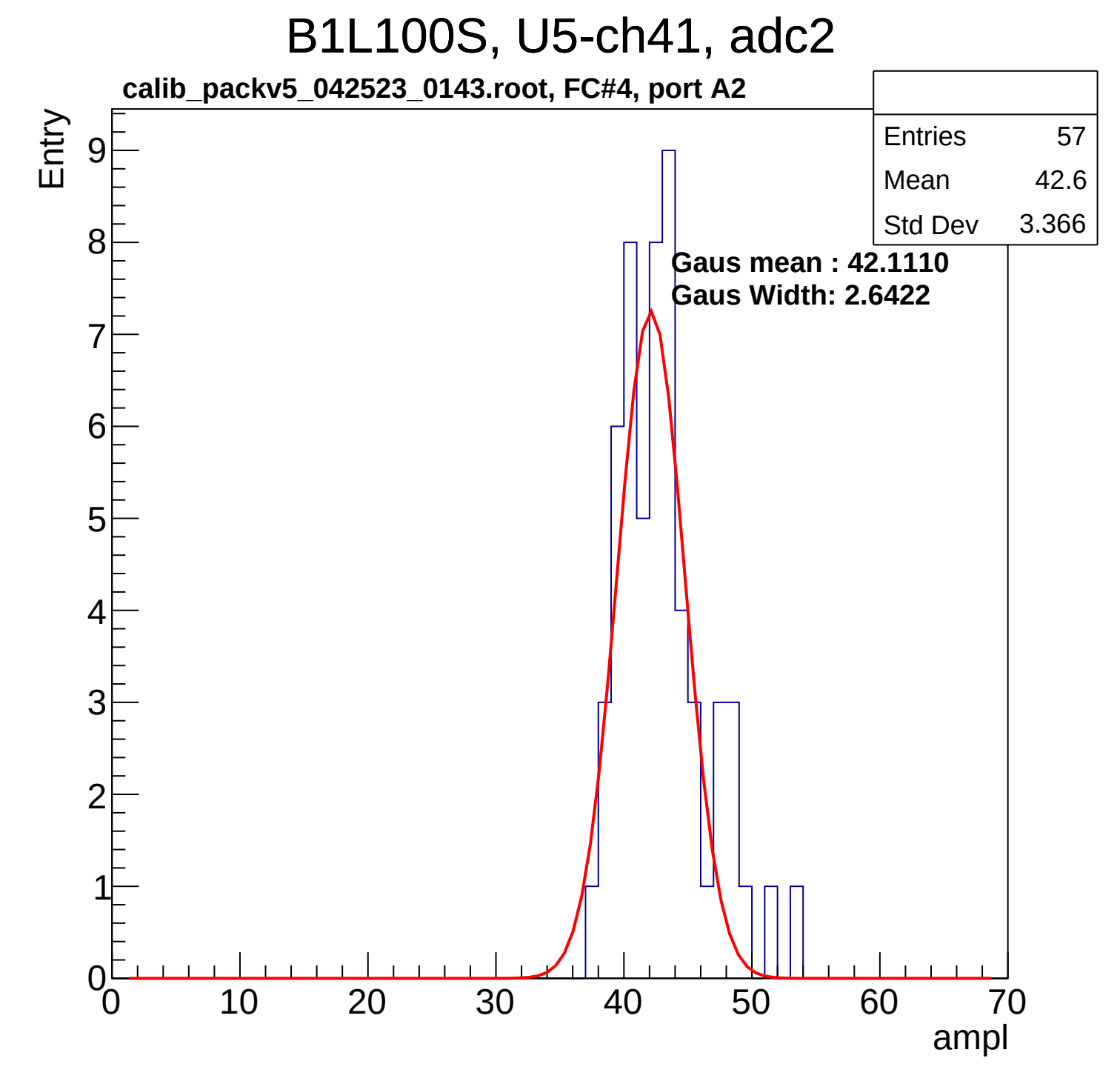
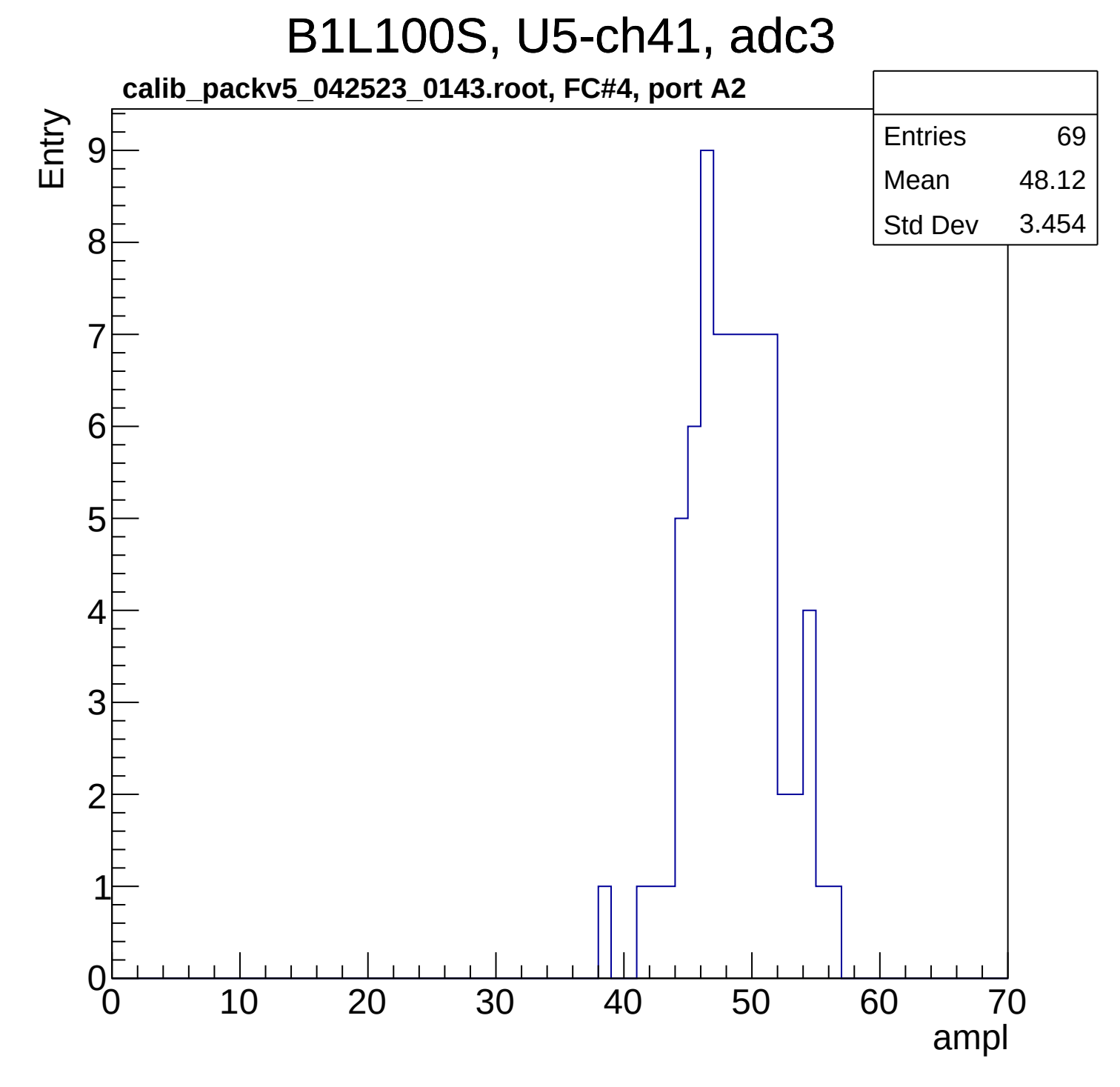

B1L100S, U5-ch41, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 35.4
Std Dev 3.172
Gaus mean : 35.8566
Gaus Width: 3.3705
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch41, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 42.6
Std Dev 3.366
Gaus mean : 42.1110
Gaus Width: 2.6422
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch41, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 48.12
Std Dev 3.454
Entry
ampl
0
1
2
3
4
5
6
7
8
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0
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60
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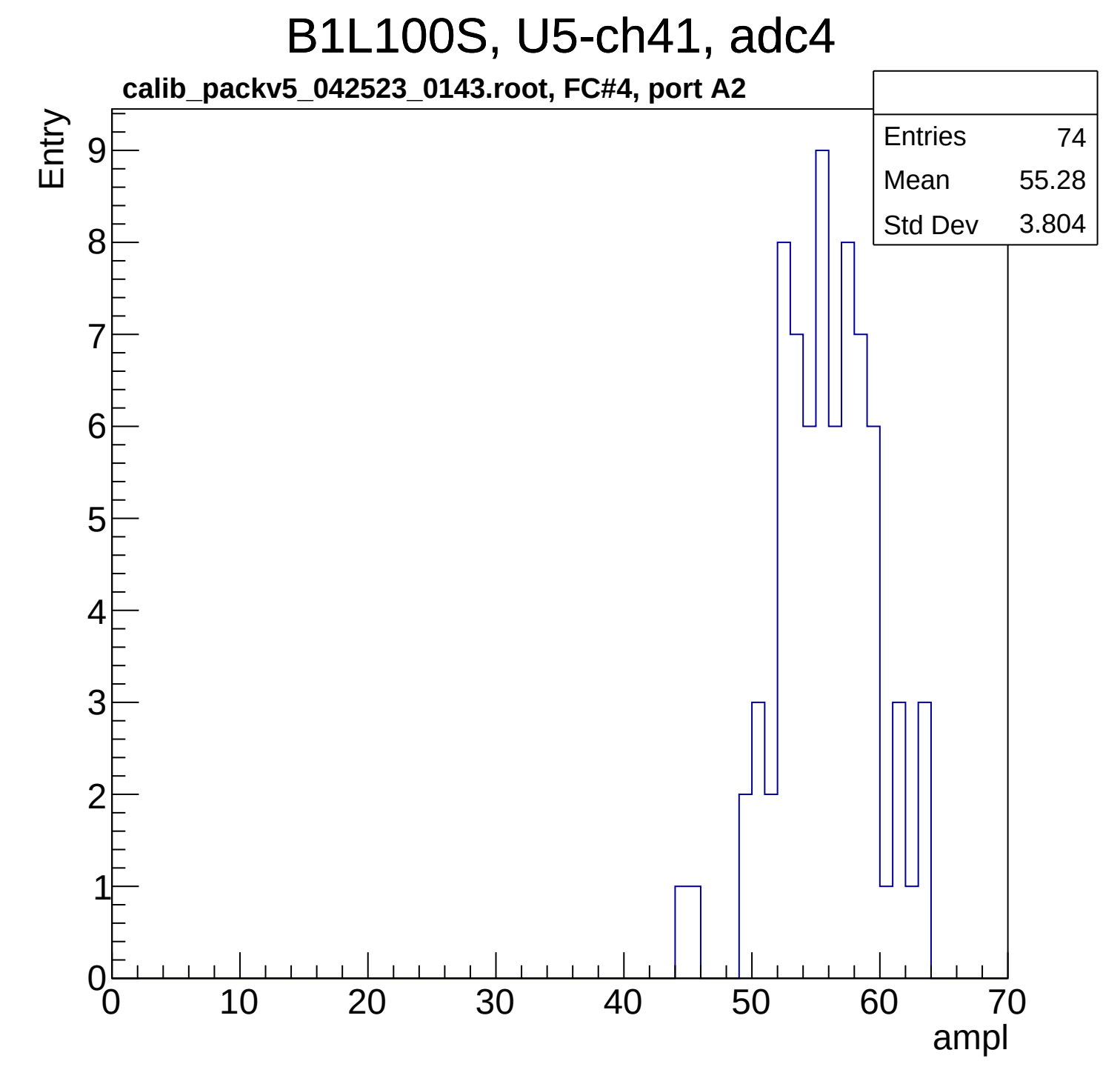
B1L100S, U5-ch41, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 74
Mean 55.28
Std Dev 3.804
Entry
ampl
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2
3
4
5
6
7
8
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0
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20
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40
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60
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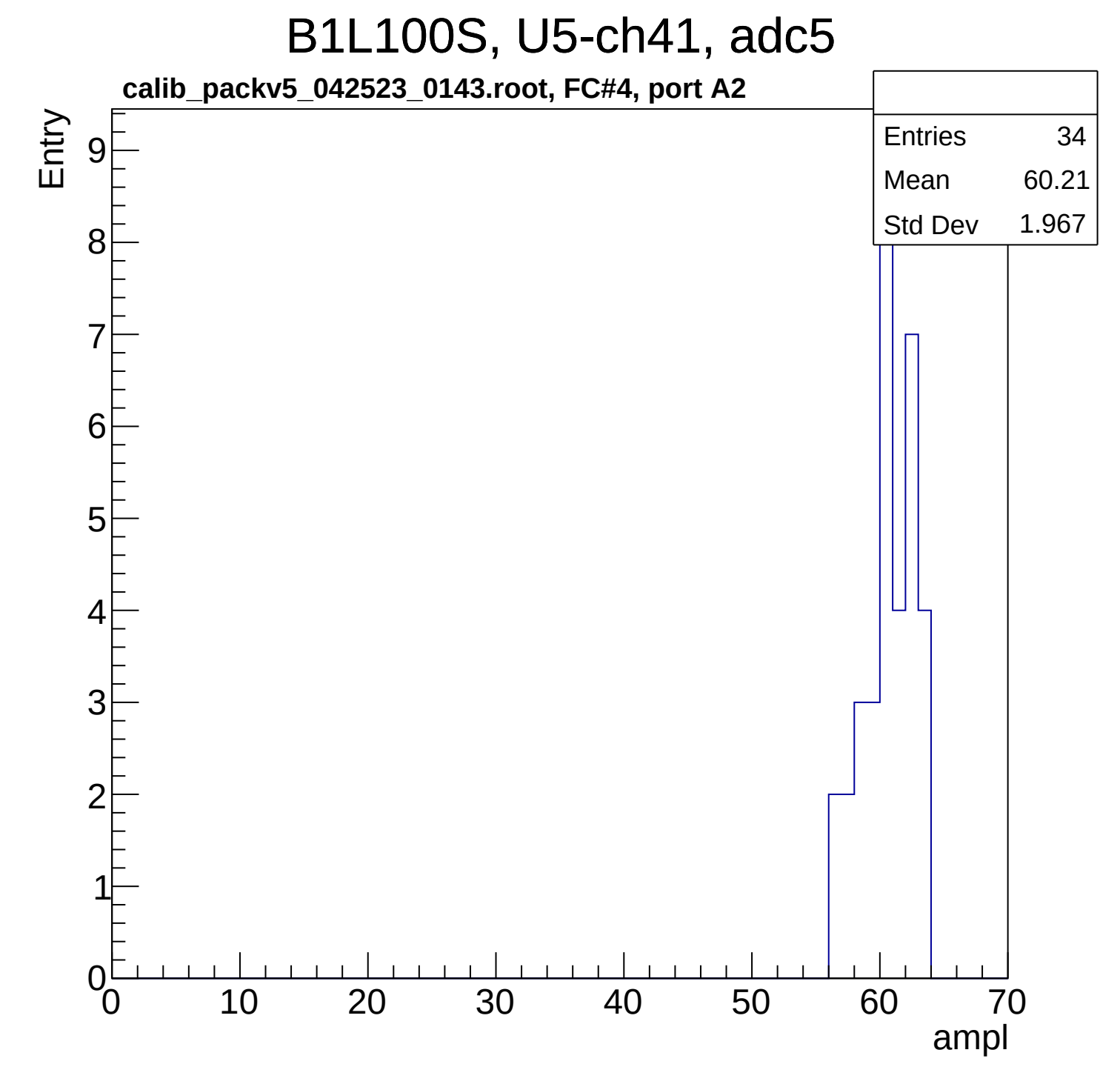
B1L100S, U5-ch41, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 34
Mean 60.21
Std Dev 1.967
Entry
ampl
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2
3
4
5
6
7
8
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0
10
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30
40
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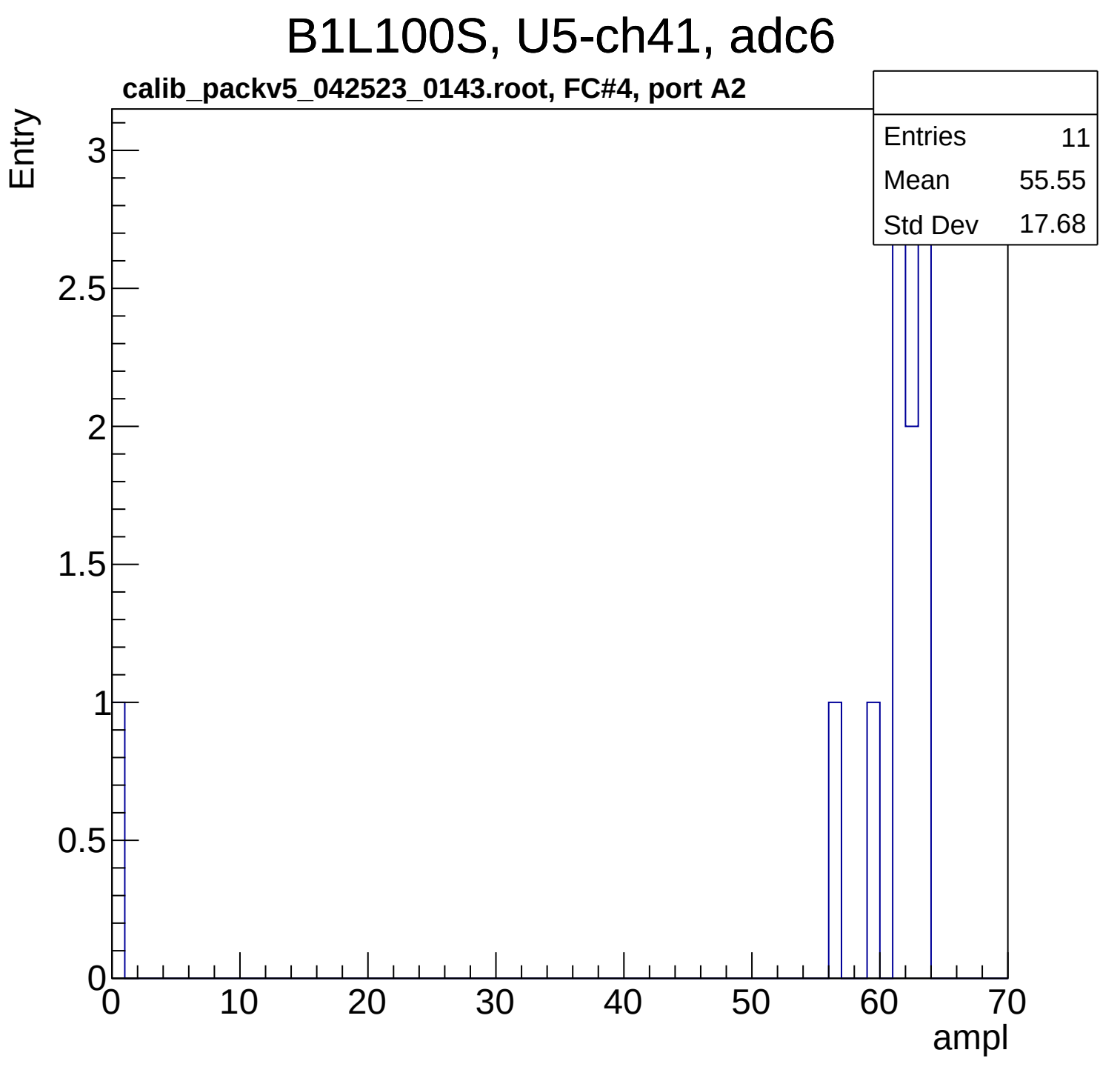
60
70


B1L100S, U5-ch41, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 11
Mean 55.55
Std Dev 17.68
Entry
ampl
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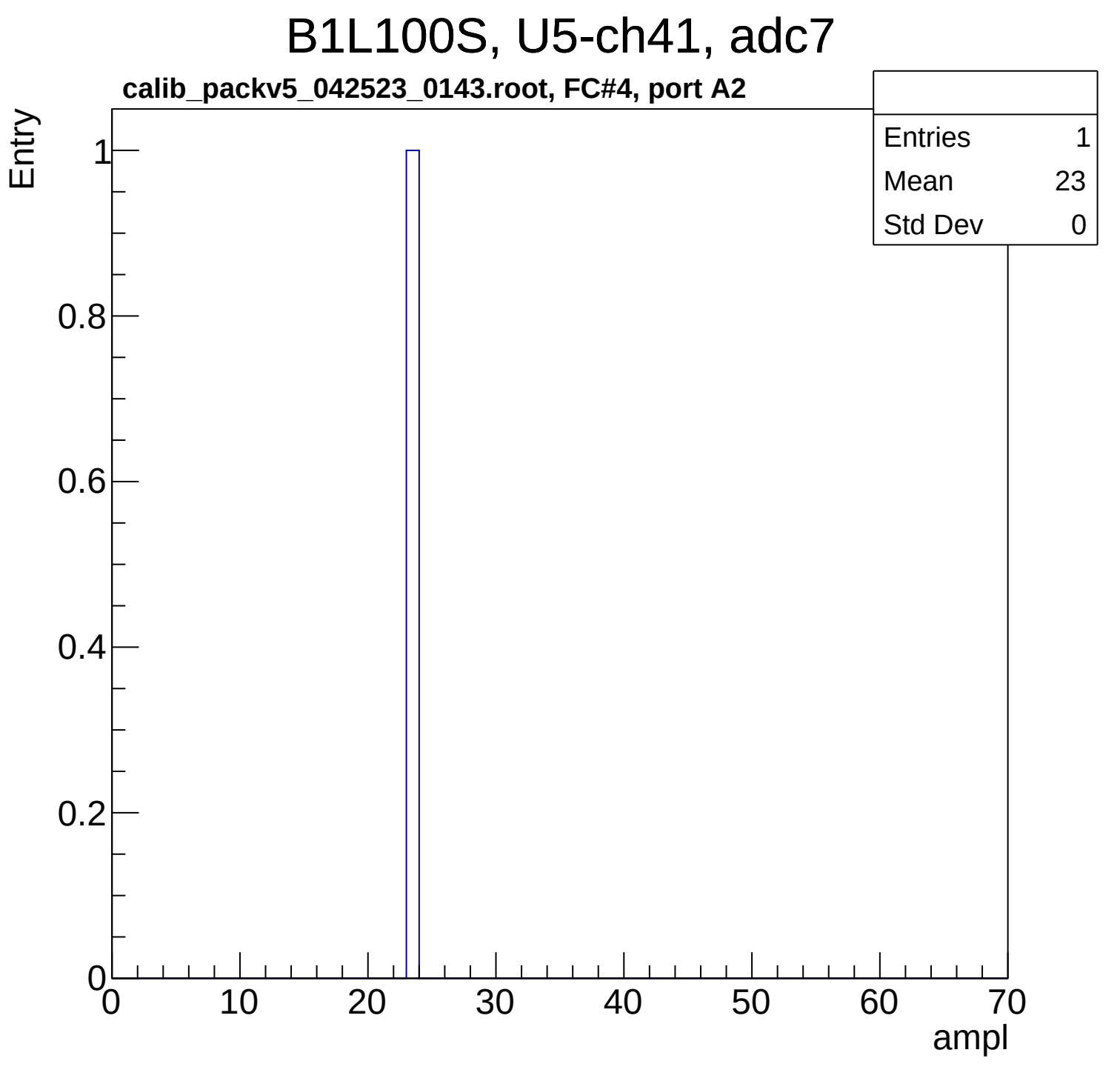
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L100S, U5-ch41, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 23
Std Dev 0
Entry
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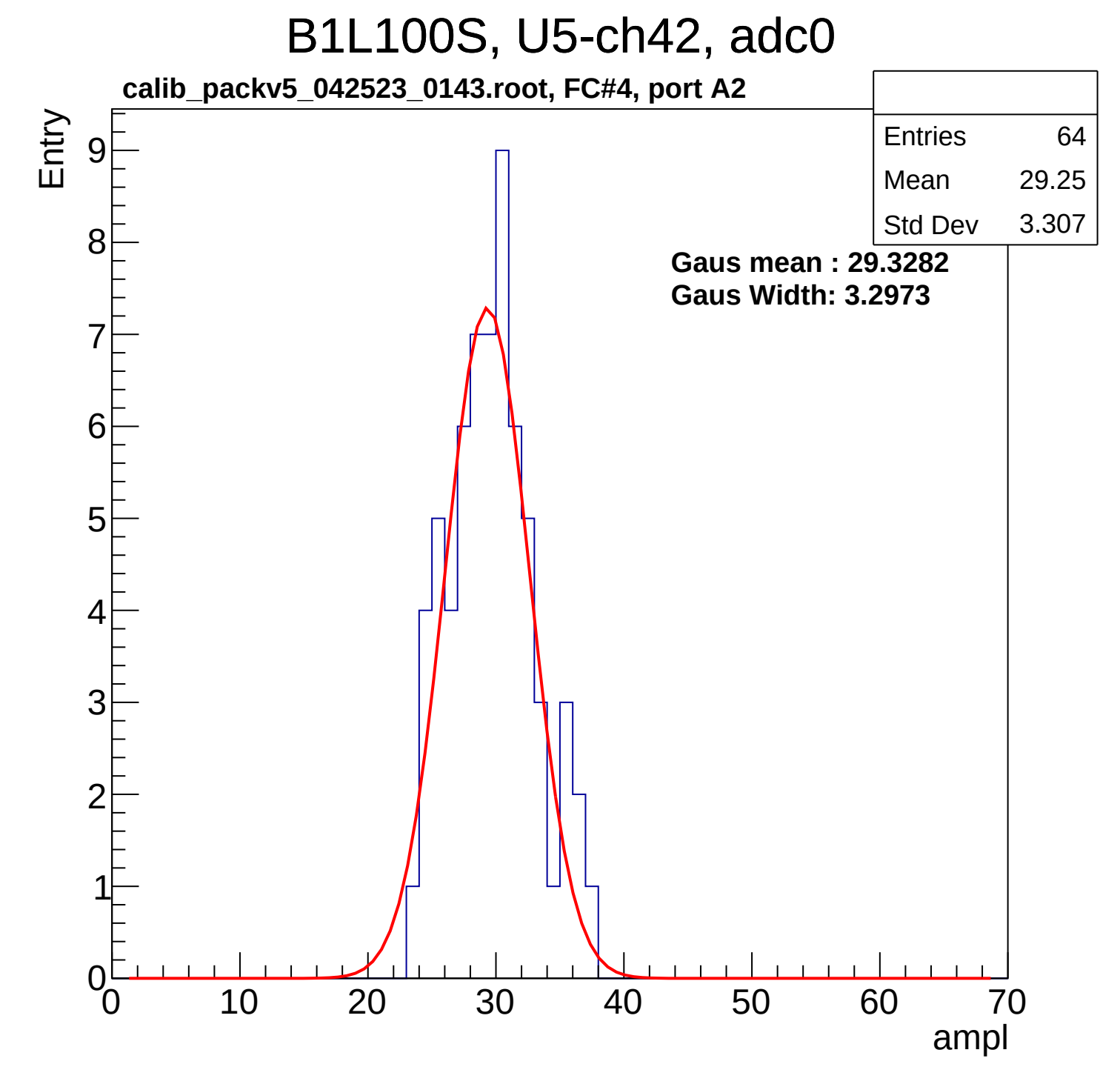
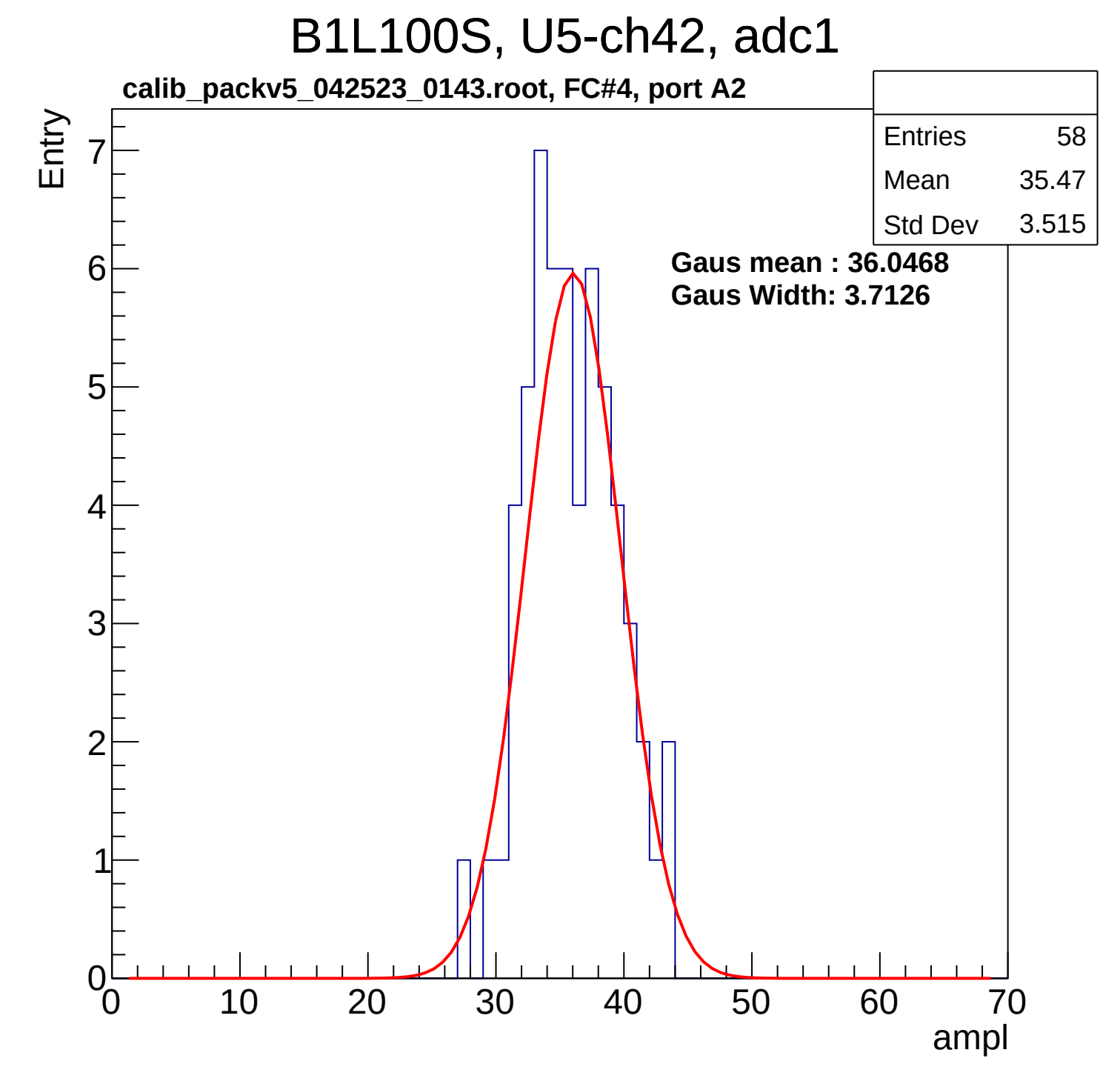
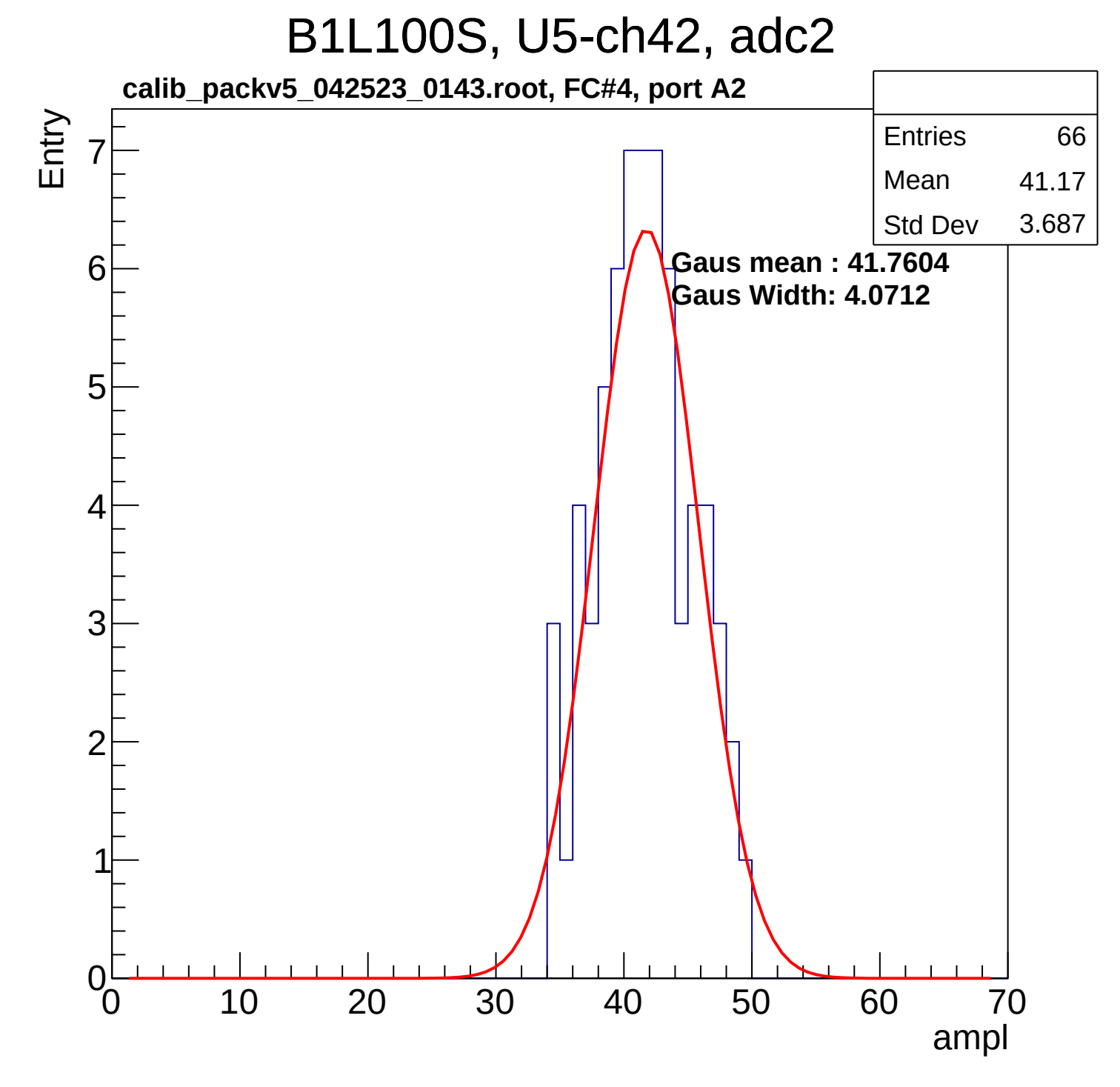
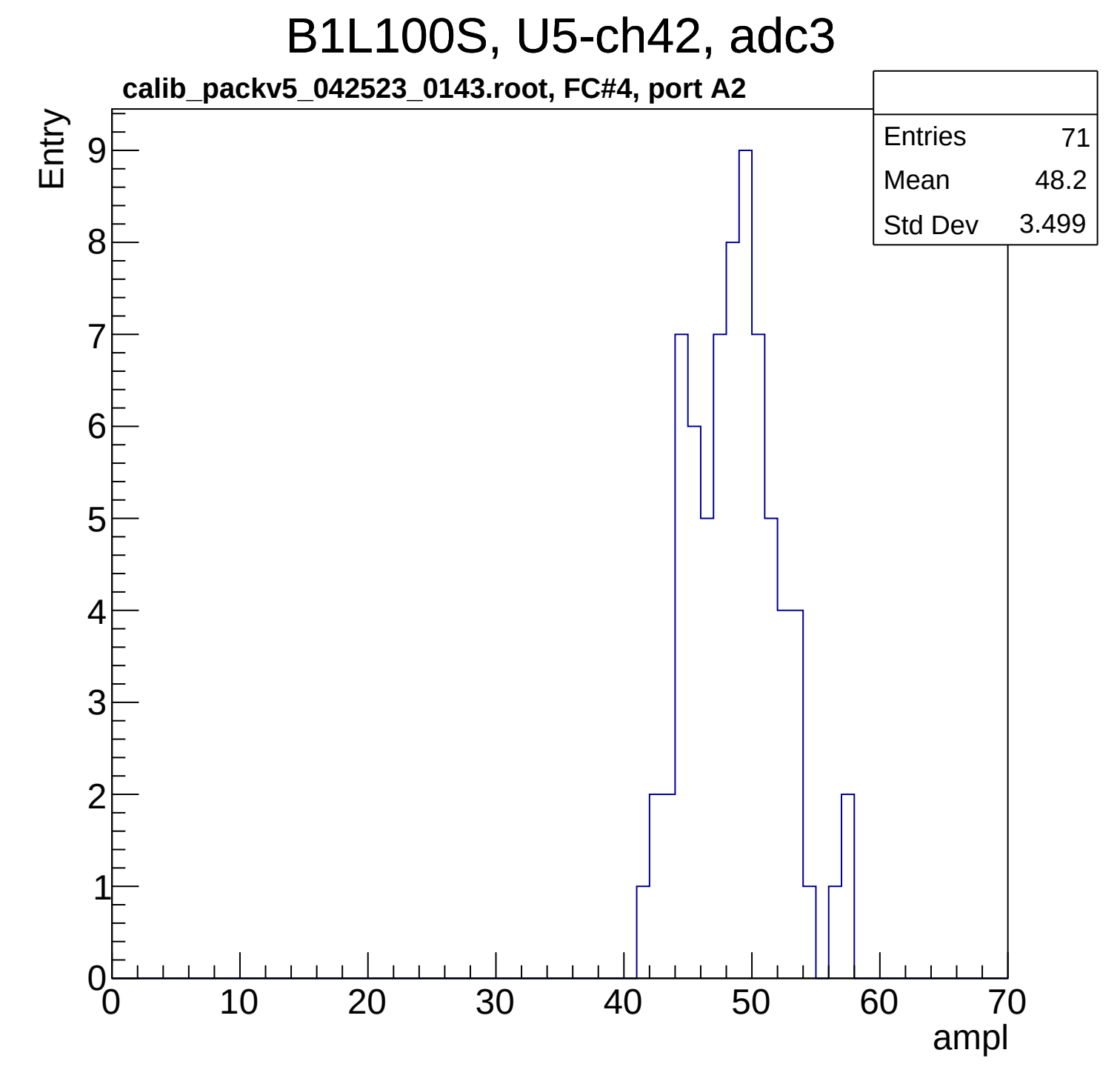
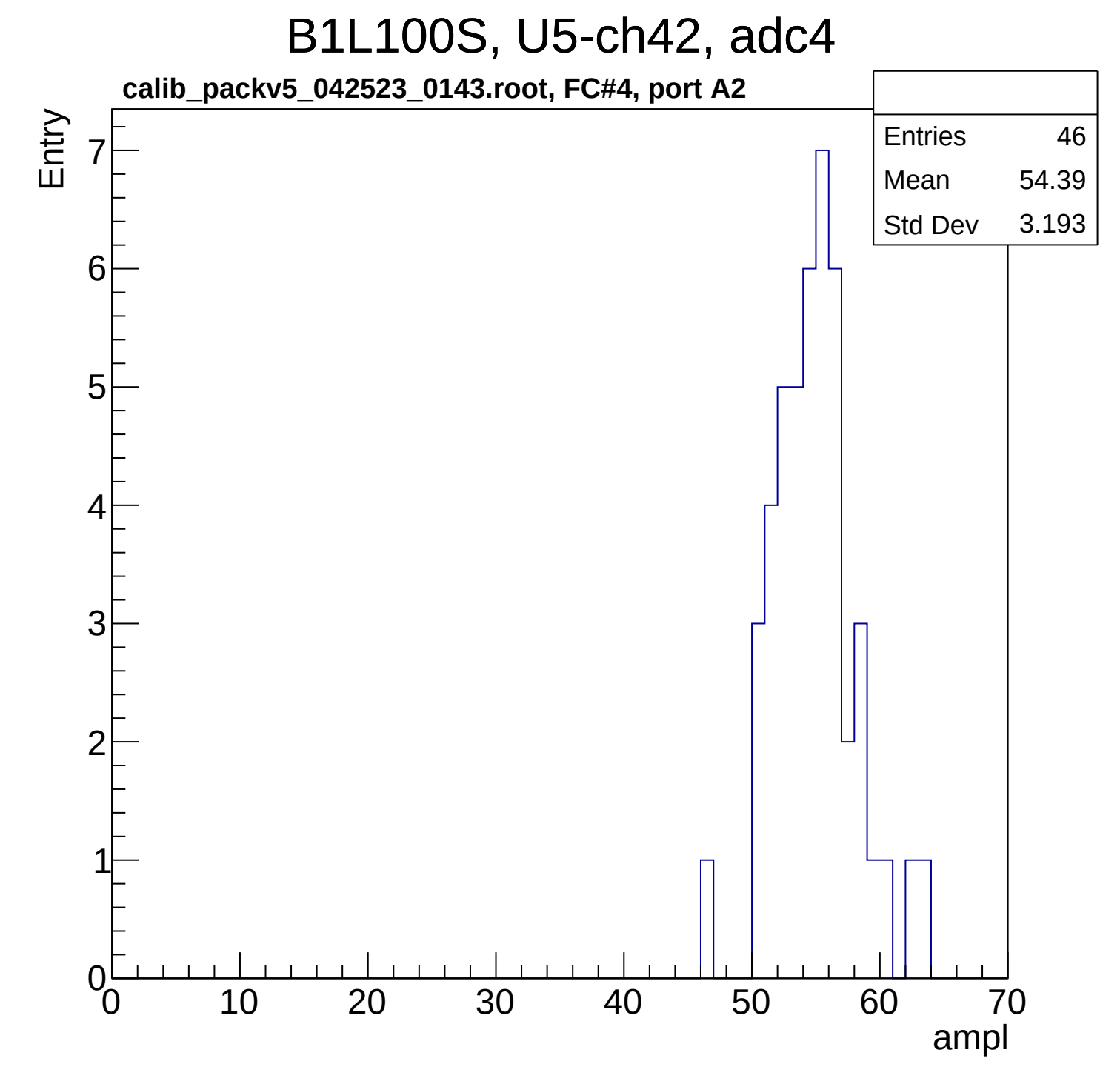
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

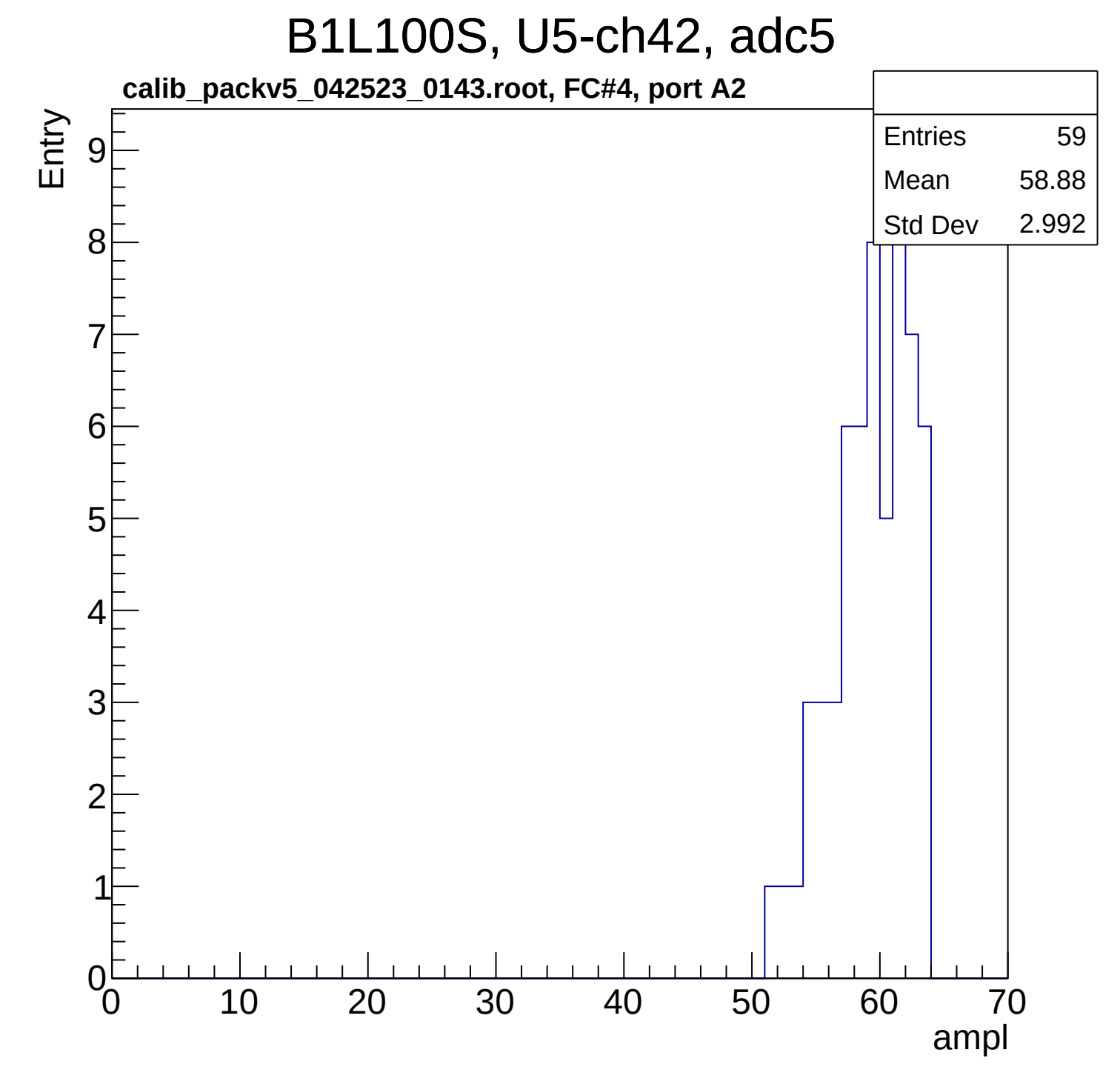

B1L100S, U5-ch42, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 29.25
Std Dev 3.307
Gaus mean : 29.3282
Gaus Width: 3.2973
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

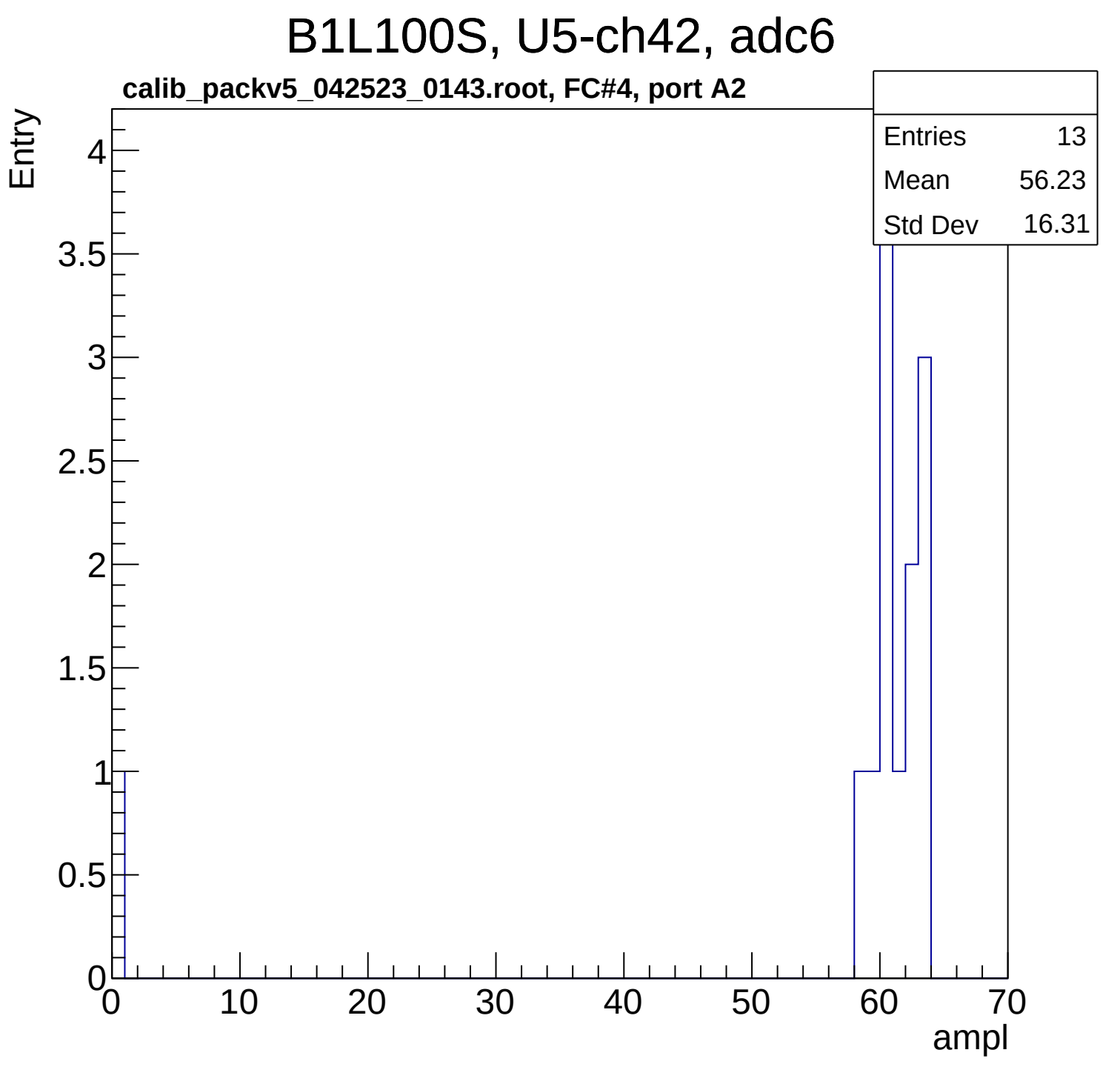

B1L100S, U5-ch42, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 35.47
Std Dev 3.515
Gaus mean : 36.0468
Gaus Width: 3.7126
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

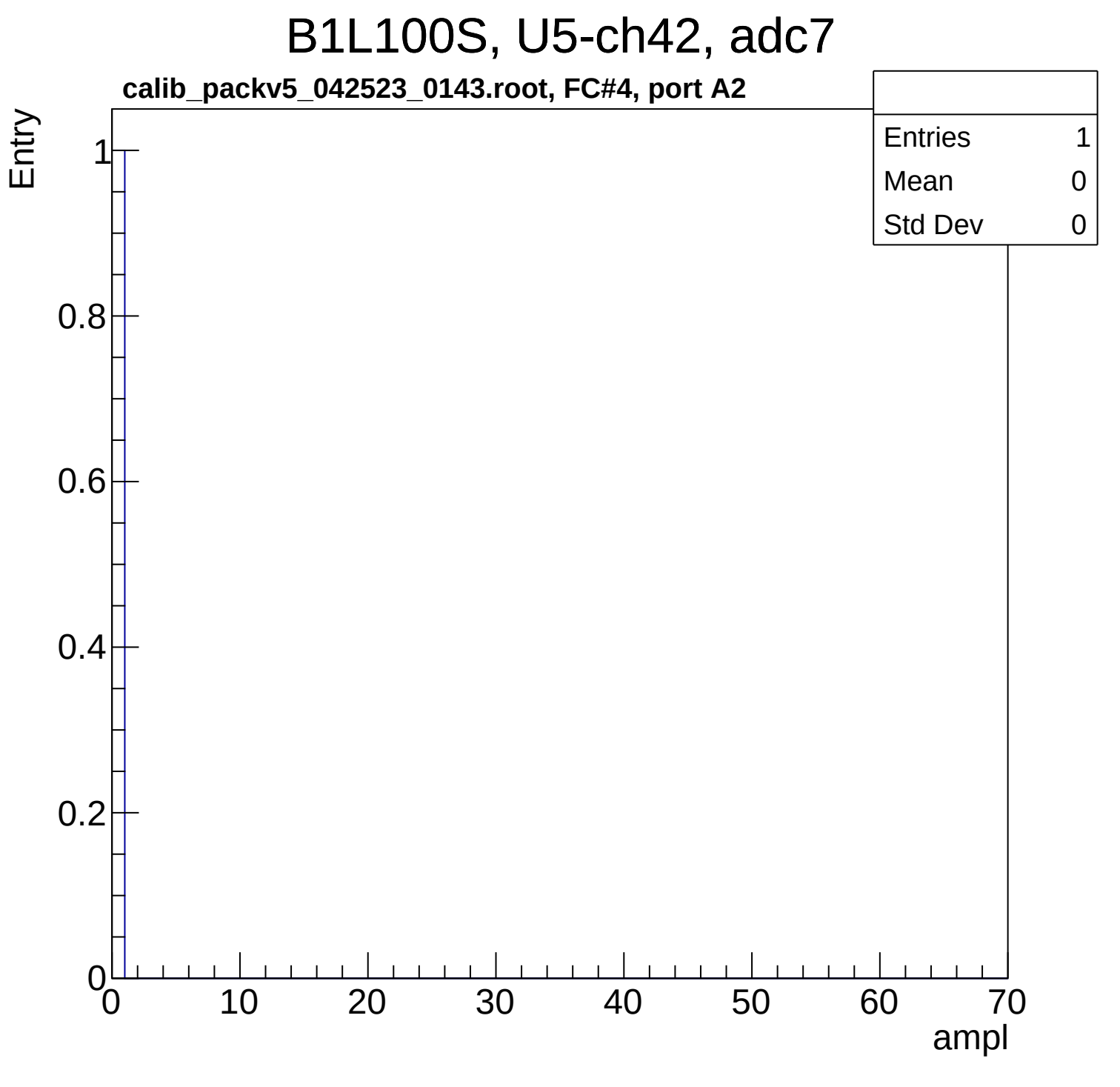

B1L100S, U5-ch42, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 41.17
Std Dev 3.687
Gaus mean : 41.7604
Gaus Width: 4.0712
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

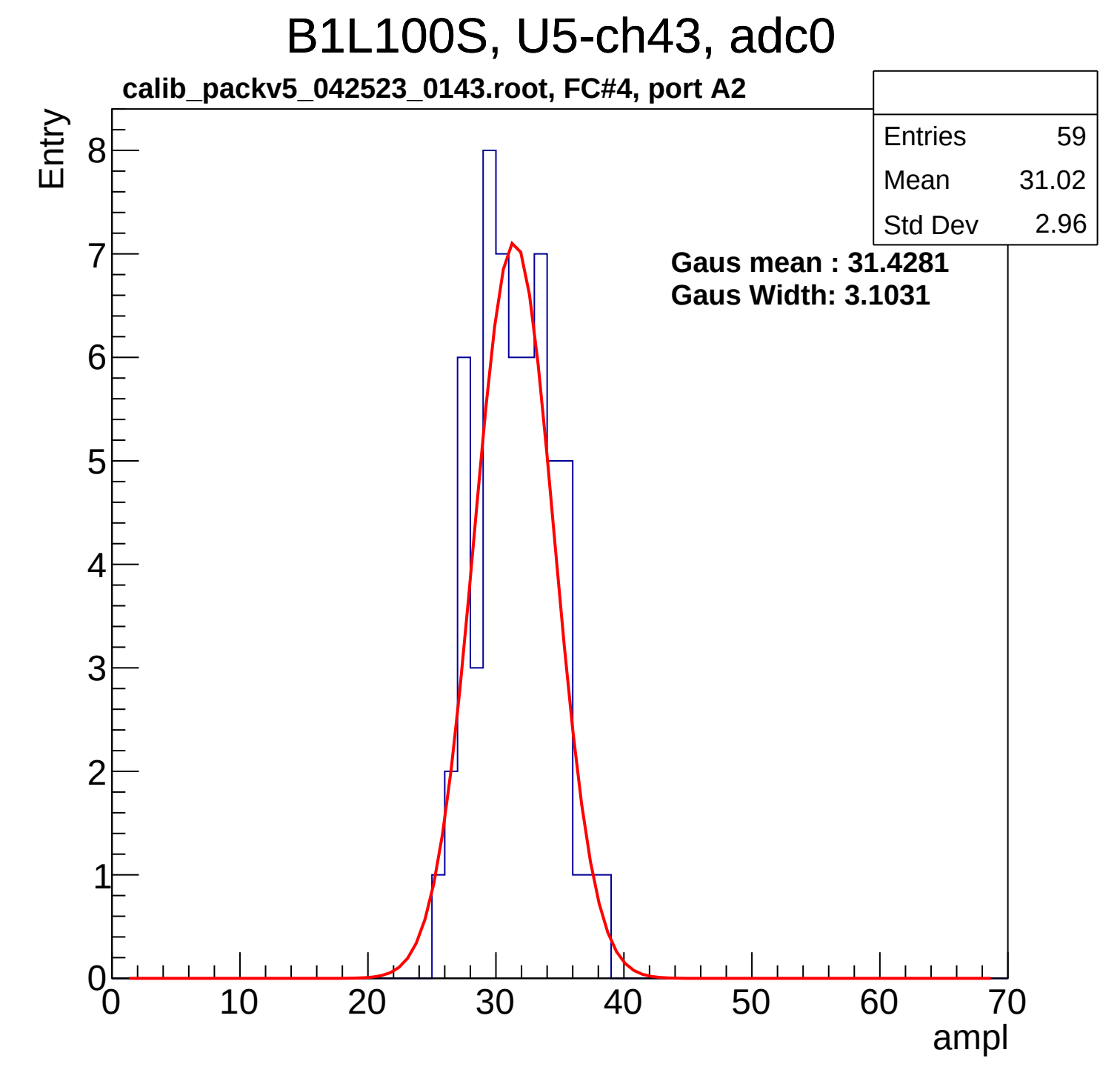

B1L100S, U5-ch42, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 48.2
Std Dev 3.499
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

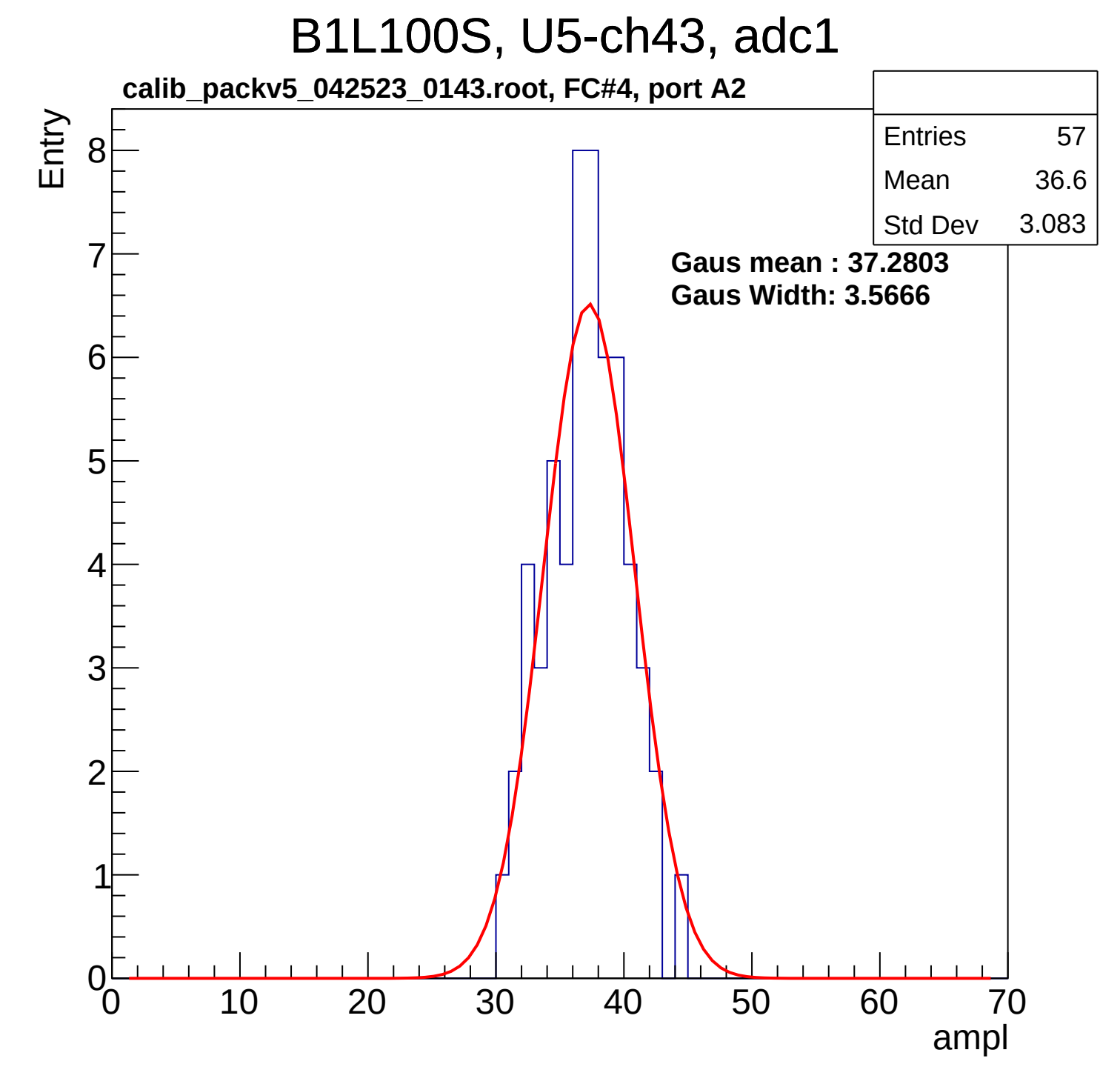

B1L100S, U5-ch42, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 46
Mean 54.39
Std Dev 3.193
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

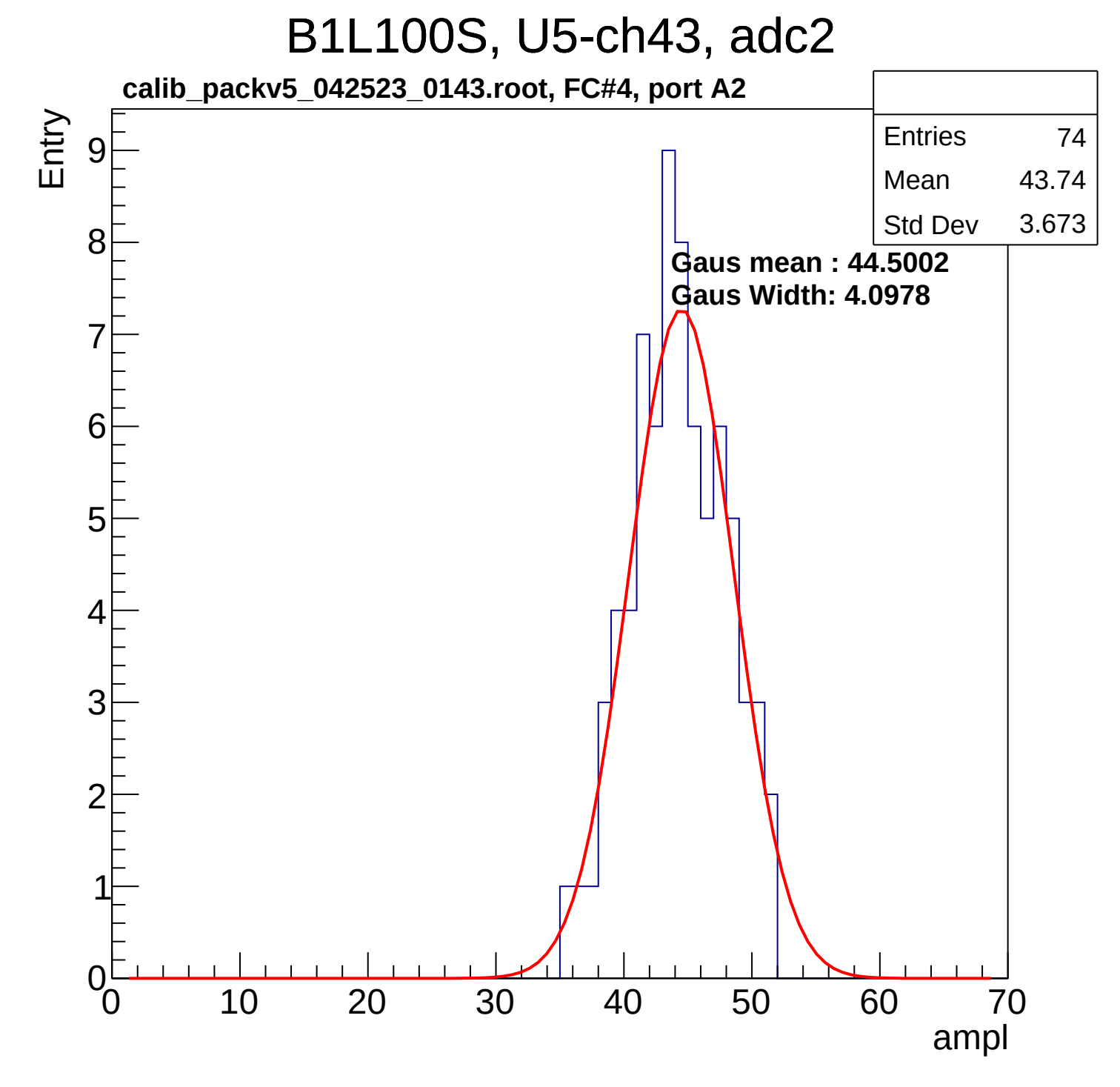

B1L100S, U5-ch42, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 58.88
Std Dev 2.992
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch42, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 13
Mean 56.23
Std Dev 16.31
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L100S, U5-ch42, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch43, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 31.02
Std Dev 2.96
Gaus mean : 31.4281
Gaus Width: 3.1031
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch43, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 36.6
Std Dev 3.083
Gaus mean : 37.2803
Gaus Width: 3.5666
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch43, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 74
Mean 43.74
Std Dev 3.673
Gaus mean : 44.5002
Gaus Width: 4.0978
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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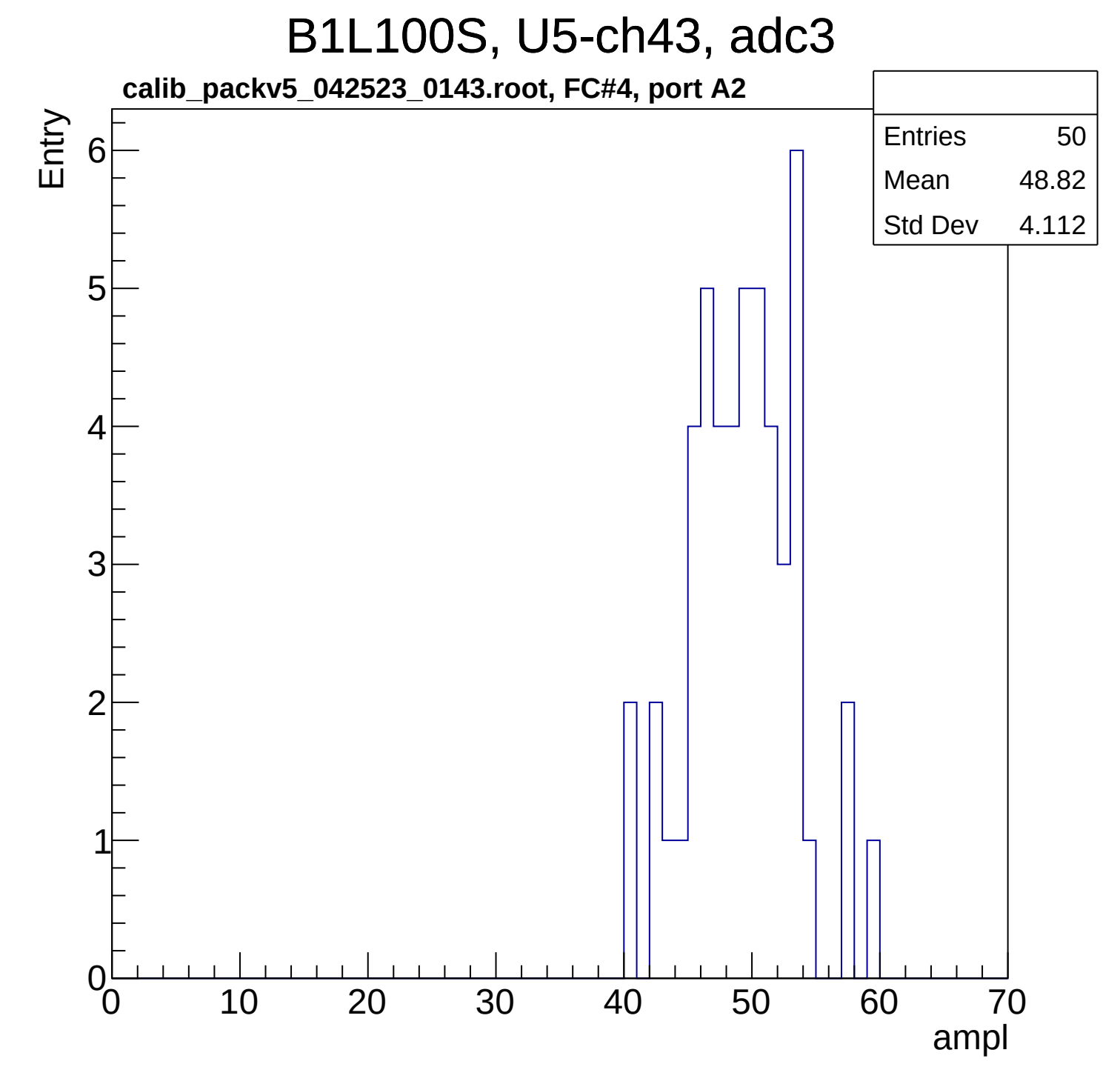
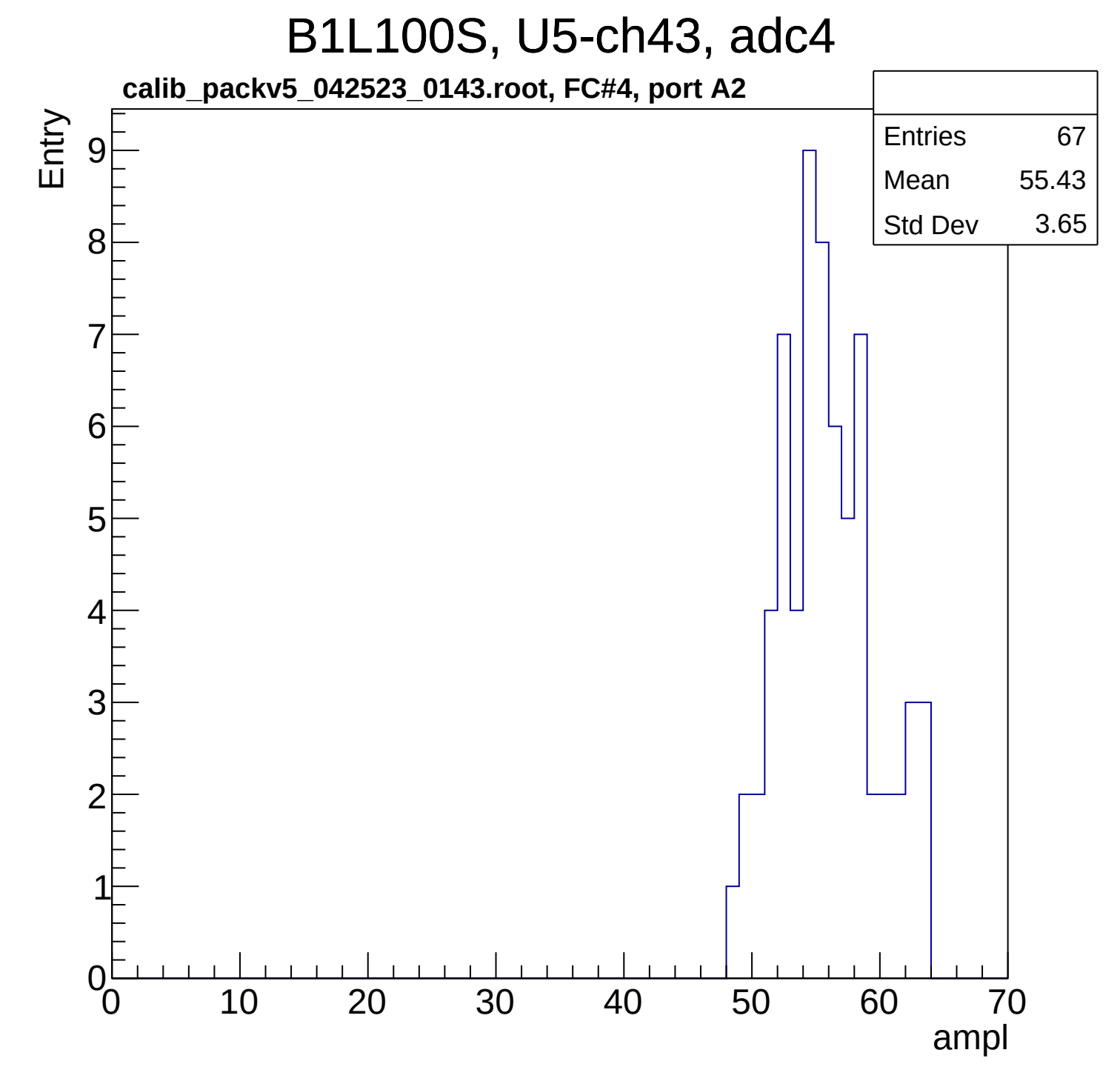

B1L100S, U5-ch43, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 48.82
Std Dev 4.112
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L100S, U5-ch43, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 55.43
Std Dev 3.65
Entry
ampl
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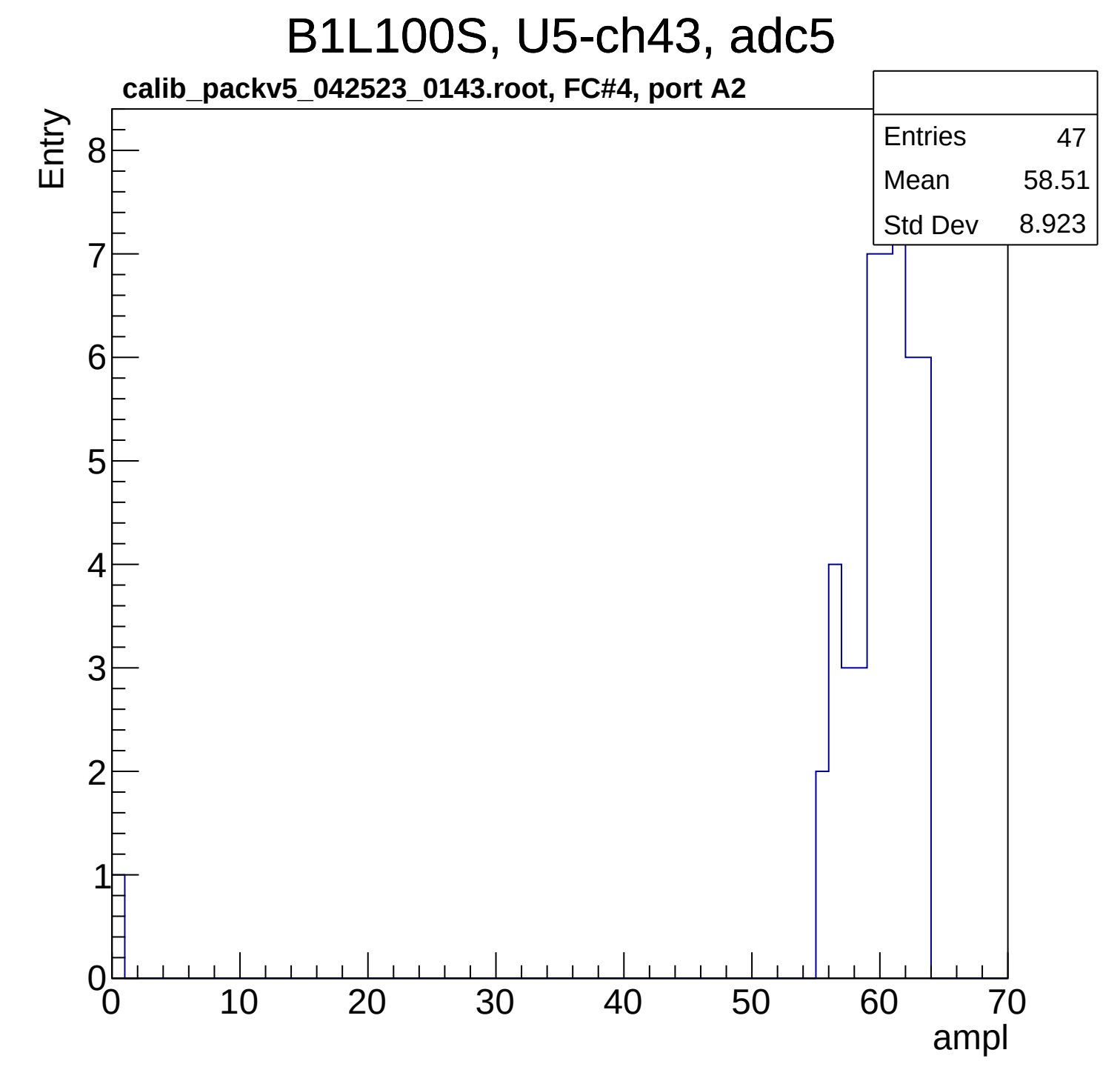
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch43, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 47
Mean 58.51
Std Dev 8.923
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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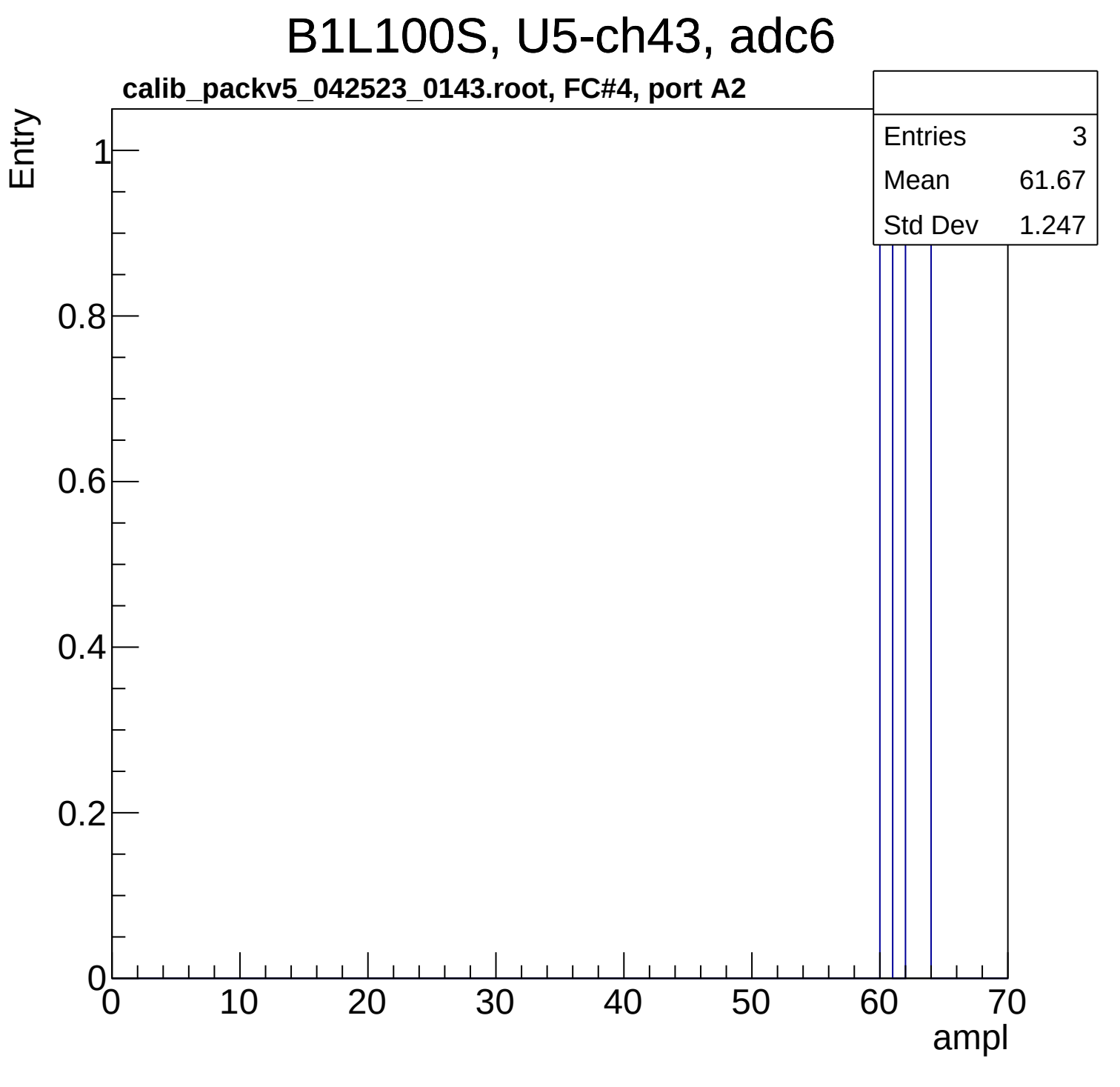
40
50
60
70


B1L100S, U5-ch43, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 61.67
Std Dev 1.247
Entry
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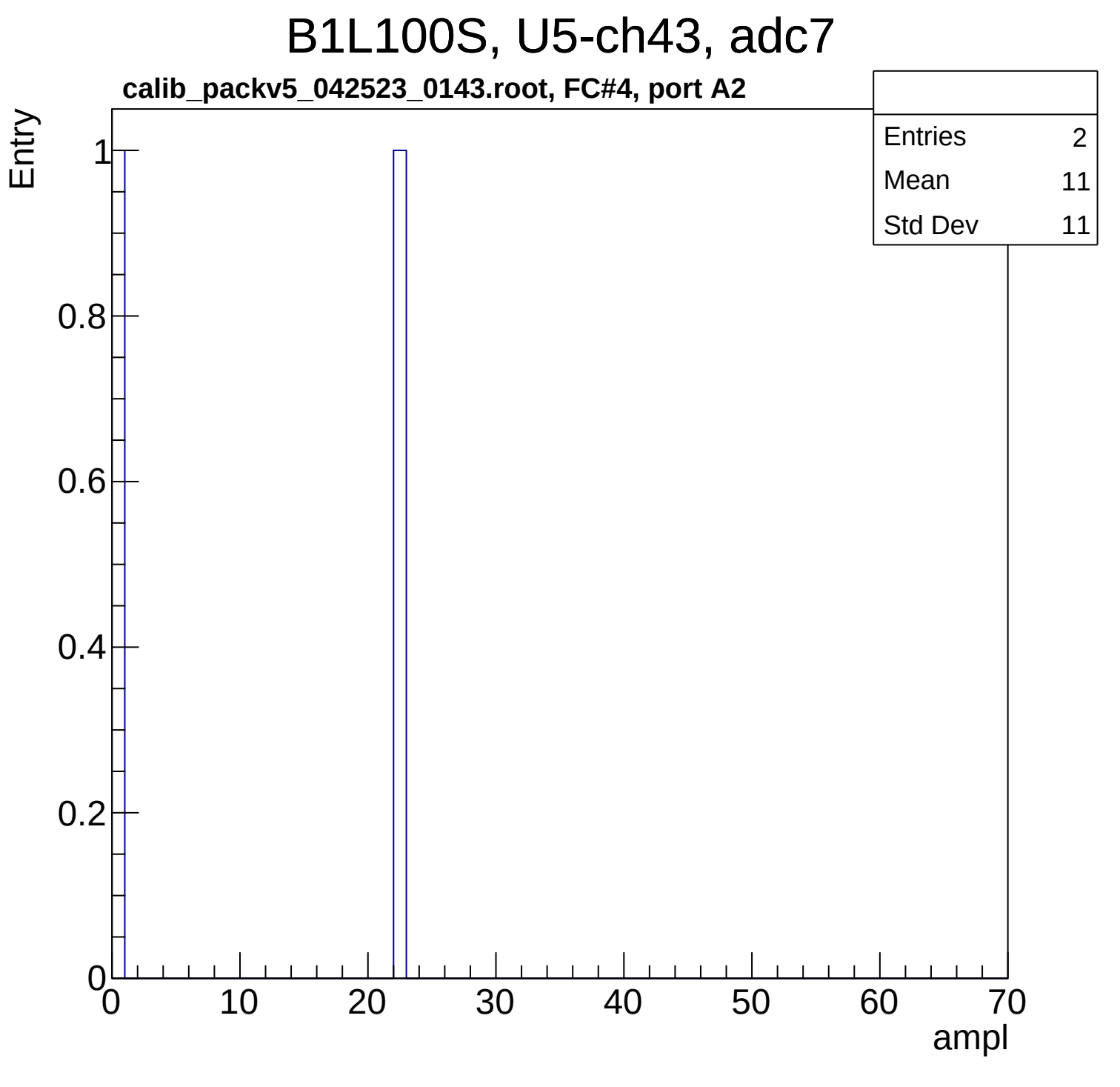
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch43, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 11
Std Dev 11
Entry
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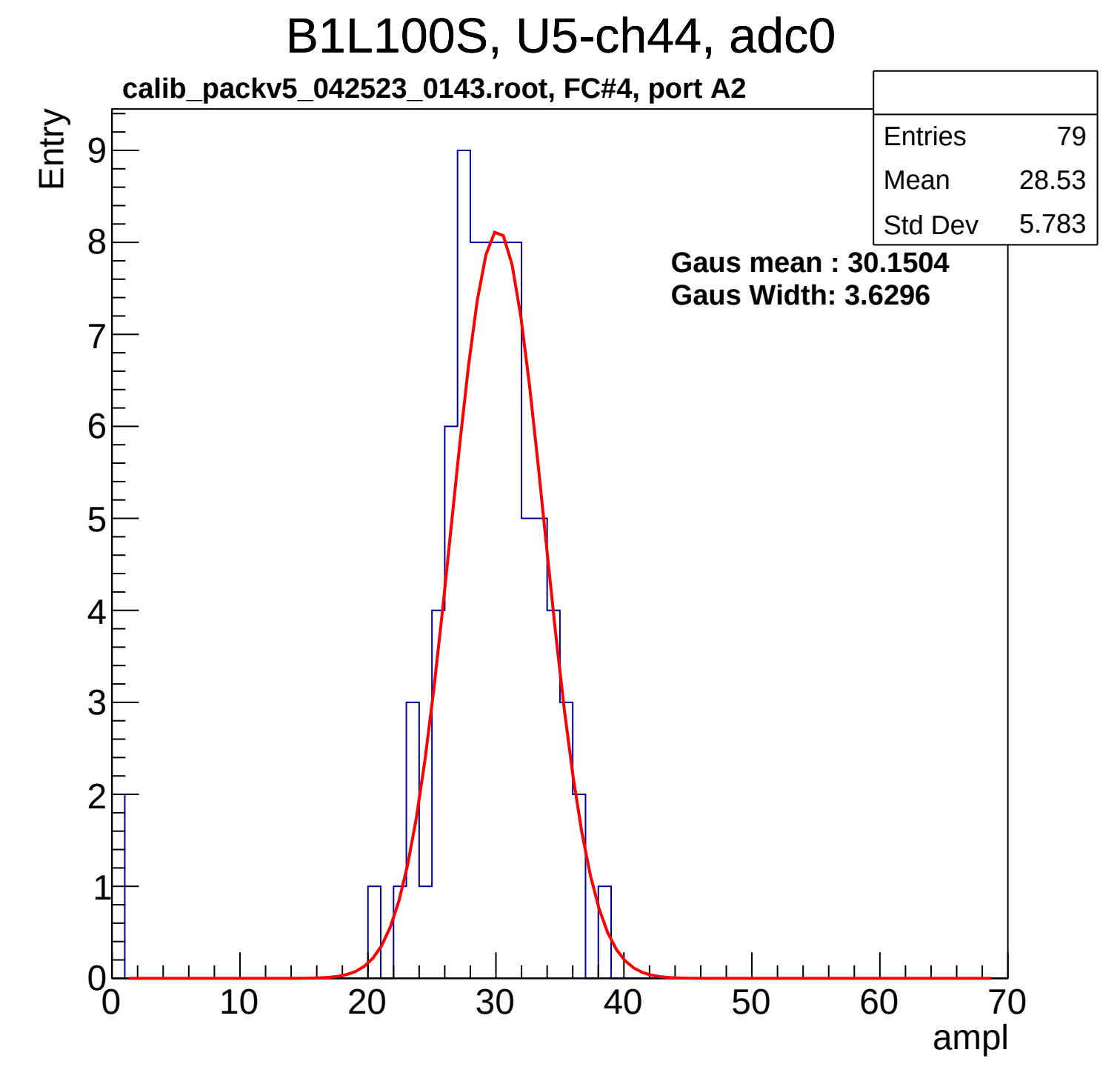
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch44, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 79
Mean 28.53
Std Dev 5.783
Gaus mean : 30.1504
Gaus Width: 3.6296
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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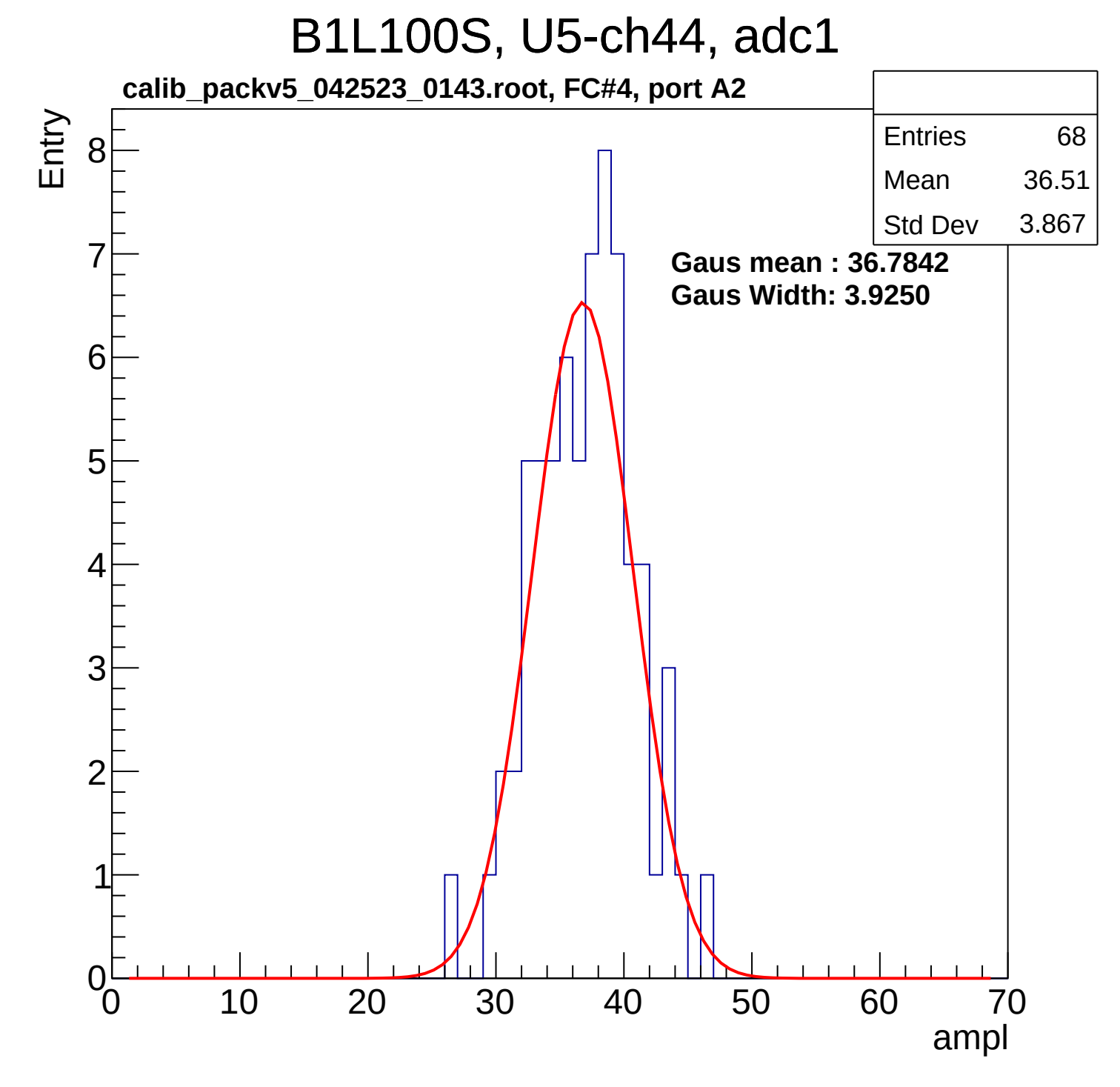
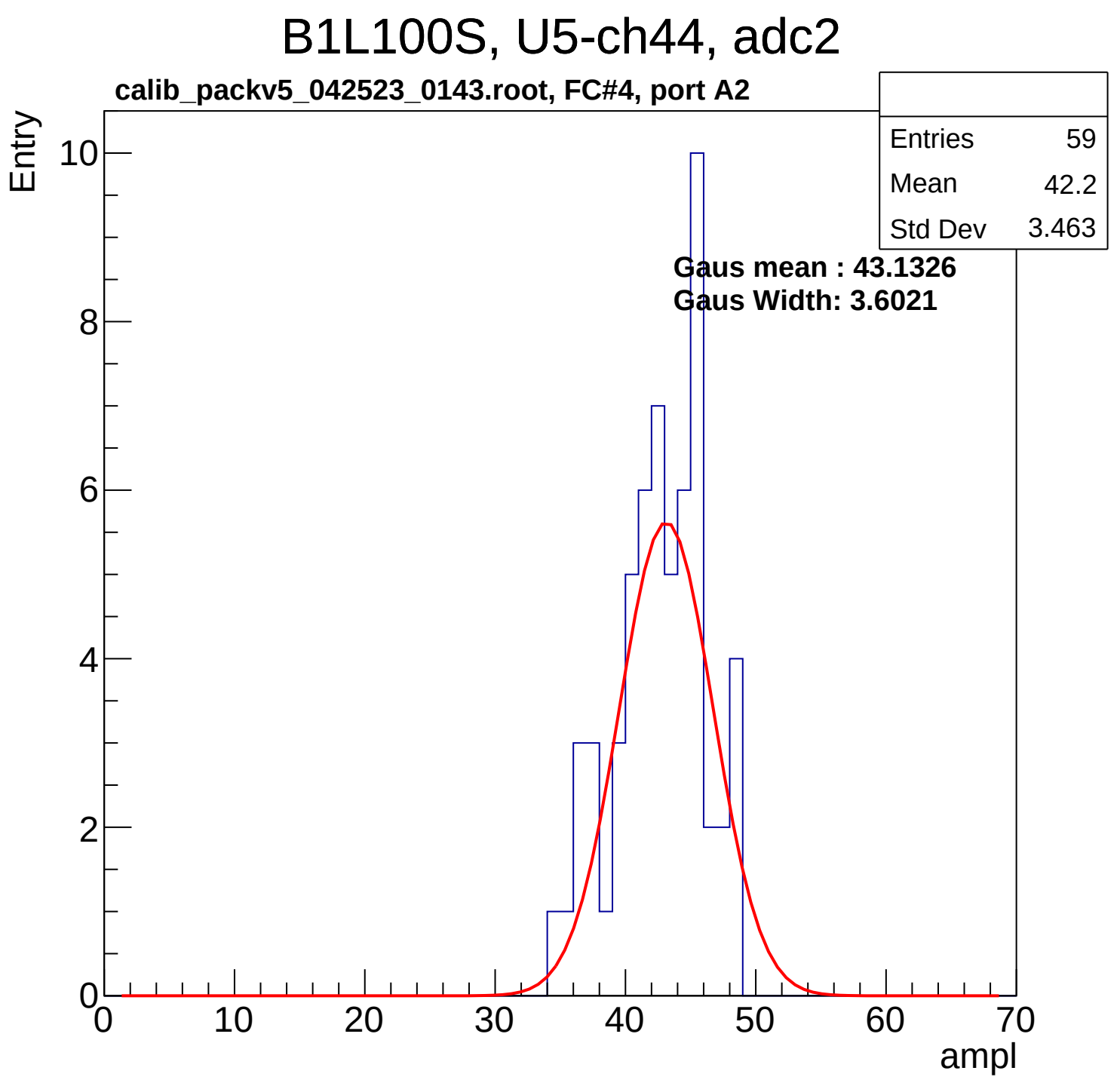
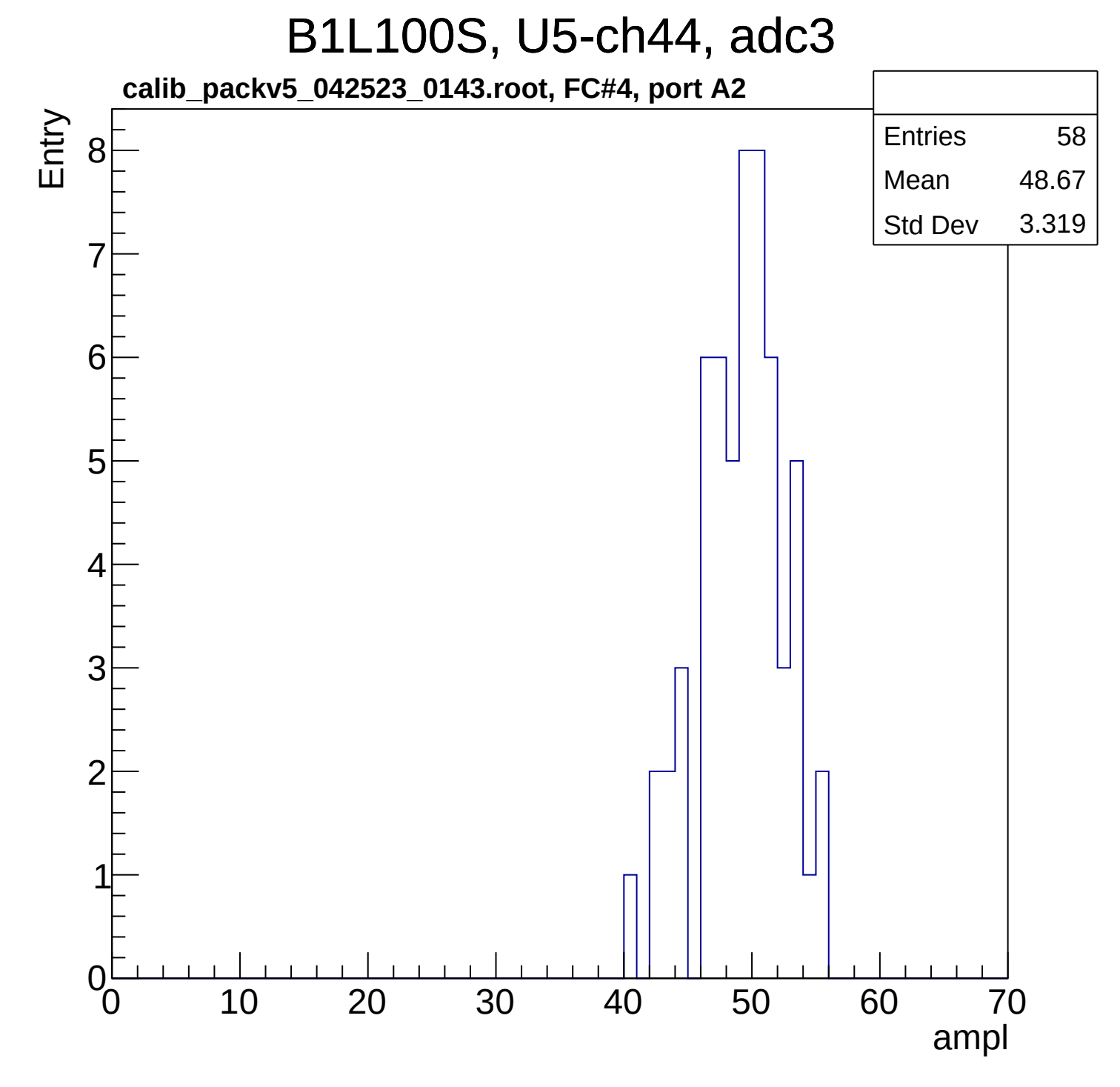
40
50
60
70


B1L100S, U5-ch44, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 36.51
Std Dev 3.867
Gaus mean : 36.7842
Gaus Width: 3.9250
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch44, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 42.2
Std Dev 3.463
Gaus mean : 43.1326
Gaus Width: 3.6021
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch44, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 48.67
Std Dev 3.319
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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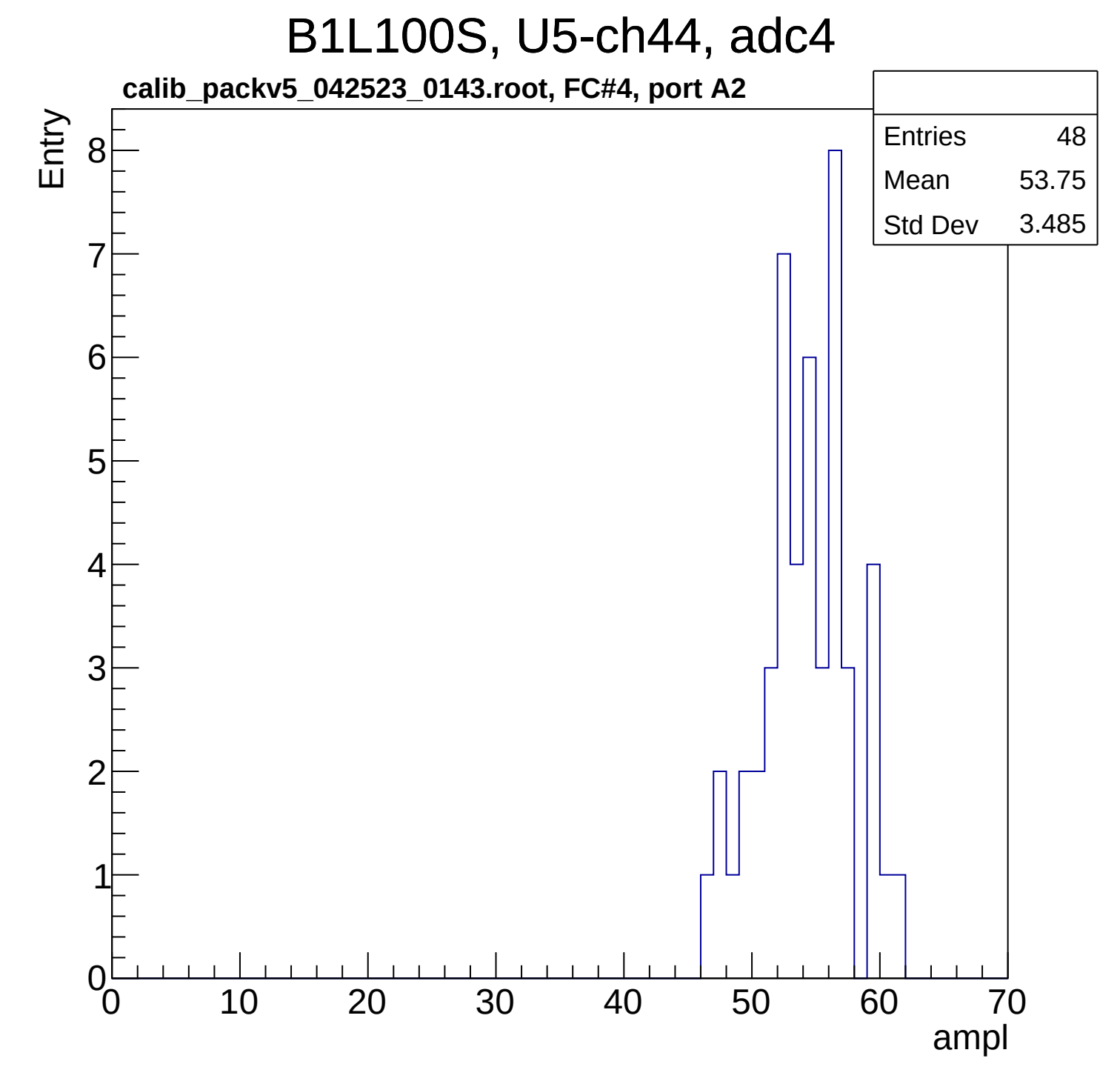
B1L100S, U5-ch44, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 48
Mean 53.75
Std Dev 3.485
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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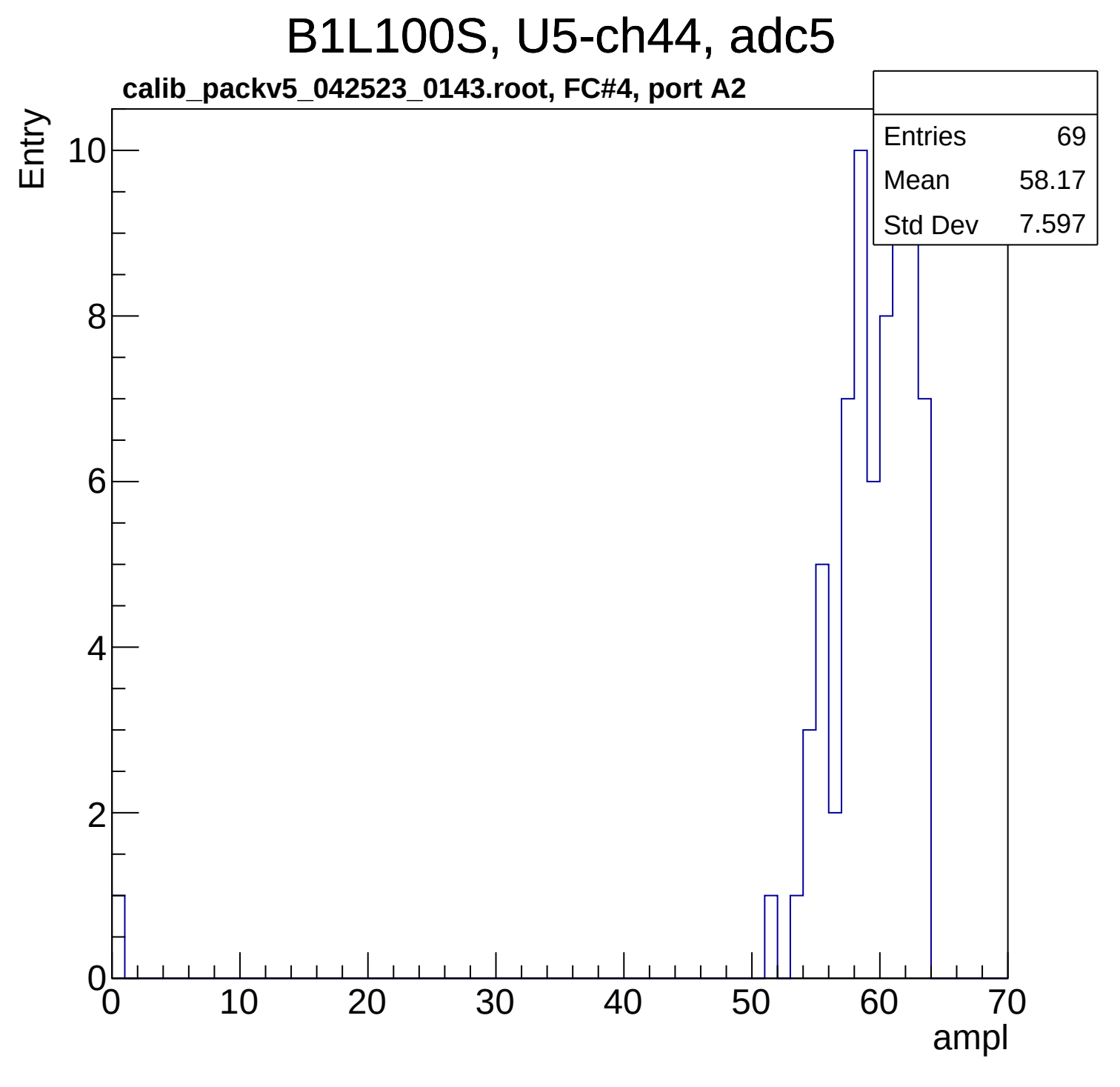
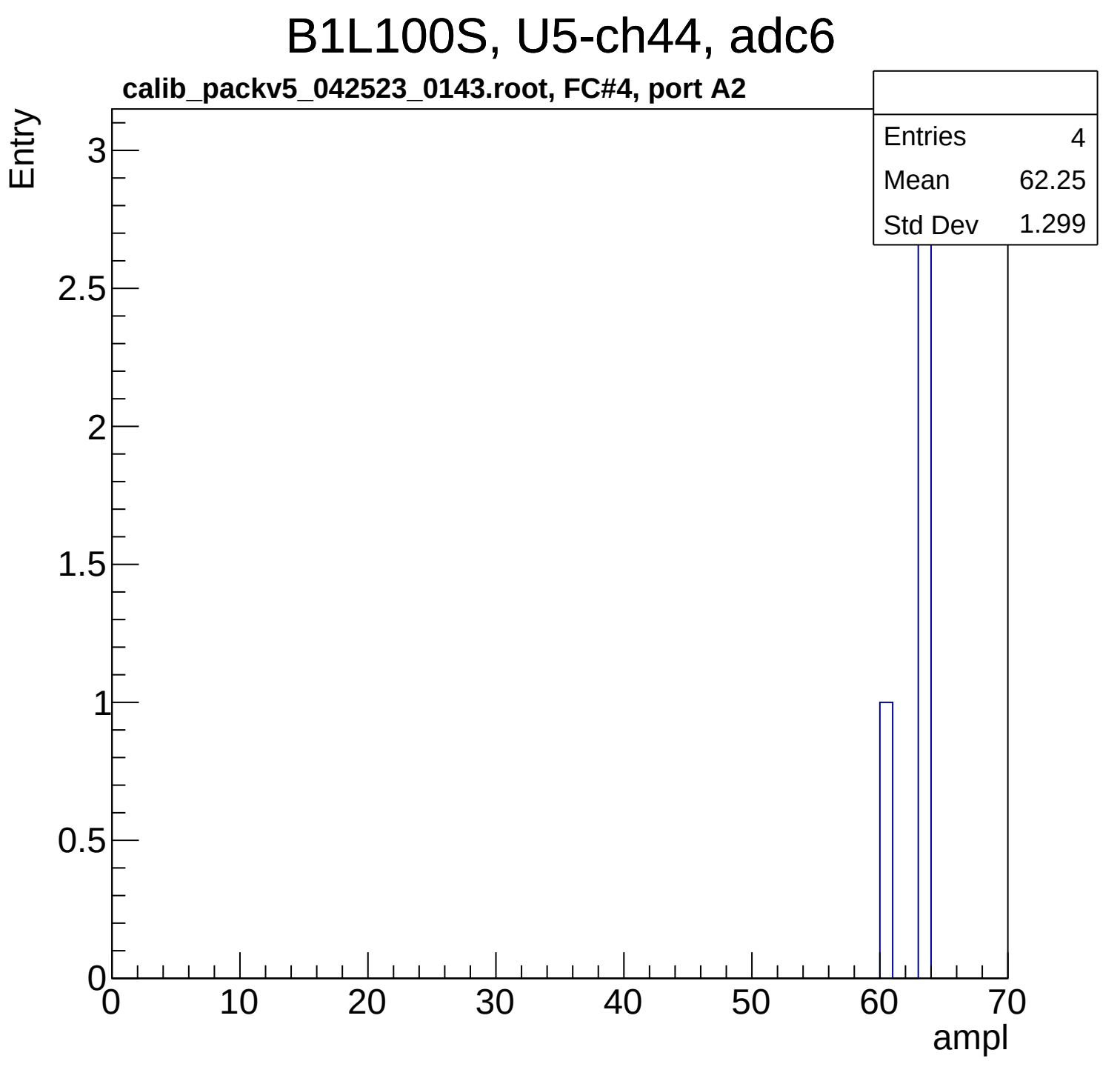

B1L100S, U5-ch44, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 58.17
Std Dev 7.597
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch44, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 4
Mean 62.25
Std Dev 1.299
Entry
ampl
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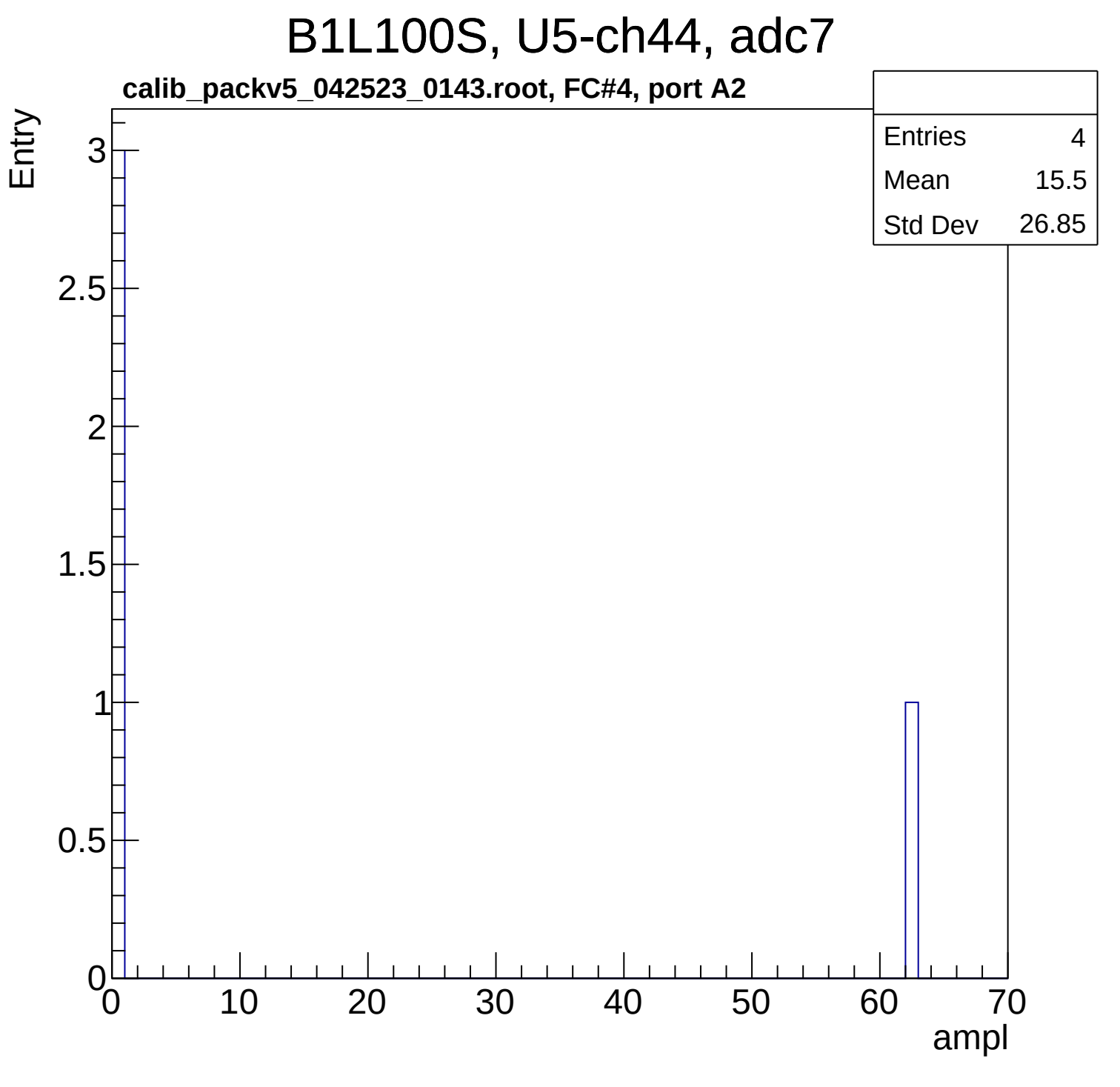
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L100S, U5-ch44, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 4
Mean 15.5
Std Dev 26.85
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
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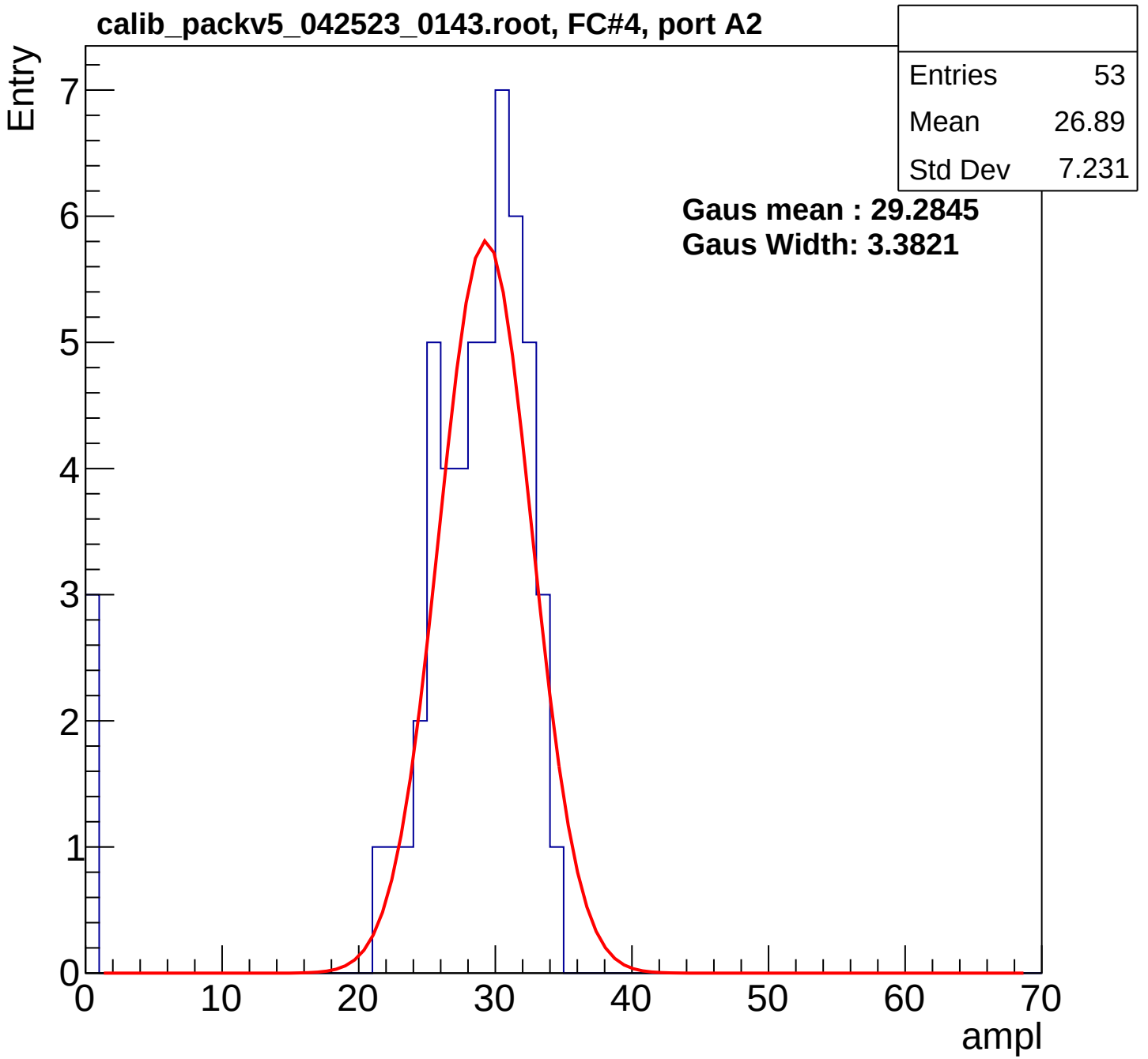
B1L100S, U5-ch45, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 26.89
Std Dev 7.231
Gaus mean : 29.2845
Gaus Width: 3.3821
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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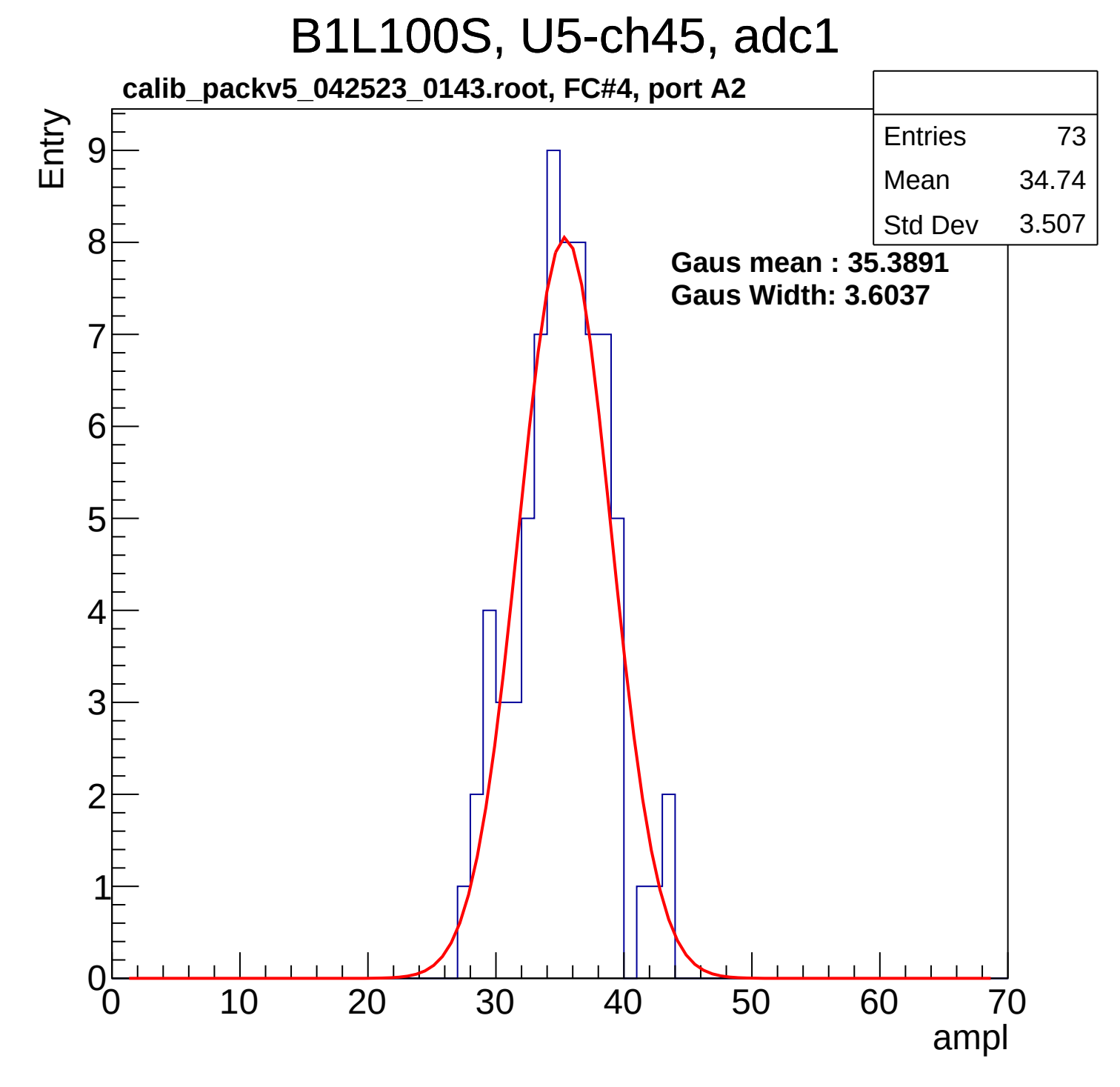
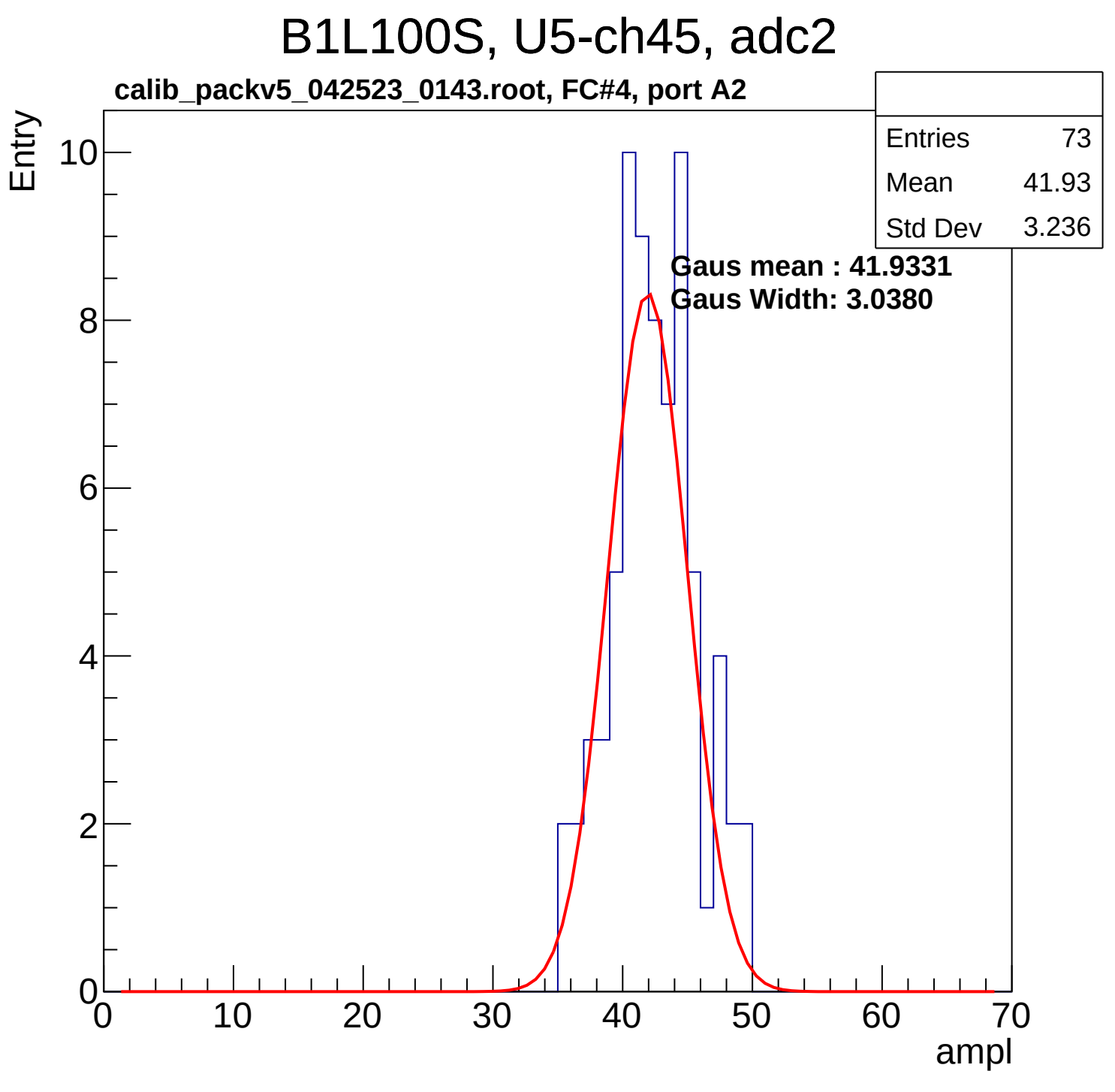
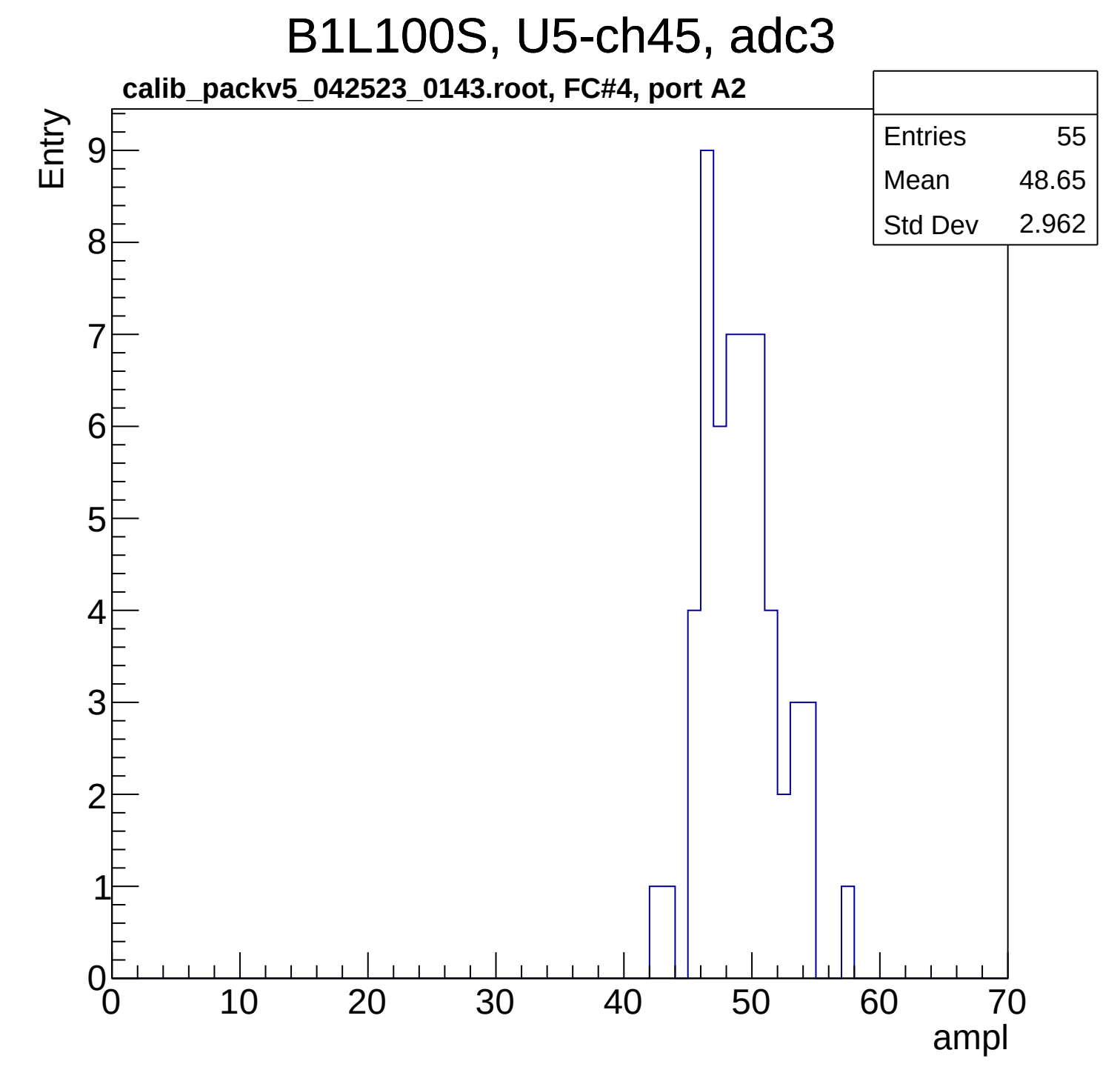
40
50
60
70


B1L100S, U5-ch45, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 34.74
Std Dev 3.507
Gaus mean : 35.3891
Gaus Width: 3.6037
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch45, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 41.93
Std Dev 3.236
Gaus mean : 41.9331
Gaus Width: 3.0380
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch45, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 48.65
Std Dev 2.962
Entry
ampl
0
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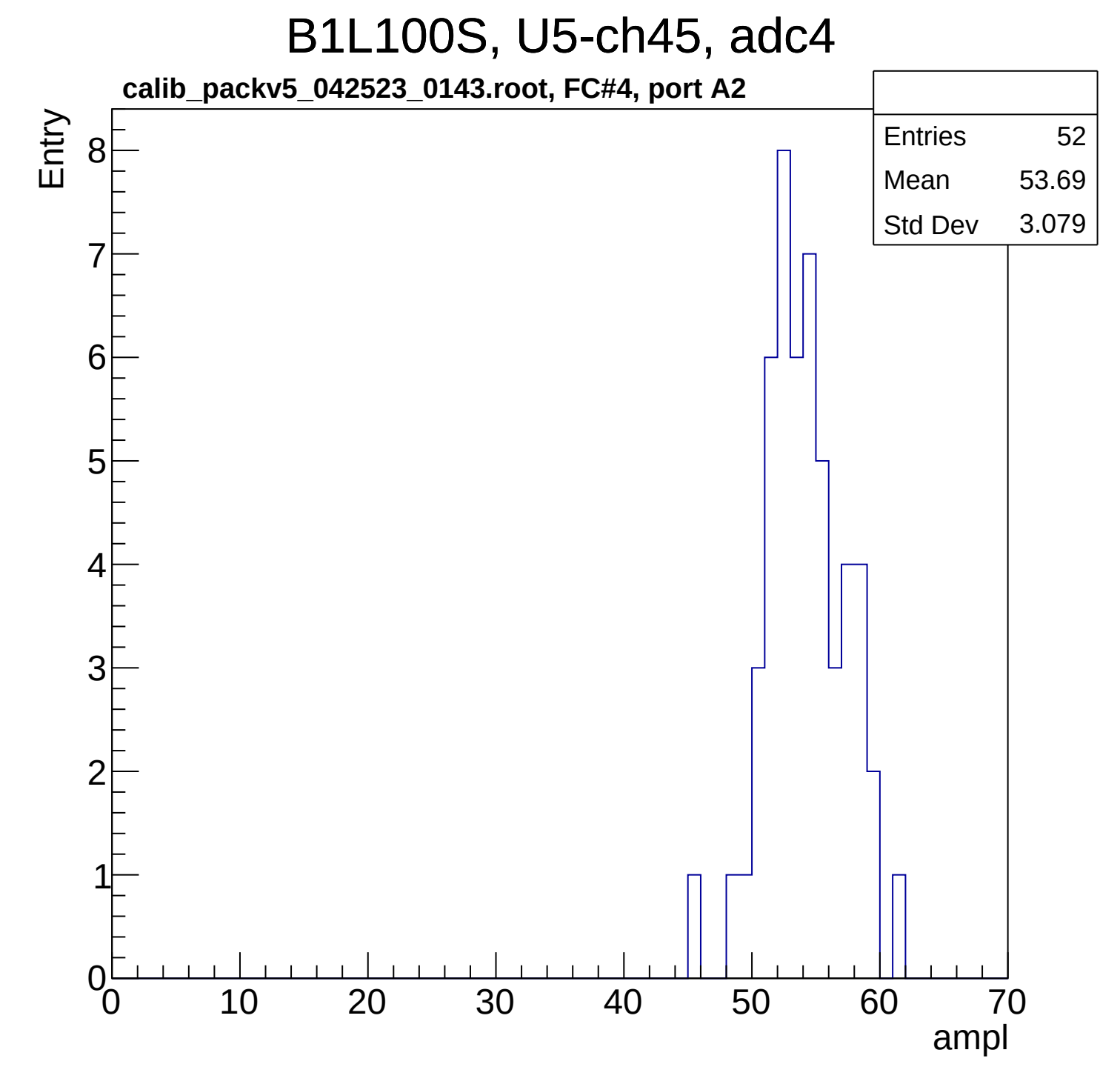
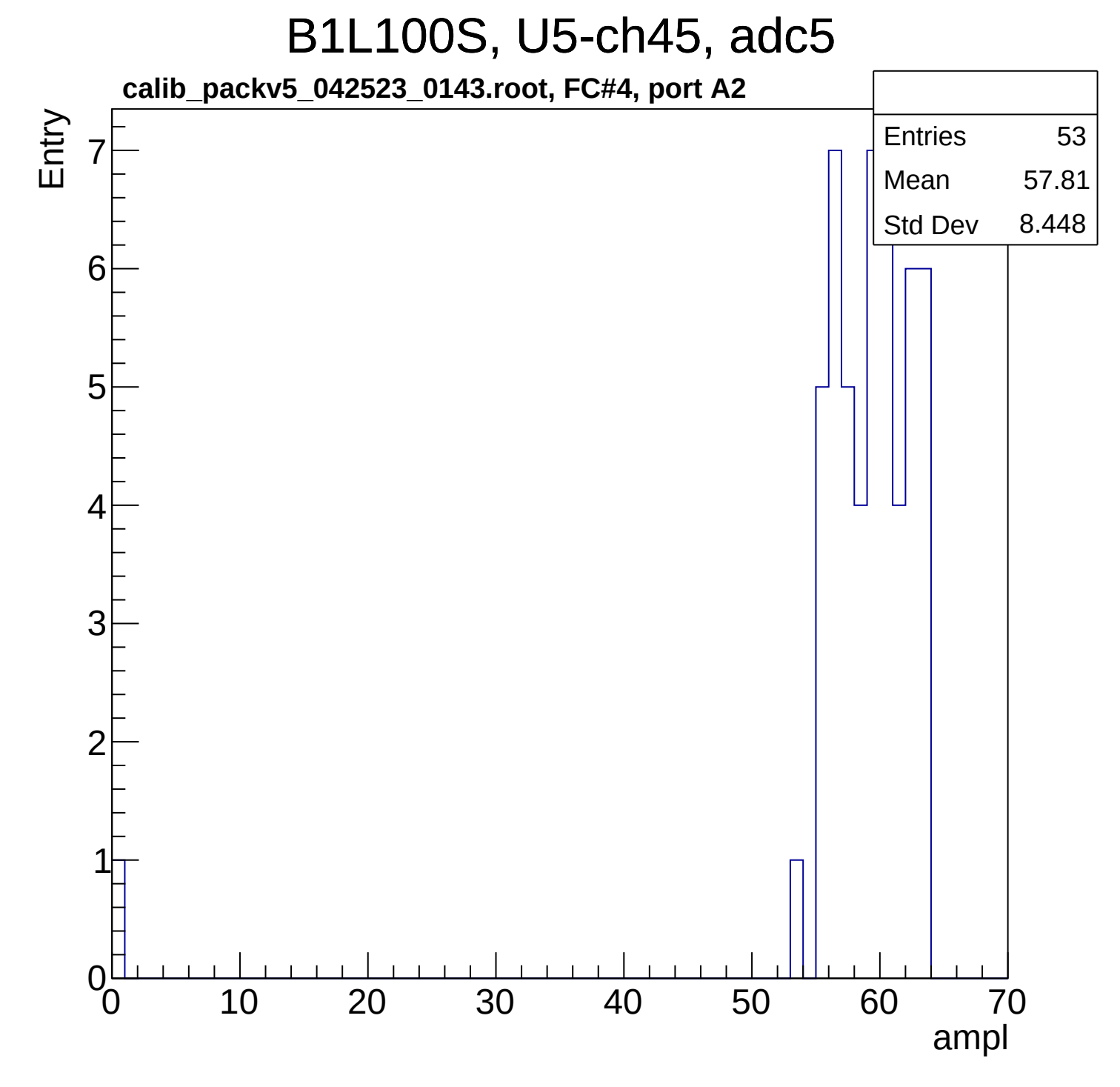
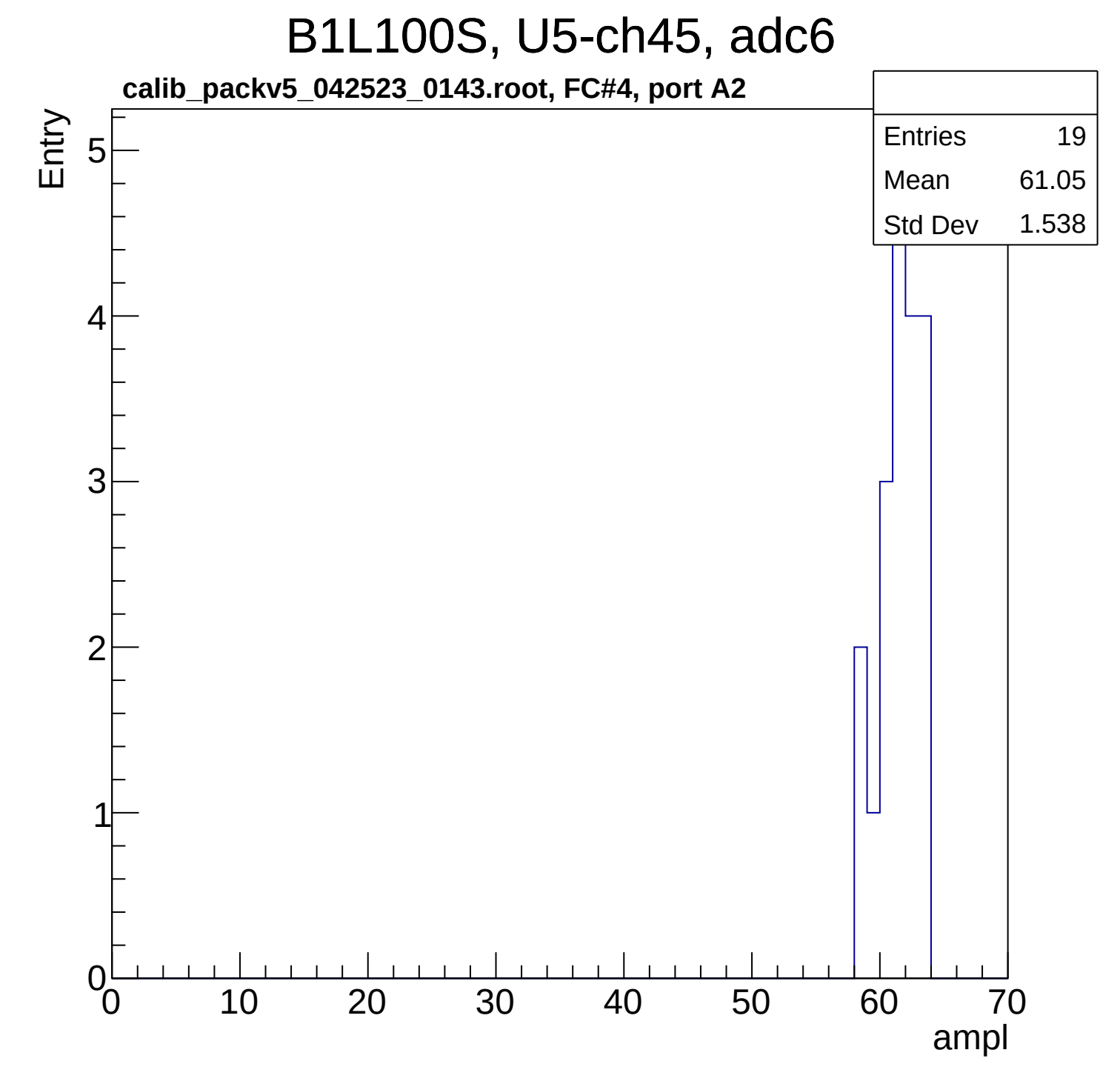
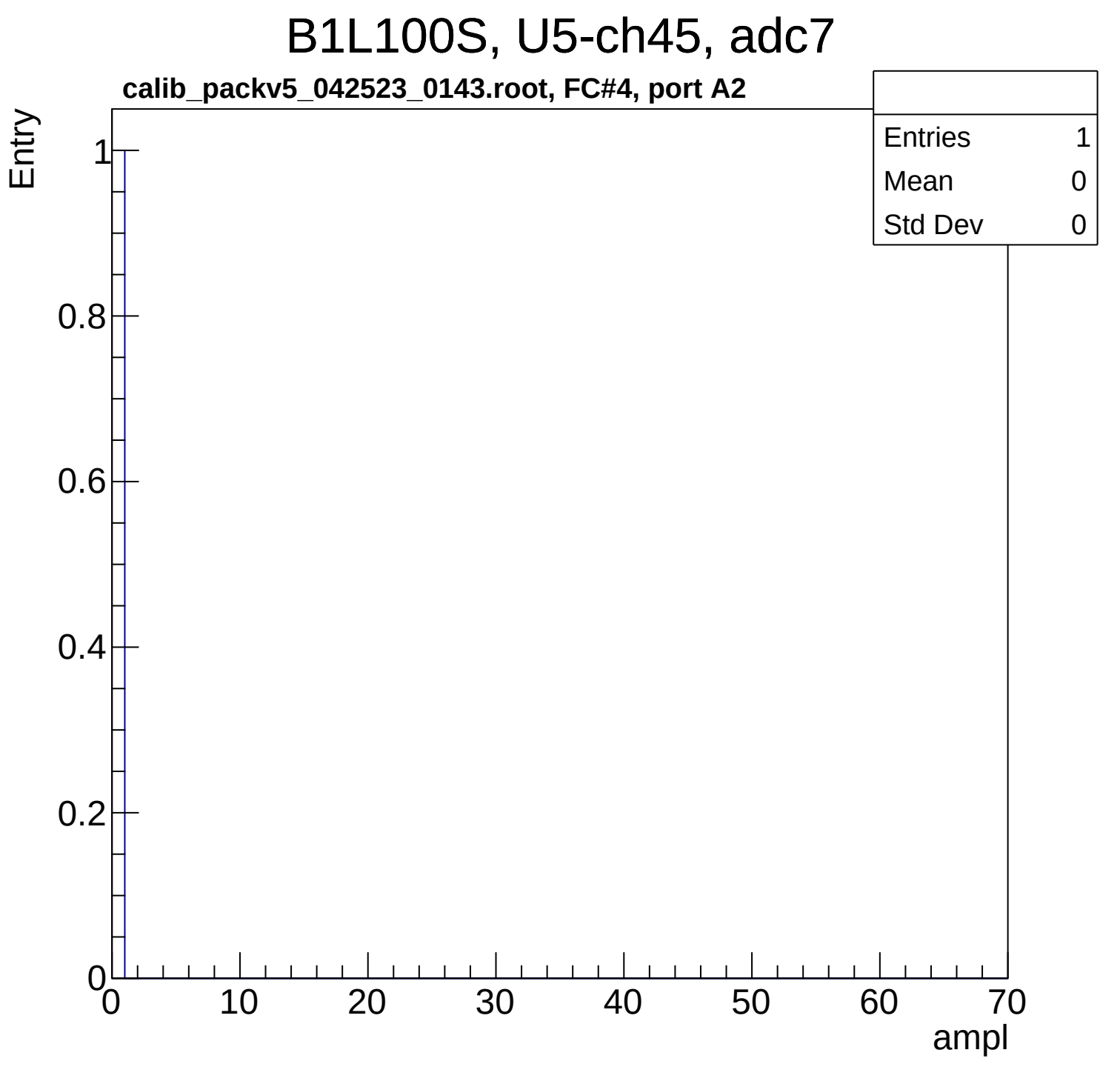
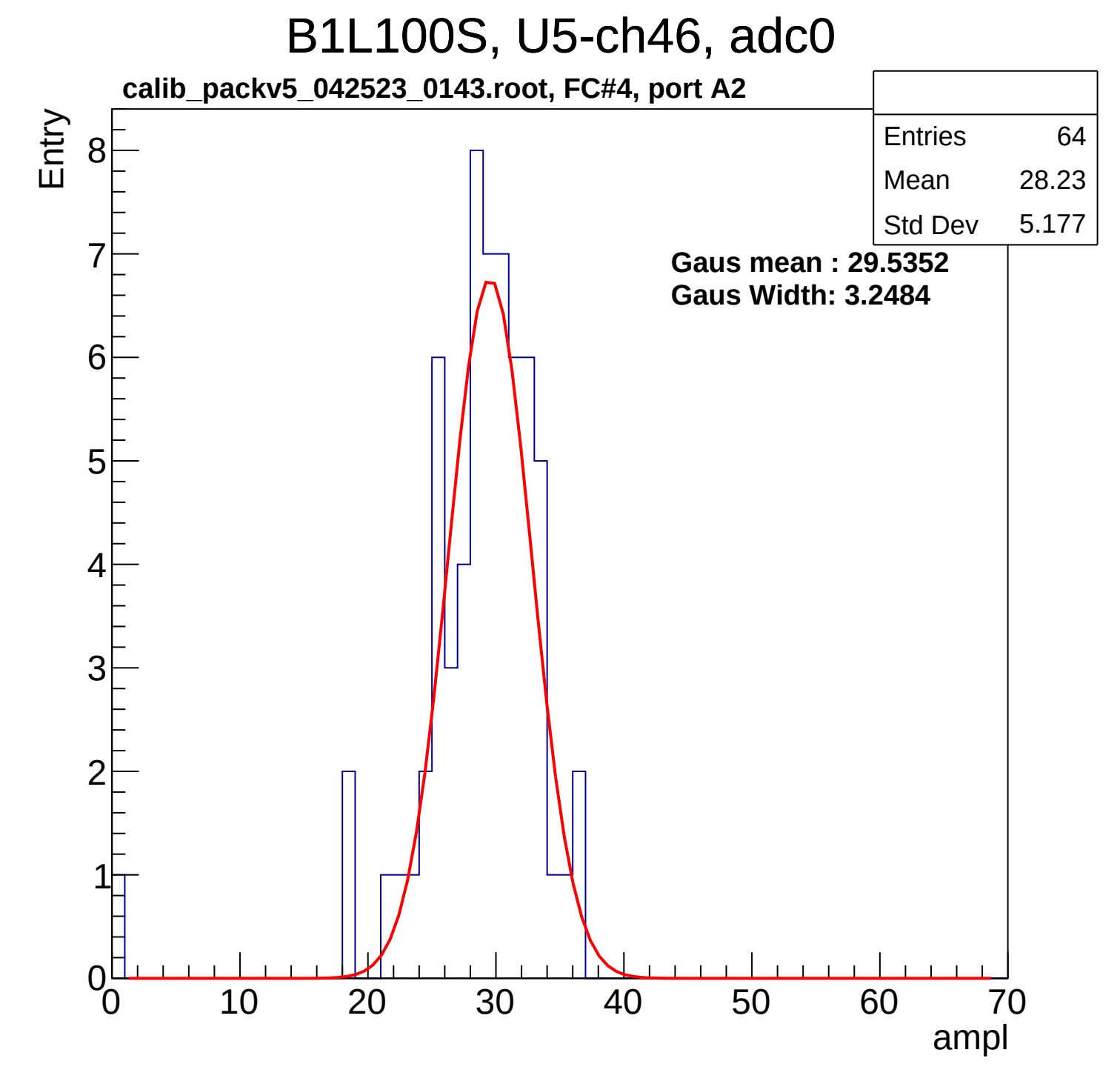
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch45, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 52
Mean 53.69
Std Dev 3.079
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch45, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 57.81
Std Dev 8.448
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U5-ch45, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 19
Mean 61.05
Std Dev 1.538
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch45, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch46, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 28.23
Std Dev 5.177
Gaus mean : 29.5352
Gaus Width: 3.2484
Entry
ampl
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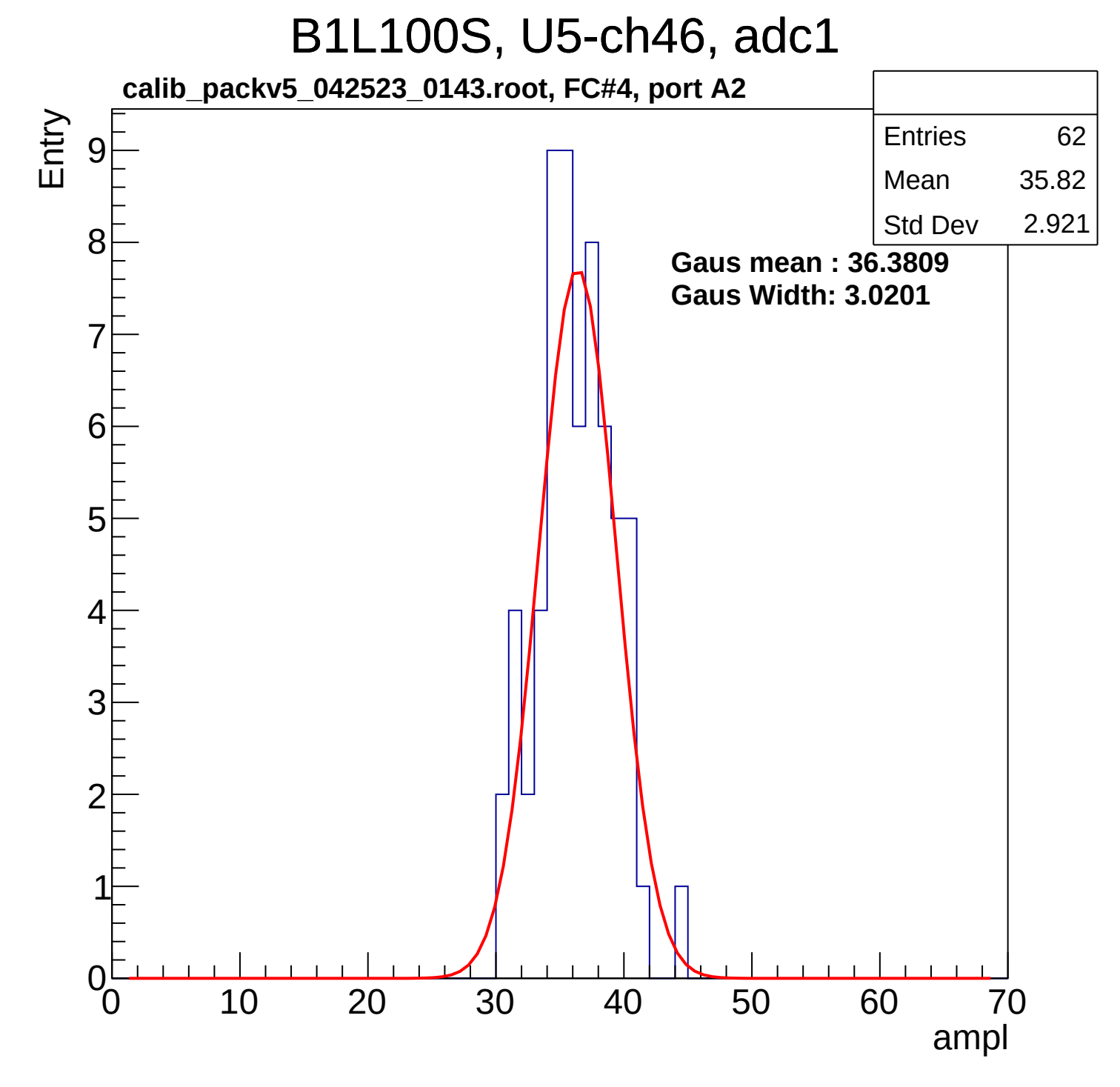
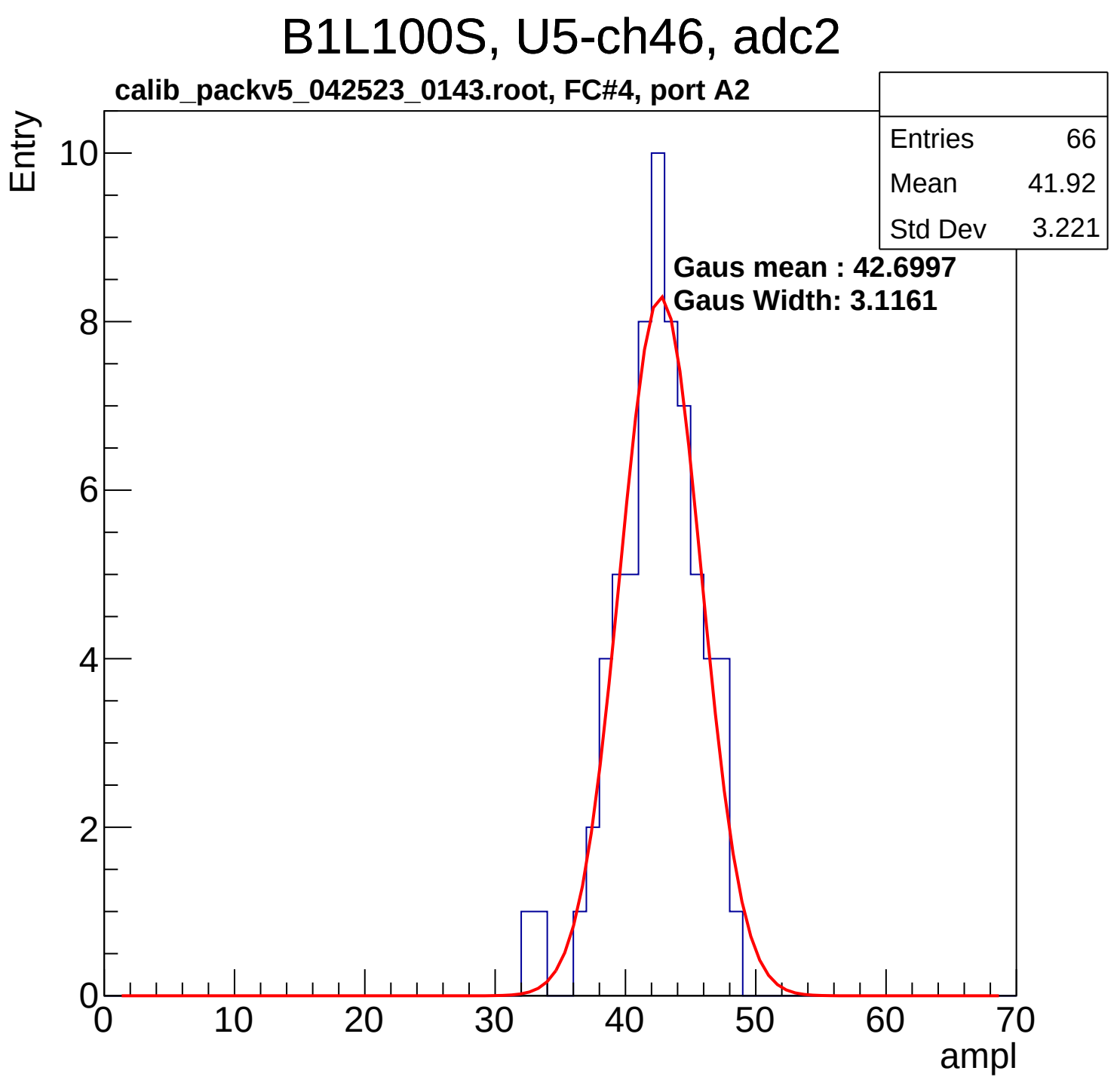
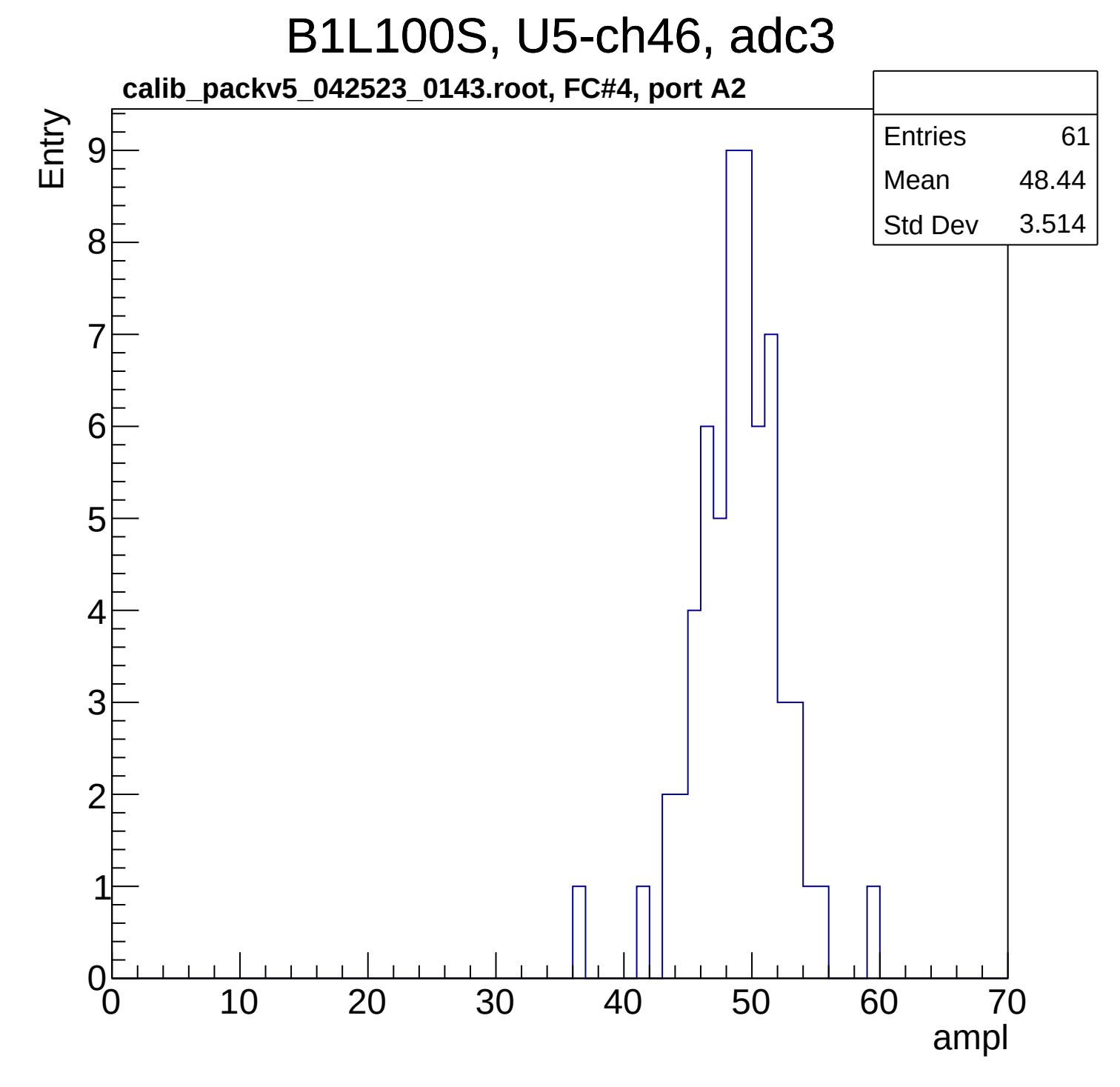
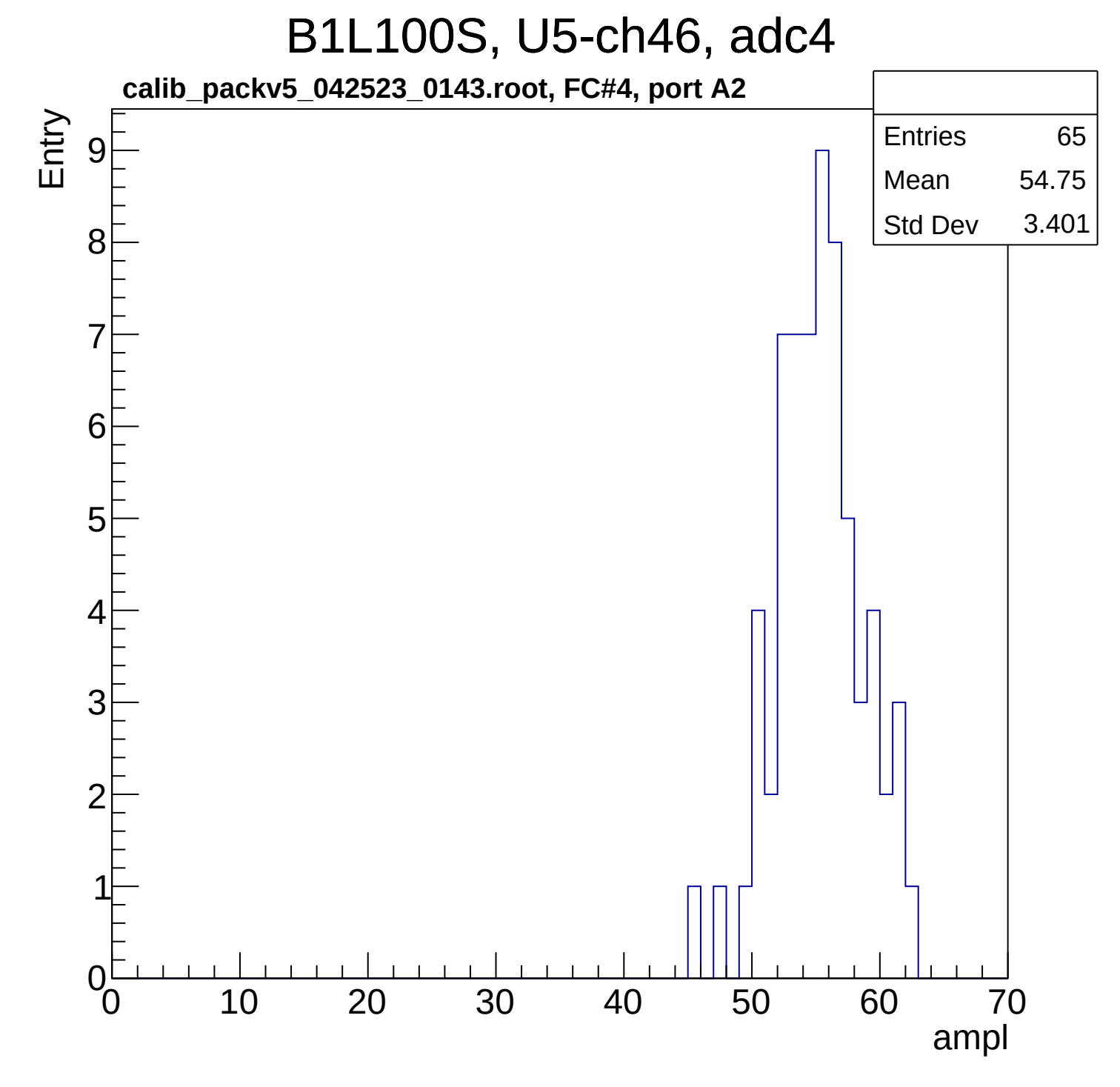
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch46, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 35.82
Std Dev 2.921
Gaus mean : 36.3809
Gaus Width: 3.0201
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch46, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 41.92
Std Dev 3.221
Gaus mean : 42.6997
Gaus Width: 3.1161
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch46, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 48.44
Std Dev 3.514
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch46, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 54.75
Std Dev 3.401
Entry
ampl
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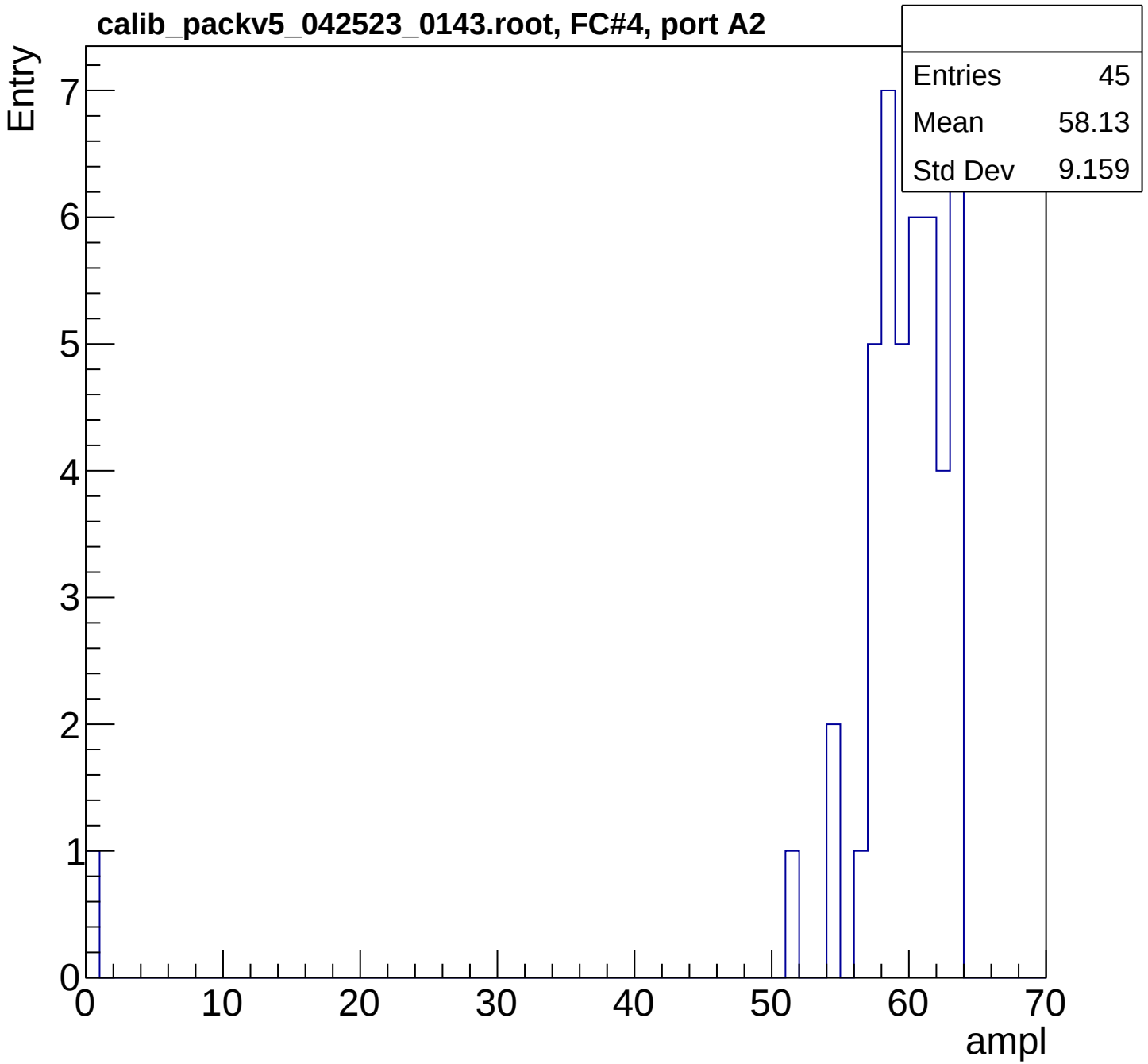
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch46, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 45
Mean 58.13
Std Dev 9.159
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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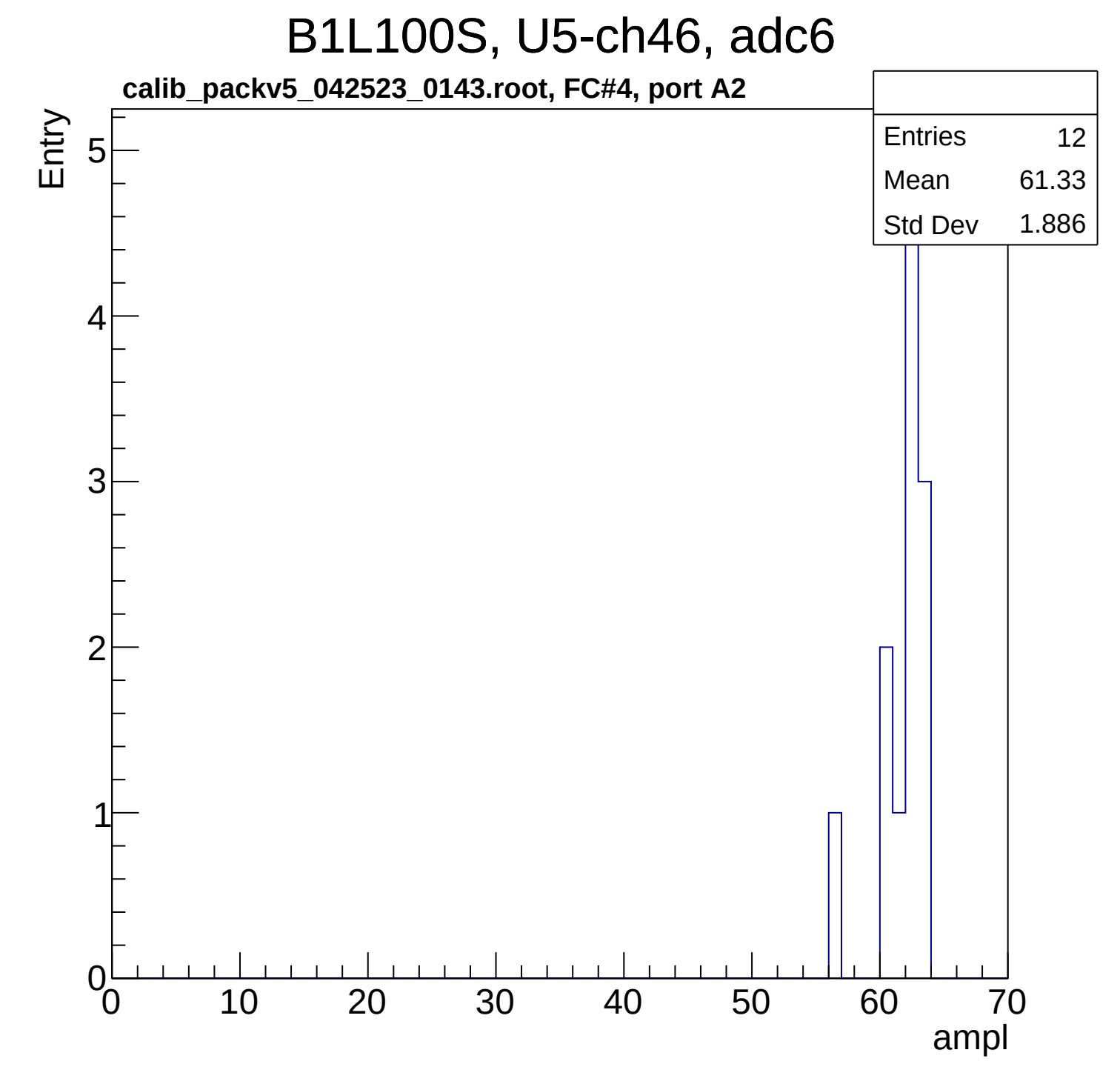
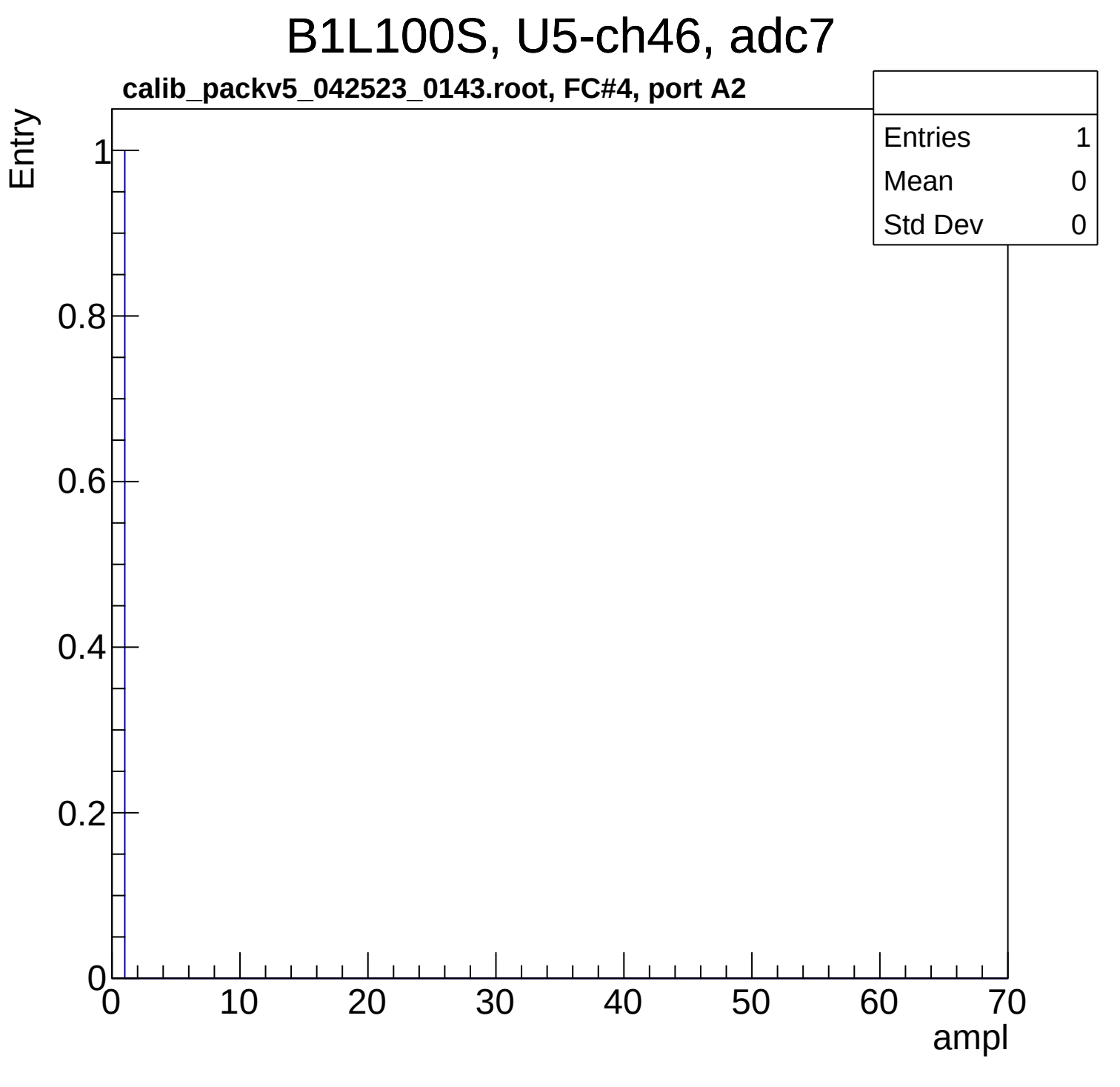
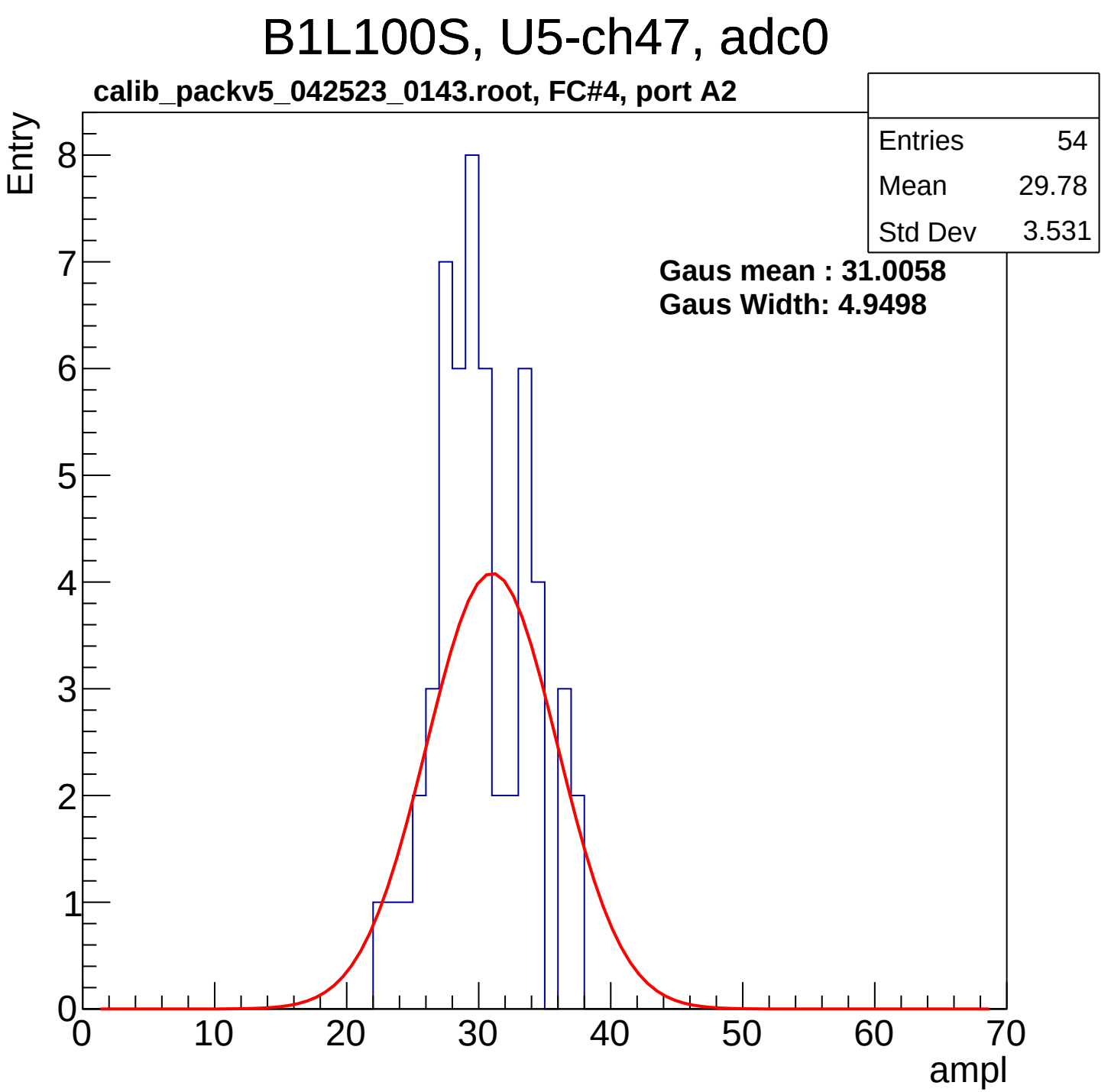
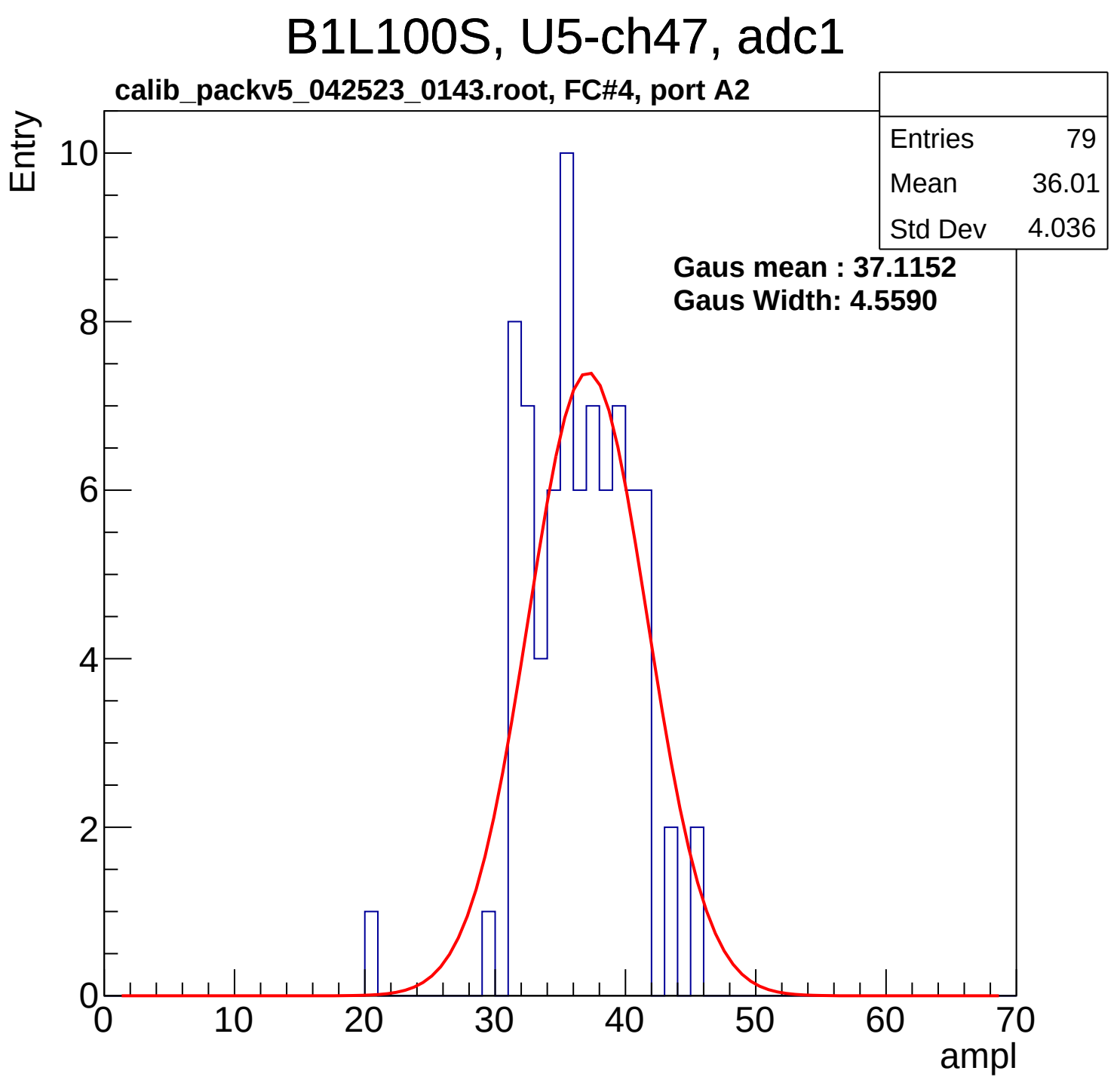
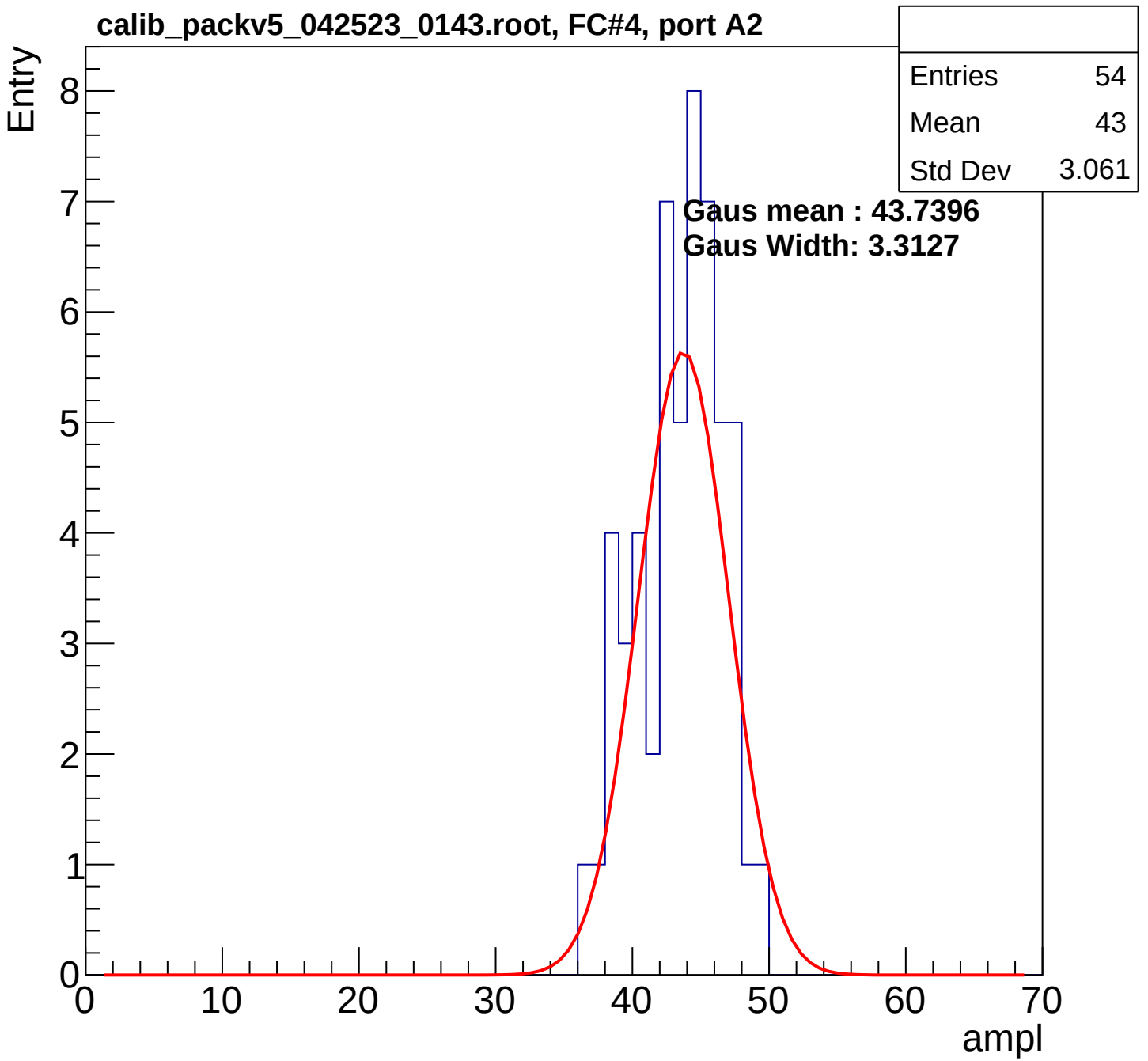
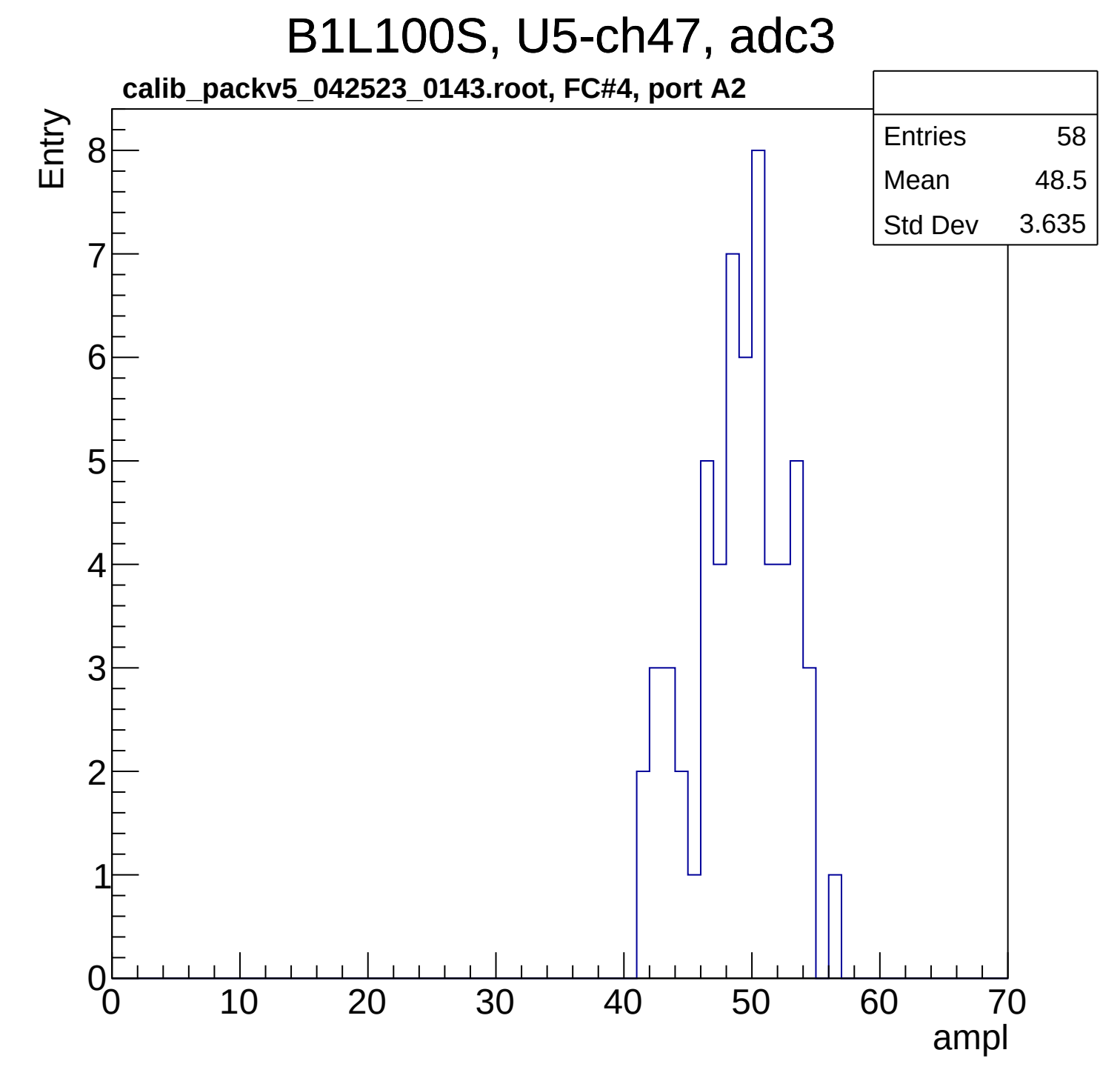

B1L100S, U5-ch46, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 12
Mean 61.33
Std Dev 1.886
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

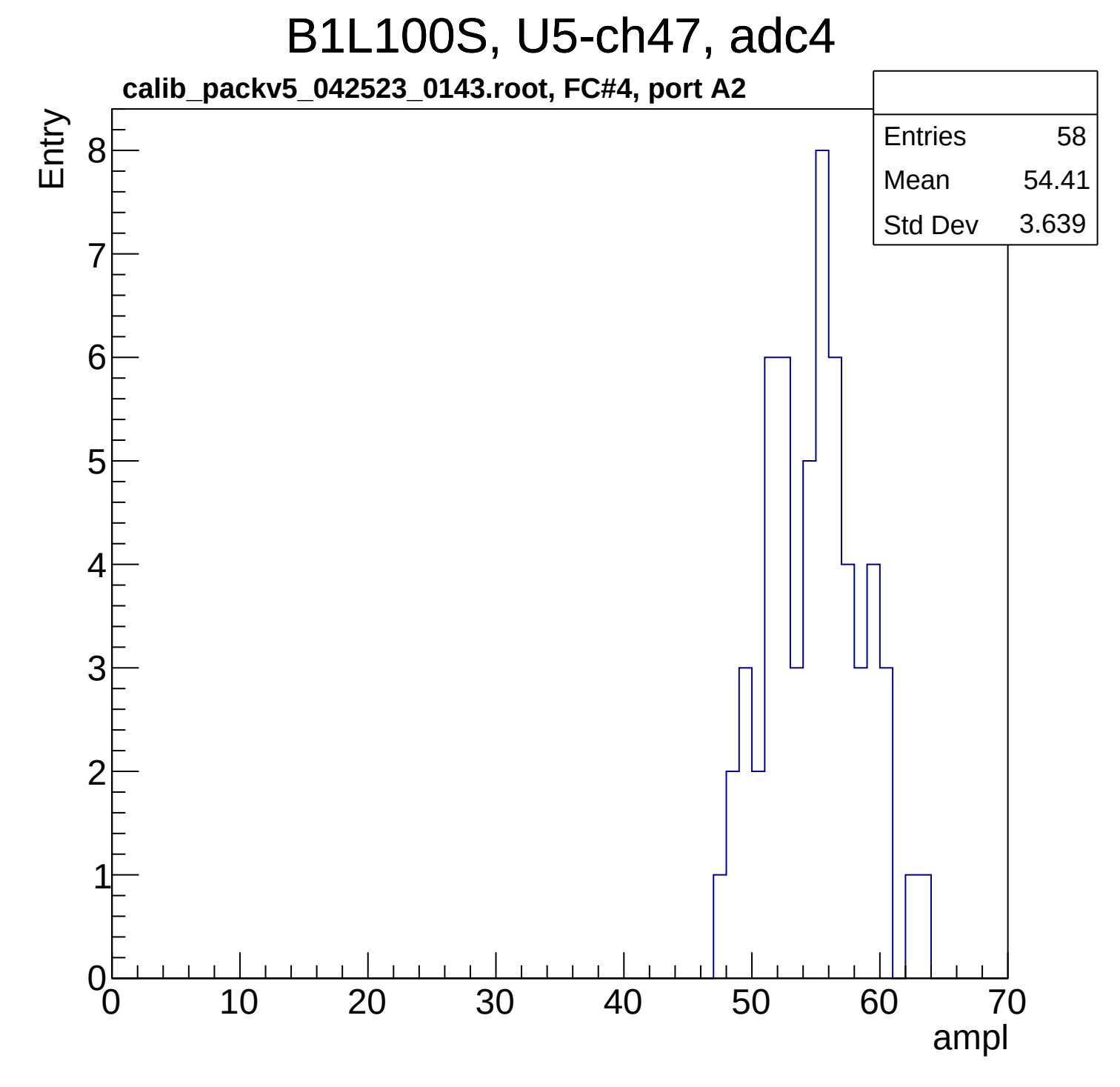

B1L100S, U5-ch46, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch47, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 29.78
Std Dev 3.531
Gaus mean : 31.0058
Gaus Width: 4.9498
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch47, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 79
Mean 36.01
Std Dev 4.036
Gaus mean : 37.1152
Gaus Width: 4.5590
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch47, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 43
Std Dev 3.061
Gaus mean : 43.7396
Gaus Width: 3.3127
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch47, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 48.5
Std Dev 3.635
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch47, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 54.41
Std Dev 3.639
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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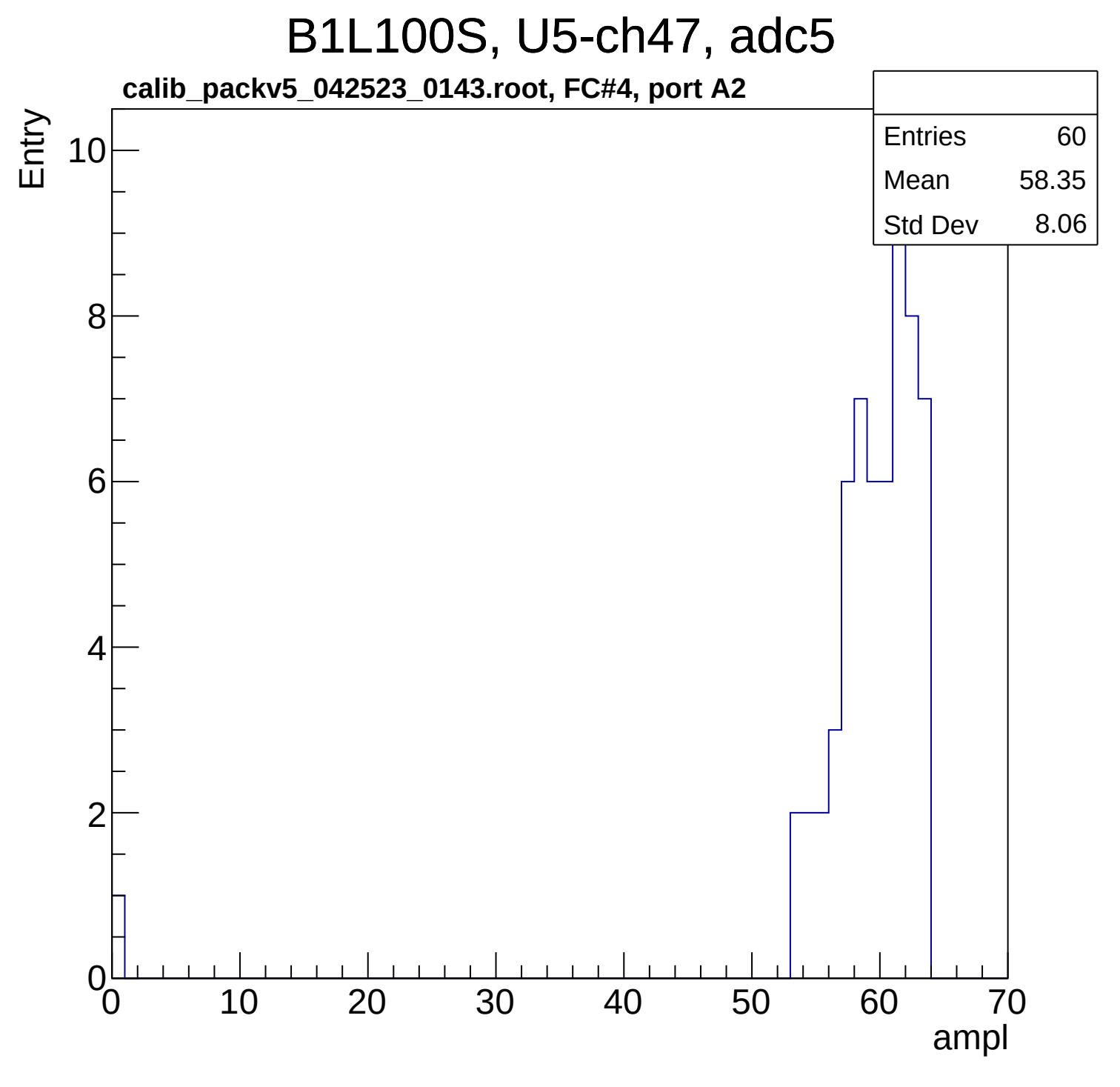
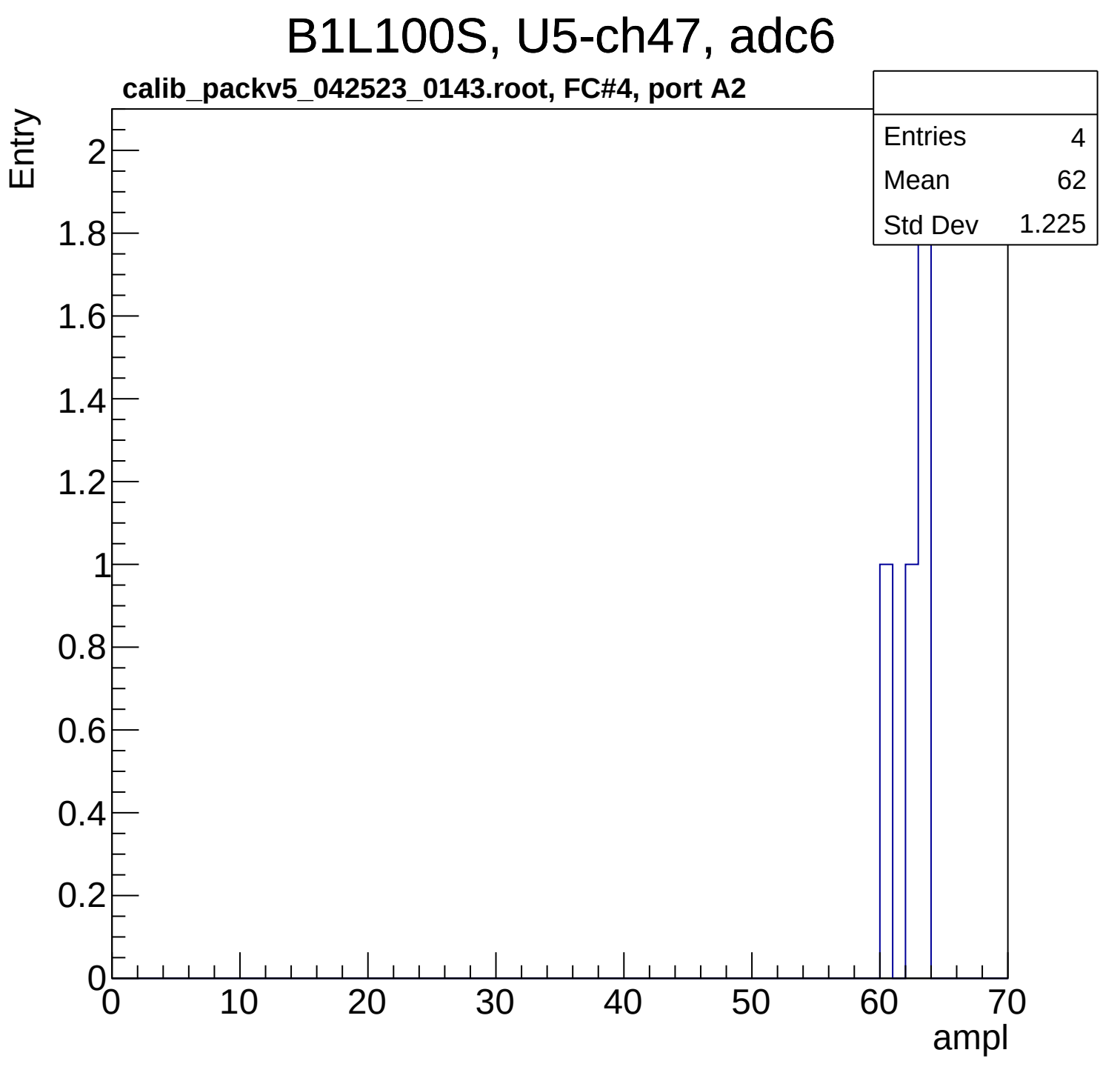
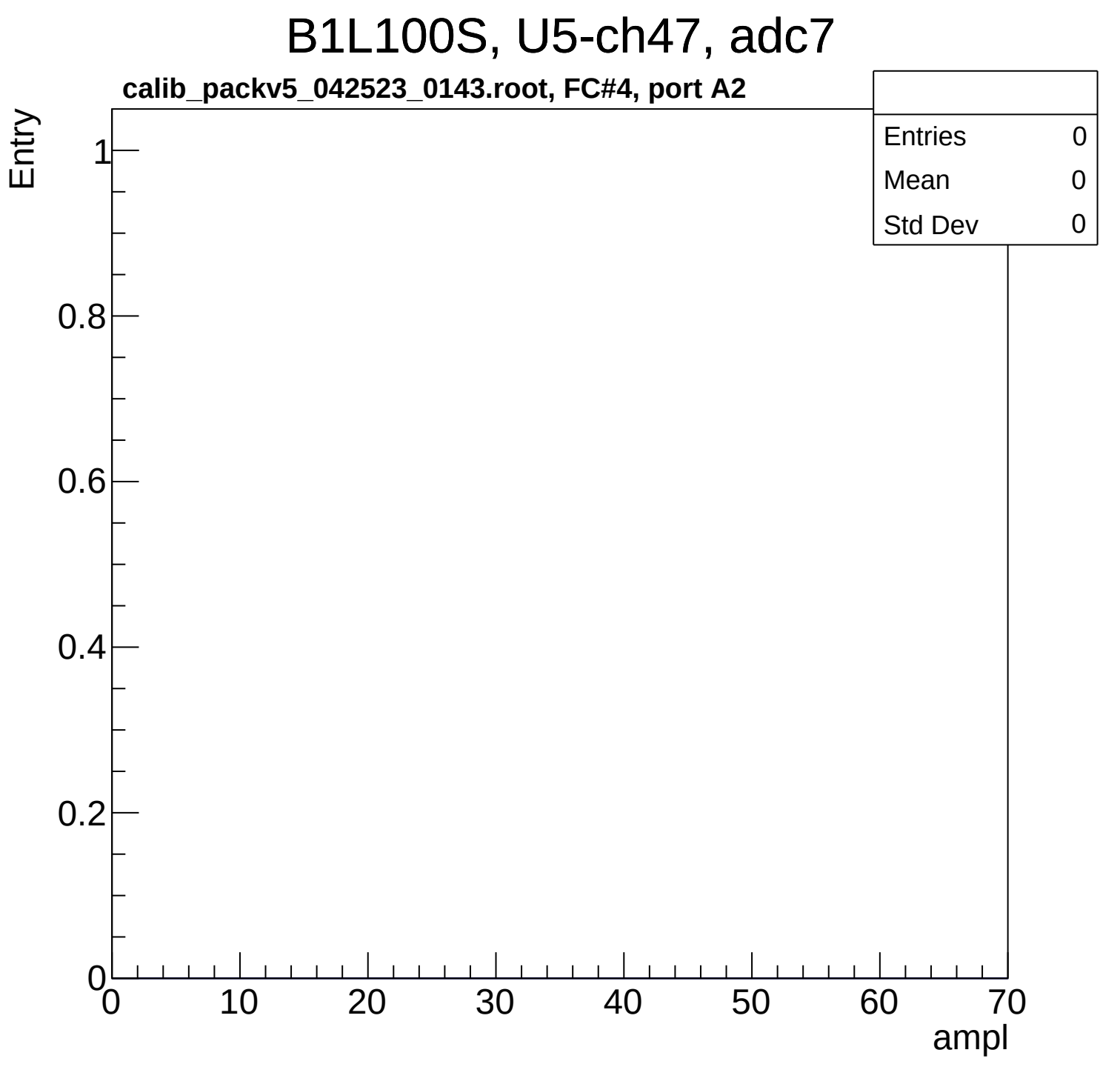

B1L100S, U5-ch47, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 58.35
Std Dev 8.06
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch47, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 4
Mean 62
Std Dev 1.225
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L100S, U5-ch47, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
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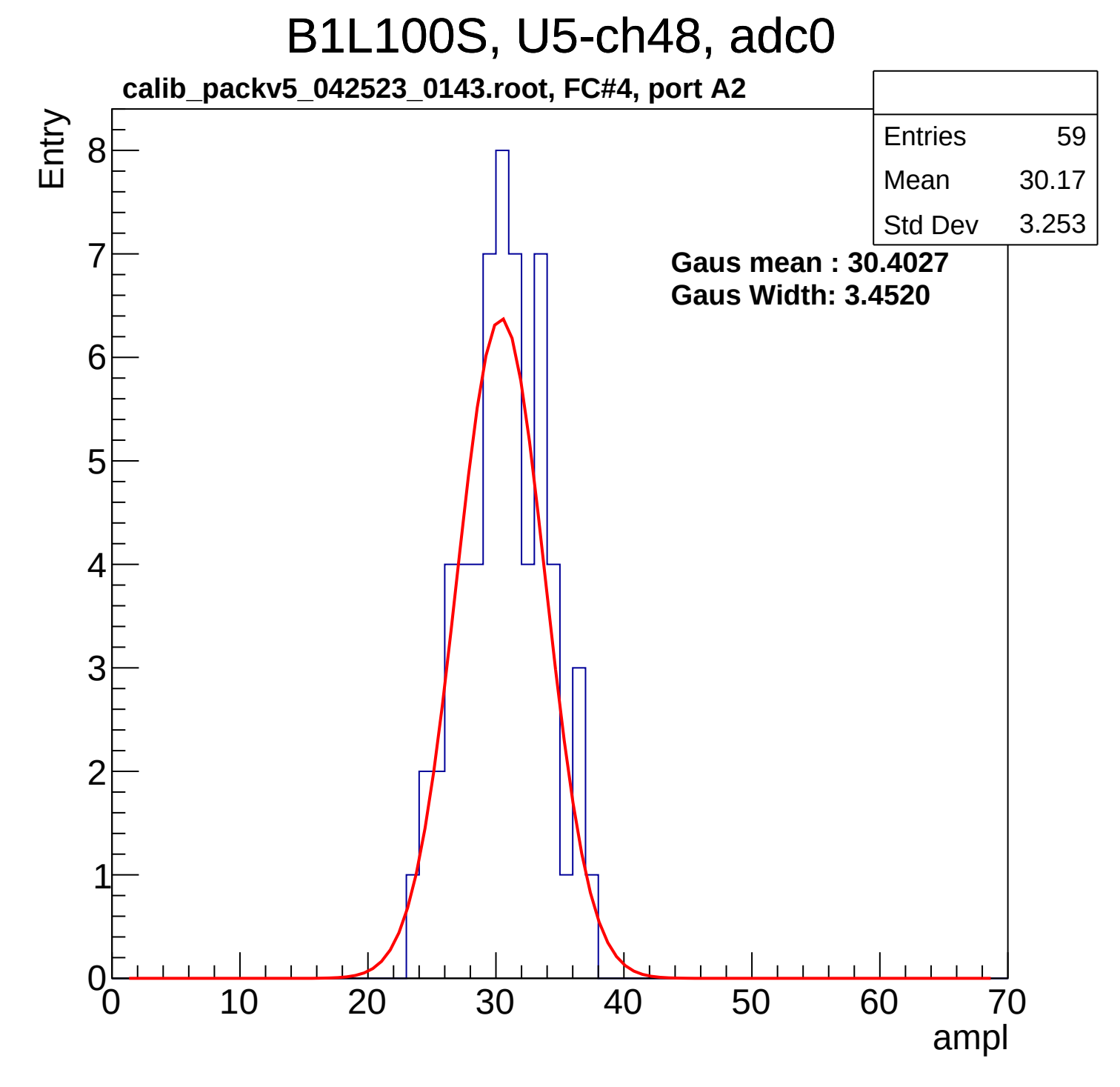
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch48, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 30.17
Std Dev 3.253
Gaus mean : 30.4027
Gaus Width: 3.4520
Entry
ampl
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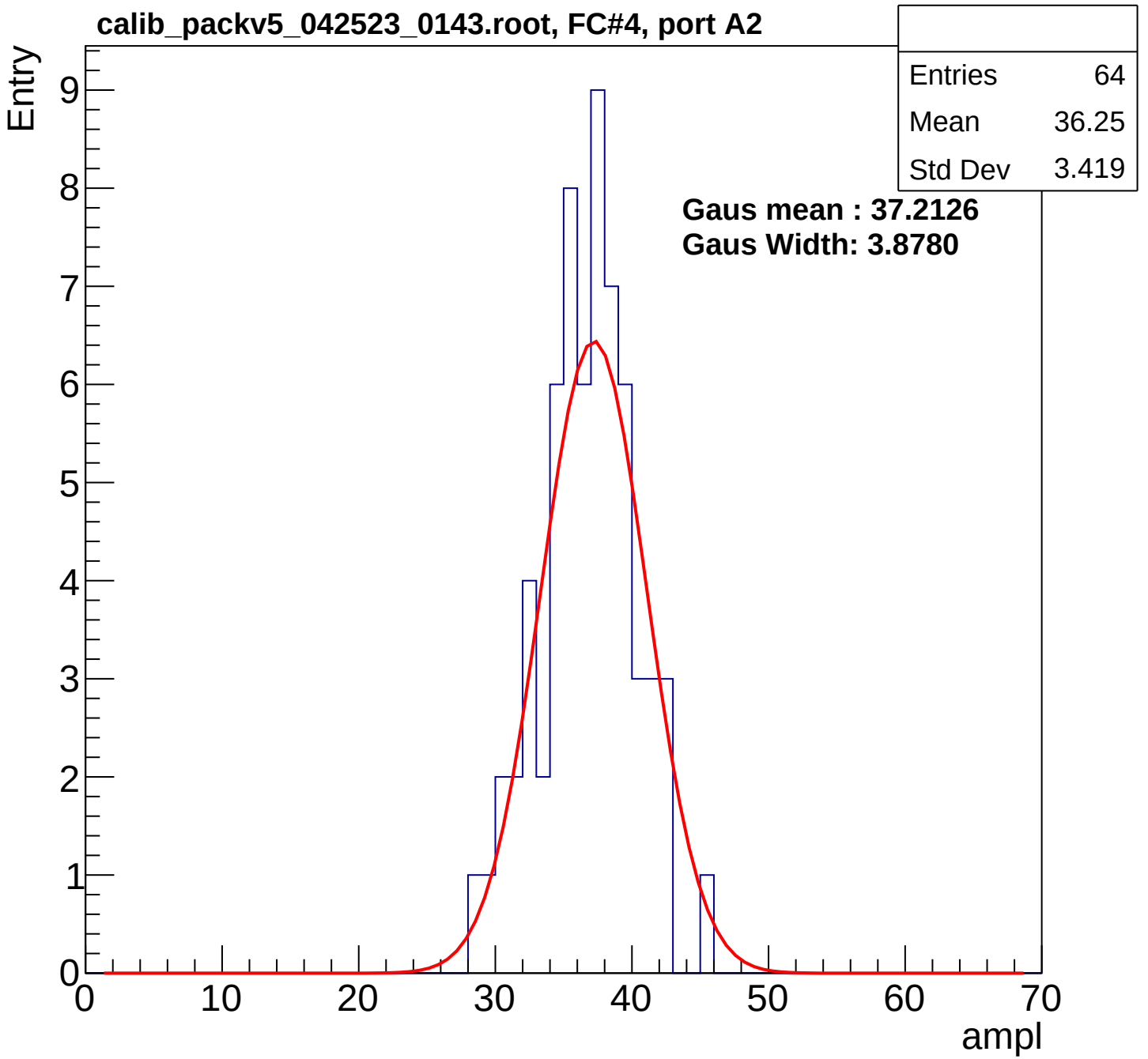
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch48, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 36.25
Std Dev 3.419
Gaus mean : 37.2126
Gaus Width: 3.8780
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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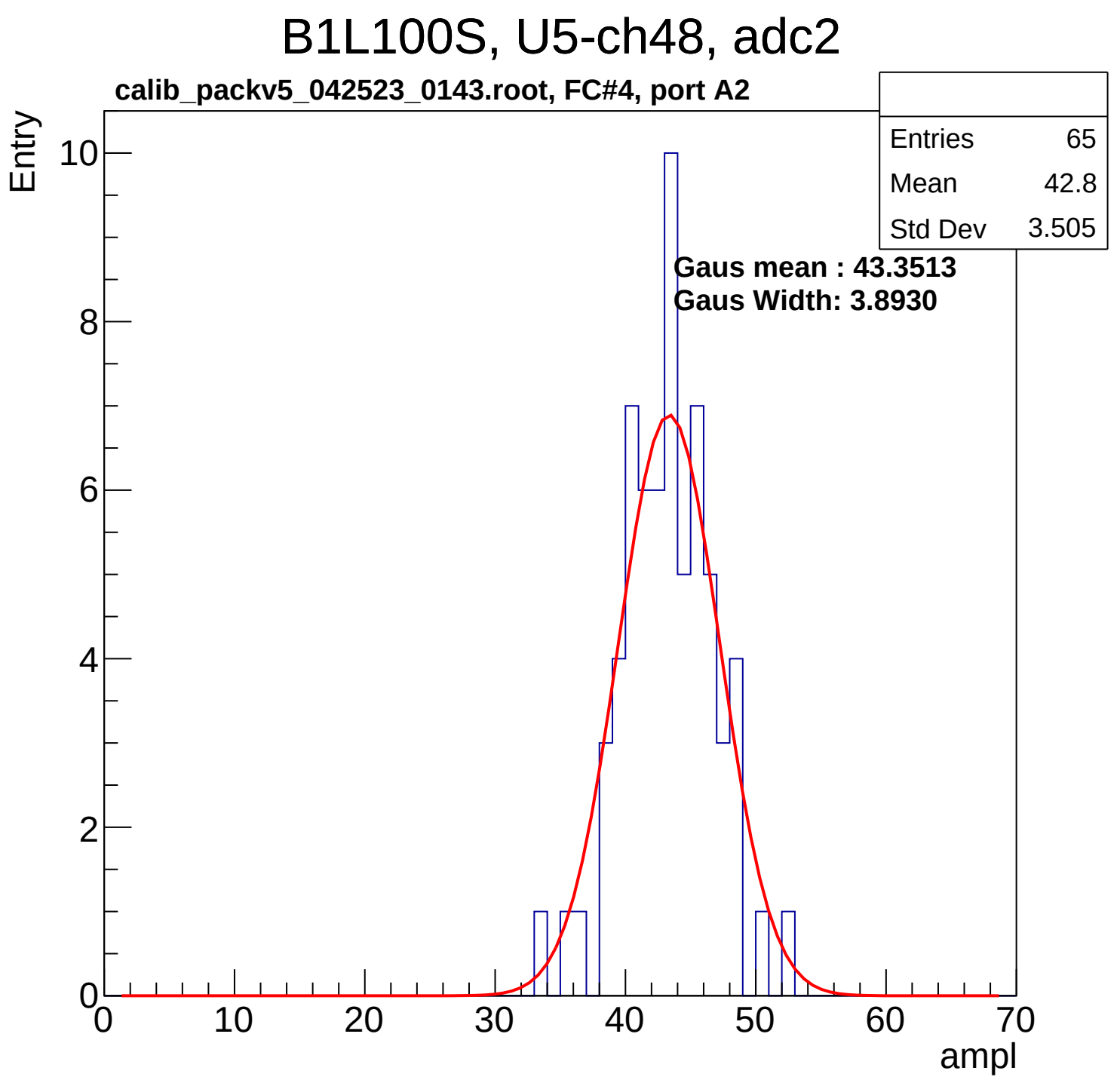
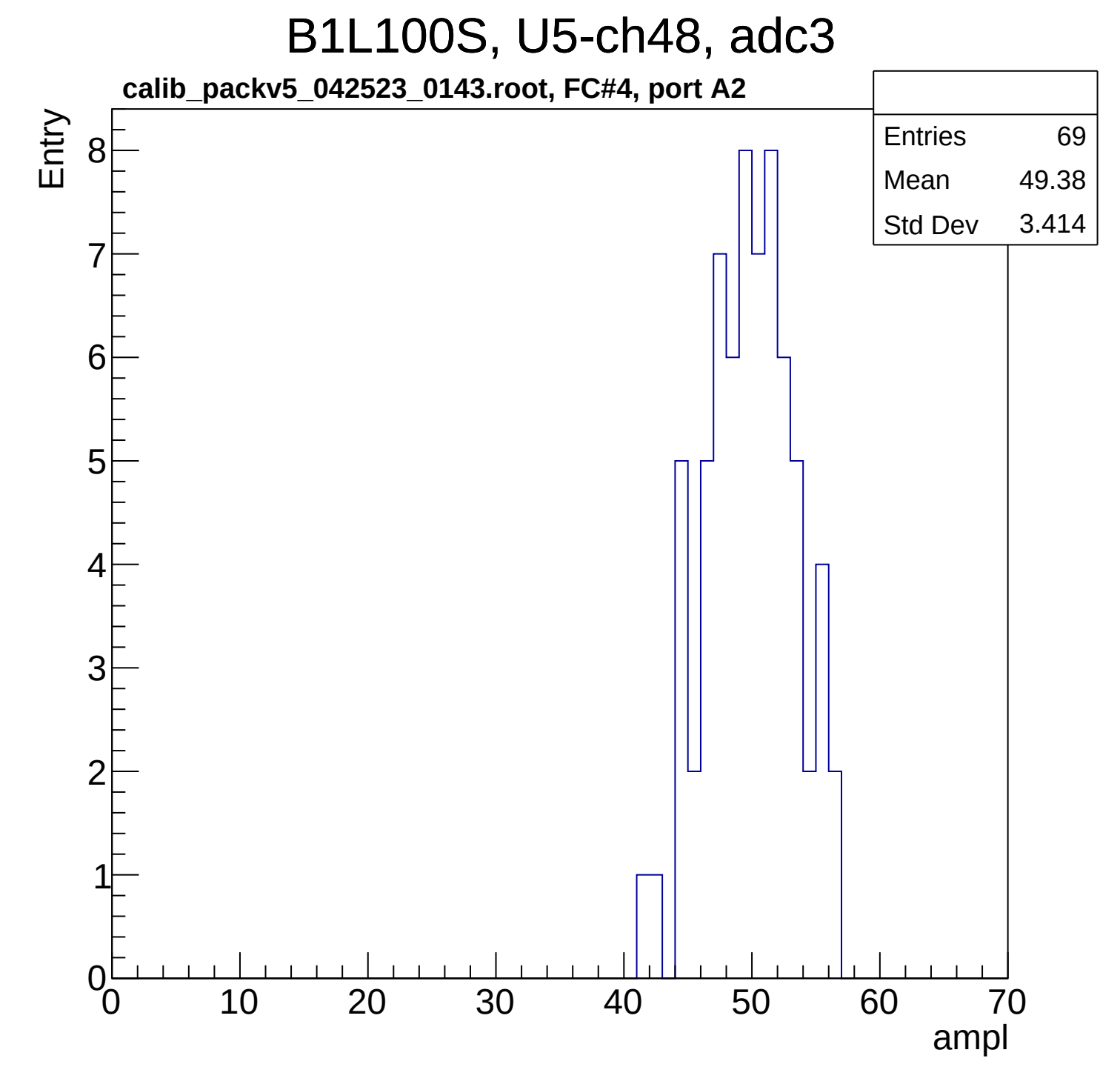

B1L100S, U5-ch48, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 42.8
Std Dev 3.505
Gaus mean : 43.3513
Gaus Width: 3.8930
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch48, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 49.38
Std Dev 3.414
Entry
ampl
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3
4
5
6
7
8
0
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40
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60
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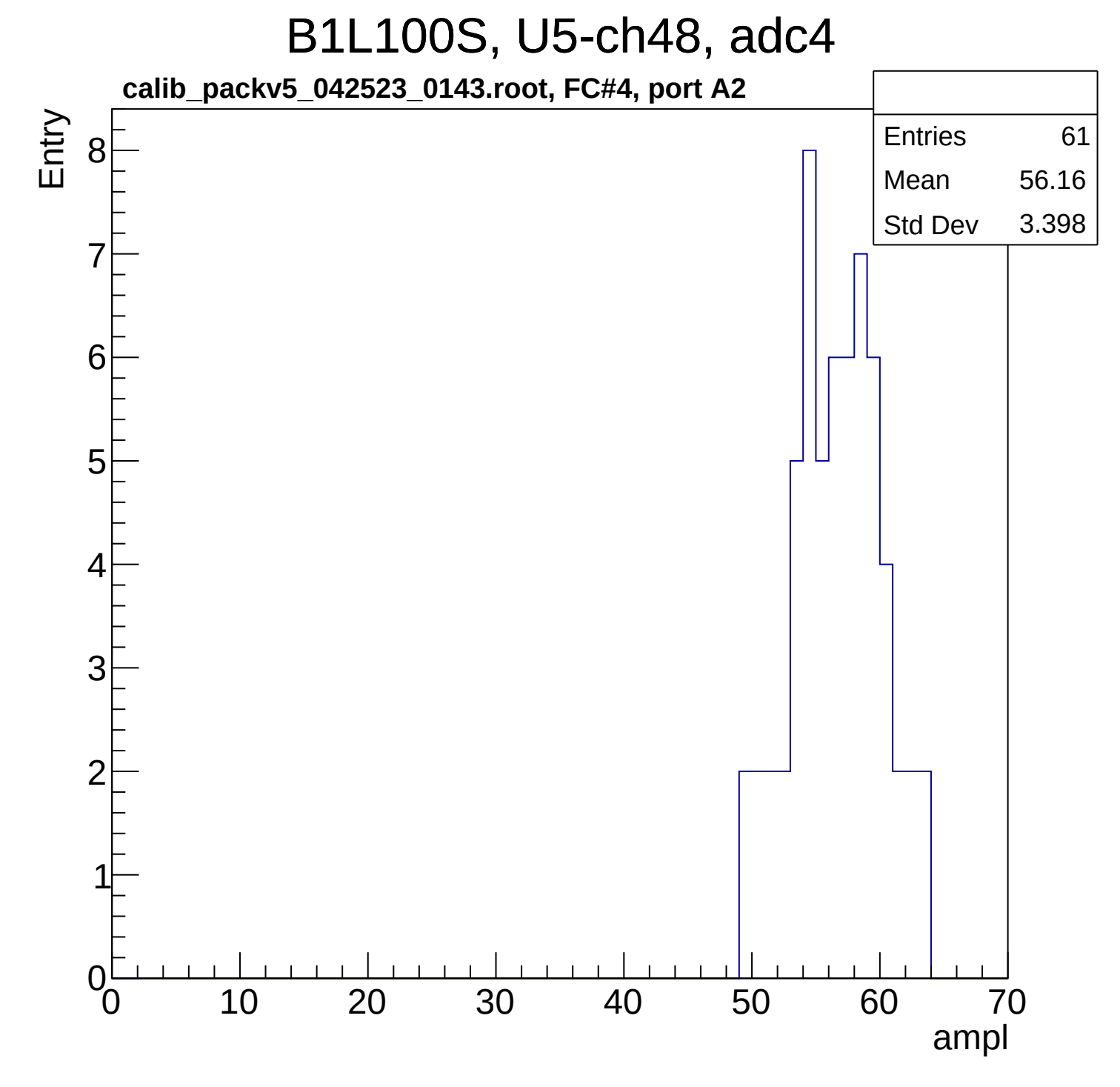
B1L100S, U5-ch48, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 56.16
Std Dev 3.398
Entry
ampl
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2
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4
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6
7
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0
10
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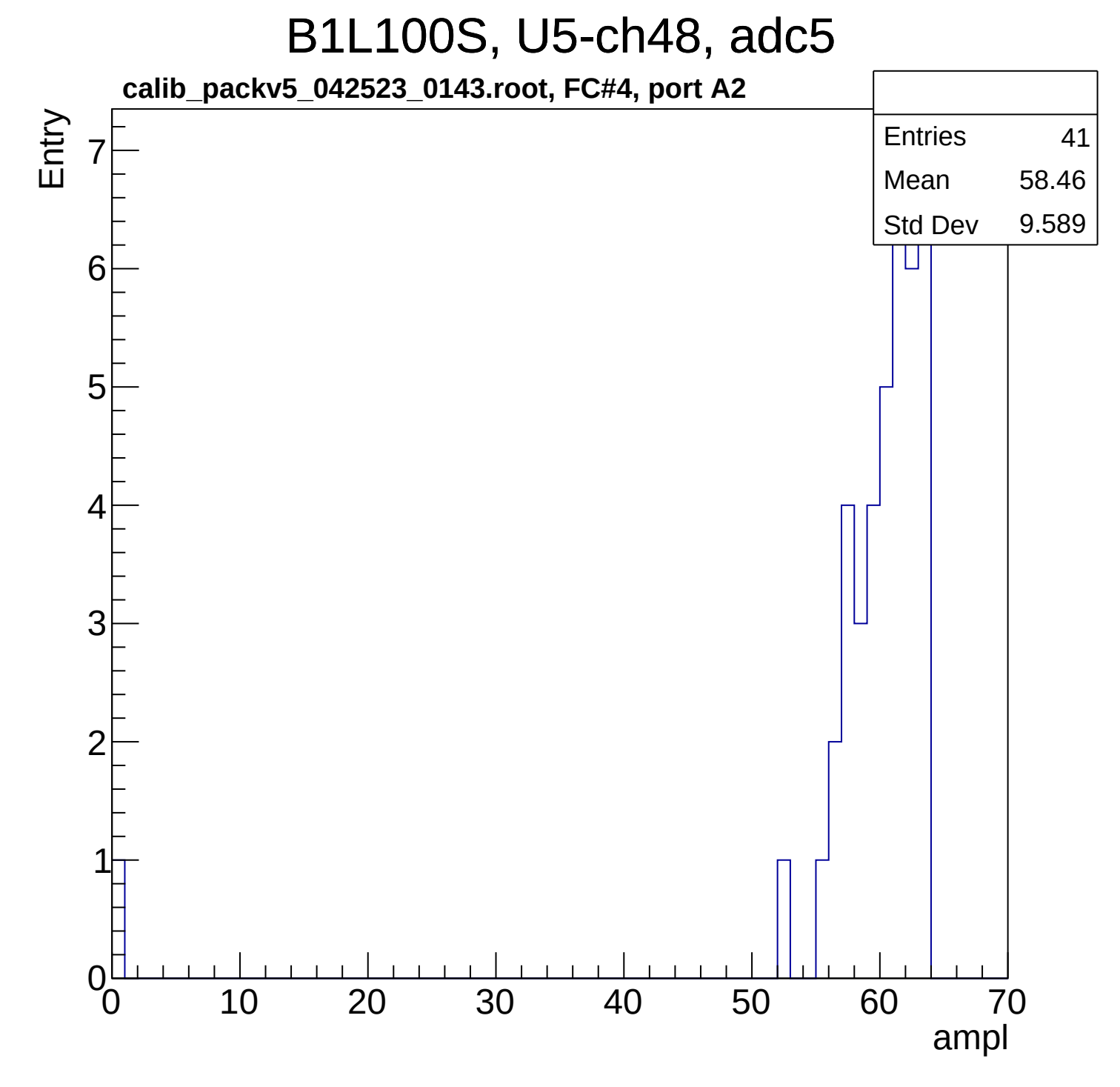
B1L100S, U5-ch48, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 41
Mean 58.46
Std Dev 9.589
Entry
ampl
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1
2
3
4
5
6
7
0
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40
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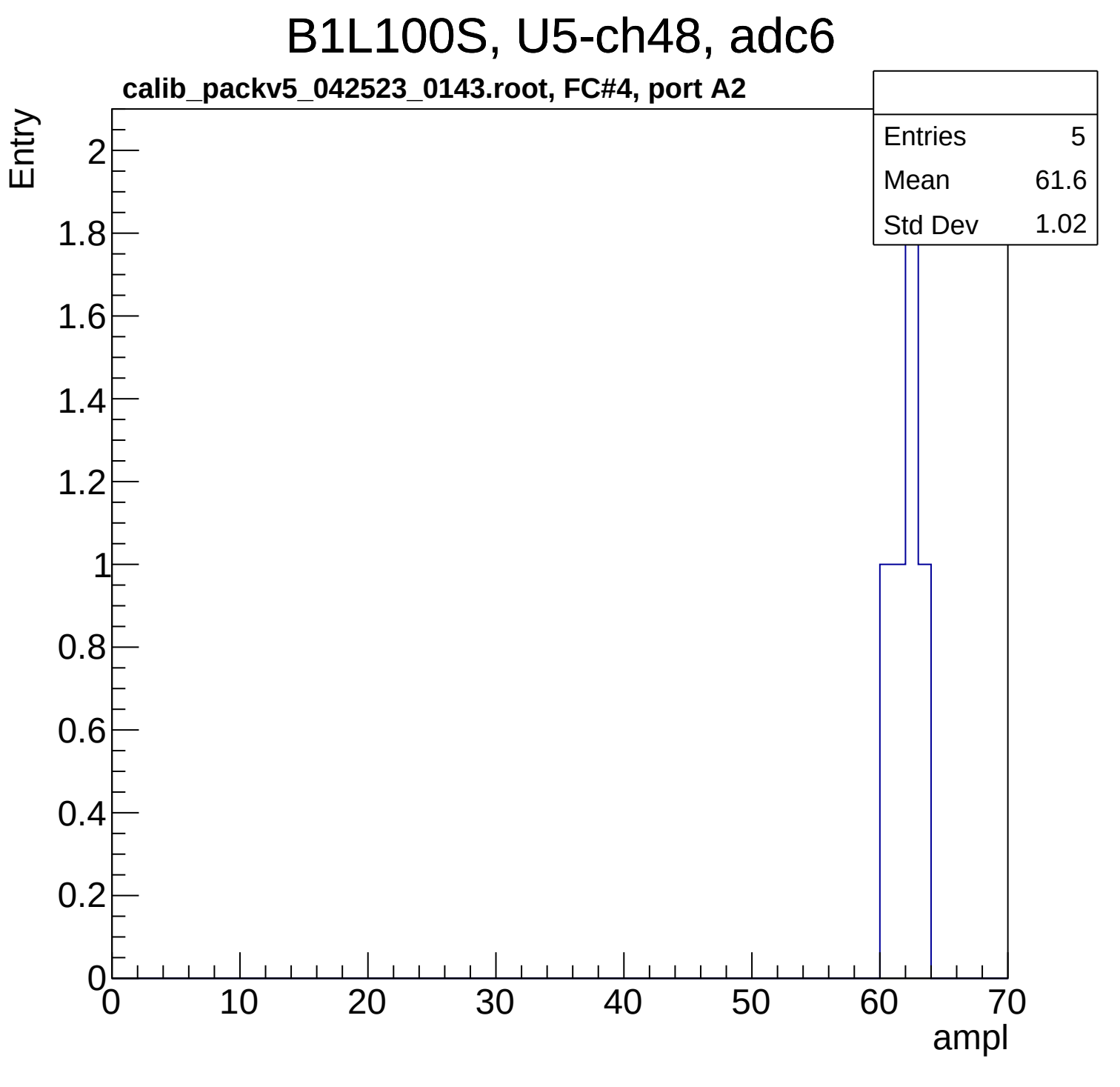
B1L100S, U5-ch48, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 5
Mean 61.6
Std Dev 1.02
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
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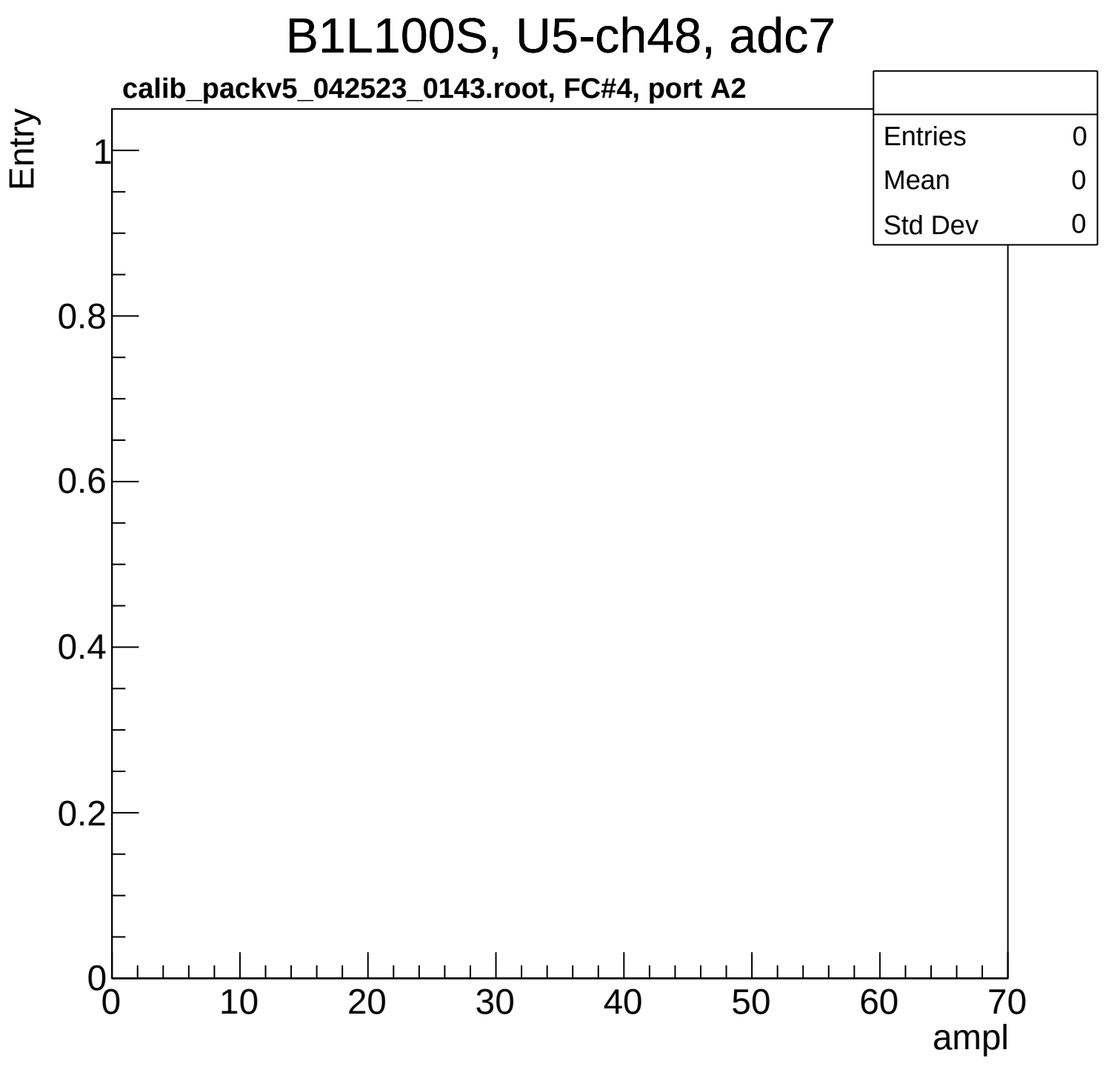
30
40
50
60
70


B1L100S, U5-ch48, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
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10
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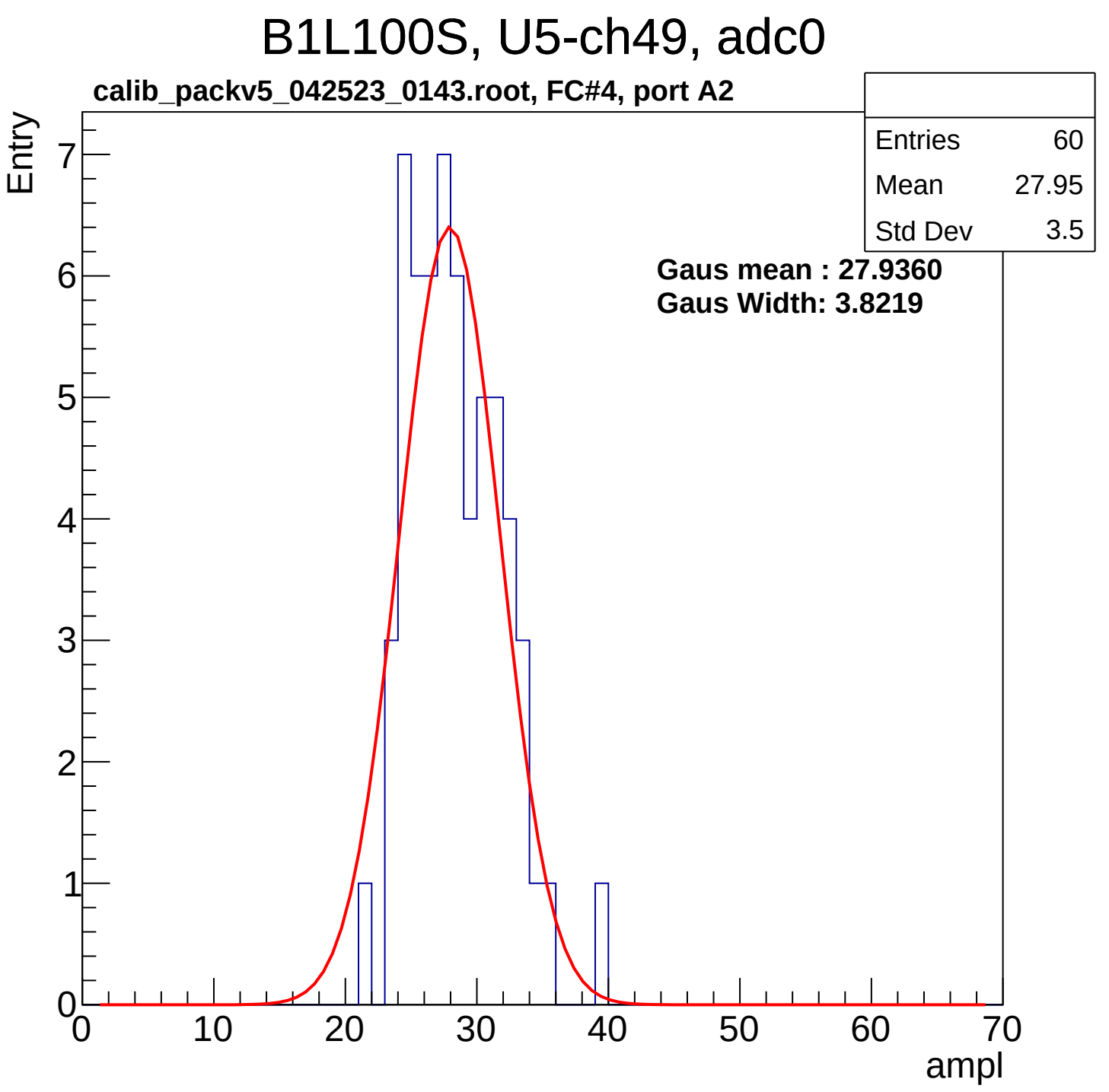
50
60
70
ampl


B1L100S, U5-ch49, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 27.95
Std Dev 3.5
Gaus mean : 27.9360
Gaus Width: 3.8219
Entry
ampl
0
1
2
3
4
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6
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0
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40
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60
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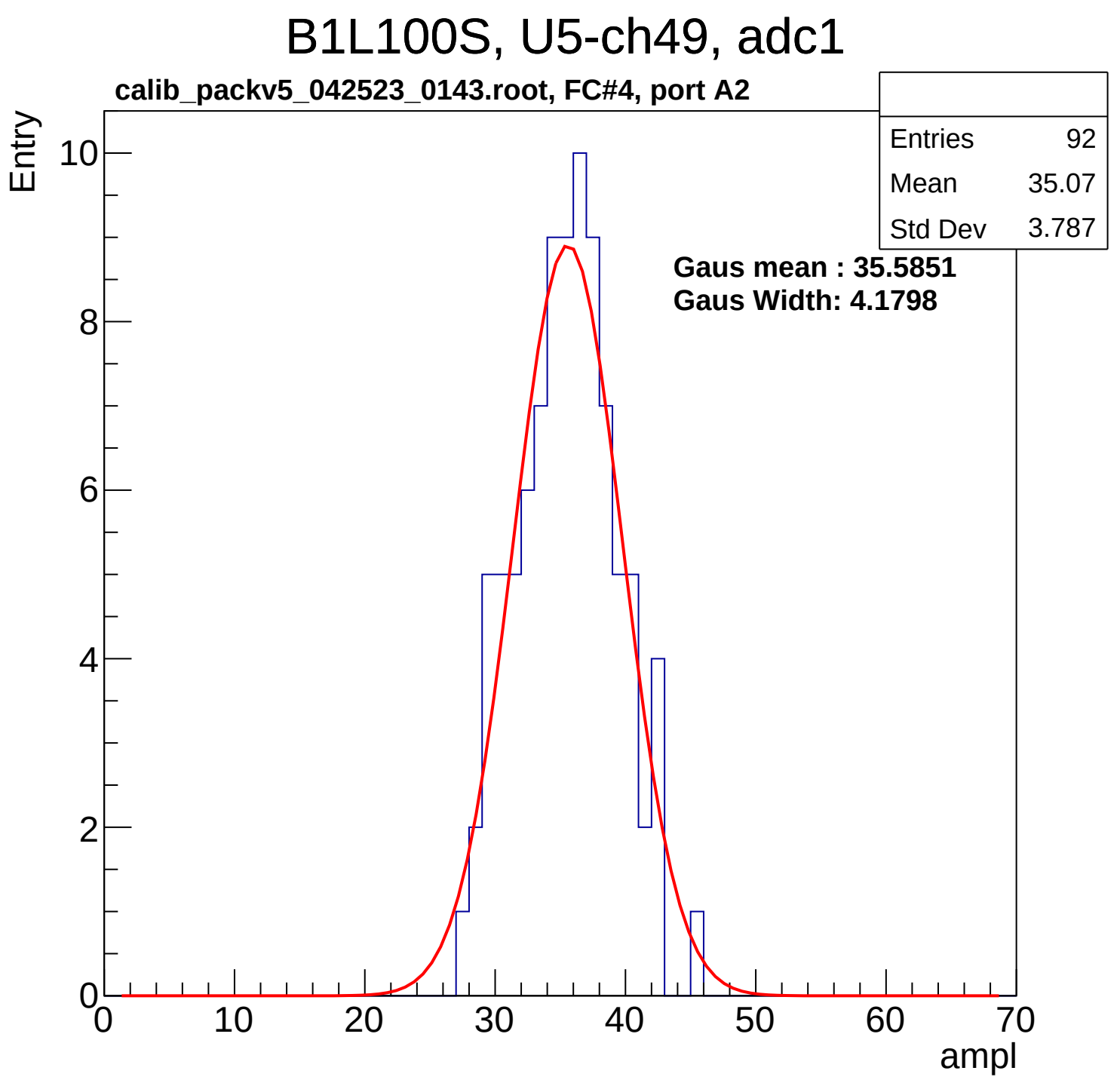
B1L100S, U5-ch49, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 92
Mean 35.07
Std Dev 3.787
Gaus mean : 35.5851
Gaus Width: 4.1798
Entry
ampl
0
2
4
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8
10
0
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40
50
60
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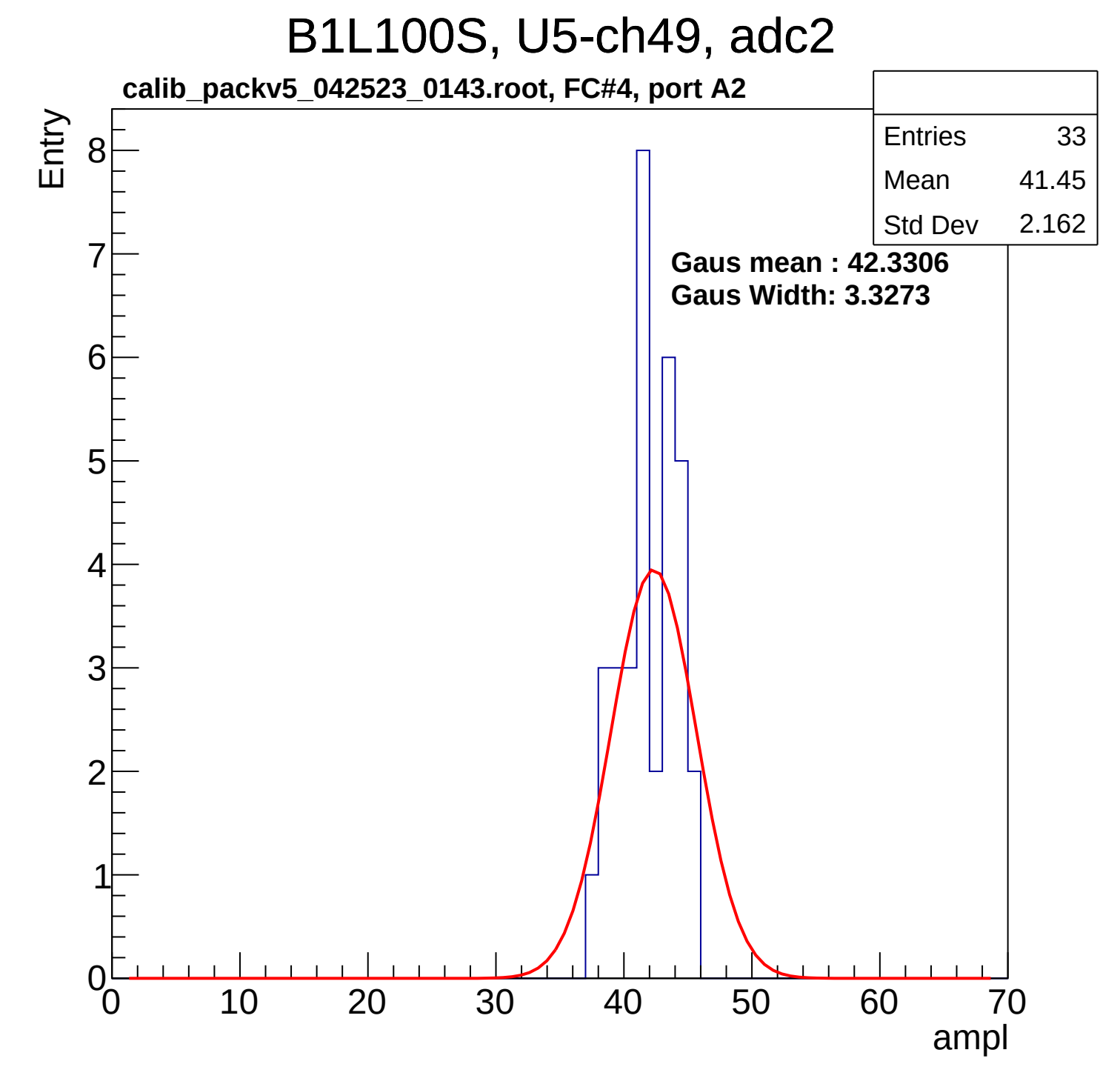
B1L100S, U5-ch49, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 33
Mean 41.45
Std Dev 2.162
Gaus mean : 42.3306
Gaus Width: 3.3273
Entry
ampl
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1
2
3
4
5
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7
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0
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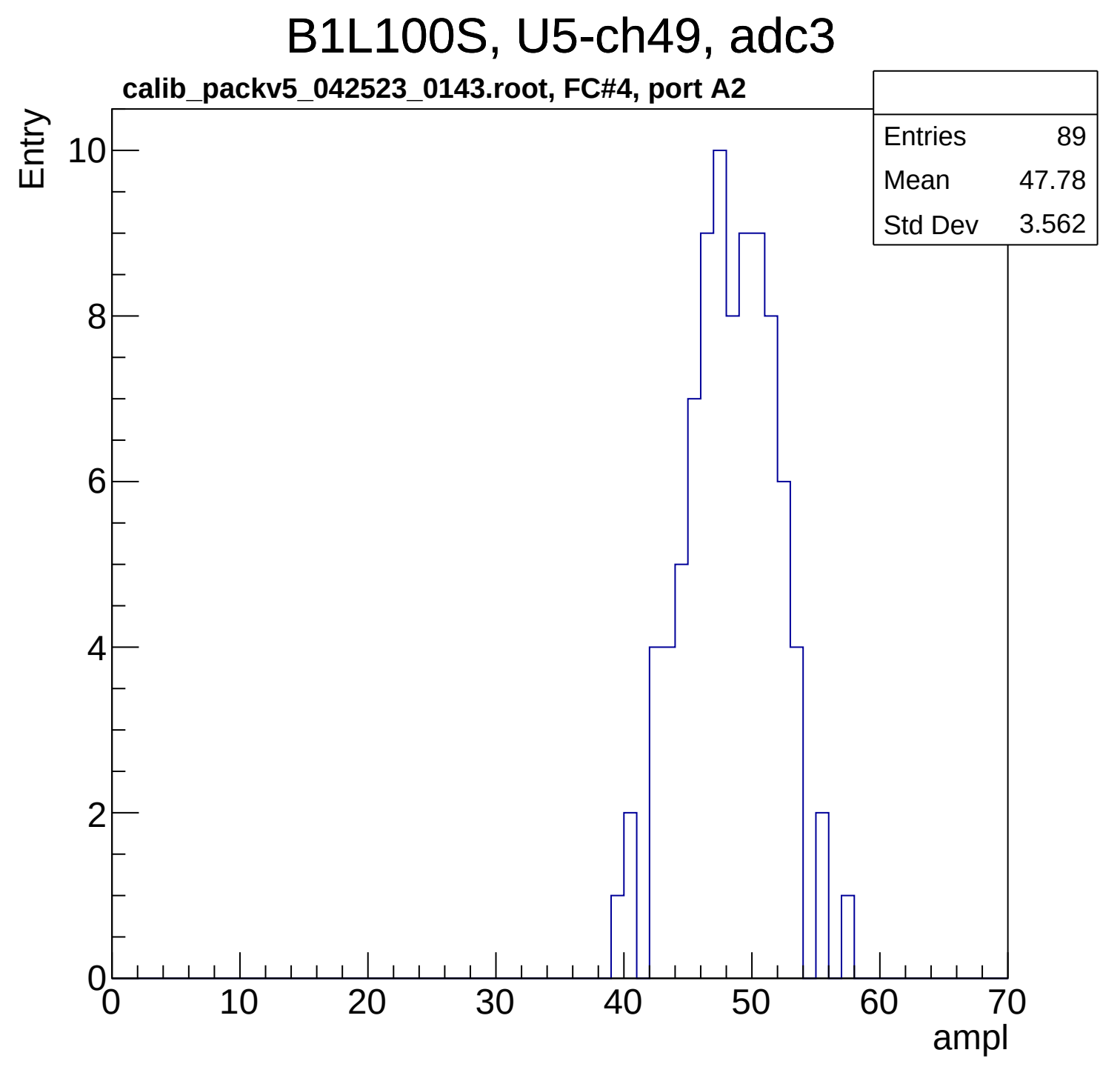
B1L100S, U5-ch49, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 89
Mean 47.78
Std Dev 3.562
Entry
ampl
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0
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60
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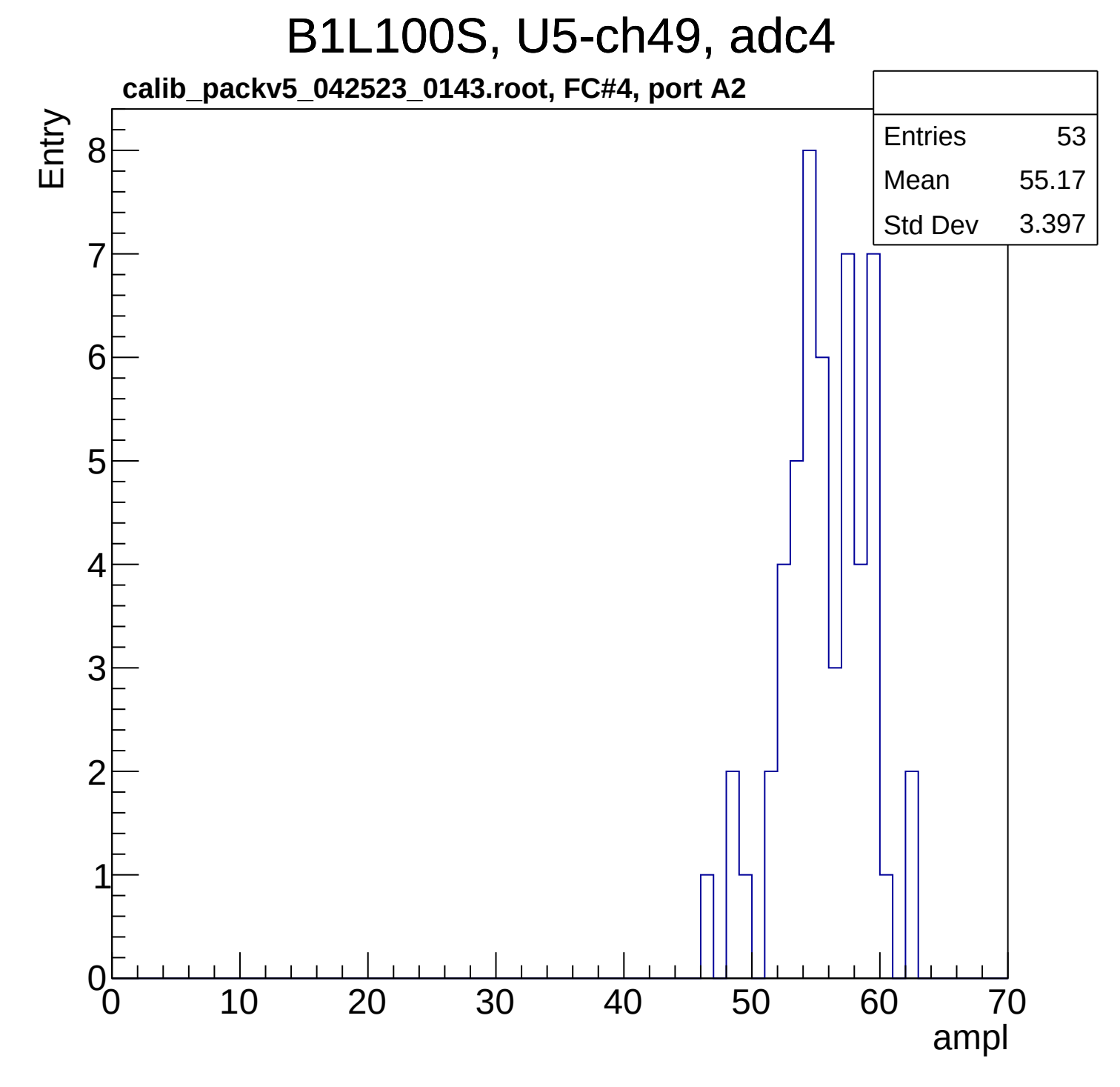
B1L100S, U5-ch49, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 55.17
Std Dev 3.397
Entry
ampl
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1
2
3
4
5
6
7
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0
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60
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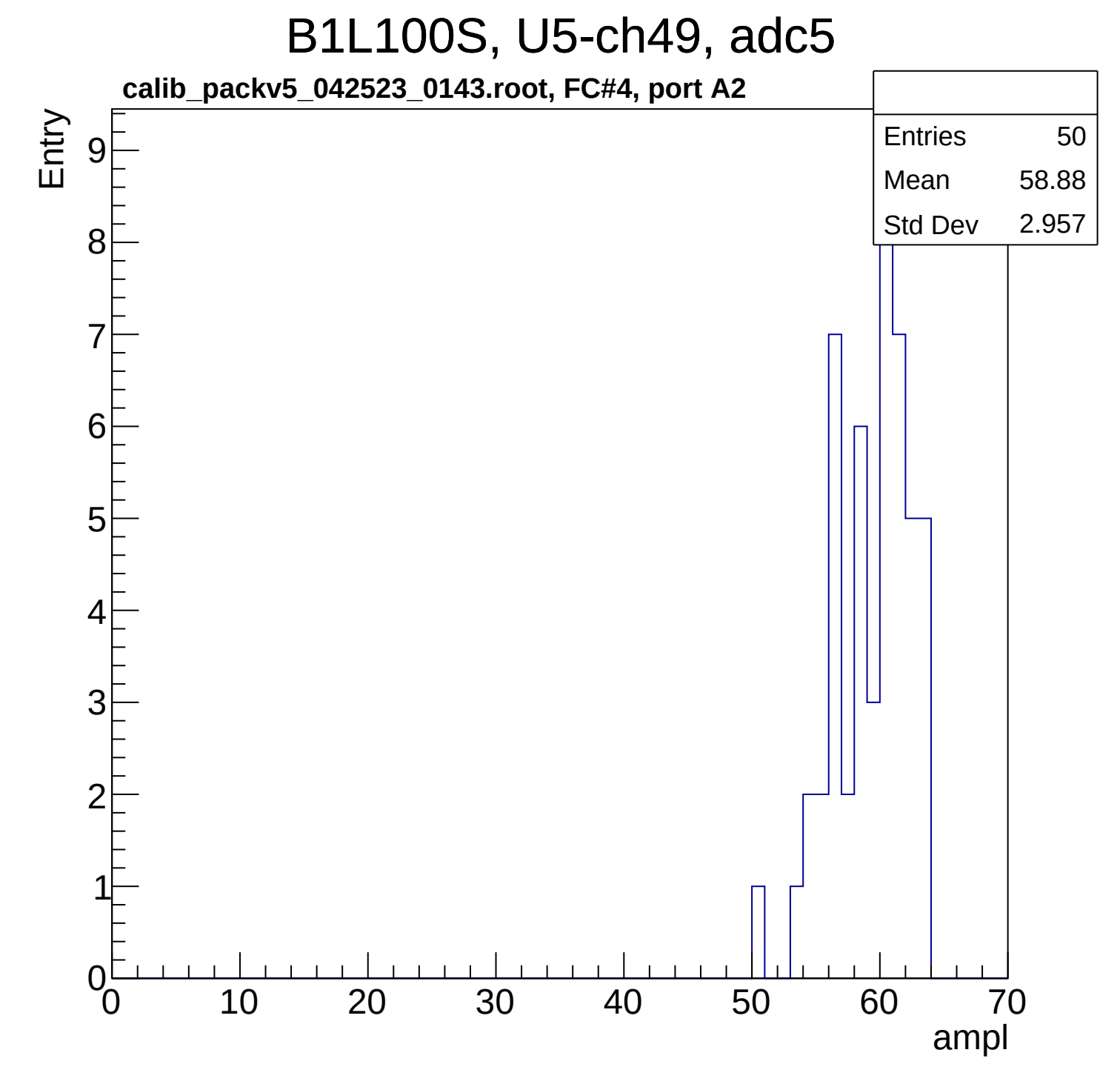
B1L100S, U5-ch49, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 58.88
Std Dev 2.957
Entry
ampl
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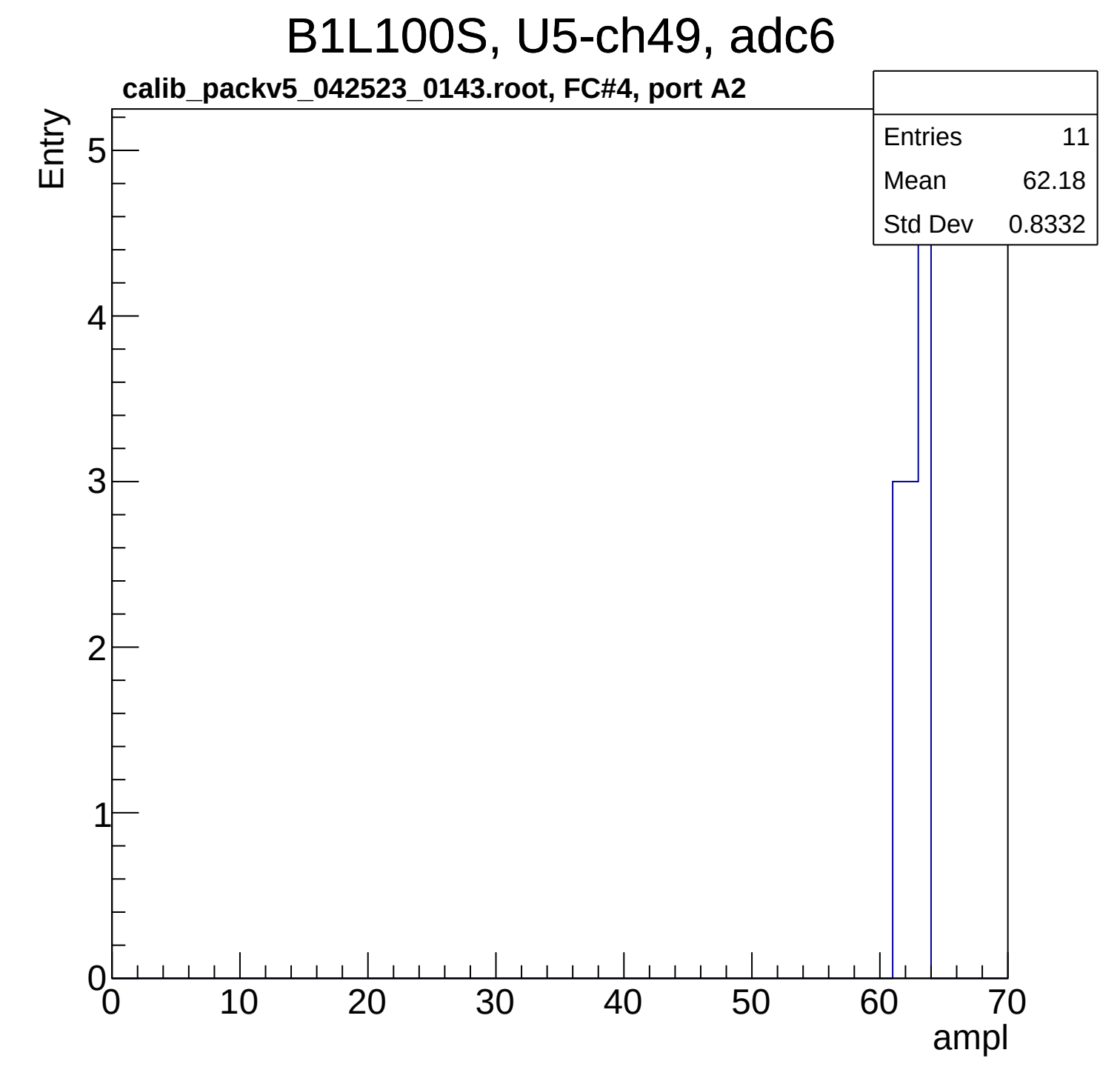
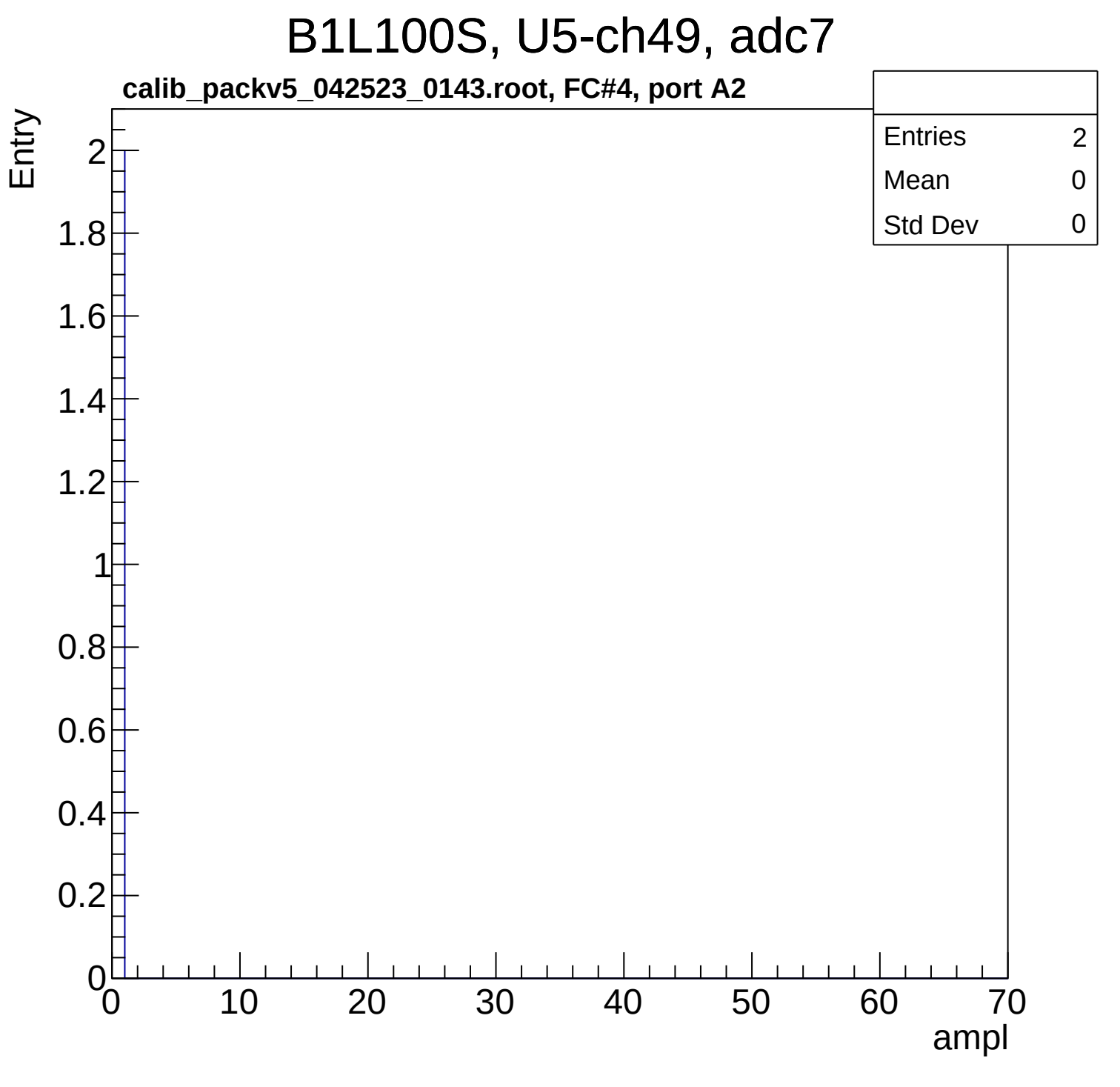
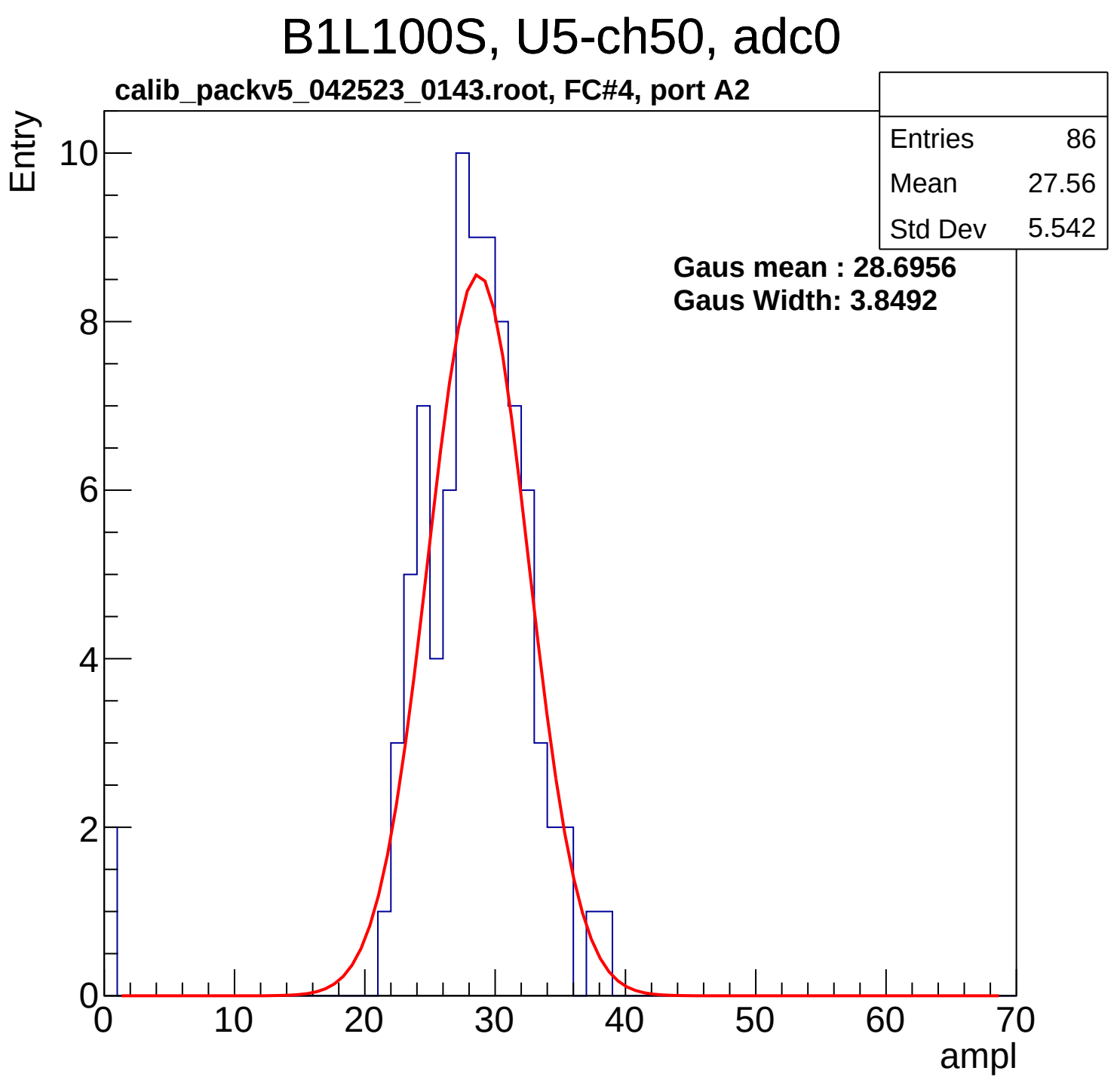
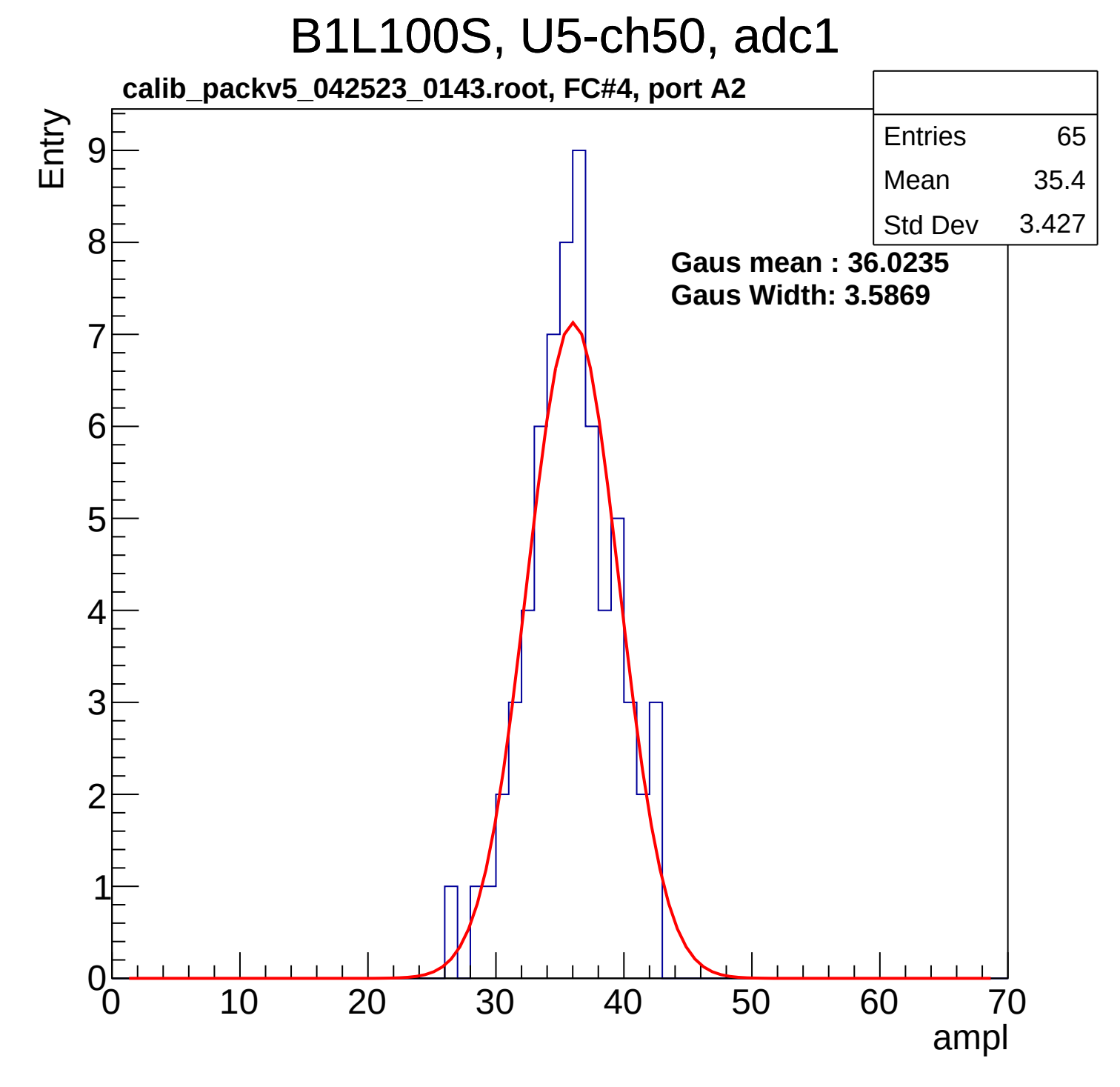
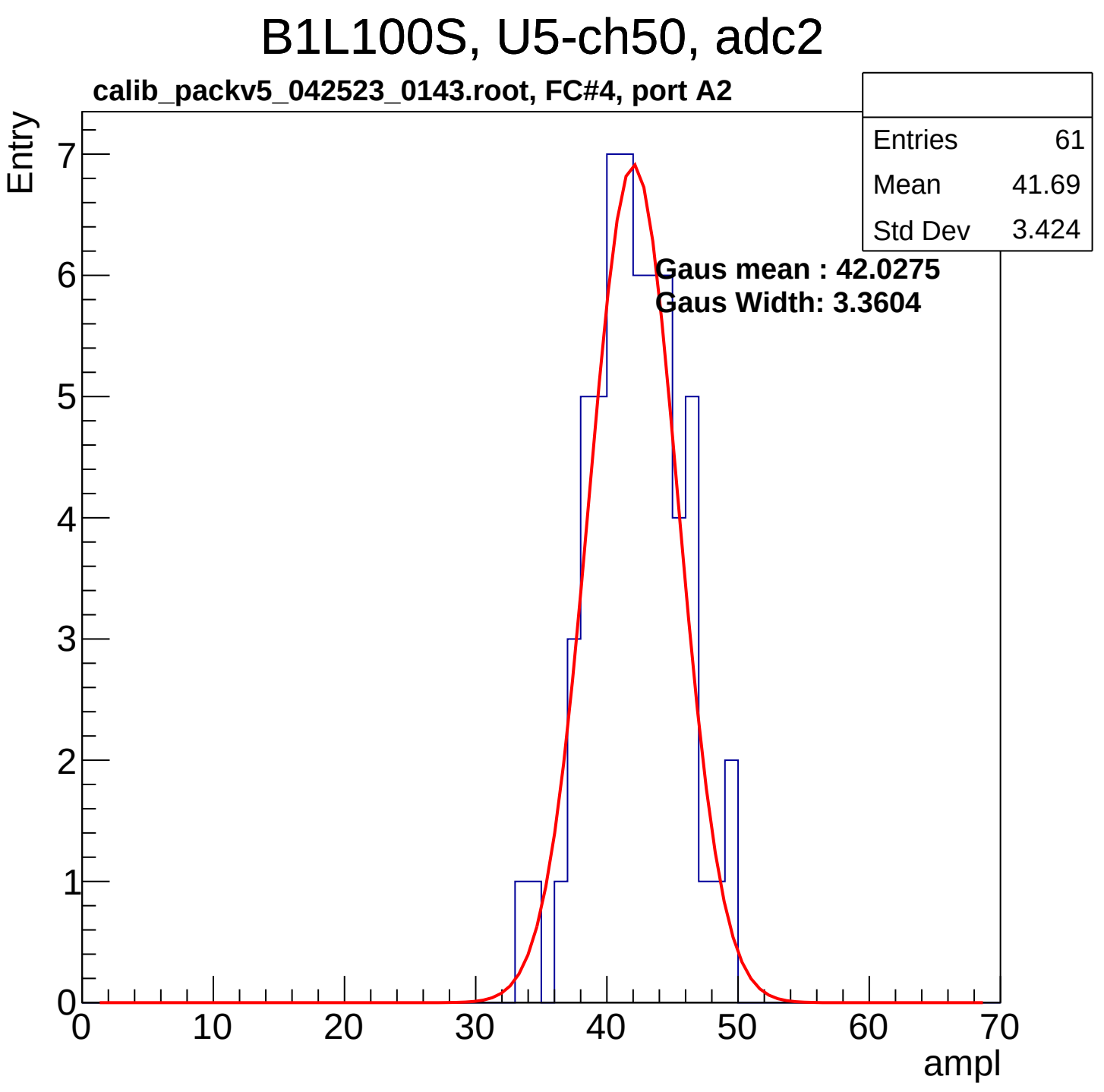
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch49, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 11
Mean 62.18
Std Dev 0.8332
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch49, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch50, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 86
Mean 27.56
Std Dev 5.542
Gaus mean : 28.6956
Gaus Width: 3.8492
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch50, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 35.4
Std Dev 3.427
Gaus mean : 36.0235
Gaus Width: 3.5869
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch50, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 41.69
Std Dev 3.424
Gaus mean : 42.0275
Gaus Width: 3.3604
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
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60
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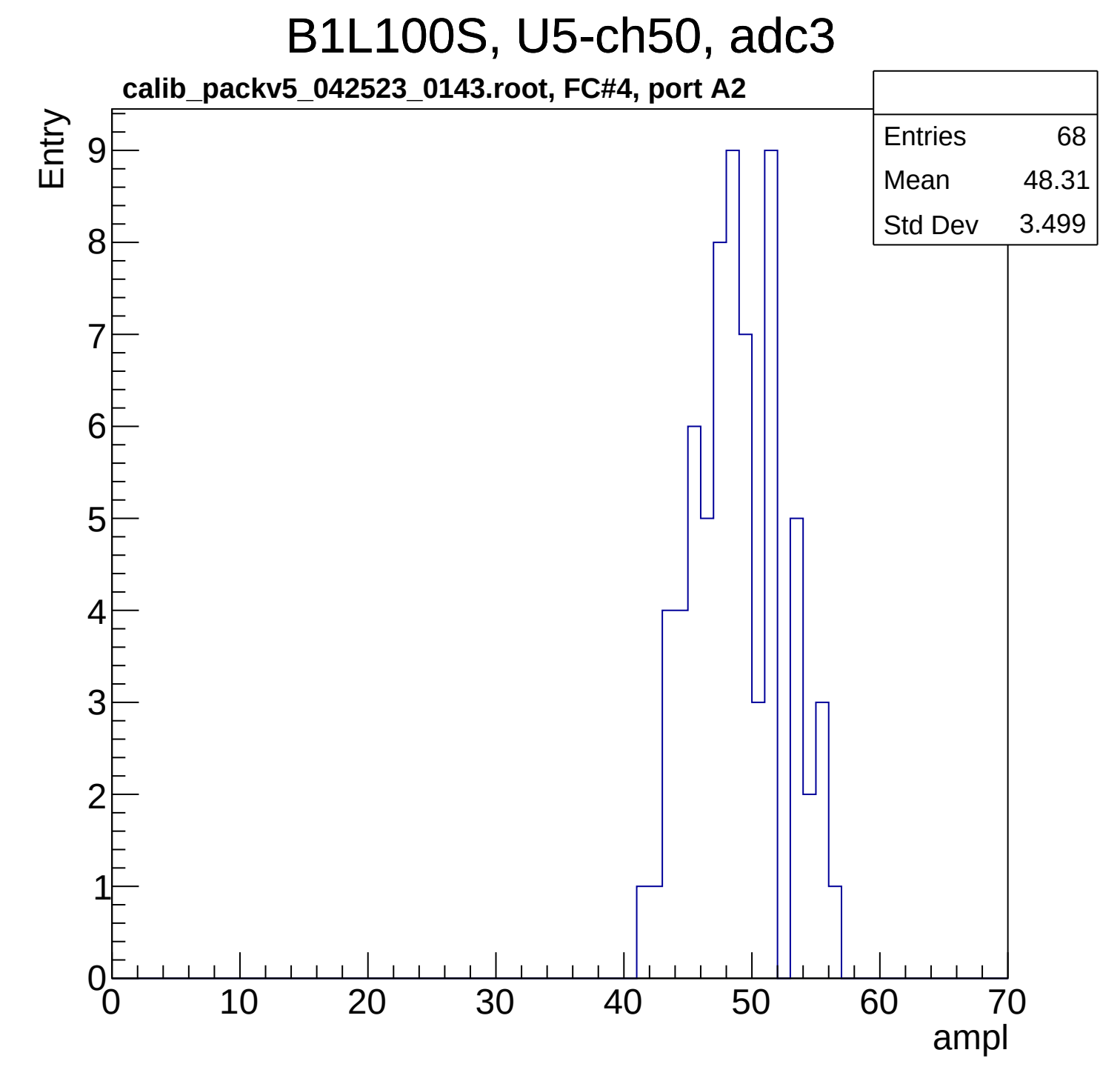
B1L100S, U5-ch50, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 48.31
Std Dev 3.499
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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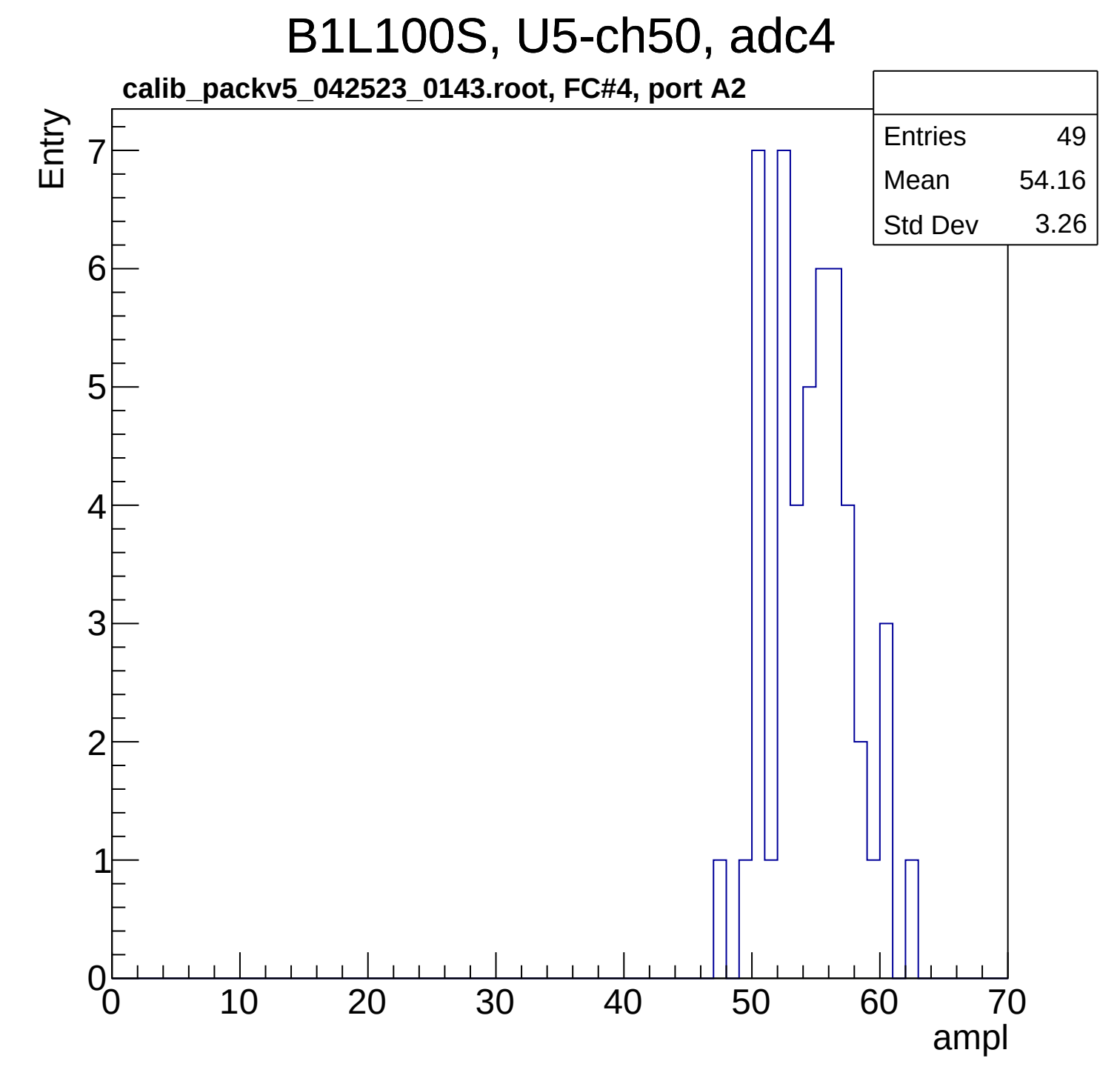
B1L100S, U5-ch50, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 49
Mean 54.16
Std Dev 3.26
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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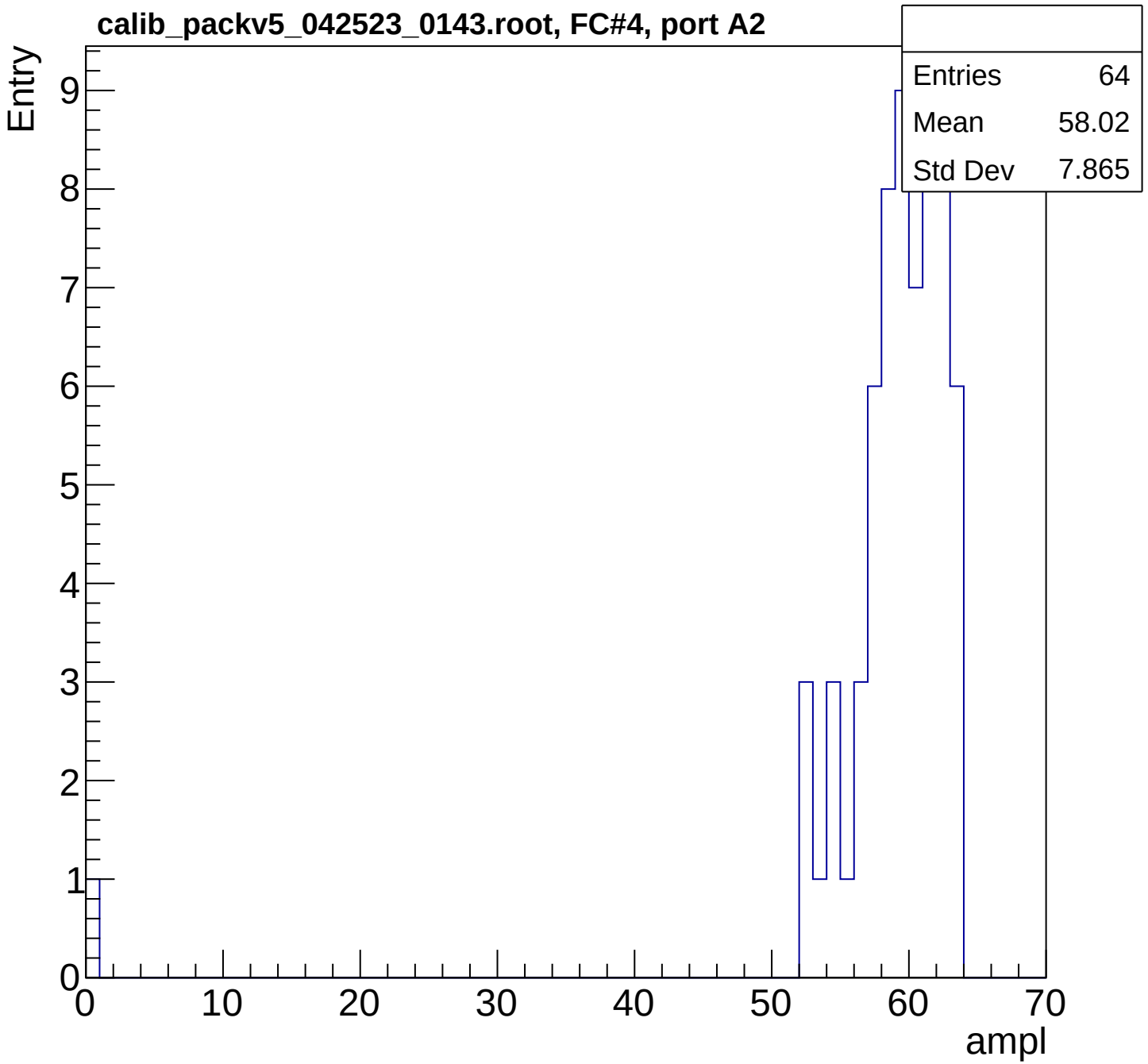
B1L100S, U5-ch50, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 58.02
Std Dev 7.865
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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60
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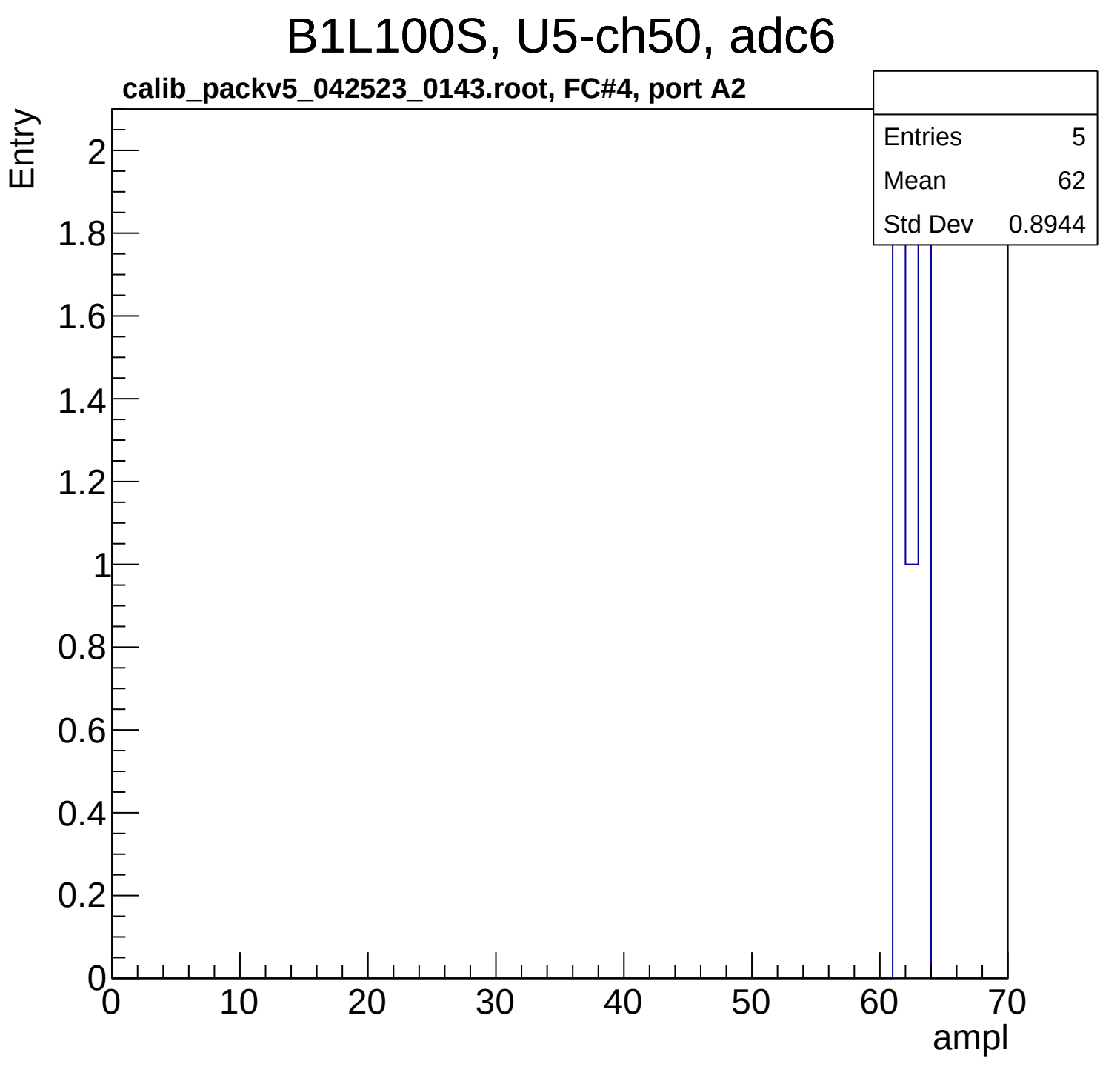
B1L100S, U5-ch50, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 5
Mean 62
Std Dev 0.8944
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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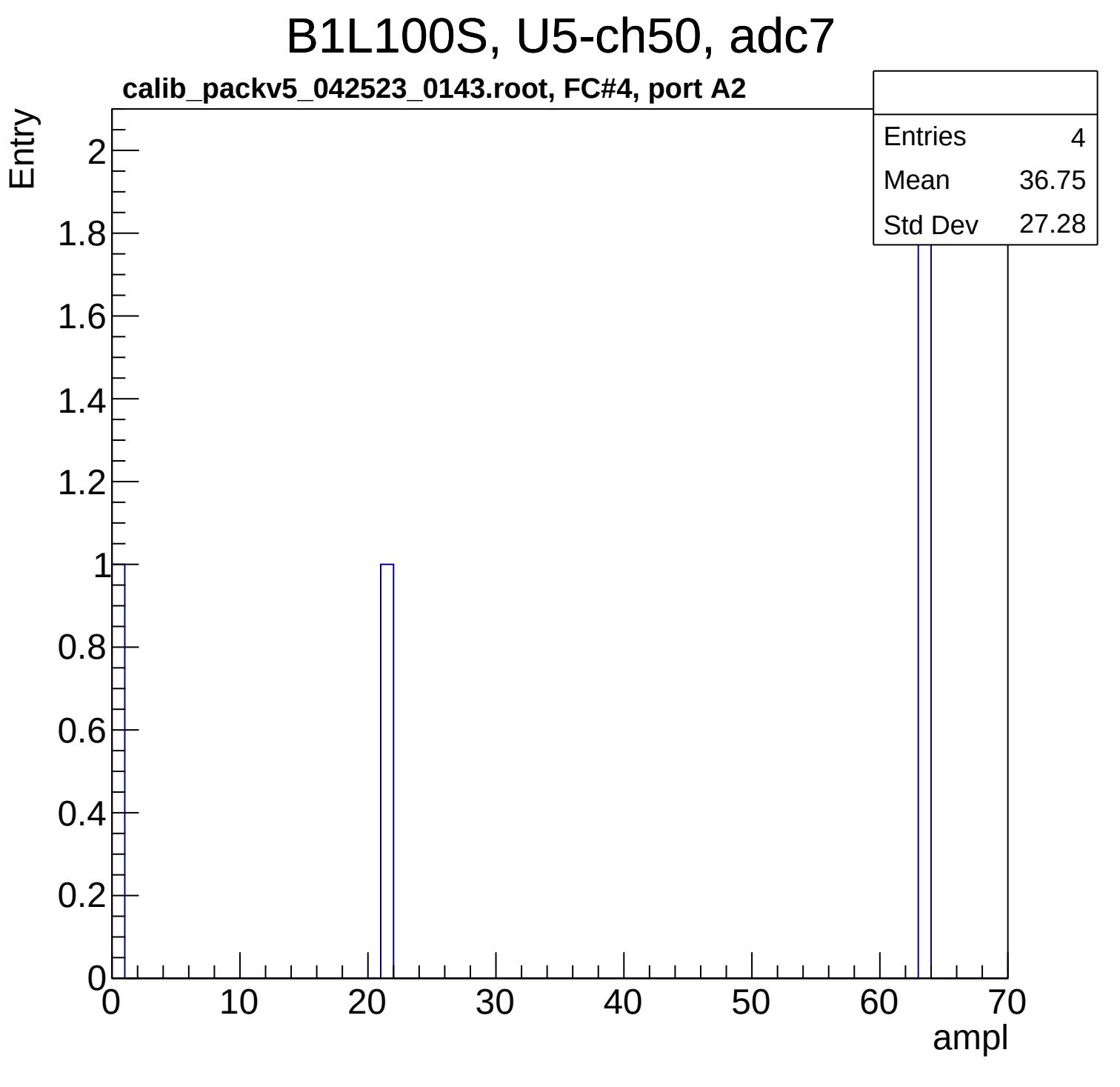
B1L100S, U5-ch50, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 4
Mean 36.75
Std Dev 27.28
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
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40
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60
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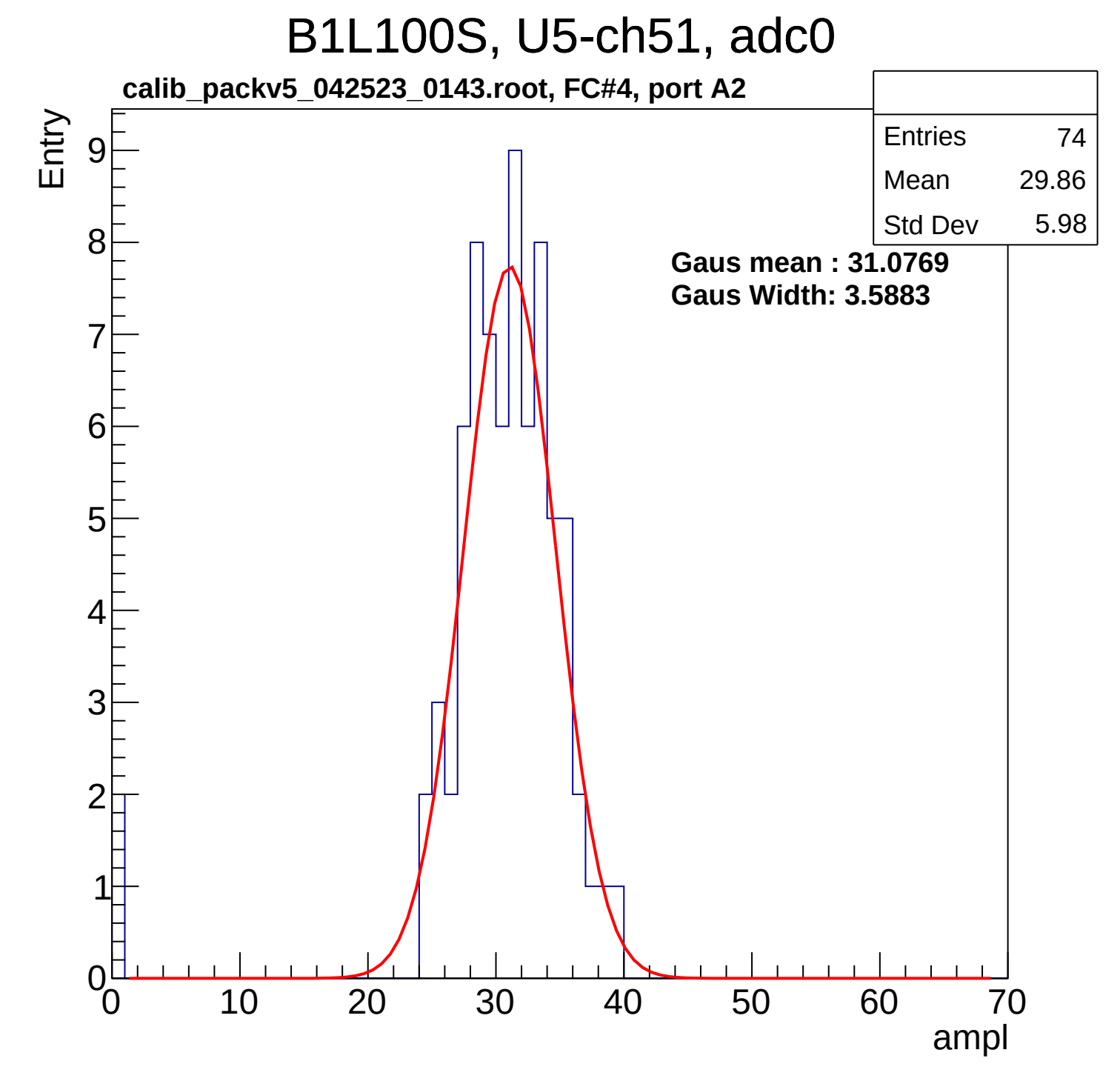
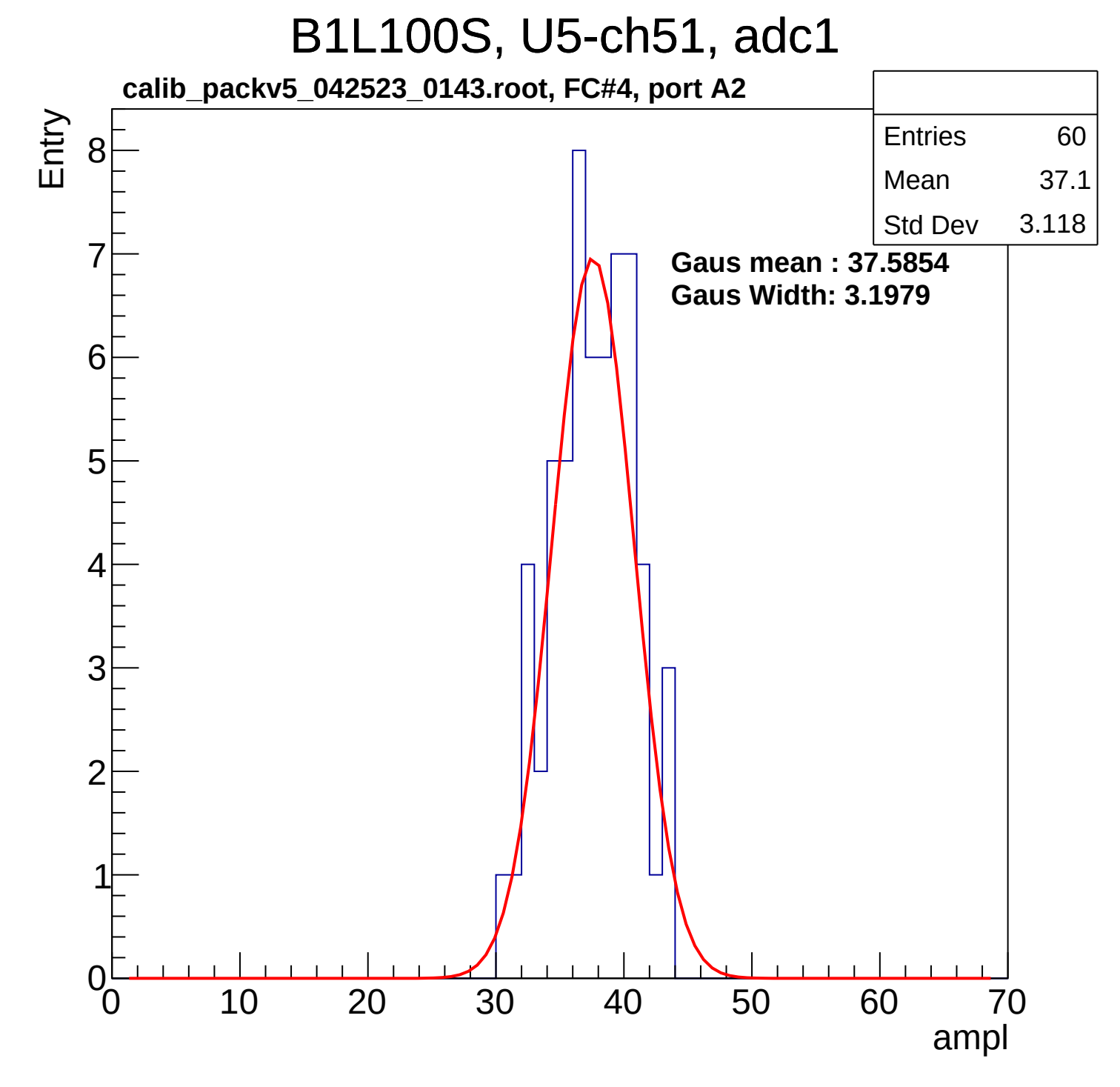

B1L100S, U5-ch51, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 74
Mean 29.86
Std Dev 5.98
Gaus mean : 31.0769
Gaus Width: 3.5883
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch51, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 37.1
Std Dev 3.118
Gaus mean : 37.5854
Gaus Width: 3.1979
Entry
ampl
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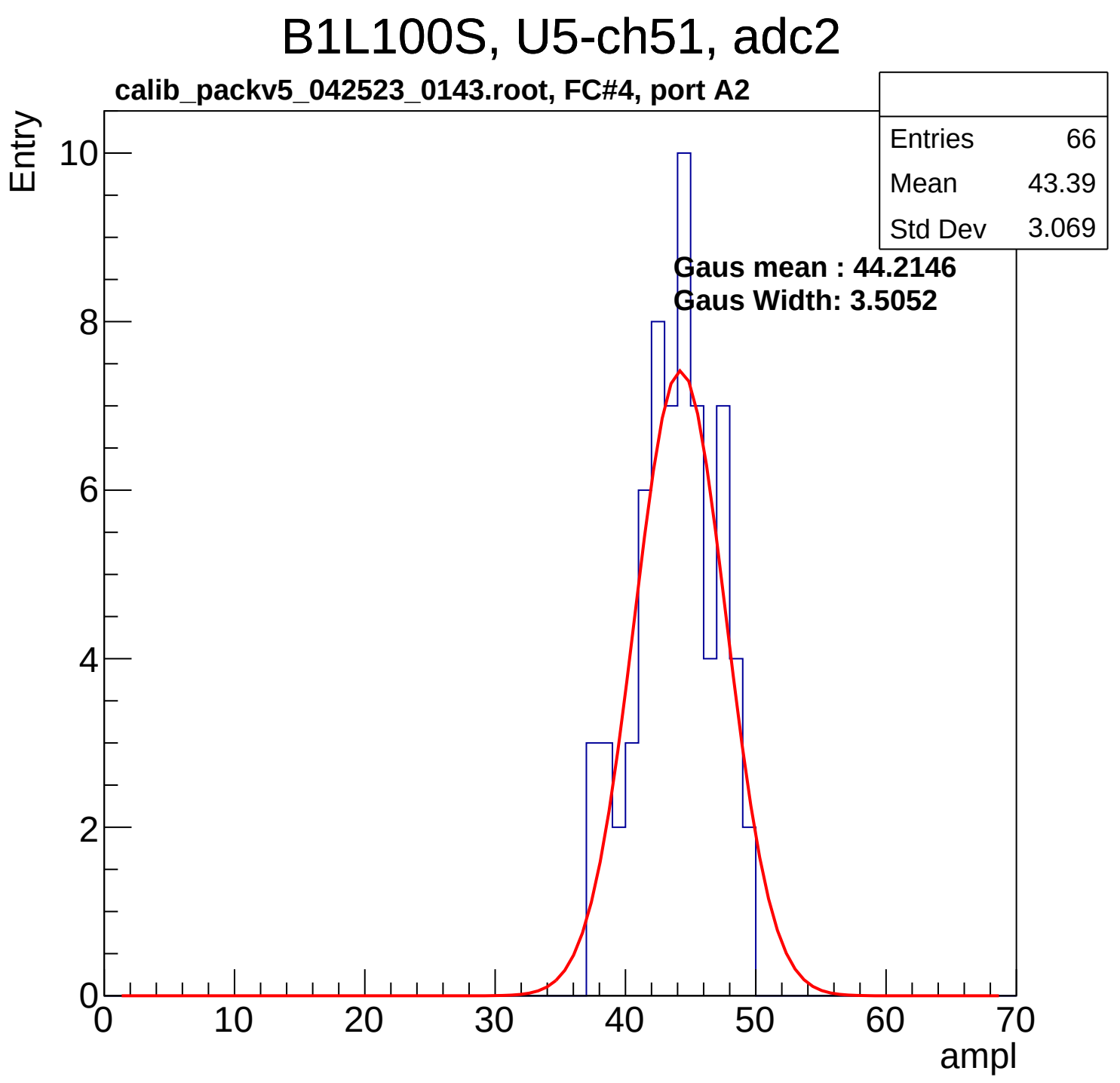
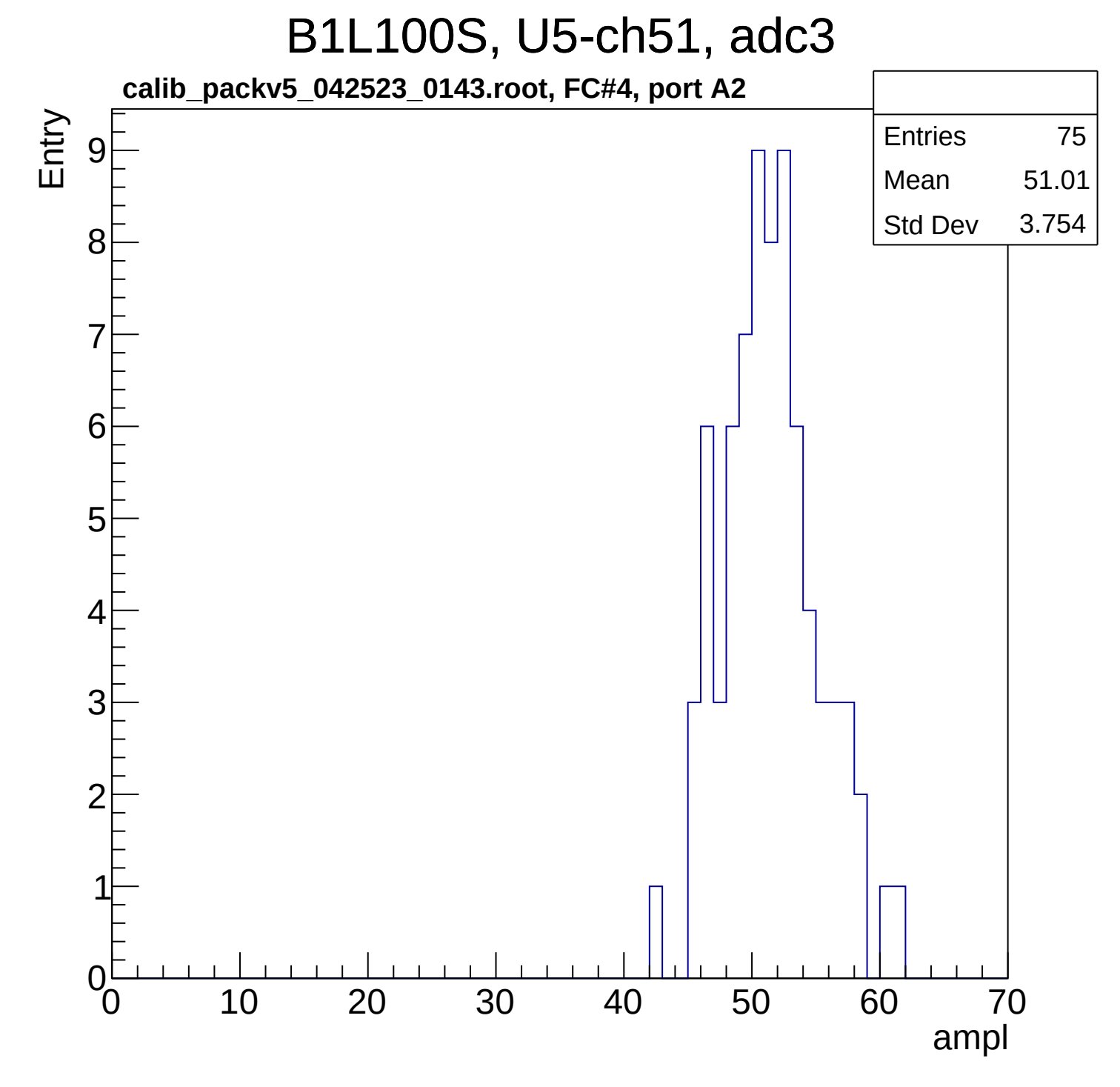
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch51, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 43.39
Std Dev 3.069
Gaus mean : 44.2146
Gaus Width: 3.5052
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch51, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 75
Mean 51.01
Std Dev 3.754
Entry
ampl
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2
3
4
5
6
7
8
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0
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60
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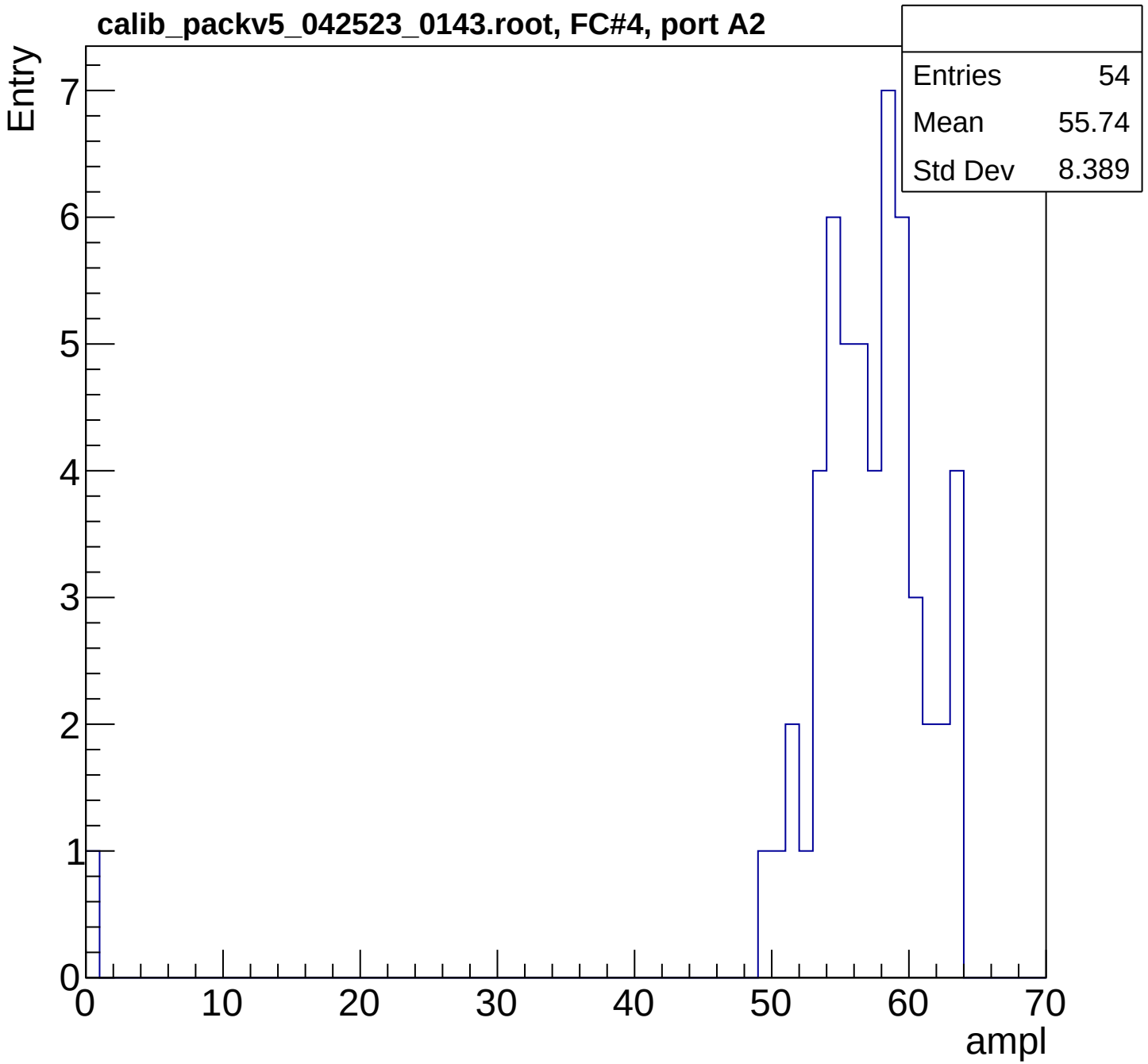
B1L100S, U5-ch51, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 55.74
Std Dev 8.389
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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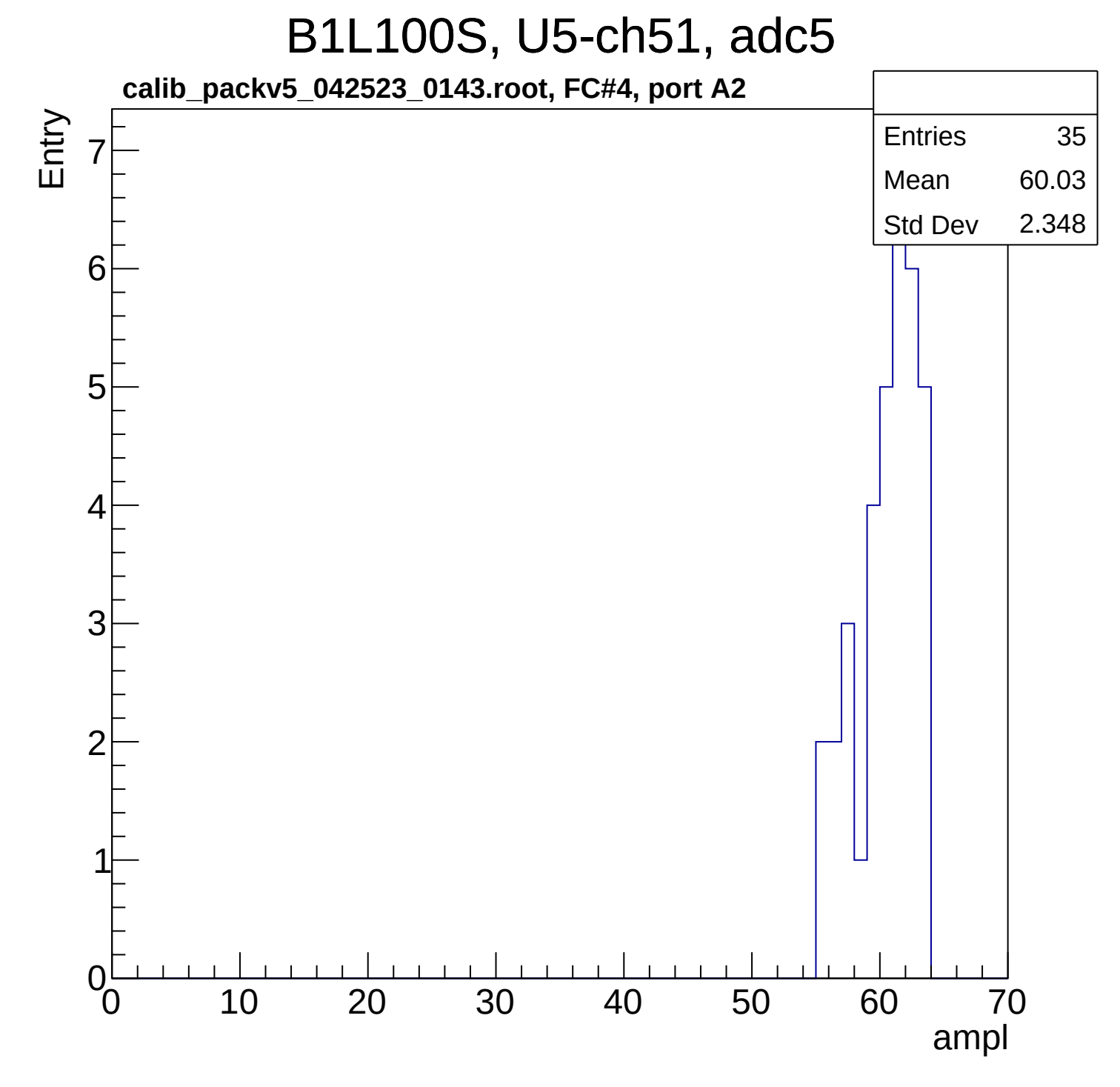
40
50
60
70


B1L100S, U5-ch51, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 35
Mean 60.03
Std Dev 2.348
Entry
ampl
0
1
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3
4
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6
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0
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20
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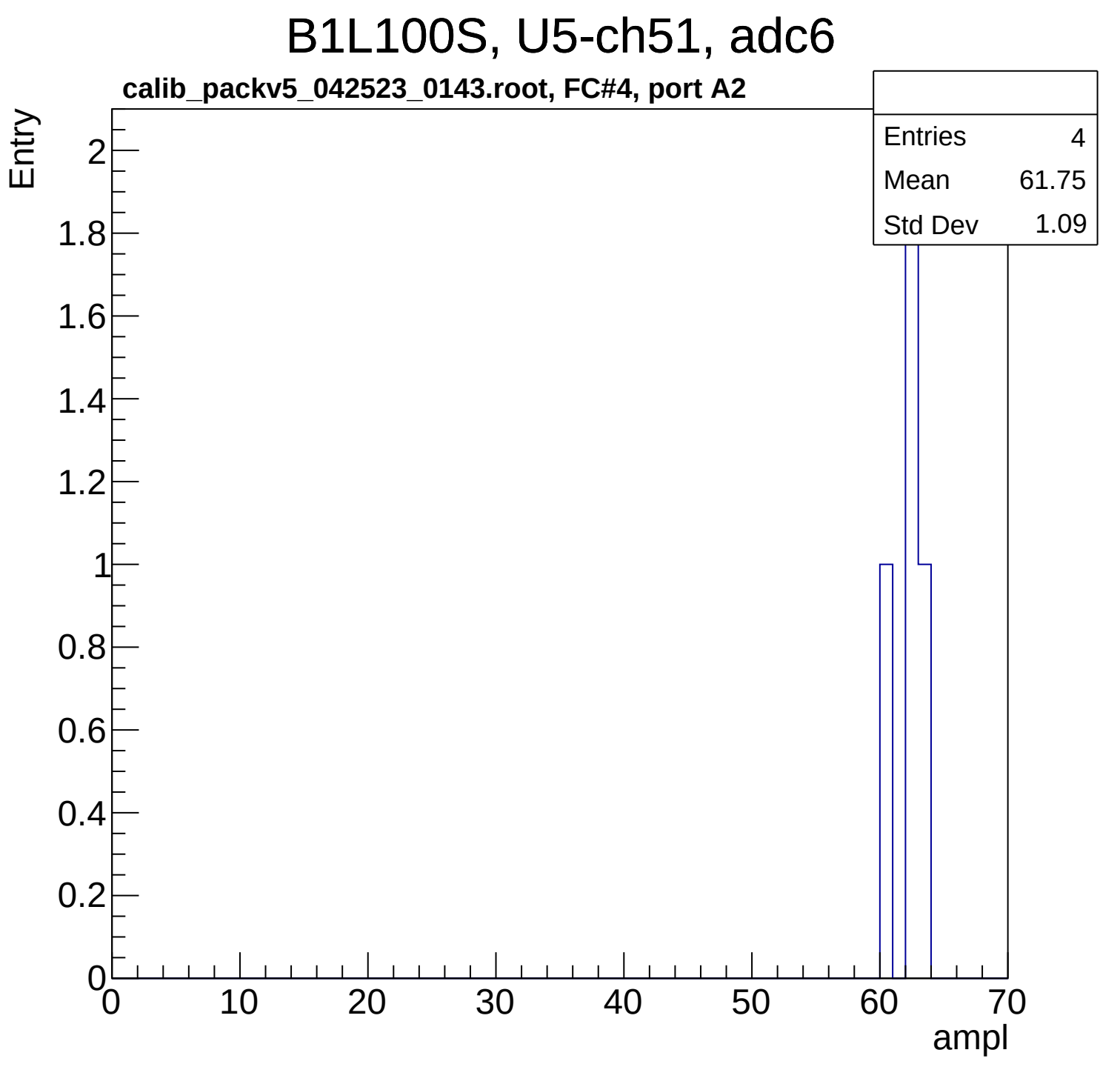
60
70


B1L100S, U5-ch51, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 4
Mean 61.75
Std Dev 1.09
Entry
ampl
0
0.2
0.4
0.6
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1
1.2
1.4
1.6
1.8
2
0
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60
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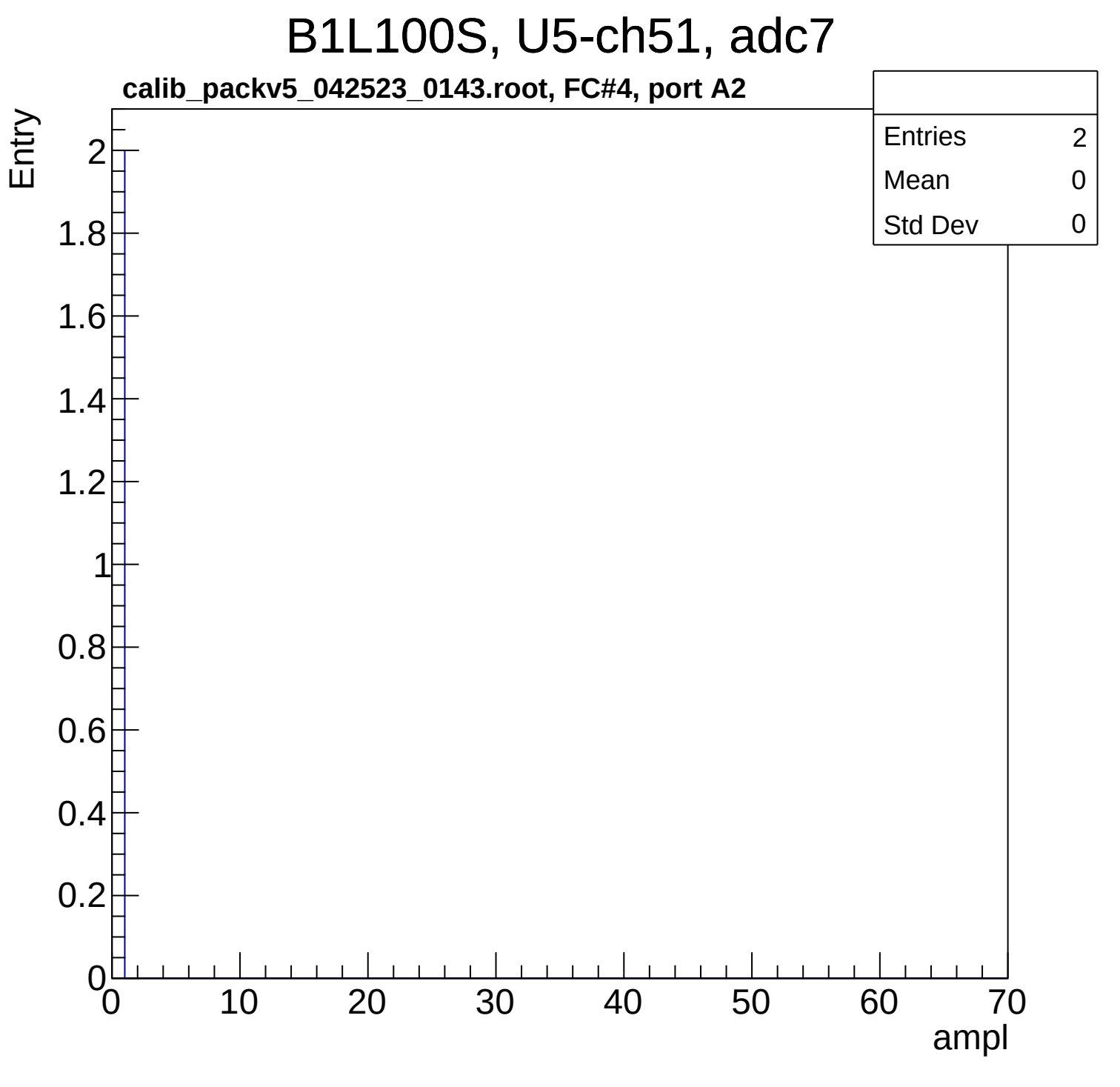
B1L100S, U5-ch51, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
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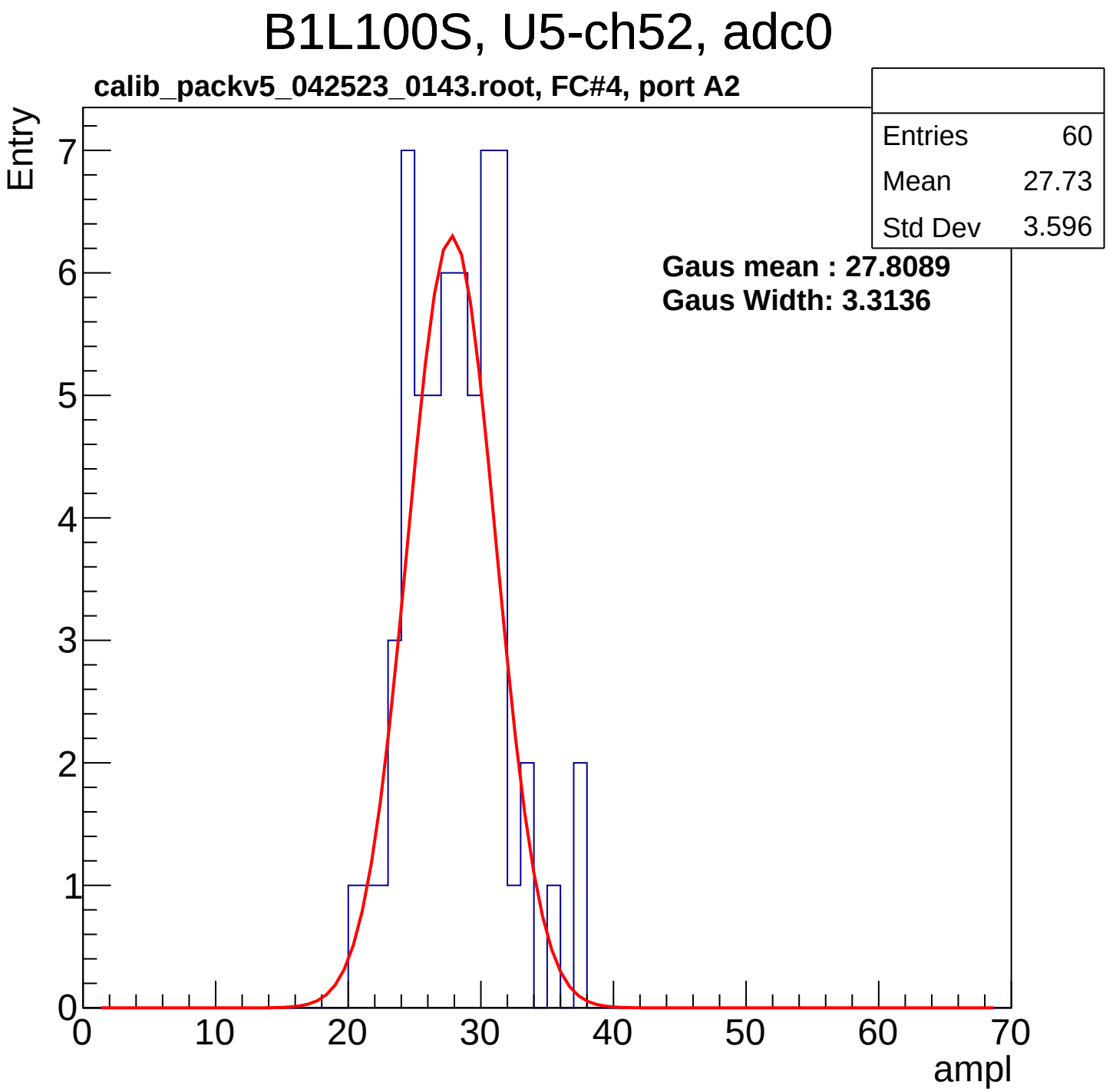
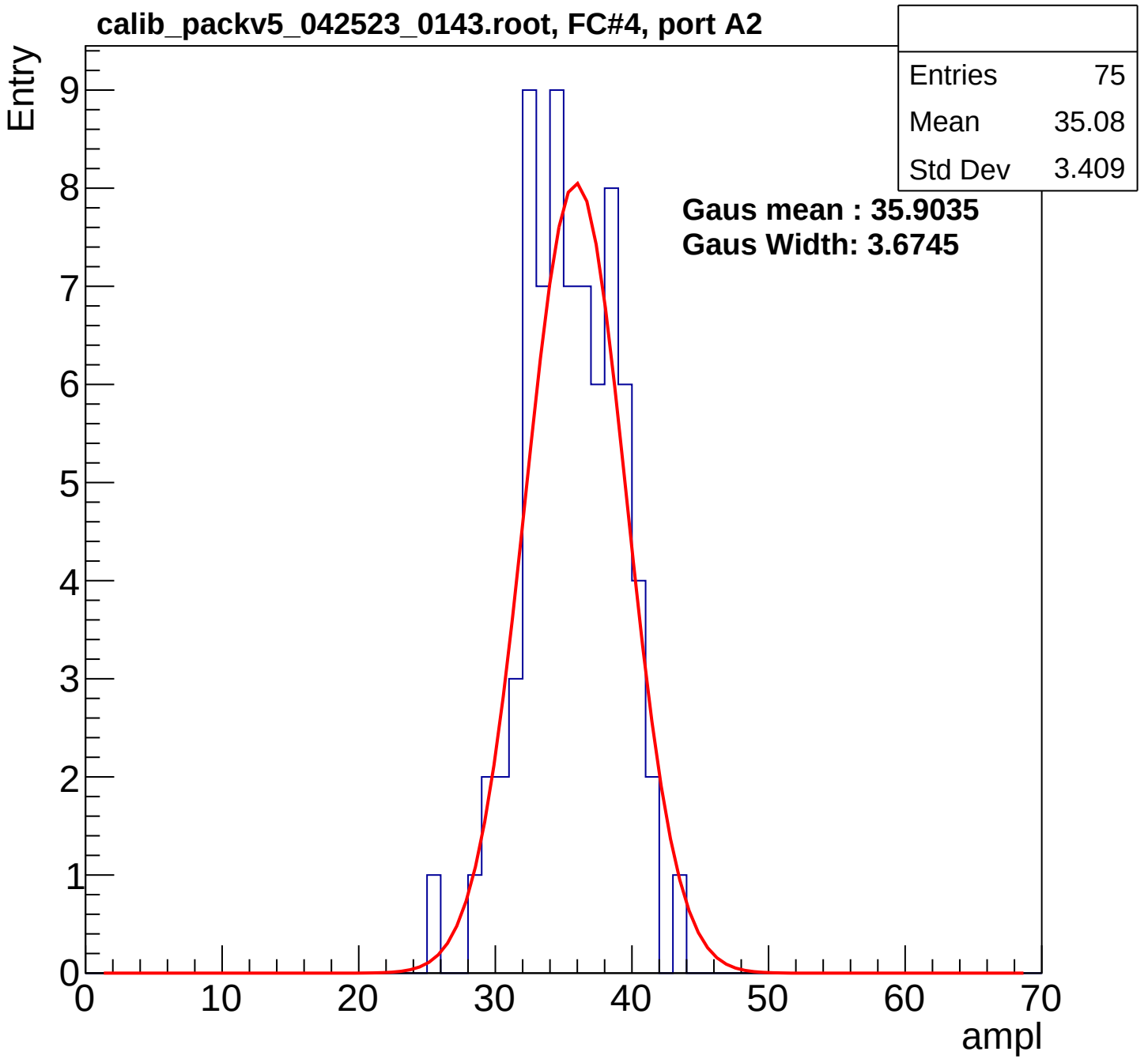
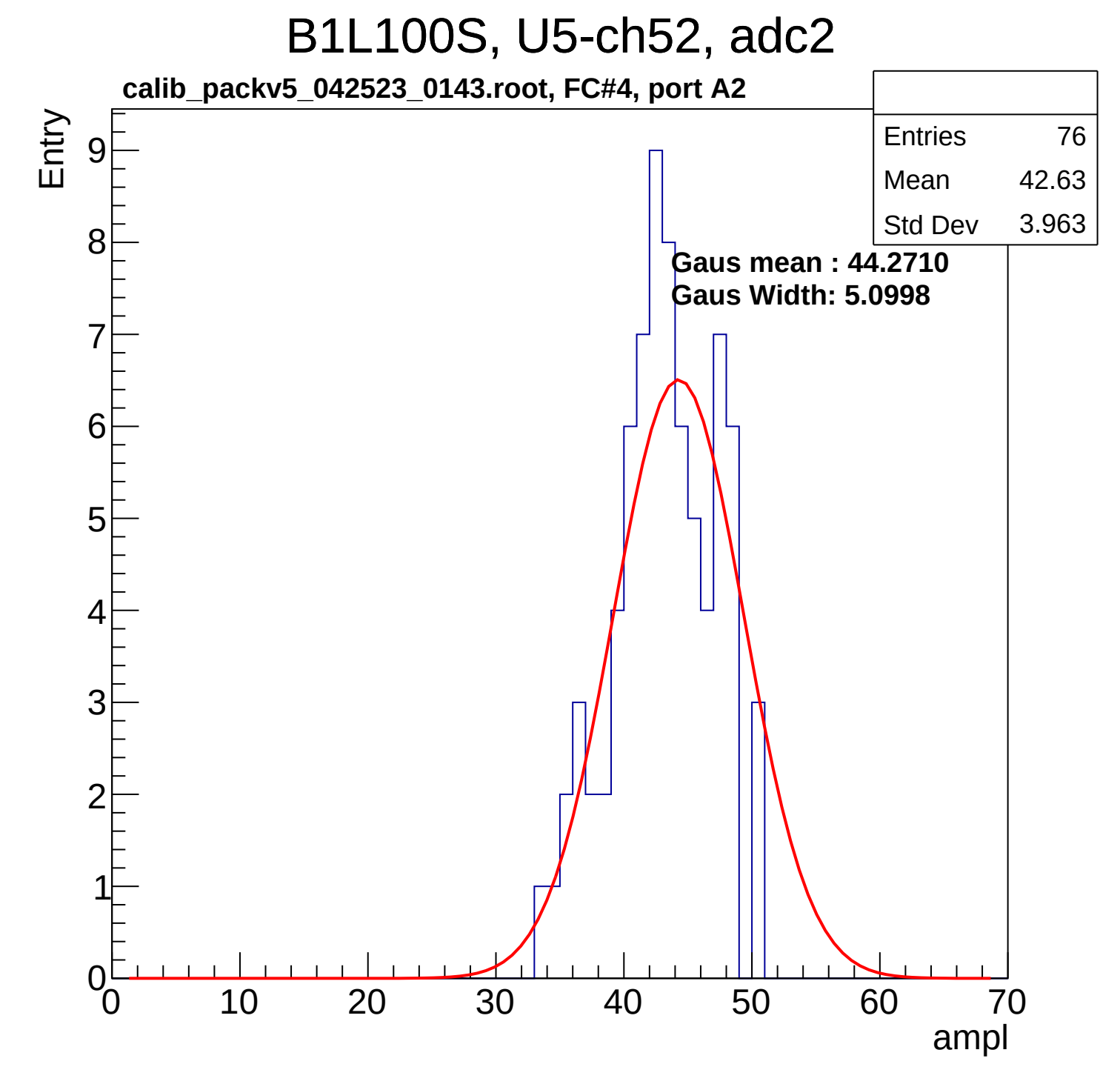
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch52, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 27.73
Std Dev 3.596
Gaus mean : 27.8089
Gaus Width: 3.3136
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U5-ch52, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 75
Mean 35.08
Std Dev 3.409
Gaus mean : 35.9035
Gaus Width: 3.6745
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch52, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 76
Mean 42.63
Std Dev 3.963
Gaus mean : 44.2710
Gaus Width: 5.0998
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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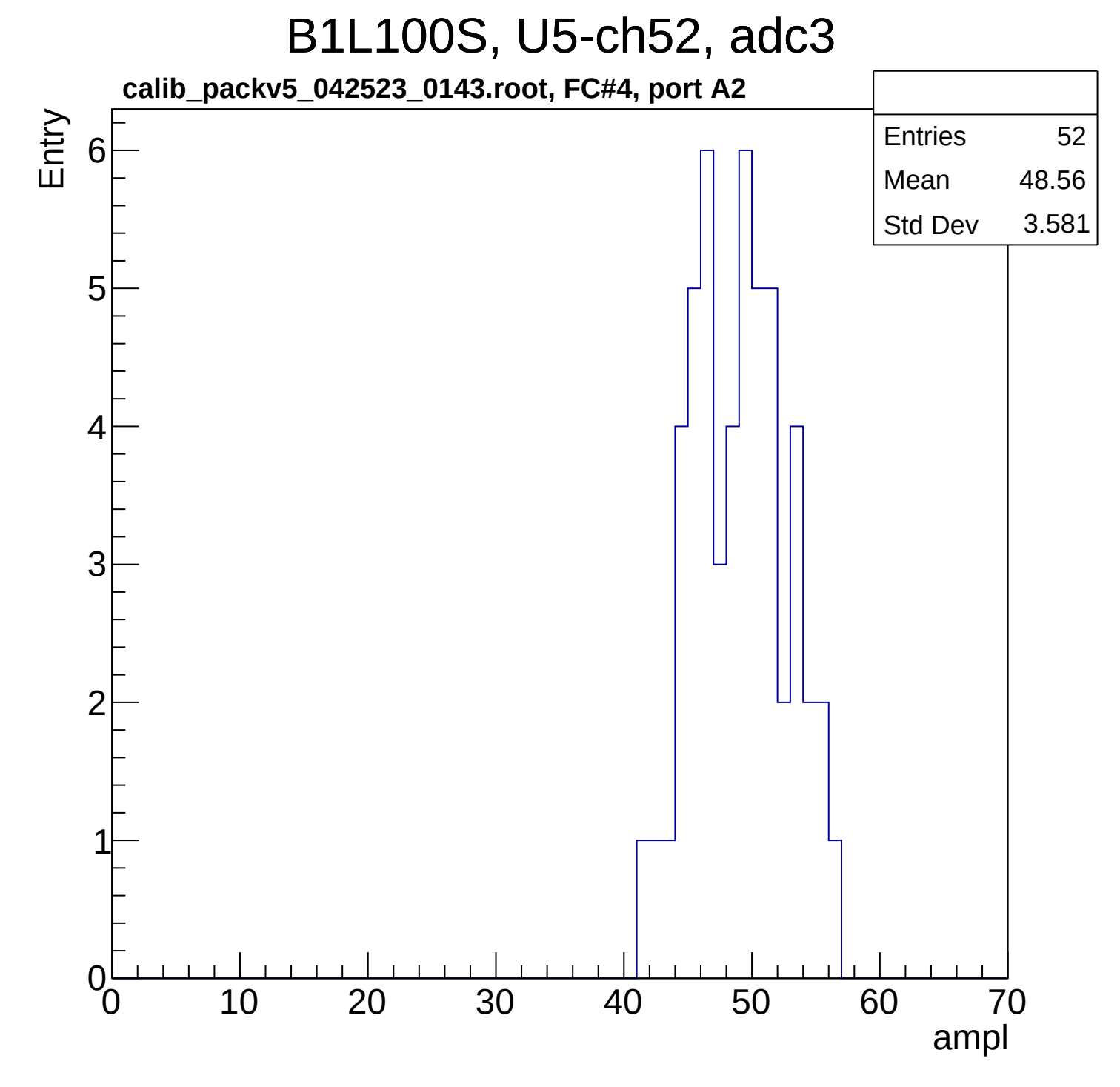
B1L100S, U5-ch52, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 52
Mean 48.56
Std Dev 3.581
Entry
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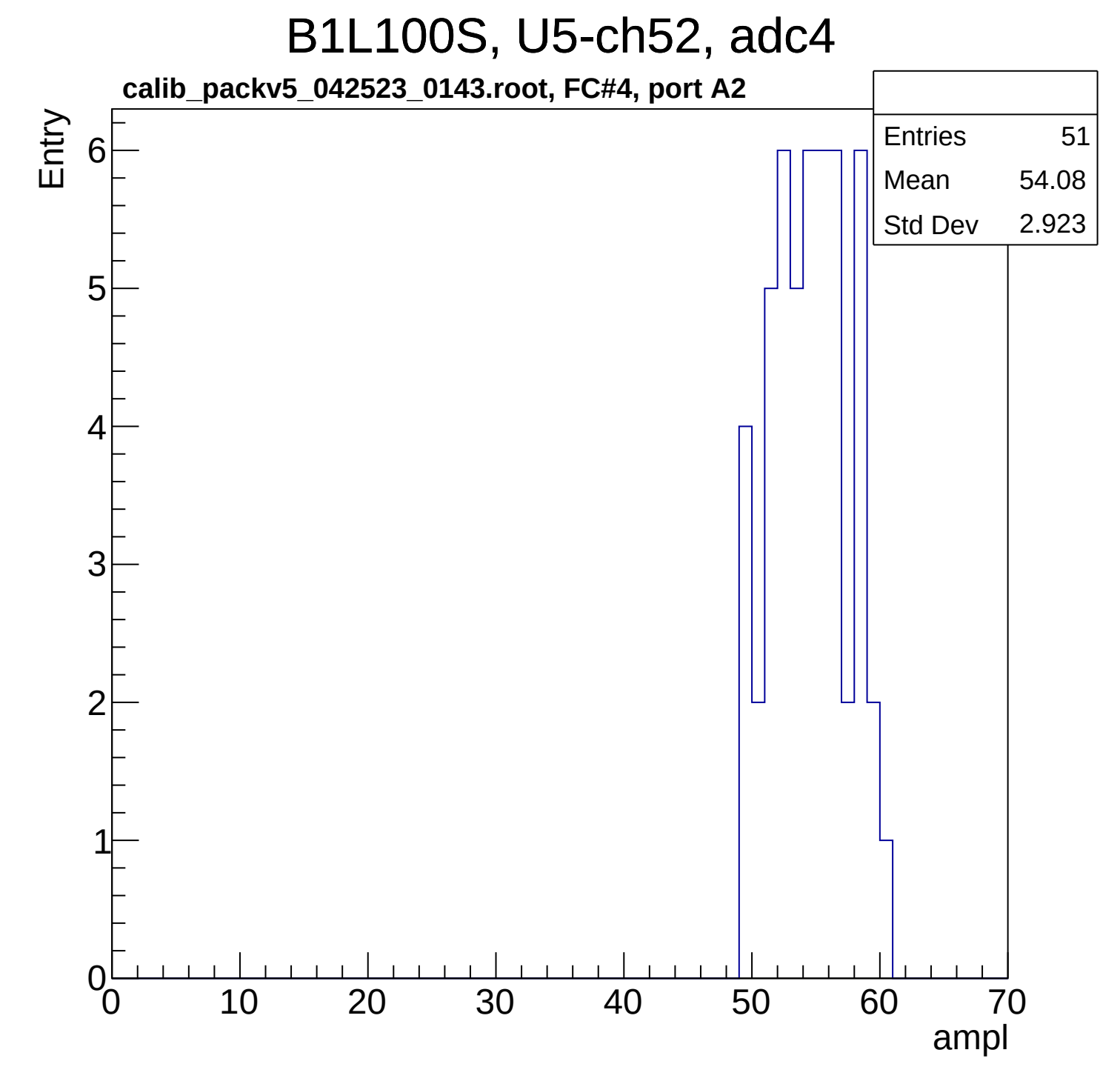
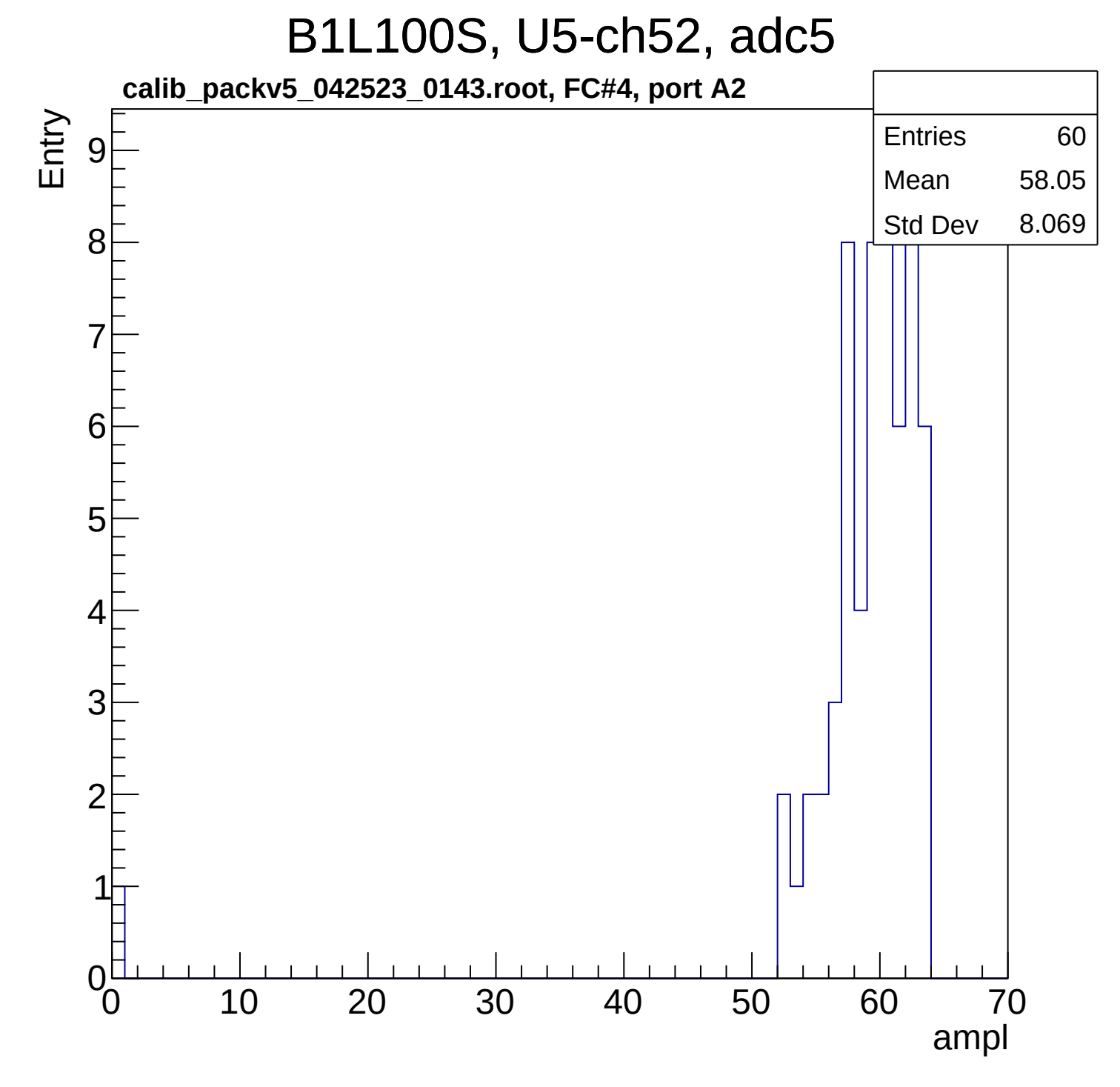
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch52, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 54.08
Std Dev 2.923
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L100S, U5-ch52, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 58.05
Std Dev 8.069
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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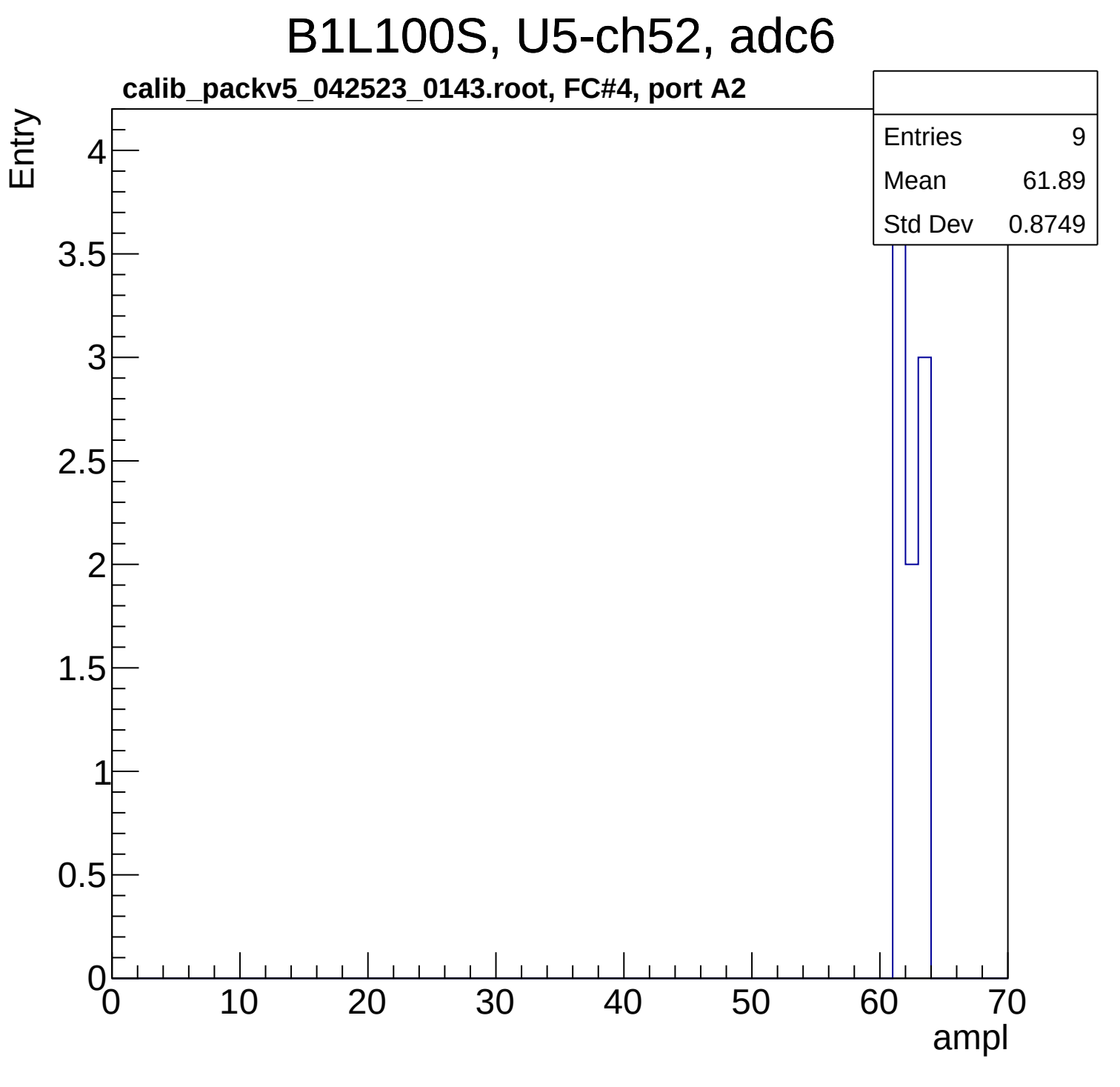
B1L100S, U5-ch52, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 9
Mean 61.89
Std Dev 0.8749
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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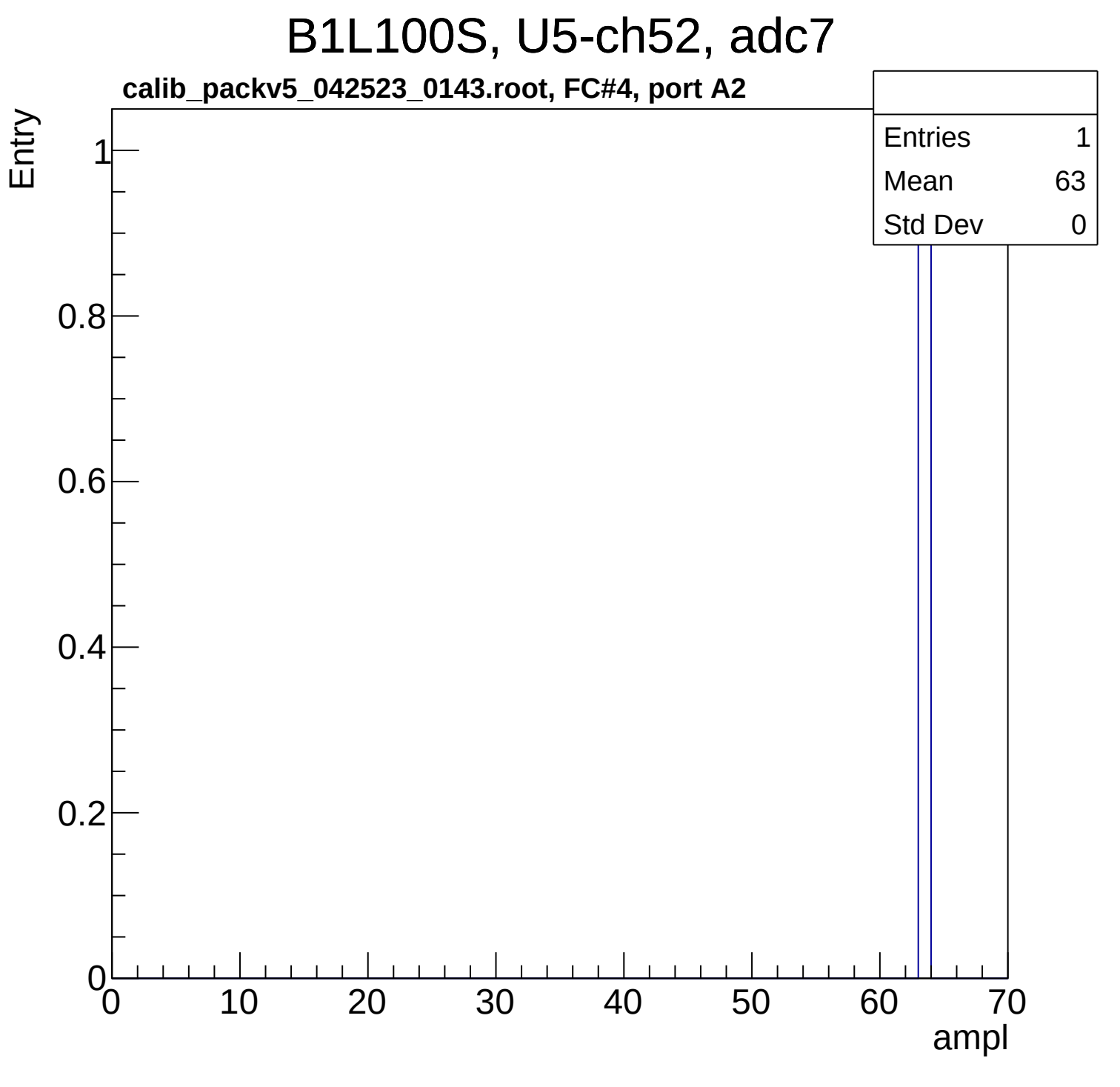
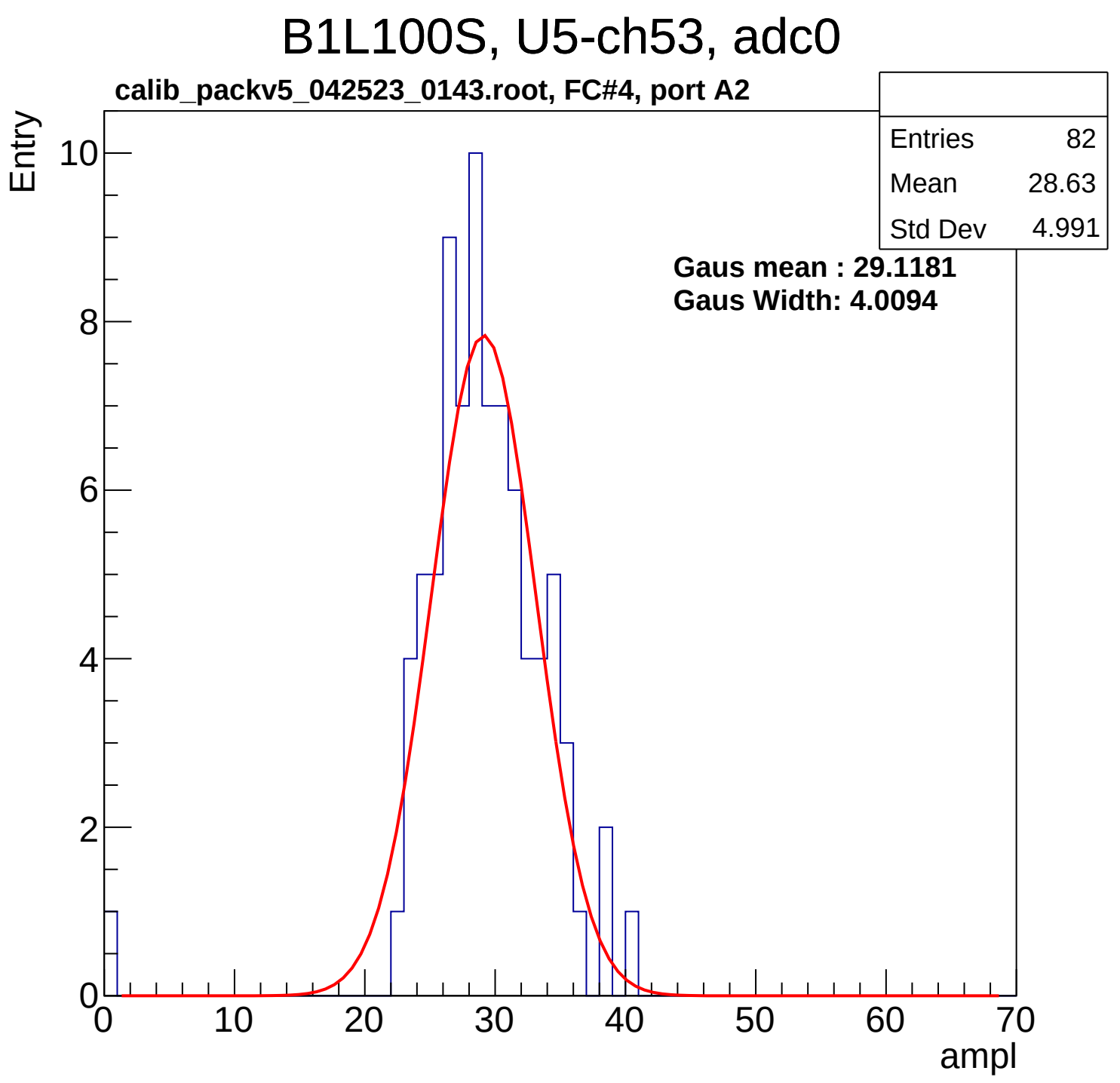
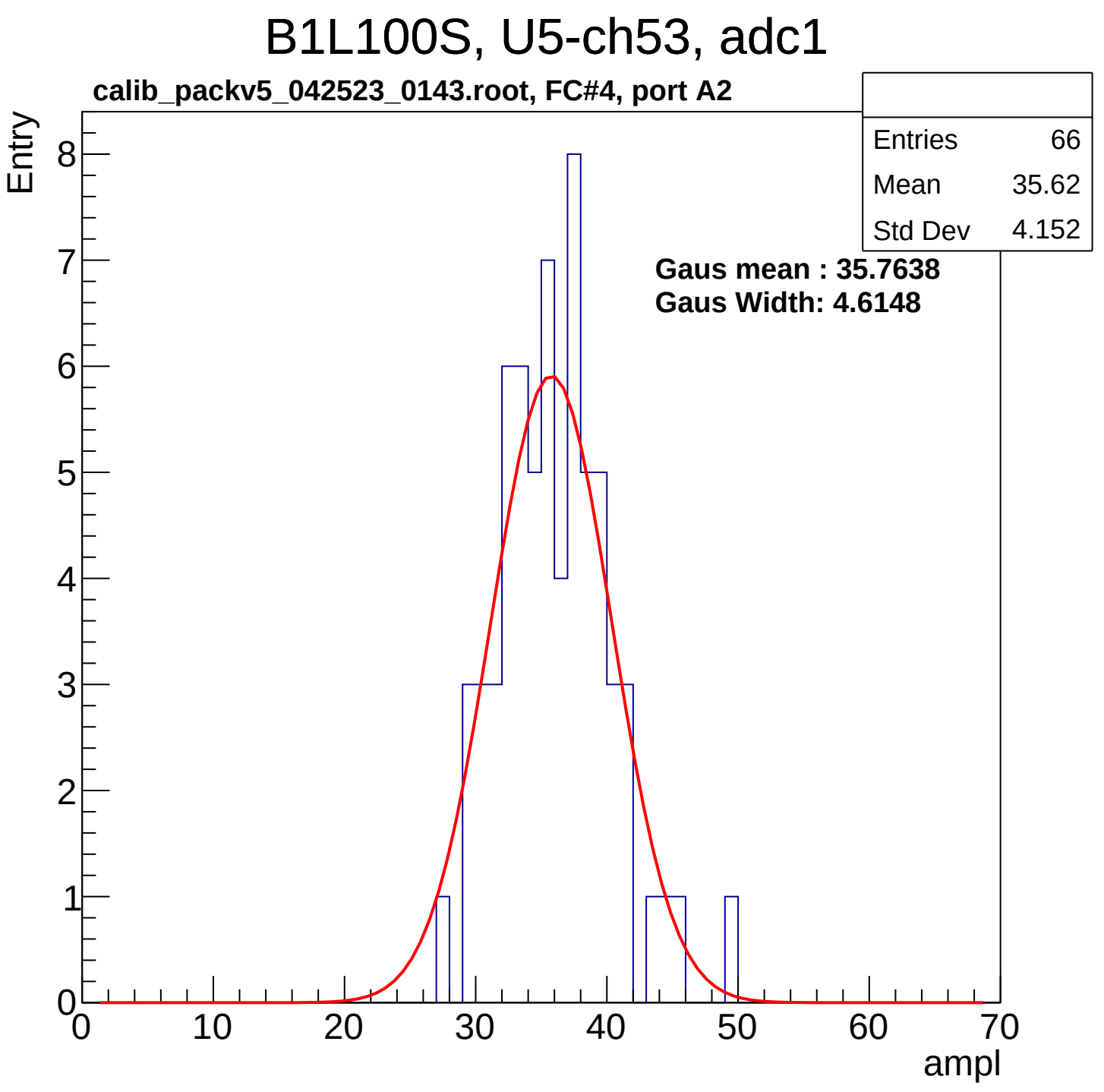
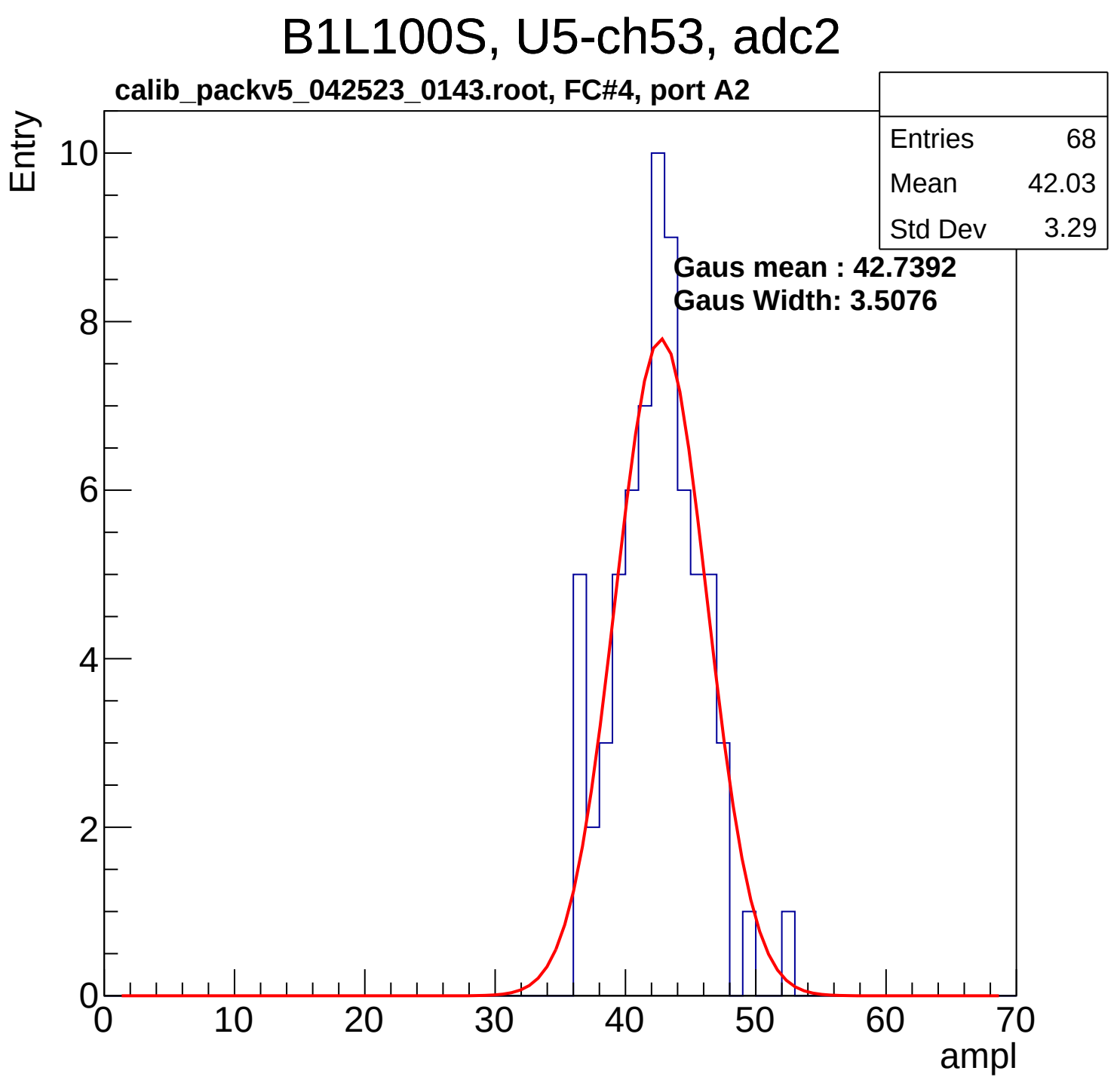
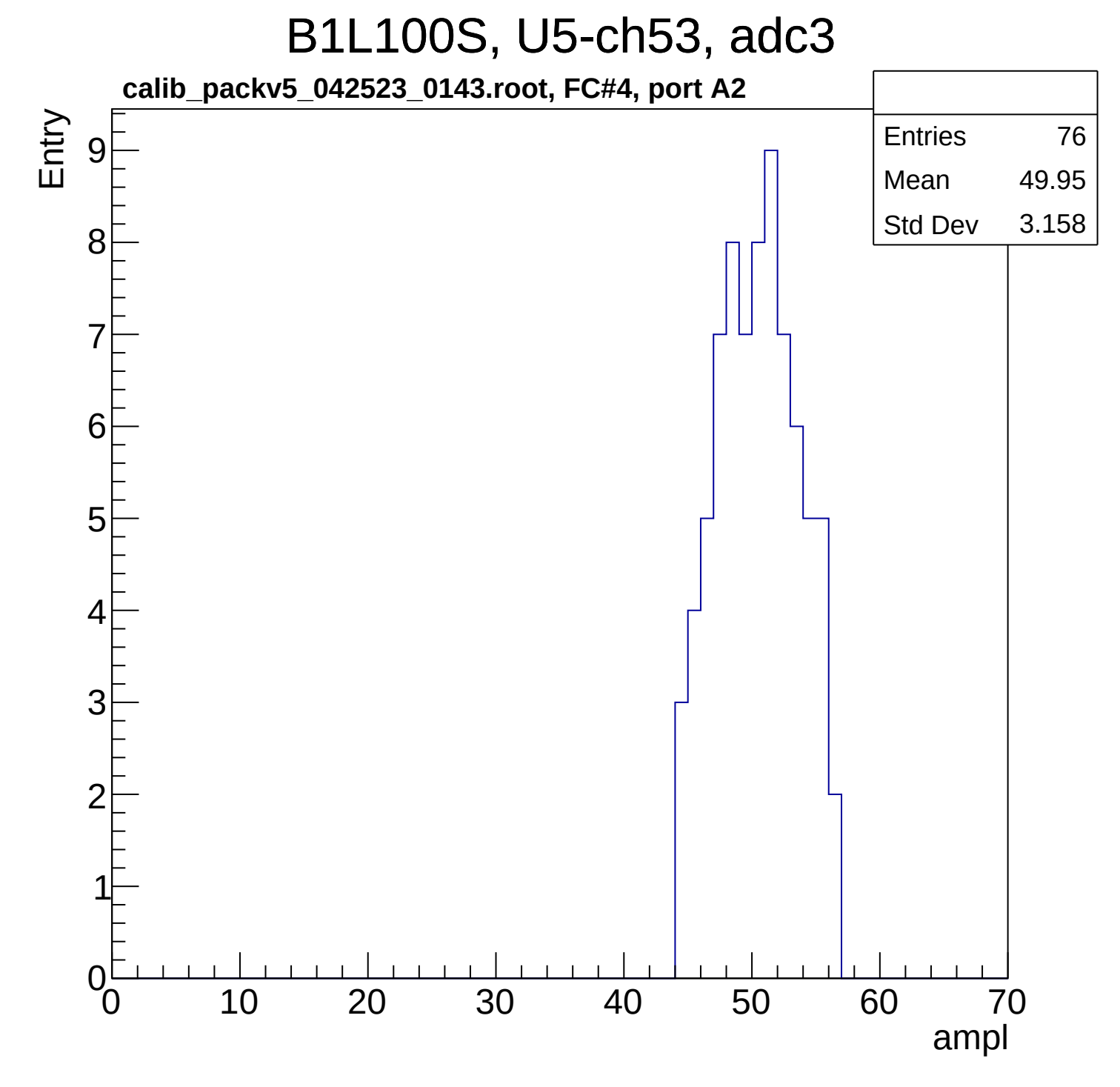
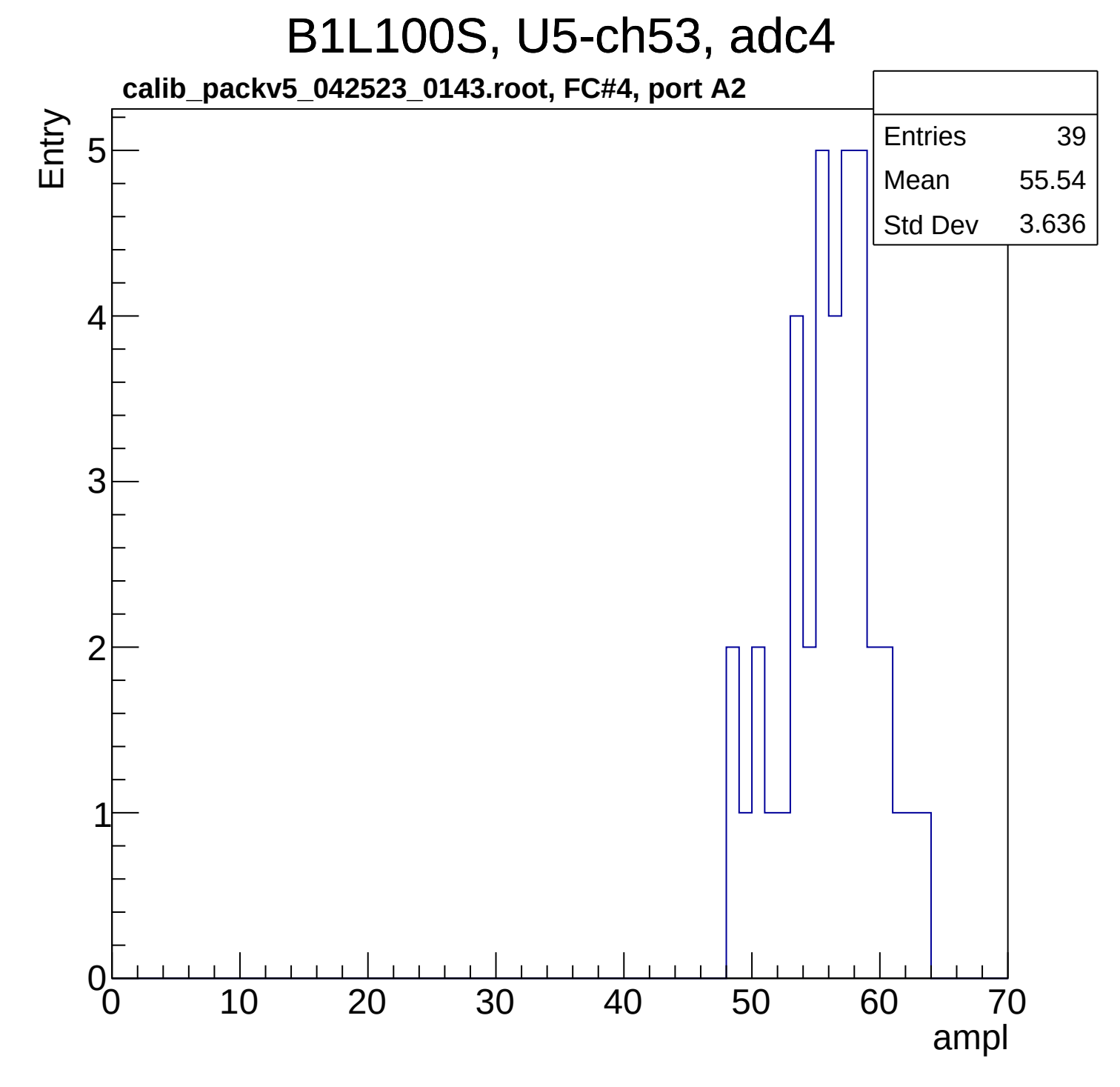

B1L100S, U5-ch52, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

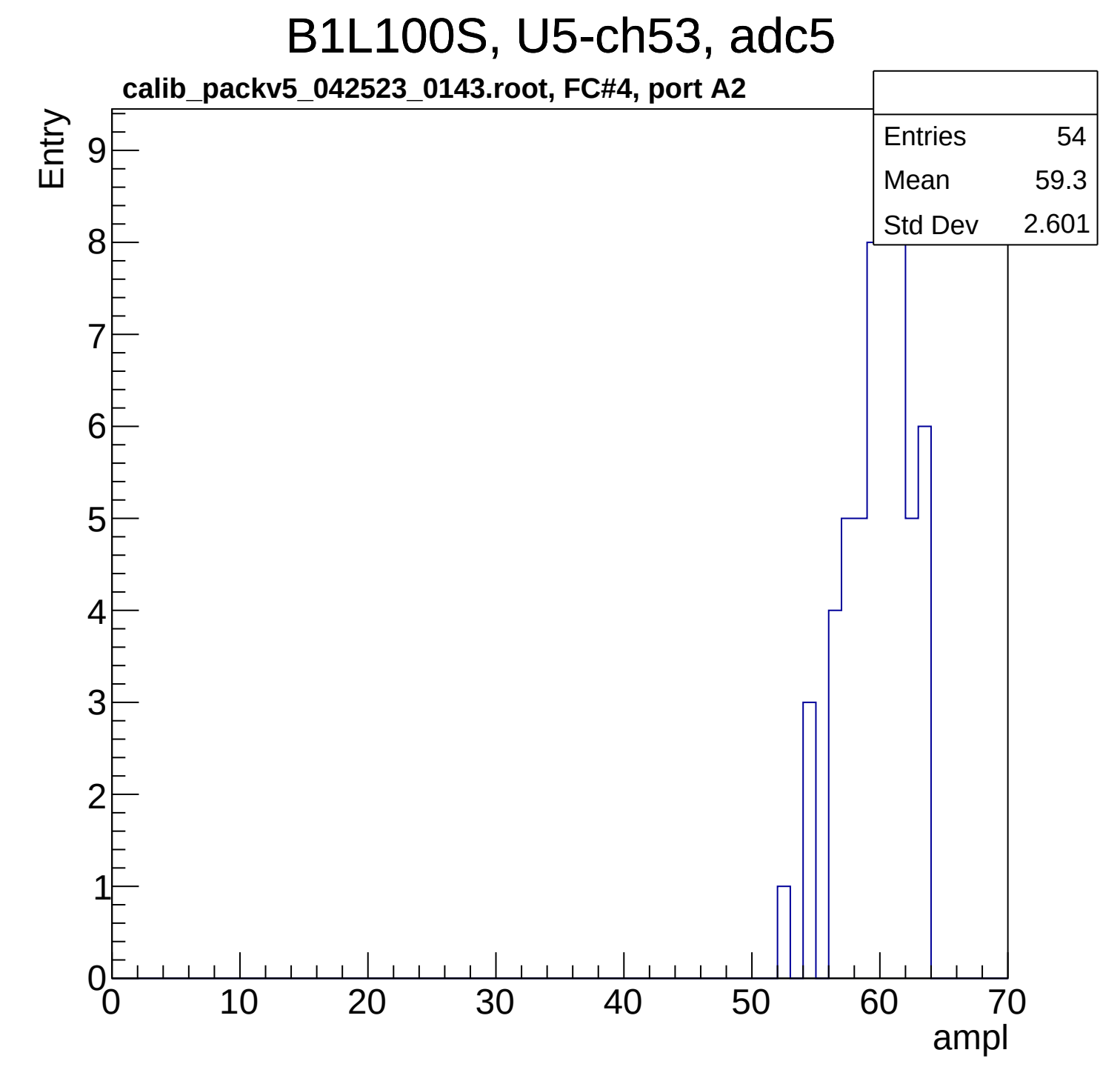

B1L100S, U5-ch53, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 82
Mean 28.63
Std Dev 4.991
Gaus mean : 29.1181
Gaus Width: 4.0094
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

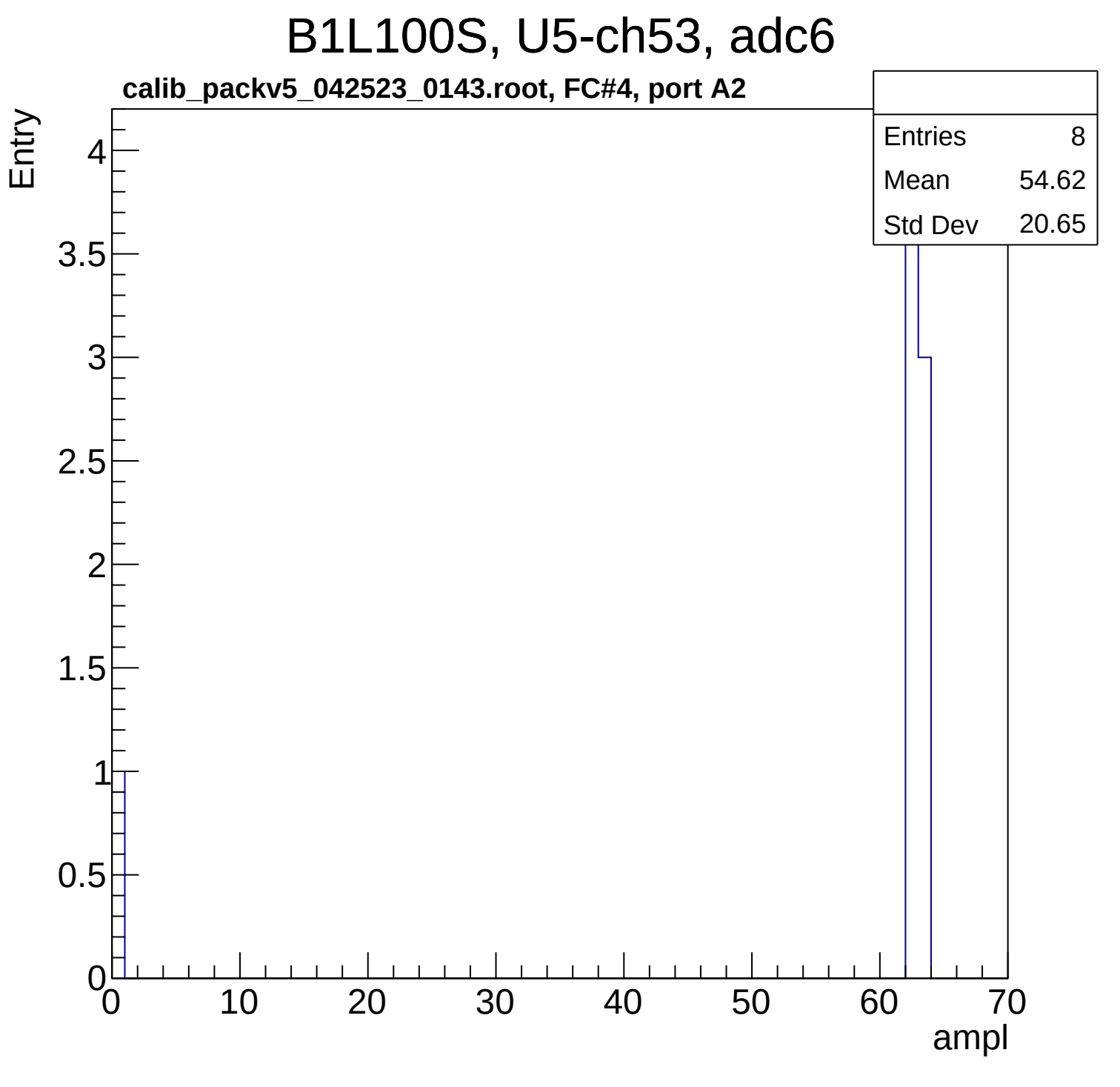

B1L100S, U5-ch53, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 35.62
Std Dev 4.152
Gaus mean : 35.7638
Gaus Width: 4.6148
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

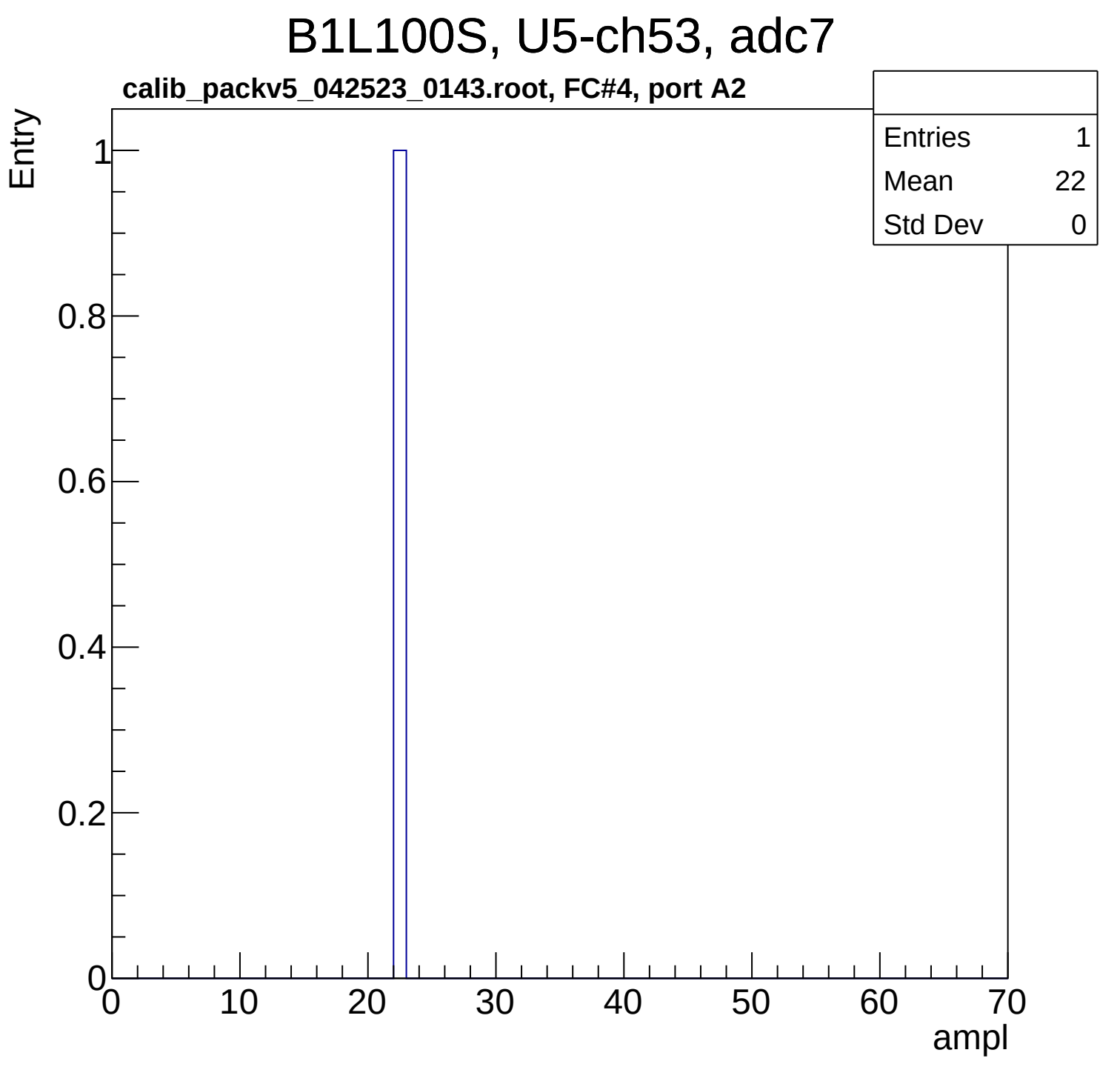

B1L100S, U5-ch53, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 42.03
Std Dev 3.29
Gaus mean : 42.7392
Gaus Width: 3.5076
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch53, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 76
Mean 49.95
Std Dev 3.158
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch53, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 39
Mean 55.54
Std Dev 3.636
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L100S, U5-ch53, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 59.3
Std Dev 2.601
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch53, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 8
Mean 54.62
Std Dev 20.65
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L100S, U5-ch53, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 22
Std Dev 0
Entry
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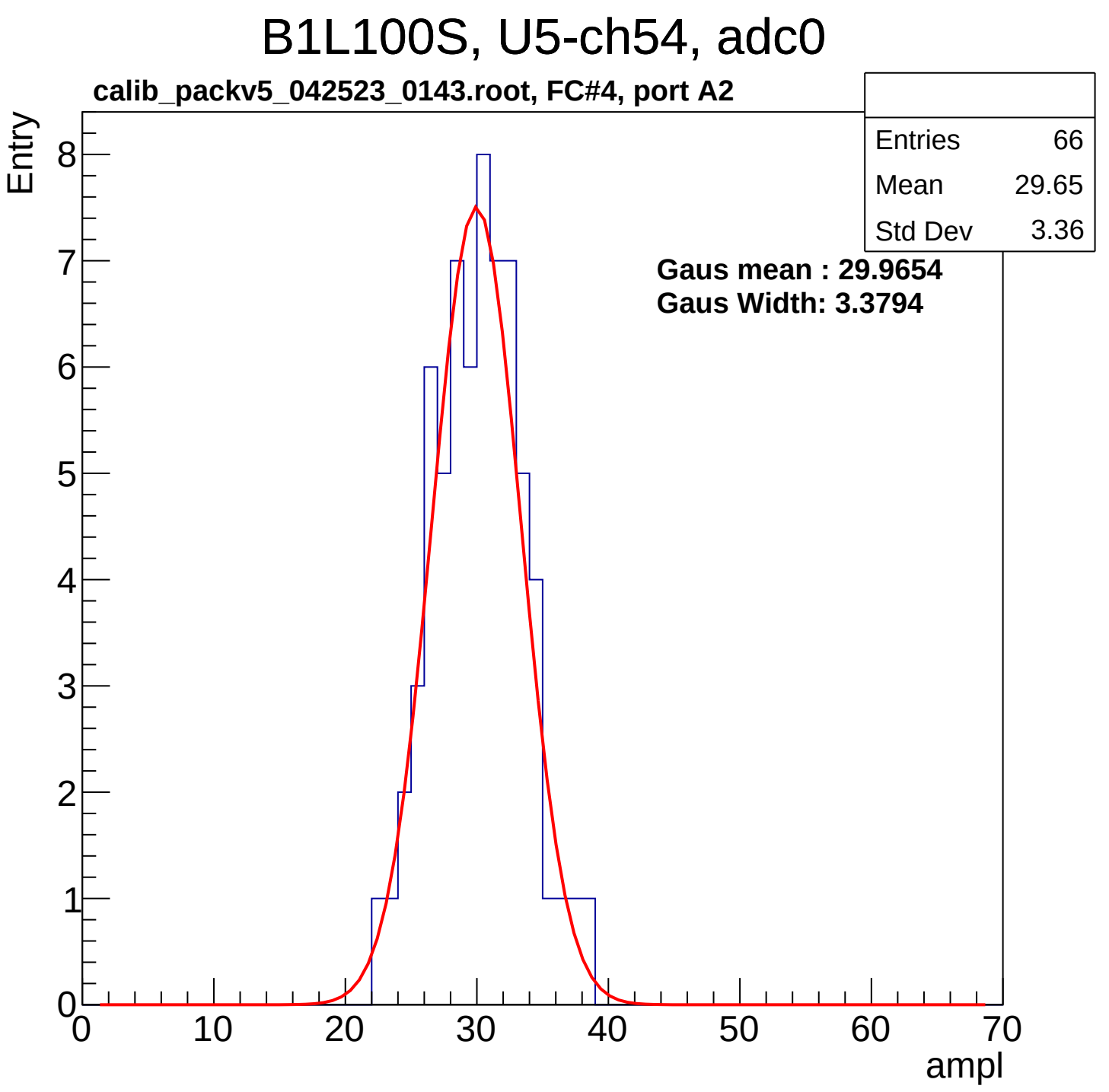
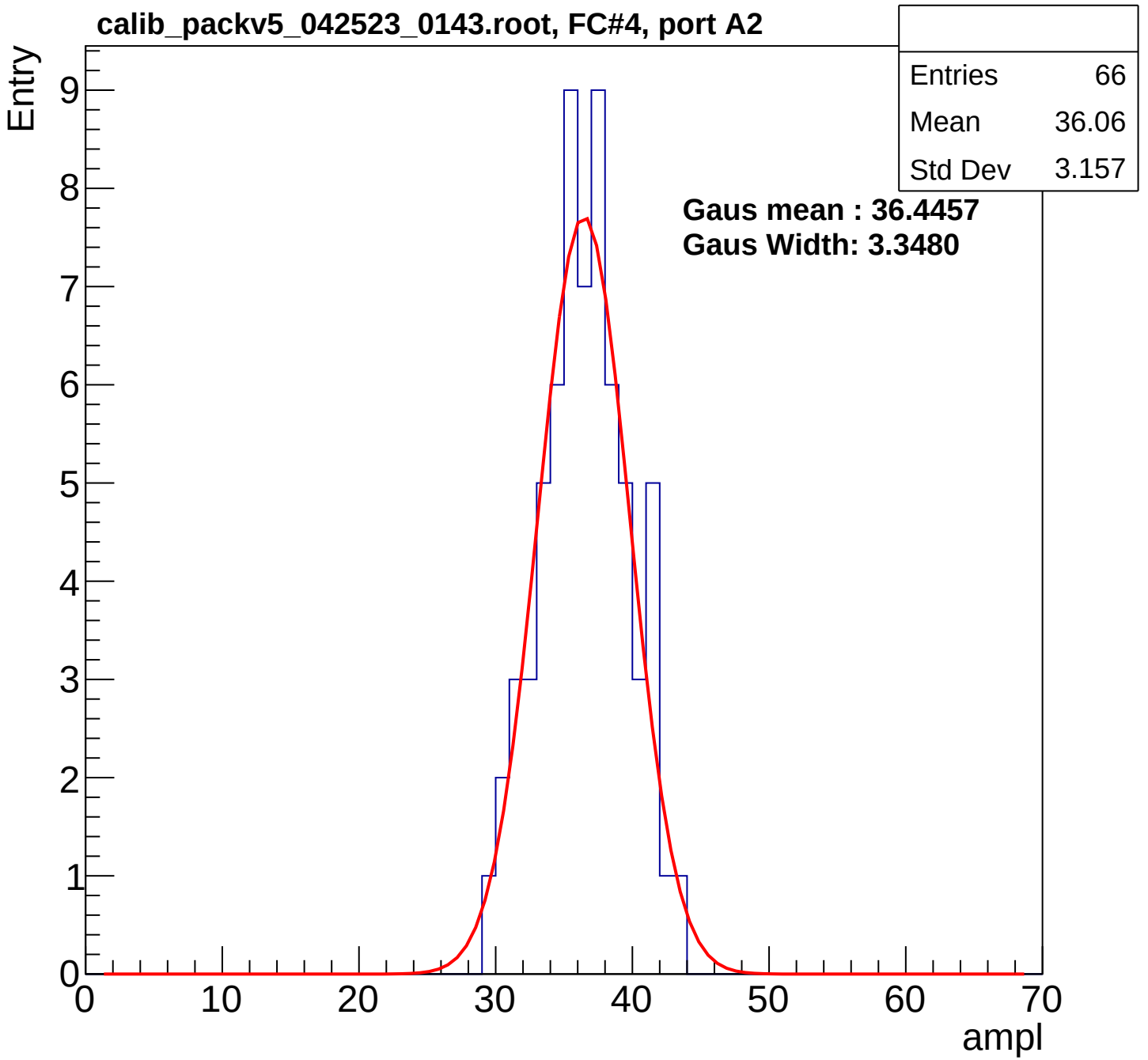
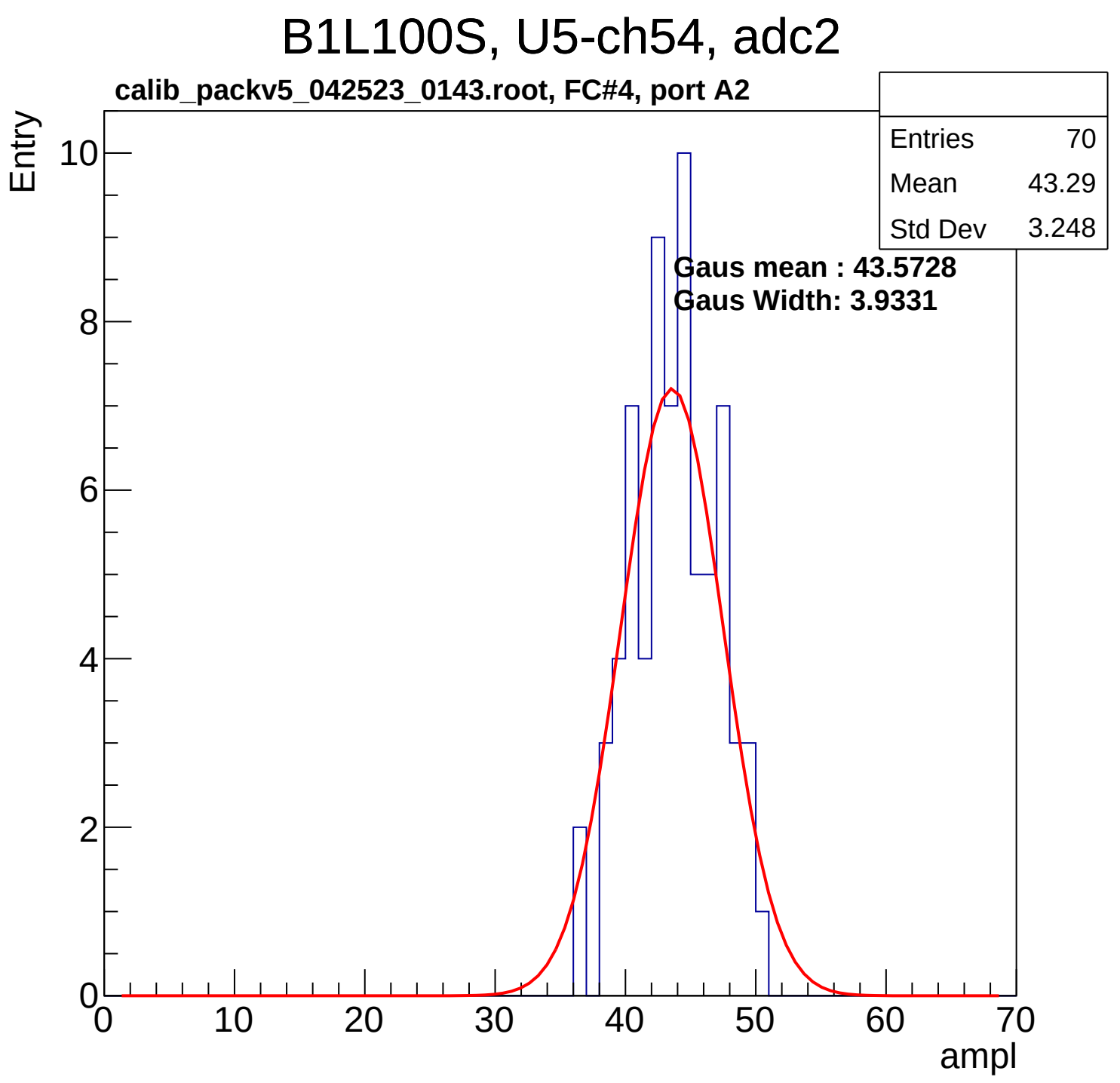
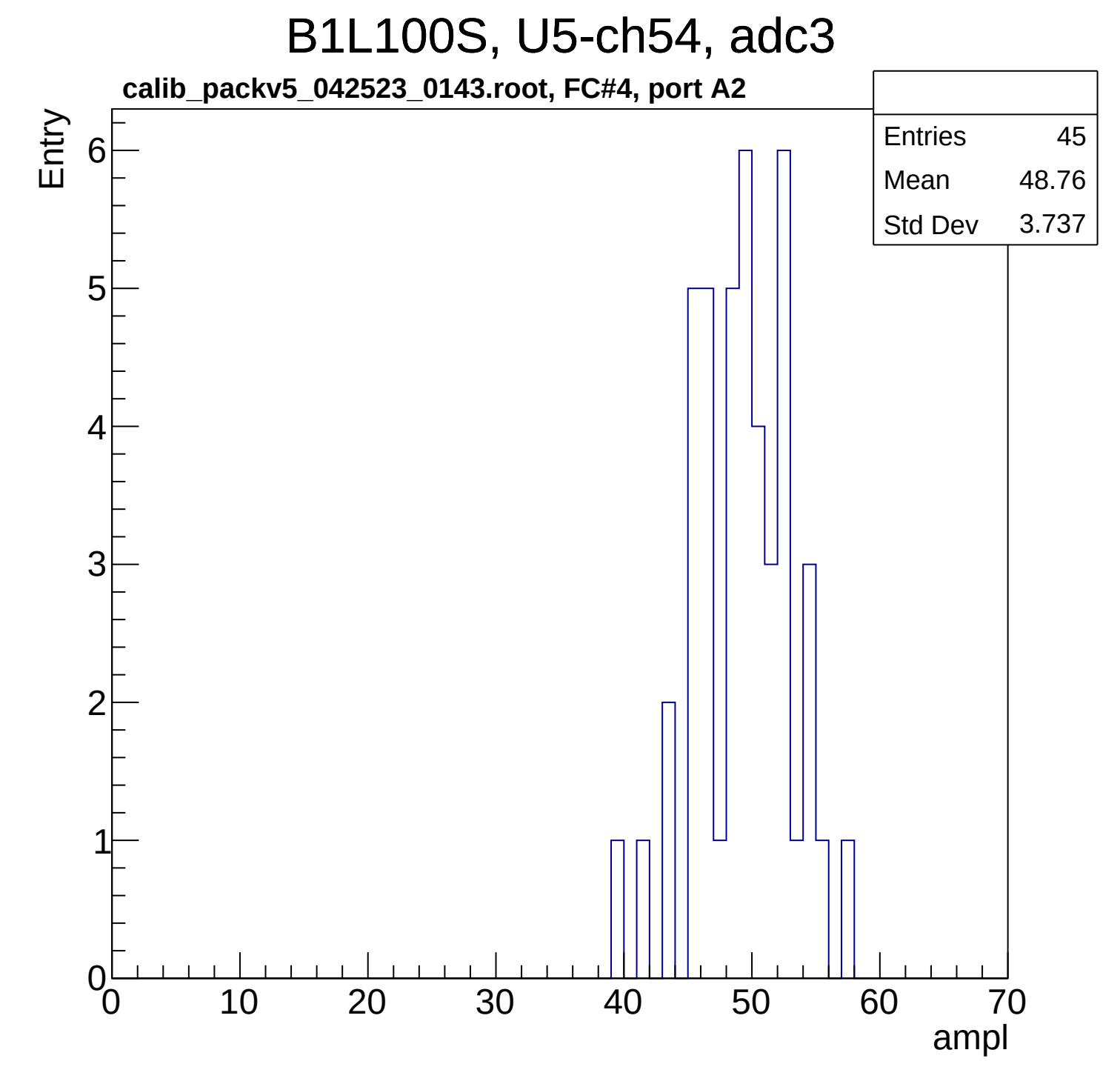
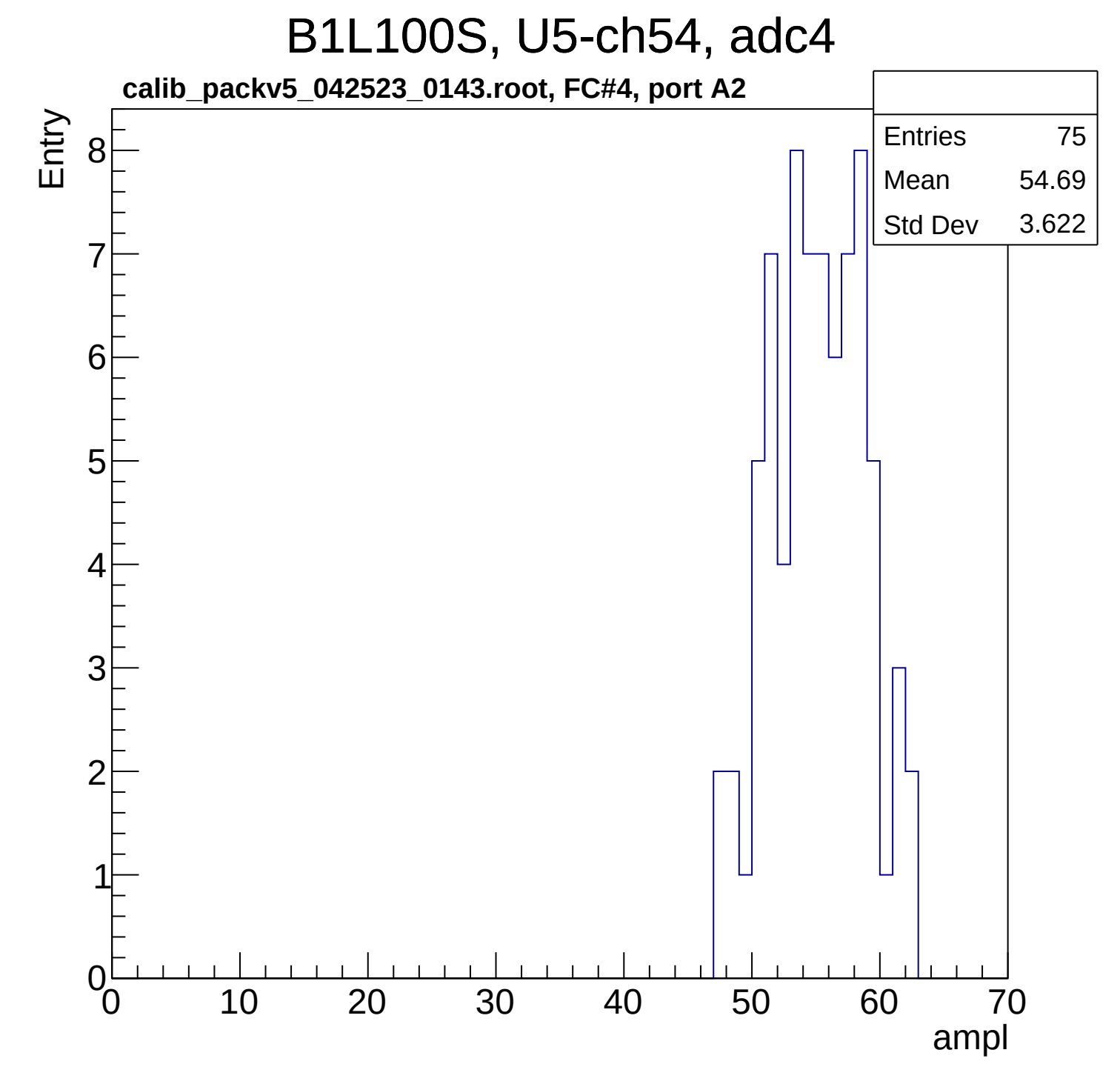
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch54, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 29.65
Std Dev 3.36
Gaus mean : 29.9654
Gaus Width: 3.3794
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch54, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 36.06
Std Dev 3.157
Gaus mean : 36.4457
Gaus Width: 3.3480
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch54, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 43.29
Std Dev 3.248
Gaus mean : 43.5728
Gaus Width: 3.9331
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch54, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 45
Mean 48.76
Std Dev 3.737
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L100S, U5-ch54, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 75
Mean 54.69
Std Dev 3.622
Entry
ampl
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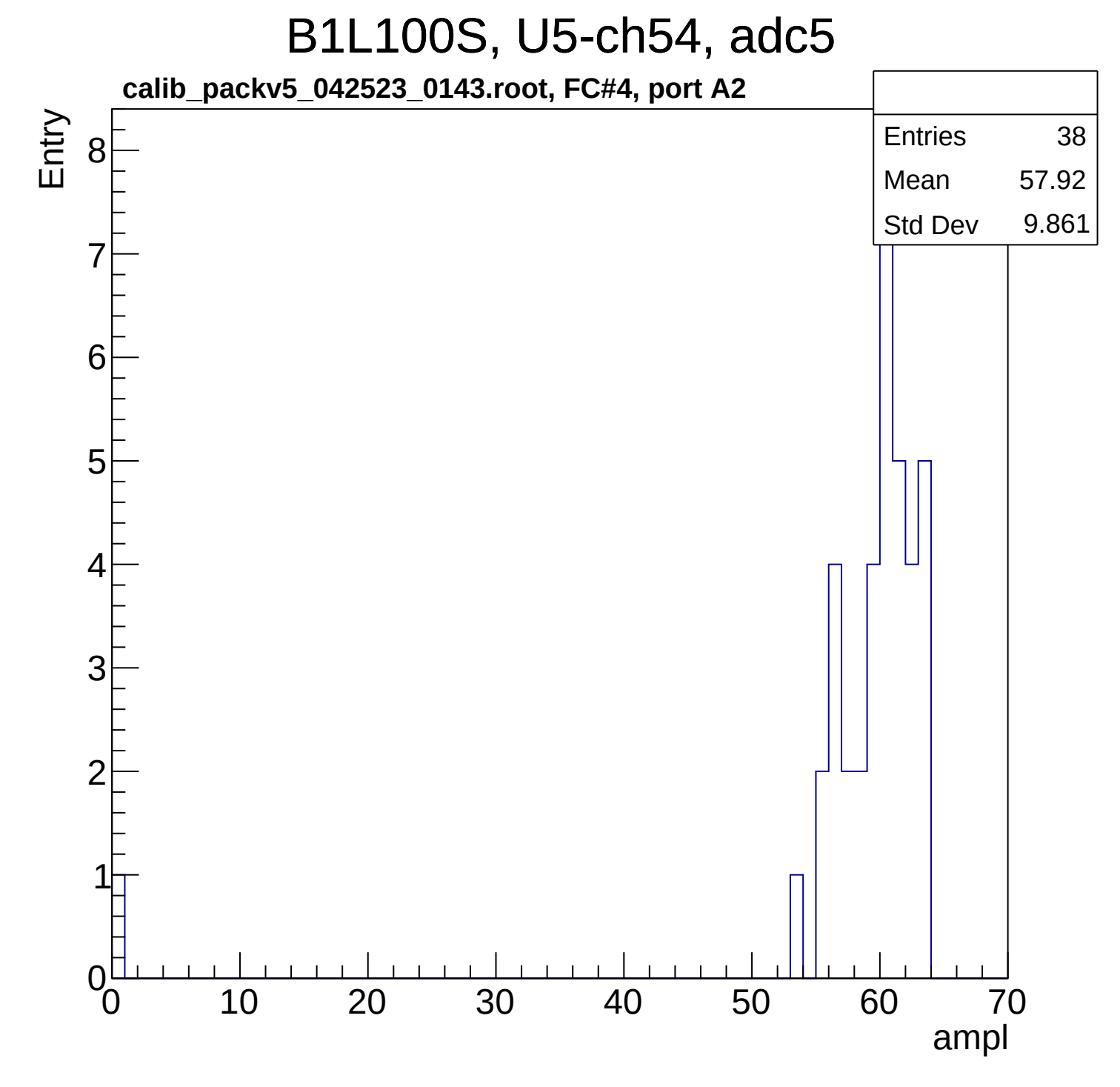
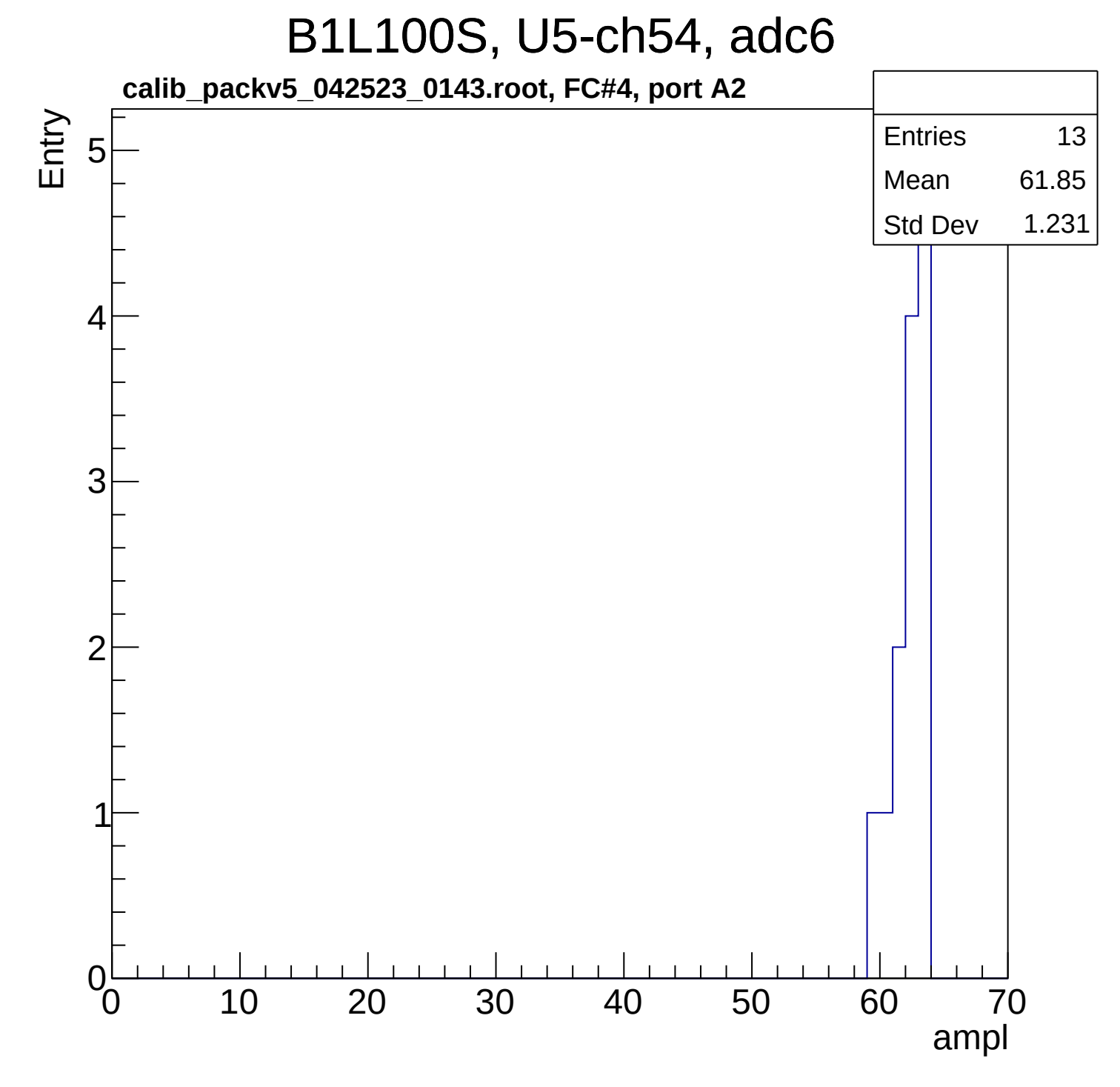
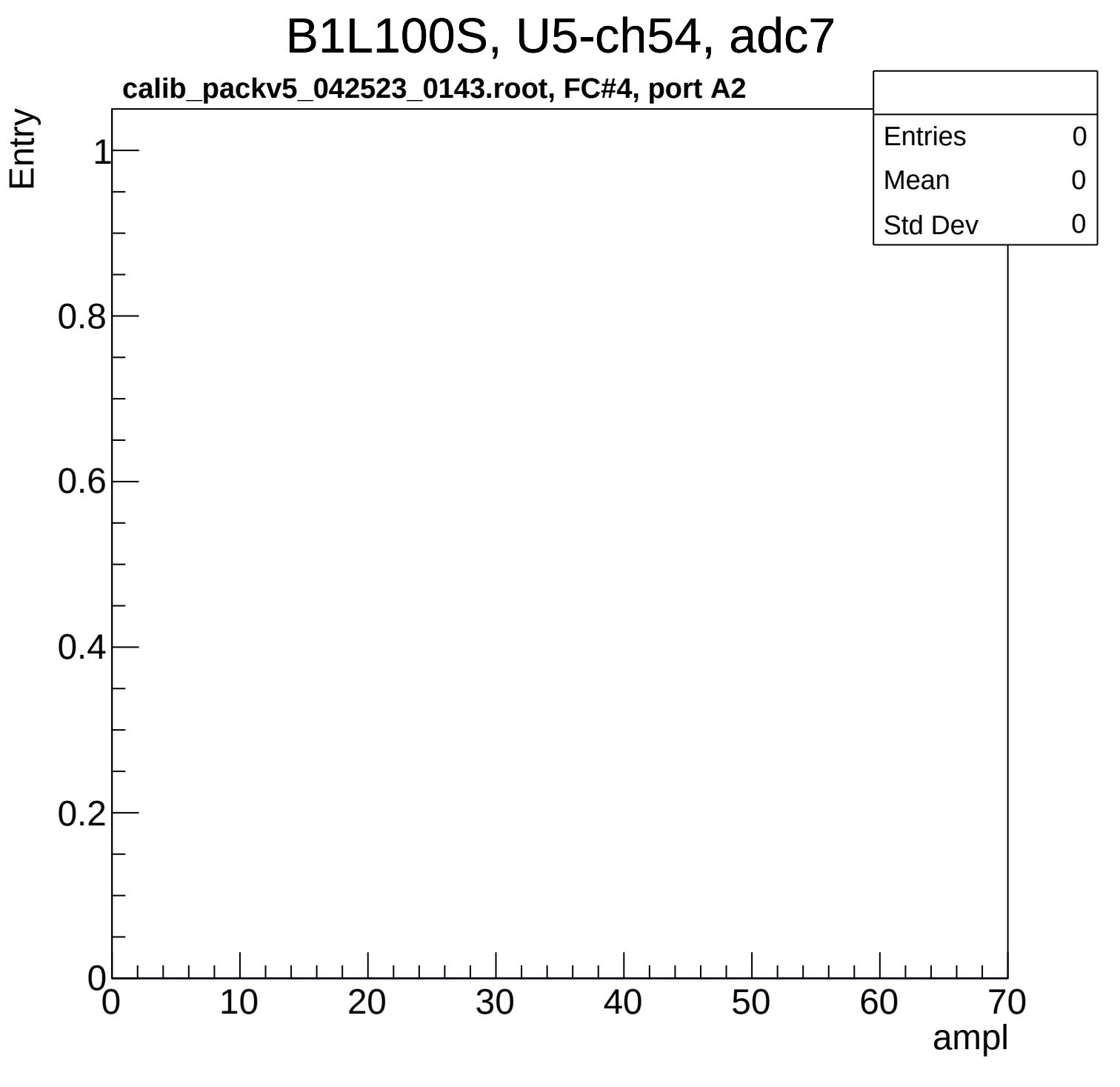
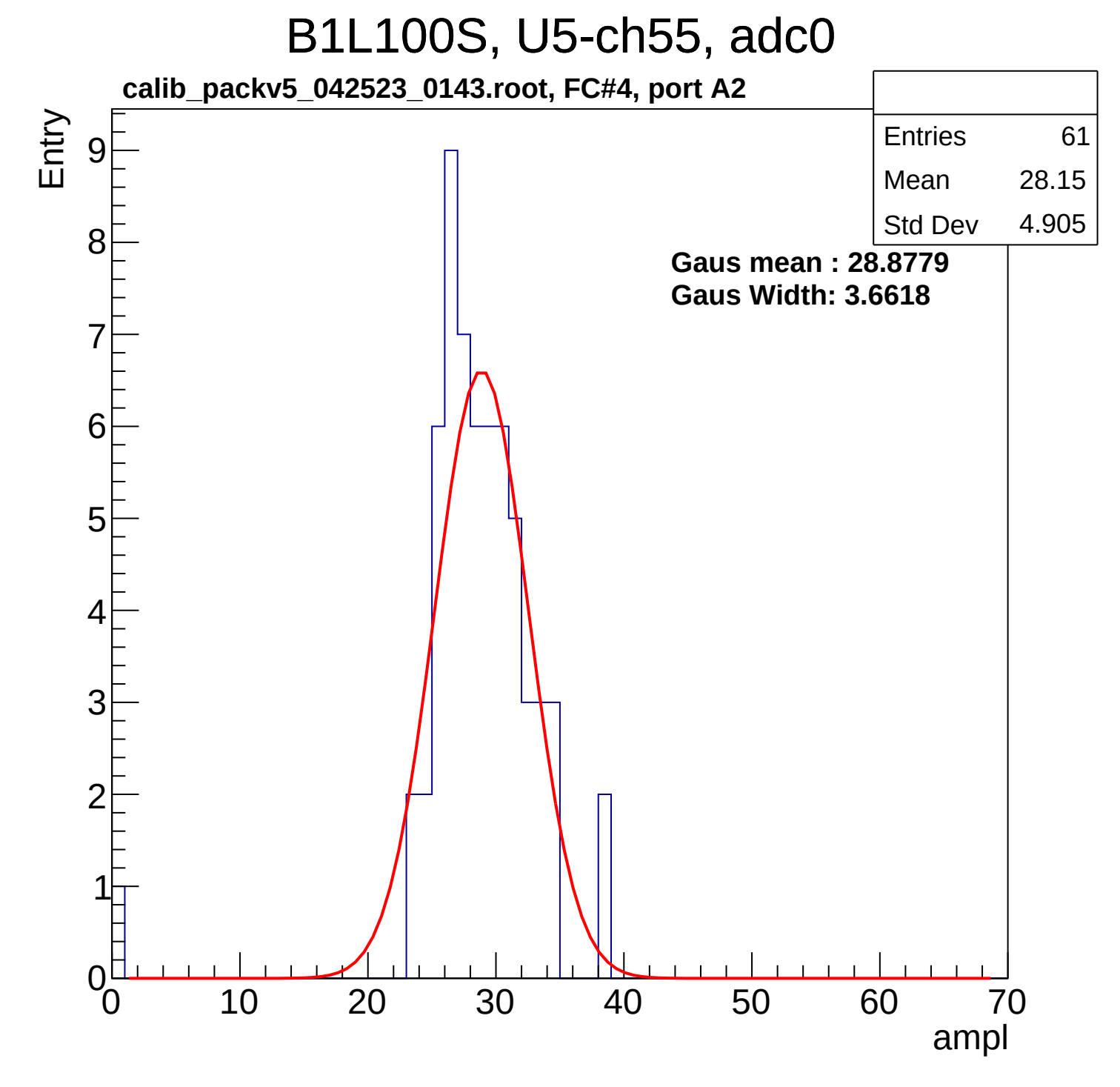
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch54, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 38
Mean 57.92
Std Dev 9.861
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch54, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 13
Mean 61.85
Std Dev 1.231
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch54, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch55, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 28.15
Std Dev 4.905
Gaus mean : 28.8779
Gaus Width: 3.6618
Entry
ampl
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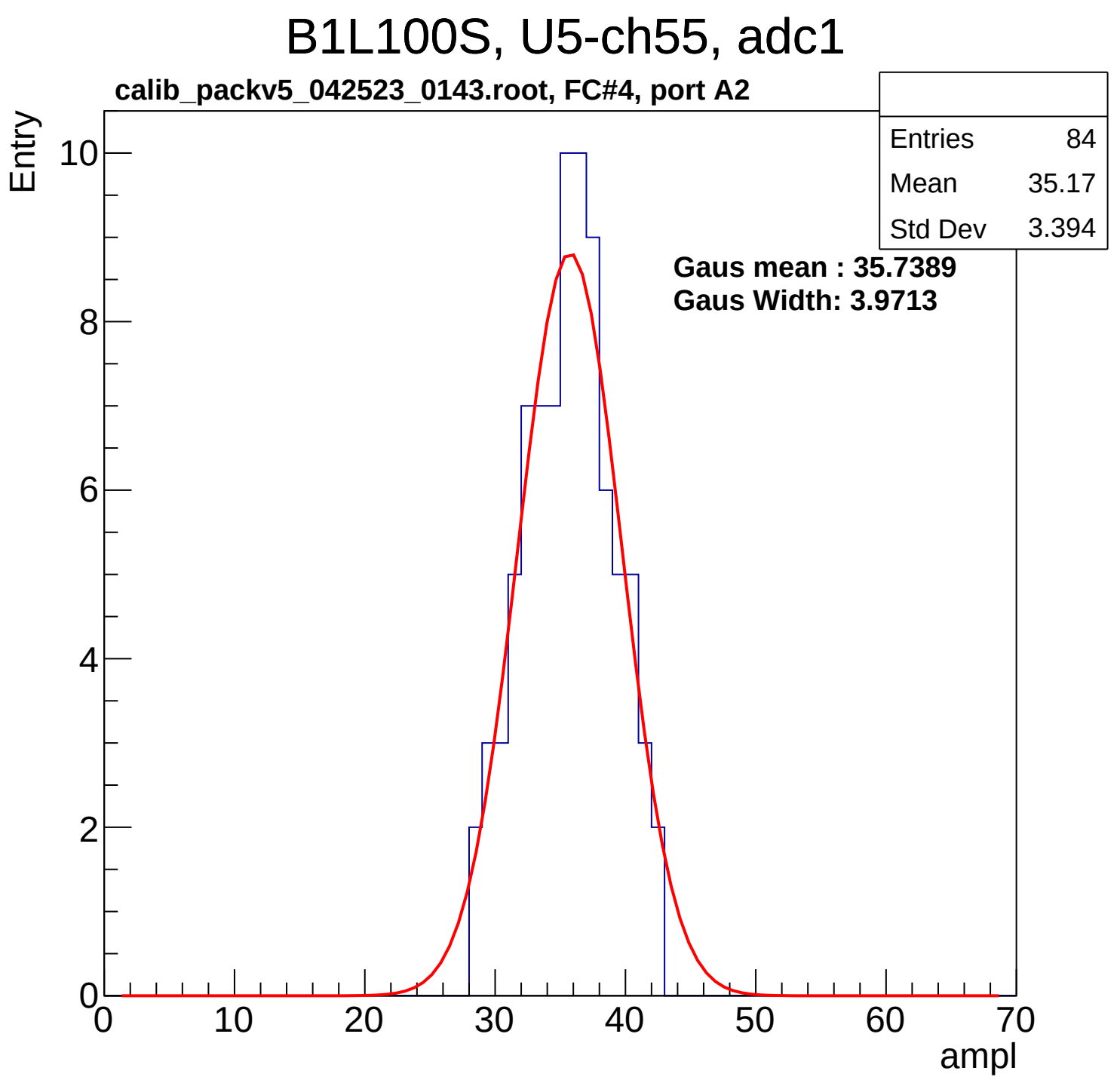
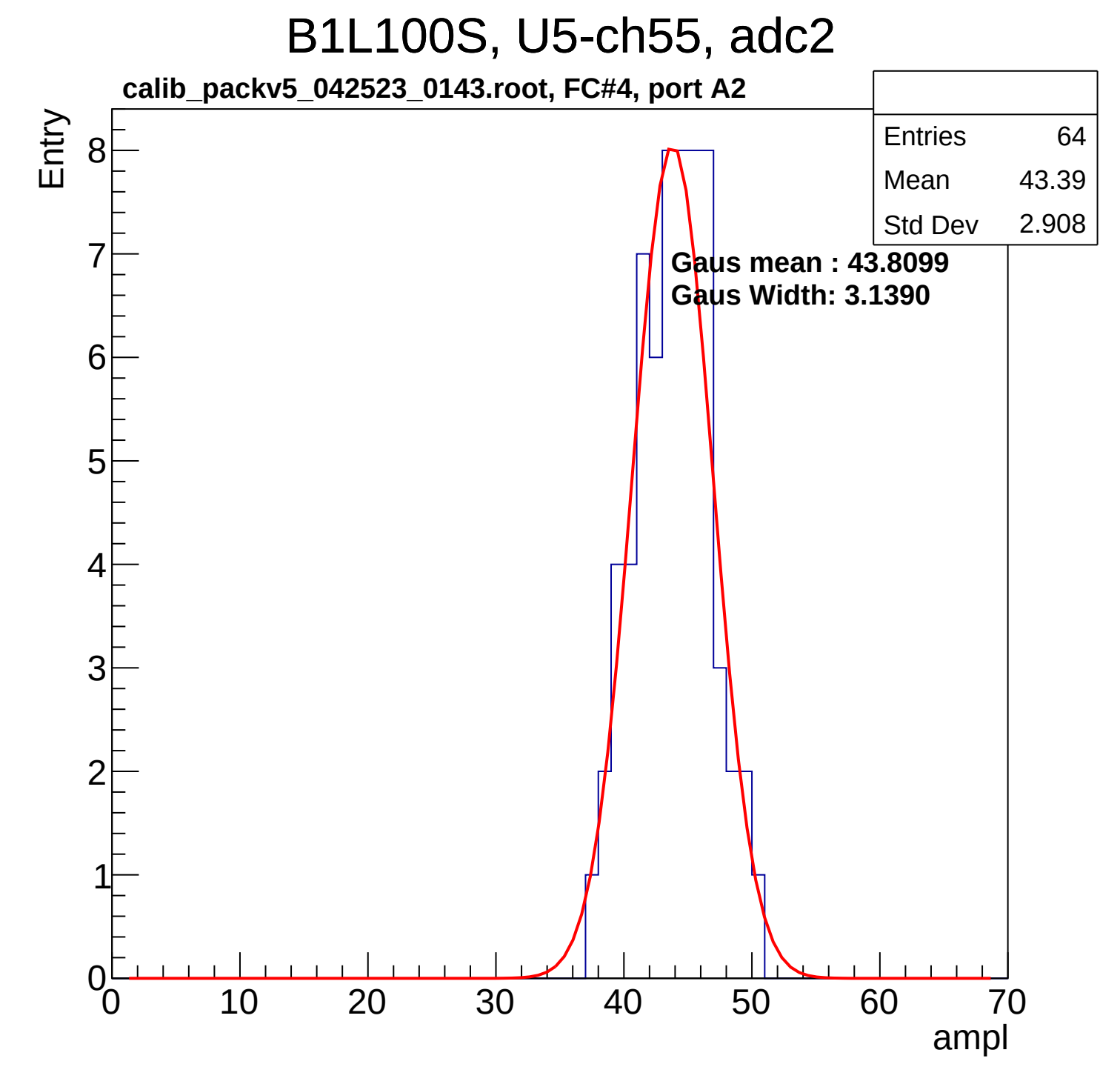
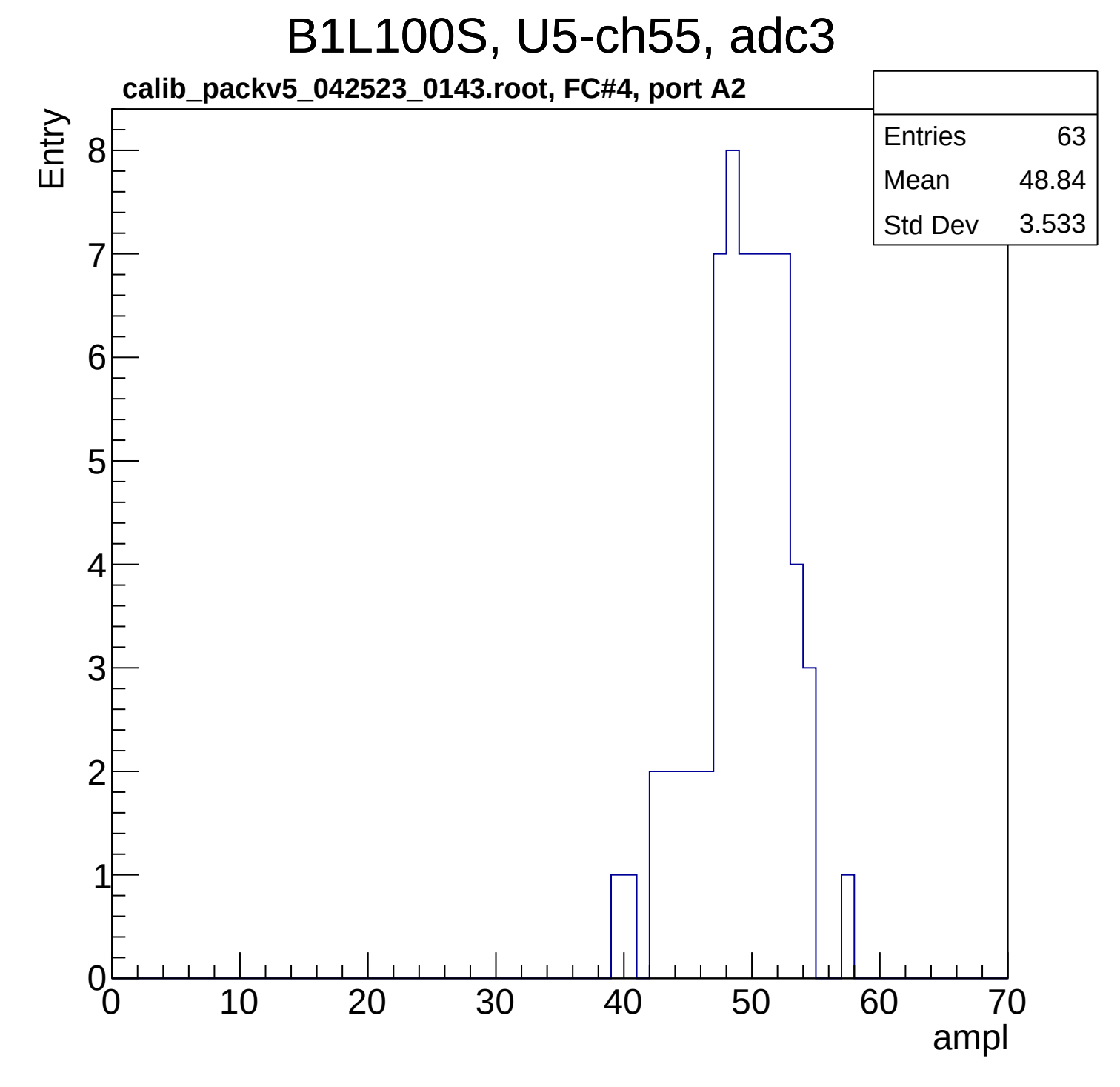
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch55, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 84
Mean 35.17
Std Dev 3.394
Gaus mean : 35.7389
Gaus Width: 3.9713
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch55, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 43.39
Std Dev 2.908
Gaus mean : 43.8099
Gaus Width: 3.1390
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch55, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 48.84
Std Dev 3.533
Entry
ampl
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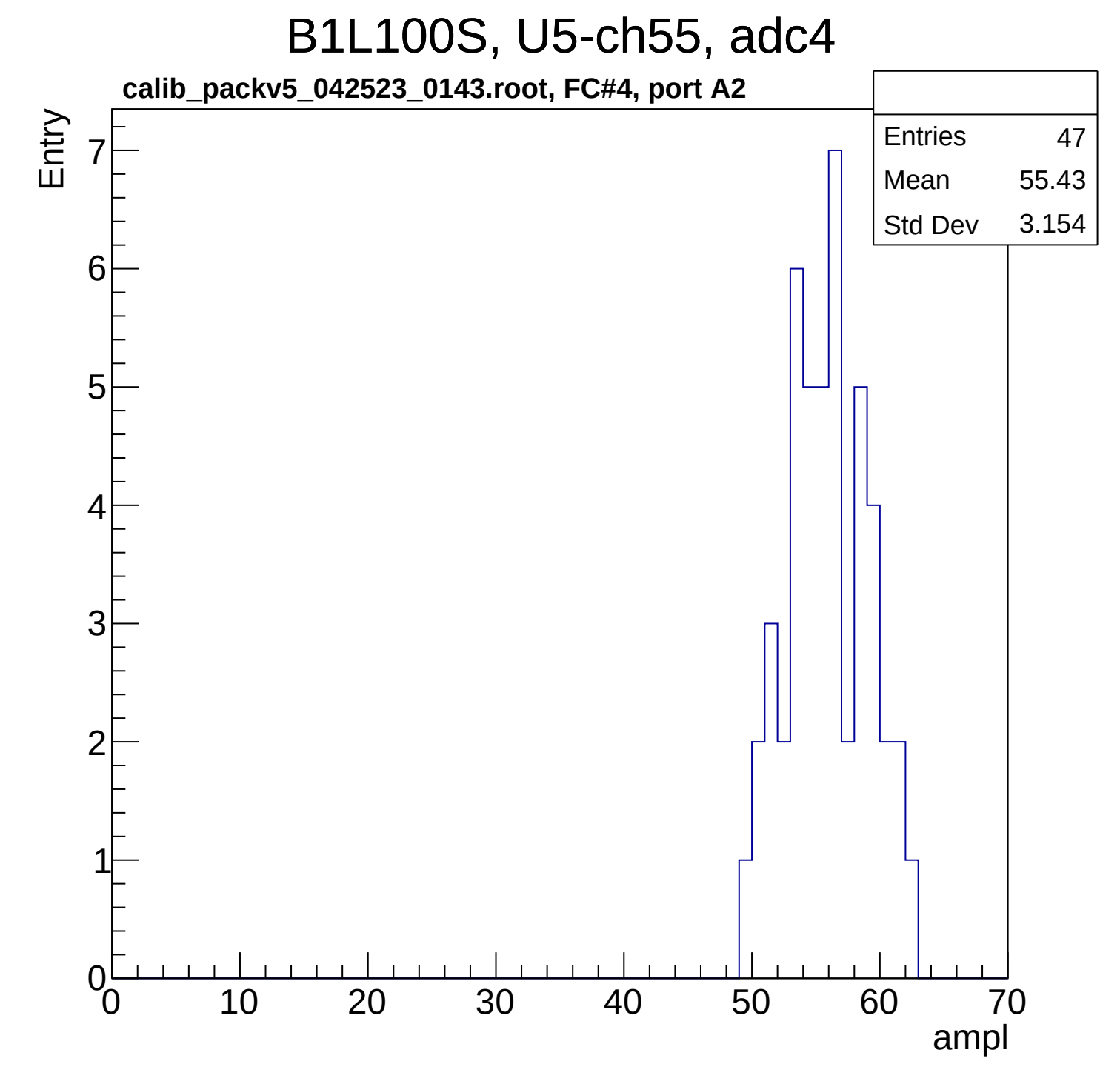
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch55, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 47
Mean 55.43
Std Dev 3.154
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
50
60
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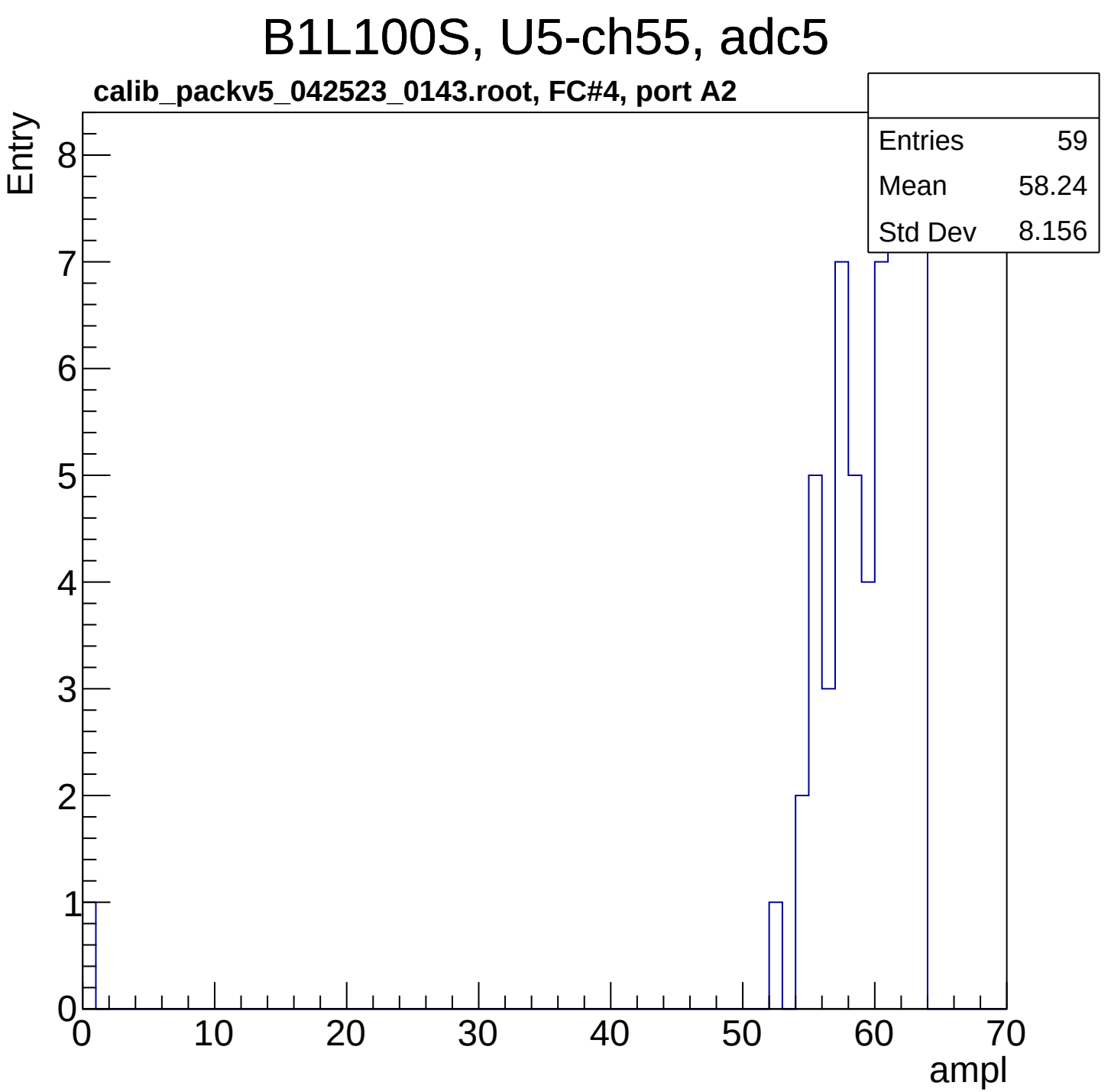
B1L100S, U5-ch55, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 58.24
Std Dev 8.156
Entry
0
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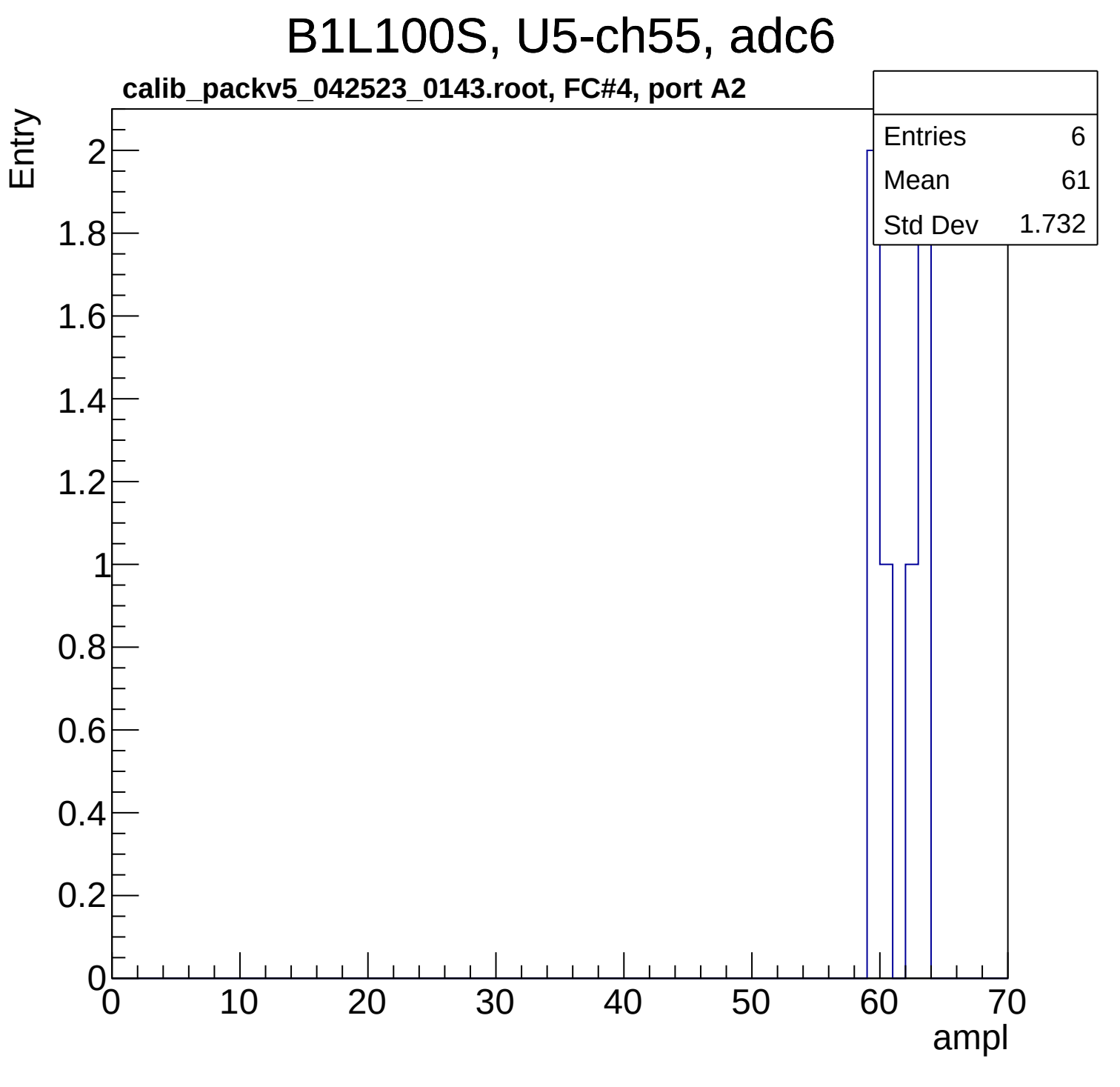
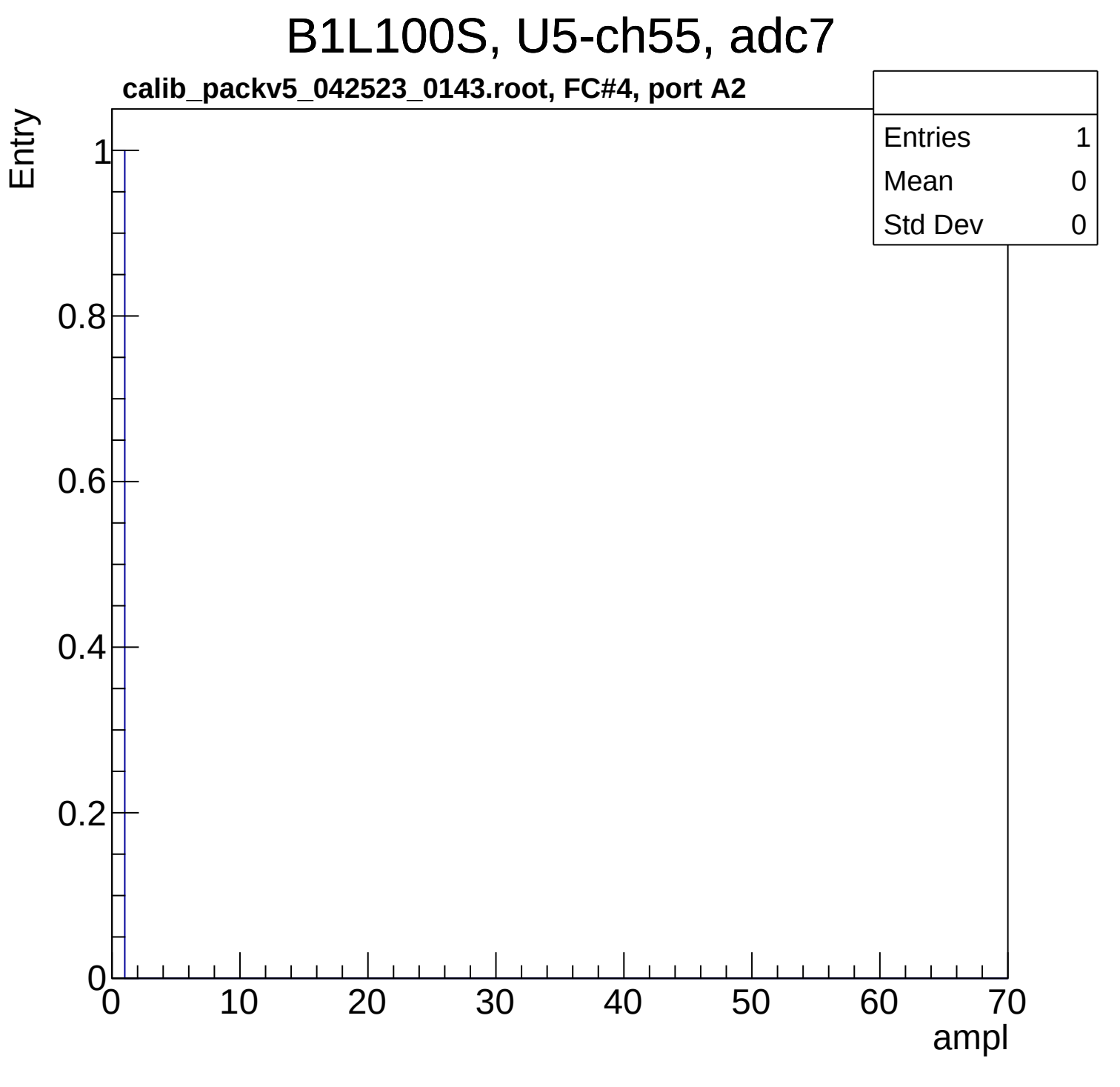
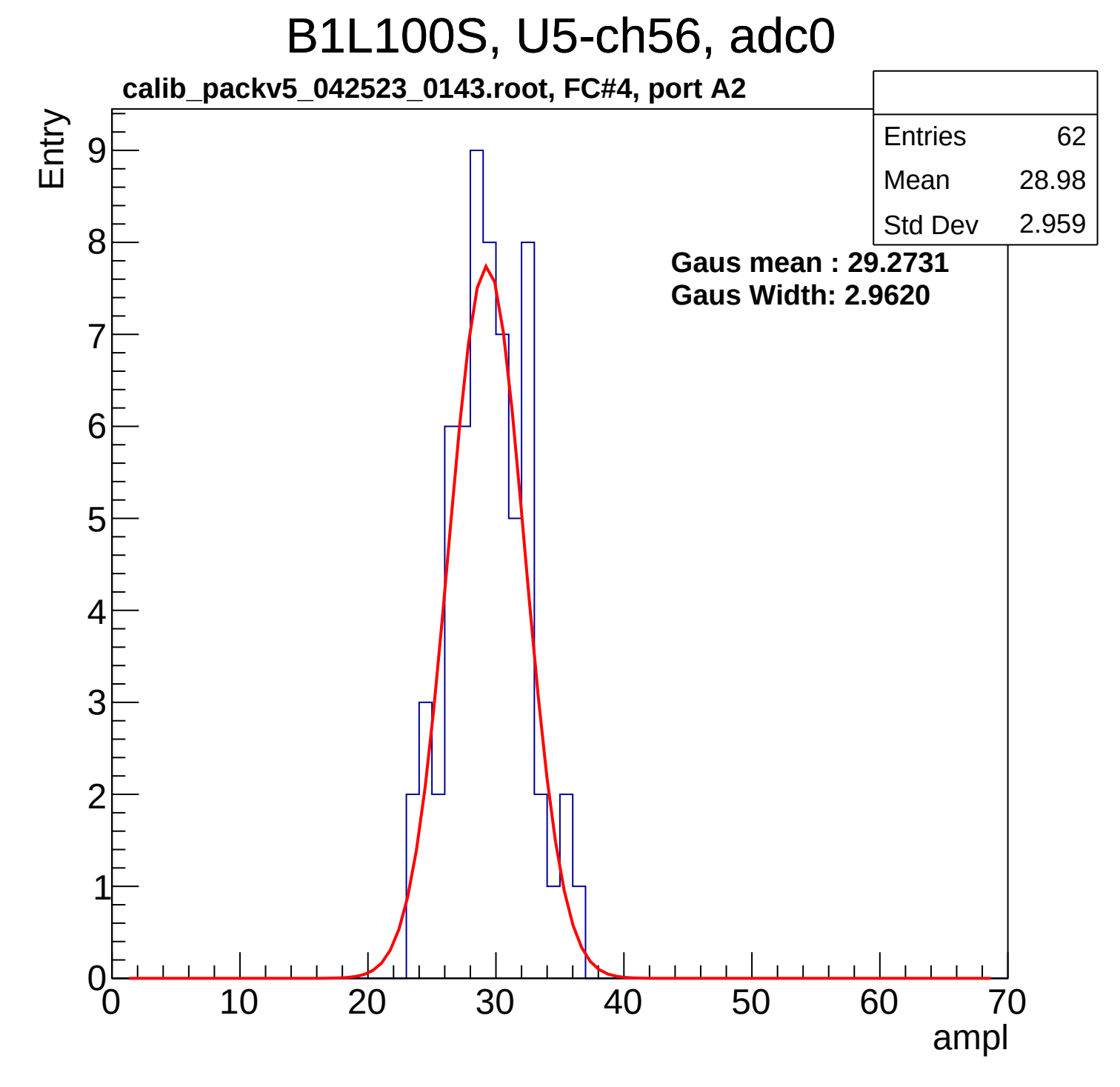
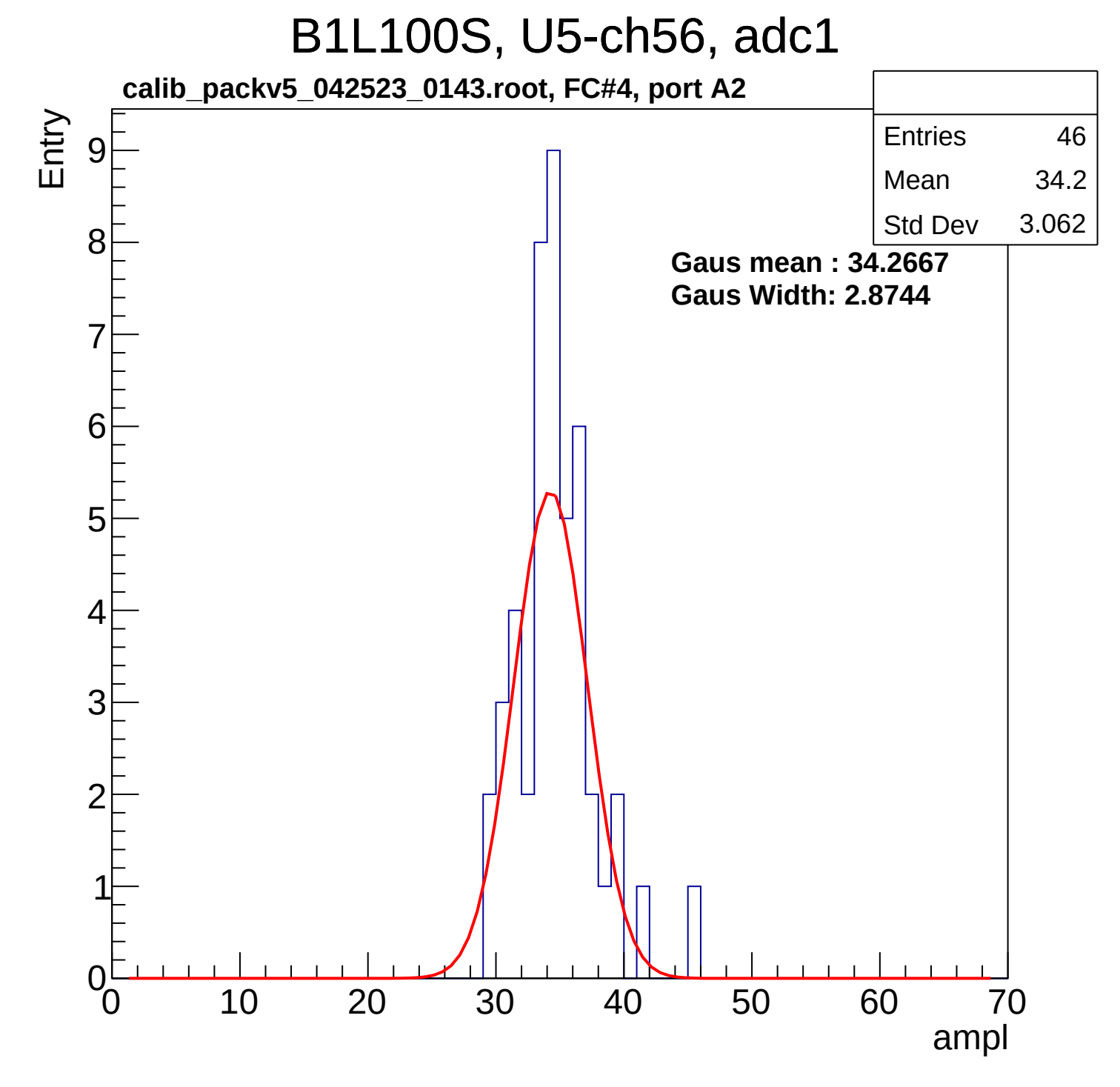
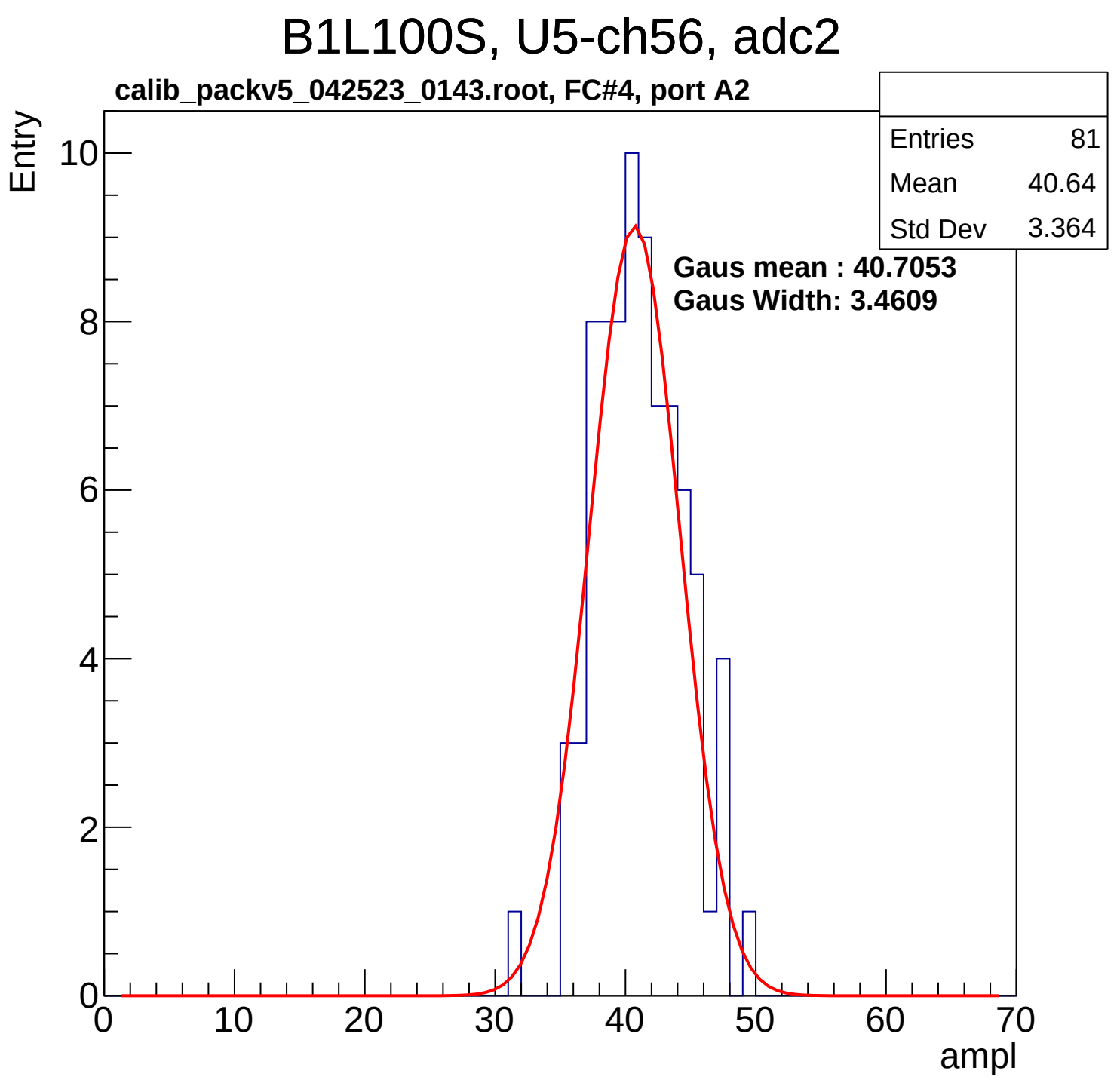
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

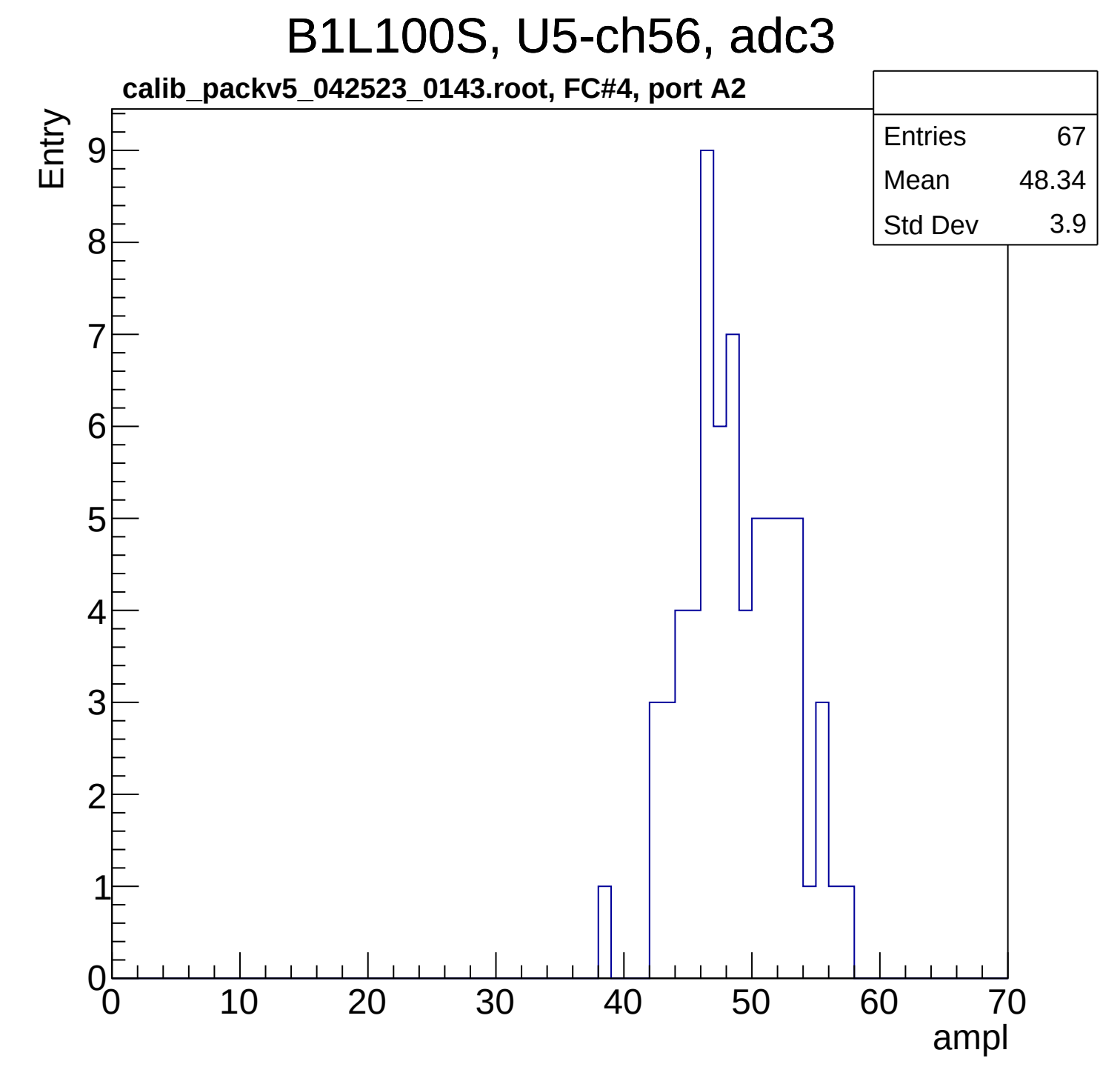

B1L100S, U5-ch55, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 6
Mean 61
Std Dev 1.732
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L100S, U5-ch55, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch56, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 28.98
Std Dev 2.959
Gaus mean : 29.2731
Gaus Width: 2.9620
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch56, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 46
Mean 34.2
Std Dev 3.062
Gaus mean : 34.2667
Gaus Width: 2.8744
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch56, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 81
Mean 40.64
Std Dev 3.364
Gaus mean : 40.7053
Gaus Width: 3.4609
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch56, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 48.34
Std Dev 3.9
Entry
ampl
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2
3
4
5
6
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0
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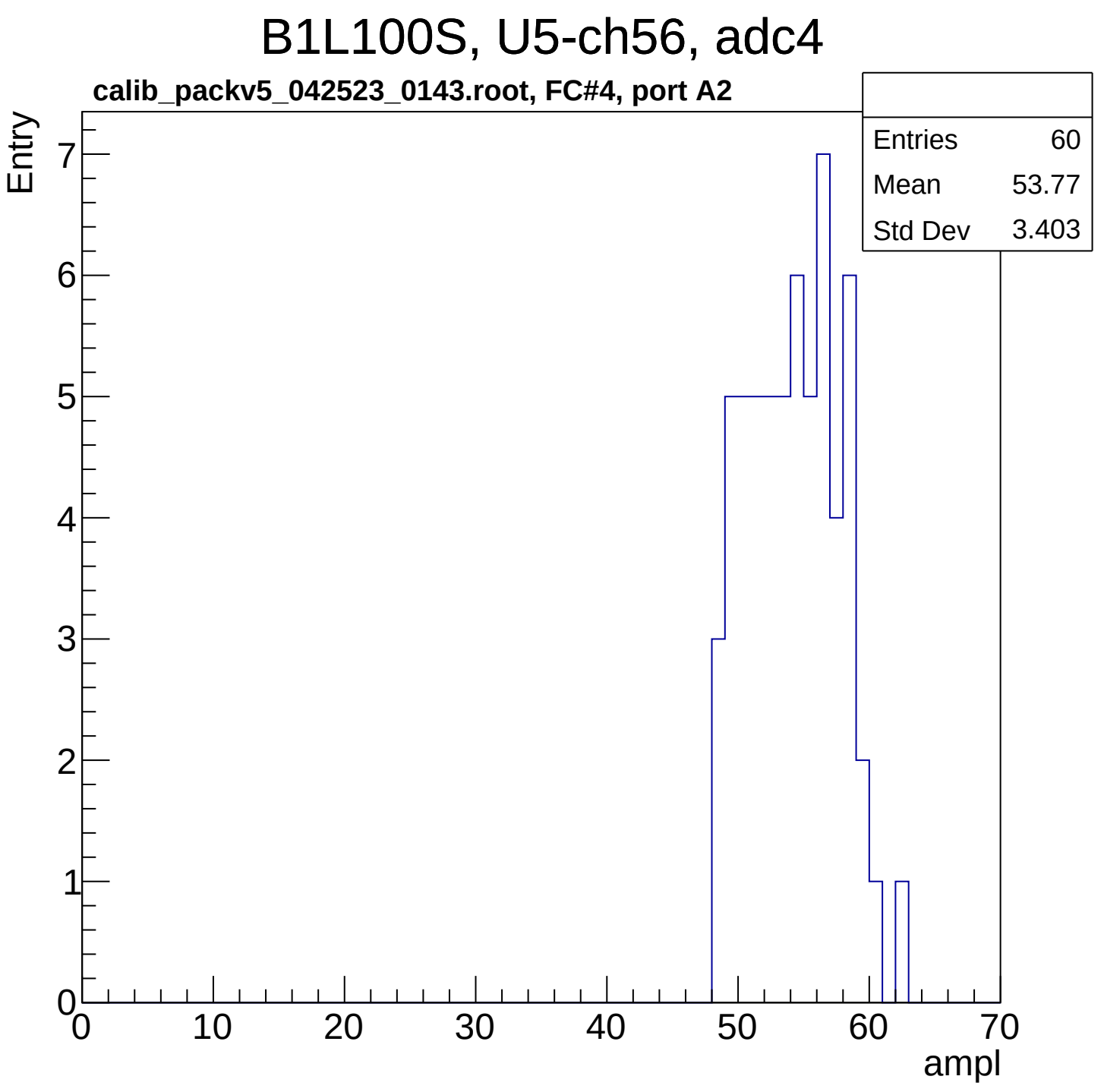
B1L100S, U5-ch56, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 53.77
Std Dev 3.403
Entry
ampl
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4
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6
7
0
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40
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60
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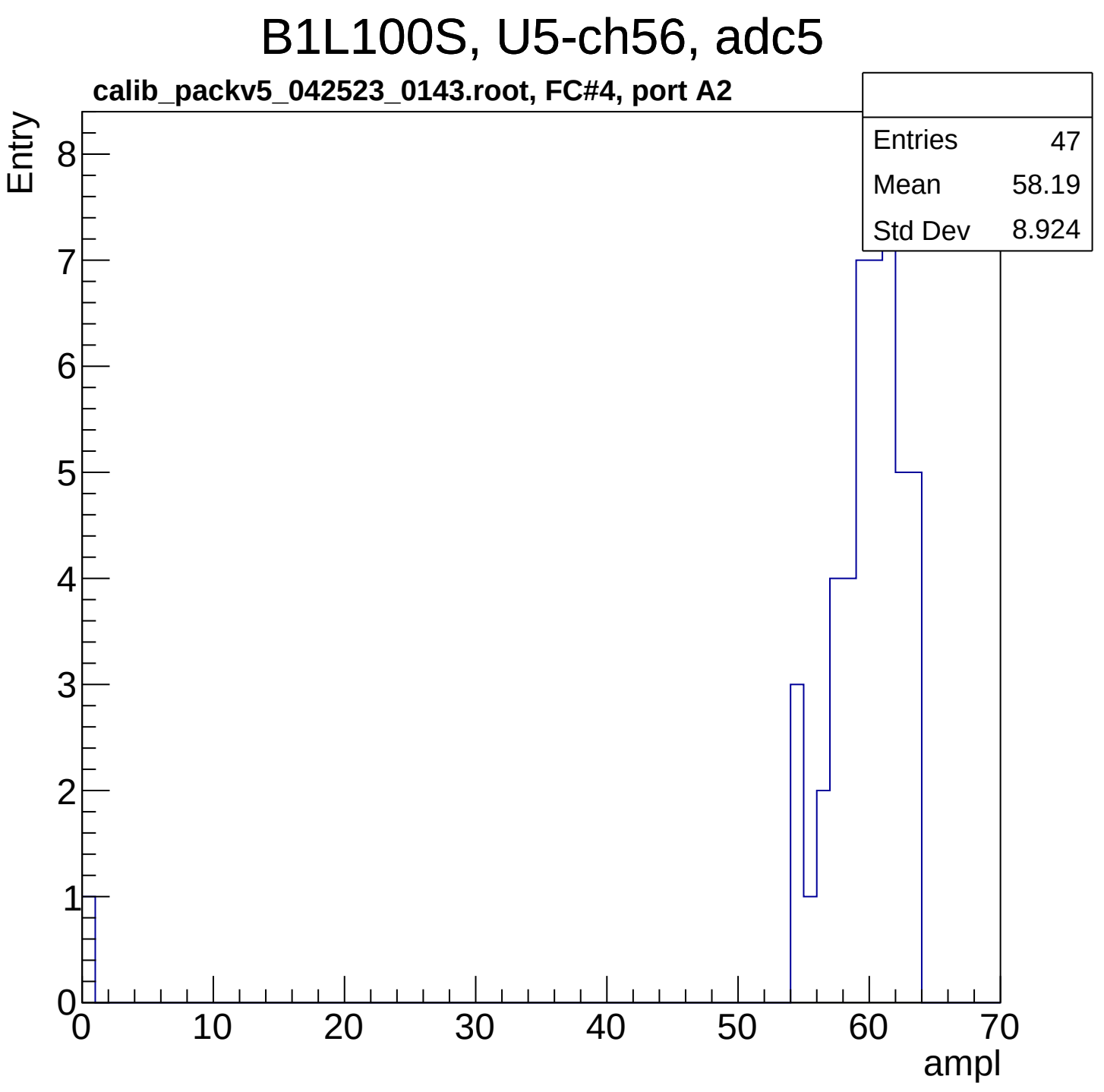
B1L100S, U5-ch56, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 47
Mean 58.19
Std Dev 8.924
Entry
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2
3
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8
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10
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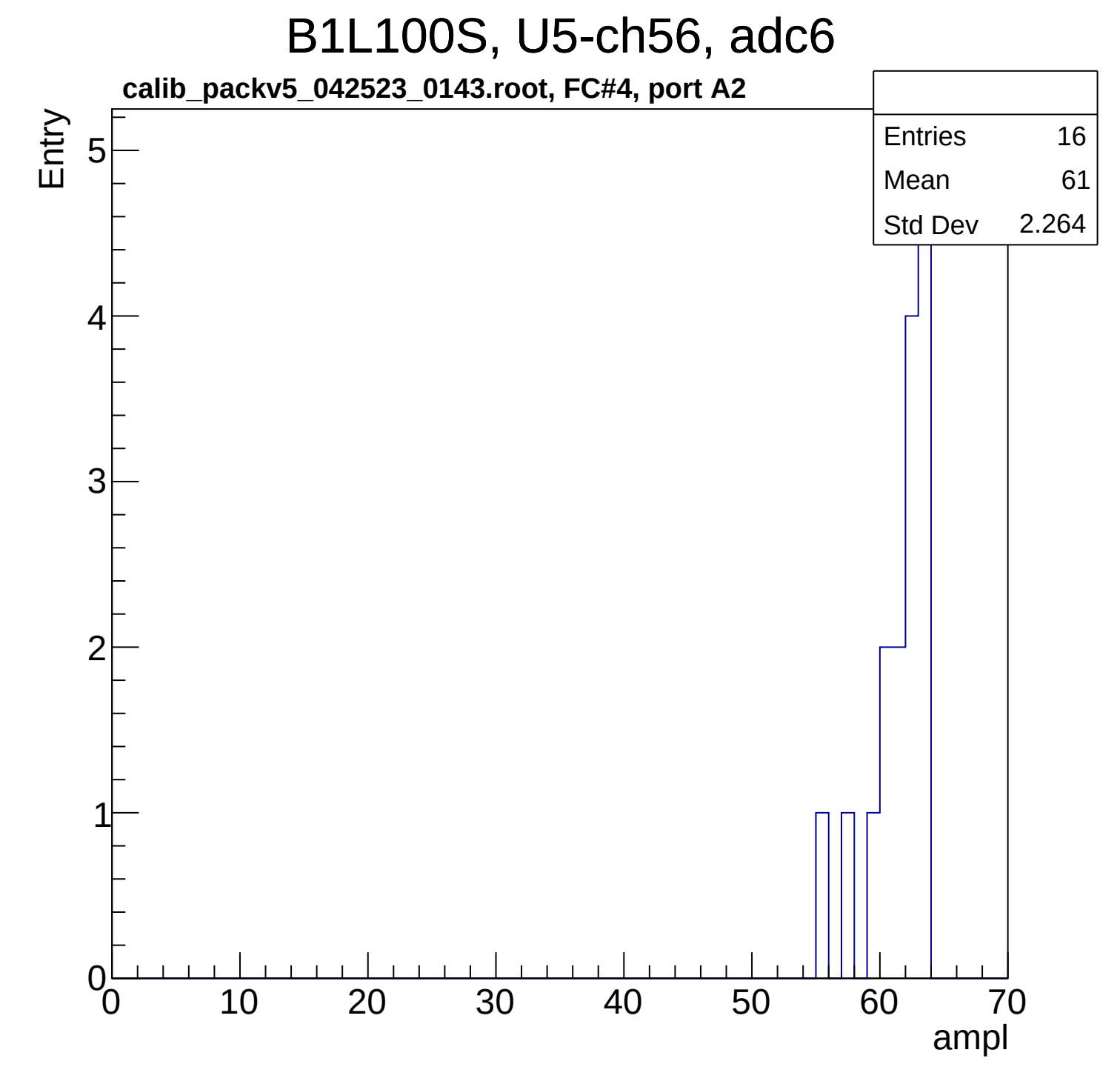
30
40
50
60
70
ampl


B1L100S, U5-ch56, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 16
Mean 61
Std Dev 2.264
Entry
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2
3
4
5
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10
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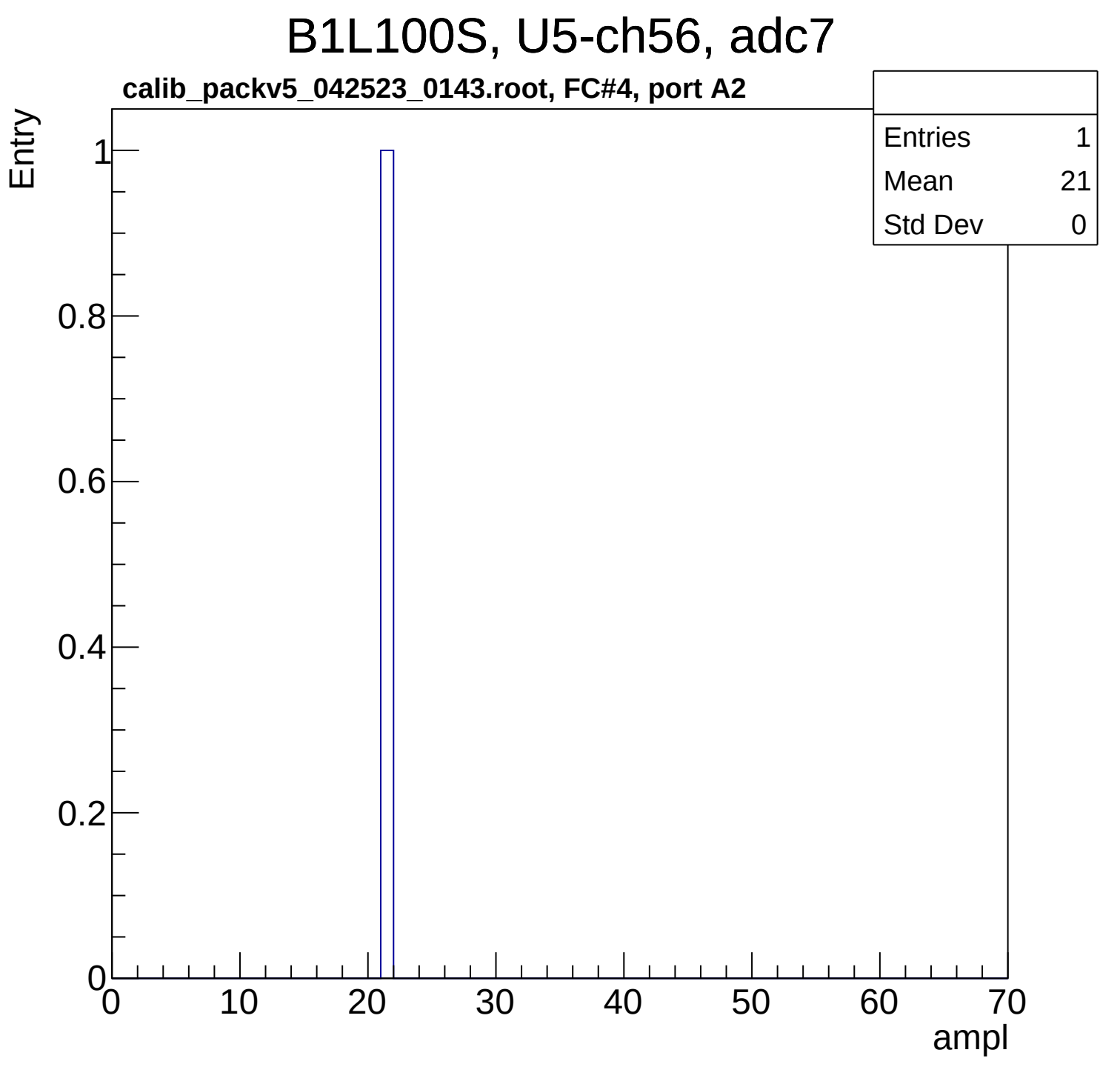
50
60
70
ampl


B1L100S, U5-ch56, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 21
Std Dev 0
Entry
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0.8
0.6
0.4
0.2
0
0
10
20
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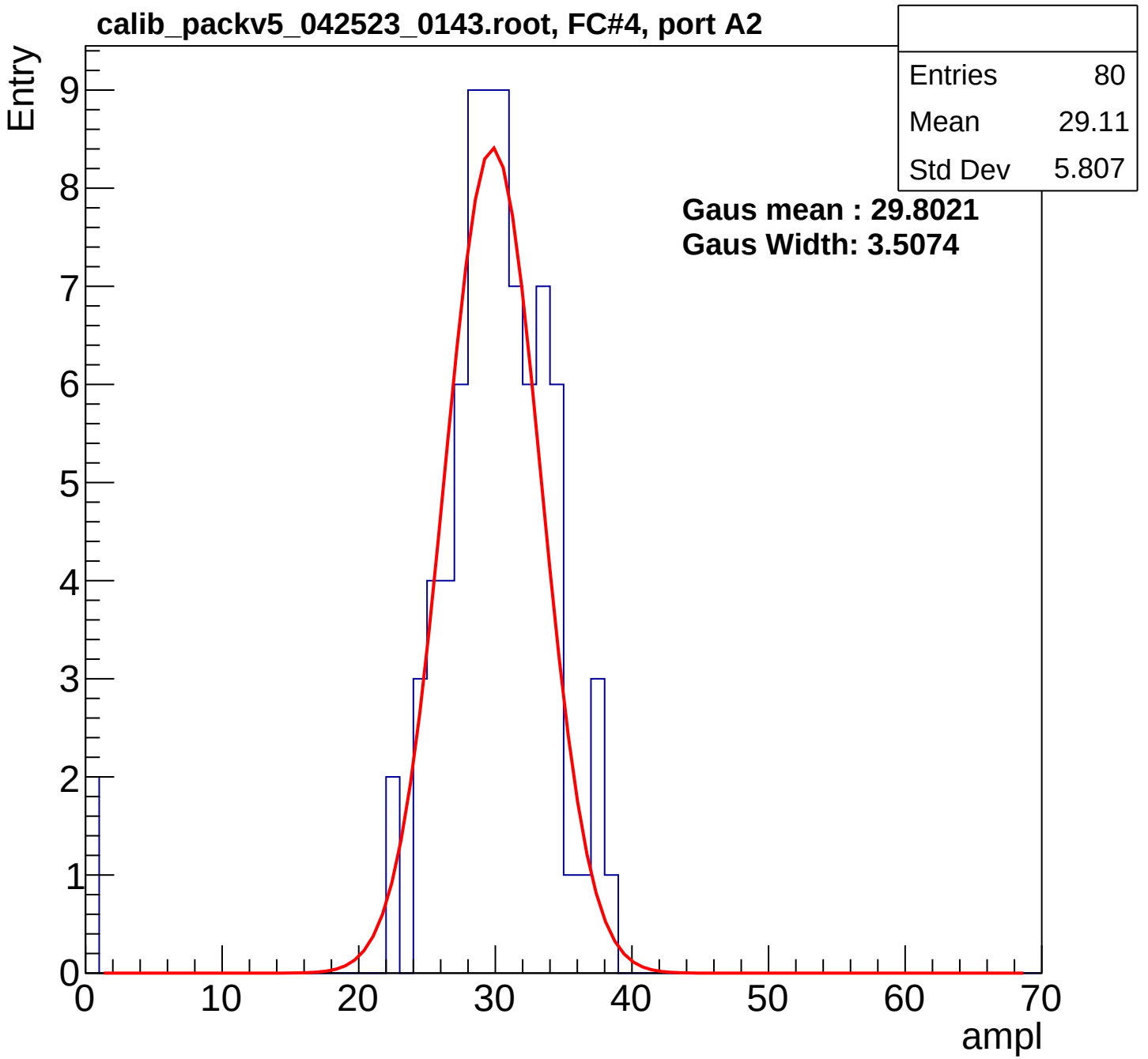
40
50
60
70
ampl


B1L100S, U5-ch57, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 80
Mean 29.11
Std Dev 5.807
Gaus mean : 29.8021
Gaus Width: 3.5074
Entry
ampl
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2
3
4
5
6
7
8
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0
10
20
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40
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60
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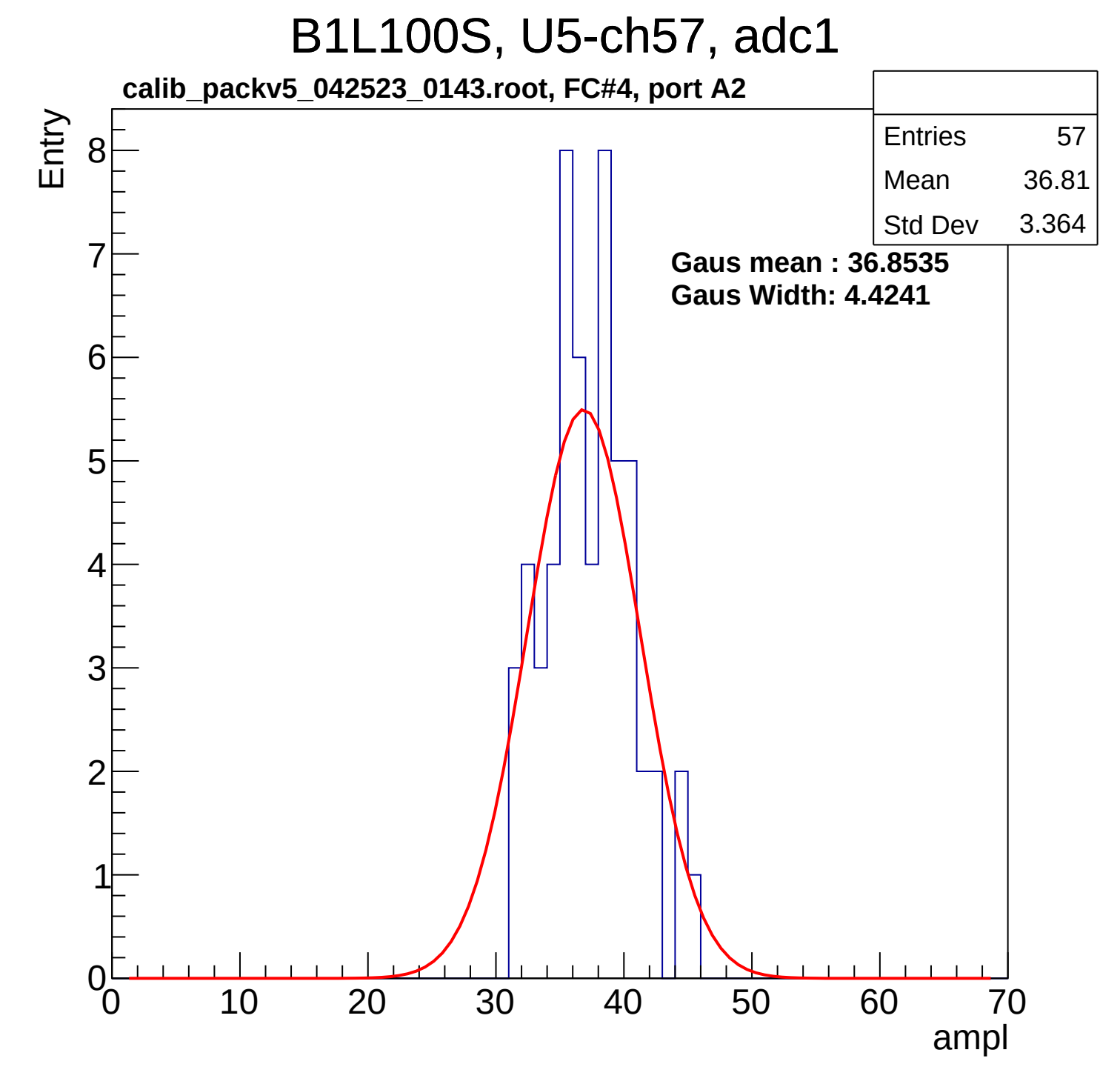
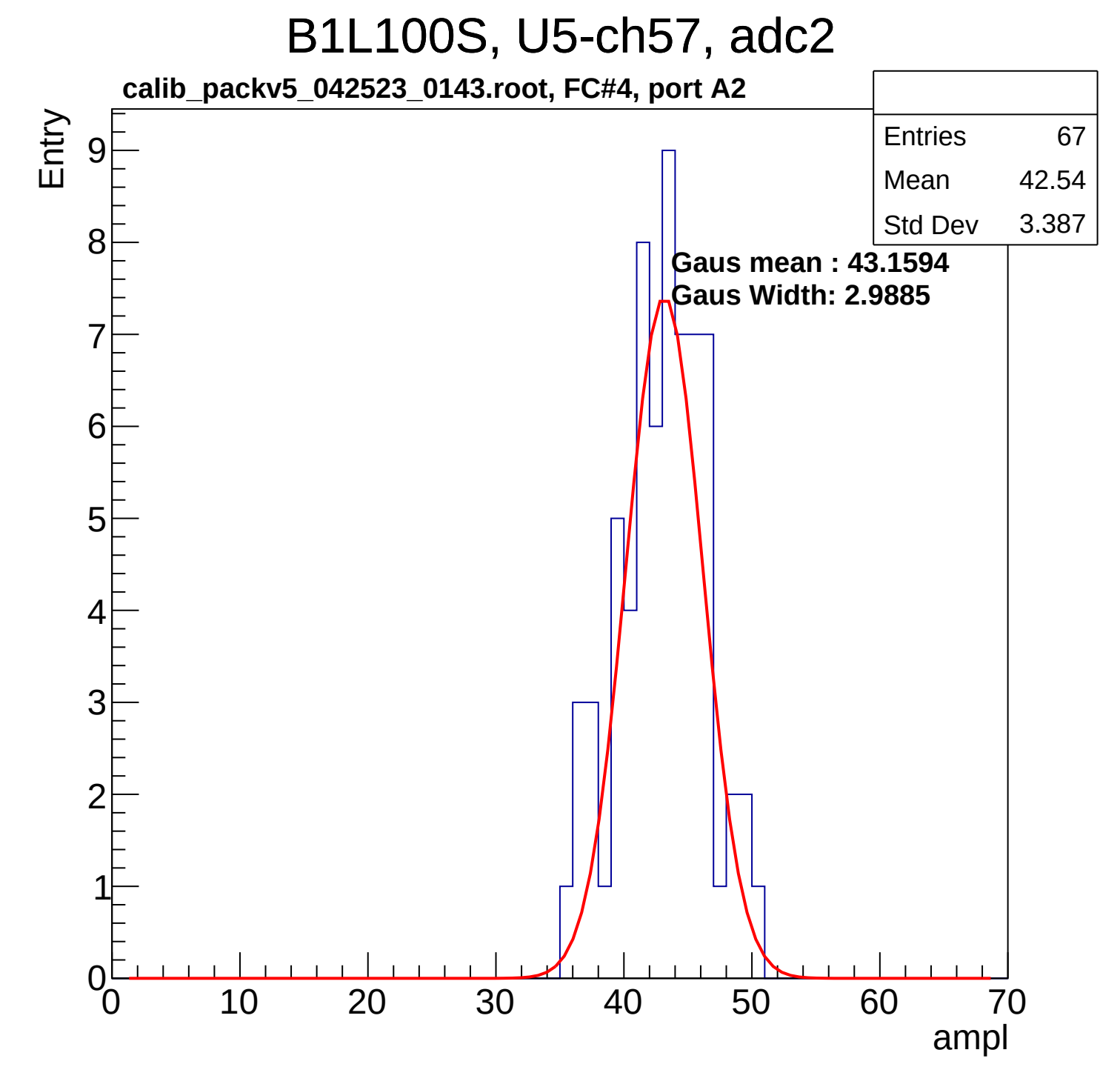

B1L100S, U5-ch57, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 36.81
Std Dev 3.364
Gaus mean : 36.8535
Gaus Width: 4.4241
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch57, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 42.54
Std Dev 3.387
Gaus mean : 43.1594
Gaus Width: 2.9885
Entry
ampl
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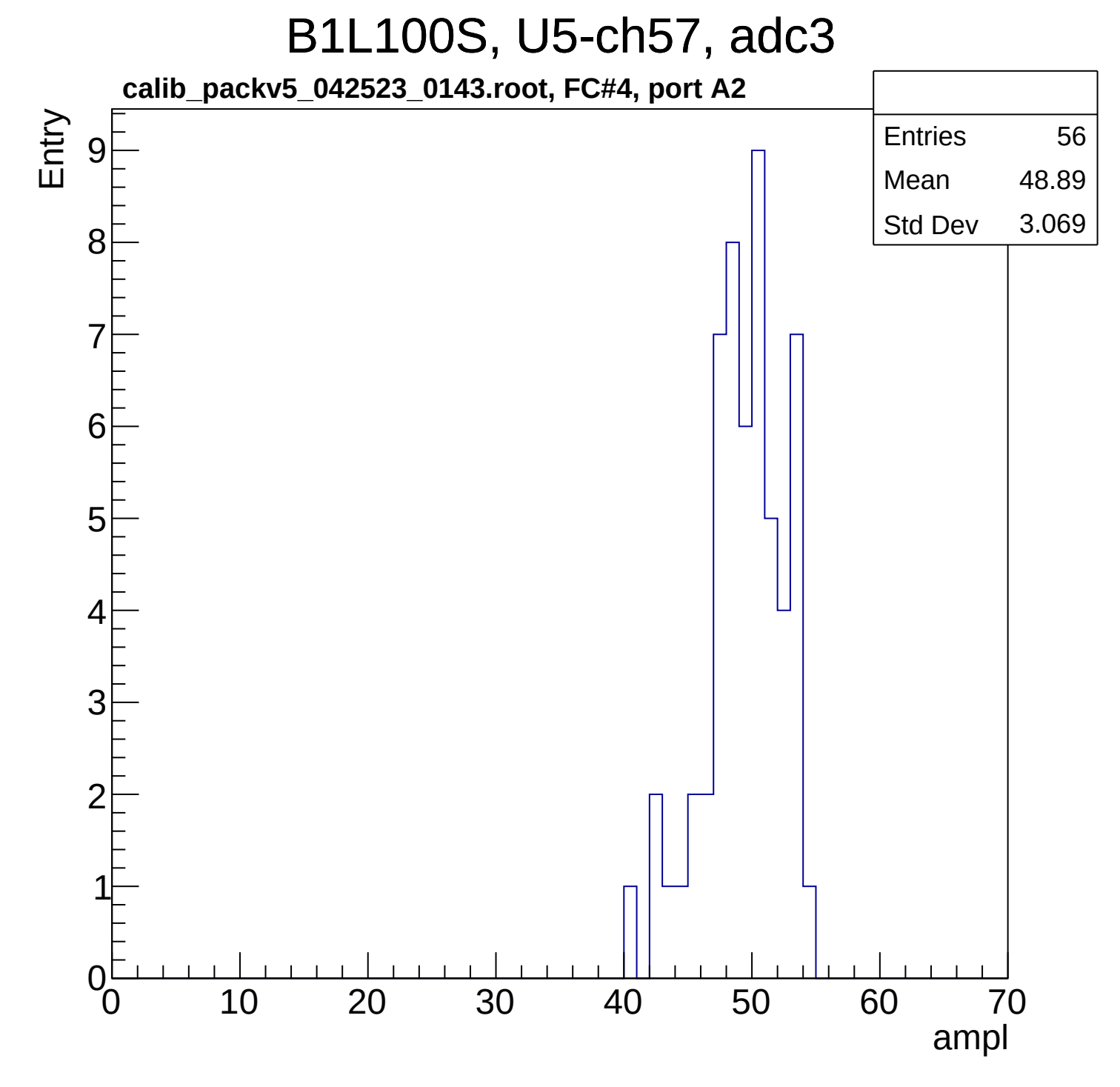
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch57, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 48.89
Std Dev 3.069
Entry
ampl
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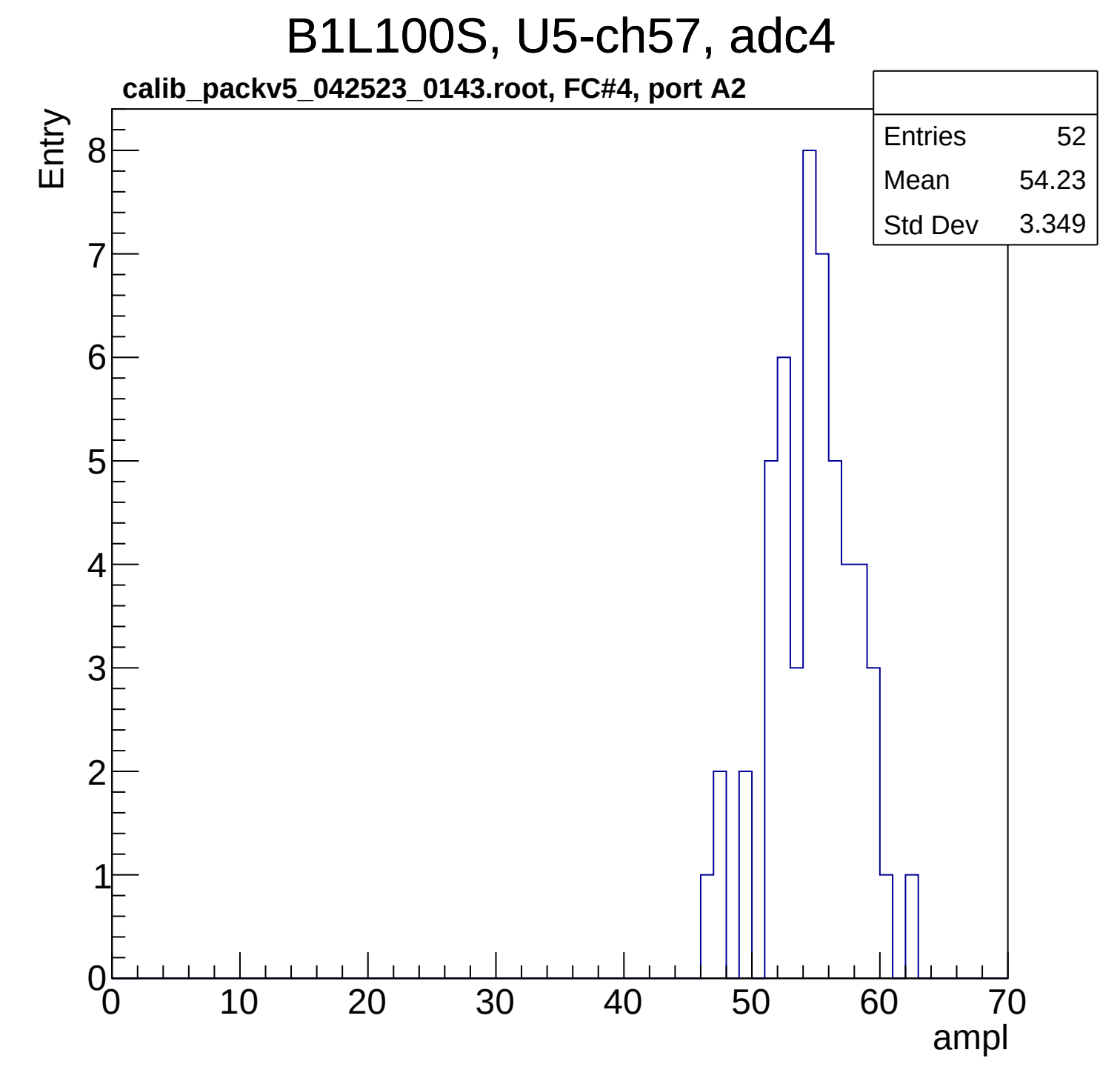
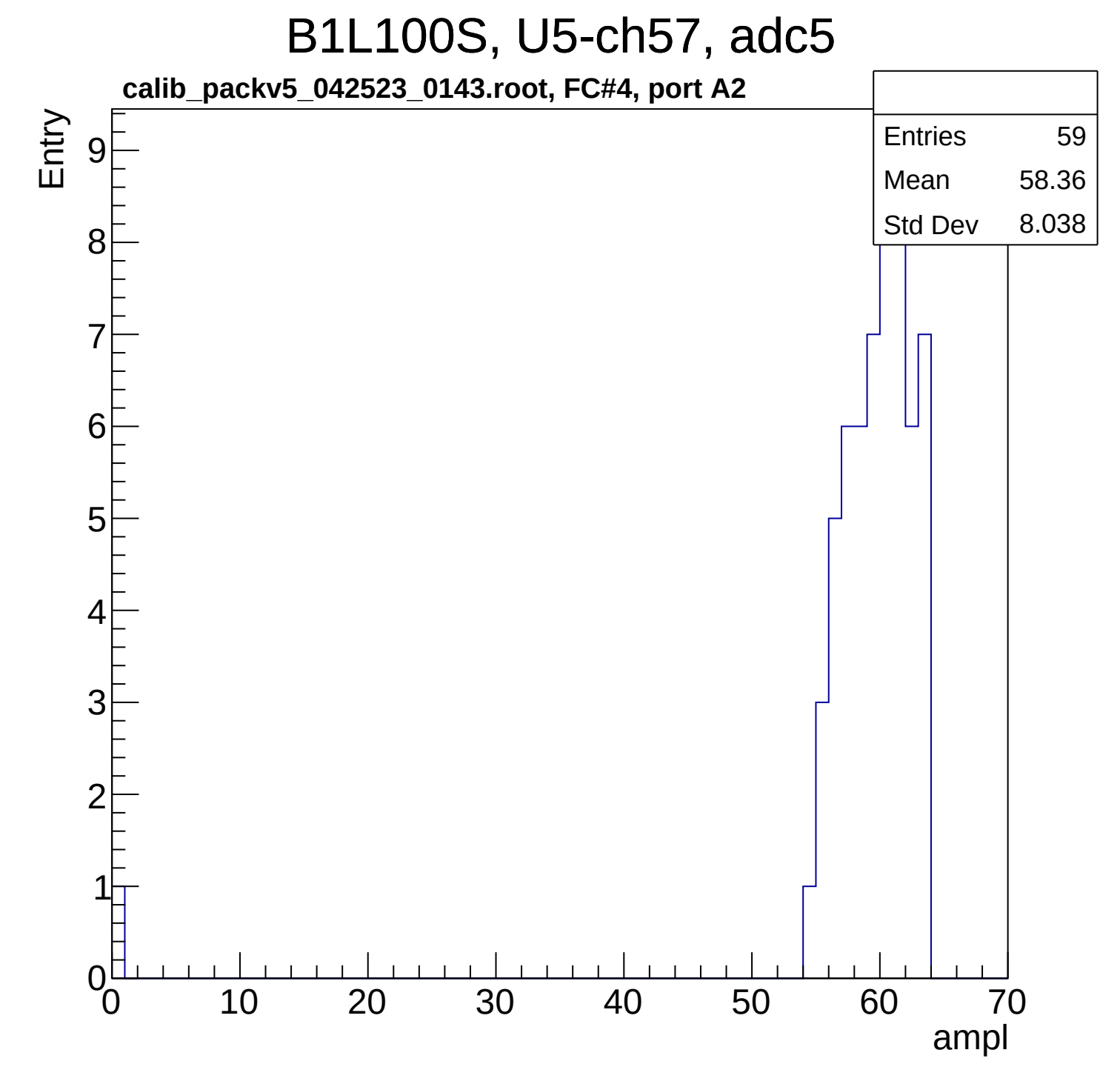
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch57, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 52
Mean 54.23
Std Dev 3.349
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch57, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 58.36
Std Dev 8.038
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
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40
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60
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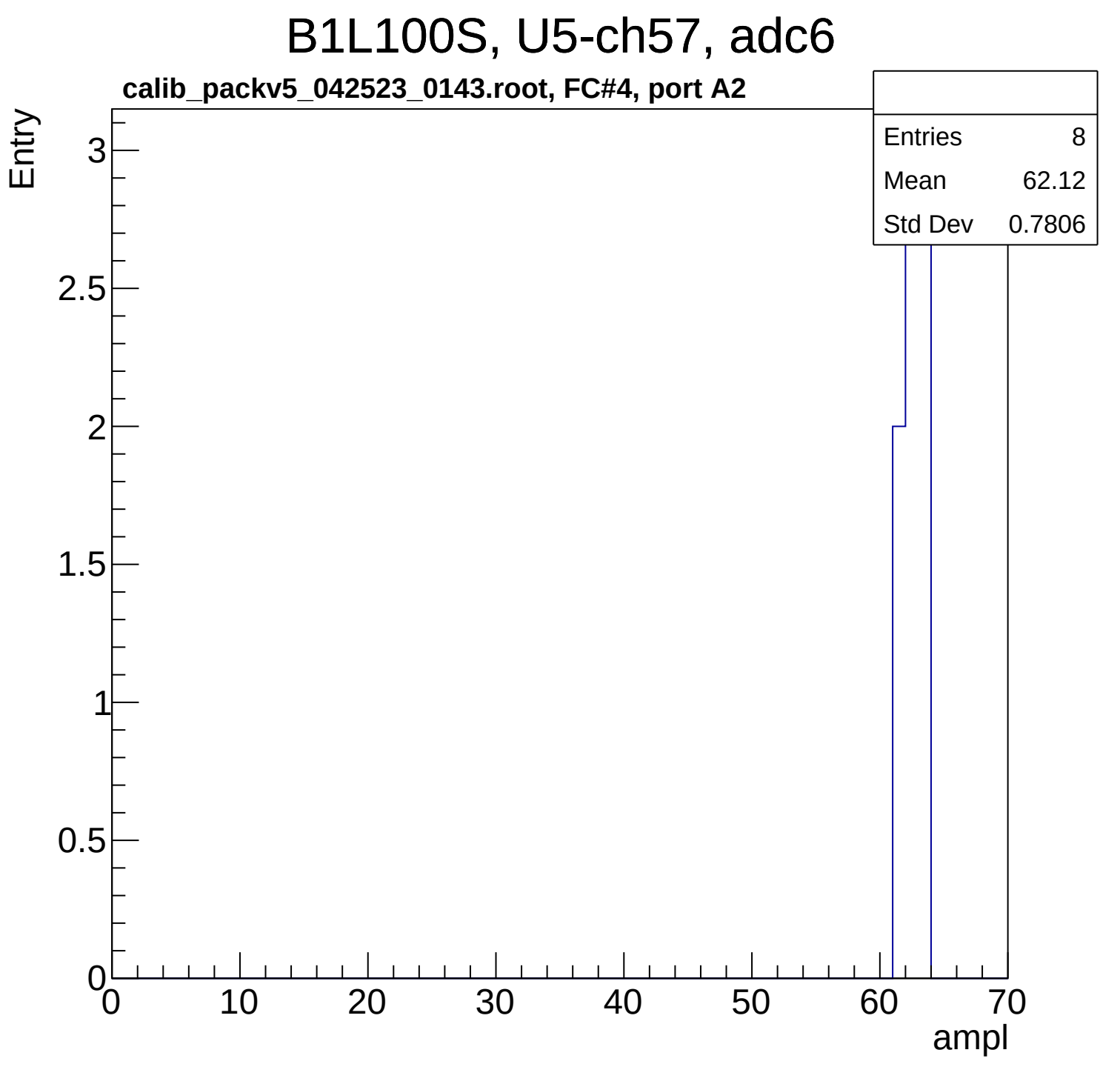
B1L100S, U5-ch57, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 8
Mean 62.12
Std Dev 0.7806
Entry
ampl
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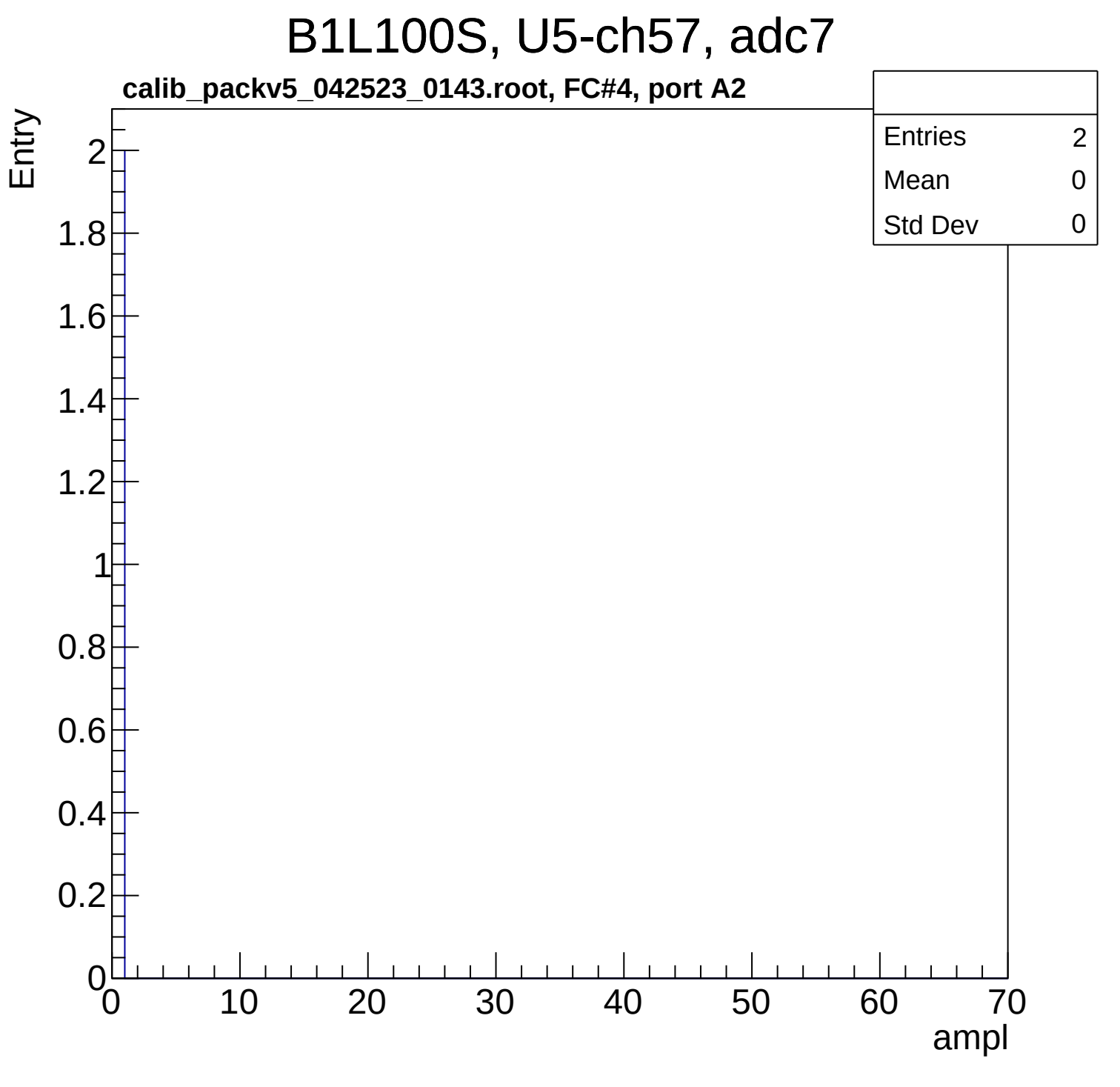
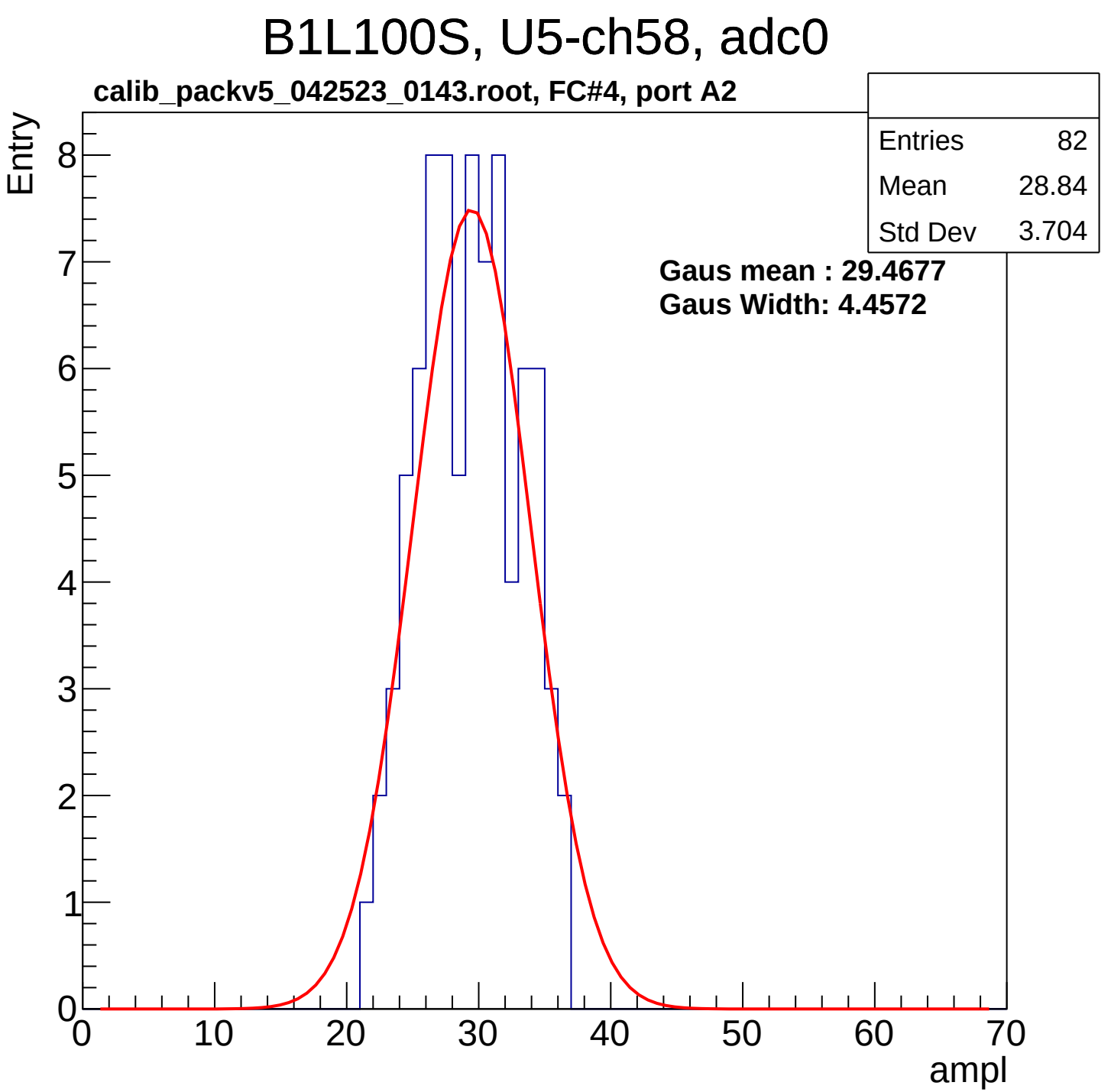
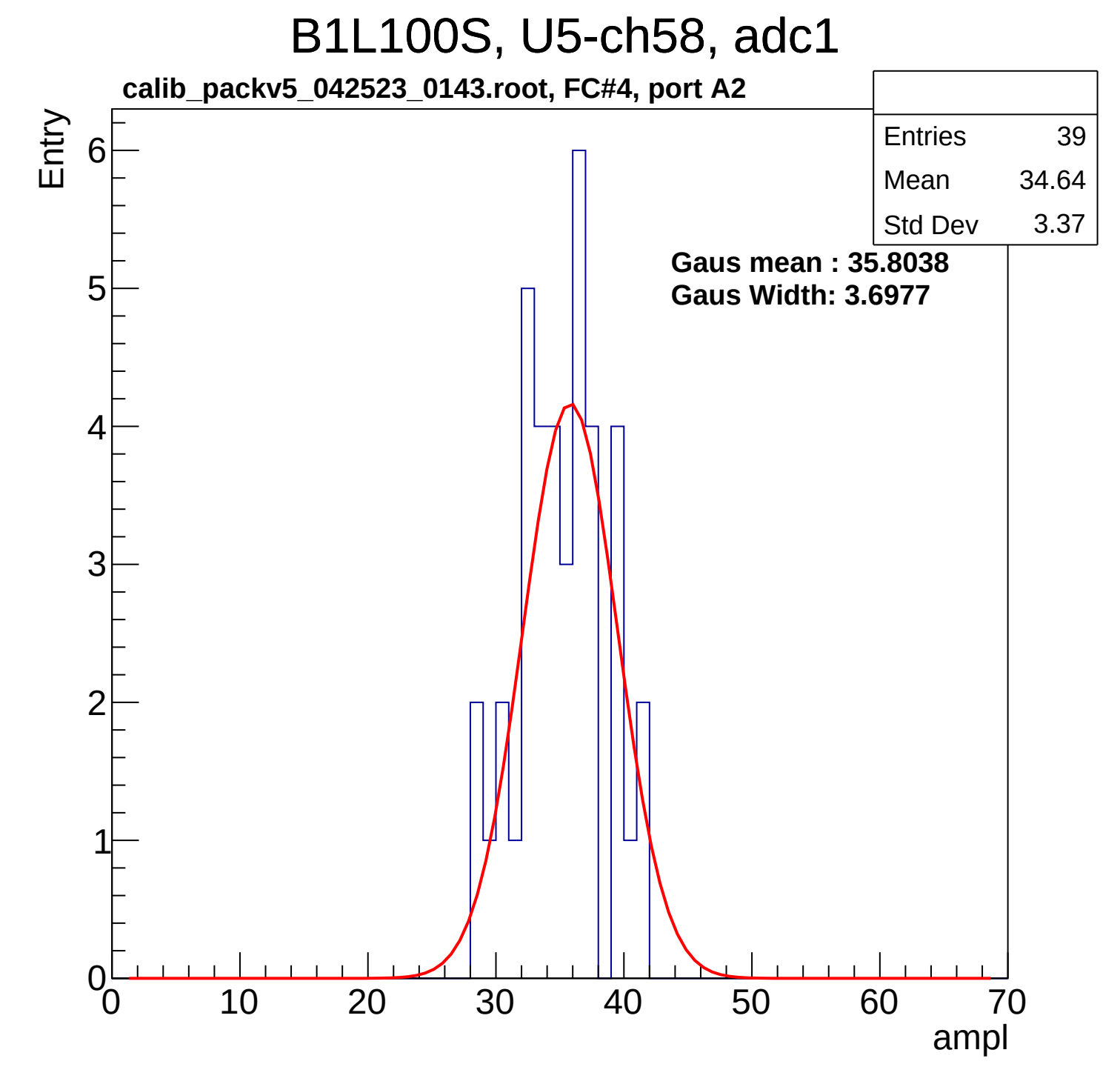
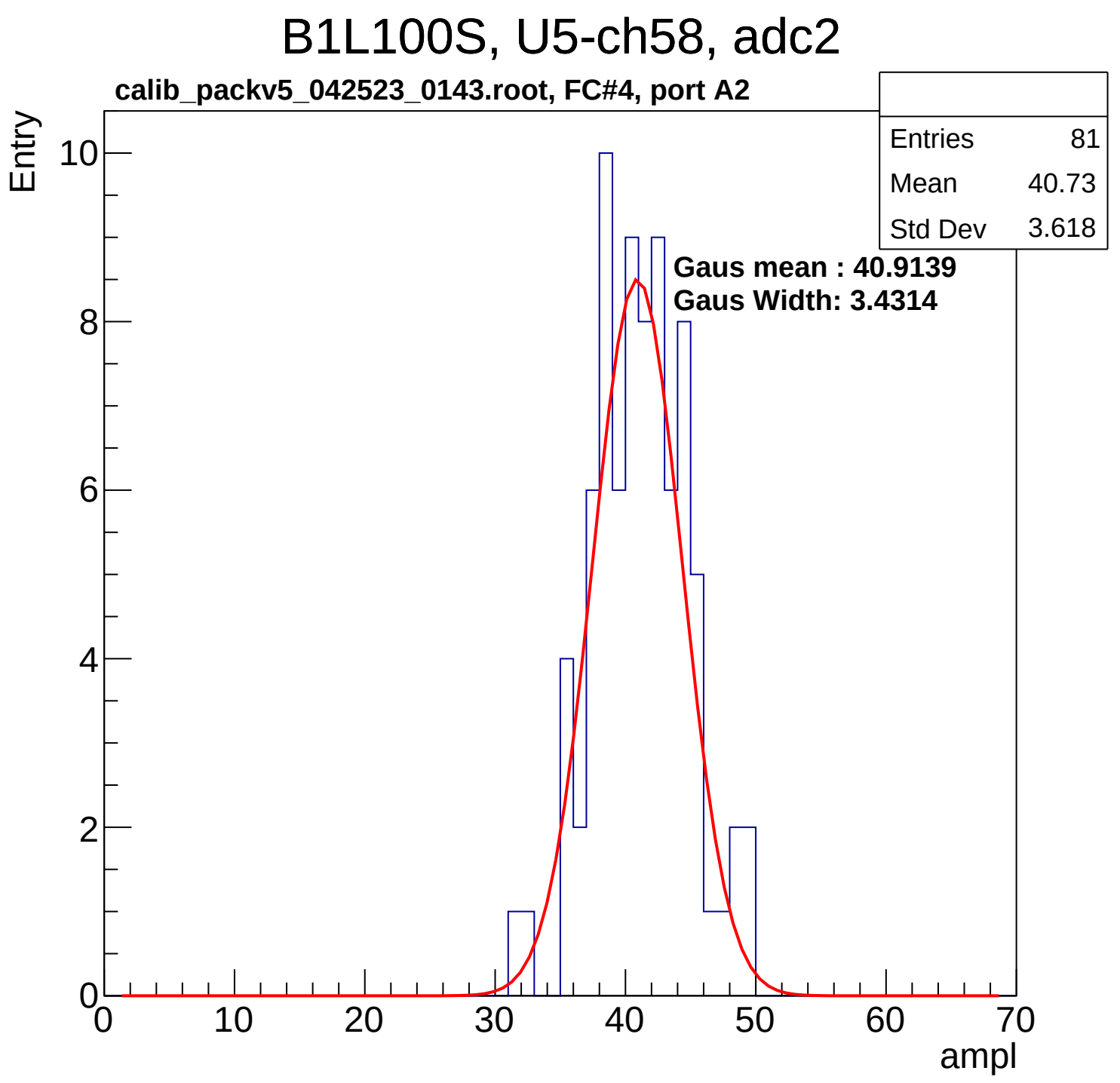
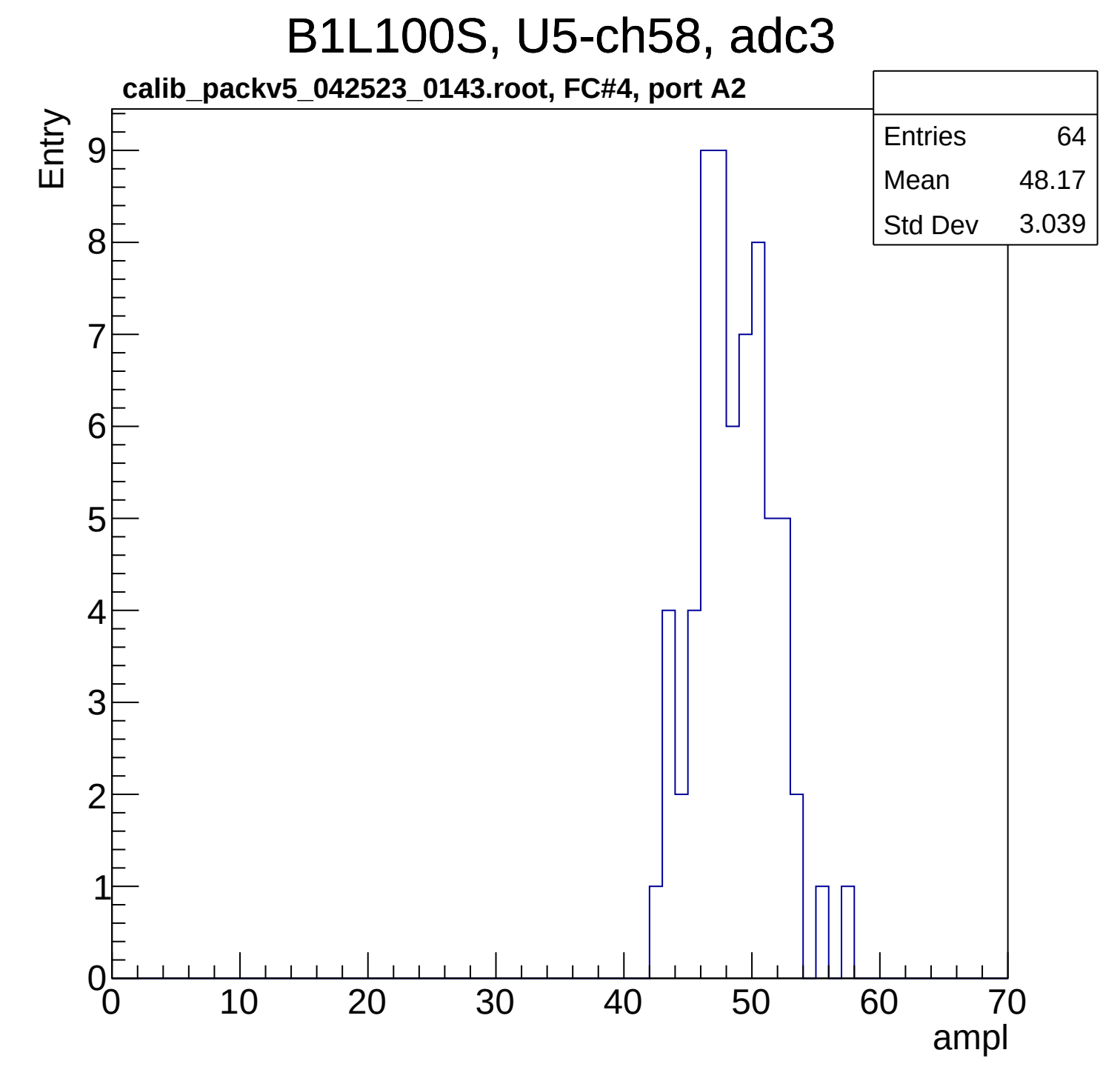
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L100S, U5-ch57, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch58, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 82
Mean 28.84
Std Dev 3.704
Gaus mean : 29.4677
Gaus Width: 4.4572
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch58, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 39
Mean 34.64
Std Dev 3.37
Gaus mean : 35.8038
Gaus Width: 3.6977
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L100S, U5-ch58, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 81
Mean 40.73
Std Dev 3.618
Gaus mean : 40.9139
Gaus Width: 3.4314
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch58, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 48.17
Std Dev 3.039
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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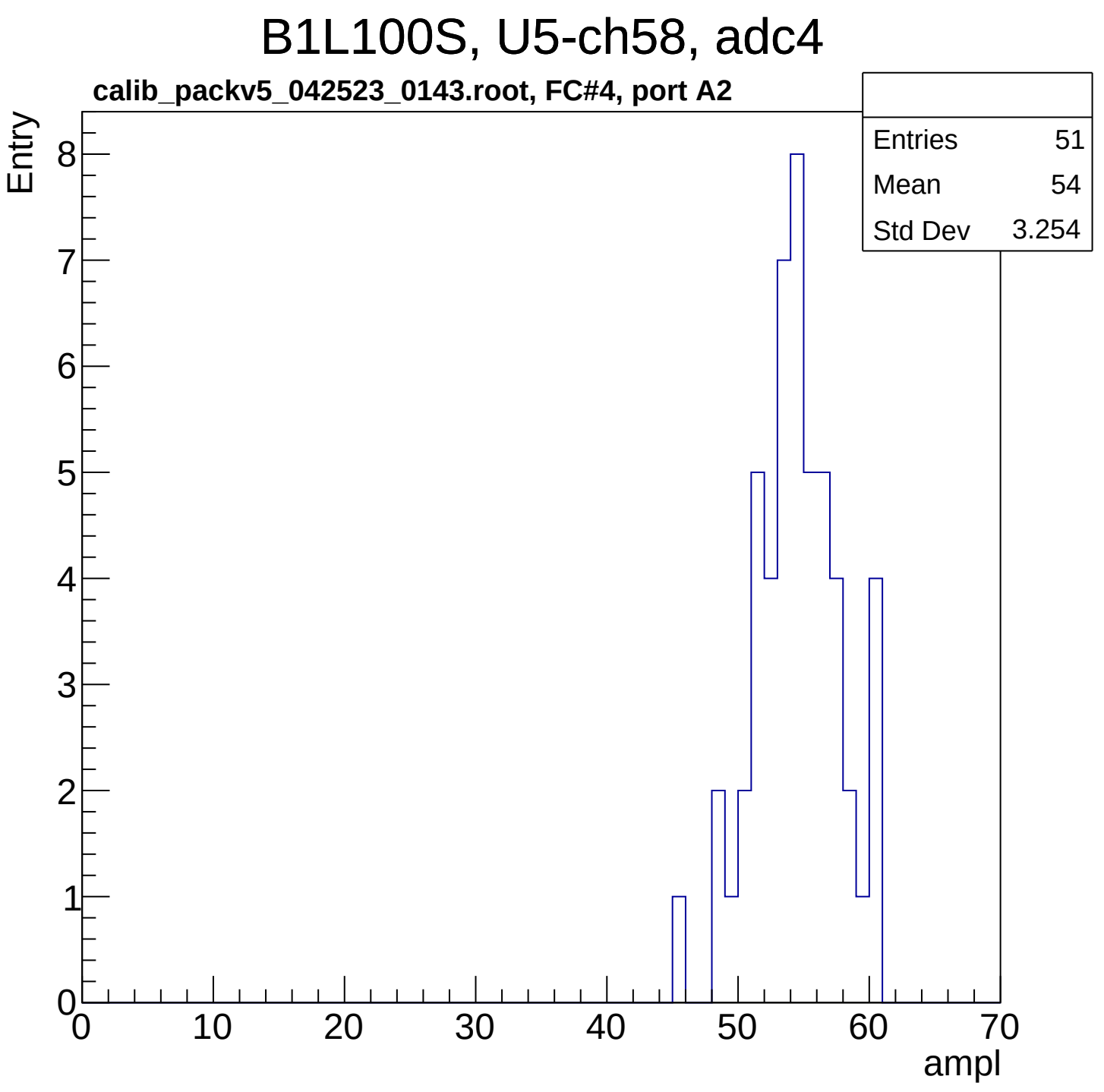
40
50
60
70


B1L100S, U5-ch58, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 54
Std Dev 3.254
Entry
ampl
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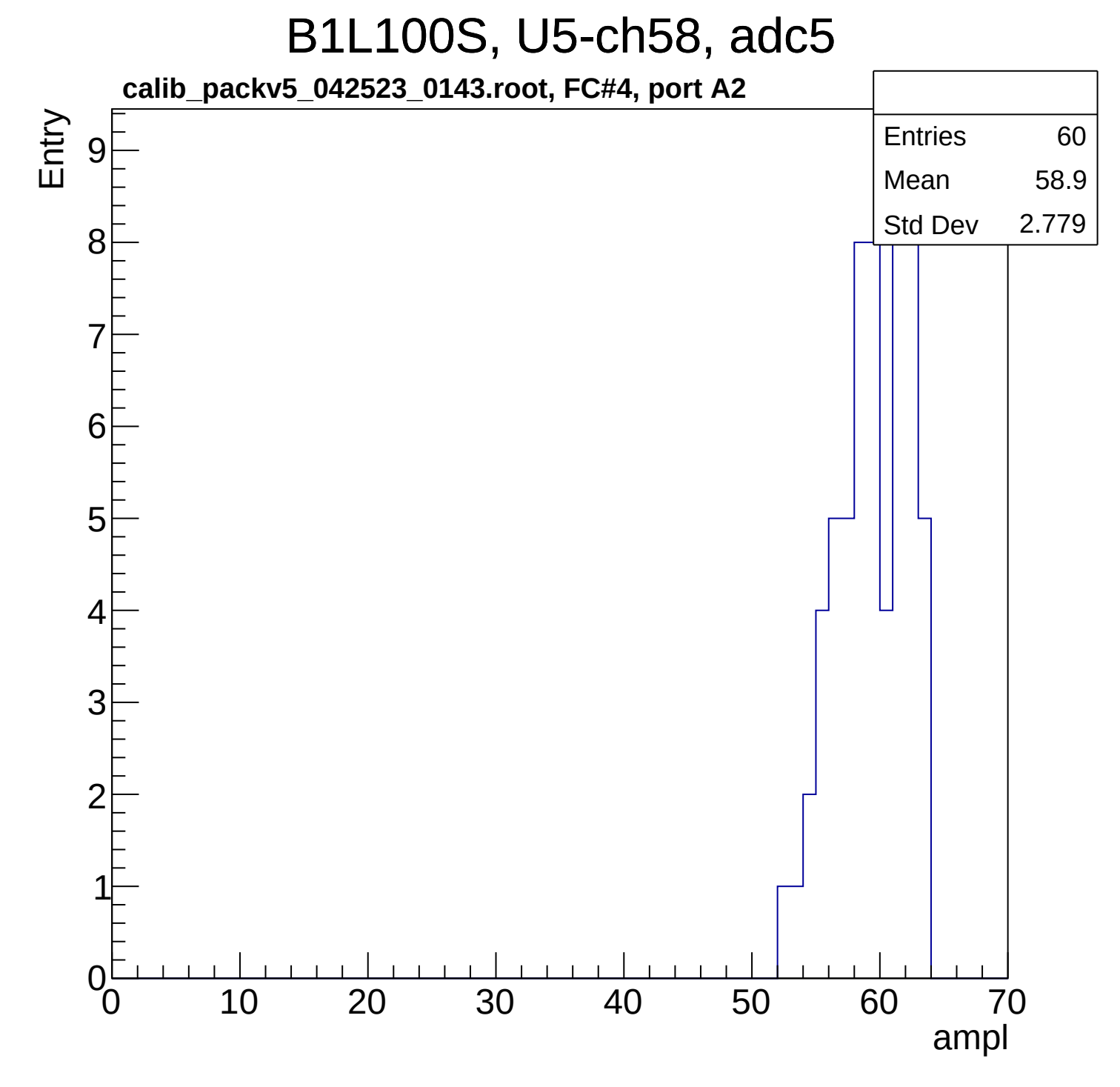
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch58, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 58.9
Std Dev 2.779
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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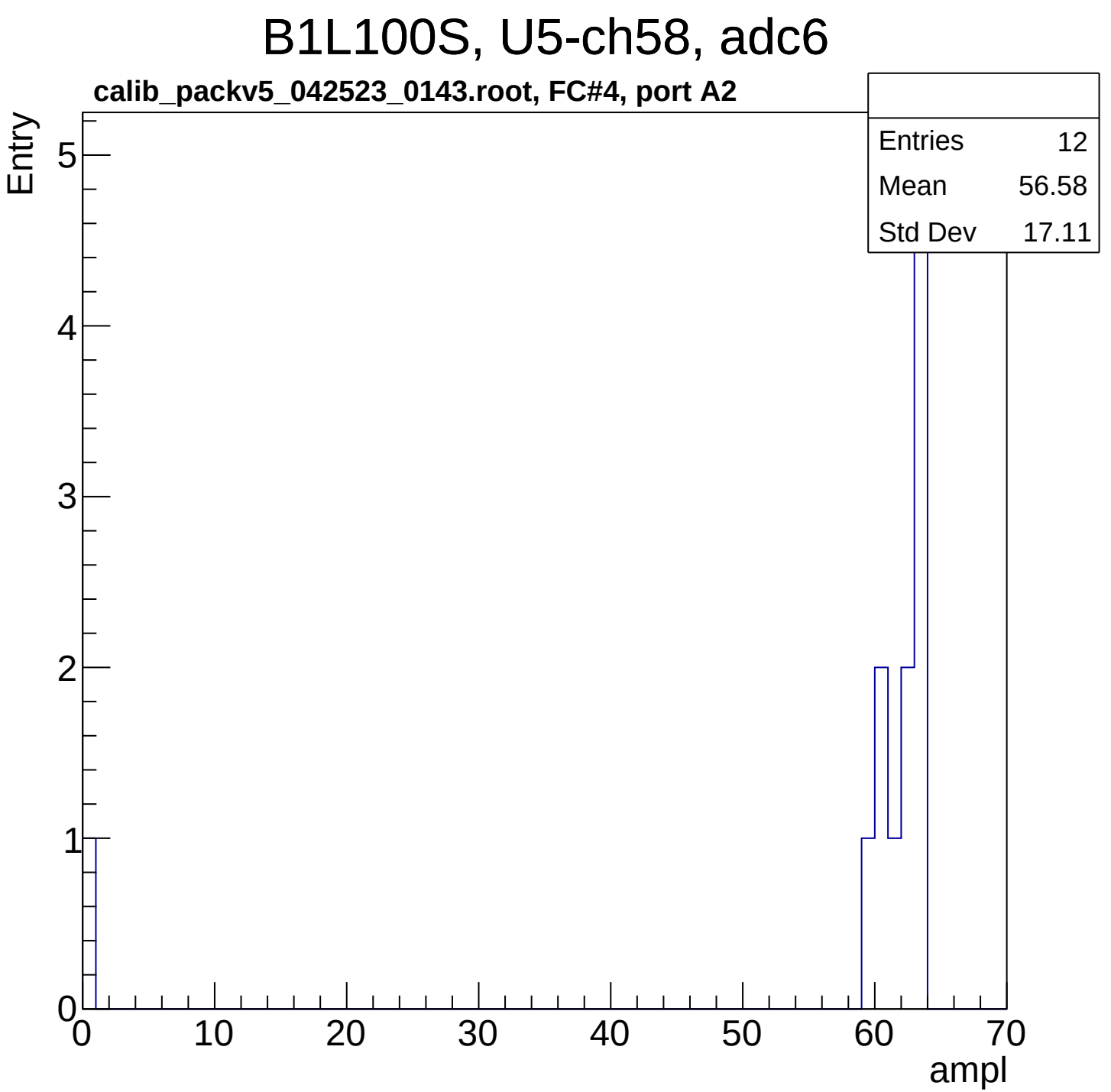
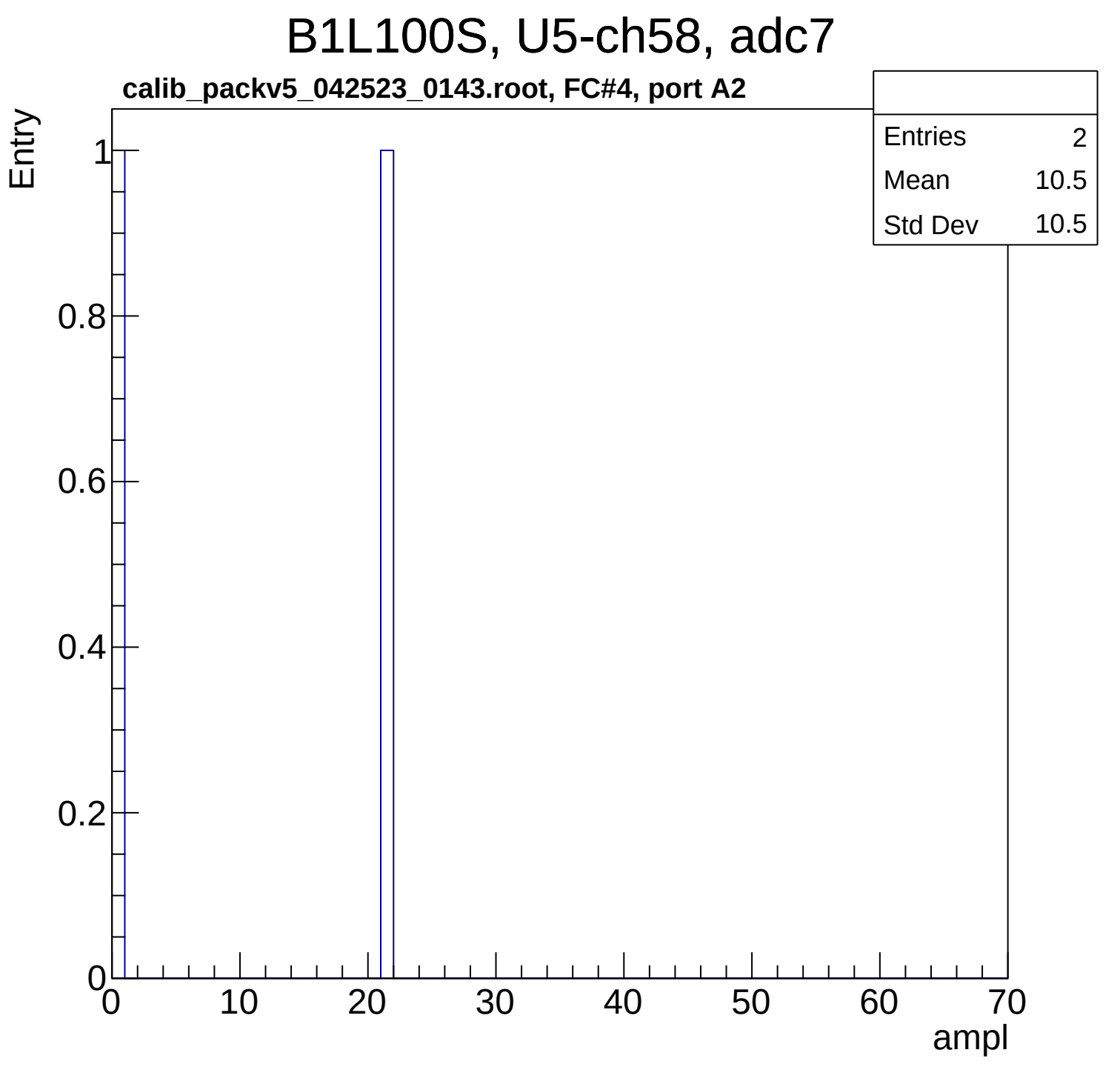
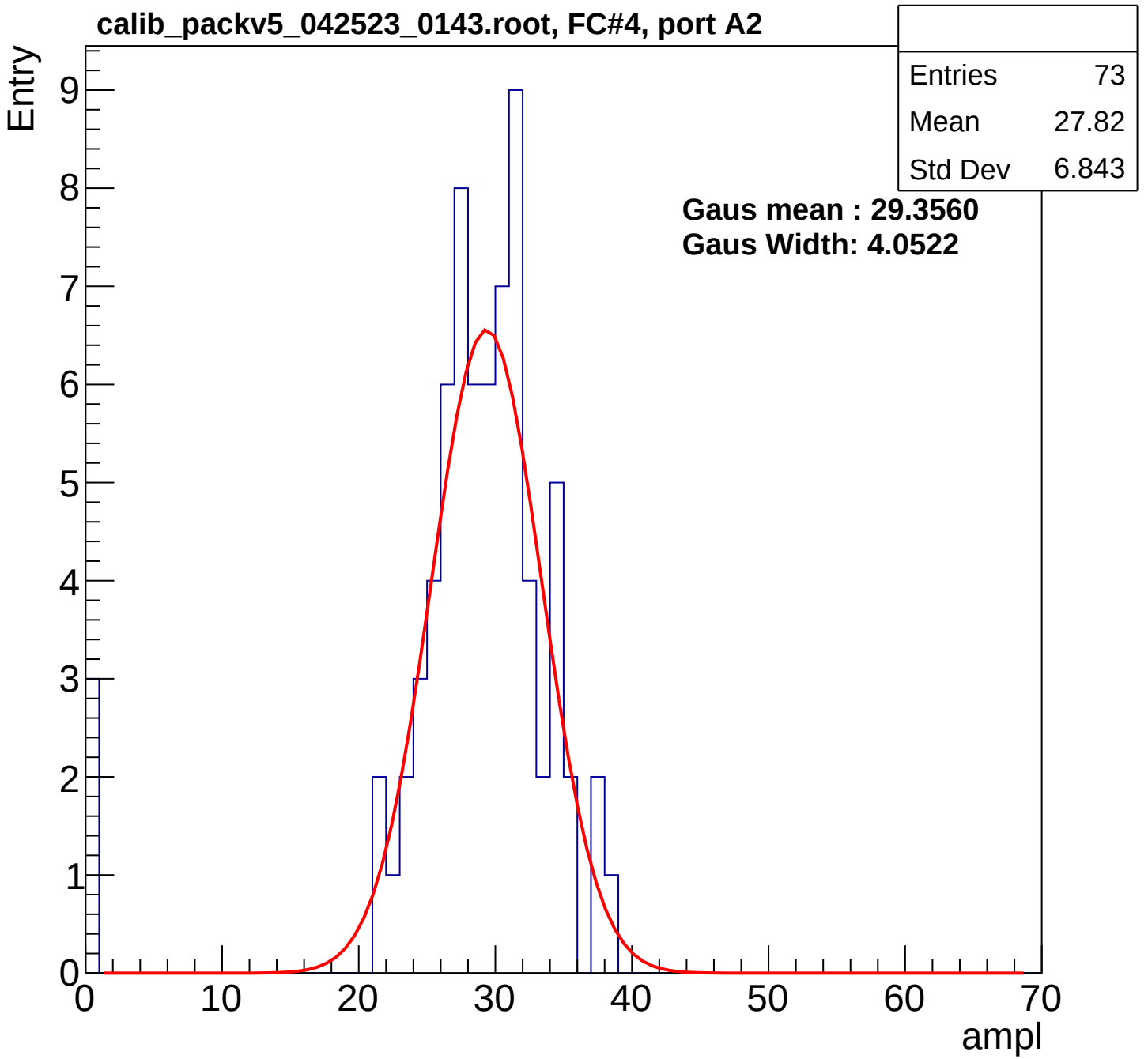
20
30
40
50
60
70


B1L100S, U5-ch58, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 12
Mean 56.58
Std Dev 17.11
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch58, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 10.5
Std Dev 10.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch59, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 27.82
Std Dev 6.843
Gaus mean : 29.3560
Gaus Width: 4.0522
Entry
ampl
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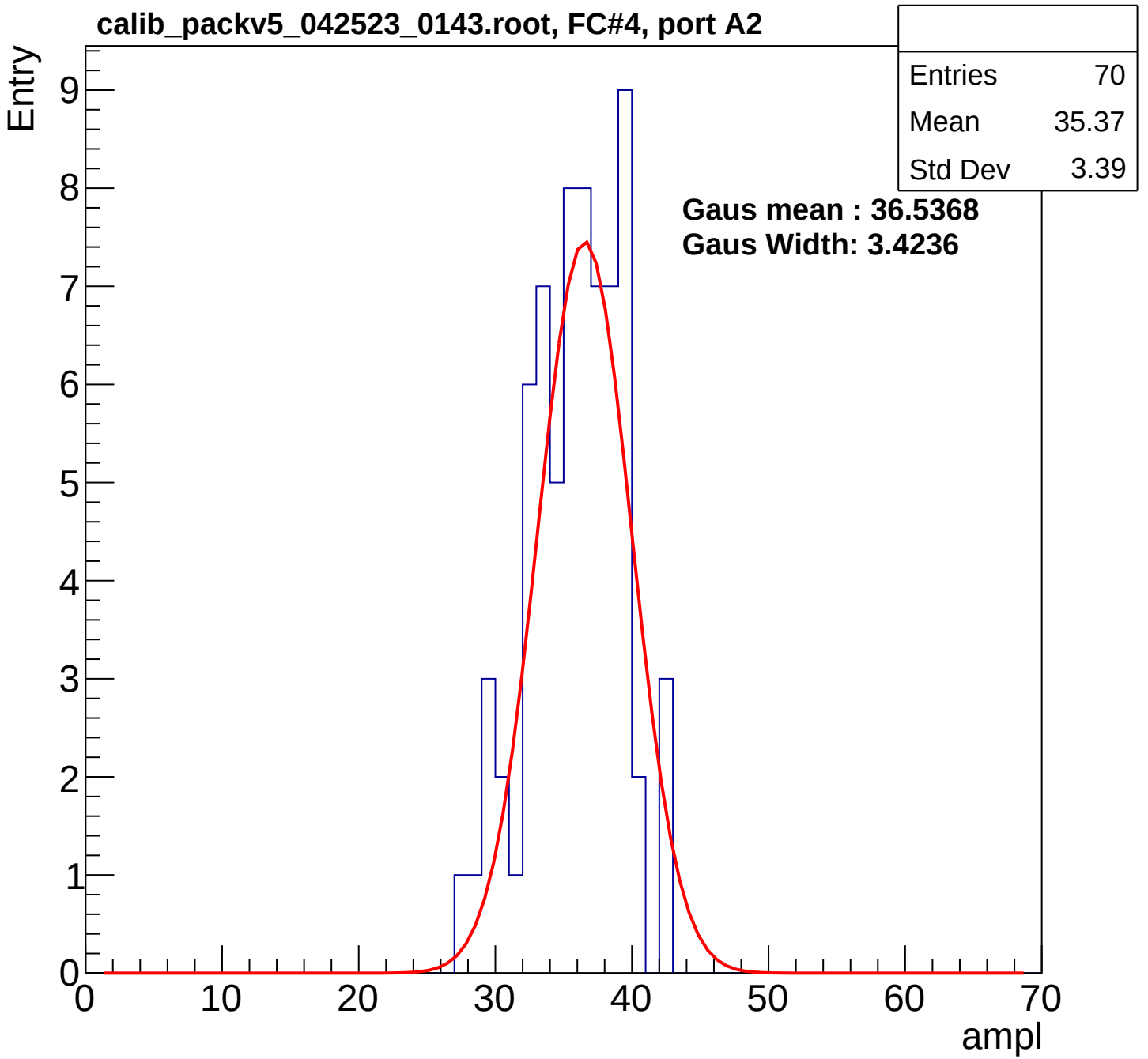
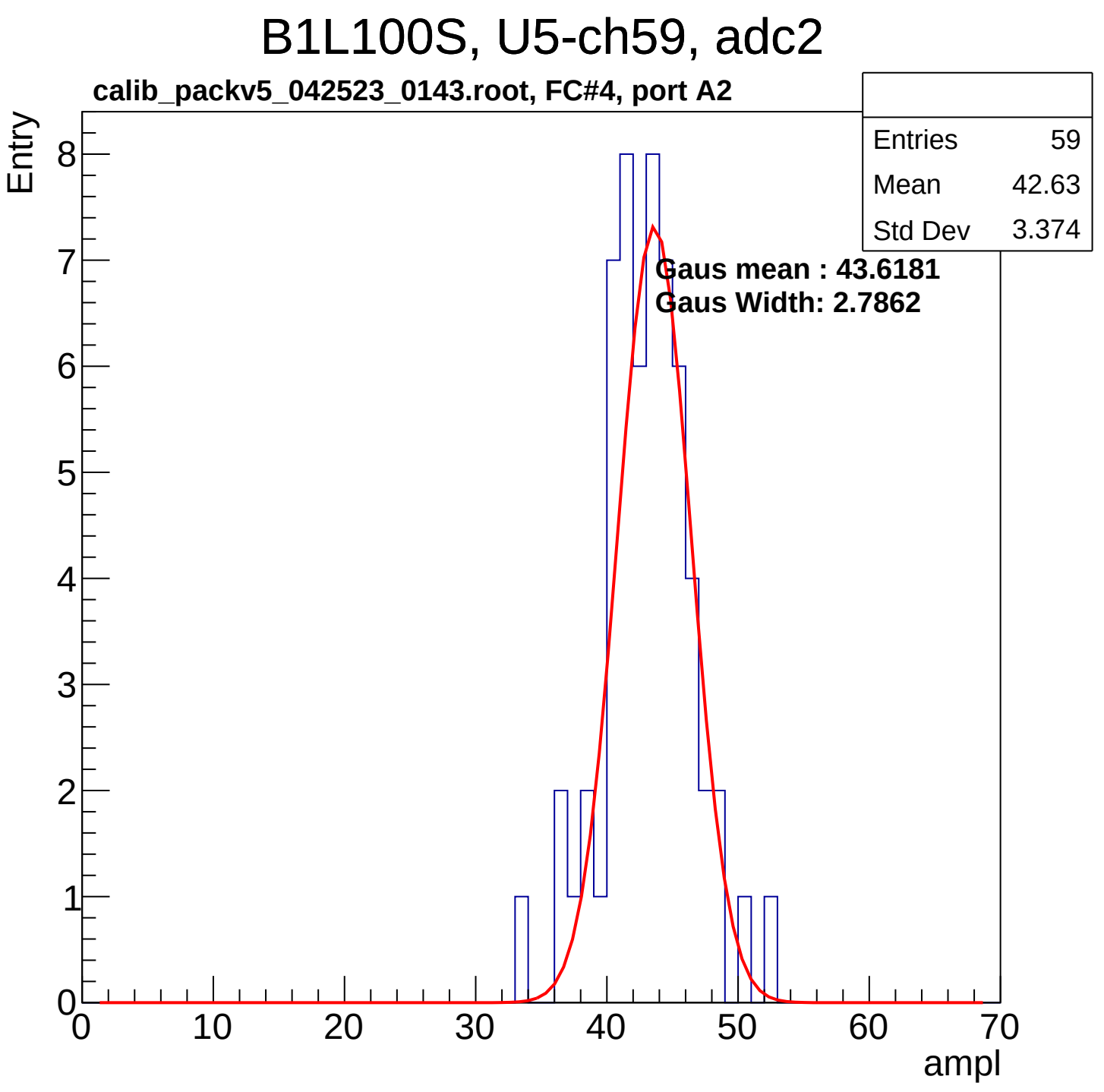
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch59, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 35.37
Std Dev 3.39
Gaus mean : 36.5368
Gaus Width: 3.4236
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch59, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 42.63
Std Dev 3.374
Gaus mean : 43.6181
Gaus Width: 2.7862
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
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40
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60
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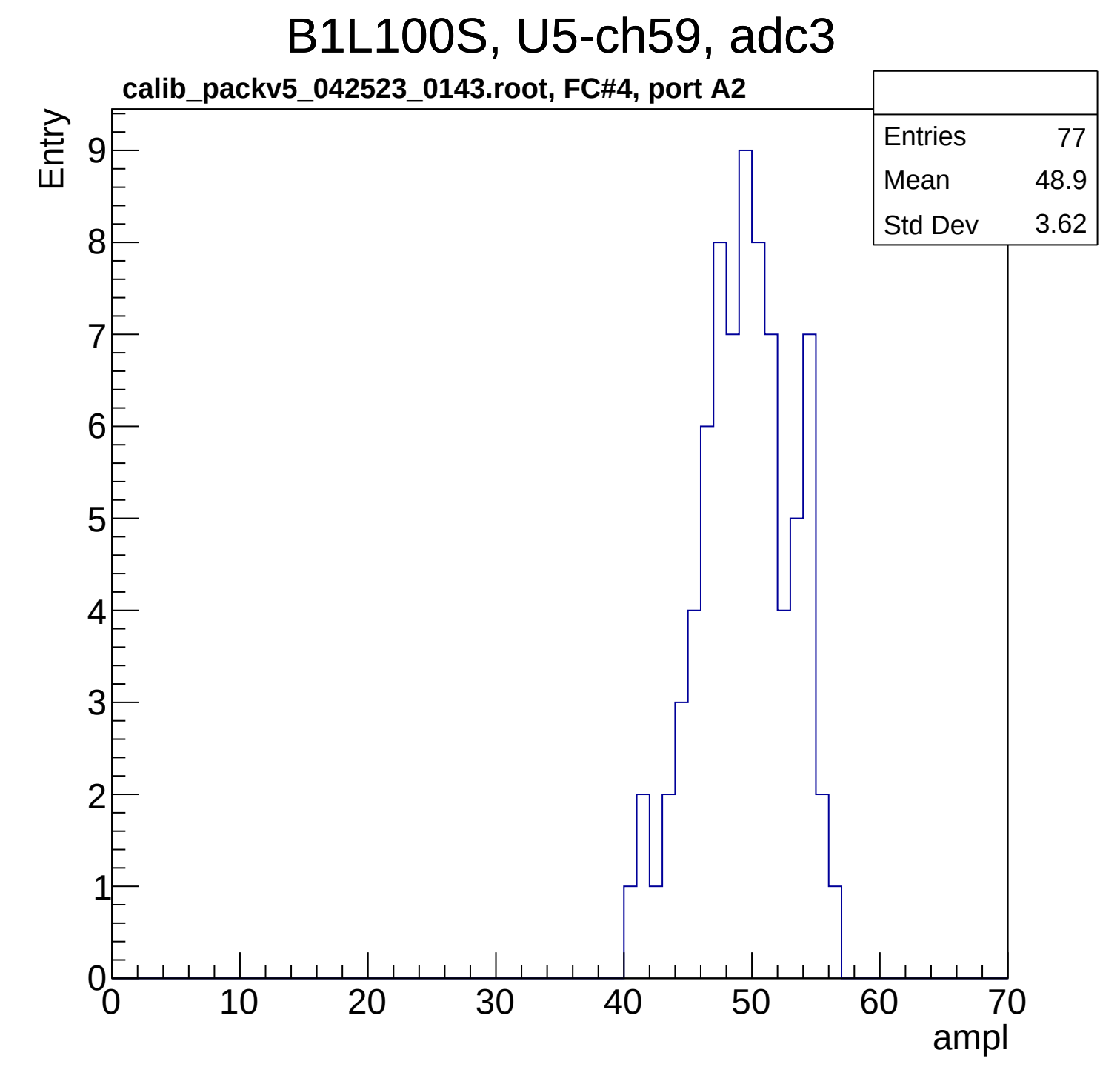
B1L100S, U5-ch59, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 77
Mean 48.9
Std Dev 3.62
Entry
ampl
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2
3
4
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6
7
8
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0
10
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60
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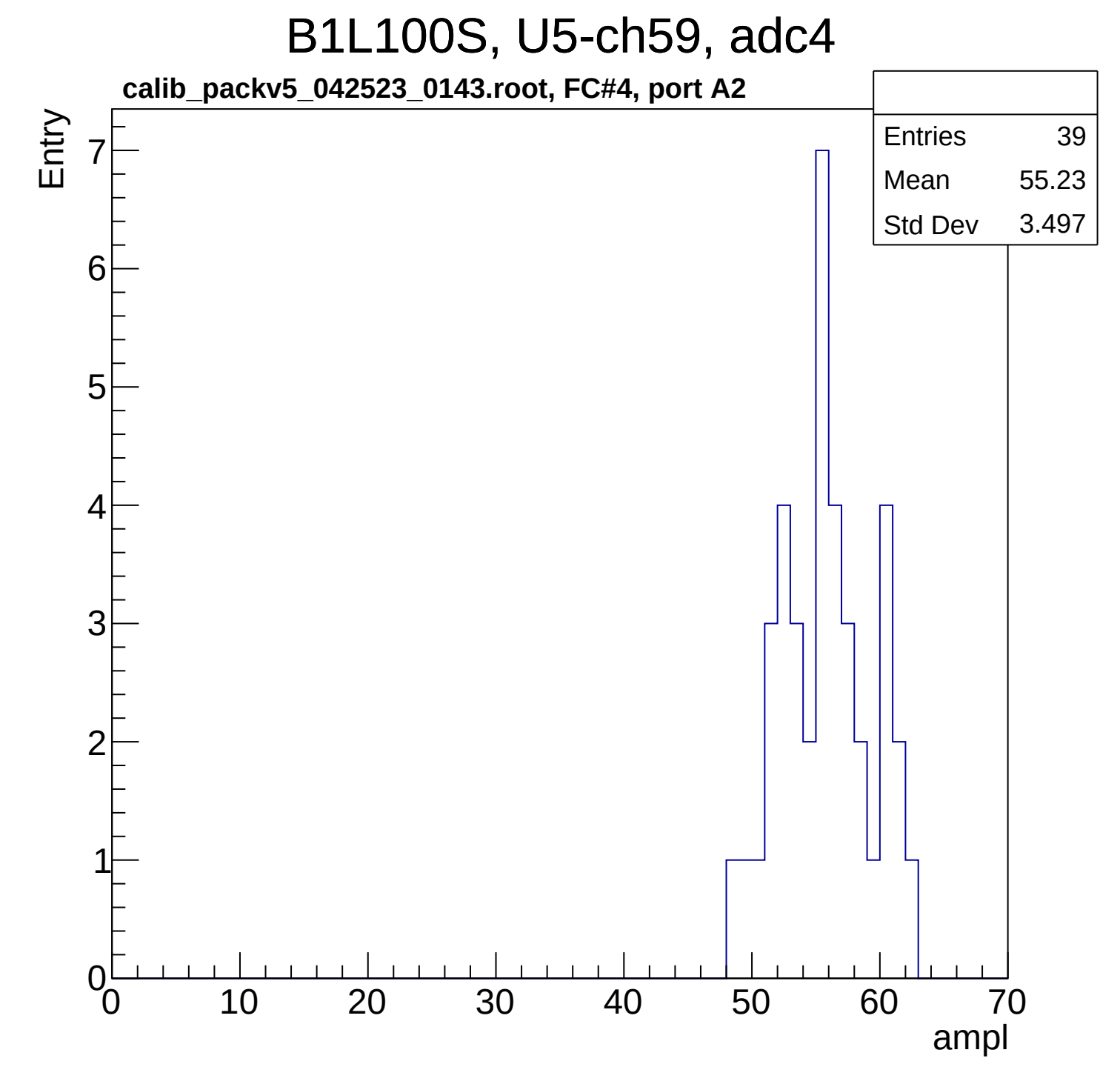
B1L100S, U5-ch59, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 39
Mean 55.23
Std Dev 3.497
Entry
ampl
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1
2
3
4
5
6
7
0
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30
40
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60
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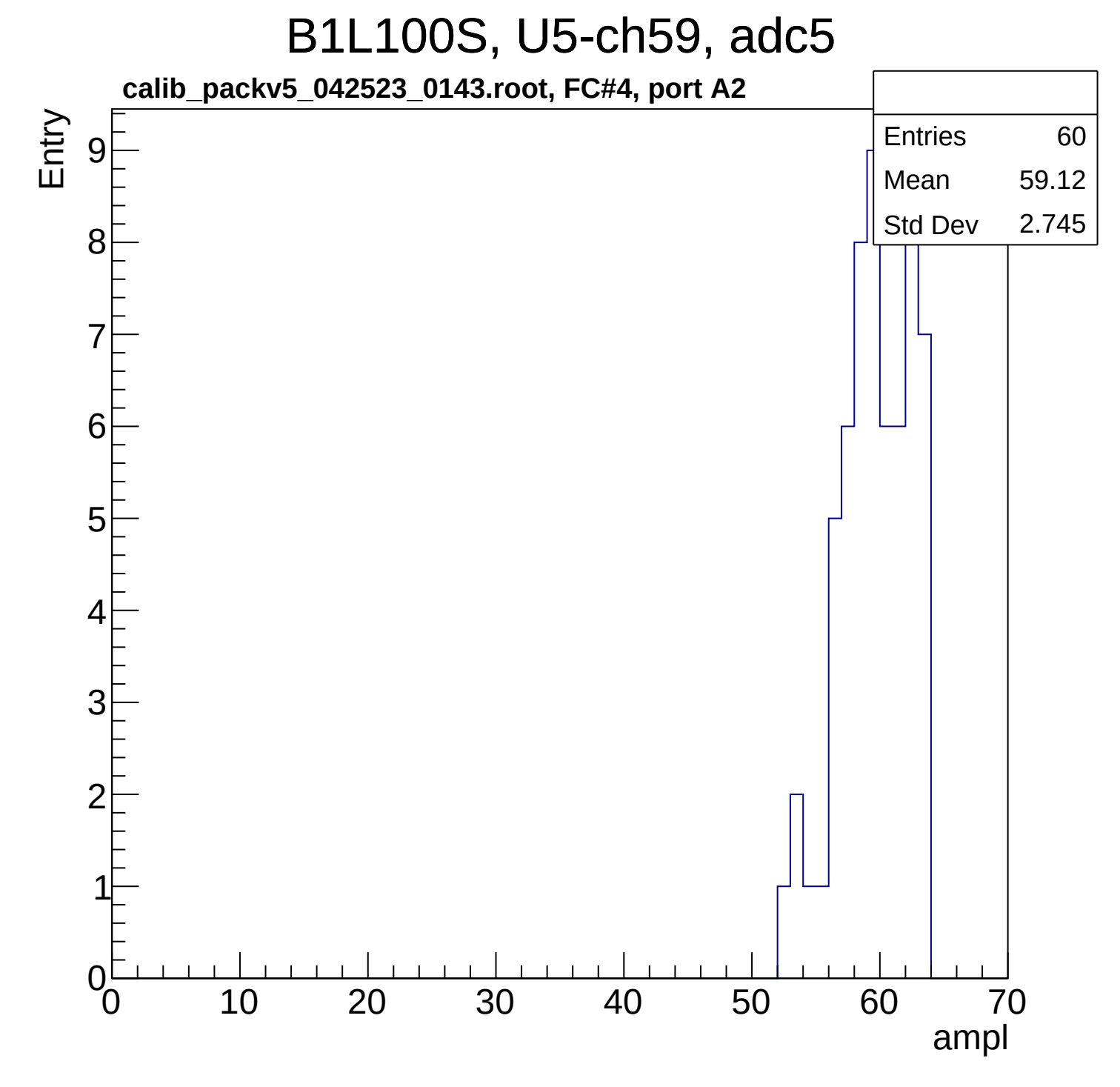
B1L100S, U5-ch59, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 59.12
Std Dev 2.745
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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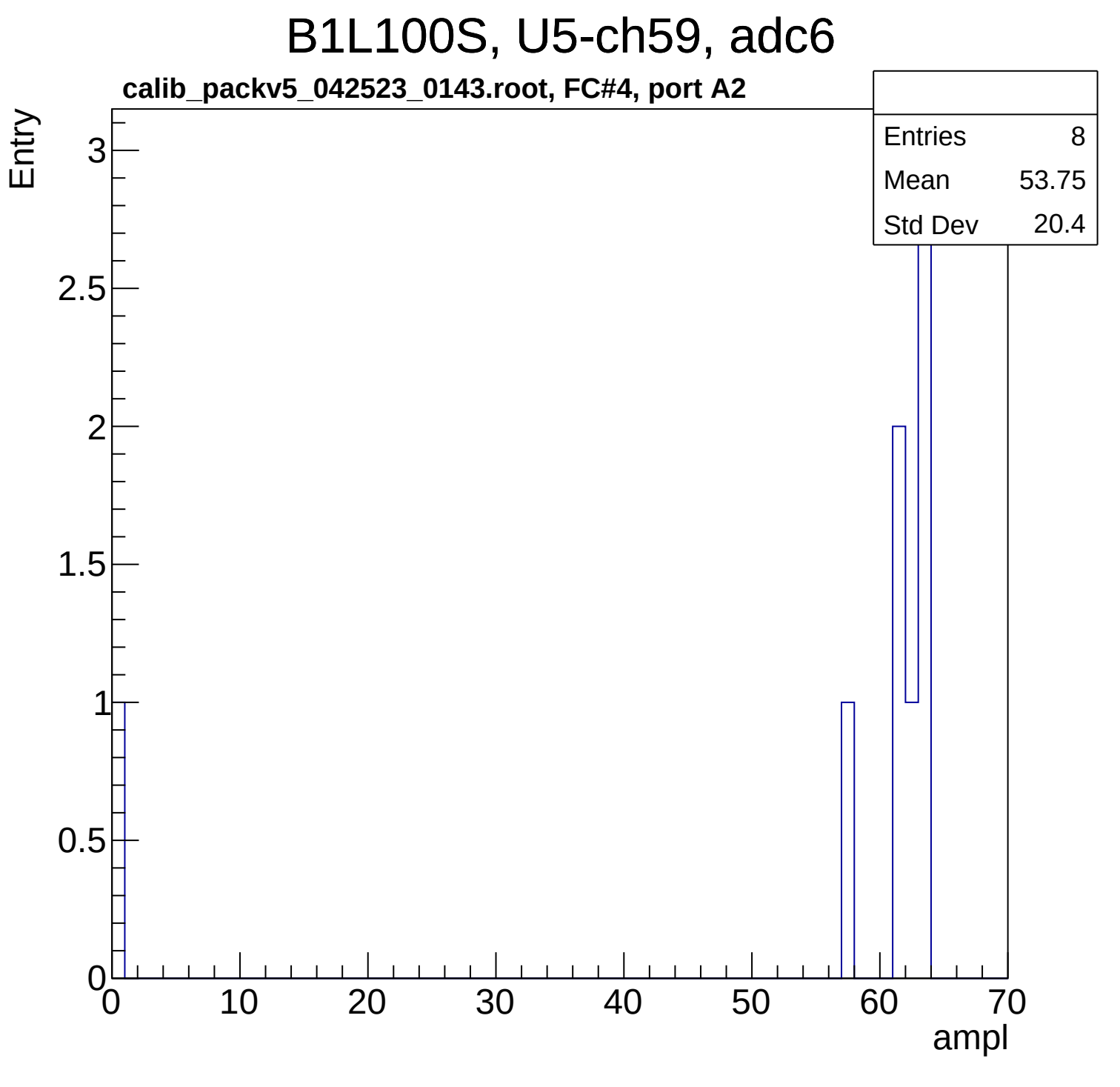
60
70


B1L100S, U5-ch59, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 8
Mean 53.75
Std Dev 20.4
Entry
ampl
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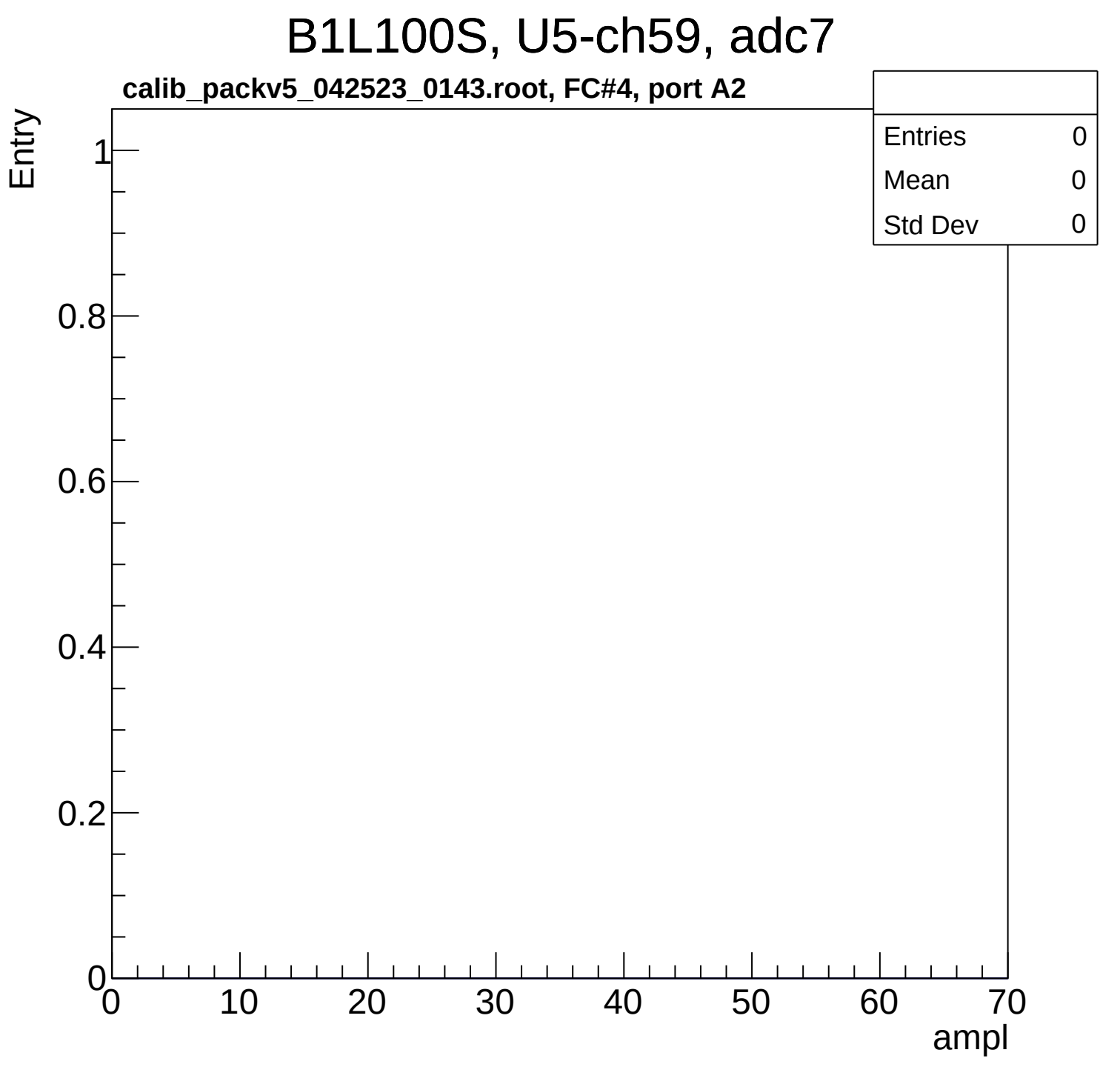
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L100S, U5-ch59, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
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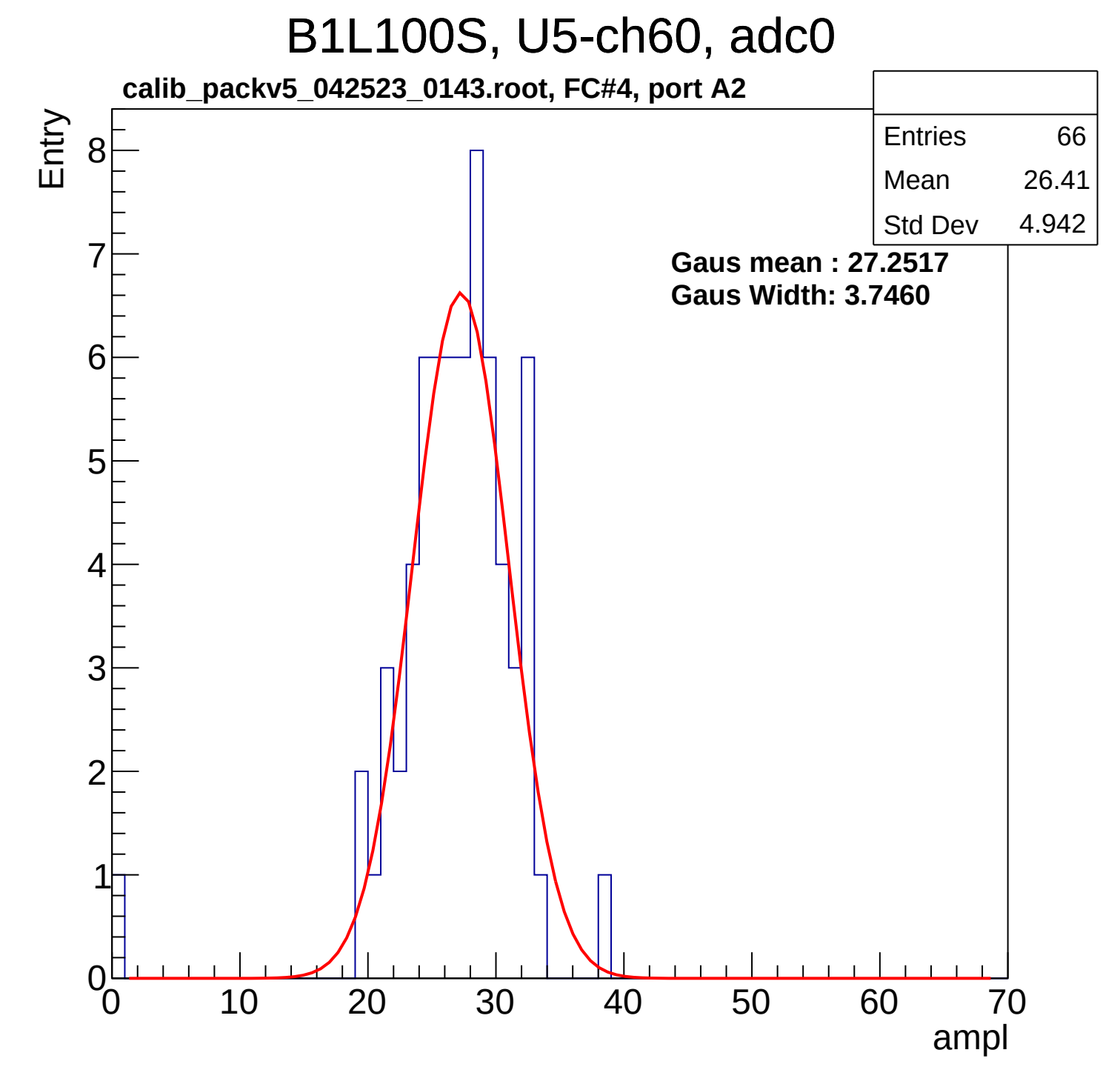
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch60, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 26.41
Std Dev 4.942
Gaus mean : 27.2517
Gaus Width: 3.7460
Entry
ampl
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1
2
3
4
5
6
7
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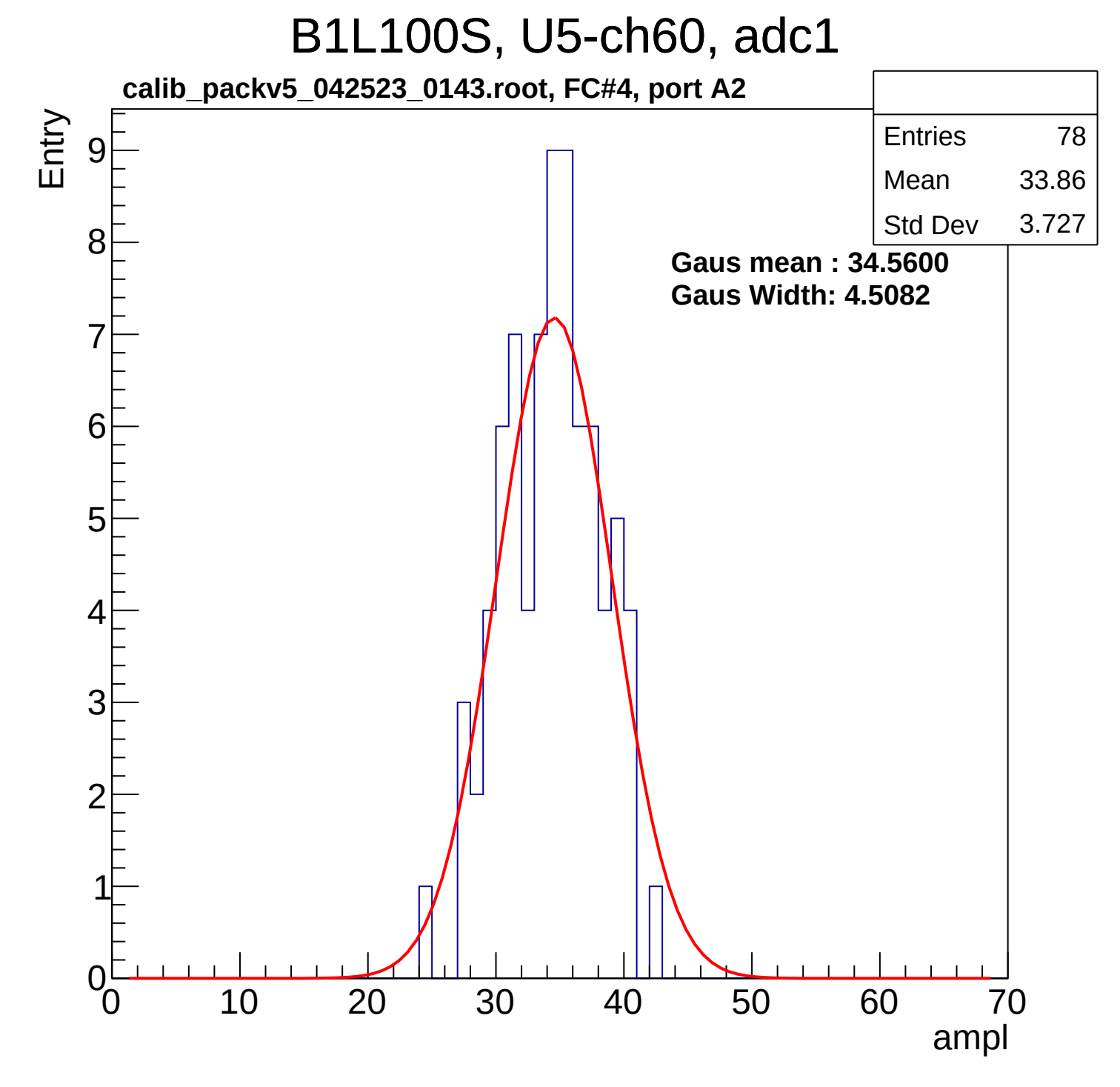
0
10
20
30
40
50
60
70


B1L100S, U5-ch60, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 78
Mean 33.86
Std Dev 3.727
Gaus mean : 34.5600
Gaus Width: 4.5082
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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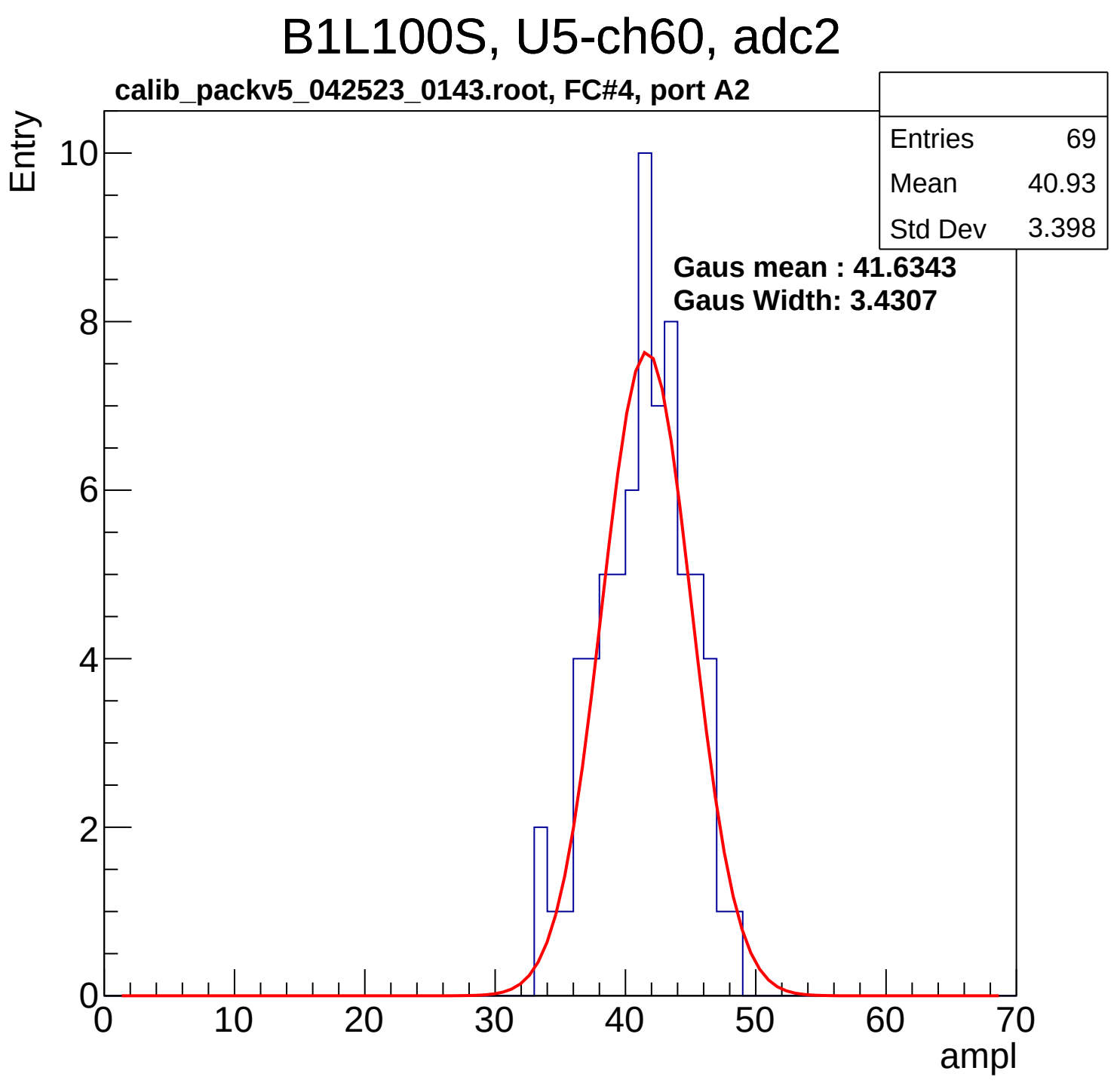
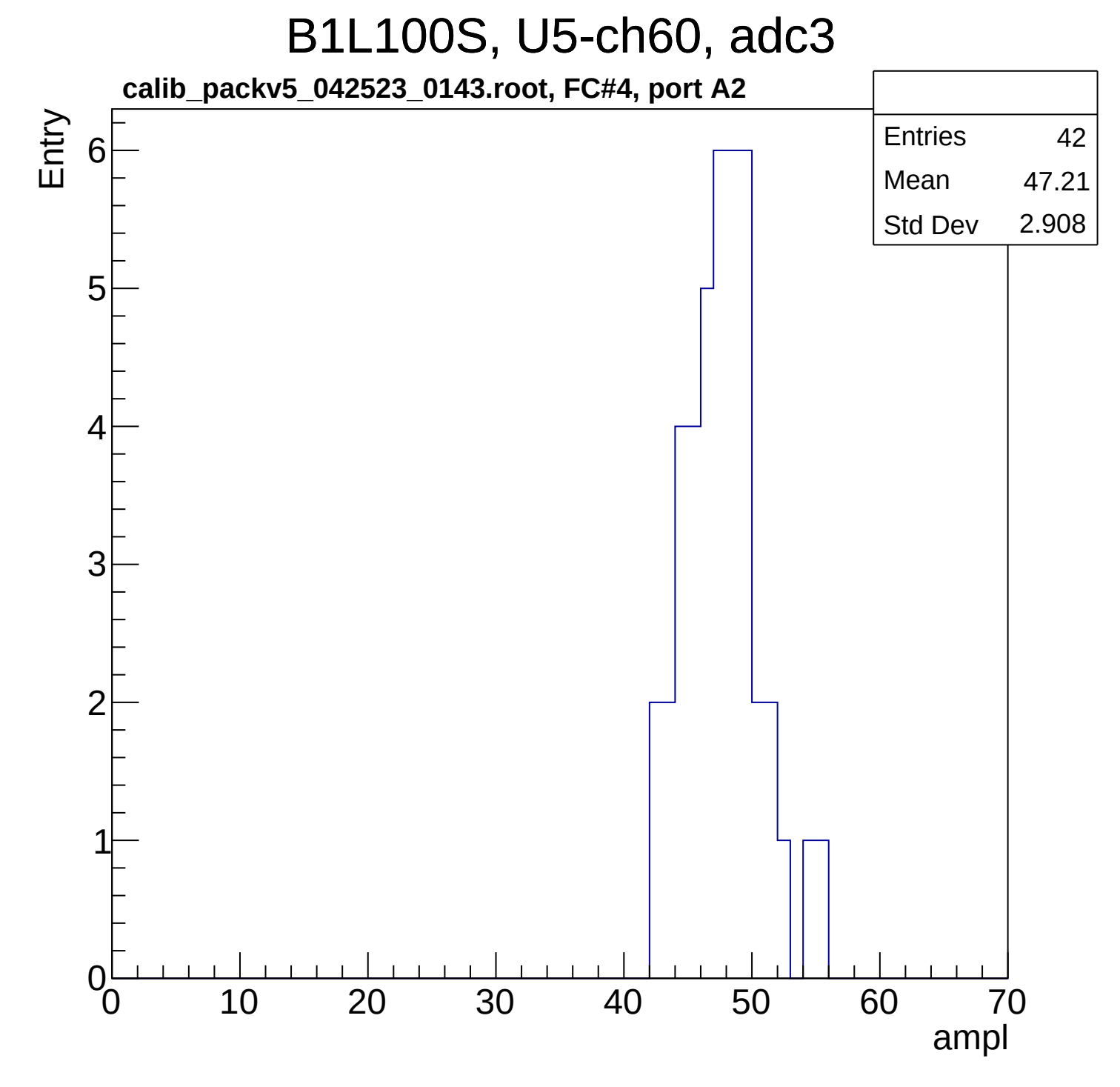
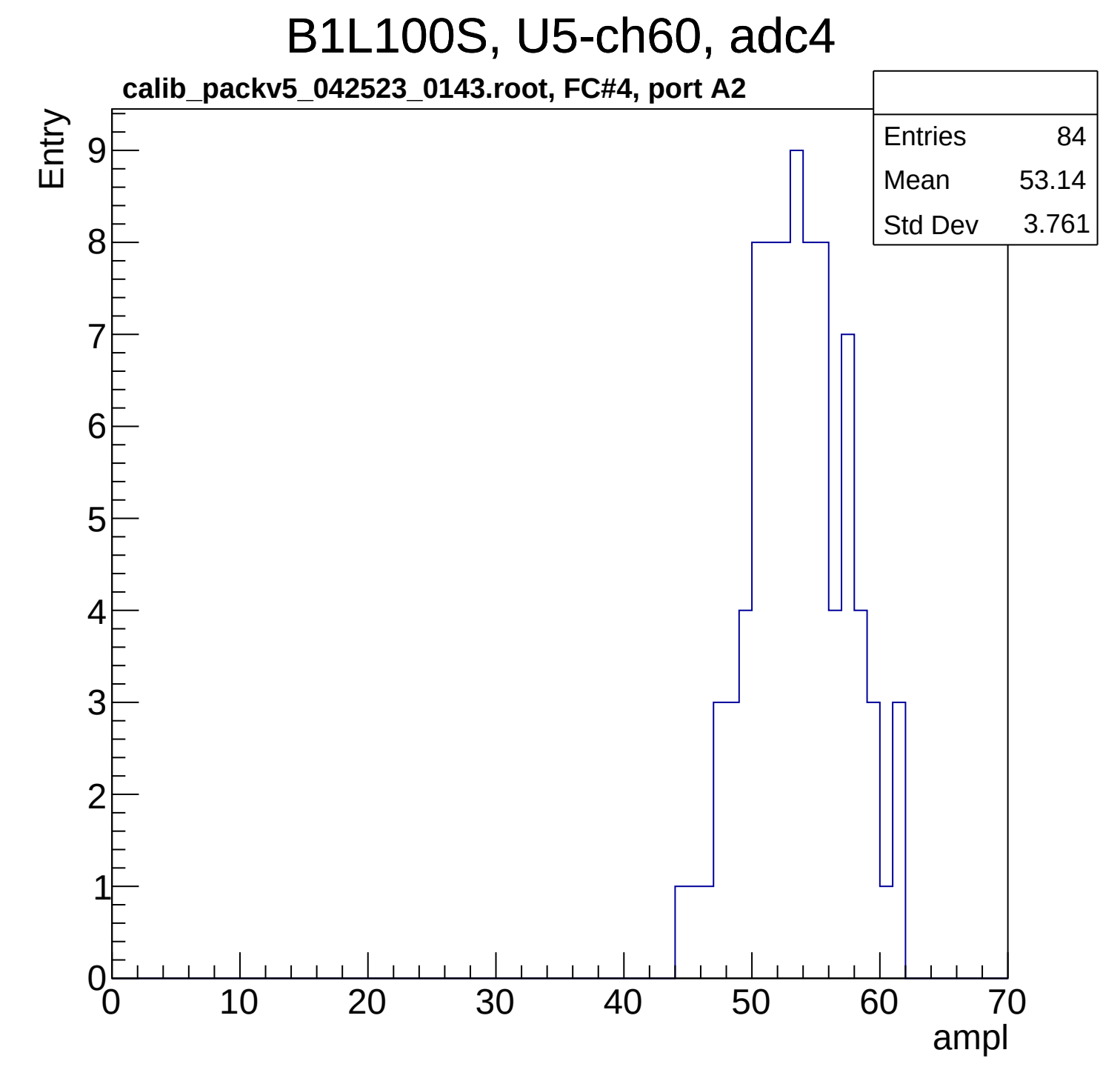

B1L100S, U5-ch60, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 40.93
Std Dev 3.398
Gaus mean : 41.6343
Gaus Width: 3.4307
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch60, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 42
Mean 47.21
Std Dev 2.908
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch60, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 84
Mean 53.14
Std Dev 3.761
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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40
50
60
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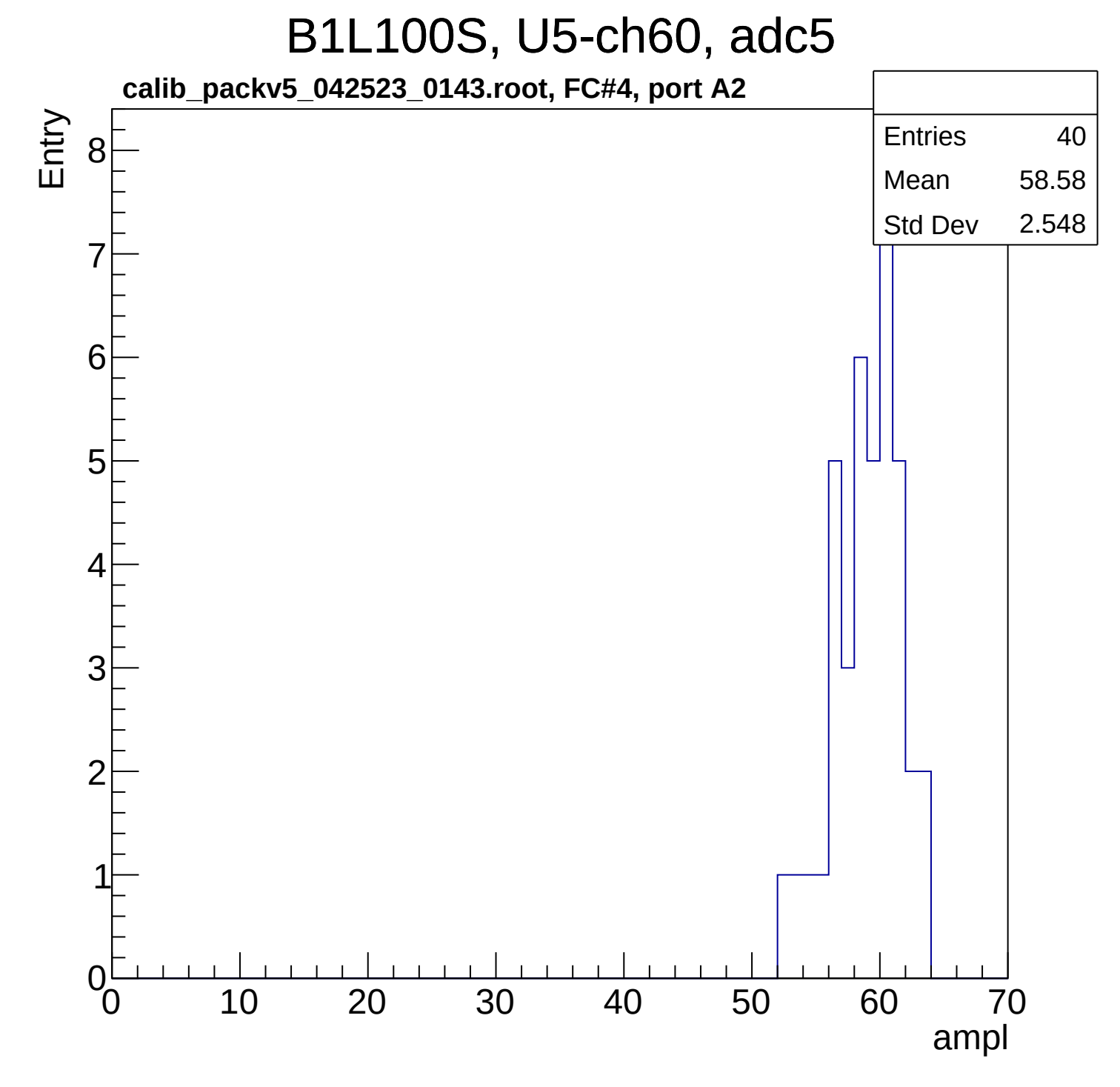
B1L100S, U5-ch60, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 40
Mean 58.58
Std Dev 2.548
Entry
ampl
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1
2
3
4
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0
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40
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60
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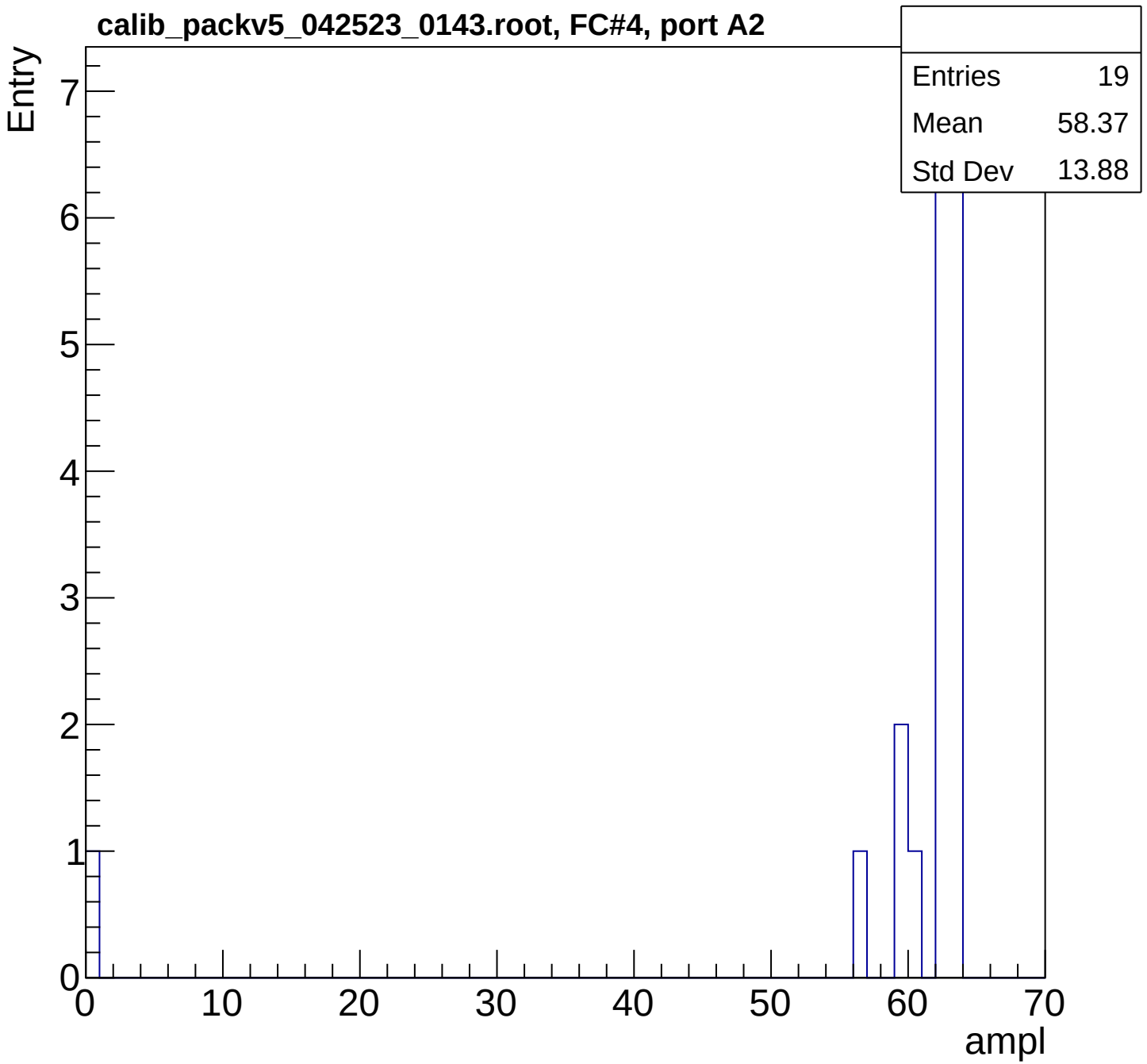
B1L100S, U5-ch60, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 19
Mean 58.37
Std Dev 13.88
Entry
ampl
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1
2
3
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6
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0
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40
50
60
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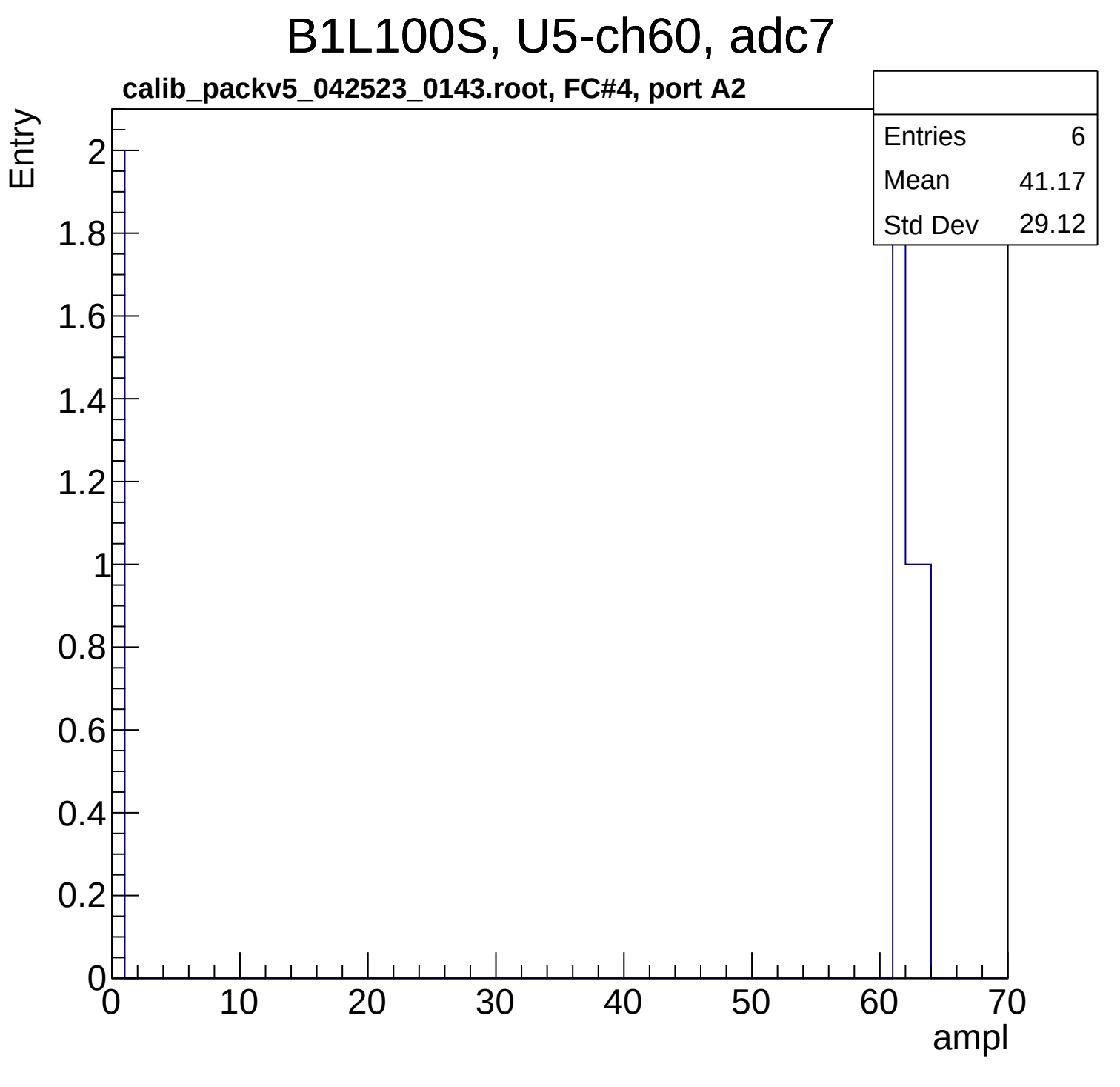
B1L100S, U5-ch60, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 6
Mean 41.17
Std Dev 29.12
Entry
ampl
0
0.2
0.4
0.6
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1
1.2
1.4
1.6
1.8
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0
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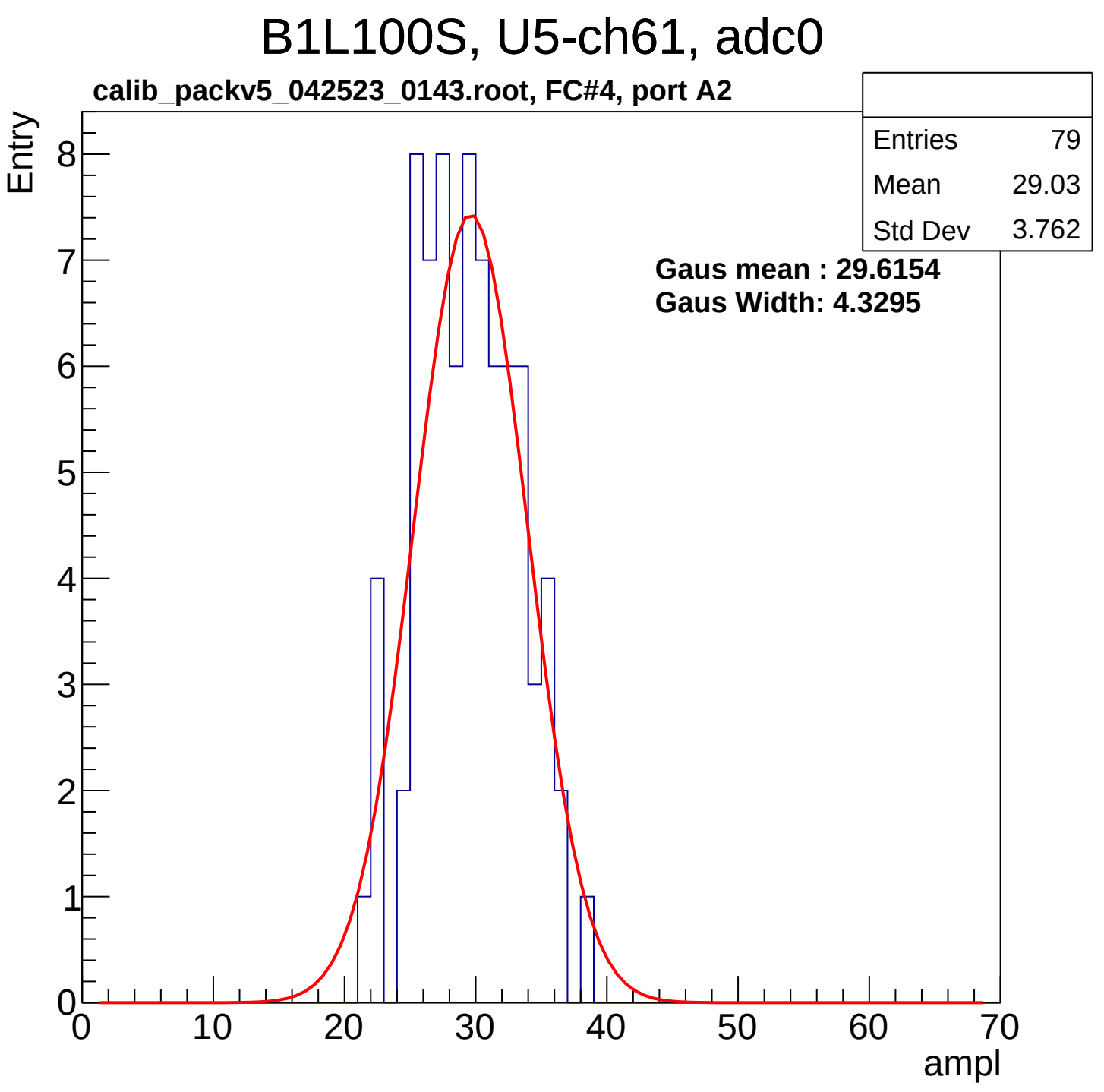
20
30
40
50
60
70


B1L100S, U5-ch61, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 79
Mean 29.03
Std Dev 3.762
Gaus mean : 29.6154
Gaus Width: 4.3295
Entry
ampl
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1
2
3
4
5
6
7
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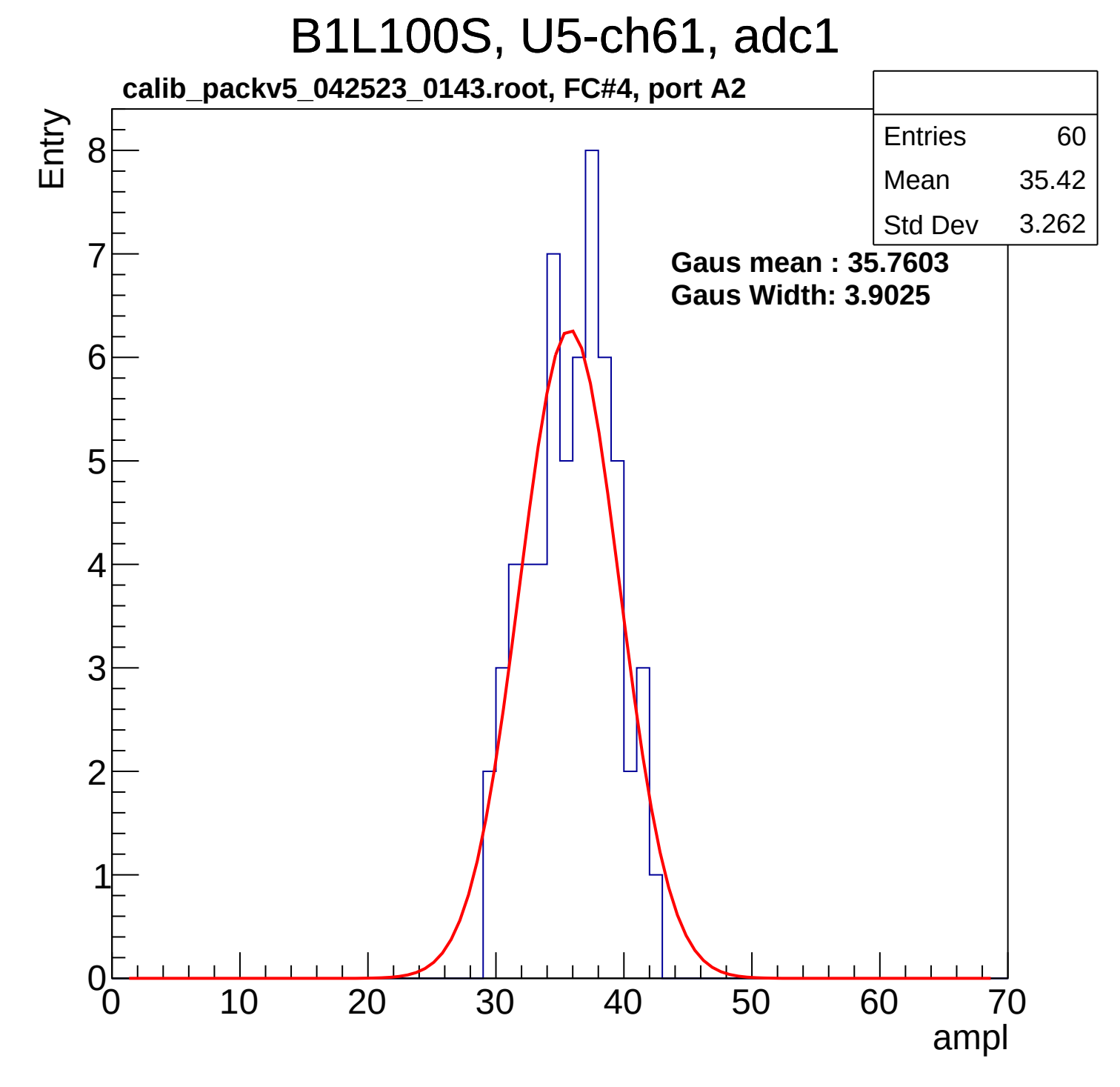
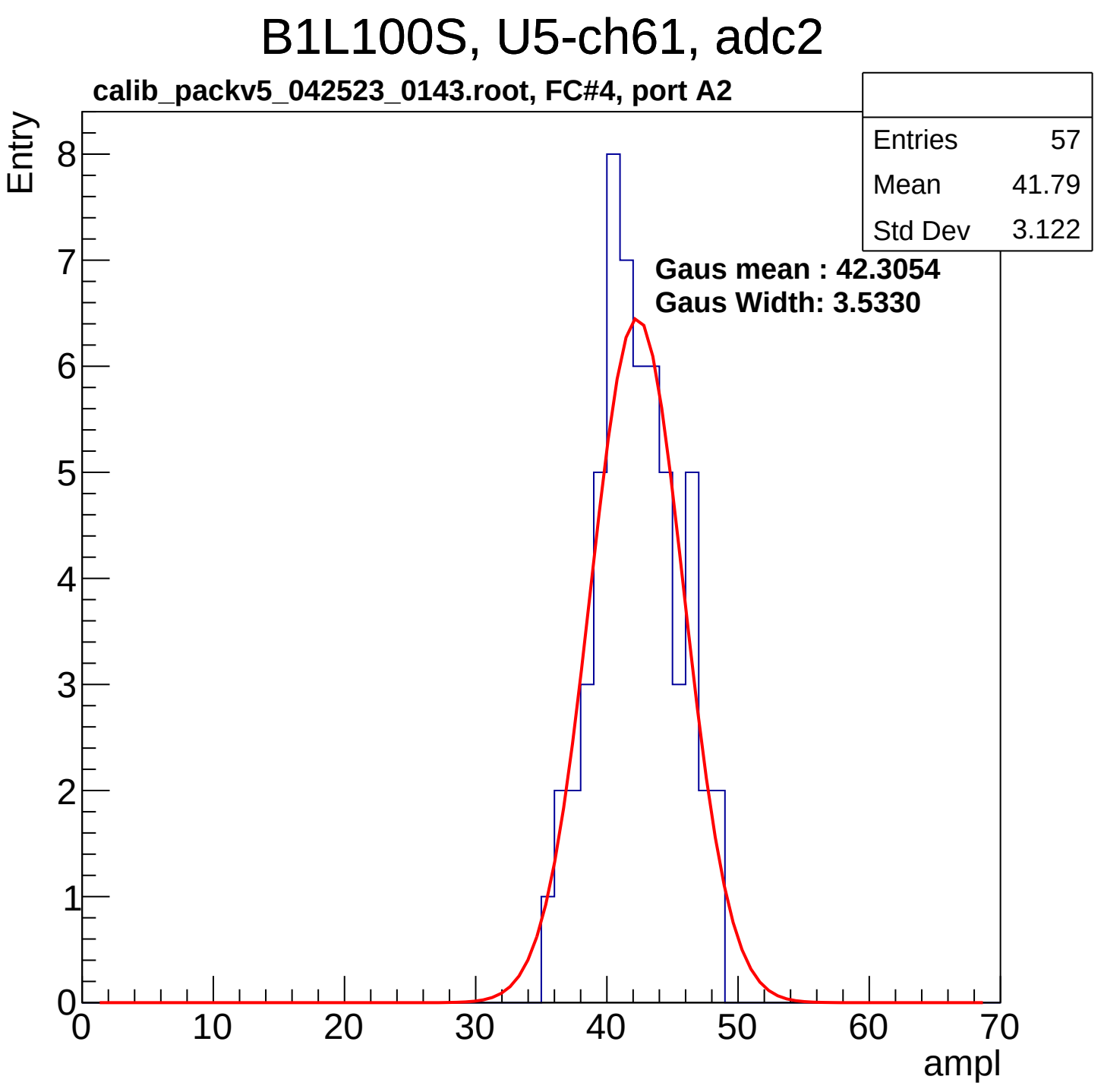
0
10
20
30
40
50
60
70


B1L100S, U5-ch61, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 35.42
Std Dev 3.262
Gaus mean : 35.7603
Gaus Width: 3.9025
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch61, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 41.79
Std Dev 3.122
Gaus mean : 42.3054
Gaus Width: 3.5330
Entry
ampl
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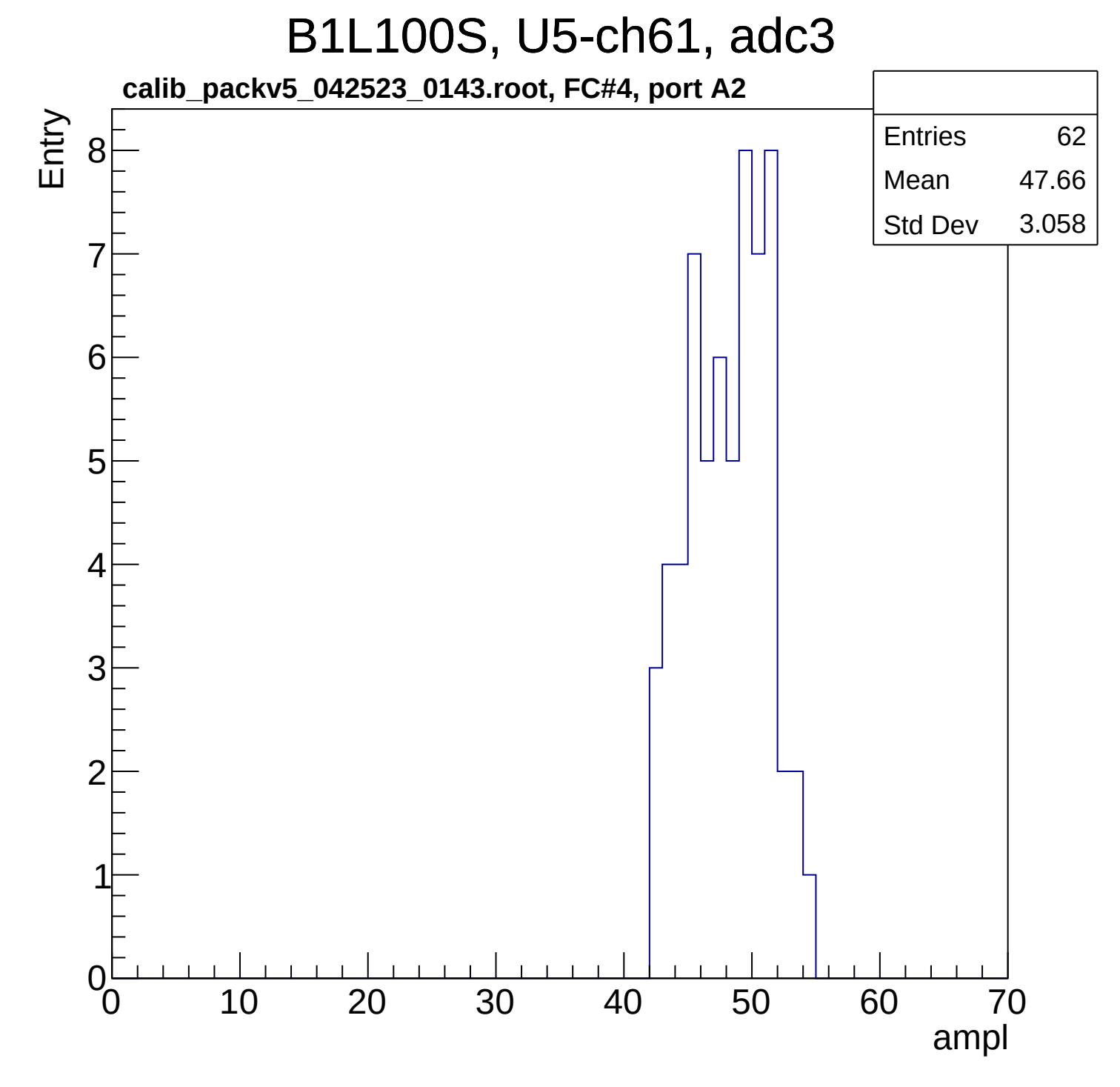
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch61, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 47.66
Std Dev 3.058
Entry
ampl
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1
2
3
4
5
6
7
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0
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60
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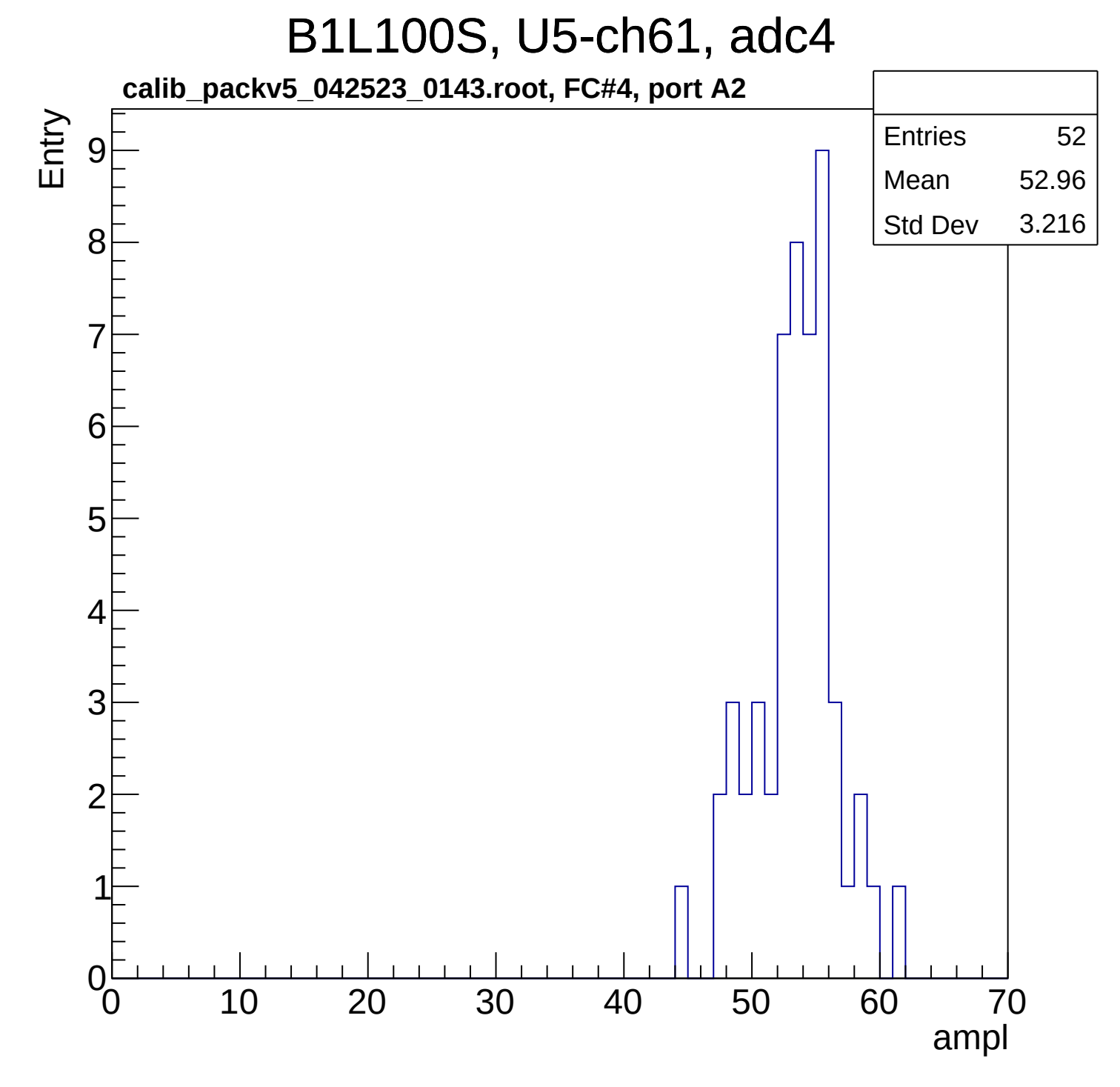
B1L100S, U5-ch61, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 52
Mean 52.96
Std Dev 3.216
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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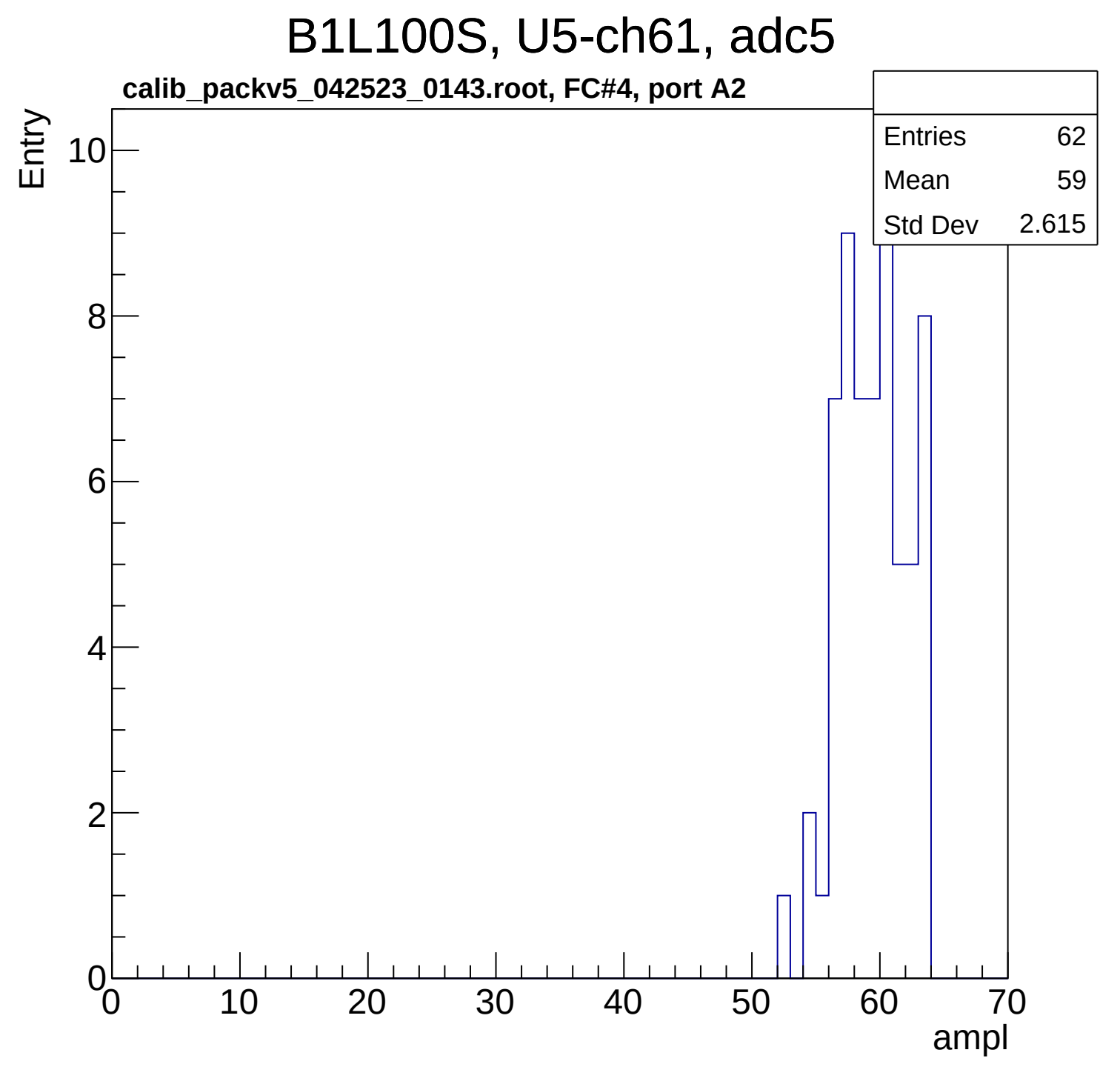
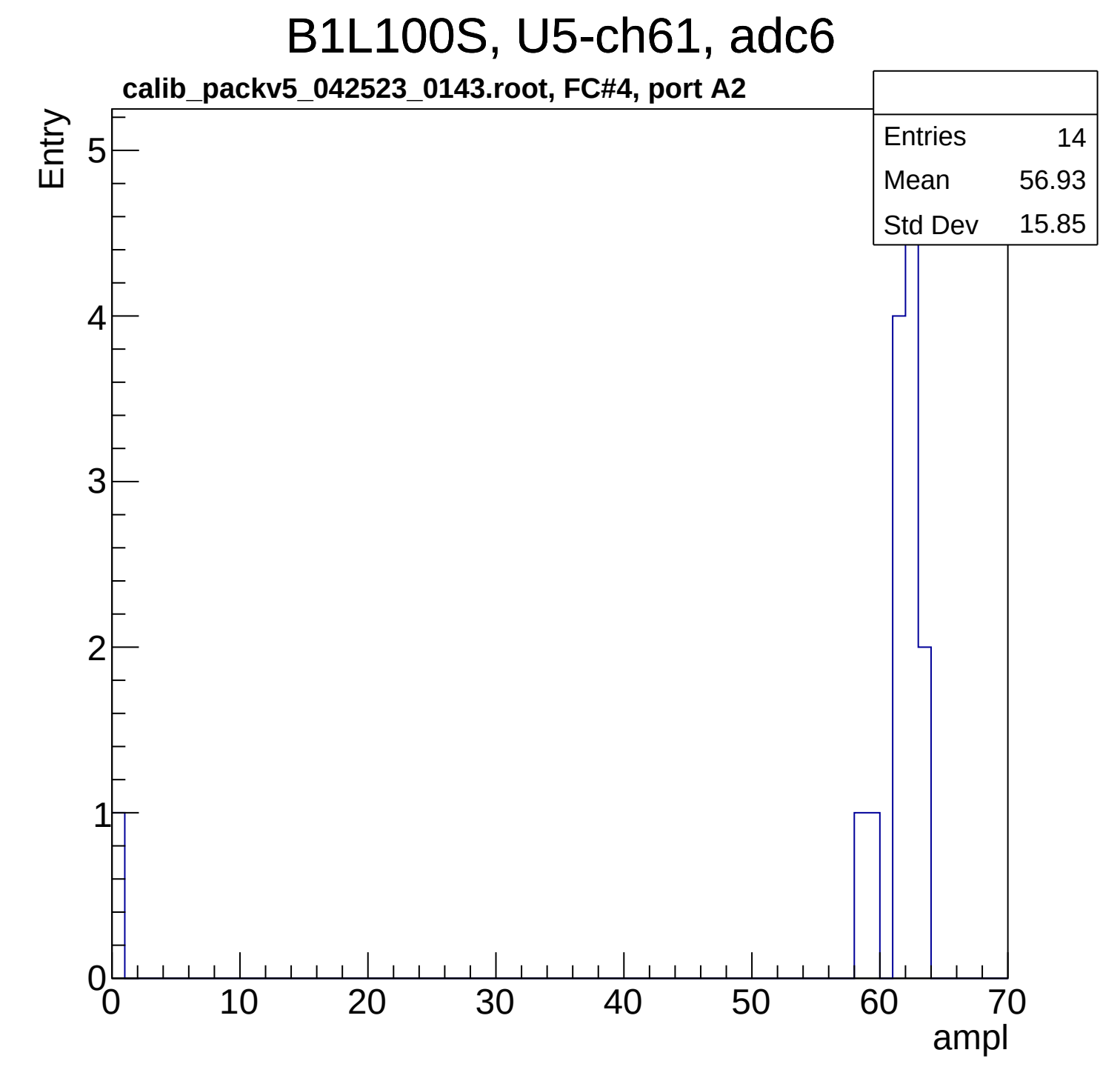
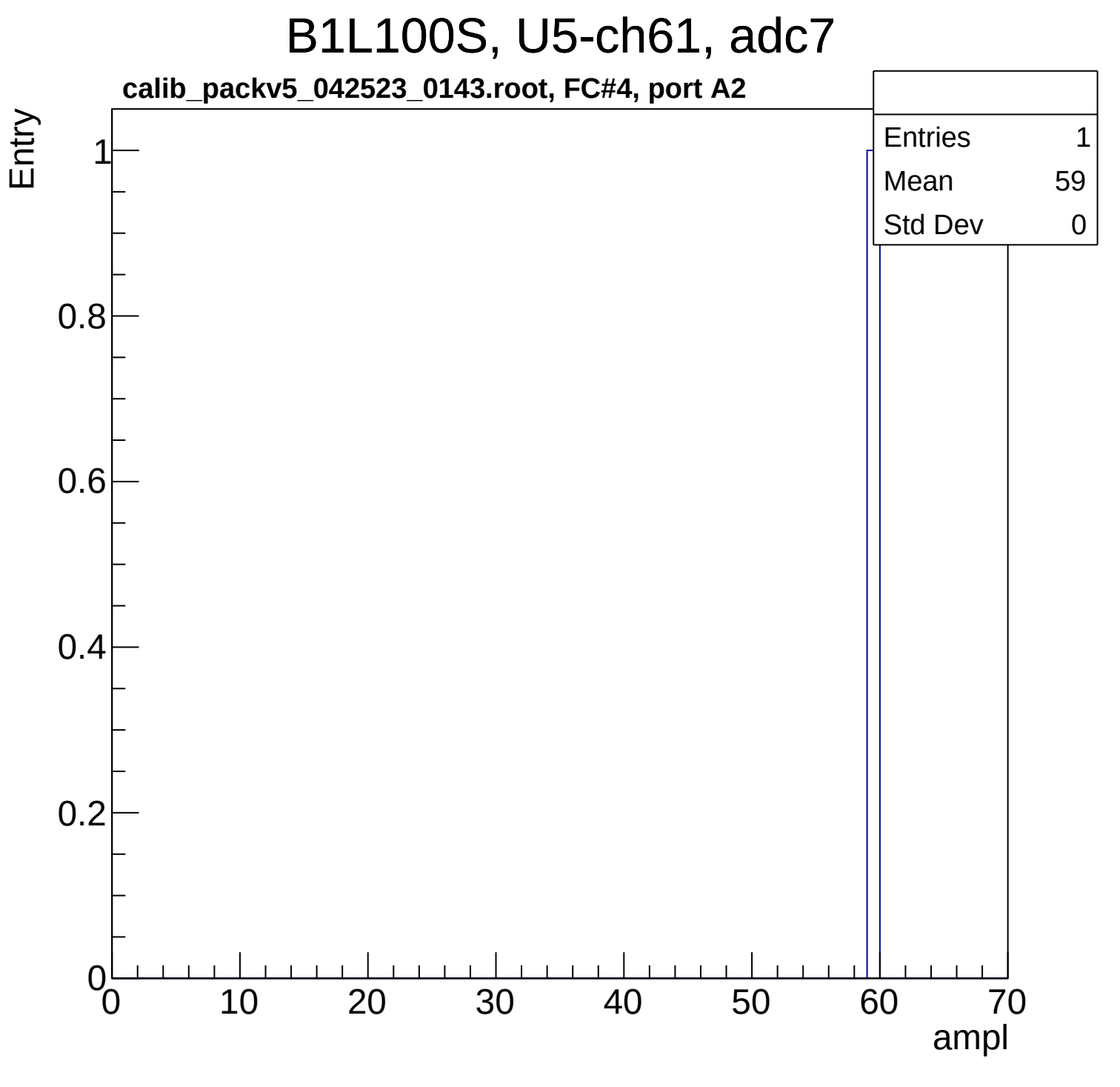
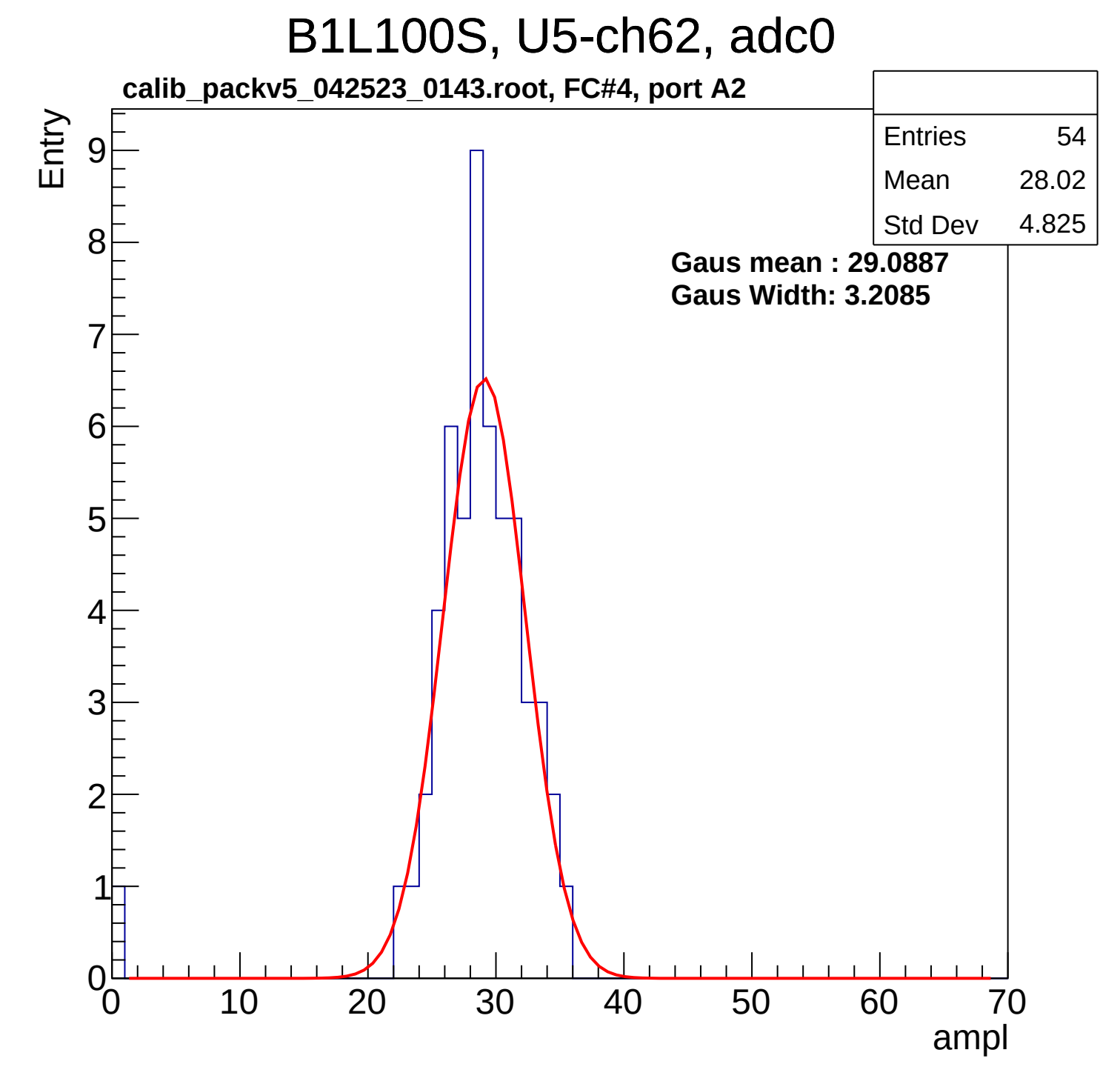

B1L100S, U5-ch61, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 59
Std Dev 2.615
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch61, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 14
Mean 56.93
Std Dev 15.85
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch61, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 59
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch62, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 28.02
Std Dev 4.825
Gaus mean : 29.0887
Gaus Width: 3.2085
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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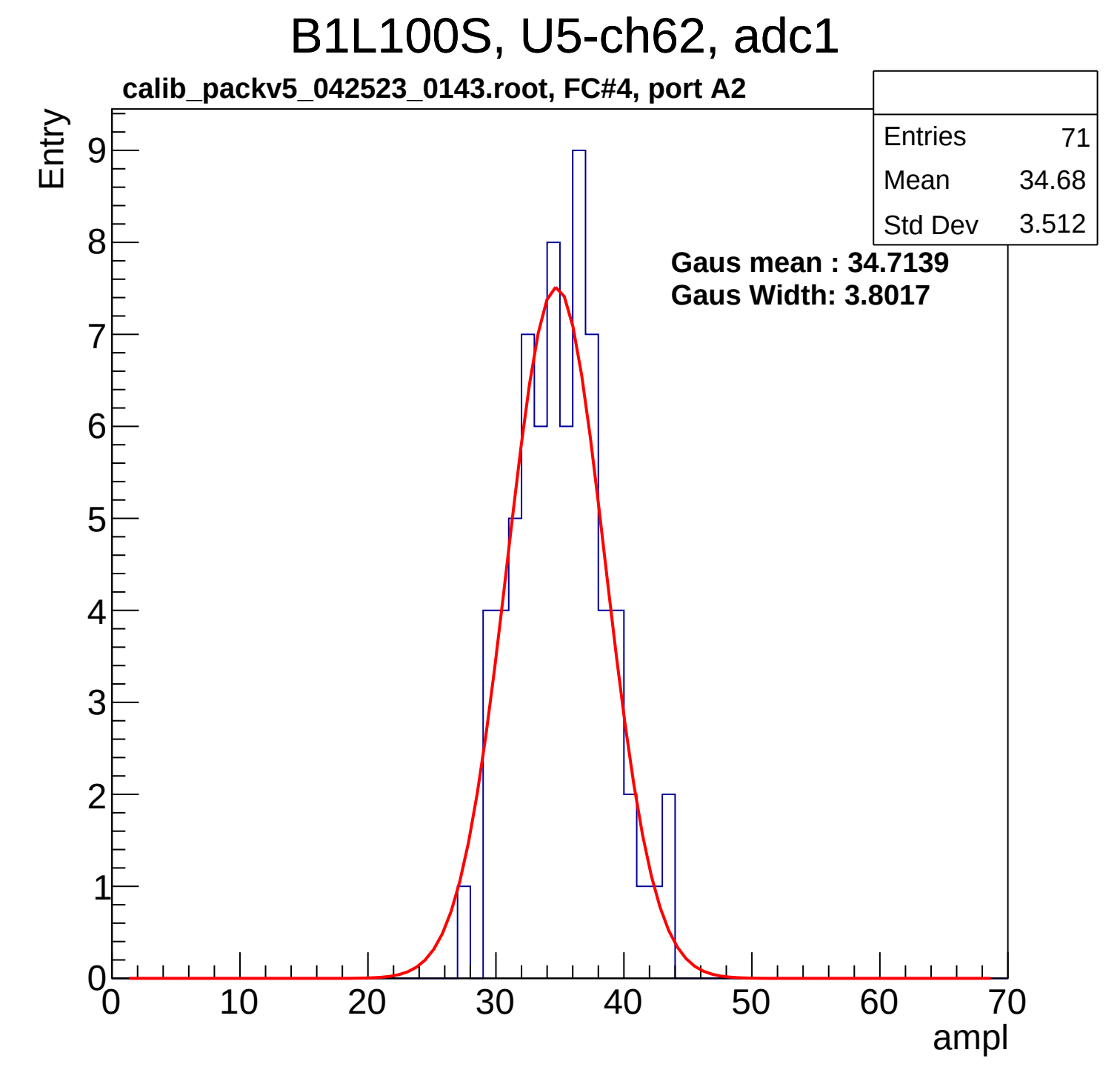
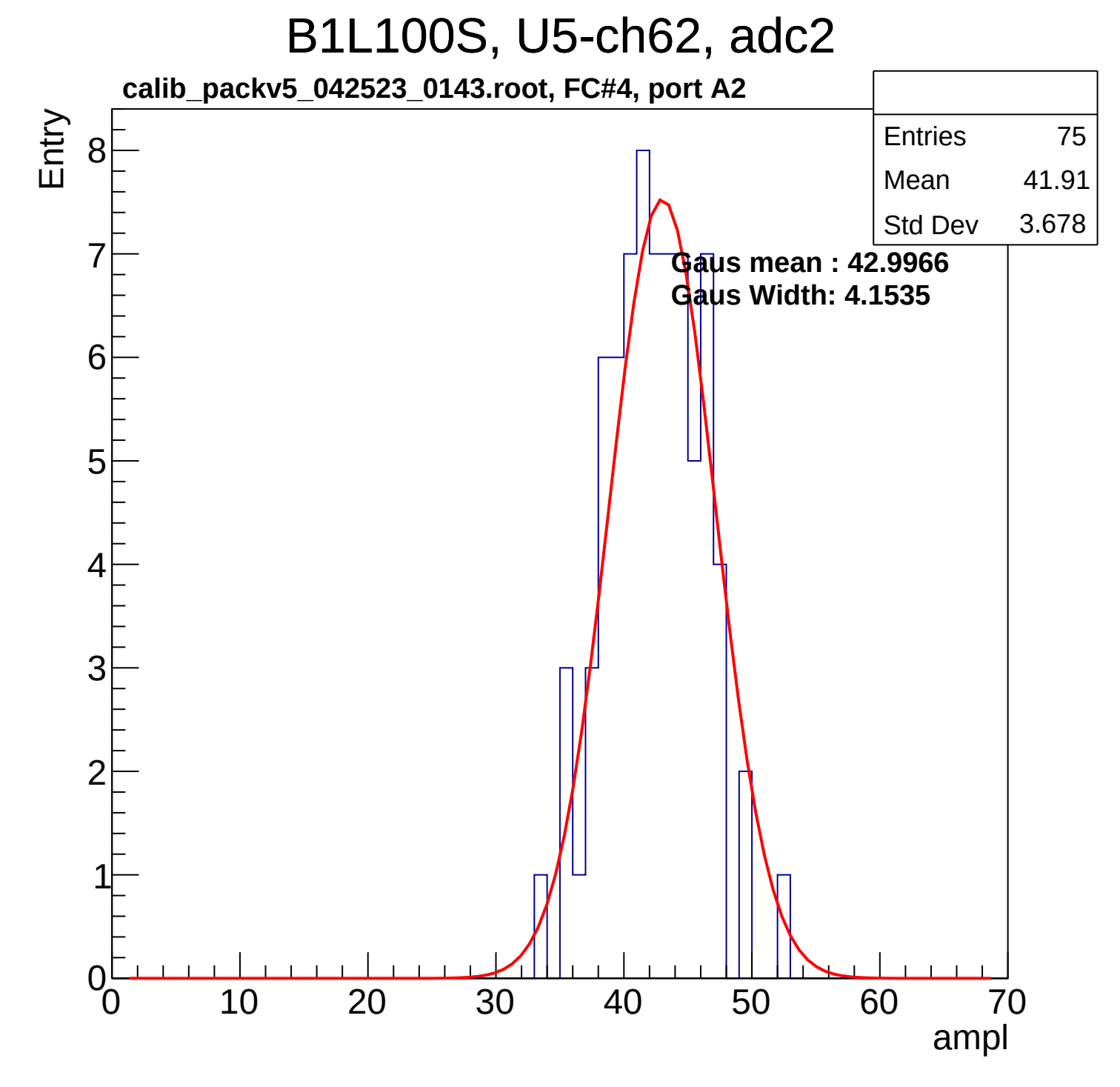
40
50
60
70


B1L100S, U5-ch62, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 34.68
Std Dev 3.512
Gaus mean : 34.7139
Gaus Width: 3.8017
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch62, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 75
Mean 41.91
Std Dev 3.678
Gaus mean : 42.9966
Gaus Width: 4.1535
Entry
ampl
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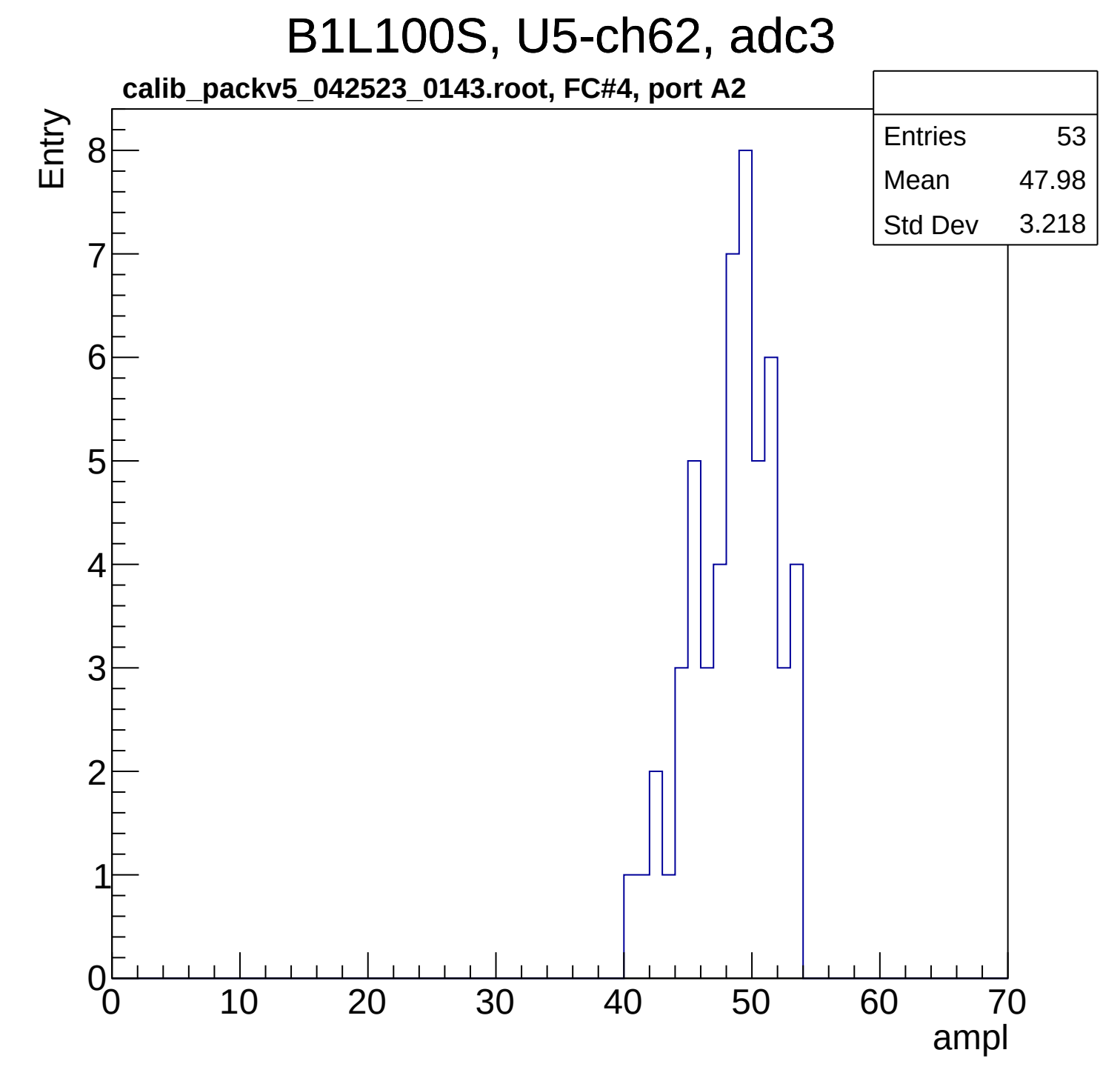
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch62, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 47.98
Std Dev 3.218
Entry
ampl
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1
2
3
4
5
6
7
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0
10
20
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40
50
60
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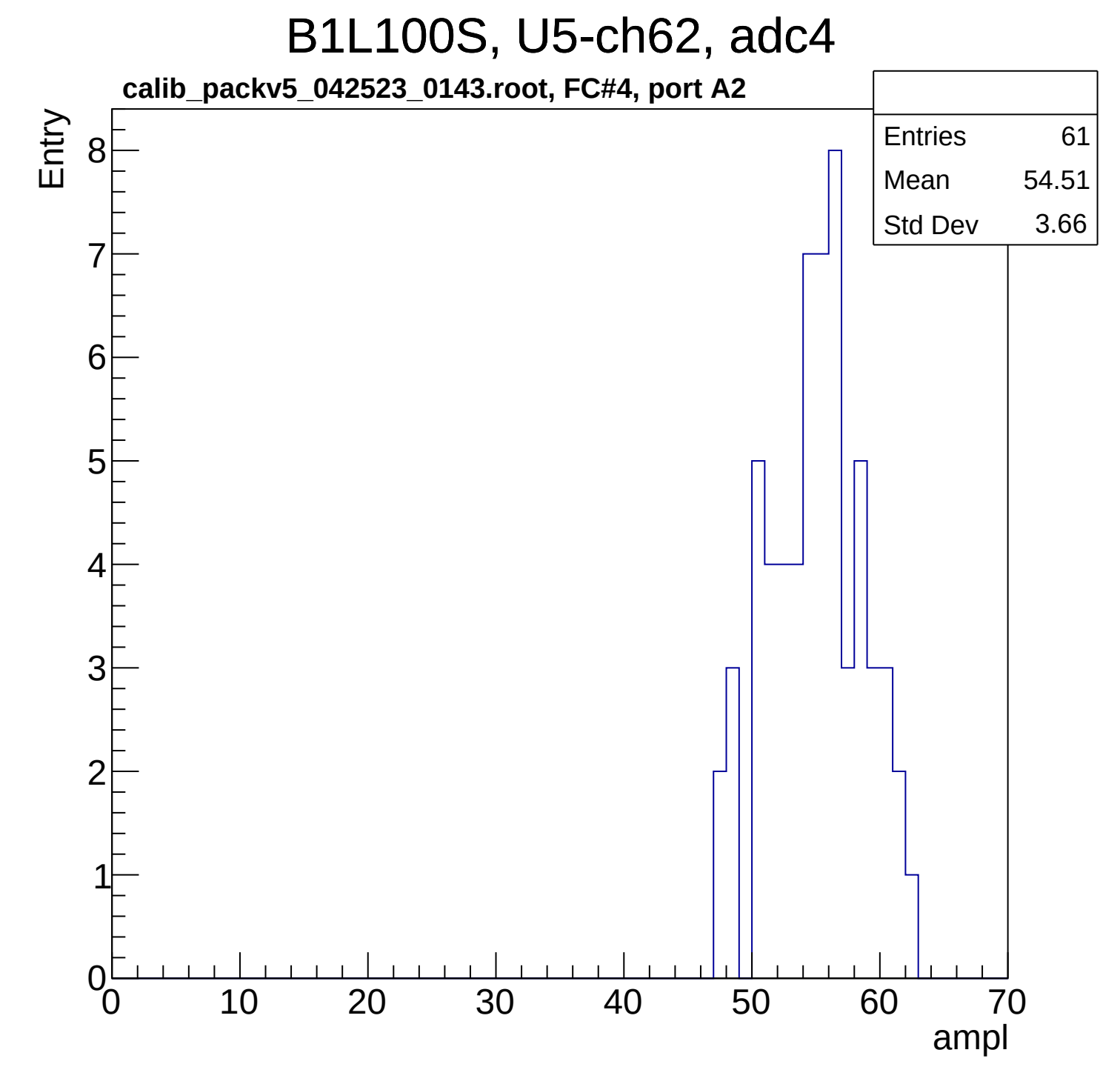
B1L100S, U5-ch62, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 54.51
Std Dev 3.66
Entry
ampl
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2
3
4
5
6
7
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0
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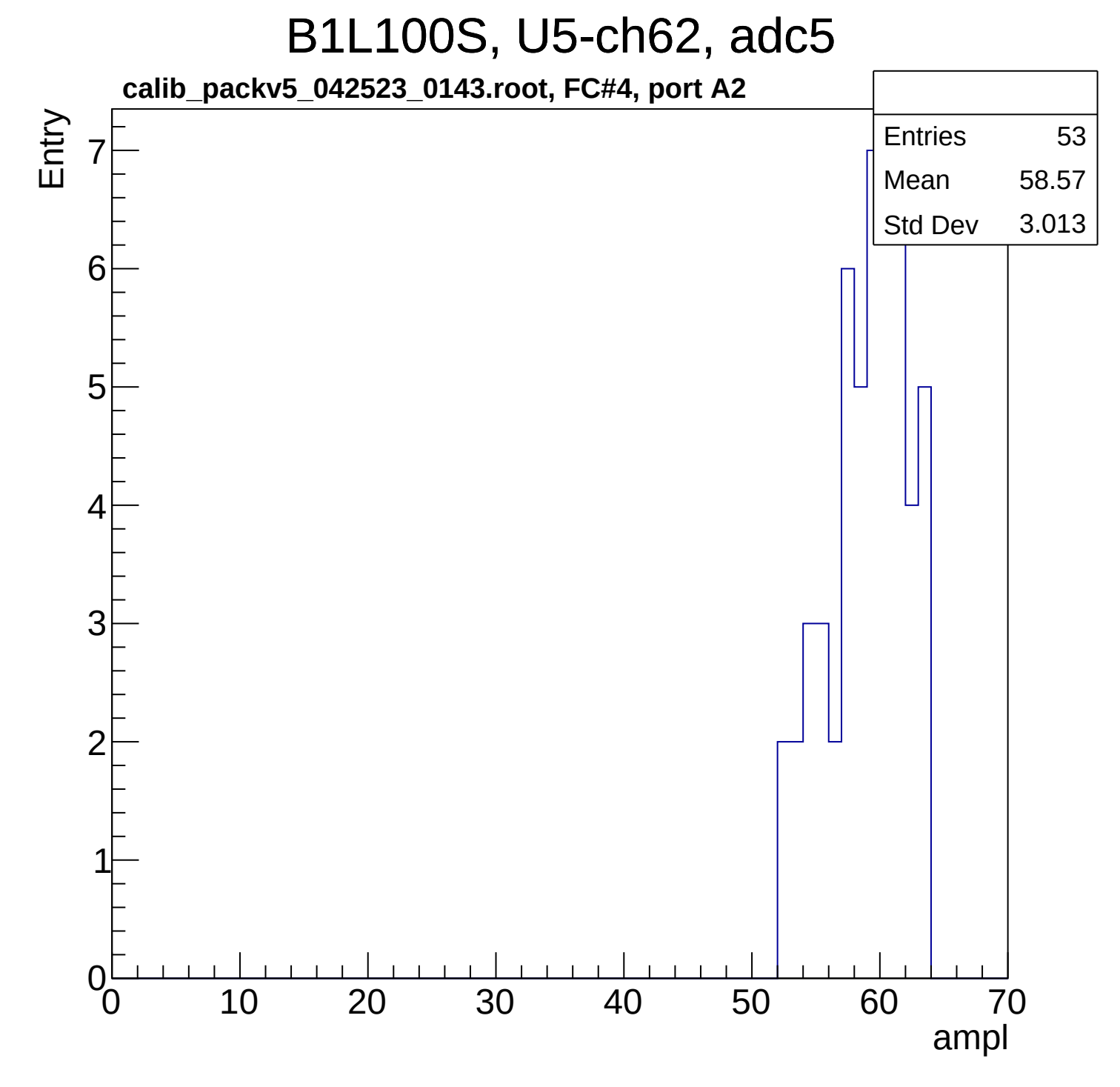
B1L100S, U5-ch62, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 58.57
Std Dev 3.013
Entry
ampl
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1
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4
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6
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0
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20
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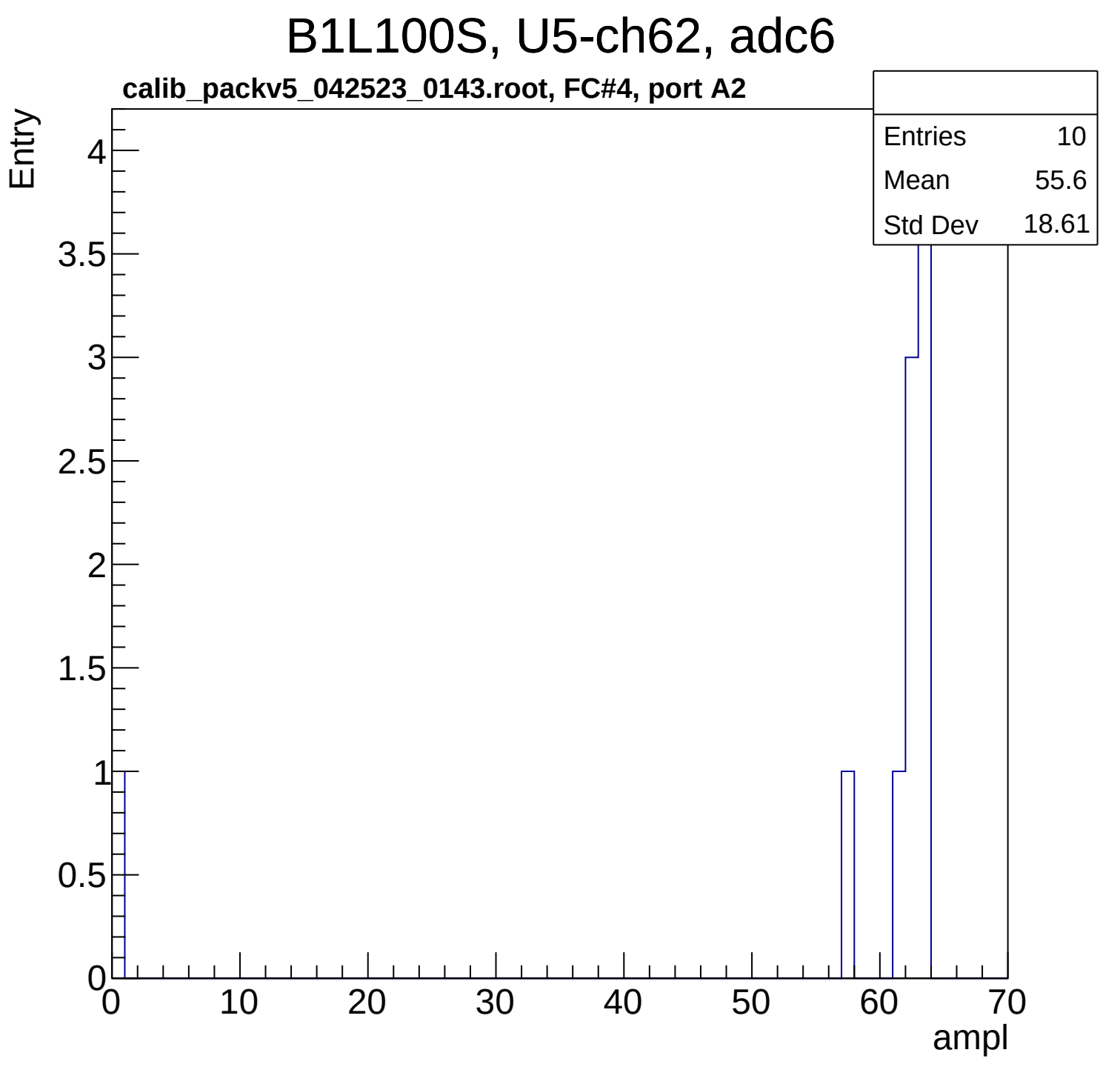
40
50
60
70


B1L100S, U5-ch62, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 10
Mean 55.6
Std Dev 18.61
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
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20
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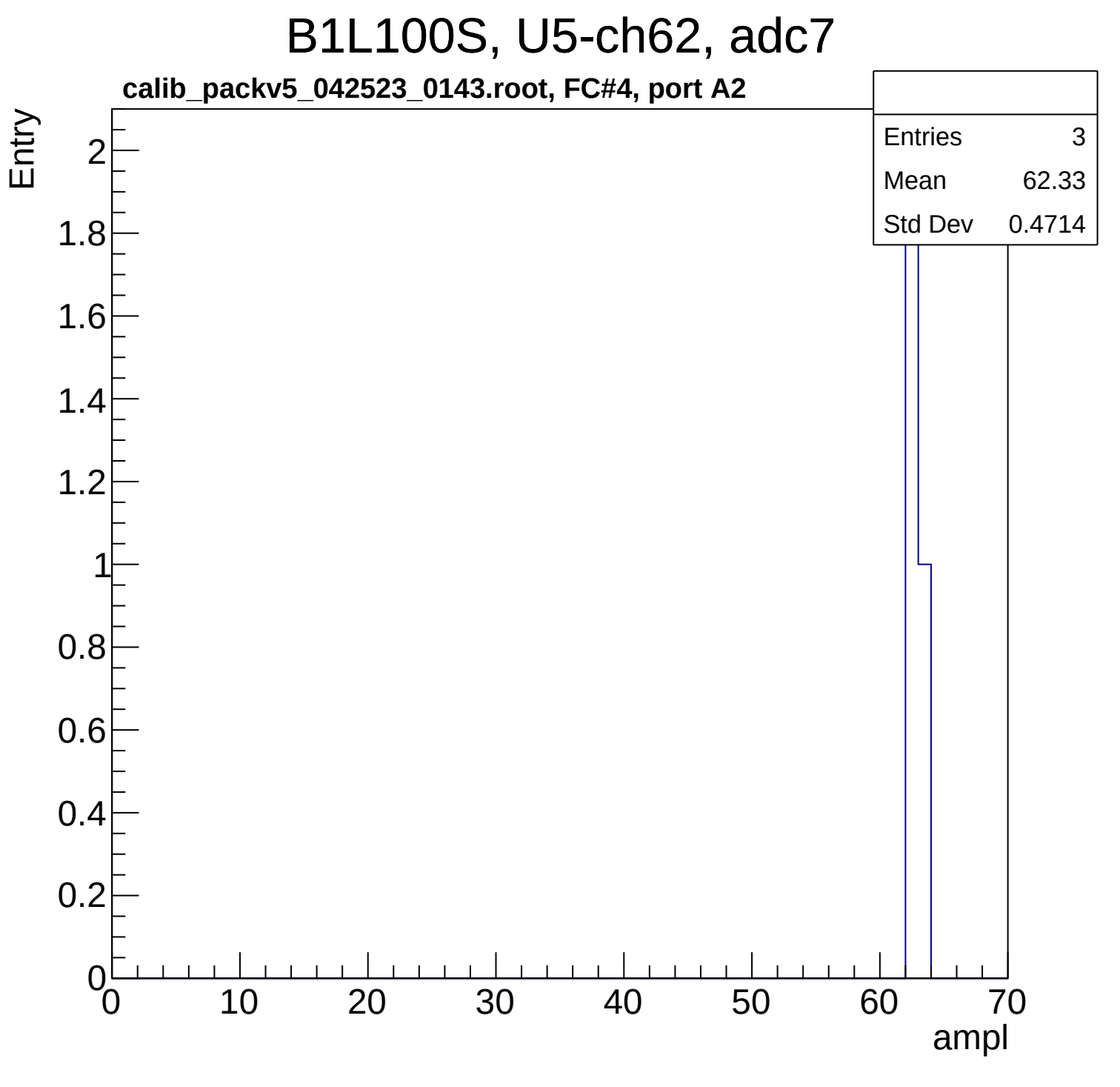
40
50
60
70


B1L100S, U5-ch62, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 62.33
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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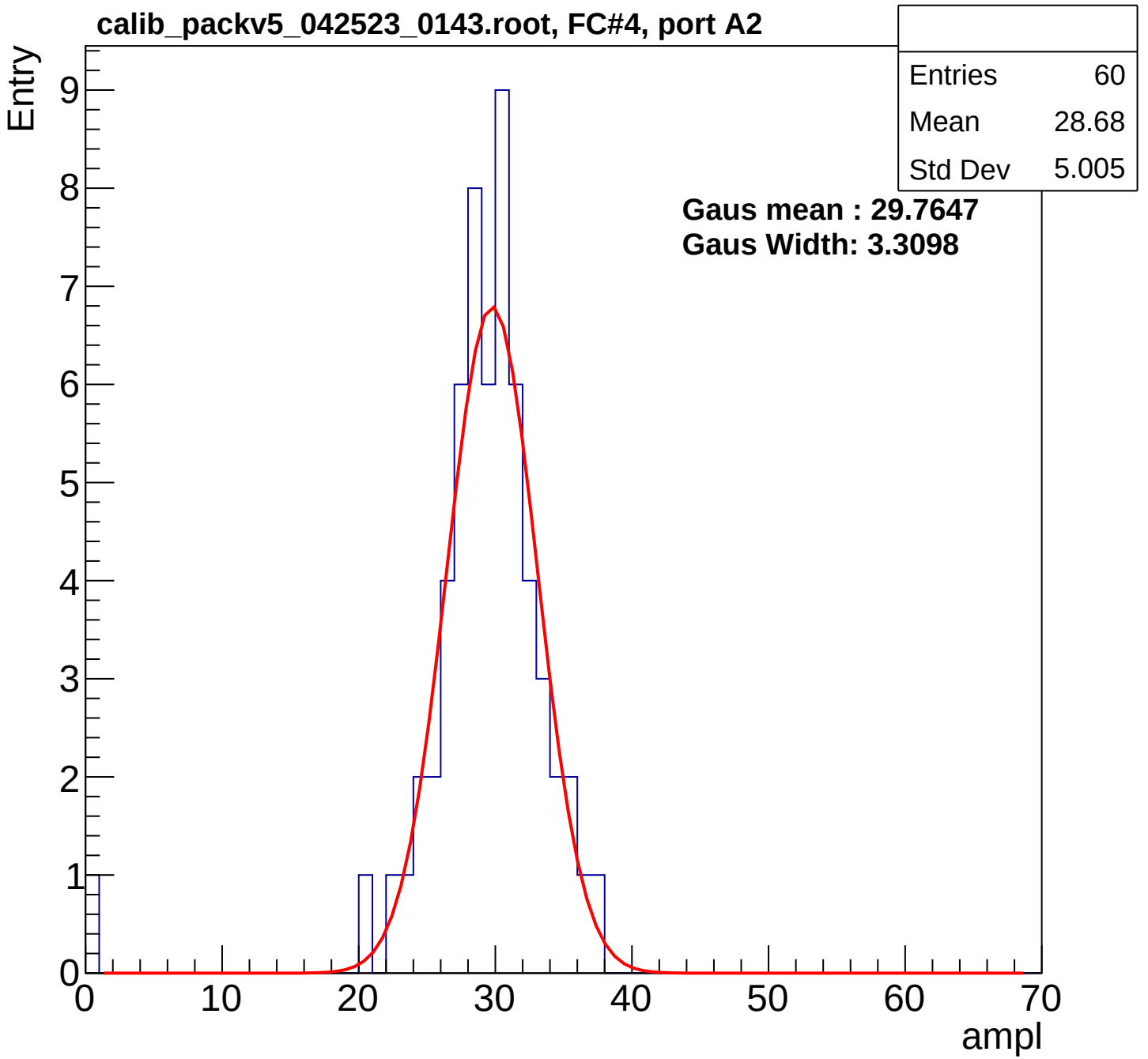
40
50
60
70


B1L100S, U5-ch63, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 28.68
Std Dev 5.005
Gaus mean : 29.7647
Gaus Width: 3.3098
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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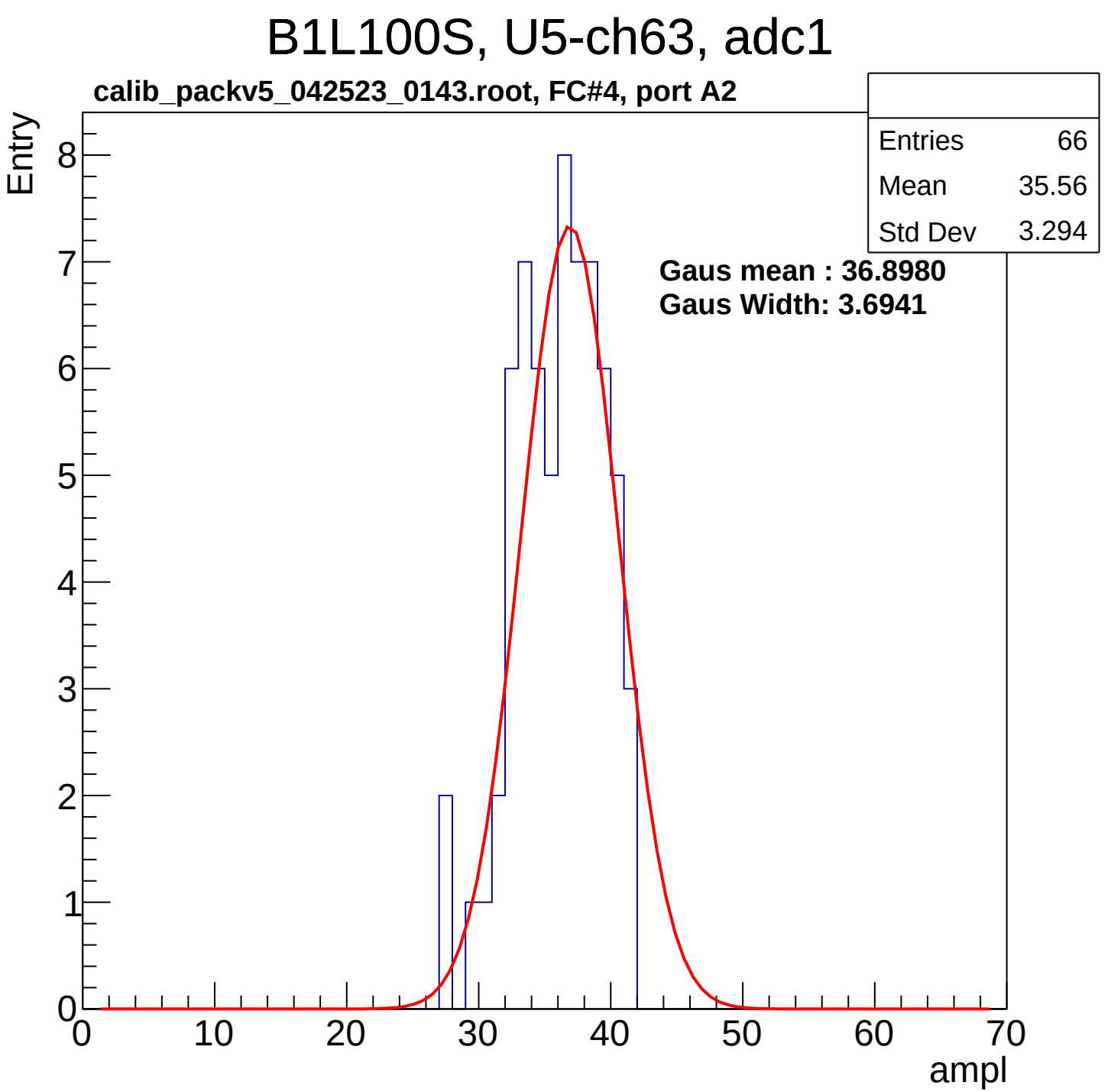
B1L100S, U5-ch63, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 35.56
Std Dev 3.294
Gaus mean : 36.8980
Gaus Width: 3.6941
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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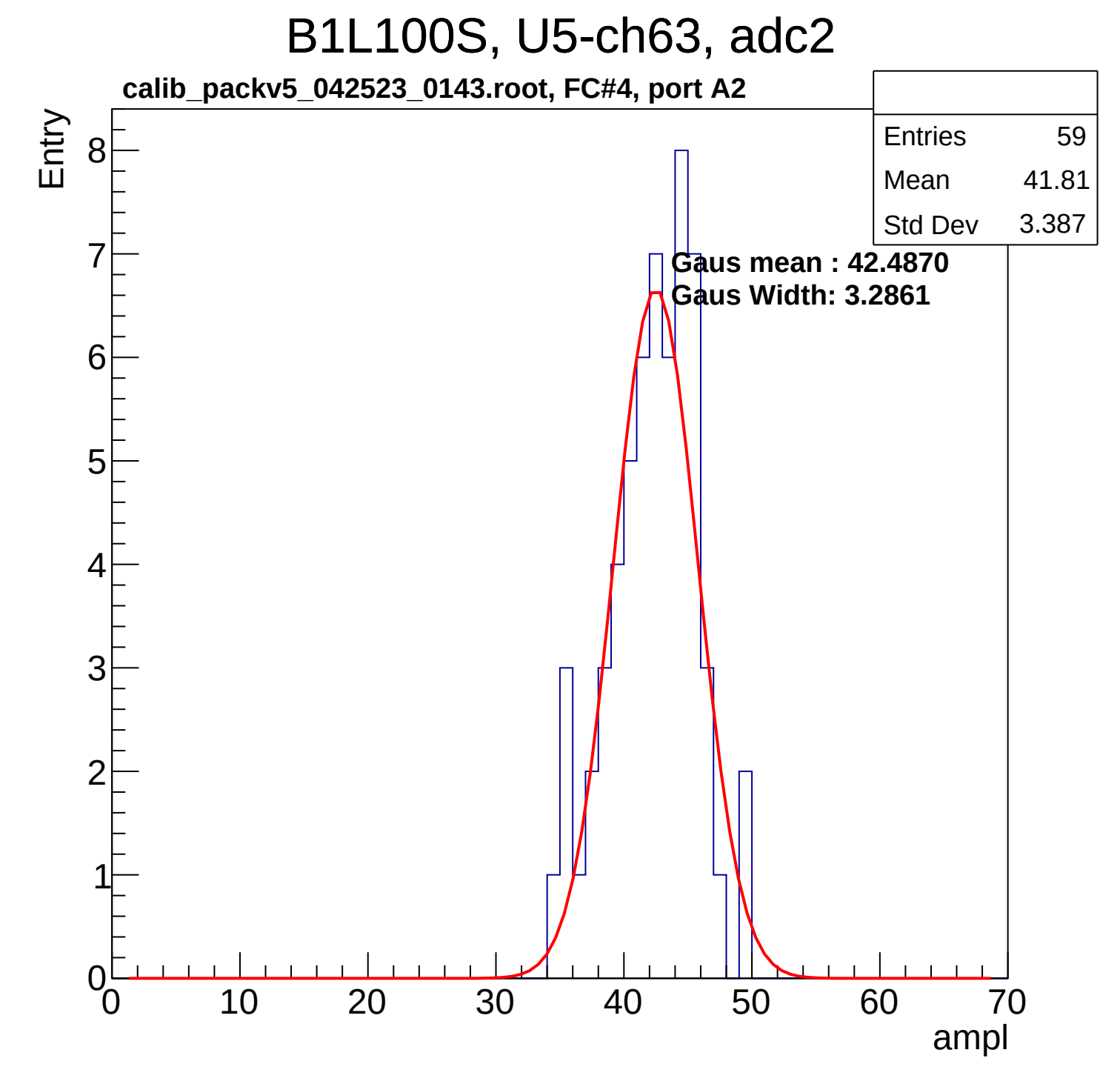
B1L100S, U5-ch63, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 41.81
Std Dev 3.387
Gaus mean : 42.4870
Gaus Width: 3.2861
Entry
ampl
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1
2
3
4
5
6
7
8
0
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50
60
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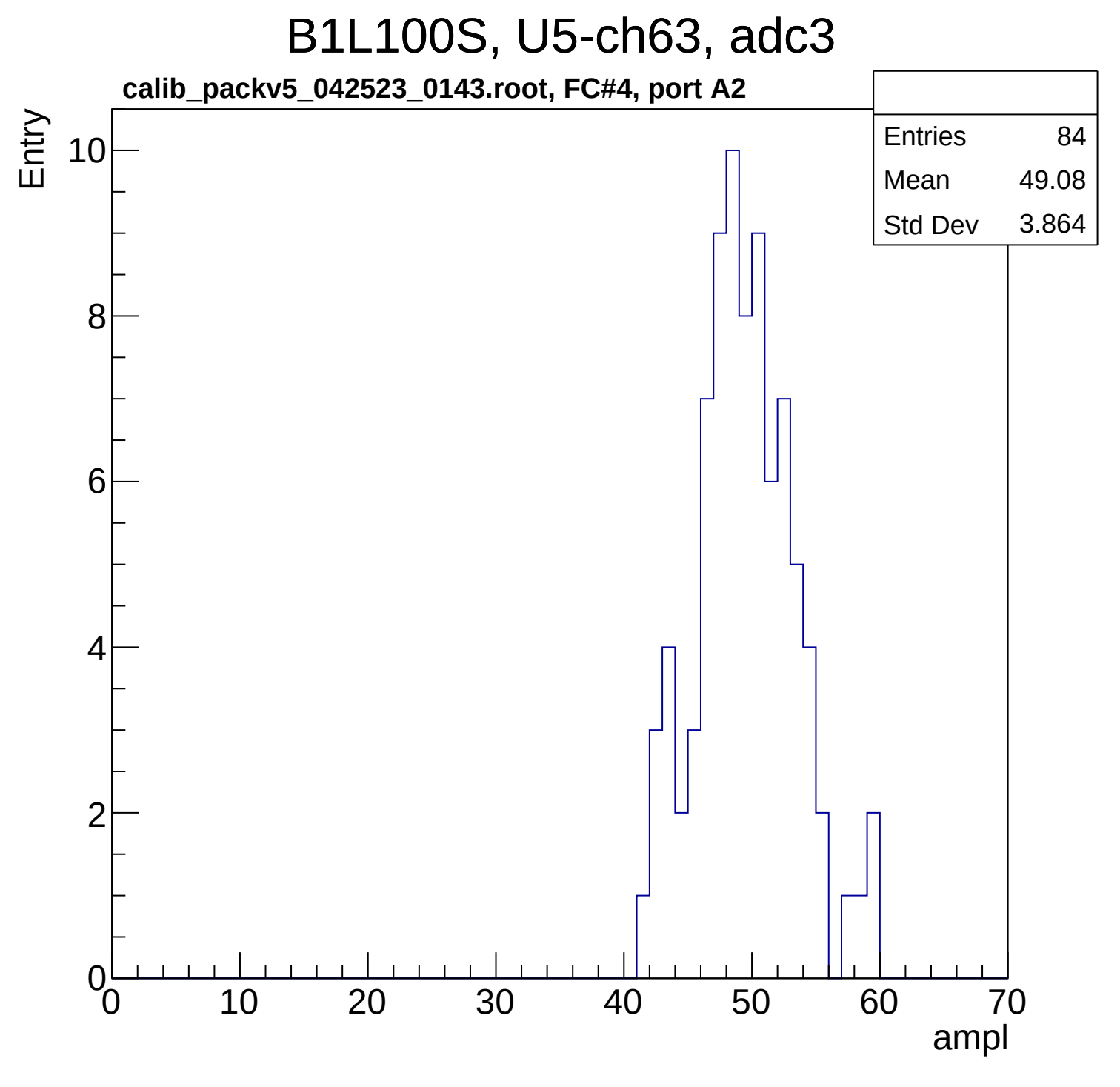
B1L100S, U5-ch63, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 84
Mean 49.08
Std Dev 3.864
Entry
ampl
0
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40
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60
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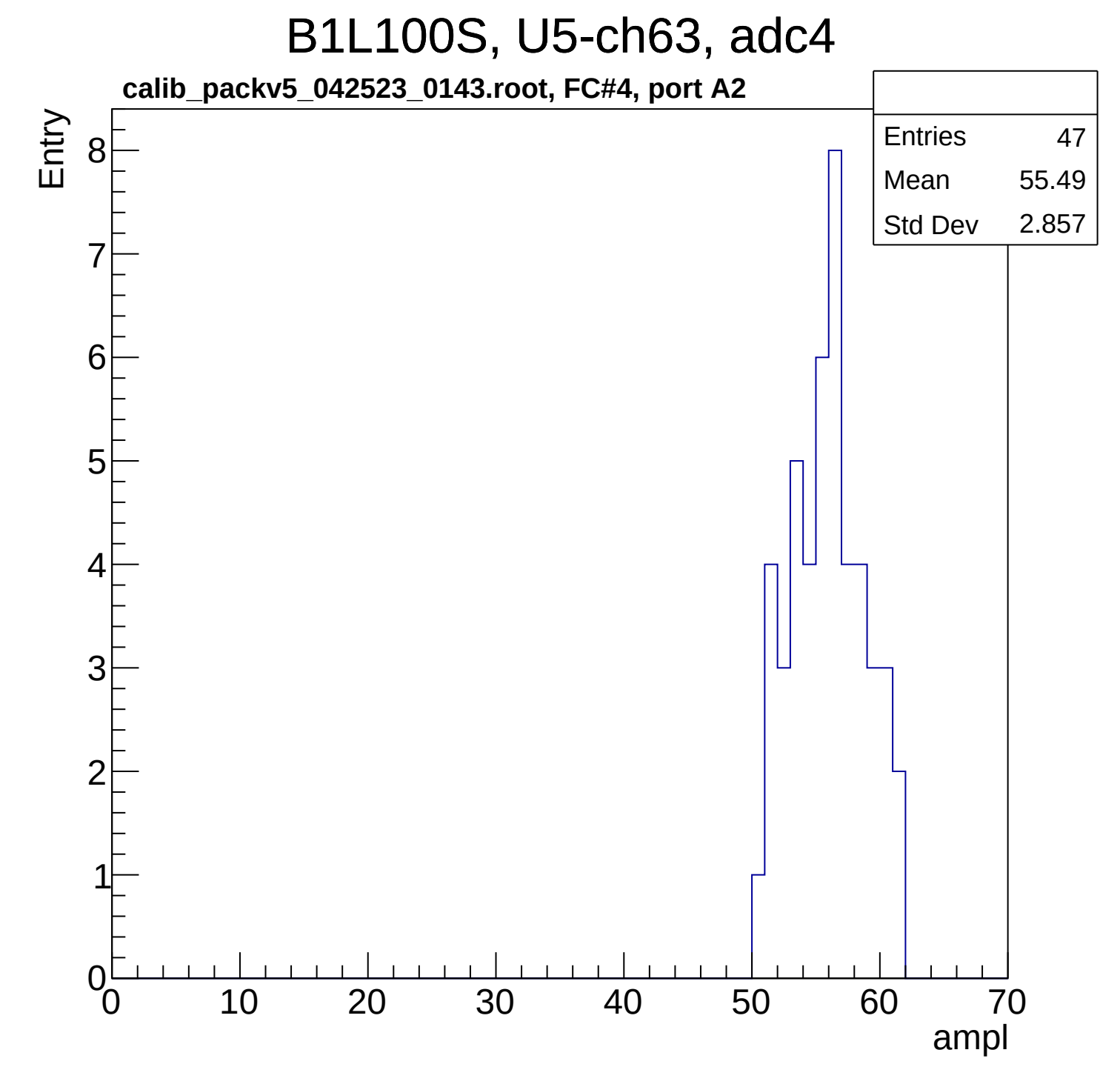
B1L100S, U5-ch63, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 47
Mean 55.49
Std Dev 2.857
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
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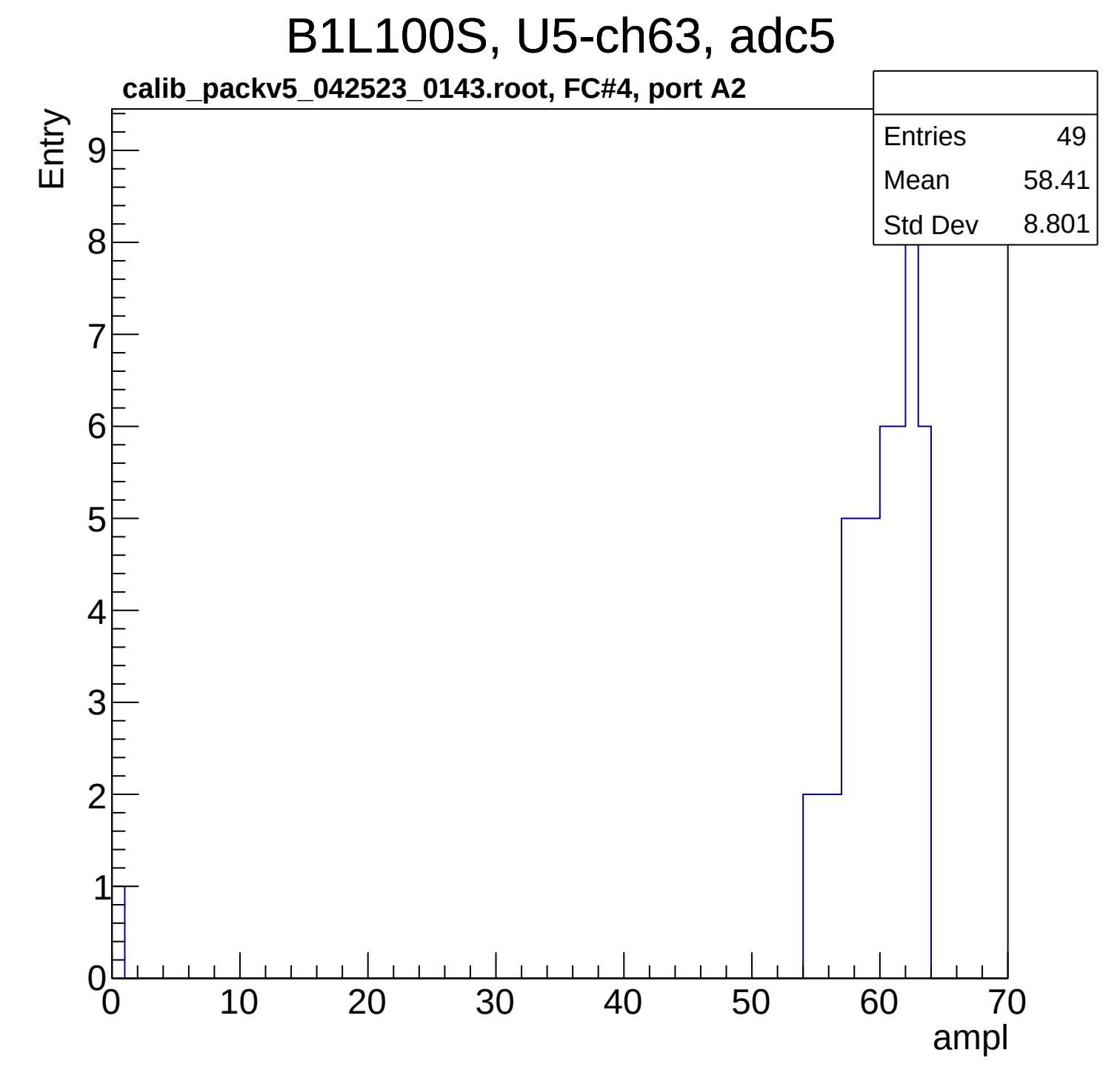
B1L100S, U5-ch63, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 49
Mean 58.41
Std Dev 8.801
Entry
ampl
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4
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6
7
8
9
0
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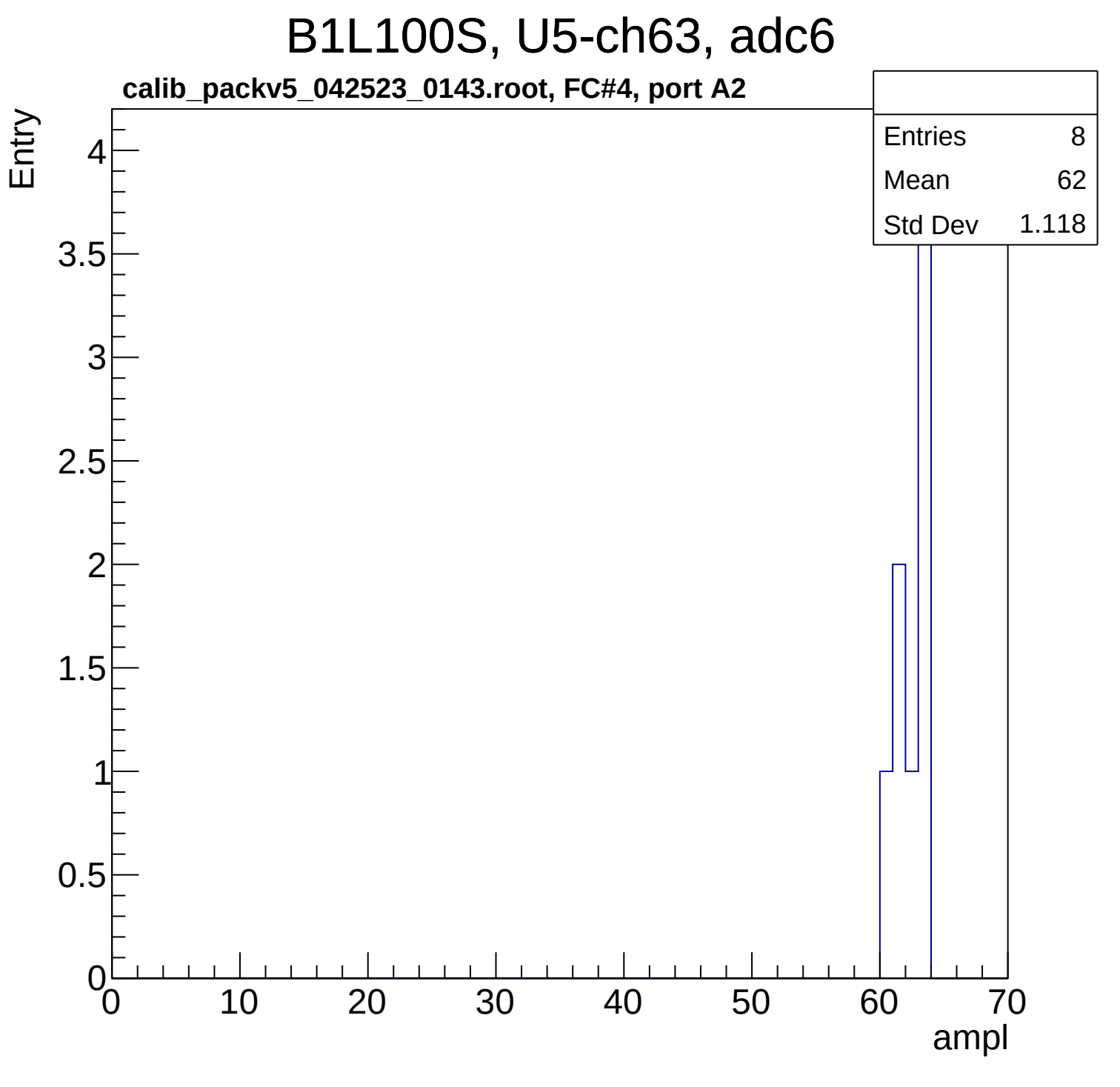
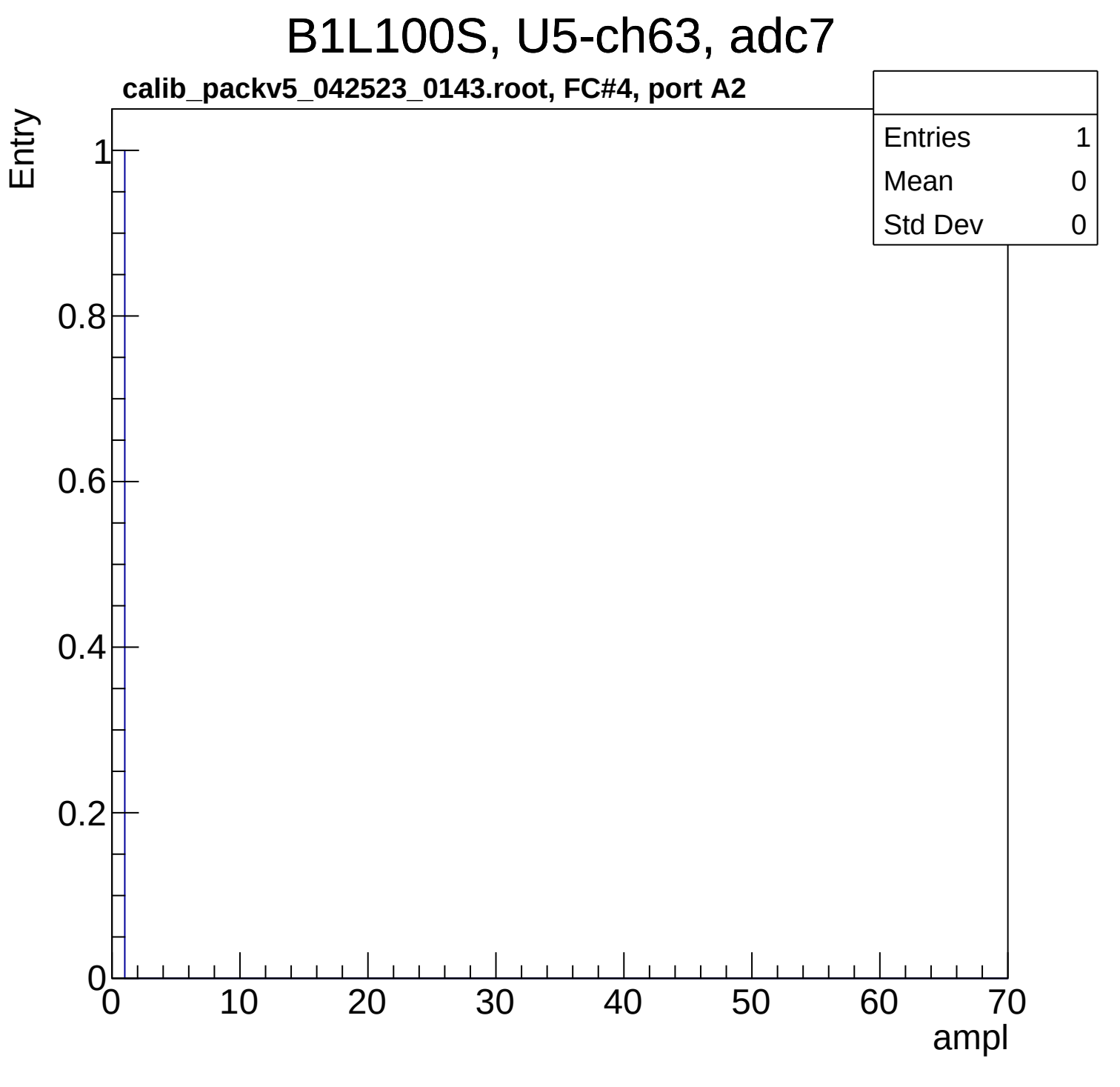
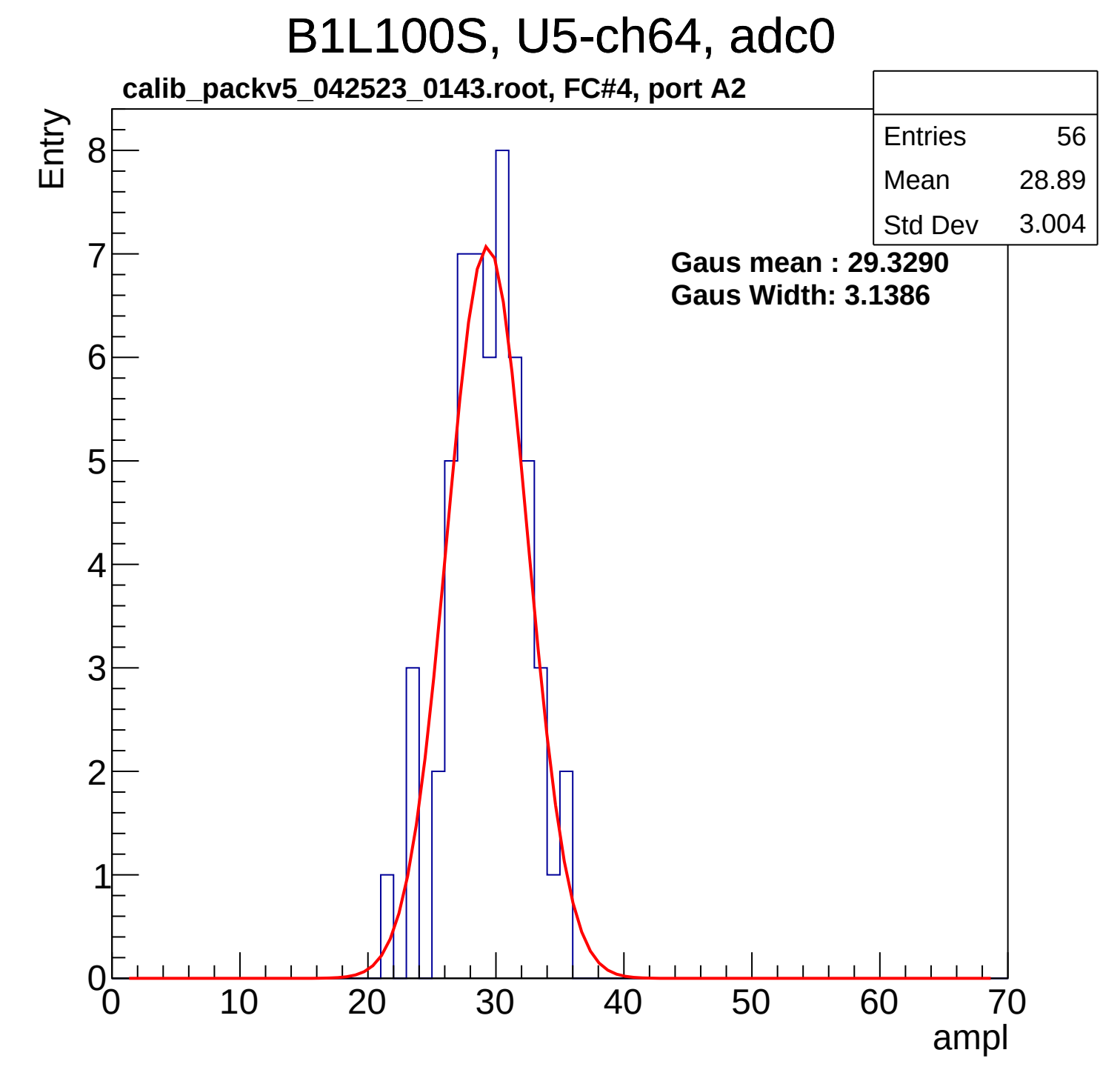
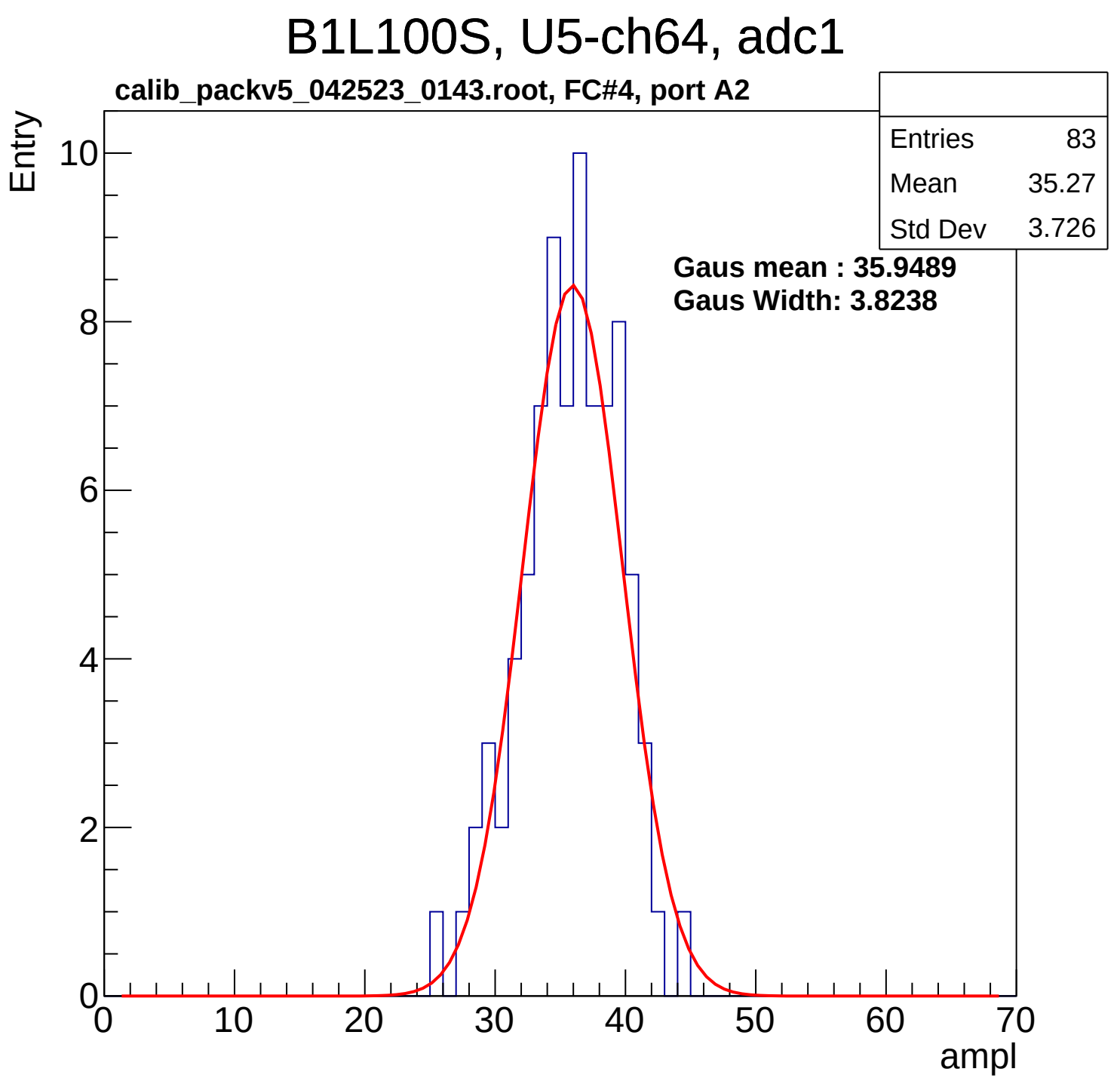
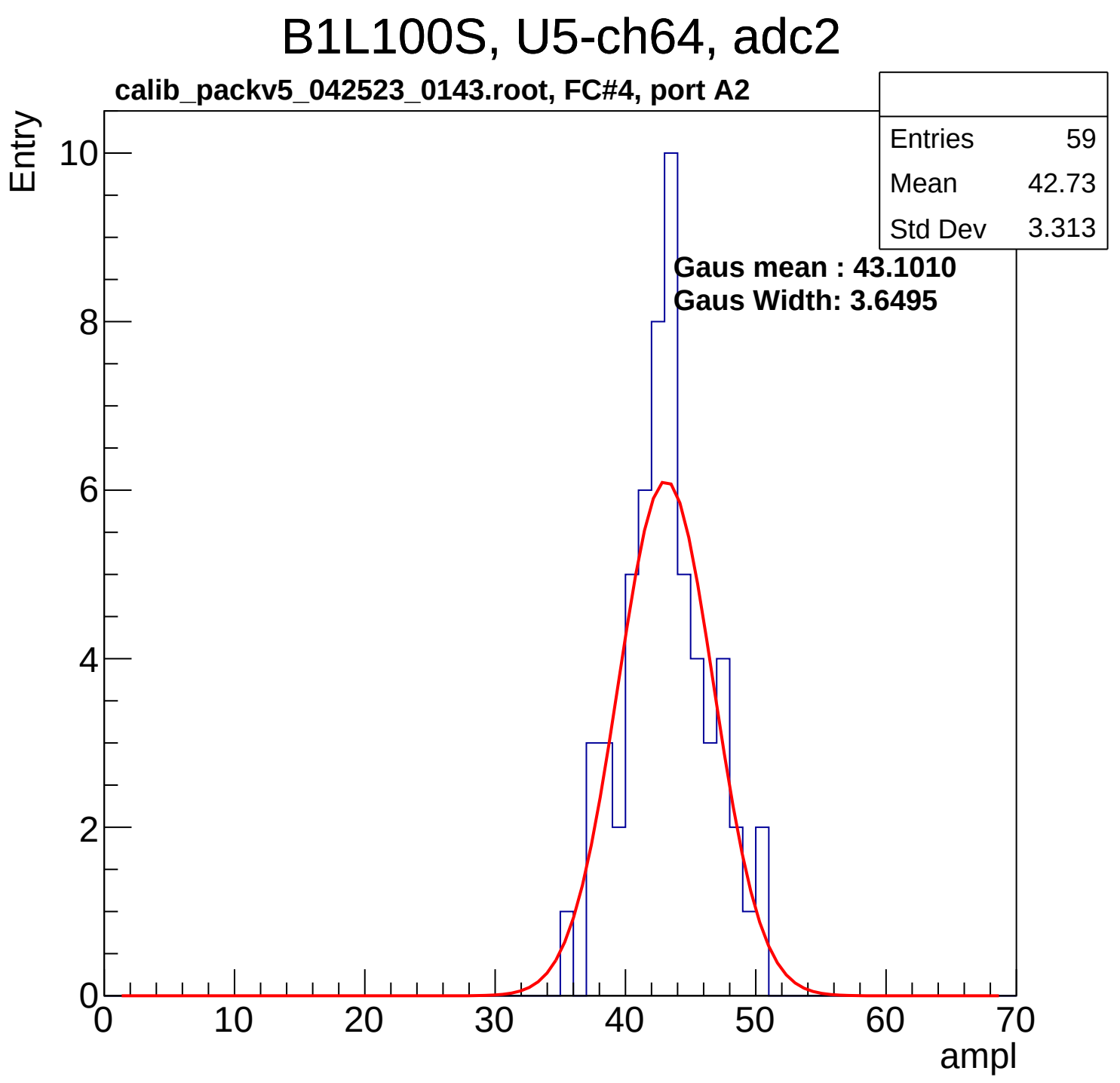
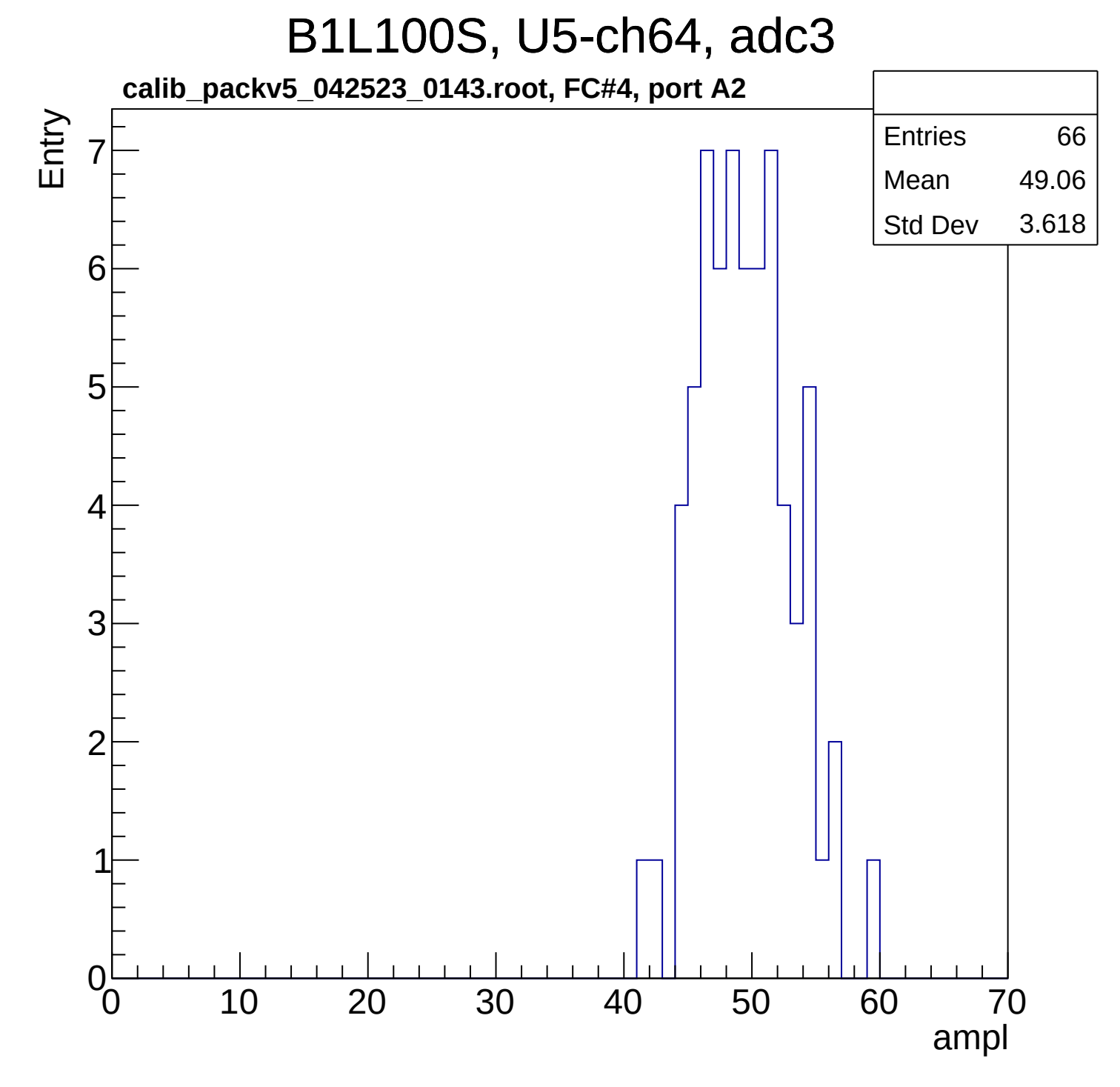

B1L100S, U5-ch63, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 8
Mean 62
Std Dev 1.118
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L100S, U5-ch63, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch64, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 28.89
Std Dev 3.004
Gaus mean : 29.3290
Gaus Width: 3.1386
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch64, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 83
Mean 35.27
Std Dev 3.726
Gaus mean : 35.9489
Gaus Width: 3.8238
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch64, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 42.73
Std Dev 3.313
Gaus mean : 43.1010
Gaus Width: 3.6495
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch64, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 49.06
Std Dev 3.618
Entry
ampl
0
1
2
3
4
5
6
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0
10
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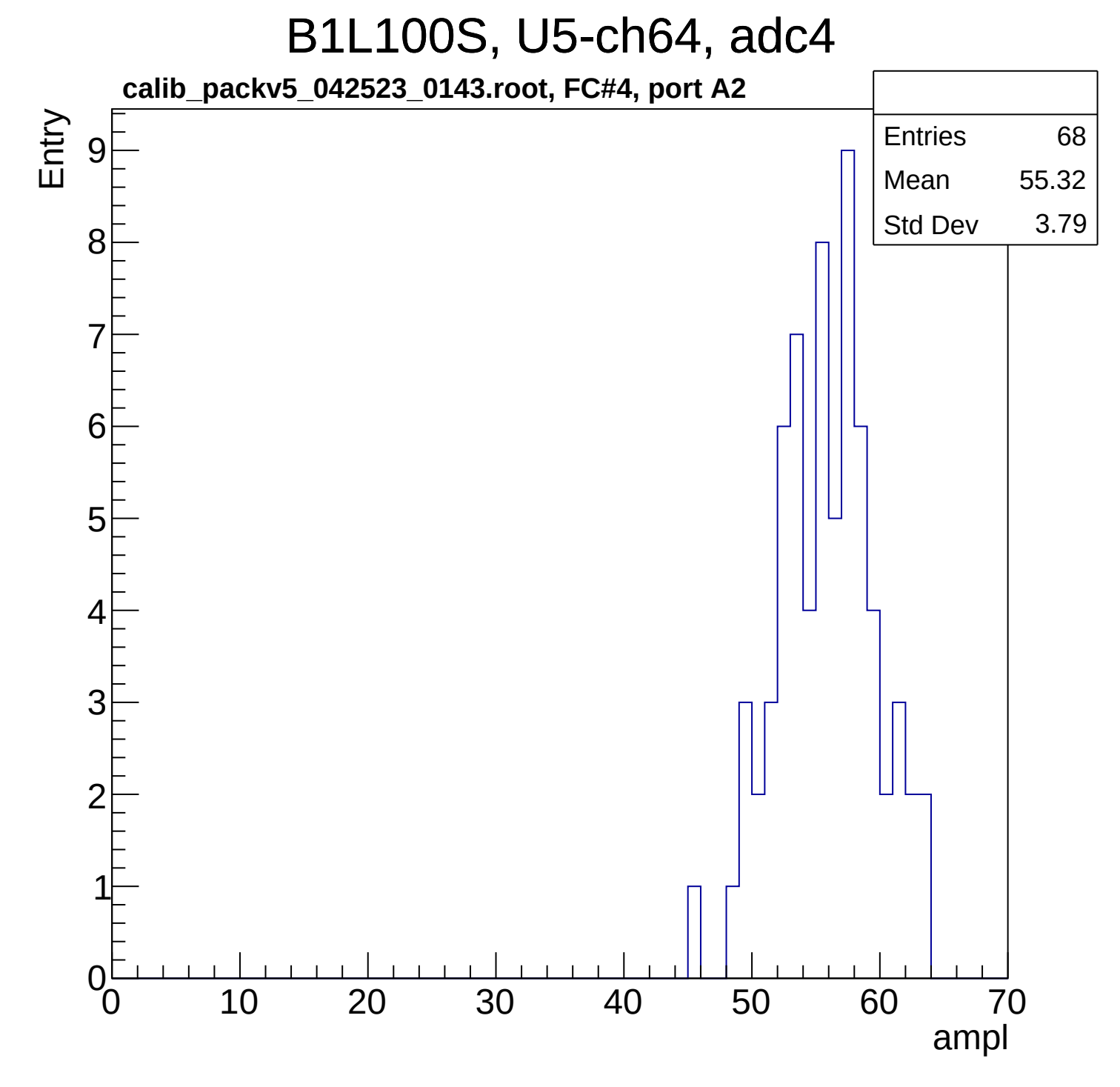
40
50
60
70


B1L100S, U5-ch64, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 55.32
Std Dev 3.79
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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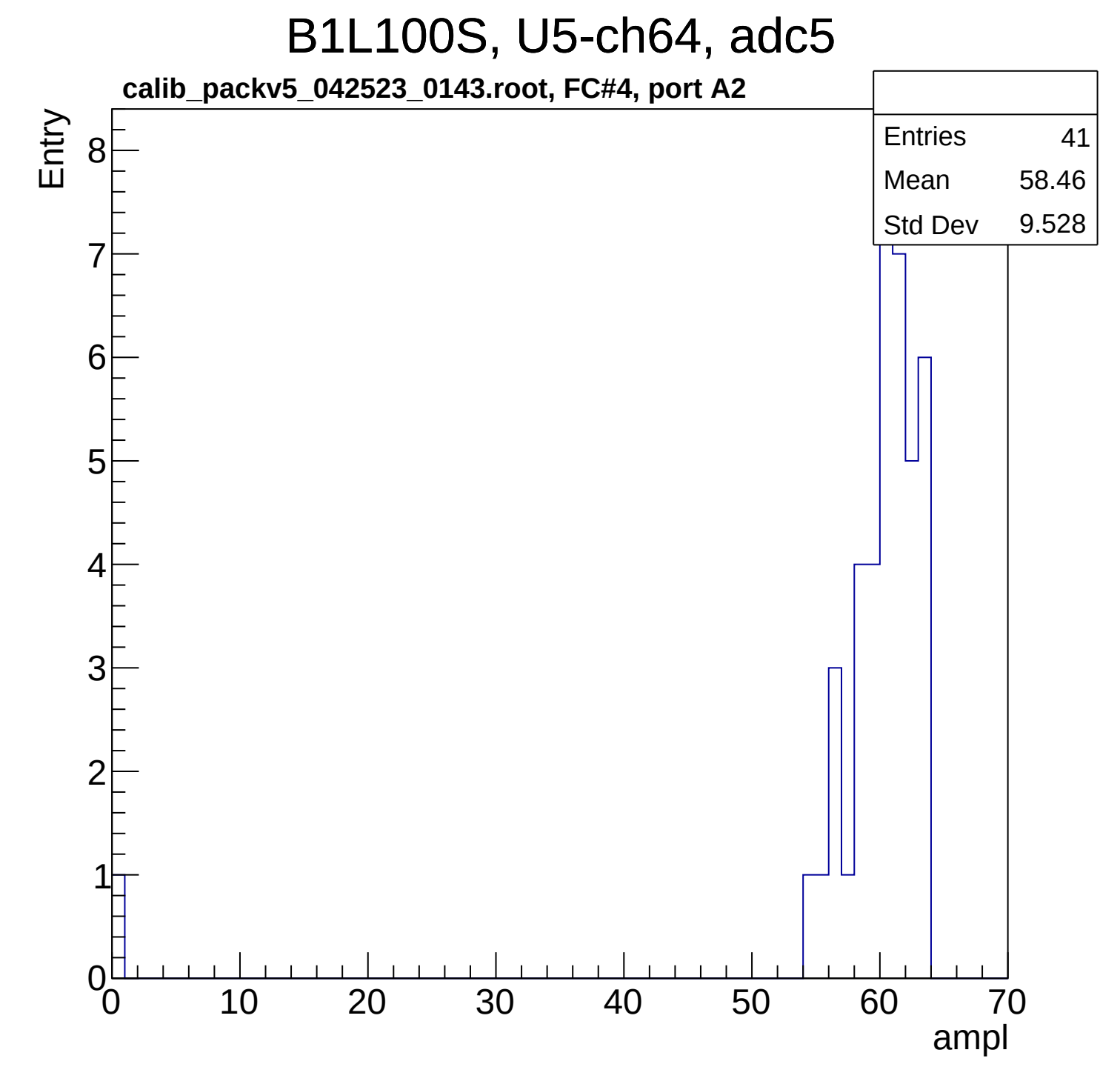
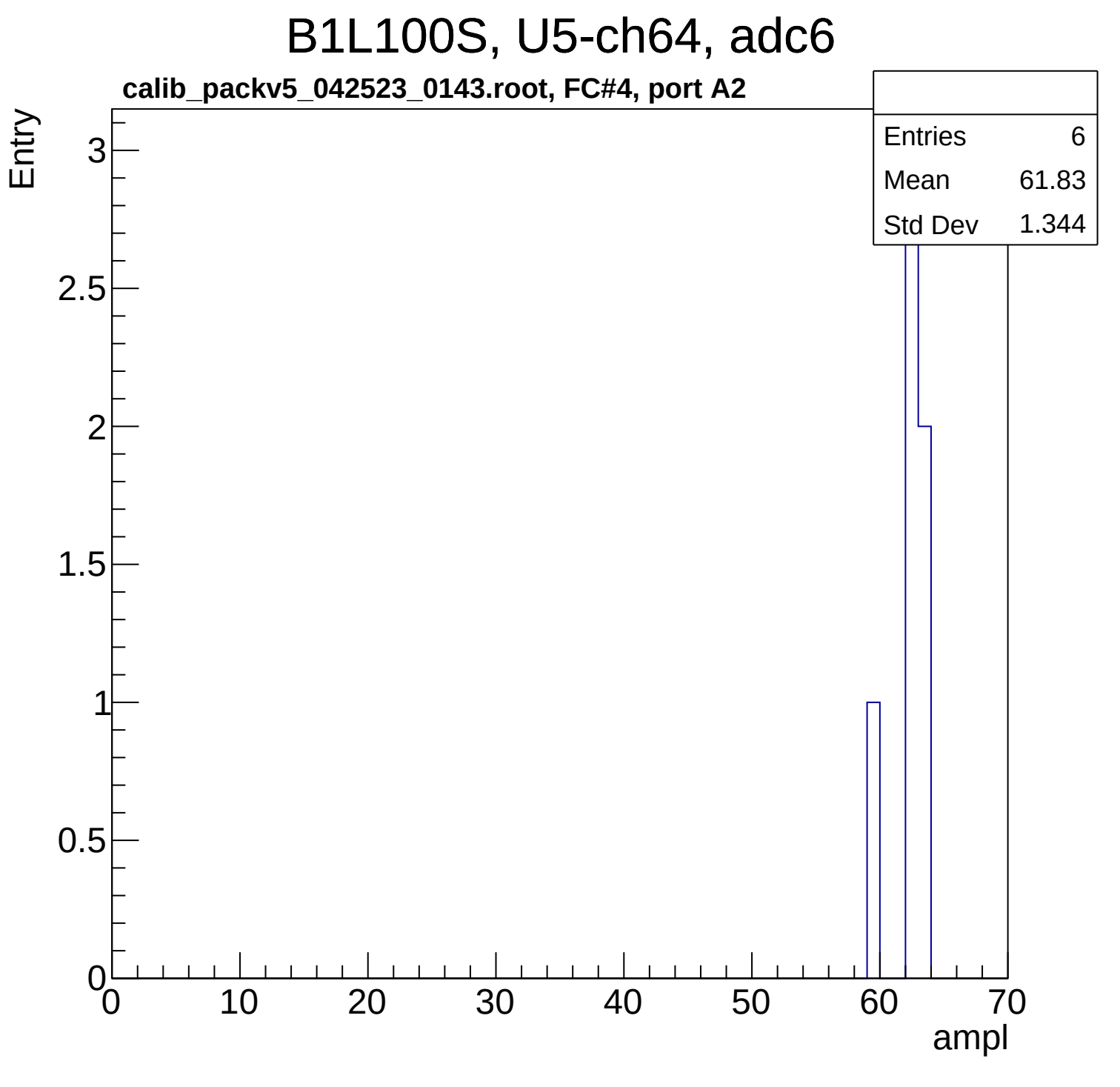

B1L100S, U5-ch64, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 41
Mean 58.46
Std Dev 9.528
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch64, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 6
Mean 61.83
Std Dev 1.344
Entry
ampl
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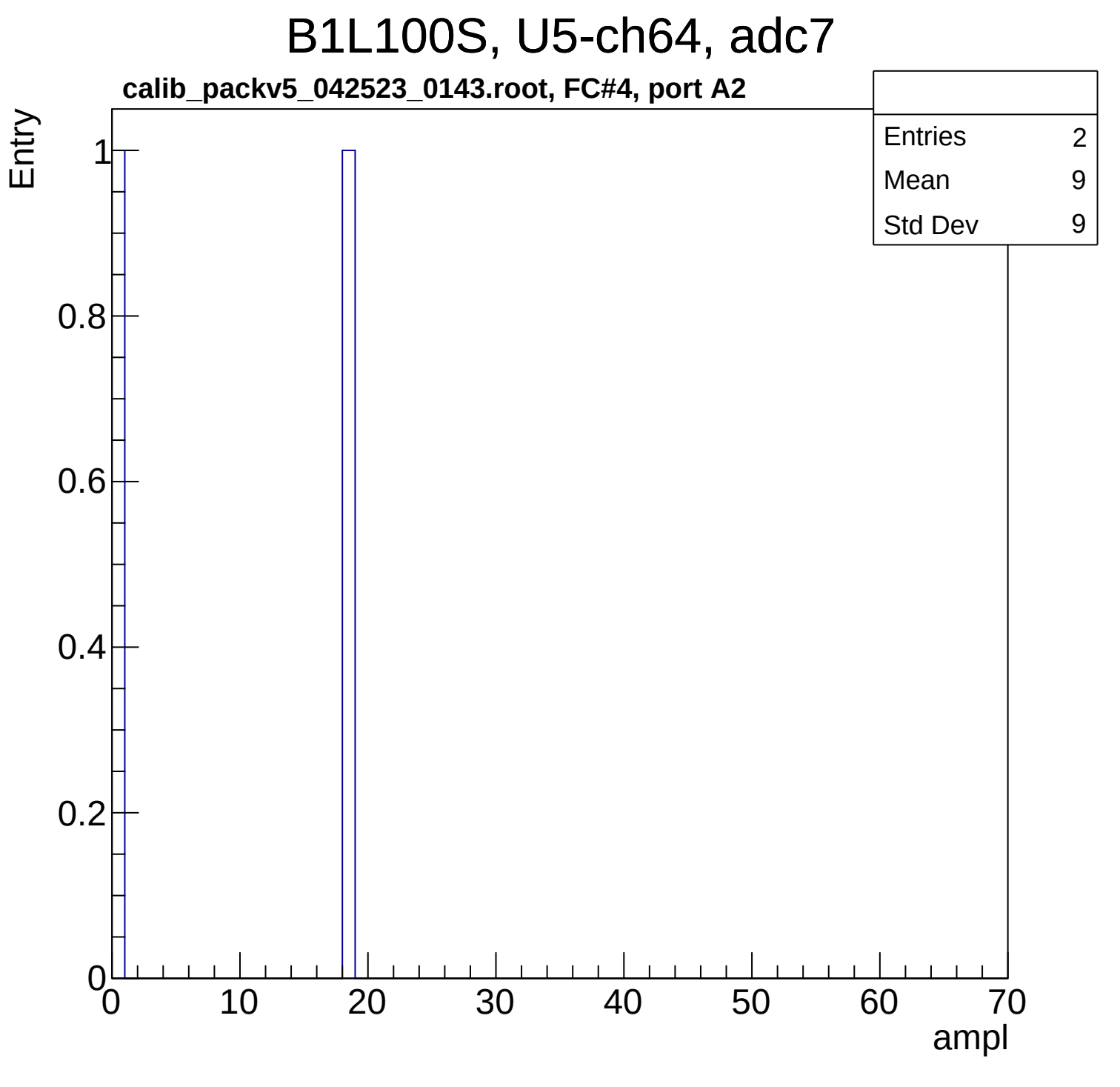
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L100S, U5-ch64, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 9
Std Dev 9
Entry
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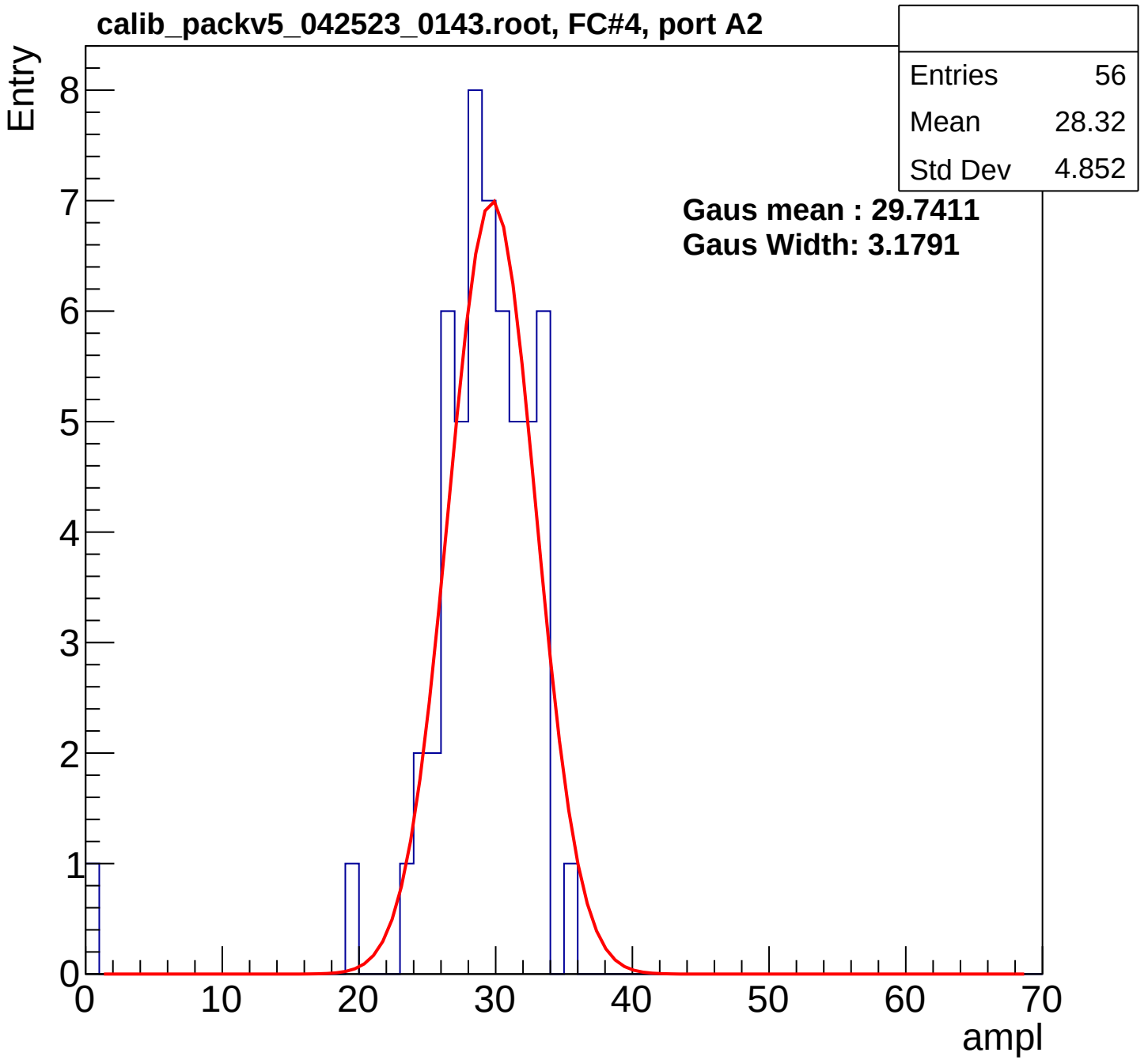
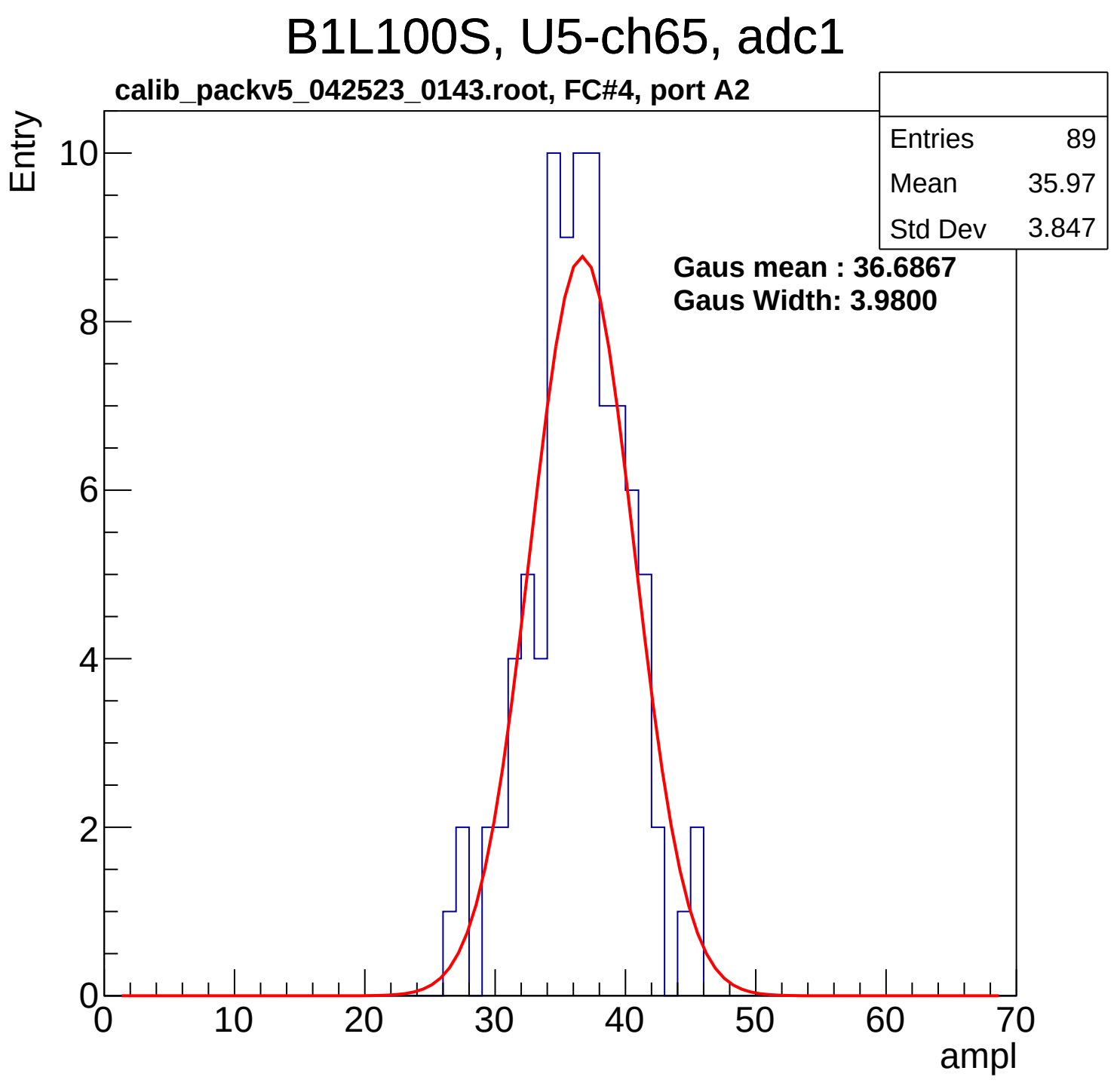
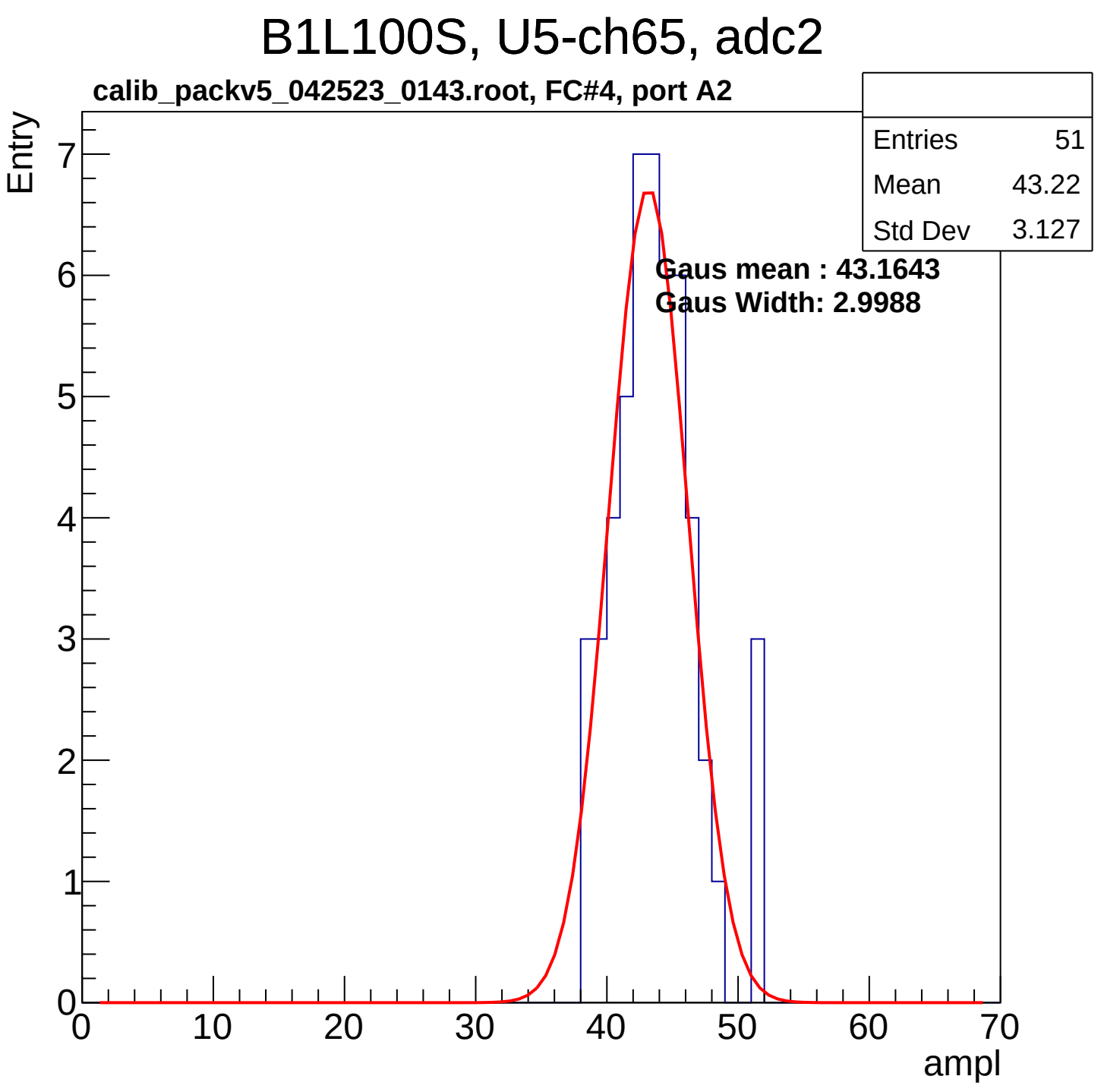
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch65, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 28.32
Std Dev 4.852
Gaus mean : 29.7411
Gaus Width: 3.1791
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch65, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 89
Mean 35.97
Std Dev 3.847
Gaus mean : 36.6867
Gaus Width: 3.9800
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch65, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 43.22
Std Dev 3.127
Gaus mean : 43.1643
Gaus Width: 2.9988
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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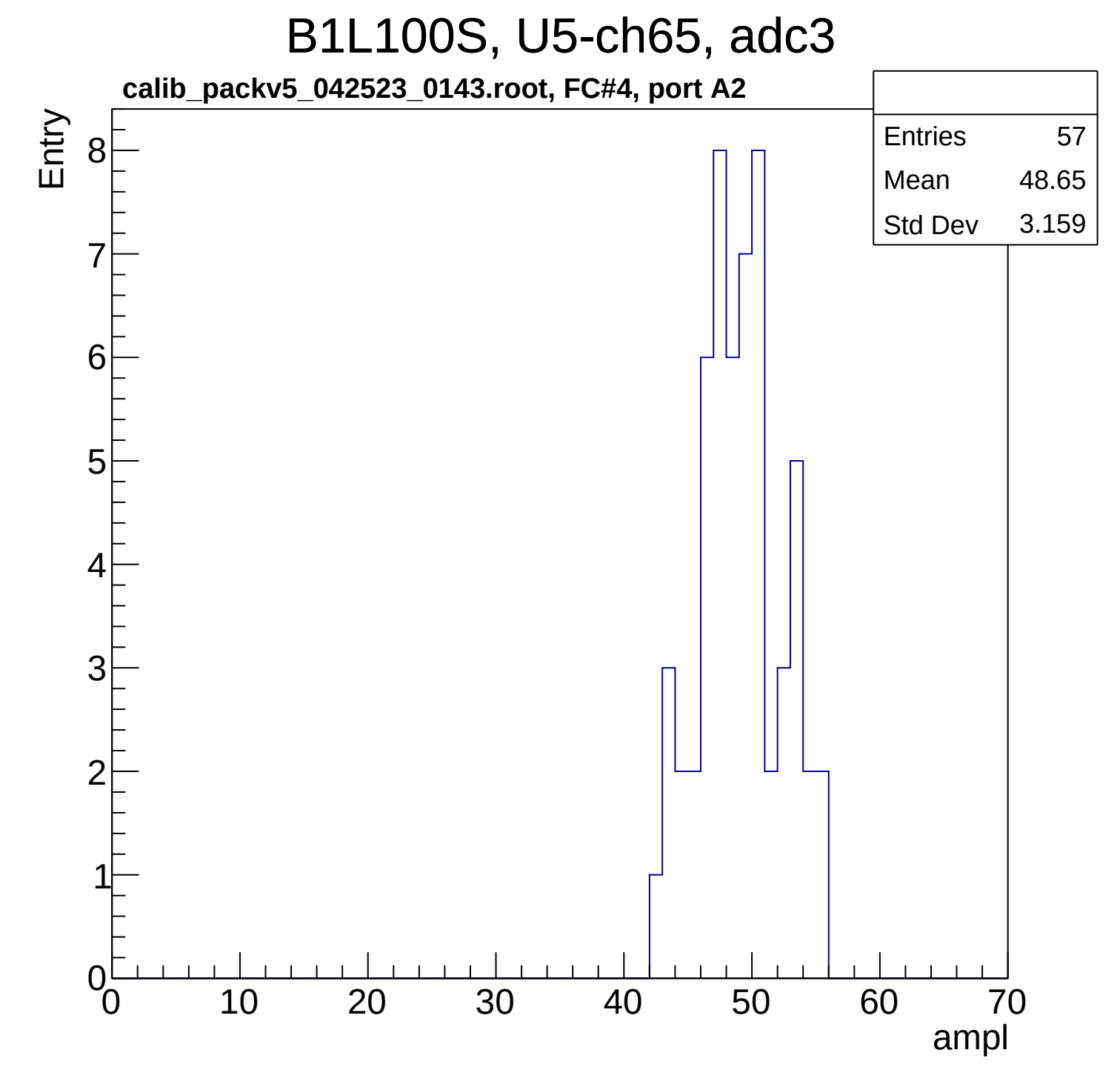
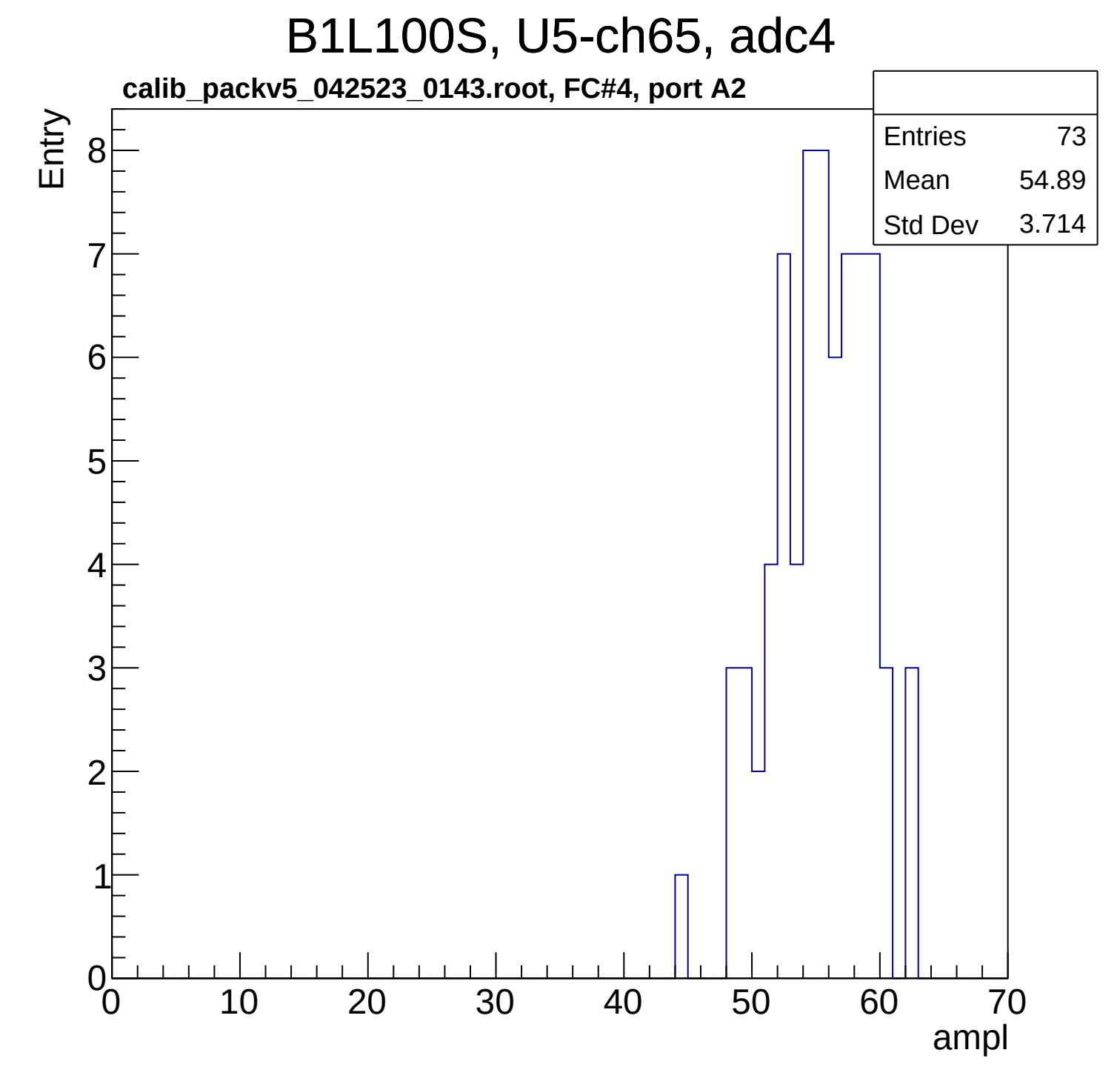

B1L100S, U5-ch65, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 48.65
Std Dev 3.159
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch65, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 54.89
Std Dev 3.714
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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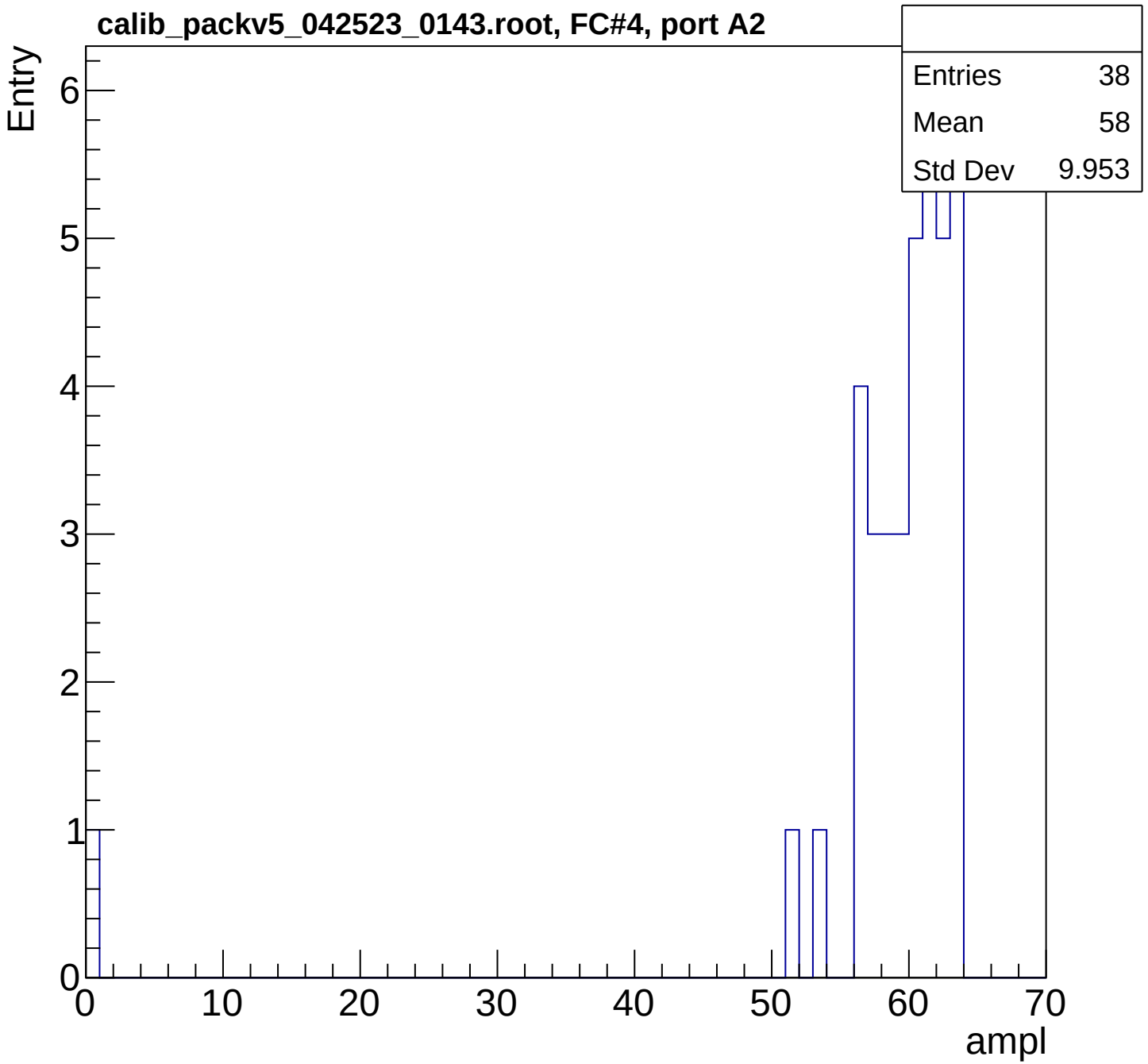
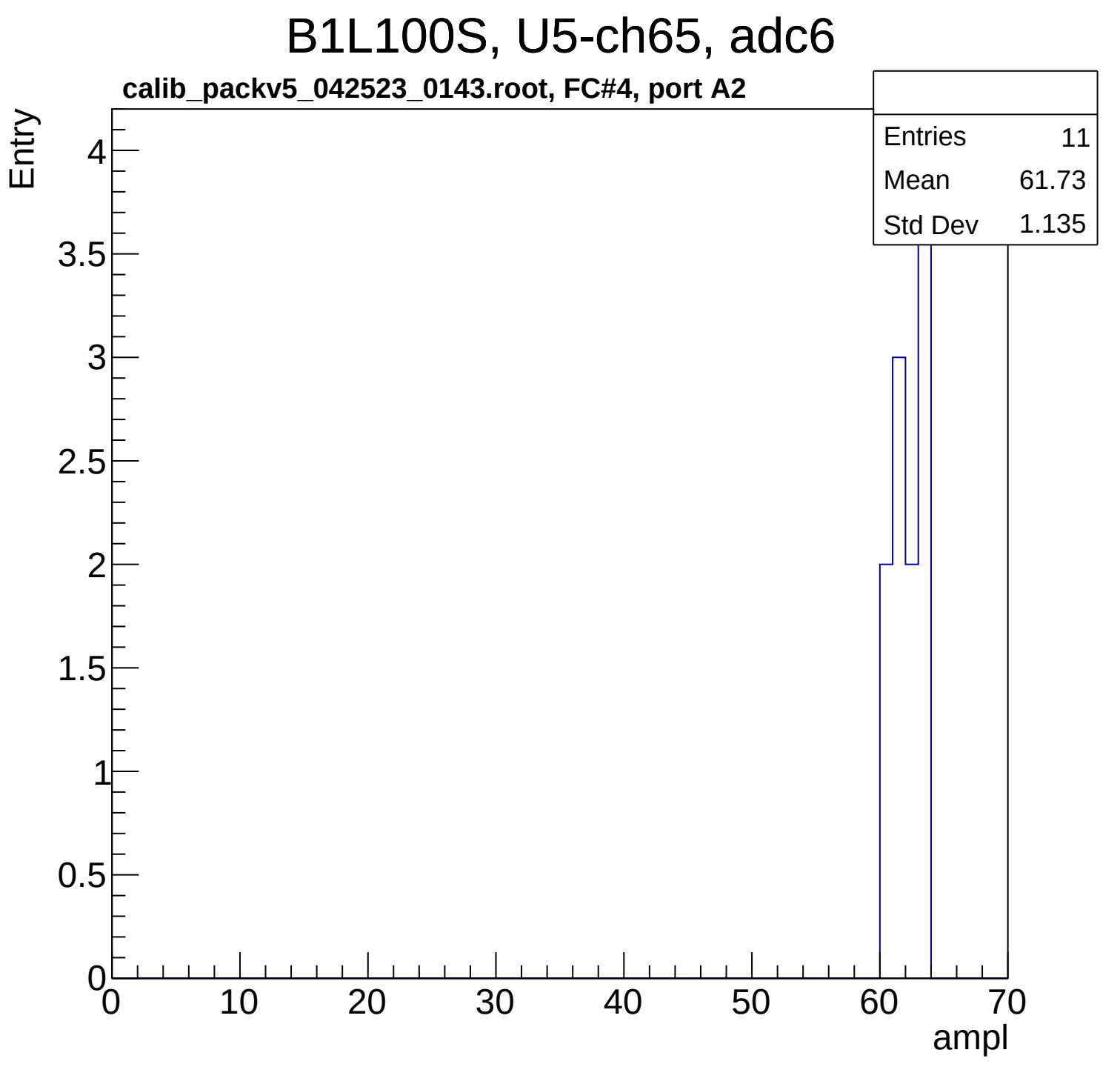
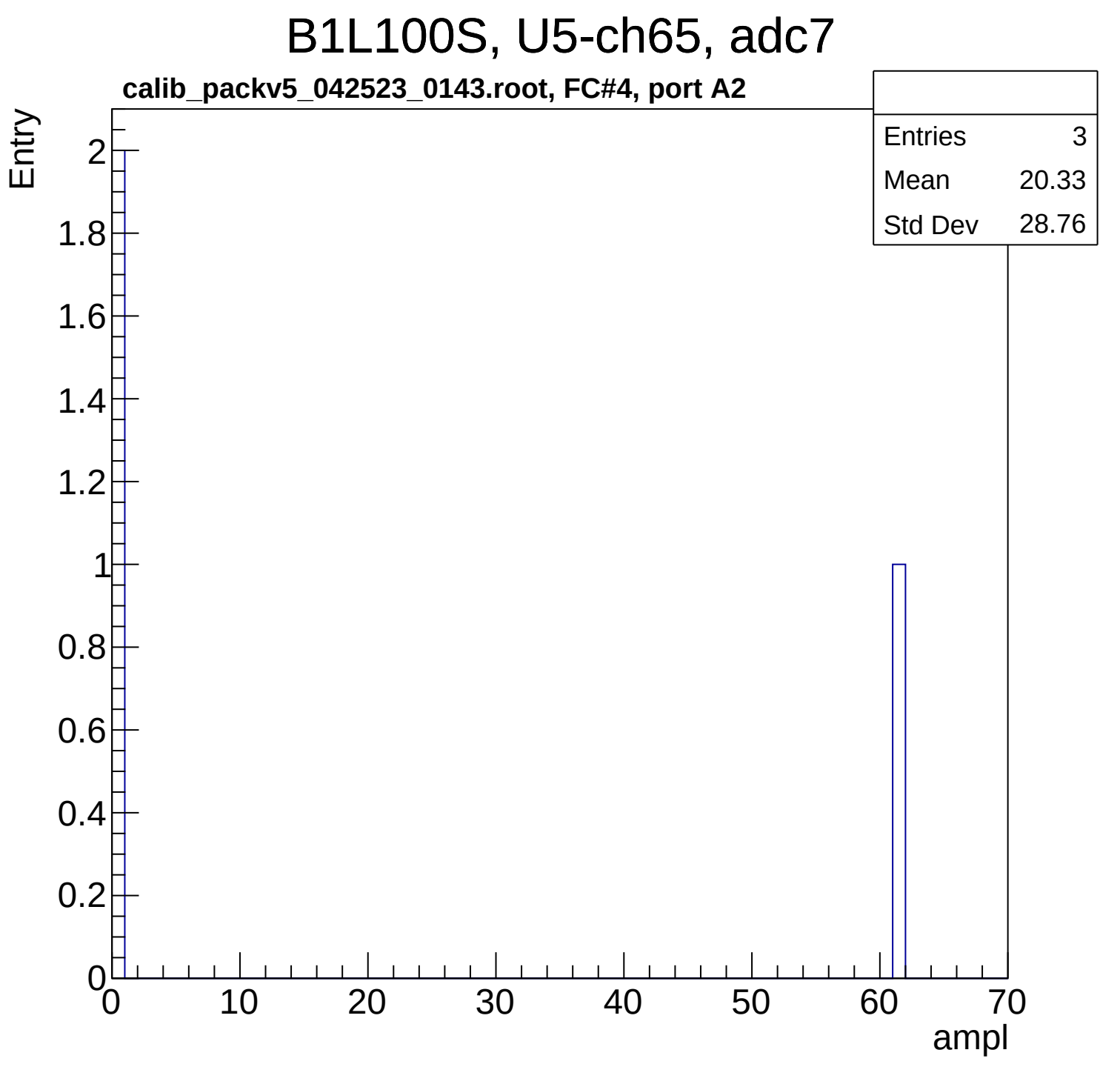
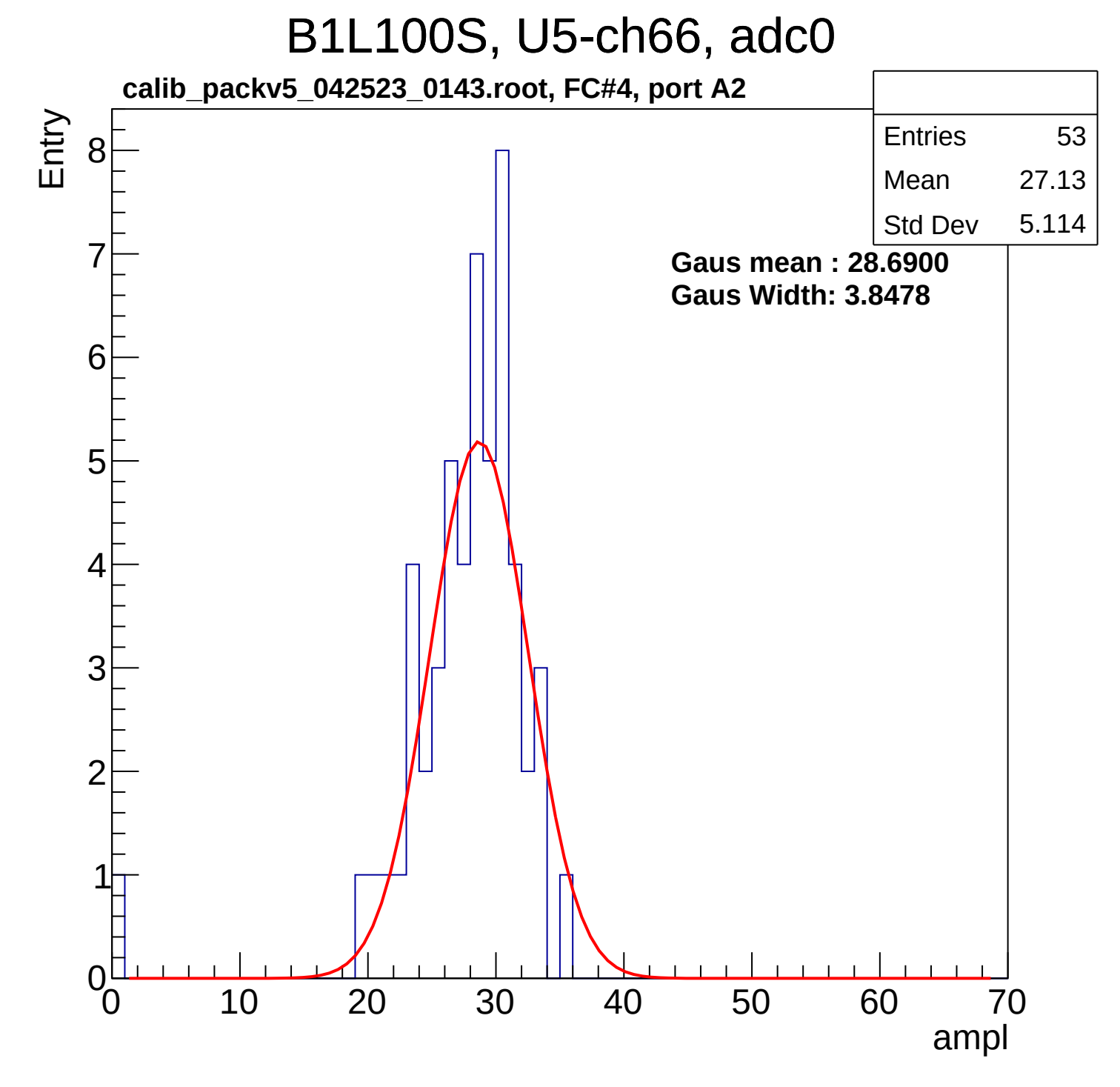
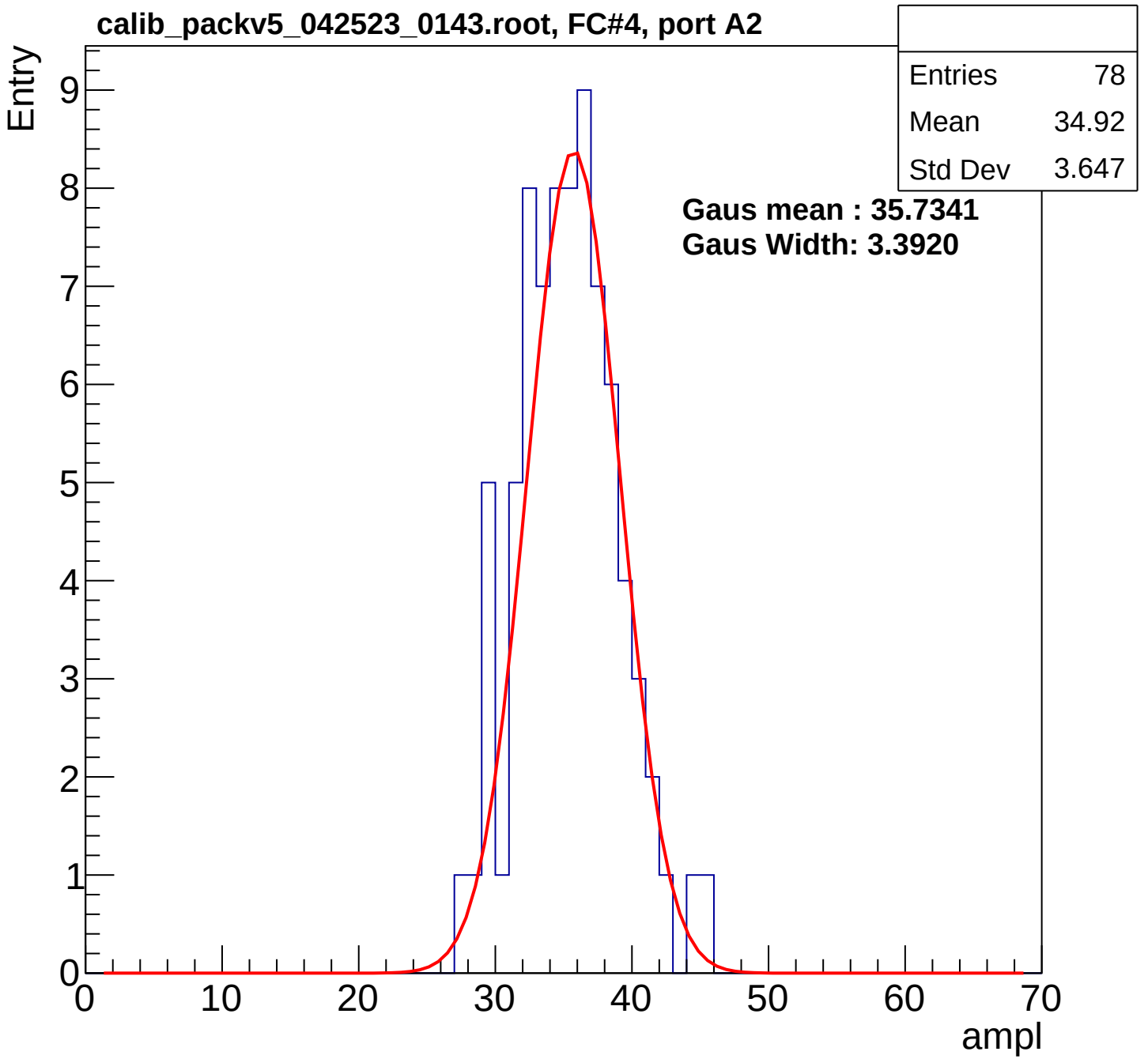
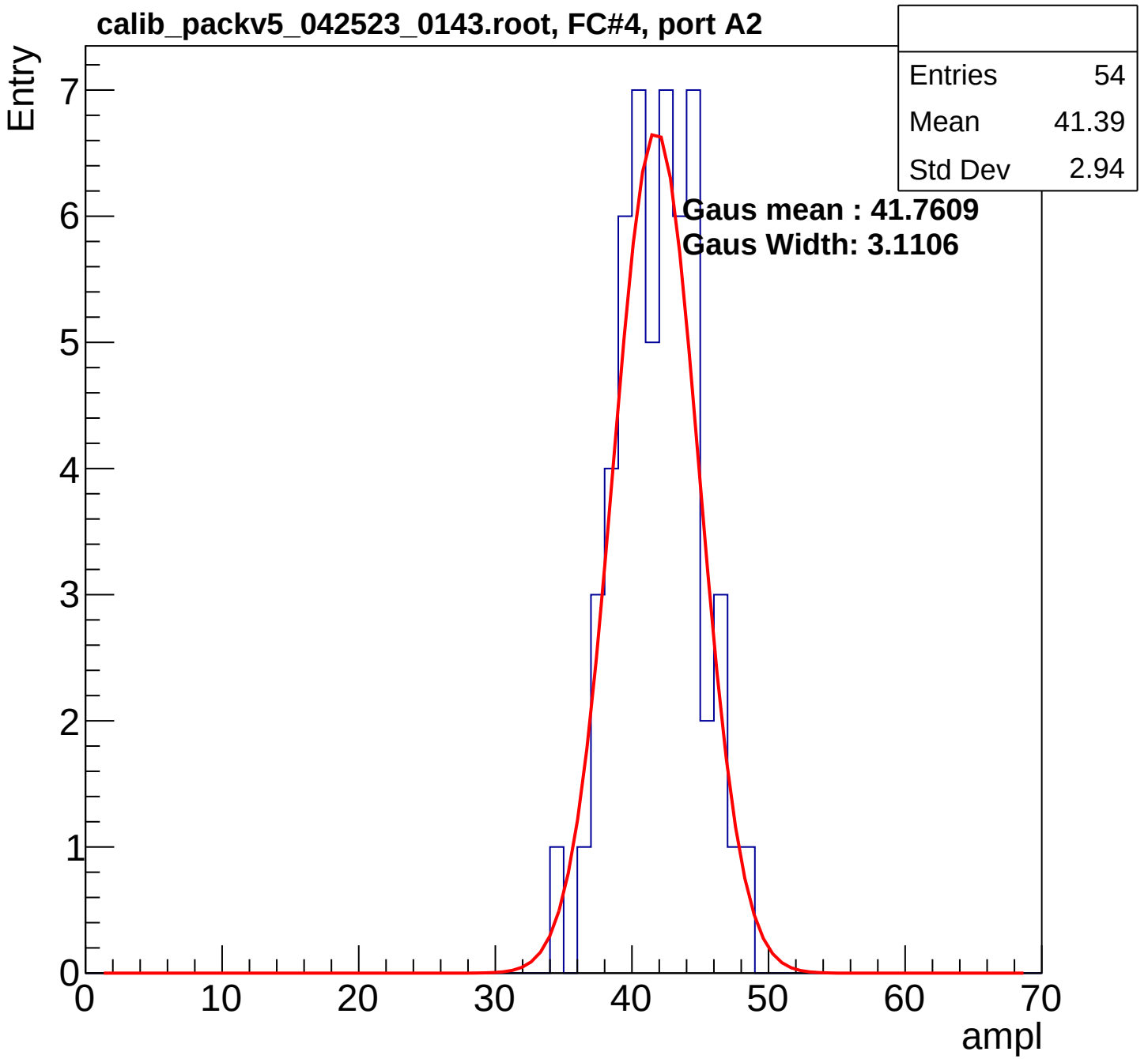

B1L100S, U5-ch65, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 38
Mean 58
Std Dev 9.953
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

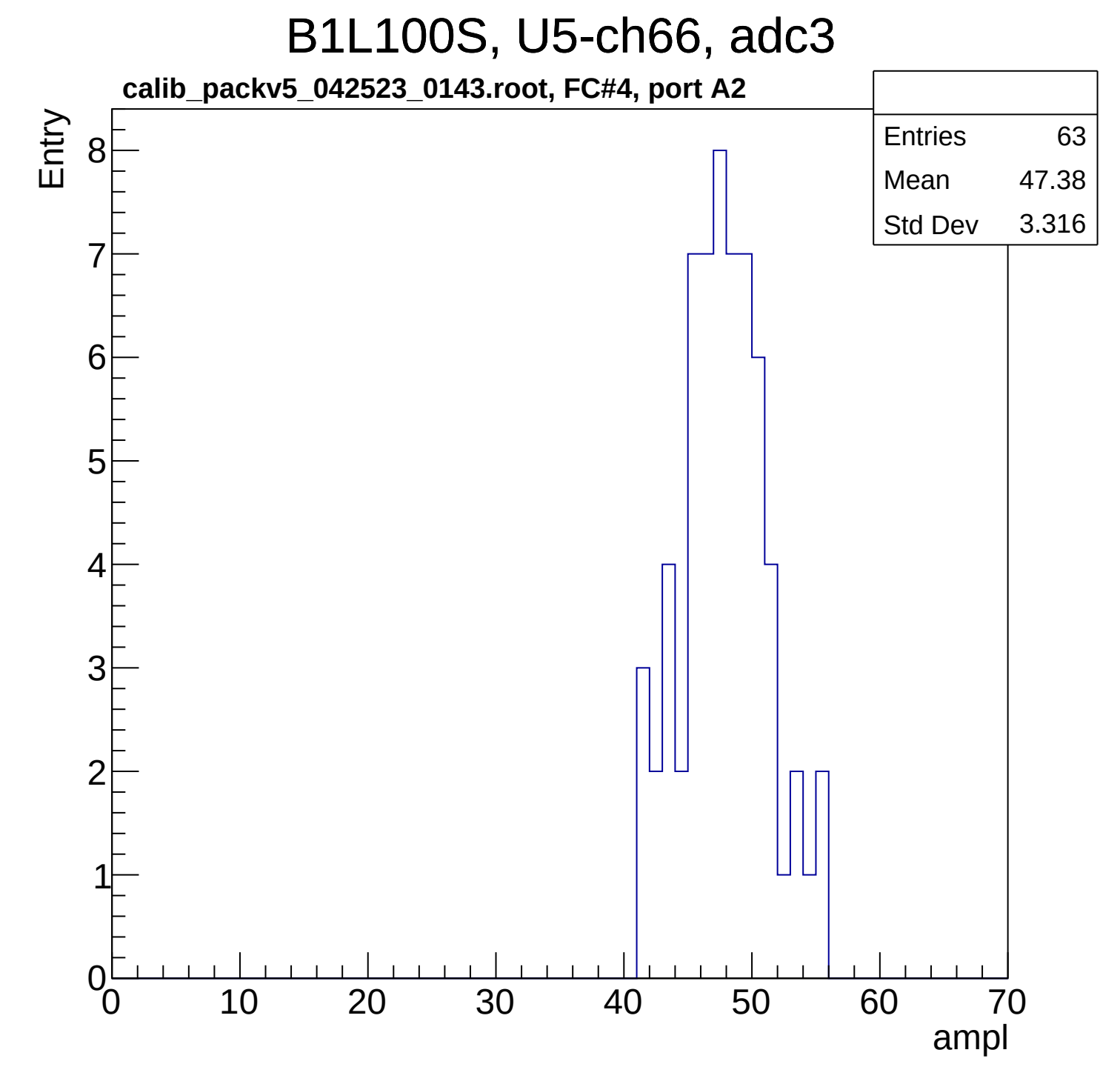

B1L100S, U5-ch65, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 11
Mean 61.73
Std Dev 1.135
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L100S, U5-ch65, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 20.33
Std Dev 28.76
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L100S, U5-ch66, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 27.13
Std Dev 5.114
Gaus mean : 28.6900
Gaus Width: 3.8478
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch66, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 78
Mean 34.92
Std Dev 3.647
Gaus mean : 35.7341
Gaus Width: 3.3920
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch66, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 41.39
Std Dev 2.94
Gaus mean : 41.7609
Gaus Width: 3.1106
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U5-ch66, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 47.38
Std Dev 3.316
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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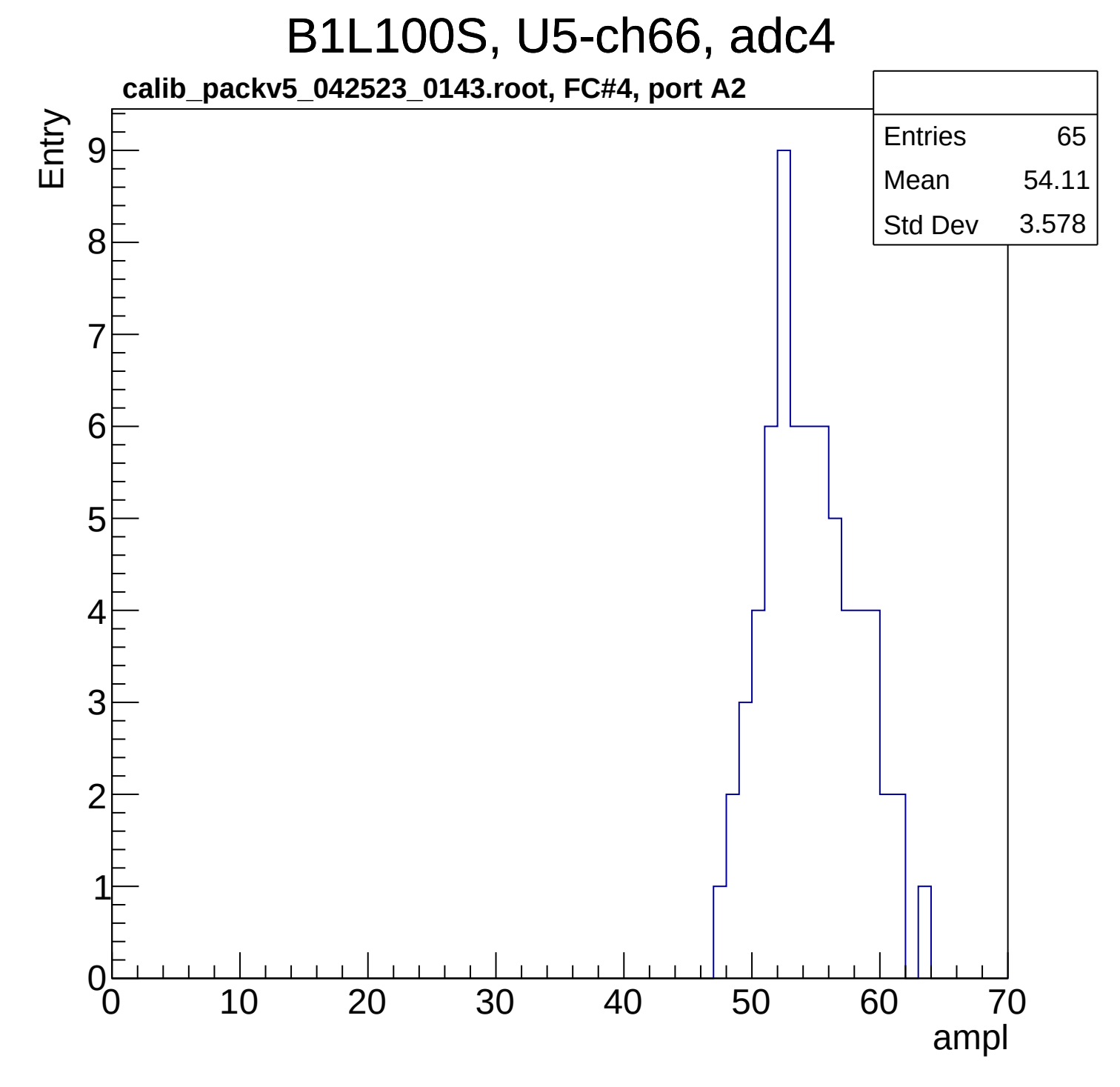
40
50
60
70


B1L100S, U5-ch66, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 54.11
Std Dev 3.578
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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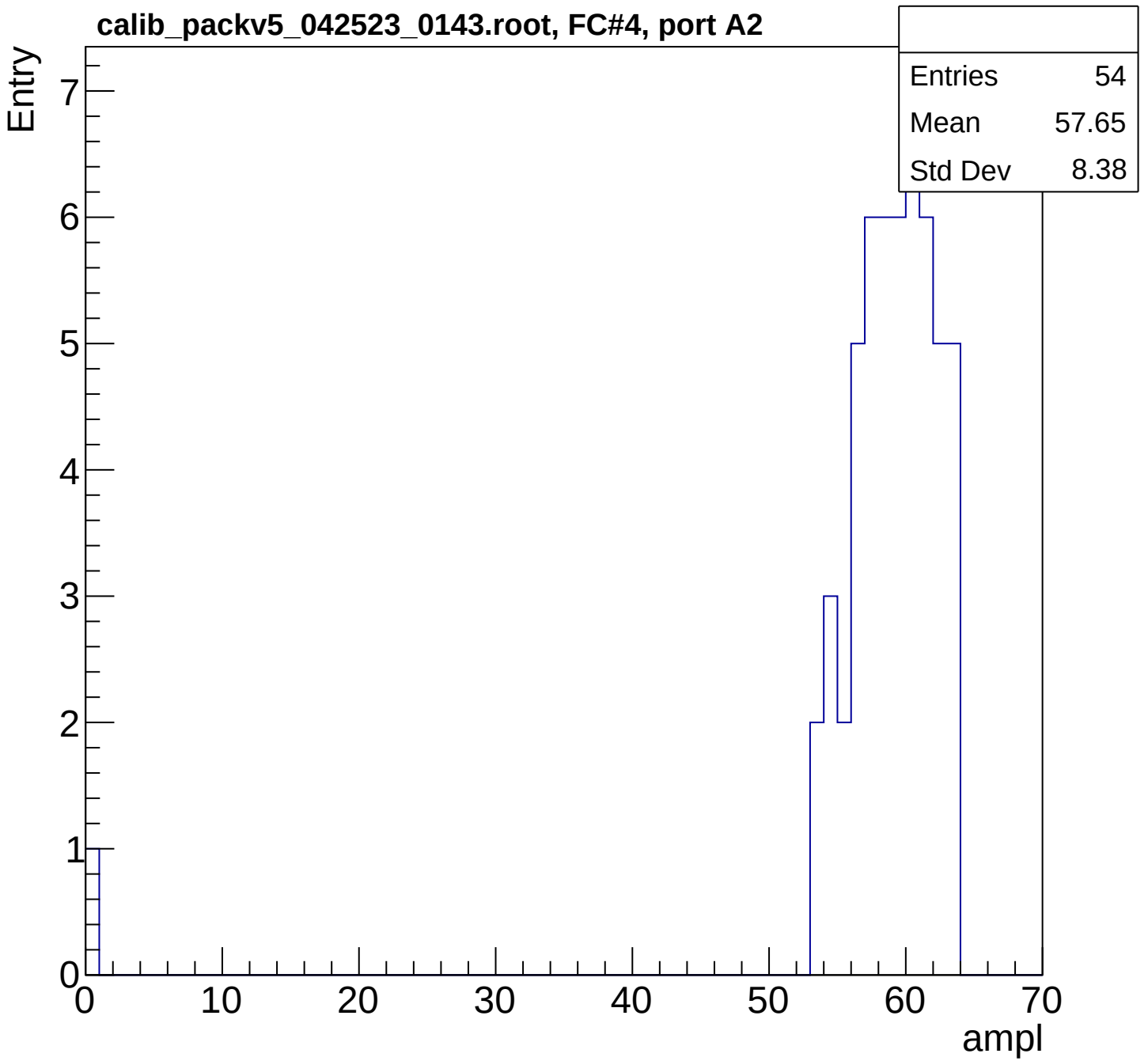
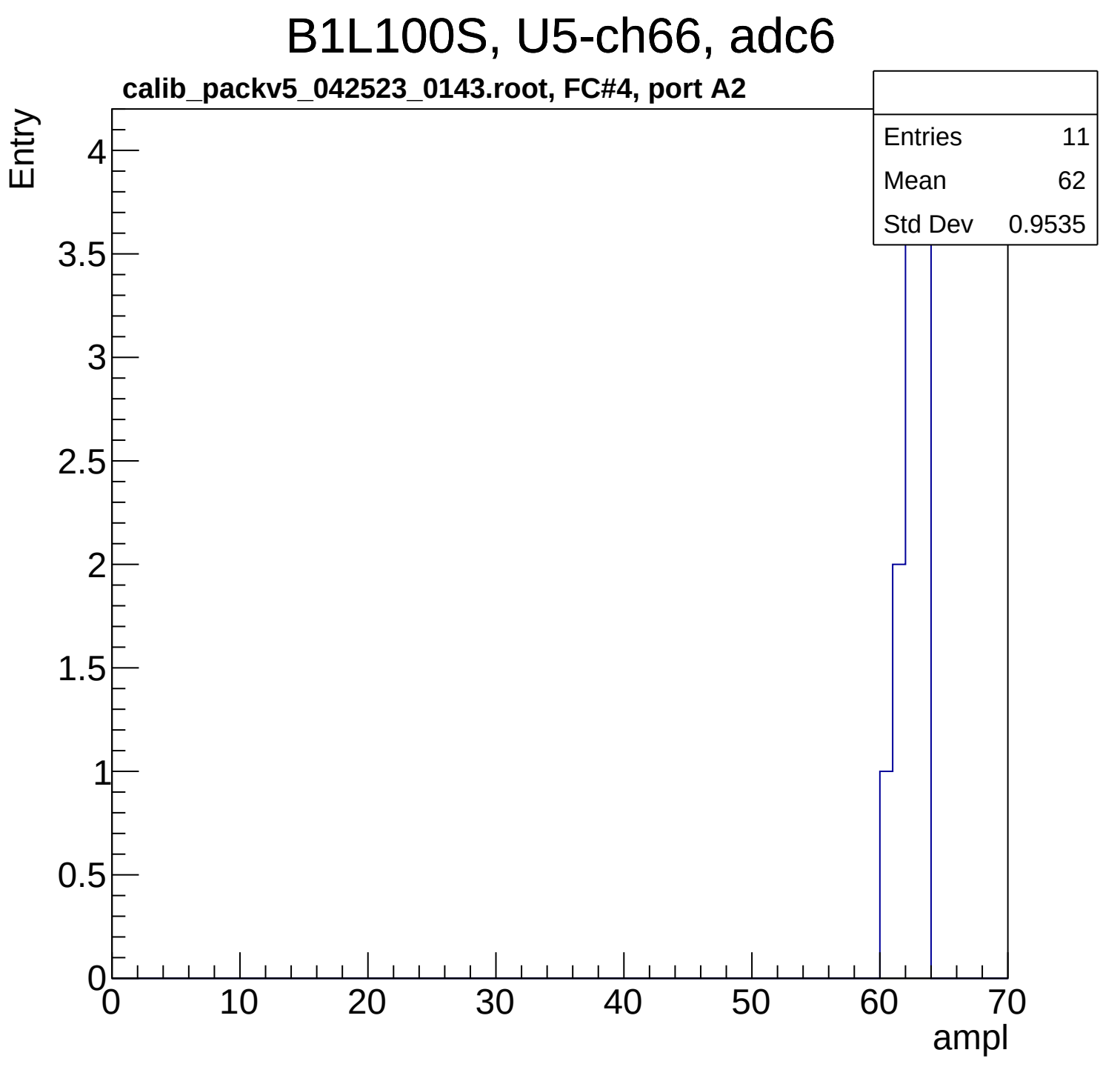

B1L100S, U5-ch66, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 57.65
Std Dev 8.38
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U5-ch66, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 11
Mean 62
Std Dev 0.9535
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
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40
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60
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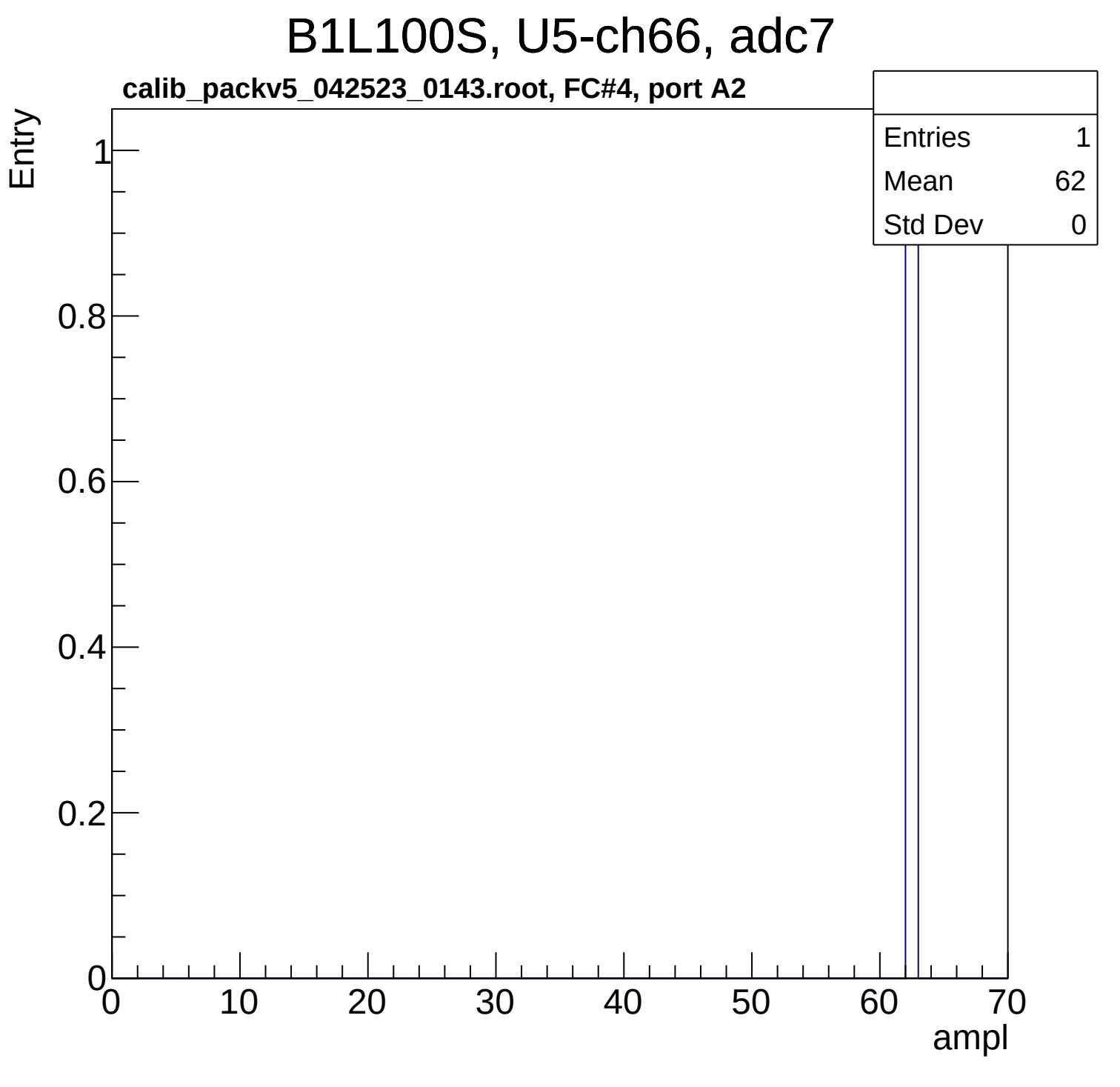
B1L100S, U5-ch66, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 62
Std Dev 0
Entry
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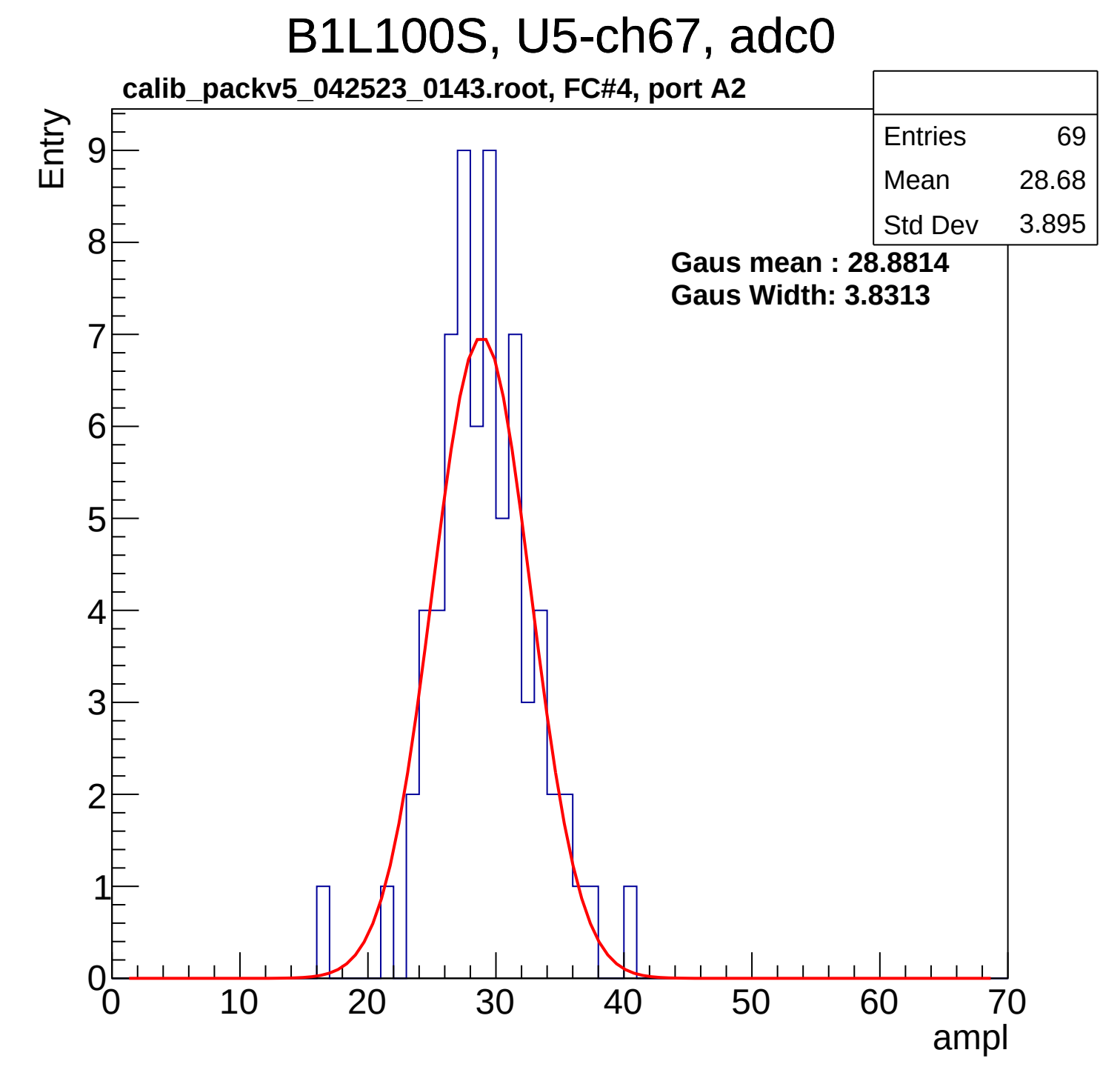
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch67, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 28.68
Std Dev 3.895
Gaus mean : 28.8814
Gaus Width: 3.8313
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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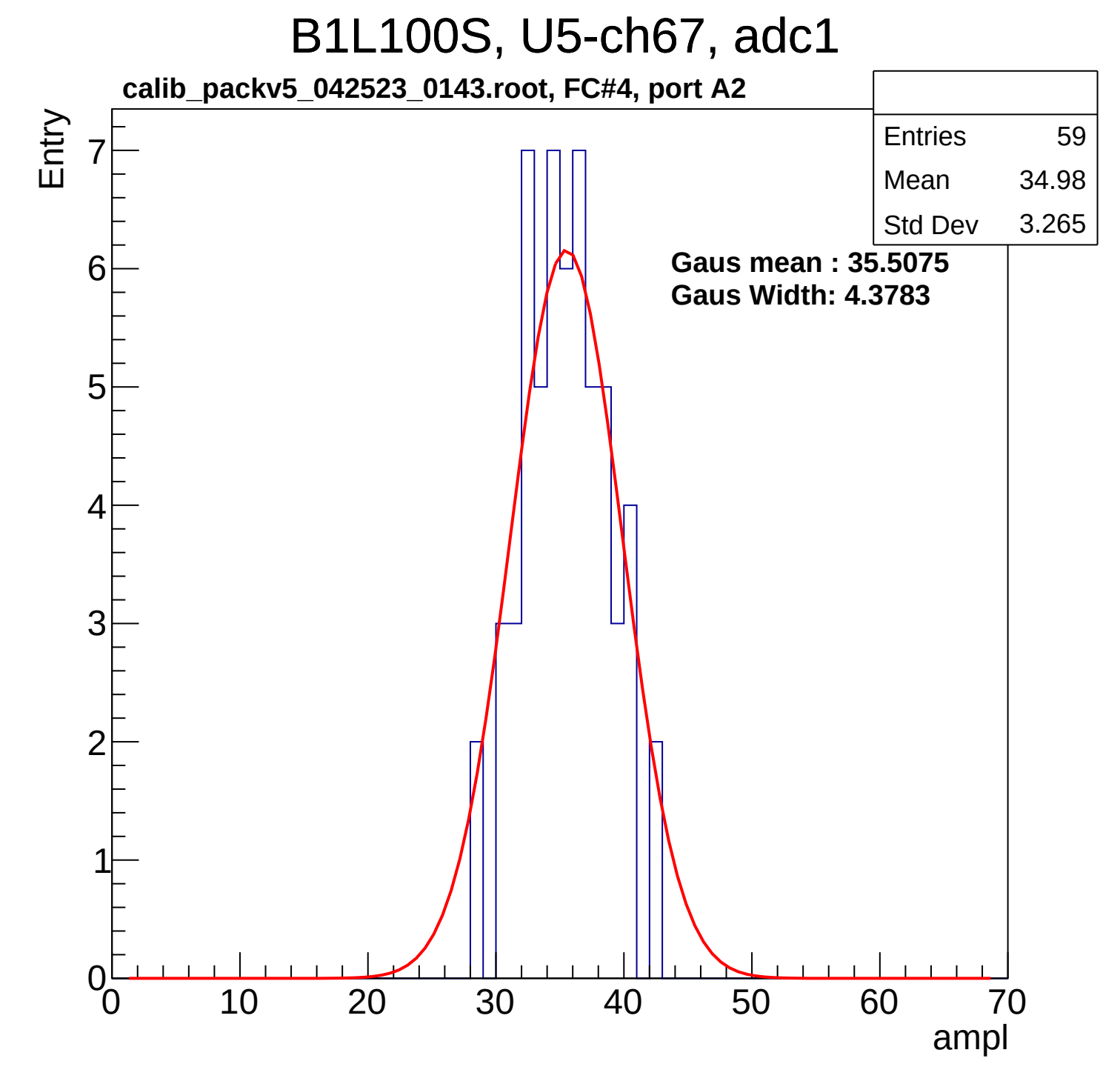
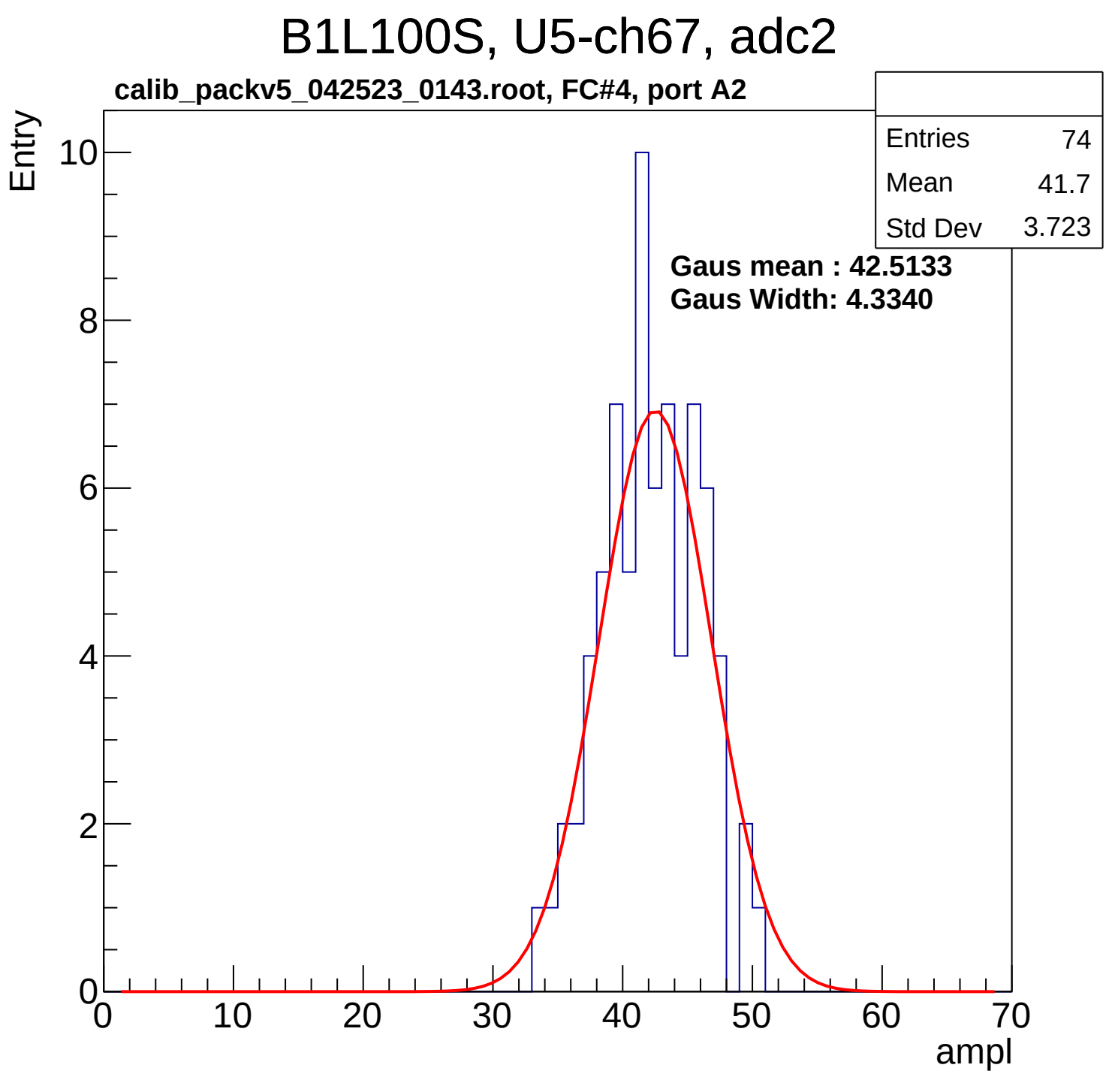

B1L100S, U5-ch67, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 34.98
Std Dev 3.265
Gaus mean : 35.5075
Gaus Width: 4.3783
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U5-ch67, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 74
Mean 41.7
Std Dev 3.723
Gaus mean : 42.5133
Gaus Width: 4.3340
Entry
ampl
0
2
4
6
8
10
0
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20
30
40
50
60
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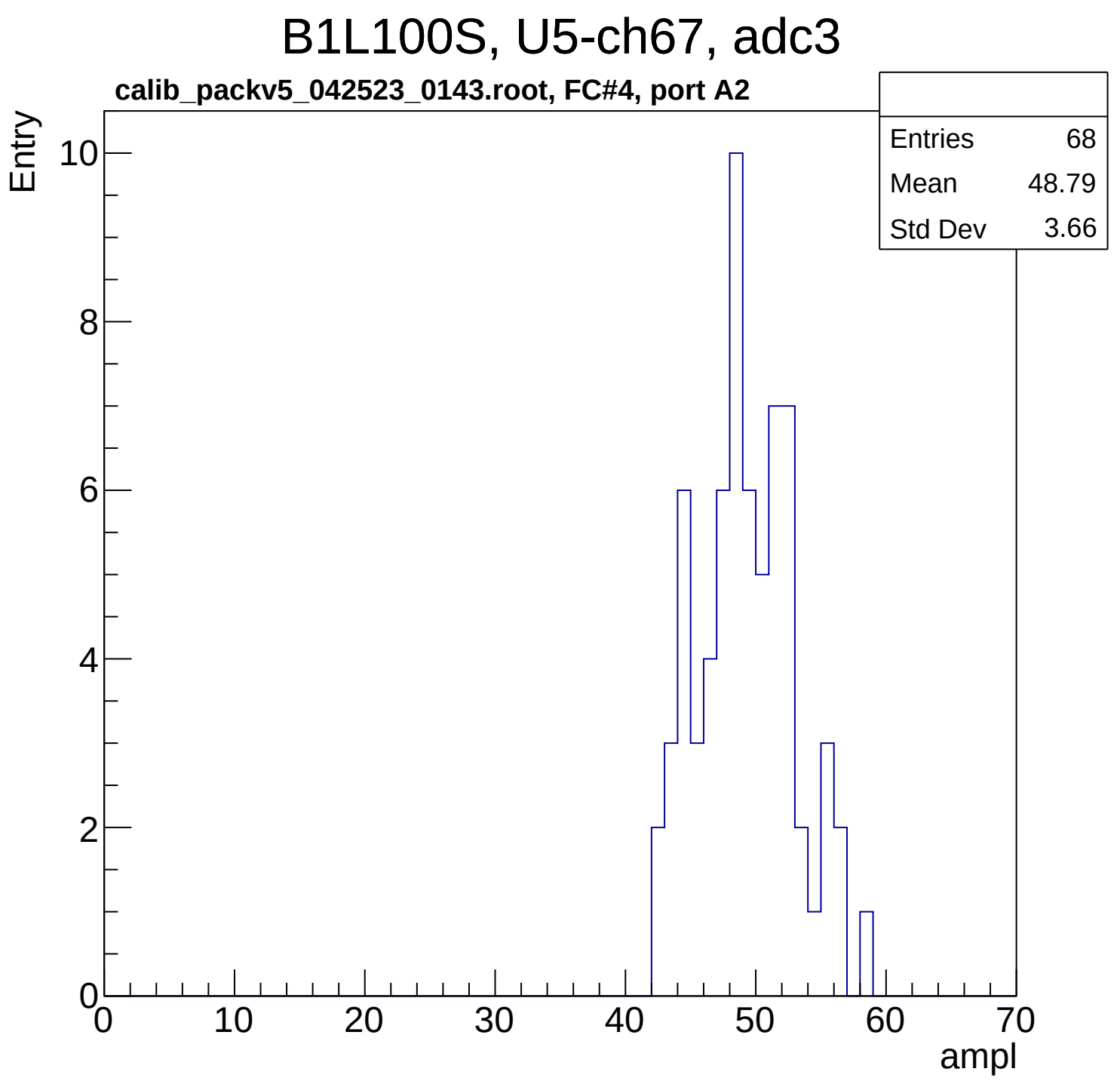
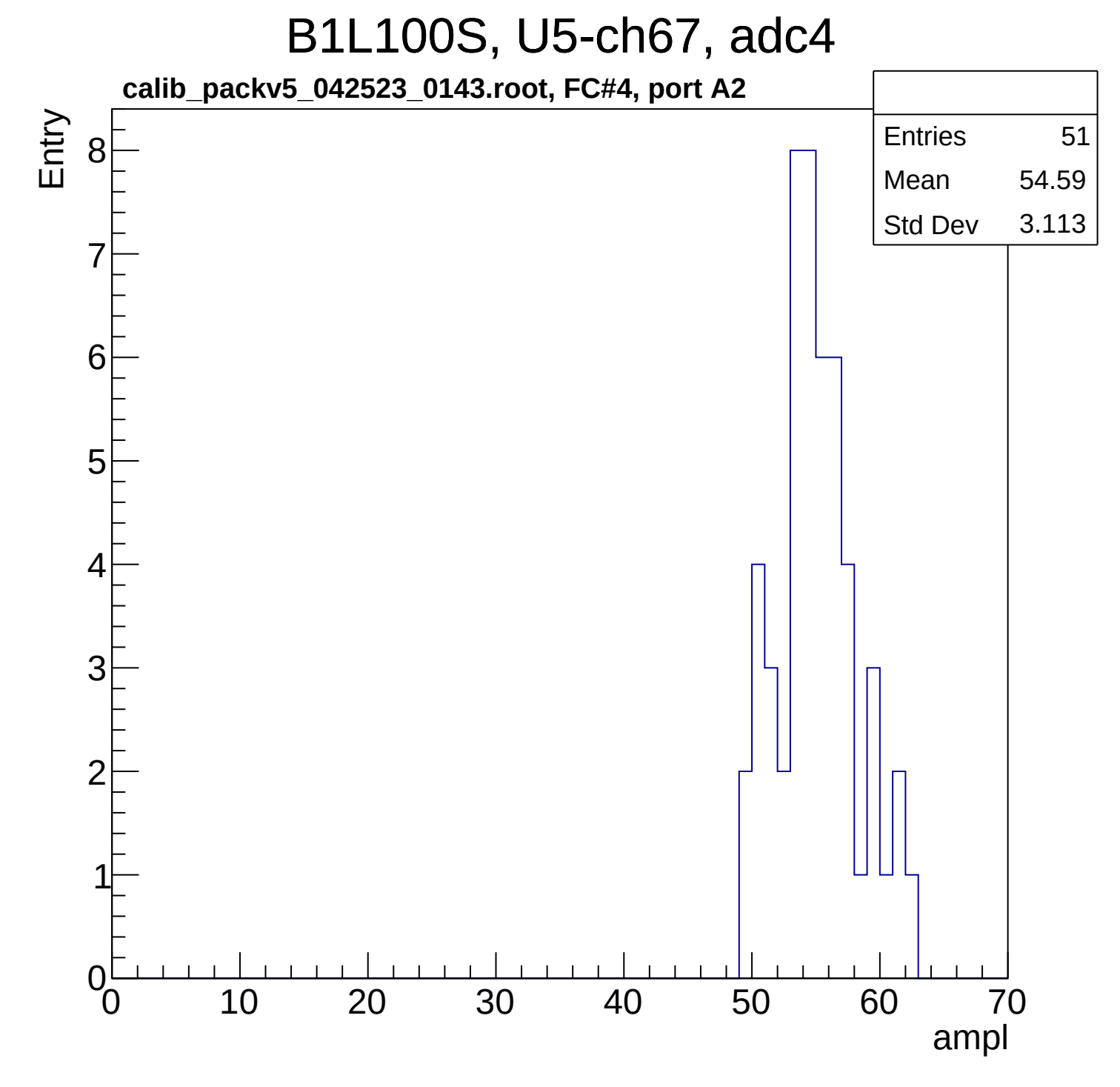
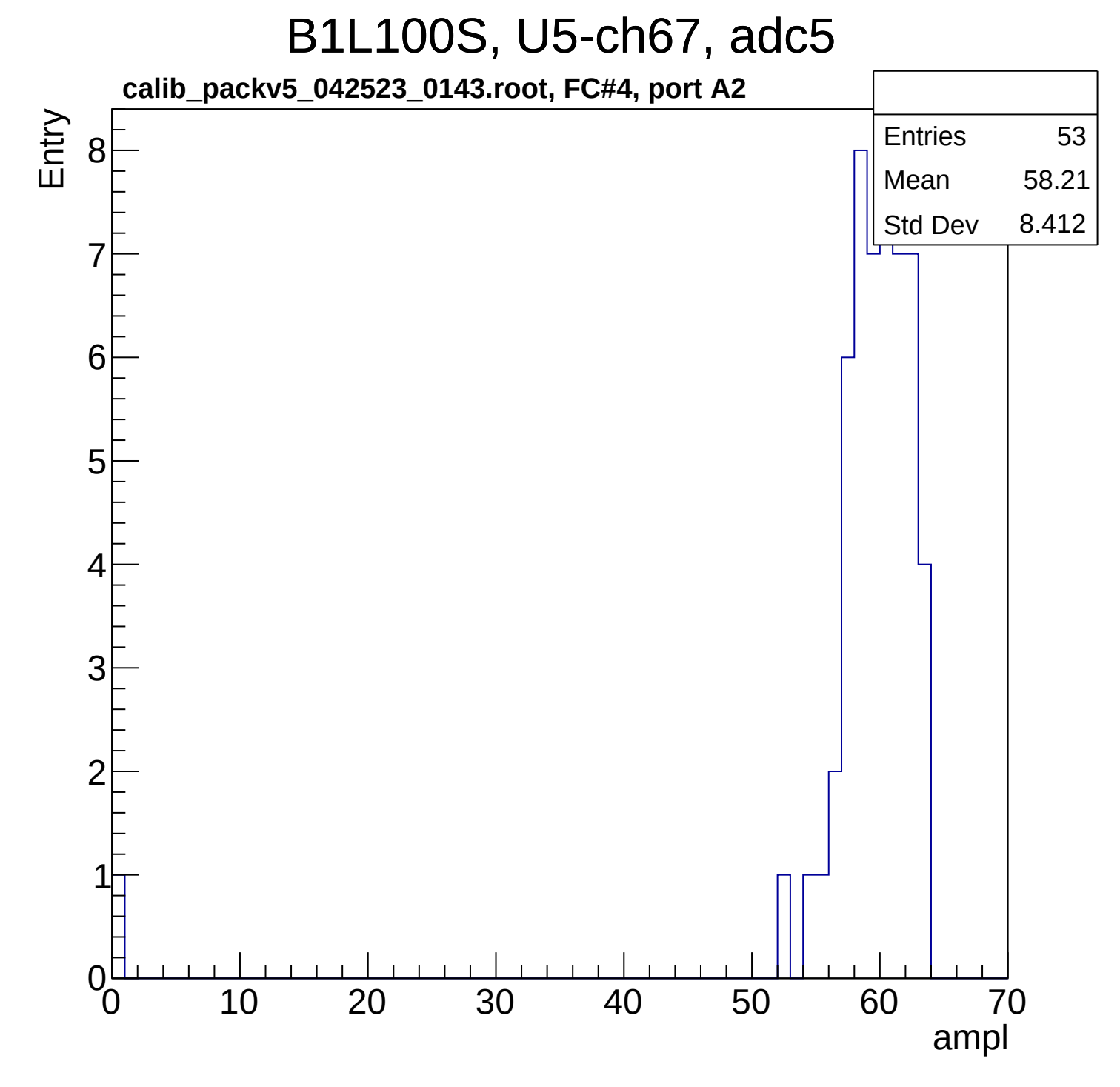

B1L100S, U5-ch67, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 48.79
Std Dev 3.66
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch67, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 54.59
Std Dev 3.113
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch67, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 58.21
Std Dev 8.412
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
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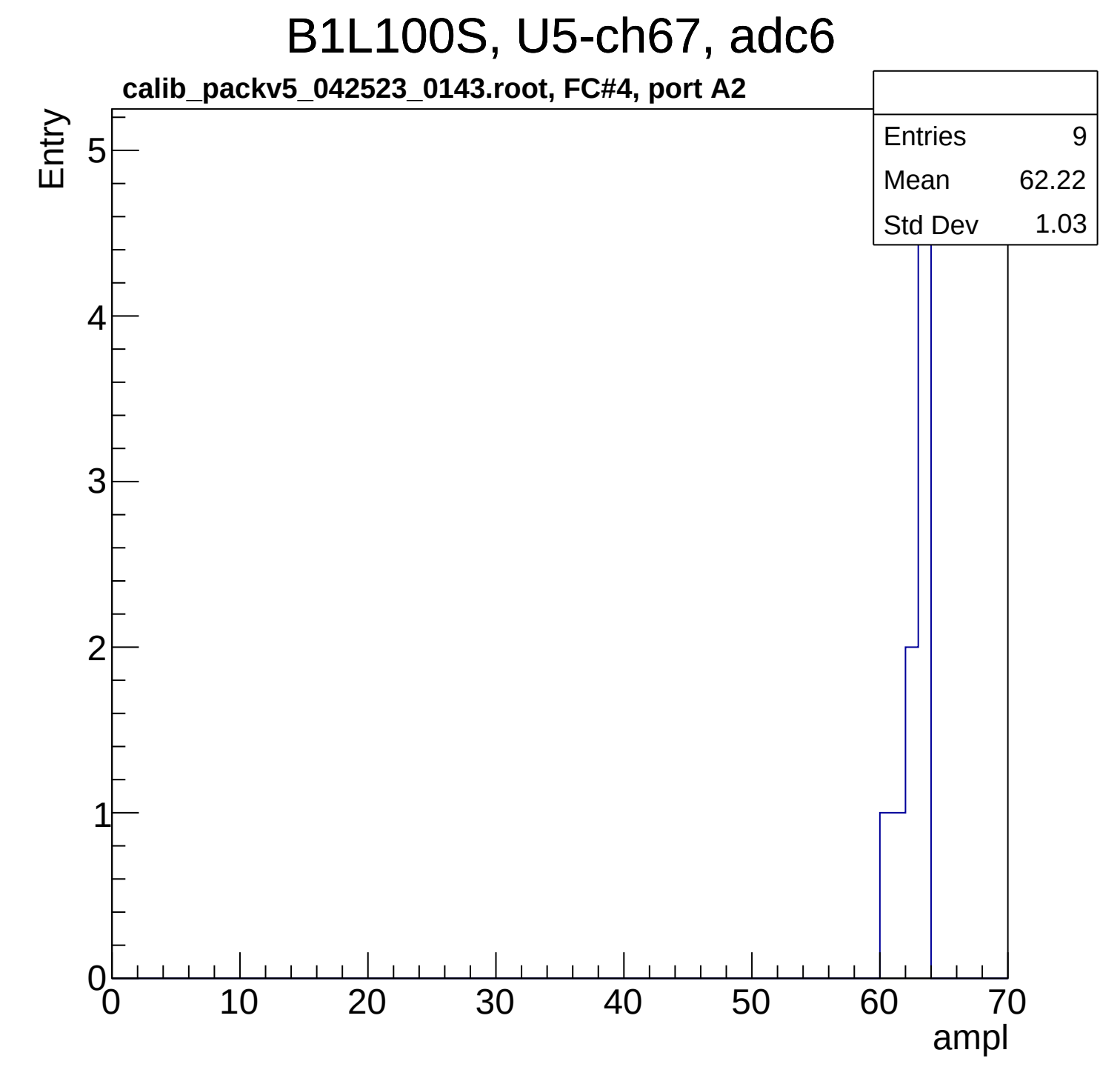
60
70


B1L100S, U5-ch67, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 9
Mean 62.22
Std Dev 1.03
Entry
ampl
0
1
2
3
4
5
0
10
20
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40
50
60
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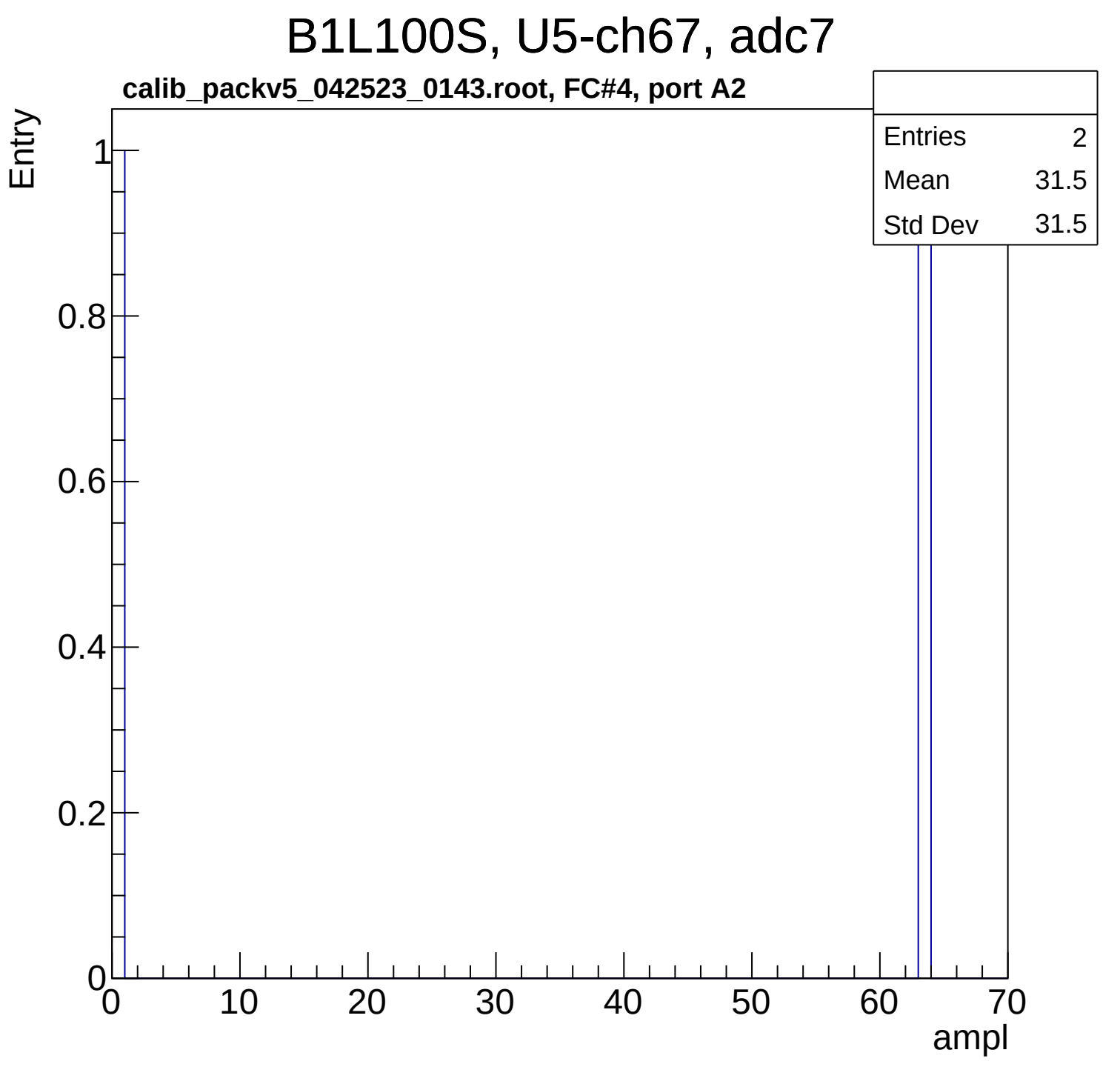
B1L100S, U5-ch67, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 31.5
Std Dev 31.5
Entry
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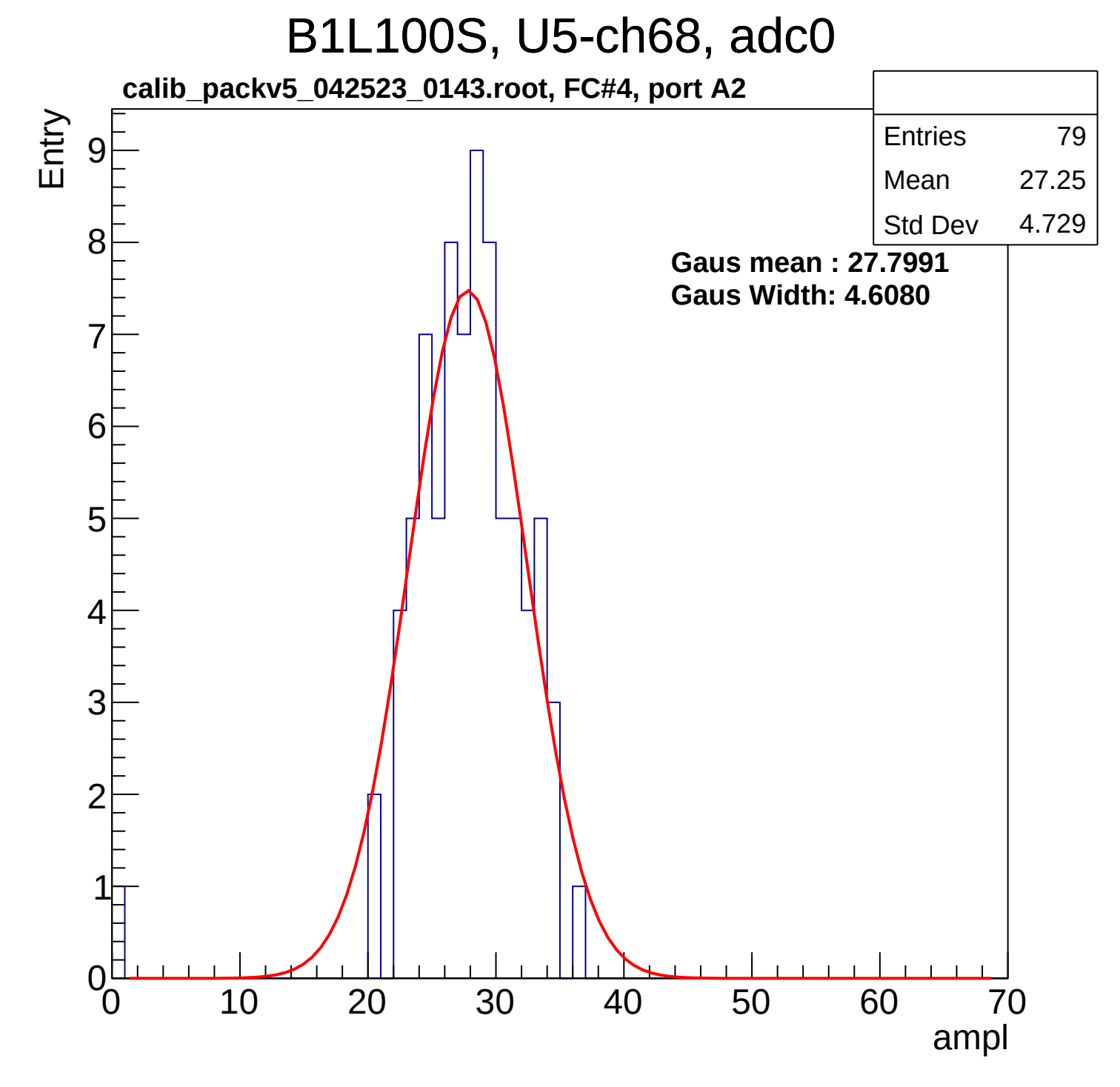
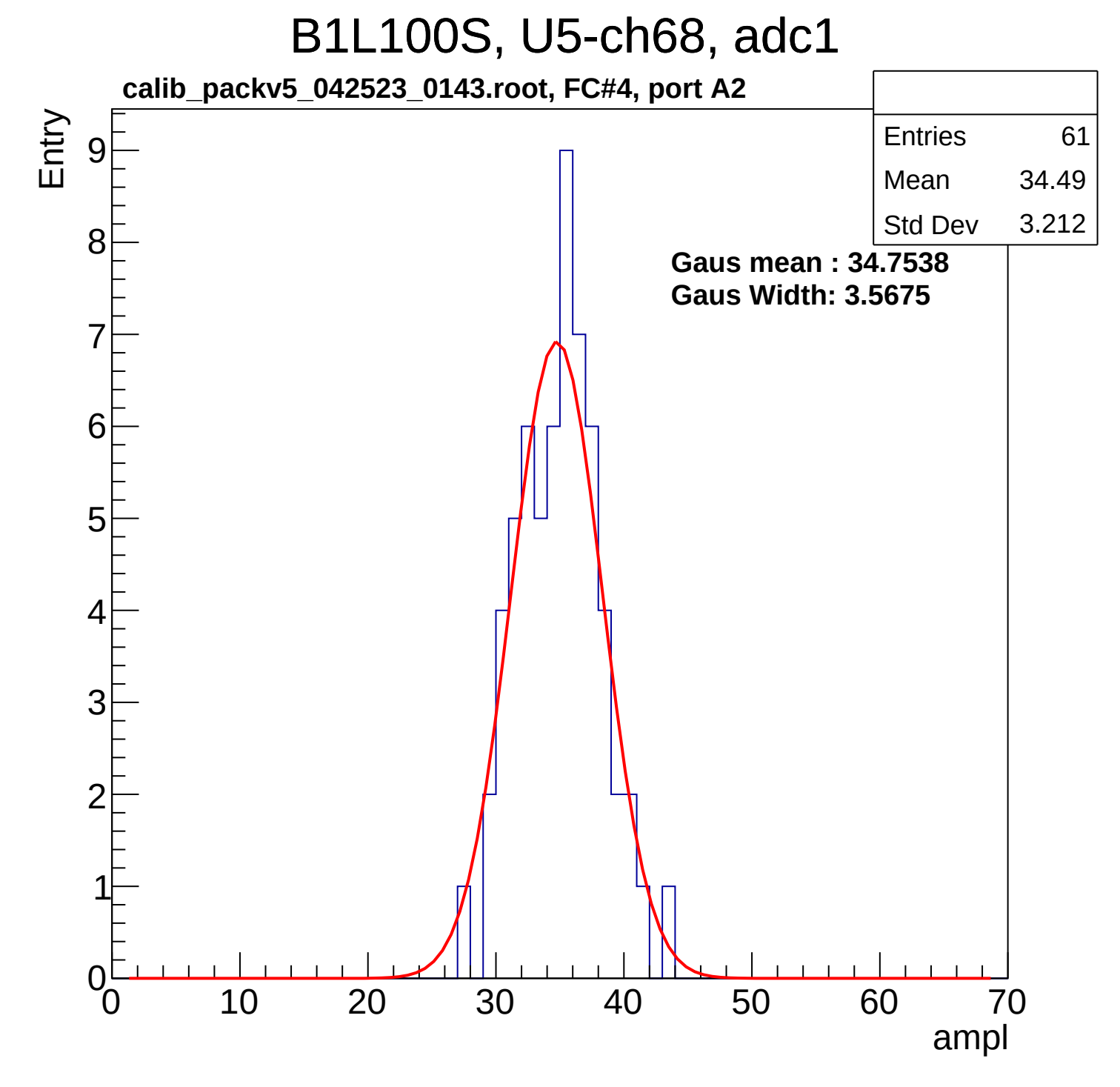
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch68, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 79
Mean 27.25
Std Dev 4.729
Gaus mean : 27.7991
Gaus Width: 4.6080
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch68, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 34.49
Std Dev 3.212
Gaus mean : 34.7538
Gaus Width: 3.5675
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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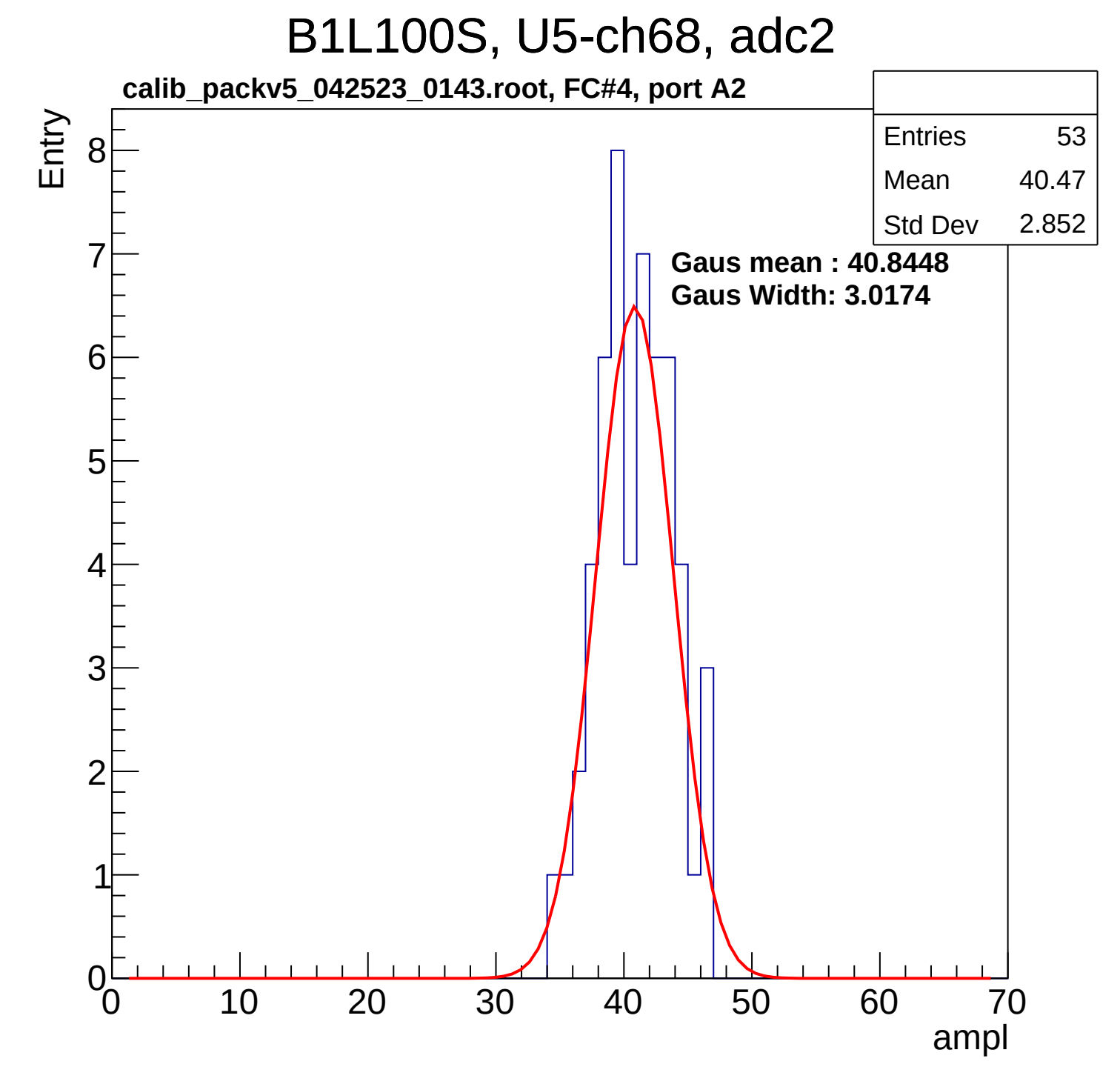
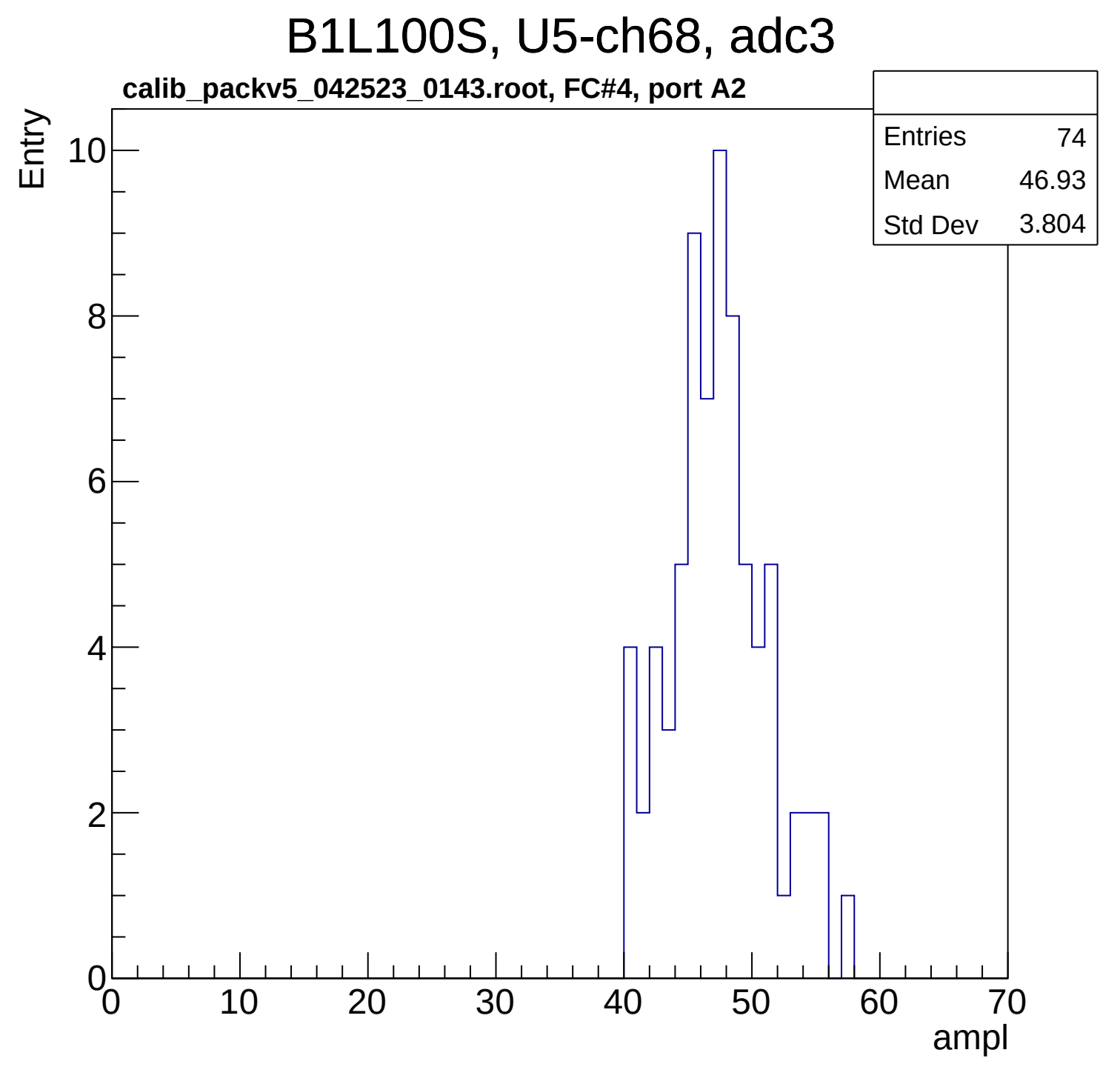
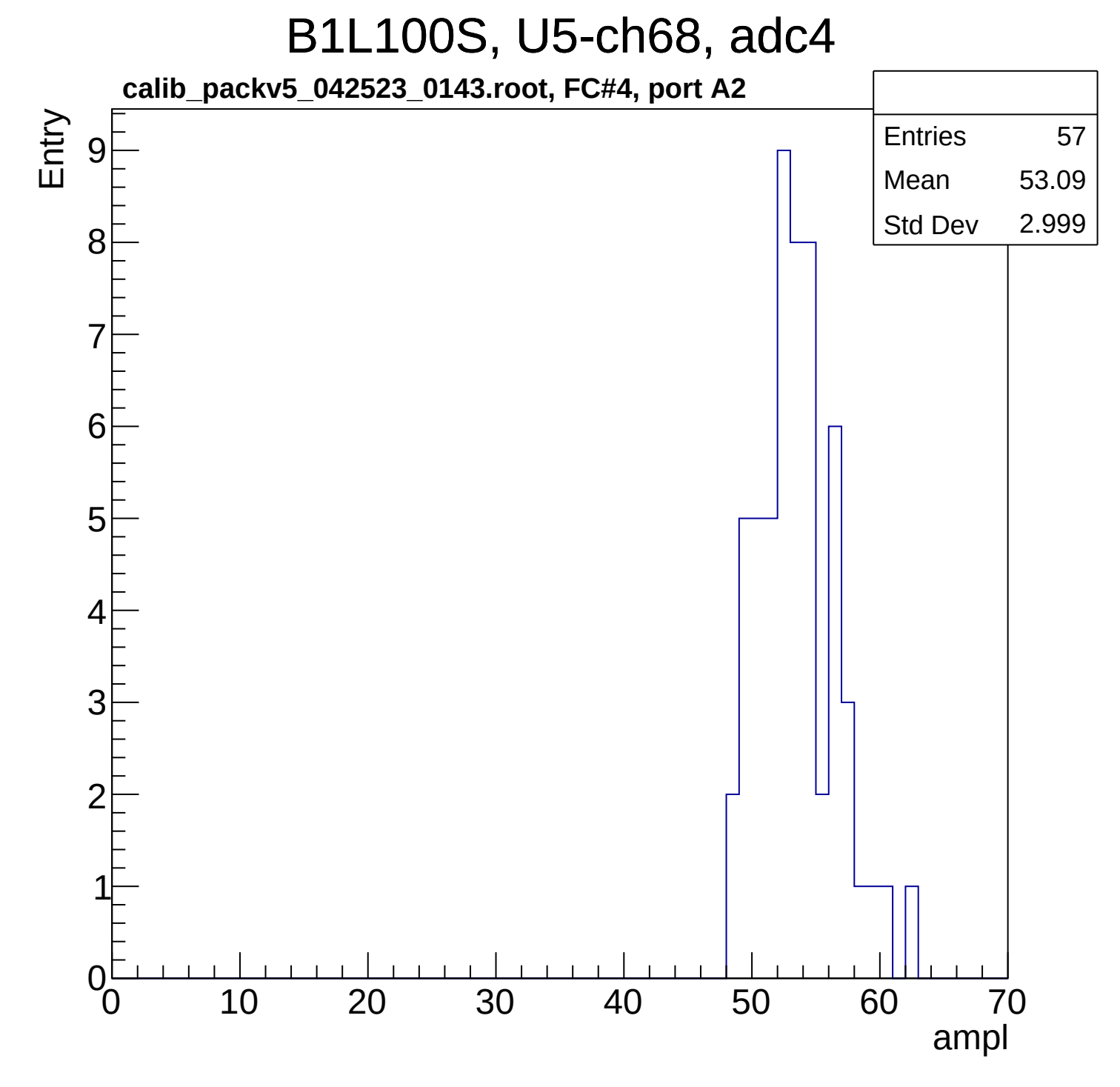
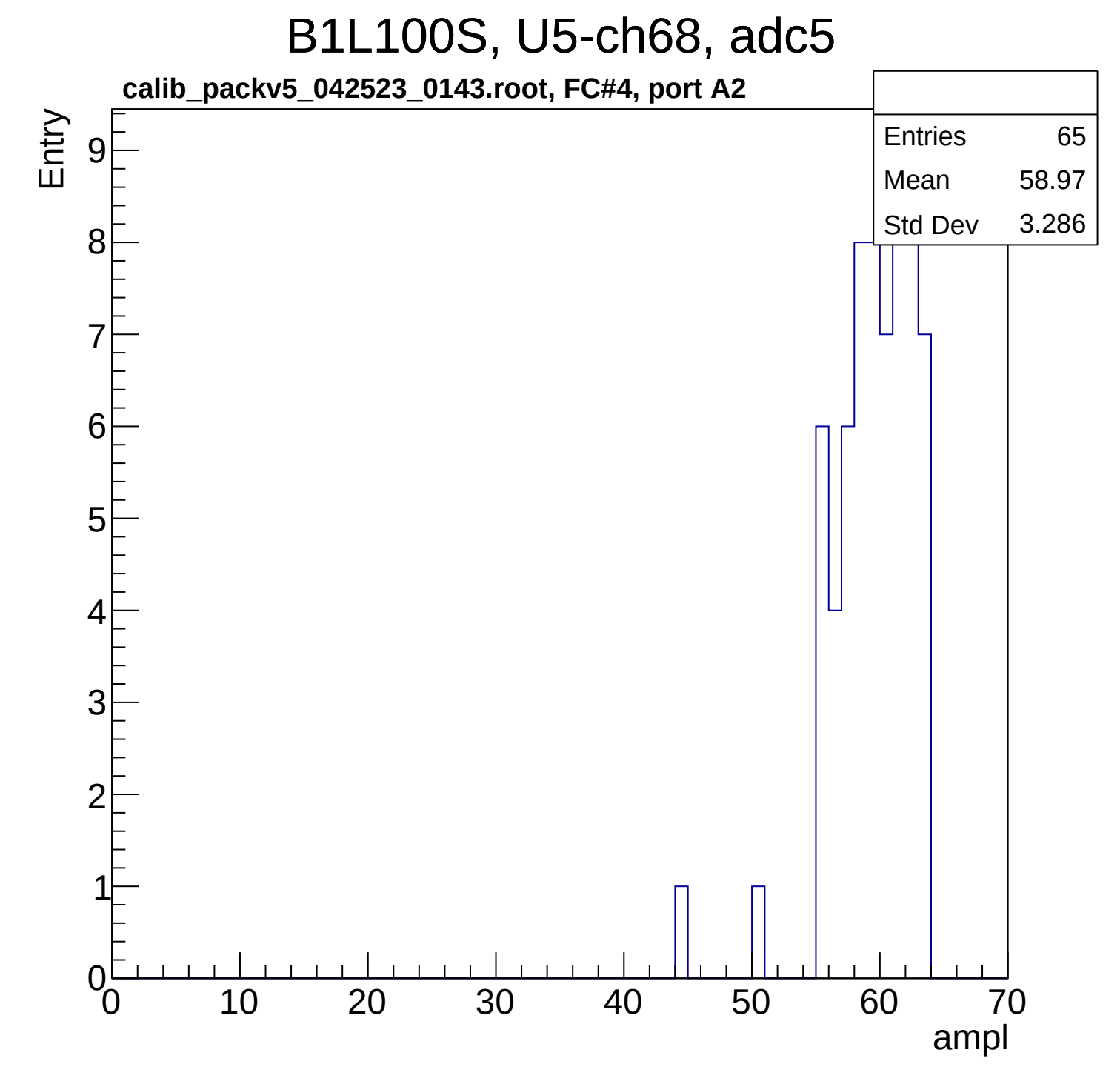
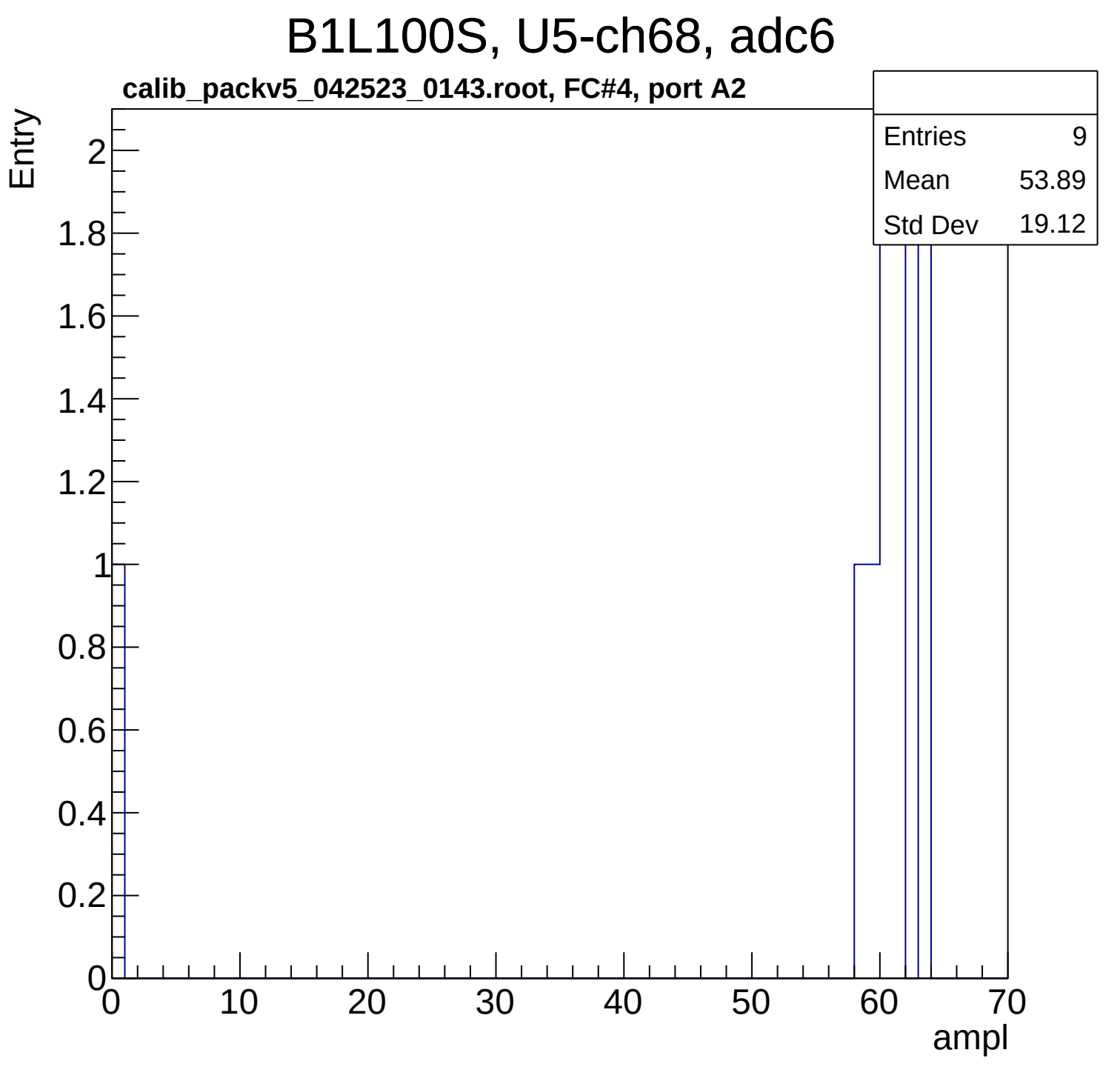
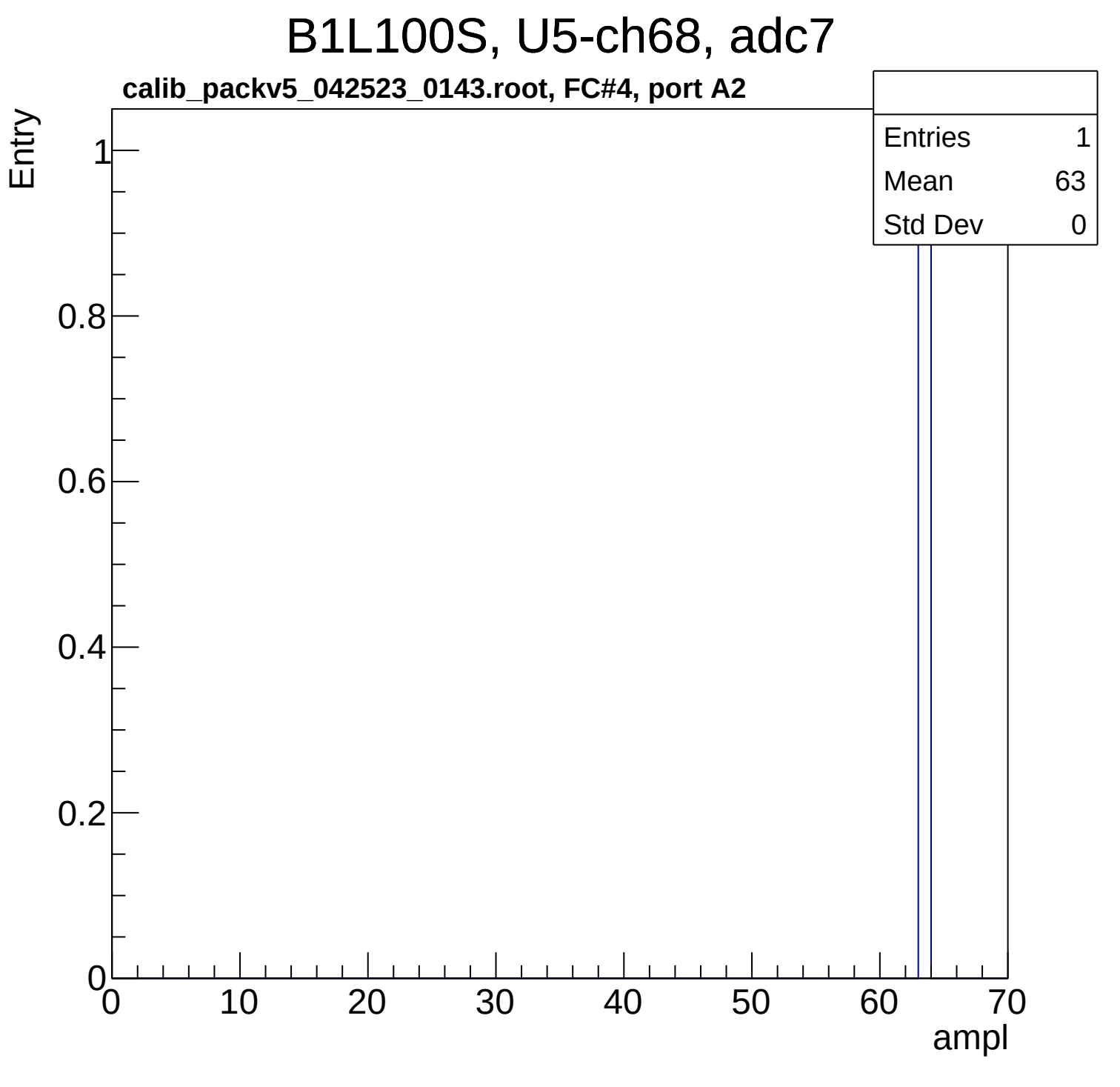

B1L100S, U5-ch68, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 40.47
Std Dev 2.852
Gaus mean : 40.8448
Gaus Width: 3.0174
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

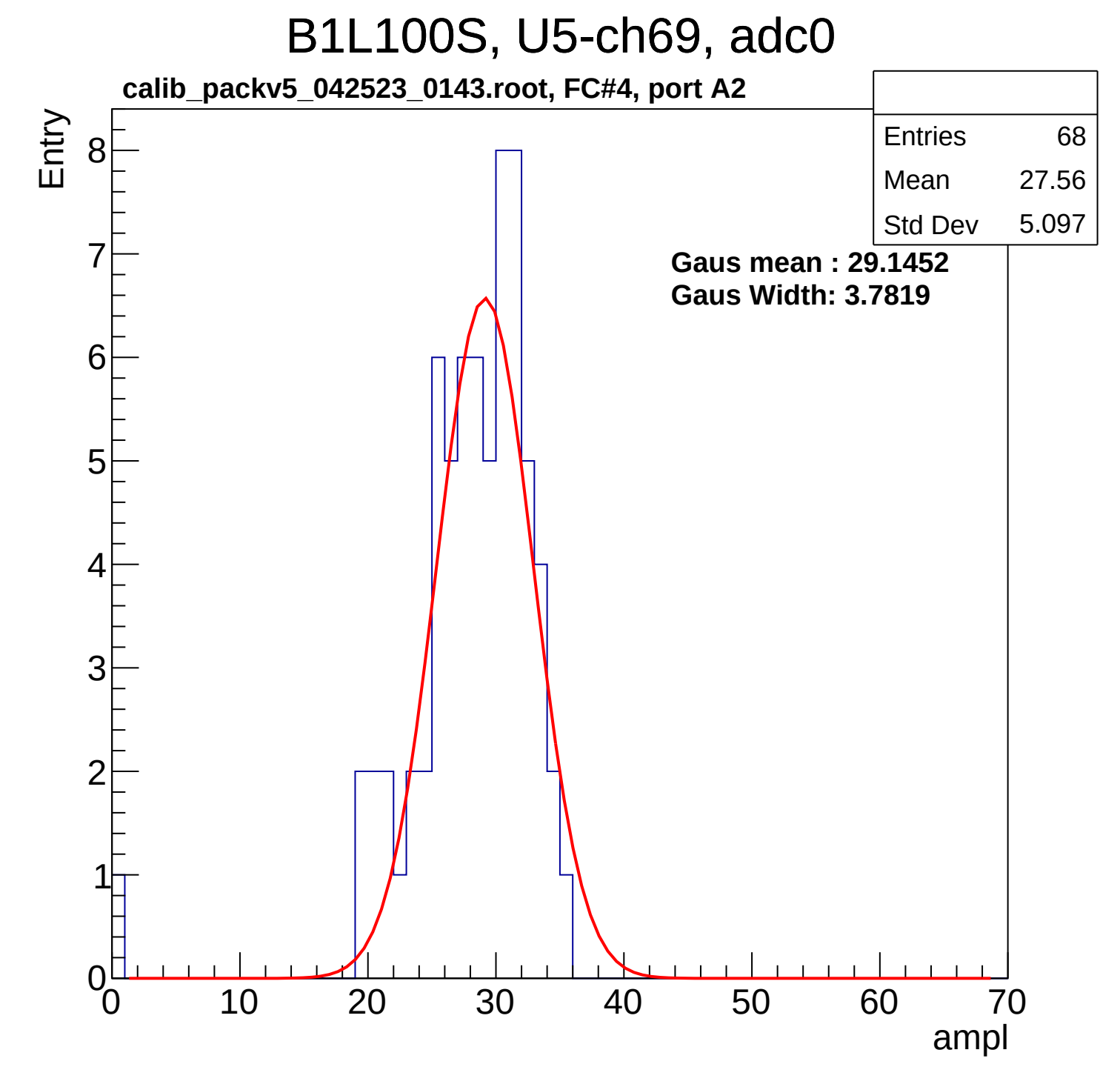

B1L100S, U5-ch68, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 74
Mean 46.93
Std Dev 3.804
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

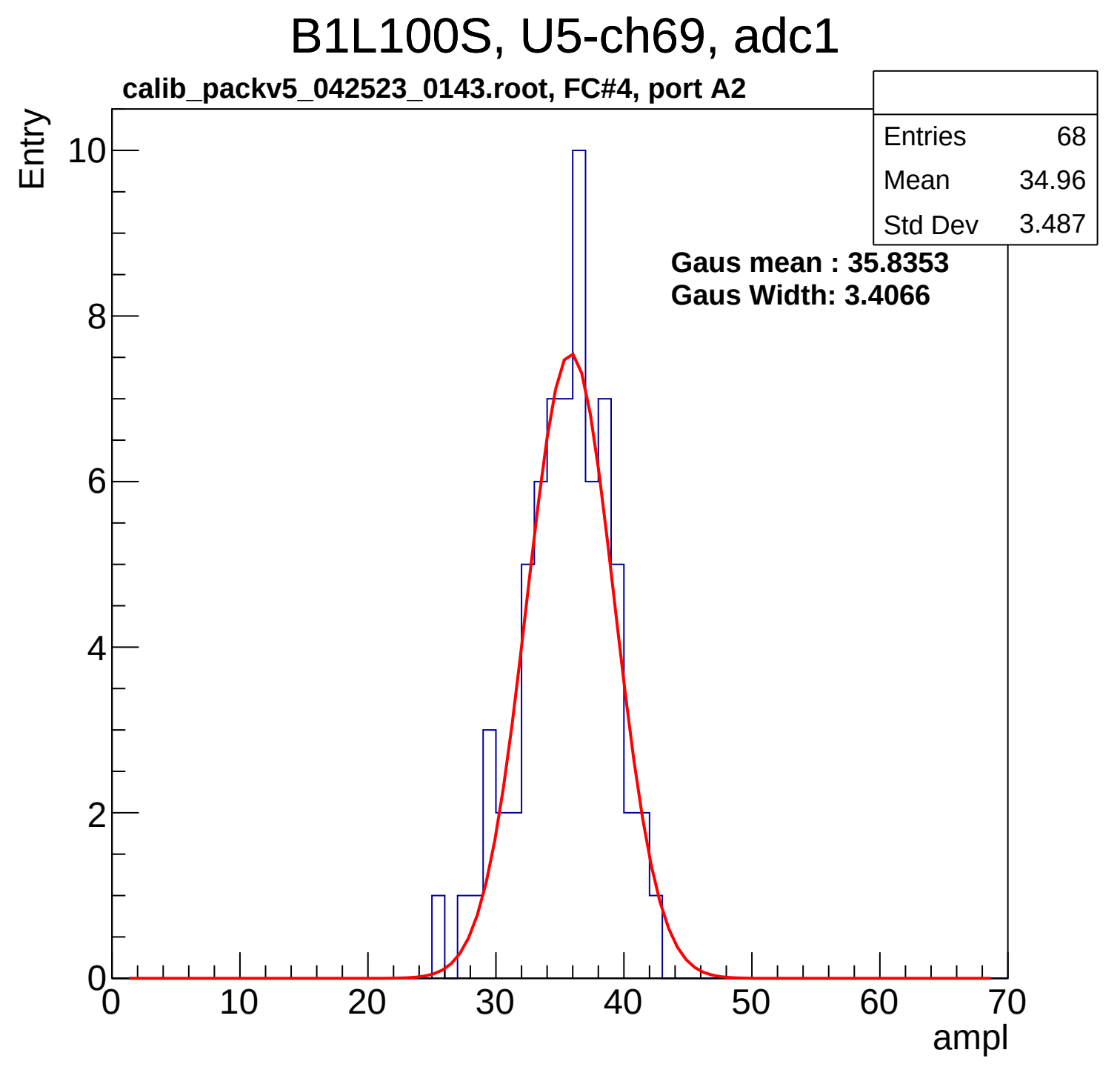

B1L100S, U5-ch68, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 53.09
Std Dev 2.999
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

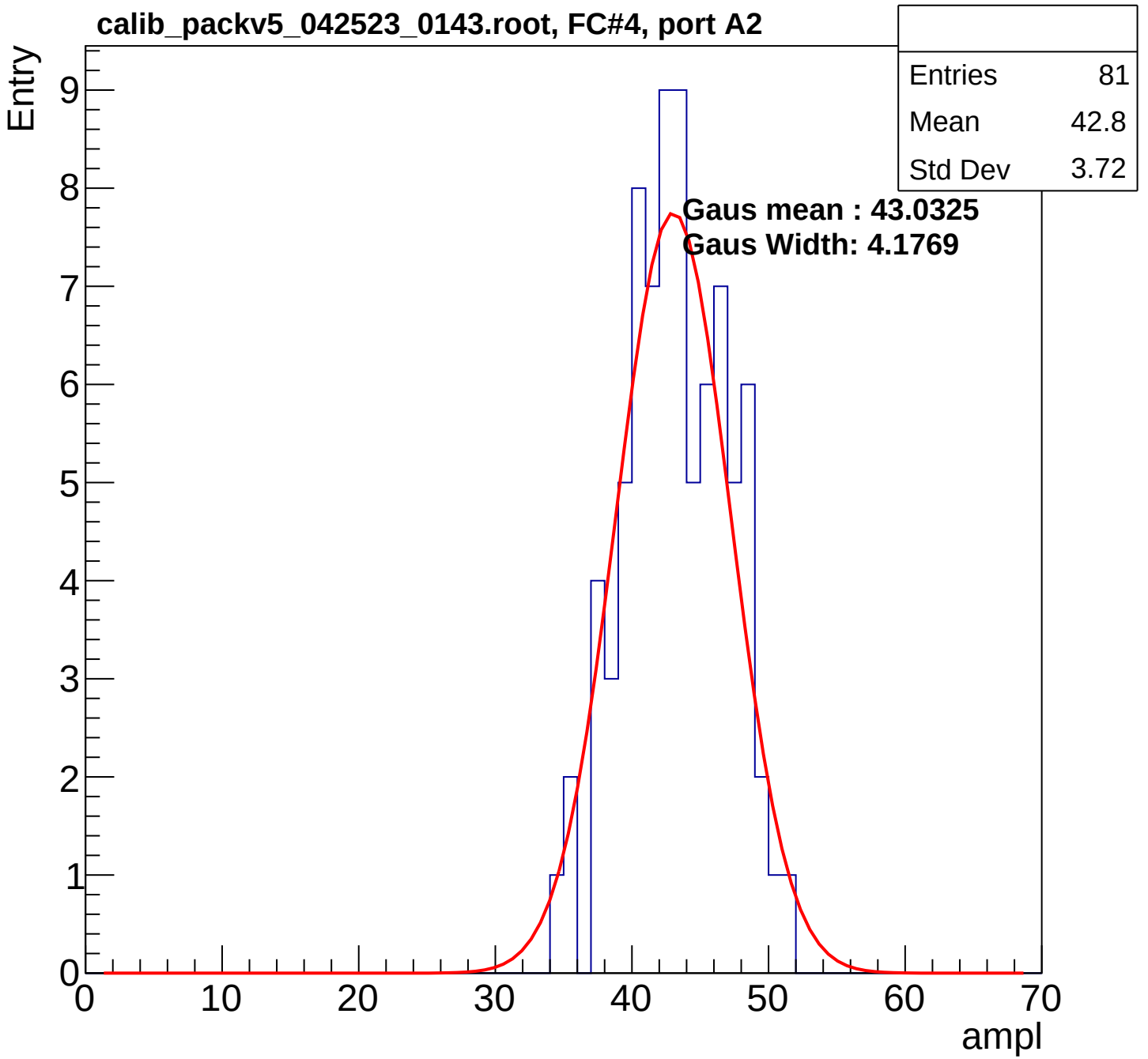

B1L100S, U5-ch68, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 58.97
Std Dev 3.286
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

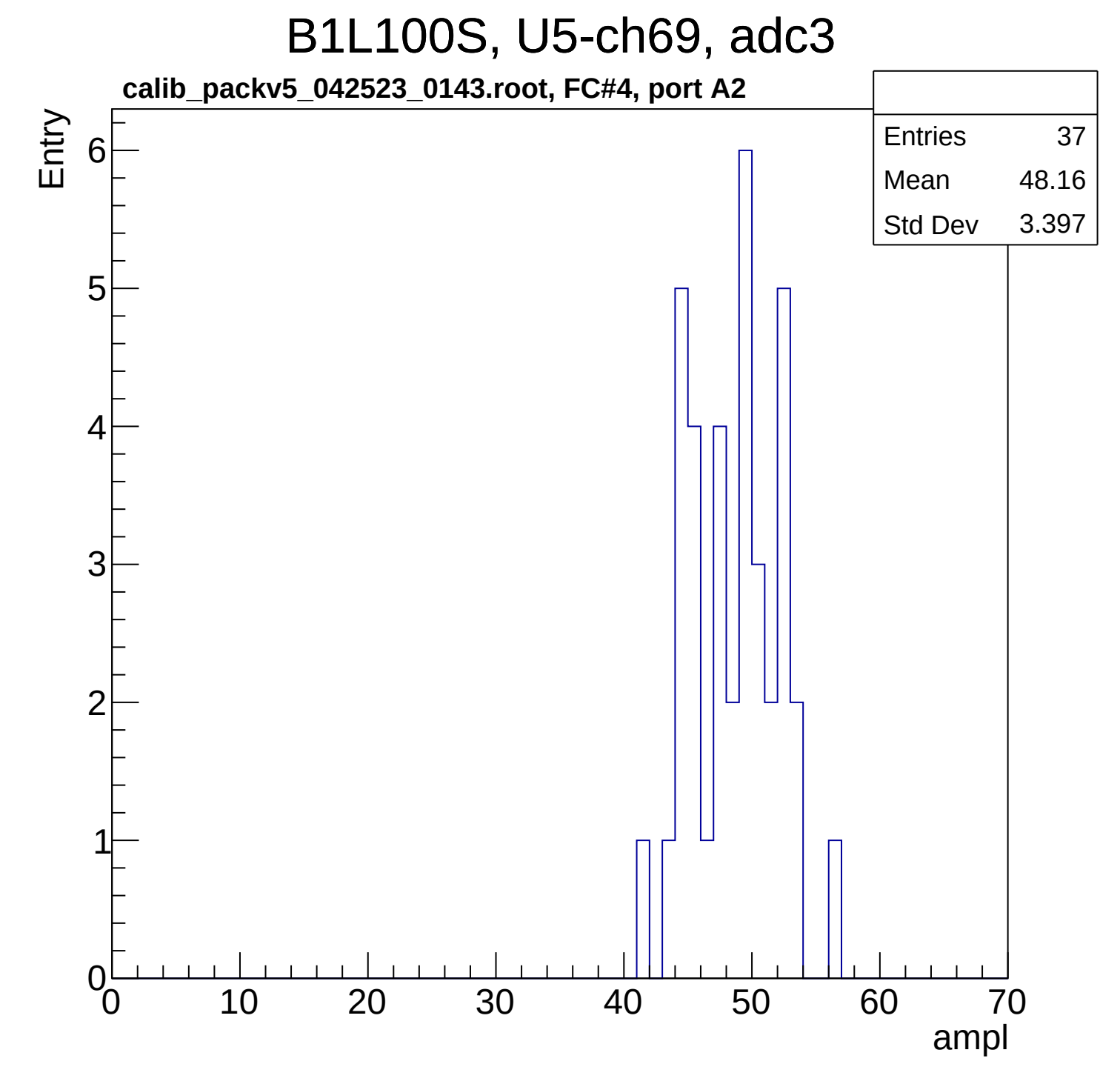

B1L100S, U5-ch68, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 9
Mean 53.89
Std Dev 19.12
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

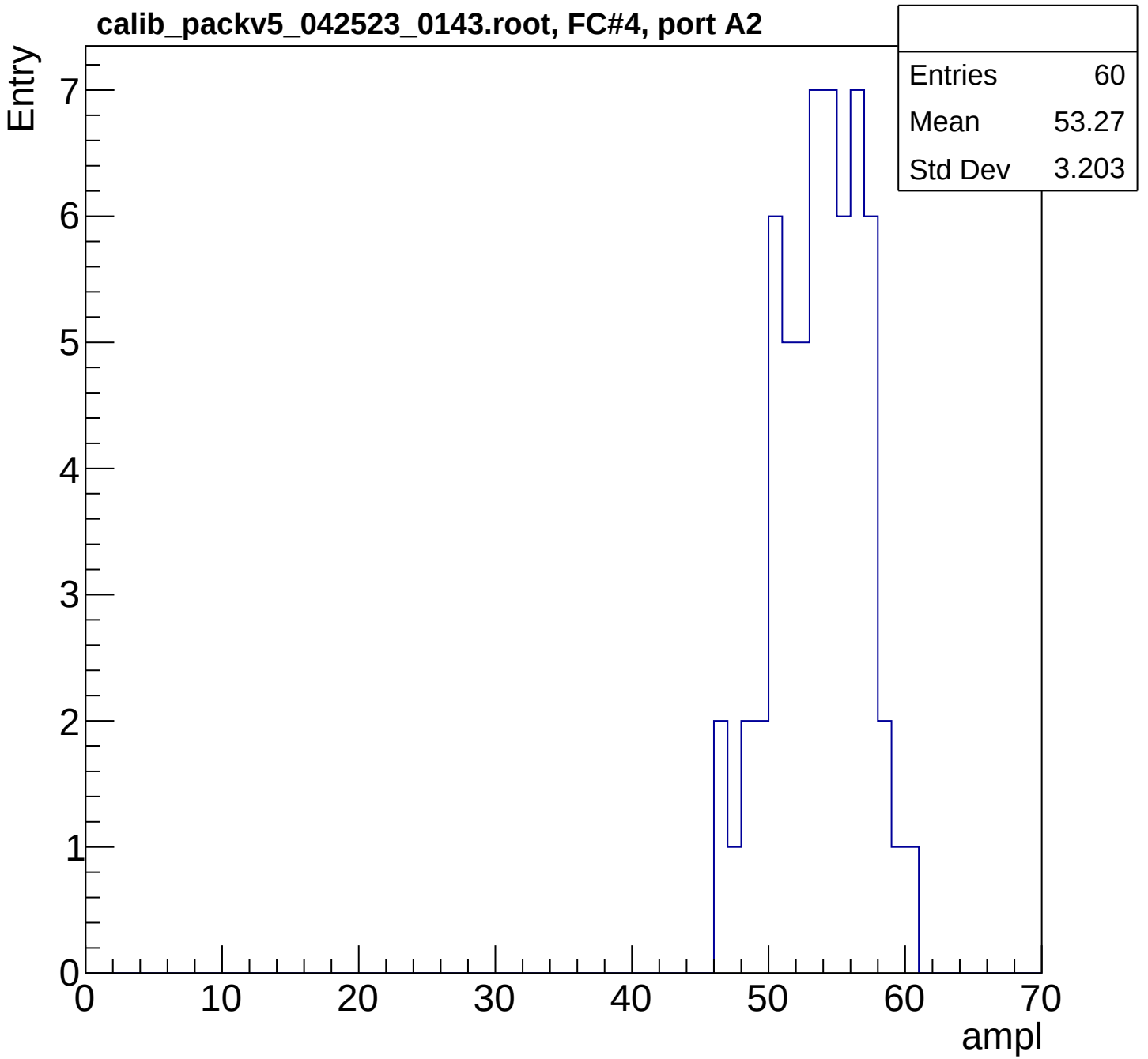

B1L100S, U5-ch68, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

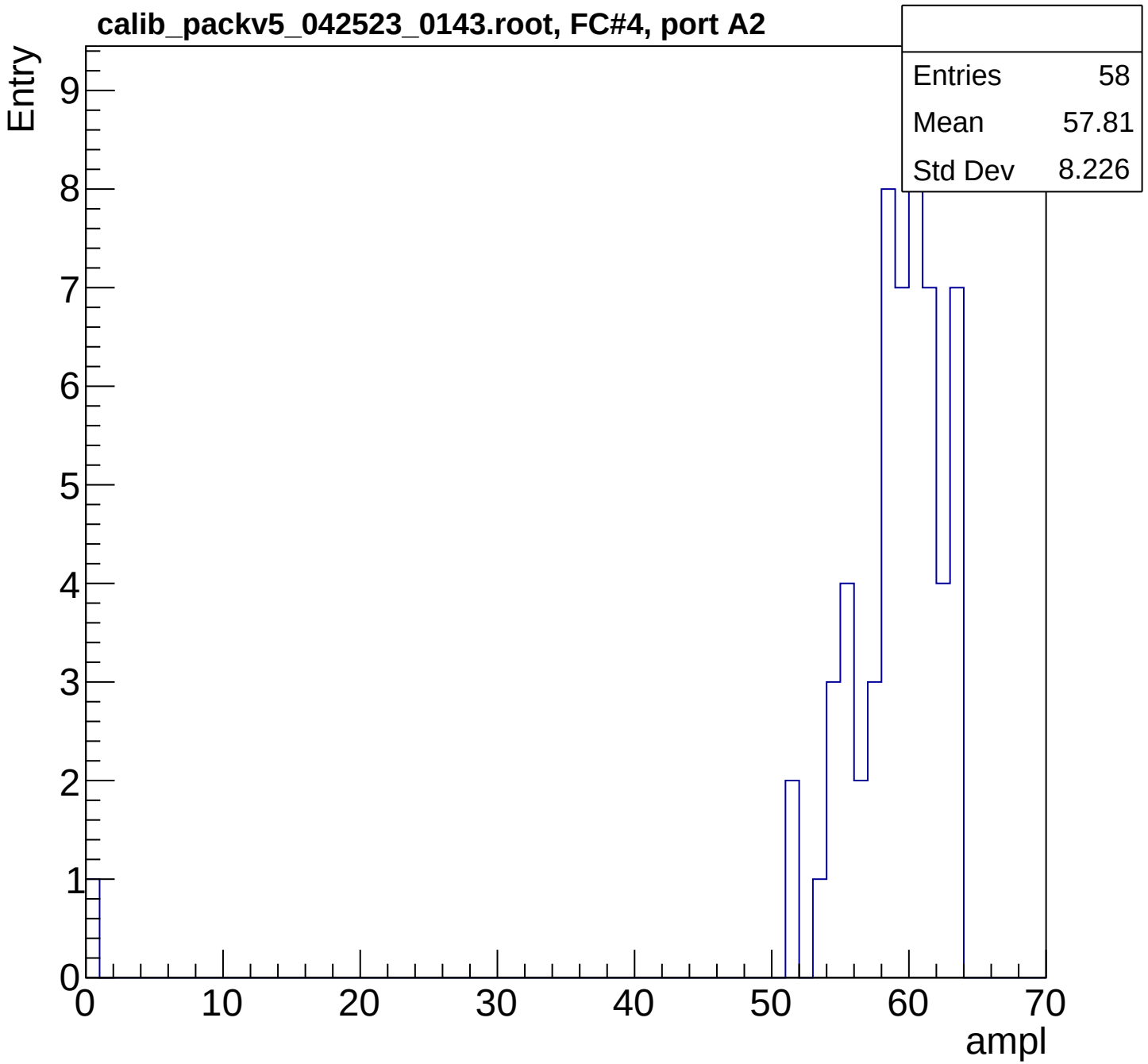

B1L100S, U5-ch69, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 27.56
Std Dev 5.097
Gaus mean : 29.1452
Gaus Width: 3.7819
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch69, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 34.96
Std Dev 3.487
Gaus mean : 35.8353
Gaus Width: 3.4066
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch69, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 81
Mean 42.8
Std Dev 3.72
Gaus mean : 43.0325
Gaus Width: 4.1769
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch69, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 37
Mean 48.16
Std Dev 3.397
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L100S, U5-ch69, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 53.27
Std Dev 3.203
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U5-ch69, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 57.81
Std Dev 8.226
Entry
ampl
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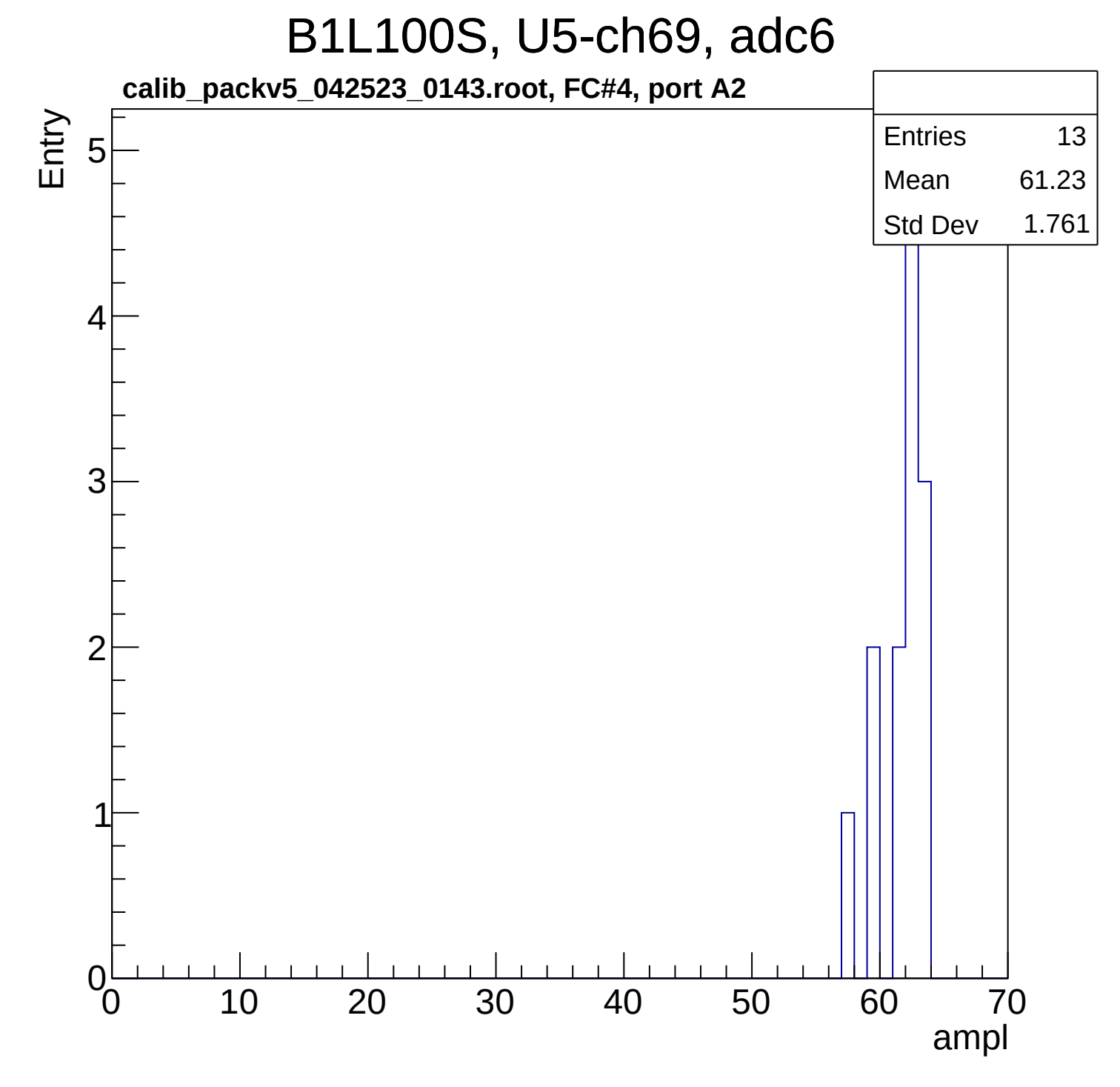
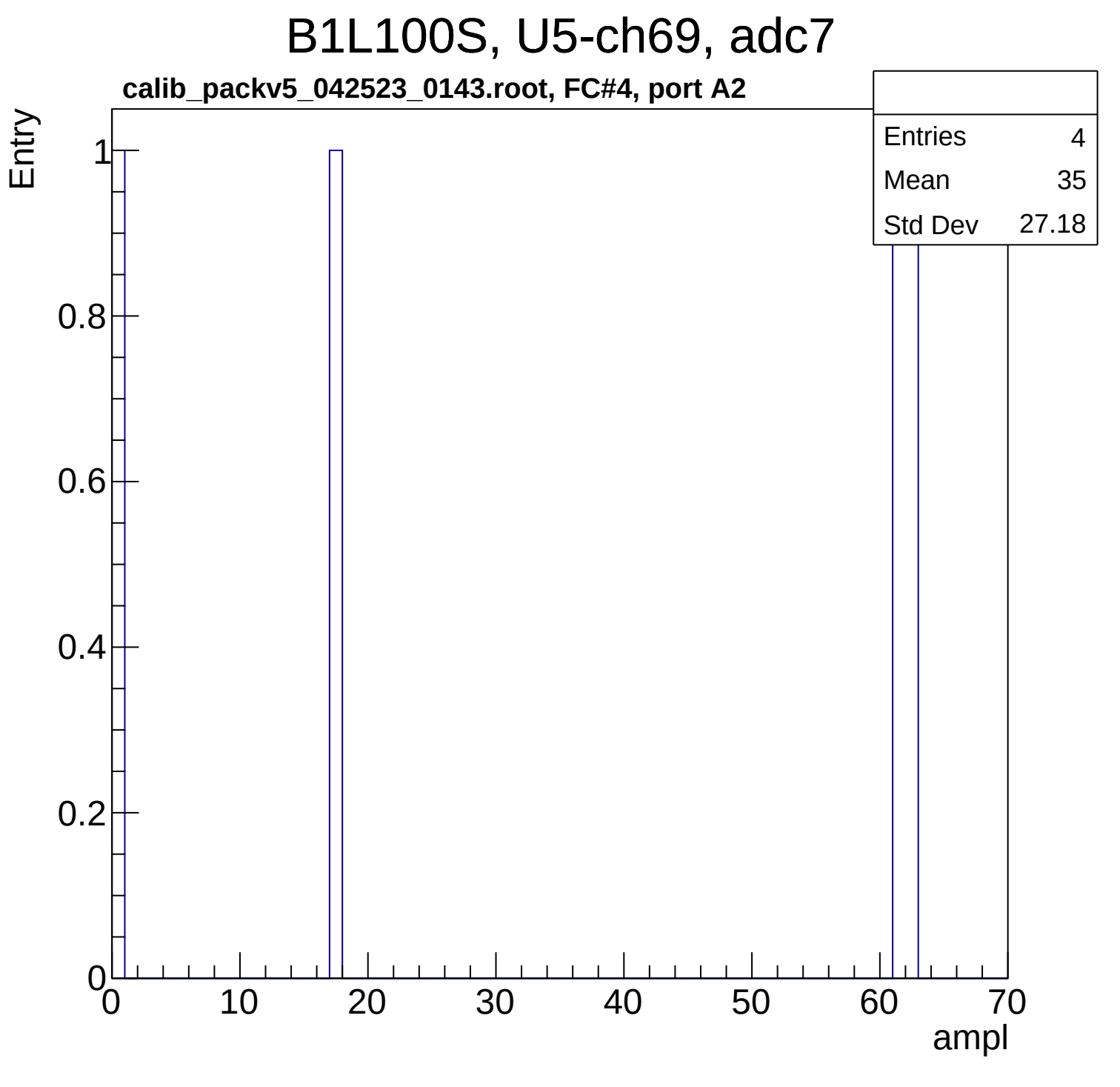
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch69, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 13
Mean 61.23
Std Dev 1.761
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch69, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 4
Mean 35
Std Dev 27.18
Entry
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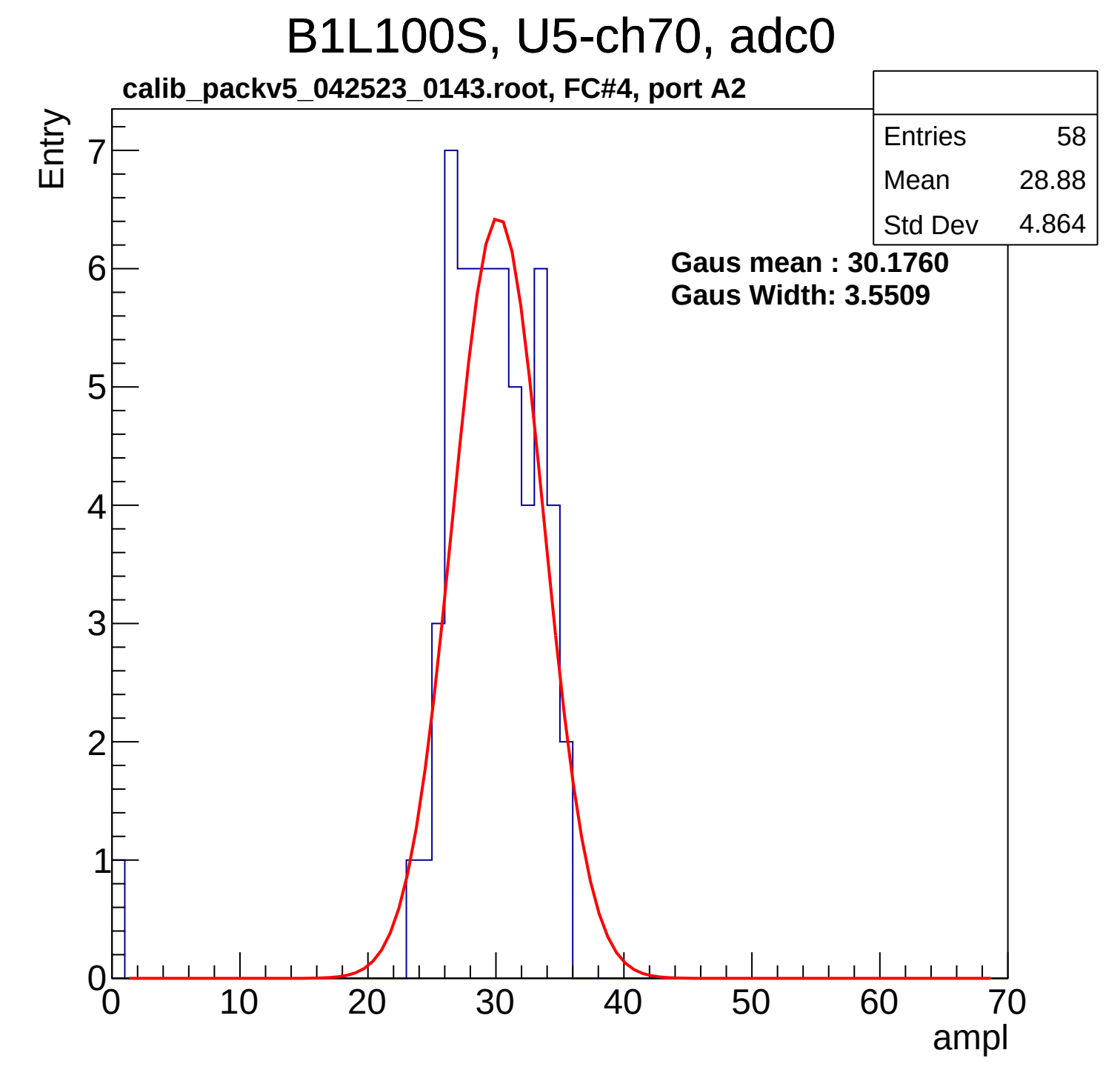
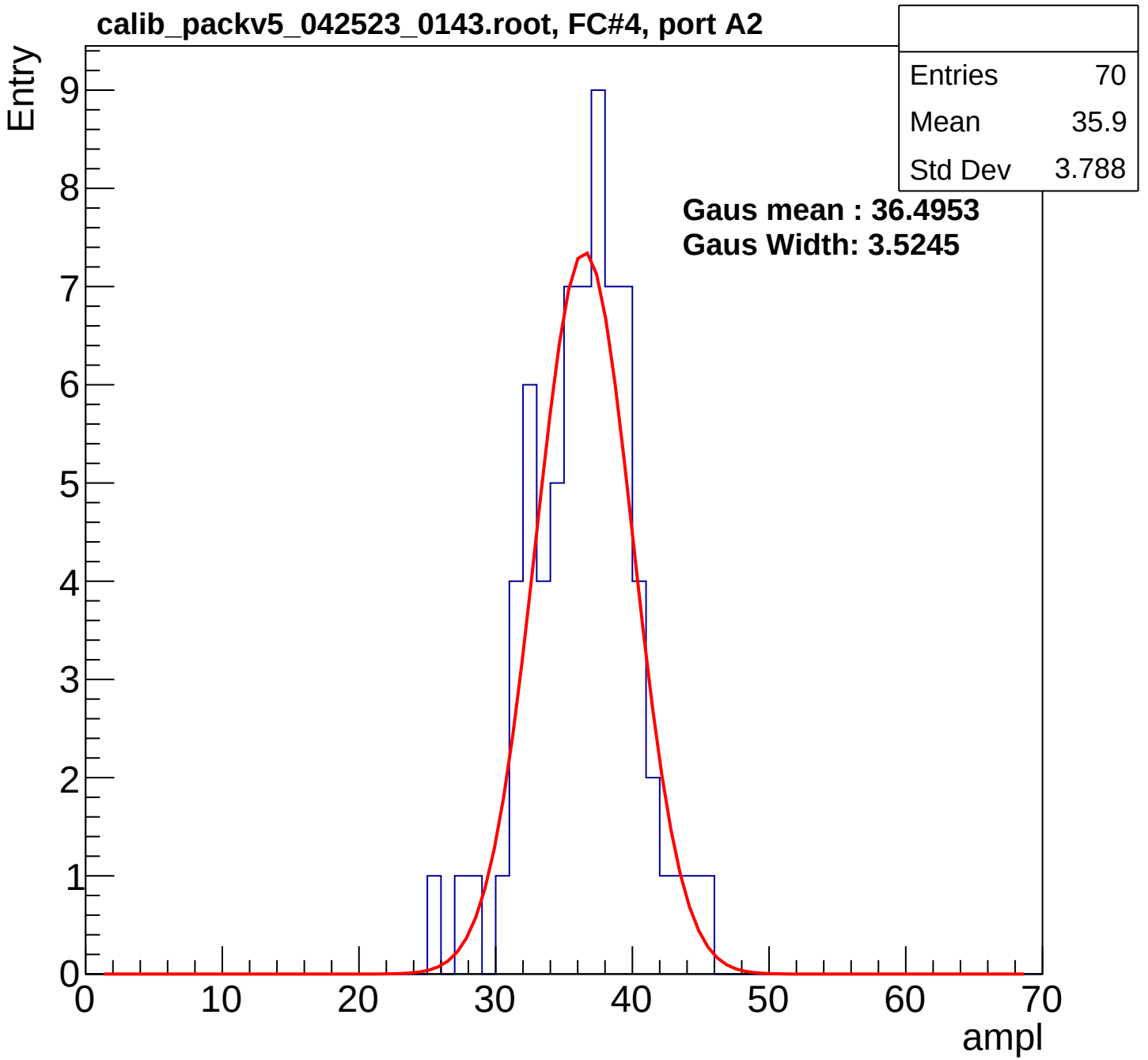
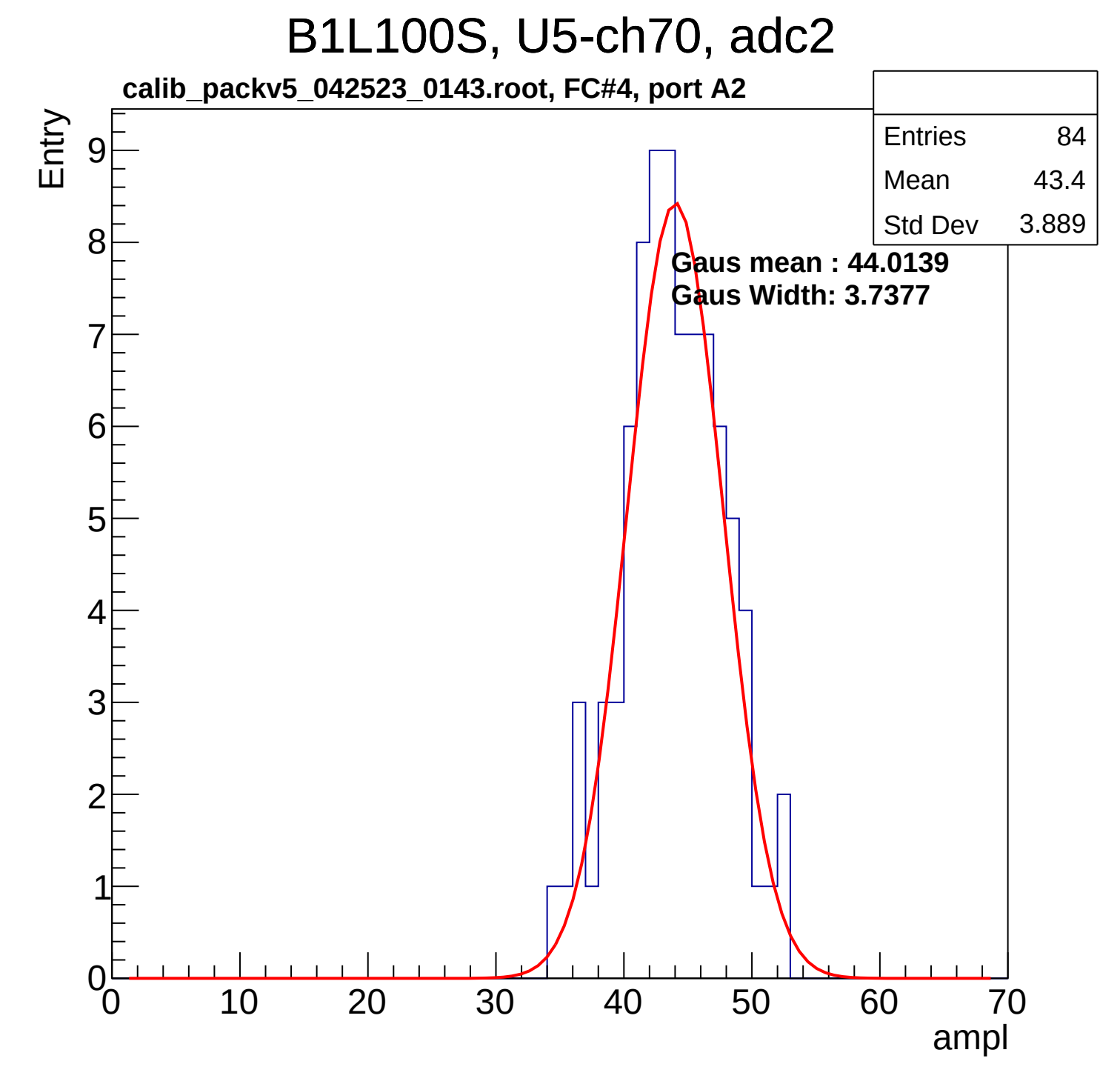
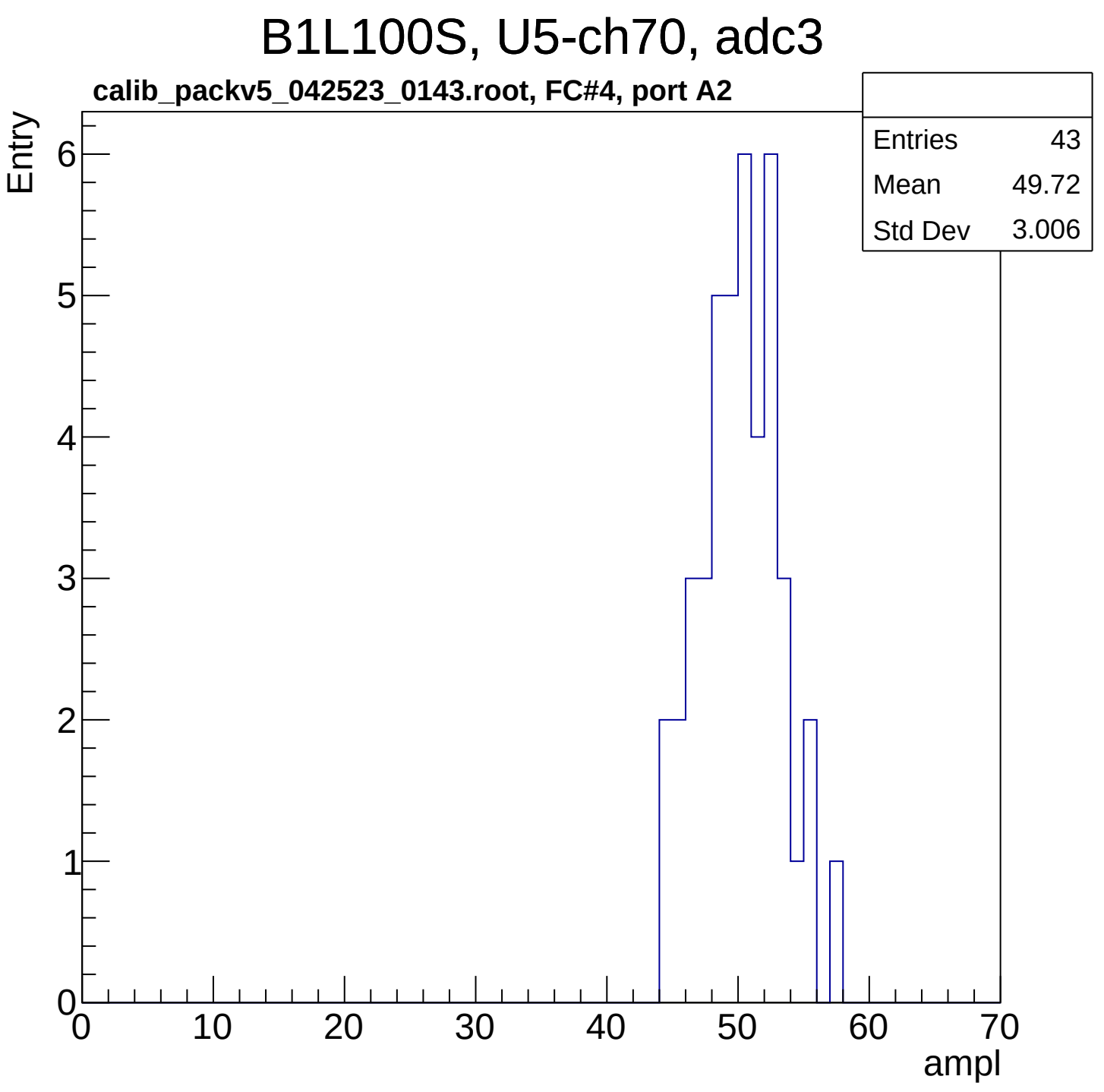
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch70, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 28.88
Std Dev 4.864
Gaus mean : 30.1760
Gaus Width: 3.5509
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U5-ch70, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 35.9
Std Dev 3.788
Gaus mean : 36.4953
Gaus Width: 3.5245
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch70, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 84
Mean 43.4
Std Dev 3.889
Gaus mean : 44.0139
Gaus Width: 3.7377
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch70, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 43
Mean 49.72
Std Dev 3.006
Entry
0
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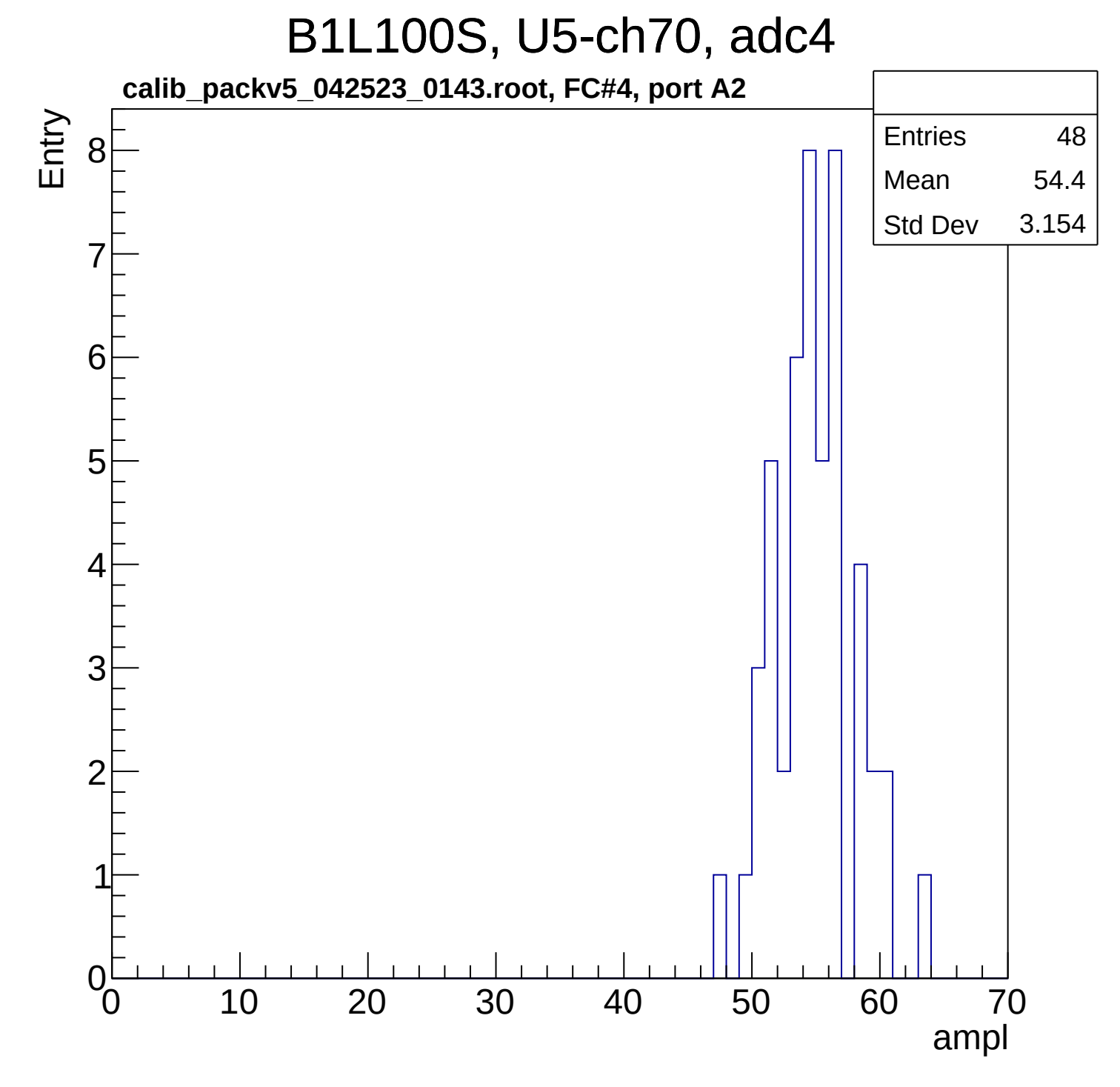
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch70, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 48
Mean 54.4
Std Dev 3.154
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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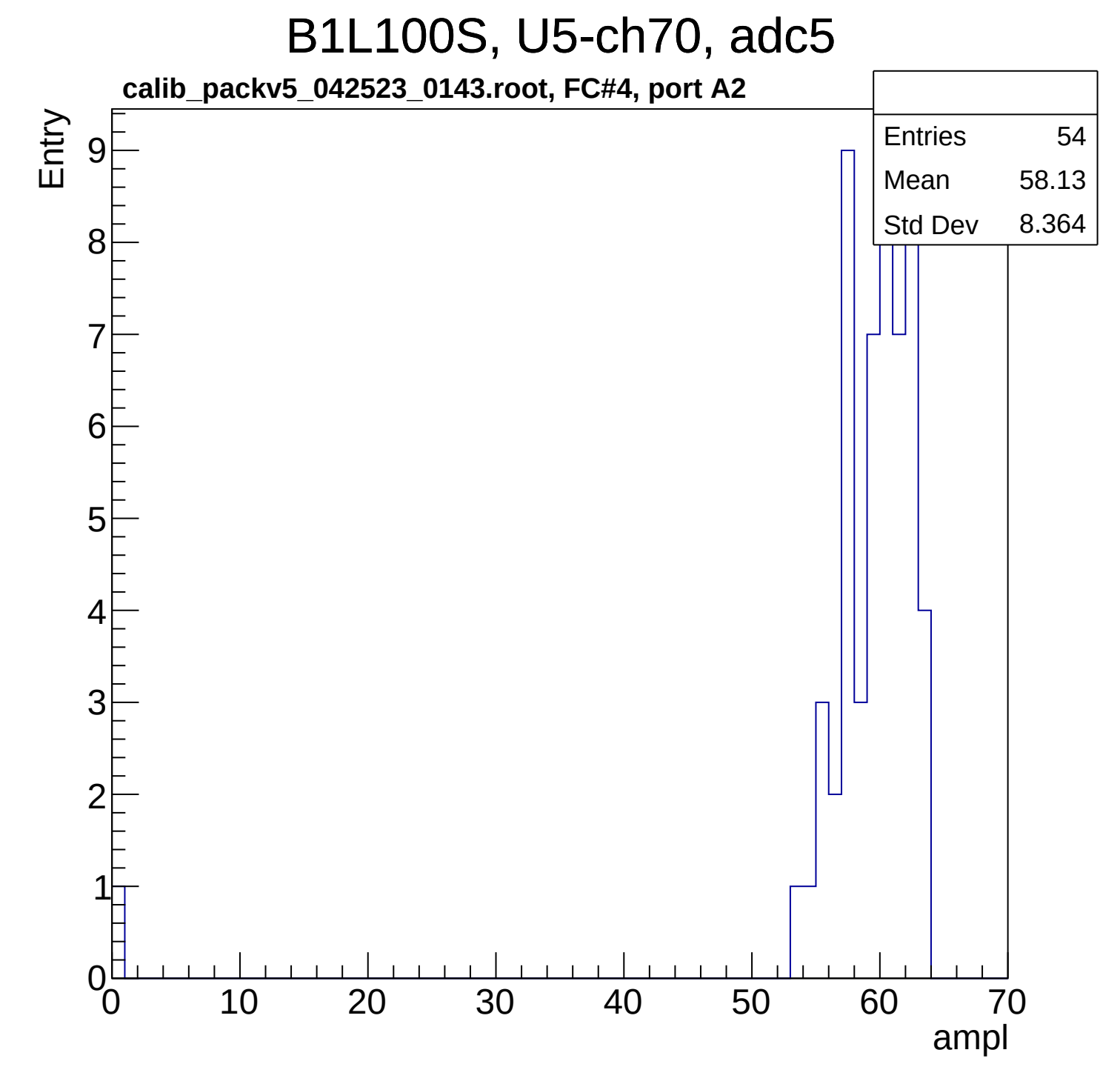
40
50
60
70


B1L100S, U5-ch70, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 58.13
Std Dev 8.364
Entry
ampl
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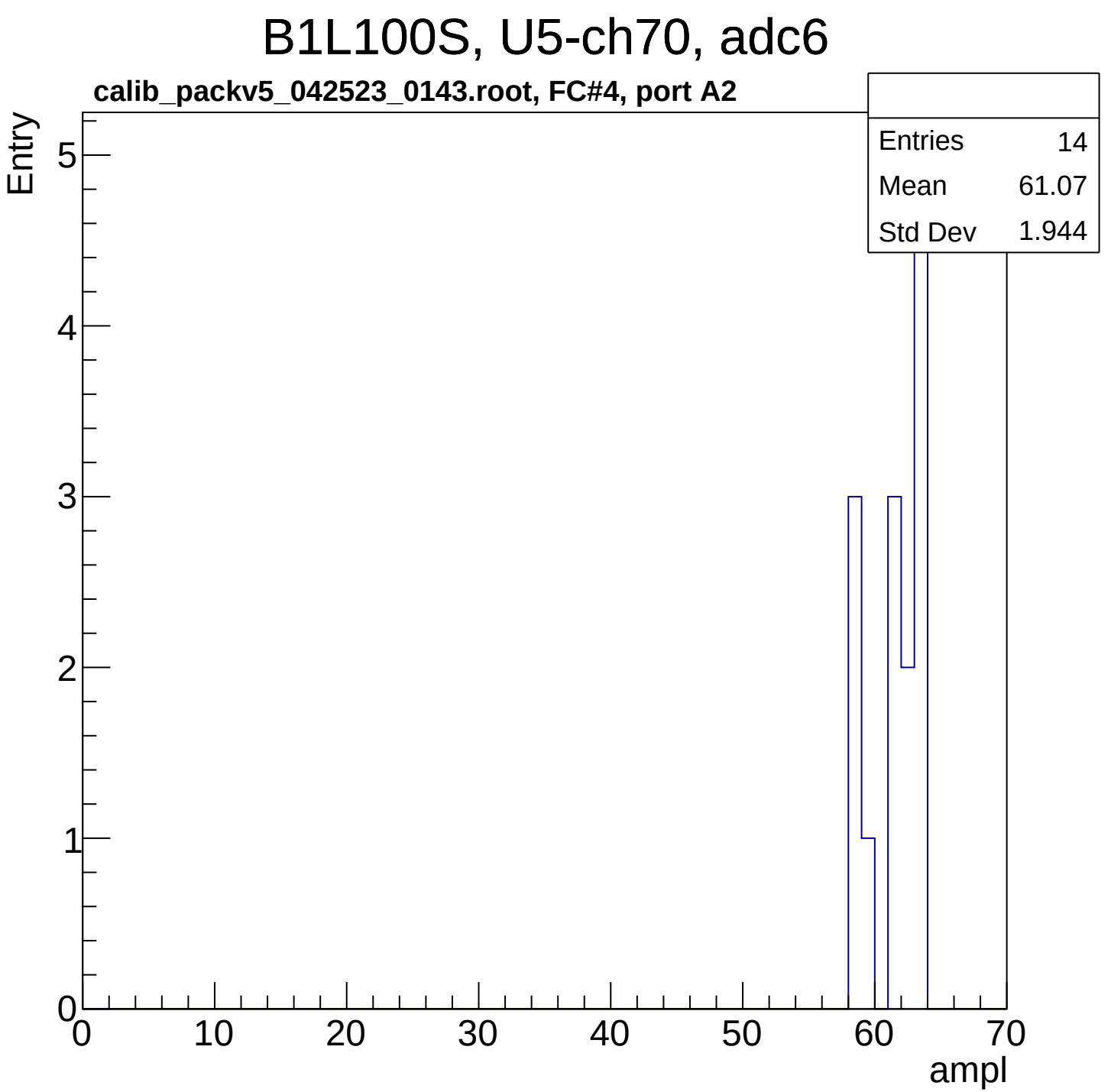
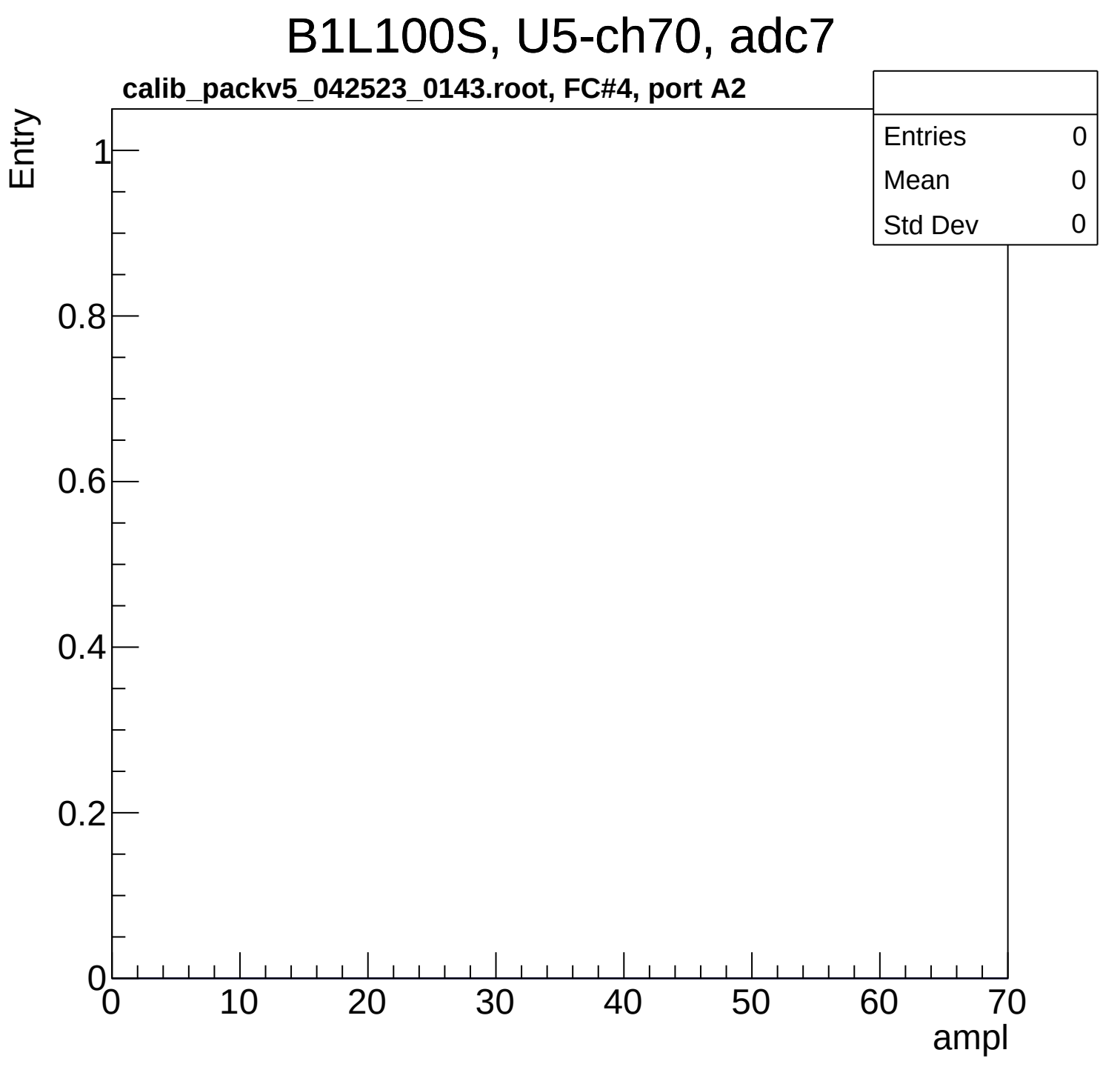
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch70, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 14
Mean 61.07
Std Dev 1.944
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch70, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
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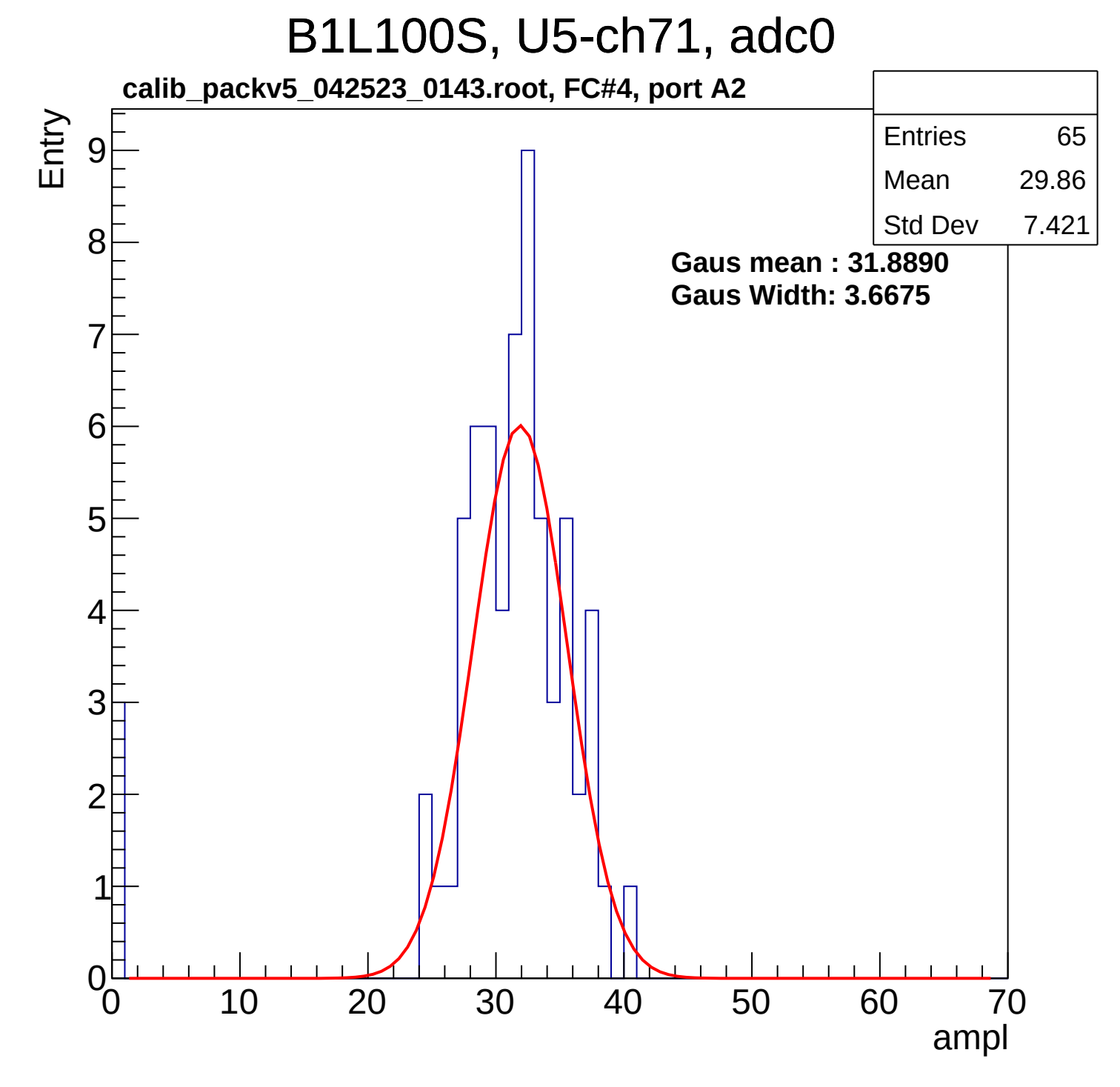
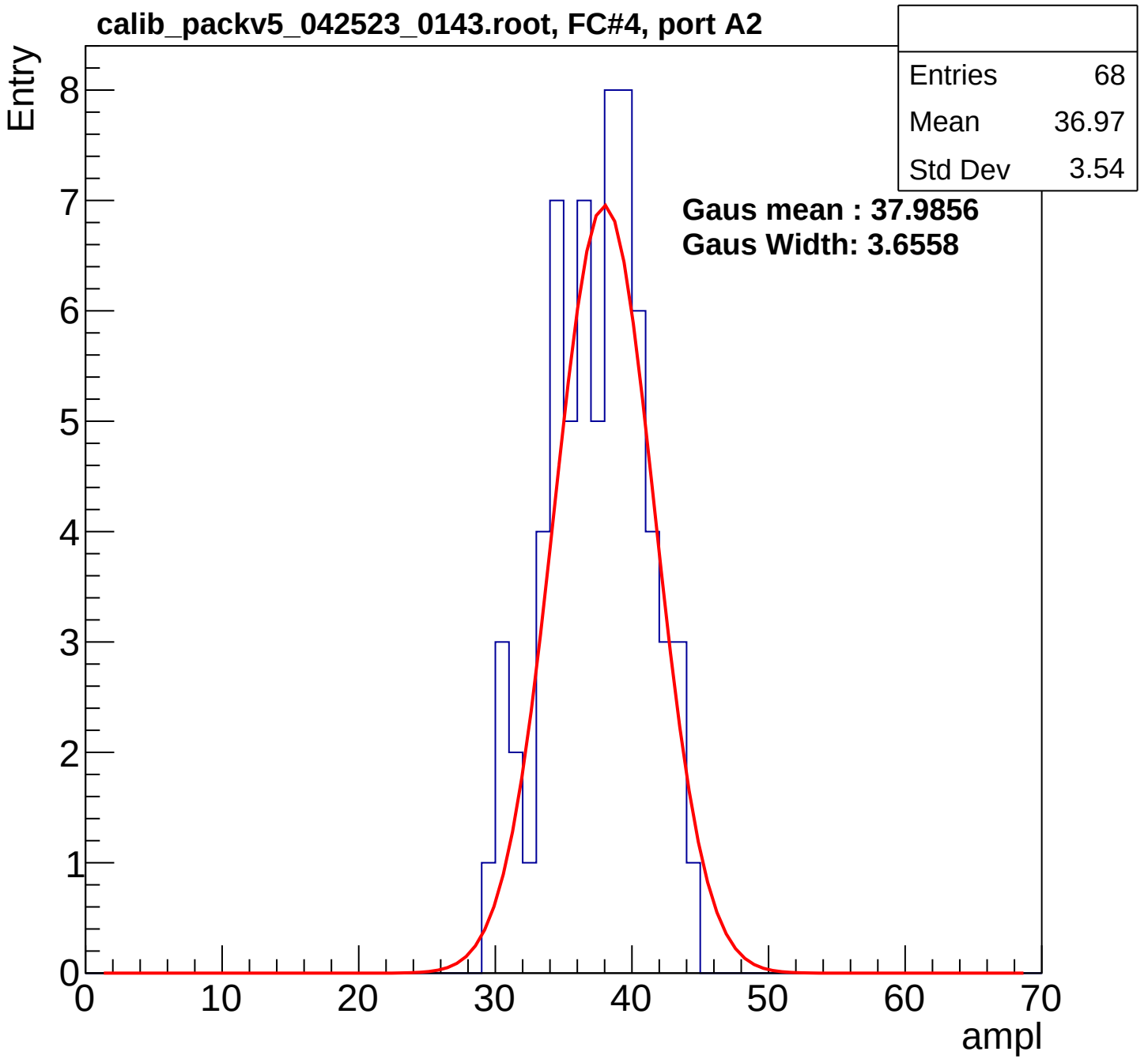
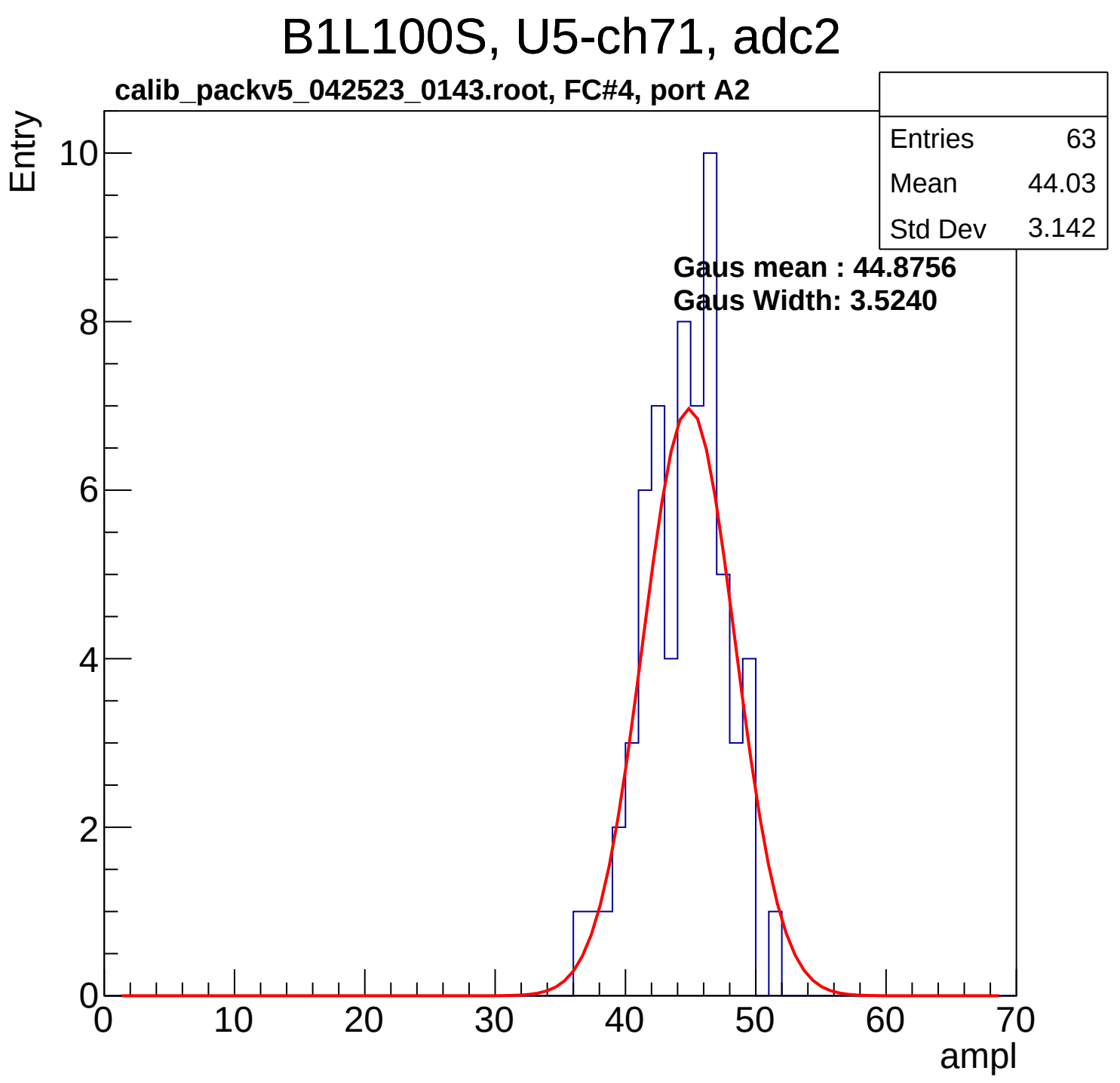
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch71, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 29.86
Std Dev 7.421
Gaus mean : 31.8890
Gaus Width: 3.6675
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch71, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 36.97
Std Dev 3.54
Gaus mean : 37.9856
Gaus Width: 3.6558
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch71, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 44.03
Std Dev 3.142
Gaus mean : 44.8756
Gaus Width: 3.5240
Entry
ampl
0
2
4
6
8
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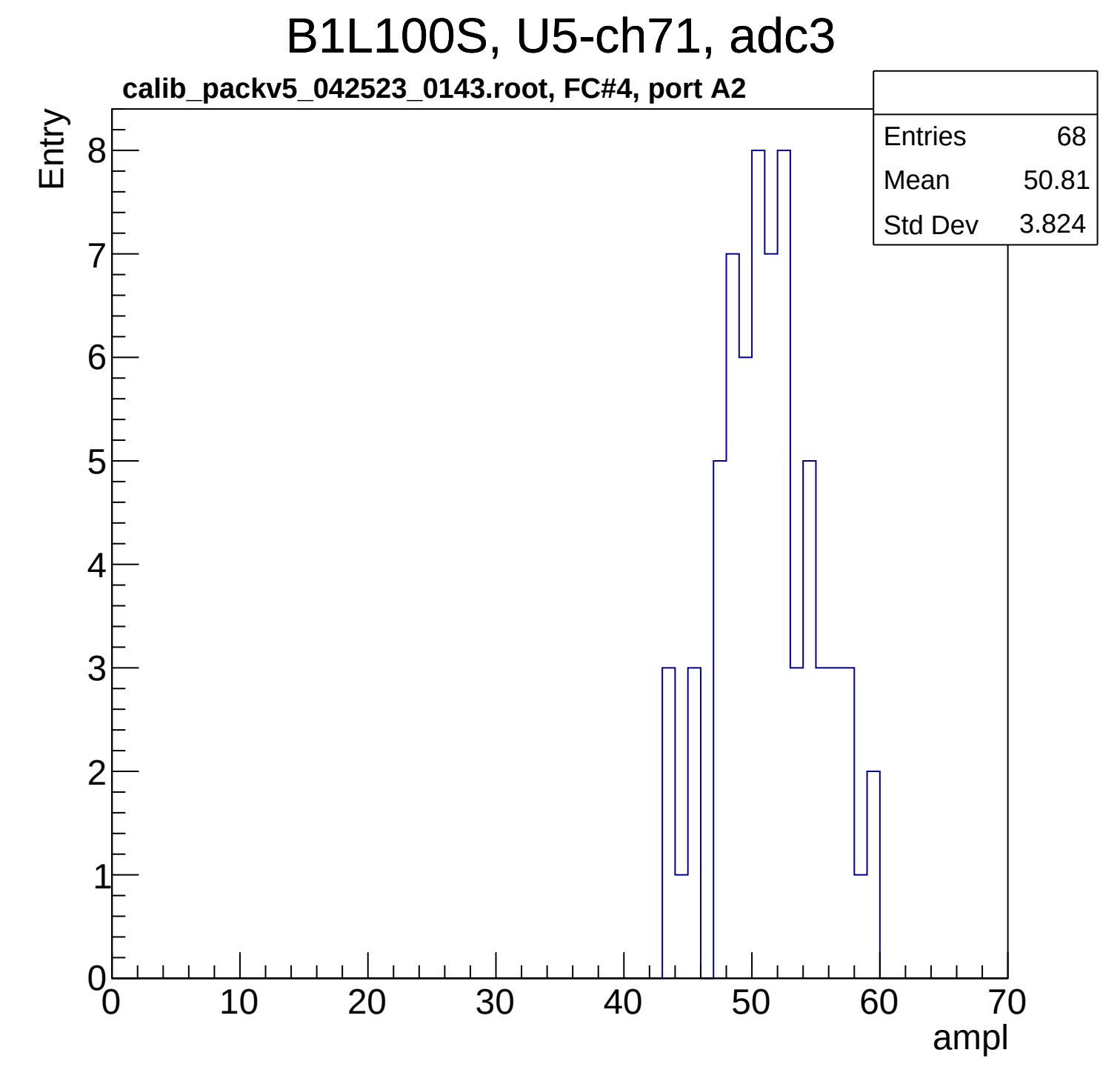
0
10
20
30
40
50
60
70


B1L100S, U5-ch71, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 50.81
Std Dev 3.824
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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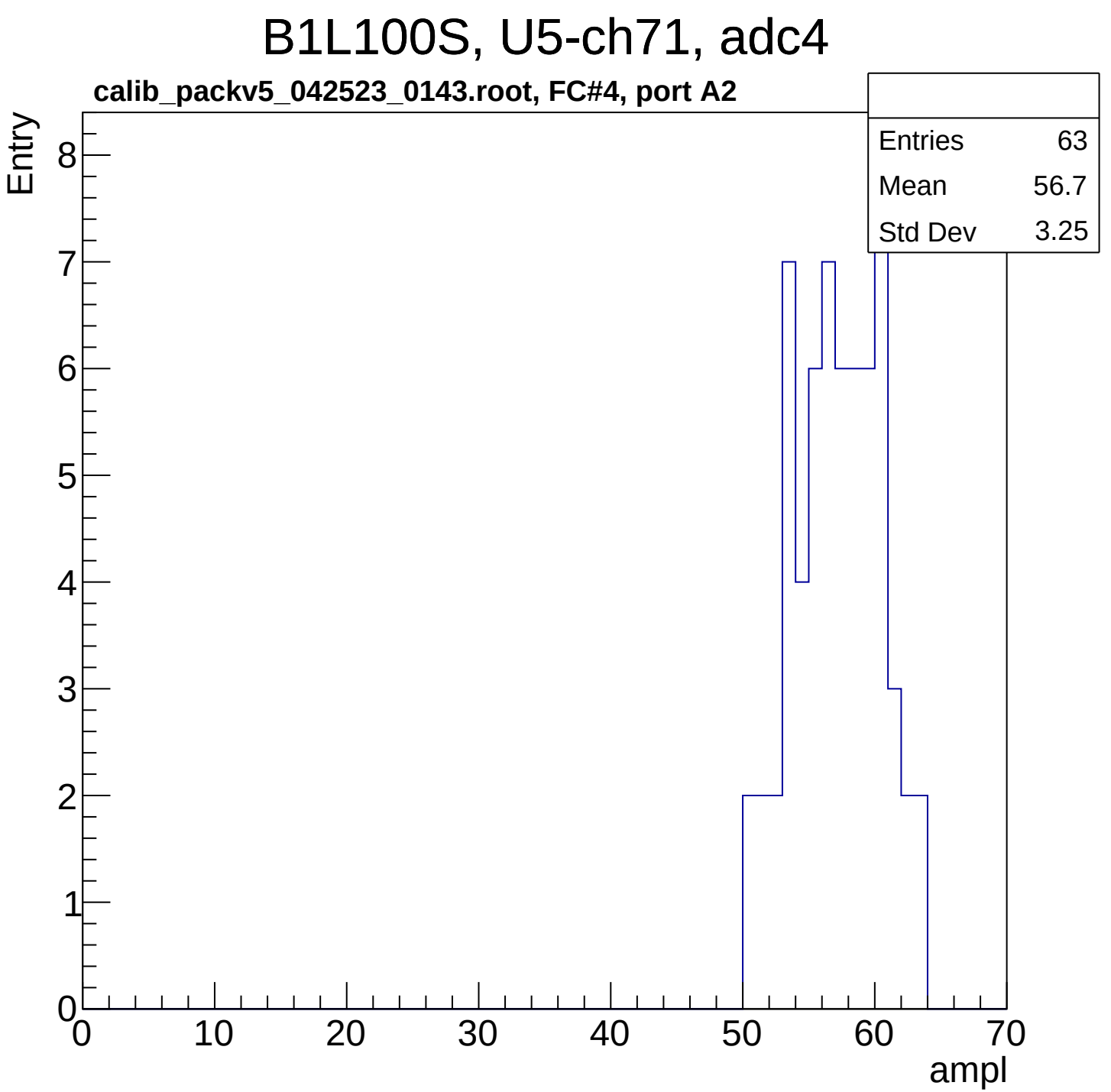
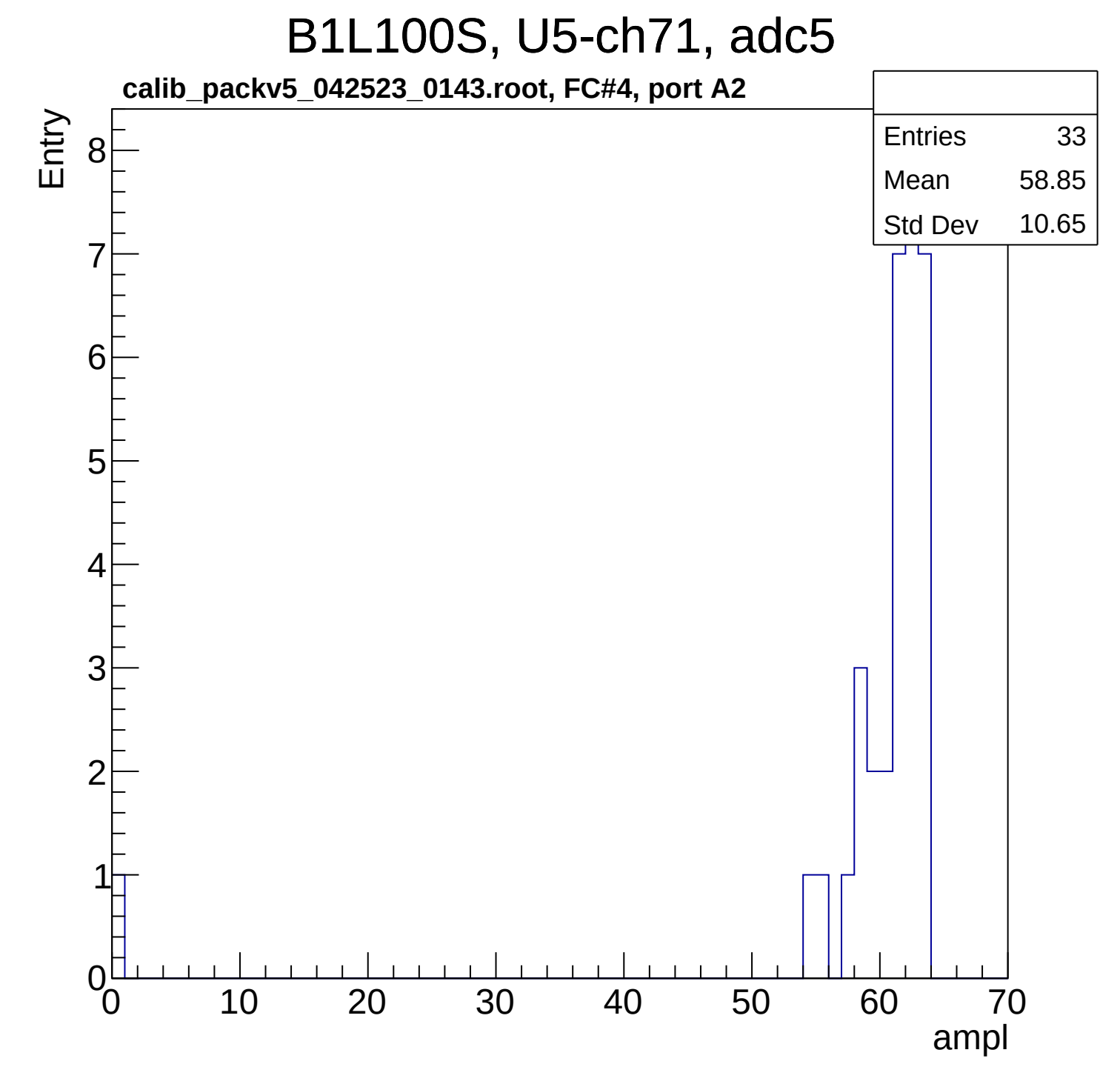

B1L100S, U5-ch71, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 56.7
Std Dev 3.25
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch71, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 33
Mean 58.85
Std Dev 10.65
Entry
ampl
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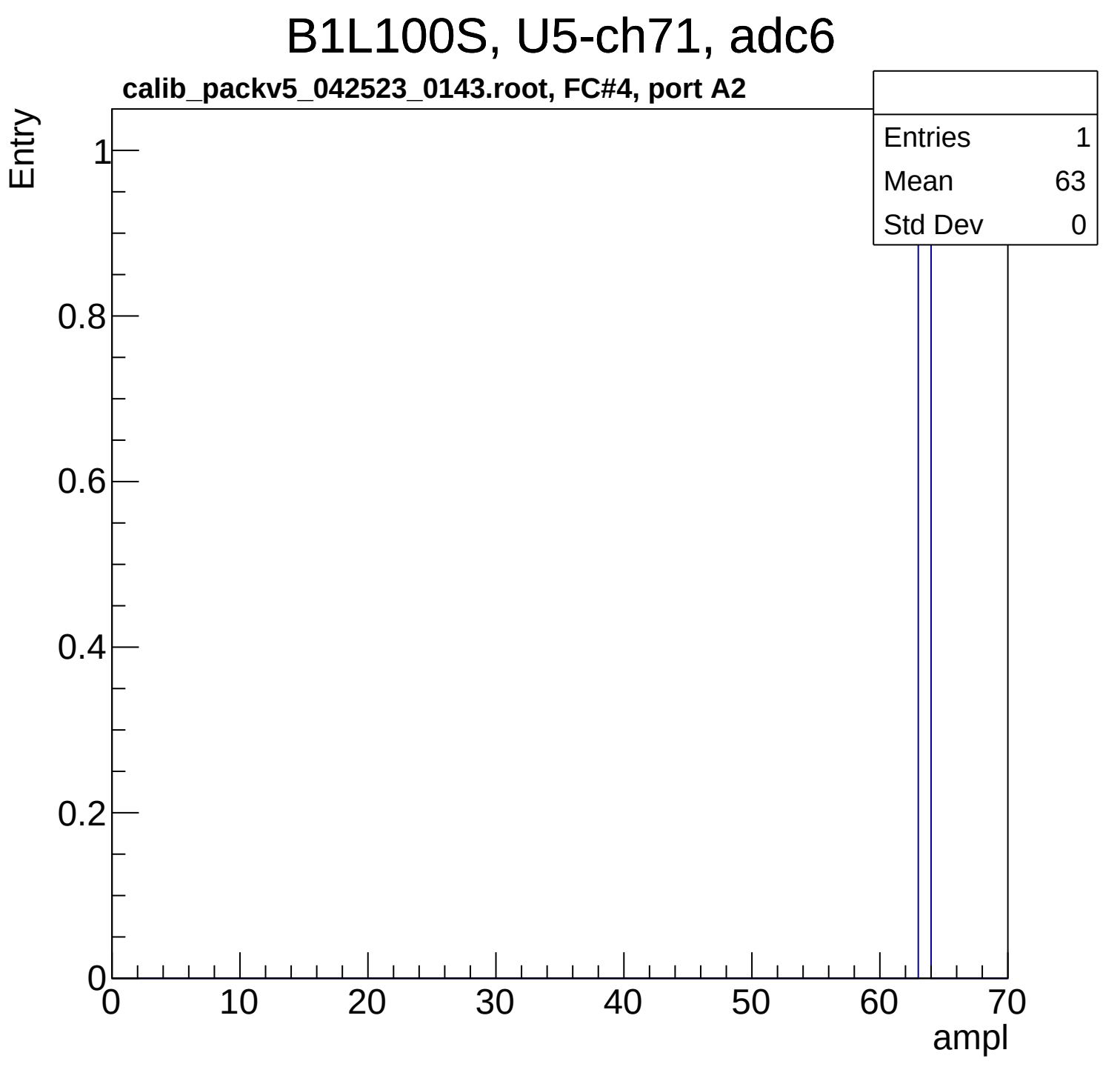
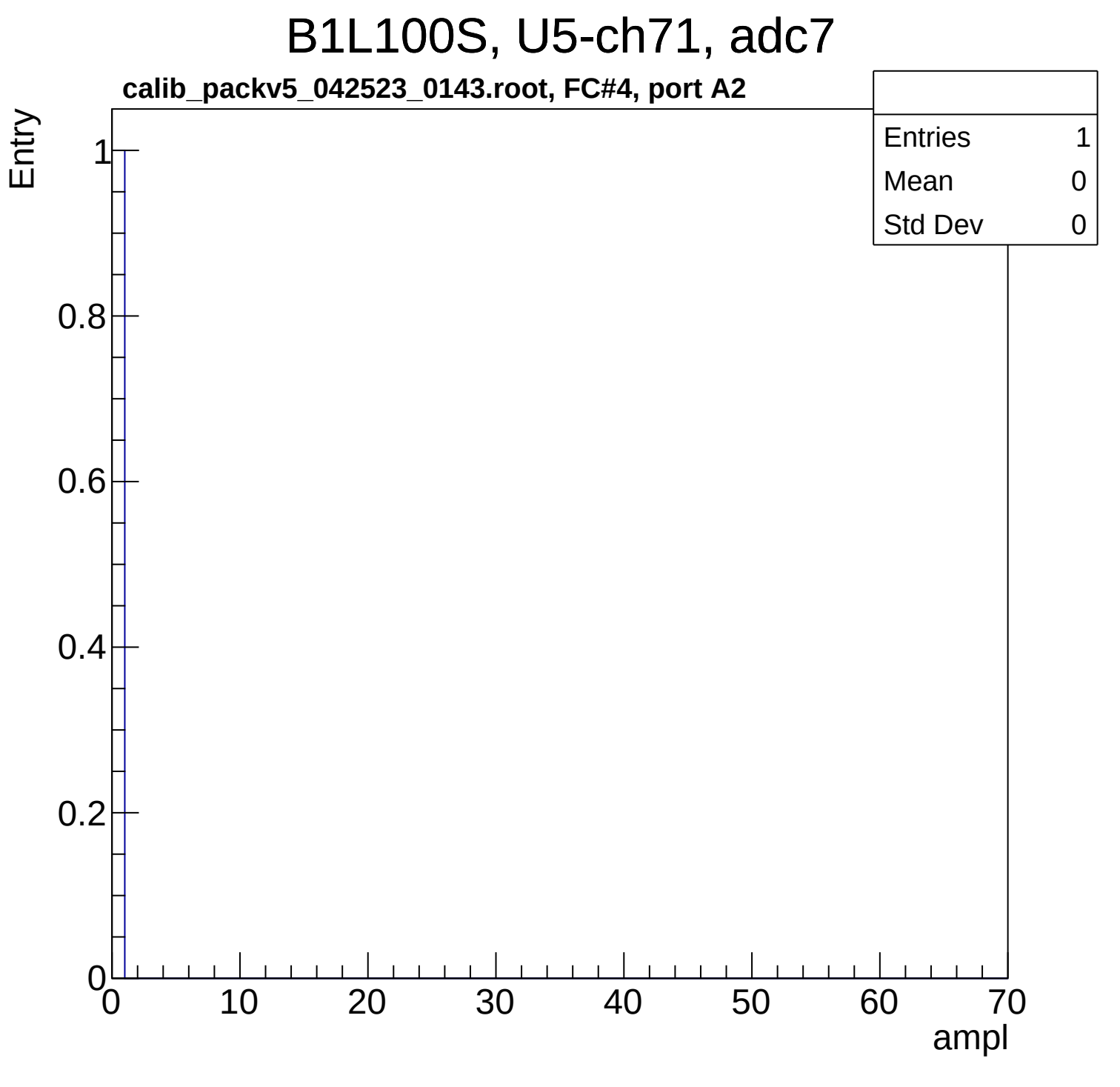
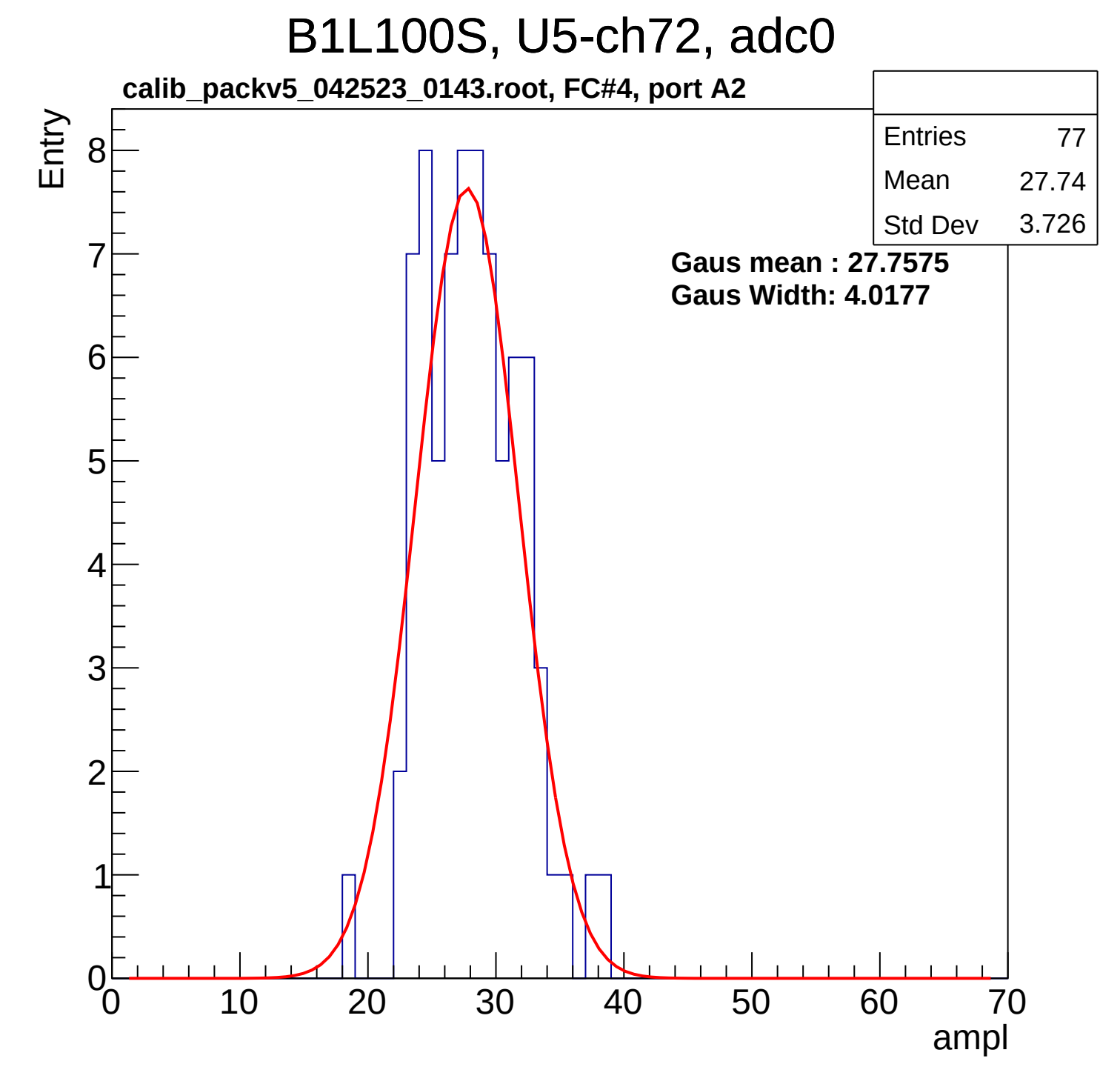
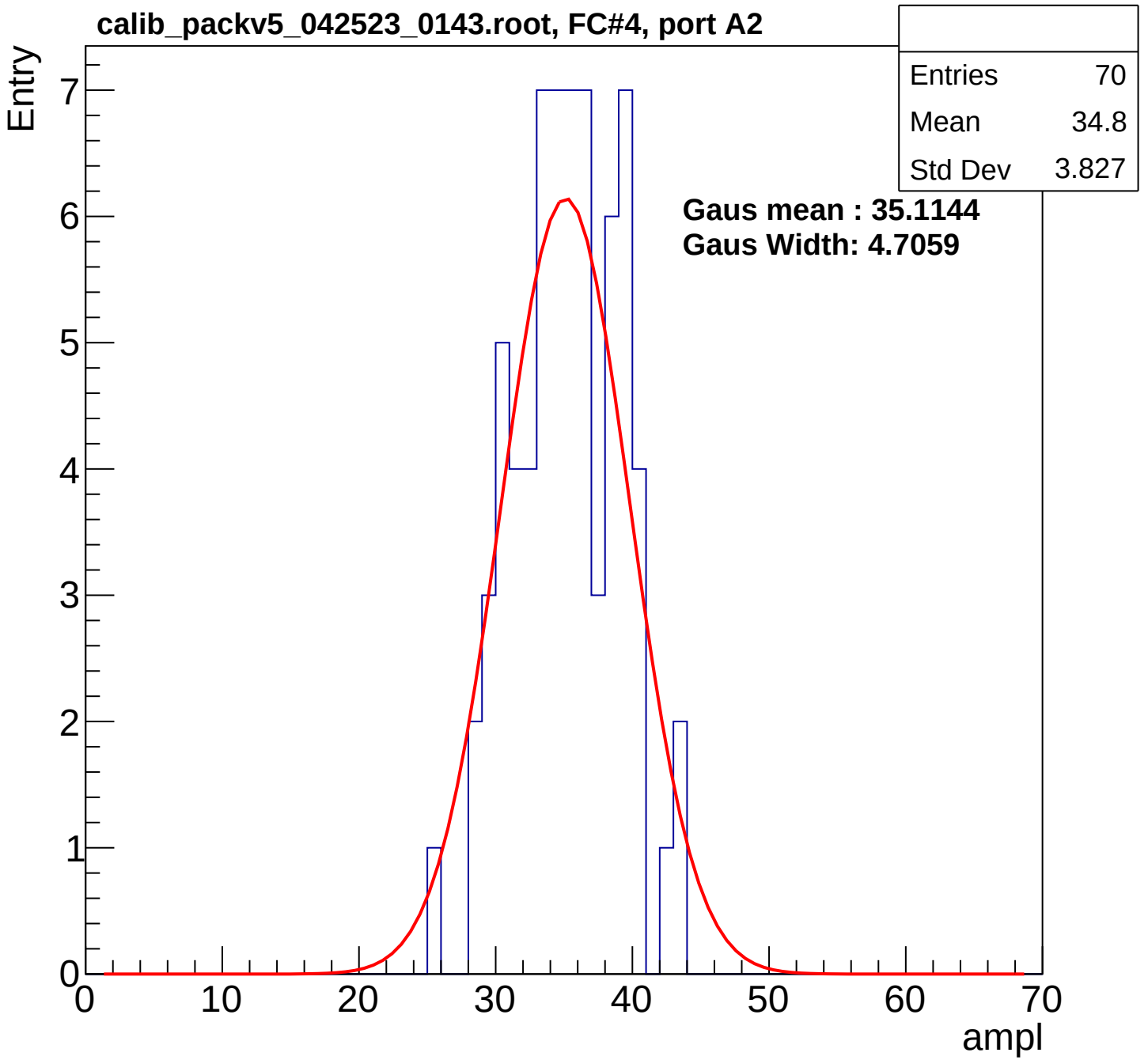
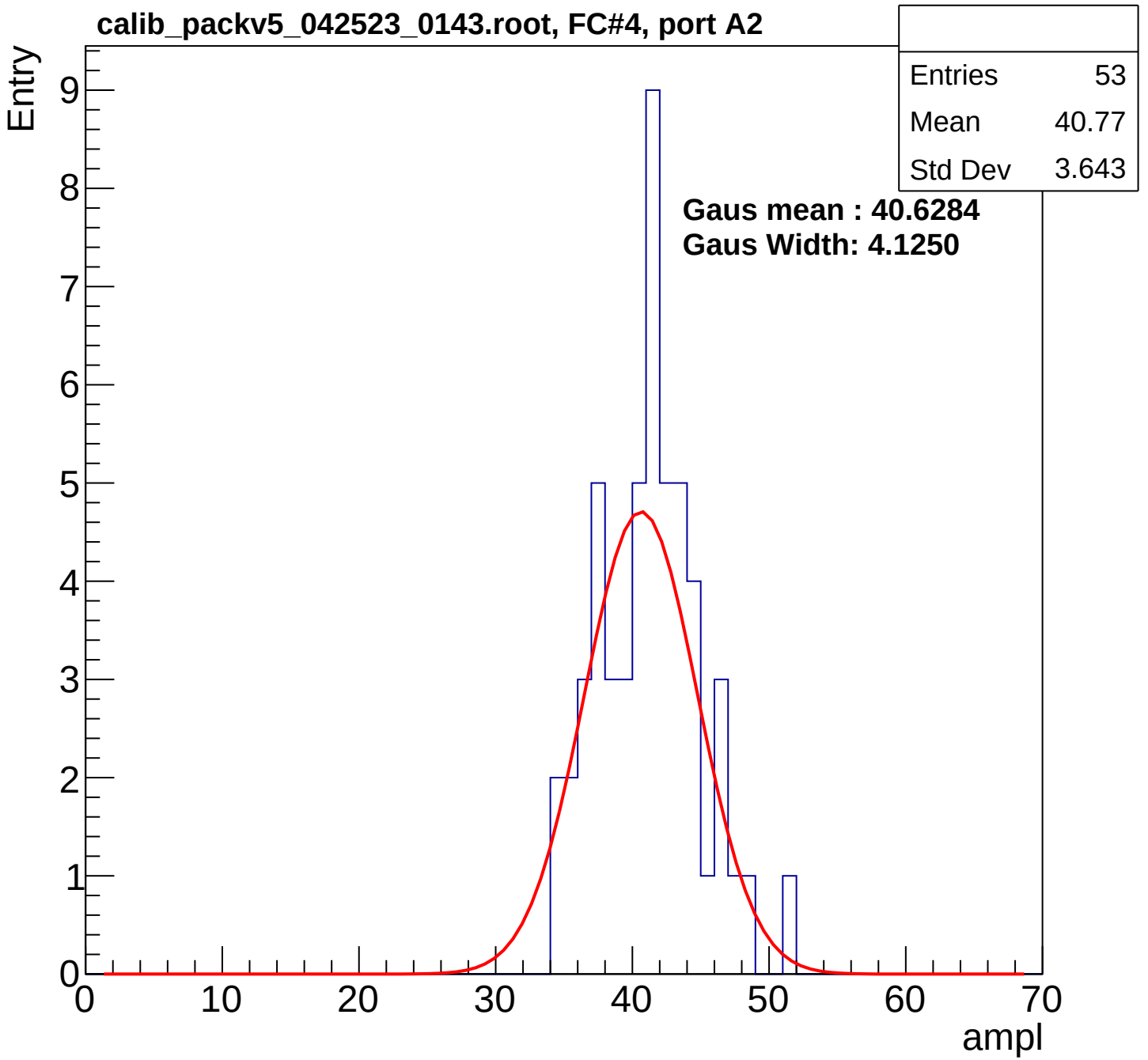
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

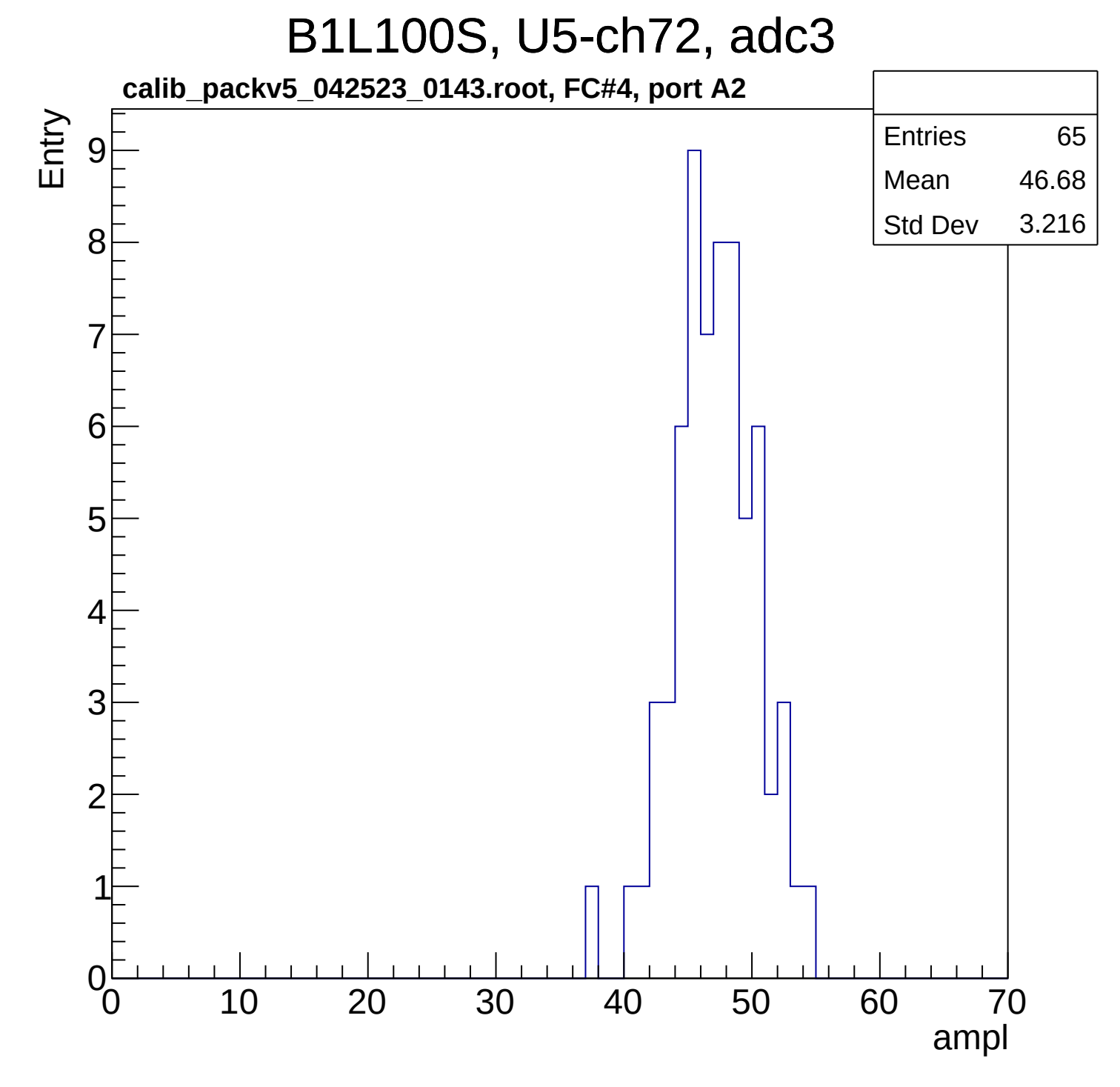

B1L100S, U5-ch71, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

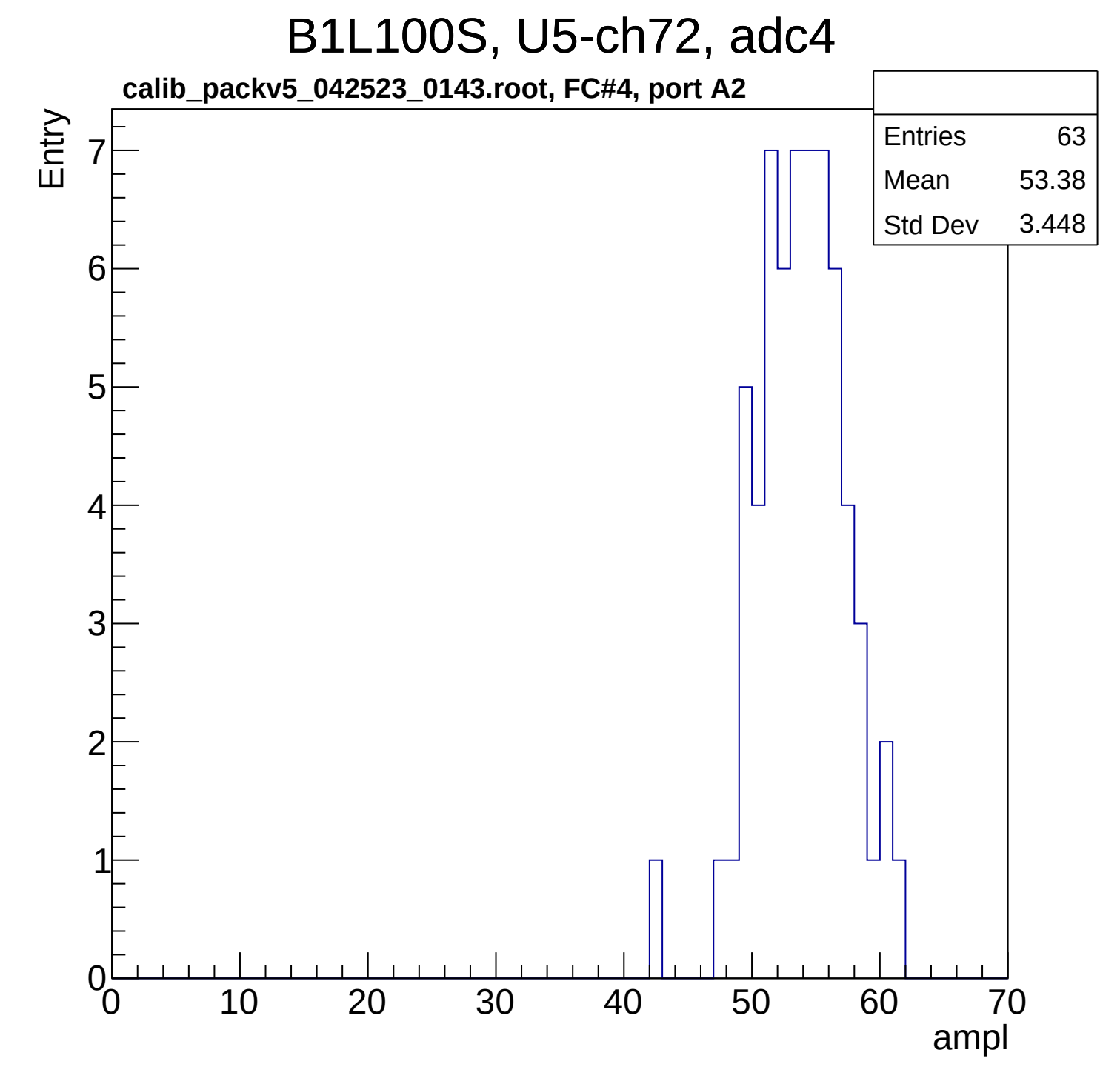

B1L100S, U5-ch71, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

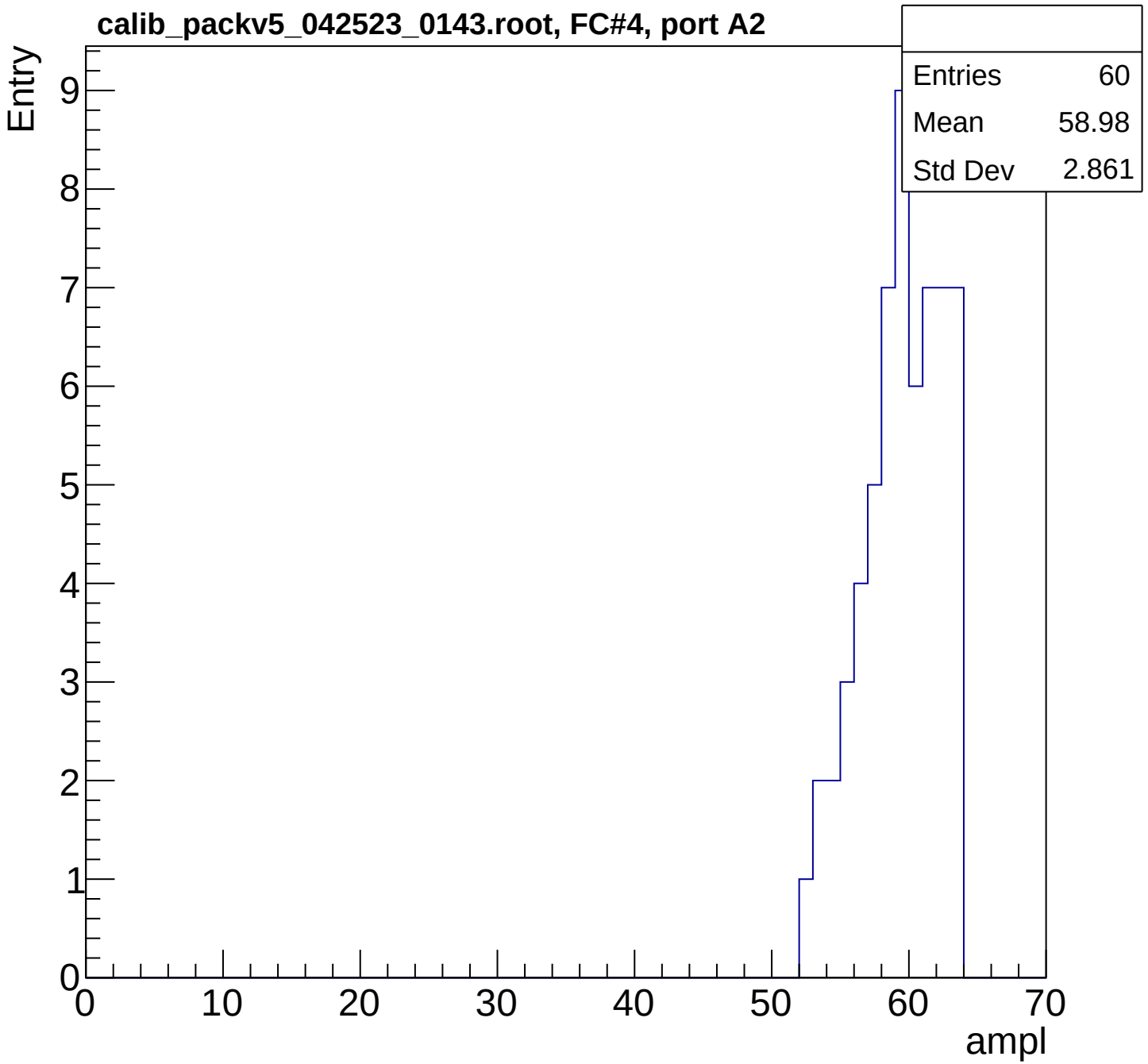

B1L100S, U5-ch72, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 77
Mean 27.74
Std Dev 3.726
Gaus mean : 27.7575
Gaus Width: 4.0177
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch72, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 34.8
Std Dev 3.827
Gaus mean : 35.1144
Gaus Width: 4.7059
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U5-ch72, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 40.77
Std Dev 3.643
Gaus mean : 40.6284
Gaus Width: 4.1250
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch72, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 46.68
Std Dev 3.216
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch72, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 53.38
Std Dev 3.448
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U5-ch72, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 58.98
Std Dev 2.861
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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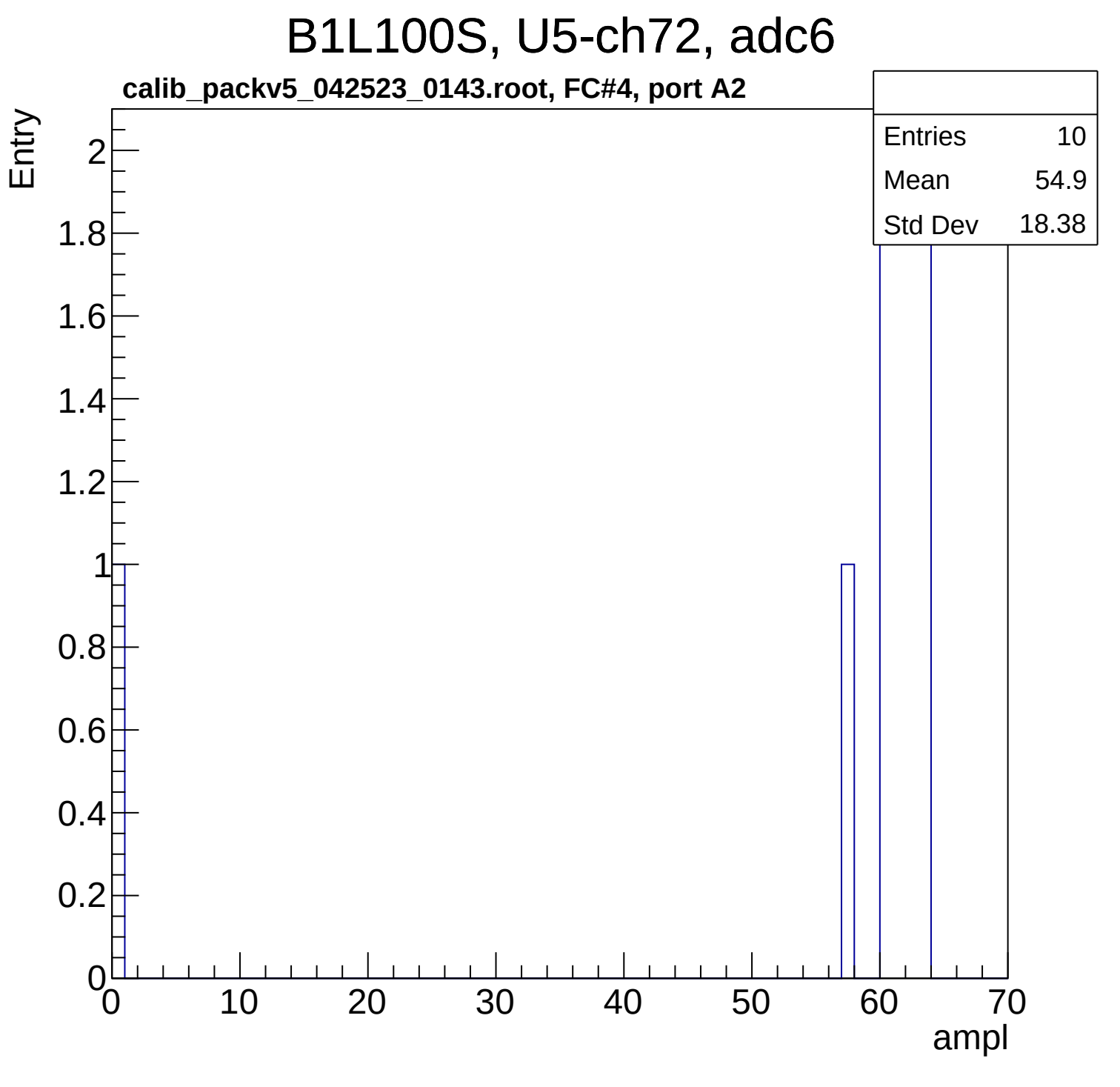
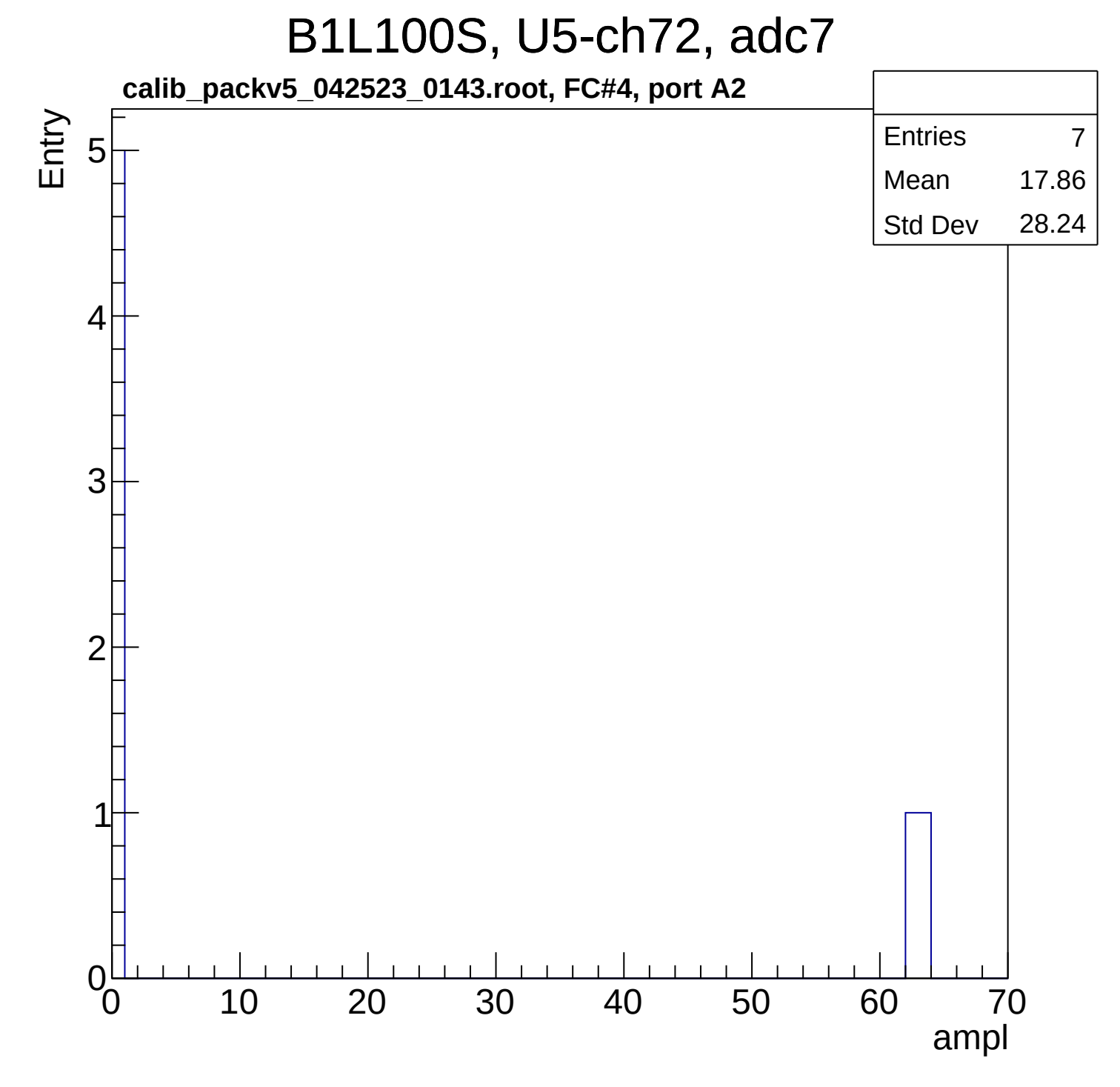
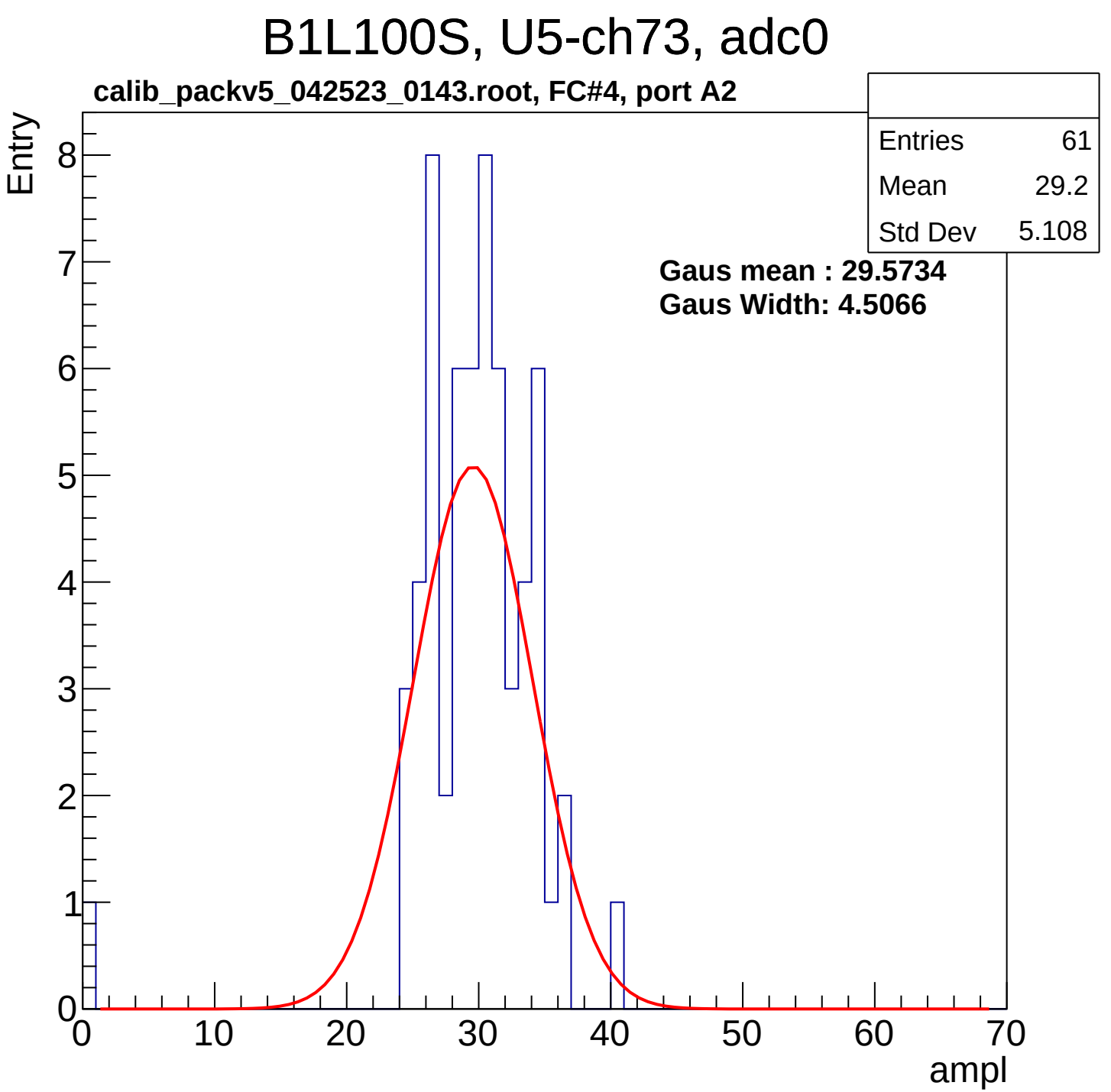
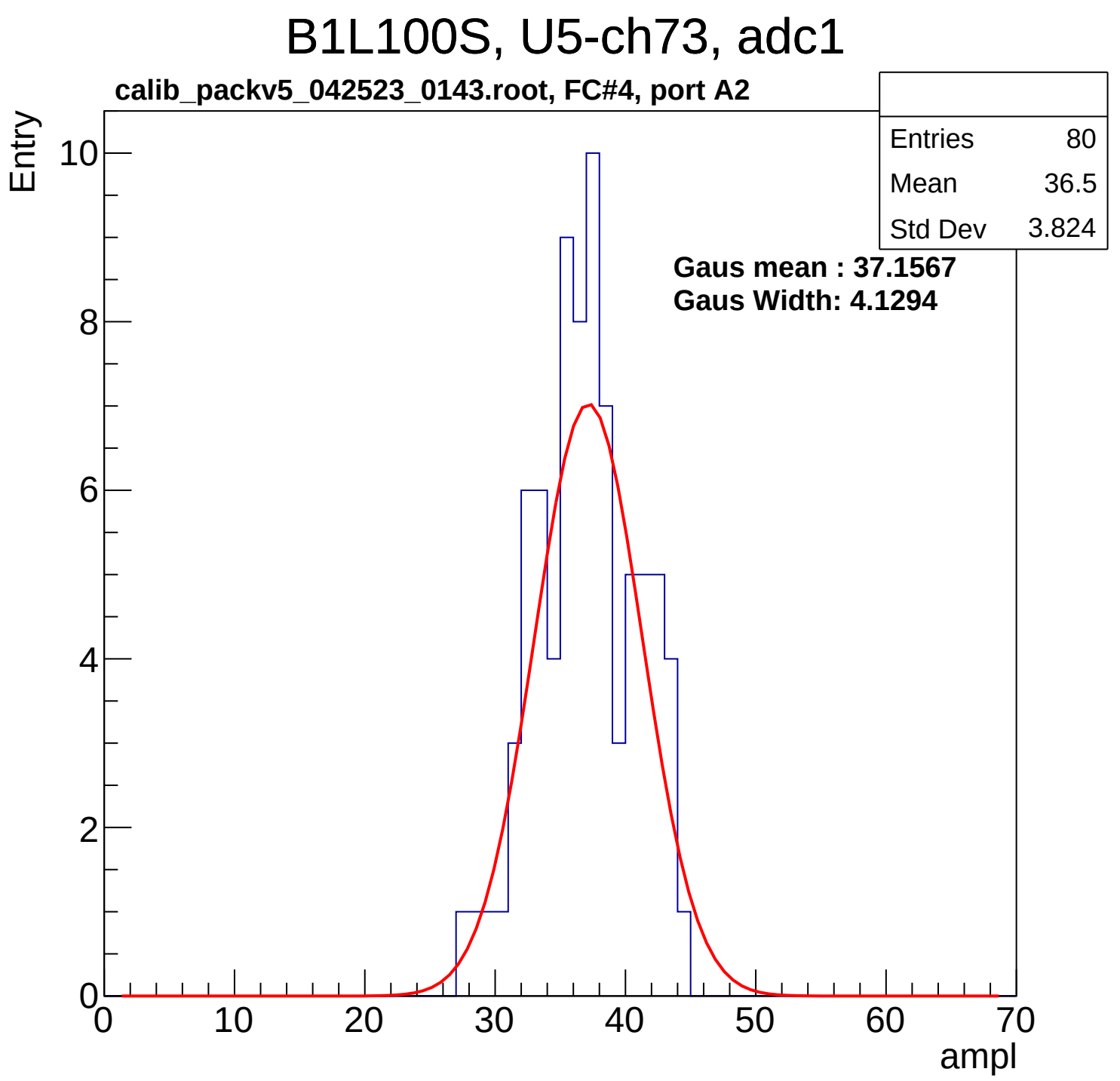
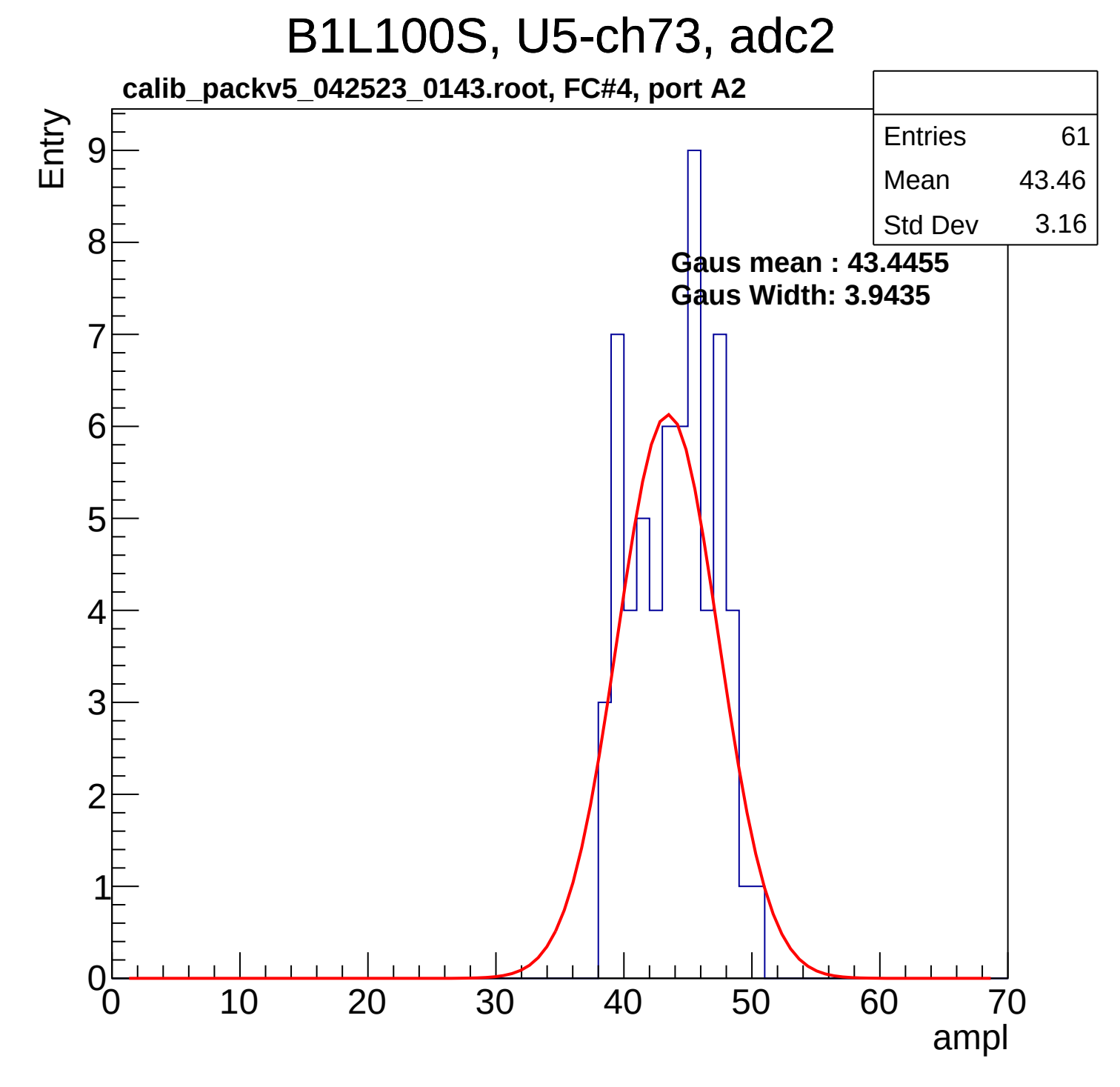
40
50
60
70

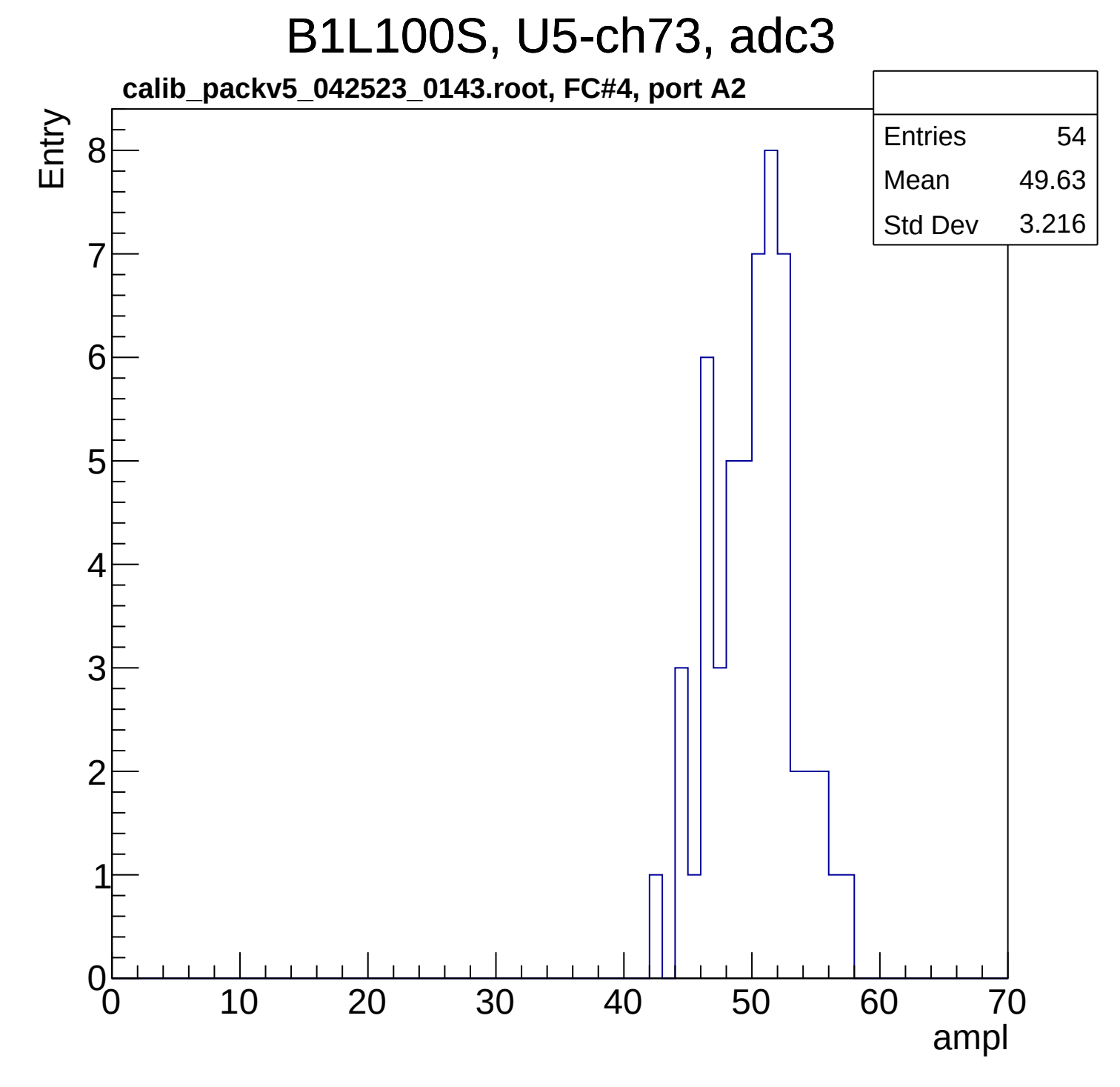

B1L100S, U5-ch72, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 10
Mean 54.9
Std Dev 18.38
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L100S, U5-ch72, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 7
Mean 17.86
Std Dev 28.24
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch73, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 29.2
Std Dev 5.108
Gaus mean : 29.5734
Gaus Width: 4.5066
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch73, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 80
Mean 36.5
Std Dev 3.824
Gaus mean : 37.1567
Gaus Width: 4.1294
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch73, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 43.46
Std Dev 3.16
Gaus mean : 43.4455
Gaus Width: 3.9435
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch73, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 49.63
Std Dev 3.216
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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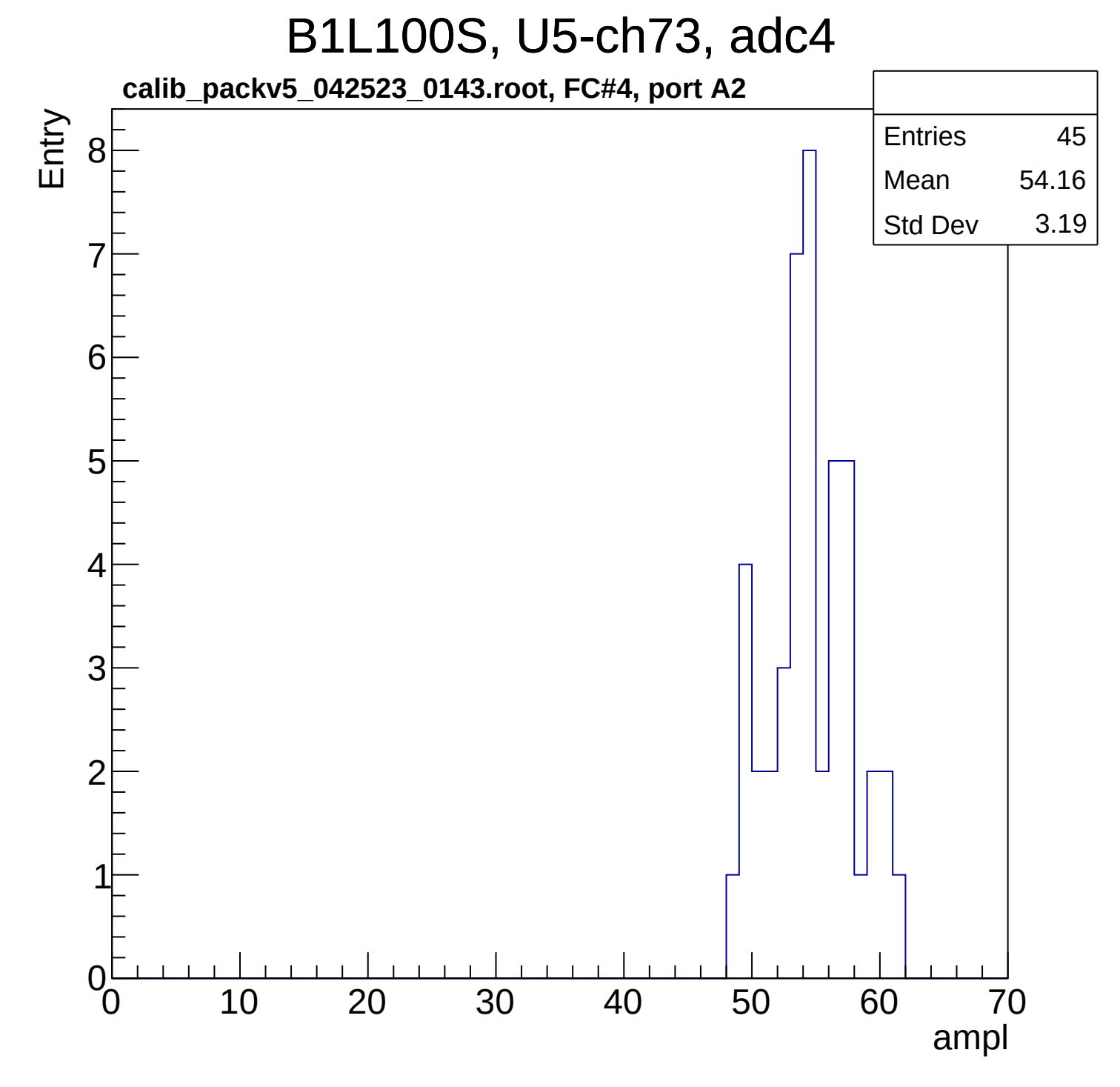
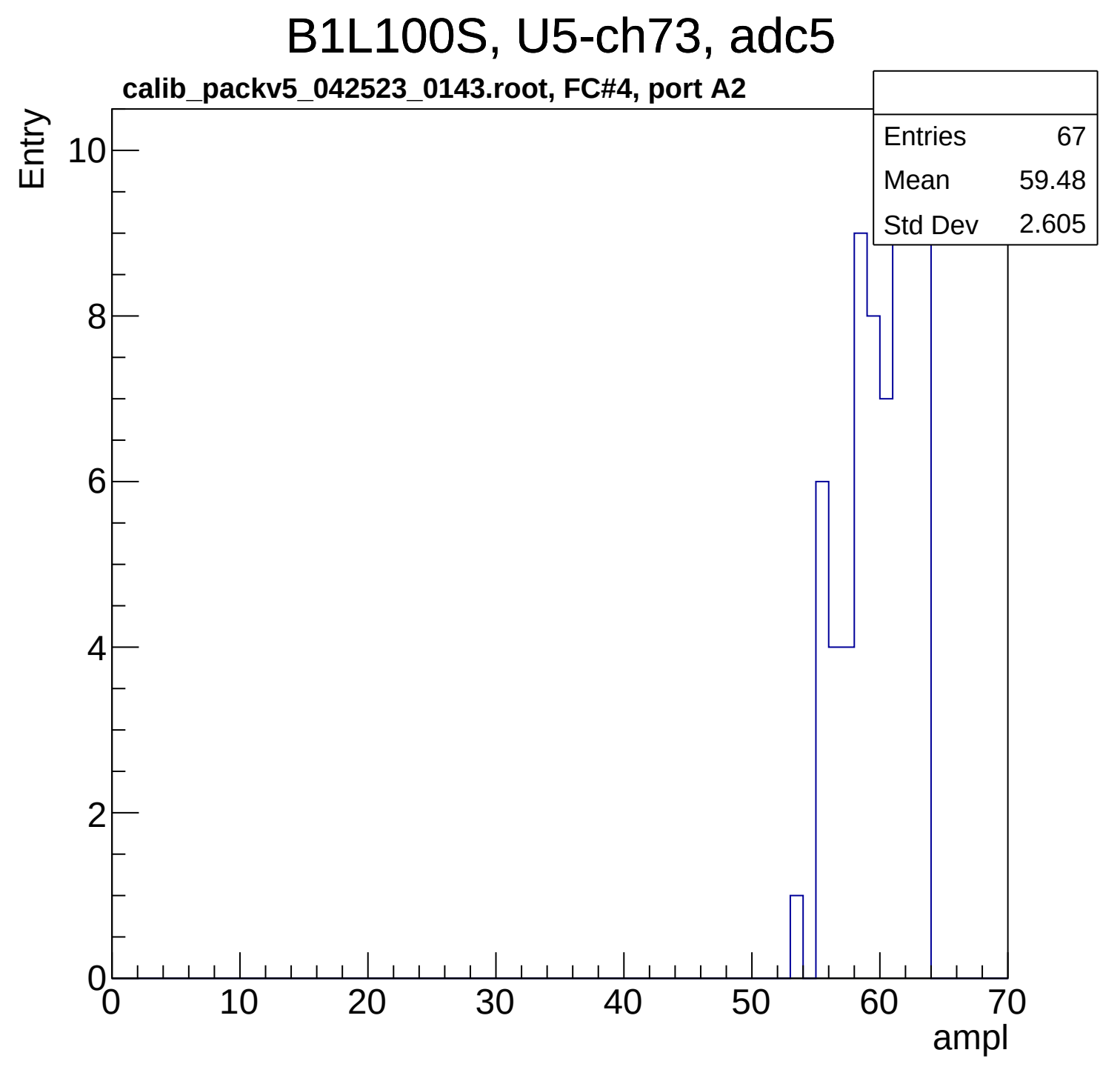
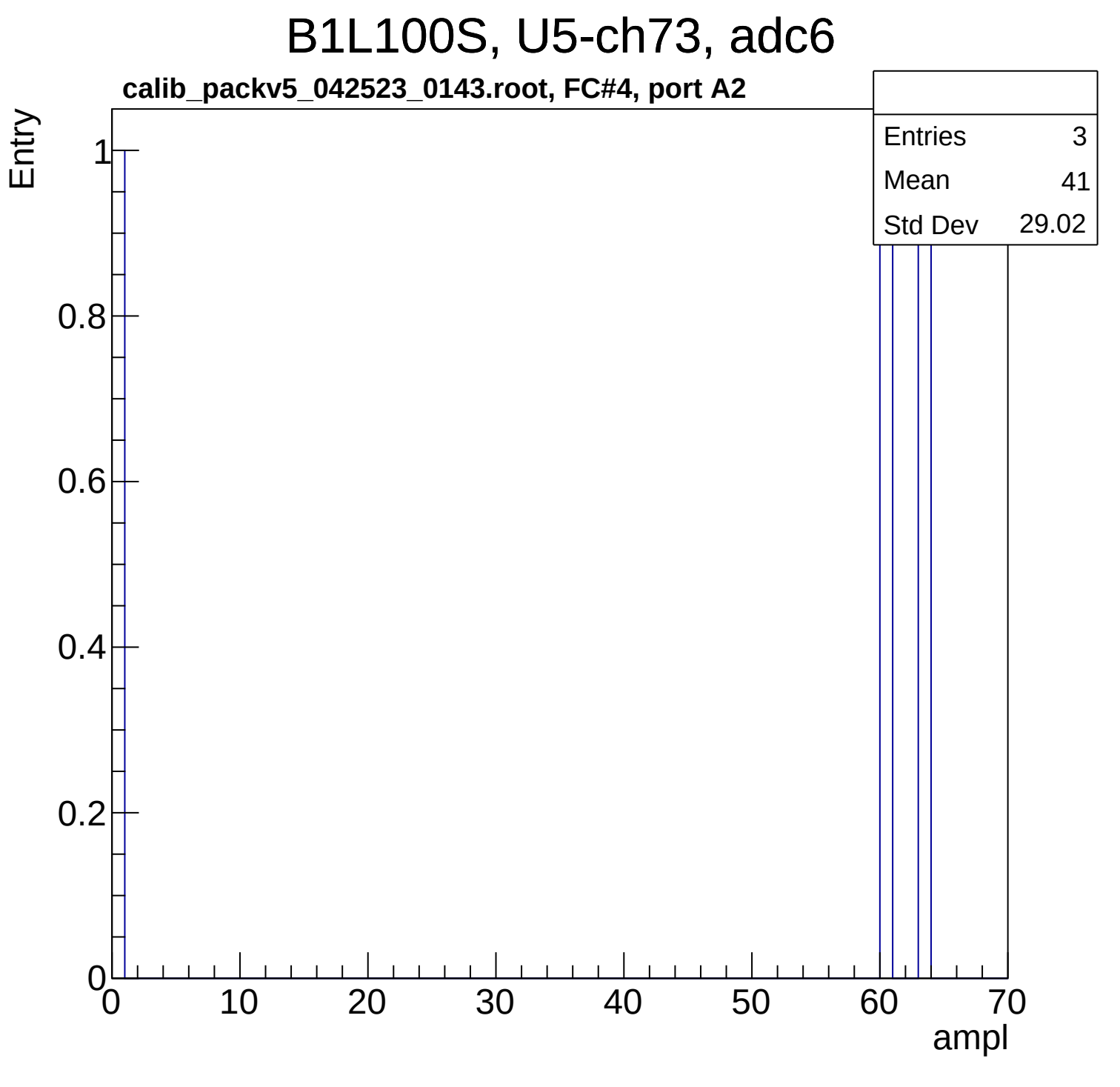
40
50
60
70


B1L100S, U5-ch73, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 45
Mean 54.16
Std Dev 3.19
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch73, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 59.48
Std Dev 2.605
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch73, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 41
Std Dev 29.02
Entry
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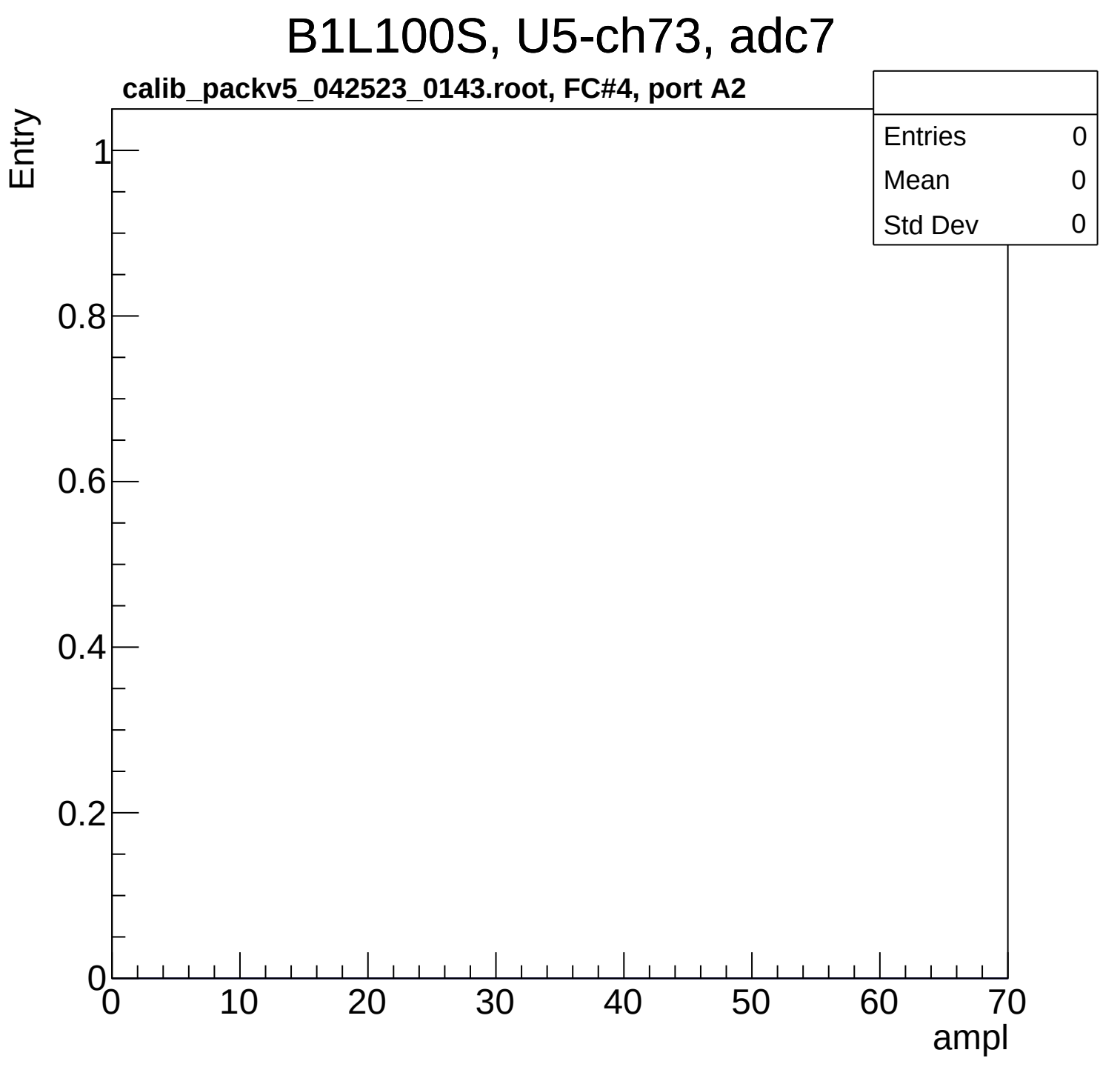
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch73, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
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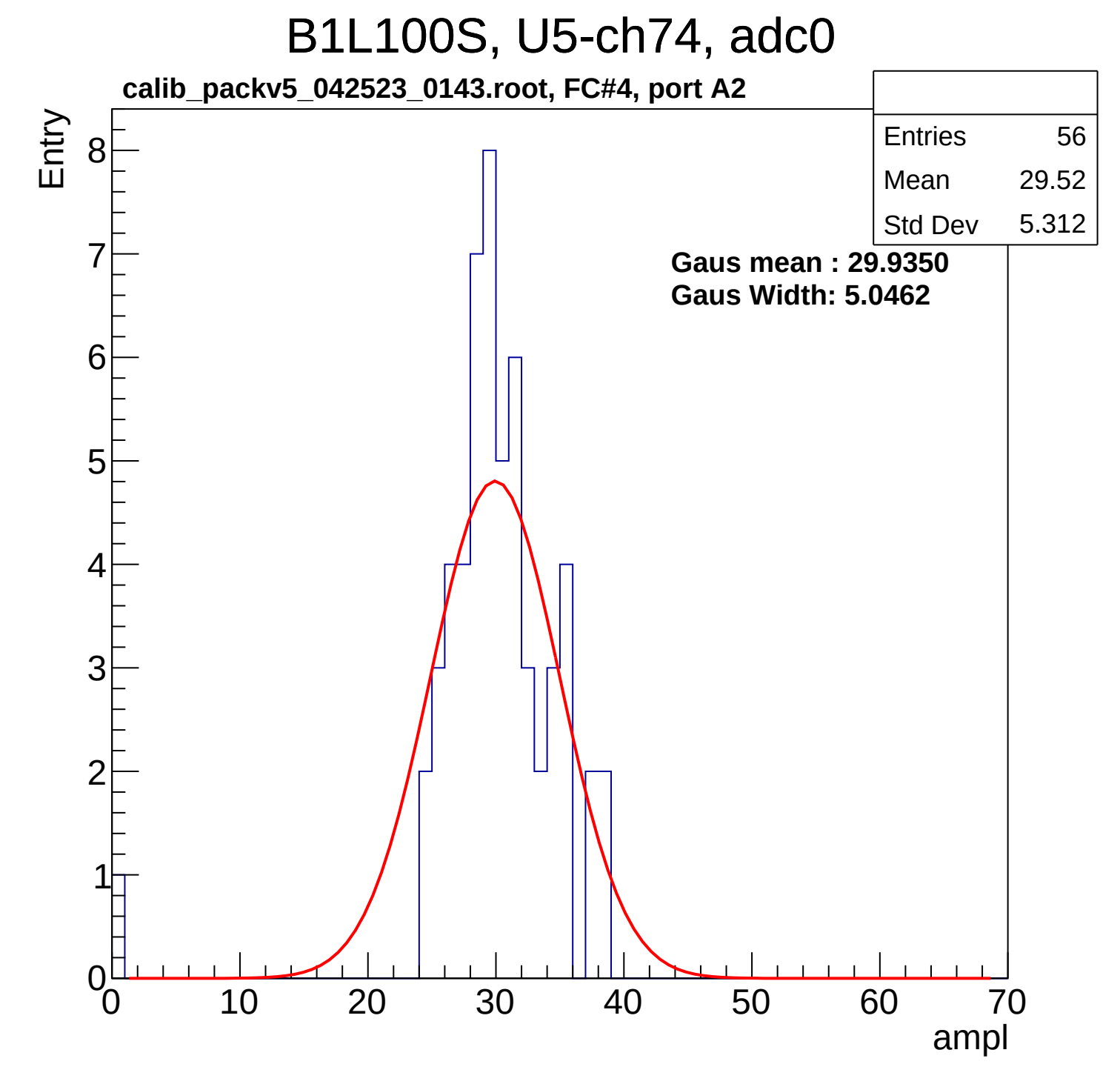
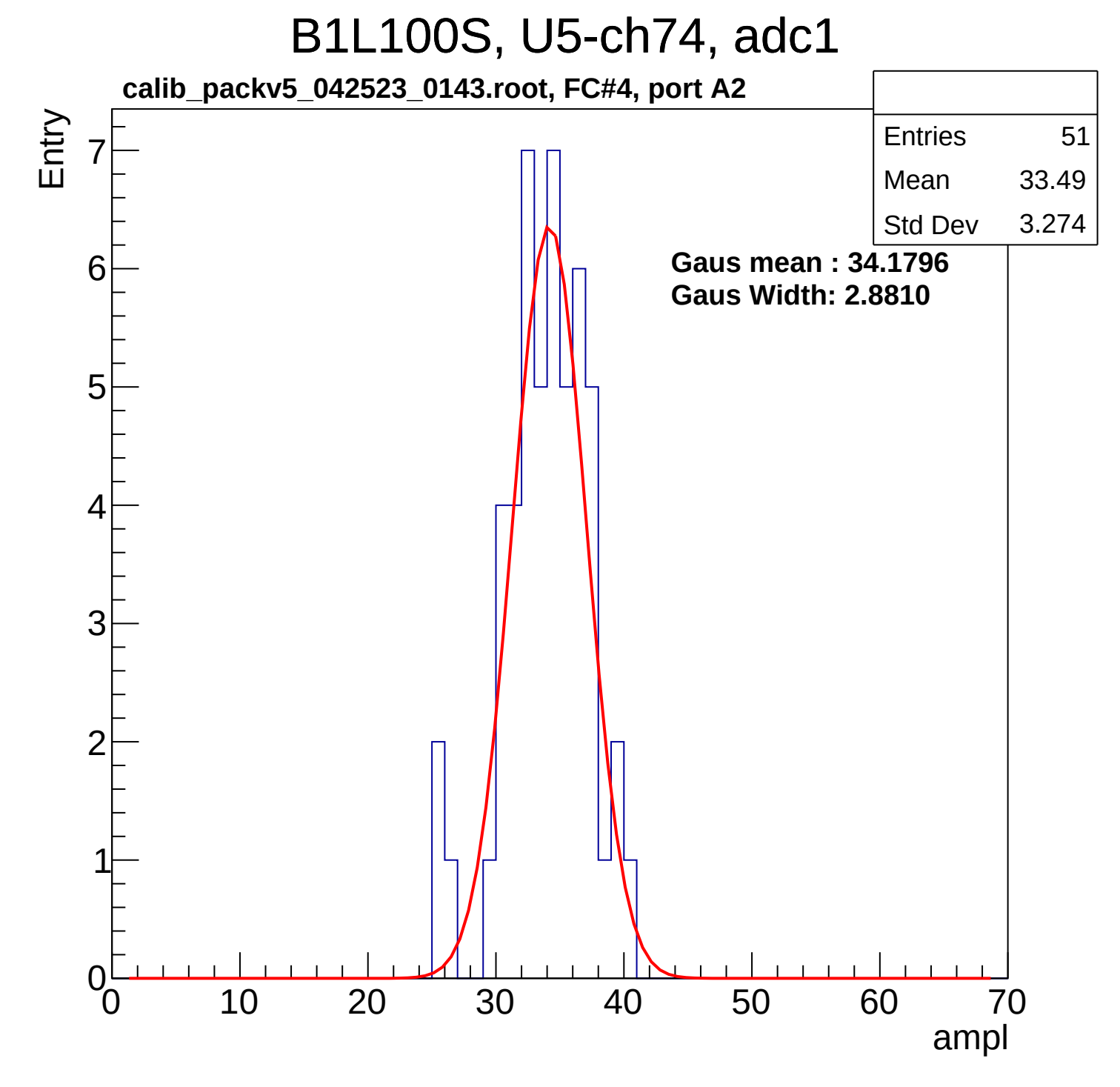
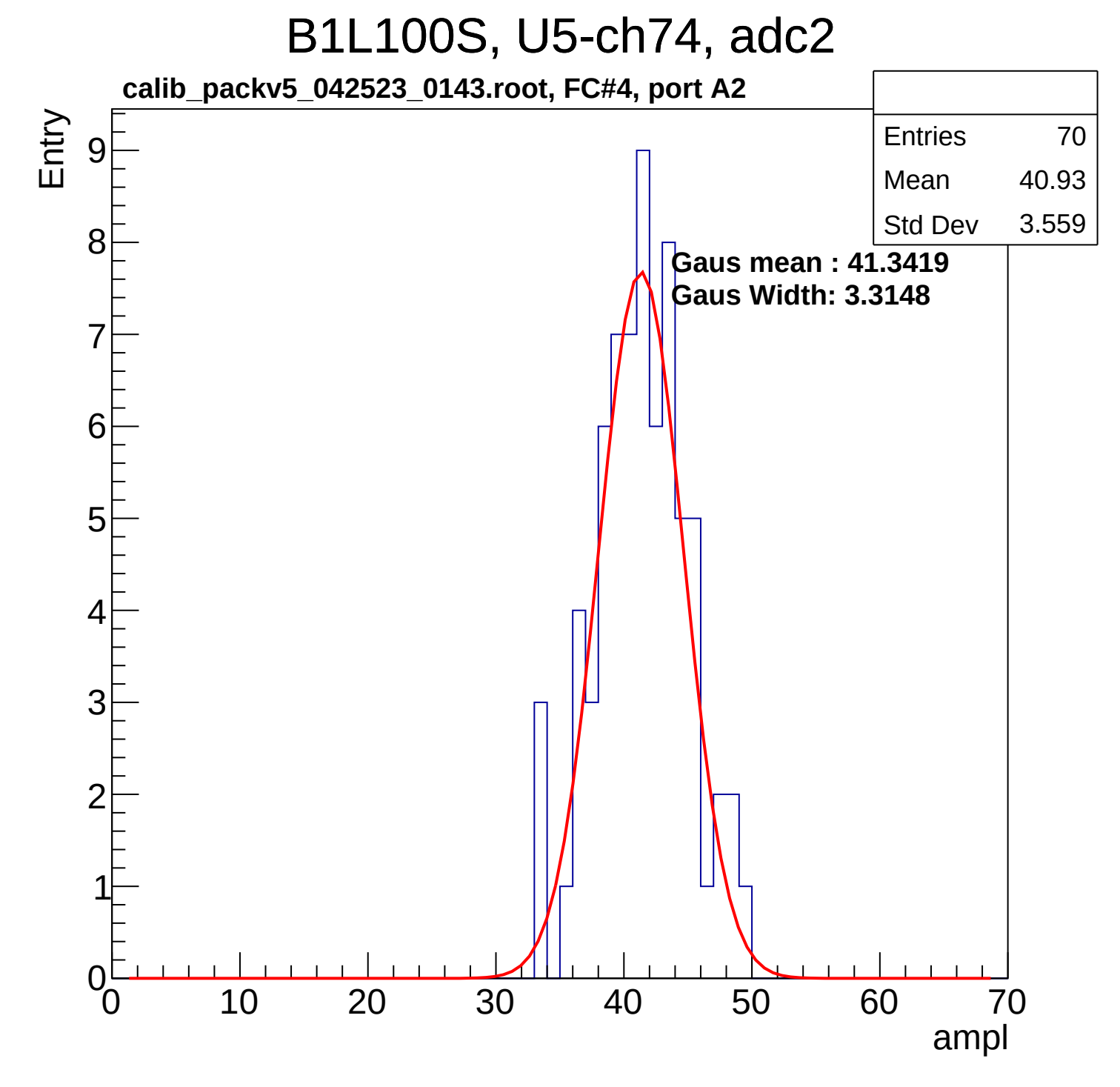
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch74, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 29.52
Std Dev 5.312
Gaus mean : 29.9350
Gaus Width: 5.0462
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch74, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 33.49
Std Dev 3.274
Gaus mean : 34.1796
Gaus Width: 2.8810
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U5-ch74, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 40.93
Std Dev 3.559
Gaus mean : 41.3419
Gaus Width: 3.3148
Entry
ampl
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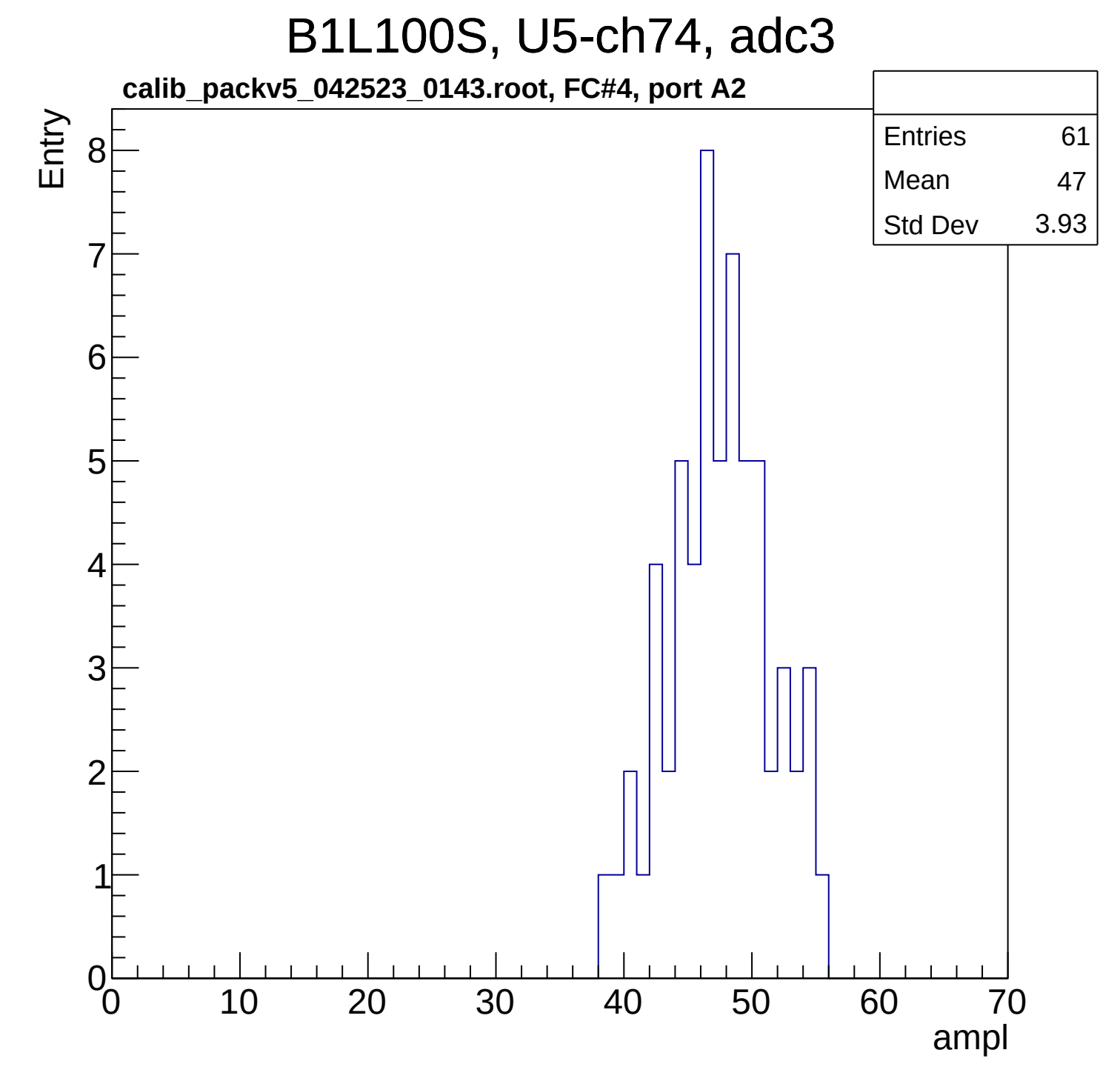
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch74, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 47
Std Dev 3.93
Entry
ampl
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2
3
4
5
6
7
8
0
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20
30
40
50
60
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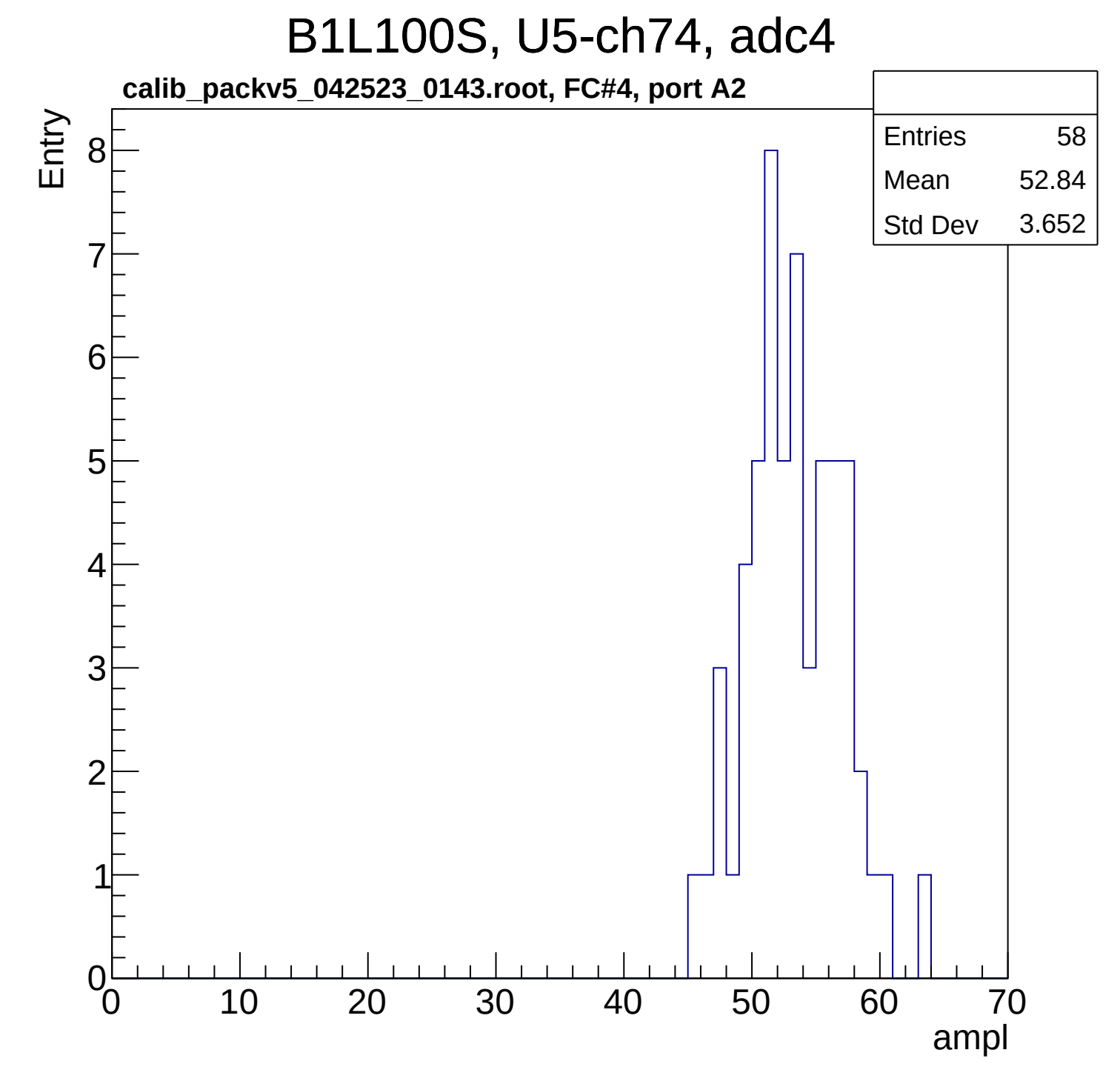
B1L100S, U5-ch74, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 52.84
Std Dev 3.652
Entry
ampl
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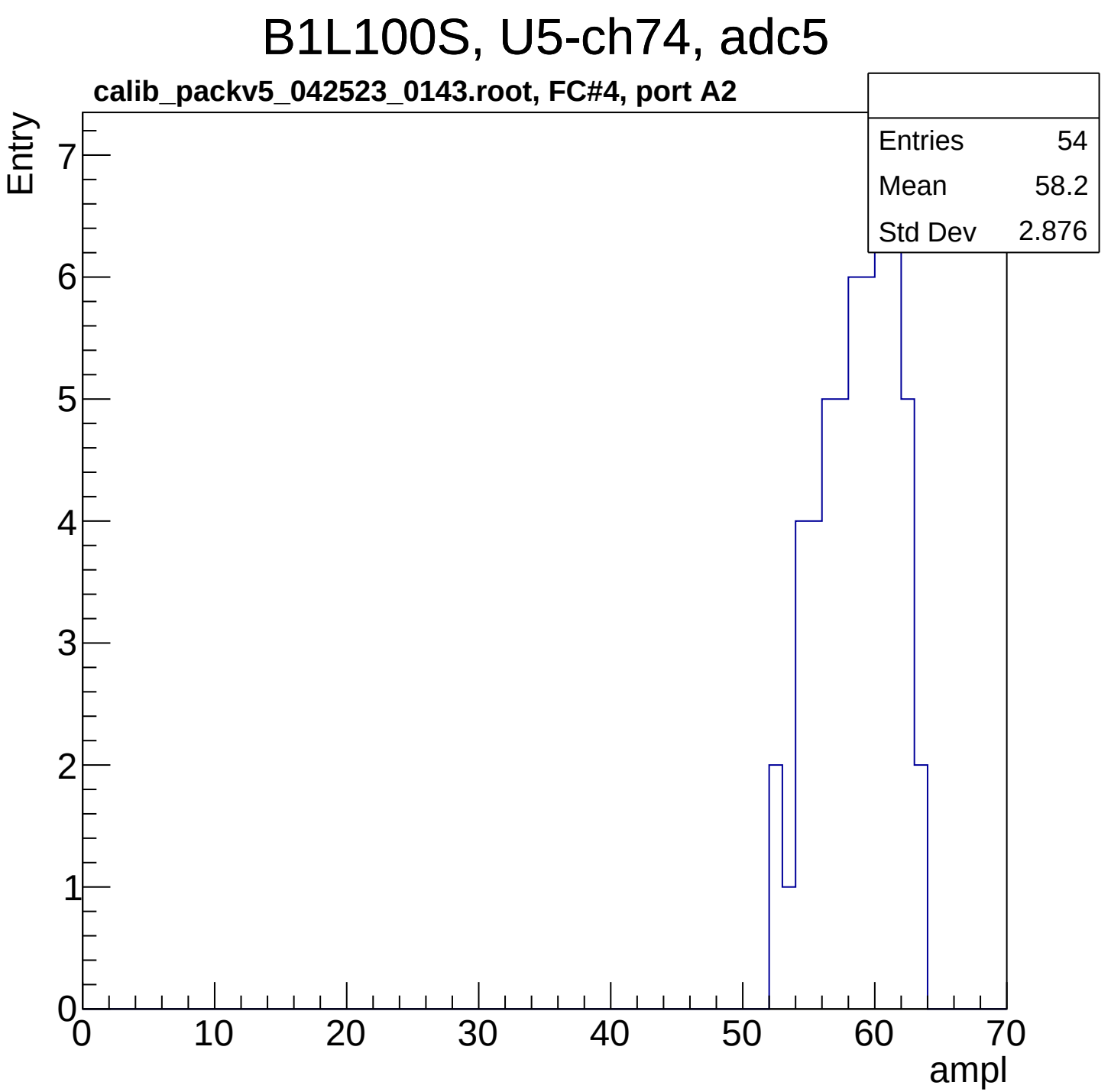
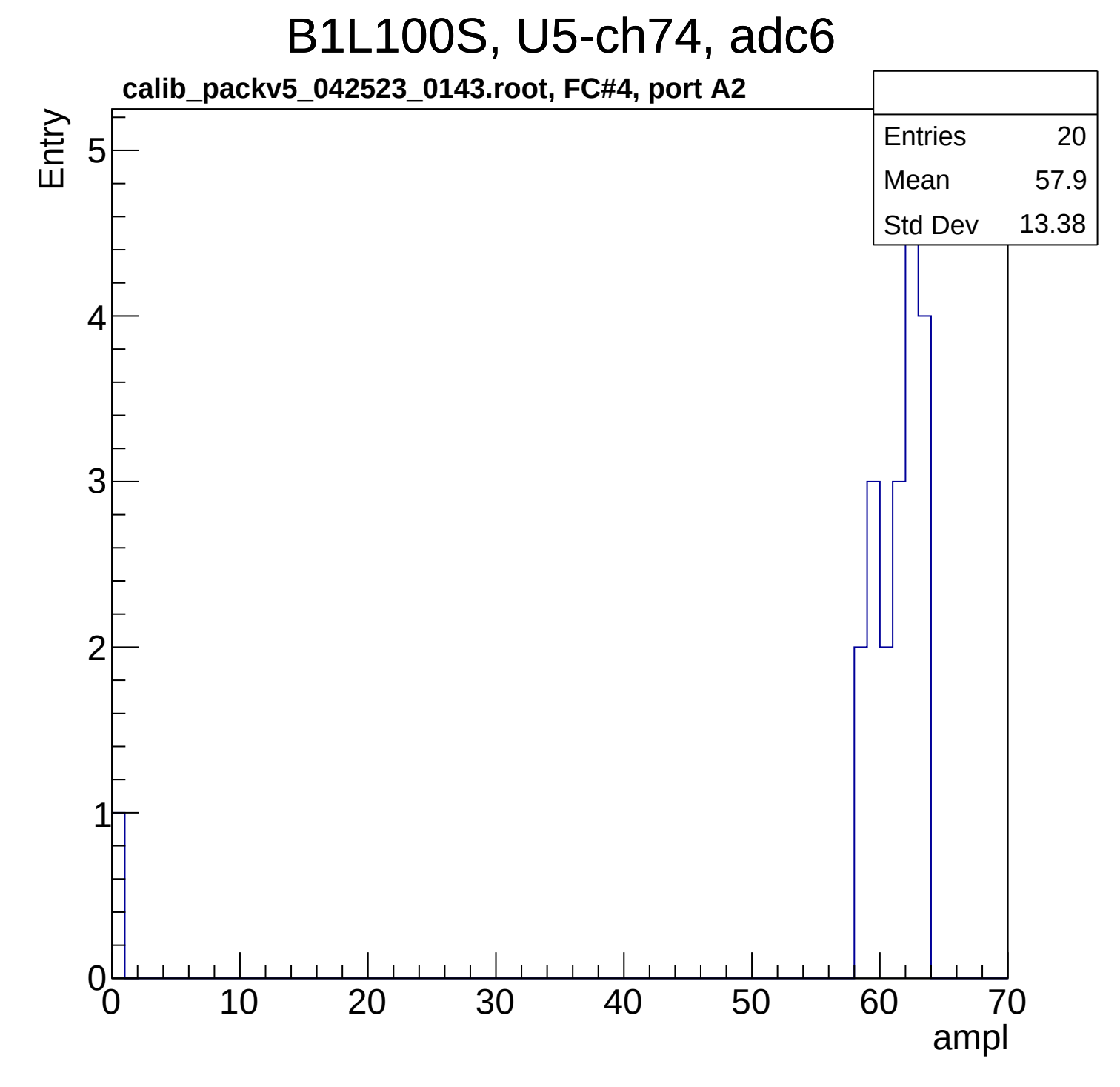
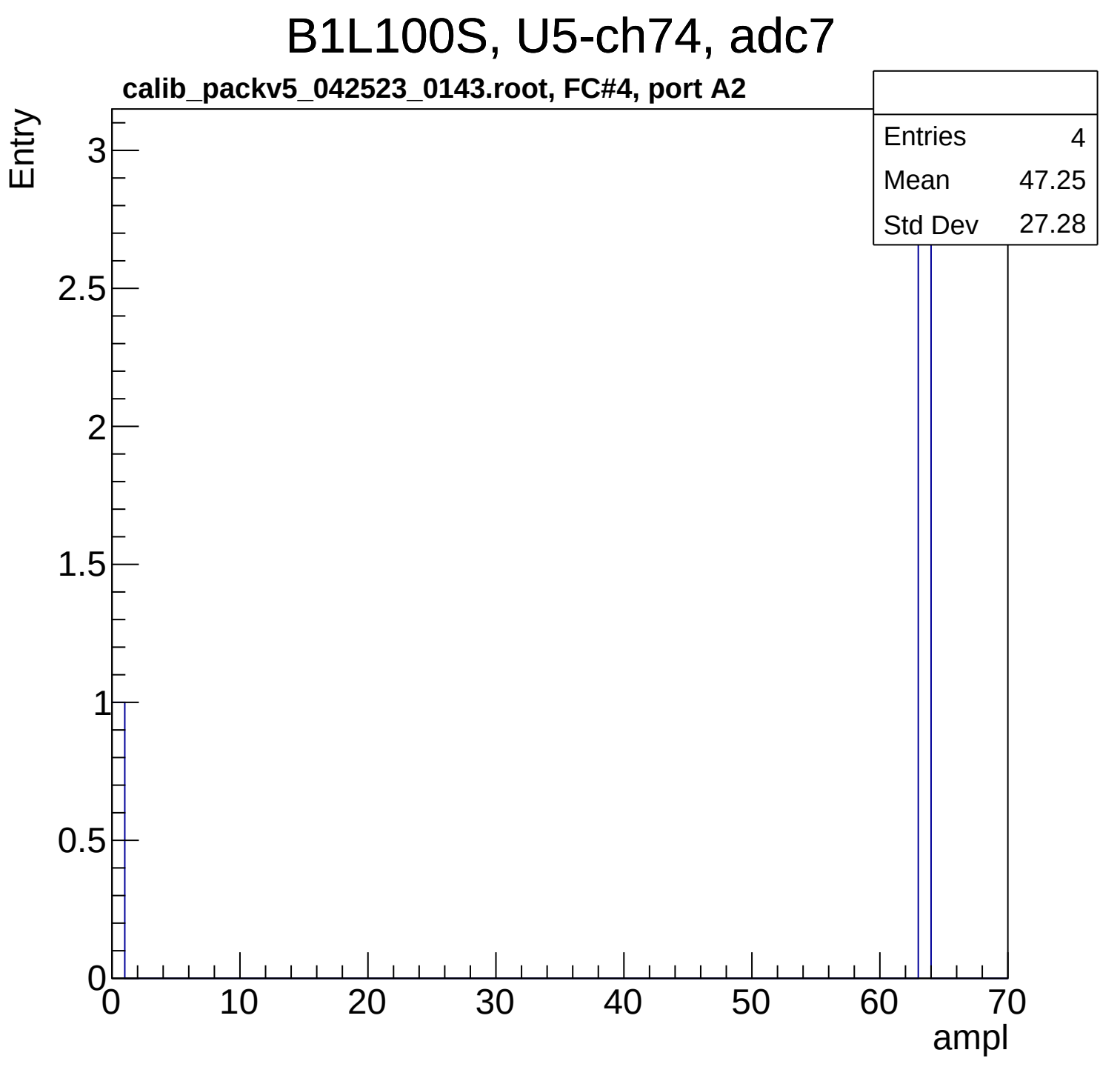
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch74, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 58.2
Std Dev 2.876
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U5-ch74, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 20
Mean 57.9
Std Dev 13.38
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch74, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 4
Mean 47.25
Std Dev 27.28
Entry
ampl
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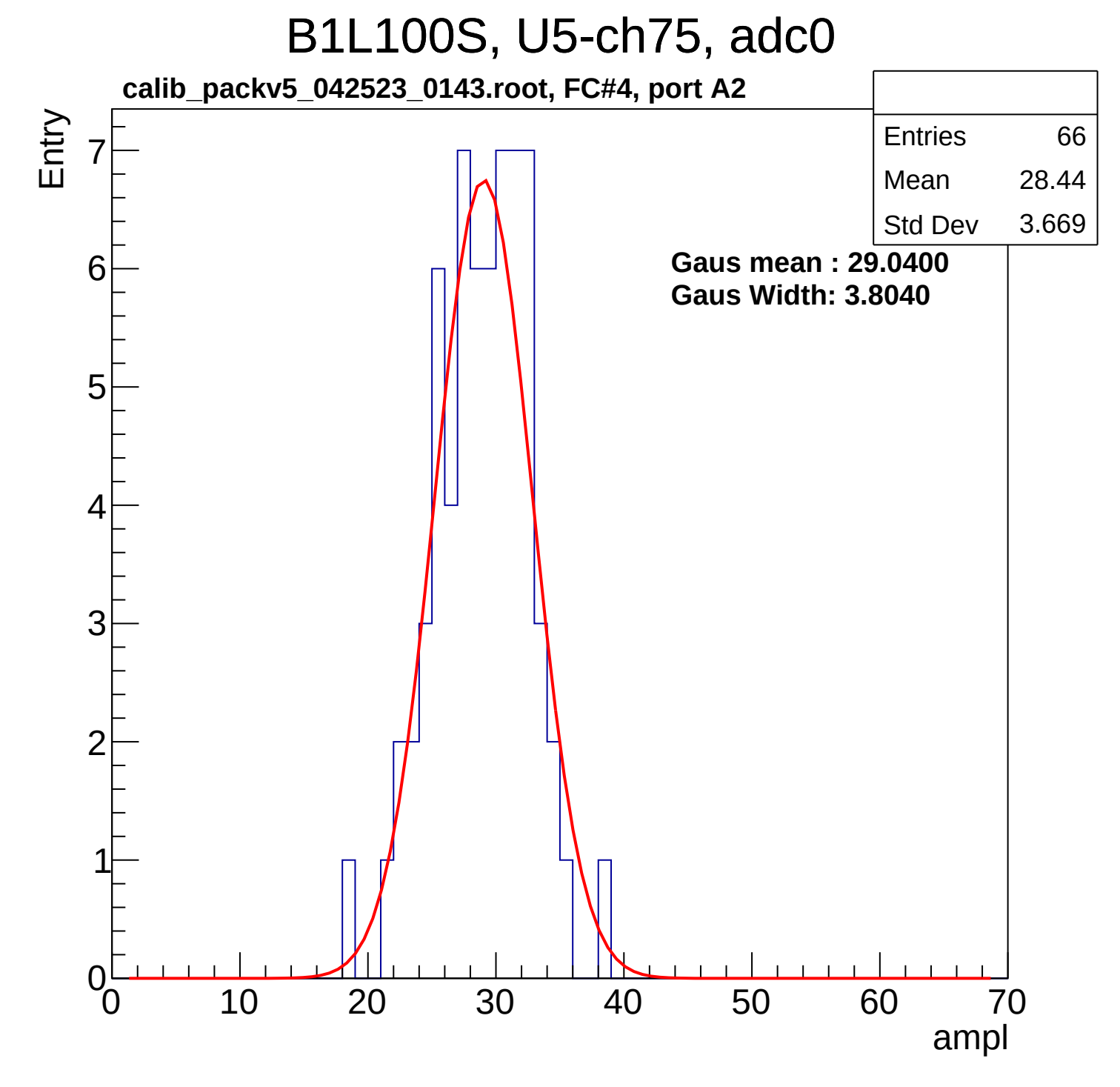
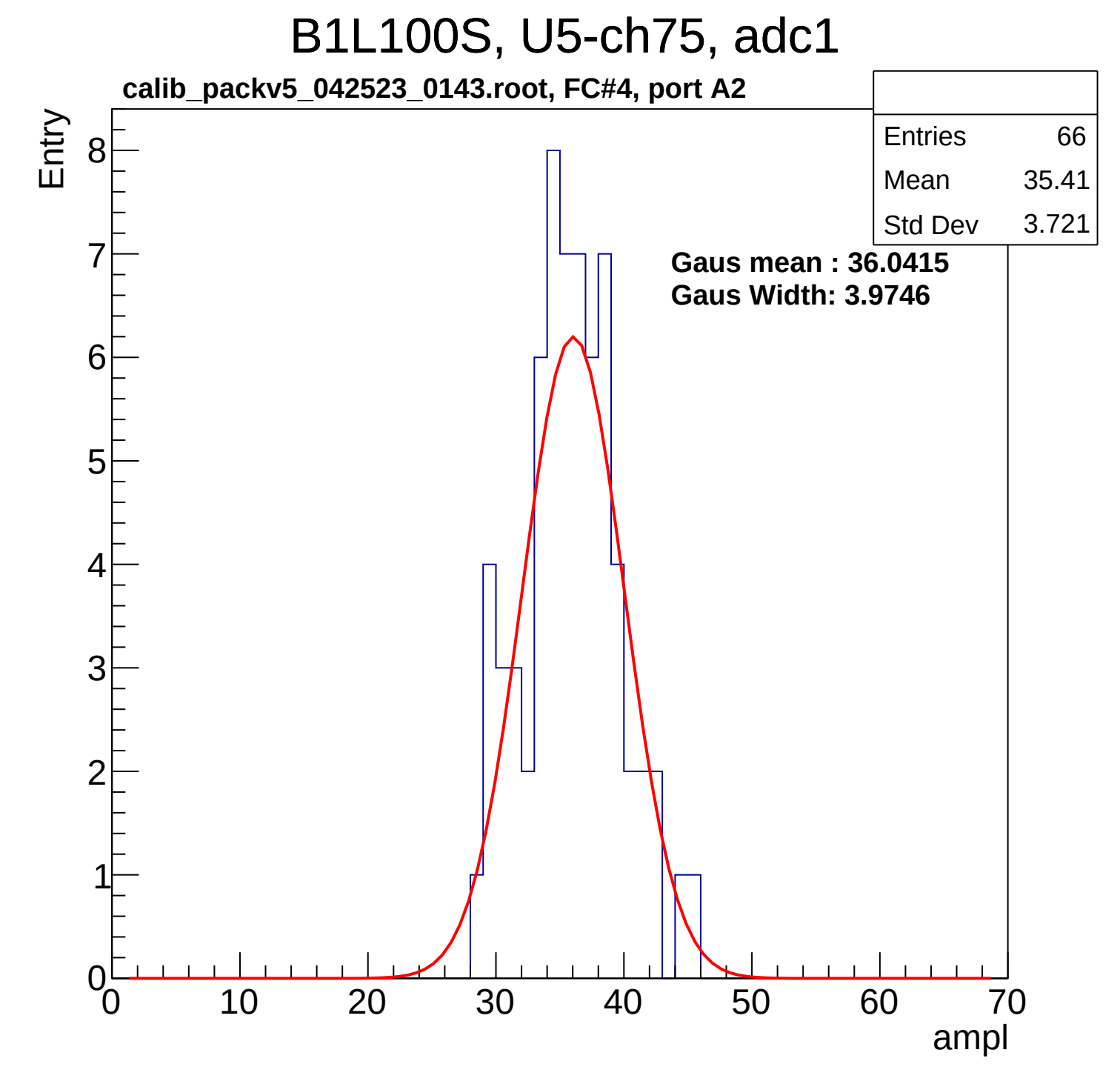
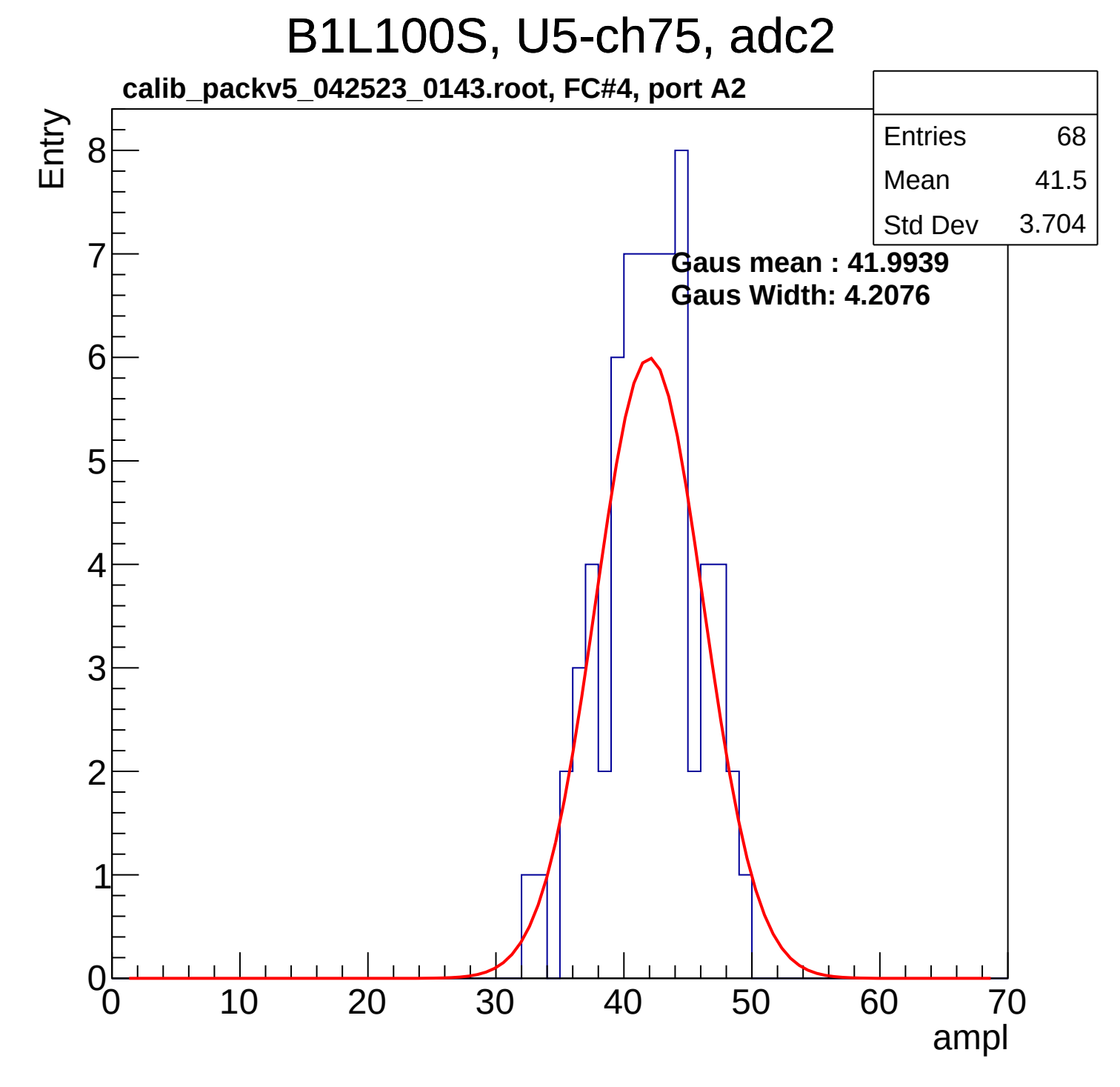
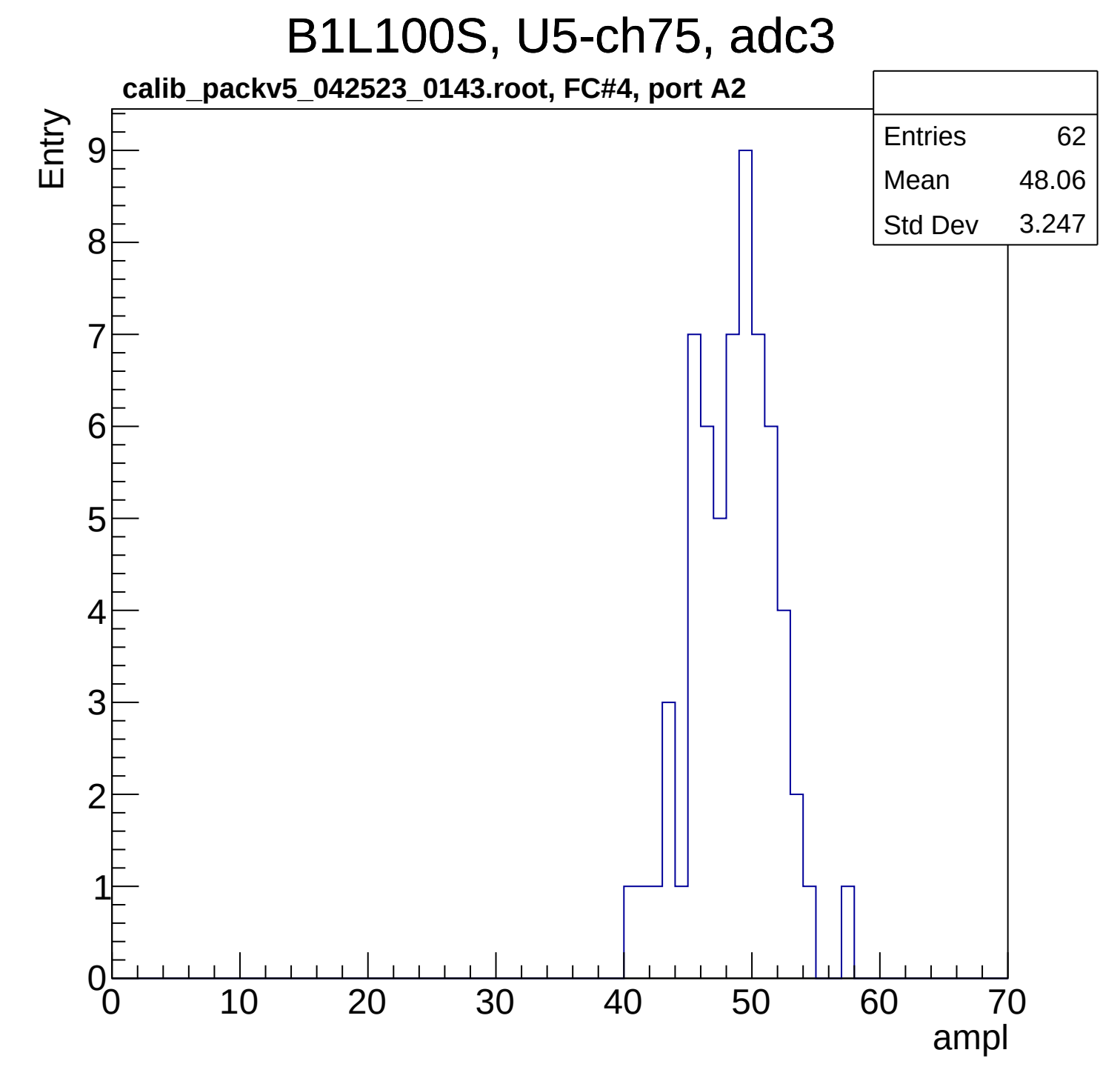
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L100S, U5-ch75, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 28.44
Std Dev 3.669
Gaus mean : 29.0400
Gaus Width: 3.8040
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U5-ch75, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 35.41
Std Dev 3.721
Gaus mean : 36.0415
Gaus Width: 3.9746
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch75, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 41.5
Std Dev 3.704
Gaus mean : 41.9939
Gaus Width: 4.2076
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch75, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 48.06
Std Dev 3.247
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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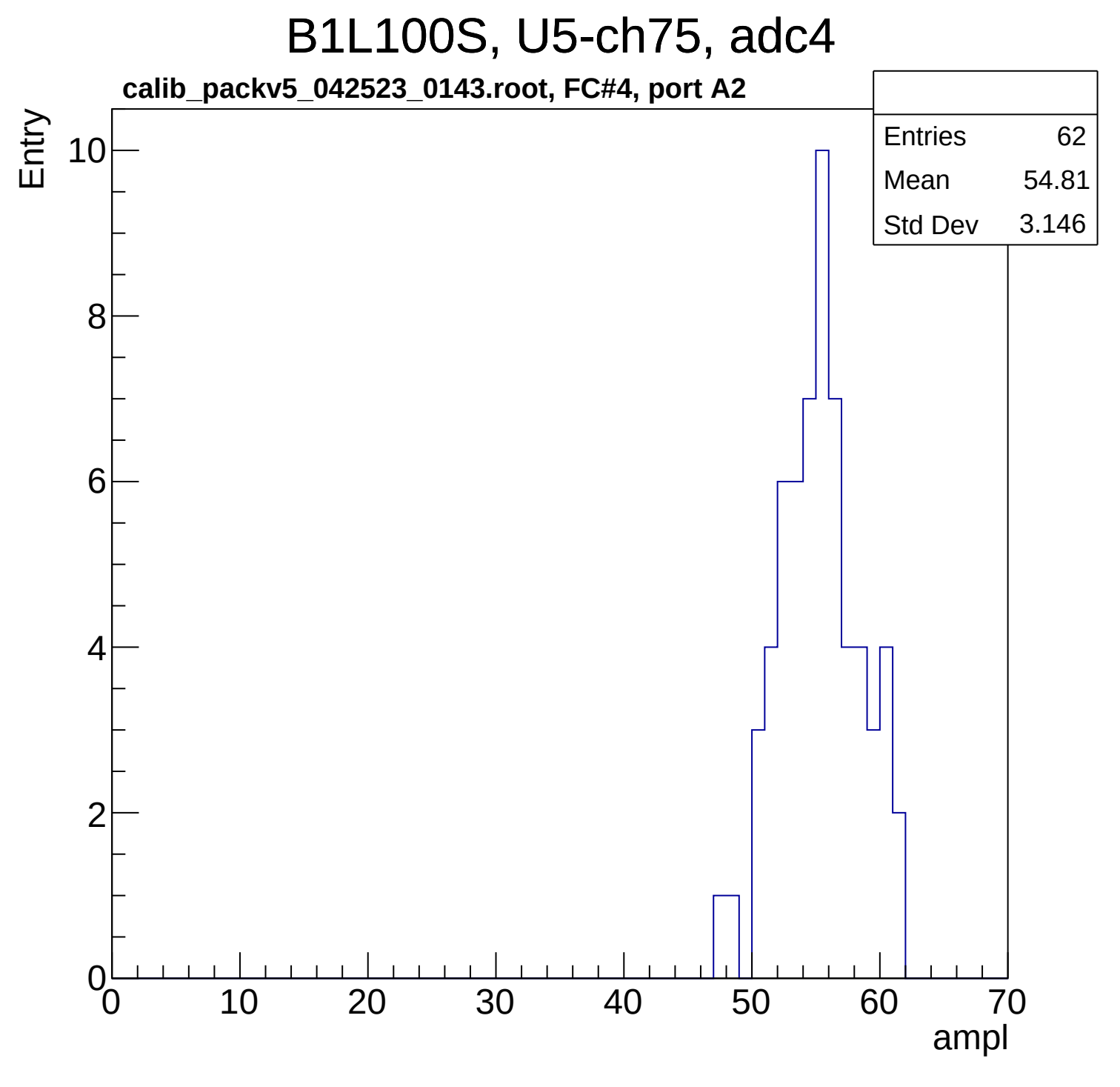
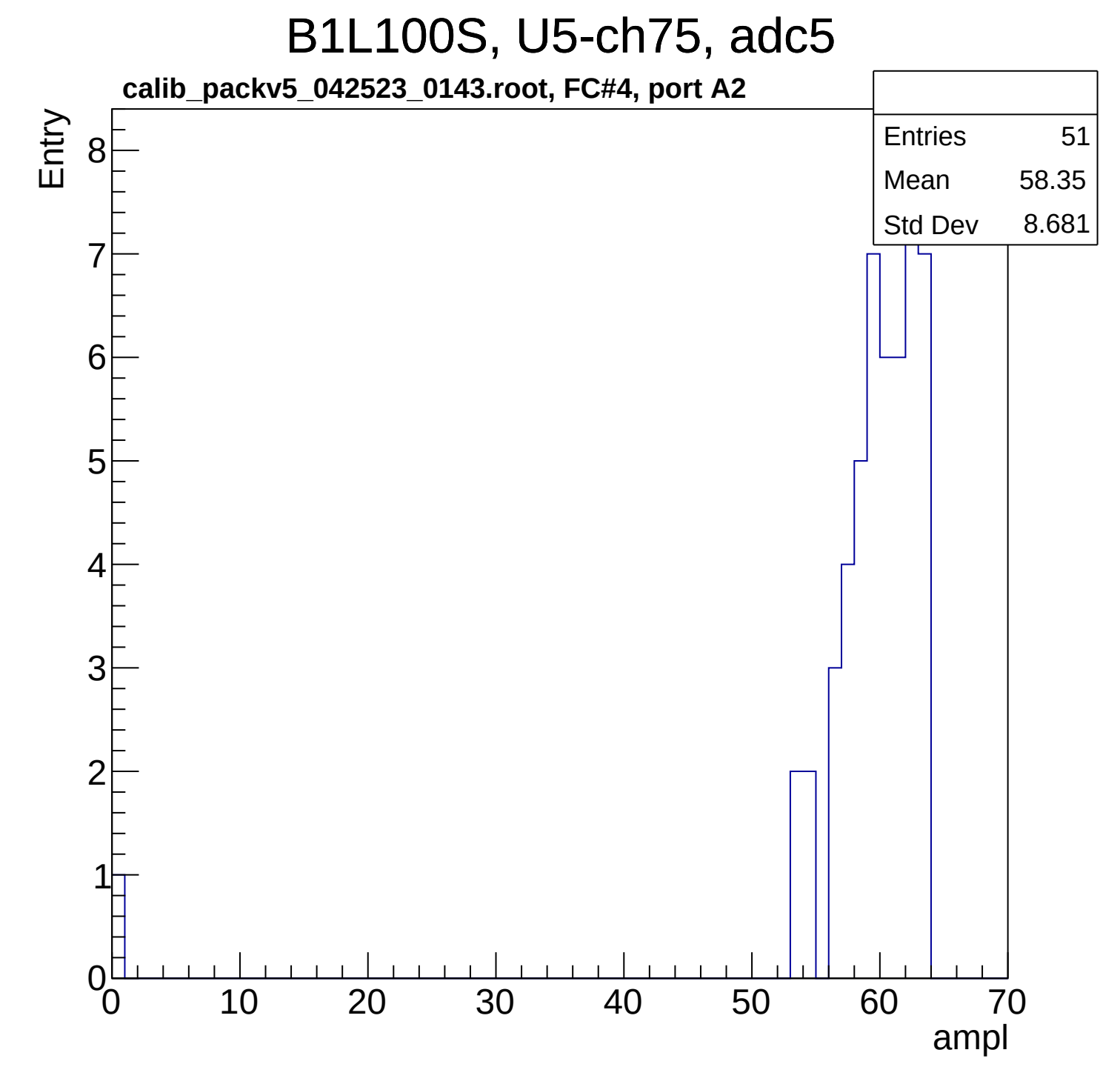
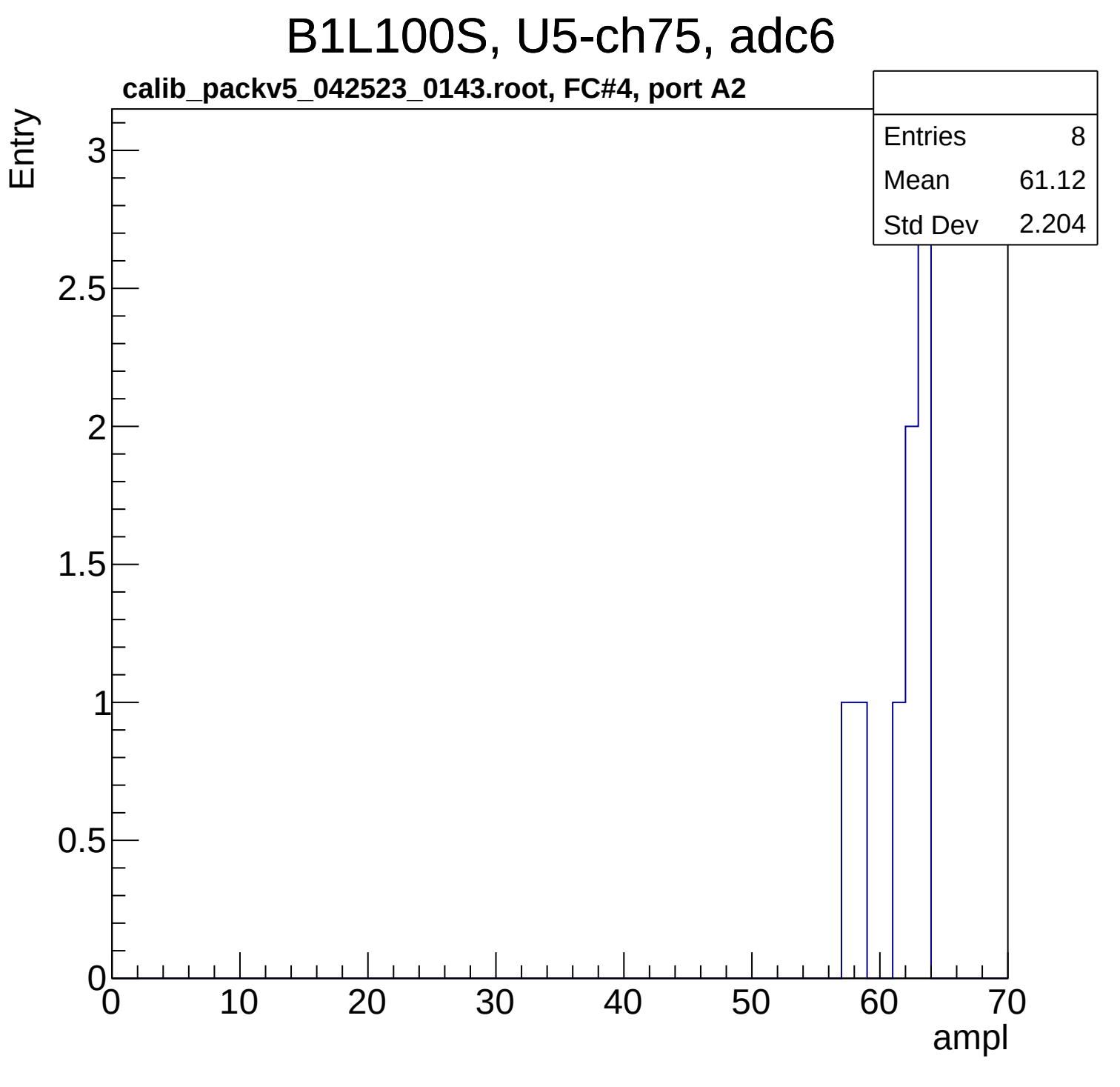
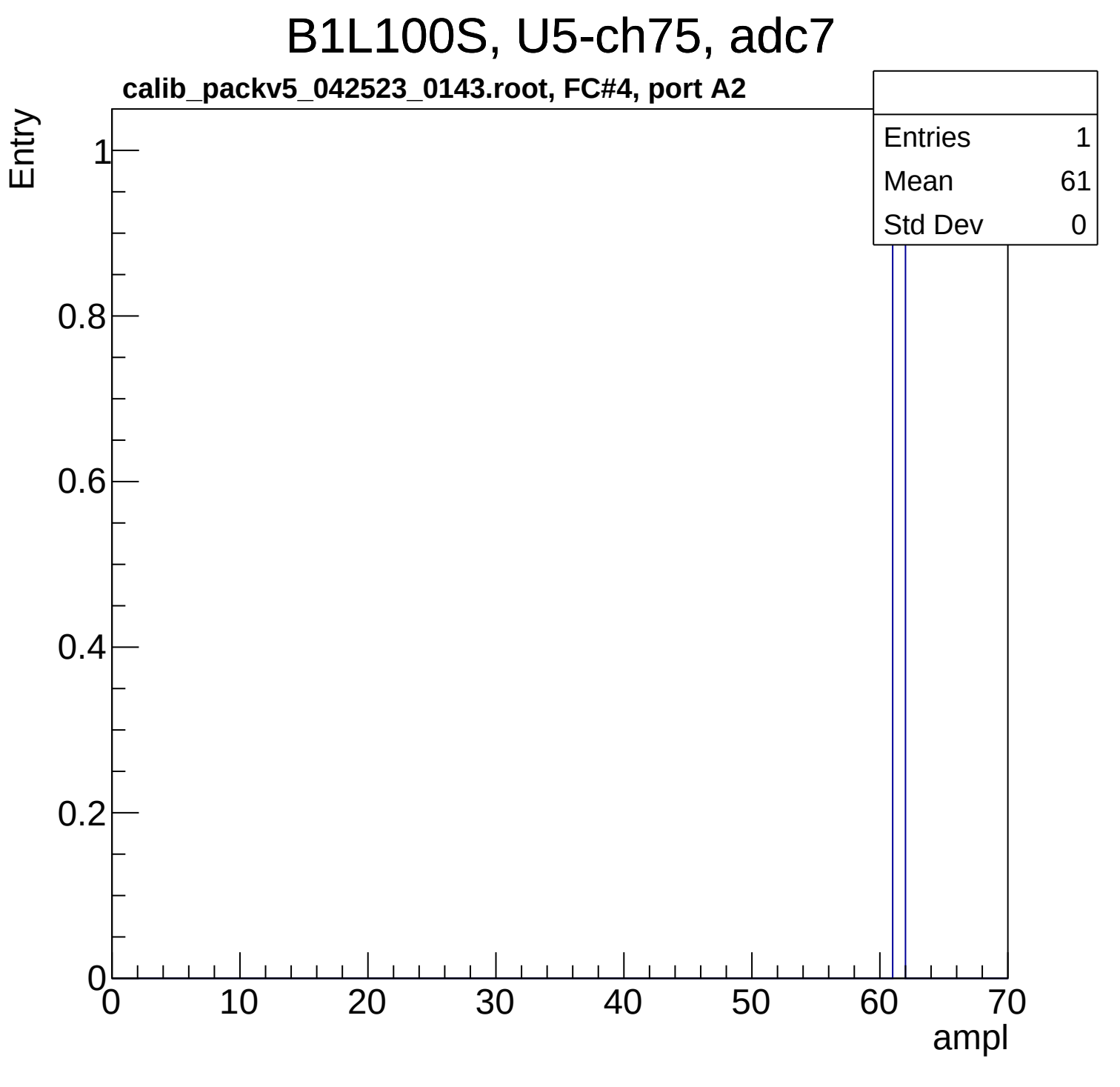
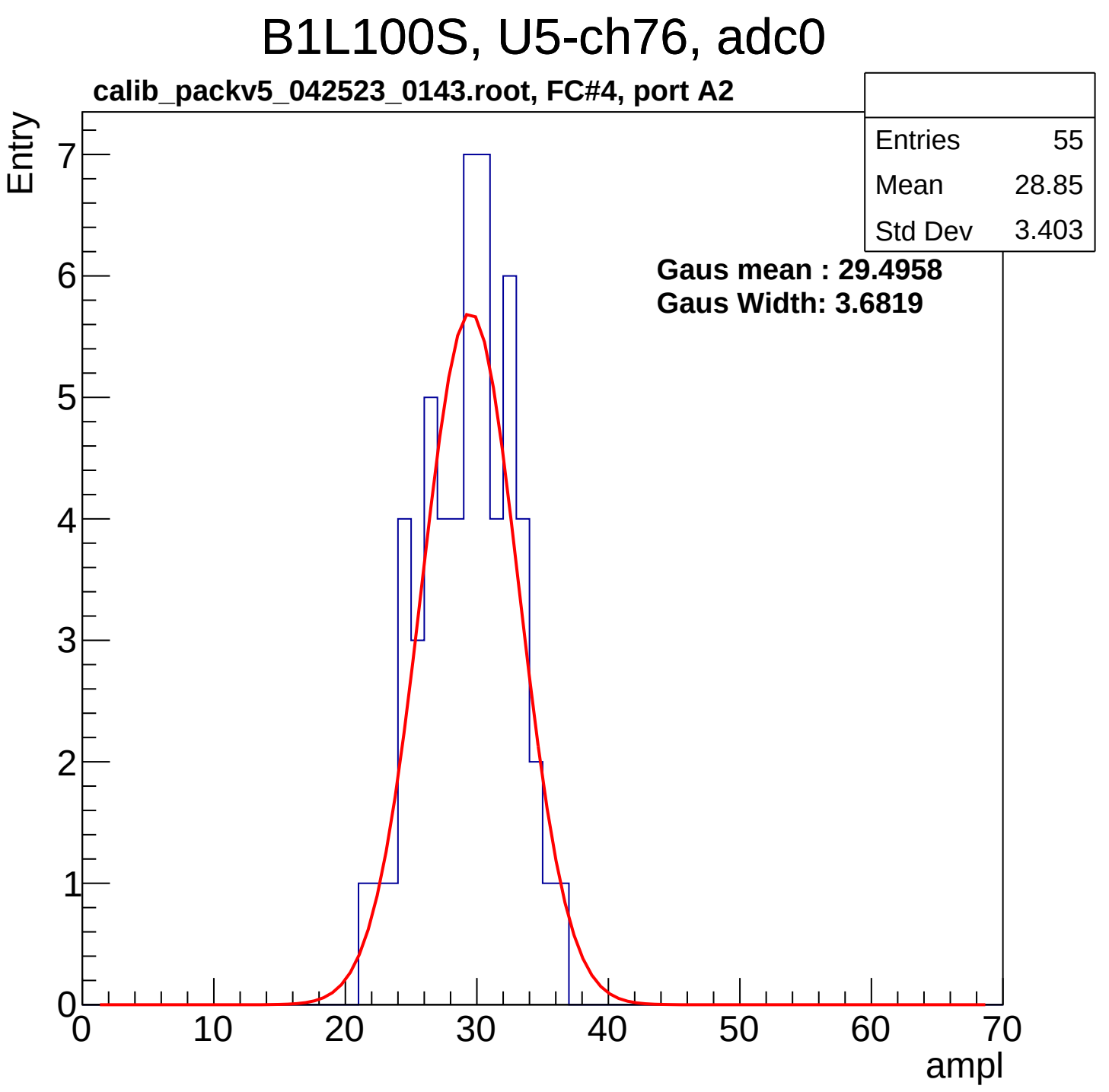
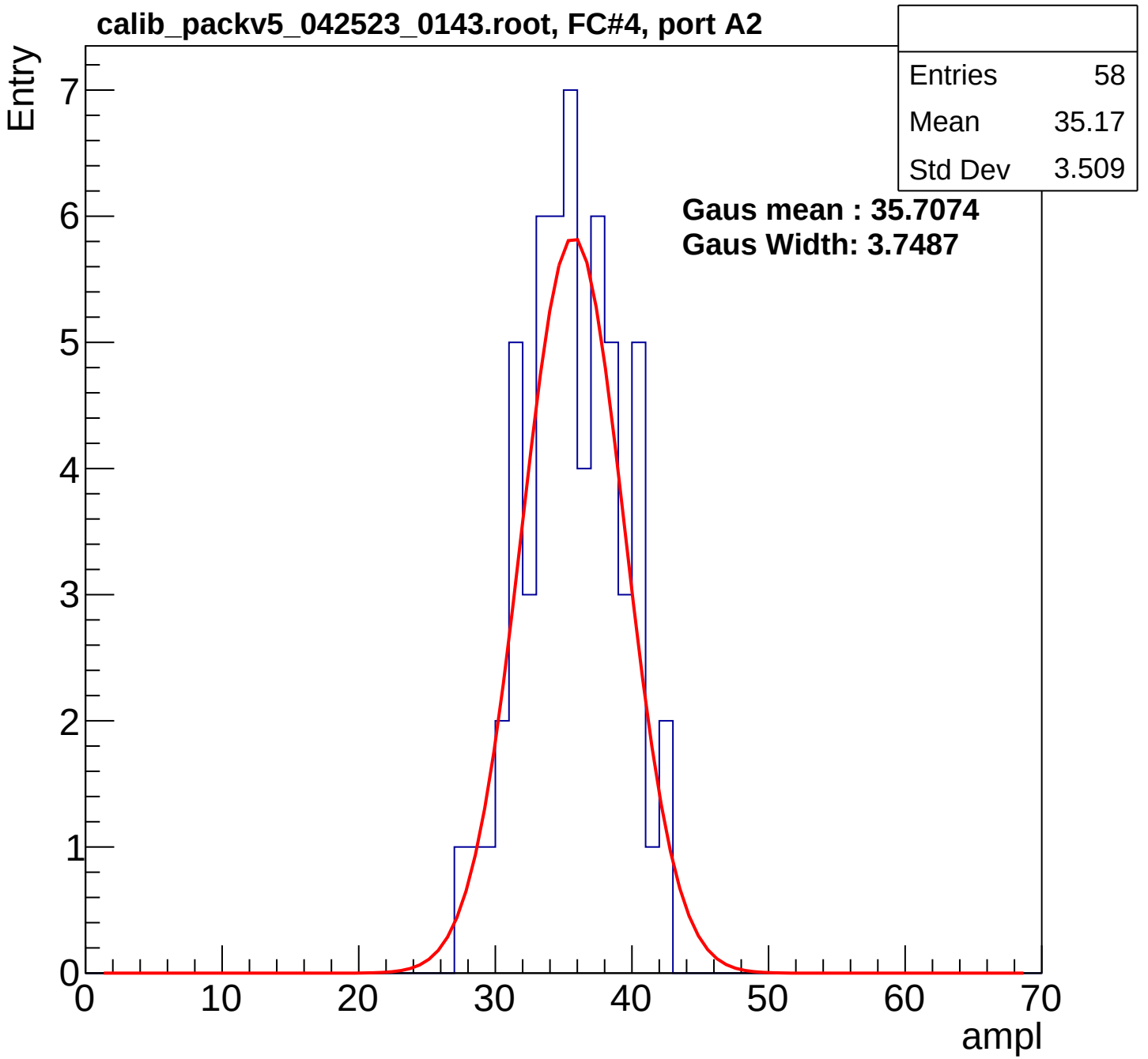

B1L100S, U5-ch75, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 54.81
Std Dev 3.146
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

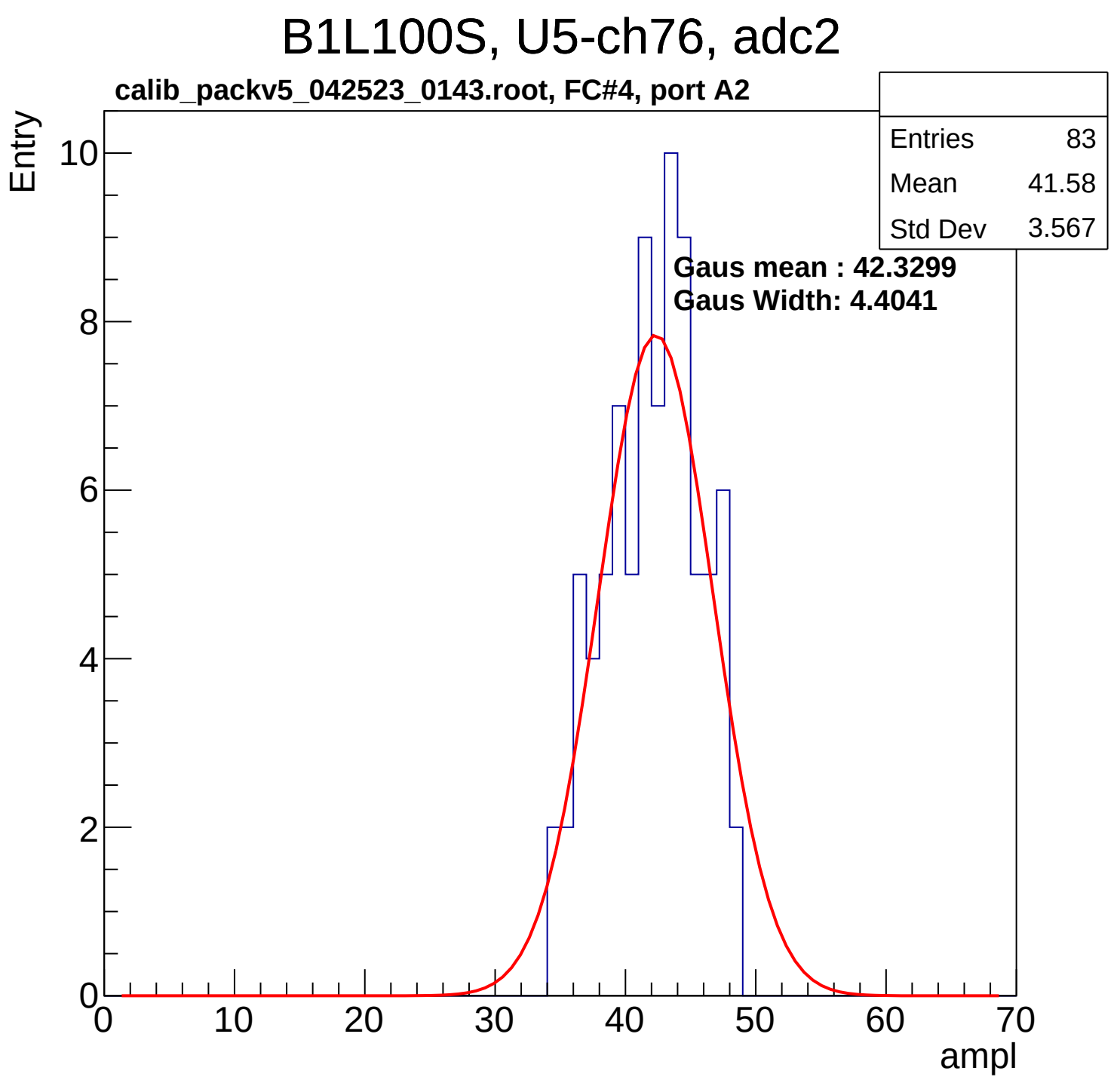

B1L100S, U5-ch75, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 58.35
Std Dev 8.681
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

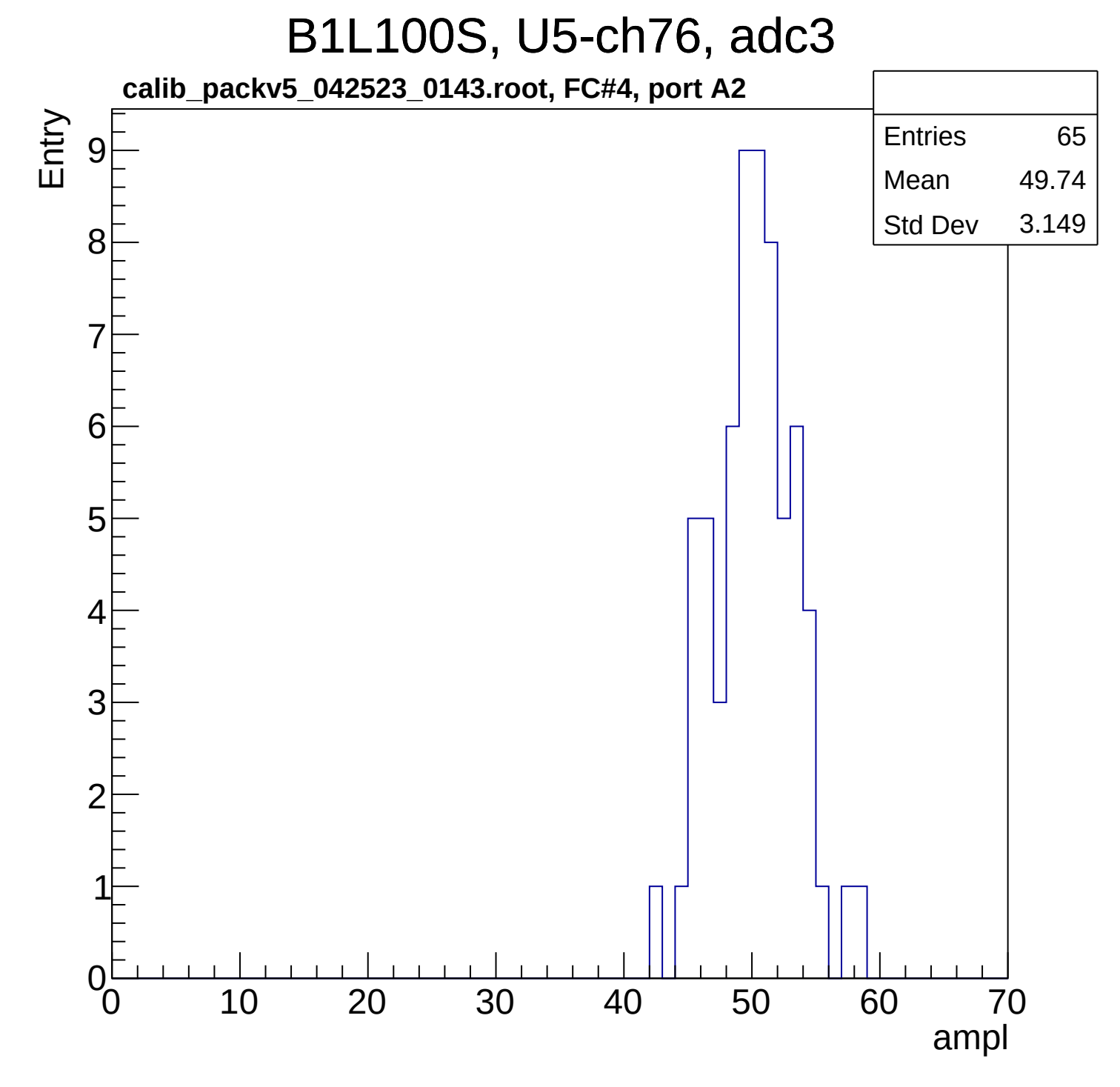

B1L100S, U5-ch75, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 8
Mean 61.12
Std Dev 2.204
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L100S, U5-ch75, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 61
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch76, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 28.85
Std Dev 3.403
Gaus mean : 29.4958
Gaus Width: 3.6819
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U5-ch76, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 35.17
Std Dev 3.509
Gaus mean : 35.7074
Gaus Width: 3.7487
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U5-ch76, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 83
Mean 41.58
Std Dev 3.567
Gaus mean : 42.3299
Gaus Width: 4.4041
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch76, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 49.74
Std Dev 3.149
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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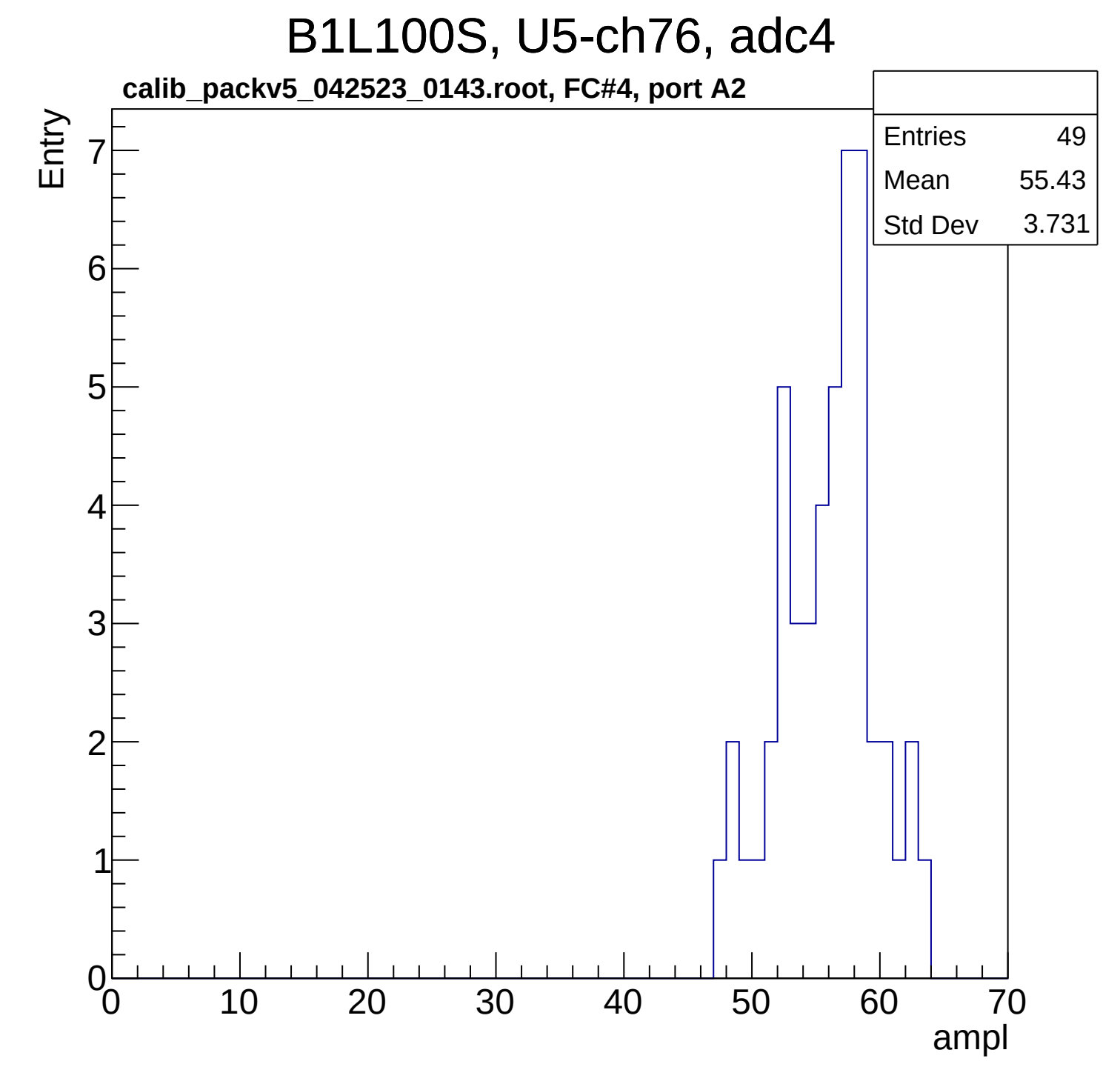
B1L100S, U5-ch76, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 49
Mean 55.43
Std Dev 3.731
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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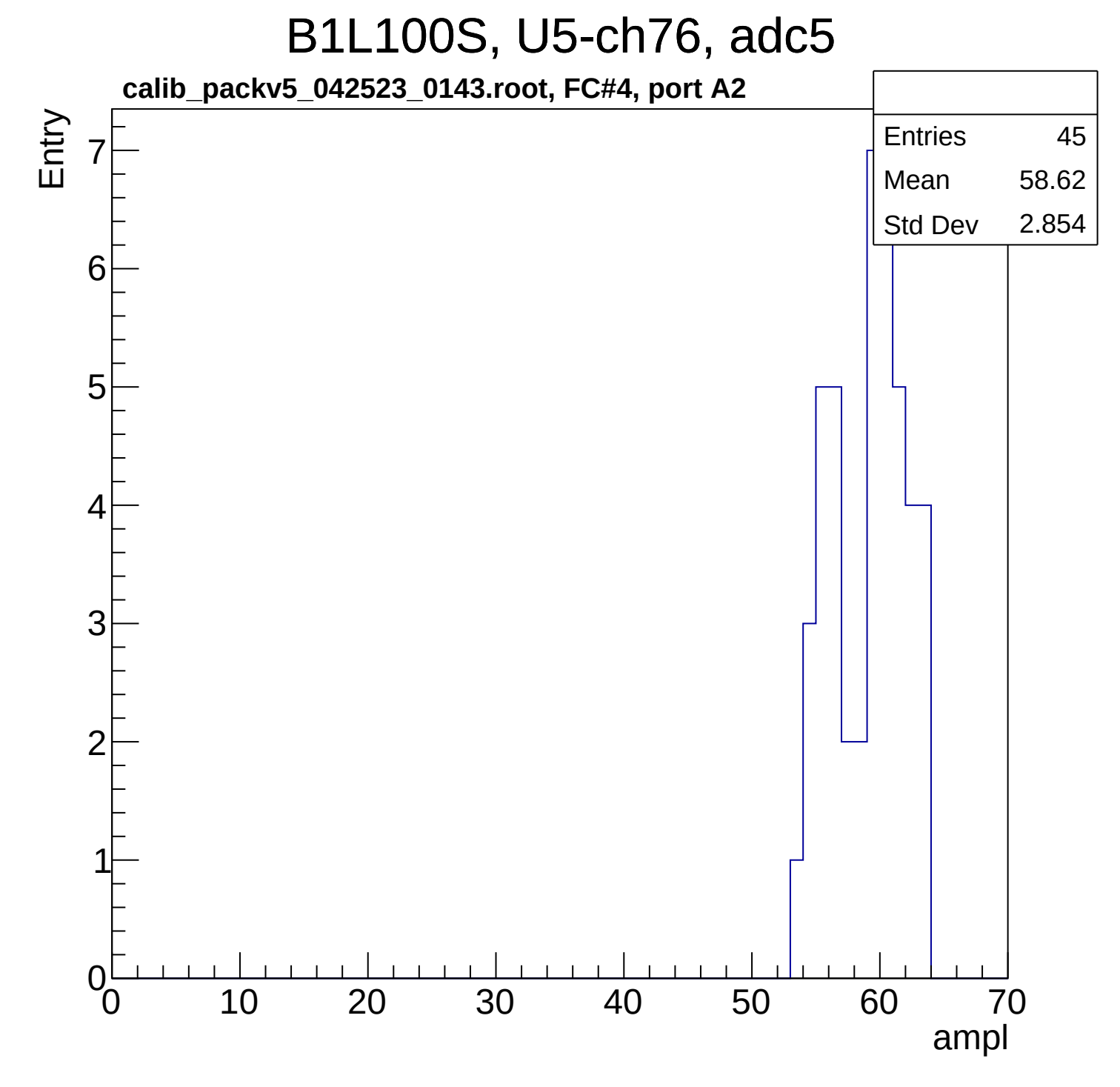
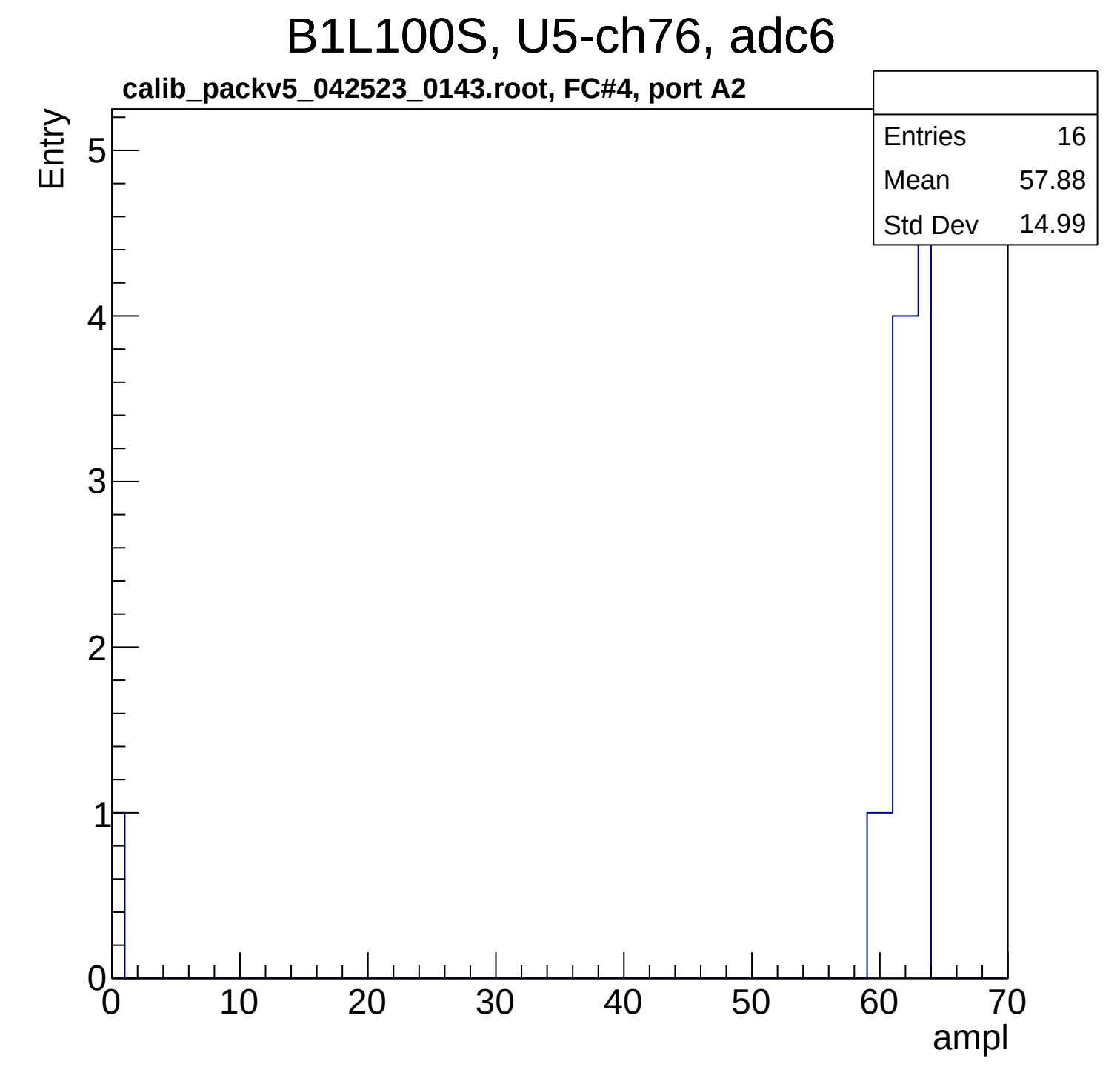
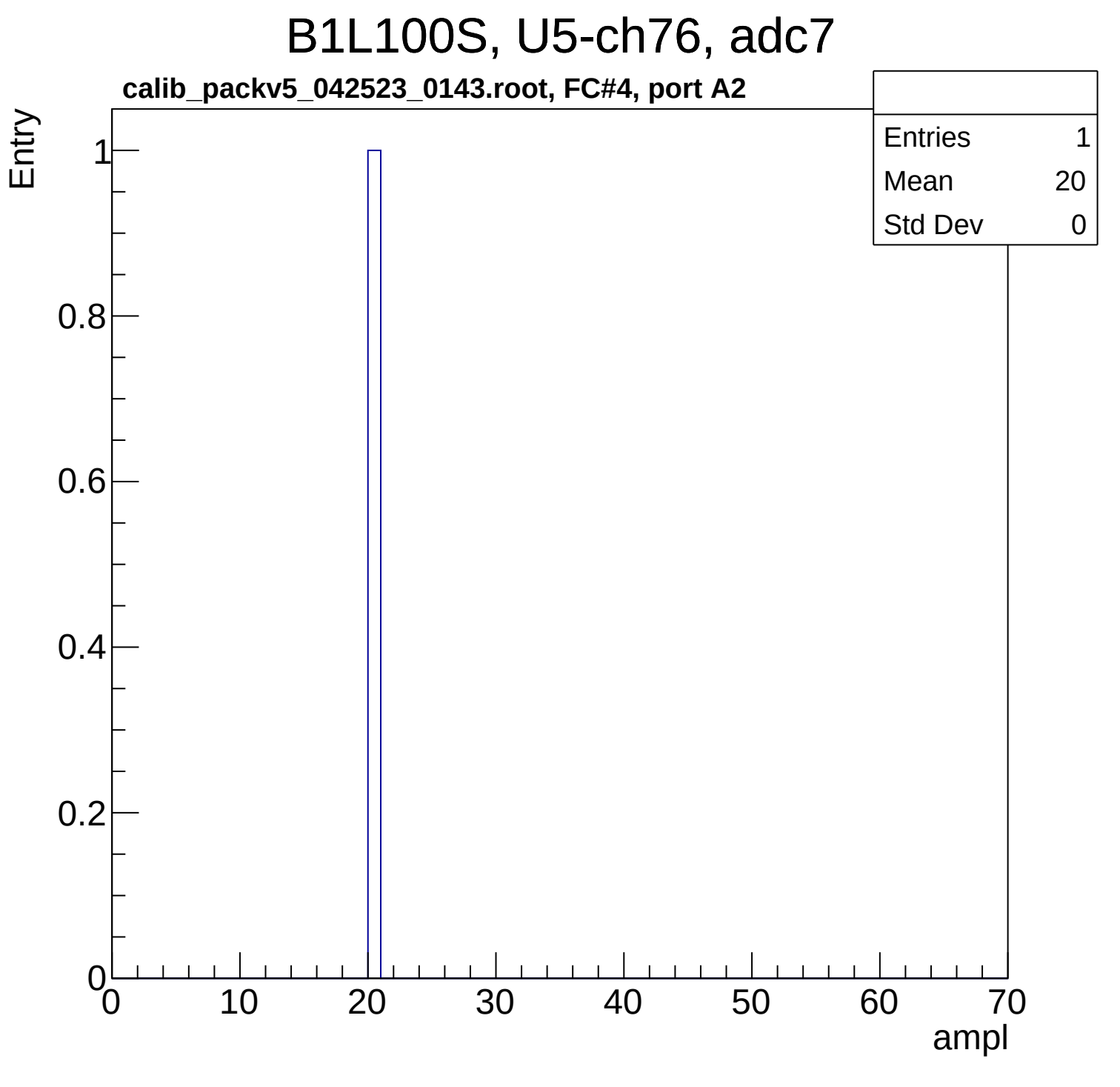
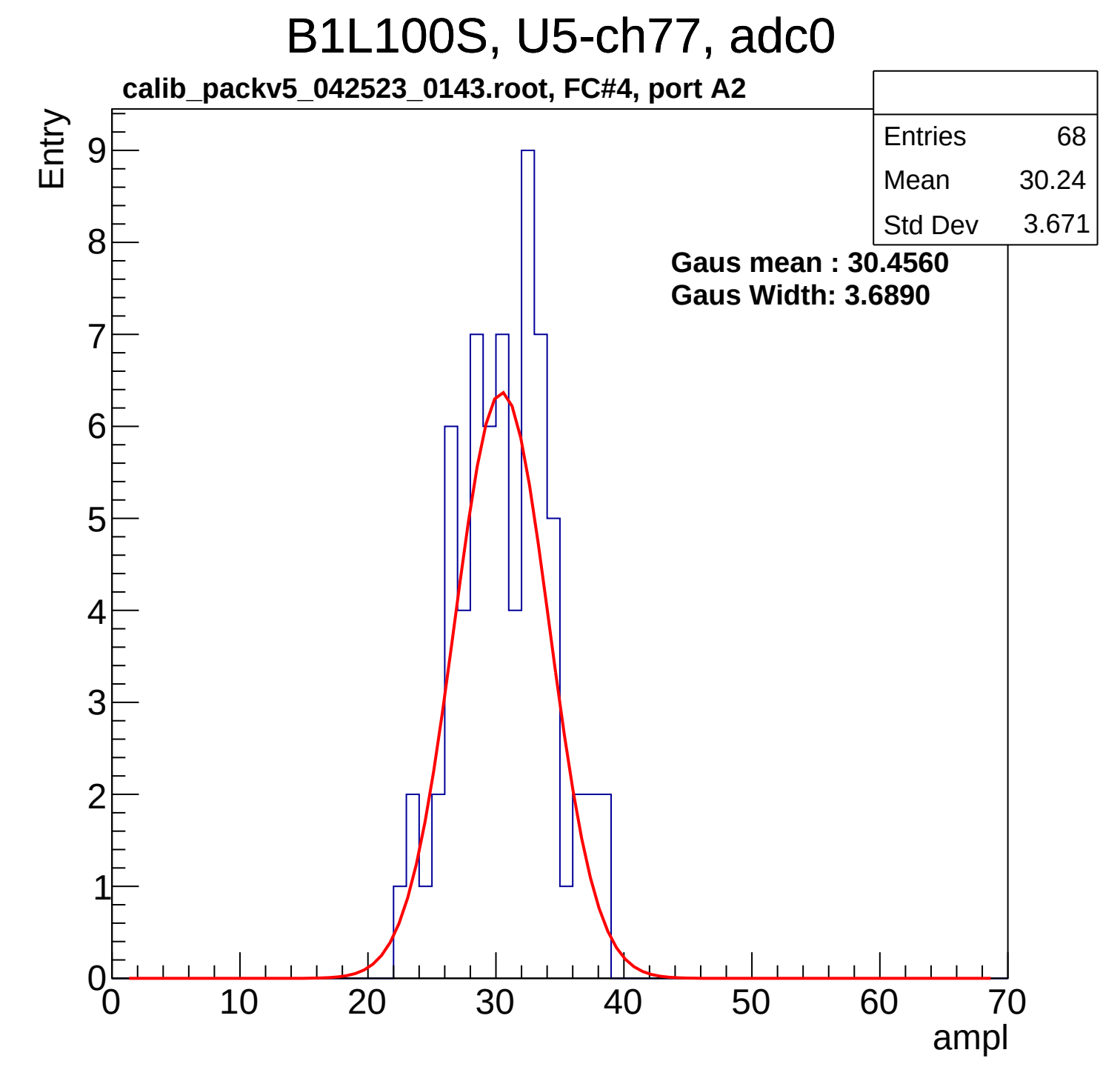
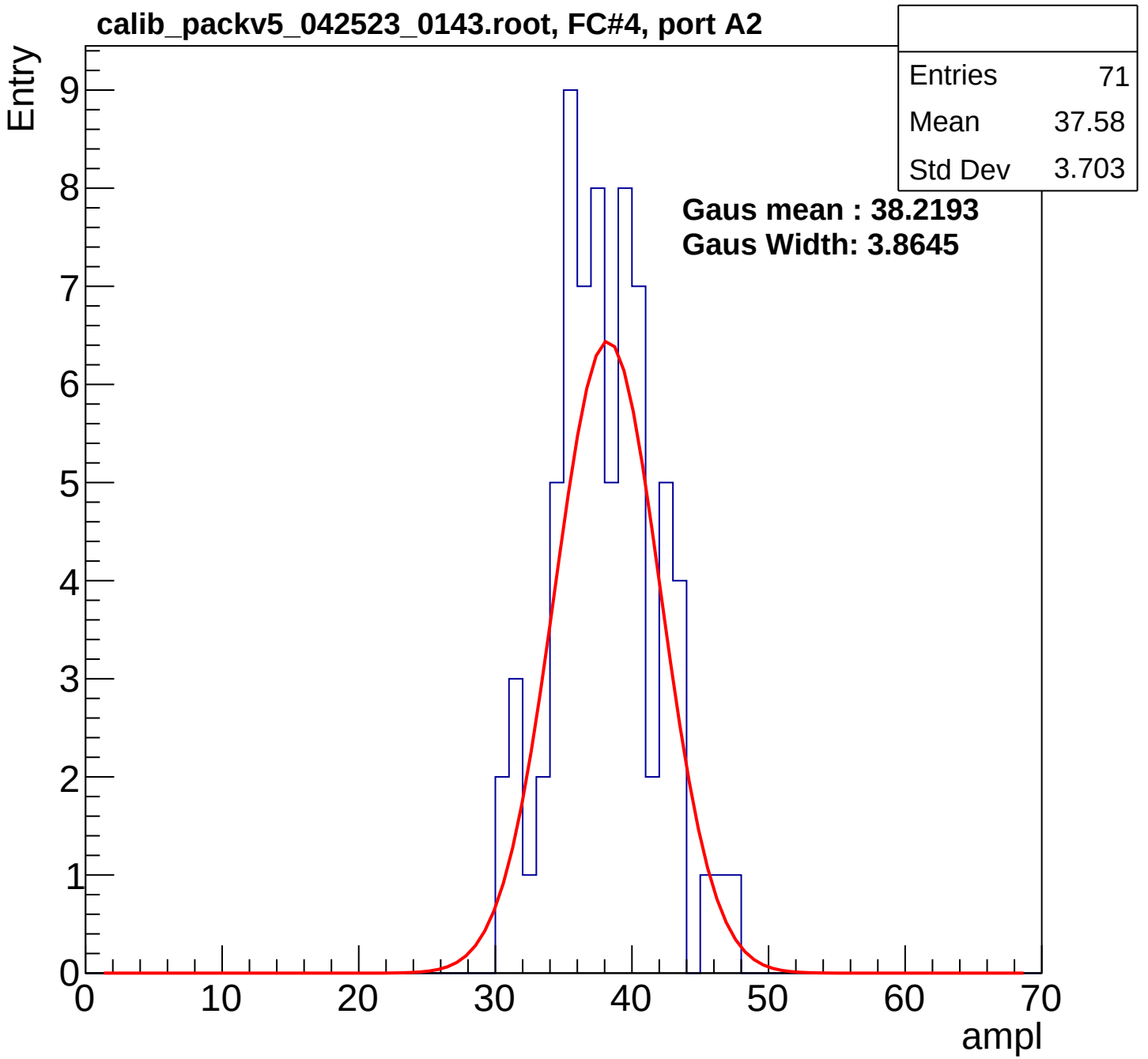
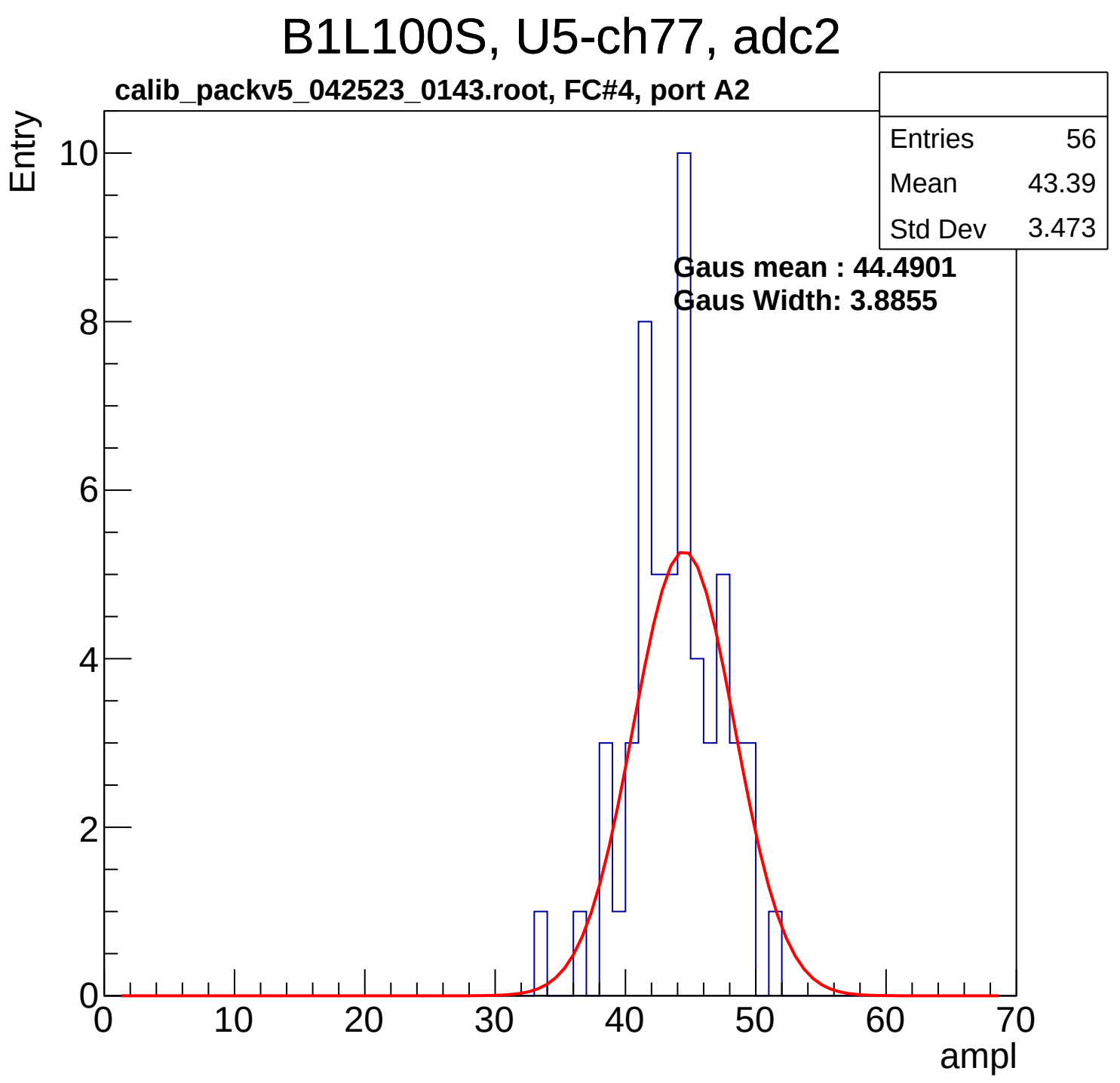

B1L100S, U5-ch76, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 45
Mean 58.62
Std Dev 2.854
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

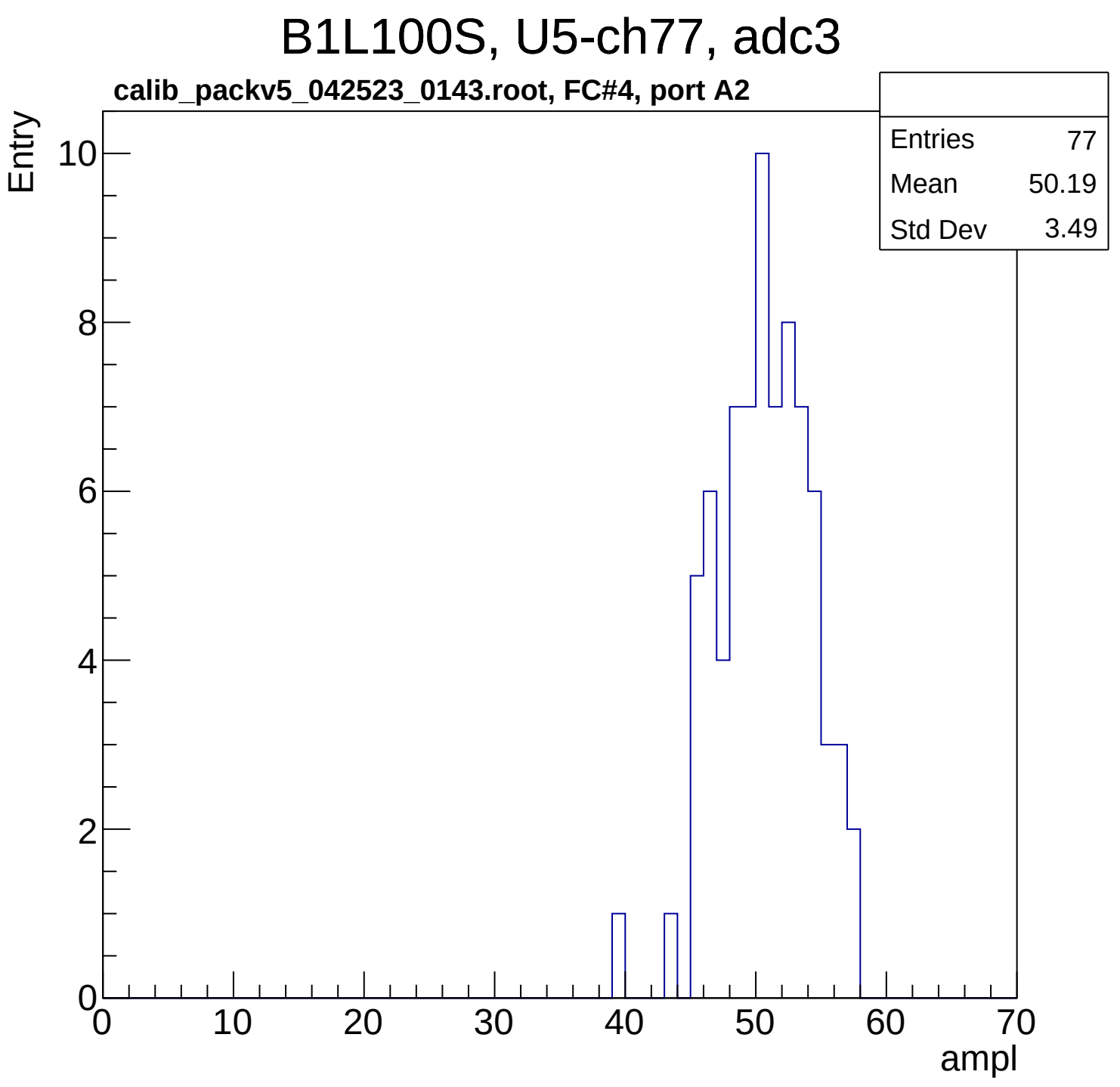

B1L100S, U5-ch76, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 16
Mean 57.88
Std Dev 14.99
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

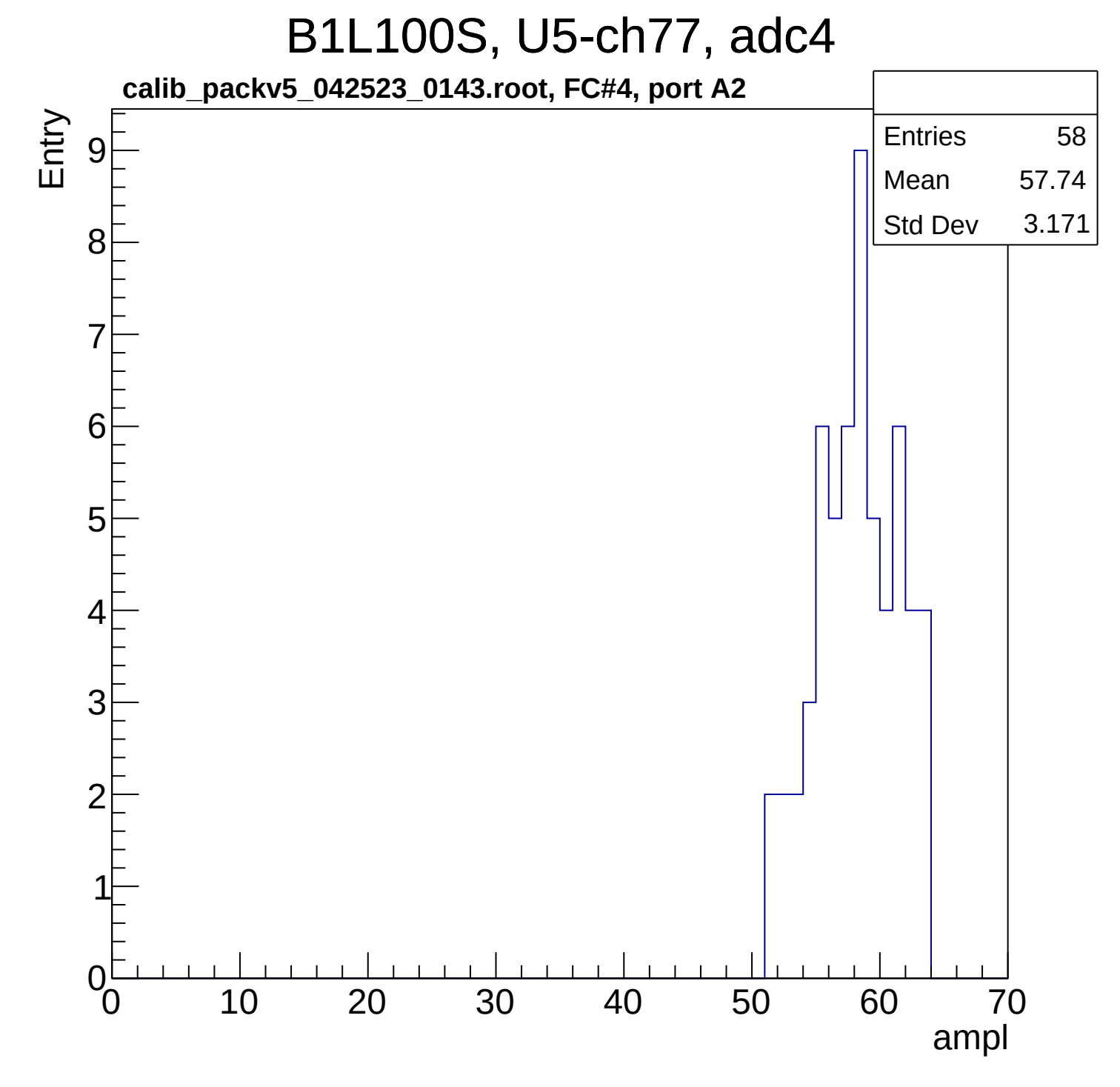

B1L100S, U5-ch76, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 20
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch77, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 30.24
Std Dev 3.671
Gaus mean : 30.4560
Gaus Width: 3.6890
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch77, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 37.58
Std Dev 3.703
Gaus mean : 38.2193
Gaus Width: 3.8645
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch77, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 43.39
Std Dev 3.473
Gaus mean : 44.4901
Gaus Width: 3.8855
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch77, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 77
Mean 50.19
Std Dev 3.49
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch77, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 57.74
Std Dev 3.171
Entry
ampl
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2
3
4
5
6
7
8
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0
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20
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40
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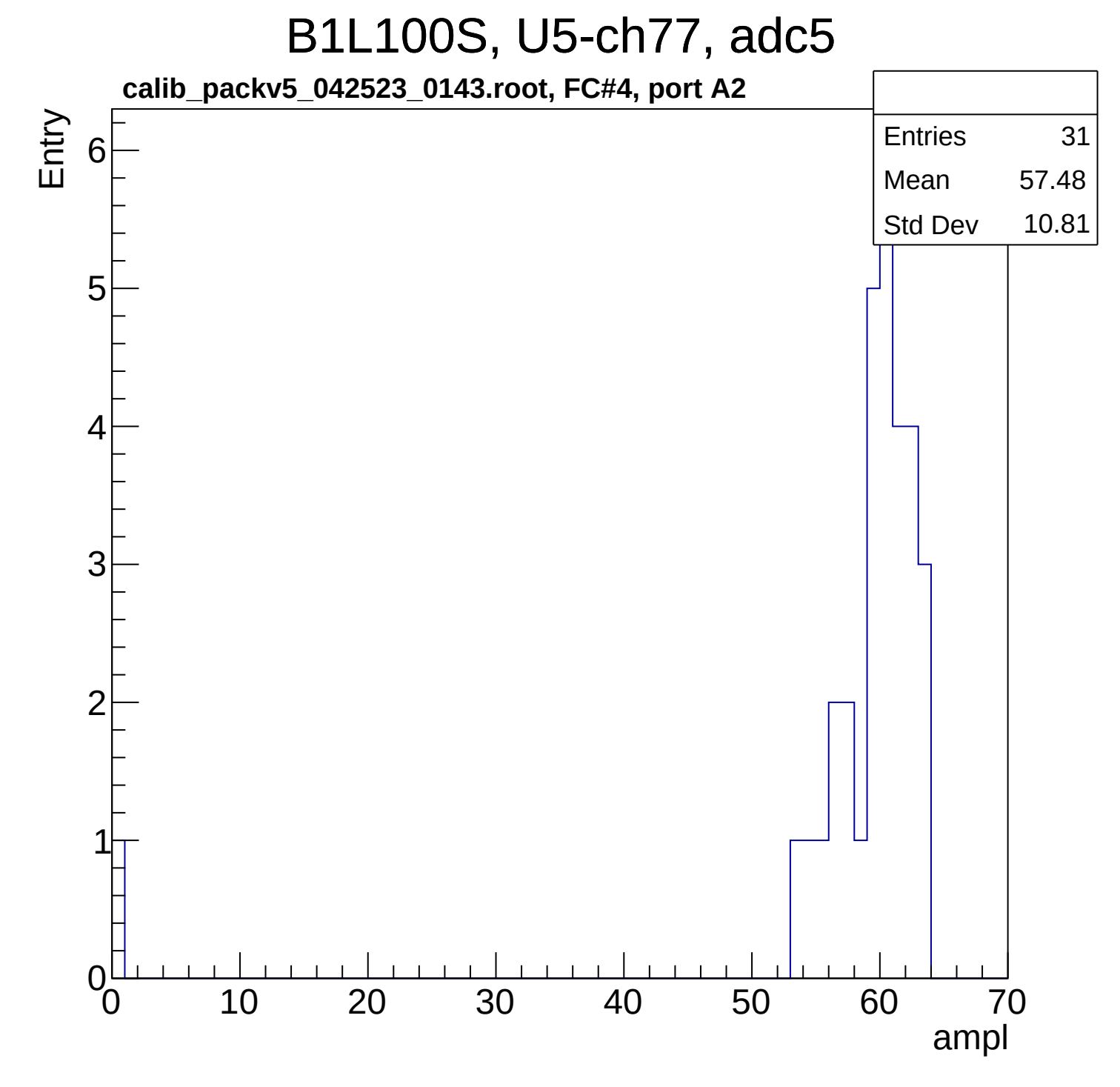
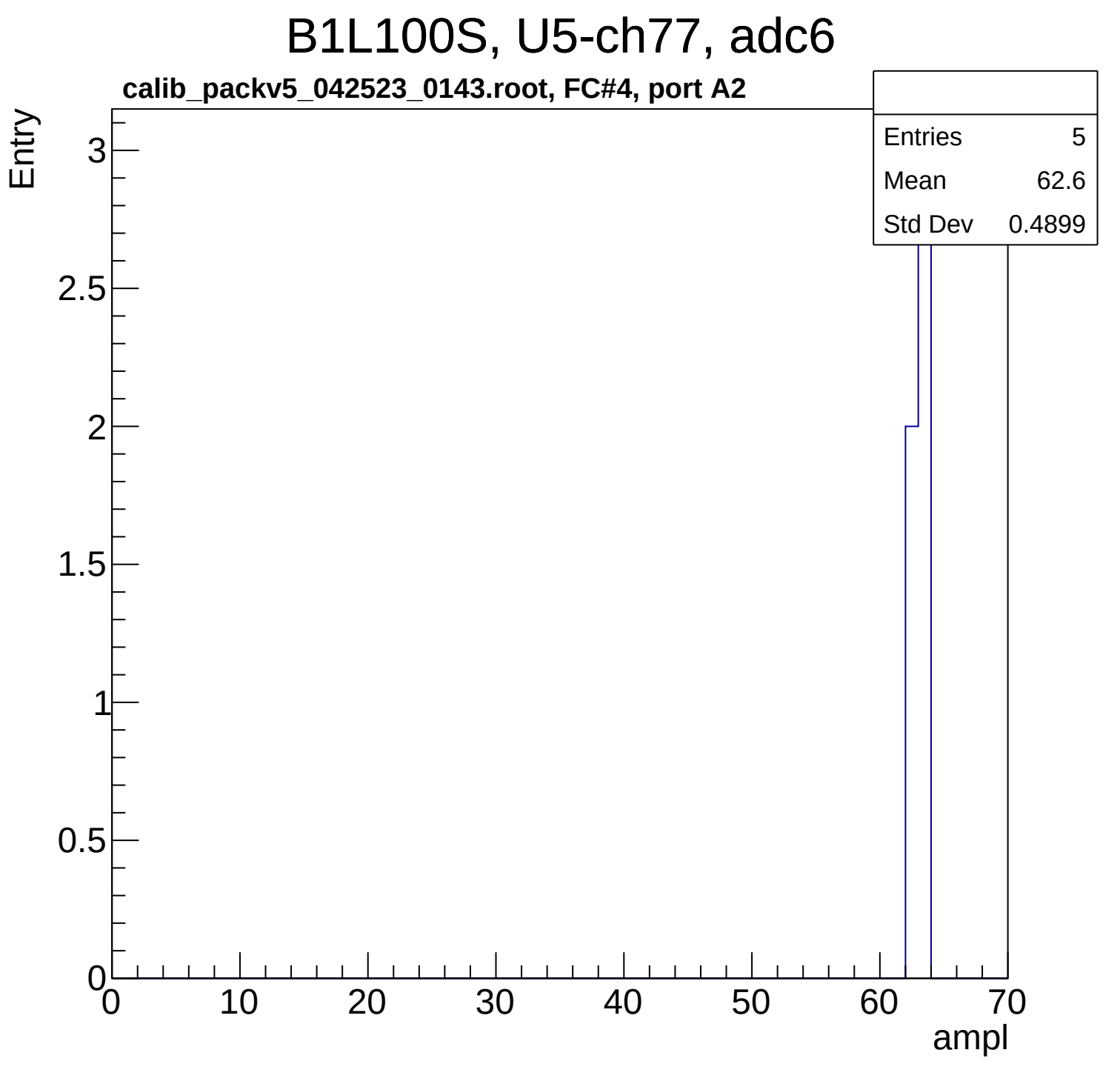
60
70


B1L100S, U5-ch77, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 31
Mean 57.48
Std Dev 10.81
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch77, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 5
Mean 62.6
Std Dev 0.4899
Entry
ampl
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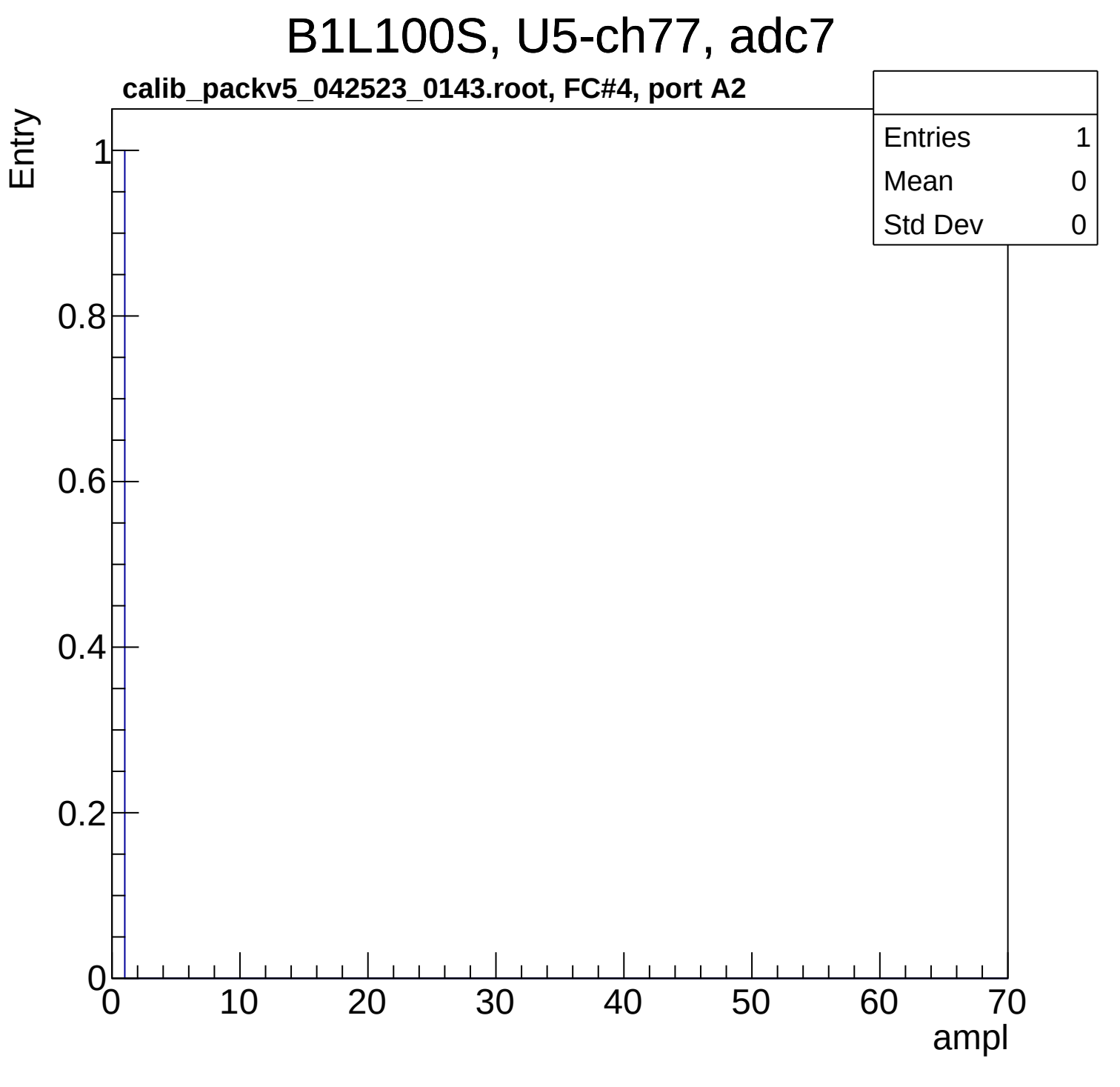
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L100S, U5-ch77, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
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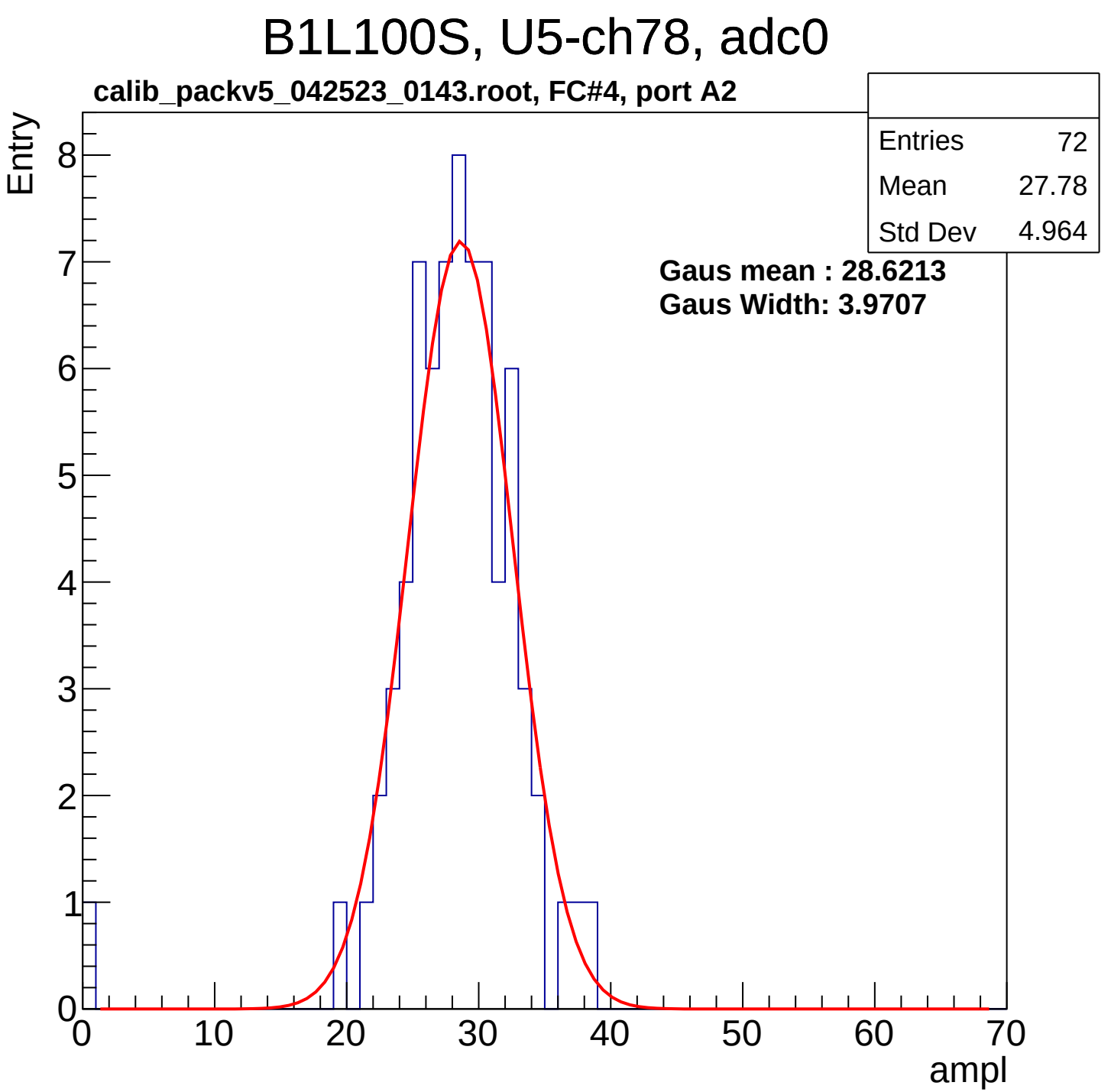
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch78, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 27.78
Std Dev 4.964
Gaus mean : 28.6213
Gaus Width: 3.9707
Entry
ampl
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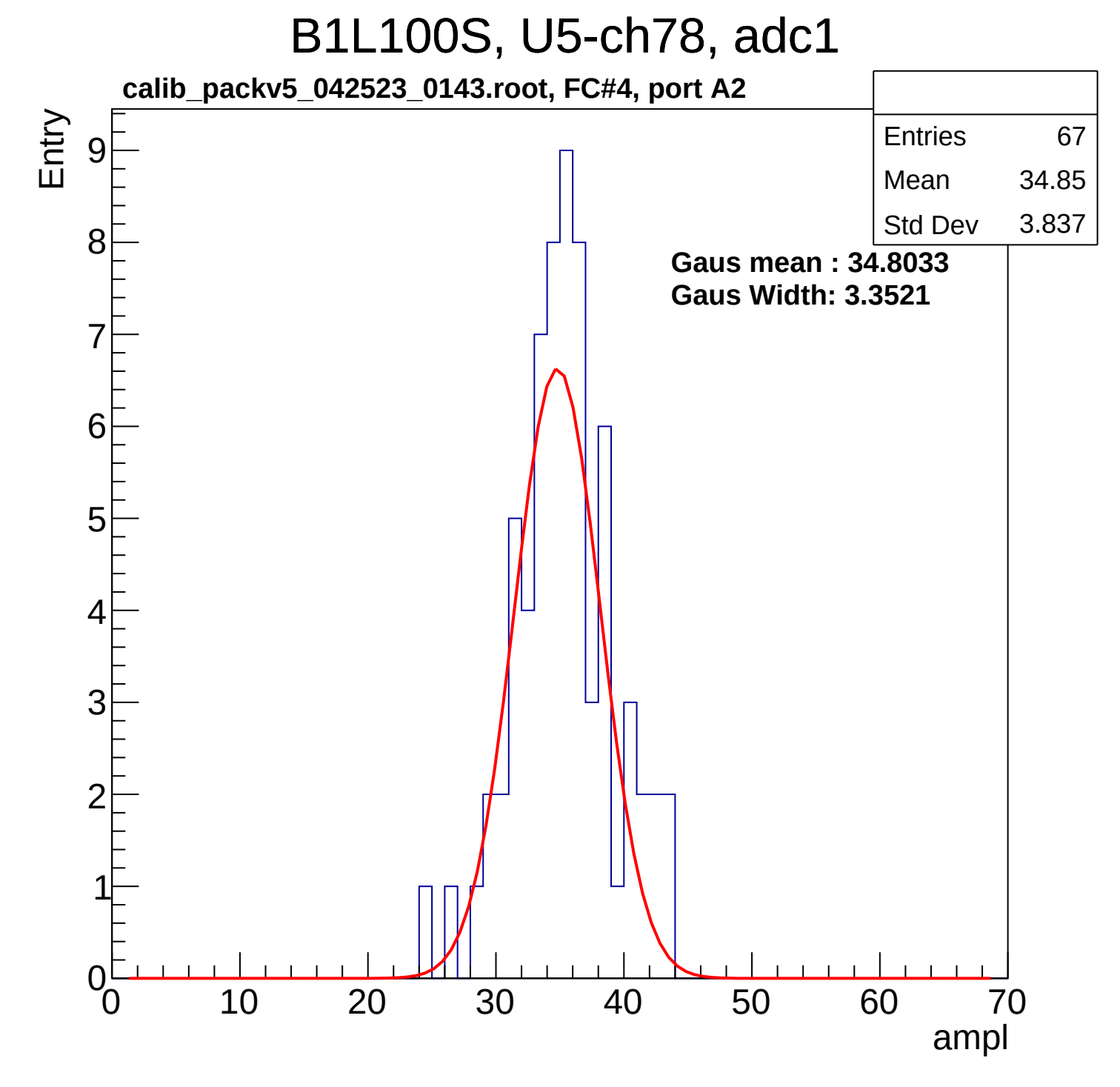
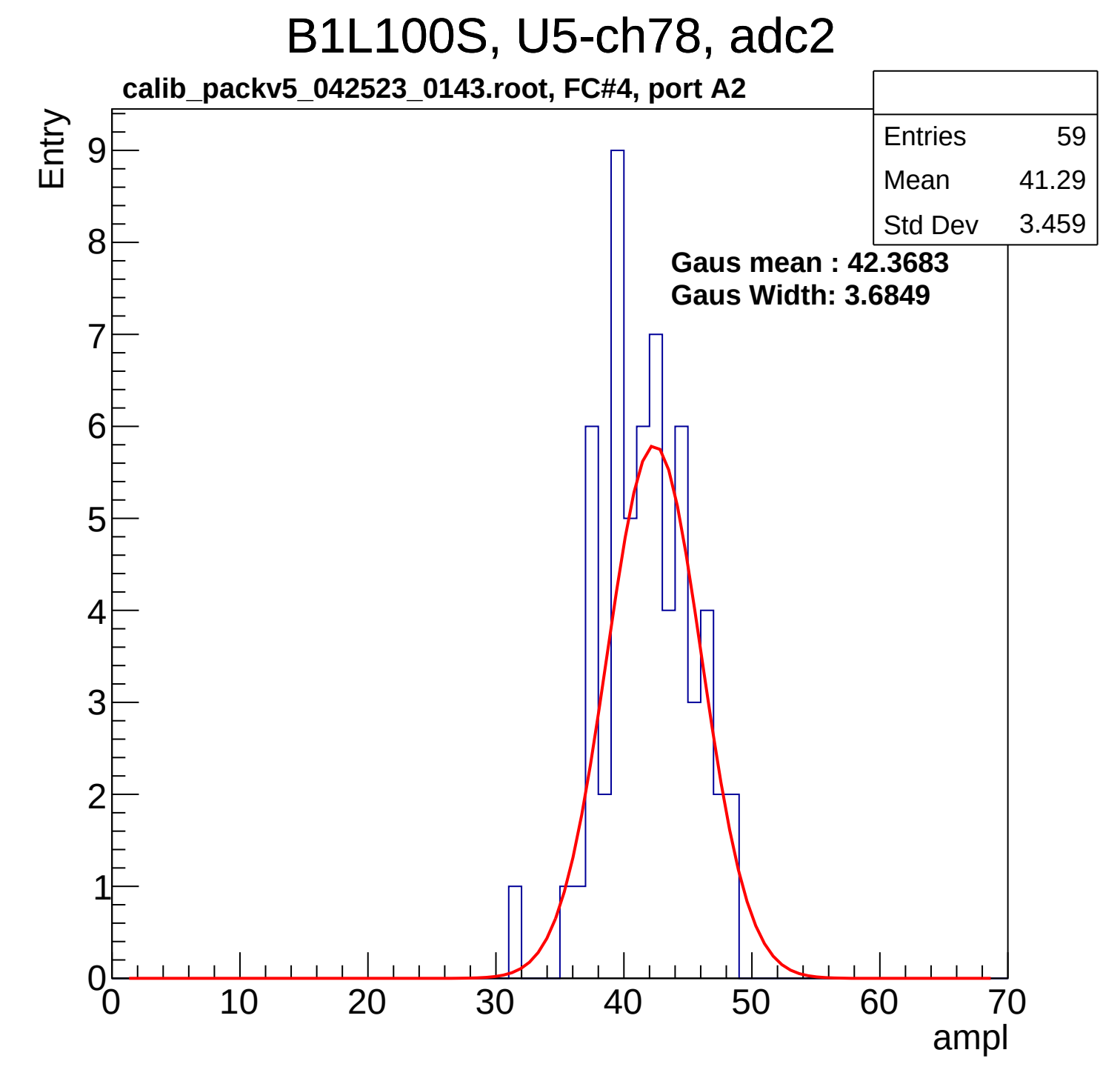
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch78, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 34.85
Std Dev 3.837
Gaus mean : 34.8033
Gaus Width: 3.3521
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch78, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 41.29
Std Dev 3.459
Gaus mean : 42.3683
Gaus Width: 3.6849
Entry
ampl
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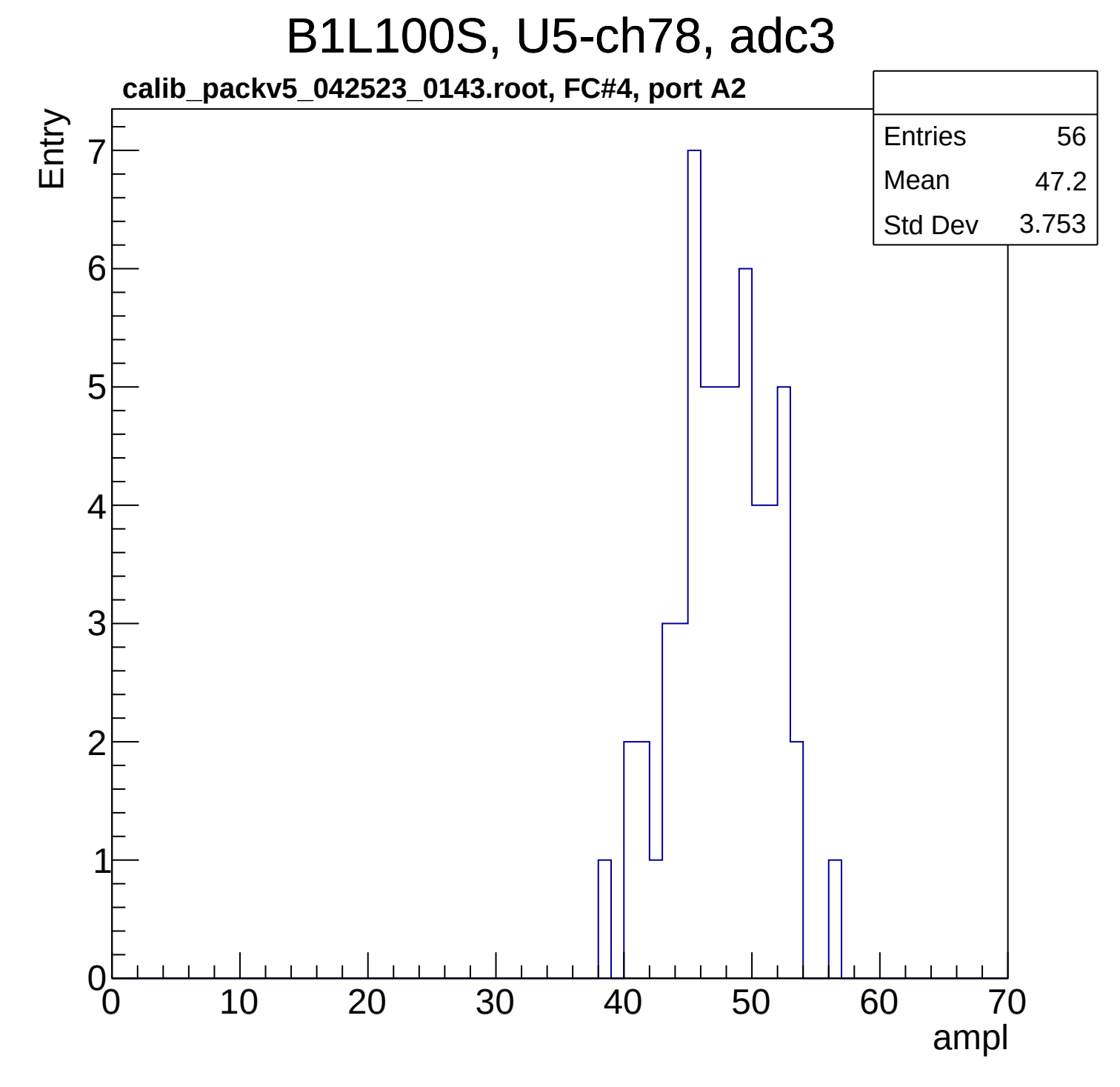
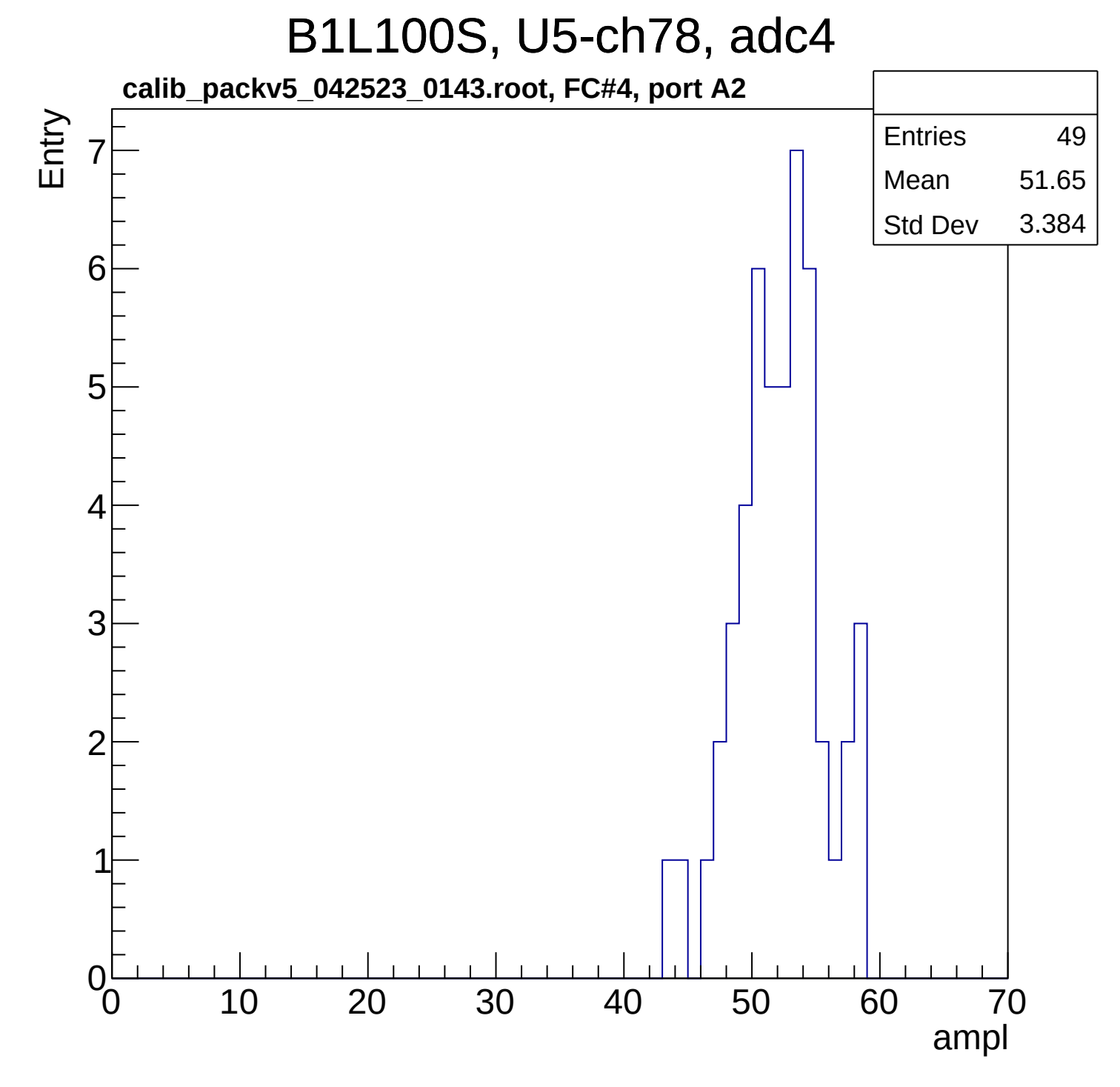
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L100S, U5-ch78, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 47.2
Std Dev 3.753
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U5-ch78, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 49
Mean 51.65
Std Dev 3.384
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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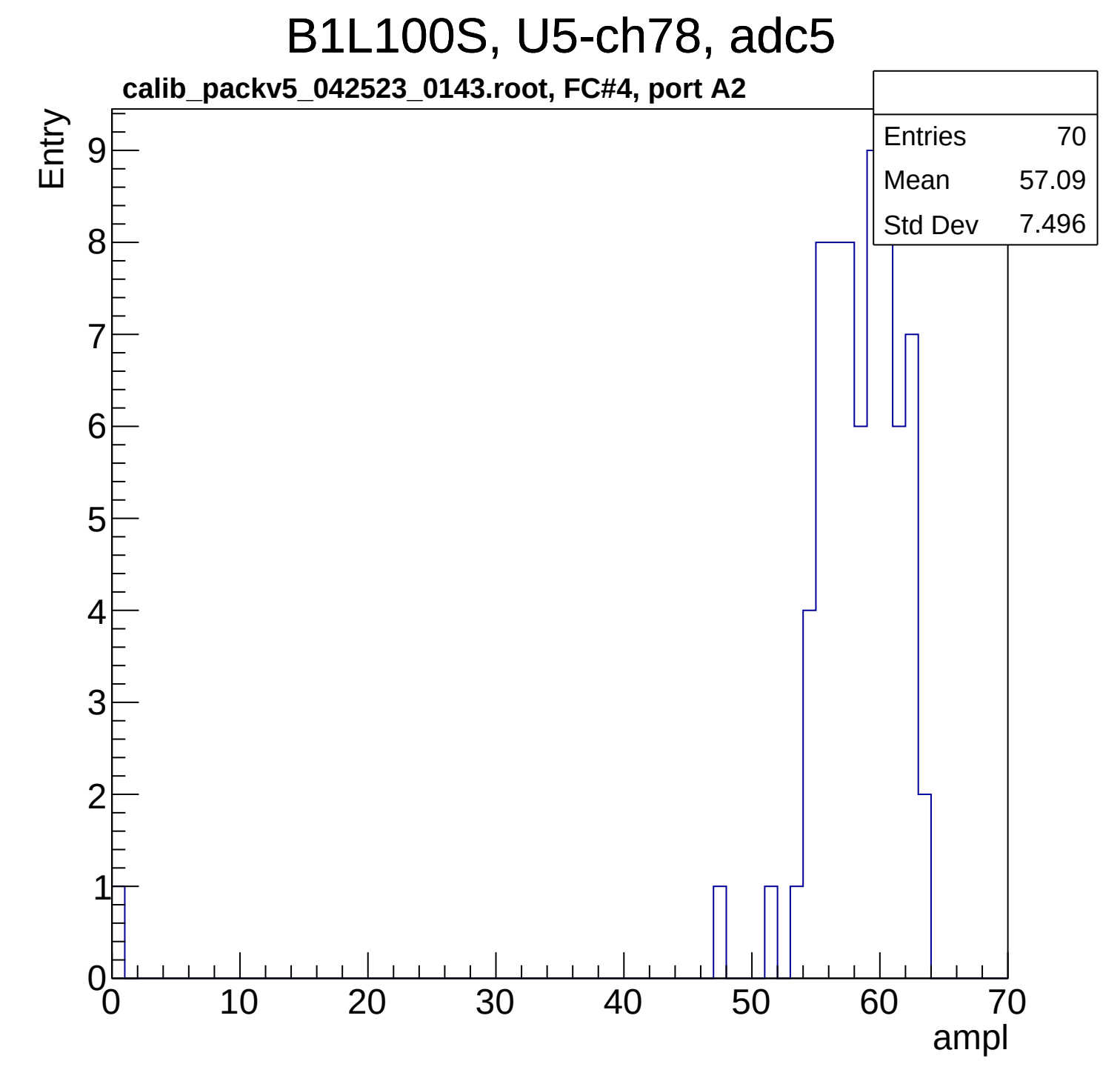
40
50
60
70


B1L100S, U5-ch78, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 57.09
Std Dev 7.496
Entry
ampl
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2
3
4
5
6
7
8
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40
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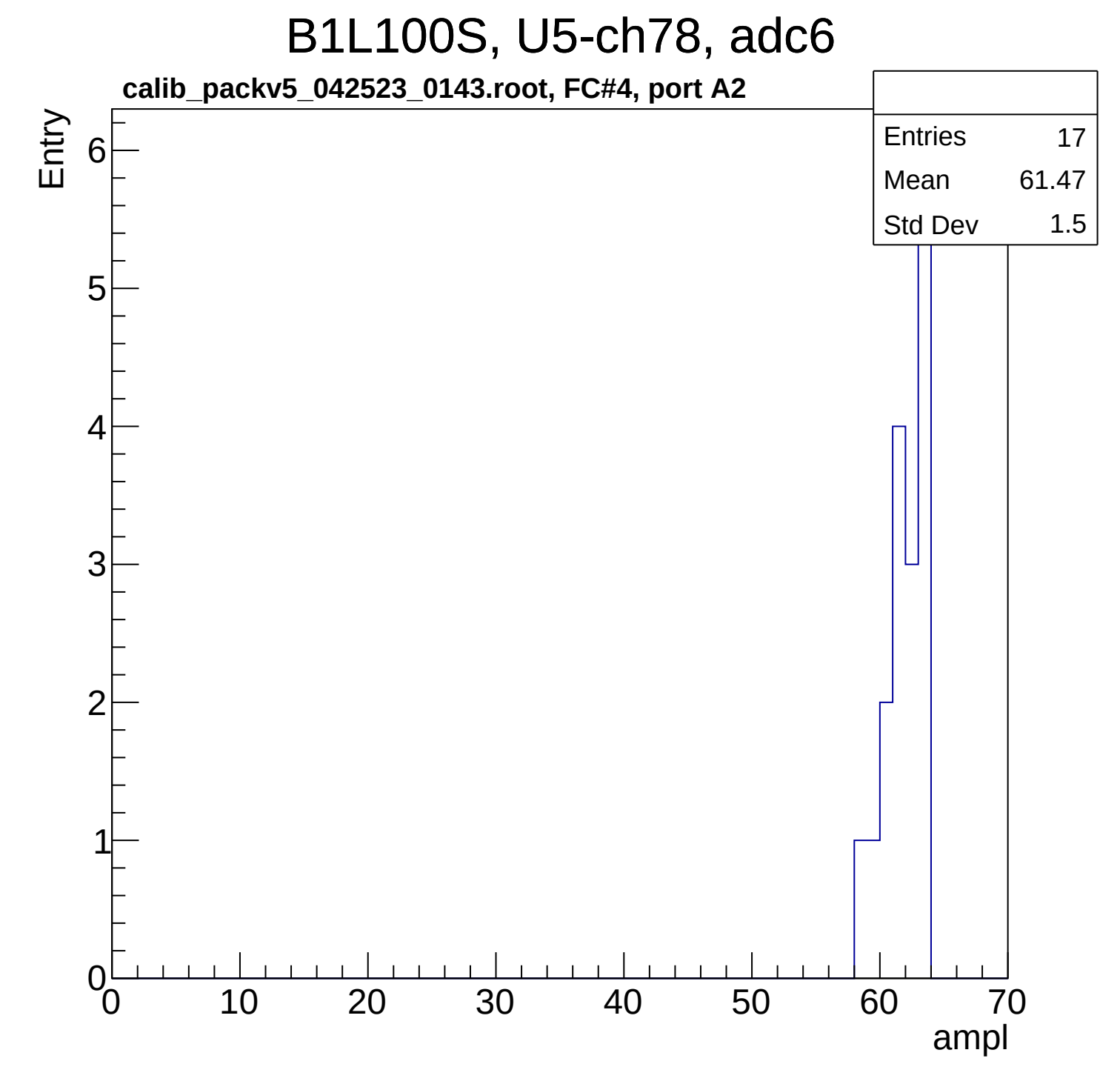
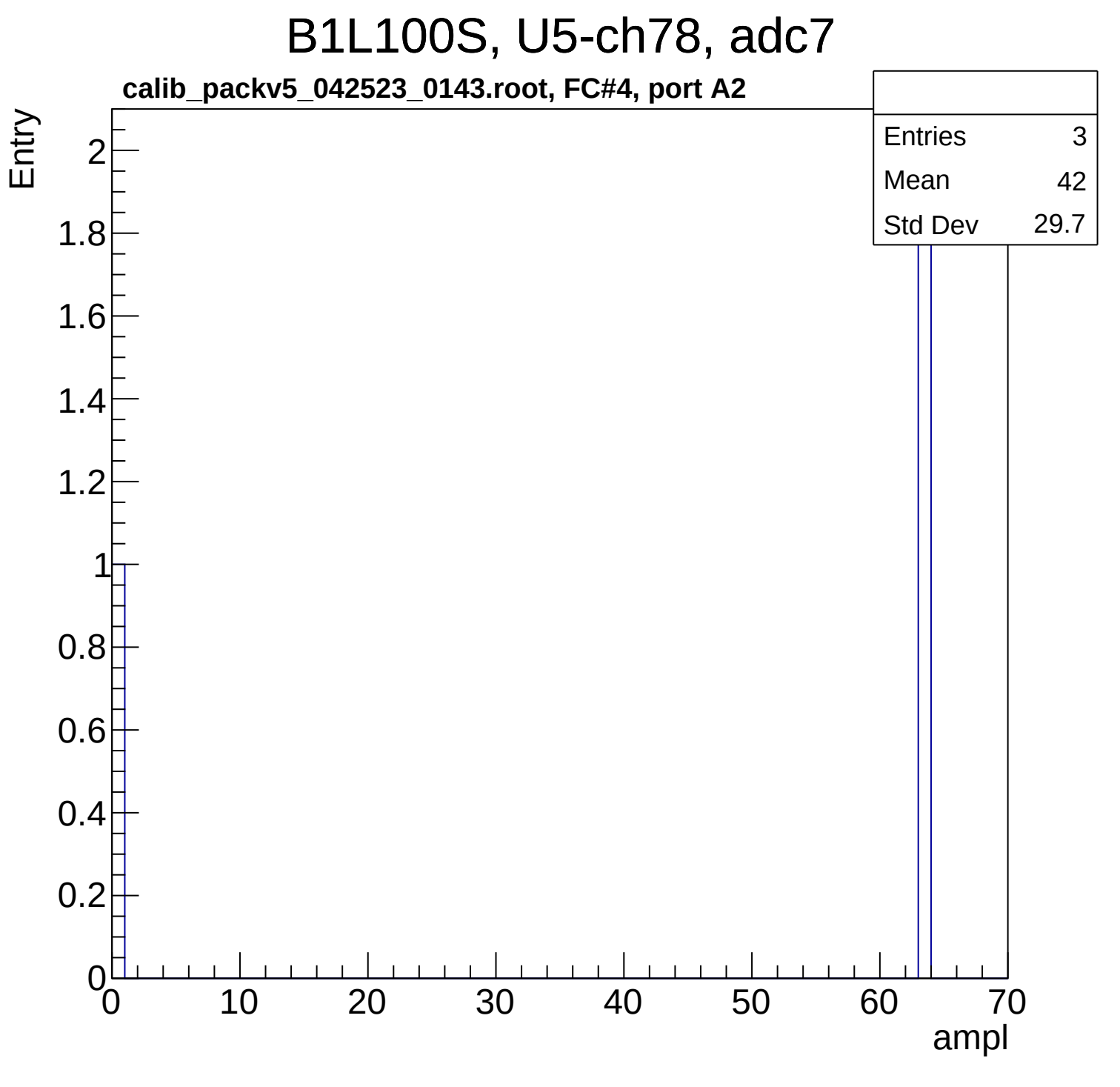
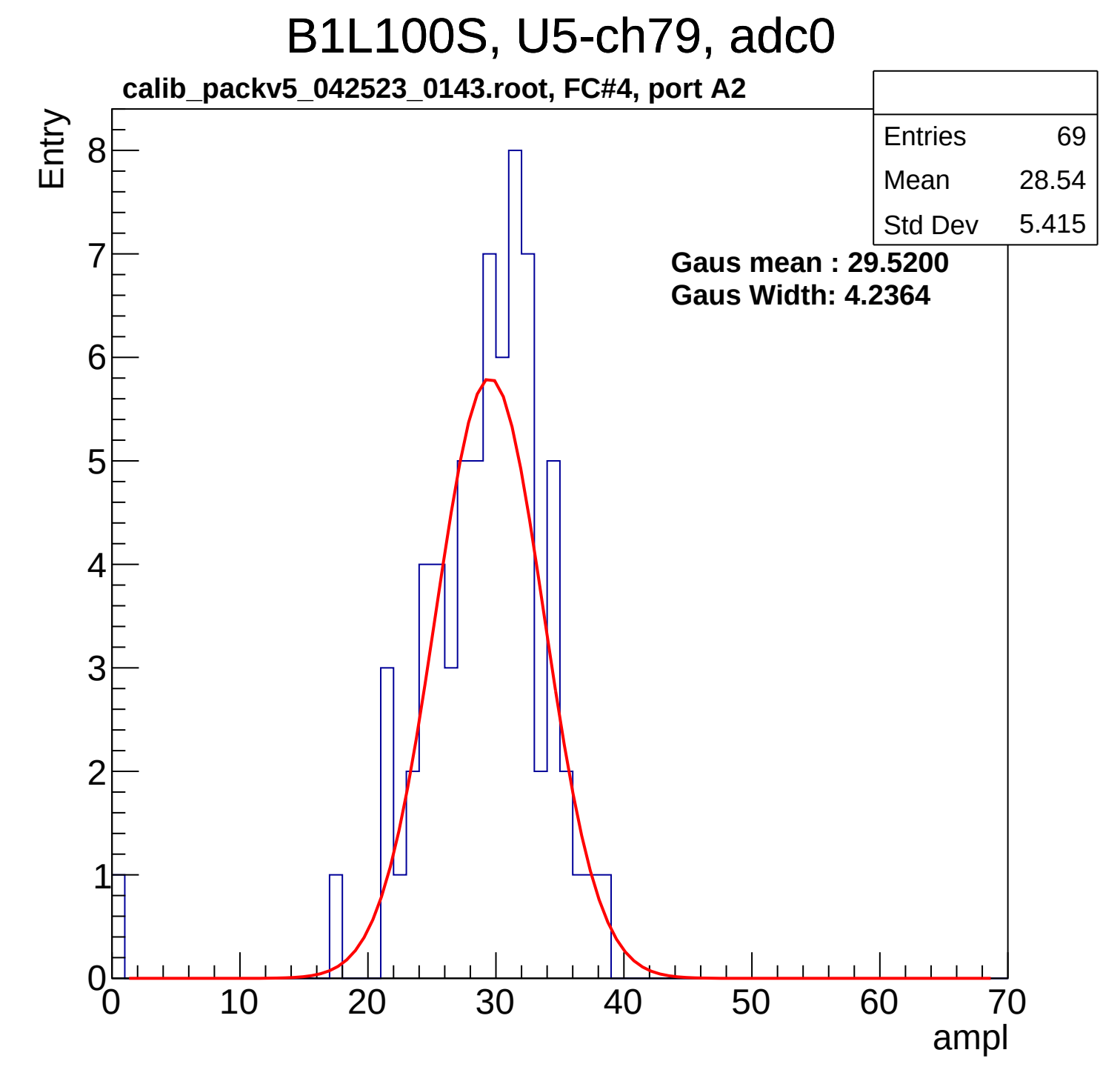

B1L100S, U5-ch78, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 17
Mean 61.47
Std Dev 1.5
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch78, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 42
Std Dev 29.7
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L100S, U5-ch79, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 28.54
Std Dev 5.415
Gaus mean : 29.5200
Gaus Width: 4.2364
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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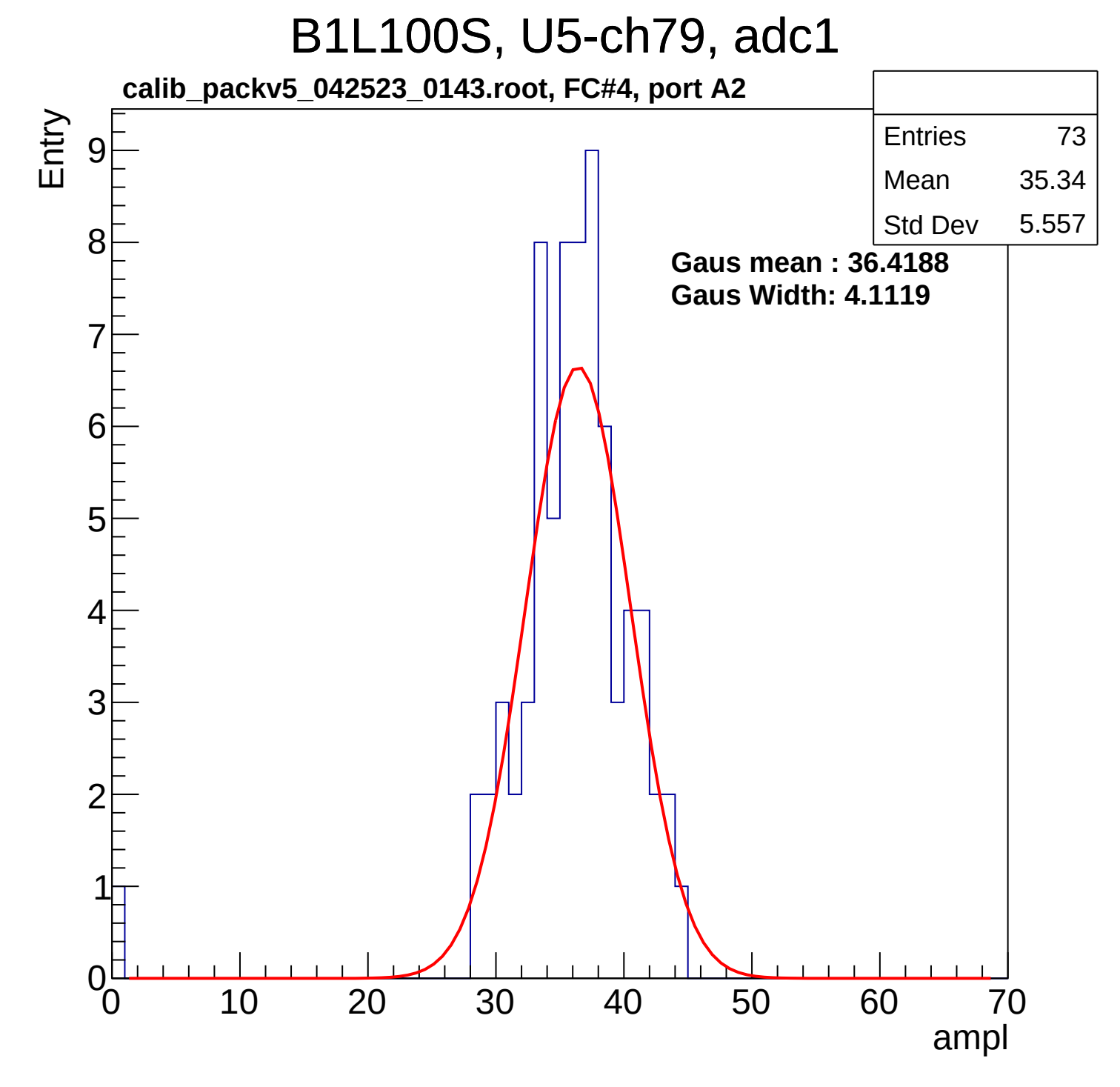
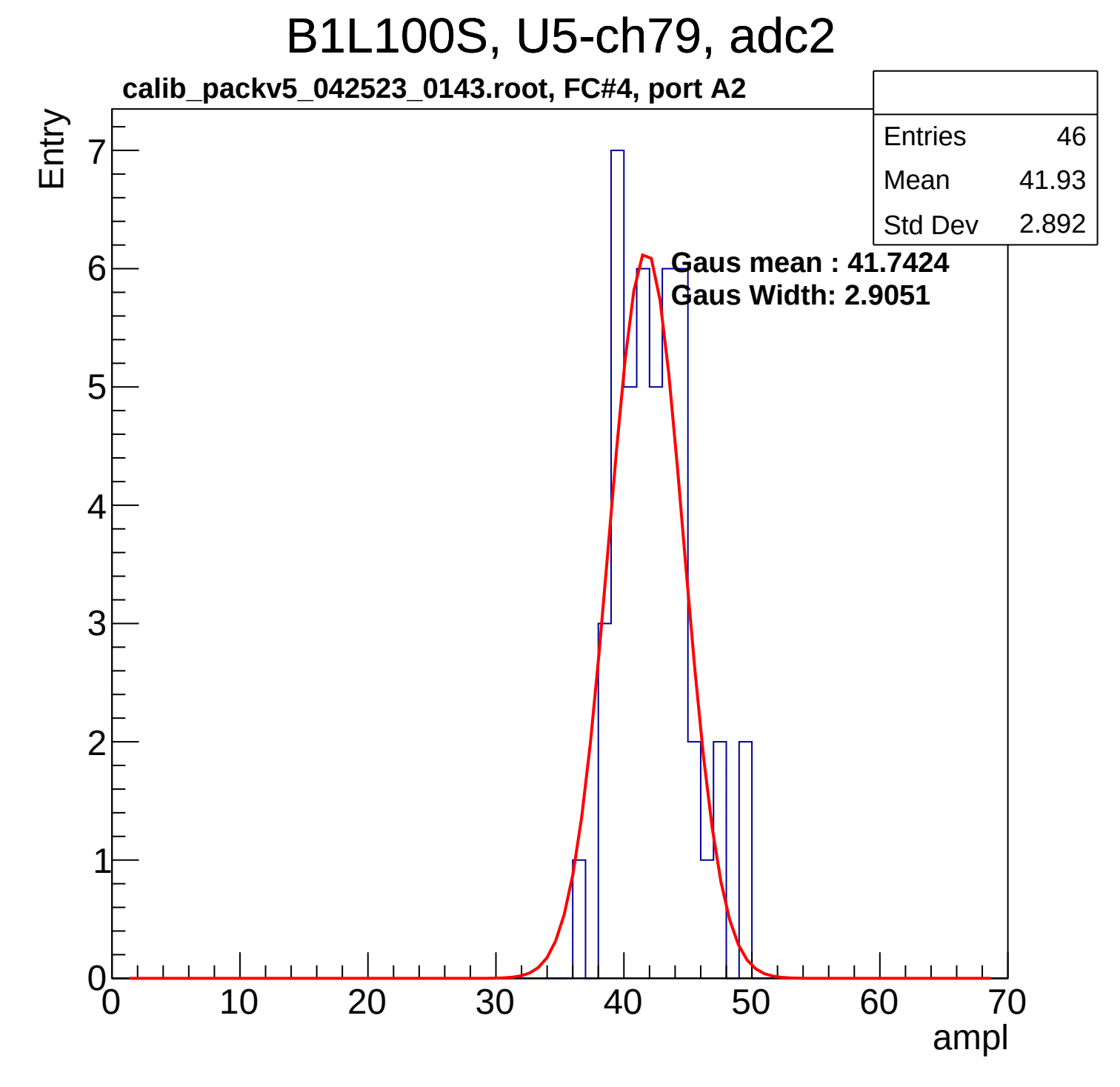
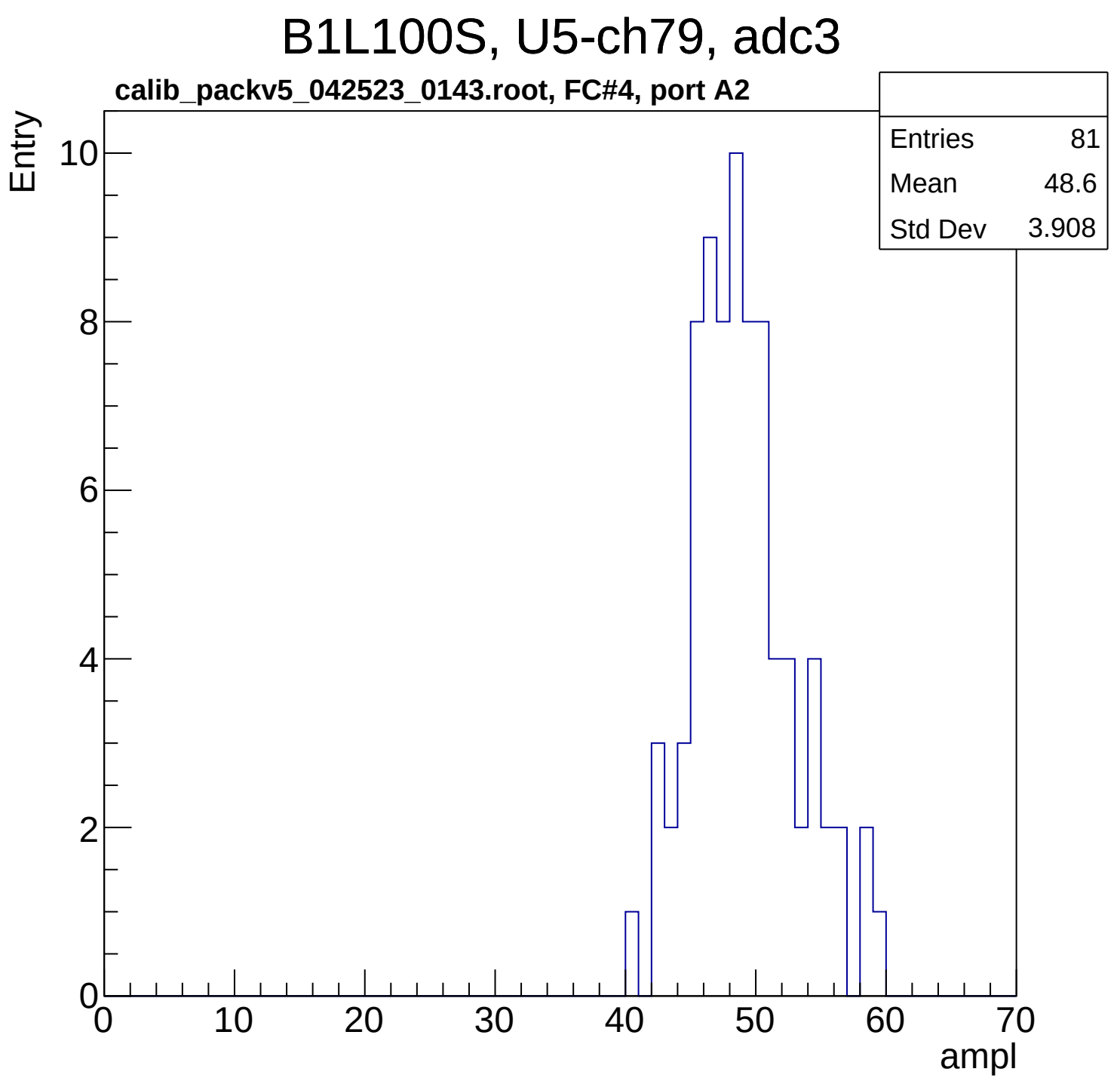
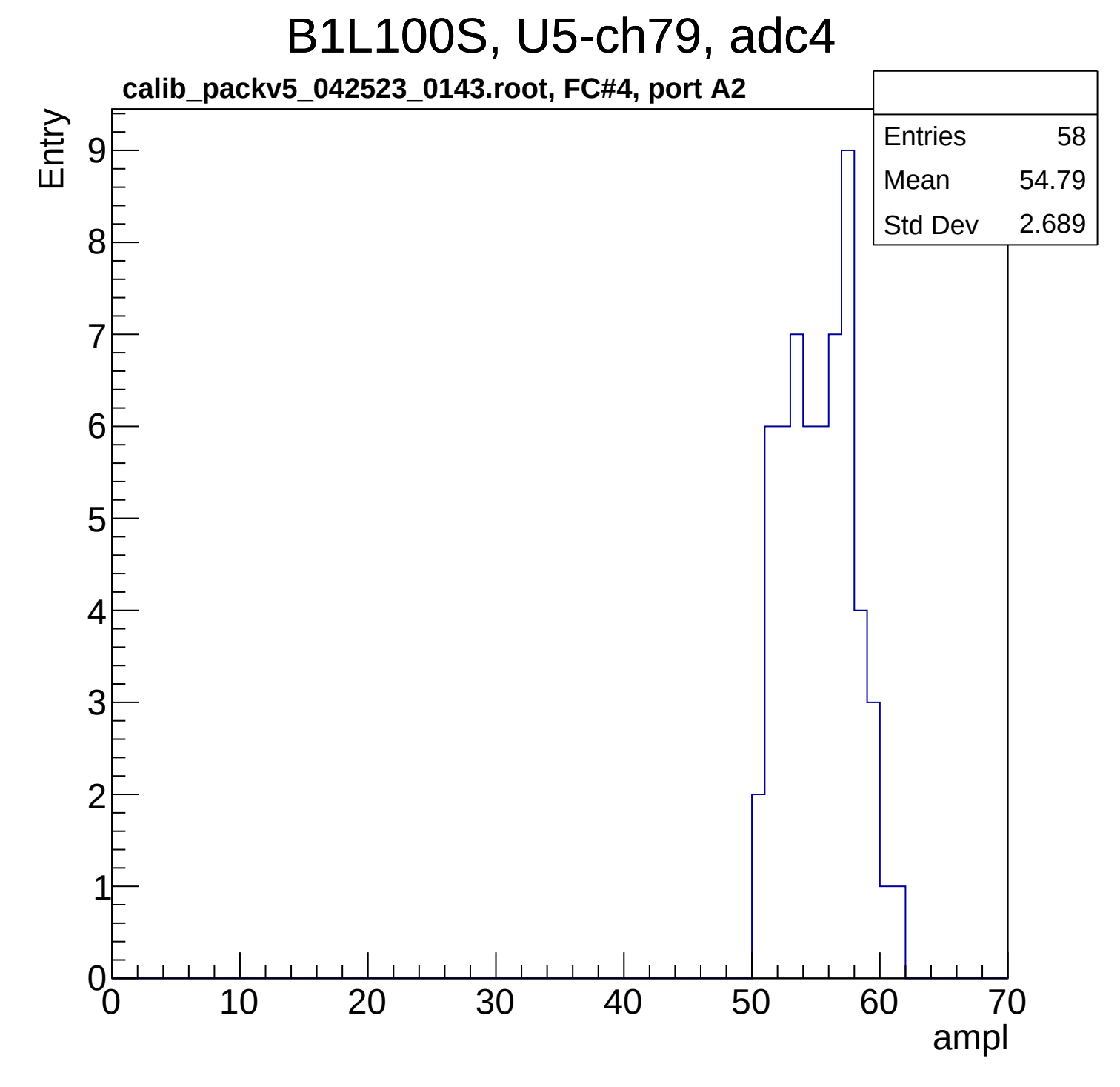
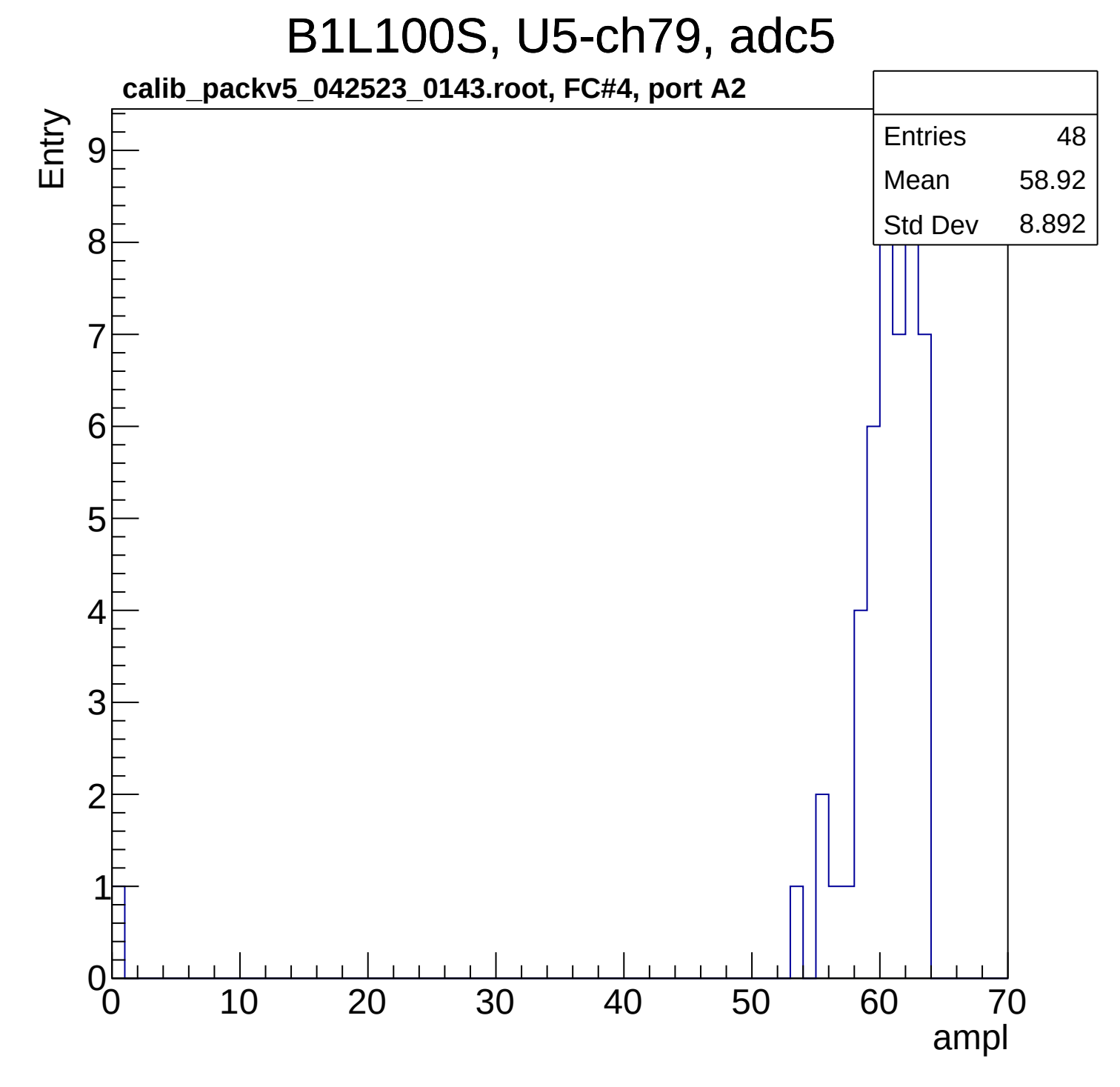

B1L100S, U5-ch79, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 35.34
Std Dev 5.557
Gaus mean : 36.4188
Gaus Width: 4.1119
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch79, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 46
Mean 41.93
Std Dev 2.892
Gaus mean : 41.7424
Gaus Width: 2.9051
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U5-ch79, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 81
Mean 48.6
Std Dev 3.908
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch79, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 54.79
Std Dev 2.689
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch79, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 48
Mean 58.92
Std Dev 8.892
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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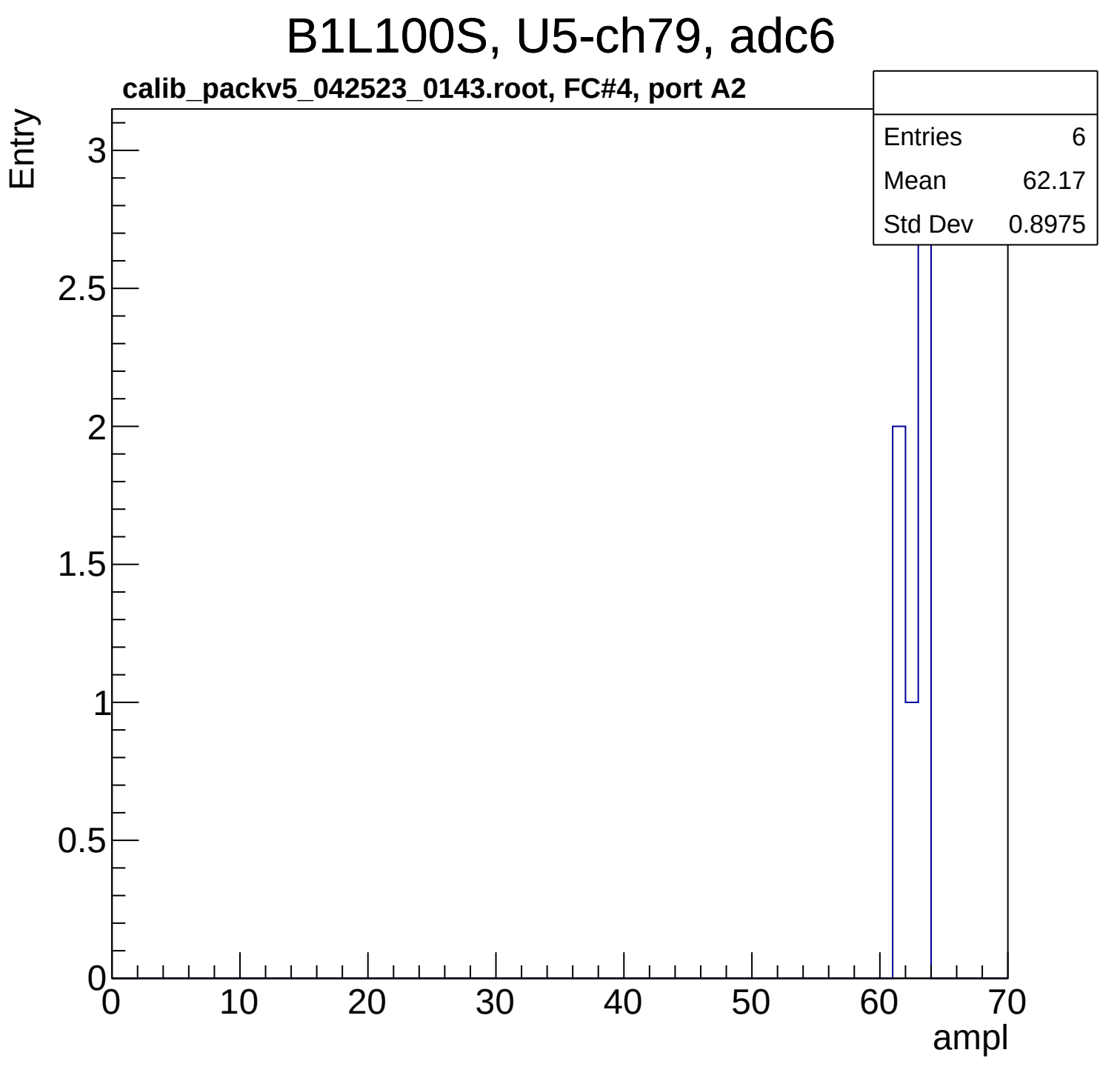
B1L100S, U5-ch79, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 6
Mean 62.17
Std Dev 0.8975
Entry
ampl
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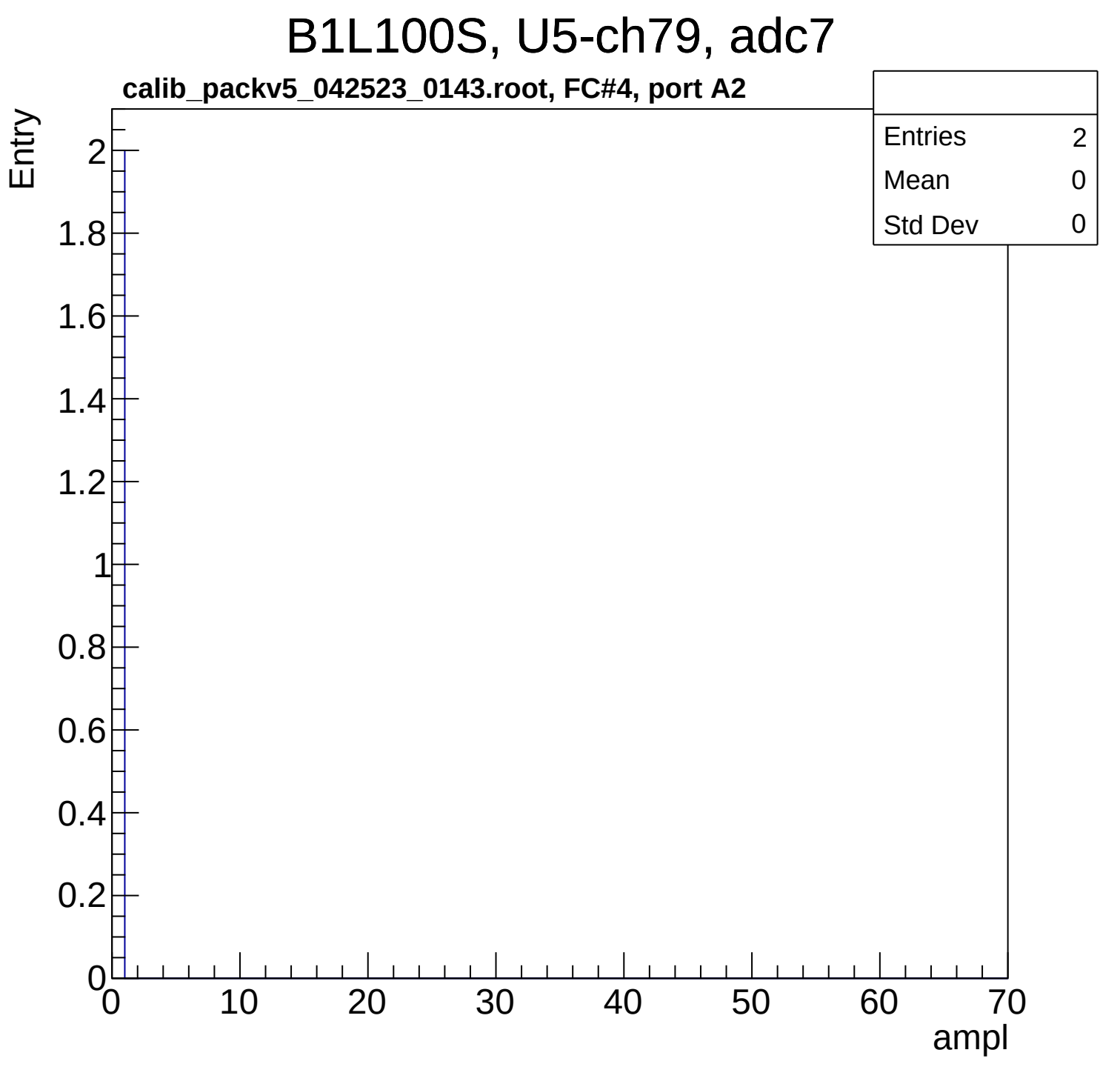
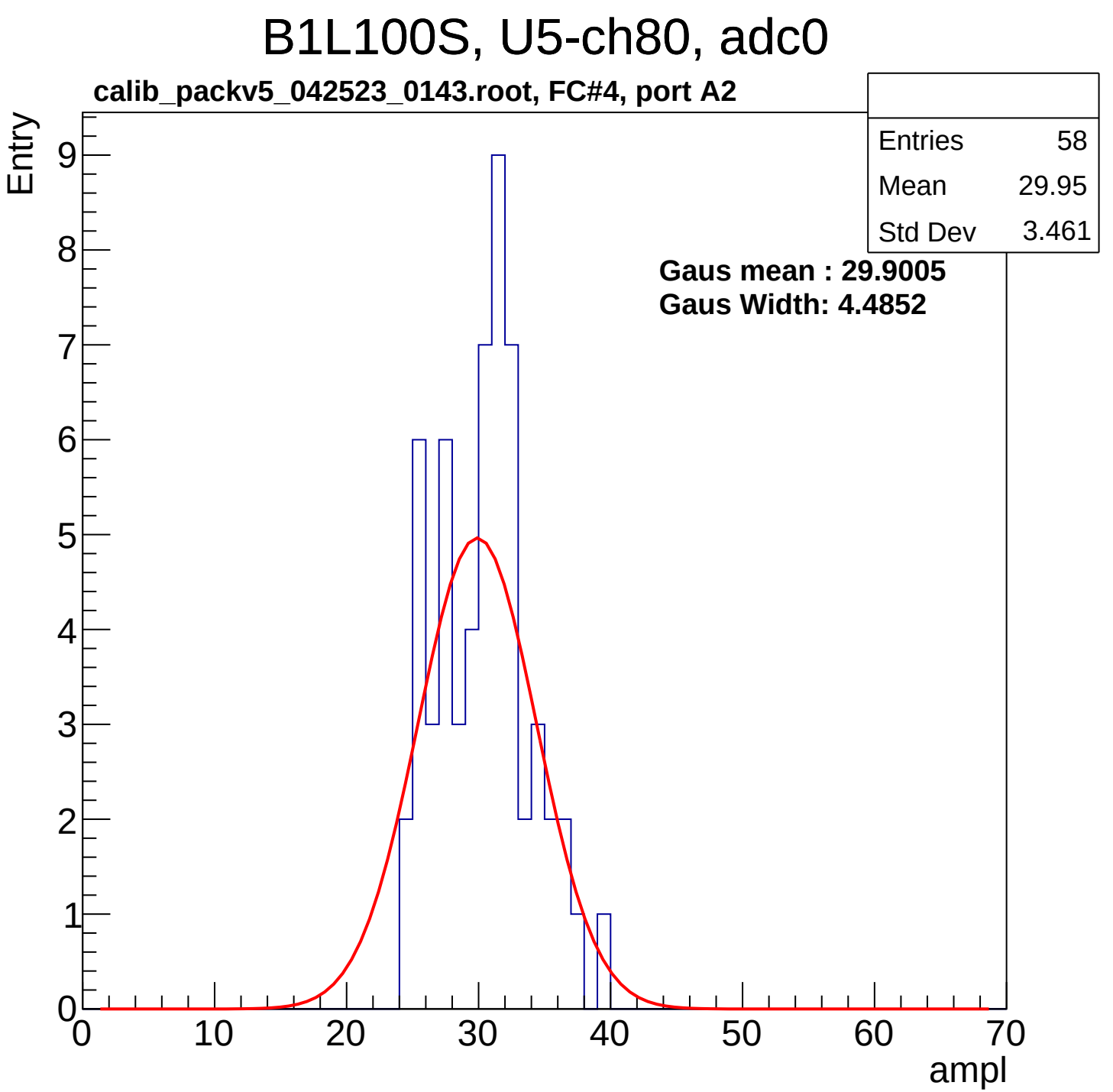
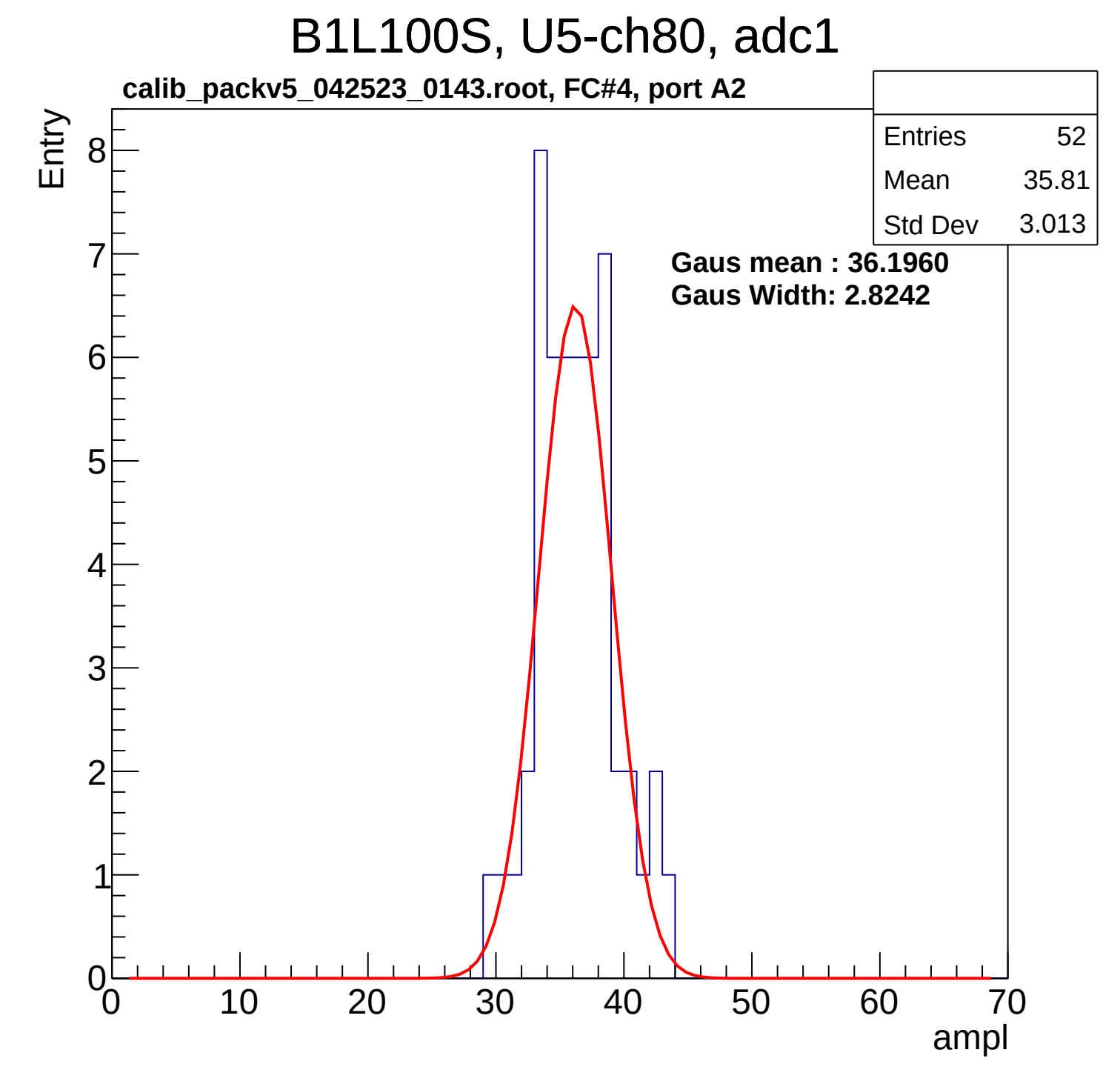
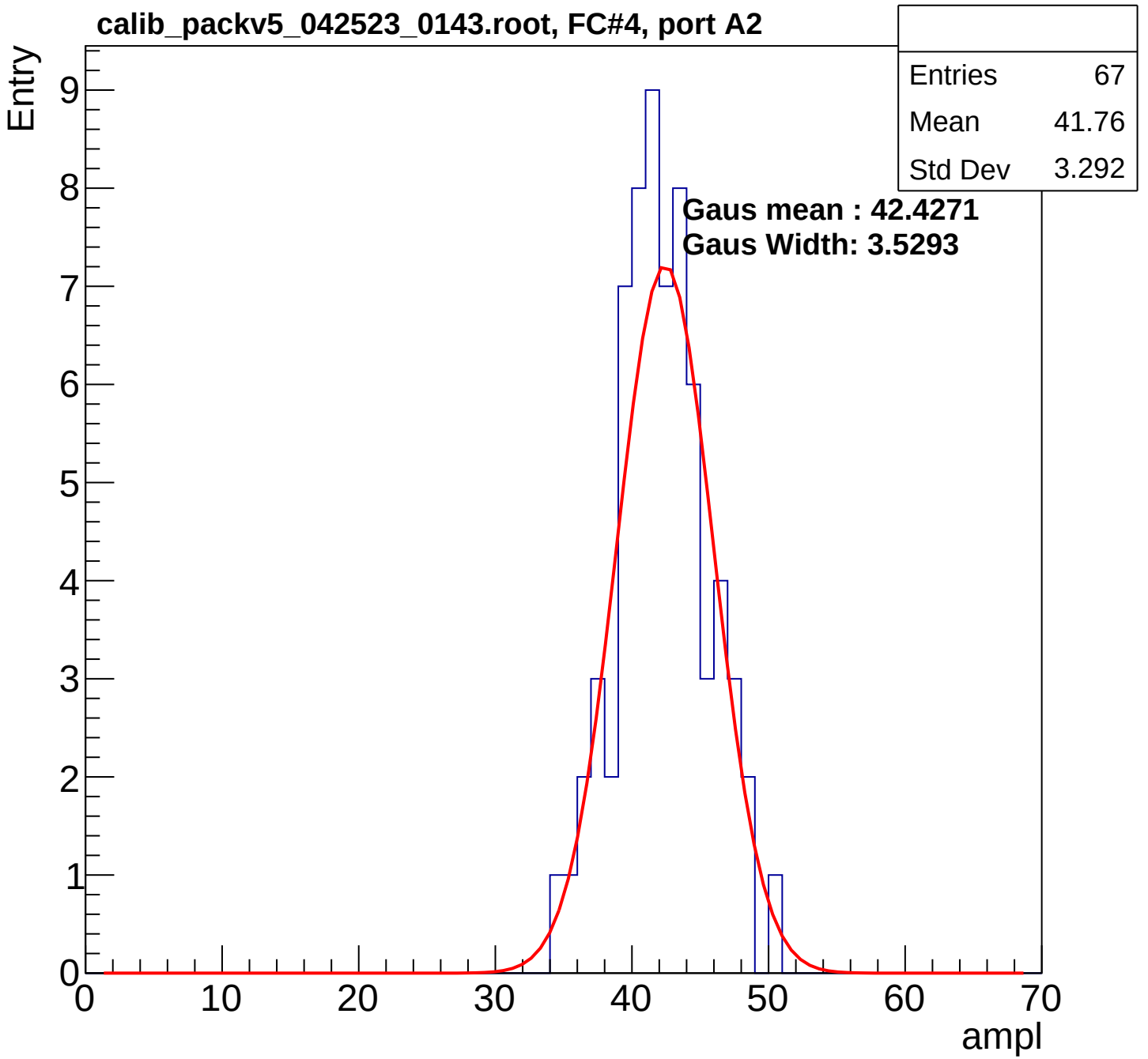
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L100S, U5-ch79, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch80, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 29.95
Std Dev 3.461
Gaus mean : 29.9005
Gaus Width: 4.4852
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch80, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 52
Mean 35.81
Std Dev 3.013
Gaus mean : 36.1960
Gaus Width: 2.8242
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch80, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 41.76
Std Dev 3.292
Gaus mean : 42.4271
Gaus Width: 3.5293
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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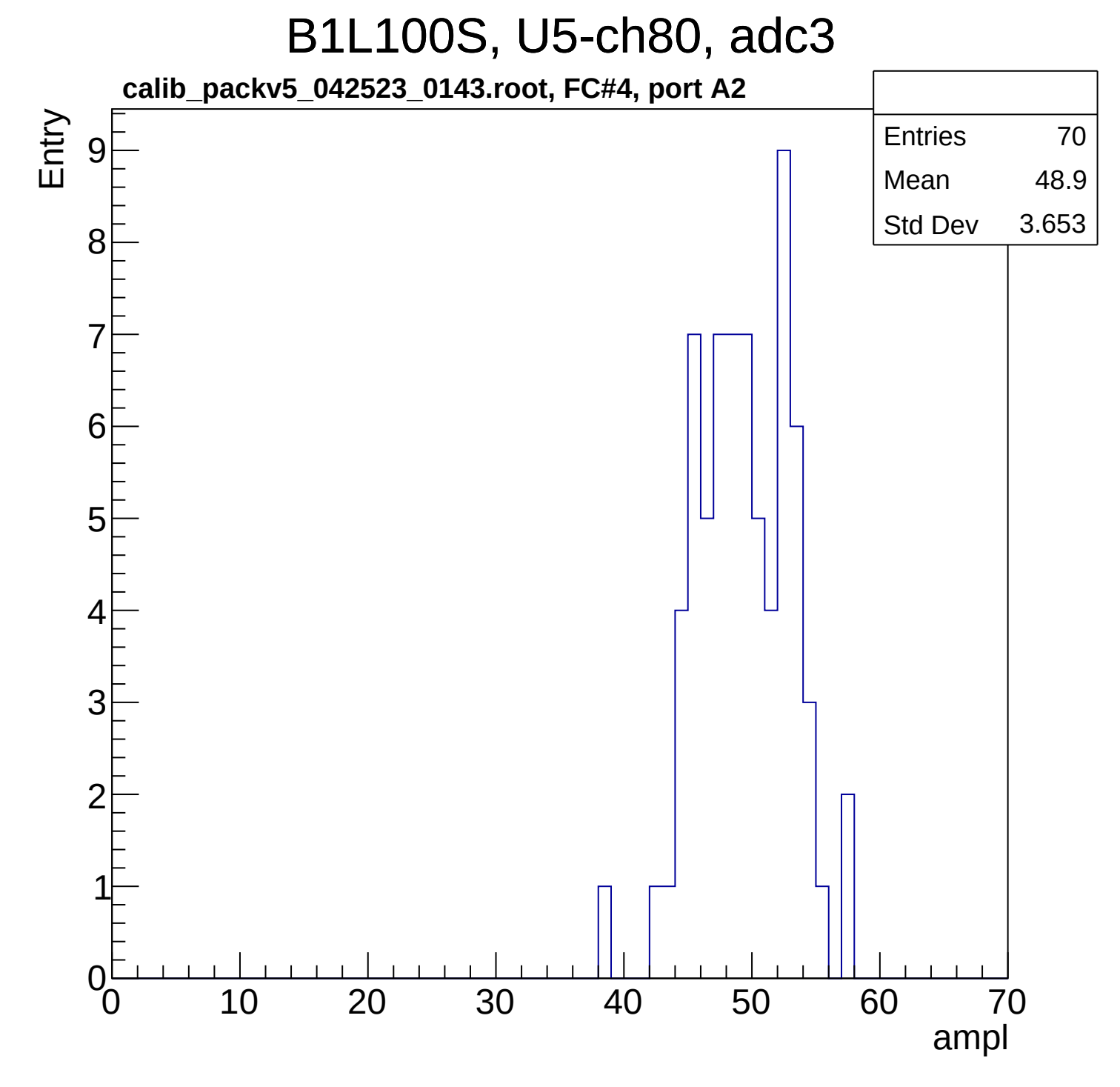
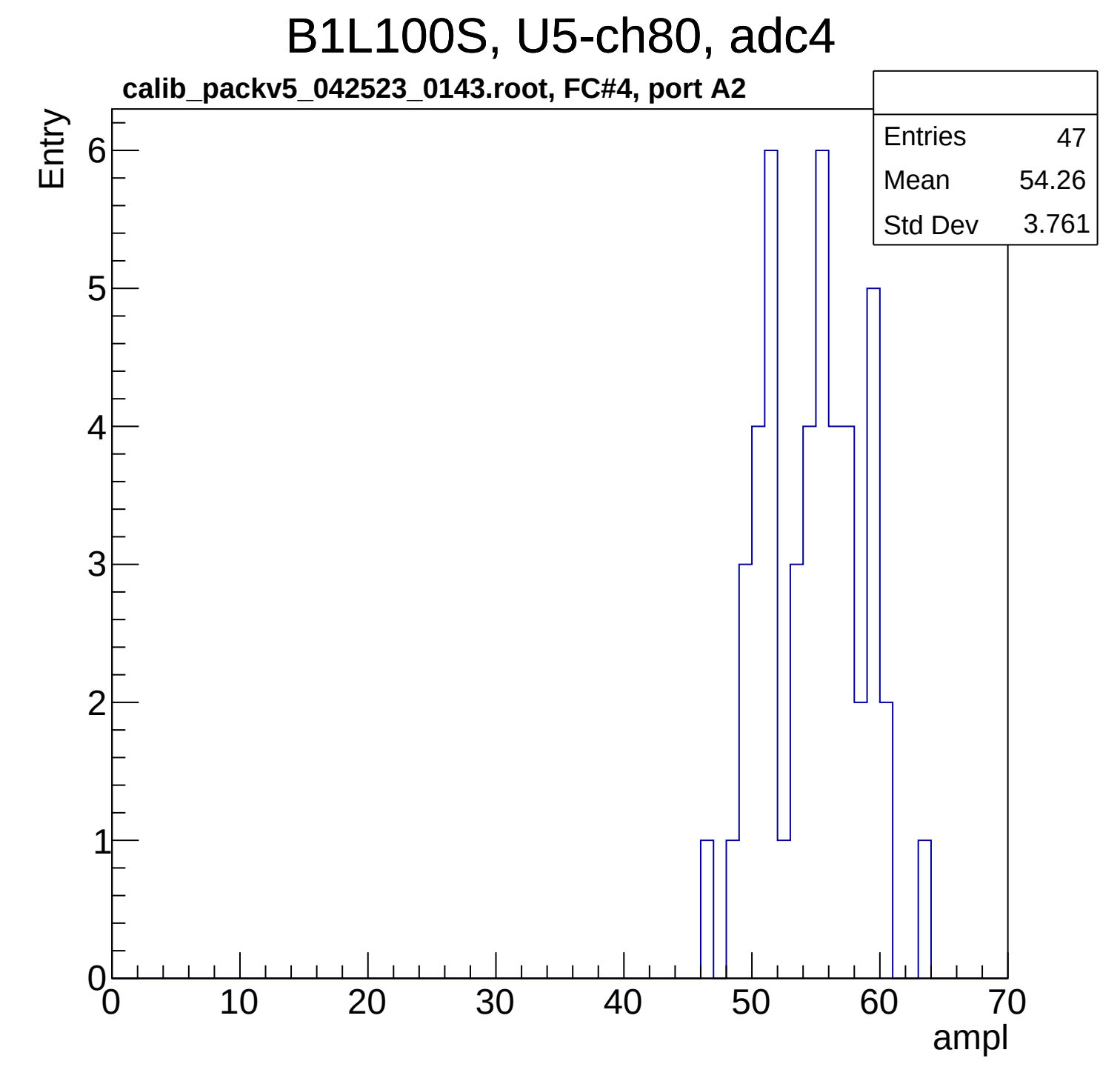
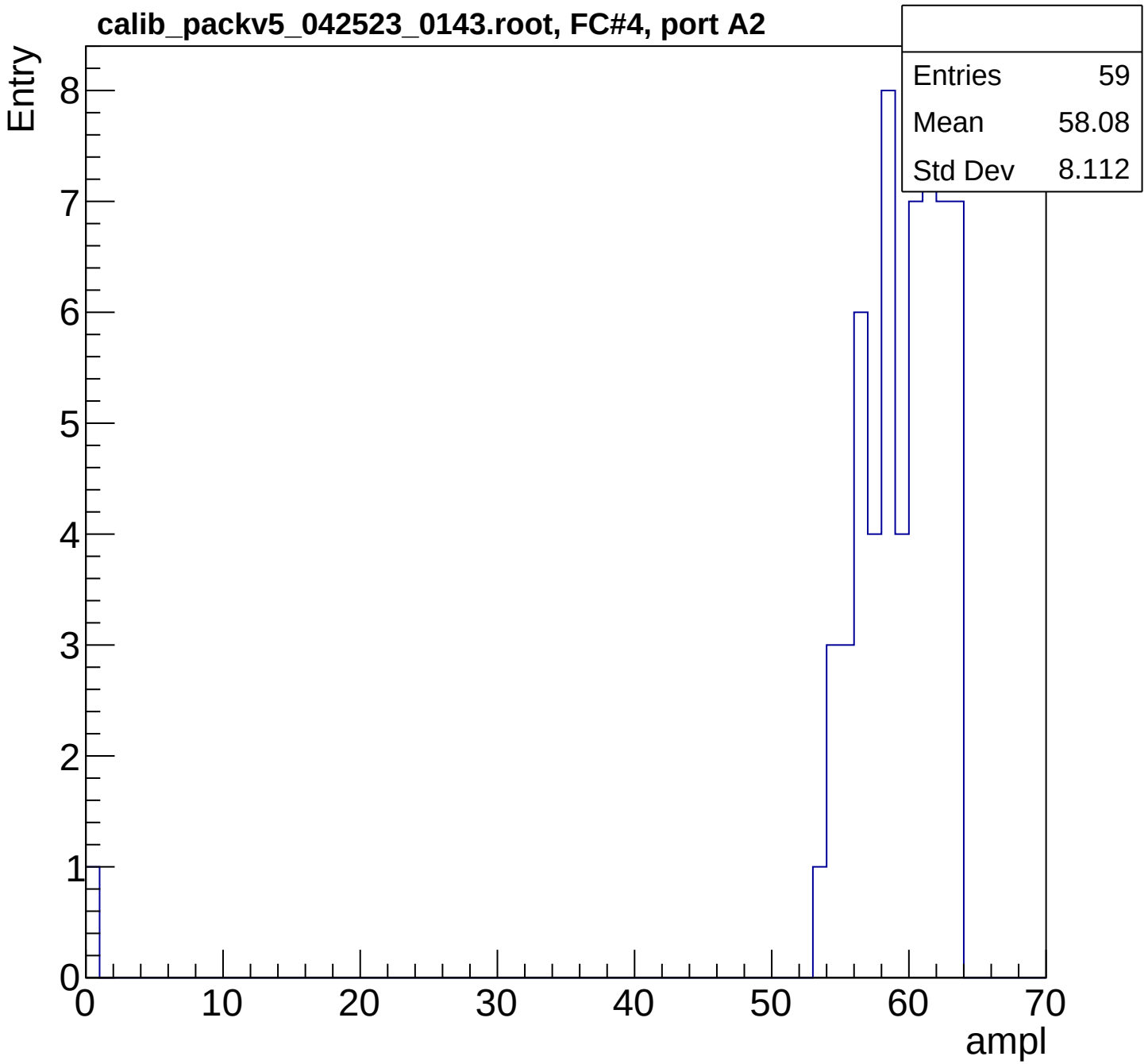
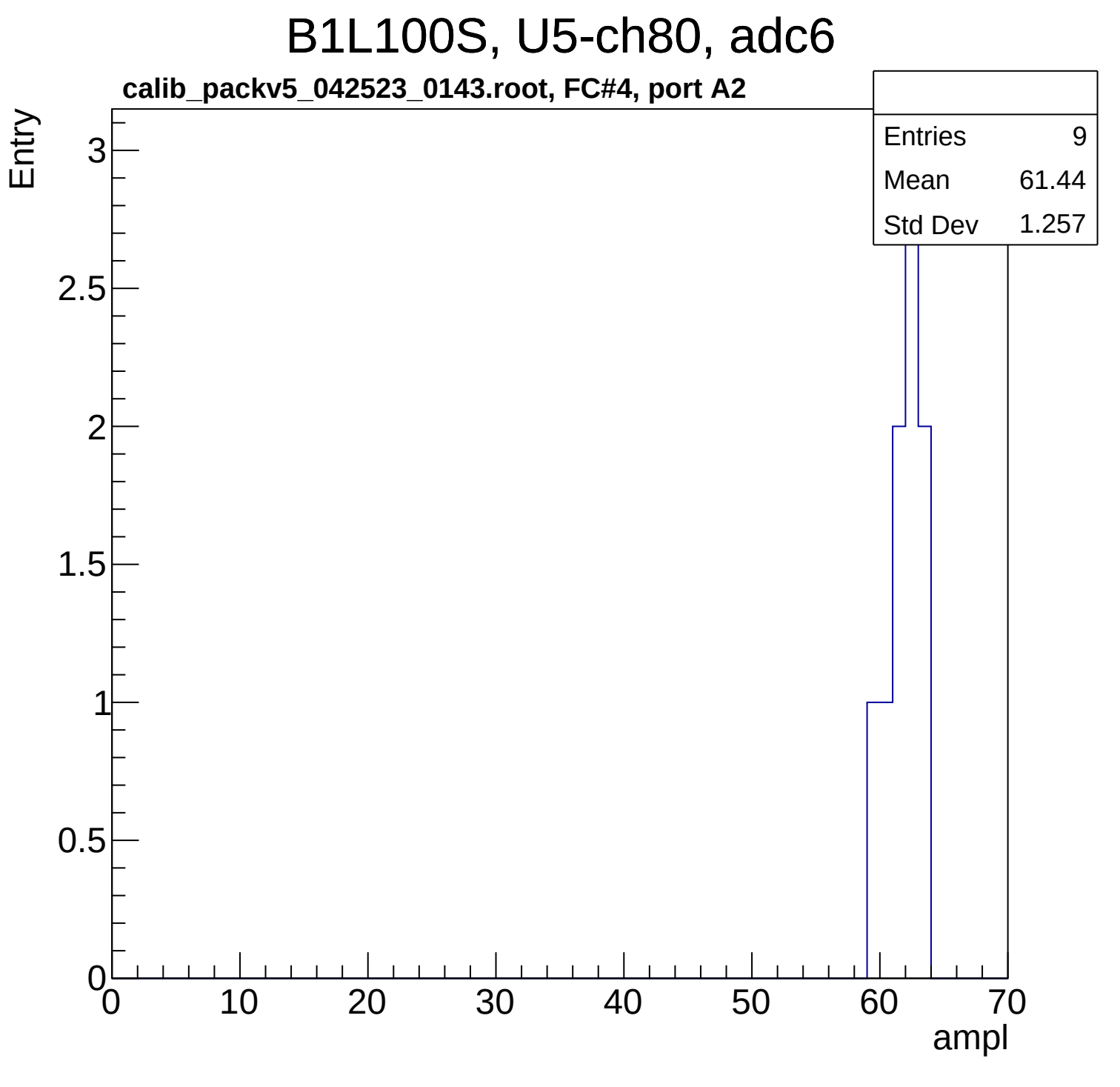
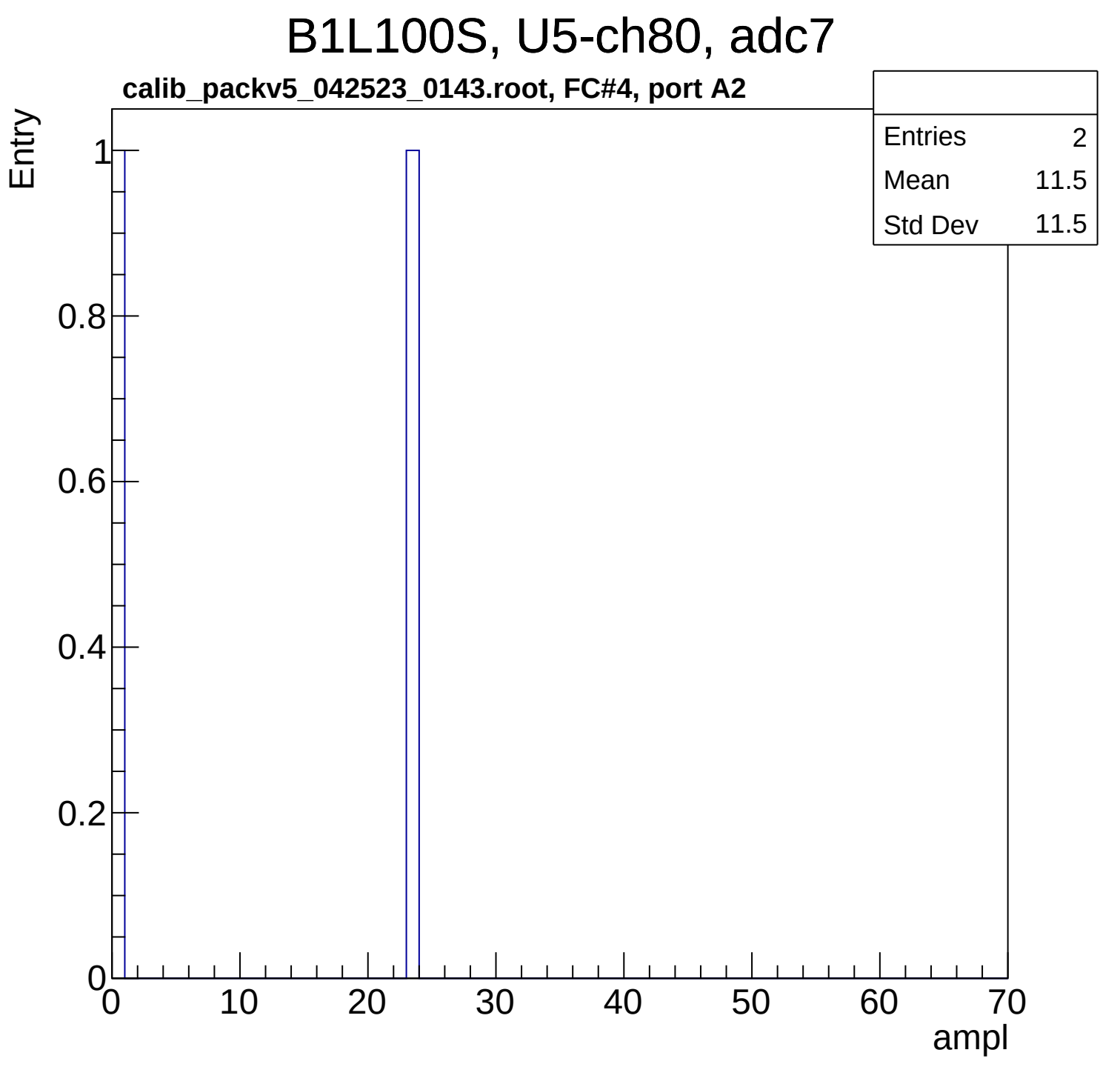
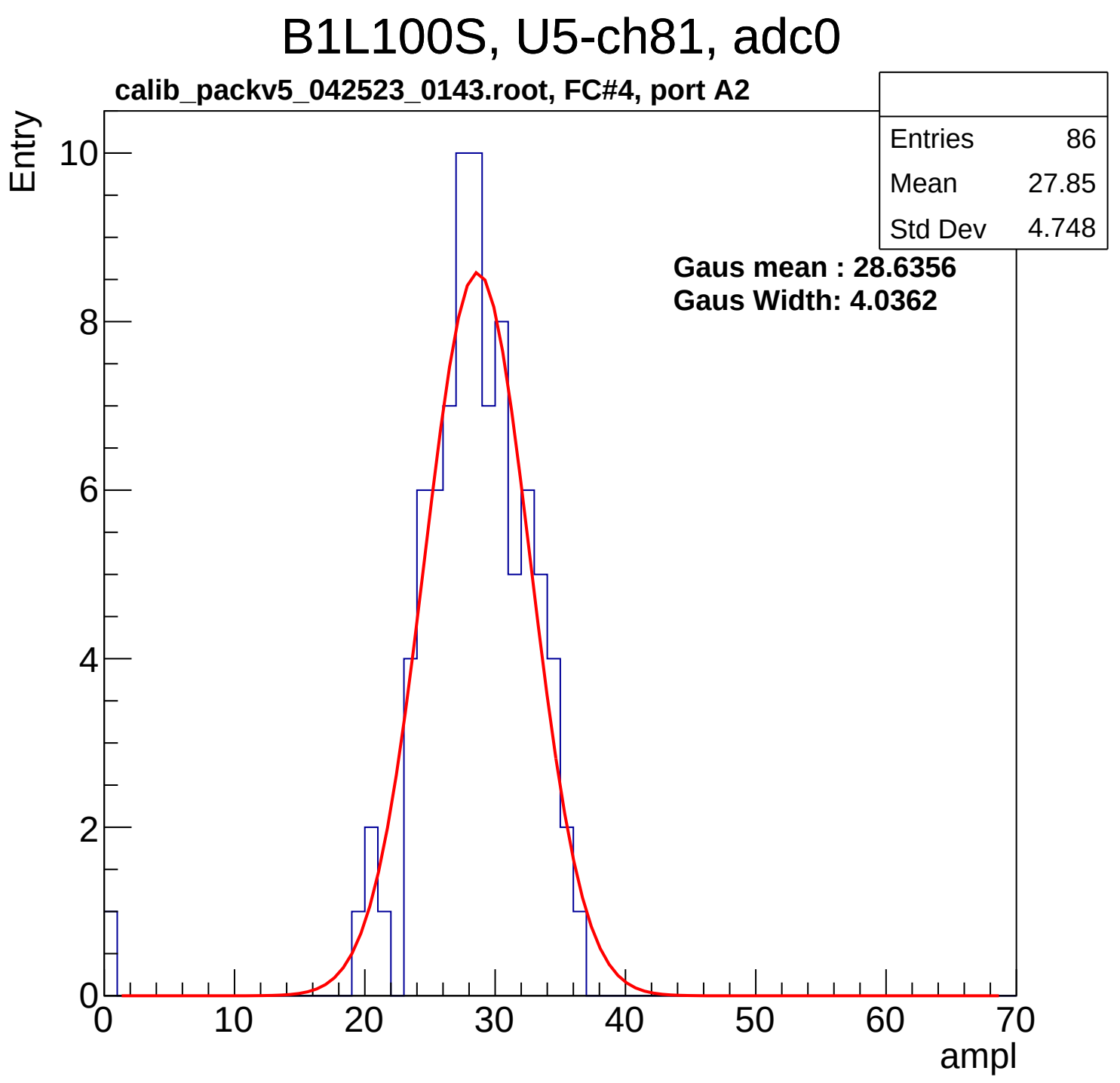

B1L100S, U5-ch80, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 48.9
Std Dev 3.653
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

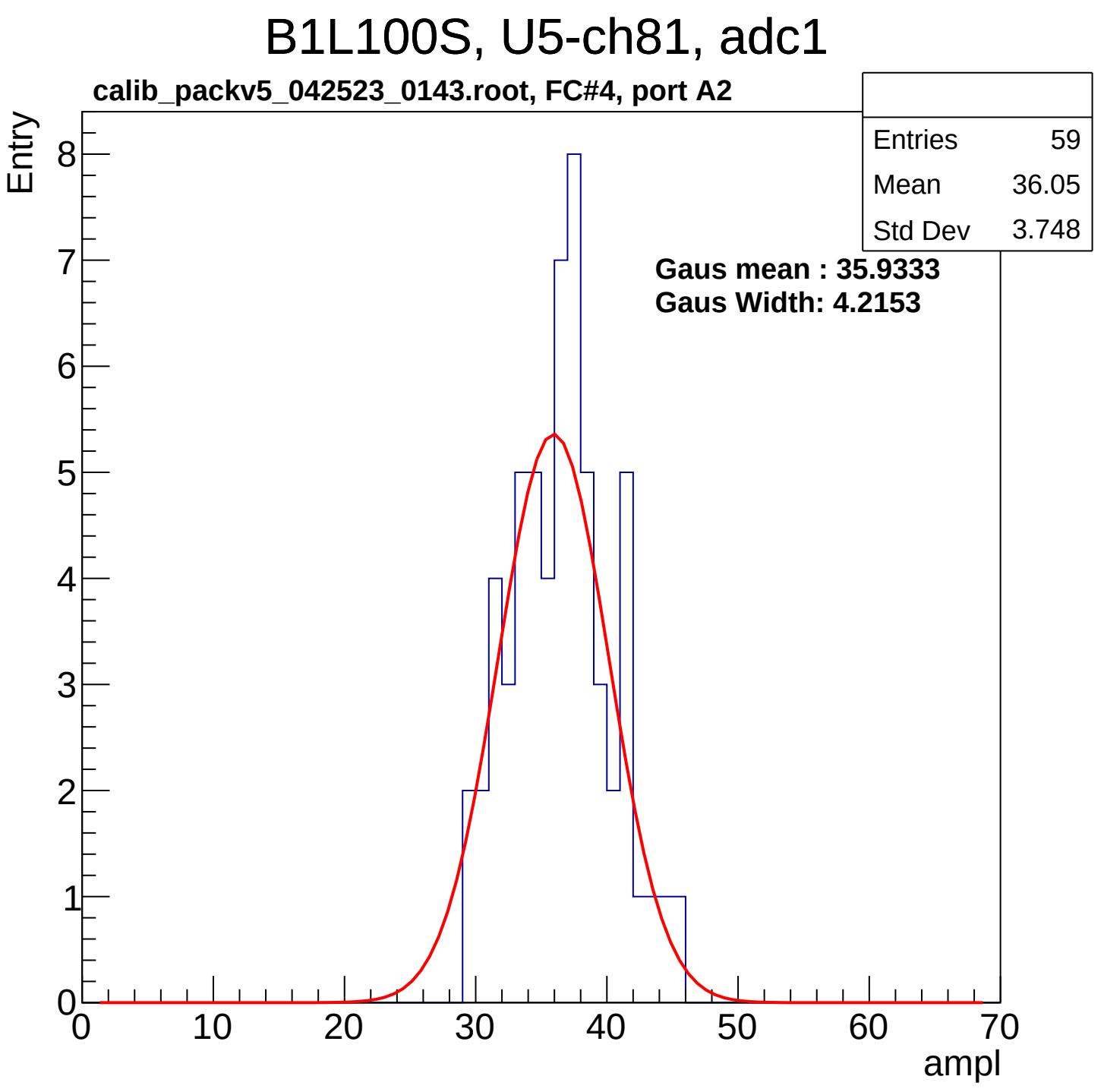

B1L100S, U5-ch80, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 47
Mean 54.26
Std Dev 3.761
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

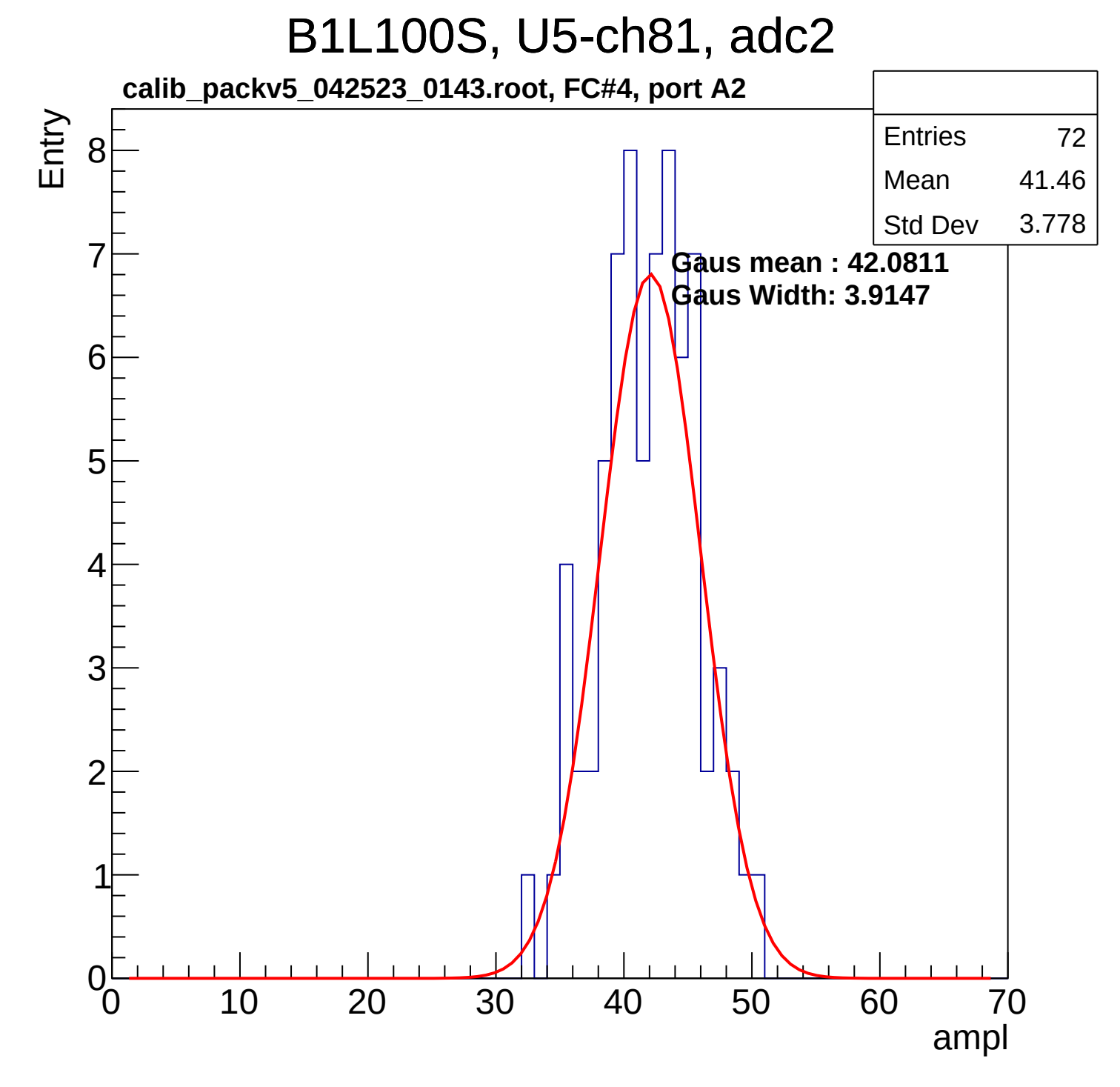

B1L100S, U5-ch80, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 58.08
Std Dev 8.112
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

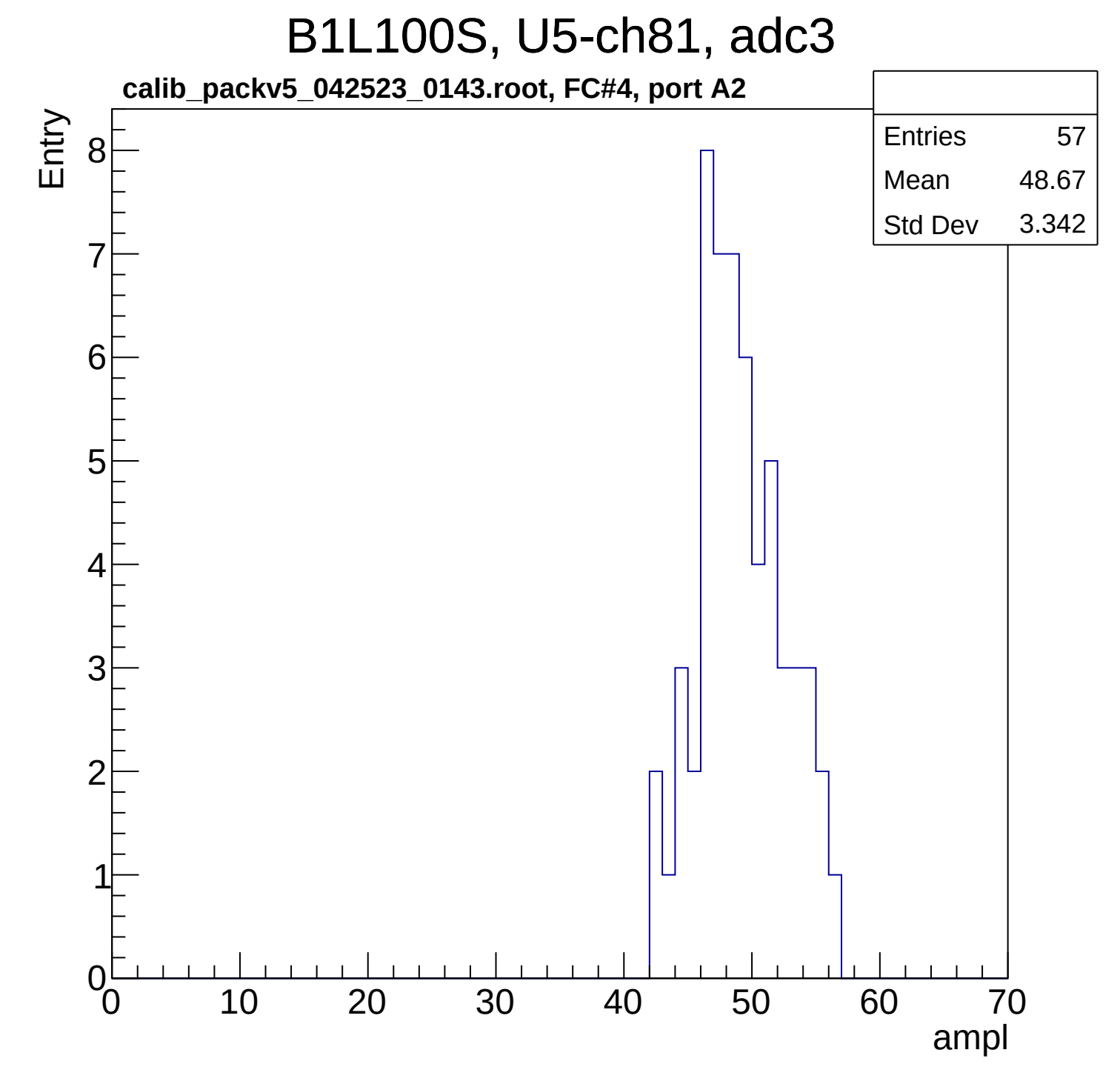

B1L100S, U5-ch80, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 9
Mean 61.44
Std Dev 1.257
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L100S, U5-ch80, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 11.5
Std Dev 11.5
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B1L100S, U5-ch81, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 86
Mean 27.85
Std Dev 4.748
Gaus mean : 28.6356
Gaus Width: 4.0362
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch81, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 36.05
Std Dev 3.748
Gaus mean : 35.9333
Gaus Width: 4.2153
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch81, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 41.46
Std Dev 3.778
Gaus mean : 42.0811
Gaus Width: 3.9147
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch81, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 48.67
Std Dev 3.342
Entry
ampl
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1
2
3
4
5
6
7
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0
10
20
30
40
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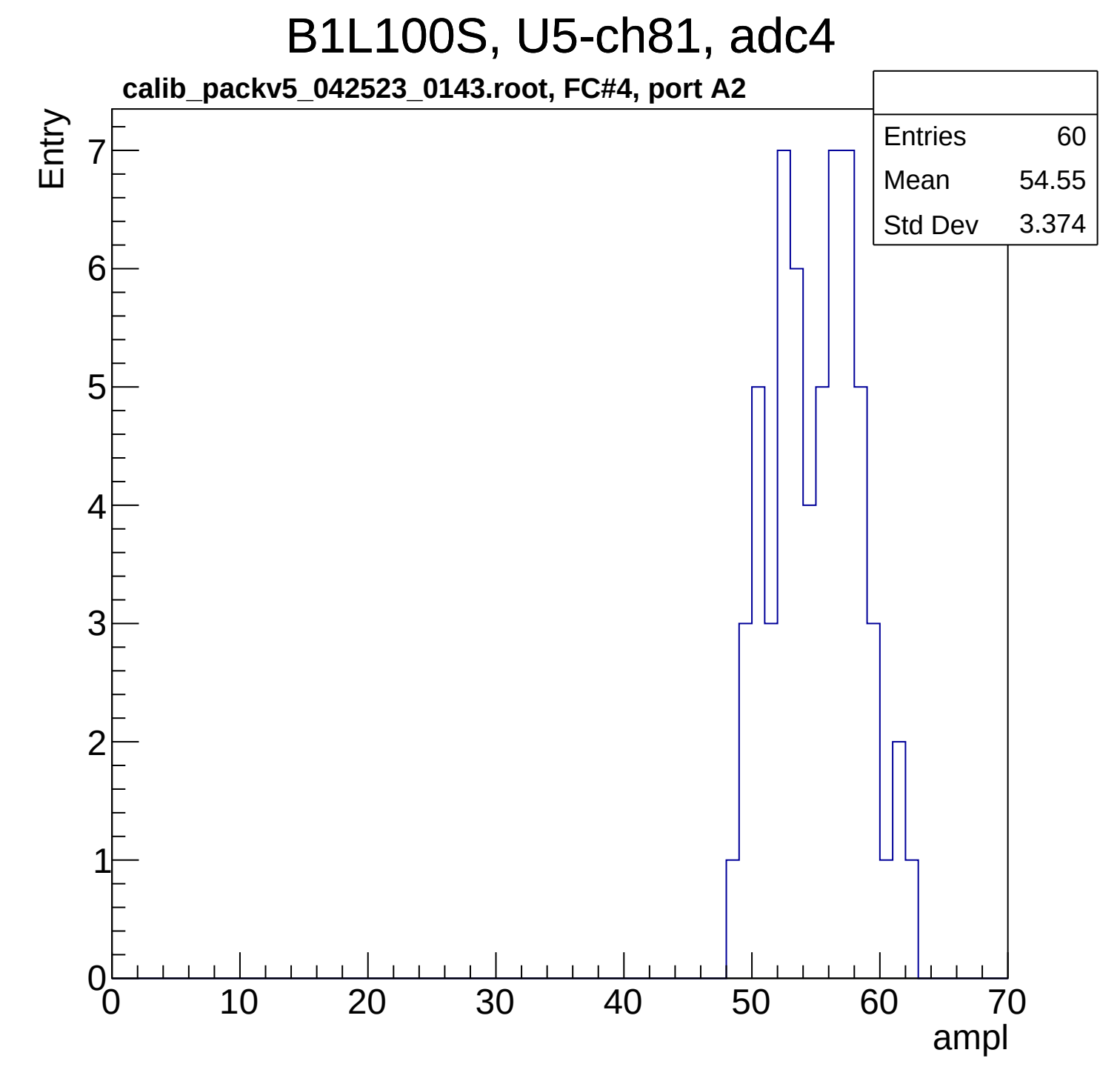
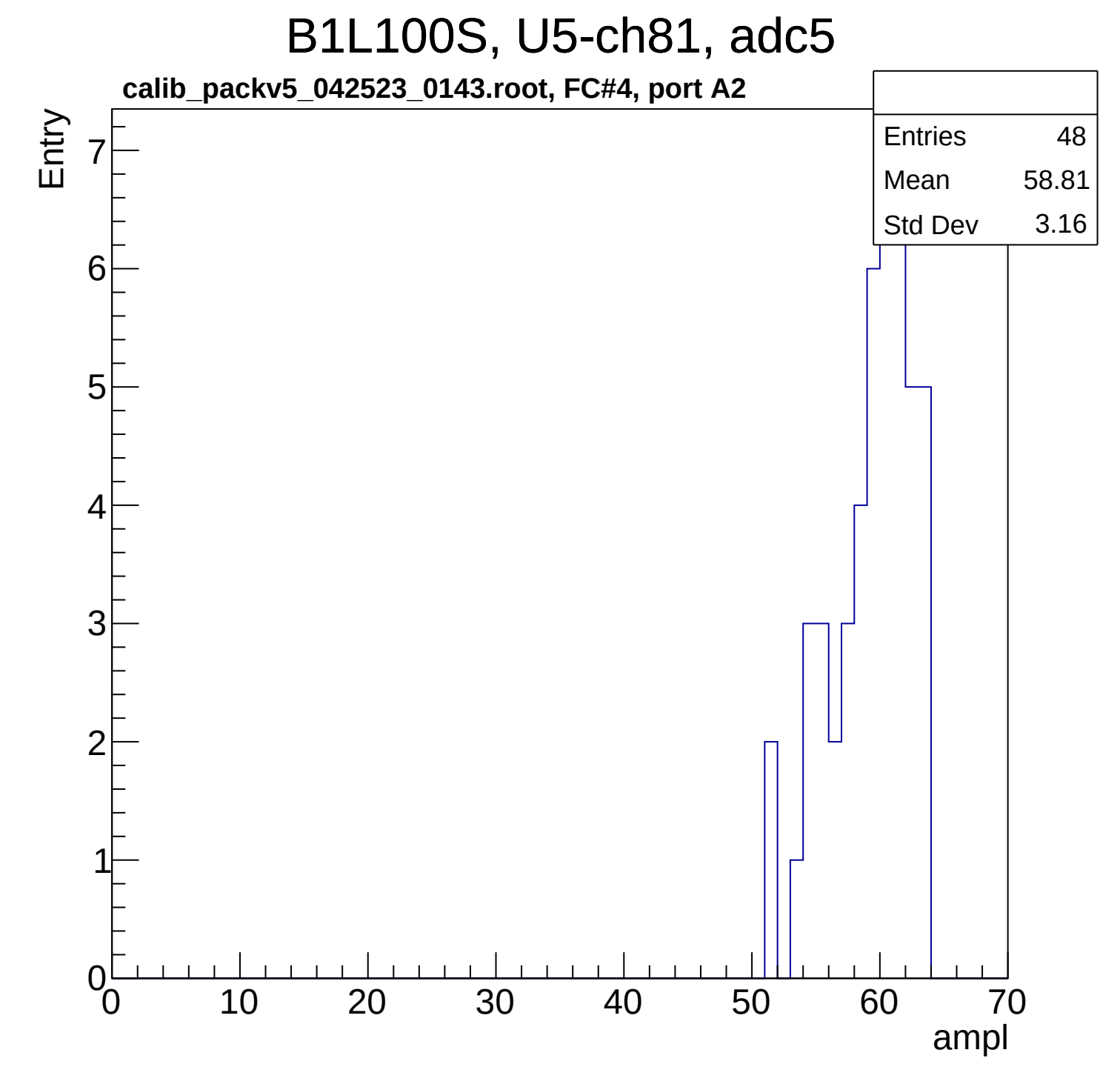
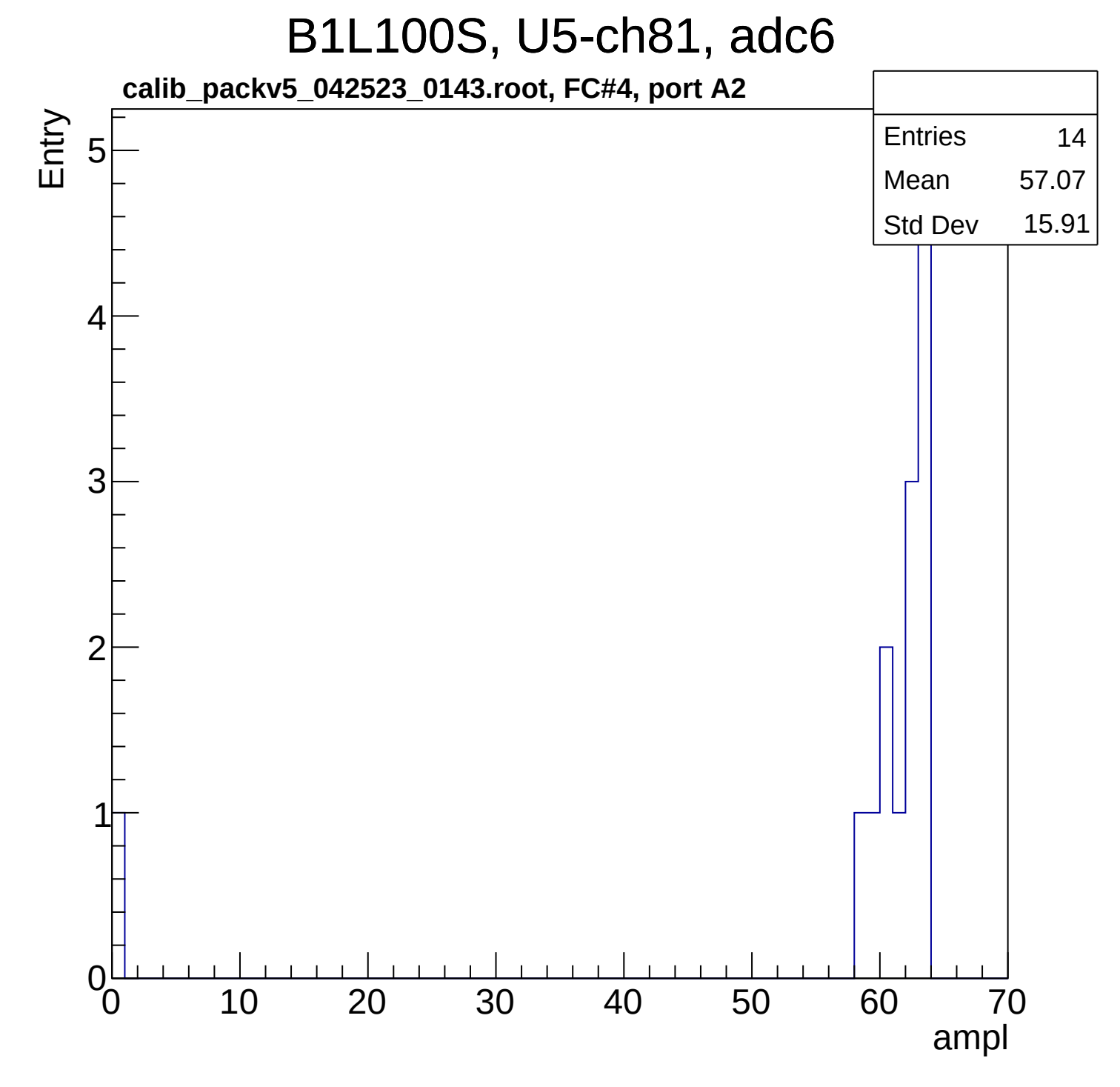
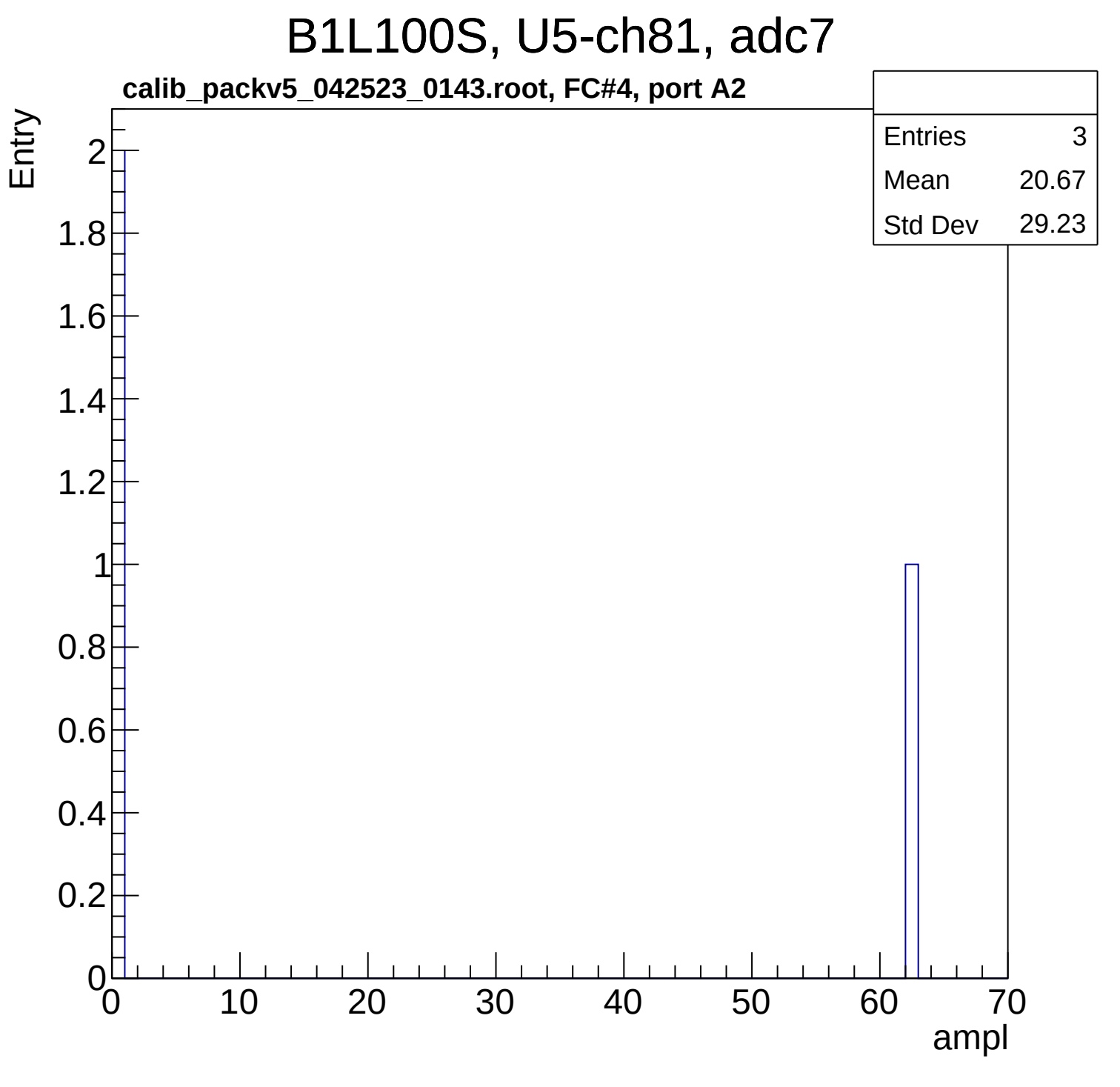
60
70


B1L100S, U5-ch81, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 54.55
Std Dev 3.374
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U5-ch81, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 48
Mean 58.81
Std Dev 3.16
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U5-ch81, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 14
Mean 57.07
Std Dev 15.91
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch81, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 20.67
Std Dev 29.23
Entry
ampl
0
0.2
0.4
0.6
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1
1.2
1.4
1.6
1.8
2
0
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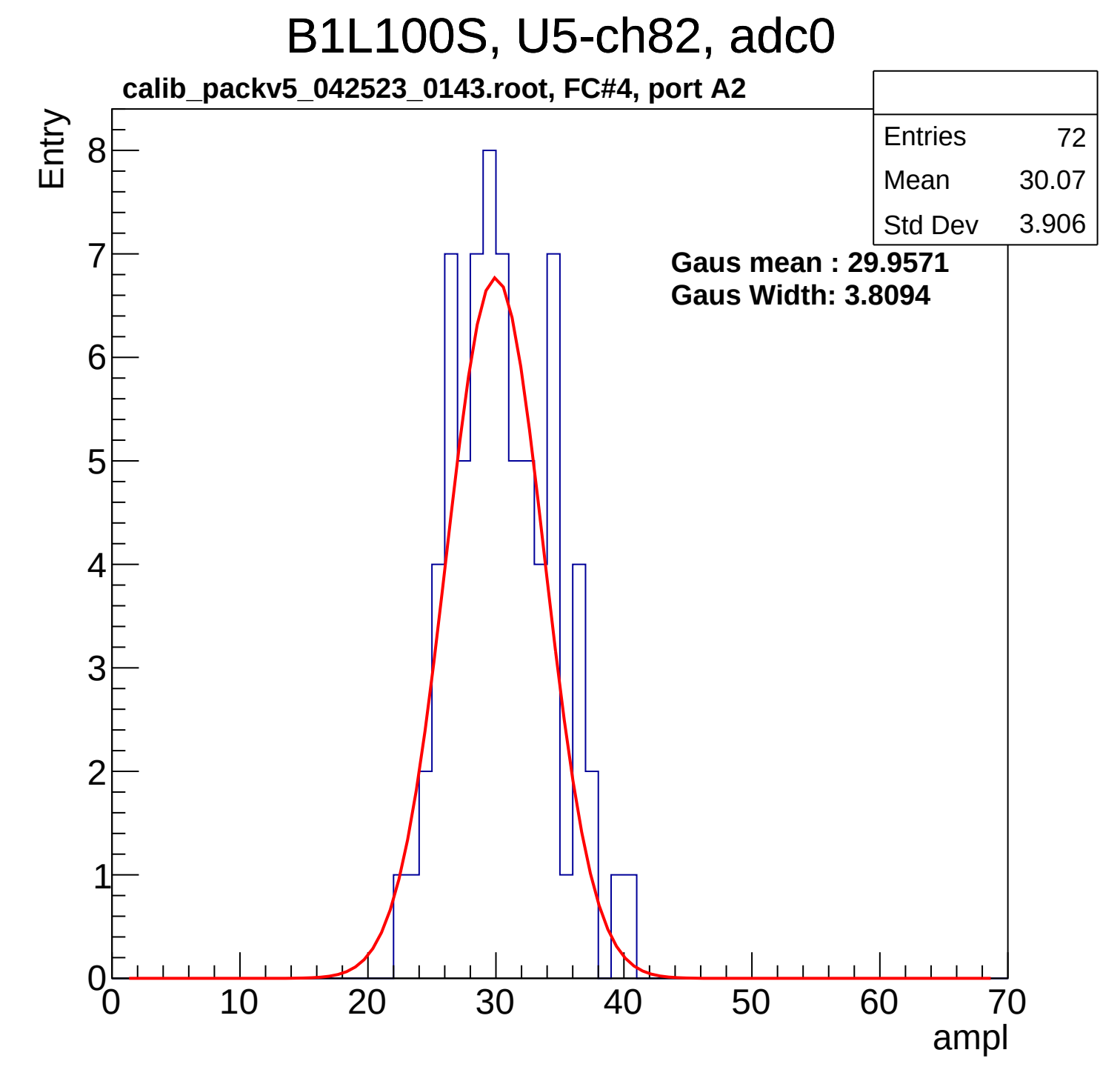
60
70


B1L100S, U5-ch82, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 30.07
Std Dev 3.906
Gaus mean : 29.9571
Gaus Width: 3.8094
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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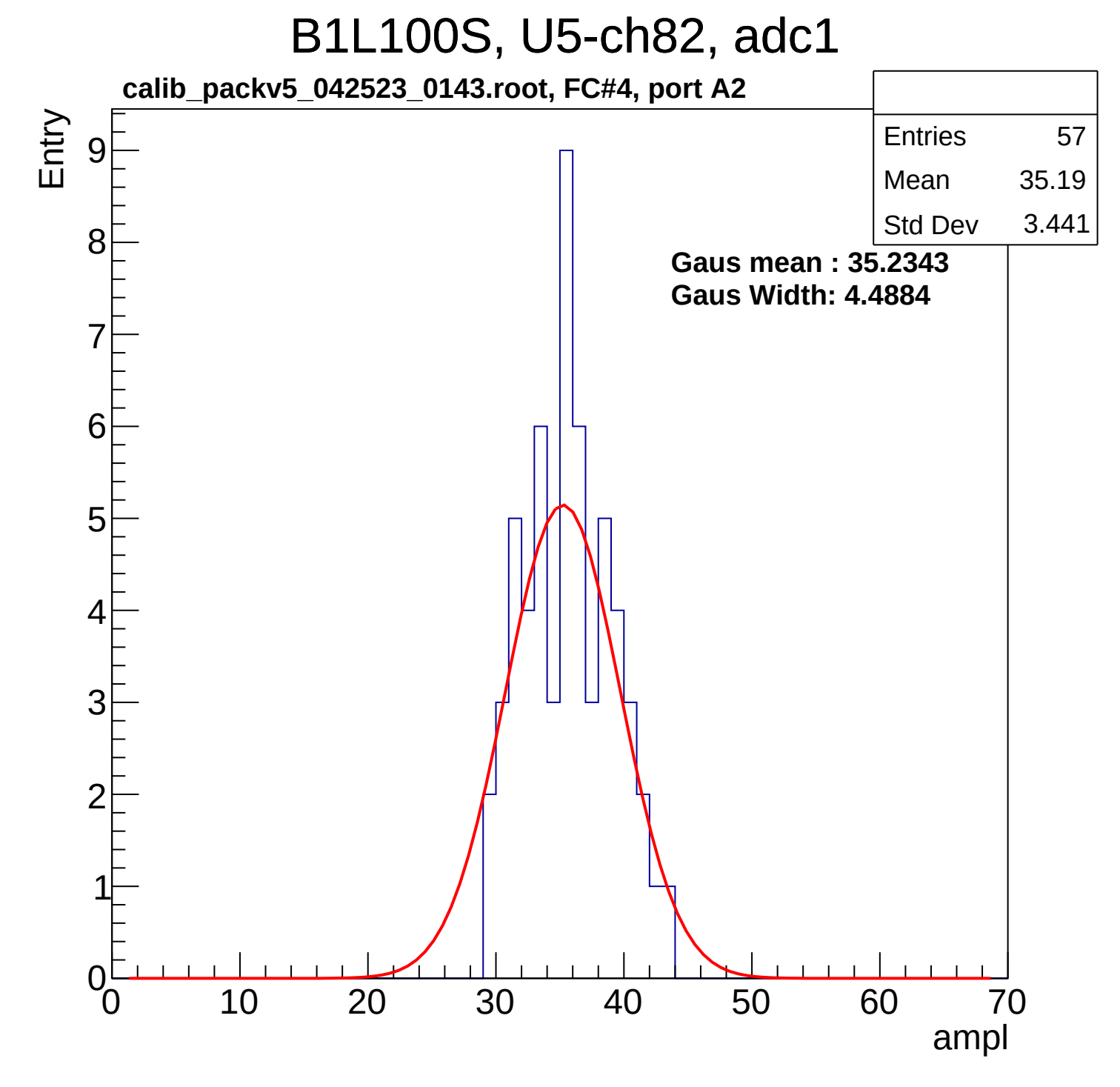
60
70


B1L100S, U5-ch82, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 35.19
Std Dev 3.441
Gaus mean : 35.2343
Gaus Width: 4.4884
Entry
ampl
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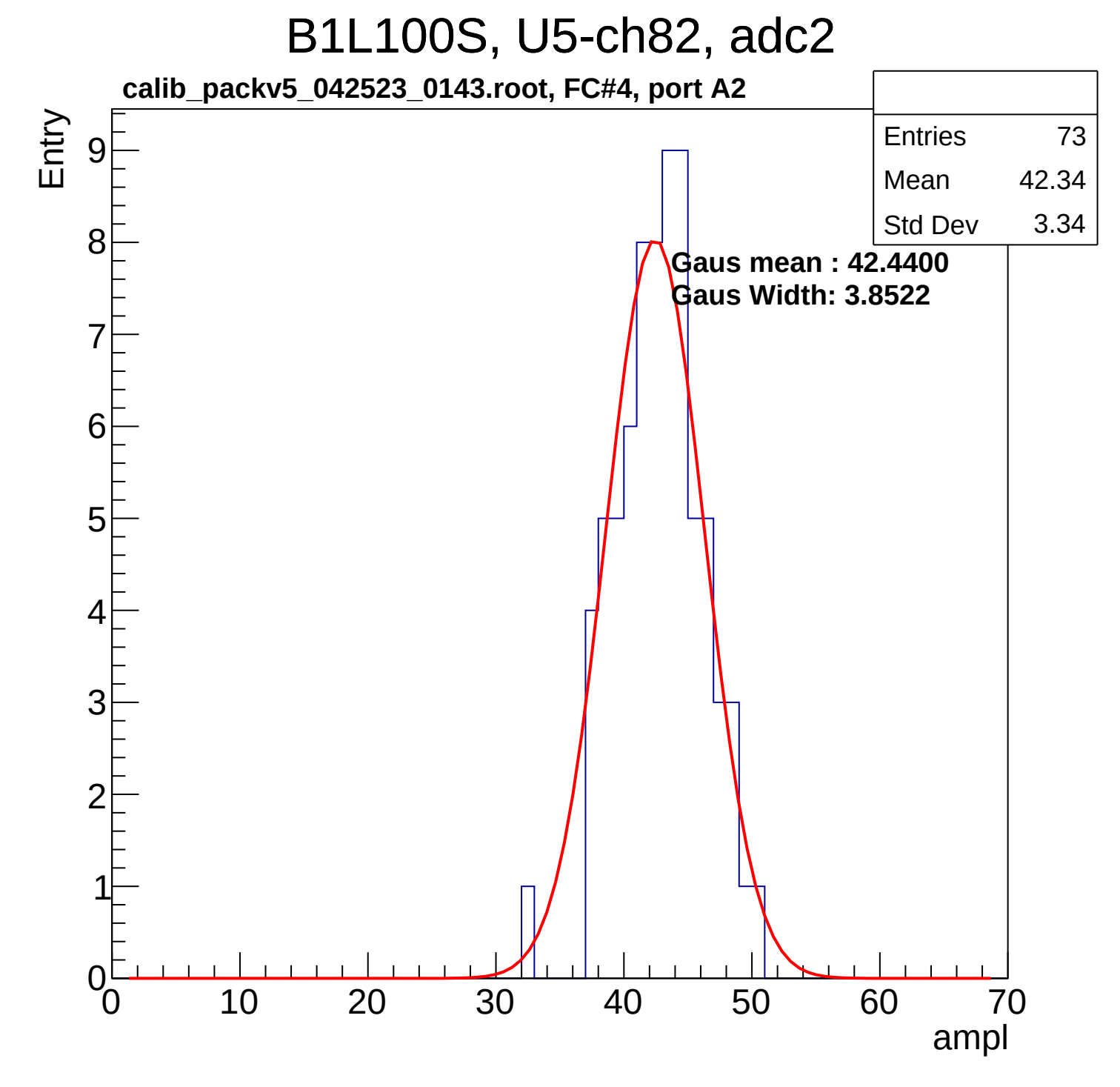
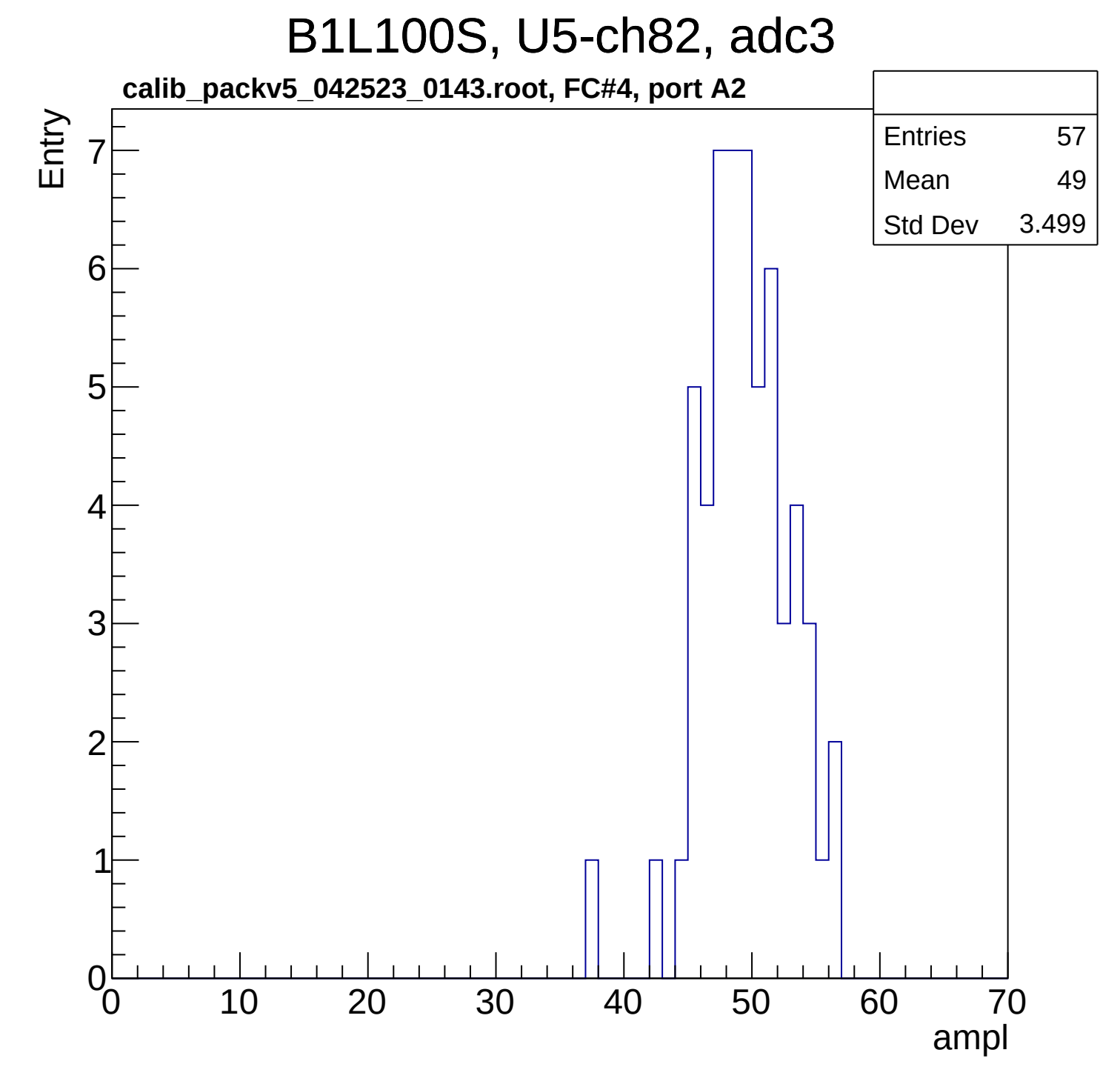
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch82, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 42.34
Std Dev 3.34
Gaus mean : 42.4400
Gaus Width: 3.8522
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch82, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 49
Std Dev 3.499
Entry
ampl
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1
2
3
4
5
6
7
0
10
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60
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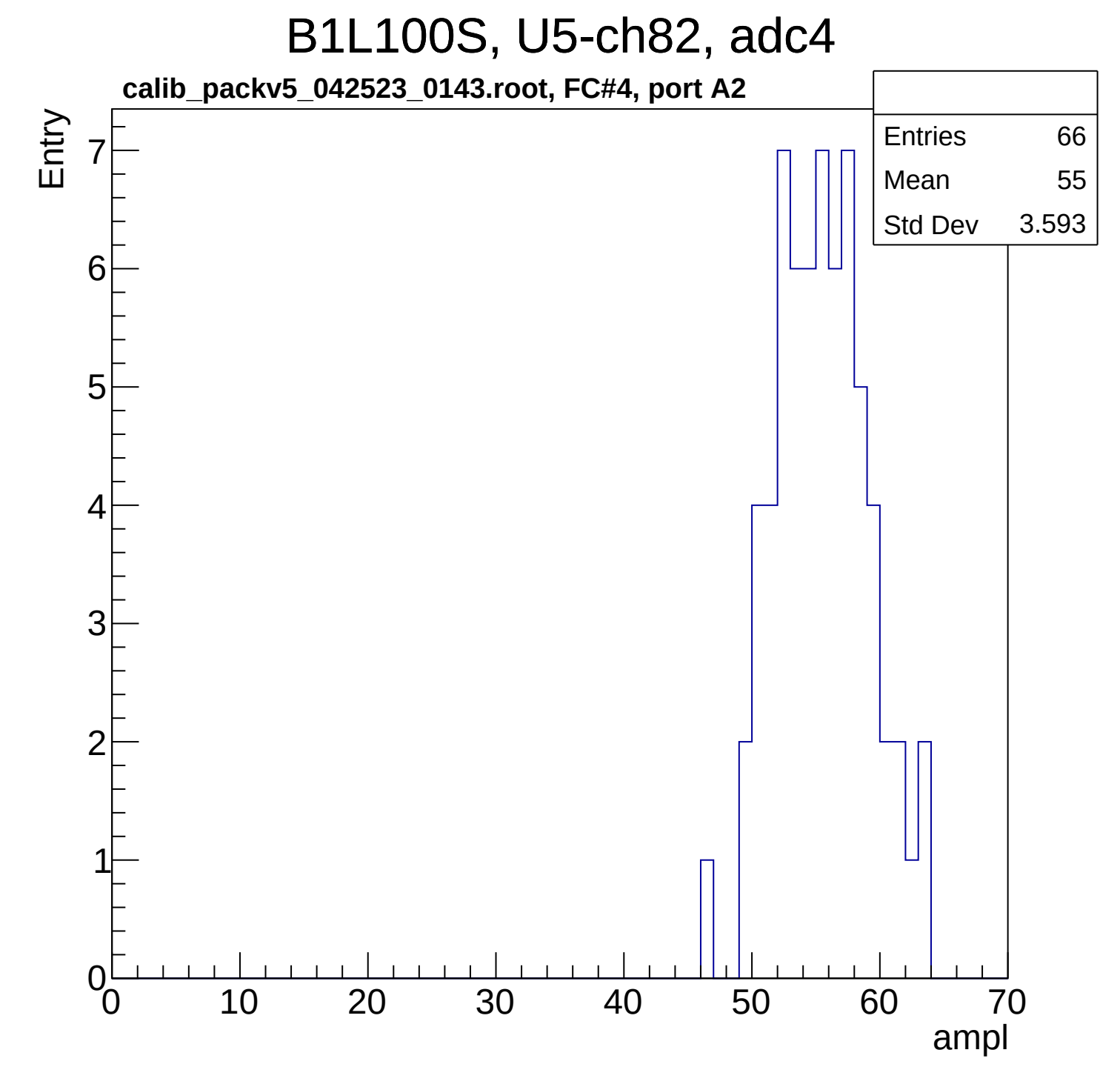
B1L100S, U5-ch82, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 55
Std Dev 3.593
Entry
ampl
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1
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3
4
5
6
7
0
10
20
30
40
50
60
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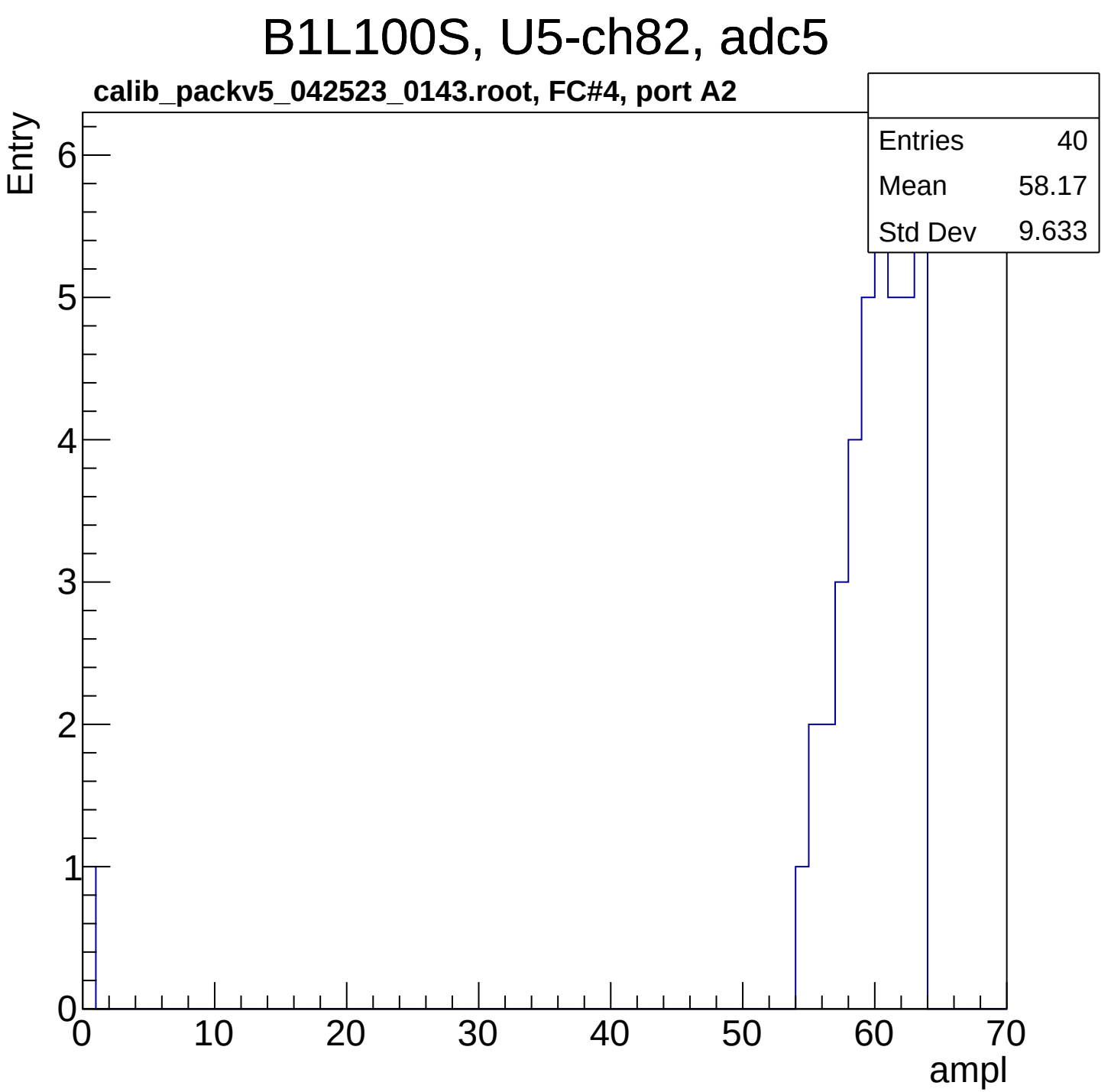
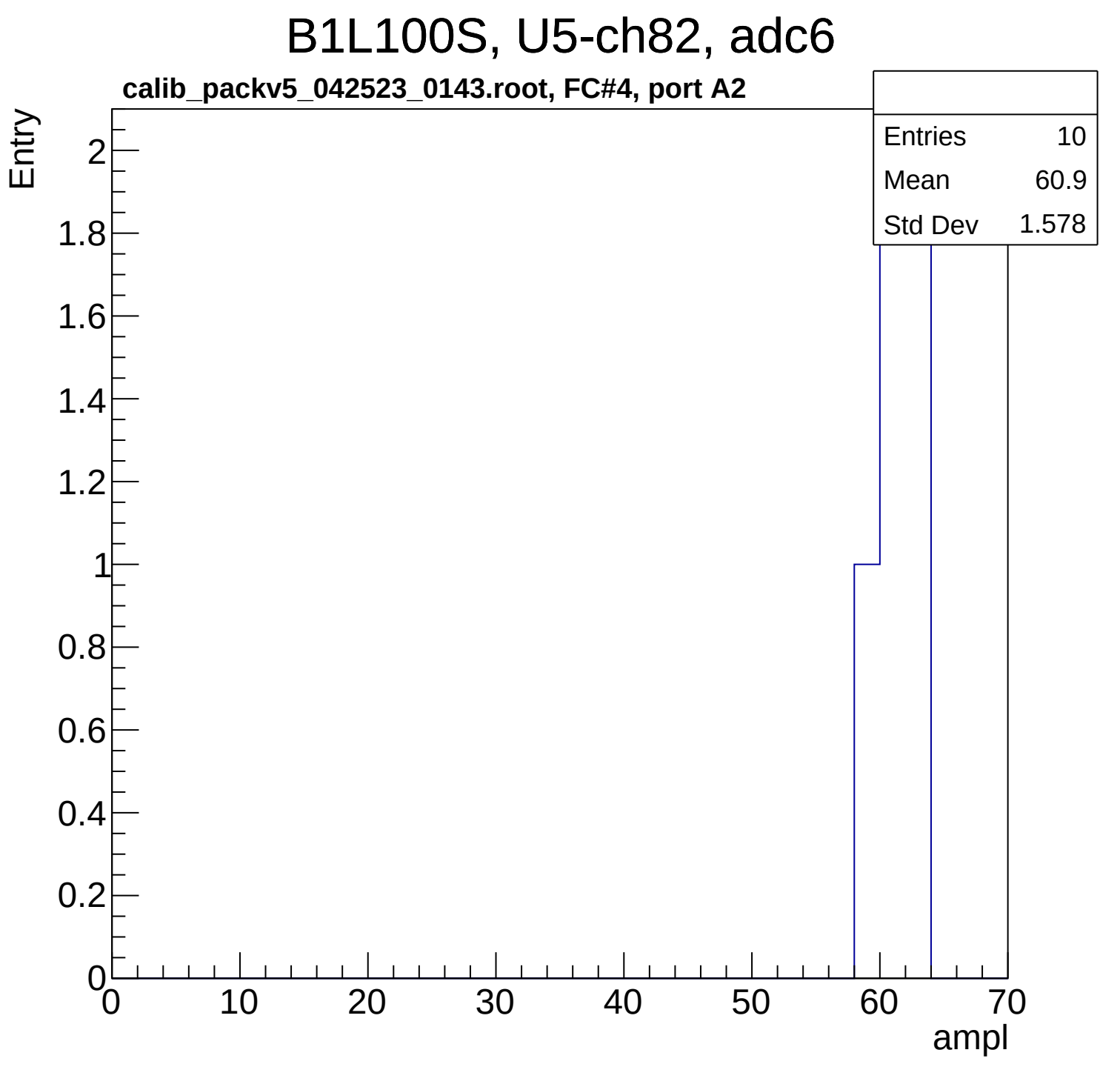
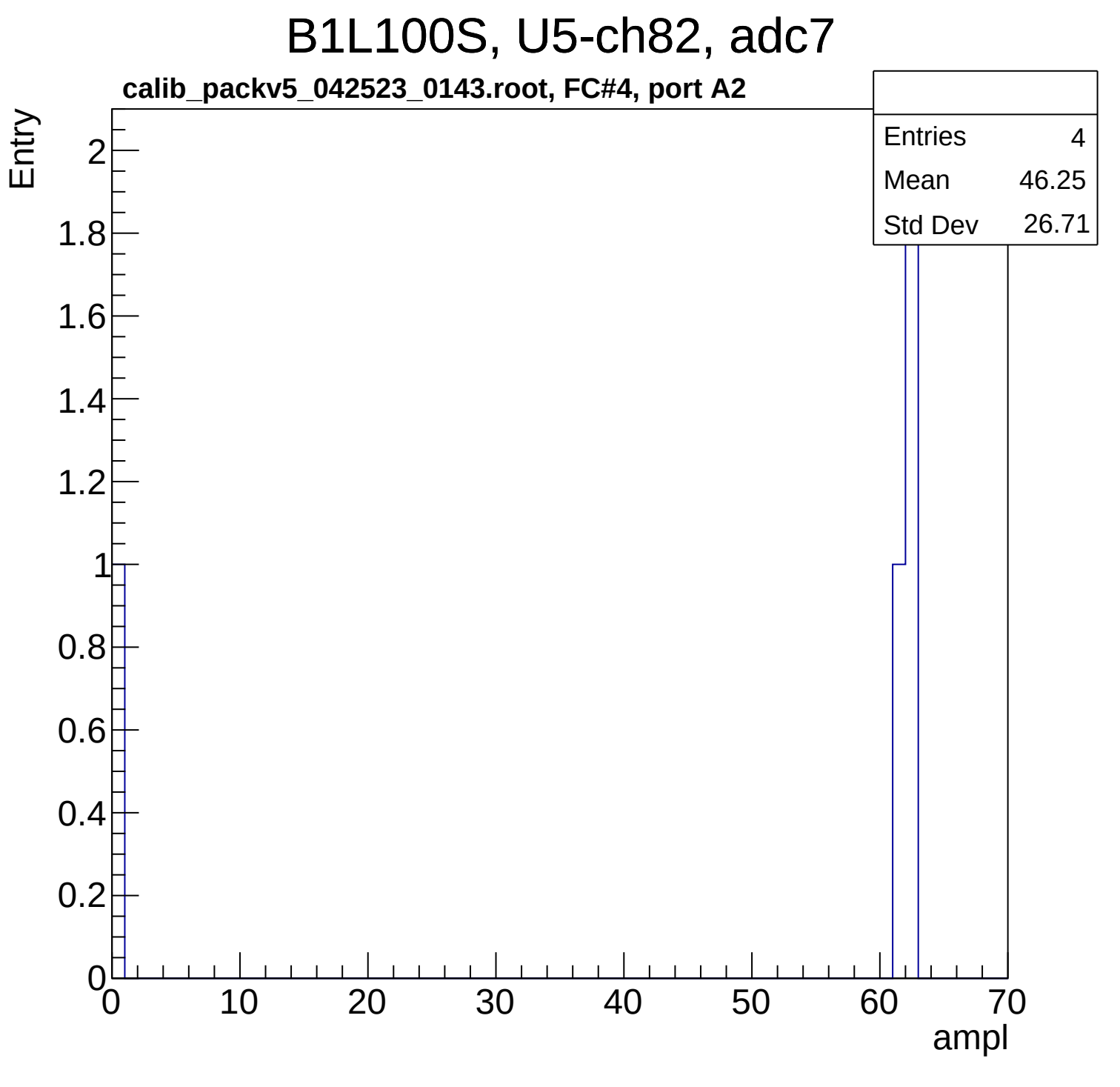
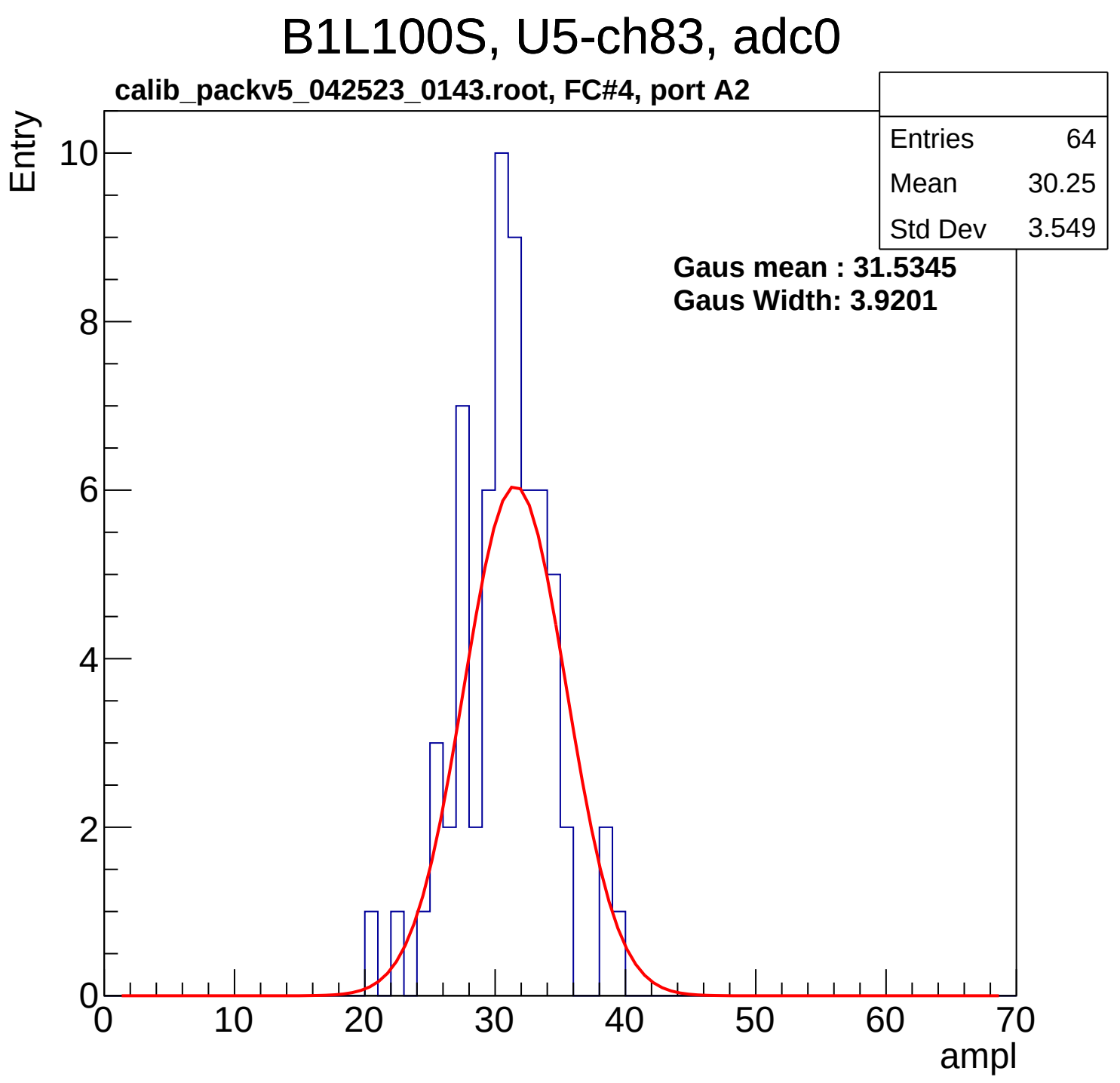
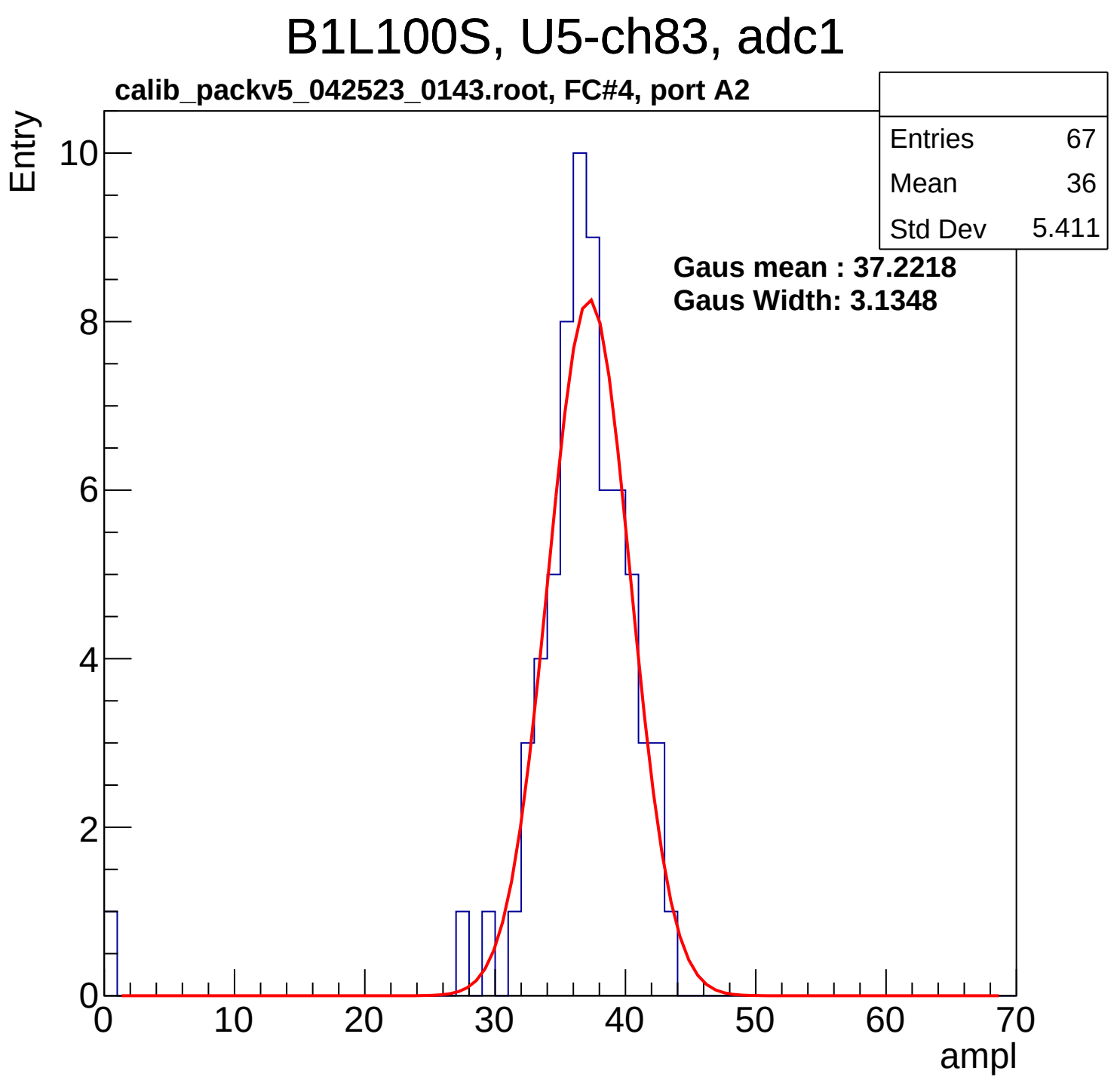
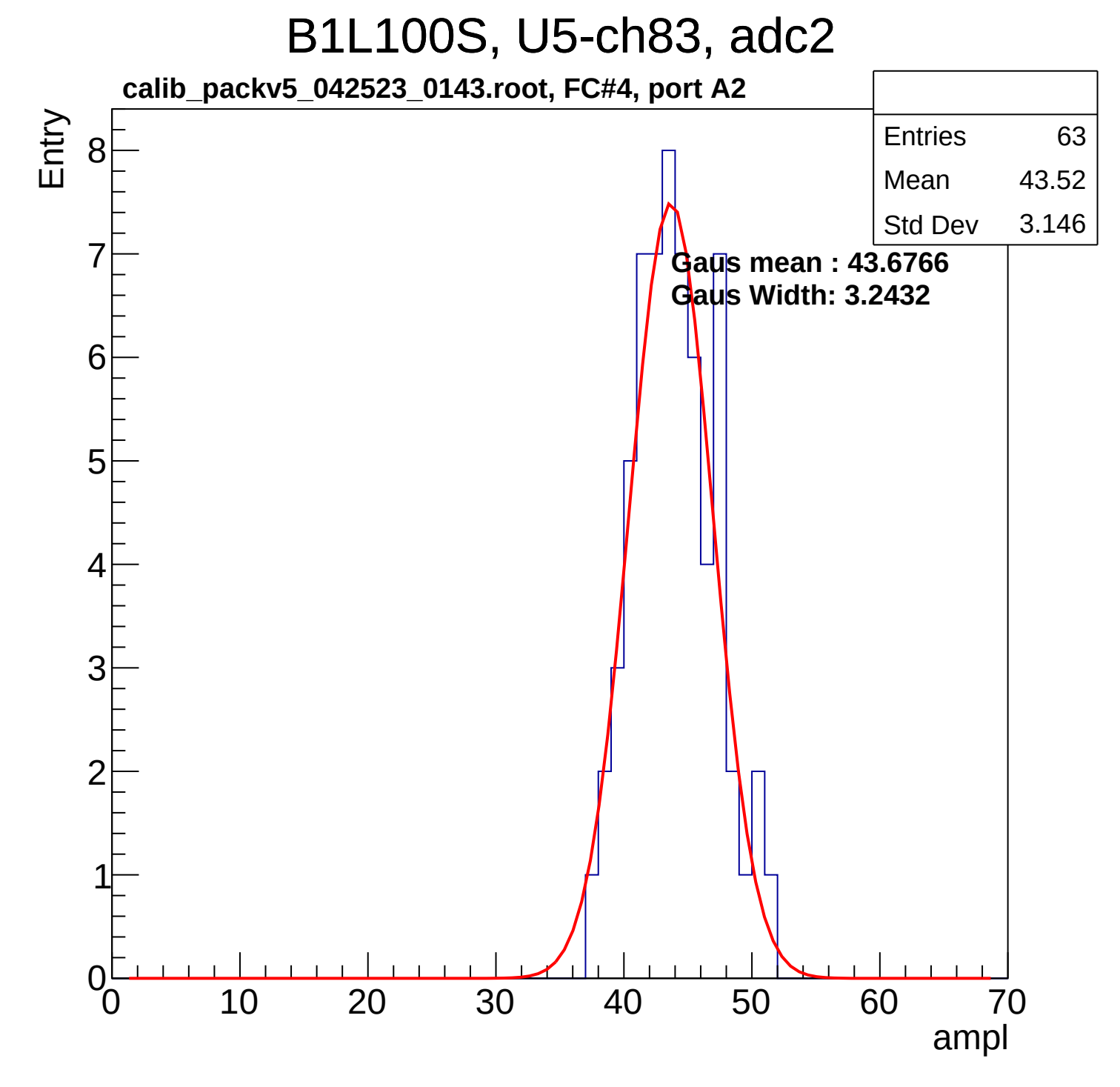

B1L100S, U5-ch82, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 40
Mean 58.17
Std Dev 9.633
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

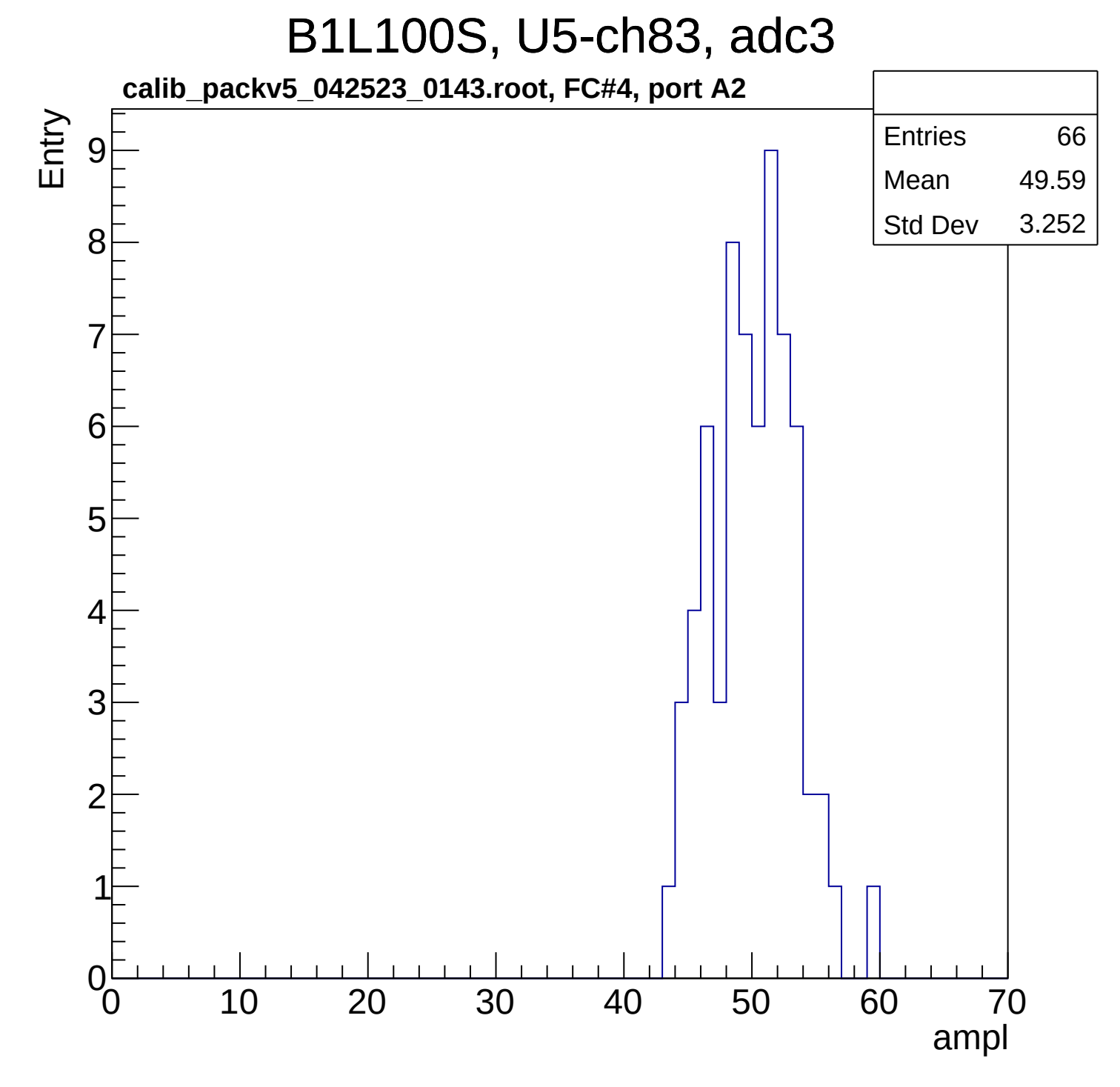

B1L100S, U5-ch82, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 10
Mean 60.9
Std Dev 1.578
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L100S, U5-ch82, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 4
Mean 46.25
Std Dev 26.71
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L100S, U5-ch83, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 30.25
Std Dev 3.549
Gaus mean : 31.5345
Gaus Width: 3.9201
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch83, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 36
Std Dev 5.411
Gaus mean : 37.2218
Gaus Width: 3.1348
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch83, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 43.52
Std Dev 3.146
Gaus mean : 43.6766
Gaus Width: 3.2432
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch83, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 49.59
Std Dev 3.252
Entry
ampl
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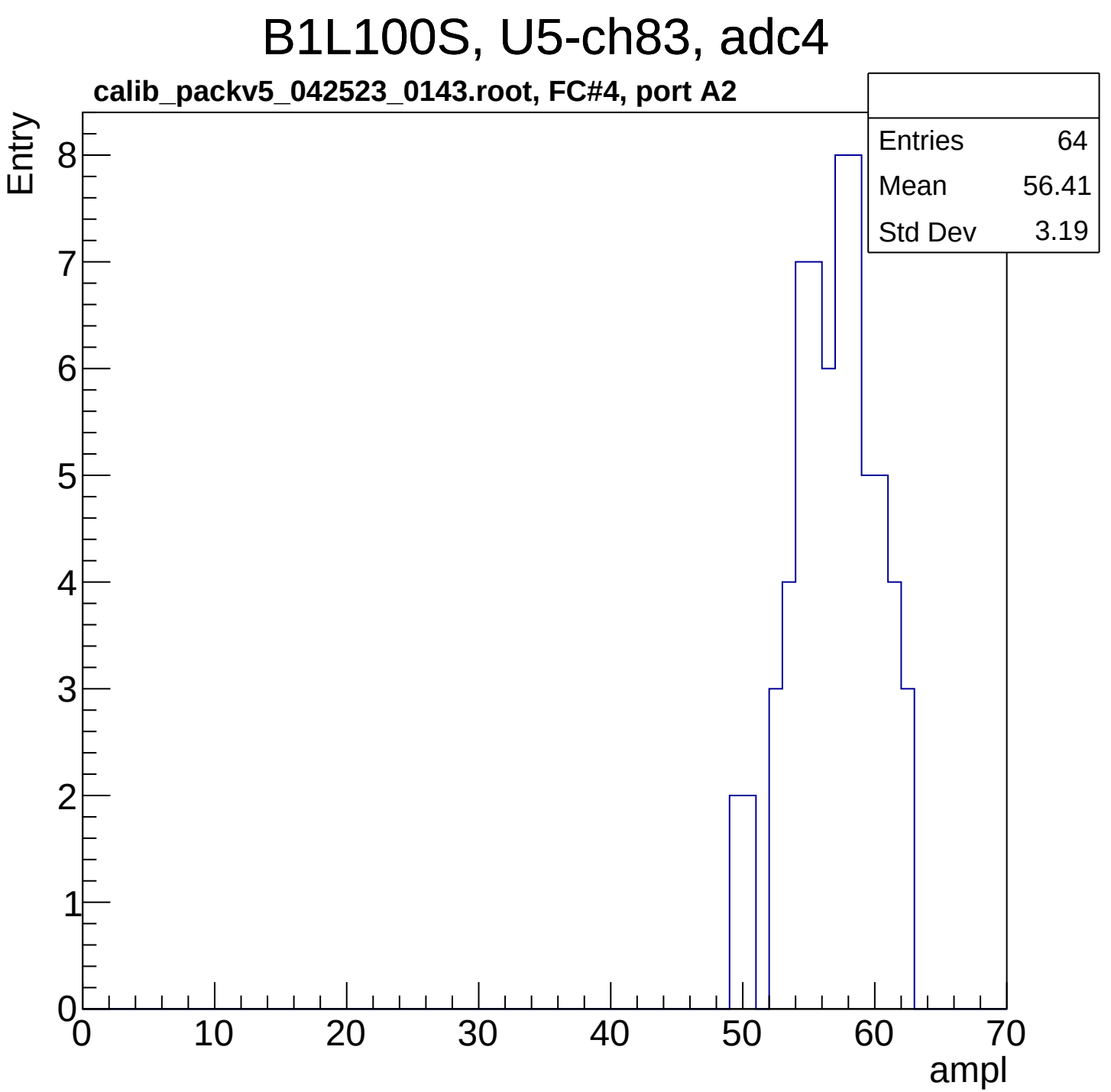
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch83, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 56.41
Std Dev 3.19
Entry
ampl
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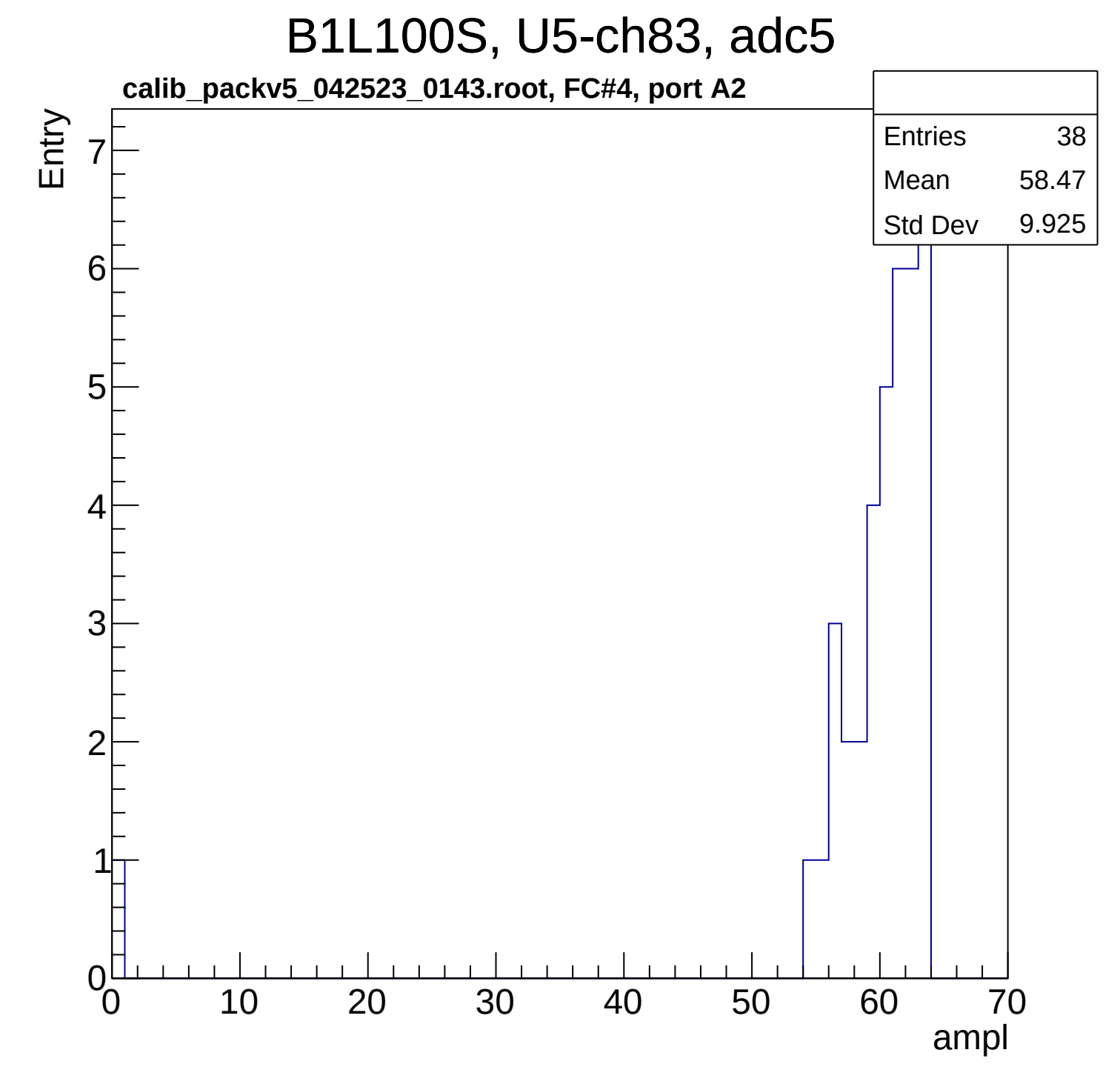
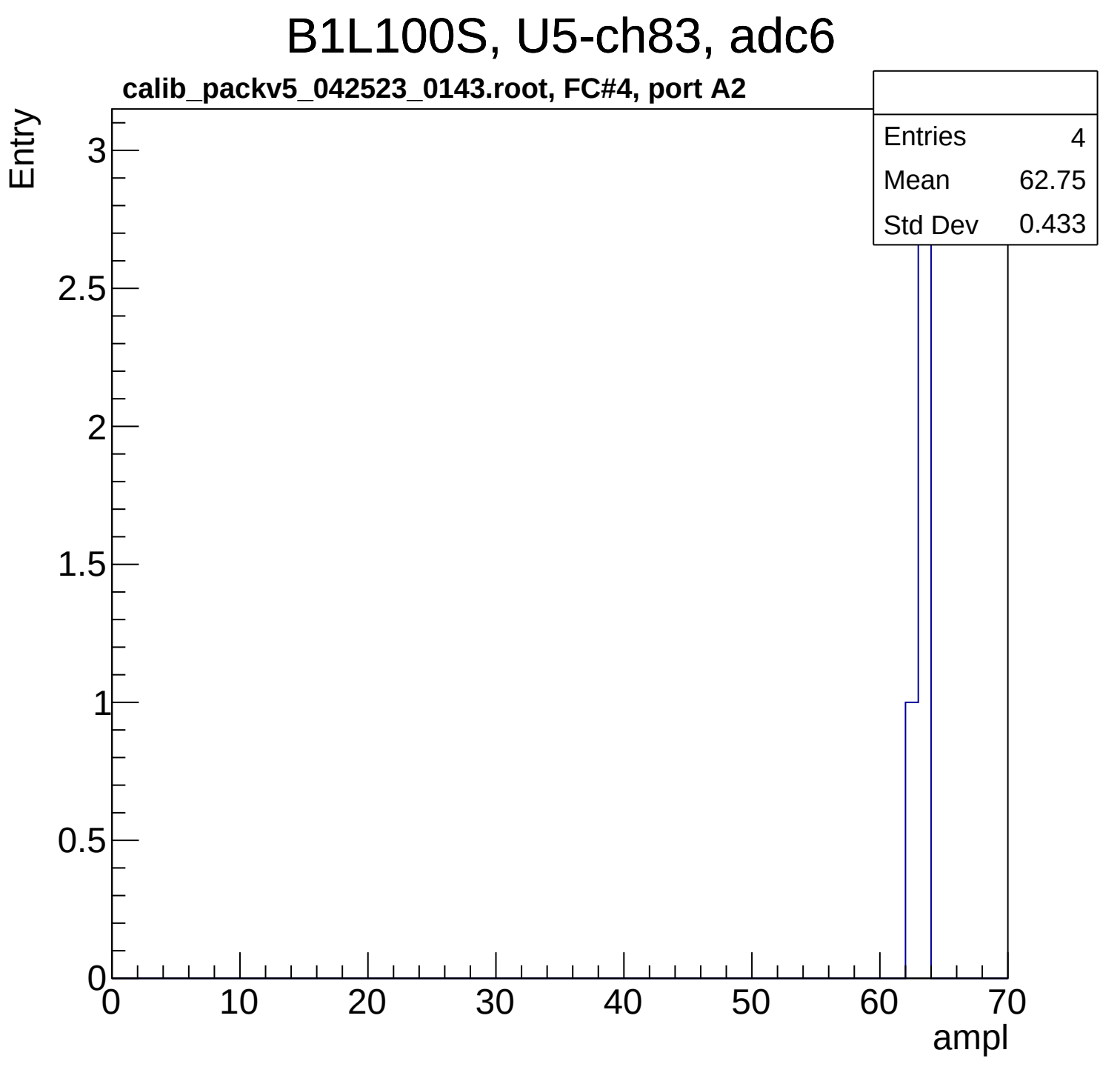
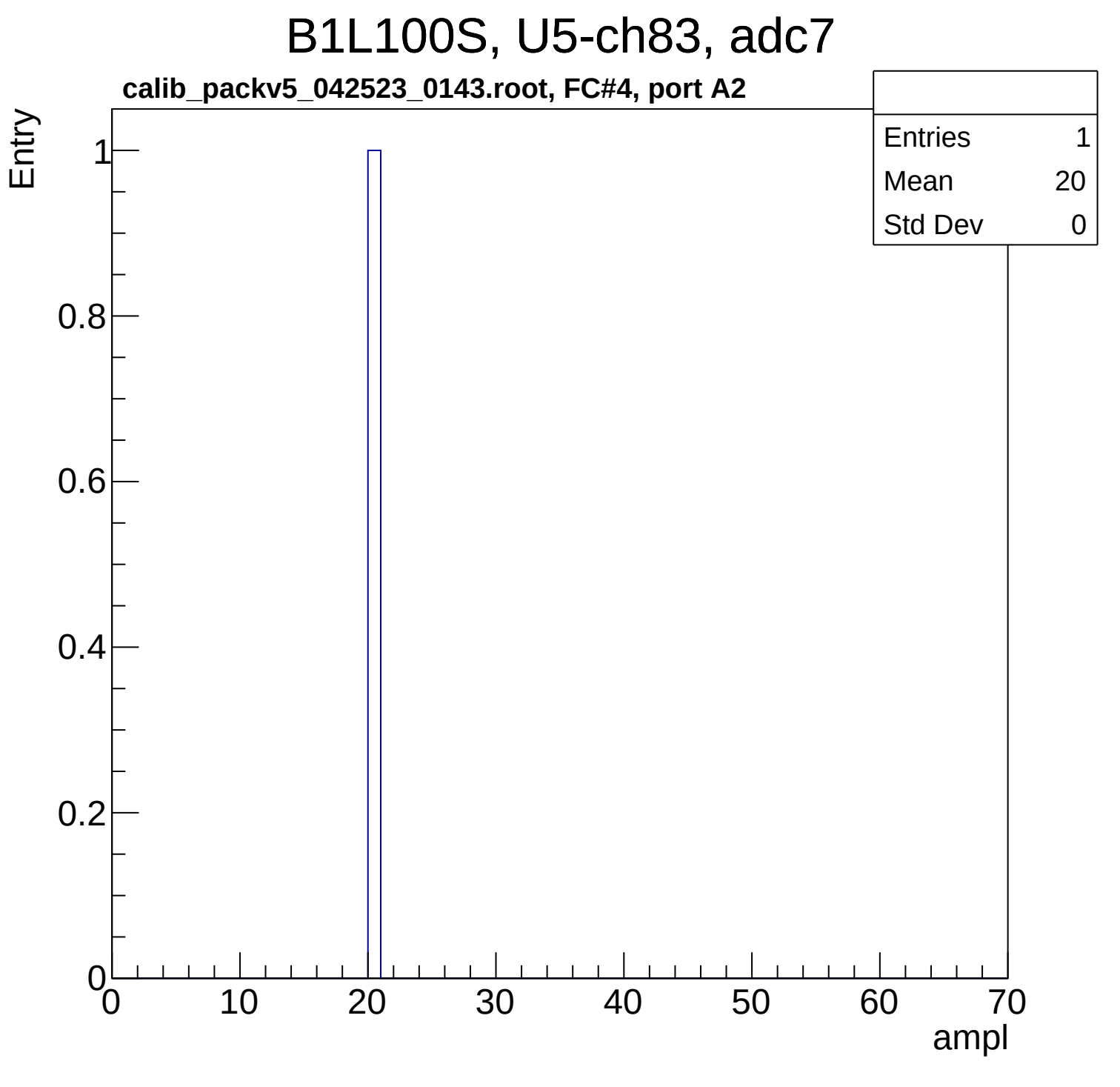
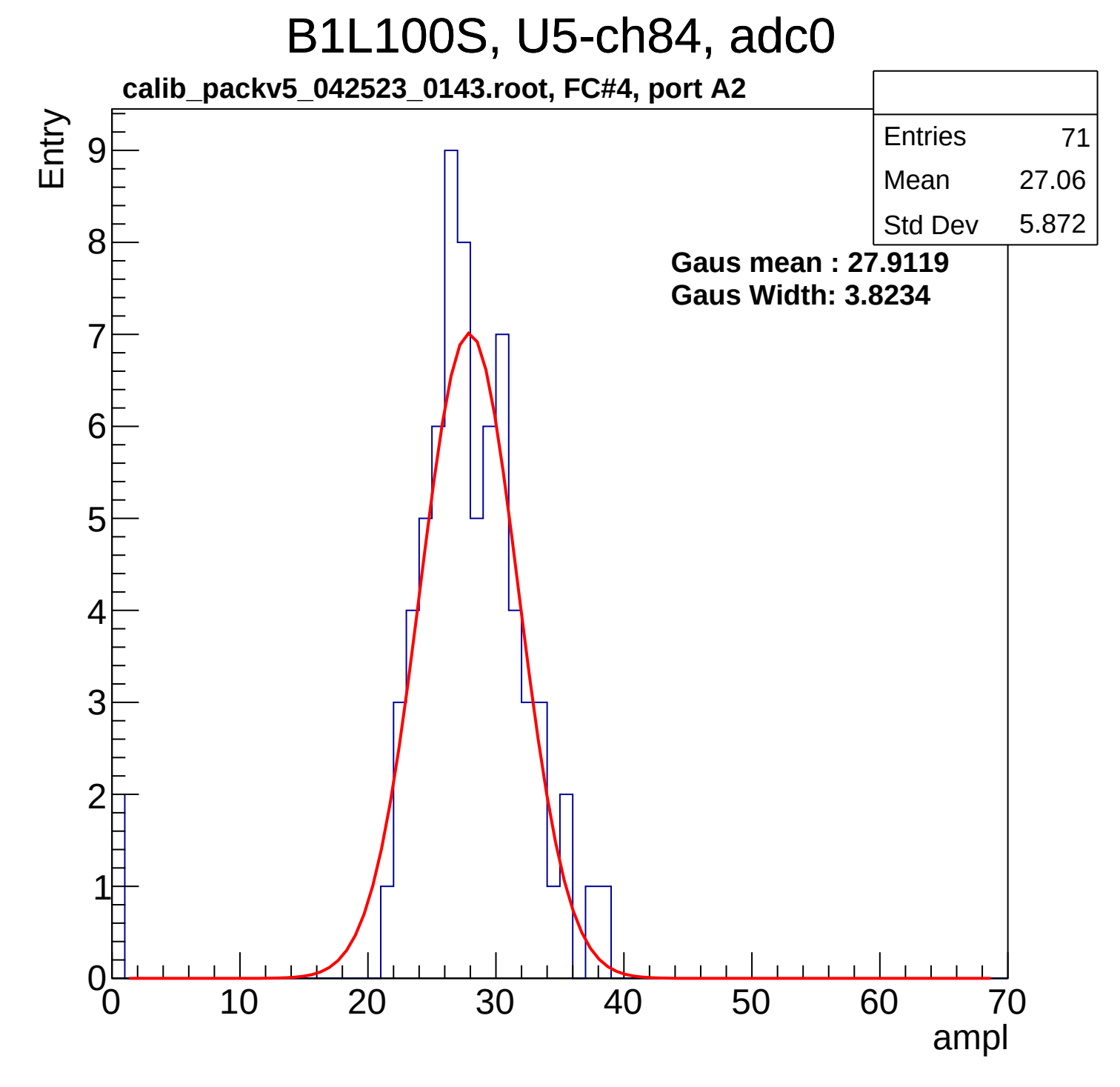
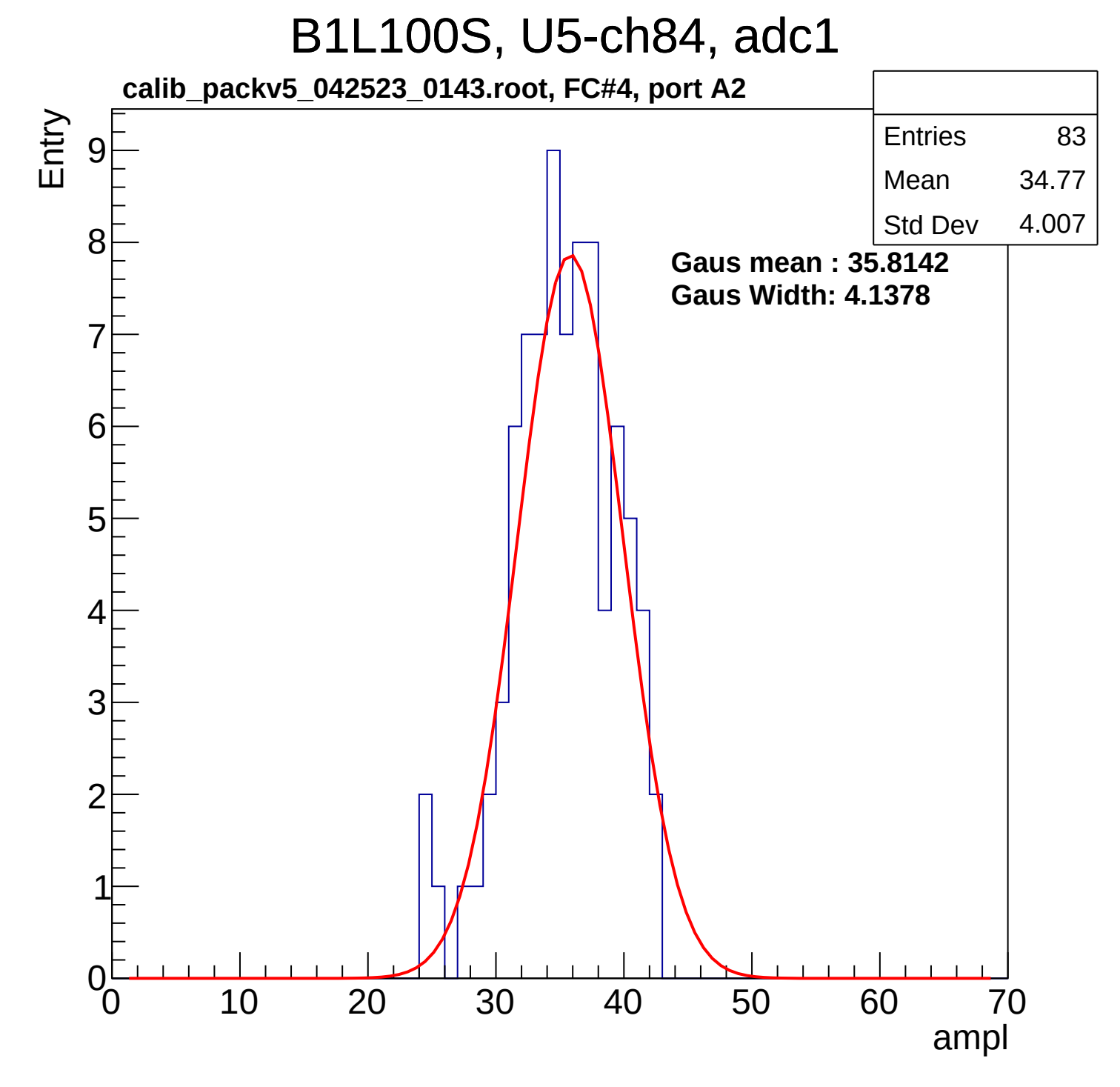
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

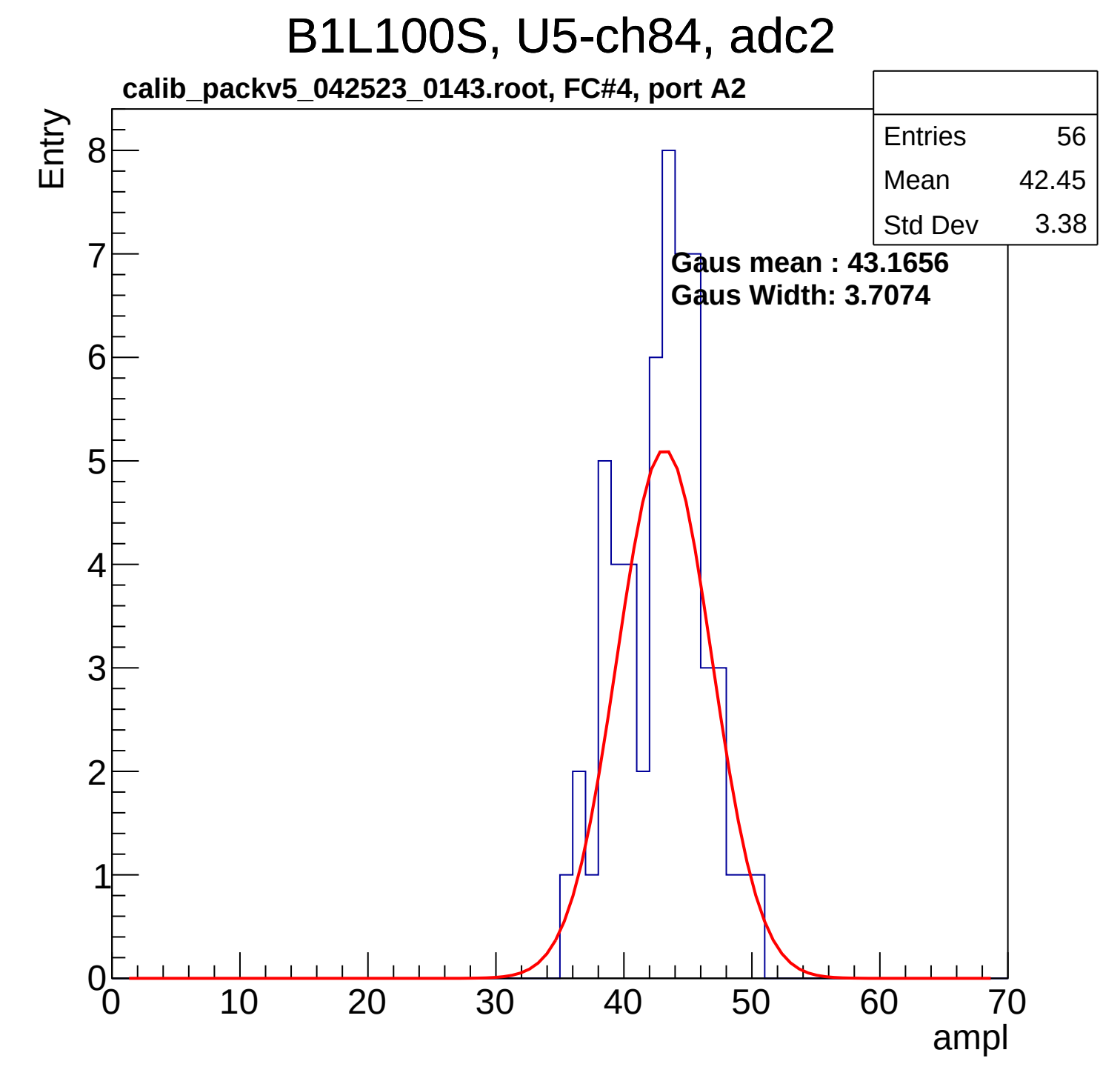

B1L100S, U5-ch83, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 38
Mean 58.47
Std Dev 9.925
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

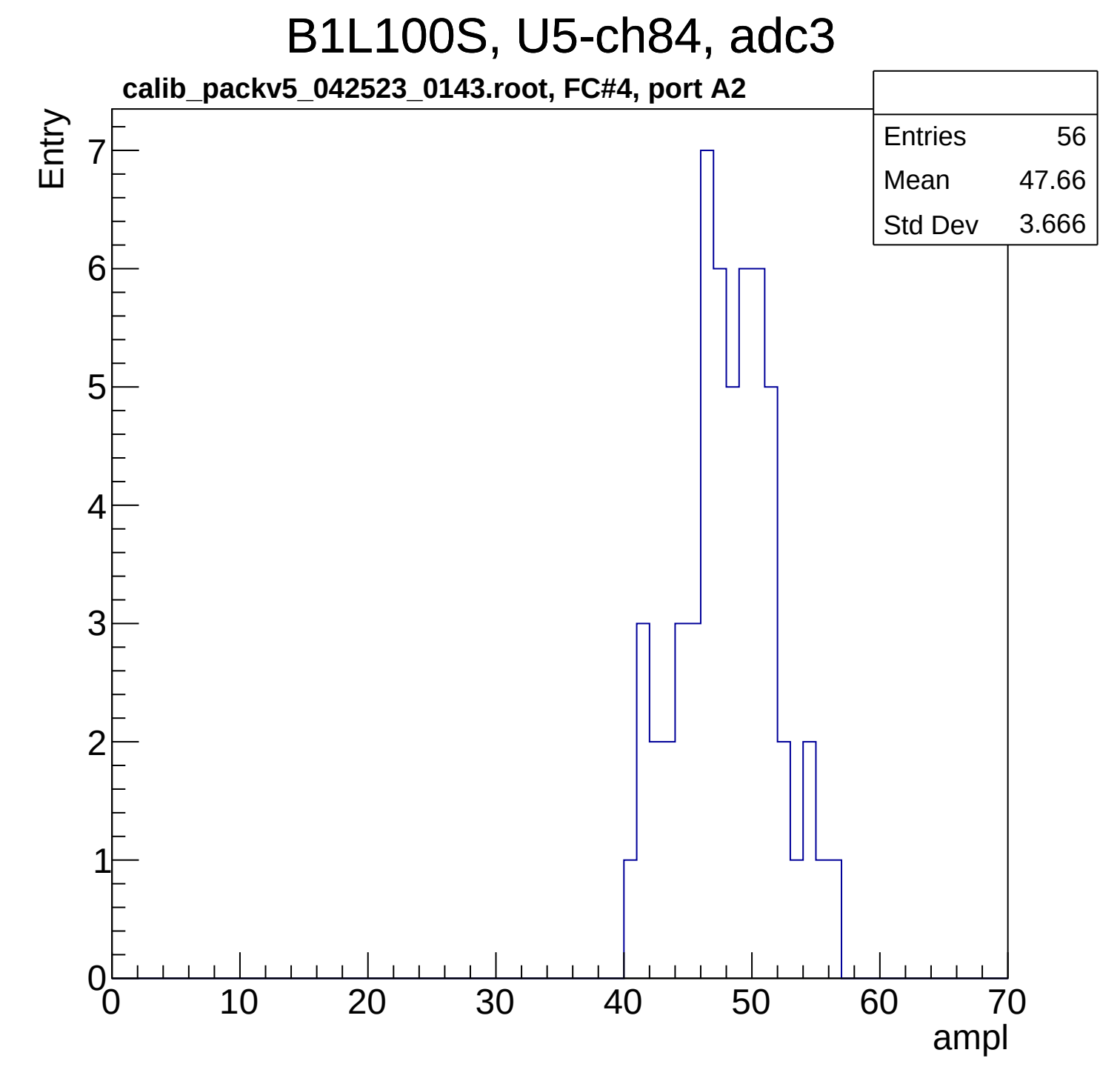

B1L100S, U5-ch83, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 4
Mean 62.75
Std Dev 0.433
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

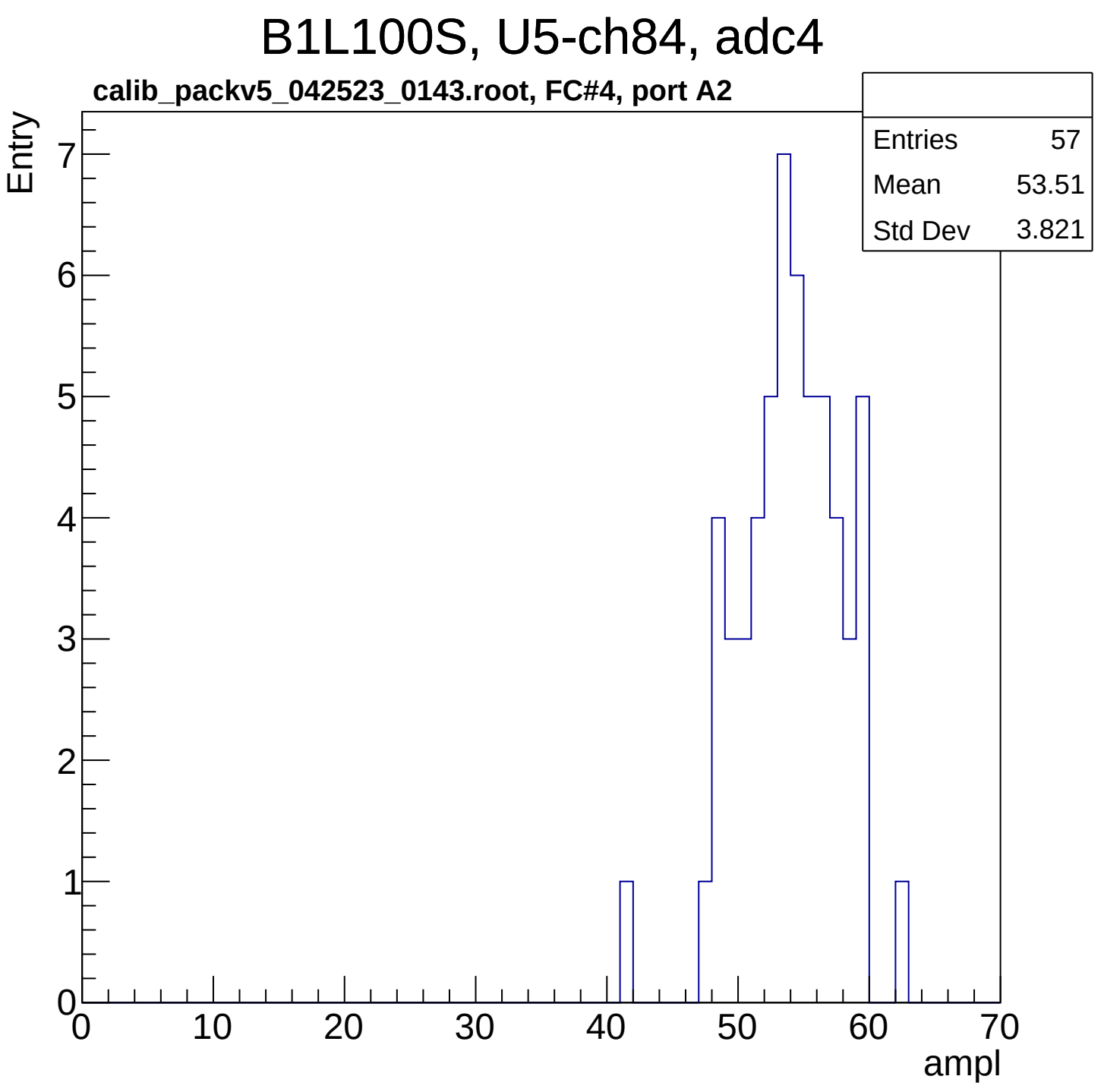

B1L100S, U5-ch83, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 20
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

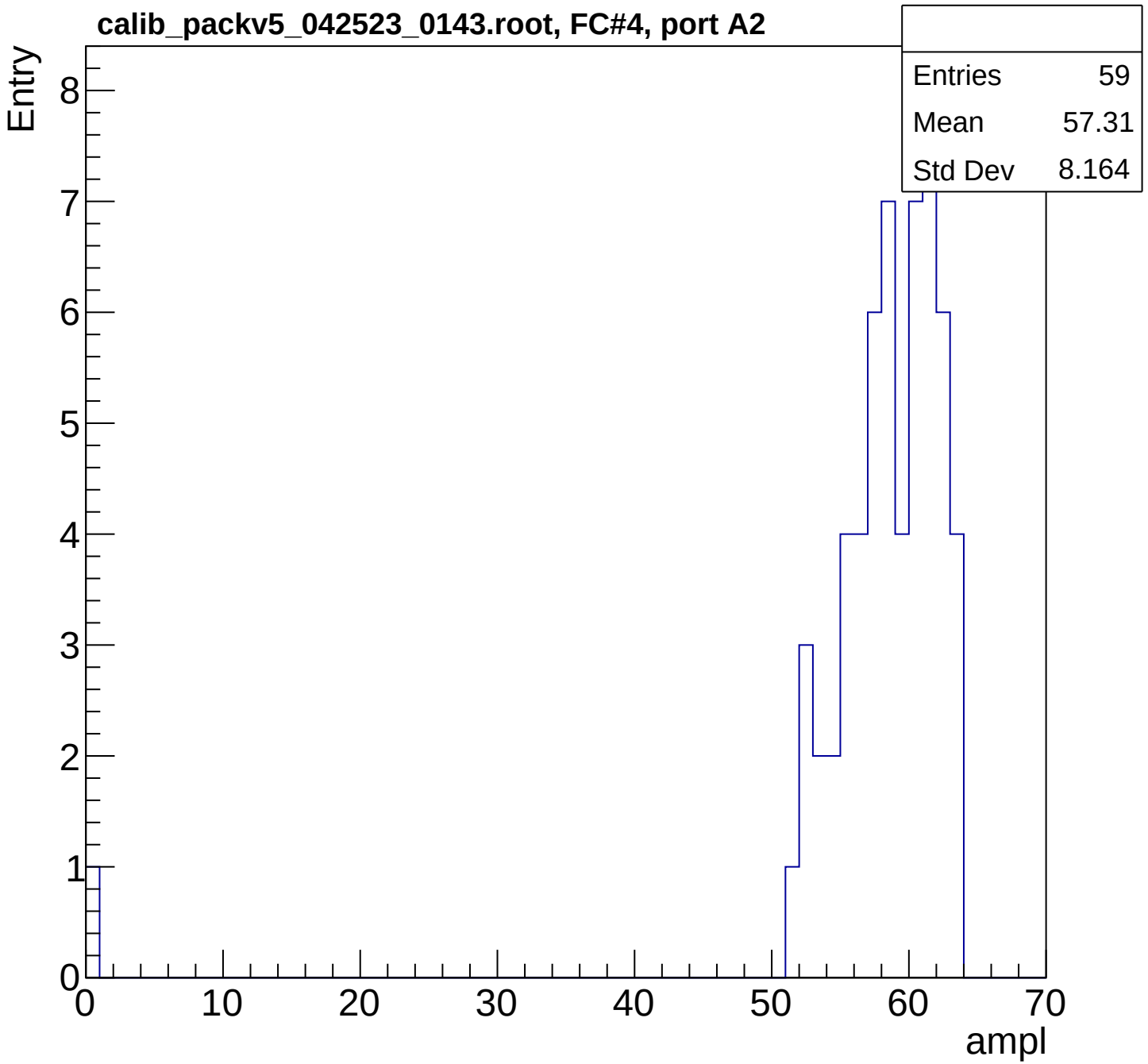

B1L100S, U5-ch84, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 27.06
Std Dev 5.872
Gaus mean : 27.9119
Gaus Width: 3.8234
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

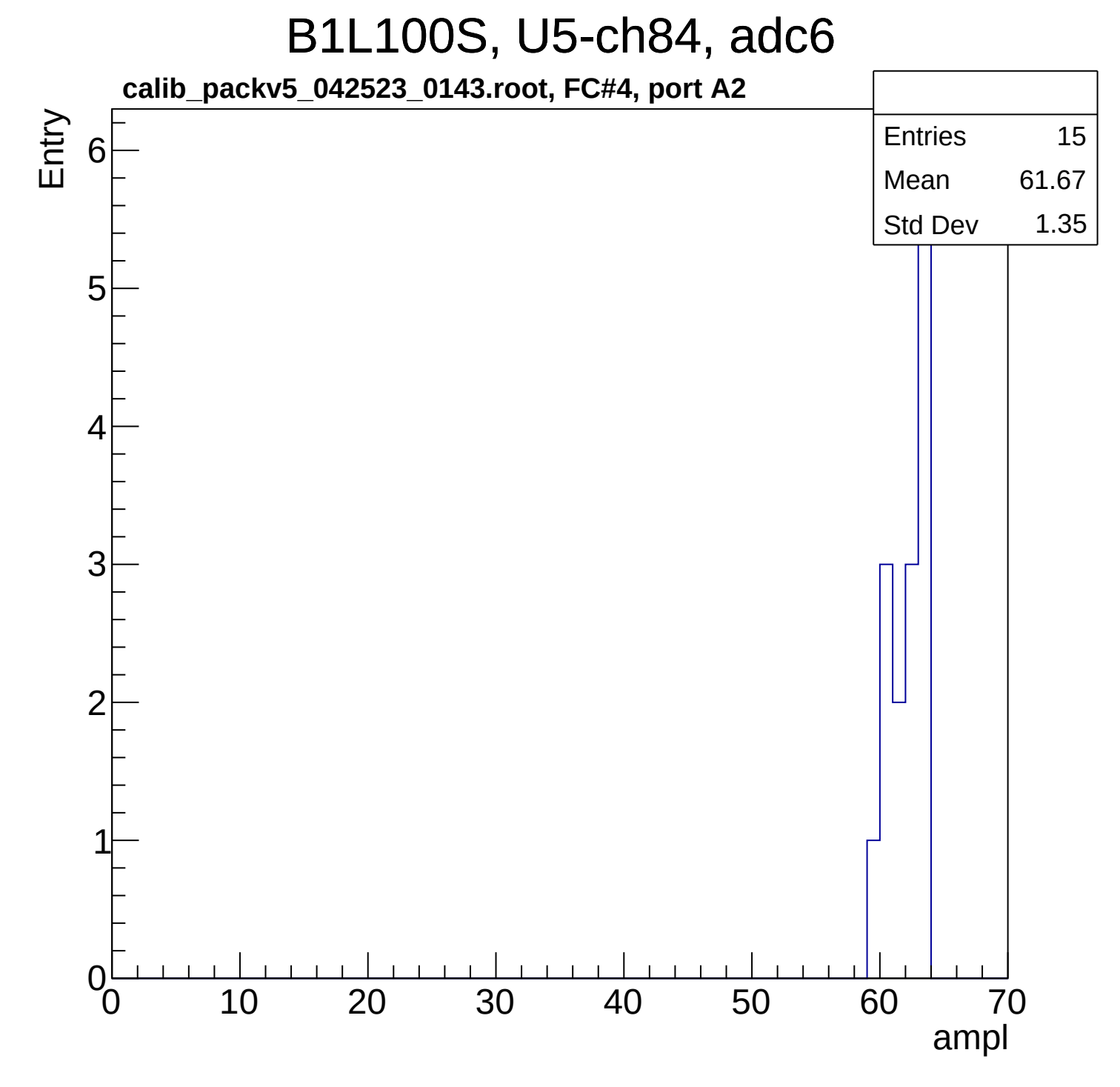

B1L100S, U5-ch84, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 83
Mean 34.77
Std Dev 4.007
Gaus mean : 35.8142
Gaus Width: 4.1378
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

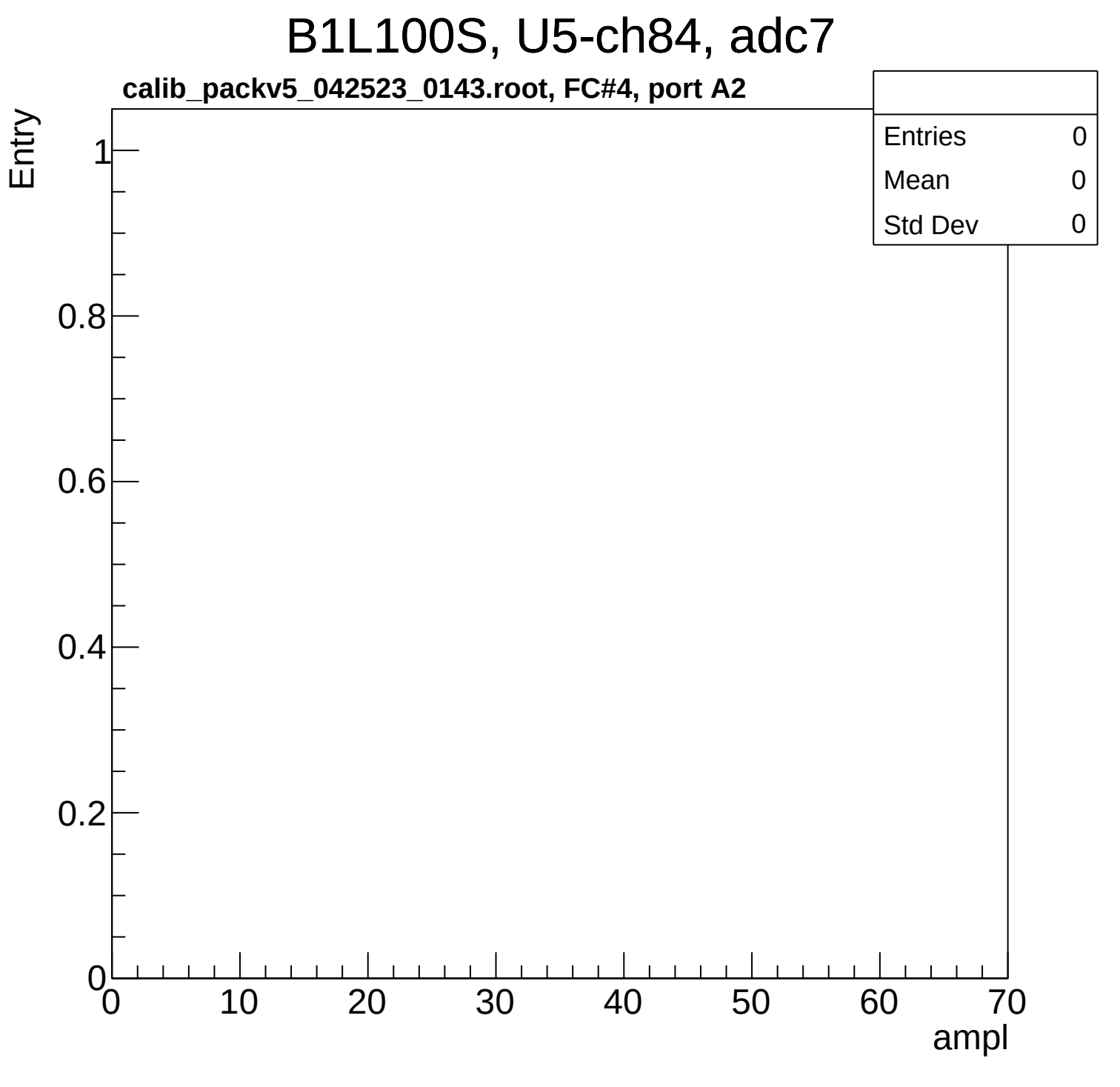

B1L100S, U5-ch84, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 42.45
Std Dev 3.38
Gaus mean : 43.1656
Gaus Width: 3.7074
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

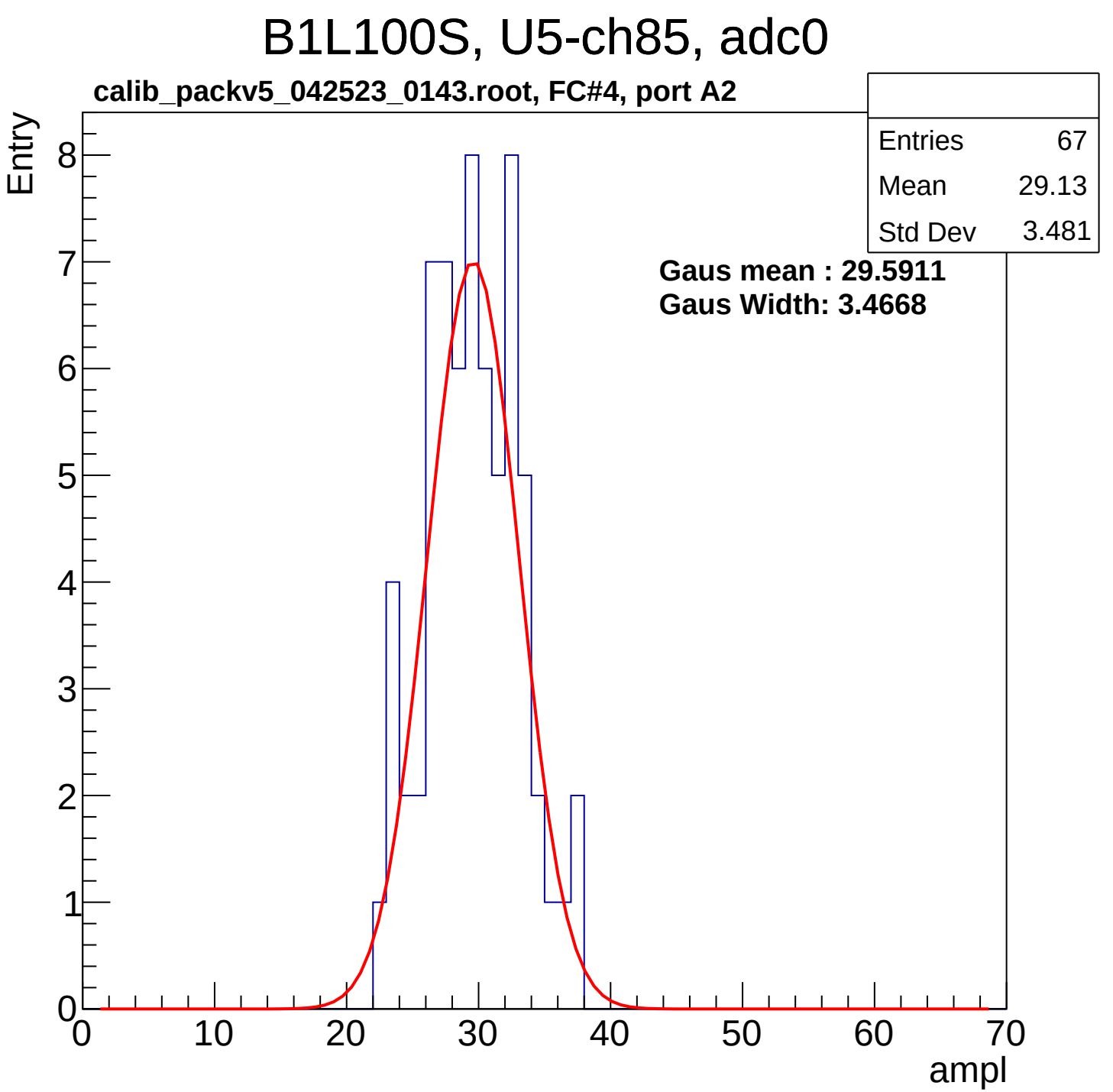

B1L100S, U5-ch84, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 47.66
Std Dev 3.666
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U5-ch84, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 53.51
Std Dev 3.821
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U5-ch84, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 57.31
Std Dev 8.164
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch84, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 15
Mean 61.67
Std Dev 1.35
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch84, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch85, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 29.13
Std Dev 3.481
Gaus mean : 29.5911
Gaus Width: 3.4668
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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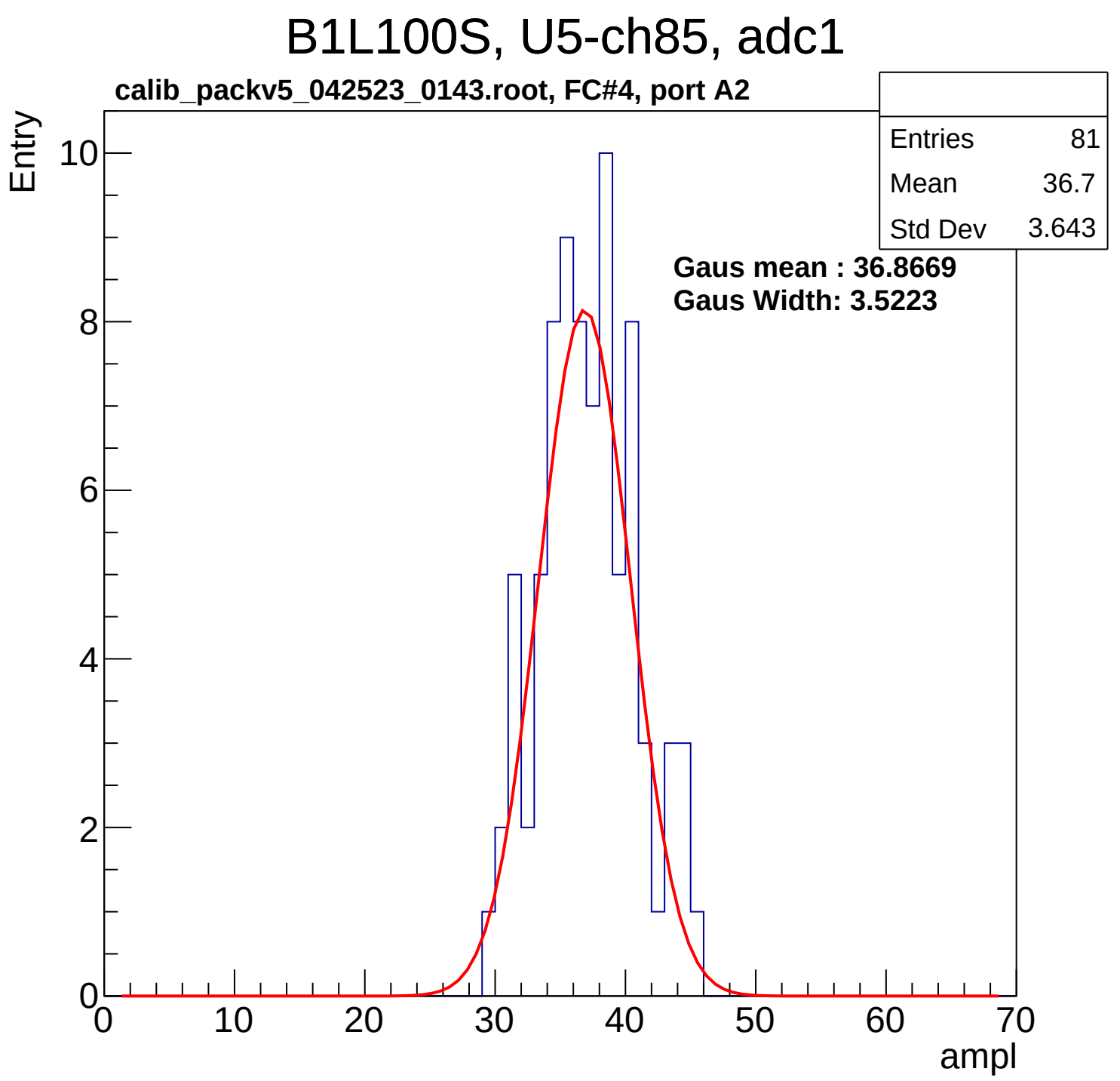
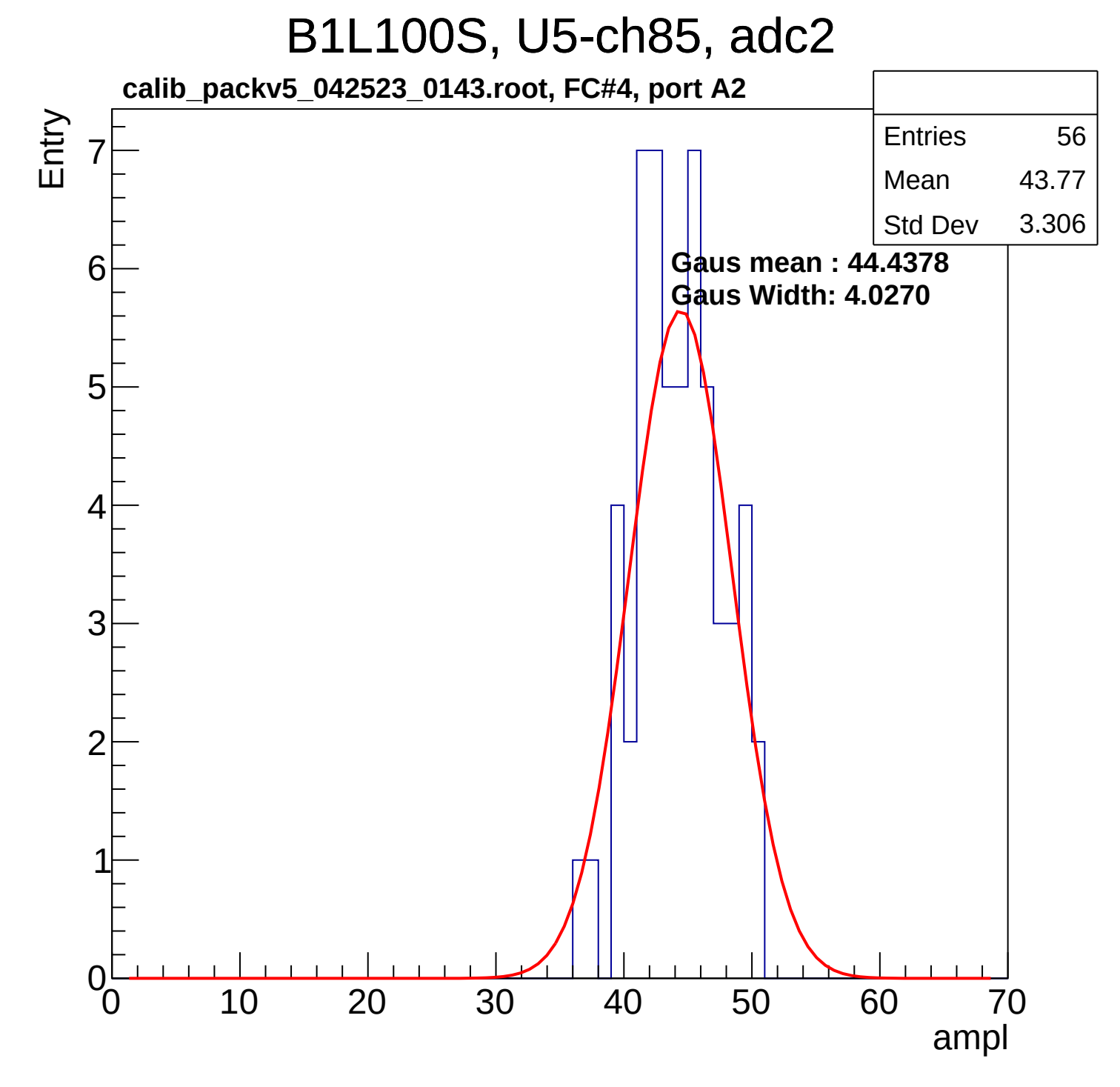
20
30
40
50
60
70


B1L100S, U5-ch85, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 81
Mean 36.7
Std Dev 3.643
Gaus mean : 36.8669
Gaus Width: 3.5223
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch85, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 43.77
Std Dev 3.306
Gaus mean : 44.4378
Gaus Width: 4.0270
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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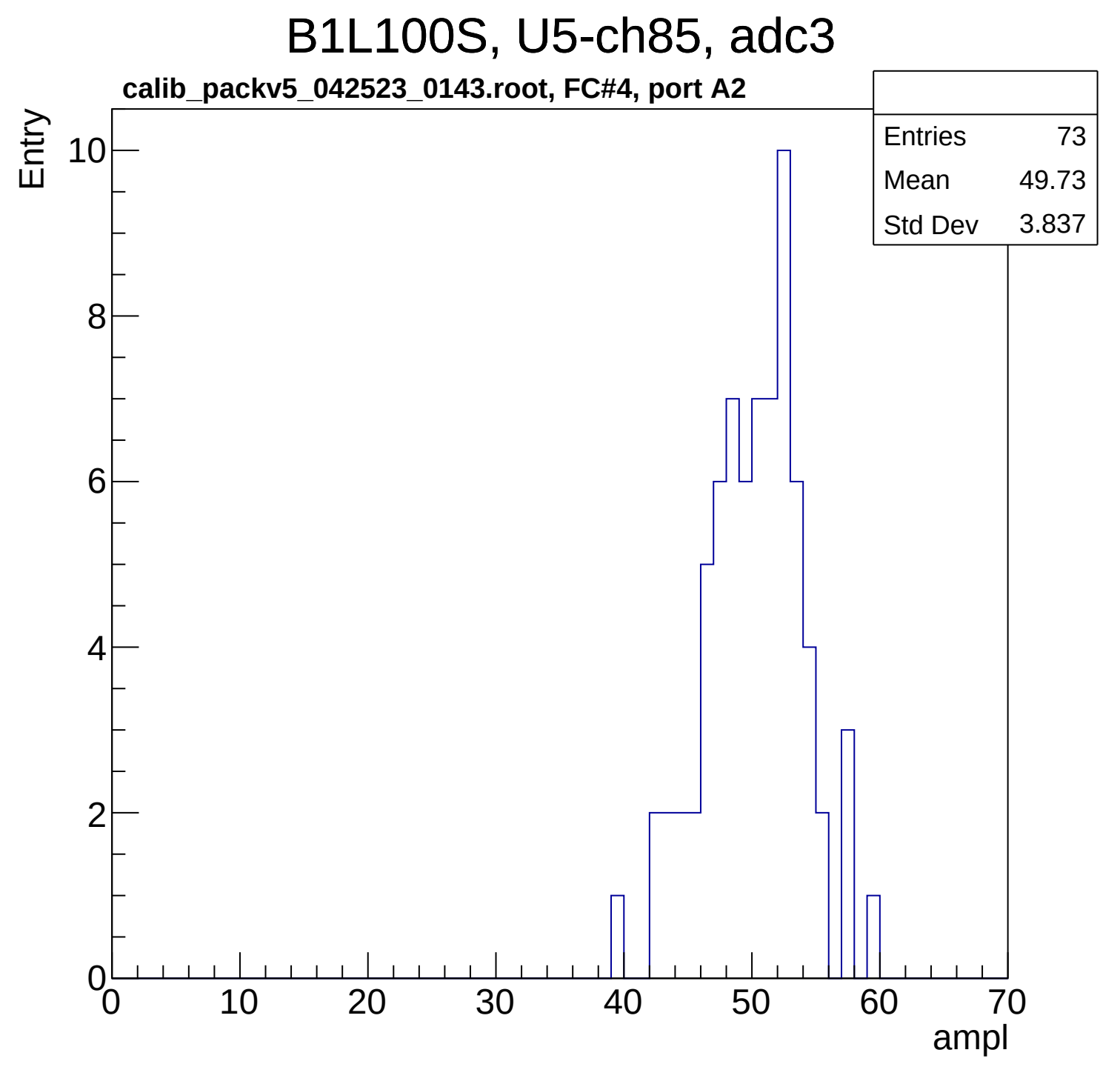
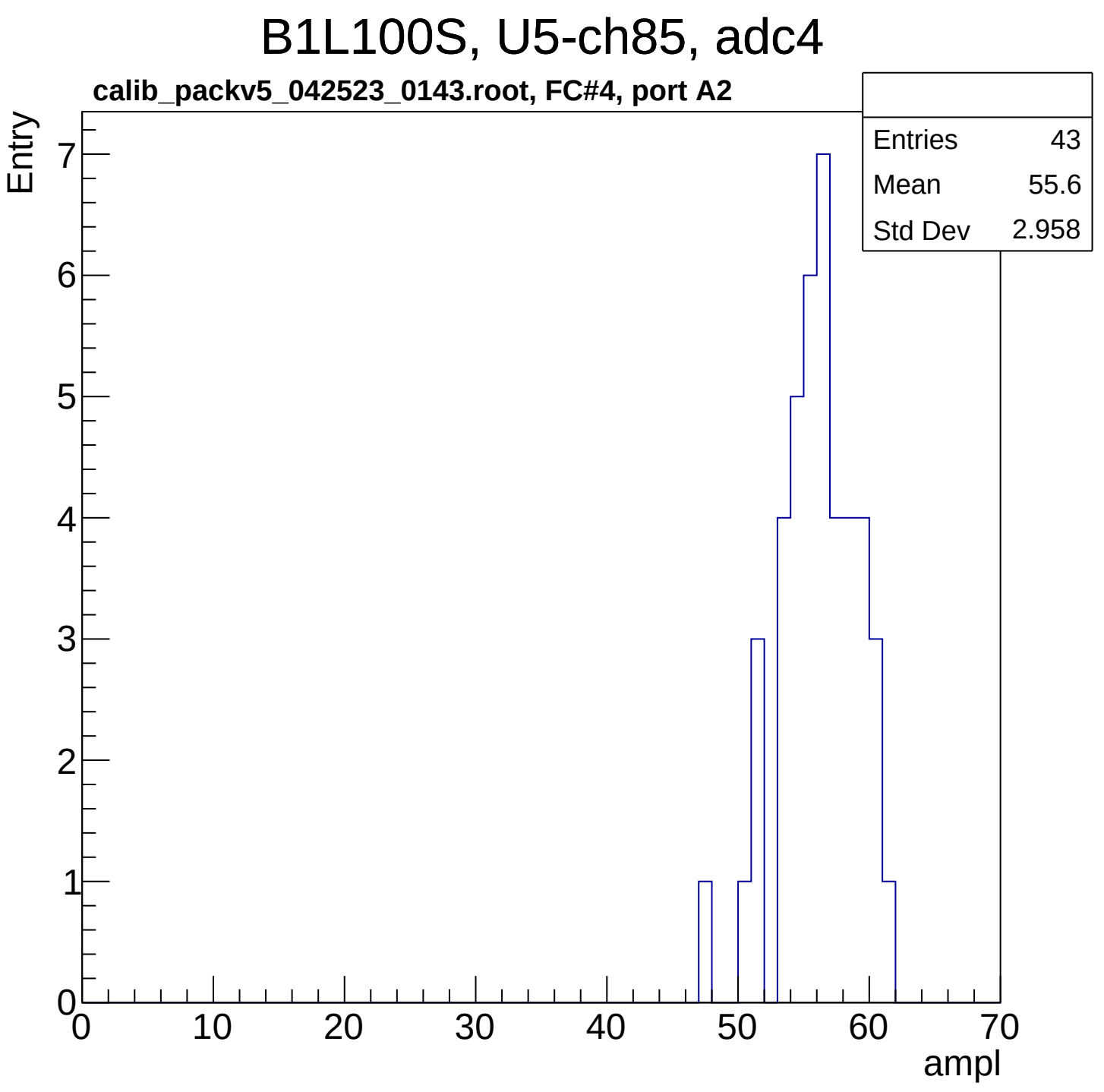
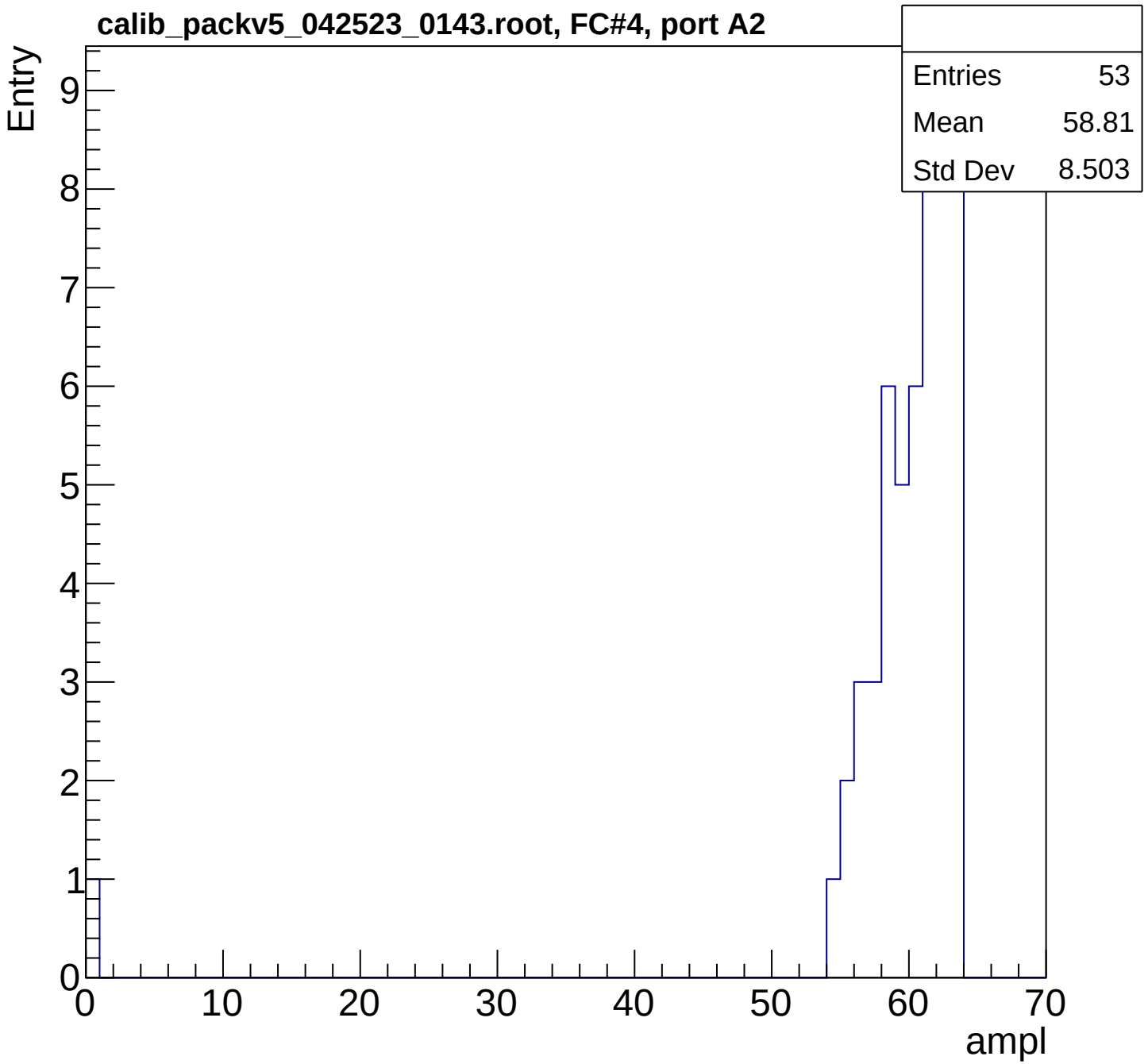

B1L100S, U5-ch85, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 49.73
Std Dev 3.837
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch85, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 43
Mean 55.6
Std Dev 2.958
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U5-ch85, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 58.81
Std Dev 8.503
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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60
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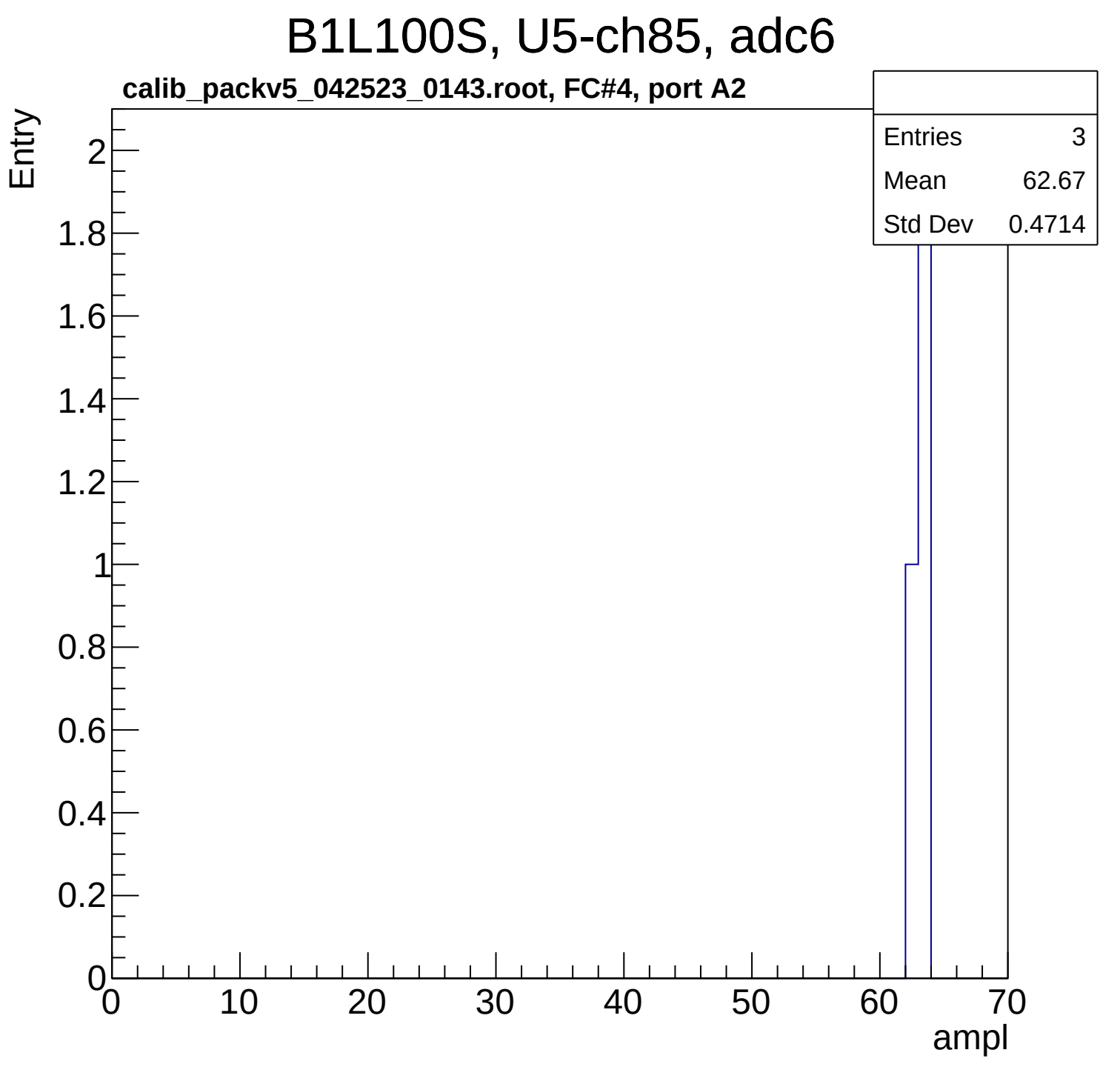
B1L100S, U5-ch85, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 62.67
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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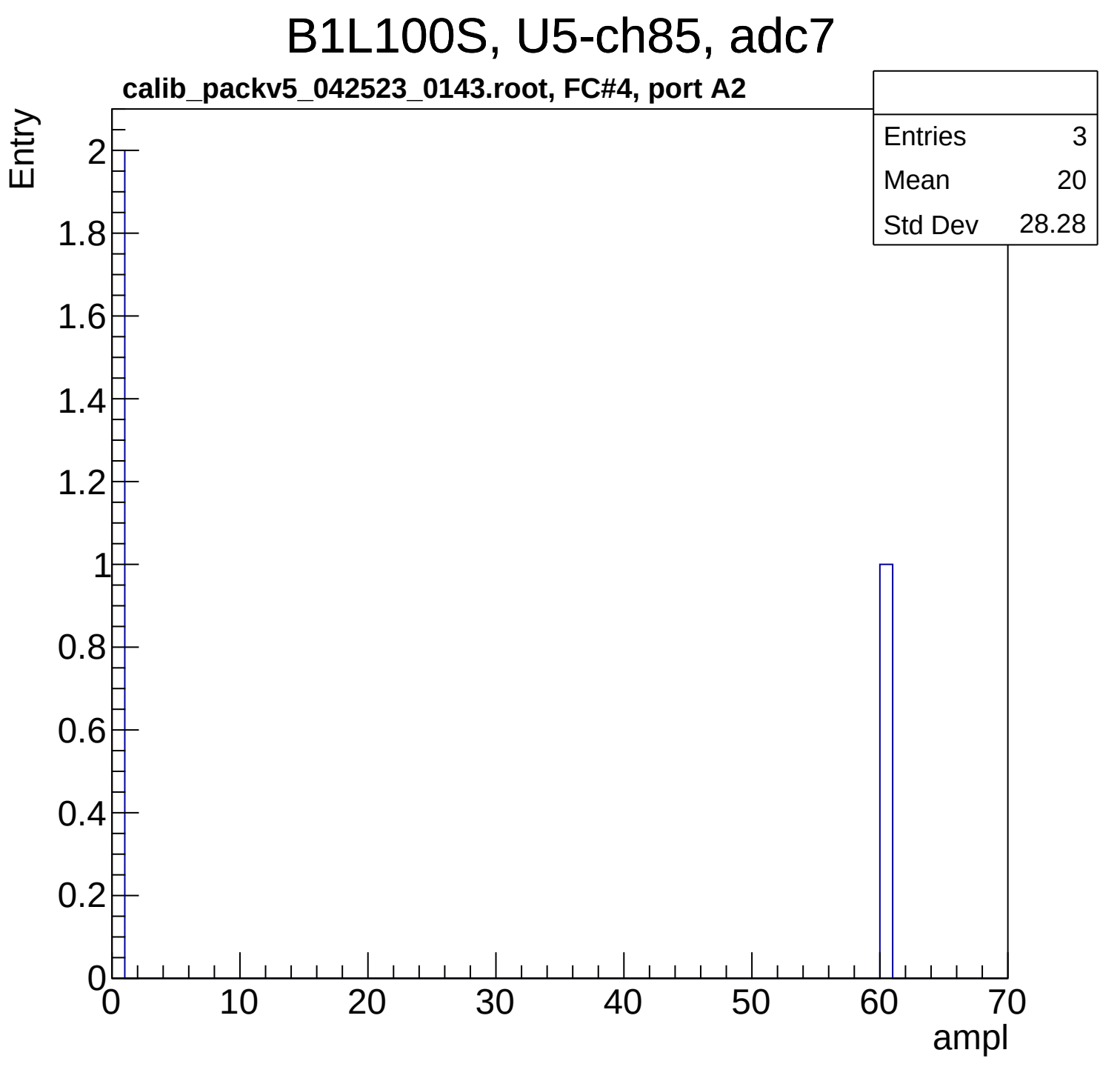
30
40
50
60
70


B1L100S, U5-ch85, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 20
Std Dev 28.28
Entry
ampl
0
0.2
0.4
0.6
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1
1.2
1.4
1.6
1.8
2
0
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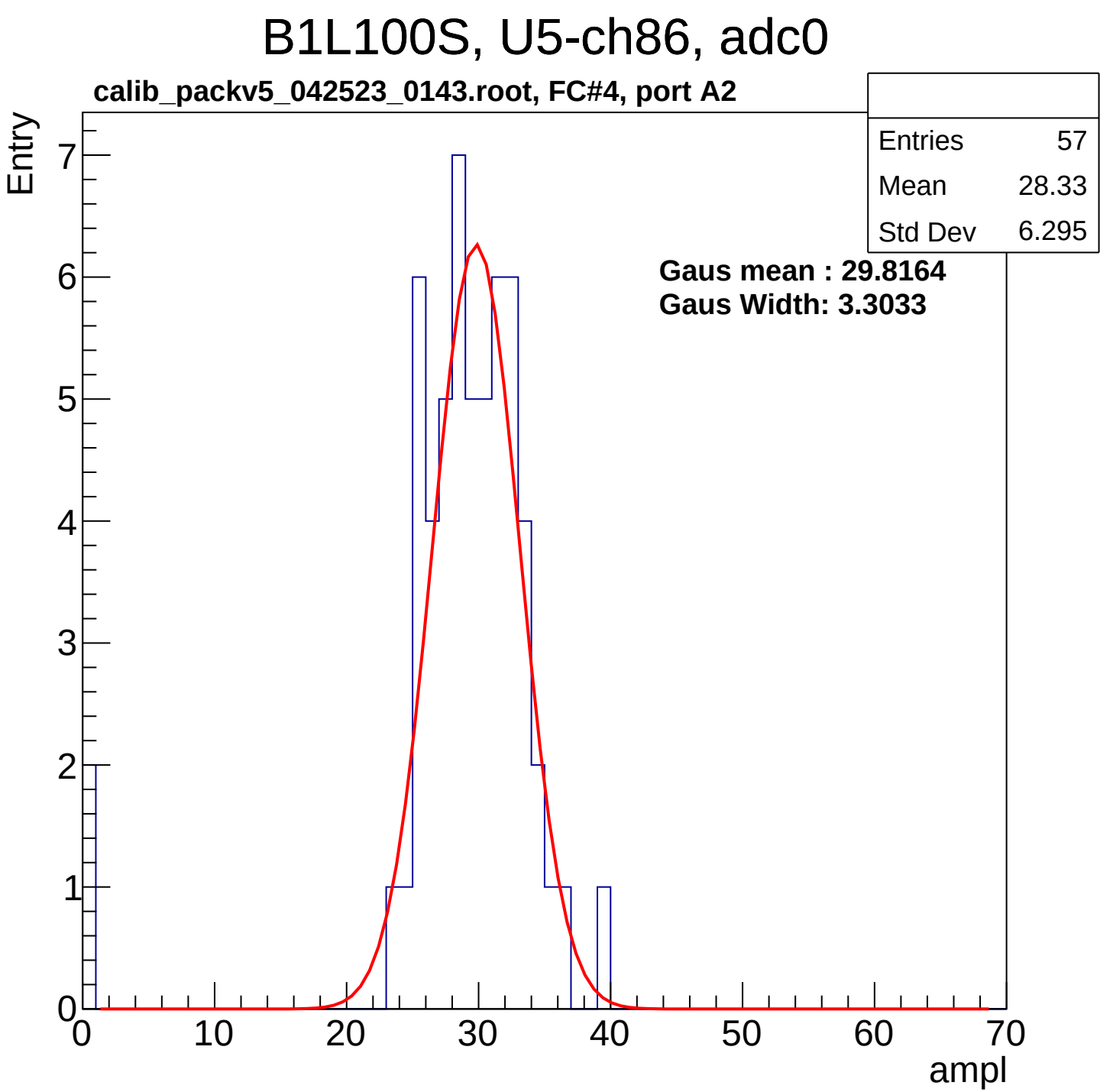
20
30
40
50
60
70


B1L100S, U5-ch86, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 28.33
Std Dev 6.295
Gaus mean : 29.8164
Gaus Width: 3.3033
Entry
ampl
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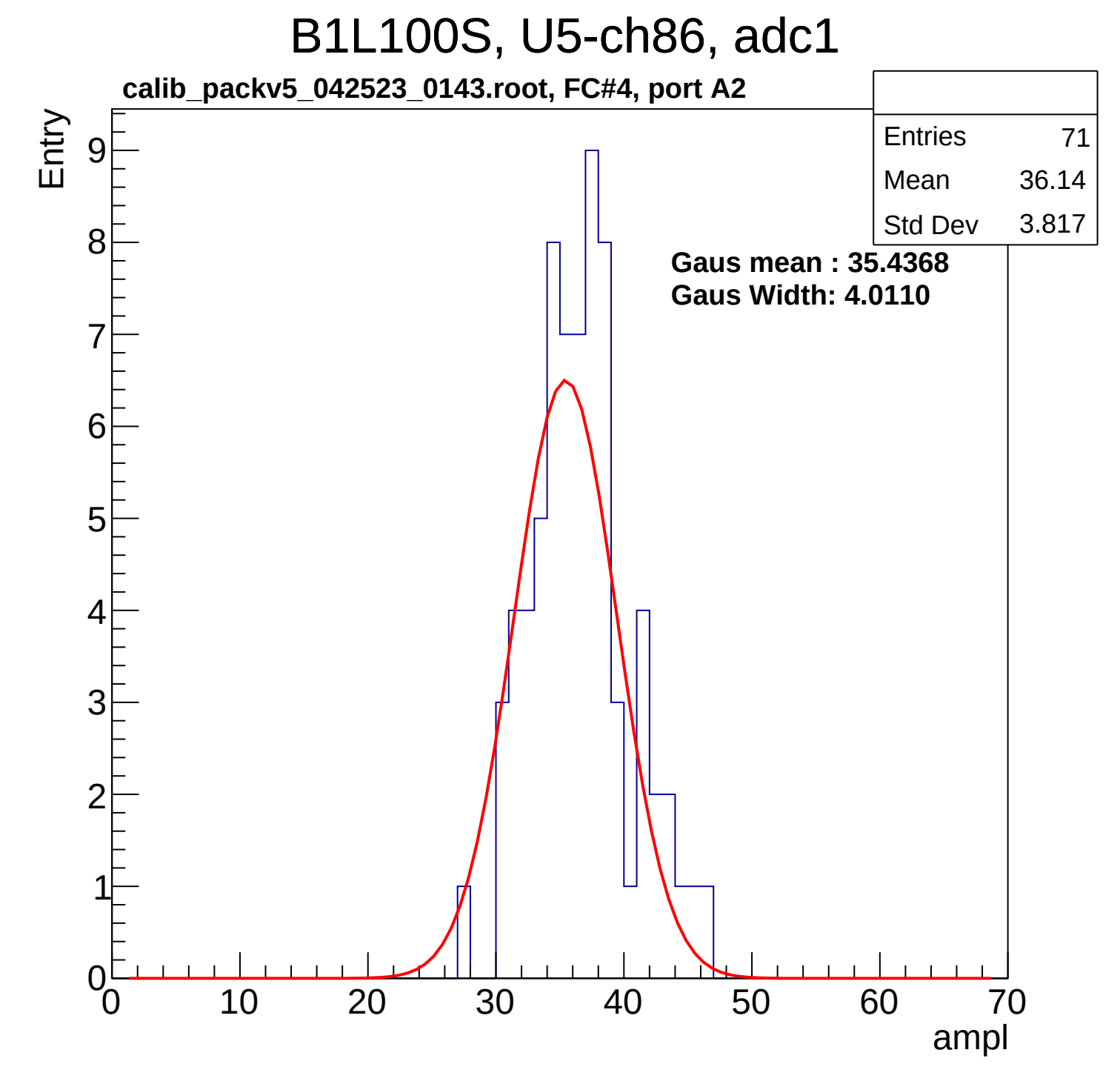
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U5-ch86, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 36.14
Std Dev 3.817
Gaus mean : 35.4368
Gaus Width: 4.0110
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
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30
40
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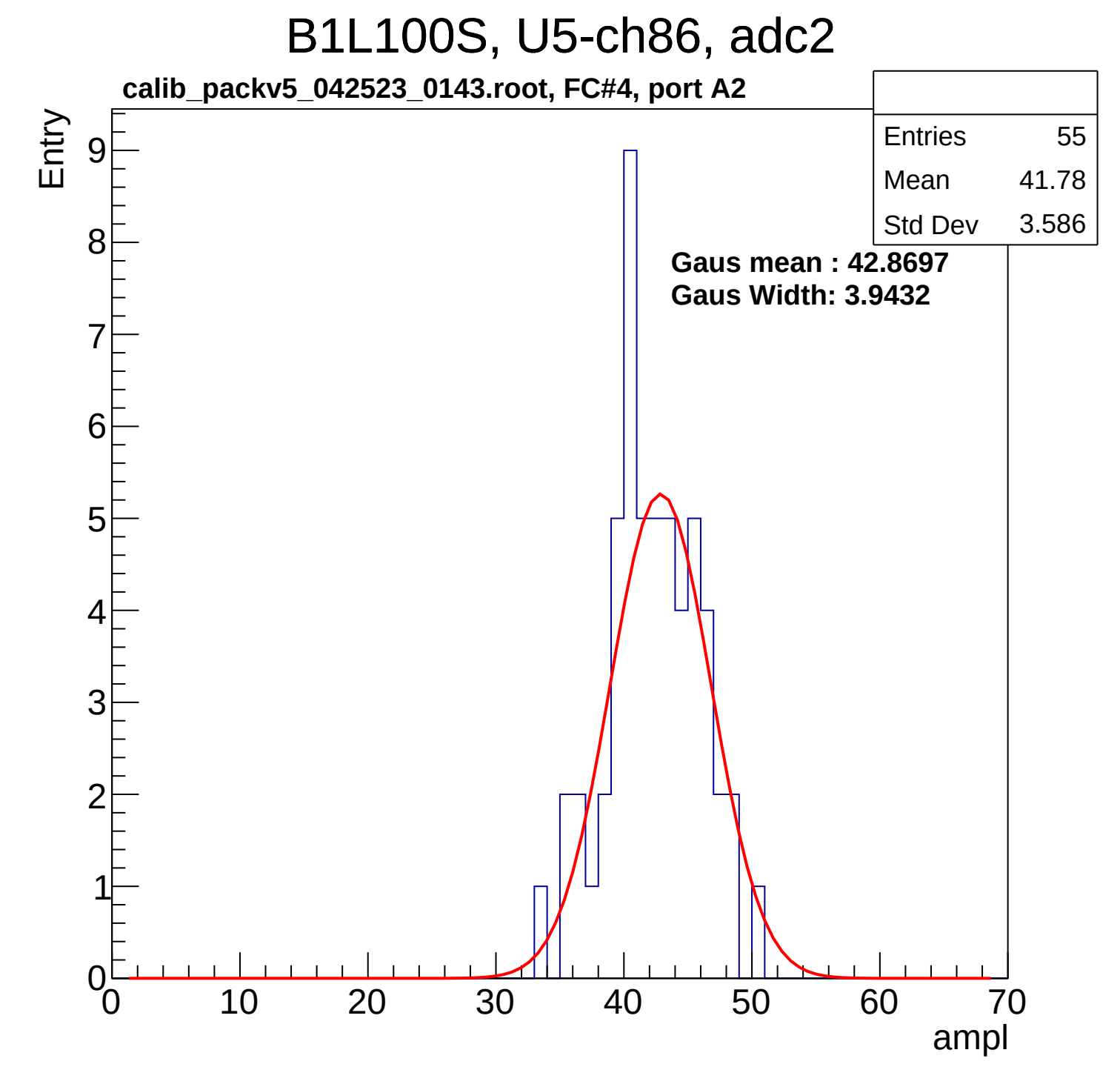
B1L100S, U5-ch86, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 41.78
Std Dev 3.586
Gaus mean : 42.8697
Gaus Width: 3.9432
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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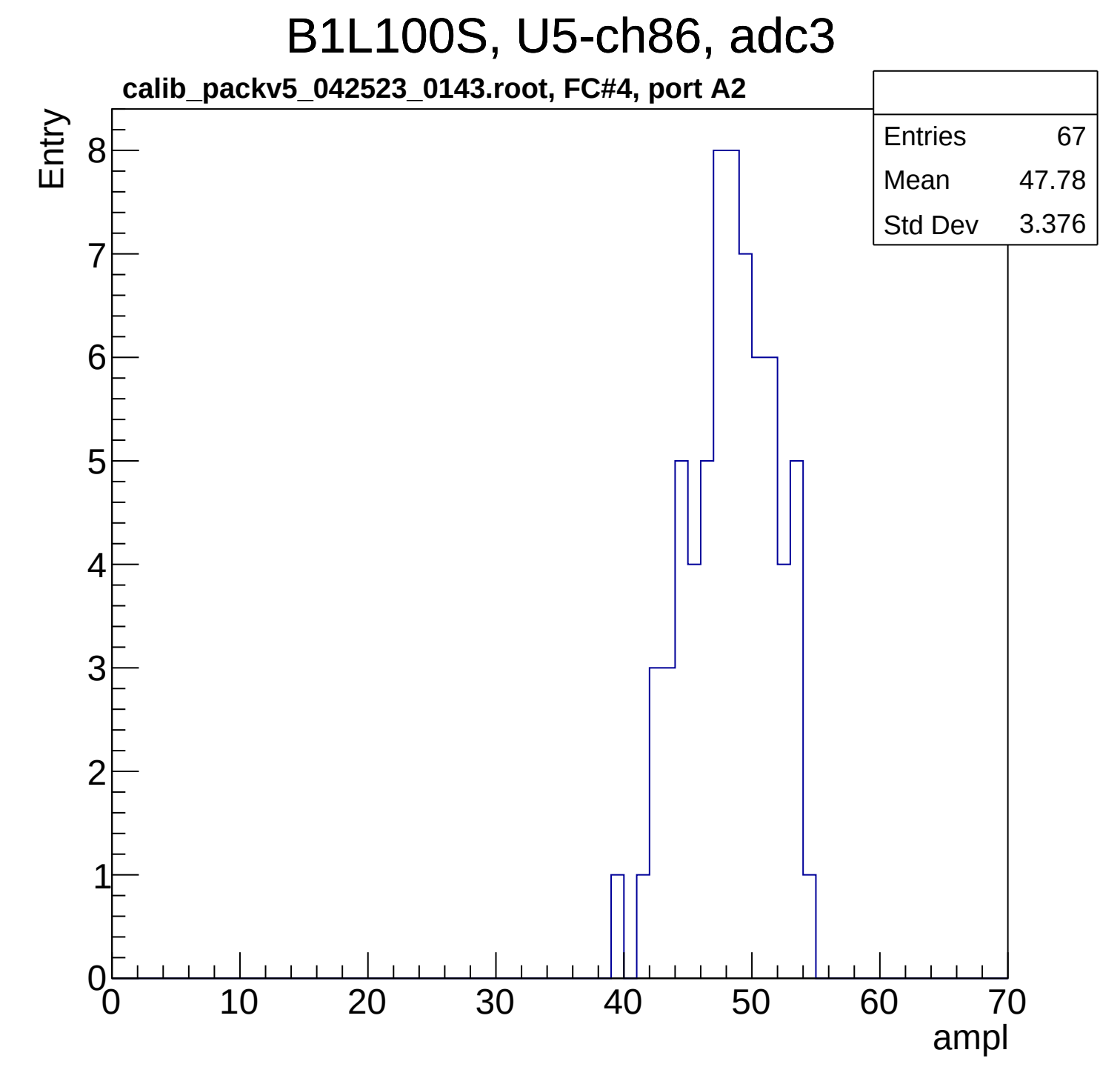
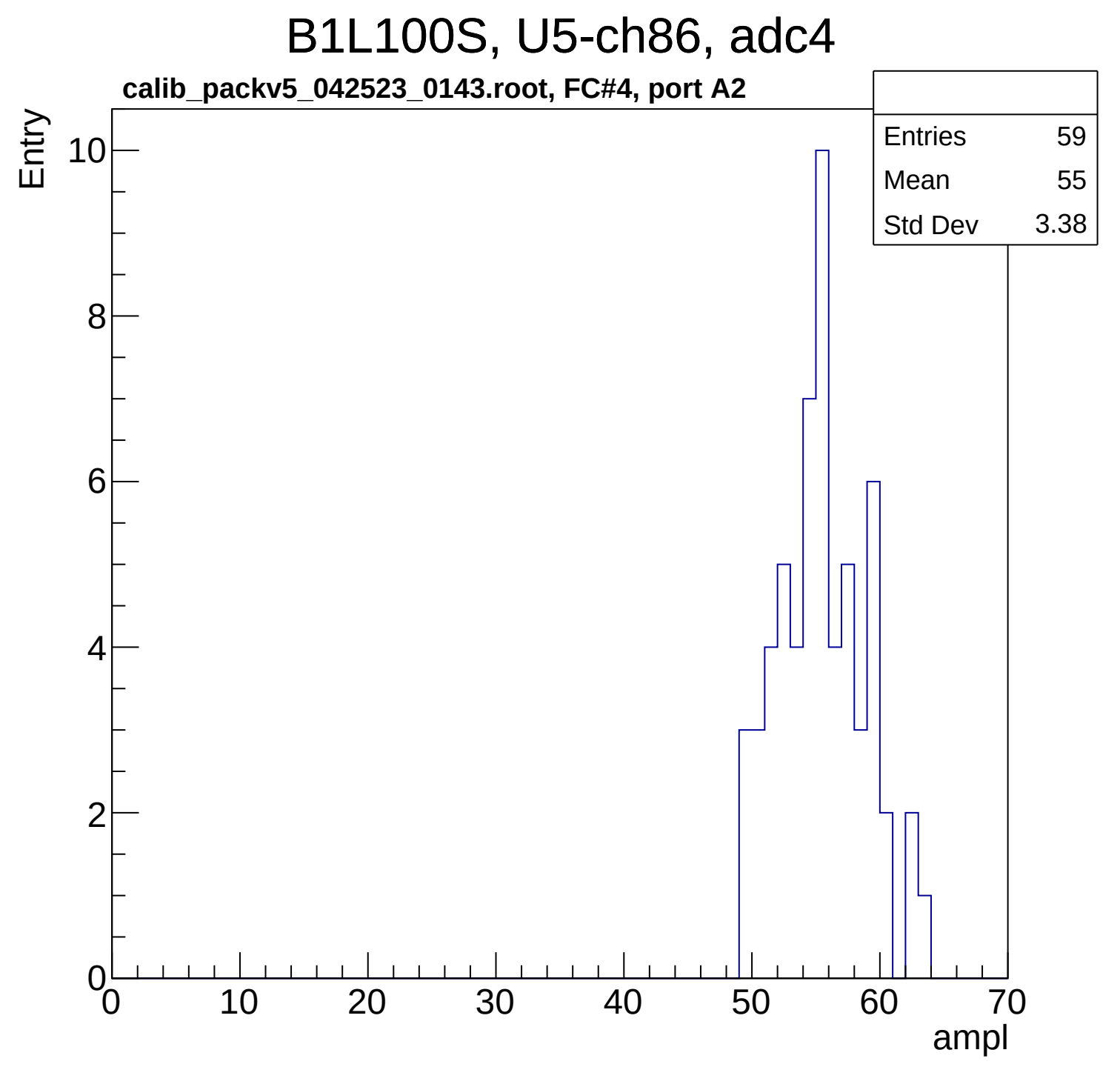
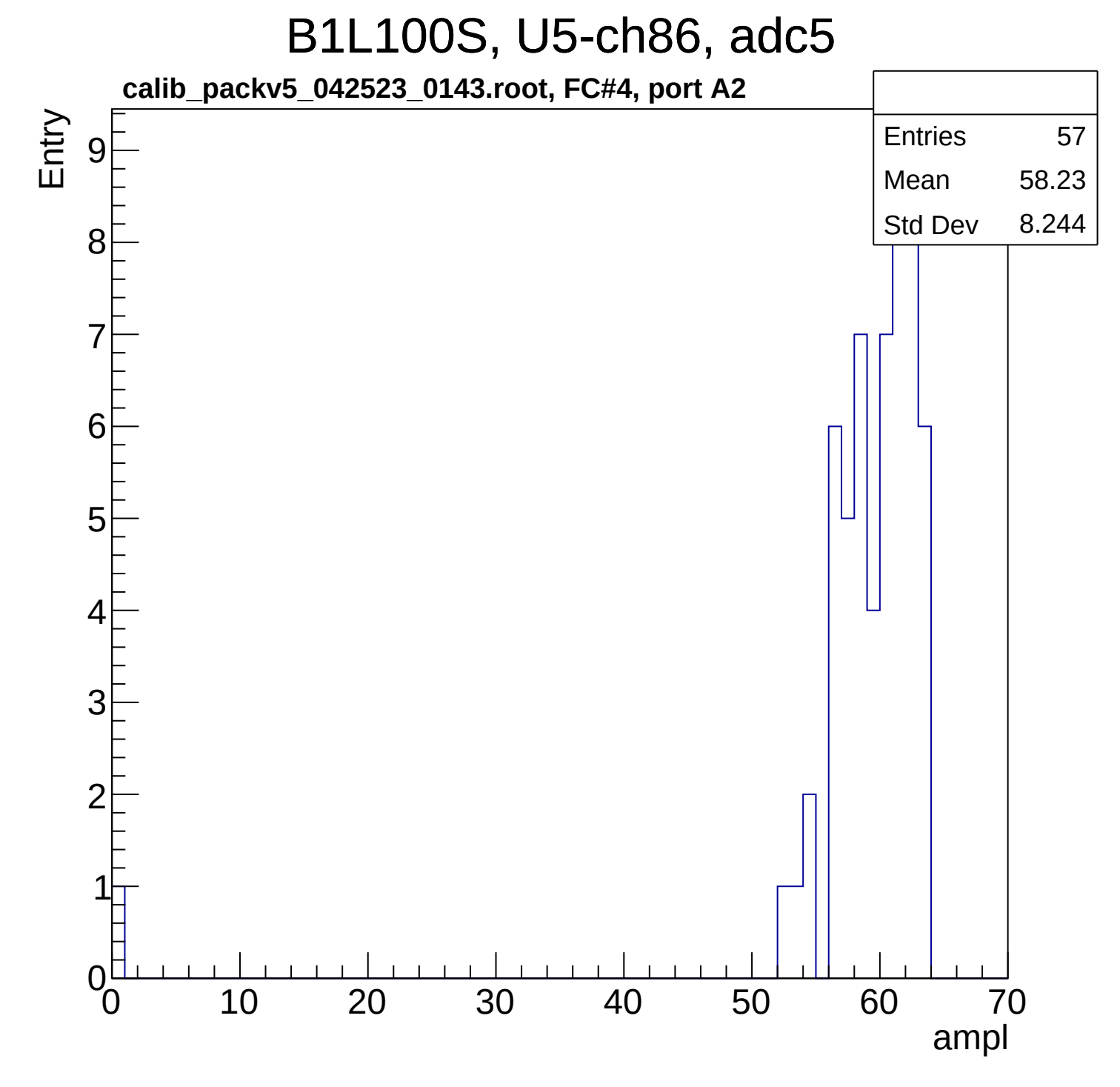

B1L100S, U5-ch86, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 47.78
Std Dev 3.376
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch86, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 55
Std Dev 3.38
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch86, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 58.23
Std Dev 8.244
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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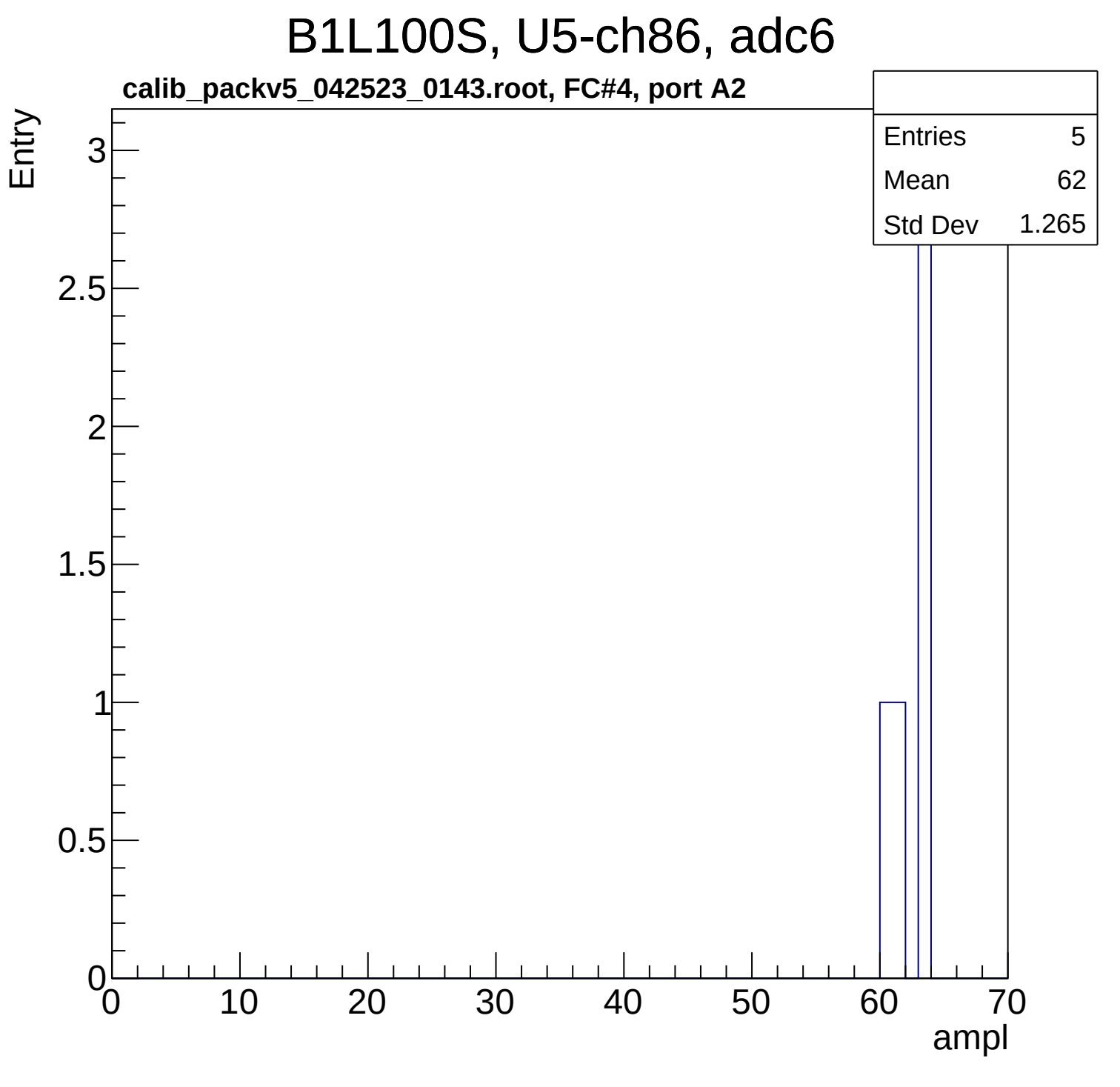
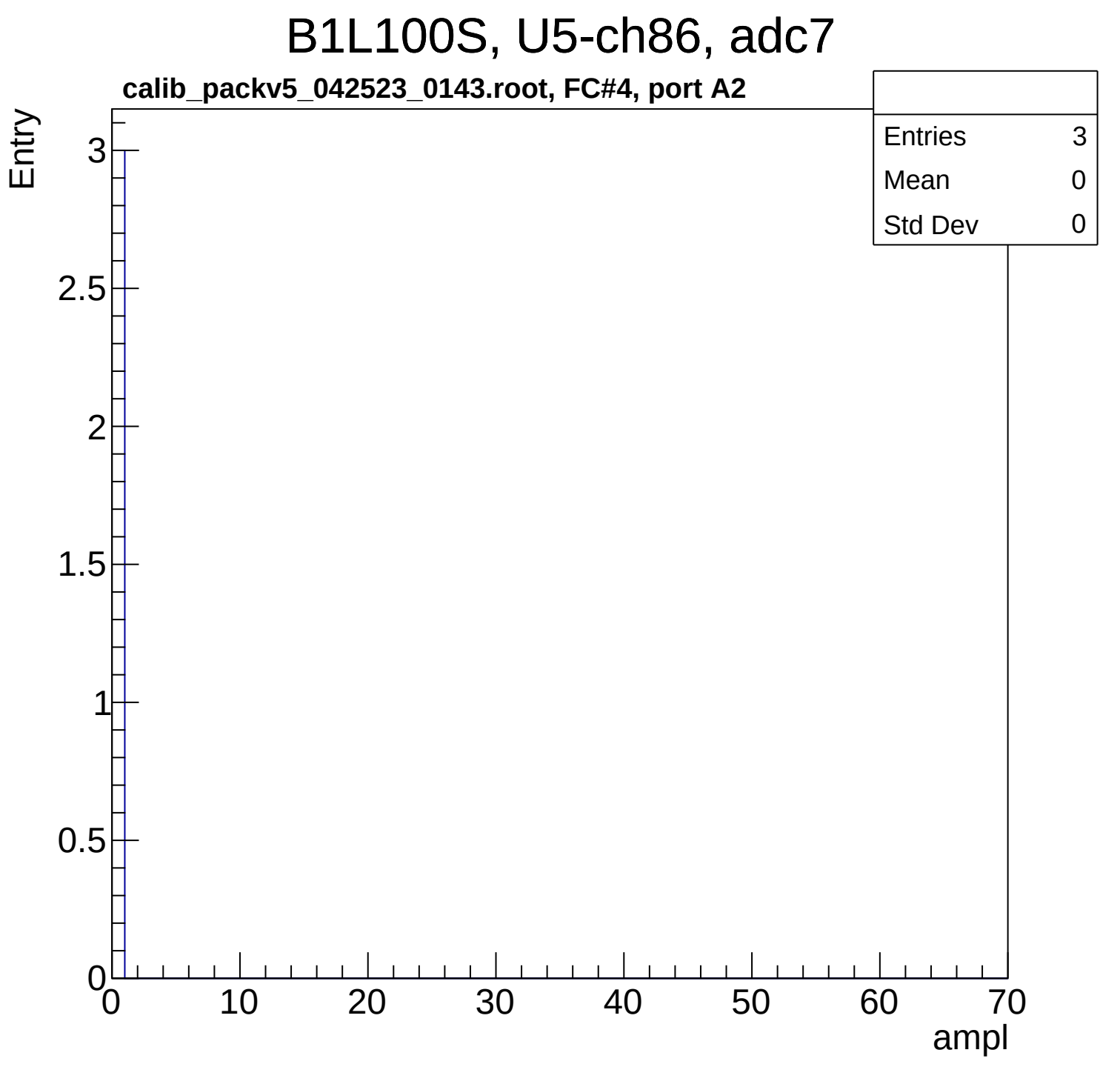
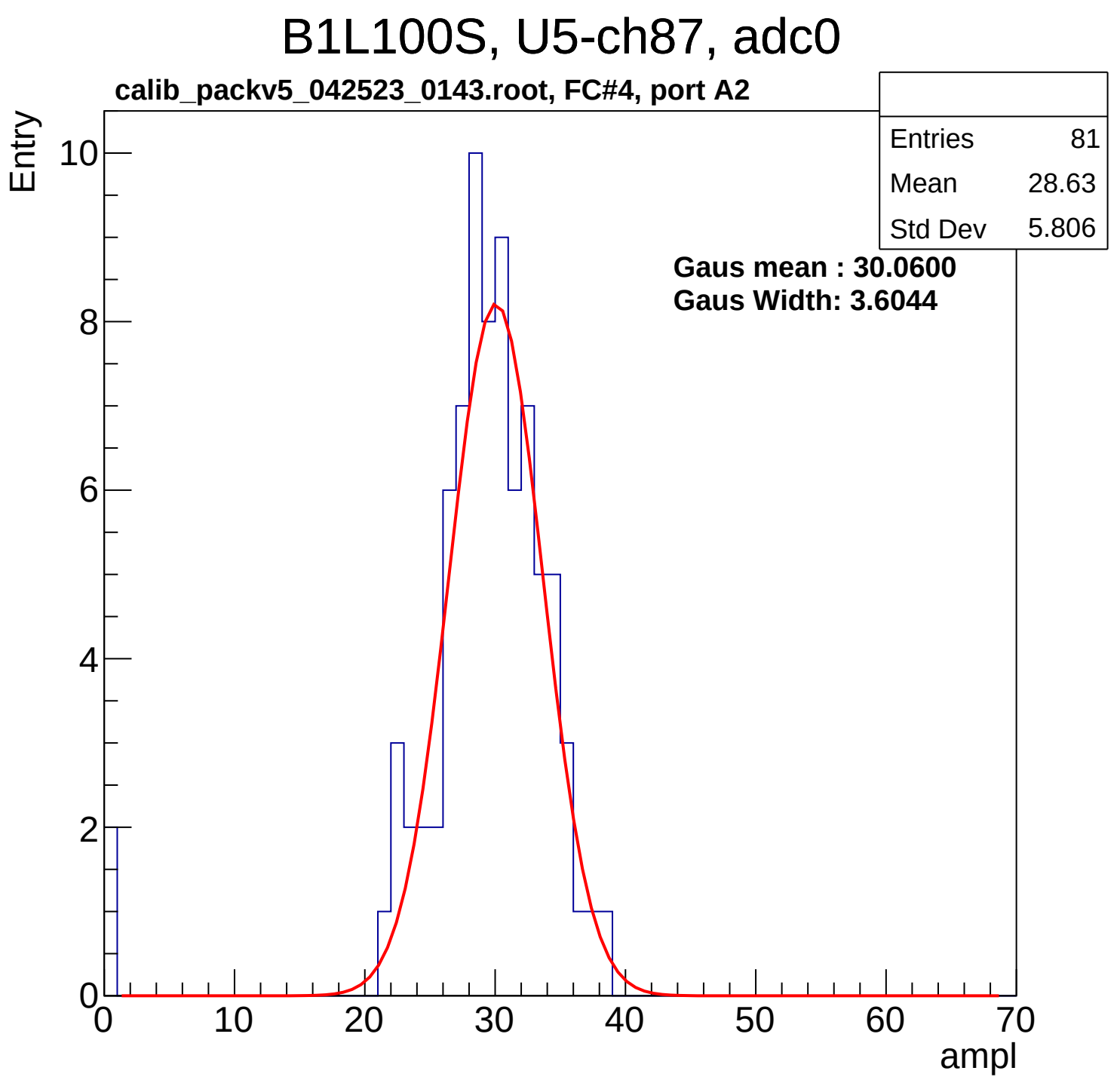
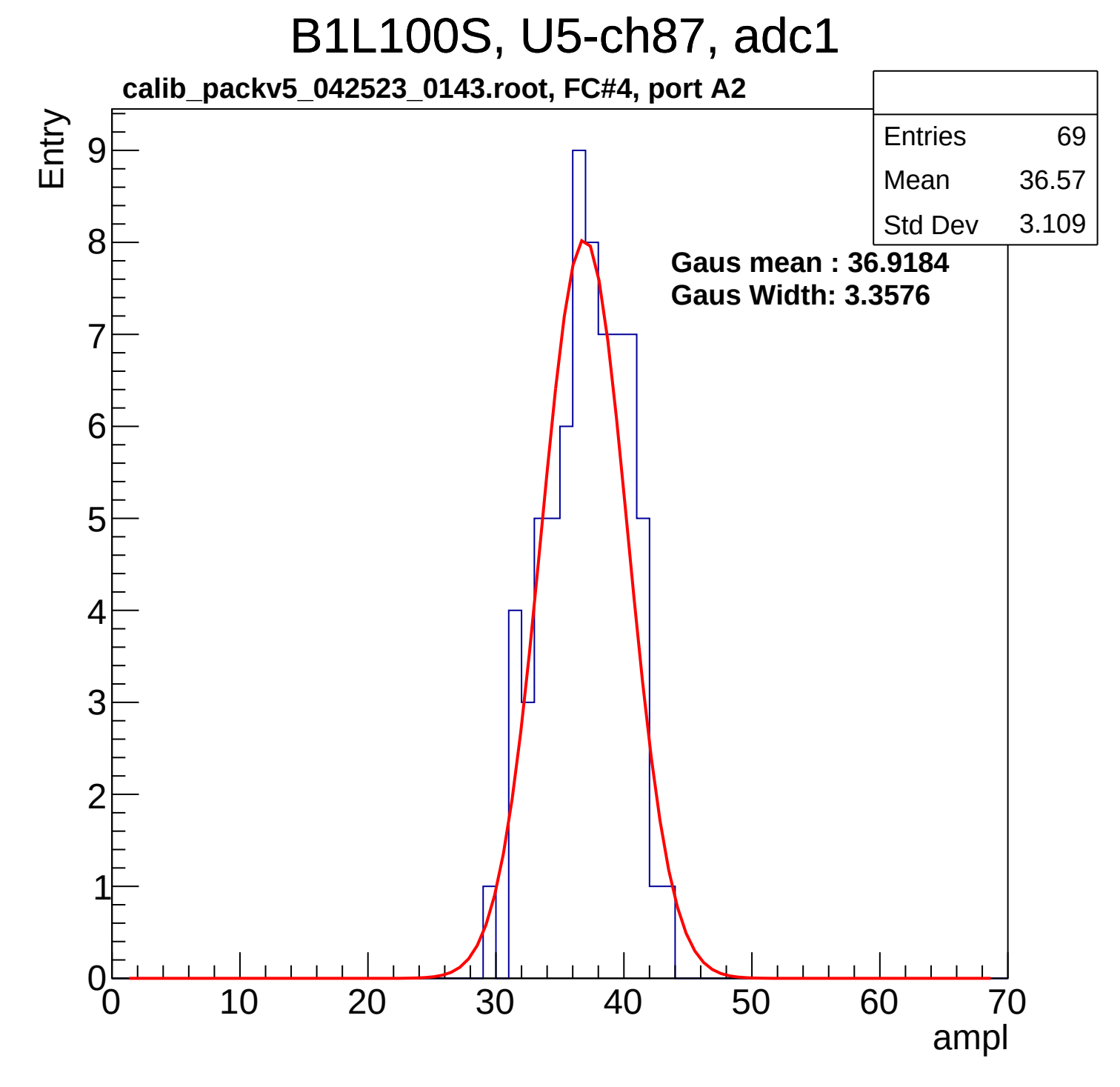
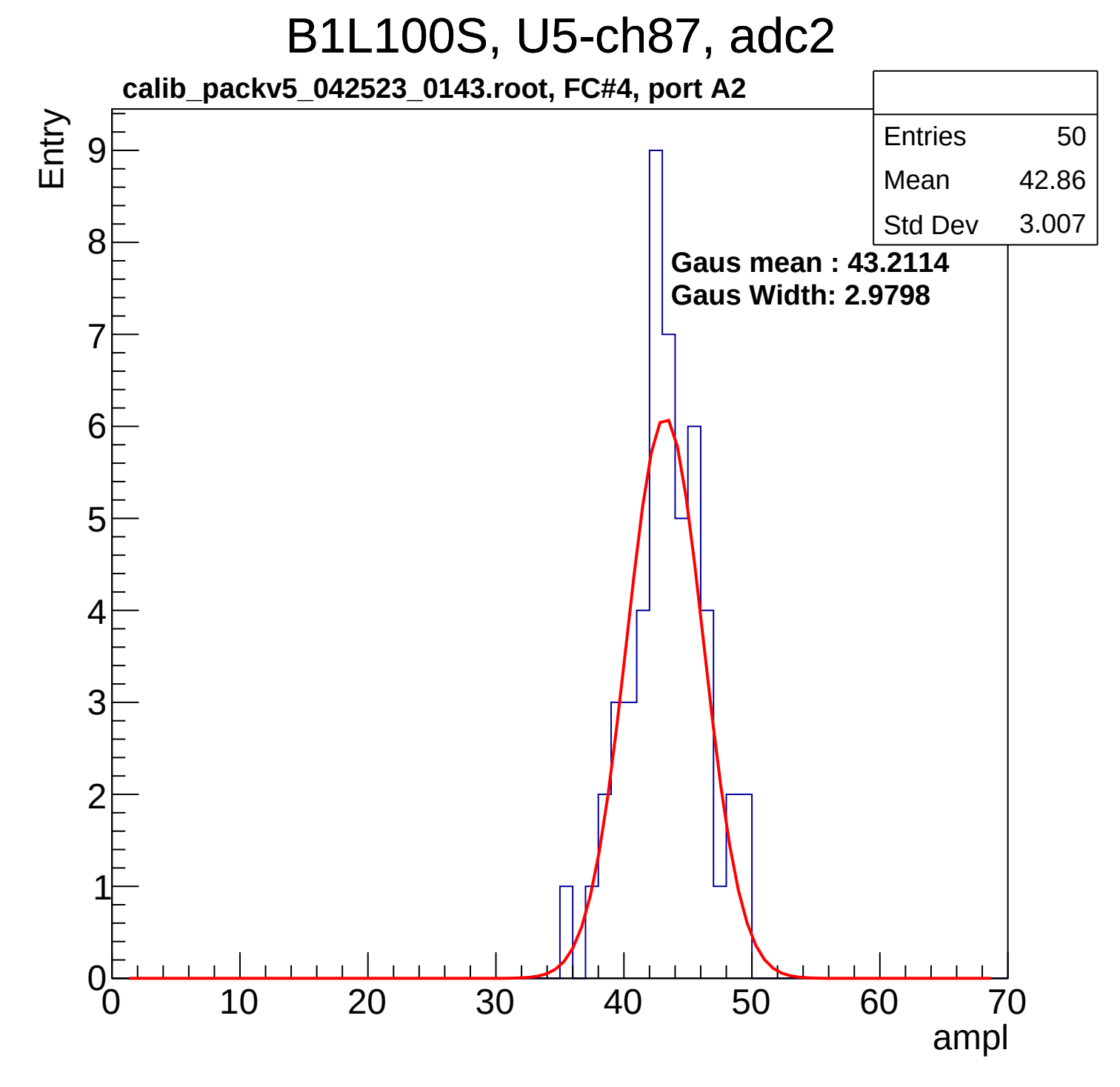
40
50
60
70

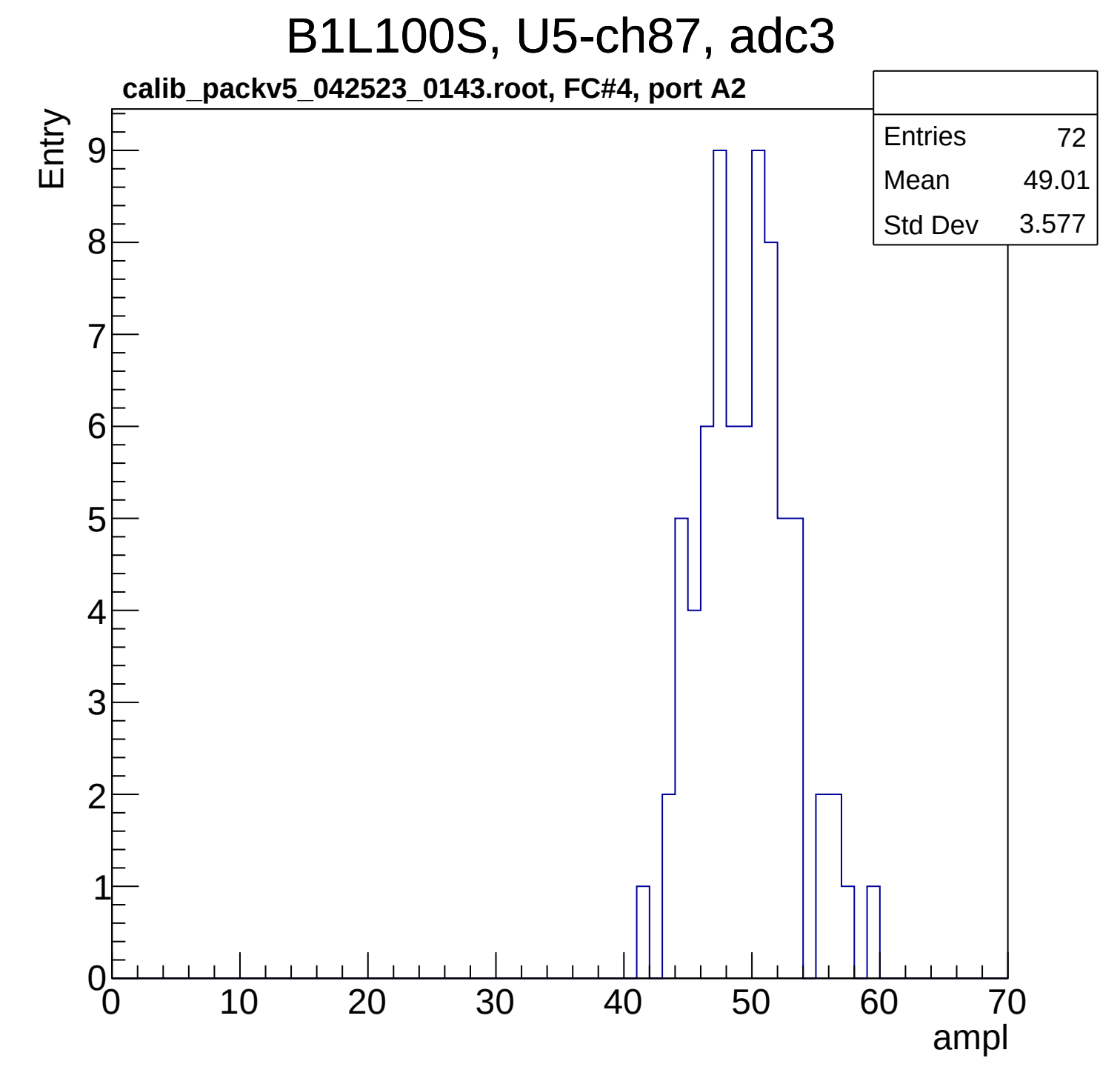

B1L100S, U5-ch86, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 5
Mean 62
Std Dev 1.265
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

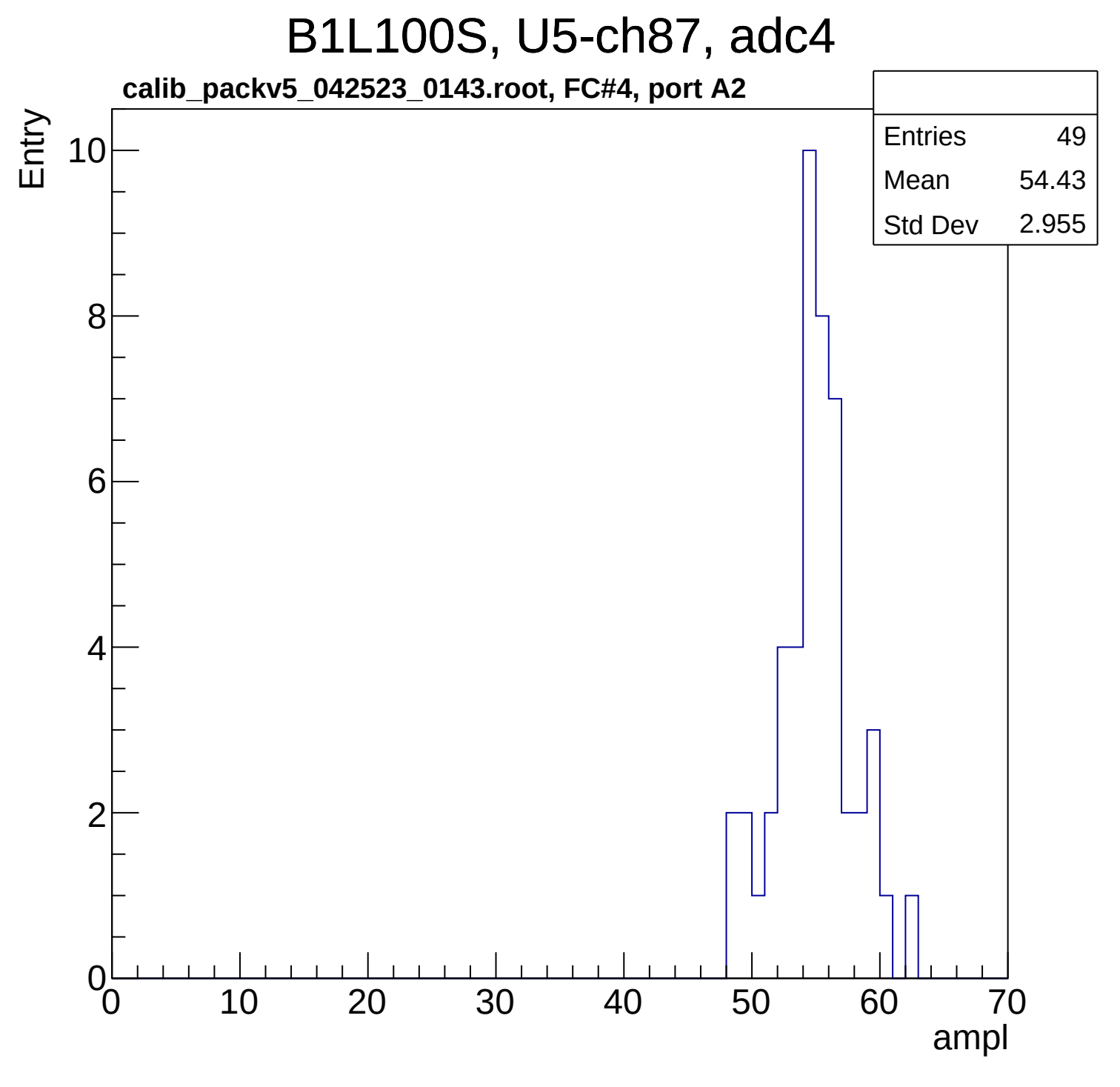

B1L100S, U5-ch86, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 0
Std Dev 0
Entry
3
2.5
2
1.5
1
0.5
0
0
10
20
30
40
50
60
70
ampl

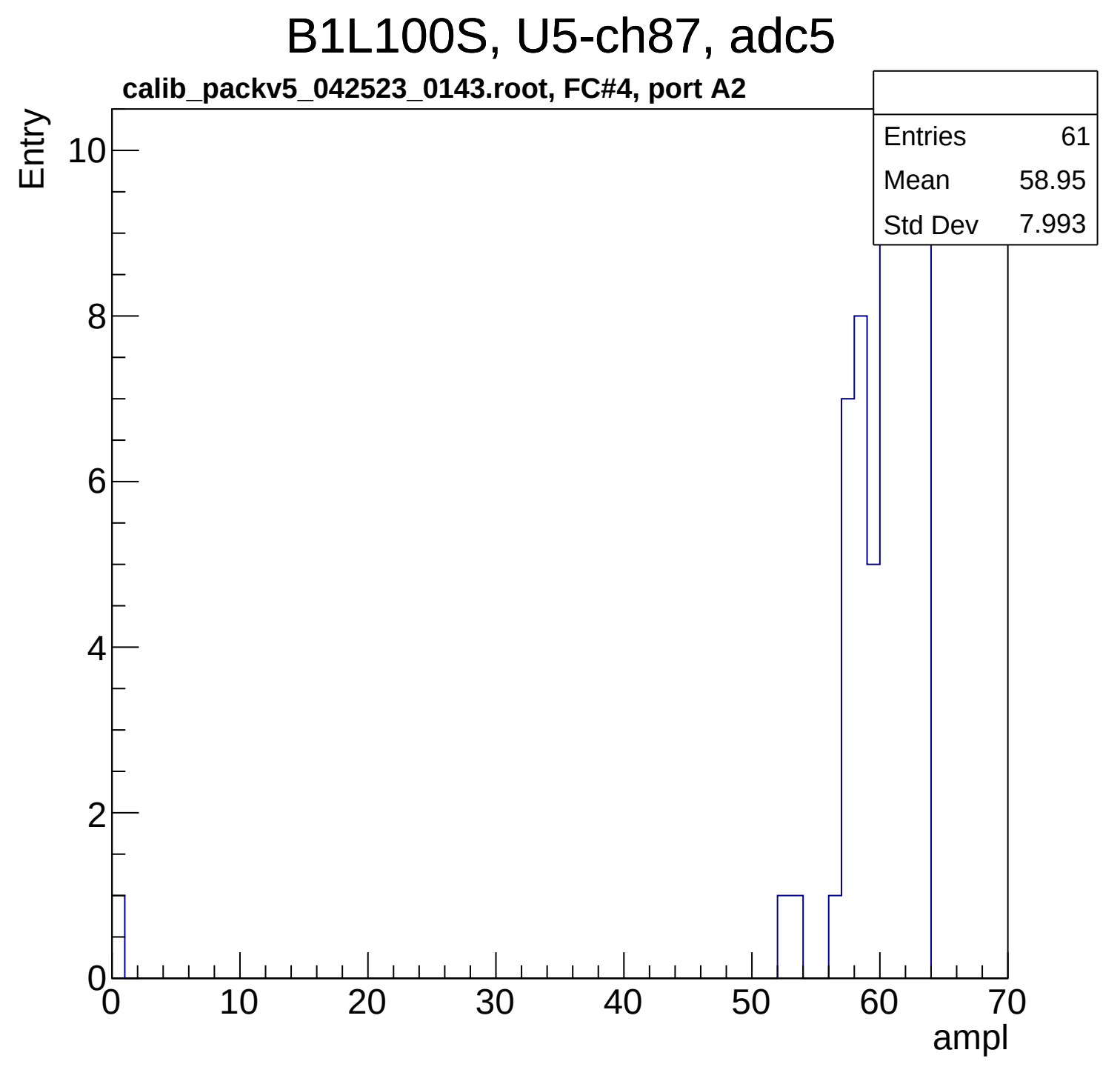

B1L100S, U5-ch87, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 81
Mean 28.63
Std Dev 5.806
Gaus mean : 30.0600
Gaus Width: 3.6044
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

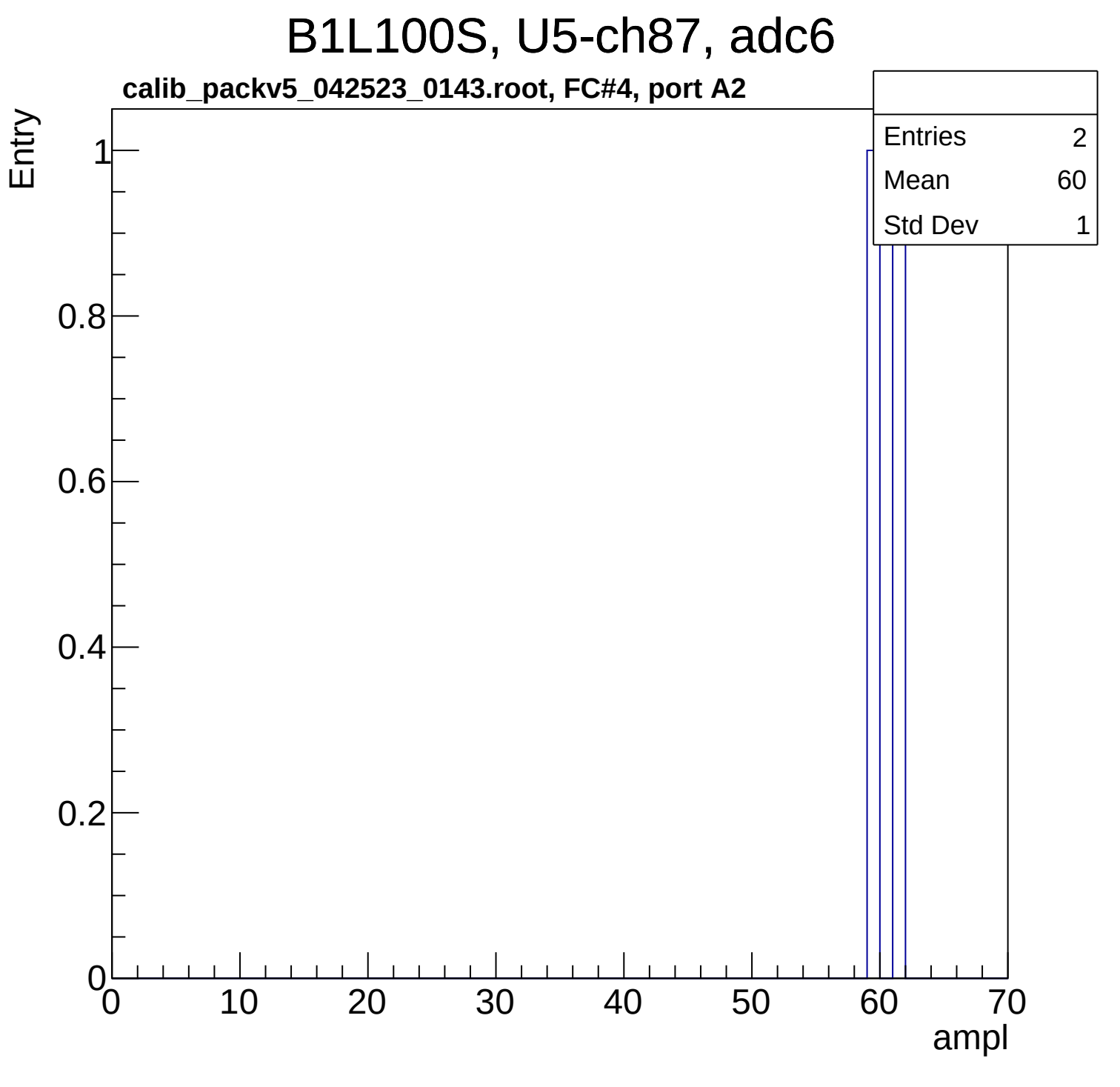

B1L100S, U5-ch87, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 36.57
Std Dev 3.109
Gaus mean : 36.9184
Gaus Width: 3.3576
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9

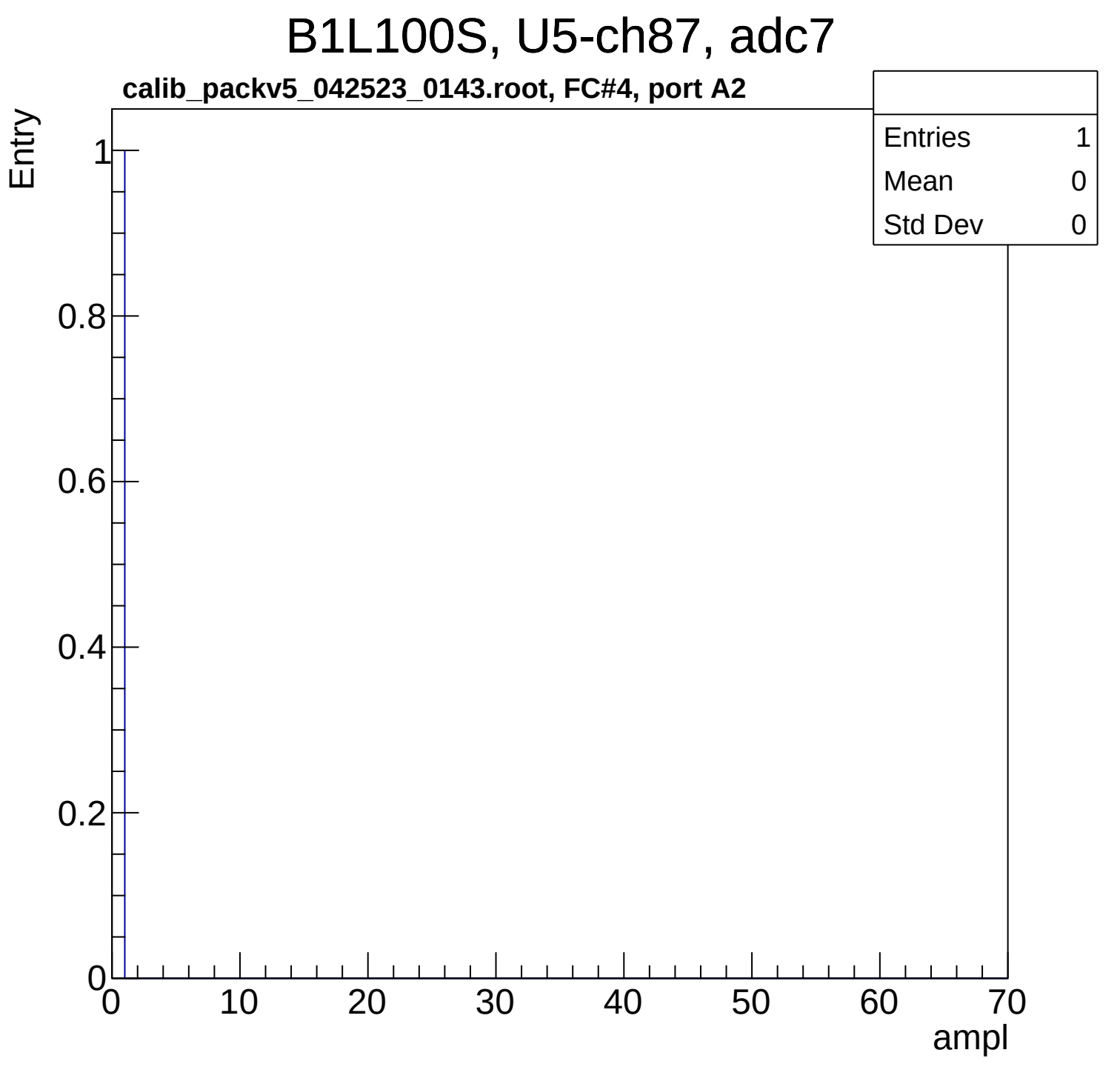

B1L100S, U5-ch87, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 42.86
Std Dev 3.007
Gaus mean : 43.2114
Gaus Width: 2.9798
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

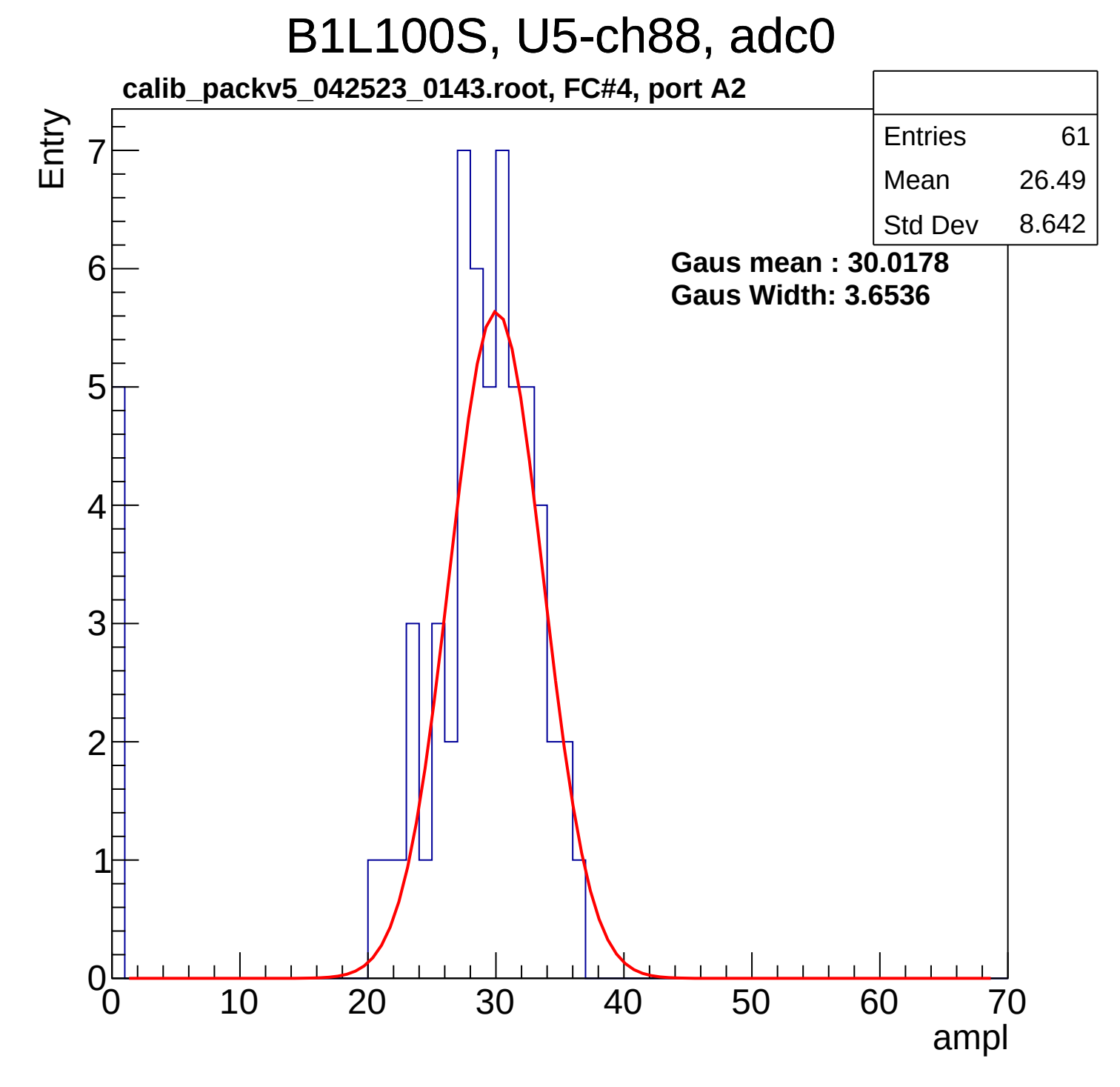

B1L100S, U5-ch87, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 49.01
Std Dev 3.577
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

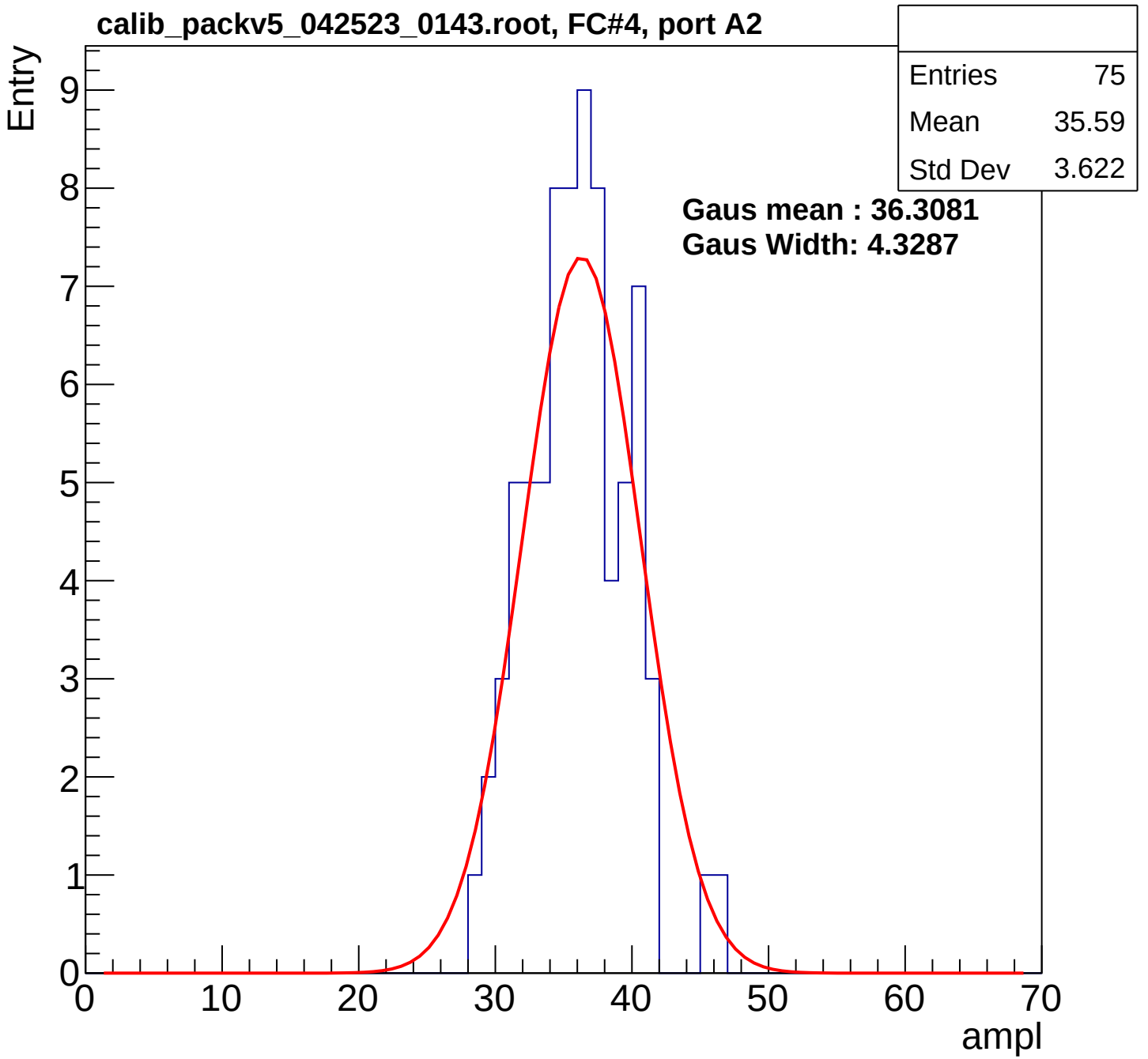

B1L100S, U5-ch87, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 49
Mean 54.43
Std Dev 2.955
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

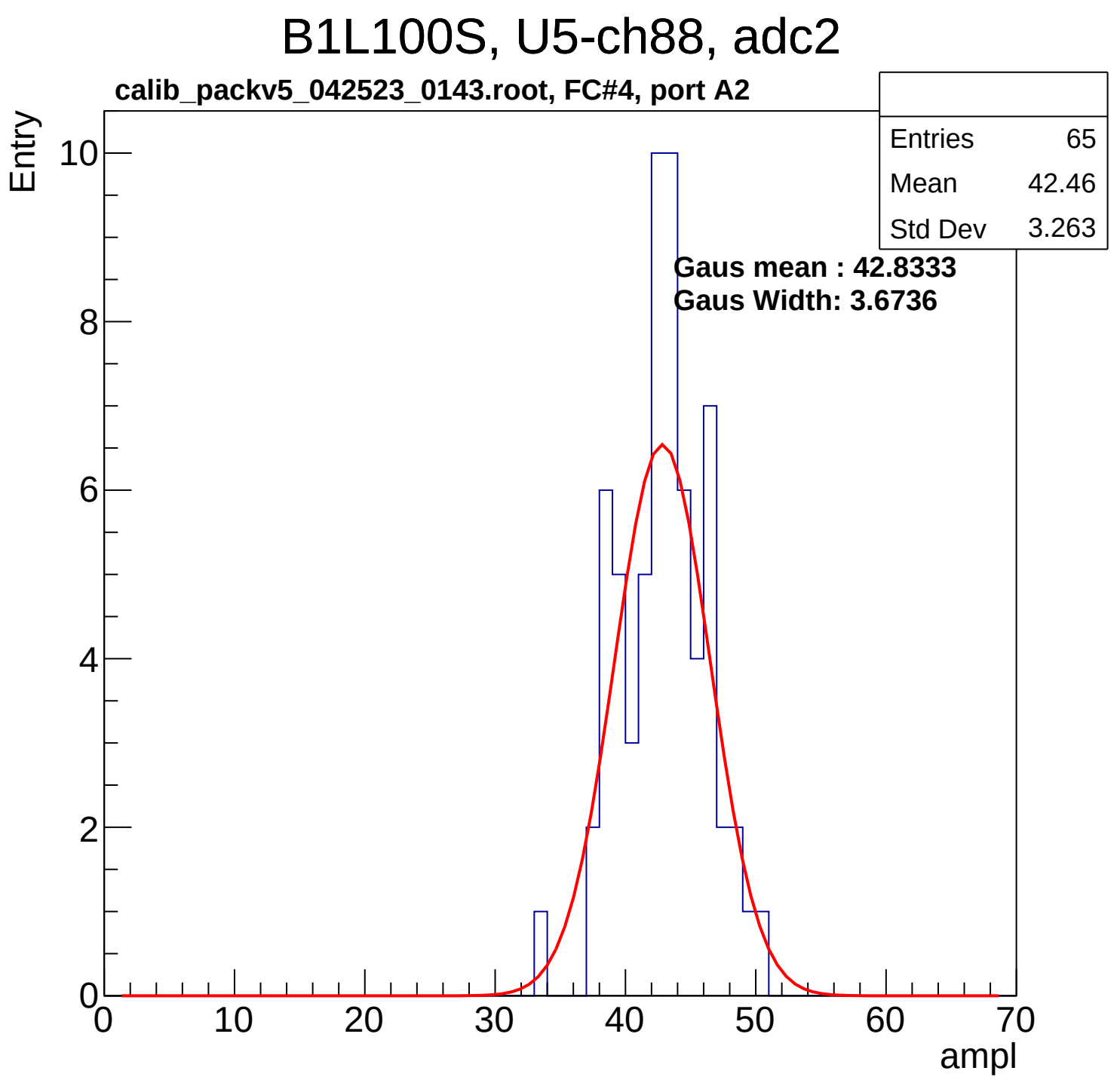

B1L100S, U5-ch87, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 58.95
Std Dev 7.993
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

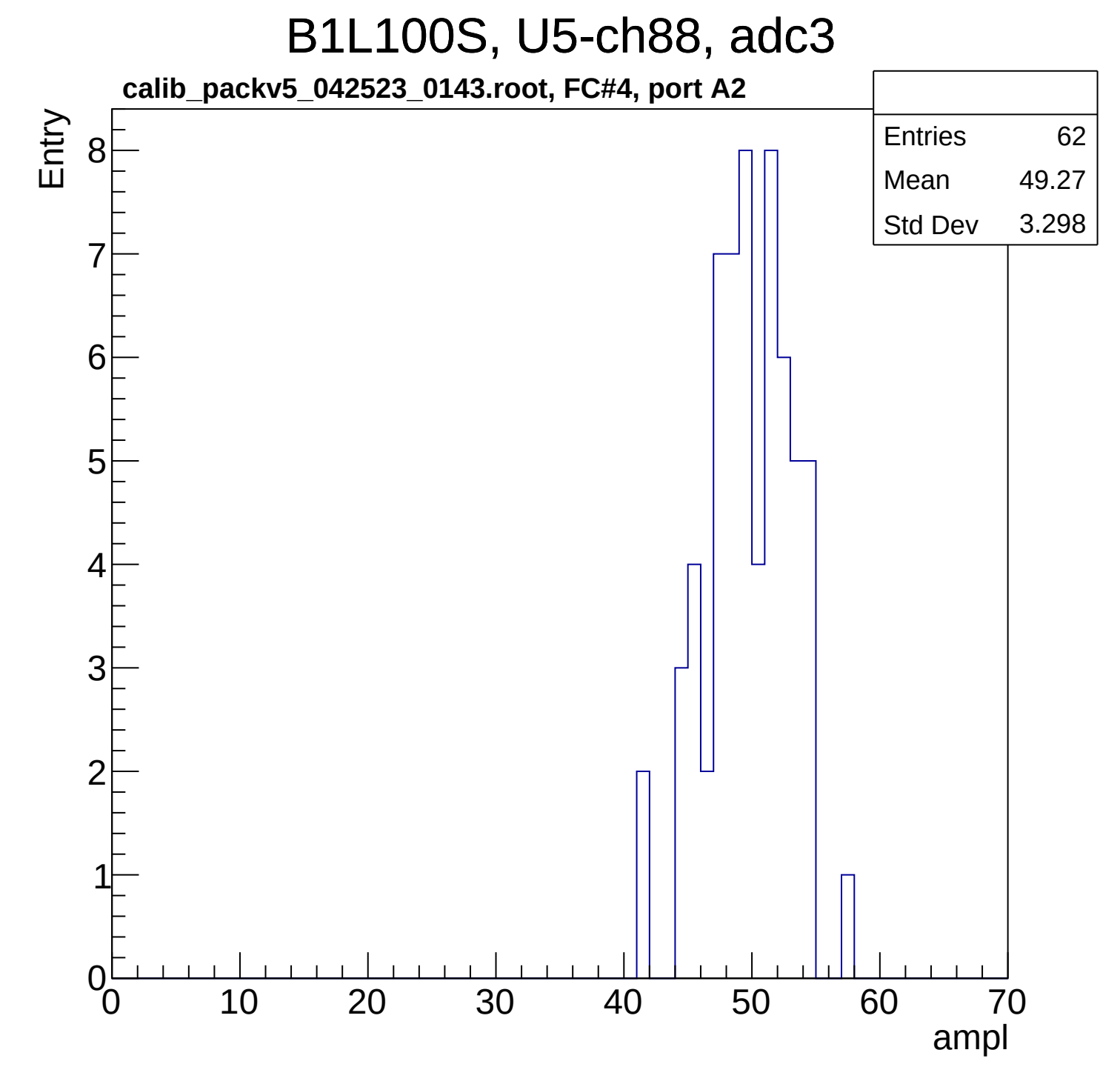

B1L100S, U5-ch87, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 60
Std Dev 1
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

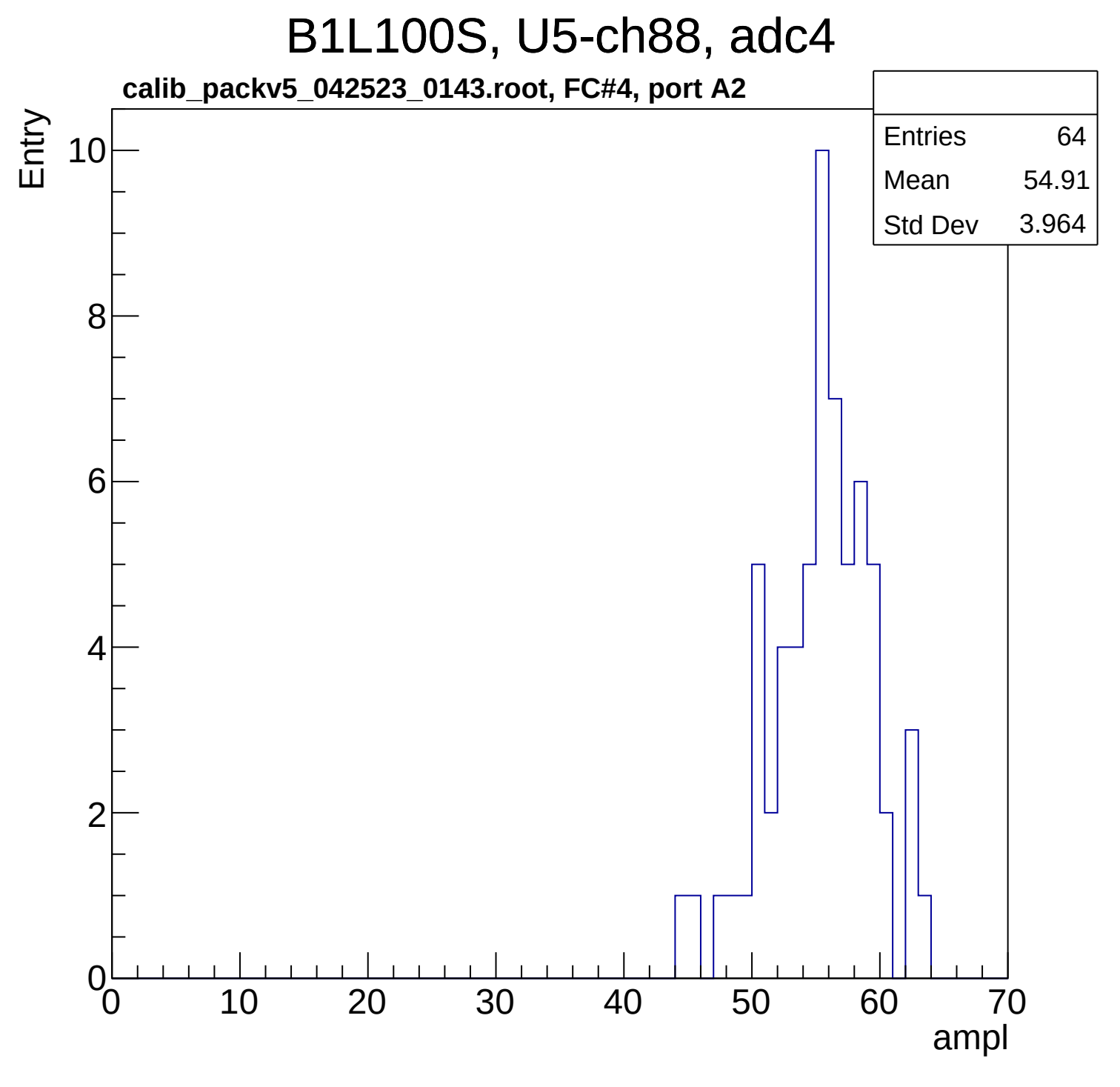

B1L100S, U5-ch87, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

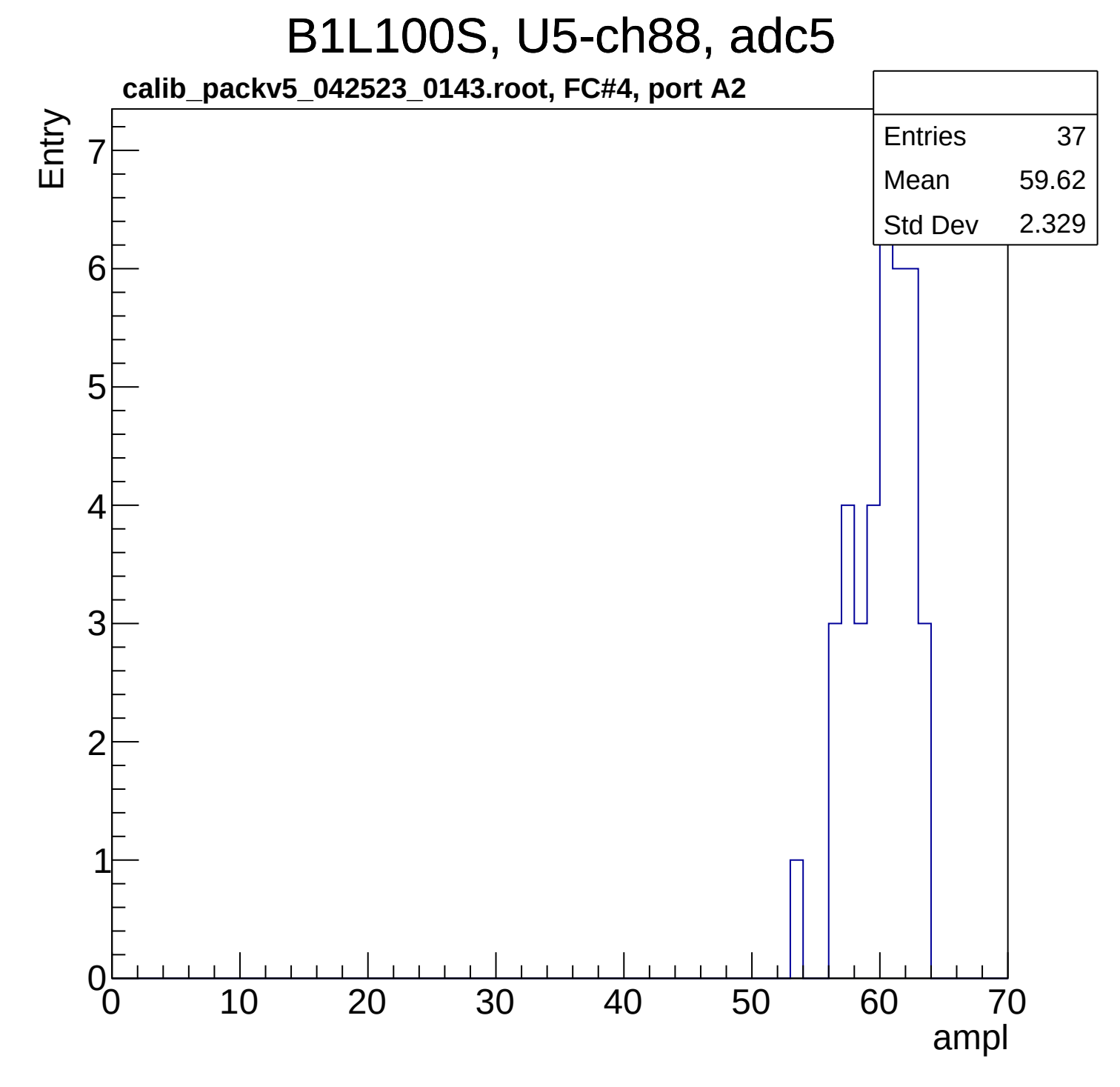

B1L100S, U5-ch88, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 26.49
Std Dev 8.642
Gaus mean : 30.0178
Gaus Width: 3.6536
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

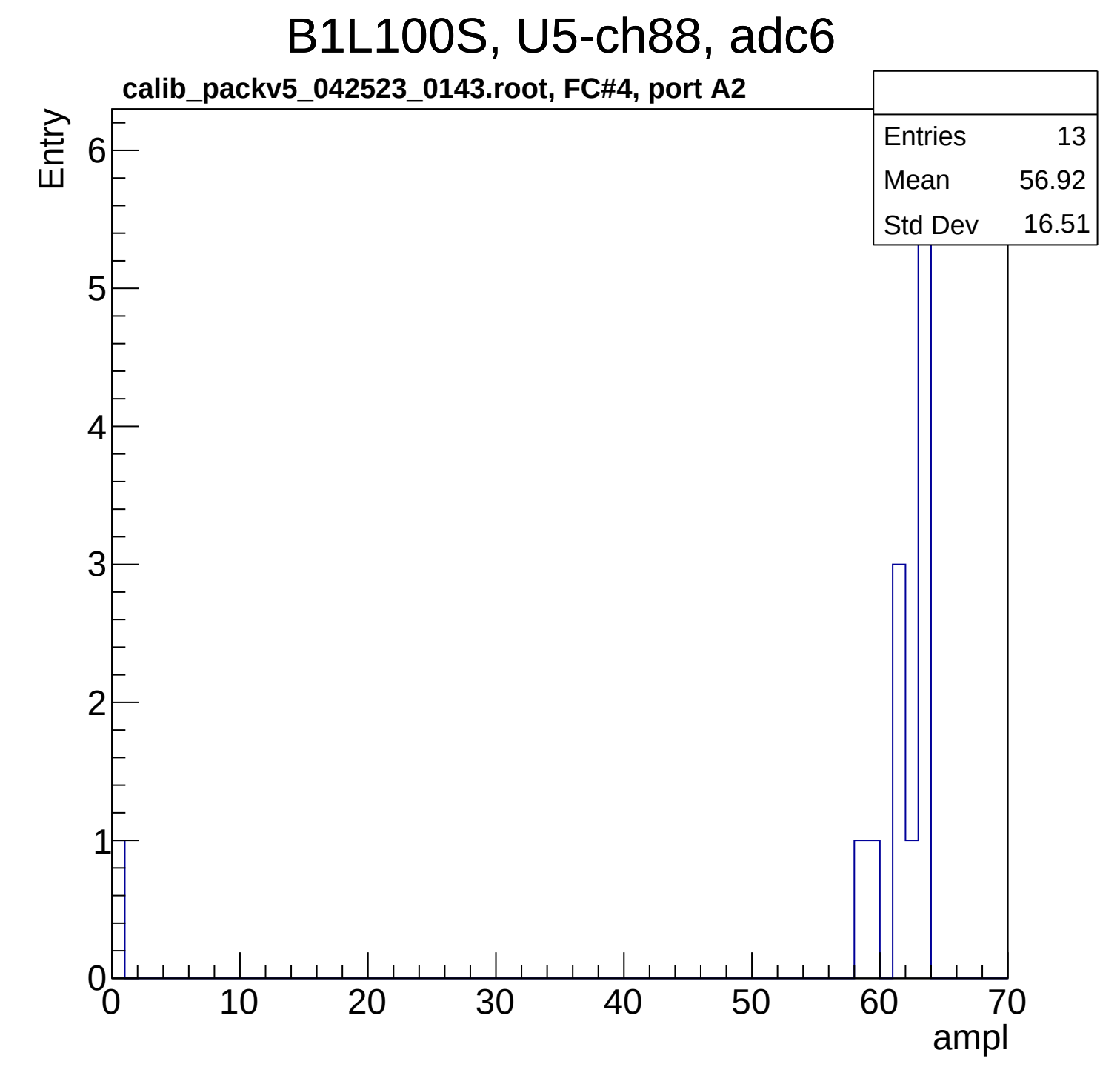

B1L100S, U5-ch88, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 75
Mean 35.59
Std Dev 3.622
Gaus mean : 36.3081
Gaus Width: 4.3287
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

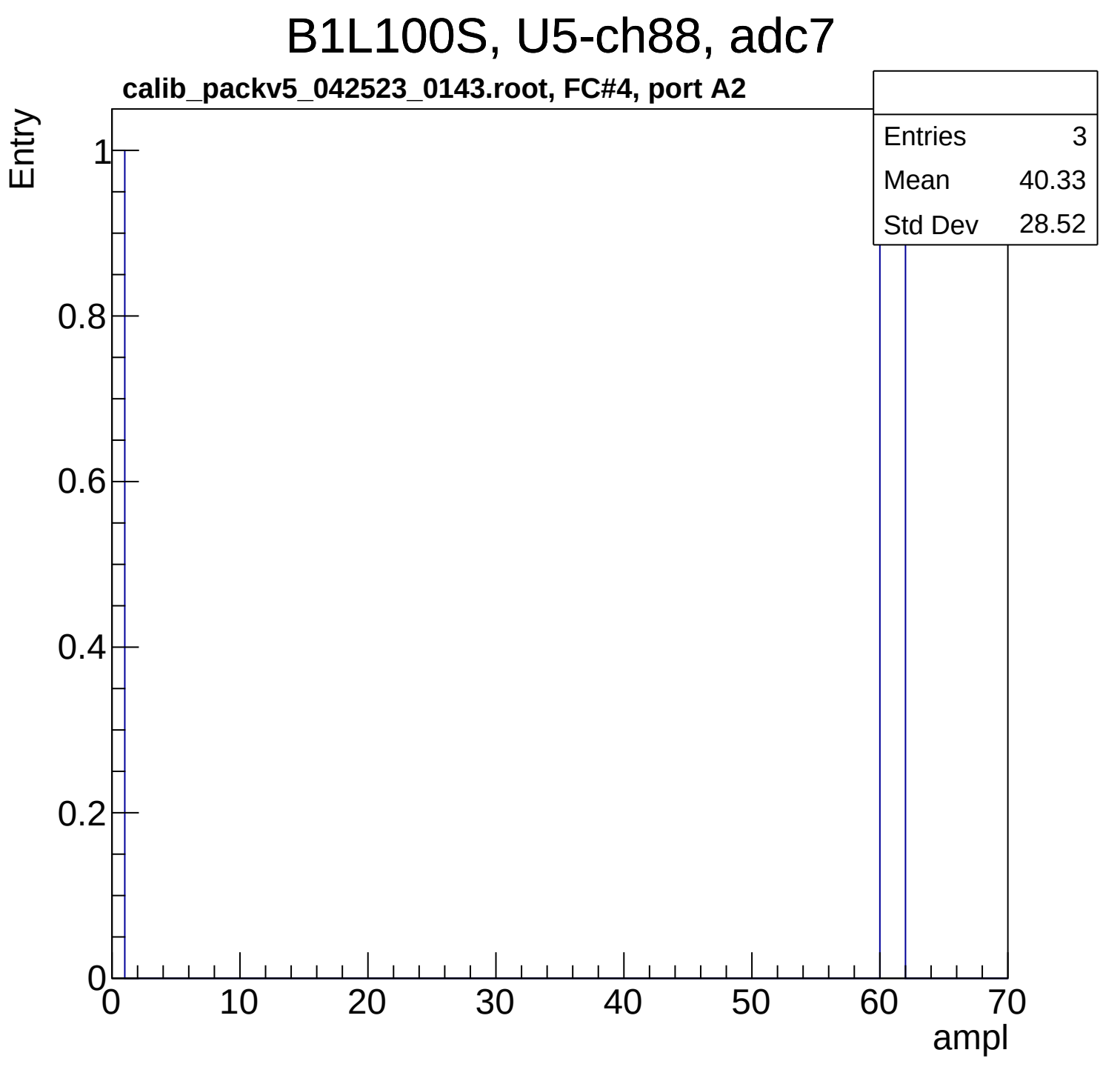

B1L100S, U5-ch88, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 42.46
Std Dev 3.263
Gaus mean : 42.8333
Gaus Width: 3.6736
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

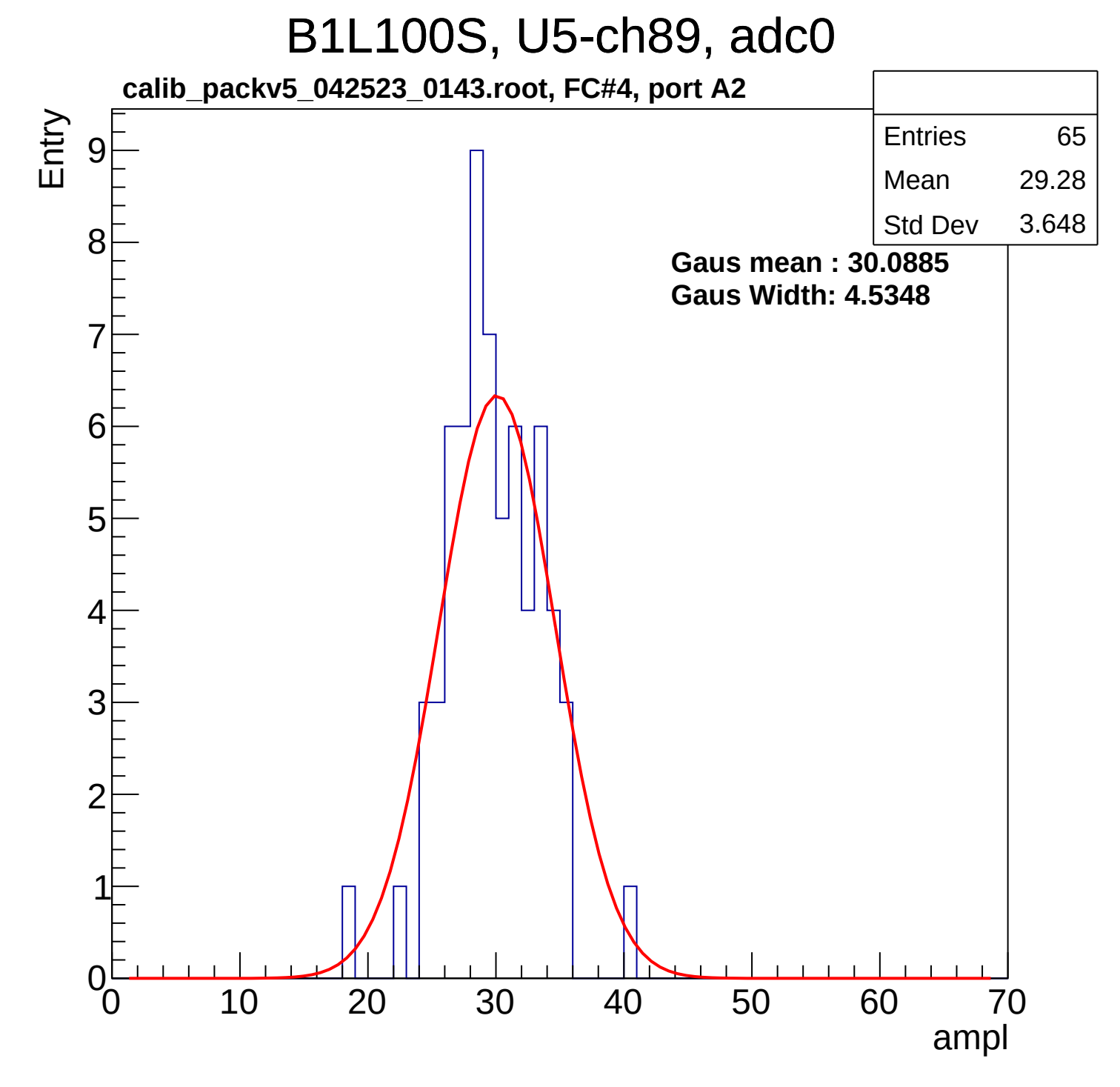

B1L100S, U5-ch88, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 49.27
Std Dev 3.298
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

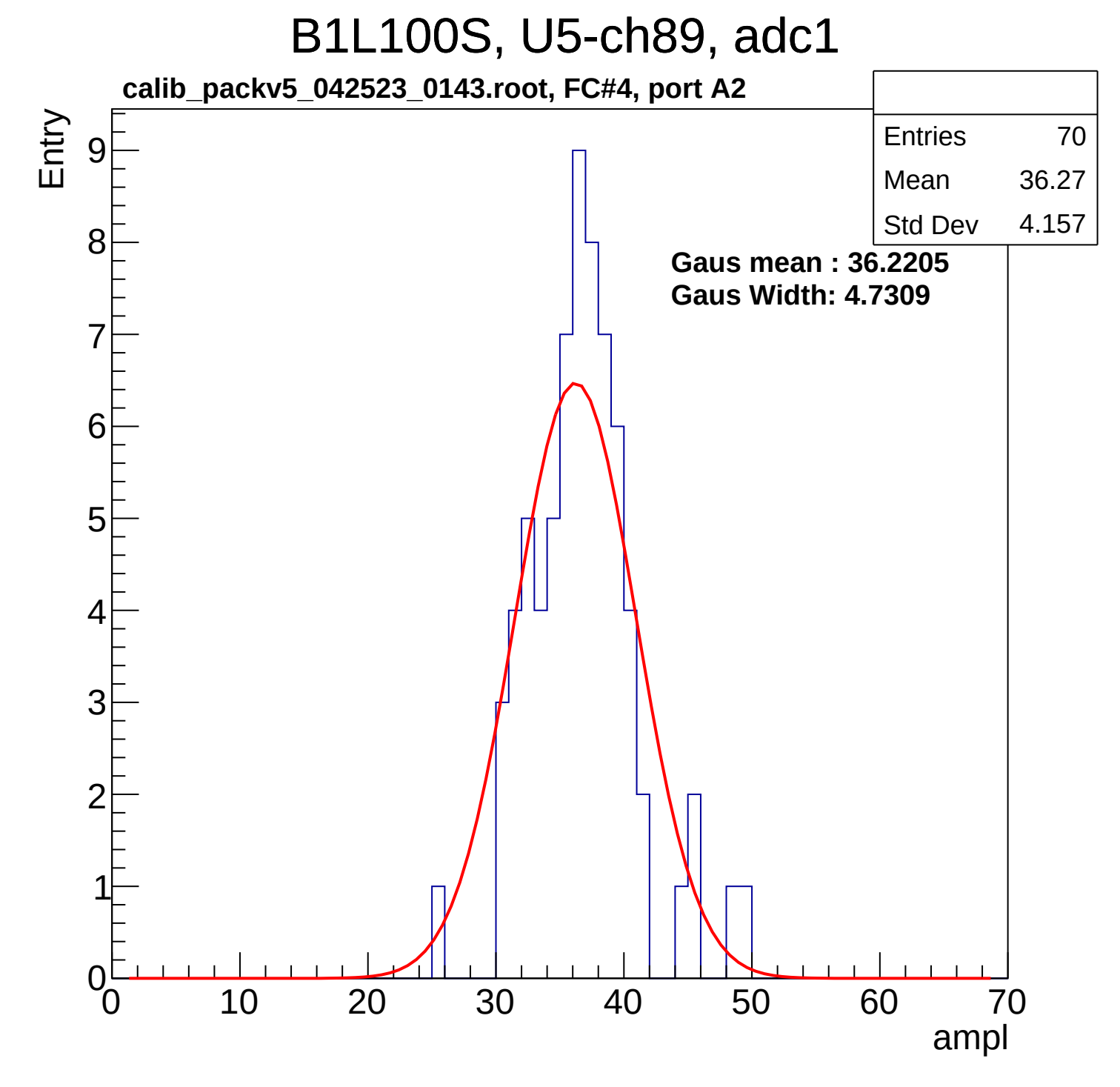

B1L100S, U5-ch88, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 54.91
Std Dev 3.964
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

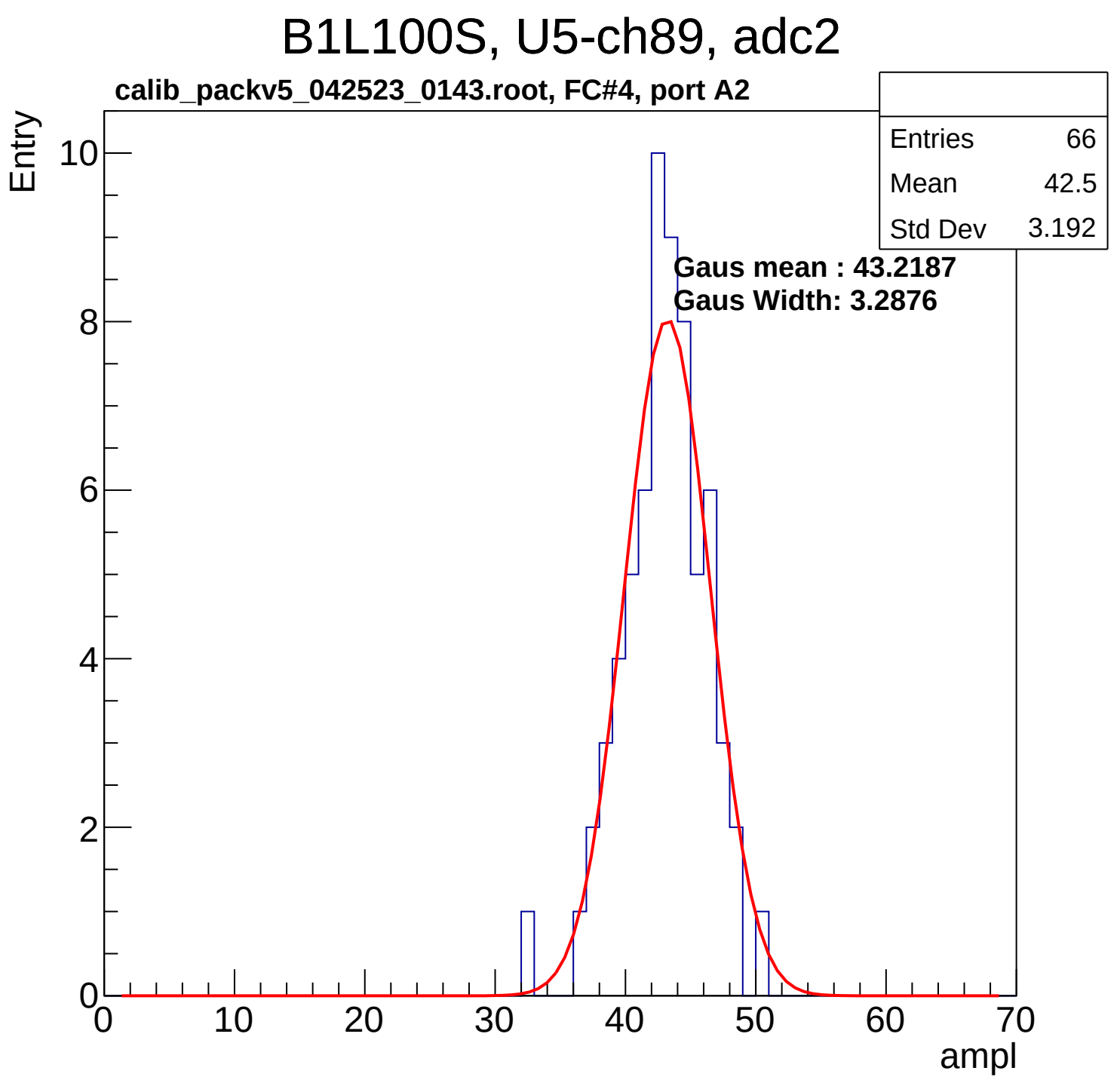

B1L100S, U5-ch88, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 37
Mean 59.62
Std Dev 2.329
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

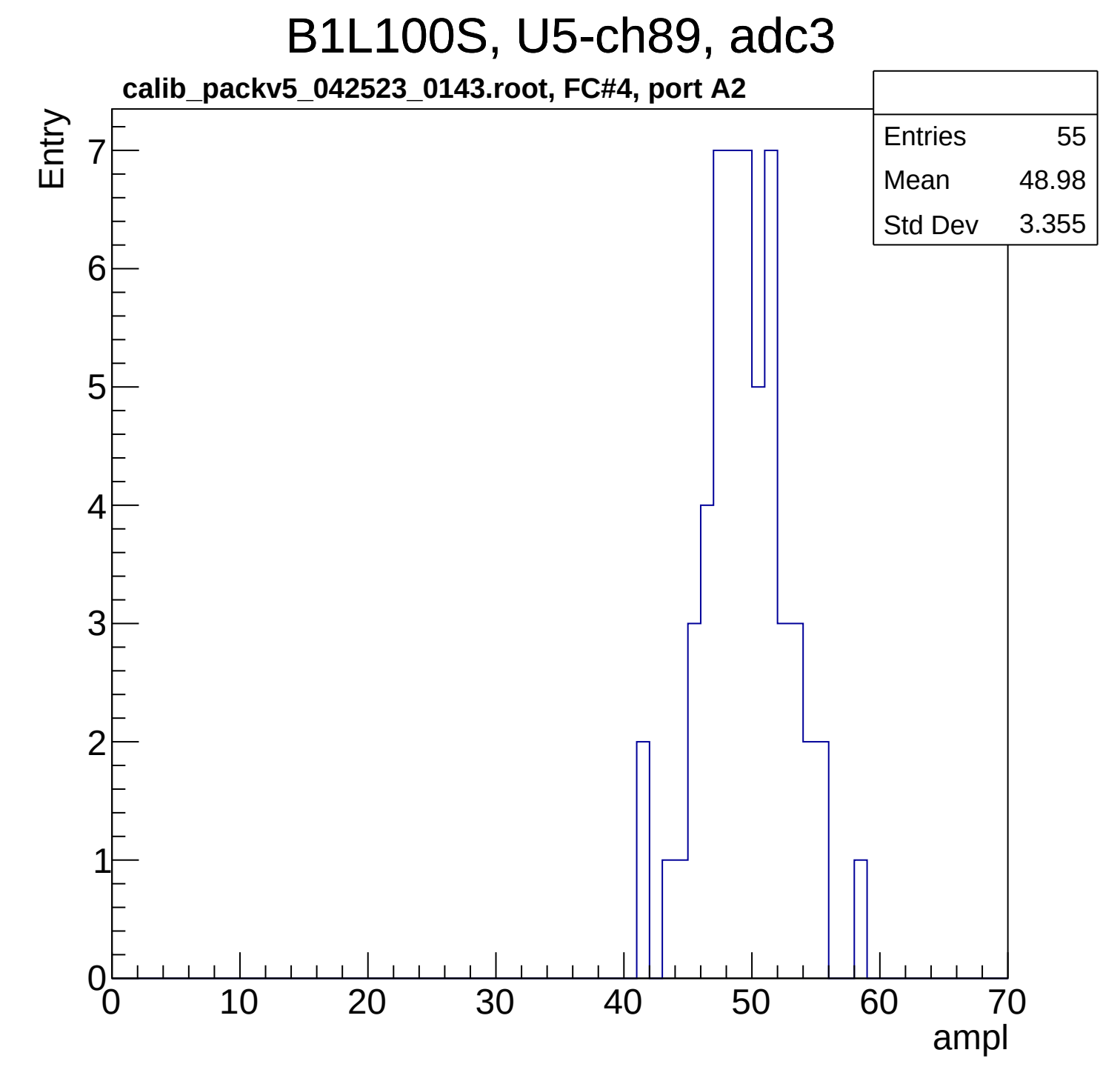

B1L100S, U5-ch88, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 13
Mean 56.92
Std Dev 16.51
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

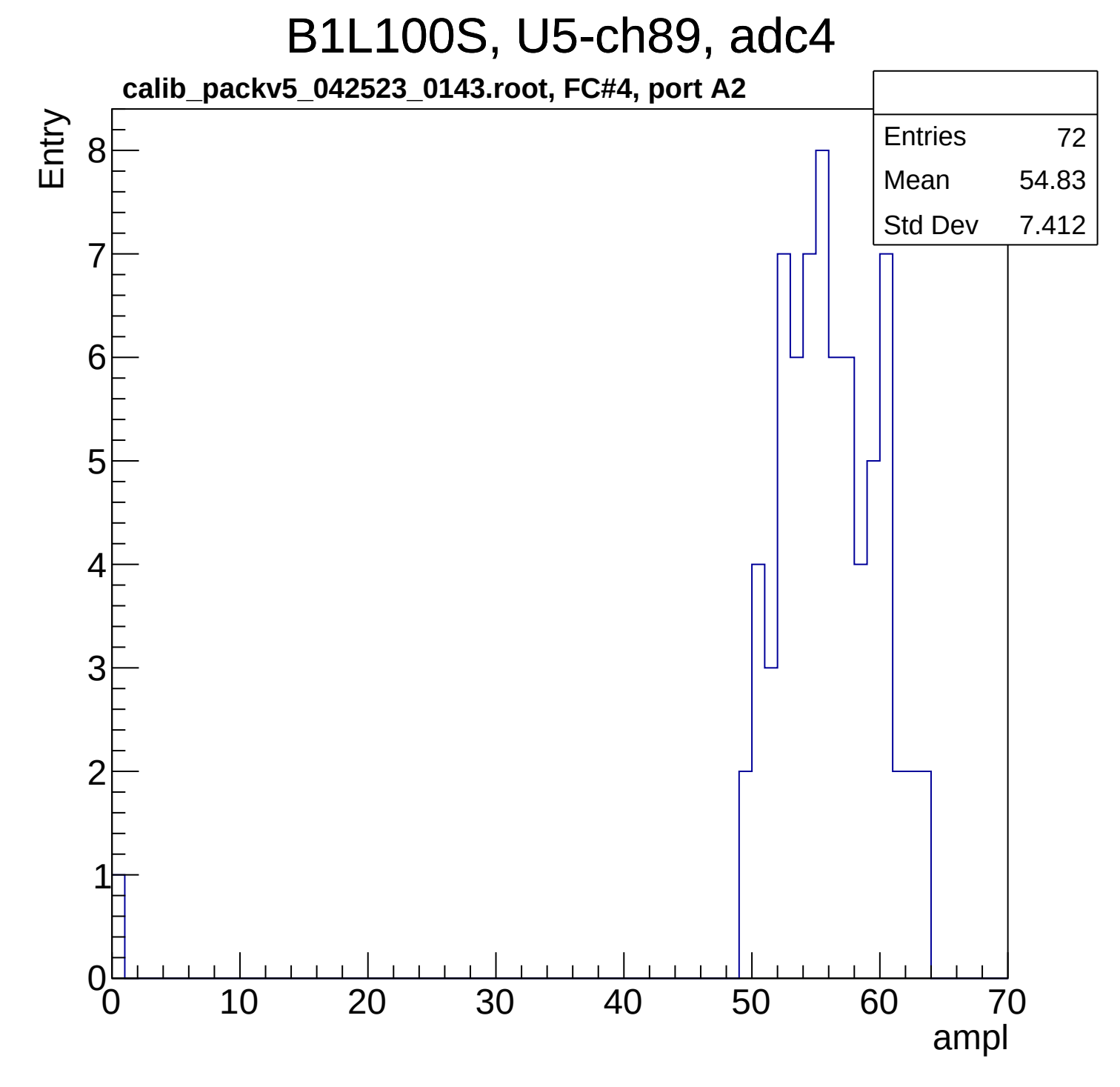

B1L100S, U5-ch88, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 40.33
Std Dev 28.52
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

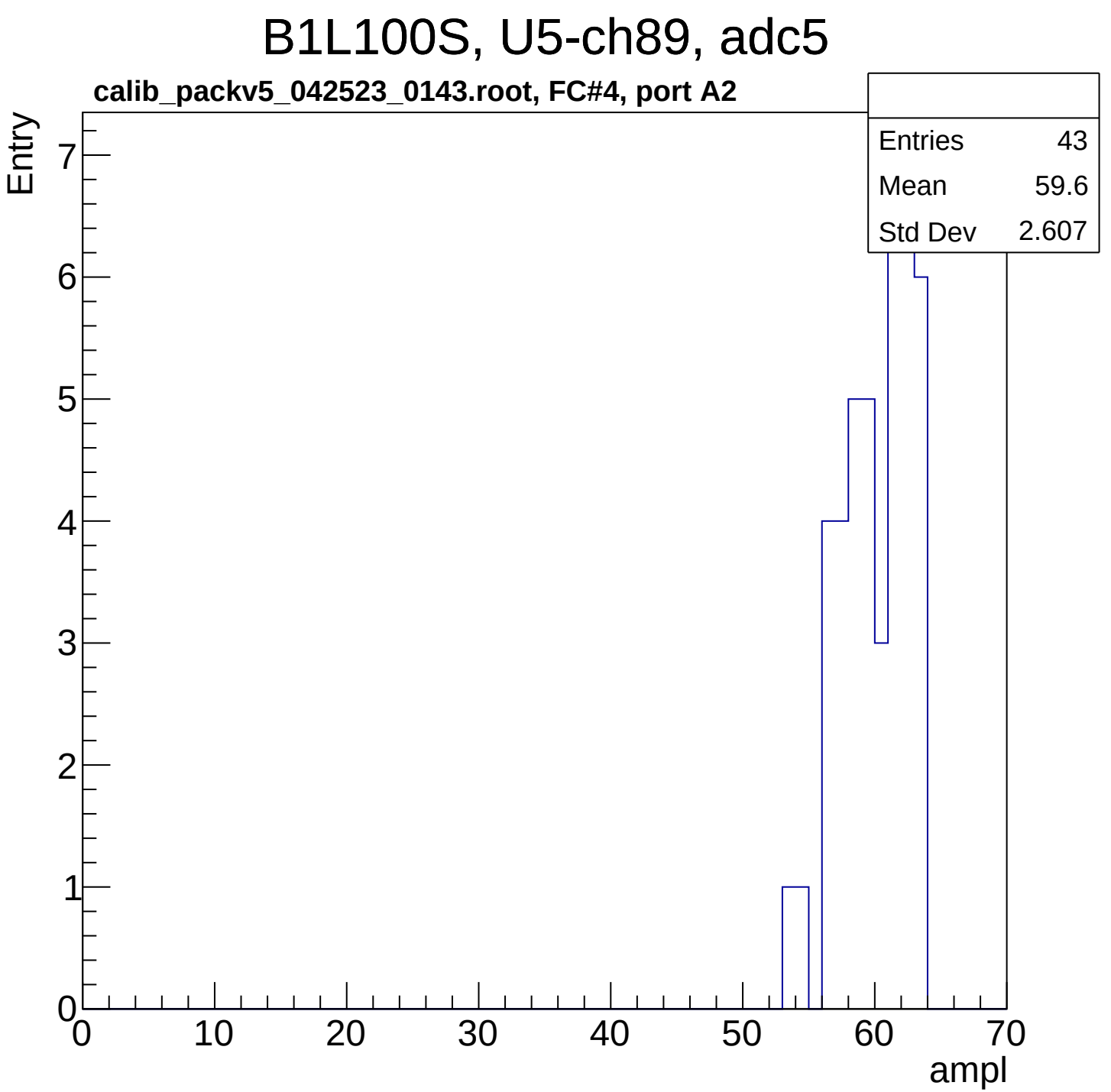

B1L100S, U5-ch89, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 29.28
Std Dev 3.648
Gaus mean : 30.0885
Gaus Width: 4.5348
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

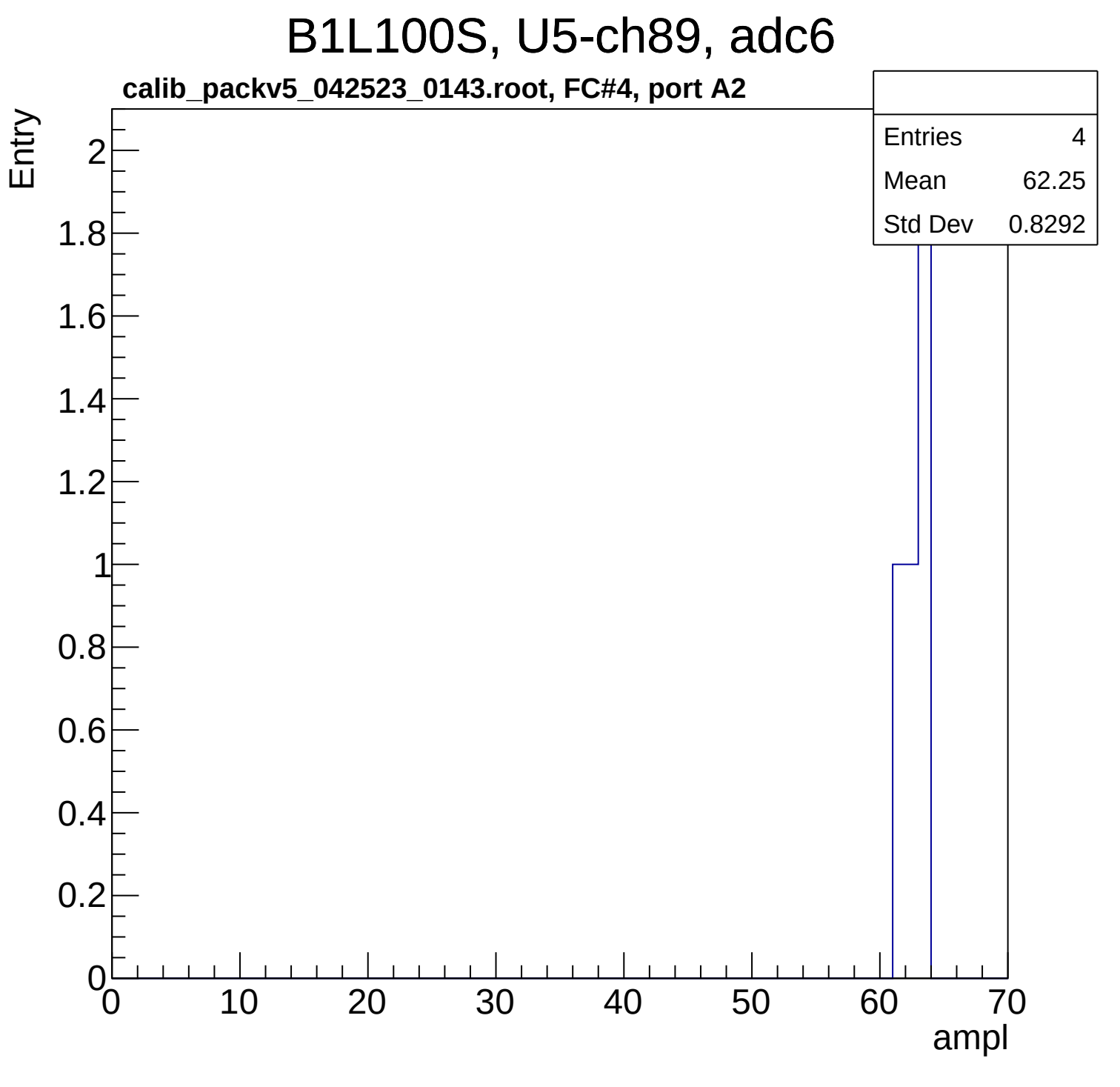

B1L100S, U5-ch89, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 36.27
Std Dev 4.157
Gaus mean : 36.2205
Gaus Width: 4.7309
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

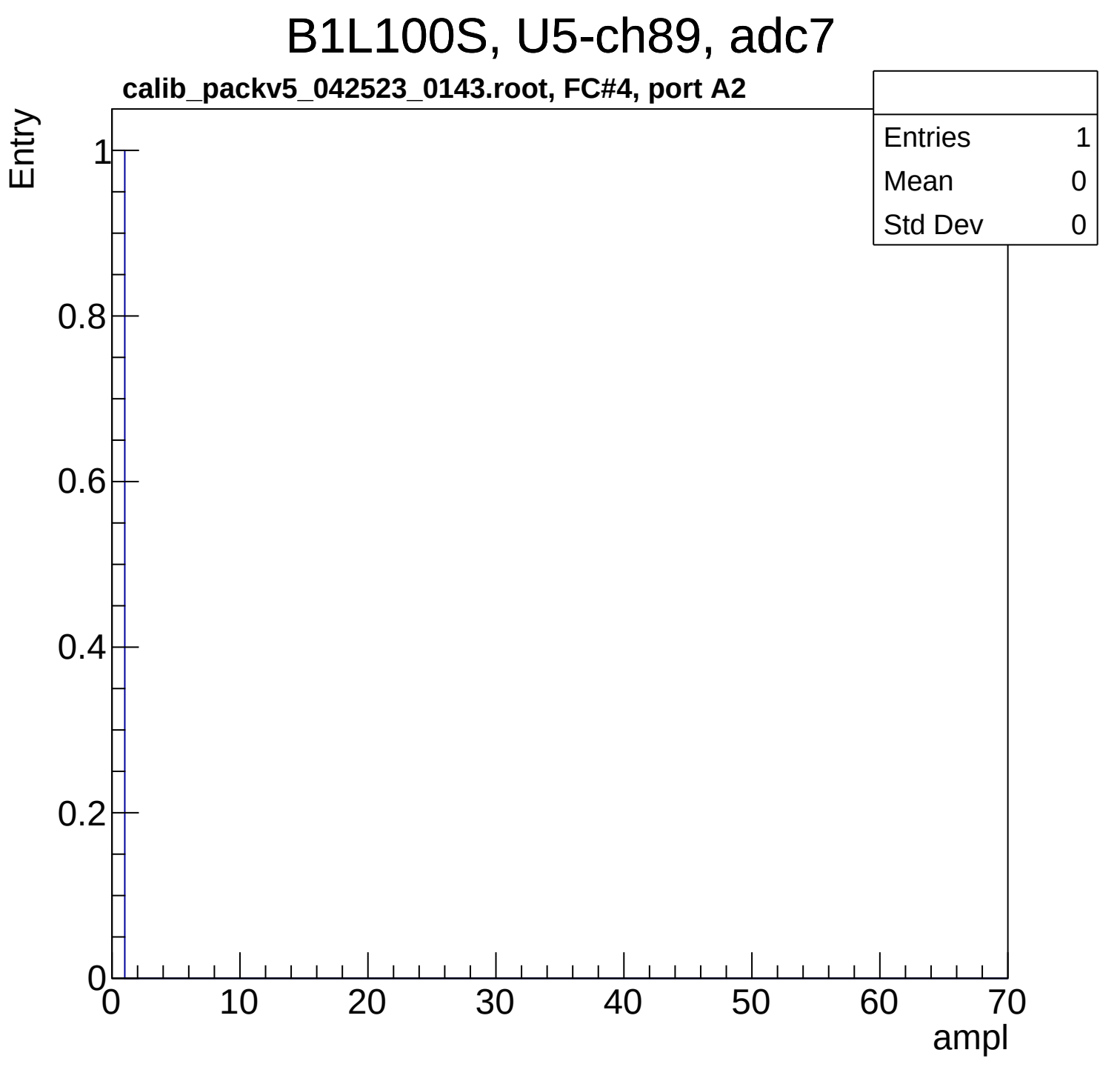

B1L100S, U5-ch89, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 42.5
Std Dev 3.192
Gaus mean : 43.2187
Gaus Width: 3.2876
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

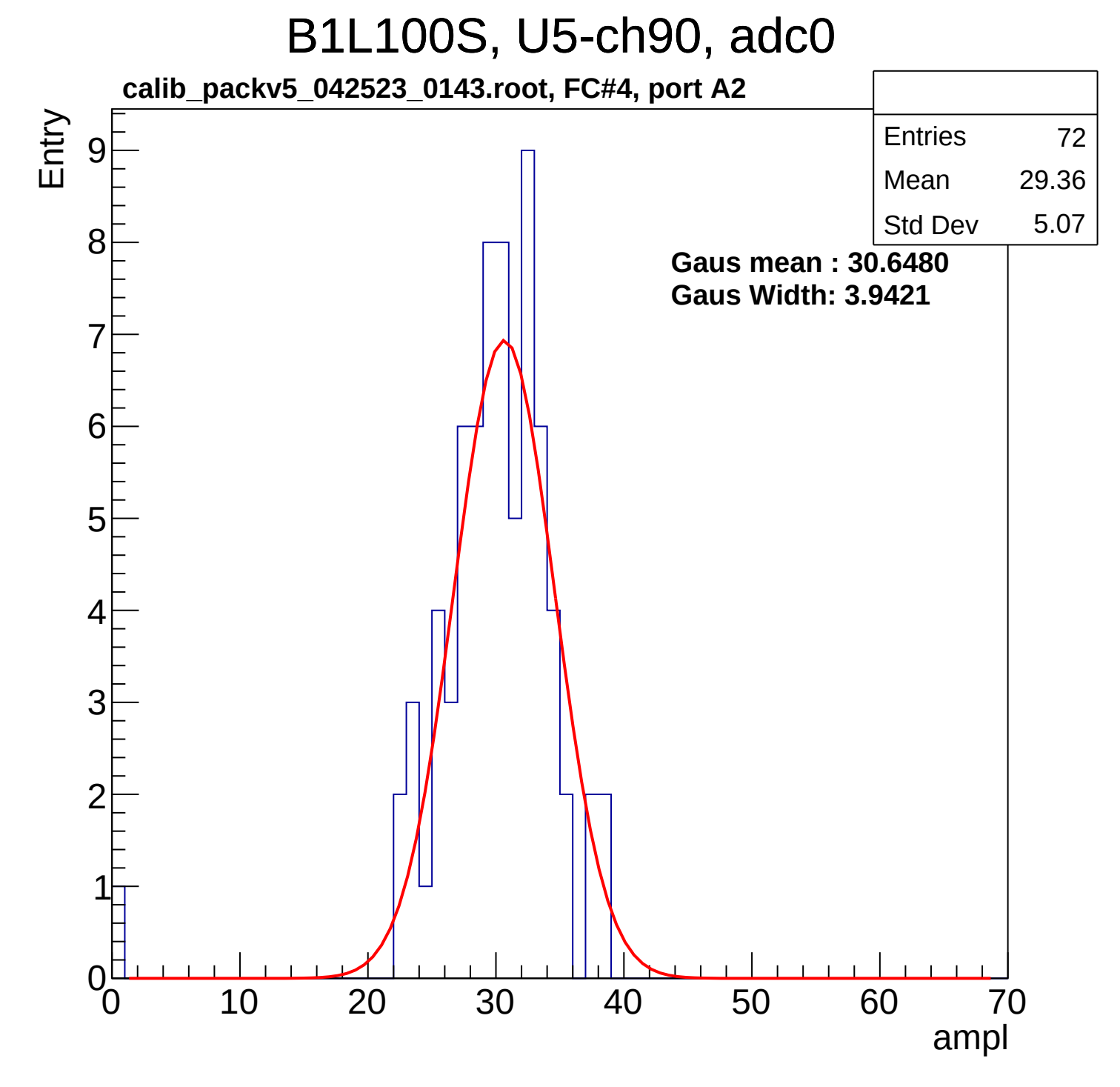

B1L100S, U5-ch89, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 48.98
Std Dev 3.355
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

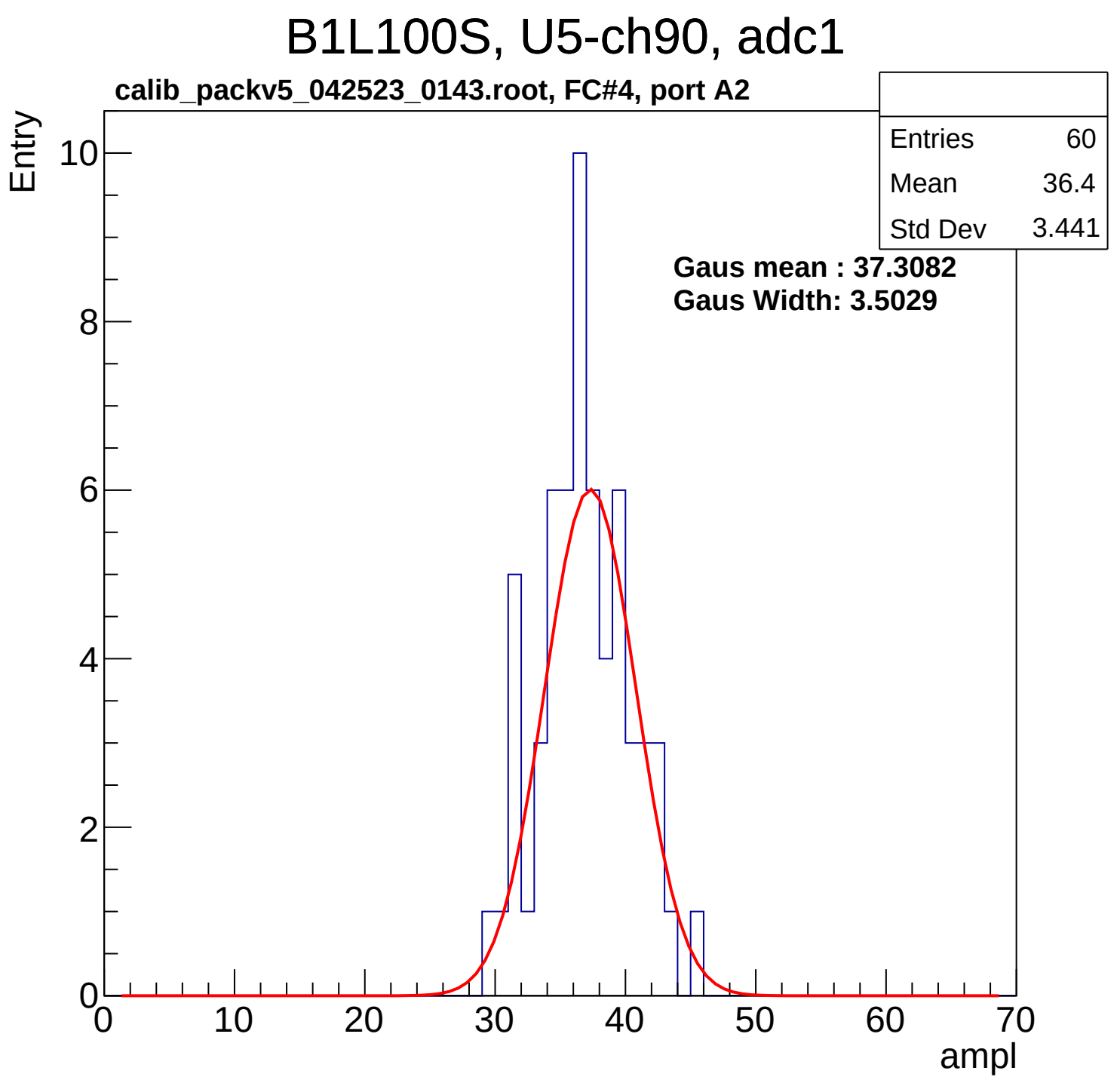

B1L100S, U5-ch89, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 54.83
Std Dev 7.412
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

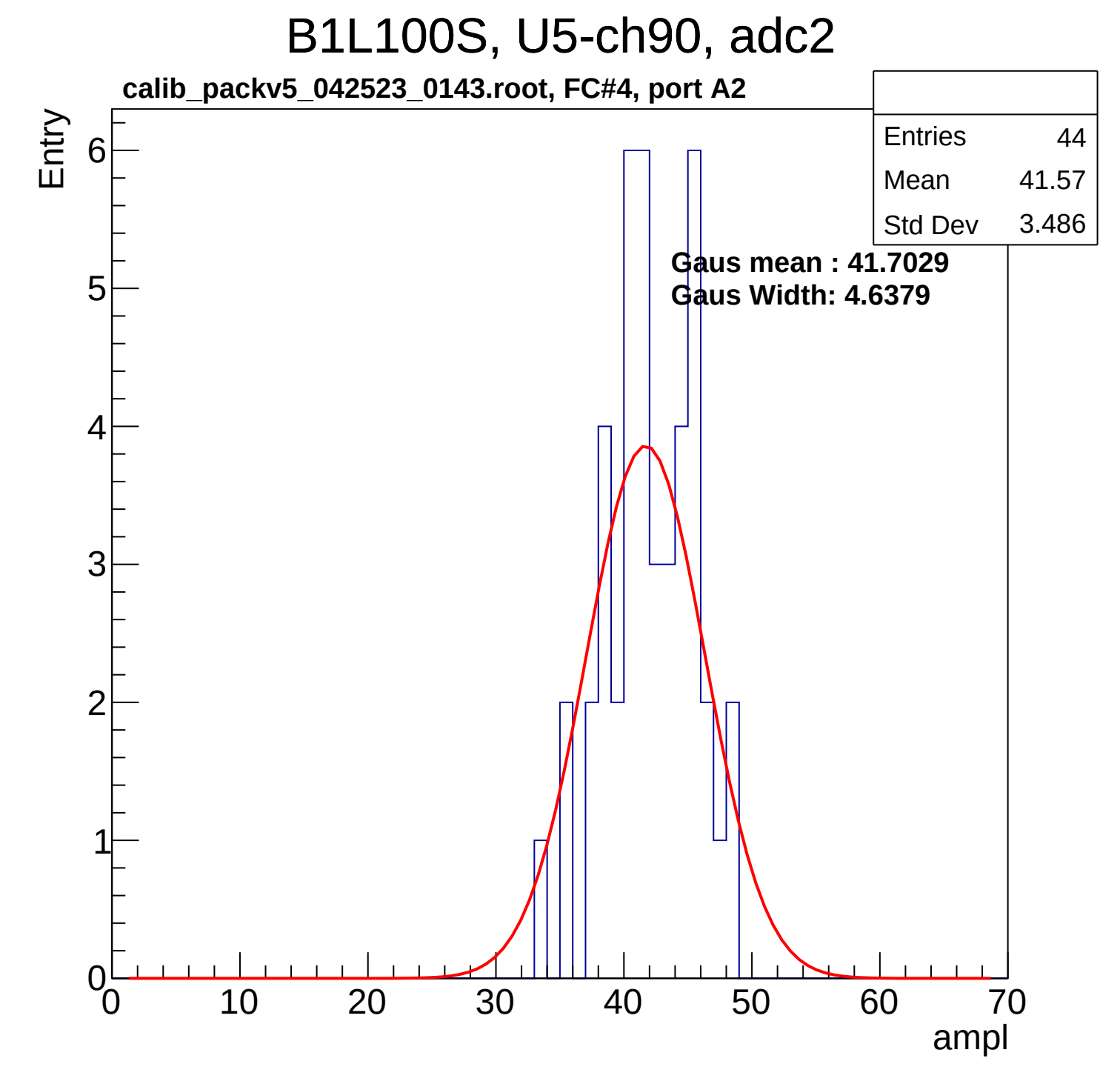

B1L100S, U5-ch89, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 43
Mean 59.6
Std Dev 2.607
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl

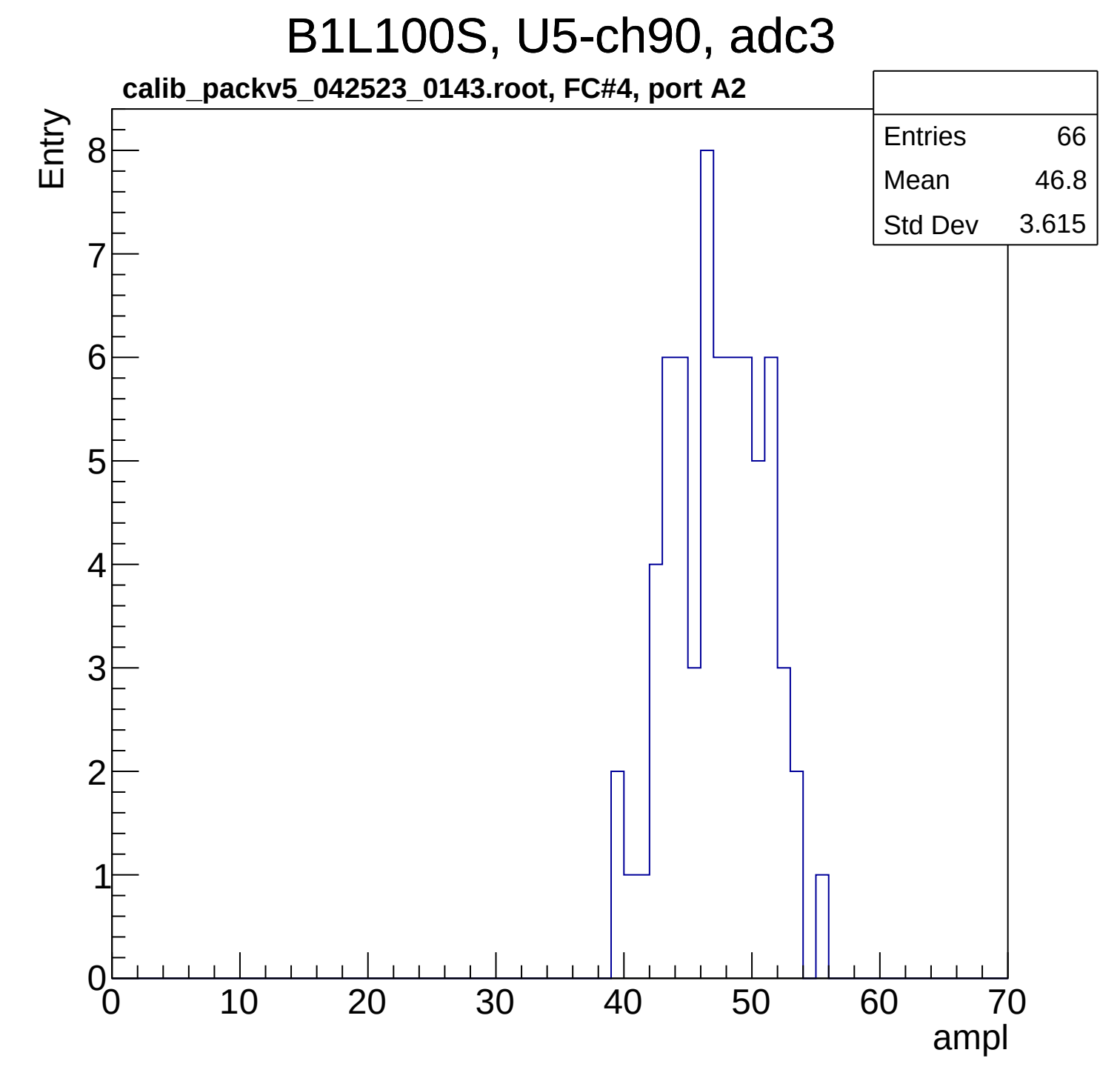

B1L100S, U5-ch89, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 4
Mean 62.25
Std Dev 0.8292
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

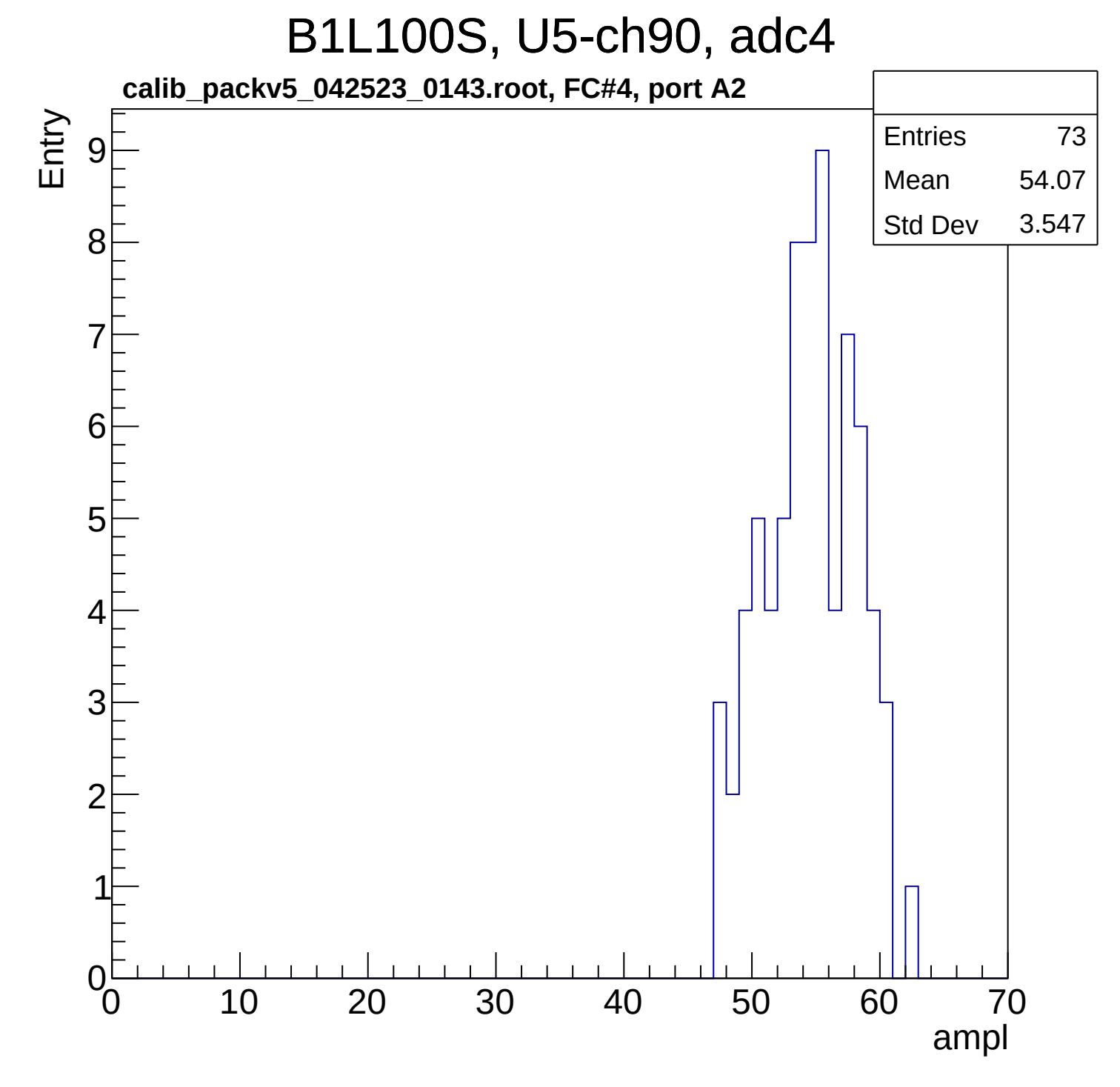

B1L100S, U5-ch89, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch90, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 29.36
Std Dev 5.07
Gaus mean : 30.6480
Gaus Width: 3.9421
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch90, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 36.4
Std Dev 3.441
Gaus mean : 37.3082
Gaus Width: 3.5029
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch90, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 44
Mean 41.57
Std Dev 3.486
Gaus mean : 41.7029
Gaus Width: 4.6379
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L100S, U5-ch90, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 46.8
Std Dev 3.615
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch90, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 54.07
Std Dev 3.547
Entry
ampl
0
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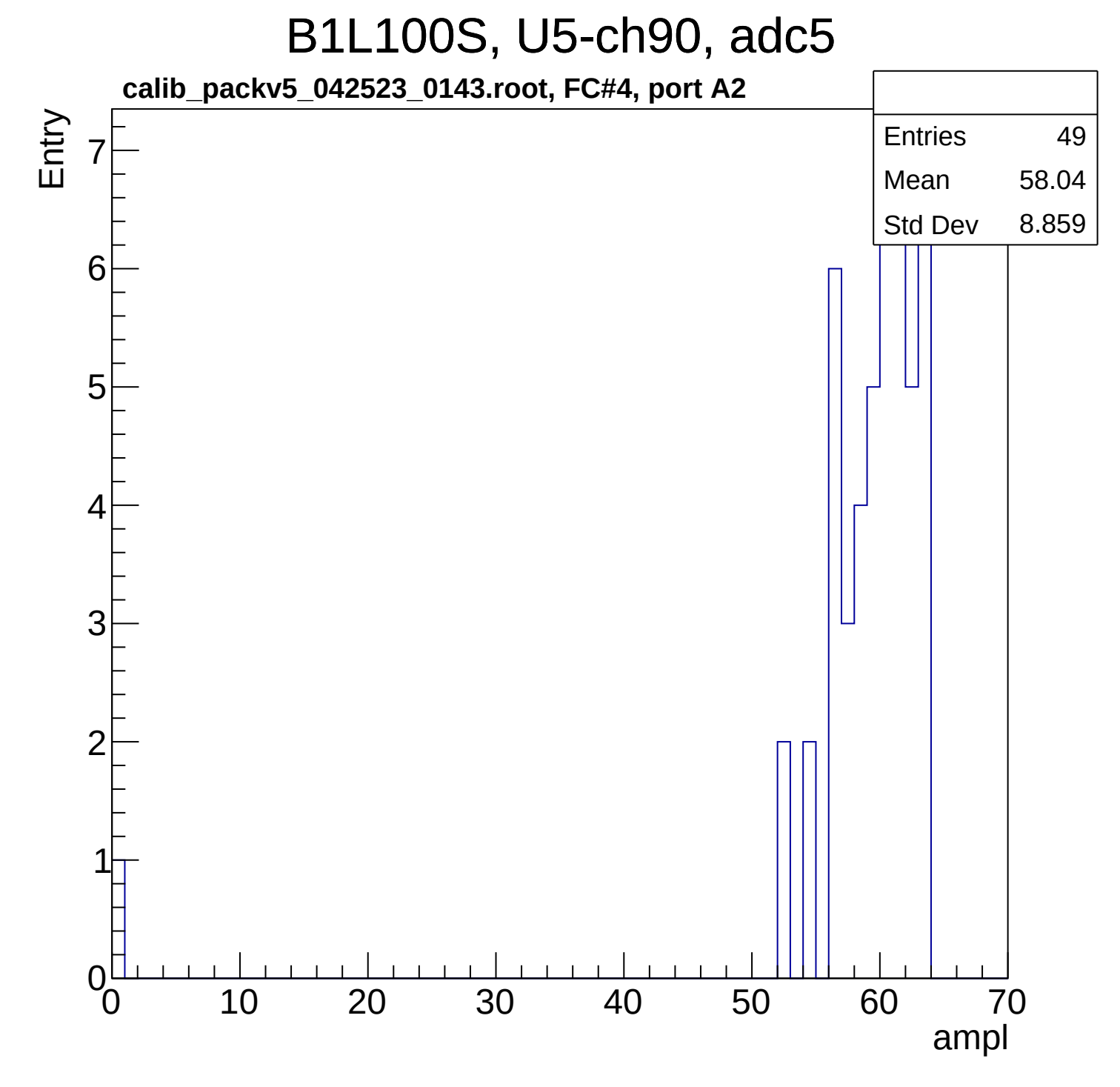
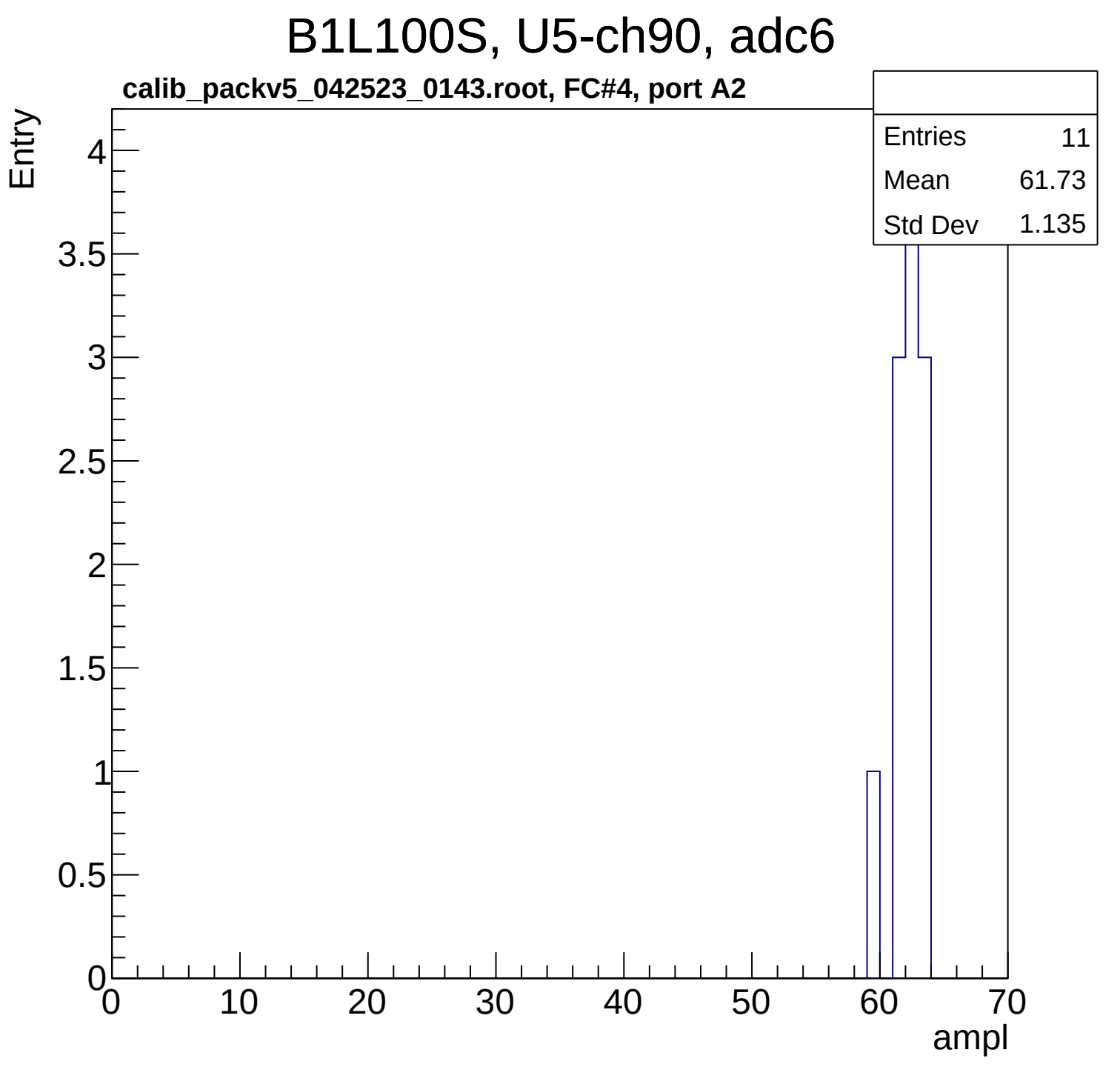
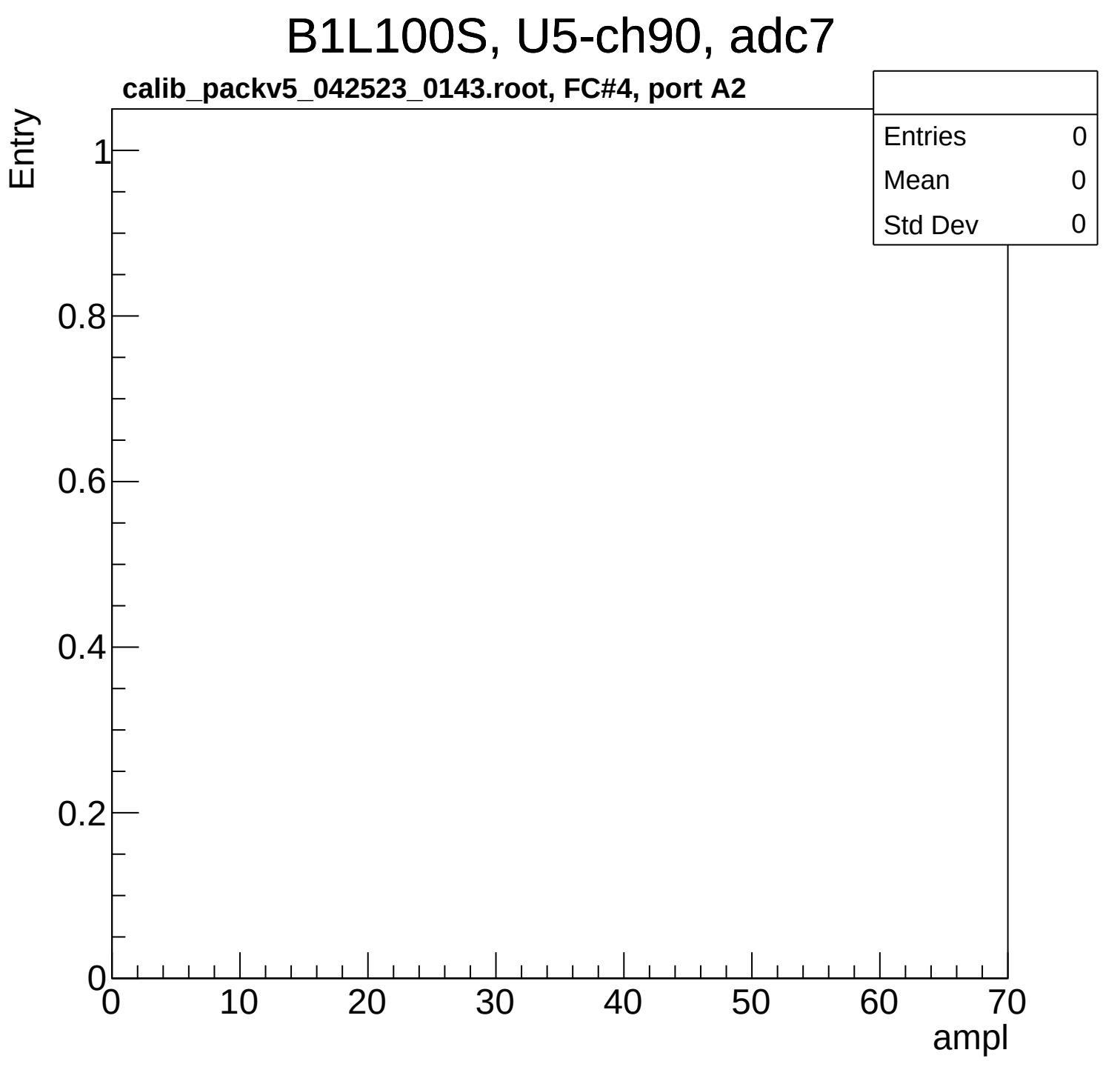
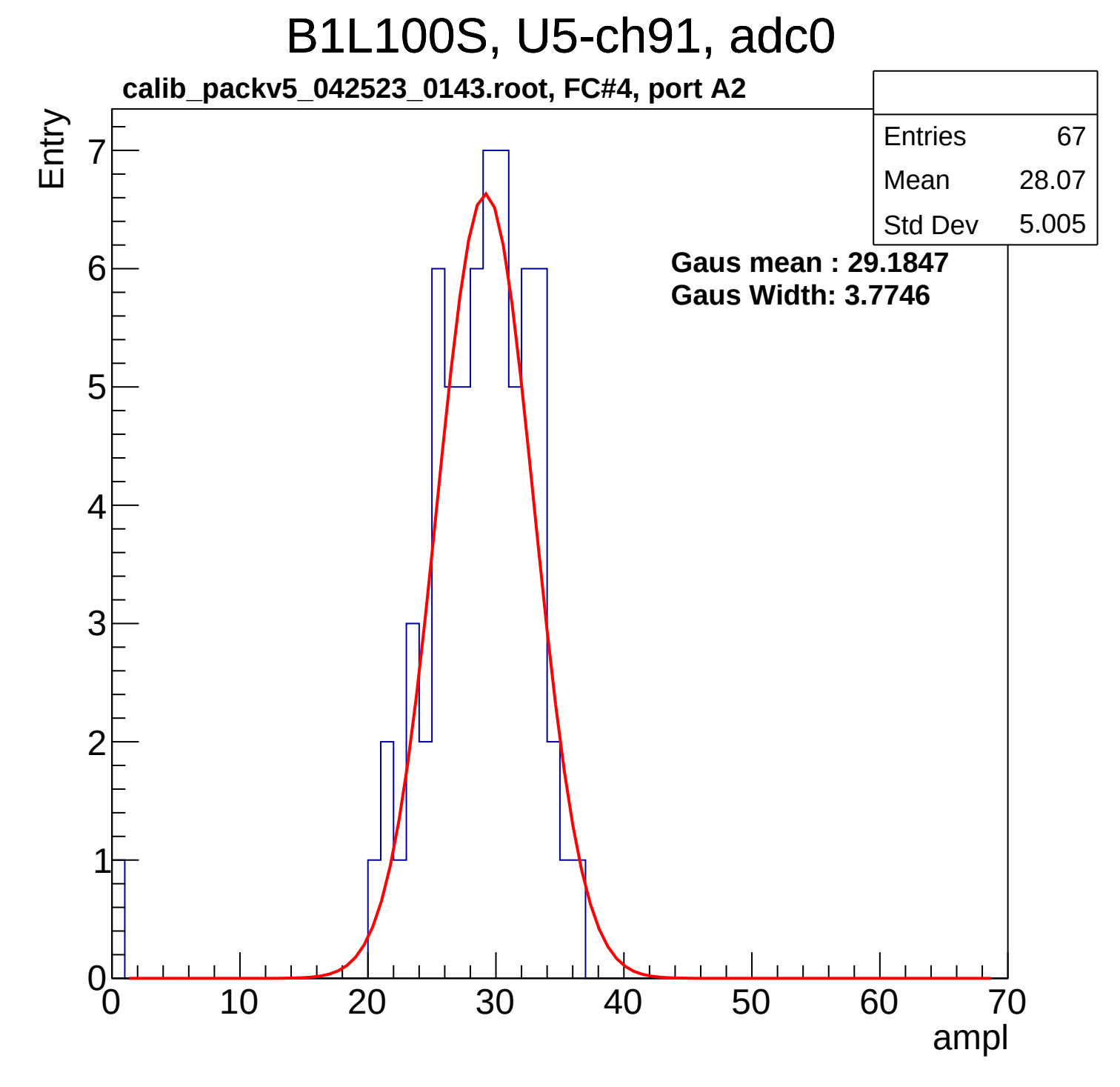
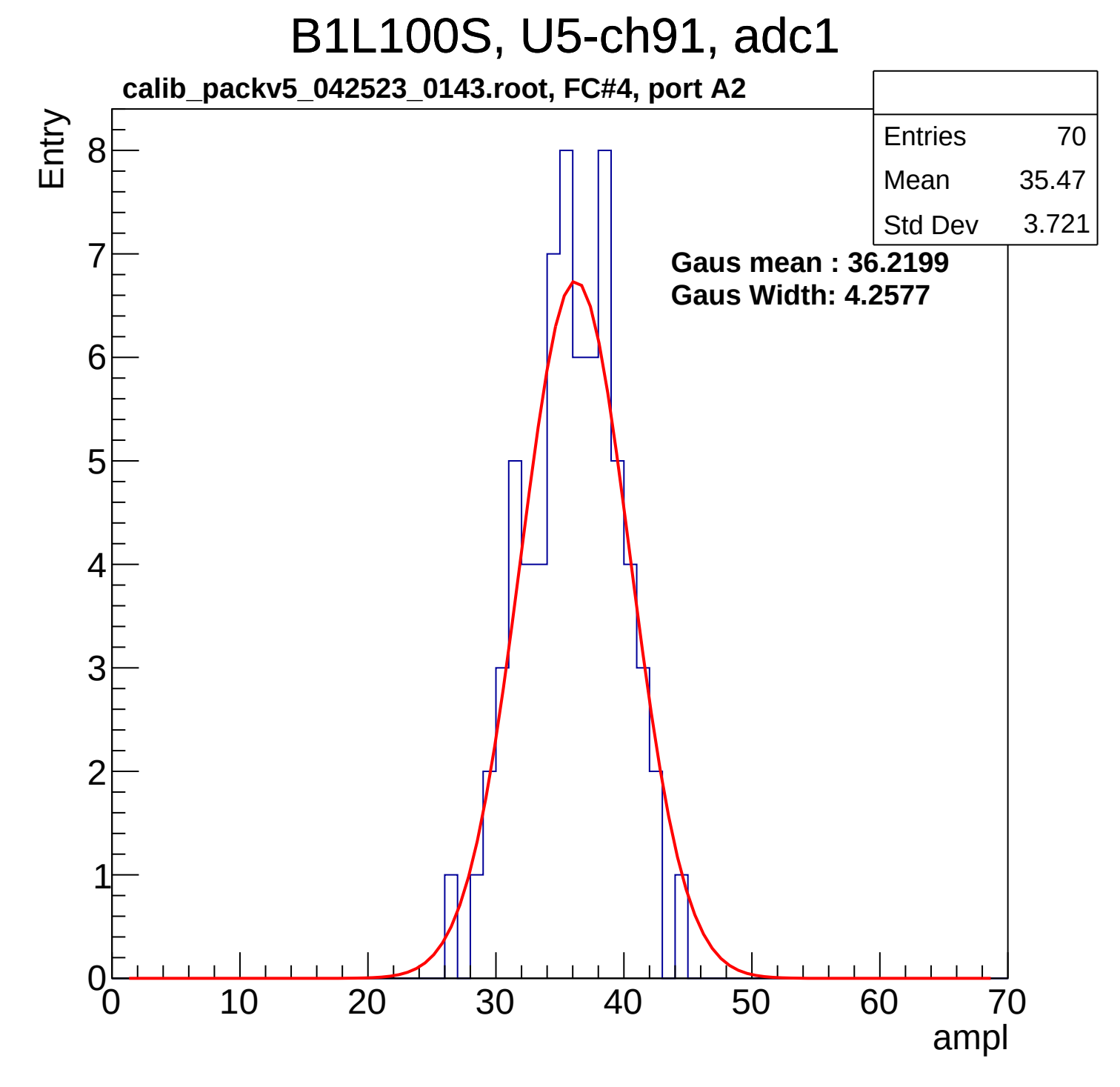
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

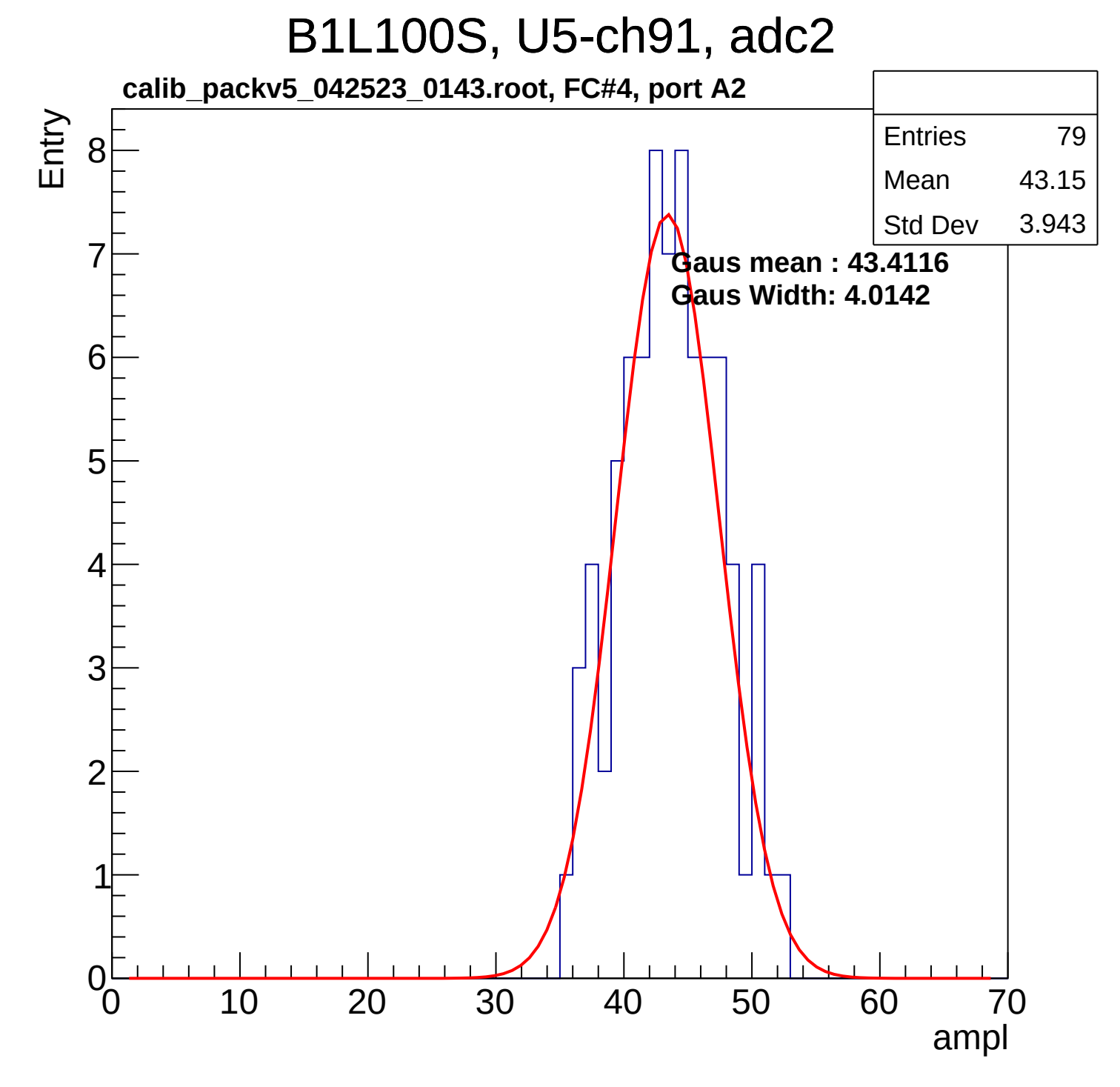

B1L100S, U5-ch90, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 49
Mean 58.04
Std Dev 8.859
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

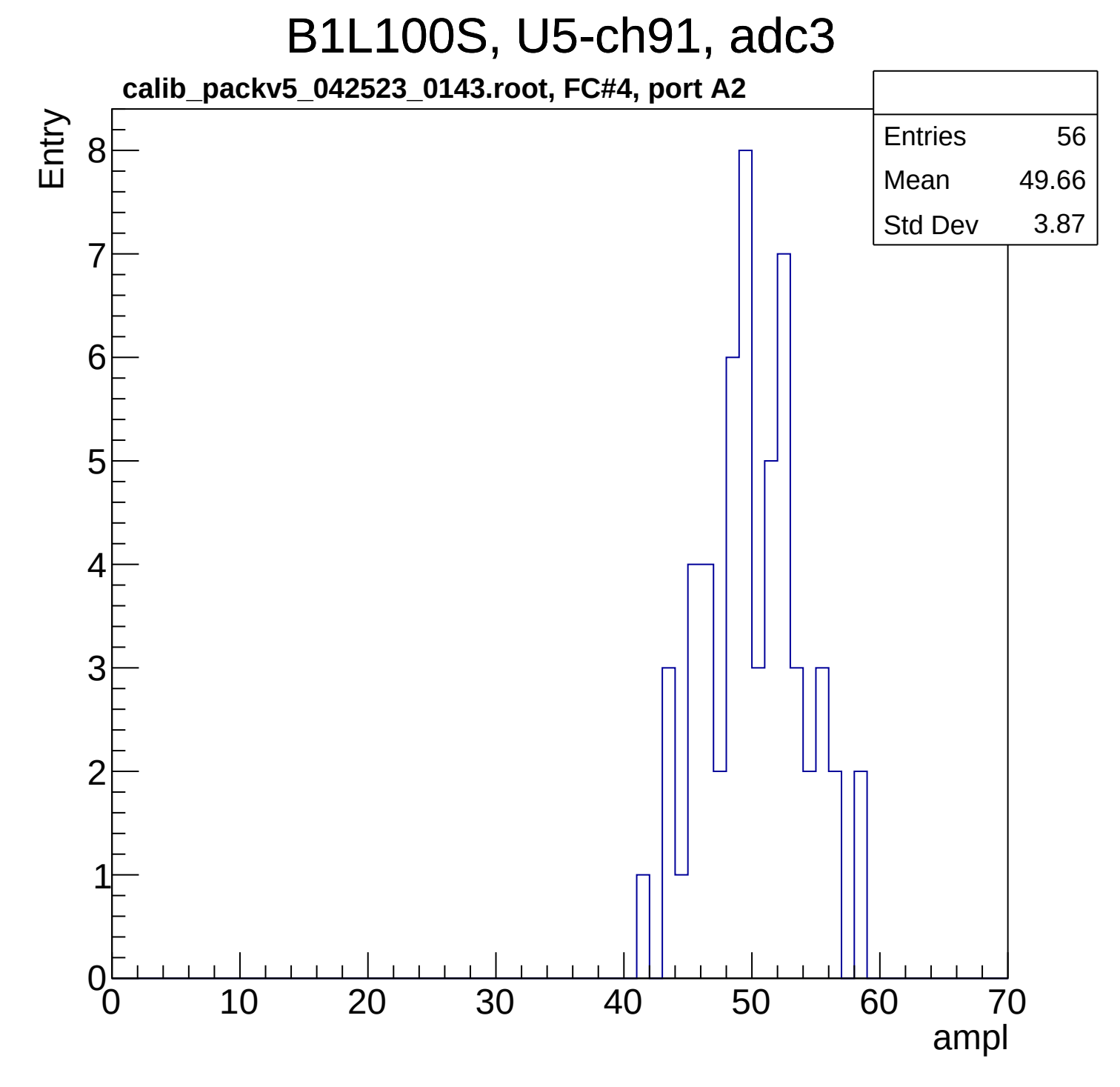

B1L100S, U5-ch90, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 11
Mean 61.73
Std Dev 1.135
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

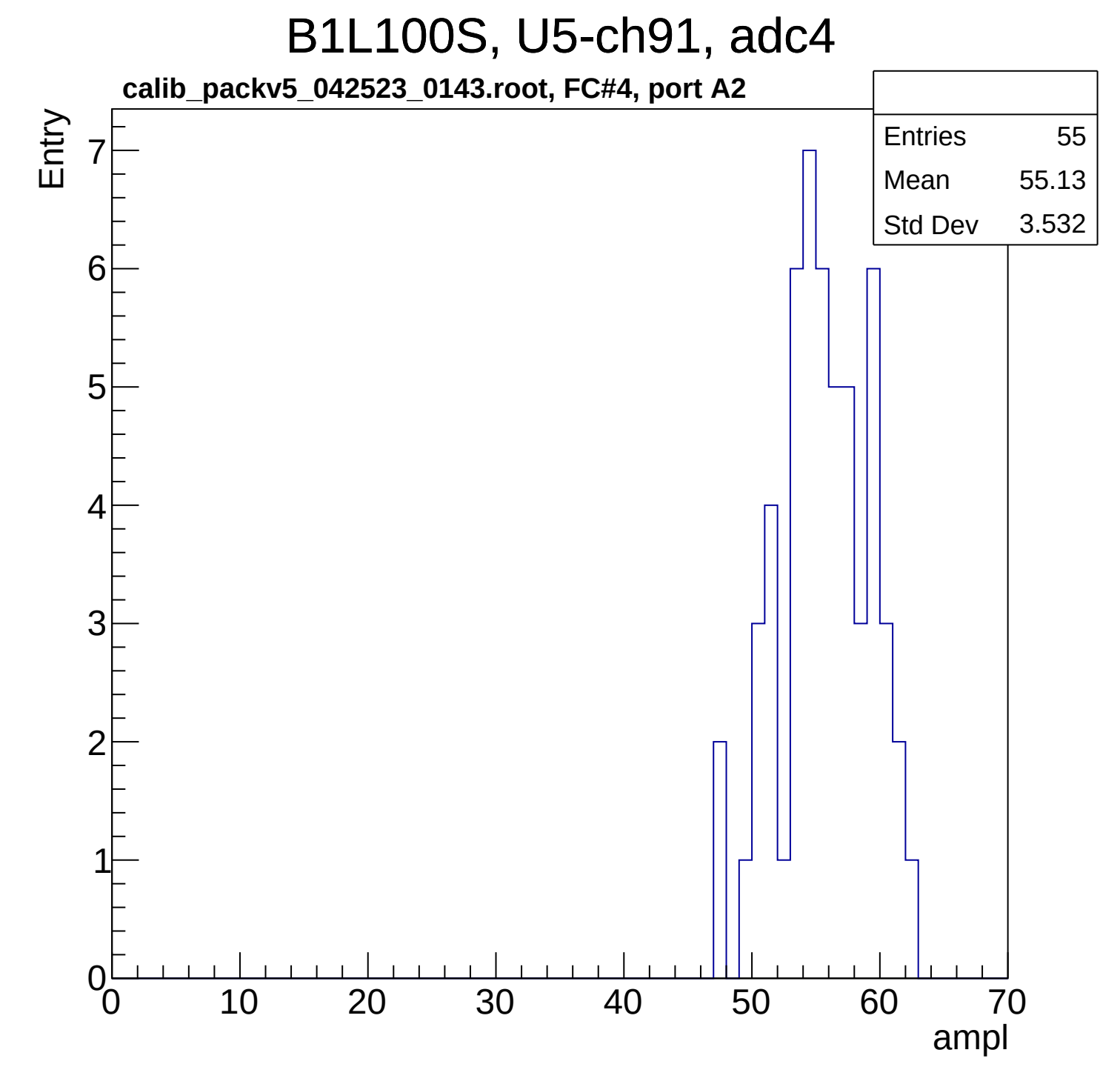

B1L100S, U5-ch90, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

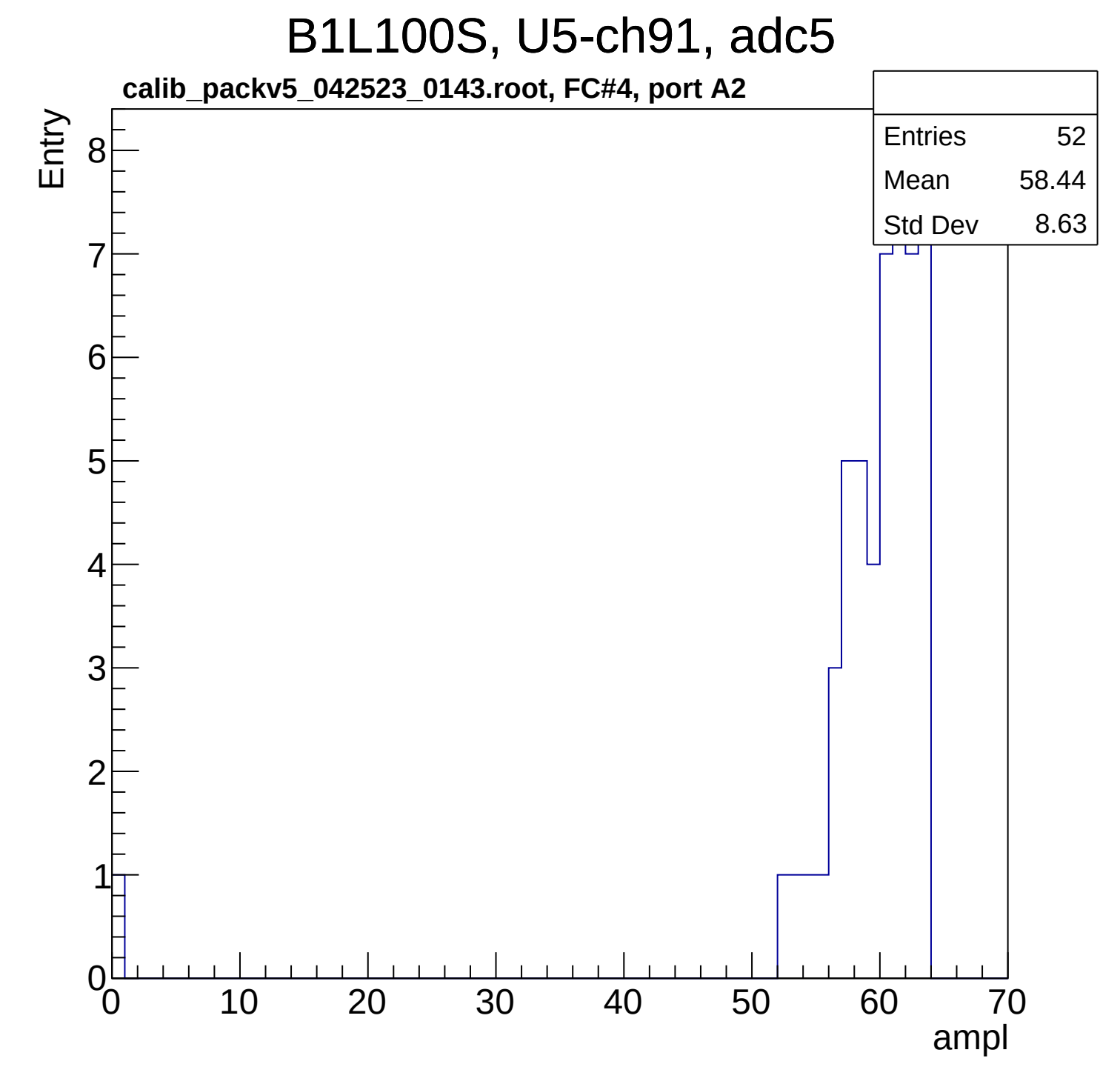

B1L100S, U5-ch91, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 28.07
Std Dev 5.005
Gaus mean : 29.1847
Gaus Width: 3.7746
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

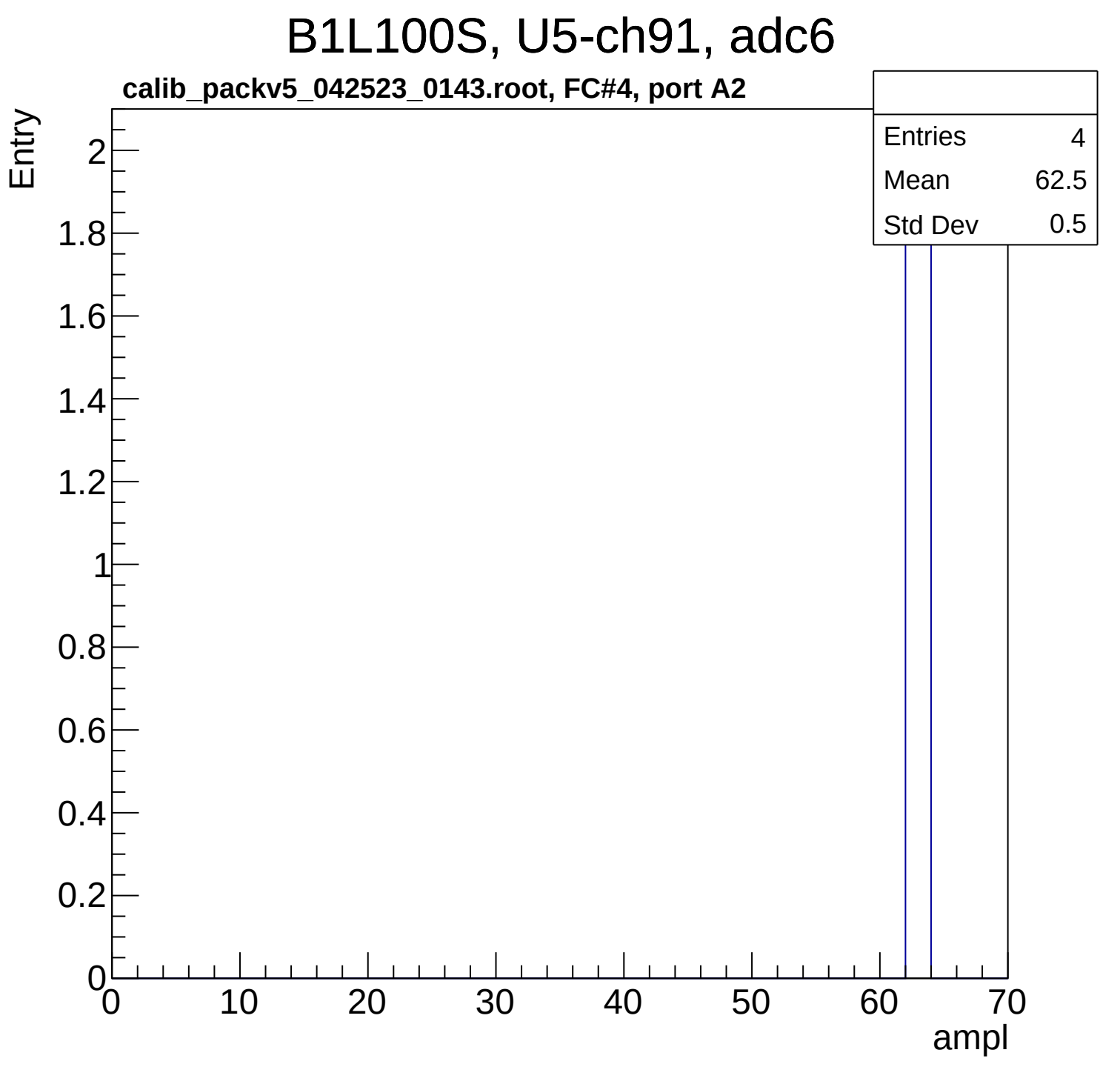

B1L100S, U5-ch91, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 35.47
Std Dev 3.721
Gaus mean : 36.2199
Gaus Width: 4.2577
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

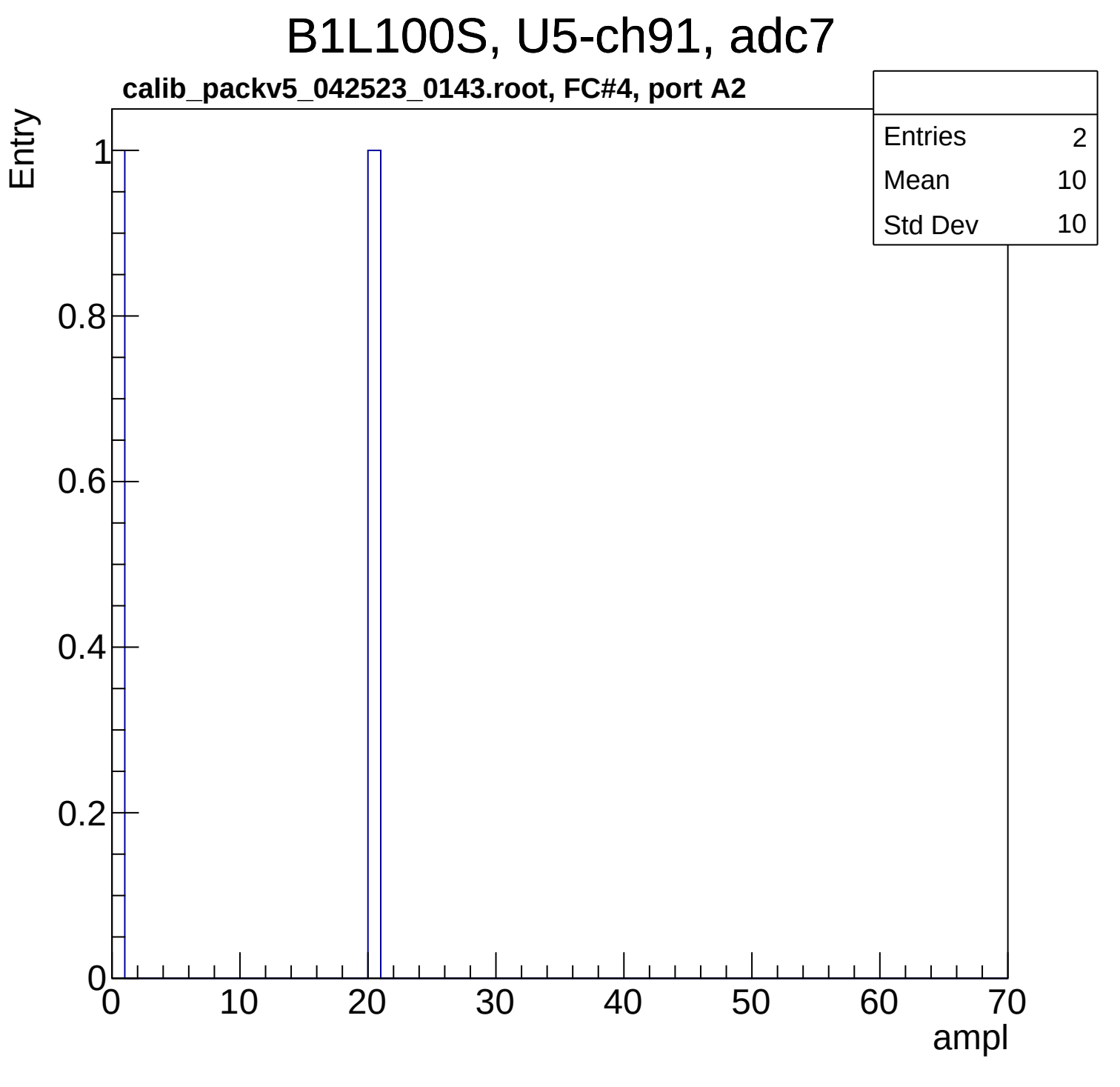

B1L100S, U5-ch91, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 79
Mean 43.15
Std Dev 3.943
Gaus mean : 43.4116
Gaus Width: 4.0142
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

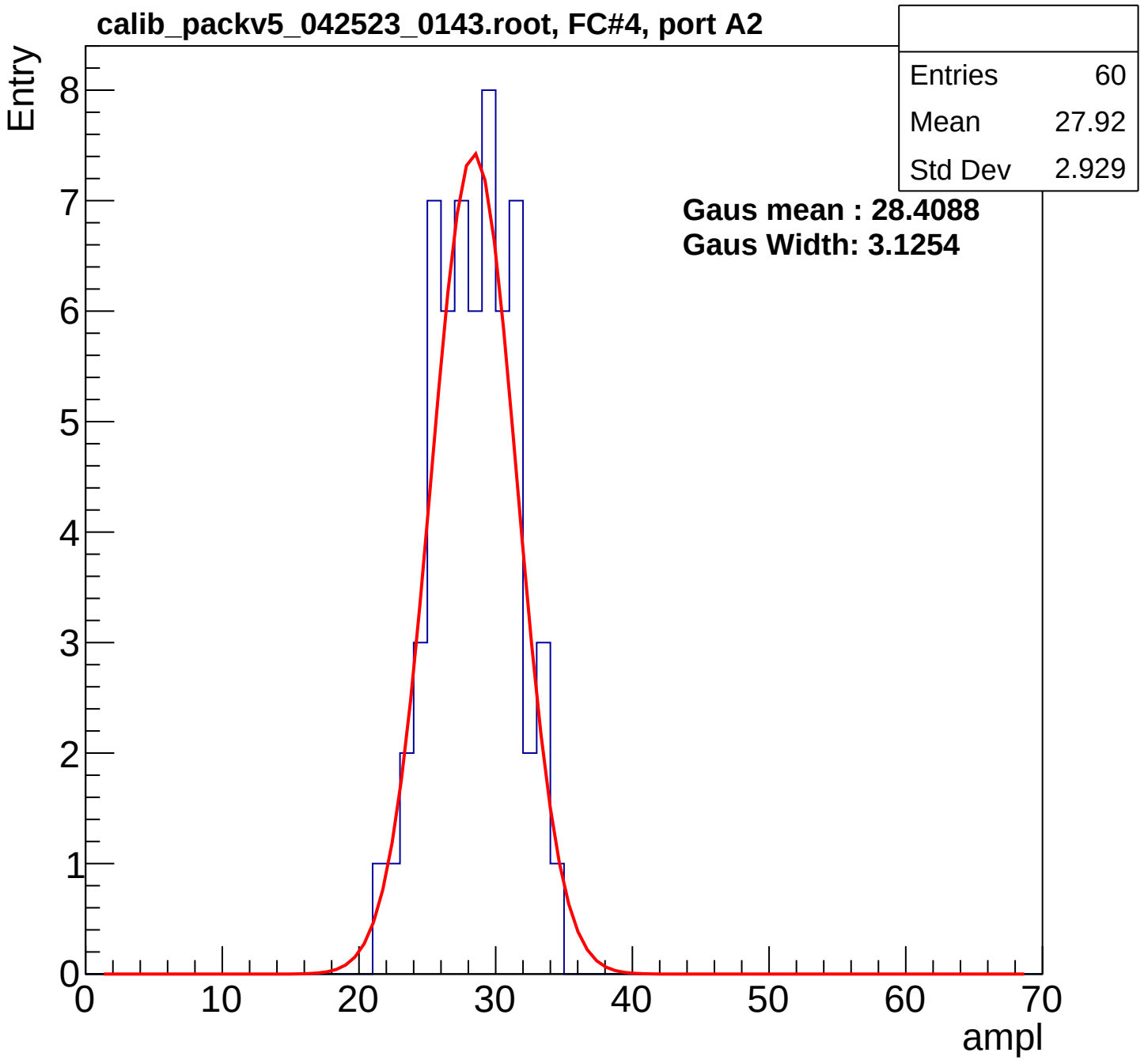

B1L100S, U5-ch91, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 49.66
Std Dev 3.87
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

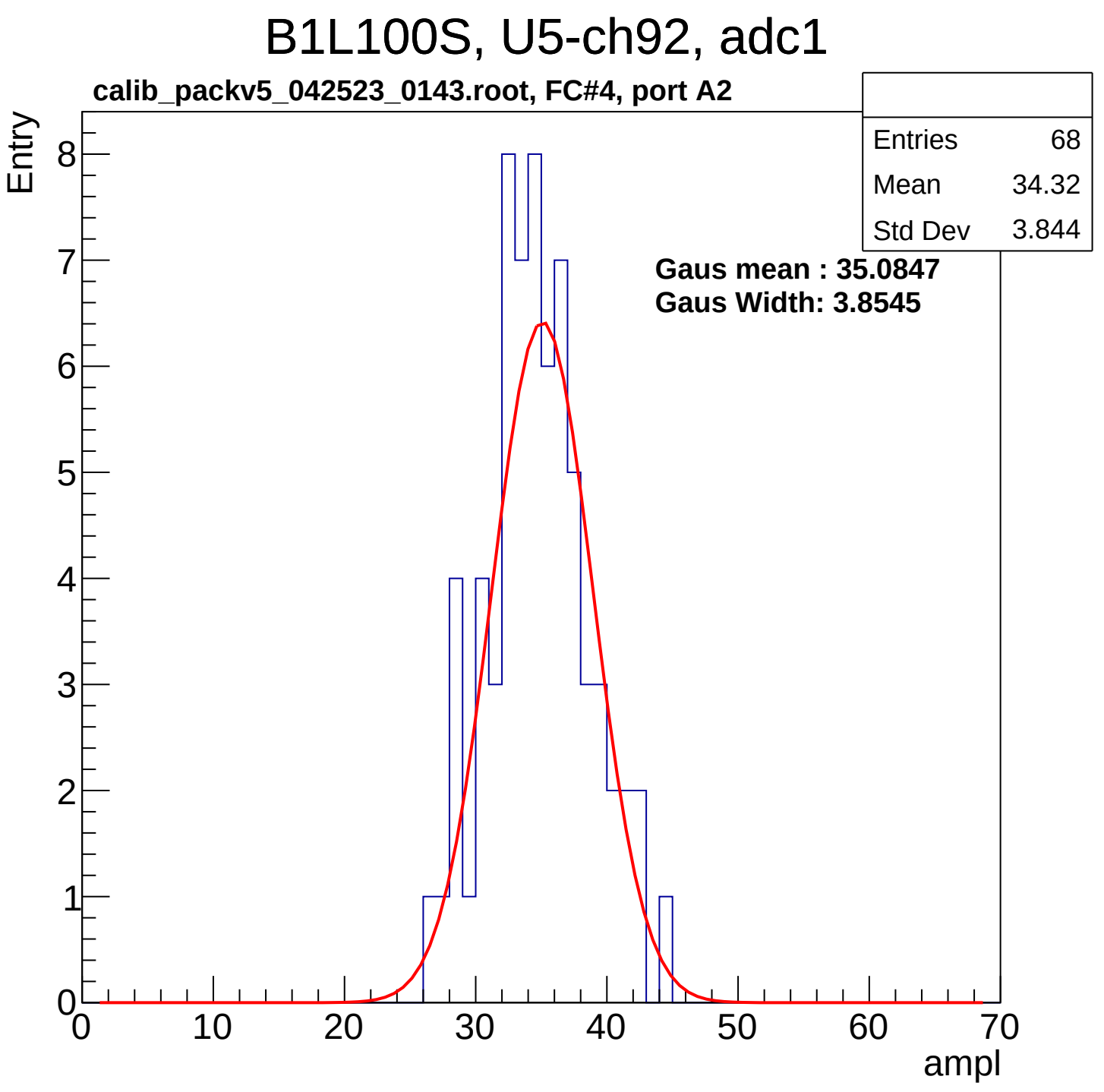

B1L100S, U5-ch91, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 55.13
Std Dev 3.532
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

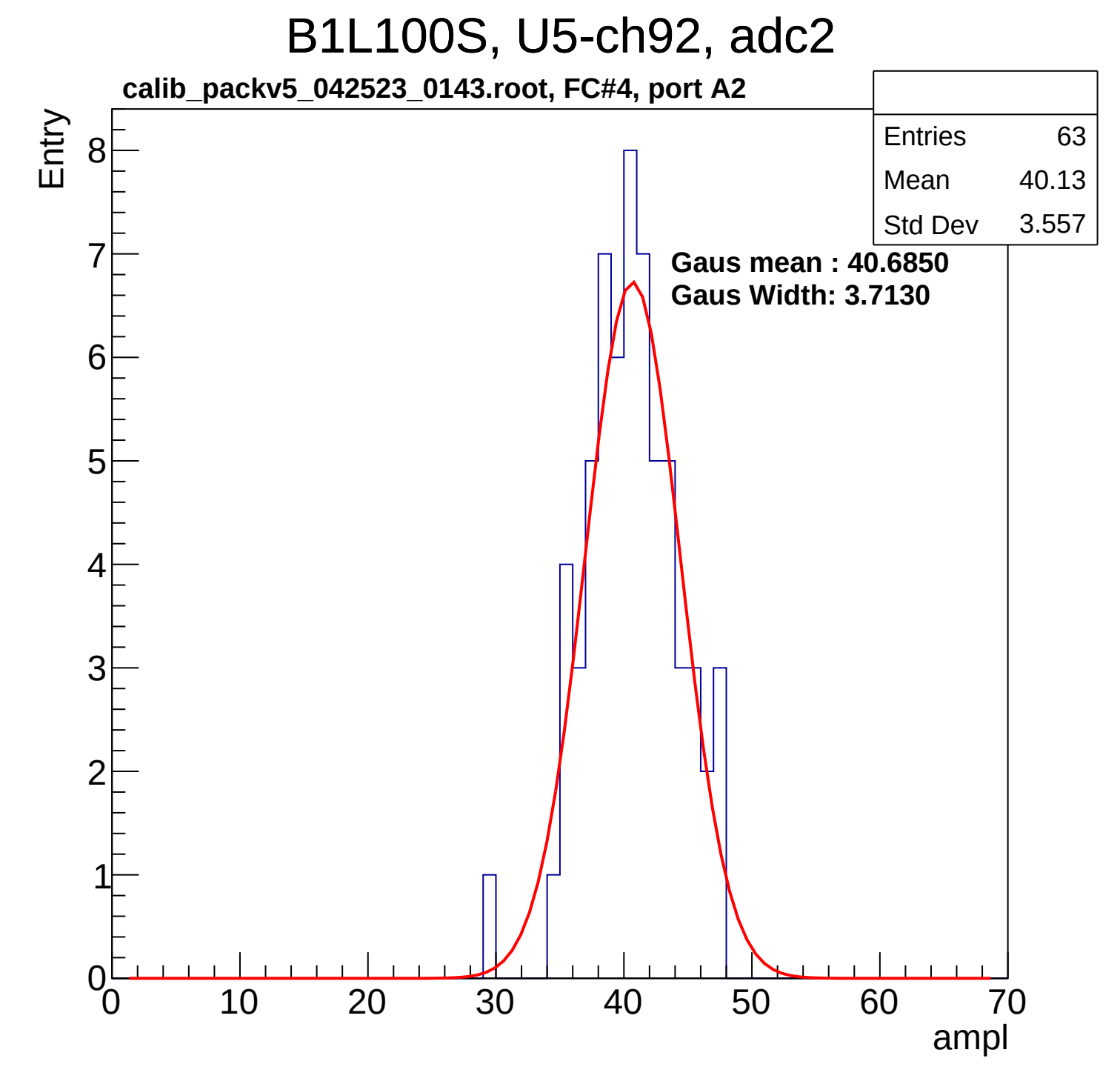

B1L100S, U5-ch91, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 52
Mean 58.44
Std Dev 8.63
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

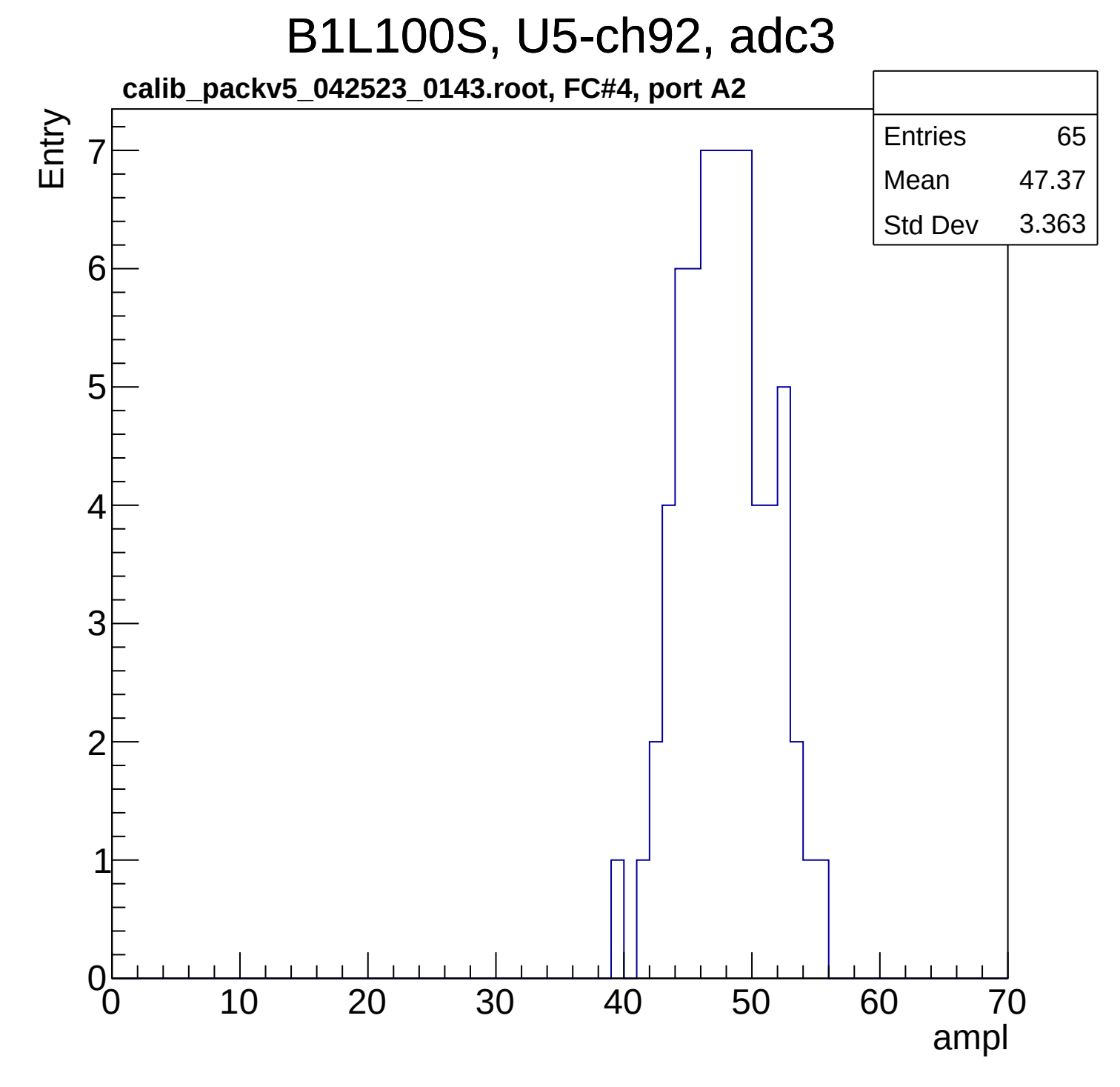

B1L100S, U5-ch91, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 4
Mean 62.5
Std Dev 0.5
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

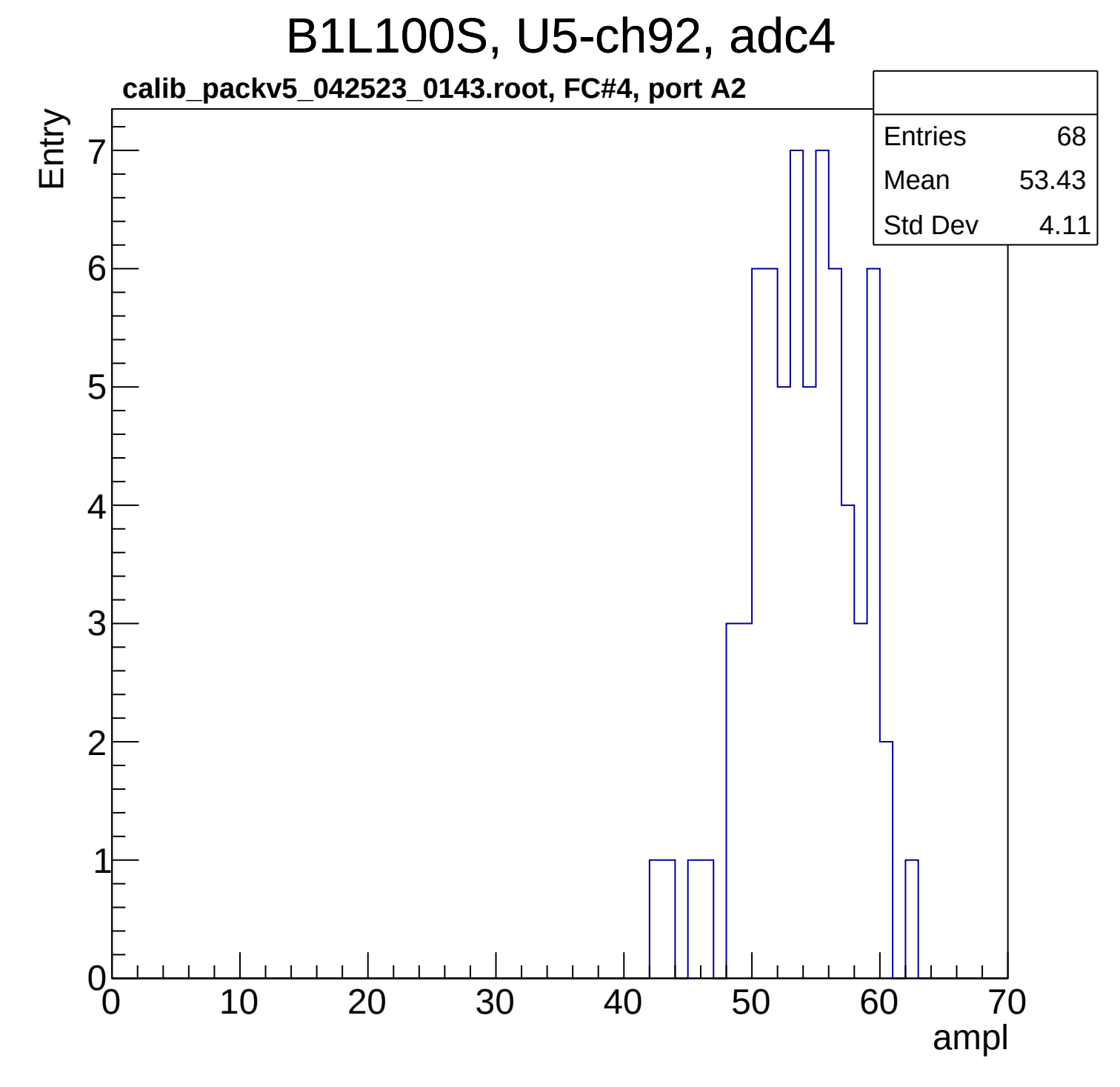

B1L100S, U5-ch91, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 10
Std Dev 10
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

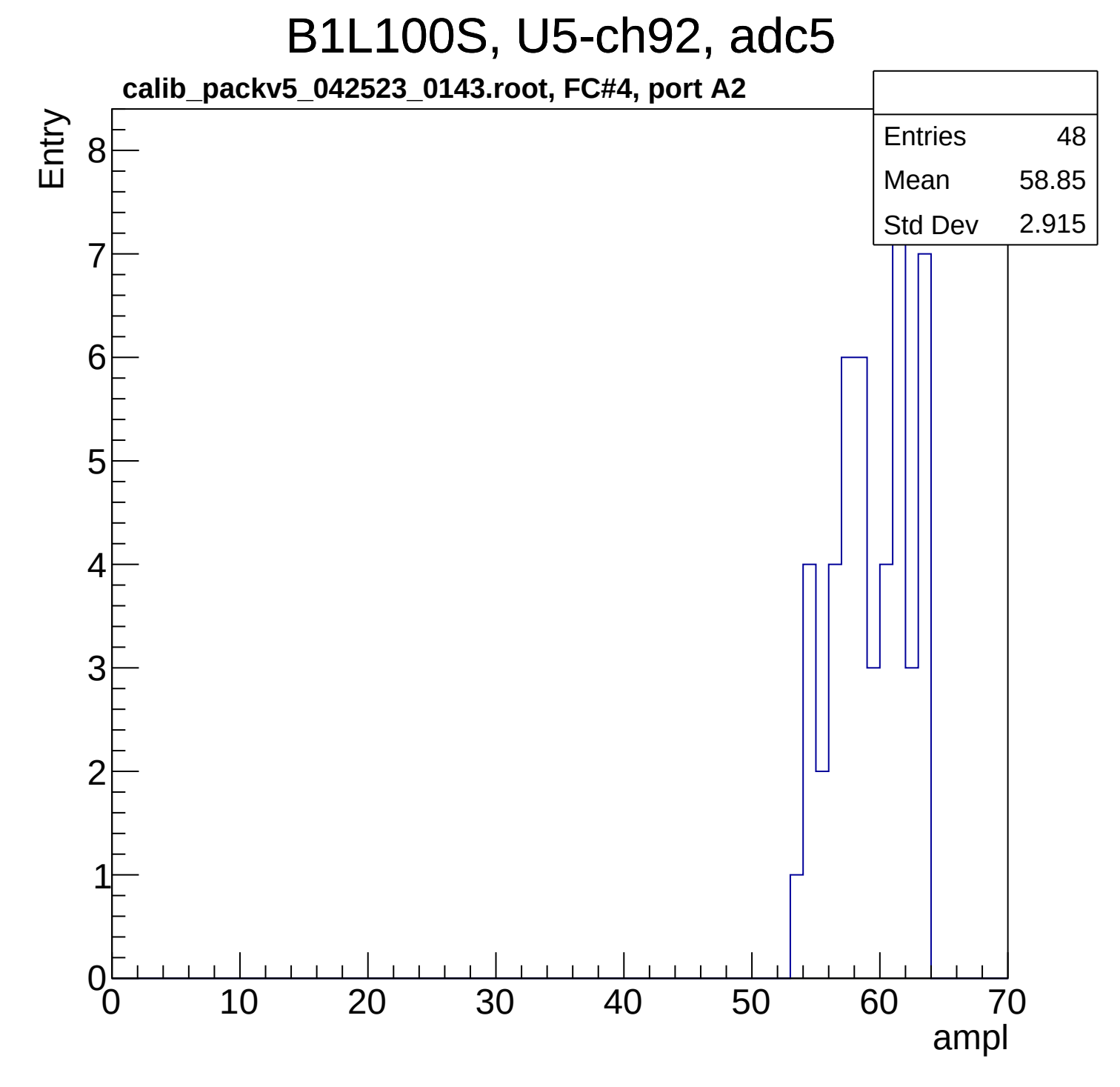

B1L100S, U5-ch92, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 27.92
Std Dev 2.929
Gaus mean : 28.4088
Gaus Width: 3.1254
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

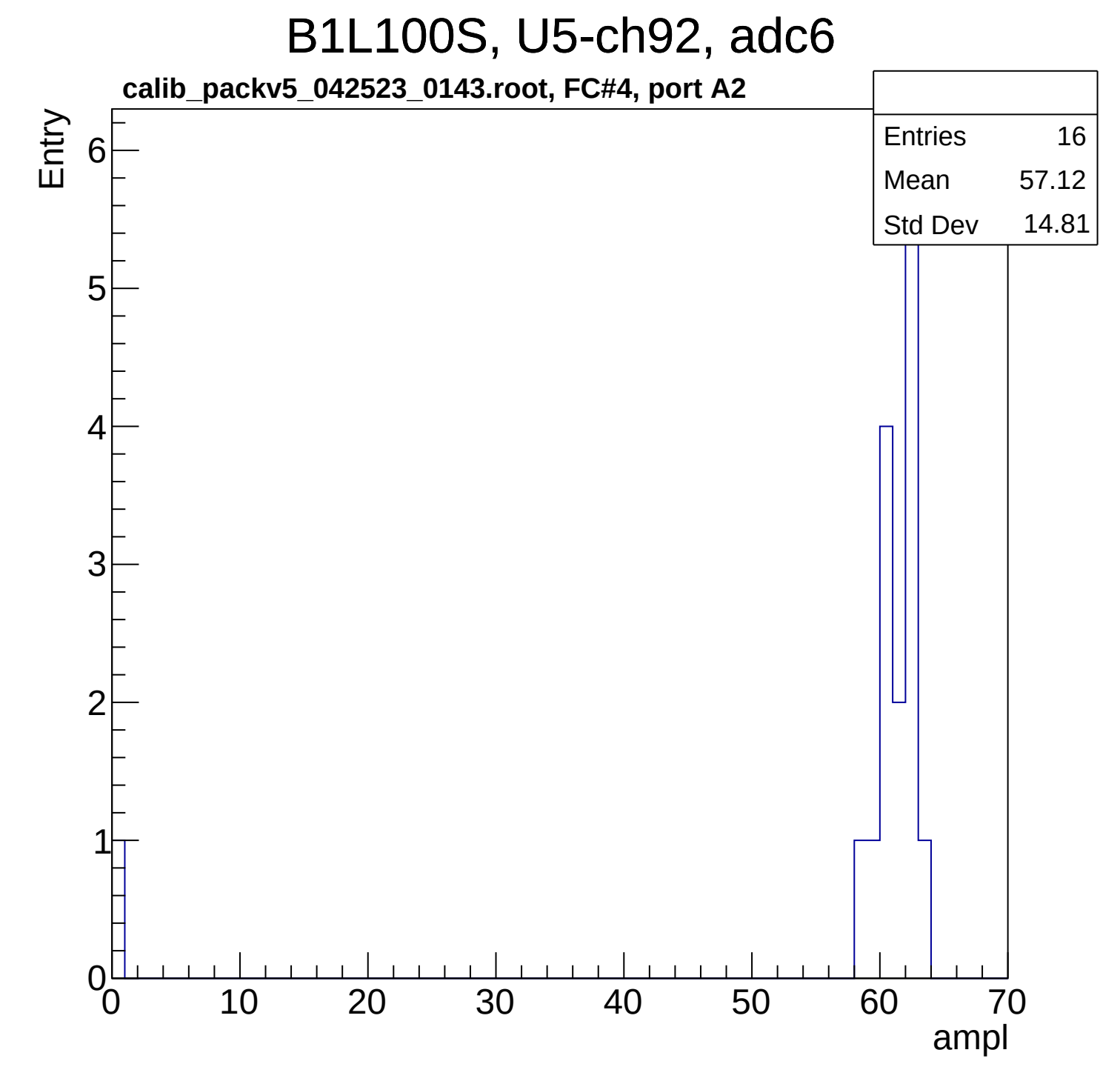

B1L100S, U5-ch92, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 34.32
Std Dev 3.844
Gaus mean : 35.0847
Gaus Width: 3.8545
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

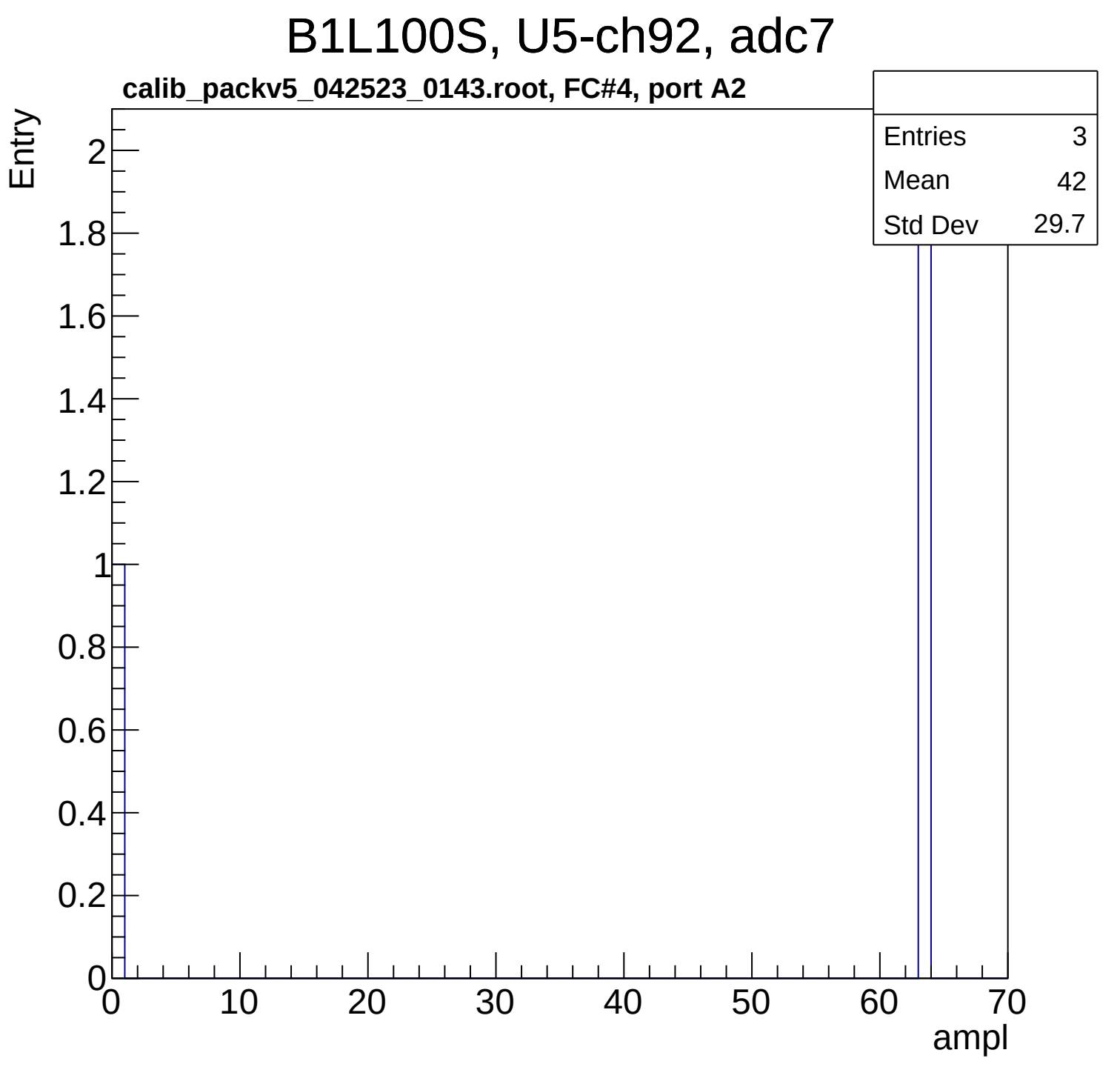

B1L100S, U5-ch92, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 40.13
Std Dev 3.557
Gaus mean : 40.6850
Gaus Width: 3.7130
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

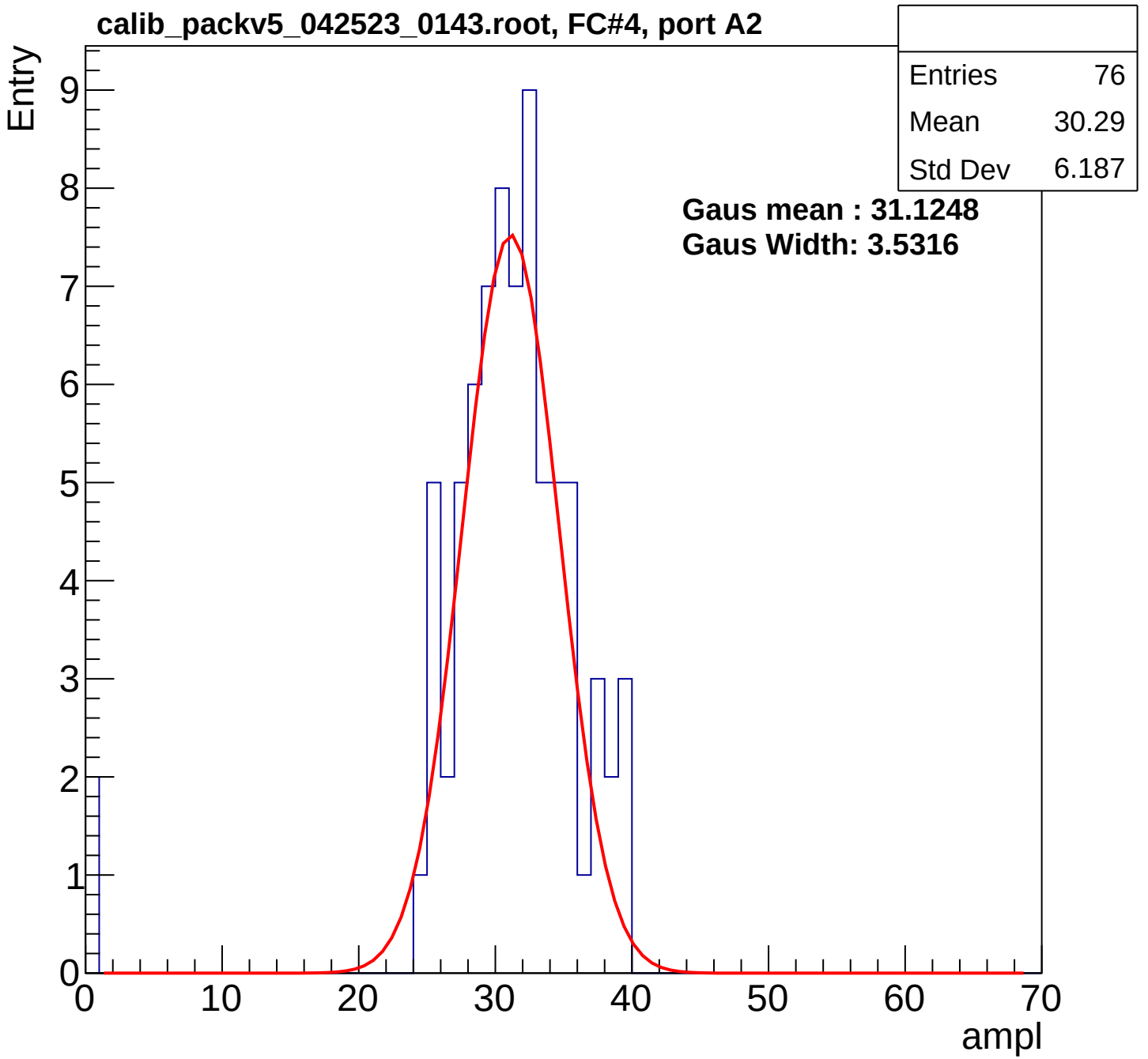

B1L100S, U5-ch92, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 47.37
Std Dev 3.363
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

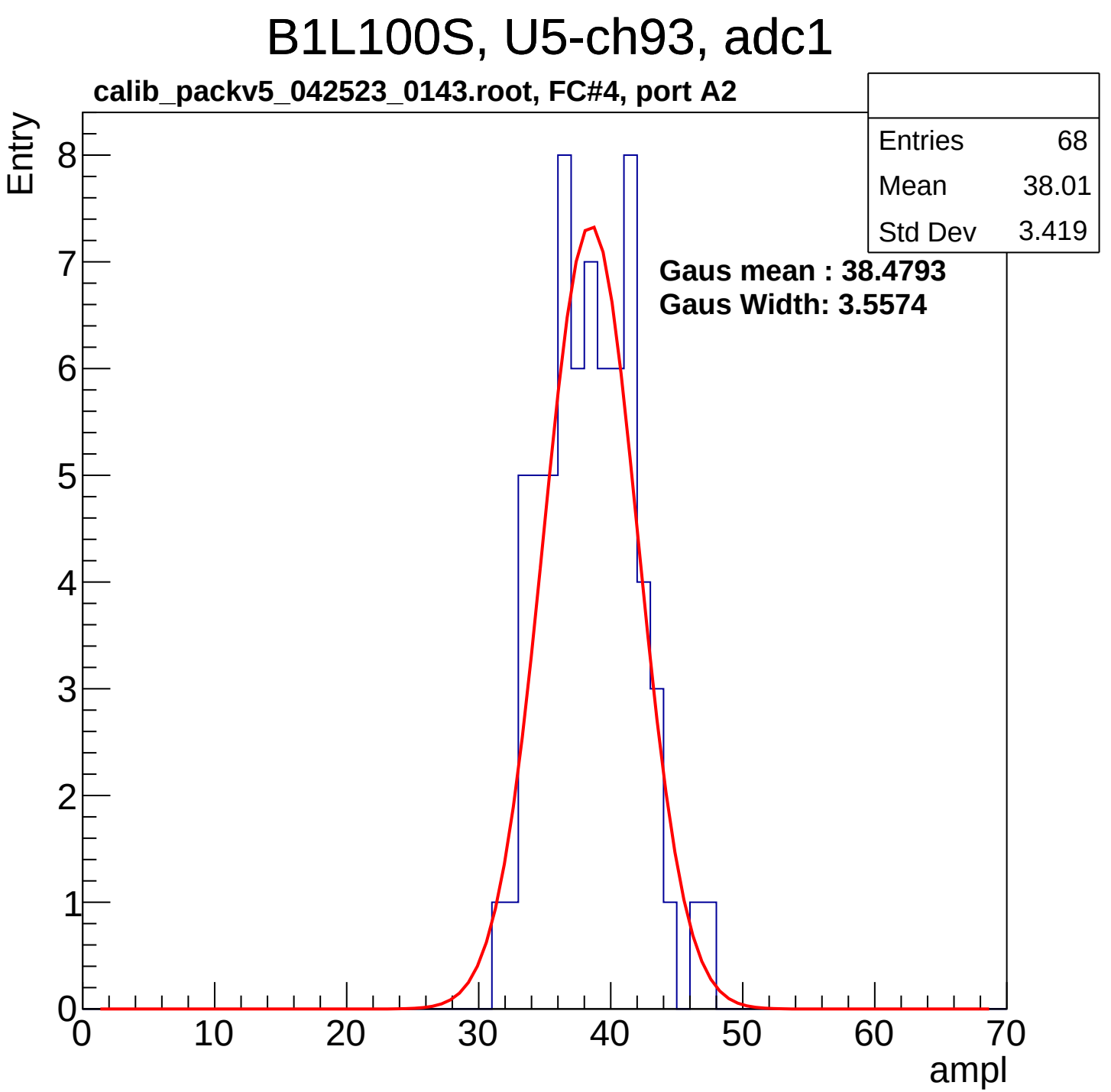

B1L100S, U5-ch92, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 53.43
Std Dev 4.11
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

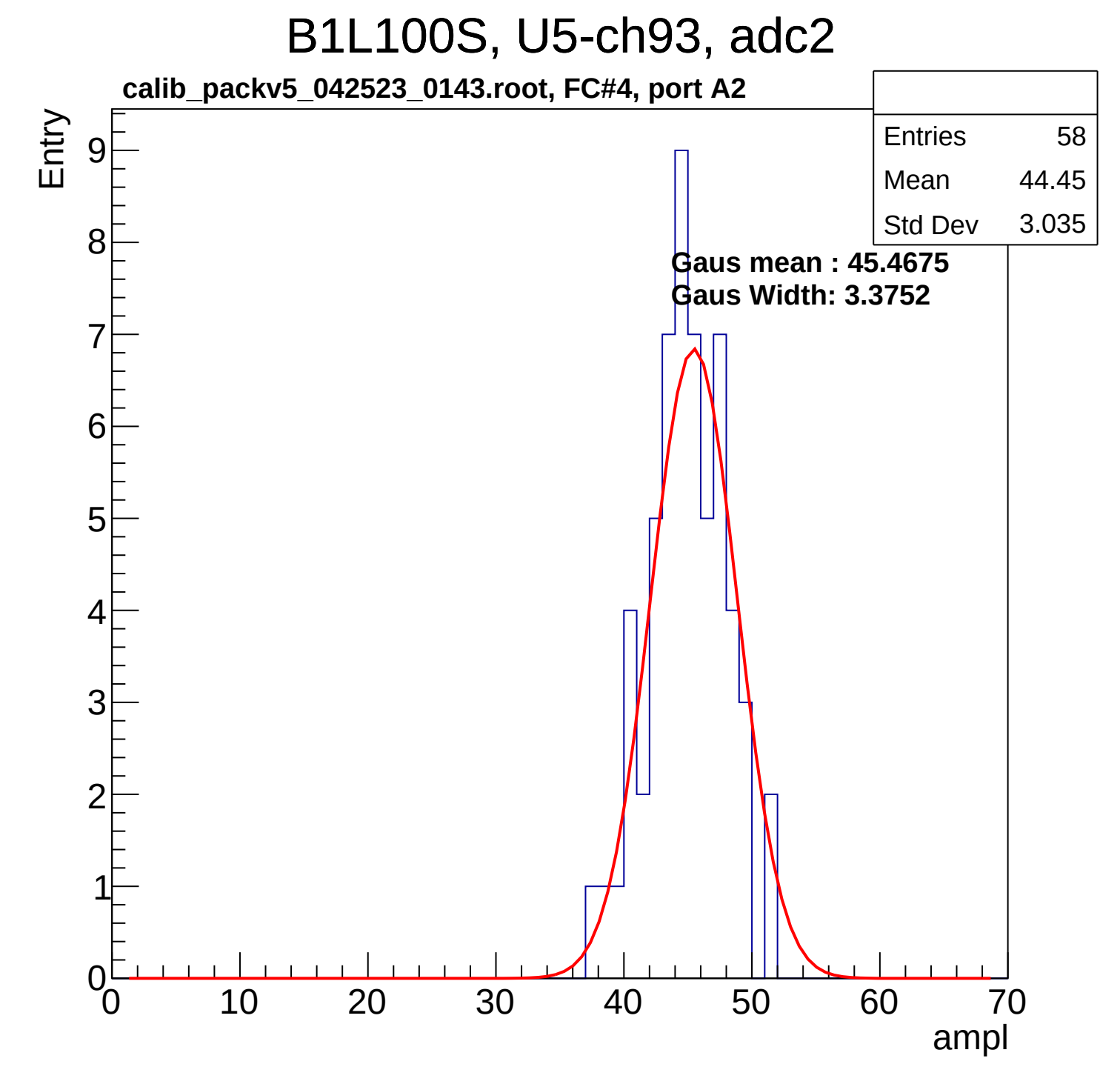

B1L100S, U5-ch92, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 48
Mean 58.85
Std Dev 2.915
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

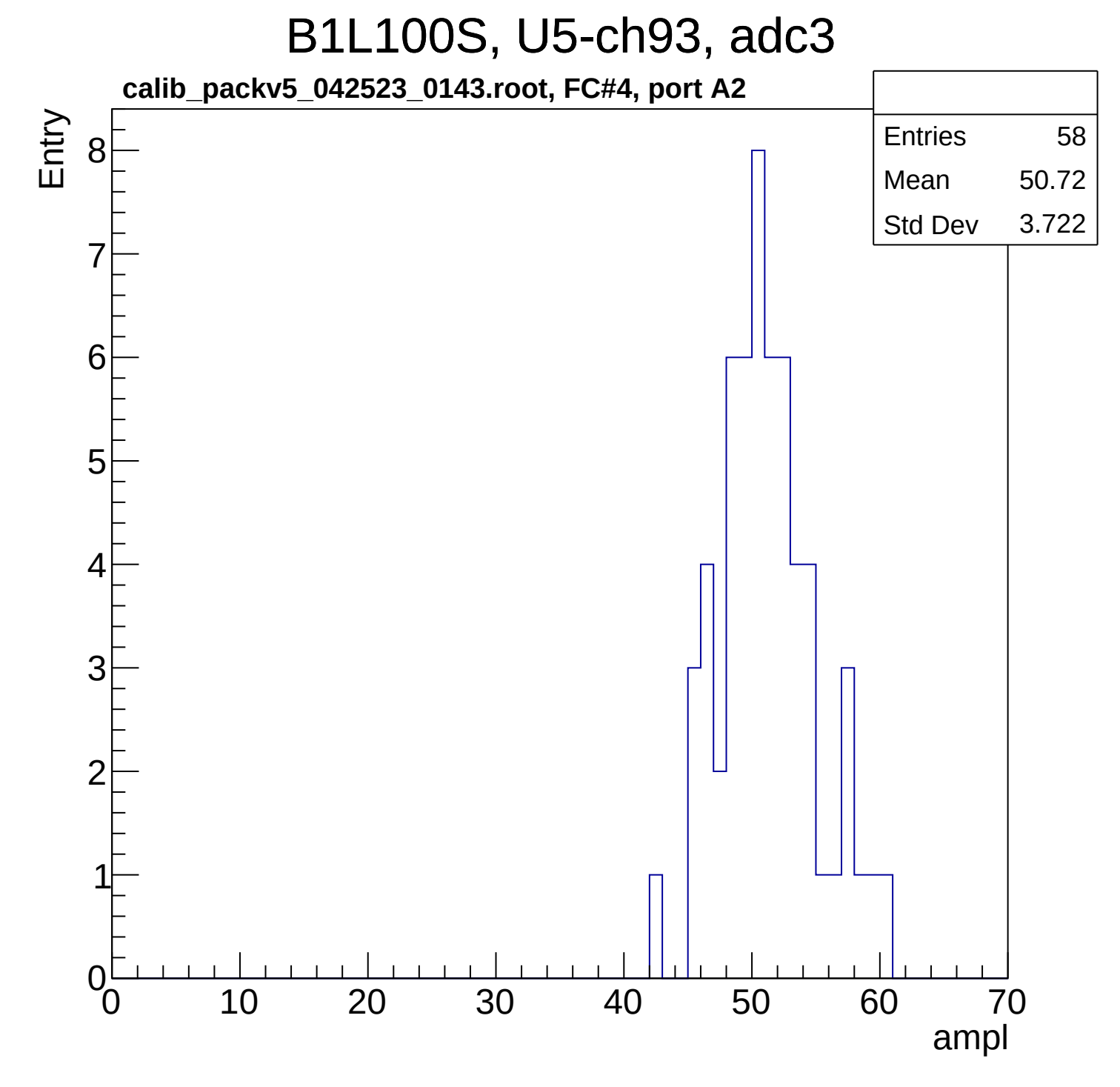

B1L100S, U5-ch92, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 16
Mean 57.12
Std Dev 14.81
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

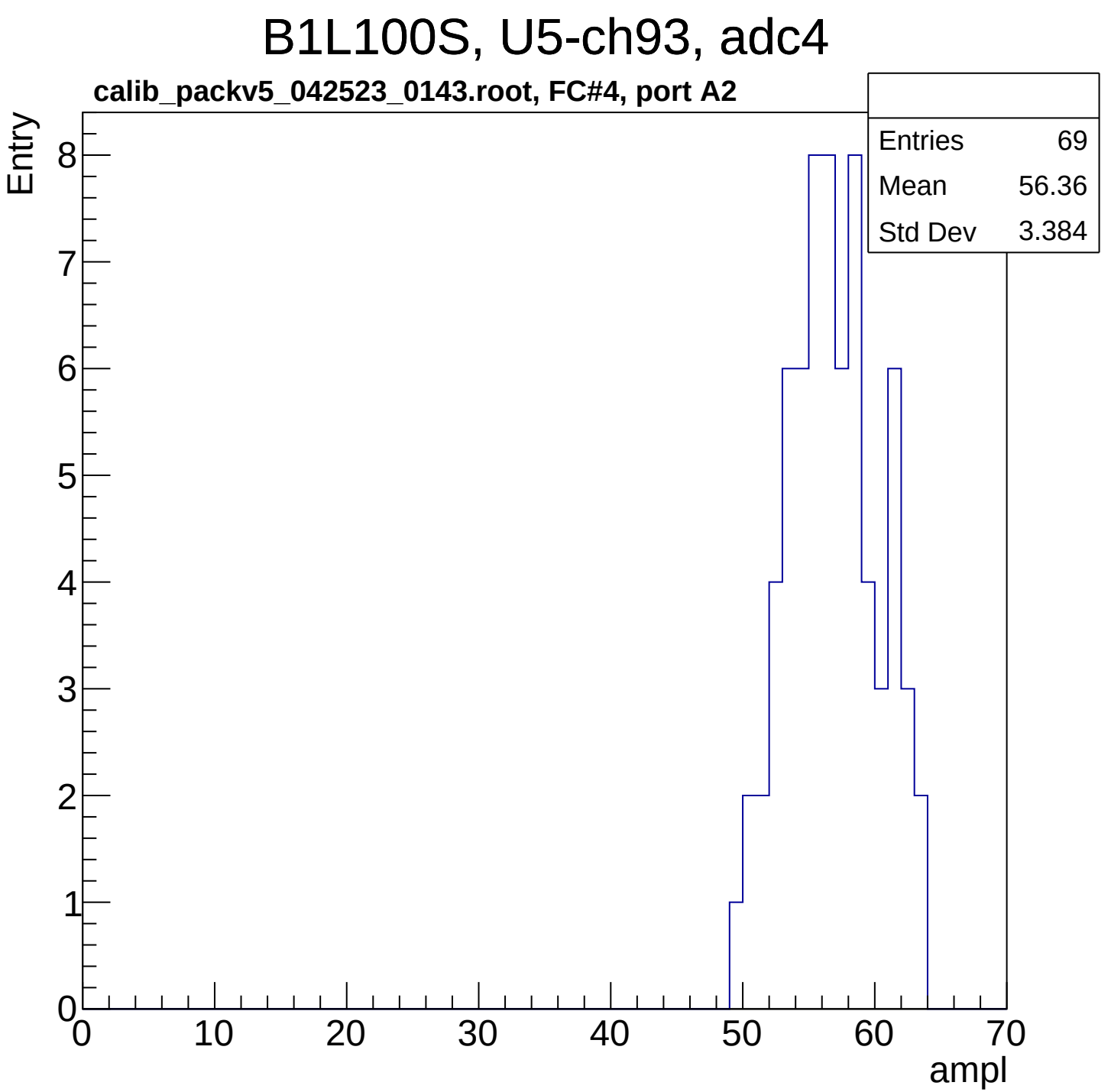

B1L100S, U5-ch92, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 42
Std Dev 29.7
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

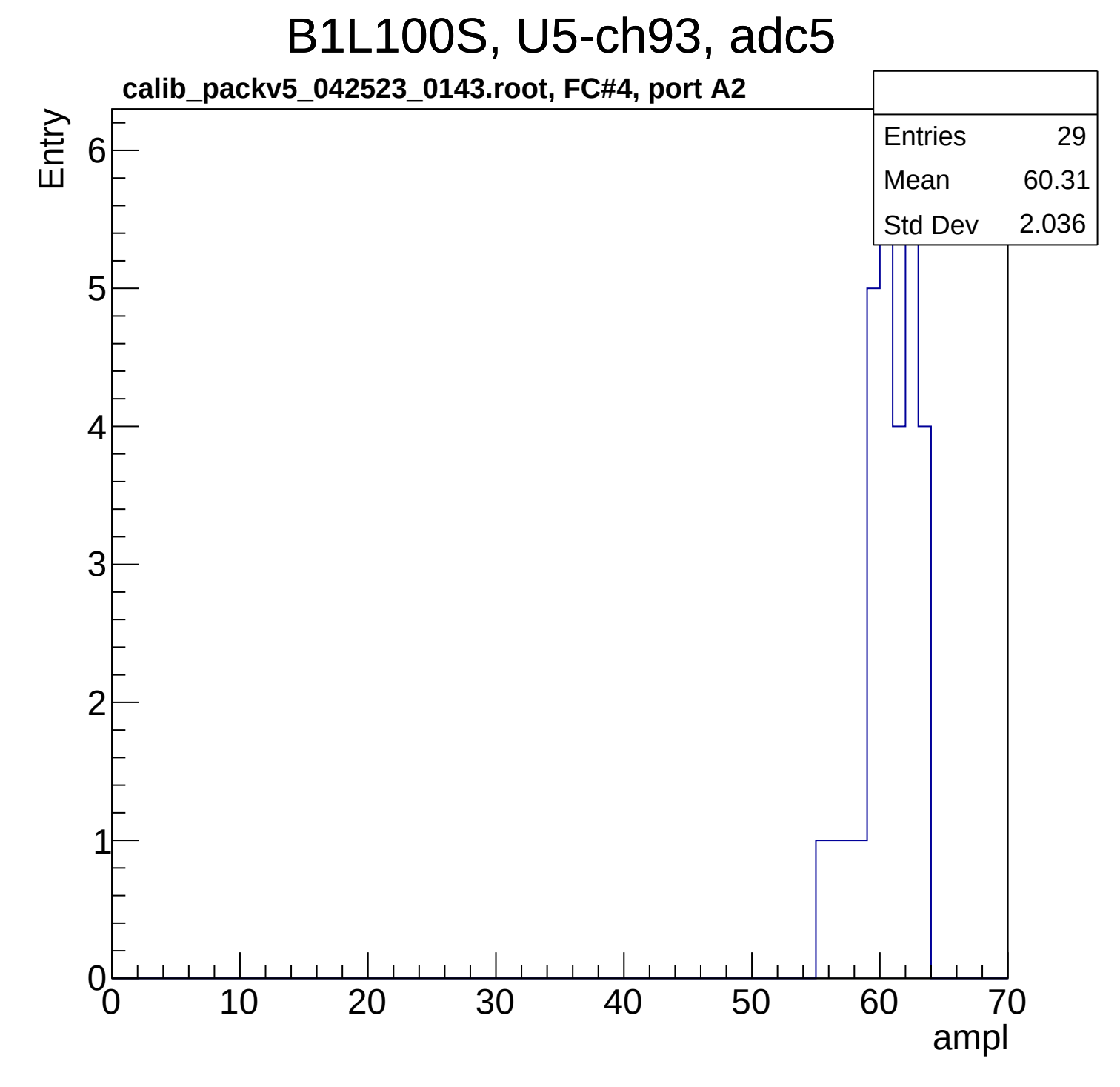

B1L100S, U5-ch93, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 76
Mean 30.29
Std Dev 6.187
Gaus mean : 31.1248
Gaus Width: 3.5316
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

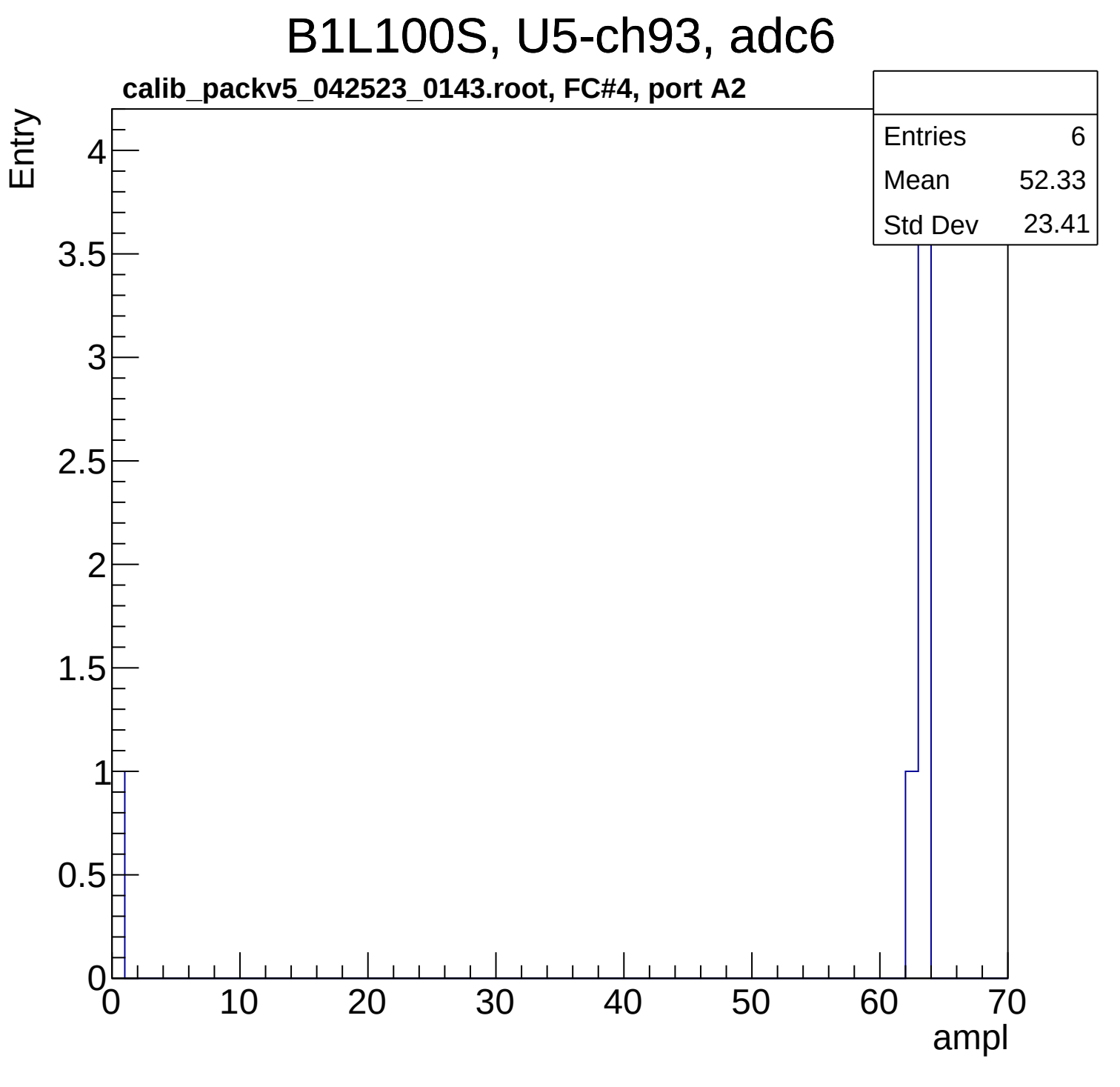

B1L100S, U5-ch93, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 38.01
Std Dev 3.419
Gaus mean : 38.4793
Gaus Width: 3.5574
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

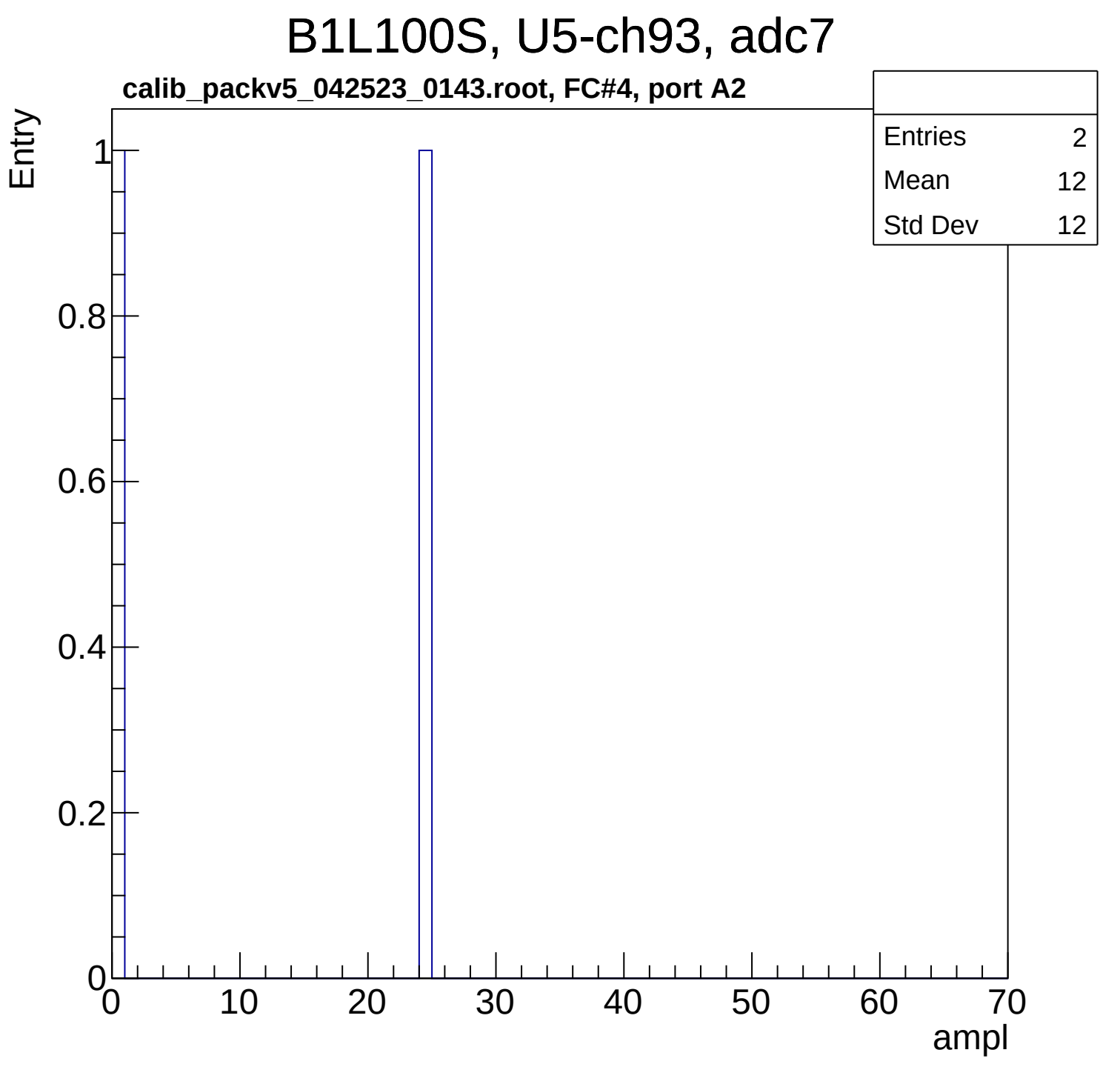

B1L100S, U5-ch93, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 44.45
Std Dev 3.035
Gaus mean : 45.4675
Gaus Width: 3.3752
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

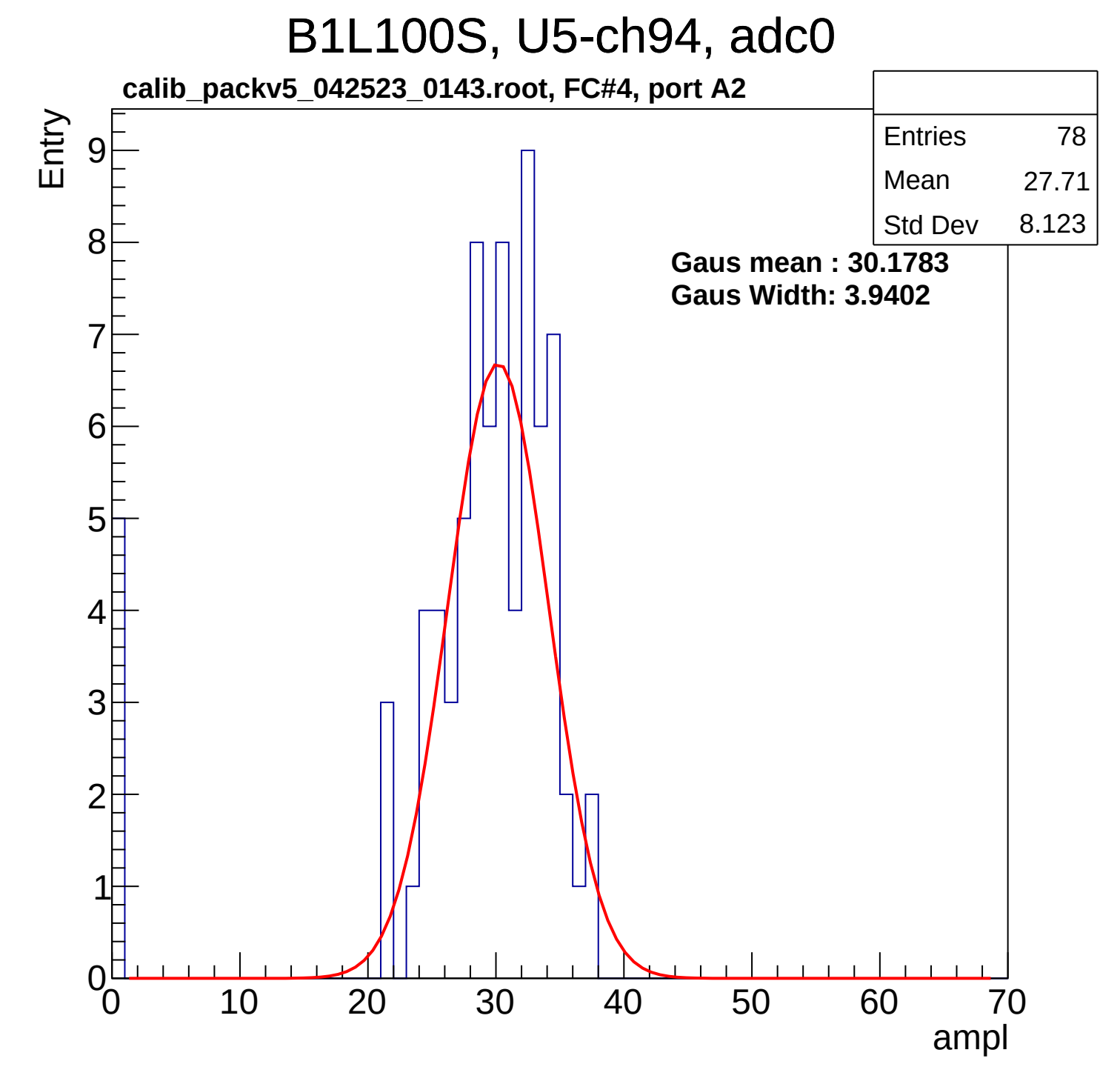

B1L100S, U5-ch93, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 50.72
Std Dev 3.722
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

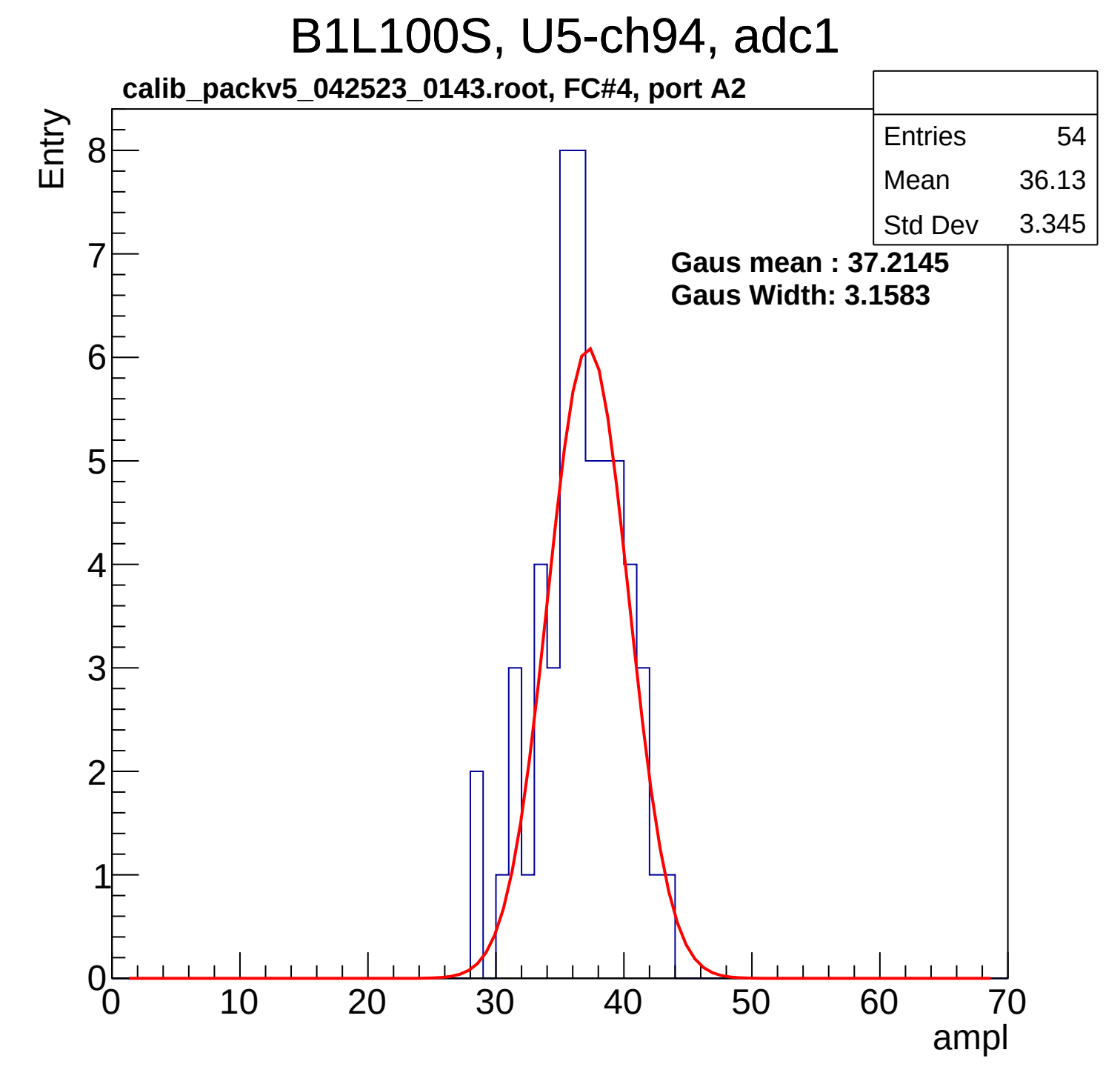

B1L100S, U5-ch93, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 56.36
Std Dev 3.384
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

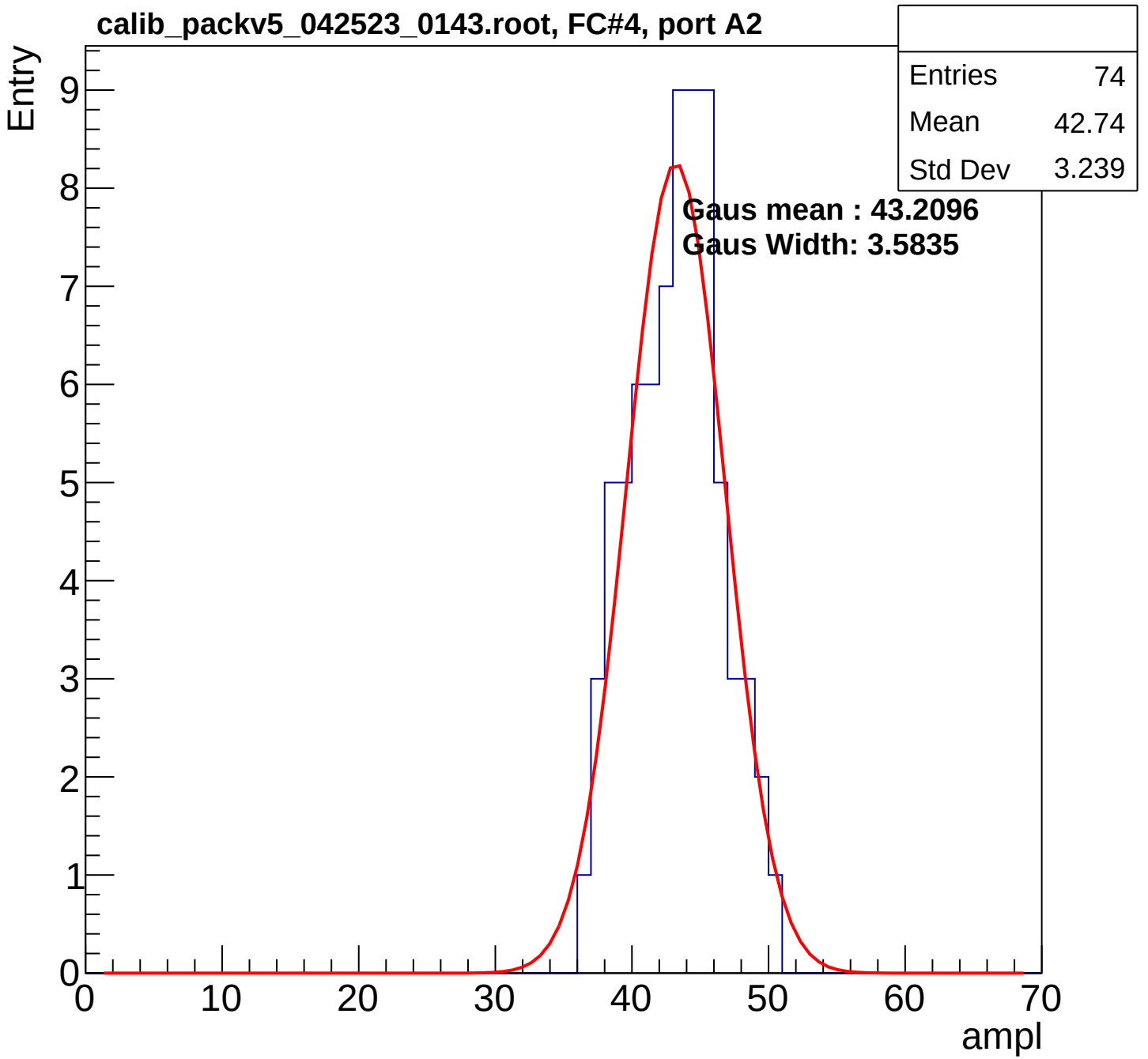

B1L100S, U5-ch93, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 29
Mean 60.31
Std Dev 2.036
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

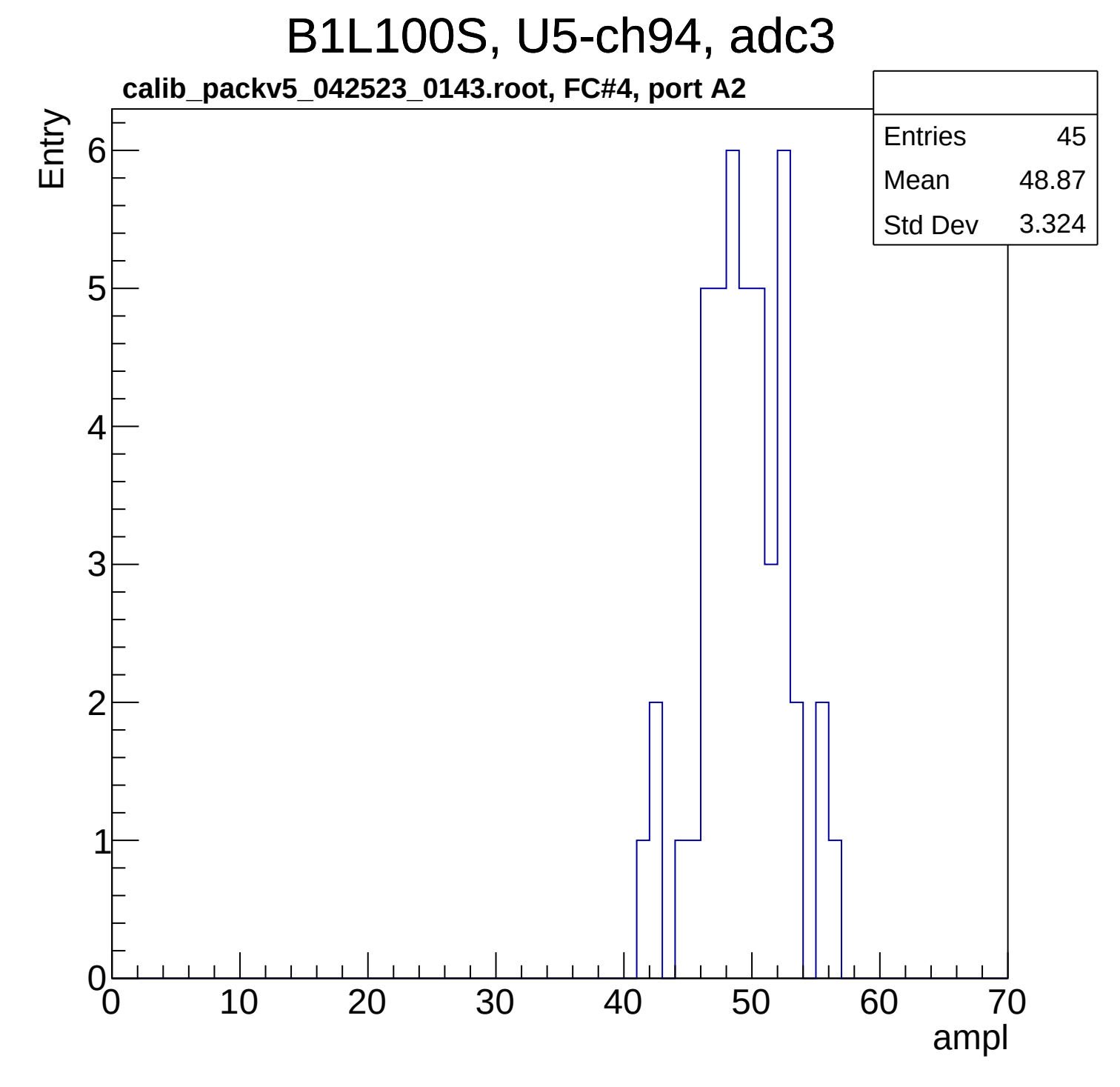

B1L100S, U5-ch93, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 6
Mean 52.33
Std Dev 23.41
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

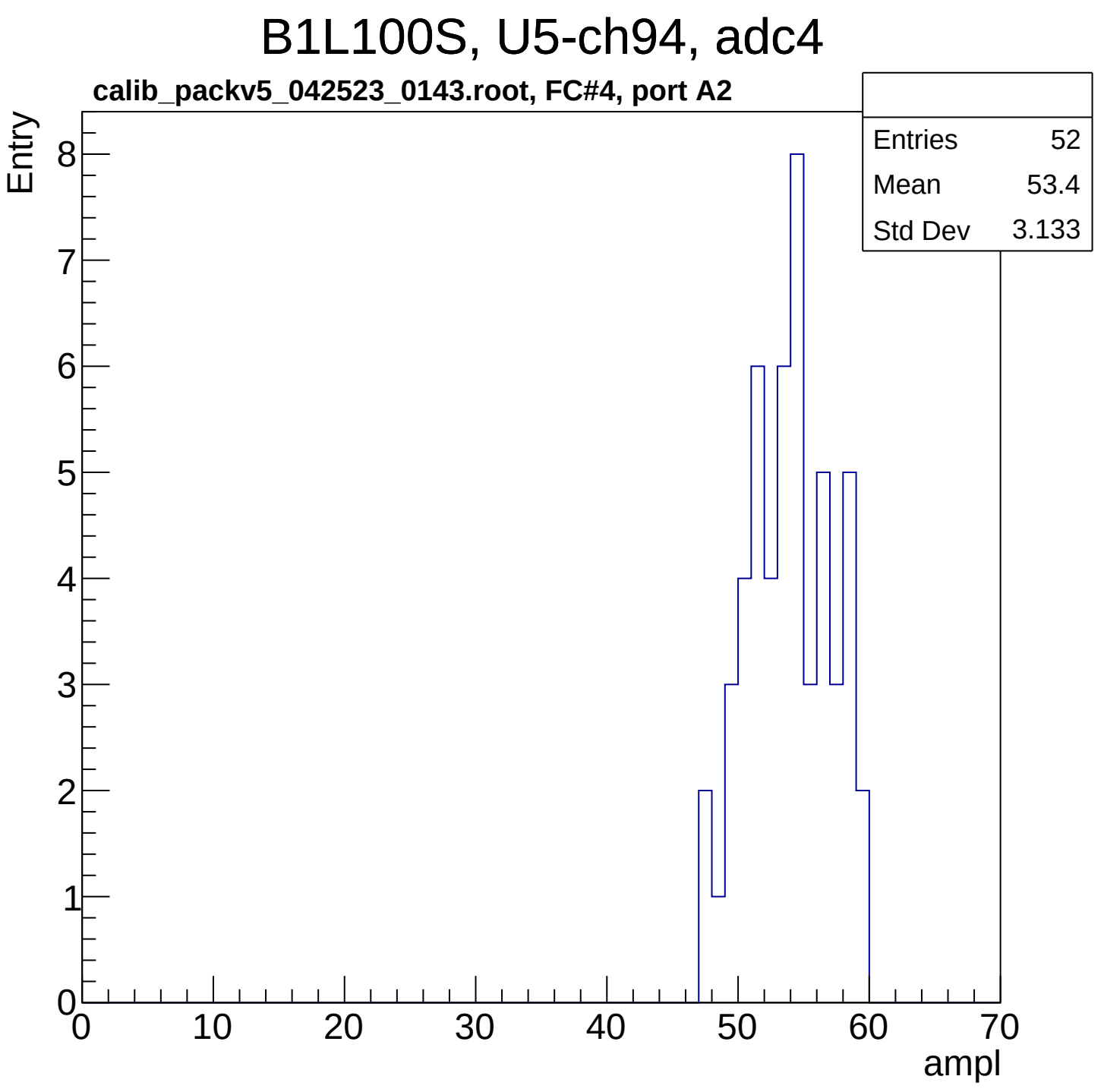

B1L100S, U5-ch93, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 12
Std Dev 12
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

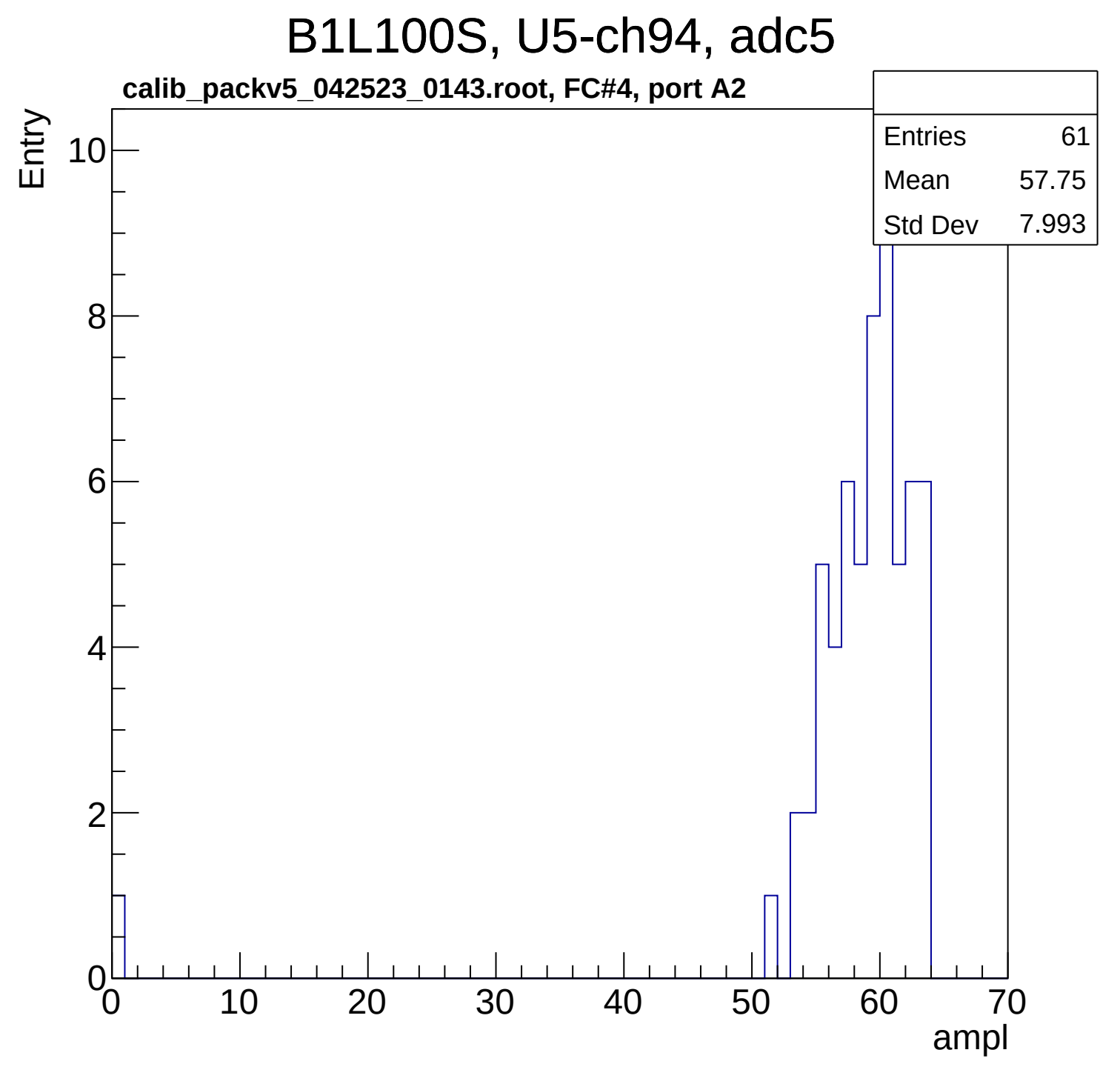

B1L100S, U5-ch94, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 78
Mean 27.71
Std Dev 8.123
Gaus mean : 30.1783
Gaus Width: 3.9402
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

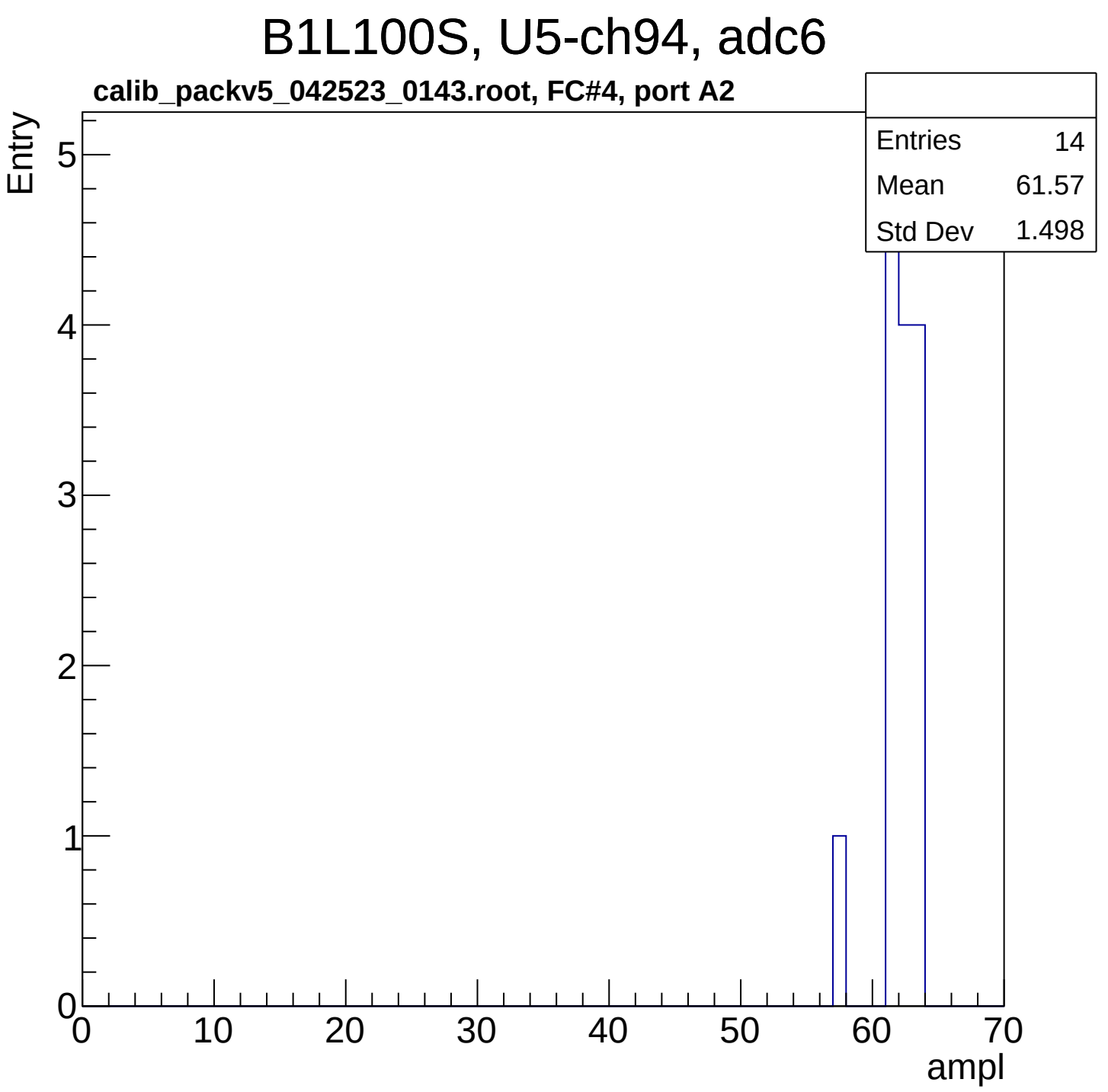

B1L100S, U5-ch94, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 36.13
Std Dev 3.345
Gaus mean : 37.2145
Gaus Width: 3.1583
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

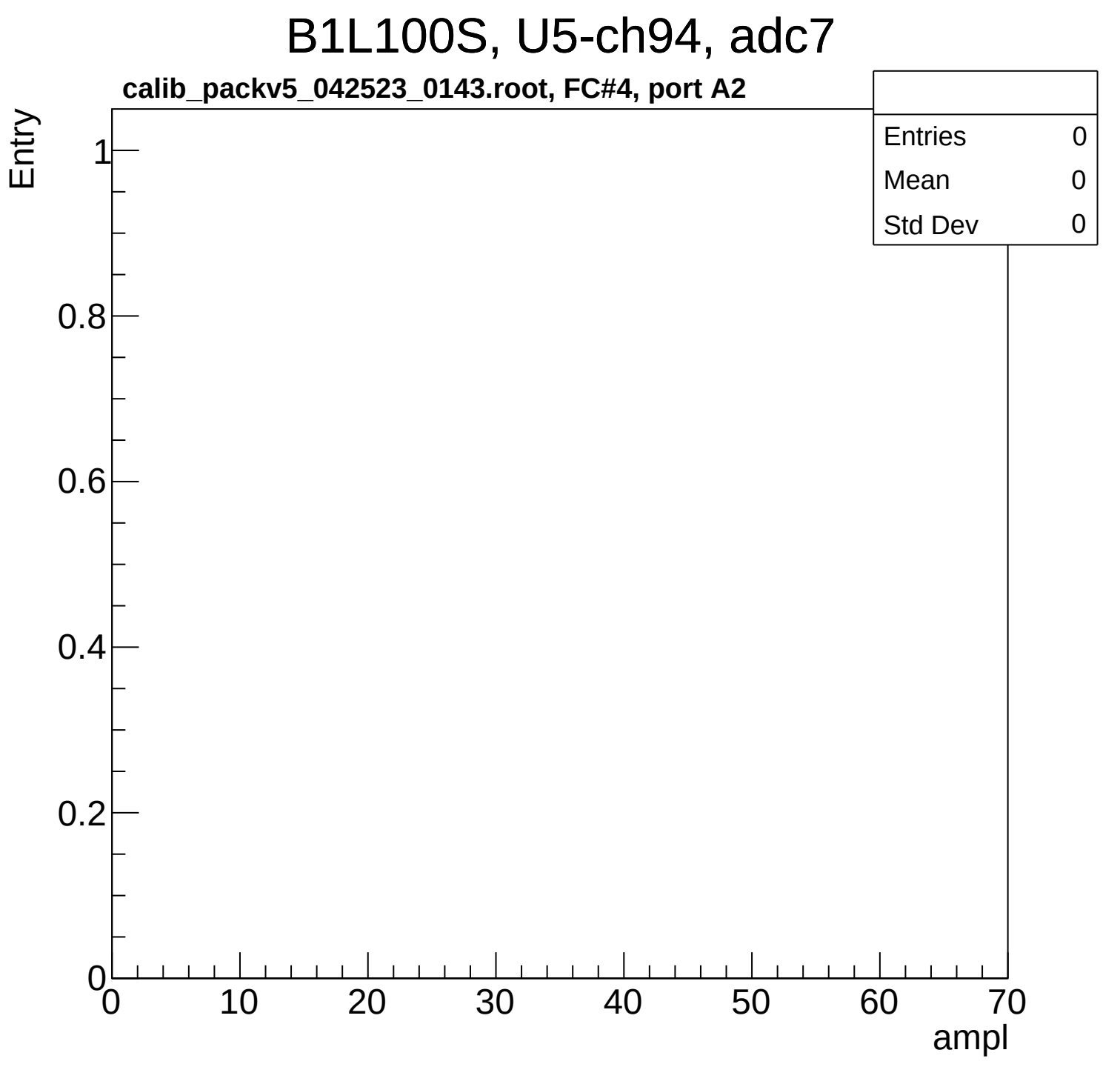

B1L100S, U5-ch94, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 74
Mean 42.74
Std Dev 3.239
Gaus mean : 43.2096
Gaus Width: 3.5835
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

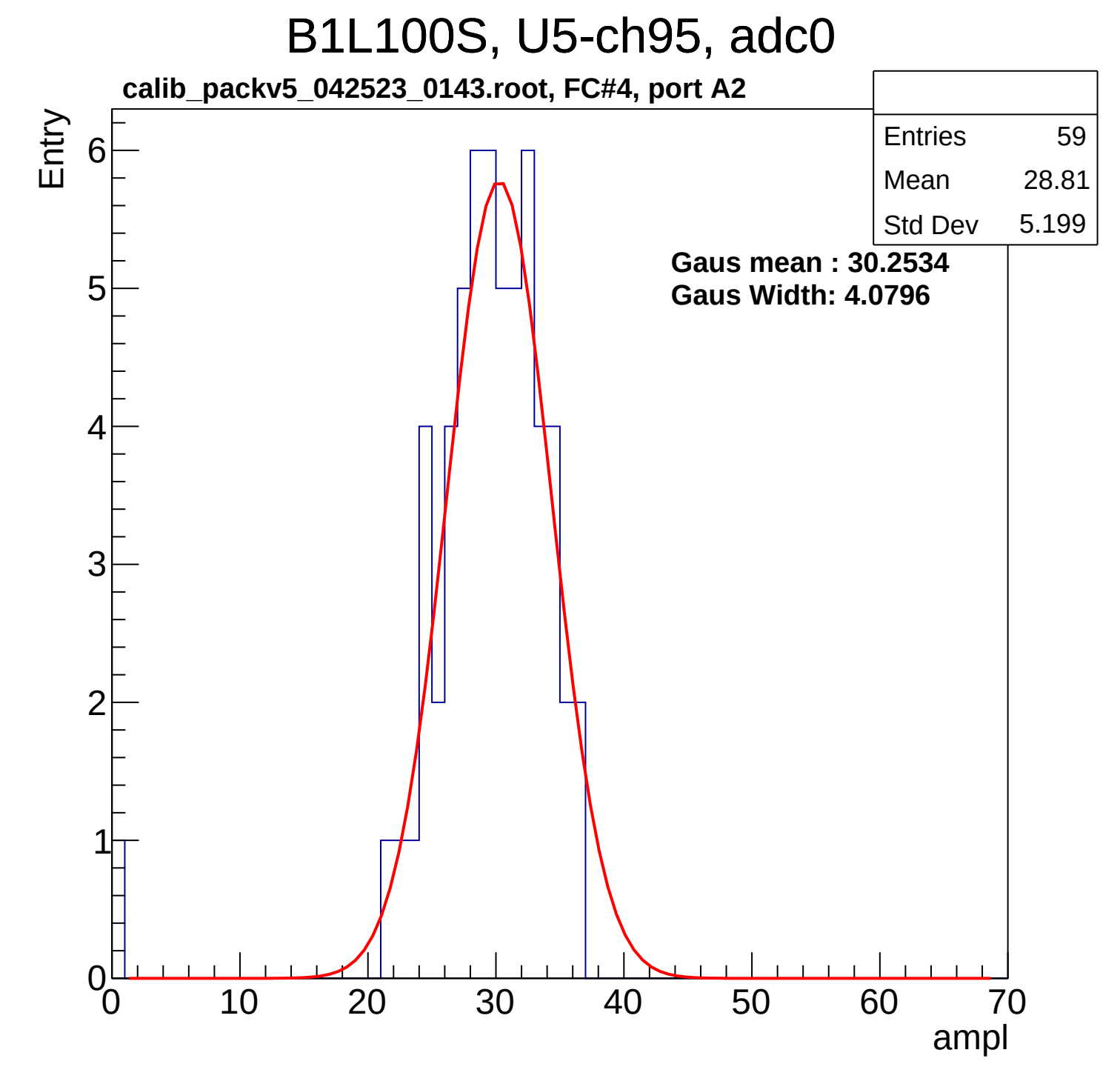

B1L100S, U5-ch94, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 45
Mean 48.87
Std Dev 3.324
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

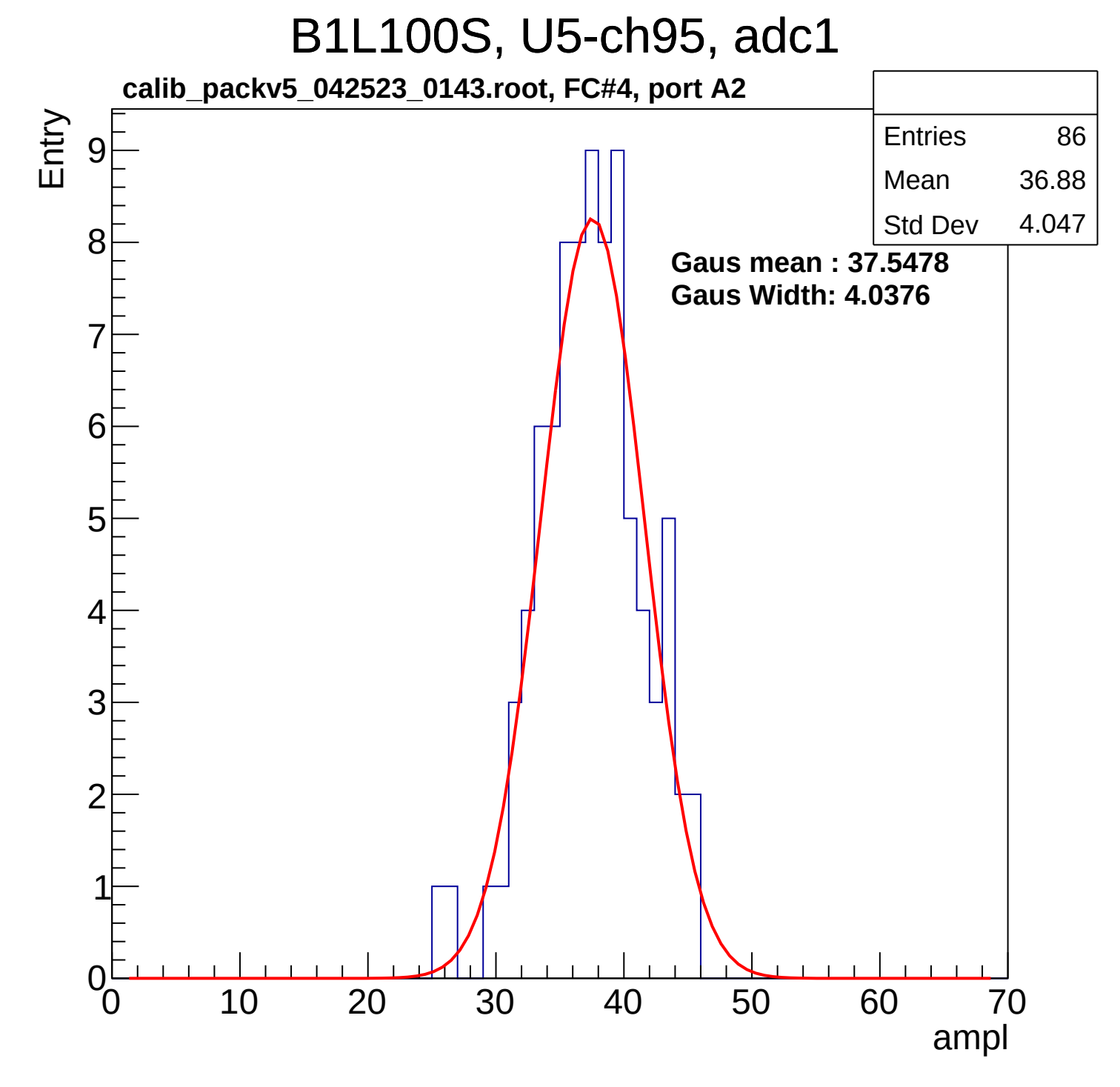

B1L100S, U5-ch94, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 52
Mean 53.4
Std Dev 3.133
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

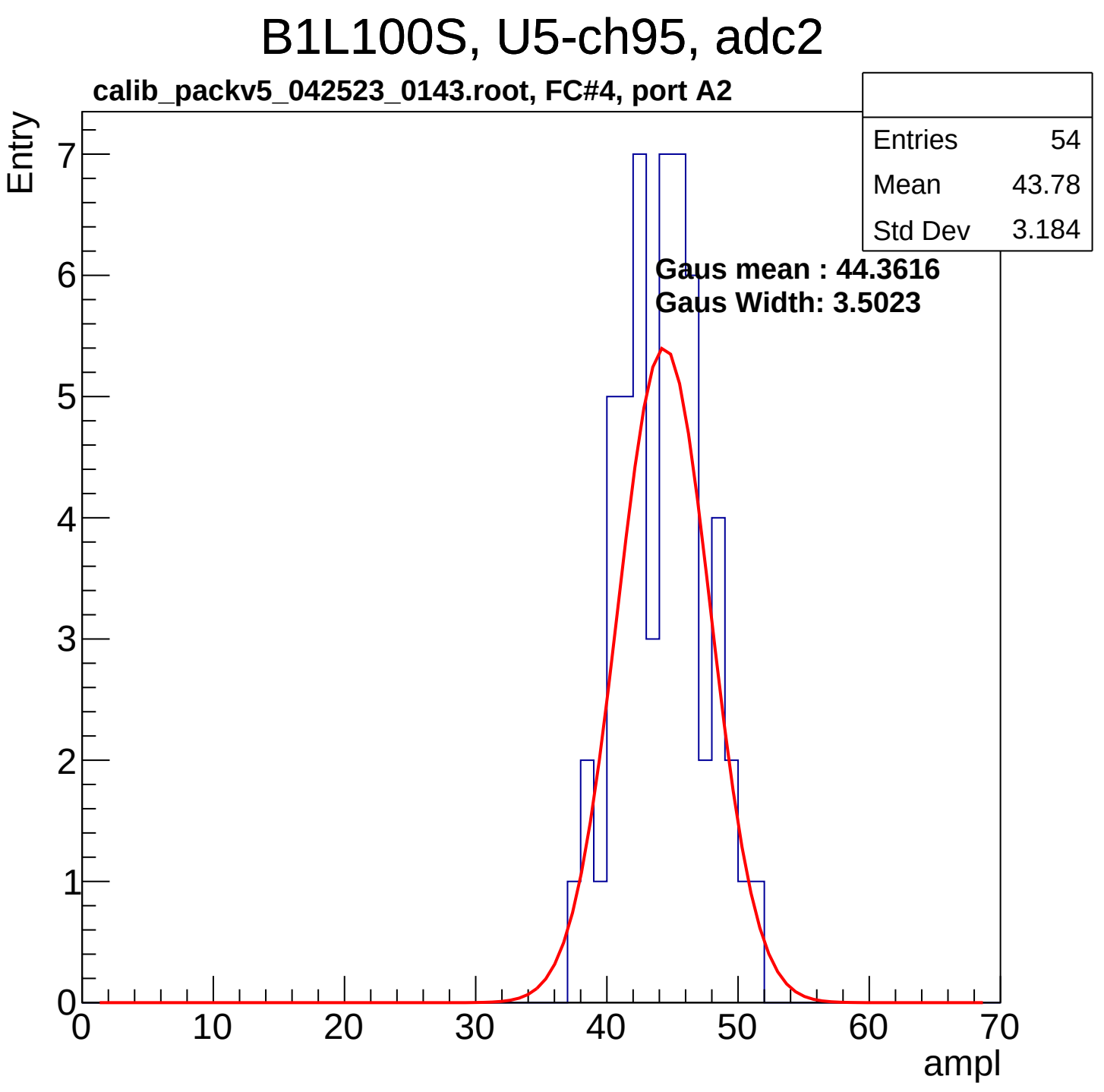

B1L100S, U5-ch94, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 57.75
Std Dev 7.993
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

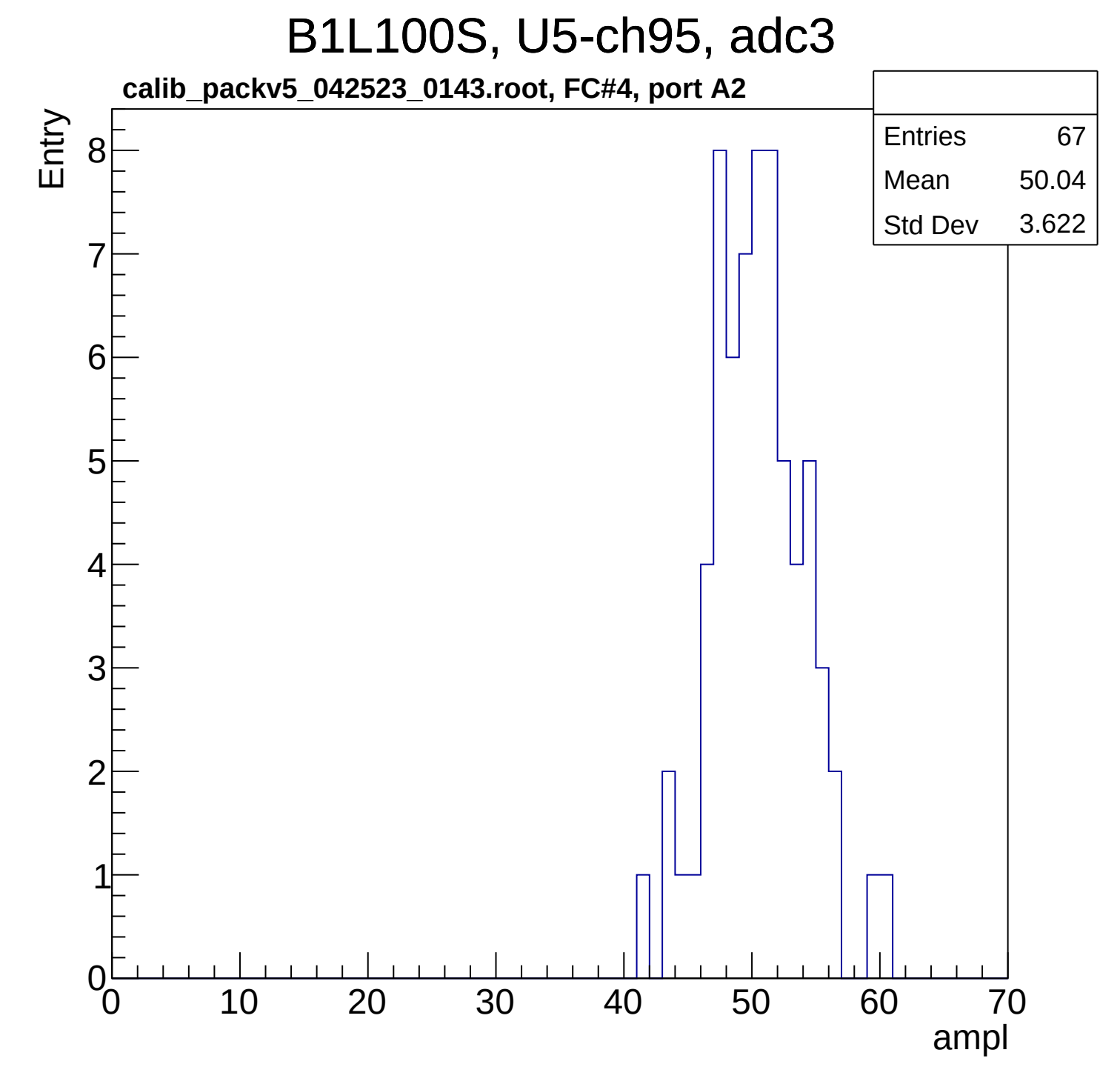

B1L100S, U5-ch94, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 14
Mean 61.57
Std Dev 1.498
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

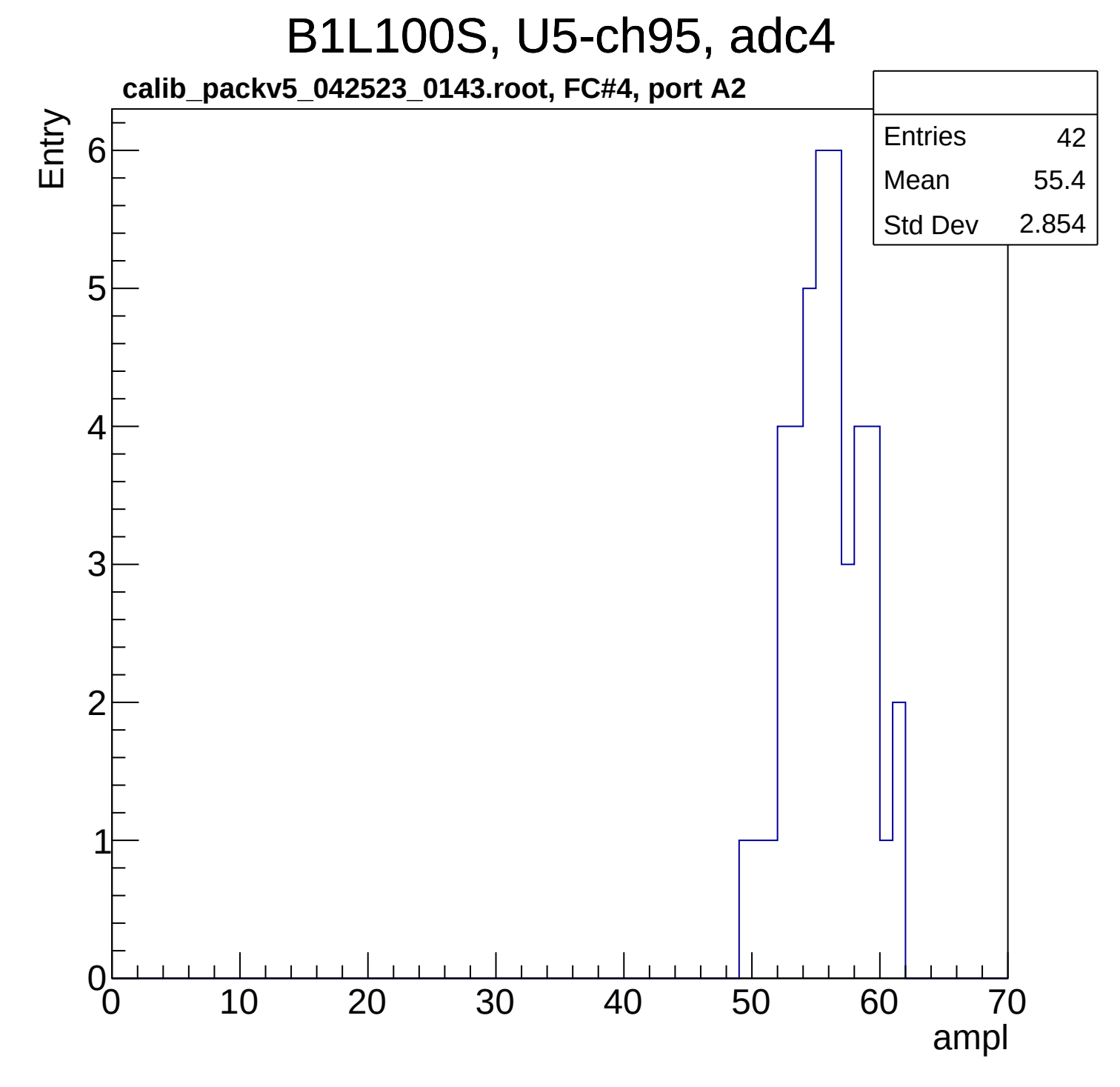

B1L100S, U5-ch94, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch95, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 28.81
Std Dev 5.199
Gaus mean : 30.2534
Gaus Width: 4.0796
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L100S, U5-ch95, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 86
Mean 36.88
Std Dev 4.047
Gaus mean : 37.5478
Gaus Width: 4.0376
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch95, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 43.78
Std Dev 3.184
Gaus mean : 44.3616
Gaus Width: 3.5023
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U5-ch95, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 50.04
Std Dev 3.622
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch95, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 42
Mean 55.4
Std Dev 2.854
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
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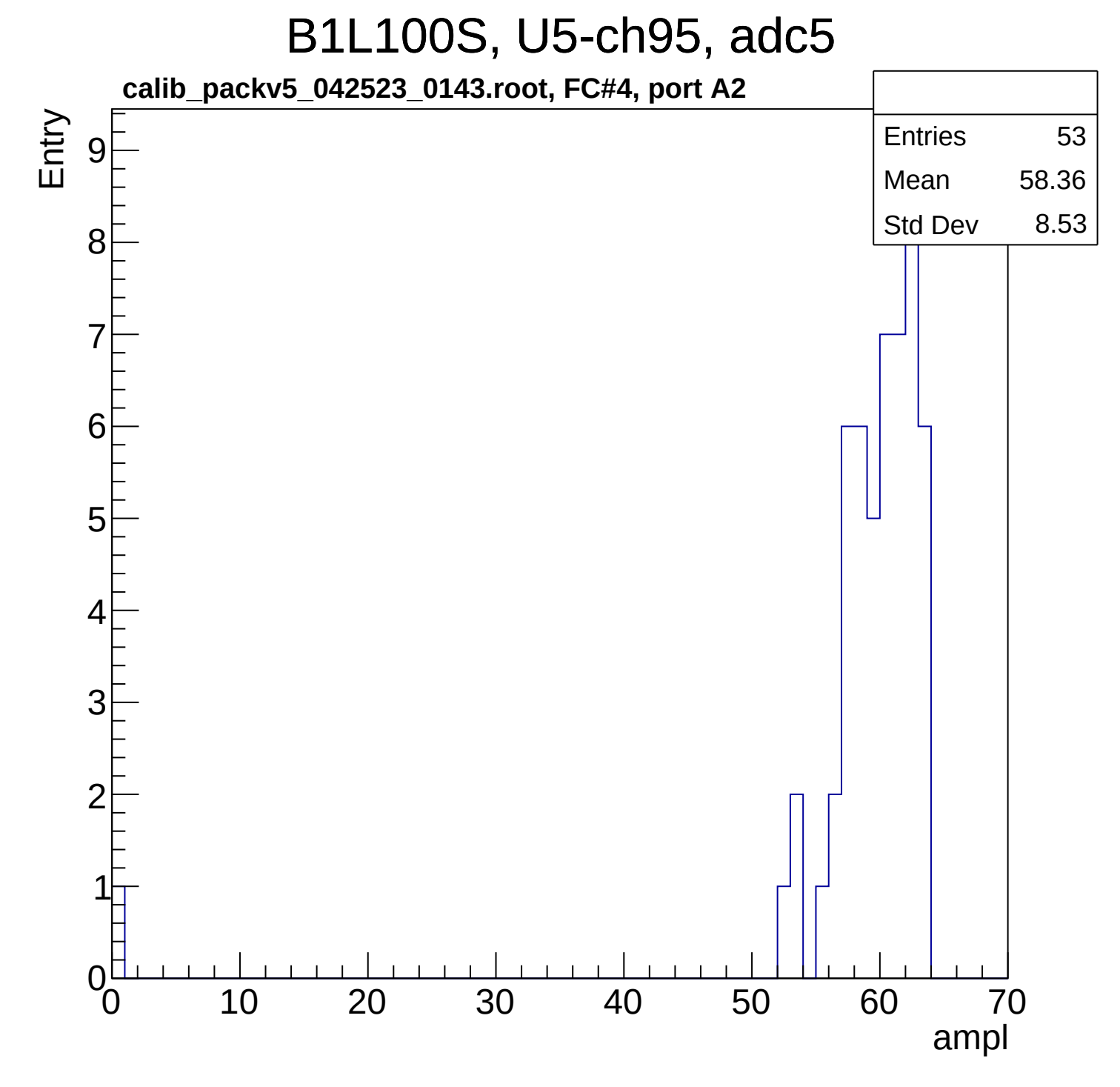
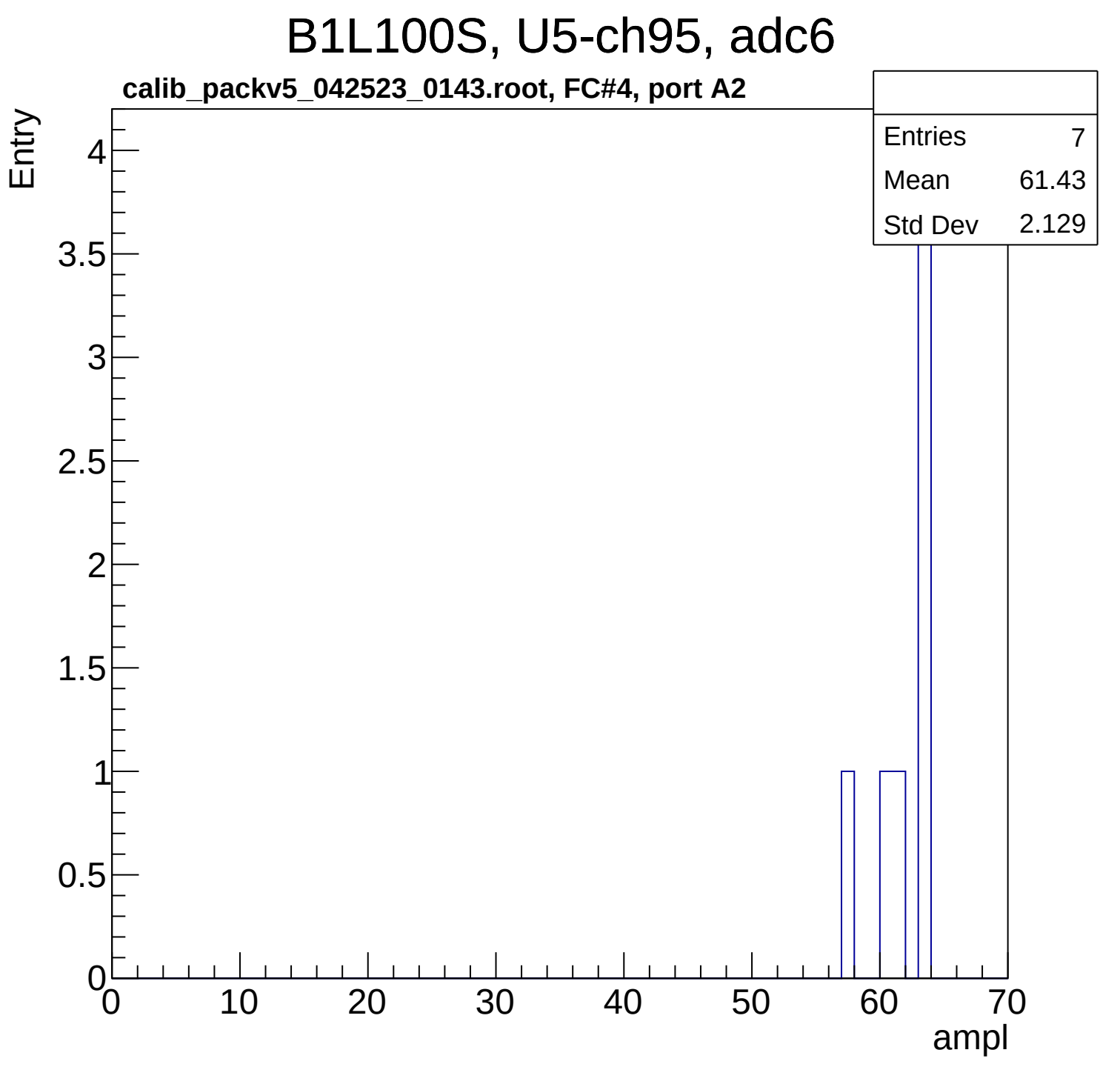
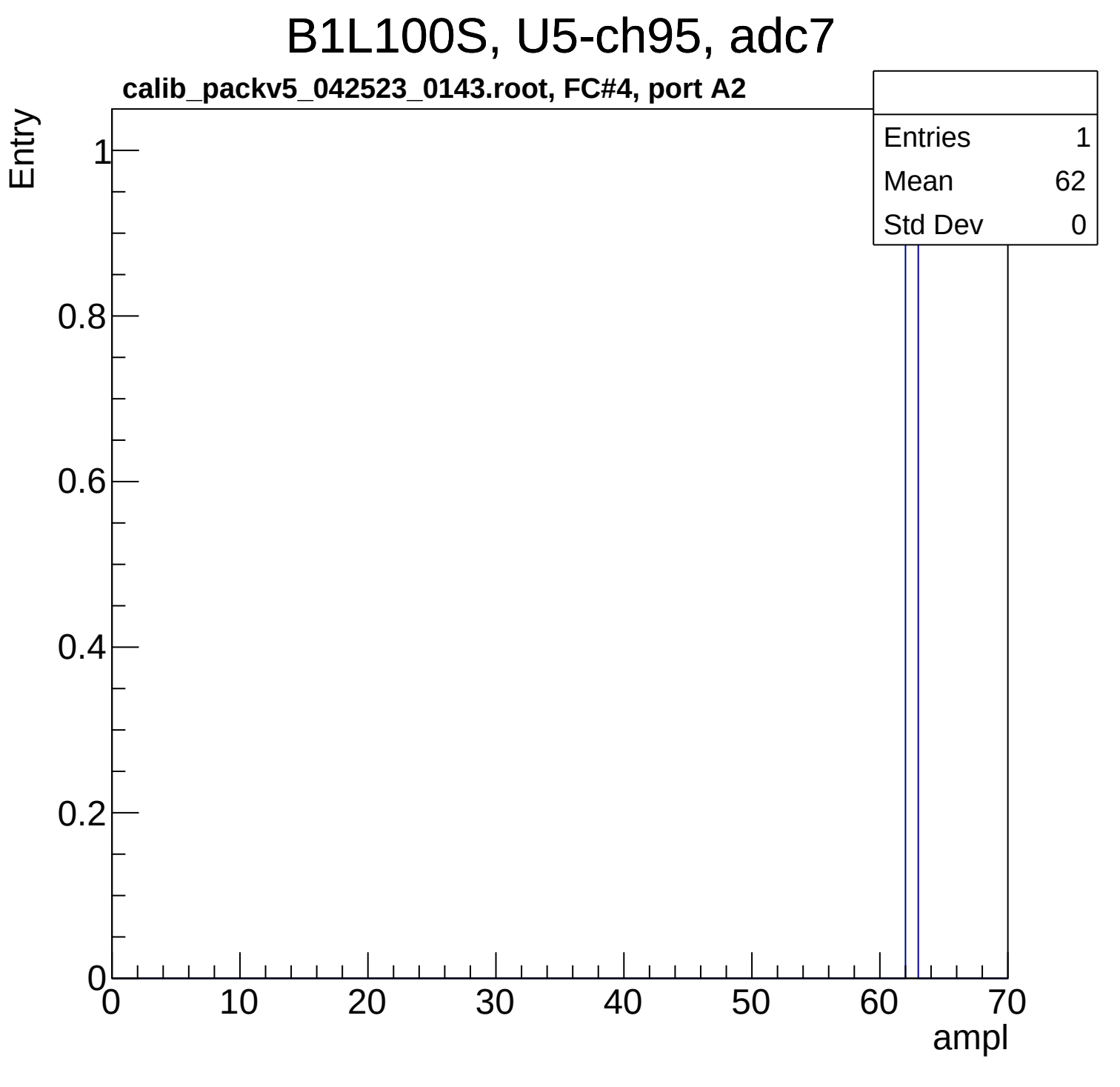

B1L100S, U5-ch95, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 58.36
Std Dev 8.53
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch95, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 7
Mean 61.43
Std Dev 2.129
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L100S, U5-ch95, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 62
Std Dev 0
Entry
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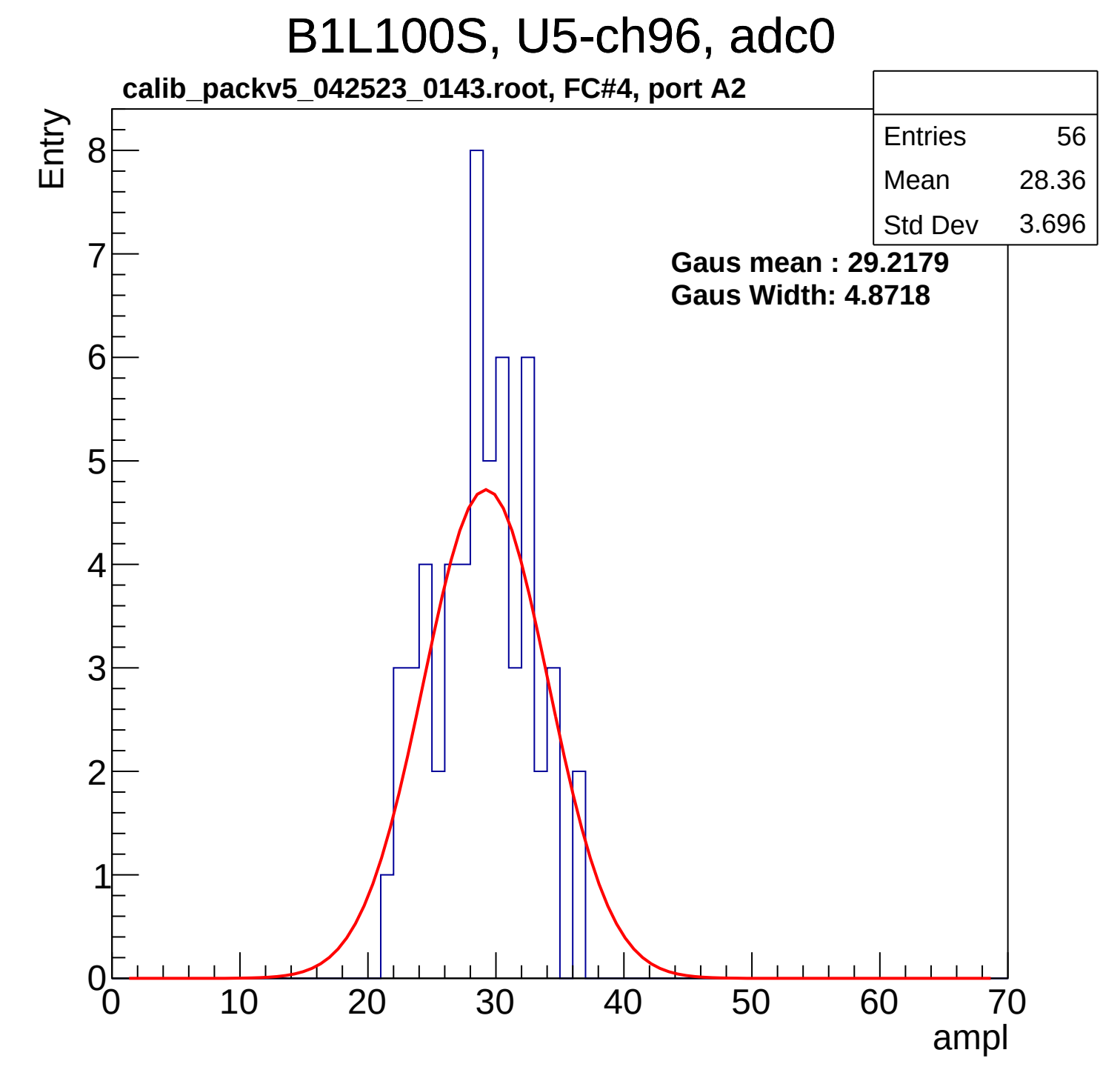
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch96, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 28.36
Std Dev 3.696
Gaus mean : 29.2179
Gaus Width: 4.8718
Entry
ampl
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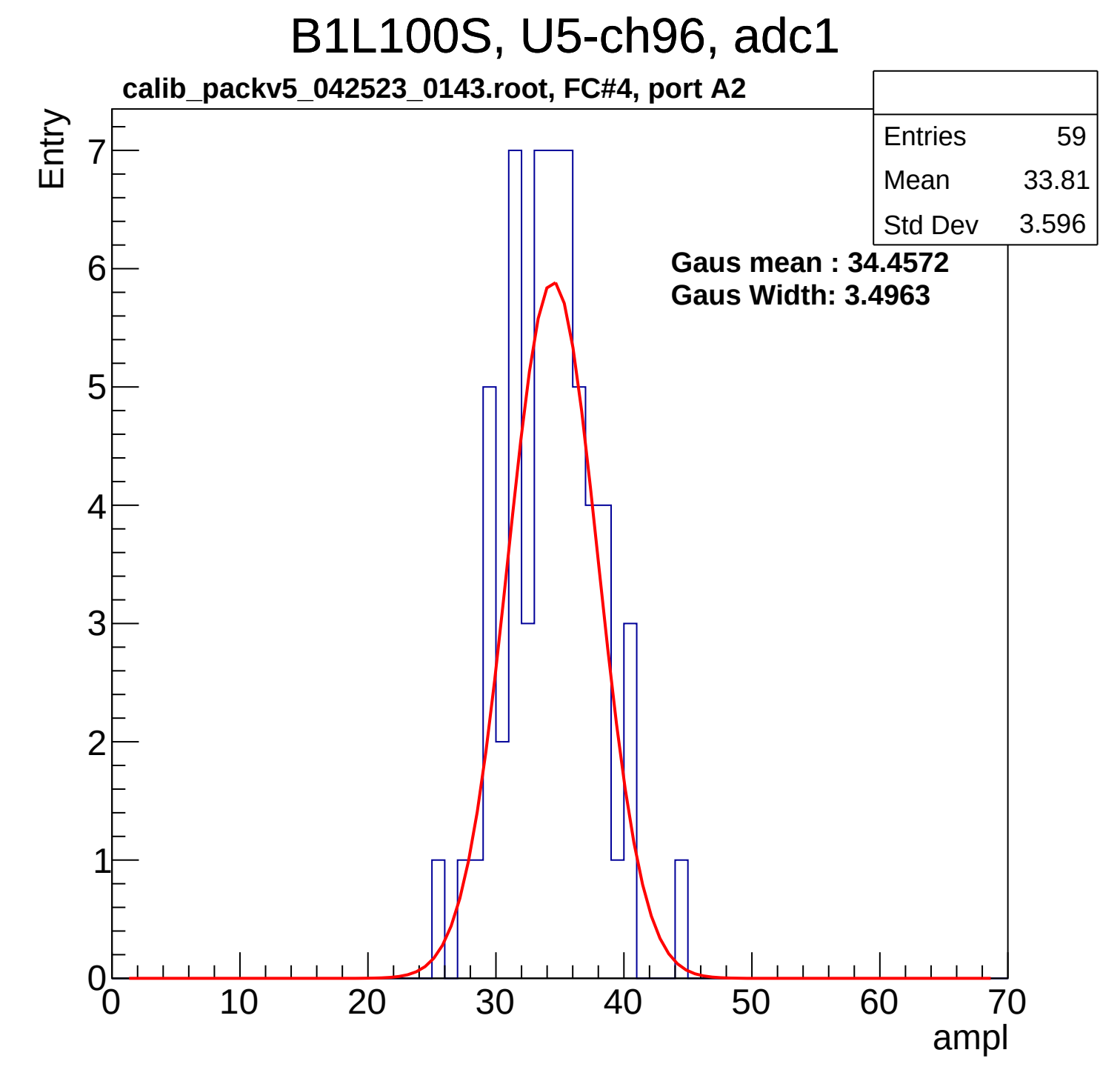
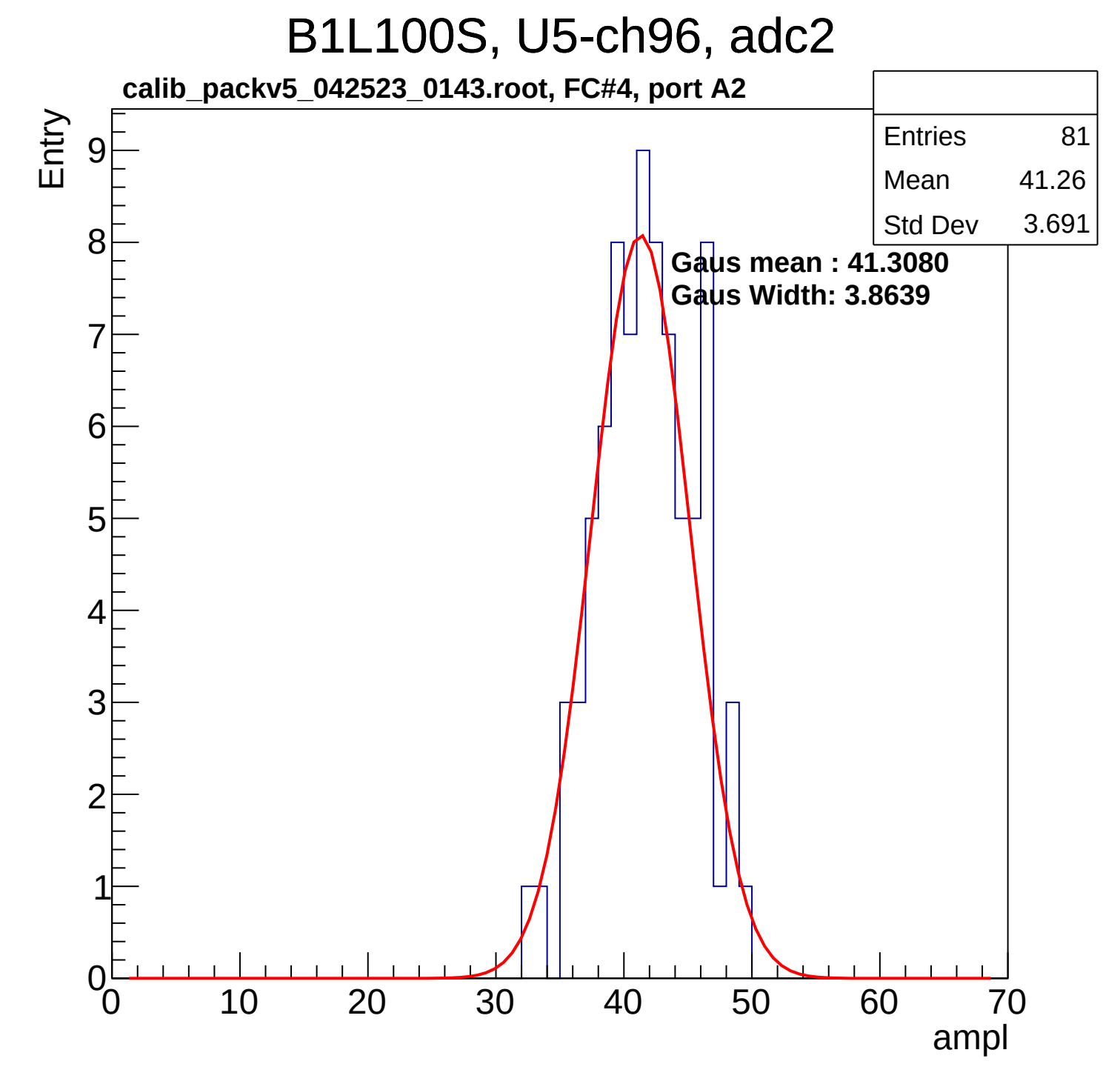
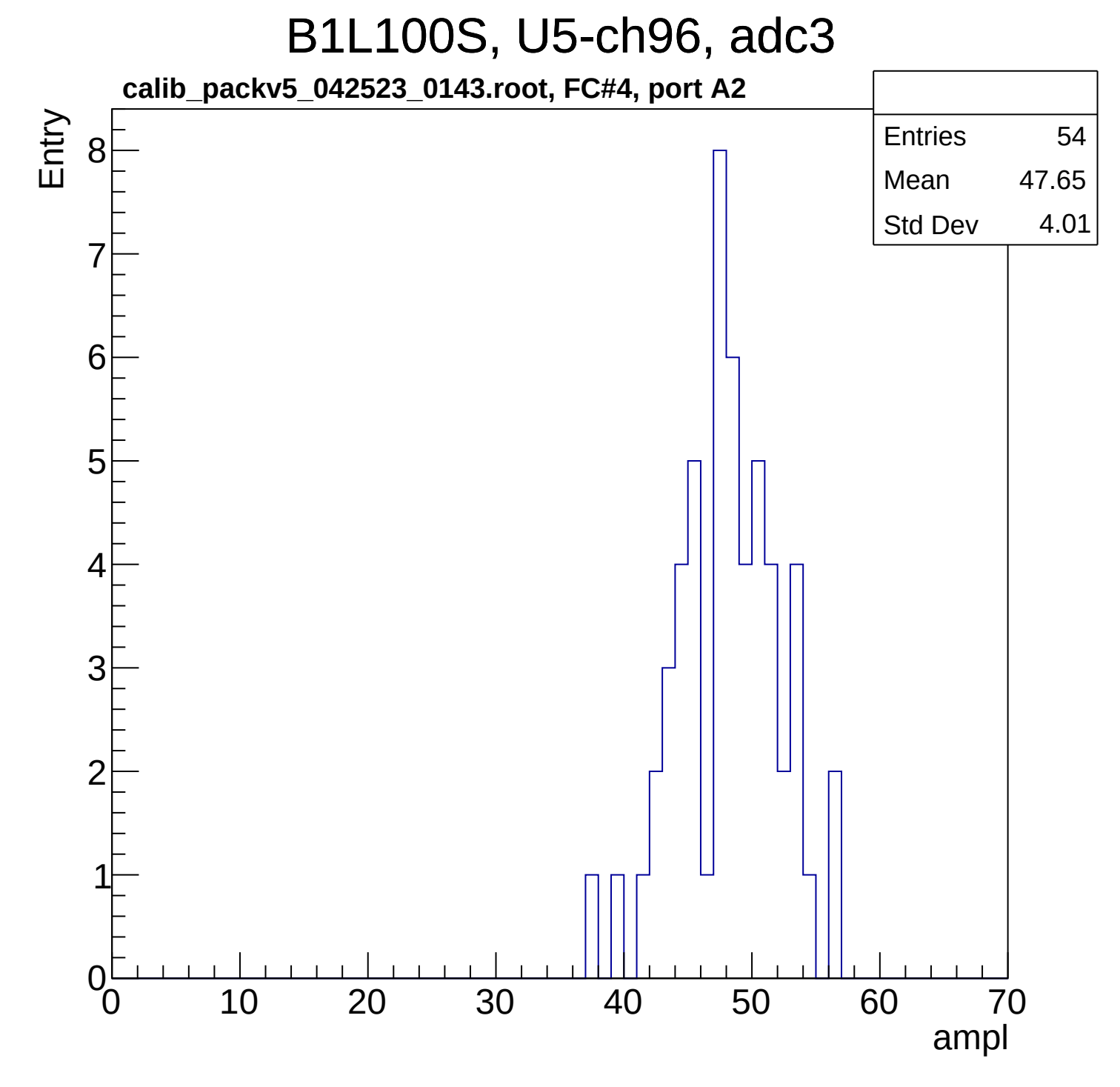
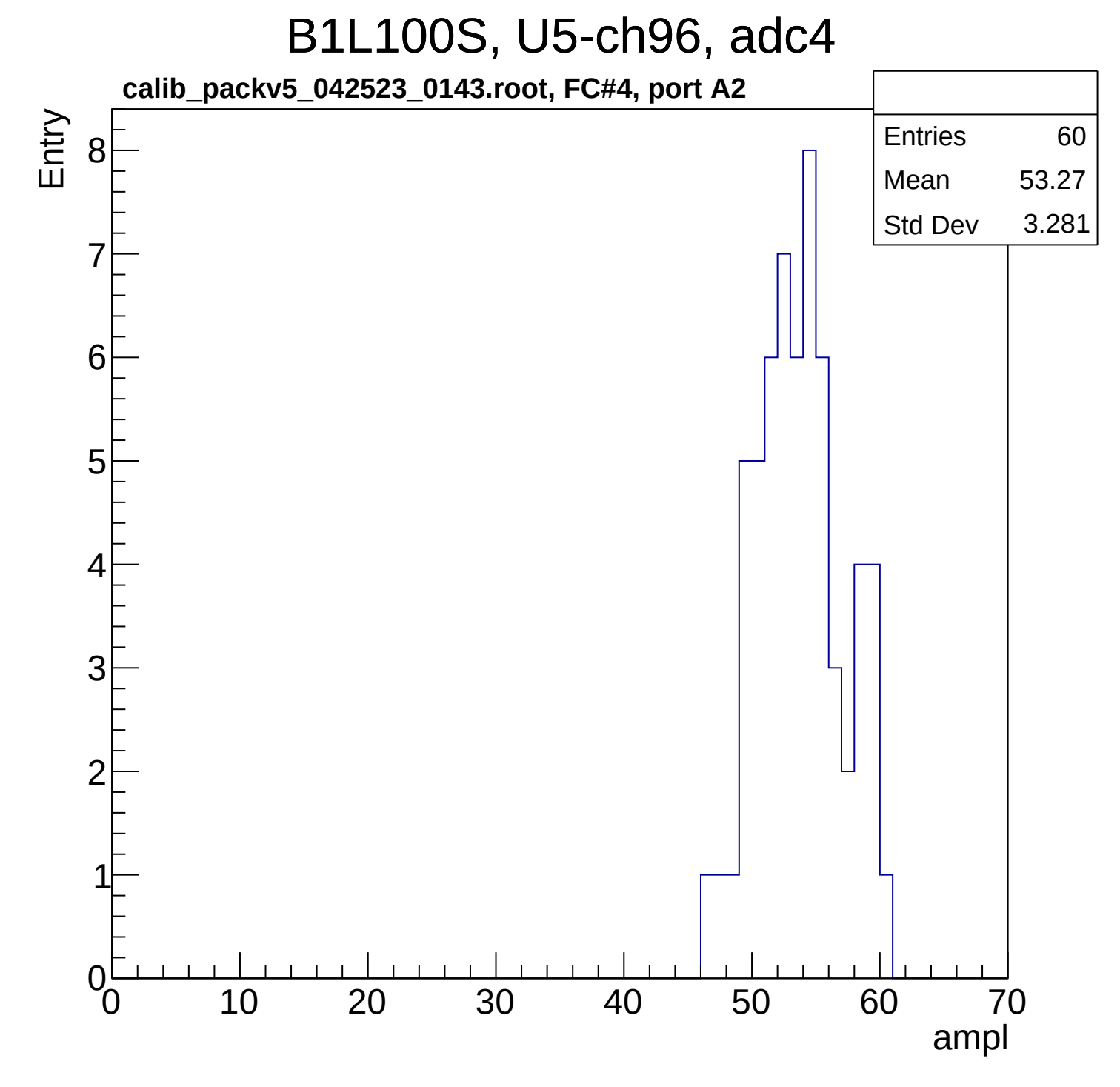
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch96, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 33.81
Std Dev 3.596
Gaus mean : 34.4572
Gaus Width: 3.4963
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U5-ch96, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 81
Mean 41.26
Std Dev 3.691
Gaus mean : 41.3080
Gaus Width: 3.8639
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch96, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 47.65
Std Dev 4.01
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch96, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 53.27
Std Dev 3.281
Entry
ampl
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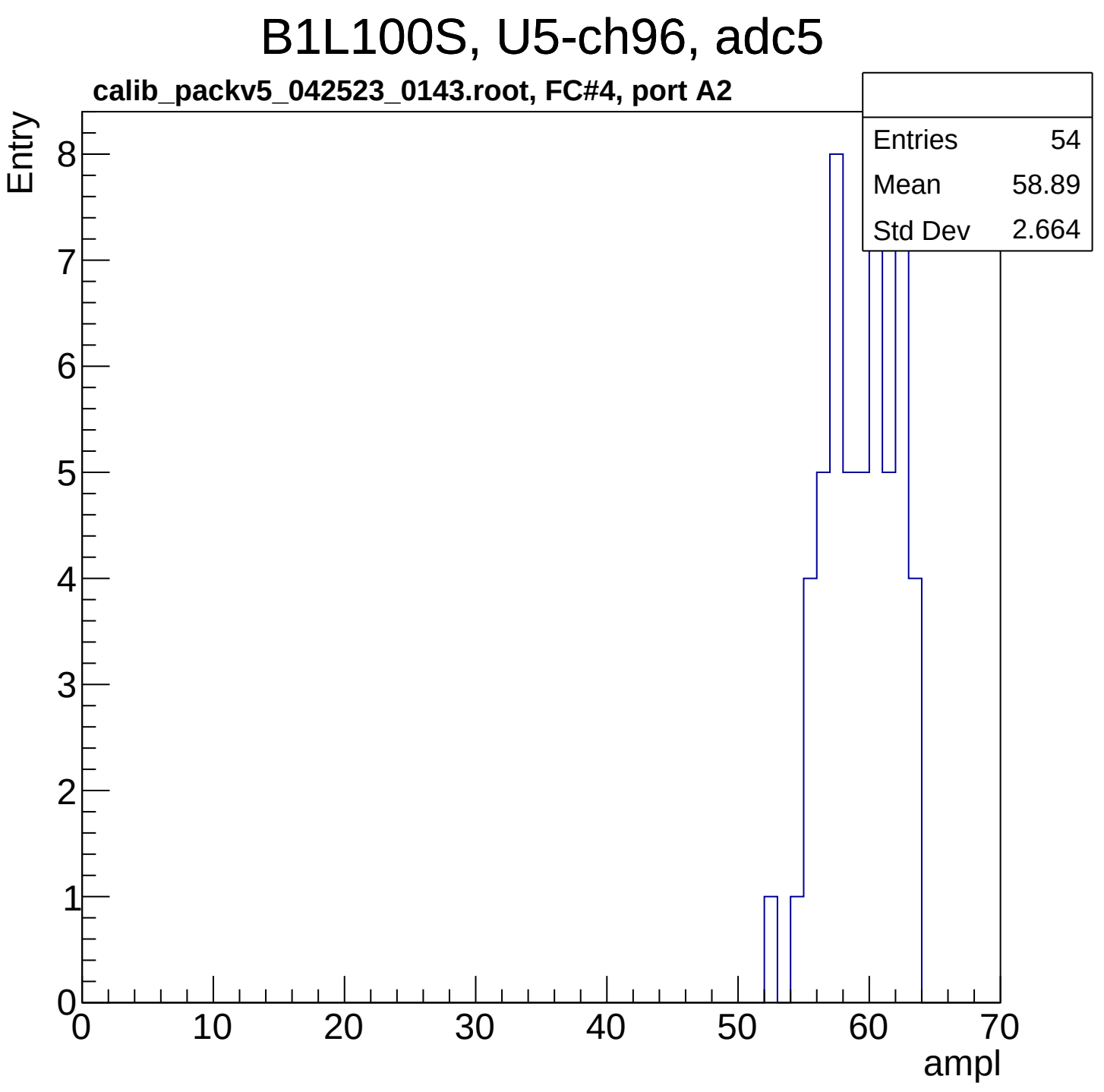
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch96, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 58.89
Std Dev 2.664
Entry
ampl
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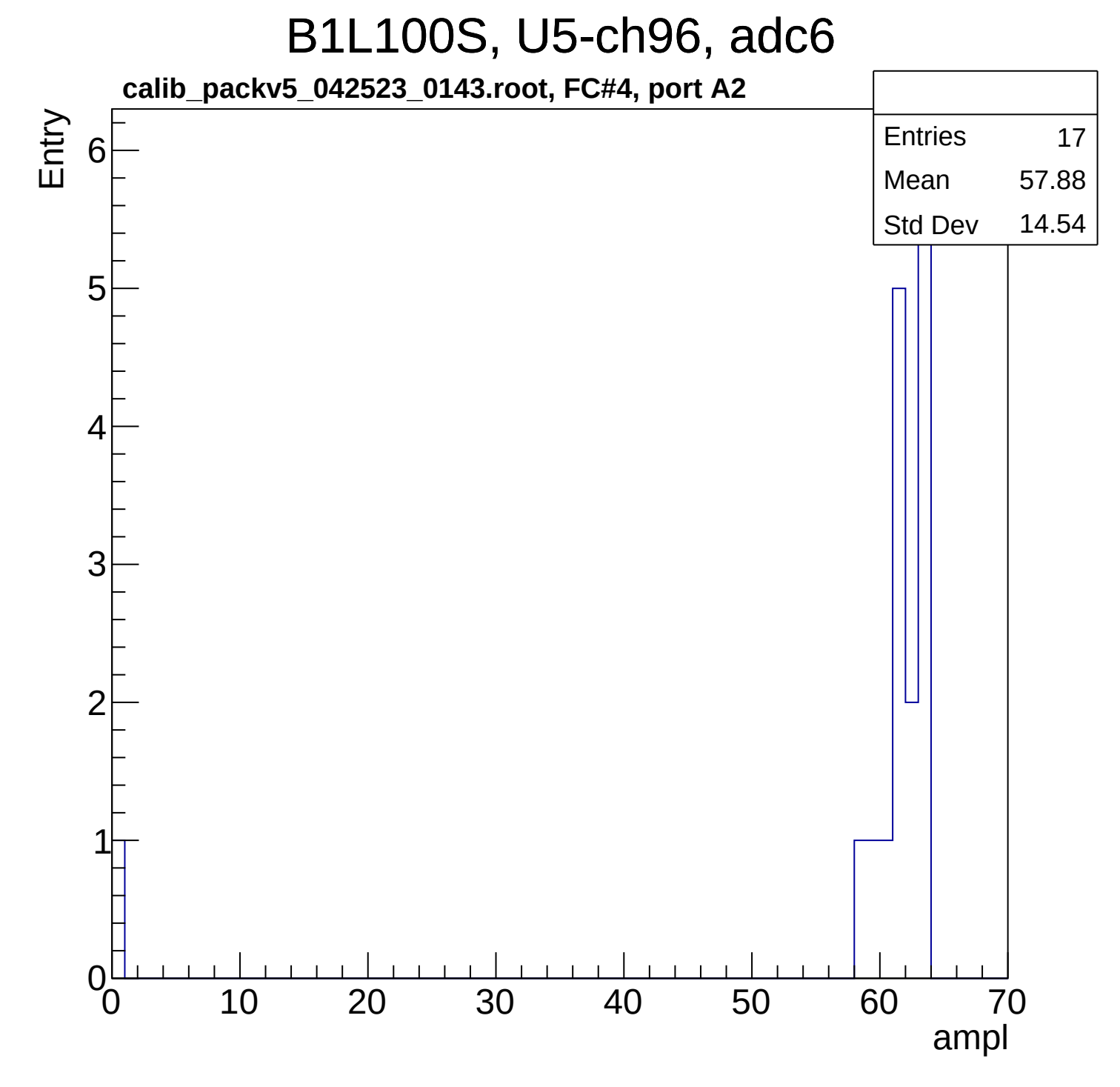
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch96, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 17
Mean 57.88
Std Dev 14.54
Entry
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2
3
4
5
6
0
10
20
30
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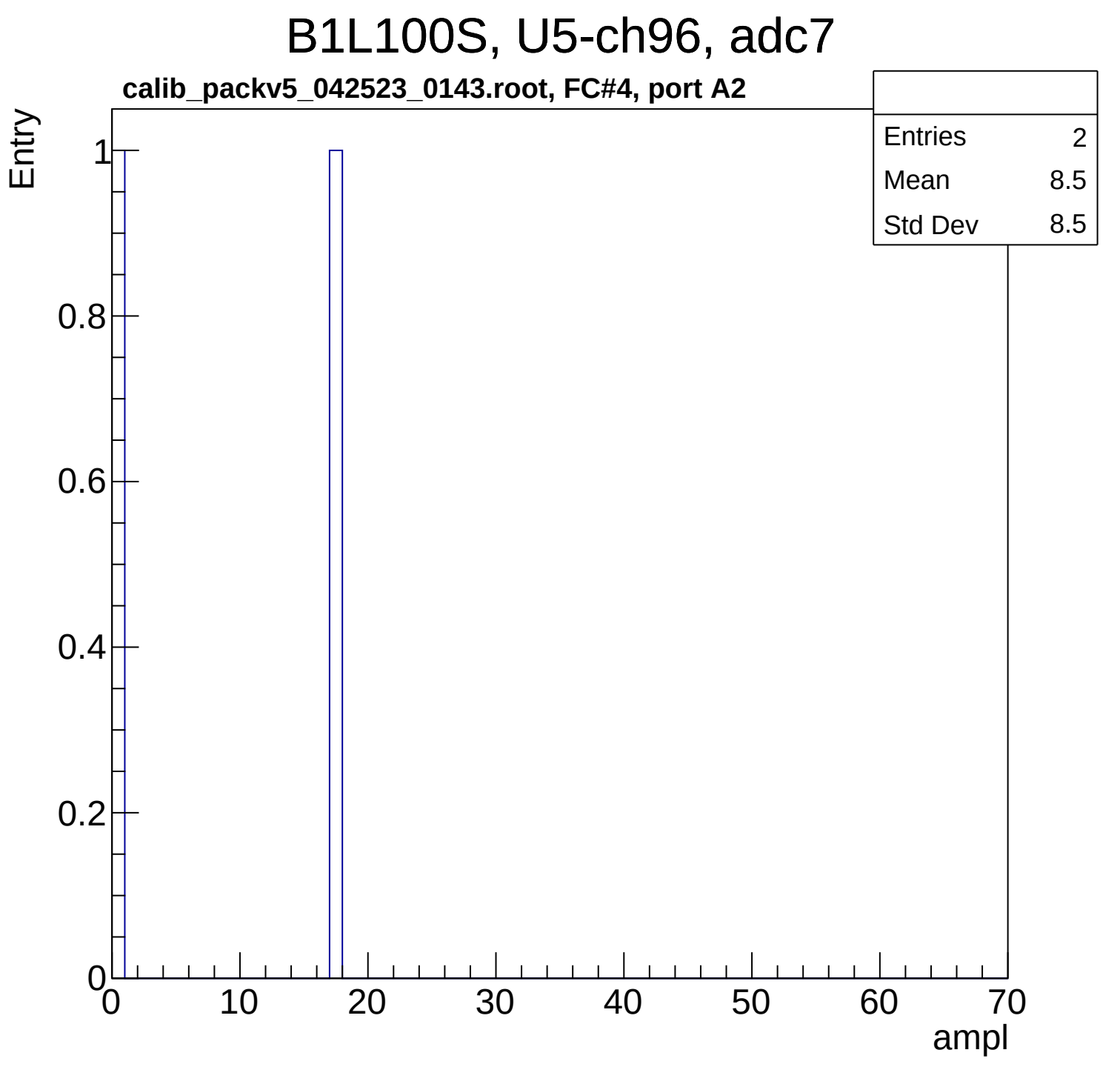
50
60
70
ampl


B1L100S, U5-ch96, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 8.5
Std Dev 8.5
Entry
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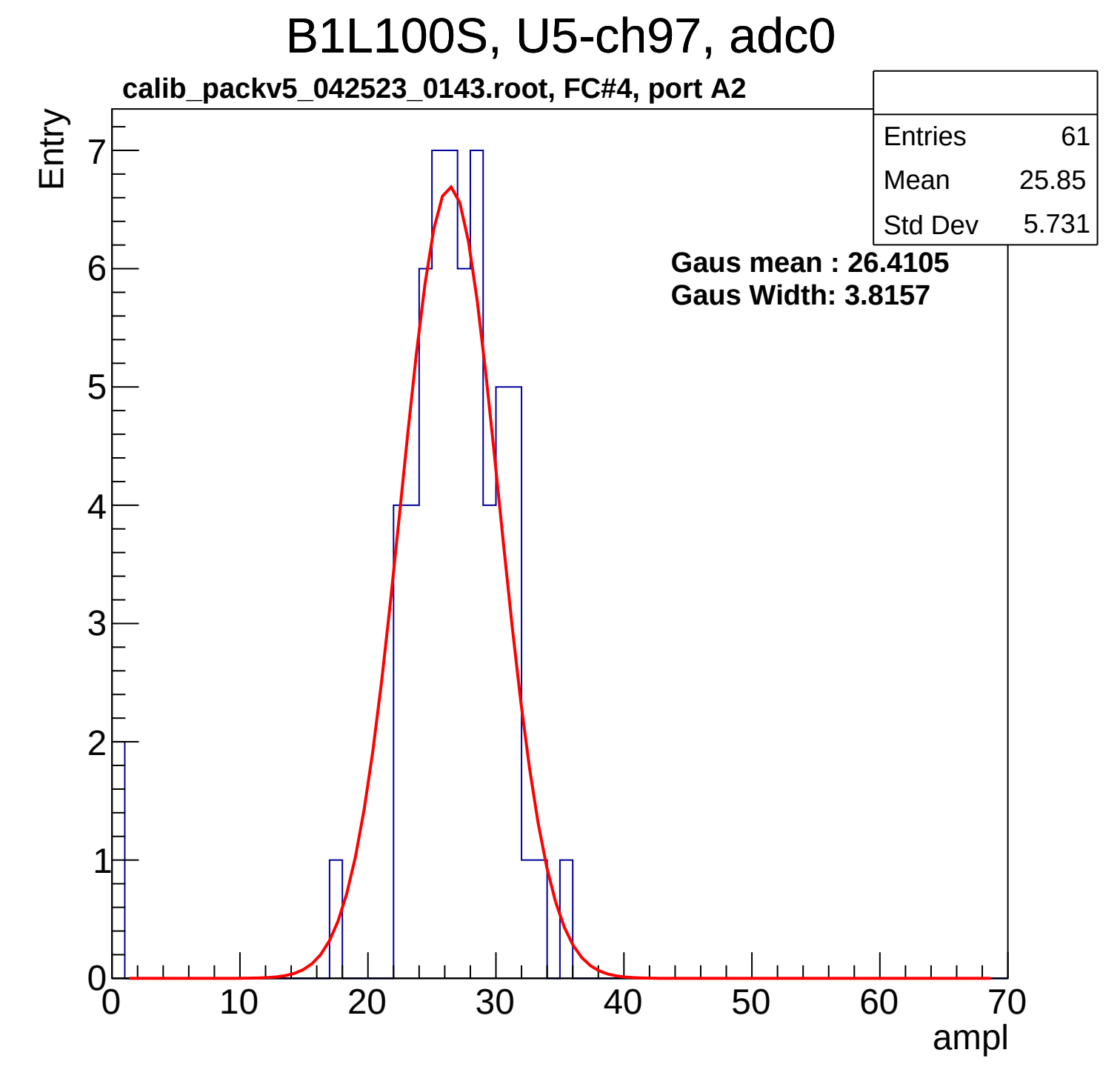
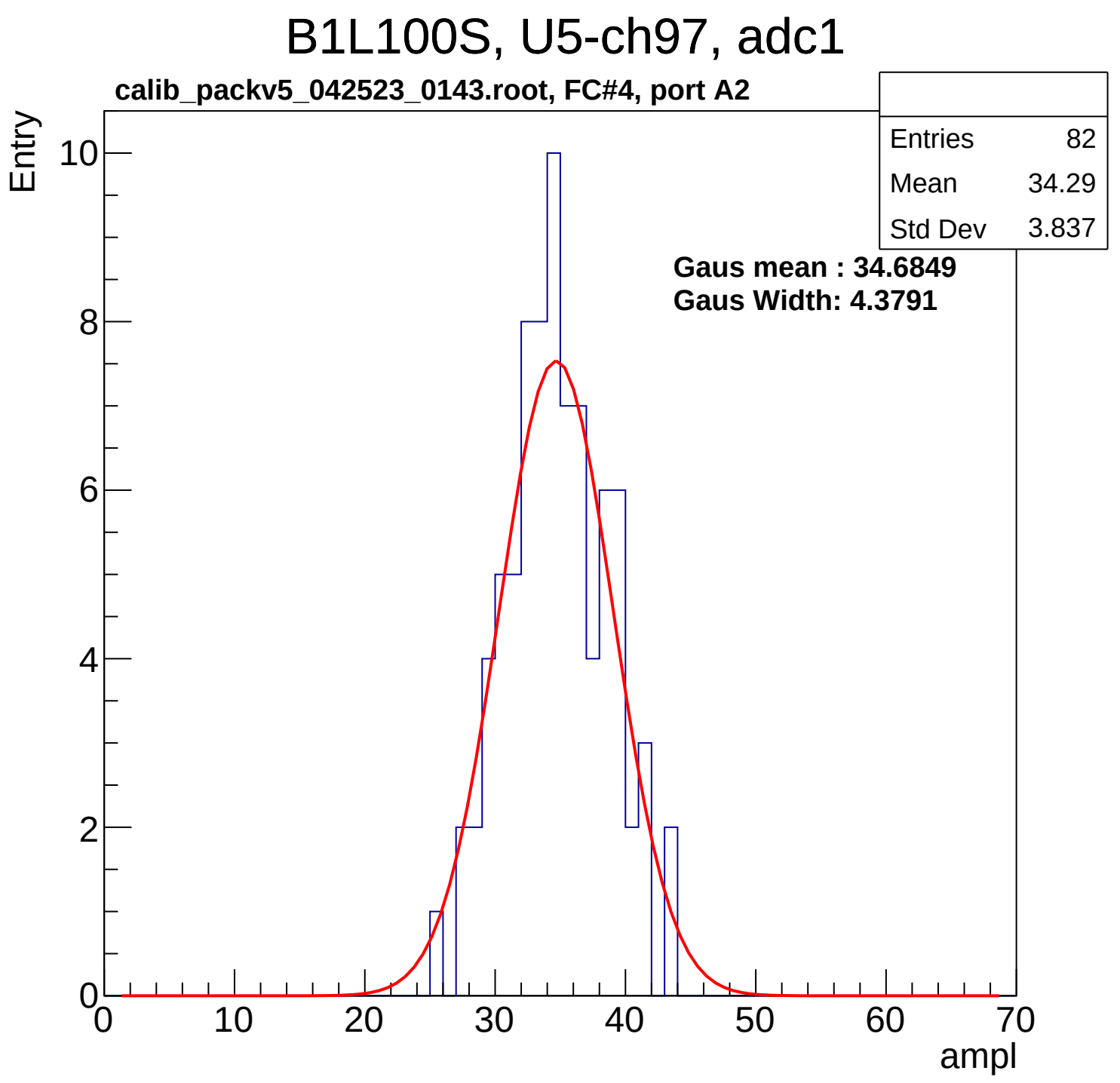
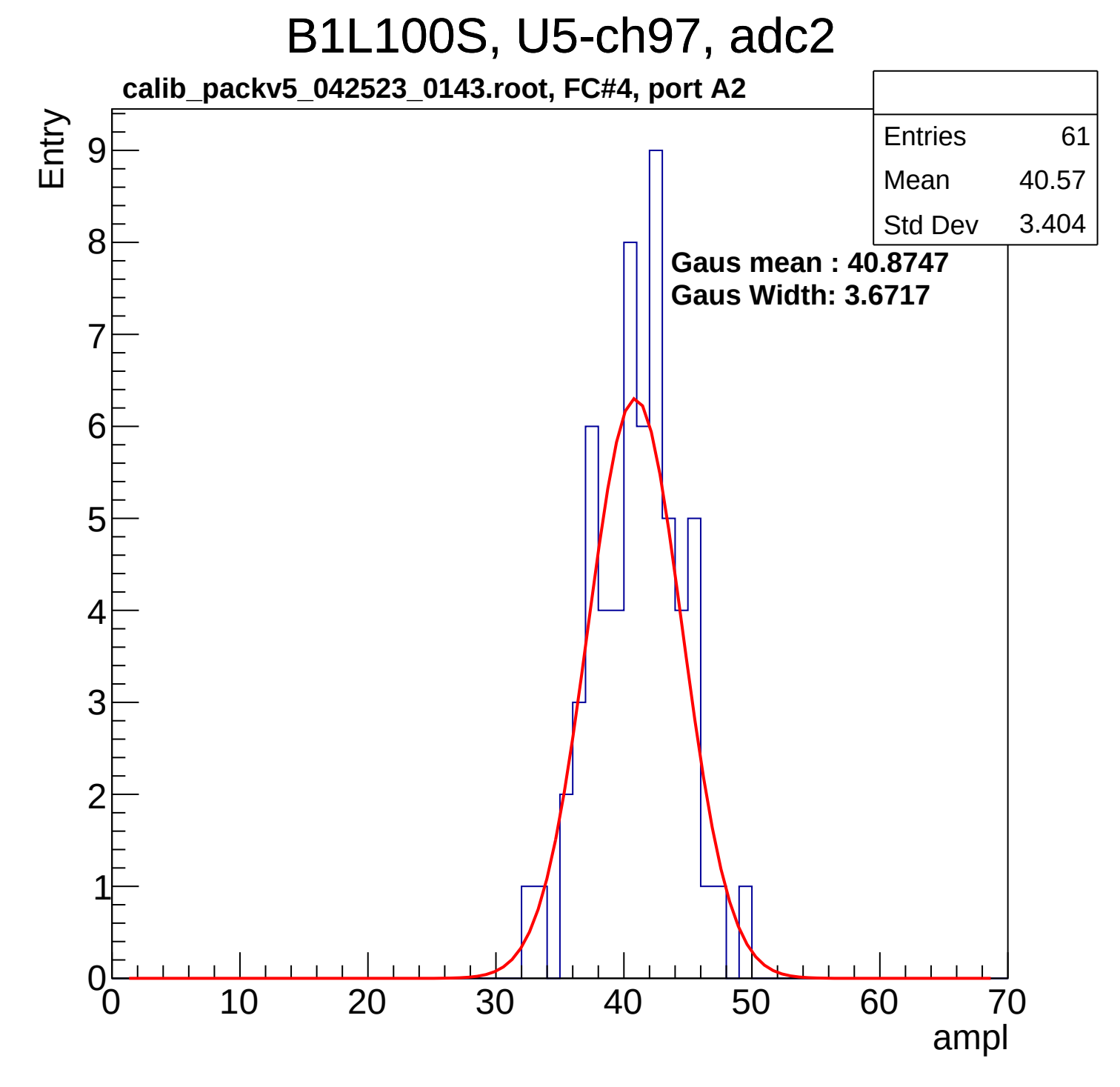
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch97, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 25.85
Std Dev 5.731
Gaus mean : 26.4105
Gaus Width: 3.8157
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U5-ch97, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 82
Mean 34.29
Std Dev 3.837
Gaus mean : 34.6849
Gaus Width: 4.3791
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch97, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 40.57
Std Dev 3.404
Gaus mean : 40.8747
Gaus Width: 3.6717
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
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60
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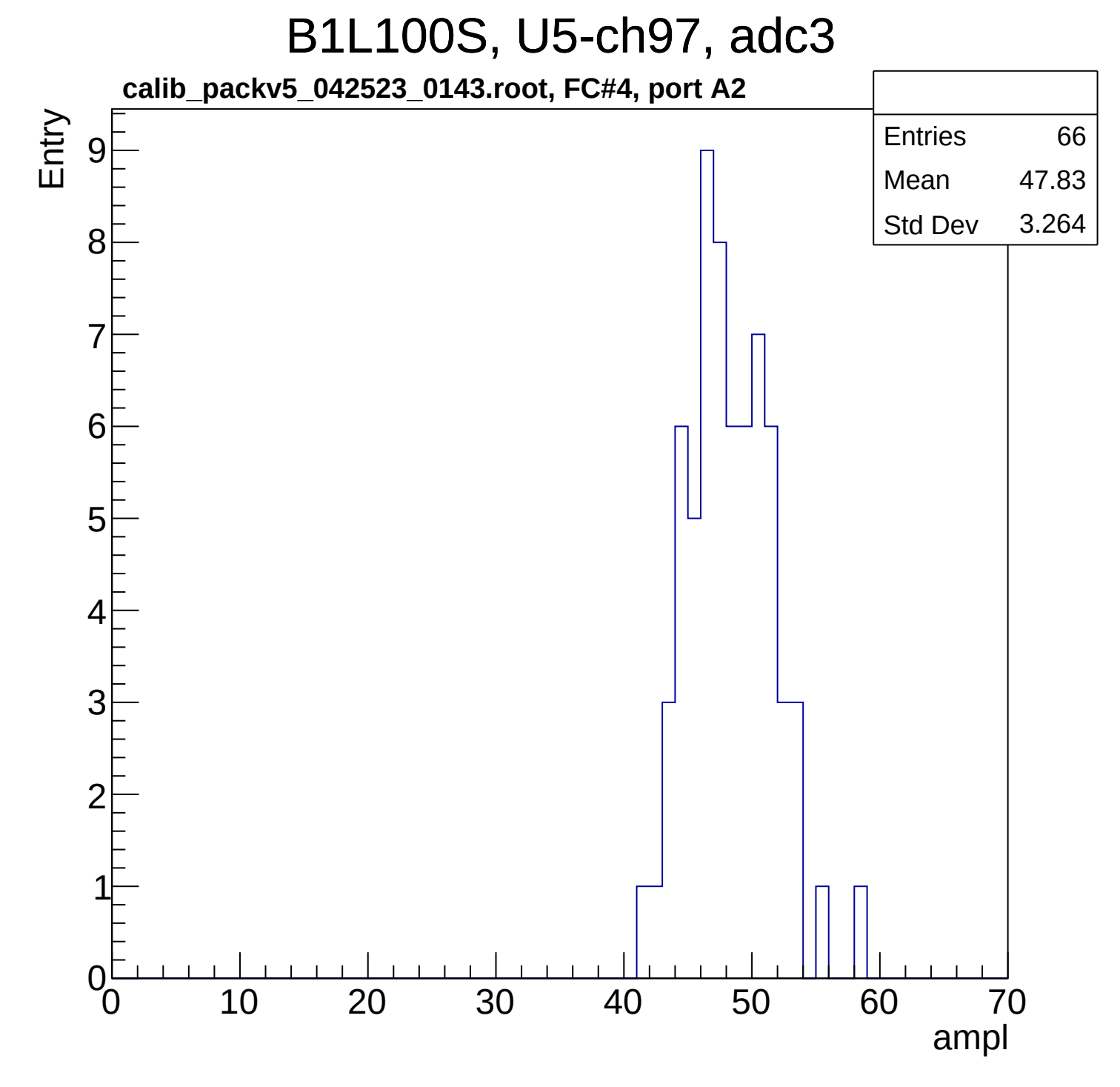
B1L100S, U5-ch97, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 47.83
Std Dev 3.264
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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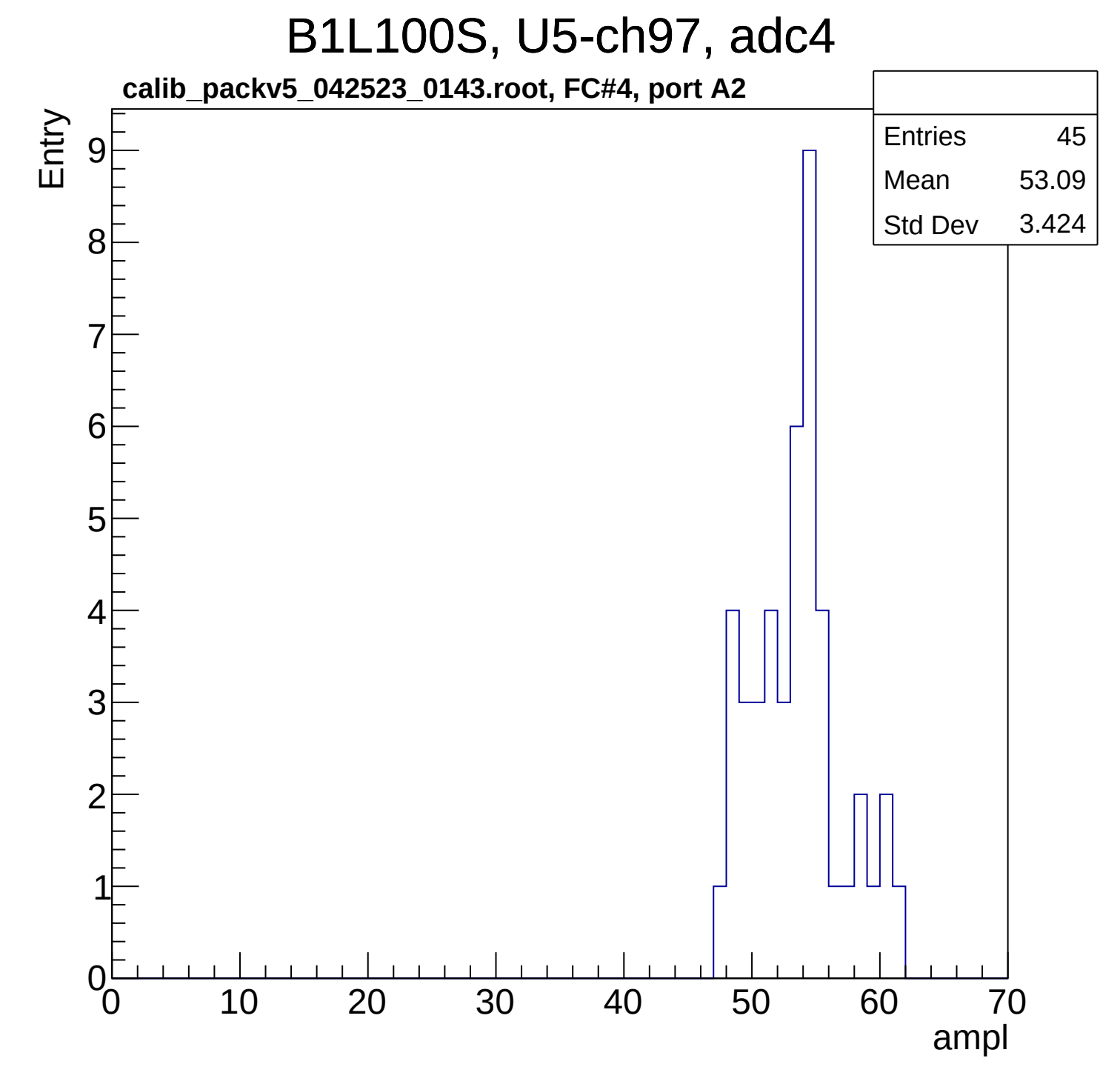
B1L100S, U5-ch97, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 45
Mean 53.09
Std Dev 3.424
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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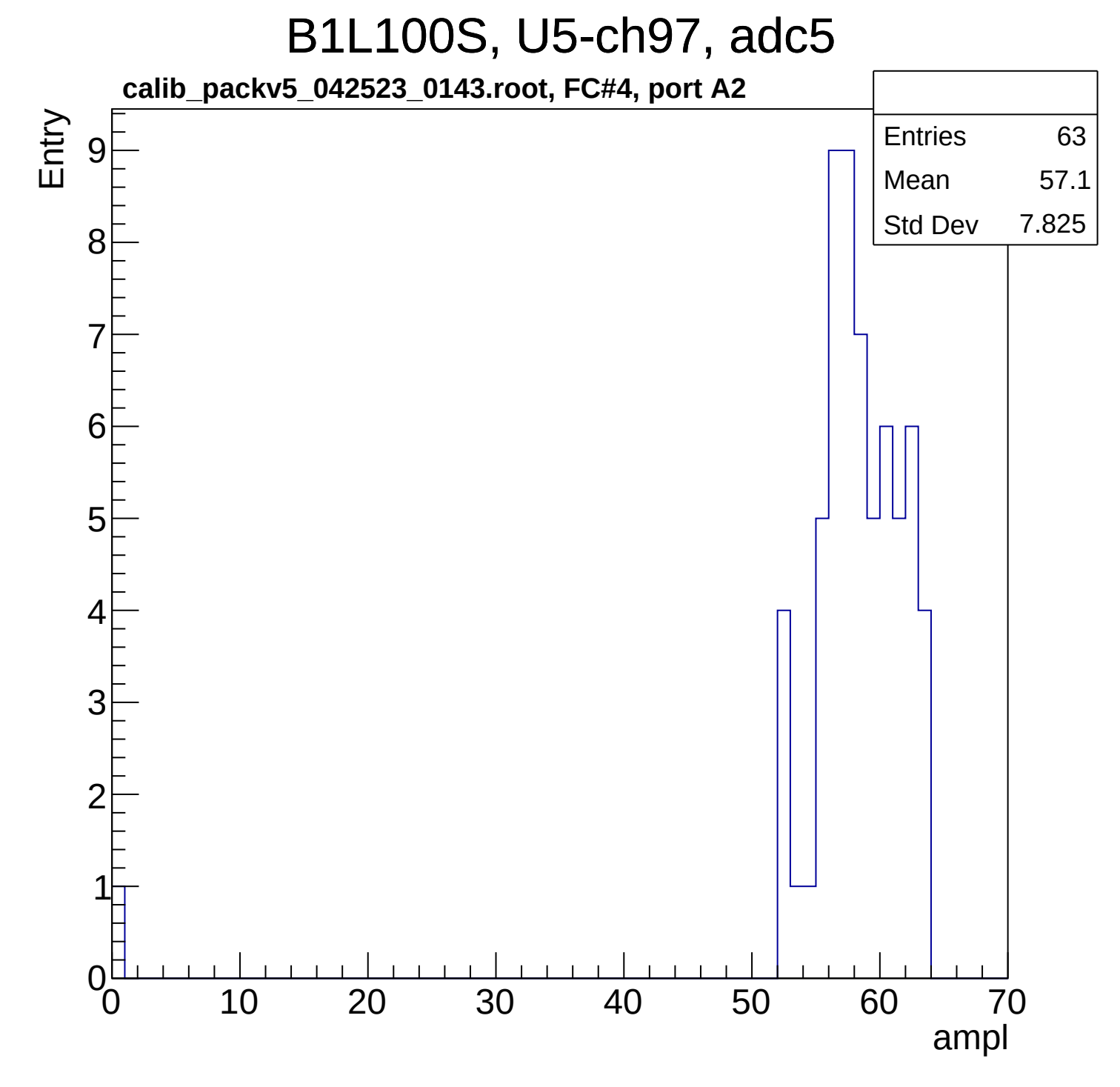
B1L100S, U5-ch97, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 57.1
Std Dev 7.825
Entry
ampl
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3
4
5
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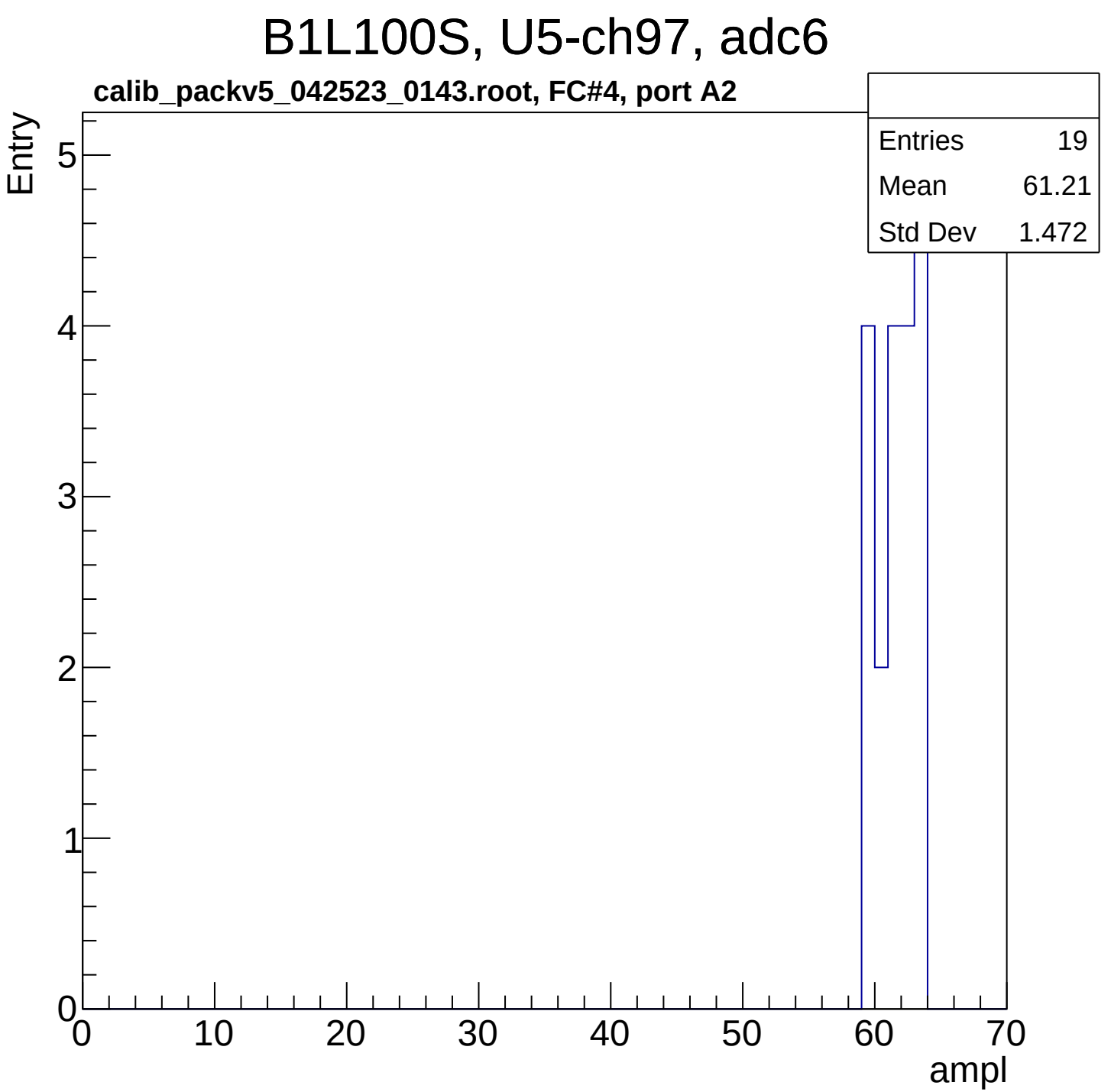
B1L100S, U5-ch97, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 19
Mean 61.21
Std Dev 1.472
Entry
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1
2
3
4
5
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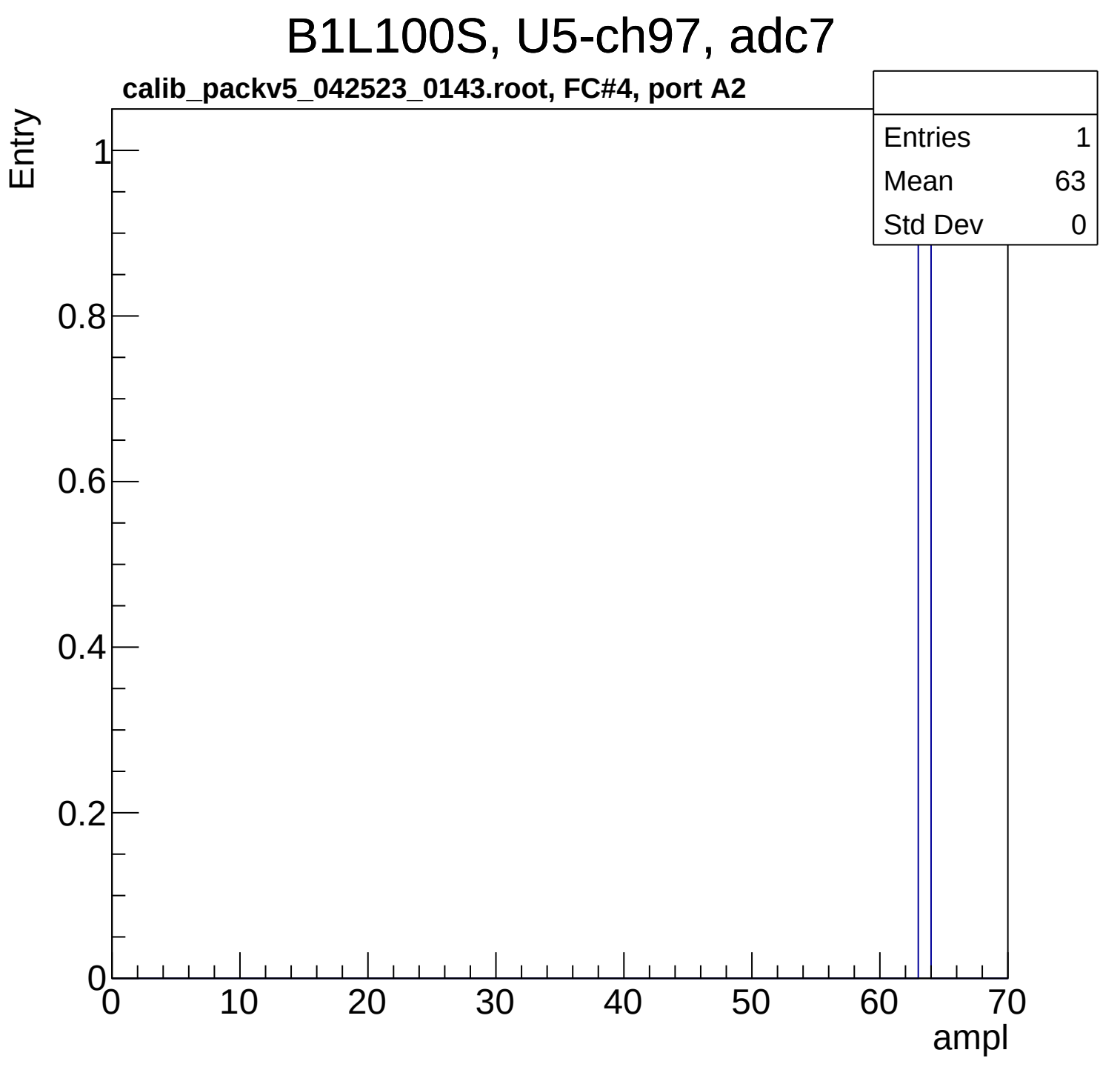
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch97, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
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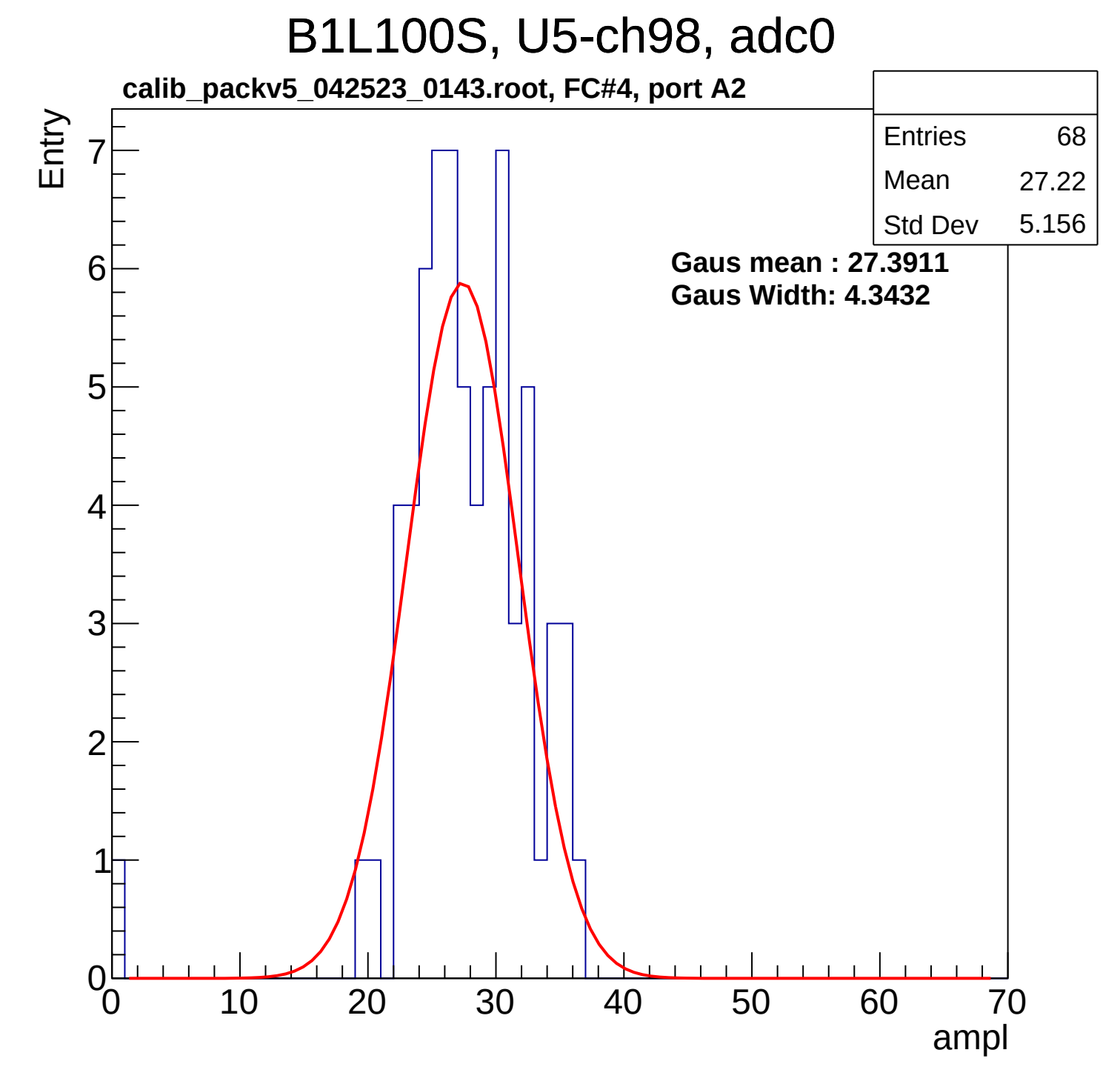
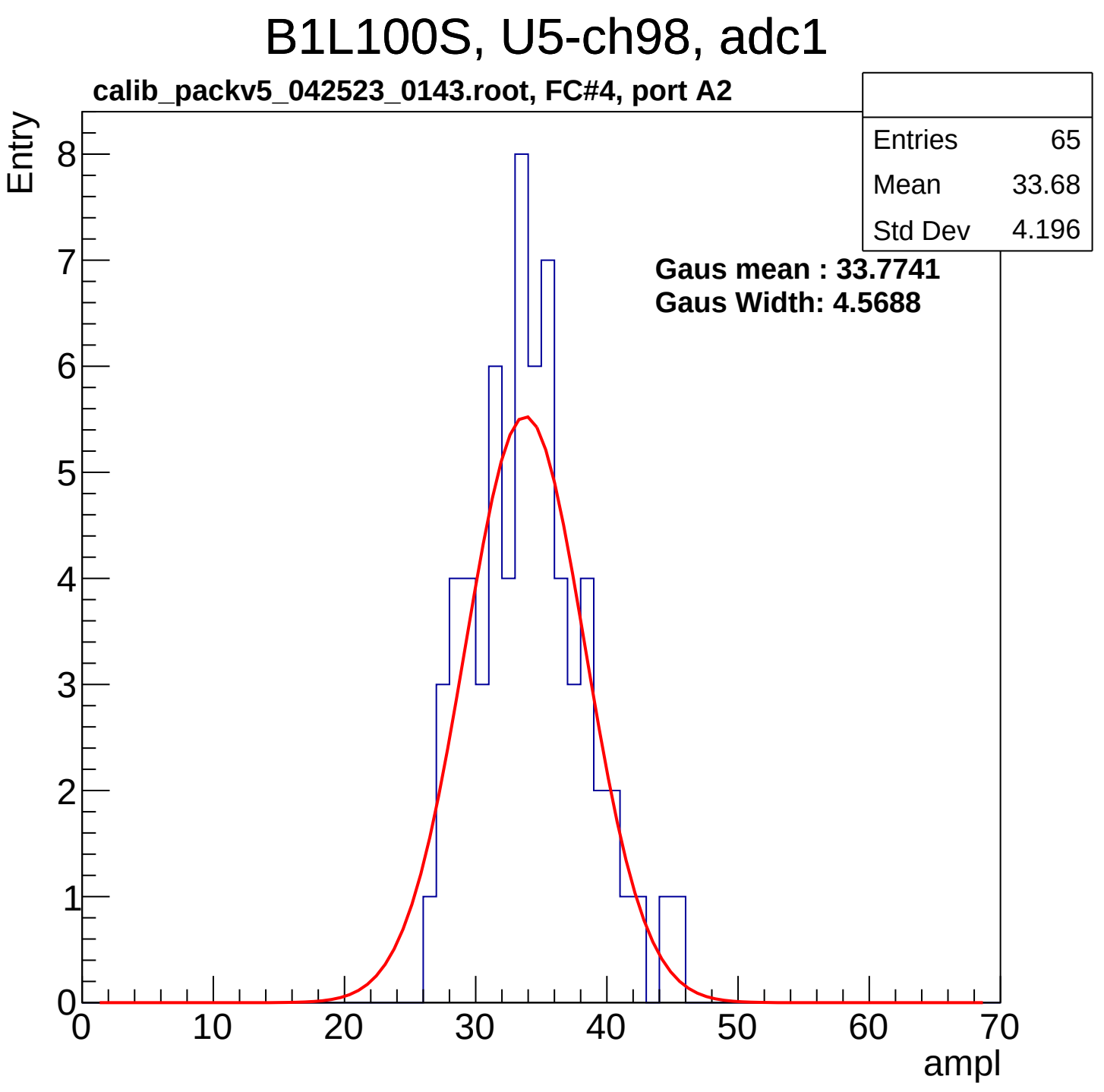
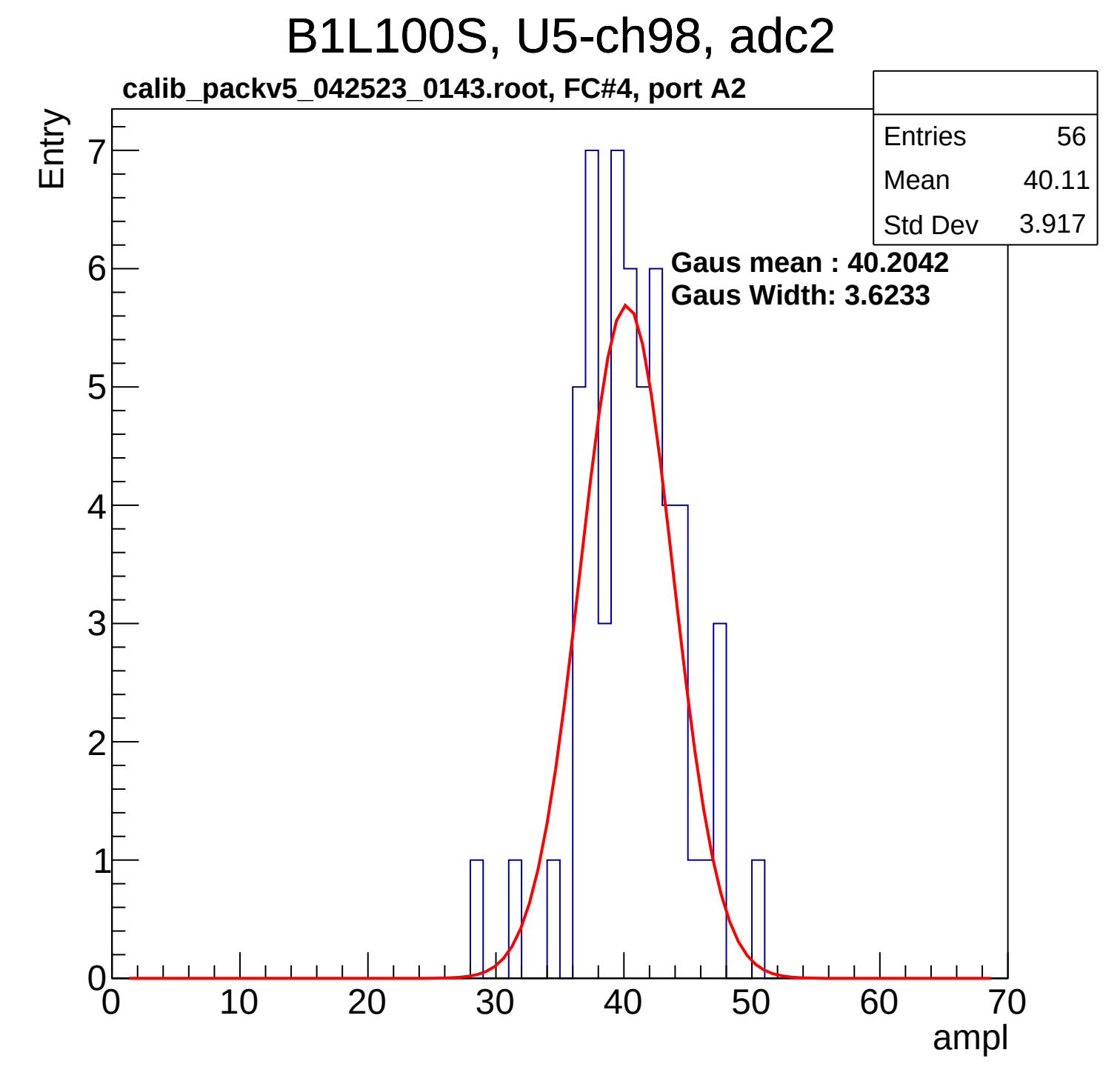
50
60
70
ampl


B1L100S, U5-ch98, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 27.22
Std Dev 5.156
Gaus mean : 27.3911
Gaus Width: 4.3432
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U5-ch98, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 33.68
Std Dev 4.196
Gaus mean : 33.7741
Gaus Width: 4.5688
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch98, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 40.11
Std Dev 3.917
Gaus mean : 40.2042
Gaus Width: 3.6233
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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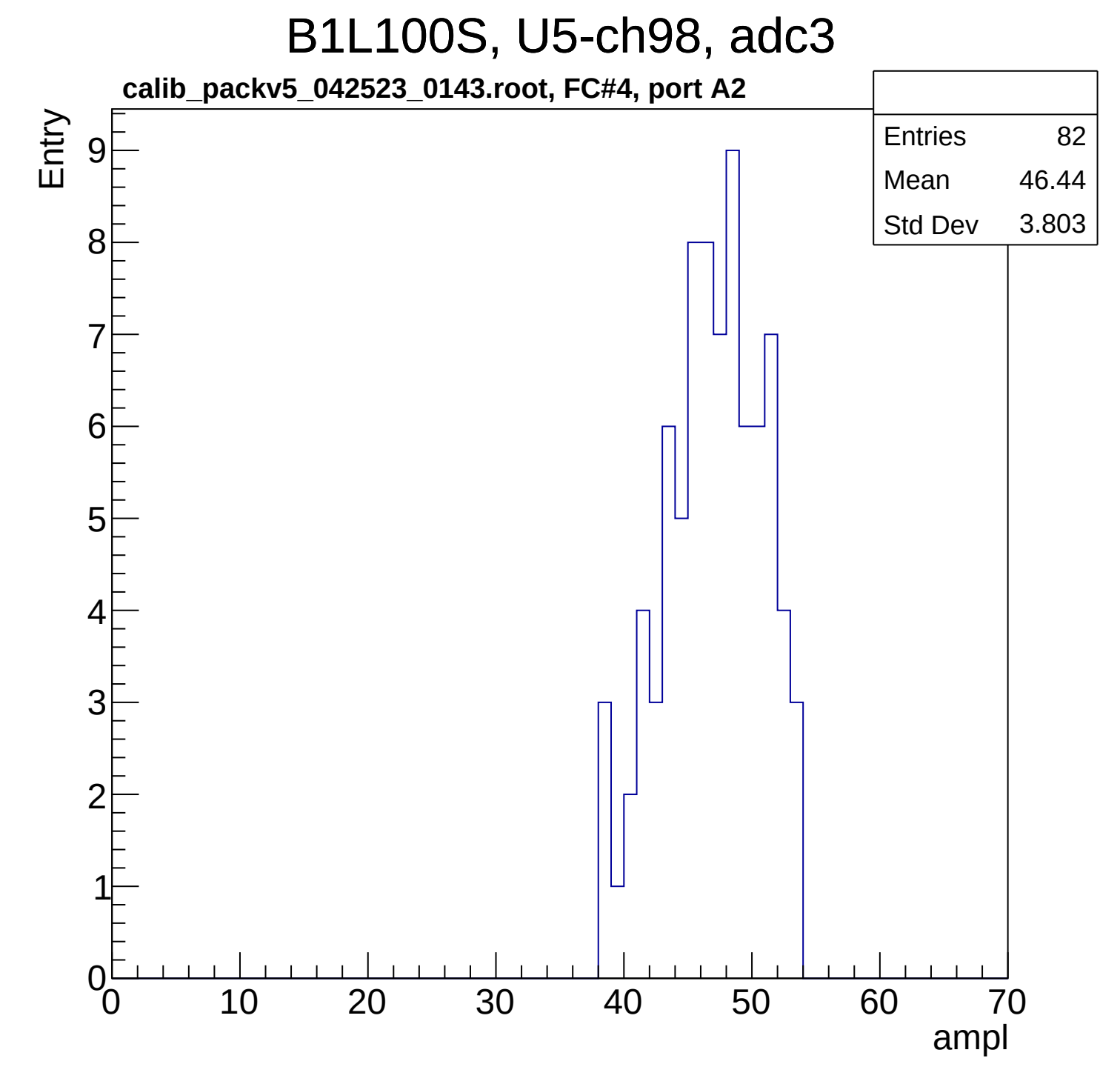
B1L100S, U5-ch98, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 82
Mean 46.44
Std Dev 3.803
Entry
ampl
0
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2
3
4
5
6
7
8
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0
10
20
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60
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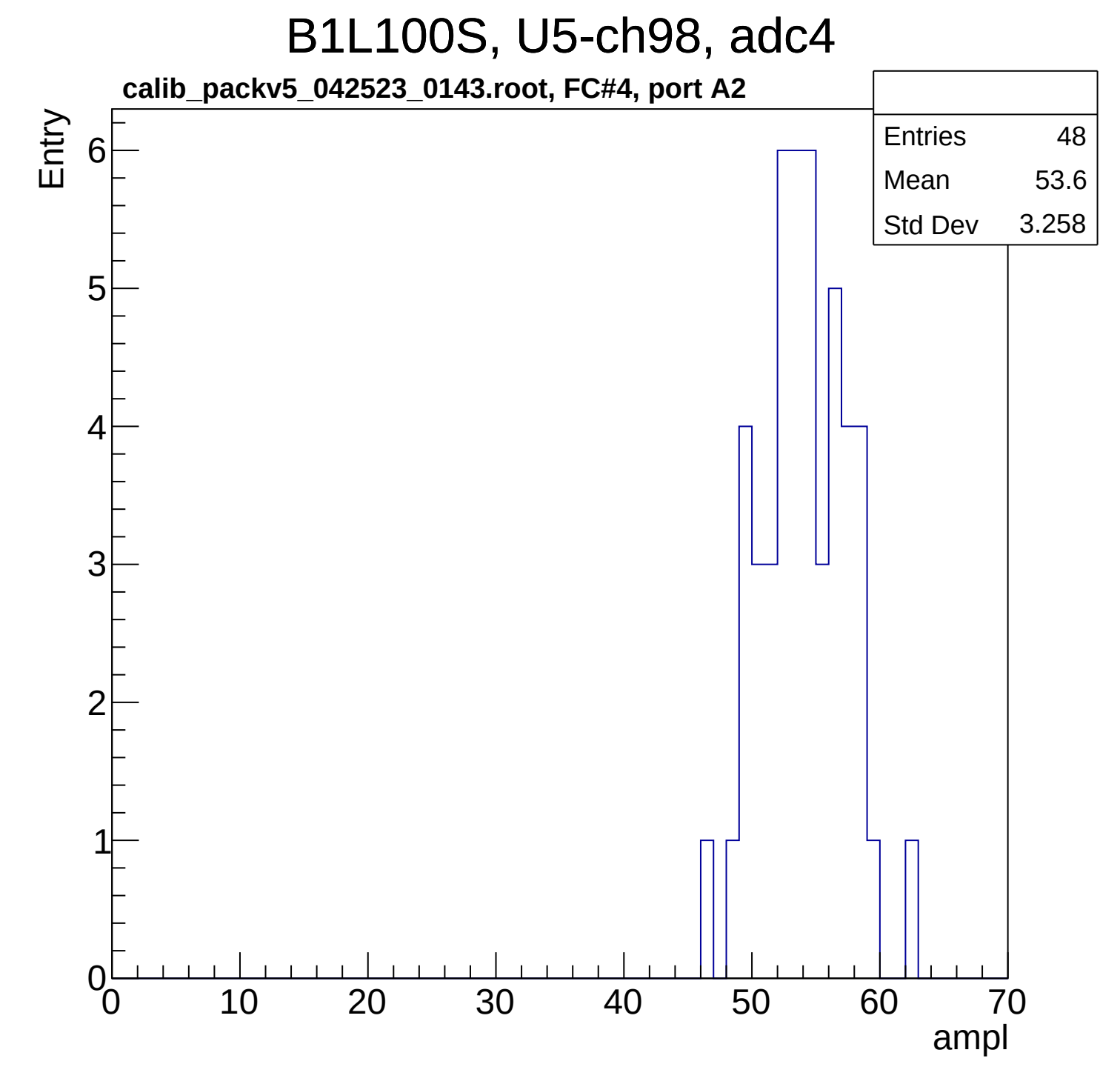
B1L100S, U5-ch98, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 48
Mean 53.6
Std Dev 3.258
Entry
ampl
0
1
2
3
4
5
6
0
10
20
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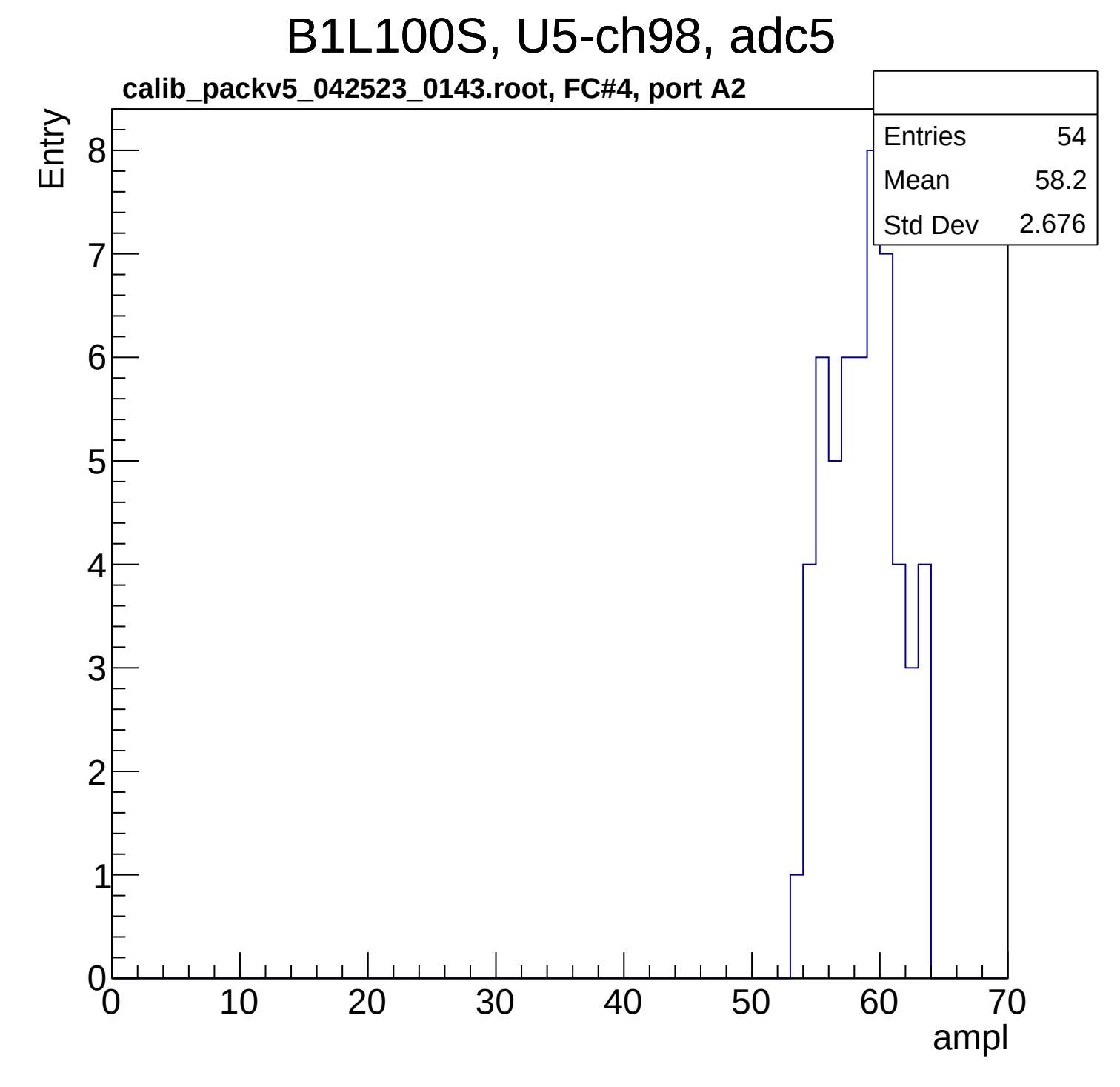
40
50
60
70


B1L100S, U5-ch98, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 58.2
Std Dev 2.676
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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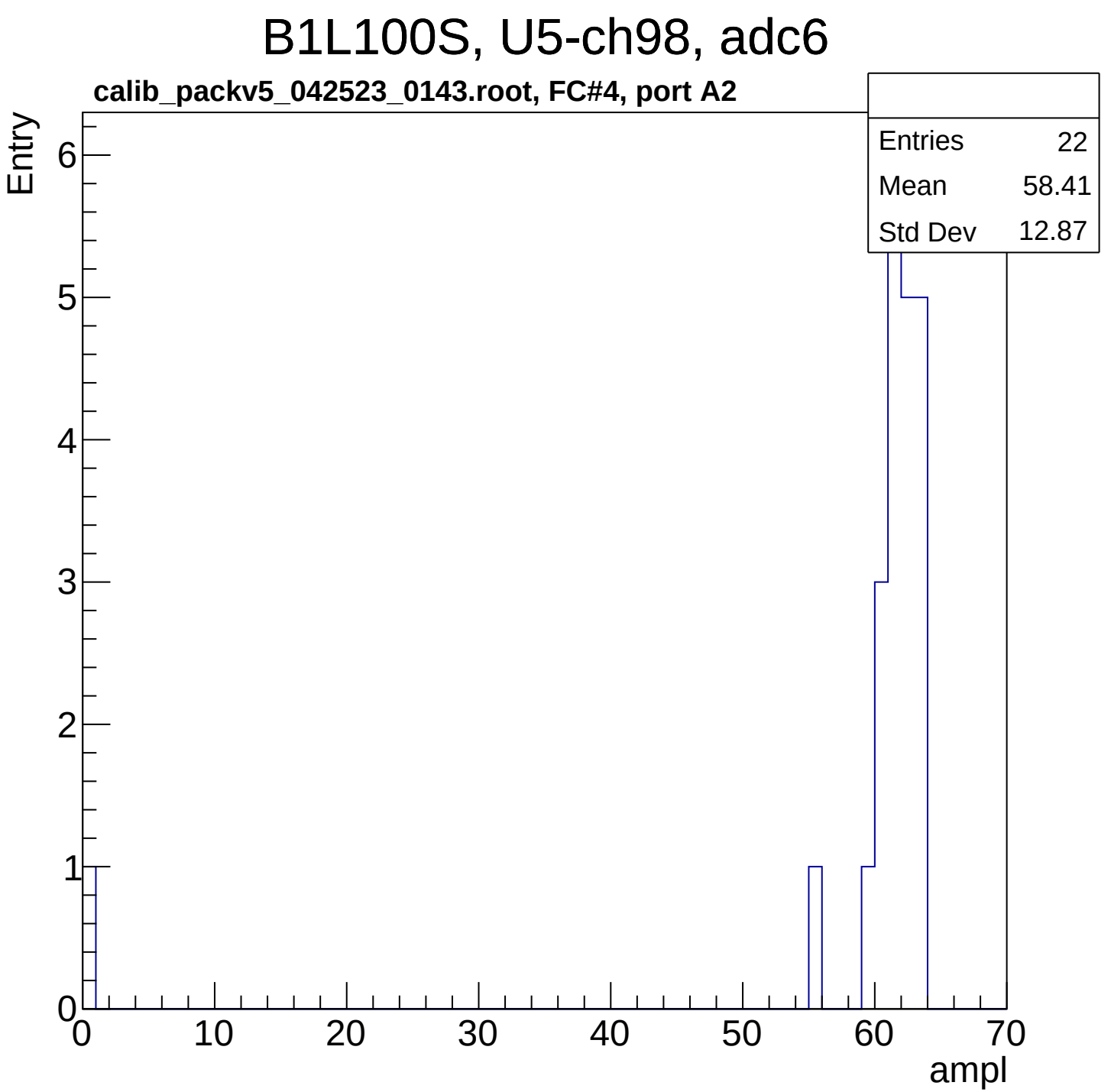
B1L100S, U5-ch98, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 22
Mean 58.41
Std Dev 12.87
Entry
0
1
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3
4
5
6
0
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20
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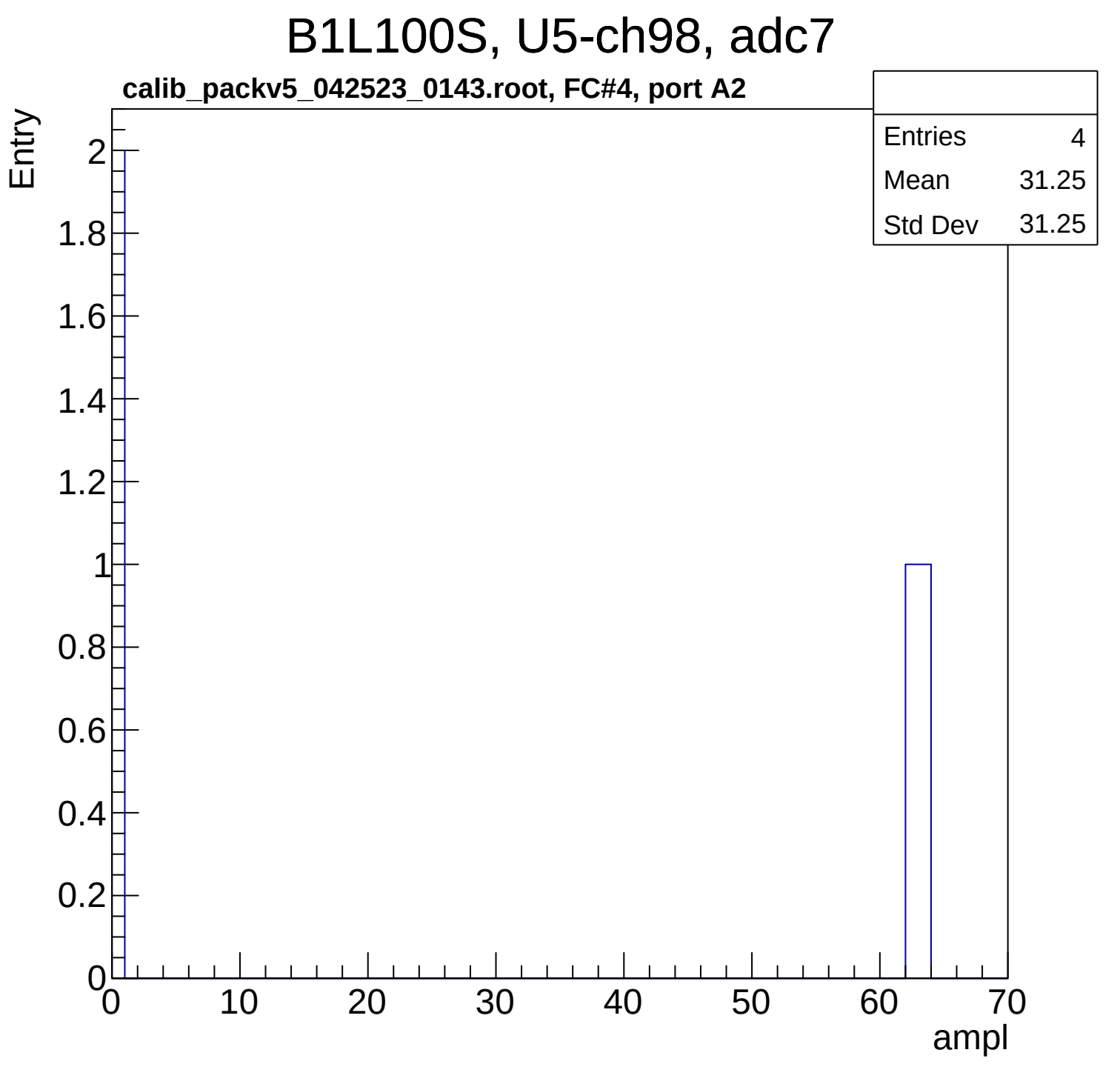
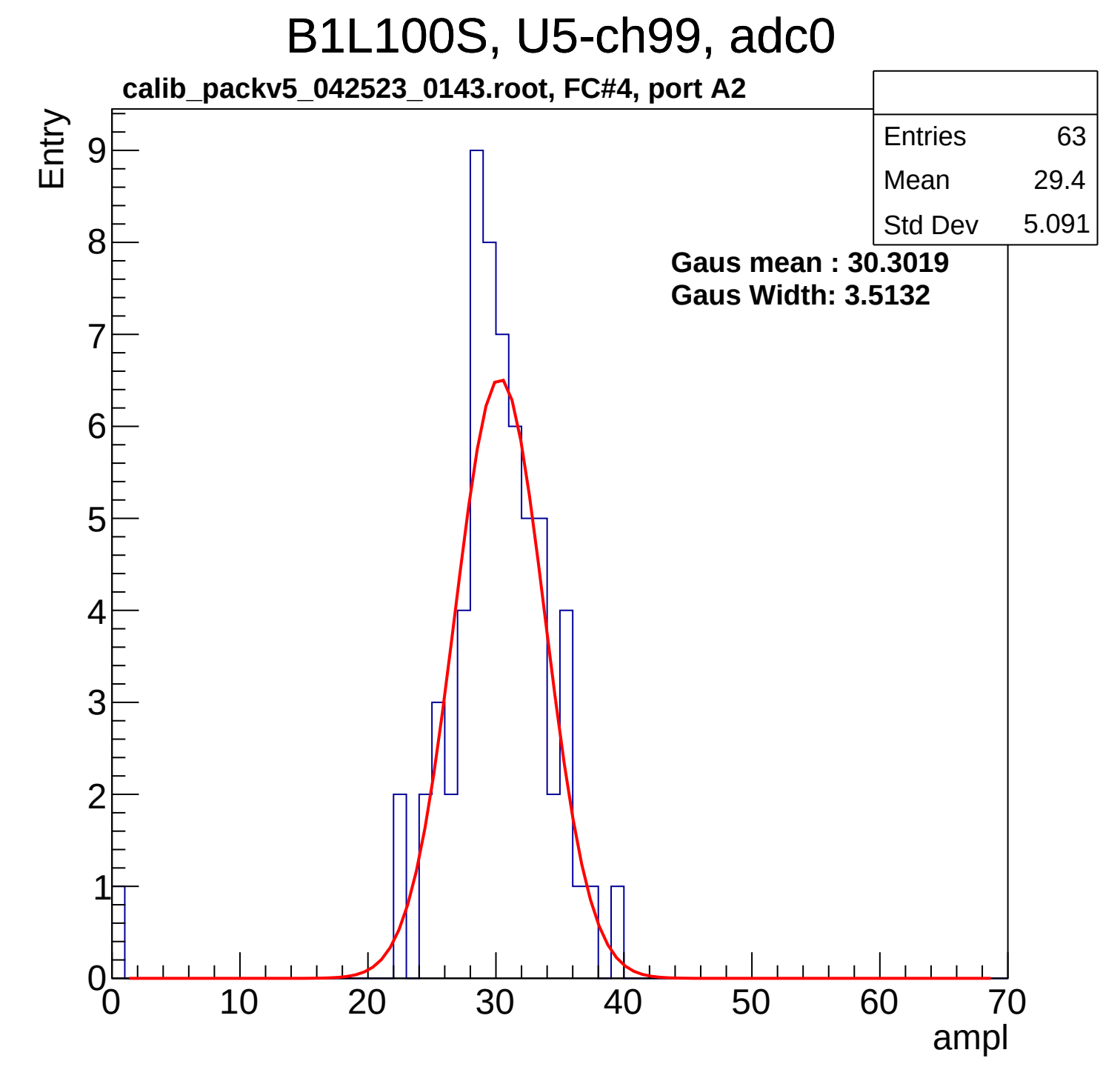
50
60
70
ampl


B1L100S, U5-ch98, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 4
Mean 31.25
Std Dev 31.25
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L100S, U5-ch99, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 29.4
Std Dev 5.091
Gaus mean : 30.3019
Gaus Width: 3.5132
Entry
ampl
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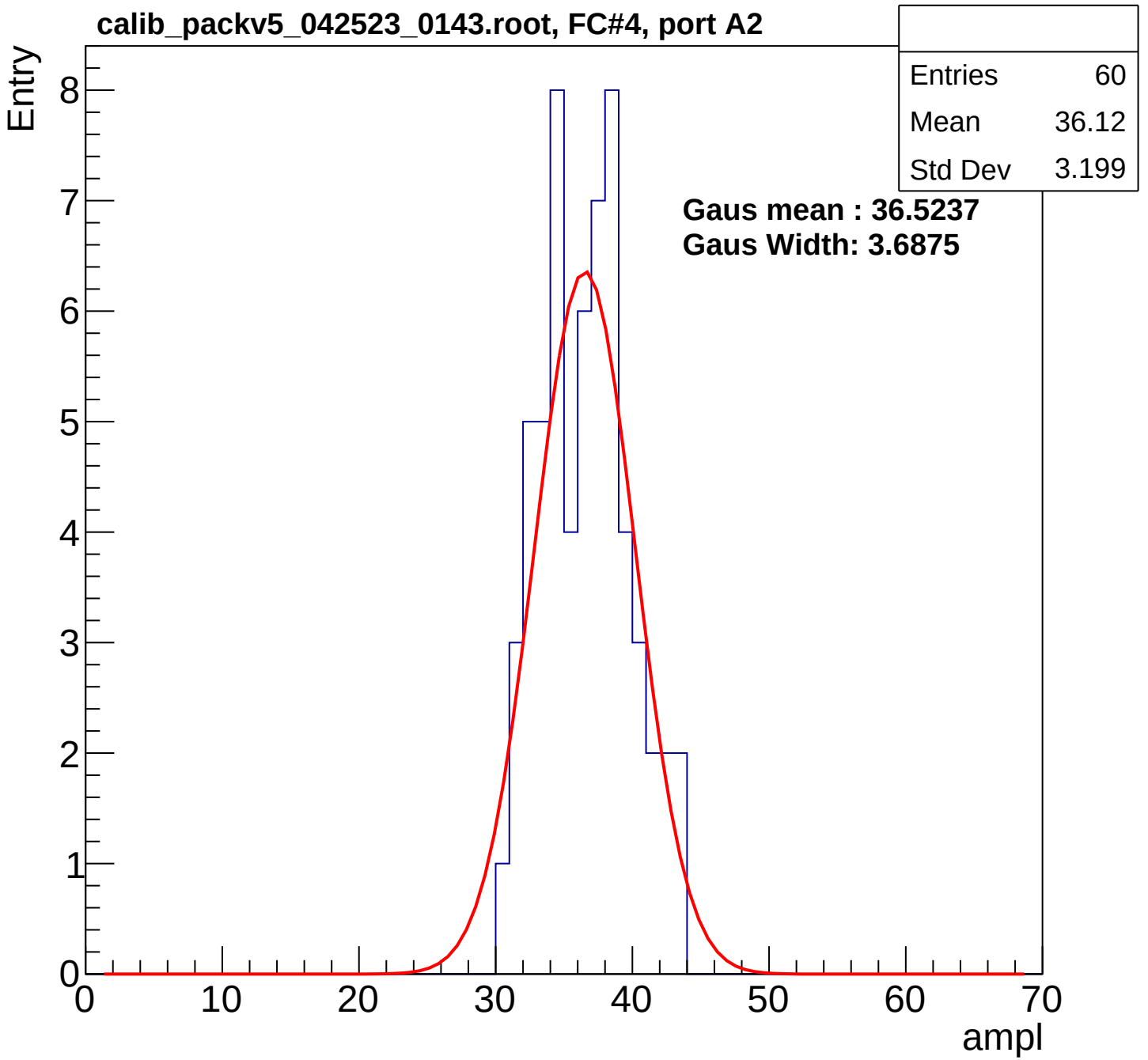
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch99, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 36.12
Std Dev 3.199
Gaus mean : 36.5237
Gaus Width: 3.6875
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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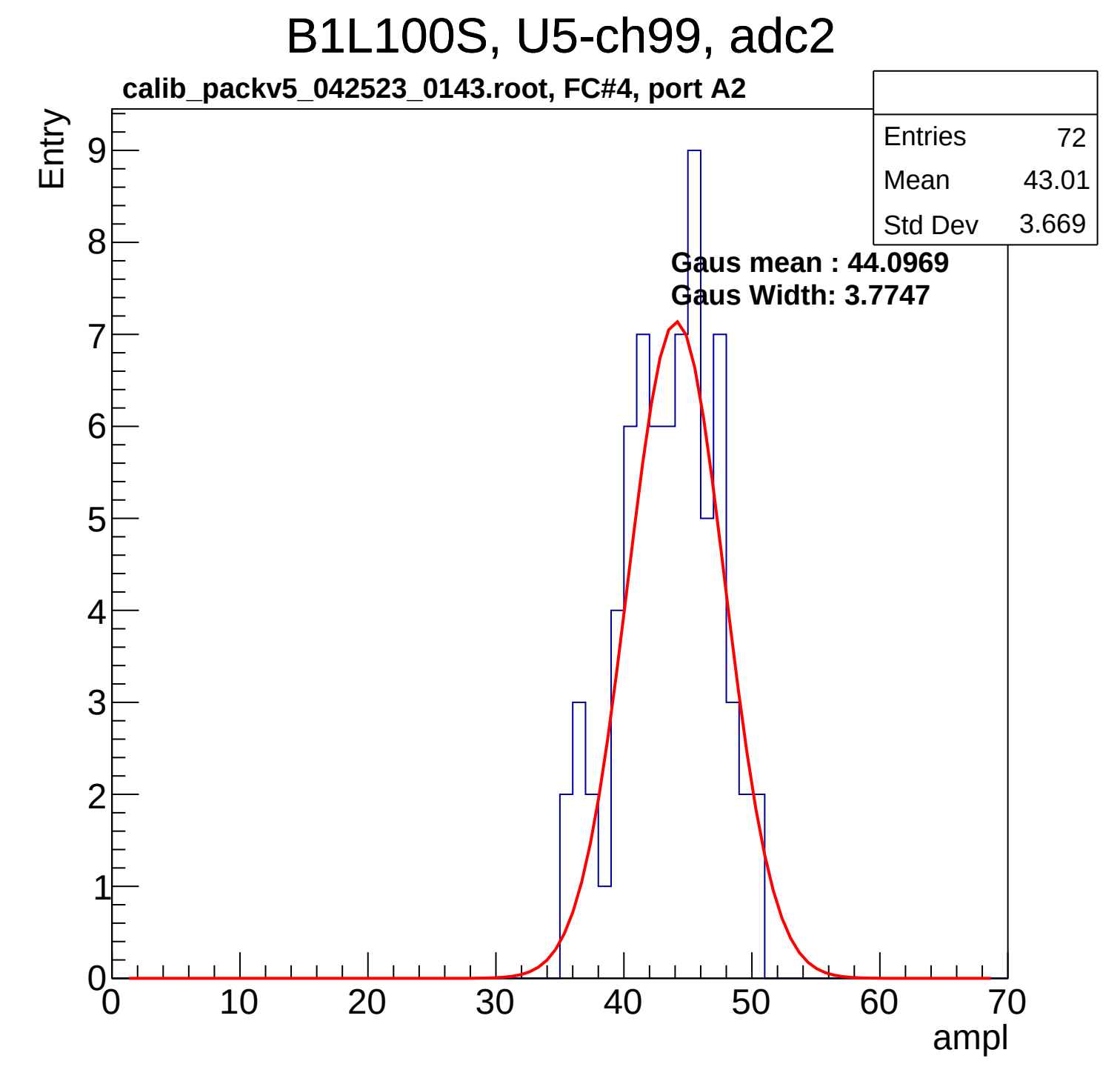
B1L100S, U5-ch99, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 43.01
Std Dev 3.669
Gaus mean : 44.0969
Gaus Width: 3.7747
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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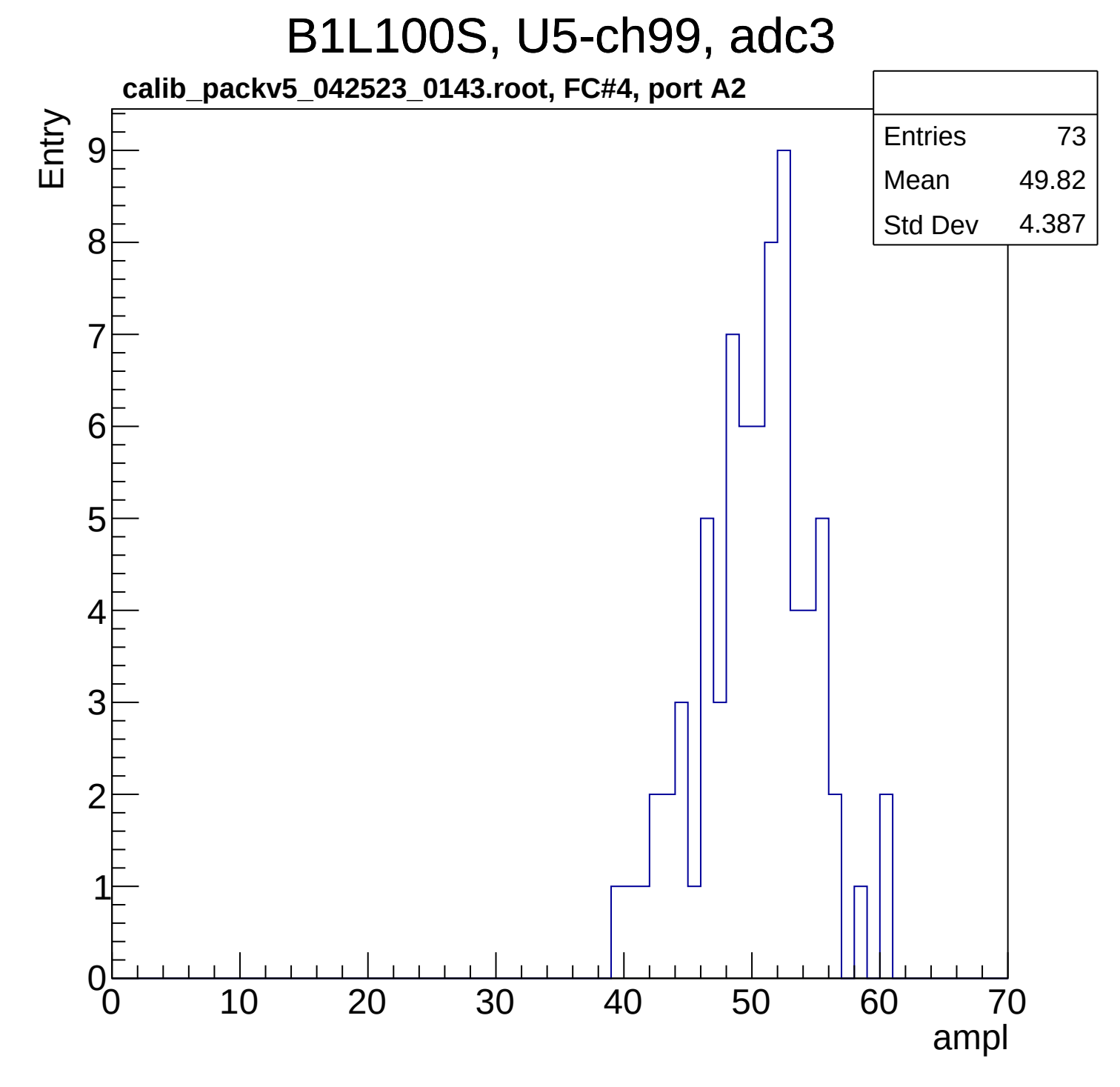
B1L100S, U5-ch99, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 49.82
Std Dev 4.387
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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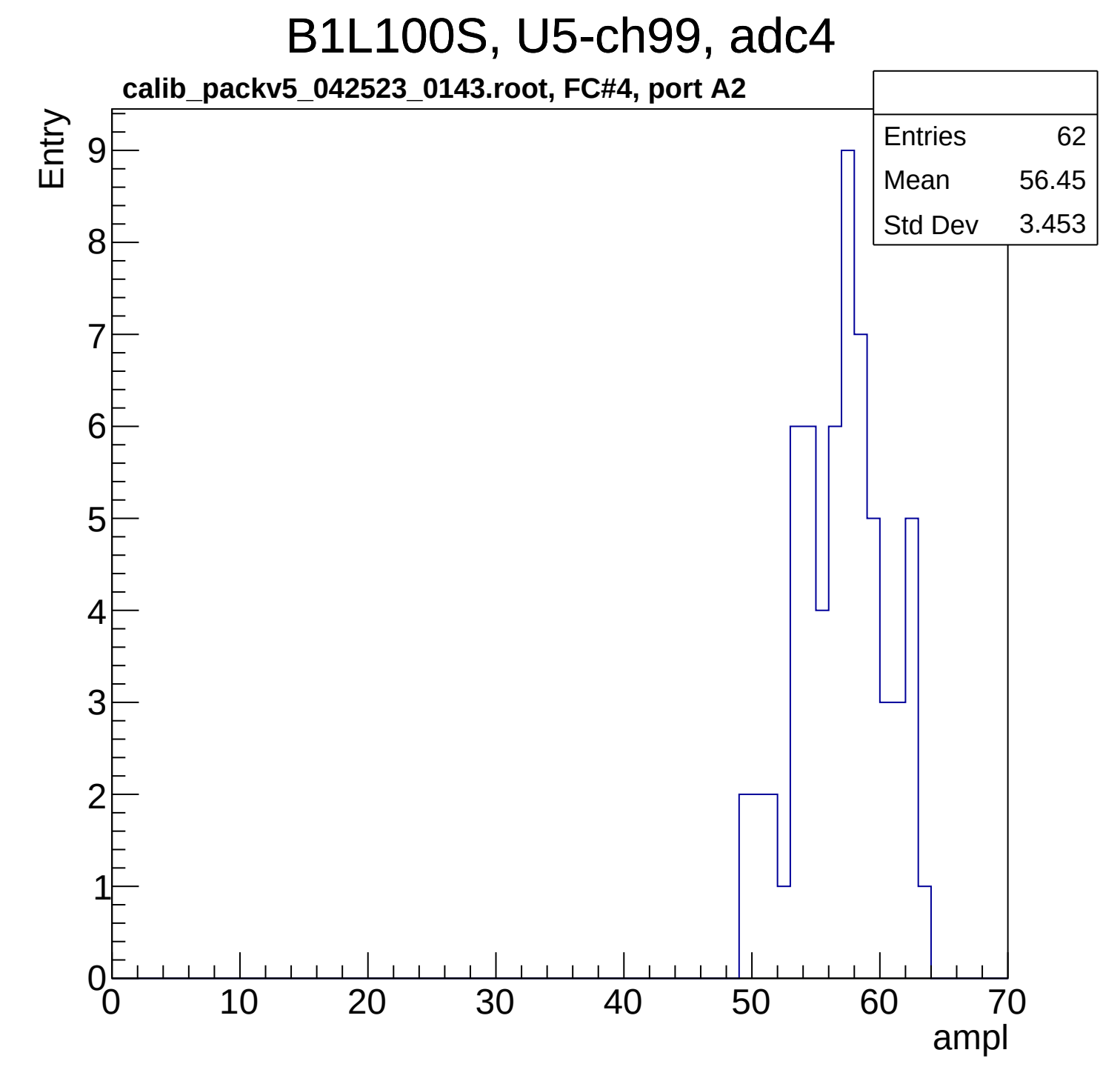
B1L100S, U5-ch99, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 56.45
Std Dev 3.453
Entry
ampl
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2
3
4
5
6
7
8
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0
10
20
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60
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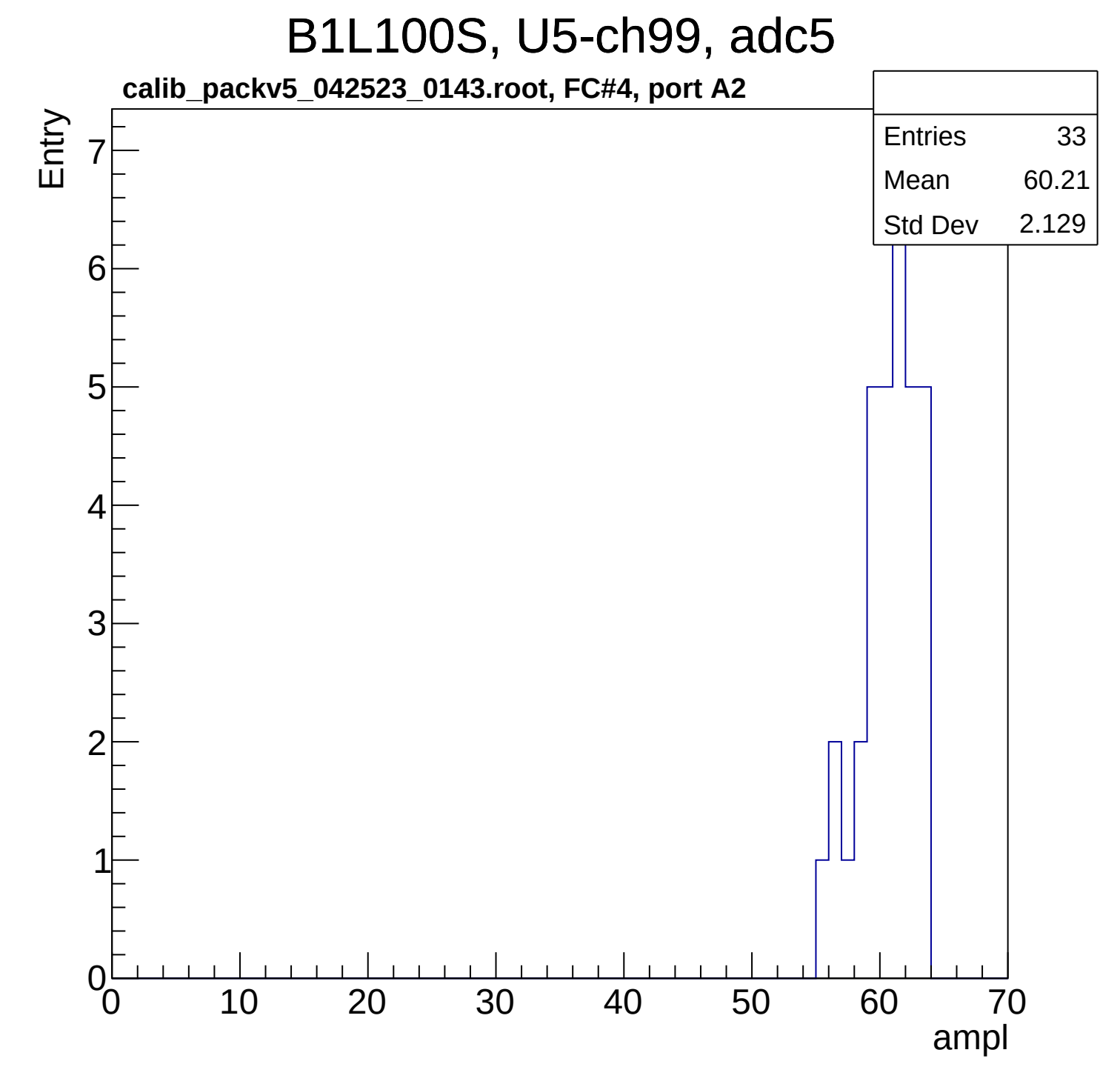
B1L100S, U5-ch99, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 33
Mean 60.21
Std Dev 2.129
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
50
60
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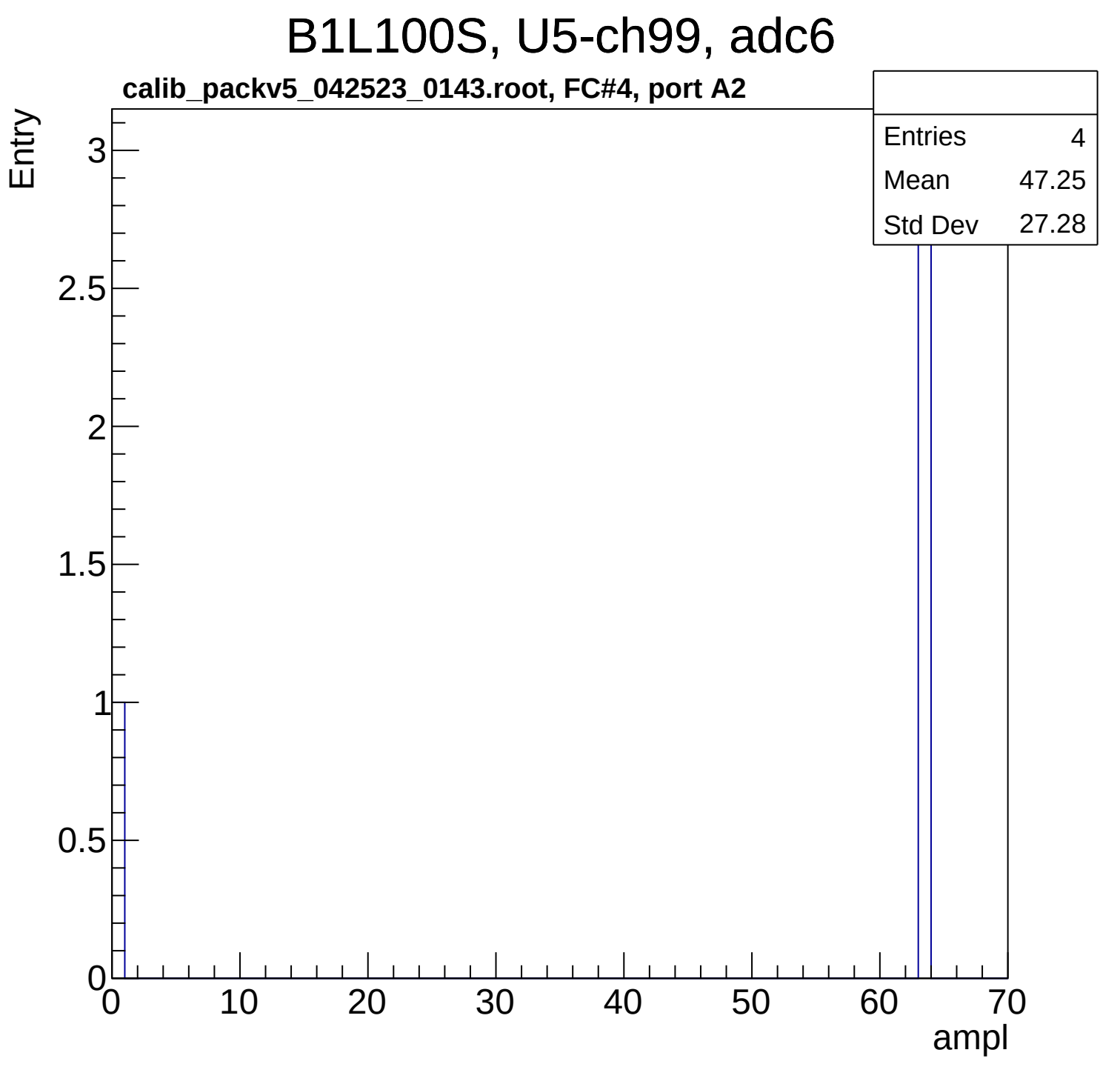
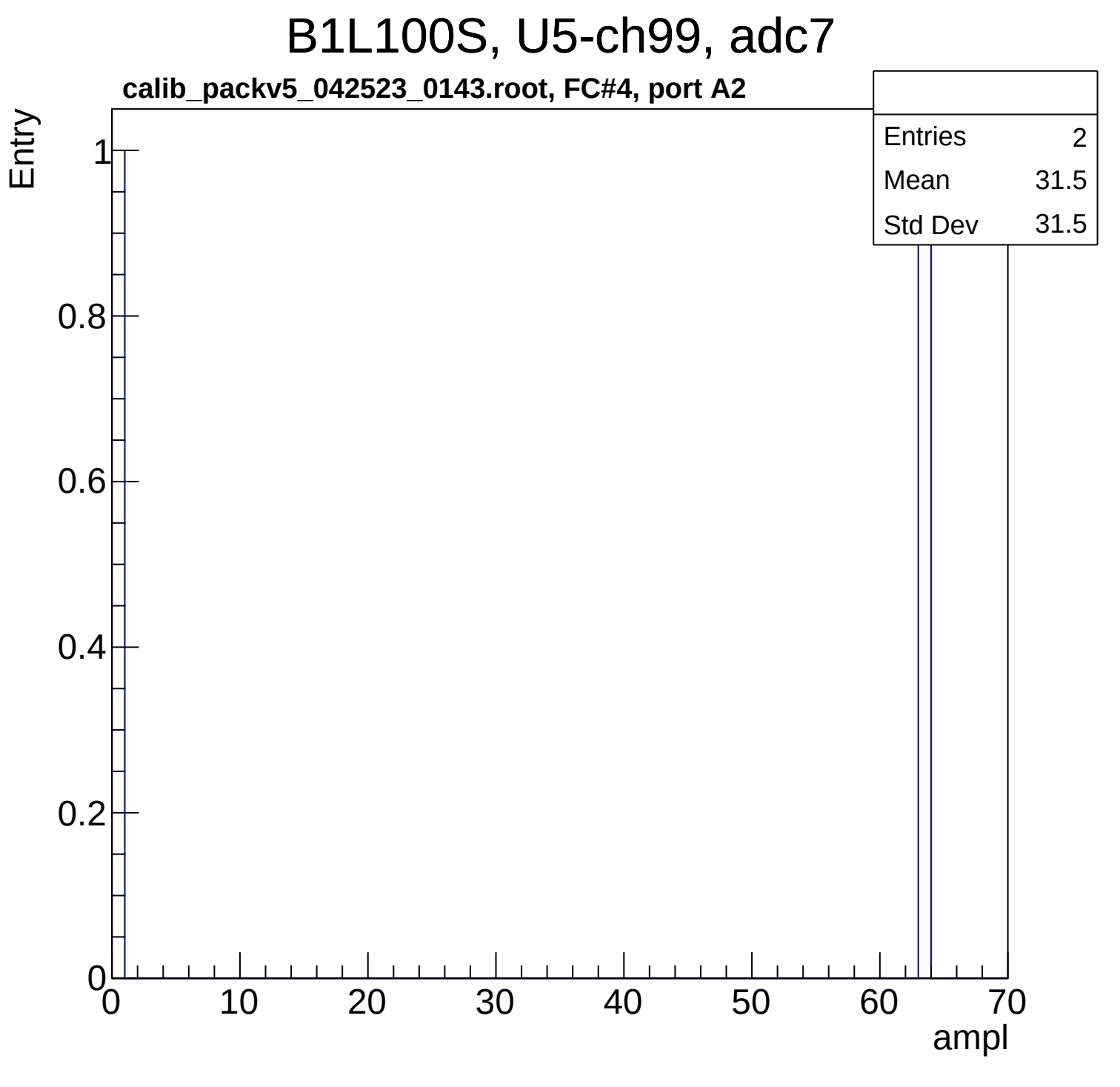

B1L100S, U5-ch99, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 4
Mean 47.25
Std Dev 27.28
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L100S, U5-ch99, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 31.5
Std Dev 31.5
Entry
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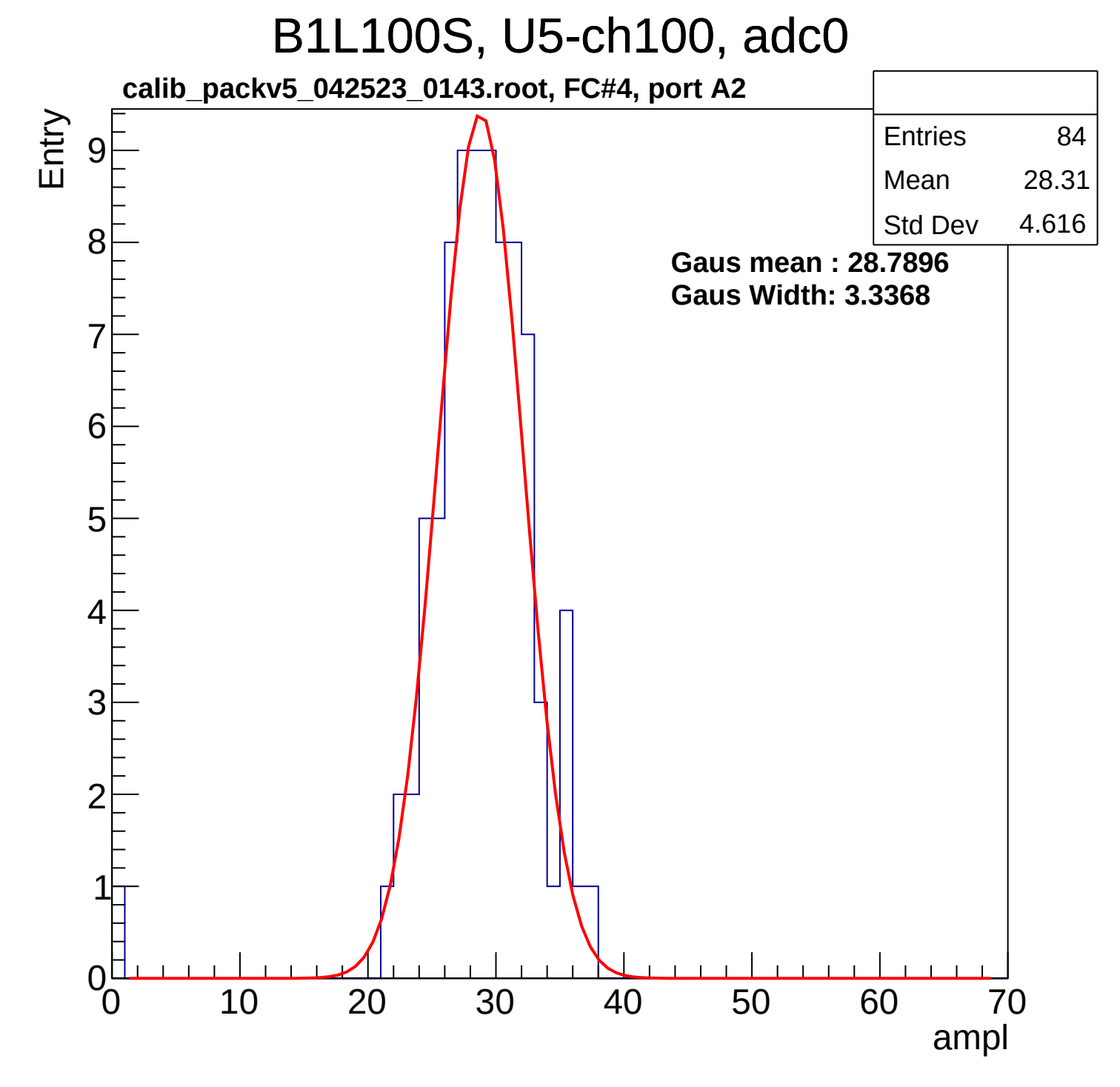
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch100, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 84
Mean 28.31
Std Dev 4.616
Gaus mean : 28.7896
Gaus Width: 3.3368
Entry
ampl
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2
3
4
5
6
7
8
9
0
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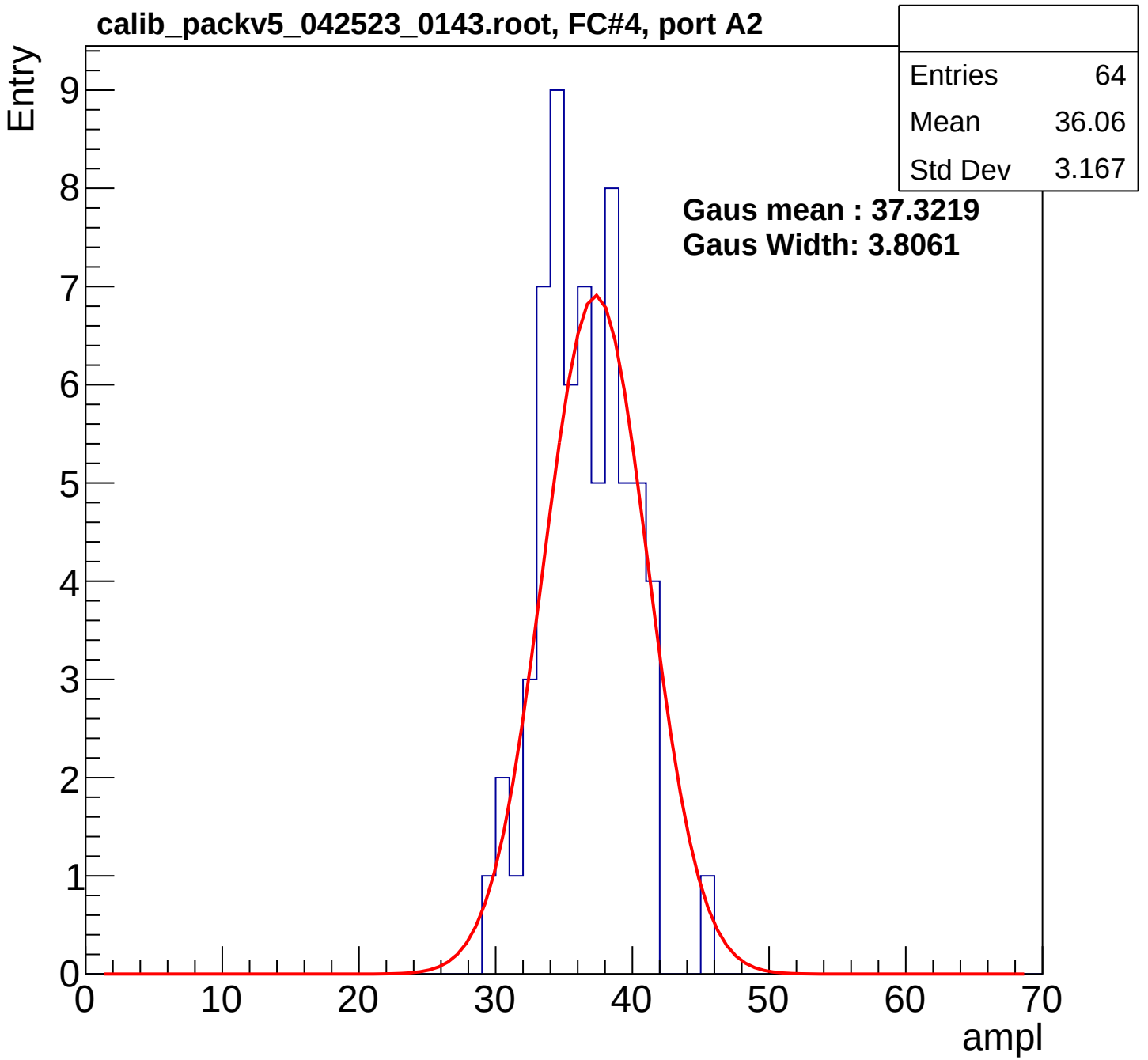
20
30
40
50
60
70


B1L100S, U5-ch100, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 36.06
Std Dev 3.167
Gaus mean : 37.3219
Gaus Width: 3.8061
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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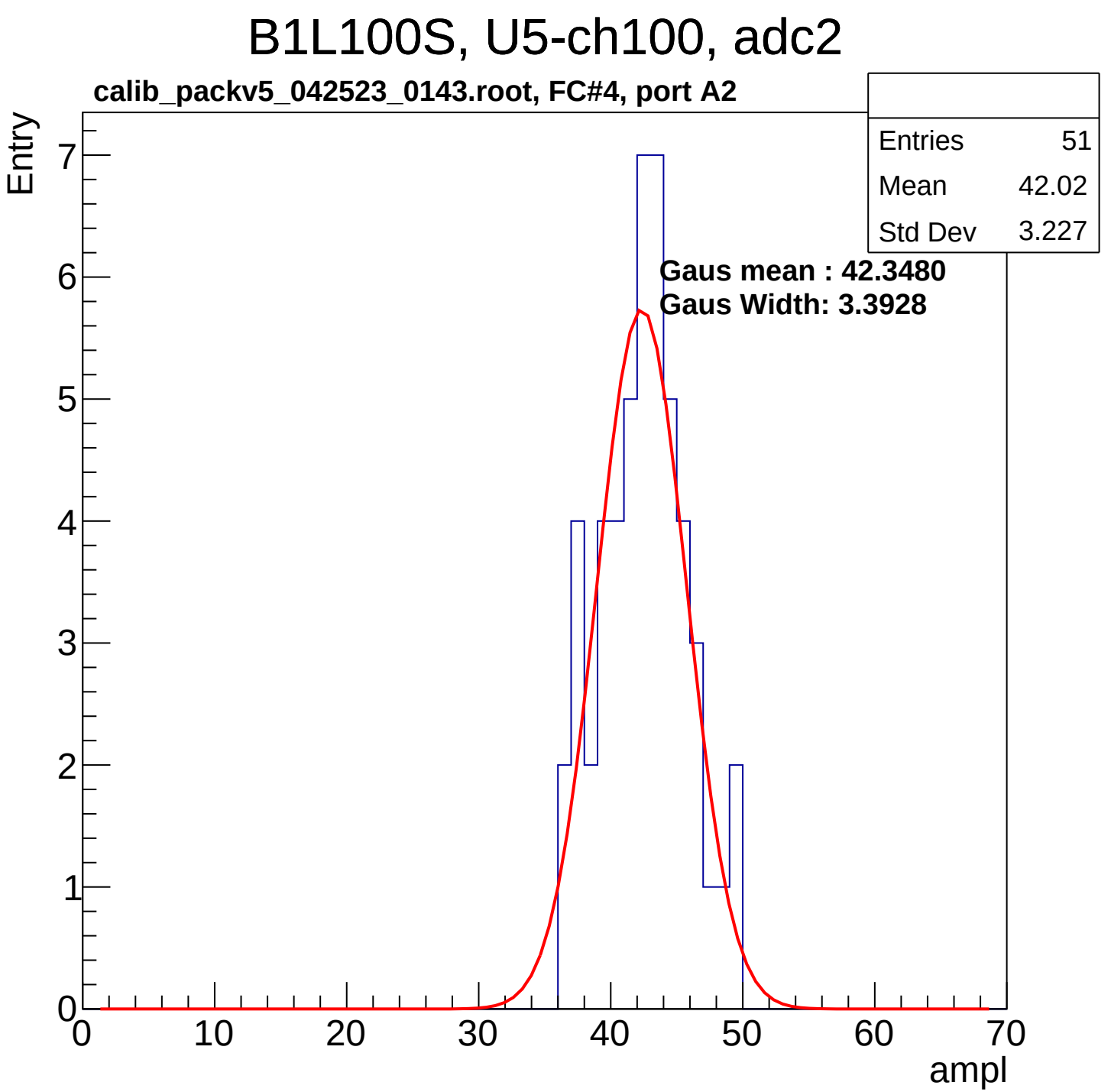
20
30
40
50
60
70


B1L100S, U5-ch100, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 42.02
Std Dev 3.227
Gaus mean : 42.3480
Gaus Width: 3.3928
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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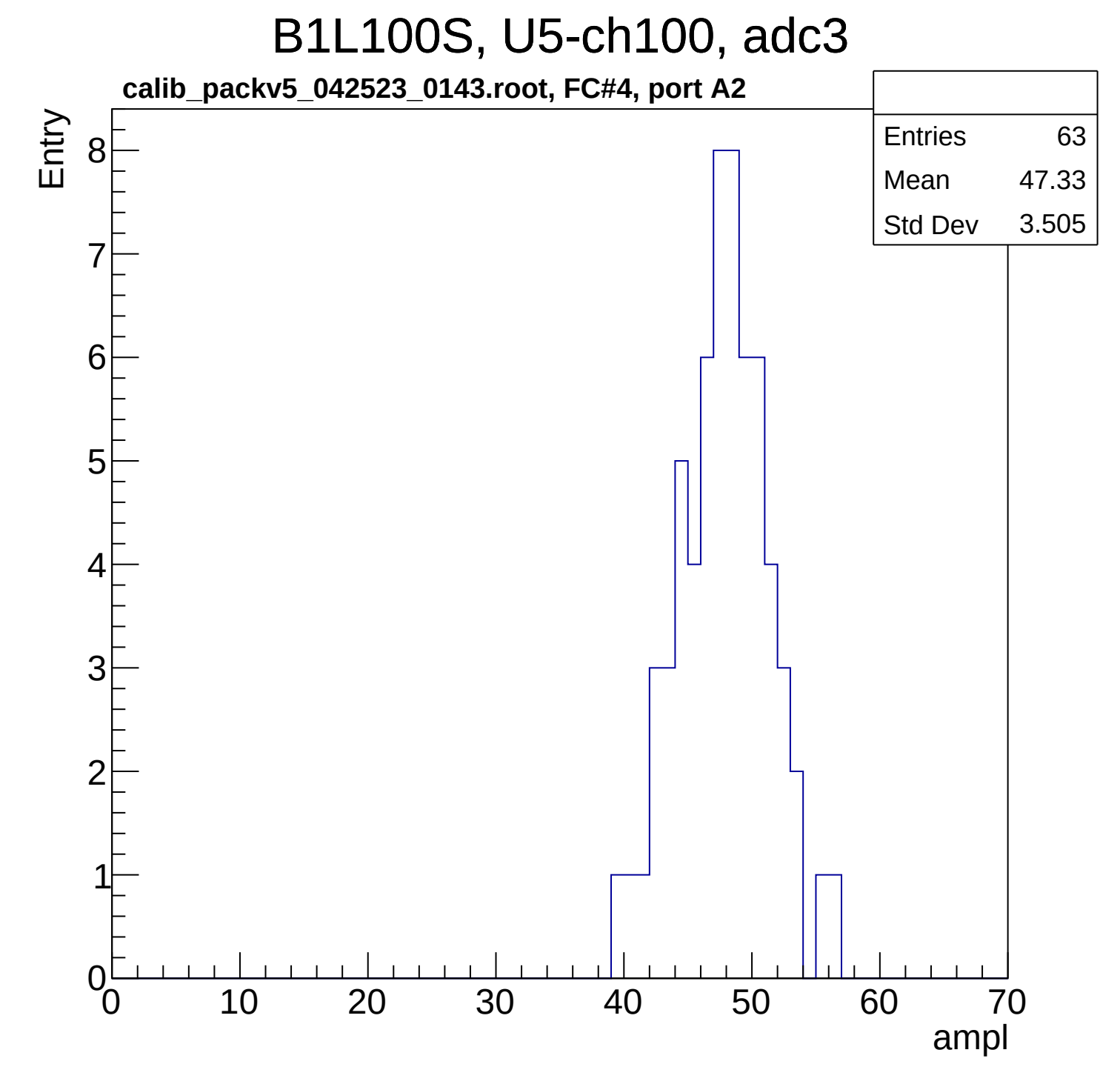
B1L100S, U5-ch100, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 47.33
Std Dev 3.505
Entry
ampl
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2
3
4
5
6
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0
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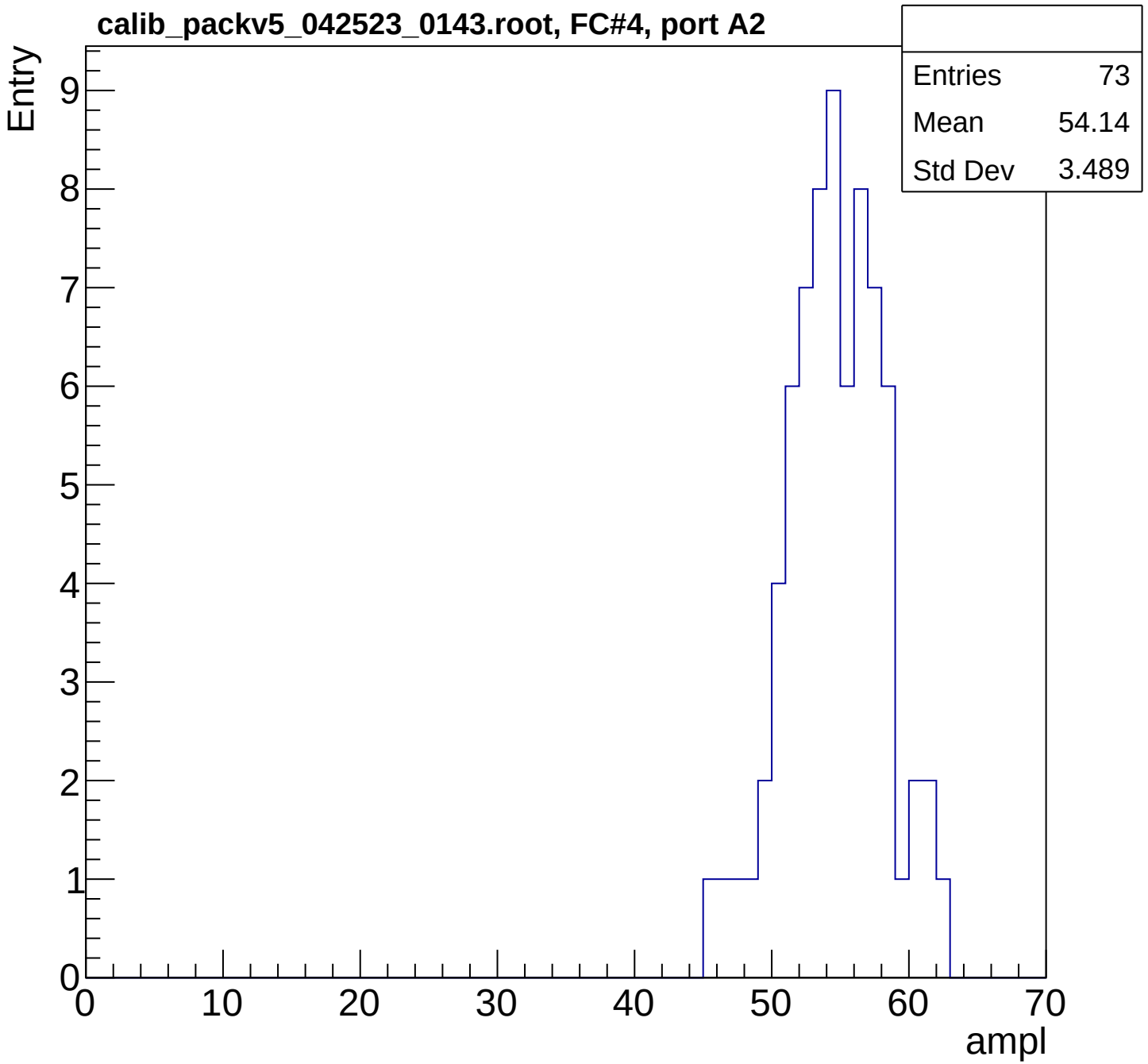
B1L100S, U5-ch100, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 54.14
Std Dev 3.489
Entry
ampl
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2
3
4
5
6
7
8
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0
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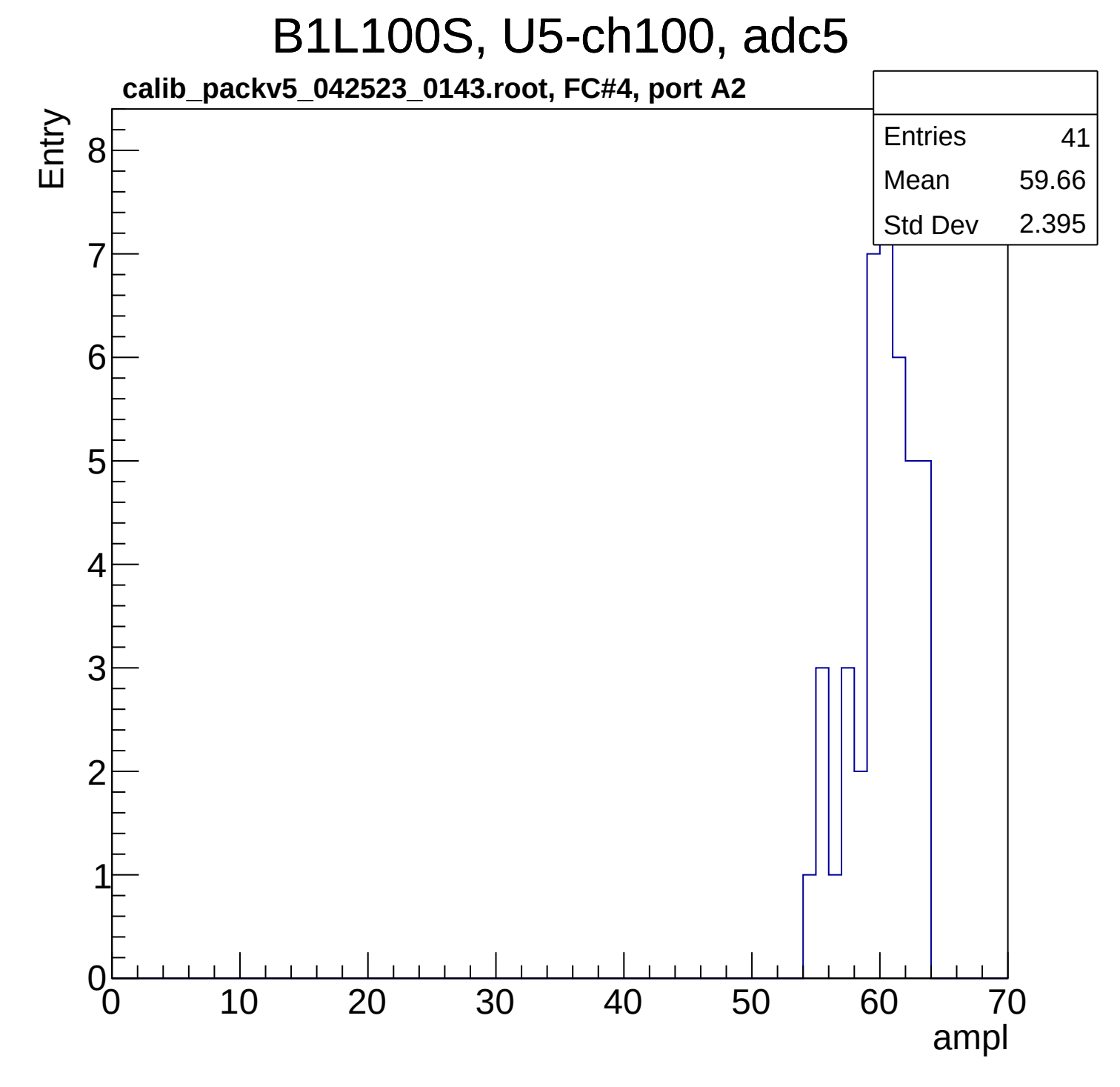
B1L100S, U5-ch100, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 41
Mean 59.66
Std Dev 2.395
Entry
ampl
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3
4
5
6
7
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0
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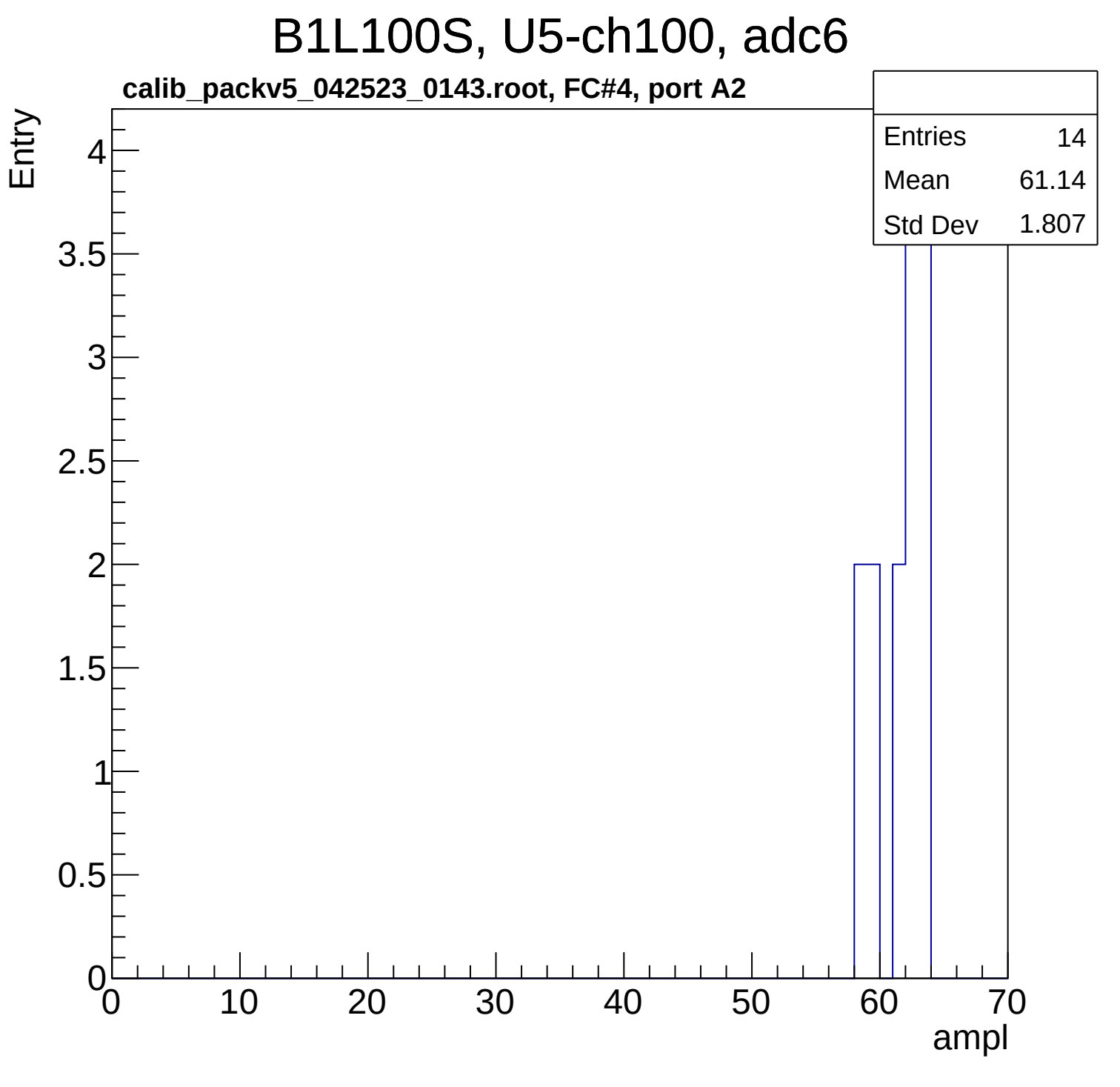
B1L100S, U5-ch100, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 14
Mean 61.14
Std Dev 1.807
Entry
ampl
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1.5
2
2.5
3
3.5
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0
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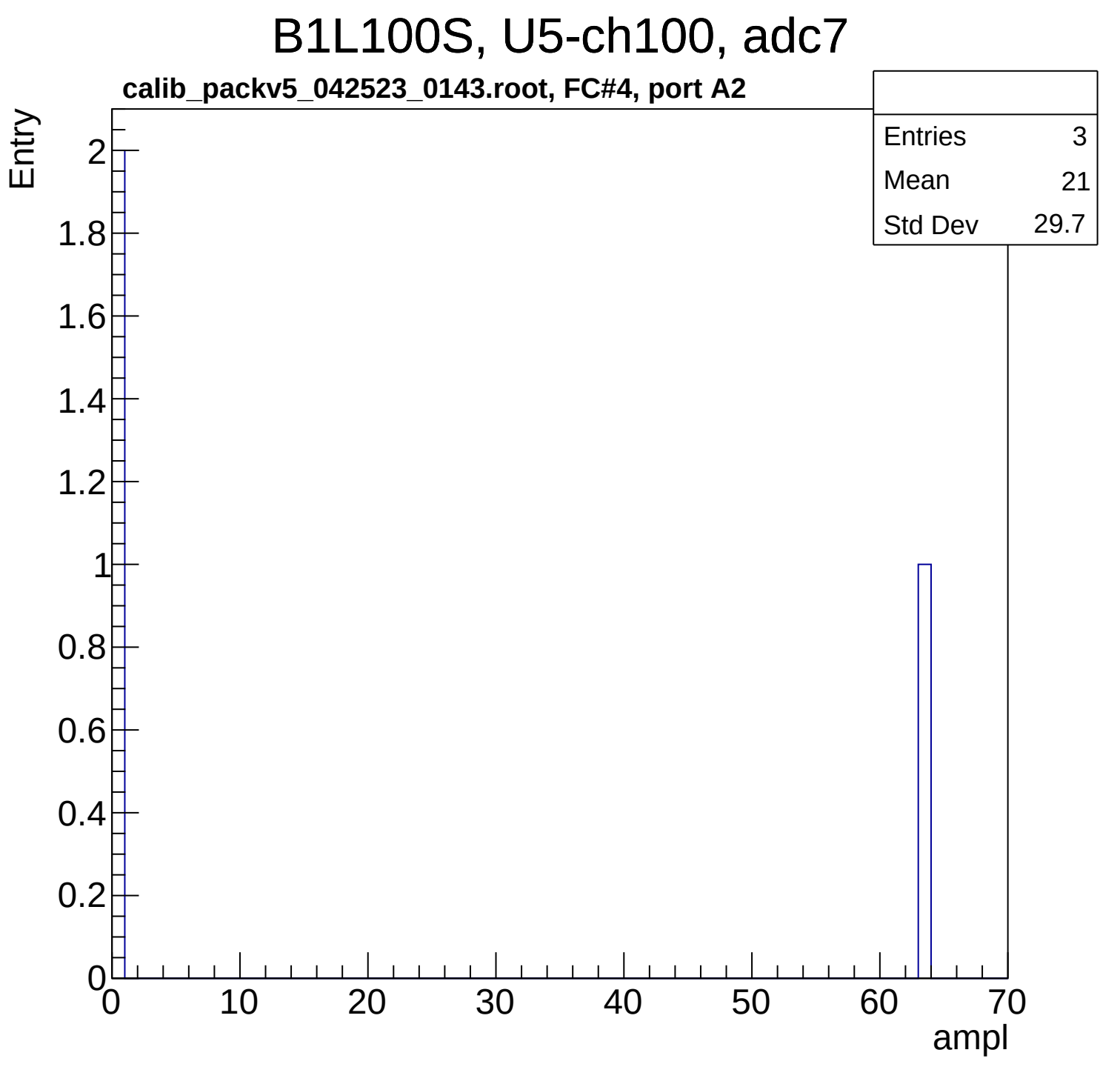
B1L100S, U5-ch100, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 21
Std Dev 29.7
Entry
ampl
0
0.2
0.4
0.6
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1
1.2
1.4
1.6
1.8
2
0
10
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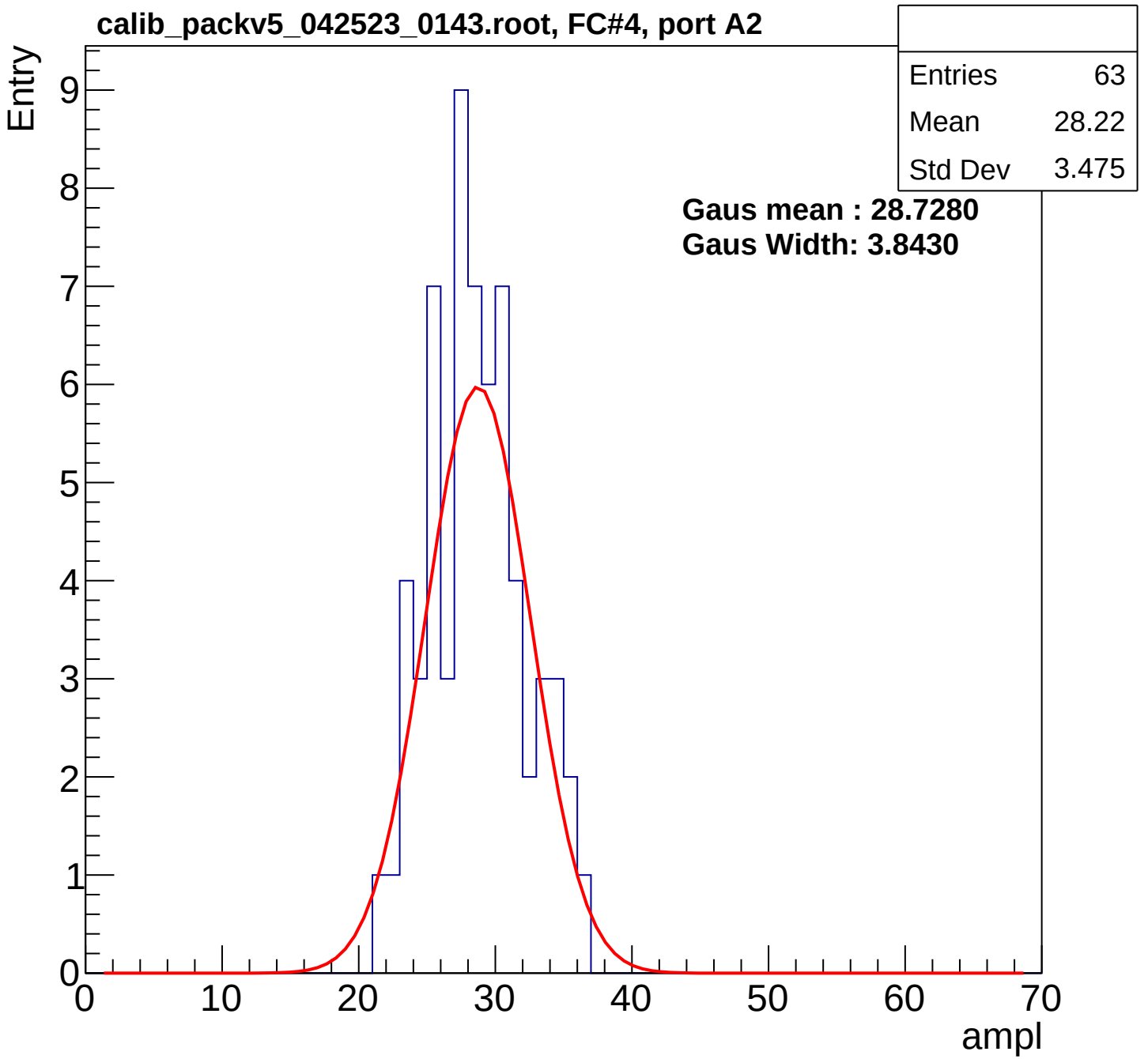
B1L100S, U5-ch101, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 28.22
Std Dev 3.475
Gaus mean : 28.7280
Gaus Width: 3.8430
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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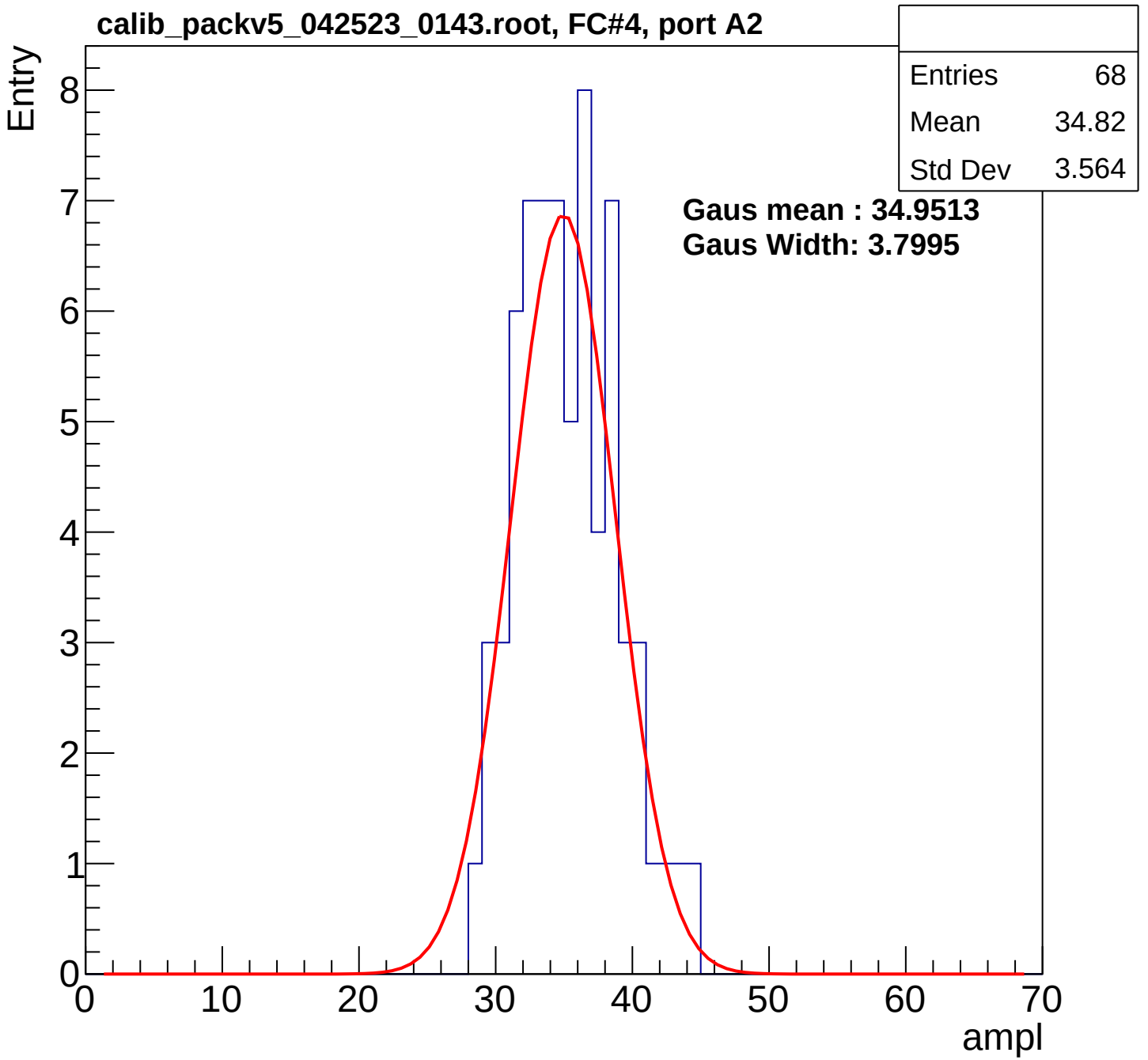
B1L100S, U5-ch101, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 34.82
Std Dev 3.564
Gaus mean : 34.9513
Gaus Width: 3.7995
Entry
ampl
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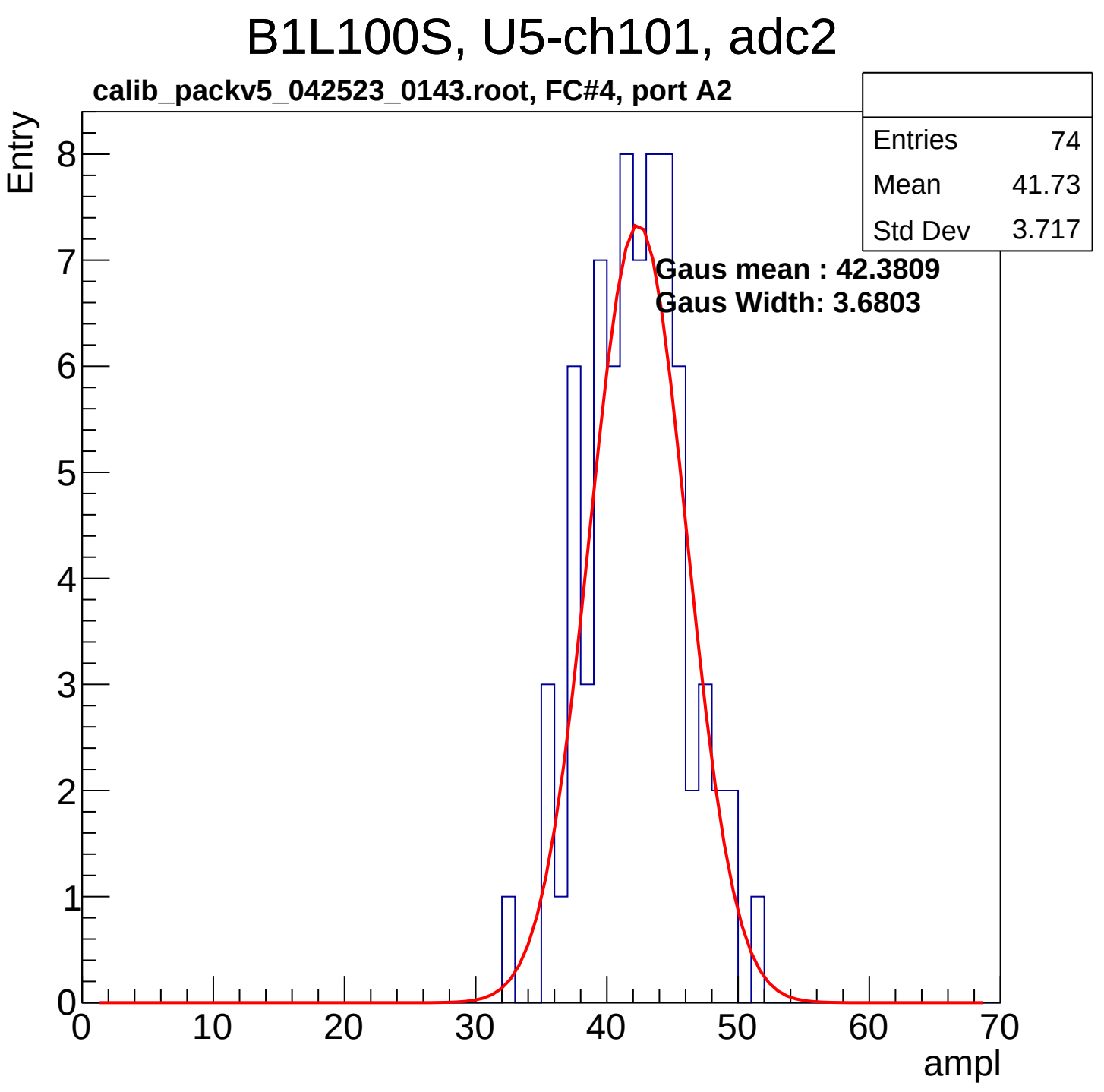
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch101, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 74
Mean 41.73
Std Dev 3.717
Gaus mean : 42.3809
Gaus Width: 3.6803
Entry
ampl
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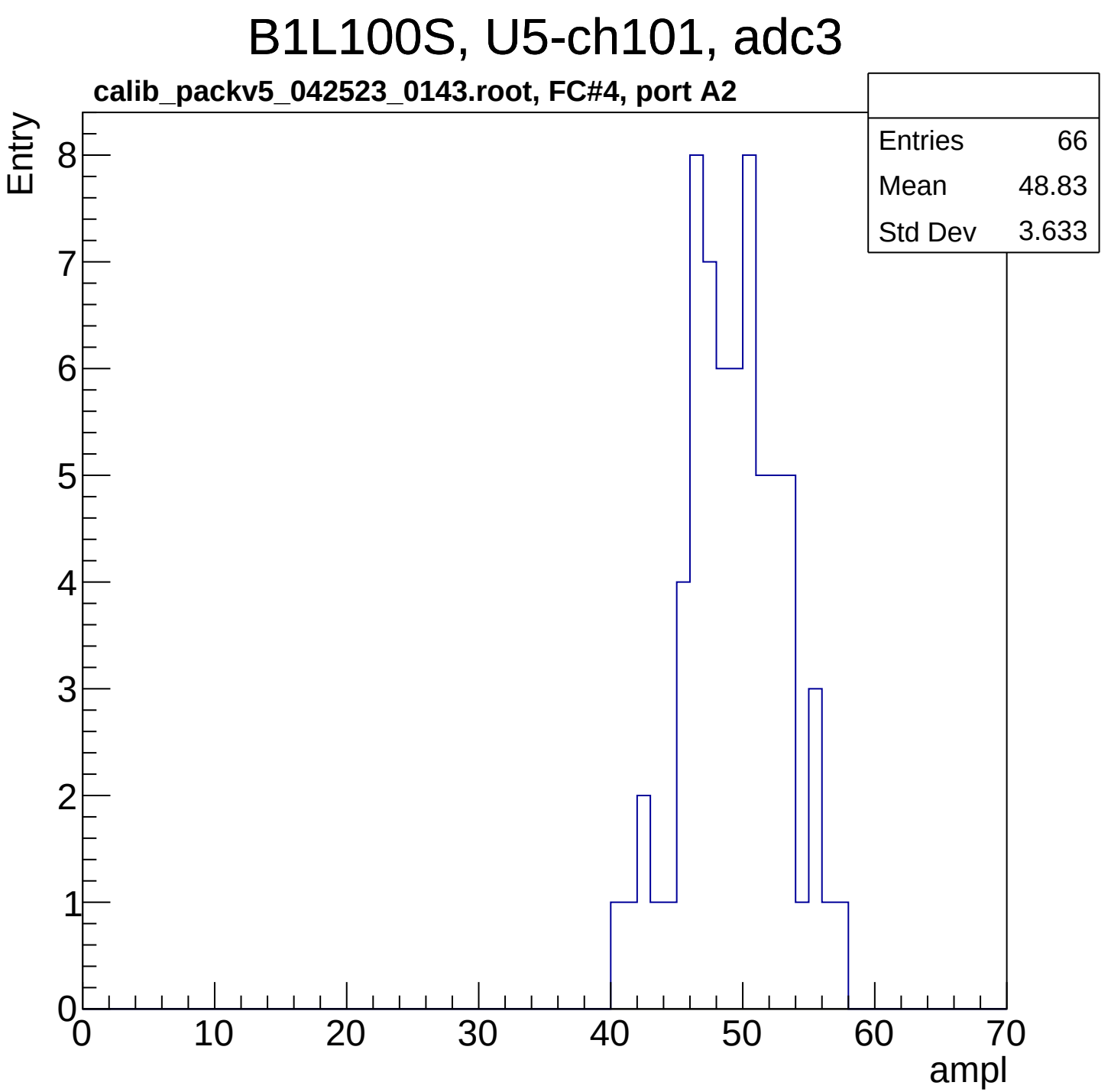
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch101, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 48.83
Std Dev 3.633
Entry
ampl
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4
5
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0
10
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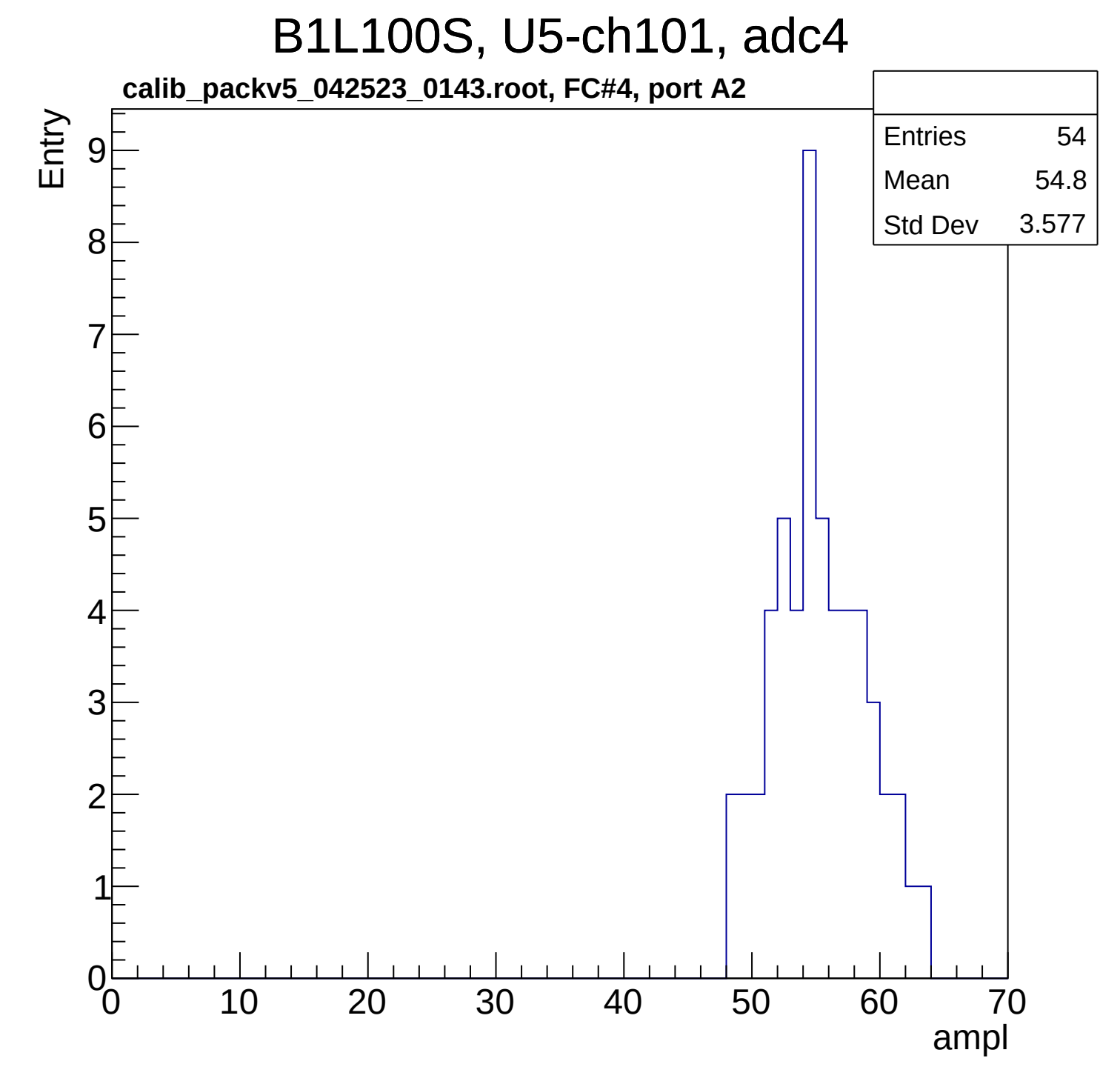
B1L100S, U5-ch101, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 54.8
Std Dev 3.577
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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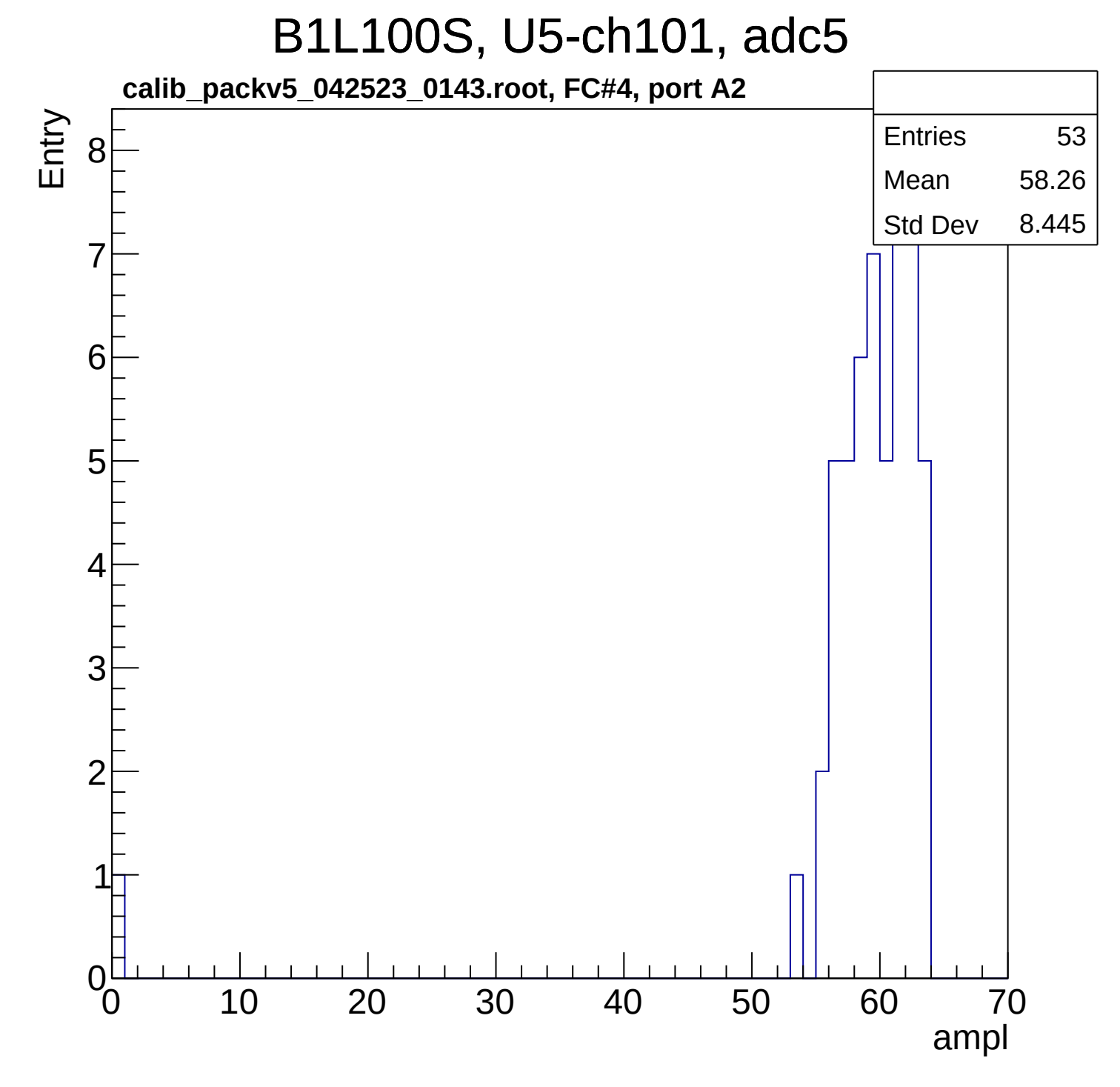
B1L100S, U5-ch101, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 58.26
Std Dev 8.445
Entry
ampl
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2
3
4
5
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0
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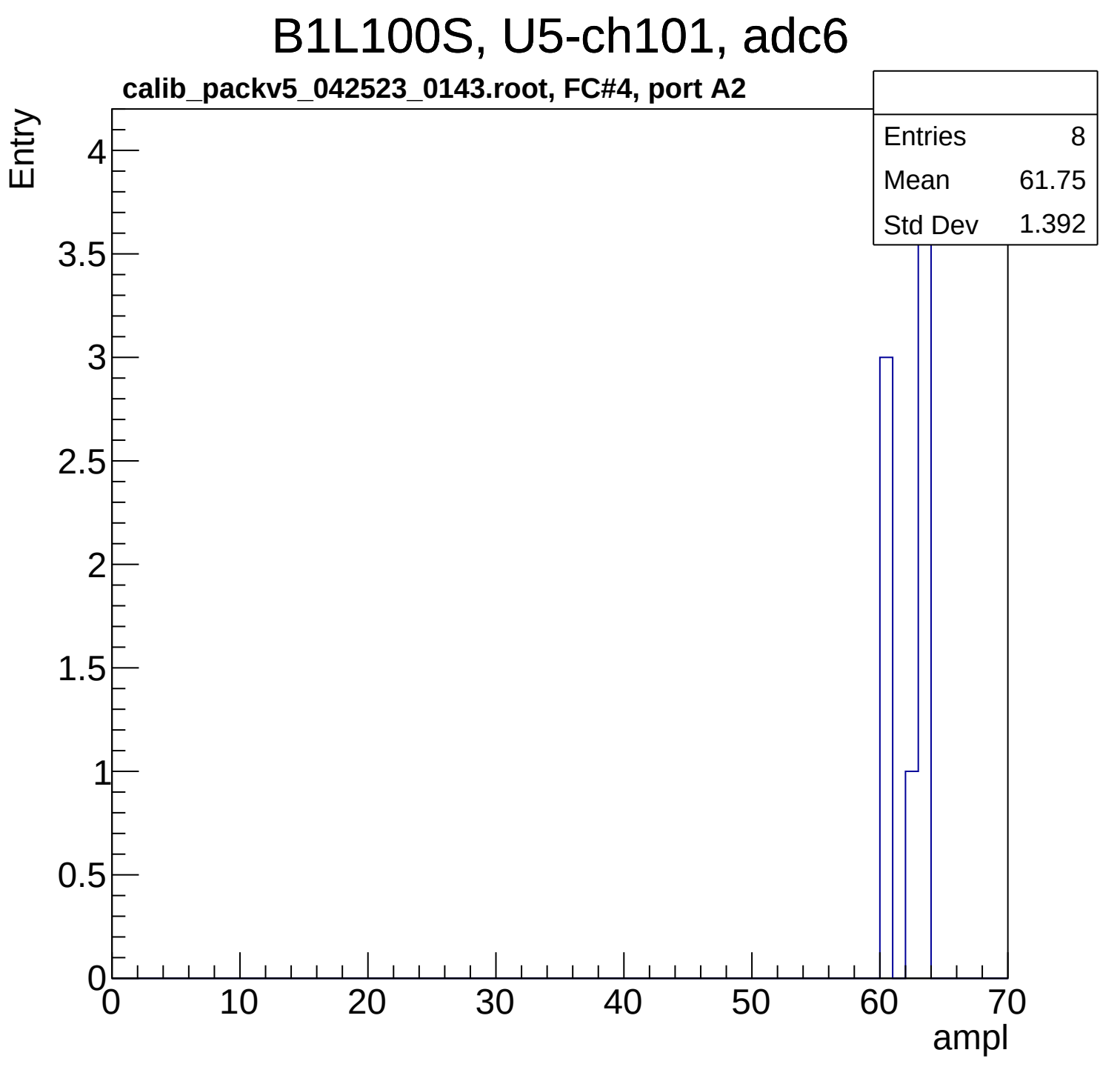
B1L100S, U5-ch101, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 8
Mean 61.75
Std Dev 1.392
Entry
ampl
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0.5
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1.5
2
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3
3.5
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0
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60
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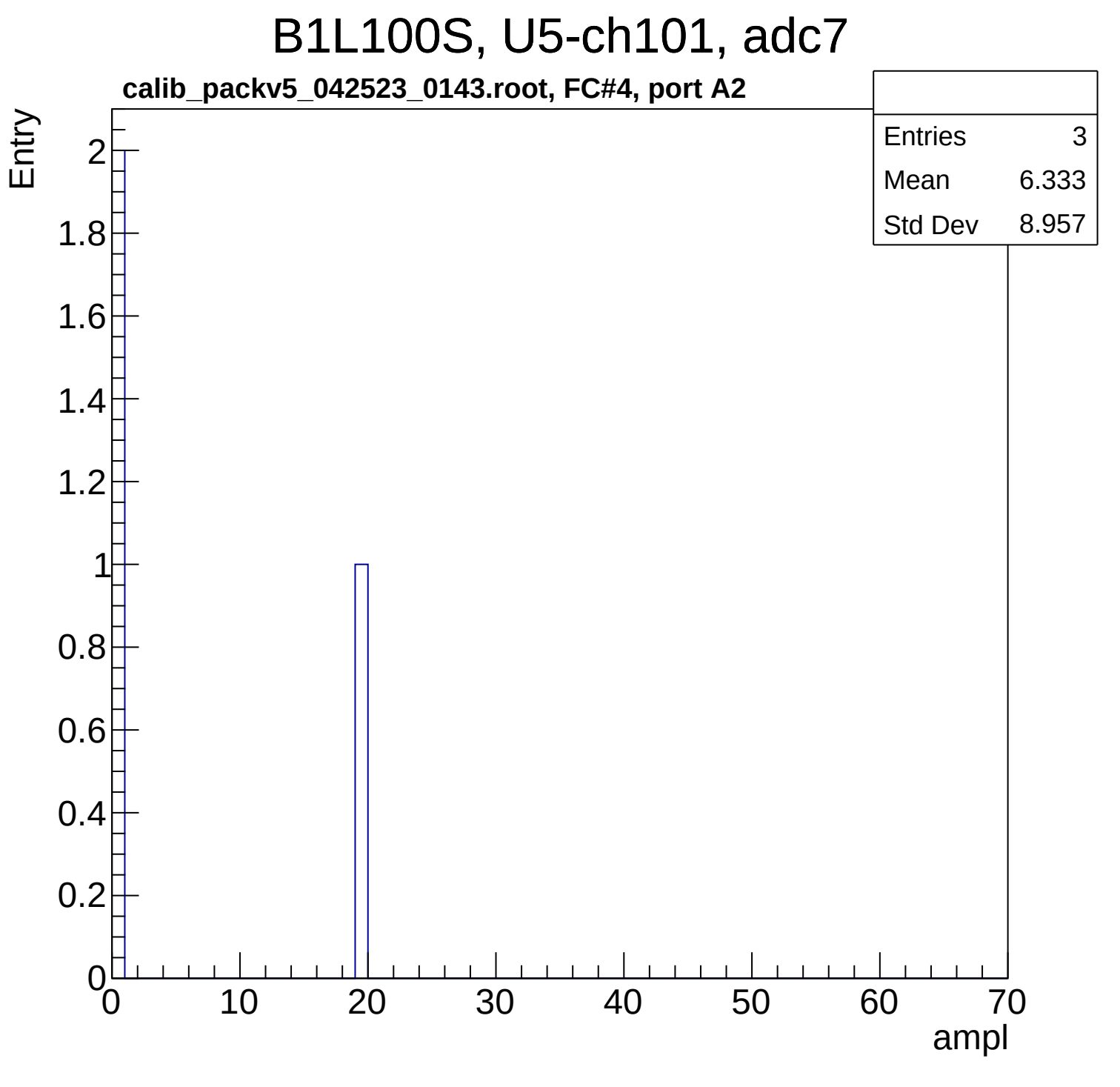
B1L100S, U5-ch101, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 6.333
Std Dev 8.957
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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20
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40
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60
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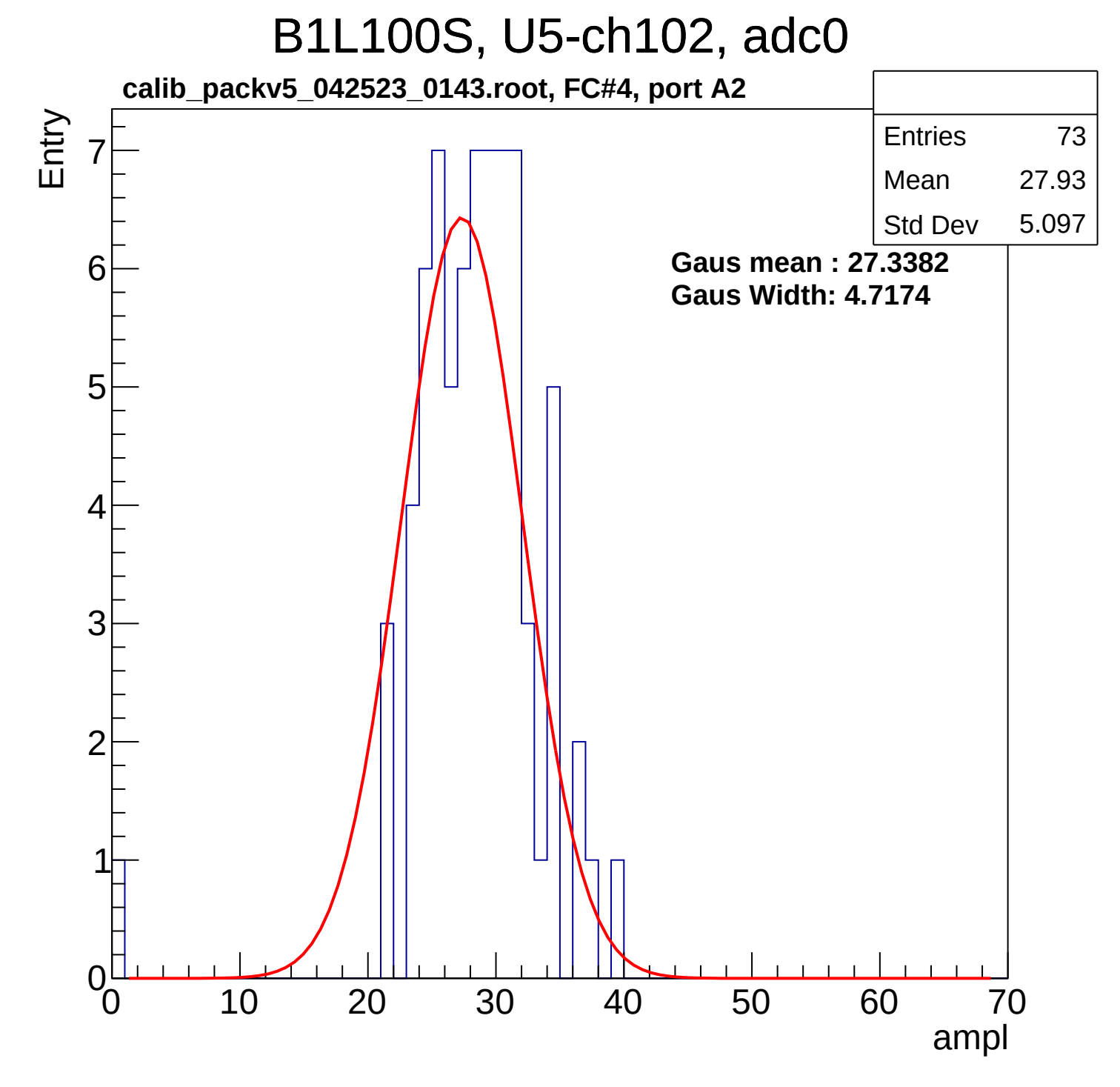
B1L100S, U5-ch102, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 27.93
Std Dev 5.097
Gaus mean : 27.3382
Gaus Width: 4.7174
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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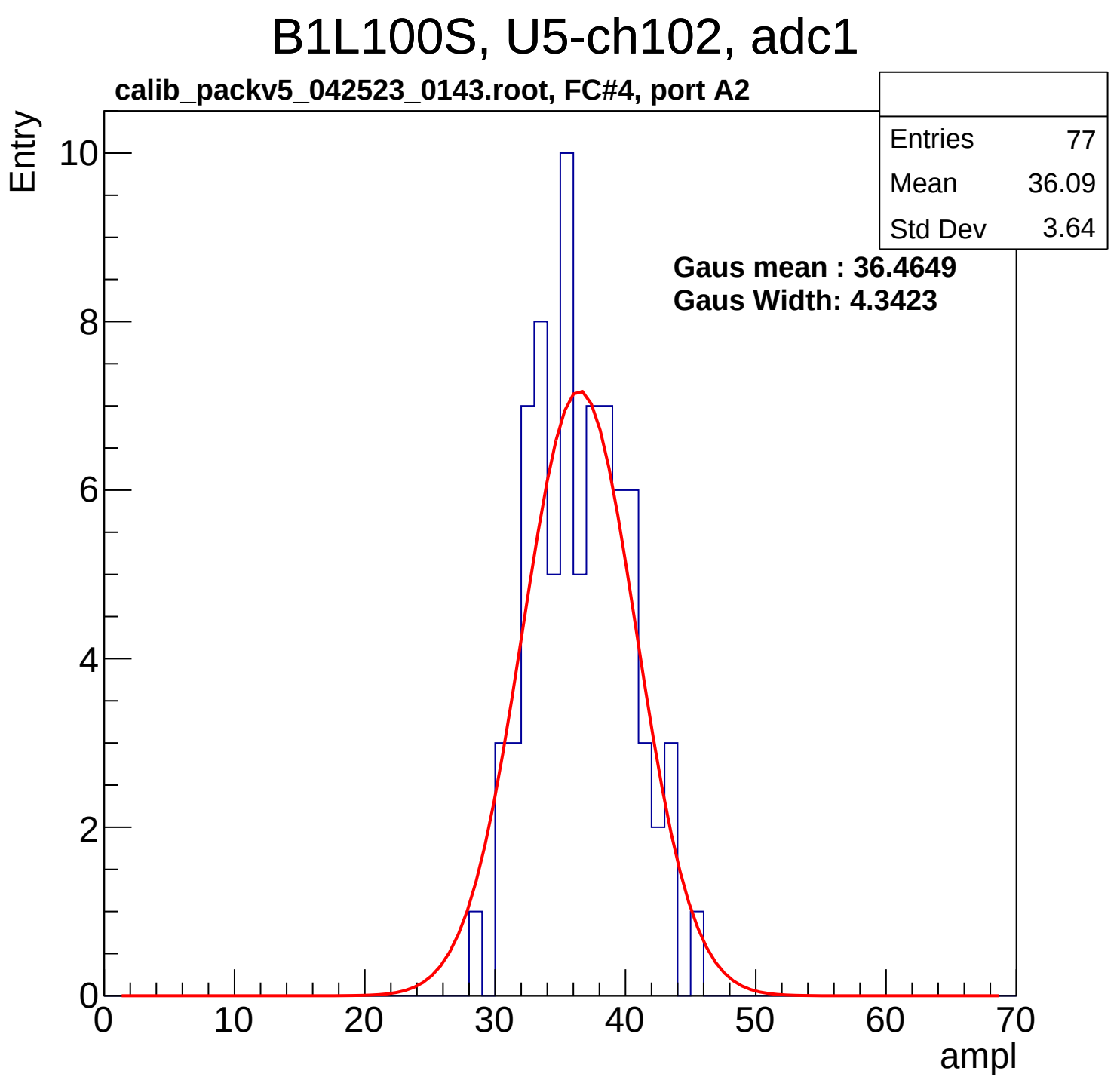
B1L100S, U5-ch102, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 77
Mean 36.09
Std Dev 3.64
Gaus mean : 36.4649
Gaus Width: 4.3423
Entry
ampl
0
2
4
6
8
10
0
10
20
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40
50
60
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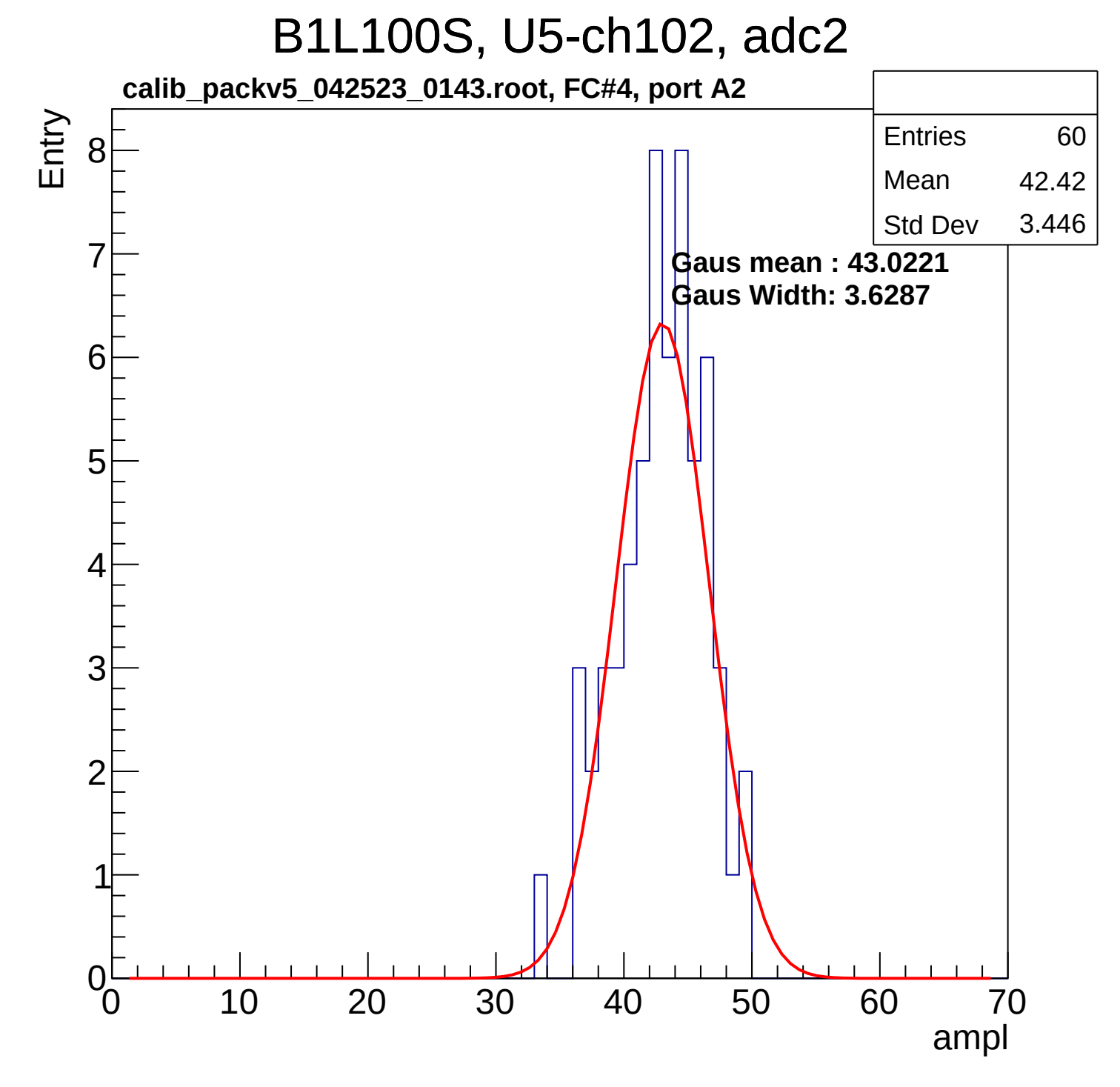
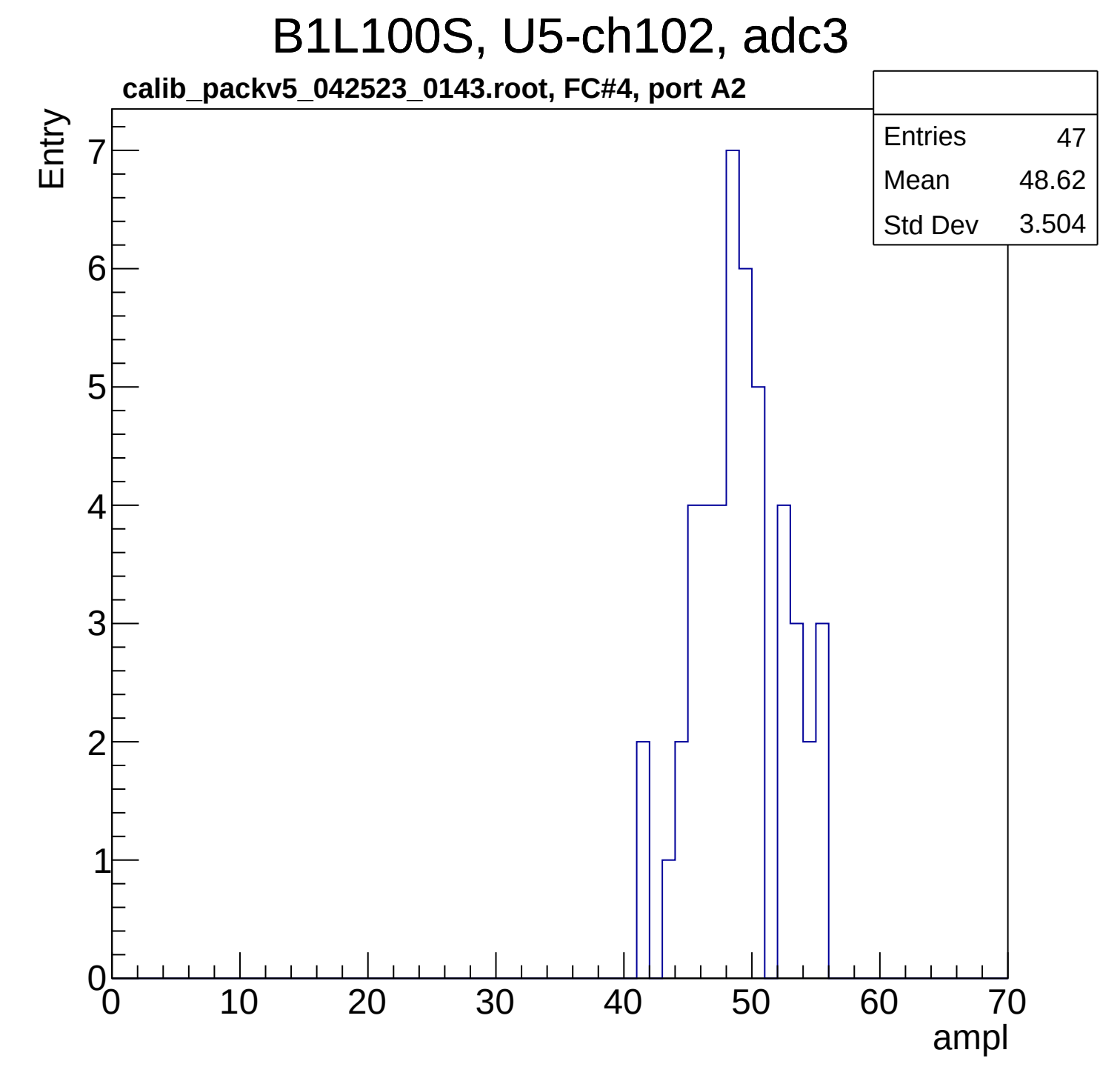
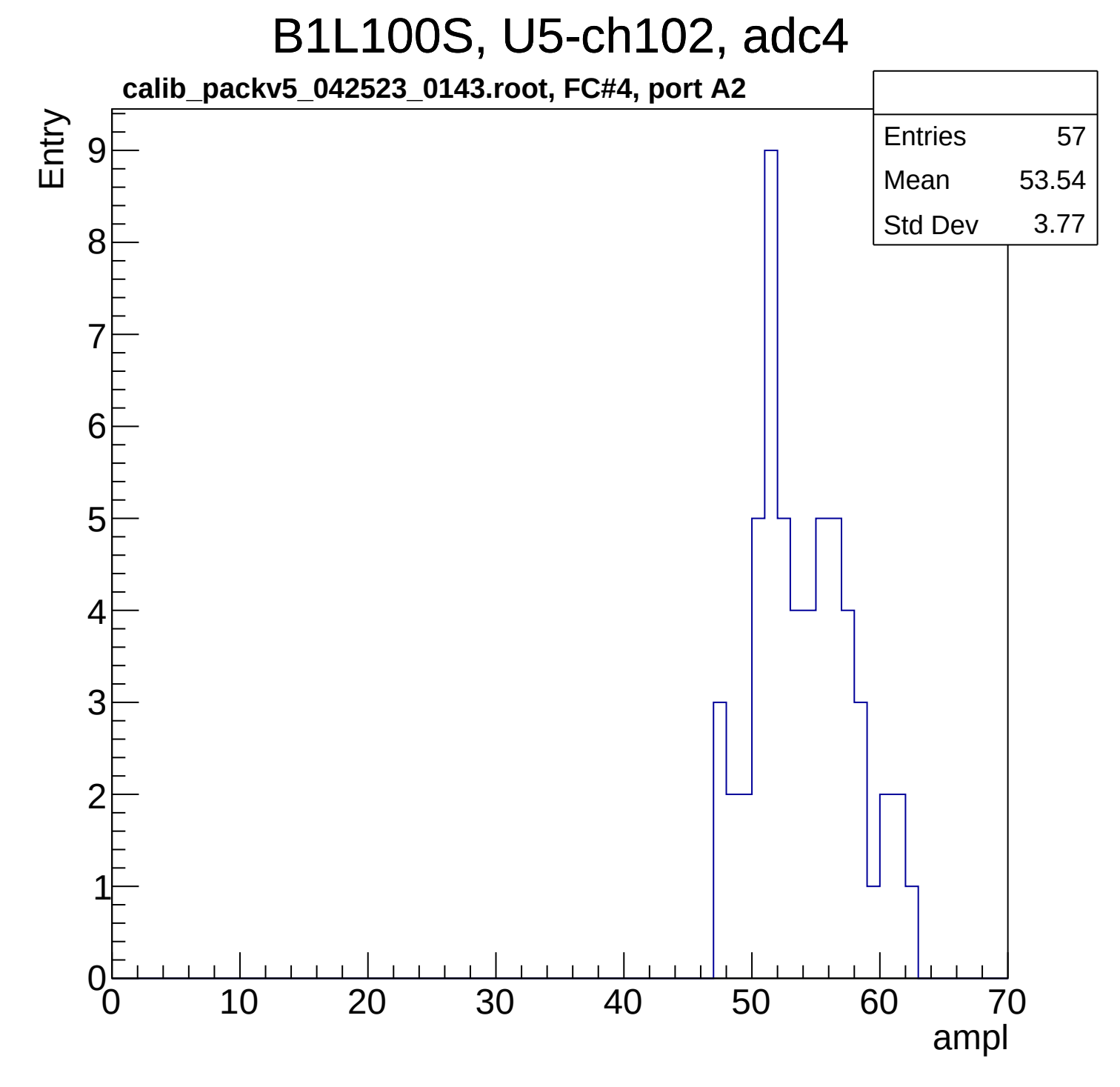

B1L100S, U5-ch102, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 42.42
Std Dev 3.446
Gaus mean : 43.0221
Gaus Width: 3.6287
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch102, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 47
Mean 48.62
Std Dev 3.504
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U5-ch102, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 53.54
Std Dev 3.77
Entry
ampl
0
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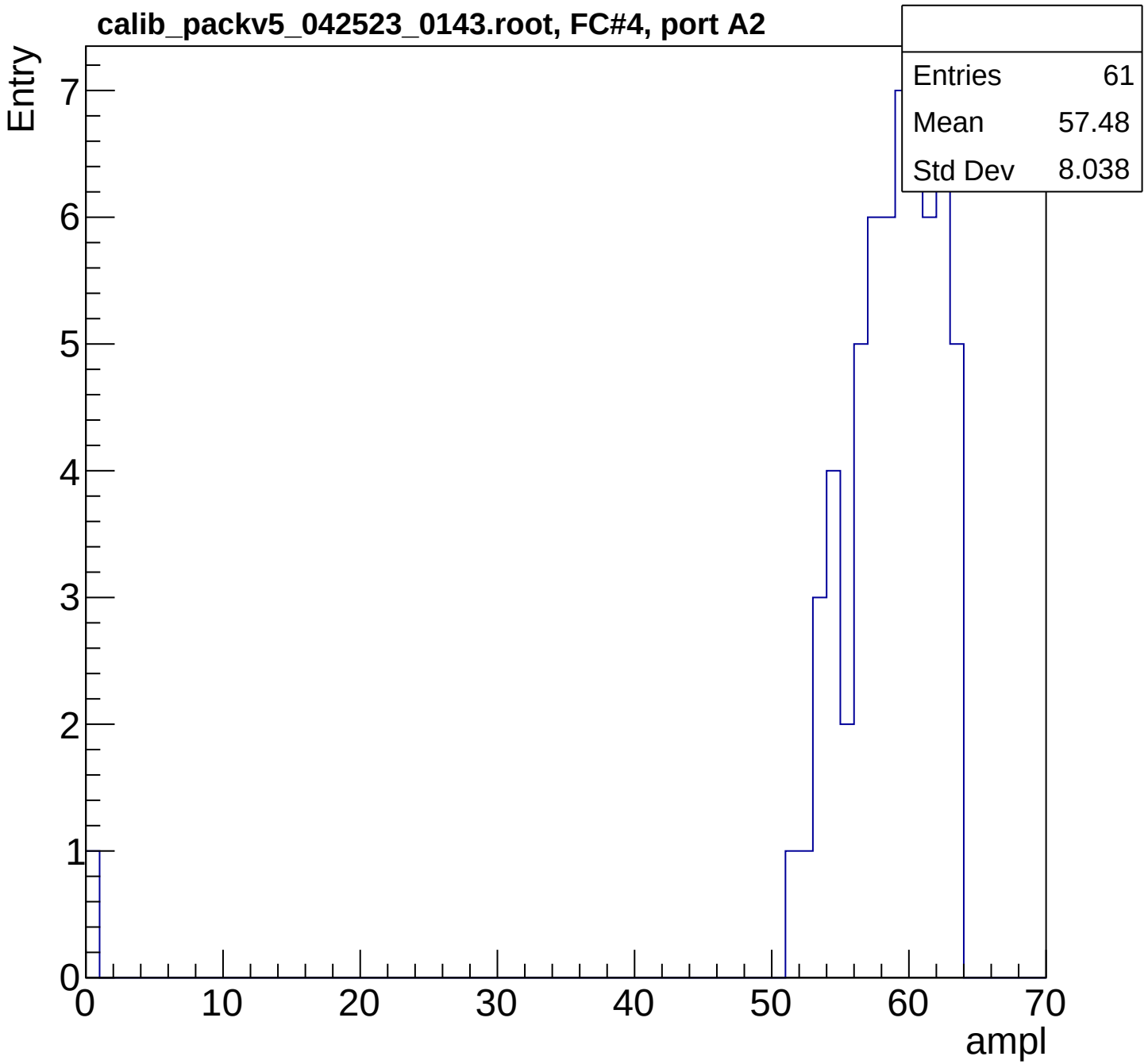
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch102, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 57.48
Std Dev 8.038
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
50
60
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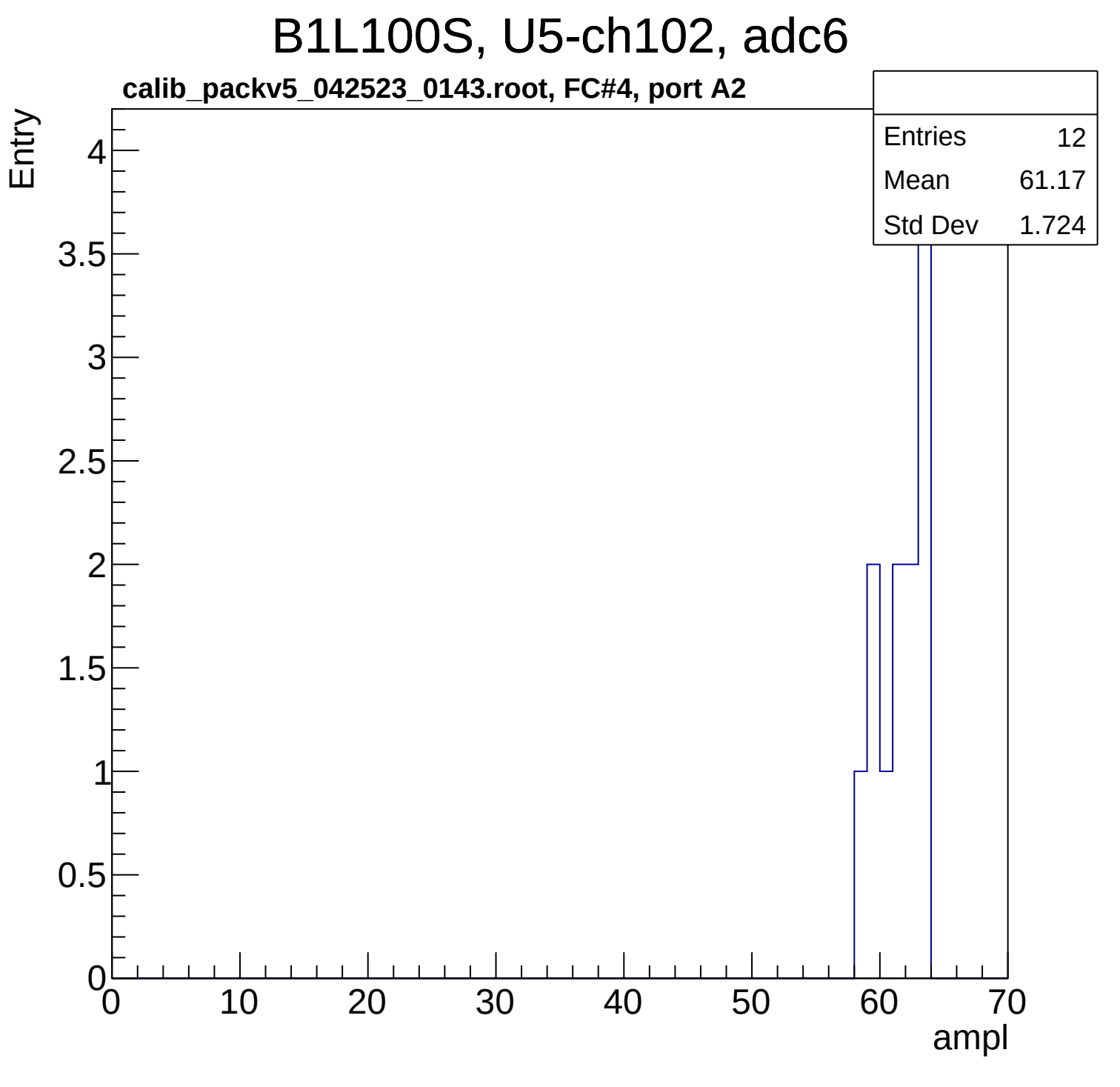
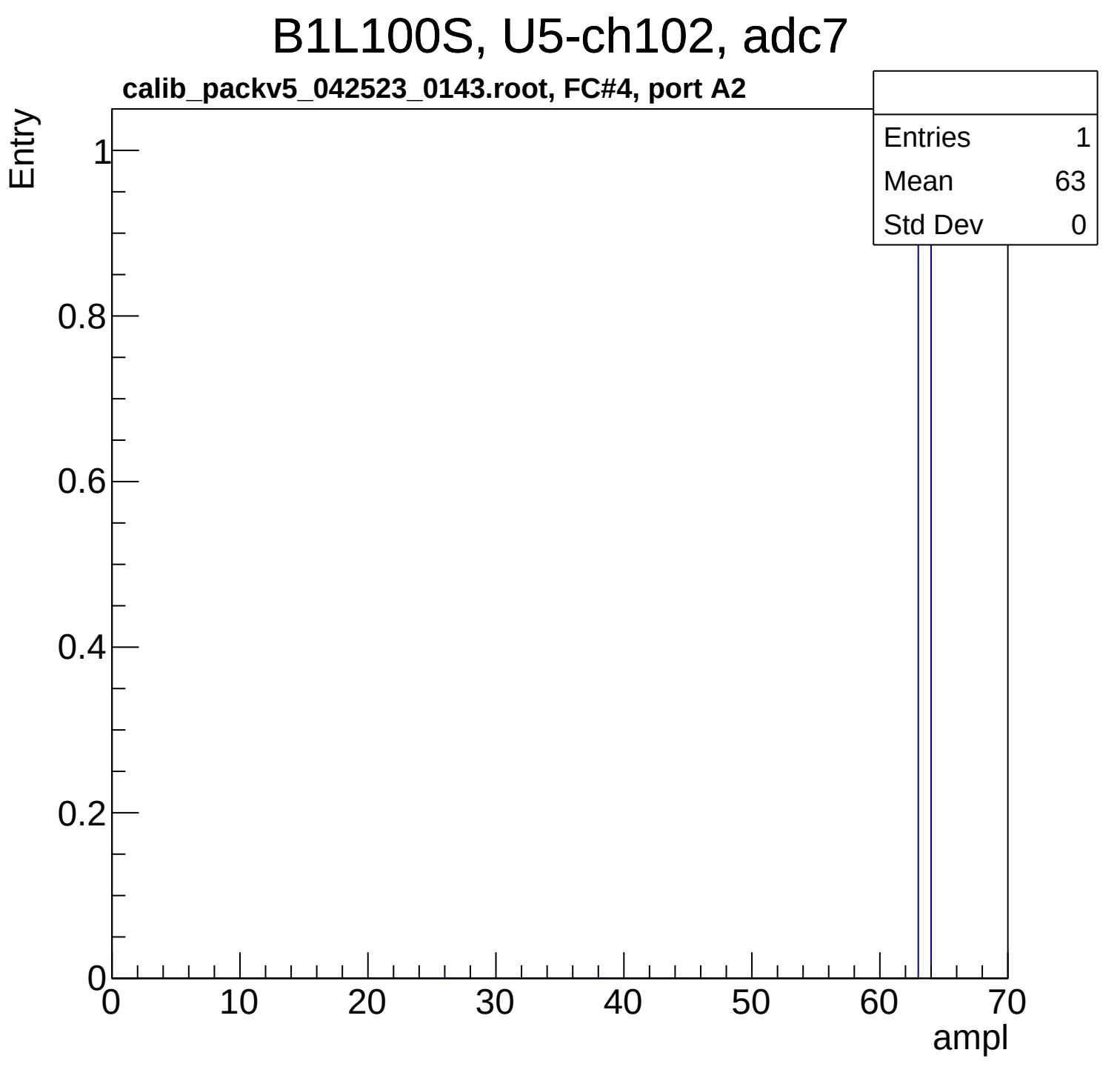
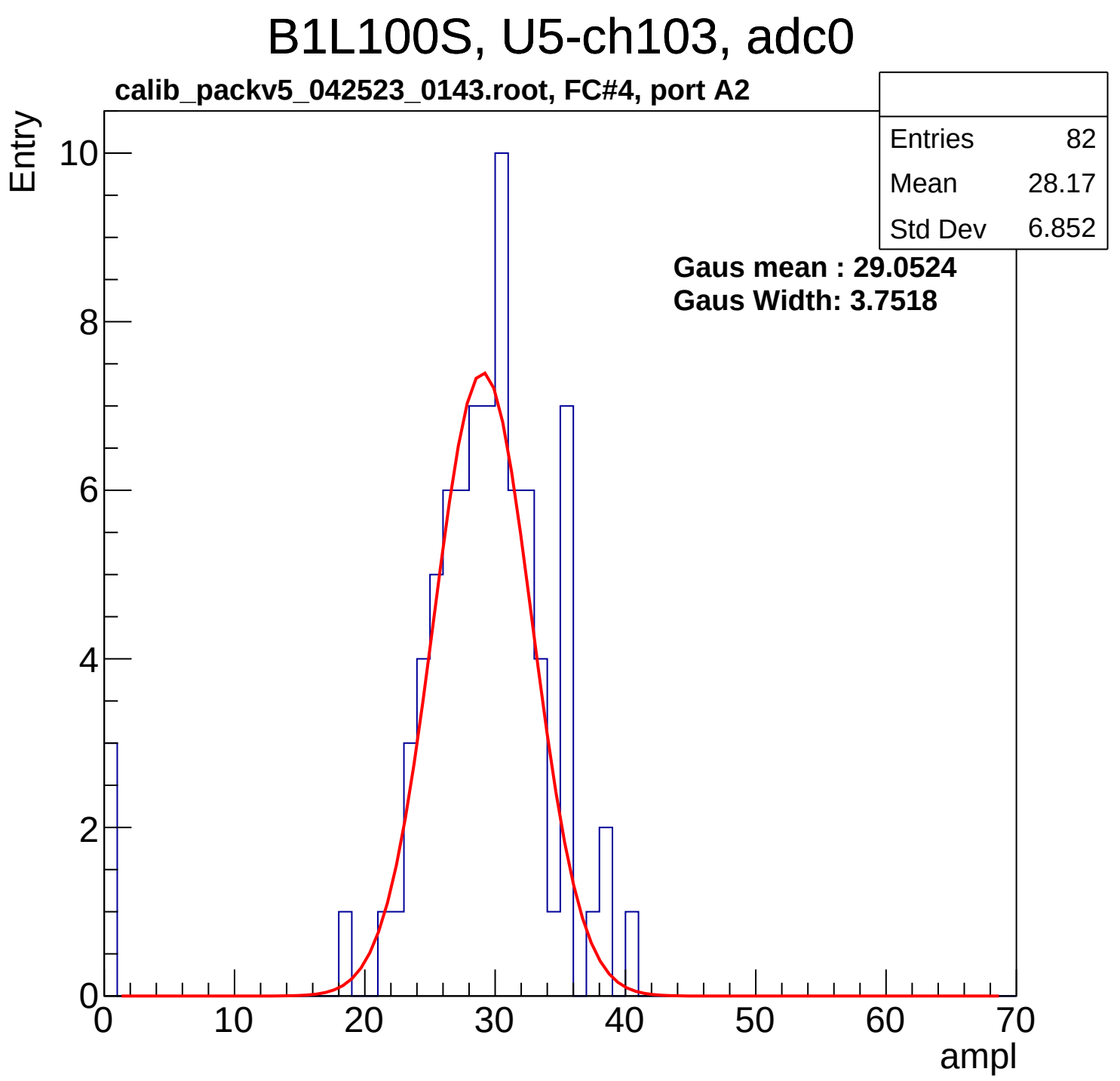

B1L100S, U5-ch102, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 12
Mean 61.17
Std Dev 1.724
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L100S, U5-ch102, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch103, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 82
Mean 28.17
Std Dev 6.852
Gaus mean : 29.0524
Gaus Width: 3.7518
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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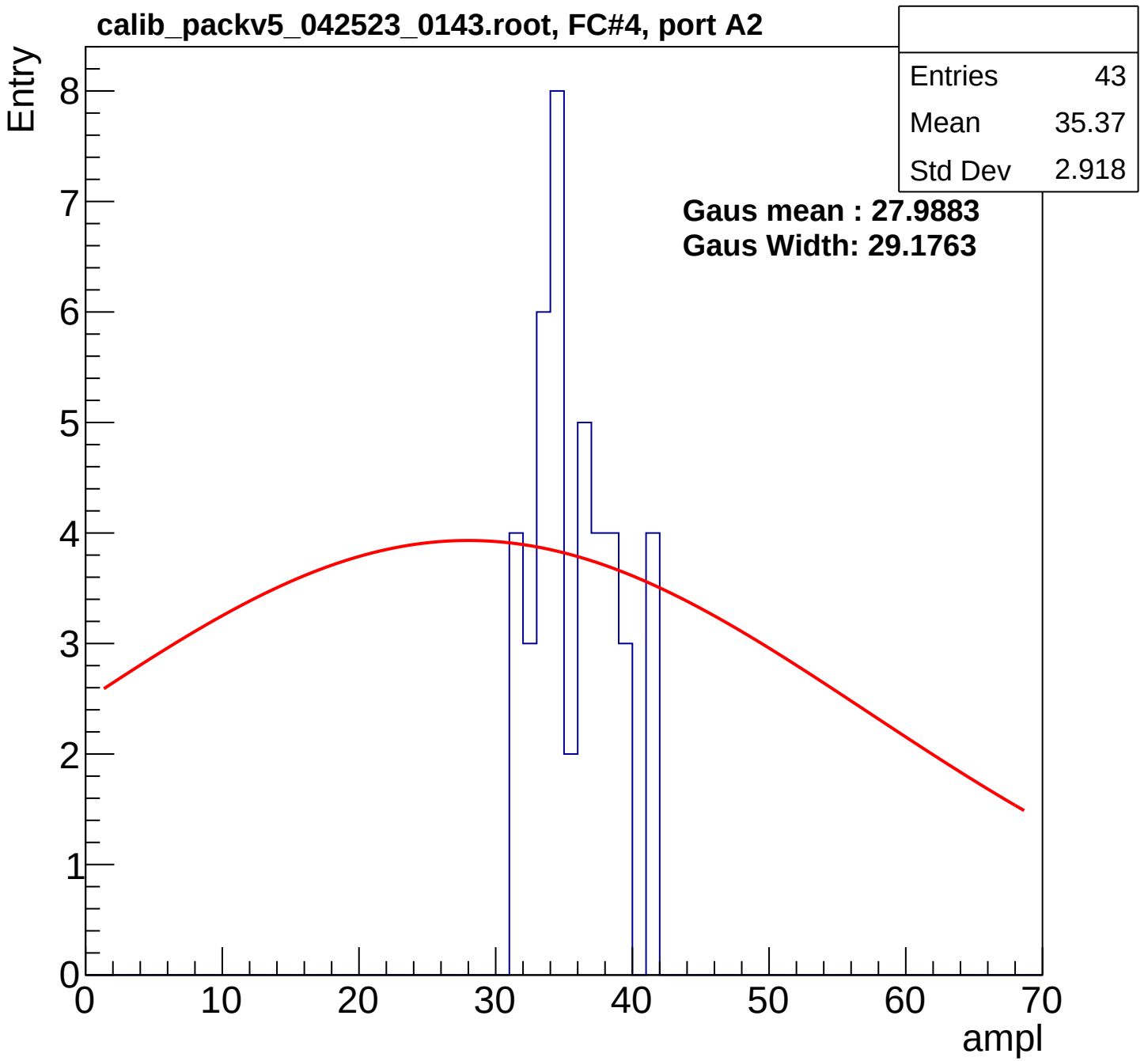
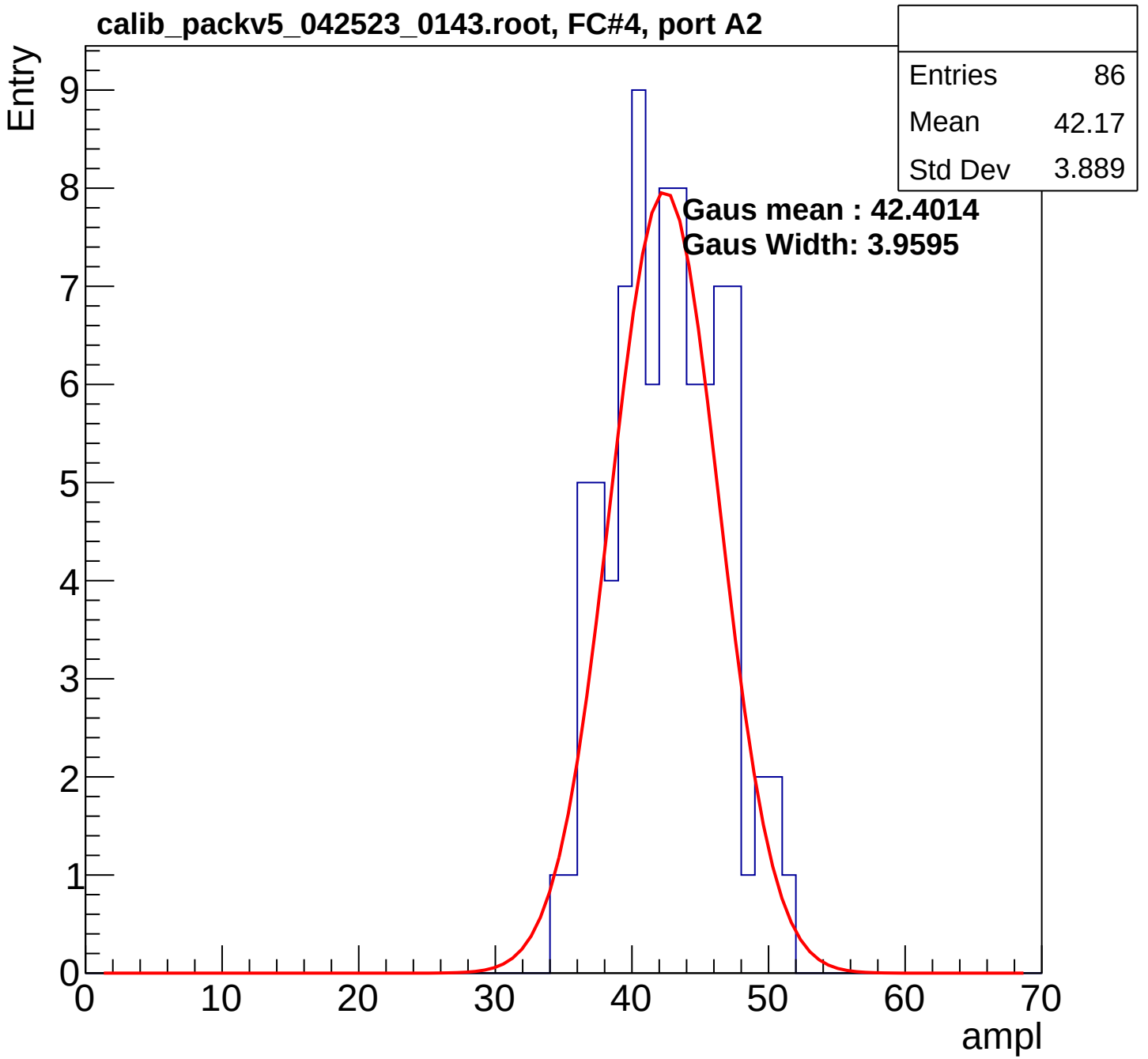

B1L100S, U5-ch103, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 43
Mean 35.37
Std Dev 2.918
Gaus mean : 27.9883
Gaus Width: 29.1763
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch103, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 86
Mean 42.17
Std Dev 3.889
Gaus mean : 42.4014
Gaus Width: 3.9595
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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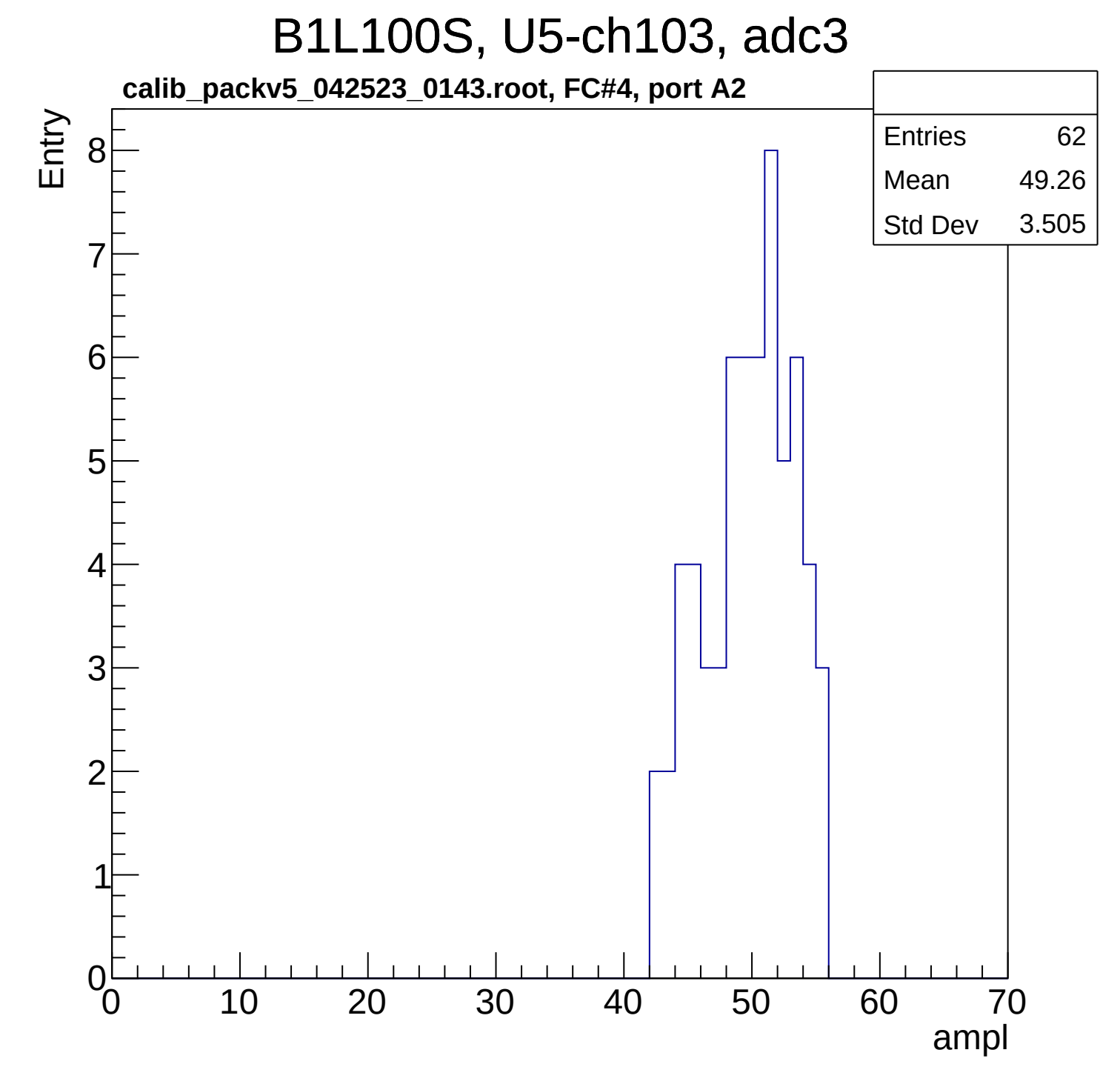
B1L100S, U5-ch103, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 49.26
Std Dev 3.505
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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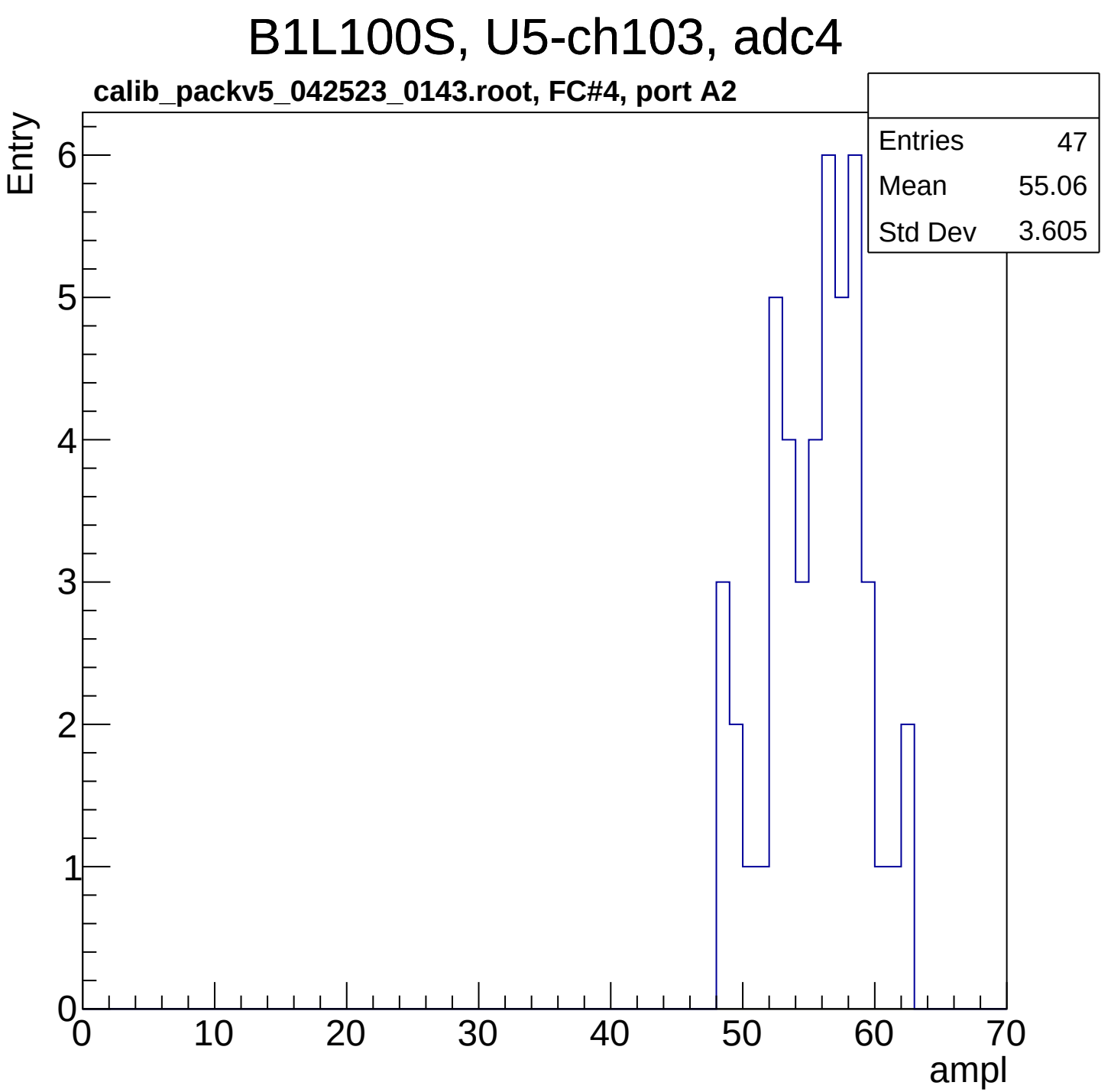
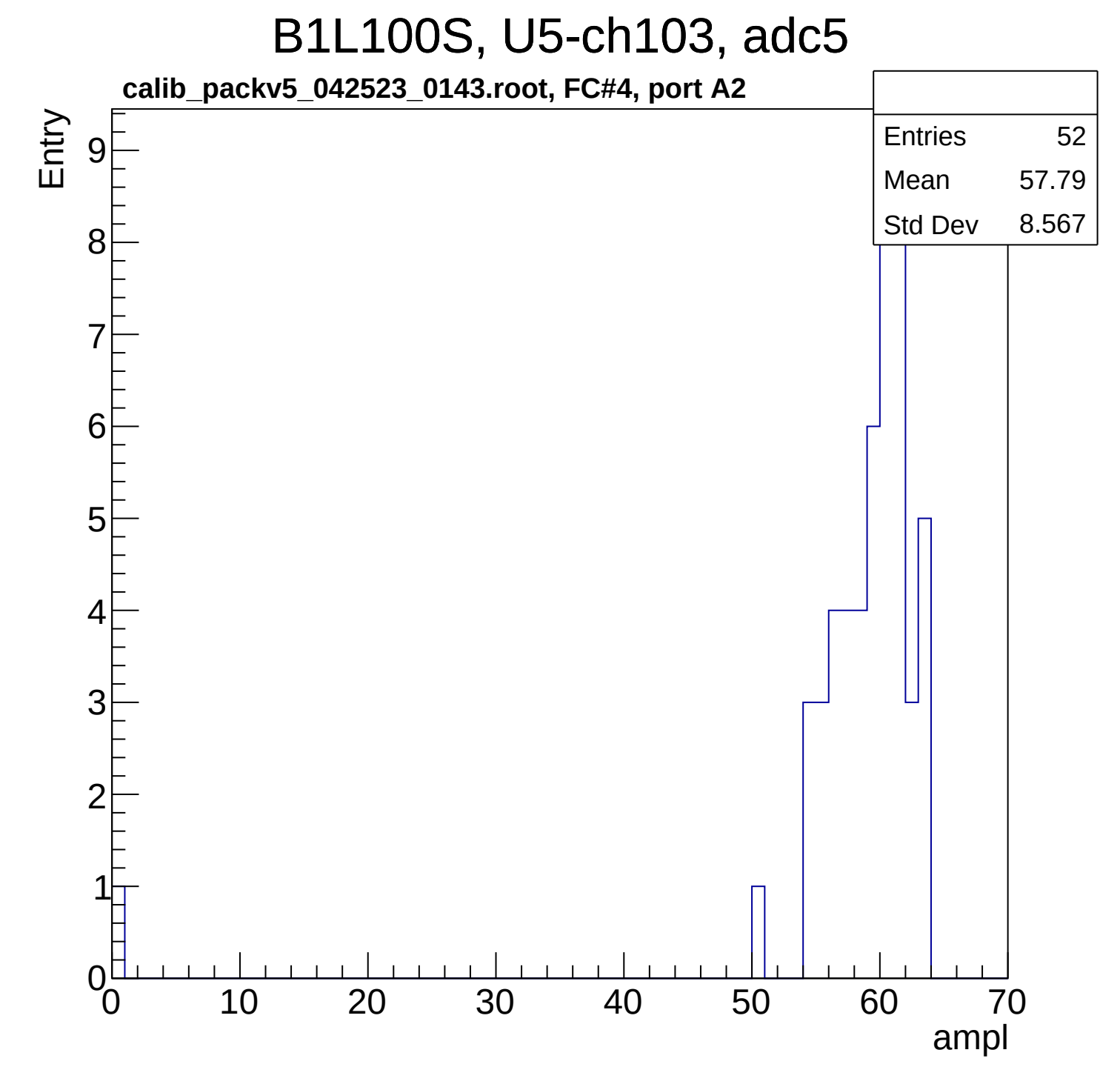

B1L100S, U5-ch103, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 47
Mean 55.06
Std Dev 3.605
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch103, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 52
Mean 57.79
Std Dev 8.567
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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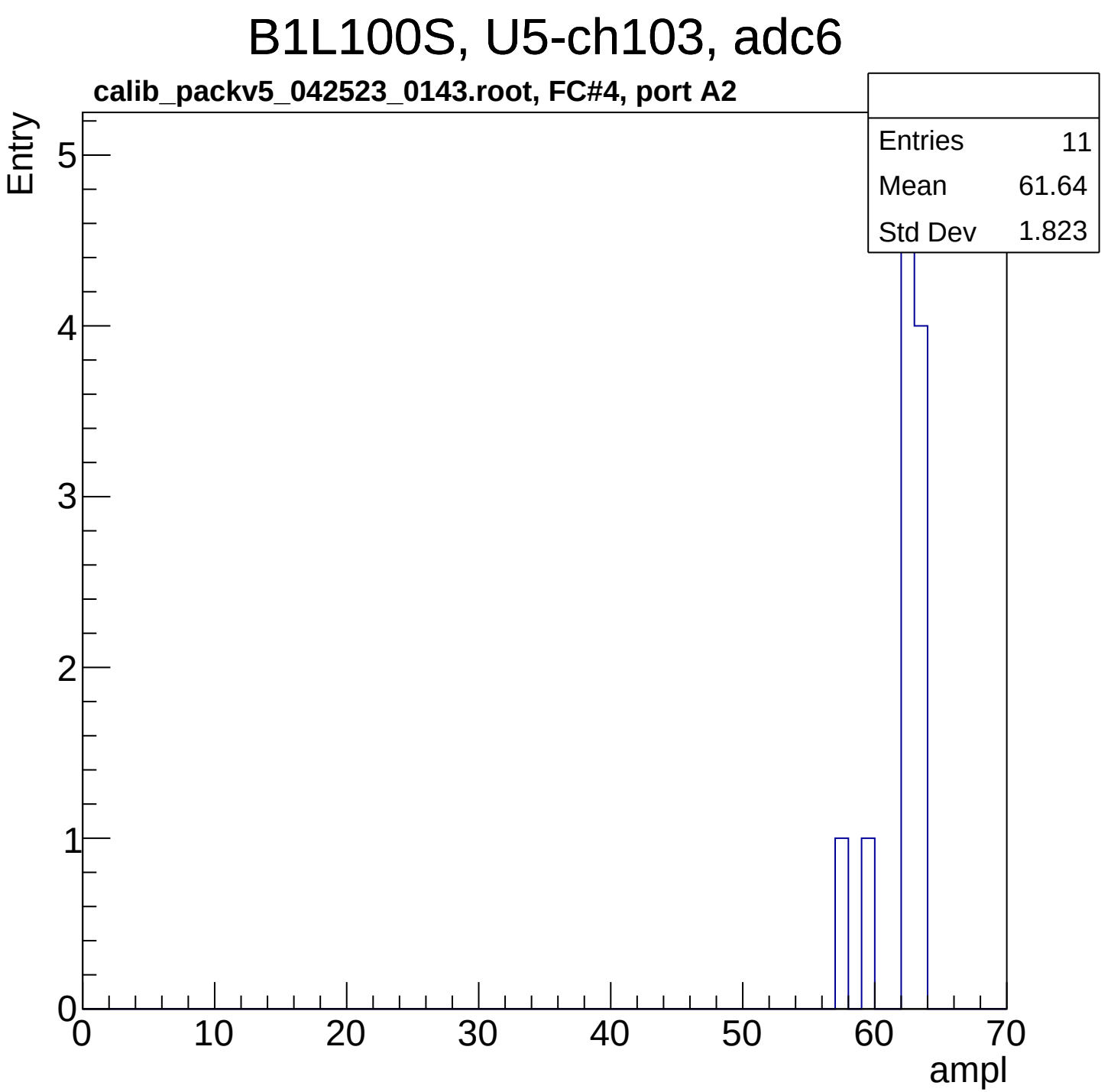
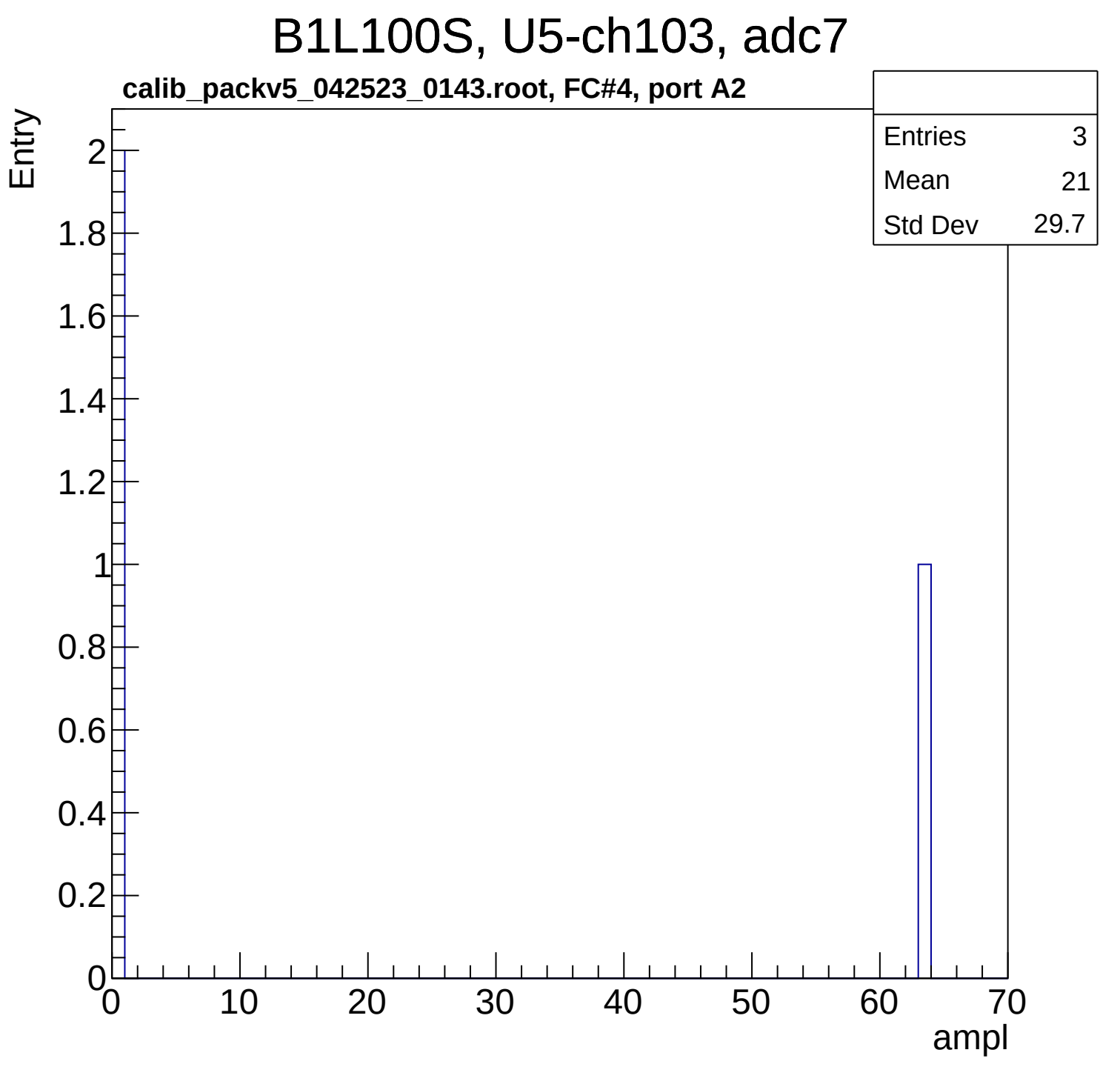
40
50
60
70


B1L100S, U5-ch103, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 11
Mean 61.64
Std Dev 1.823
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch103, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 21
Std Dev 29.7
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
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0
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20
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40
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60
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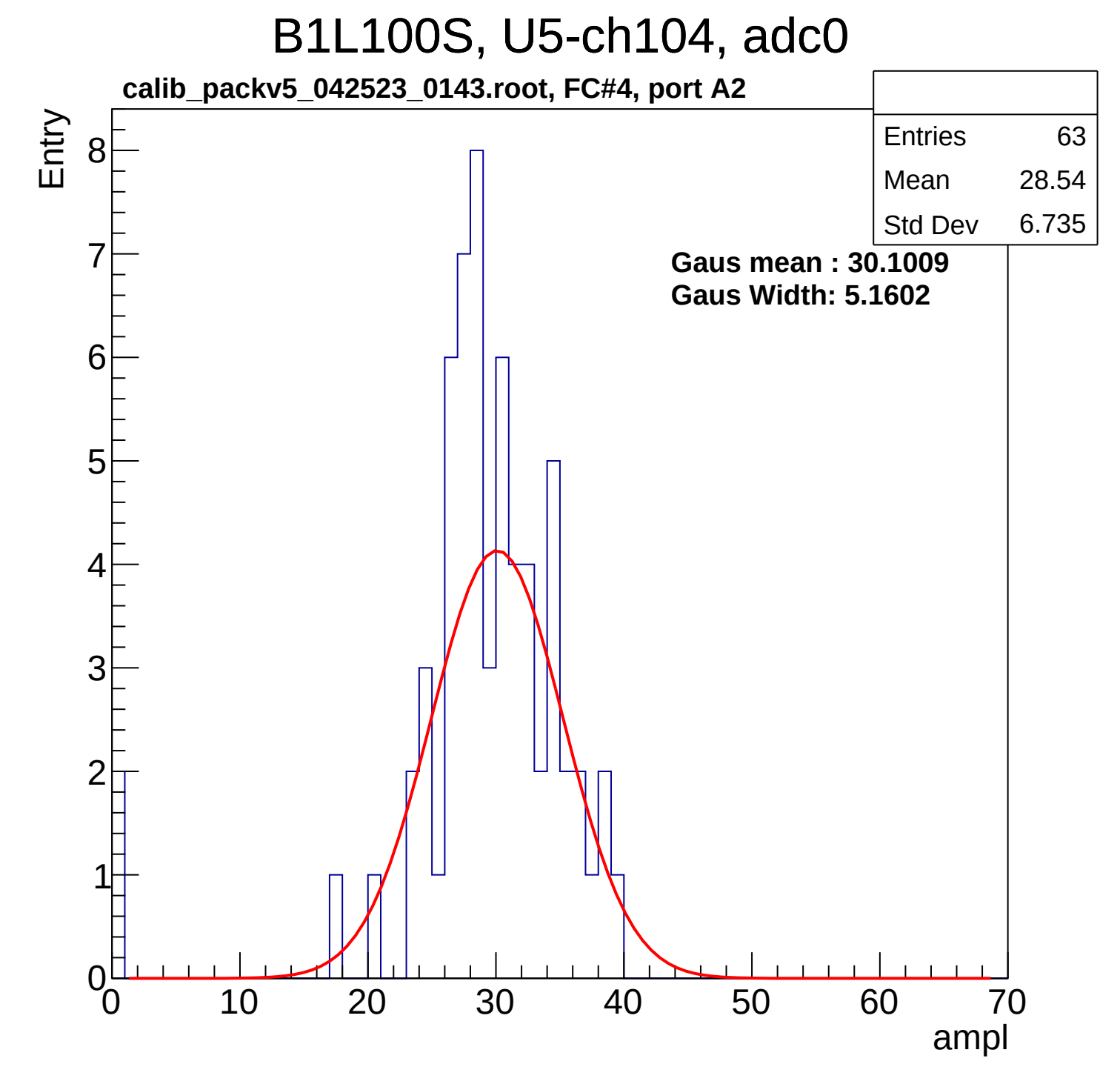
B1L100S, U5-ch104, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 28.54
Std Dev 6.735
Gaus mean : 30.1009
Gaus Width: 5.1602
Entry
ampl
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1
2
3
4
5
6
7
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0
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20
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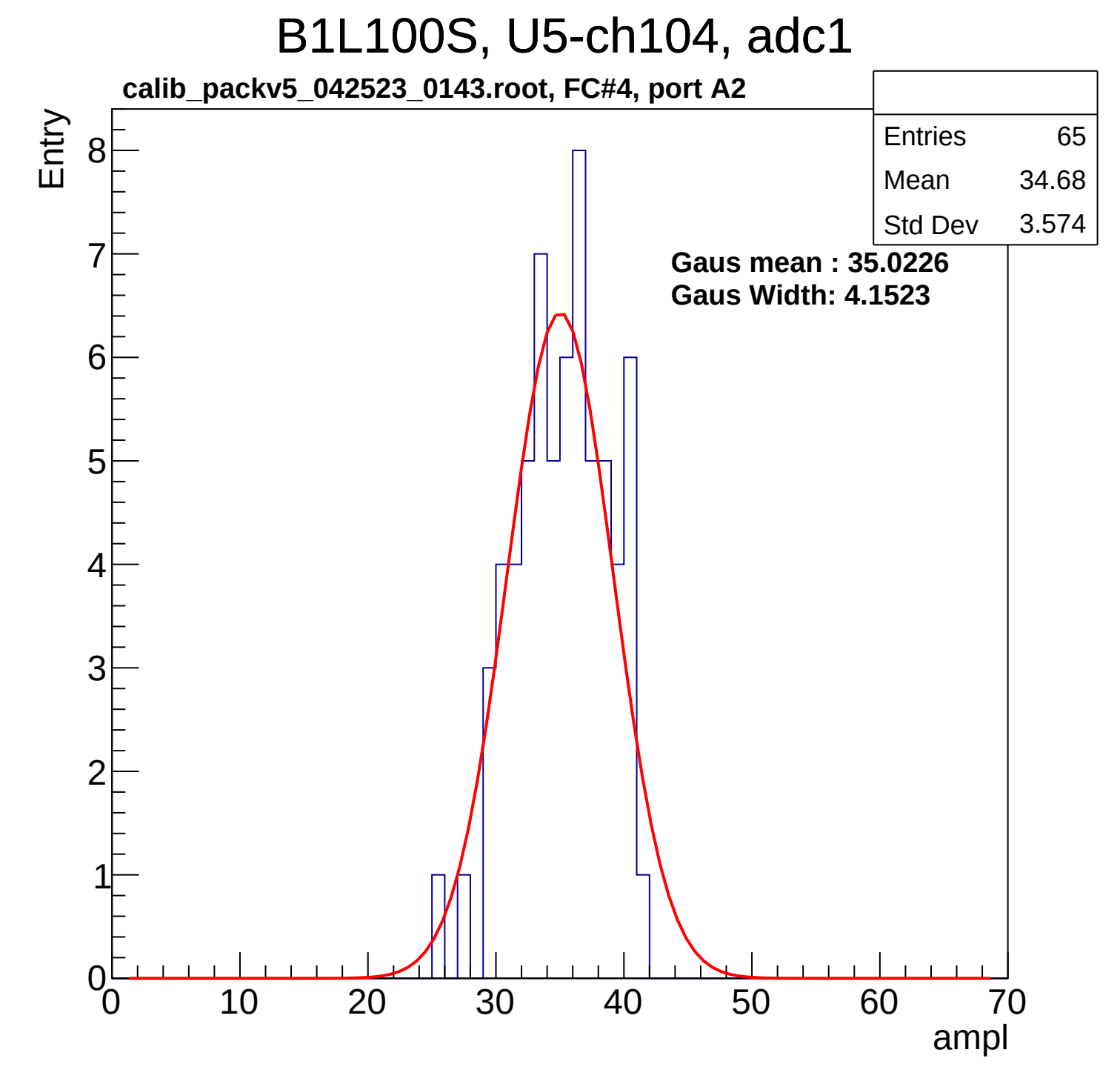
40
50
60
70


B1L100S, U5-ch104, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 34.68
Std Dev 3.574
Gaus mean : 35.0226
Gaus Width: 4.1523
Entry
ampl
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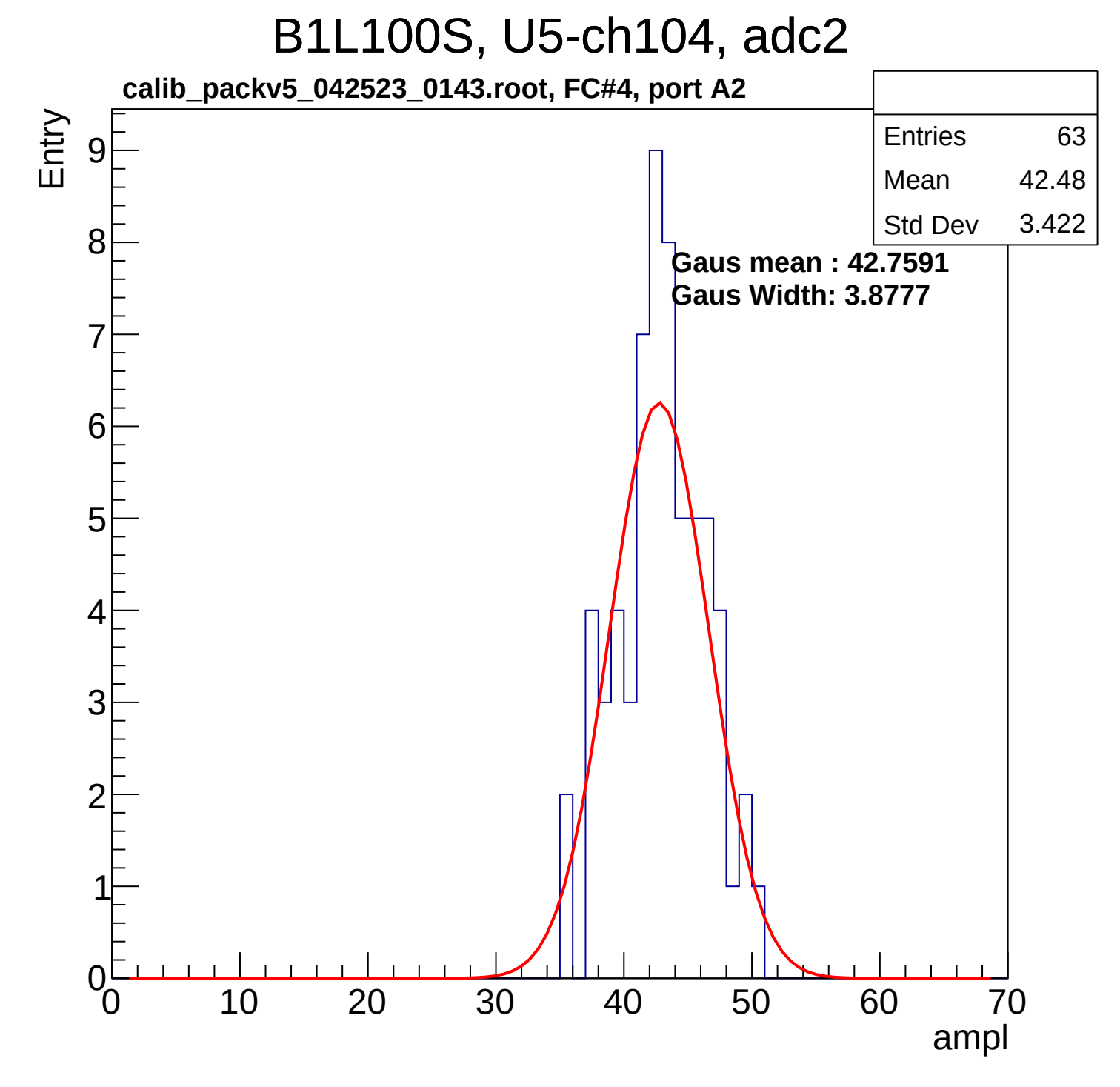
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch104, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 42.48
Std Dev 3.422
Gaus mean : 42.7591
Gaus Width: 3.8777
Entry
ampl
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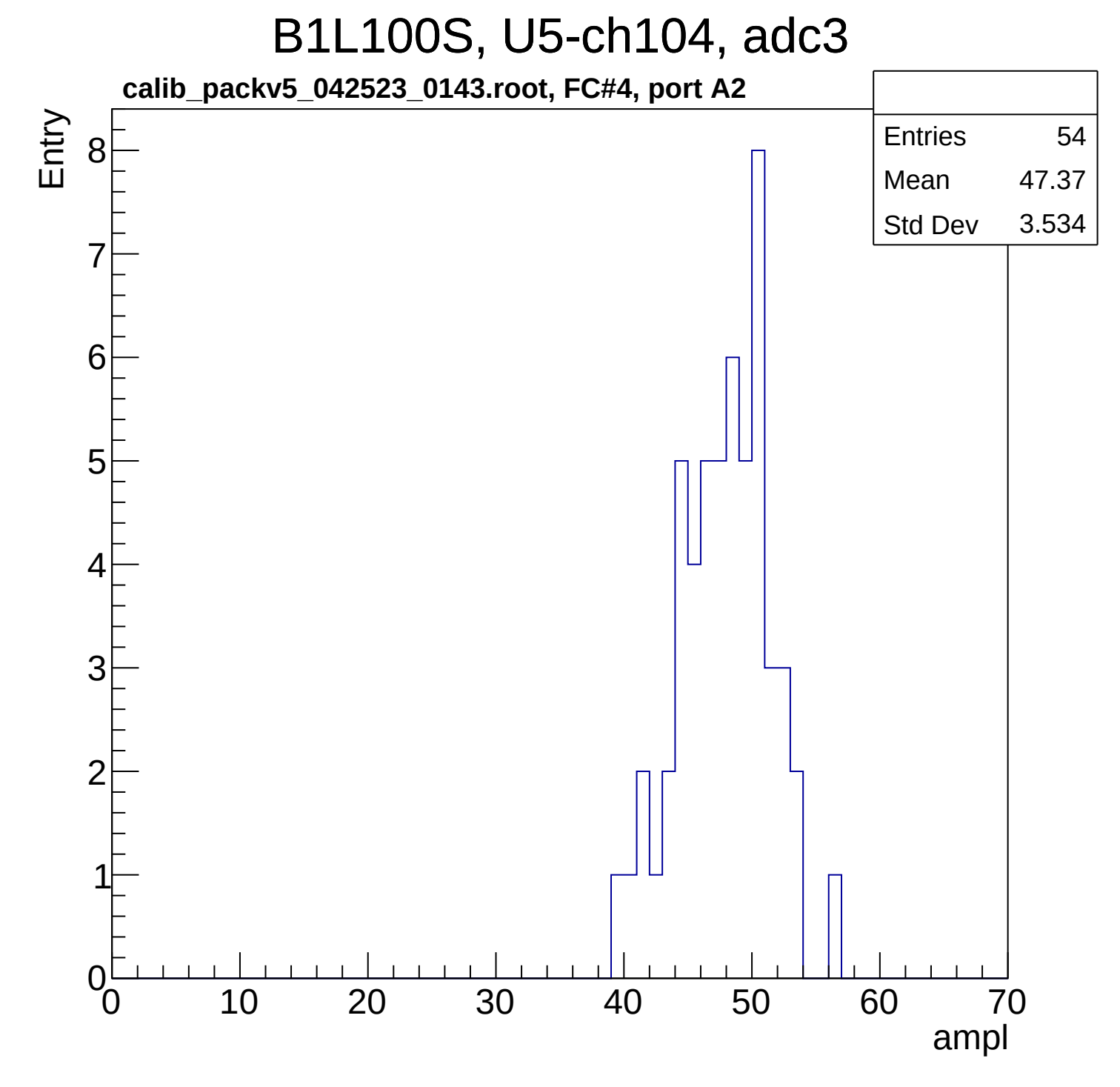
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch104, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 47.37
Std Dev 3.534
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
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60
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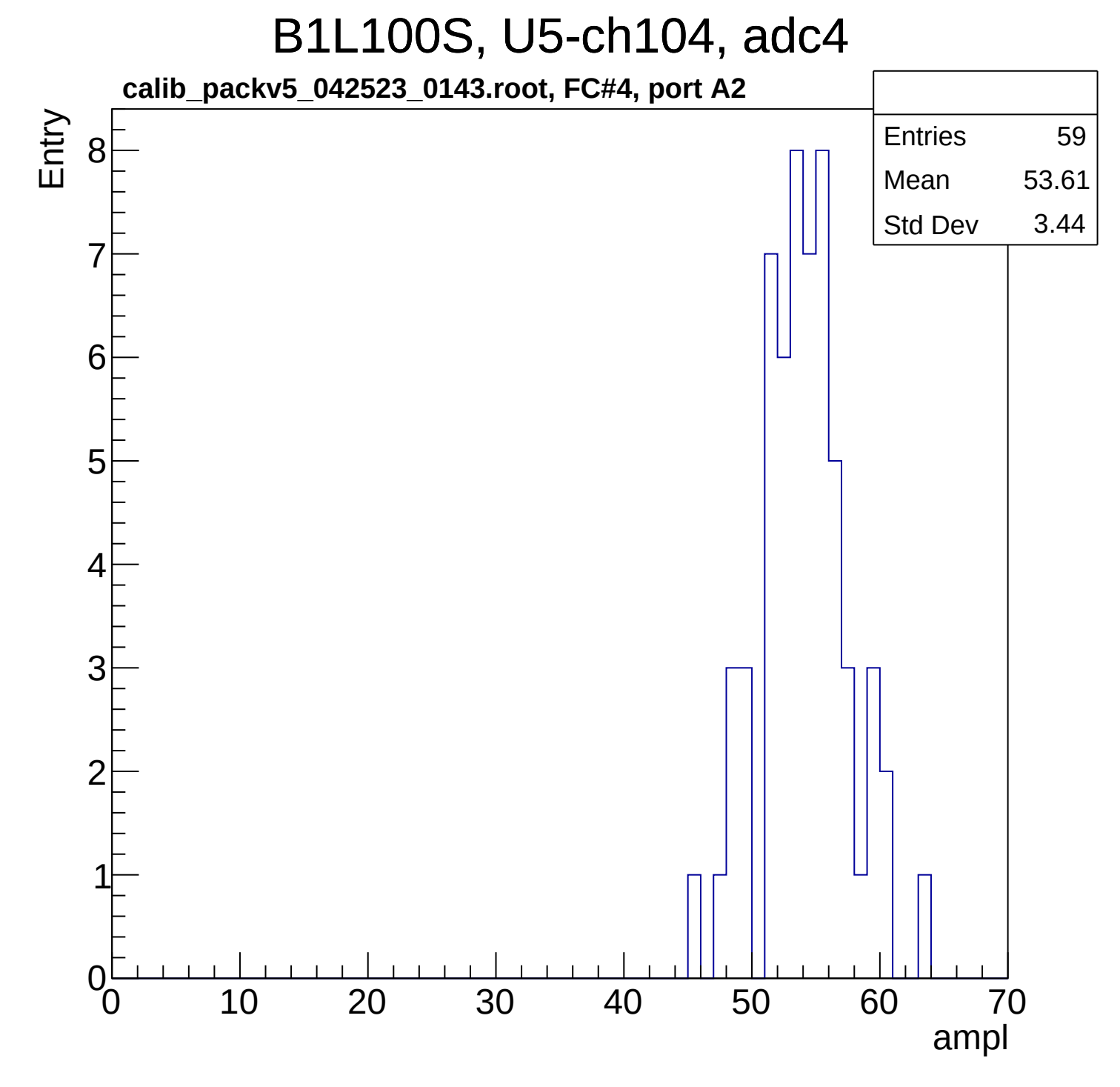
B1L100S, U5-ch104, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 53.61
Std Dev 3.44
Entry
ampl
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2
3
4
5
6
7
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0
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40
50
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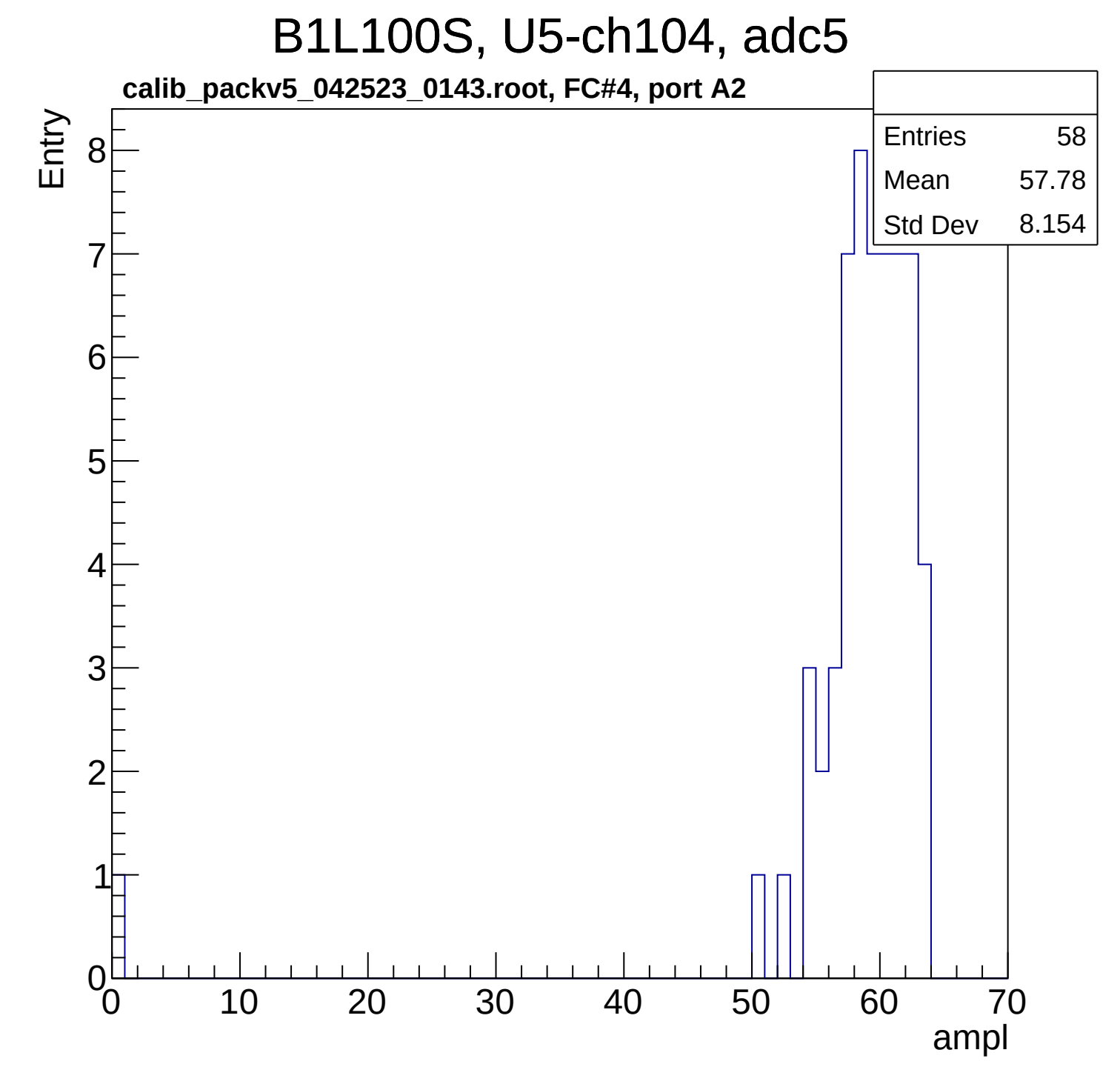
B1L100S, U5-ch104, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 57.78
Std Dev 8.154
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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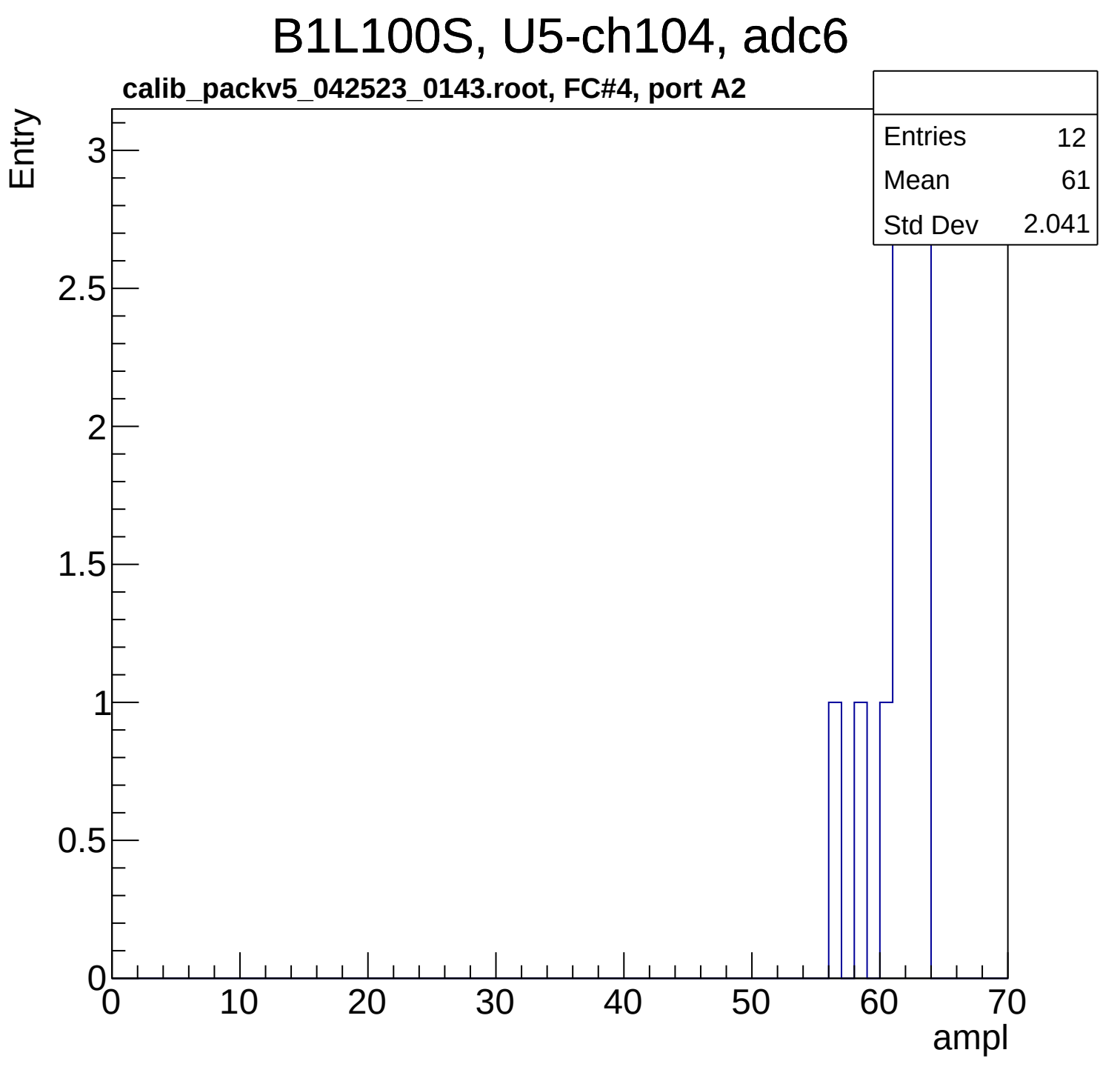
40
50
60
70


B1L100S, U5-ch104, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 12
Mean 61
Std Dev 2.041
Entry
ampl
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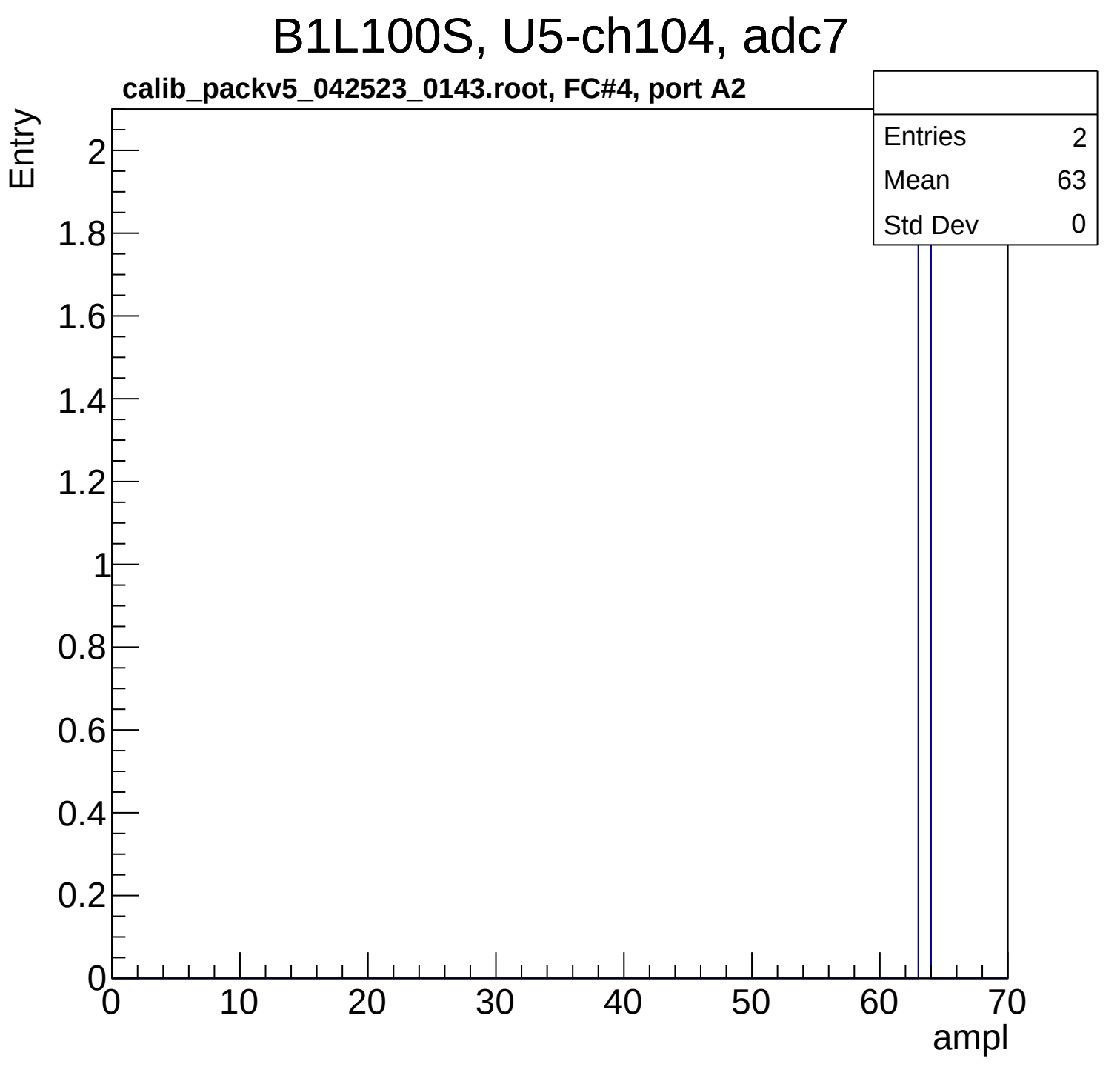
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L100S, U5-ch104, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 63
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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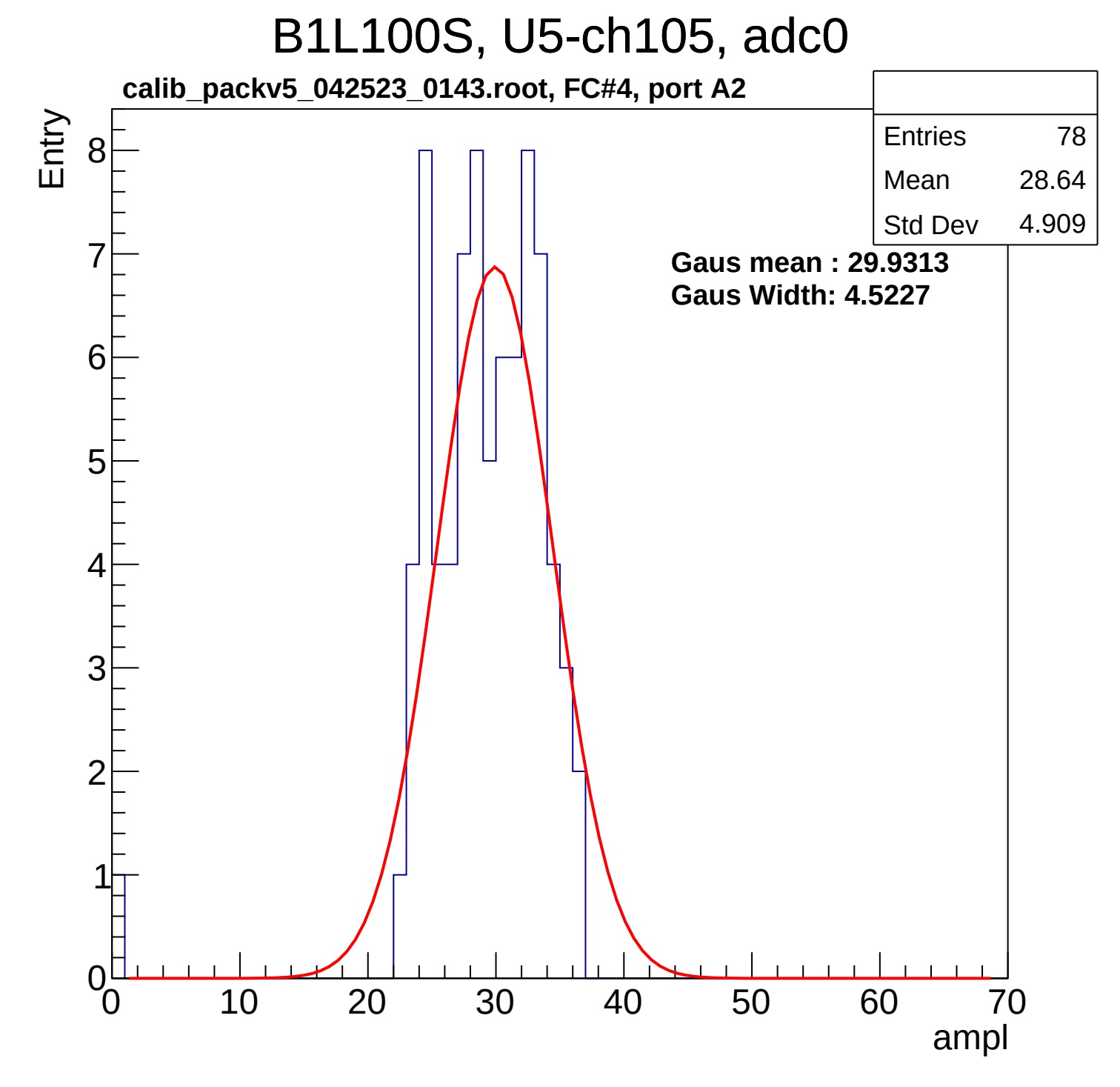
B1L100S, U5-ch105, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 78
Mean 28.64
Std Dev 4.909
Gaus mean : 29.9313
Gaus Width: 4.5227
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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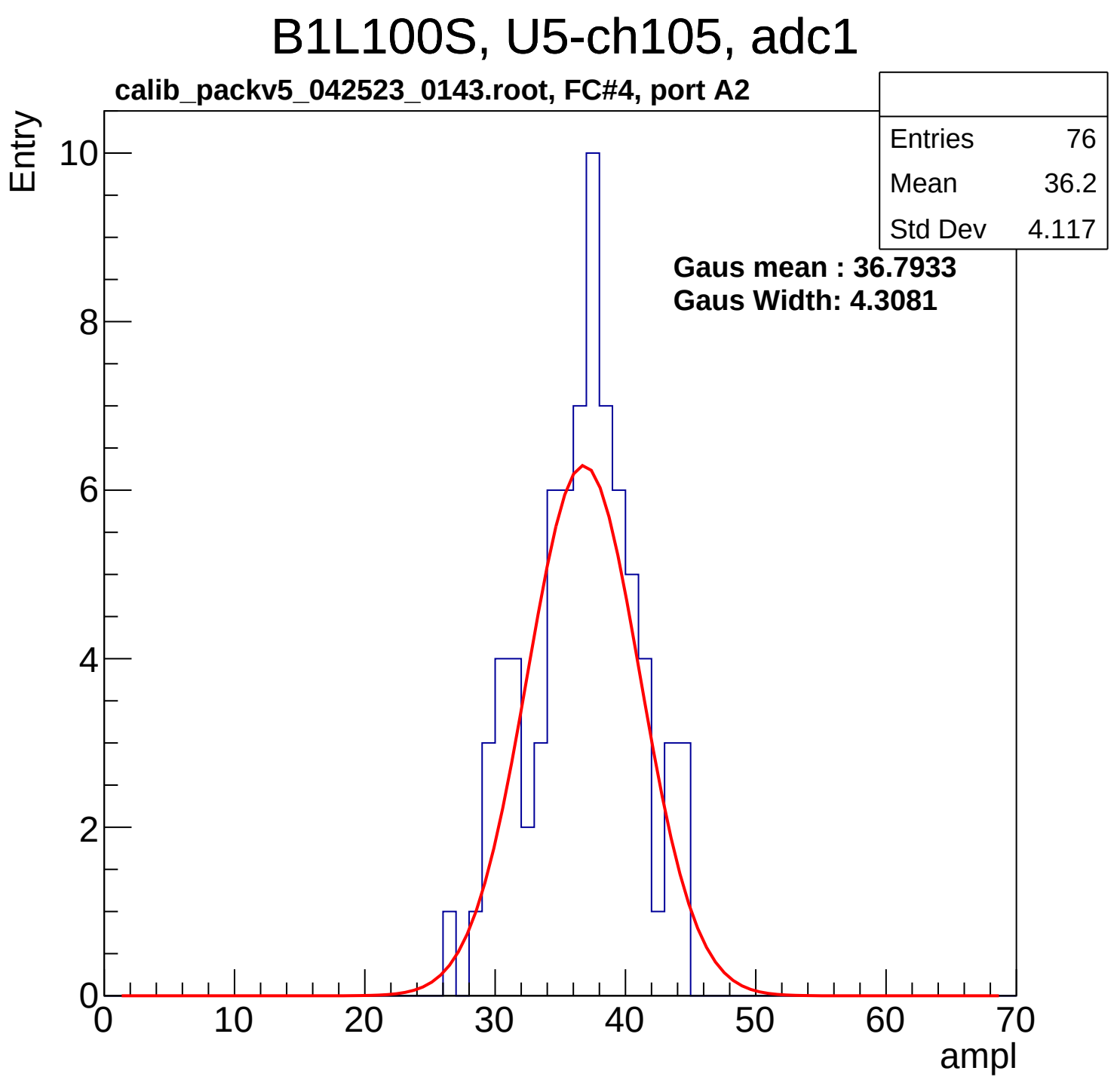
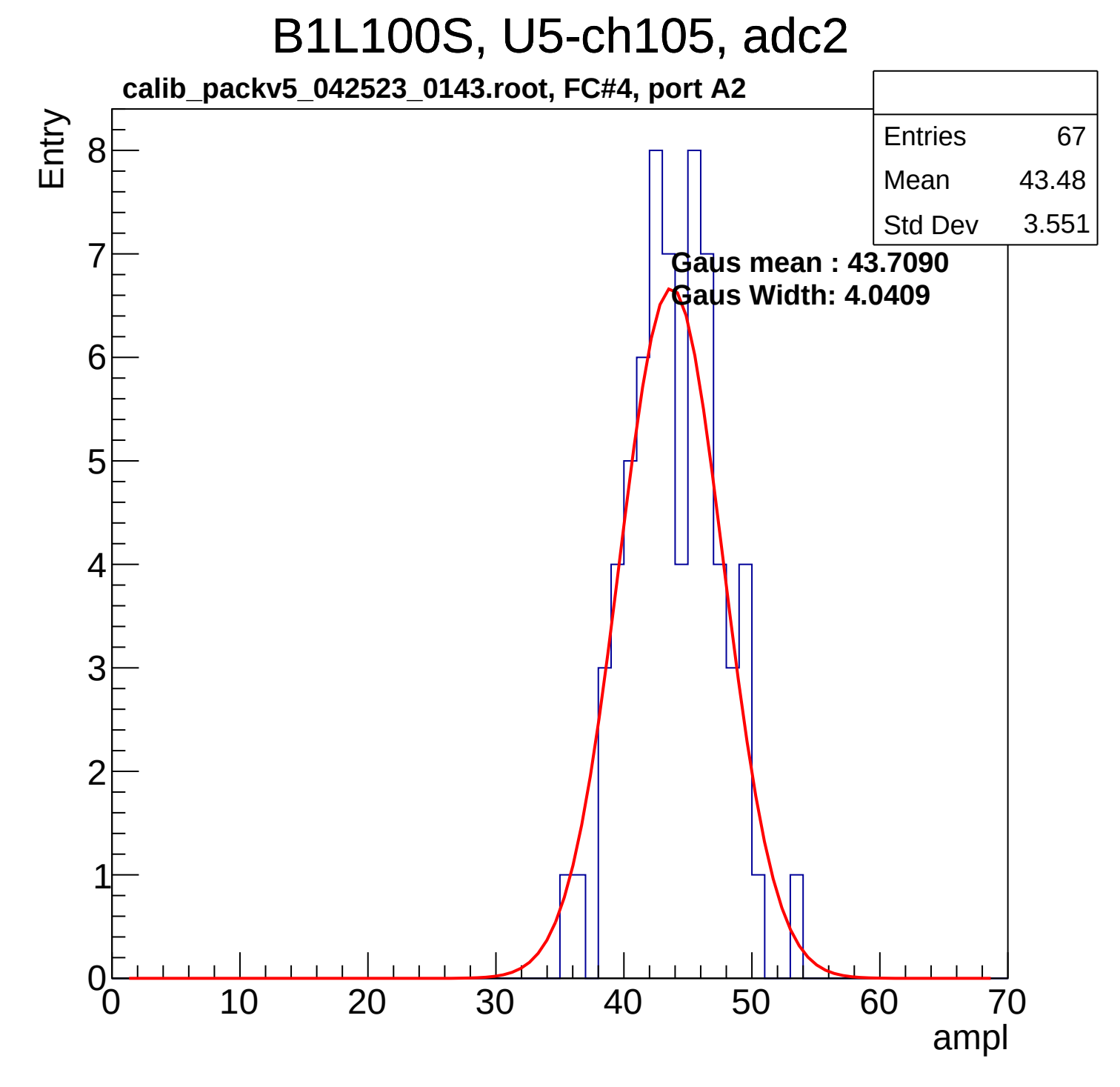
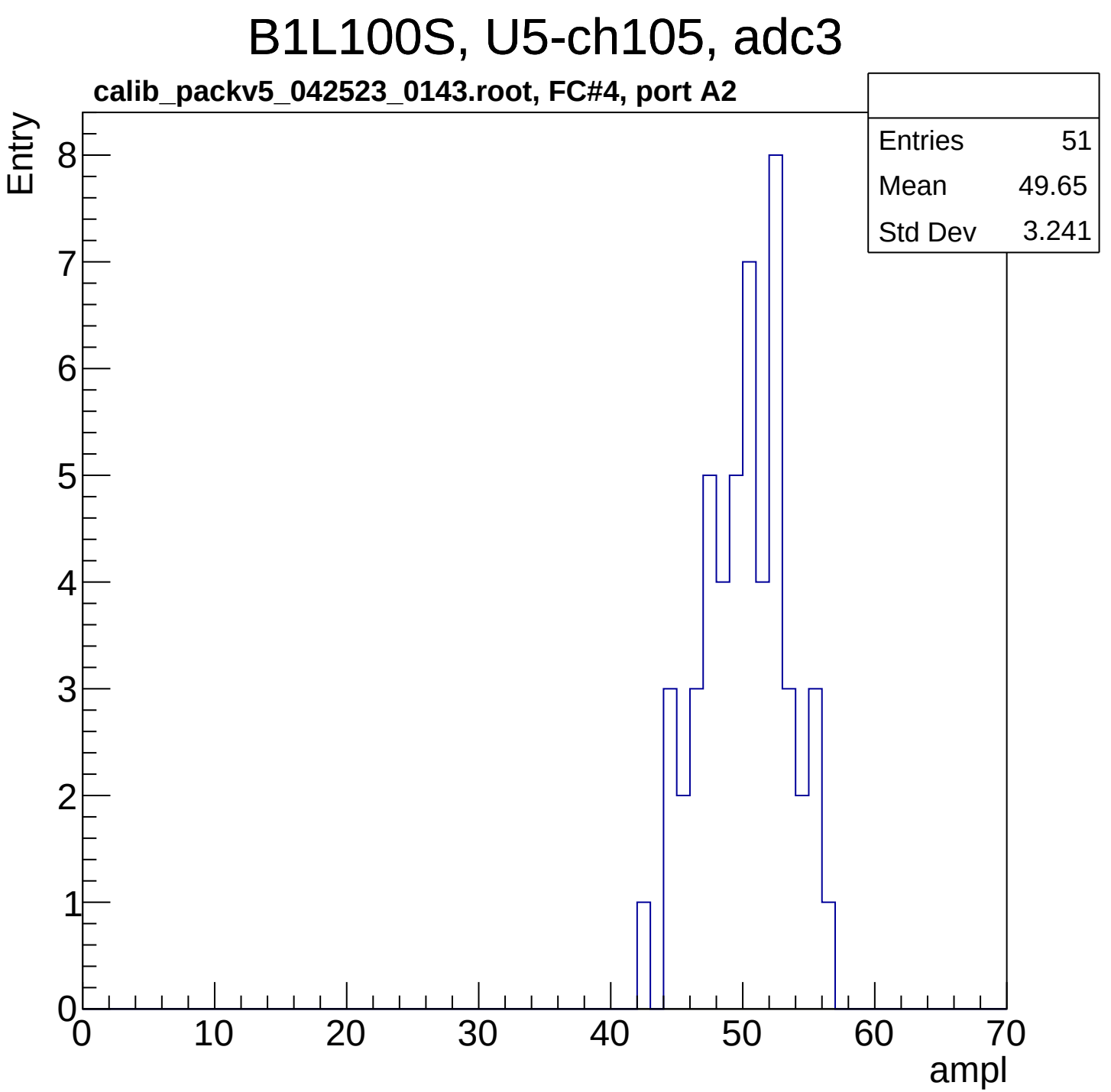

B1L100S, U5-ch105, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 76
Mean 36.2
Std Dev 4.117
Gaus mean : 36.7933
Gaus Width: 4.3081
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch105, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 43.48
Std Dev 3.551
Gaus mean : 43.7090
Gaus Width: 4.0409
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch105, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 49.65
Std Dev 3.241
Entry
ampl
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1
2
3
4
5
6
7
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0
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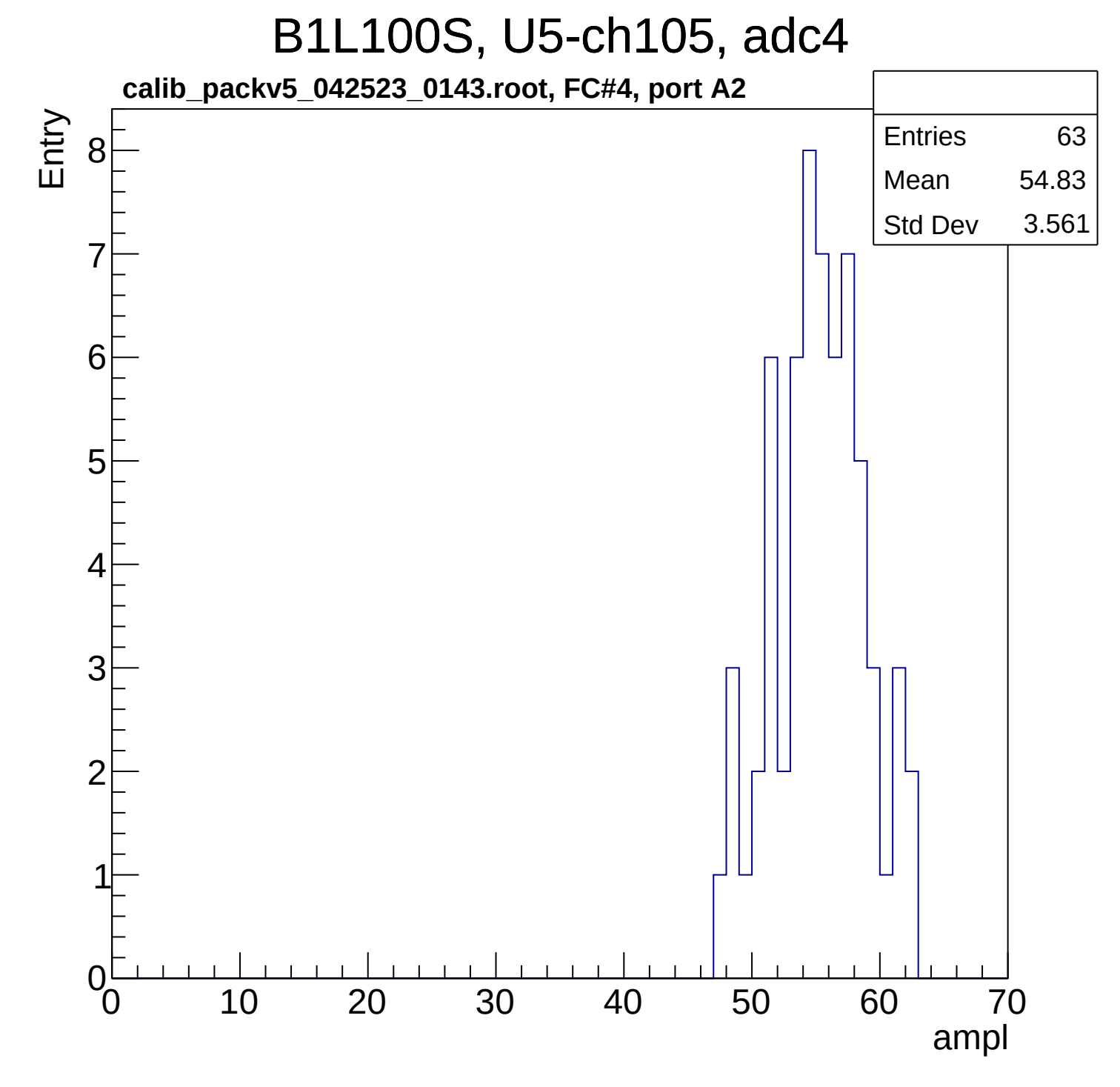
B1L100S, U5-ch105, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 54.83
Std Dev 3.561
Entry
ampl
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1
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5
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0
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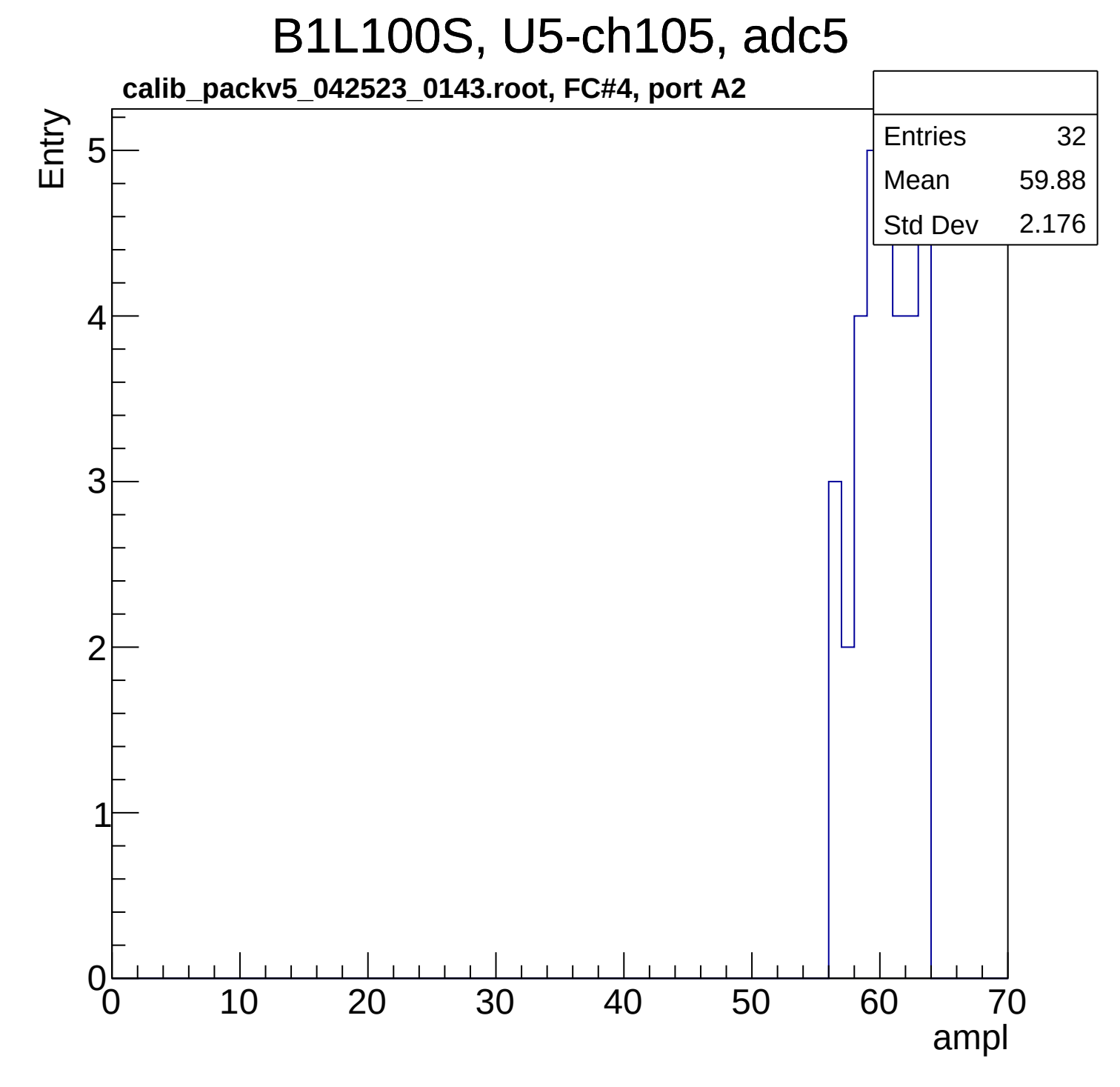
B1L100S, U5-ch105, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 32
Mean 59.88
Std Dev 2.176
Entry
ampl
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2
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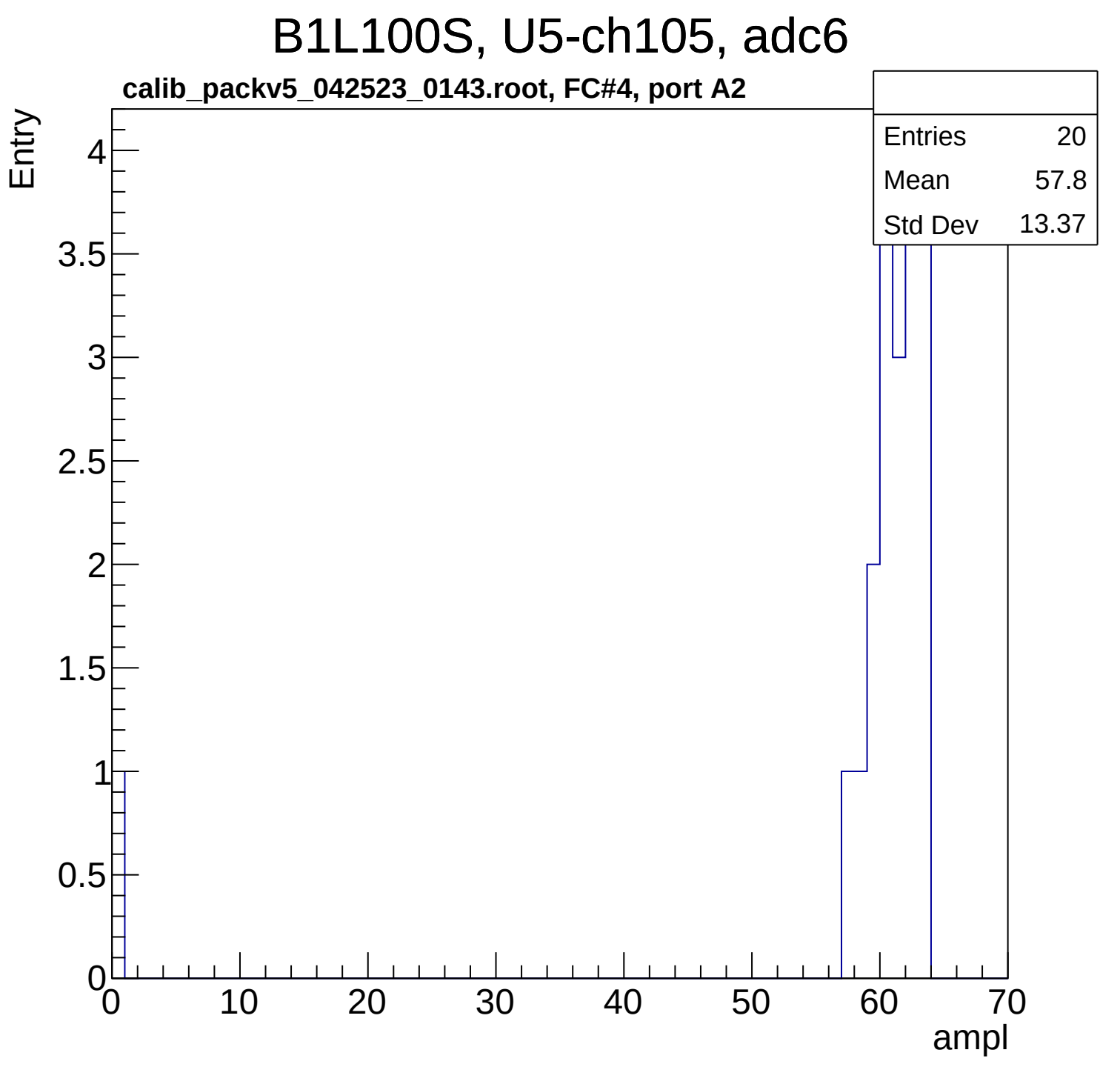
B1L100S, U5-ch105, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 20
Mean 57.8
Std Dev 13.37
Entry
ampl
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0.5
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1.5
2
2.5
3
3.5
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0
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60
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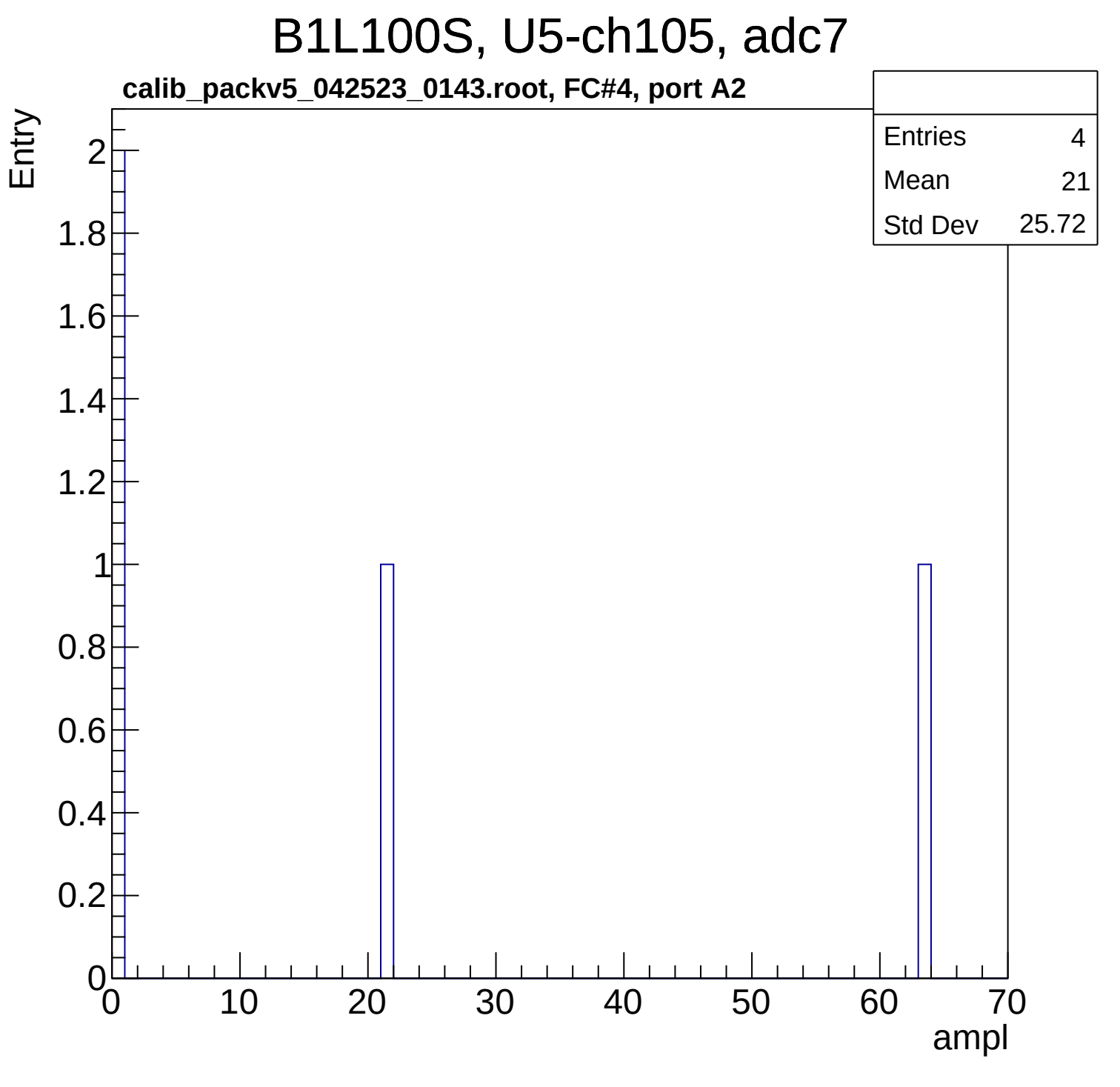
B1L100S, U5-ch105, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 4
Mean 21
Std Dev 25.72
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
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0
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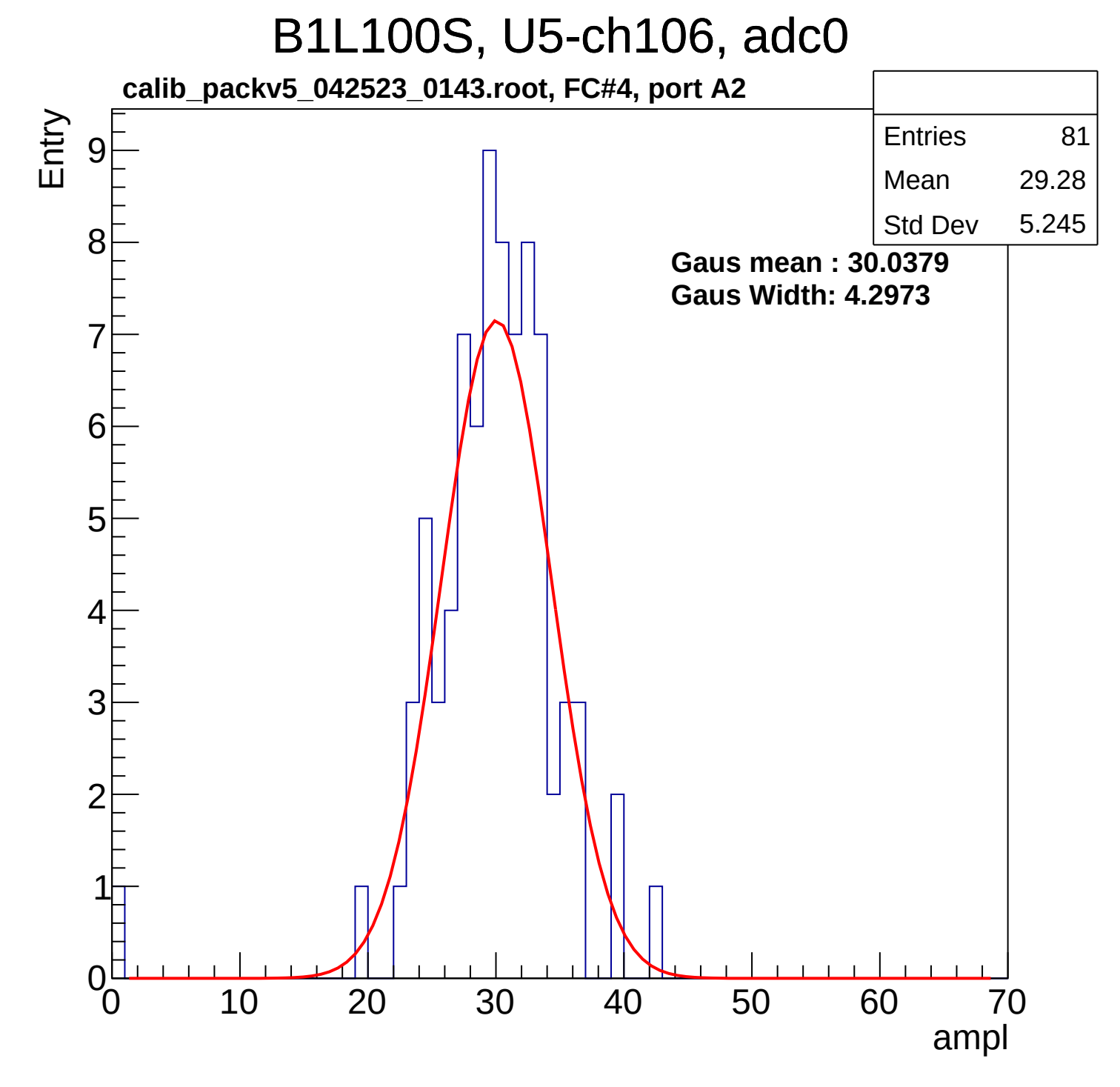
B1L100S, U5-ch106, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 81
Mean 29.28
Std Dev 5.245
Gaus mean : 30.0379
Gaus Width: 4.2973
Entry
ampl
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2
3
4
5
6
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0
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40
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60
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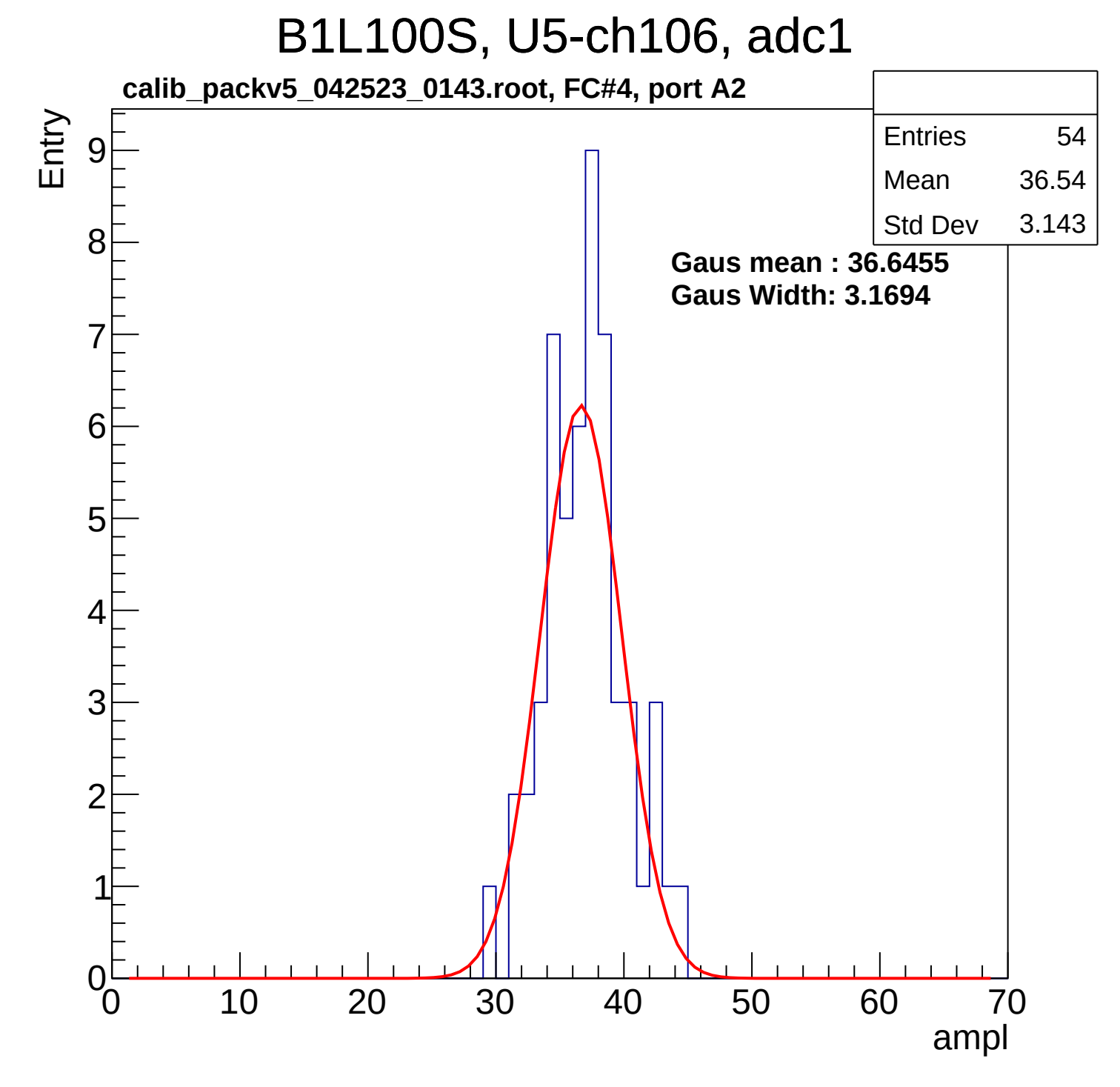
B1L100S, U5-ch106, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 36.54
Std Dev 3.143
Gaus mean : 36.6455
Gaus Width: 3.1694
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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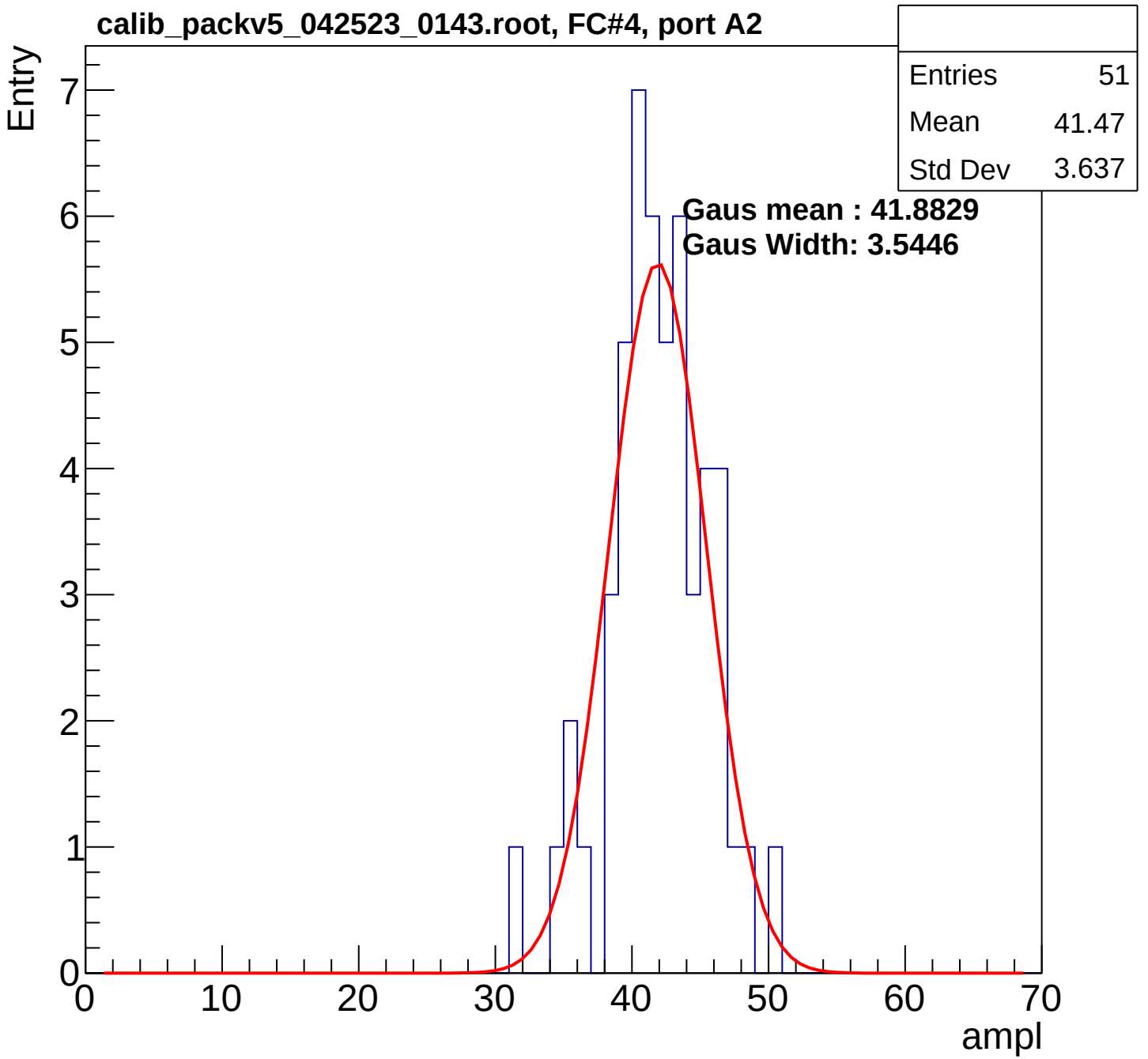
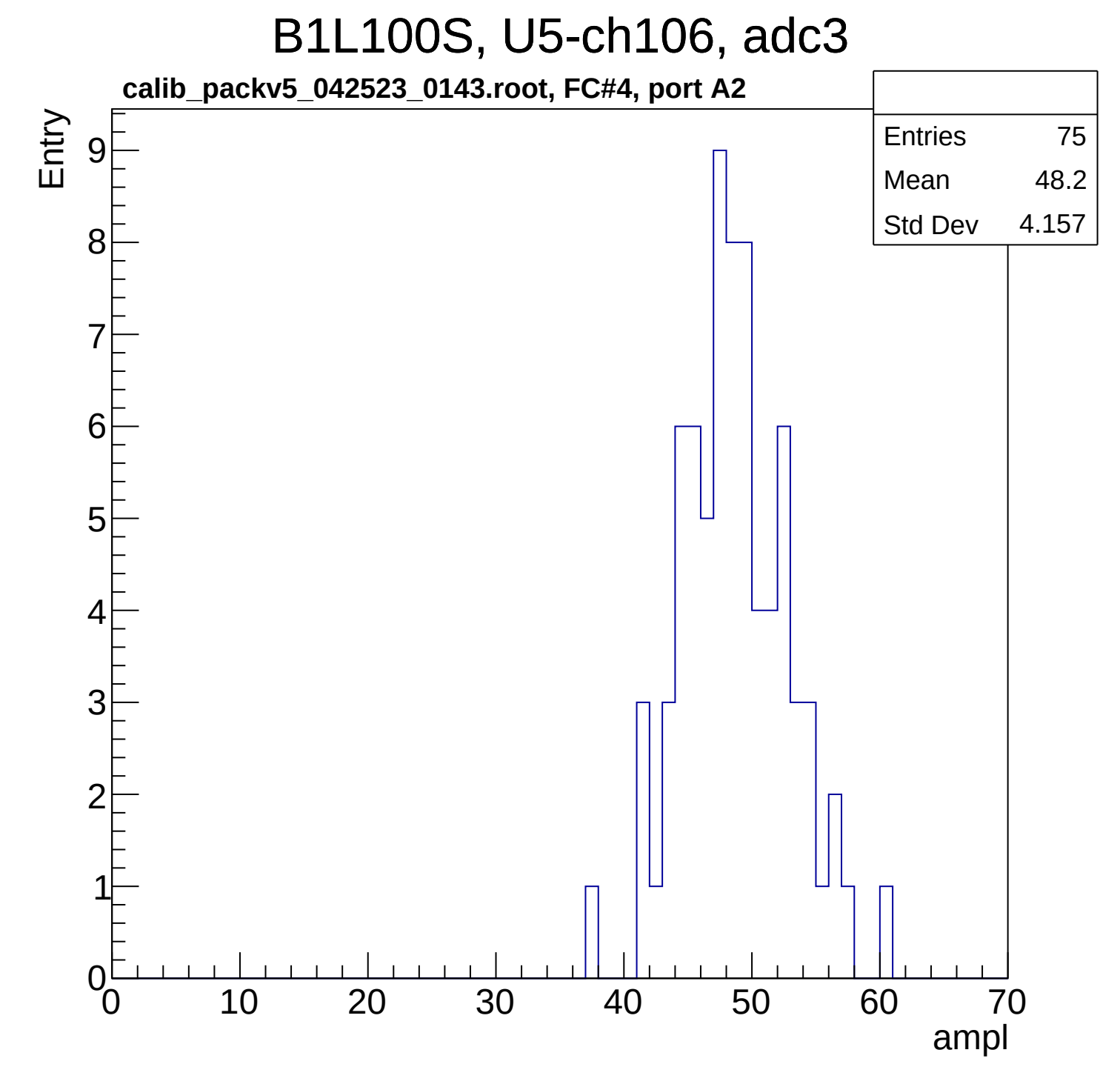

B1L100S, U5-ch106, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 41.47
Std Dev 3.637
Gaus mean : 41.8829
Gaus Width: 3.5446
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U5-ch106, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 75
Mean 48.2
Std Dev 4.157
Entry
ampl
0
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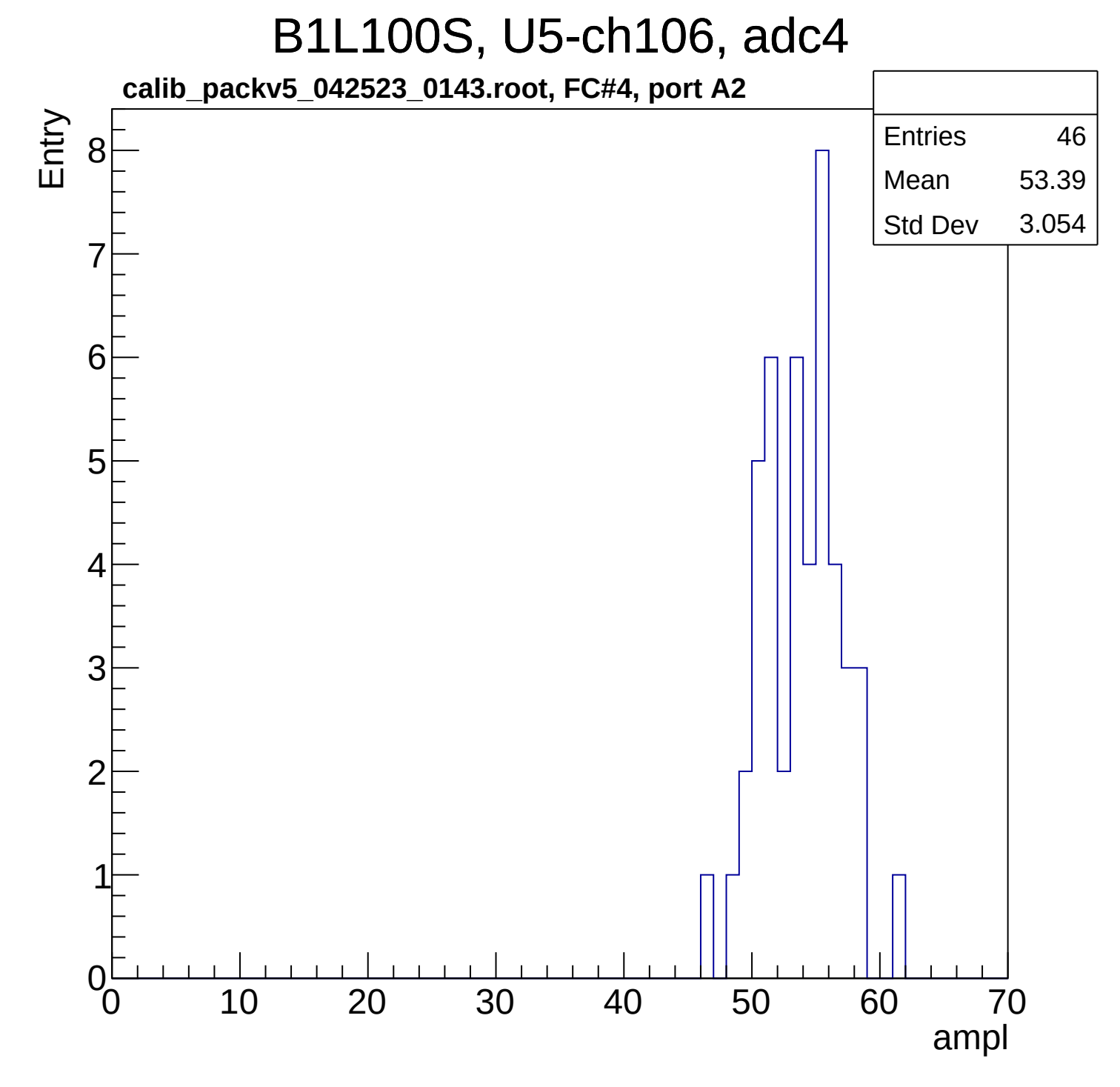
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch106, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 46
Mean 53.39
Std Dev 3.054
Entry
ampl
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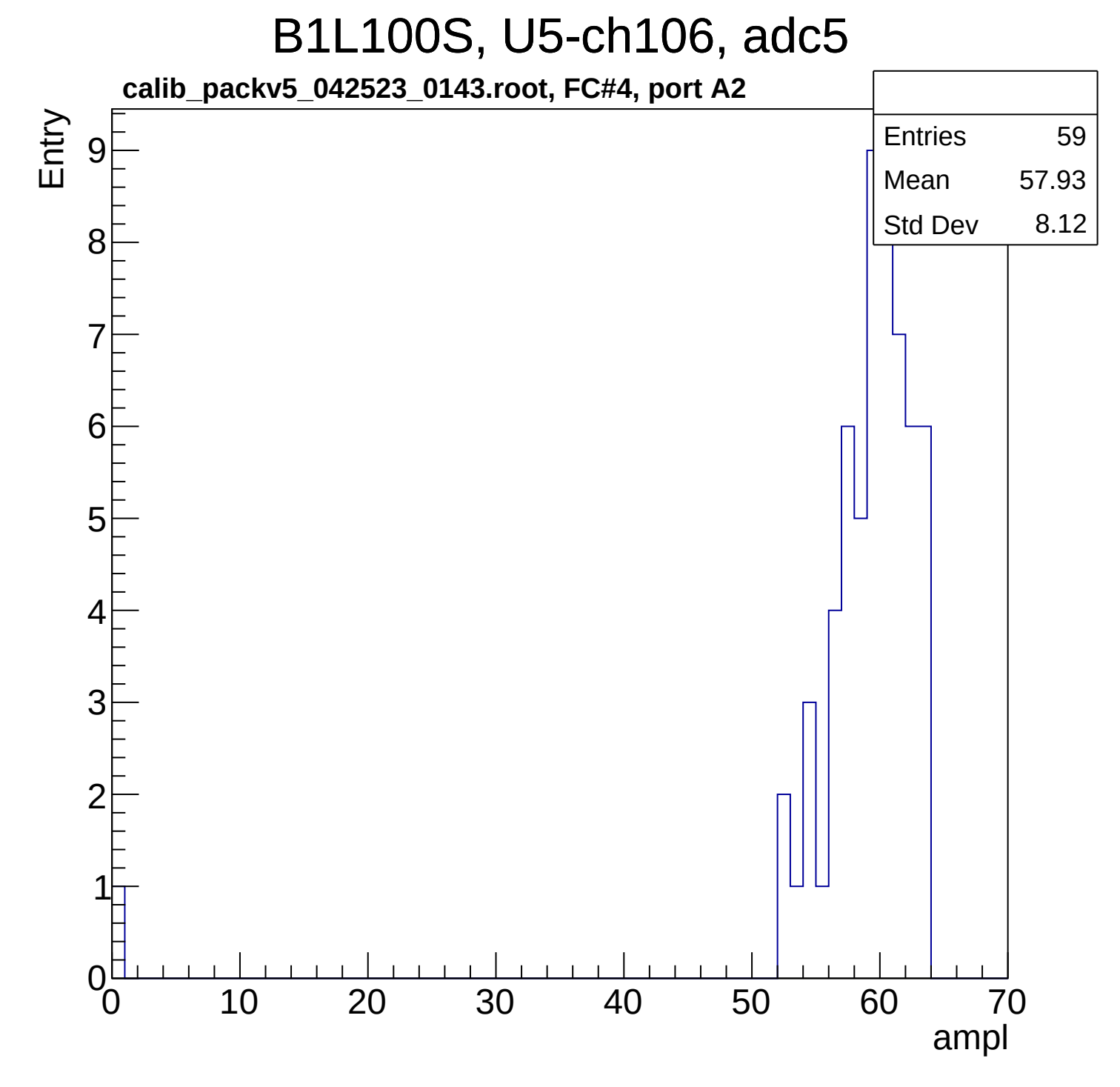
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch106, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 57.93
Std Dev 8.12
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
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60
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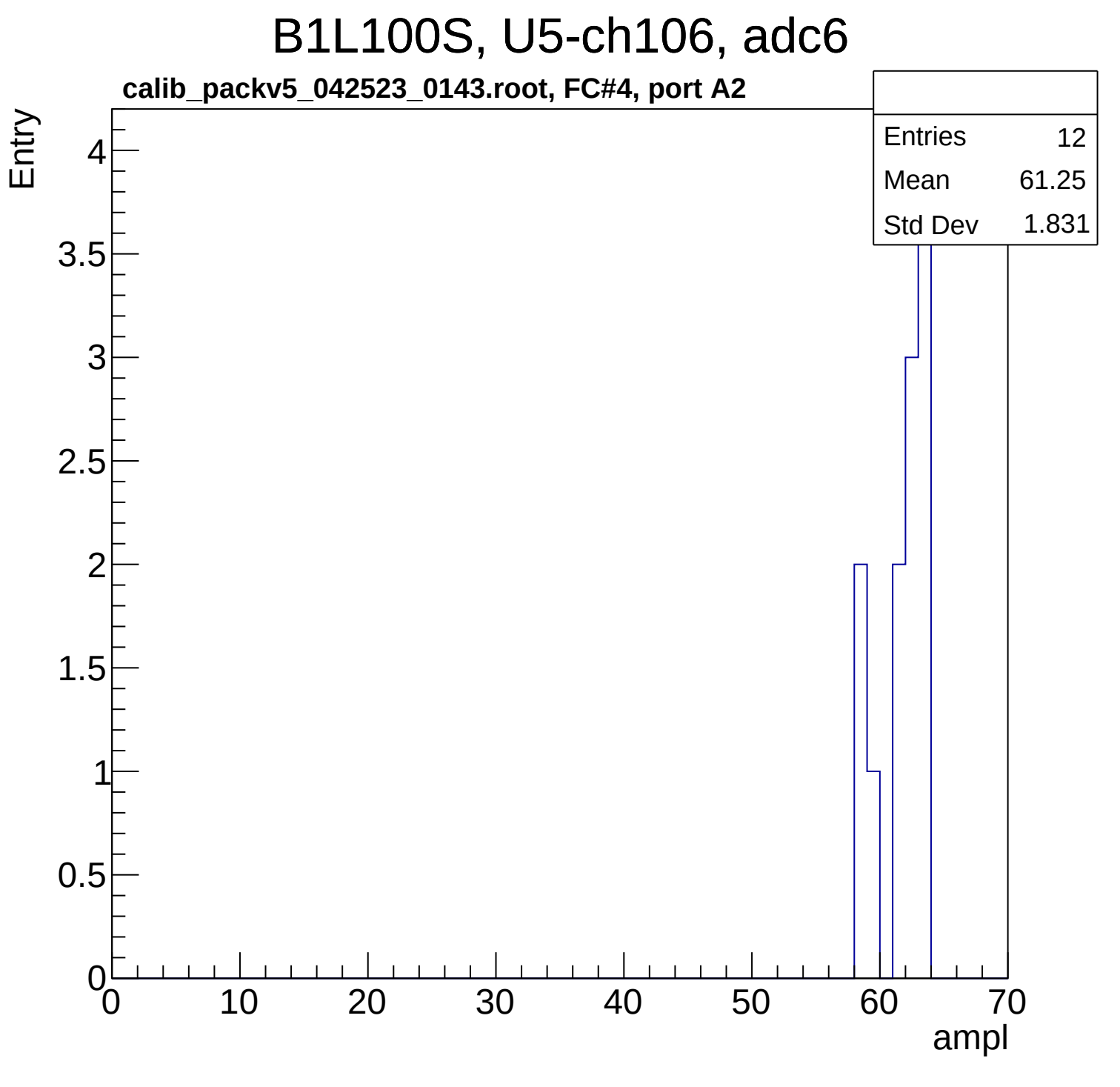
B1L100S, U5-ch106, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 12
Mean 61.25
Std Dev 1.831
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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40
50
60
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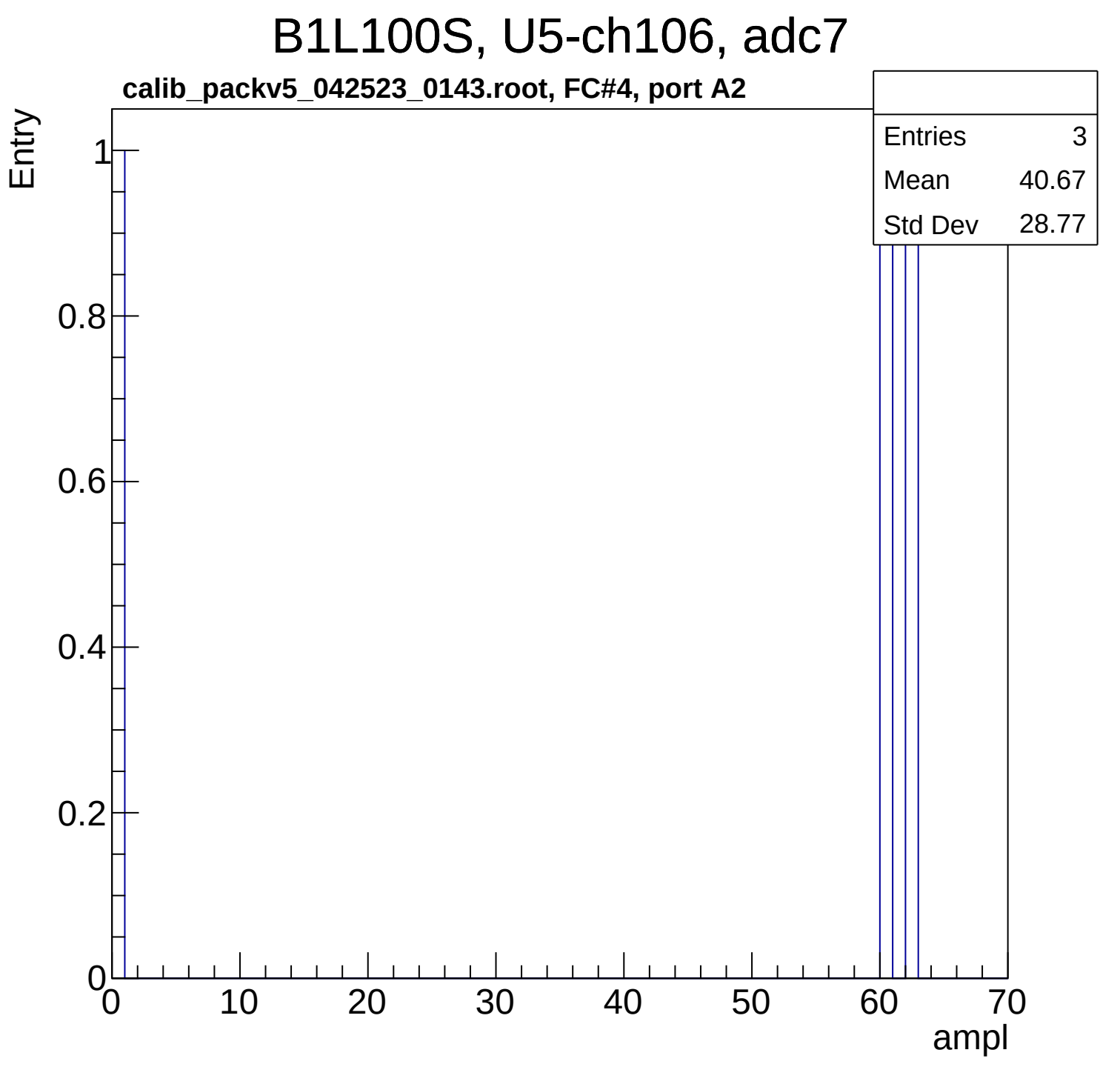
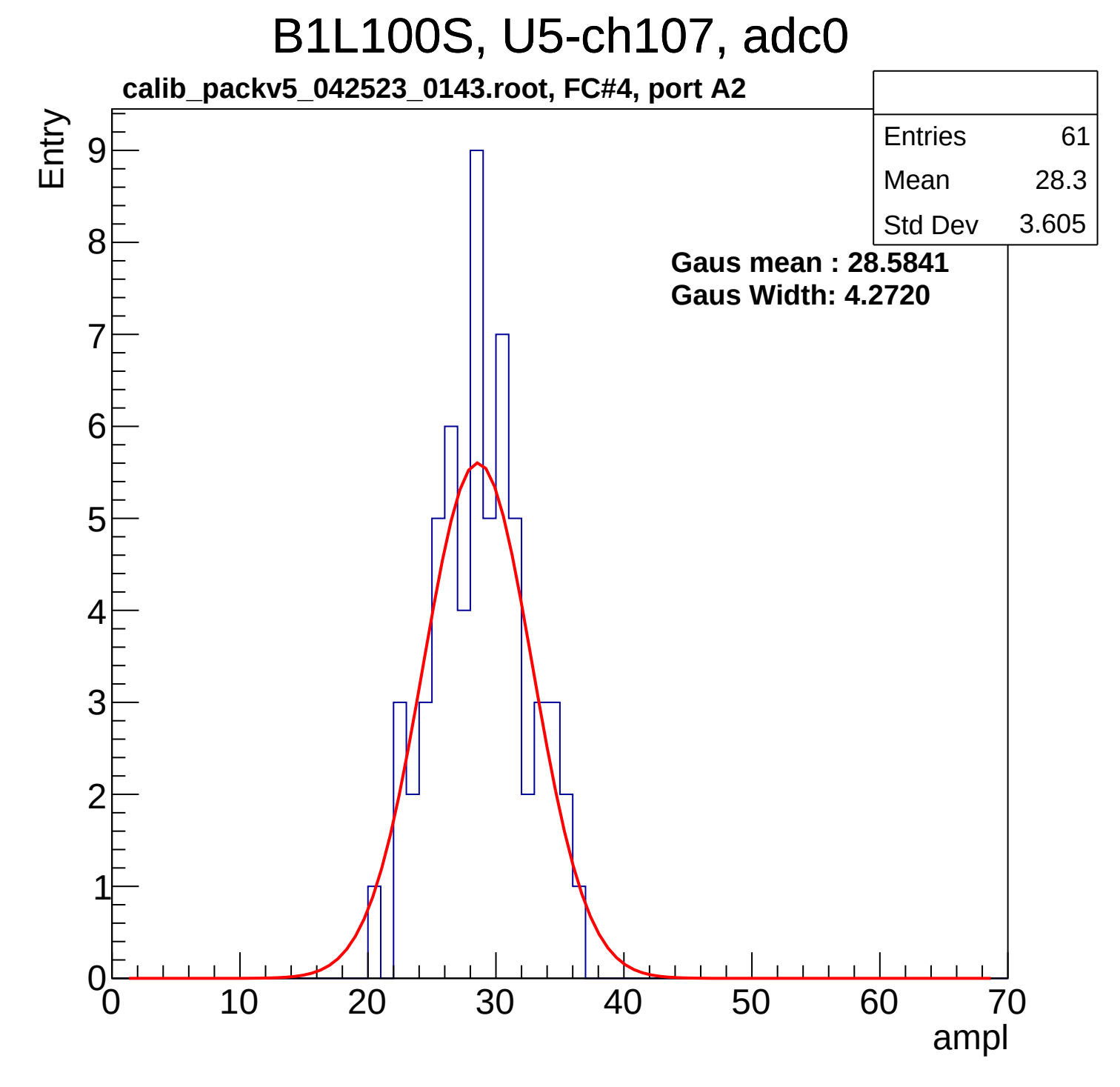

B1L100S, U5-ch106, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 40.67
Std Dev 28.77
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B1L100S, U5-ch107, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 28.3
Std Dev 3.605
Gaus mean : 28.5841
Gaus Width: 4.2720
Entry
ampl
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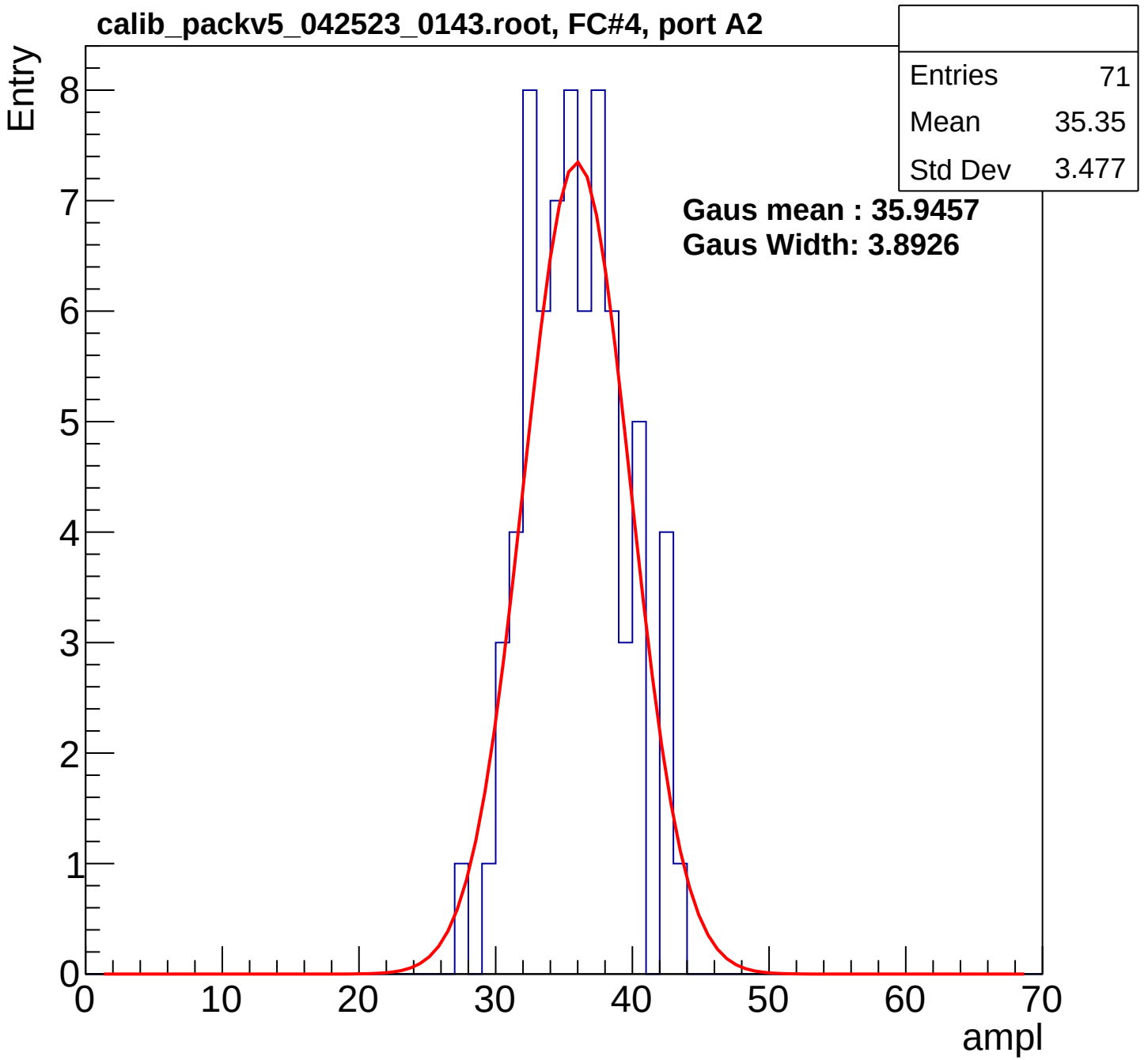
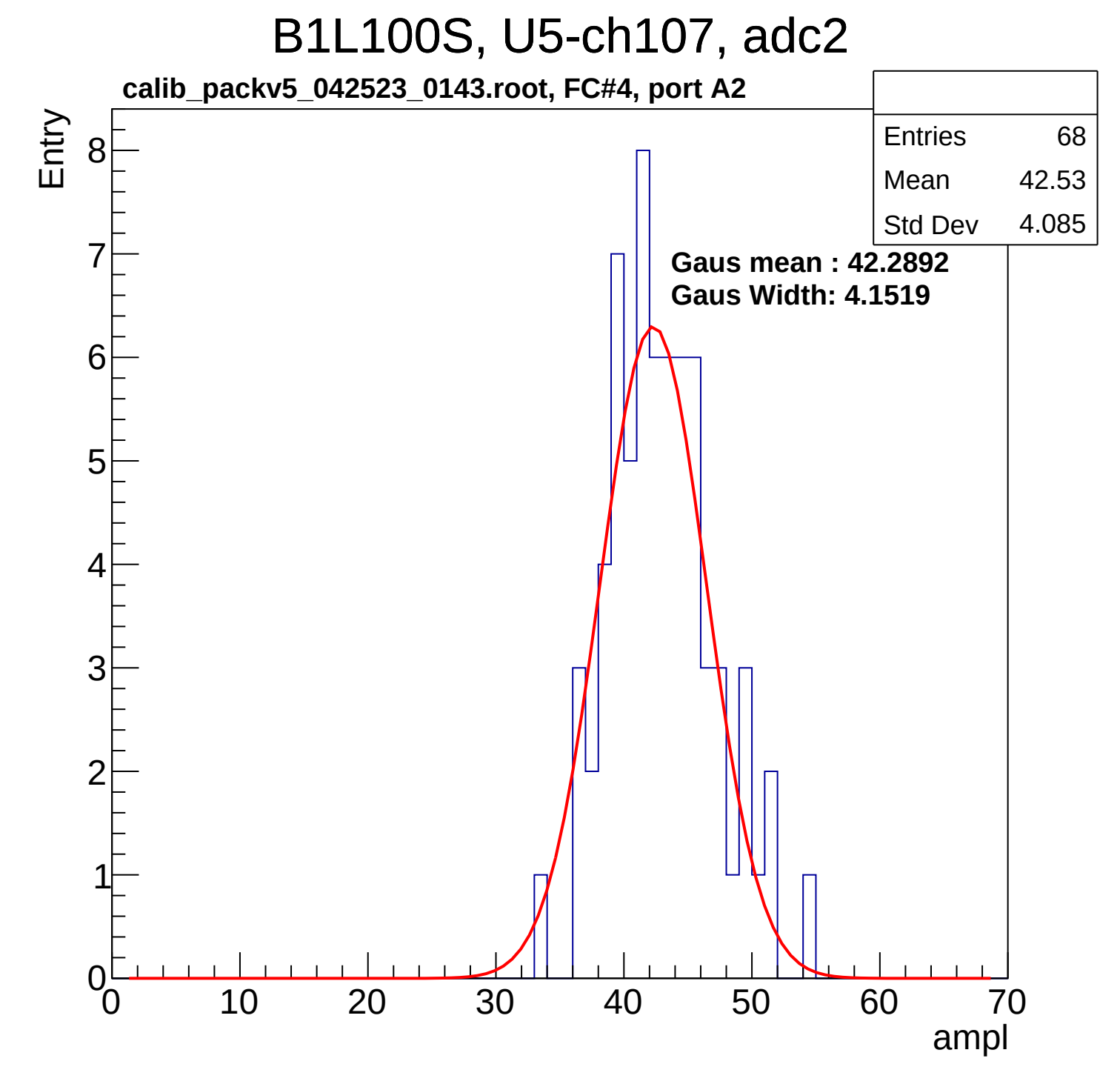
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch107, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 35.35
Std Dev 3.477
Gaus mean : 35.9457
Gaus Width: 3.8926
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch107, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 42.53
Std Dev 4.085
Gaus mean : 42.2892
Gaus Width: 4.1519
Entry
ampl
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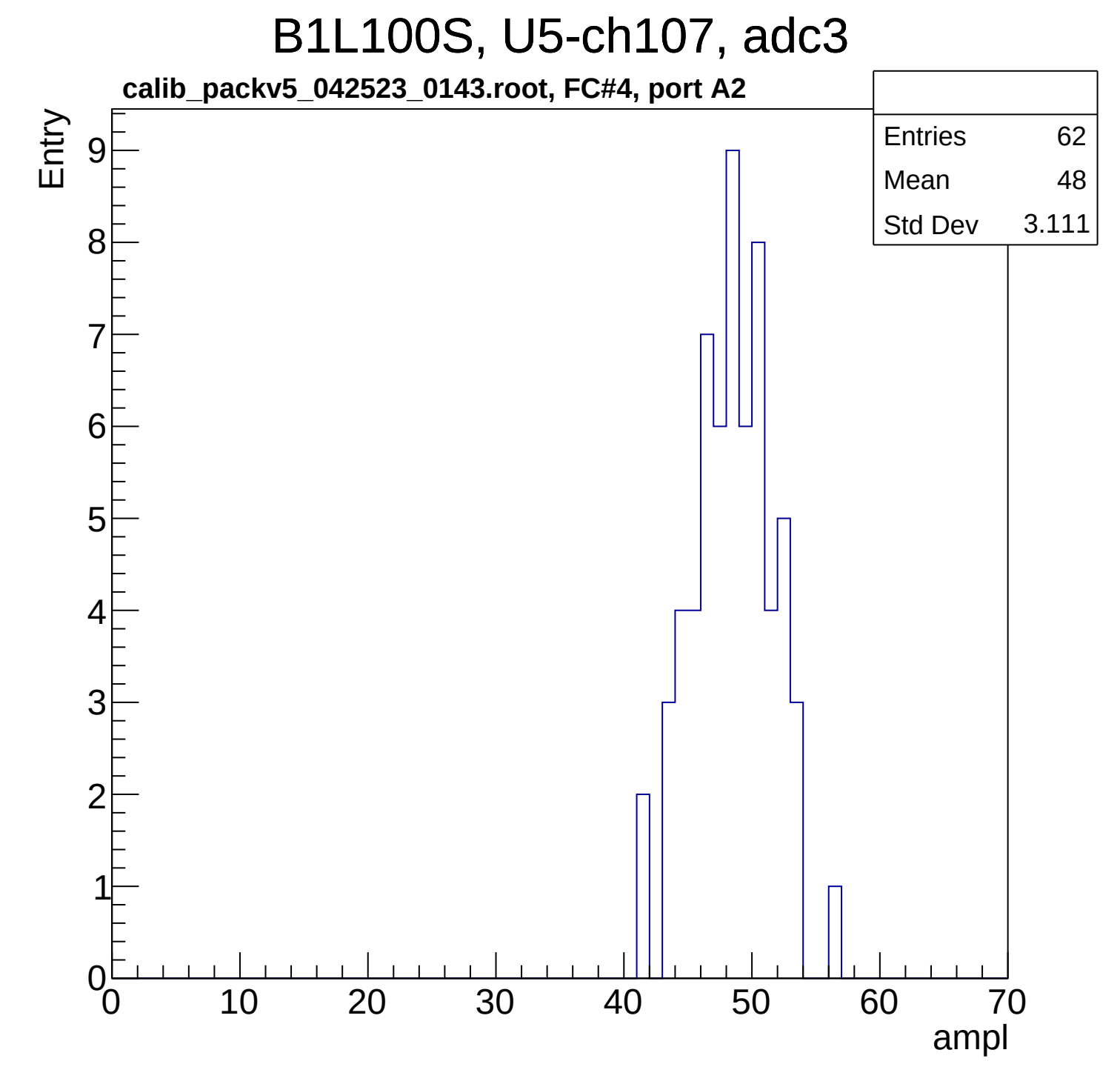
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch107, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 48
Std Dev 3.111
Entry
ampl
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2
3
4
5
6
7
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0
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20
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60
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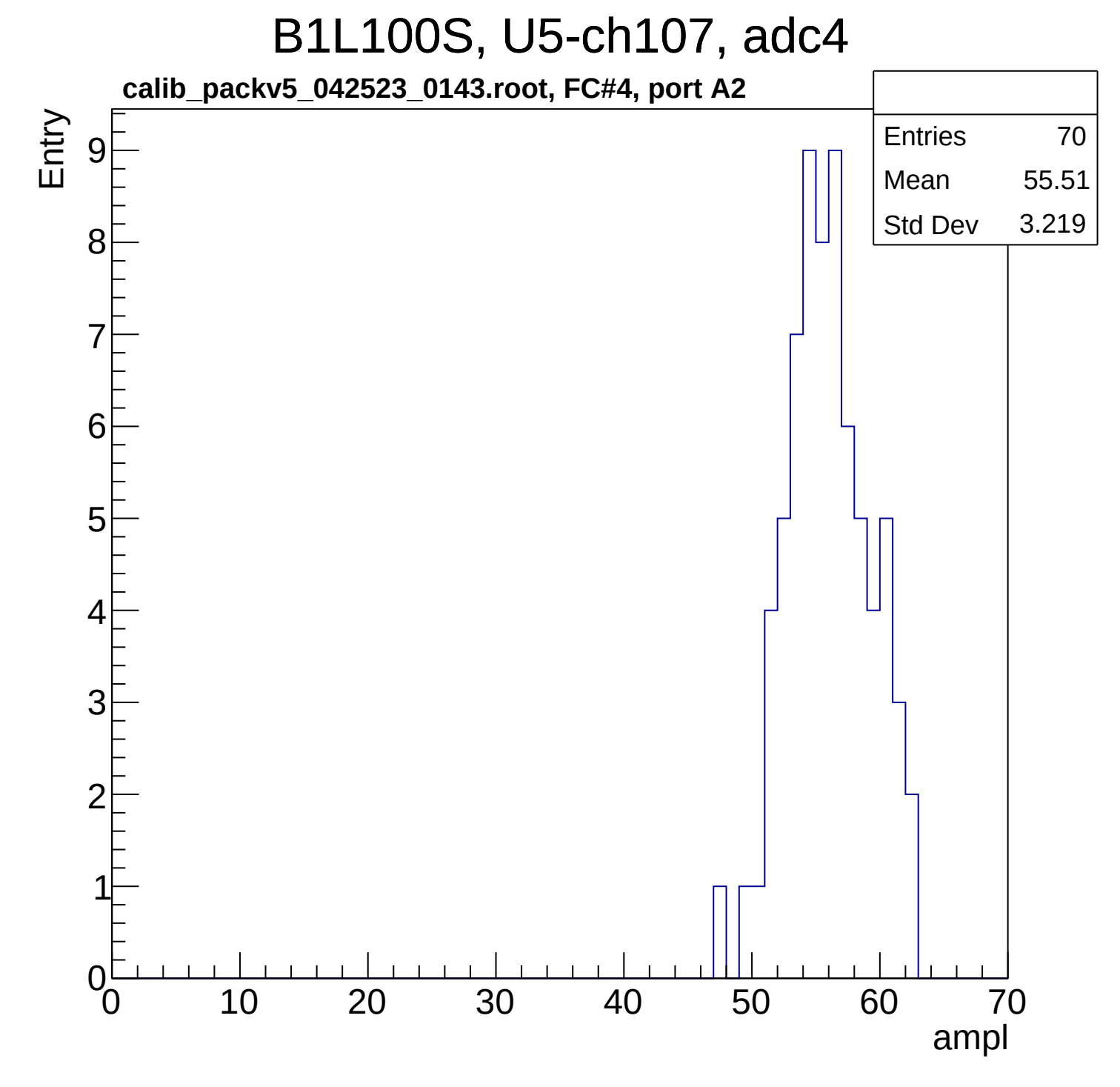
B1L100S, U5-ch107, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 55.51
Std Dev 3.219
Entry
ampl
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3
4
5
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7
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0
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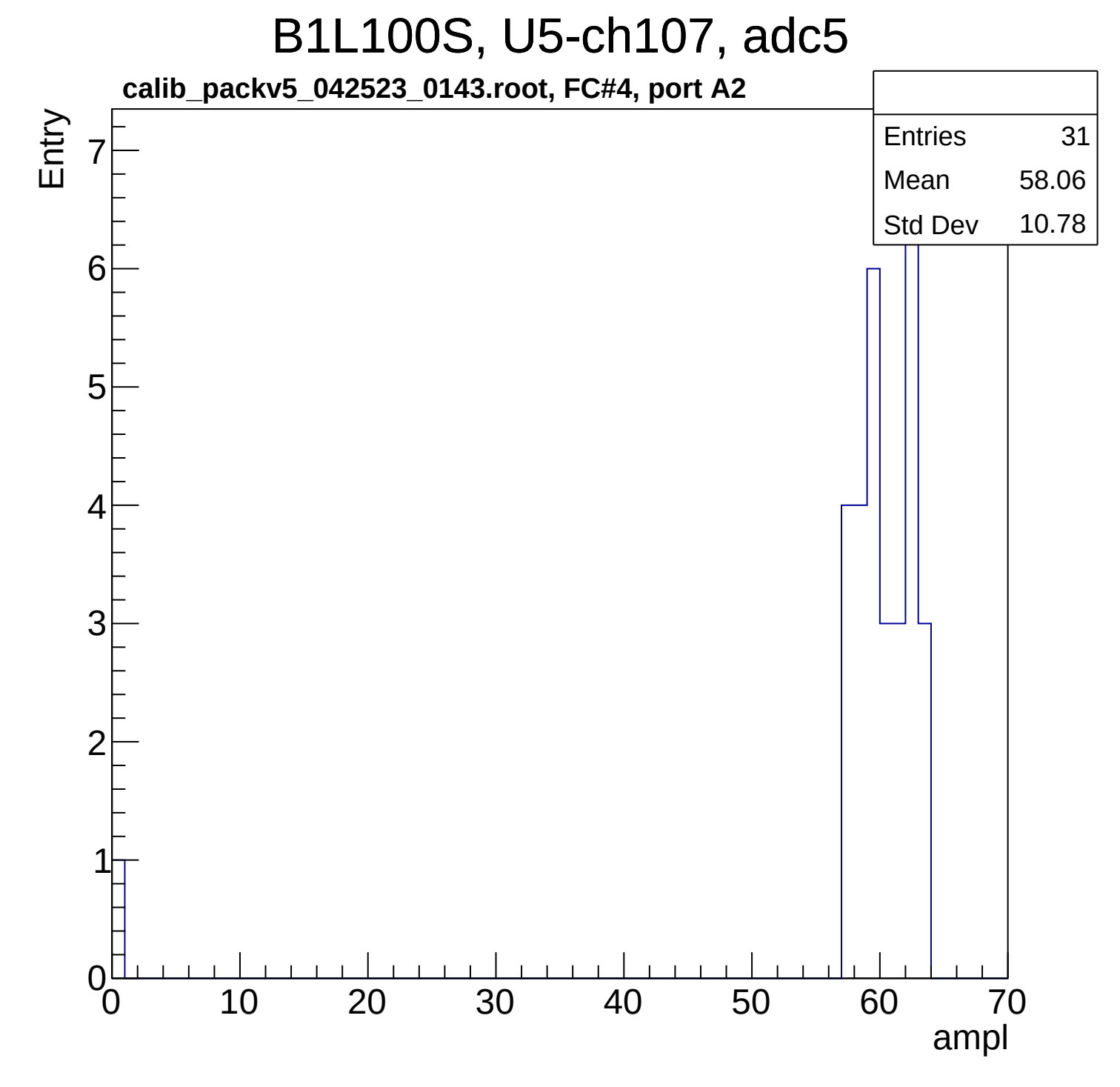
B1L100S, U5-ch107, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 31
Mean 58.06
Std Dev 10.78
Entry
ampl
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1
2
3
4
5
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0
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40
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60
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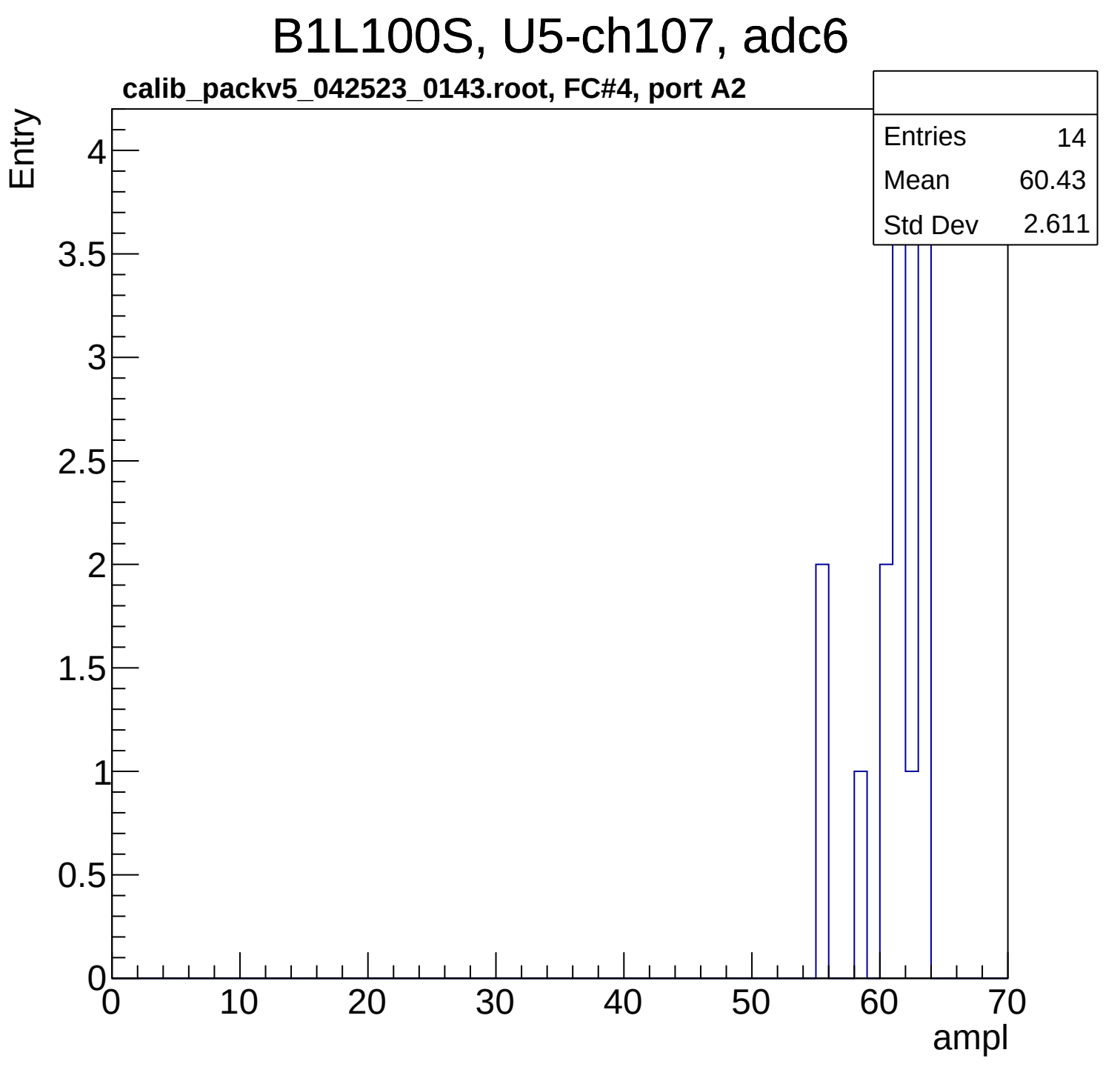
B1L100S, U5-ch107, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 14
Mean 60.43
Std Dev 2.611
Entry
ampl
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1.5
2
2.5
3
3.5
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0
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60
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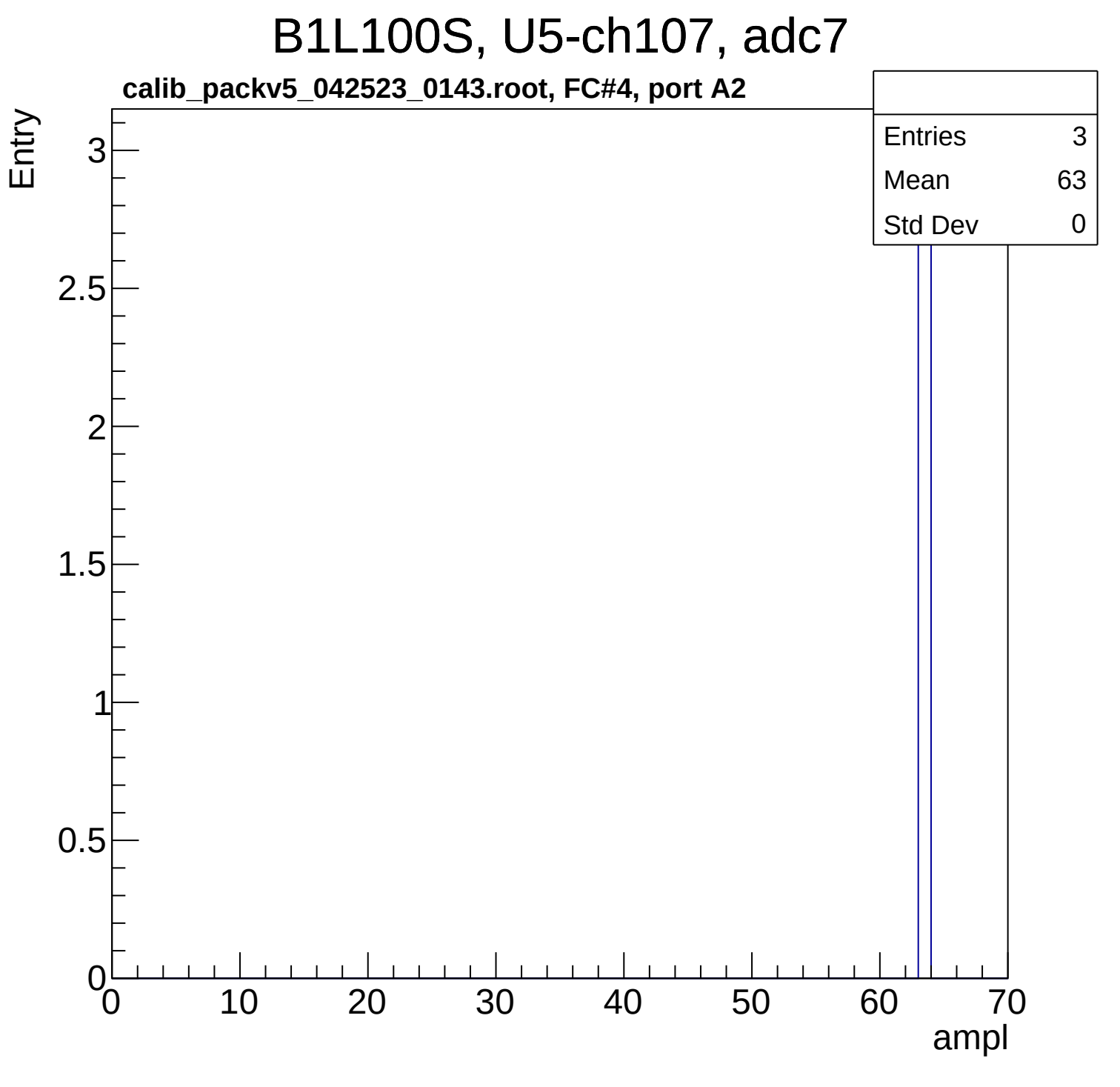
B1L100S, U5-ch107, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 63
Std Dev 0
Entry
ampl
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0.5
1
1.5
2
2.5
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0
10
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40
50
60
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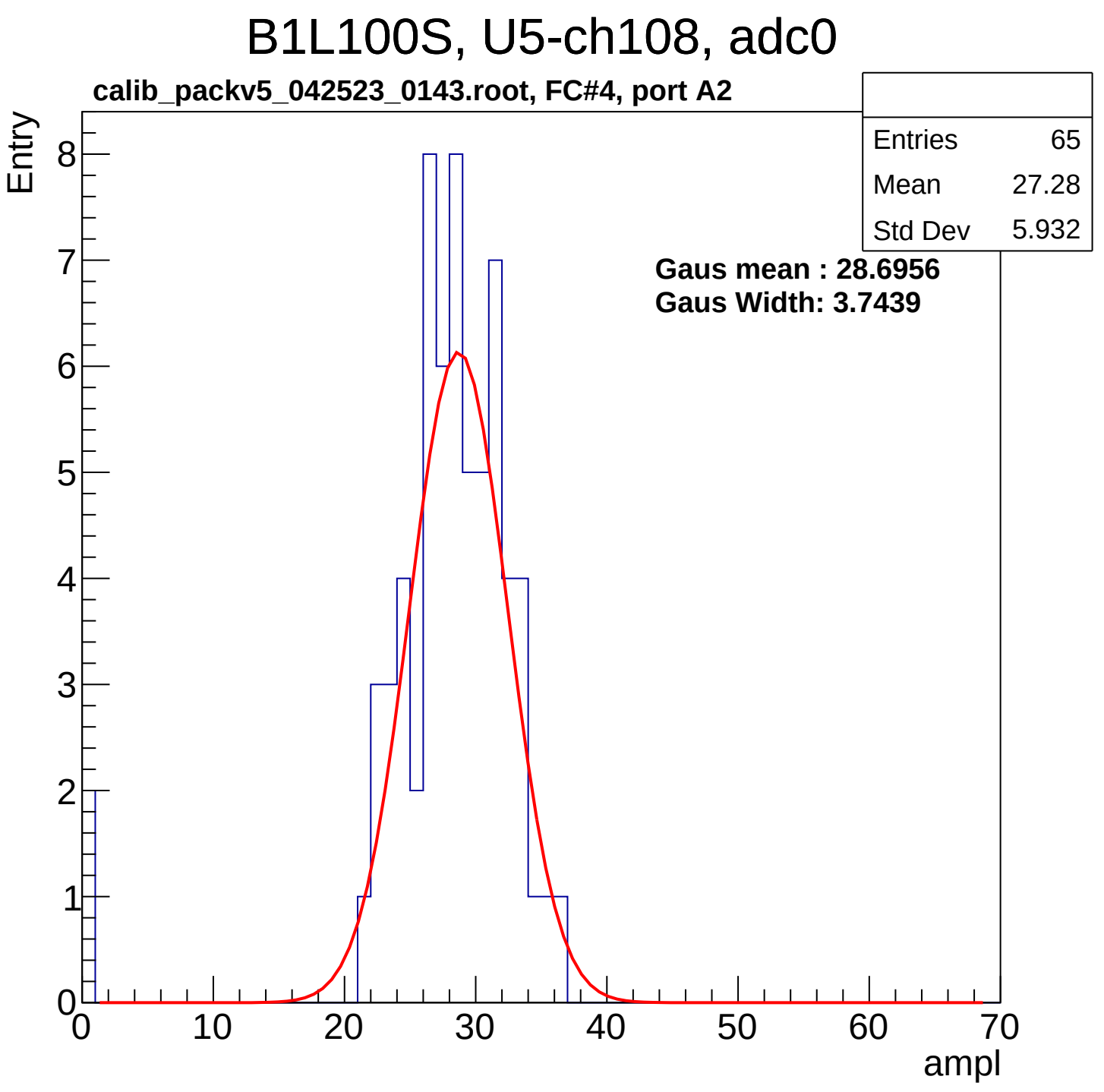
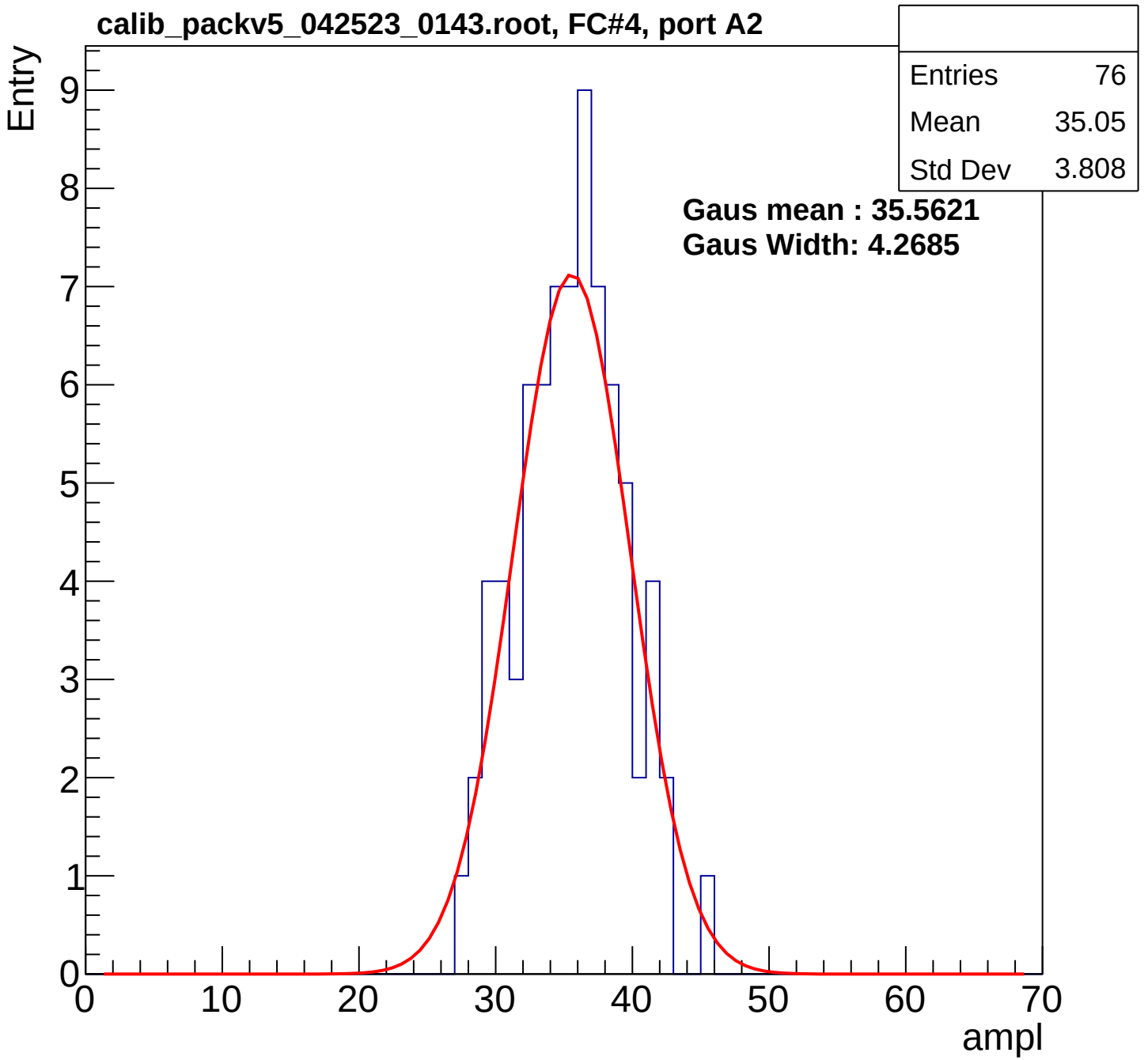

B1L100S, U5-ch108, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 27.28
Std Dev 5.932
Gaus mean : 28.6956
Gaus Width: 3.7439
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch108, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 76
Mean 35.05
Std Dev 3.808
Gaus mean : 35.5621
Gaus Width: 4.2685
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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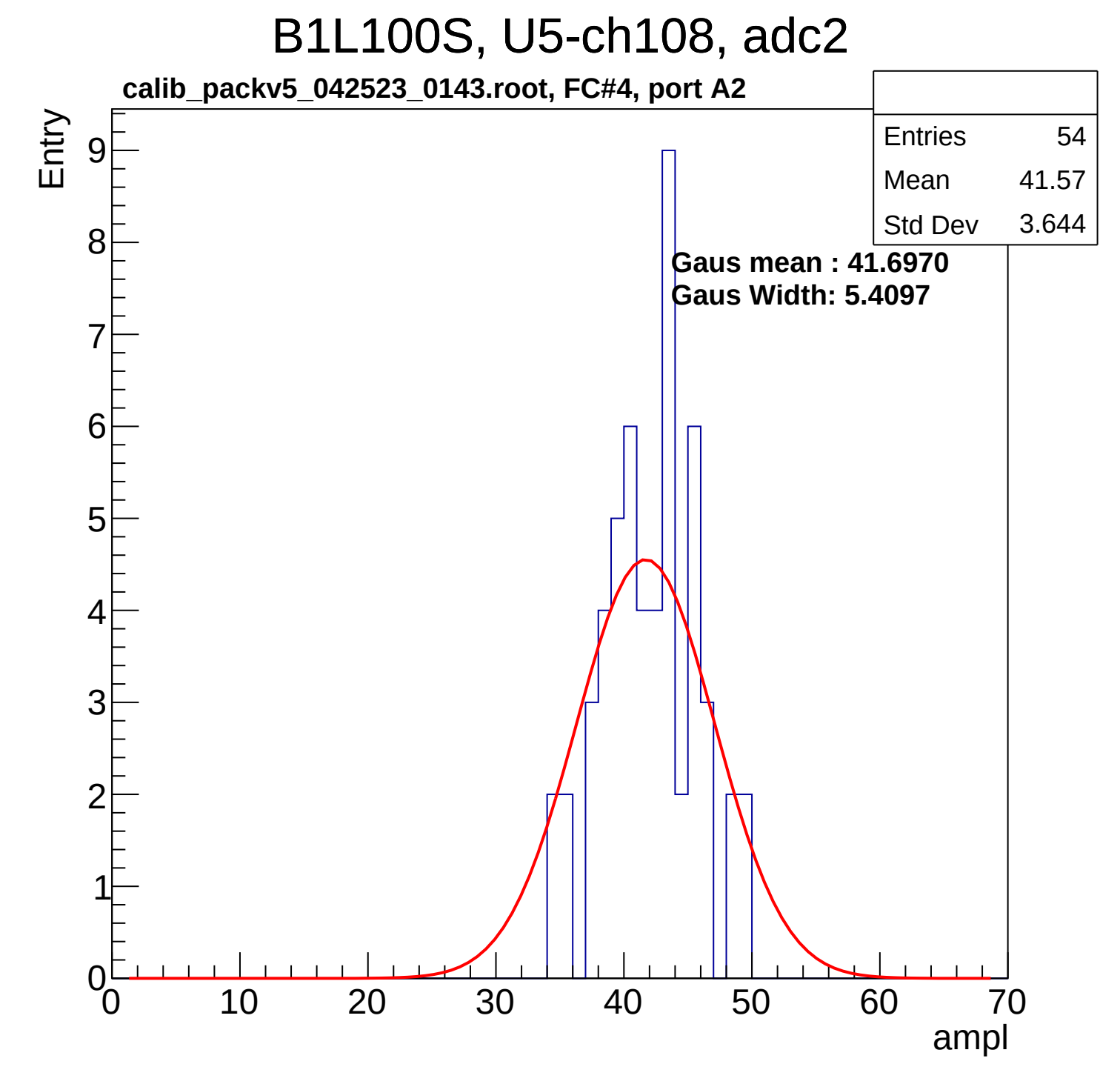
B1L100S, U5-ch108, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 41.57
Std Dev 3.644
Gaus mean : 41.6970
Gaus Width: 5.4097
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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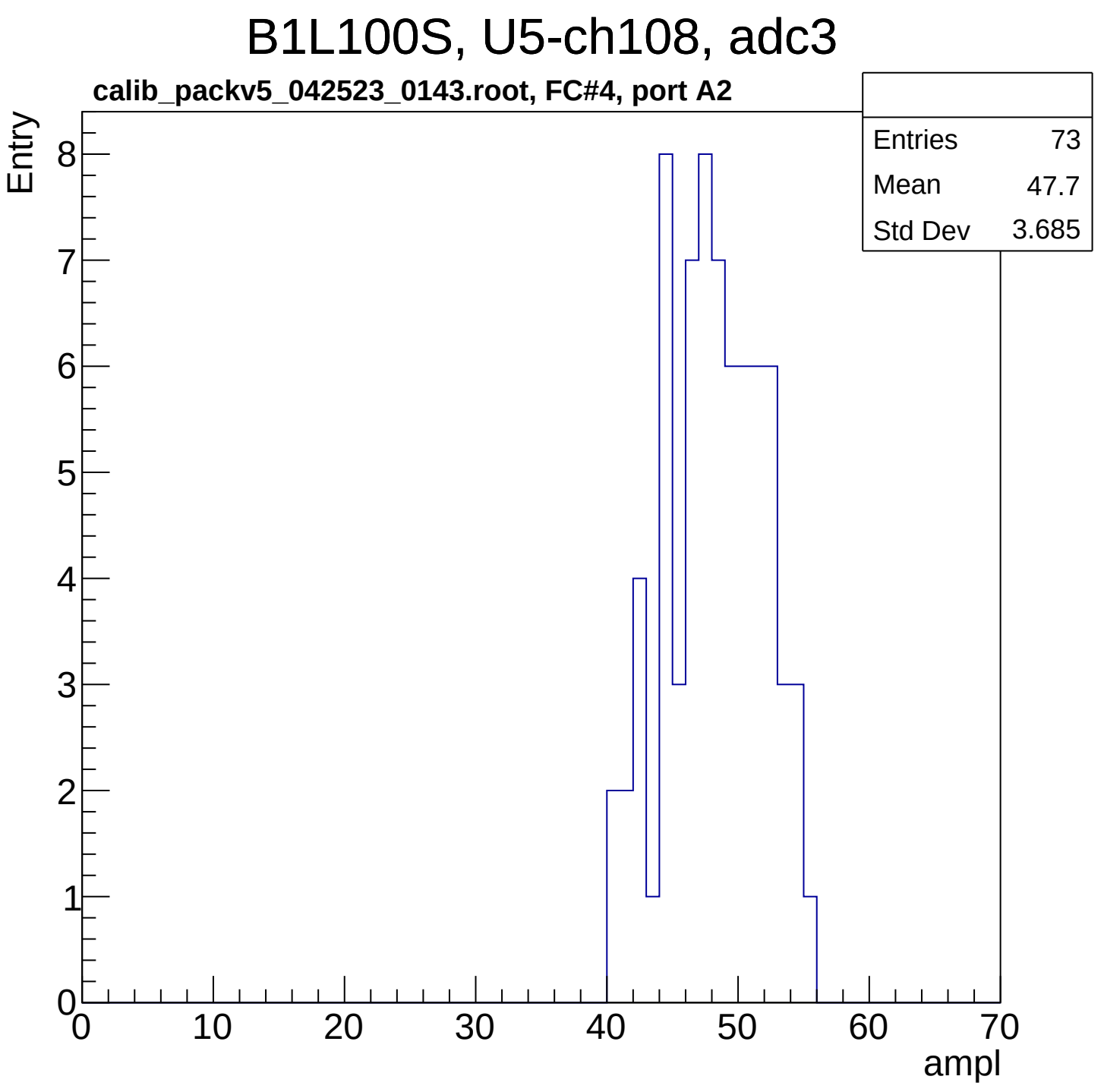
B1L100S, U5-ch108, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 47.7
Std Dev 3.685
Entry
ampl
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1
2
3
4
5
6
7
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0
10
20
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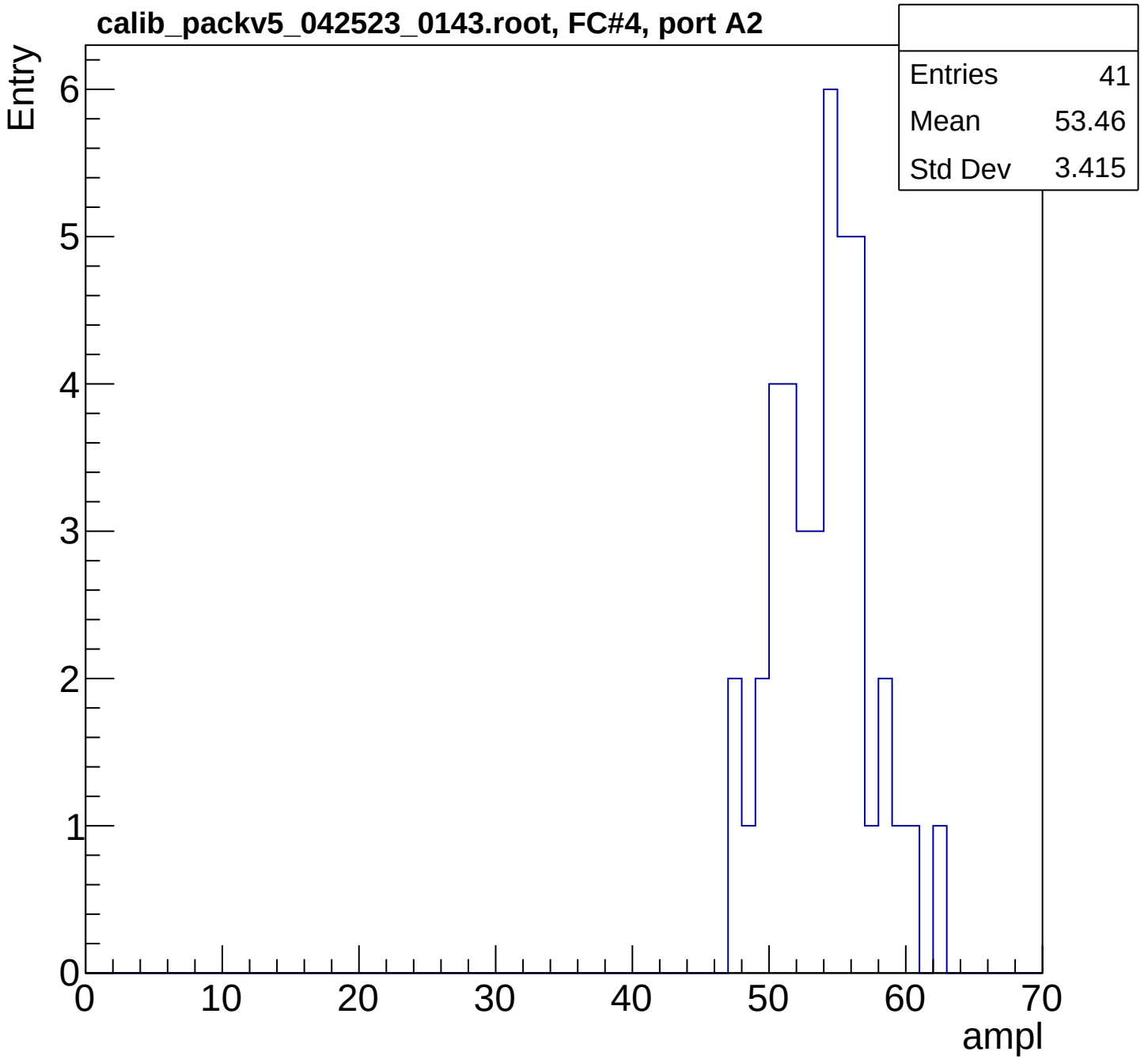
B1L100S, U5-ch108, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 41
Mean 53.46
Std Dev 3.415
Entry
0
1
2
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4
5
6
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10
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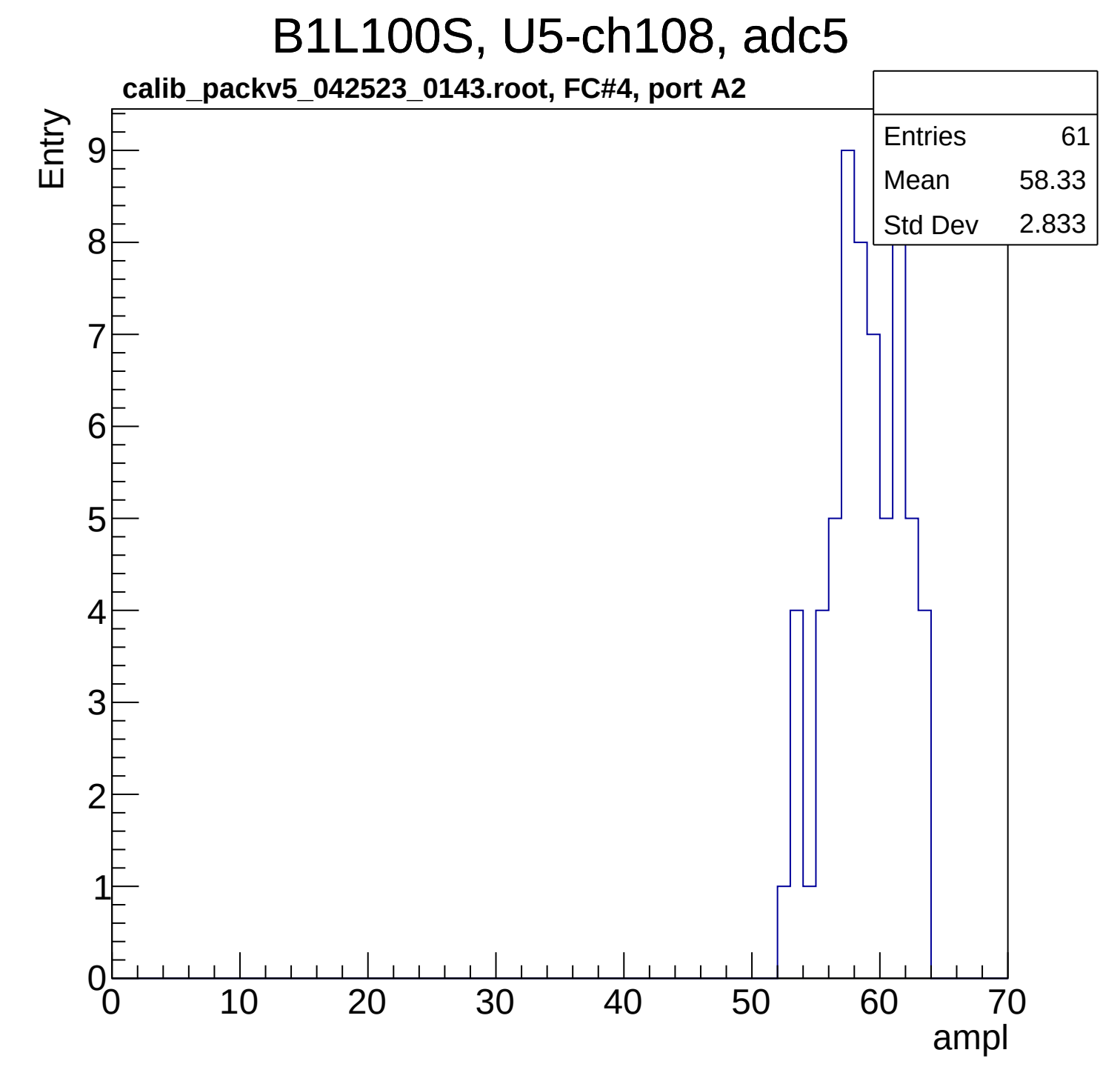
30
40
50
60
70
ampl


B1L100S, U5-ch108, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 58.33
Std Dev 2.833
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
30
40
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60
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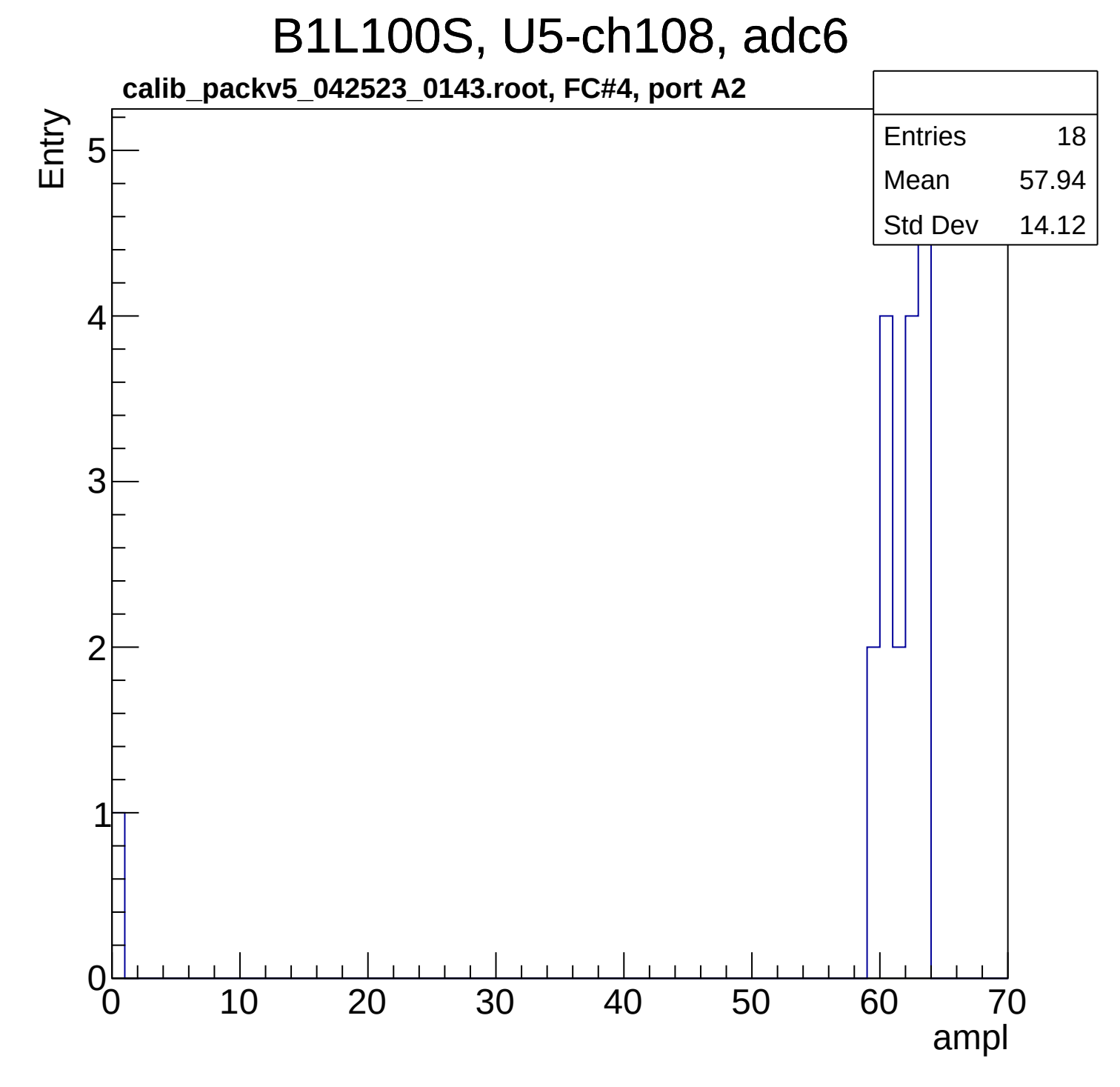
B1L100S, U5-ch108, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 18
Mean 57.94
Std Dev 14.12
Entry
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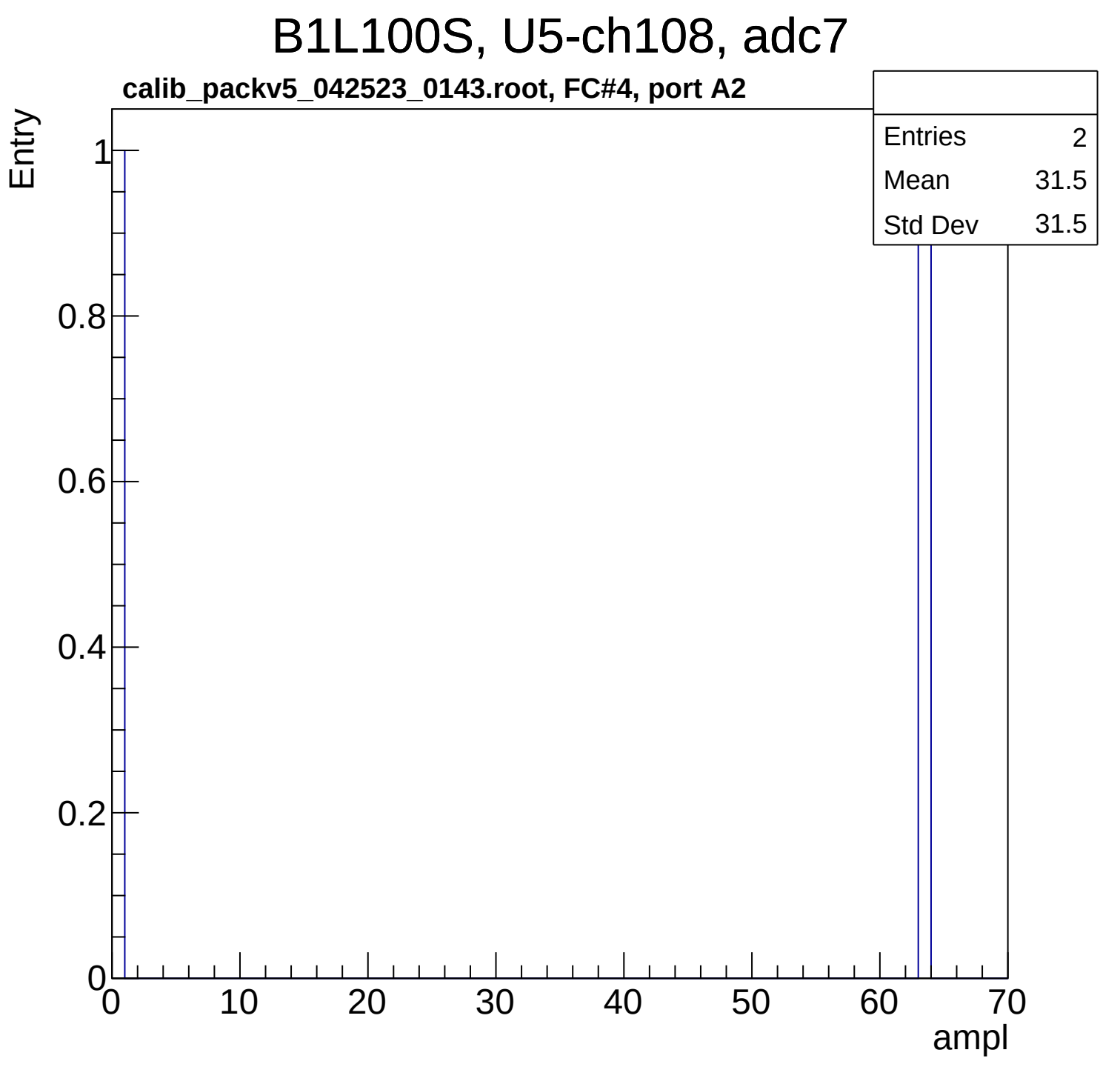
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch108, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 31.5
Std Dev 31.5
Entry
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0.6
0.4
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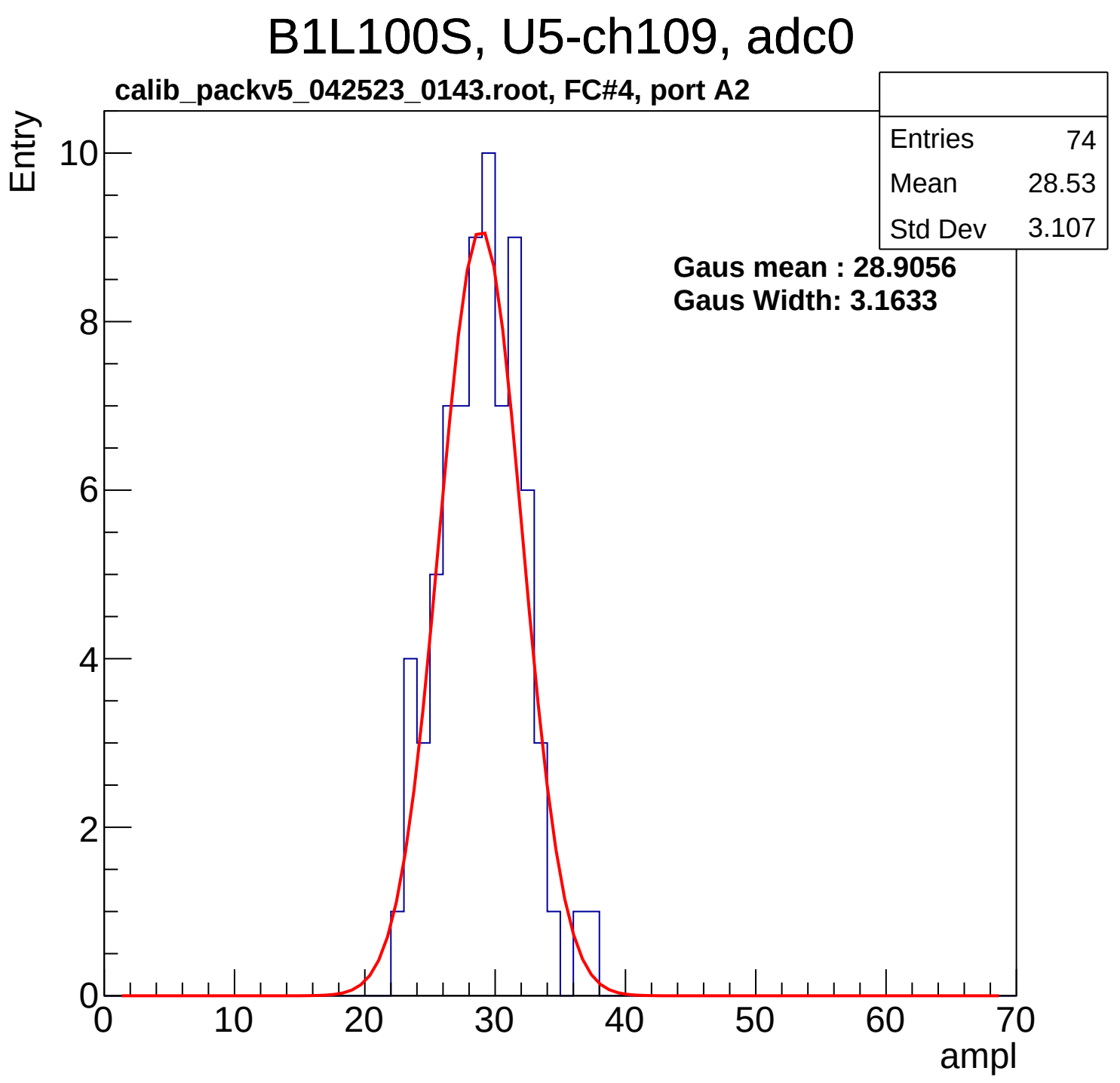
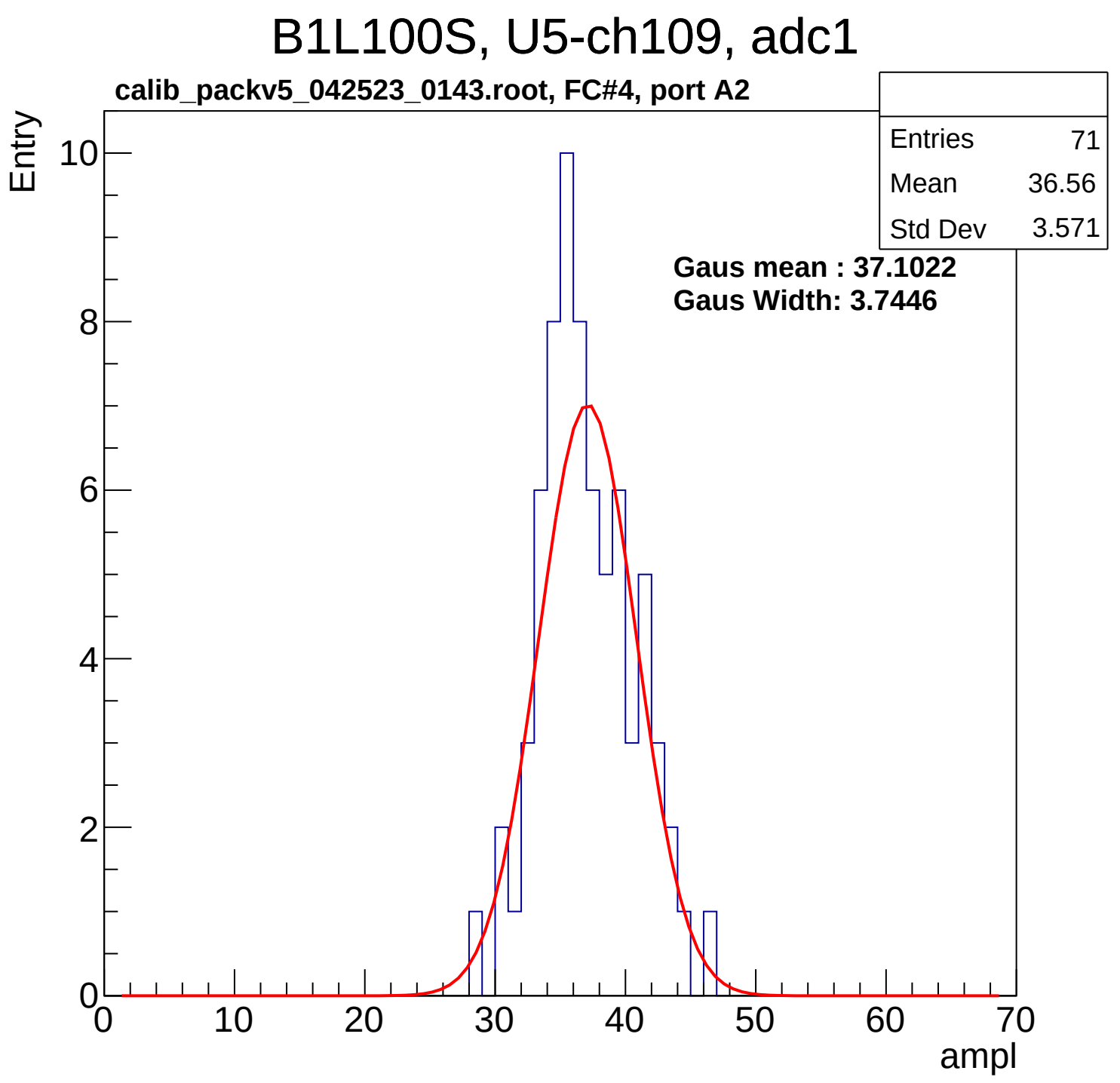
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch109, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 74
Mean 28.53
Std Dev 3.107
Gaus mean : 28.9056
Gaus Width: 3.1633
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch109, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 36.56
Std Dev 3.571
Gaus mean : 37.1022
Gaus Width: 3.7446
Entry
ampl
0
2
4
6
8
10
0
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40
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60
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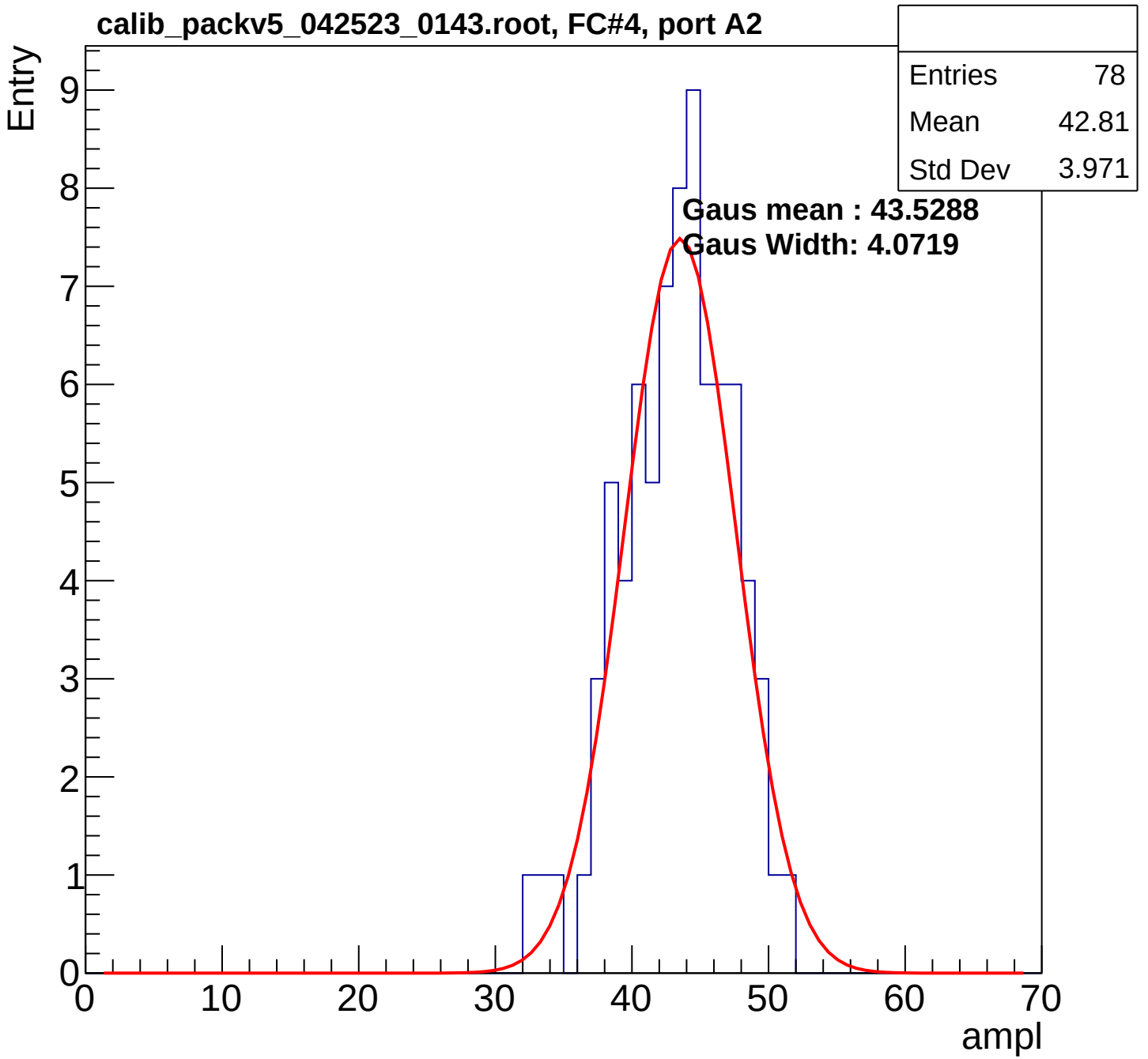
B1L100S, U5-ch109, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 78
Mean 42.81
Std Dev 3.971
Gaus mean : 43.5288
Gaus Width: 4.0719
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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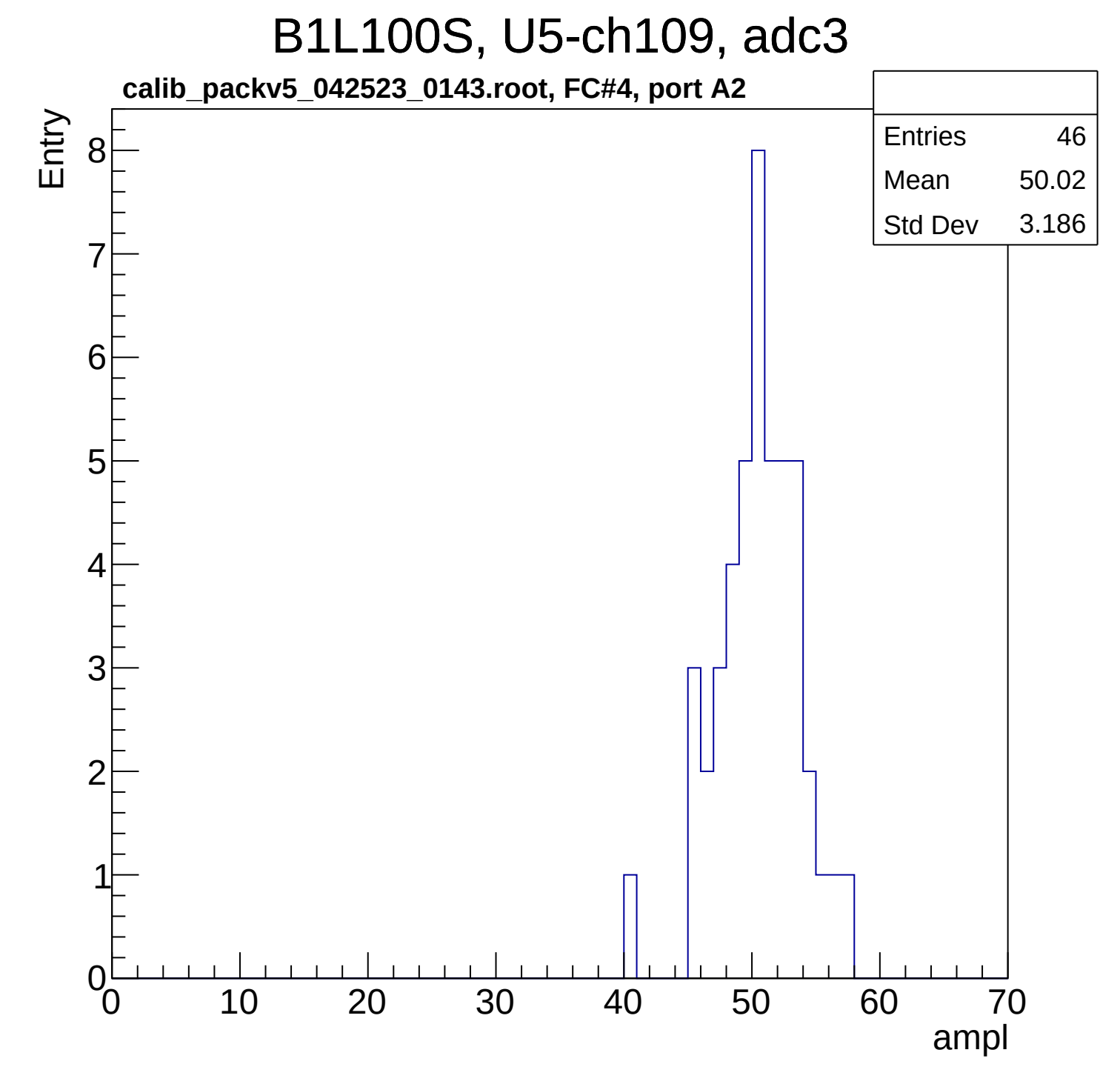
B1L100S, U5-ch109, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 46
Mean 50.02
Std Dev 3.186
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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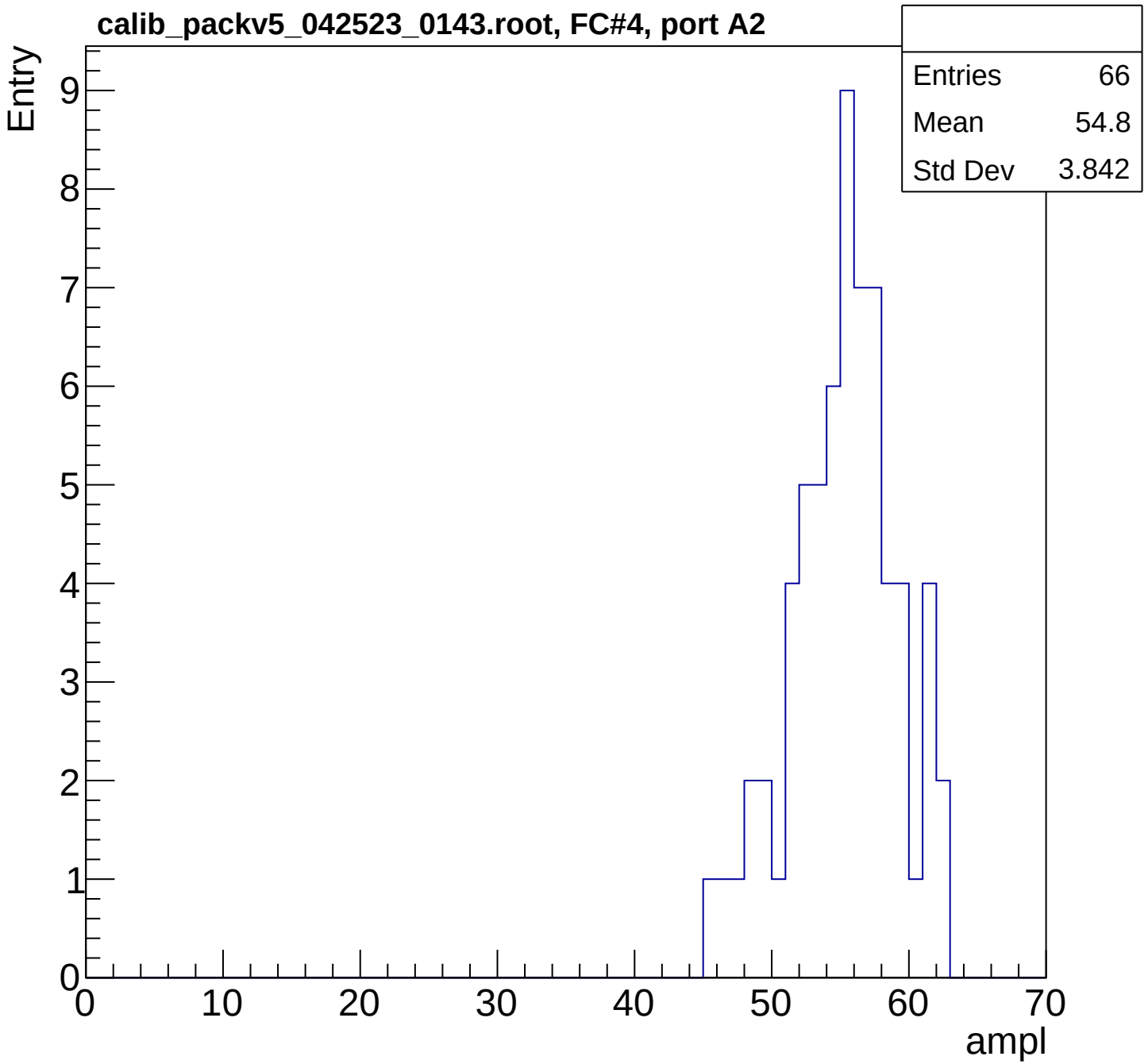
B1L100S, U5-ch109, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 54.8
Std Dev 3.842
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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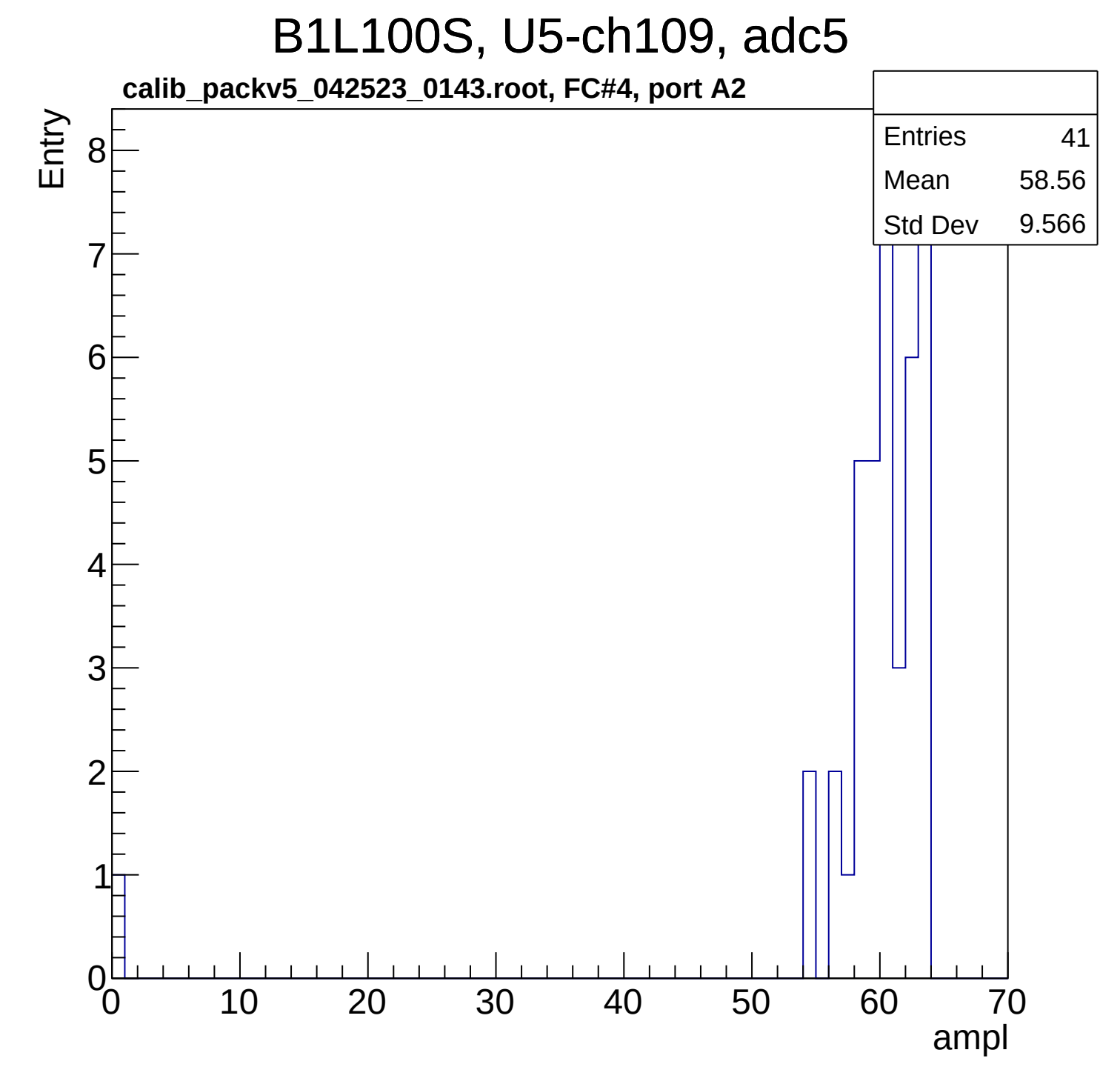
40
50
60
70


B1L100S, U5-ch109, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 41
Mean 58.56
Std Dev 9.566
Entry
ampl
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2
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5
6
7
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0
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60
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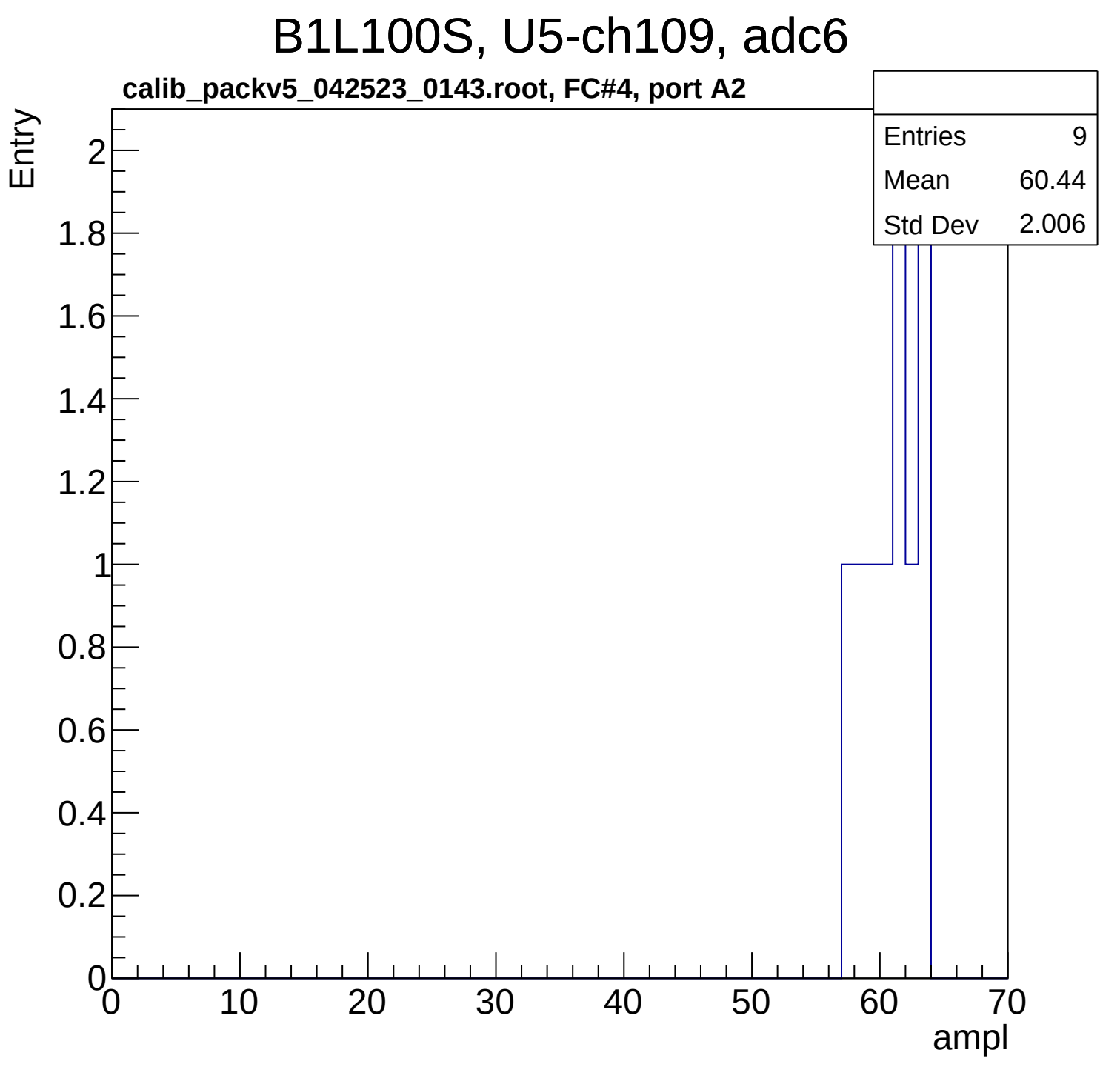
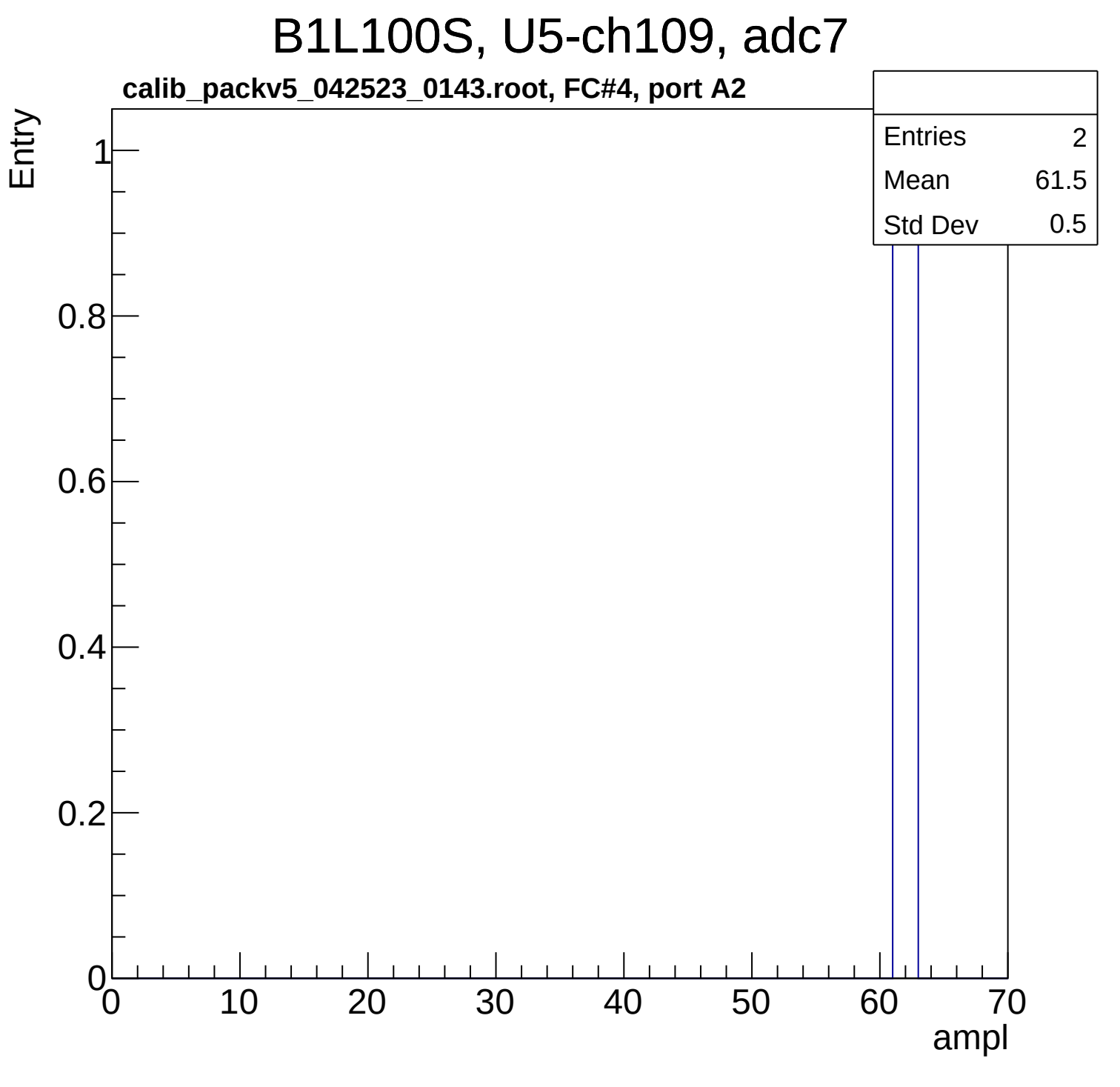

B1L100S, U5-ch109, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 9
Mean 60.44
Std Dev 2.006
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L100S, U5-ch109, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 61.5
Std Dev 0.5
Entry
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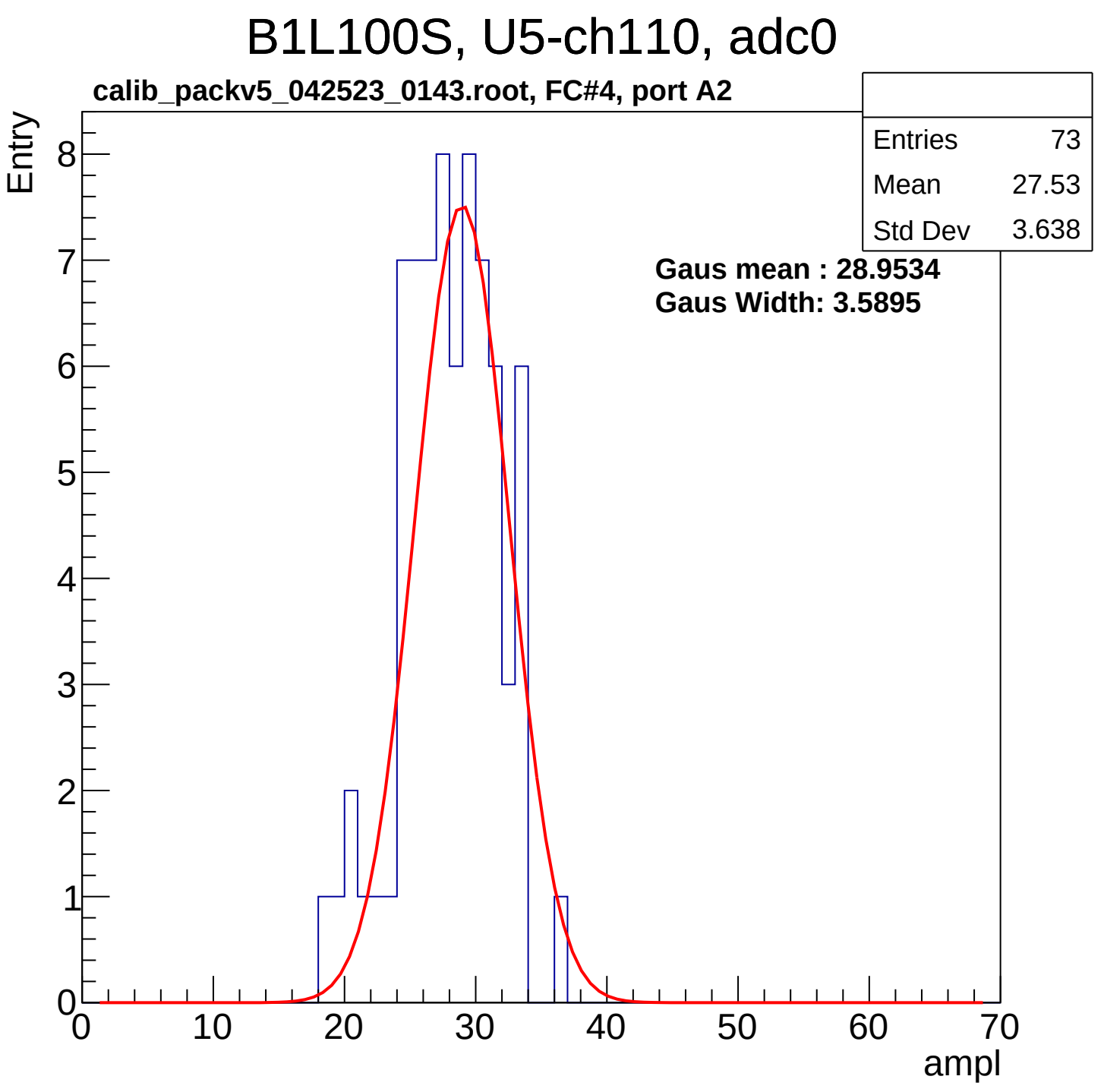
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch110, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 27.53
Std Dev 3.638
Gaus mean : 28.9534
Gaus Width: 3.5895
Entry
ampl
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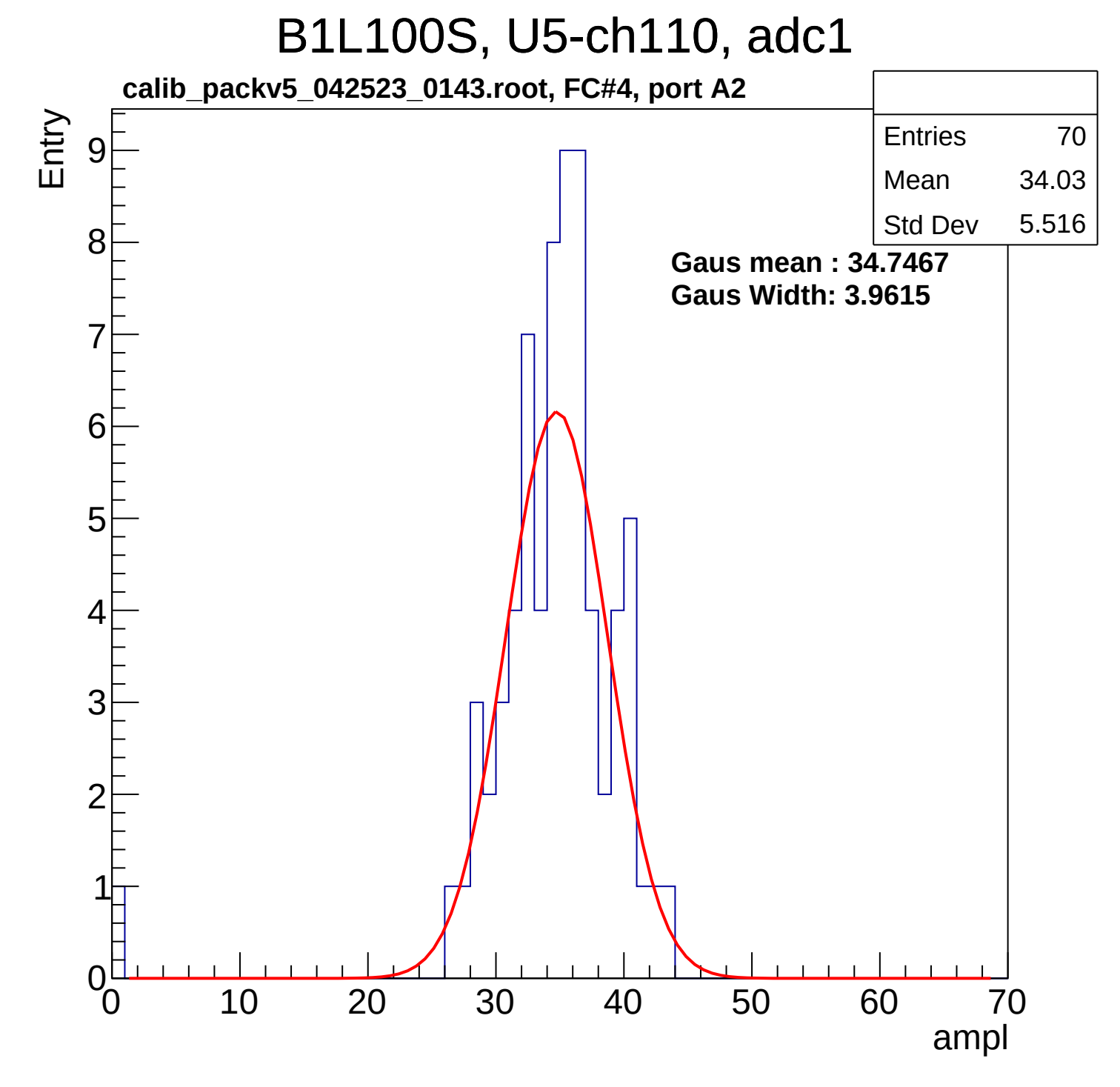
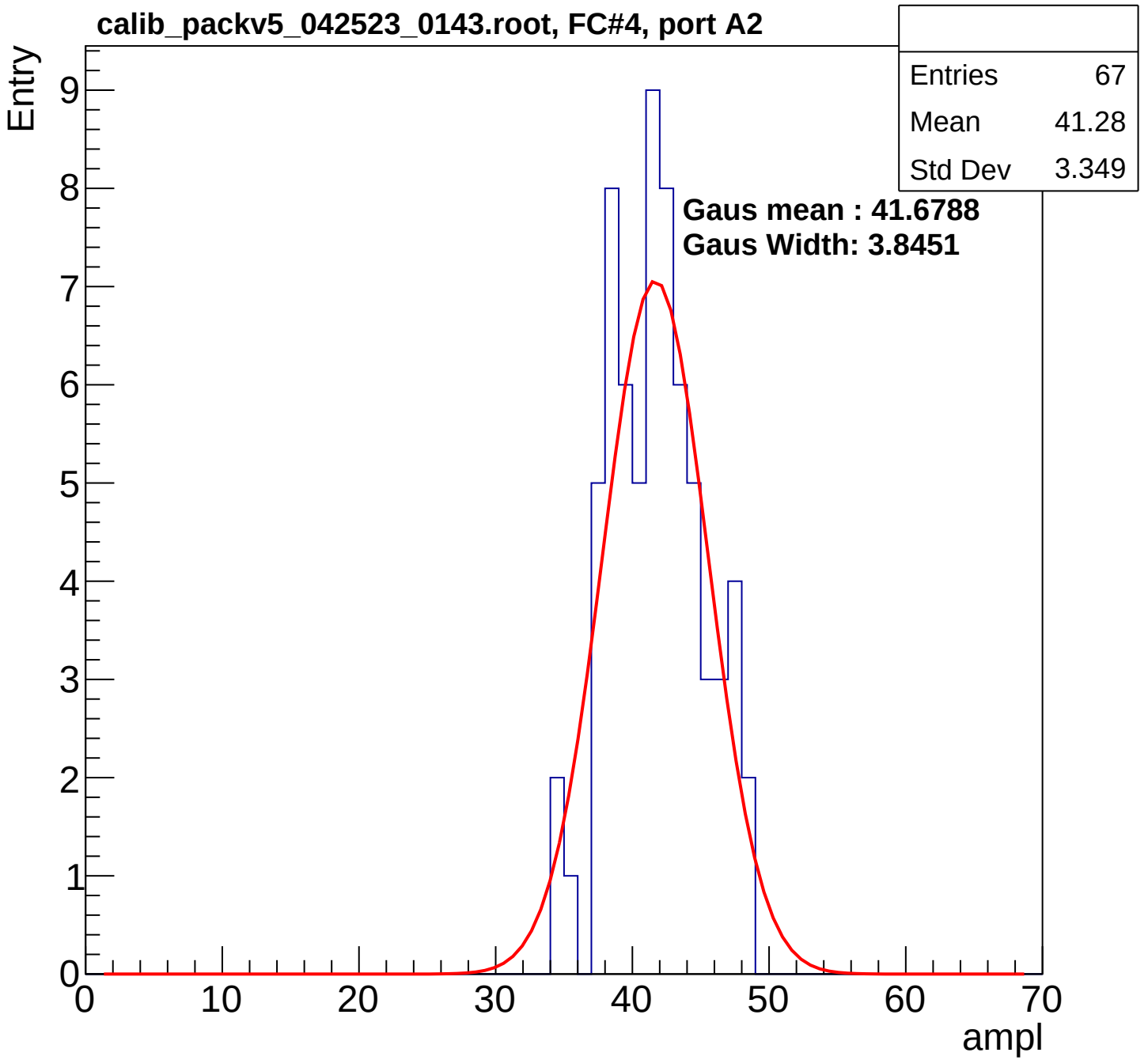
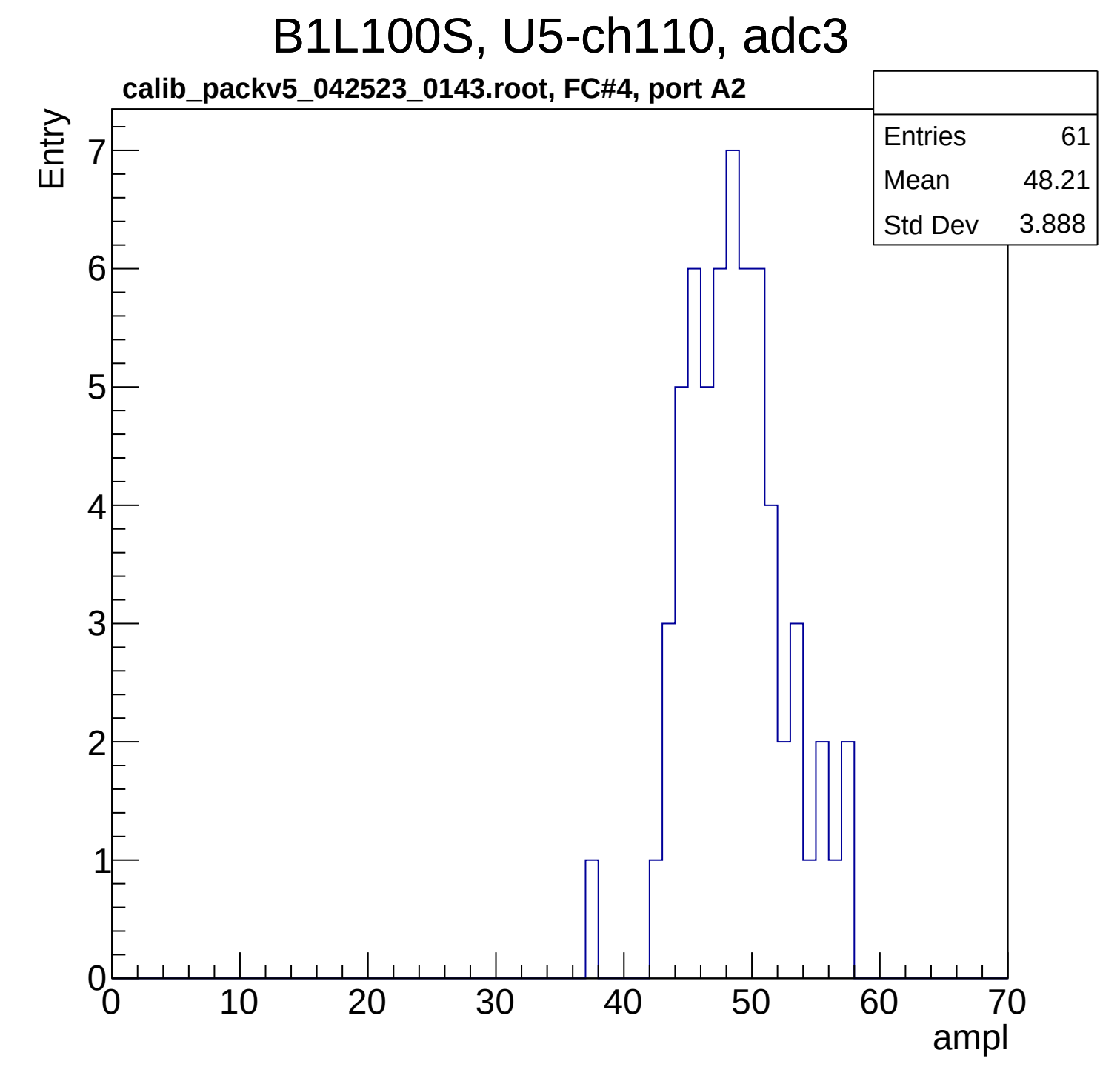
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch110, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 34.03
Std Dev 5.516
Gaus mean : 34.7467
Gaus Width: 3.9615
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch110, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 41.28
Std Dev 3.349
Gaus mean : 41.6788
Gaus Width: 3.8451
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch110, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 48.21
Std Dev 3.888
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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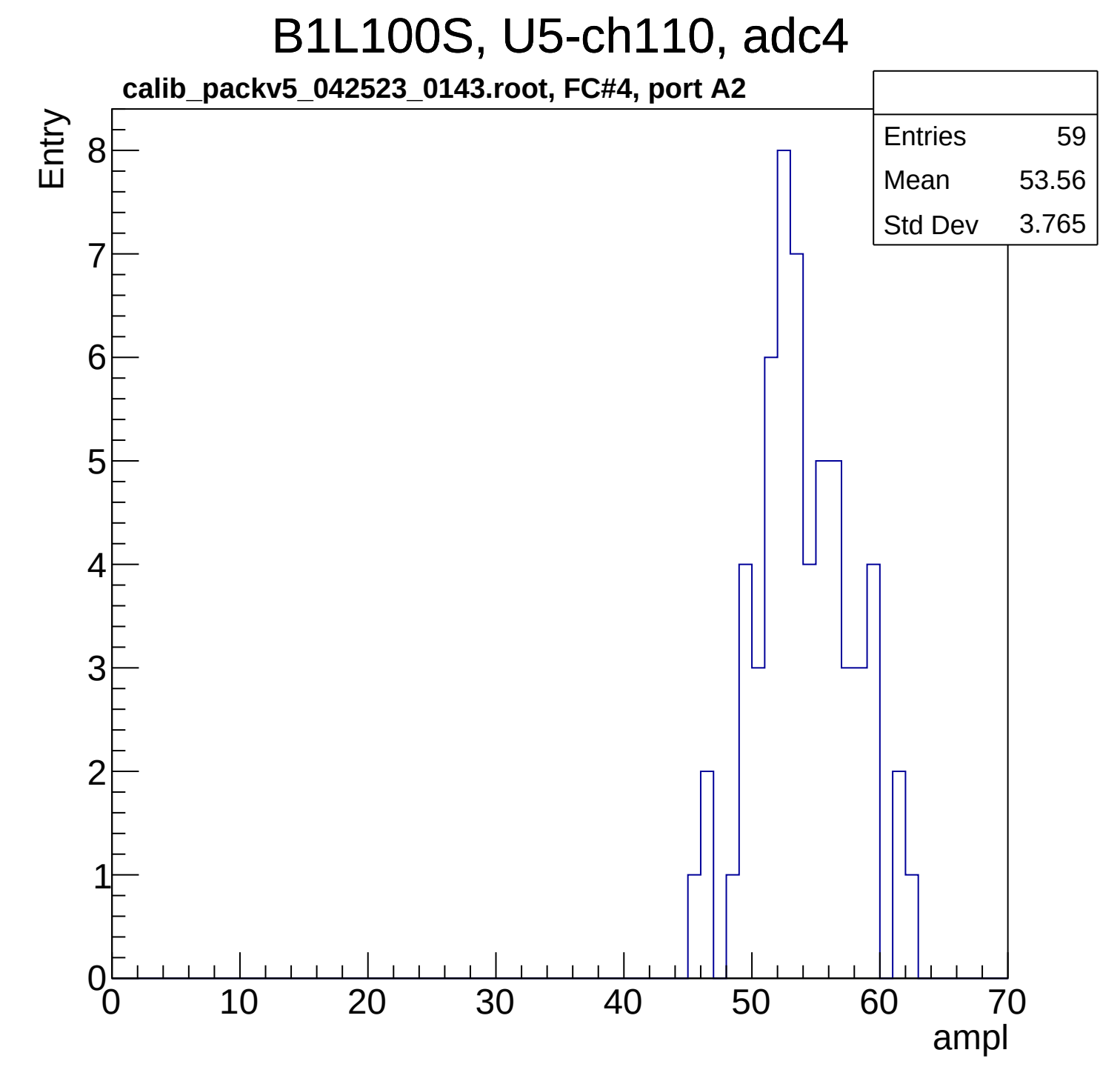
B1L100S, U5-ch110, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 53.56
Std Dev 3.765
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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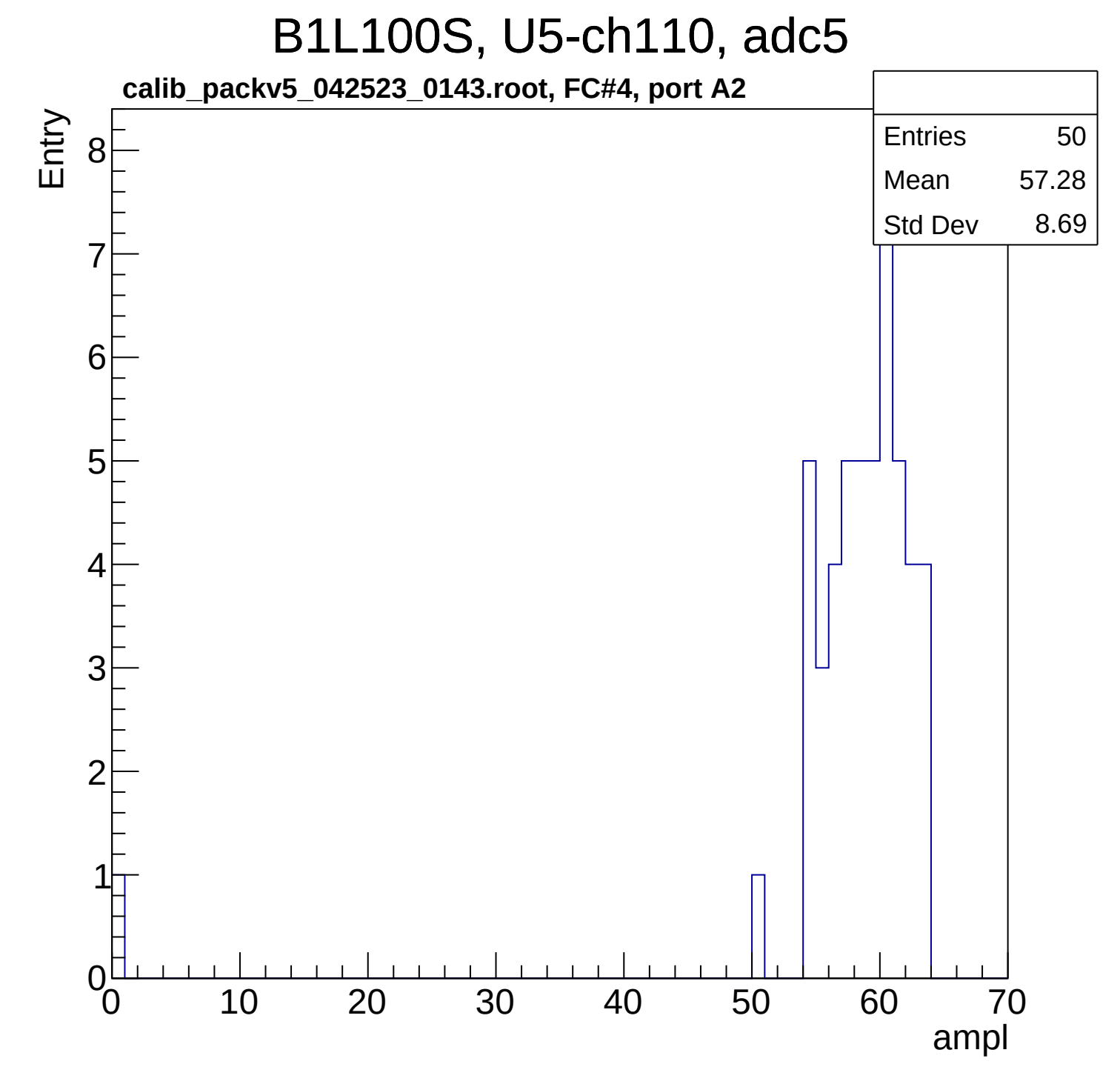
B1L100S, U5-ch110, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 57.28
Std Dev 8.69
Entry
ampl
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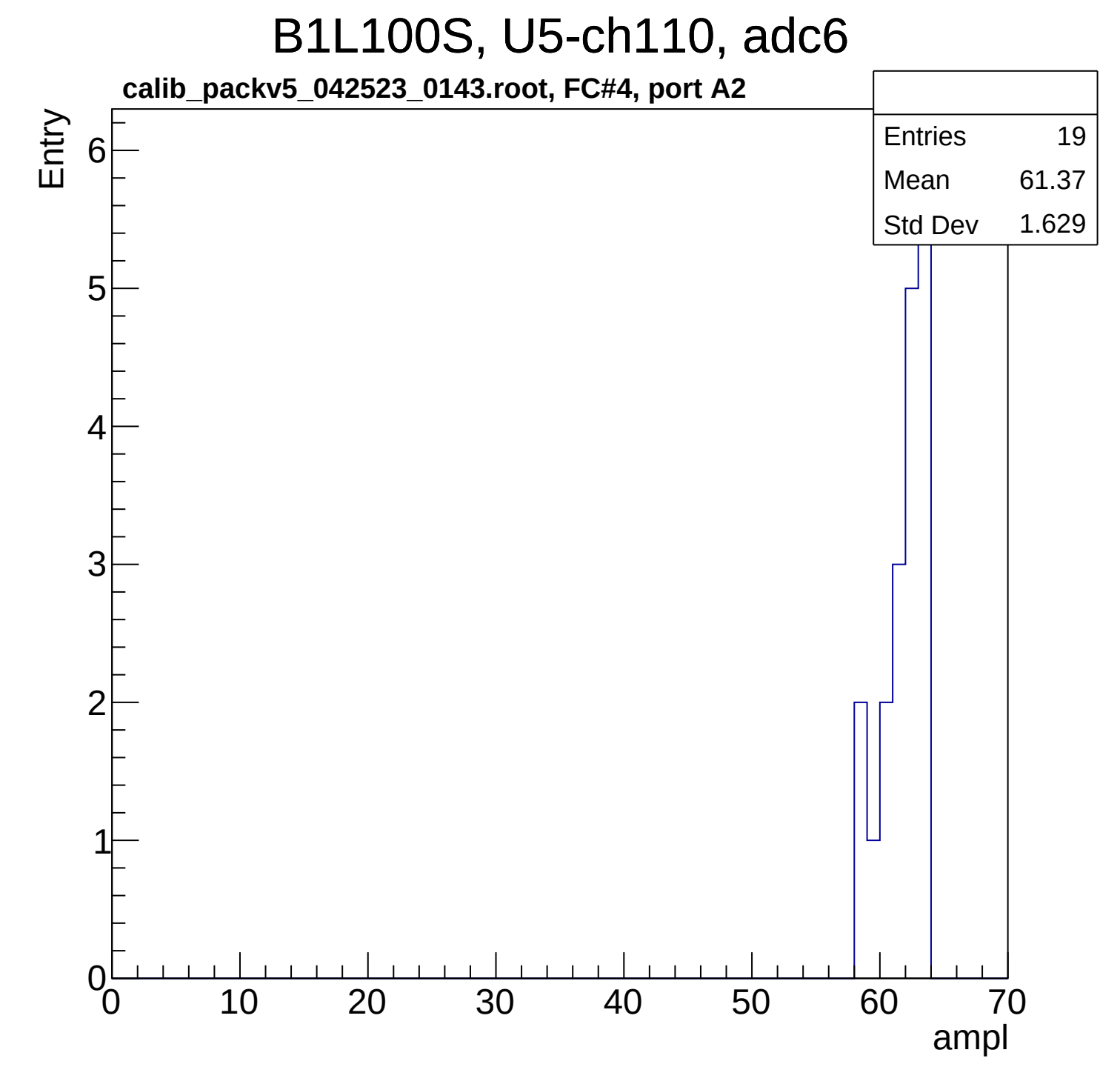
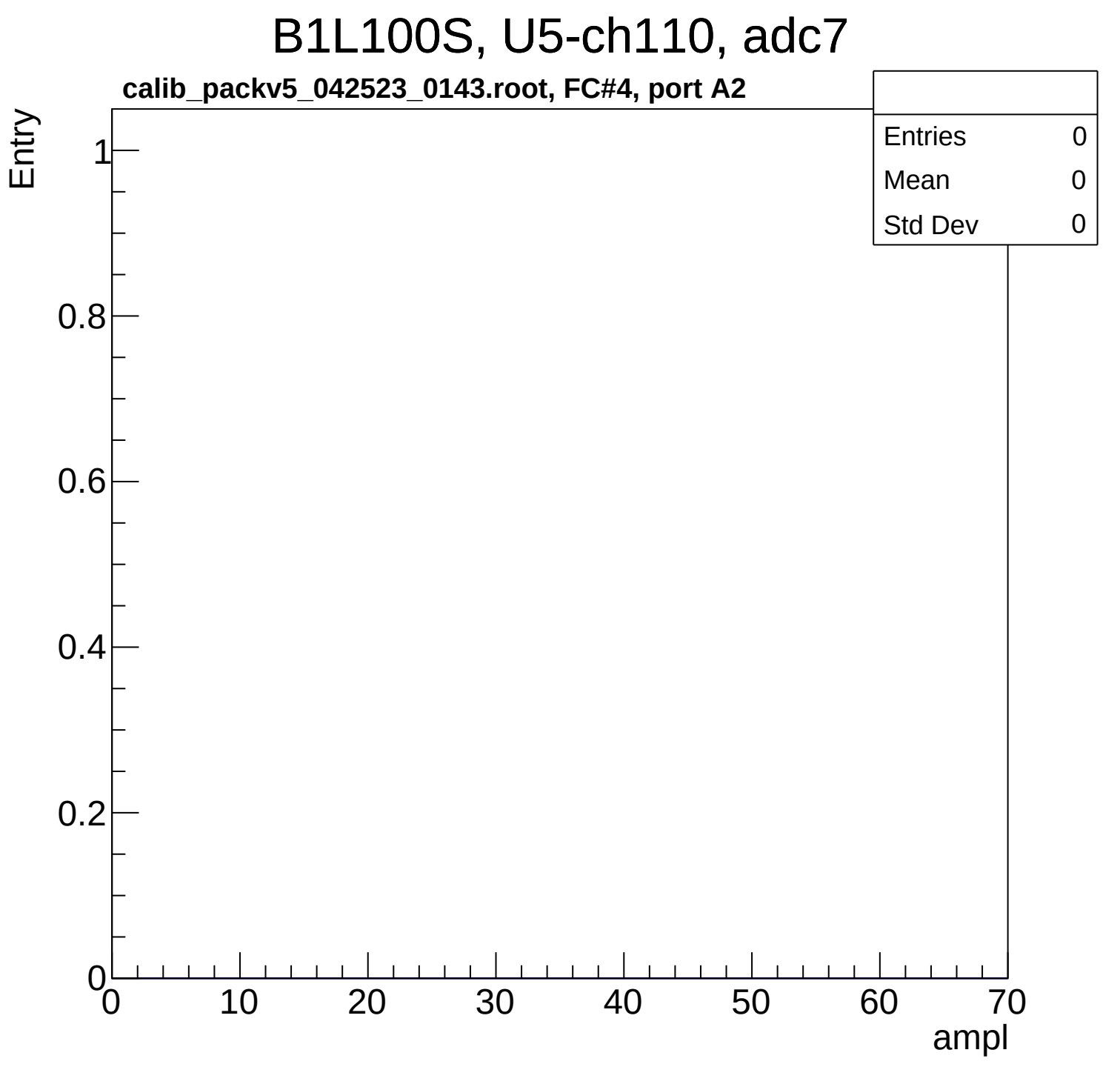
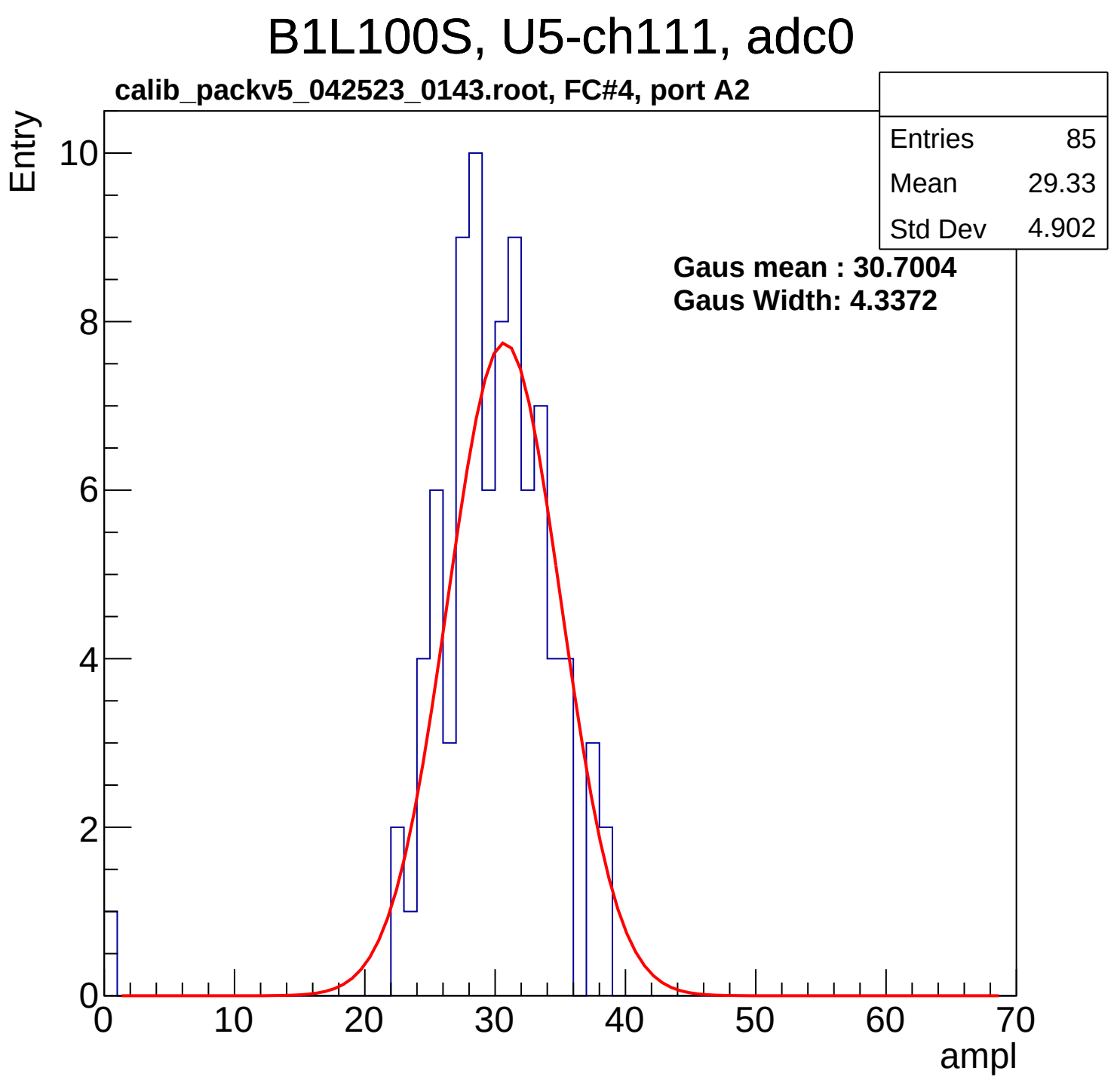
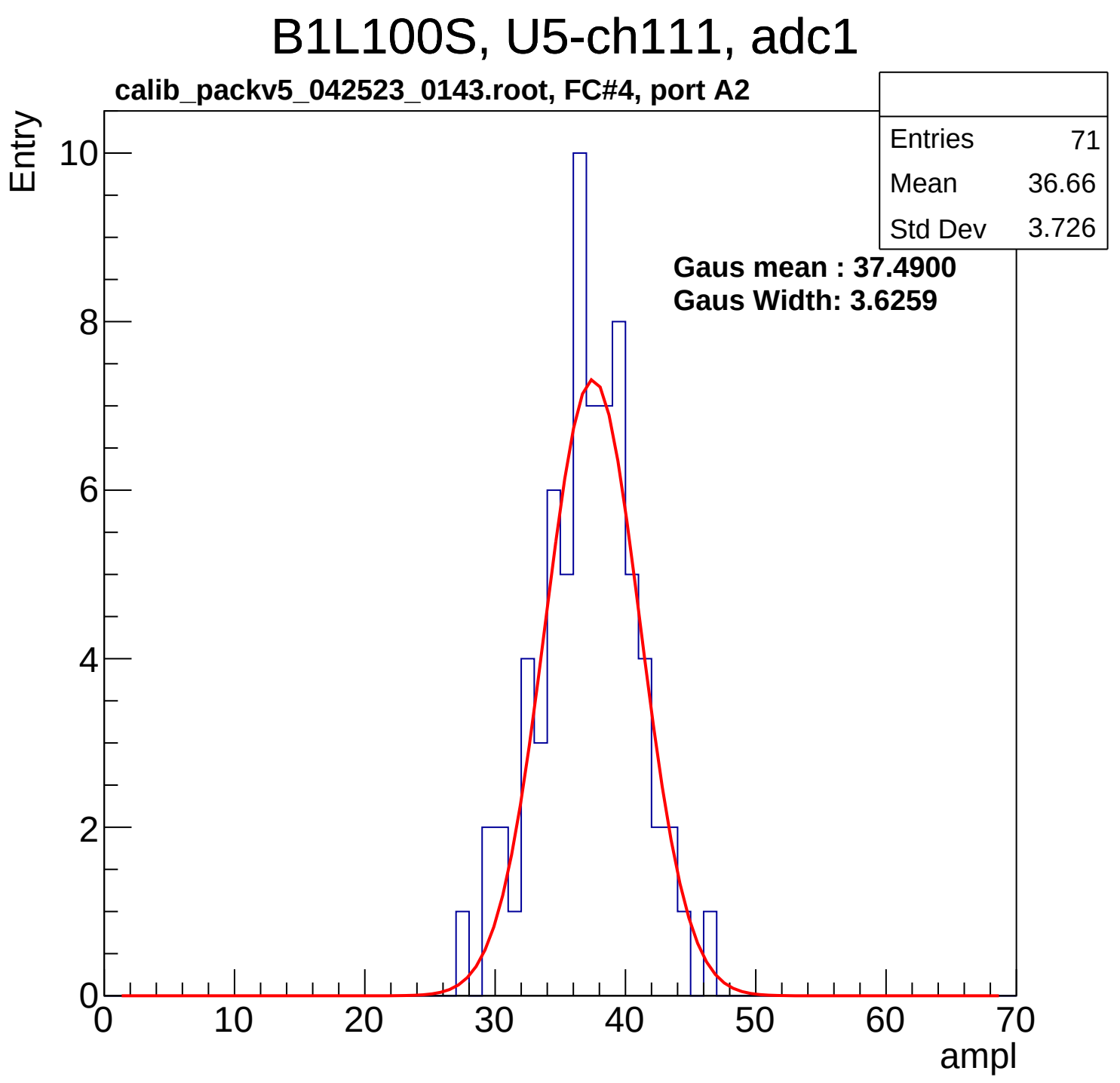
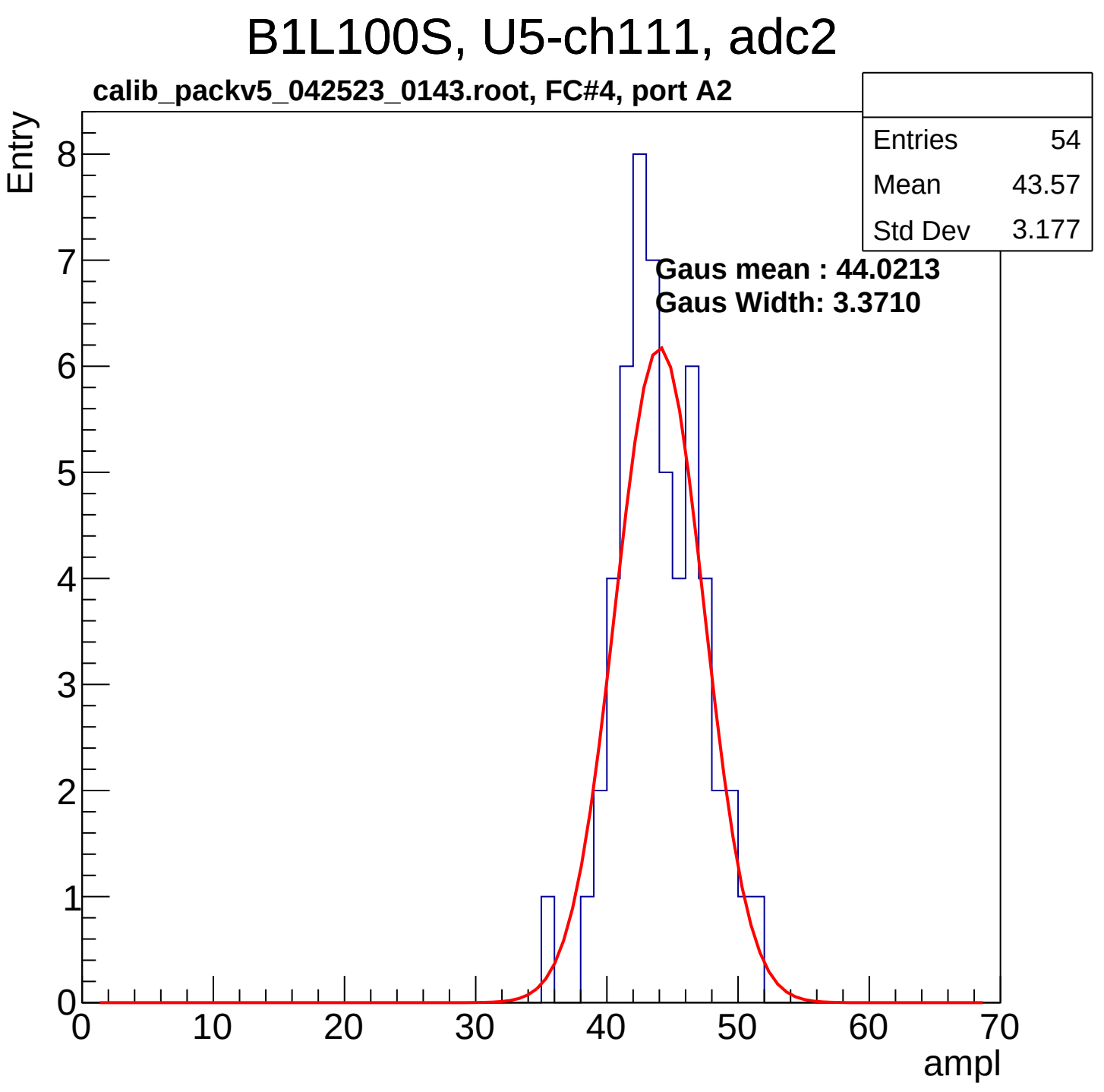
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch110, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 19
Mean 61.37
Std Dev 1.629
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L100S, U5-ch110, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch111, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 85
Mean 29.33
Std Dev 4.902
Gaus mean : 30.7004
Gaus Width: 4.3372
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch111, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 36.66
Std Dev 3.726
Gaus mean : 37.4900
Gaus Width: 3.6259
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch111, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 43.57
Std Dev 3.177
Gaus mean : 44.0213
Gaus Width: 3.3710
Entry
ampl
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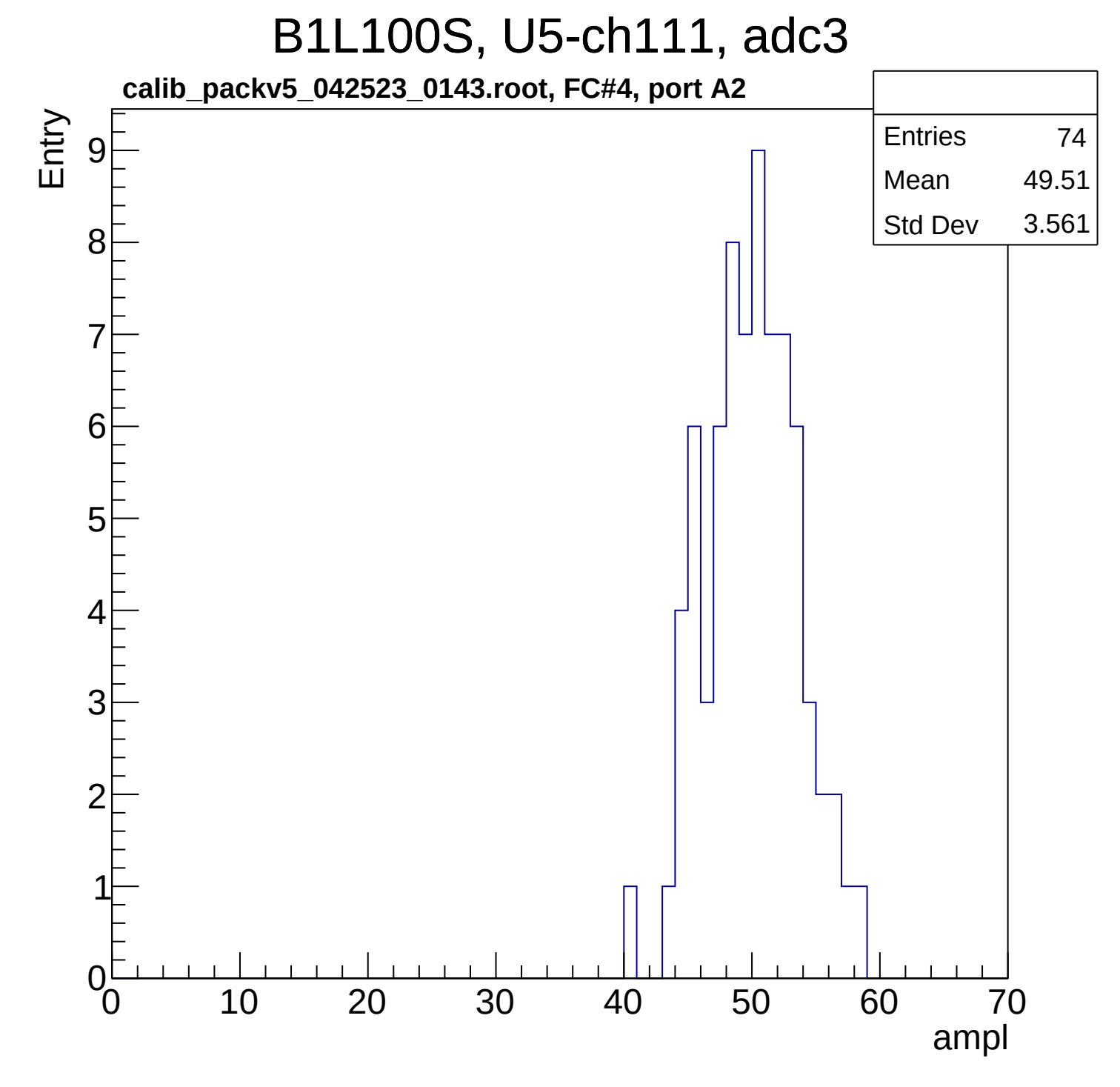
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch111, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 74
Mean 49.51
Std Dev 3.561
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
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40
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60
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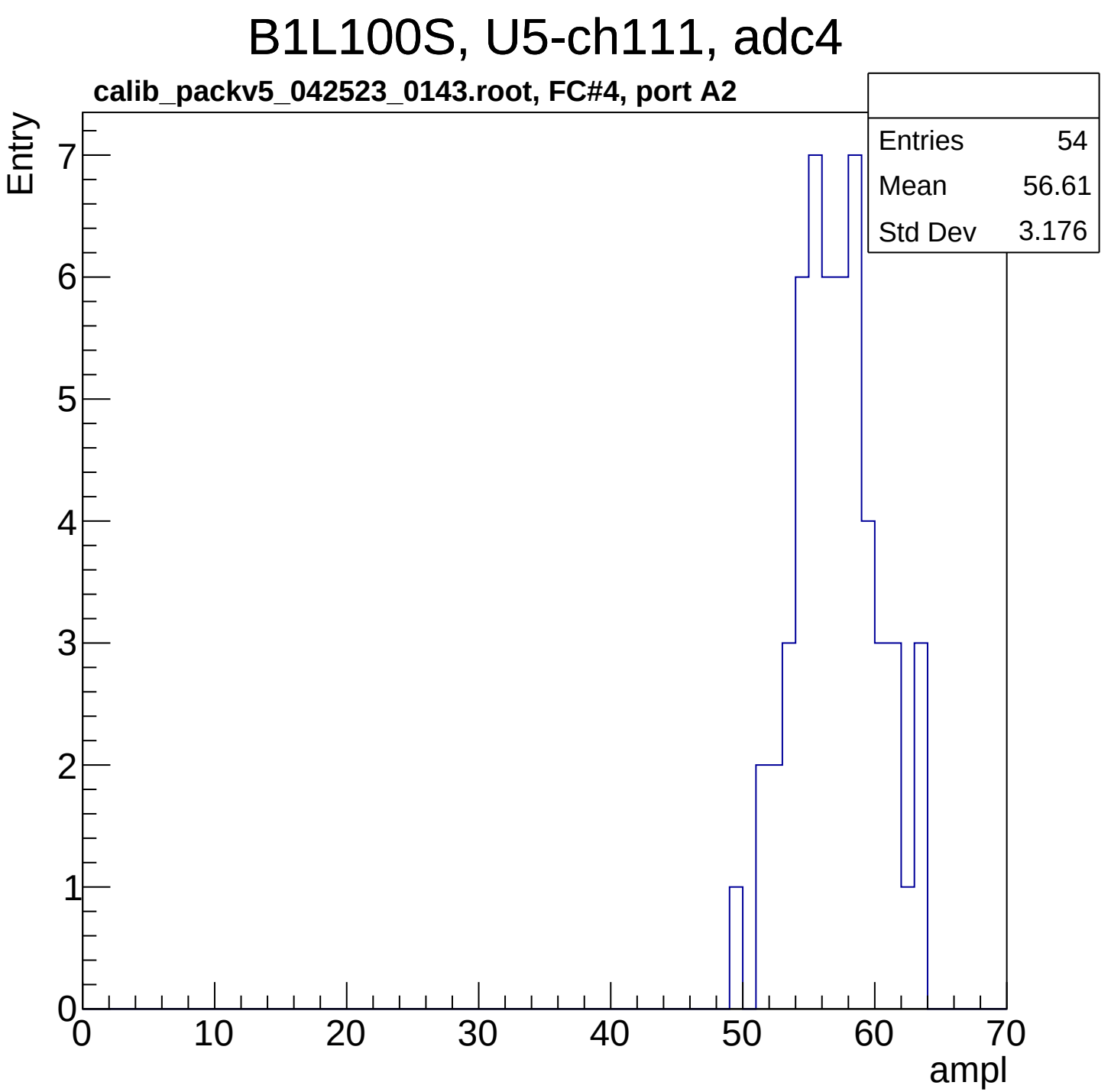
B1L100S, U5-ch111, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 56.61
Std Dev 3.176
Entry
ampl
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2
3
4
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0
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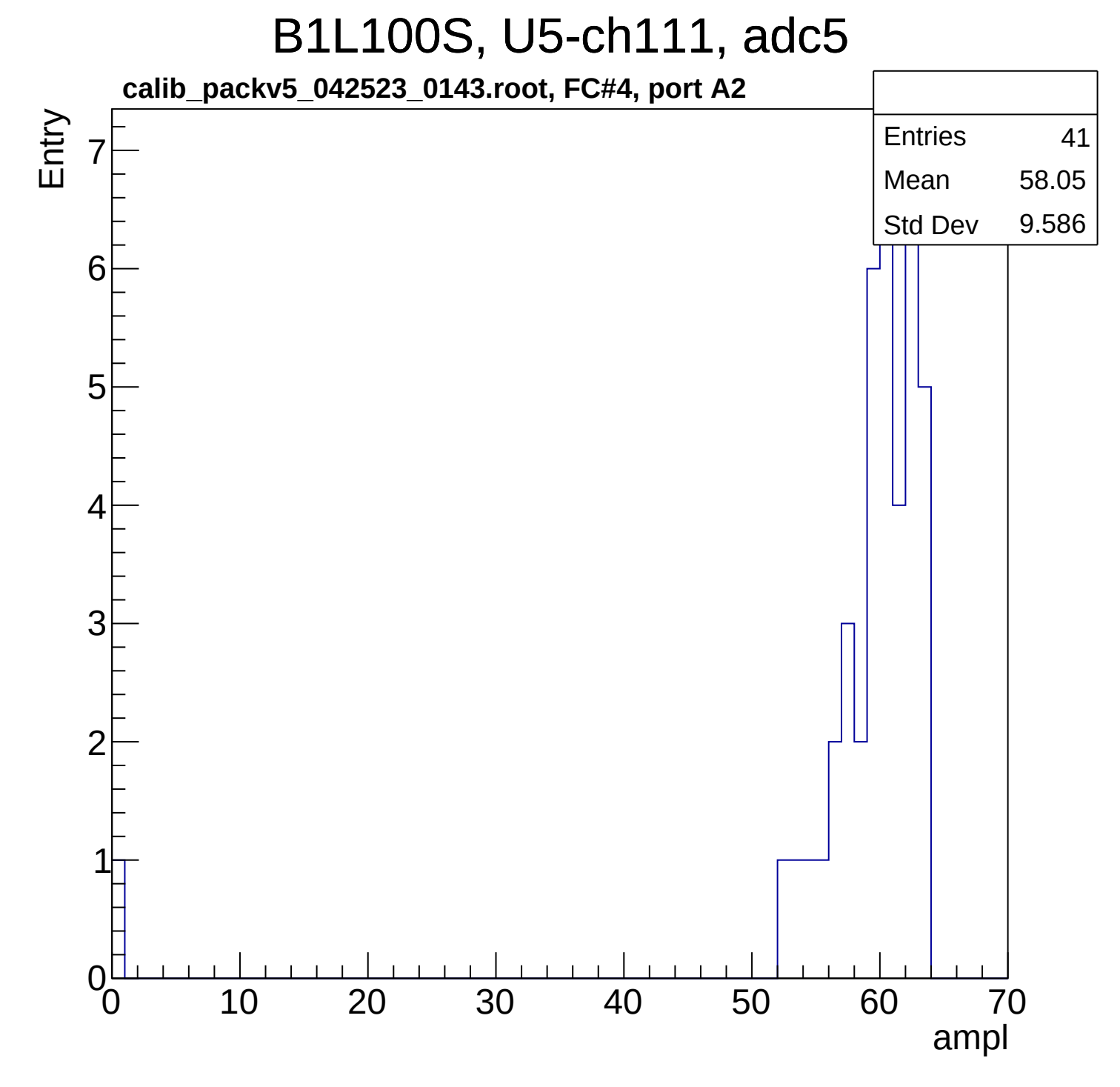
B1L100S, U5-ch111, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 41
Mean 58.05
Std Dev 9.586
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
50
60
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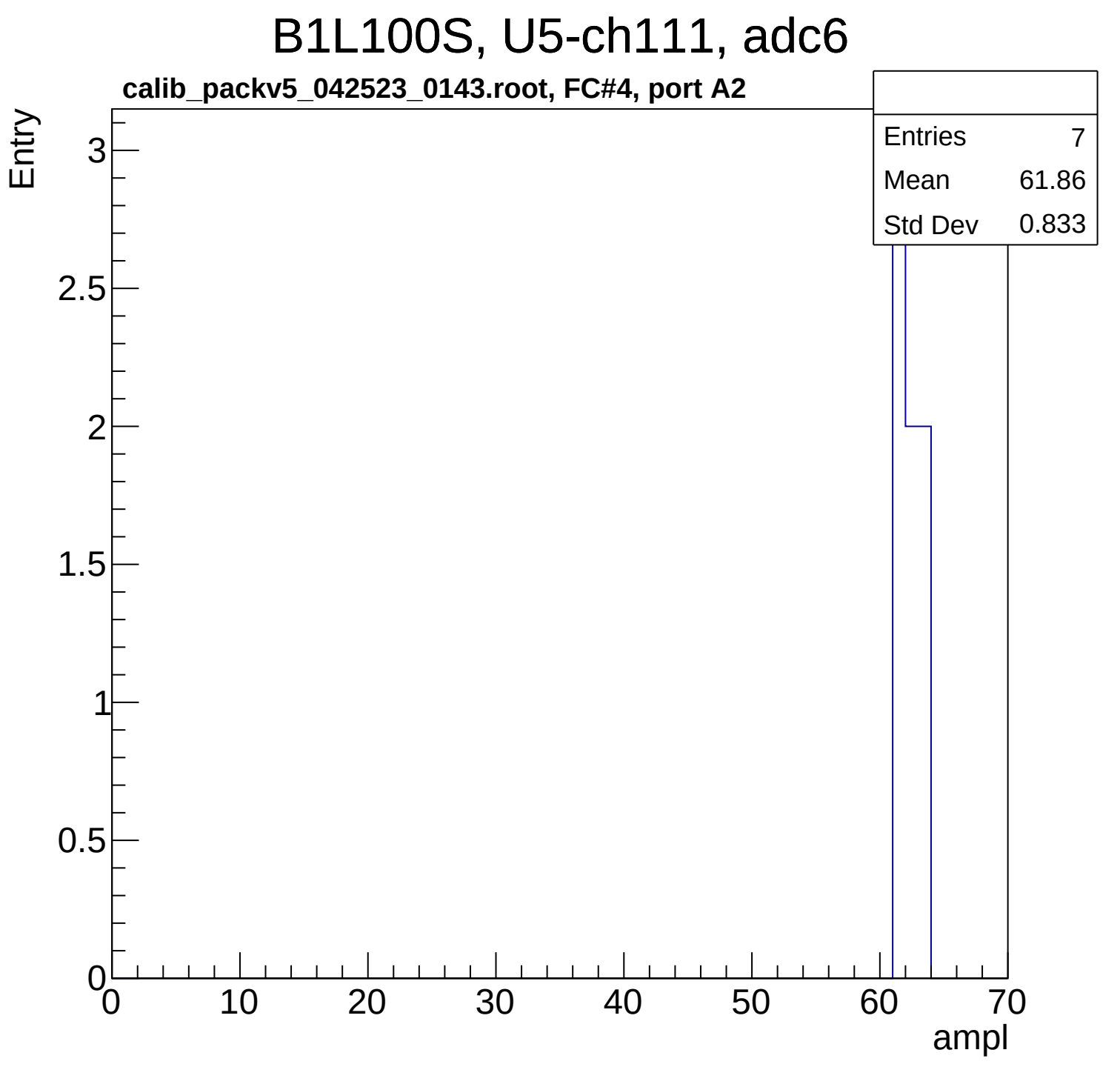
B1L100S, U5-ch111, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 7
Mean 61.86
Std Dev 0.833
Entry
ampl
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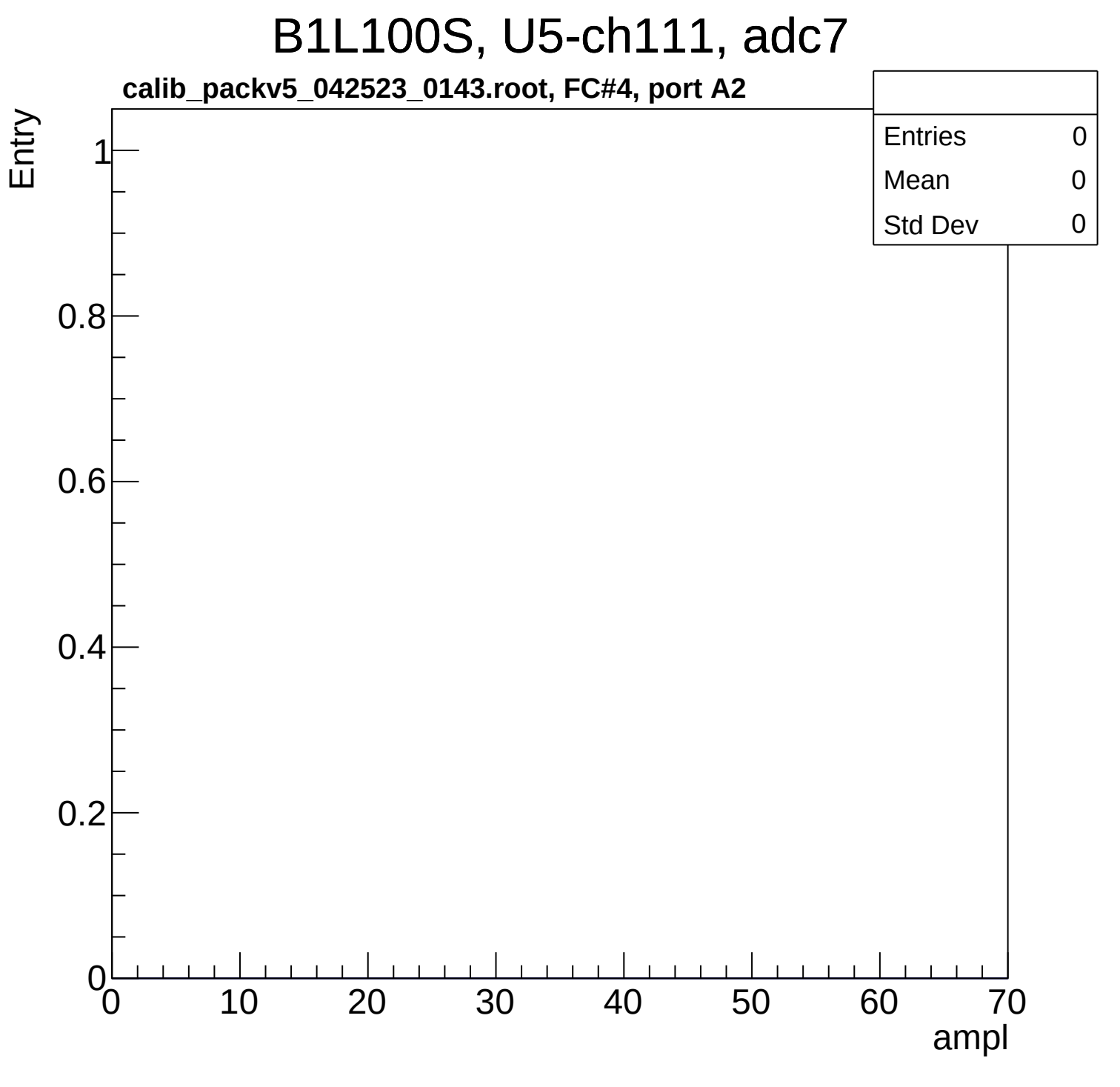
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L100S, U5-ch111, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
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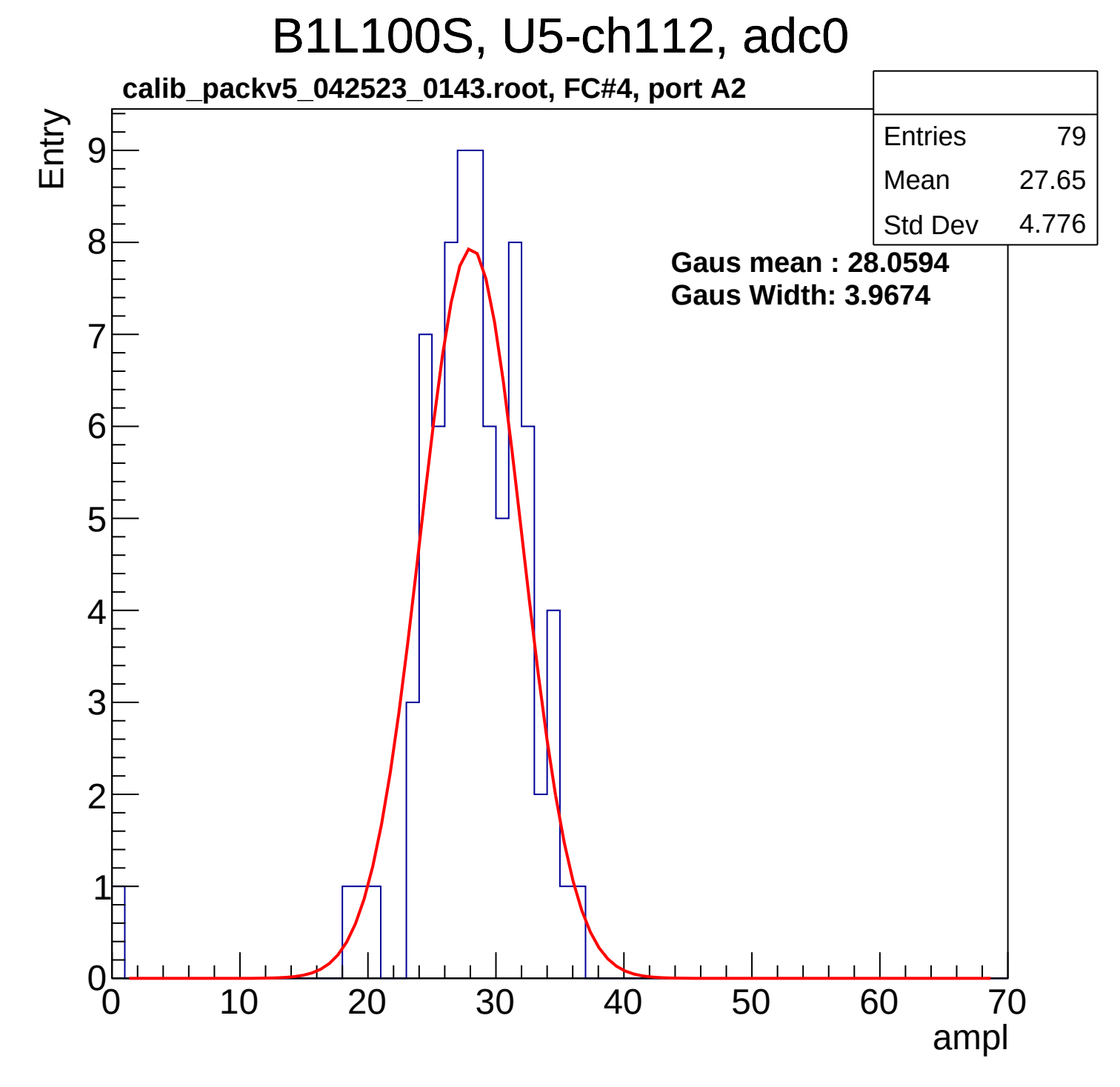
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch112, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 79
Mean 27.65
Std Dev 4.776
Gaus mean : 28.0594
Gaus Width: 3.9674
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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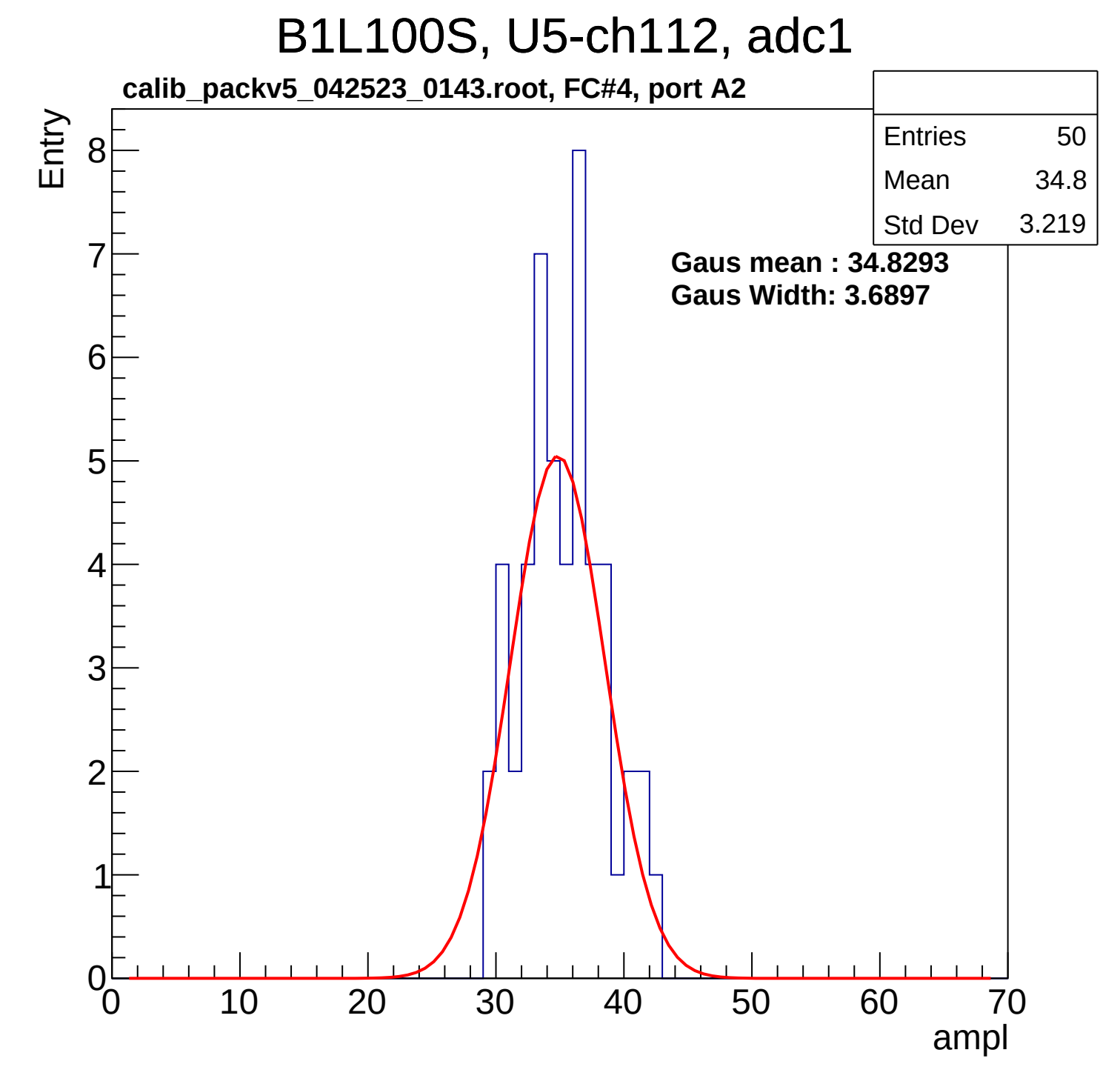
B1L100S, U5-ch112, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 34.8
Std Dev 3.219
Gaus mean : 34.8293
Gaus Width: 3.6897
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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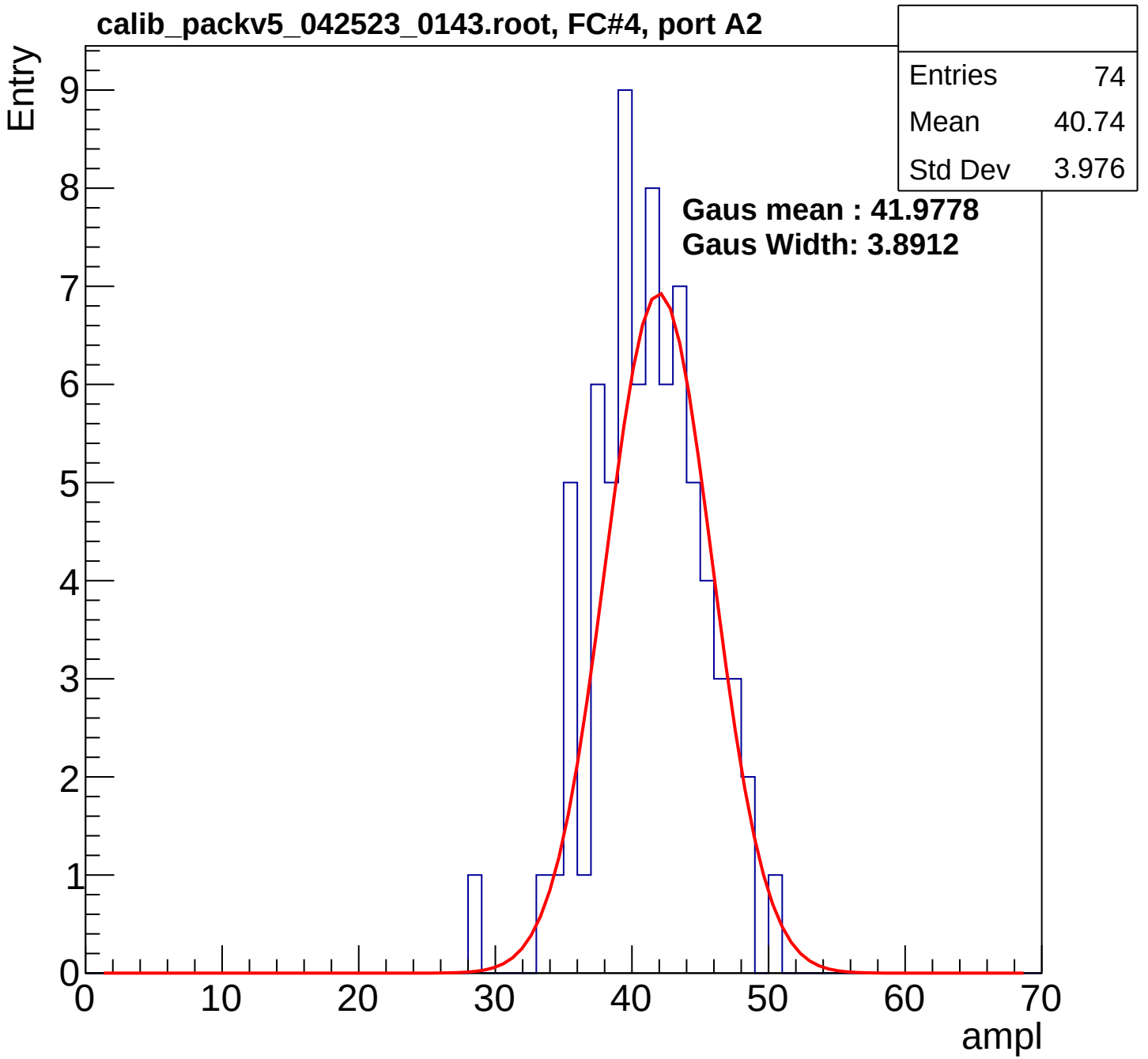
B1L100S, U5-ch112, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 74
Mean 40.74
Std Dev 3.976
Gaus mean : 41.9778
Gaus Width: 3.8912
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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20
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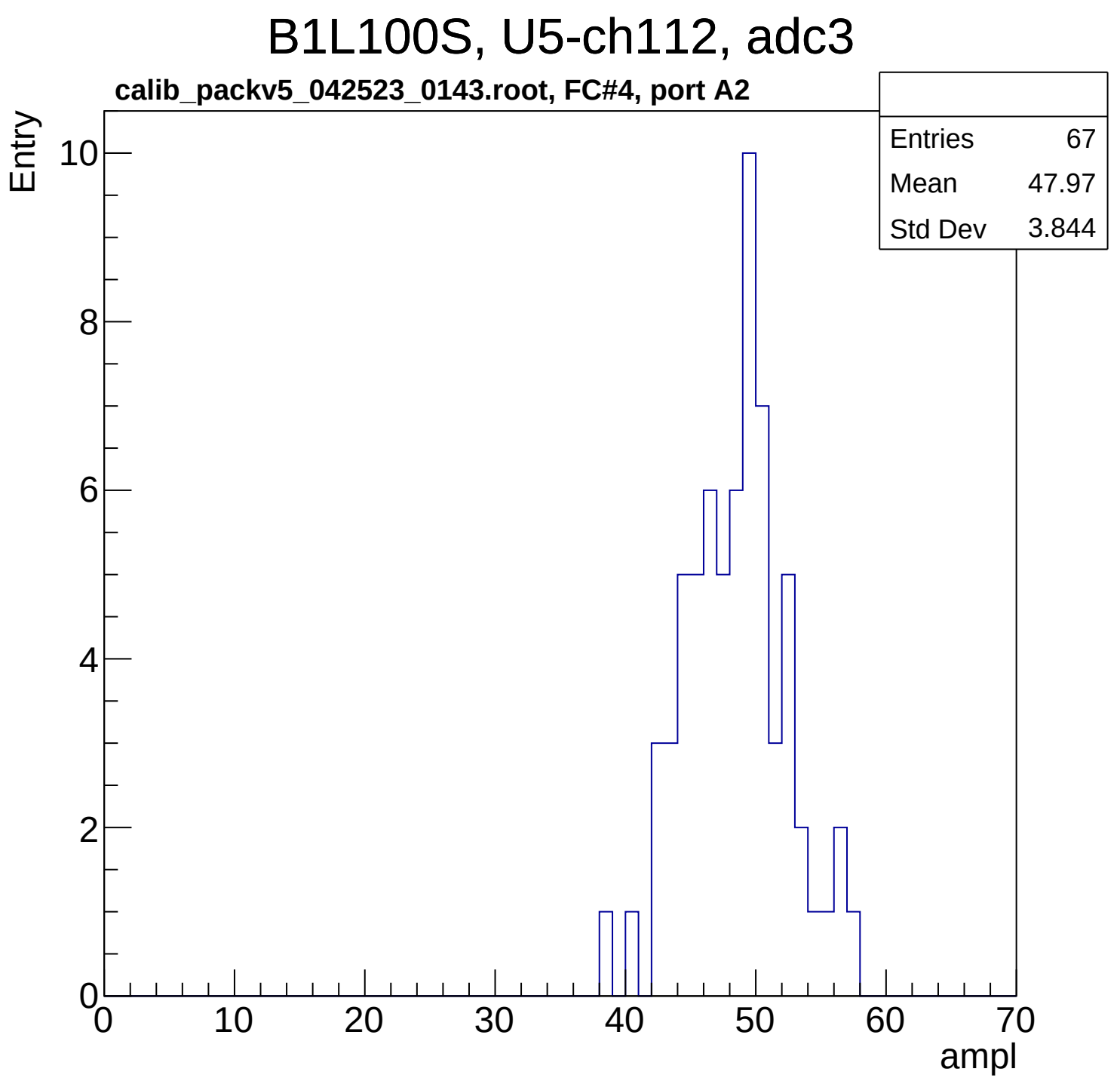
B1L100S, U5-ch112, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 47.97
Std Dev 3.844
Entry
ampl
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2
4
6
8
10
0
10
20
30
40
50
60
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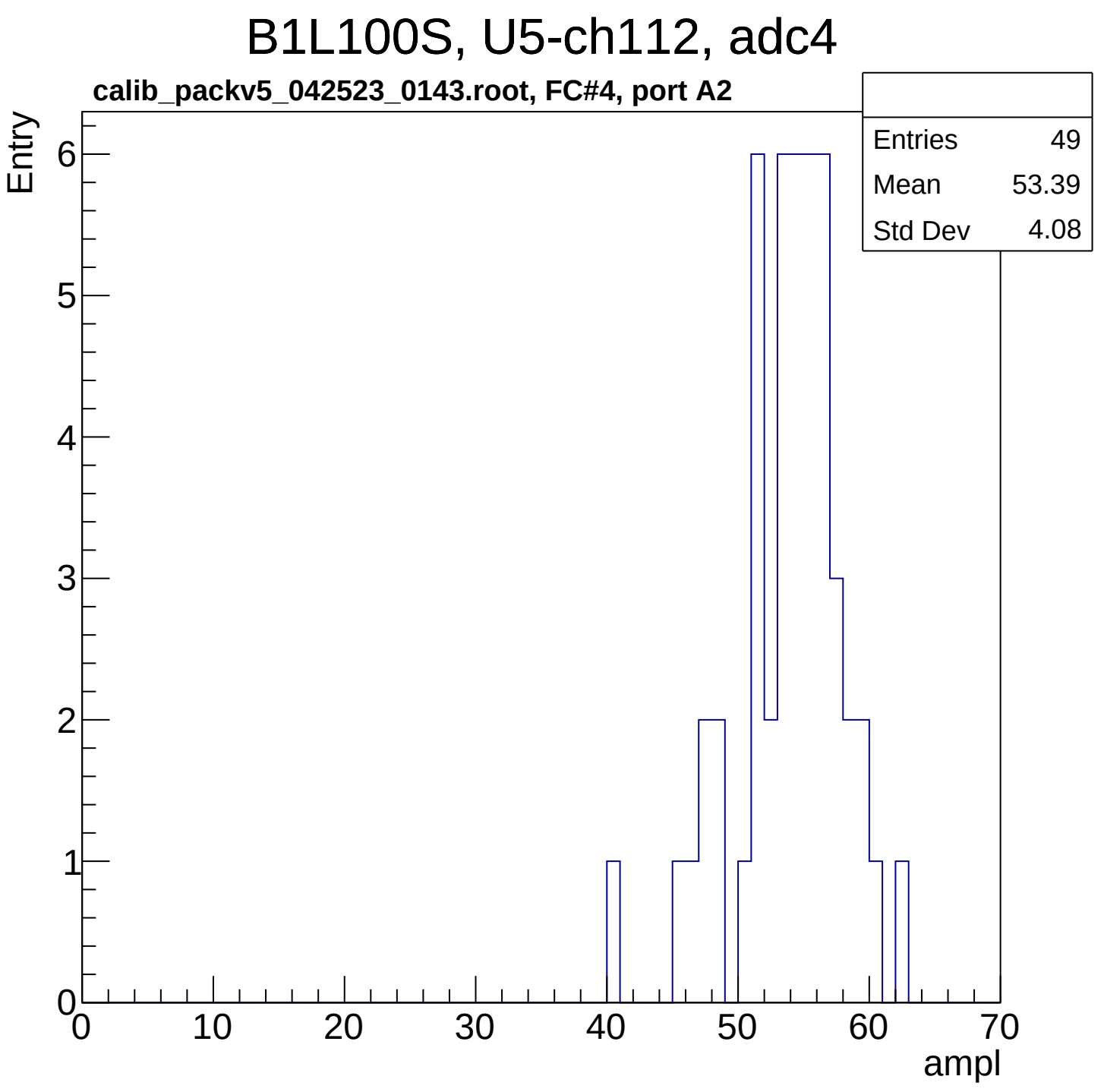
B1L100S, U5-ch112, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 49
Mean 53.39
Std Dev 4.08
Entry
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1
2
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4
5
6
0
10
20
30
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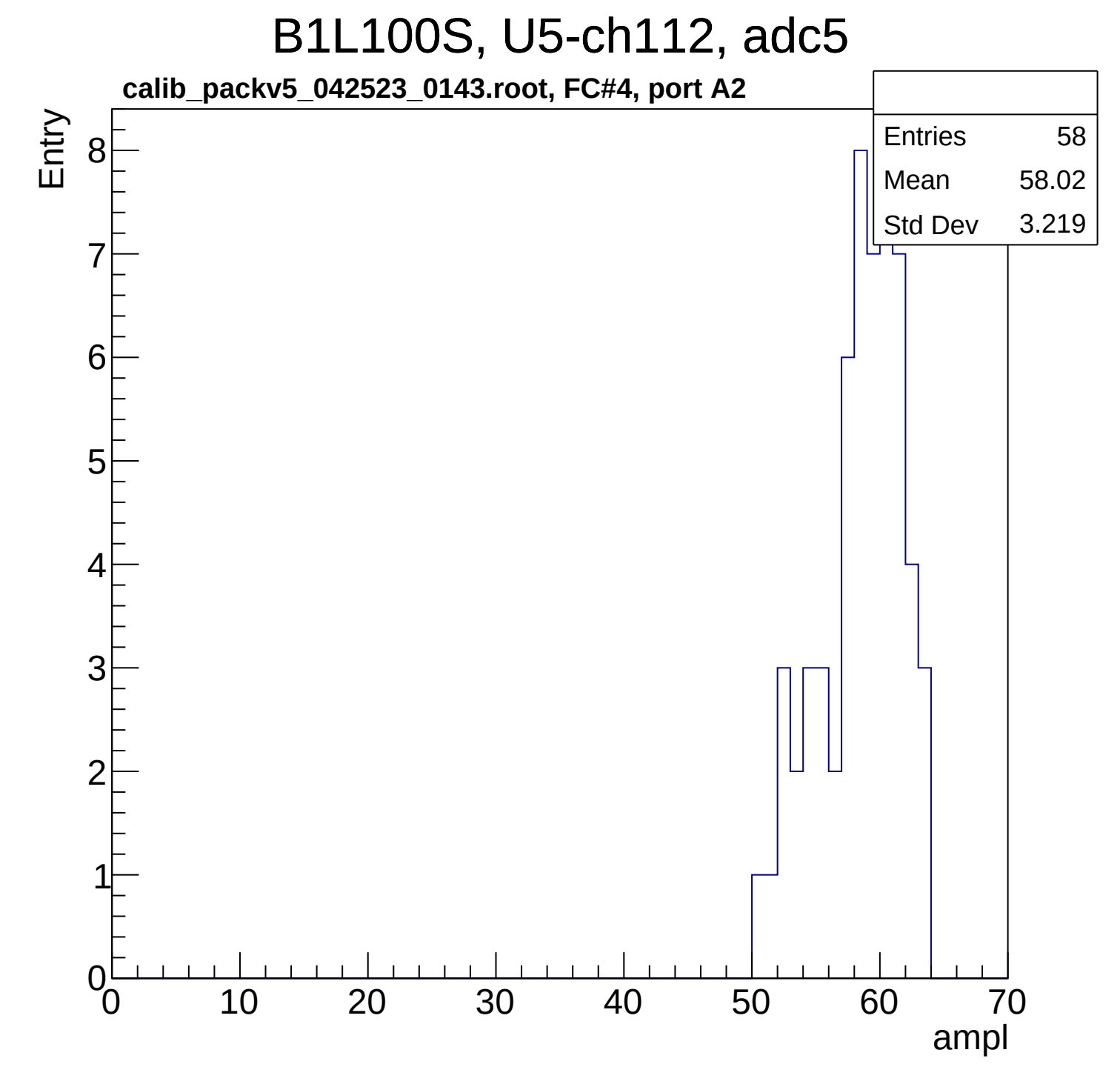
50
60
70
ampl


B1L100S, U5-ch112, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 58.02
Std Dev 3.219
Entry
ampl
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2
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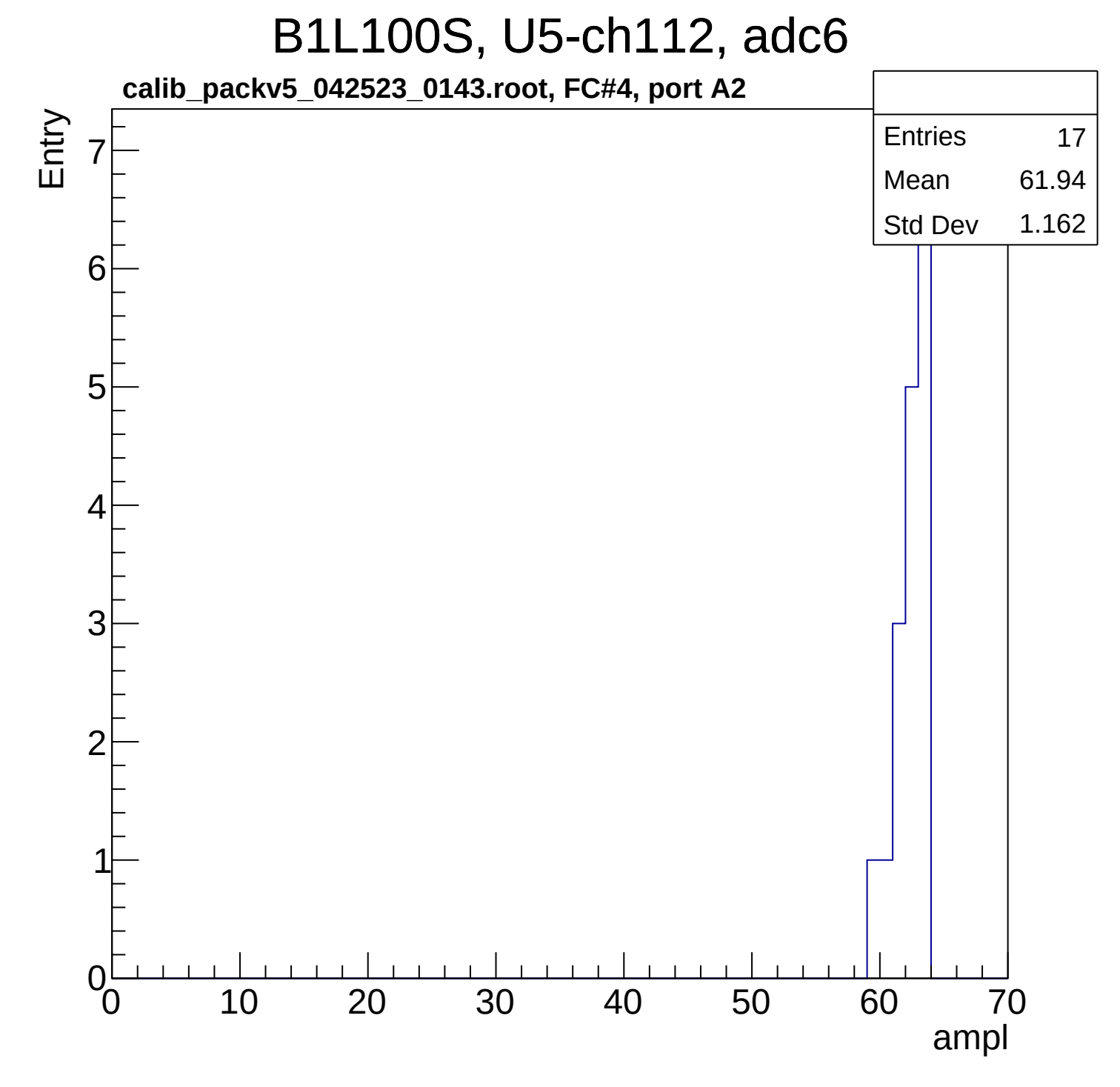
B1L100S, U5-ch112, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 17
Mean 61.94
Std Dev 1.162
Entry
ampl
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40
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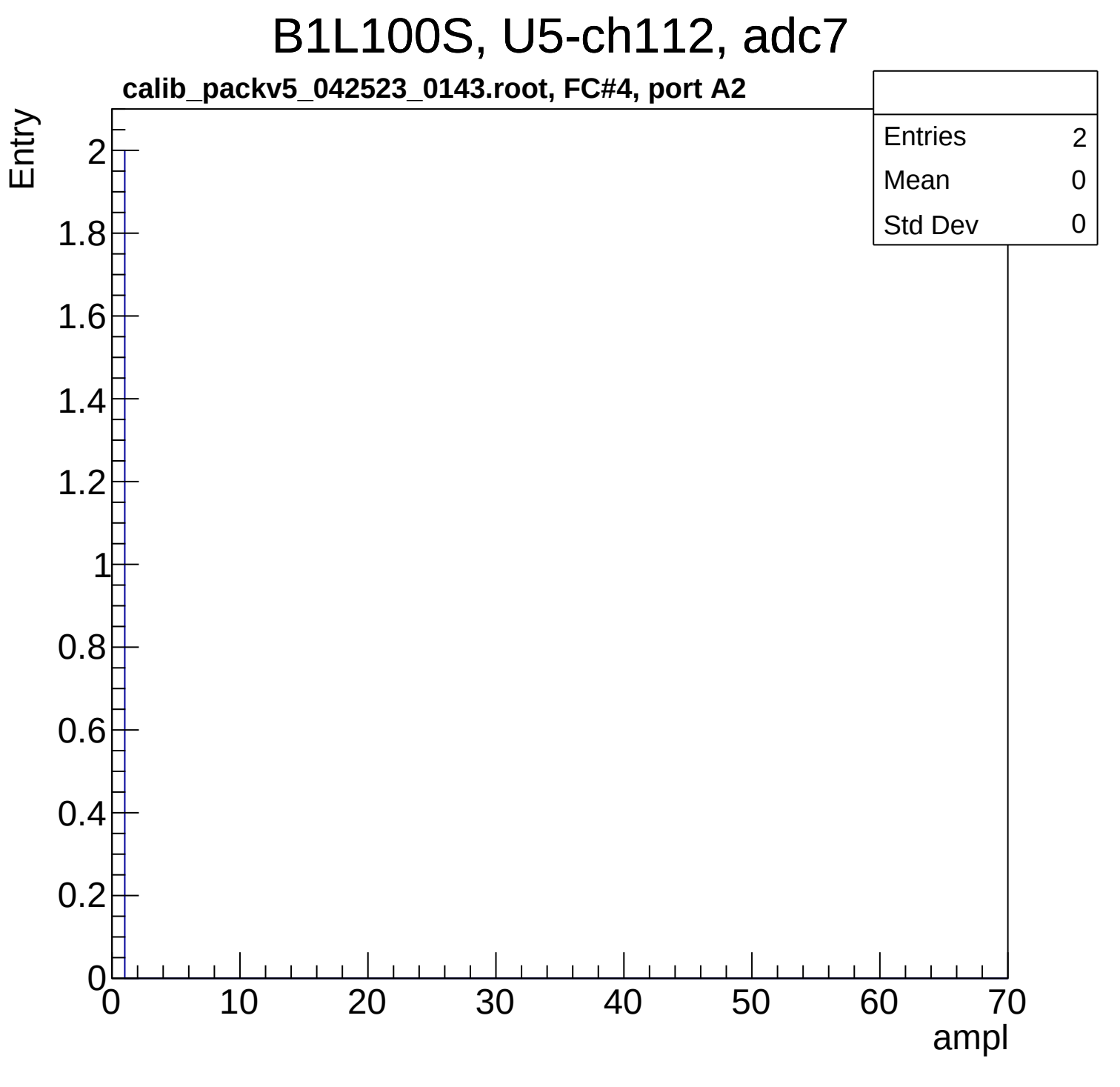
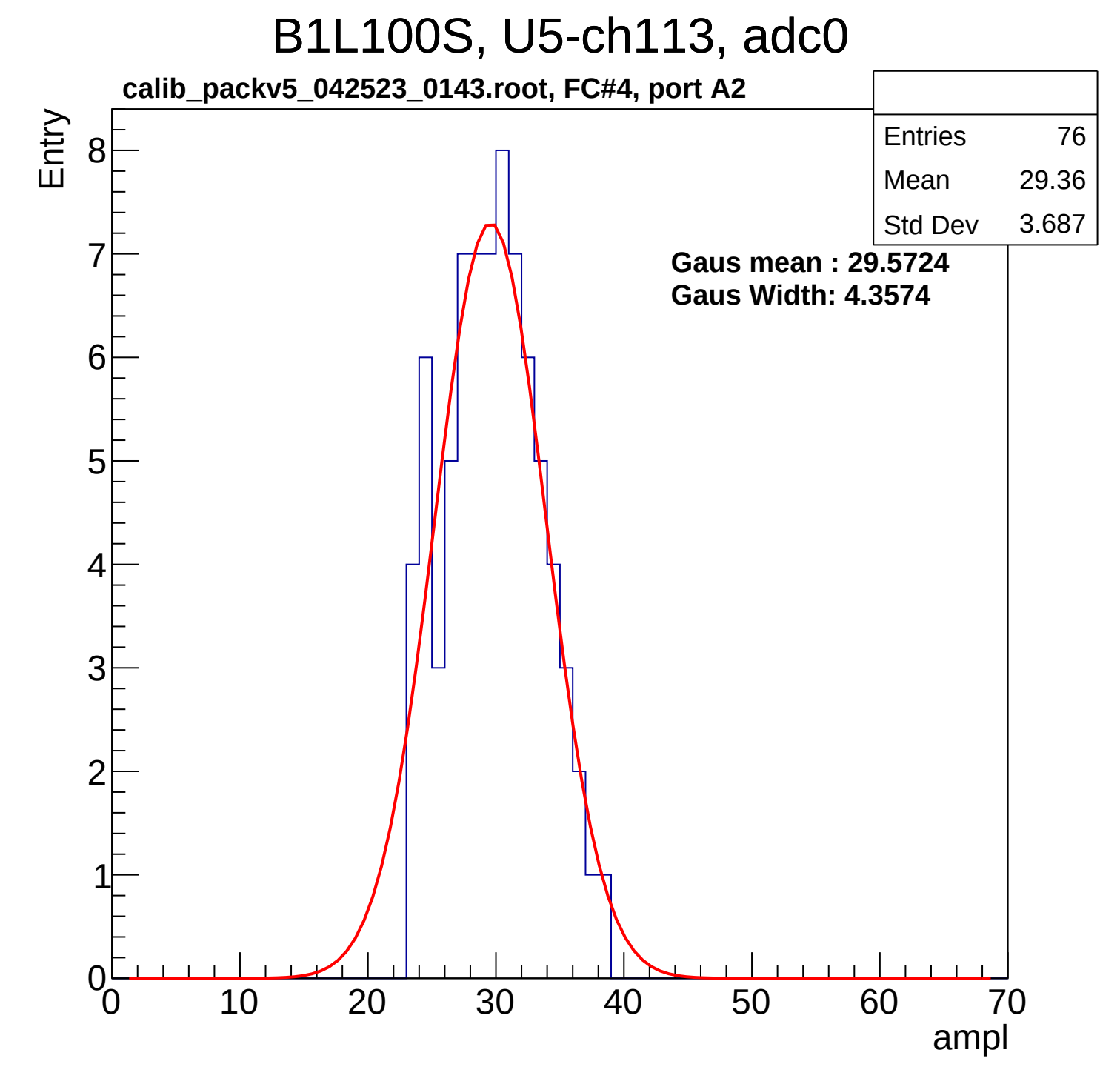
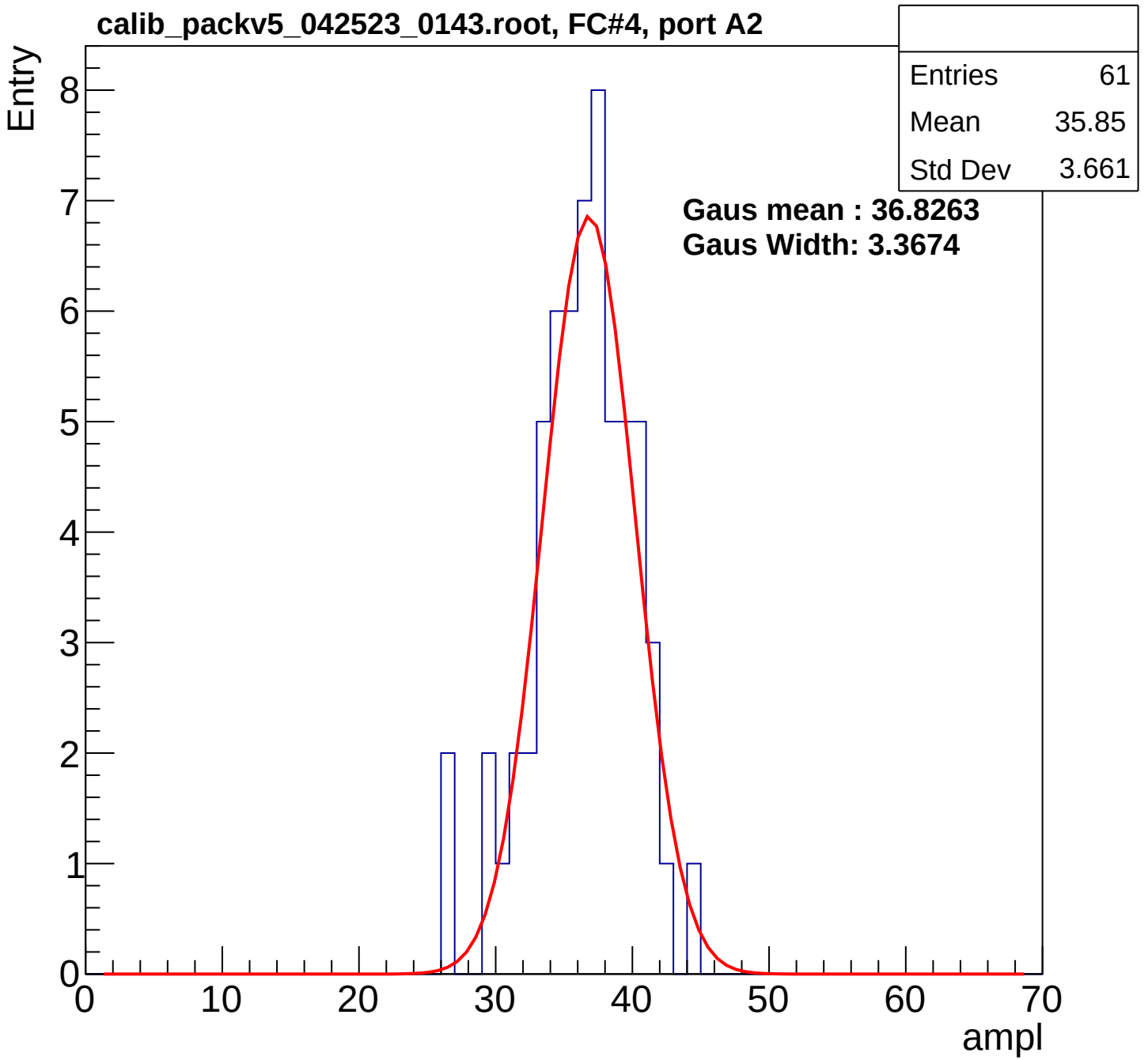
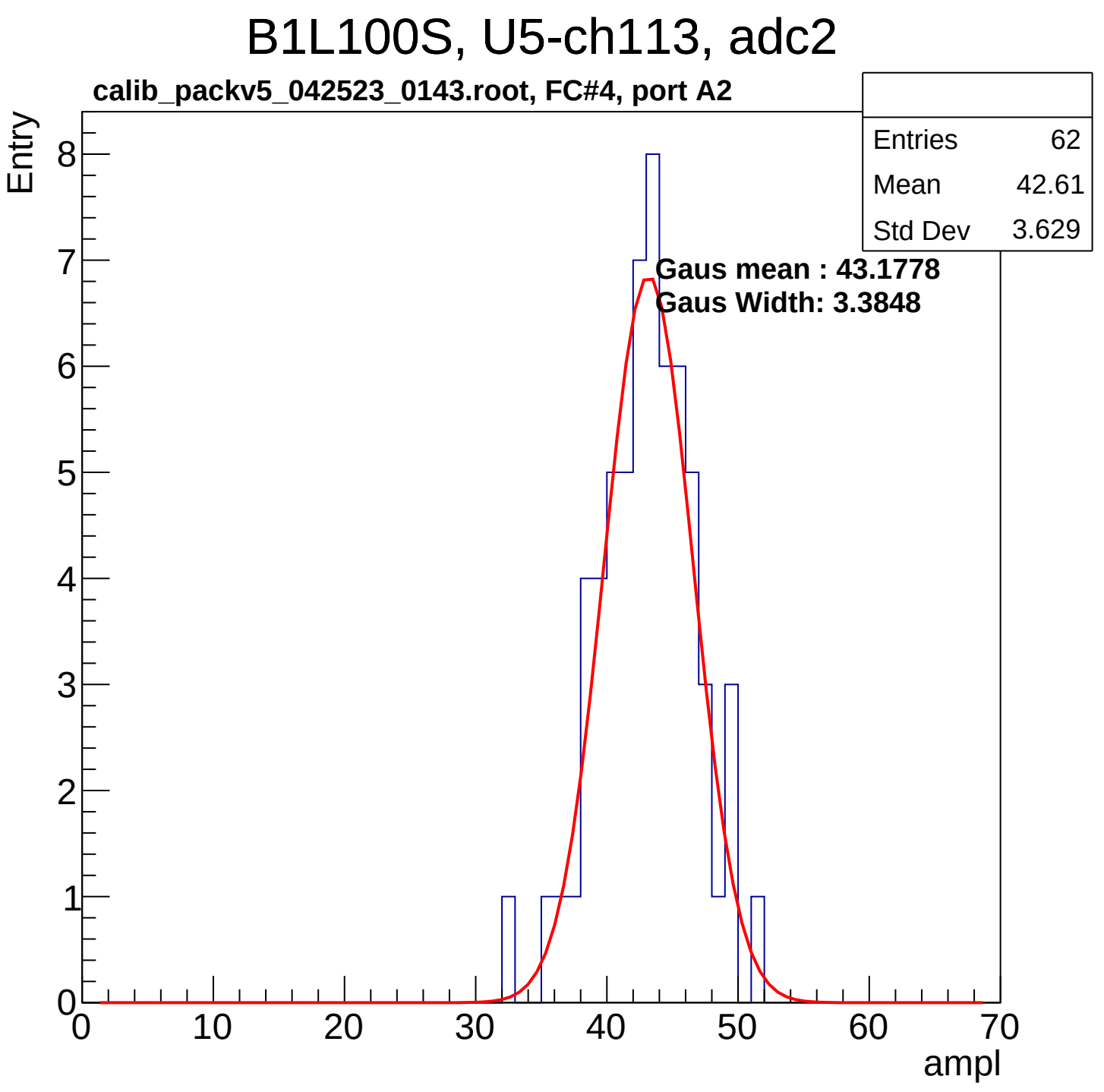
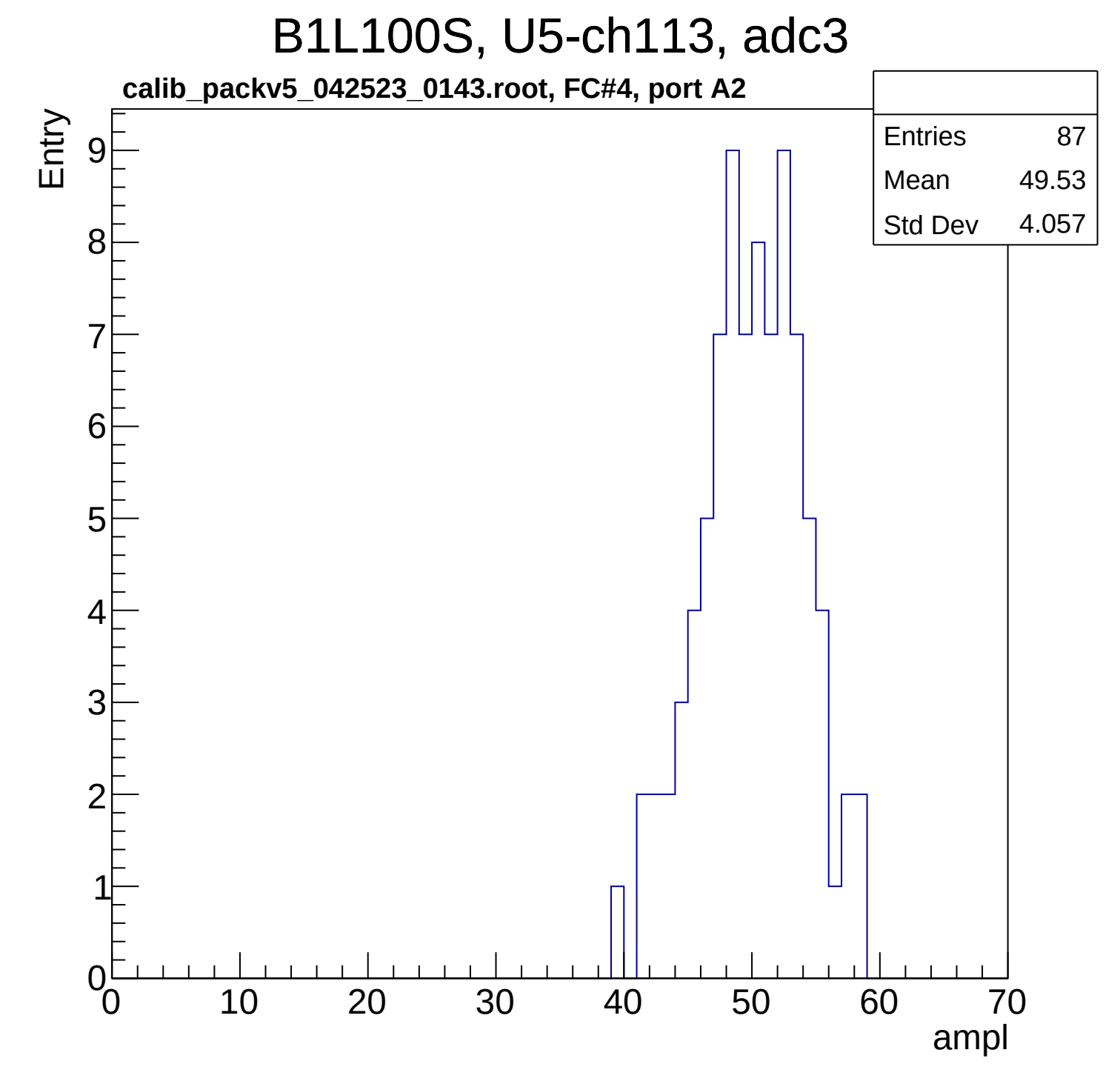
70


B1L100S, U5-ch112, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch113, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 76
Mean 29.36
Std Dev 3.687
Gaus mean : 29.5724
Gaus Width: 4.3574
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch113, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 35.85
Std Dev 3.661
Gaus mean : 36.8263
Gaus Width: 3.3674
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch113, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 42.61
Std Dev 3.629
Gaus mean : 43.1778
Gaus Width: 3.3848
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch113, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 87
Mean 49.53
Std Dev 4.057
Entry
ampl
0
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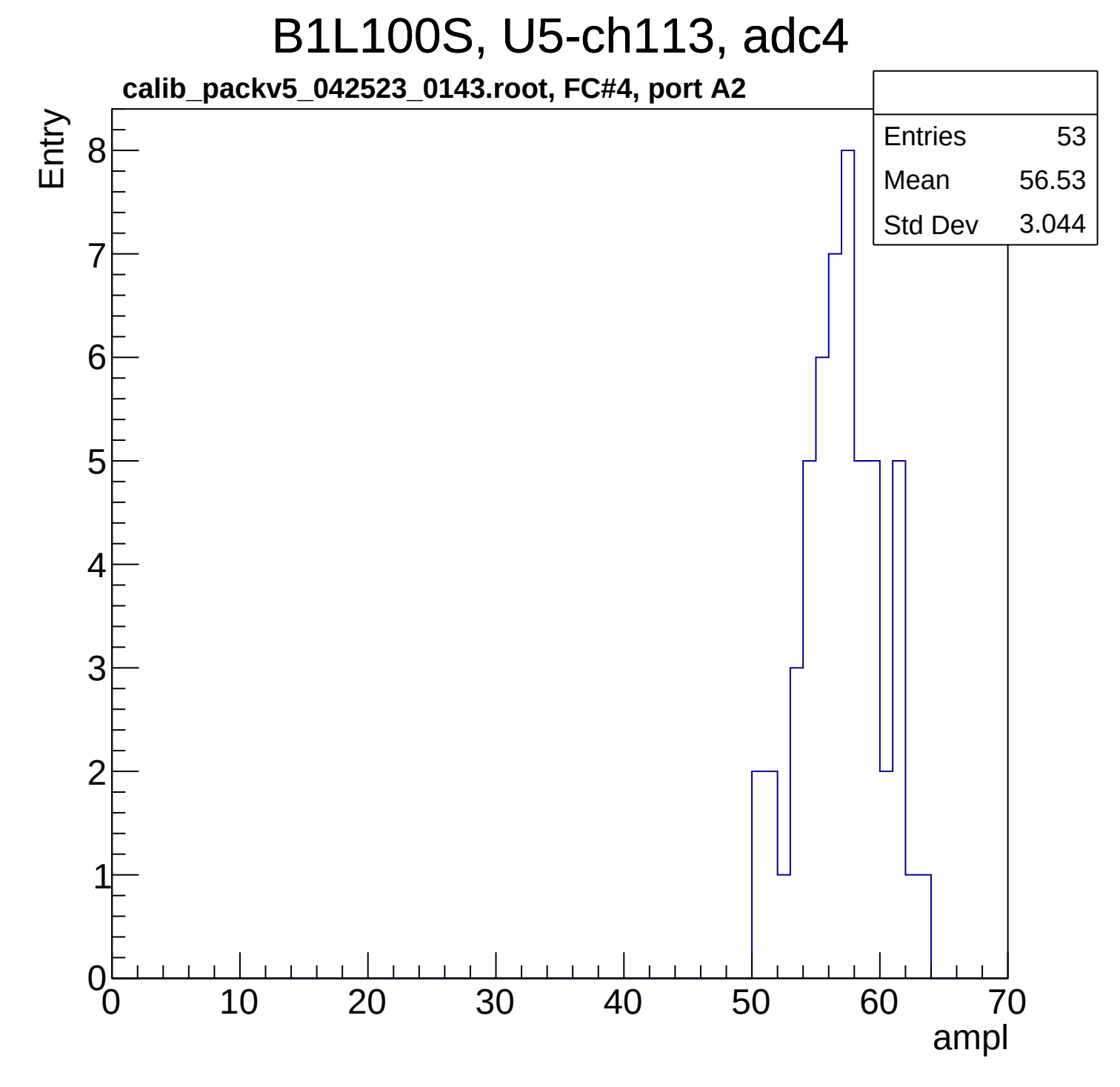
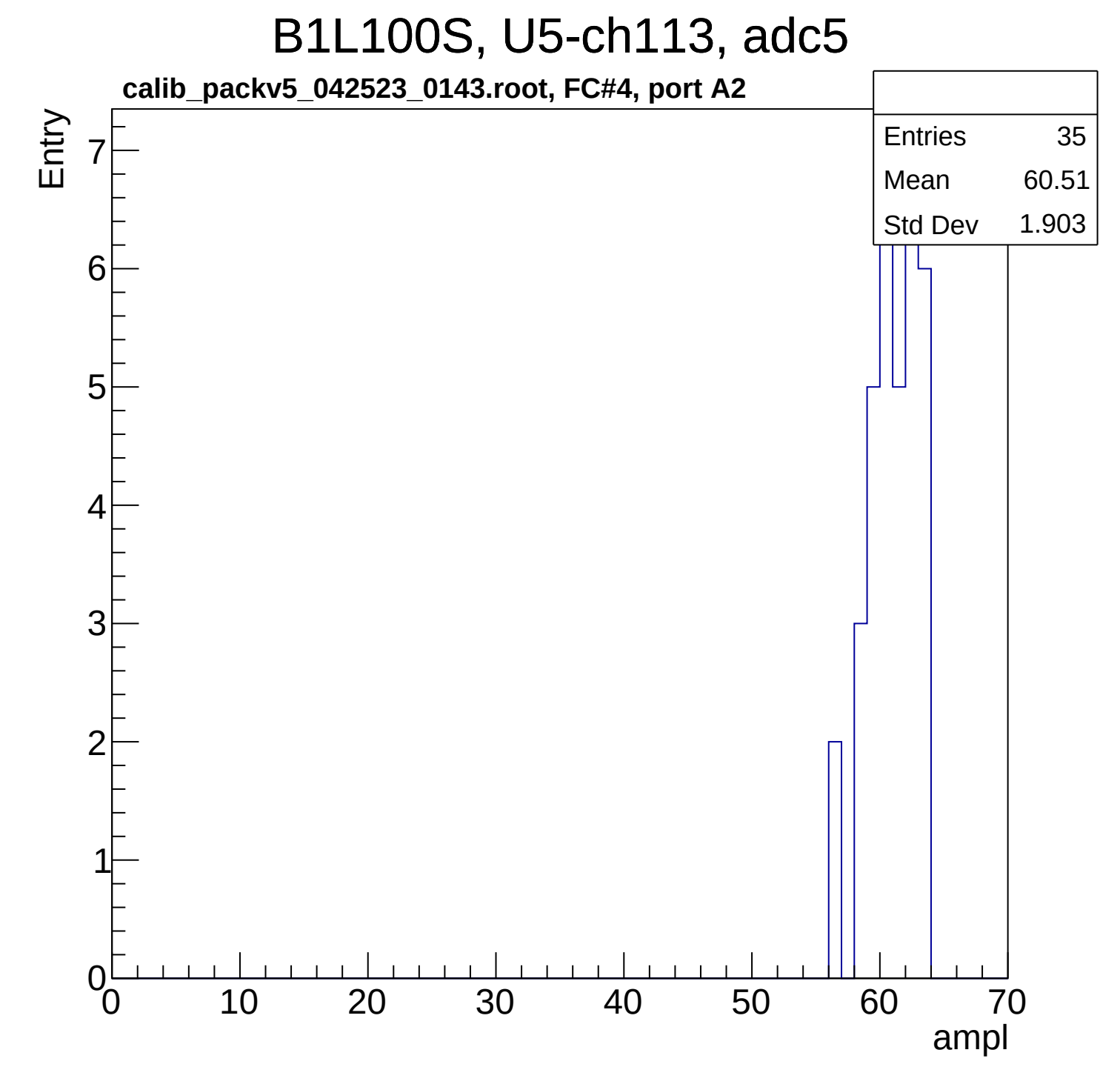
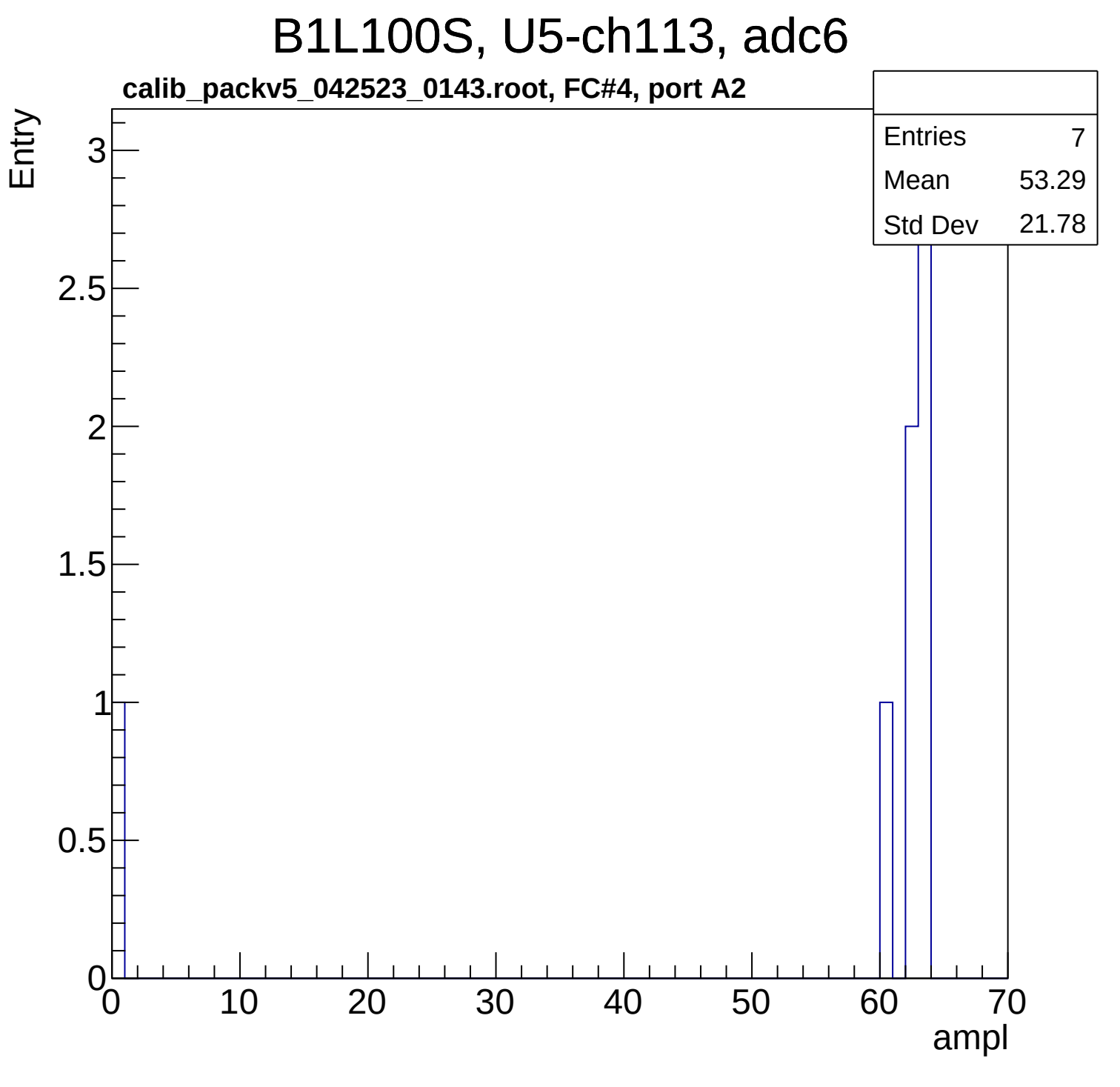
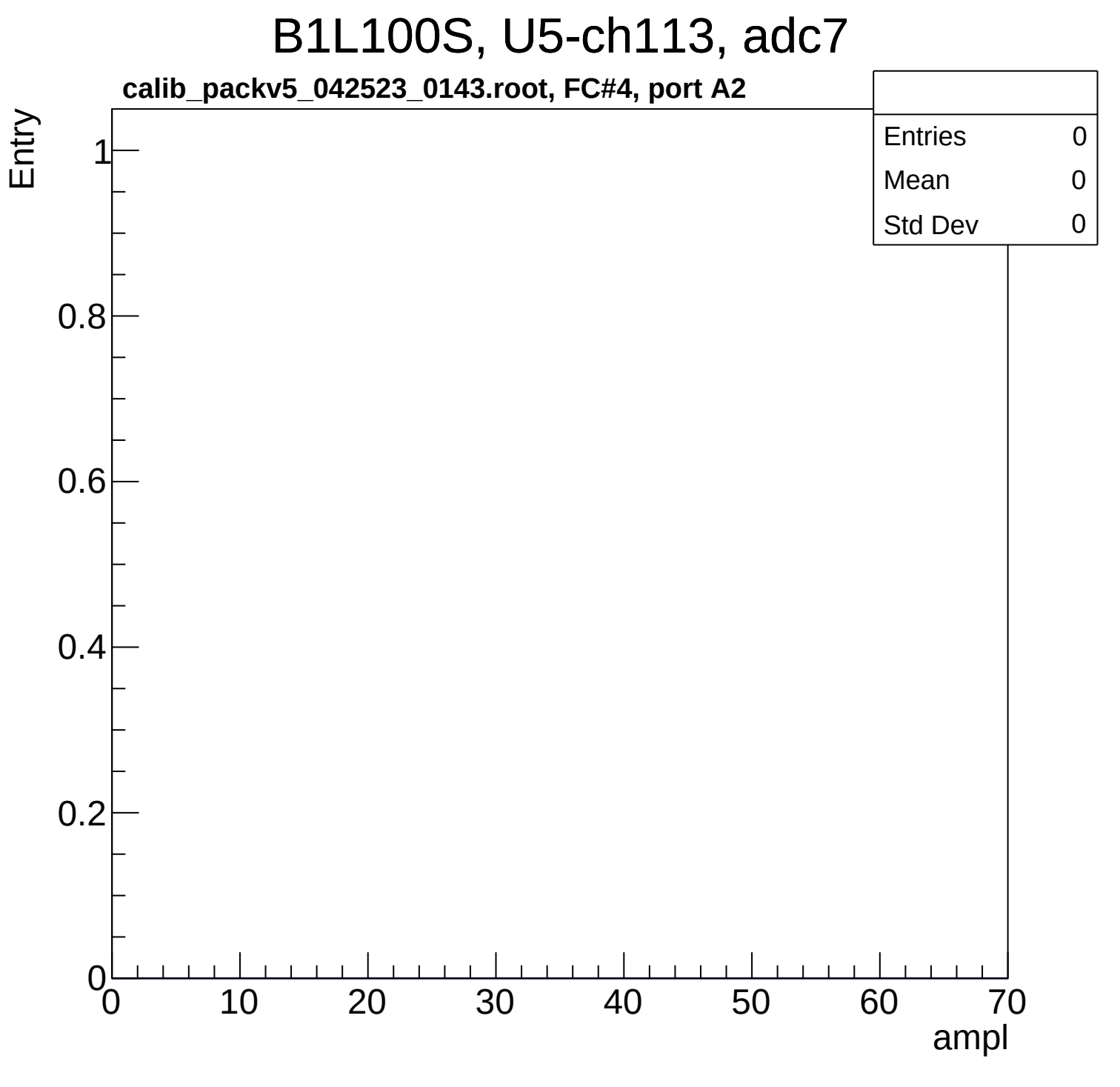
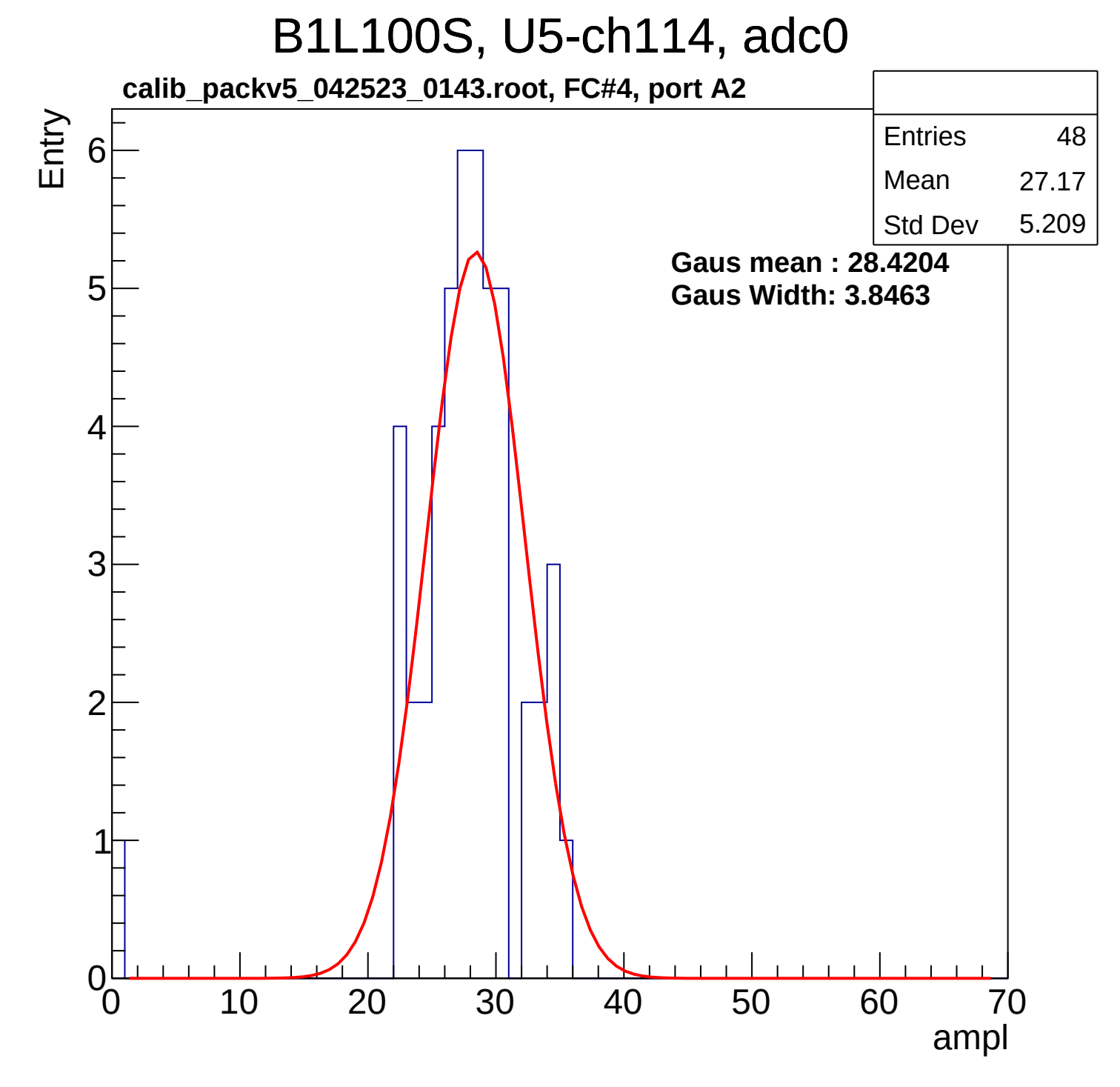
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

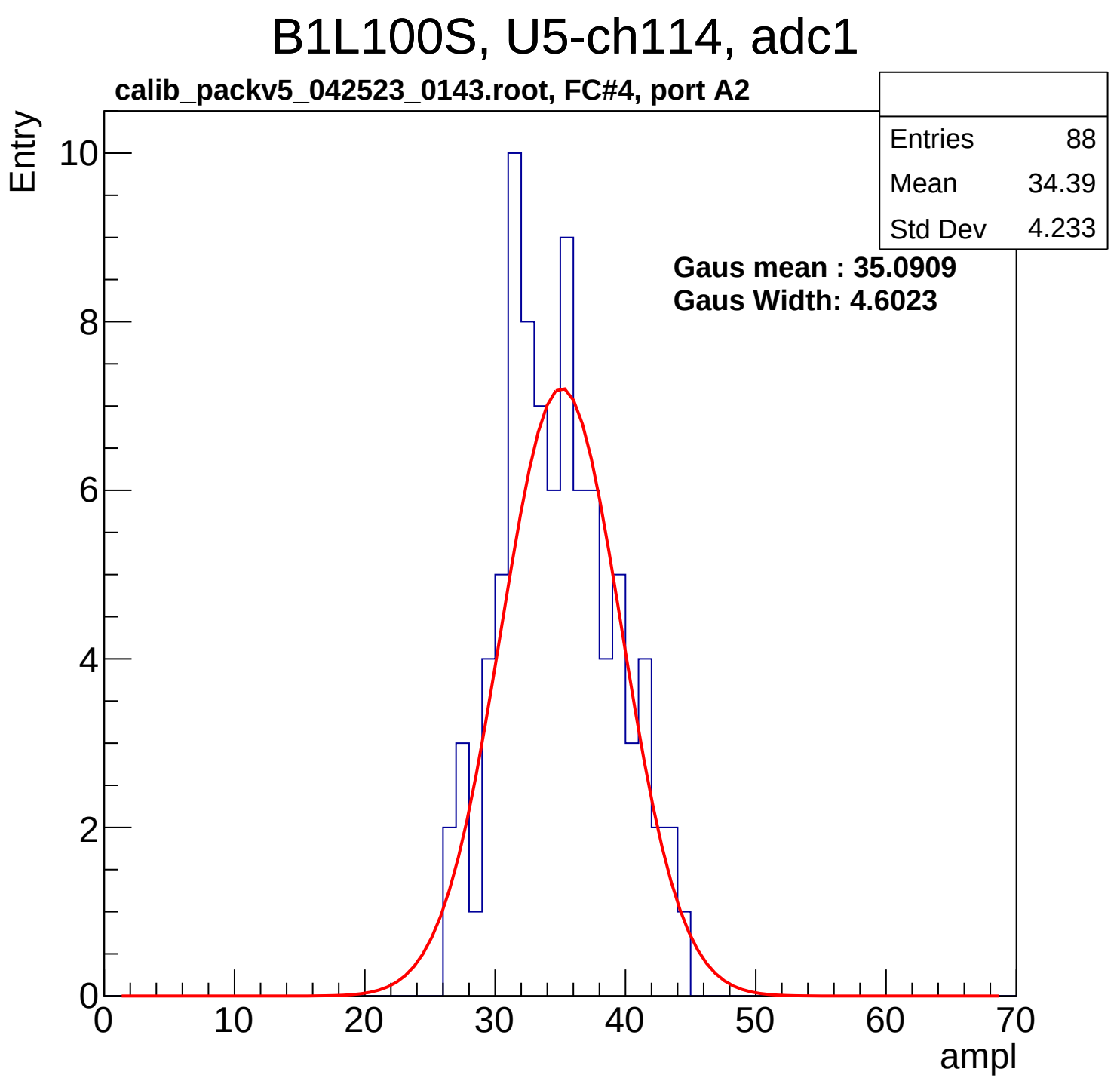

B1L100S, U5-ch113, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 56.53
Std Dev 3.044
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

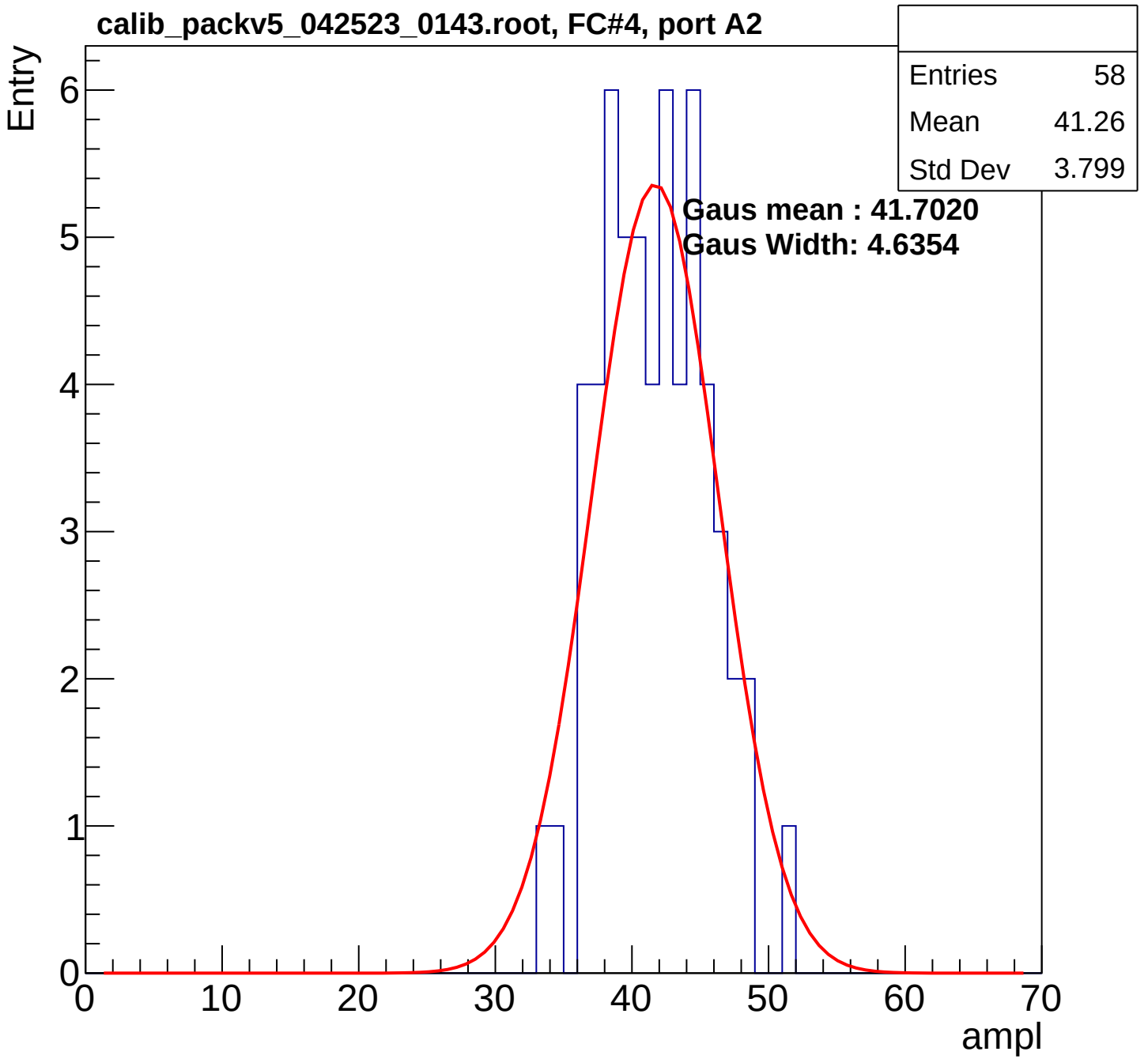

B1L100S, U5-ch113, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 35
Mean 60.51
Std Dev 1.903
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

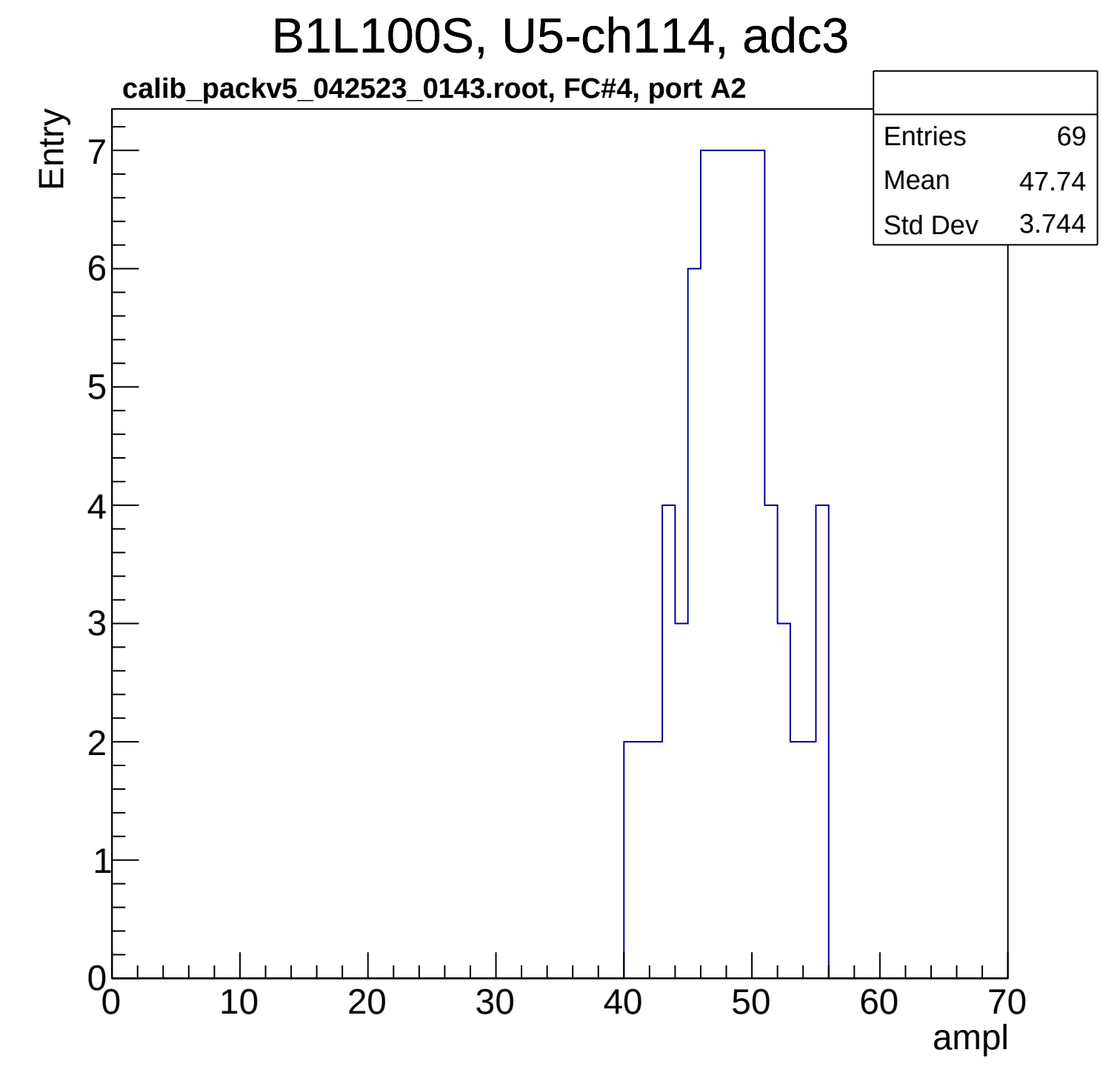

B1L100S, U5-ch113, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 7
Mean 53.29
Std Dev 21.78
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

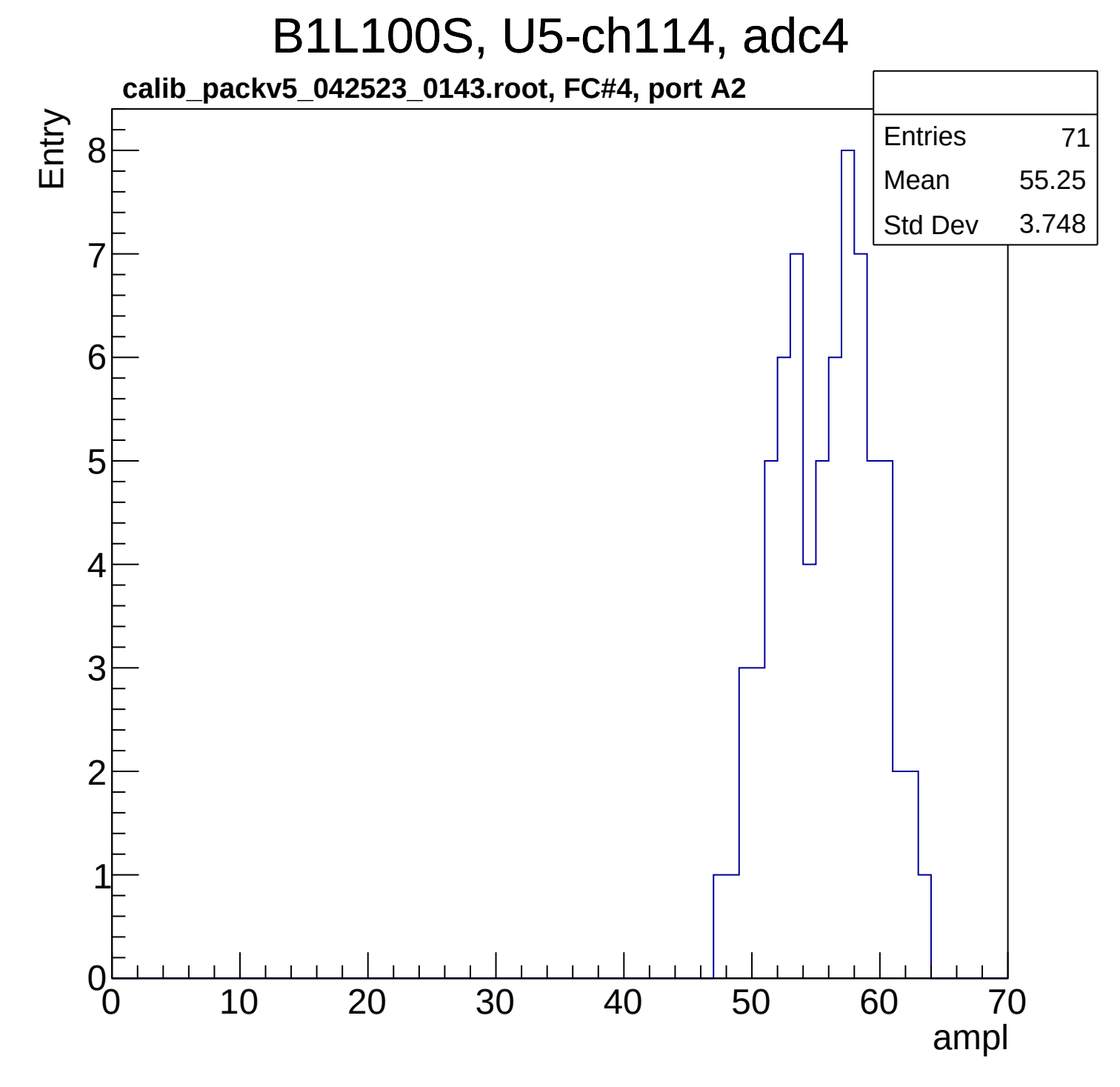

B1L100S, U5-ch113, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch114, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 48
Mean 27.17
Std Dev 5.209
Gaus mean : 28.4204
Gaus Width: 3.8463
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L100S, U5-ch114, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 88
Mean 34.39
Std Dev 4.233
Gaus mean : 35.0909
Gaus Width: 4.6023
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch114, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 41.26
Std Dev 3.799
Gaus mean : 41.7020
Gaus Width: 4.6354
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L100S, U5-ch114, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 47.74
Std Dev 3.744
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U5-ch114, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 55.25
Std Dev 3.748
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
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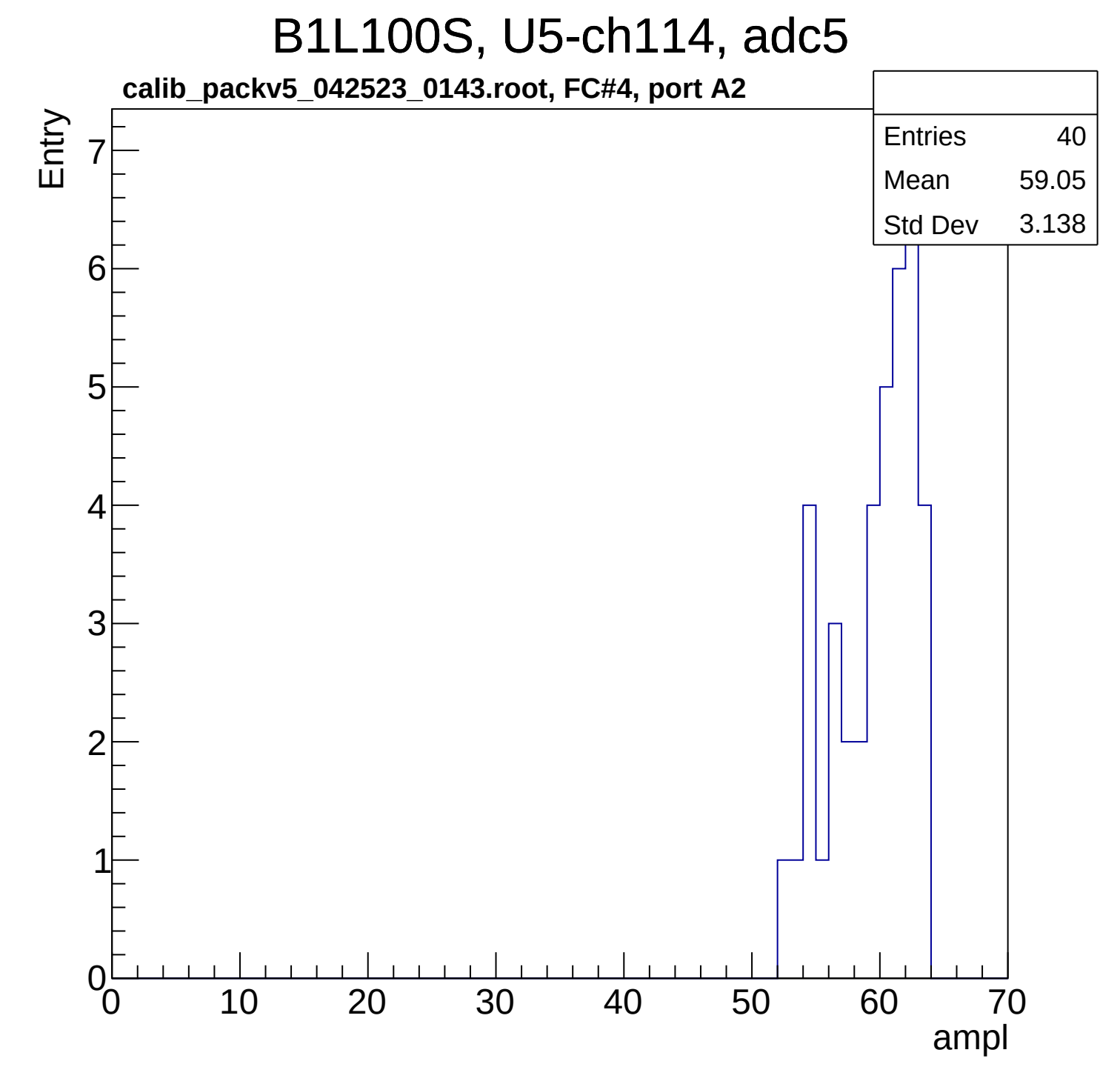
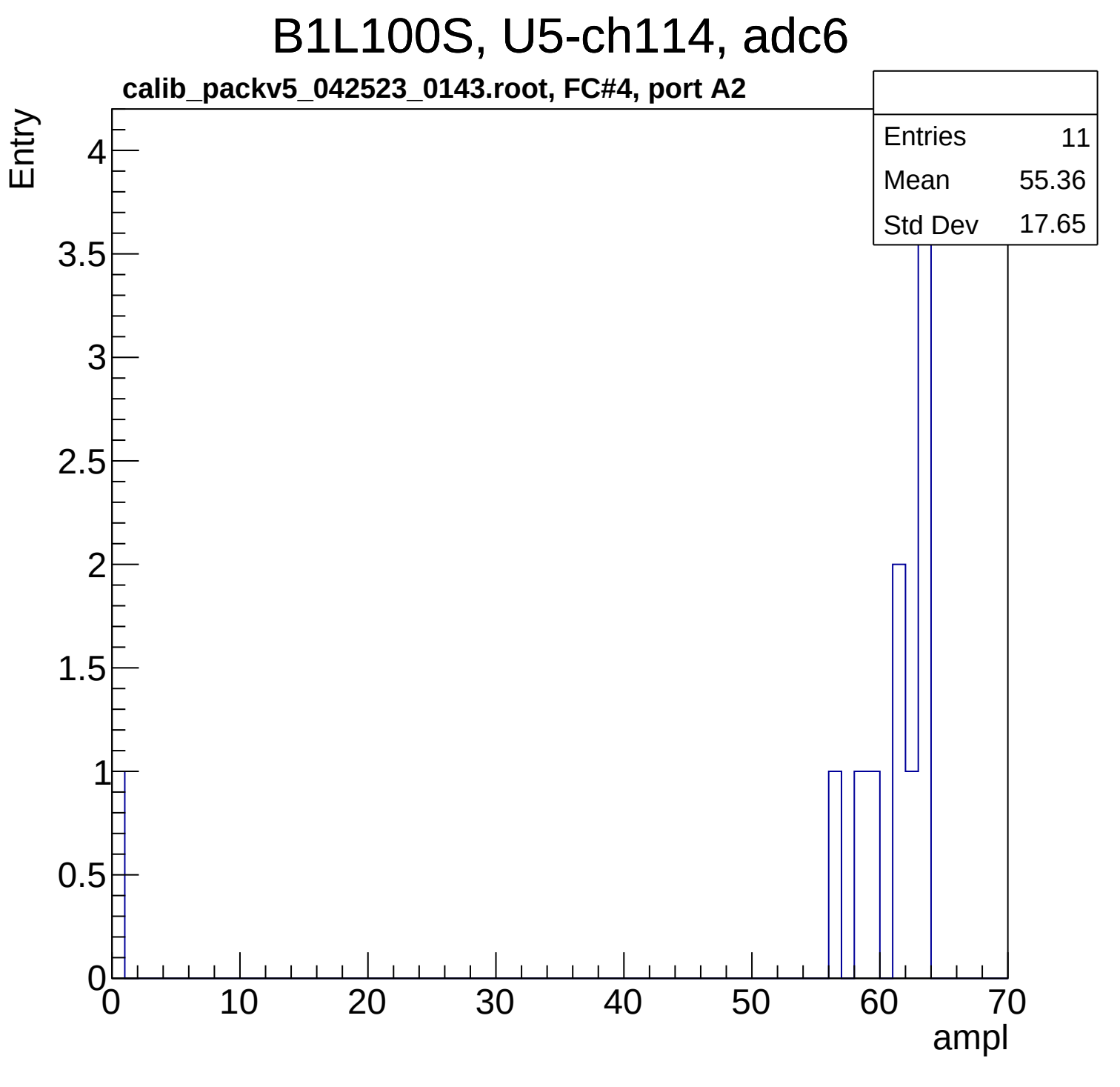
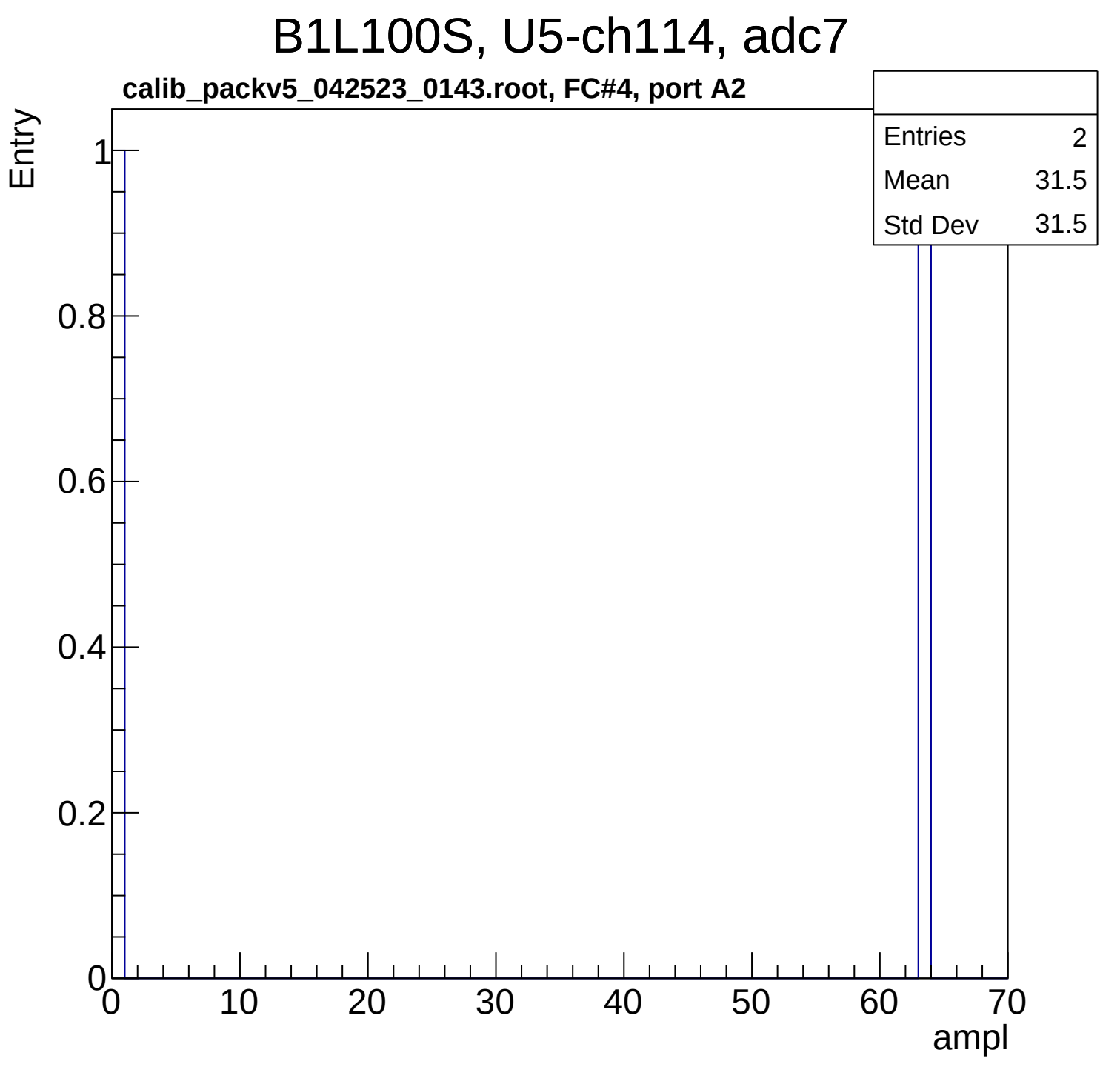
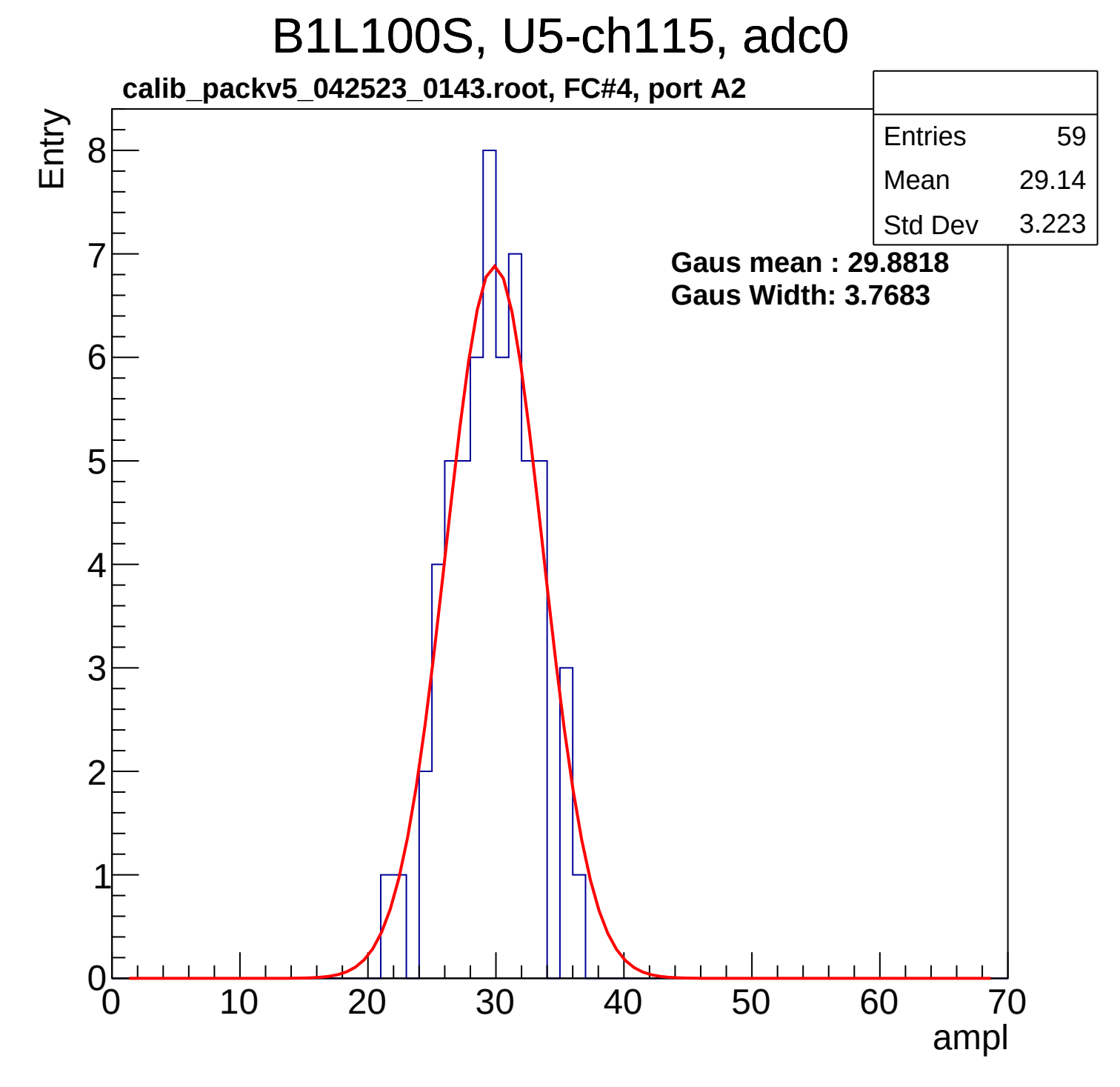
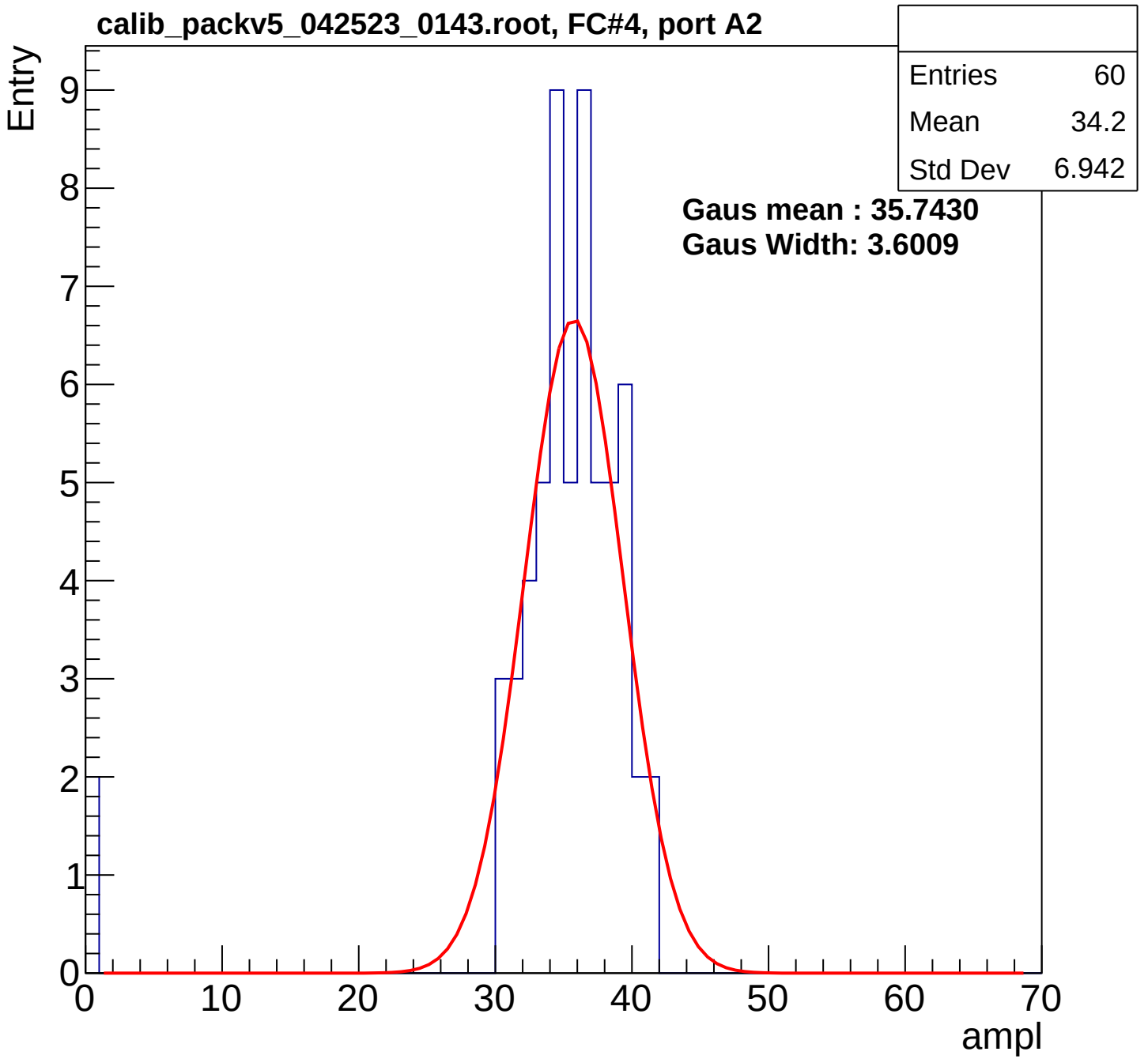
60
70

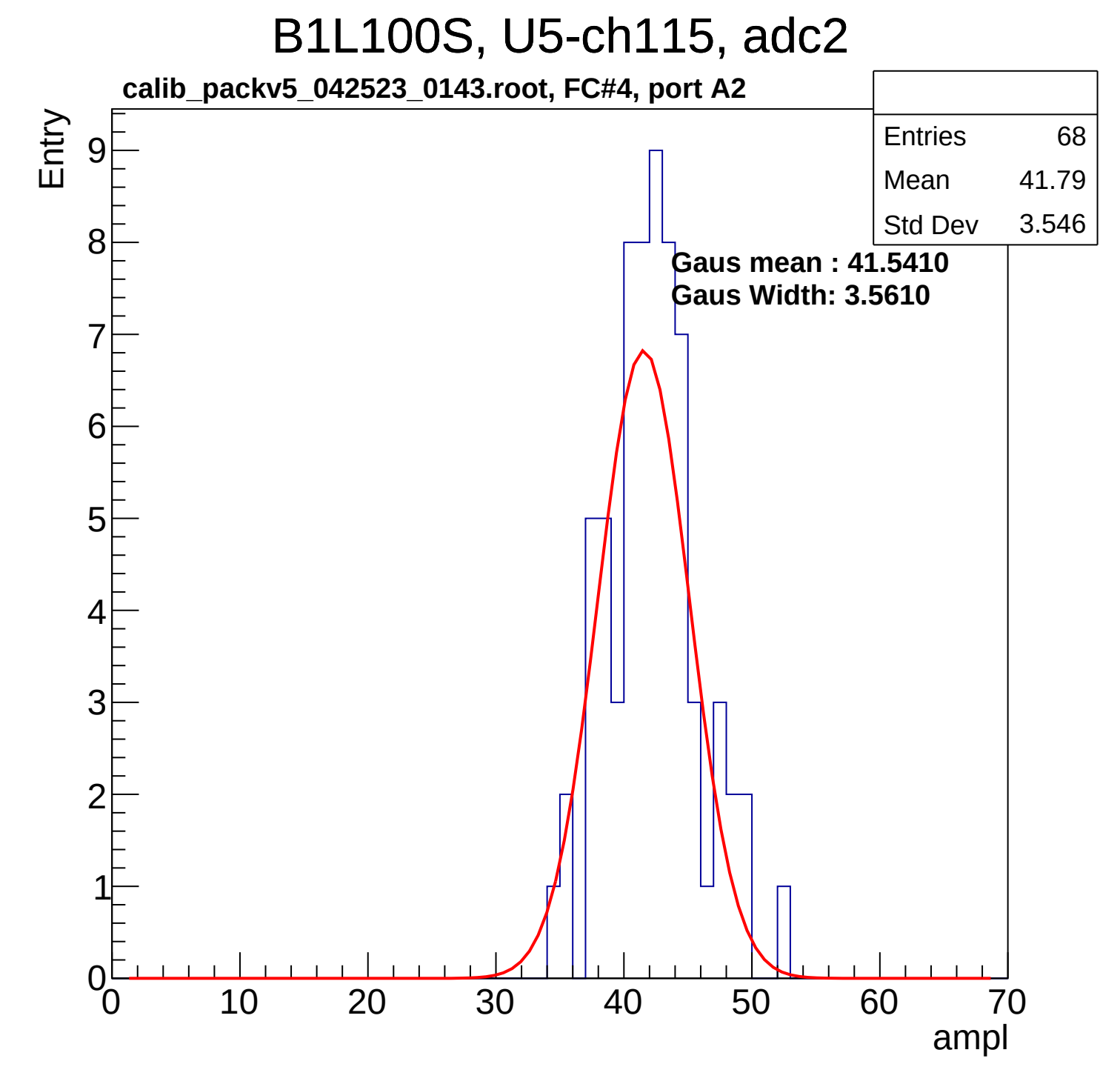

B1L100S, U5-ch114, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 40
Mean 59.05
Std Dev 3.138
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U5-ch114, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 11
Mean 55.36
Std Dev 17.65
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L100S, U5-ch114, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 31.5
Std Dev 31.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch115, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 29.14
Std Dev 3.223
Gaus mean : 29.8818
Gaus Width: 3.7683
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch115, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 34.2
Std Dev 6.942
Gaus mean : 35.7430
Gaus Width: 3.6009
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch115, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 41.79
Std Dev 3.546
Gaus mean : 41.5410
Gaus Width: 3.5610
Entry
ampl
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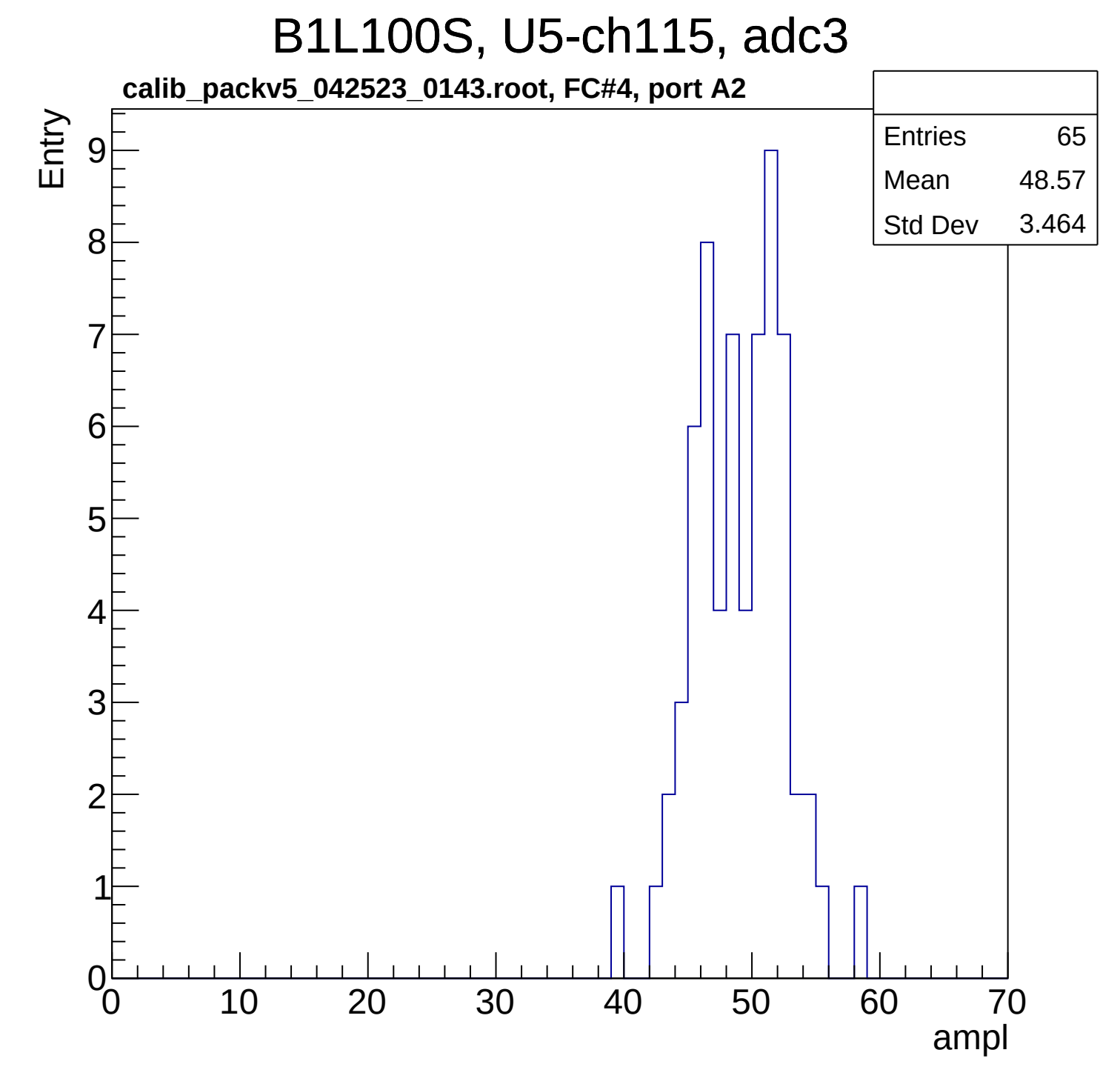
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L100S, U5-ch115, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 48.57
Std Dev 3.464
Entry
ampl
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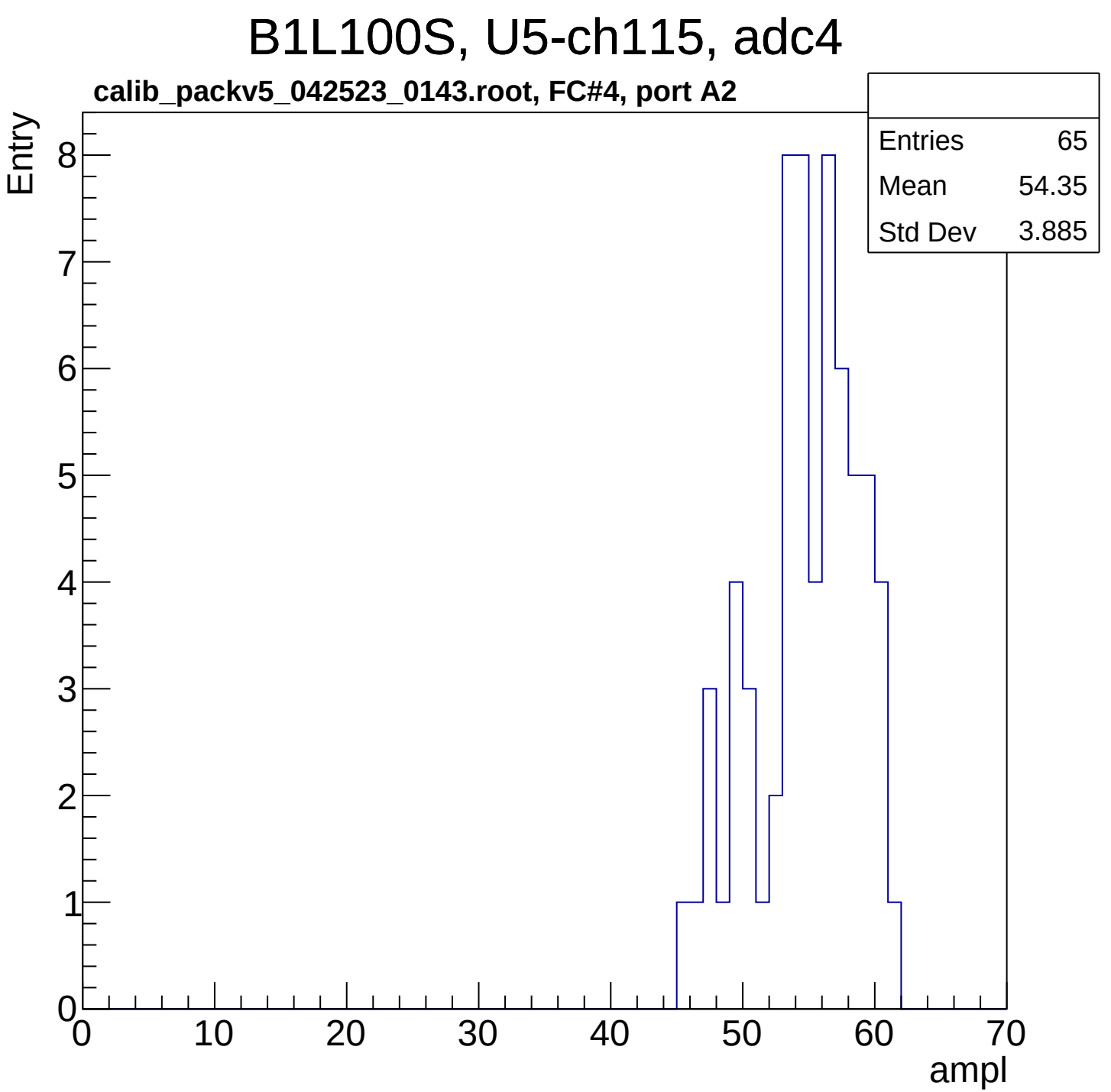
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch115, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 54.35
Std Dev 3.885
Entry
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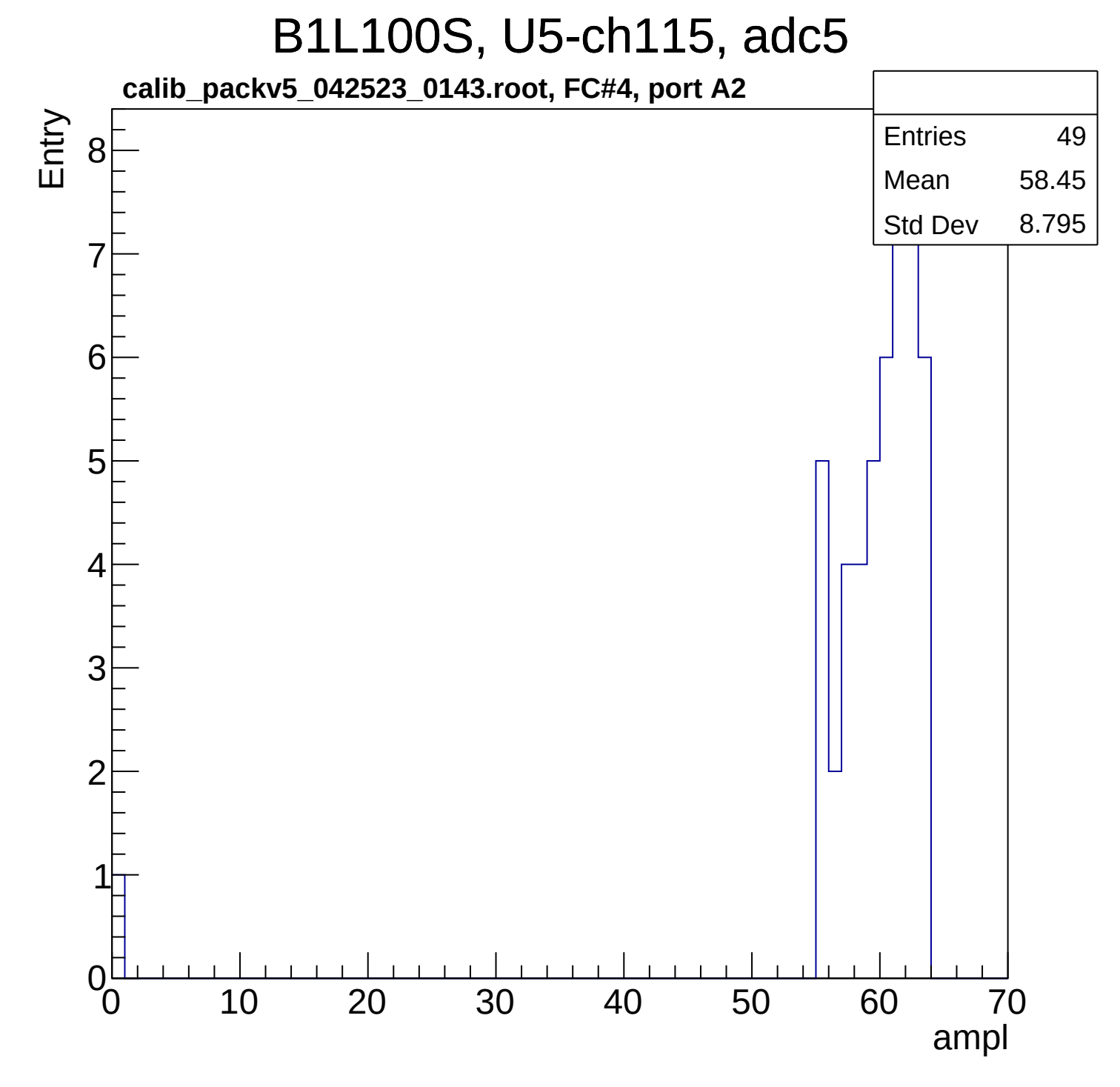
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch115, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 49
Mean 58.45
Std Dev 8.795
Entry
ampl
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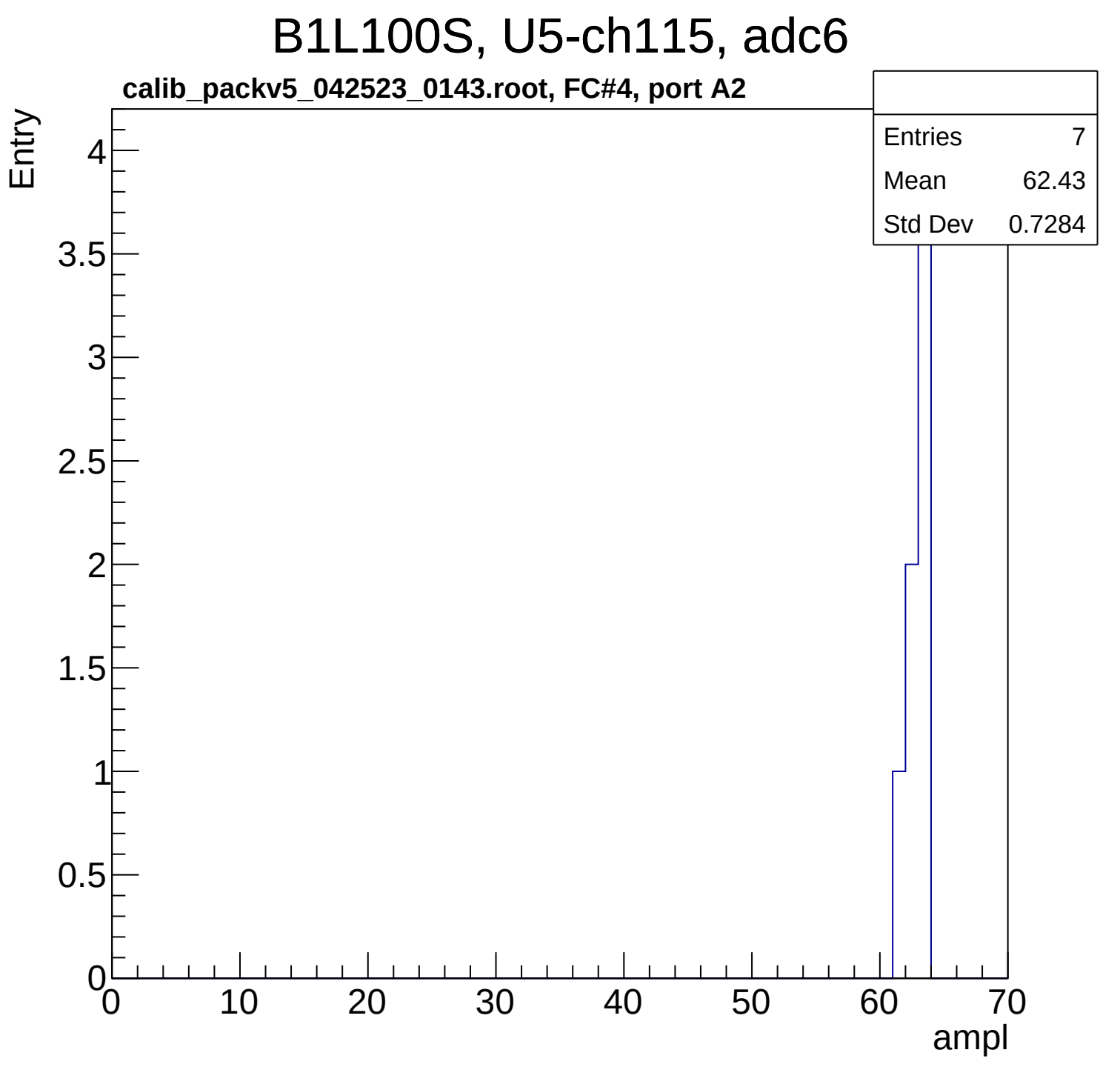
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch115, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 7
Mean 62.43
Std Dev 0.7284
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
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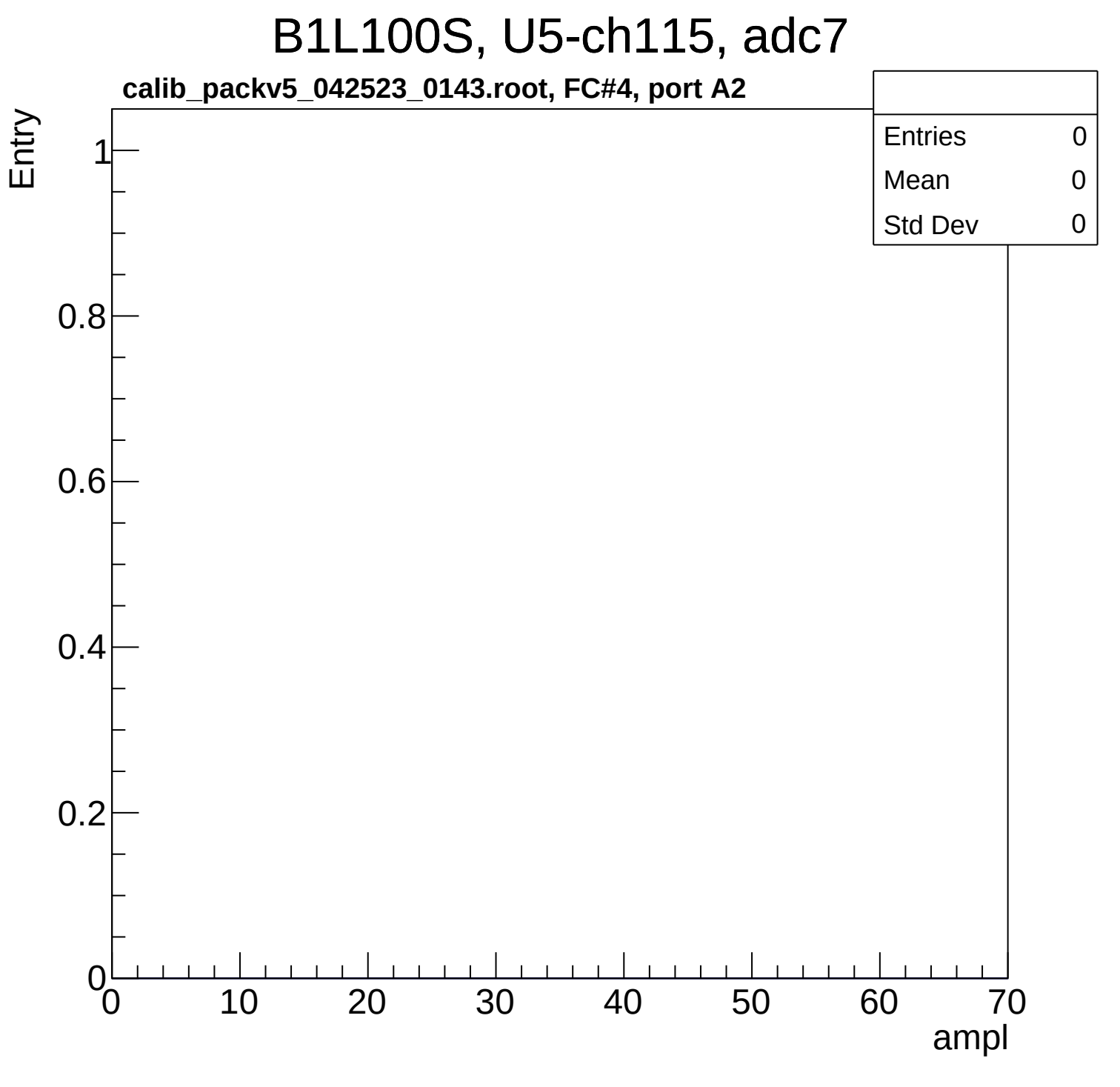
30
40
50
60
70


B1L100S, U5-ch115, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
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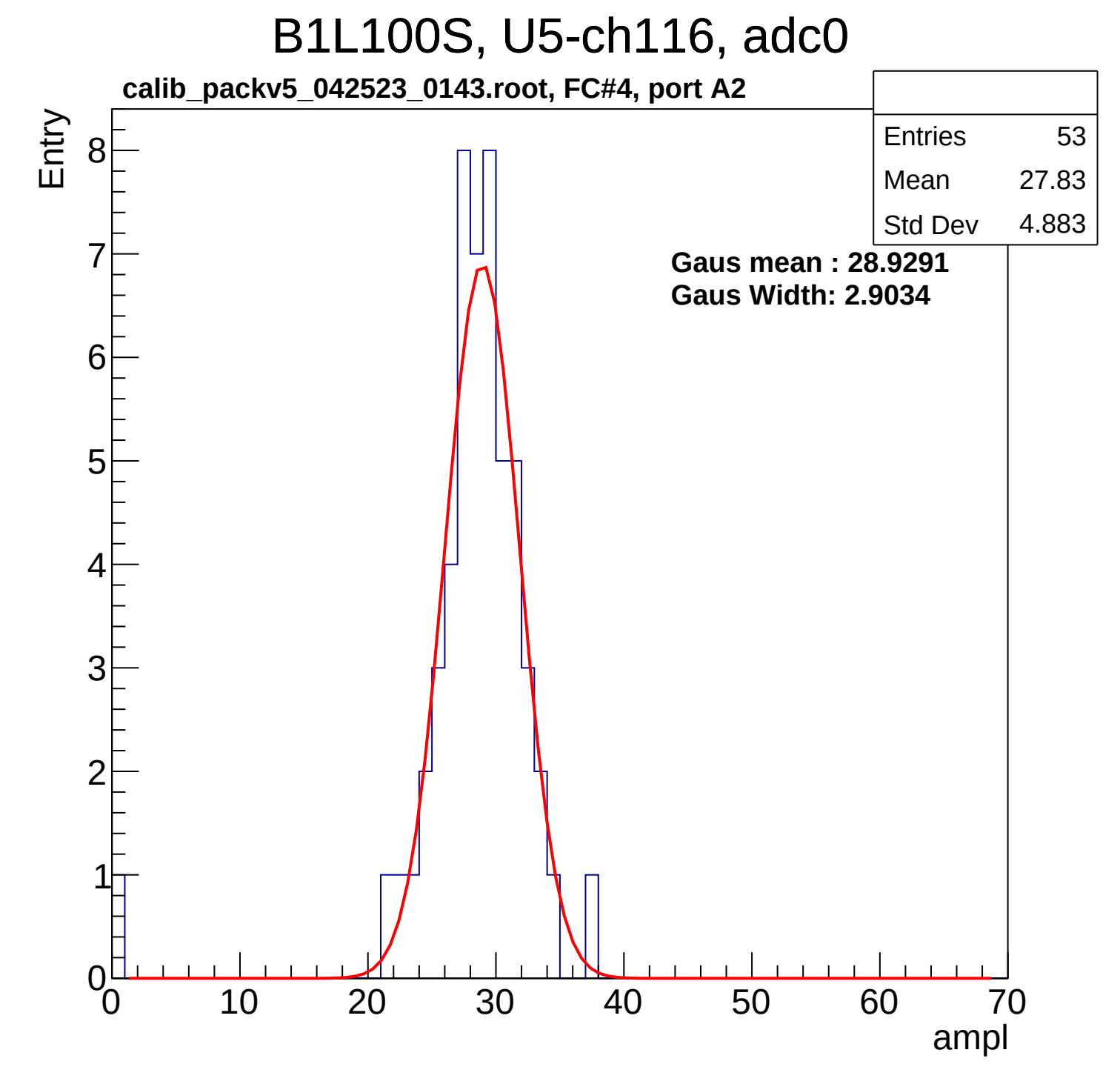
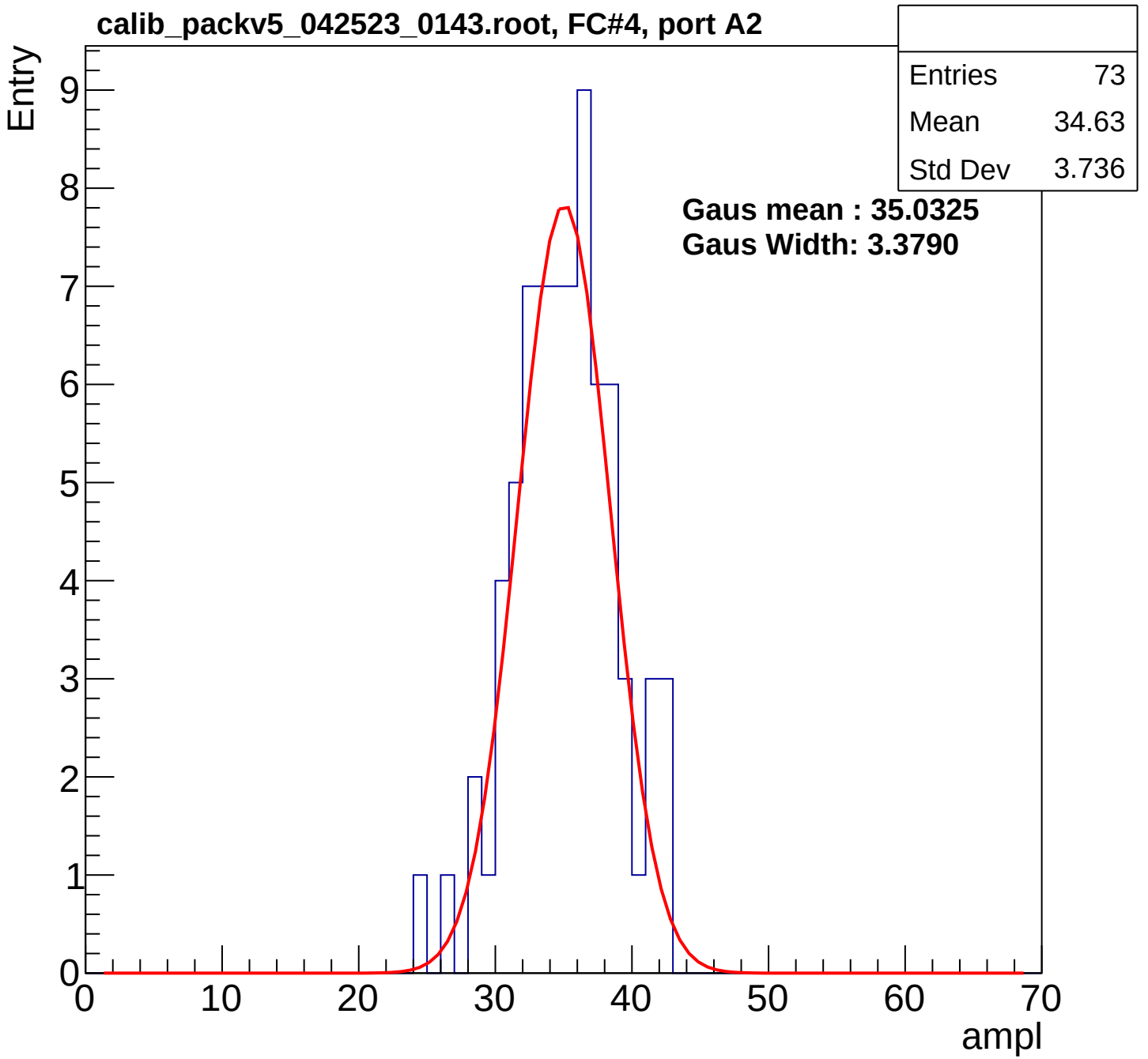
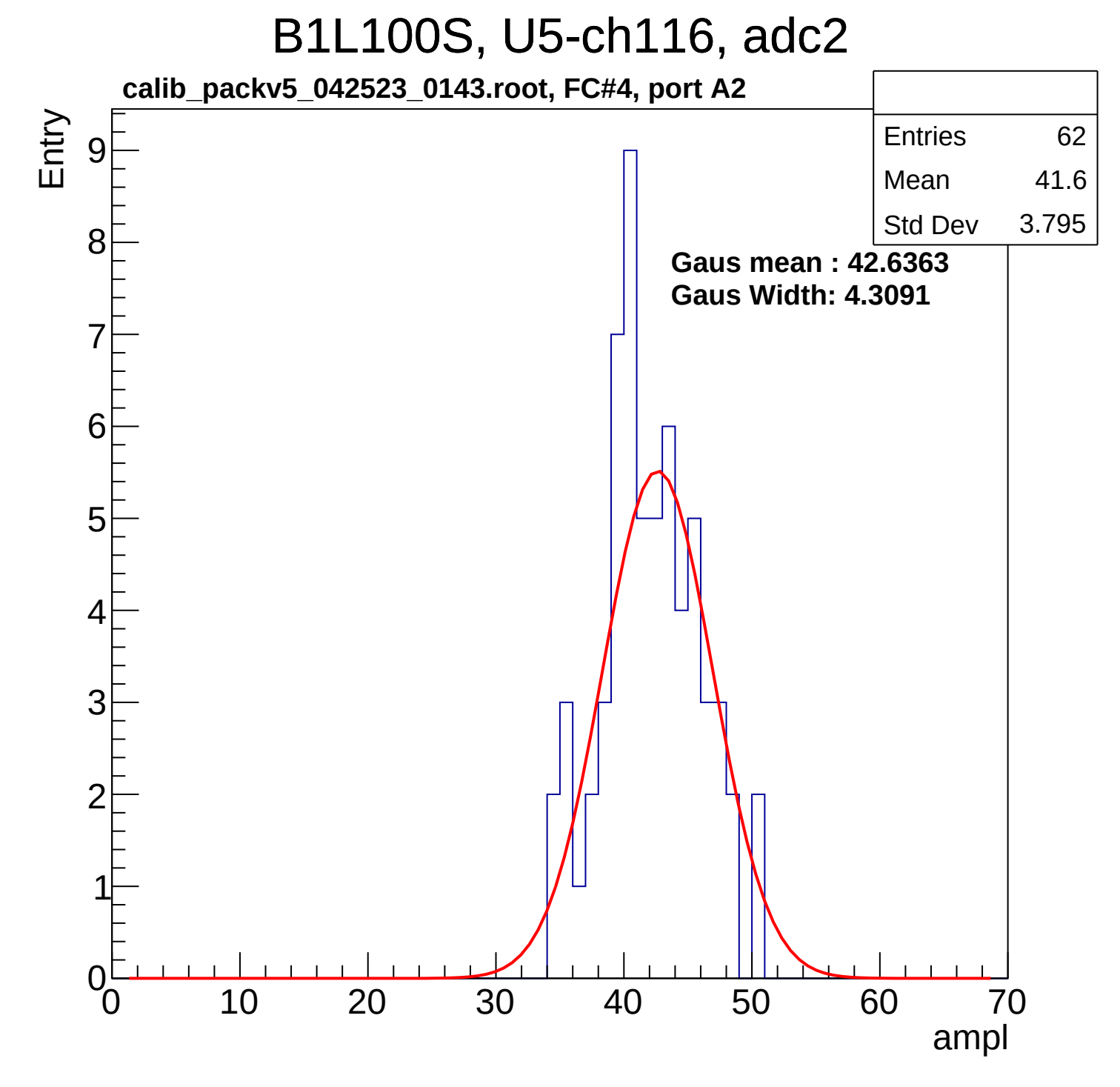
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch116, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 27.83
Std Dev 4.883
Gaus mean : 28.9291
Gaus Width: 2.9034
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch116, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 34.63
Std Dev 3.736
Gaus mean : 35.0325
Gaus Width: 3.3790
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch116, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 41.6
Std Dev 3.795
Gaus mean : 42.6363
Gaus Width: 4.3091
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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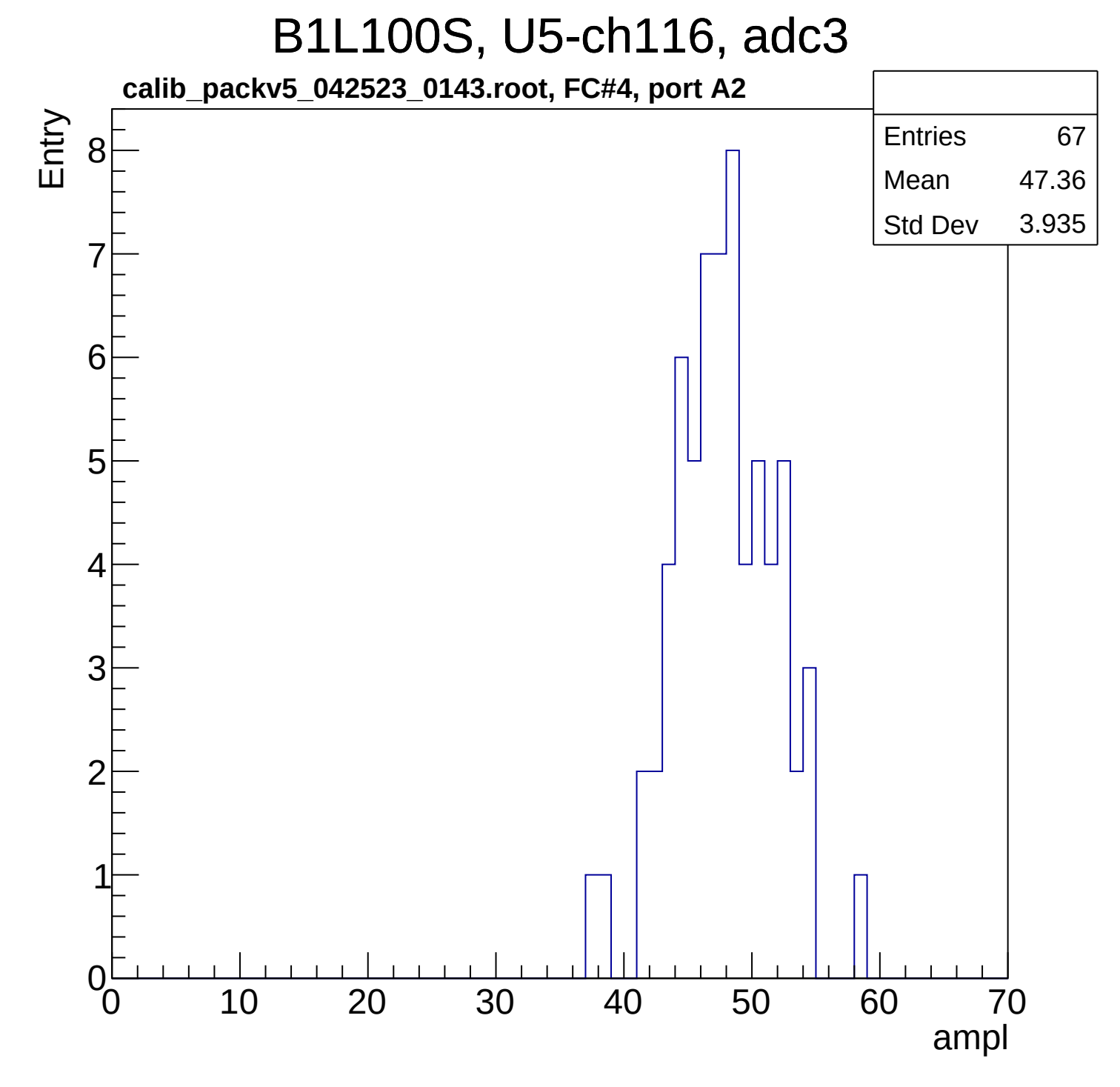
60
70


B1L100S, U5-ch116, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 47.36
Std Dev 3.935
Entry
ampl
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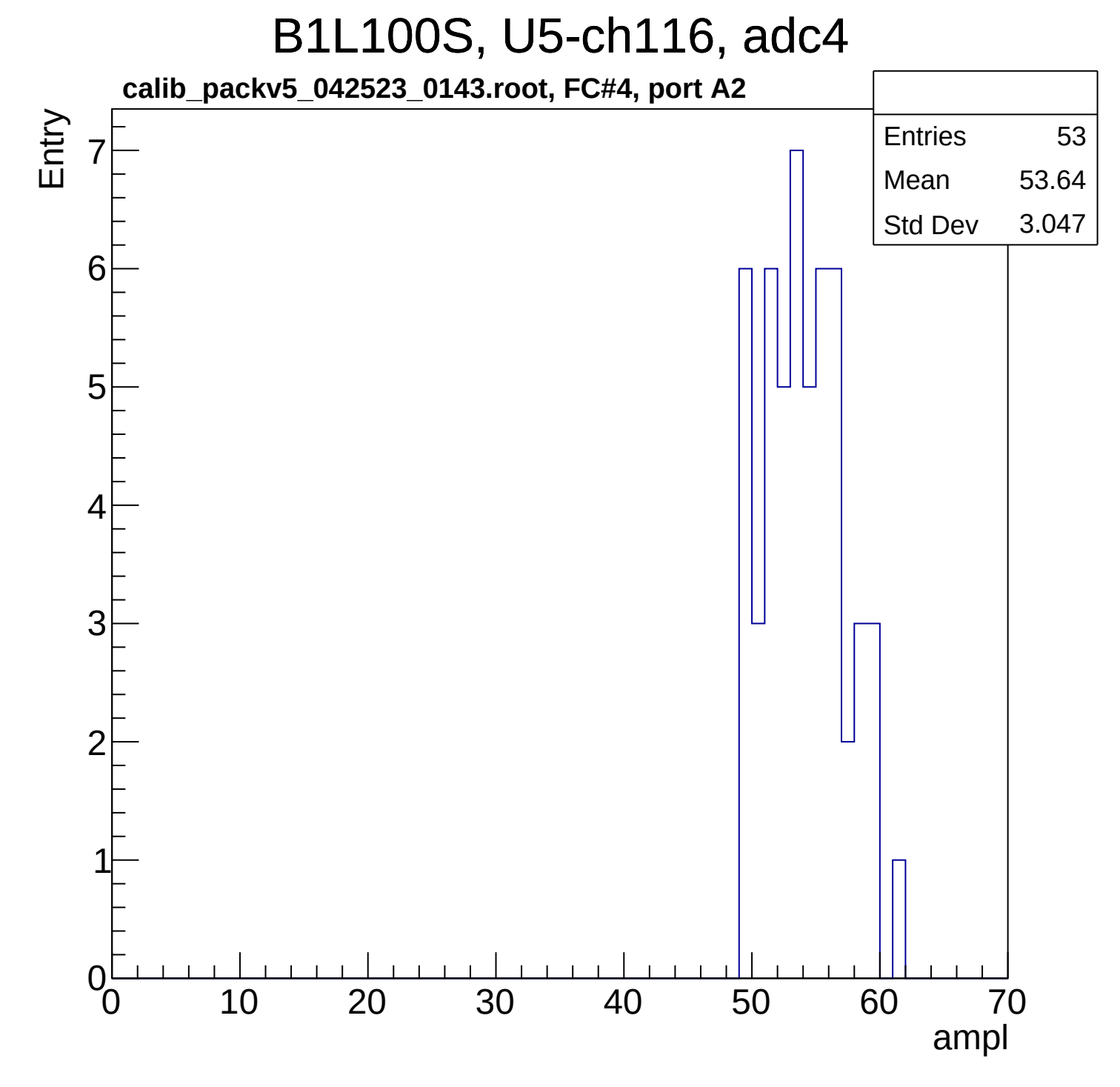
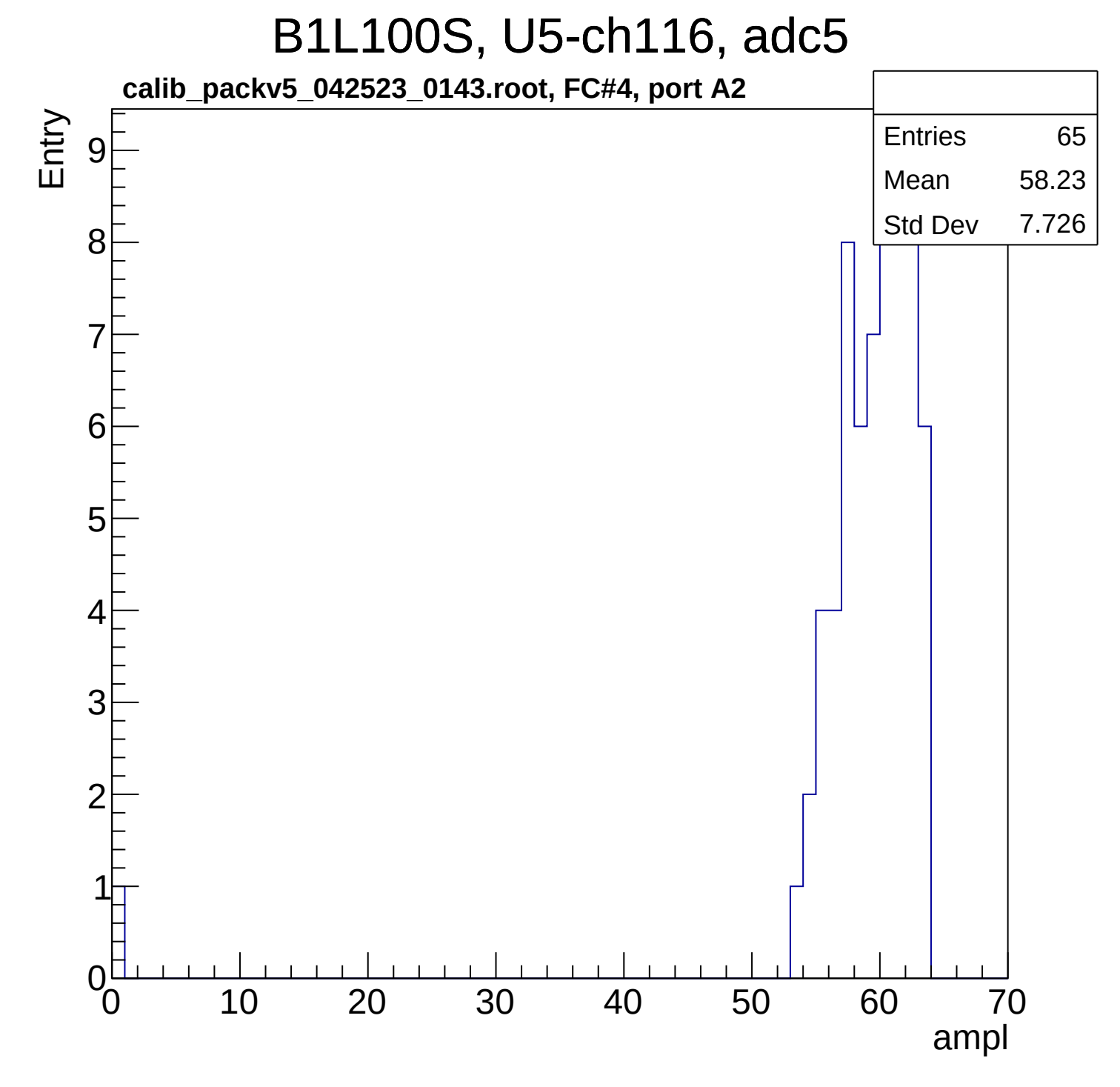
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch116, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 53.64
Std Dev 3.047
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U5-ch116, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 58.23
Std Dev 7.726
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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40
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60
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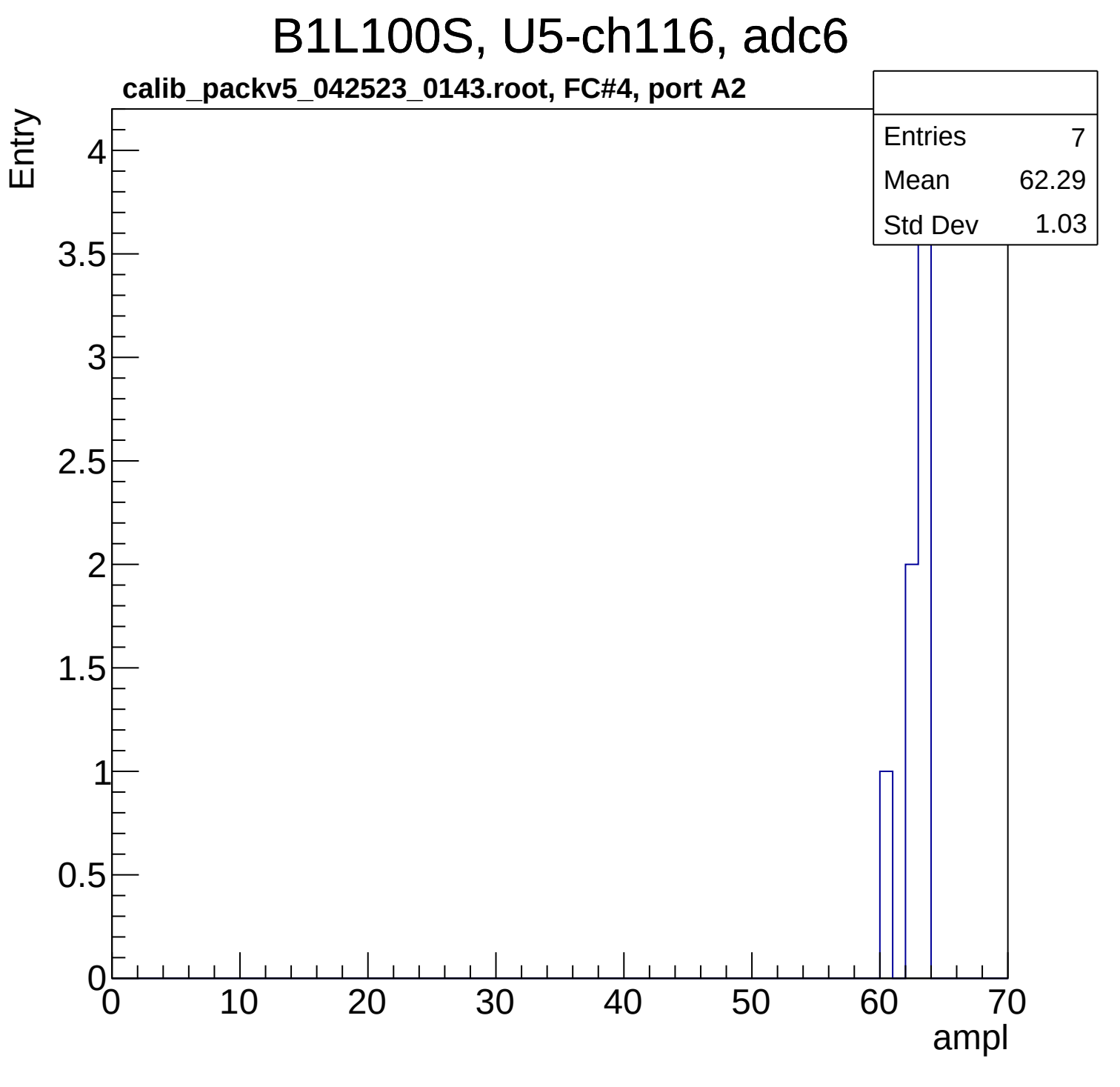
B1L100S, U5-ch116, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 7
Mean 62.29
Std Dev 1.03
Entry
ampl
0
0.5
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1.5
2
2.5
3
3.5
4
0
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20
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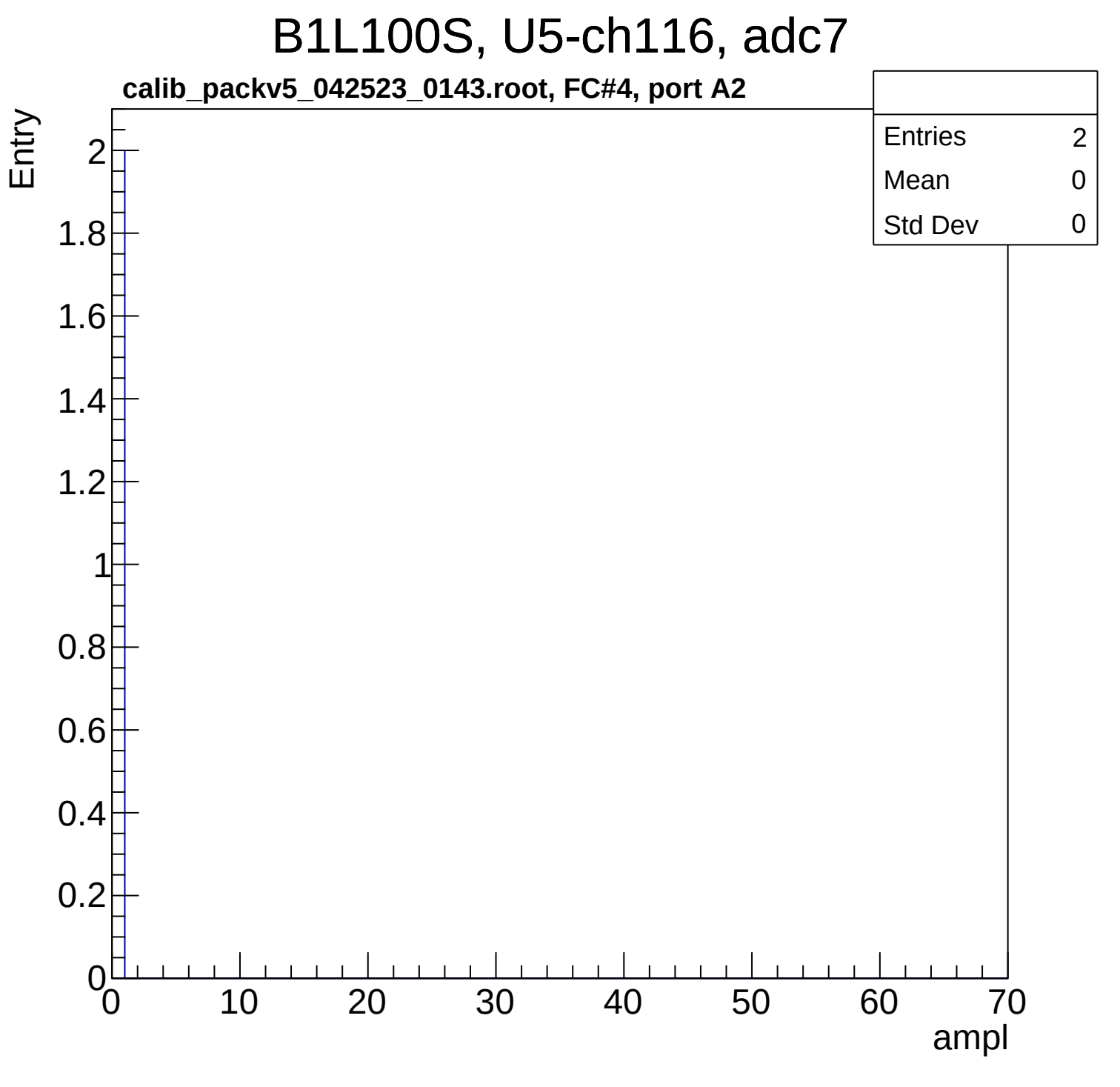
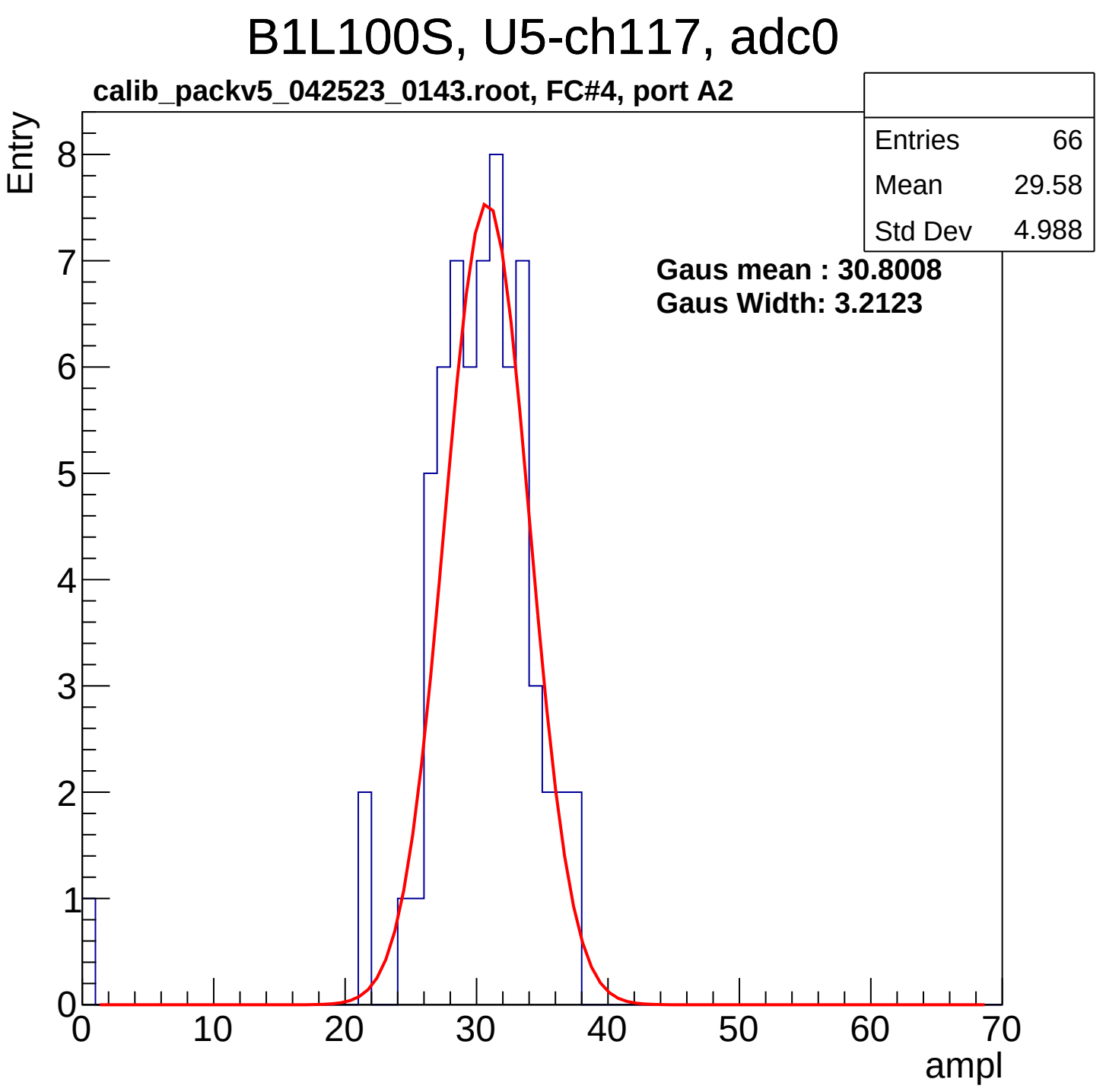
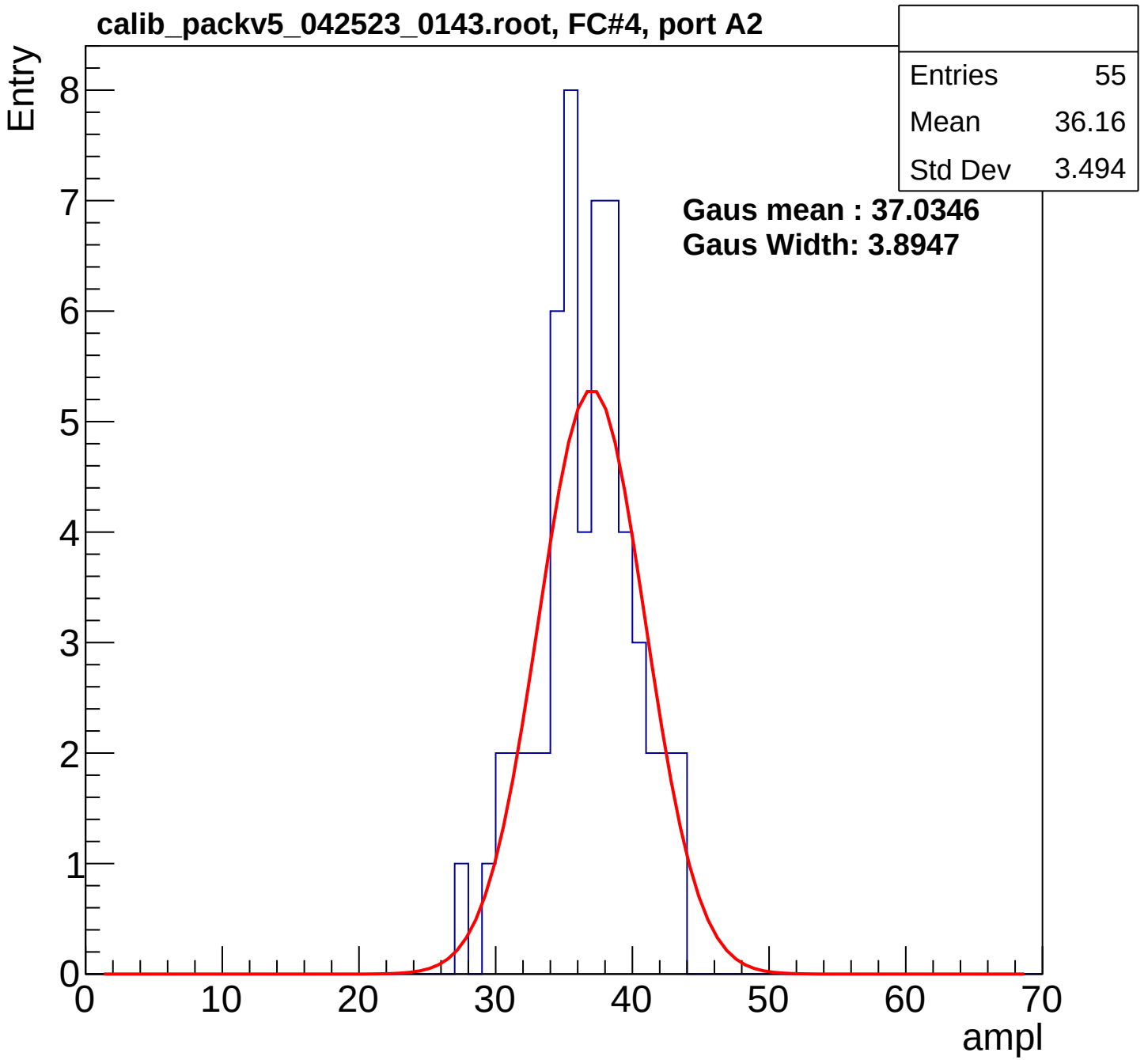
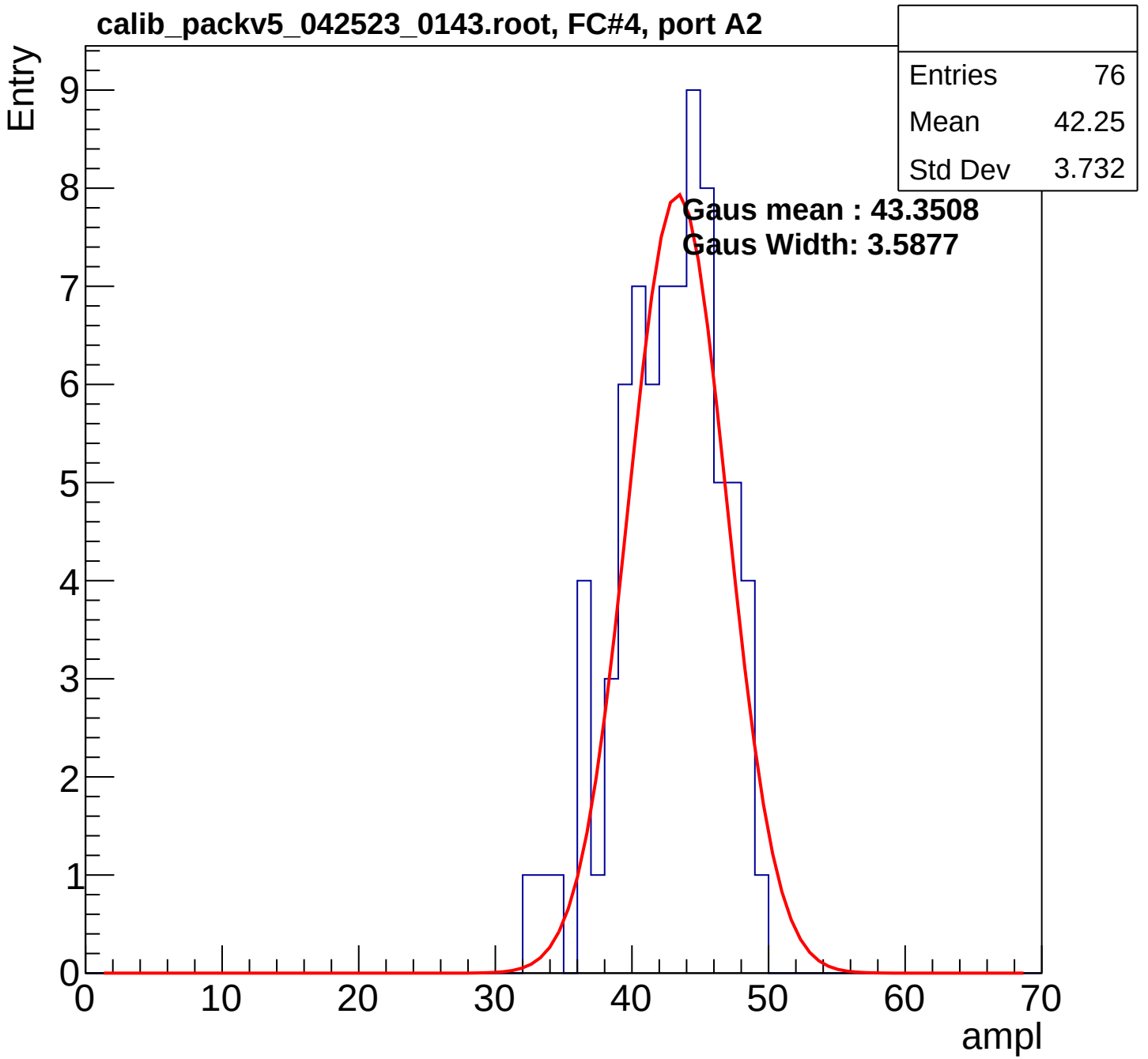
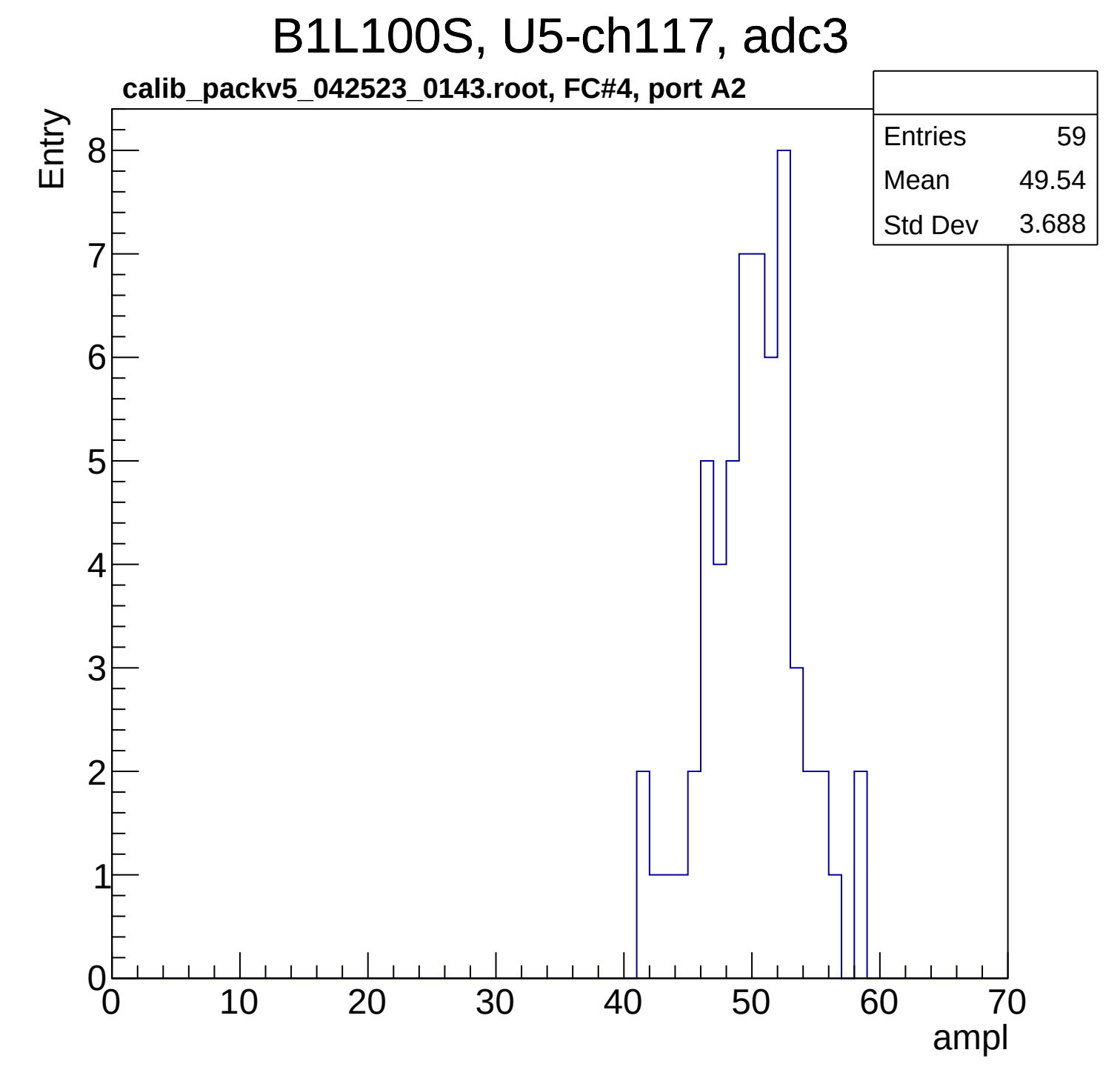
40
50
60
70

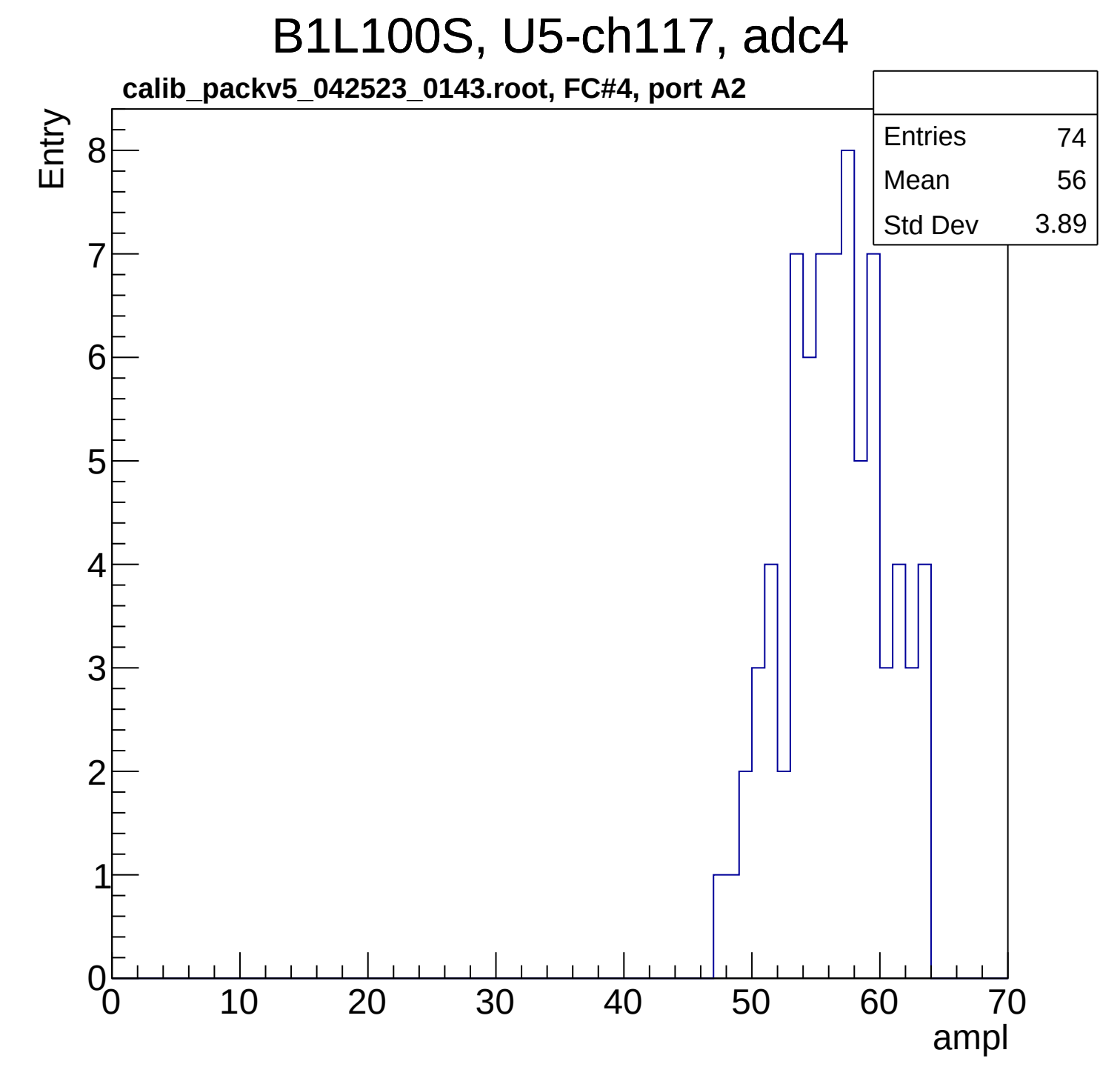

B1L100S, U5-ch116, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

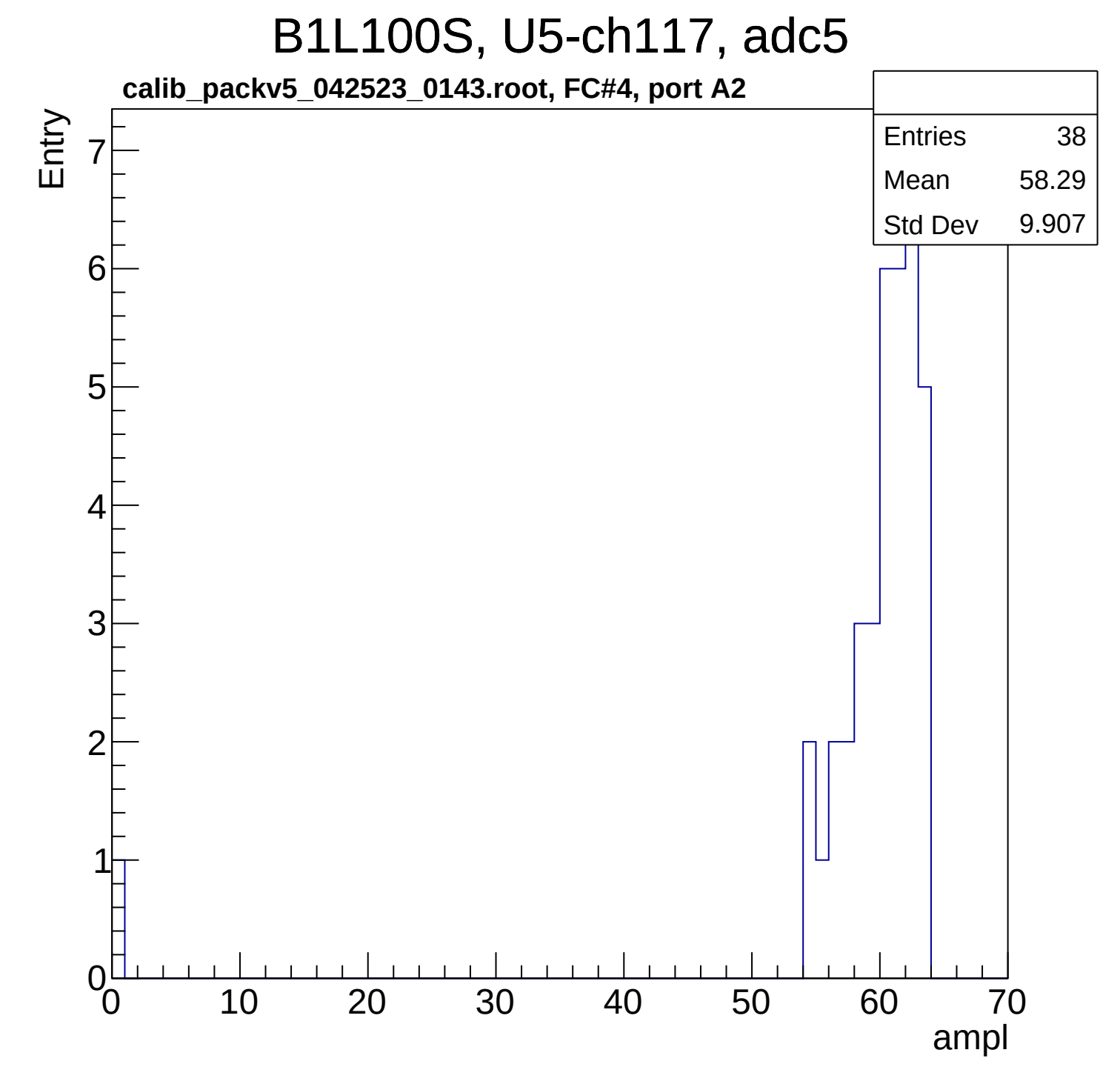

B1L100S, U5-ch117, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 29.58
Std Dev 4.988
Gaus mean : 30.8008
Gaus Width: 3.2123
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

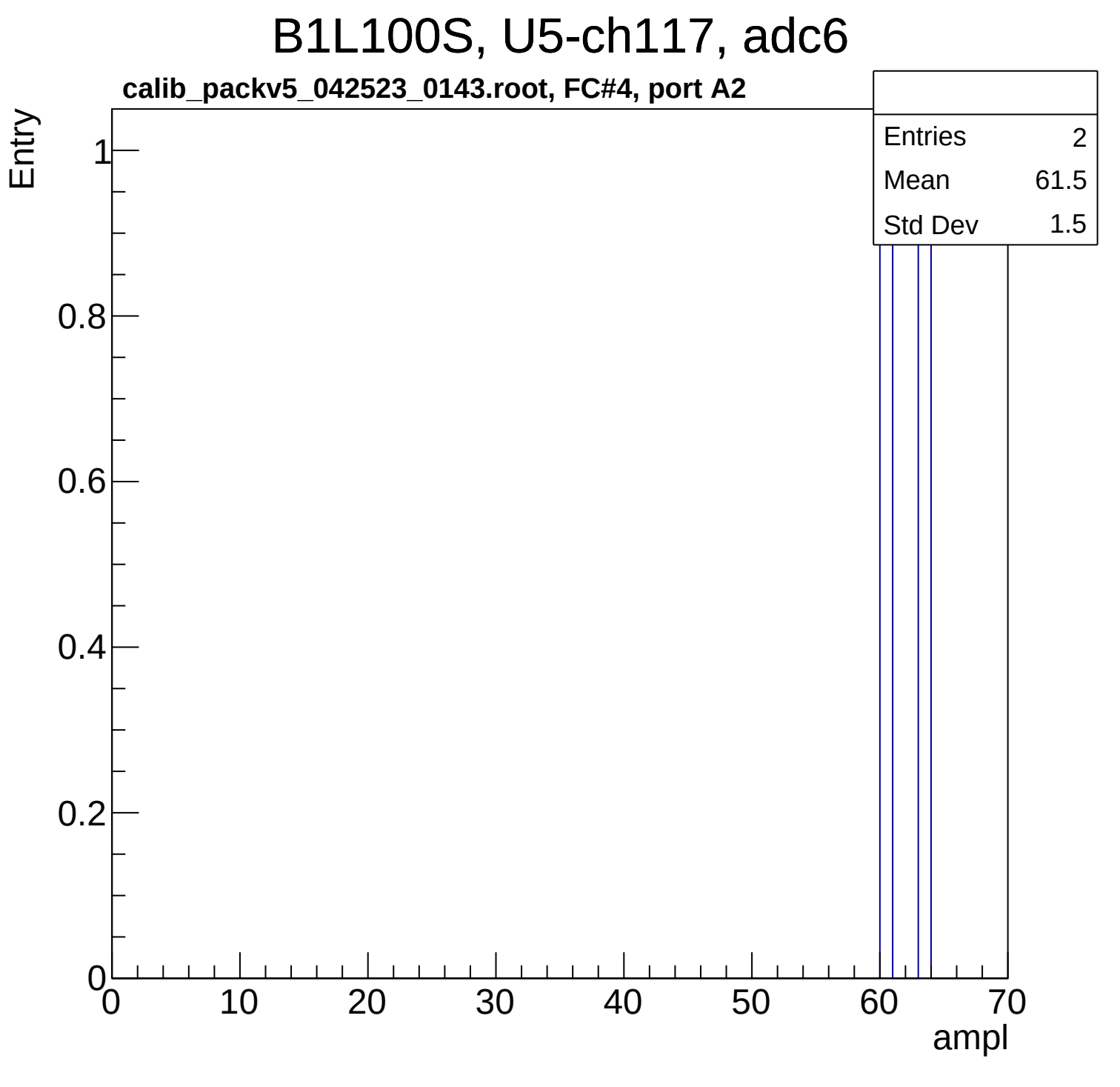

B1L100S, U5-ch117, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 36.16
Std Dev 3.494
Gaus mean : 37.0346
Gaus Width: 3.8947
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

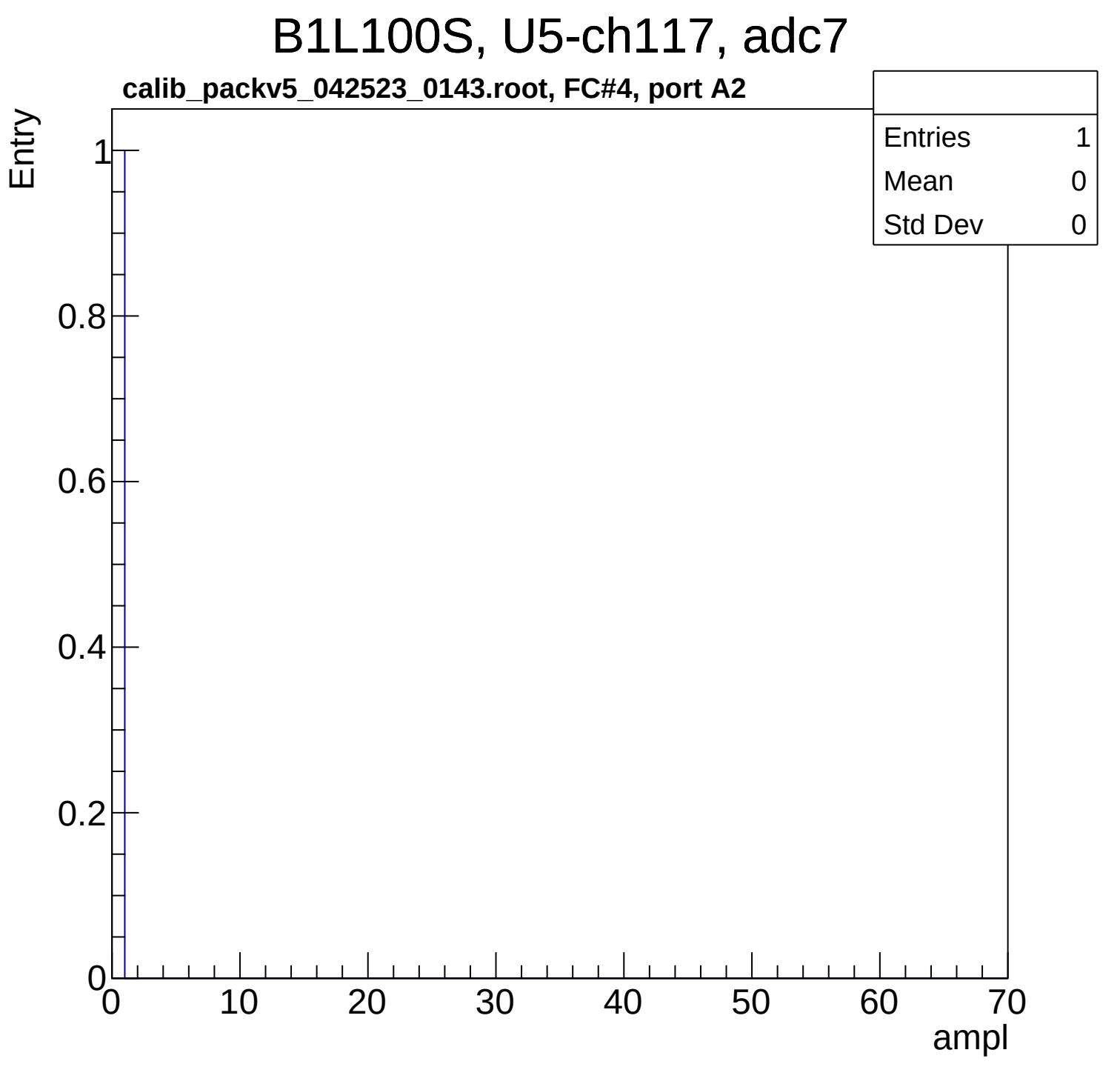

B1L100S, U5-ch117, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 76
Mean 42.25
Std Dev 3.732
Gaus mean : 43.3508
Gaus Width: 3.5877
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

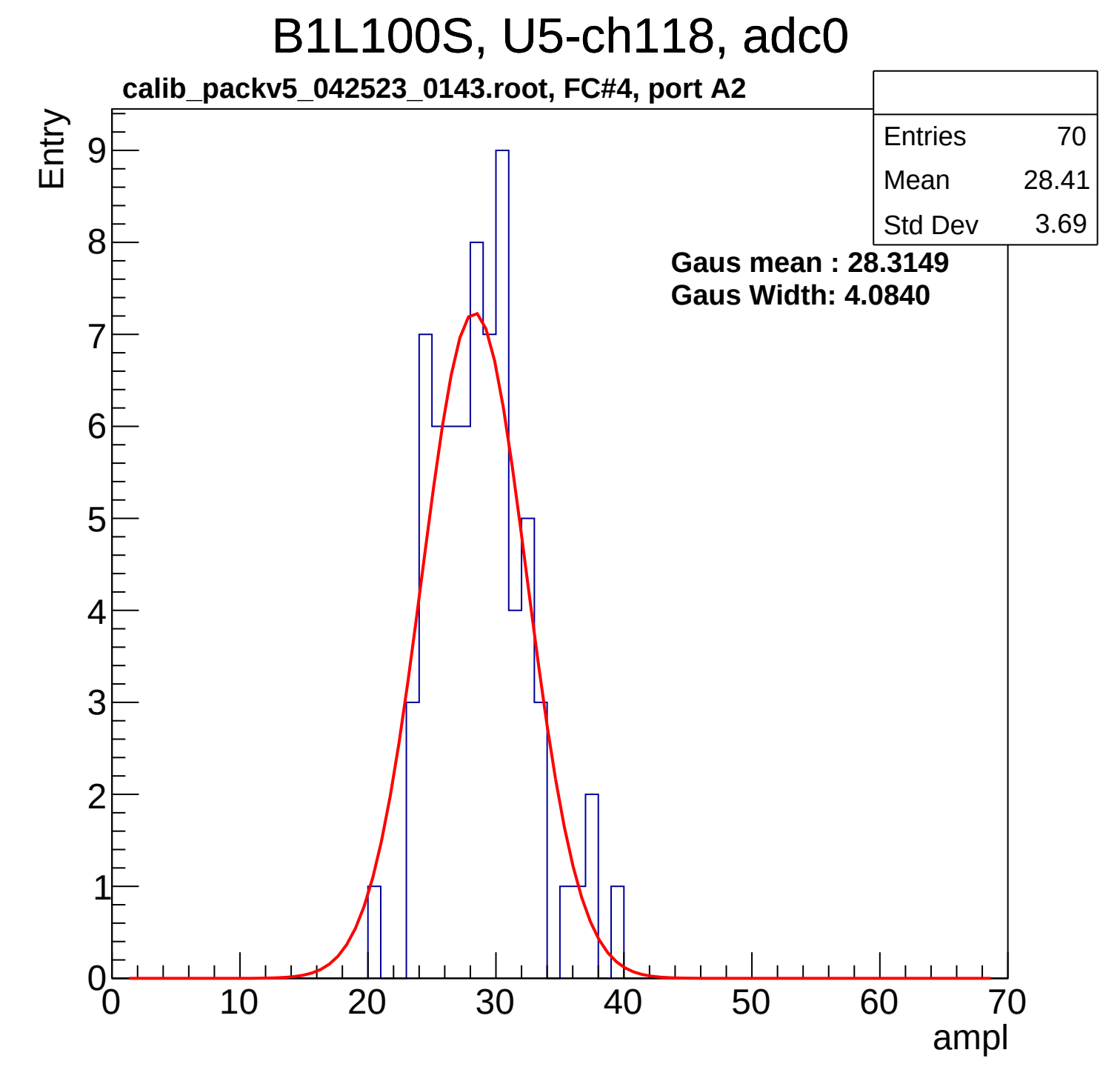

B1L100S, U5-ch117, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 49.54
Std Dev 3.688
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

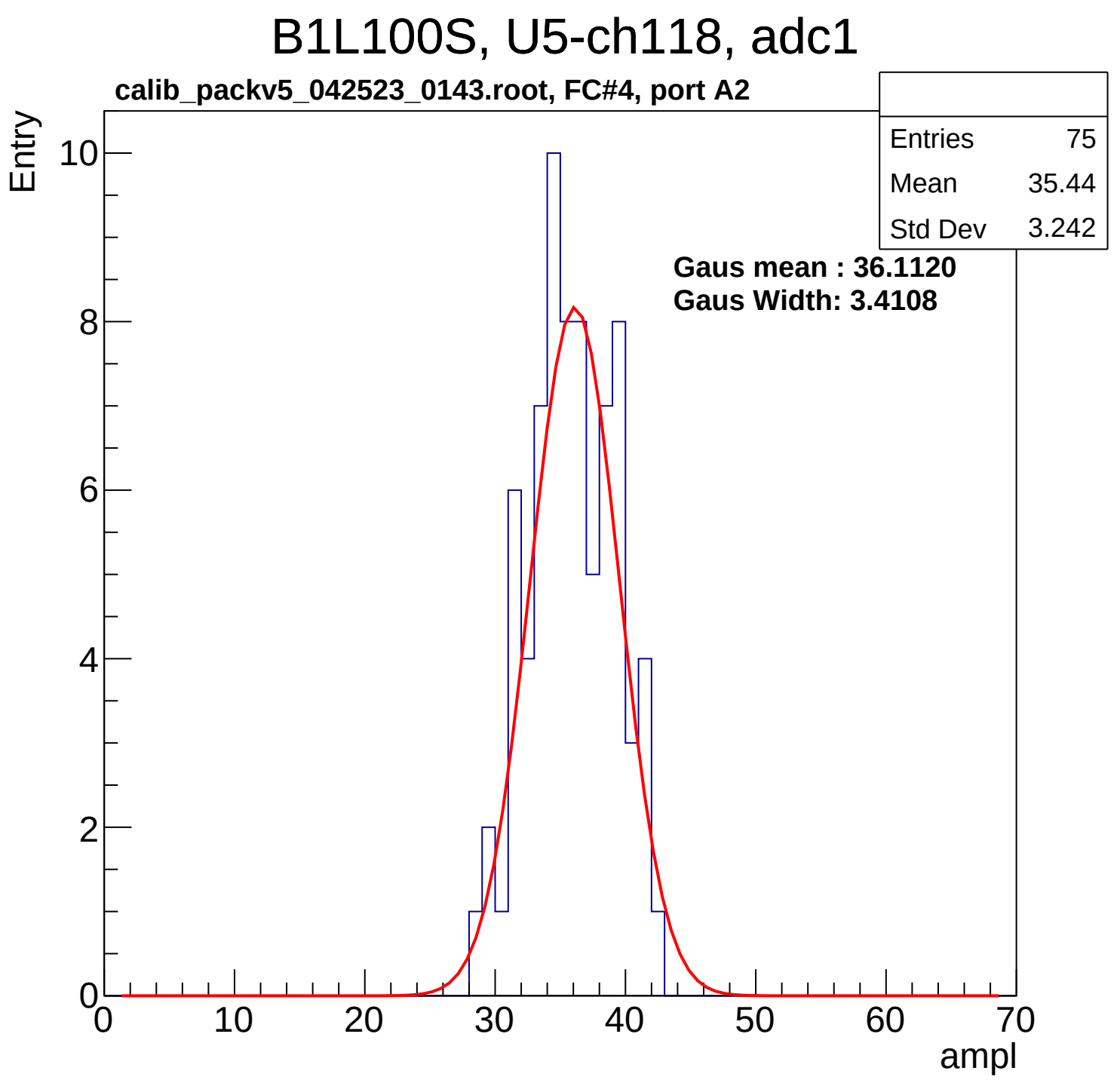

B1L100S, U5-ch117, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 74
Mean 56
Std Dev 3.89
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

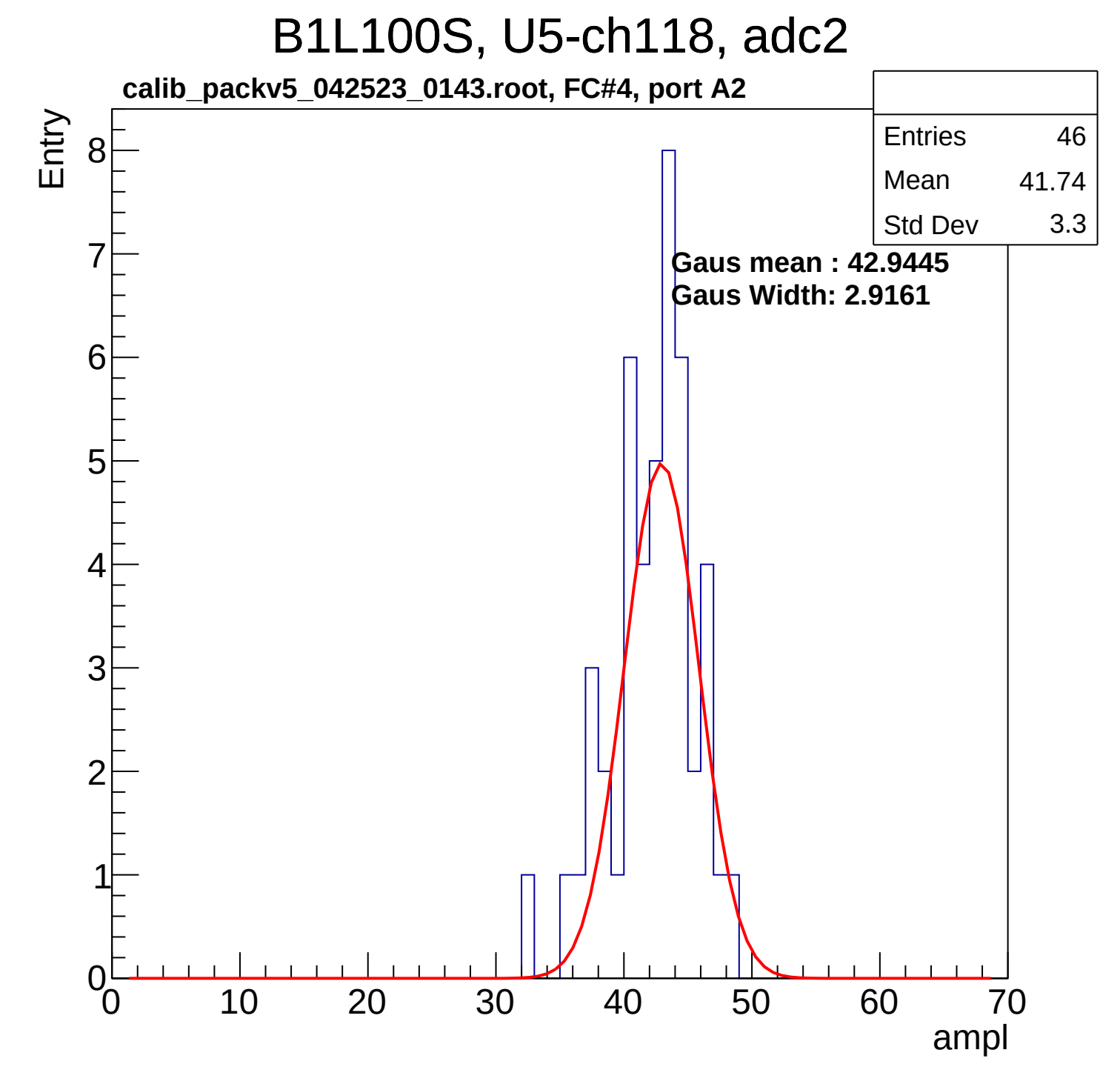

B1L100S, U5-ch117, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 38
Mean 58.29
Std Dev 9.907
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U5-ch117, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 61.5
Std Dev 1.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch117, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch118, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 28.41
Std Dev 3.69
Gaus mean : 28.3149
Gaus Width: 4.0840
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch118, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 75
Mean 35.44
Std Dev 3.242
Gaus mean : 36.1120
Gaus Width: 3.4108
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch118, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 46
Mean 41.74
Std Dev 3.3
Gaus mean : 42.9445
Gaus Width: 2.9161
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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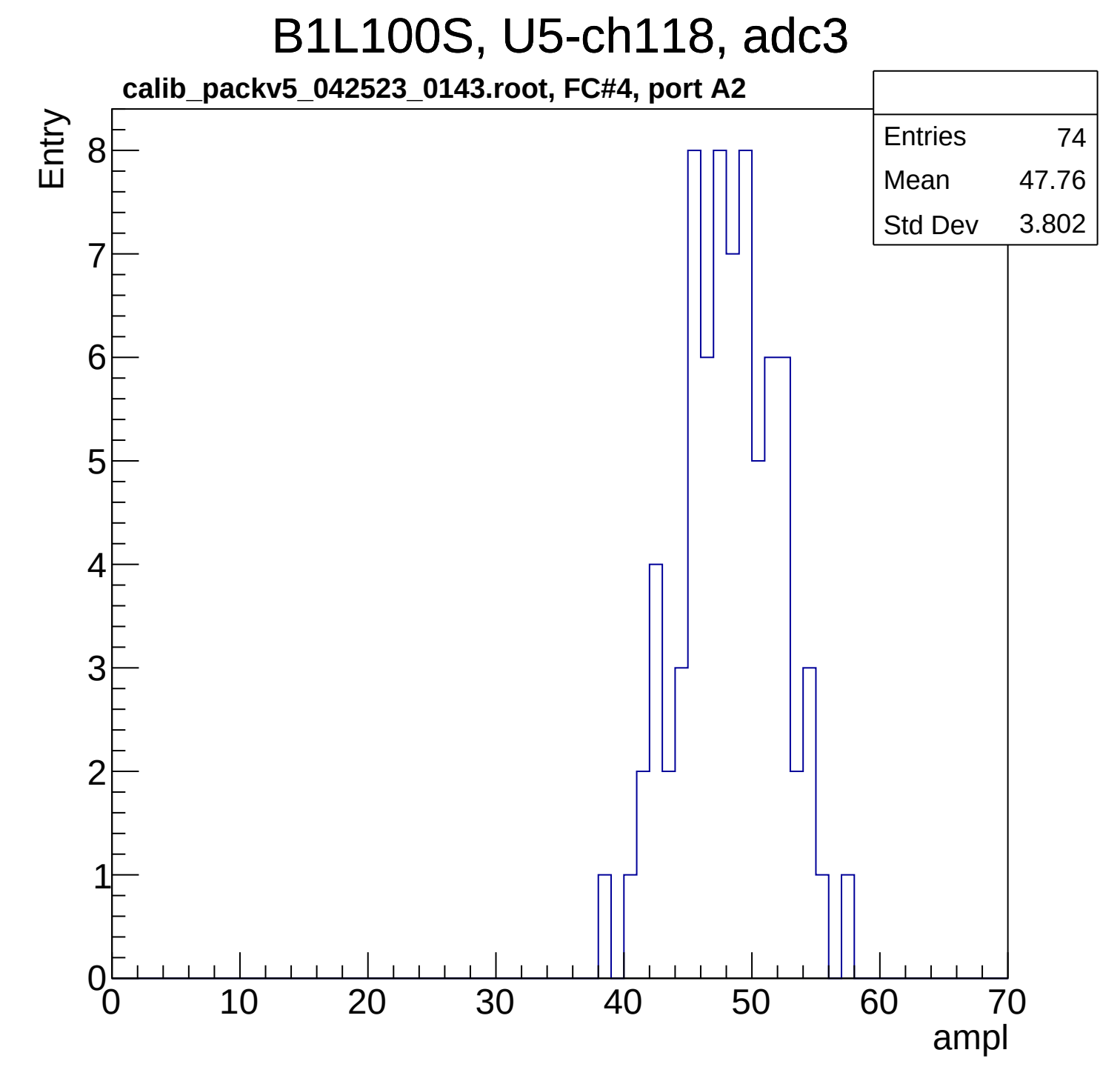
40
50
60
70


B1L100S, U5-ch118, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 74
Mean 47.76
Std Dev 3.802
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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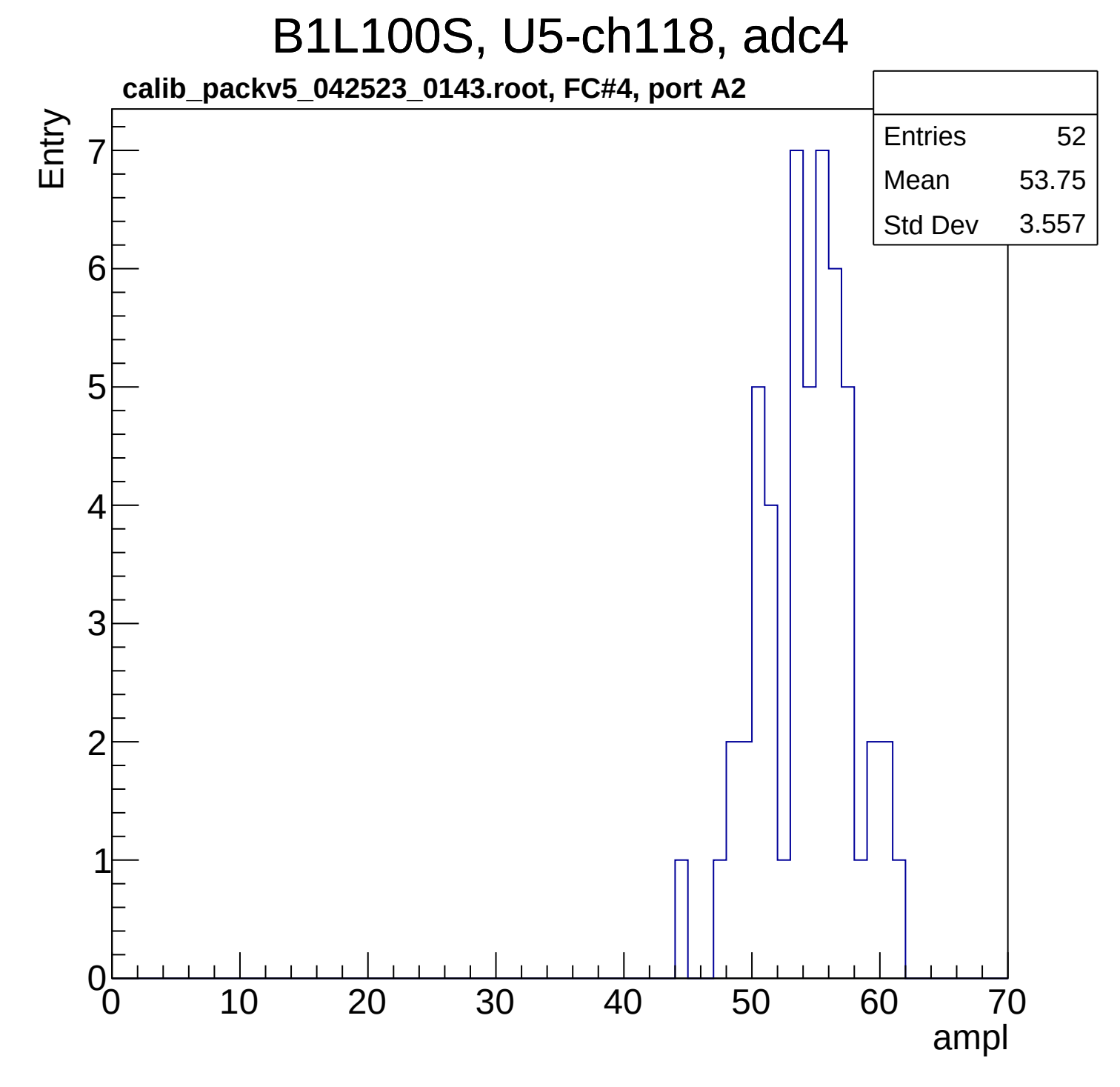
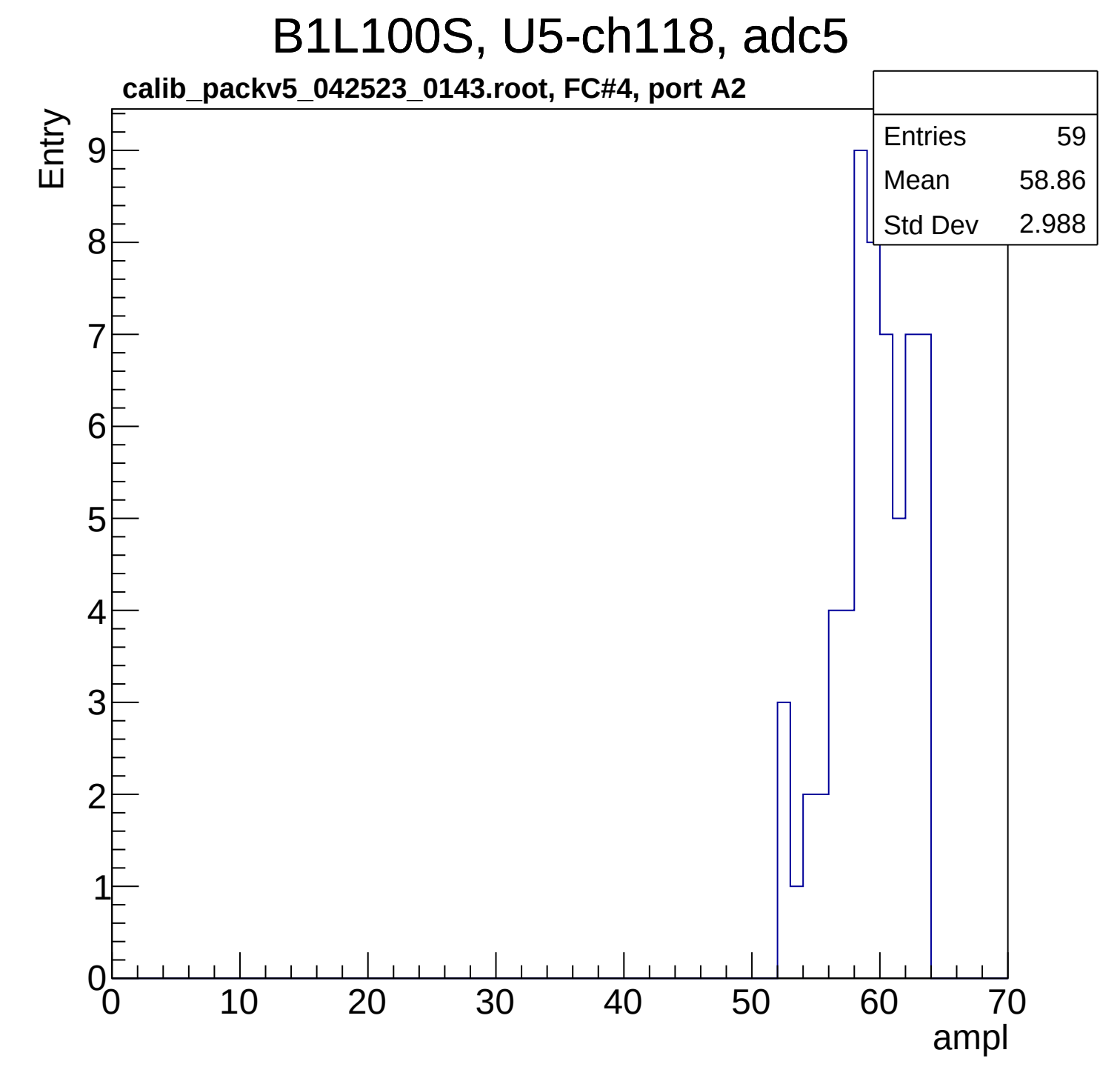
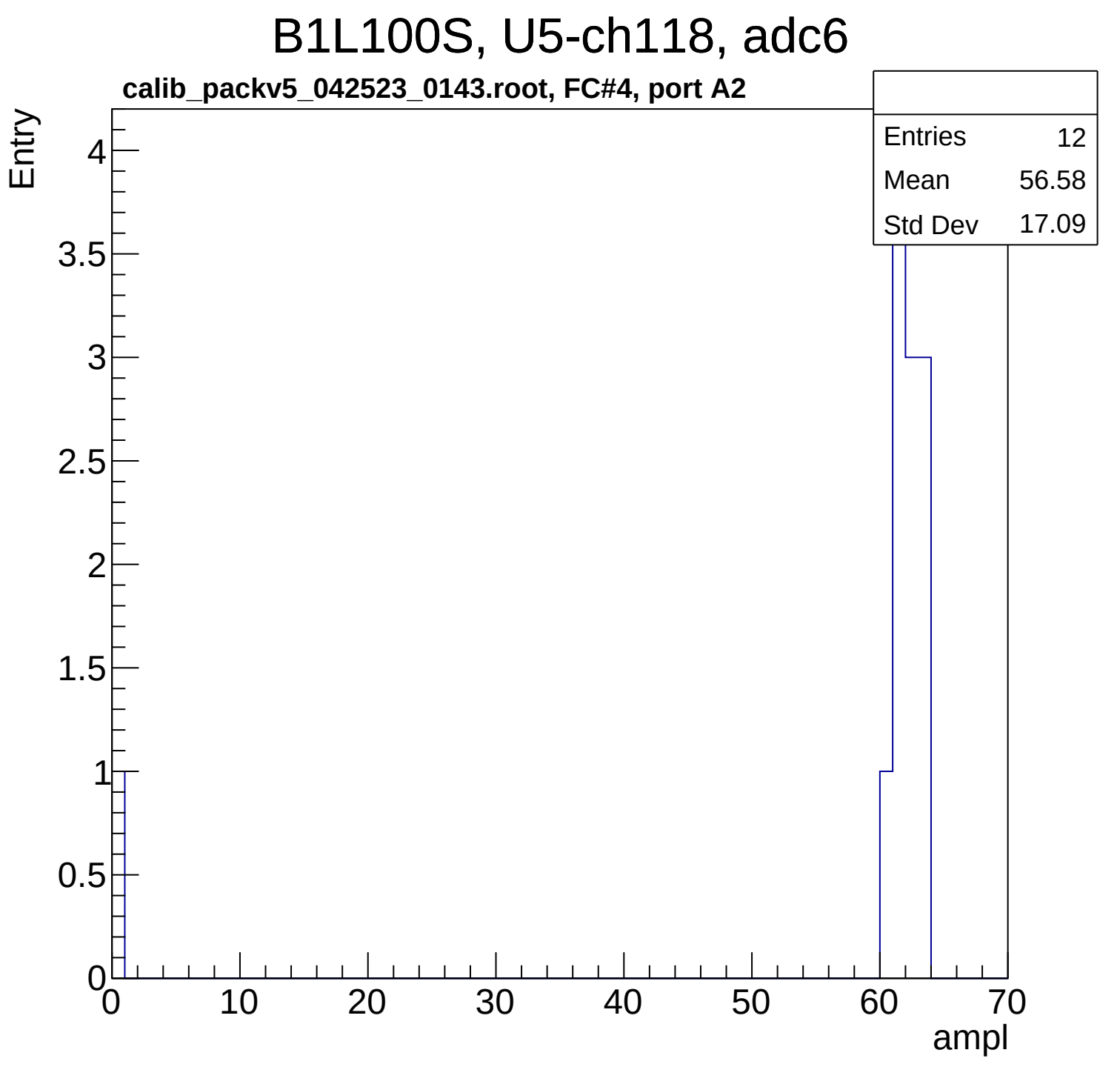

B1L100S, U5-ch118, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 52
Mean 53.75
Std Dev 3.557
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U5-ch118, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 58.86
Std Dev 2.988
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch118, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 12
Mean 56.58
Std Dev 17.09
Entry
ampl
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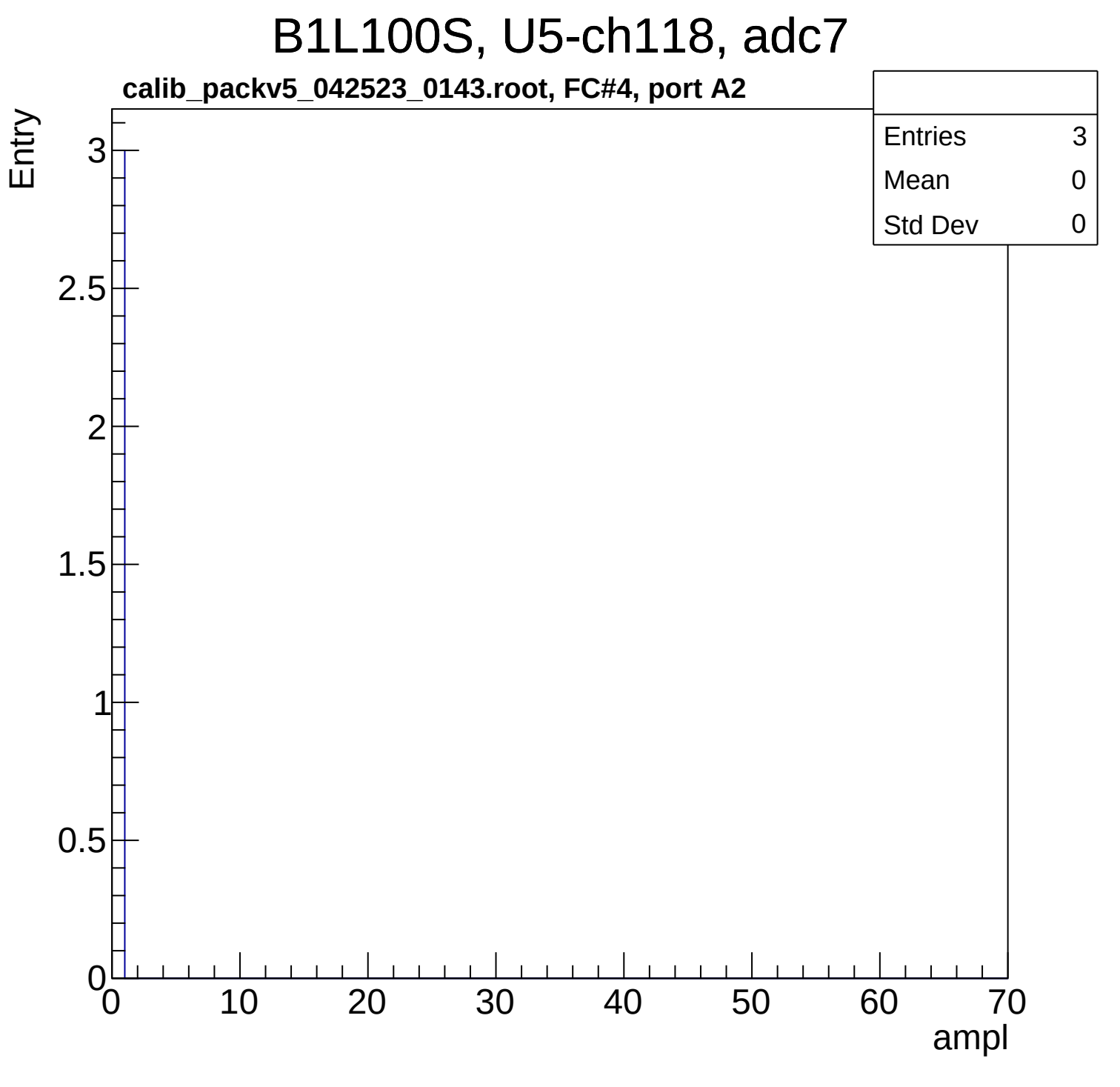
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L100S, U5-ch118, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 0
Std Dev 0
Entry
0
0.5
1
1.5
2
2.5
3
0
10
20
30
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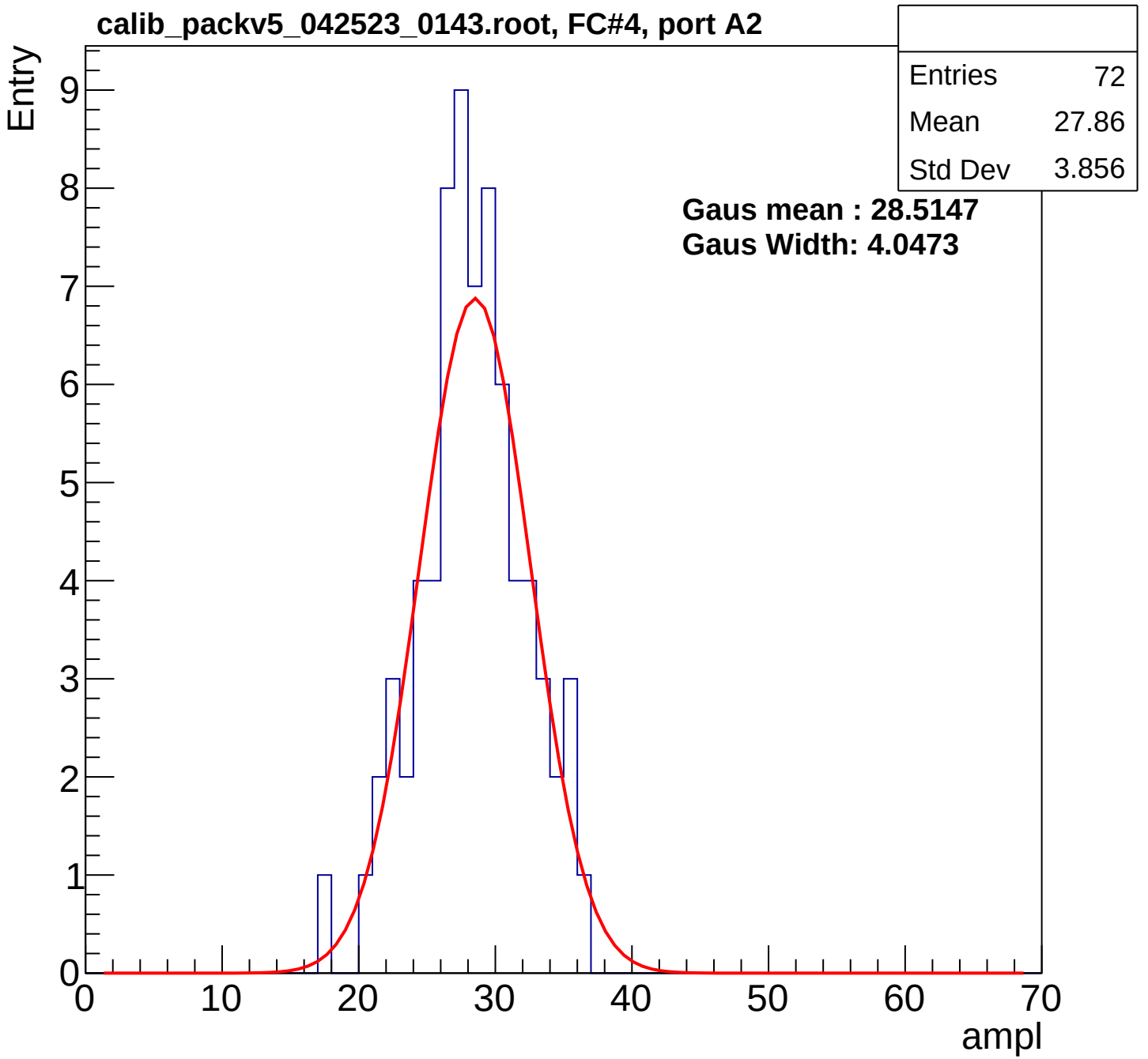
50
60
70
ampl


B1L100S, U5-ch119, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 27.86
Std Dev 3.856
Gaus mean : 28.5147
Gaus Width: 4.0473
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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20
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40
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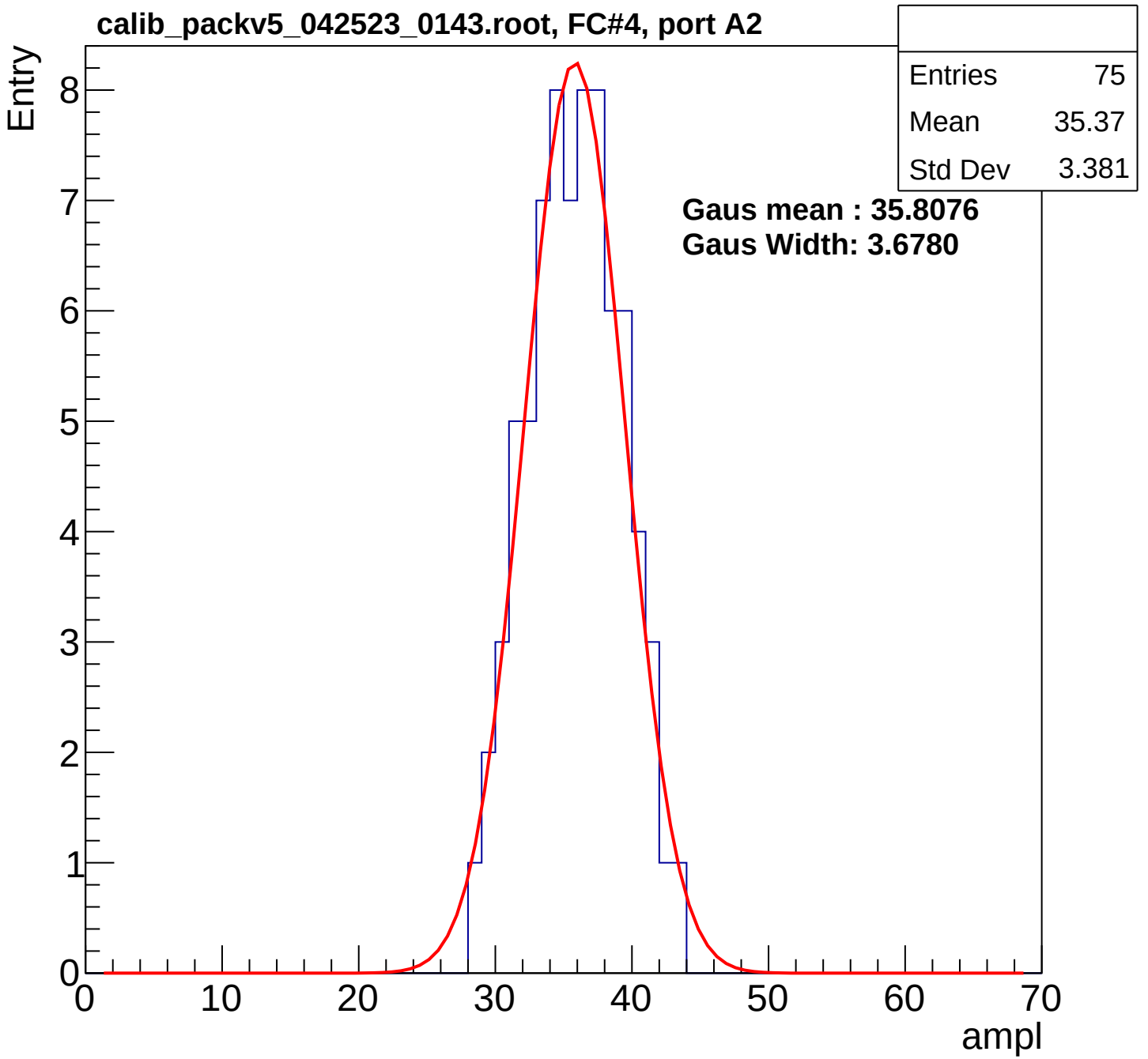
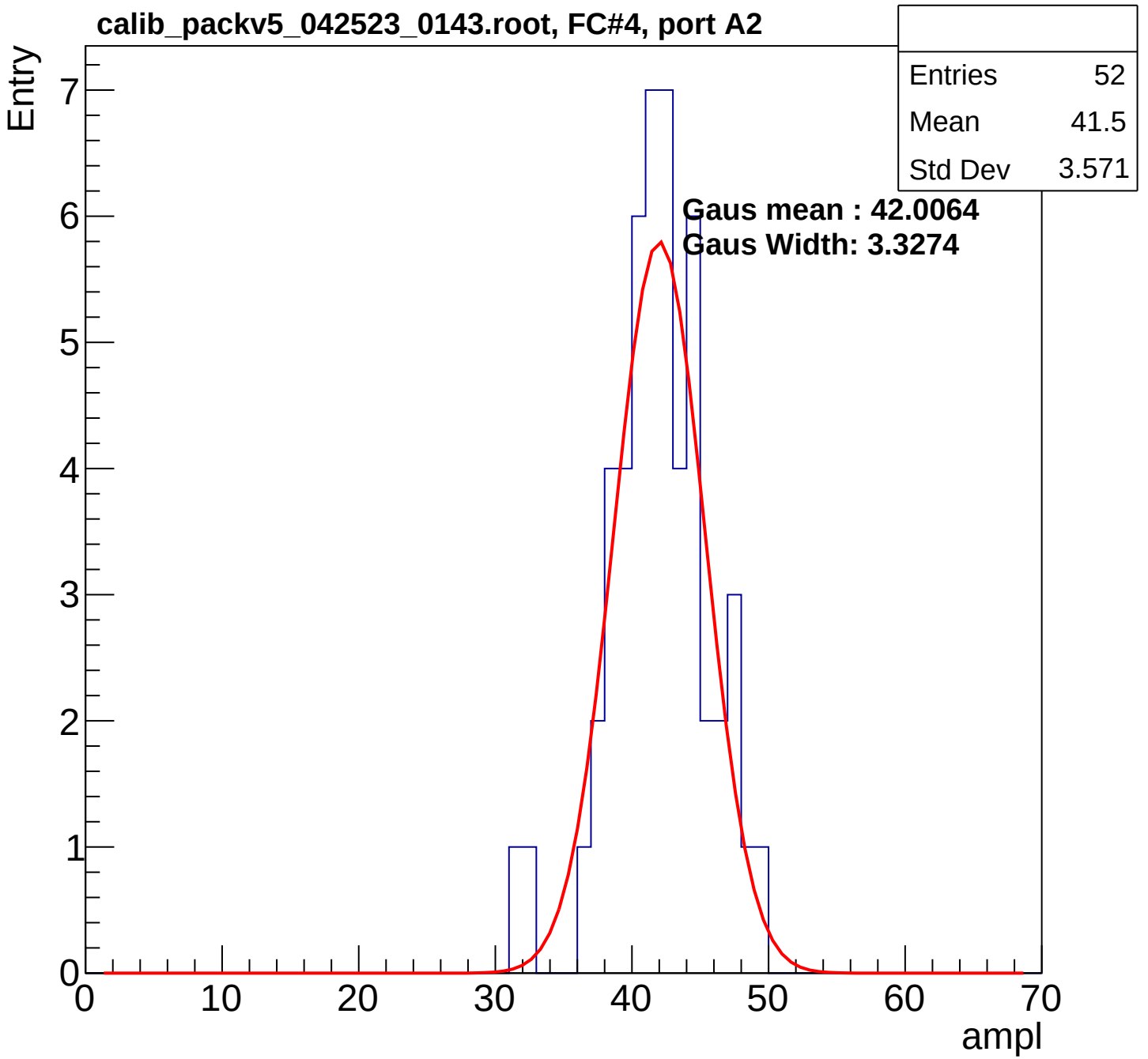
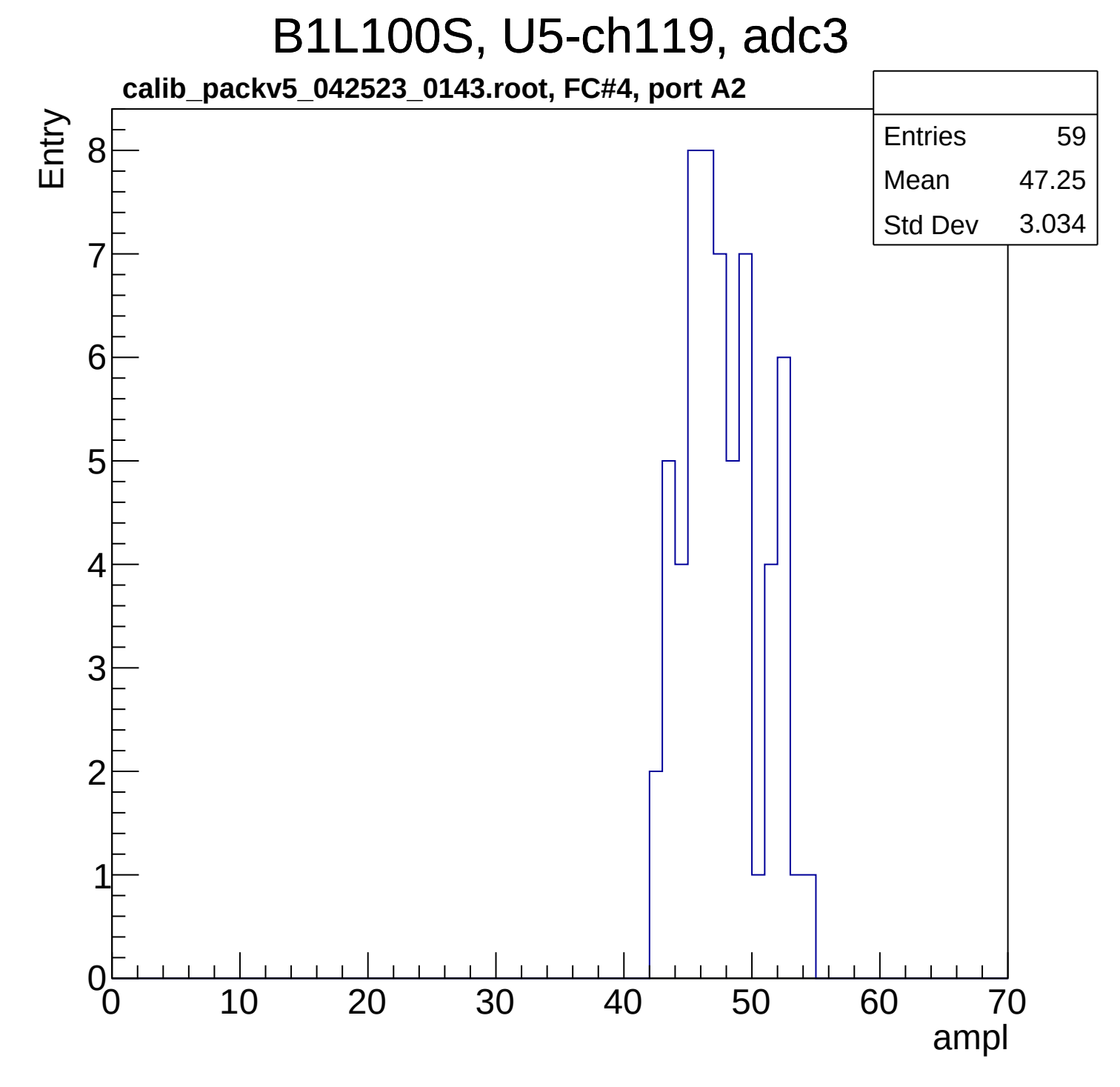
60
70


B1L100S, U5-ch119, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 75
Mean 35.37
Std Dev 3.381
Gaus mean : 35.8076
Gaus Width: 3.6780
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch119, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 52
Mean 41.5
Std Dev 3.571
Gaus mean : 42.0064
Gaus Width: 3.3274
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U5-ch119, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 47.25
Std Dev 3.034
Entry
ampl
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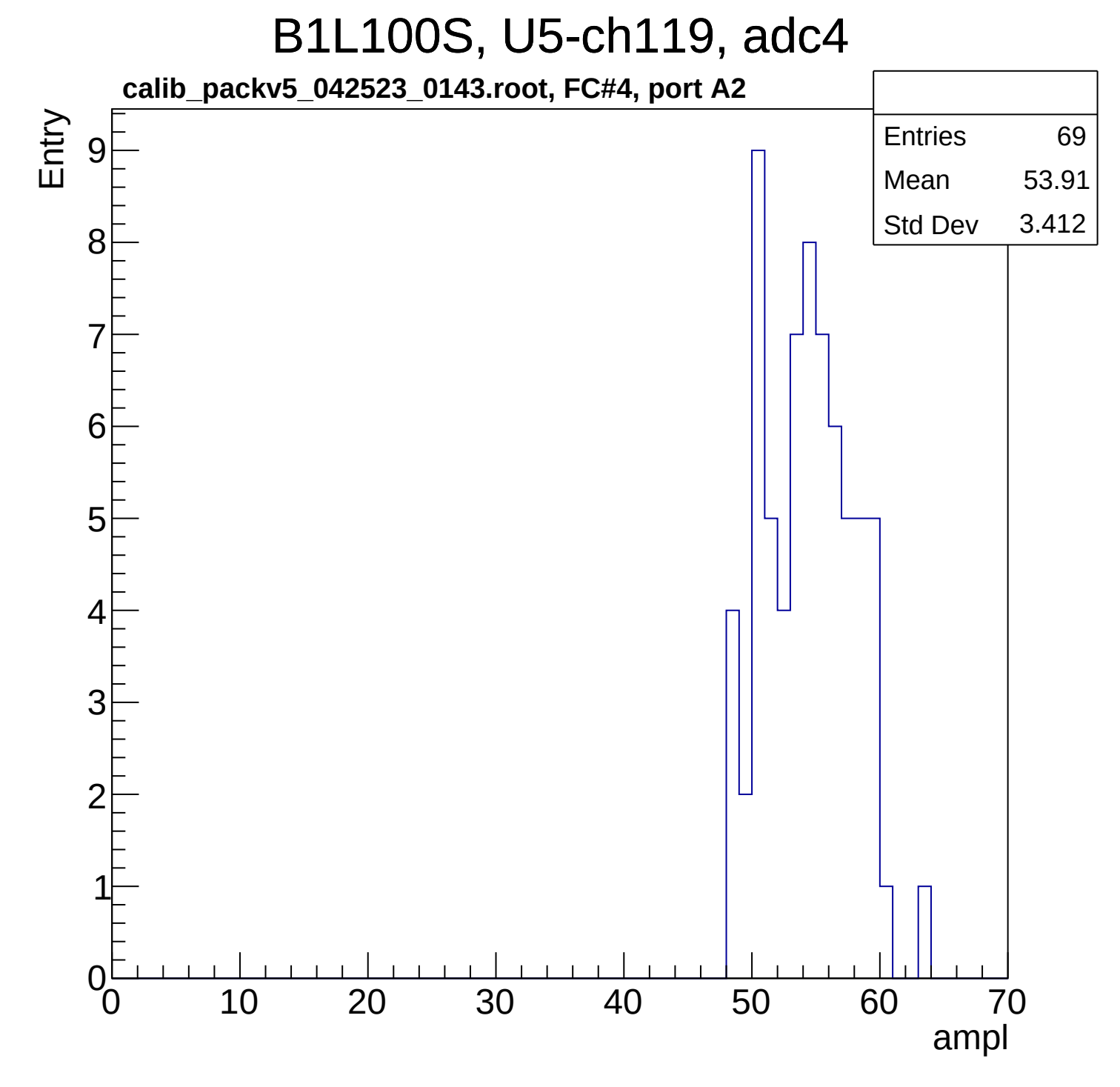
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch119, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 53.91
Std Dev 3.412
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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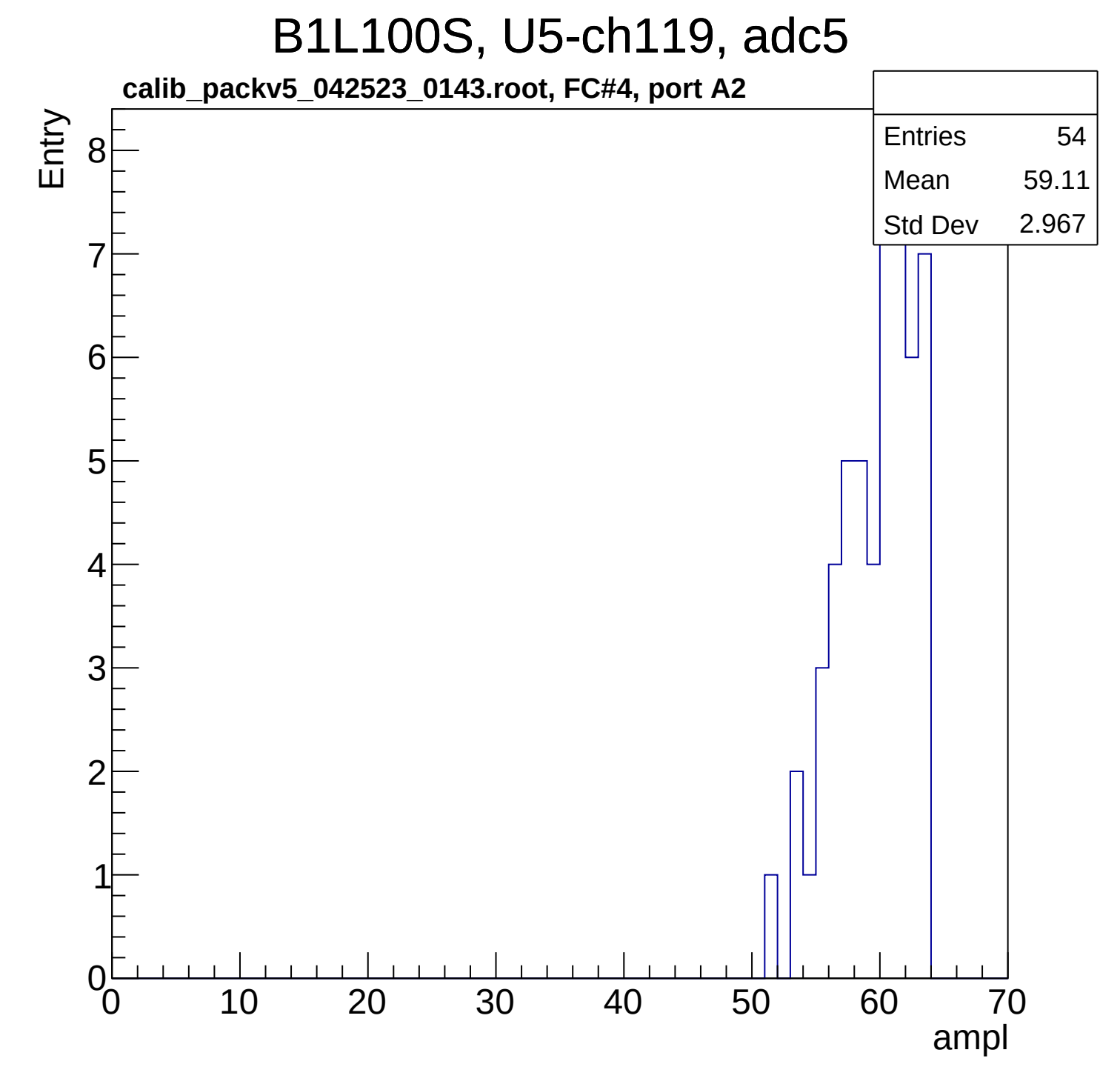
70


B1L100S, U5-ch119, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 59.11
Std Dev 2.967
Entry
ampl
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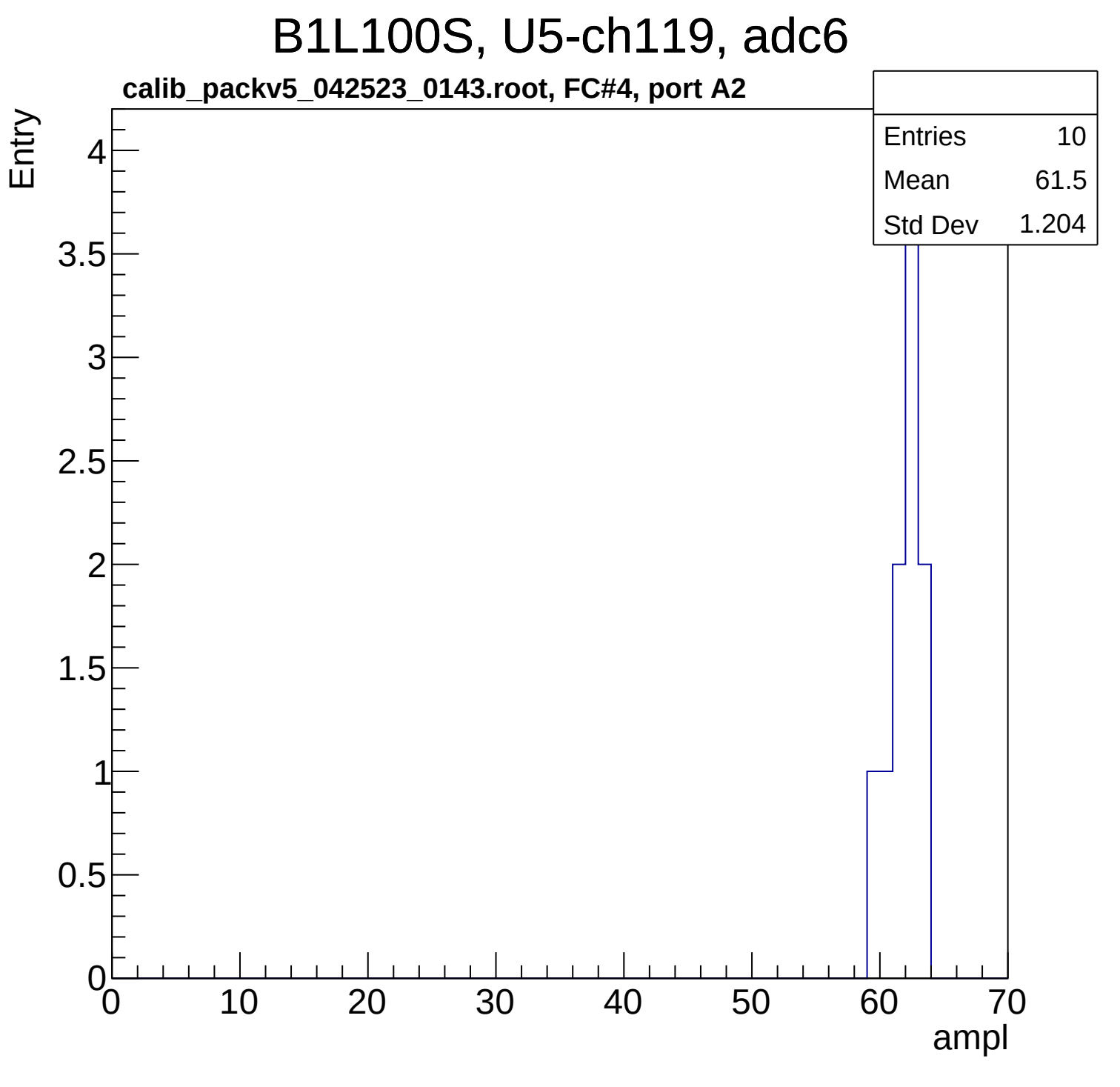
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch119, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 10
Mean 61.5
Std Dev 1.204
Entry
ampl
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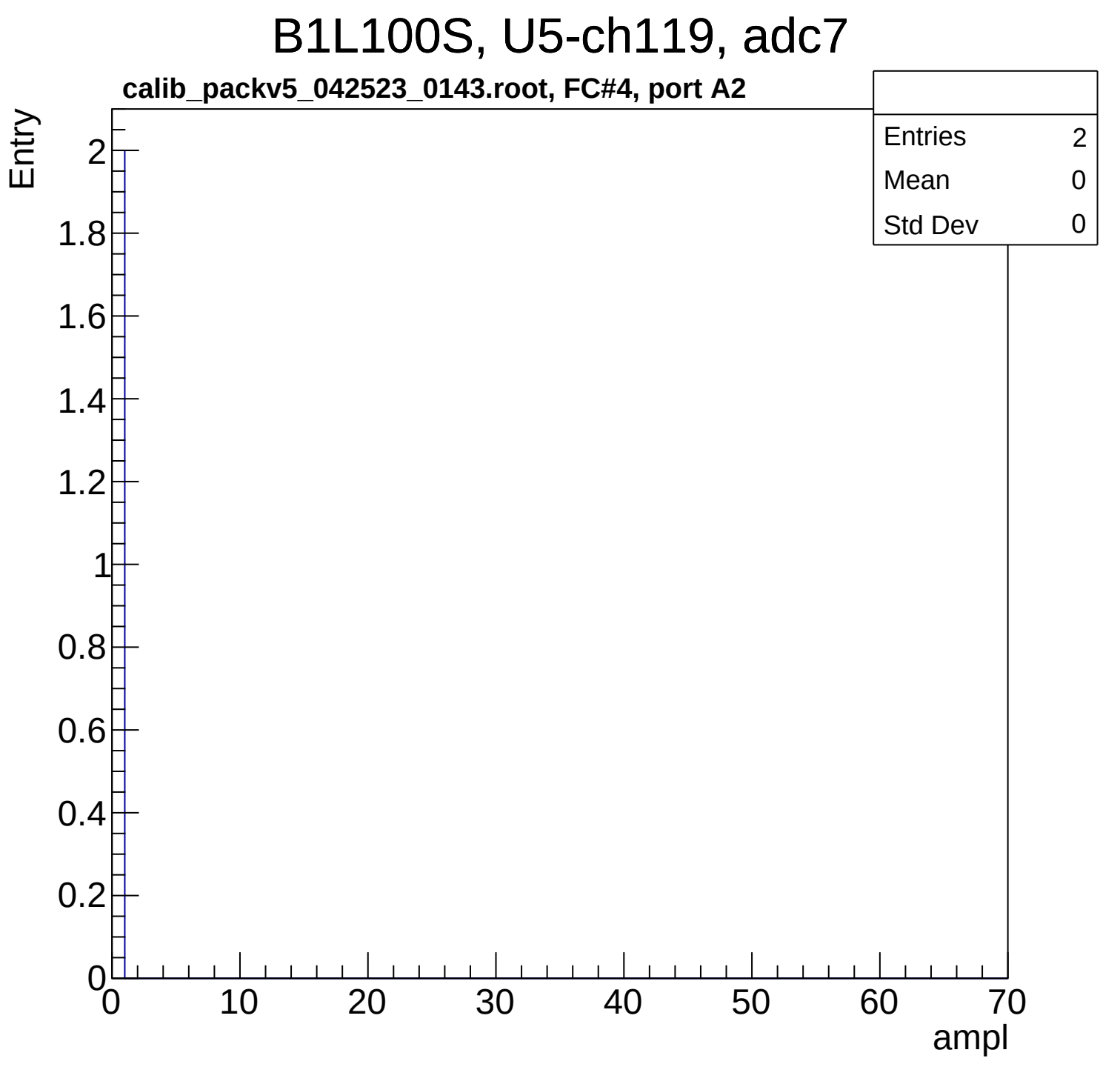
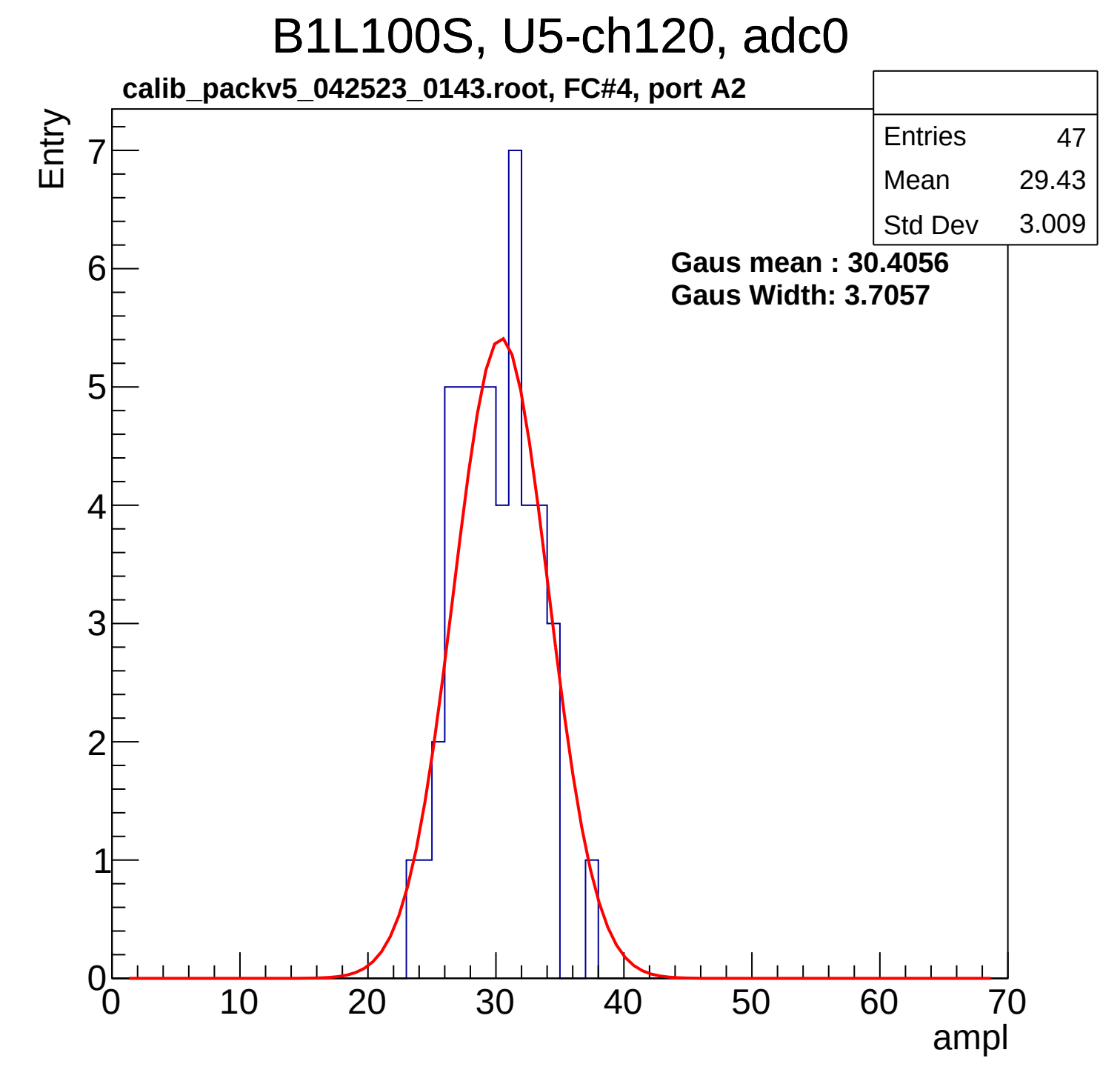
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L100S, U5-ch119, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch120, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 47
Mean 29.43
Std Dev 3.009
Gaus mean : 30.4056
Gaus Width: 3.7057
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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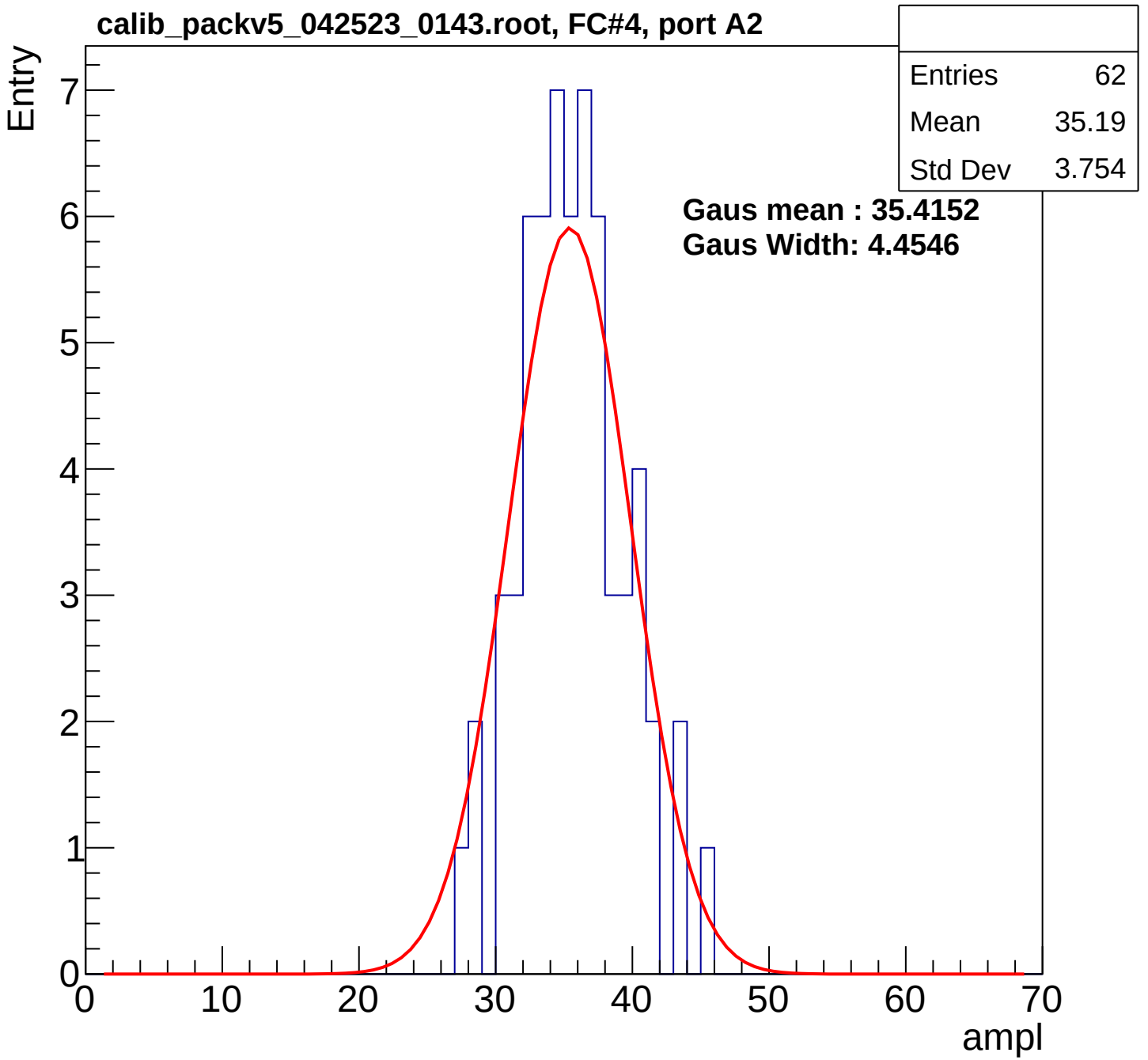
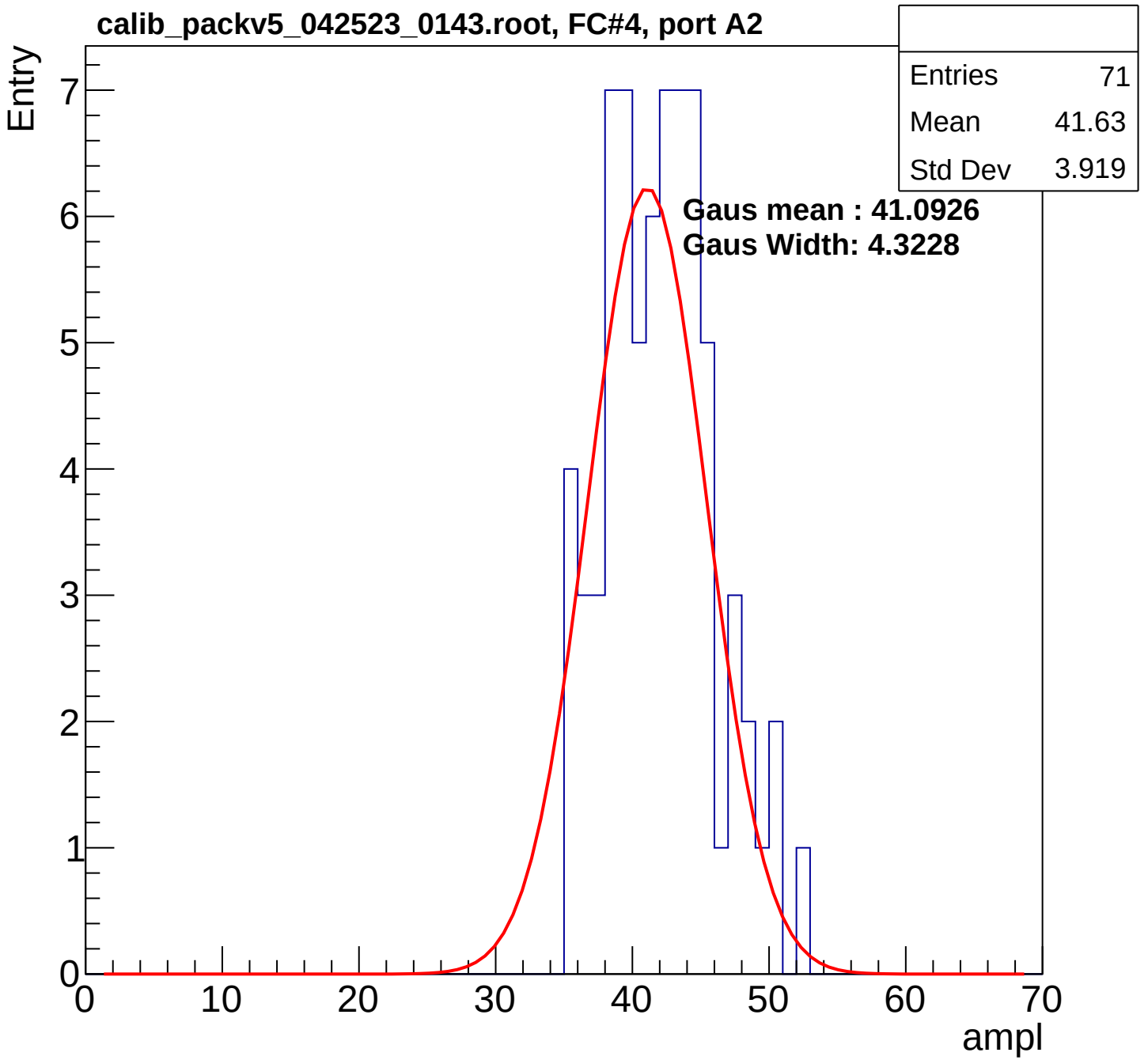
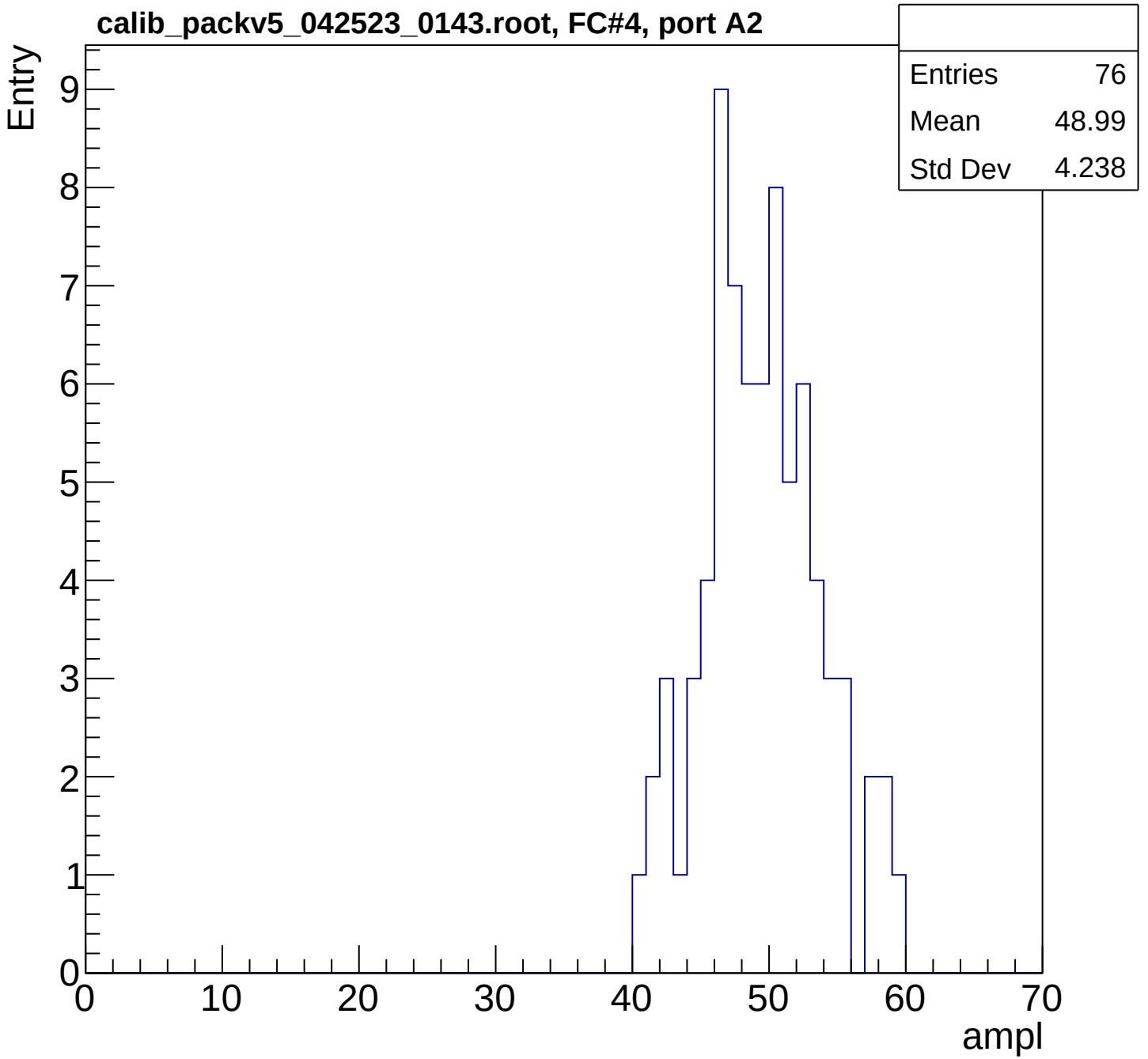
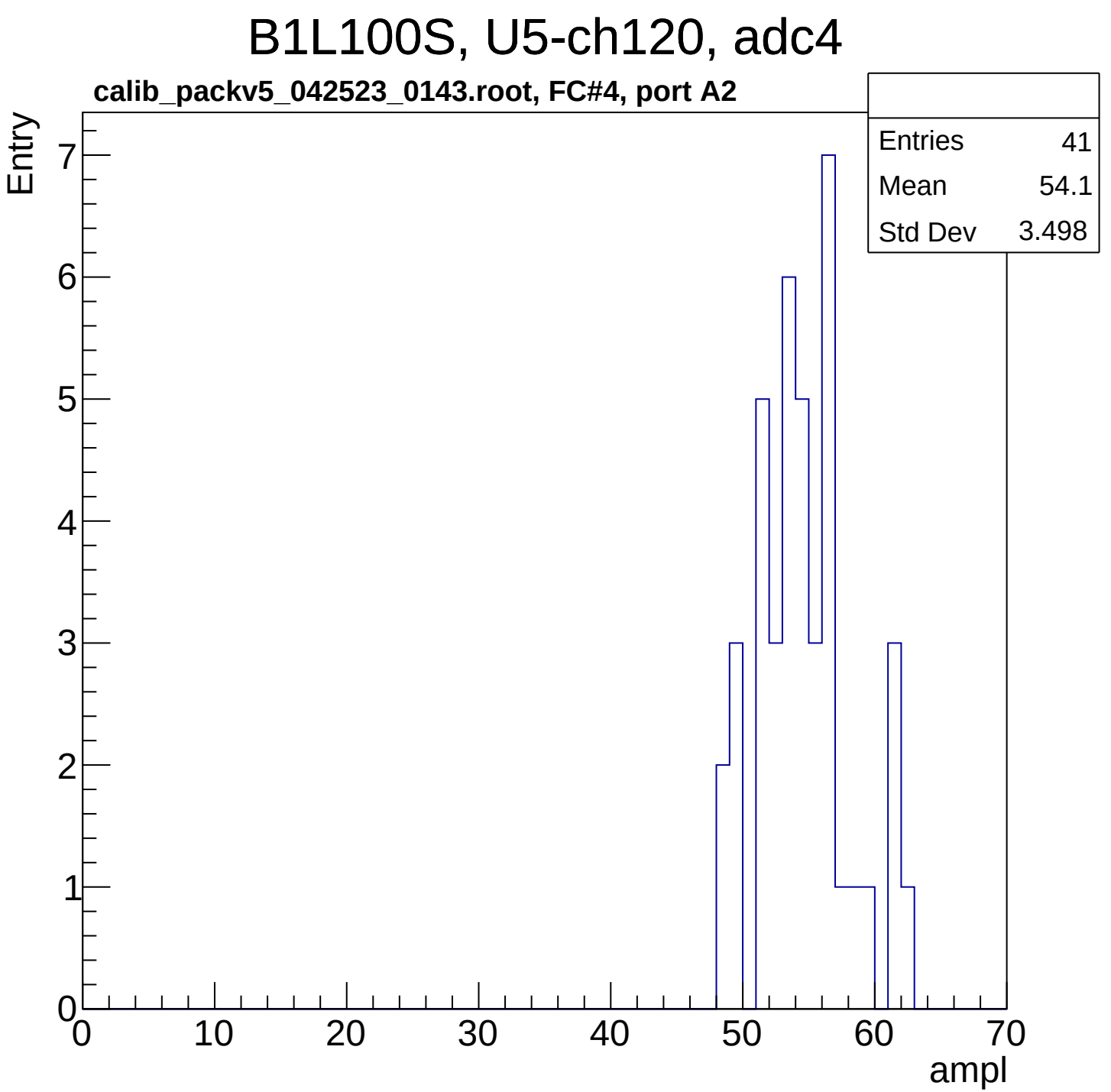
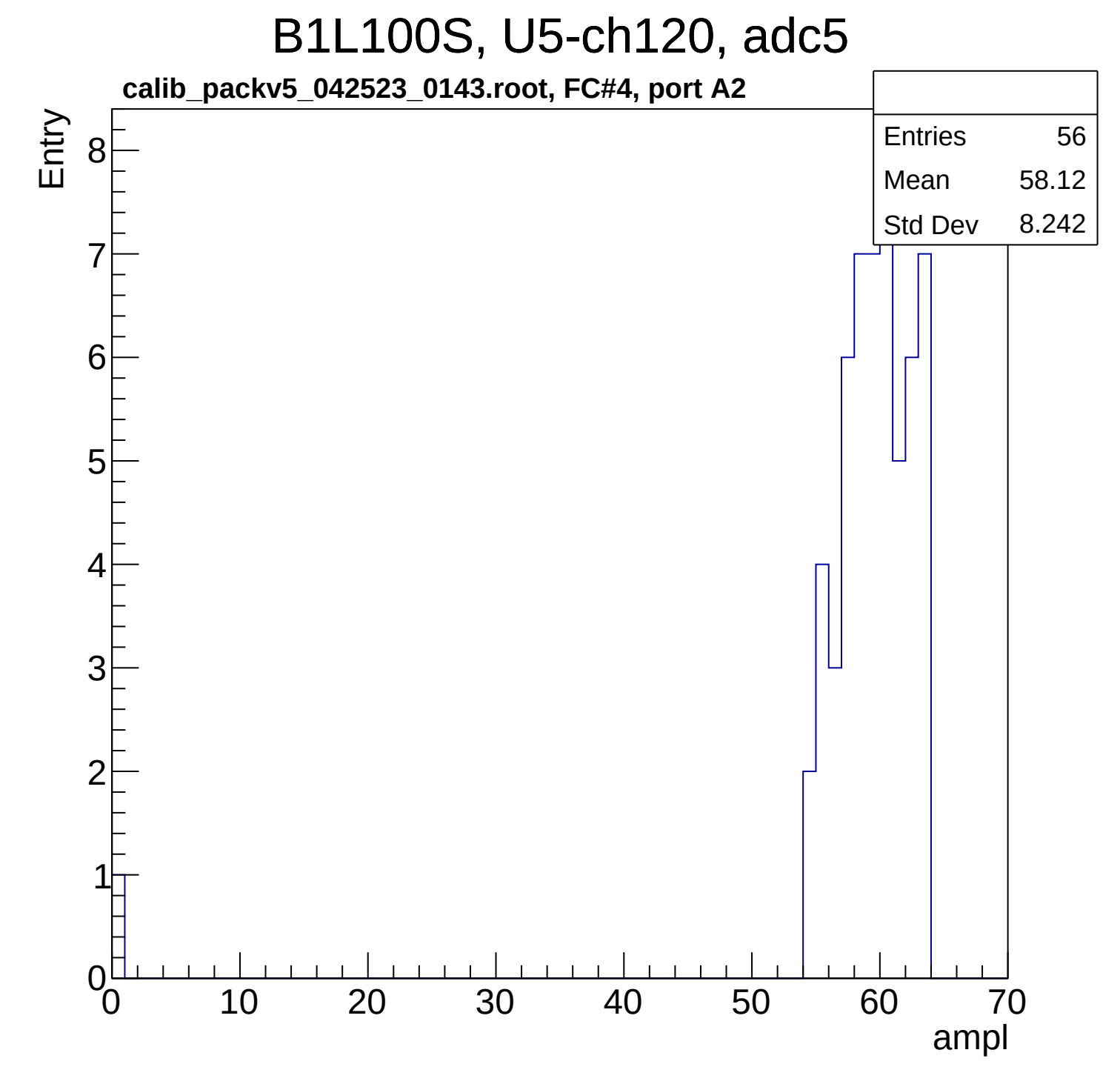
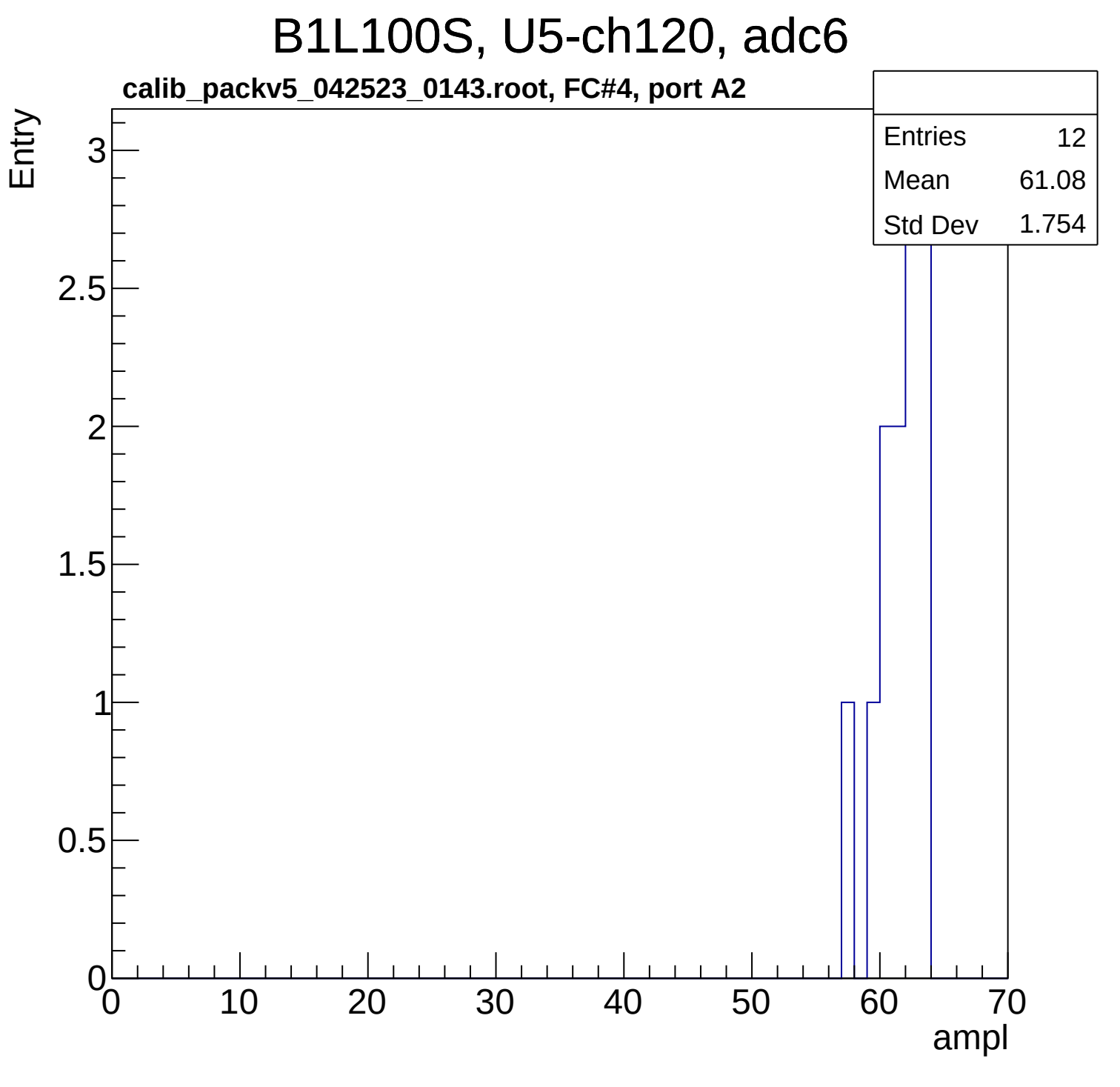

B1L100S, U5-ch120, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 35.19
Std Dev 3.754
Gaus mean : 35.4152
Gaus Width: 4.4546
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

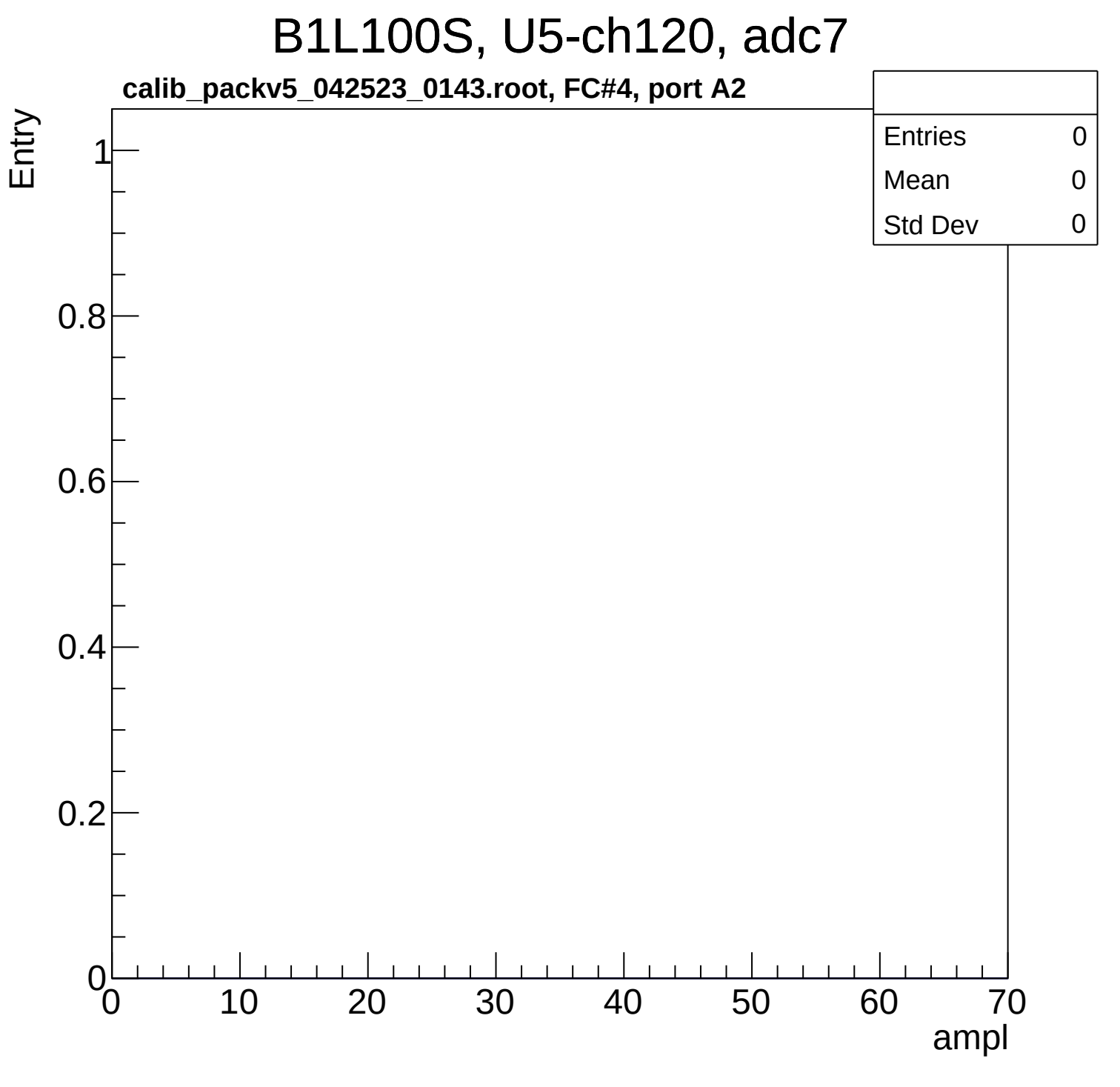

B1L100S, U5-ch120, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 41.63
Std Dev 3.919
Gaus mean : 41.0926
Gaus Width: 4.3228
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

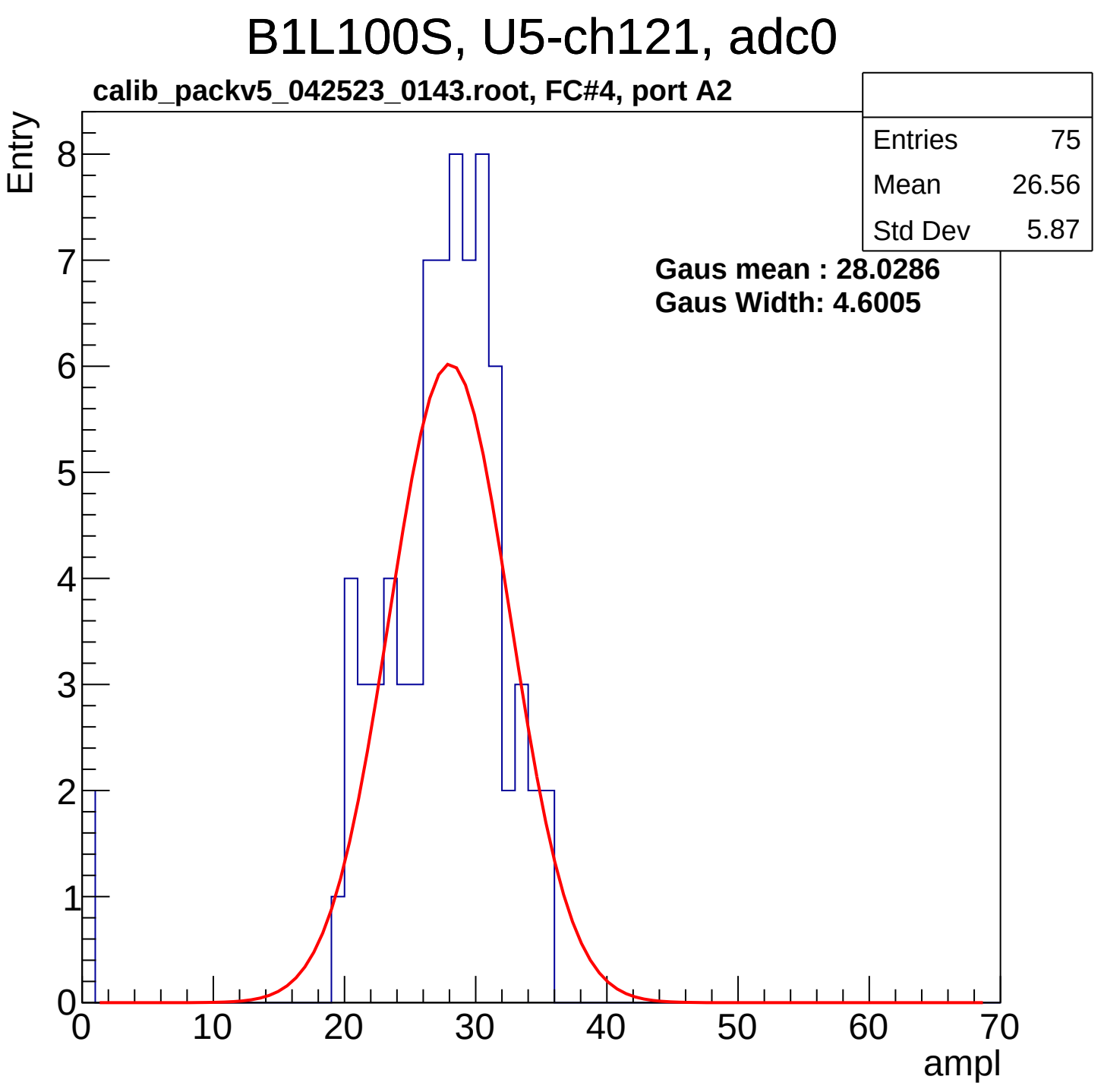

B1L100S, U5-ch120, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 76
Mean 48.99
Std Dev 4.238
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

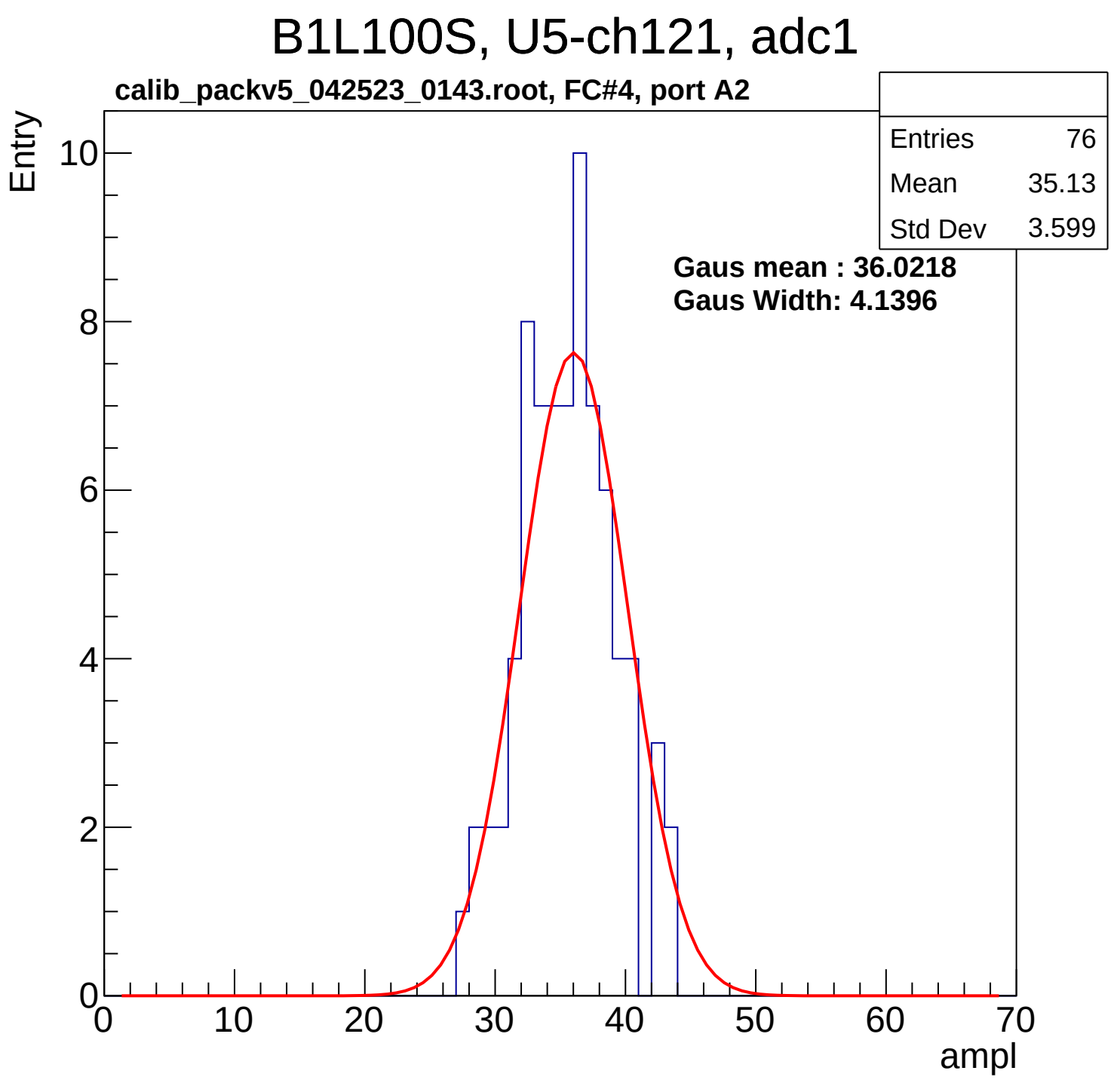

B1L100S, U5-ch120, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 41
Mean 54.1
Std Dev 3.498
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

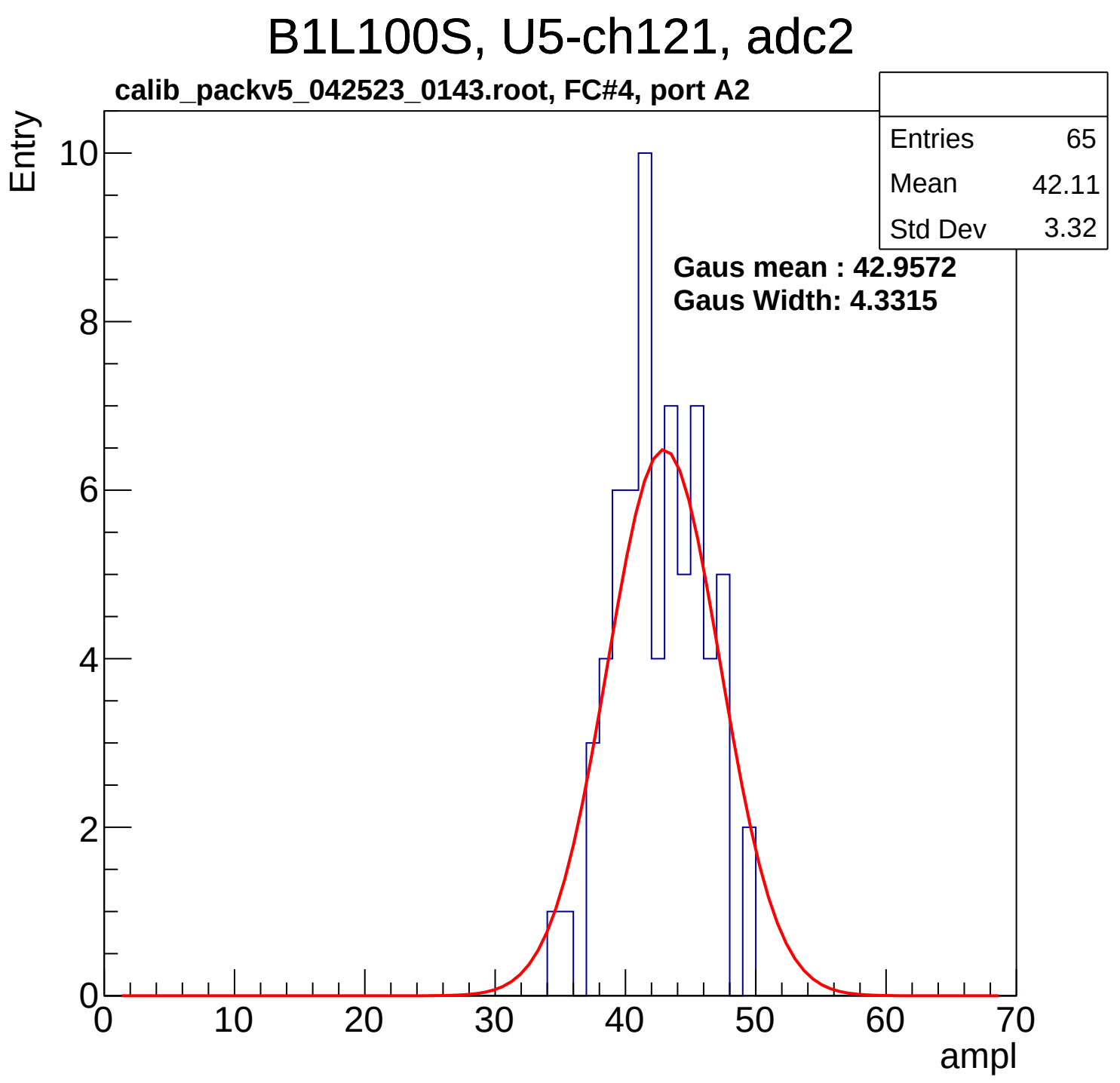

B1L100S, U5-ch120, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 58.12
Std Dev 8.242
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

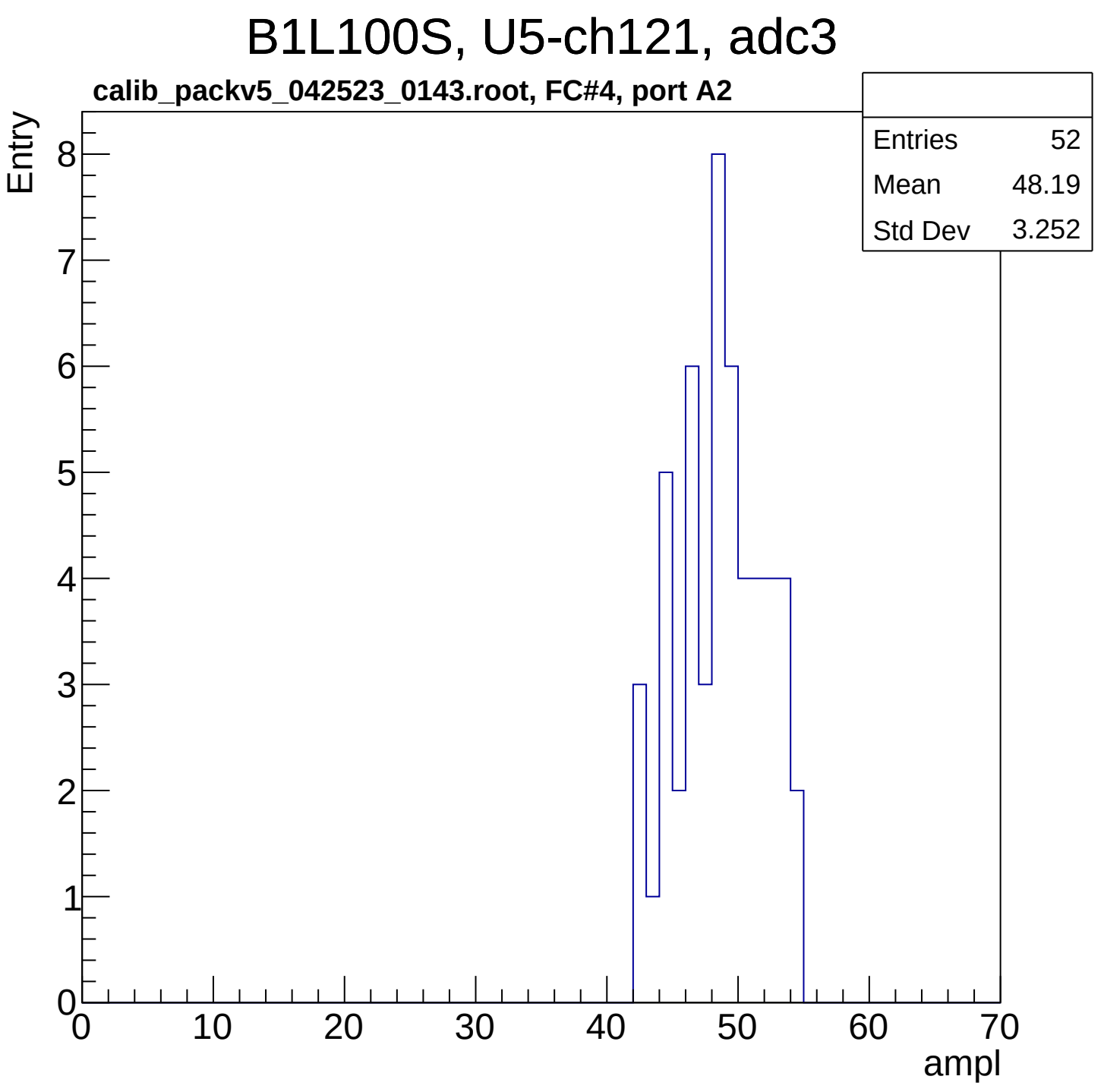

B1L100S, U5-ch120, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 12
Mean 61.08
Std Dev 1.754
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

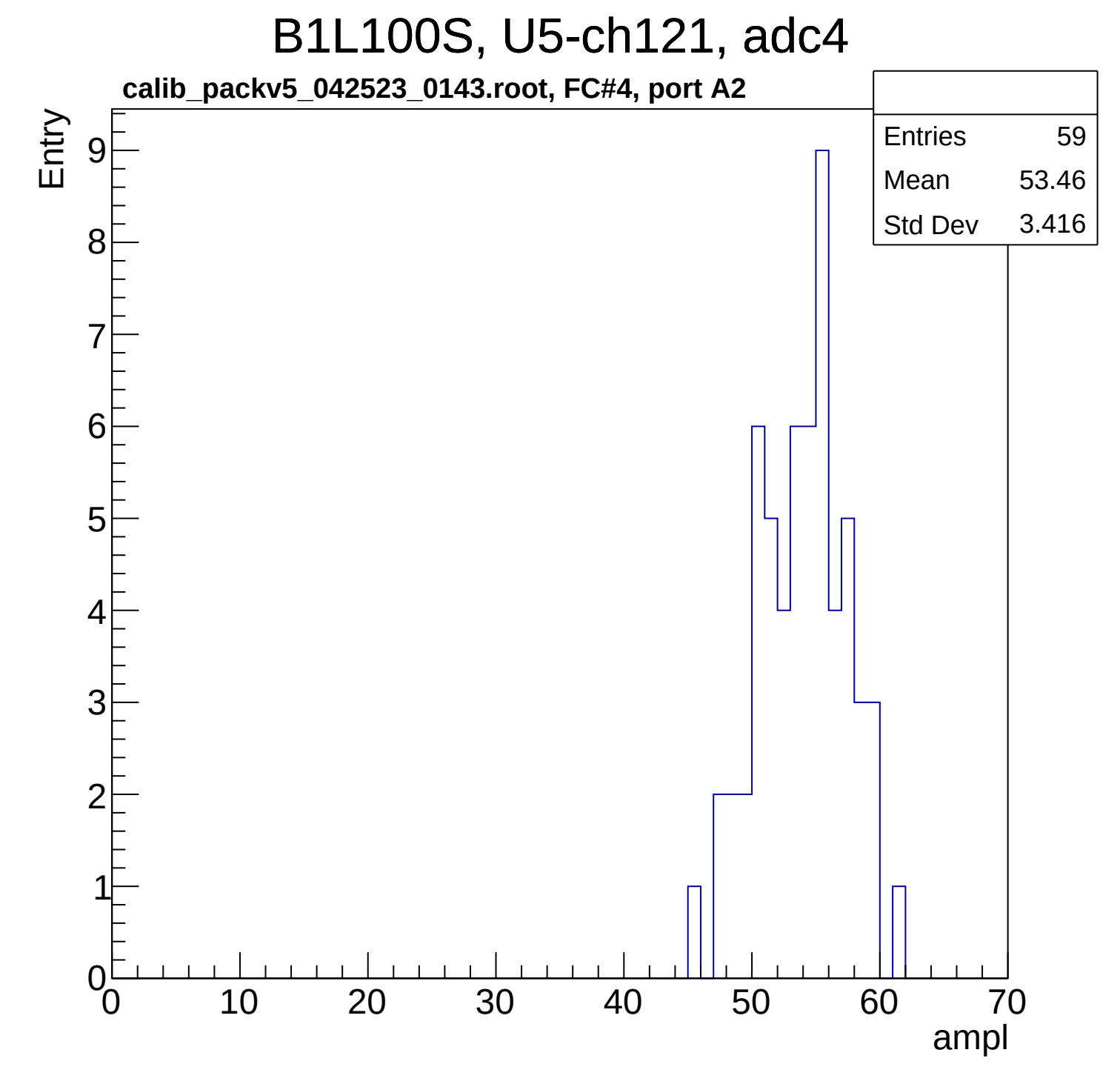

B1L100S, U5-ch120, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

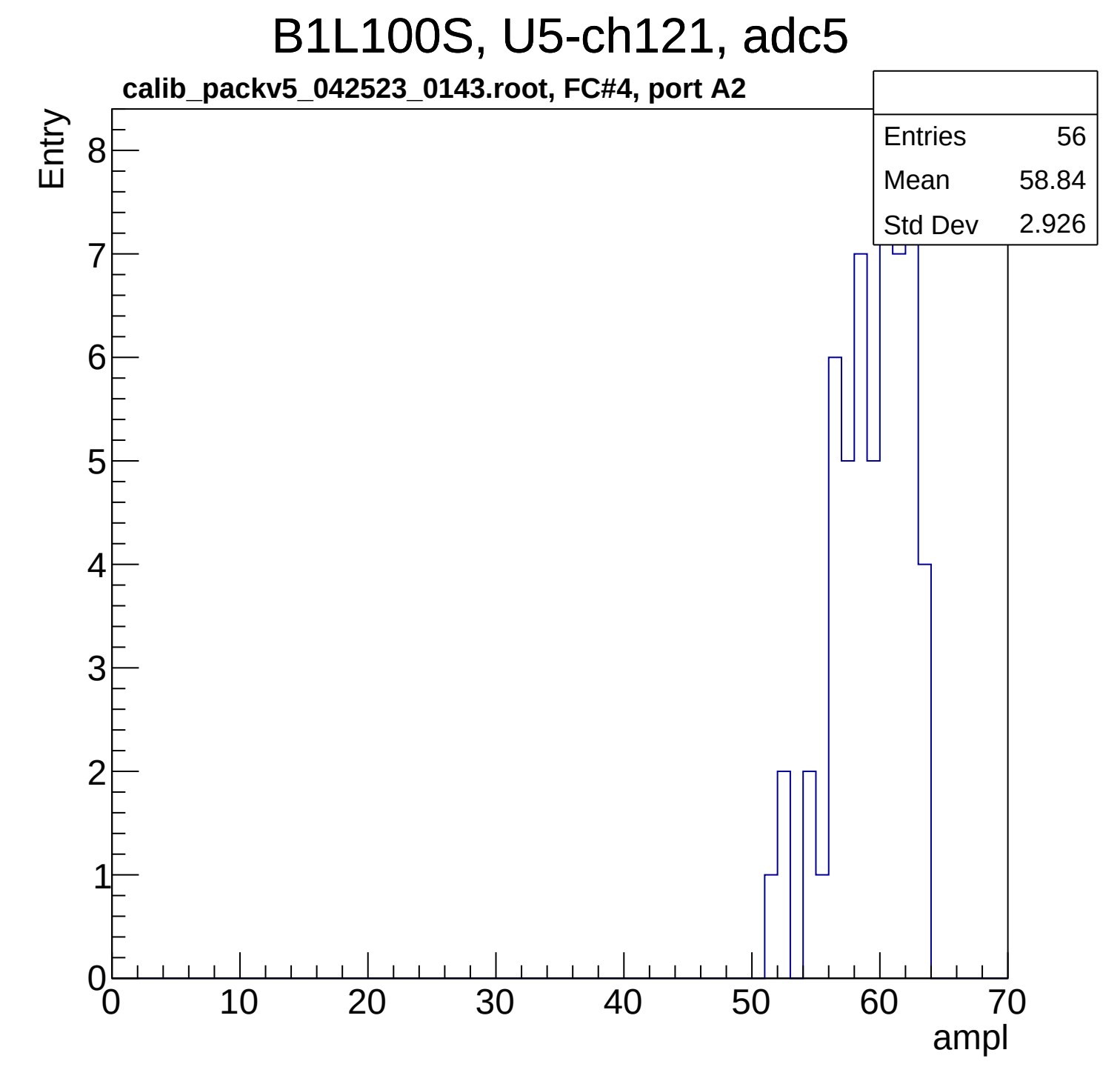

B1L100S, U5-ch121, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 75
Mean 26.56
Std Dev 5.87
Gaus mean : 28.0286
Gaus Width: 4.6005
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

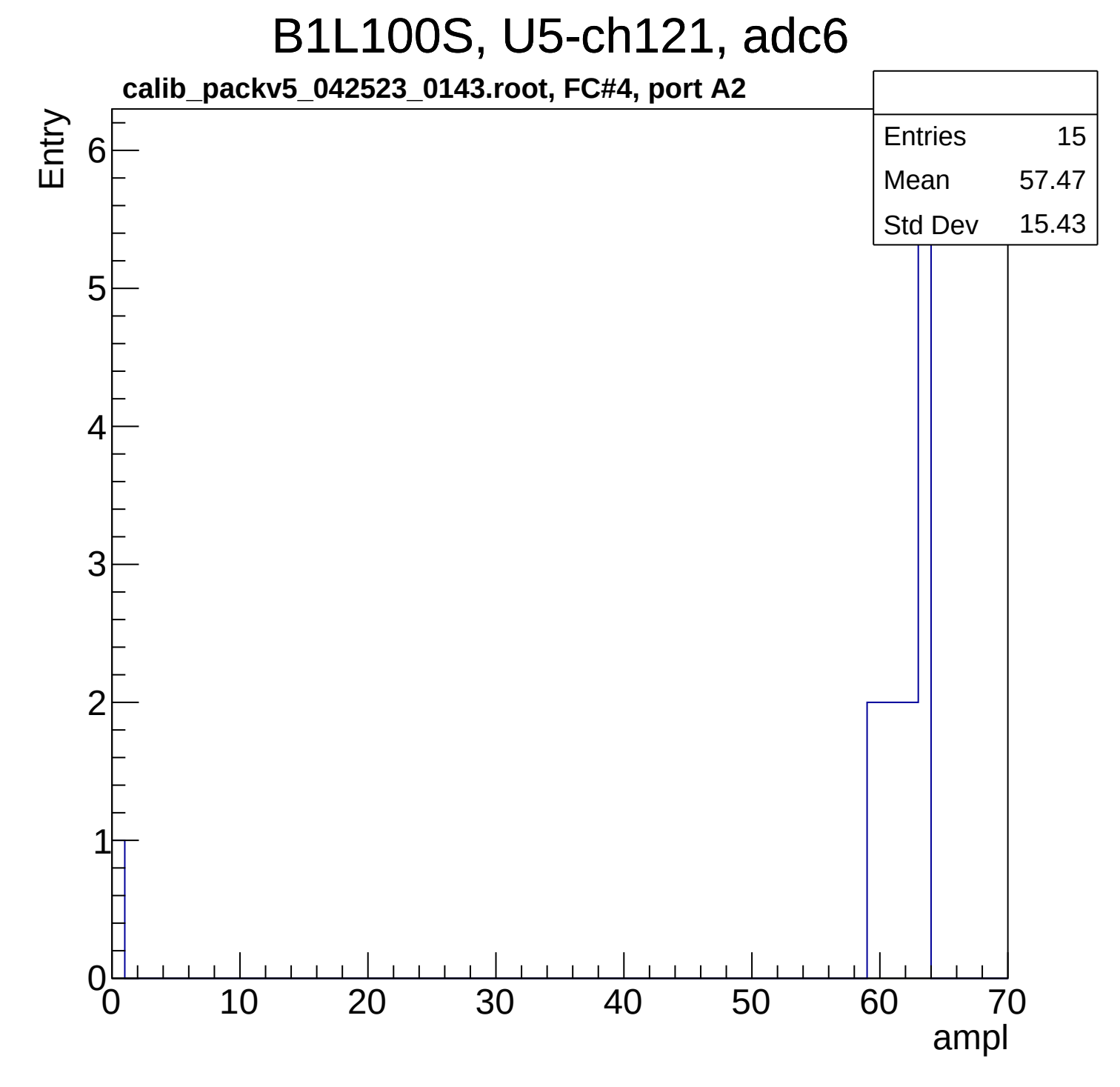

B1L100S, U5-ch121, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 76
Mean 35.13
Std Dev 3.599
Gaus mean : 36.0218
Gaus Width: 4.1396
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

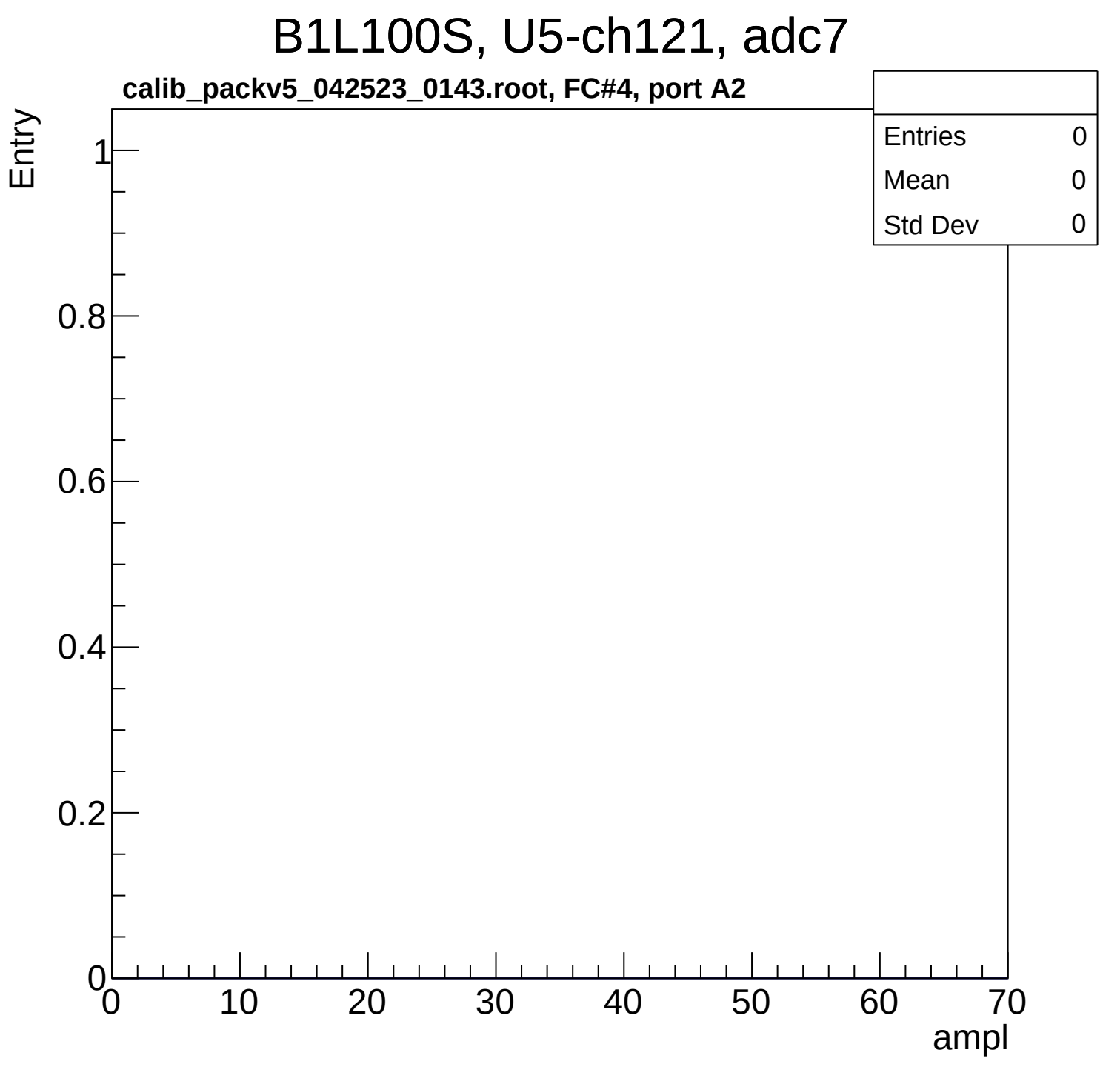

B1L100S, U5-ch121, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 42.11
Std Dev 3.32
Gaus mean : 42.9572
Gaus Width: 4.3315
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

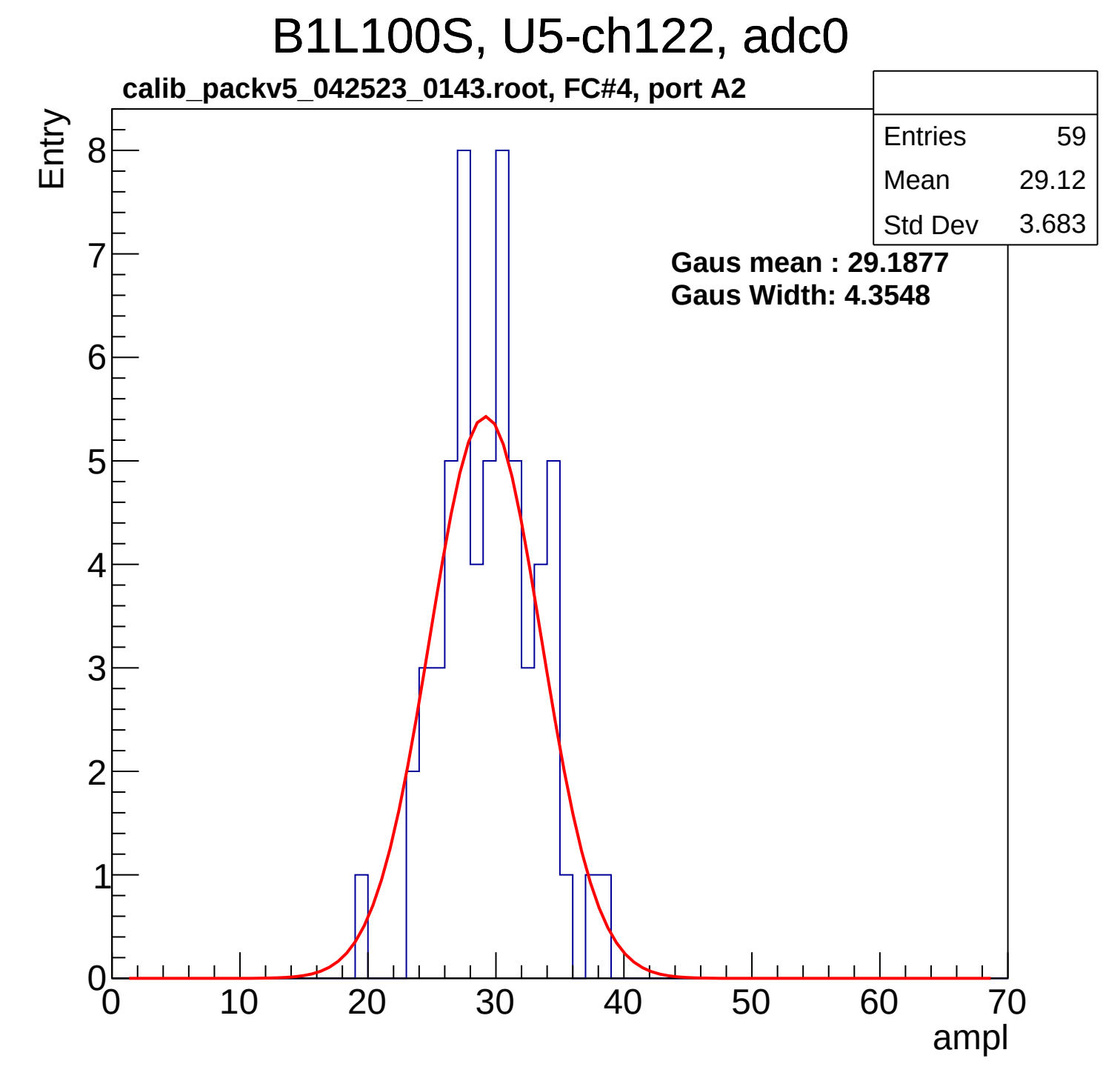

B1L100S, U5-ch121, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 52
Mean 48.19
Std Dev 3.252
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

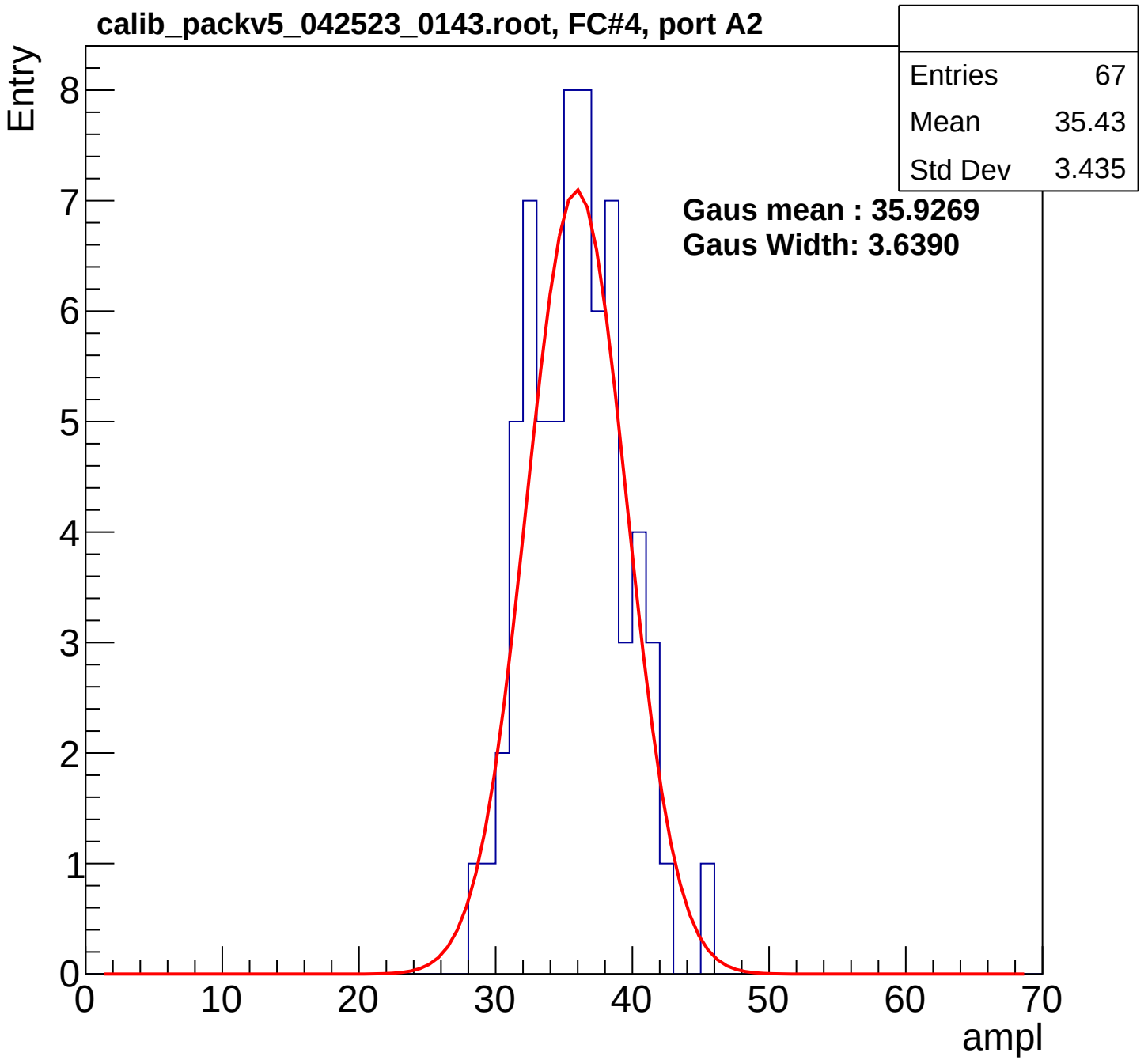

B1L100S, U5-ch121, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 53.46
Std Dev 3.416
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

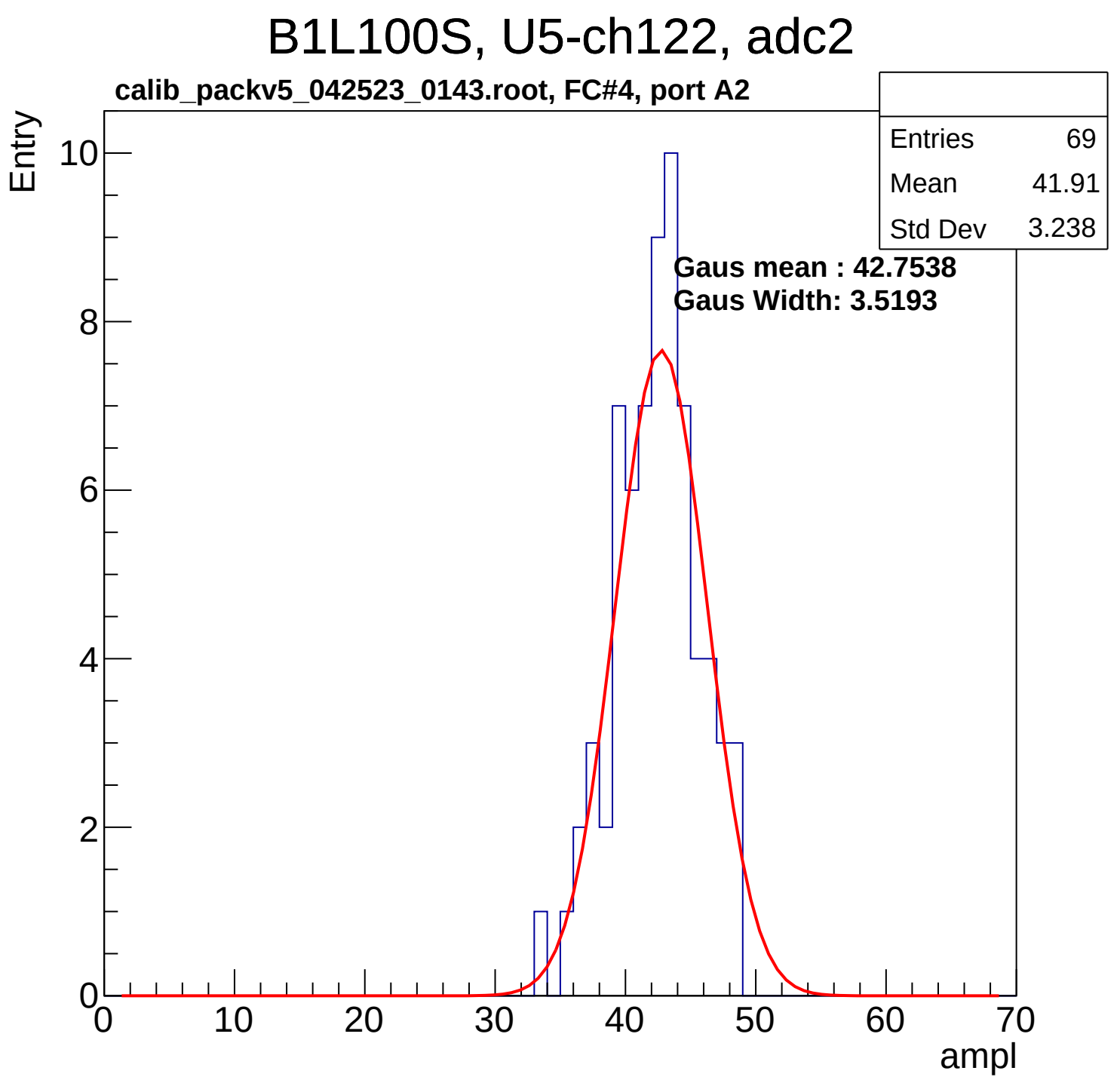

B1L100S, U5-ch121, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 58.84
Std Dev 2.926
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

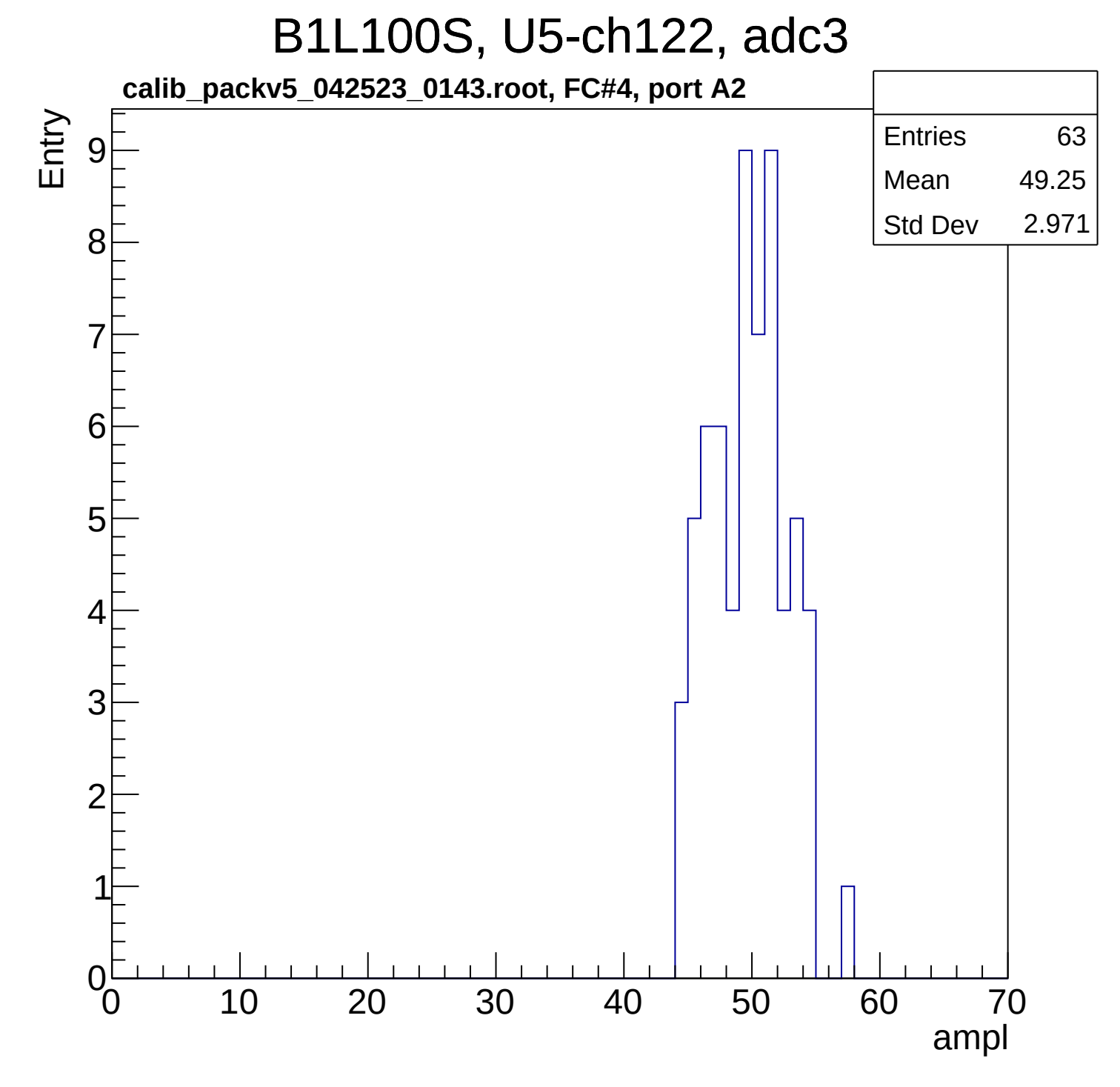

B1L100S, U5-ch121, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 15
Mean 57.47
Std Dev 15.43
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

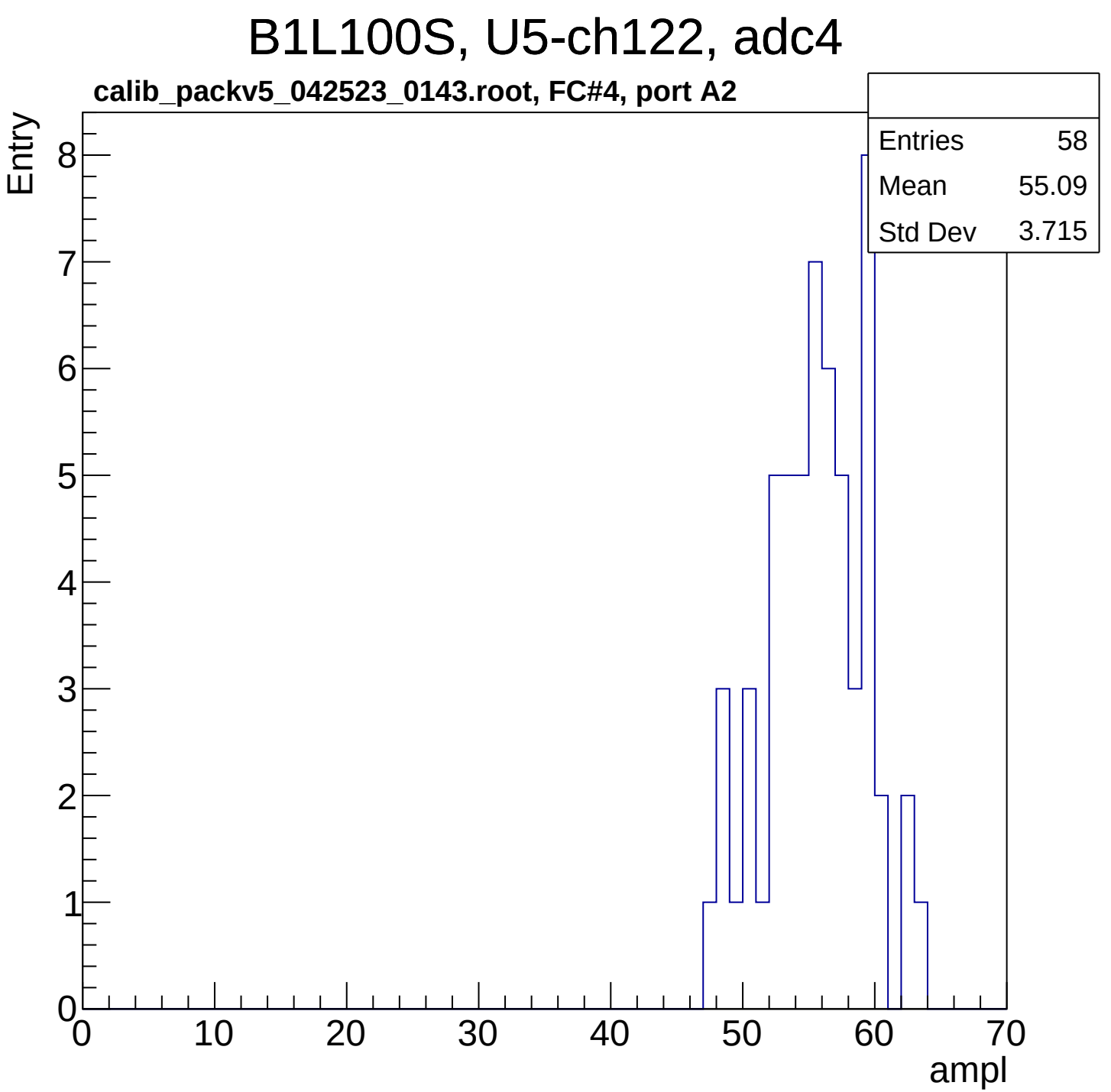

B1L100S, U5-ch121, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

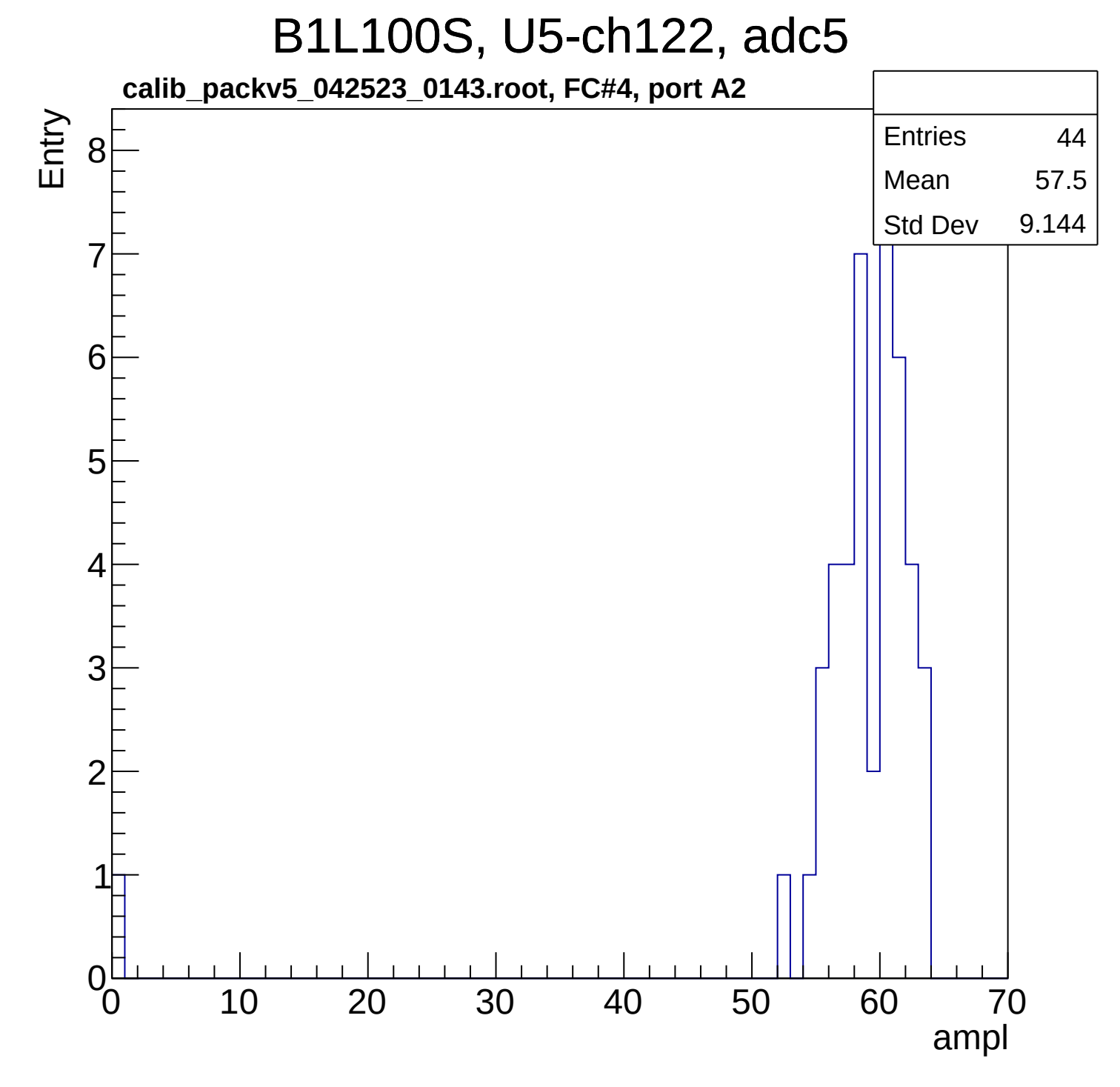

B1L100S, U5-ch122, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 29.12
Std Dev 3.683
Gaus mean : 29.1877
Gaus Width: 4.3548
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch122, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 35.43
Std Dev 3.435
Gaus mean : 35.9269
Gaus Width: 3.6390
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch122, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 41.91
Std Dev 3.238
Gaus mean : 42.7538
Gaus Width: 3.5193
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U5-ch122, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 49.25
Std Dev 2.971
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch122, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 55.09
Std Dev 3.715
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch122, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 44
Mean 57.5
Std Dev 9.144
Entry
ampl
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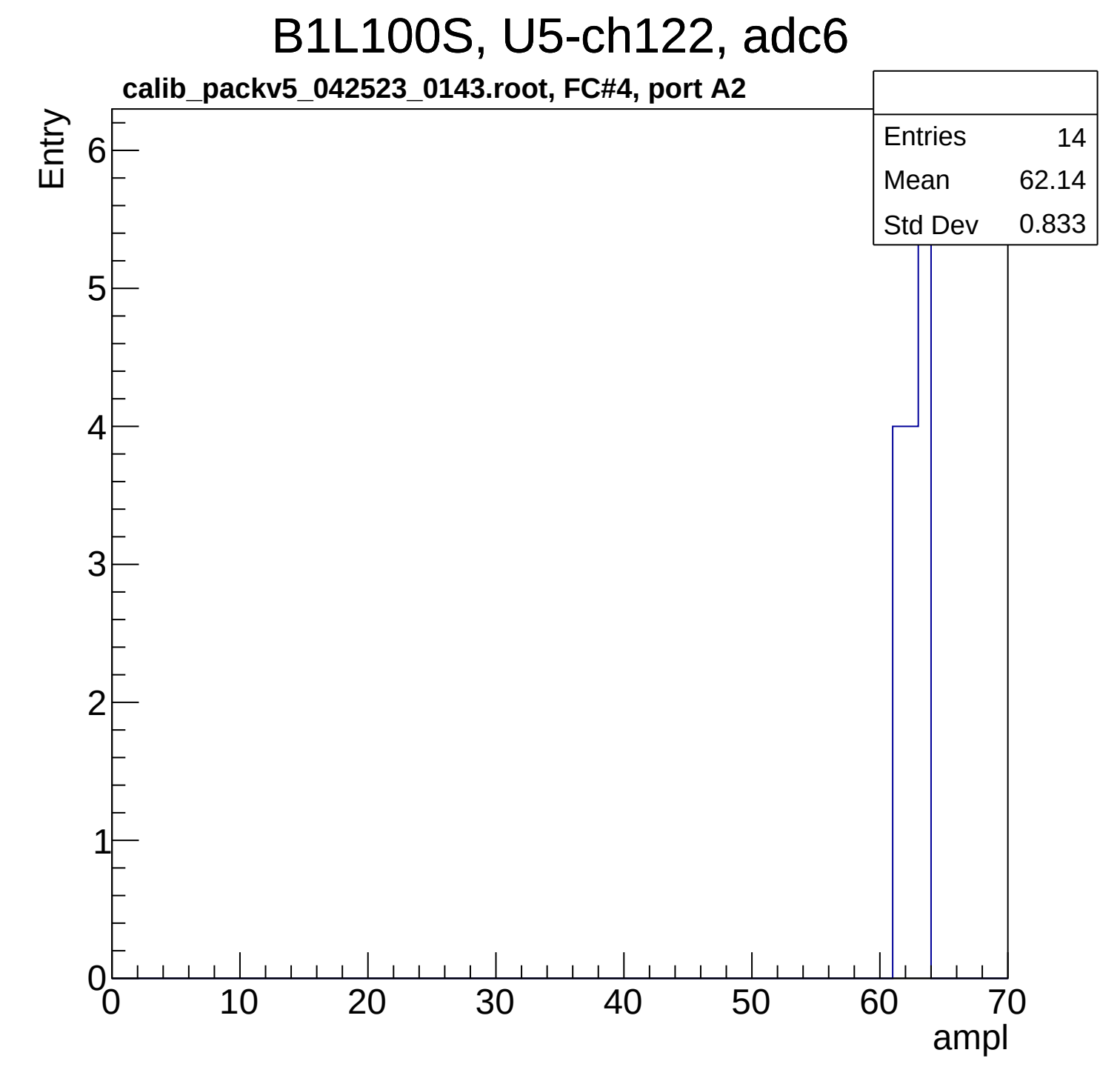
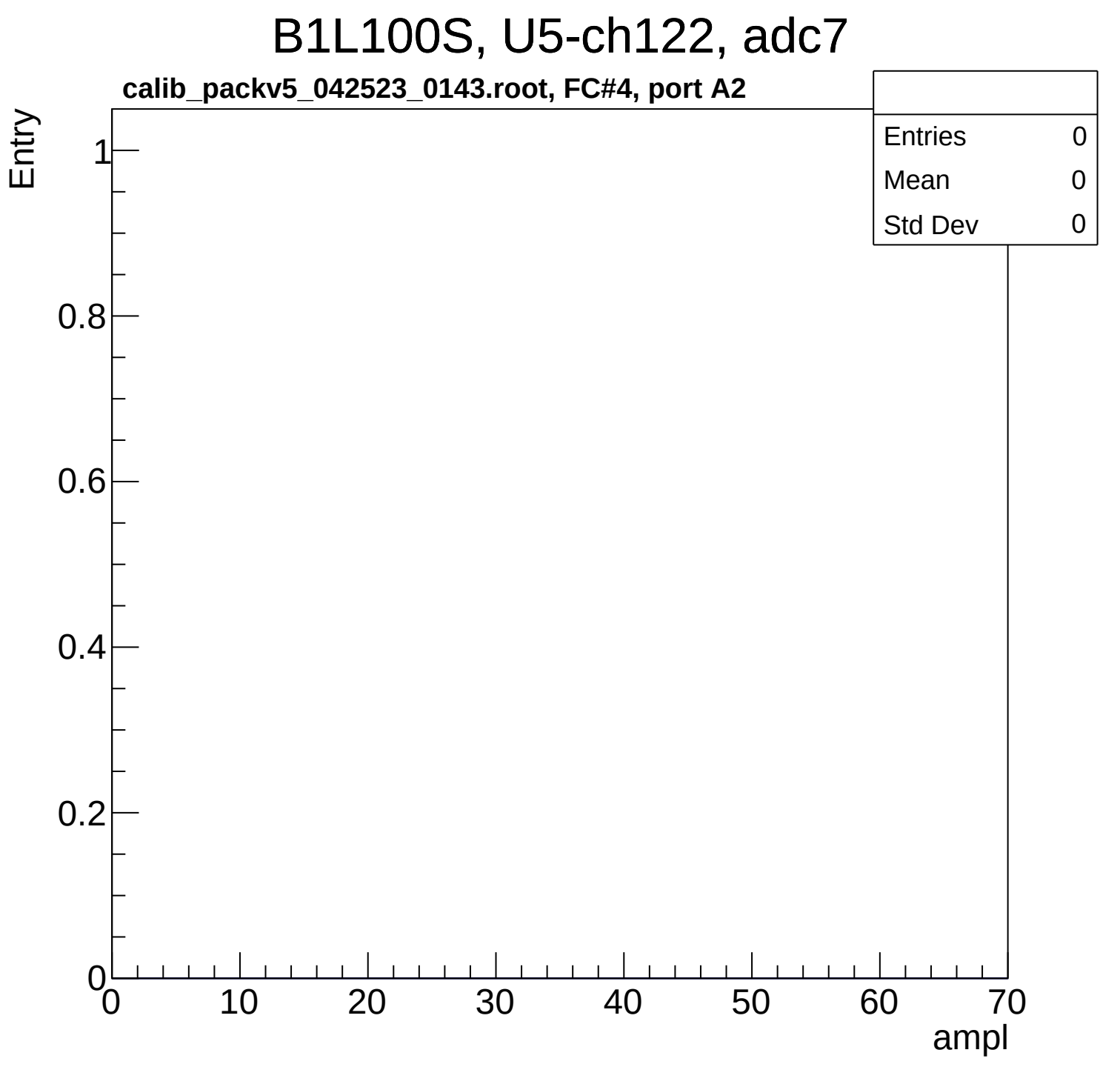
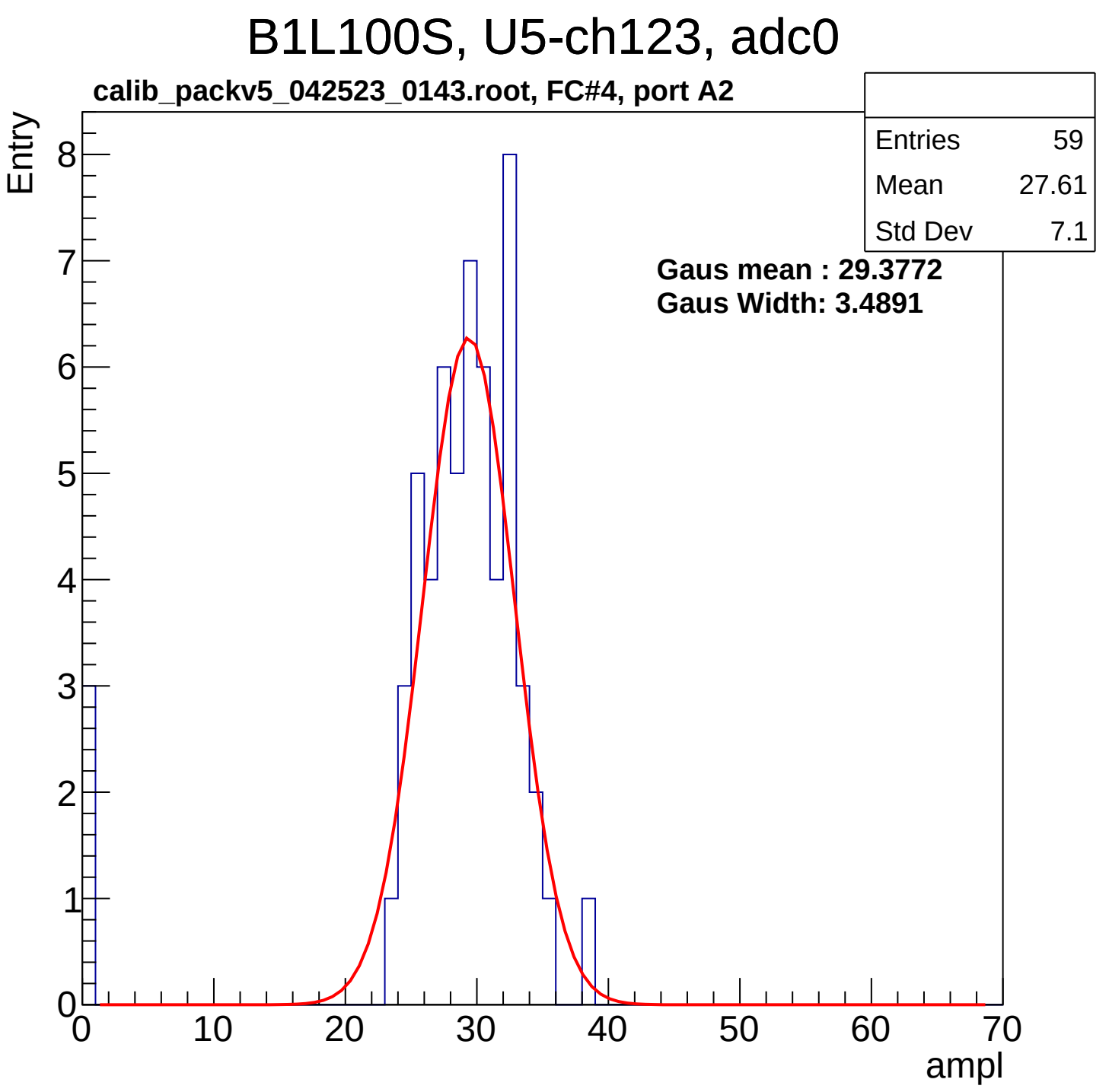
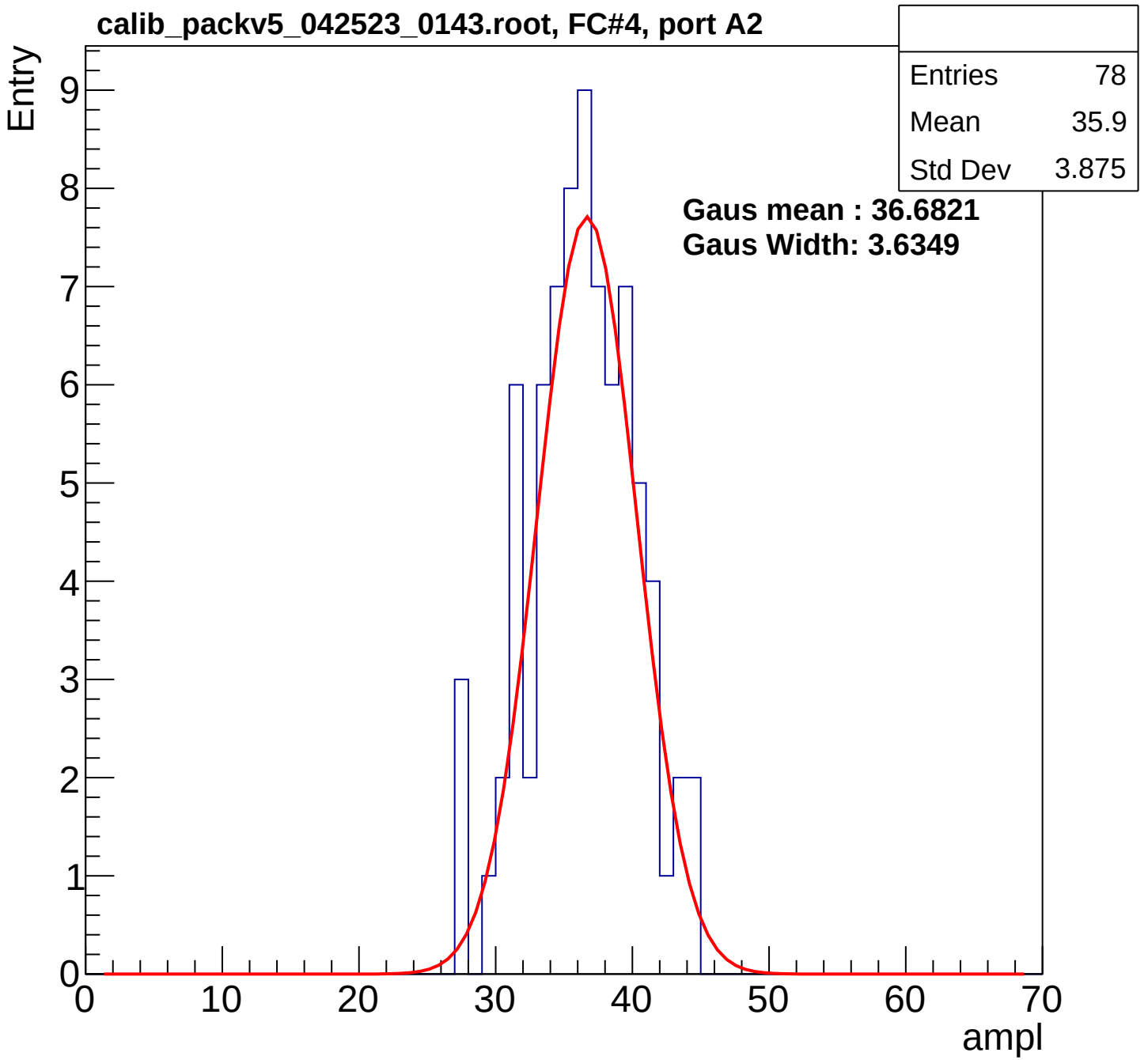
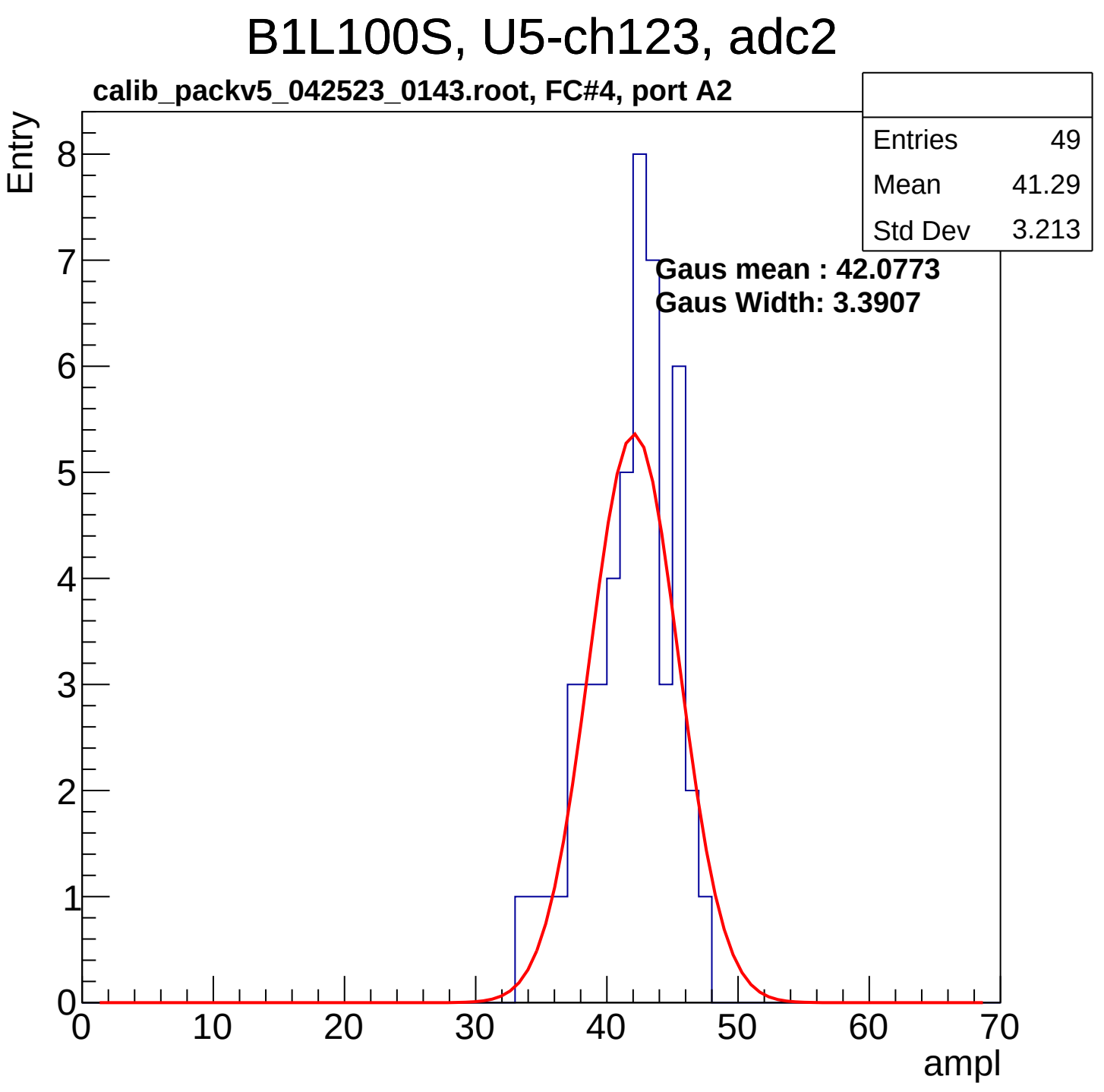
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

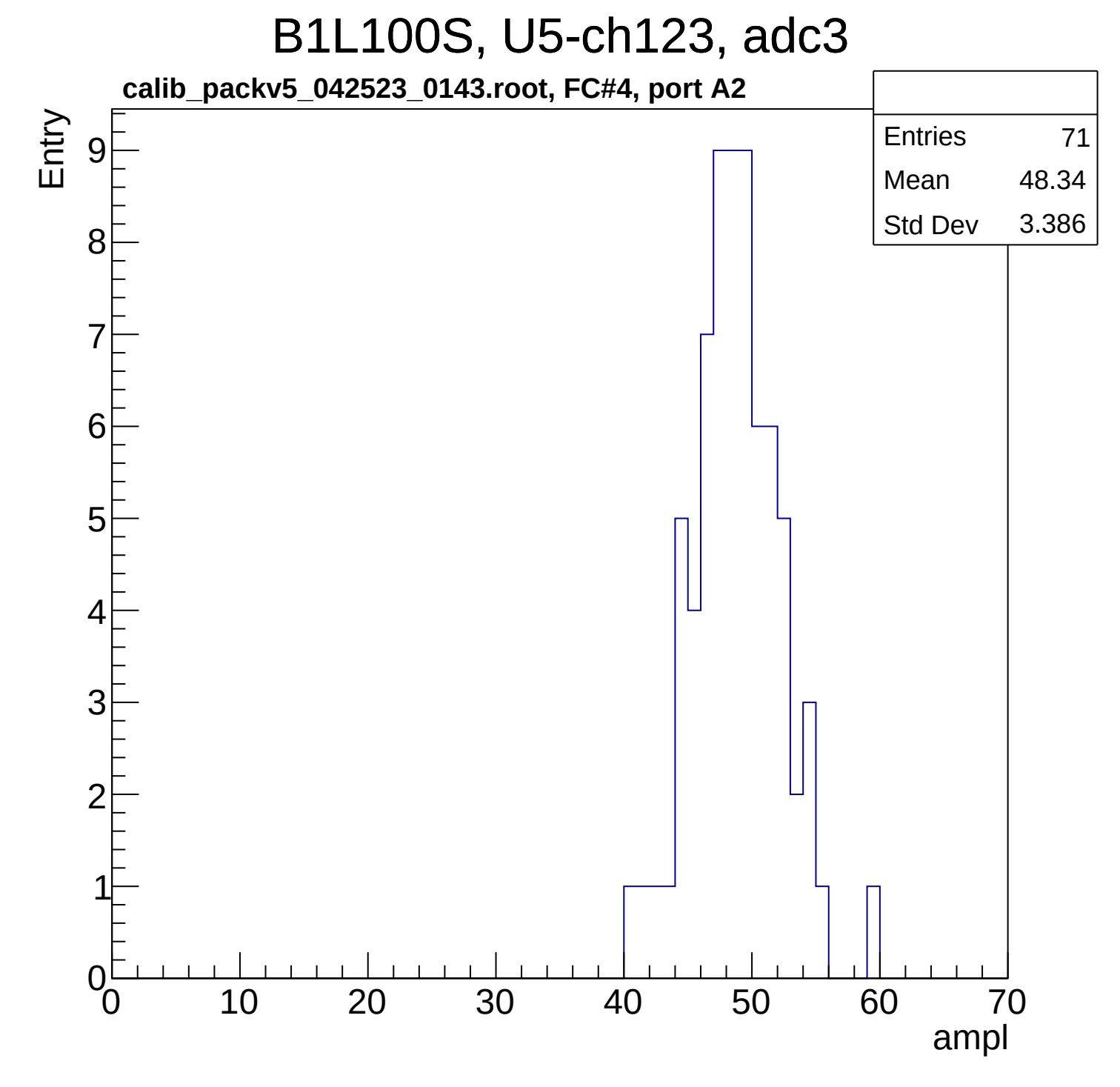

B1L100S, U5-ch122, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 14
Mean 62.14
Std Dev 0.833
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch122, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch123, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 27.61
Std Dev 7.1
Gaus mean : 29.3772
Gaus Width: 3.4891
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch123, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 78
Mean 35.9
Std Dev 3.875
Gaus mean : 36.6821
Gaus Width: 3.6349
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch123, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 49
Mean 41.29
Std Dev 3.213
Gaus mean : 42.0773
Gaus Width: 3.3907
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch123, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 48.34
Std Dev 3.386
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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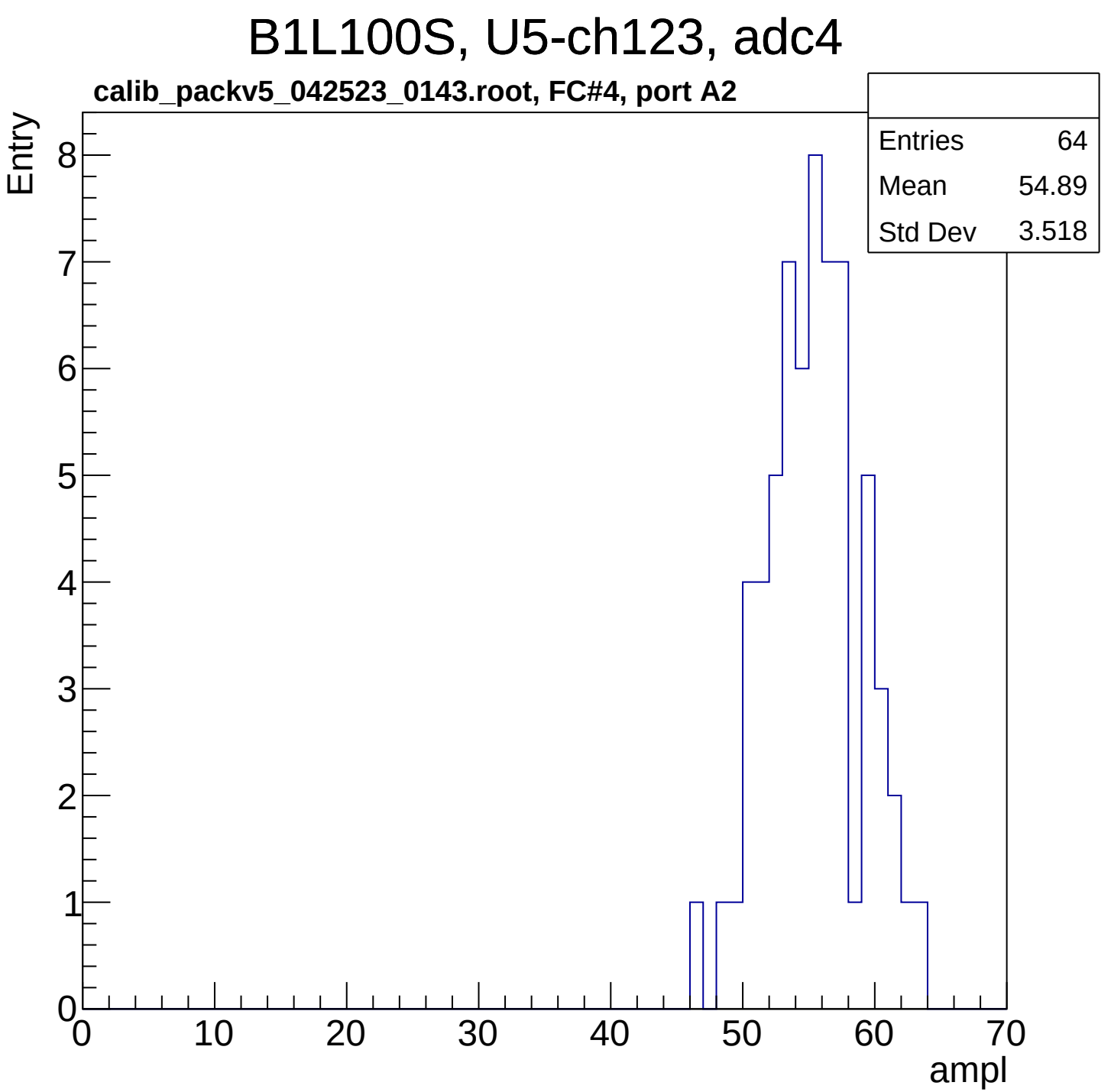
B1L100S, U5-ch123, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 54.89
Std Dev 3.518
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
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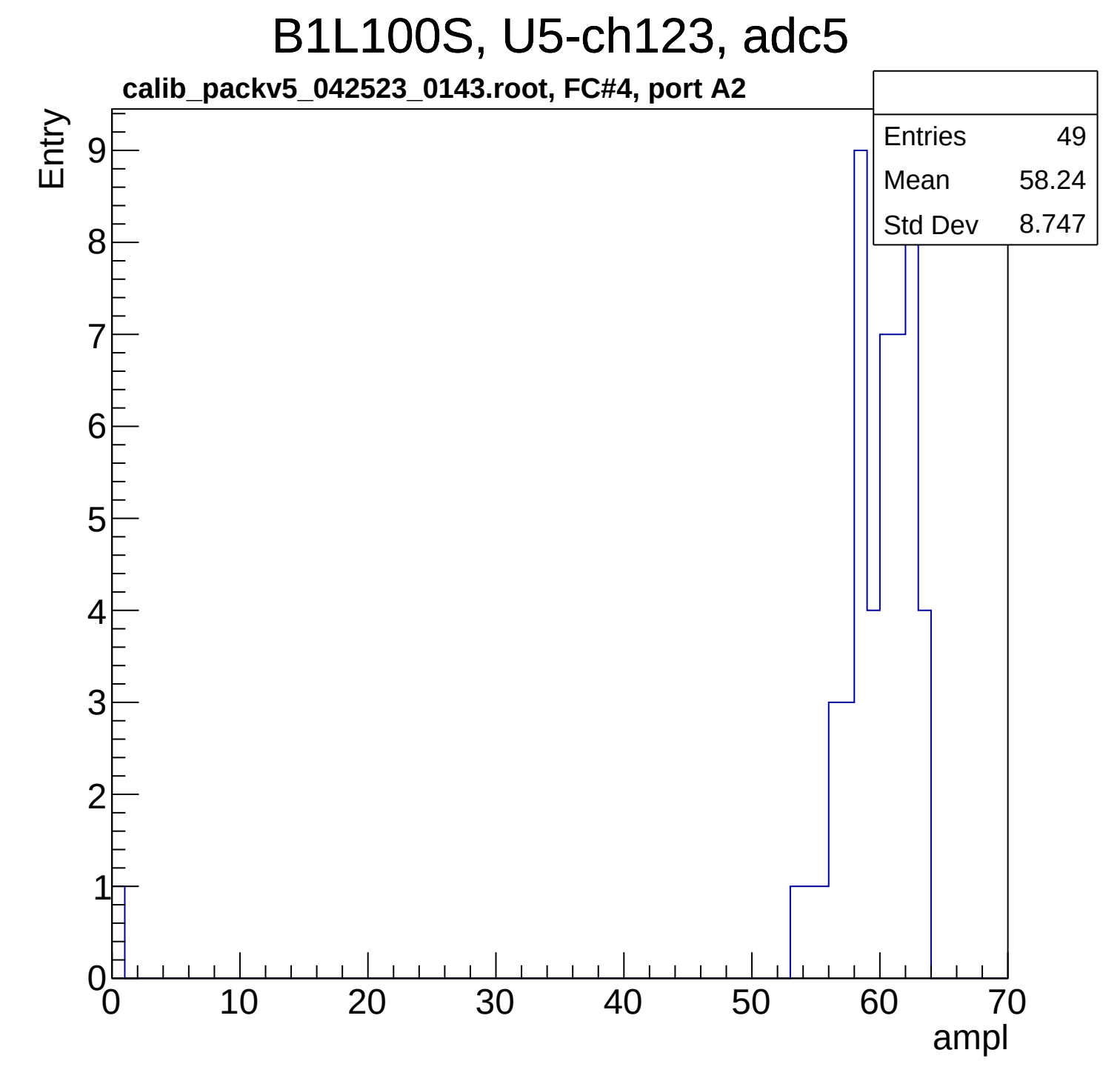
60
70


B1L100S, U5-ch123, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 49
Mean 58.24
Std Dev 8.747
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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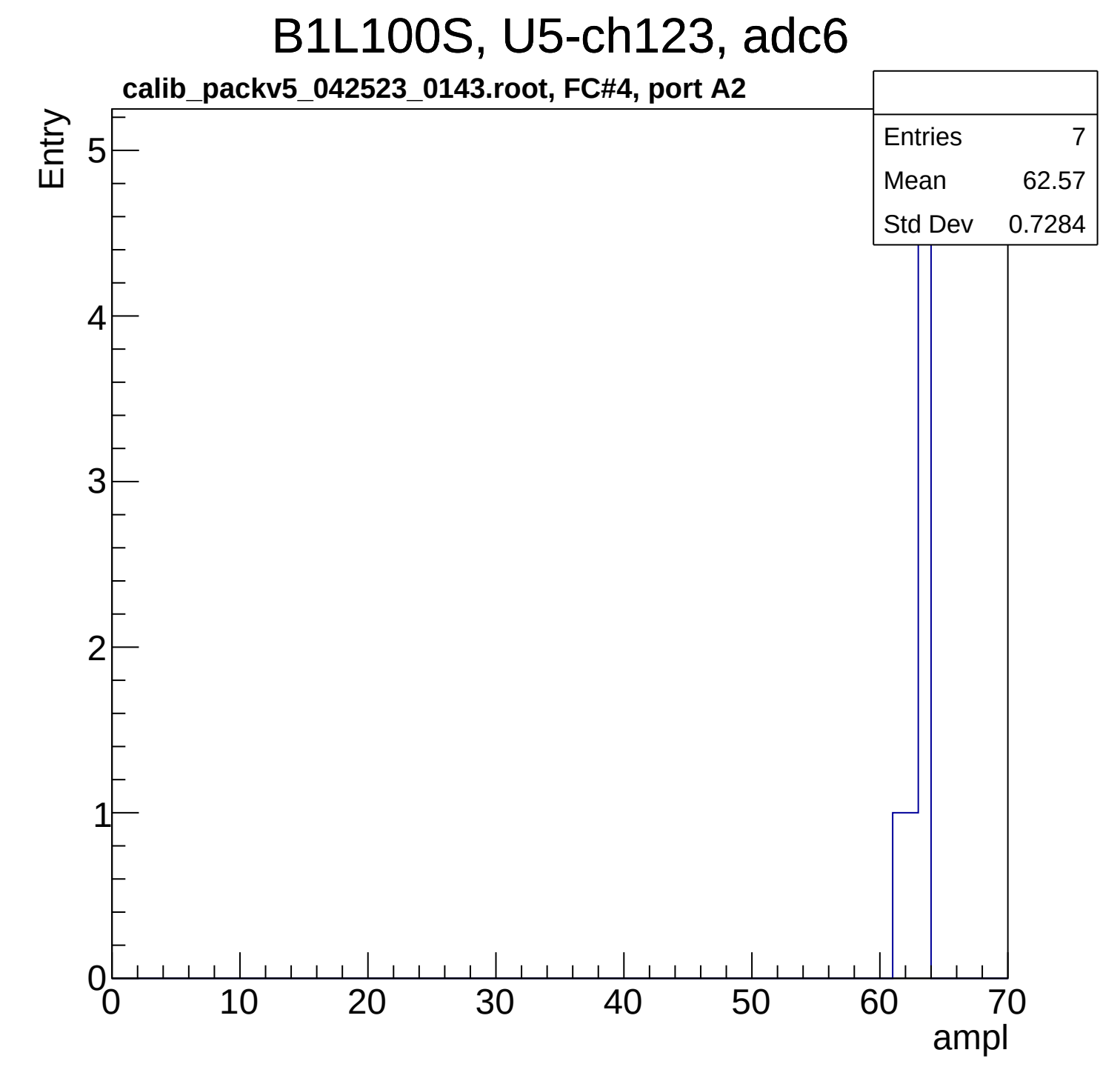
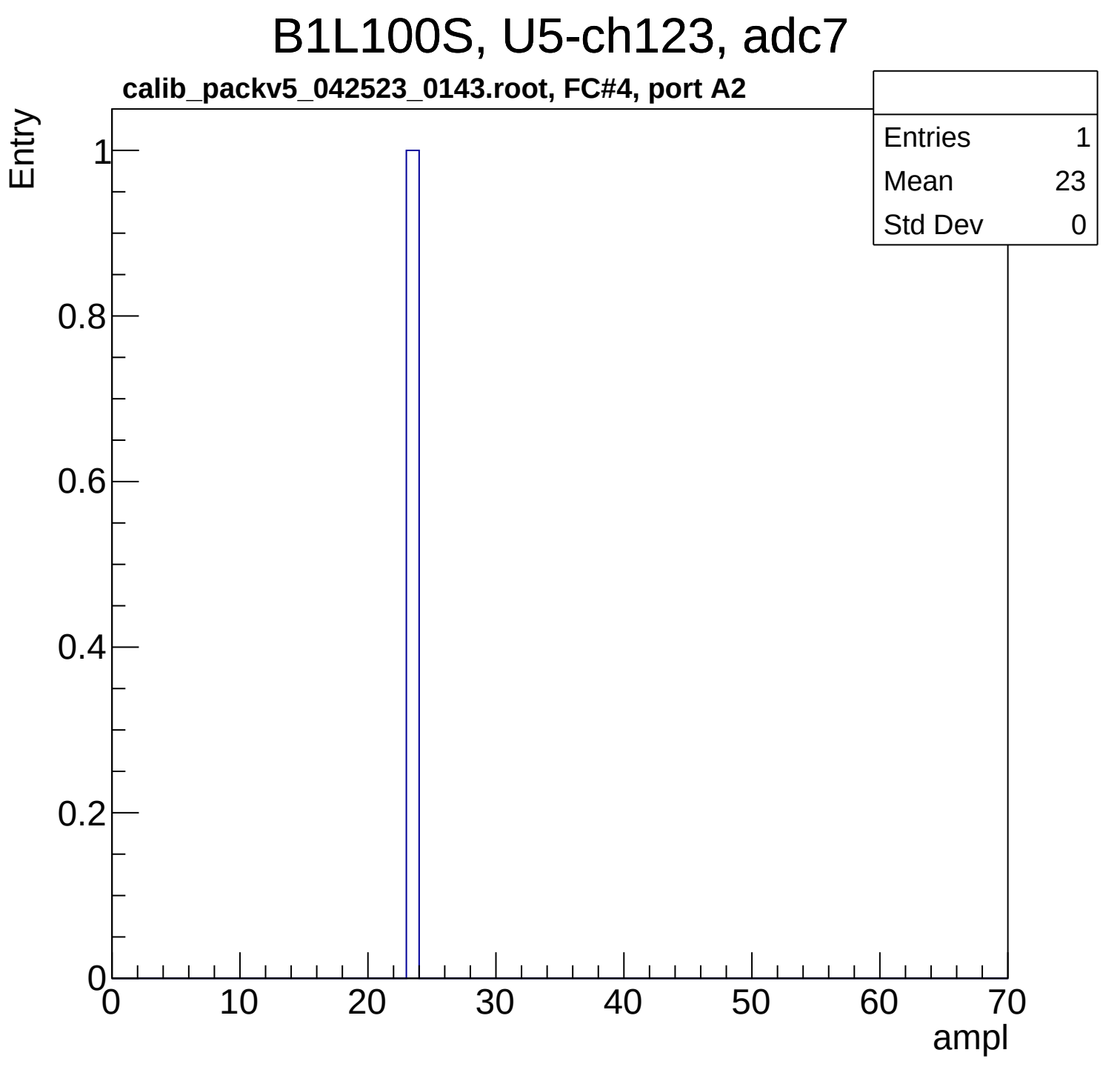
40
50
60
70


B1L100S, U5-ch123, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 7
Mean 62.57
Std Dev 0.7284
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L100S, U5-ch123, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 23
Std Dev 0
Entry
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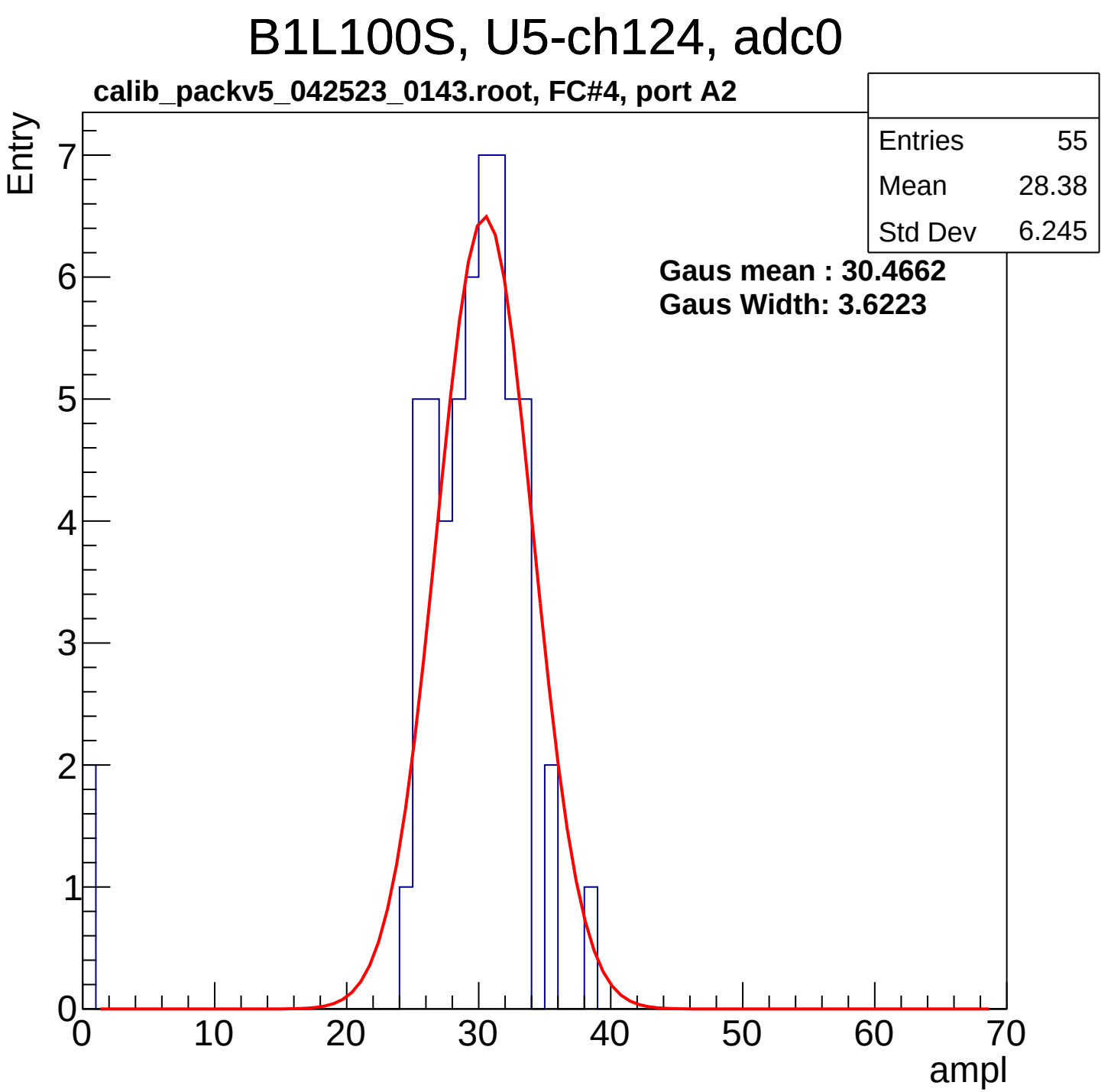
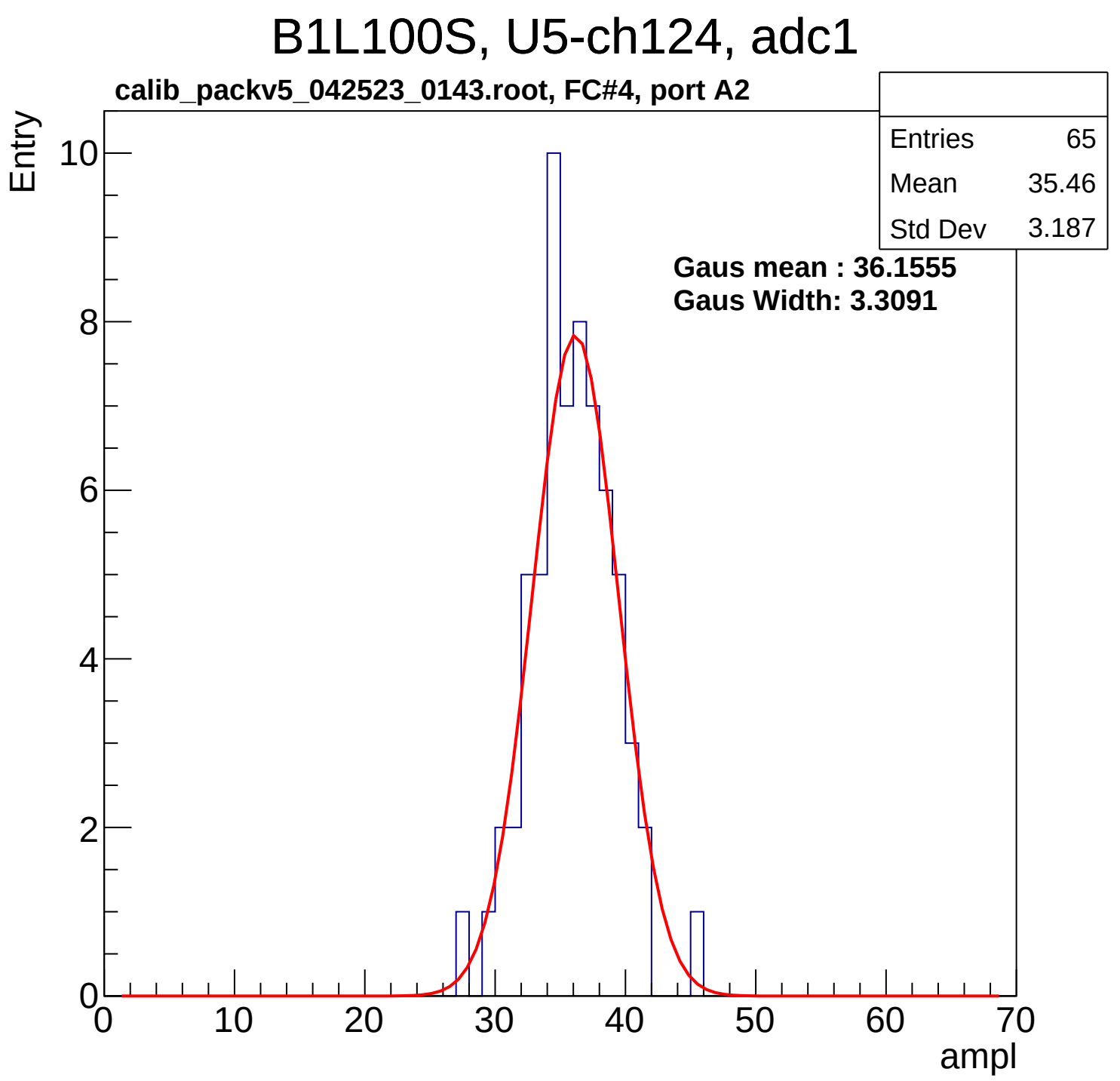
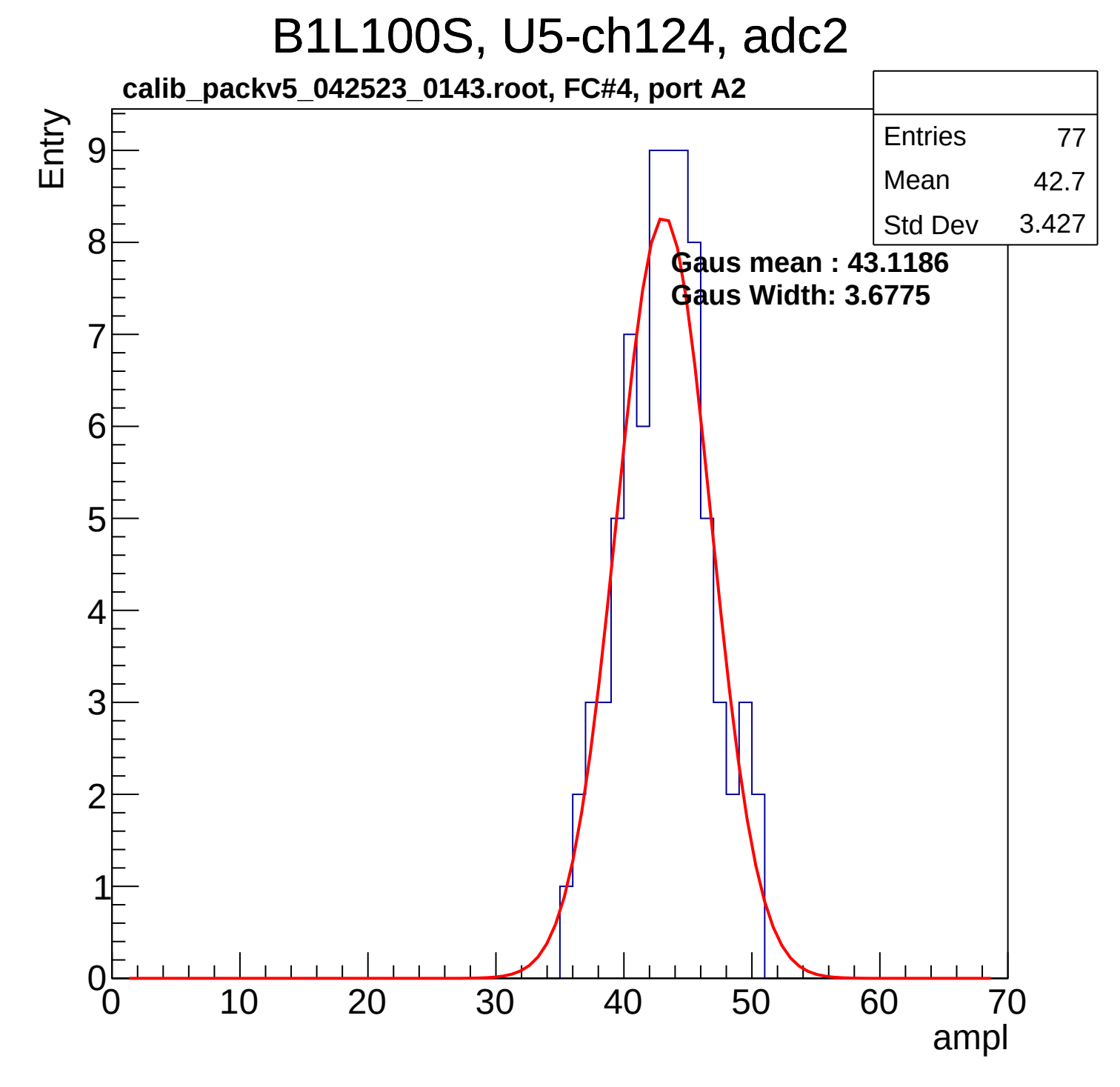
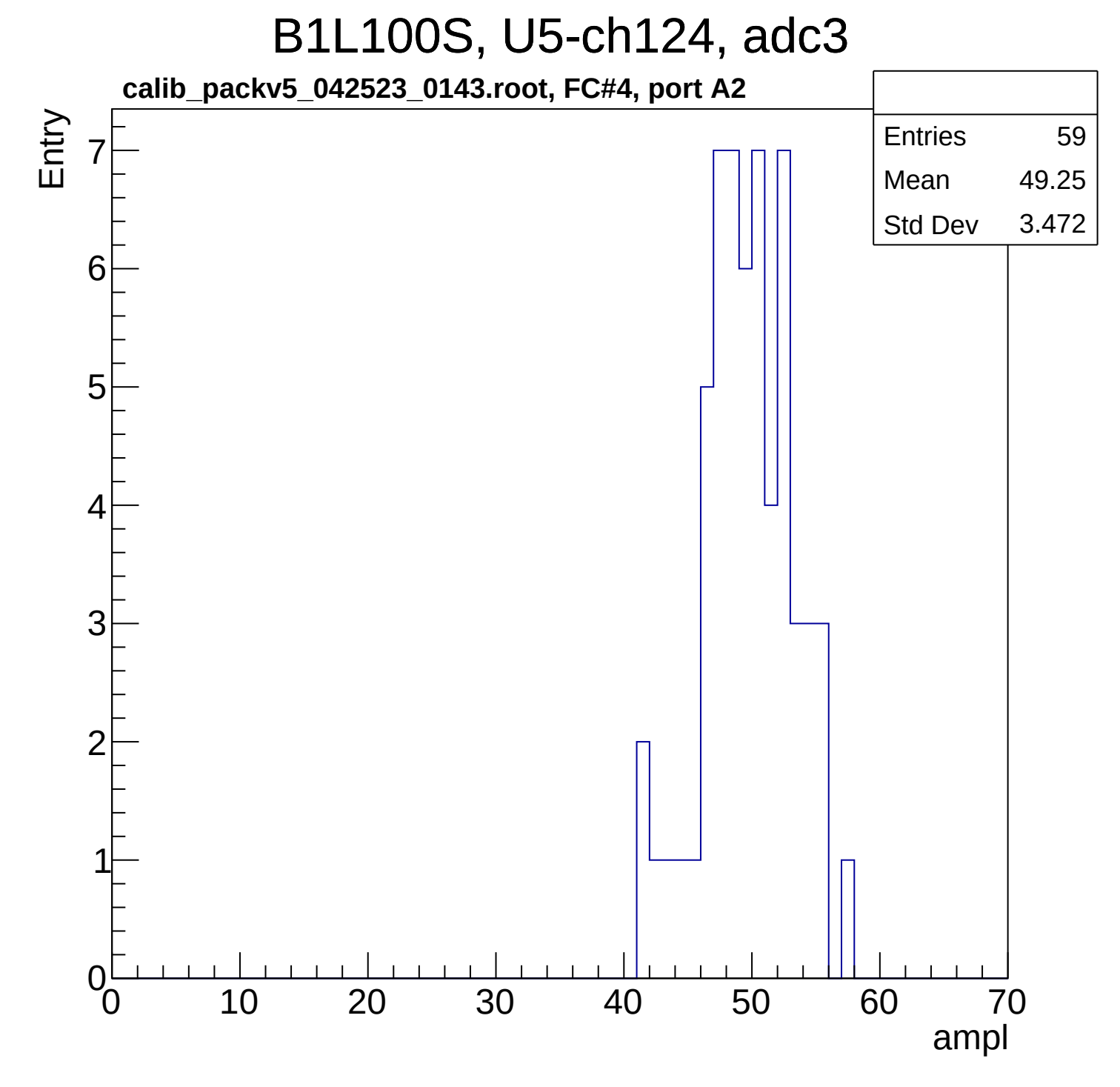
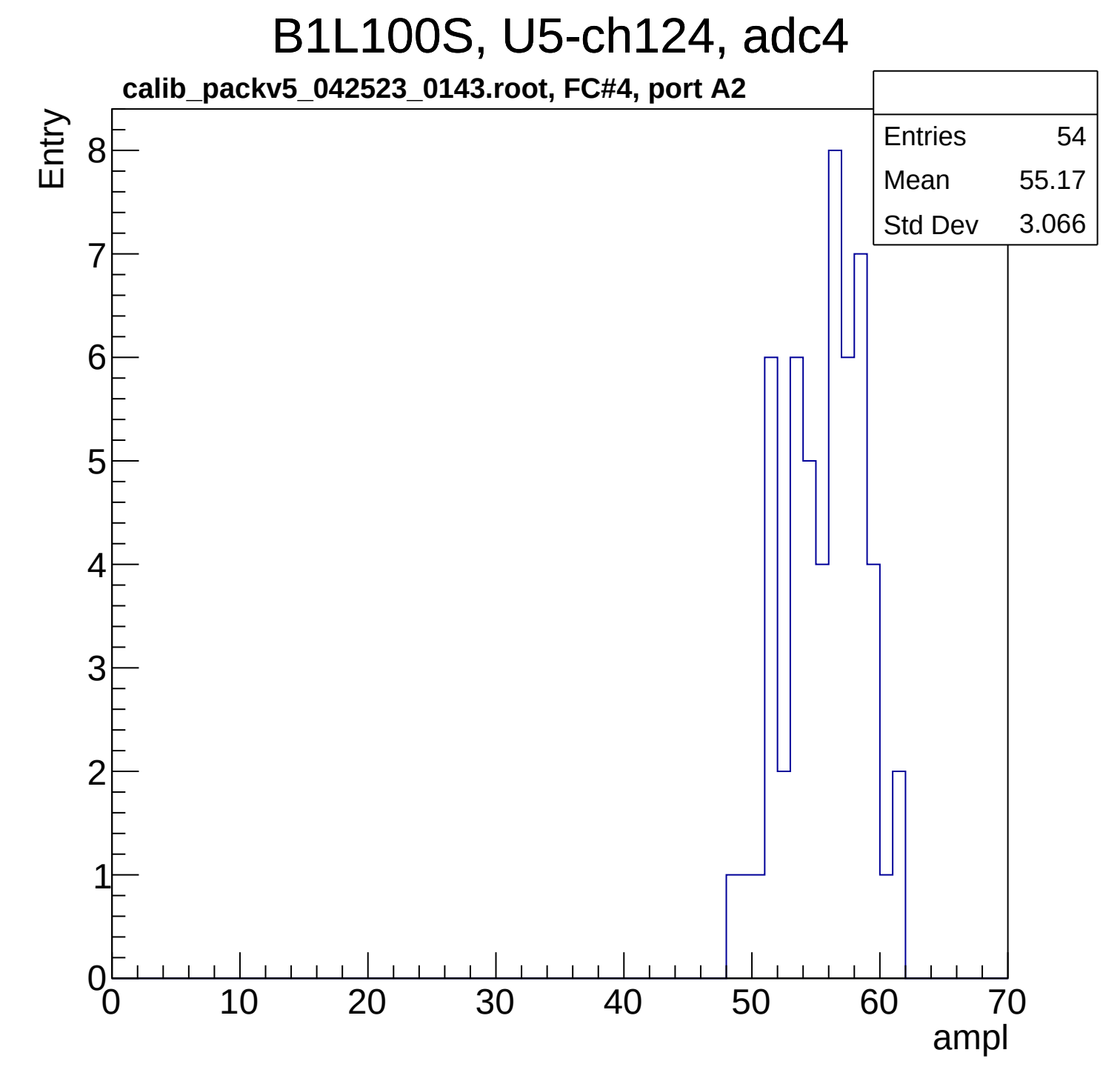
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

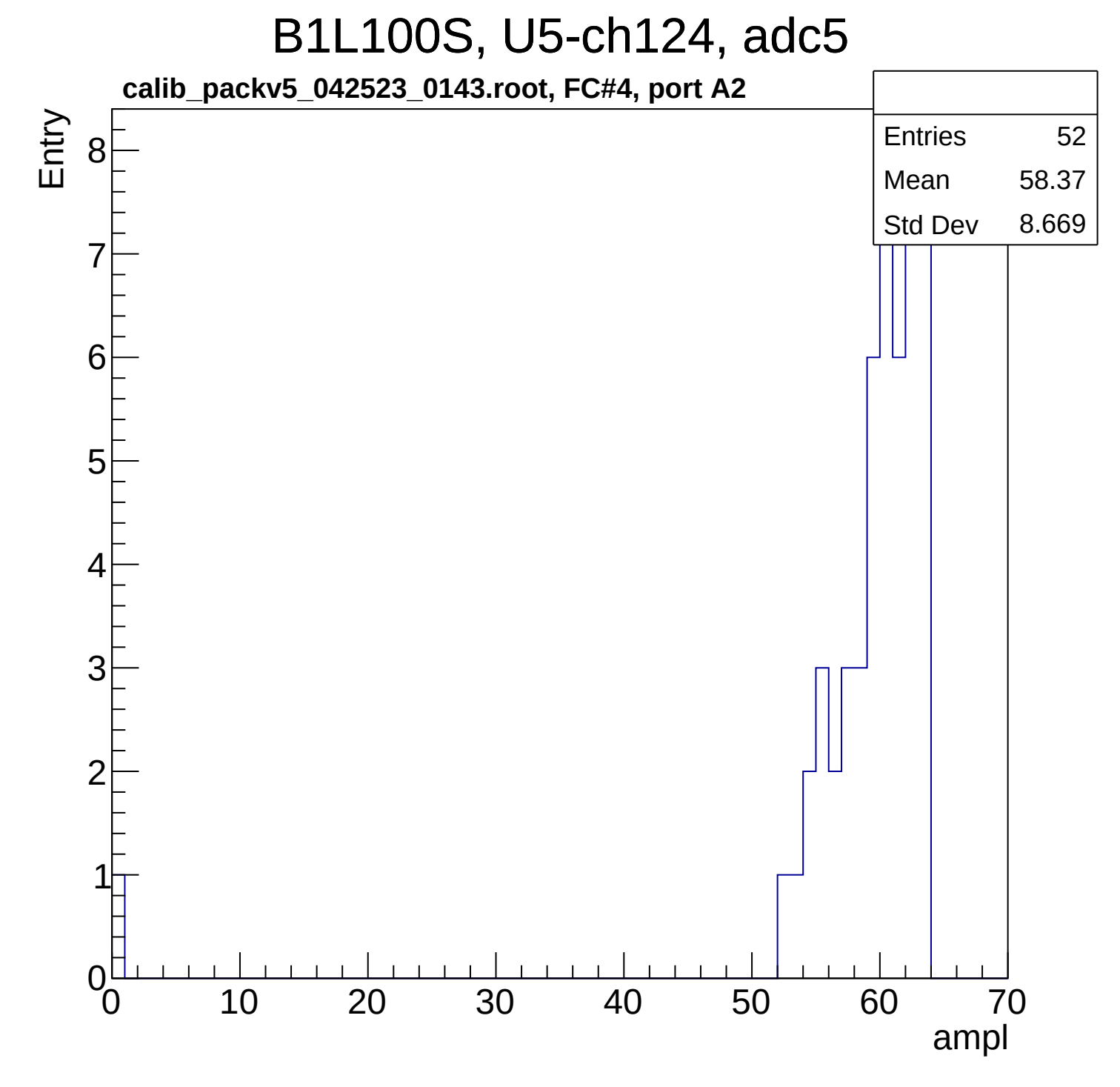

B1L100S, U5-ch124, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 28.38
Std Dev 6.245
Gaus mean : 30.4662
Gaus Width: 3.6223
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

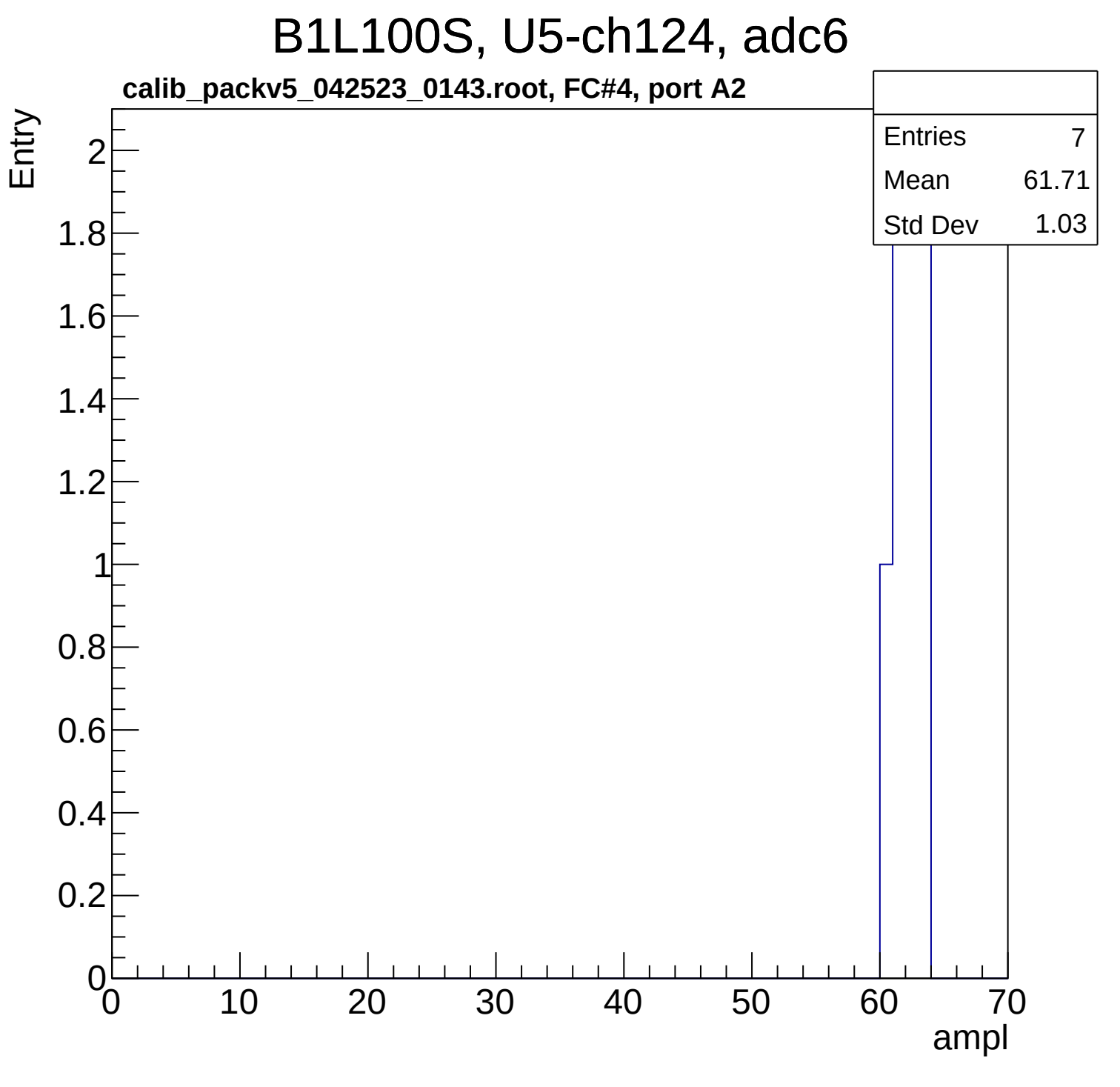

B1L100S, U5-ch124, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 35.46
Std Dev 3.187
Gaus mean : 36.1555
Gaus Width: 3.3091
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

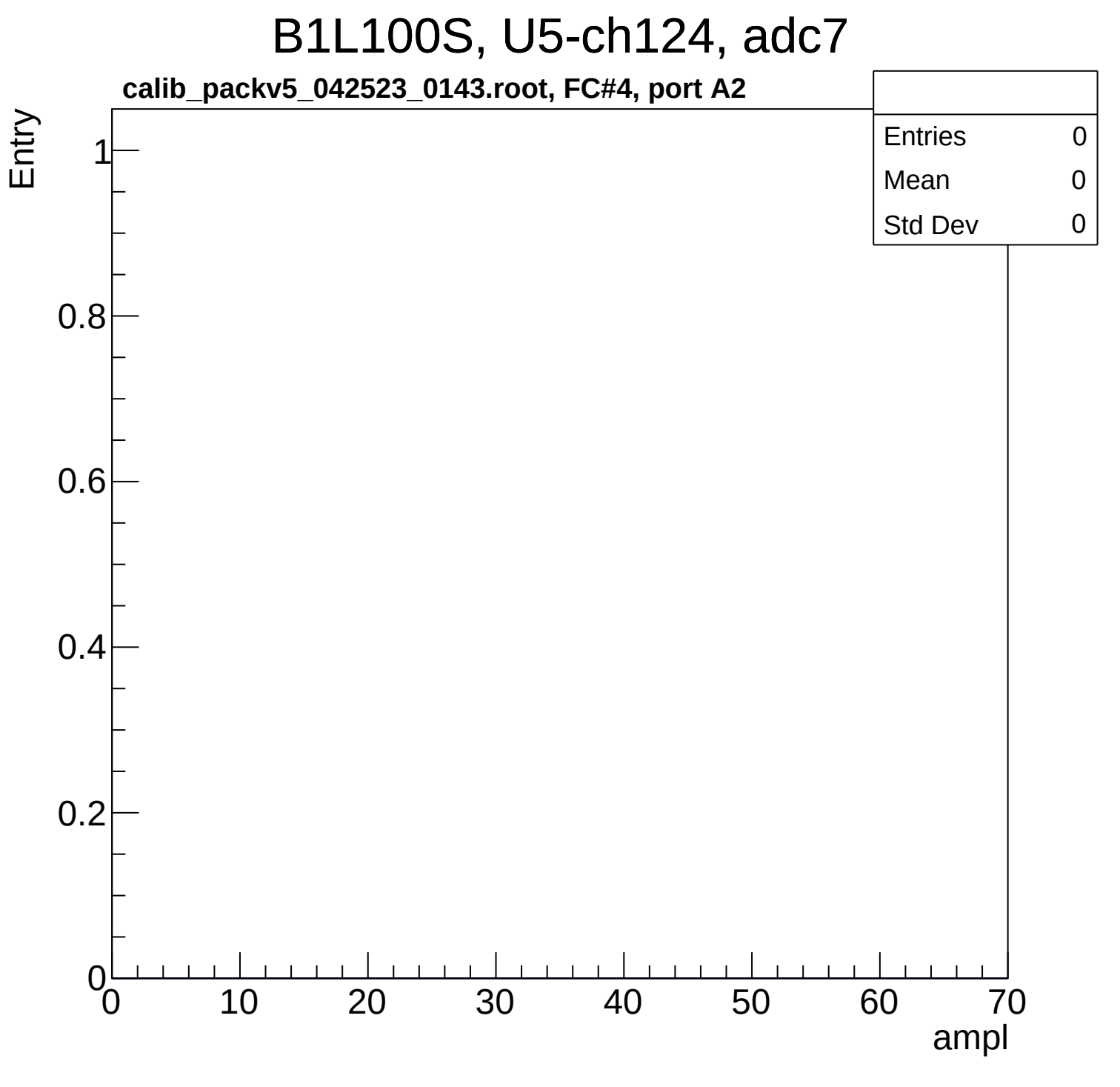

B1L100S, U5-ch124, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 77
Mean 42.7
Std Dev 3.427
Gaus mean : 43.1186
Gaus Width: 3.6775
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

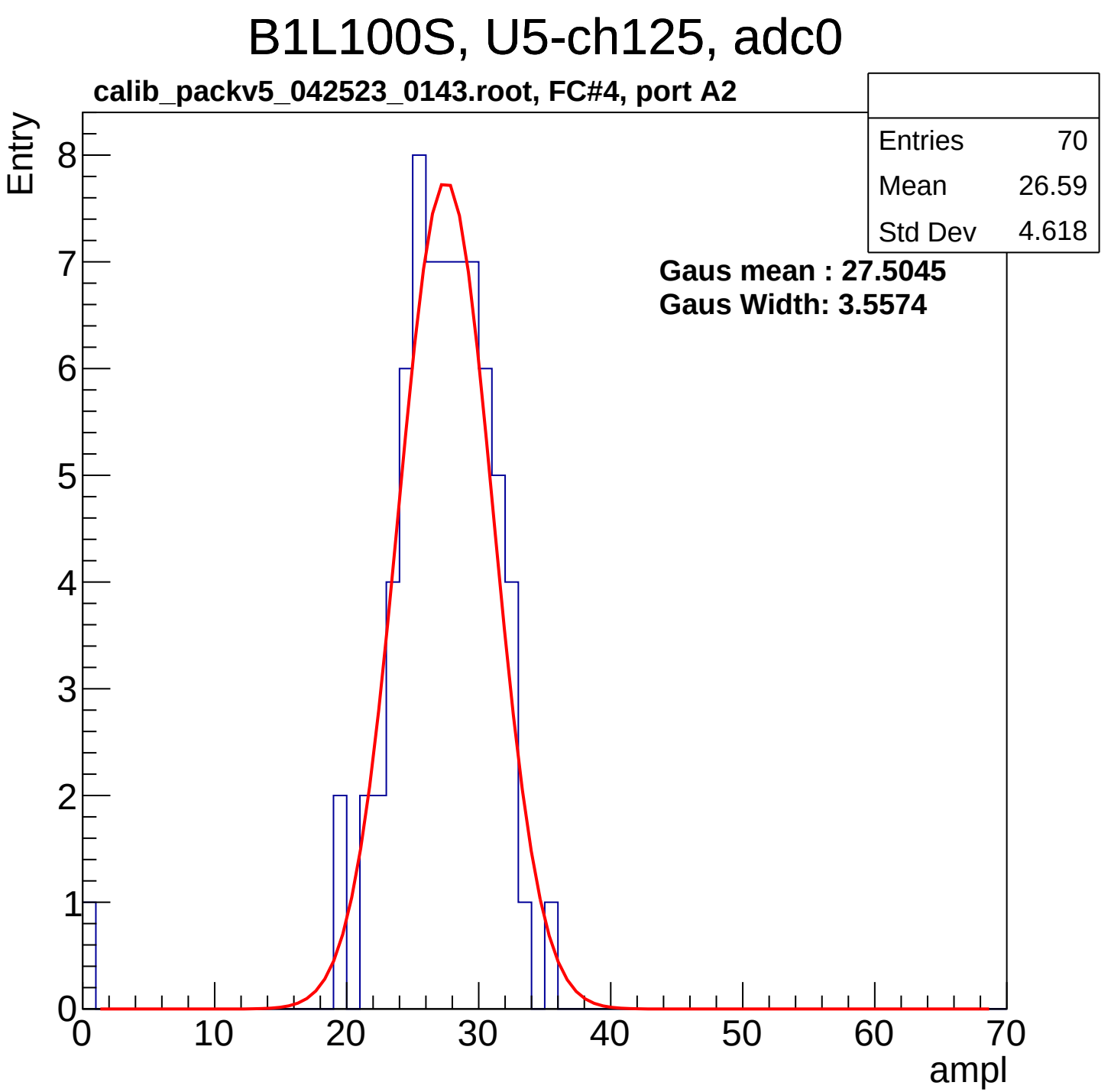

B1L100S, U5-ch124, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 49.25
Std Dev 3.472
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

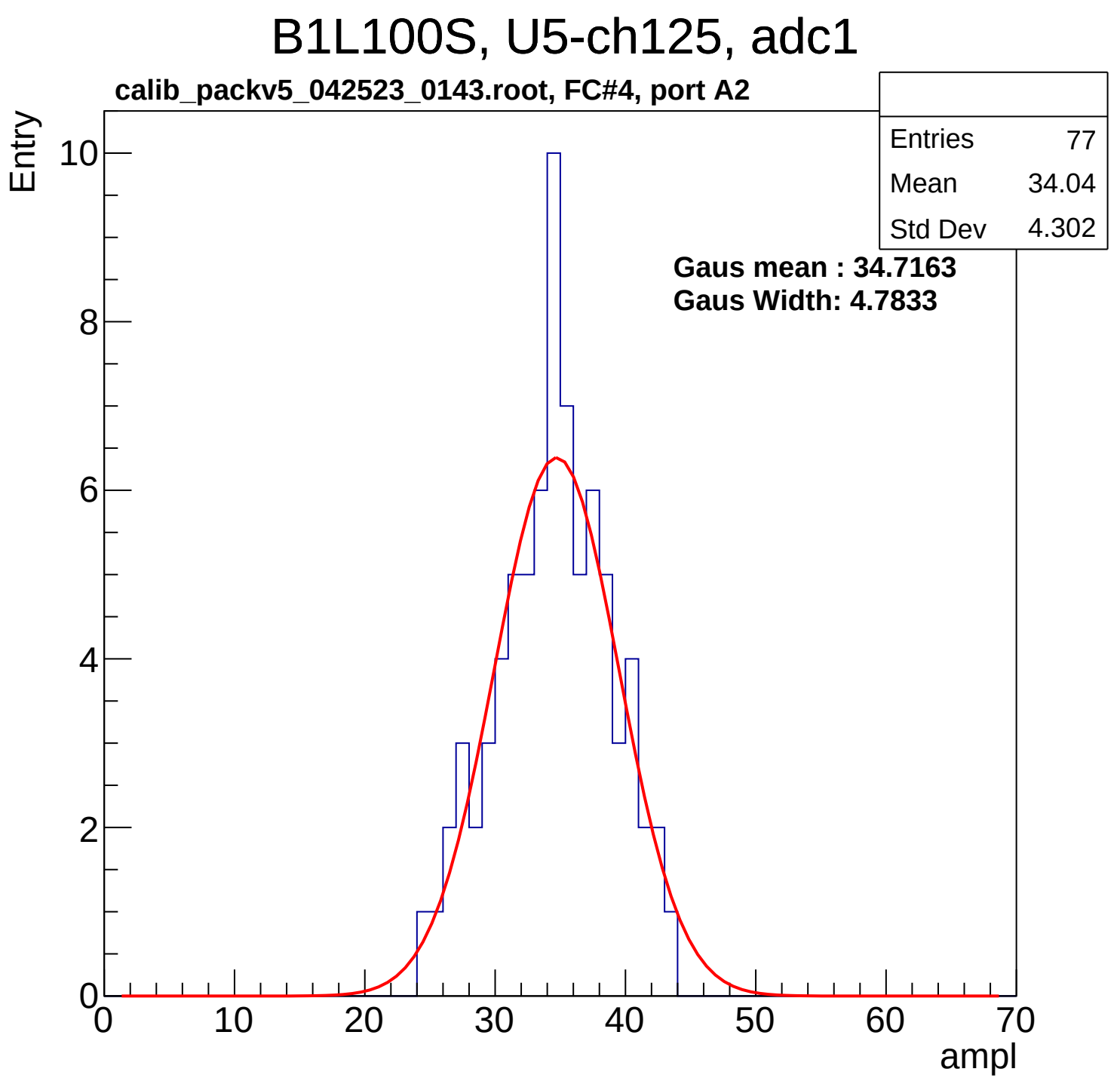

B1L100S, U5-ch124, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 55.17
Std Dev 3.066
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

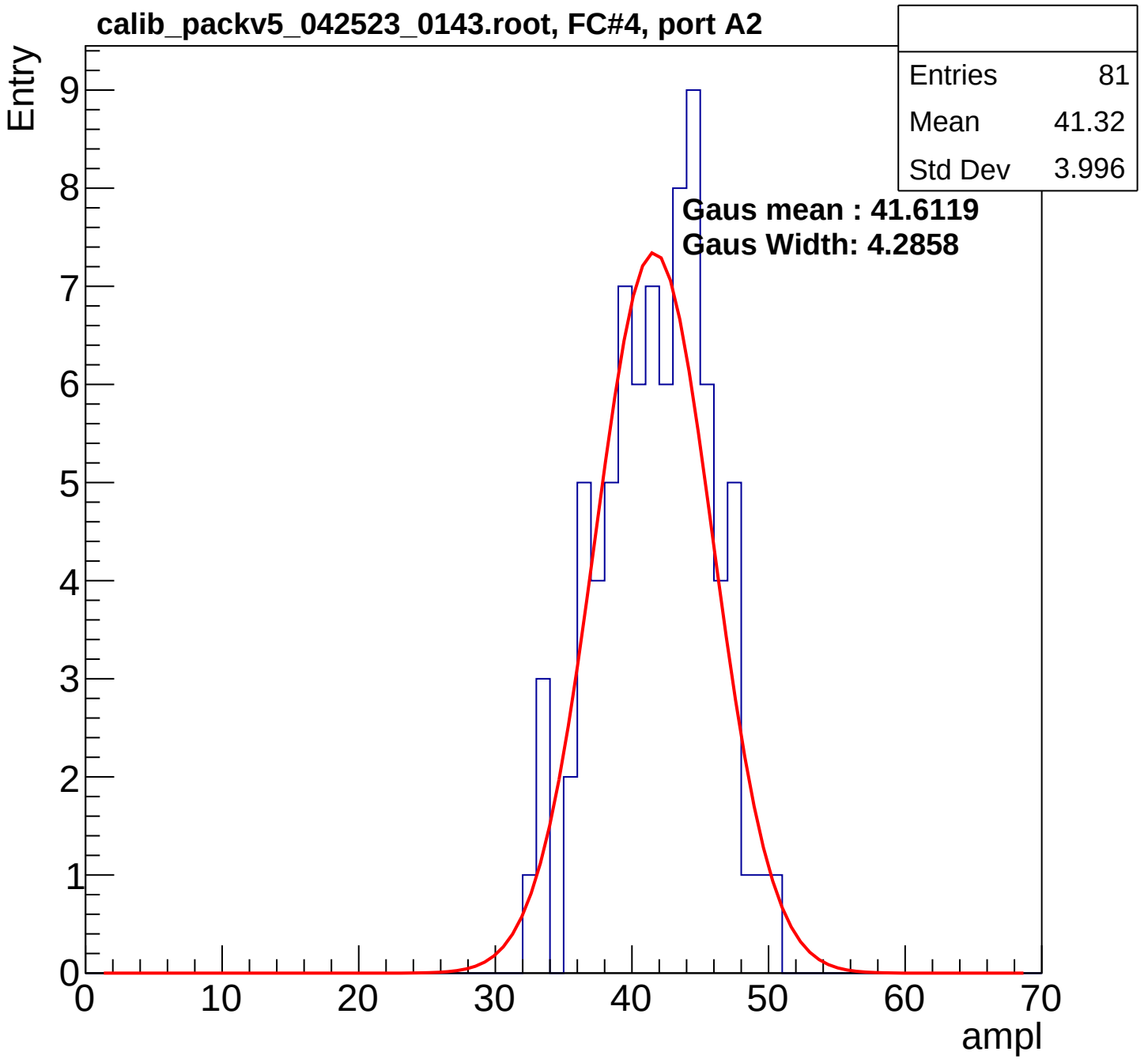

B1L100S, U5-ch124, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 52
Mean 58.37
Std Dev 8.669
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

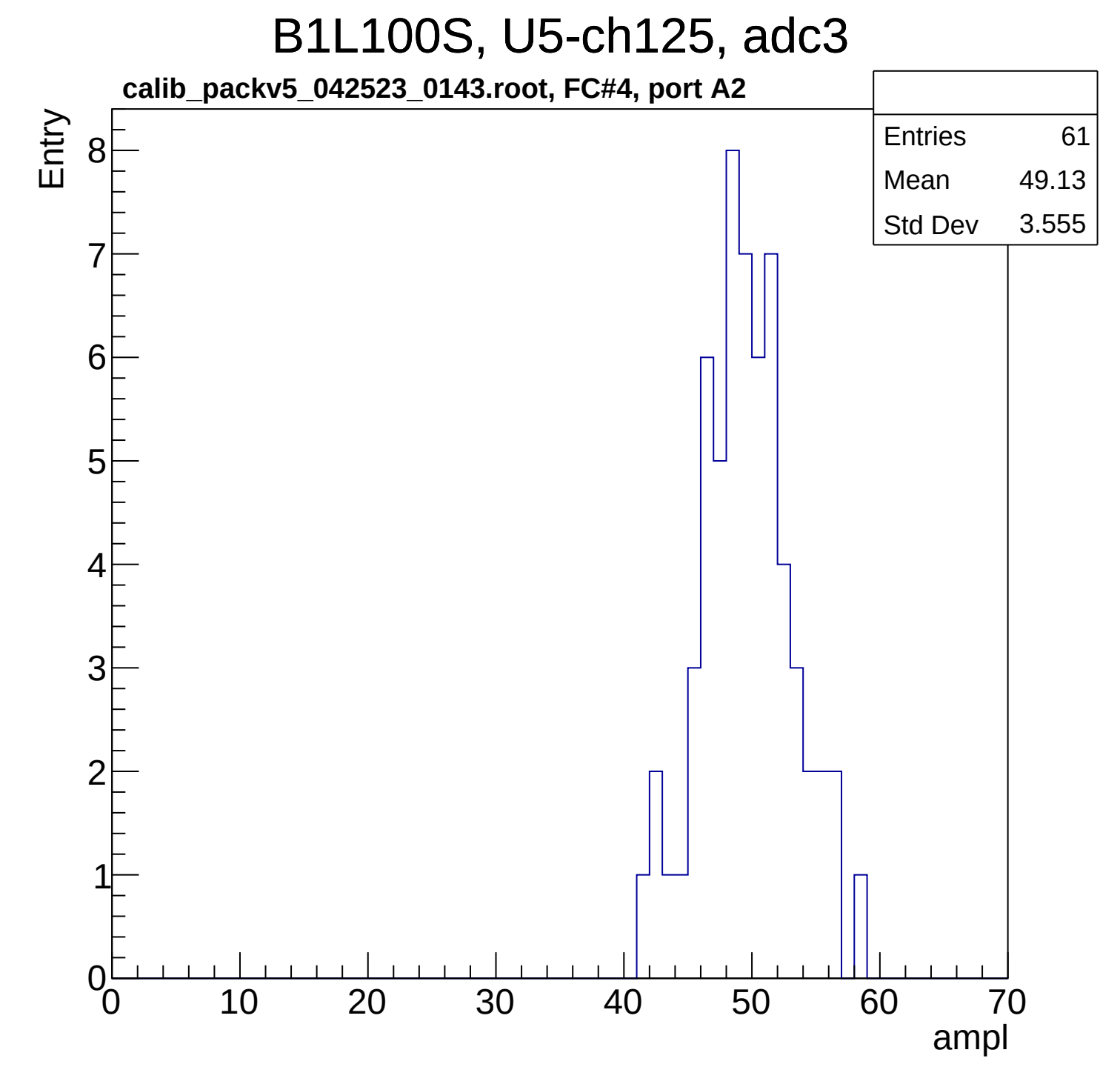

B1L100S, U5-ch124, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 7
Mean 61.71
Std Dev 1.03
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

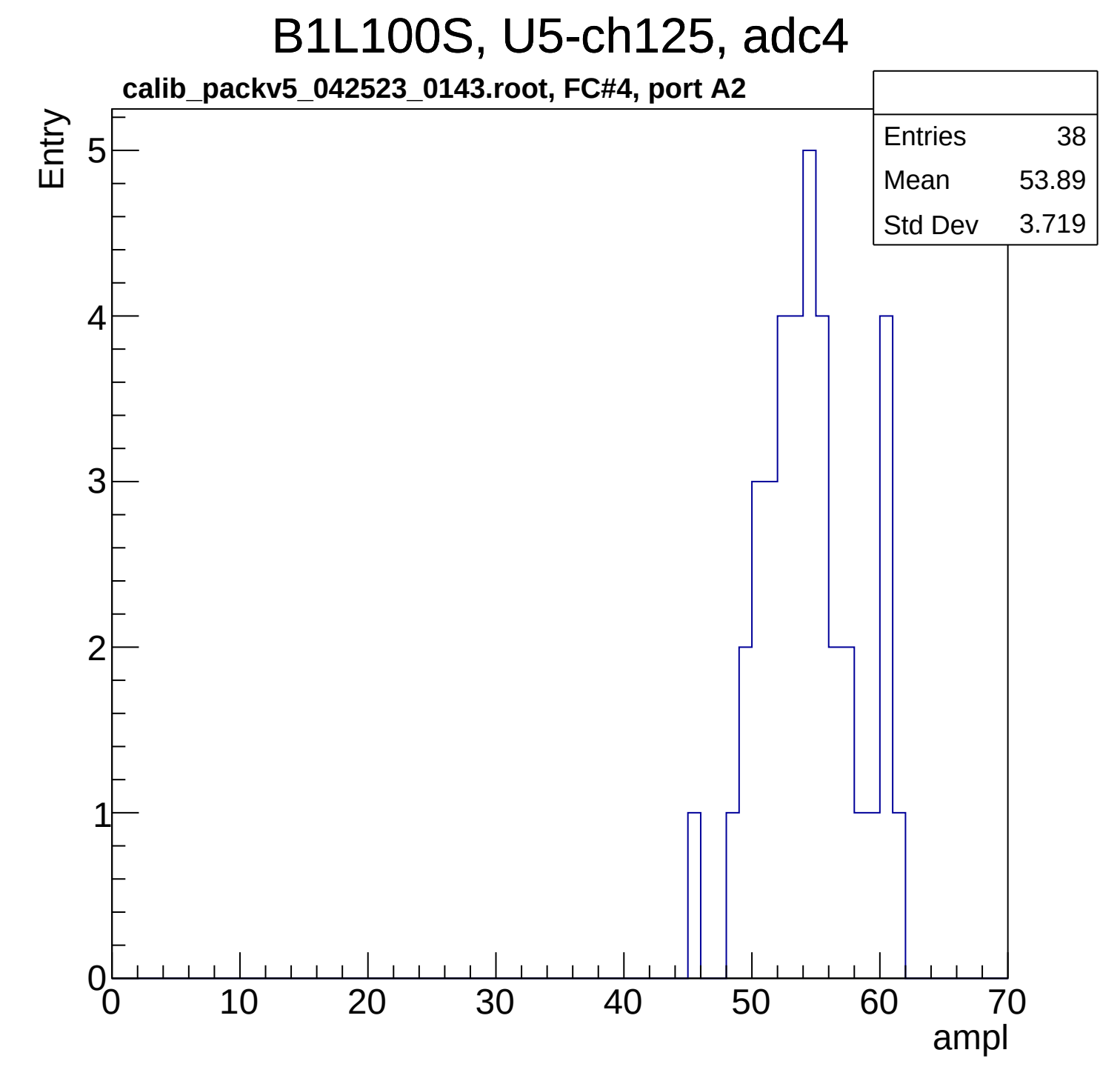

B1L100S, U5-ch124, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

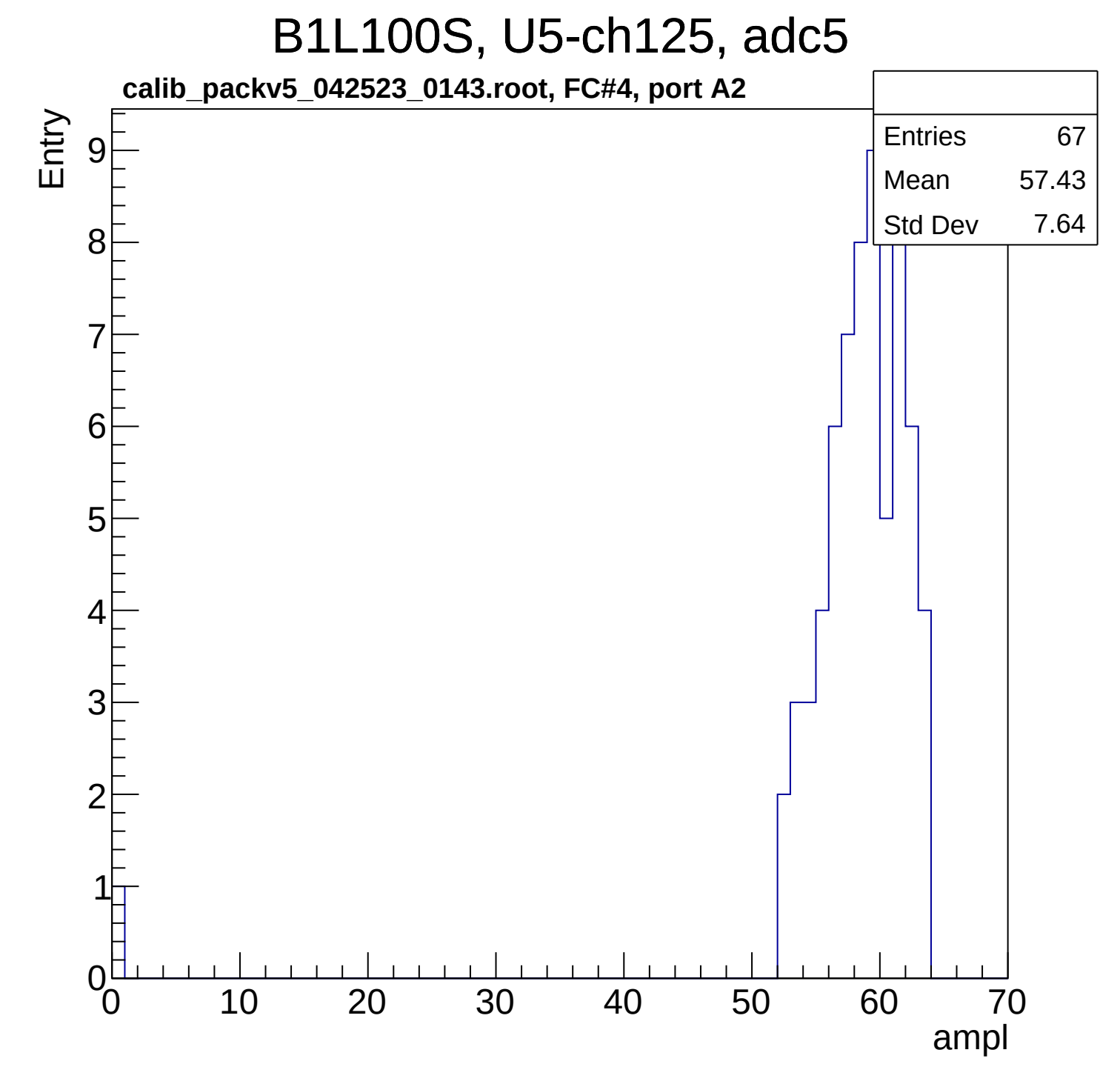

B1L100S, U5-ch125, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 26.59
Std Dev 4.618
Gaus mean : 27.5045
Gaus Width: 3.5574
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

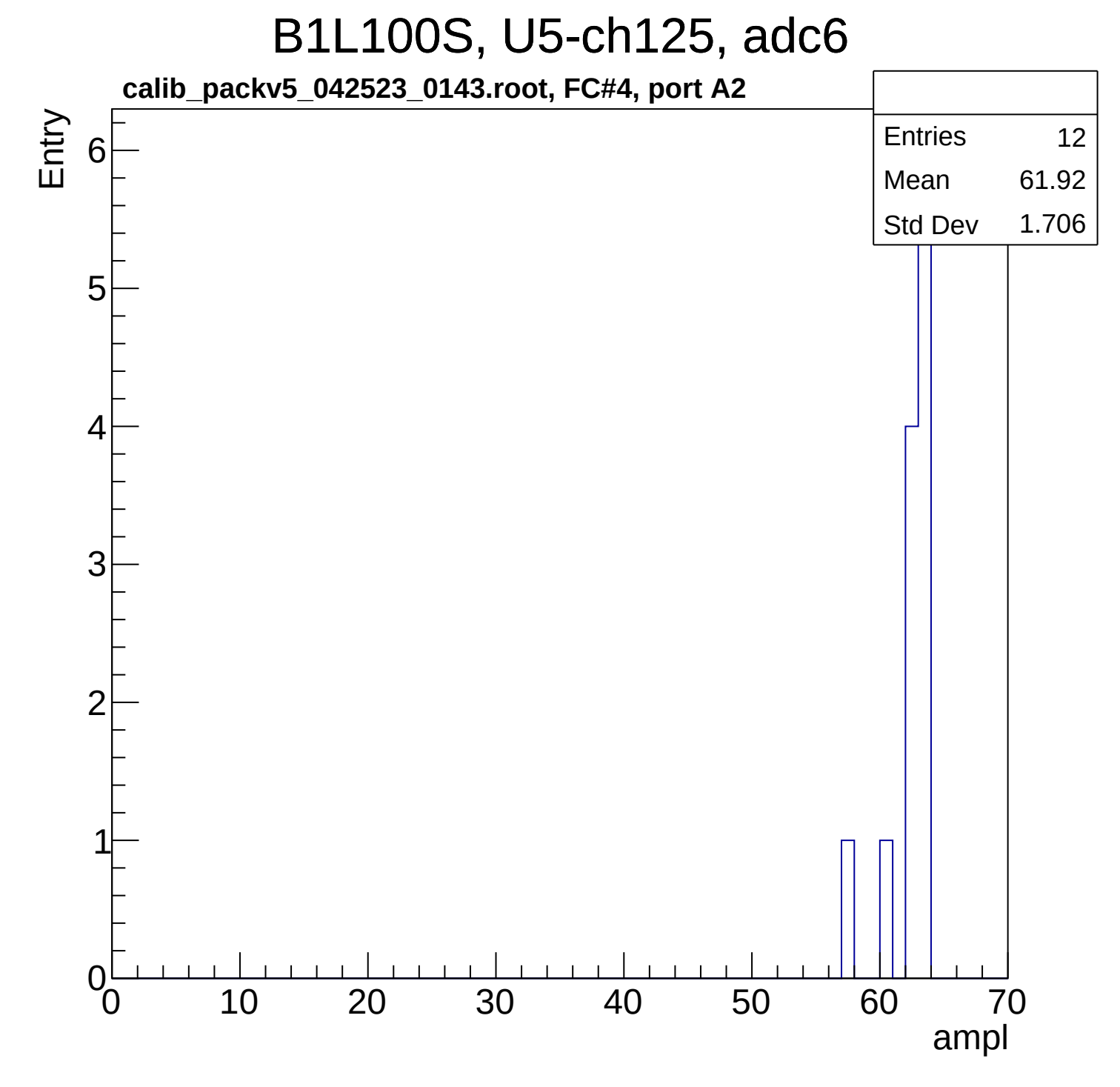

B1L100S, U5-ch125, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 77
Mean 34.04
Std Dev 4.302
Gaus mean : 34.7163
Gaus Width: 4.7833
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

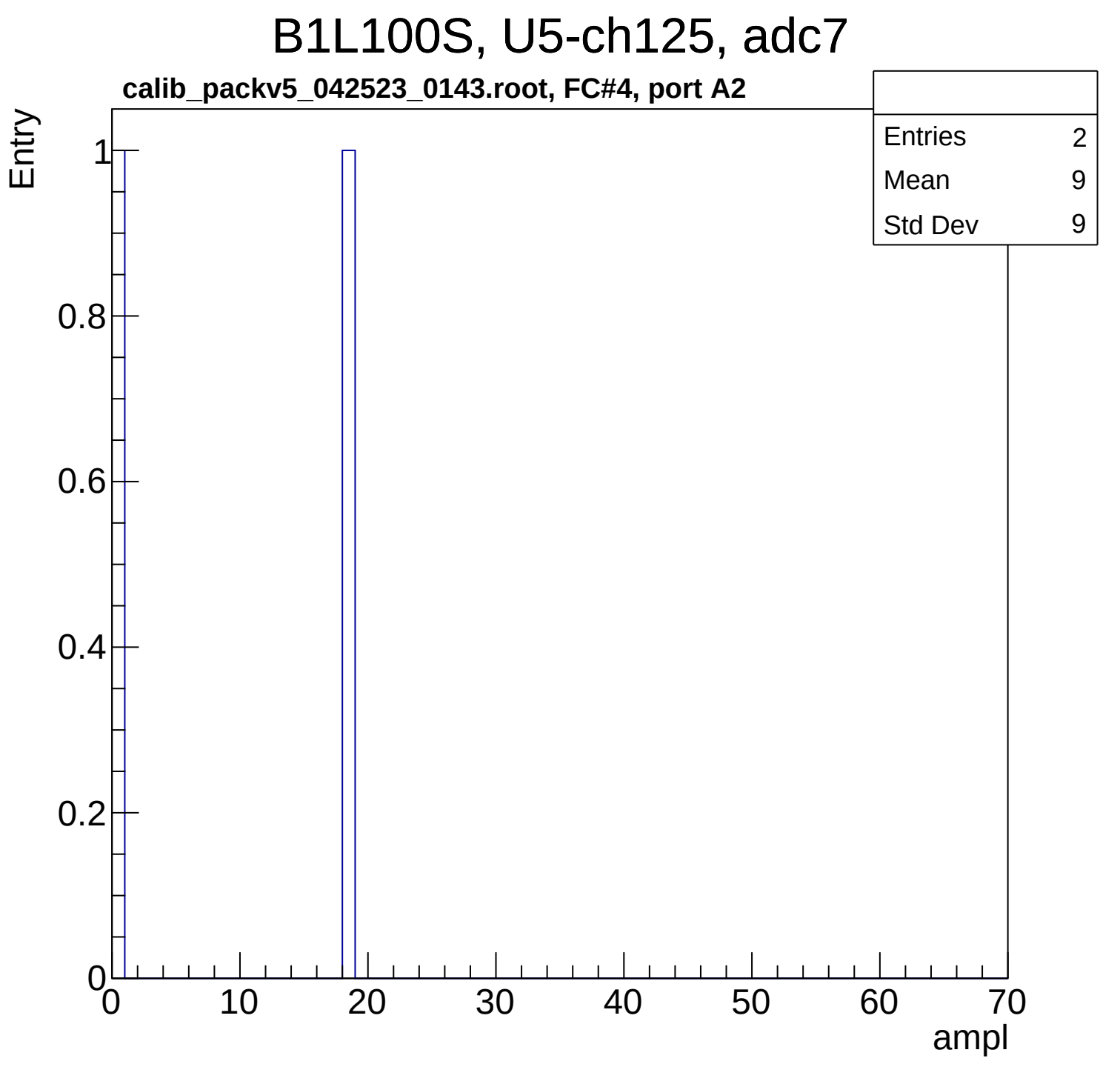

B1L100S, U5-ch125, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 81
Mean 41.32
Std Dev 3.996
Gaus mean : 41.6119
Gaus Width: 4.2858
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

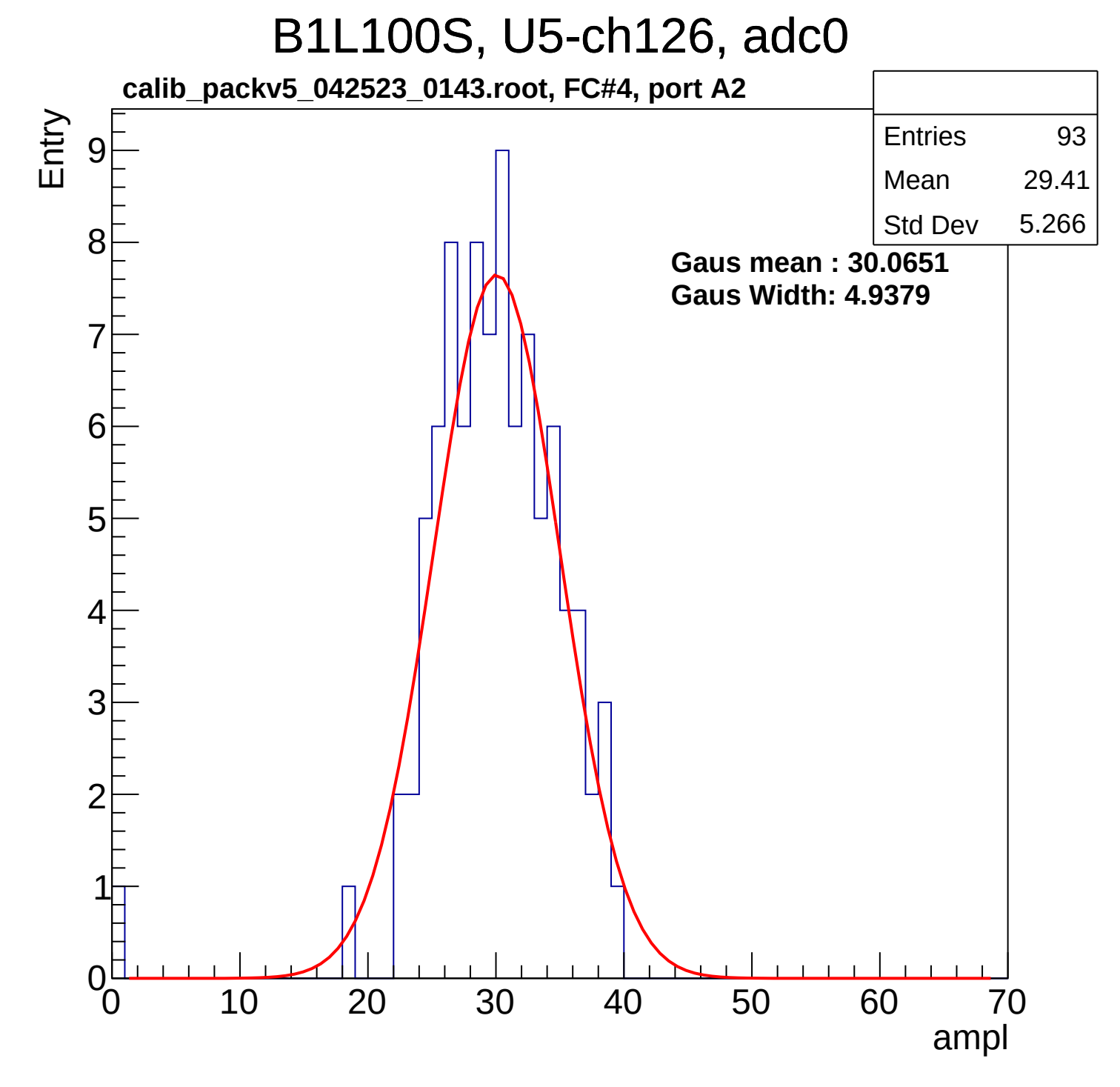

B1L100S, U5-ch125, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 49.13
Std Dev 3.555
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

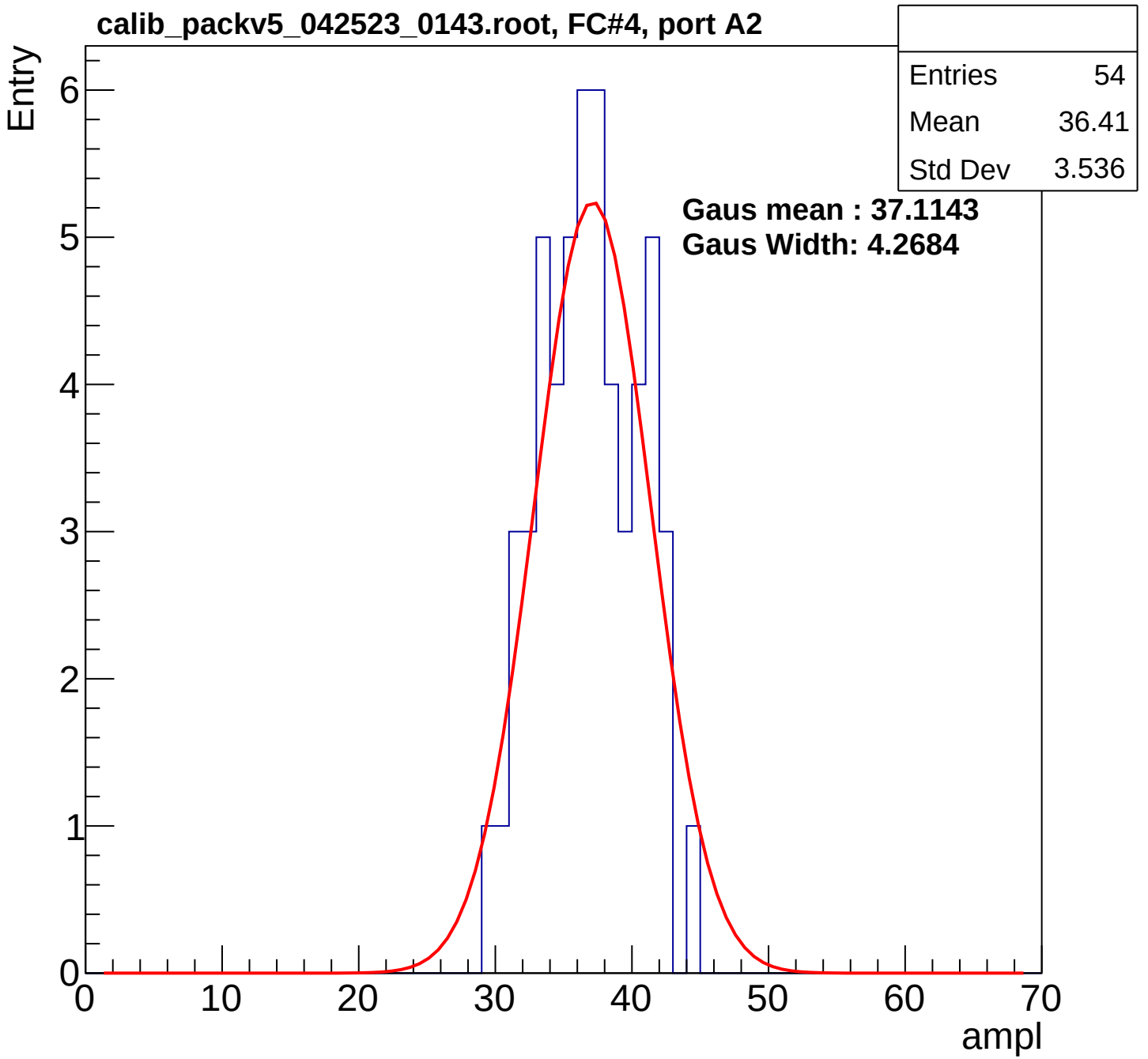

B1L100S, U5-ch125, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 38
Mean 53.89
Std Dev 3.719
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

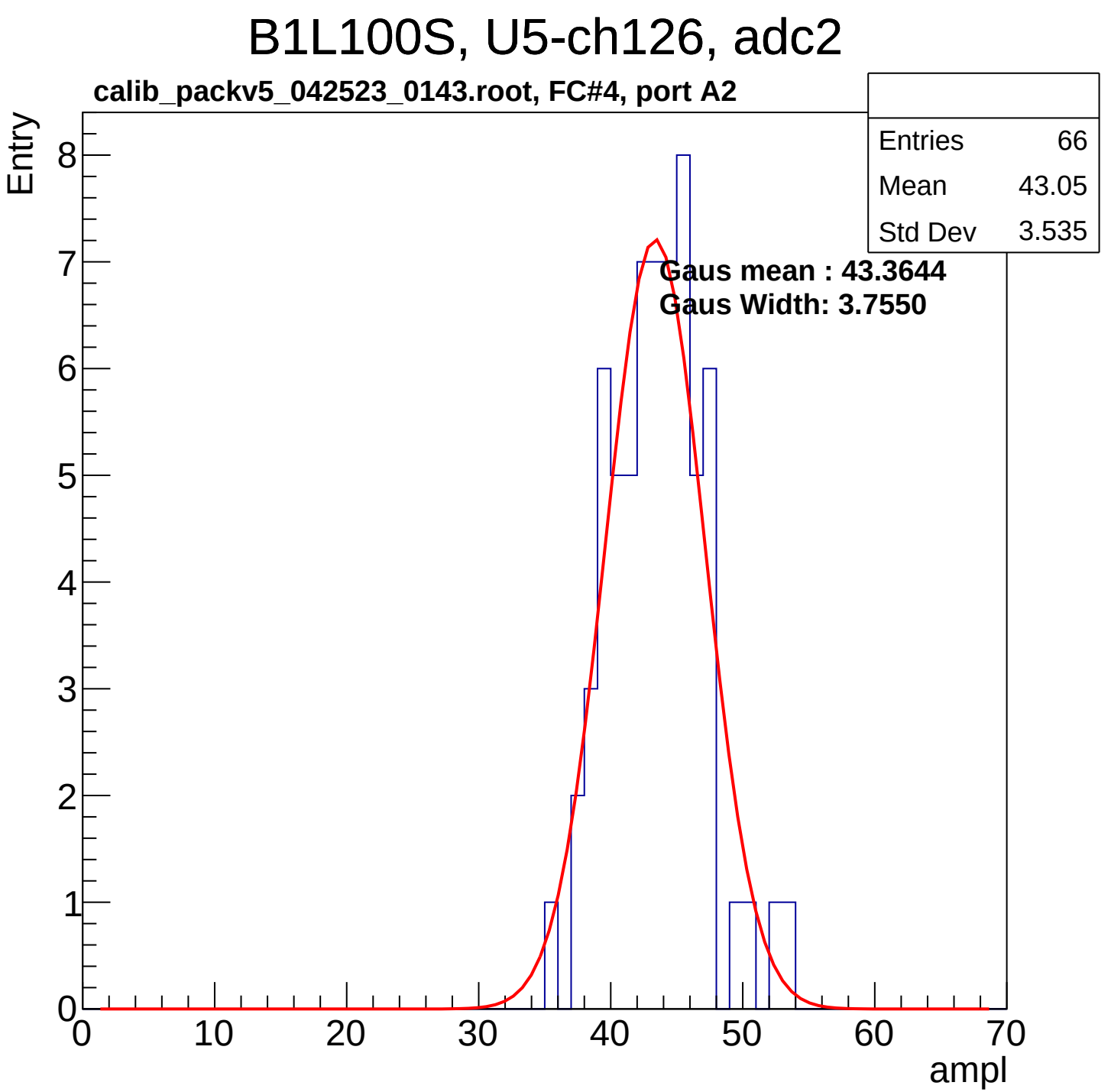

B1L100S, U5-ch125, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 57.43
Std Dev 7.64
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

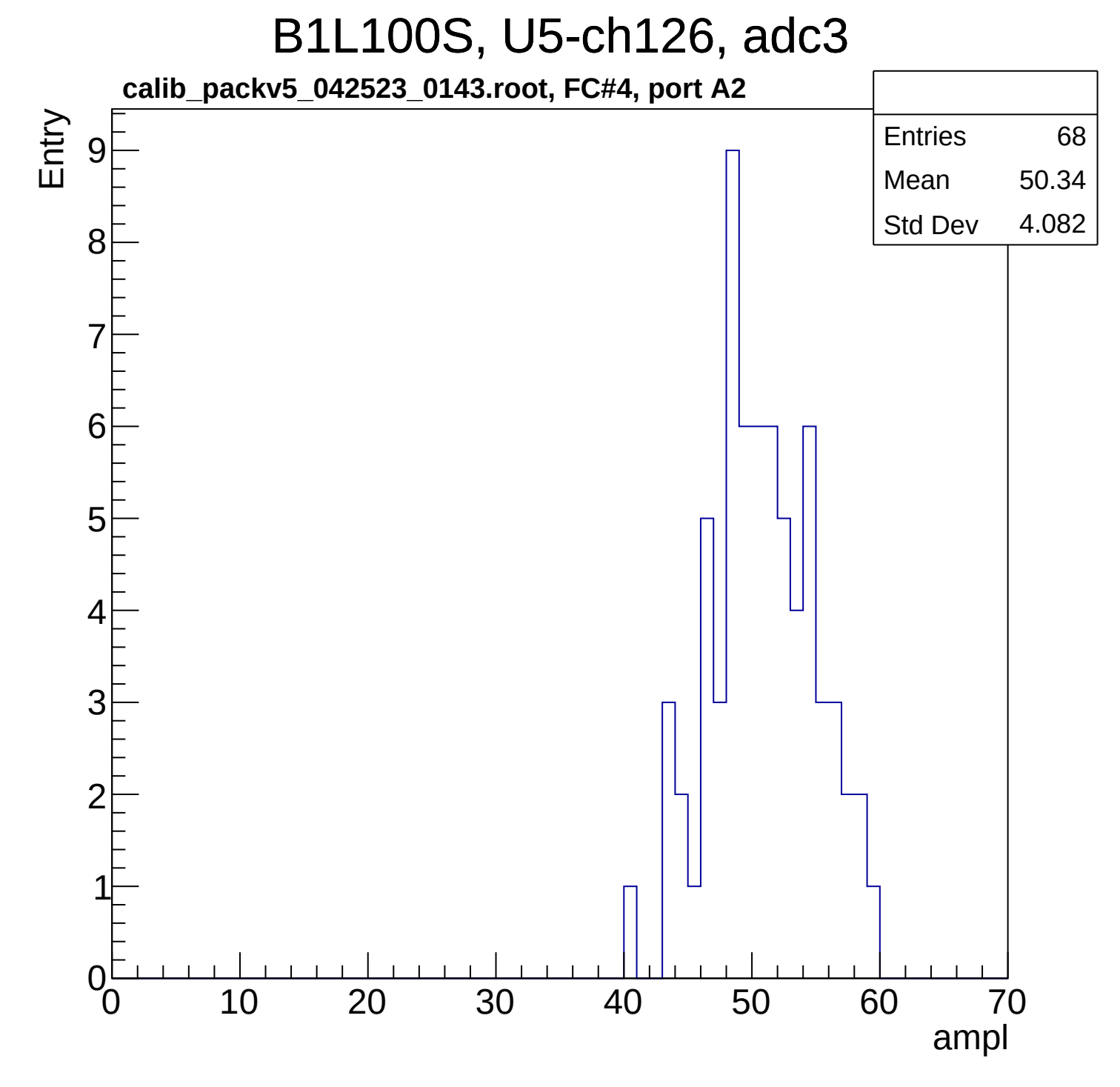

B1L100S, U5-ch125, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 12
Mean 61.92
Std Dev 1.706
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

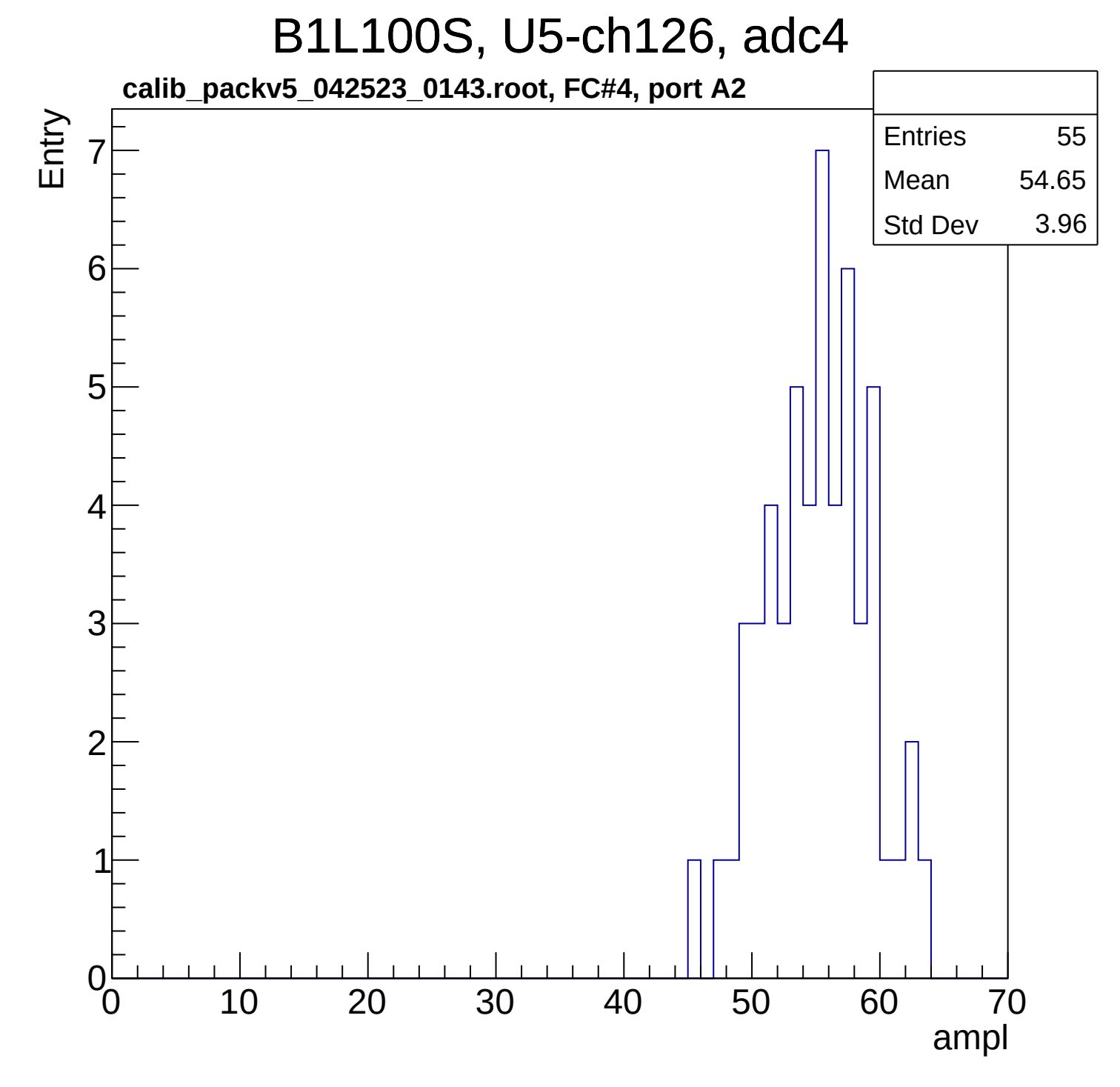

B1L100S, U5-ch125, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 9
Std Dev 9
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

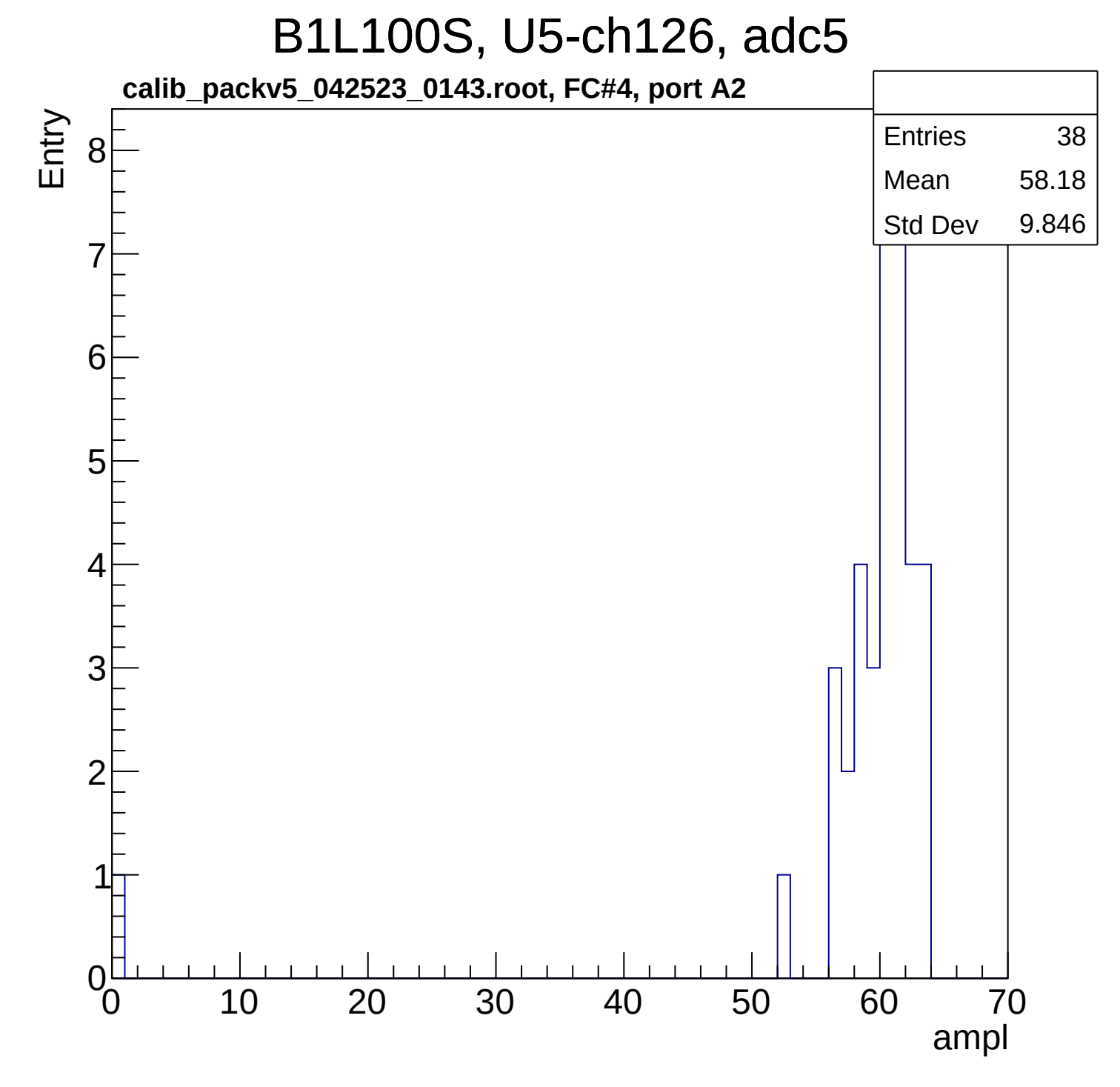

B1L100S, U5-ch126, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 93
Mean 29.41
Std Dev 5.266
Gaus mean : 30.0651
Gaus Width: 4.9379
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch126, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 36.41
Std Dev 3.536
Gaus mean : 37.1143
Gaus Width: 4.2684
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L100S, U5-ch126, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 43.05
Std Dev 3.535
Gaus mean : 43.3644
Gaus Width: 3.7550
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch126, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 50.34
Std Dev 4.082
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch126, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 54.65
Std Dev 3.96
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U5-ch126, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 38
Mean 58.18
Std Dev 9.846
Entry
0
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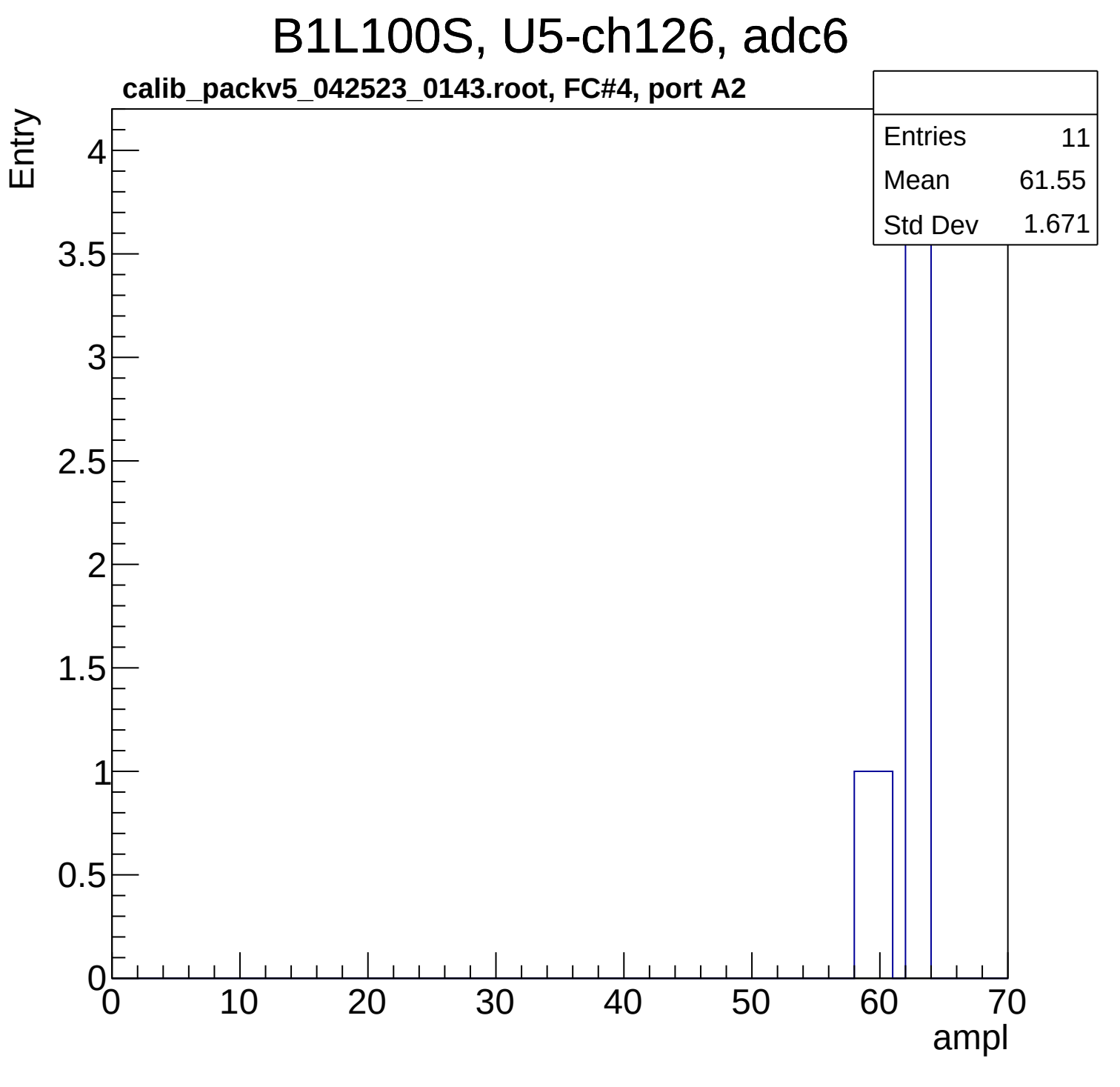
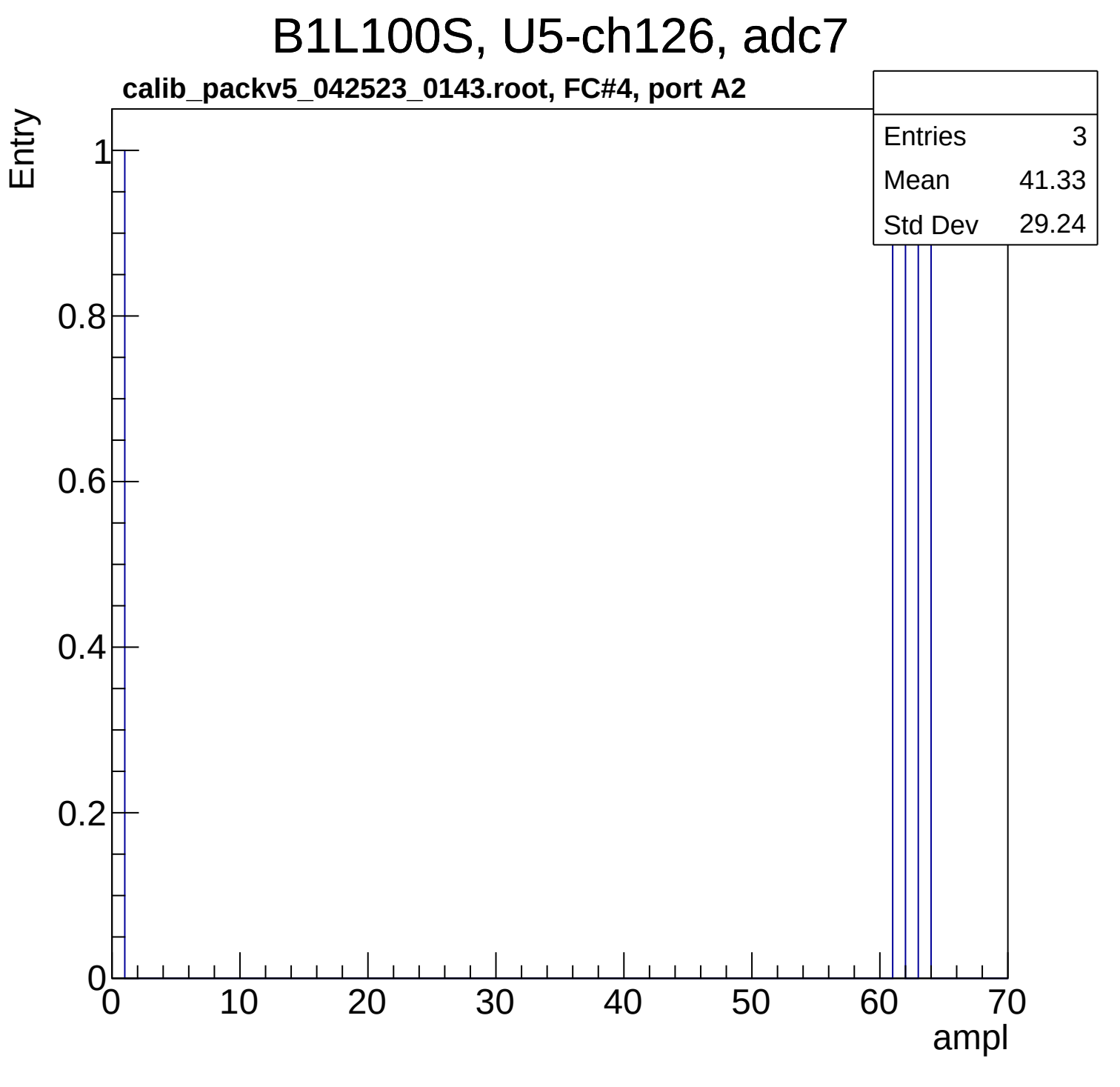
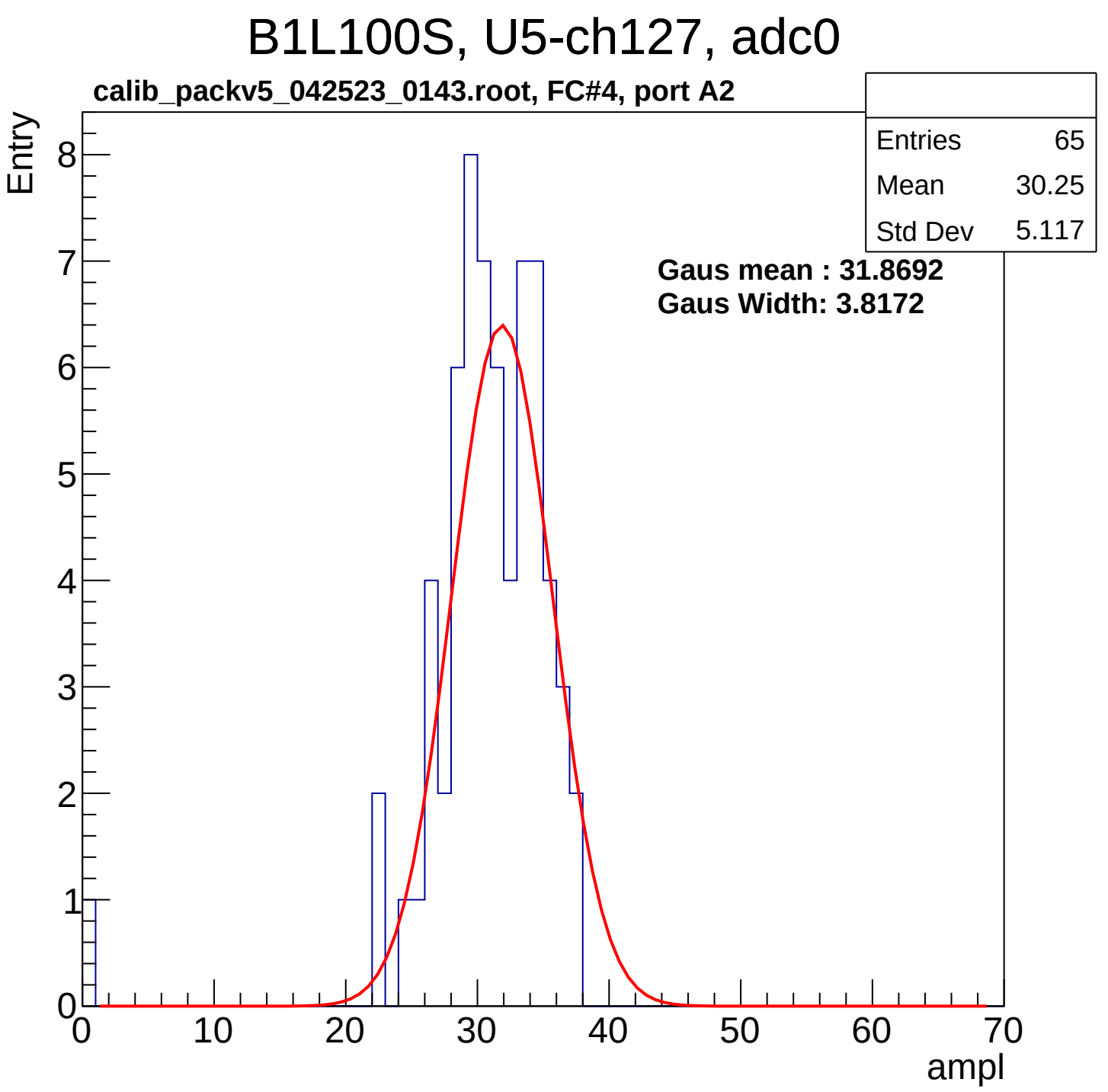
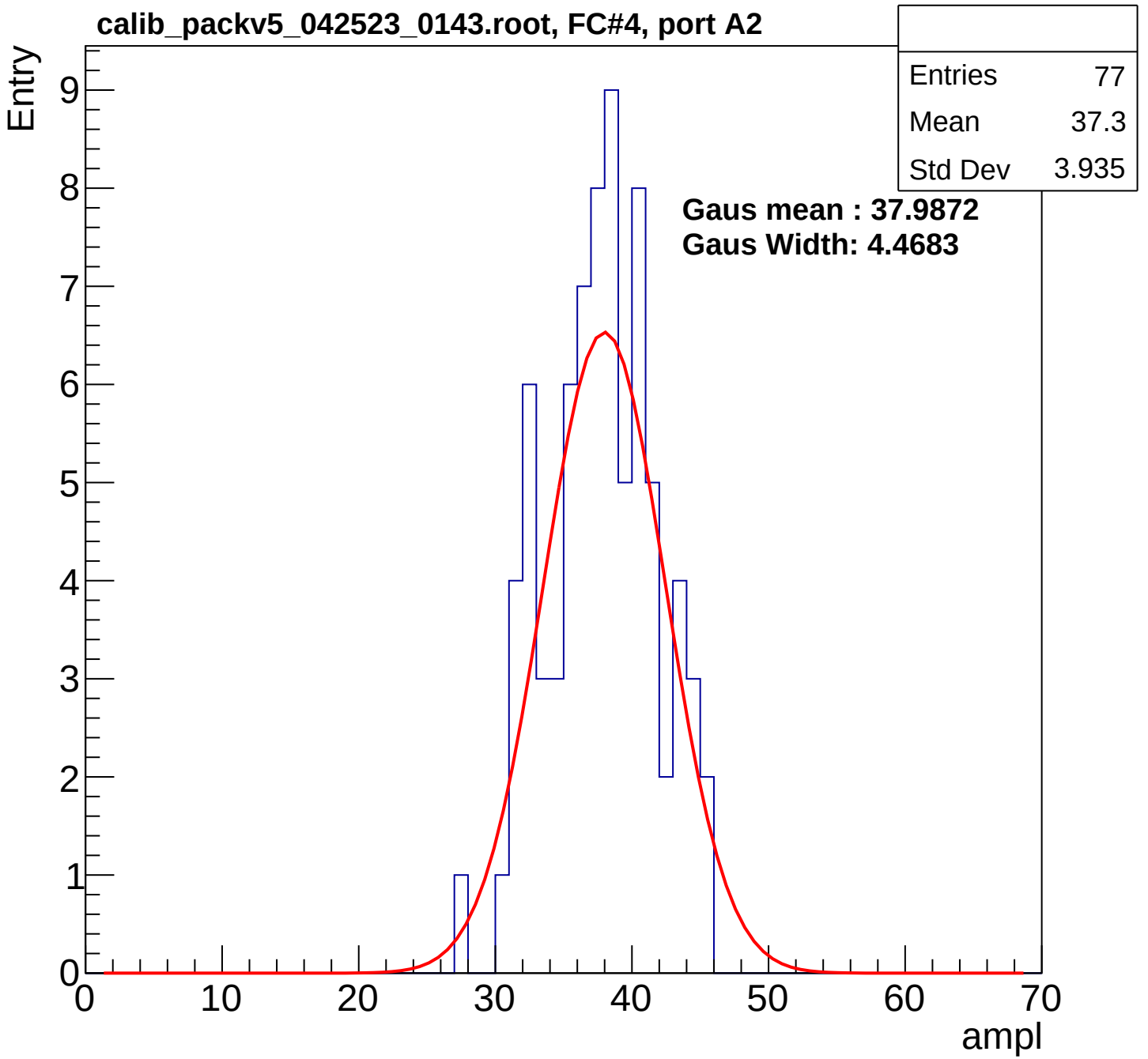
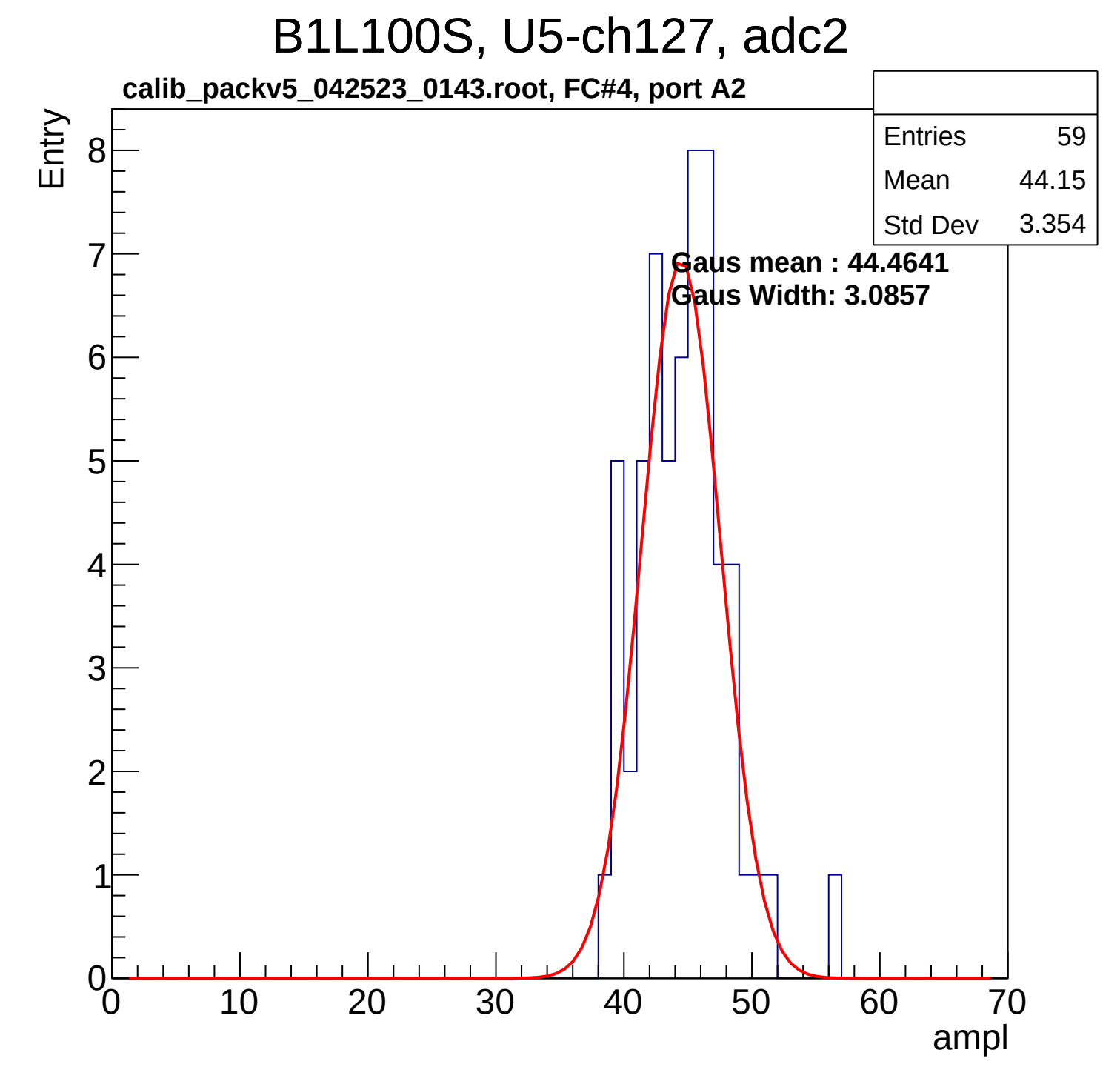
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

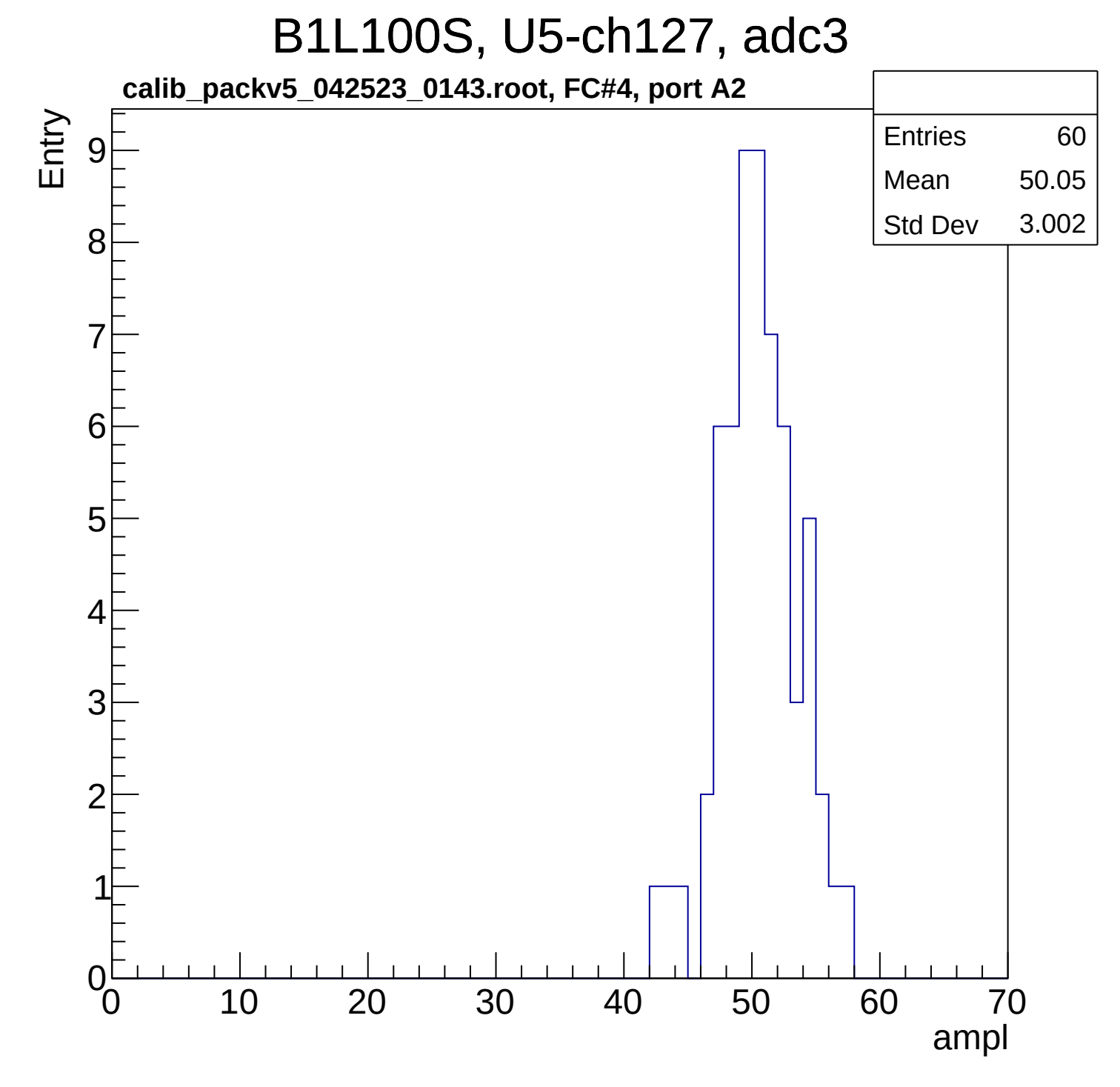

B1L100S, U5-ch126, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 11
Mean 61.55
Std Dev 1.671
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

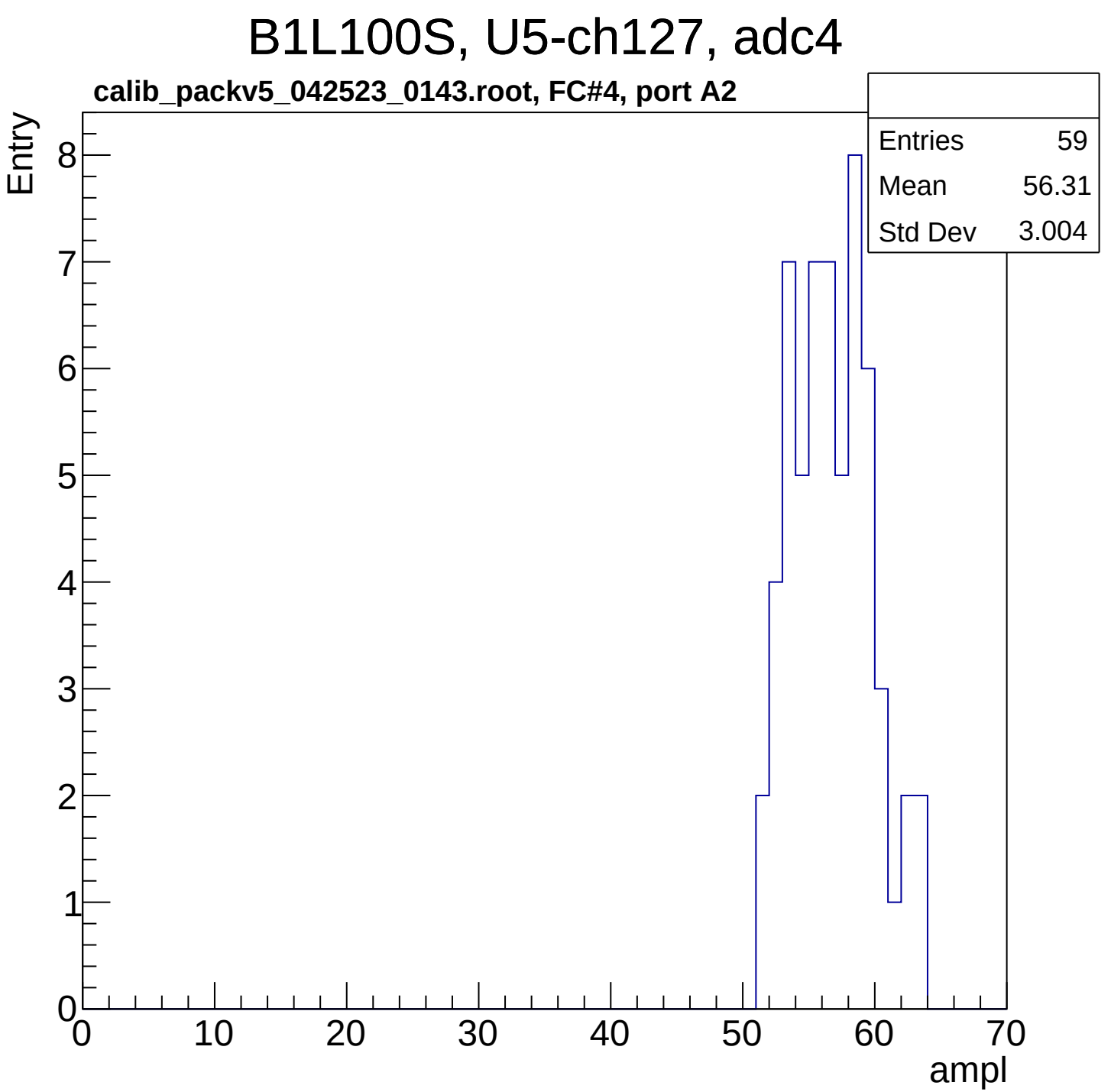

B1L100S, U5-ch126, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 41.33
Std Dev 29.24
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

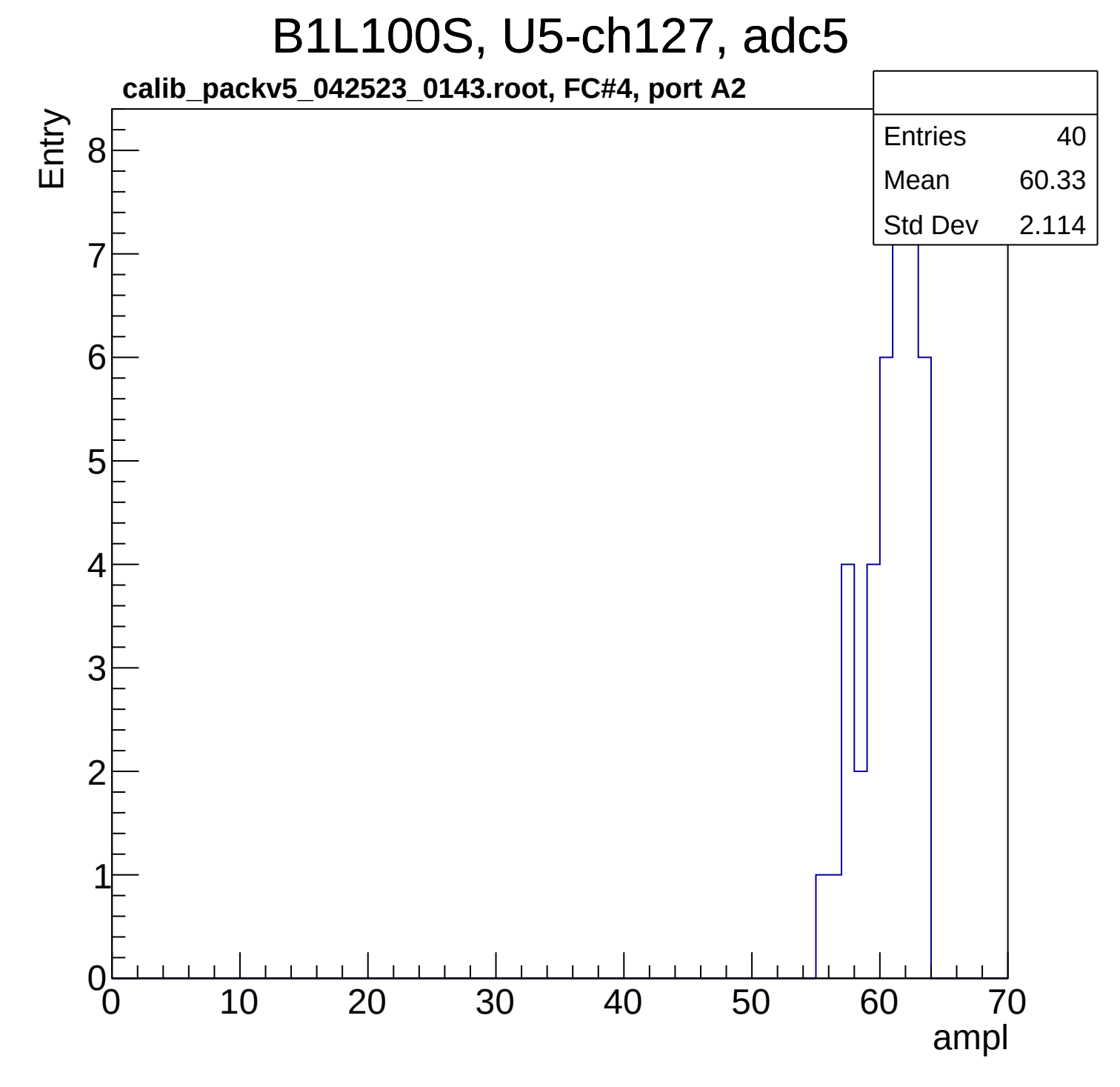

B1L100S, U5-ch127, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 30.25
Std Dev 5.117
Gaus mean : 31.8692
Gaus Width: 3.8172
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

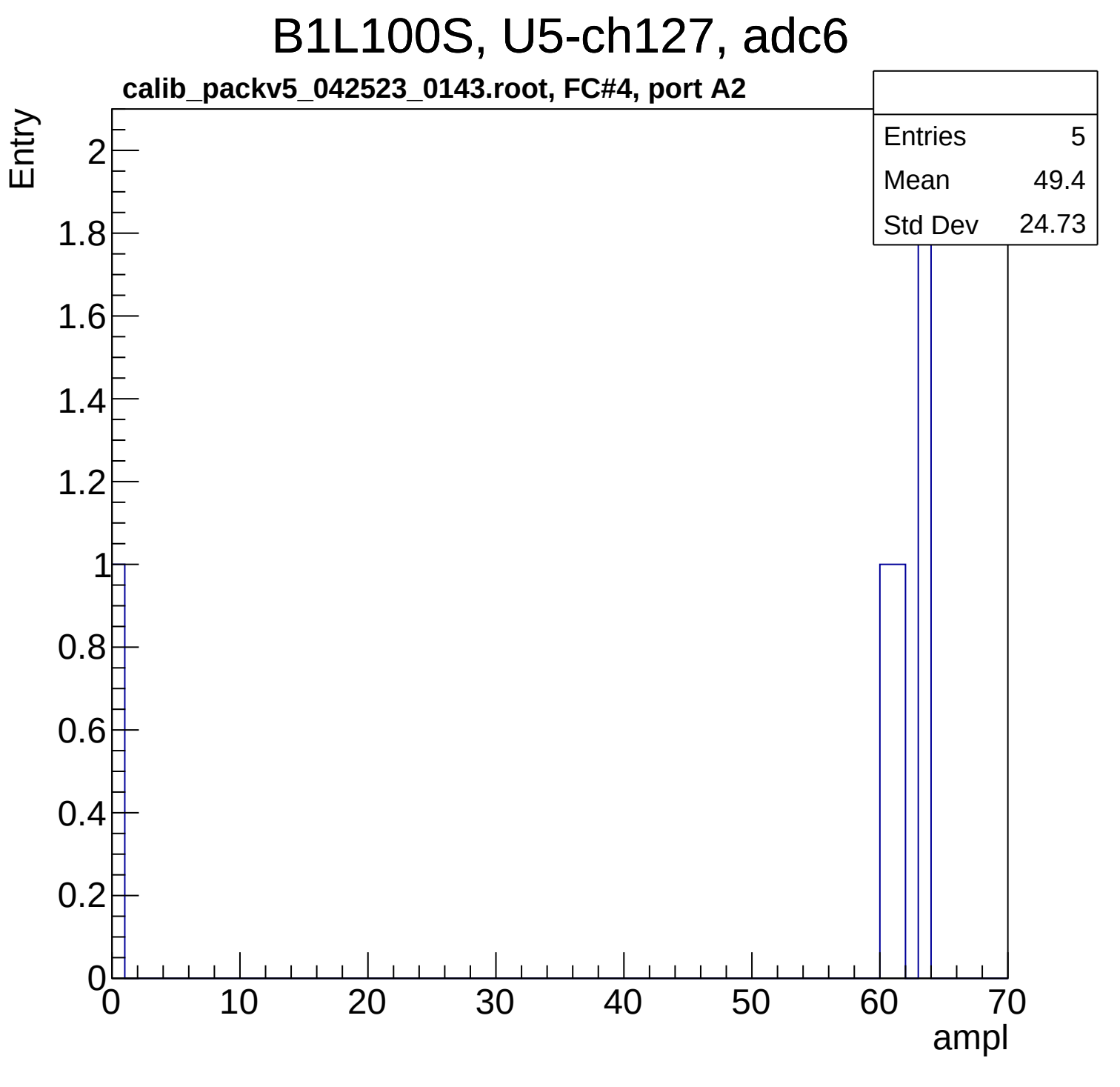

B1L100S, U5-ch127, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 77
Mean 37.3
Std Dev 3.935
Gaus mean : 37.9872
Gaus Width: 4.4683
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

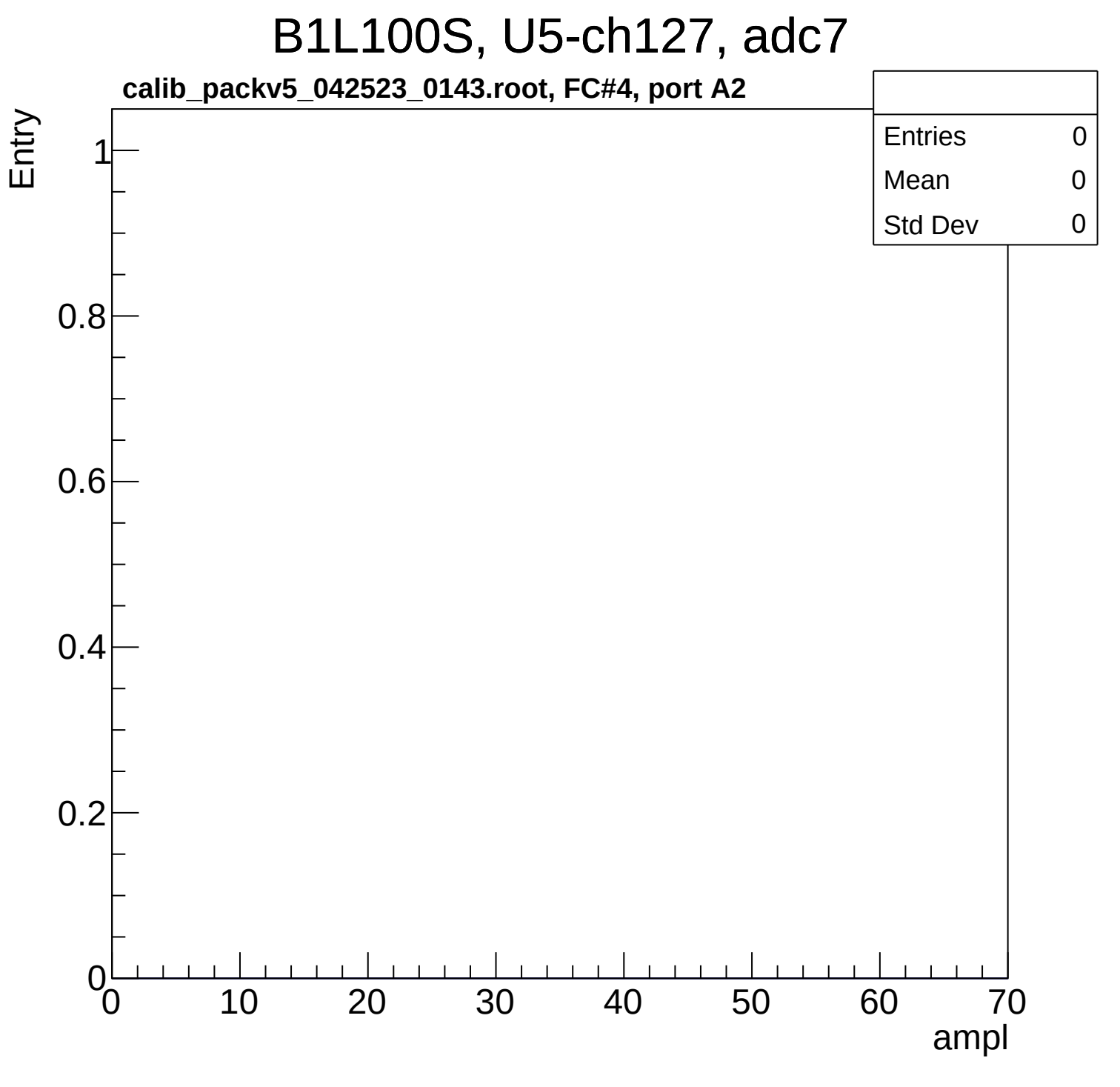

B1L100S, U5-ch127, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 44.15
Std Dev 3.354
Gaus mean : 44.4641
Gaus Width: 3.0857
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

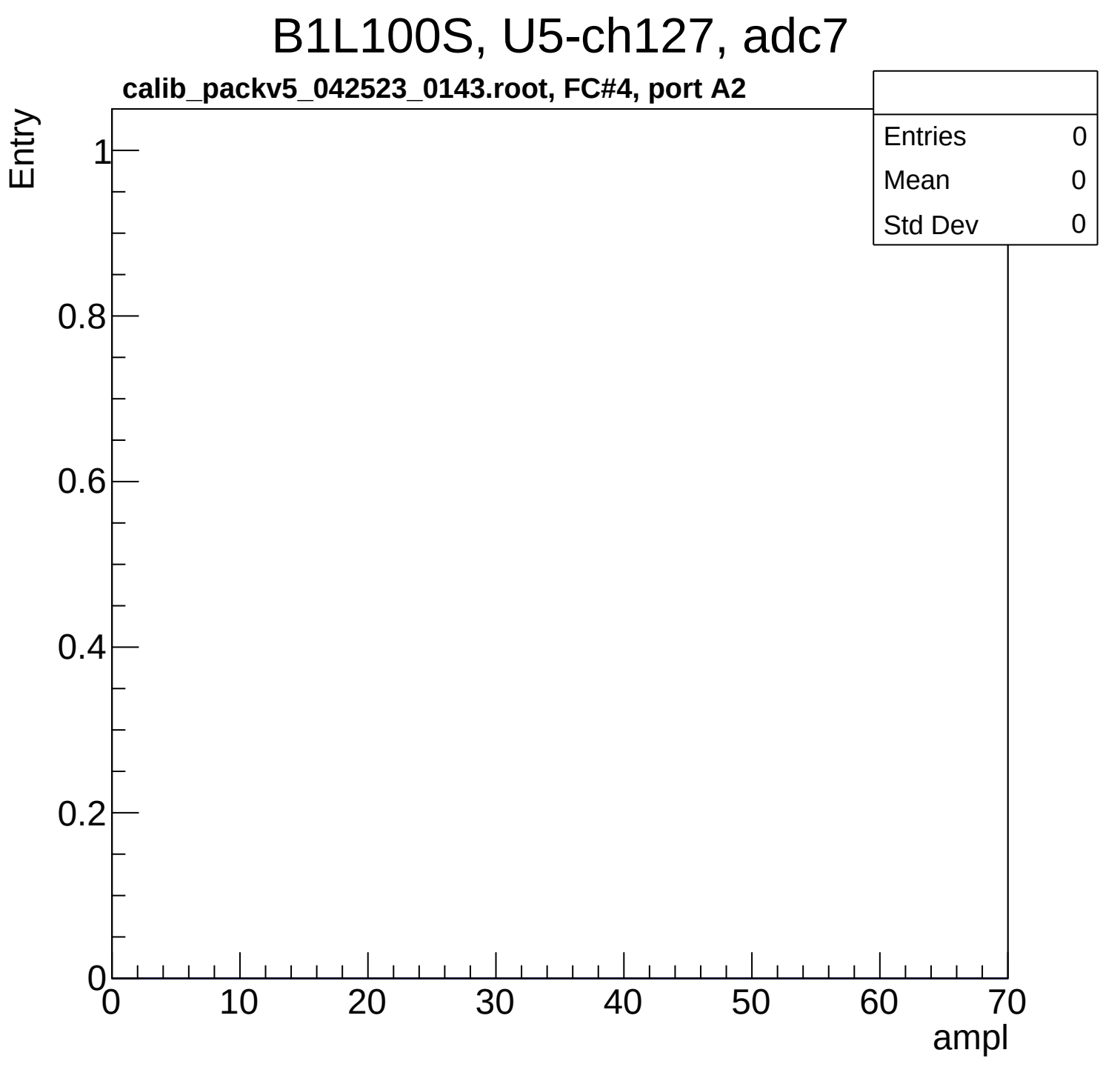

B1L100S, U5-ch127, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 50.05
Std Dev 3.002
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U5-ch127, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 56.31
Std Dev 3.004
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch127, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 40
Mean 60.33
Std Dev 2.114
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U5-ch127, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 5
Mean 49.4
Std Dev 24.73
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L100S, U5-ch127, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U5-ch127, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl