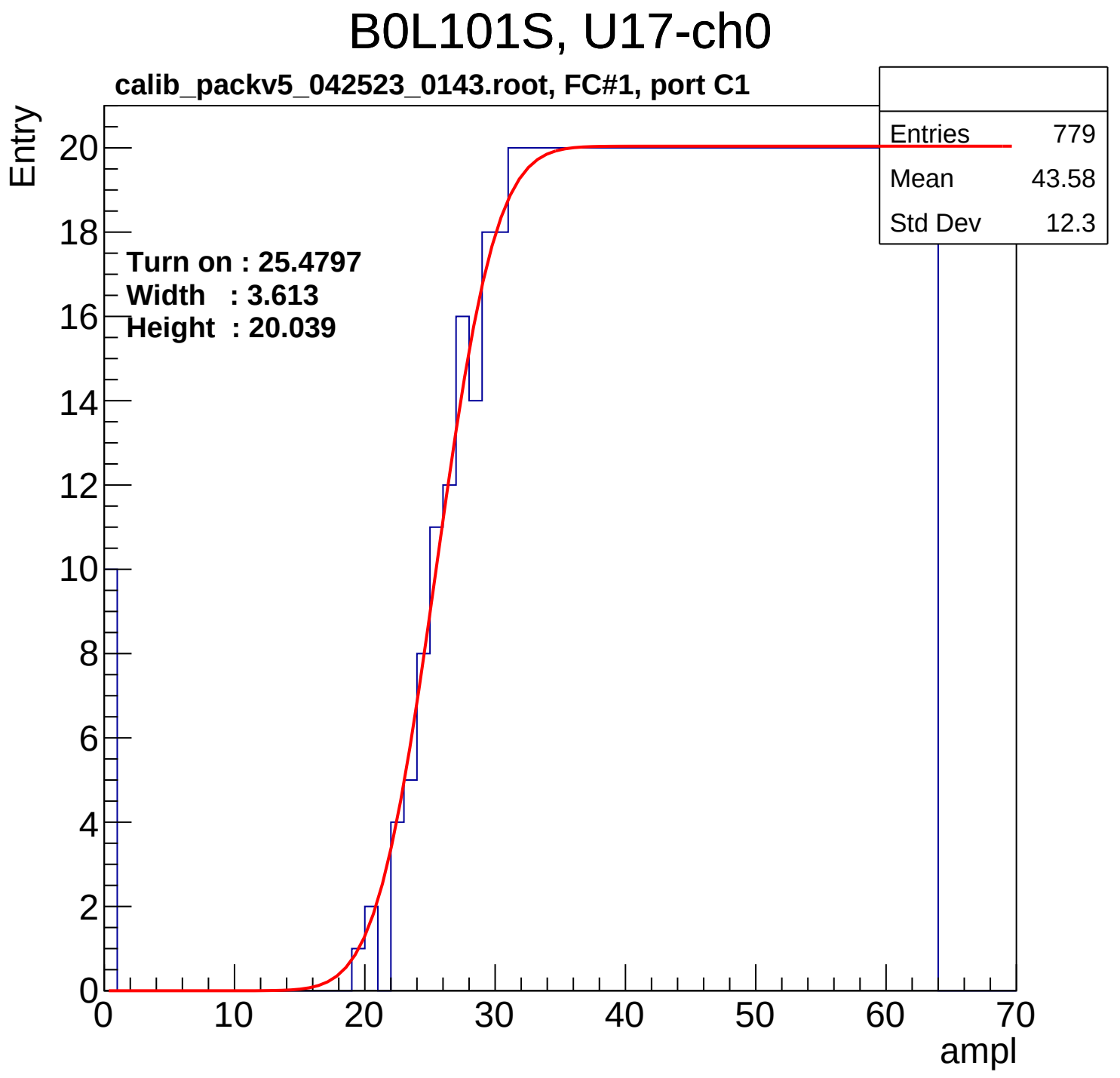
B0L101S, U17-ch0
calib_packv5_042523_0143.root, FC#1, port C1
Entries 779
Mean 43.58
Std Dev 12.3
Turn on : 25.4797
Width : 3.613
Height : 20.039
Entry
ampl
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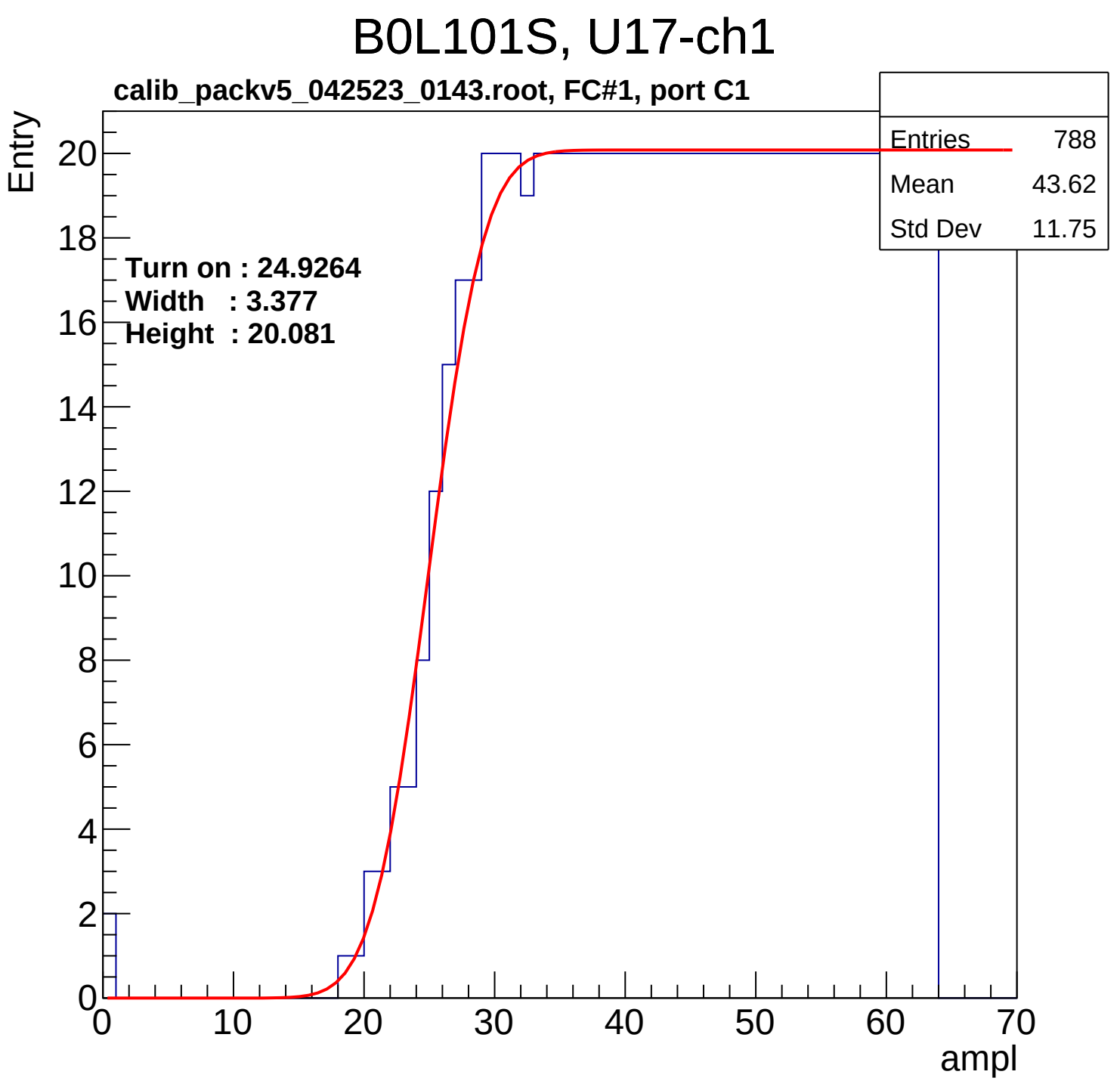
B0L101S, U17-ch1
calib_packv5_042523_0143.root, FC#1, port C1
Entries 788
Mean 43.62
Std Dev 11.75
Turn on : 24.9264
Width : 3.377
Height : 20.081
Entry
ampl
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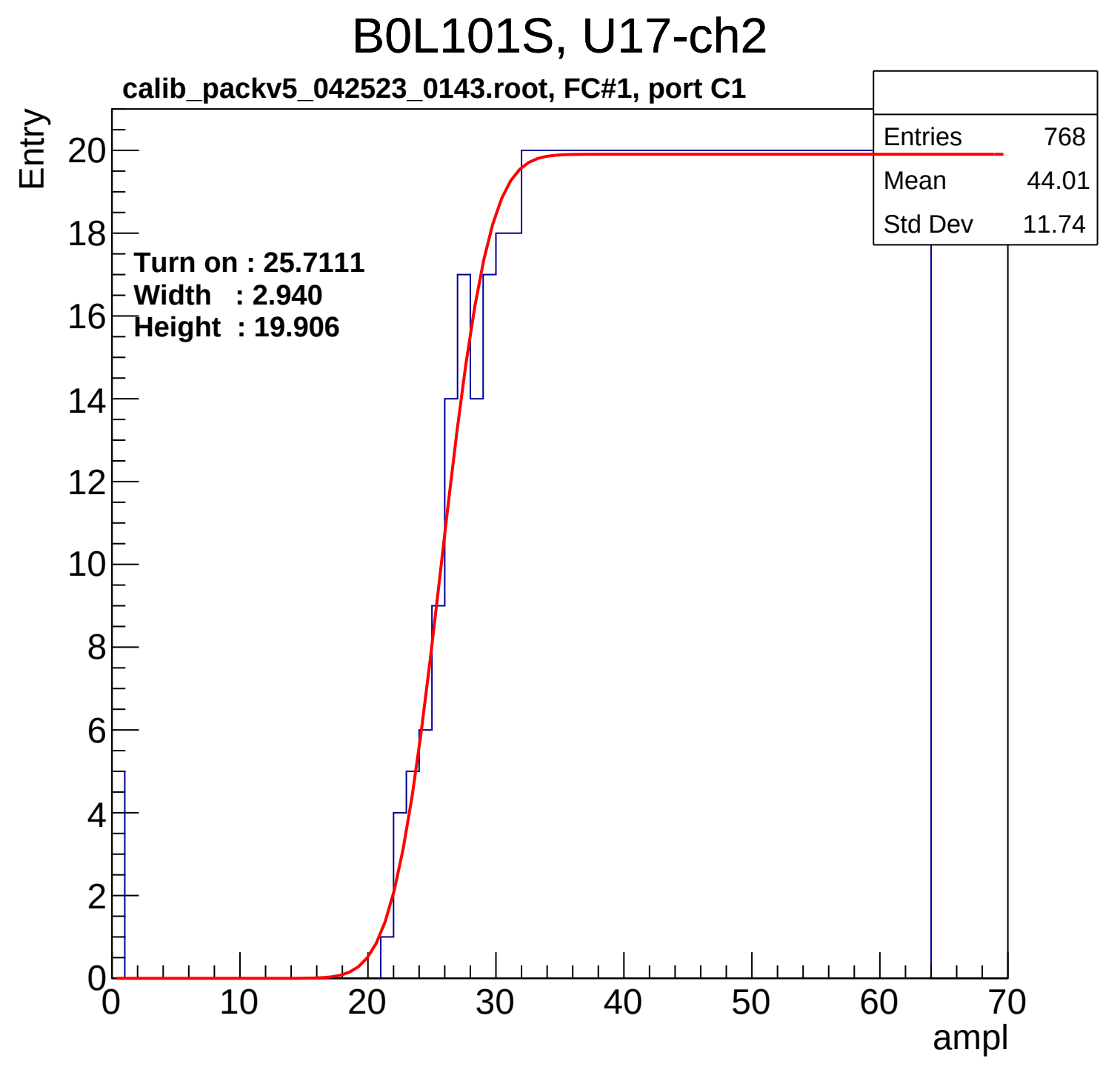
B0L101S, U17-ch2
calib_packv5_042523_0143.root, FC#1, port C1
Entries 768
Mean 44.01
Std Dev 11.74
Turn on : 25.7111
Width : 2.940
Height : 19.906
Entry
ampl
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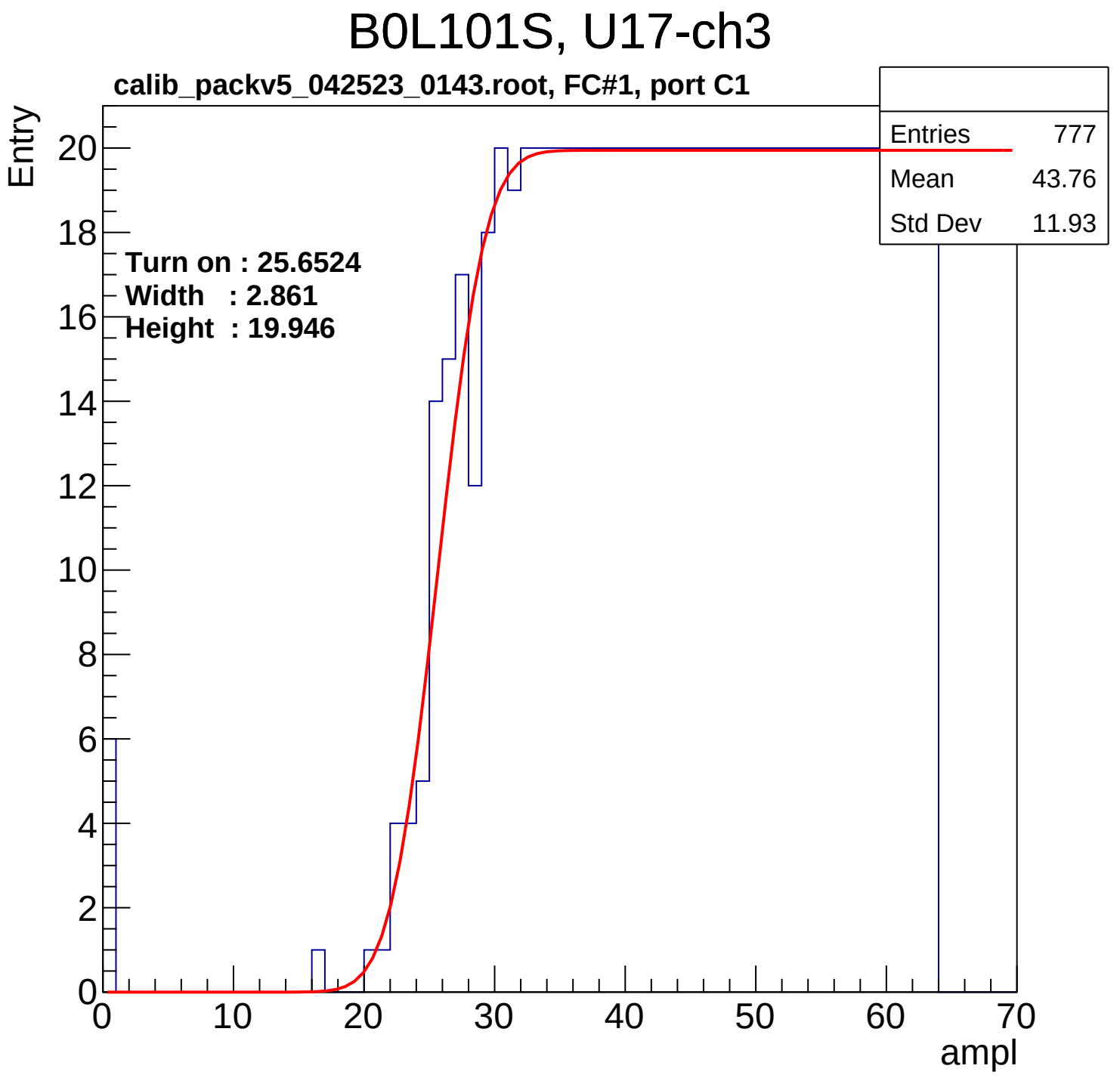
B0L101S, U17-ch3
calib_packv5_042523_0143.root, FC#1, port C1
Entries 777
Mean 43.76
Std Dev 11.93
Turn on : 25.6524
Width : 2.861
Height : 19.946
Entry
ampl
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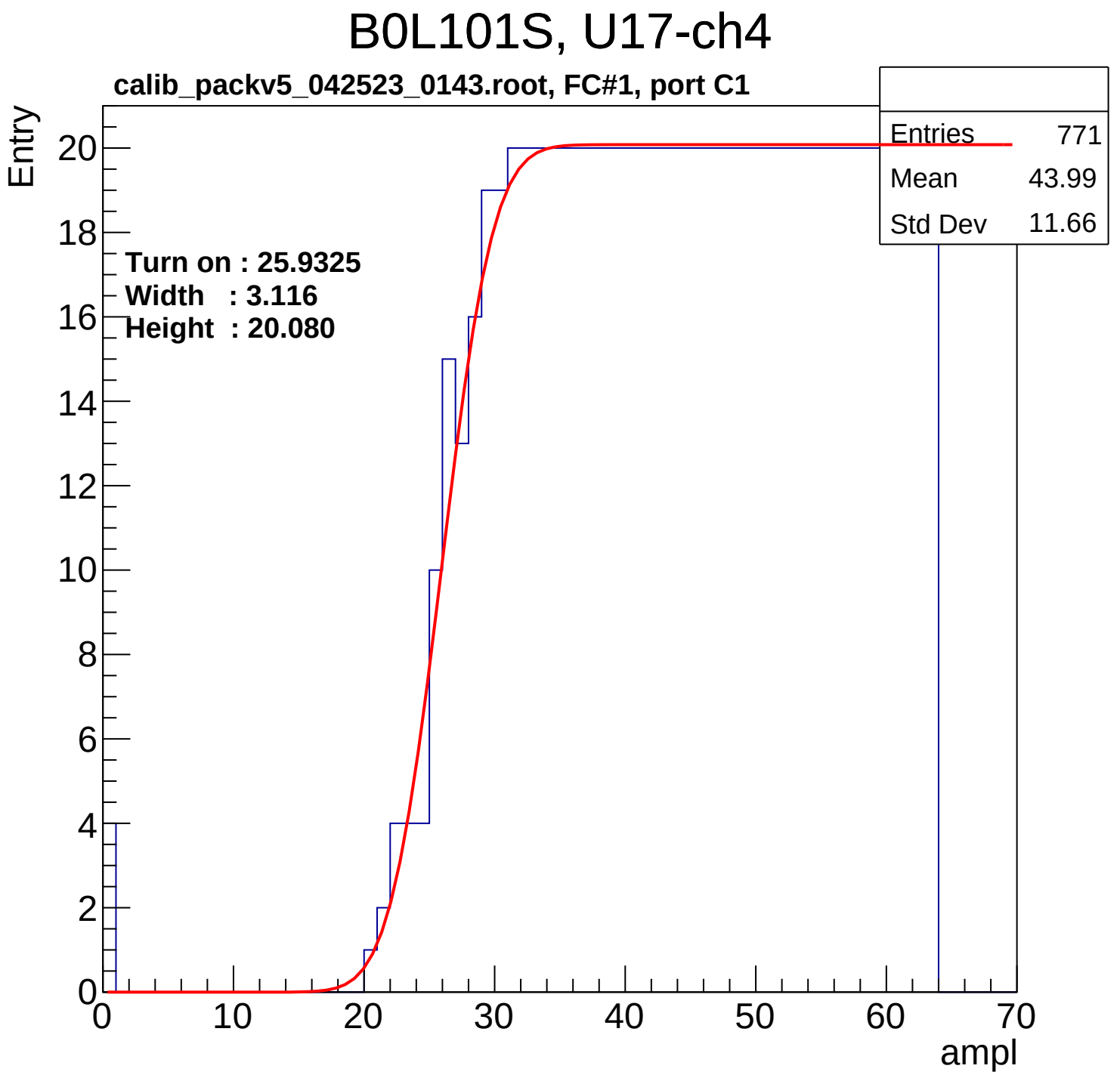
B0L101S, U17-ch4
calib_packv5_042523_0143.root, FC#1, port C1
Entries 771
Mean 43.99
Std Dev 11.66
Turn on : 25.9325
Width : 3.116
Height : 20.080
Entry
ampl
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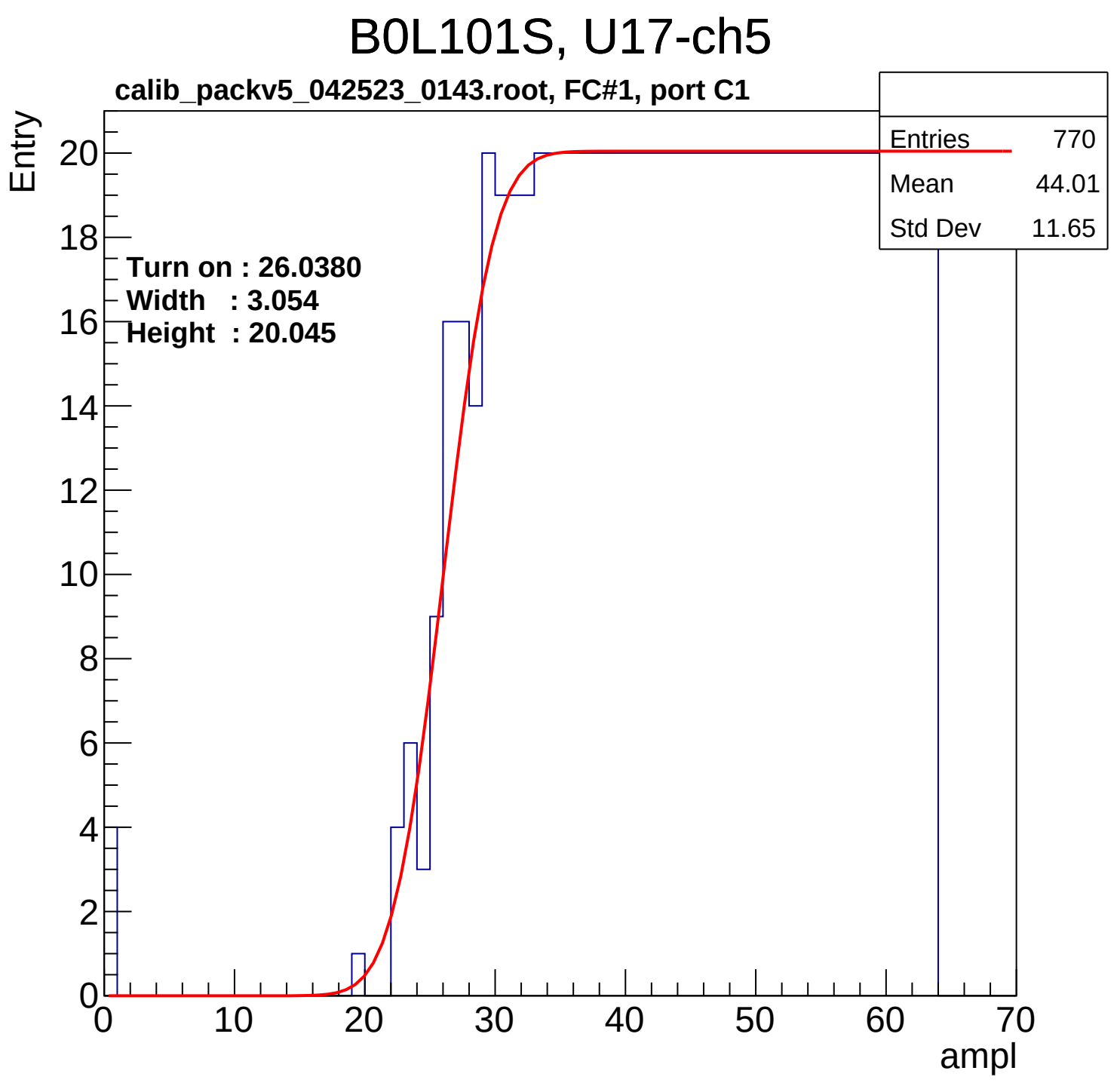
B0L101S, U17-ch5
calib_packv5_042523_0143.root, FC#1, port C1
Entries 770
Mean 44.01
Std Dev 11.65
Turn on : 26.0380
Width : 3.054
Height : 20.045
Entry
ampl
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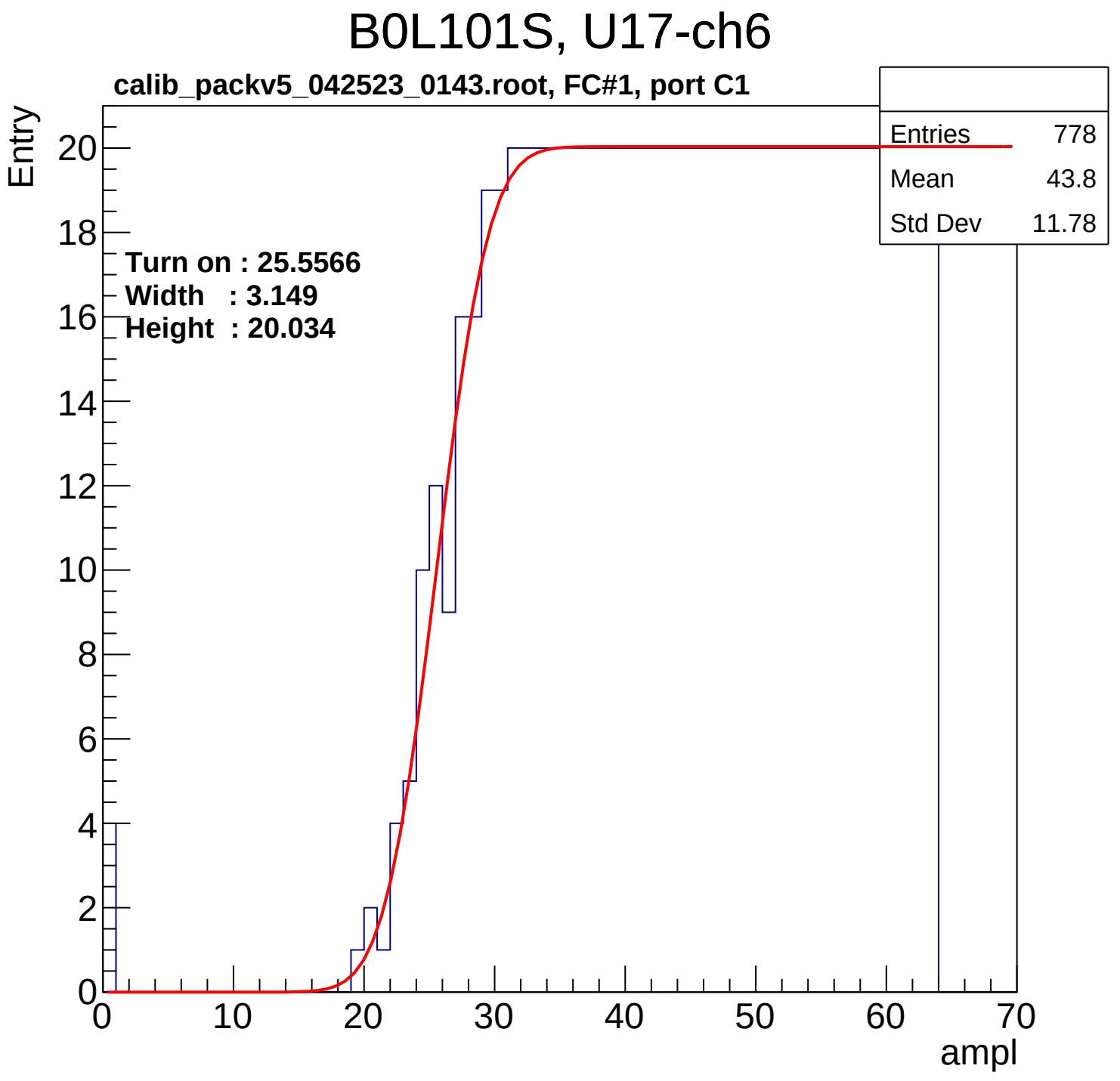
B0L101S, U17-ch6
calib_packv5_042523_0143.root, FC#1, port C1
Entries 778
Mean 43.8
Std Dev 11.78
Turn on : 25.5566
Width : 3.149
Height : 20.034
Entry
ampl
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6
8
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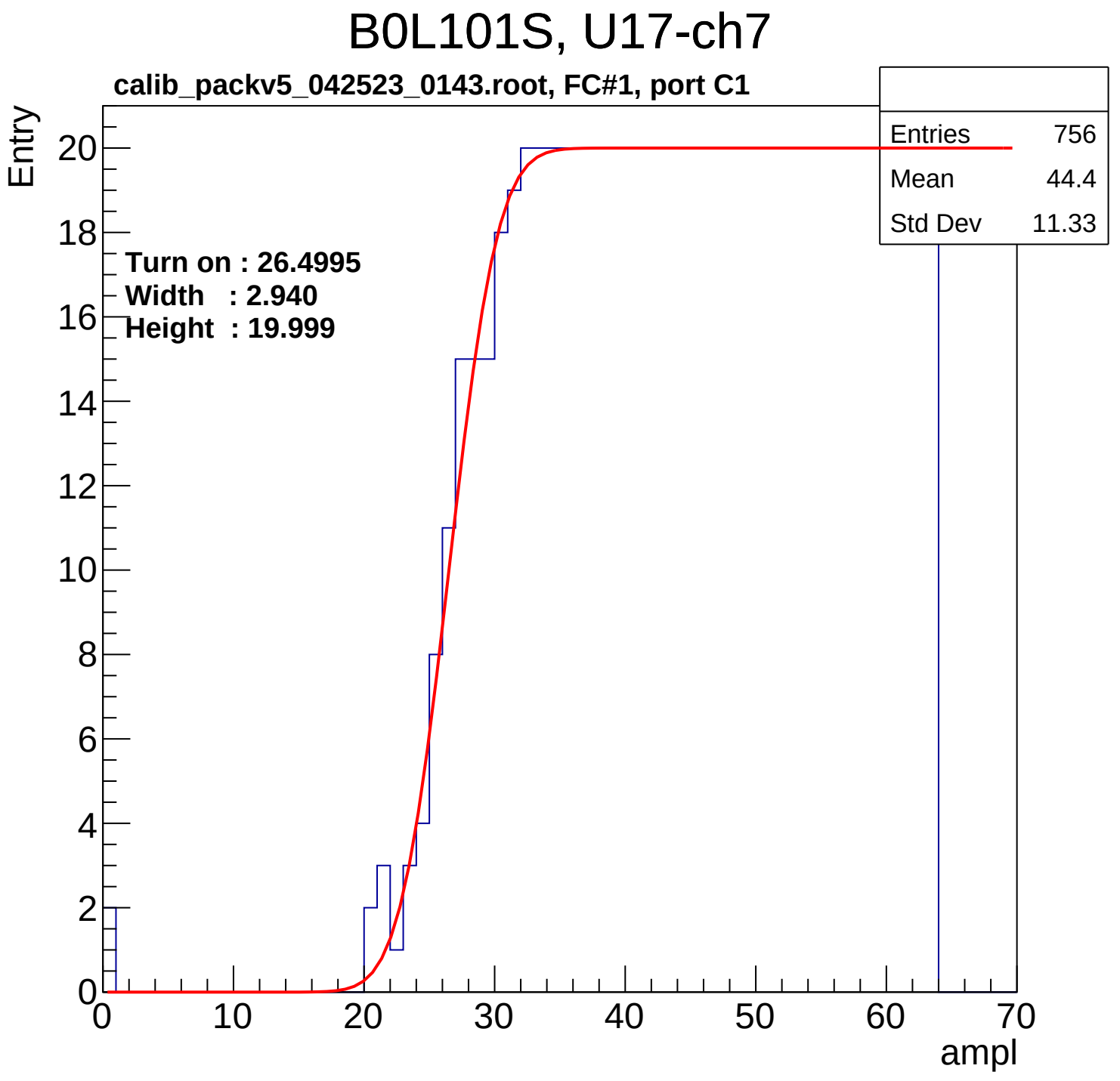
B0L101S, U17-ch7
calib_packv5_042523_0143.root, FC#1, port C1
Entries 756
Mean 44.4
Std Dev 11.33
Turn on : 26.4995
Width : 2.940
Height : 19.999
Entry
ampl
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6
8
10
12
14
16
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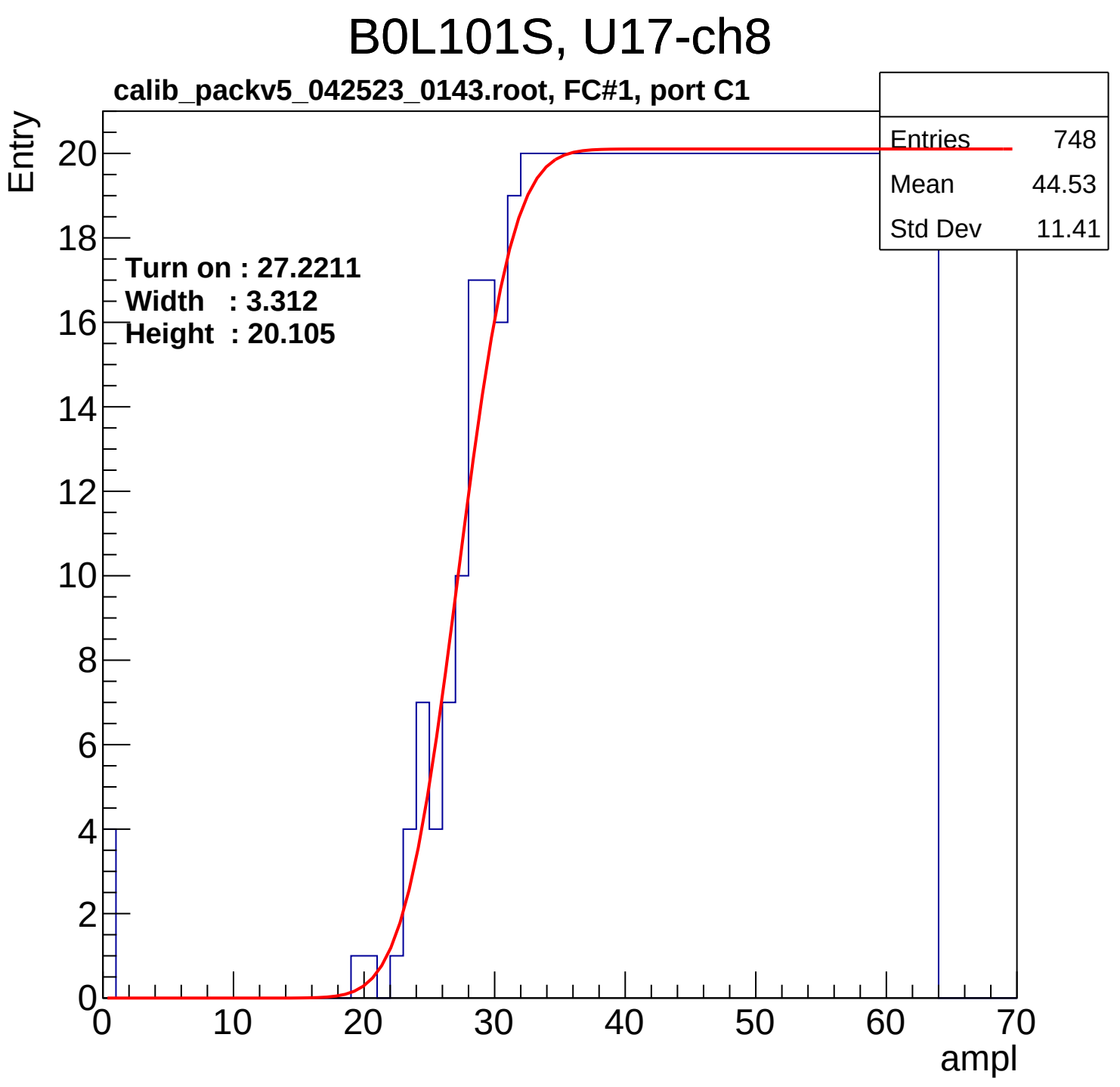
B0L101S, U17-ch8
calib_packv5_042523_0143.root, FC#1, port C1
Entries 748
Mean 44.53
Std Dev 11.41
Turn on : 27.2211
Width : 3.312
Height : 20.105
Entry
ampl
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6
8
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14
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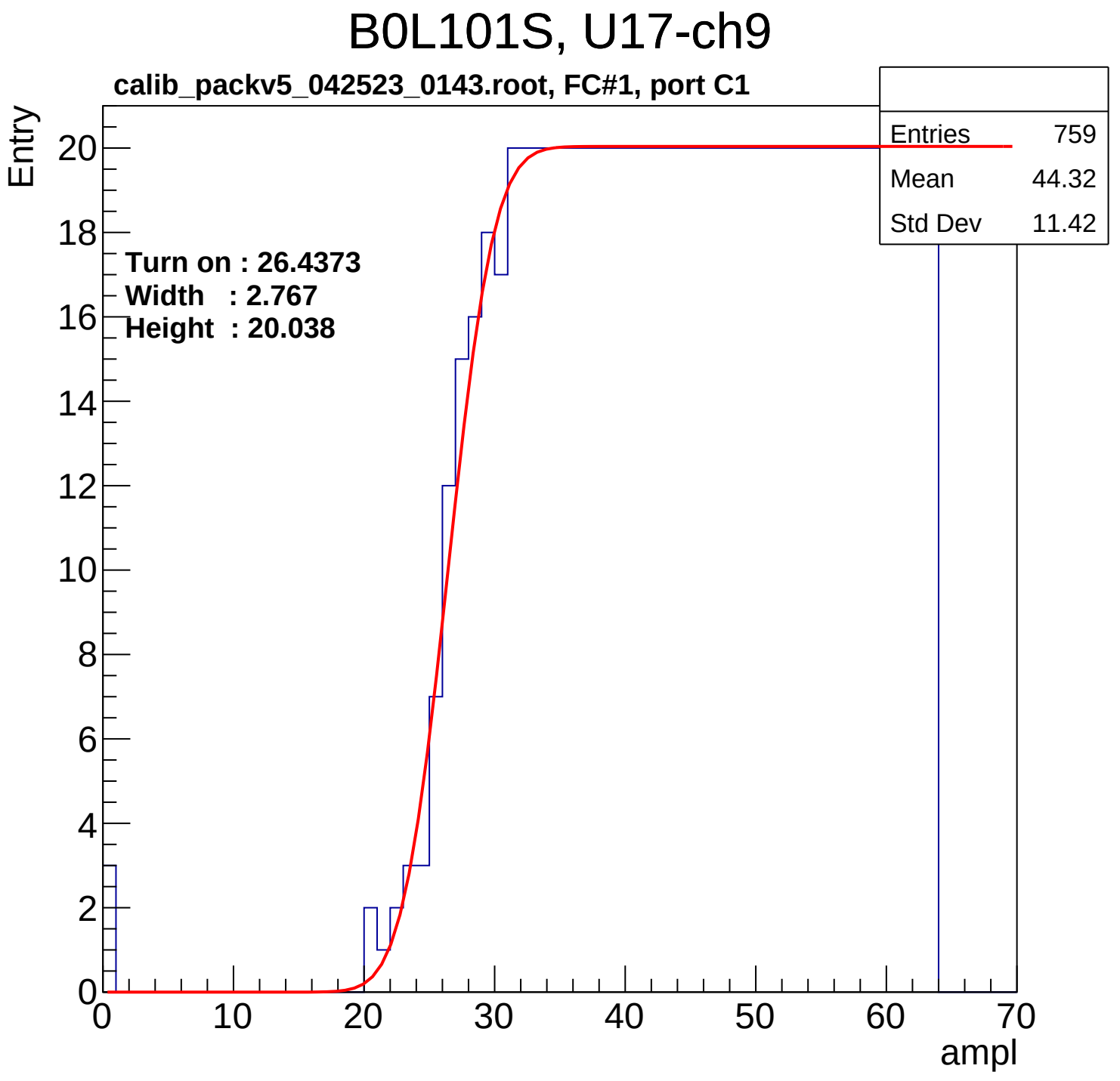
B0L101S, U17-ch9
calib_packv5_042523_0143.root, FC#1, port C1
Entries 759
Mean 44.32
Std Dev 11.42
Turn on : 26.4373
Width : 2.767
Height : 20.038
Entry
ampl
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6
8
10
12
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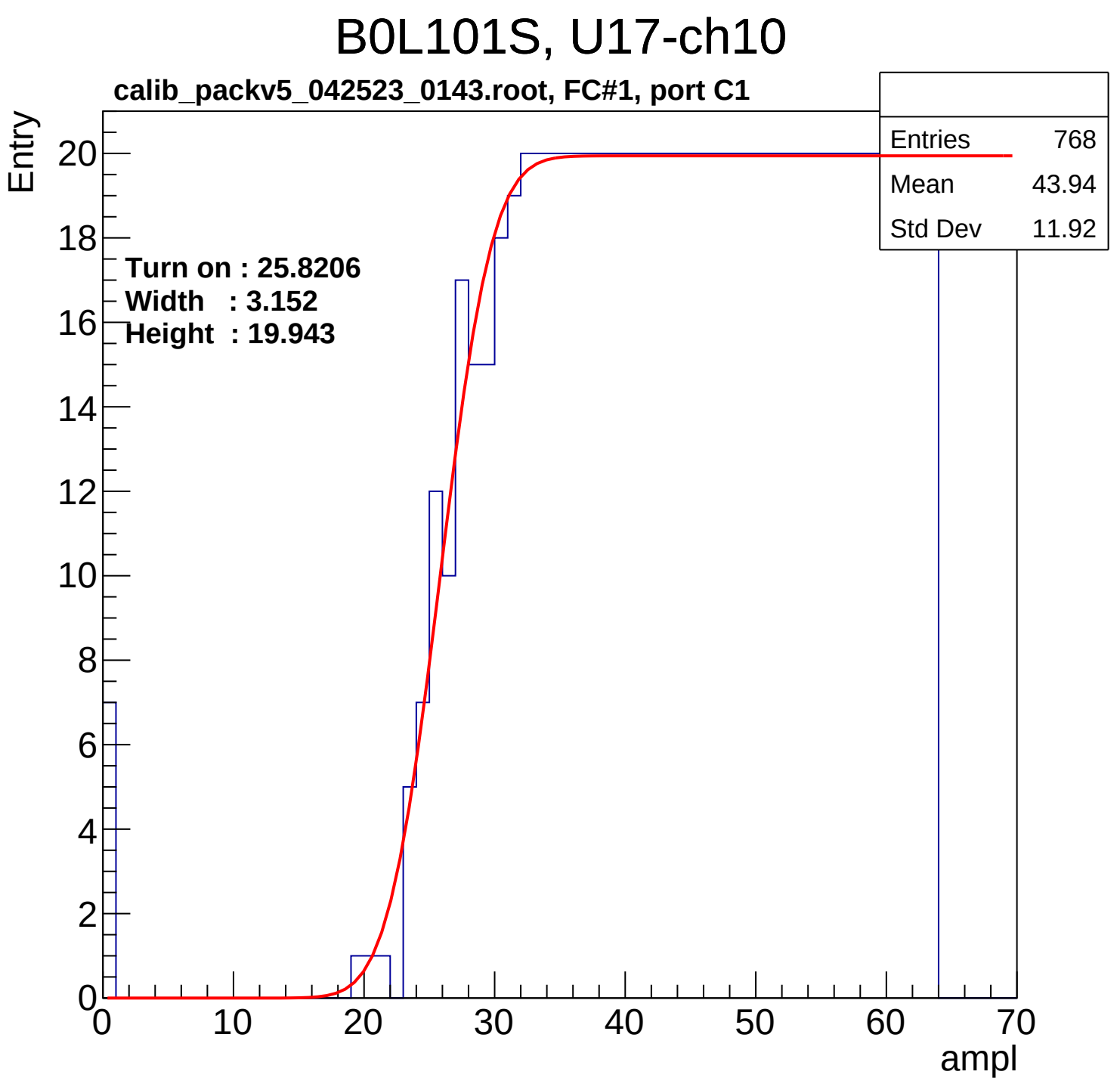
B0L101S, U17-ch10
calib_packv5_042523_0143.root, FC#1, port C1
Entries 768
Mean 43.94
Std Dev 11.92
Turn on : 25.8206
Width : 3.152
Height : 19.943
Entry
ampl
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6
8
10
12
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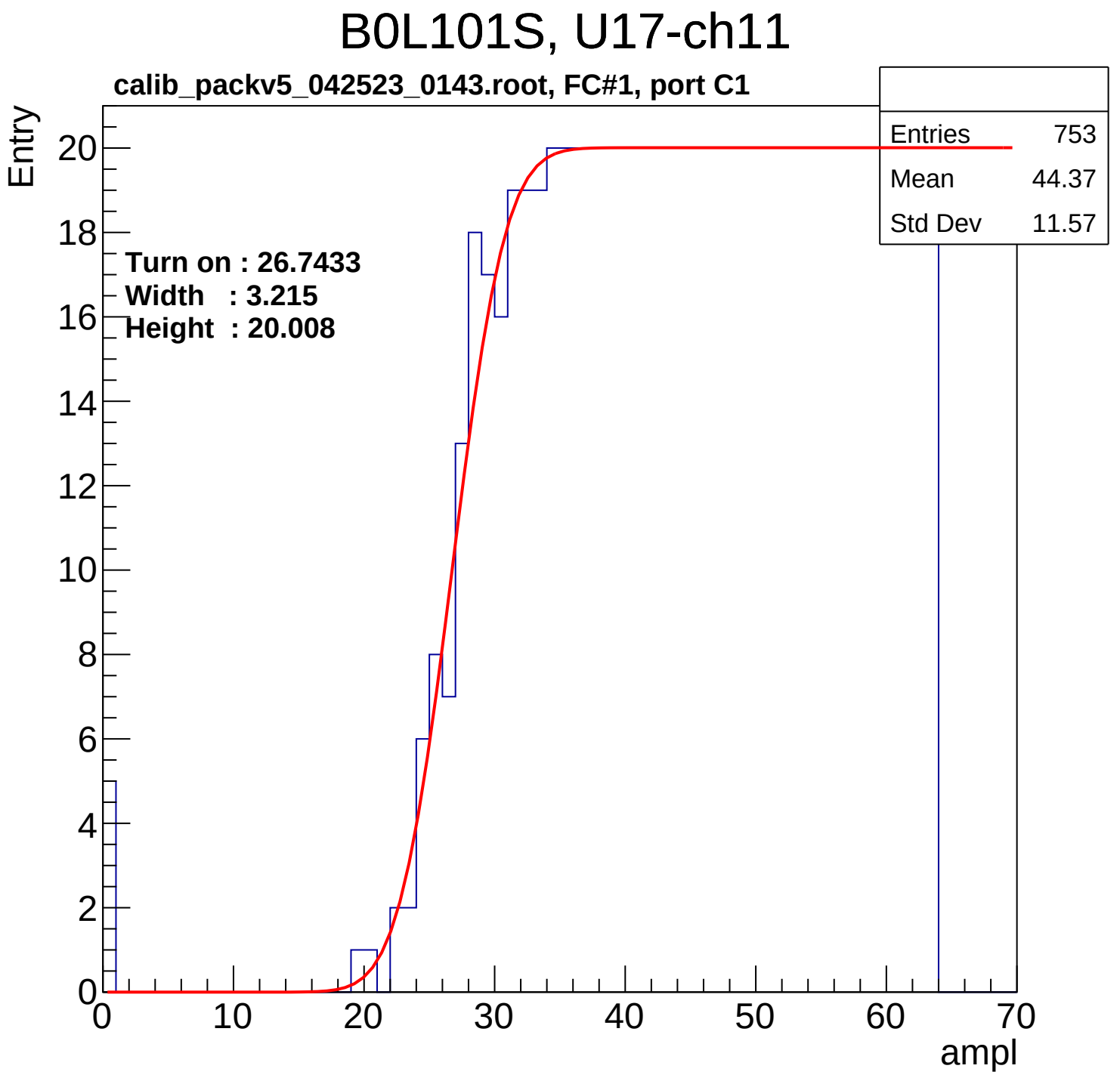
B0L101S, U17-ch11
calib_packv5_042523_0143.root, FC#1, port C1
Entries 753
Mean 44.37
Std Dev 11.57
Turn on : 26.7433
Width : 3.215
Height : 20.008
Entry
ampl
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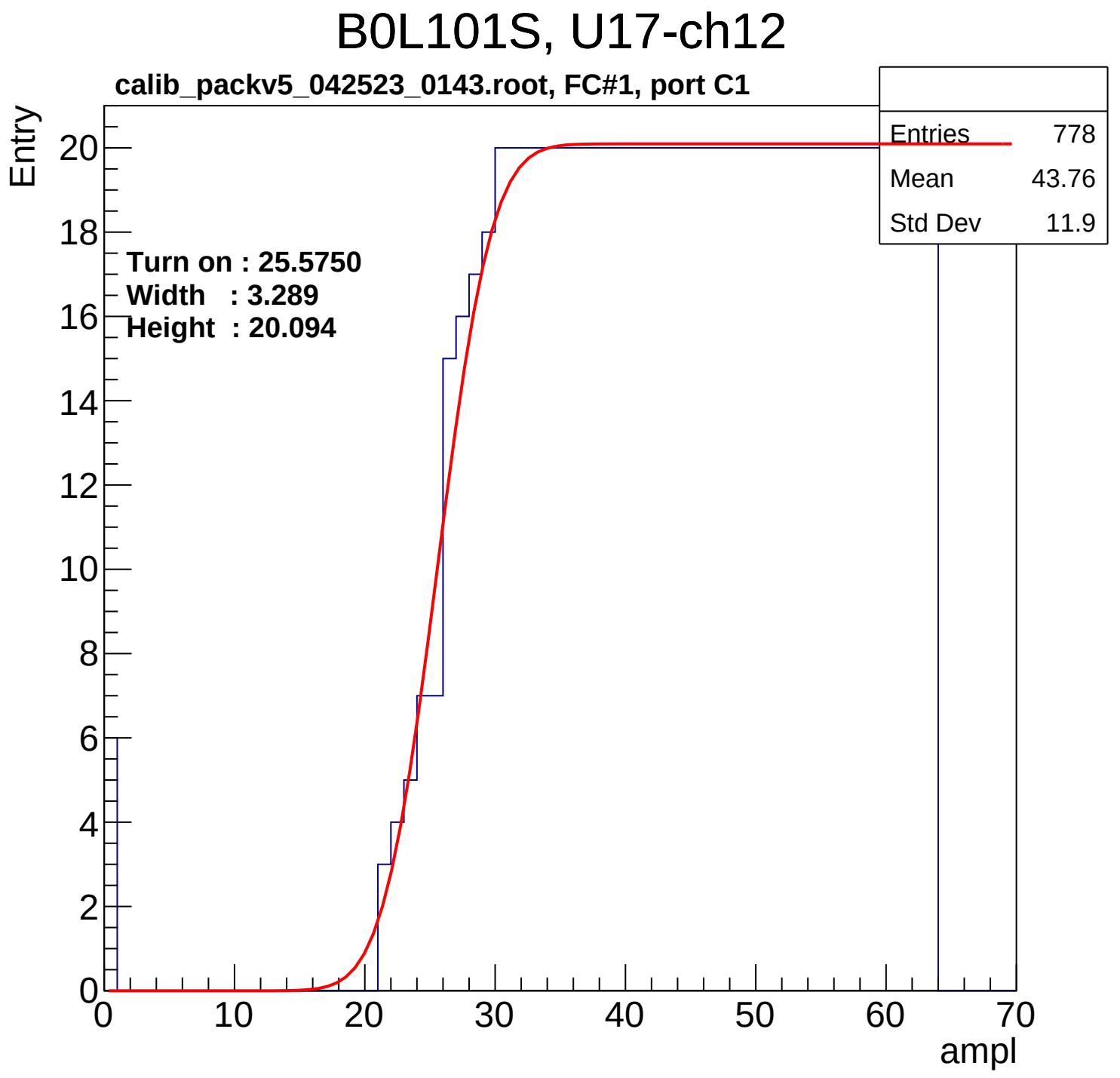
B0L101S, U17-ch12
calib_packv5_042523_0143.root, FC#1, port C1
Entries 778
Mean 43.76
Std Dev 11.9
Turn on : 25.5750
Width : 3.289
Height : 20.094
Entry
ampl
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6
8
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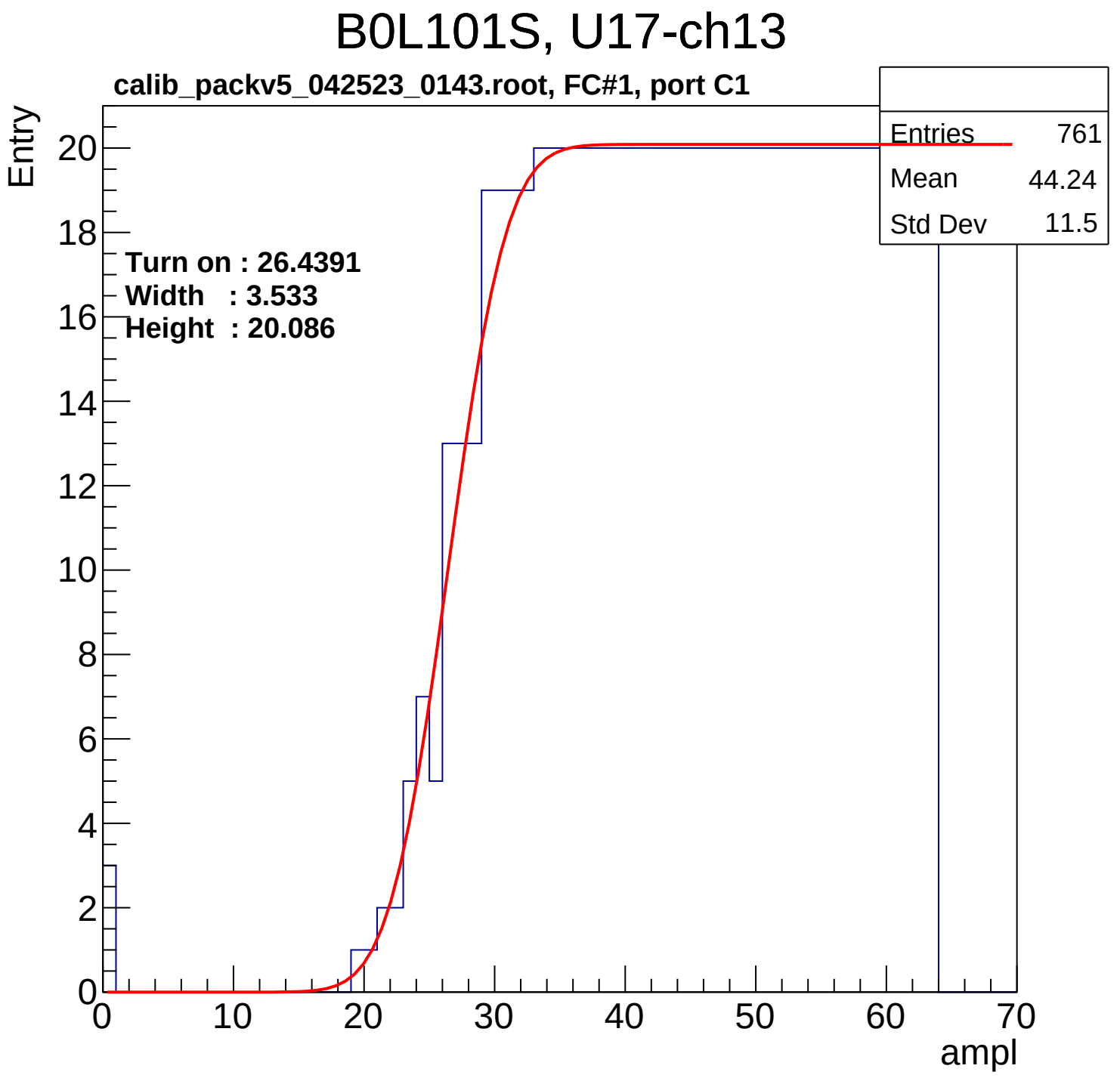
B0L101S, U17-ch13
calib_packv5_042523_0143.root, FC#1, port C1
Entries 761
Mean 44.24
Std Dev 11.5
Turn on : 26.4391
Width : 3.533
Height : 20.086
Entry
ampl
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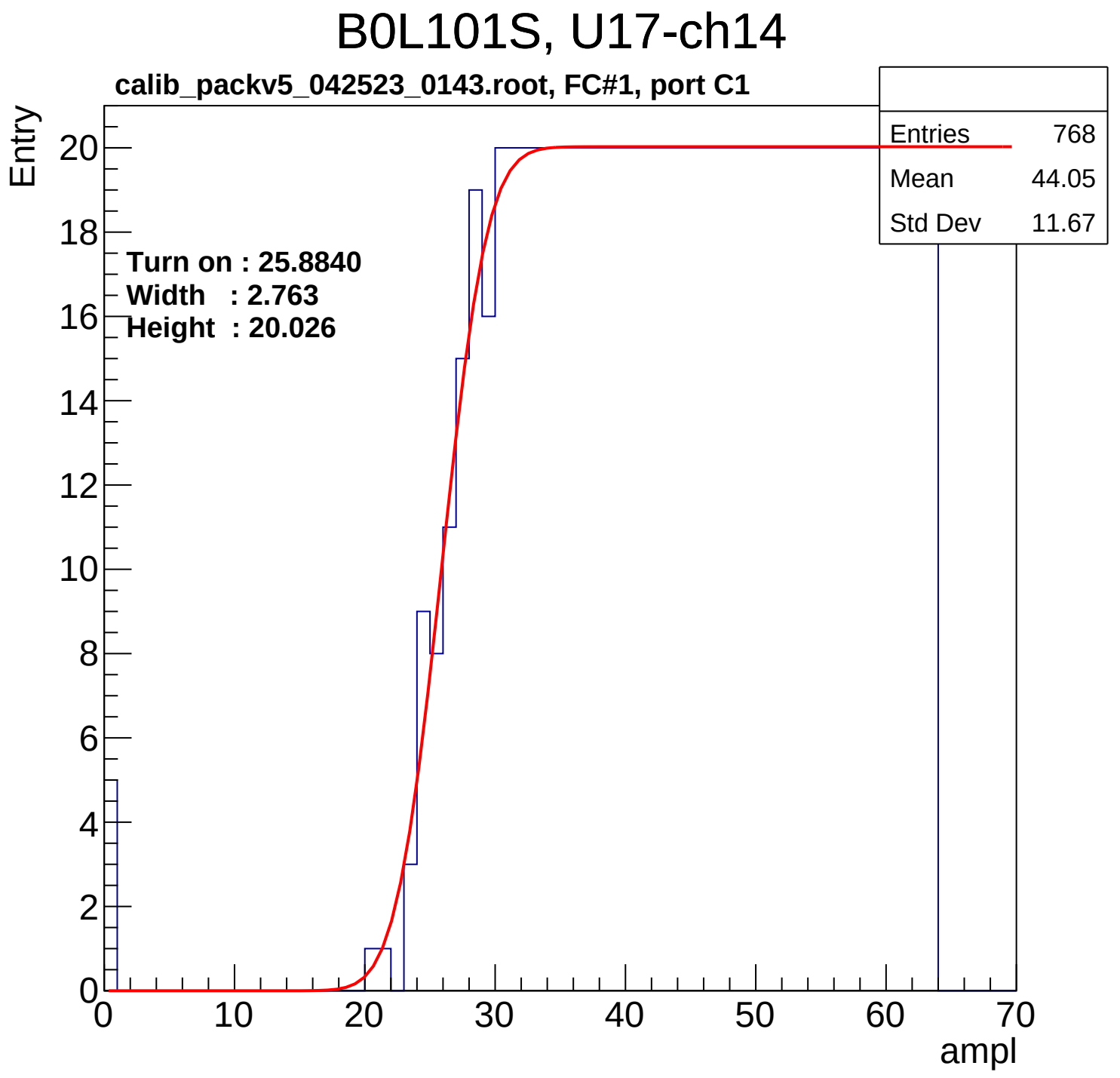
B0L101S, U17-ch14
calib_packv5_042523_0143.root, FC#1, port C1
Entries 768
Mean 44.05
Std Dev 11.67
Turn on : 25.8840
Width : 2.763
Height : 20.026
Entry
ampl
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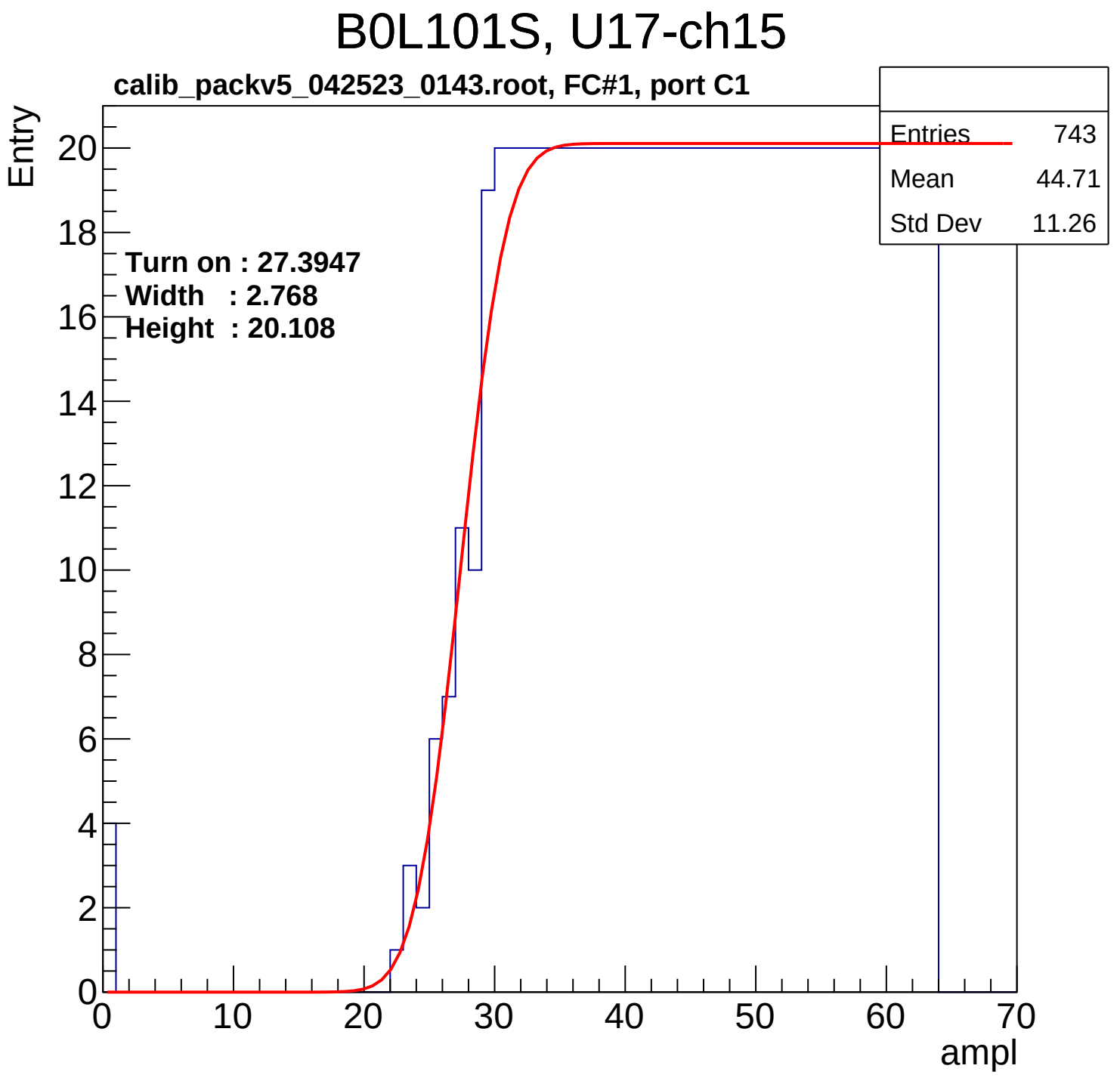
B0L101S, U17-ch15
calib_packv5_042523_0143.root, FC#1, port C1
Entries 743
Mean 44.71
Std Dev 11.26
Turn on : 27.3947
Width : 2.768
Height : 20.108
Entry
ampl
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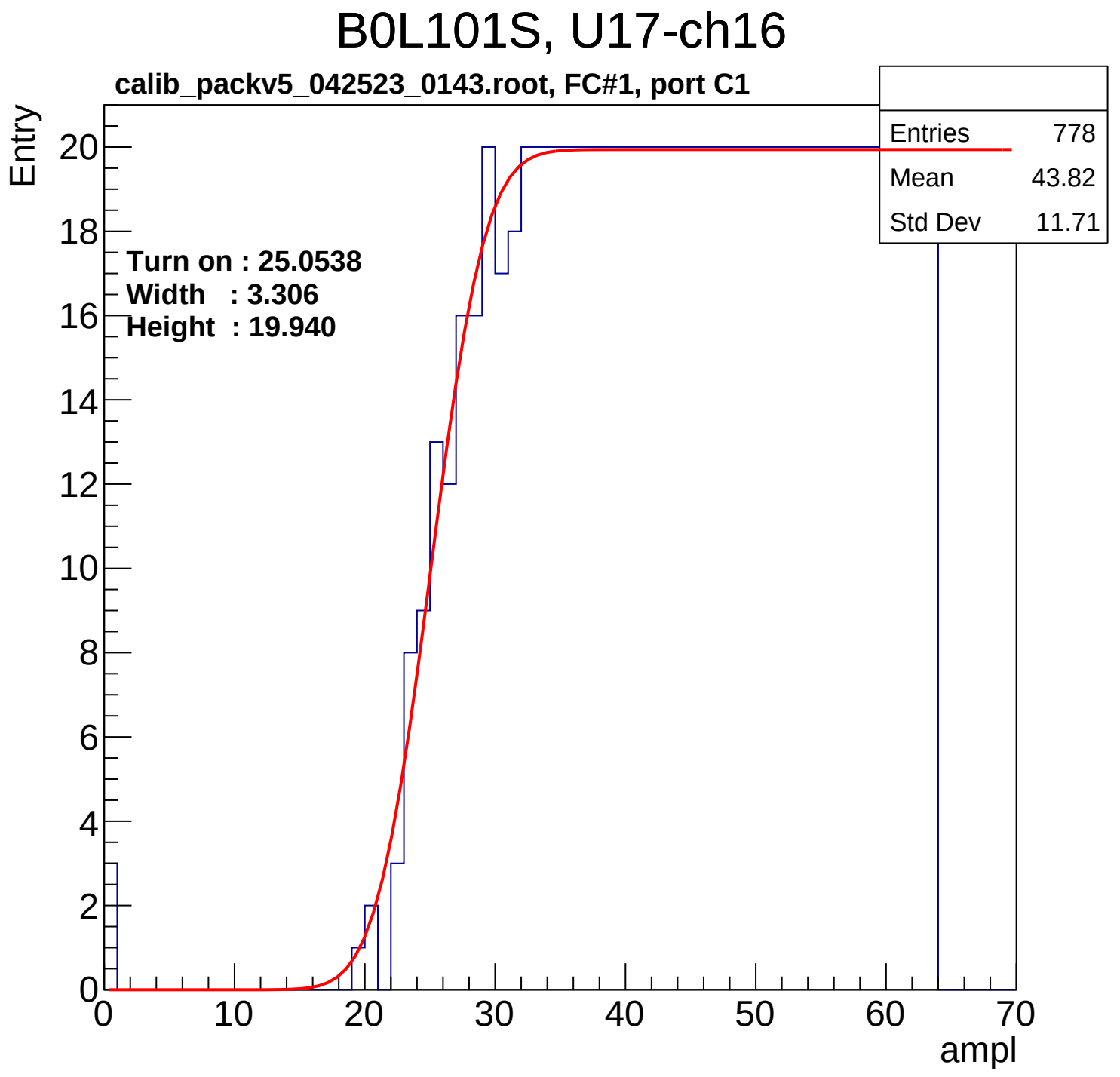
B0L101S, U17-ch16
calib_packv5_042523_0143.root, FC#1, port C1
Entries 778
Mean 43.82
Std Dev 11.71
Turn on : 25.0538
Width : 3.306
Height : 19.940
Entry
ampl
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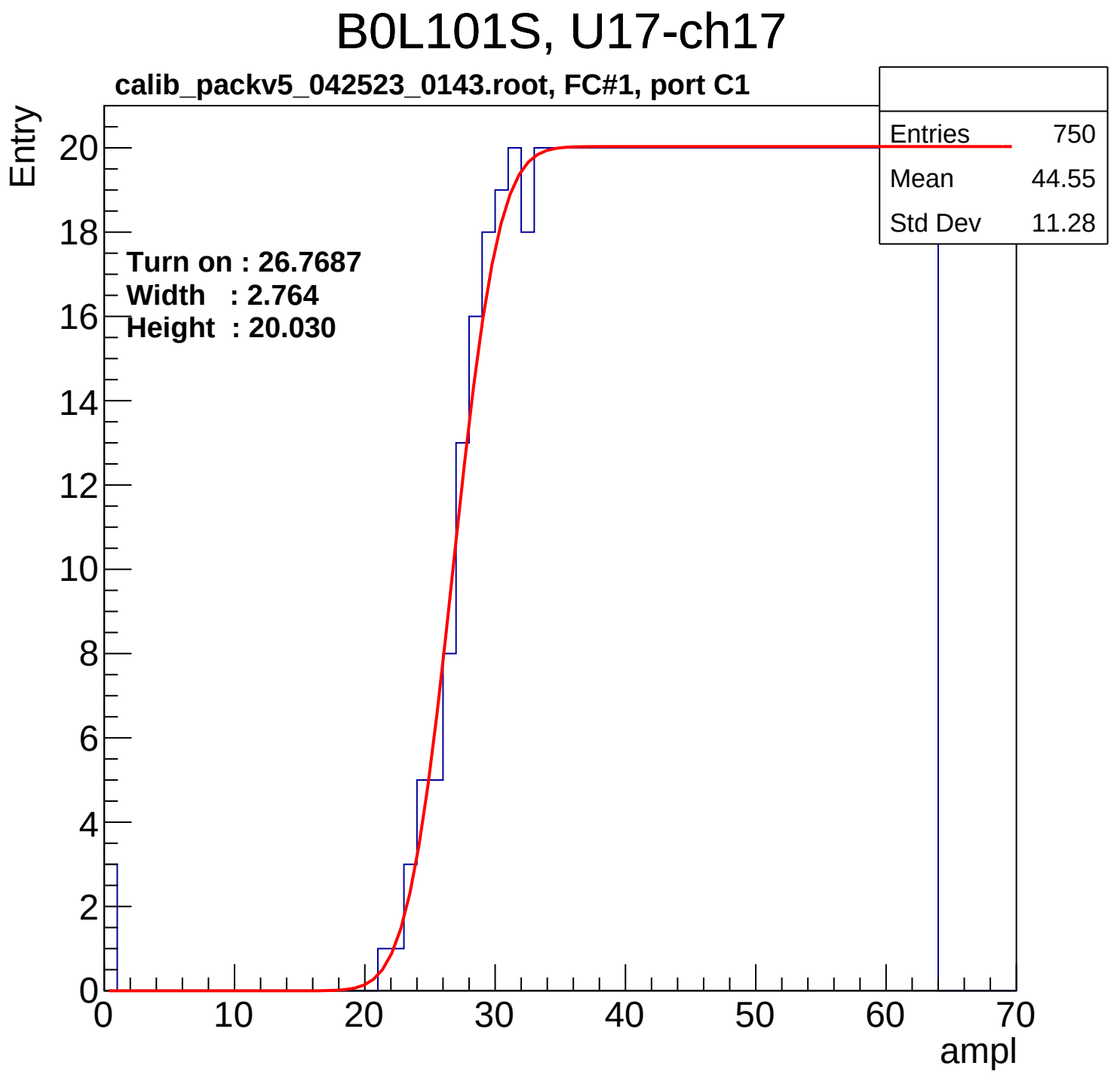
B0L101S, U17-ch17
calib_packv5_042523_0143.root, FC#1, port C1
Entries 750
Mean 44.55
Std Dev 11.28
Turn on : 26.7687
Width : 2.764
Height : 20.030
Entry
ampl
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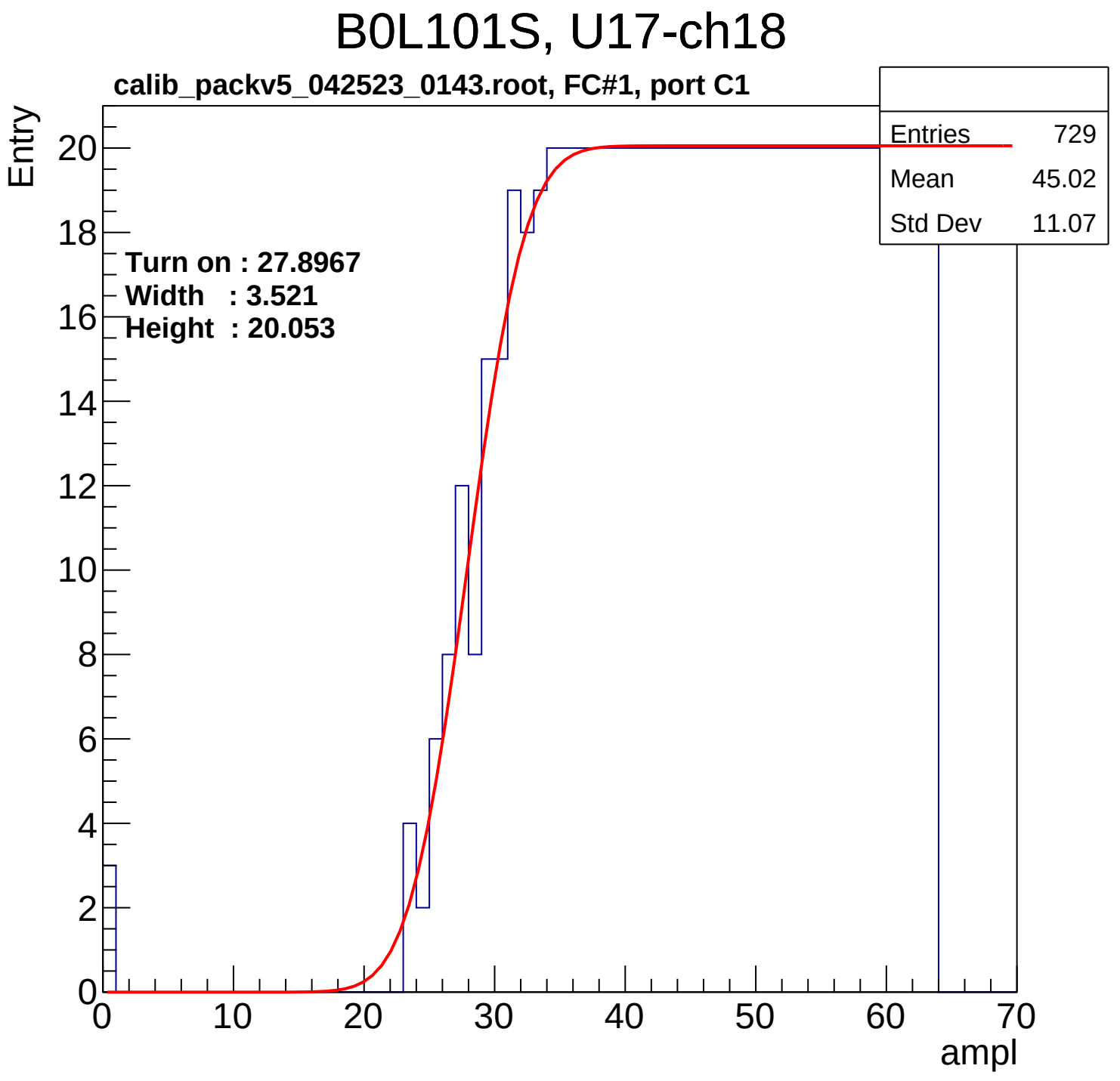
B0L101S, U17-ch18
calib_packv5_042523_0143.root, FC#1, port C1
Entries 729
Mean 45.02
Std Dev 11.07
Turn on : 27.8967
Width : 3.521
Height : 20.053
Entry
ampl
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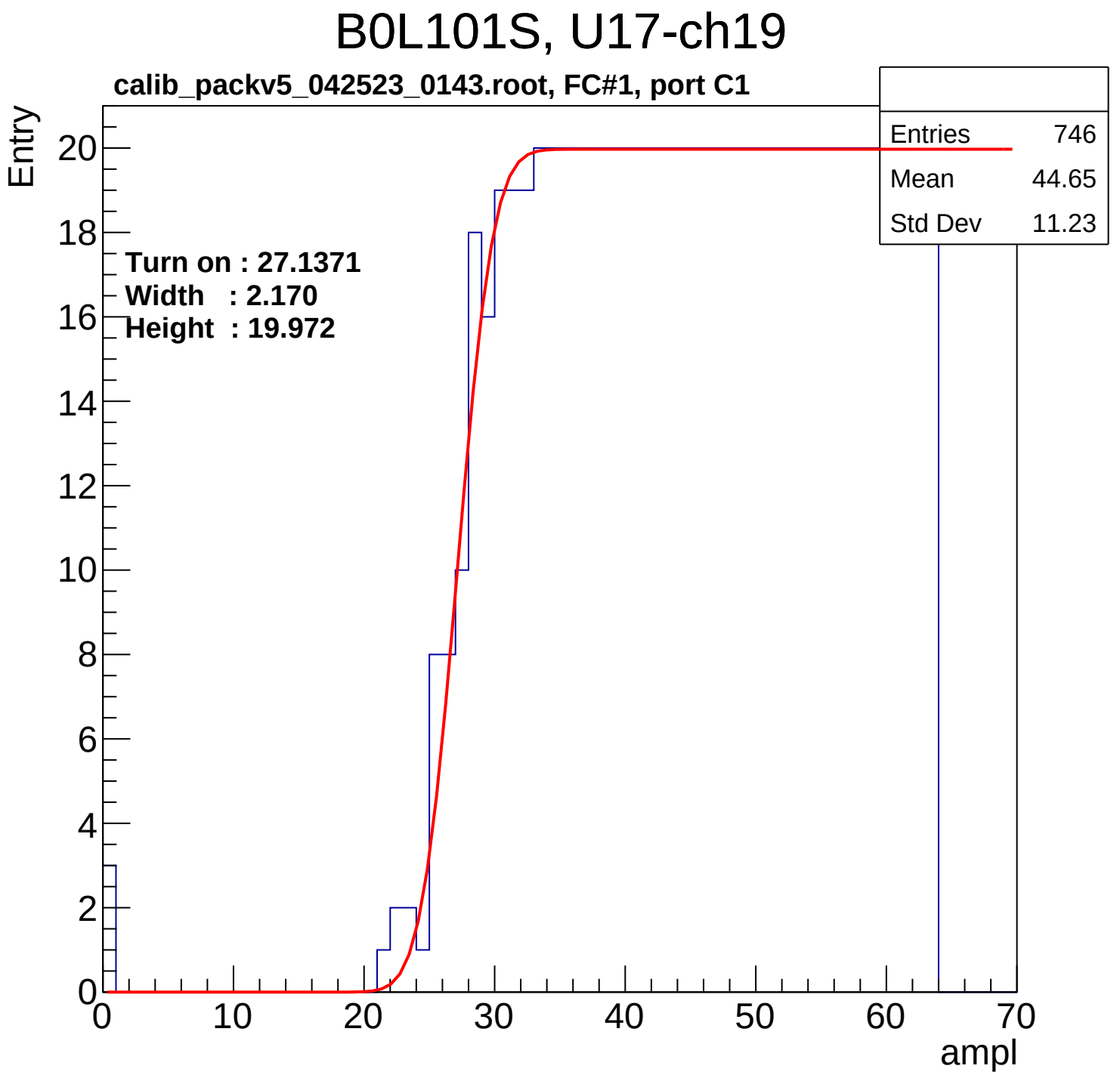
B0L101S, U17-ch19
calib_packv5_042523_0143.root, FC#1, port C1
Entries 746
Mean 44.65
Std Dev 11.23
Turn on : 27.1371
Width : 2.170
Height : 19.972
Entry
ampl
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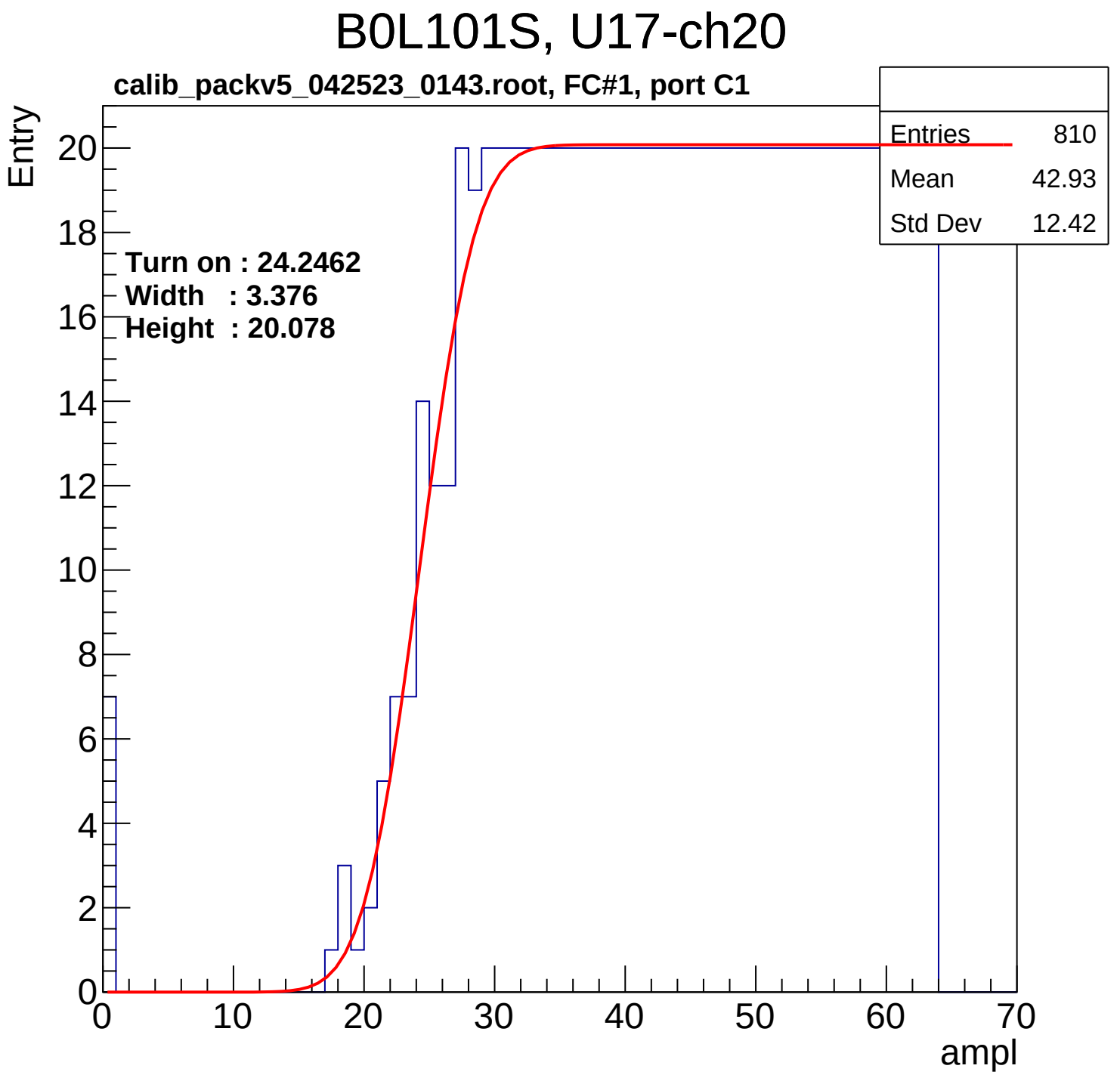
B0L101S, U17-ch20
calib_packv5_042523_0143.root, FC#1, port C1
Entries 810
Mean 42.93
Std Dev 12.42
Turn on : 24.2462
Width : 3.376
Height : 20.078
Entry
ampl
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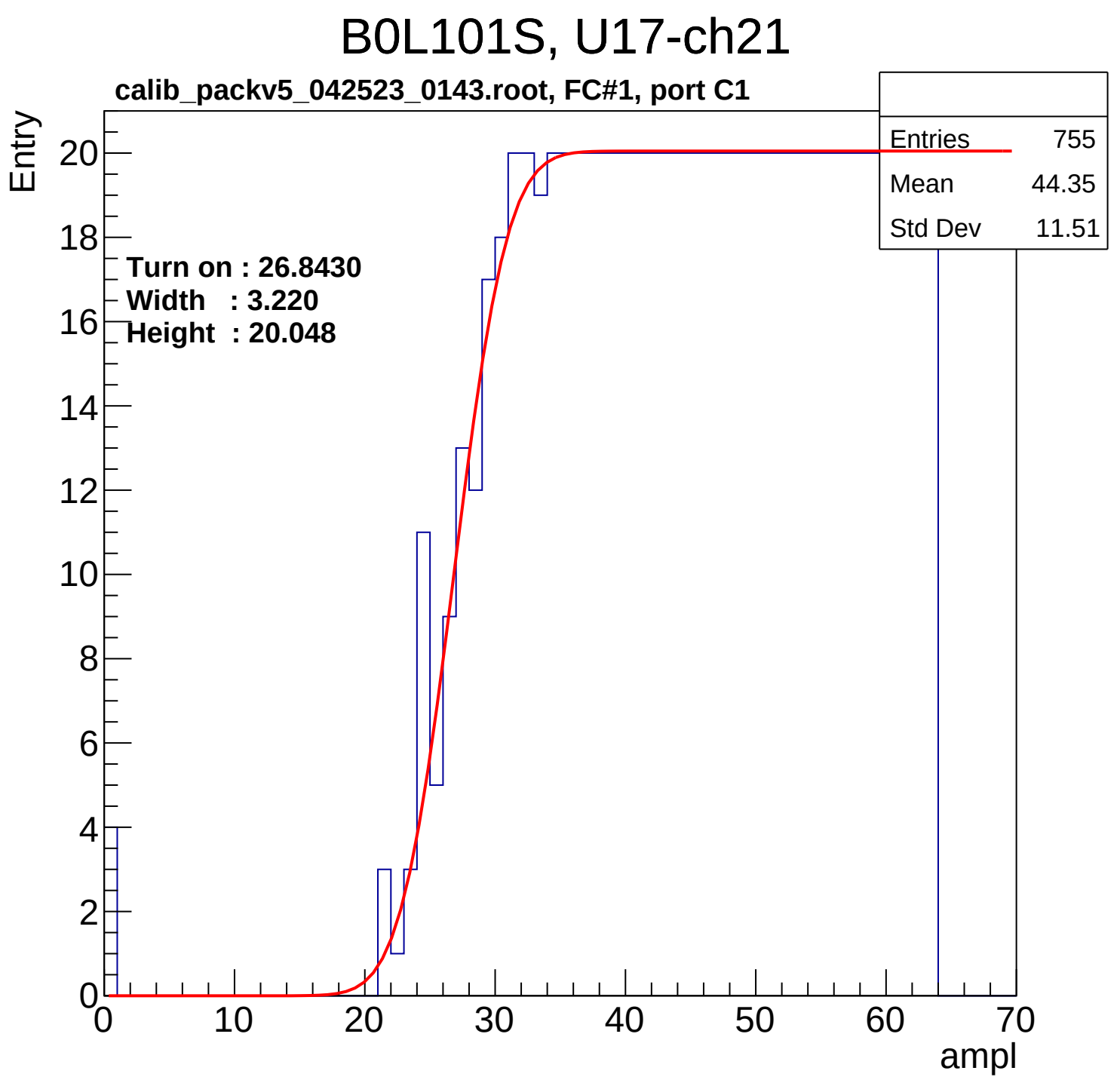
B0L101S, U17-ch21
calib_packv5_042523_0143.root, FC#1, port C1
Entries 755
Mean 44.35
Std Dev 11.51
Turn on : 26.8430
Width : 3.220
Height : 20.048
Entry
ampl
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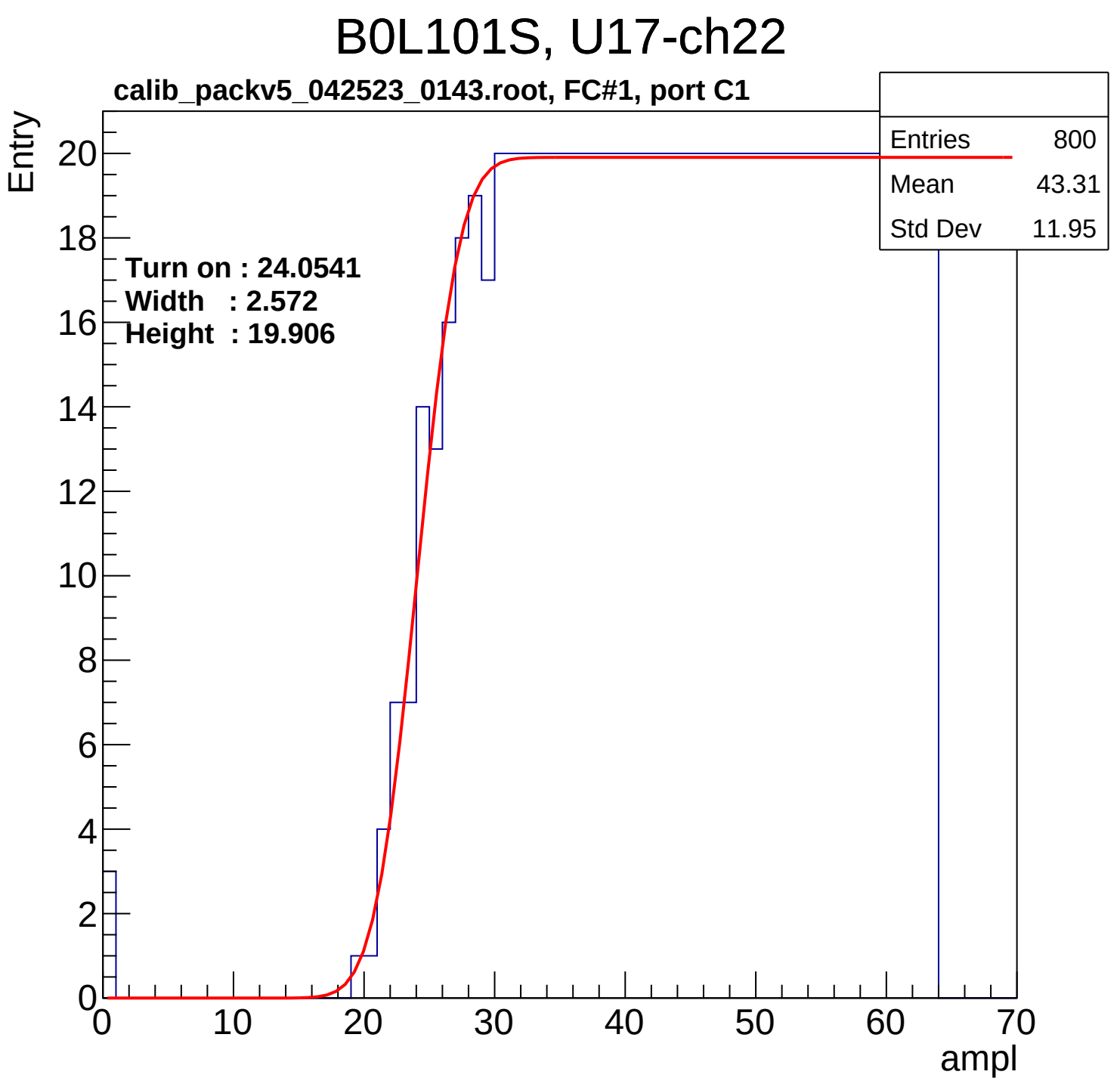
B0L101S, U17-ch22
calib_packv5_042523_0143.root, FC#1, port C1
Entries 800
Mean 43.31
Std Dev 11.95
Turn on : 24.0541
Width : 2.572
Height : 19.906
Entry
ampl
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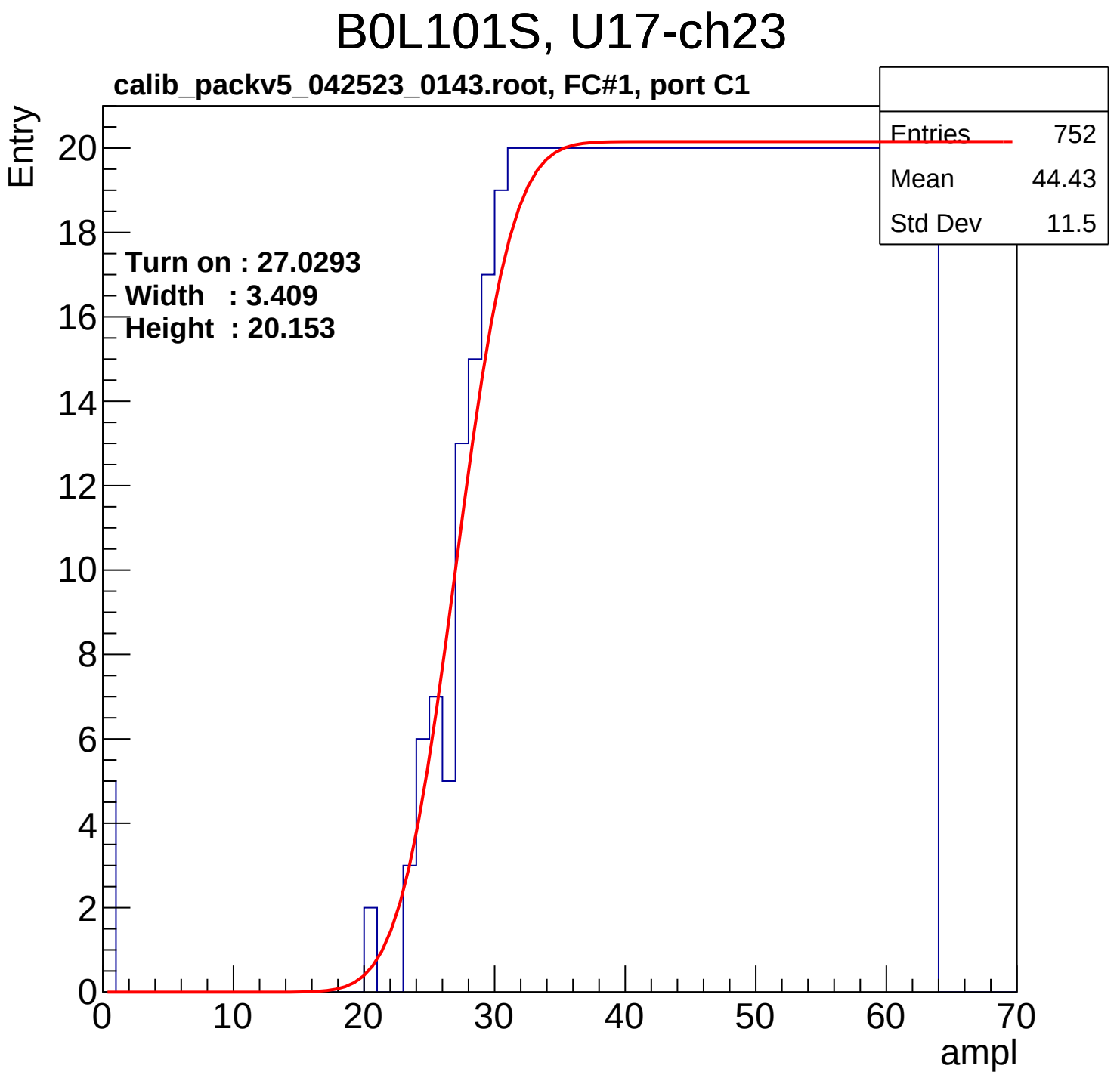
B0L101S, U17-ch23
calib_packv5_042523_0143.root, FC#1, port C1
Entries 752
Mean 44.43
Std Dev 11.5
Turn on : 27.0293
Width : 3.409
Height : 20.153
Entry
ampl
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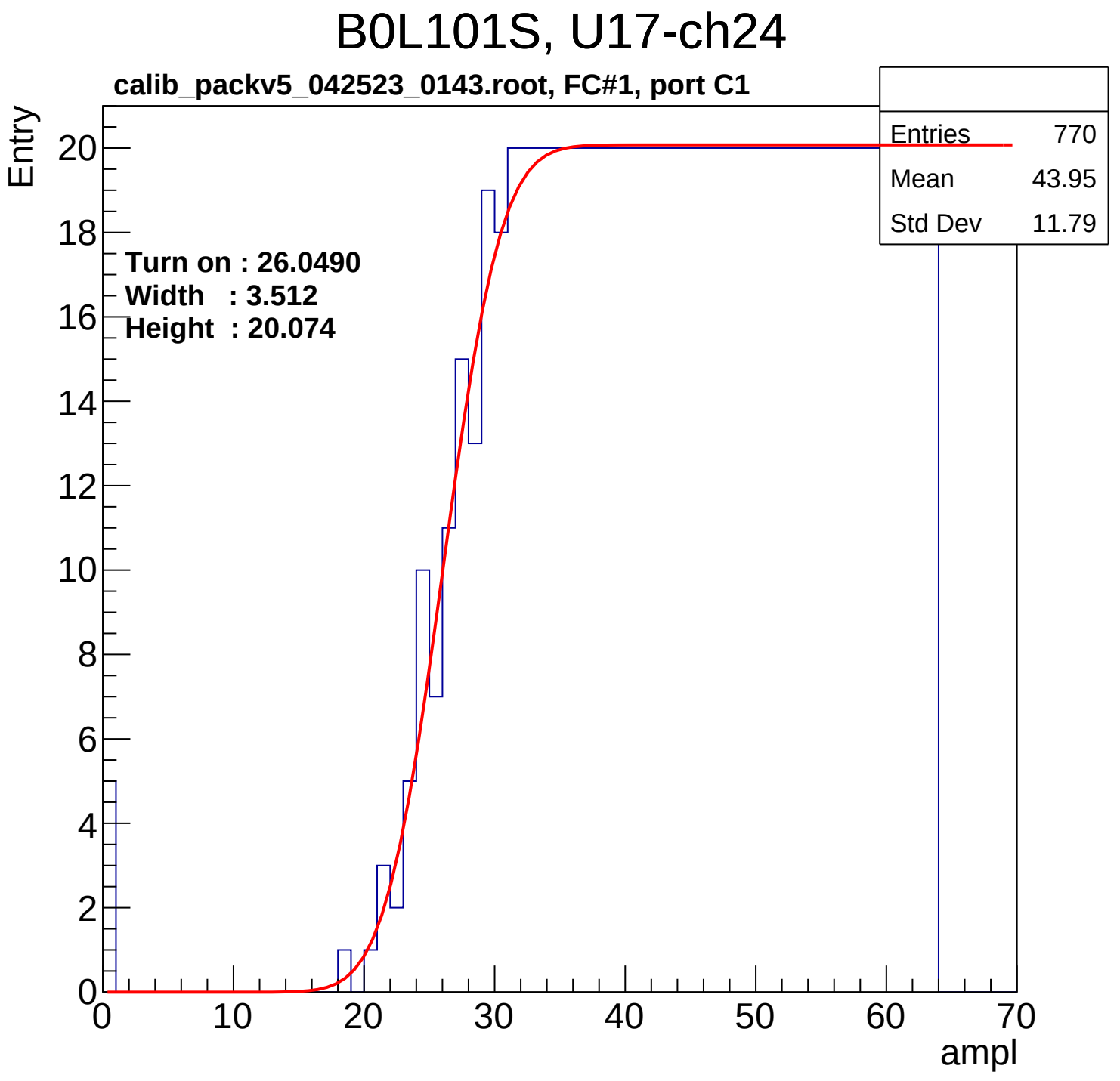
B0L101S, U17-ch24
calib_packv5_042523_0143.root, FC#1, port C1
Entries 770
Mean 43.95
Std Dev 11.79
Turn on : 26.0490
Width : 3.512
Height : 20.074
Entry
ampl
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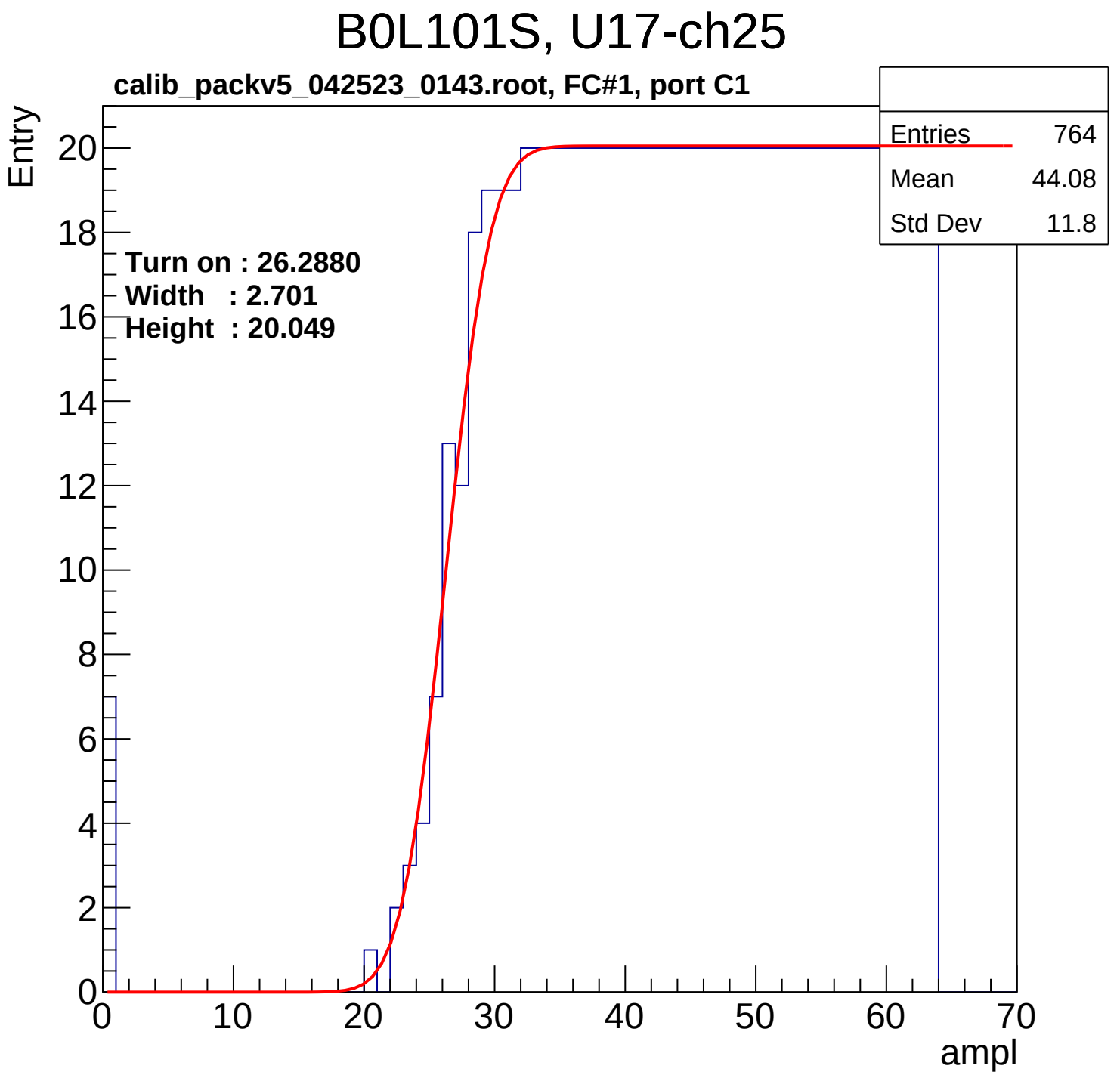
B0L101S, U17-ch25
calib_packv5_042523_0143.root, FC#1, port C1
Entries 764
Mean 44.08
Std Dev 11.8
Turn on : 26.2880
Width : 2.701
Height : 20.049
Entry
ampl
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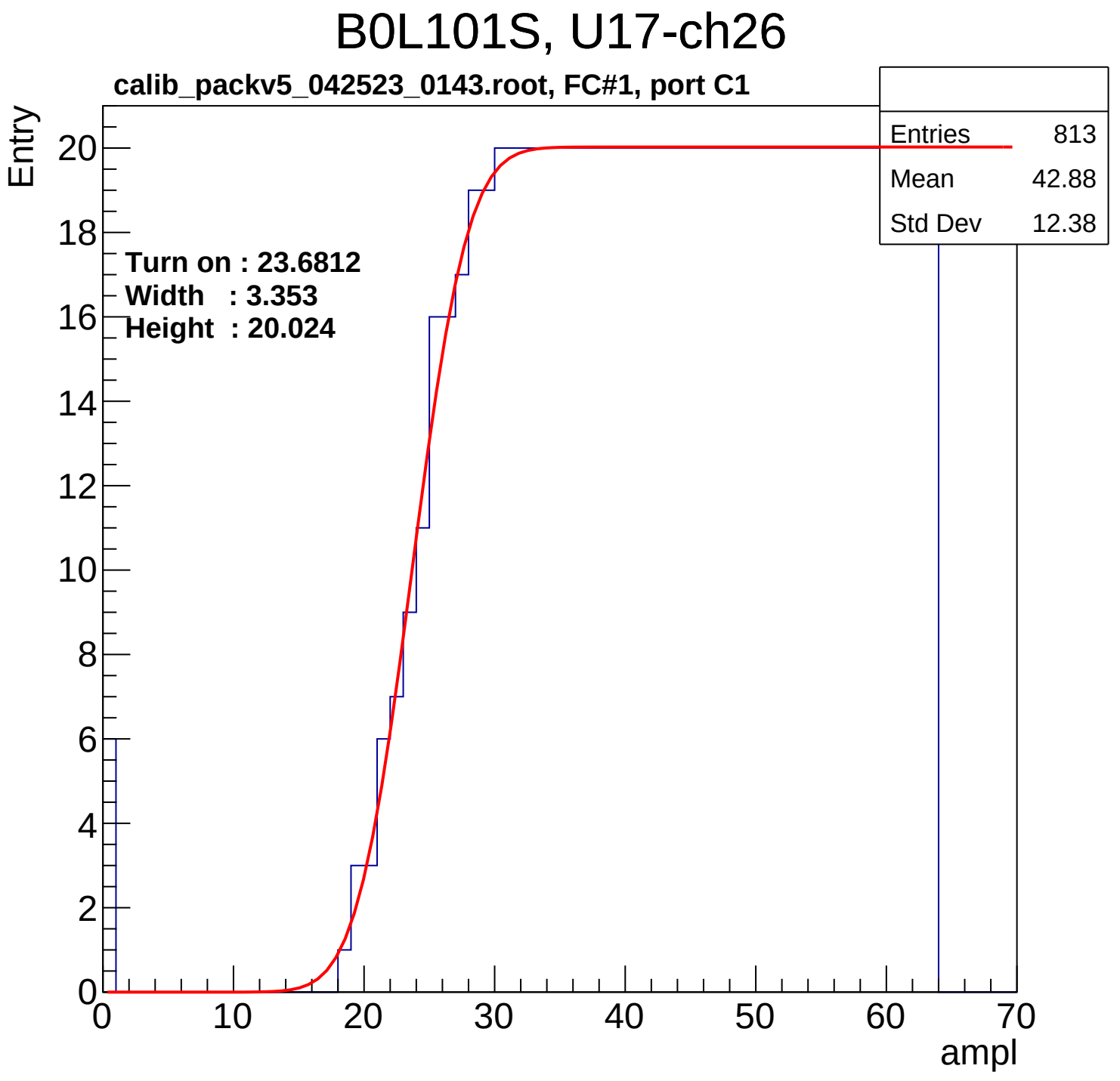
B0L101S, U17-ch26
calib_packv5_042523_0143.root, FC#1, port C1
Entries 813
Mean 42.88
Std Dev 12.38
Turn on : 23.6812
Width : 3.353
Height : 20.024
Entry
ampl
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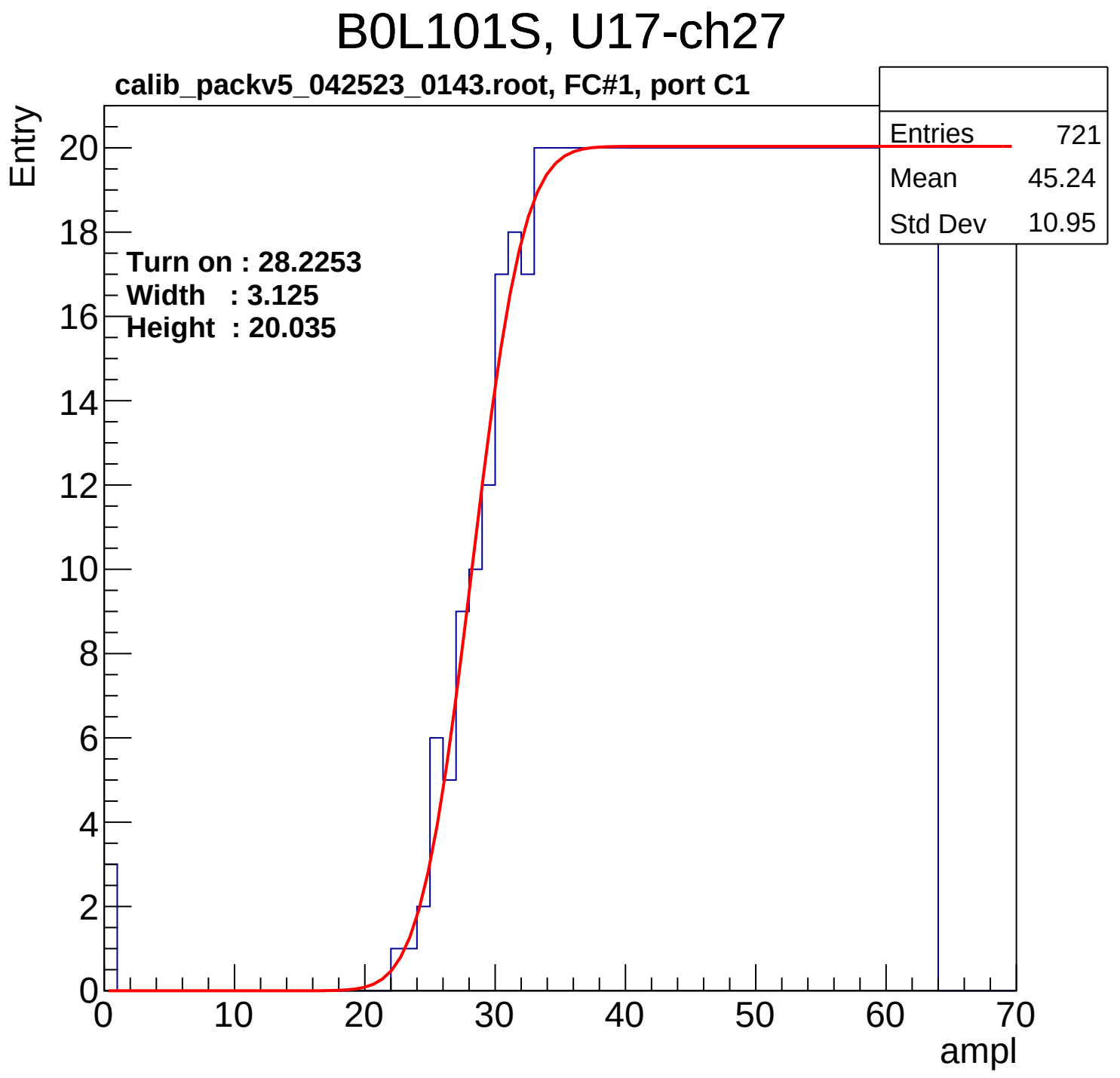
B0L101S, U17-ch27
calib_packv5_042523_0143.root, FC#1, port C1
Entries 721
Mean 45.24
Std Dev 10.95
Turn on : 28.2253
Width : 3.125
Height : 20.035
Entry
ampl
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6
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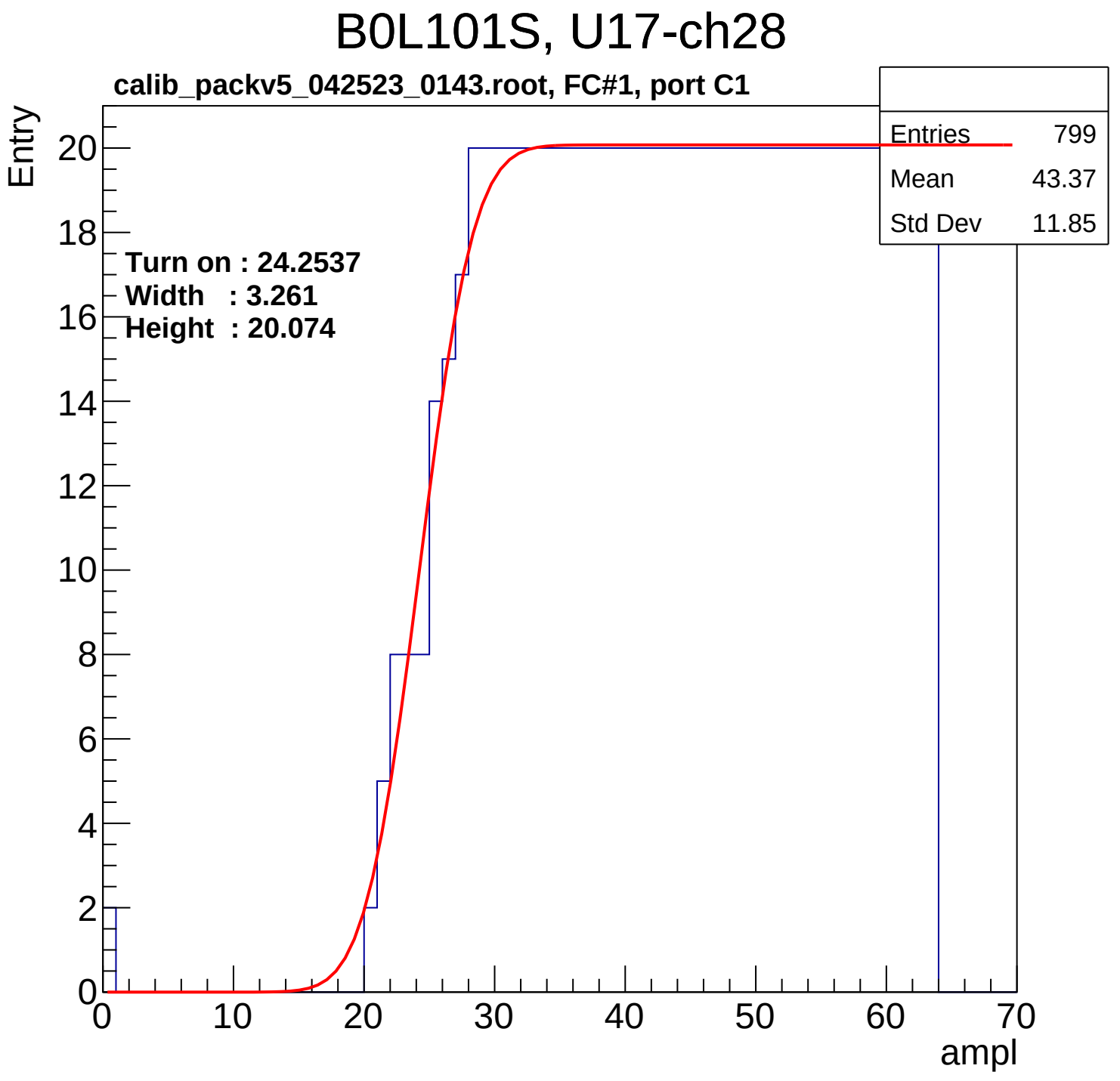
B0L101S, U17-ch28
calib_packv5_042523_0143.root, FC#1, port C1
Entries 799
Mean 43.37
Std Dev 11.85
Turn on : 24.2537
Width : 3.261
Height : 20.074
Entry
ampl
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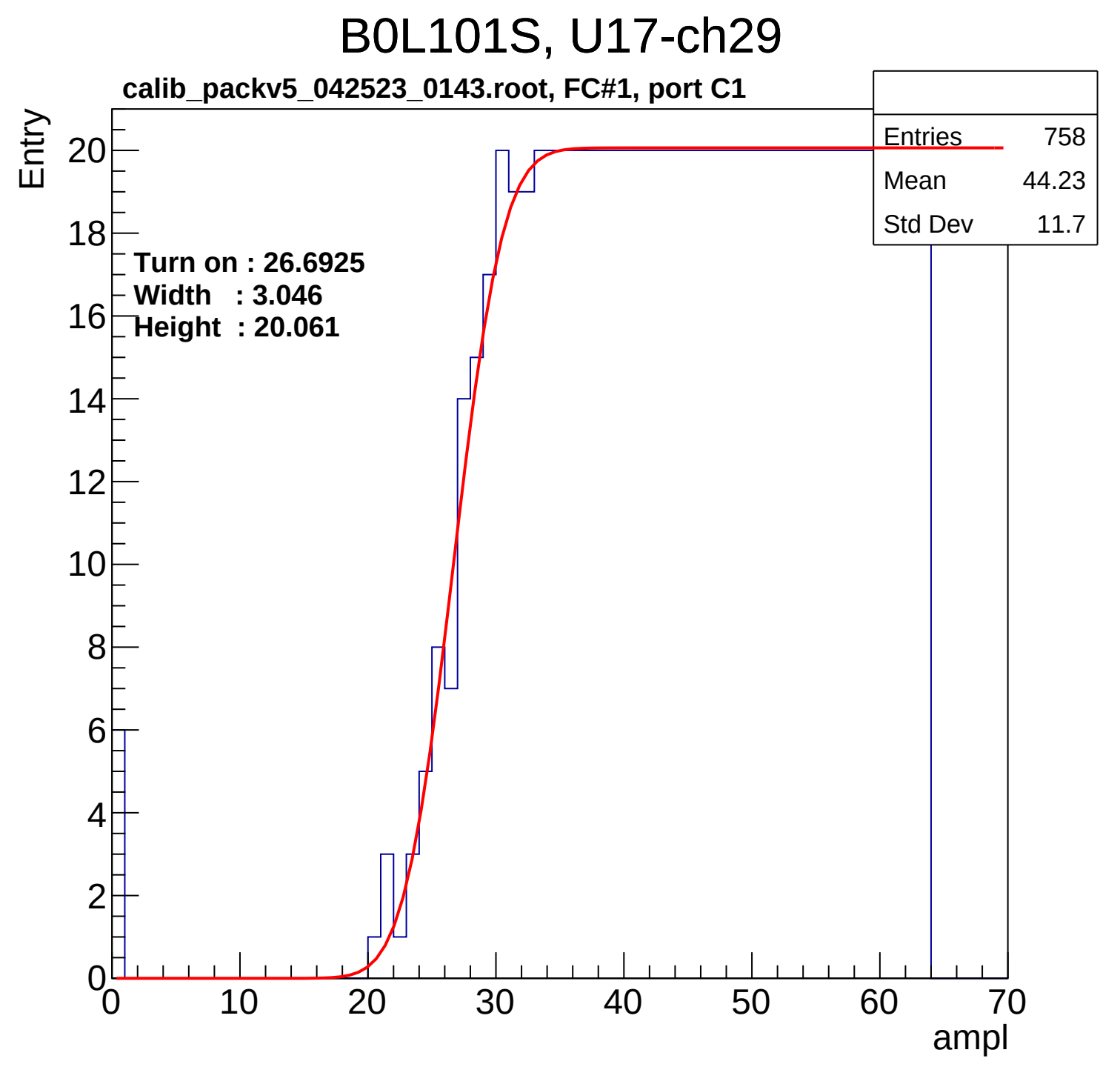
B0L101S, U17-ch29
calib_packv5_042523_0143.root, FC#1, port C1
Entries 758
Mean 44.23
Std Dev 11.7
Turn on : 26.6925
Width : 3.046
Height : 20.061
Entry
ampl
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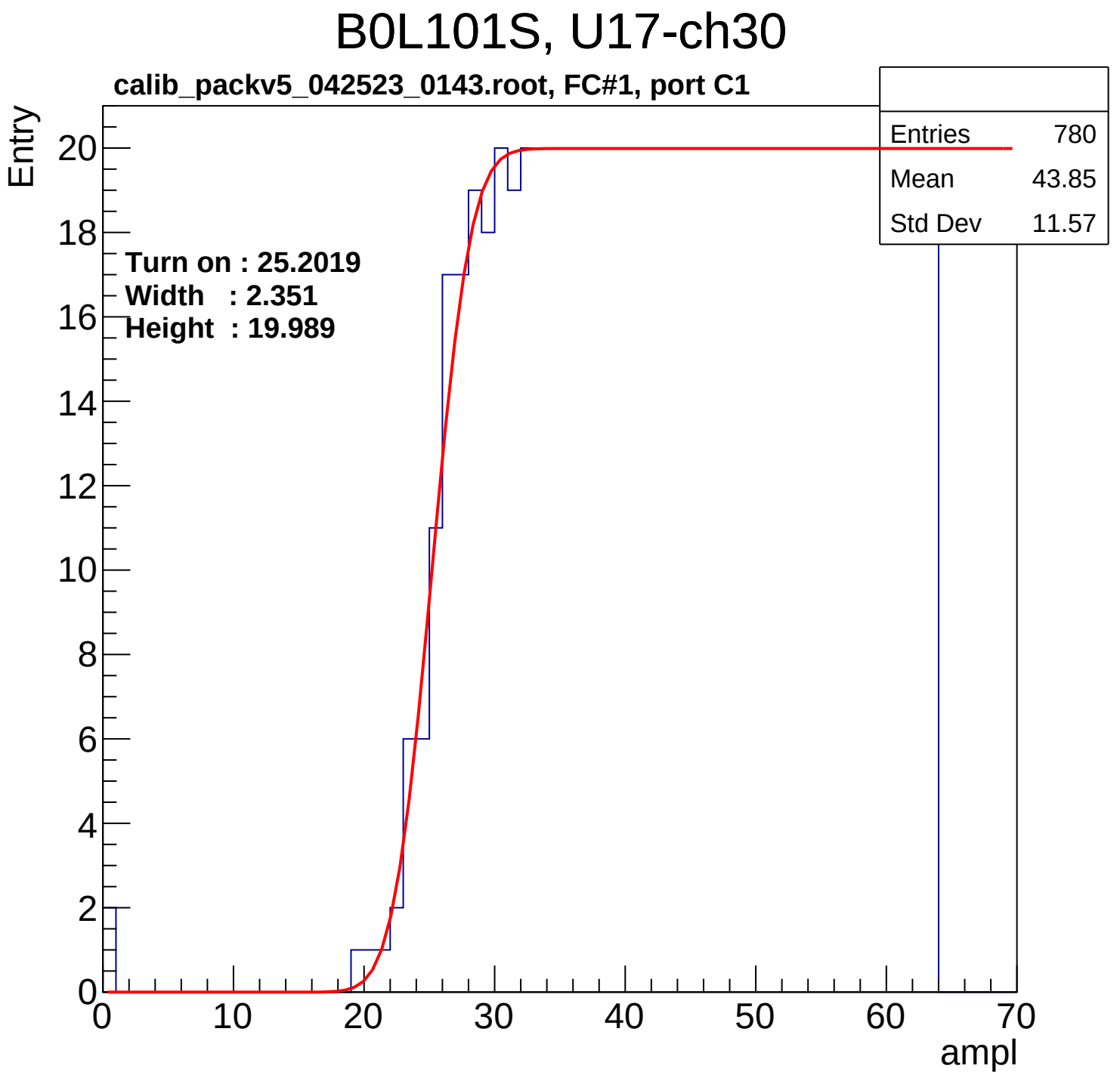
B0L101S, U17-ch30
calib_packv5_042523_0143.root, FC#1, port C1
Entries 780
Mean 43.85
Std Dev 11.57
Turn on : 25.2019
Width : 2.351
Height : 19.989
Entry
ampl
0
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6
8
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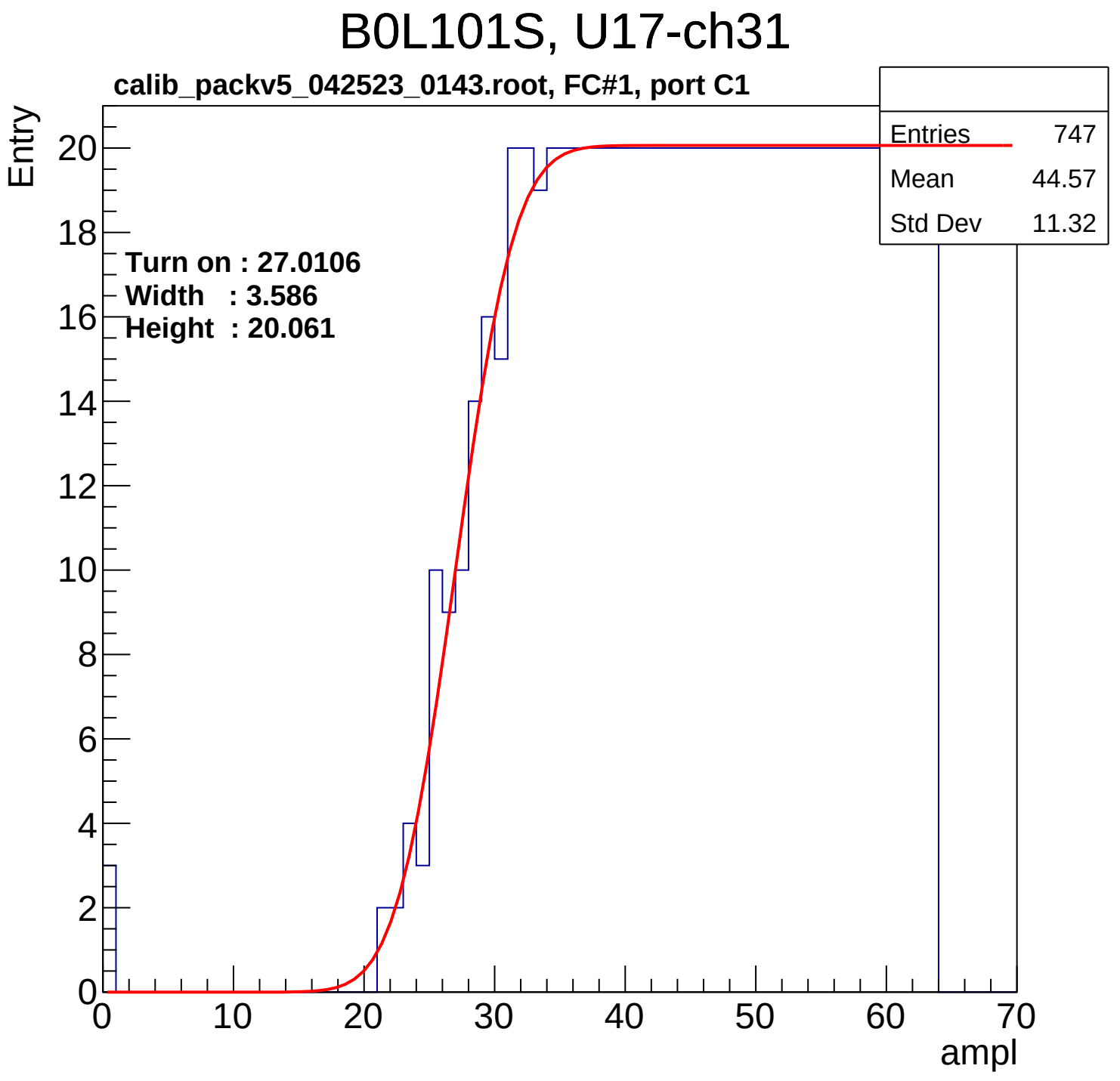
B0L101S, U17-ch31
calib_packv5_042523_0143.root, FC#1, port C1
Entries 747
Mean 44.57
Std Dev 11.32
Turn on : 27.0106
Width : 3.586
Height : 20.061
Entry
ampl
0
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6
8
10
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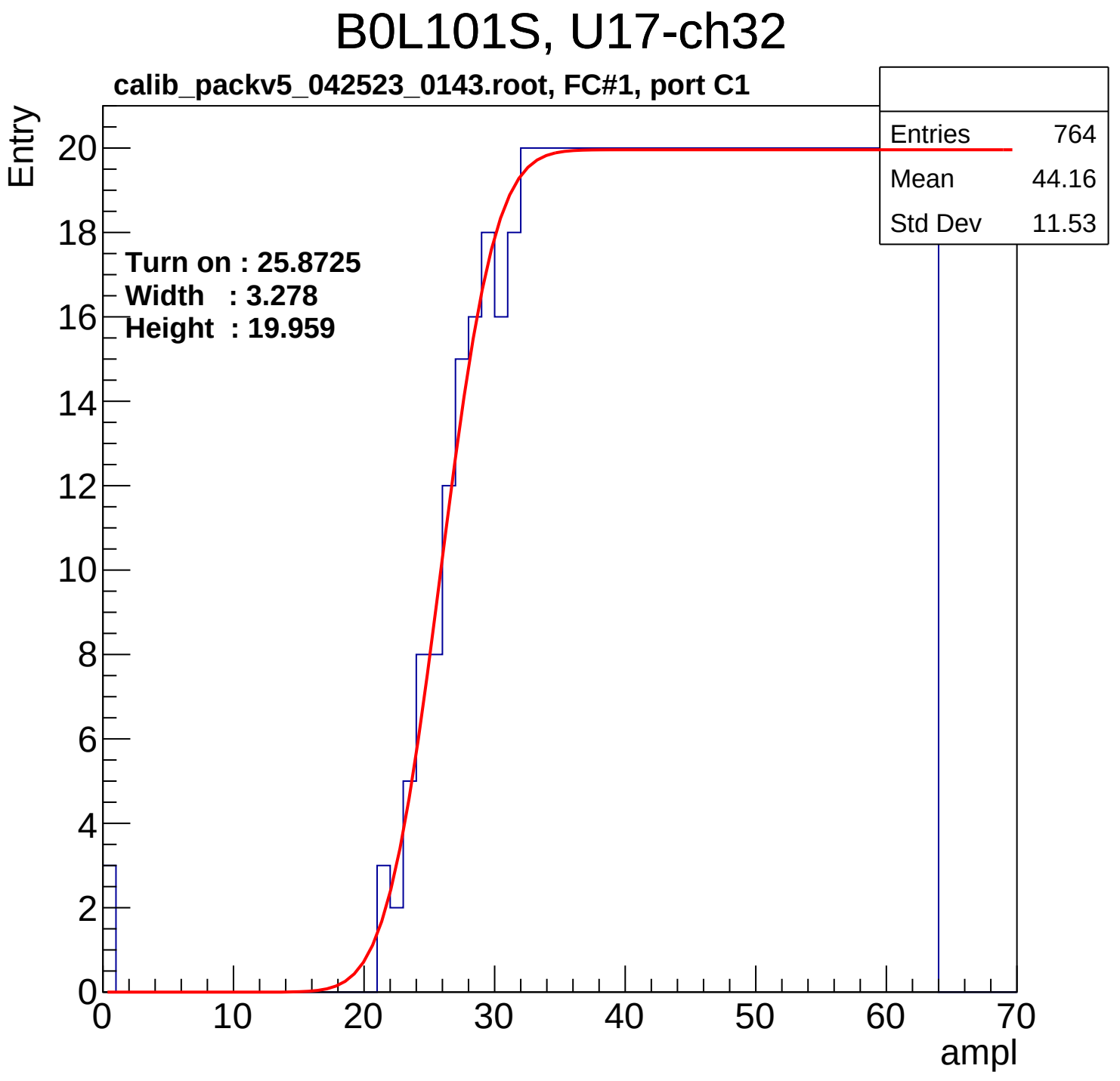
B0L101S, U17-ch32
calib_packv5_042523_0143.root, FC#1, port C1
Entries 764
Mean 44.16
Std Dev 11.53
Turn on : 25.8725
Width : 3.278
Height : 19.959
Entry
ampl
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6
8
10
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14
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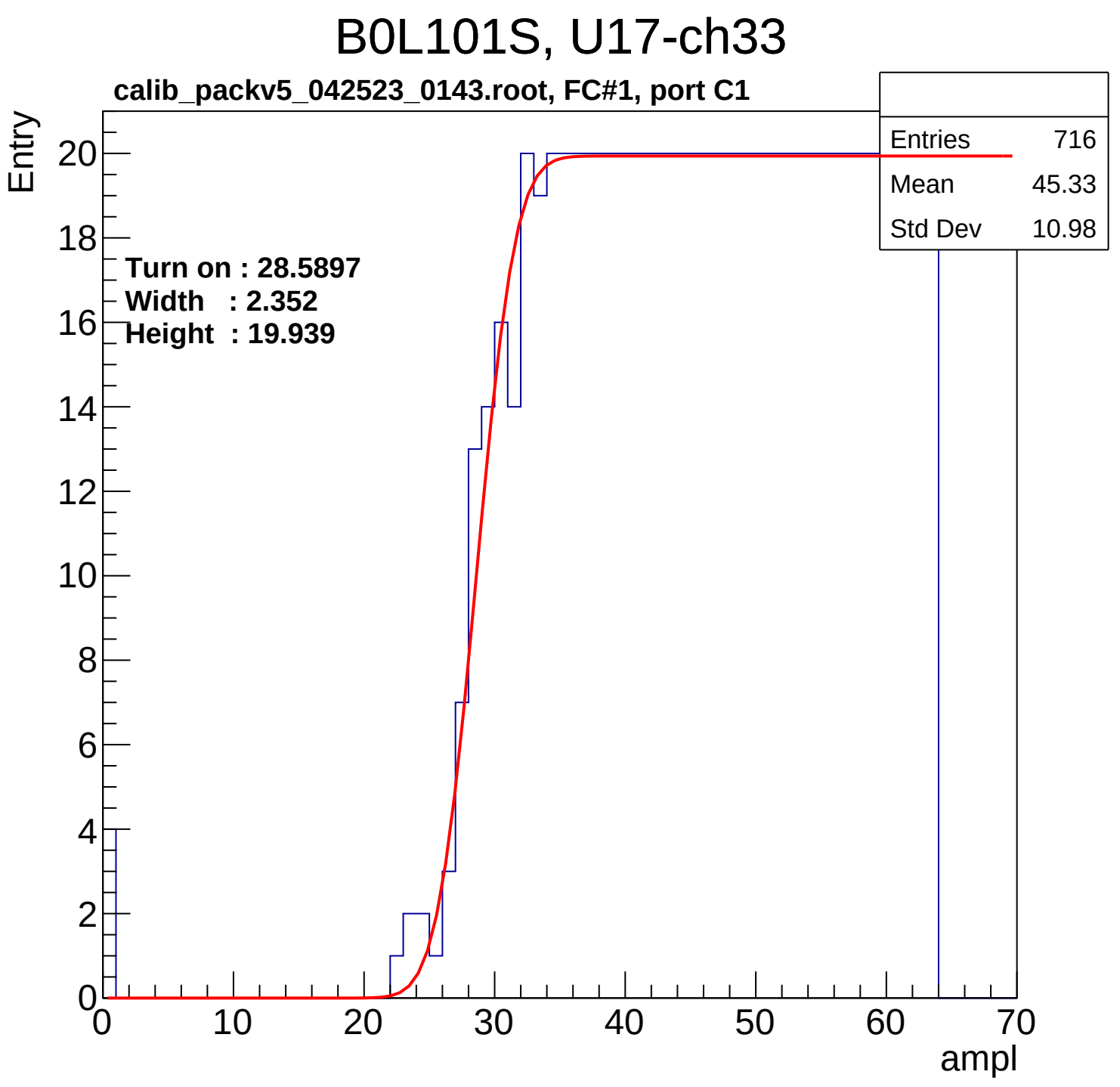
B0L101S, U17-ch33
calib_packv5_042523_0143.root, FC#1, port C1
Entries 716
Mean 45.33
Std Dev 10.98
Turn on : 28.5897
Width : 2.352
Height : 19.939
Entry
ampl
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6
8
10
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14
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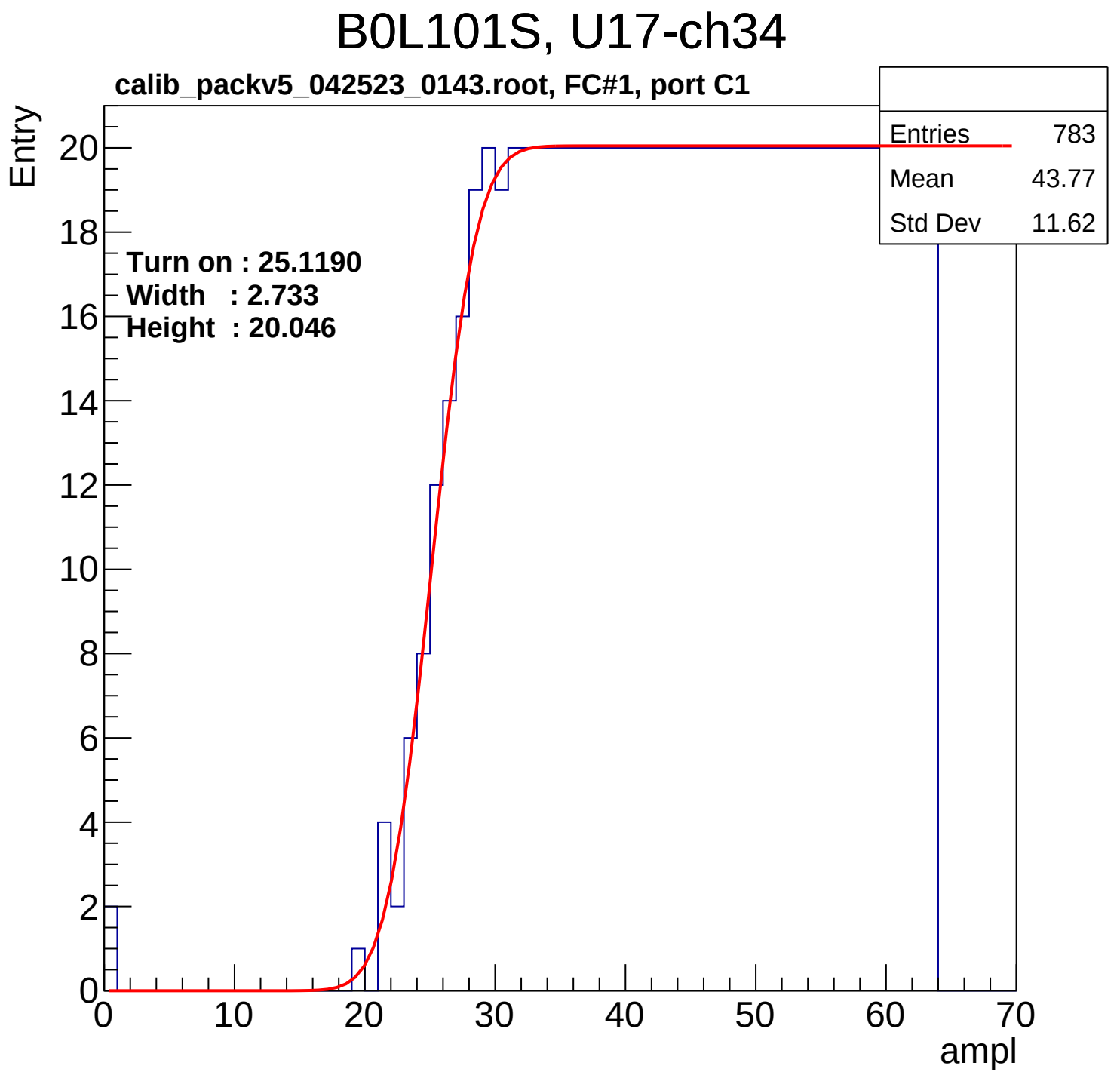
B0L101S, U17-ch34
calib_packv5_042523_0143.root, FC#1, port C1
Entries 783
Mean 43.77
Std Dev 11.62
Turn on : 25.1190
Width : 2.733
Height : 20.046
Entry
ampl
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6
8
10
12
14
16
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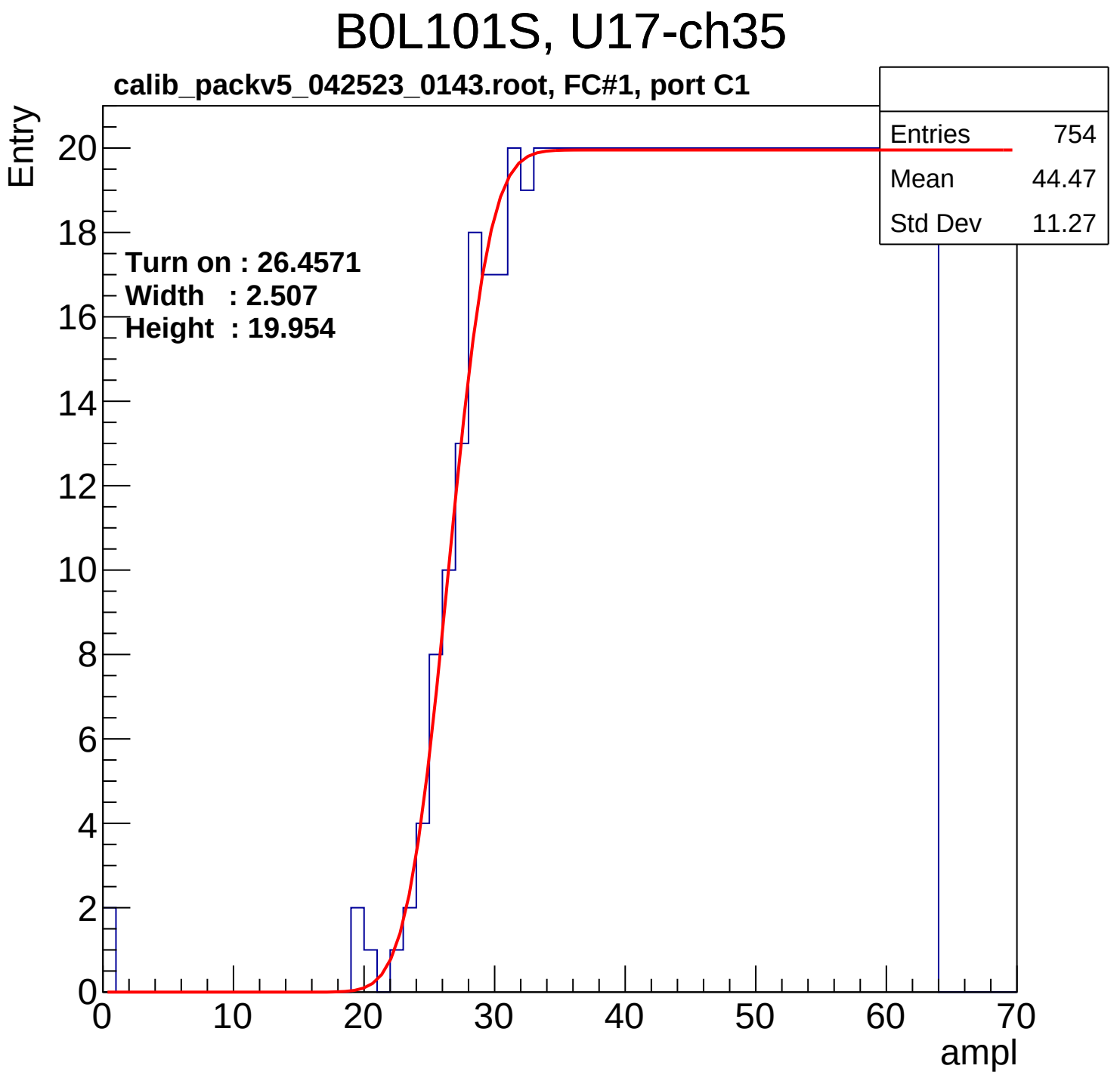
B0L101S, U17-ch35
calib_packv5_042523_0143.root, FC#1, port C1
Entries 754
Mean 44.47
Std Dev 11.27
Turn on : 26.4571
Width : 2.507
Height : 19.954
Entry
ampl
0
2
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6
8
10
12
14
16
18
20
0
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20
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40
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60
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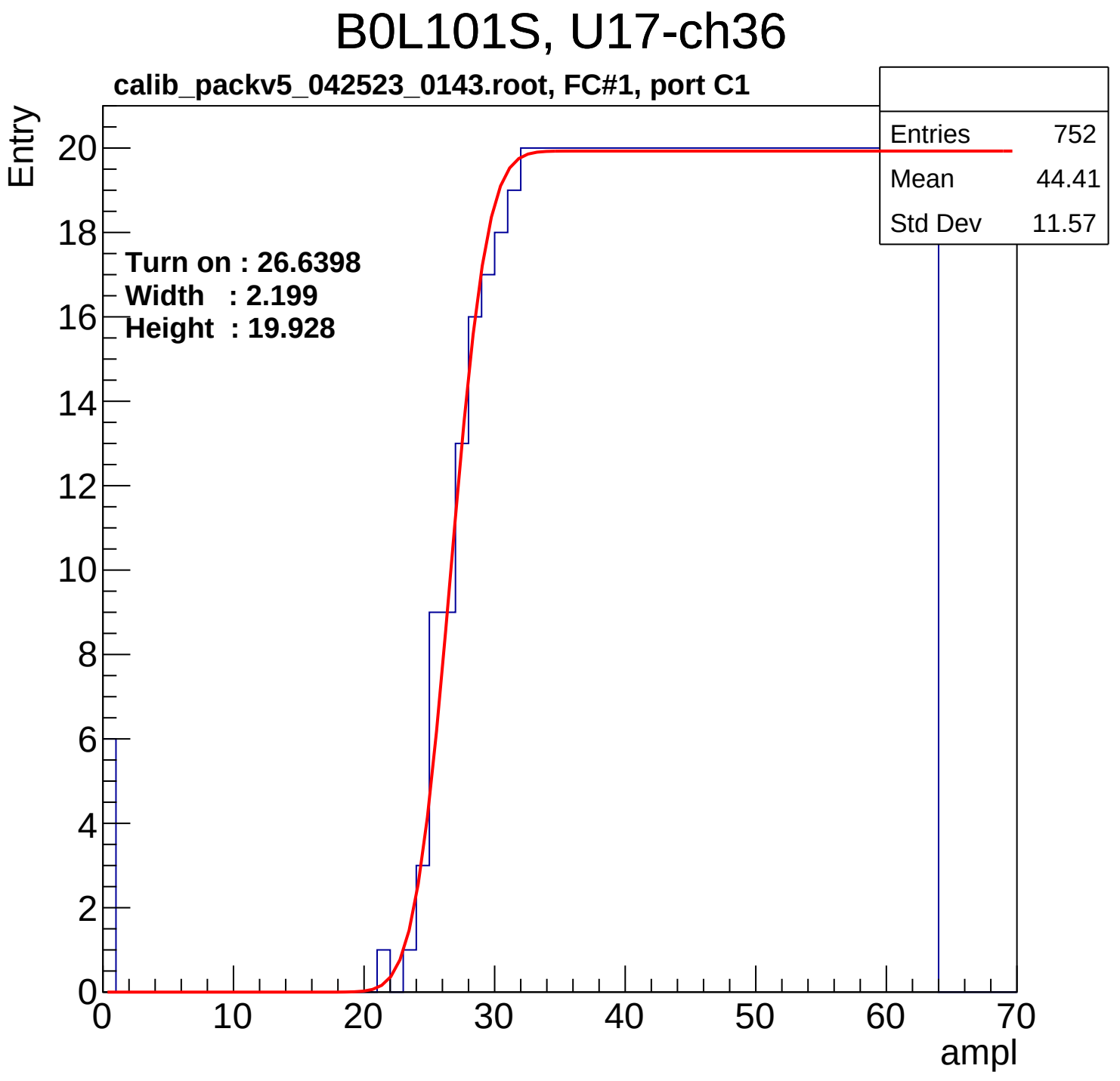
B0L101S, U17-ch36
calib_packv5_042523_0143.root, FC#1, port C1
Entries 752
Mean 44.41
Std Dev 11.57
Turn on : 26.6398
Width : 2.199
Height : 19.928
Entry
ampl
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6
8
10
12
14
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60
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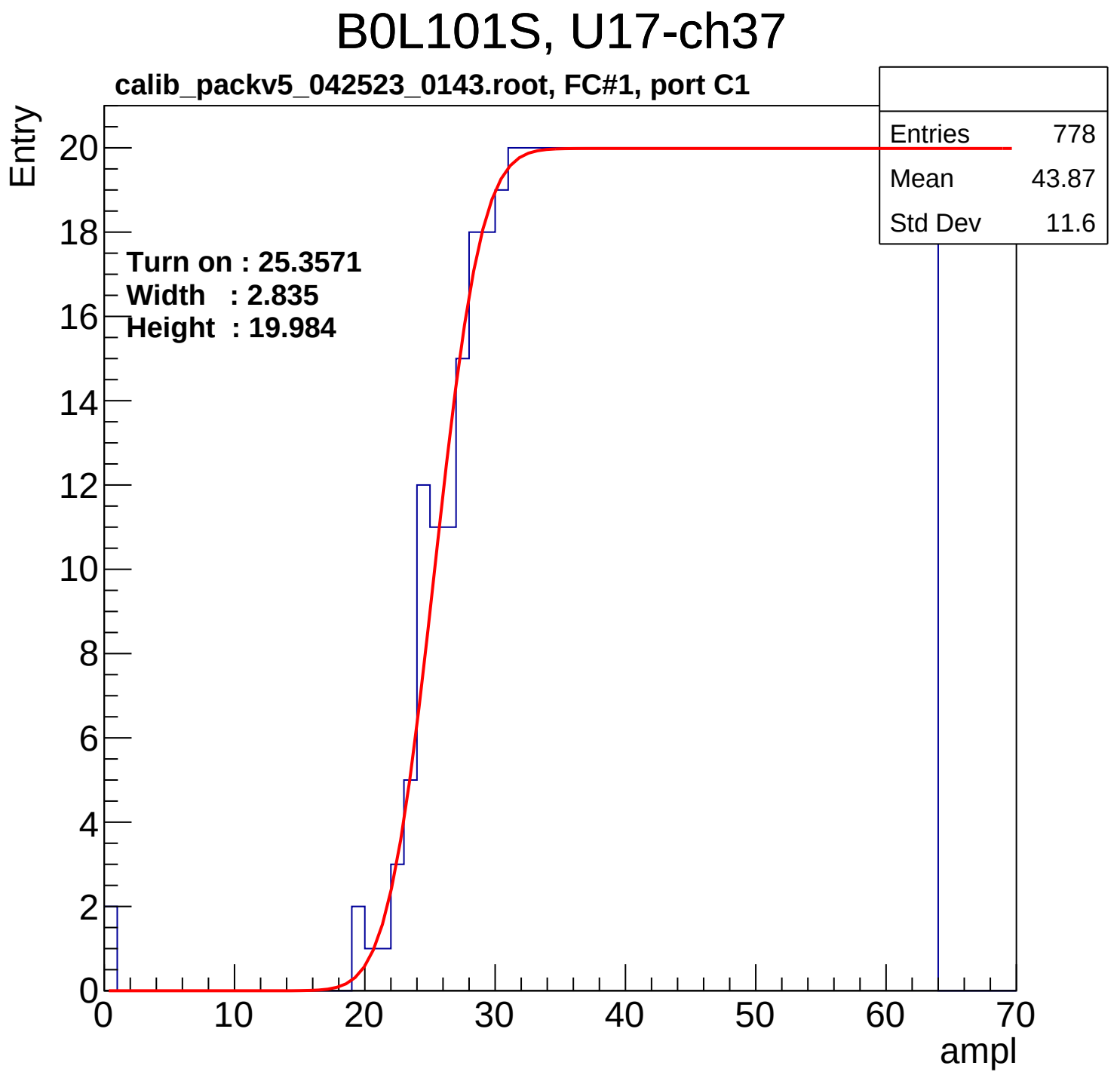
B0L101S, U17-ch37
calib_packv5_042523_0143.root, FC#1, port C1
Entries 778
Mean 43.87
Std Dev 11.6
Turn on : 25.3571
Width : 2.835
Height : 19.984
Entry
ampl
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6
8
10
12
14
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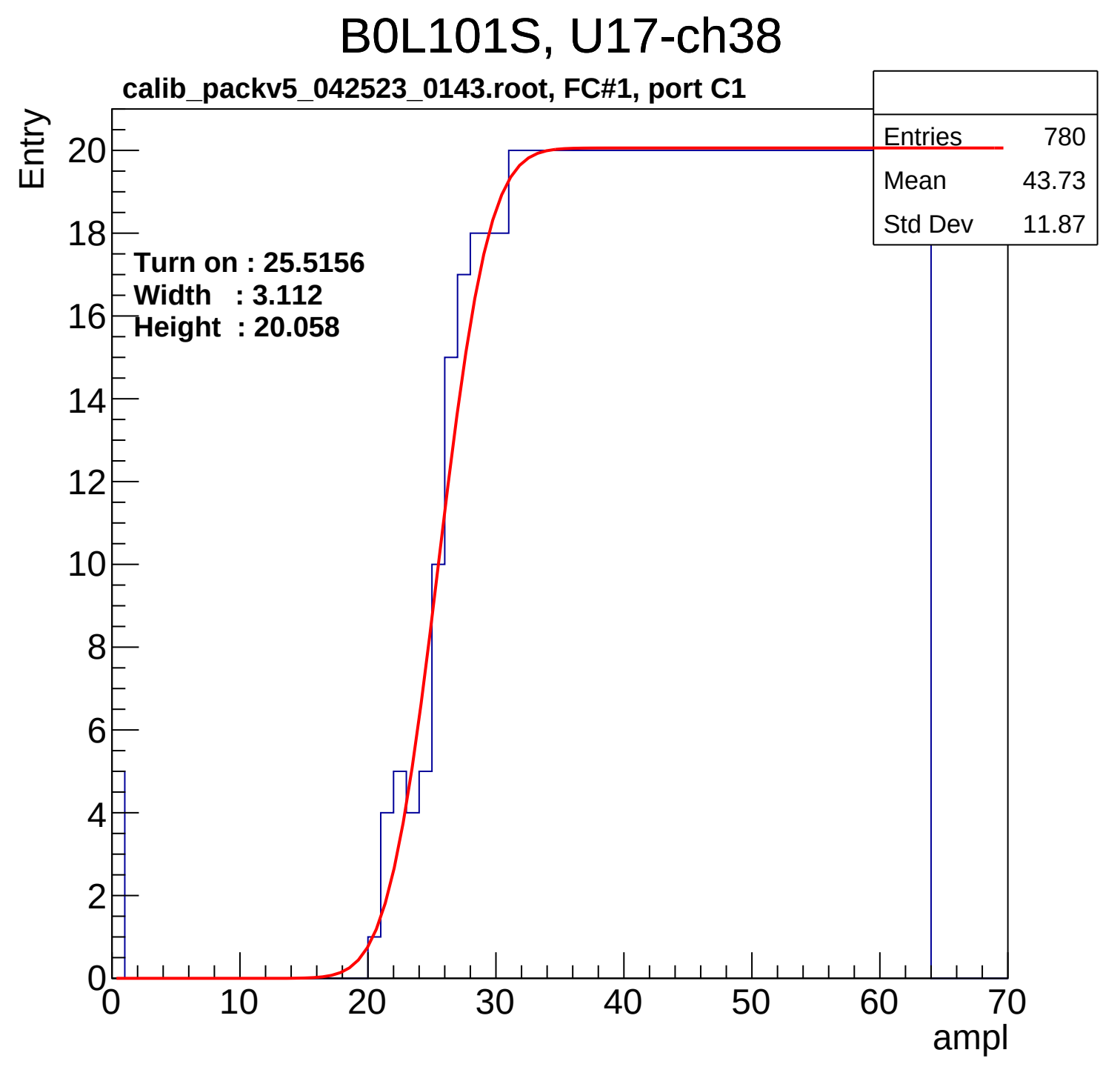
B0L101S, U17-ch38
calib_packv5_042523_0143.root, FC#1, port C1
Entries 780
Mean 43.73
Std Dev 11.87
Turn on : 25.5156
Width : 3.112
Height : 20.058
Entry
ampl
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6
8
10
12
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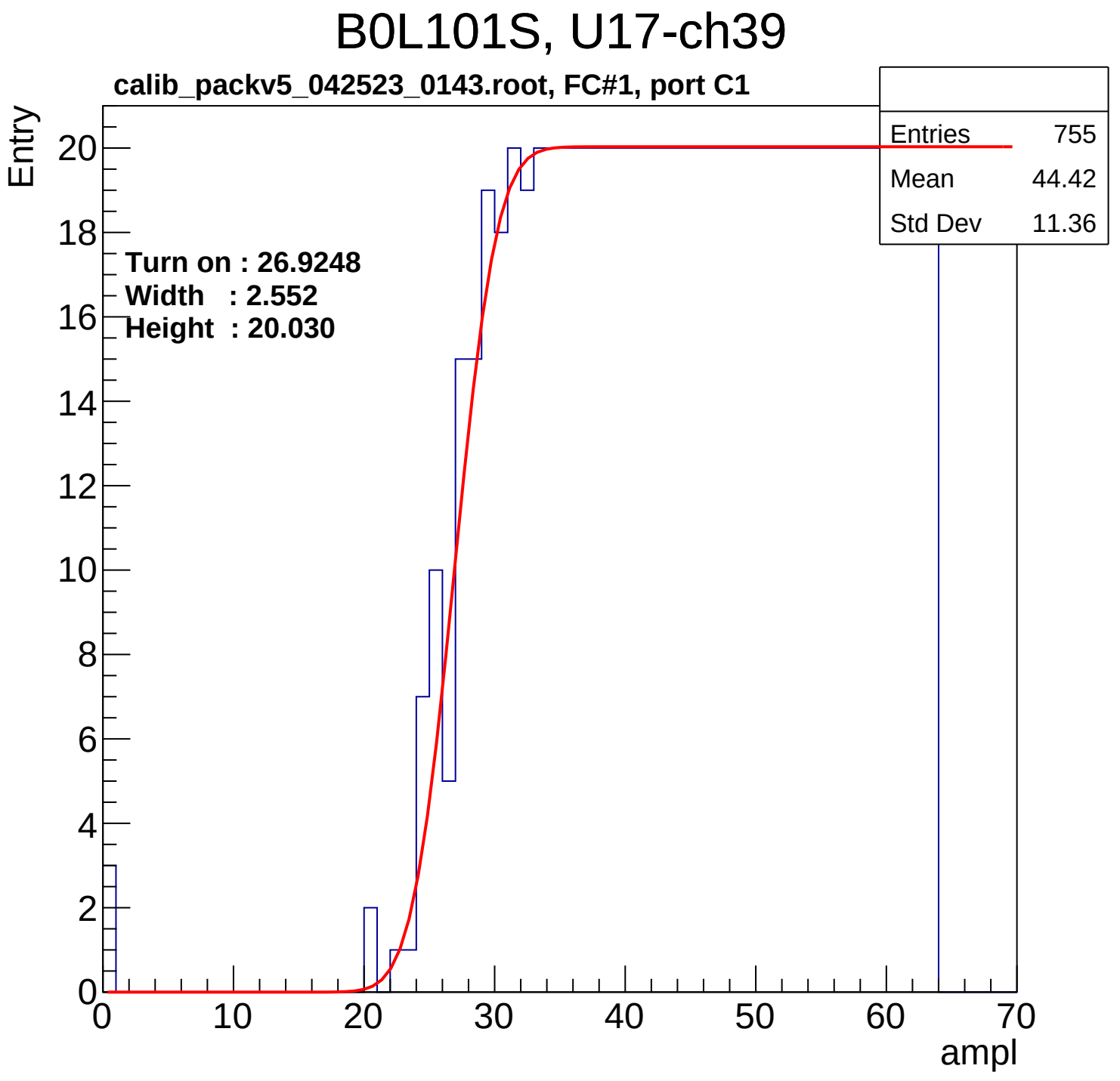
B0L101S, U17-ch39
calib_packv5_042523_0143.root, FC#1, port C1
Entries 755
Mean 44.42
Std Dev 11.36
Turn on : 26.9248
Width : 2.552
Height : 20.030
Entry
ampl
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6
8
10
12
14
16
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0
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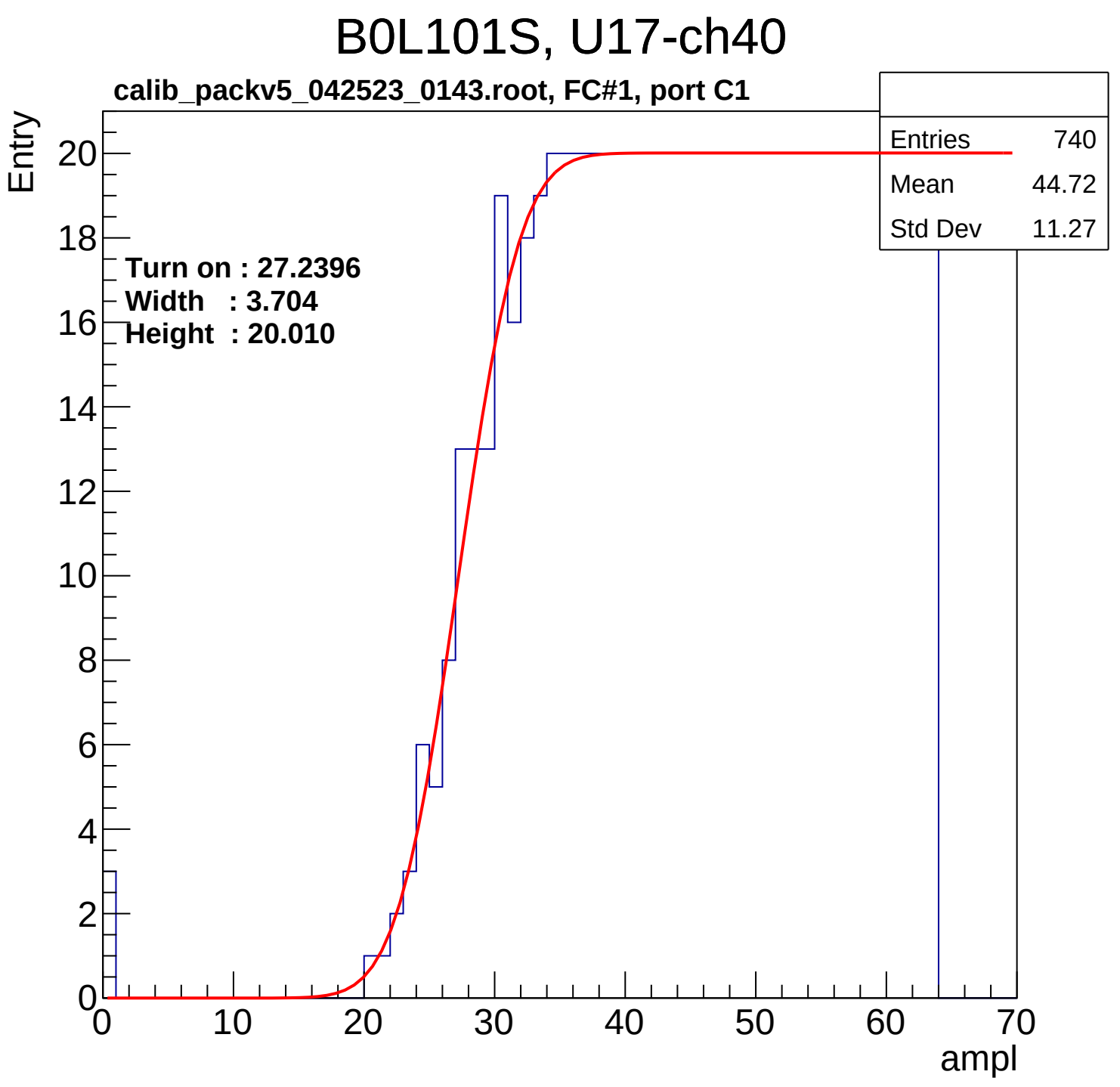
B0L101S, U17-ch40
calib_packv5_042523_0143.root, FC#1, port C1
Entries 740
Mean 44.72
Std Dev 11.27
Turn on : 27.2396
Width : 3.704
Height : 20.010
Entry
ampl
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6
8
10
12
14
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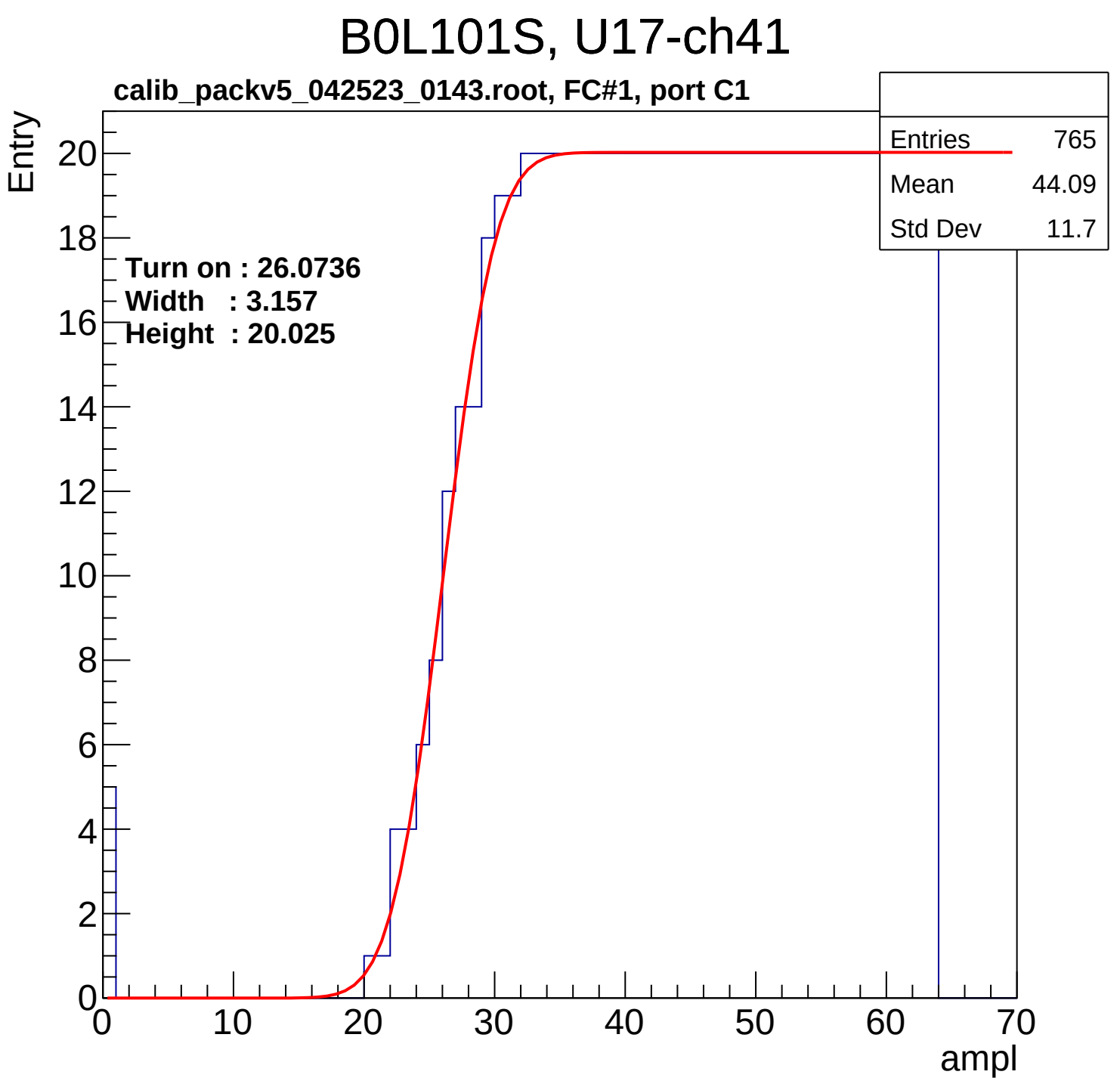
B0L101S, U17-ch41
calib_packv5_042523_0143.root, FC#1, port C1
Entries 765
Mean 44.09
Std Dev 11.7
Turn on : 26.0736
Width : 3.157
Height : 20.025
Entry
ampl
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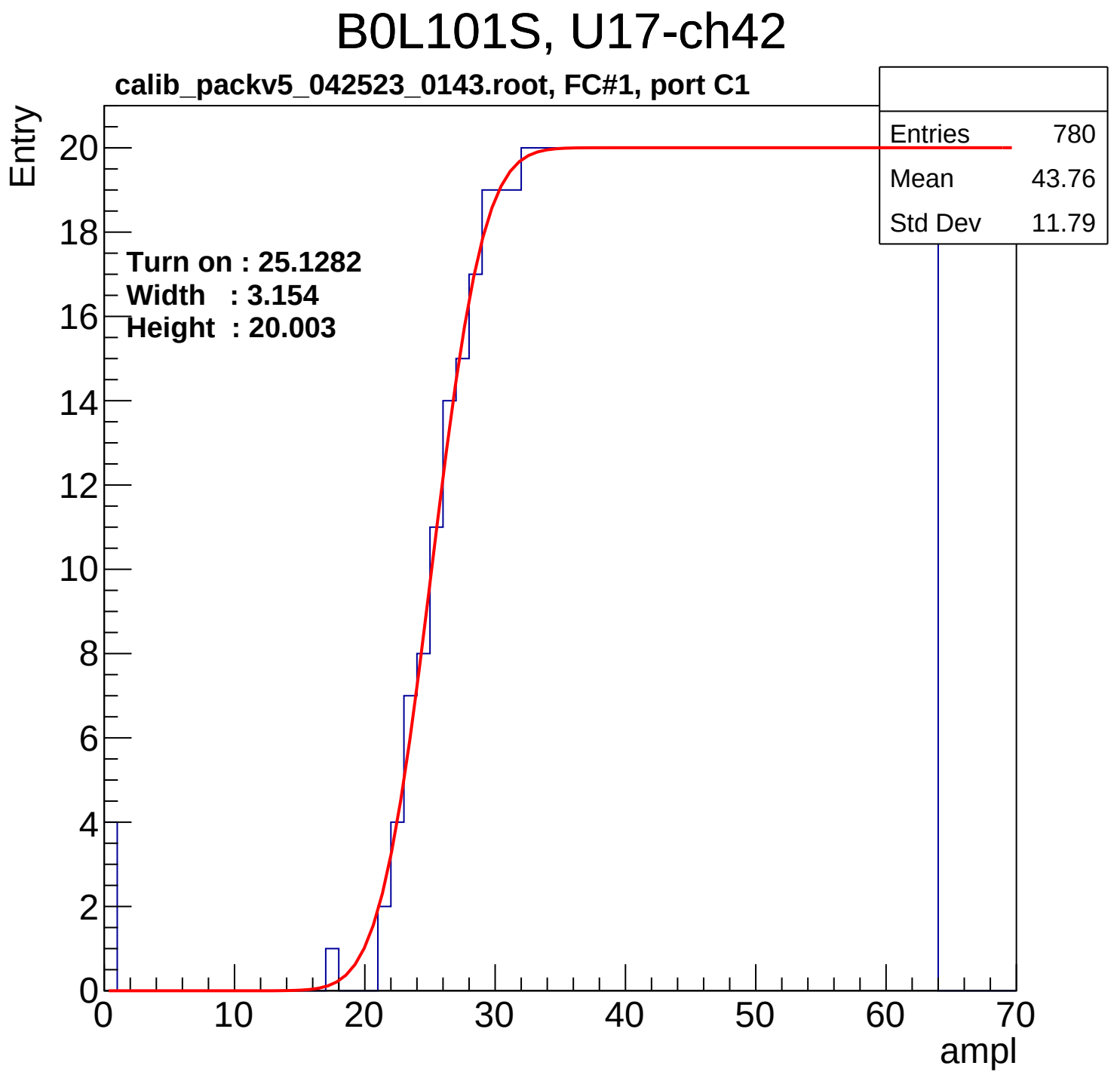
B0L101S, U17-ch42
calib_packv5_042523_0143.root, FC#1, port C1
Entries 780
Mean 43.76
Std Dev 11.79
Turn on : 25.1282
Width : 3.154
Height : 20.003
Entry
ampl
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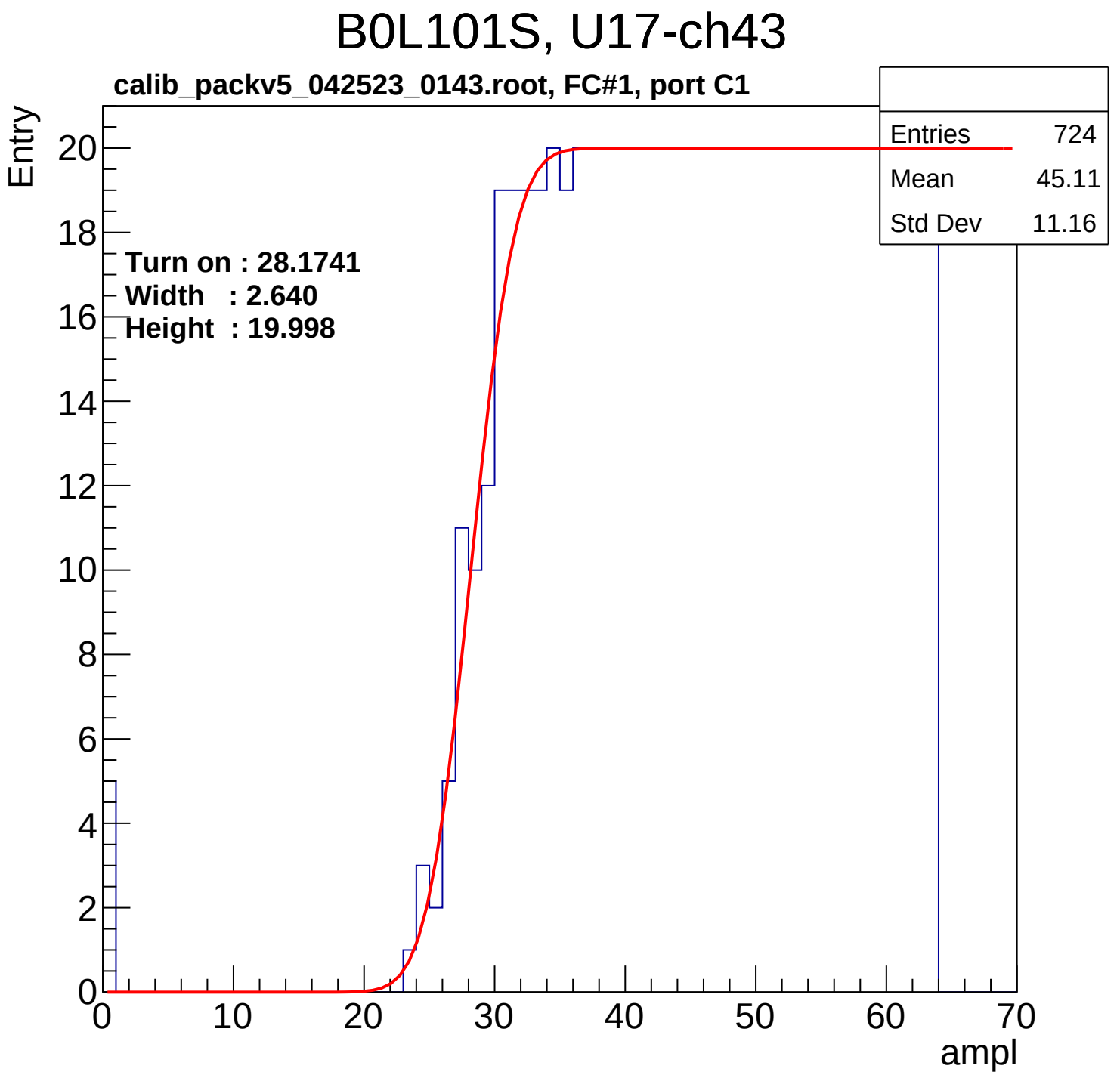
B0L101S, U17-ch43
calib_packv5_042523_0143.root, FC#1, port C1
Entries 724
Mean 45.11
Std Dev 11.16
Turn on : 28.1741
Width : 2.640
Height : 19.998
Entry
ampl
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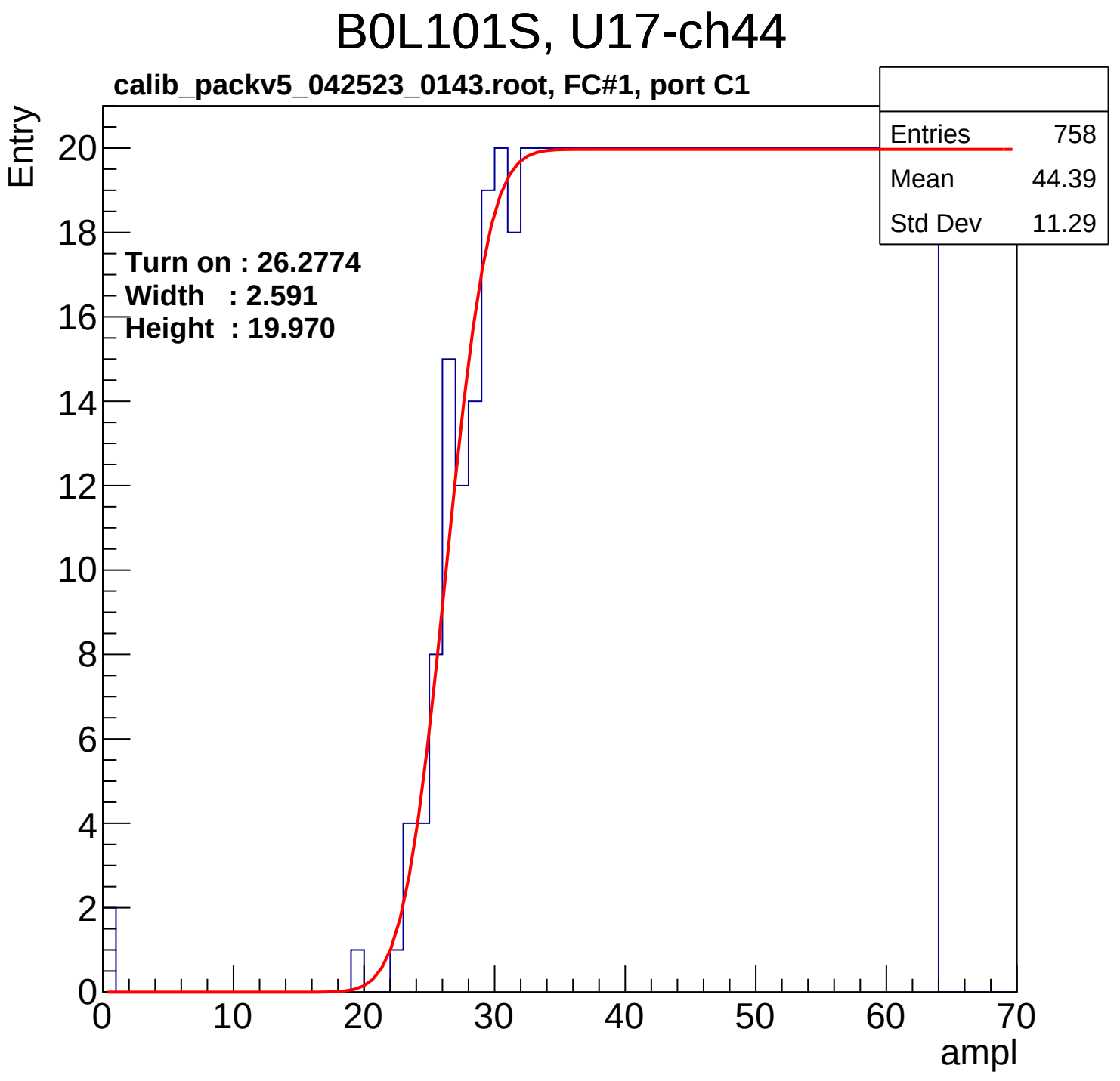
B0L101S, U17-ch44
calib_packv5_042523_0143.root, FC#1, port C1
Entries 758
Mean 44.39
Std Dev 11.29
Turn on : 26.2774
Width : 2.591
Height : 19.970
Entry
ampl
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10
12
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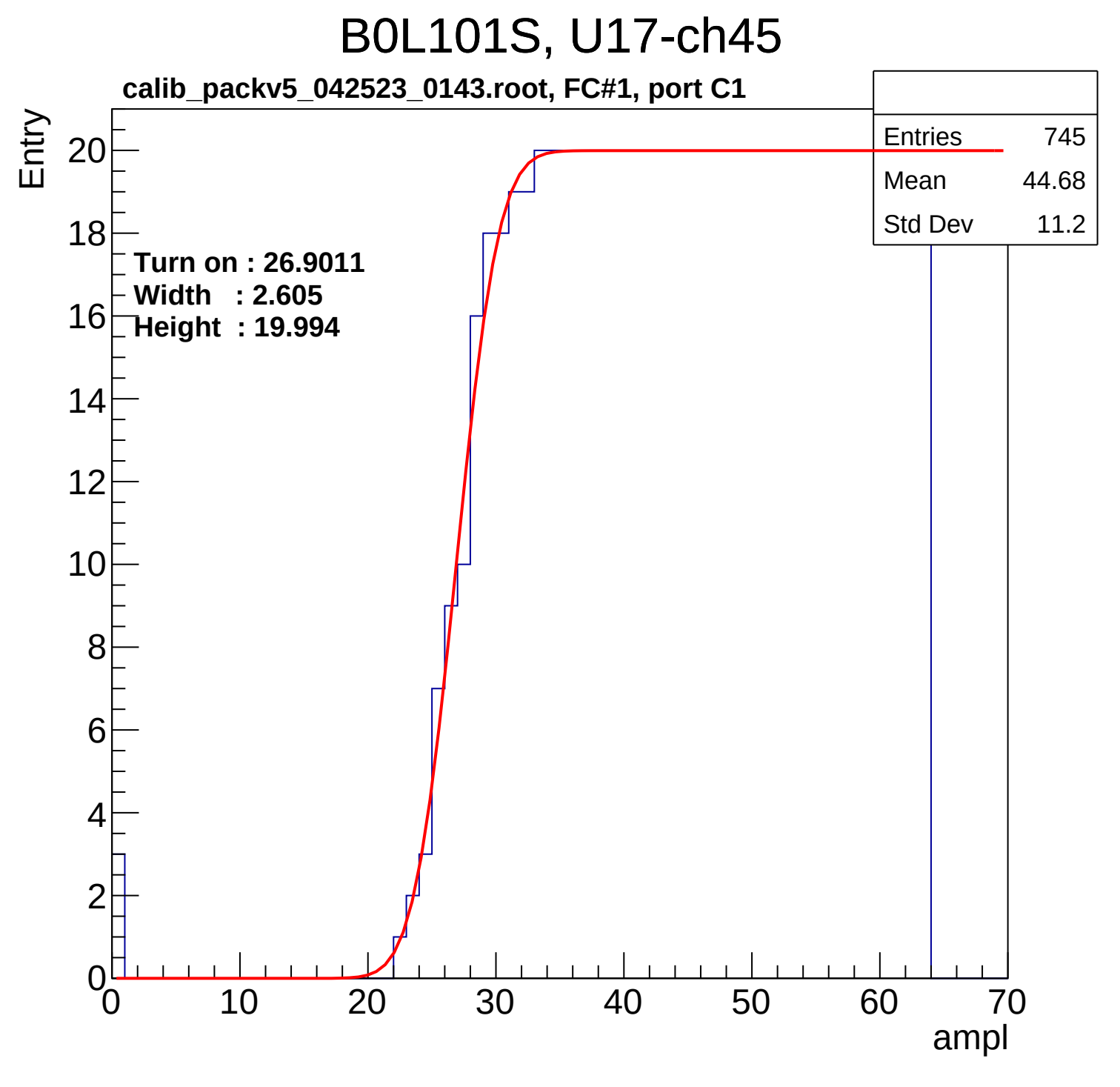
B0L101S, U17-ch45
calib_packv5_042523_0143.root, FC#1, port C1
Entries 745
Mean 44.68
Std Dev 11.2
Turn on : 26.9011
Width : 2.605
Height : 19.994
Entry
ampl
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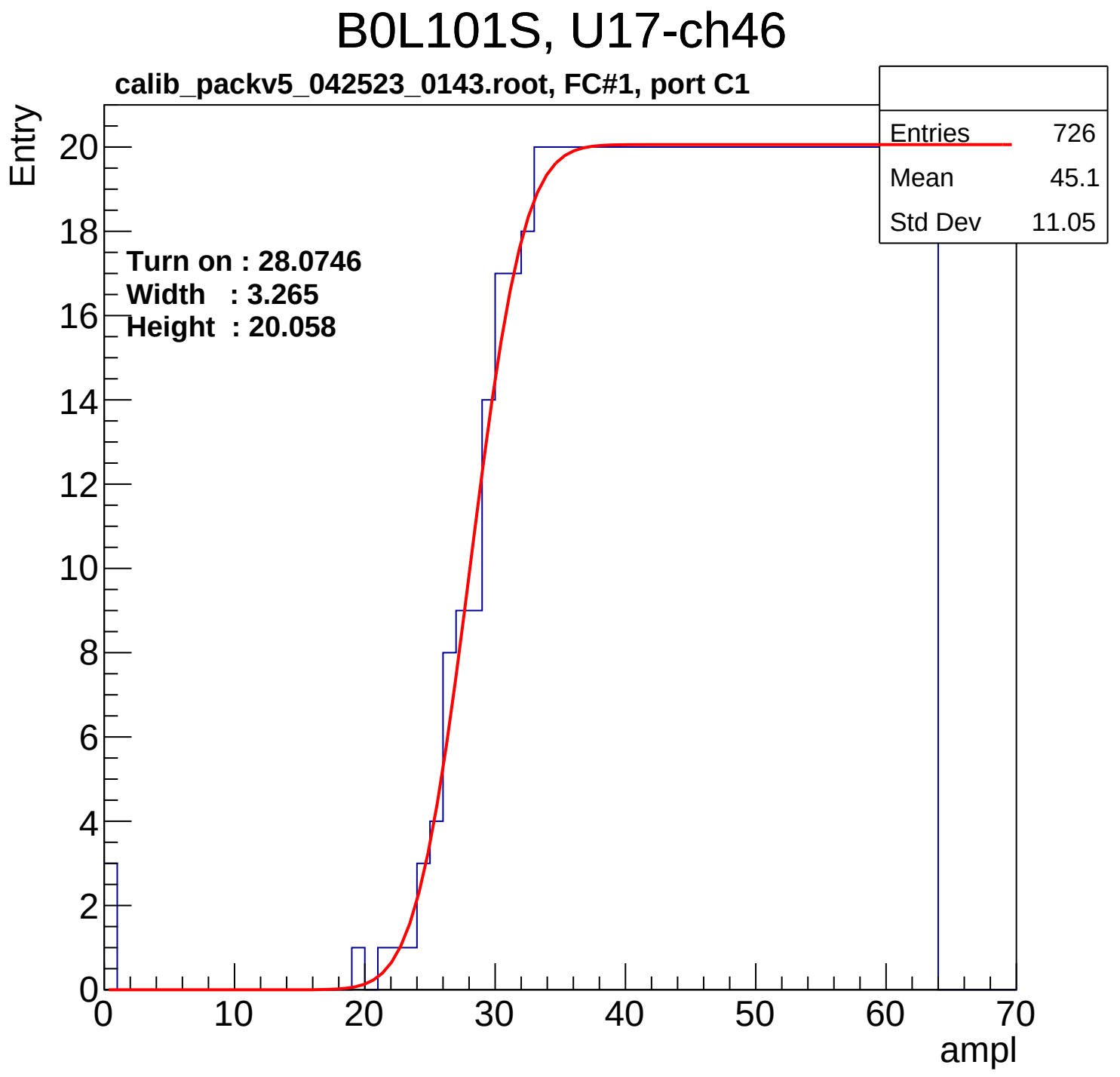
B0L101S, U17-ch46
calib_packv5_042523_0143.root, FC#1, port C1
Entries 726
Mean 45.1
Std Dev 11.05
Turn on : 28.0746
Width : 3.265
Height : 20.058
Entry
ampl
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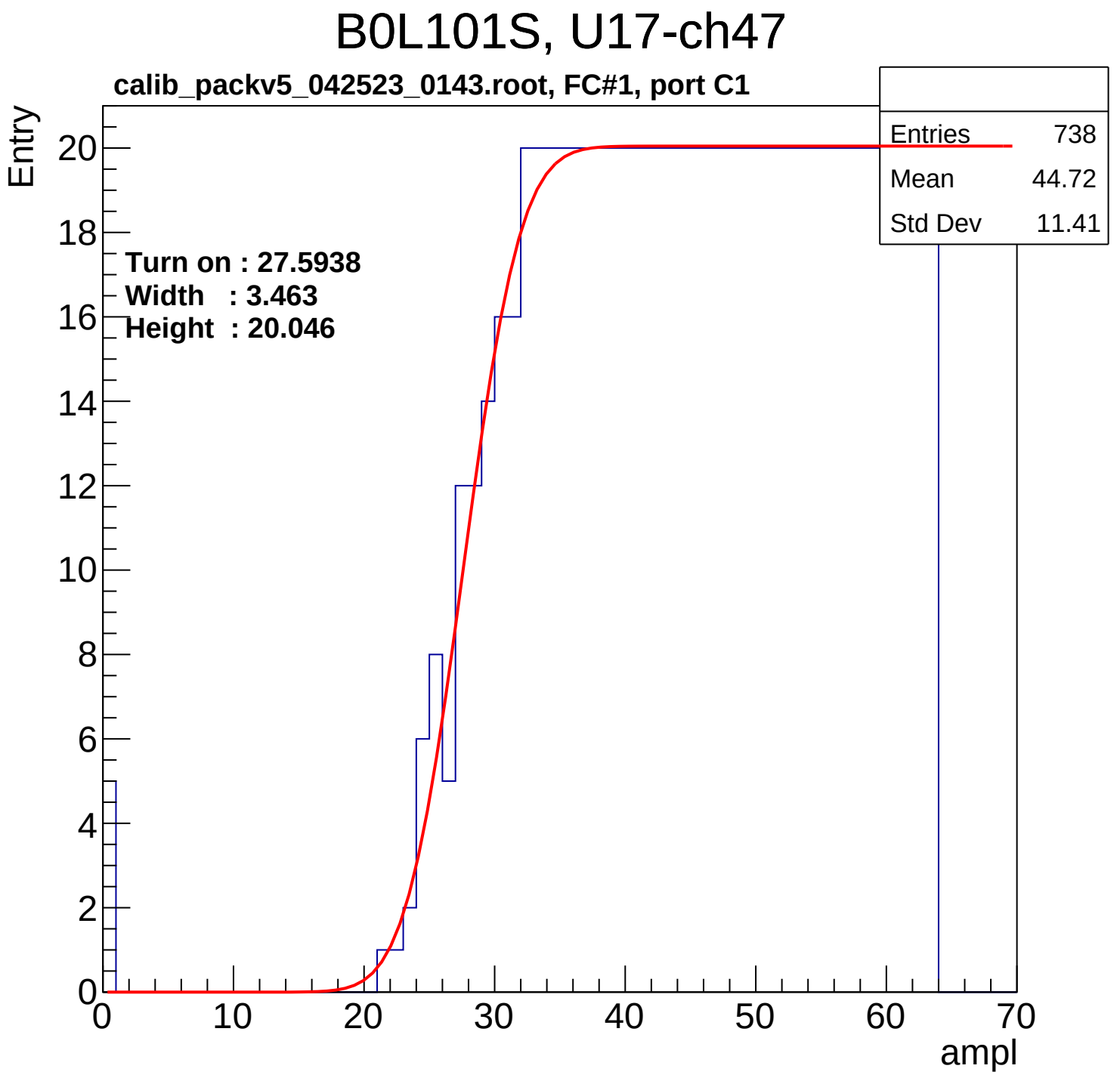
B0L101S, U17-ch47
calib_packv5_042523_0143.root, FC#1, port C1
Entries 738
Mean 44.72
Std Dev 11.41
Turn on : 27.5938
Width : 3.463
Height : 20.046
Entry
ampl
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8
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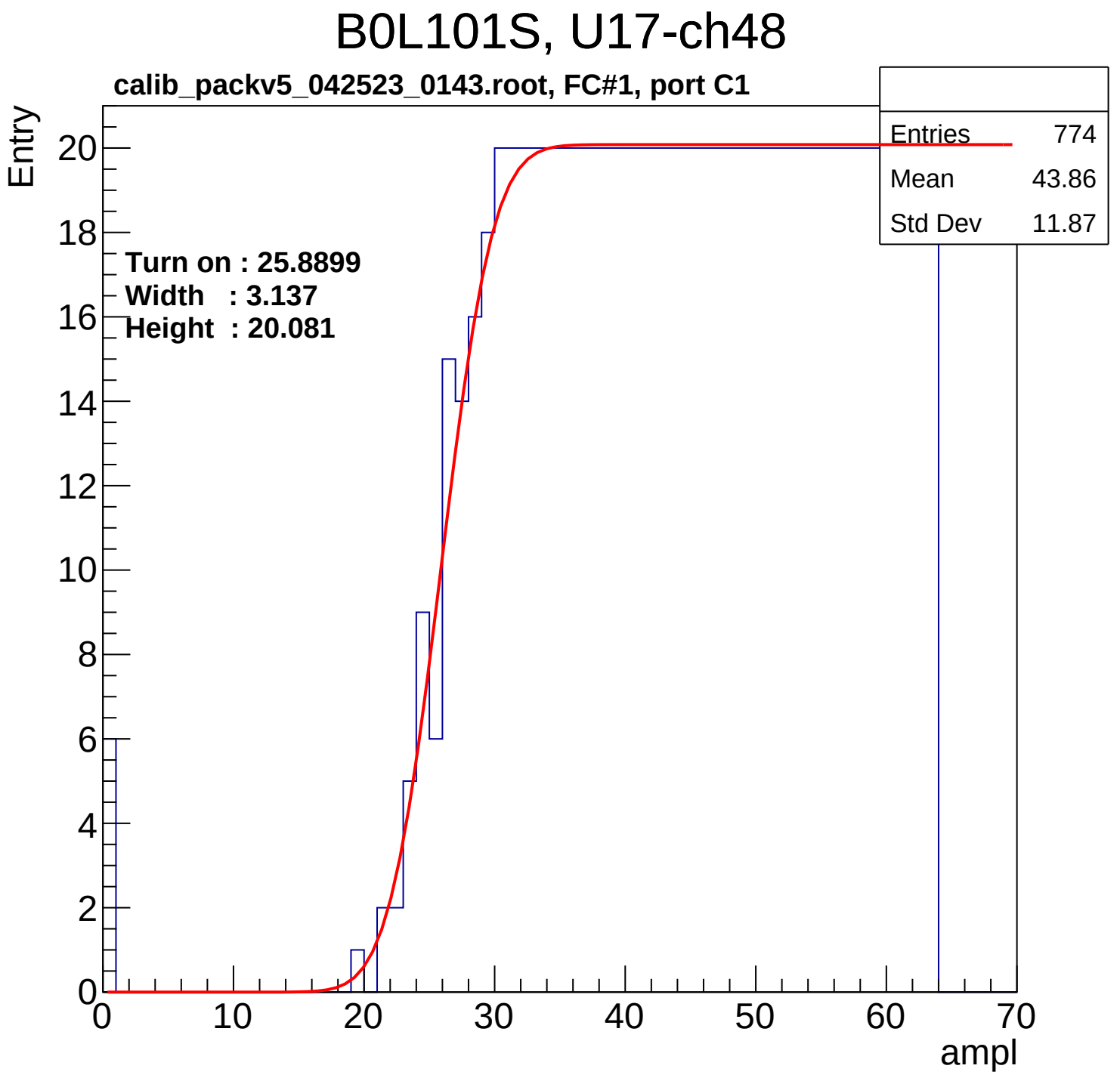
B0L101S, U17-ch48
calib_packv5_042523_0143.root, FC#1, port C1
Entries 774
Mean 43.86
Std Dev 11.87
Turn on : 25.8899
Width : 3.137
Height : 20.081
Entry
ampl
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6
8
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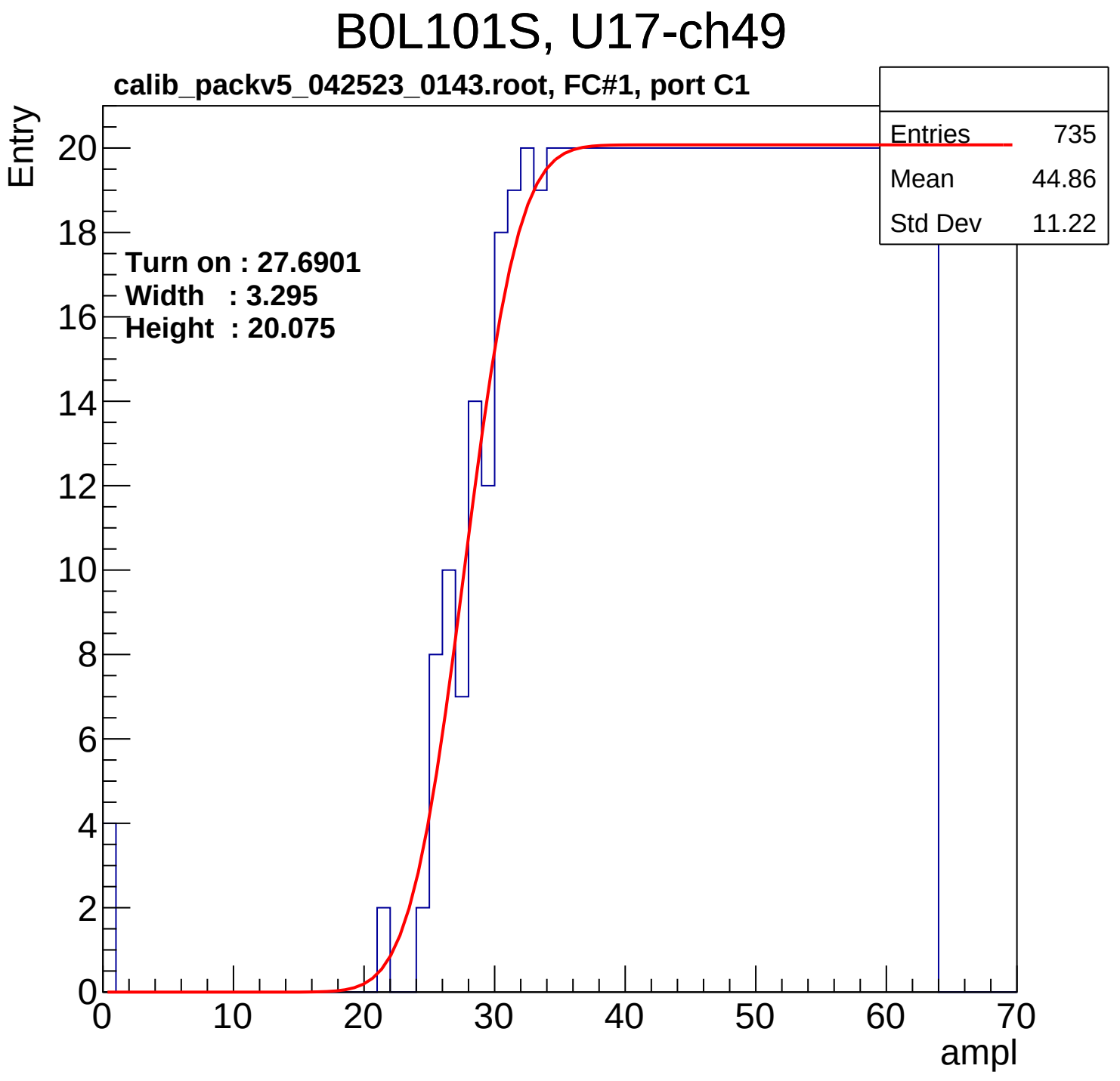
B0L101S, U17-ch49
calib_packv5_042523_0143.root, FC#1, port C1
Entries 735
Mean 44.86
Std Dev 11.22
Turn on : 27.6901
Width : 3.295
Height : 20.075
Entry
ampl
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6
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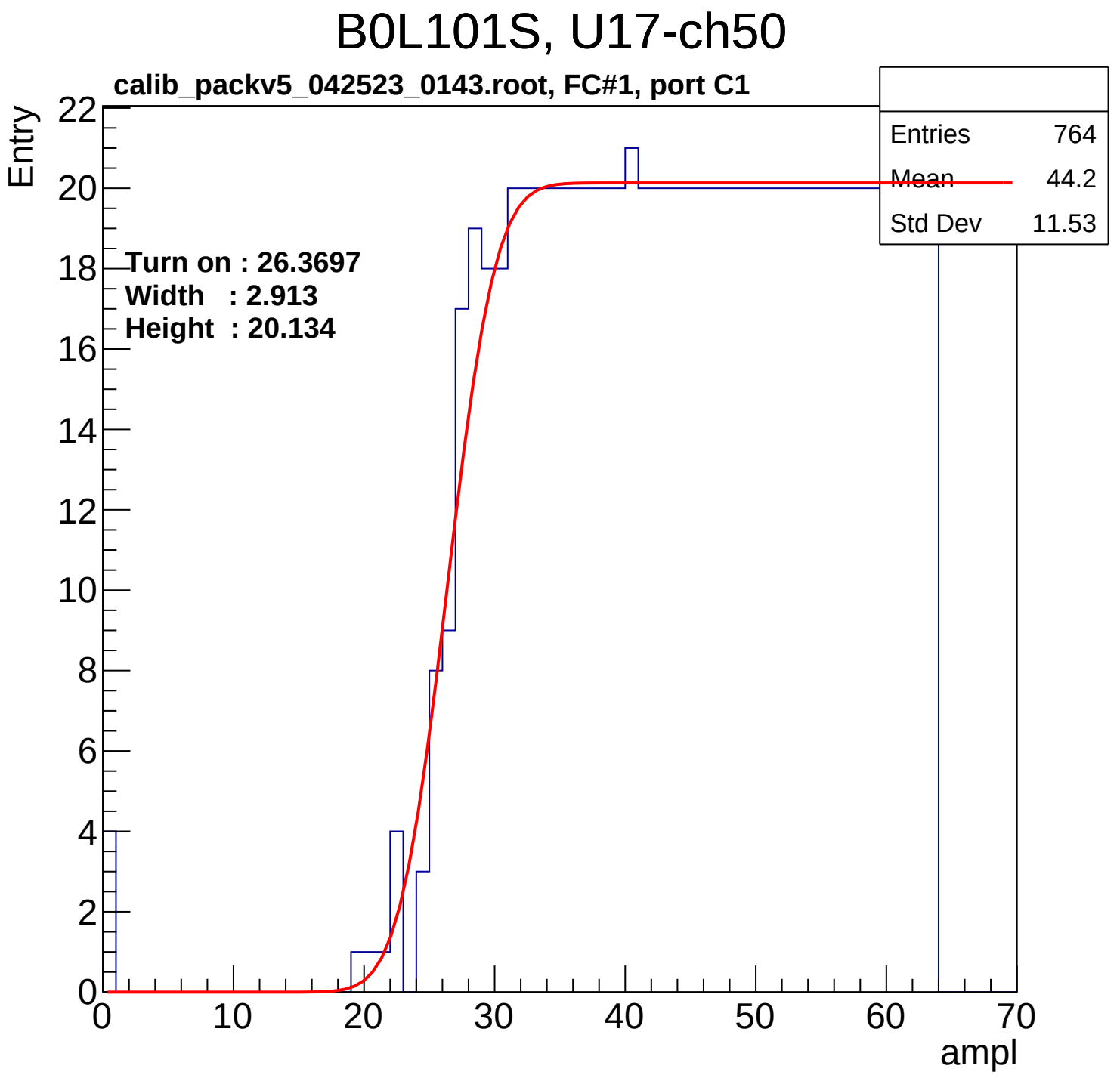
B0L101S, U17-ch50
calib_packv5_042523_0143.root, FC#1, port C1
Entries 764
Mean 44.2
Std Dev 11.53
Turn on : 26.3697
Width : 2.913
Height : 20.134
Entry
ampl
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8
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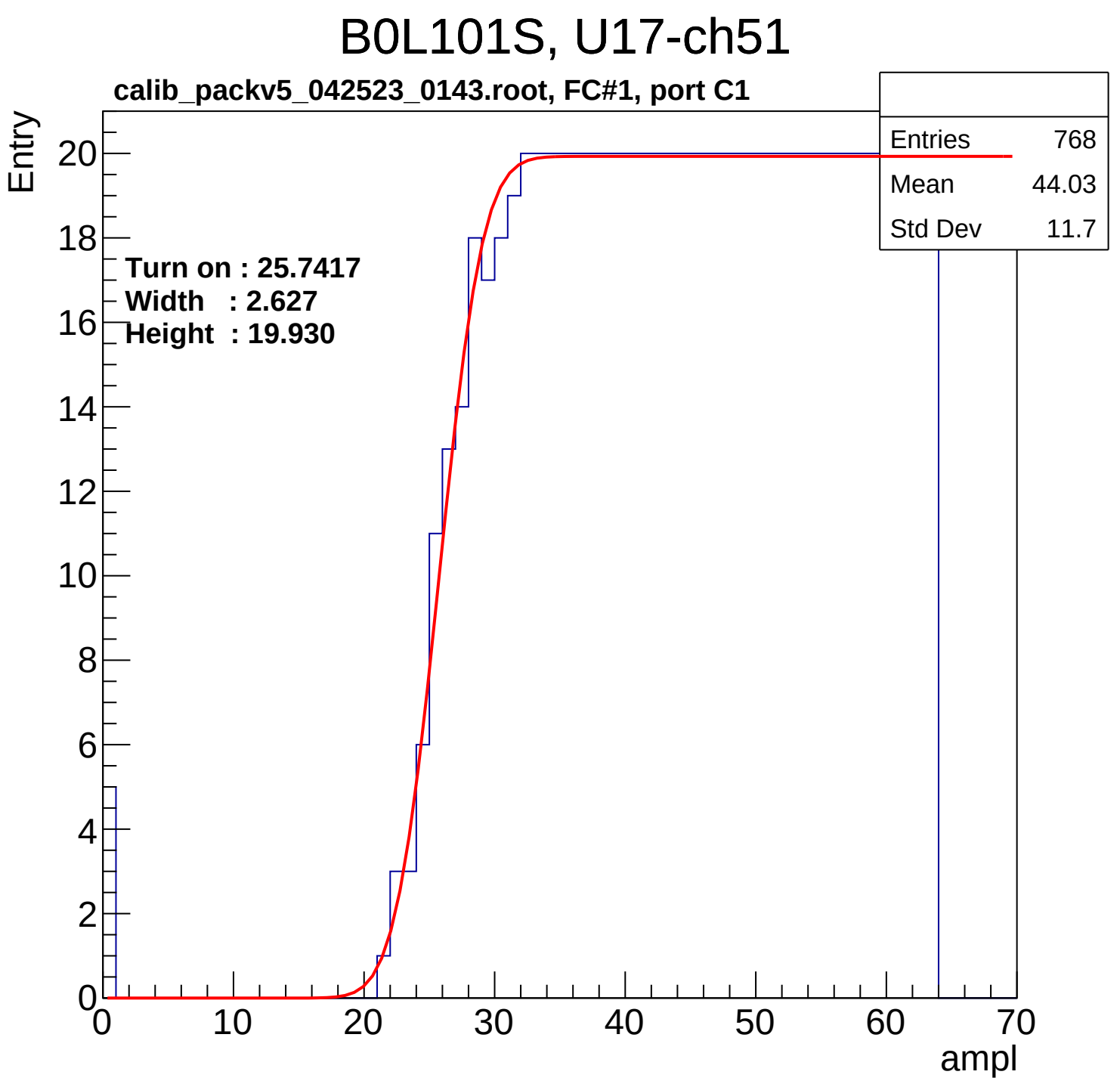
B0L101S, U17-ch51
calib_packv5_042523_0143.root, FC#1, port C1
Entries 768
Mean 44.03
Std Dev 11.7
Turn on : 25.7417
Width : 2.627
Height : 19.930
Entry
ampl
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6
8
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14
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0
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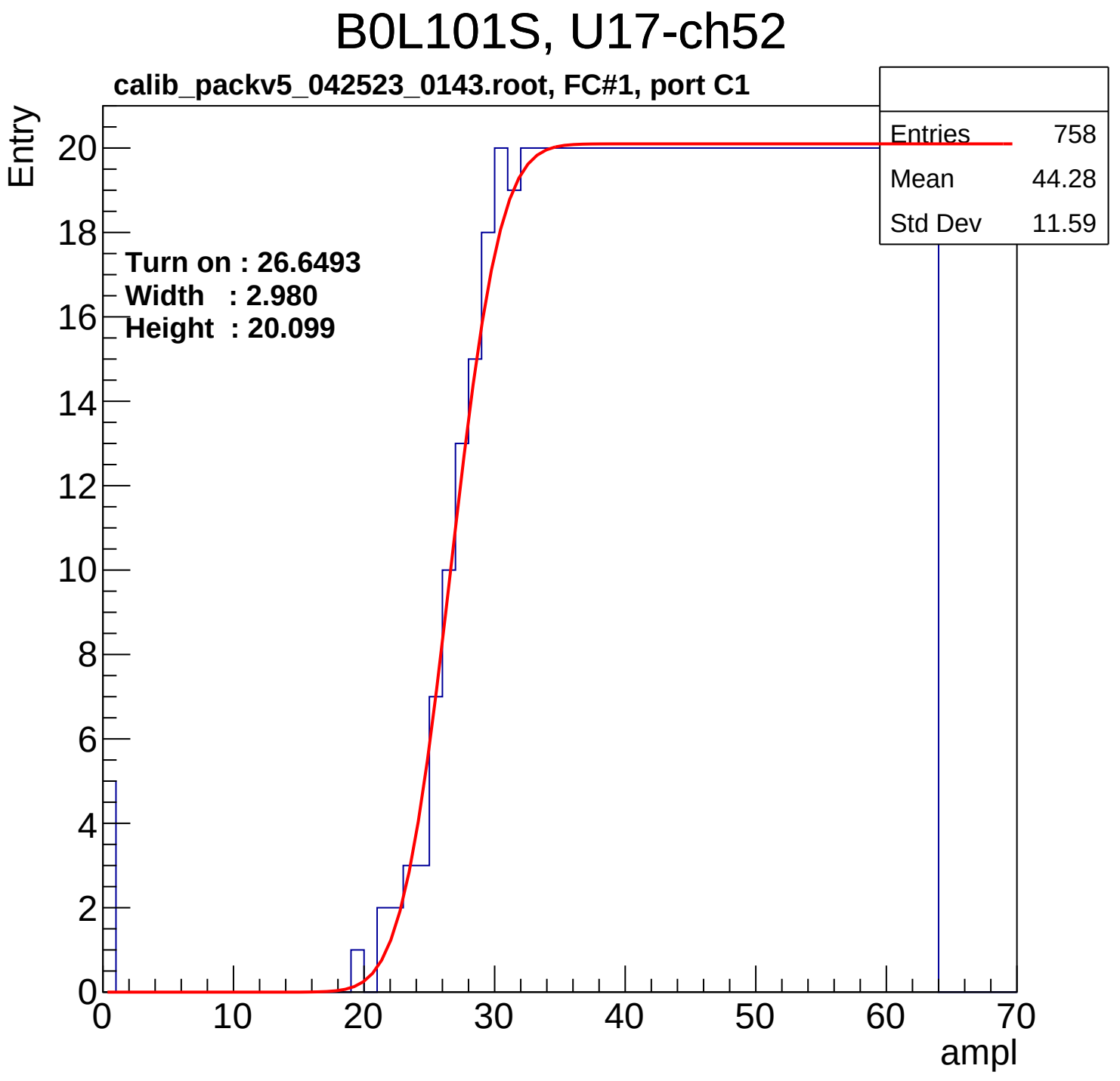
B0L101S, U17-ch52
calib_packv5_042523_0143.root, FC#1, port C1
Entries 758
Mean 44.28
Std Dev 11.59
Turn on : 26.6493
Width : 2.980
Height : 20.099
Entry
ampl
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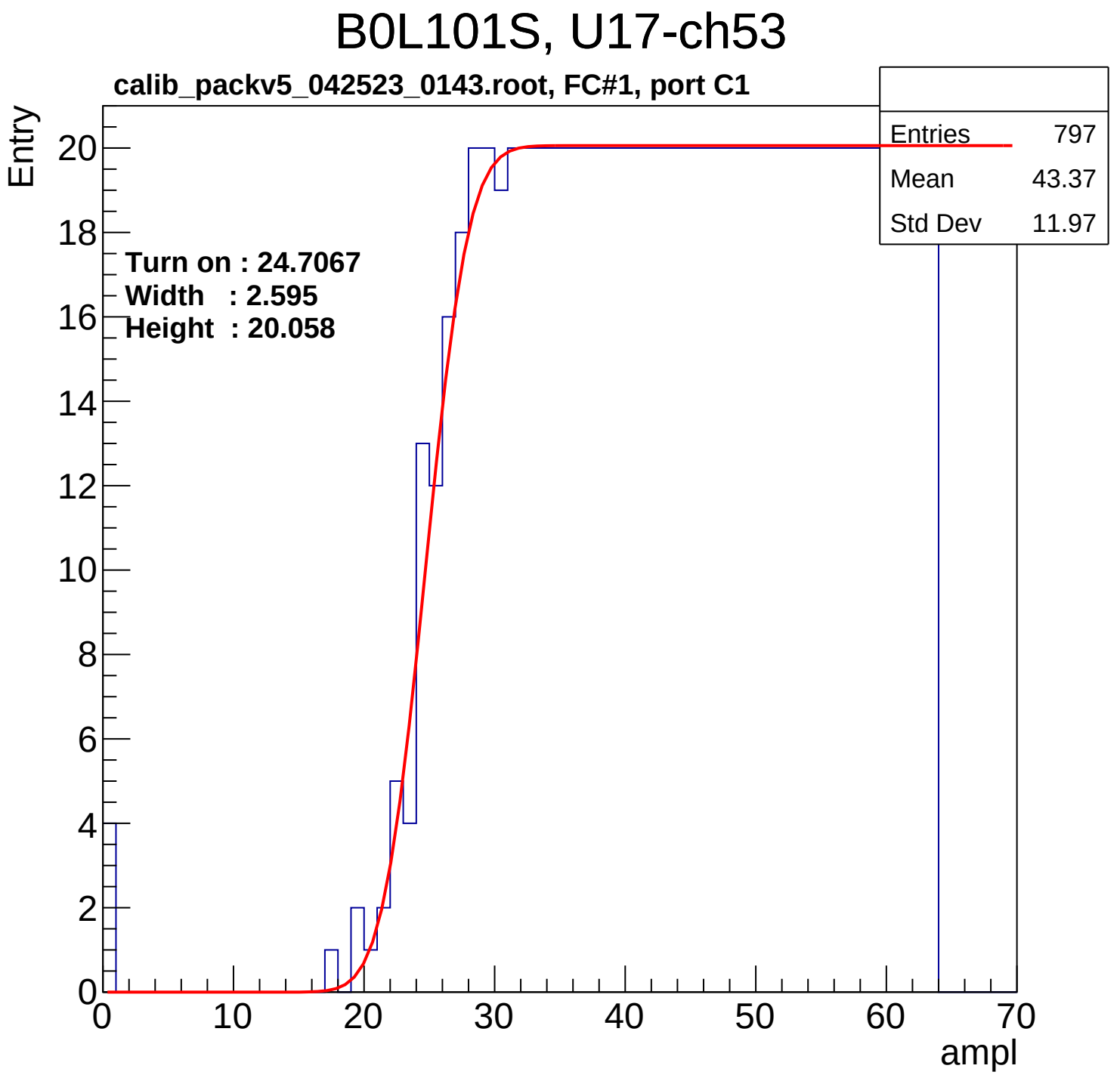
B0L101S, U17-ch53
calib_packv5_042523_0143.root, FC#1, port C1
Entries 797
Mean 43.37
Std Dev 11.97
Turn on : 24.7067
Width : 2.595
Height : 20.058
Entry
ampl
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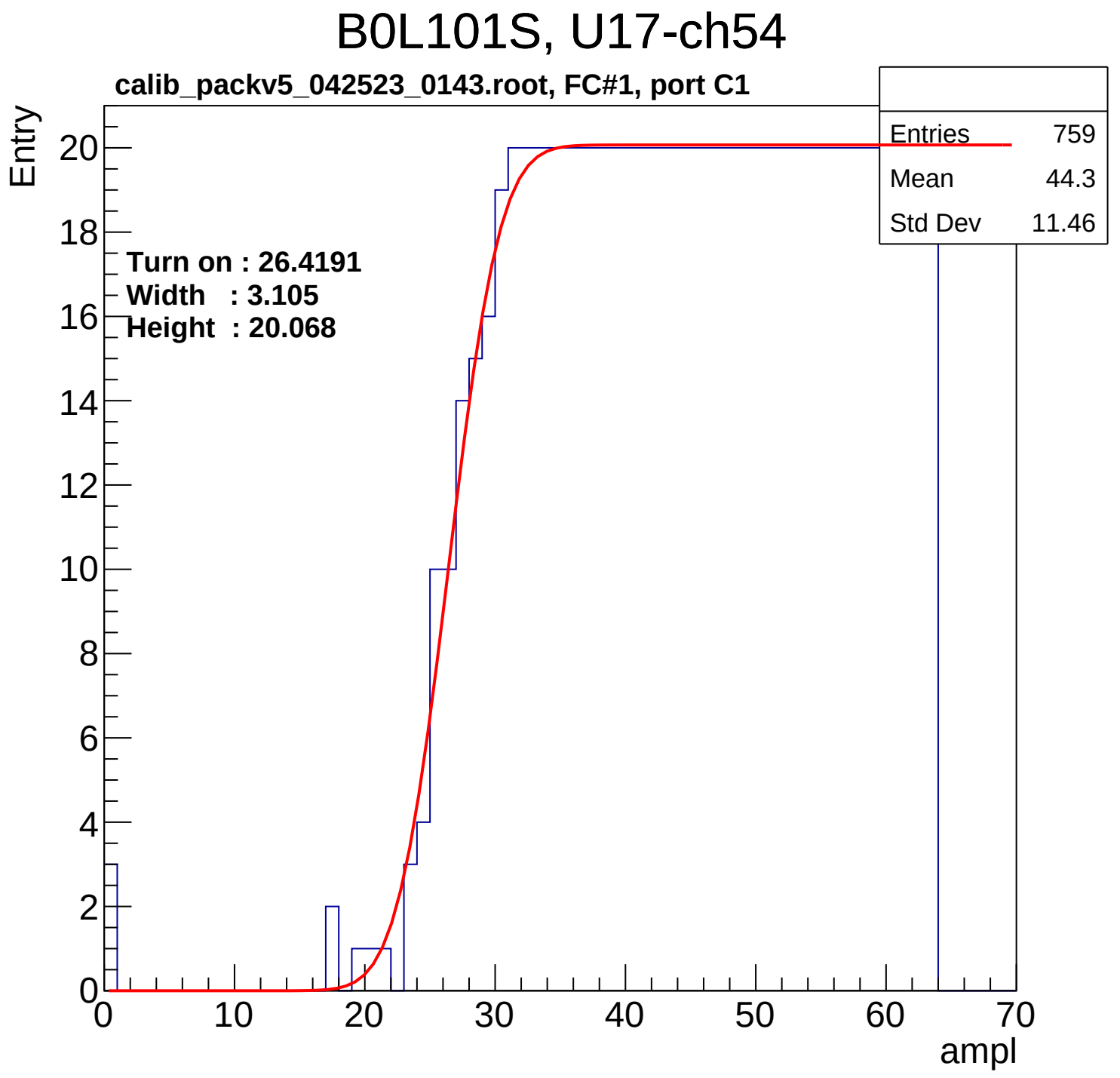
B0L101S, U17-ch54
calib_packv5_042523_0143.root, FC#1, port C1
Entries 759
Mean 44.3
Std Dev 11.46
Turn on : 26.4191
Width : 3.105
Height : 20.068
Entry
ampl
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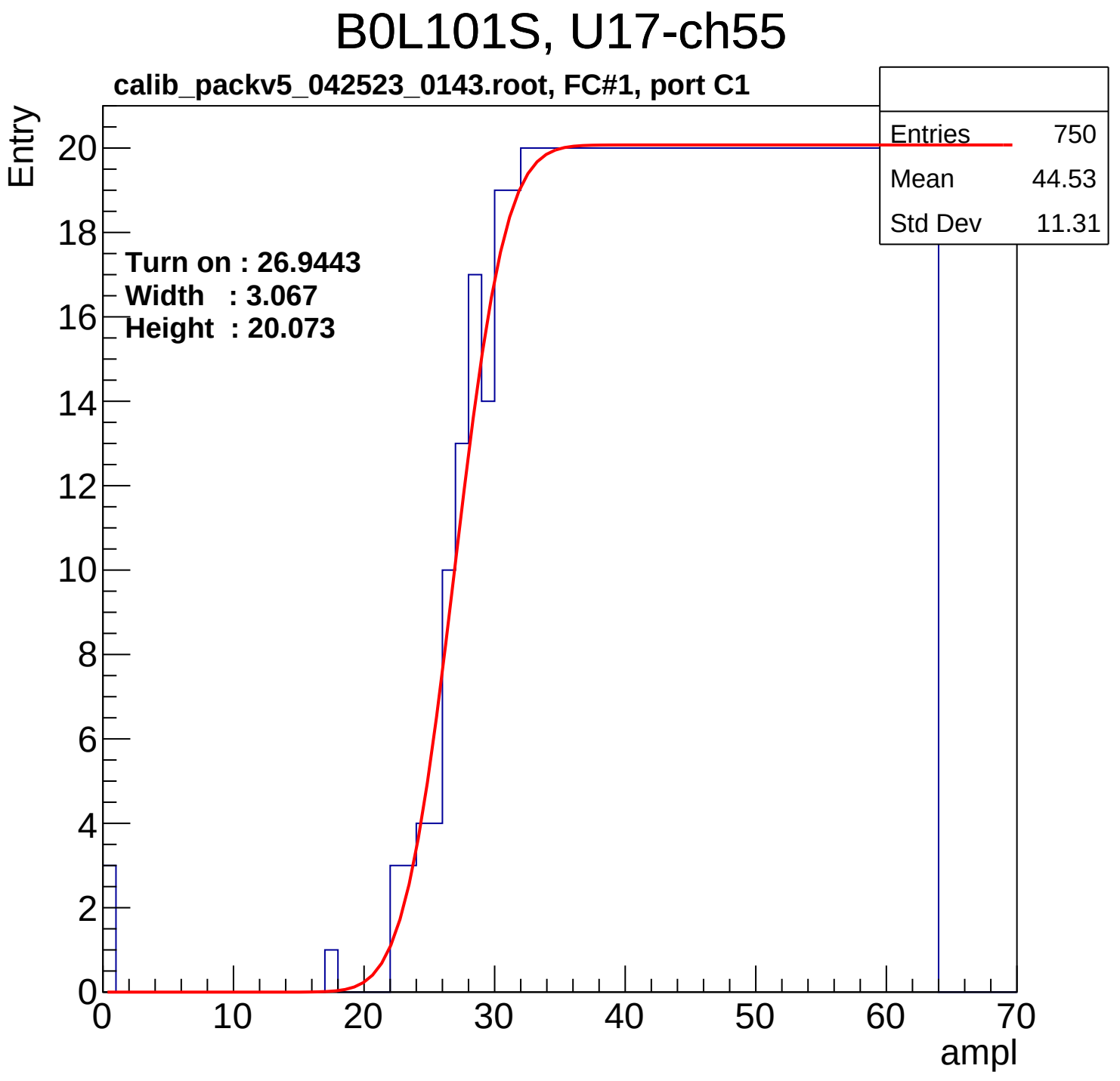
B0L101S, U17-ch55
calib_packv5_042523_0143.root, FC#1, port C1
Entries 750
Mean 44.53
Std Dev 11.31
Turn on : 26.9443
Width : 3.067
Height : 20.073
Entry
ampl
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2
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6
8
10
12
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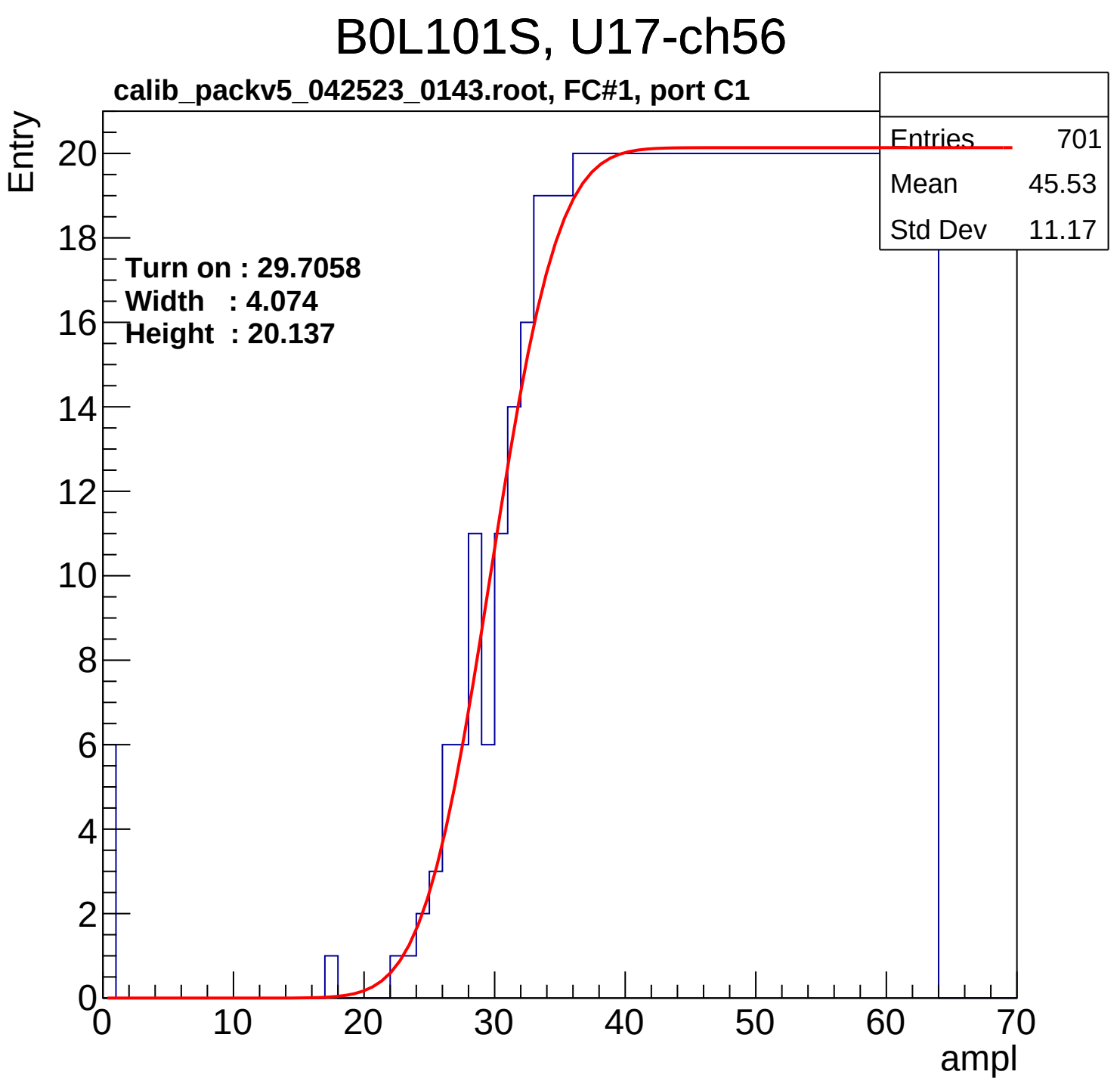
B0L101S, U17-ch56
calib_packv5_042523_0143.root, FC#1, port C1
Entries 701
Mean 45.53
Std Dev 11.17
Turn on : 29.7058
Width : 4.074
Height : 20.137
Entry
ampl
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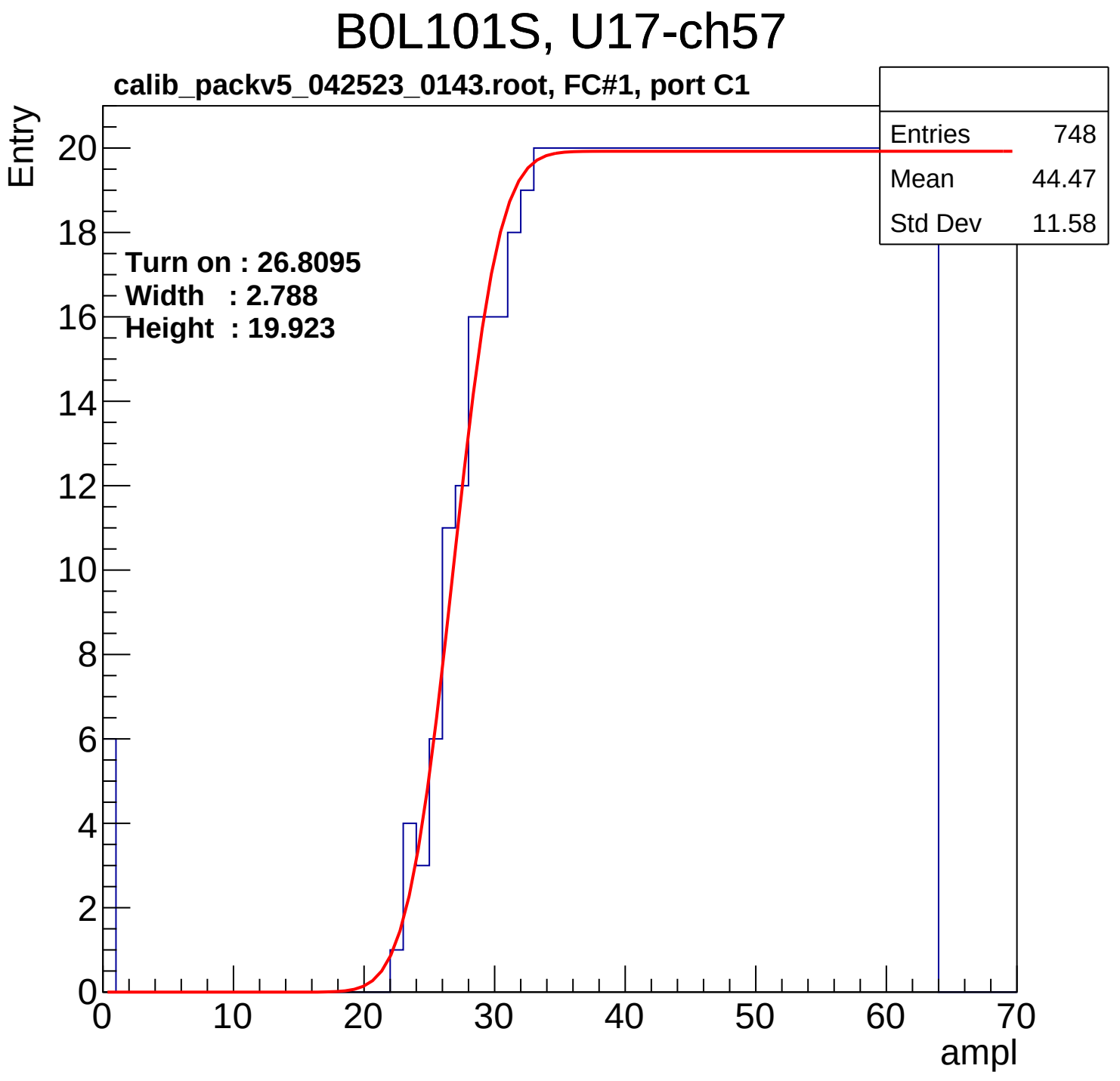
B0L101S, U17-ch57
calib_packv5_042523_0143.root, FC#1, port C1
Entries 748
Mean 44.47
Std Dev 11.58
Turn on : 26.8095
Width : 2.788
Height : 19.923
Entry
ampl
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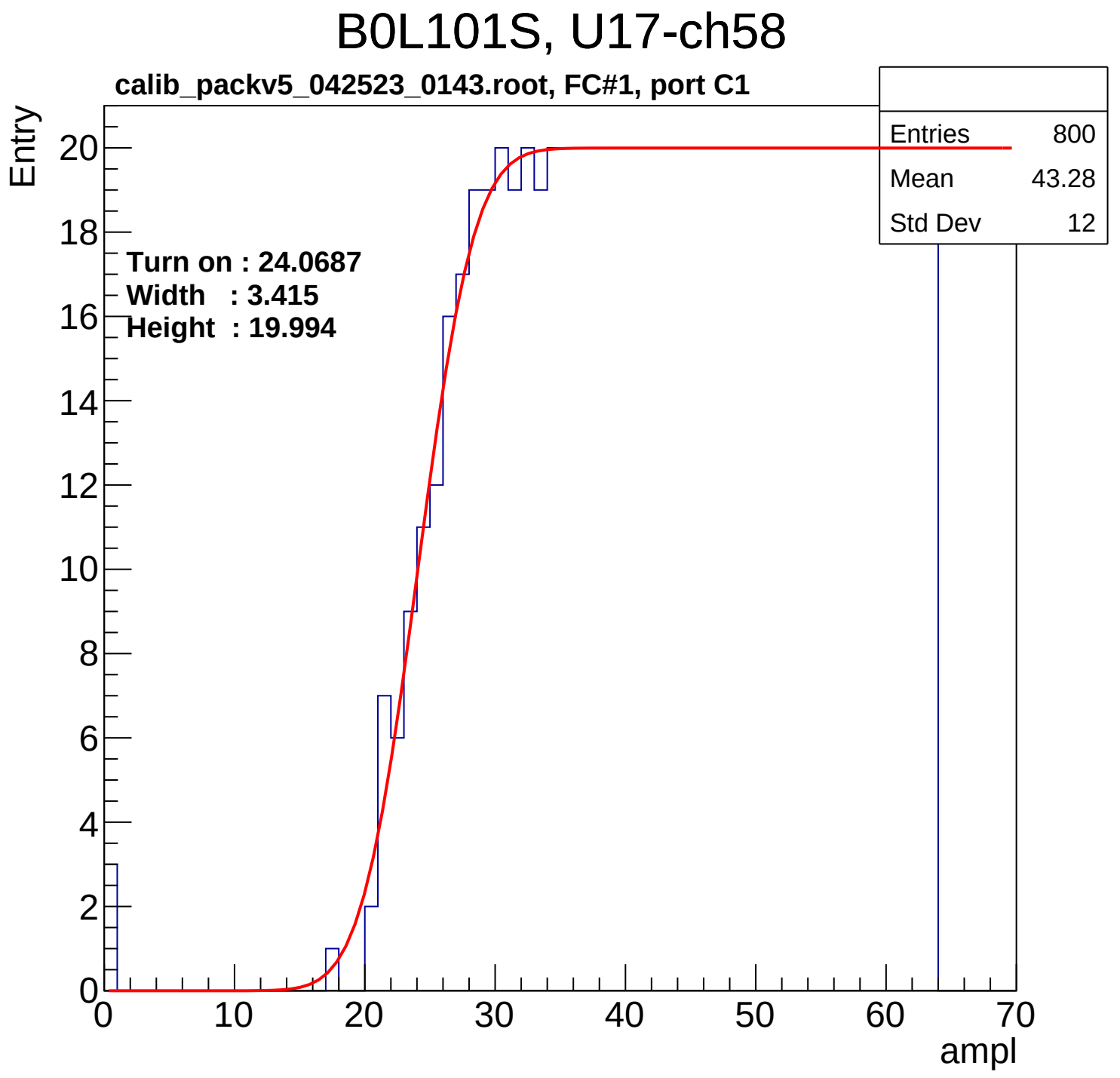
B0L101S, U17-ch58
calib_packv5_042523_0143.root, FC#1, port C1
Entries 800
Mean 43.28
Std Dev 12
Turn on : 24.0687
Width : 3.415
Height : 19.994
Entry
ampl
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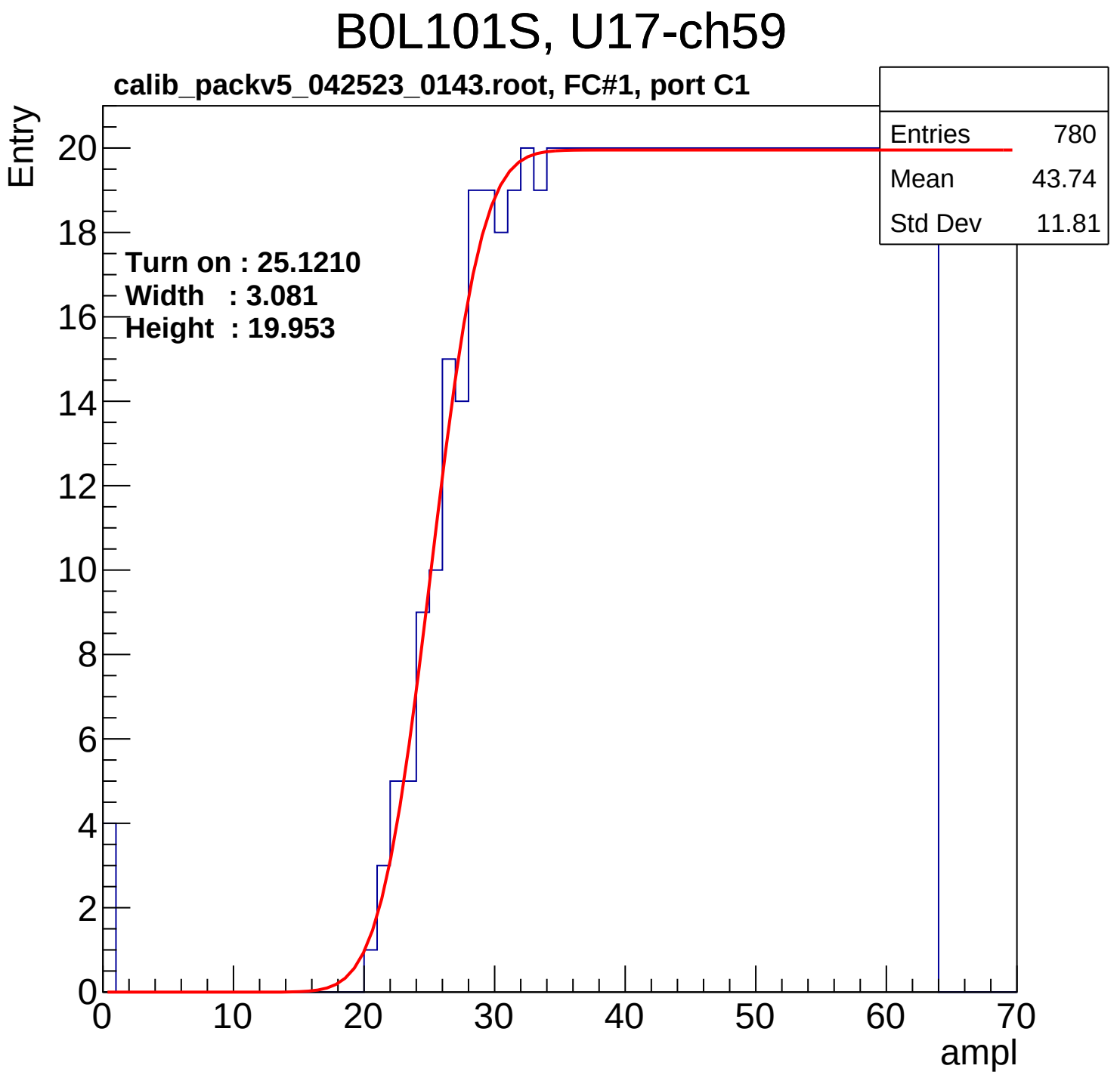
B0L101S, U17-ch59
calib_packv5_042523_0143.root, FC#1, port C1
Entries 780
Mean 43.74
Std Dev 11.81
Turn on : 25.1210
Width : 3.081
Height : 19.953
Entry
ampl
0
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6
8
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12
14
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0
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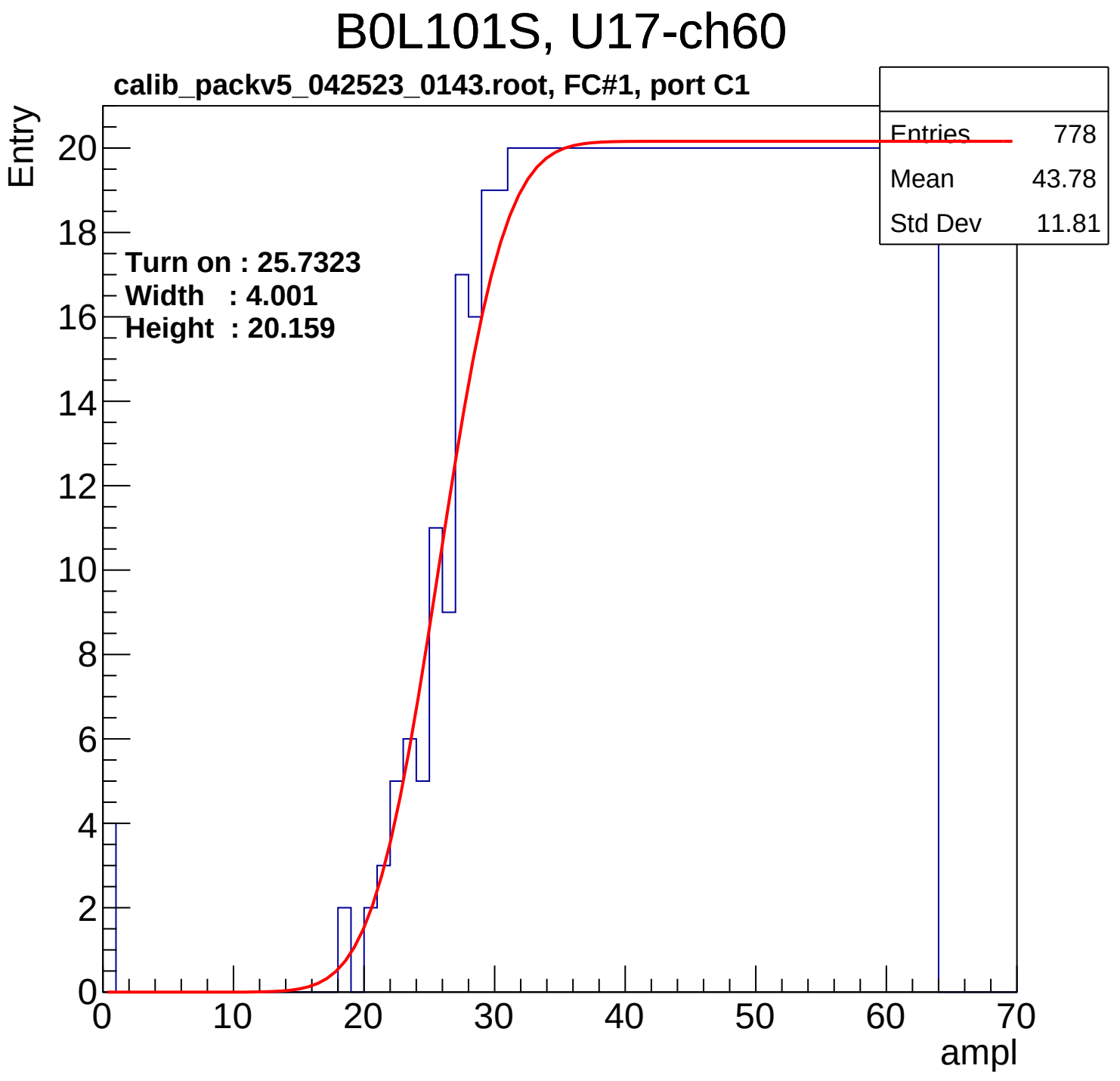
B0L101S, U17-ch60
calib_packv5_042523_0143.root, FC#1, port C1
Entries 778
Mean 43.78
Std Dev 11.81
Turn on : 25.7323
Width : 4.001
Height : 20.159
Entry
ampl
0
2
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6
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14
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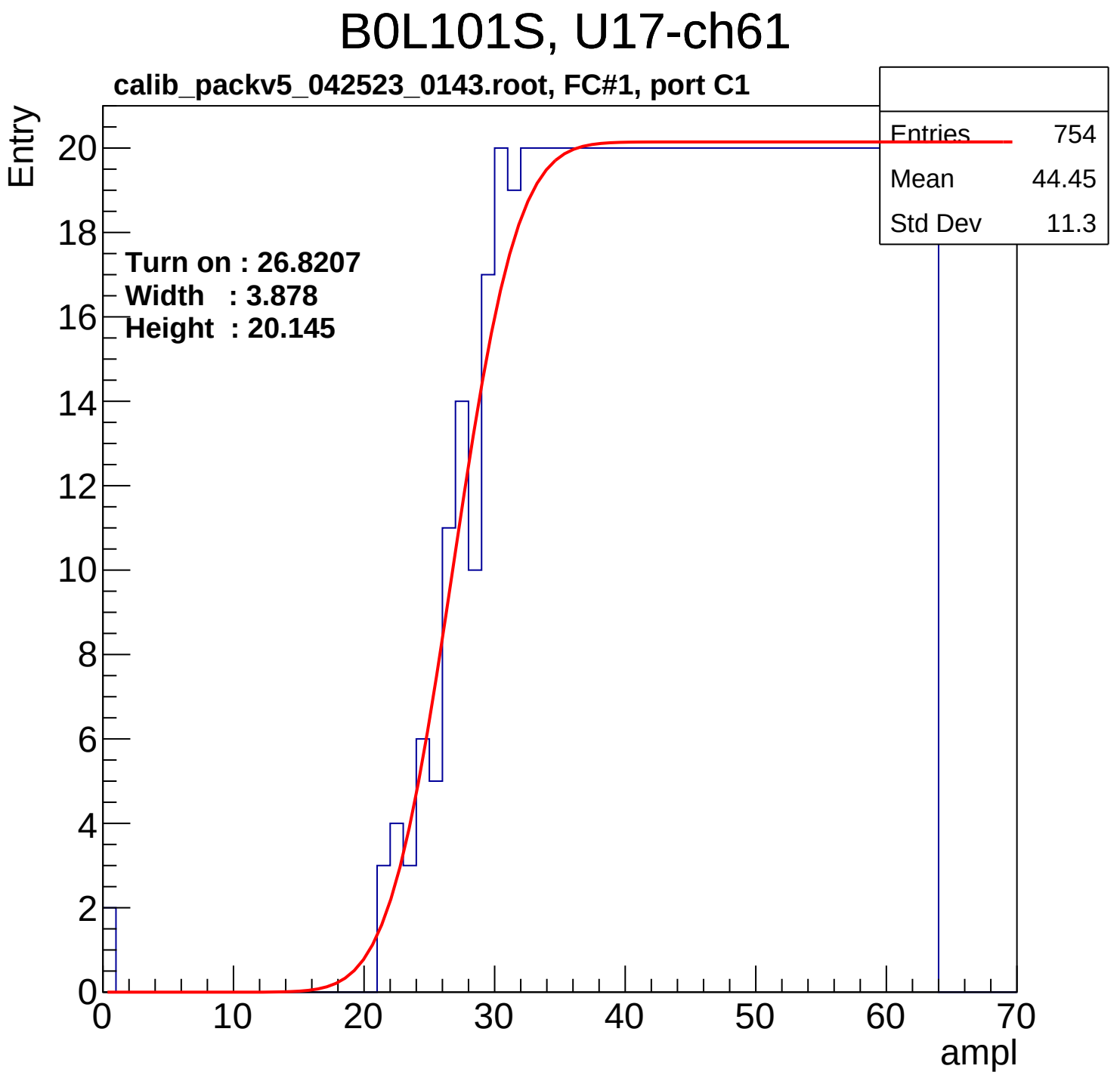
B0L101S, U17-ch61
calib_packv5_042523_0143.root, FC#1, port C1
Entries 754
Mean 44.45
Std Dev 11.3
Turn on : 26.8207
Width : 3.878
Height : 20.145
Entry
ampl
0
2
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6
8
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12
14
16
18
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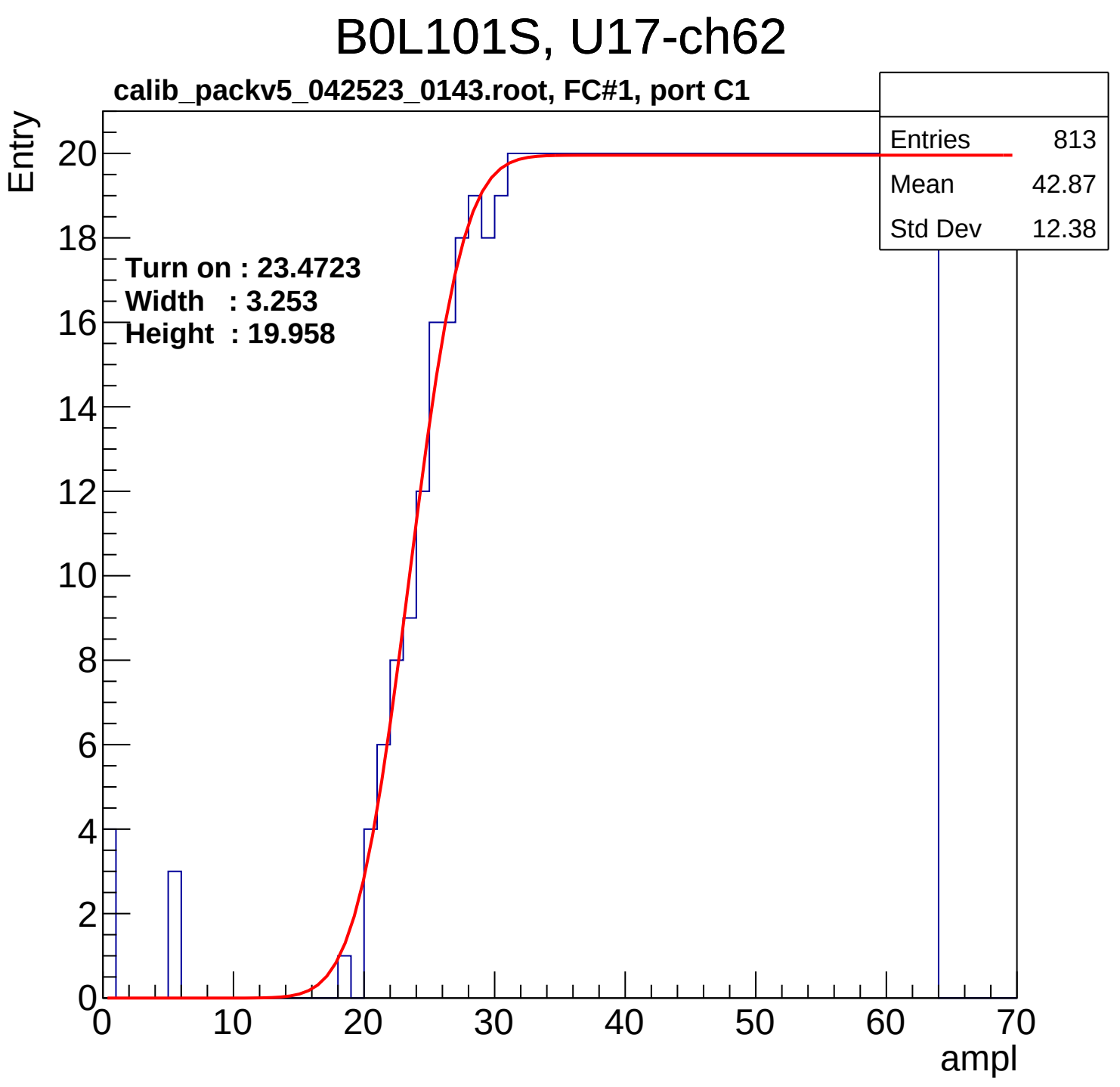
B0L101S, U17-ch62
calib_packv5_042523_0143.root, FC#1, port C1
Entries 813
Mean 42.87
Std Dev 12.38
Turn on : 23.4723
Width : 3.253
Height : 19.958
Entry
ampl
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8
10
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14
16
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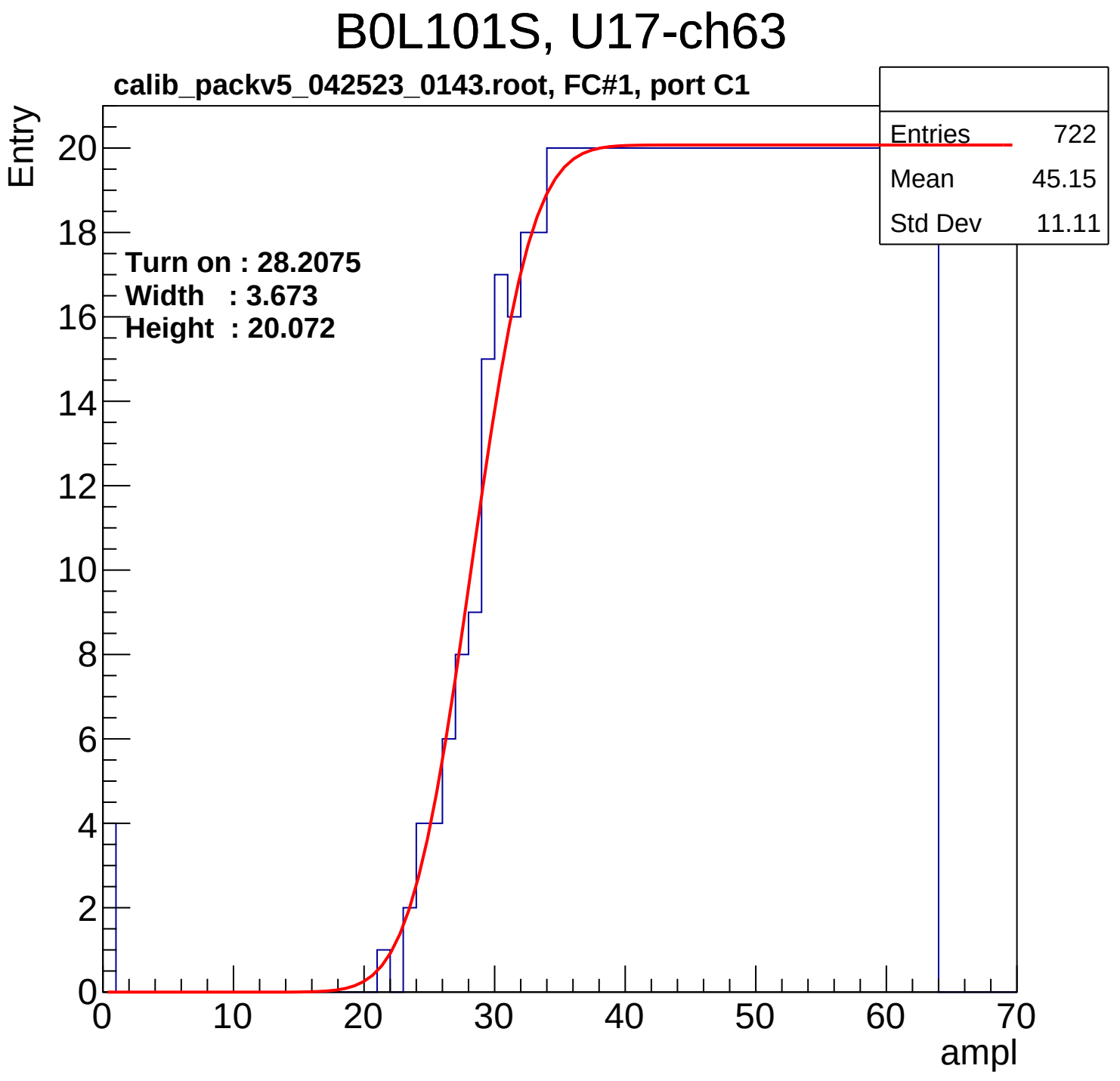
B0L101S, U17-ch63
calib_packv5_042523_0143.root, FC#1, port C1
Entries 722
Mean 45.15
Std Dev 11.11
Turn on : 28.2075
Width : 3.673
Height : 20.072
Entry
ampl
0
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6
8
10
12
14
16
18
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0
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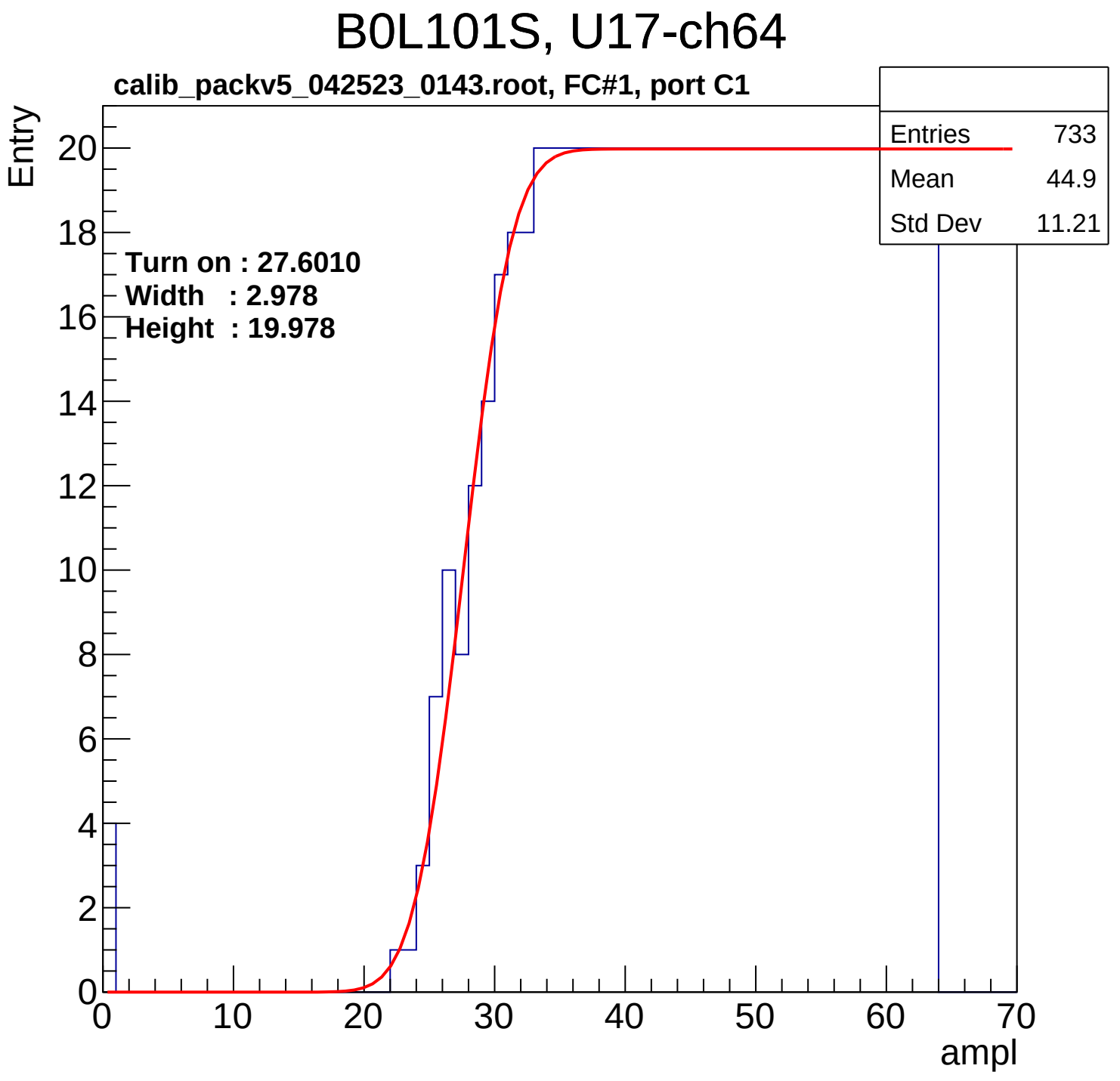
B0L101S, U17-ch64
calib_packv5_042523_0143.root, FC#1, port C1
Entries 733
Mean 44.9
Std Dev 11.21
Turn on : 27.6010
Width : 2.978
Height : 19.978
Entry
ampl
0
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6
8
10
12
14
16
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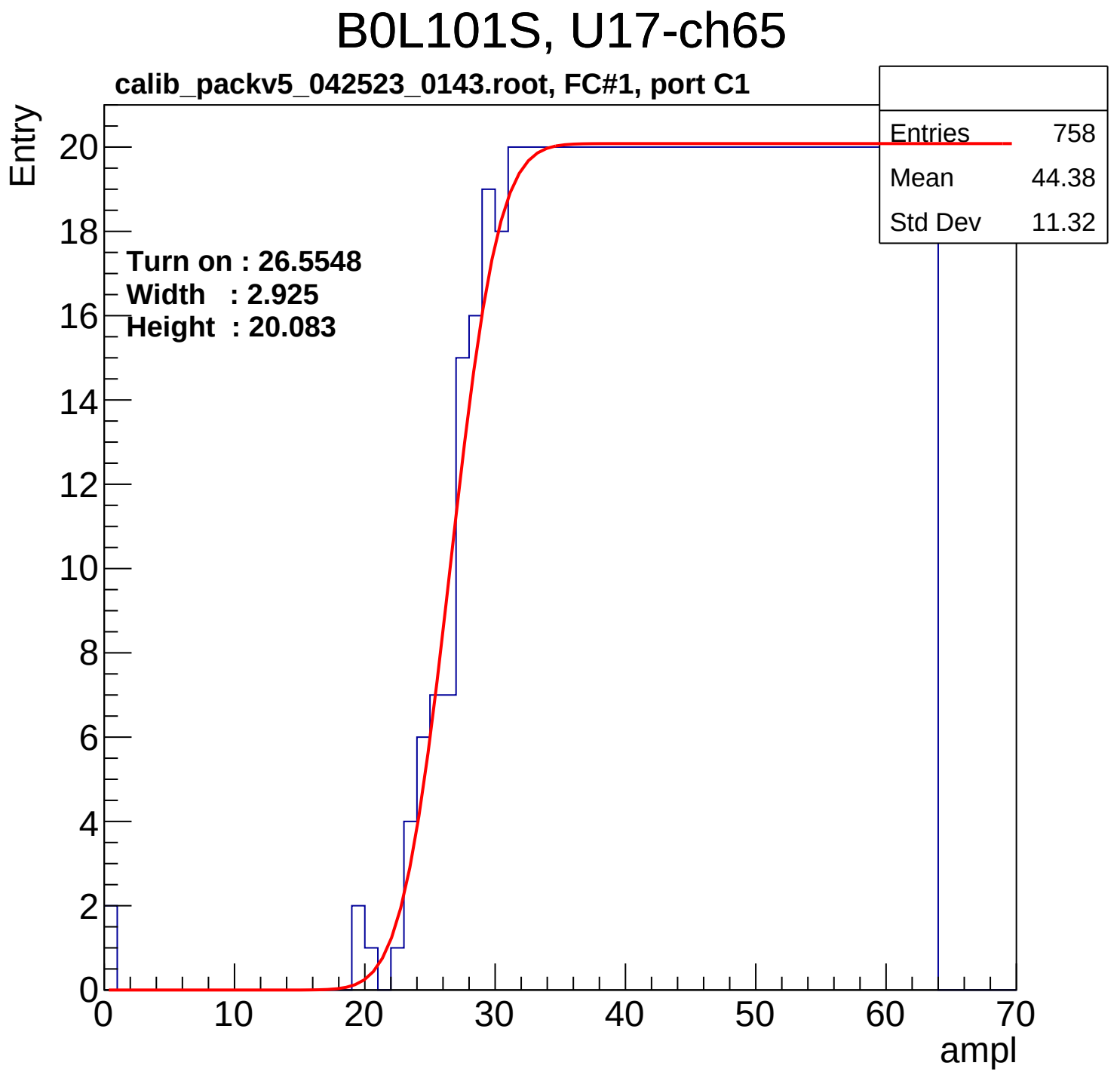
B0L101S, U17-ch65
calib_packv5_042523_0143.root, FC#1, port C1
Entries 758
Mean 44.38
Std Dev 11.32
Turn on : 26.5548
Width : 2.925
Height : 20.083
Entry
ampl
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6
8
10
12
14
16
18
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0
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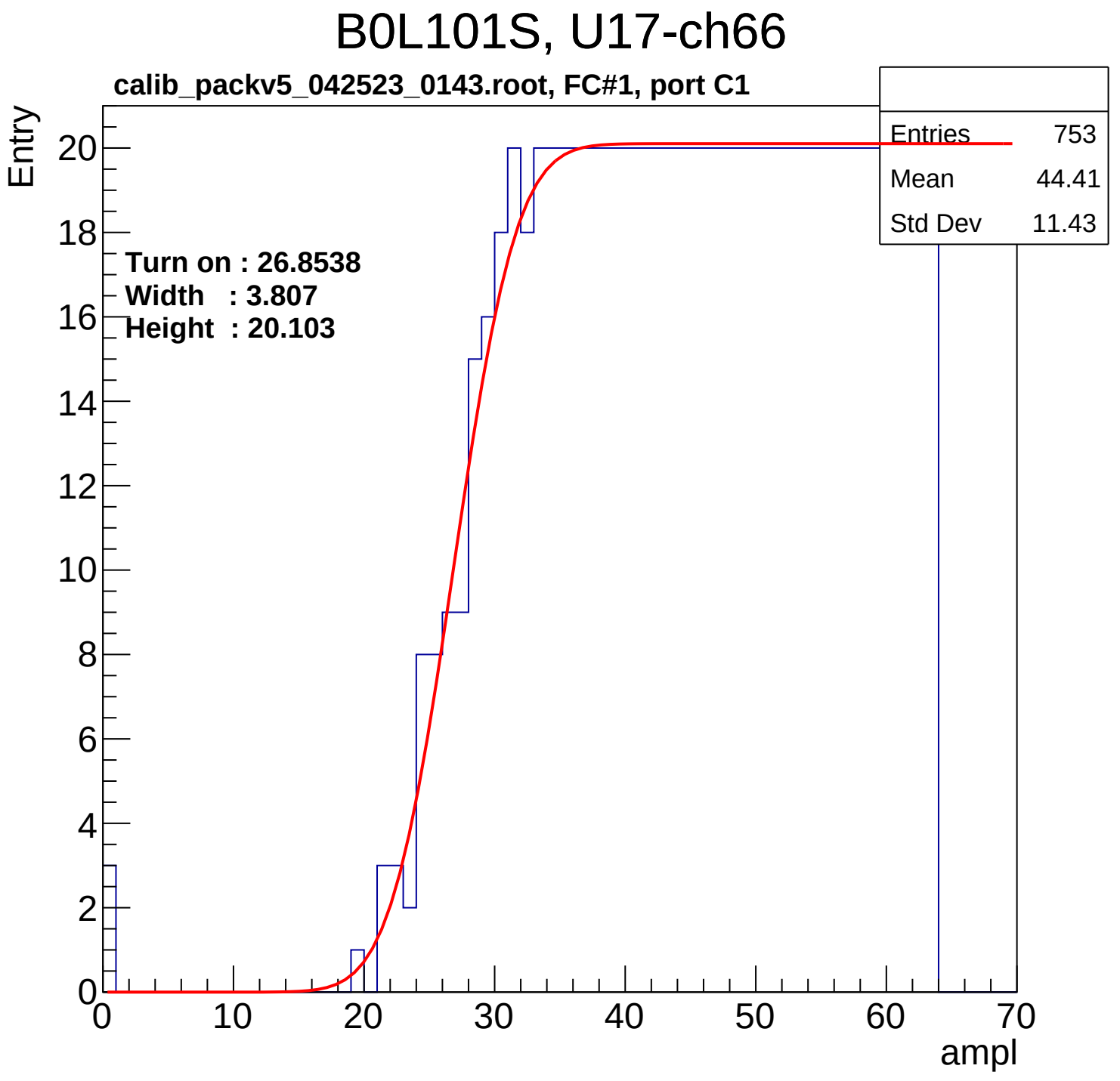
B0L101S, U17-ch66
calib_packv5_042523_0143.root, FC#1, port C1
Entries 753
Mean 44.41
Std Dev 11.43
Turn on : 26.8538
Width : 3.807
Height : 20.103
Entry
ampl
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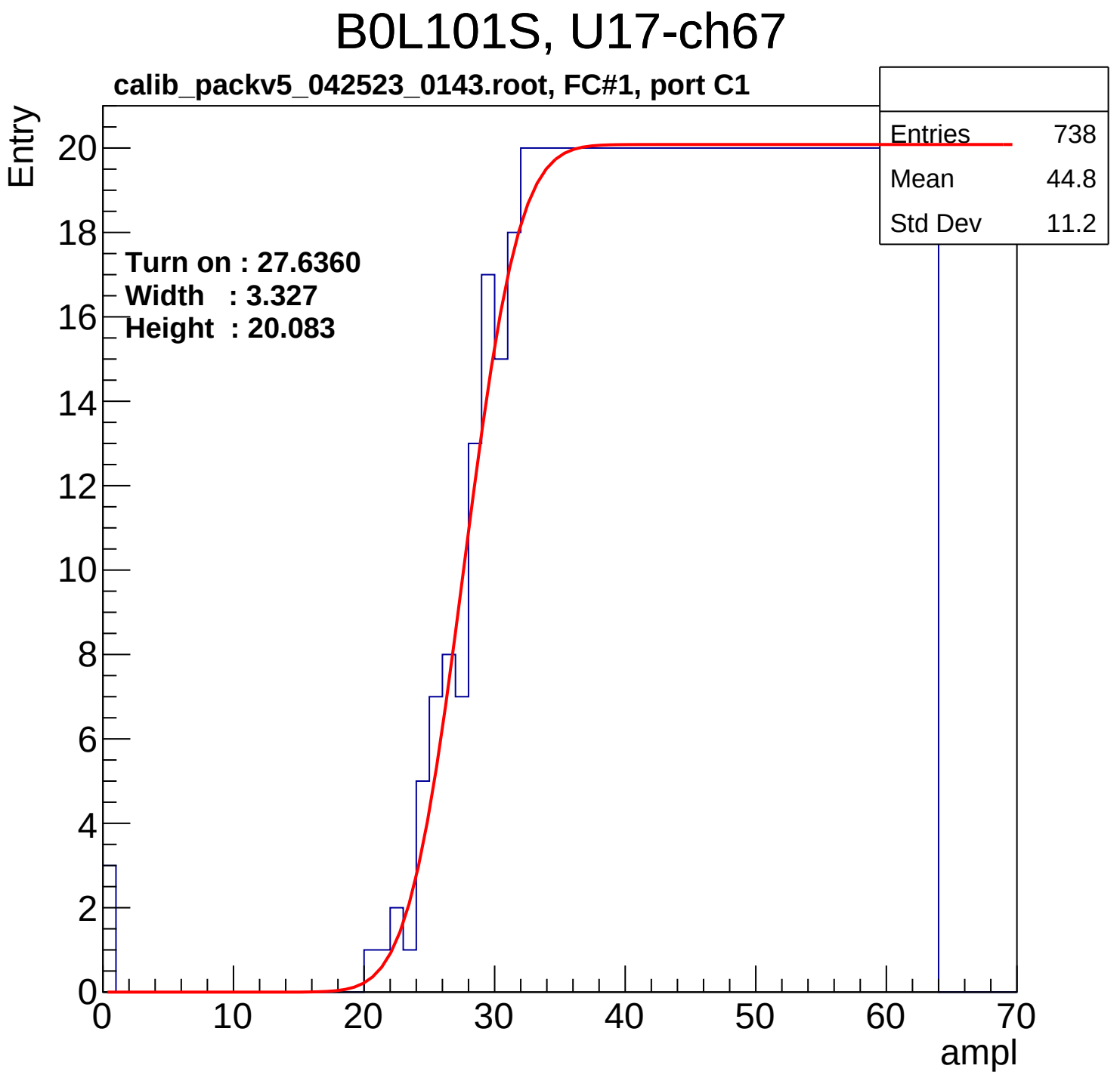
B0L101S, U17-ch67
calib_packv5_042523_0143.root, FC#1, port C1
Entries 738
Mean 44.8
Std Dev 11.2
Turn on : 27.6360
Width : 3.327
Height : 20.083
Entry
ampl
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12
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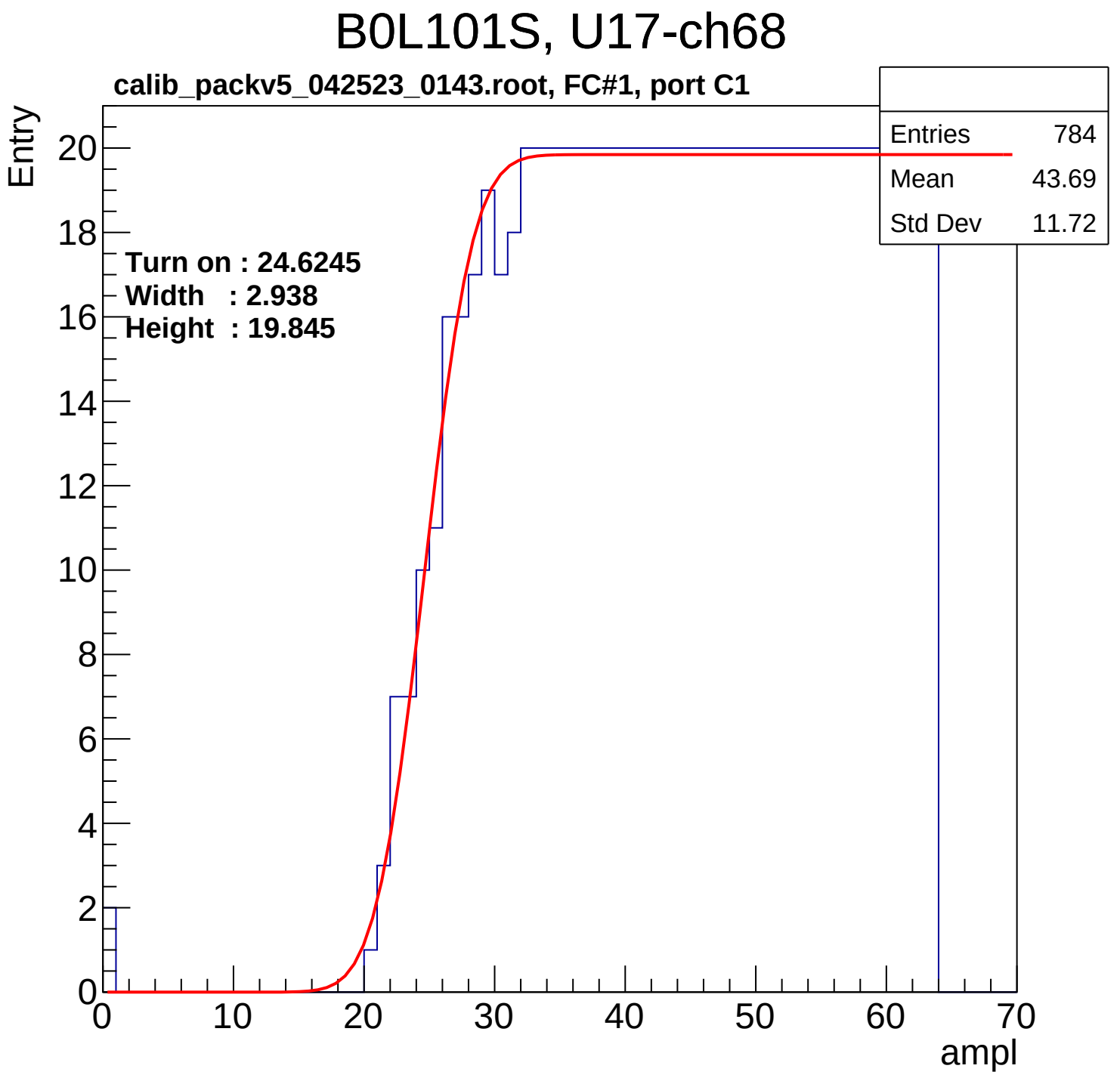
B0L101S, U17-ch68
calib_packv5_042523_0143.root, FC#1, port C1
Entries 784
Mean 43.69
Std Dev 11.72
Turn on : 24.6245
Width : 2.938
Height : 19.845
Entry
ampl
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6
8
10
12
14
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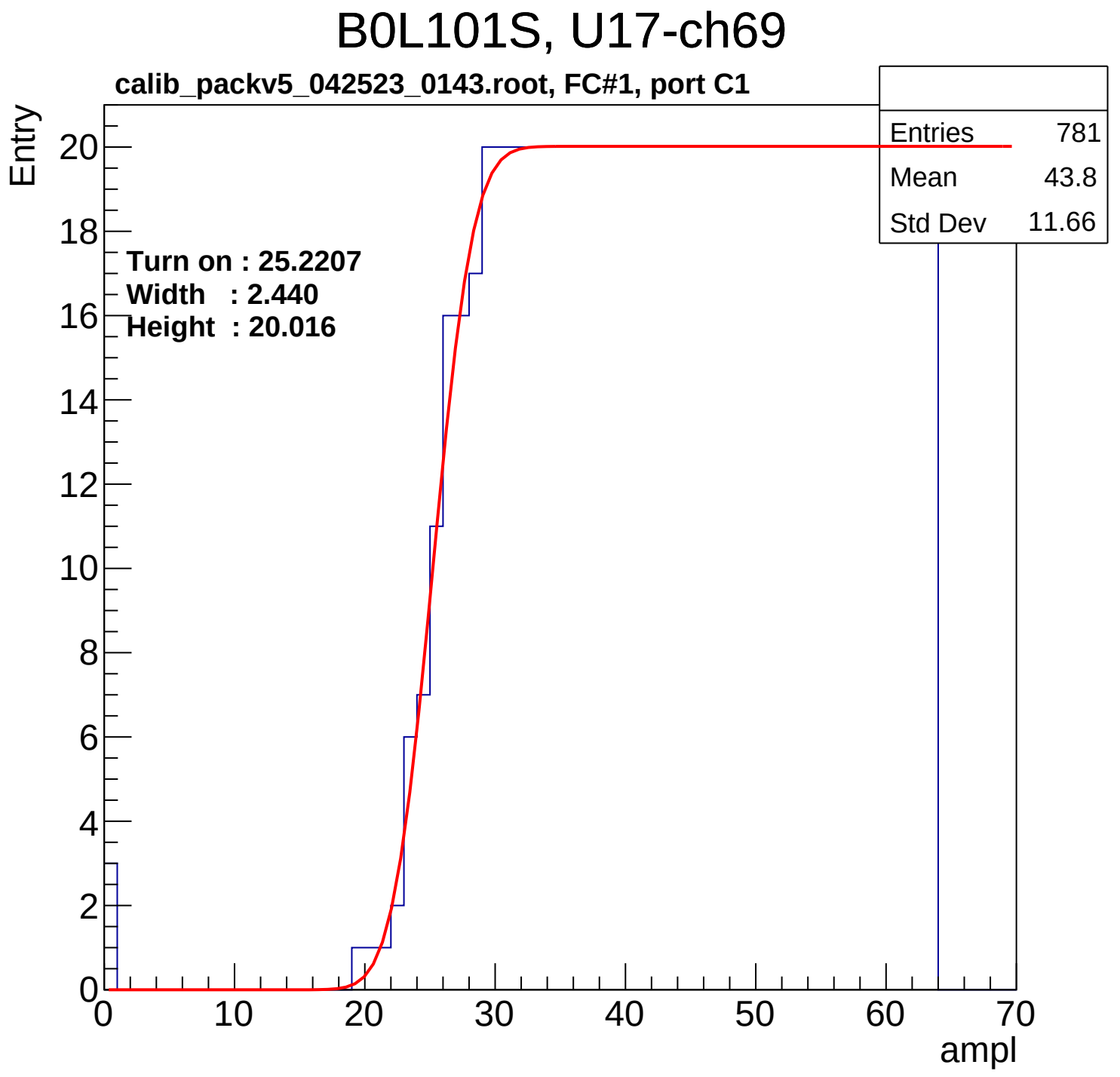
B0L101S, U17-ch69
calib_packv5_042523_0143.root, FC#1, port C1
Entries 781
Mean 43.8
Std Dev 11.66
Turn on : 25.2207
Width : 2.440
Height : 20.016
Entry
ampl
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6
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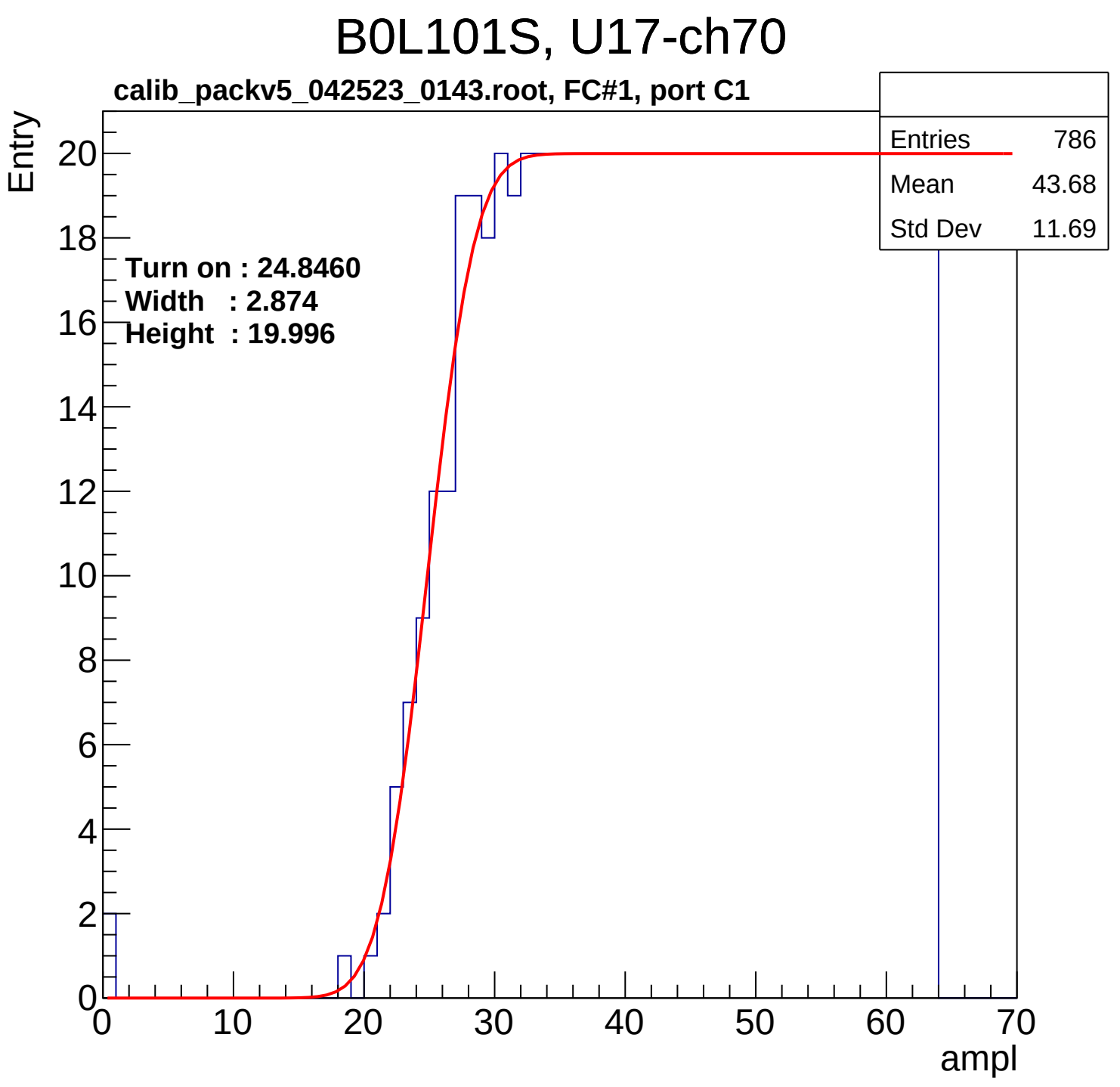
B0L101S, U17-ch70
calib_packv5_042523_0143.root, FC#1, port C1
Entries 786
Mean 43.68
Std Dev 11.69
Turn on : 24.8460
Width : 2.874
Height : 19.996
Entry
ampl
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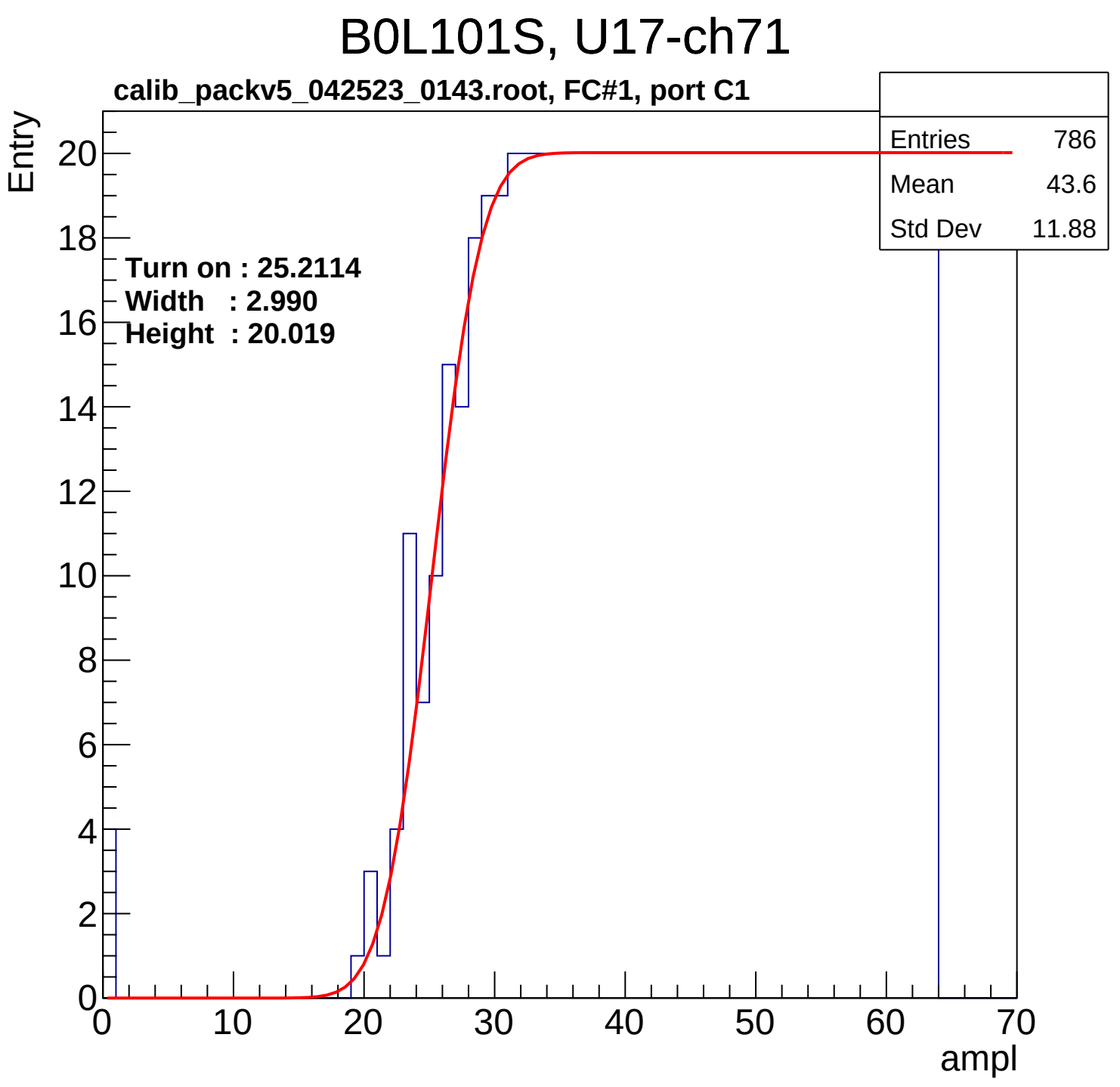
B0L101S, U17-ch71
calib_packv5_042523_0143.root, FC#1, port C1
Entries 786
Mean 43.6
Std Dev 11.88
Turn on : 25.2114
Width : 2.990
Height : 20.019
Entry
ampl
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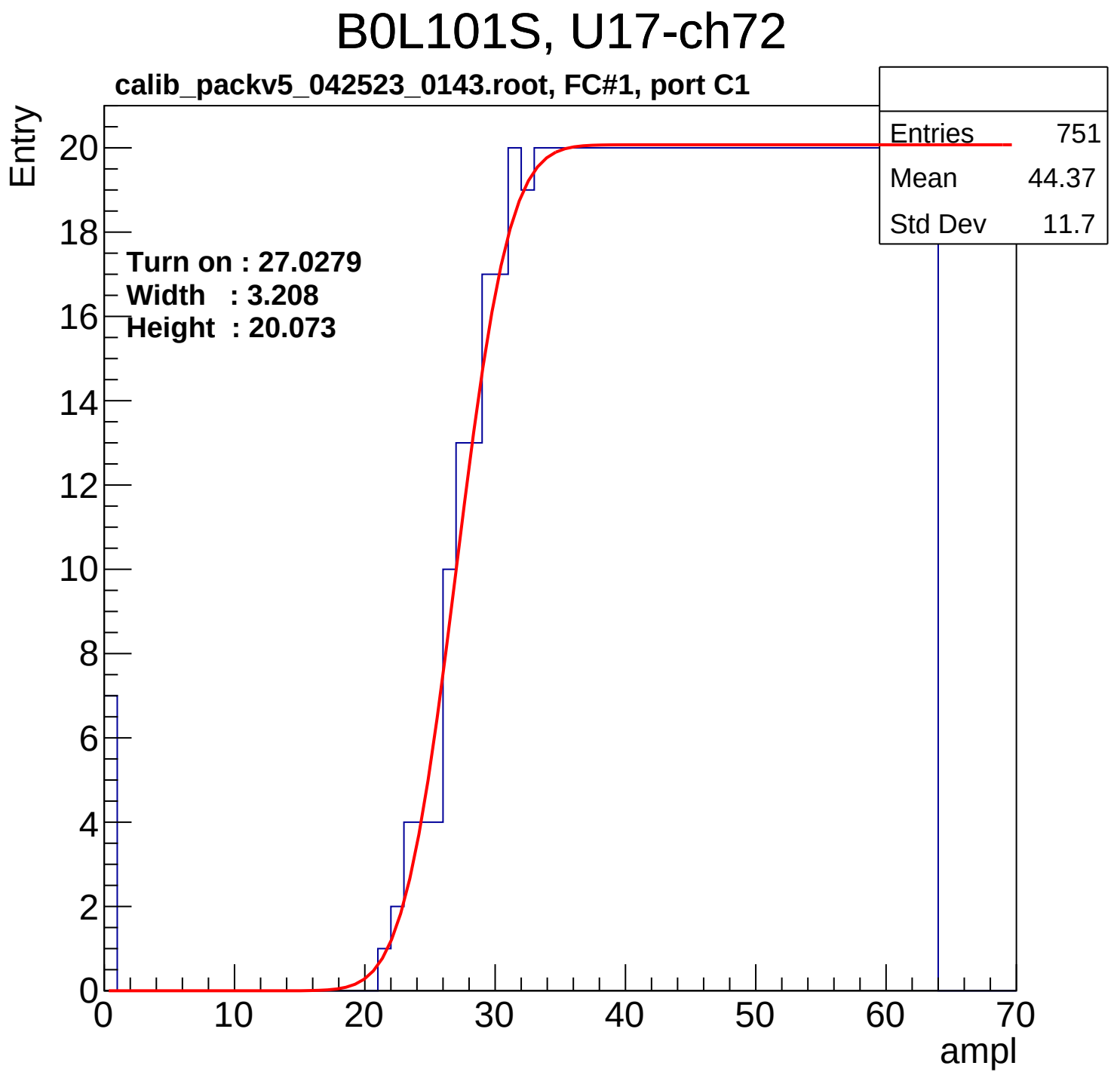
B0L101S, U17-ch72
calib_packv5_042523_0143.root, FC#1, port C1
Entries 751
Mean 44.37
Std Dev 11.7
Turn on : 27.0279
Width : 3.208
Height : 20.073
Entry
ampl
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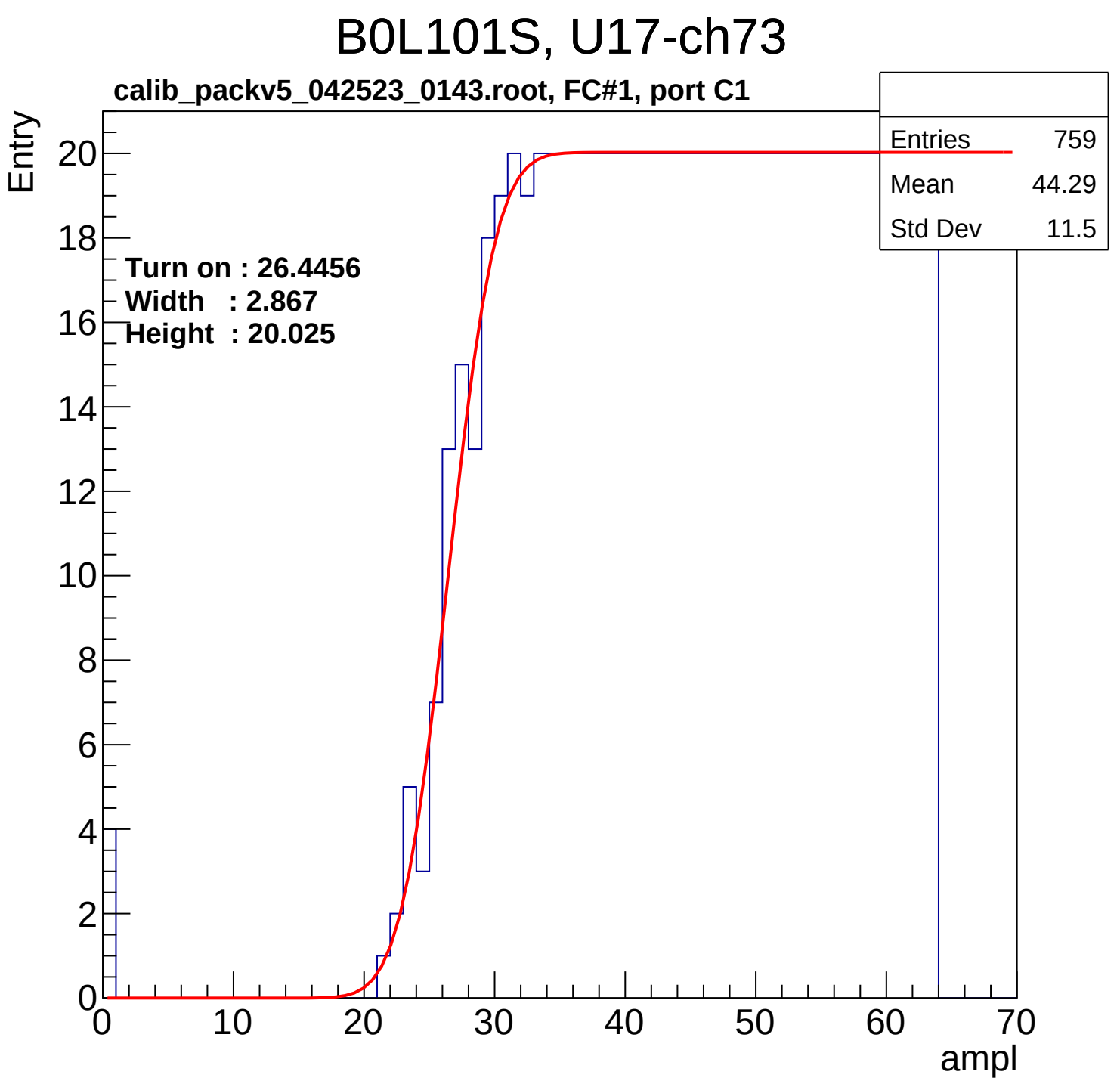
B0L101S, U17-ch73
calib_packv5_042523_0143.root, FC#1, port C1
Entries 759
Mean 44.29
Std Dev 11.5
Turn on : 26.4456
Width : 2.867
Height : 20.025
Entry
ampl
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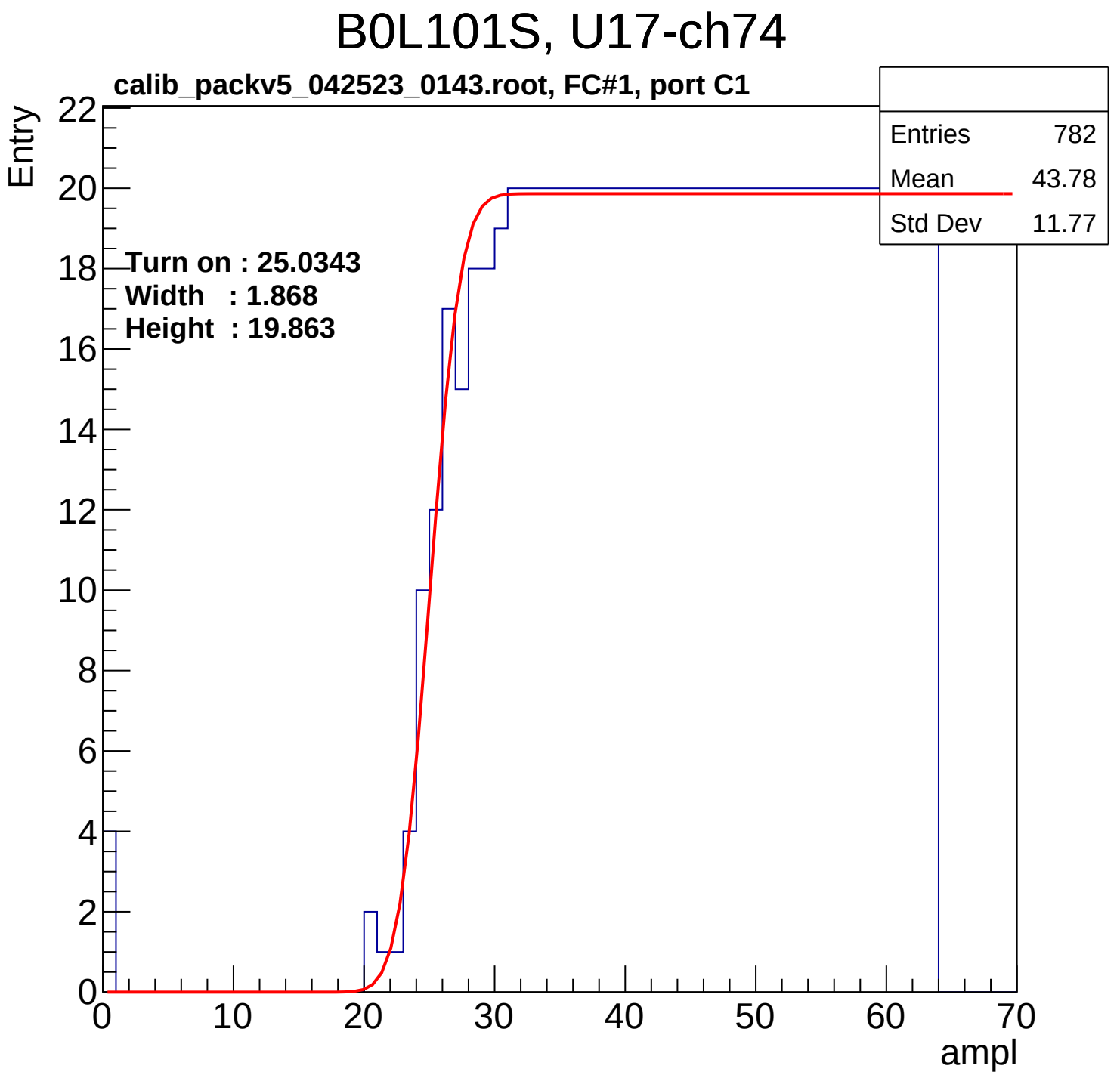
B0L101S, U17-ch74
calib_packv5_042523_0143.root, FC#1, port C1
Entries 782
Mean 43.78
Std Dev 11.77
Turn on : 25.0343
Width : 1.868
Height : 19.863
Entry
ampl
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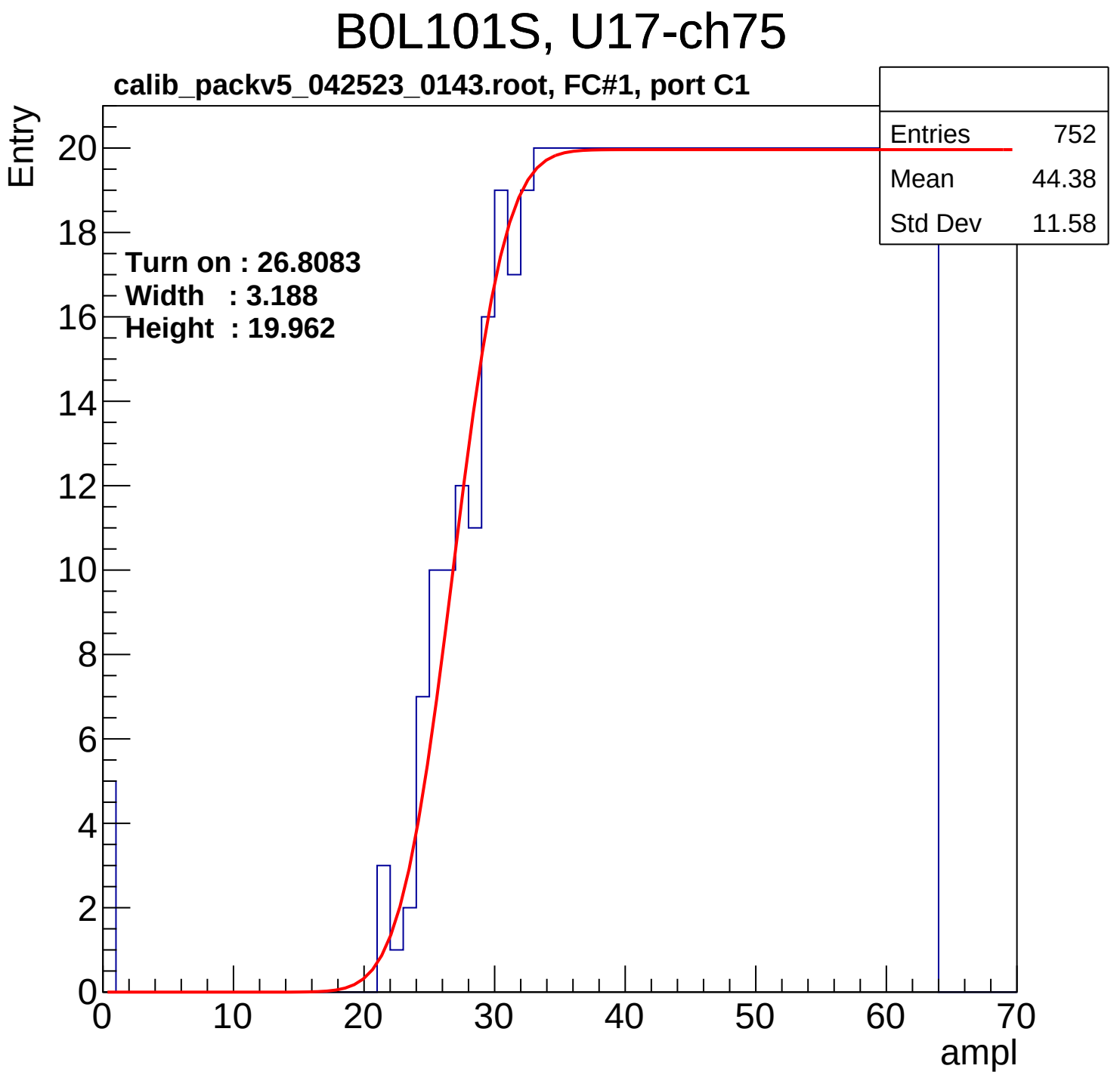
B0L101S, U17-ch75
calib_packv5_042523_0143.root, FC#1, port C1
Entries 752
Mean 44.38
Std Dev 11.58
Turn on : 26.8083
Width : 3.188
Height : 19.962
Entry
ampl
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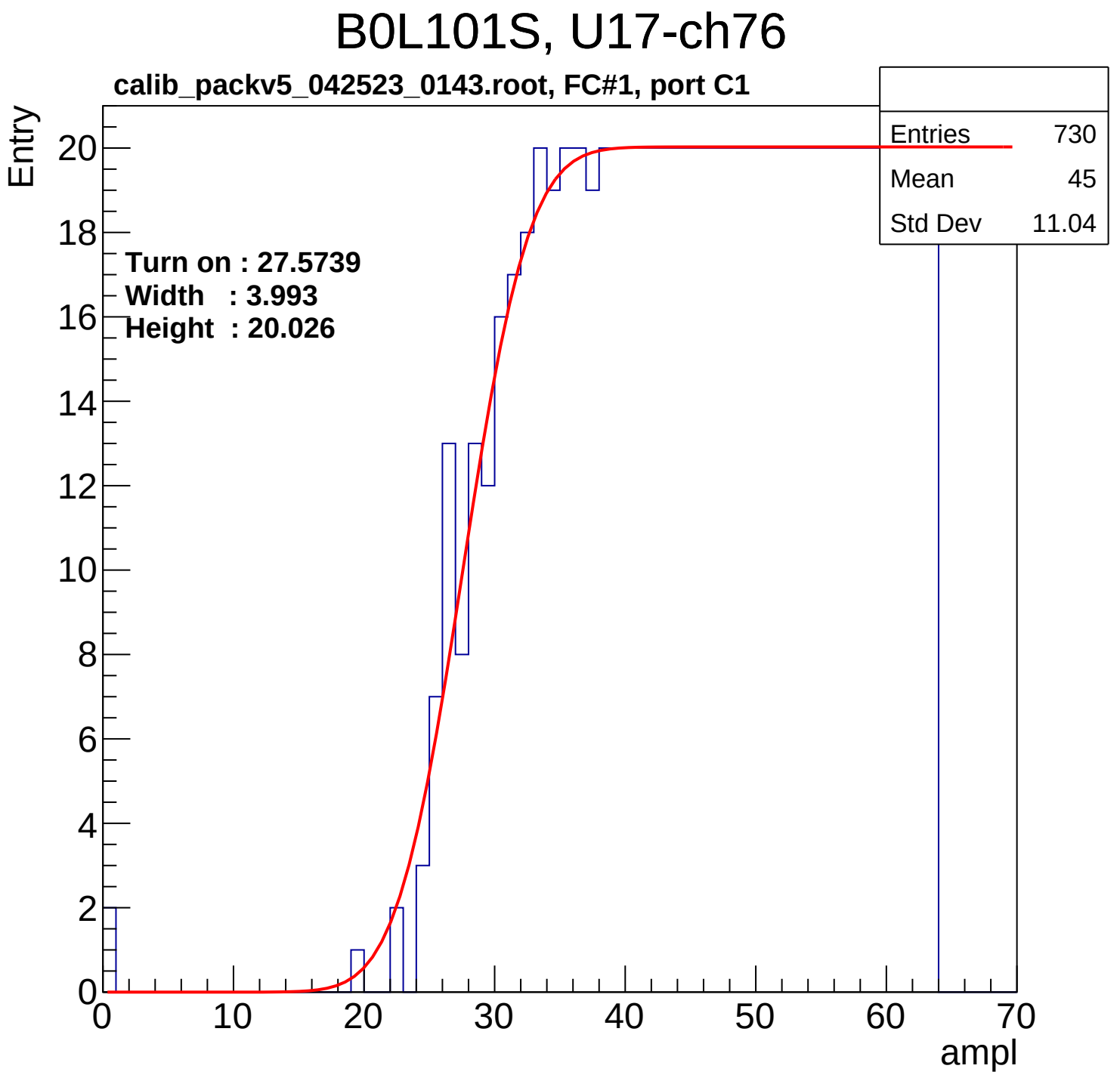
B0L101S, U17-ch76
calib_packv5_042523_0143.root, FC#1, port C1
Entries 730
Mean 45
Std Dev 11.04
Turn on : 27.5739
Width : 3.993
Height : 20.026
Entry
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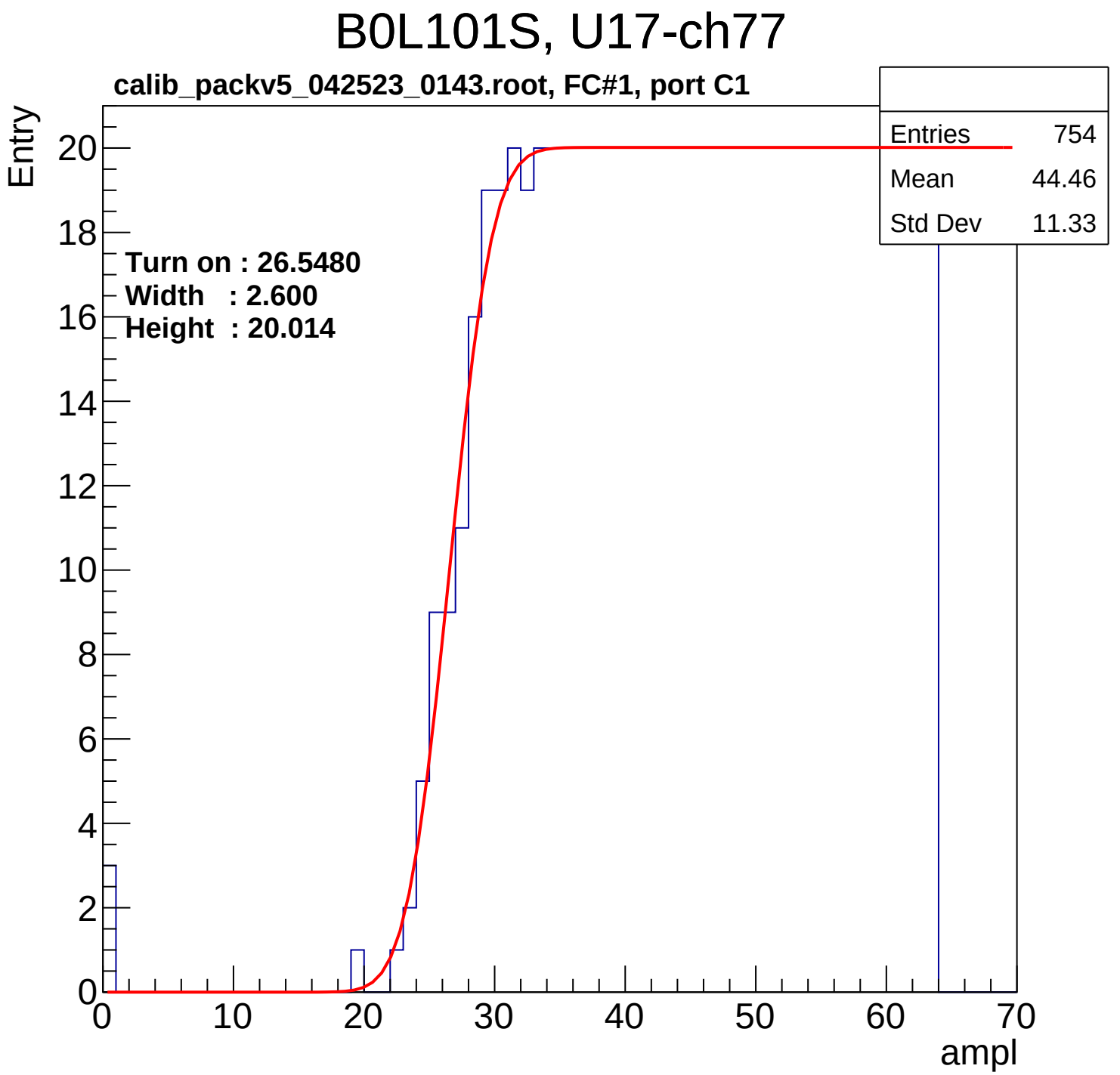
B0L101S, U17-ch77
calib_packv5_042523_0143.root, FC#1, port C1
Entries 754
Mean 44.46
Std Dev 11.33
Turn on : 26.5480
Width : 2.600
Height : 20.014
Entry
ampl
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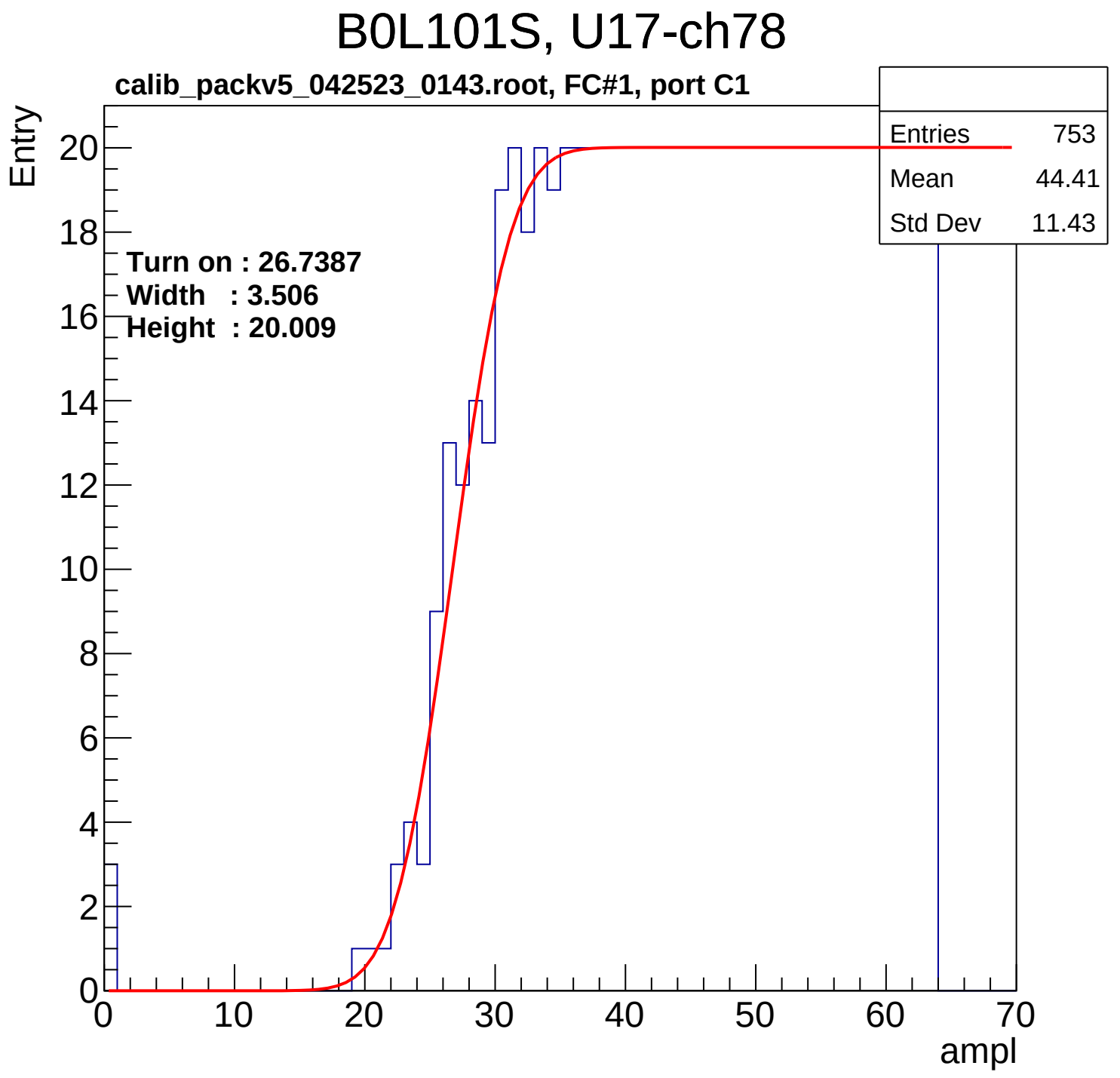
B0L101S, U17-ch78
calib_packv5_042523_0143.root, FC#1, port C1
Entries 753
Mean 44.41
Std Dev 11.43
Turn on : 26.7387
Width : 3.506
Height : 20.009
Entry
ampl
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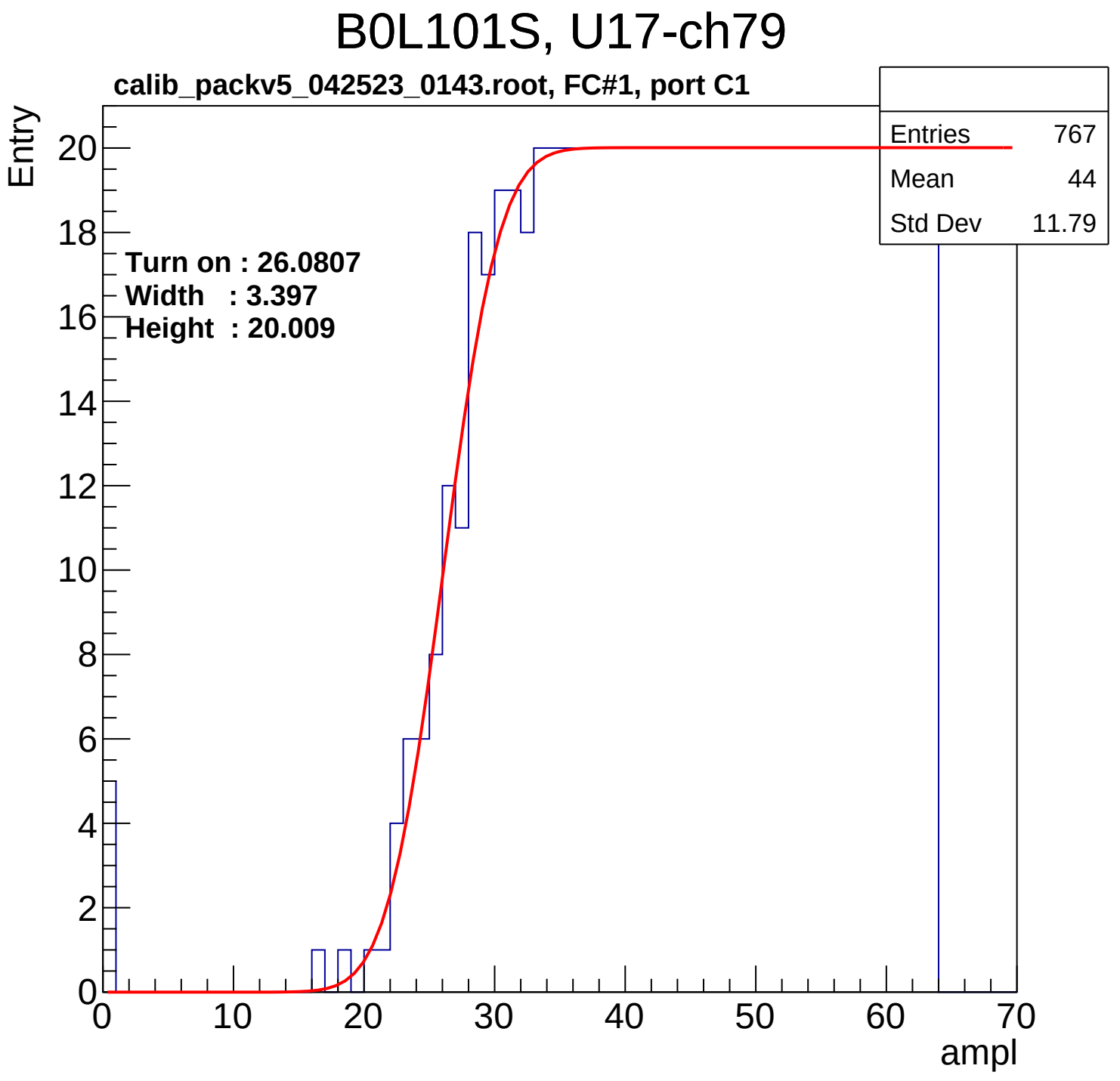
B0L101S, U17-ch79
calib_packv5_042523_0143.root, FC#1, port C1
Entries 767
Mean 44
Std Dev 11.79
Turn on : 26.0807
Width : 3.397
Height : 20.009
Entry
ampl
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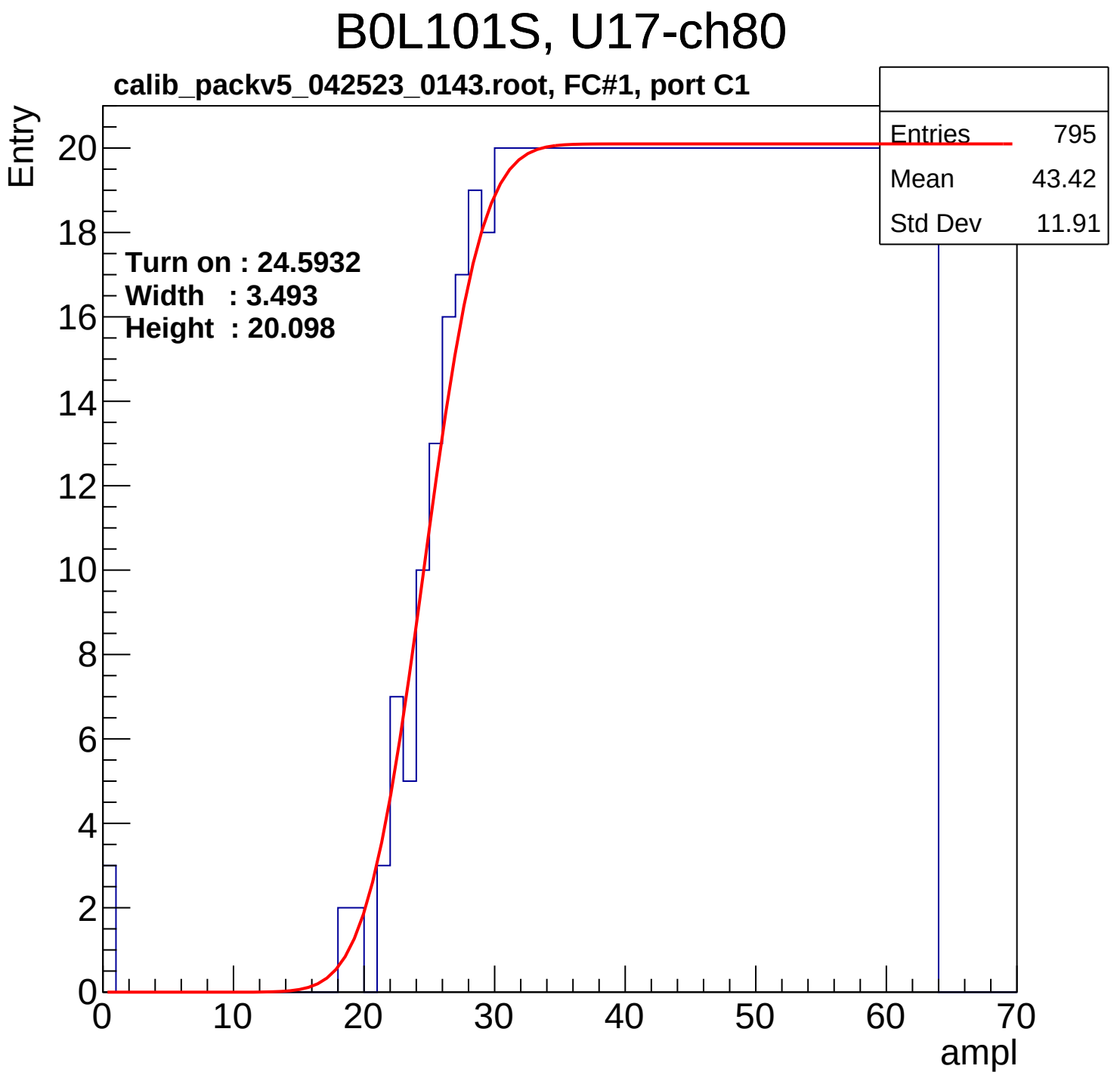
B0L101S, U17-ch80
calib_packv5_042523_0143.root, FC#1, port C1
Entries 795
Mean 43.42
Std Dev 11.91
Turn on : 24.5932
Width : 3.493
Height : 20.098
Entry
ampl
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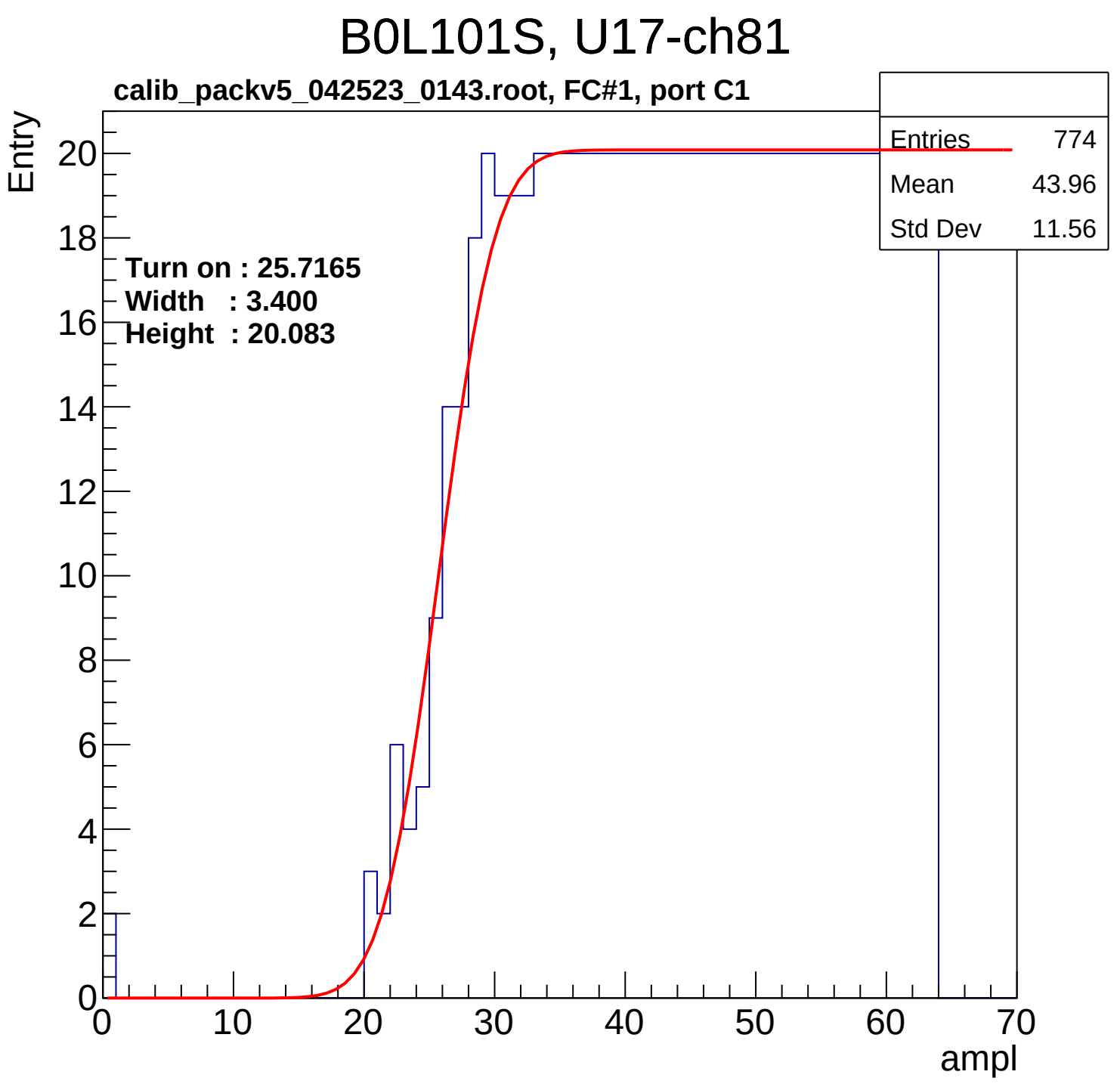
B0L101S, U17-ch81
calib_packv5_042523_0143.root, FC#1, port C1
Entries 774
Mean 43.96
Std Dev 11.56
Turn on : 25.7165
Width : 3.400
Height : 20.083
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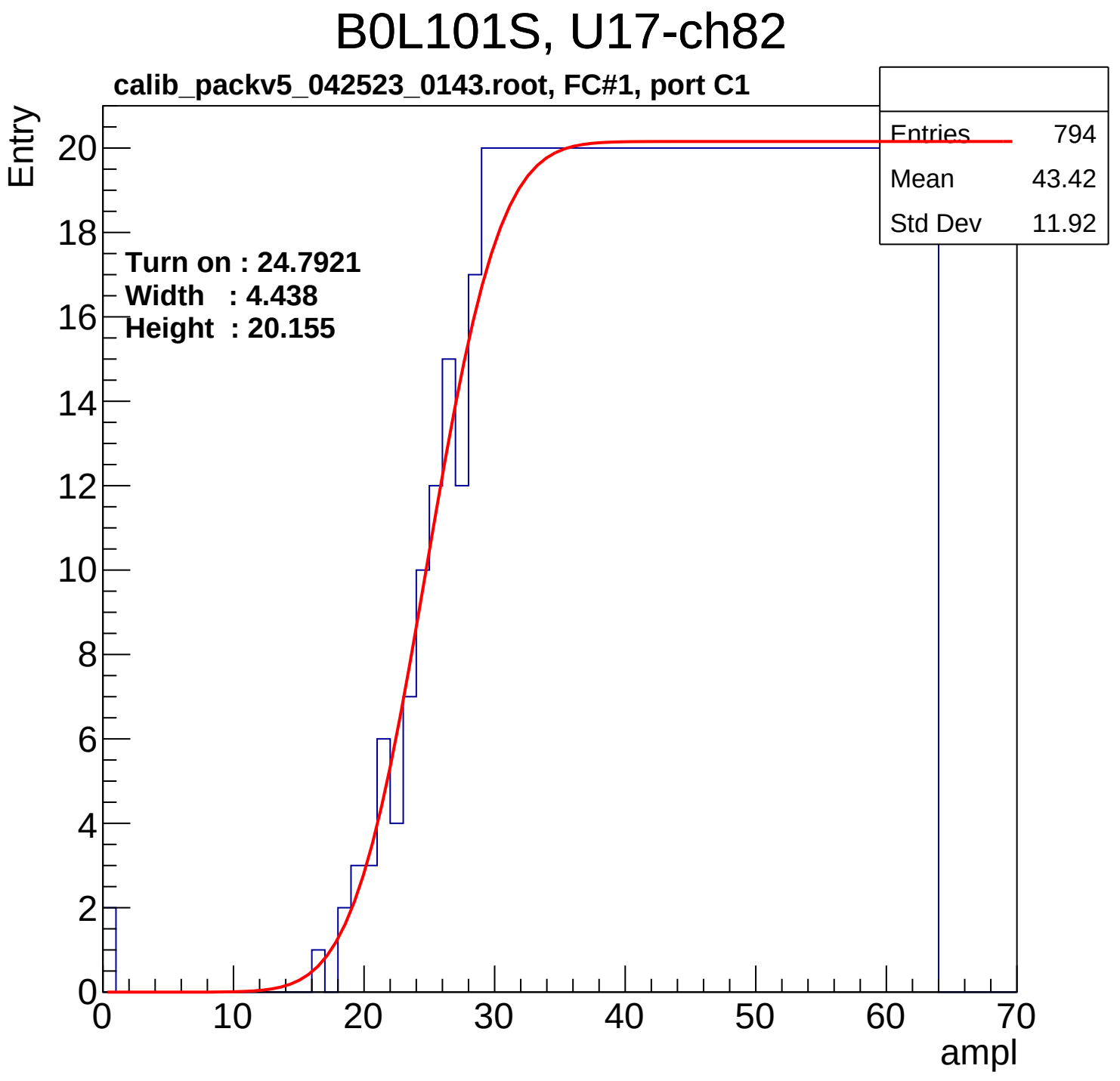
B0L101S, U17-ch82
calib_packv5_042523_0143.root, FC#1, port C1
Entries 794
Mean 43.42
Std Dev 11.92
Turn on : 24.7921
Width : 4.438
Height : 20.155
Entry
ampl
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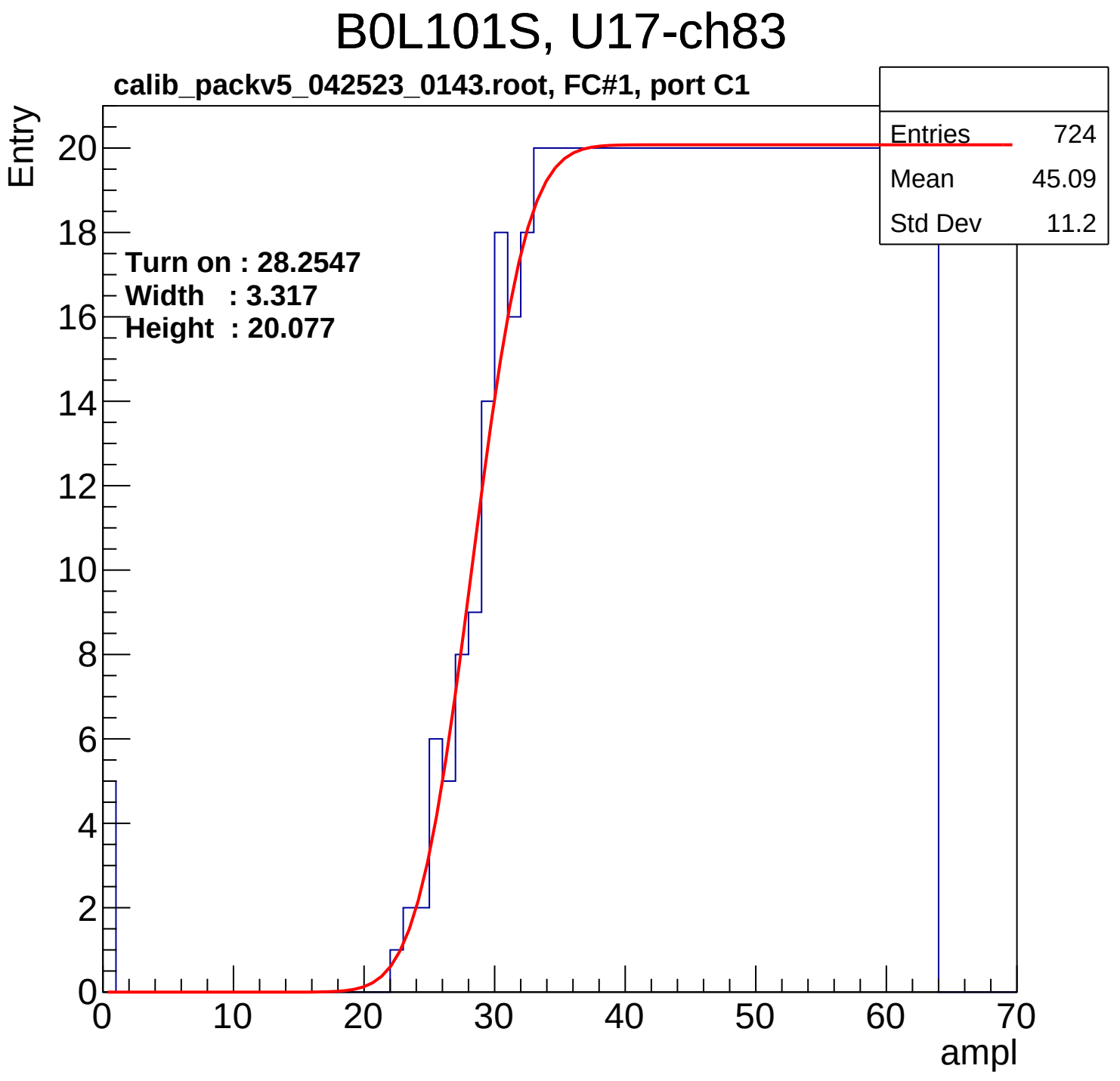
B0L101S, U17-ch83
calib_packv5_042523_0143.root, FC#1, port C1
Entries 724
Mean 45.09
Std Dev 11.2
Turn on : 28.2547
Width : 3.317
Height : 20.077
Entry
ampl
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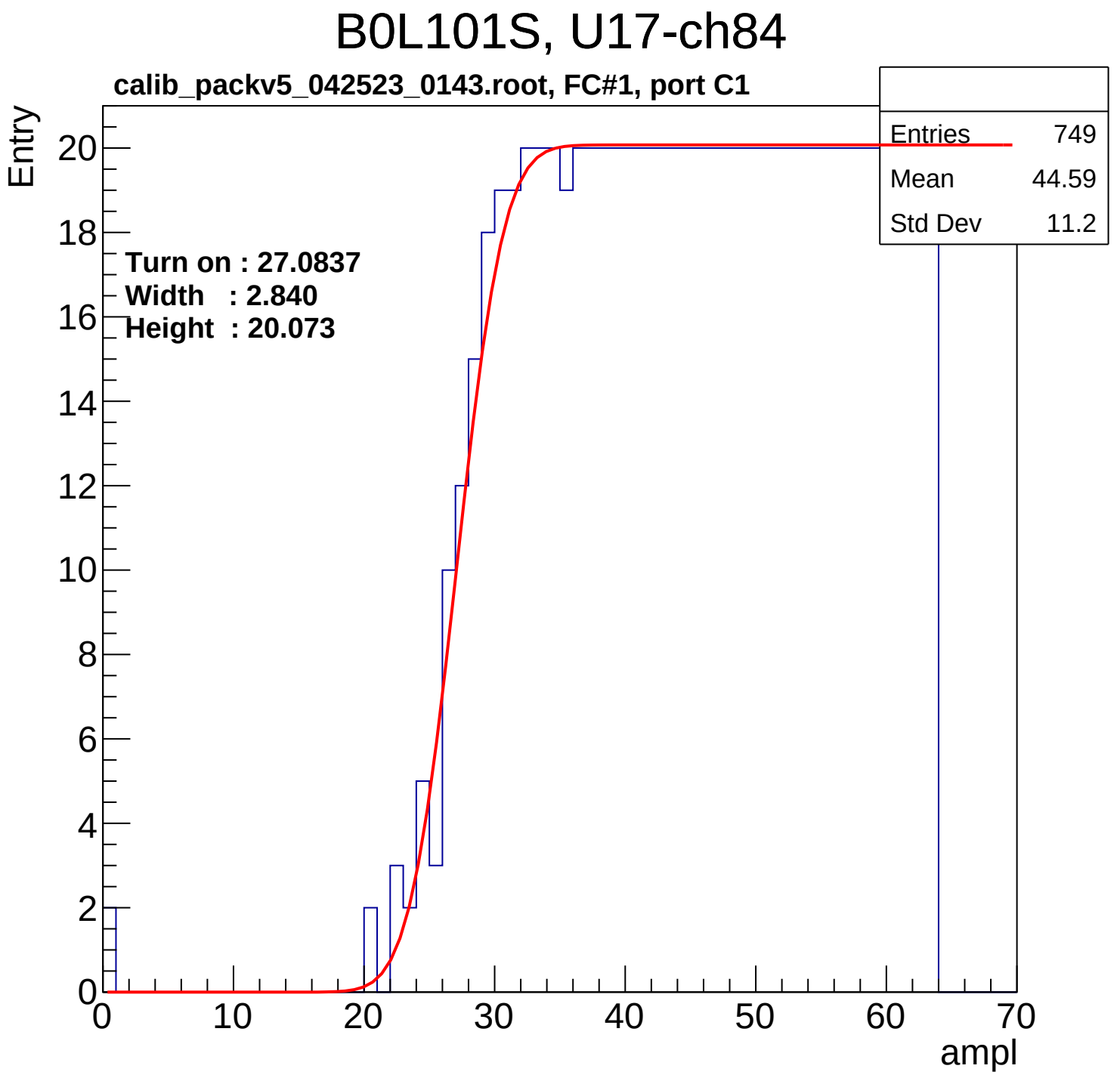
B0L101S, U17-ch84
calib_packv5_042523_0143.root, FC#1, port C1
Entries 749
Mean 44.59
Std Dev 11.2
Turn on : 27.0837
Width : 2.840
Height : 20.073
Entry
ampl
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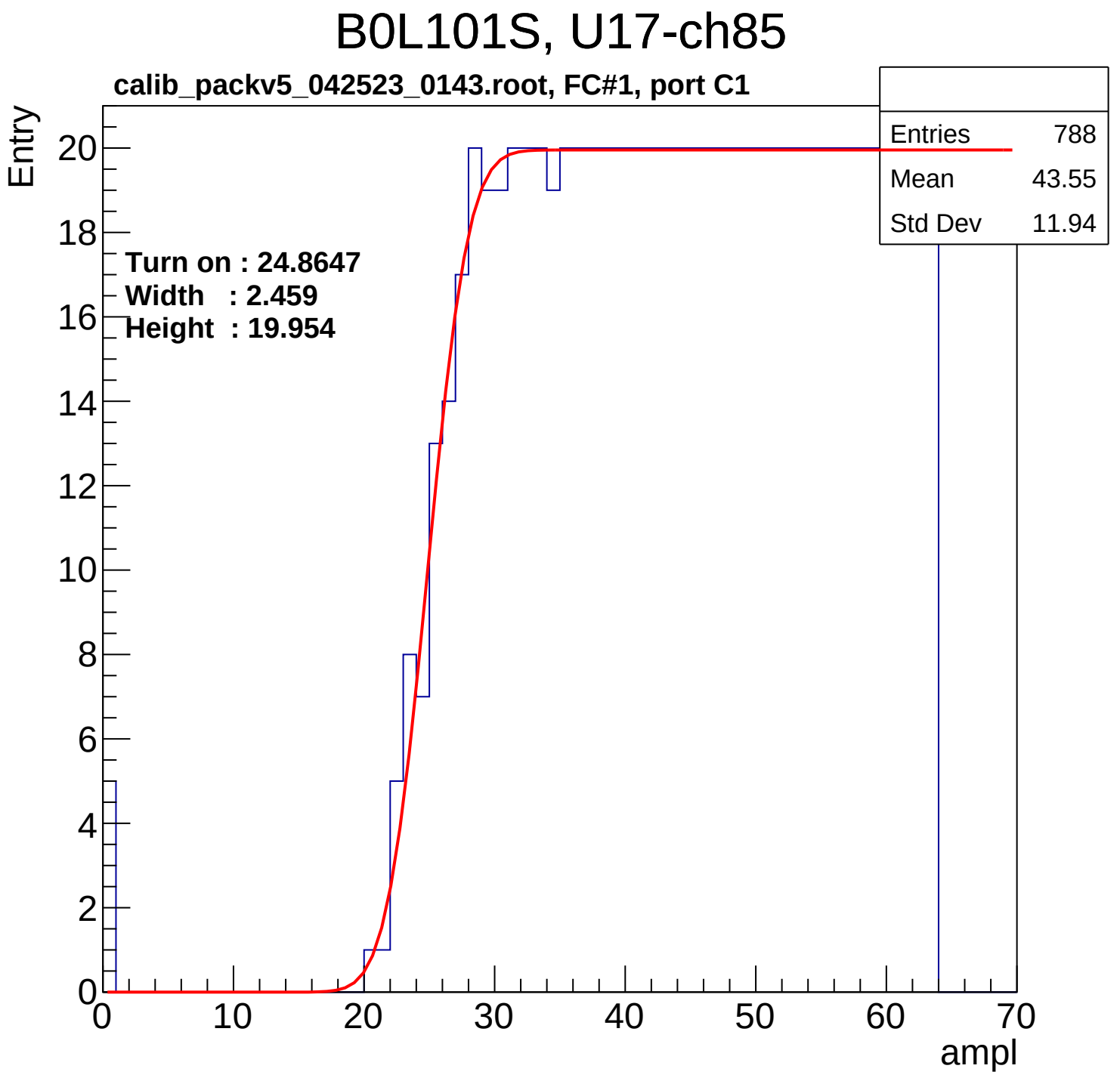
B0L101S, U17-ch85
calib_packv5_042523_0143.root, FC#1, port C1
Entries 788
Mean 43.55
Std Dev 11.94
Turn on : 24.8647
Width : 2.459
Height : 19.954
Entry
ampl
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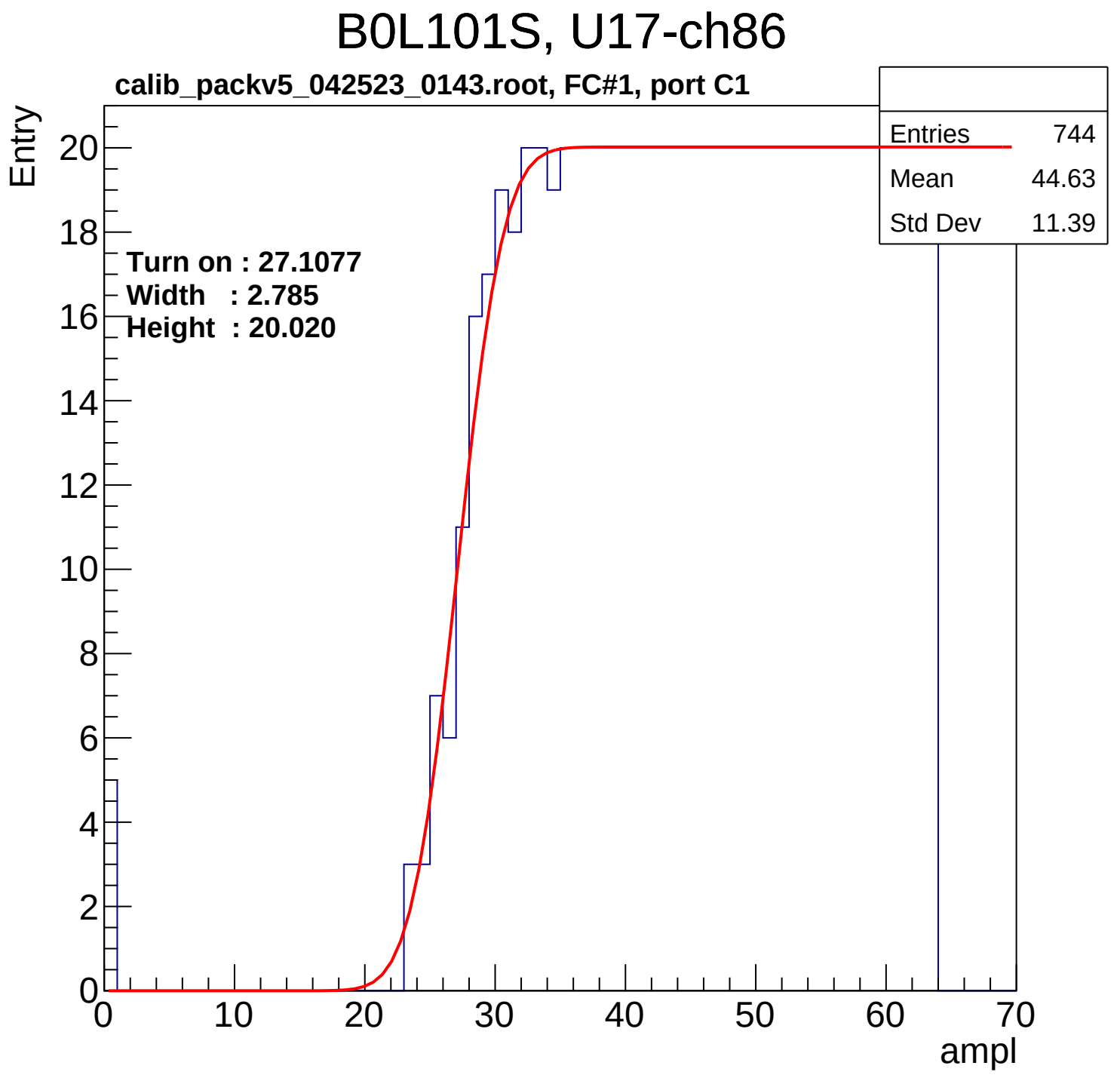
B0L101S, U17-ch86
calib_packv5_042523_0143.root, FC#1, port C1
Entries 744
Mean 44.63
Std Dev 11.39
Turn on : 27.1077
Width : 2.785
Height : 20.020
Entry
ampl
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6
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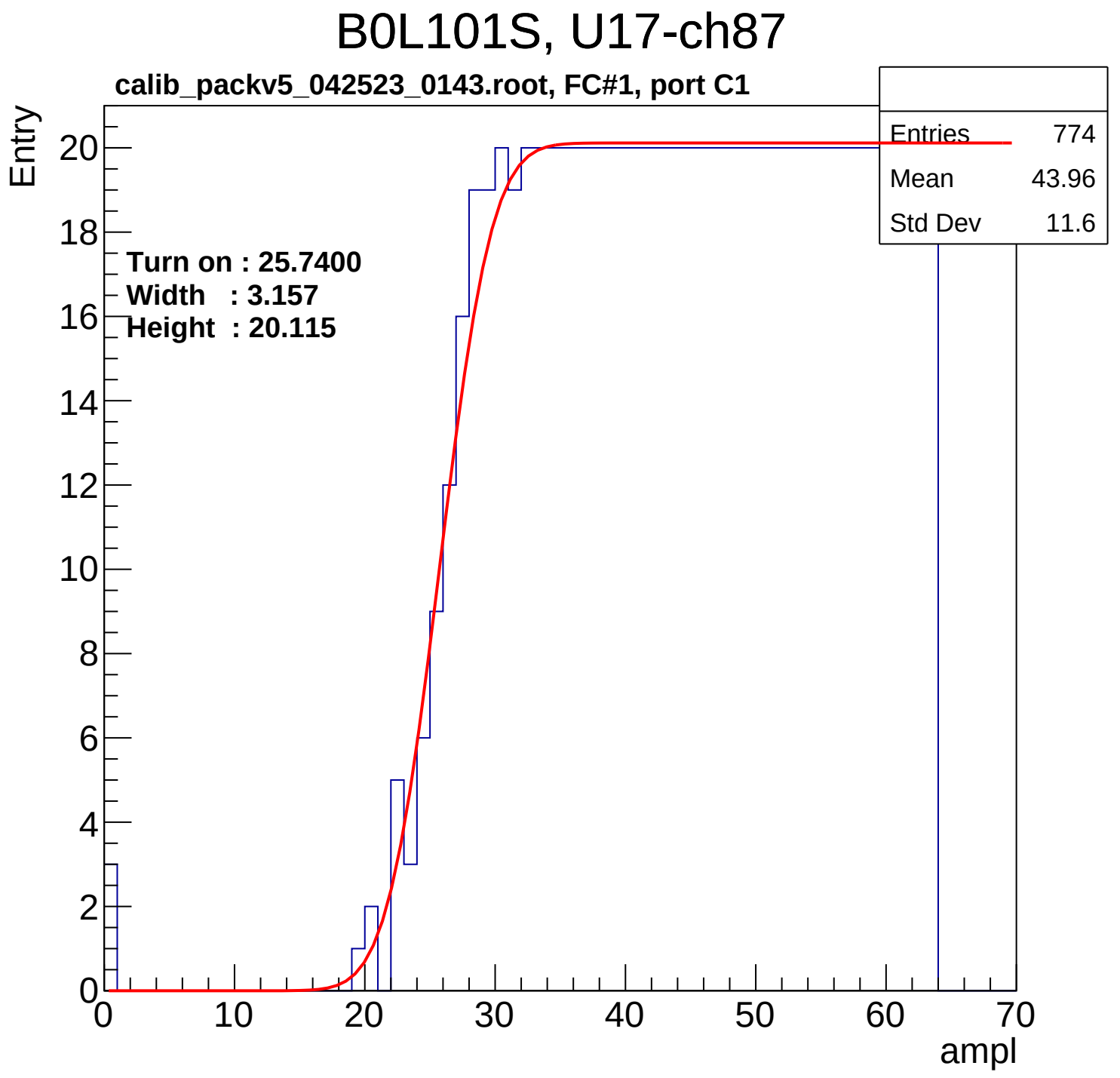
B0L101S, U17-ch87
calib_packv5_042523_0143.root, FC#1, port C1
Entries 774
Mean 43.96
Std Dev 11.6
Turn on : 25.7400
Width : 3.157
Height : 20.115
Entry
ampl
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6
8
10
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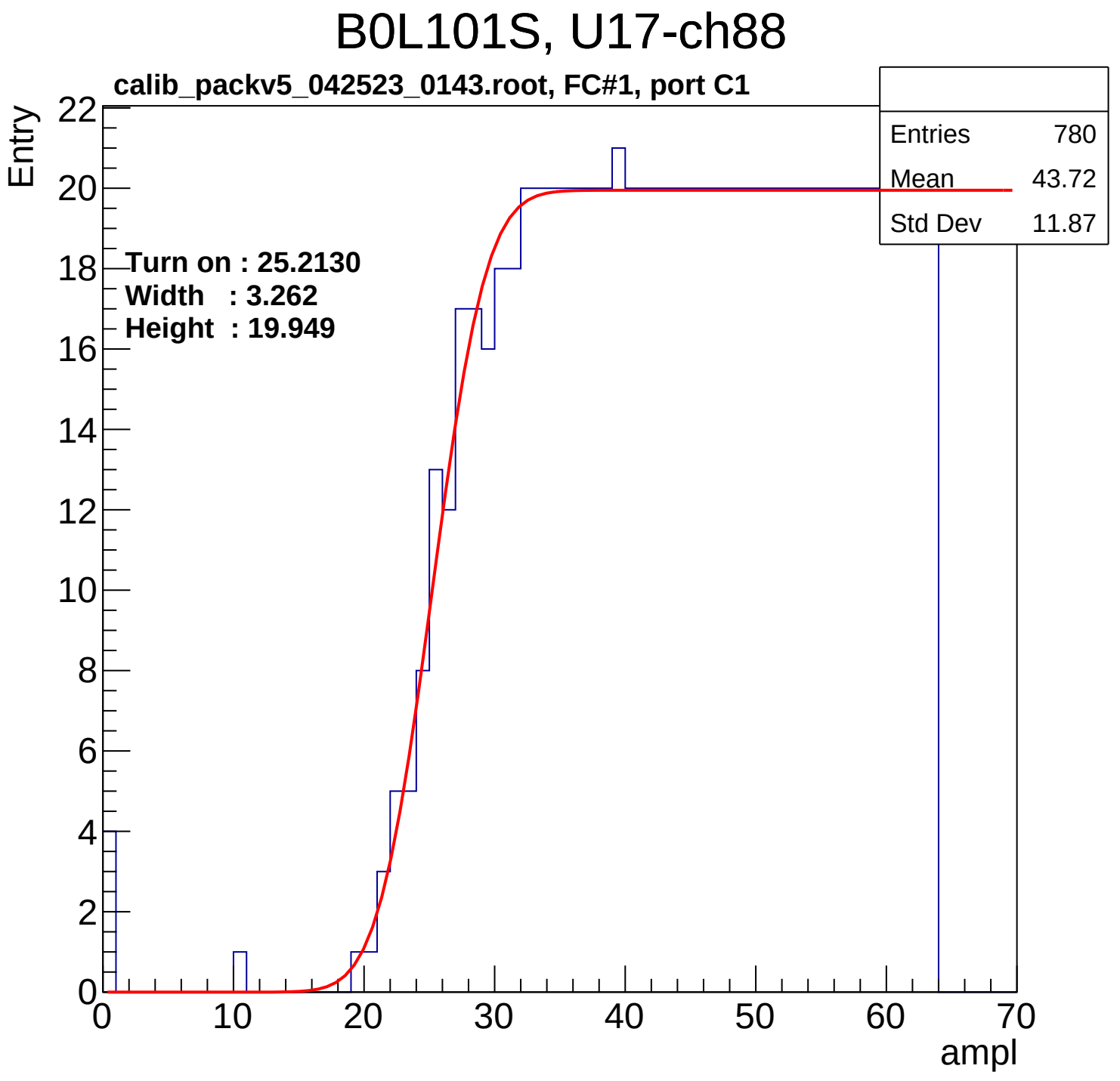
B0L101S, U17-ch88
calib_packv5_042523_0143.root, FC#1, port C1
Entries 780
Mean 43.72
Std Dev 11.87
Turn on : 25.2130
Width : 3.262
Height : 19.949
Entry
ampl
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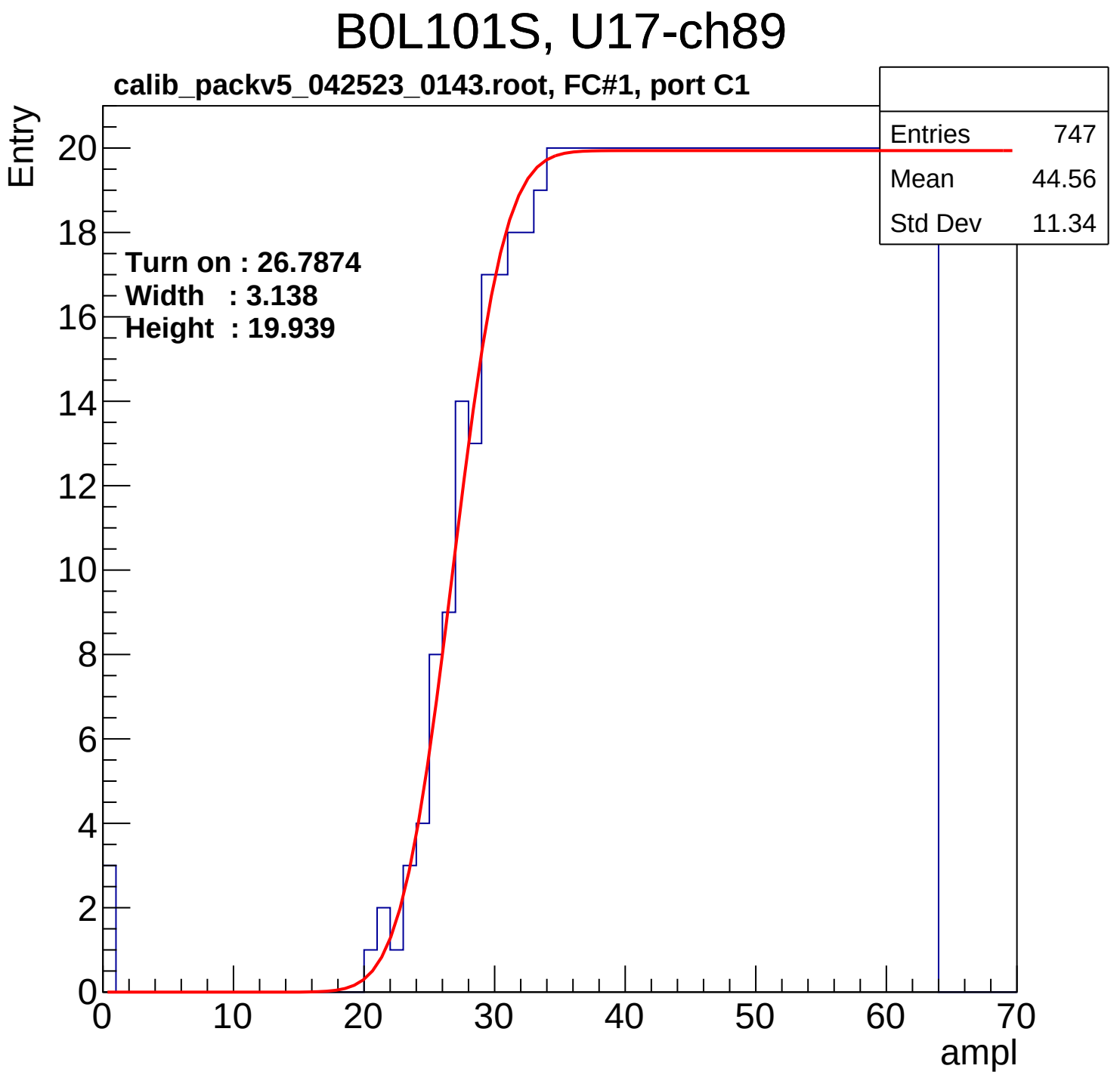
B0L101S, U17-ch89
calib_packv5_042523_0143.root, FC#1, port C1
Entries 747
Mean 44.56
Std Dev 11.34
Turn on : 26.7874
Width : 3.138
Height : 19.939
Entry
ampl
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6
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10
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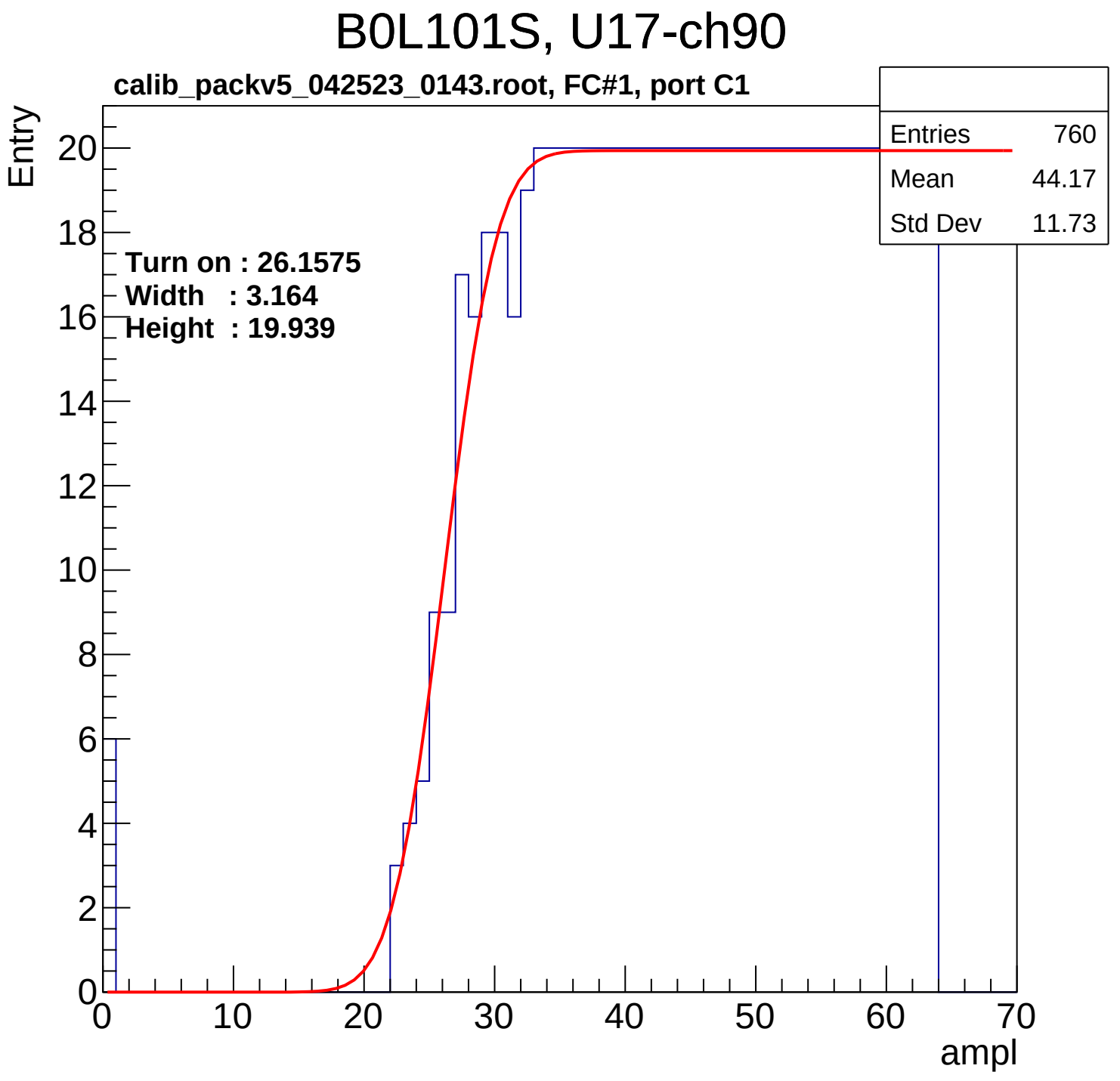
B0L101S, U17-ch90
calib_packv5_042523_0143.root, FC#1, port C1
Entries 760
Mean 44.17
Std Dev 11.73
Turn on : 26.1575
Width : 3.164
Height : 19.939
Entry
ampl
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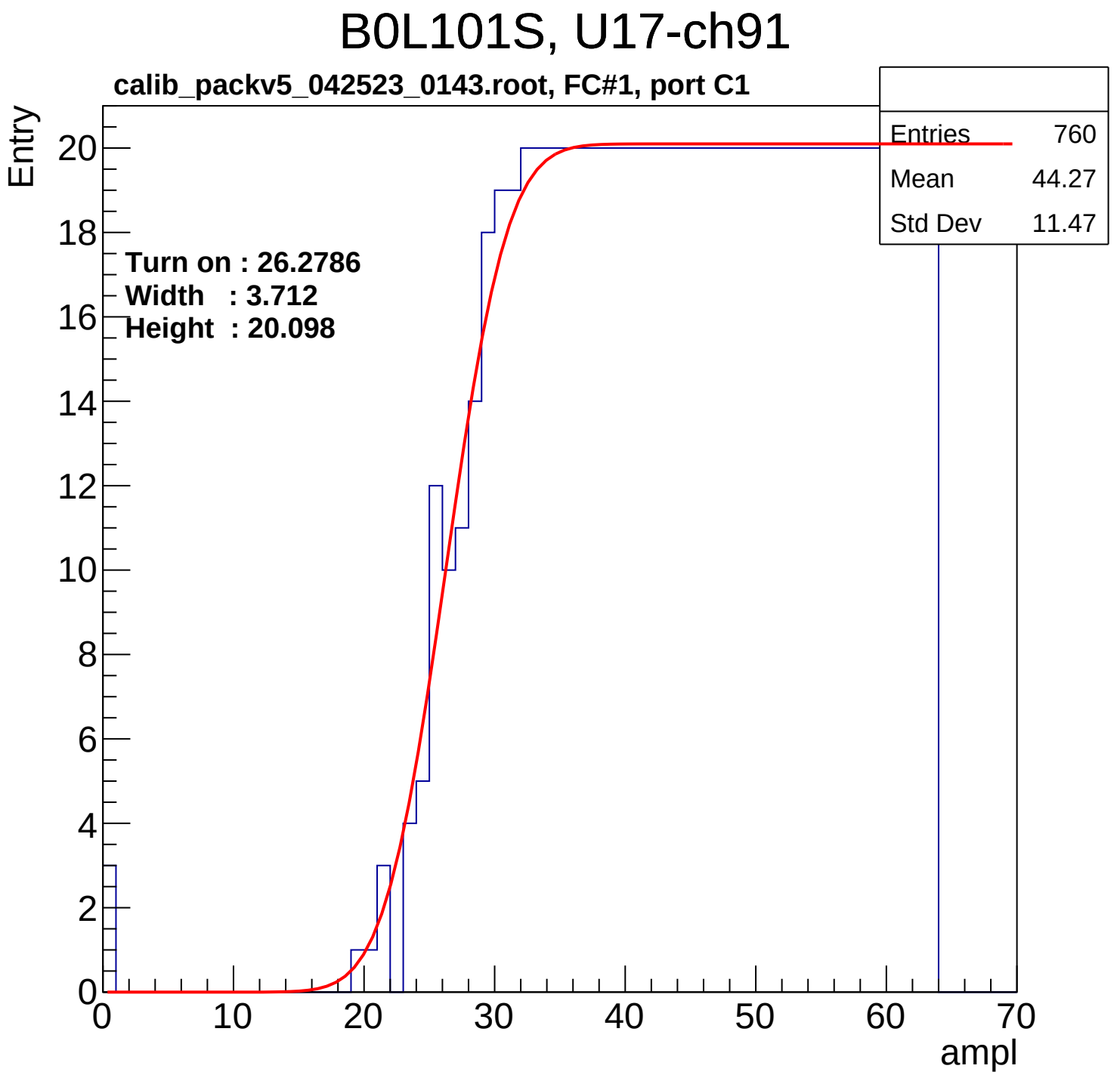
B0L101S, U17-ch91
calib_packv5_042523_0143.root, FC#1, port C1
Entries 760
Mean 44.27
Std Dev 11.47
Turn on : 26.2786
Width : 3.712
Height : 20.098
Entry
ampl
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2
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6
8
10
12
14
16
18
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0
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60
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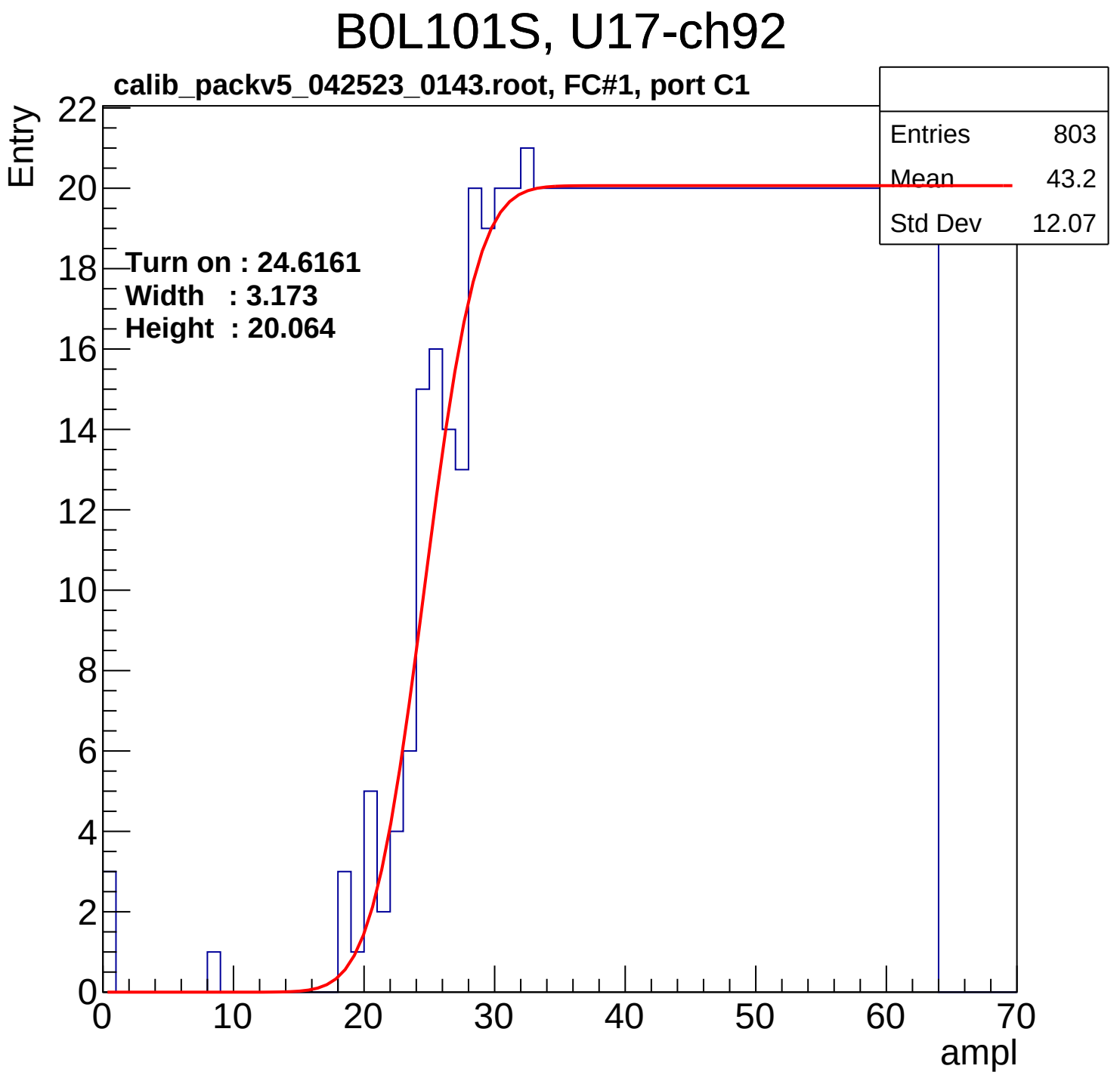
B0L101S, U17-ch92
calib_packv5_042523_0143.root, FC#1, port C1
Entries 803
Mean 43.2
Std Dev 12.07
Turn on : 24.6161
Width : 3.173
Height : 20.064
Entry
ampl
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8
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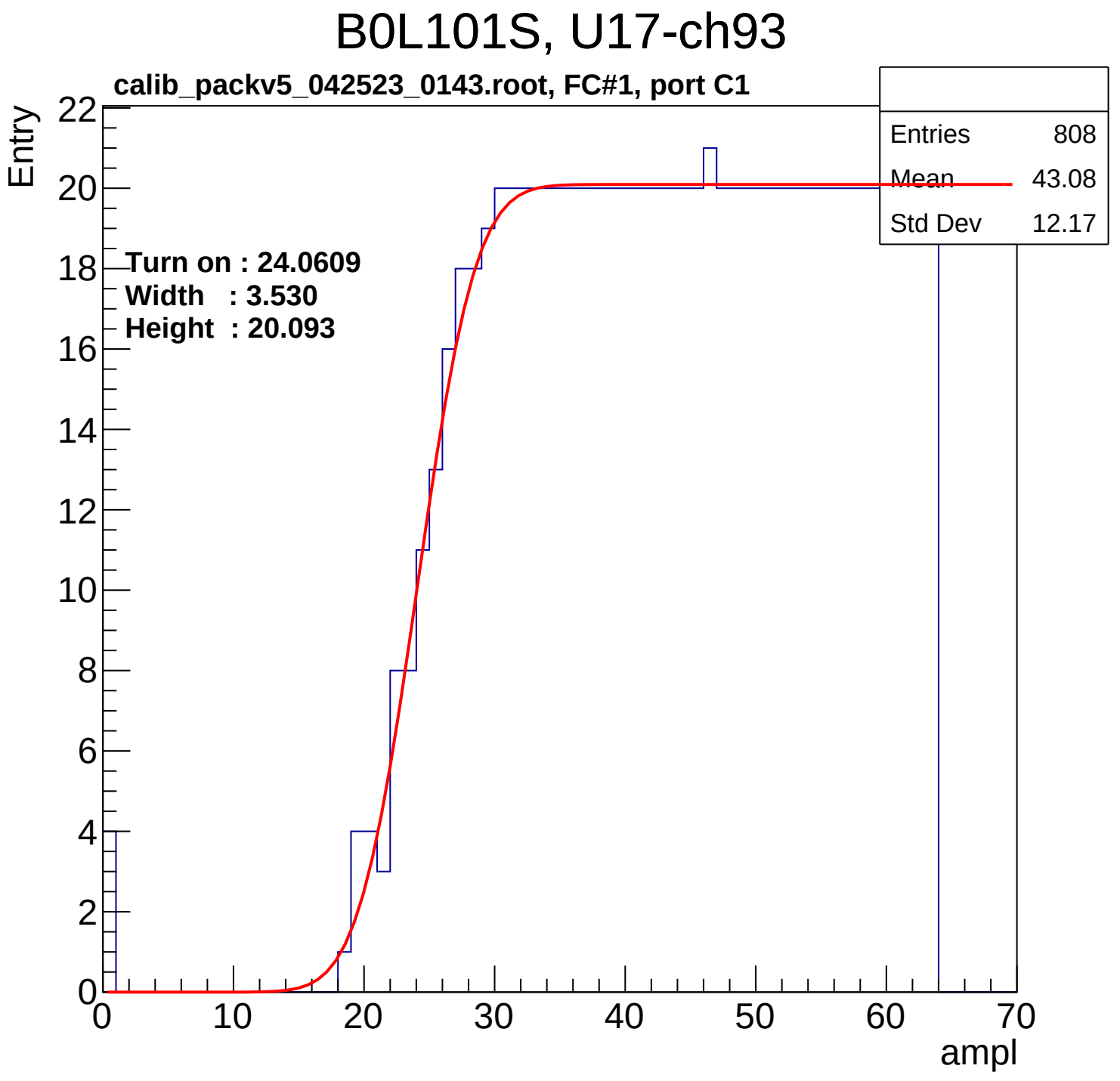
B0L101S, U17-ch93
calib_packv5_042523_0143.root, FC#1, port C1
Entries 808
Mean 43.08
Std Dev 12.17
Turn on : 24.0609
Width : 3.530
Height : 20.093
Entry
ampl
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10
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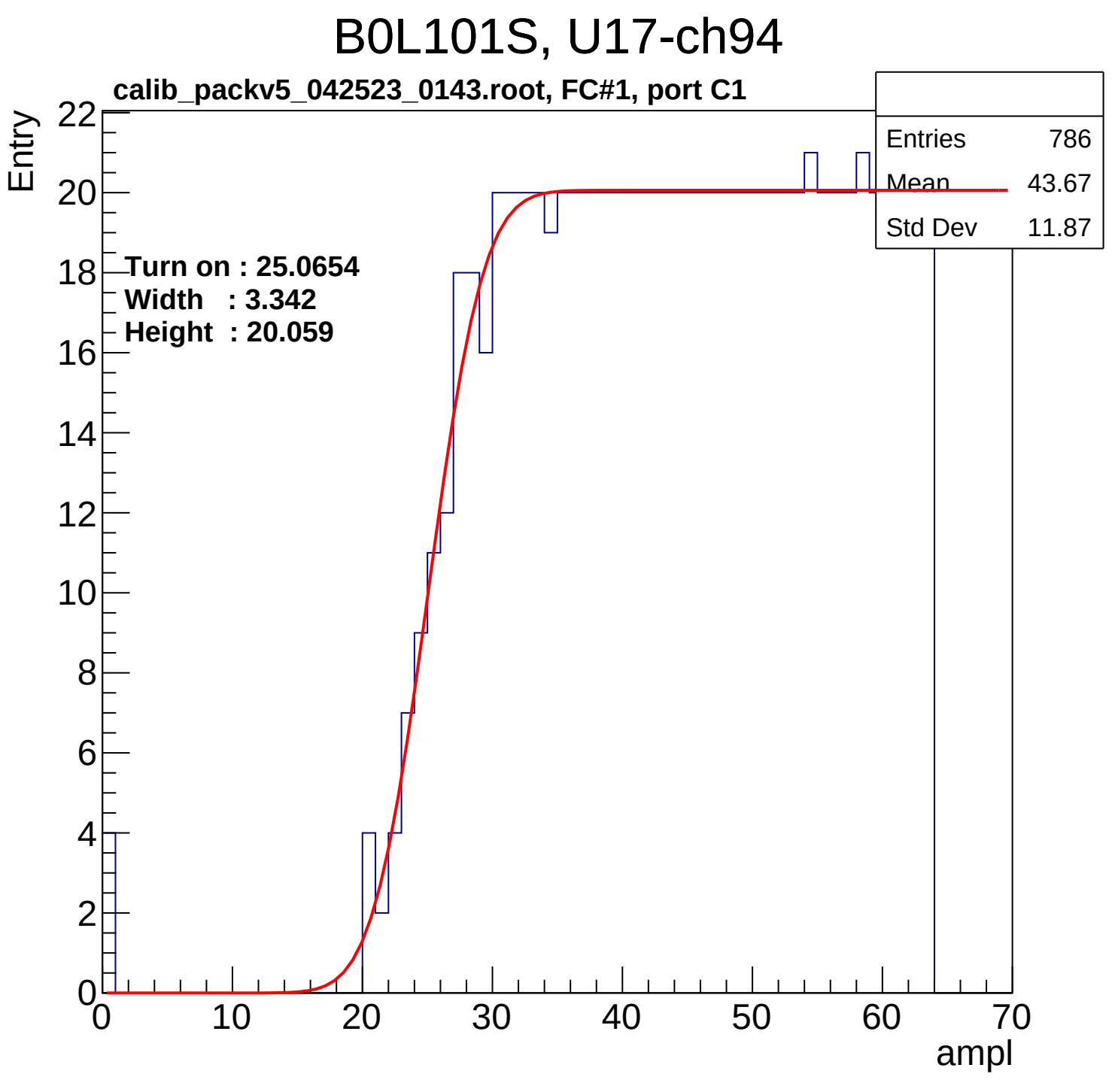
B0L101S, U17-ch94
calib_packv5_042523_0143.root, FC#1, port C1
Entries 786
Mean 43.67
Std Dev 11.87
Turn on : 25.0654
Width : 3.342
Height : 20.059
Entry
ampl
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8
10
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14
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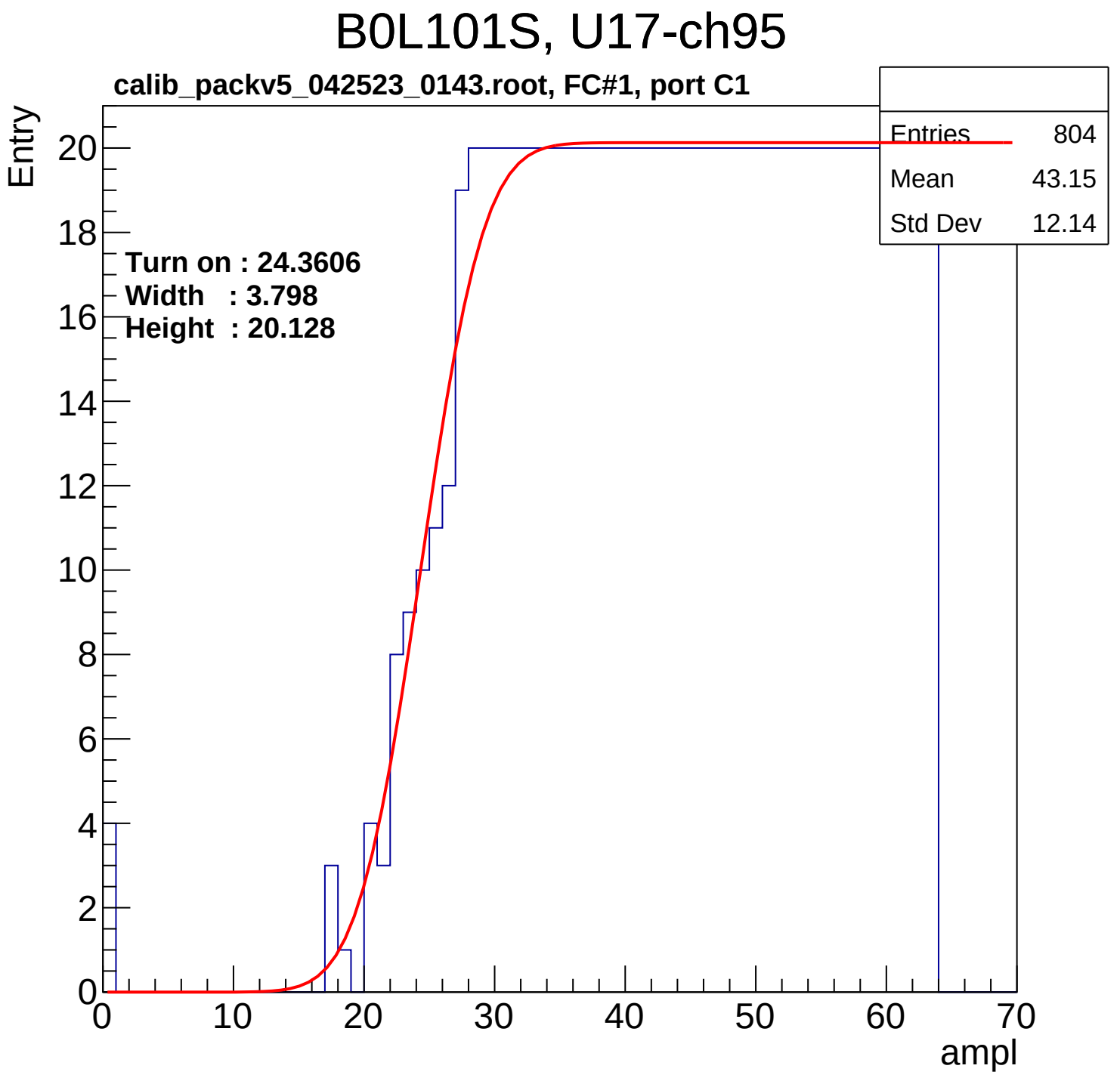
B0L101S, U17-ch95
calib_packv5_042523_0143.root, FC#1, port C1
Entries 804
Mean 43.15
Std Dev 12.14
Turn on : 24.3606
Width : 3.798
Height : 20.128
Entry
ampl
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6
8
10
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14
16
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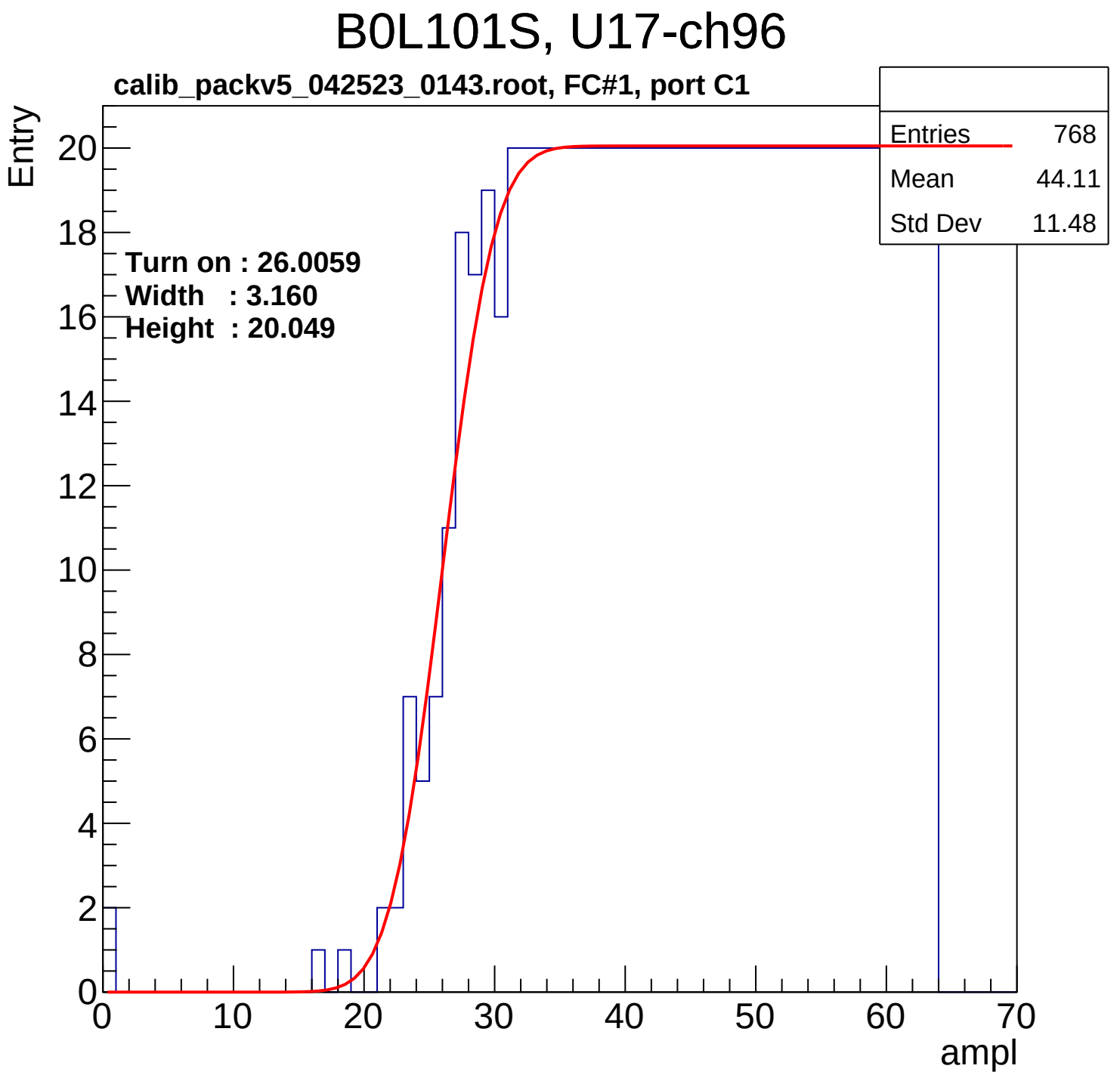
B0L101S, U17-ch96
calib_packv5_042523_0143.root, FC#1, port C1
Entries 768
Mean 44.11
Std Dev 11.48
Turn on : 26.0059
Width : 3.160
Height : 20.049
Entry
ampl
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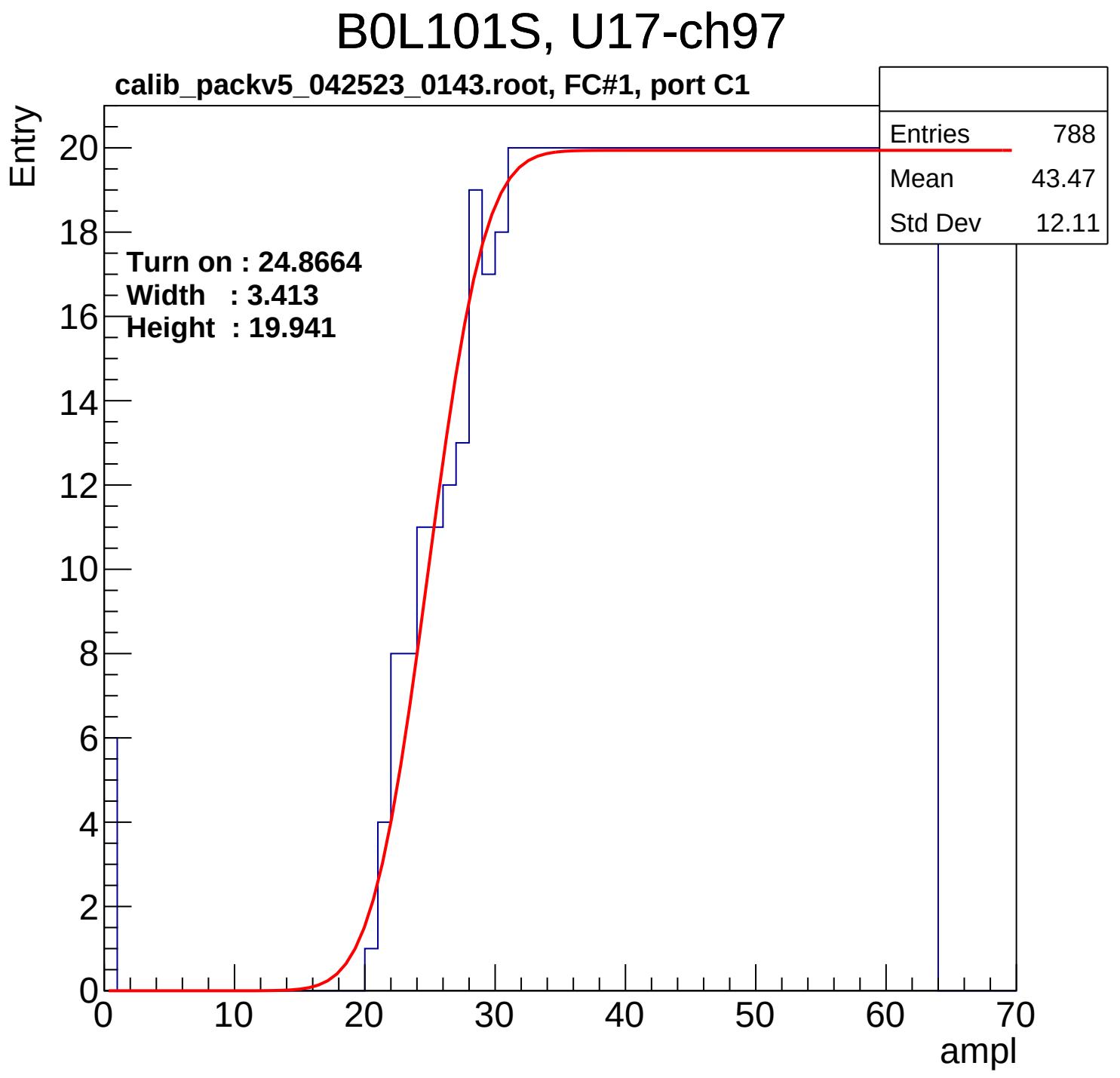
B0L101S, U17-ch97
calib_packv5_042523_0143.root, FC#1, port C1
Entries 788
Mean 43.47
Std Dev 12.11
Turn on : 24.8664
Width : 3.413
Height : 19.941
Entry
ampl
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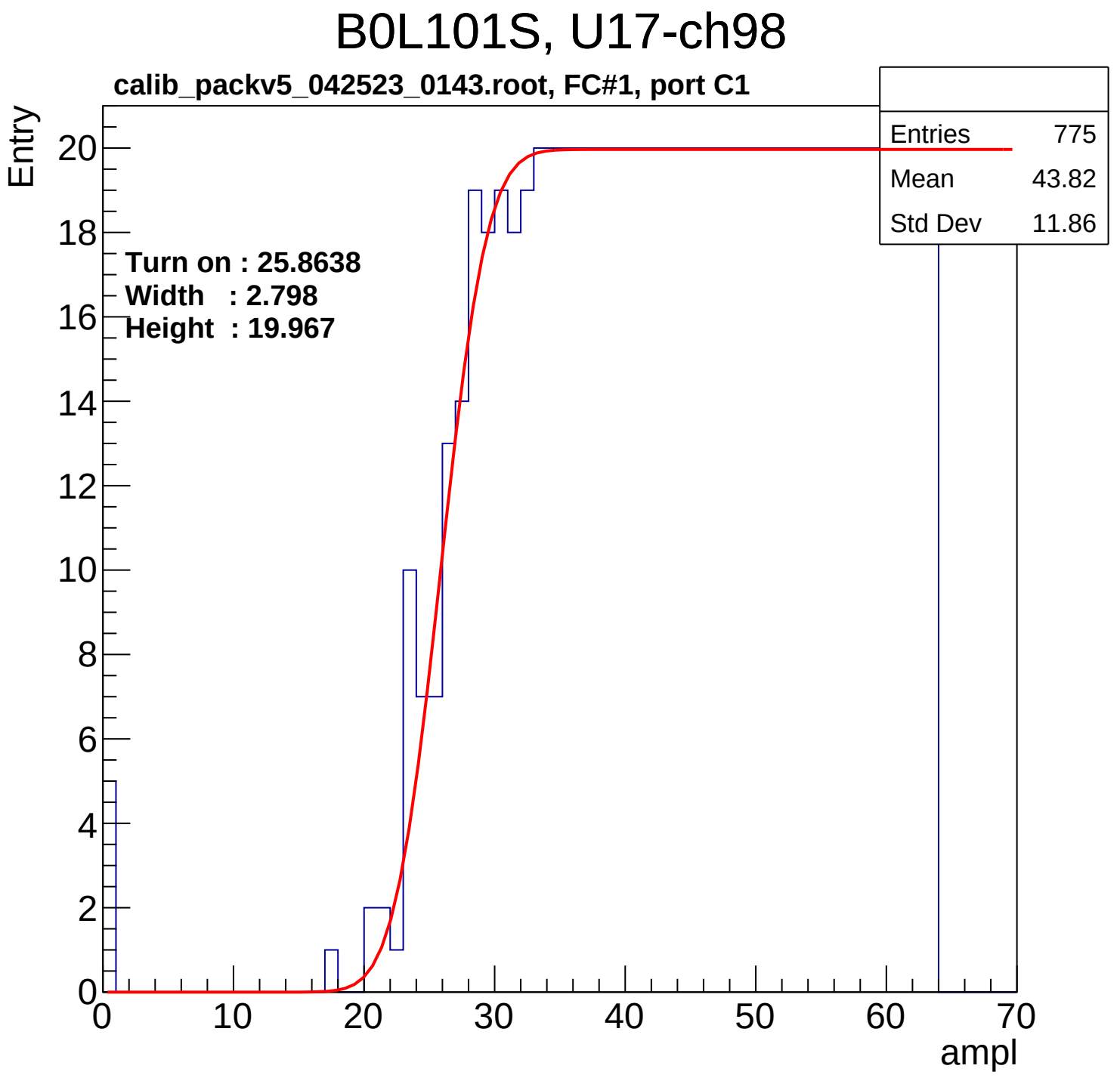
B0L101S, U17-ch98
calib_packv5_042523_0143.root, FC#1, port C1
Entries 775
Mean 43.82
Std Dev 11.86
Turn on : 25.8638
Width : 2.798
Height : 19.967
Entry
ampl
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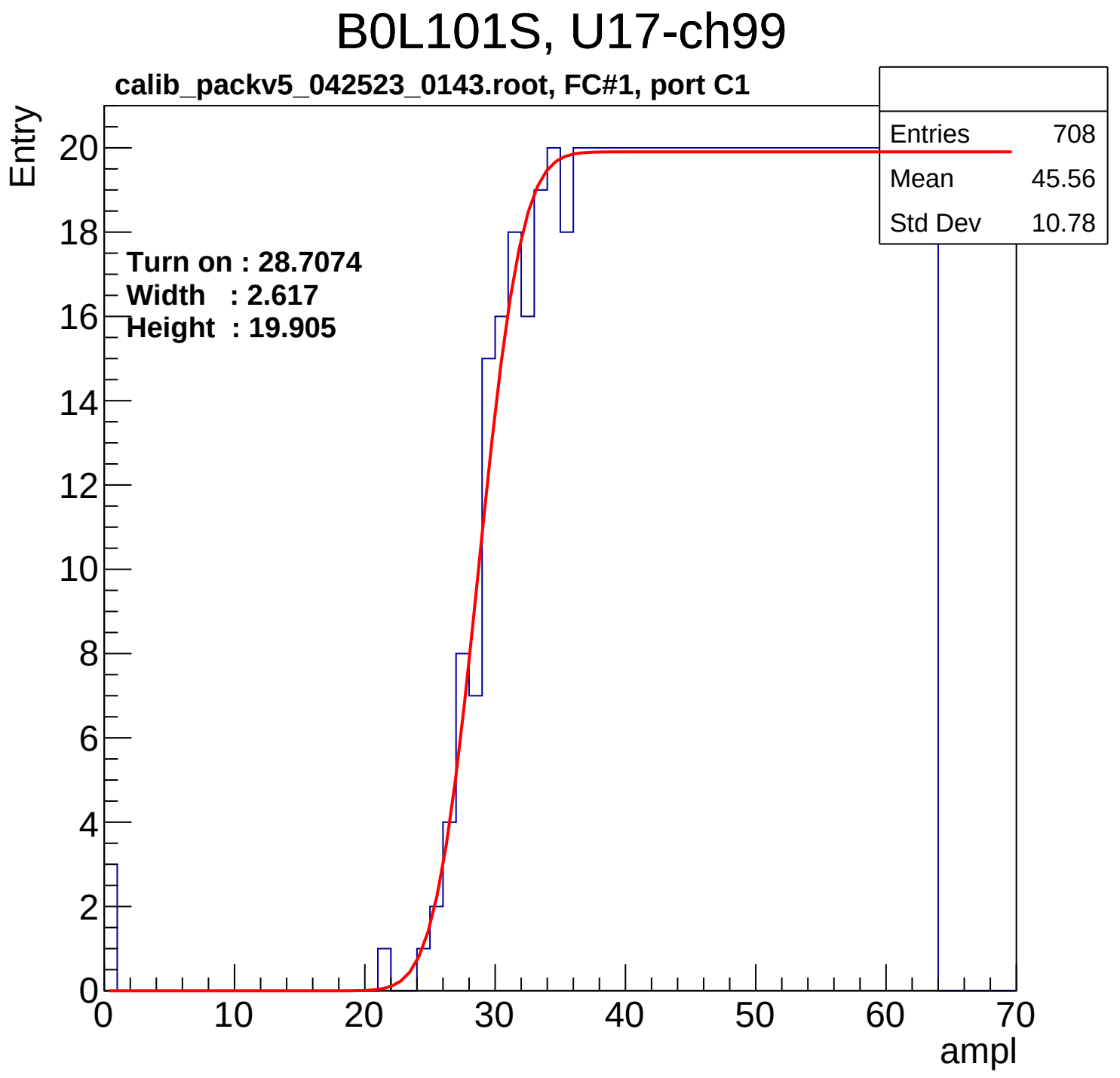
B0L101S, U17-ch99
calib_packv5_042523_0143.root, FC#1, port C1
Entries 708
Mean 45.56
Std Dev 10.78
Turn on : 28.7074
Width : 2.617
Height : 19.905
Entry
ampl
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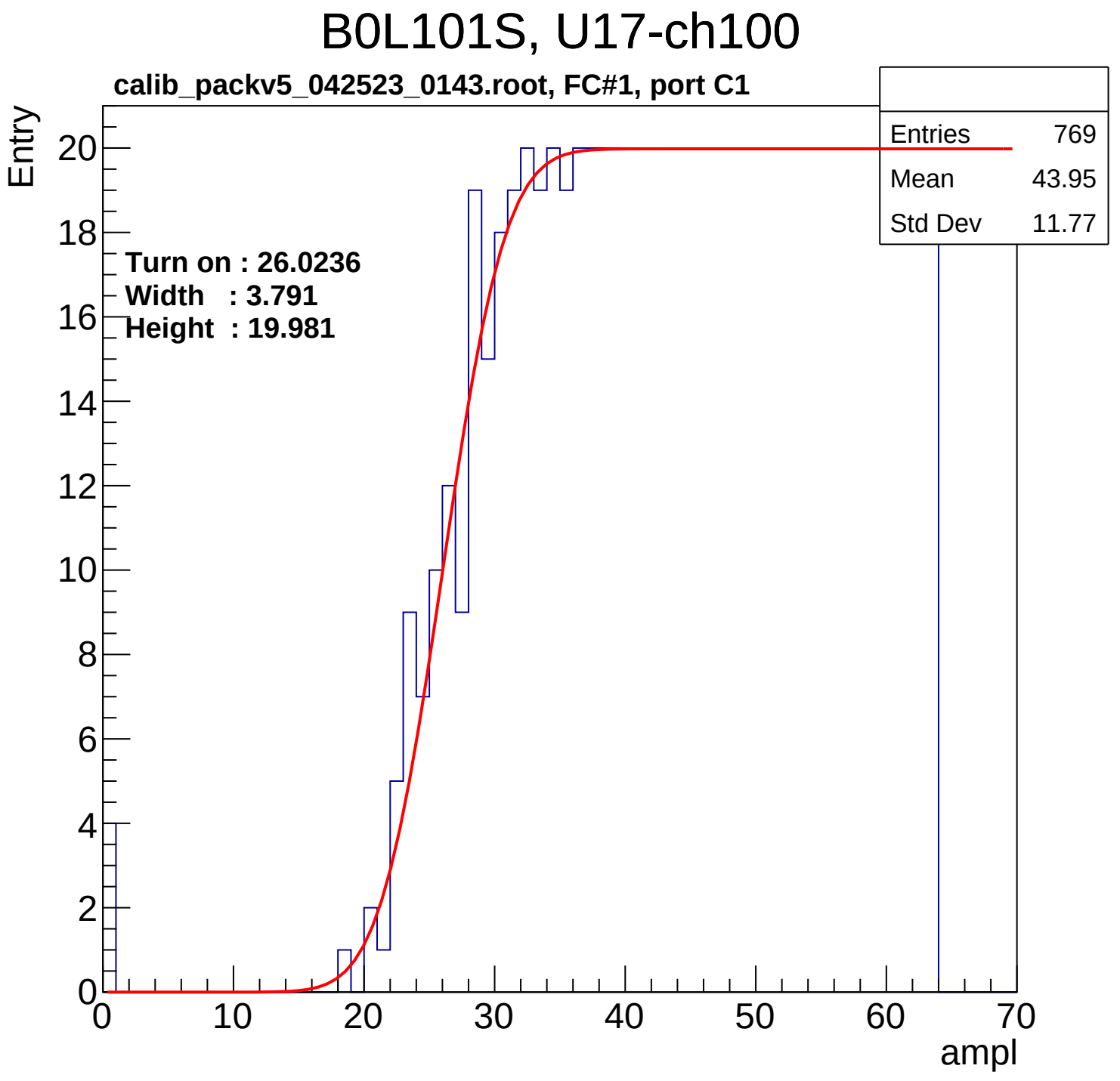
B0L101S, U17-ch100
calib_packv5_042523_0143.root, FC#1, port C1
Entries 769
Mean 43.95
Std Dev 11.77
Turn on : 26.0236
Width : 3.791
Height : 19.981
Entry
ampl
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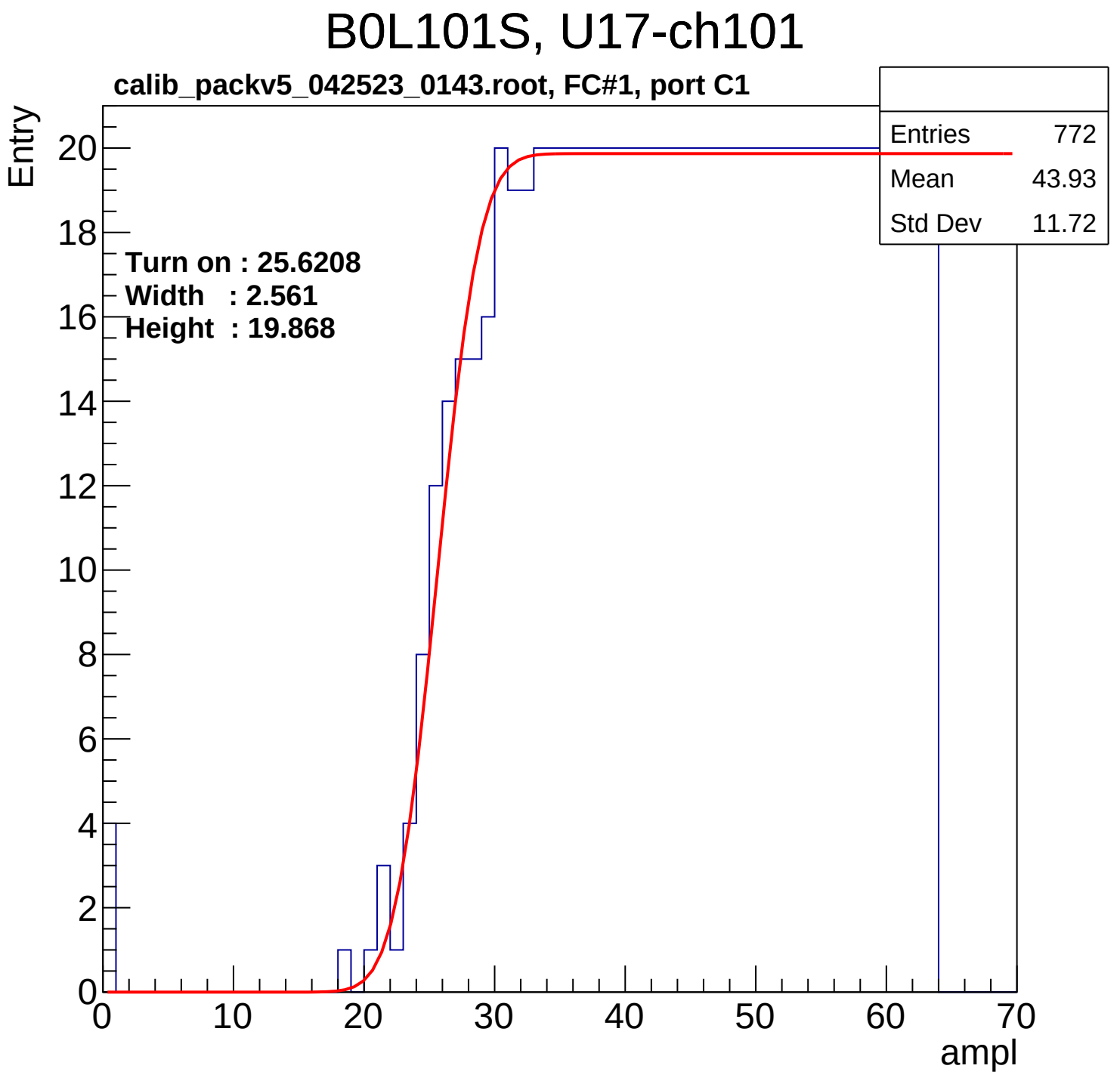
B0L101S, U17-ch101
calib_packv5_042523_0143.root, FC#1, port C1
Entries 772
Mean 43.93
Std Dev 11.72
Turn on : 25.6208
Width : 2.561
Height : 19.868
Entry
ampl
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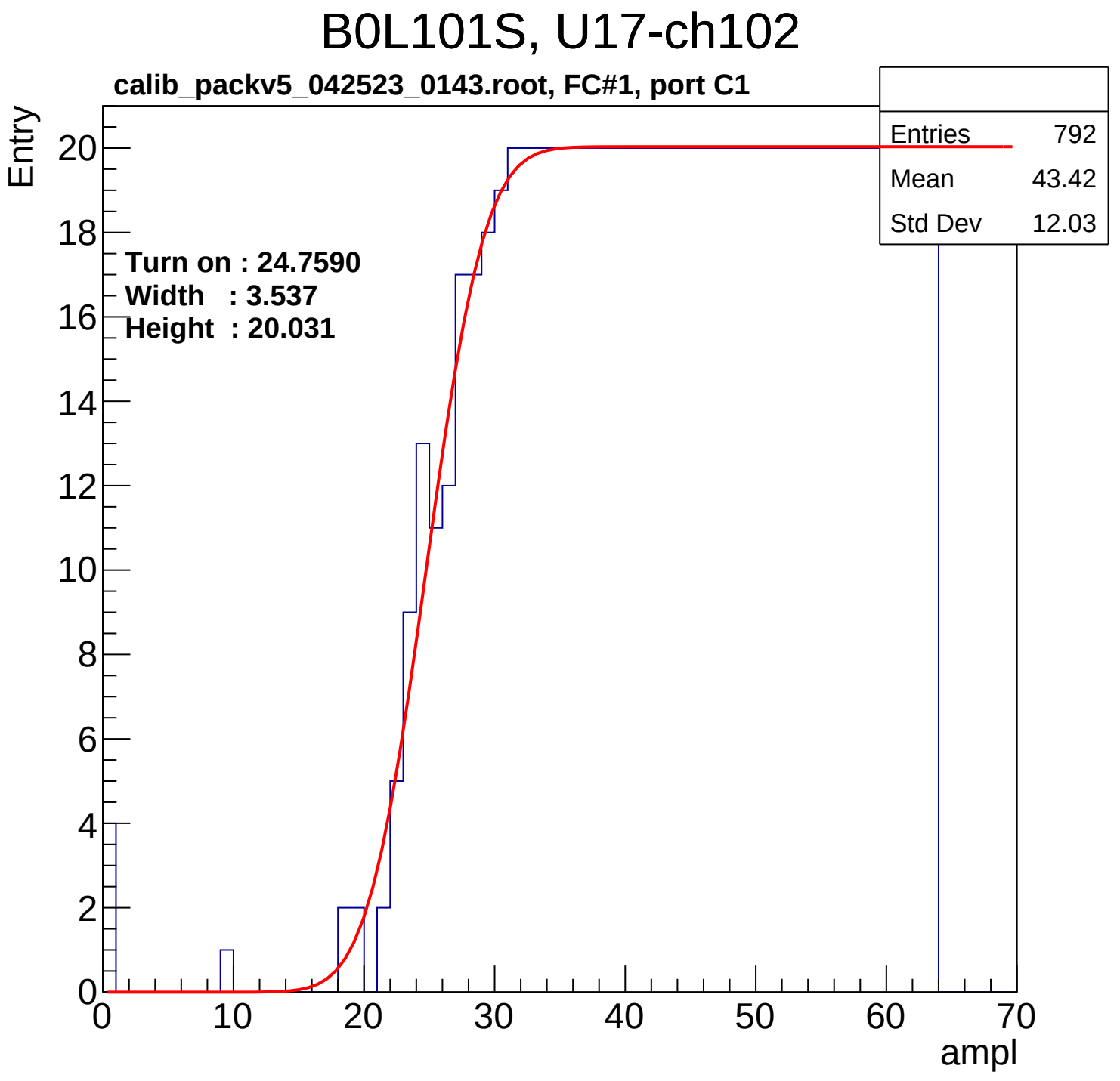
B0L101S, U17-ch102
calib_packv5_042523_0143.root, FC#1, port C1
Entries 792
Mean 43.42
Std Dev 12.03
Turn on : 24.7590
Width : 3.537
Height : 20.031
Entry
ampl
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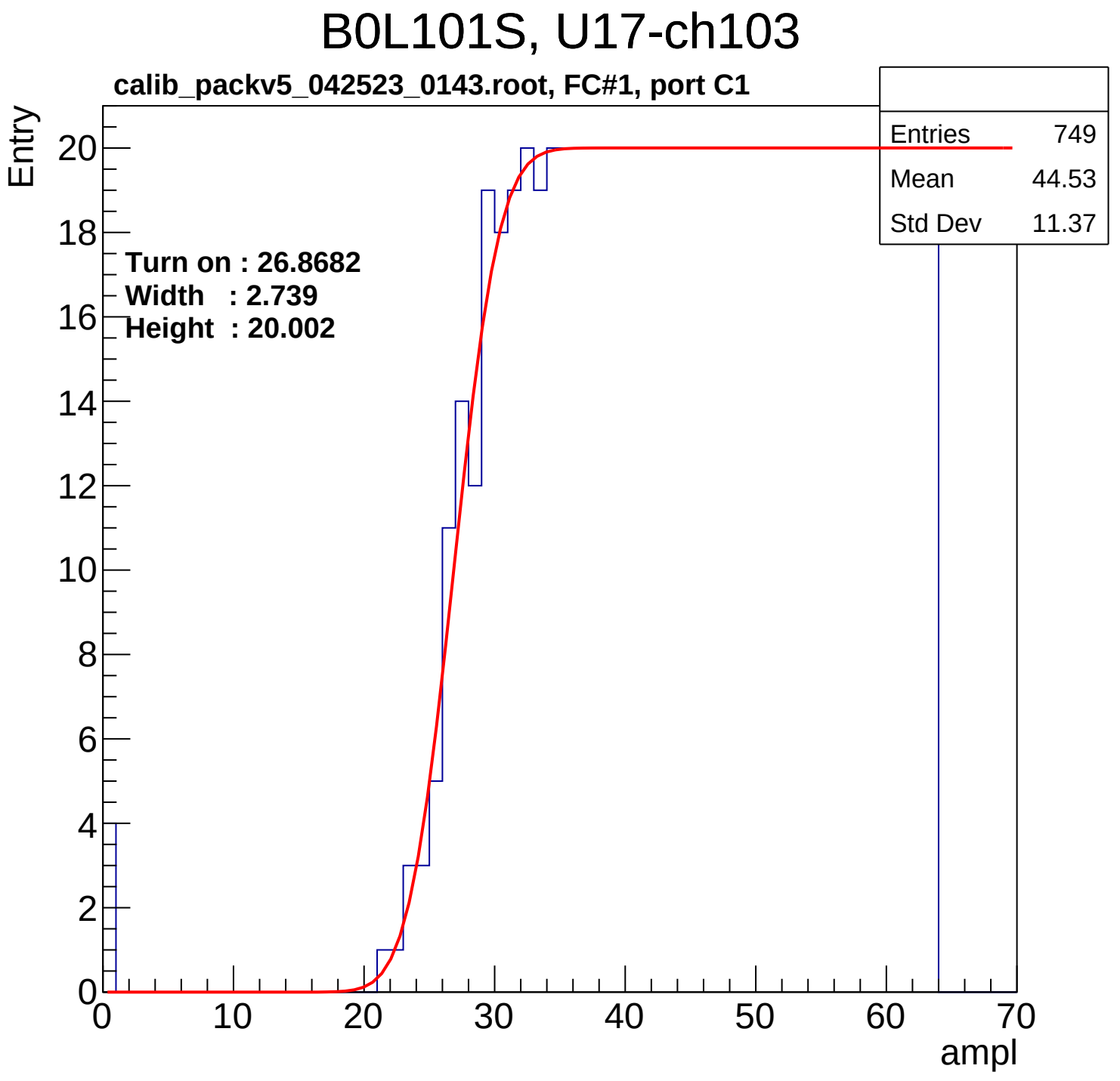
B0L101S, U17-ch103
calib_packv5_042523_0143.root, FC#1, port C1
Entries 749
Mean 44.53
Std Dev 11.37
Turn on : 26.8682
Width : 2.739
Height : 20.002
Entry
ampl
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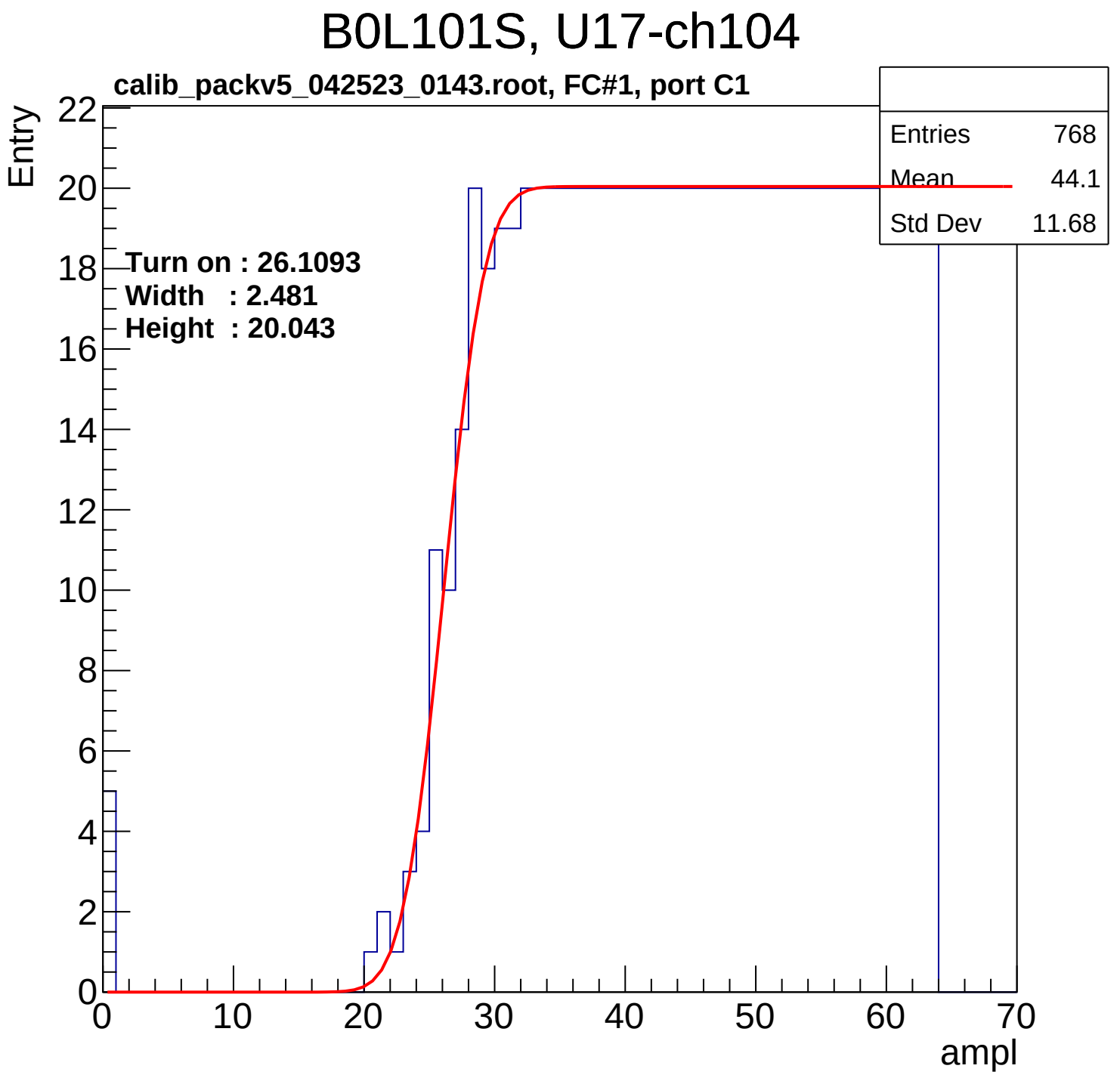
B0L101S, U17-ch104
calib_packv5_042523_0143.root, FC#1, port C1
Entries 768
Mean 44.1
Std Dev 11.68
Turn on : 26.1093
Width : 2.481
Height : 20.043
Entry
ampl
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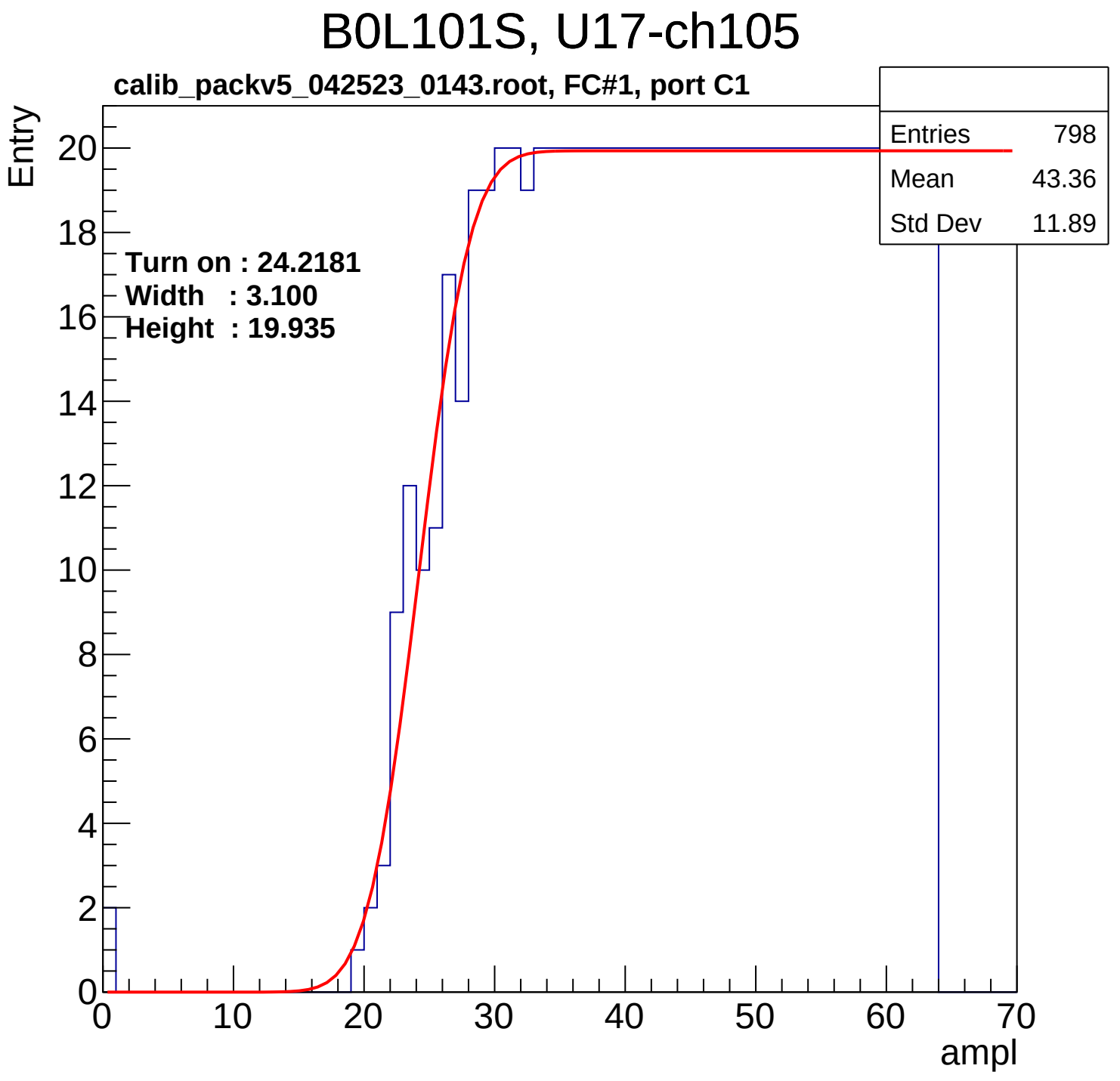
B0L101S, U17-ch105
calib_packv5_042523_0143.root, FC#1, port C1
Entries 798
Mean 43.36
Std Dev 11.89
Turn on : 24.2181
Width : 3.100
Height : 19.935
Entry
ampl
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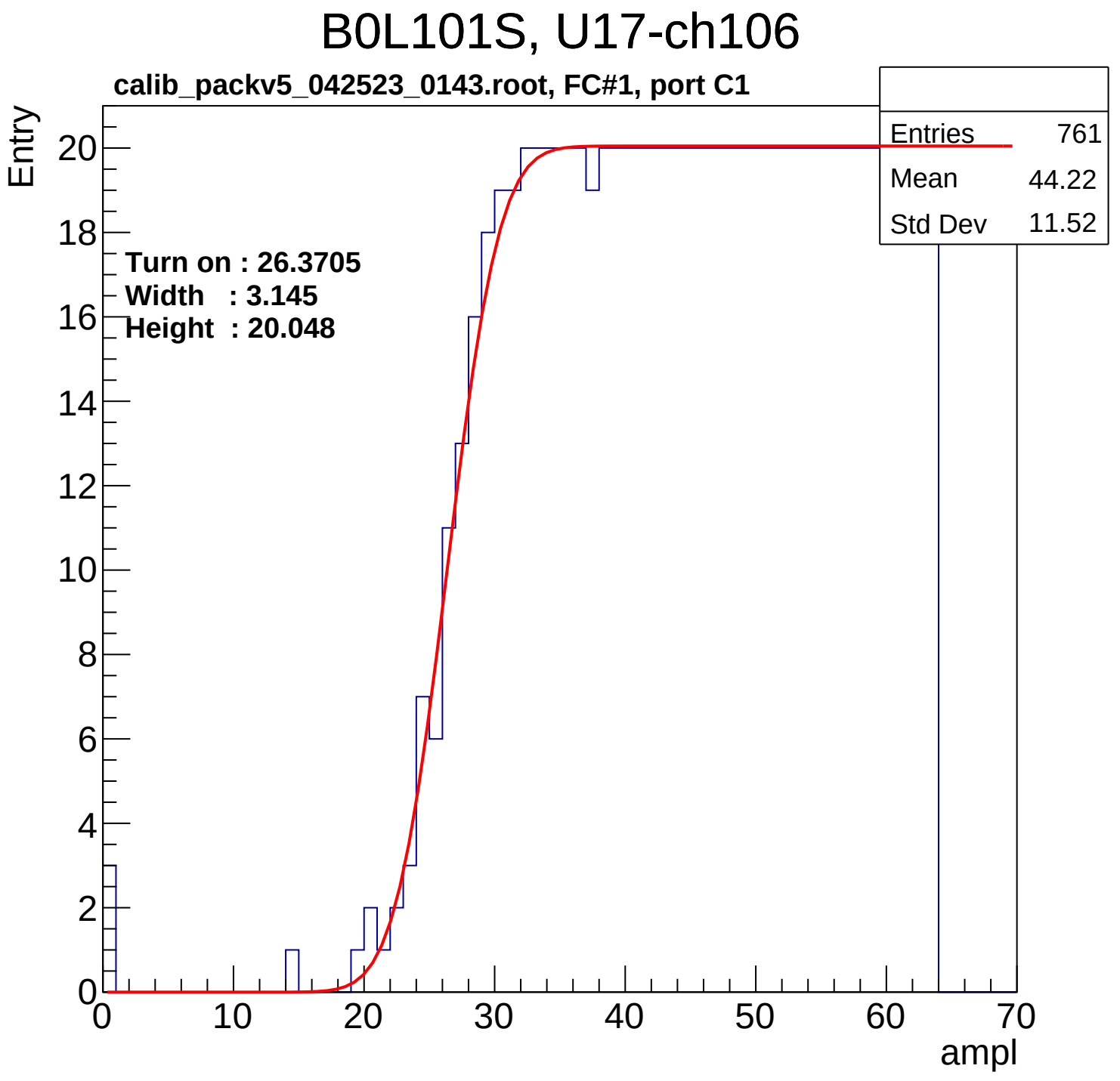
B0L101S, U17-ch106
calib_packv5_042523_0143.root, FC#1, port C1
Entries 761
Mean 44.22
Std Dev 11.52
Turn on : 26.3705
Width : 3.145
Height : 20.048
Entry
ampl
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8
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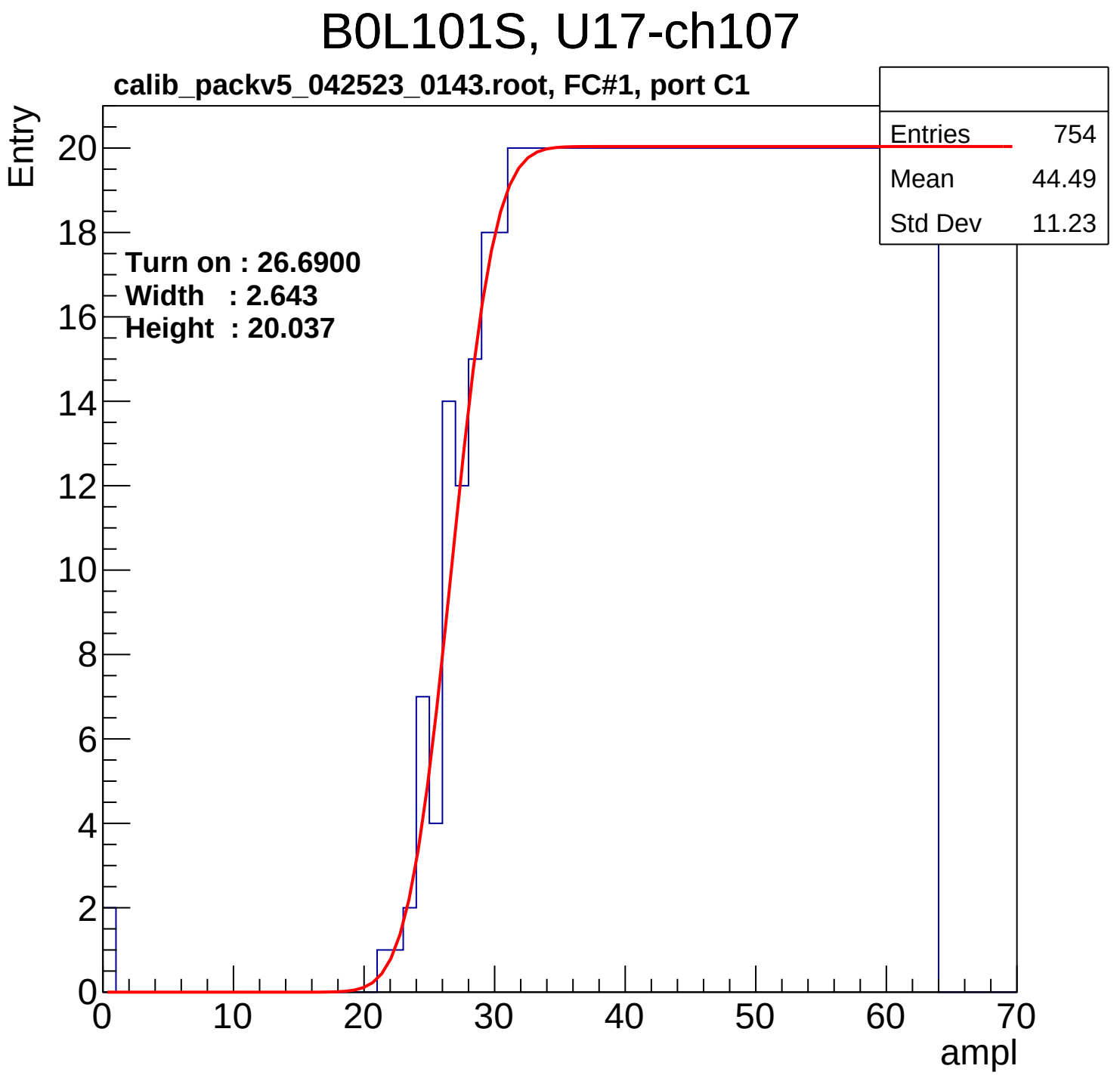
B0L101S, U17-ch107
calib_packv5_042523_0143.root, FC#1, port C1
Entries 754
Mean 44.49
Std Dev 11.23
Turn on : 26.6900
Width : 2.643
Height : 20.037
Entry
ampl
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8
10
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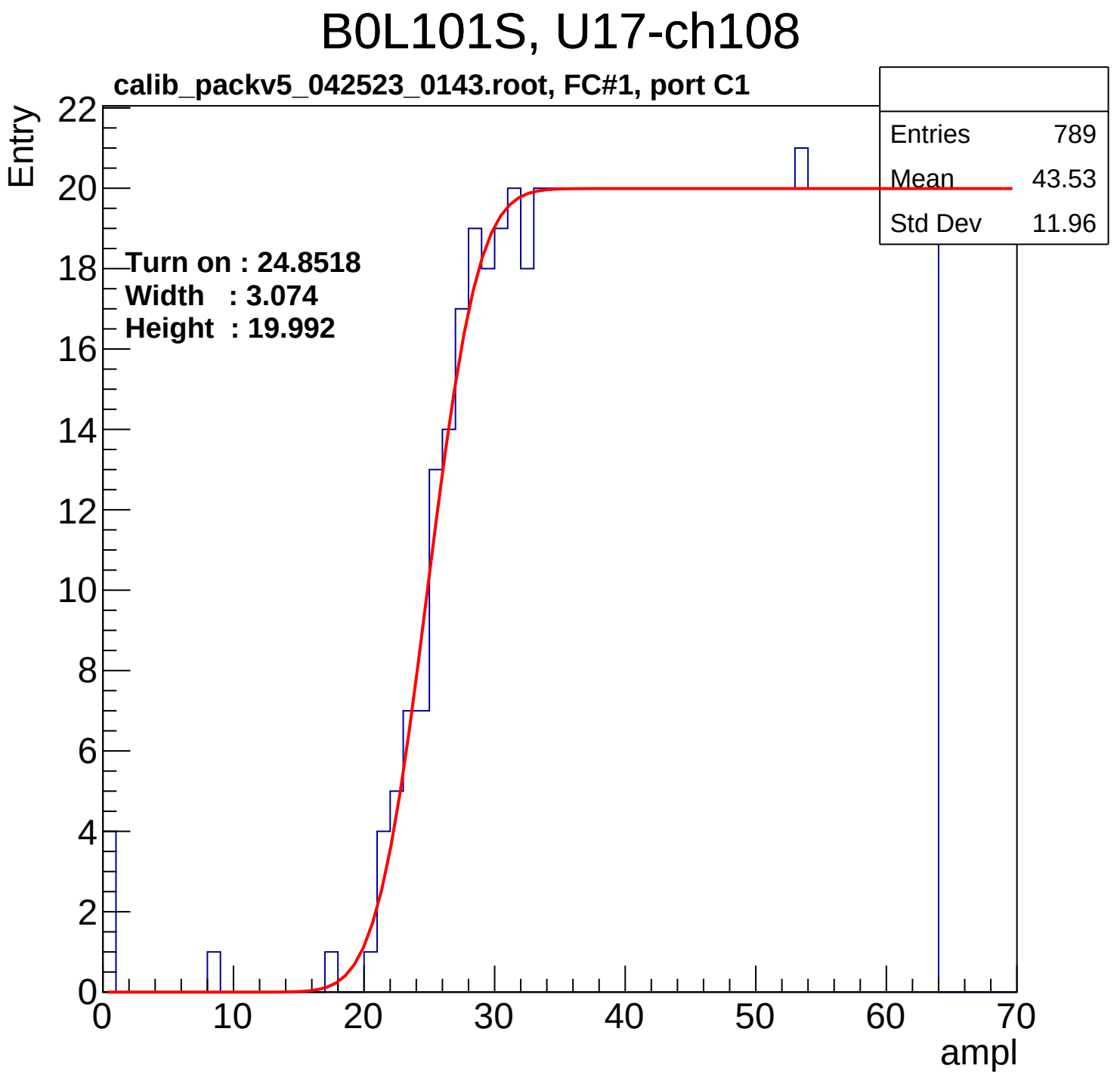
B0L101S, U17-ch108
calib_packv5_042523_0143.root, FC#1, port C1
Entries 789
Mean 43.53
Std Dev 11.96
Turn on : 24.8518
Width : 3.074
Height : 19.992
Entry
ampl
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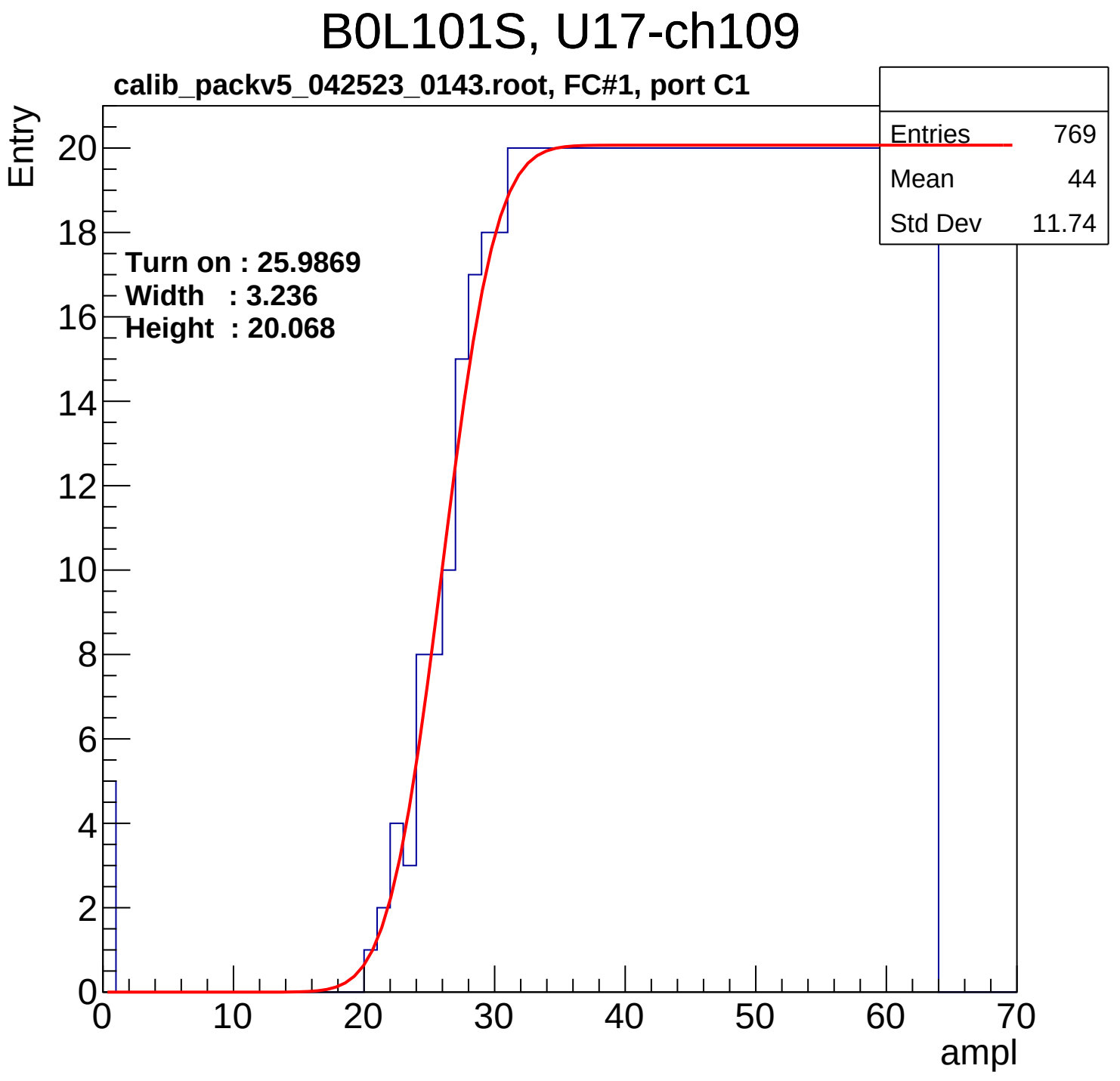
B0L101S, U17-ch109
calib_packv5_042523_0143.root, FC#1, port C1
Entries 769
Mean 44
Std Dev 11.74
Turn on : 25.9869
Width : 3.236
Height : 20.068
Entry
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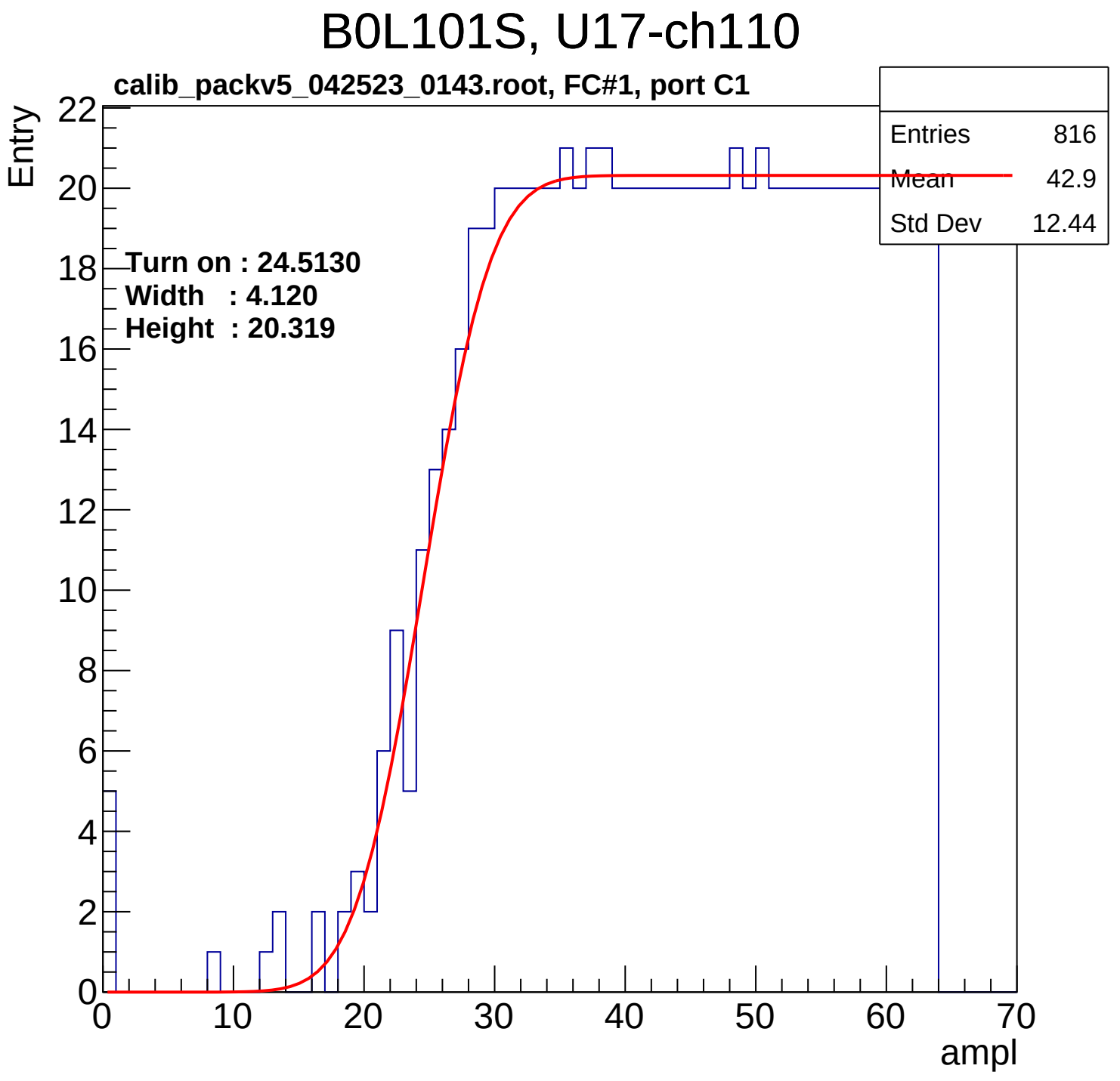
B0L101S, U17-ch110
calib_packv5_042523_0143.root, FC#1, port C1
Entries 816
Mean 42.9
Std Dev 12.44
Turn on : 24.5130
Width : 4.120
Height : 20.319
Entry
ampl
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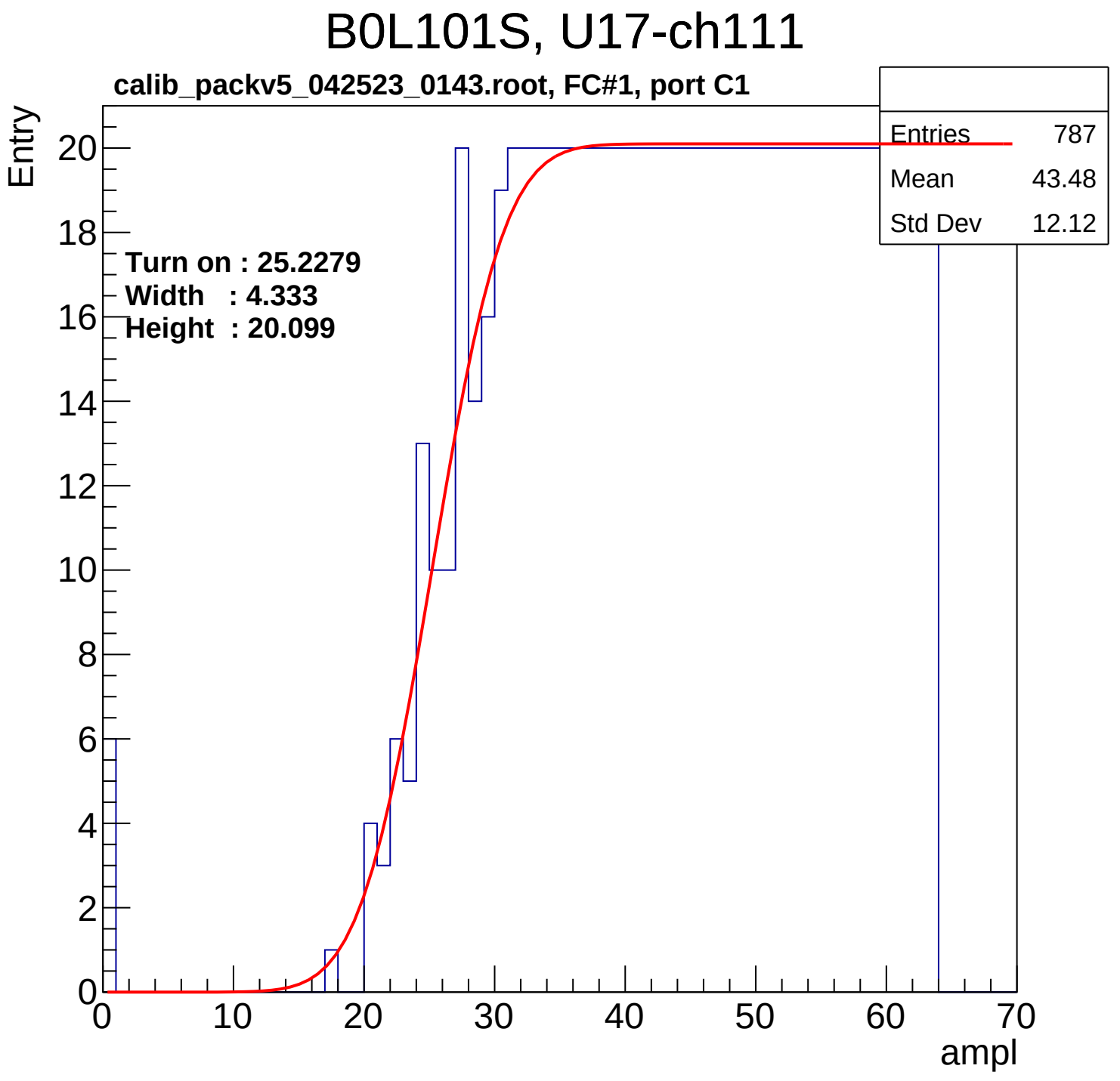
B0L101S, U17-ch111
calib_packv5_042523_0143.root, FC#1, port C1
Entries 787
Mean 43.48
Std Dev 12.12
Turn on : 25.2279
Width : 4.333
Height : 20.099
Entry
ampl
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6
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10
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20
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10
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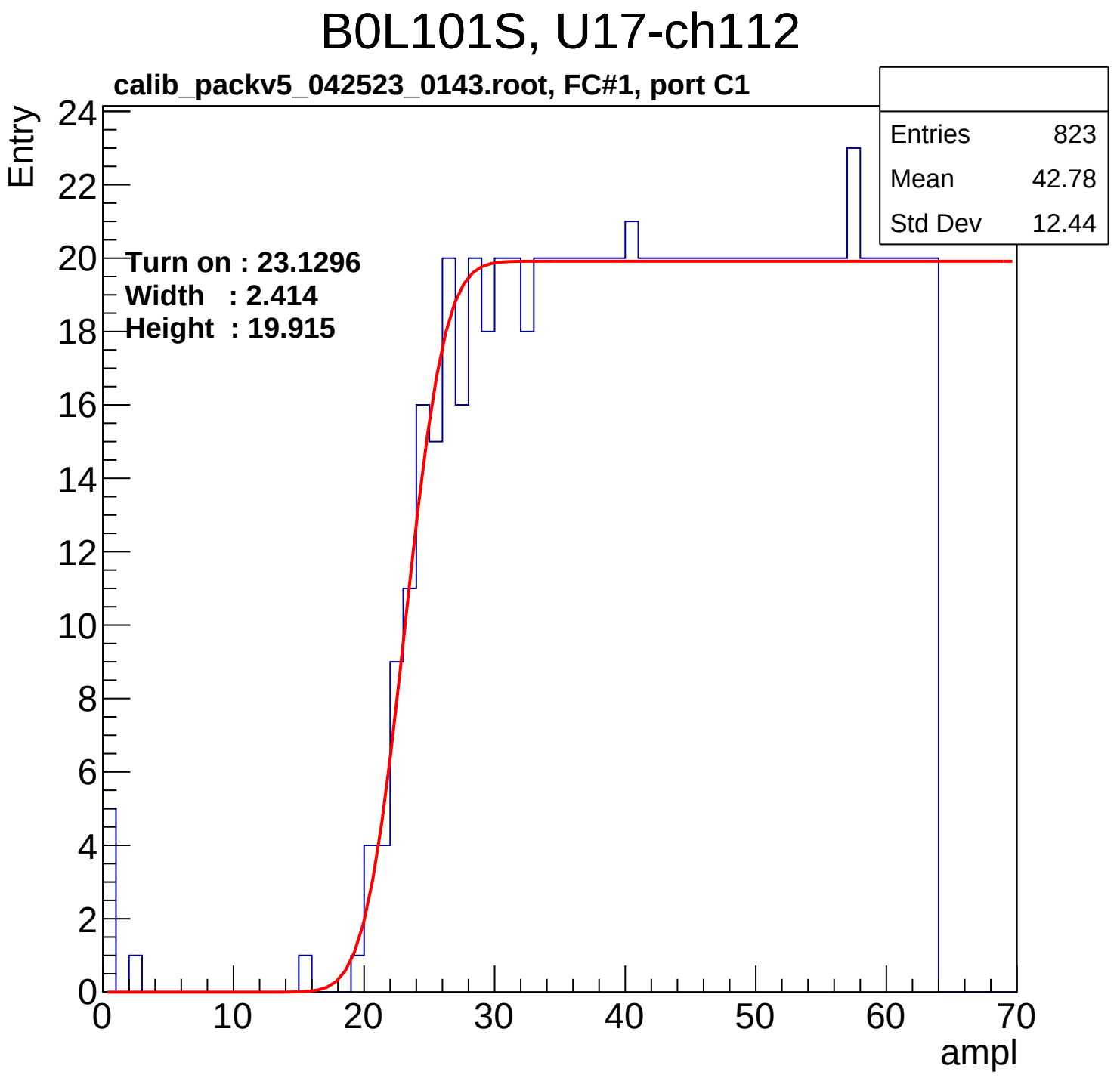
B0L101S, U17-ch112
calib_packv5_042523_0143.root, FC#1, port C1
Entries 823
Mean 42.78
Std Dev 12.44
Turn on : 23.1296
Width : 2.414
Height : 19.915
Entry
ampl
0
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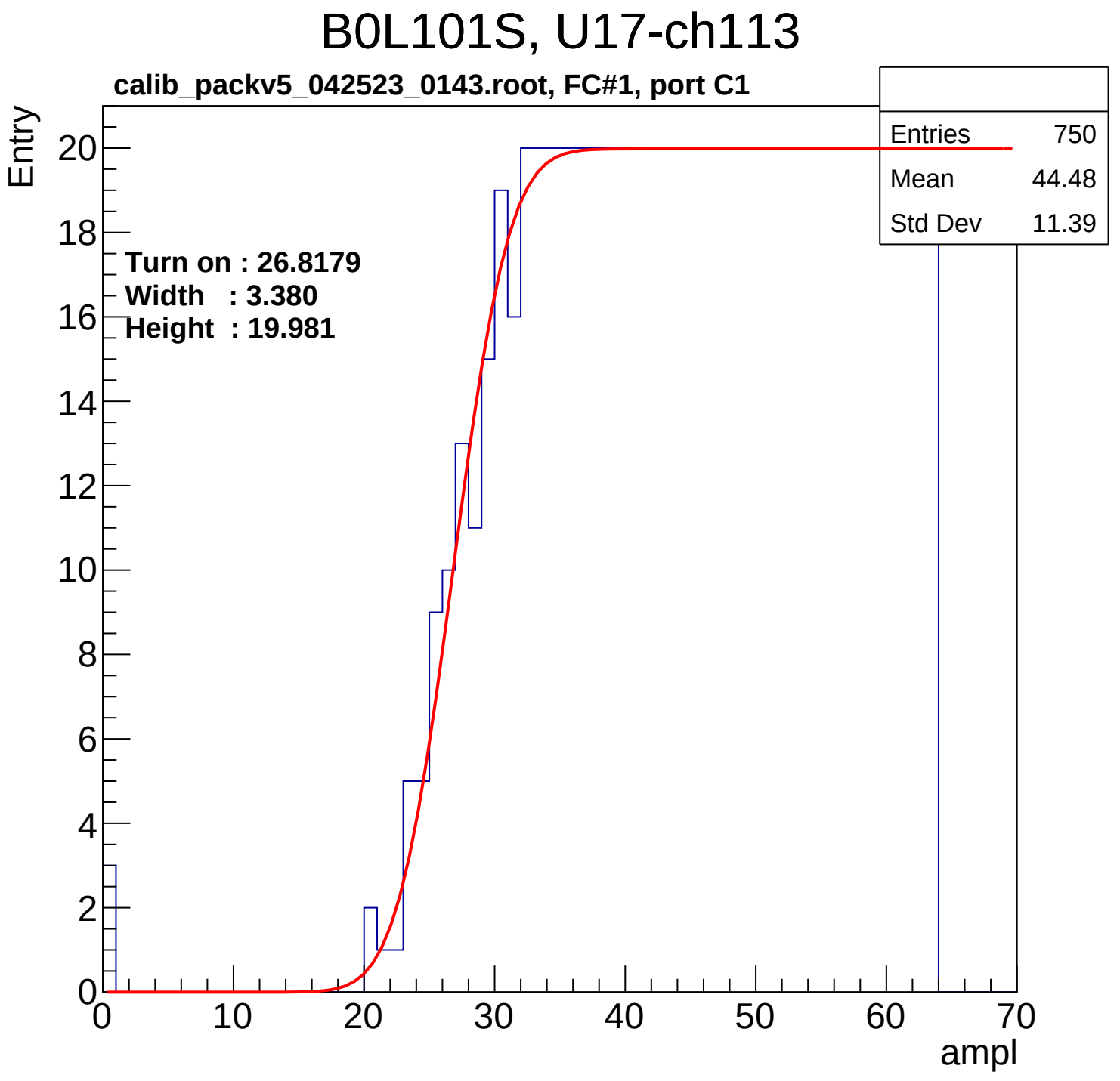
B0L101S, U17-ch113
calib_packv5_042523_0143.root, FC#1, port C1
Entries 750
Mean 44.48
Std Dev 11.39
Turn on : 26.8179
Width : 3.380
Height : 19.981
Entry
ampl
0
2
4
6
8
10
12
14
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18
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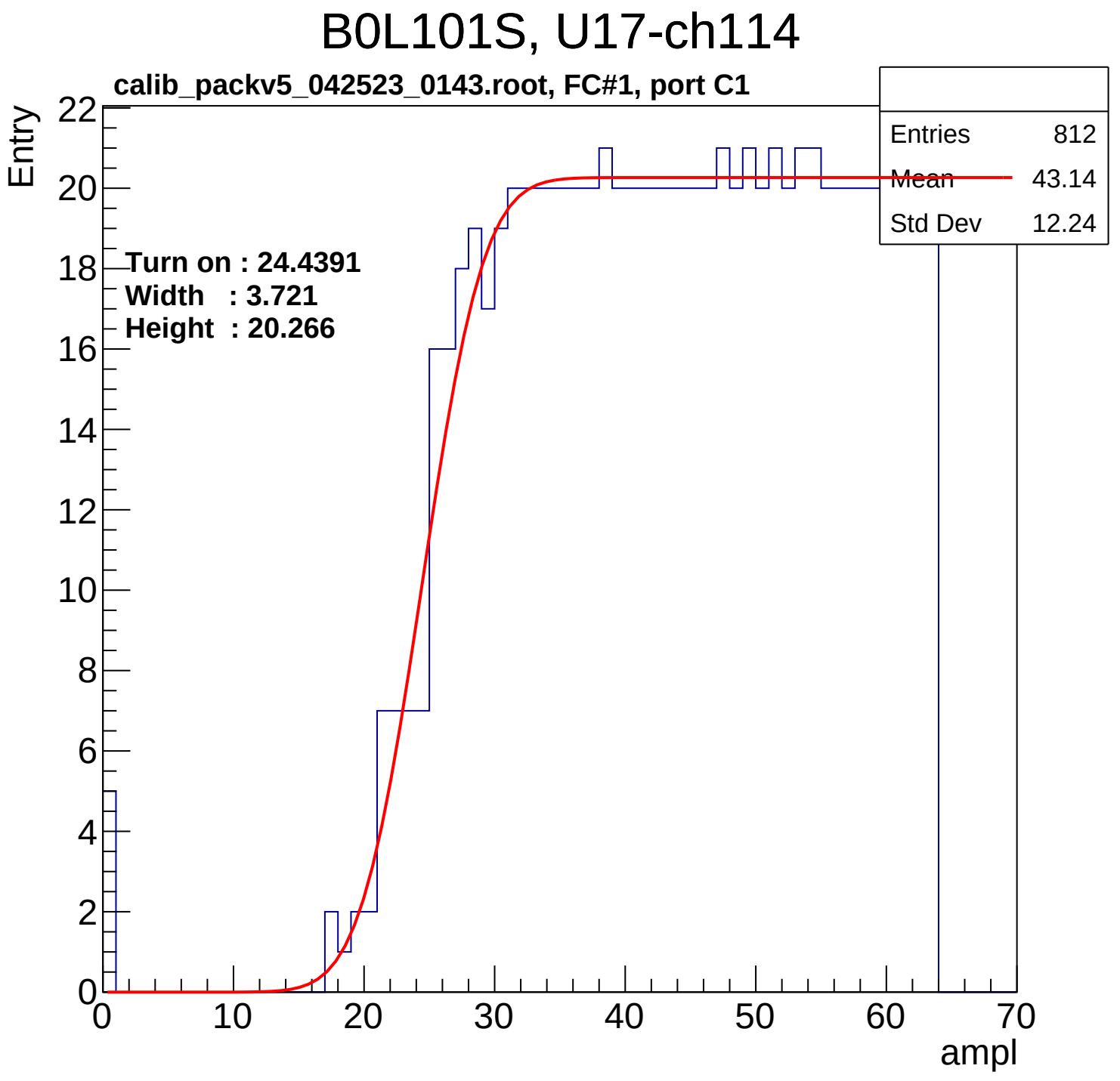
B0L101S, U17-ch114
calib_packv5_042523_0143.root, FC#1, port C1
Entries 812
Mean 43.14
Std Dev 12.24
Turn on : 24.4391
Width : 3.721
Height : 20.266
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
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0
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20
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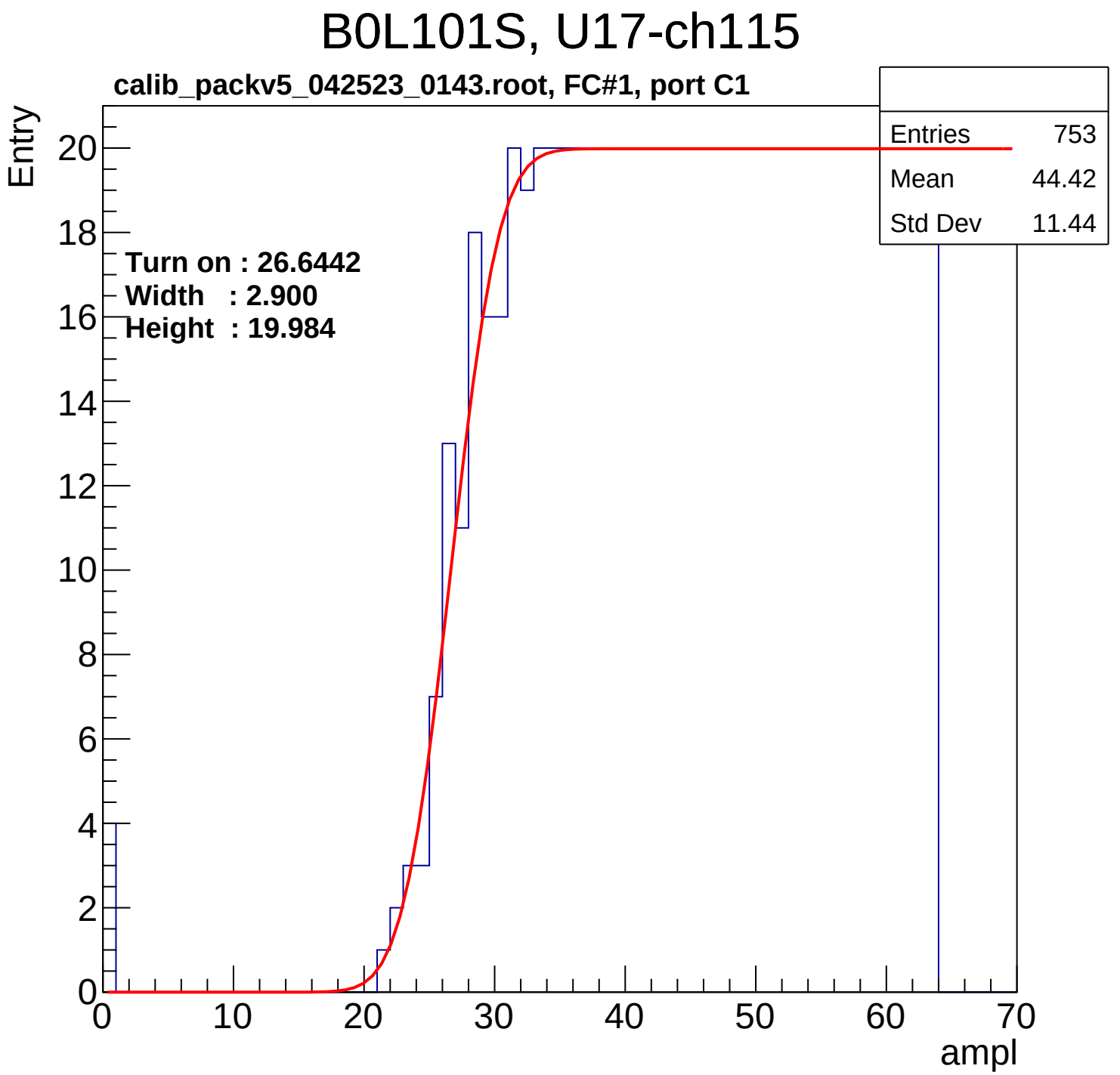
B0L101S, U17-ch115
calib_packv5_042523_0143.root, FC#1, port C1
Entries 753
Mean 44.42
Std Dev 11.44
Turn on : 26.6442
Width : 2.900
Height : 19.984
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
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20
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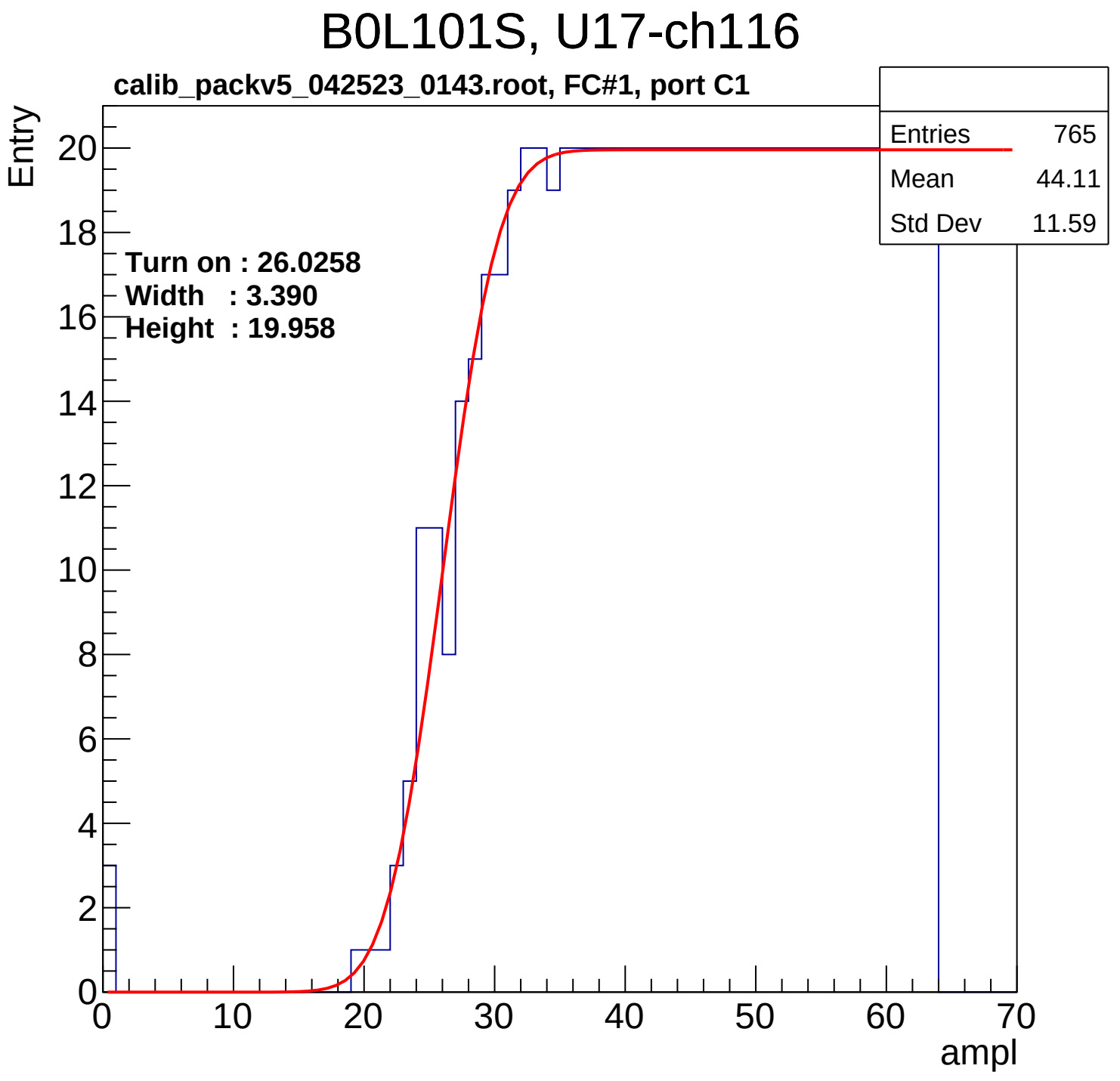
B0L101S, U17-ch116
calib_packv5_042523_0143.root, FC#1, port C1
Entries 765
Mean 44.11
Std Dev 11.59
Turn on : 26.0258
Width : 3.390
Height : 19.958
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
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20
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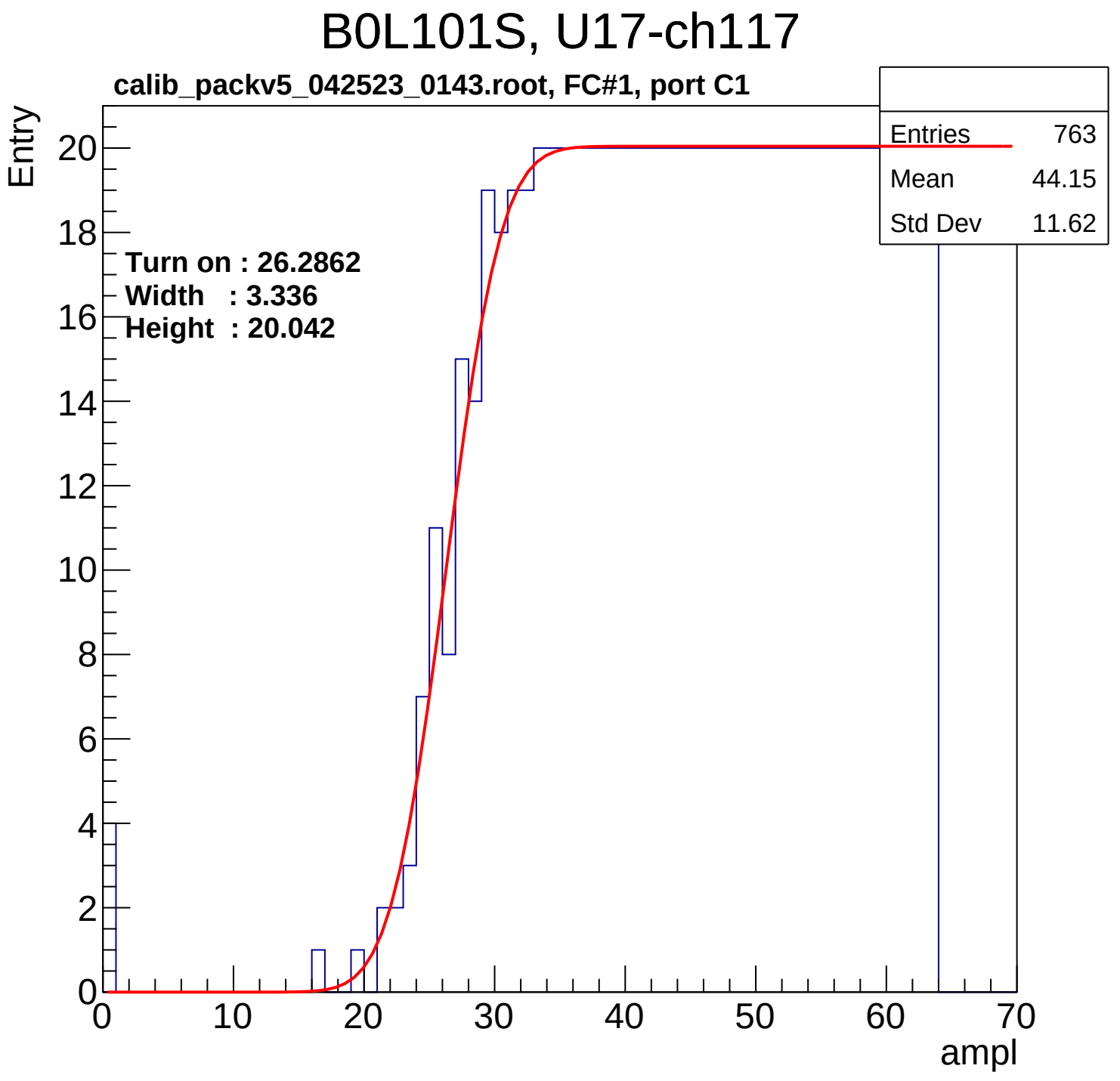
B0L101S, U17-ch117
calib_packv5_042523_0143.root, FC#1, port C1
Entries 763
Mean 44.15
Std Dev 11.62
Turn on : 26.2862
Width : 3.336
Height : 20.042
Entry
ampl
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6
8
10
12
14
16
18
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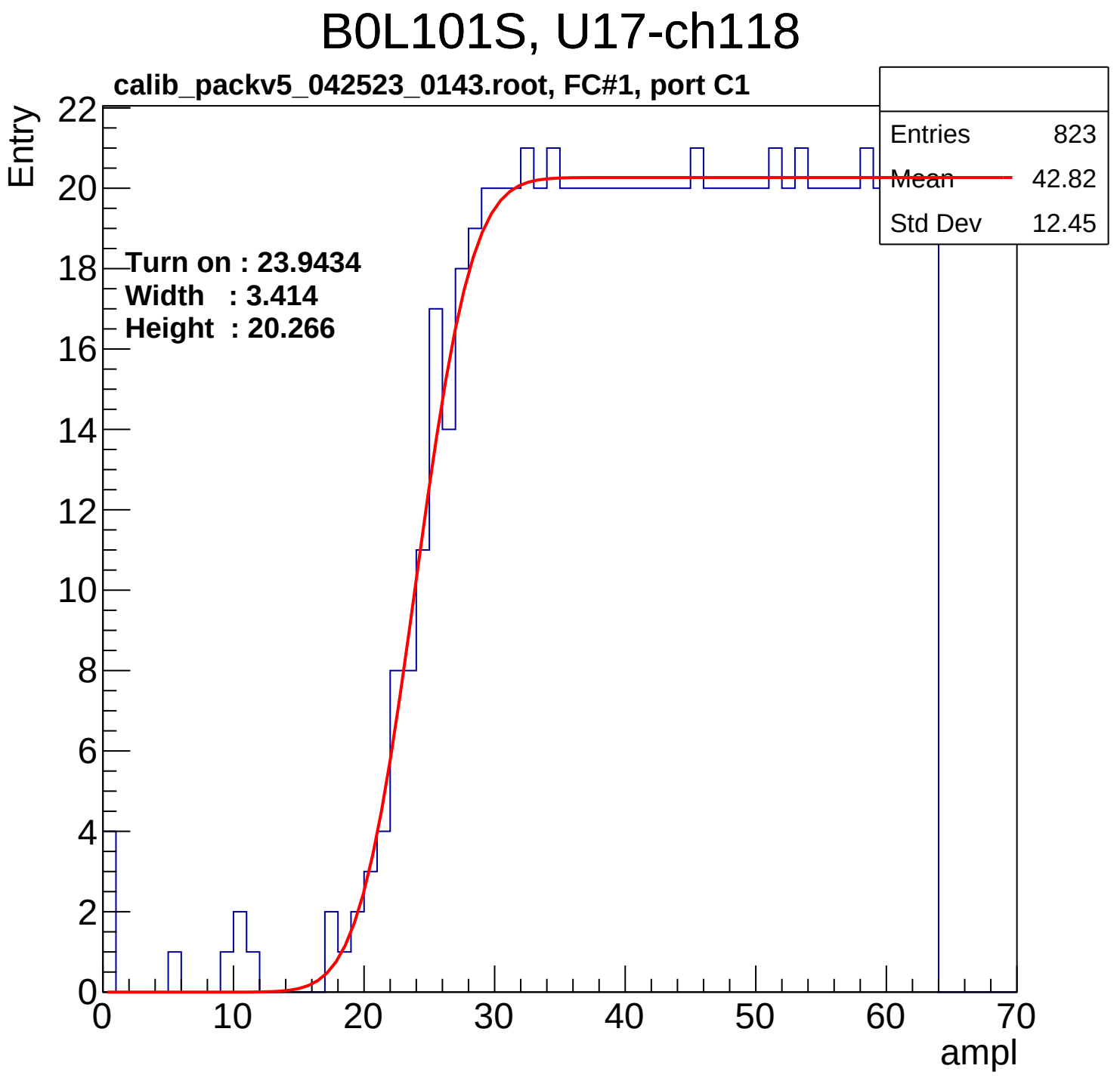
B0L101S, U17-ch118
calib_packv5_042523_0143.root, FC#1, port C1
Entries 823
Mean 42.82
Std Dev 12.45
Turn on : 23.9434
Width : 3.414
Height : 20.266
Entry
ampl
0
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6
8
10
12
14
16
18
20
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0
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20
30
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60
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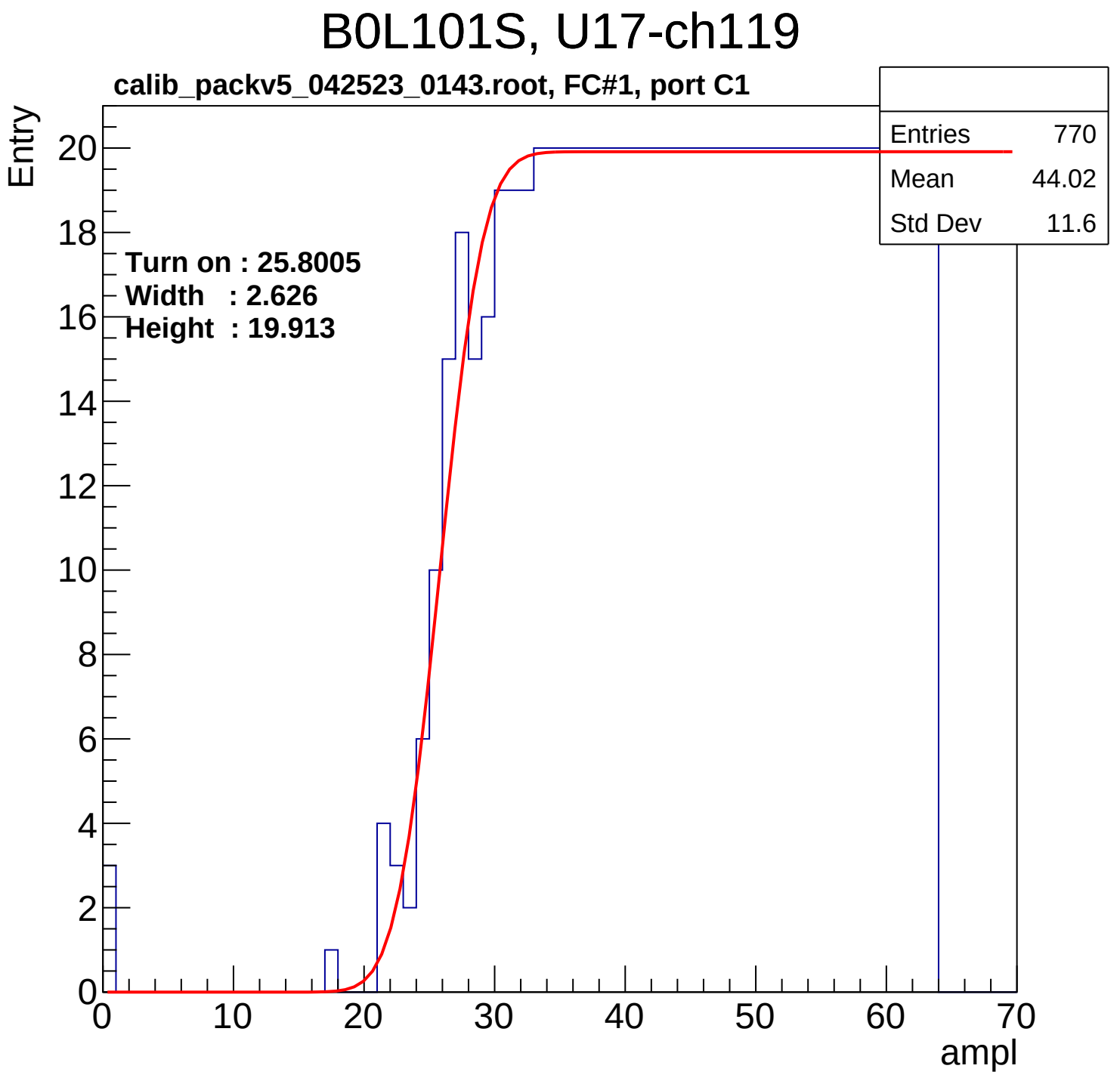
B0L101S, U17-ch119
calib_packv5_042523_0143.root, FC#1, port C1
Entries 770
Mean 44.02
Std Dev 11.6
Turn on : 25.8005
Width : 2.626
Height : 19.913
Entry
ampl
0
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4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
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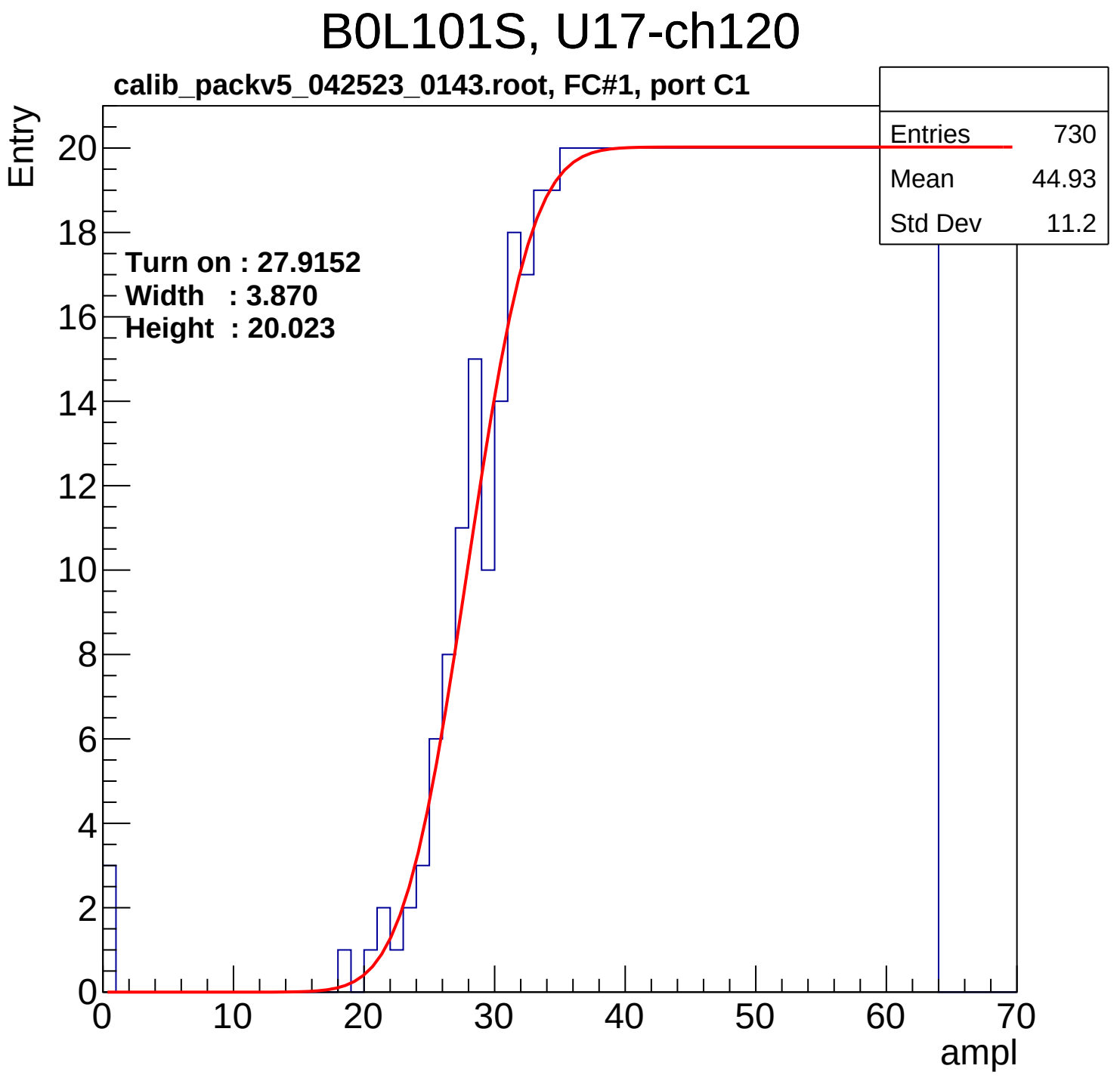
B0L101S, U17-ch120
calib_packv5_042523_0143.root, FC#1, port C1
Entries 730
Mean 44.93
Std Dev 11.2
Turn on : 27.9152
Width : 3.870
Height : 20.023
Entry
ampl
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6
8
10
12
14
16
18
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0
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60
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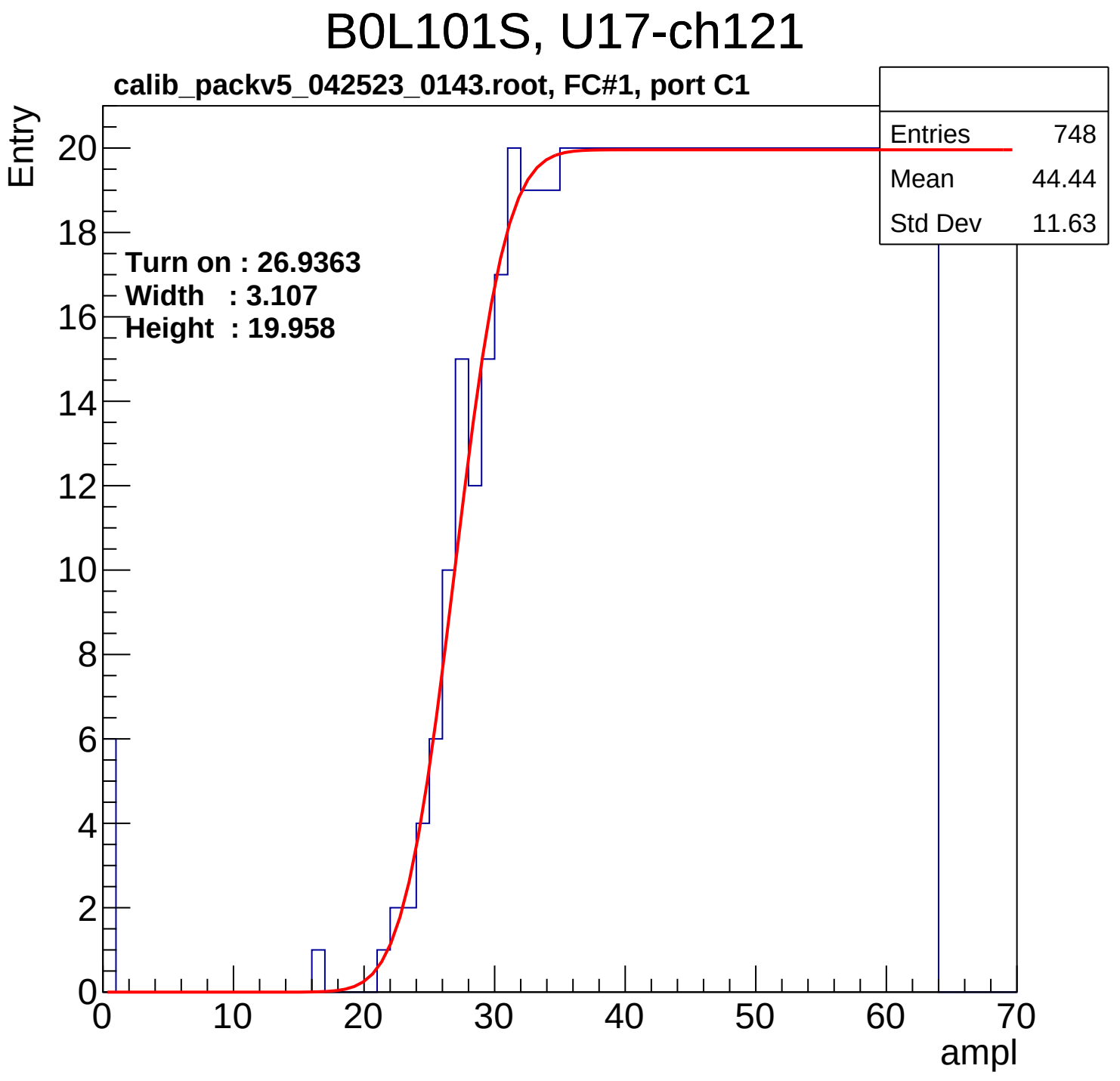
B0L101S, U17-ch121
calib_packv5_042523_0143.root, FC#1, port C1
Entries 748
Mean 44.44
Std Dev 11.63
Turn on : 26.9363
Width : 3.107
Height : 19.958
Entry
ampl
0
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4
6
8
10
12
14
16
18
20
0
10
20
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40
50
60
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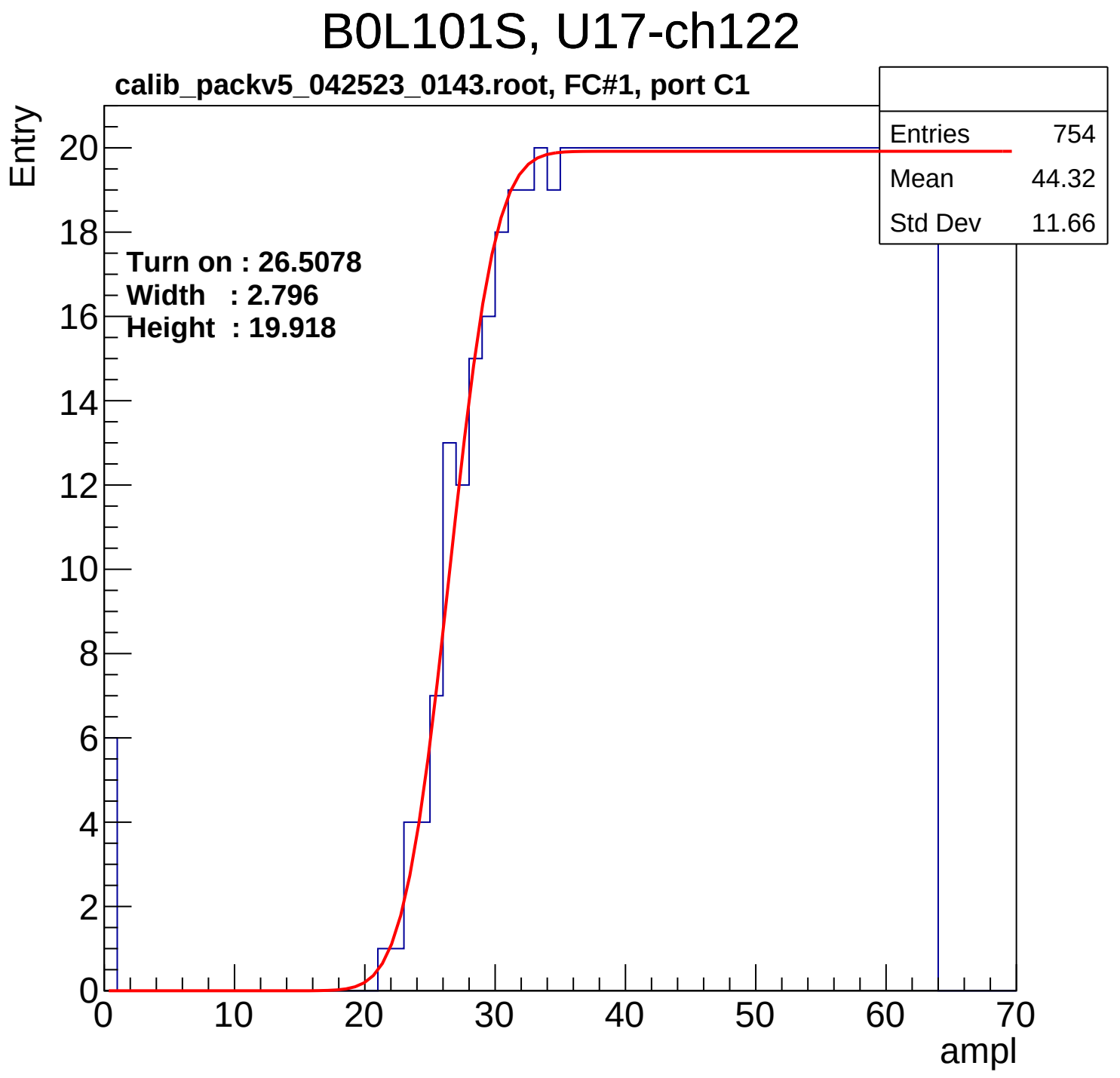
B0L101S, U17-ch122
calib_packv5_042523_0143.root, FC#1, port C1
Entries 754
Mean 44.32
Std Dev 11.66
Turn on : 26.5078
Width : 2.796
Height : 19.918
Entry
ampl
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4
6
8
10
12
14
16
18
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0
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20
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60
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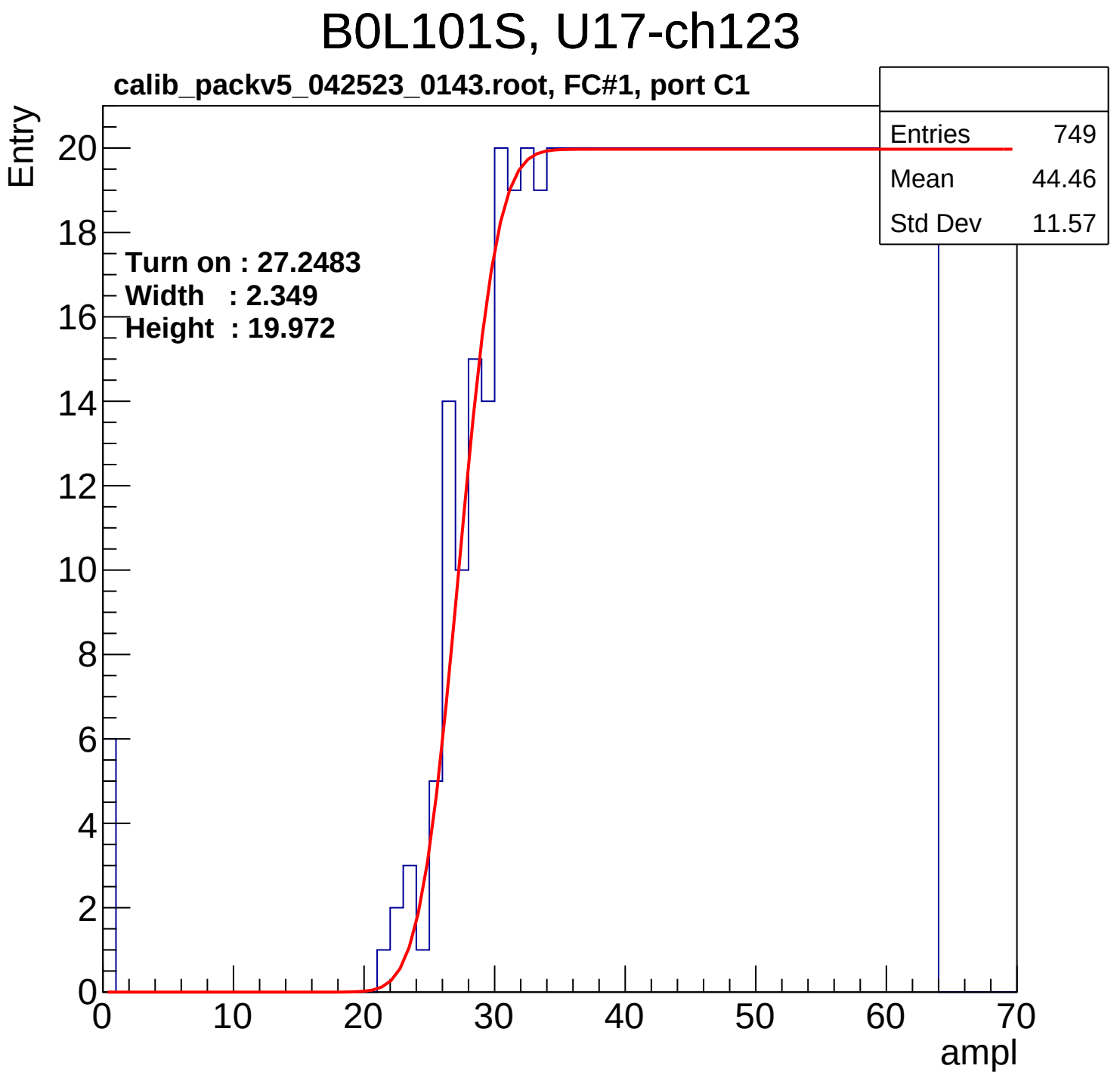
B0L101S, U17-ch123
calib_packv5_042523_0143.root, FC#1, port C1
Entries 749
Mean 44.46
Std Dev 11.57
Turn on : 27.2483
Width : 2.349
Height : 19.972
Entry
ampl
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6
8
10
12
14
16
18
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0
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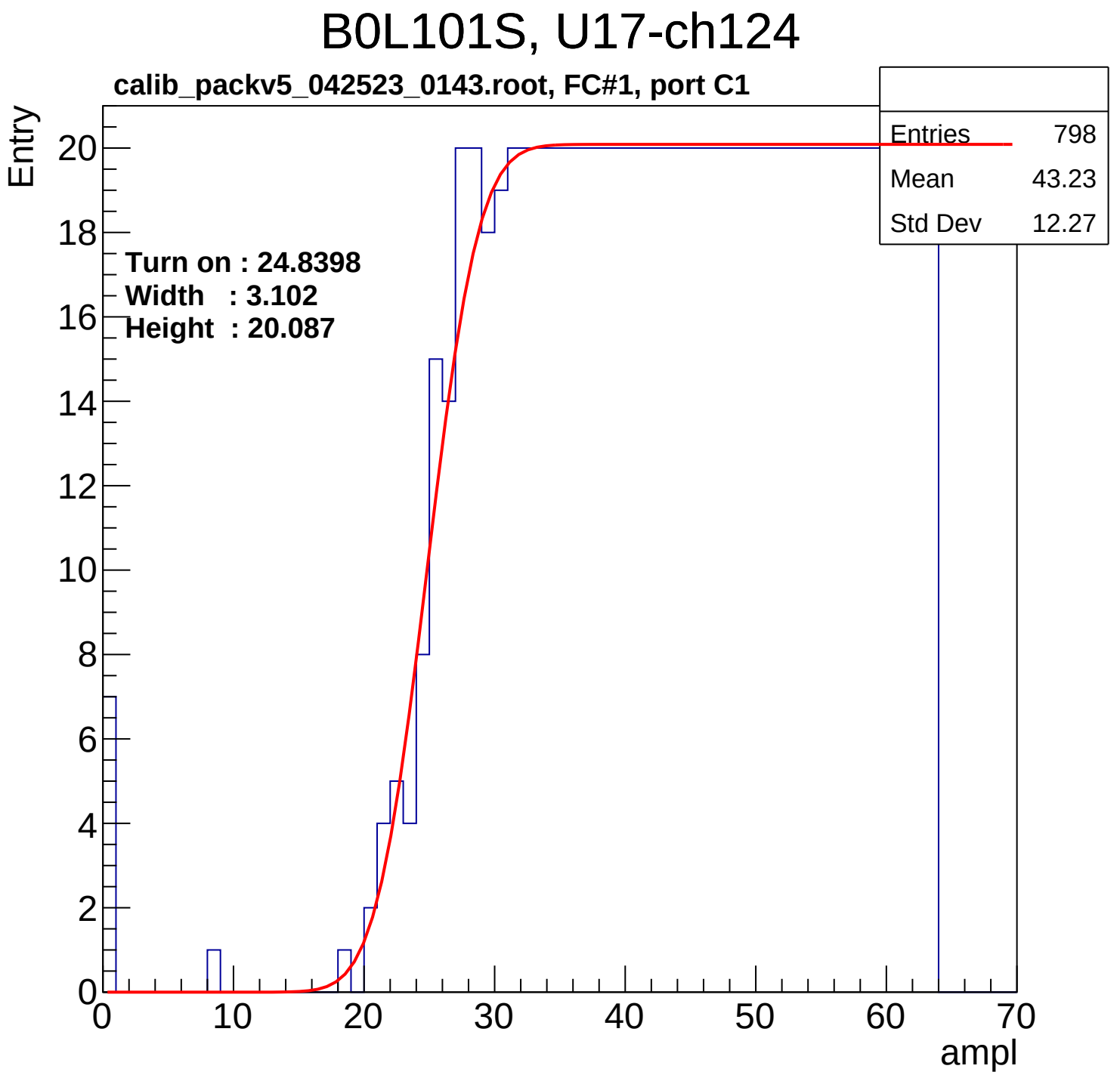
B0L101S, U17-ch124
calib_packv5_042523_0143.root, FC#1, port C1
Entries 798
Mean 43.23
Std Dev 12.27
Turn on : 24.8398
Width : 3.102
Height : 20.087
Entry
ampl
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6
8
10
12
14
16
18
20
0
10
20
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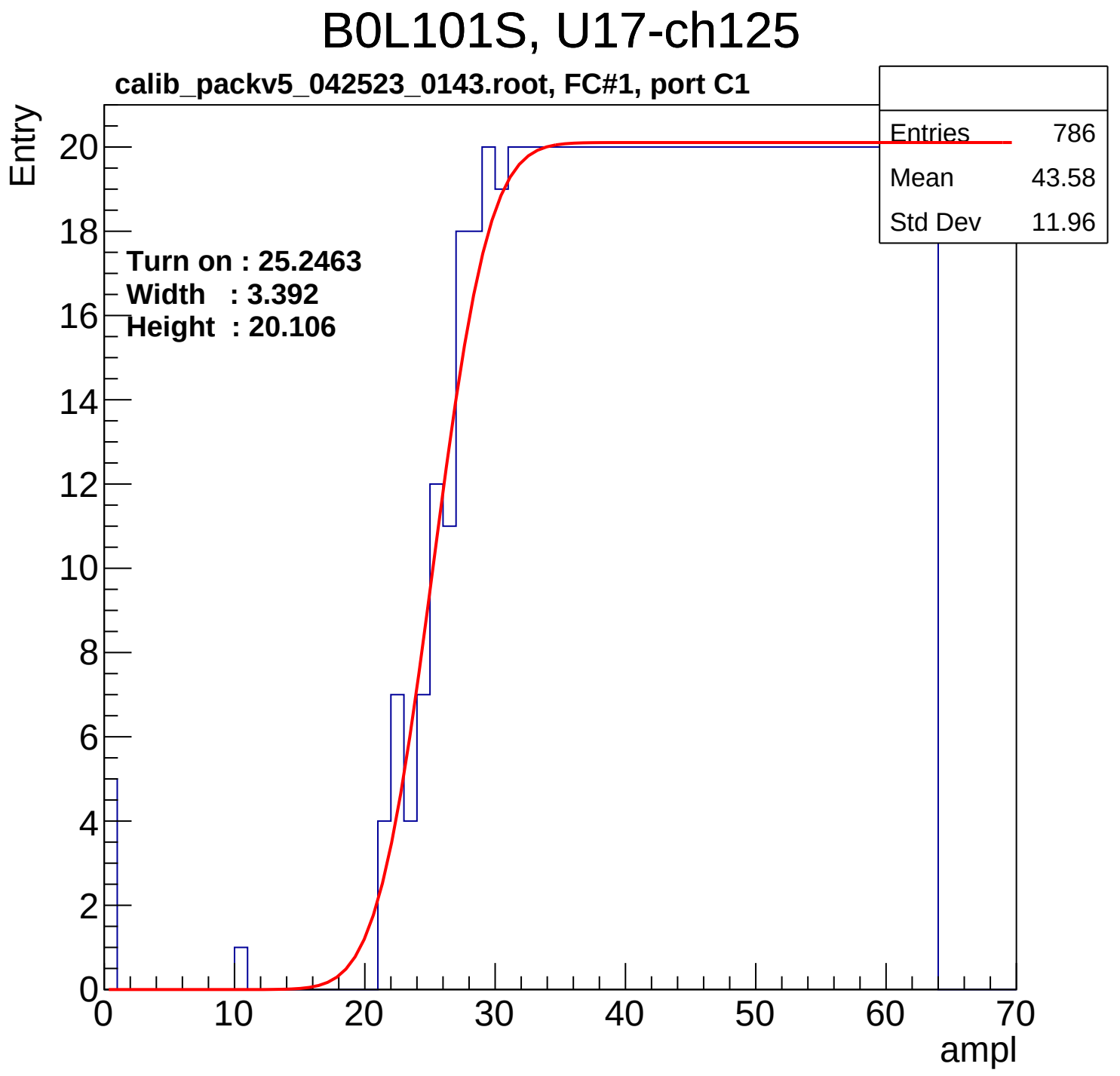
B0L101S, U17-ch125
calib_packv5_042523_0143.root, FC#1, port C1
Entries 786
Mean 43.58
Std Dev 11.96
Turn on : 25.2463
Width : 3.392
Height : 20.106
Entry
ampl
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6
8
10
12
14
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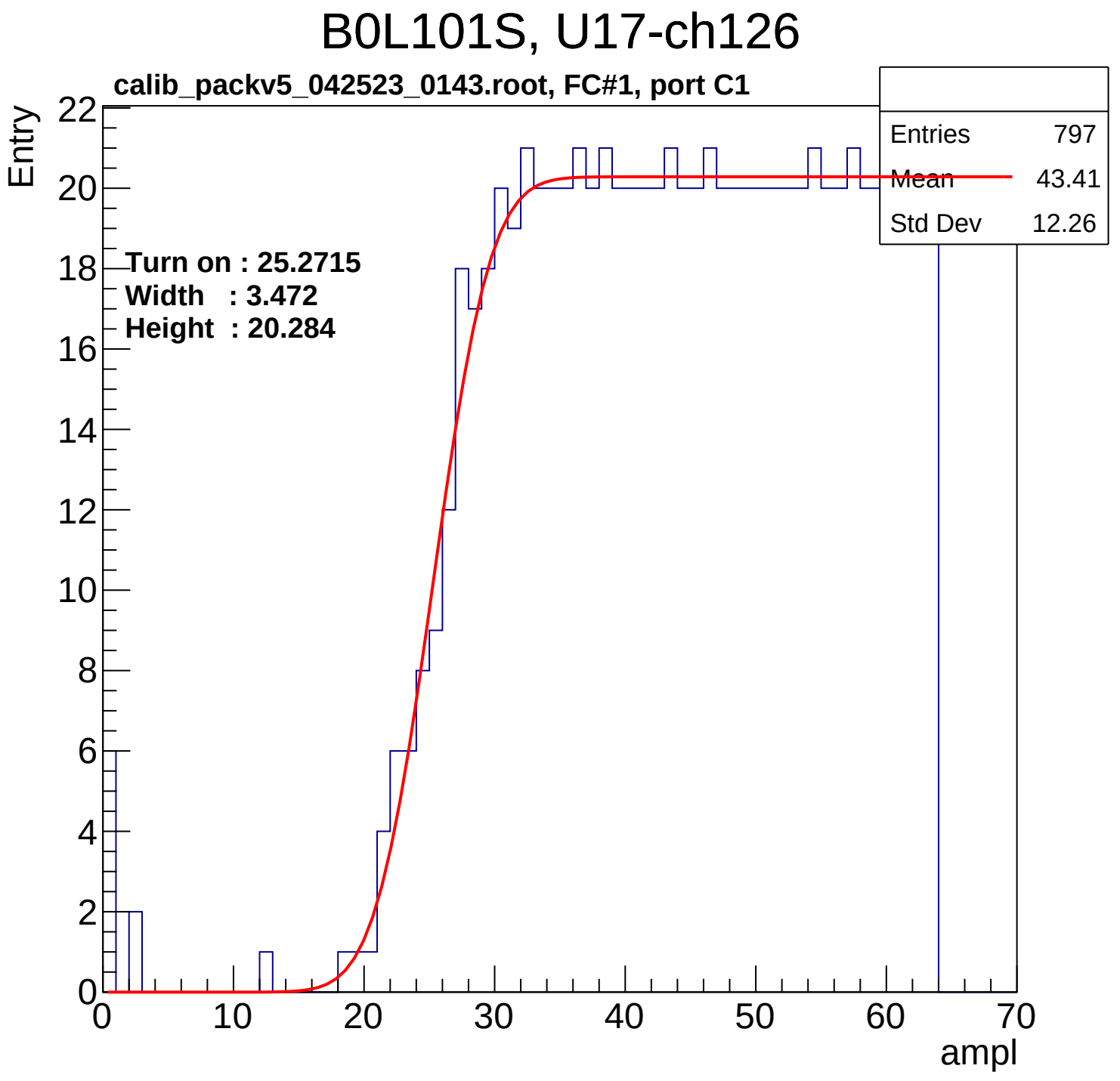
B0L101S, U17-ch126
calib_packv5_042523_0143.root, FC#1, port C1
Entries 797
Mean 43.41
Std Dev 12.26
Turn on : 25.2715
Width : 3.472
Height : 20.284
Entry
ampl
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8
10
12
14
16
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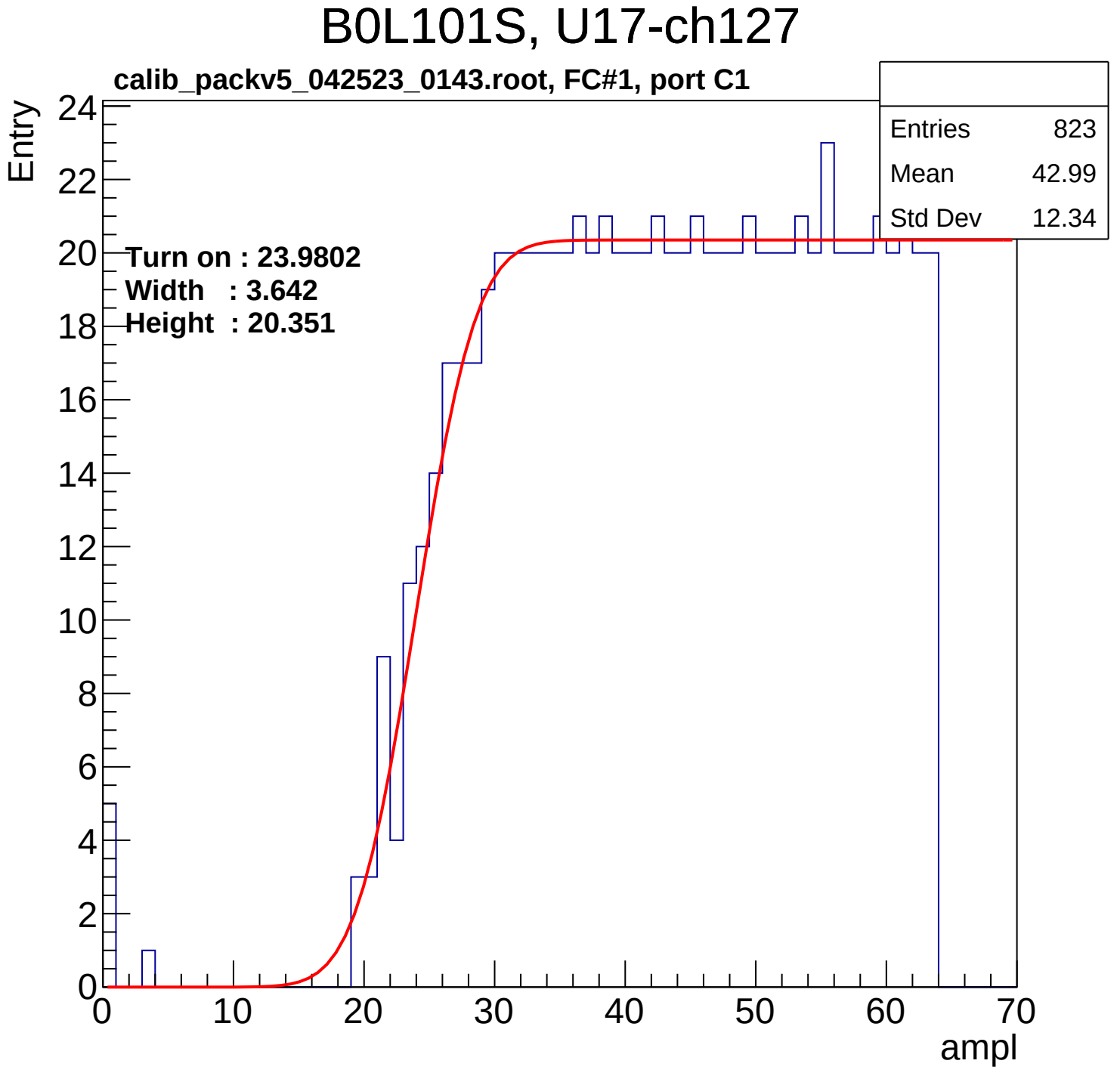
B0L101S, U17-ch127
calib_packv5_042523_0143.root, FC#1, port C1
Entries 823
Mean 42.99
Std Dev 12.34
Turn on : 23.9802
Width : 3.642
Height : 20.351
Entry
ampl
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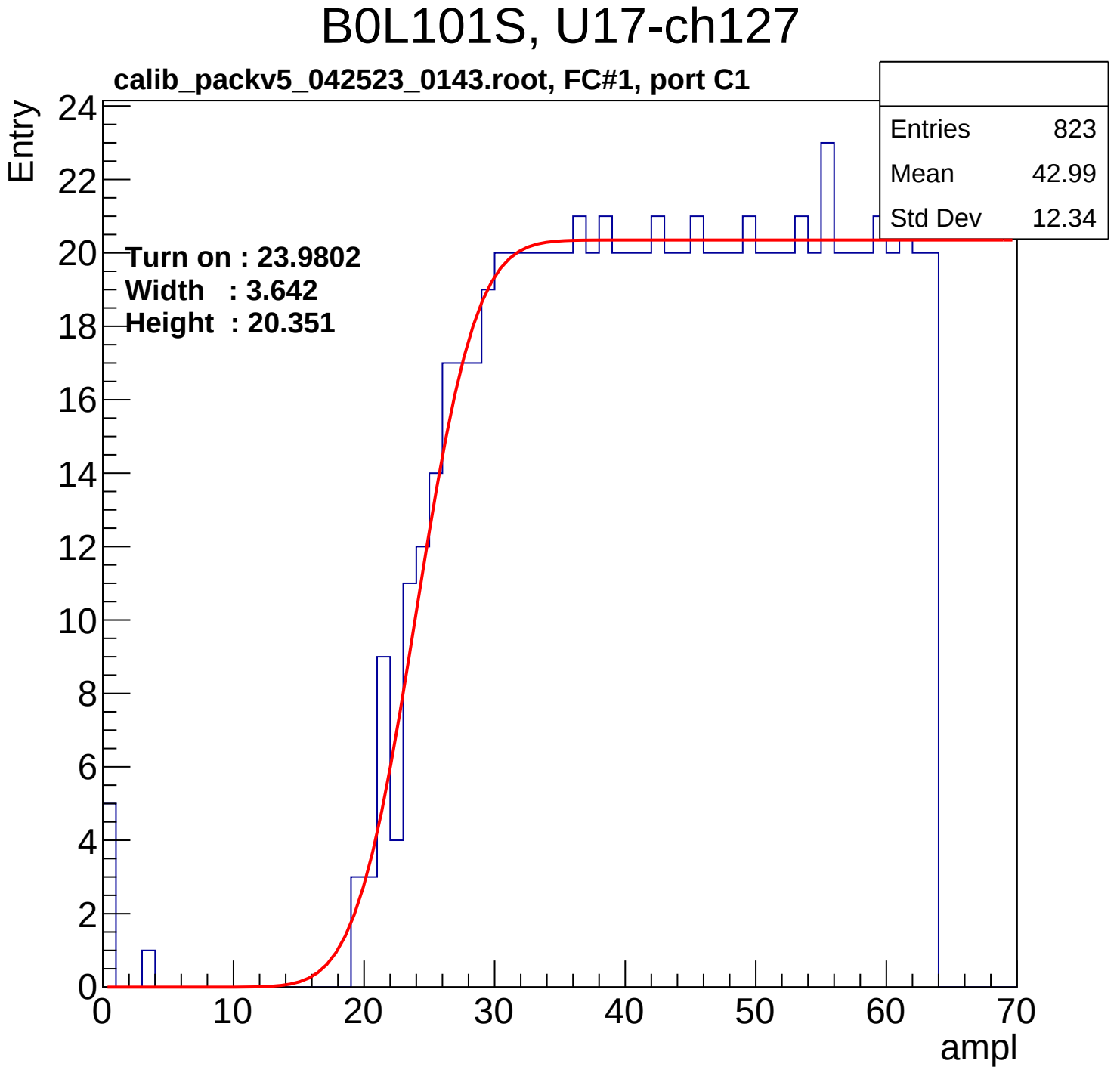
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calib_packv5_042523_0143.root, FC#1, port C1
Entries 823
Mean 42.99
Std Dev 12.34
Turn on : 23.9802
Width : 3.642
Height : 20.351
Entry
ampl
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