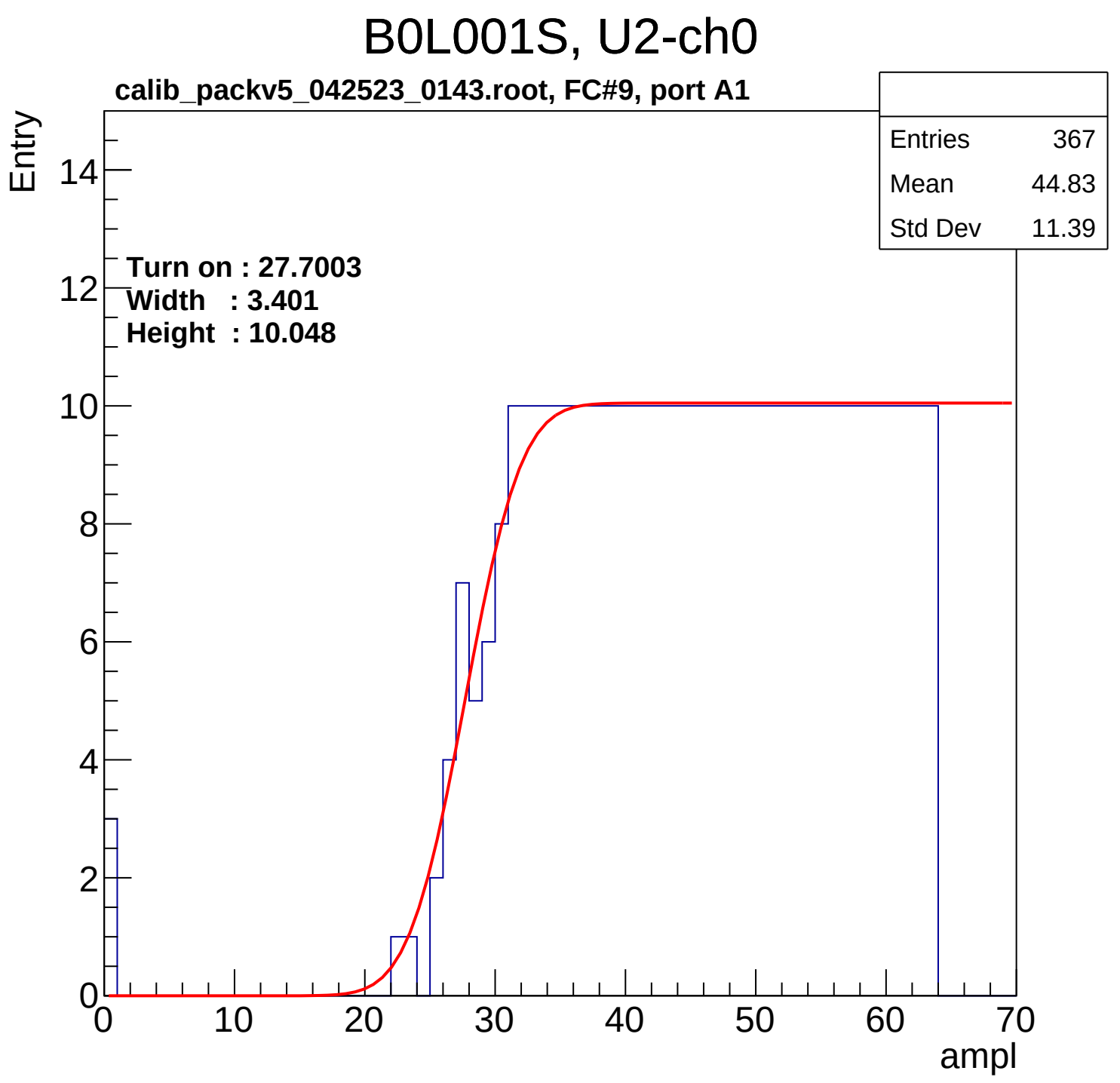
B0L001S, U2-ch0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.83
Std Dev 11.39
Turn on : 27.7003
Width : 3.401
Height : 10.048
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ampl
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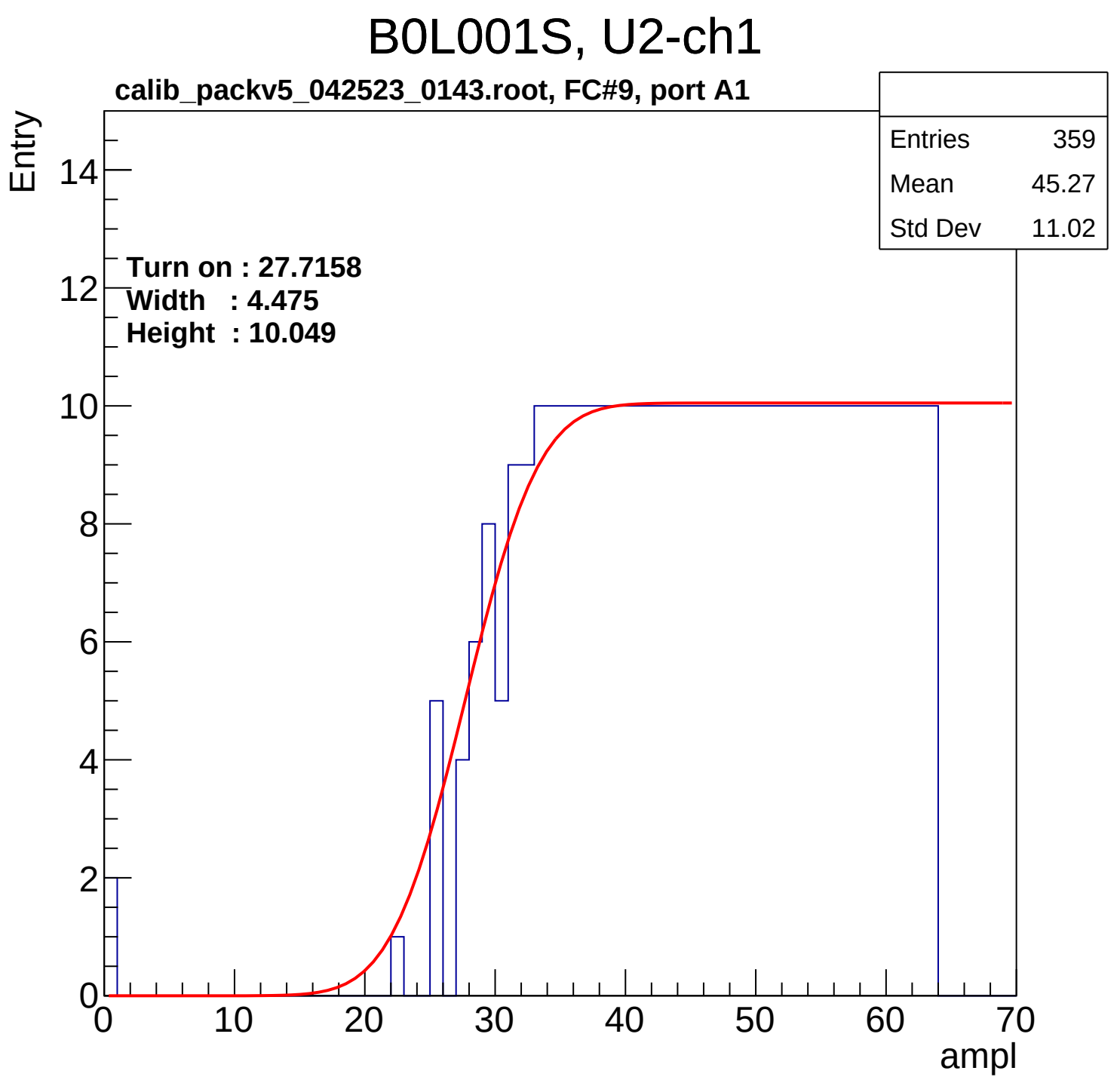
B0L001S, U2-ch1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 45.27
Std Dev 11.02
Turn on : 27.7158
Width : 4.475
Height : 10.049
Entry
ampl
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2
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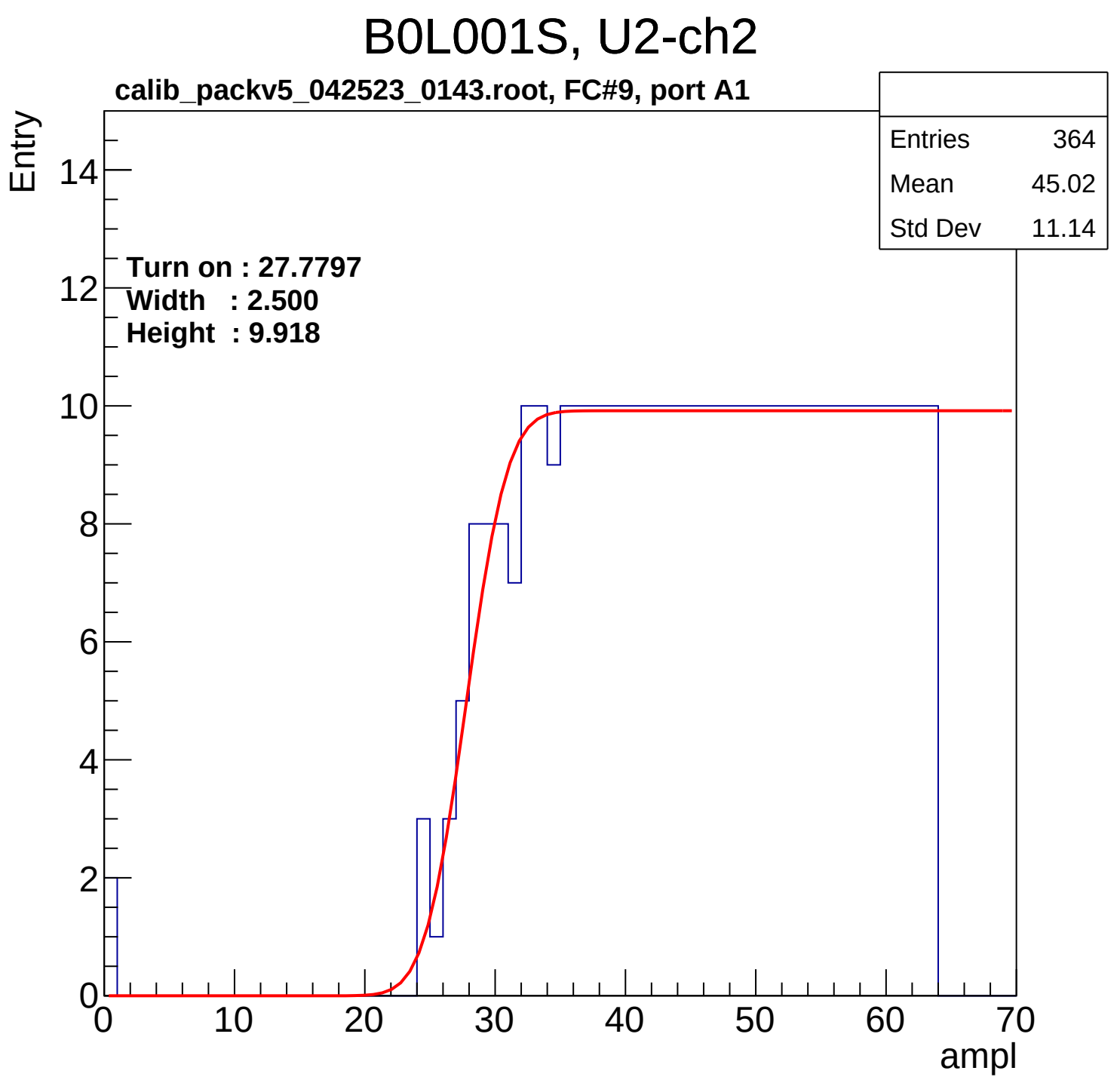
B0L001S, U2-ch2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 45.02
Std Dev 11.14
Turn on : 27.7797
Width : 2.500
Height : 9.918
Entry
ampl
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2
4
6
8
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0
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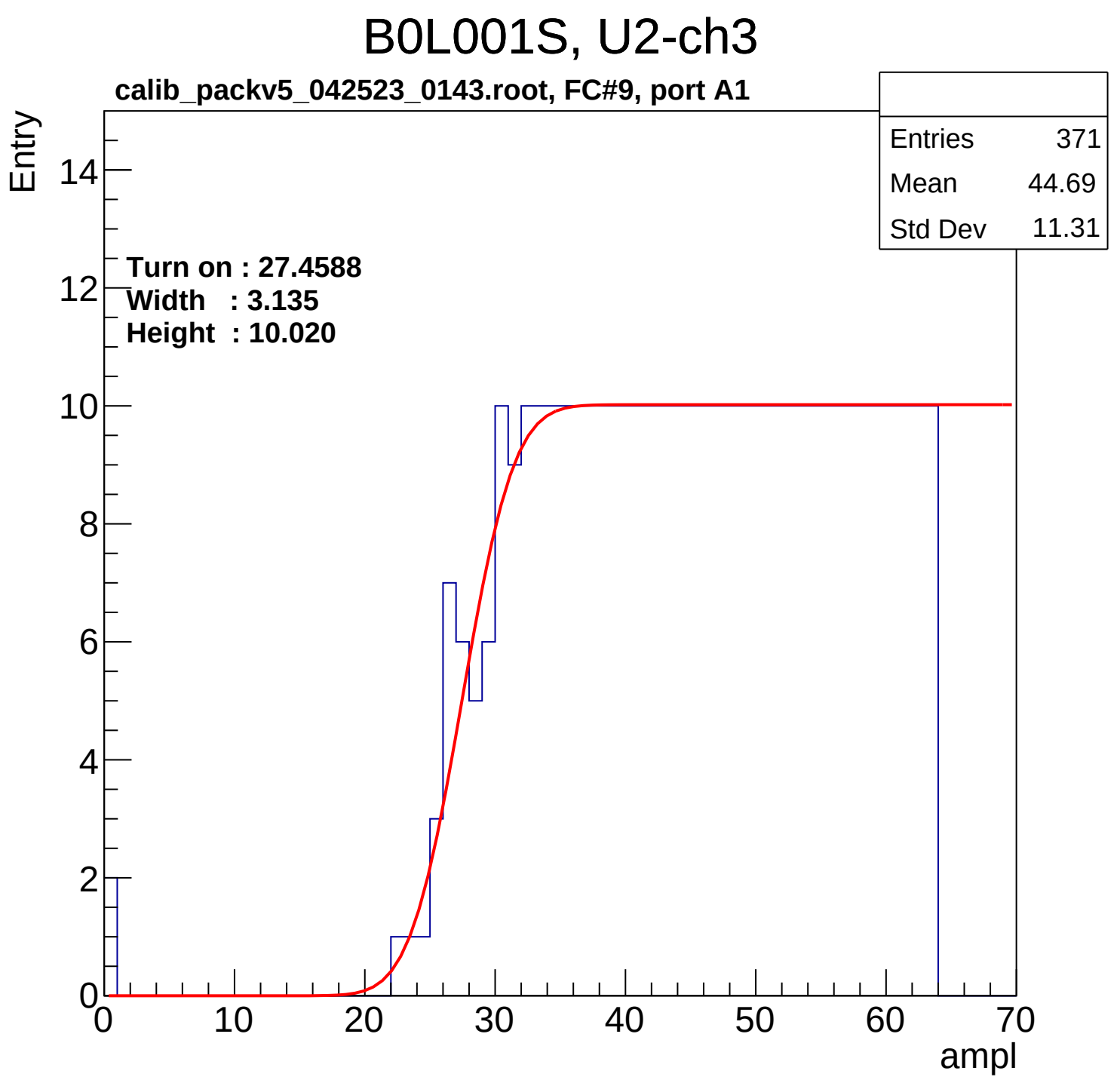
B0L001S, U2-ch3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 371
Mean 44.69
Std Dev 11.31
Turn on : 27.4588
Width : 3.135
Height : 10.020
Entry
ampl
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6
8
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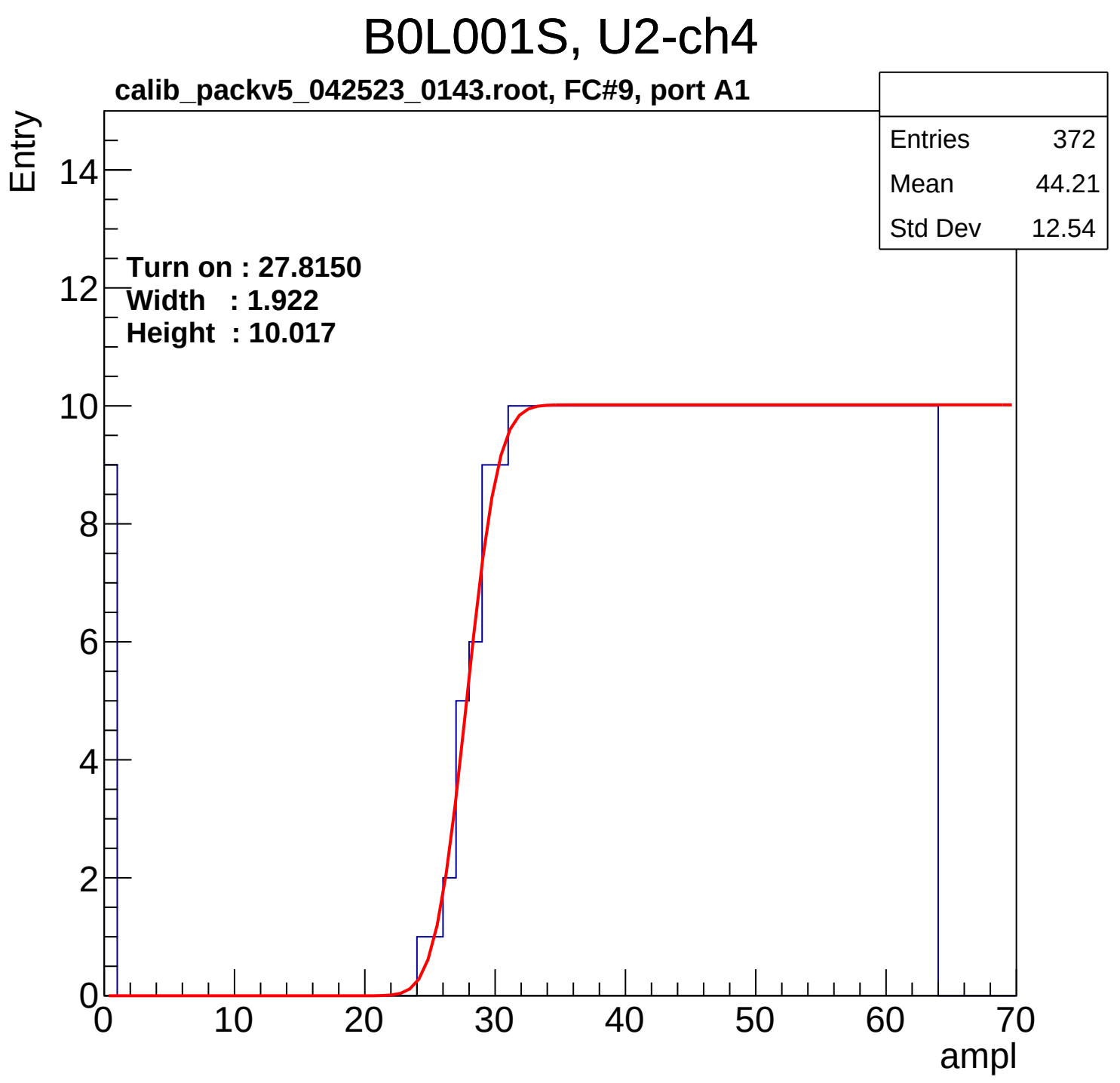
B0L001S, U2-ch4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 372
Mean 44.21
Std Dev 12.54
Turn on : 27.8150
Width : 1.922
Height : 10.017
Entry
ampl
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2
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6
8
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0
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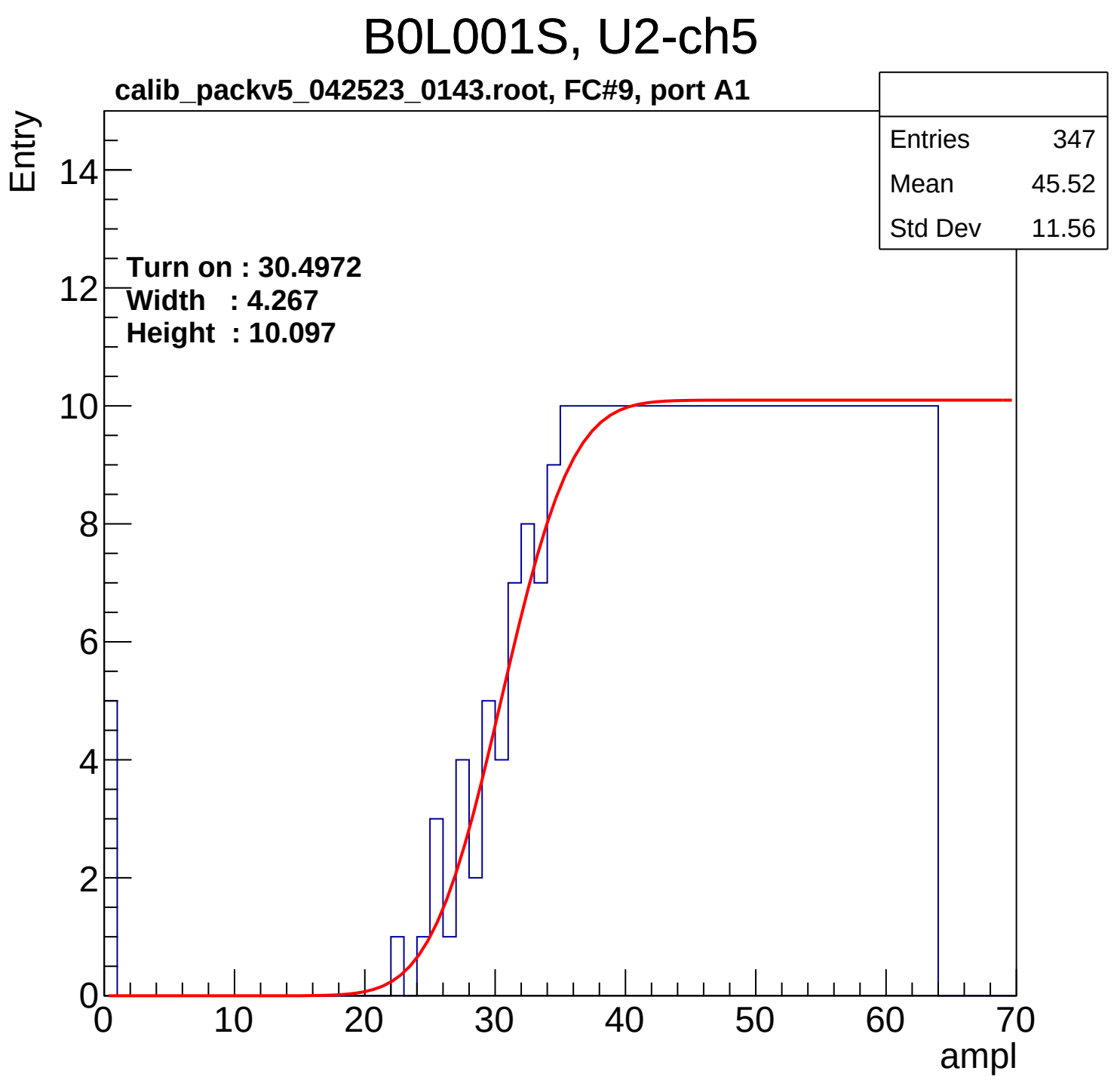
B0L001S, U2-ch5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 347
Mean 45.52
Std Dev 11.56
Turn on : 30.4972
Width : 4.267
Height : 10.097
Entry
ampl
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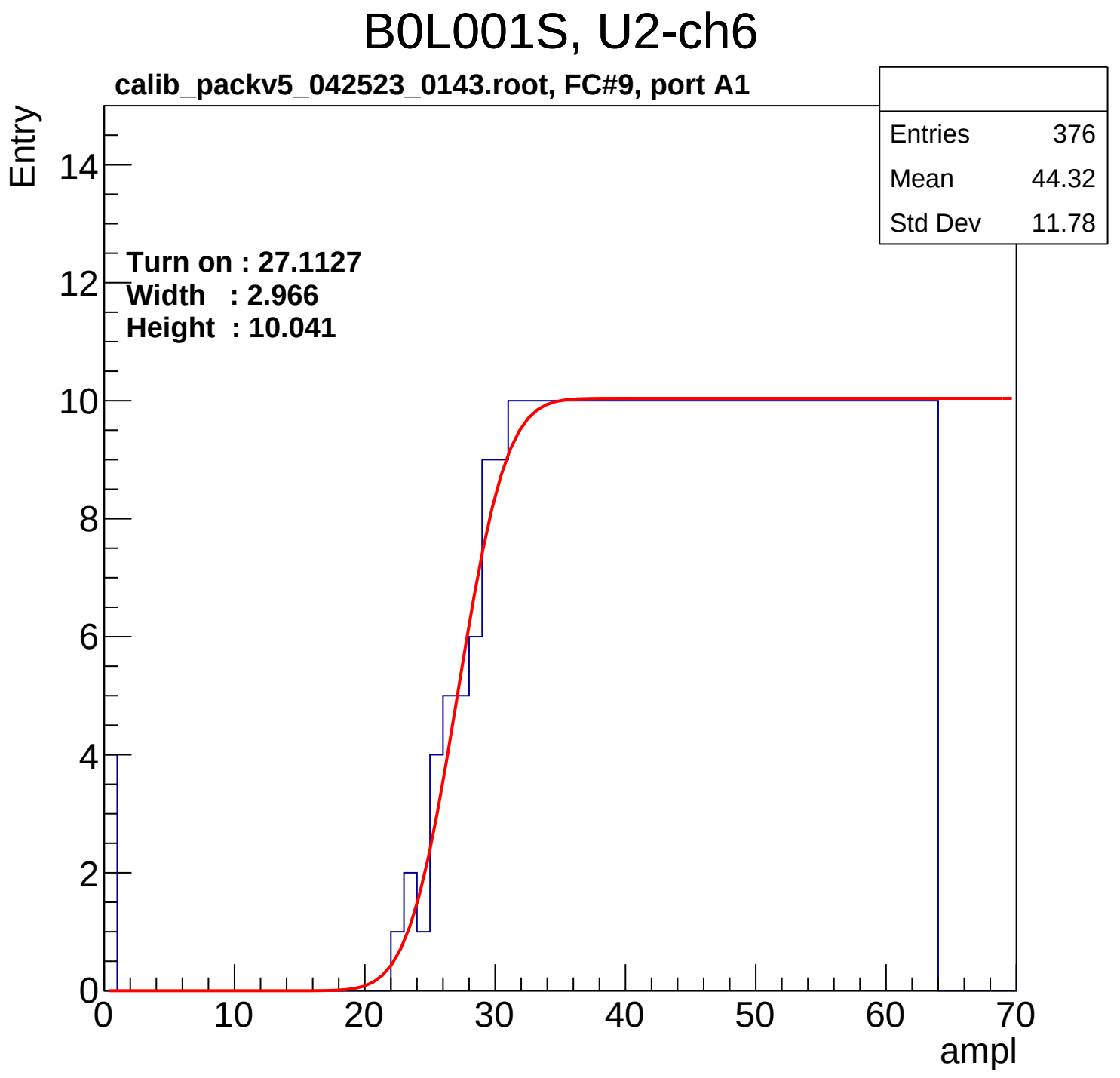
B0L001S, U2-ch6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 376
Mean 44.32
Std Dev 11.78
Turn on : 27.1127
Width : 2.966
Height : 10.041
Entry
ampl
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2
4
6
8
10
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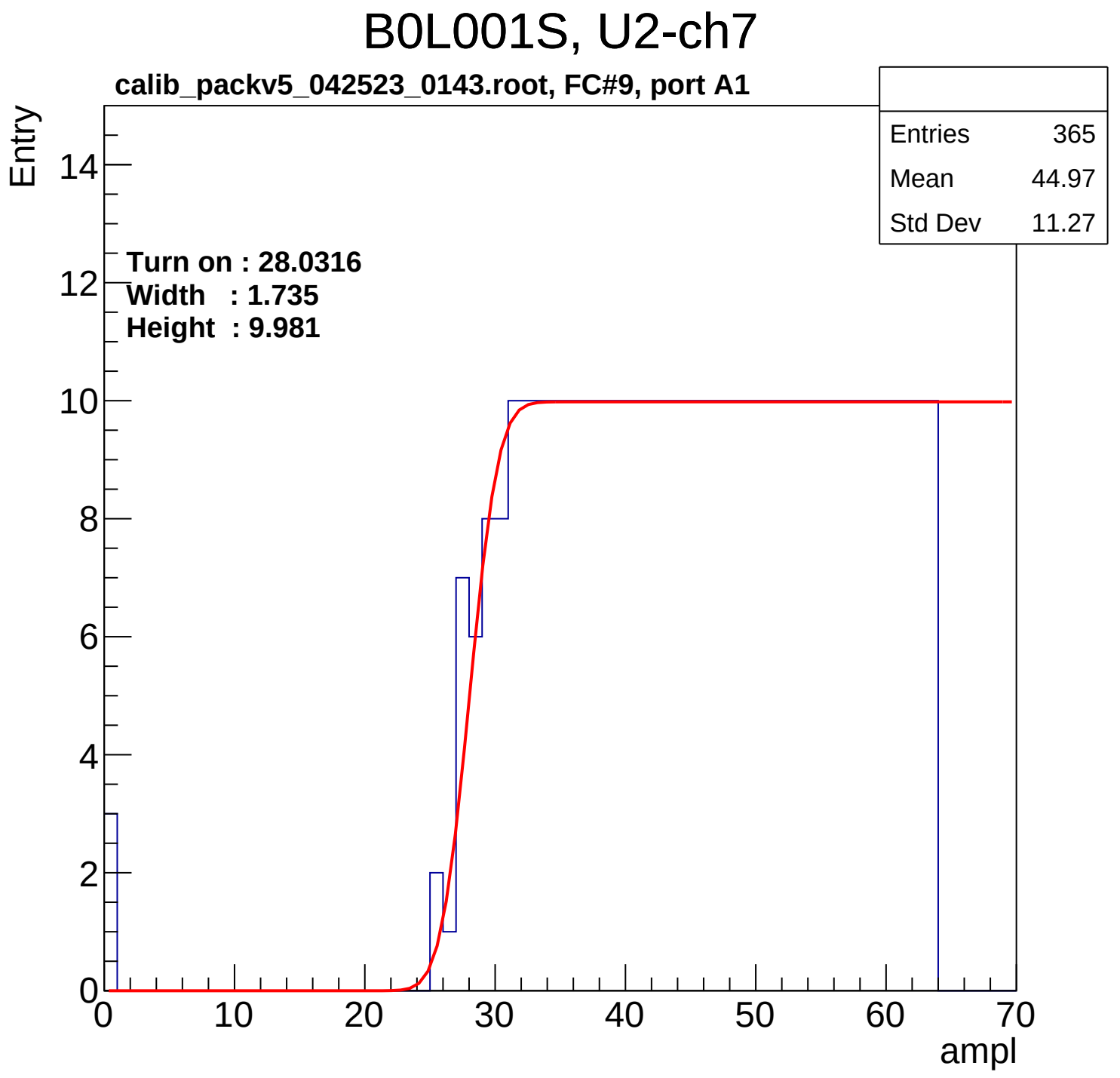
B0L001S, U2-ch7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 44.97
Std Dev 11.27
Turn on : 28.0316
Width : 1.735
Height : 9.981
Entry
ampl
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2
4
6
8
10
12
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0
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60
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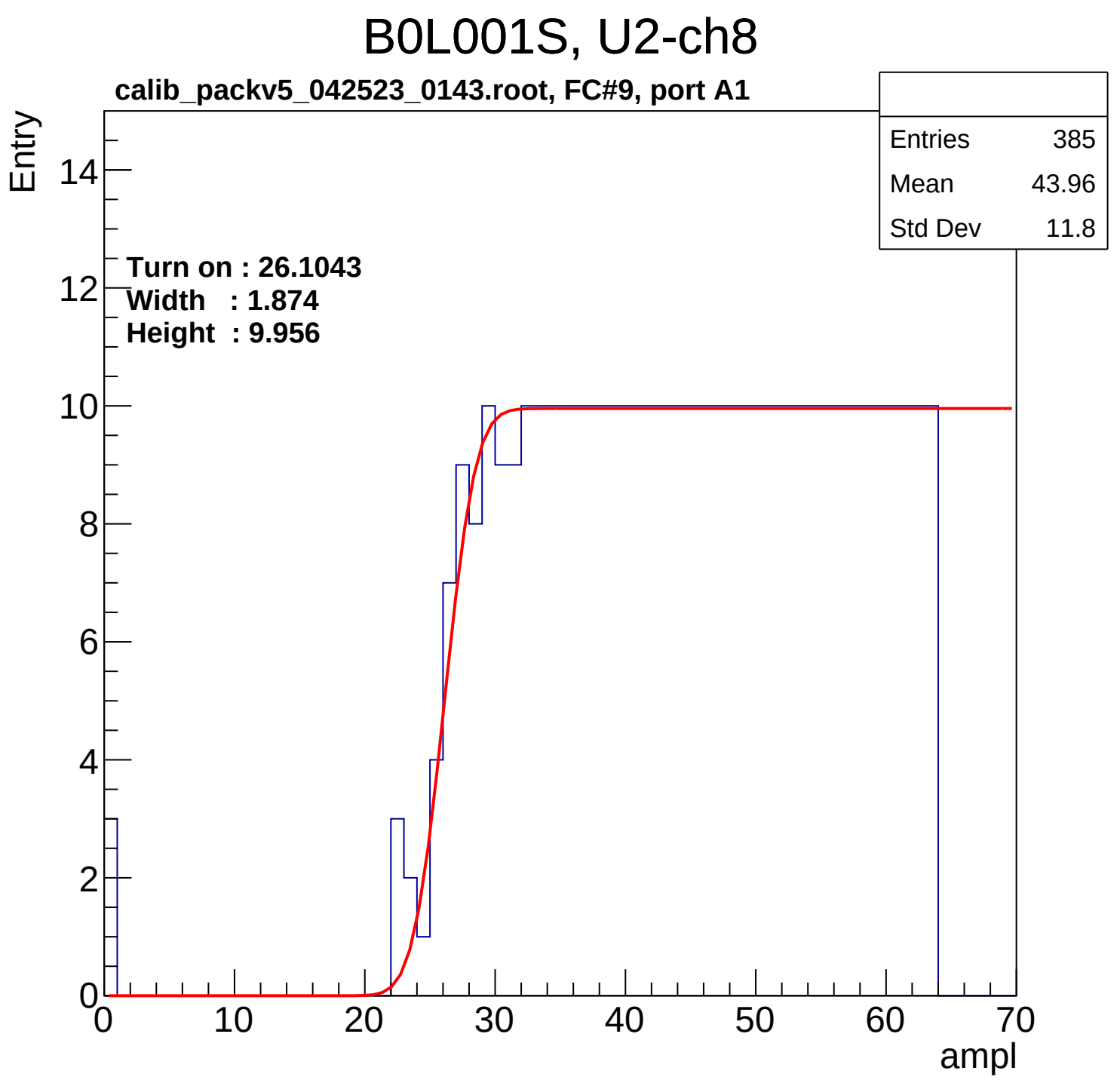
B0L001S, U2-ch8
calib_packv5_042523_0143.root, FC#9, port A1
Entries 385
Mean 43.96
Std Dev 11.8
Turn on : 26.1043
Width : 1.874
Height : 9.956
Entry
ampl
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2
4
6
8
10
12
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0
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60
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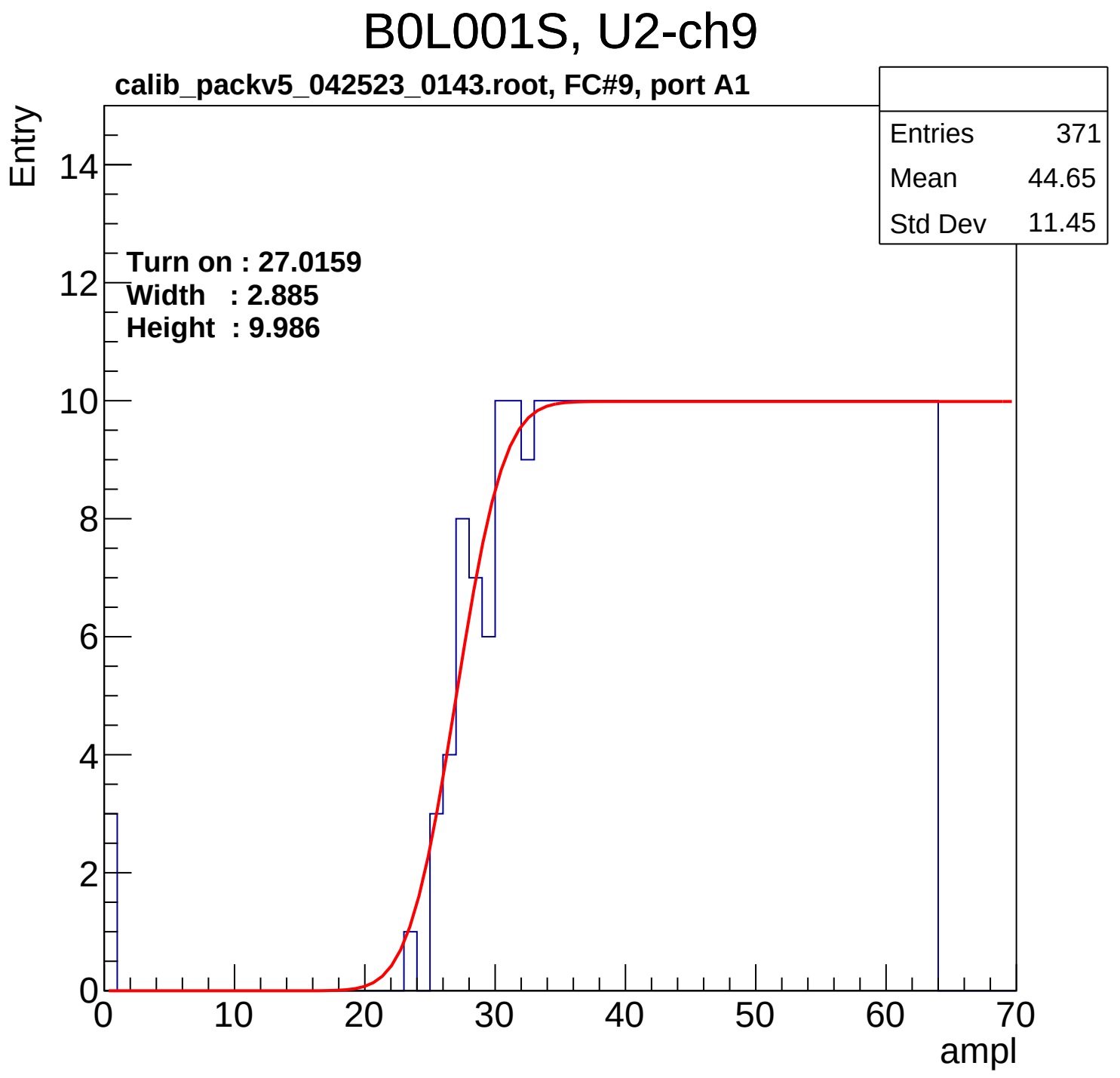
B0L001S, U2-ch9
calib_packv5_042523_0143.root, FC#9, port A1
Entries 371
Mean 44.65
Std Dev 11.45
Turn on : 27.0159
Width : 2.885
Height : 9.986
Entry
ampl
0
2
4
6
8
10
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60
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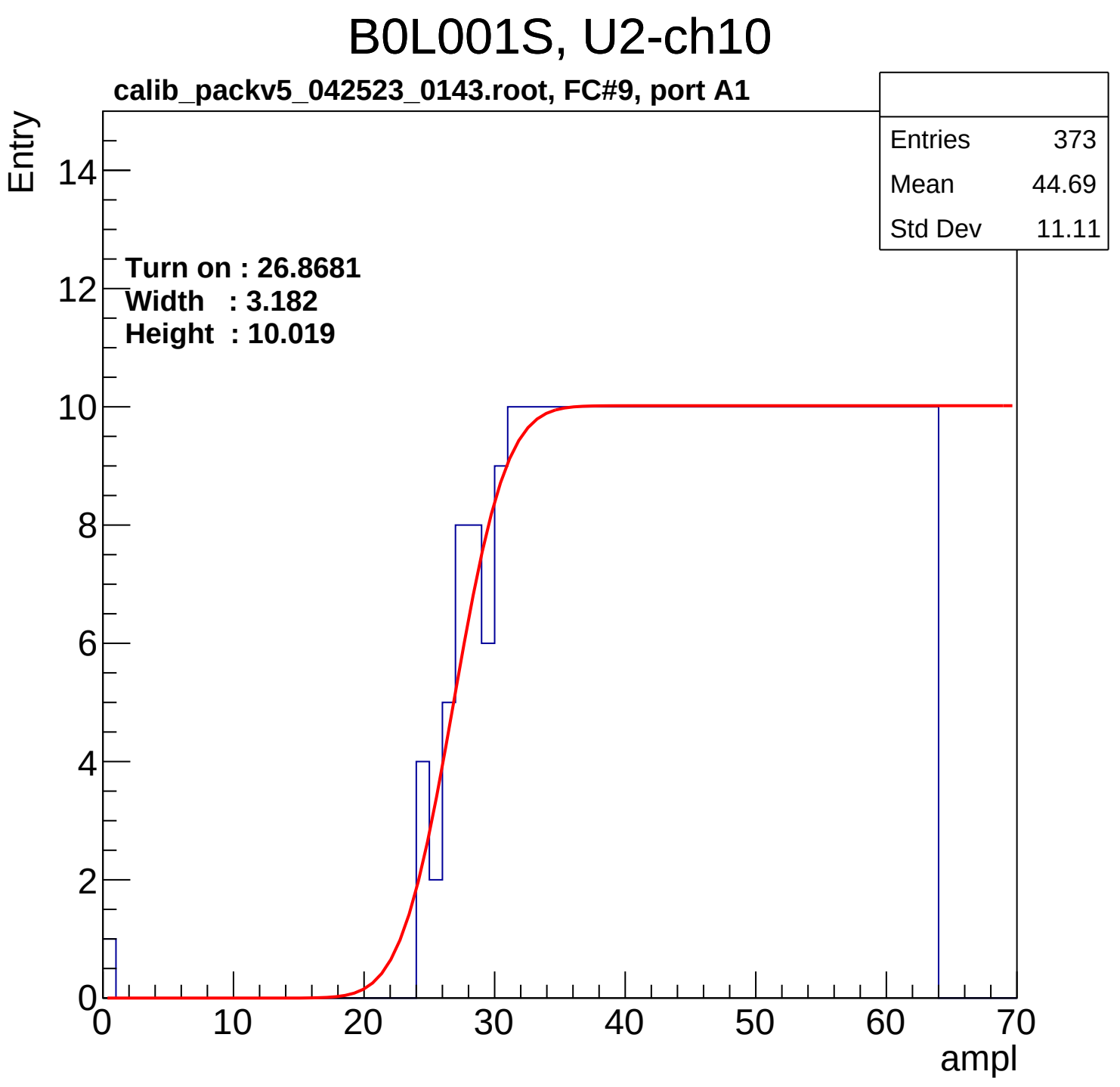
B0L001S, U2-ch10
calib_packv5_042523_0143.root, FC#9, port A1
Entries 373
Mean 44.69
Std Dev 11.11
Turn on : 26.8681
Width : 3.182
Height : 10.019
Entry
ampl
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2
4
6
8
10
12
14
0
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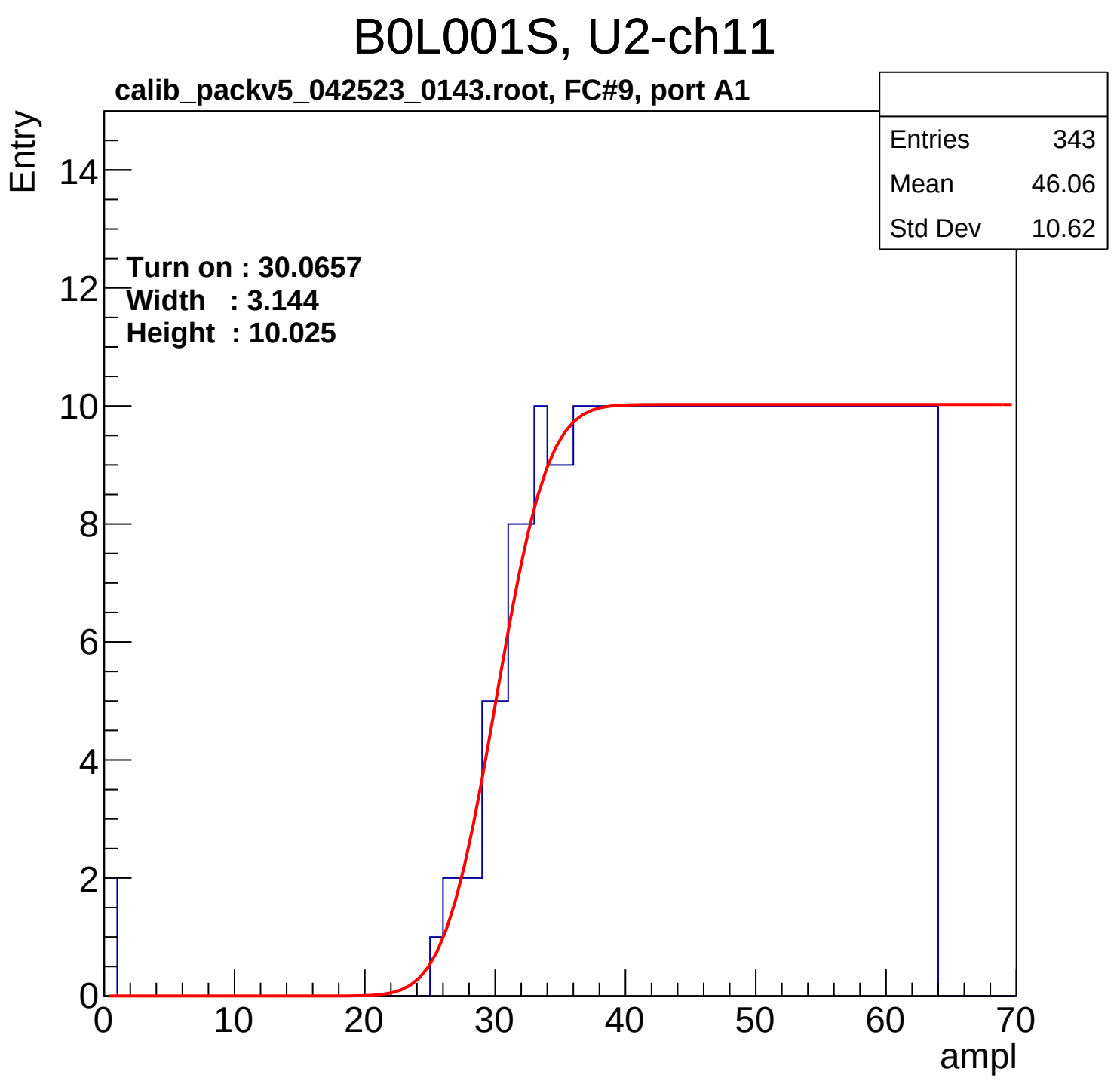
B0L001S, U2-ch11
calib_packv5_042523_0143.root, FC#9, port A1
Entries 343
Mean 46.06
Std Dev 10.62
Turn on : 30.0657
Width : 3.144
Height : 10.025
Entry
ampl
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8
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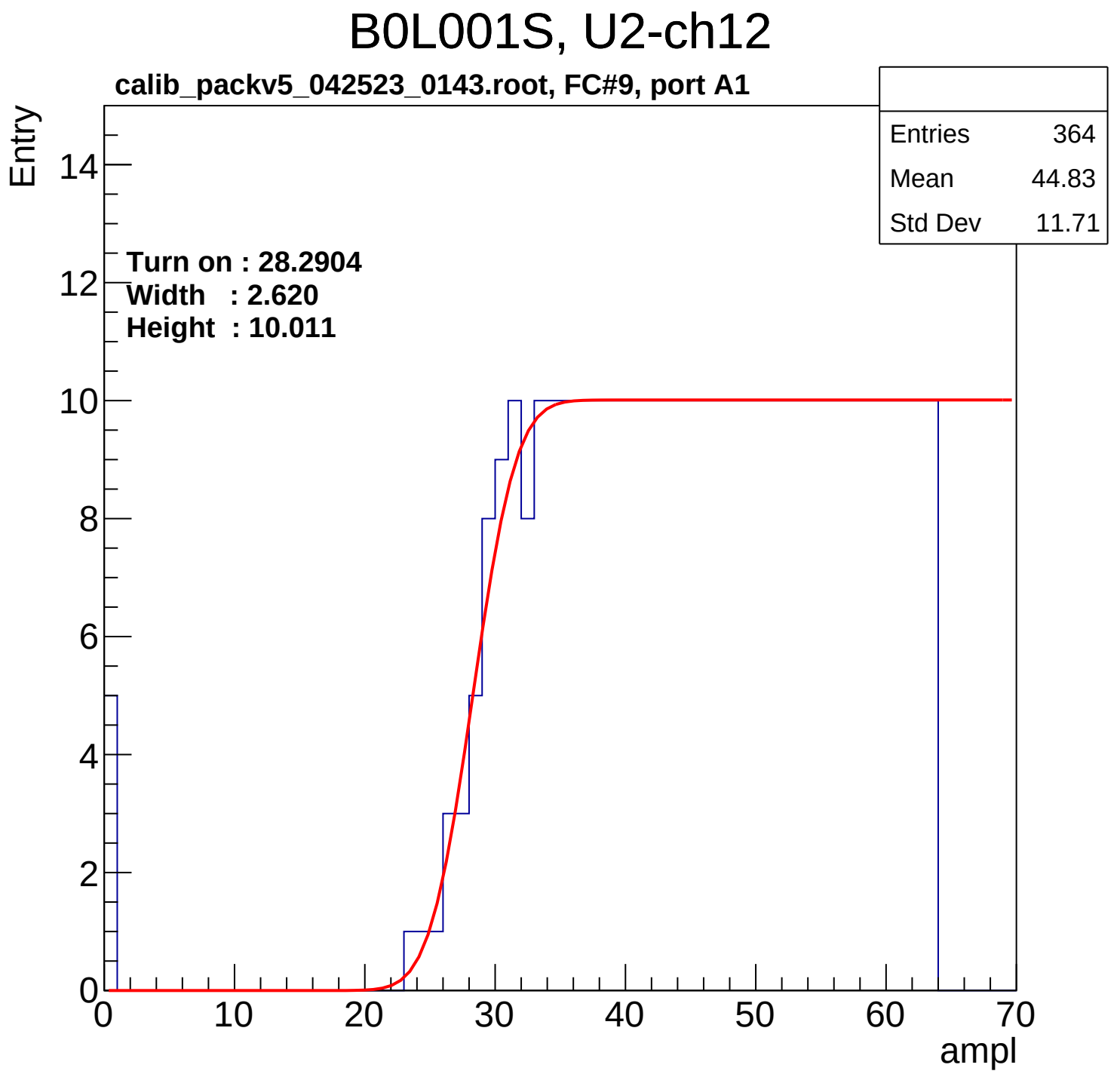
B0L001S, U2-ch12
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 44.83
Std Dev 11.71
Turn on : 28.2904
Width : 2.620
Height : 10.011
Entry
ampl
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4
6
8
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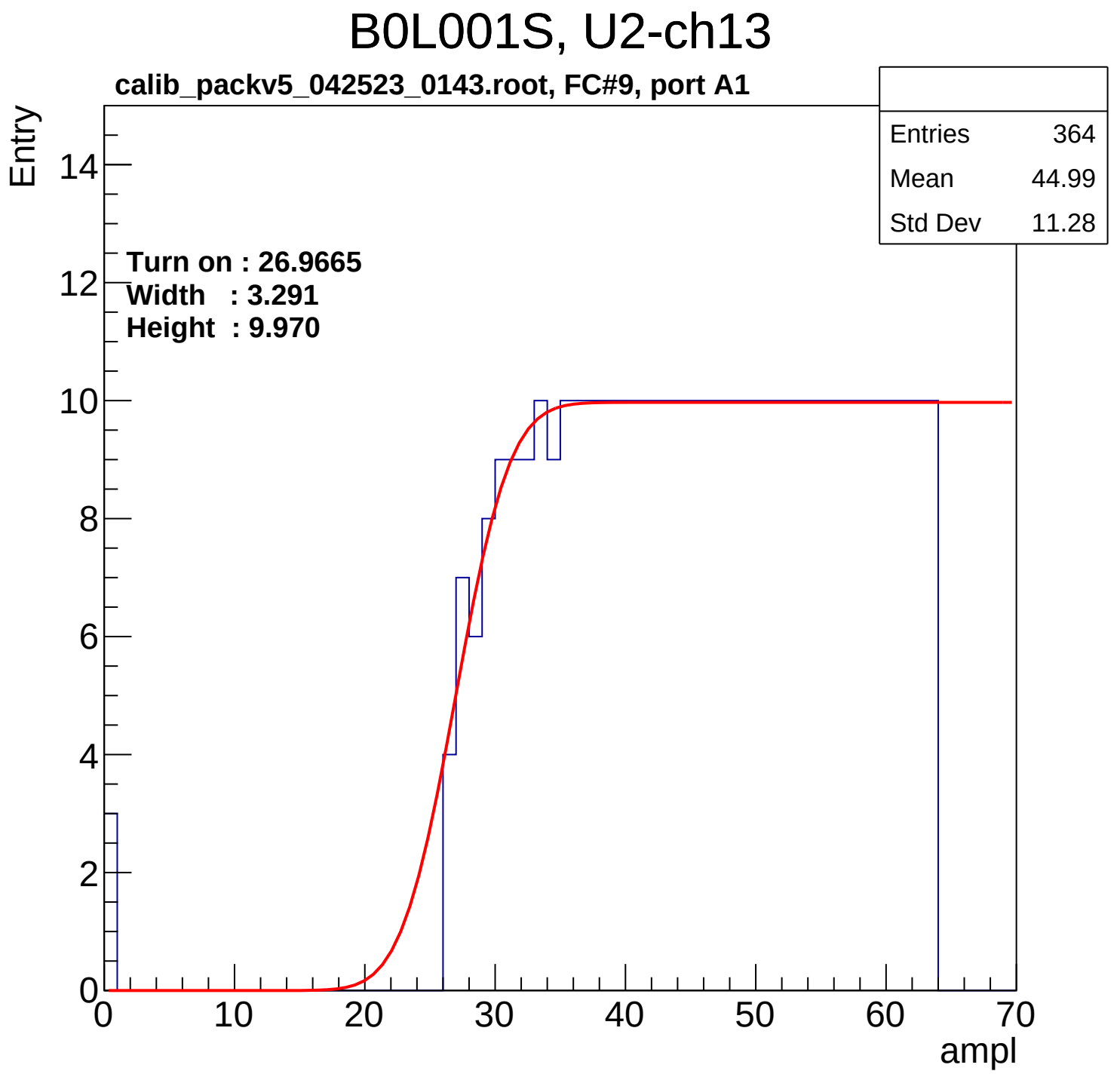
B0L001S, U2-ch13
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 44.99
Std Dev 11.28
Turn on : 26.9665
Width : 3.291
Height : 9.970
Entry
ampl
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4
6
8
10
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0
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60
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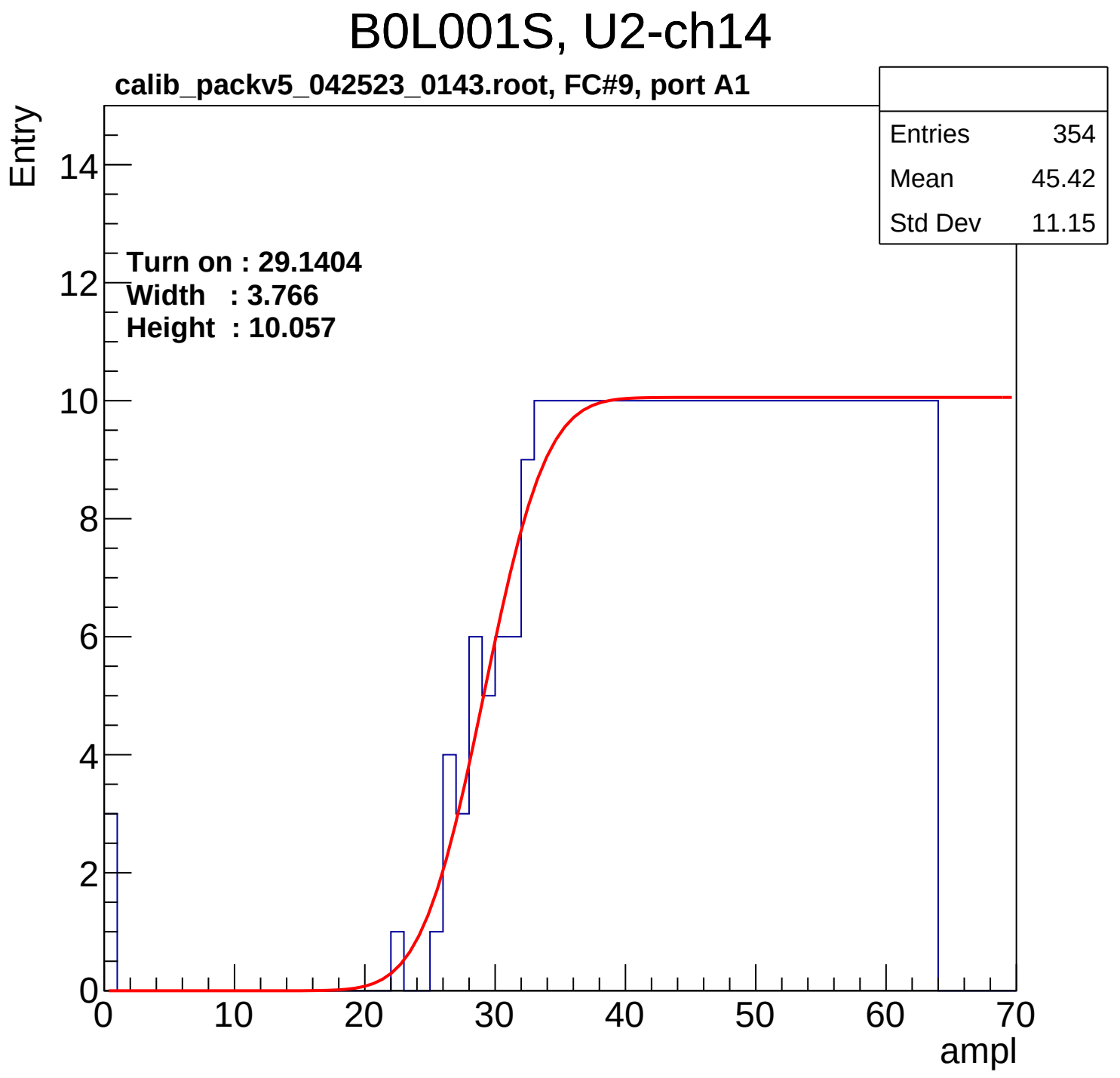
B0L001S, U2-ch14
calib_packv5_042523_0143.root, FC#9, port A1
Entries 354
Mean 45.42
Std Dev 11.15
Turn on : 29.1404
Width : 3.766
Height : 10.057
Entry
ampl
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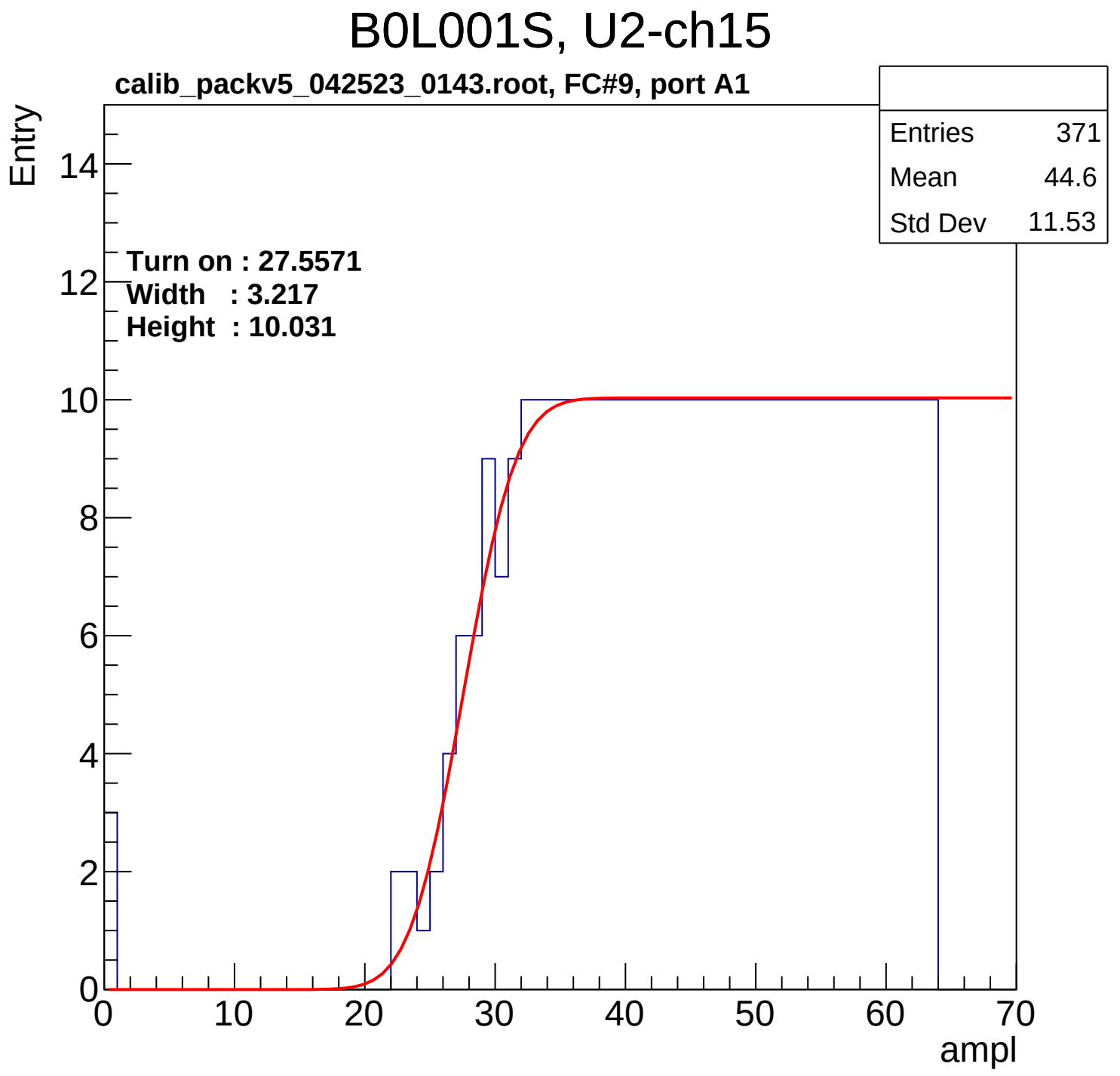
B0L001S, U2-ch15
calib_packv5_042523_0143.root, FC#9, port A1
Entries 371
Mean 44.6
Std Dev 11.53
Turn on : 27.5571
Width : 3.217
Height : 10.031
Entry
ampl
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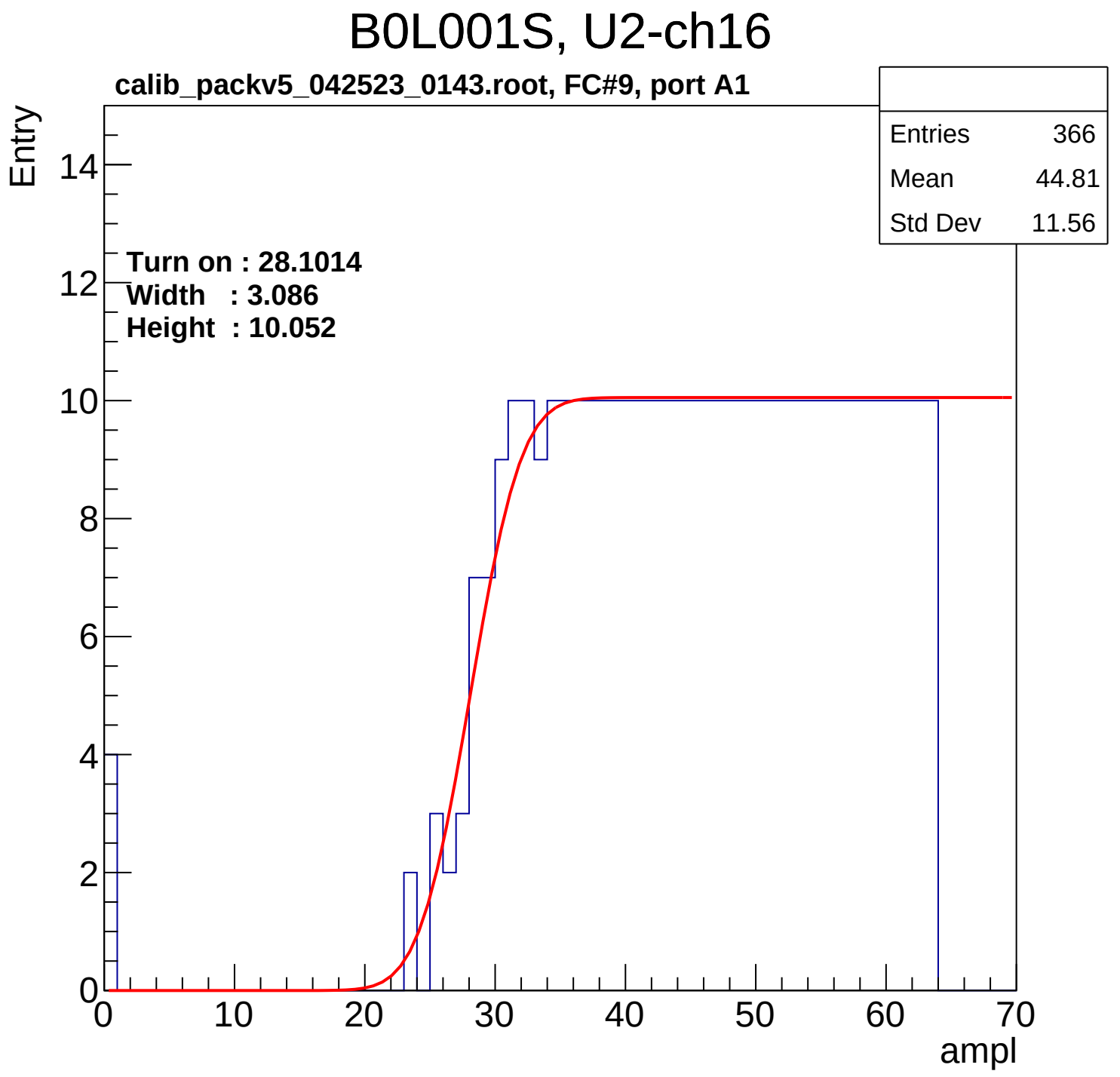
B0L001S, U2-ch16
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.81
Std Dev 11.56
Turn on : 28.1014
Width : 3.086
Height : 10.052
Entry
ampl
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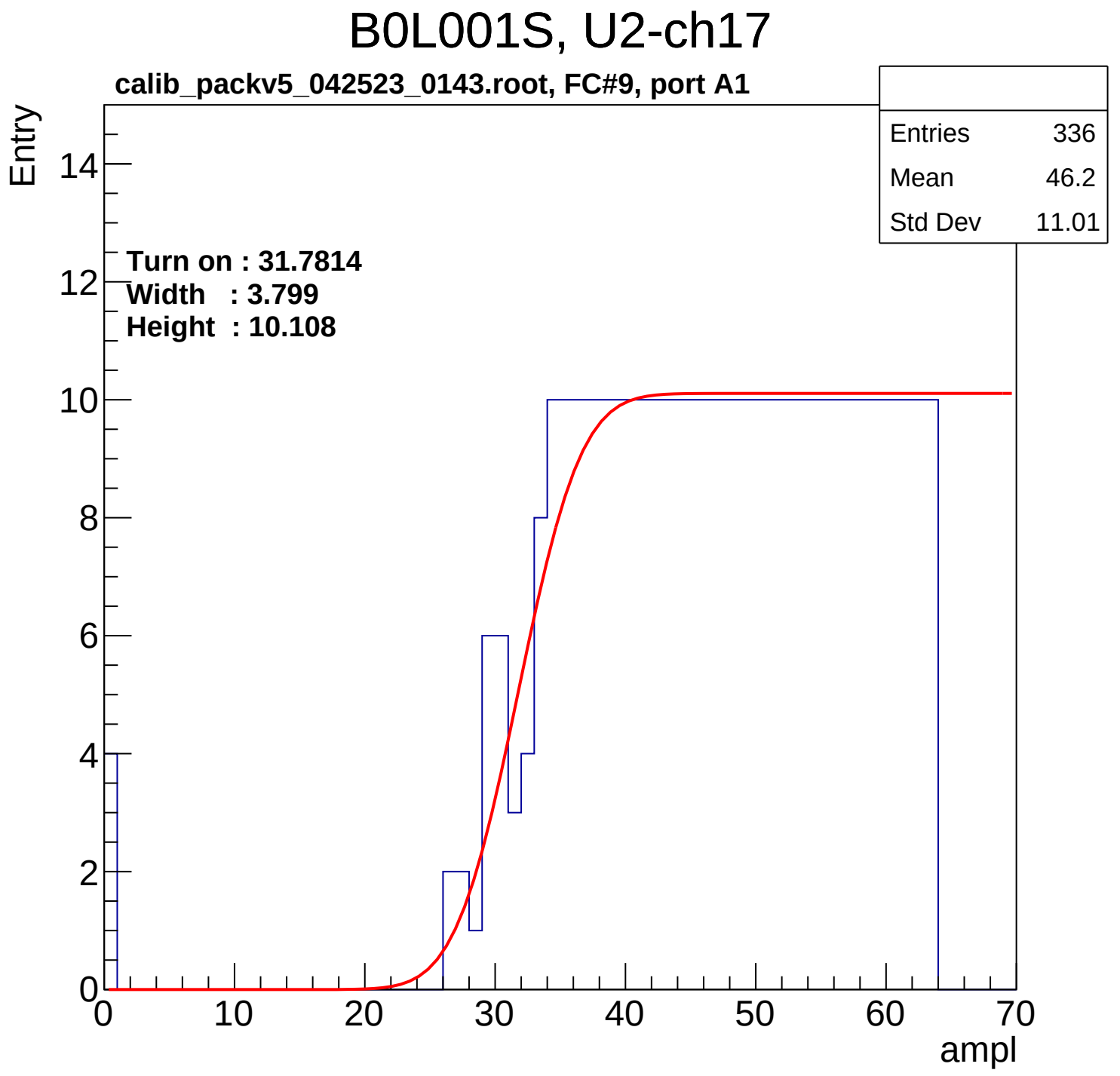
B0L001S, U2-ch17
calib_packv5_042523_0143.root, FC#9, port A1
Entries 336
Mean 46.2
Std Dev 11.01
Turn on : 31.7814
Width : 3.799
Height : 10.108
Entry
ampl
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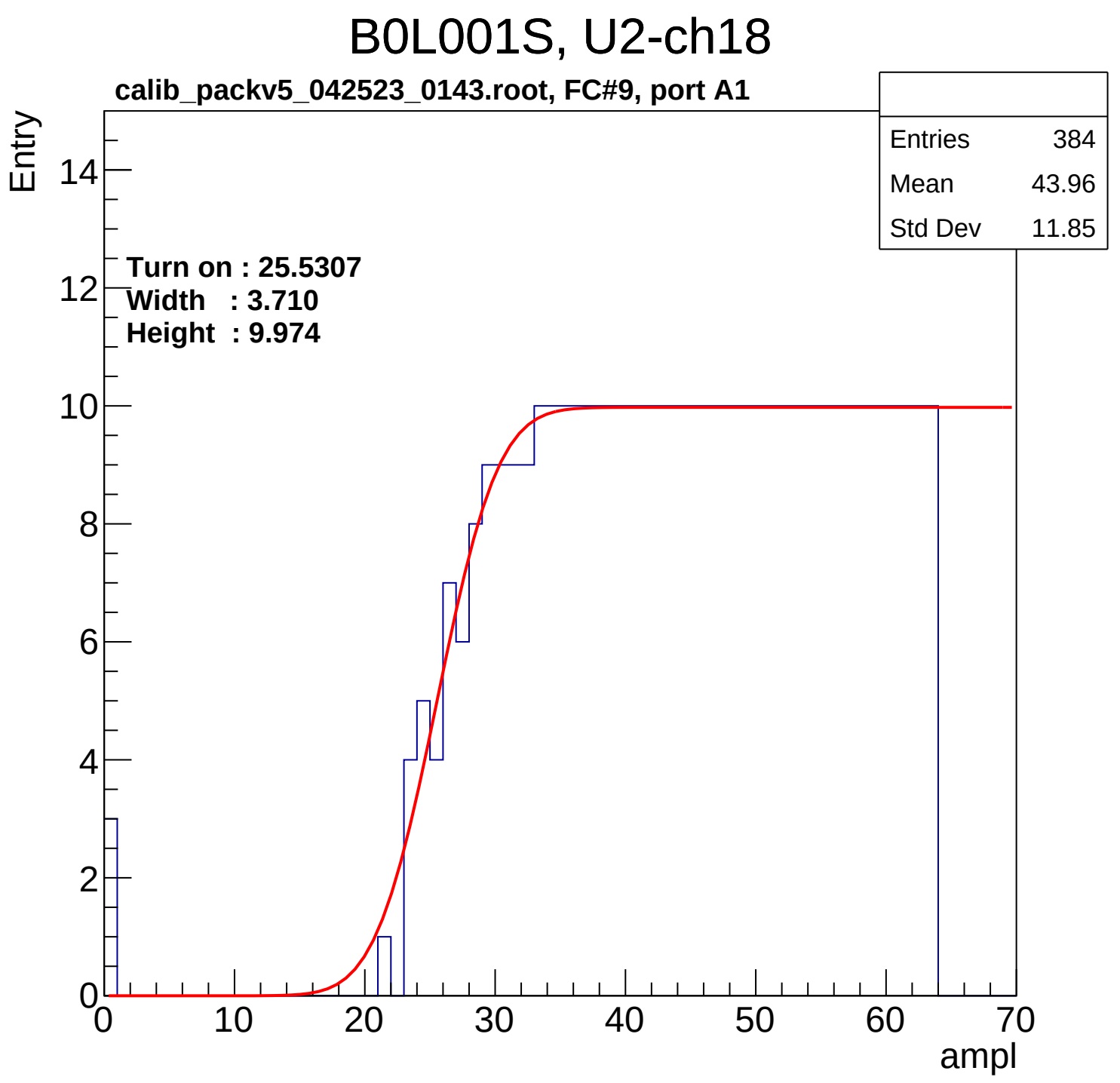
B0L001S, U2-ch18
calib_packv5_042523_0143.root, FC#9, port A1
Entries 384
Mean 43.96
Std Dev 11.85
Turn on : 25.5307
Width : 3.710
Height : 9.974
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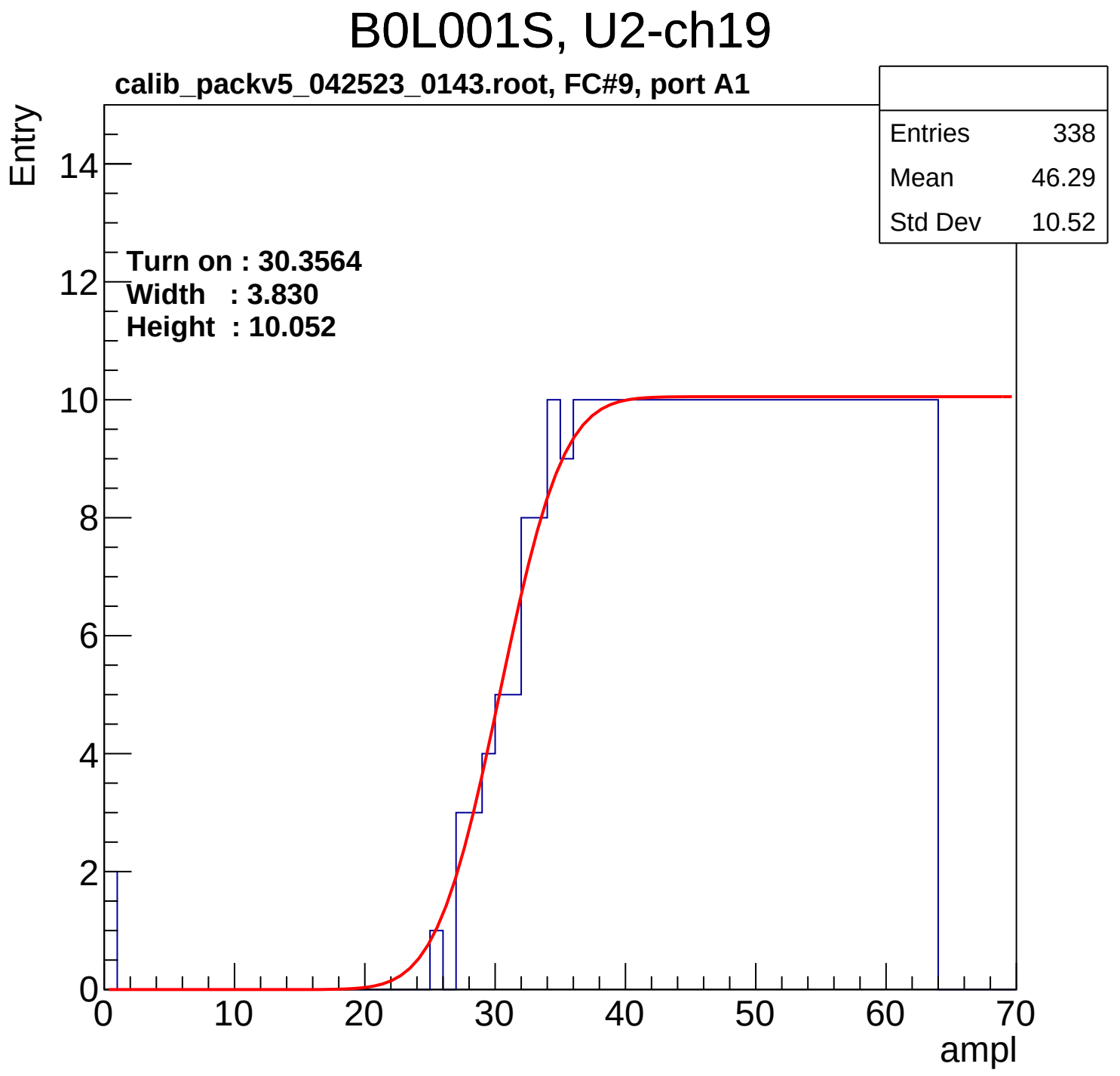
B0L001S, U2-ch19
calib_packv5_042523_0143.root, FC#9, port A1
Entries 338
Mean 46.29
Std Dev 10.52
Turn on : 30.3564
Width : 3.830
Height : 10.052
Entry
ampl
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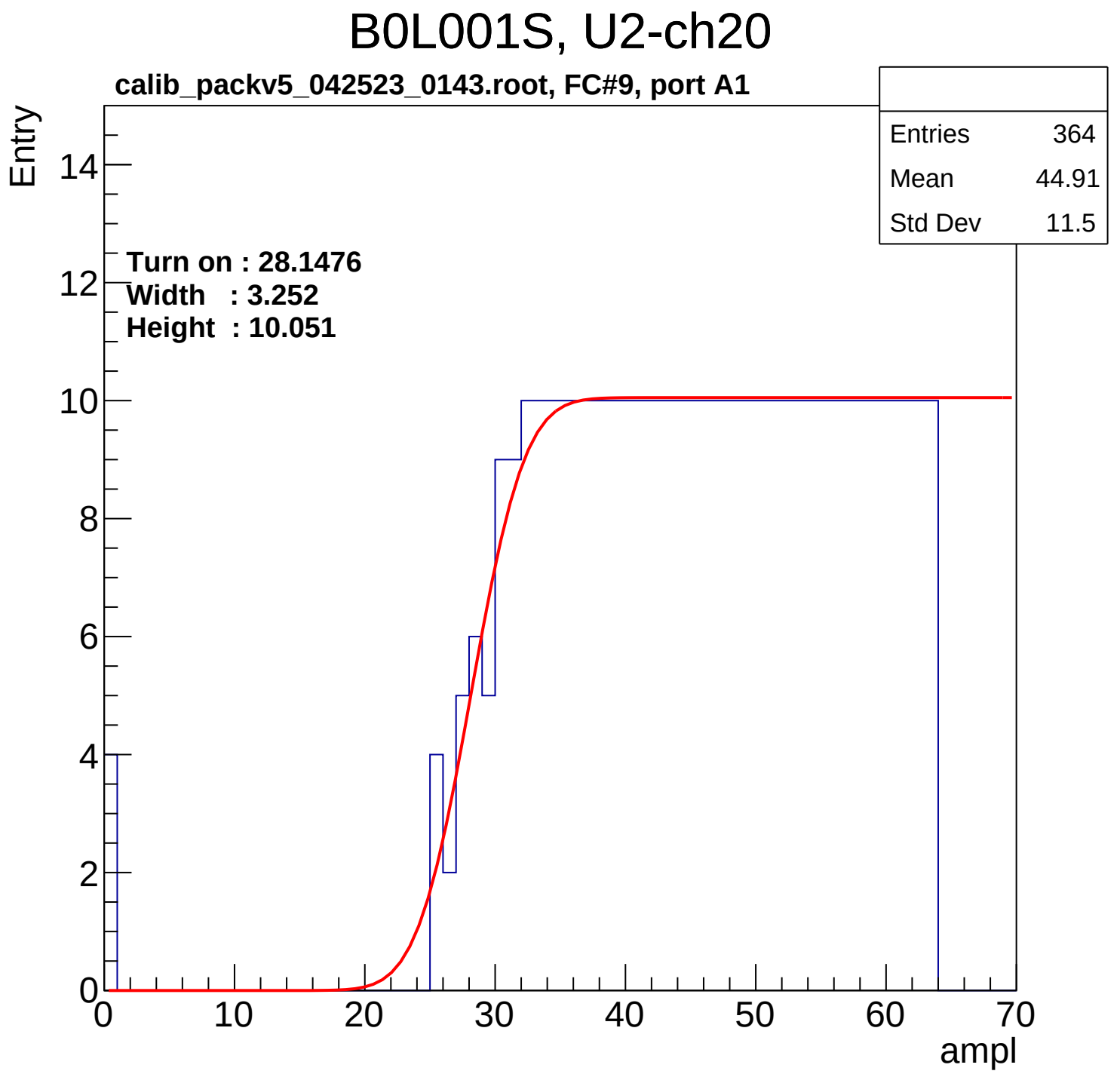
B0L001S, U2-ch20
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 44.91
Std Dev 11.5
Turn on : 28.1476
Width : 3.252
Height : 10.051
Entry
ampl
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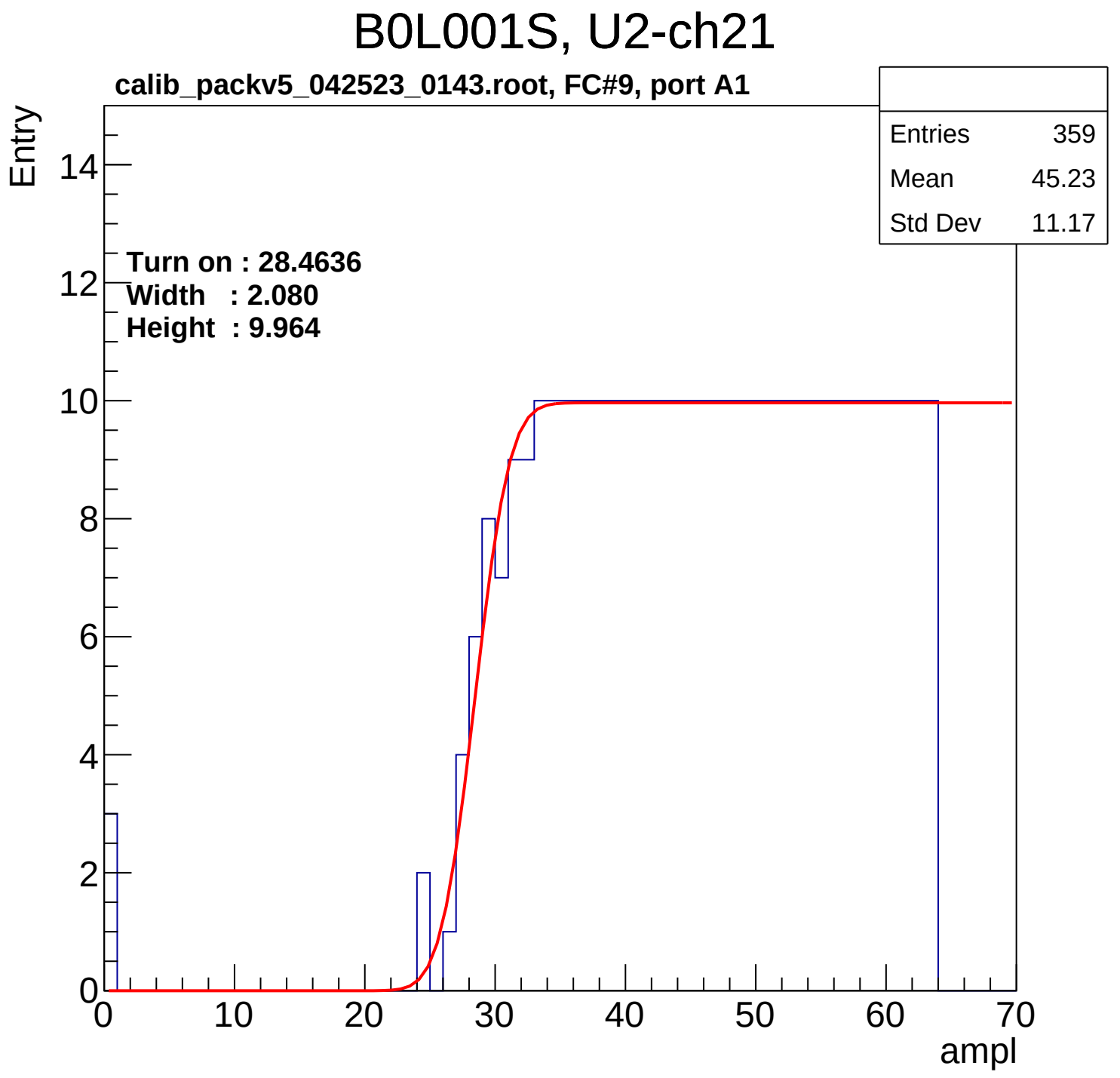
B0L001S, U2-ch21
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 45.23
Std Dev 11.17
Turn on : 28.4636
Width : 2.080
Height : 9.964
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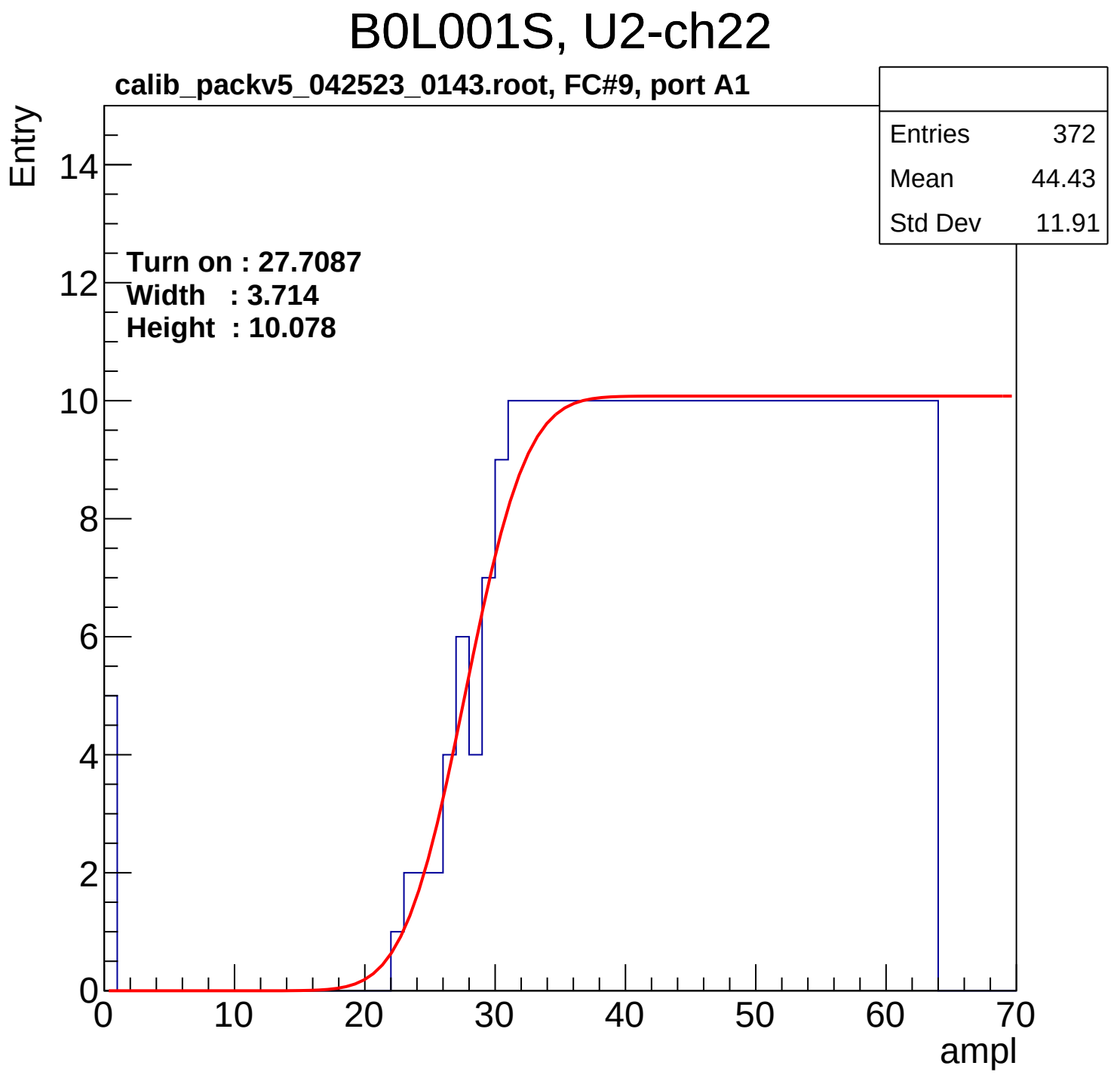
B0L001S, U2-ch22
calib_packv5_042523_0143.root, FC#9, port A1
Entries 372
Mean 44.43
Std Dev 11.91
Turn on : 27.7087
Width : 3.714
Height : 10.078
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ampl
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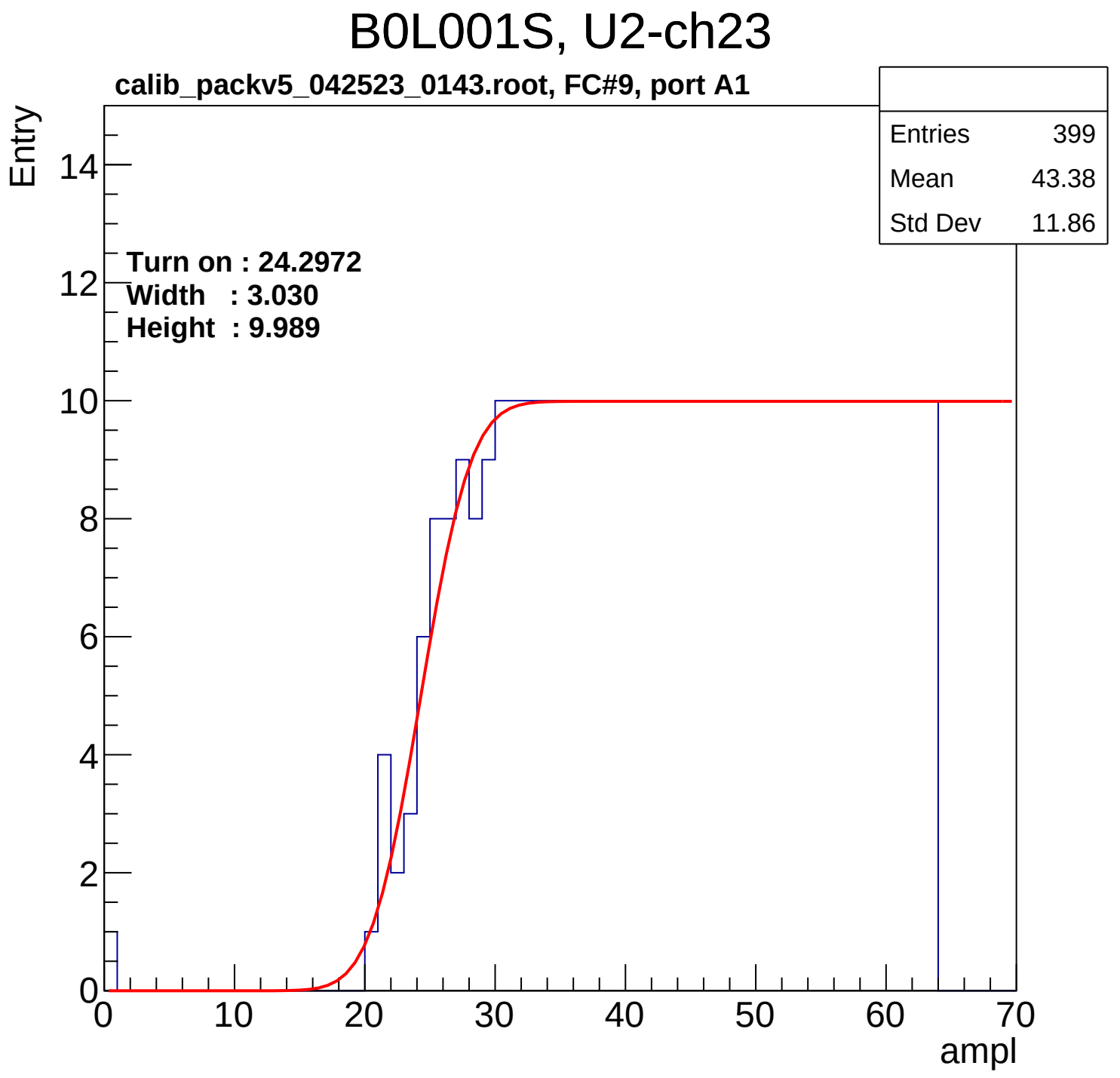
B0L001S, U2-ch23
calib_packv5_042523_0143.root, FC#9, port A1
Entries 399
Mean 43.38
Std Dev 11.86
Turn on : 24.2972
Width : 3.030
Height : 9.989
Entry
ampl
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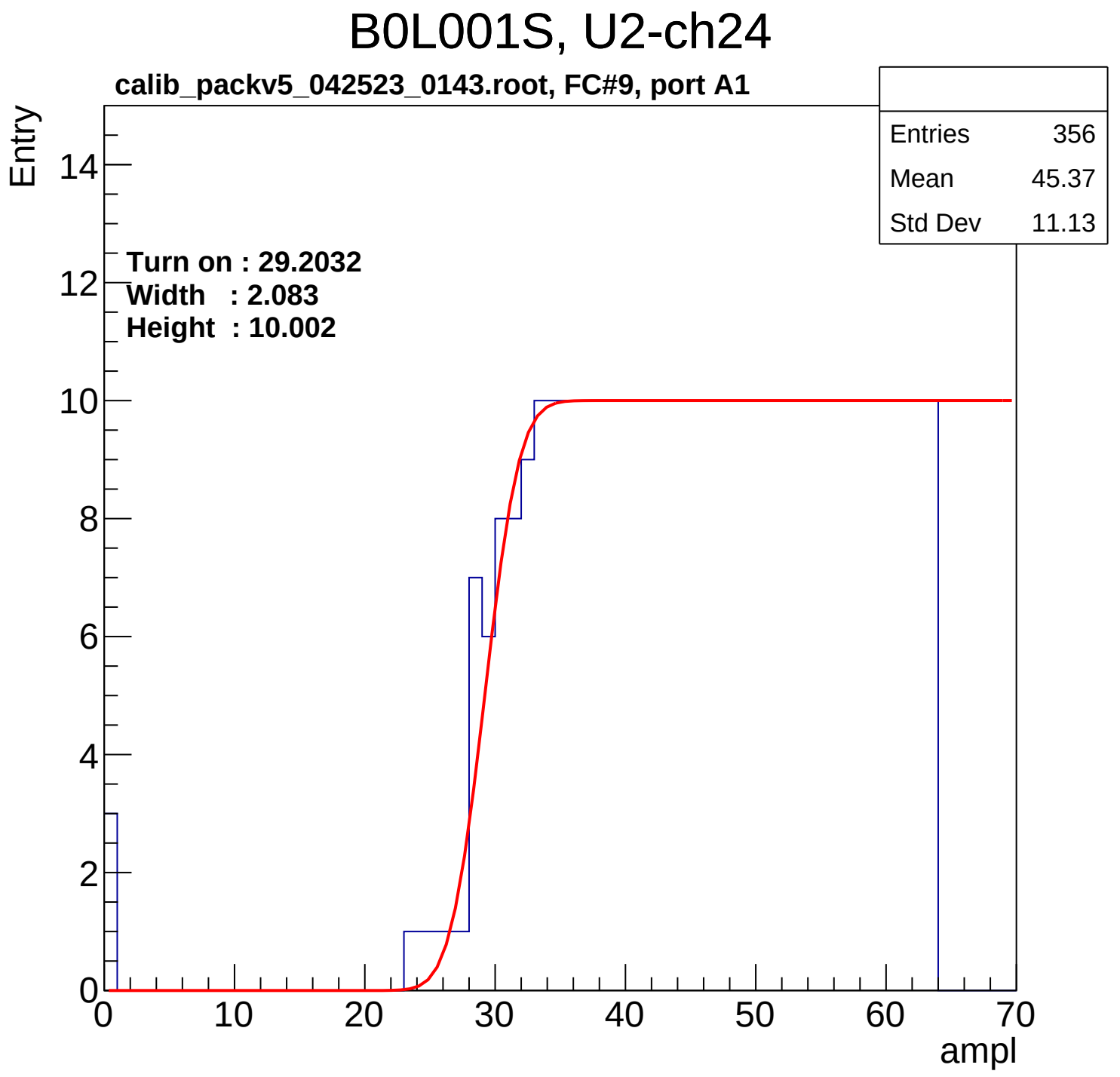
B0L001S, U2-ch24
calib_packv5_042523_0143.root, FC#9, port A1
Entries 356
Mean 45.37
Std Dev 11.13
Turn on : 29.2032
Width : 2.083
Height : 10.002
Entry
ampl
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6
8
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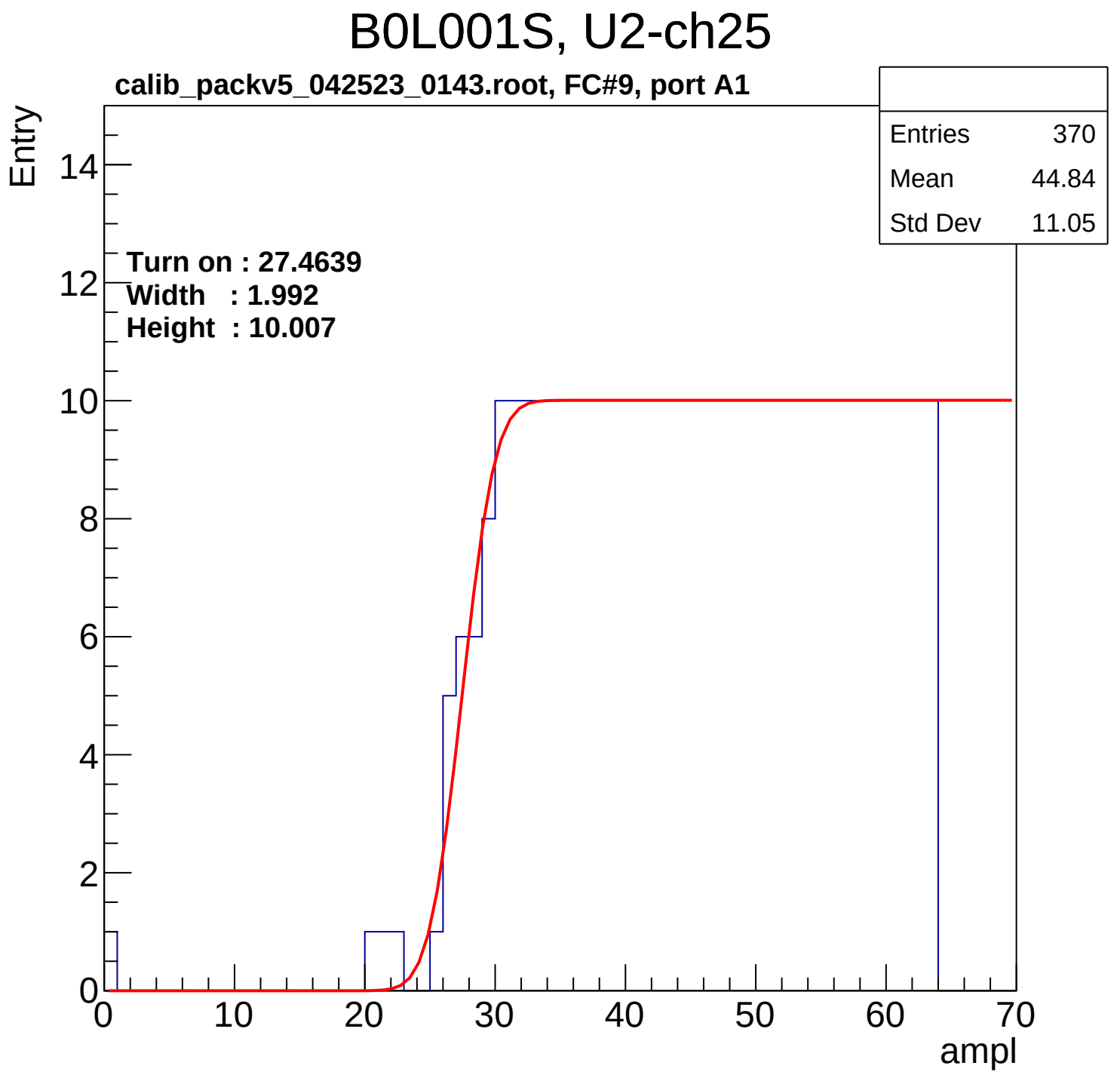
B0L001S, U2-ch25
calib_packv5_042523_0143.root, FC#9, port A1
Entries 370
Mean 44.84
Std Dev 11.05
Turn on : 27.4639
Width : 1.992
Height : 10.007
Entry
ampl
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8
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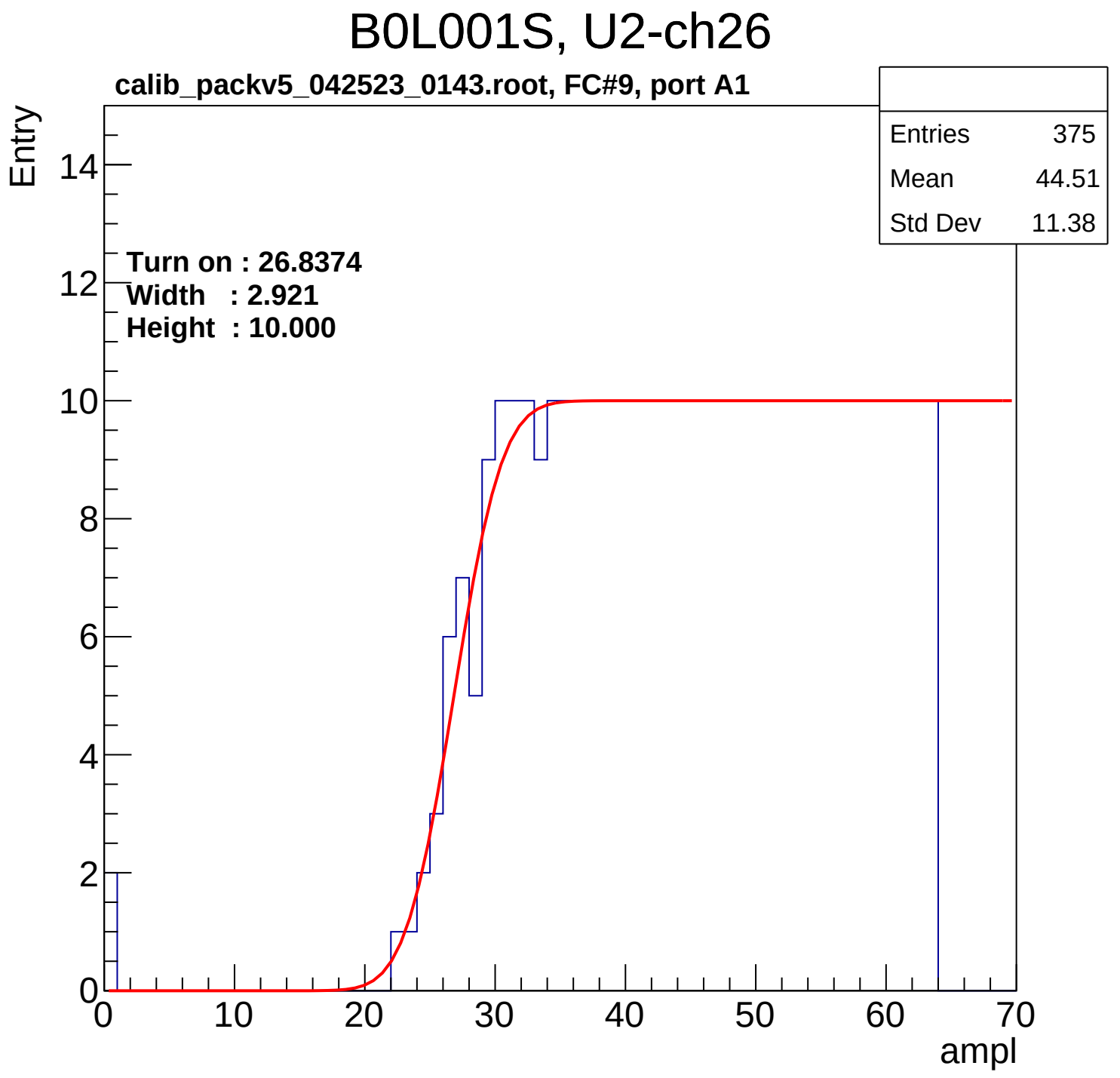
B0L001S, U2-ch26
calib_packv5_042523_0143.root, FC#9, port A1
Entries 375
Mean 44.51
Std Dev 11.38
Turn on : 26.8374
Width : 2.921
Height : 10.000
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ampl
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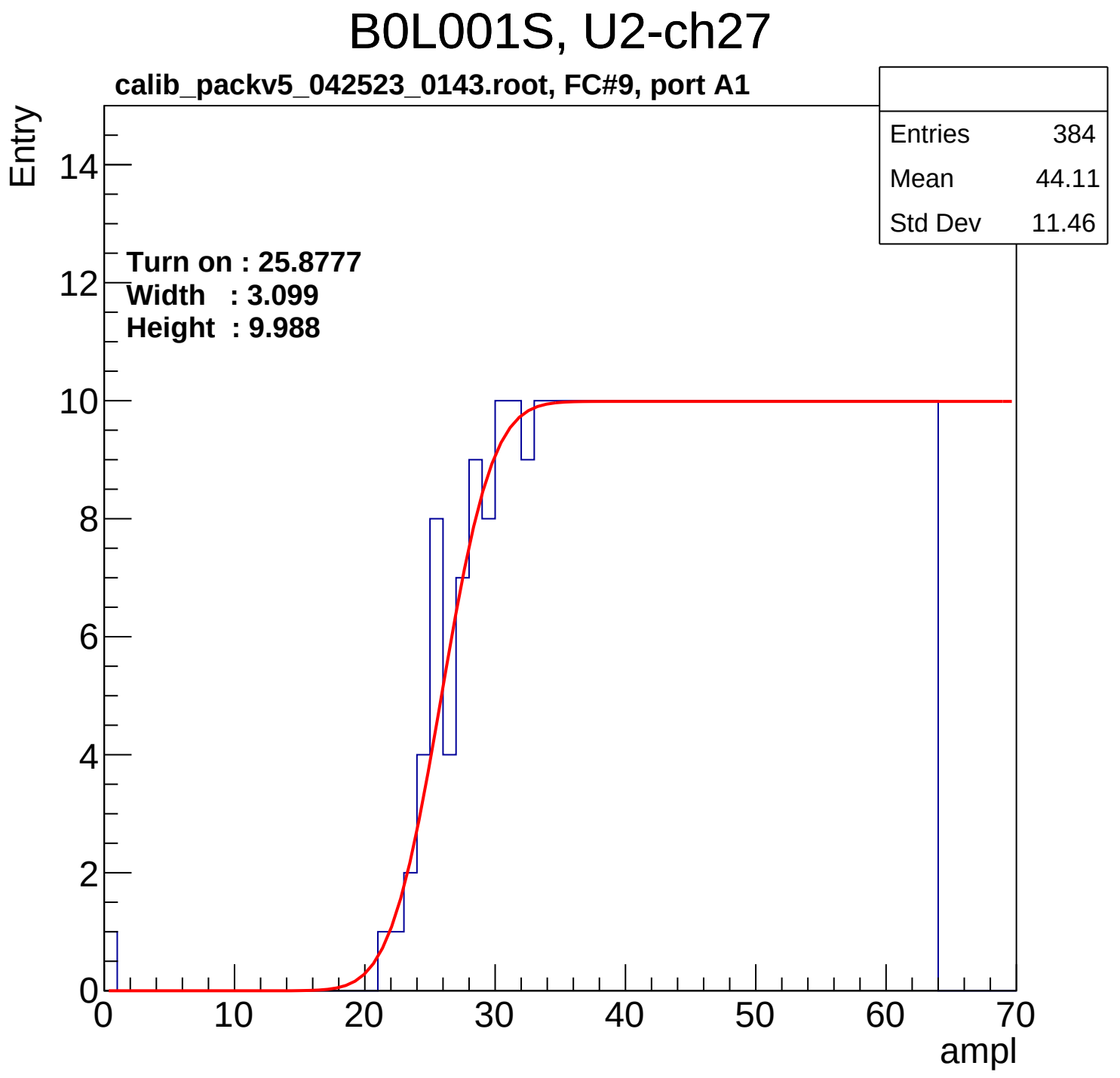
B0L001S, U2-ch27
calib_packv5_042523_0143.root, FC#9, port A1
Entries 384
Mean 44.11
Std Dev 11.46
Turn on : 25.8777
Width : 3.099
Height : 9.988
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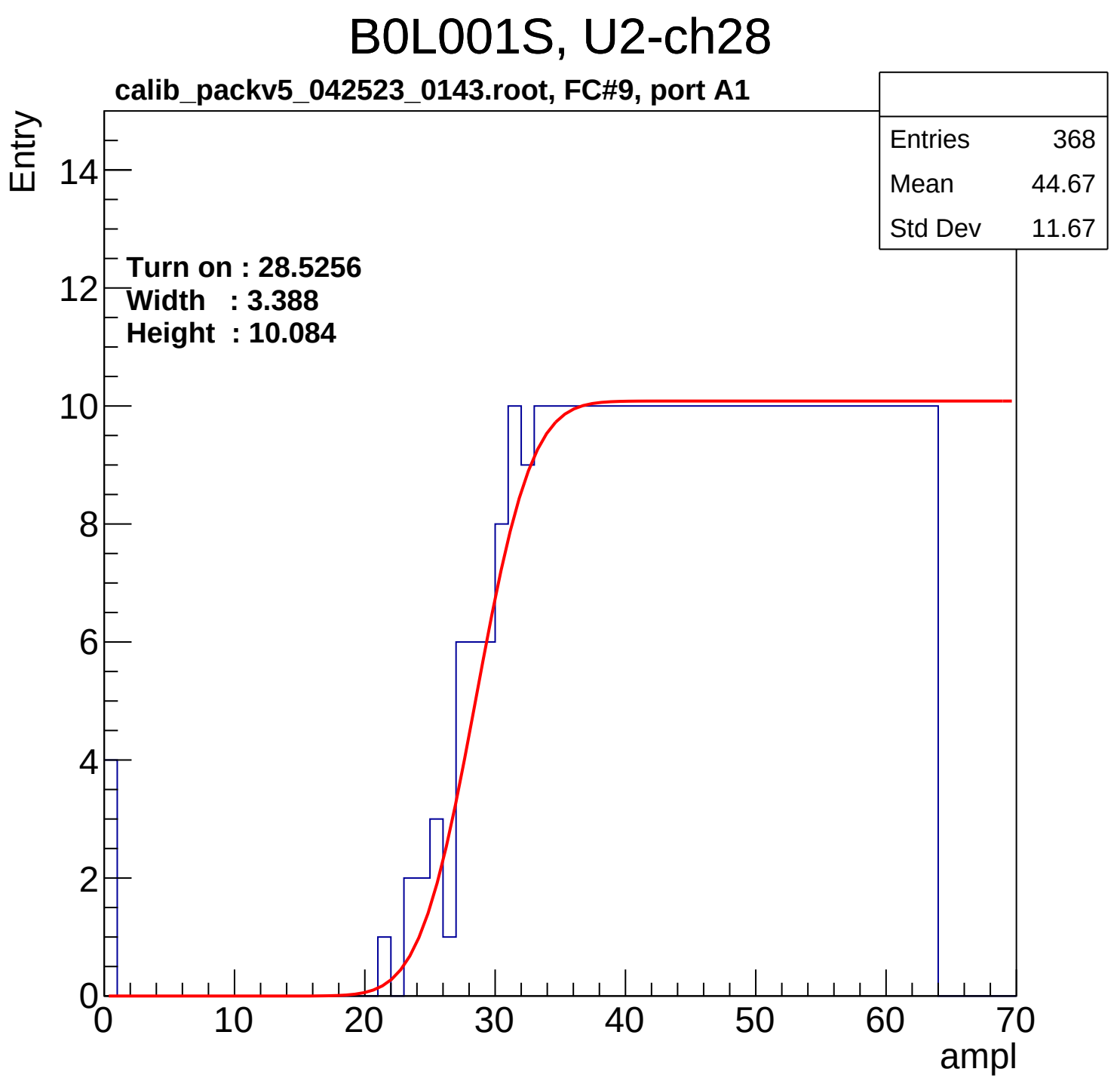
B0L001S, U2-ch28
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.67
Std Dev 11.67
Turn on : 28.5256
Width : 3.388
Height : 10.084
Entry
ampl
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4
6
8
10
12
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10
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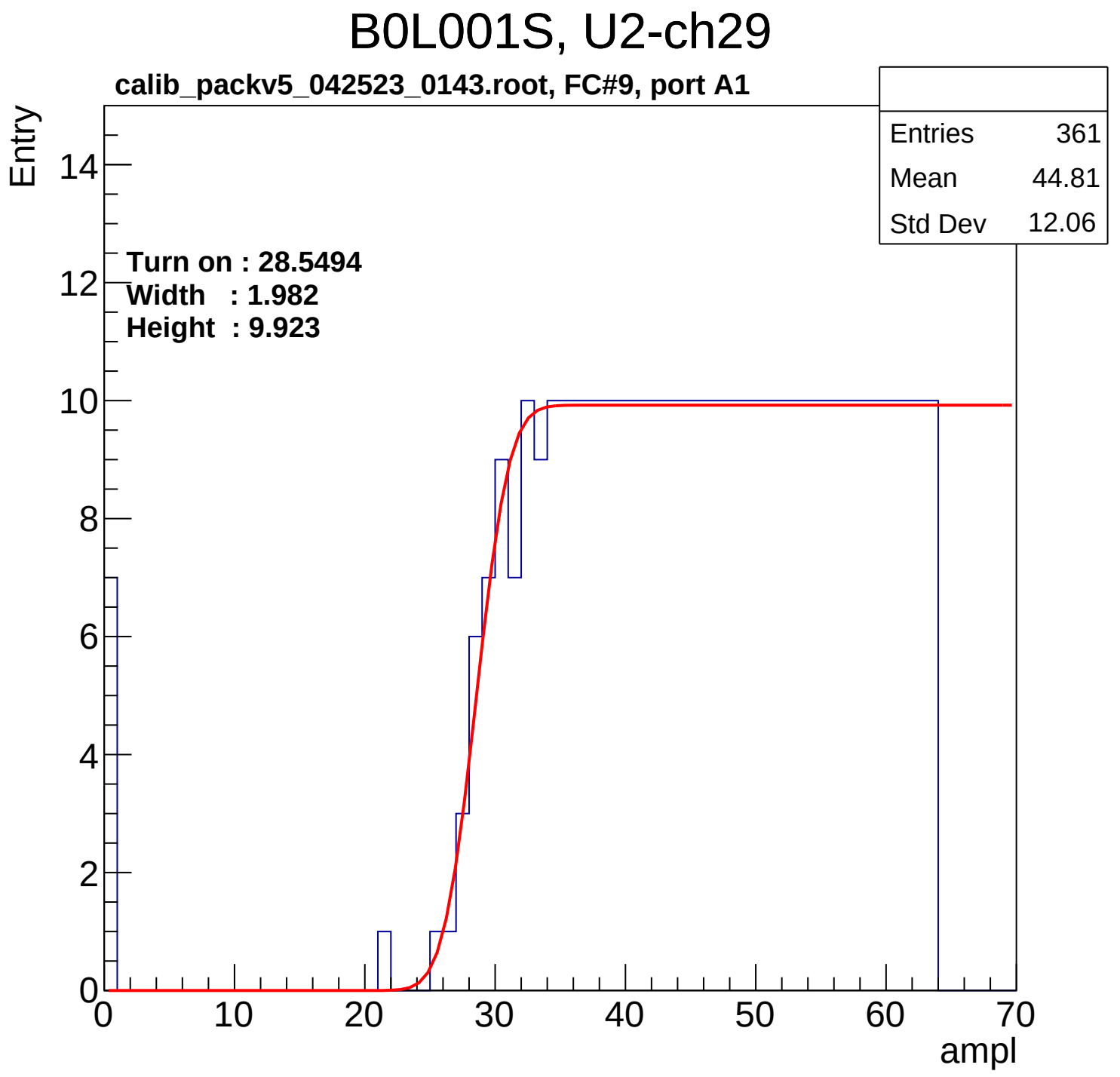
B0L001S, U2-ch29
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 44.81
Std Dev 12.06
Turn on : 28.5494
Width : 1.982
Height : 9.923
Entry
ampl
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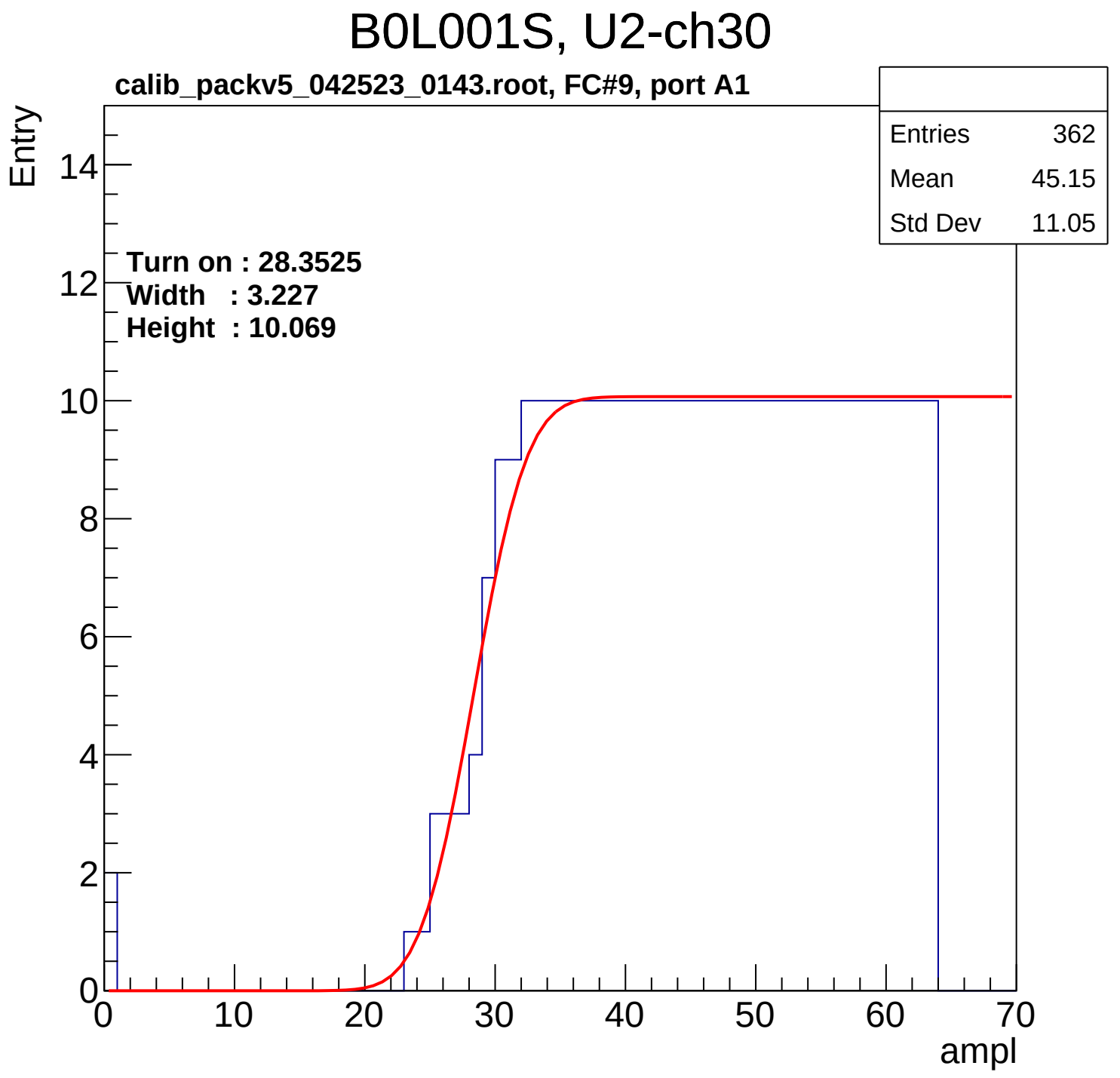
B0L001S, U2-ch30
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 45.15
Std Dev 11.05
Turn on : 28.3525
Width : 3.227
Height : 10.069
Entry
ampl
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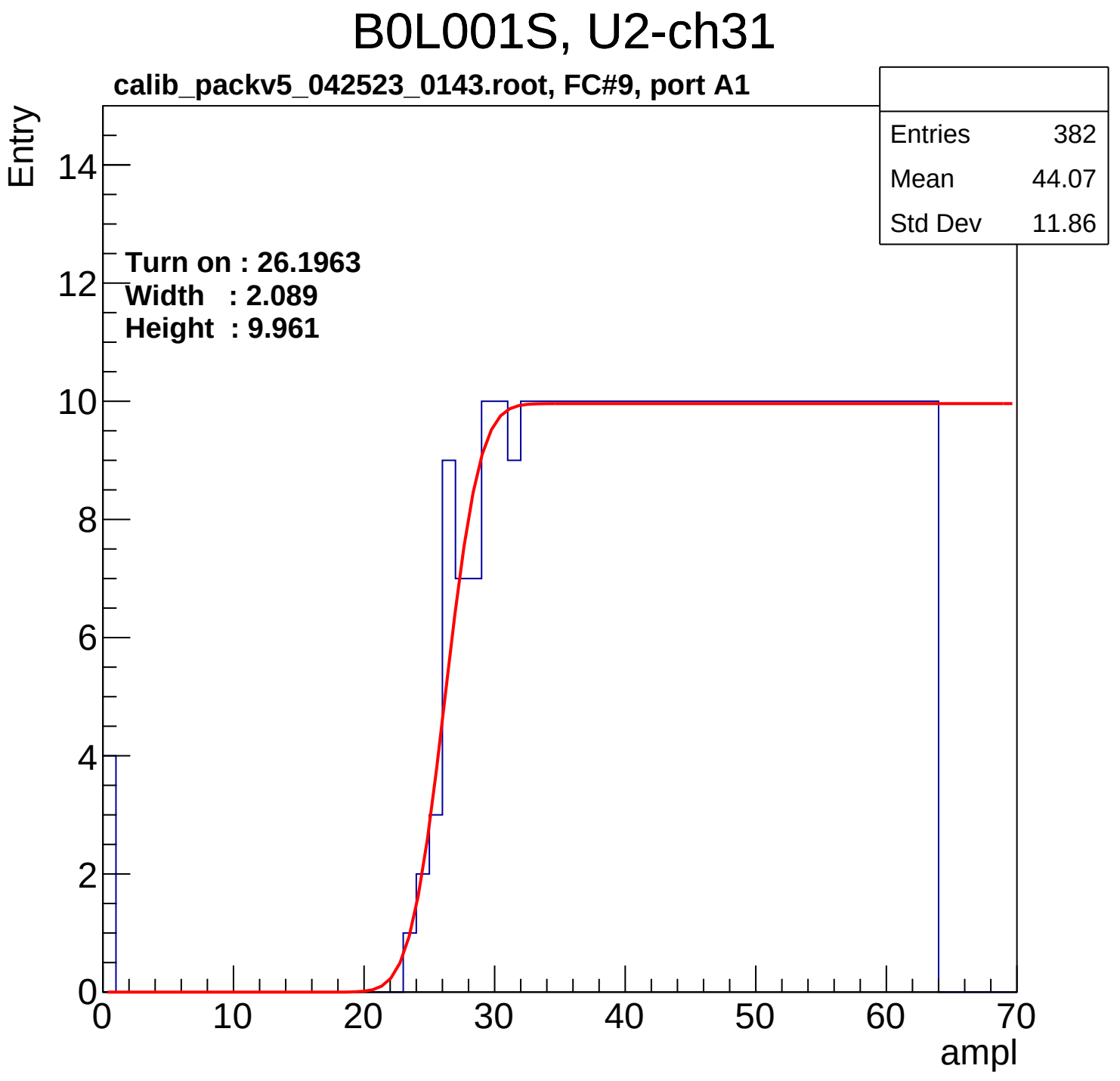
B0L001S, U2-ch31
calib_packv5_042523_0143.root, FC#9, port A1
Entries 382
Mean 44.07
Std Dev 11.86
Turn on : 26.1963
Width : 2.089
Height : 9.961
Entry
ampl
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6
8
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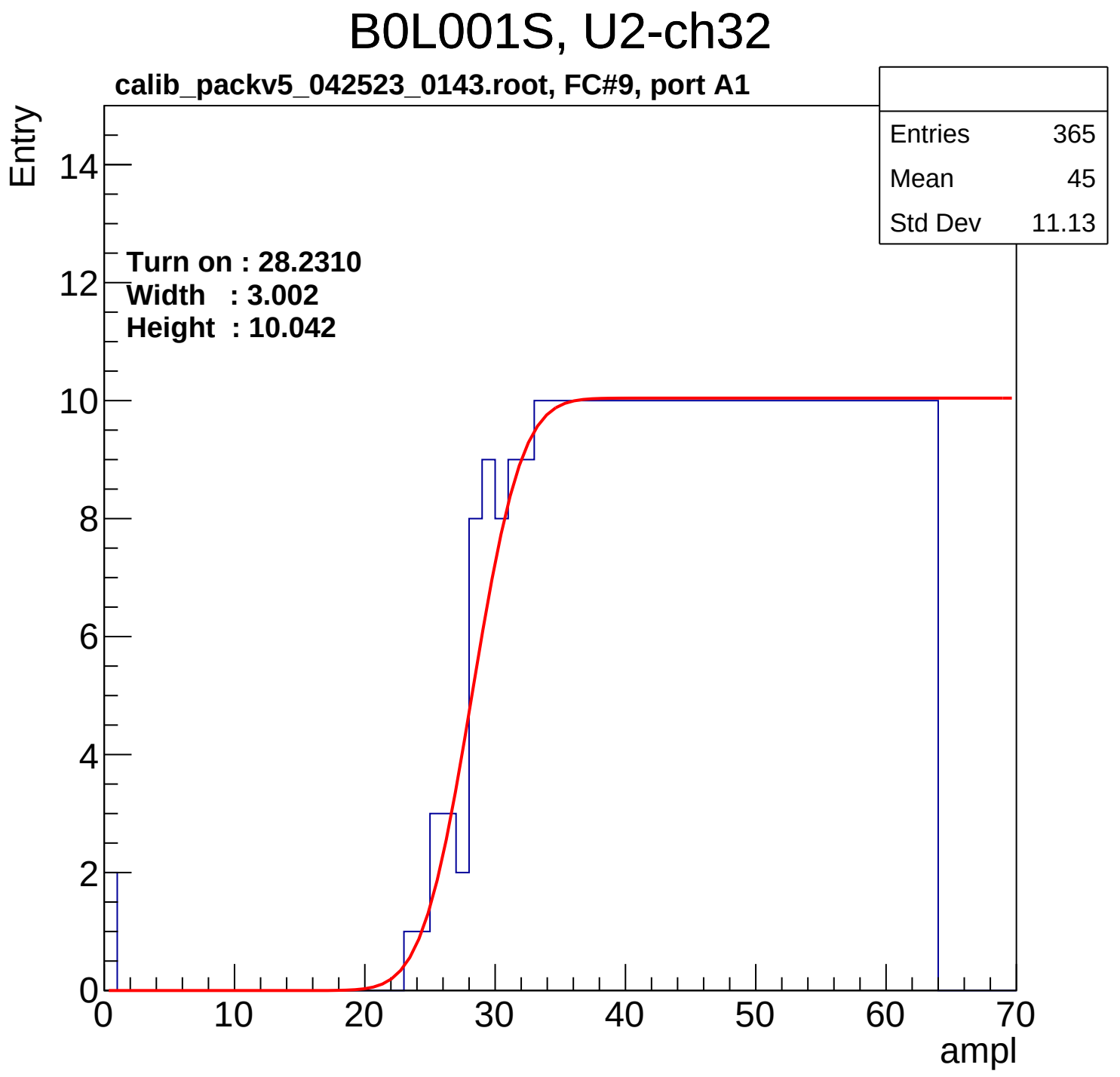
B0L001S, U2-ch32
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 45
Std Dev 11.13
Turn on : 28.2310
Width : 3.002
Height : 10.042
Entry
ampl
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8
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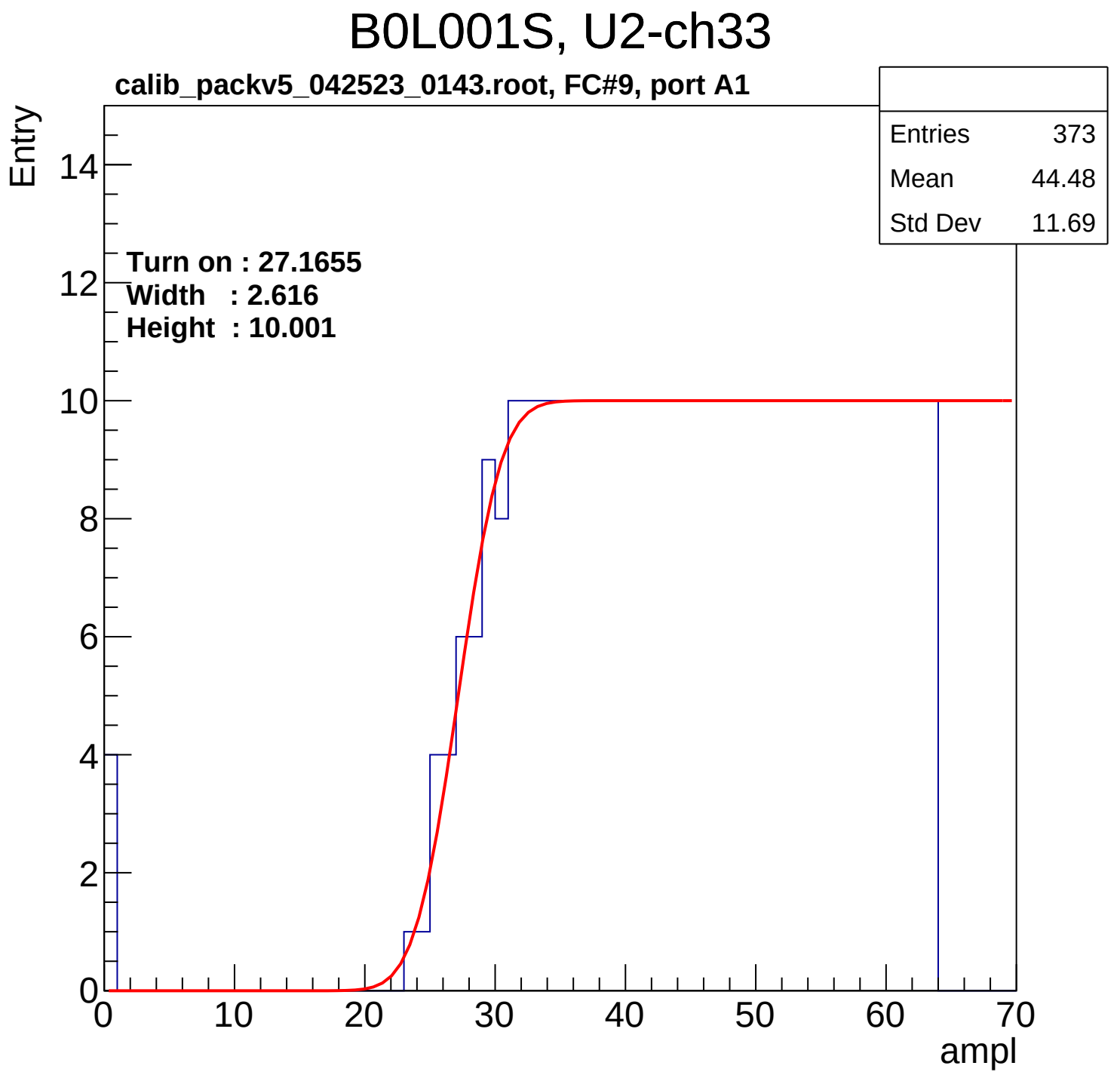
B0L001S, U2-ch33
calib_packv5_042523_0143.root, FC#9, port A1
Entries 373
Mean 44.48
Std Dev 11.69
Turn on : 27.1655
Width : 2.616
Height : 10.001
Entry
ampl
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6
8
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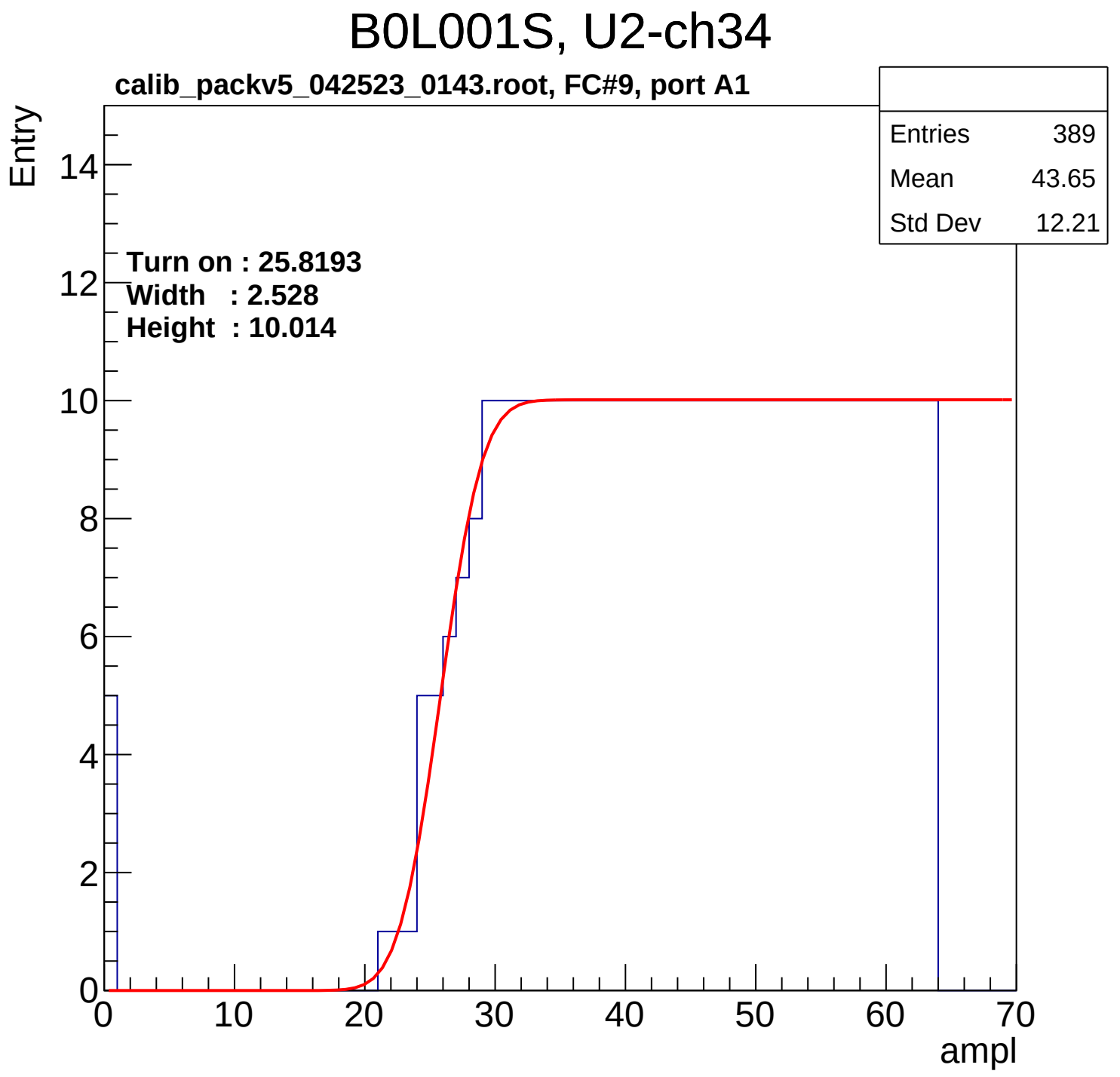
B0L001S, U2-ch34
calib_packv5_042523_0143.root, FC#9, port A1
Entries 389
Mean 43.65
Std Dev 12.21
Turn on : 25.8193
Width : 2.528
Height : 10.014
Entry
ampl
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6
8
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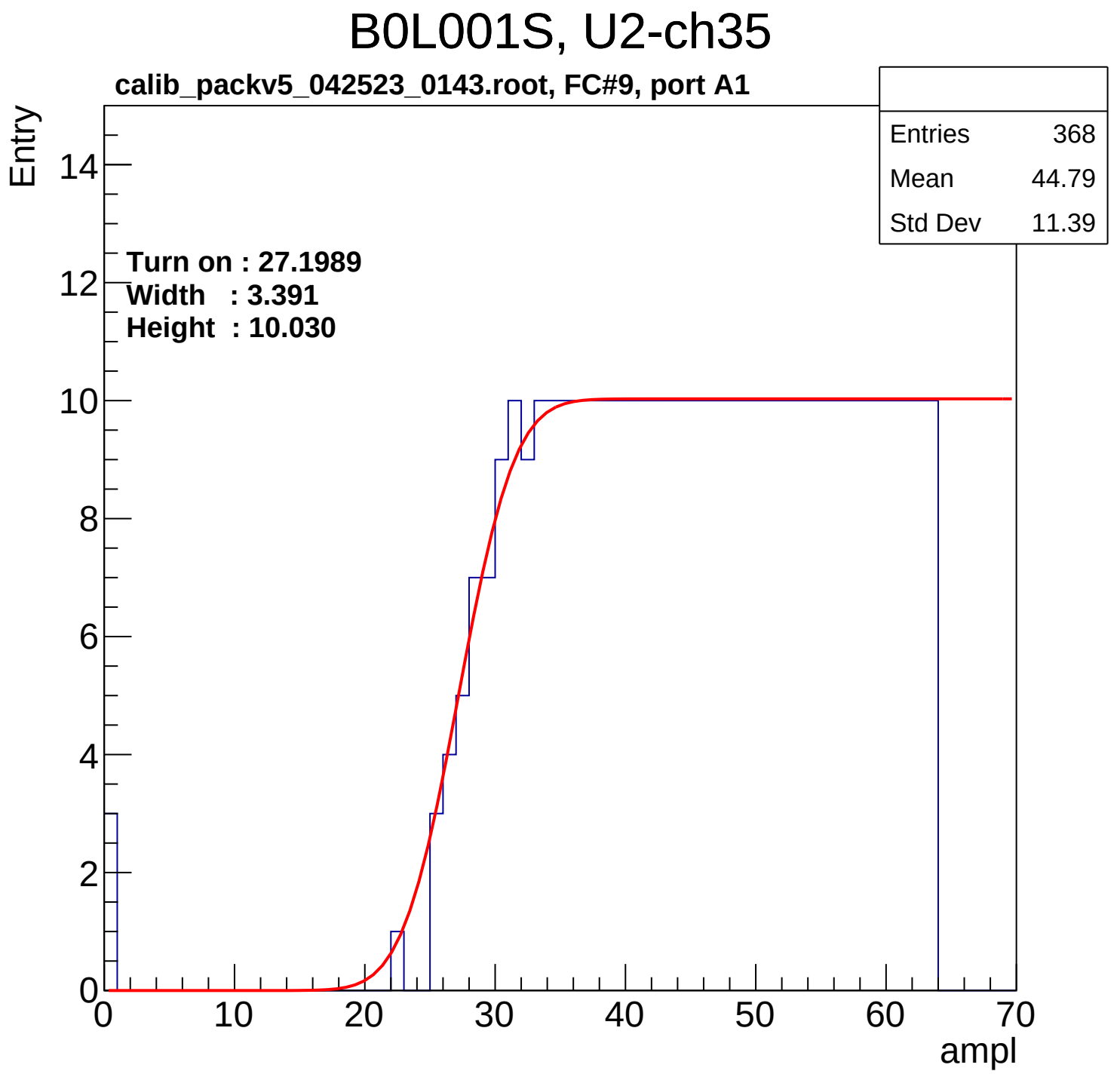
B0L001S, U2-ch35
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.79
Std Dev 11.39
Turn on : 27.1989
Width : 3.391
Height : 10.030
Entry
ampl
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6
8
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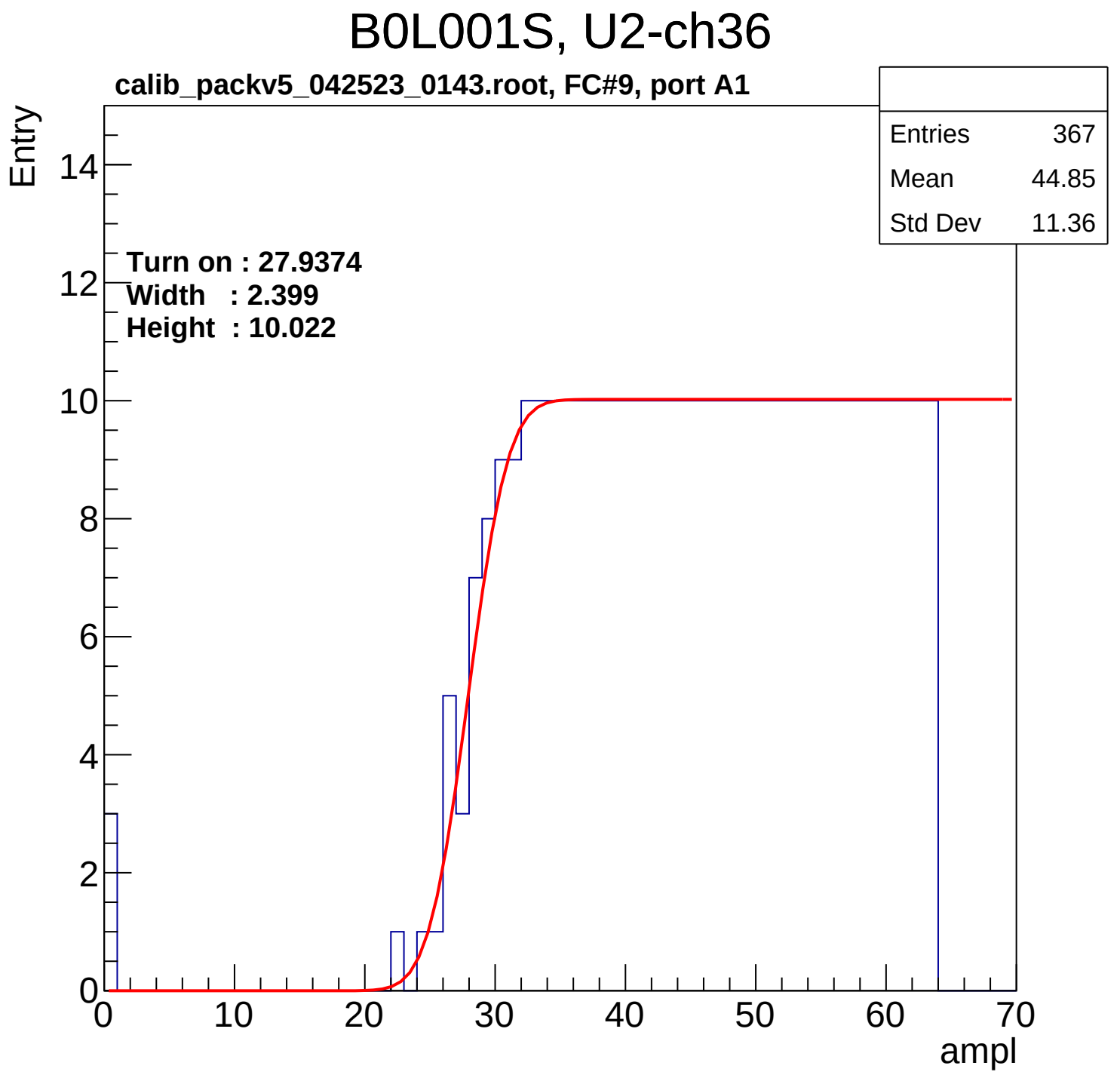
B0L001S, U2-ch36
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.85
Std Dev 11.36
Turn on : 27.9374
Width : 2.399
Height : 10.022
Entry
ampl
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2
4
6
8
10
12
14
0
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60
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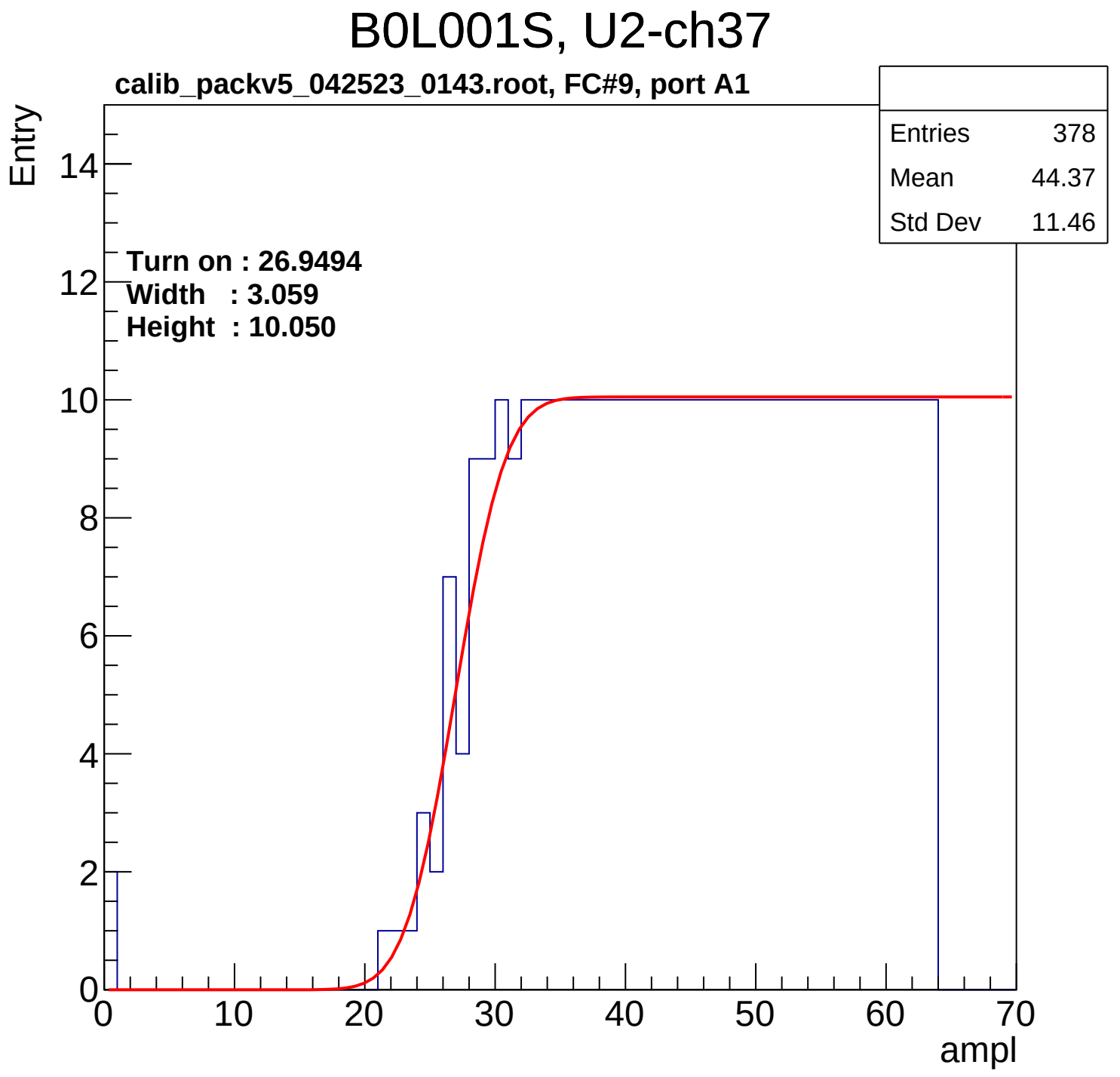
B0L001S, U2-ch37
calib_packv5_042523_0143.root, FC#9, port A1
Entries 378
Mean 44.37
Std Dev 11.46
Turn on : 26.9494
Width : 3.059
Height : 10.050
Entry
ampl
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4
6
8
10
12
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0
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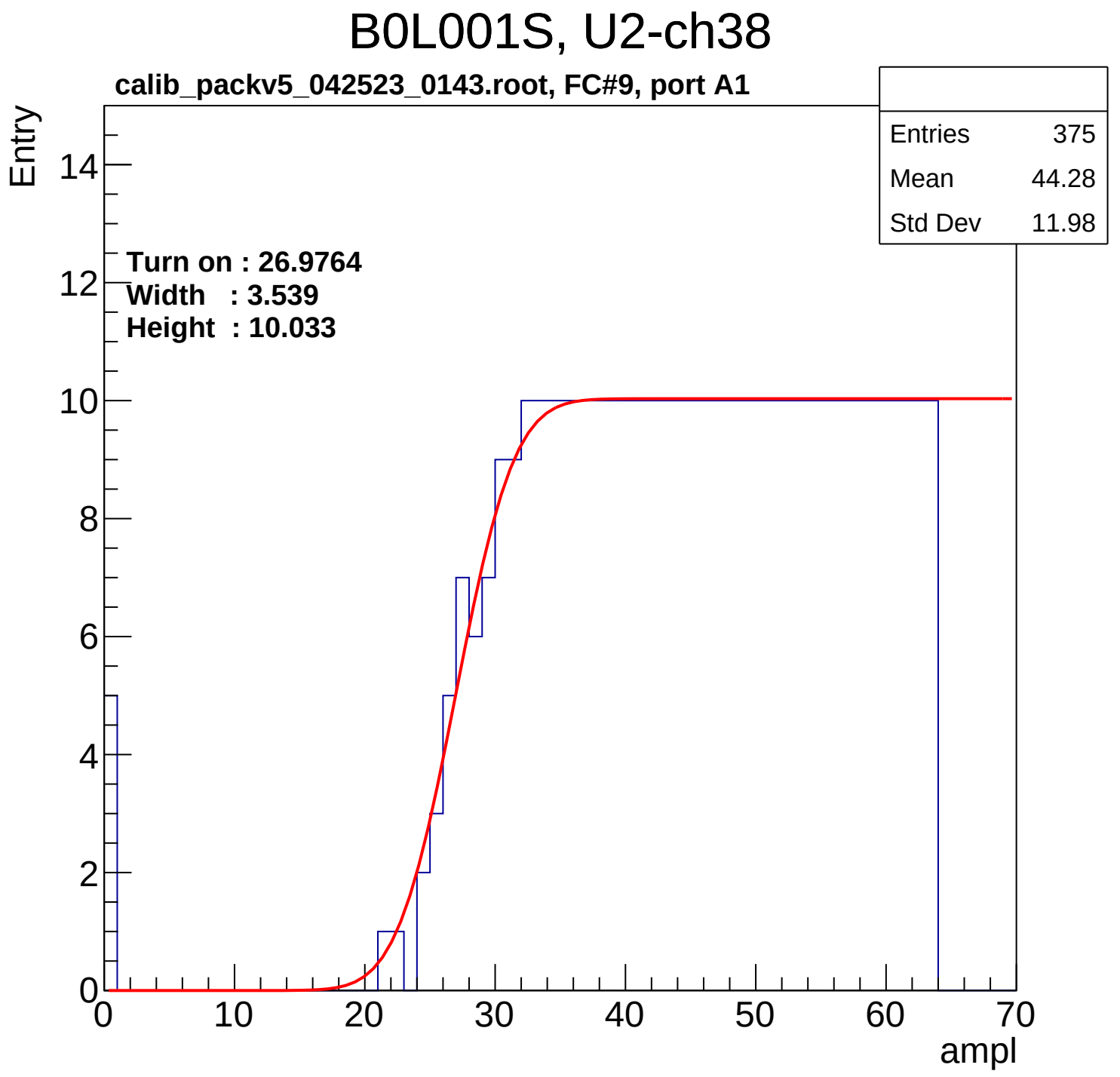
B0L001S, U2-ch38
calib_packv5_042523_0143.root, FC#9, port A1
Entries 375
Mean 44.28
Std Dev 11.98
Turn on : 26.9764
Width : 3.539
Height : 10.033
Entry
ampl
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2
4
6
8
10
12
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0
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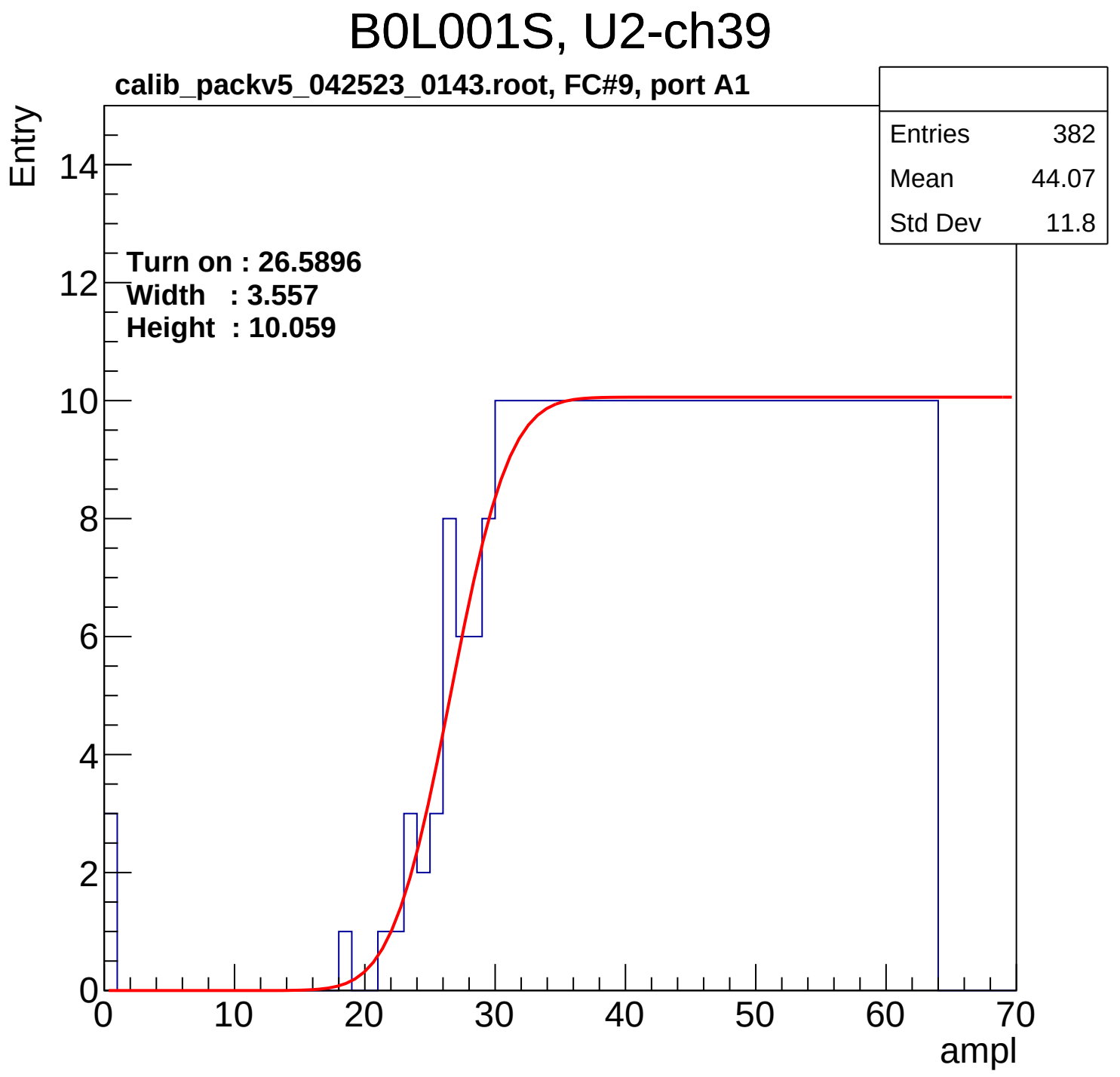
B0L001S, U2-ch39
calib_packv5_042523_0143.root, FC#9, port A1
Entries 382
Mean 44.07
Std Dev 11.8
Turn on : 26.5896
Width : 3.557
Height : 10.059
Entry
ampl
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6
8
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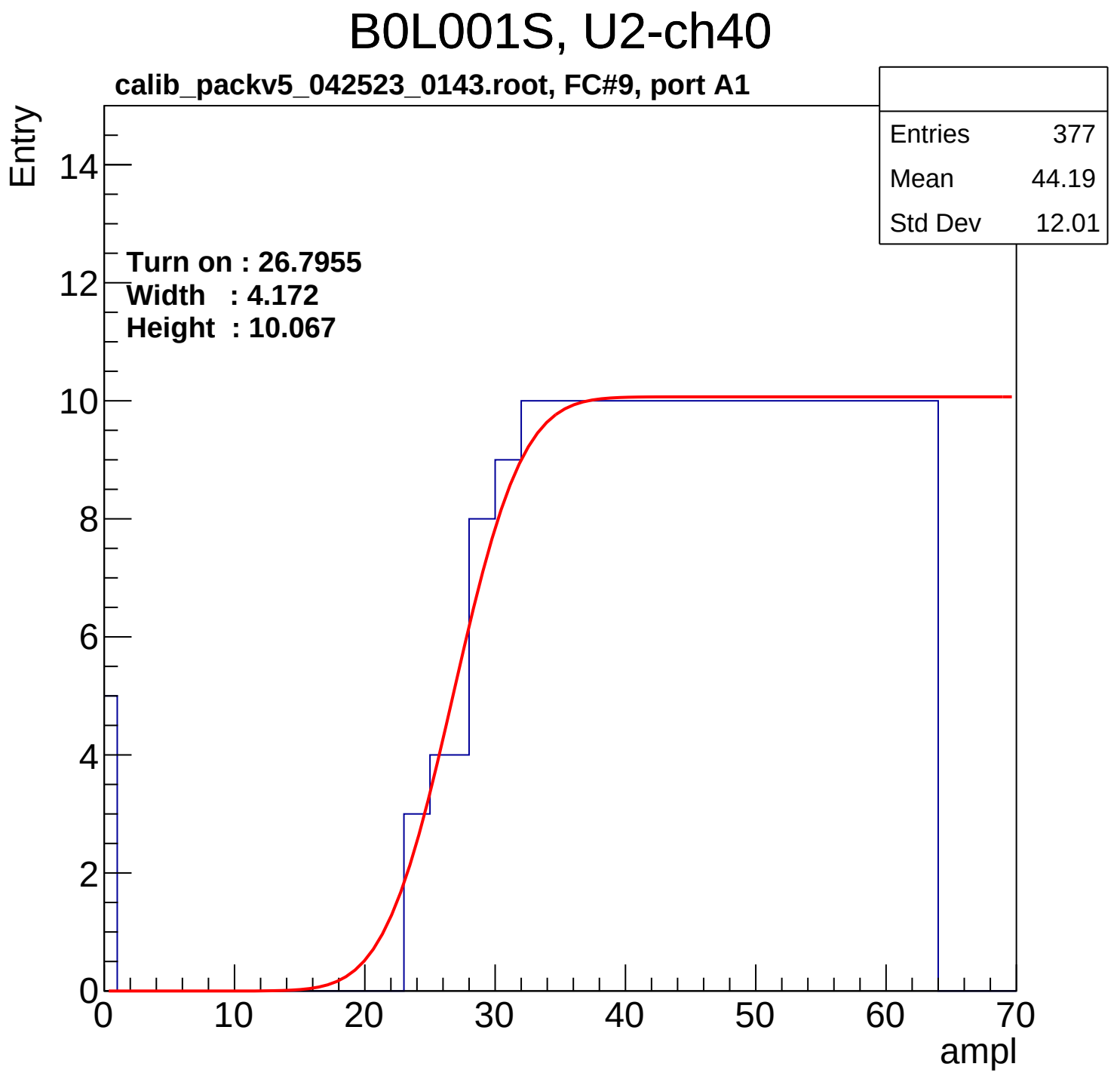
B0L001S, U2-ch40
calib_packv5_042523_0143.root, FC#9, port A1
Entries 377
Mean 44.19
Std Dev 12.01
Turn on : 26.7955
Width : 4.172
Height : 10.067
Entry
ampl
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8
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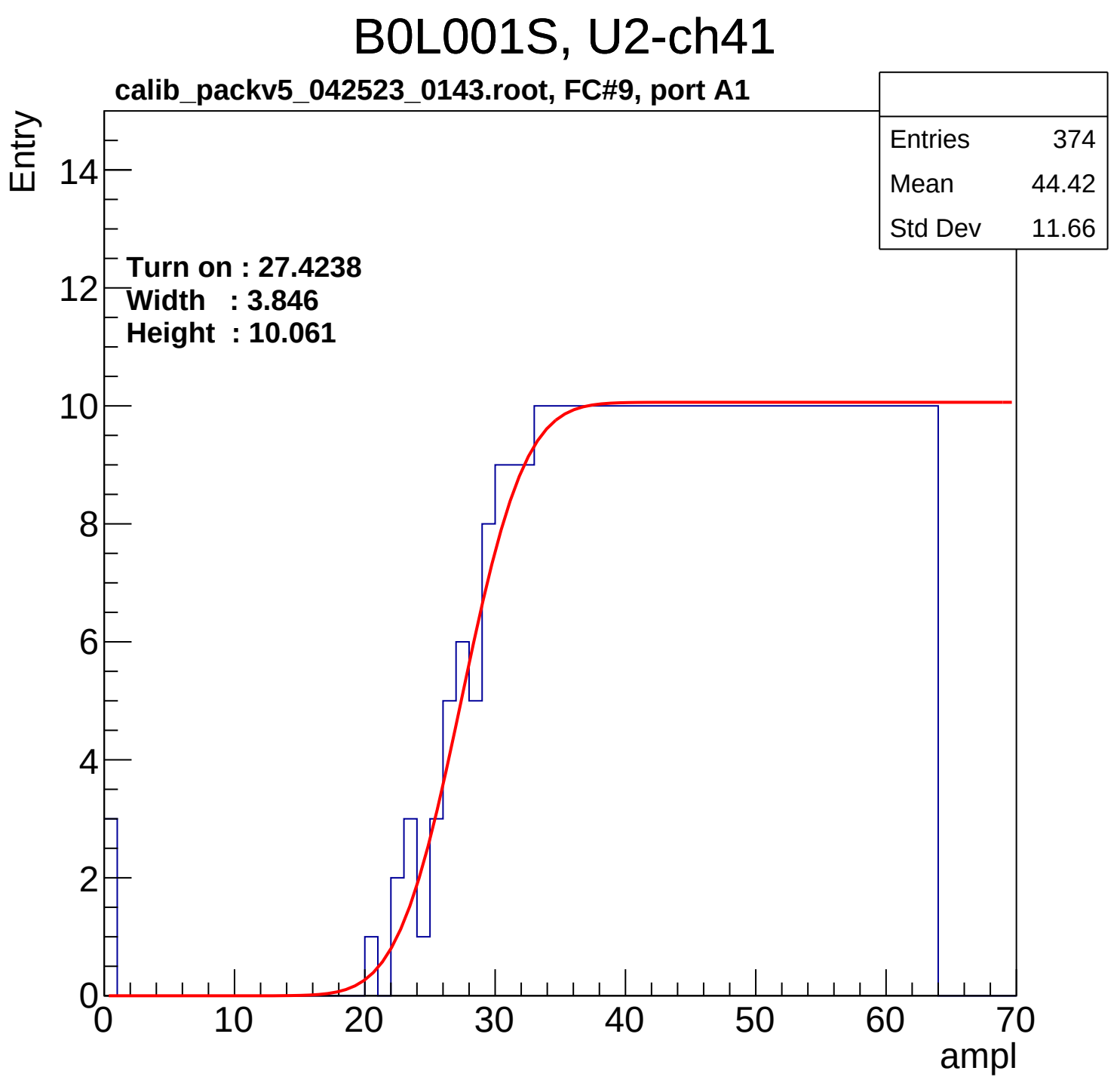
B0L001S, U2-ch41
calib_packv5_042523_0143.root, FC#9, port A1
Entries 374
Mean 44.42
Std Dev 11.66
Turn on : 27.4238
Width : 3.846
Height : 10.061
Entry
ampl
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2
4
6
8
10
12
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0
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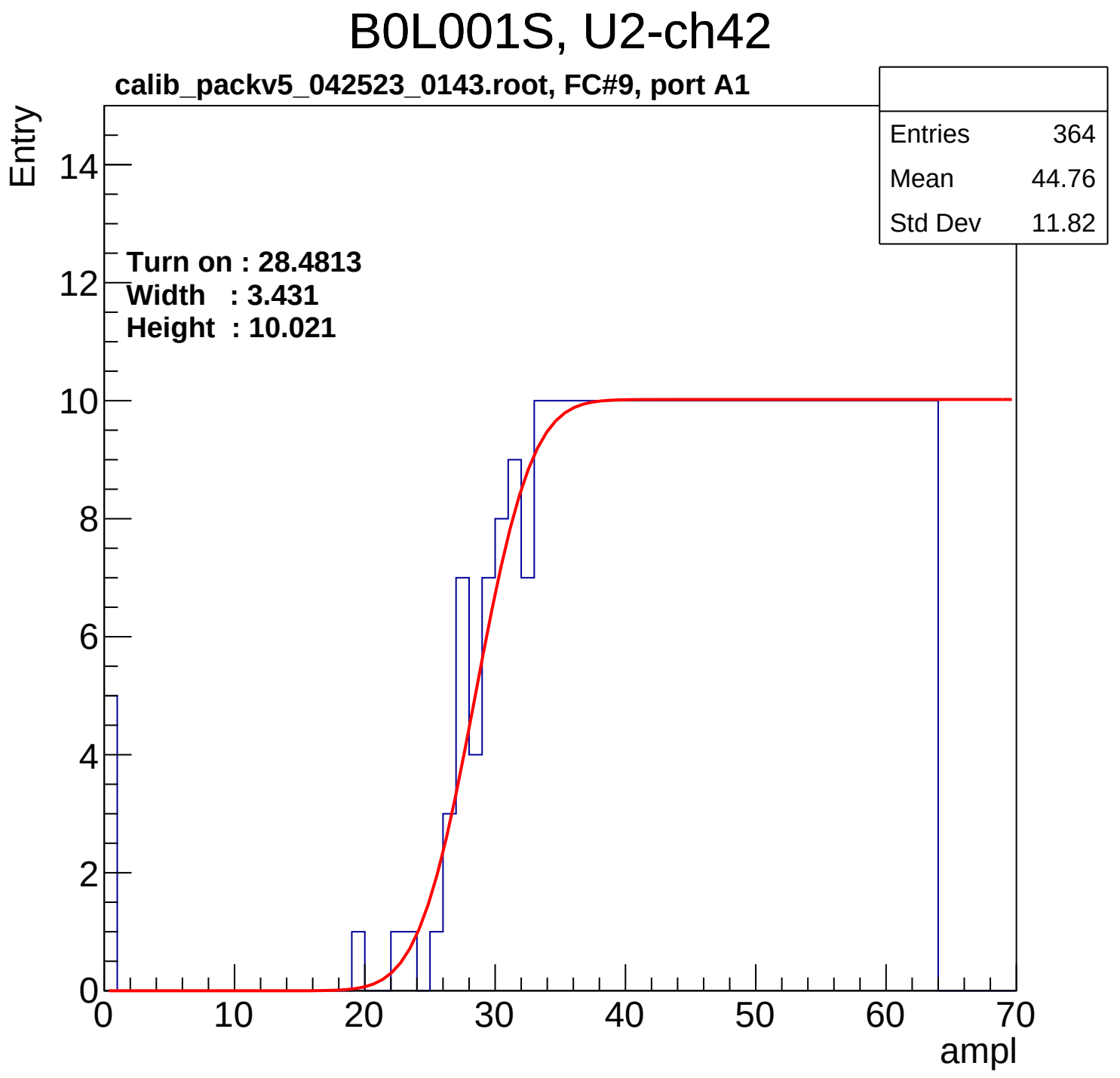
B0L001S, U2-ch42
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 44.76
Std Dev 11.82
Turn on : 28.4813
Width : 3.431
Height : 10.021
Entry
ampl
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4
6
8
10
12
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0
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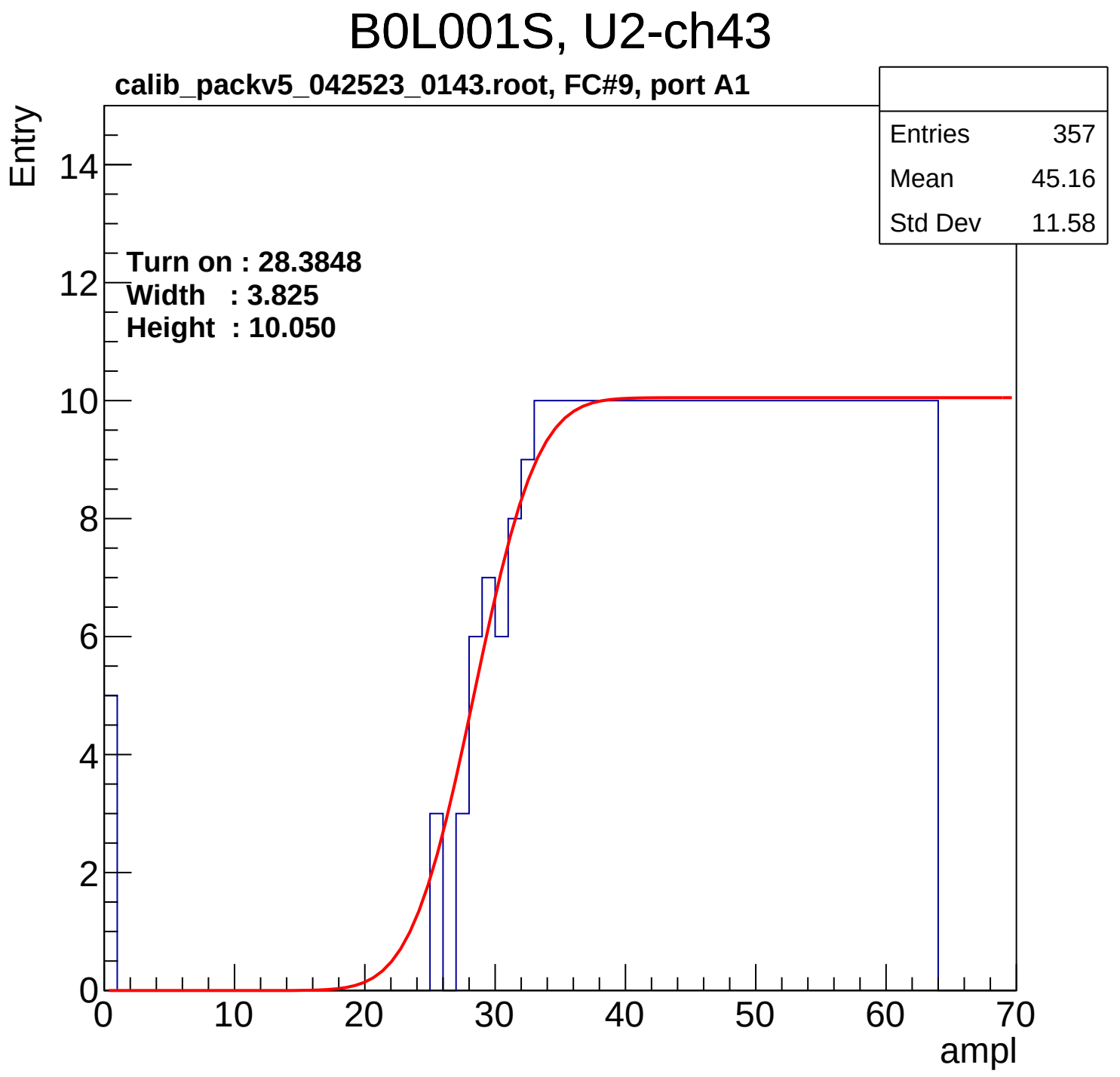
B0L001S, U2-ch43
calib_packv5_042523_0143.root, FC#9, port A1
Entries 357
Mean 45.16
Std Dev 11.58
Turn on : 28.3848
Width : 3.825
Height : 10.050
Entry
ampl
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6
8
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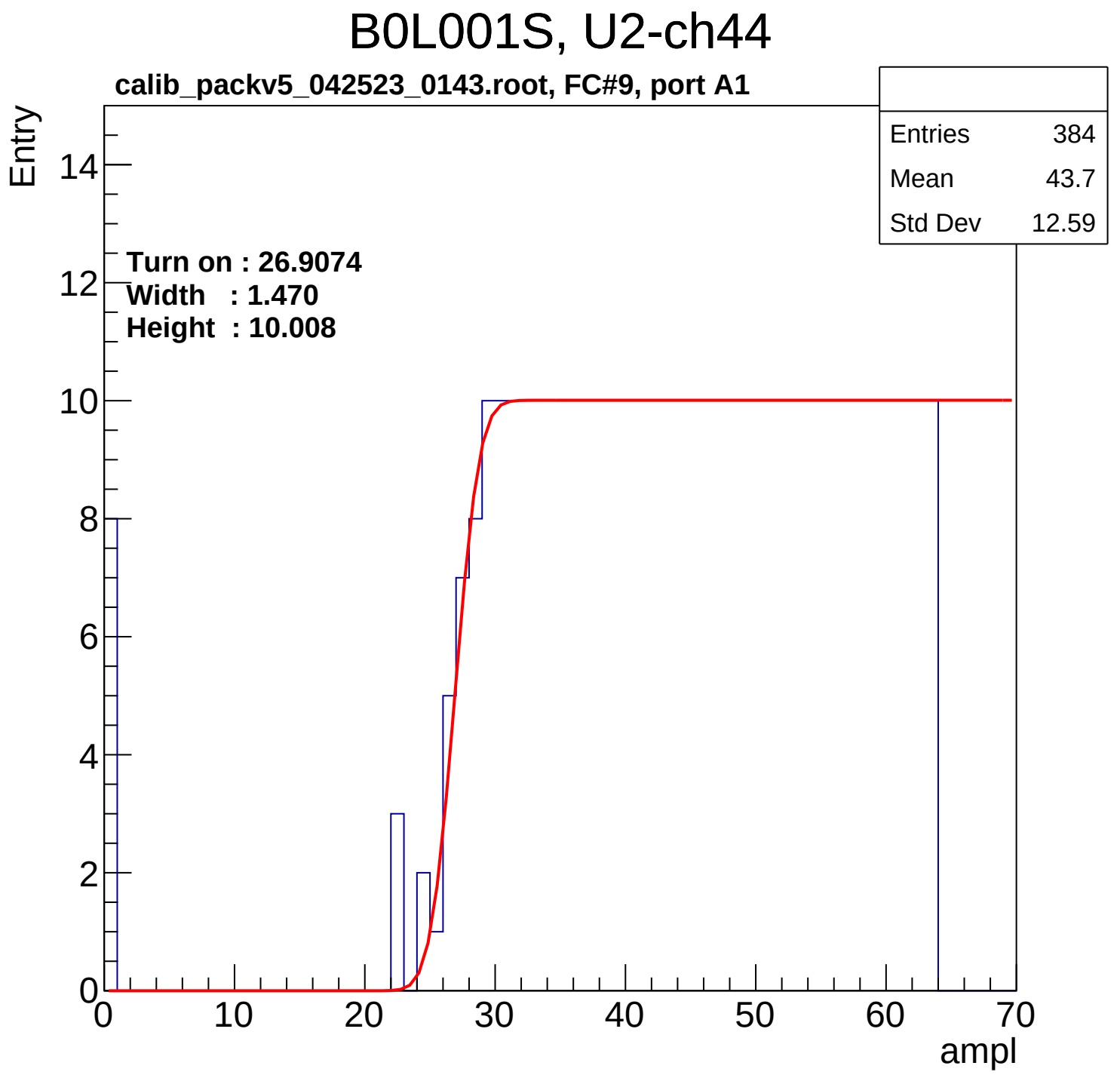
B0L001S, U2-ch44
calib_packv5_042523_0143.root, FC#9, port A1
Entries 384
Mean 43.7
Std Dev 12.59
Turn on : 26.9074
Width : 1.470
Height : 10.008
Entry
ampl
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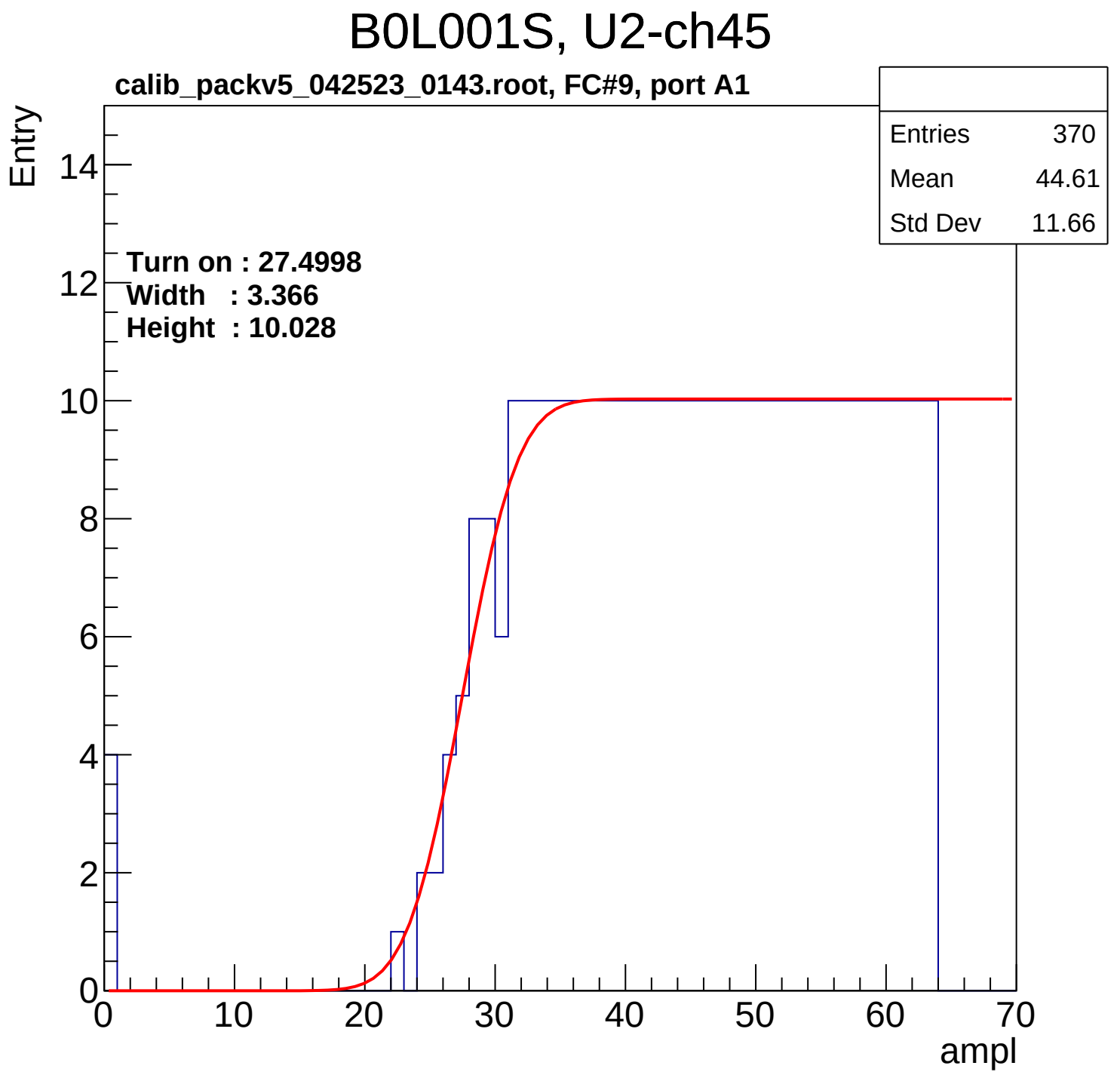
B0L001S, U2-ch45
calib_packv5_042523_0143.root, FC#9, port A1
Entries 370
Mean 44.61
Std Dev 11.66
Turn on : 27.4998
Width : 3.366
Height : 10.028
Entry
ampl
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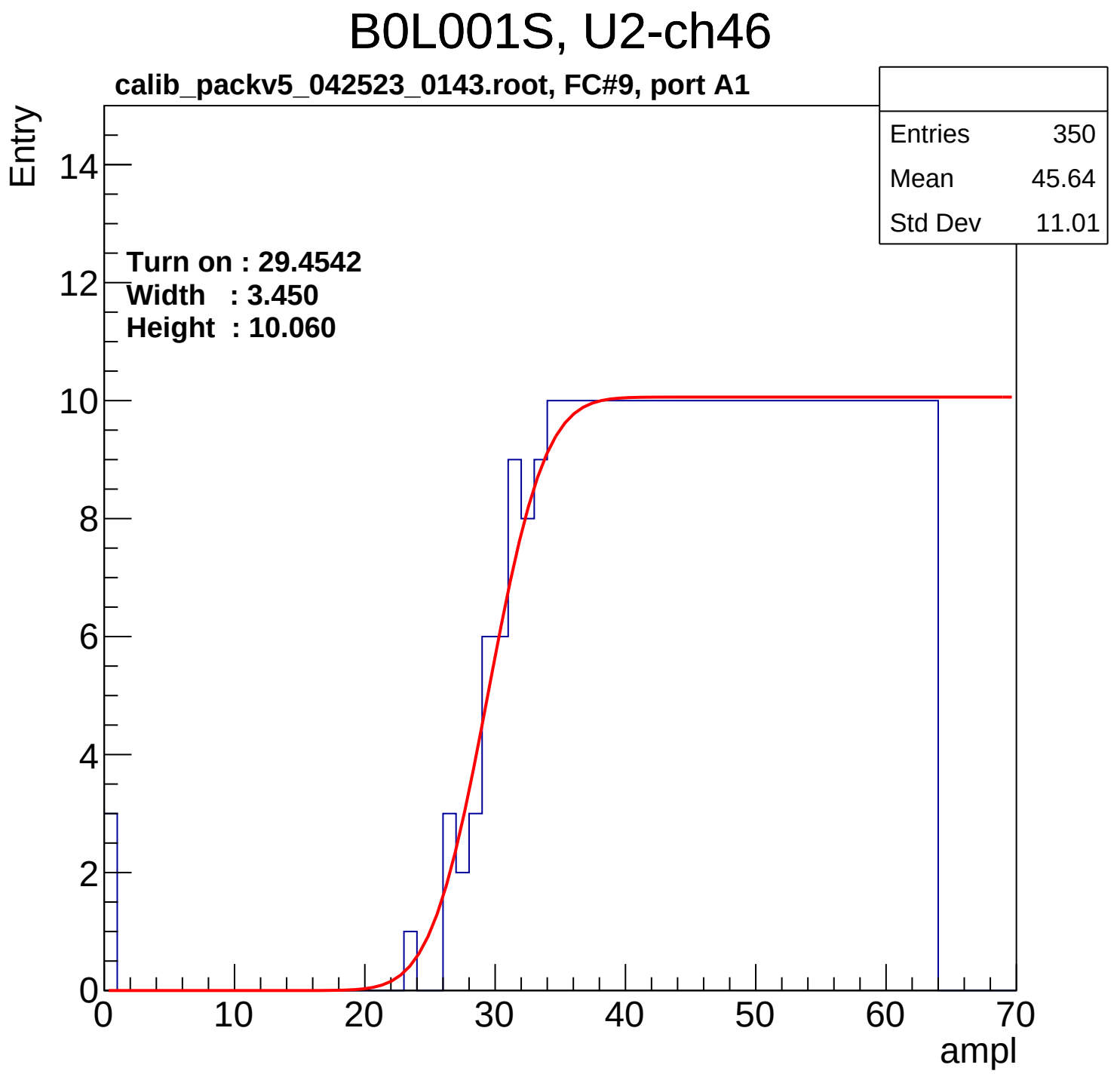
B0L001S, U2-ch46
calib_packv5_042523_0143.root, FC#9, port A1
Entries 350
Mean 45.64
Std Dev 11.01
Turn on : 29.4542
Width : 3.450
Height : 10.060
Entry
ampl
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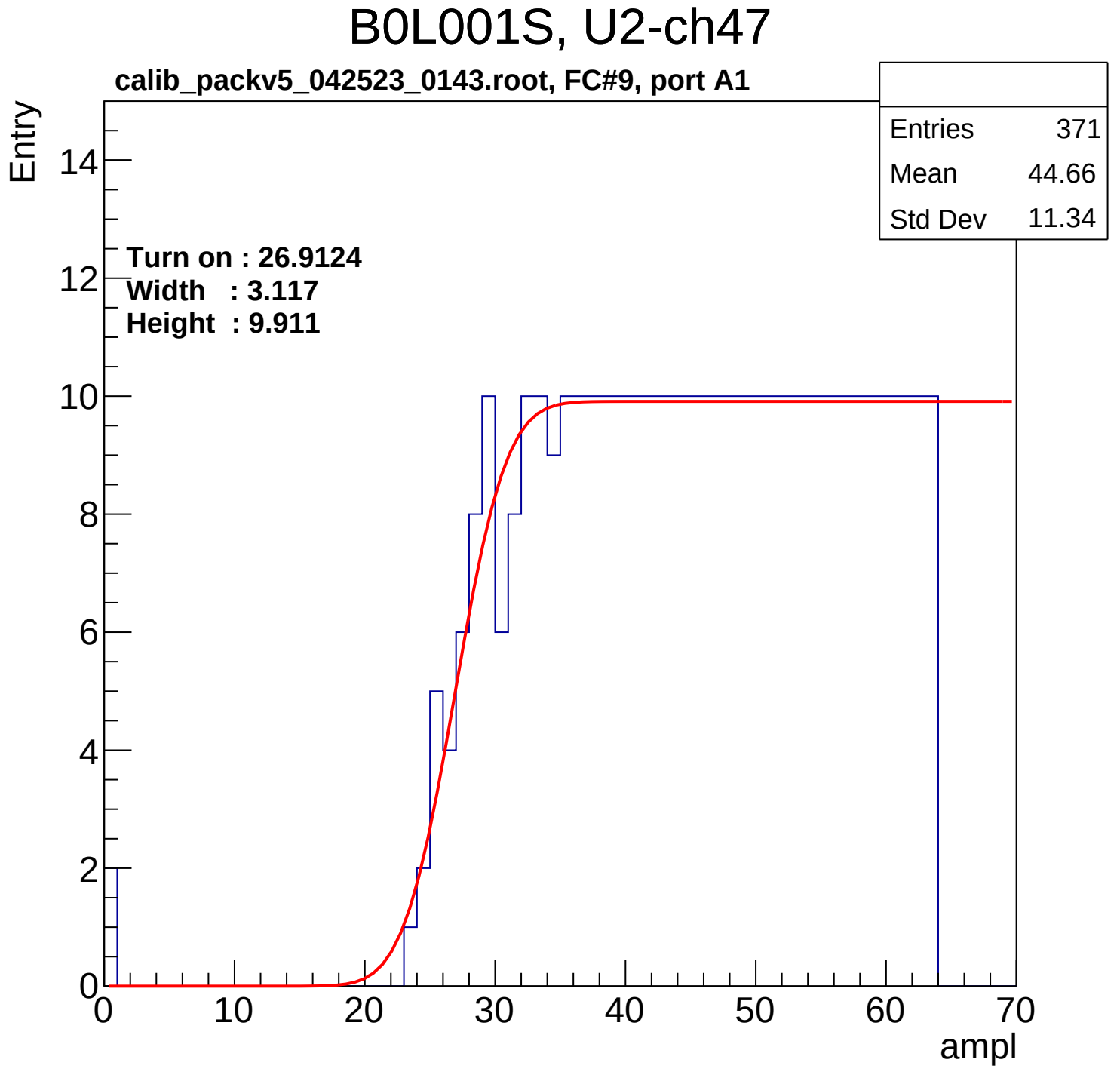
B0L001S, U2-ch47
calib_packv5_042523_0143.root, FC#9, port A1
Entries 371
Mean 44.66
Std Dev 11.34
Turn on : 26.9124
Width : 3.117
Height : 9.911
Entry
ampl
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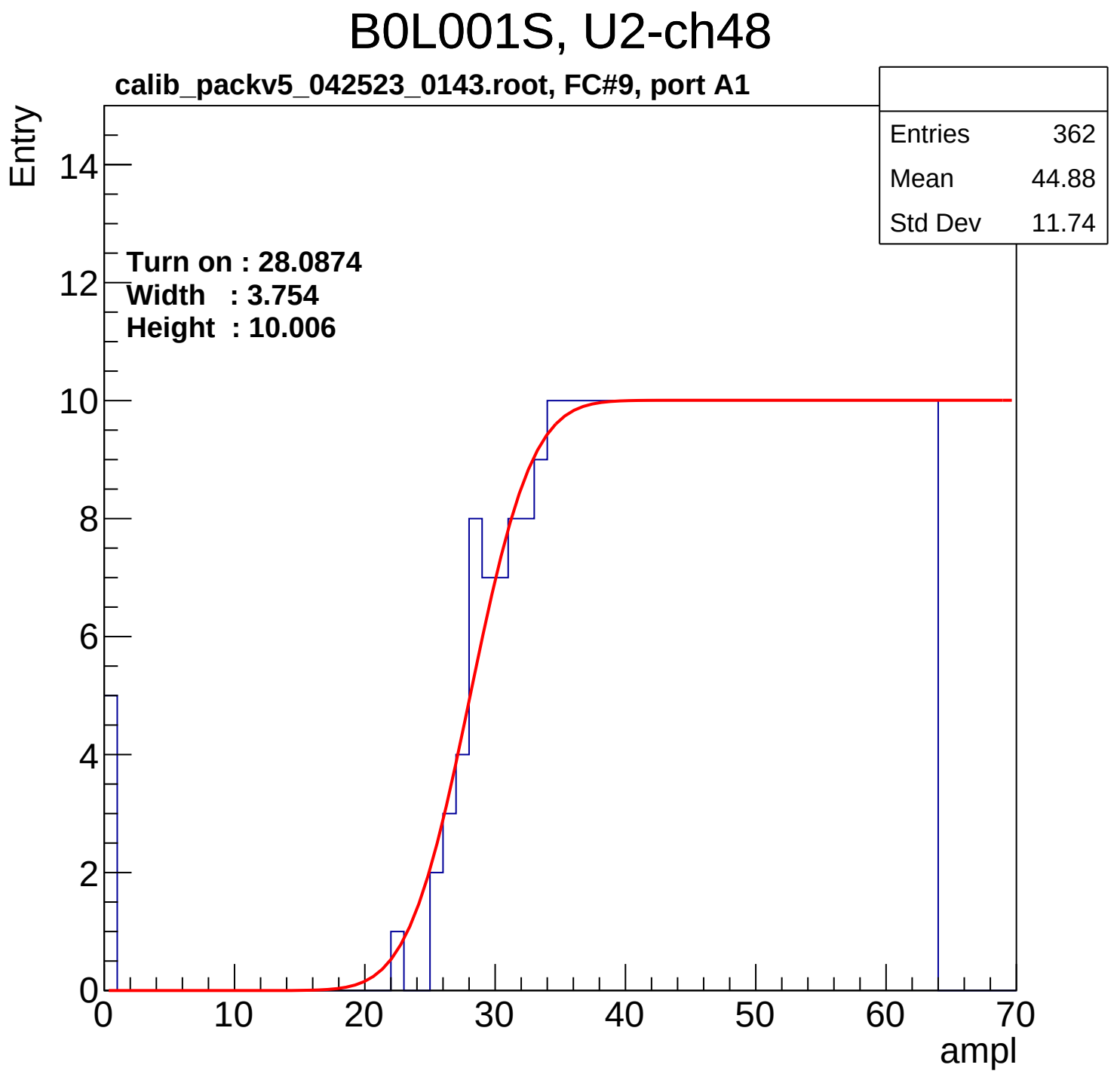
B0L001S, U2-ch48
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 44.88
Std Dev 11.74
Turn on : 28.0874
Width : 3.754
Height : 10.006
Entry
ampl
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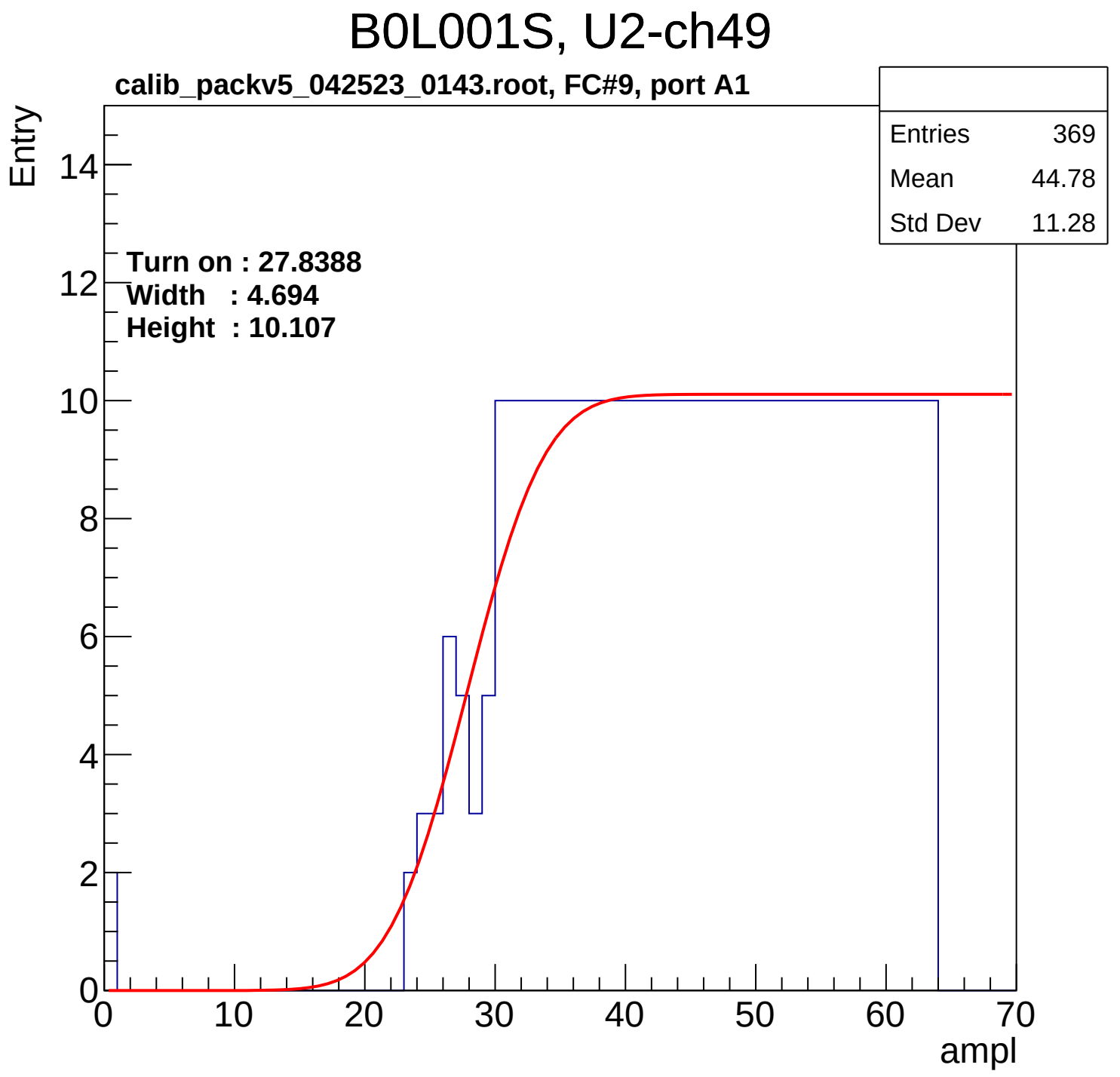
B0L001S, U2-ch49
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.78
Std Dev 11.28
Turn on : 27.8388
Width : 4.694
Height : 10.107
Entry
ampl
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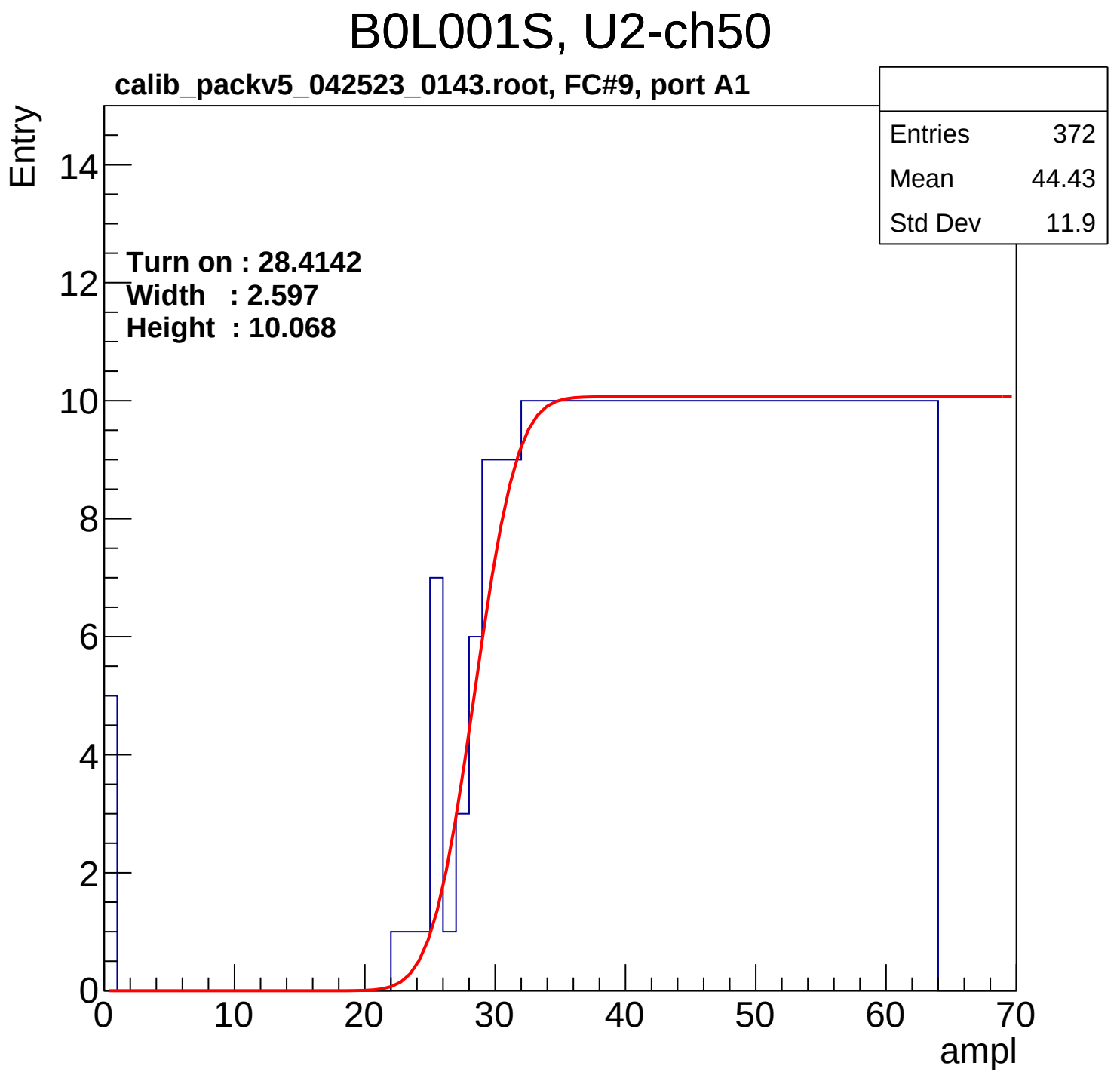
B0L001S, U2-ch50
calib_packv5_042523_0143.root, FC#9, port A1
Entries 372
Mean 44.43
Std Dev 11.9
Turn on : 28.4142
Width : 2.597
Height : 10.068
Entry
ampl
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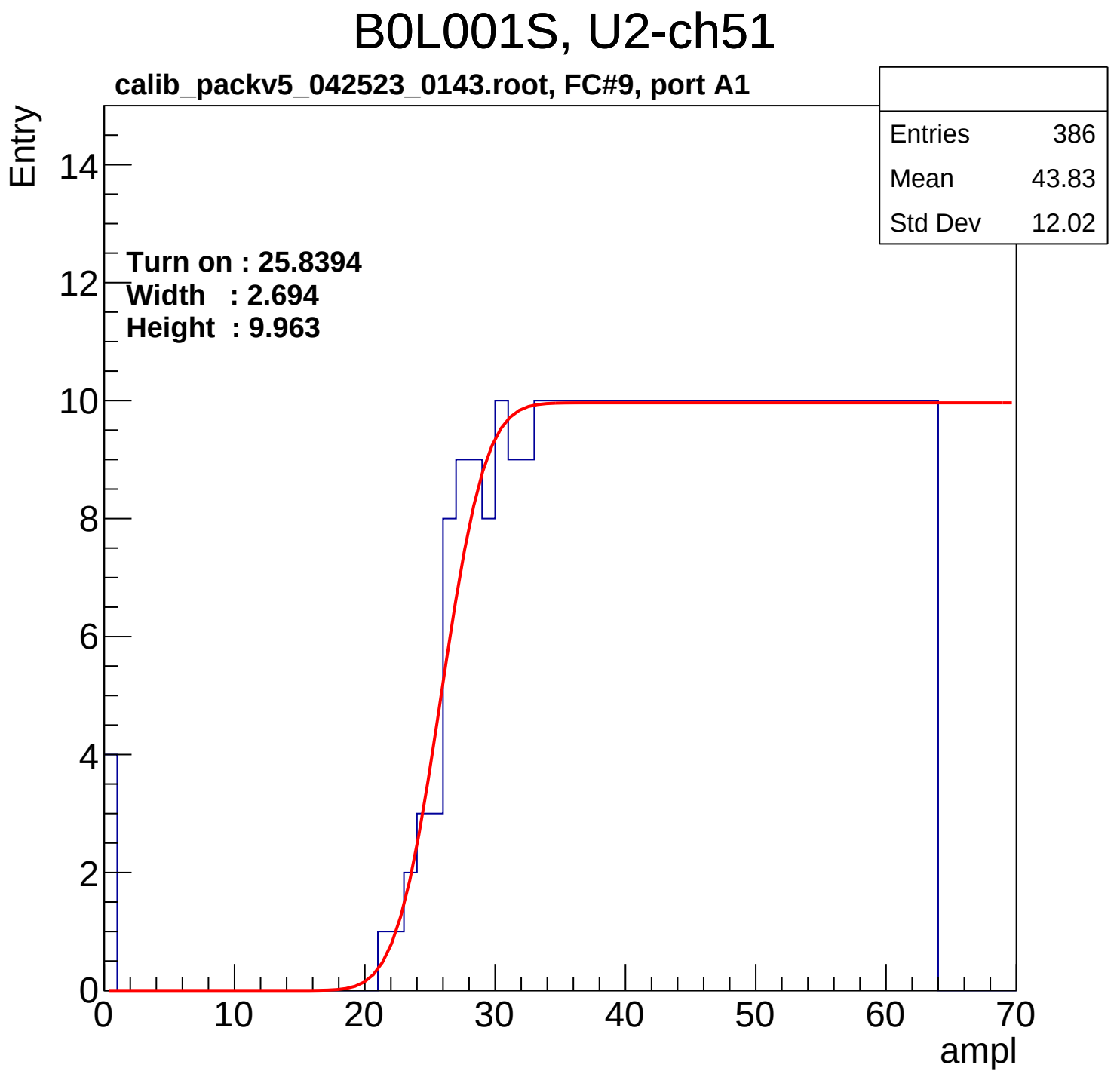
B0L001S, U2-ch51
calib_packv5_042523_0143.root, FC#9, port A1
Entries 386
Mean 43.83
Std Dev 12.02
Turn on : 25.8394
Width : 2.694
Height : 9.963
Entry
ampl
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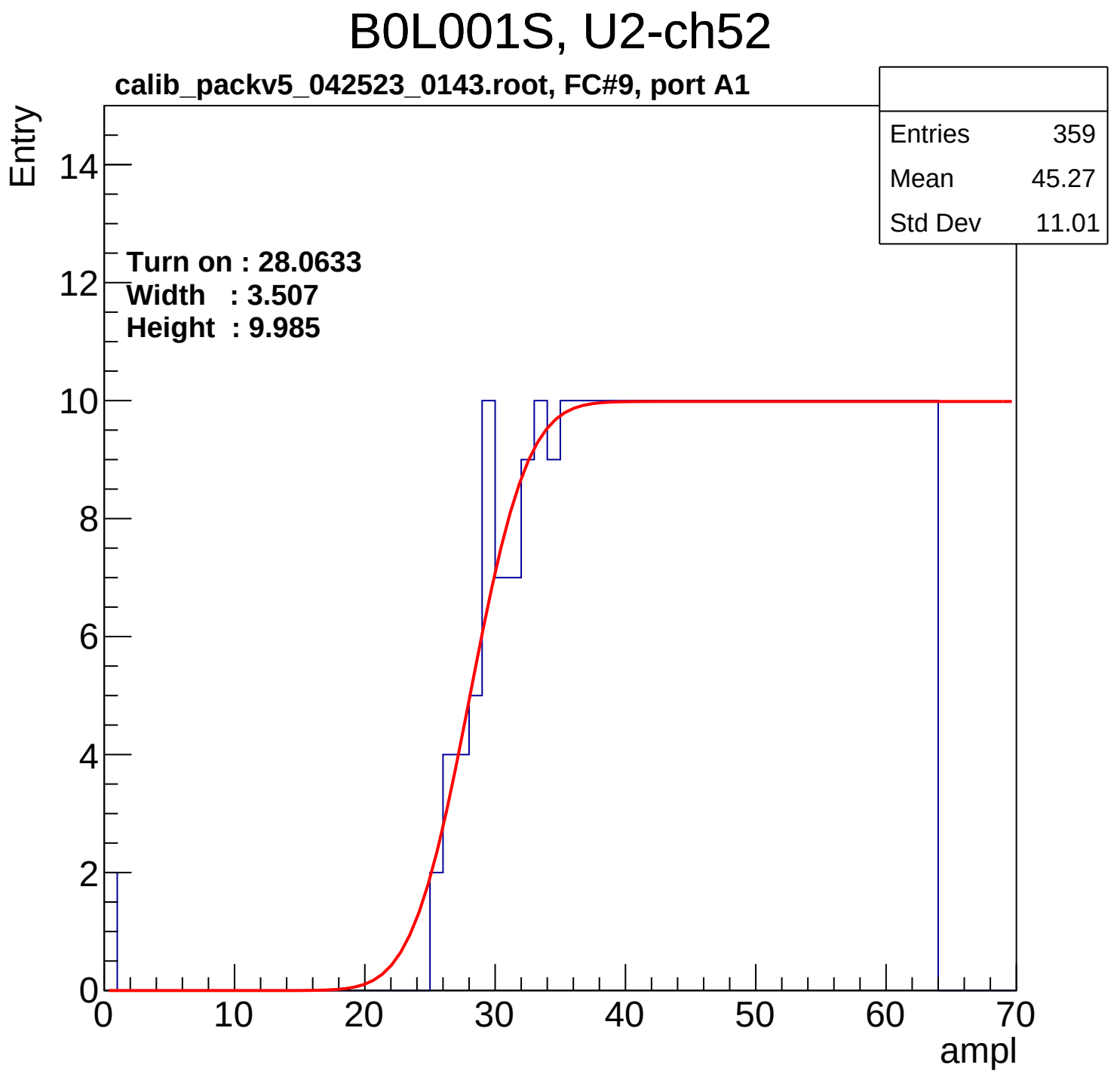
B0L001S, U2-ch52
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 45.27
Std Dev 11.01
Turn on : 28.0633
Width : 3.507
Height : 9.985
Entry
ampl
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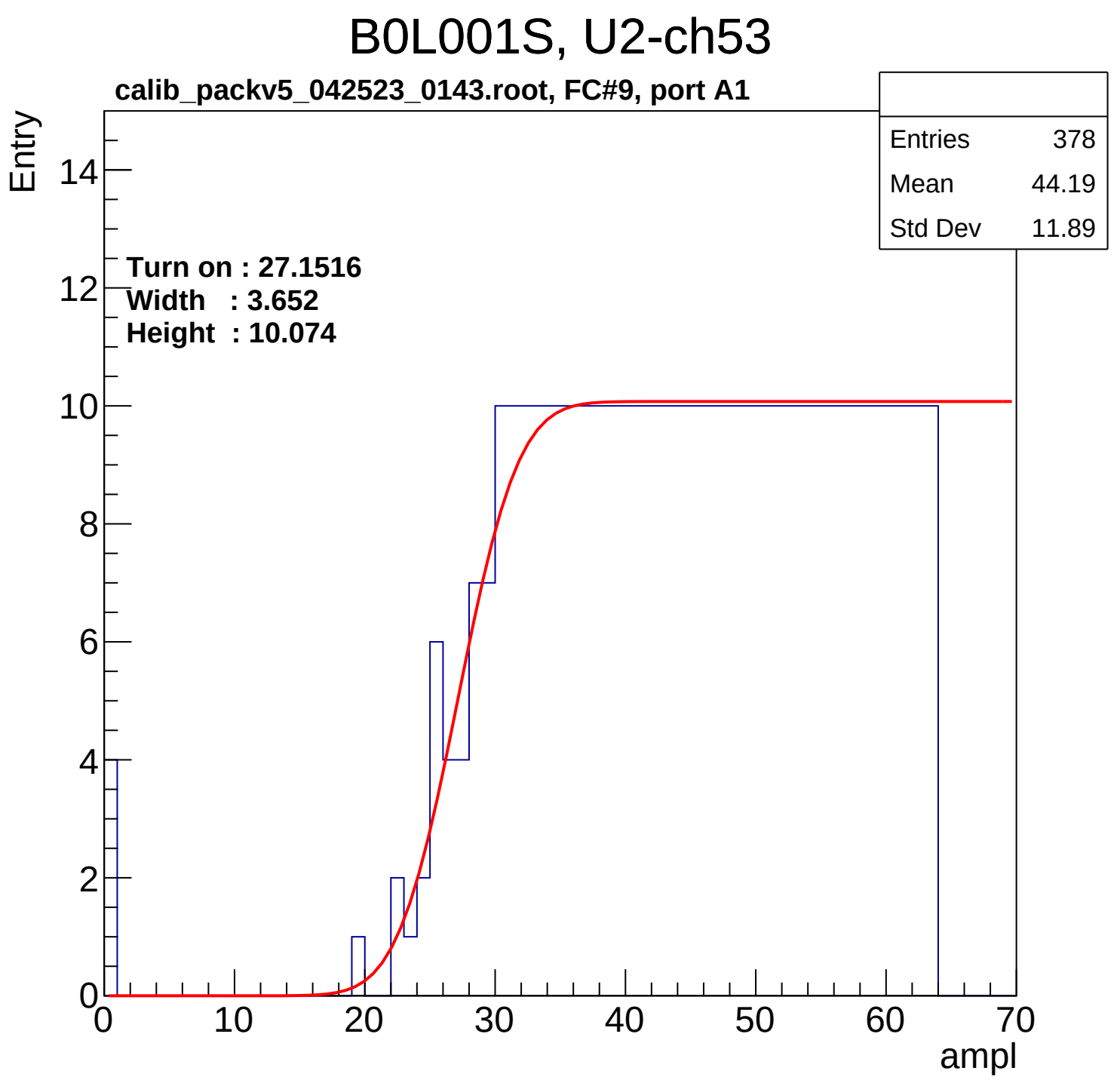
B0L001S, U2-ch53
calib_packv5_042523_0143.root, FC#9, port A1
Entries 378
Mean 44.19
Std Dev 11.89
Turn on : 27.1516
Width : 3.652
Height : 10.074
Entry
ampl
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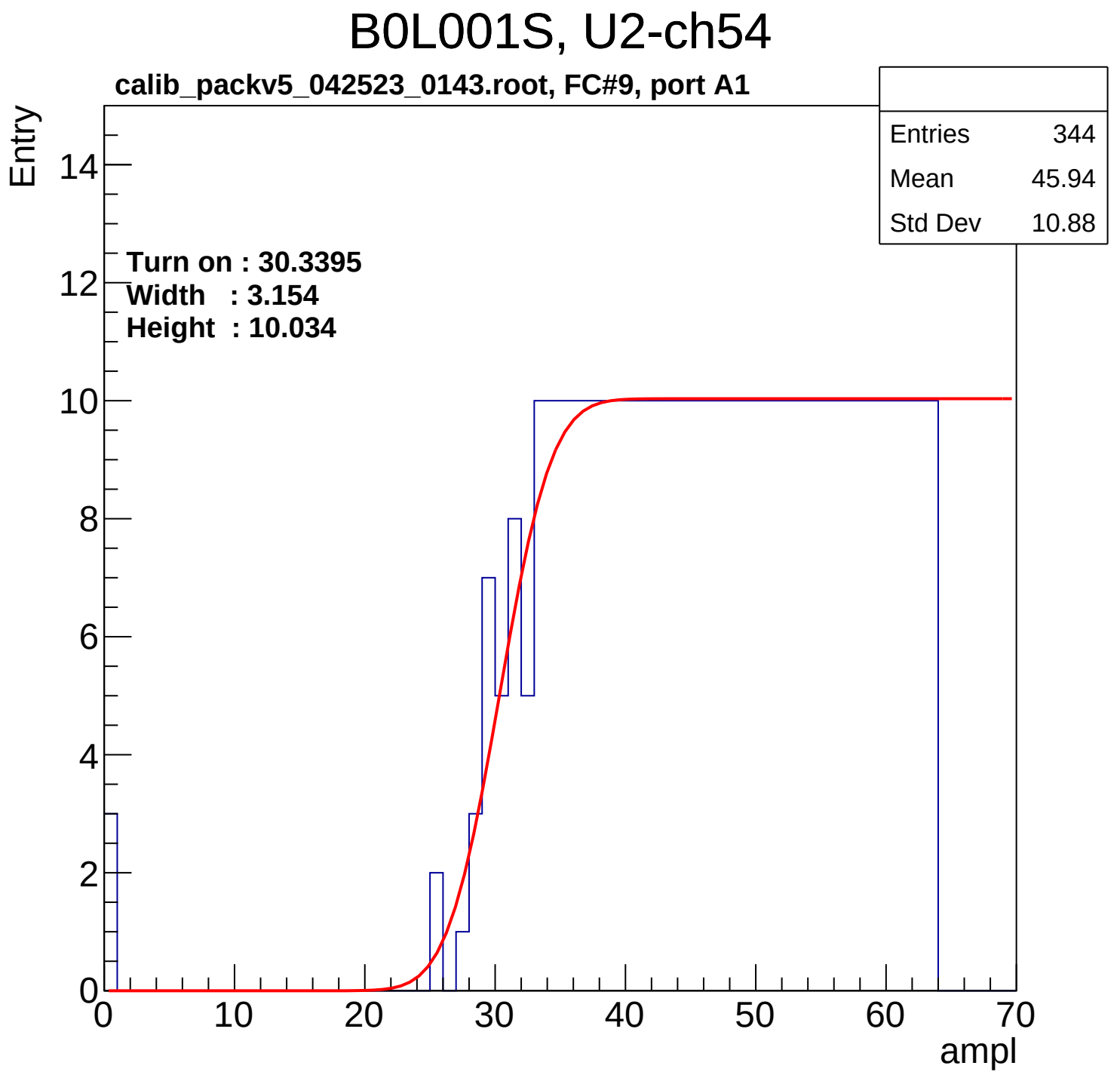
B0L001S, U2-ch54
calib_packv5_042523_0143.root, FC#9, port A1
Entries 344
Mean 45.94
Std Dev 10.88
Turn on : 30.3395
Width : 3.154
Height : 10.034
Entry
ampl
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2
4
6
8
10
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0
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20
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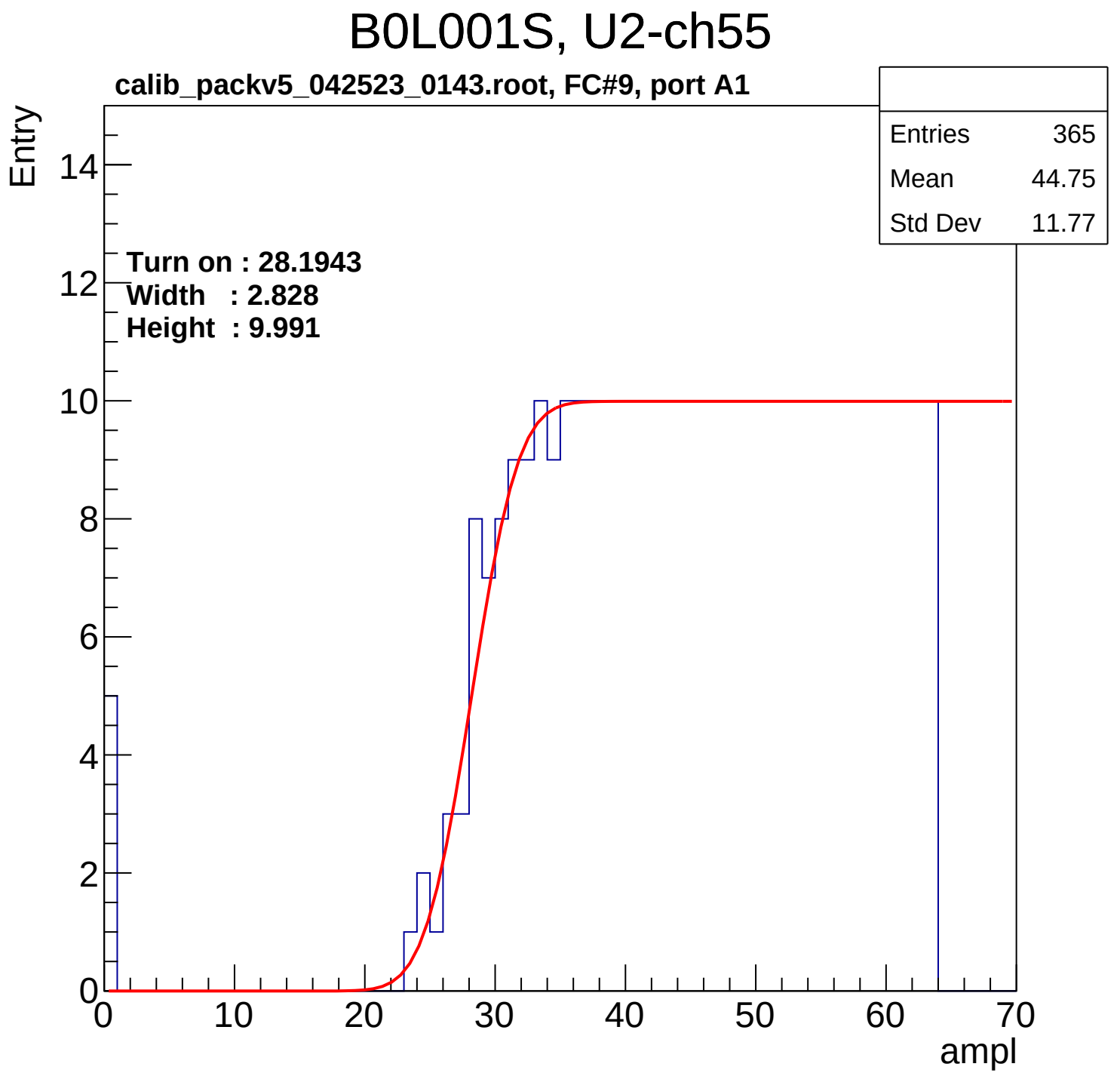
B0L001S, U2-ch55
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 44.75
Std Dev 11.77
Turn on : 28.1943
Width : 2.828
Height : 9.991
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ampl
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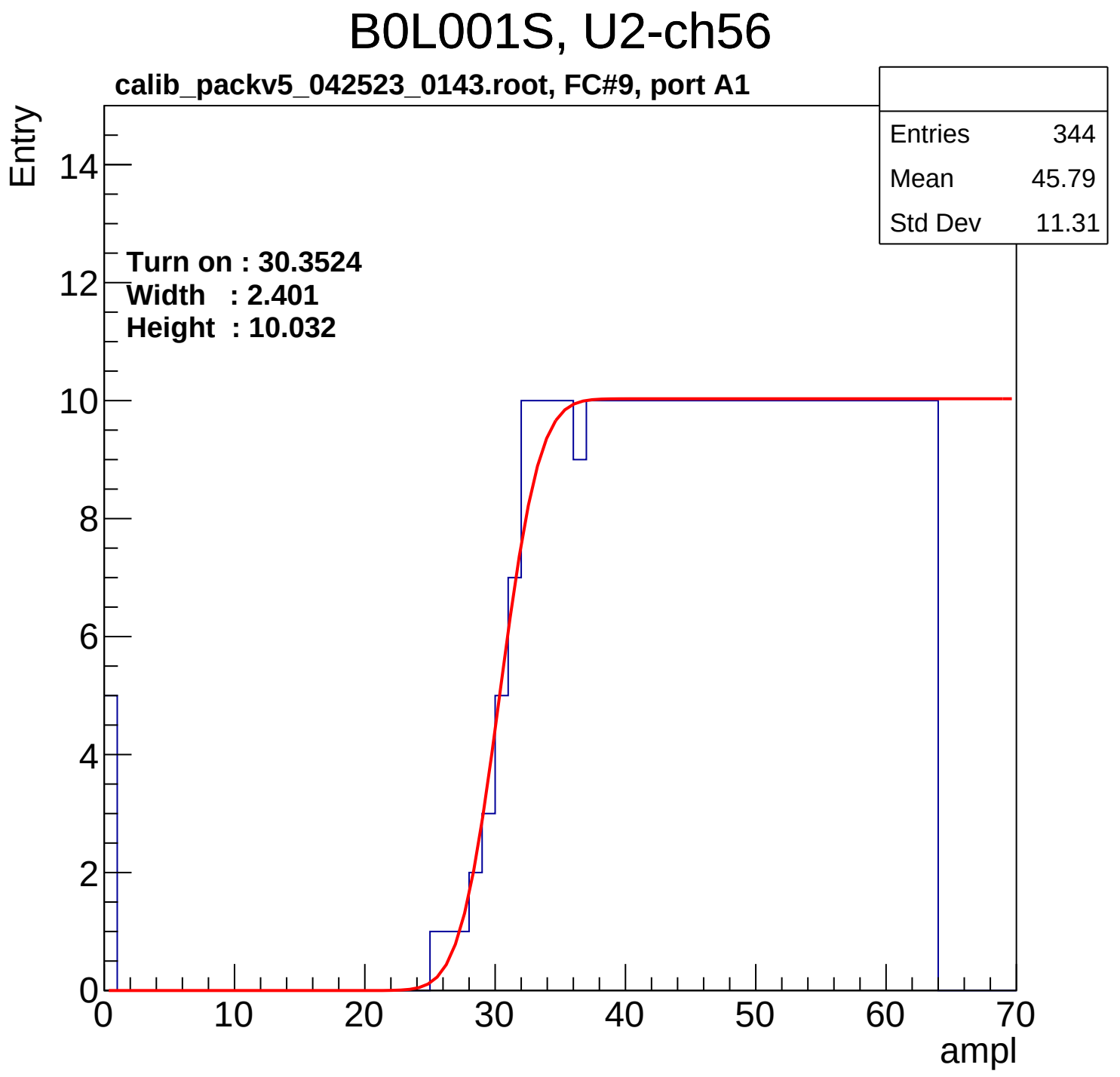
B0L001S, U2-ch56
calib_packv5_042523_0143.root, FC#9, port A1
Entries 344
Mean 45.79
Std Dev 11.31
Turn on : 30.3524
Width : 2.401
Height : 10.032
Entry
ampl
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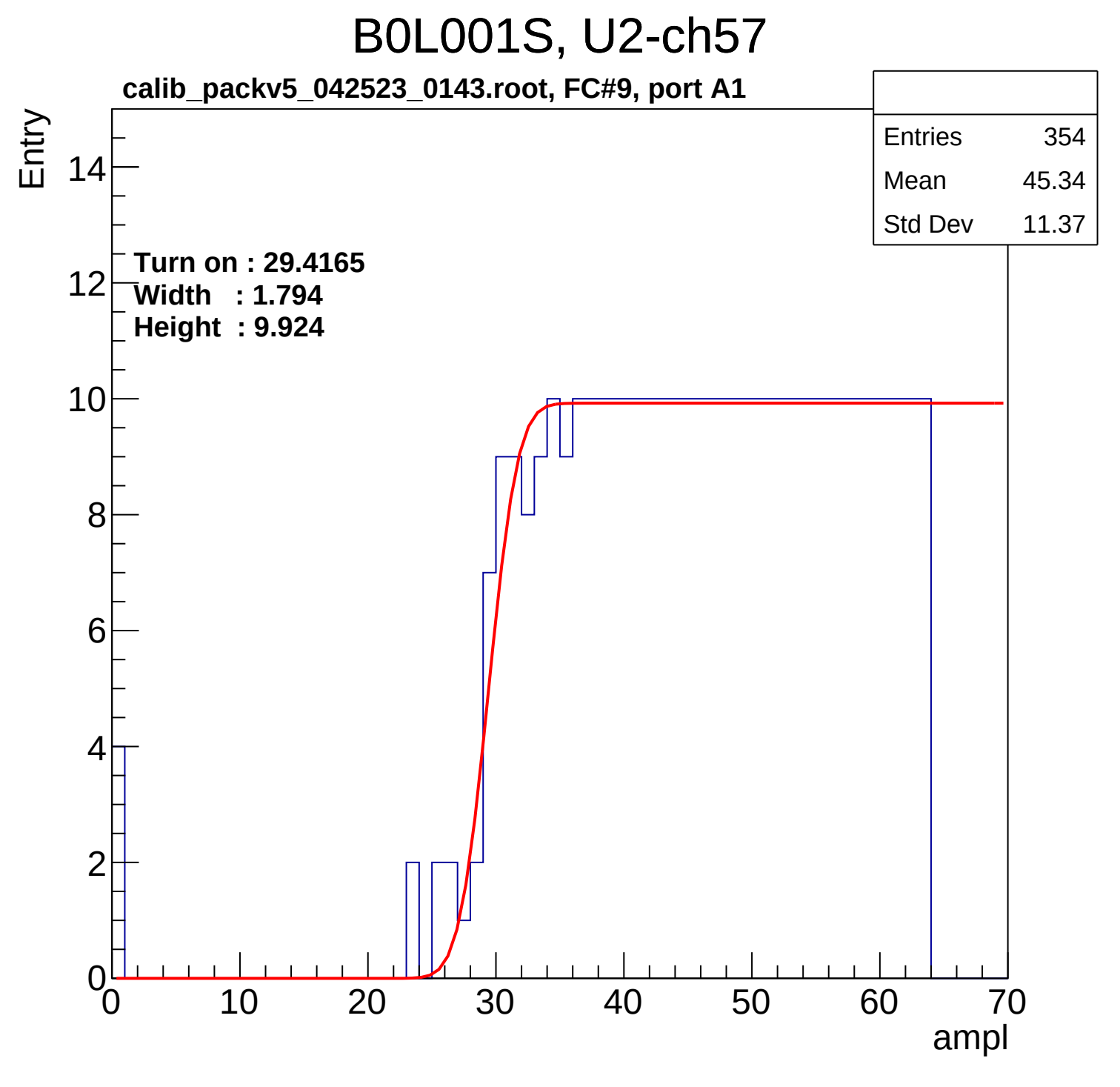
B0L001S, U2-ch57
calib_packv5_042523_0143.root, FC#9, port A1
Entries 354
Mean 45.34
Std Dev 11.37
Turn on : 29.4165
Width : 1.794
Height : 9.924
Entry
ampl
0
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4
6
8
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12
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10
20
30
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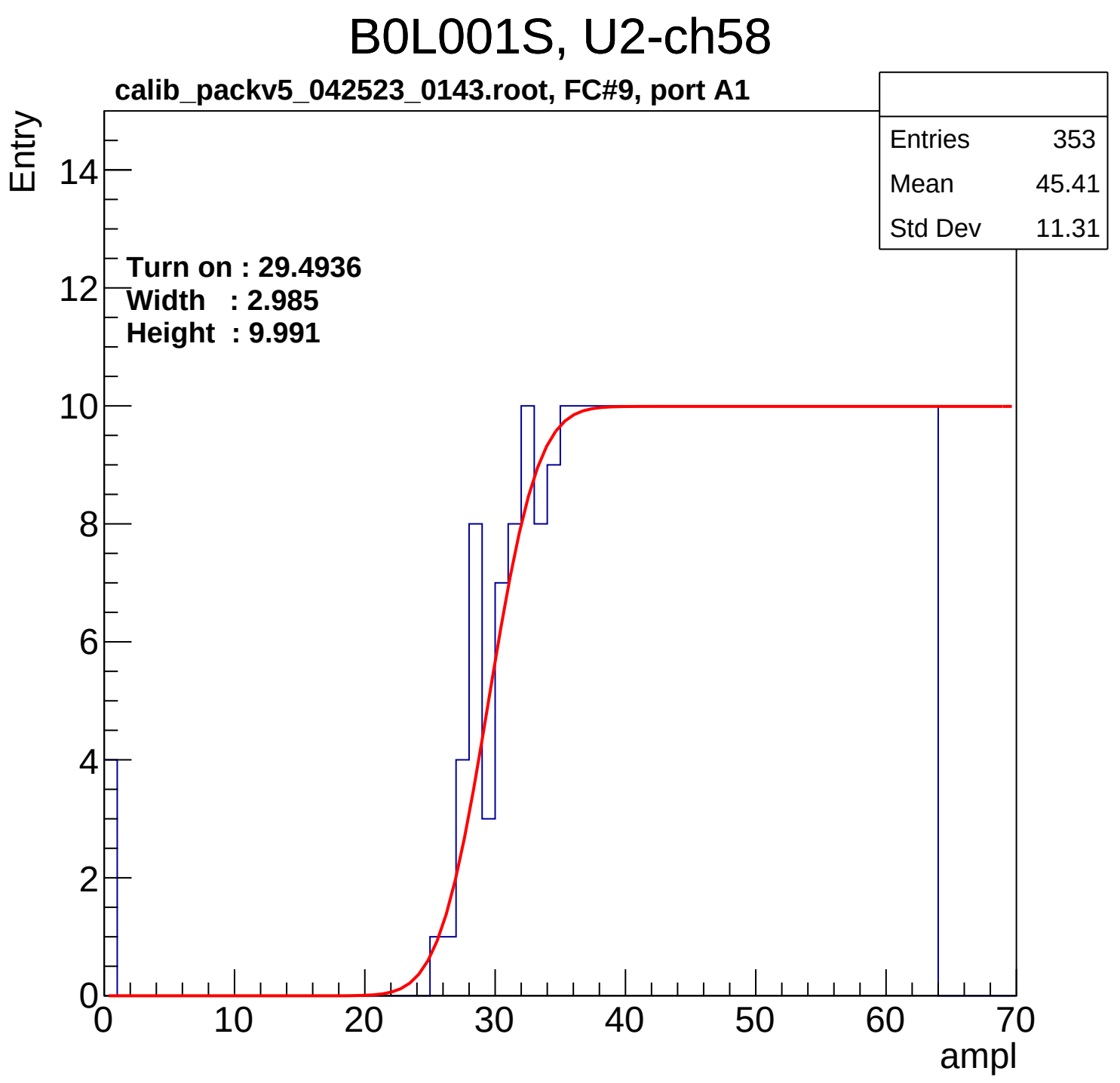
B0L001S, U2-ch58
calib_packv5_042523_0143.root, FC#9, port A1
Entries 353
Mean 45.41
Std Dev 11.31
Turn on : 29.4936
Width : 2.985
Height : 9.991
Entry
ampl
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6
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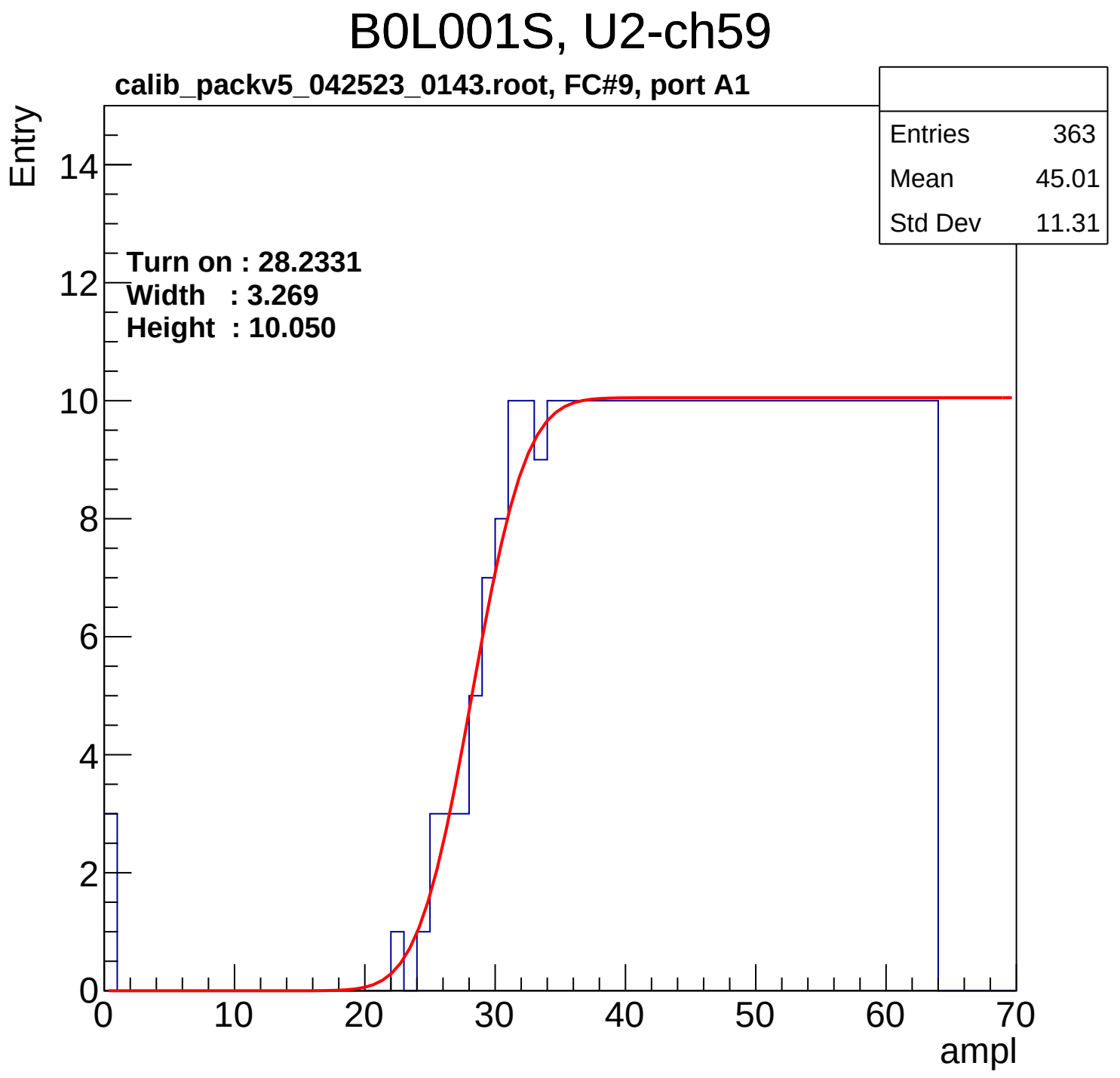
B0L001S, U2-ch59
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 45.01
Std Dev 11.31
Turn on : 28.2331
Width : 3.269
Height : 10.050
Entry
ampl
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2
4
6
8
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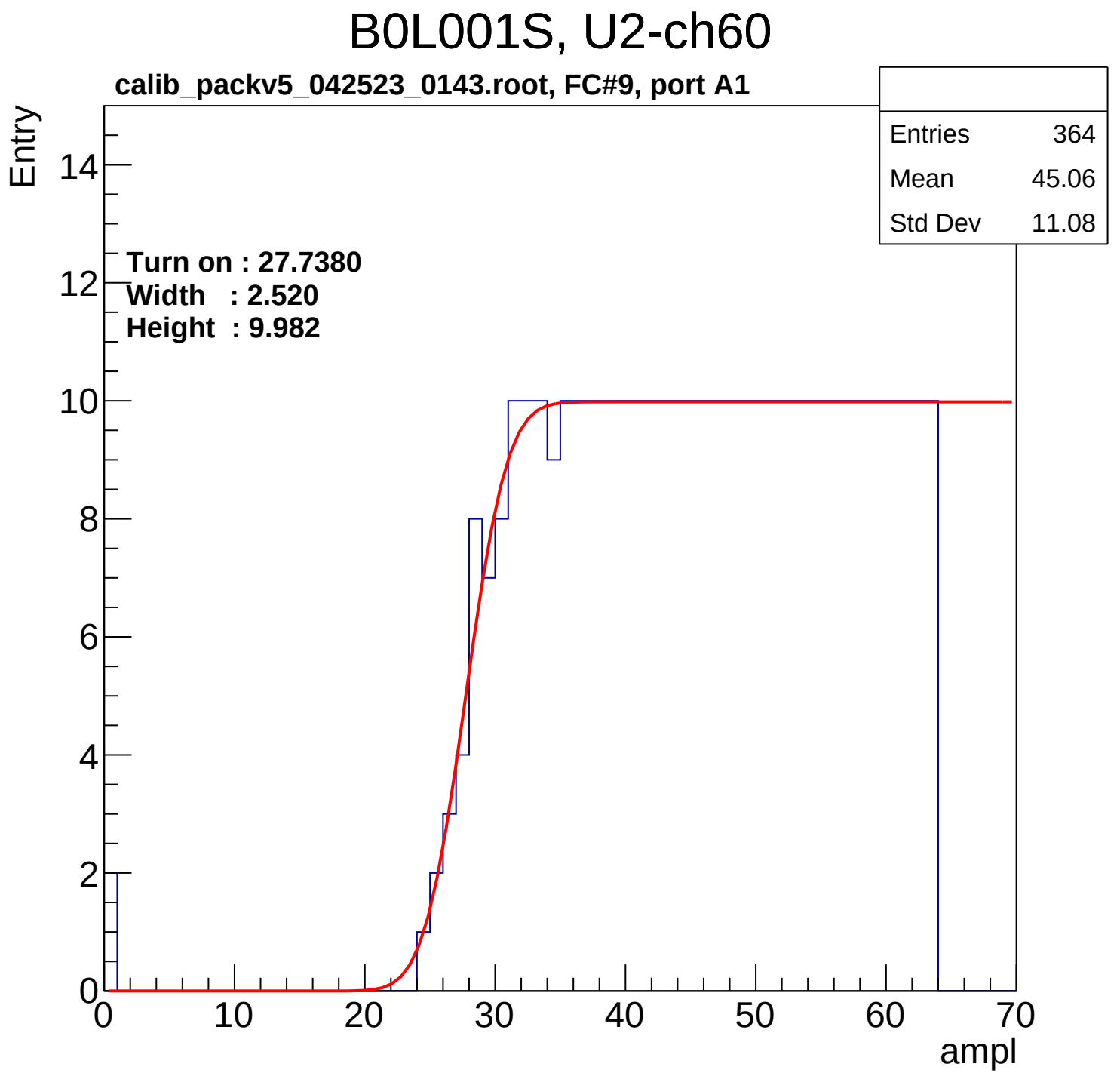
B0L001S, U2-ch60
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 45.06
Std Dev 11.08
Turn on : 27.7380
Width : 2.520
Height : 9.982
Entry
ampl
0
2
4
6
8
10
12
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0
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40
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60
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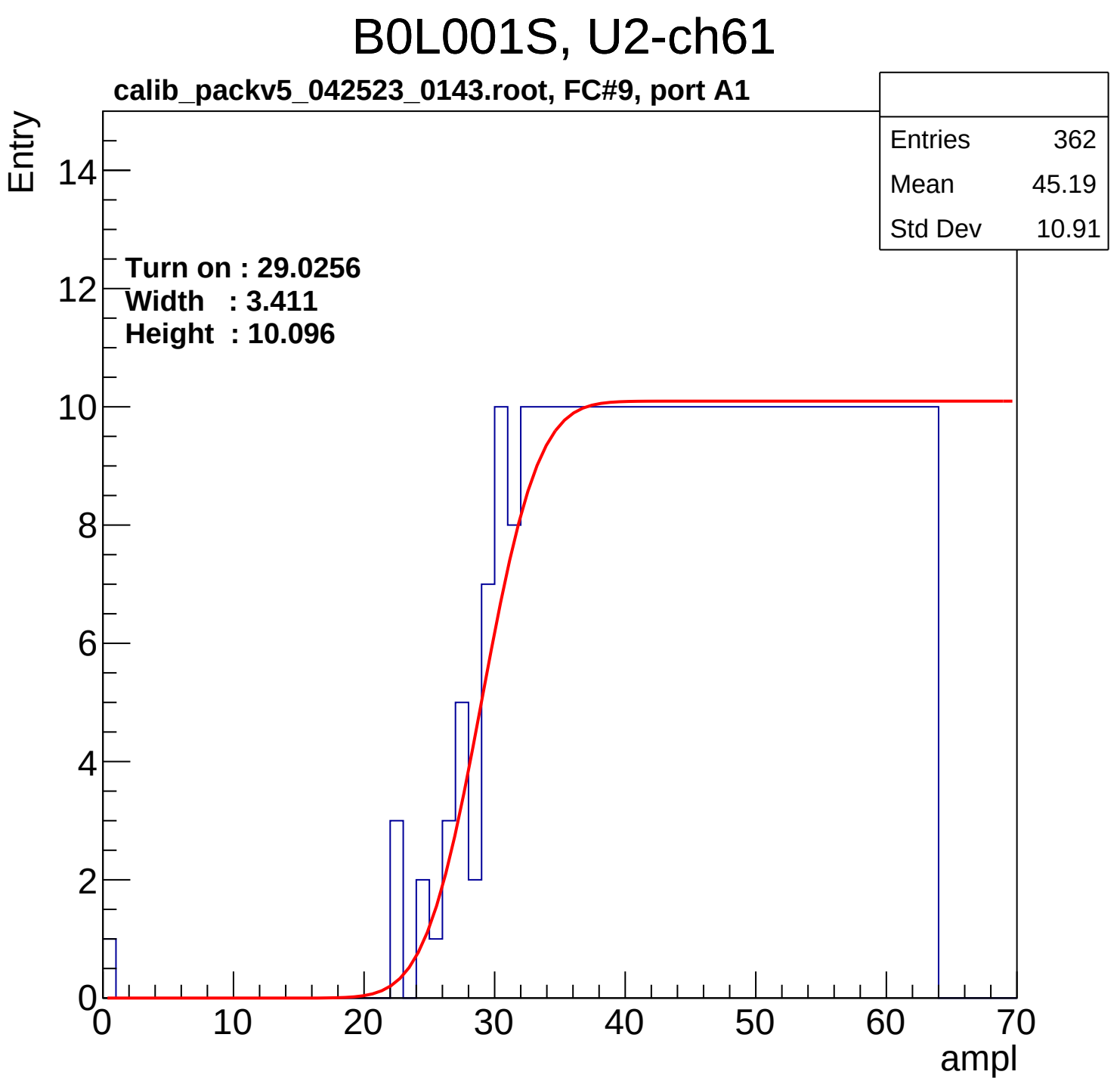
B0L001S, U2-ch61
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 45.19
Std Dev 10.91
Turn on : 29.0256
Width : 3.411
Height : 10.096
Entry
ampl
0
2
4
6
8
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12
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0
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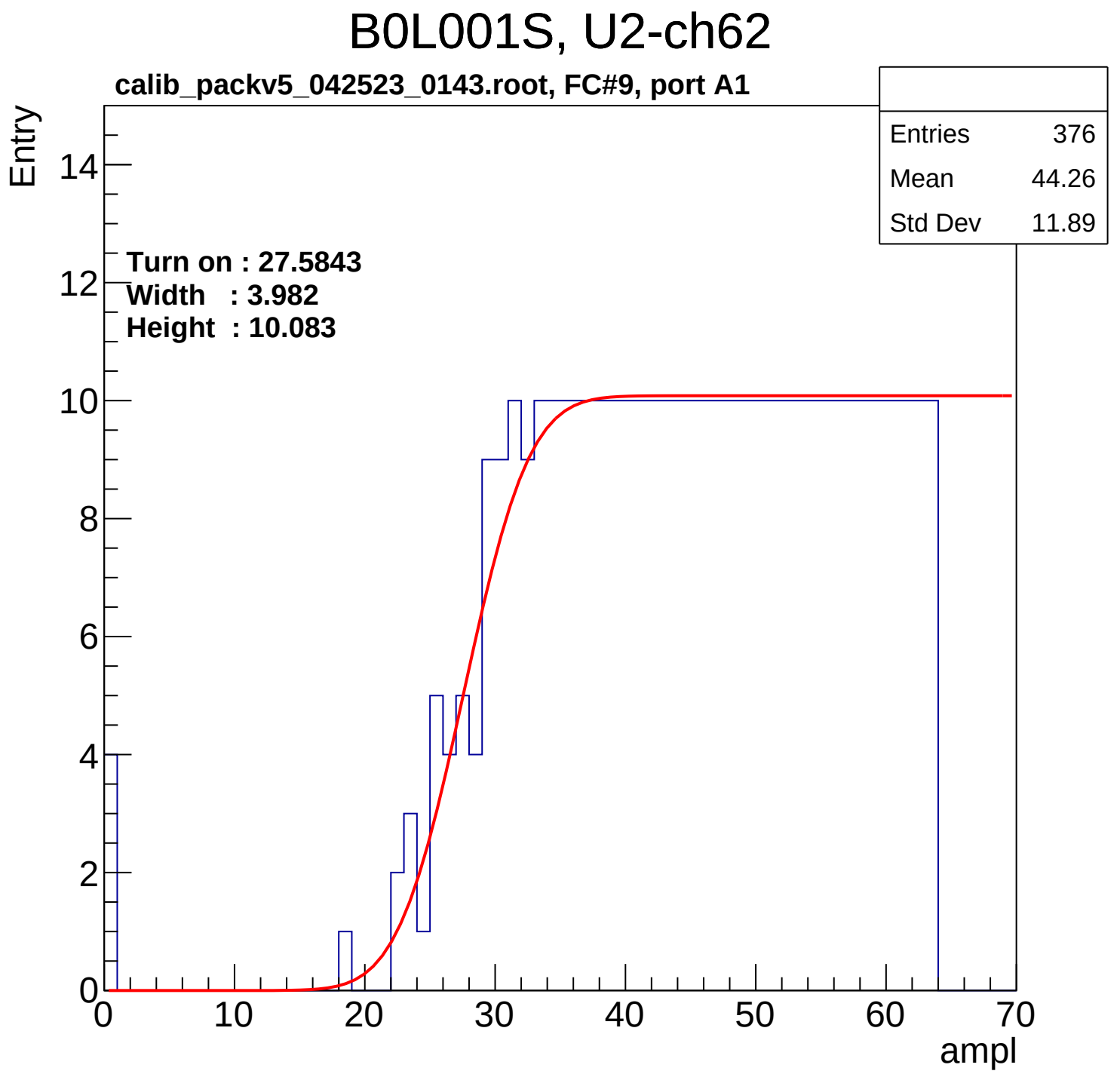
B0L001S, U2-ch62
calib_packv5_042523_0143.root, FC#9, port A1
Entries 376
Mean 44.26
Std Dev 11.89
Turn on : 27.5843
Width : 3.982
Height : 10.083
Entry
ampl
0
2
4
6
8
10
12
14
0
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60
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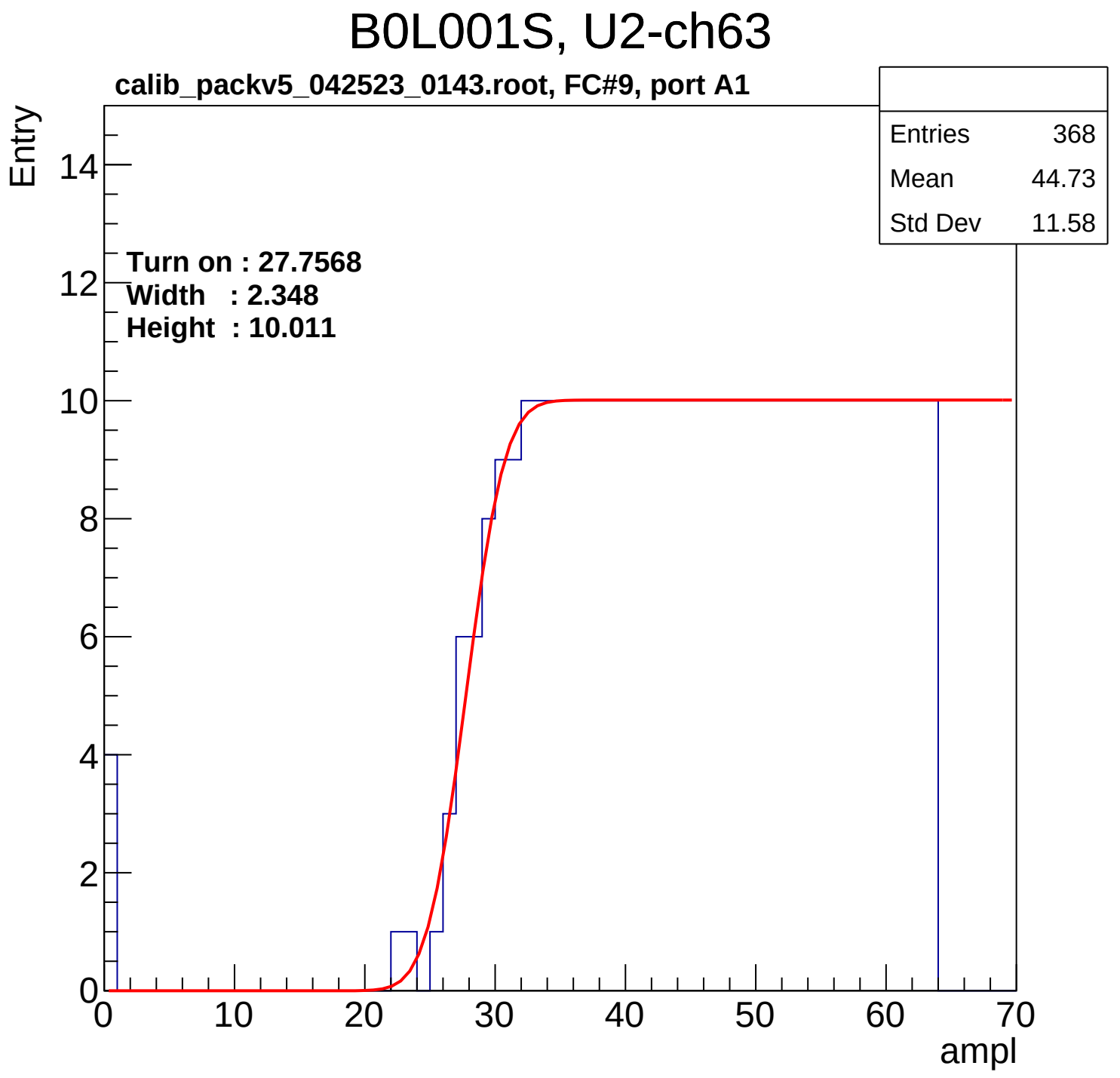
B0L001S, U2-ch63
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.73
Std Dev 11.58
Turn on : 27.7568
Width : 2.348
Height : 10.011
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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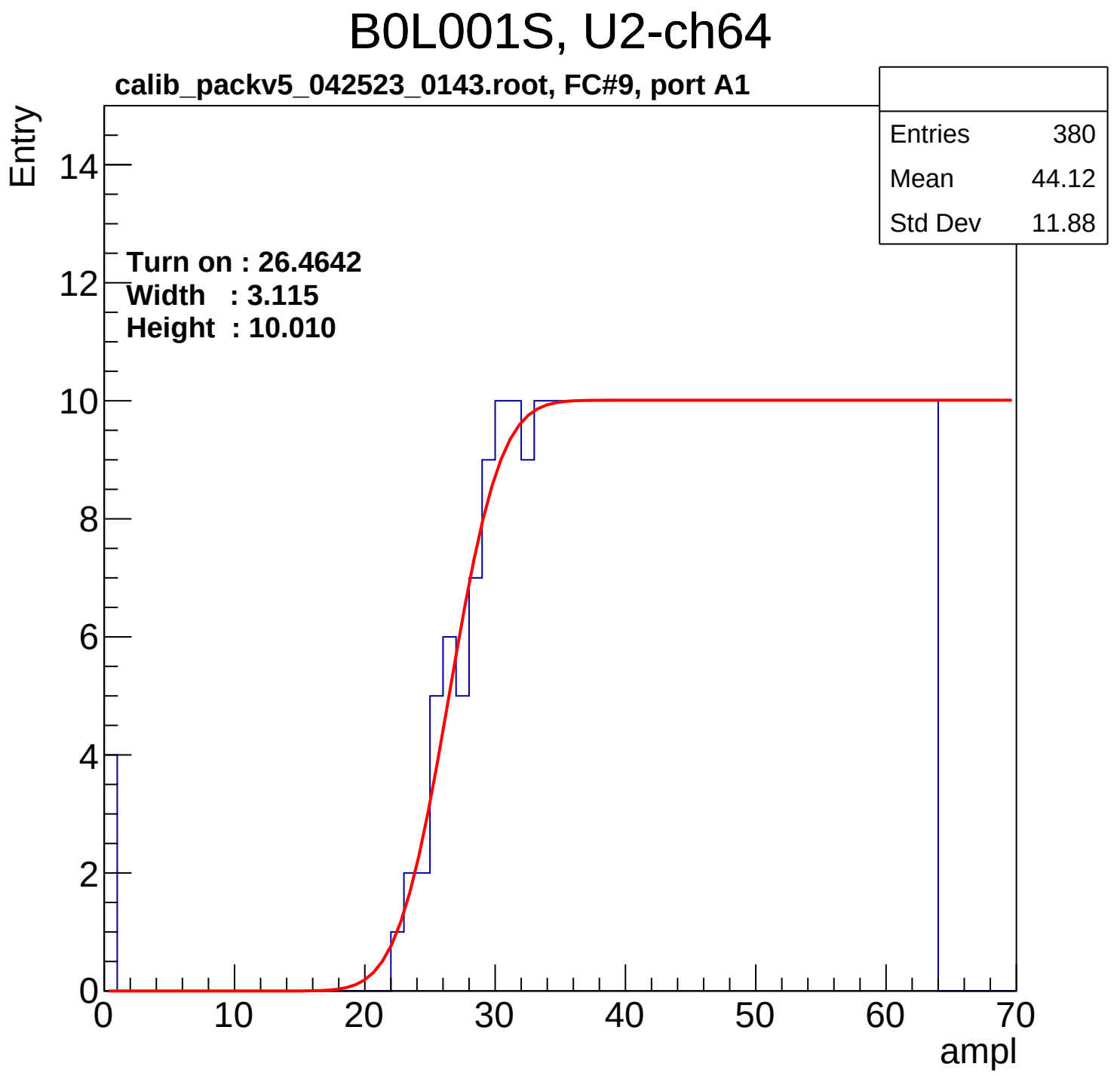
B0L001S, U2-ch64
calib_packv5_042523_0143.root, FC#9, port A1
Entries 380
Mean 44.12
Std Dev 11.88
Turn on : 26.4642
Width : 3.115
Height : 10.010
Entry
ampl
0
2
4
6
8
10
12
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0
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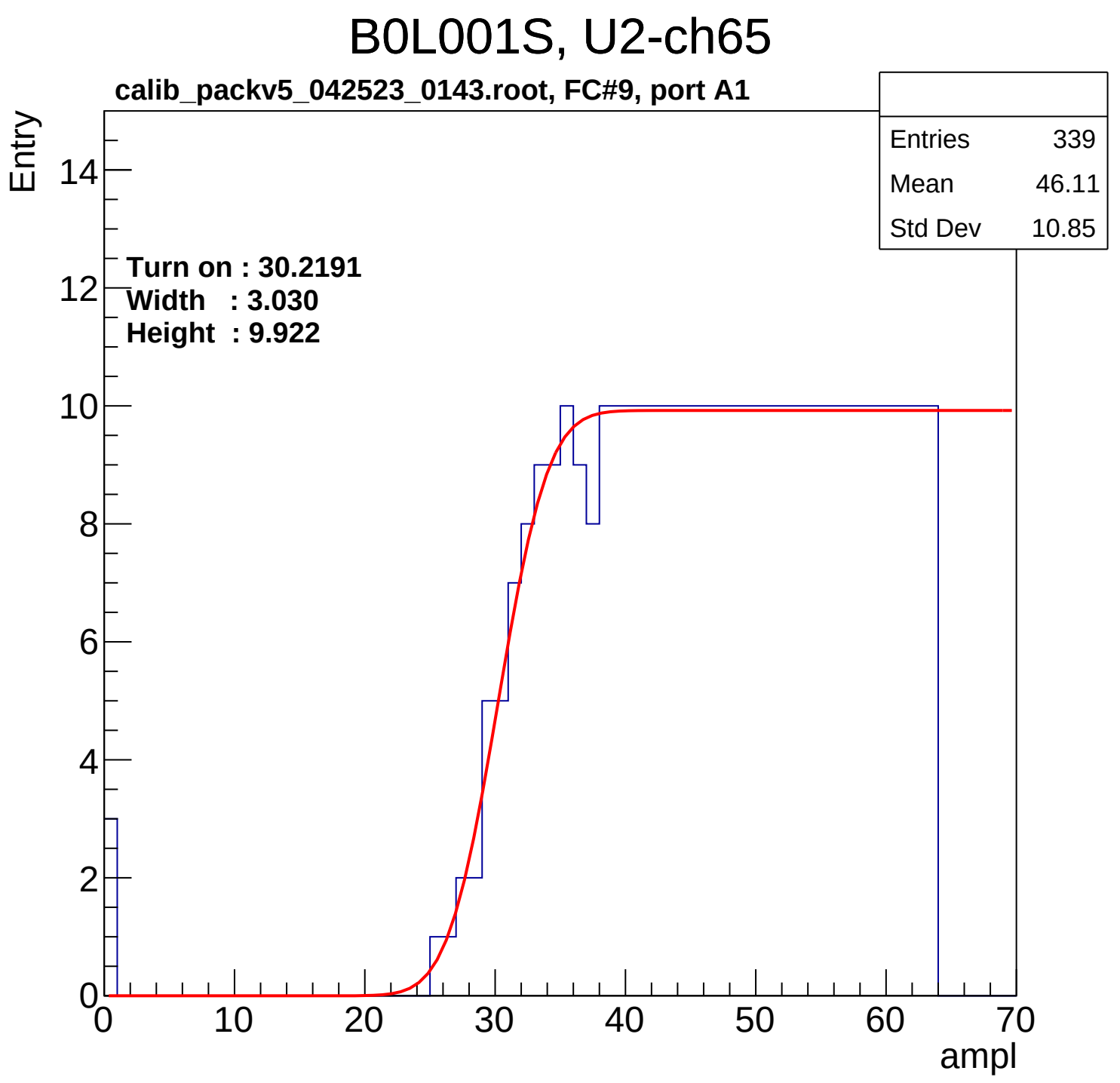
B0L001S, U2-ch65
calib_packv5_042523_0143.root, FC#9, port A1
Entries 339
Mean 46.11
Std Dev 10.85
Turn on : 30.2191
Width : 3.030
Height : 9.922
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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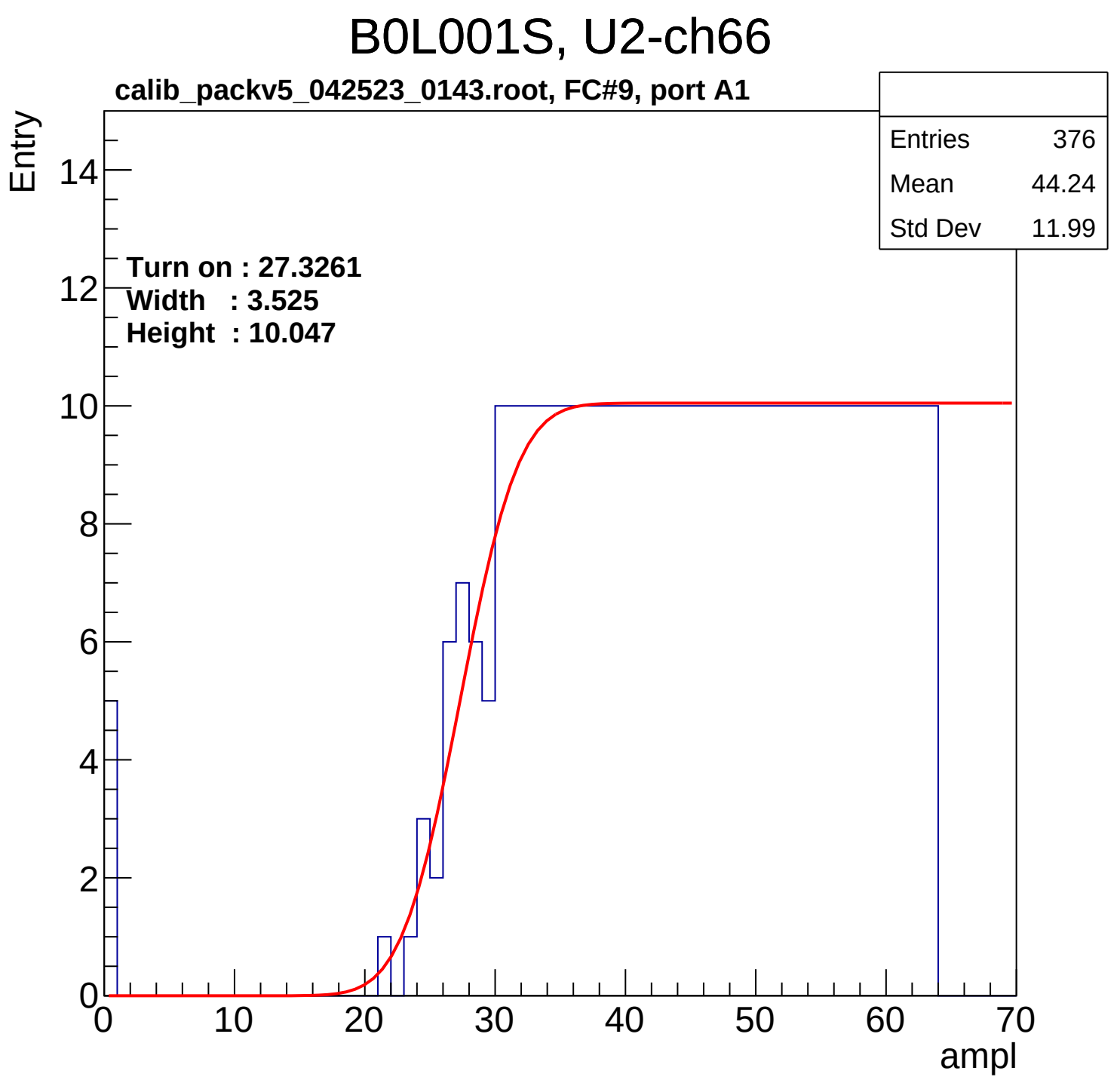
B0L001S, U2-ch66
calib_packv5_042523_0143.root, FC#9, port A1
Entries 376
Mean 44.24
Std Dev 11.99
Turn on : 27.3261
Width : 3.525
Height : 10.047
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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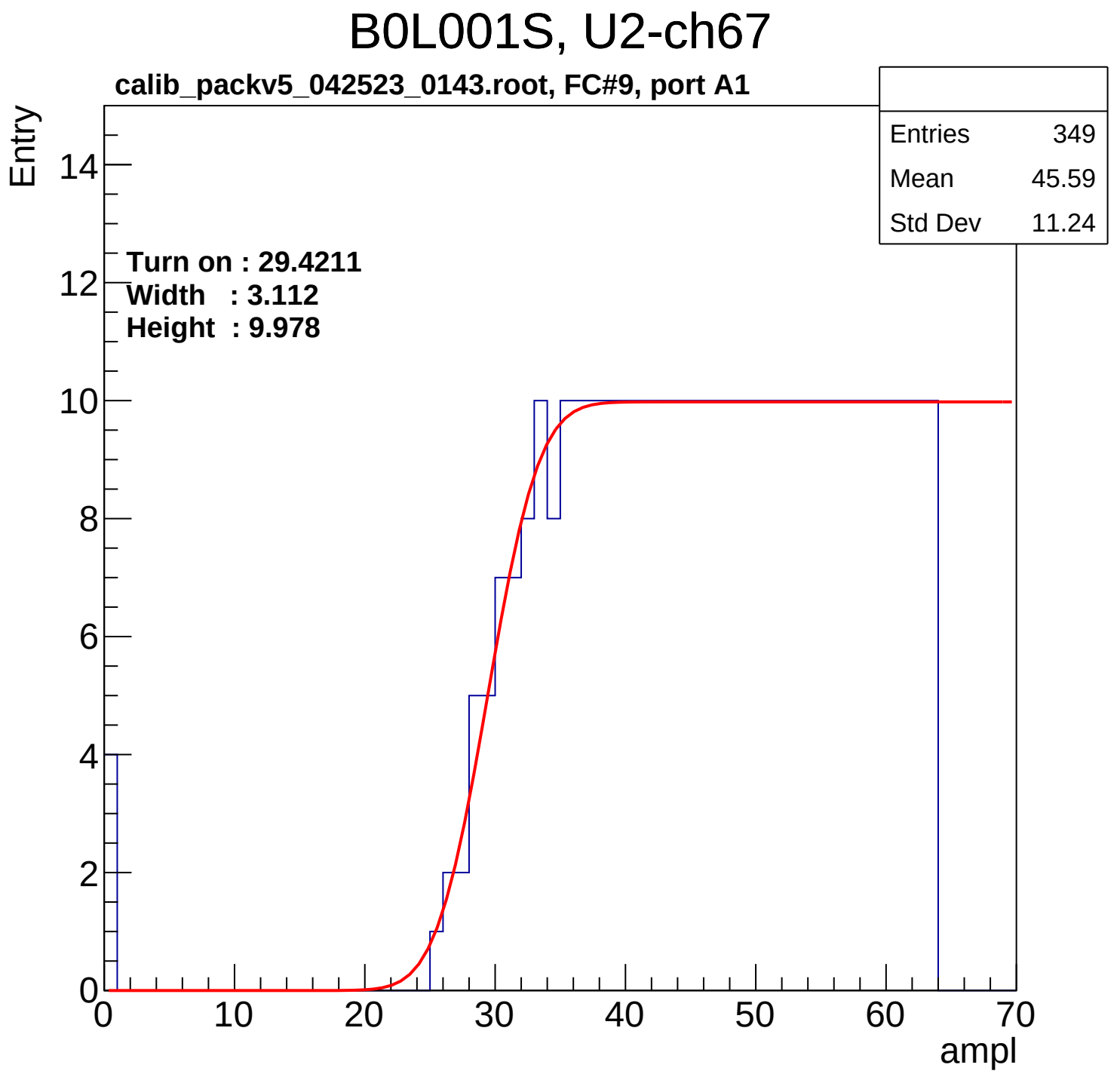
B0L001S, U2-ch67
calib_packv5_042523_0143.root, FC#9, port A1
Entries 349
Mean 45.59
Std Dev 11.24
Turn on : 29.4211
Width : 3.112
Height : 9.978
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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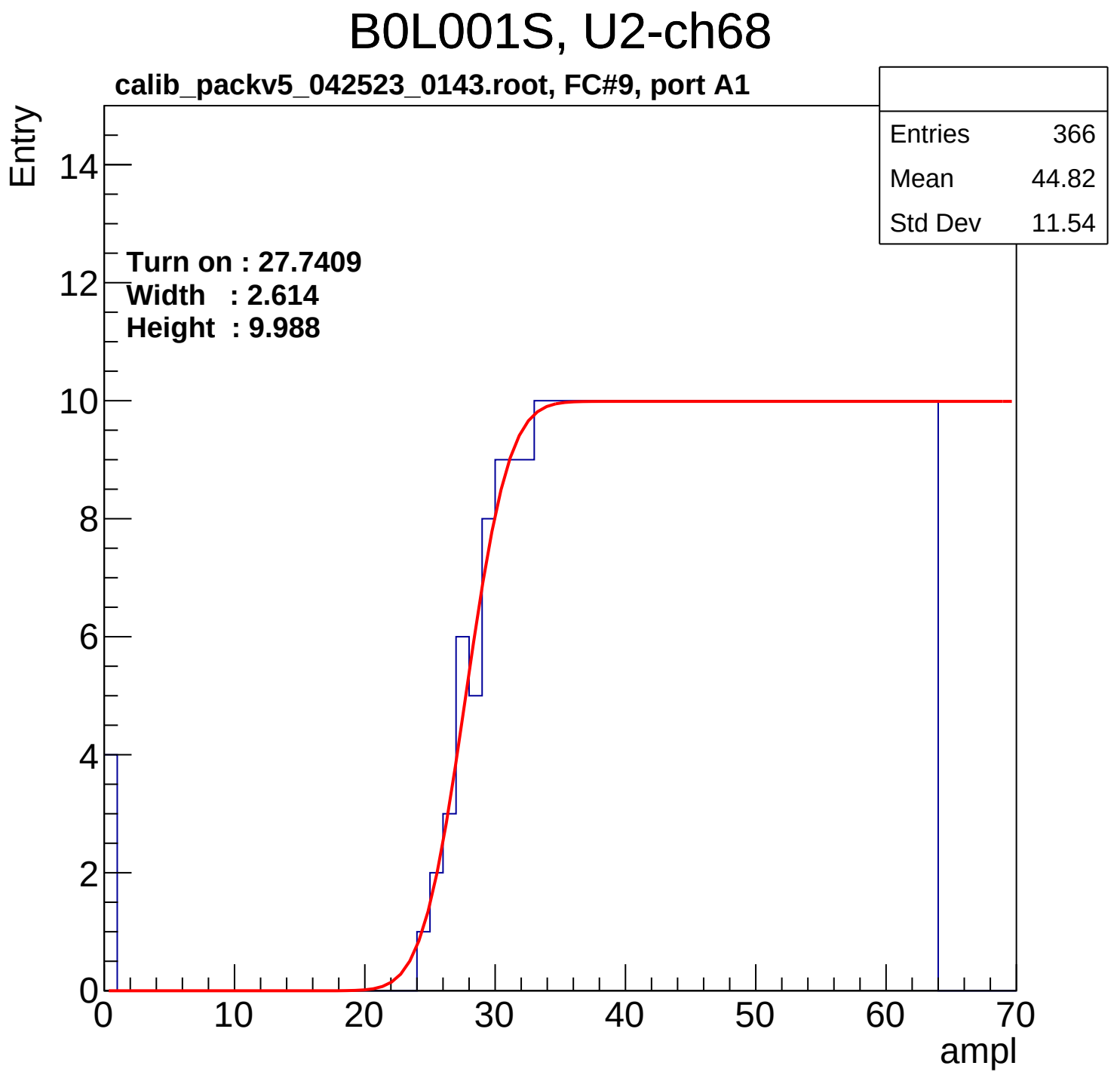
B0L001S, U2-ch68
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.82
Std Dev 11.54
Turn on : 27.7409
Width : 2.614
Height : 9.988
Entry
ampl
0
2
4
6
8
10
12
14
0
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60
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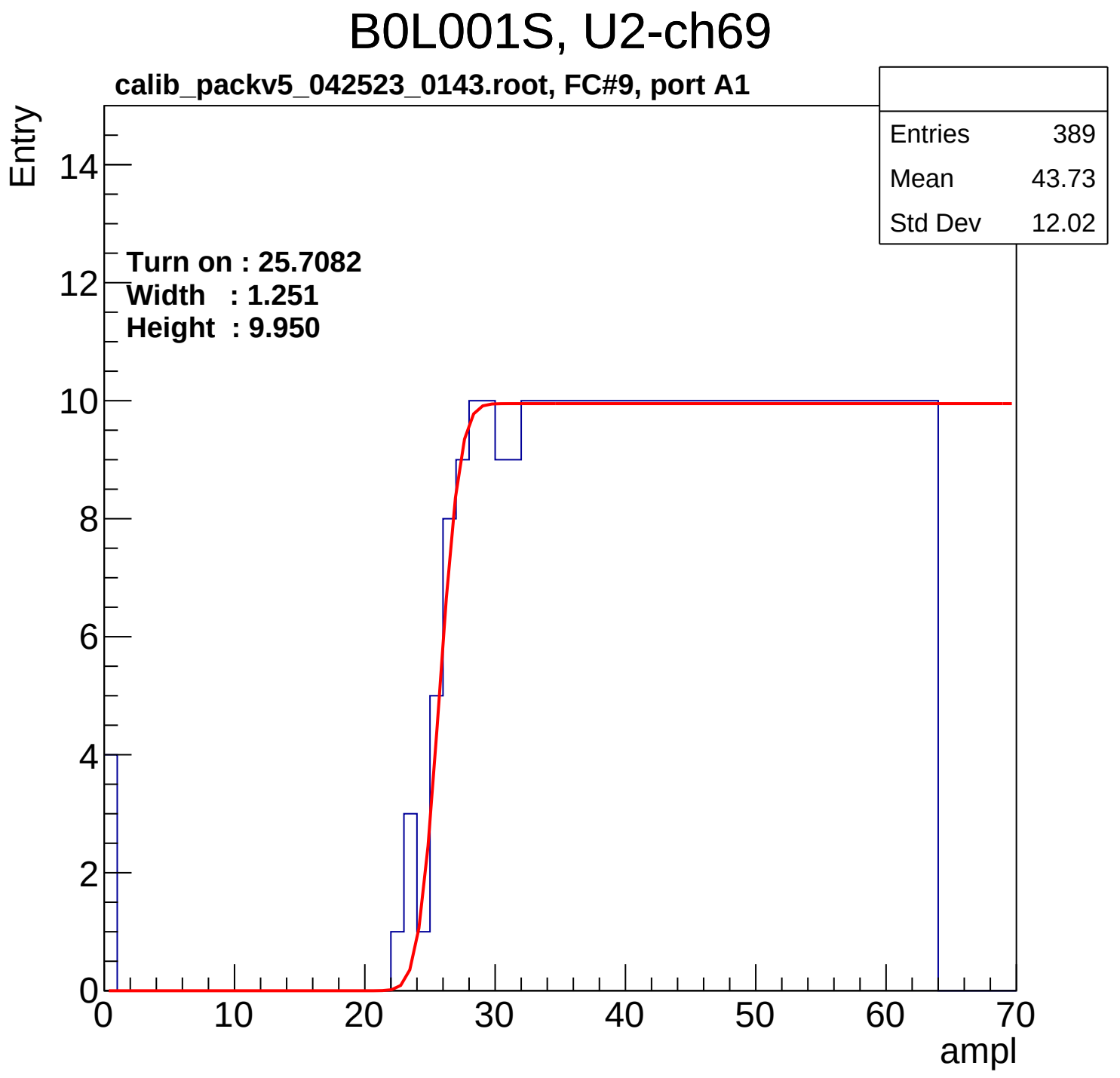
B0L001S, U2-ch69
calib_packv5_042523_0143.root, FC#9, port A1
Entries 389
Mean 43.73
Std Dev 12.02
Turn on : 25.7082
Width : 1.251
Height : 9.950
Entry
ampl
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4
6
8
10
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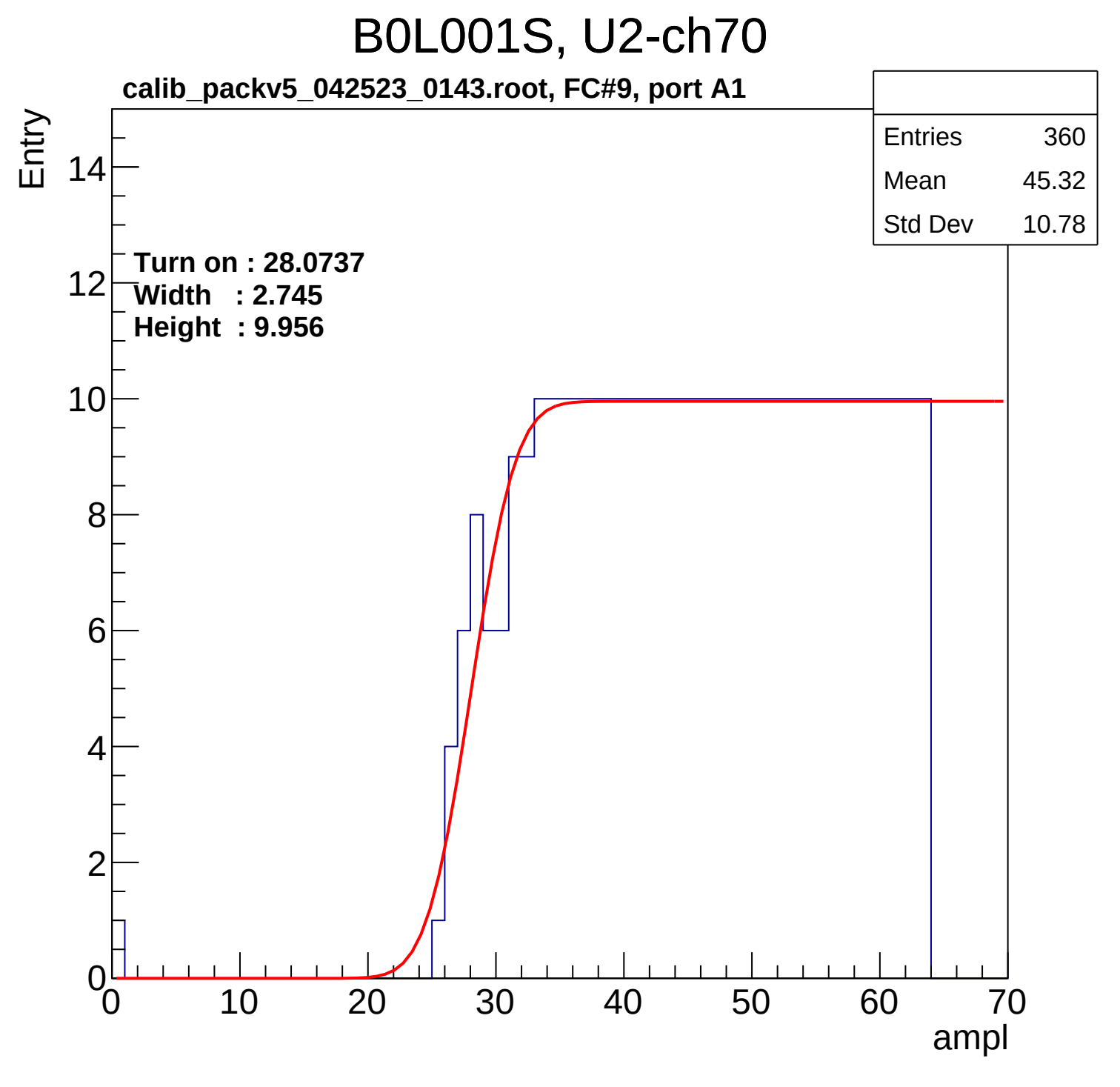
B0L001S, U2-ch70
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 45.32
Std Dev 10.78
Turn on : 28.0737
Width : 2.745
Height : 9.956
Entry
ampl
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2
4
6
8
10
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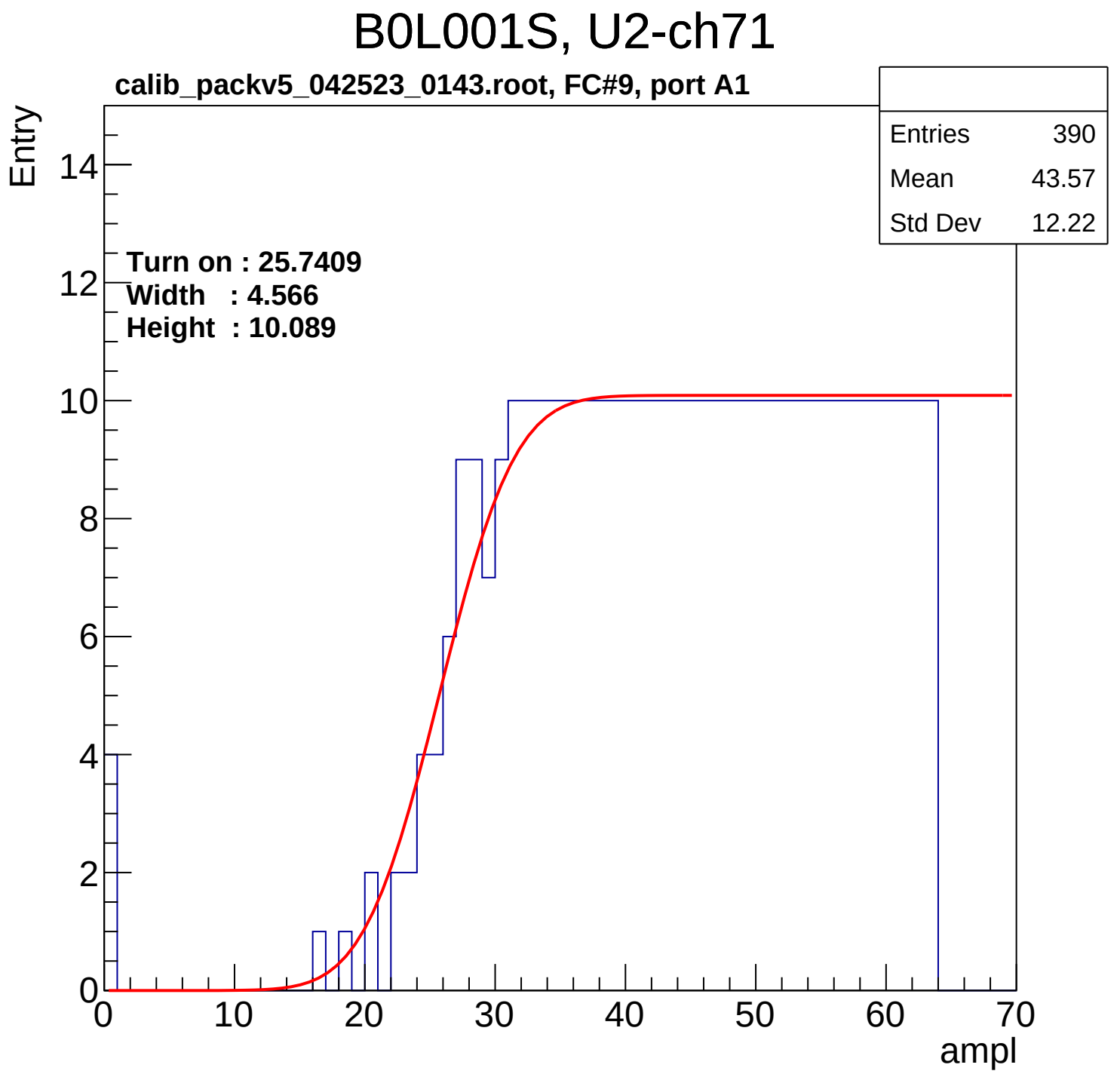
B0L001S, U2-ch71
calib_packv5_042523_0143.root, FC#9, port A1
Entries 390
Mean 43.57
Std Dev 12.22
Turn on : 25.7409
Width : 4.566
Height : 10.089
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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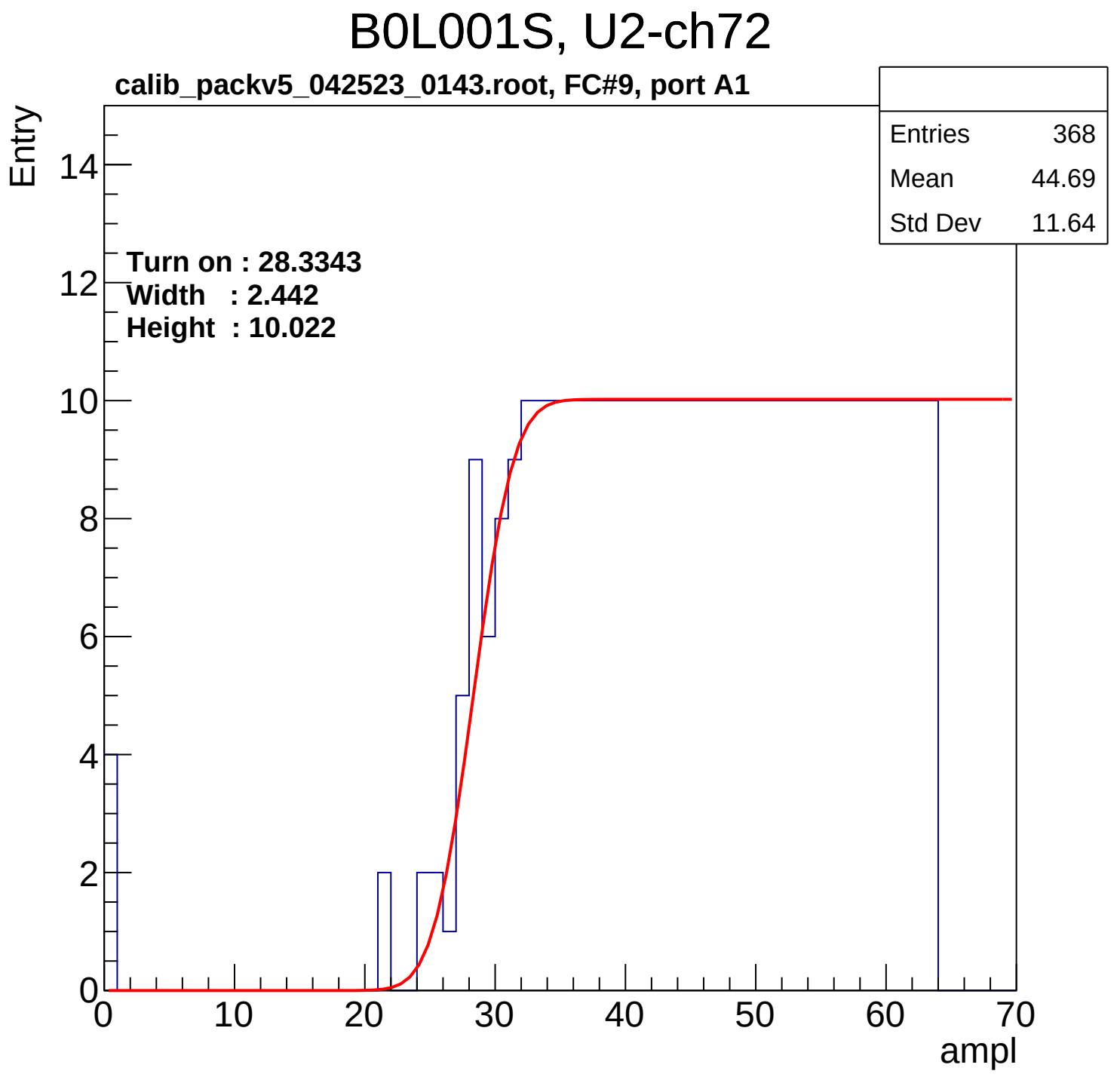
B0L001S, U2-ch72
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.69
Std Dev 11.64
Turn on : 28.3343
Width : 2.442
Height : 10.022
Entry
ampl
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6
8
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0
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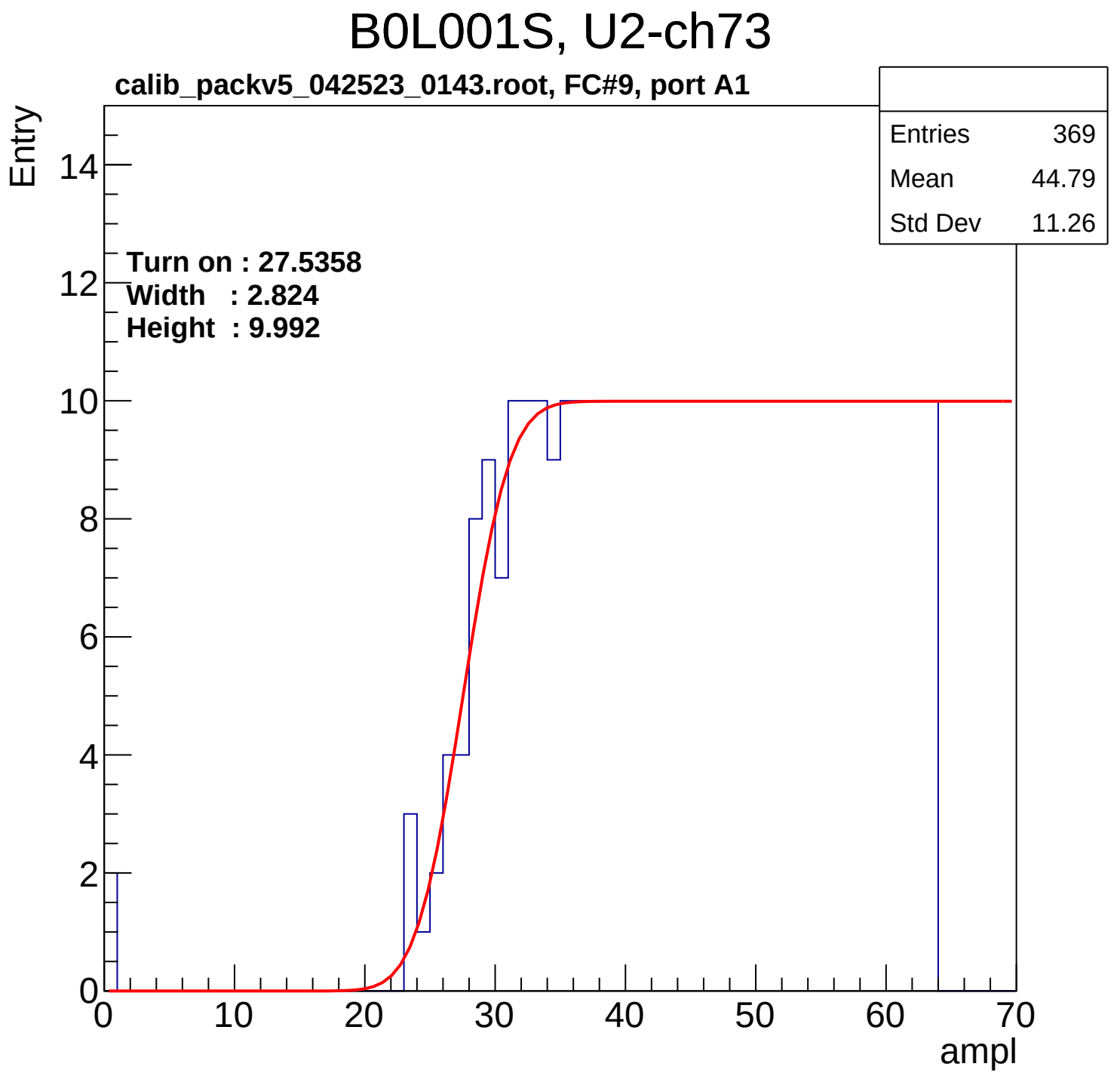
B0L001S, U2-ch73
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.79
Std Dev 11.26
Turn on : 27.5358
Width : 2.824
Height : 9.992
Entry
ampl
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4
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8
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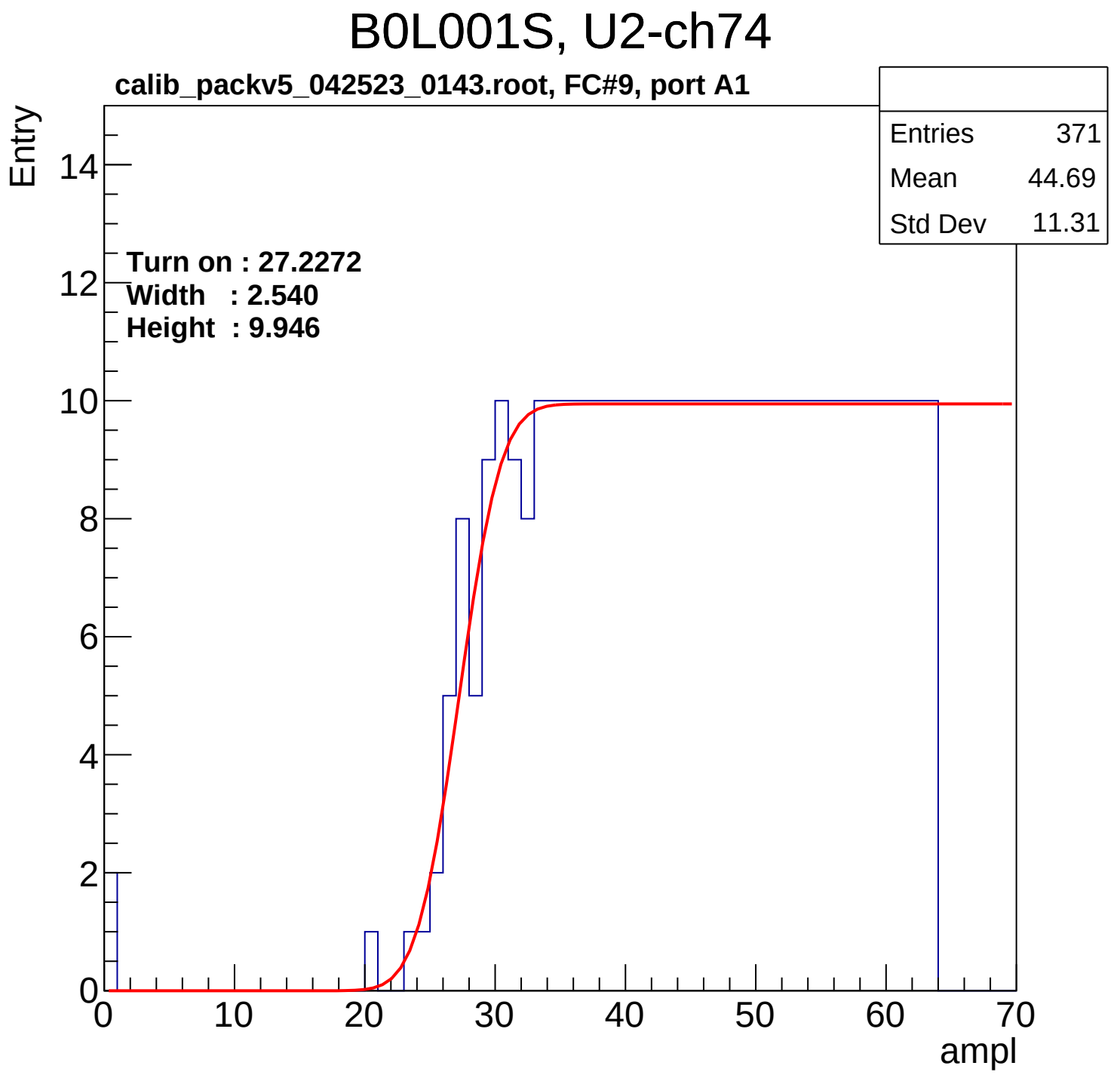
B0L001S, U2-ch74
calib_packv5_042523_0143.root, FC#9, port A1
Entries 371
Mean 44.69
Std Dev 11.31
Turn on : 27.2272
Width : 2.540
Height : 9.946
Entry
ampl
0
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4
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8
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0
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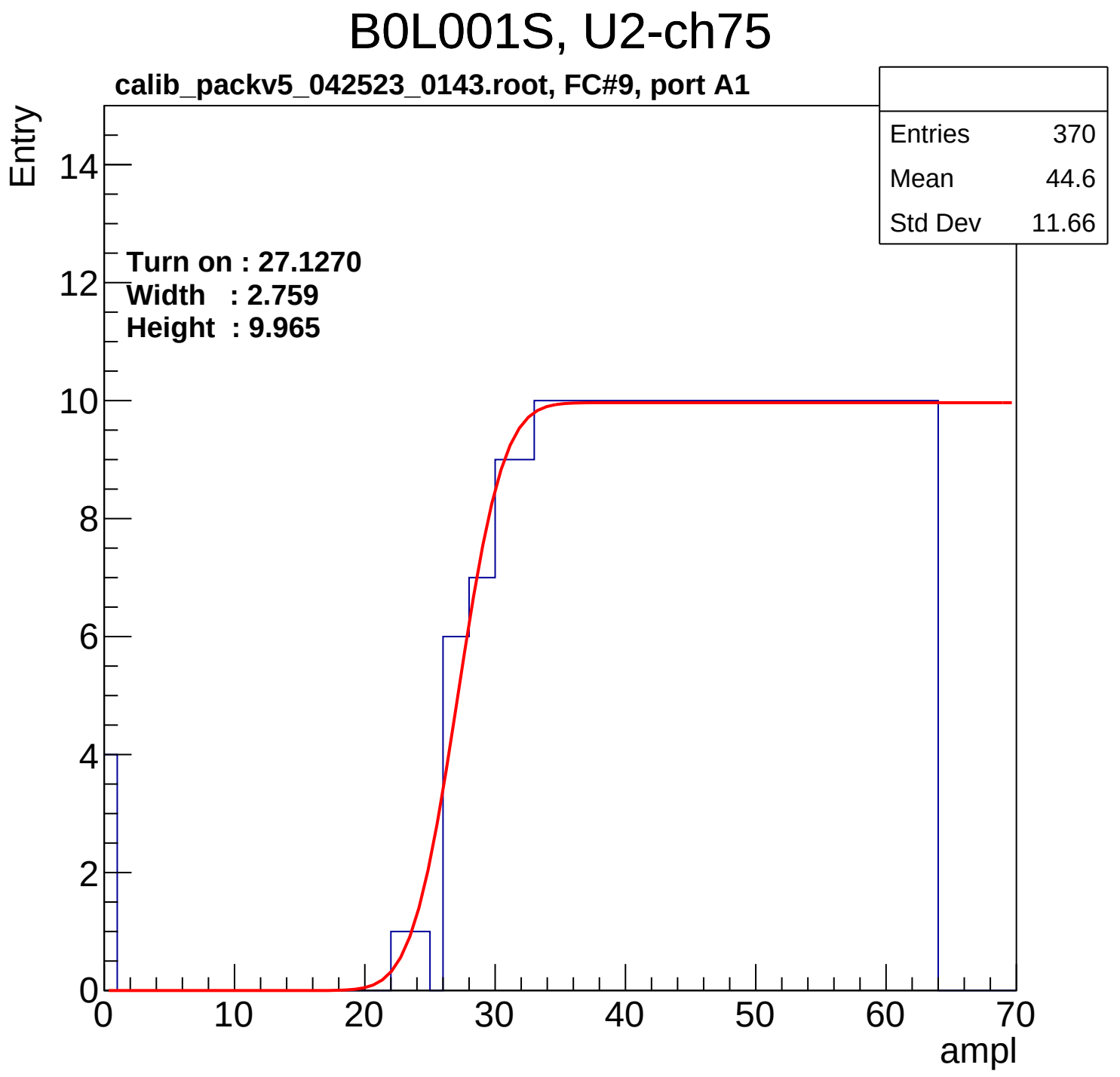
B0L001S, U2-ch75
calib_packv5_042523_0143.root, FC#9, port A1
Entries 370
Mean 44.6
Std Dev 11.66
Turn on : 27.1270
Width : 2.759
Height : 9.965
Entry
ampl
0
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6
8
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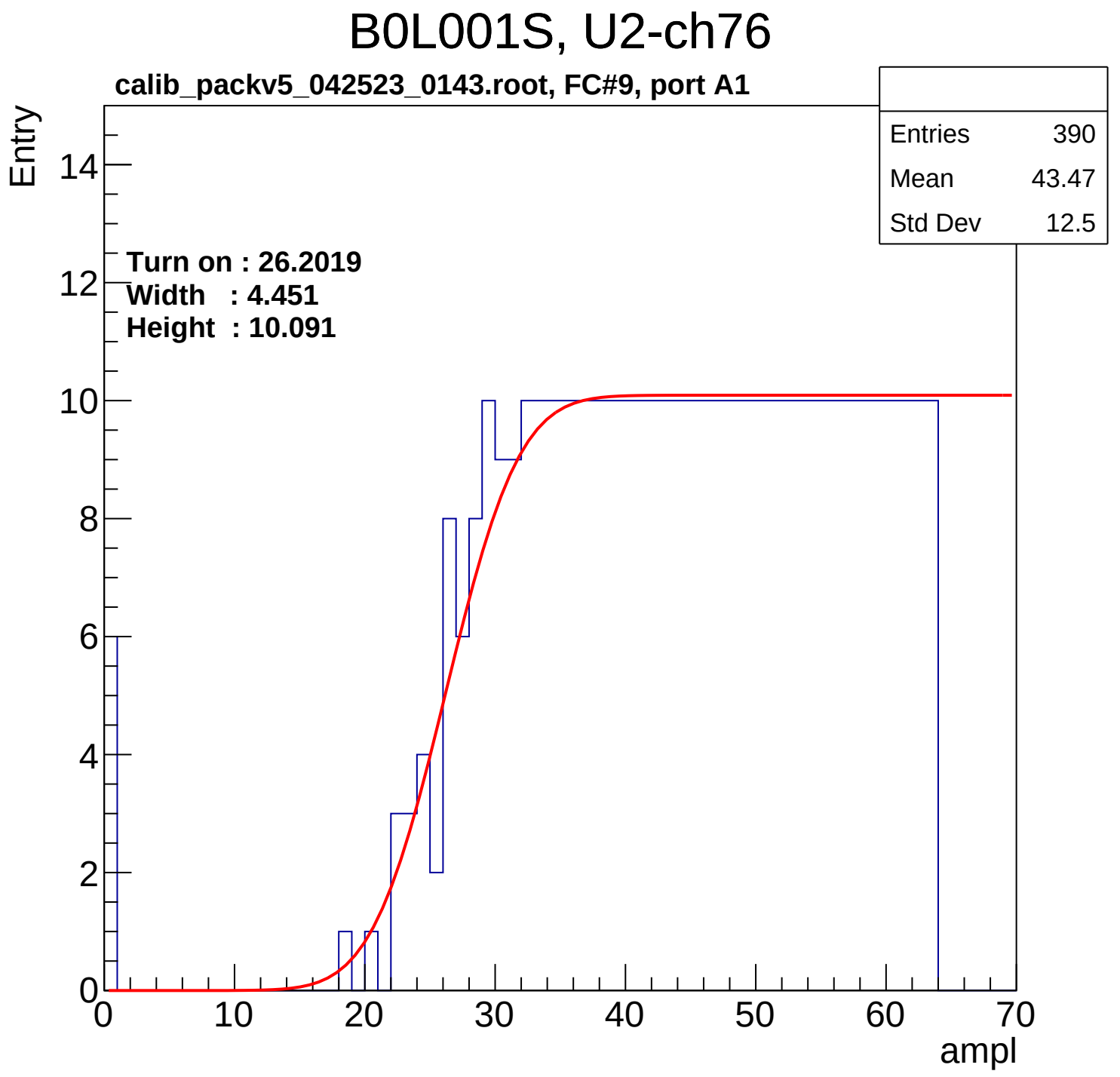
B0L001S, U2-ch76
calib_packv5_042523_0143.root, FC#9, port A1
Entries 390
Mean 43.47
Std Dev 12.5
Turn on : 26.2019
Width : 4.451
Height : 10.091
Entry
ampl
0
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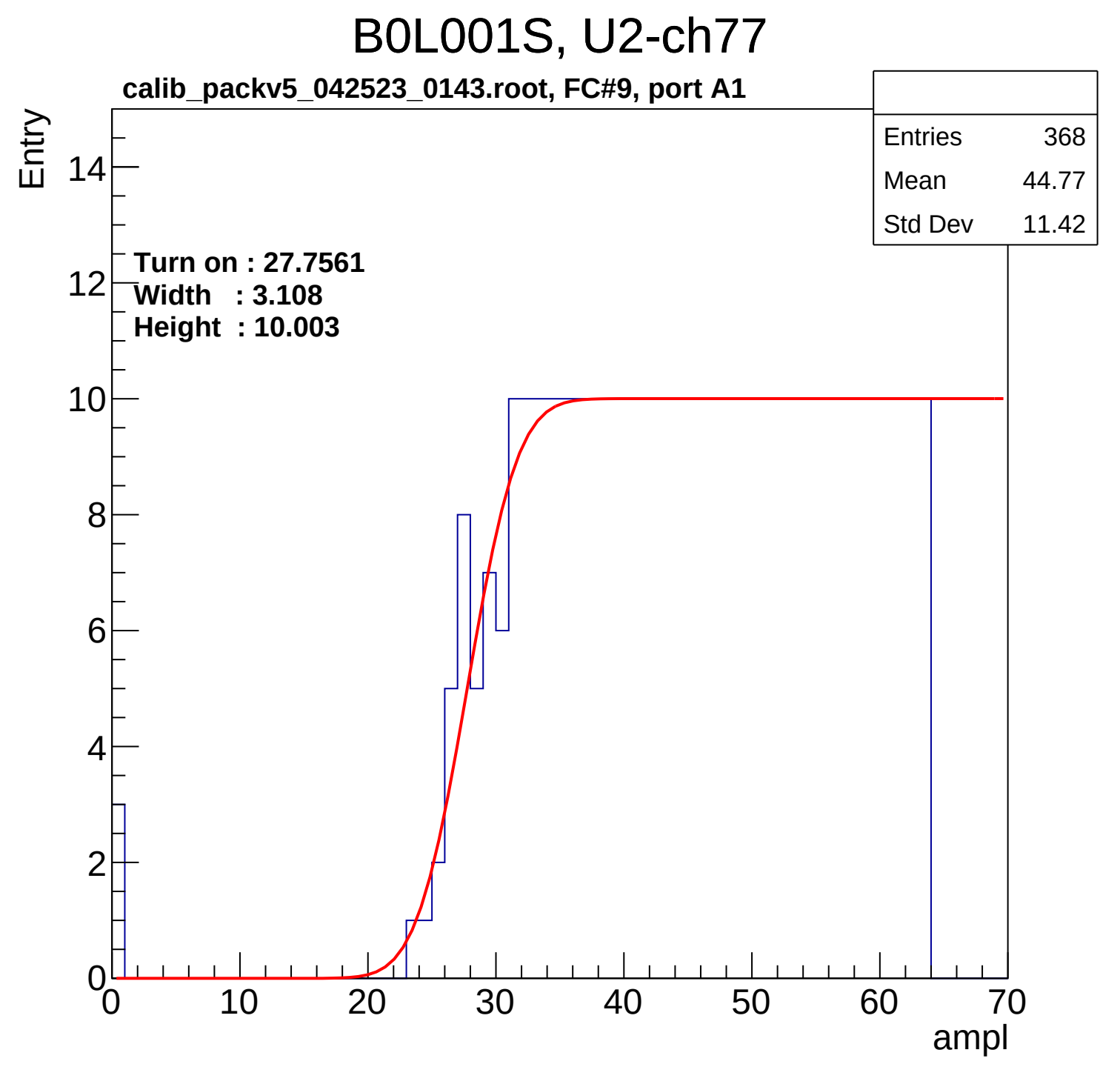
B0L001S, U2-ch77
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.77
Std Dev 11.42
Turn on : 27.7561
Width : 3.108
Height : 10.003
Entry
ampl
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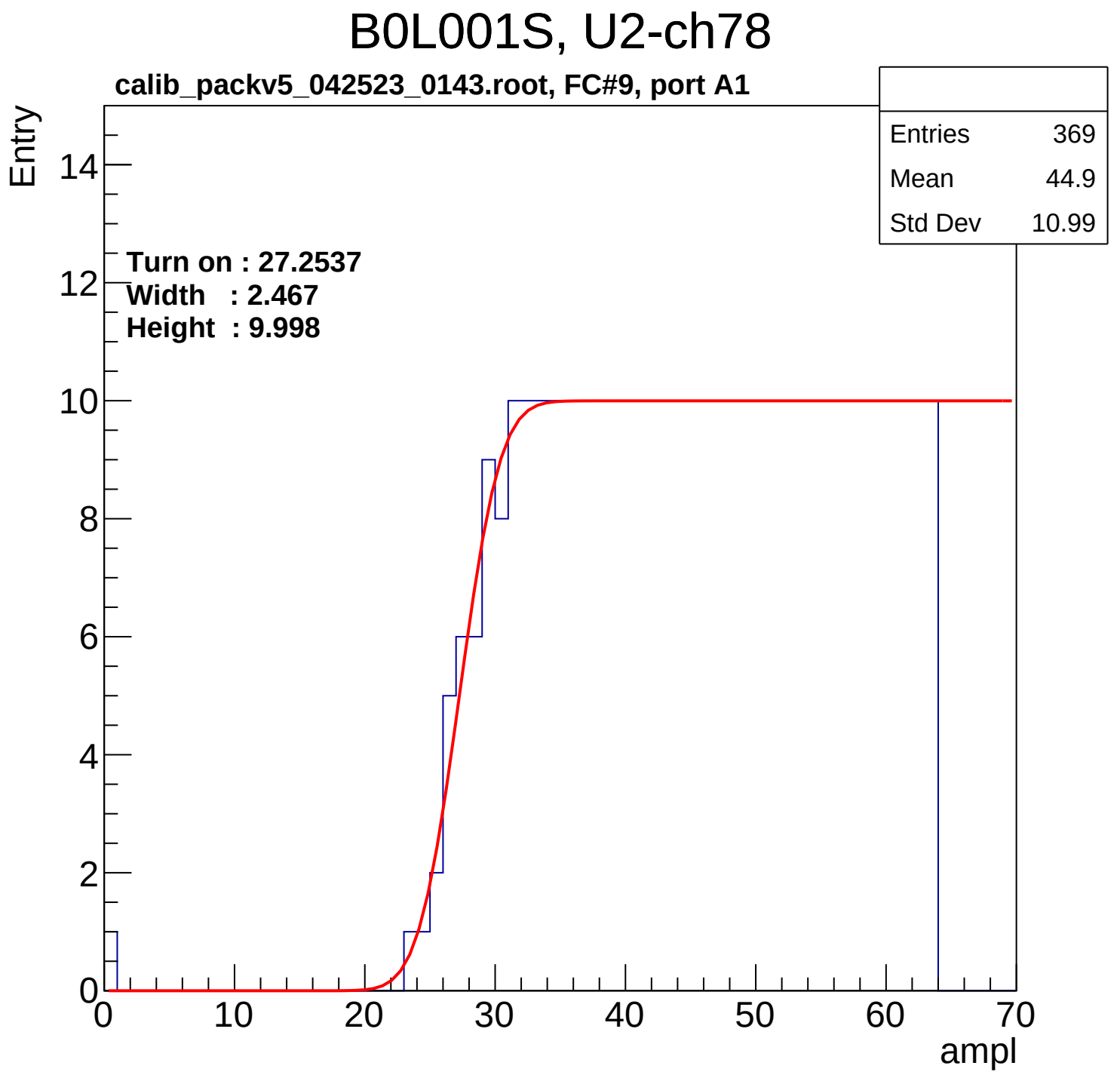
B0L001S, U2-ch78
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.9
Std Dev 10.99
Turn on : 27.2537
Width : 2.467
Height : 9.998
Entry
ampl
0
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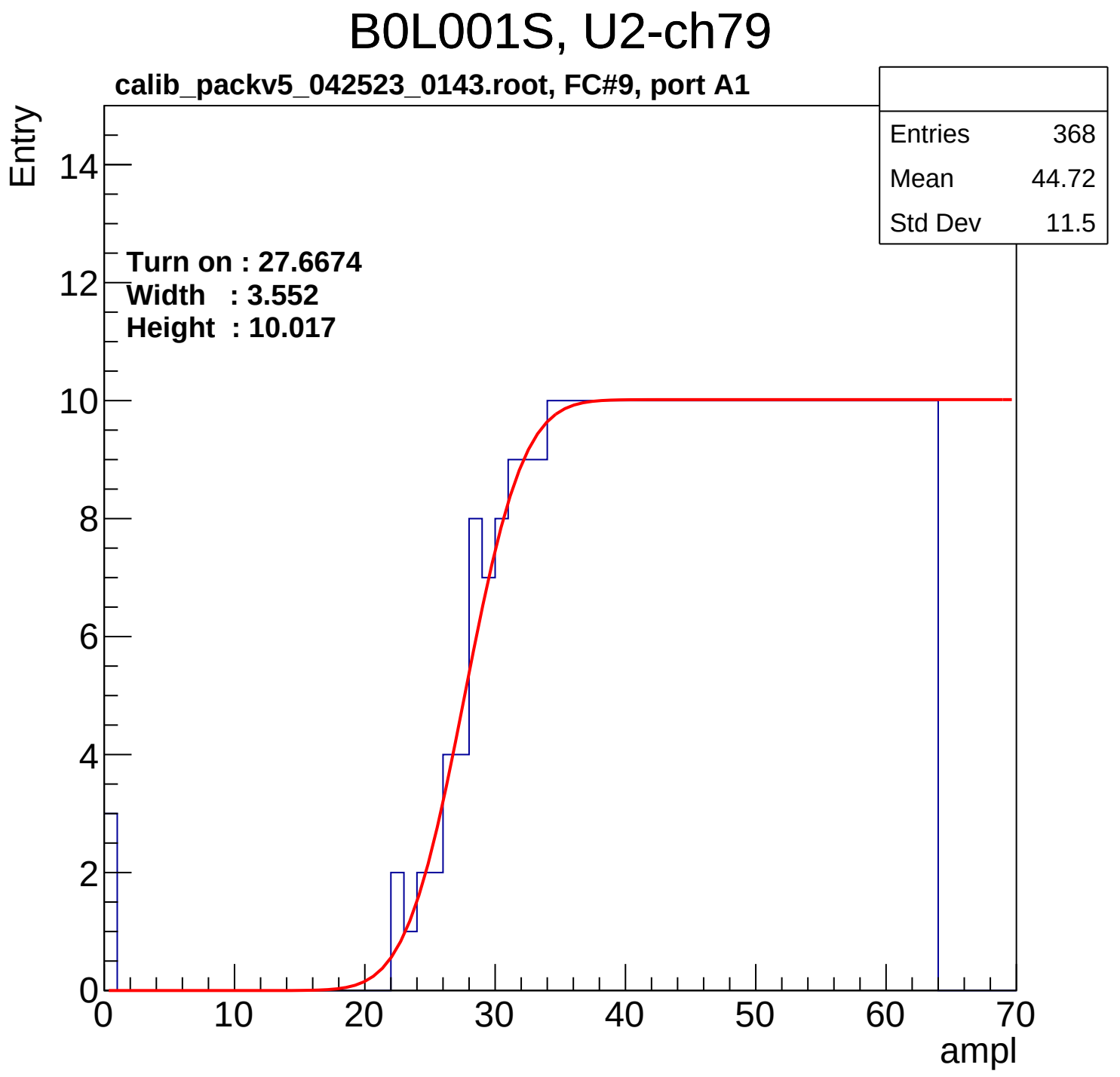
B0L001S, U2-ch79
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.72
Std Dev 11.5
Turn on : 27.6674
Width : 3.552
Height : 10.017
Entry
ampl
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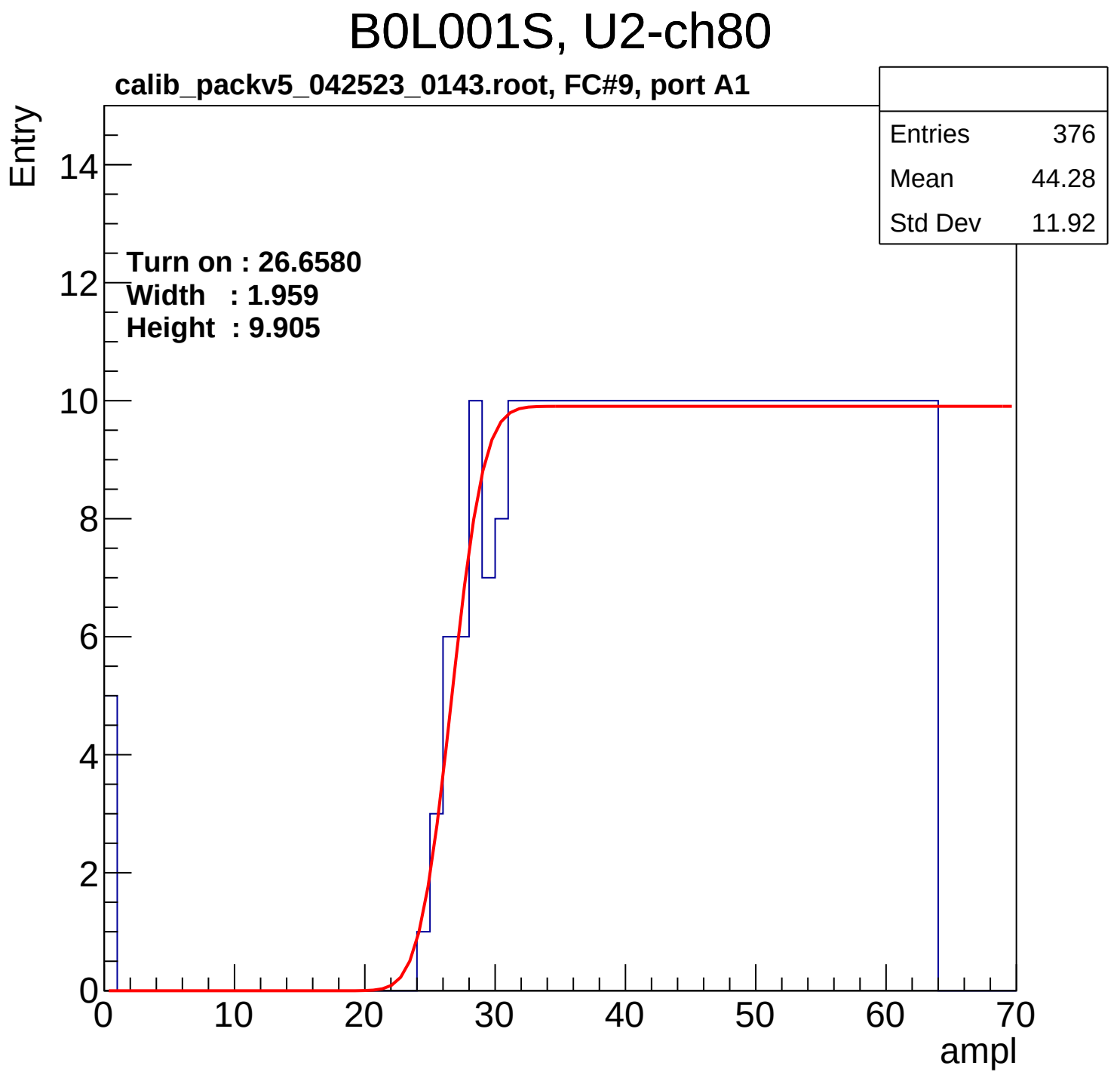
B0L001S, U2-ch80
calib_packv5_042523_0143.root, FC#9, port A1
Entries 376
Mean 44.28
Std Dev 11.92
Turn on : 26.6580
Width : 1.959
Height : 9.905
Entry
ampl
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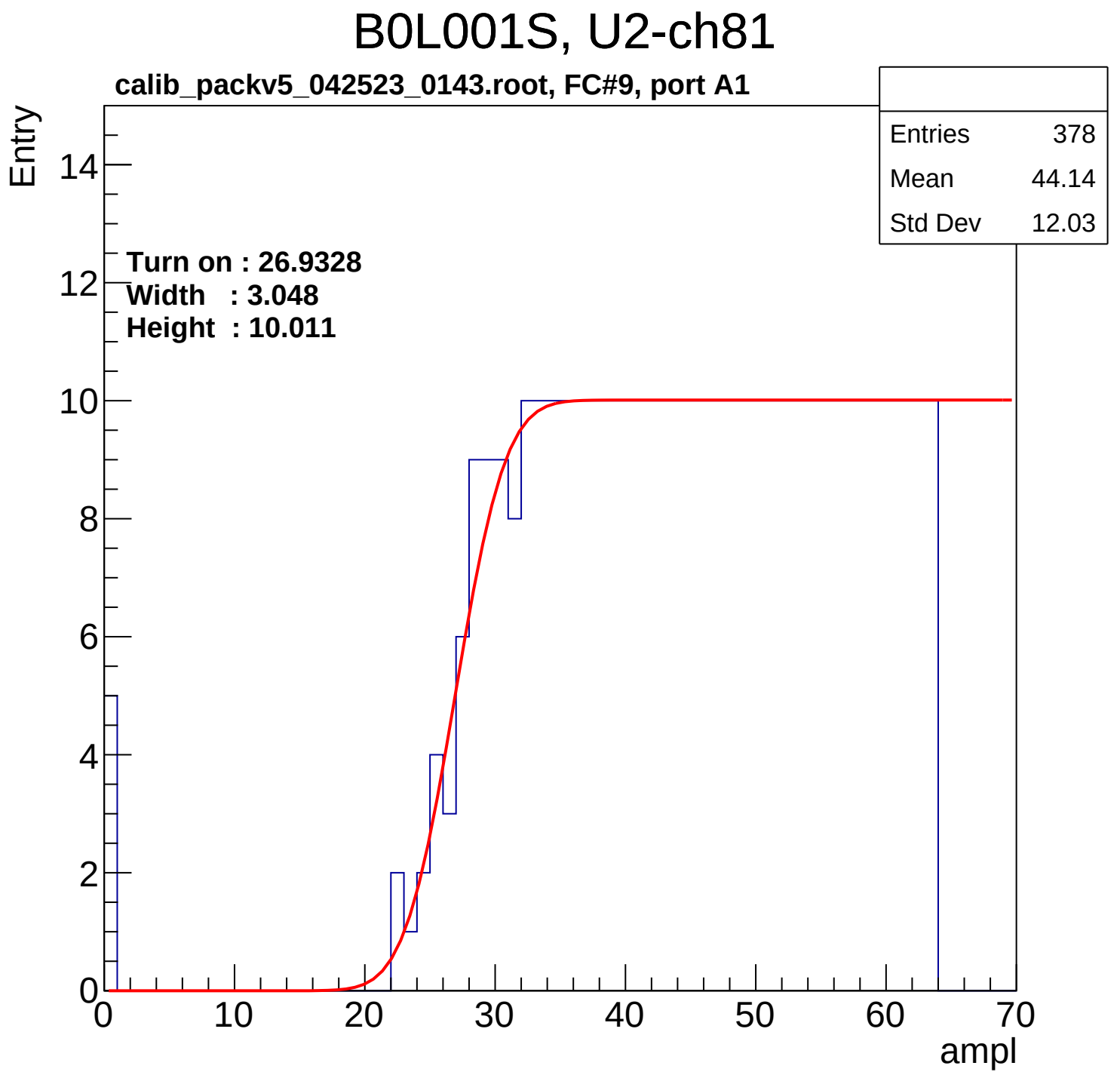
B0L001S, U2-ch81
calib_packv5_042523_0143.root, FC#9, port A1
Entries 378
Mean 44.14
Std Dev 12.03
Turn on : 26.9328
Width : 3.048
Height : 10.011
Entry
ampl
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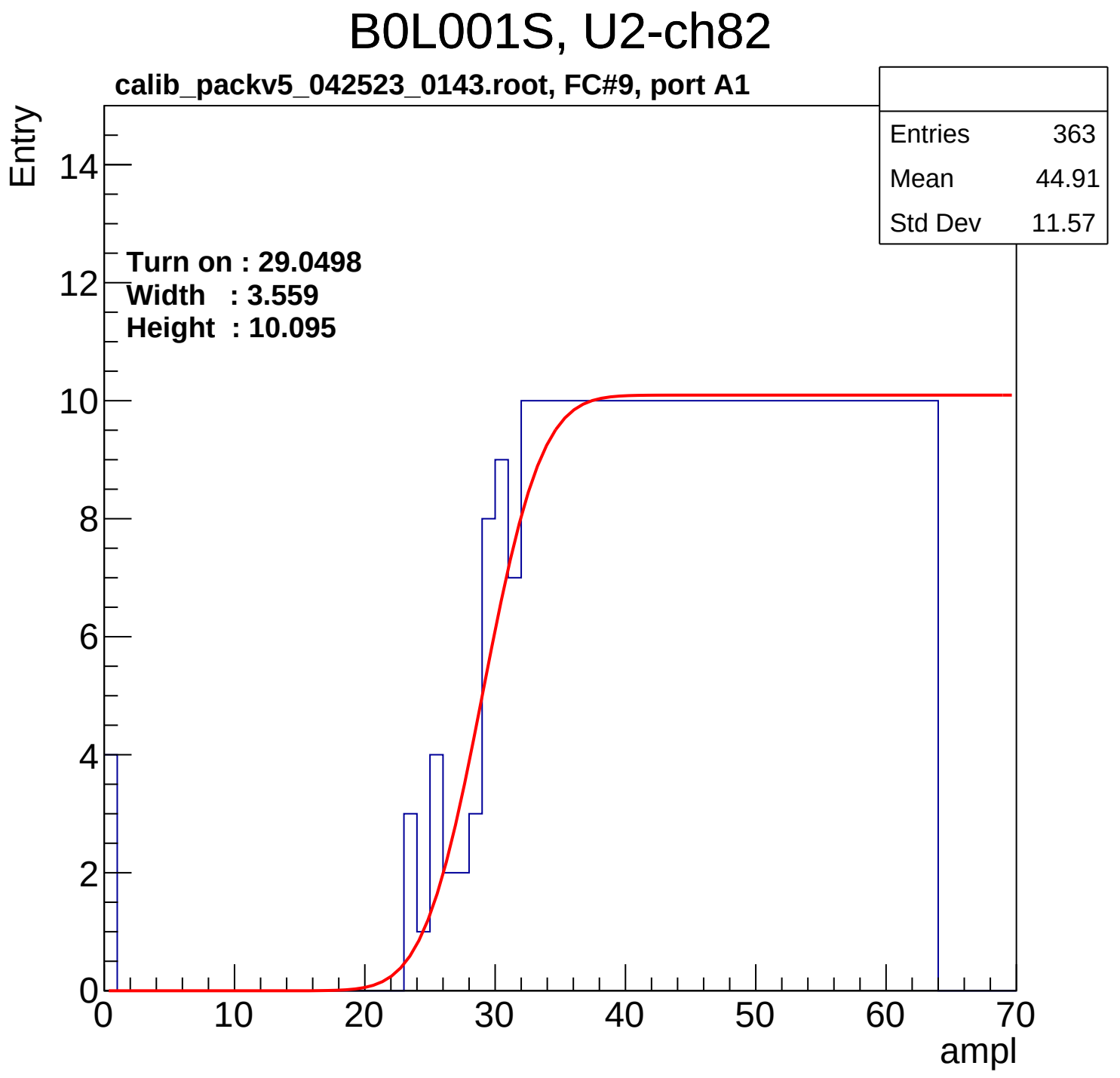
B0L001S, U2-ch82
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 44.91
Std Dev 11.57
Turn on : 29.0498
Width : 3.559
Height : 10.095
Entry
ampl
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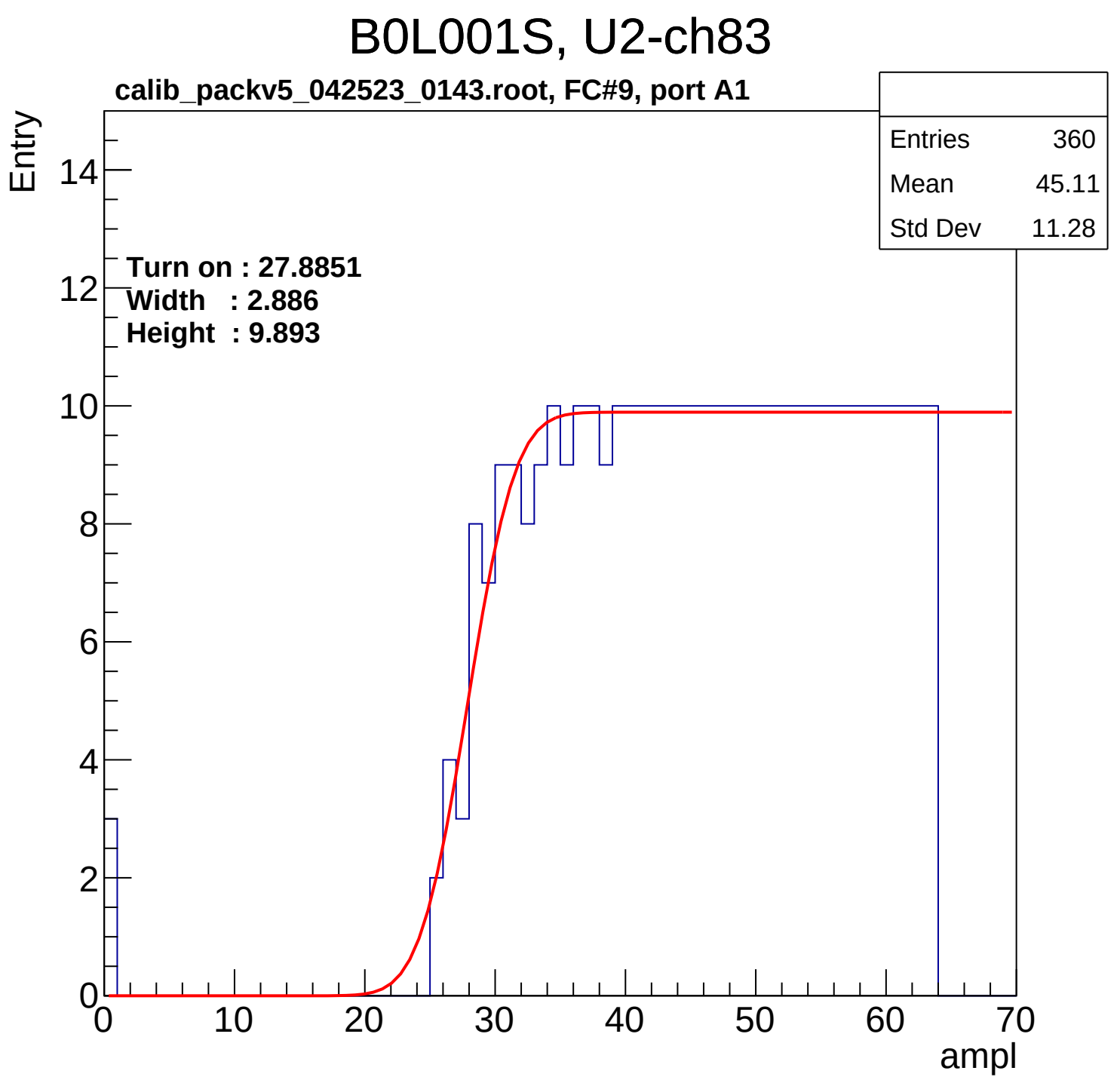
B0L001S, U2-ch83
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 45.11
Std Dev 11.28
Turn on : 27.8851
Width : 2.886
Height : 9.893
Entry
ampl
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4
6
8
10
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0
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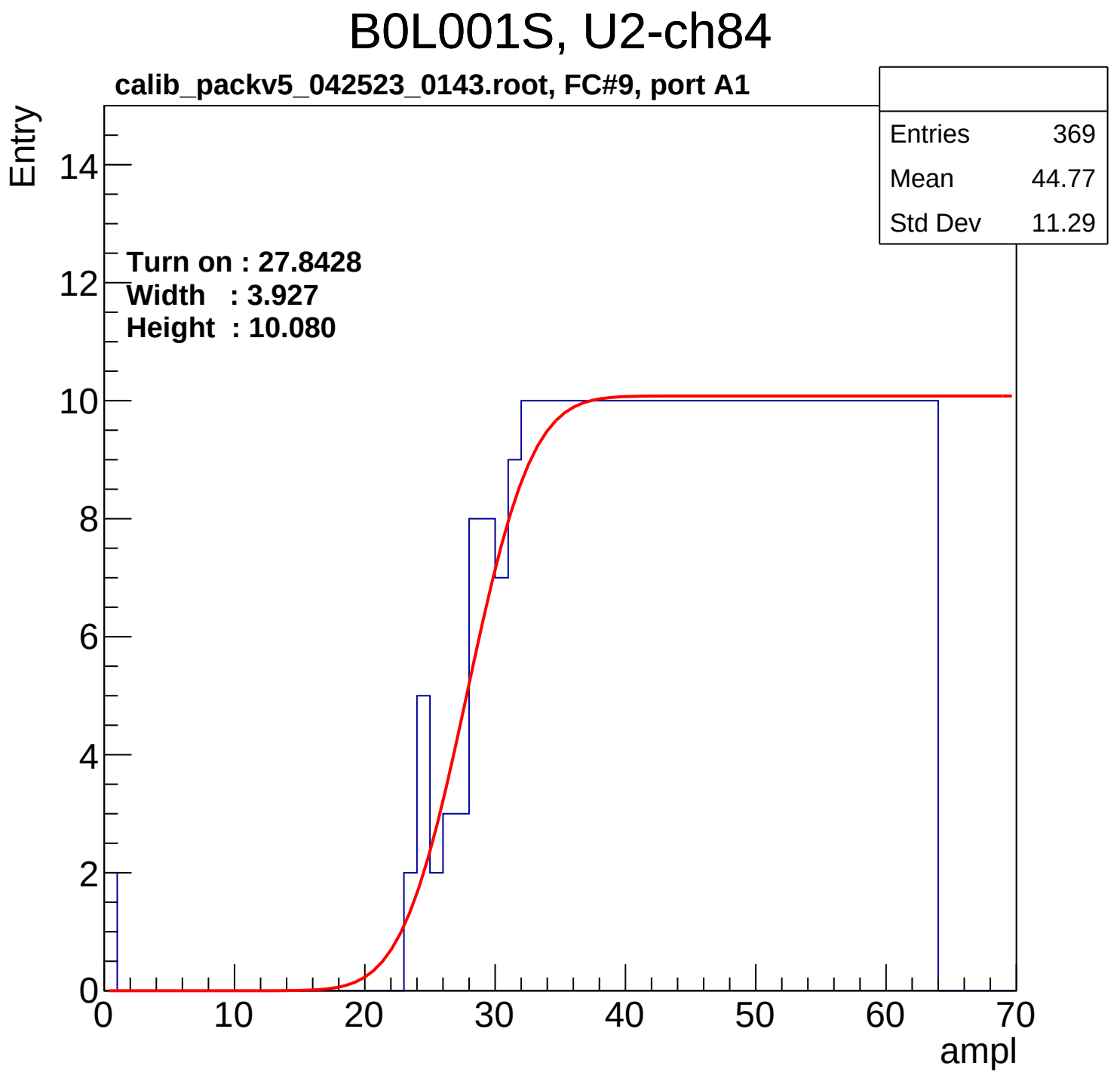
B0L001S, U2-ch84
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.77
Std Dev 11.29
Turn on : 27.8428
Width : 3.927
Height : 10.080
Entry
ampl
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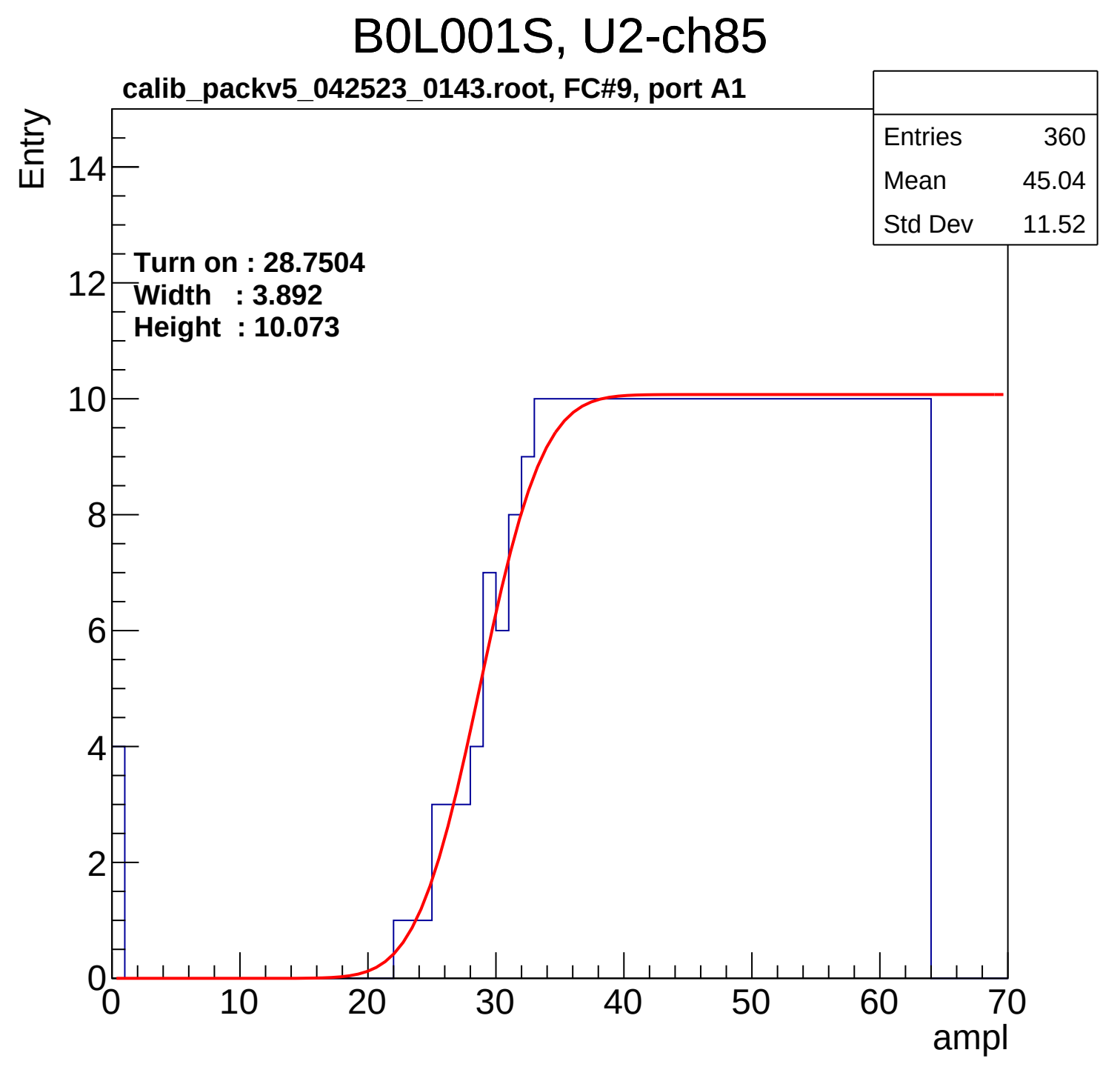
B0L001S, U2-ch85
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 45.04
Std Dev 11.52
Turn on : 28.7504
Width : 3.892
Height : 10.073
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ampl
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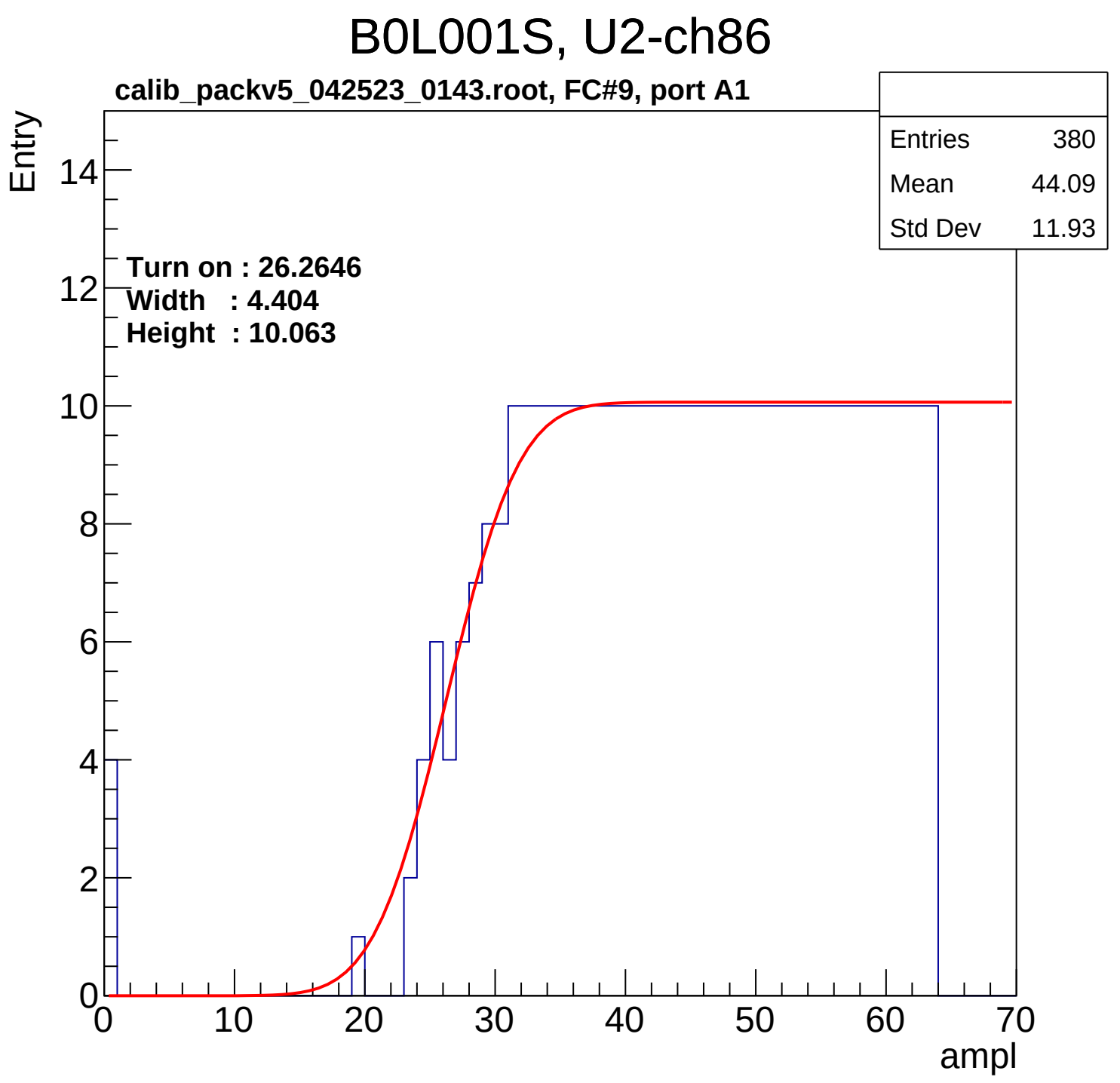
B0L001S, U2-ch86
calib_packv5_042523_0143.root, FC#9, port A1
Entries 380
Mean 44.09
Std Dev 11.93
Turn on : 26.2646
Width : 4.404
Height : 10.063
Entry
ampl
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12
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20
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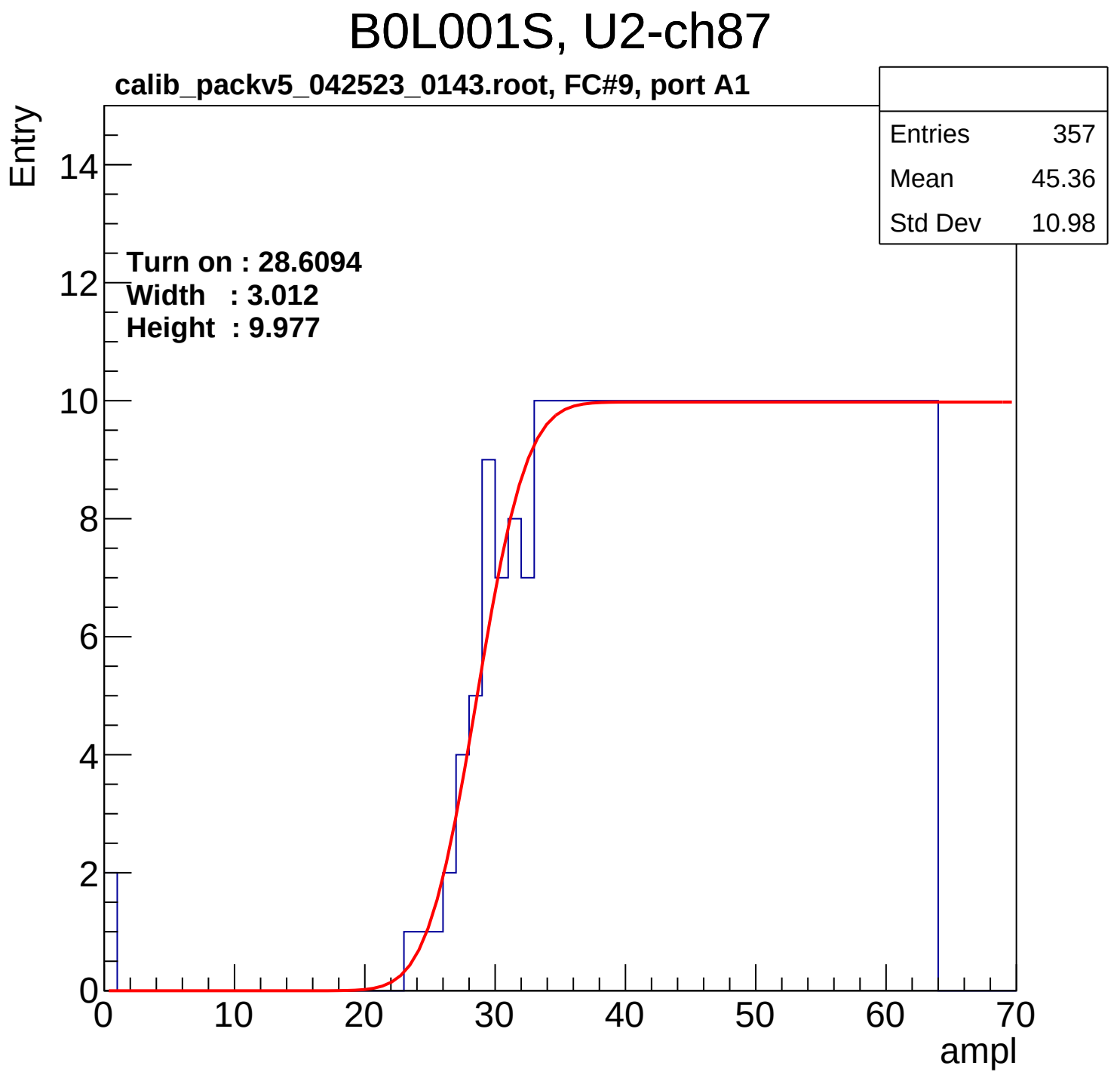
B0L001S, U2-ch87
calib_packv5_042523_0143.root, FC#9, port A1
Entries 357
Mean 45.36
Std Dev 10.98
Turn on : 28.6094
Width : 3.012
Height : 9.977
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ampl
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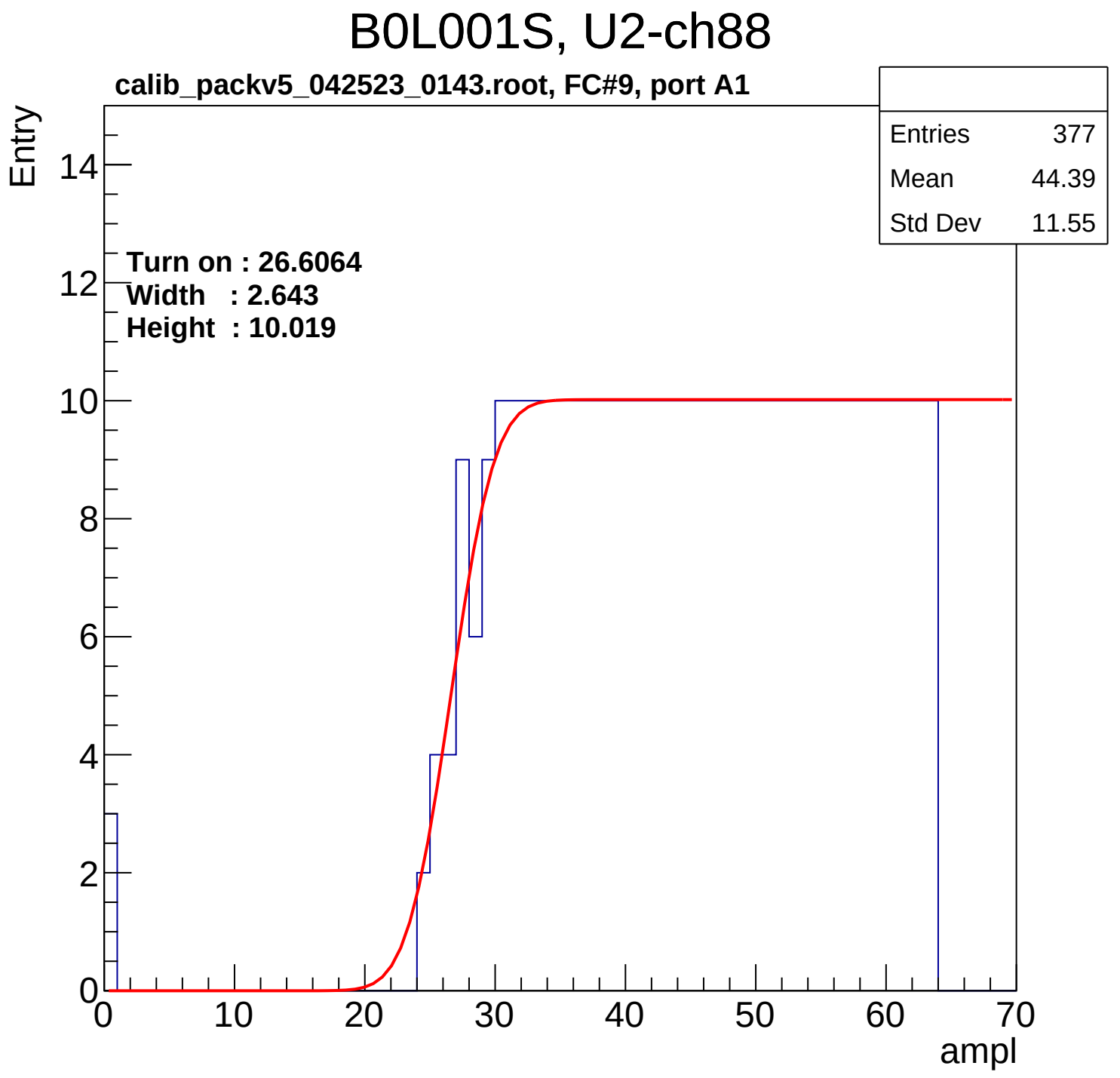
B0L001S, U2-ch88
calib_packv5_042523_0143.root, FC#9, port A1
Entries 377
Mean 44.39
Std Dev 11.55
Turn on : 26.6064
Width : 2.643
Height : 10.019
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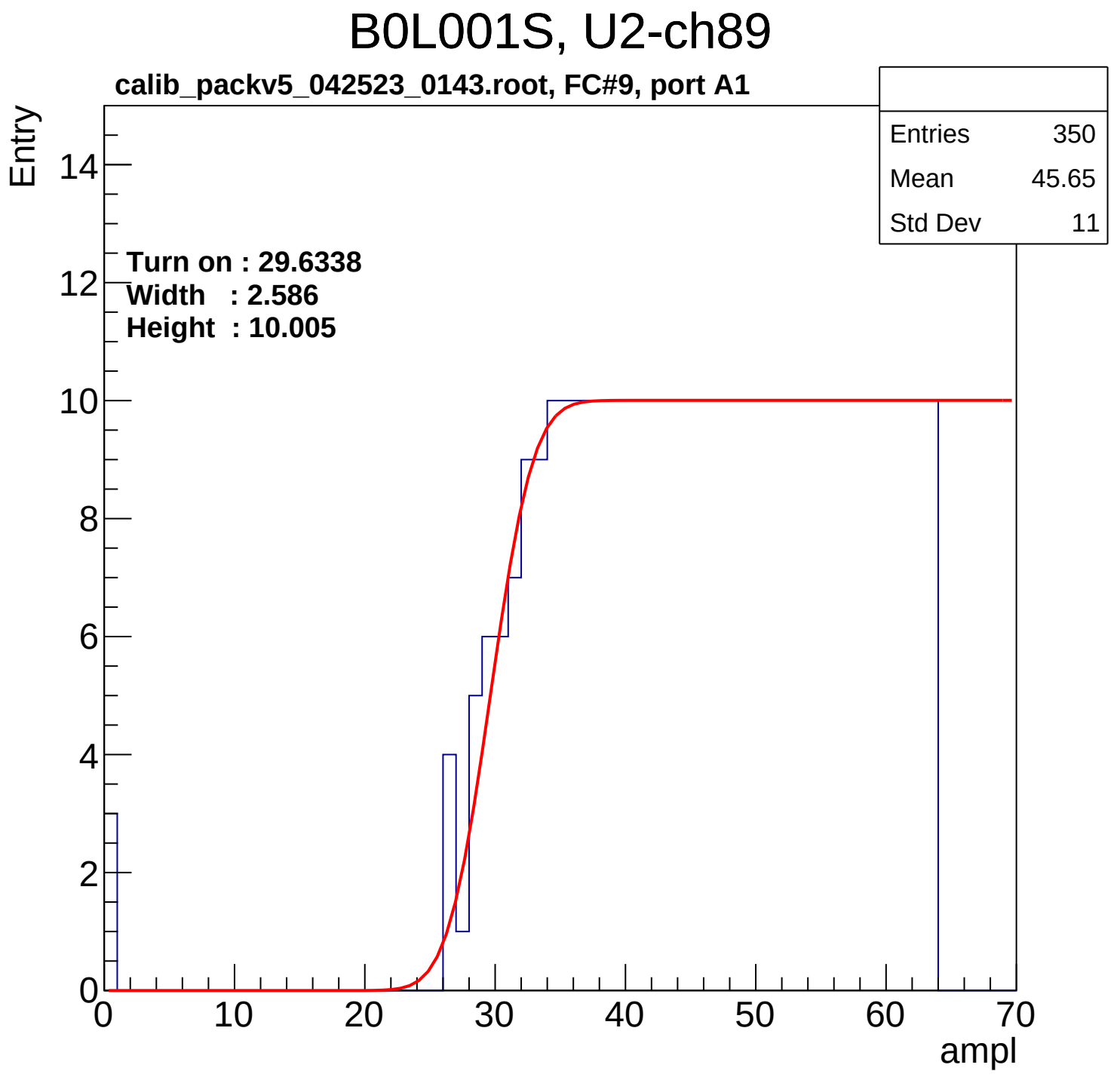
B0L001S, U2-ch89
calib_packv5_042523_0143.root, FC#9, port A1
Entries 350
Mean 45.65
Std Dev 11
Turn on : 29.6338
Width : 2.586
Height : 10.005
Entry
ampl
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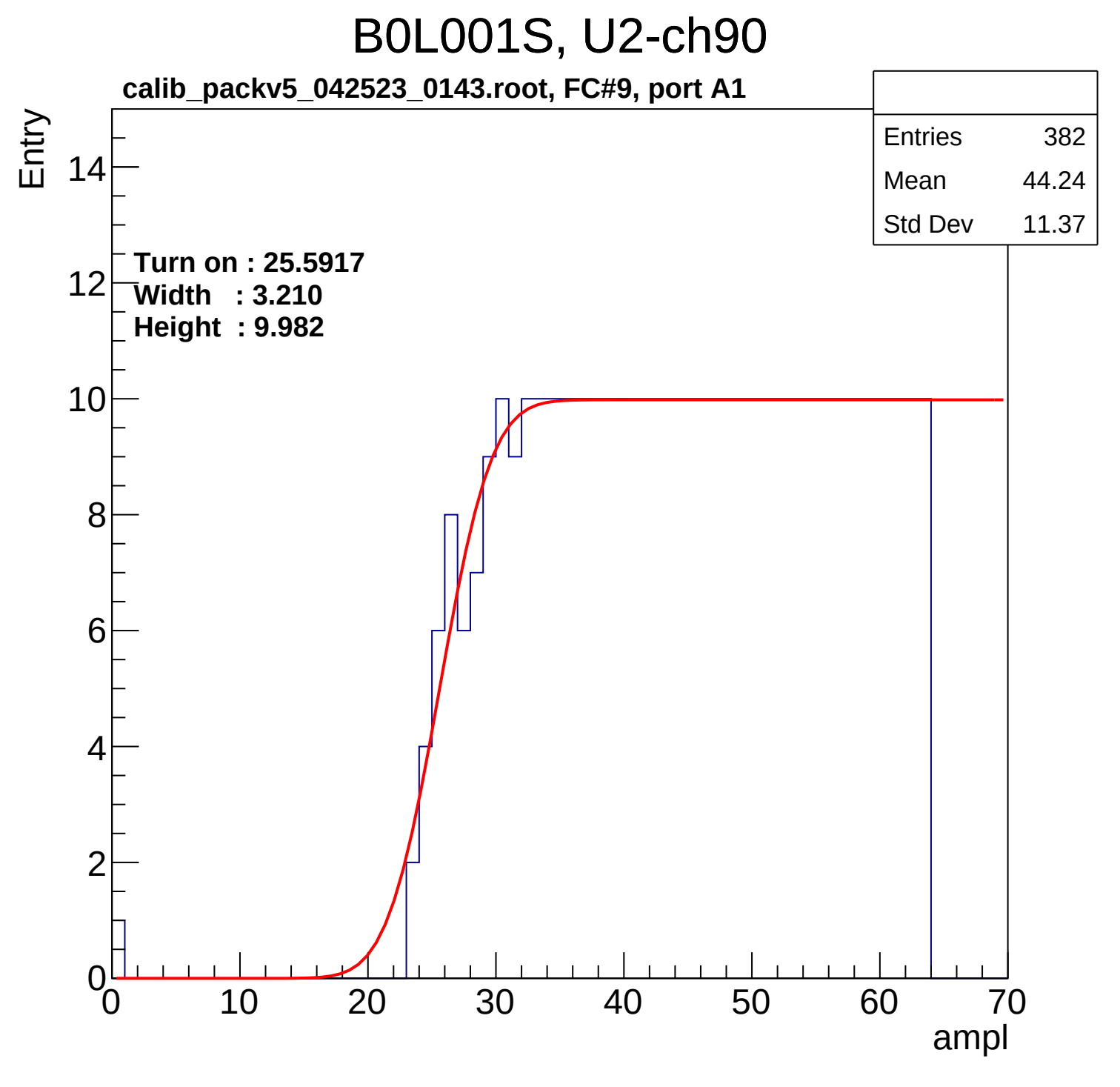
B0L001S, U2-ch90
calib_packv5_042523_0143.root, FC#9, port A1
Entries 382
Mean 44.24
Std Dev 11.37
Turn on : 25.5917
Width : 3.210
Height : 9.982
Entry
ampl
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2
4
6
8
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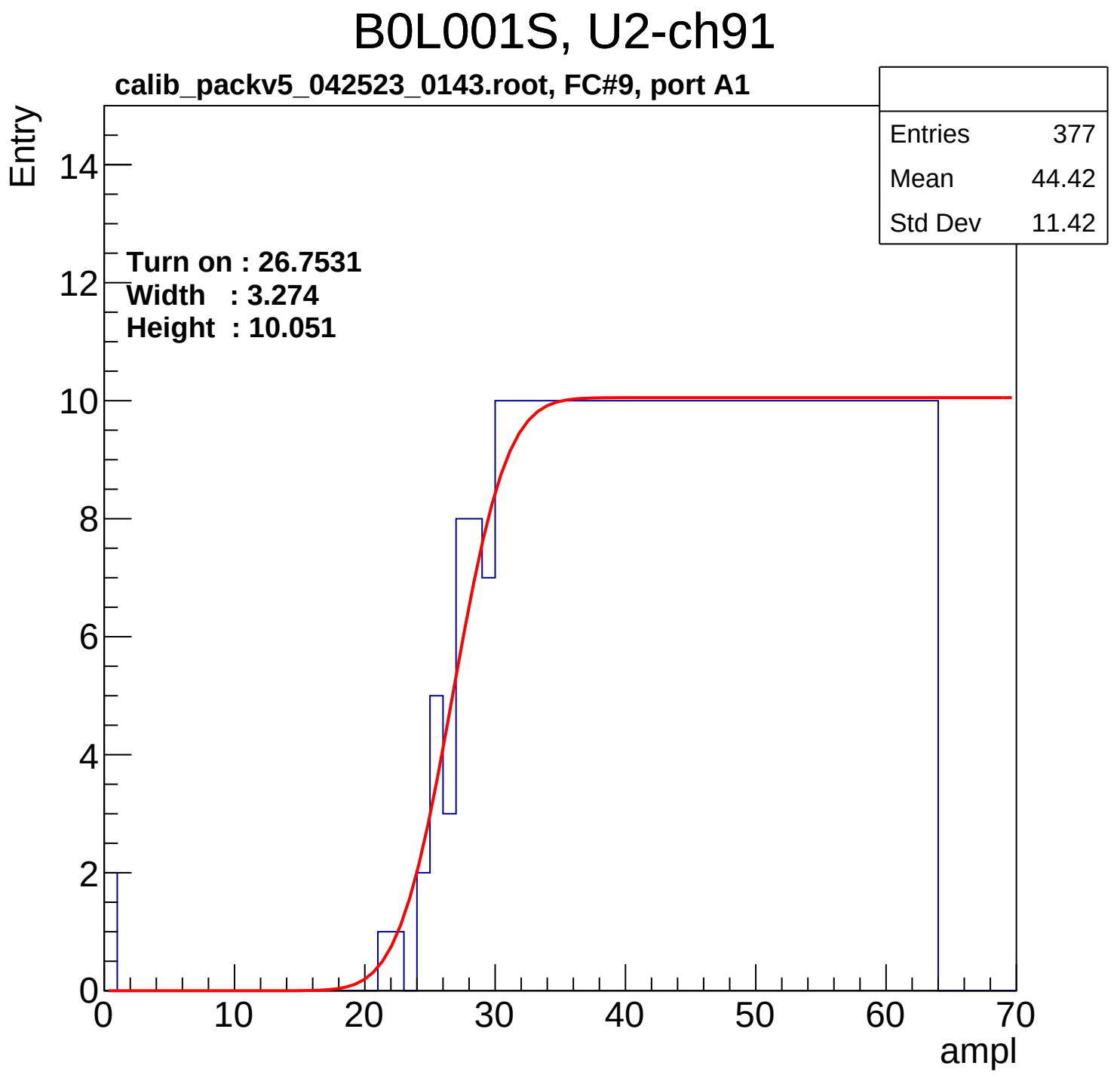
B0L001S, U2-ch91
calib_packv5_042523_0143.root, FC#9, port A1
Entries 377
Mean 44.42
Std Dev 11.42
Turn on : 26.7531
Width : 3.274
Height : 10.051
Entry
ampl
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2
4
6
8
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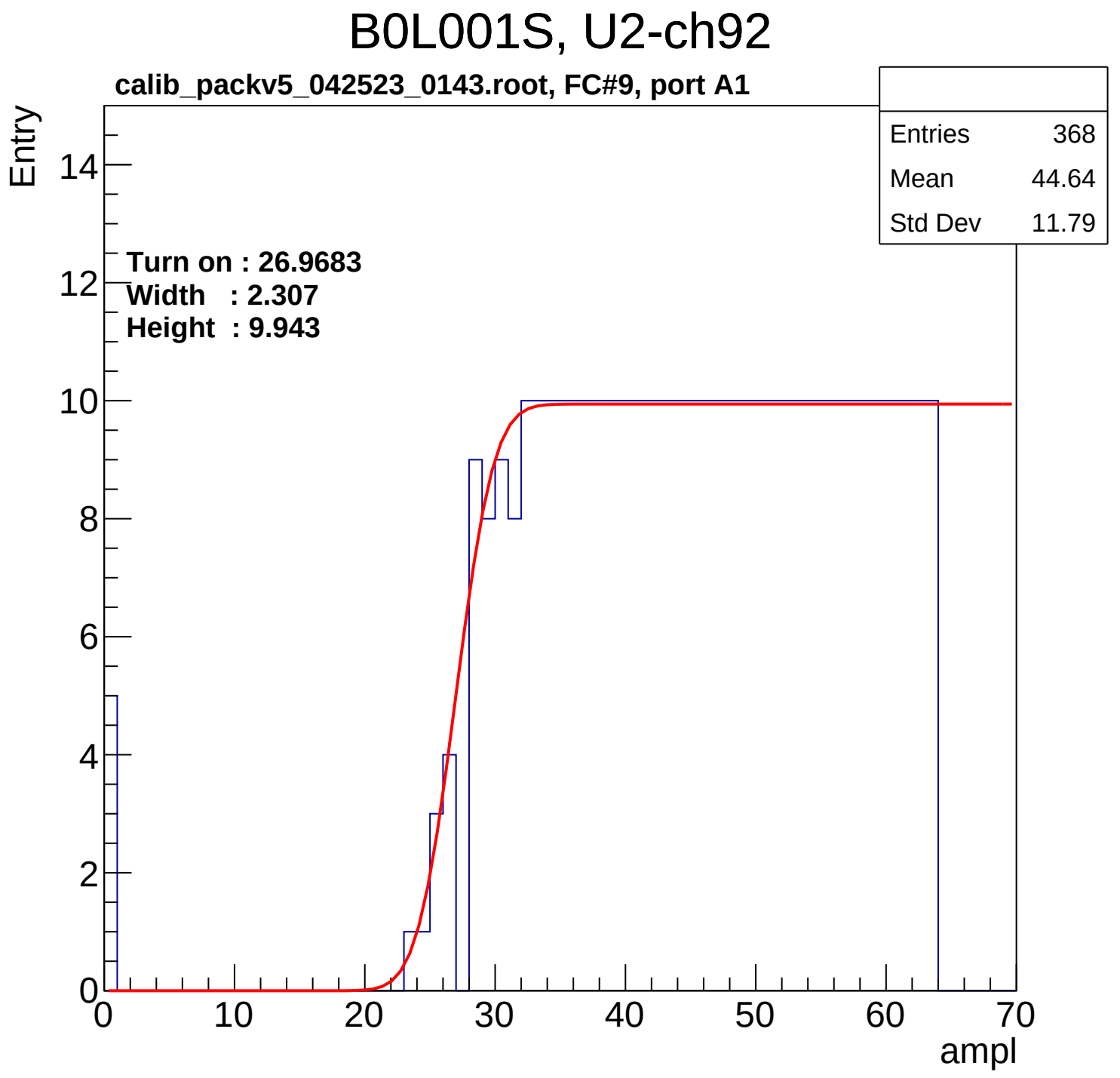
B0L001S, U2-ch92
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.64
Std Dev 11.79
Turn on : 26.9683
Width : 2.307
Height : 9.943
Entry
ampl
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2
4
6
8
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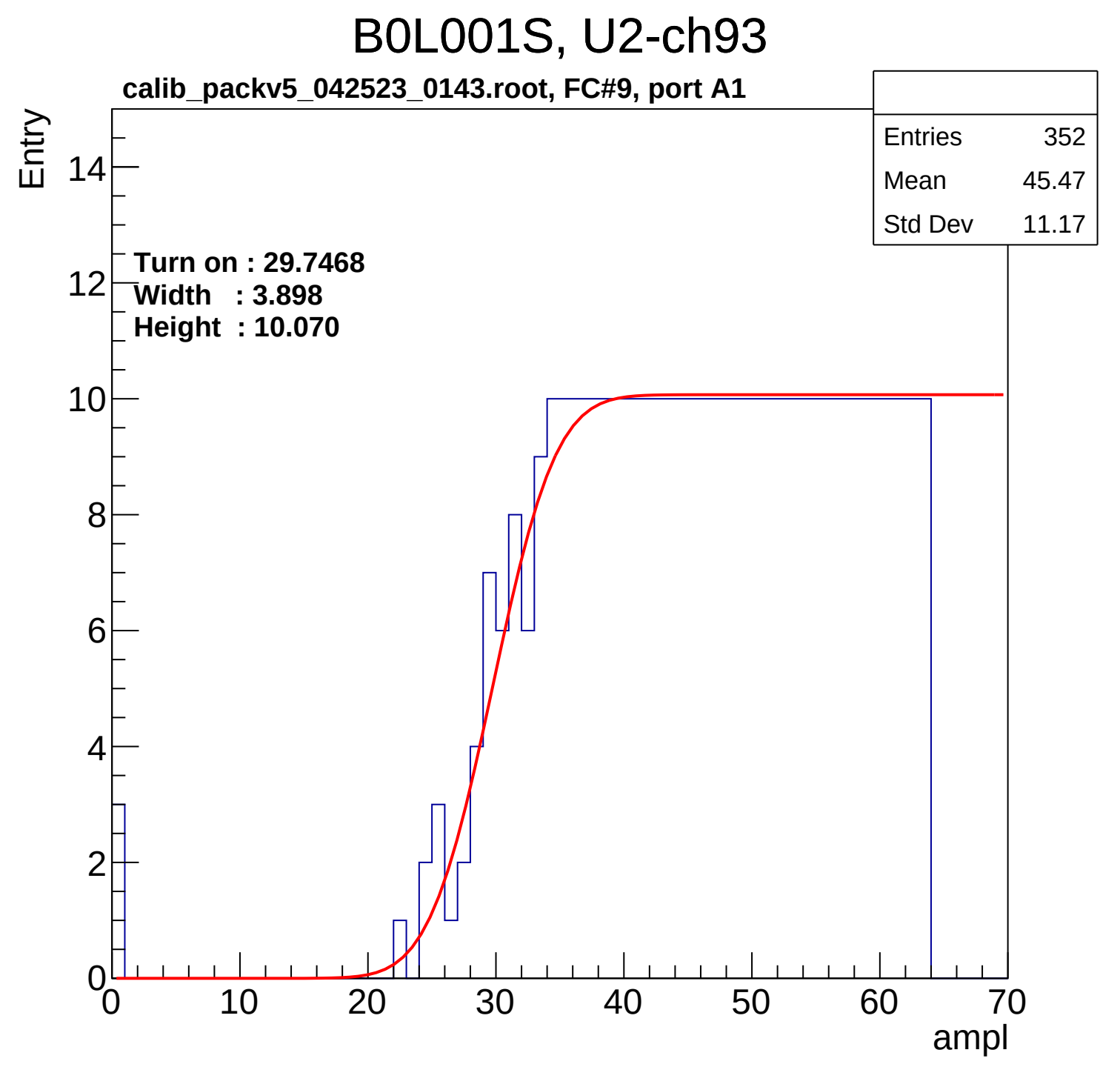
B0L001S, U2-ch93
calib_packv5_042523_0143.root, FC#9, port A1
Entries 352
Mean 45.47
Std Dev 11.17
Turn on : 29.7468
Width : 3.898
Height : 10.070
Entry
ampl
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2
4
6
8
10
12
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0
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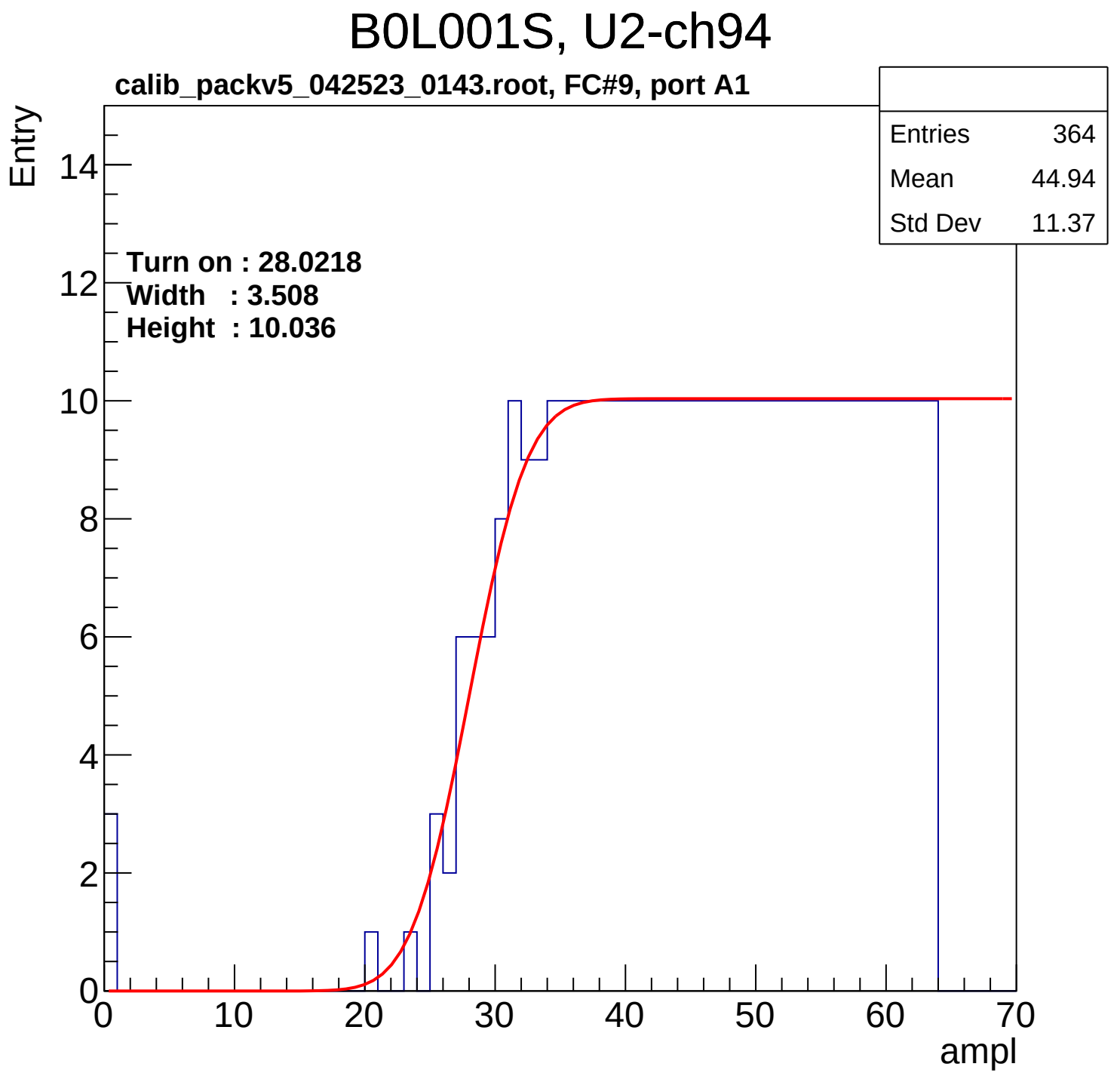
B0L001S, U2-ch94
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 44.94
Std Dev 11.37
Turn on : 28.0218
Width : 3.508
Height : 10.036
Entry
ampl
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2
4
6
8
10
12
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0
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60
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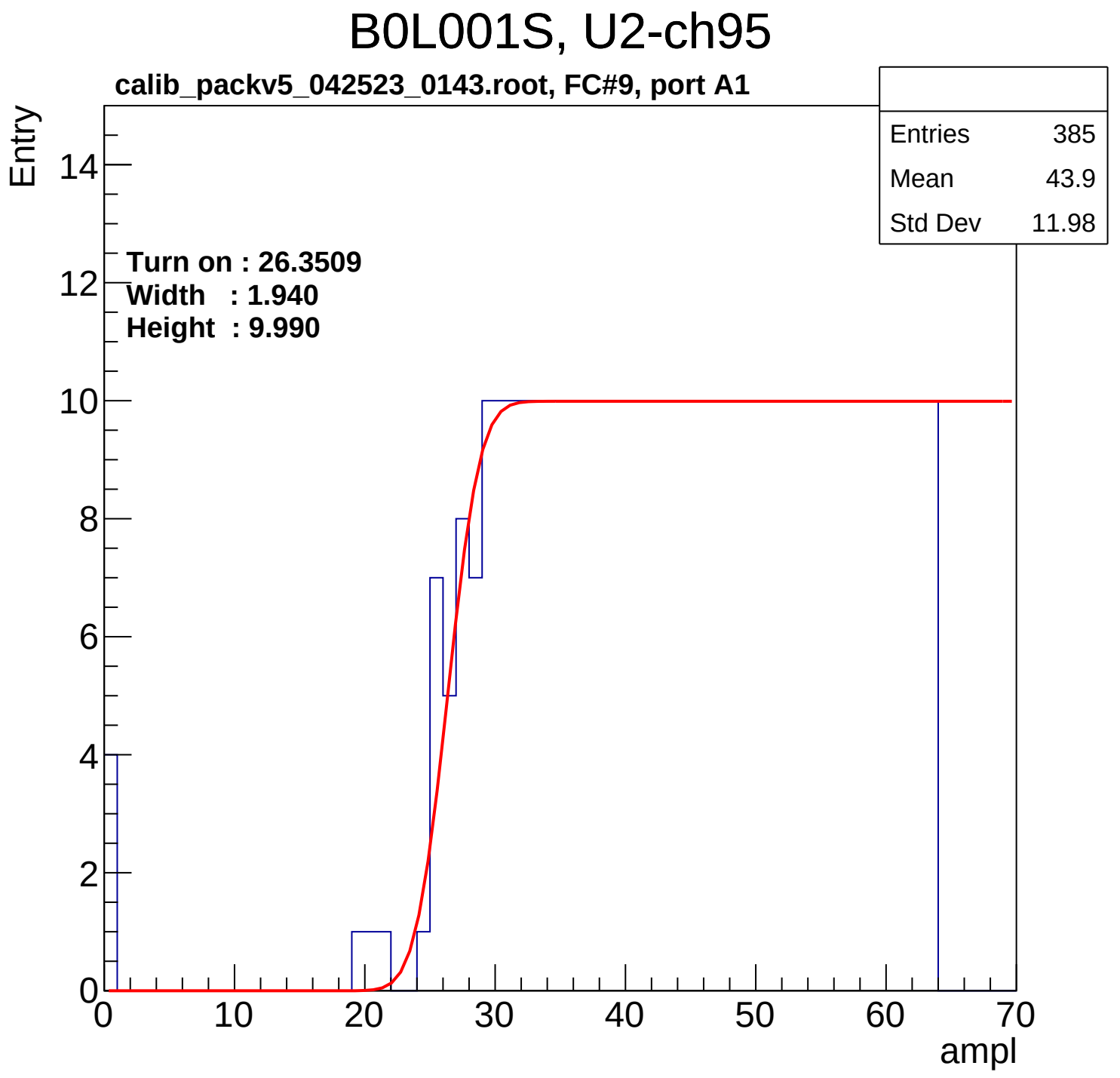
B0L001S, U2-ch95
calib_packv5_042523_0143.root, FC#9, port A1
Entries 385
Mean 43.9
Std Dev 11.98
Turn on : 26.3509
Width : 1.940
Height : 9.990
Entry
ampl
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2
4
6
8
10
12
14
0
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60
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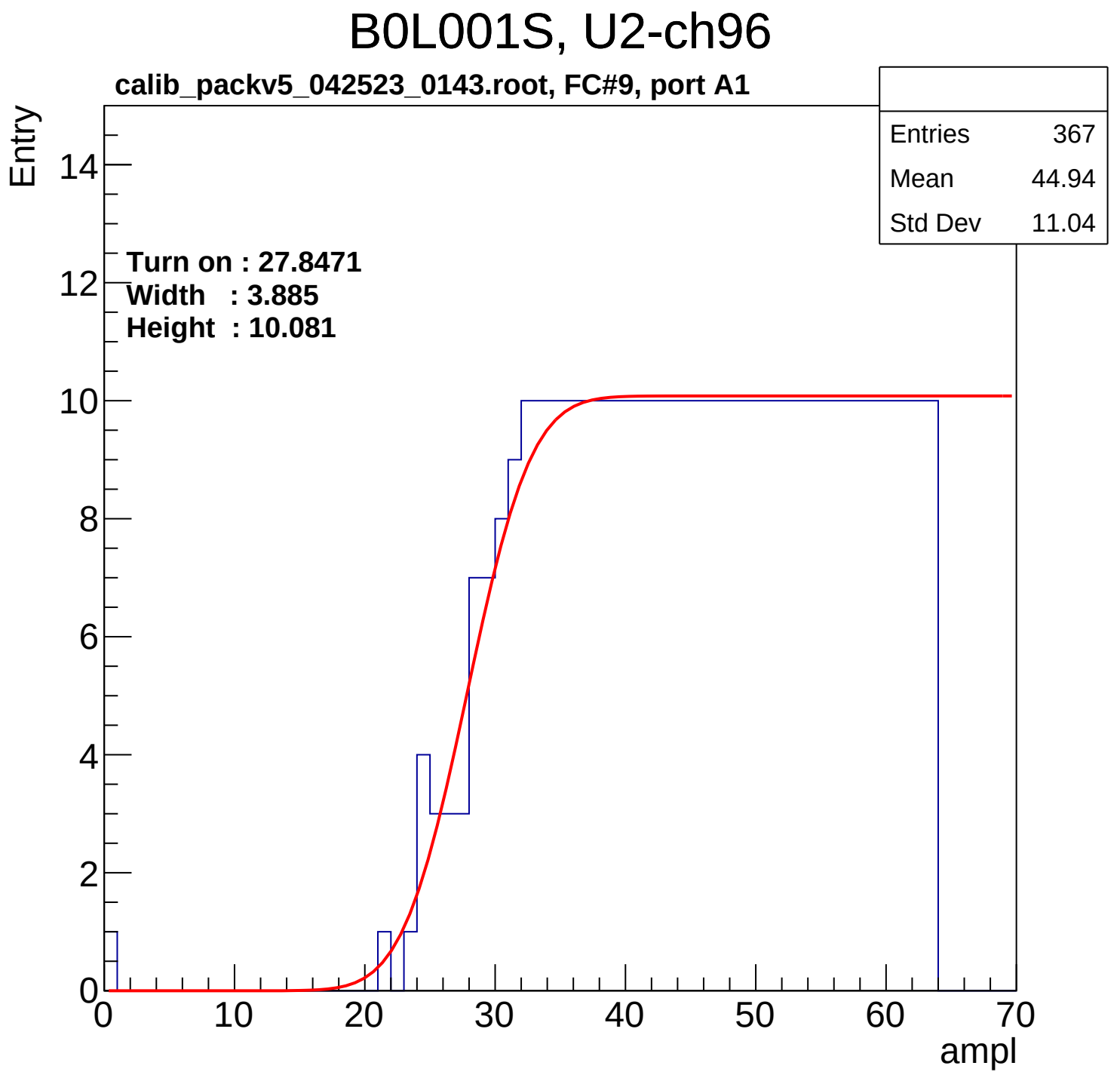
B0L001S, U2-ch96
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.94
Std Dev 11.04
Turn on : 27.8471
Width : 3.885
Height : 10.081
Entry
ampl
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2
4
6
8
10
12
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0
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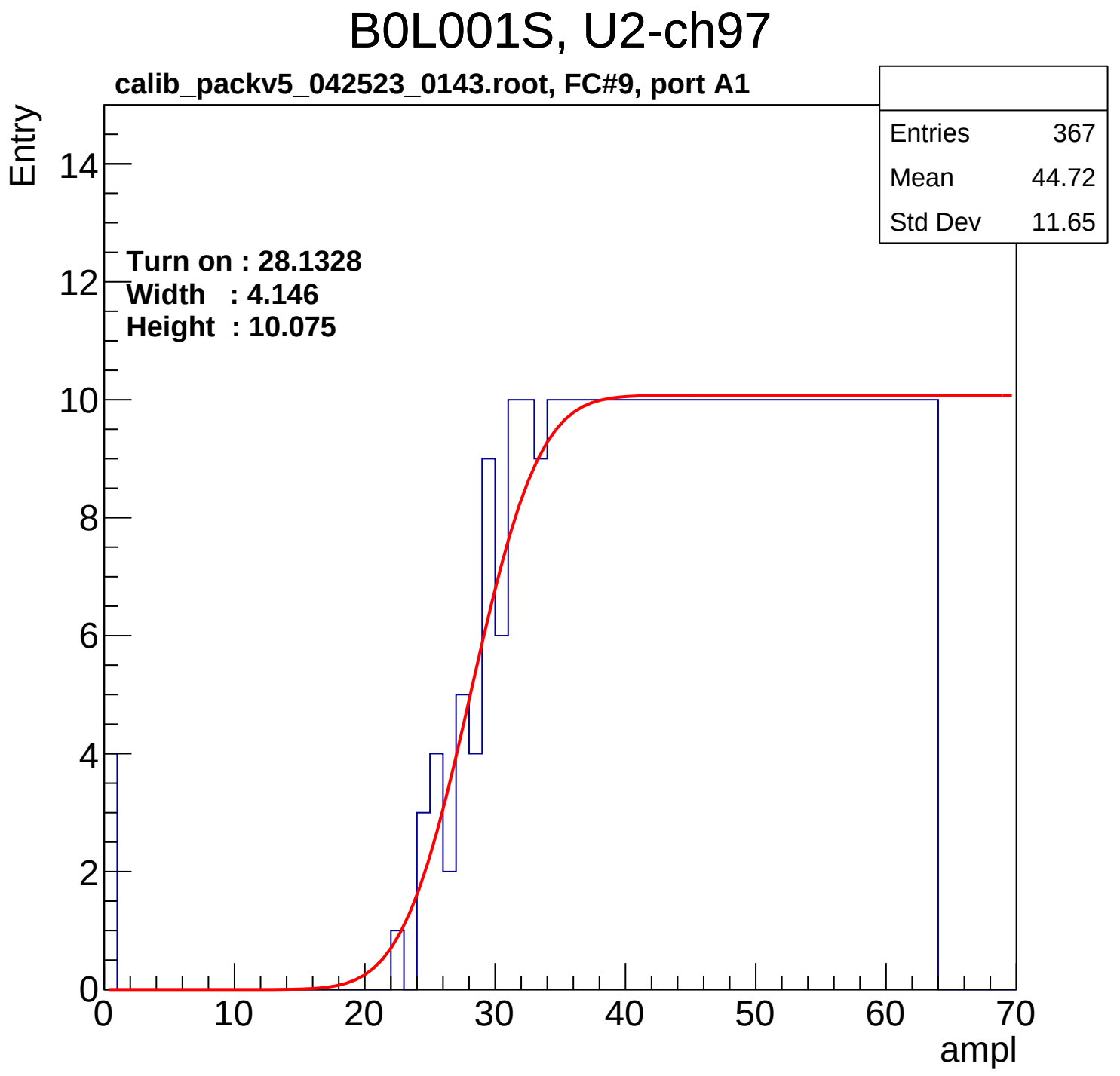
B0L001S, U2-ch97
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.72
Std Dev 11.65
Turn on : 28.1328
Width : 4.146
Height : 10.075
Entry
ampl
0
2
4
6
8
10
12
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0
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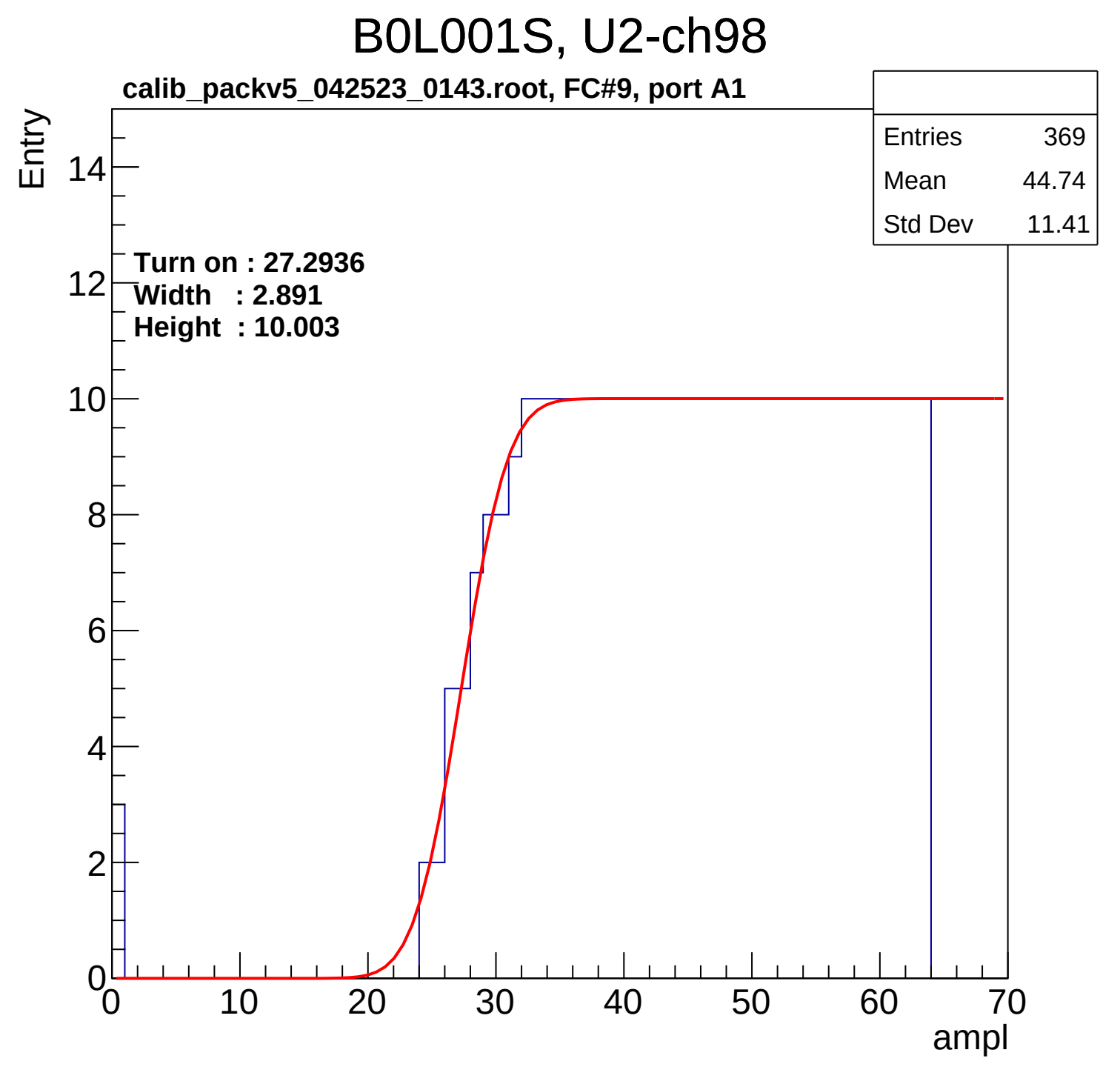
B0L001S, U2-ch98
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.74
Std Dev 11.41
Turn on : 27.2936
Width : 2.891
Height : 10.003
Entry
ampl
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6
8
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12
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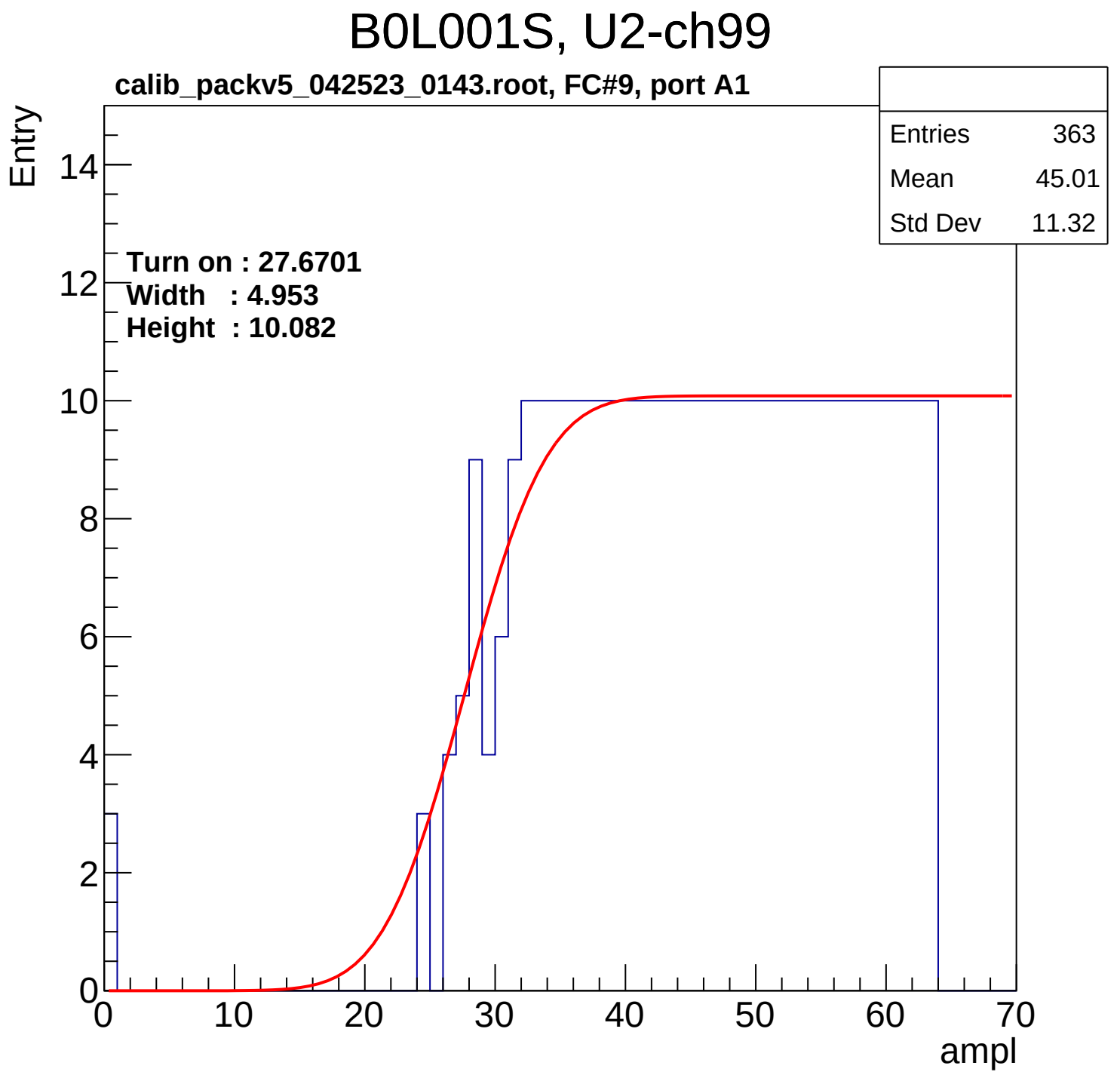
B0L001S, U2-ch99
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 45.01
Std Dev 11.32
Turn on : 27.6701
Width : 4.953
Height : 10.082
Entry
ampl
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6
8
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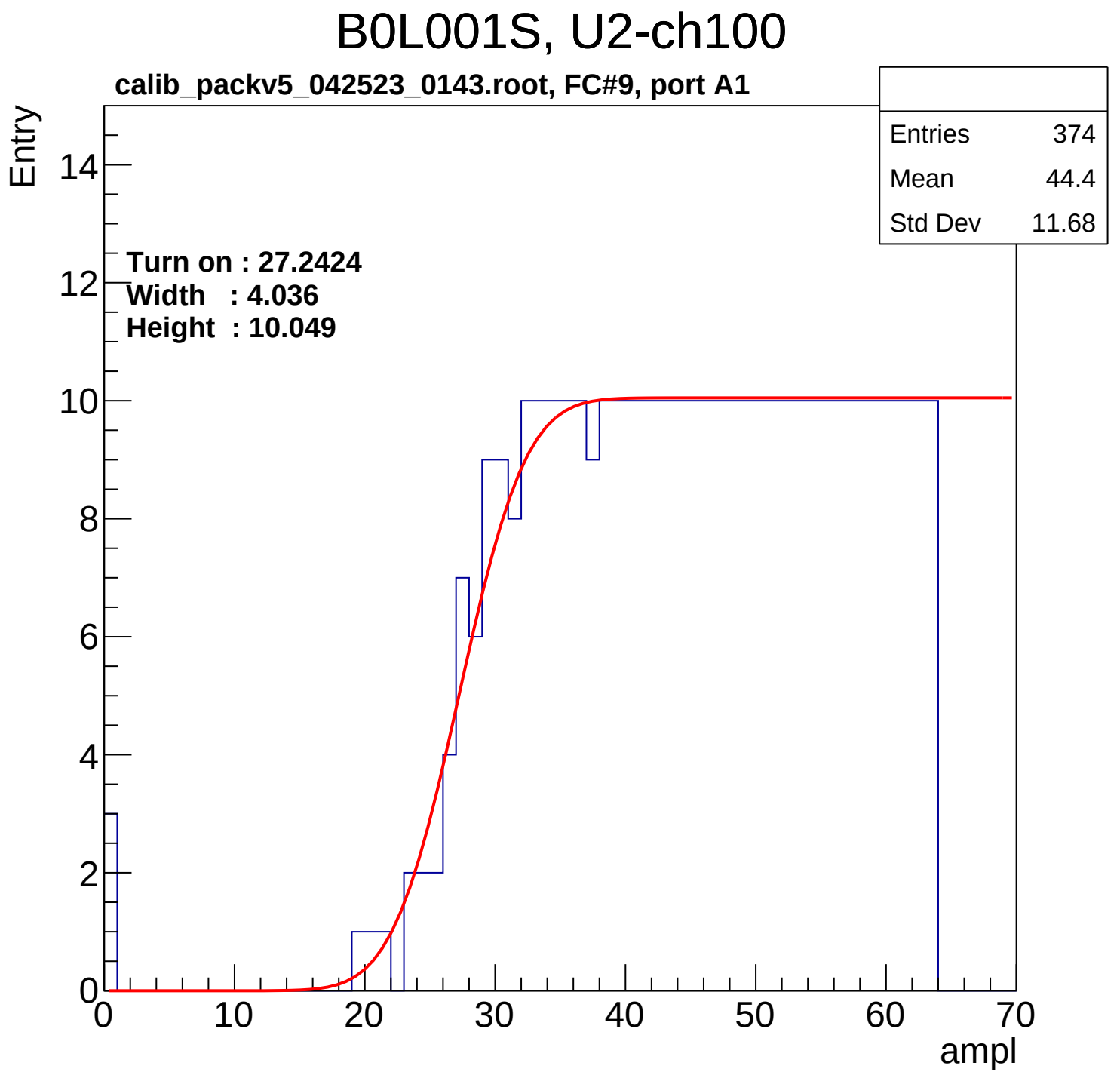
B0L001S, U2-ch100
calib_packv5_042523_0143.root, FC#9, port A1
Entries 374
Mean 44.4
Std Dev 11.68
Turn on : 27.2424
Width : 4.036
Height : 10.049
Entry
ampl
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6
8
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0
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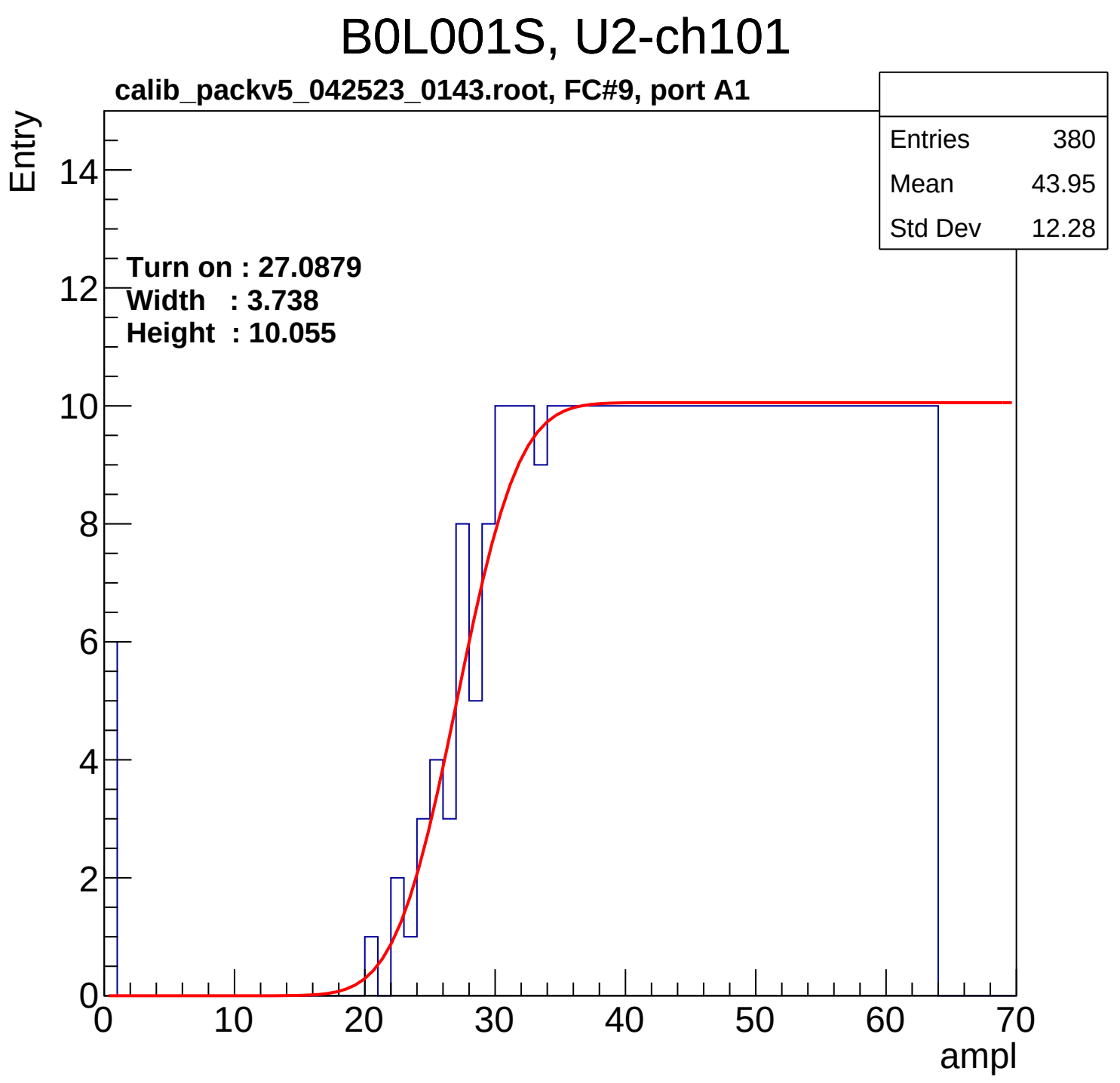
B0L001S, U2-ch101
calib_packv5_042523_0143.root, FC#9, port A1
Entries 380
Mean 43.95
Std Dev 12.28
Turn on : 27.0879
Width : 3.738
Height : 10.055
Entry
ampl
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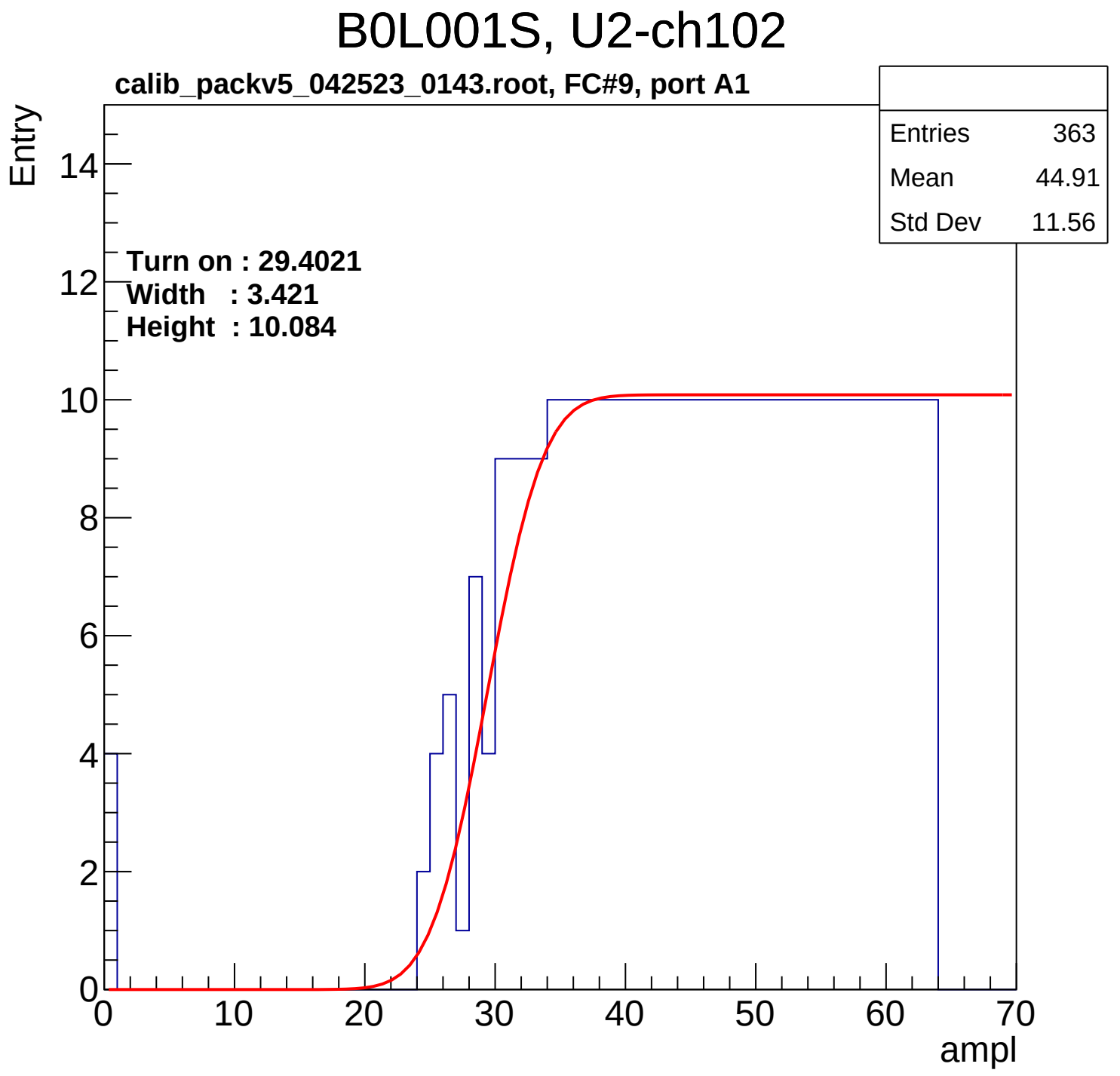
B0L001S, U2-ch102
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 44.91
Std Dev 11.56
Turn on : 29.4021
Width : 3.421
Height : 10.084
Entry
ampl
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6
8
10
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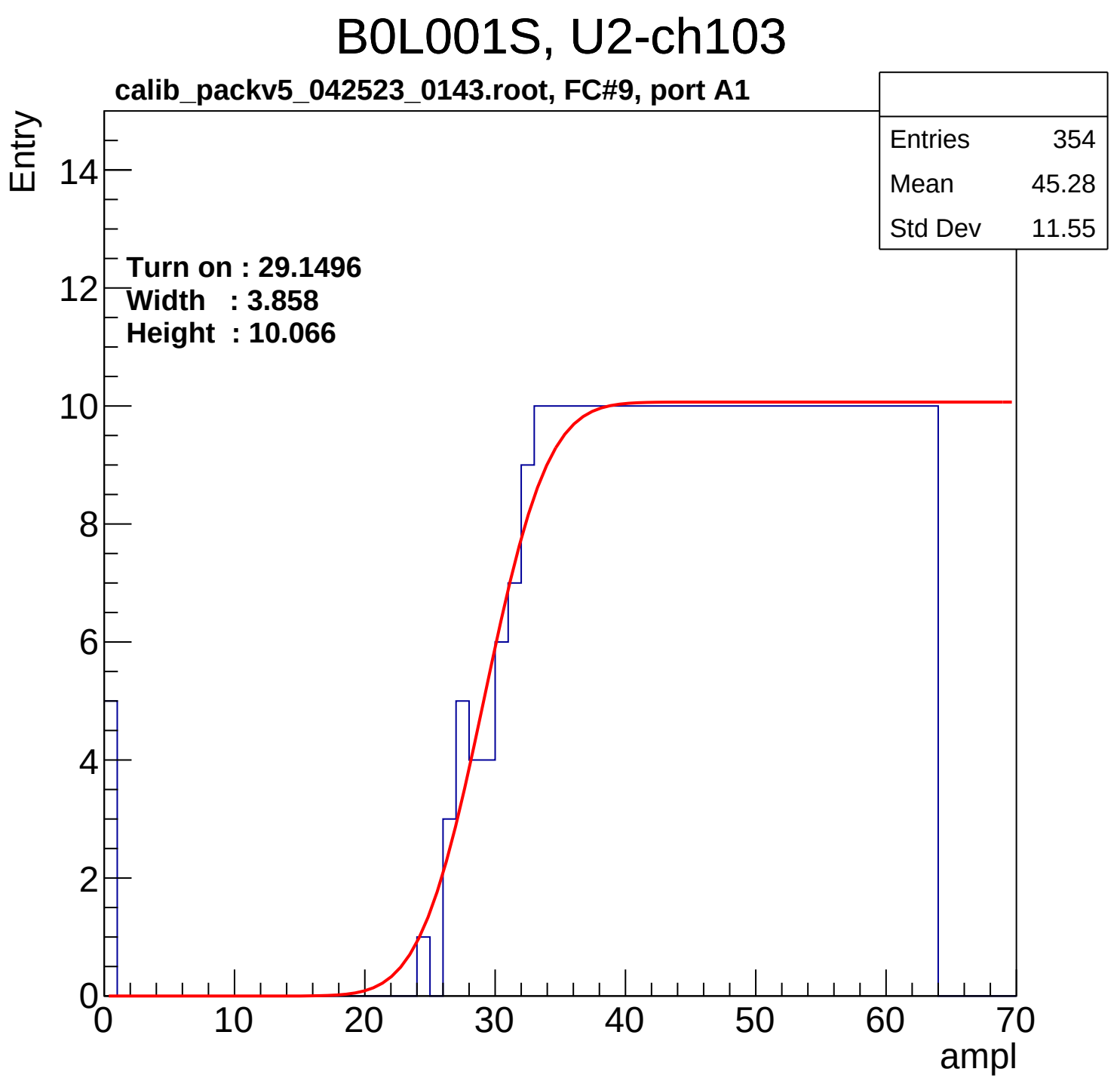
B0L001S, U2-ch103
calib_packv5_042523_0143.root, FC#9, port A1
Entries 354
Mean 45.28
Std Dev 11.55
Turn on : 29.1496
Width : 3.858
Height : 10.066
Entry
ampl
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0
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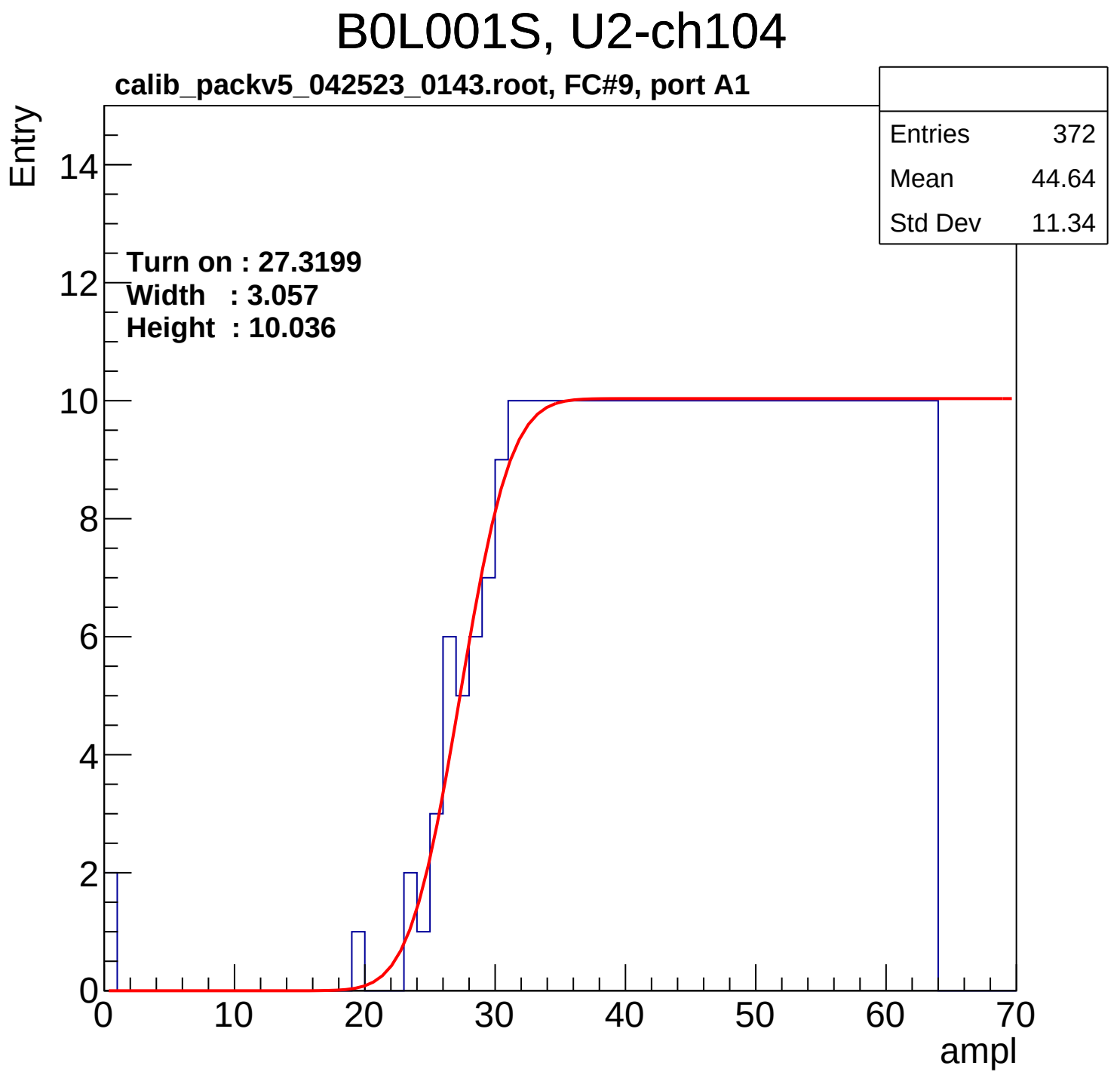
B0L001S, U2-ch104
calib_packv5_042523_0143.root, FC#9, port A1
Entries 372
Mean 44.64
Std Dev 11.34
Turn on : 27.3199
Width : 3.057
Height : 10.036
Entry
ampl
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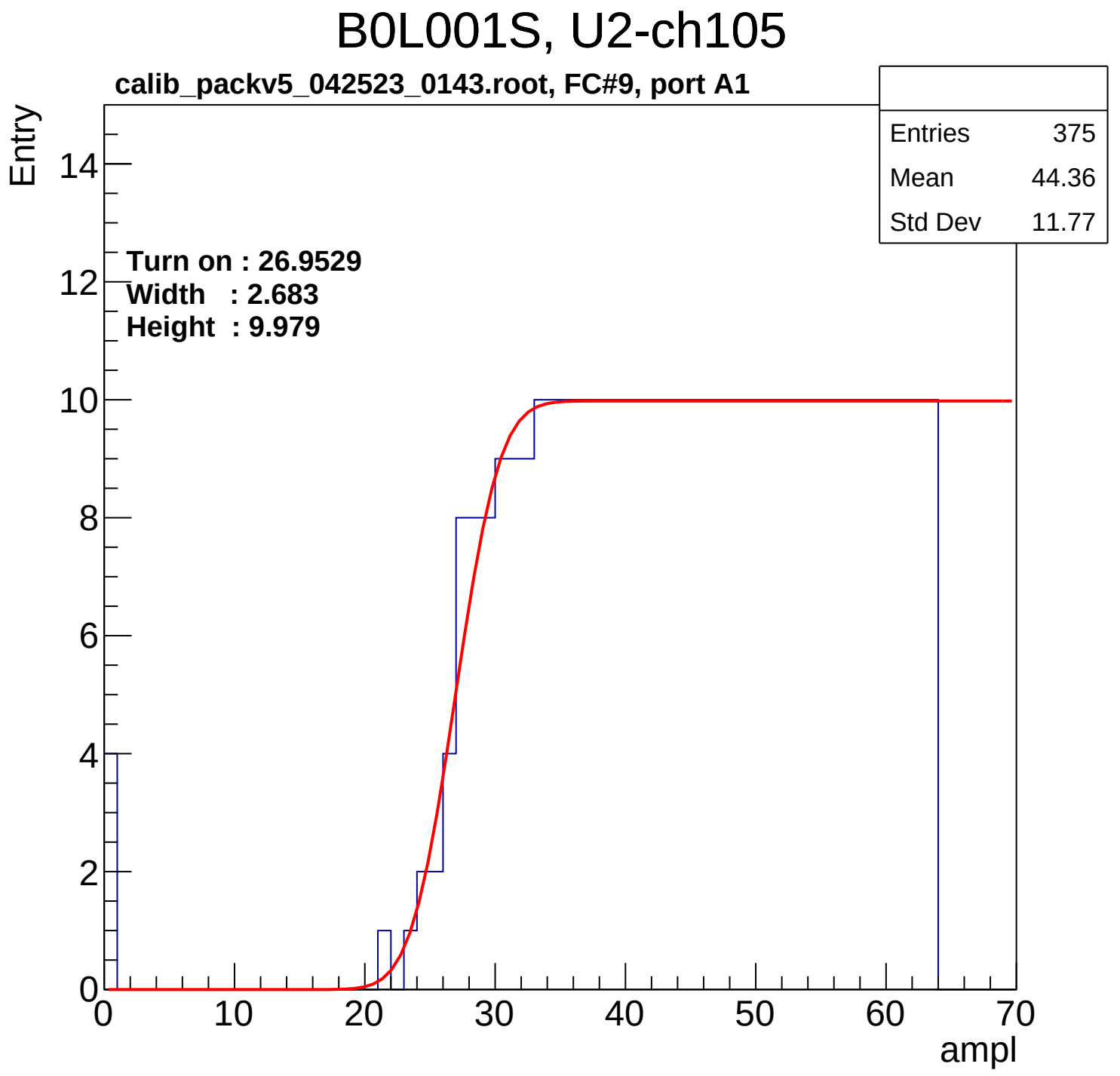
B0L001S, U2-ch105
calib_packv5_042523_0143.root, FC#9, port A1
Entries 375
Mean 44.36
Std Dev 11.77
Turn on : 26.9529
Width : 2.683
Height : 9.979
Entry
ampl
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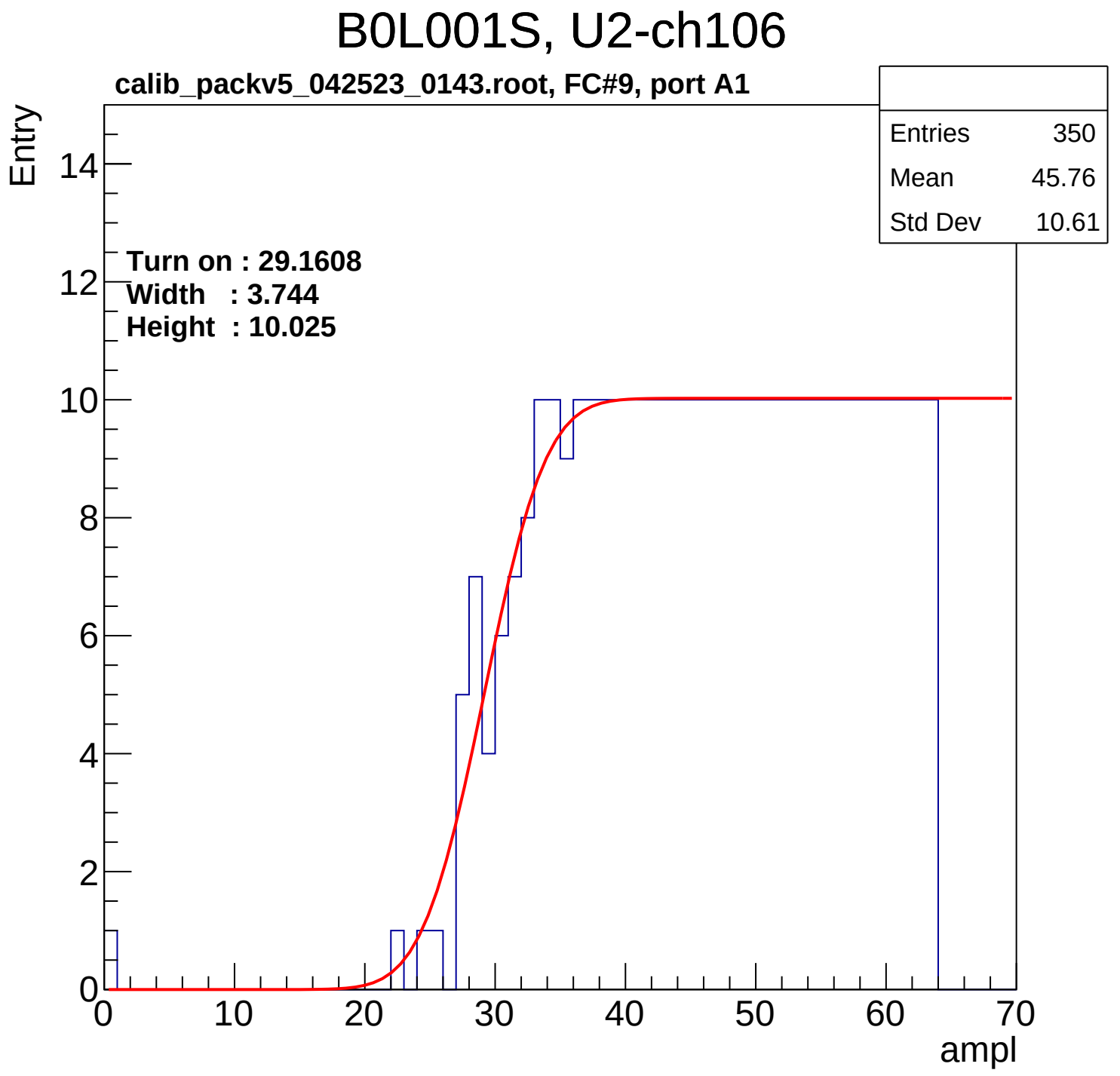
B0L001S, U2-ch106
calib_packv5_042523_0143.root, FC#9, port A1
Entries 350
Mean 45.76
Std Dev 10.61
Turn on : 29.1608
Width : 3.744
Height : 10.025
Entry
ampl
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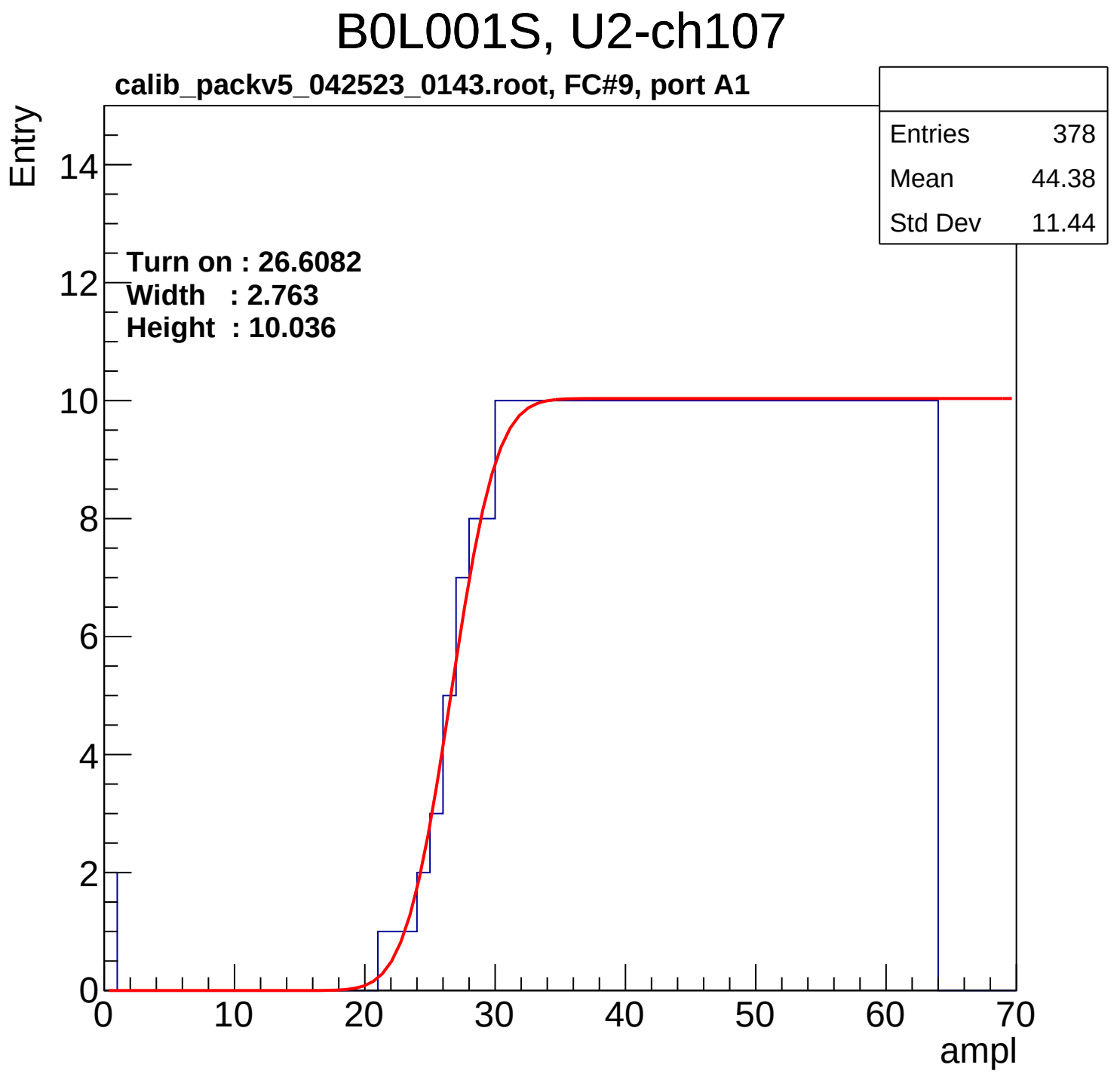
B0L001S, U2-ch107
calib_packv5_042523_0143.root, FC#9, port A1
Entries 378
Mean 44.38
Std Dev 11.44
Turn on : 26.6082
Width : 2.763
Height : 10.036
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ampl
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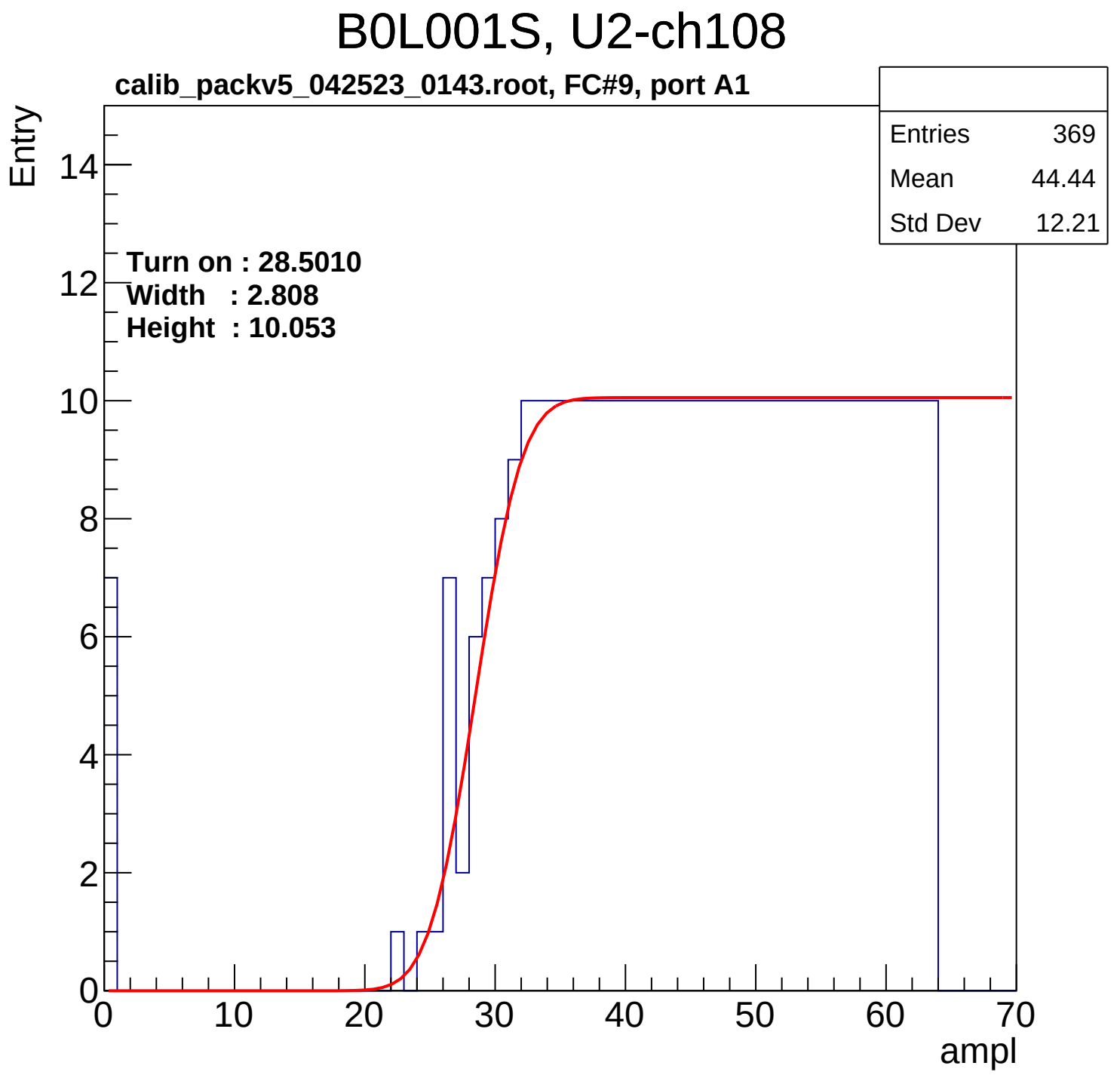
B0L001S, U2-ch108
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.44
Std Dev 12.21
Turn on : 28.5010
Width : 2.808
Height : 10.053
Entry
ampl
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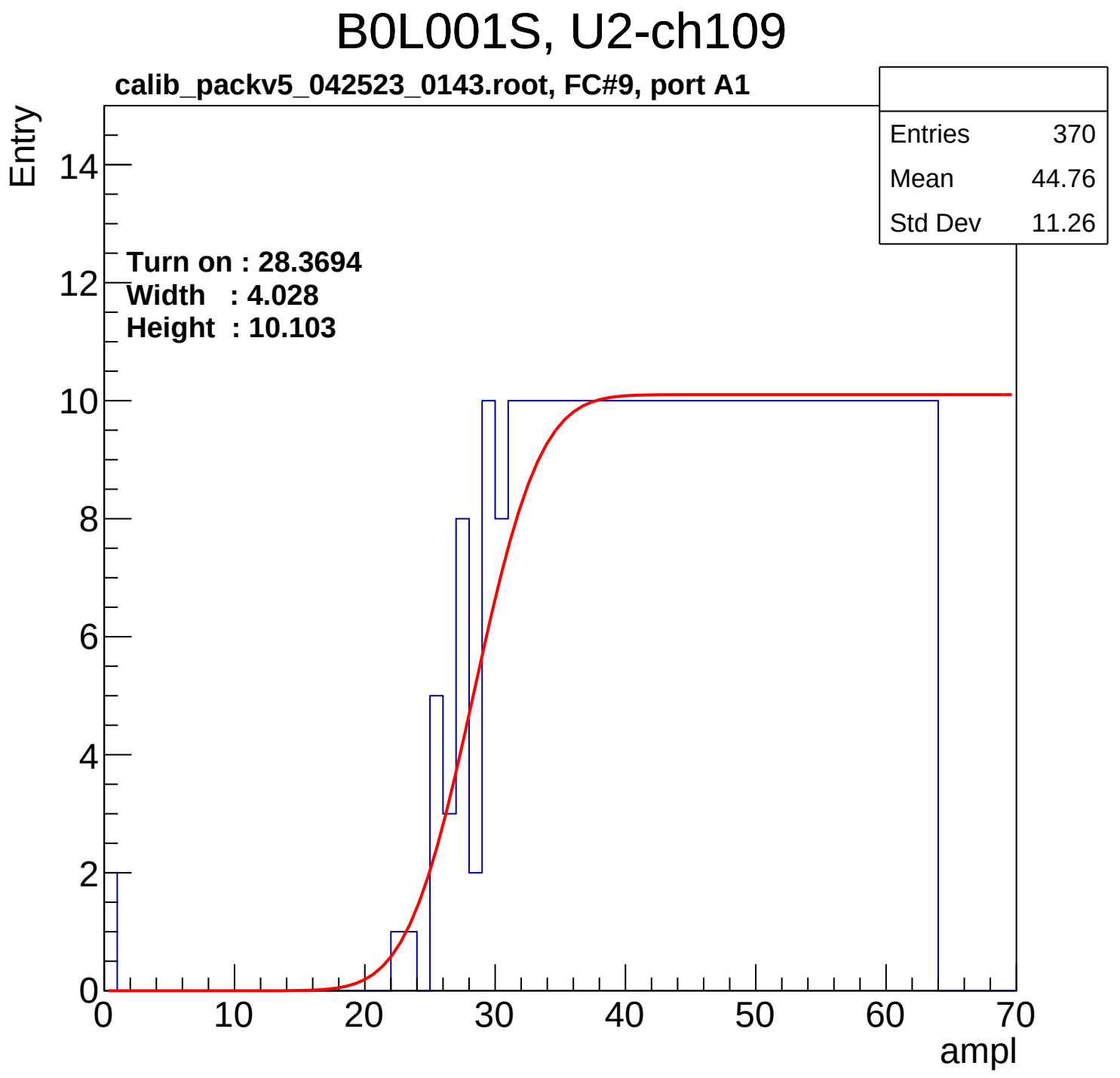
B0L001S, U2-ch109
calib_packv5_042523_0143.root, FC#9, port A1
Entries 370
Mean 44.76
Std Dev 11.26
Turn on : 28.3694
Width : 4.028
Height : 10.103
Entry
ampl
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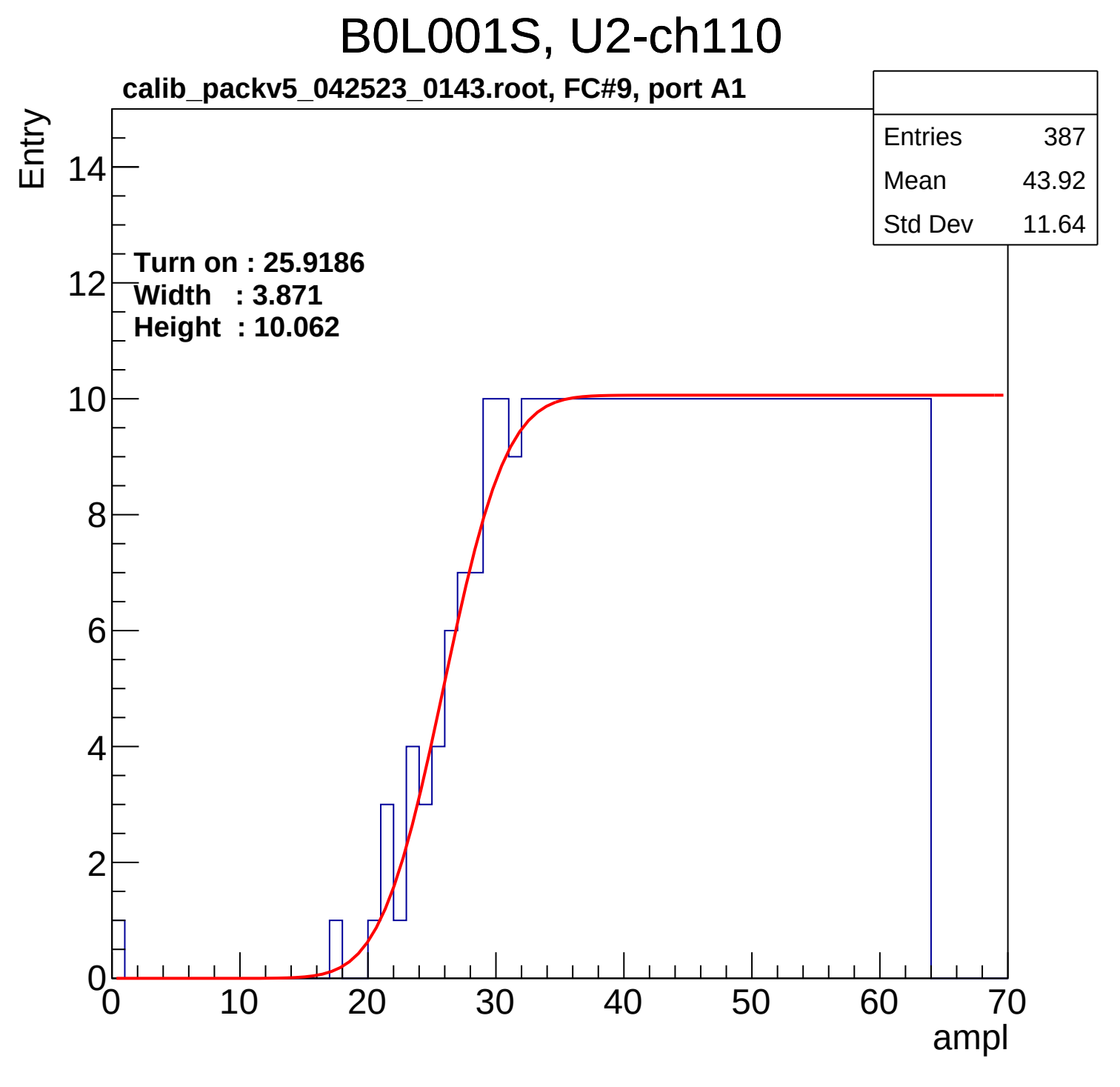
B0L001S, U2-ch110
calib_packv5_042523_0143.root, FC#9, port A1
Entries 387
Mean 43.92
Std Dev 11.64
Turn on : 25.9186
Width : 3.871
Height : 10.062
Entry
ampl
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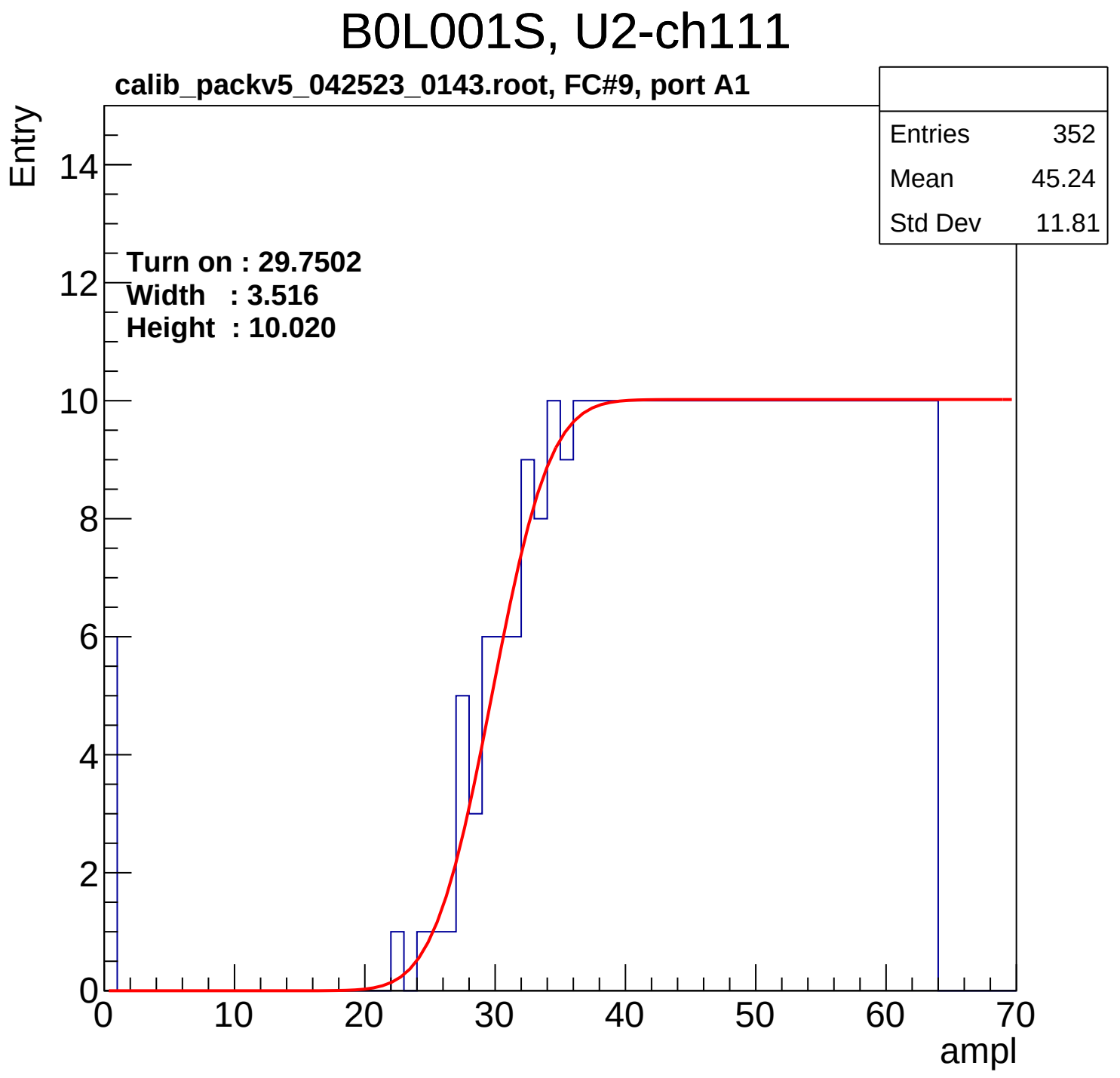
B0L001S, U2-ch111
calib_packv5_042523_0143.root, FC#9, port A1
Entries 352
Mean 45.24
Std Dev 11.81
Turn on : 29.7502
Width : 3.516
Height : 10.020
Entry
ampl
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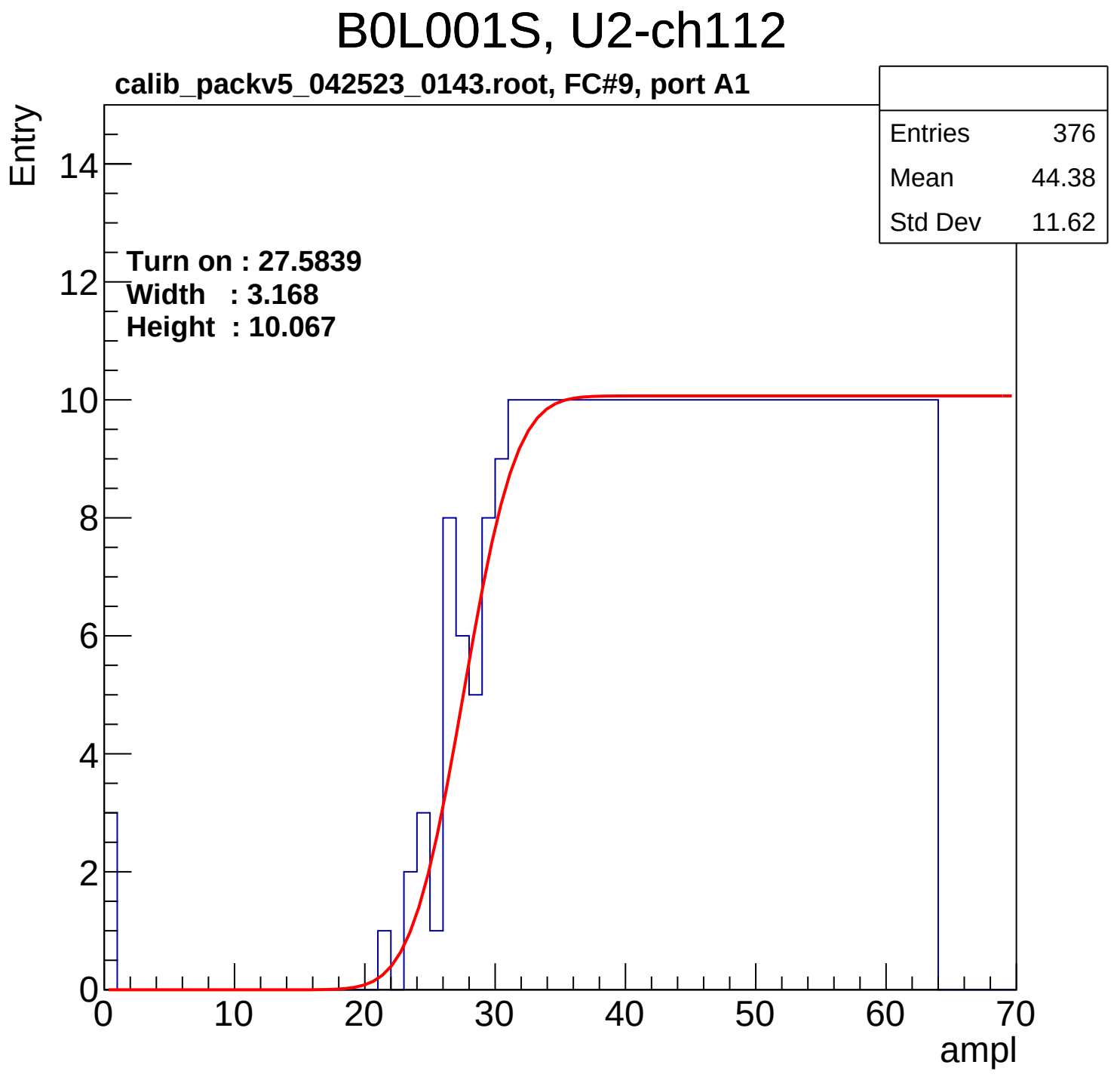
B0L001S, U2-ch112
calib_packv5_042523_0143.root, FC#9, port A1
Entries 376
Mean 44.38
Std Dev 11.62
Turn on : 27.5839
Width : 3.168
Height : 10.067
Entry
ampl
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6
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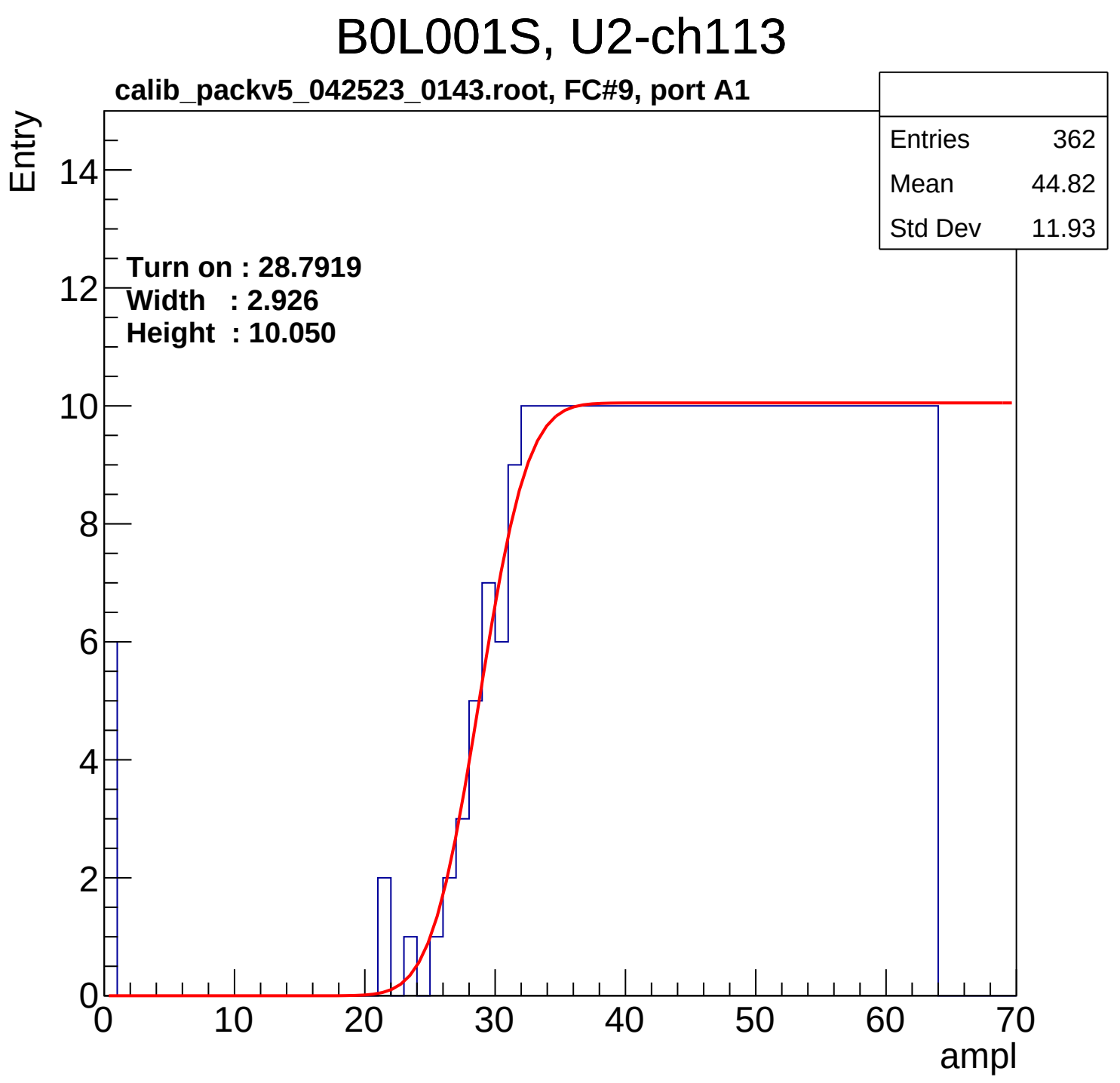
B0L001S, U2-ch113
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 44.82
Std Dev 11.93
Turn on : 28.7919
Width : 2.926
Height : 10.050
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ampl
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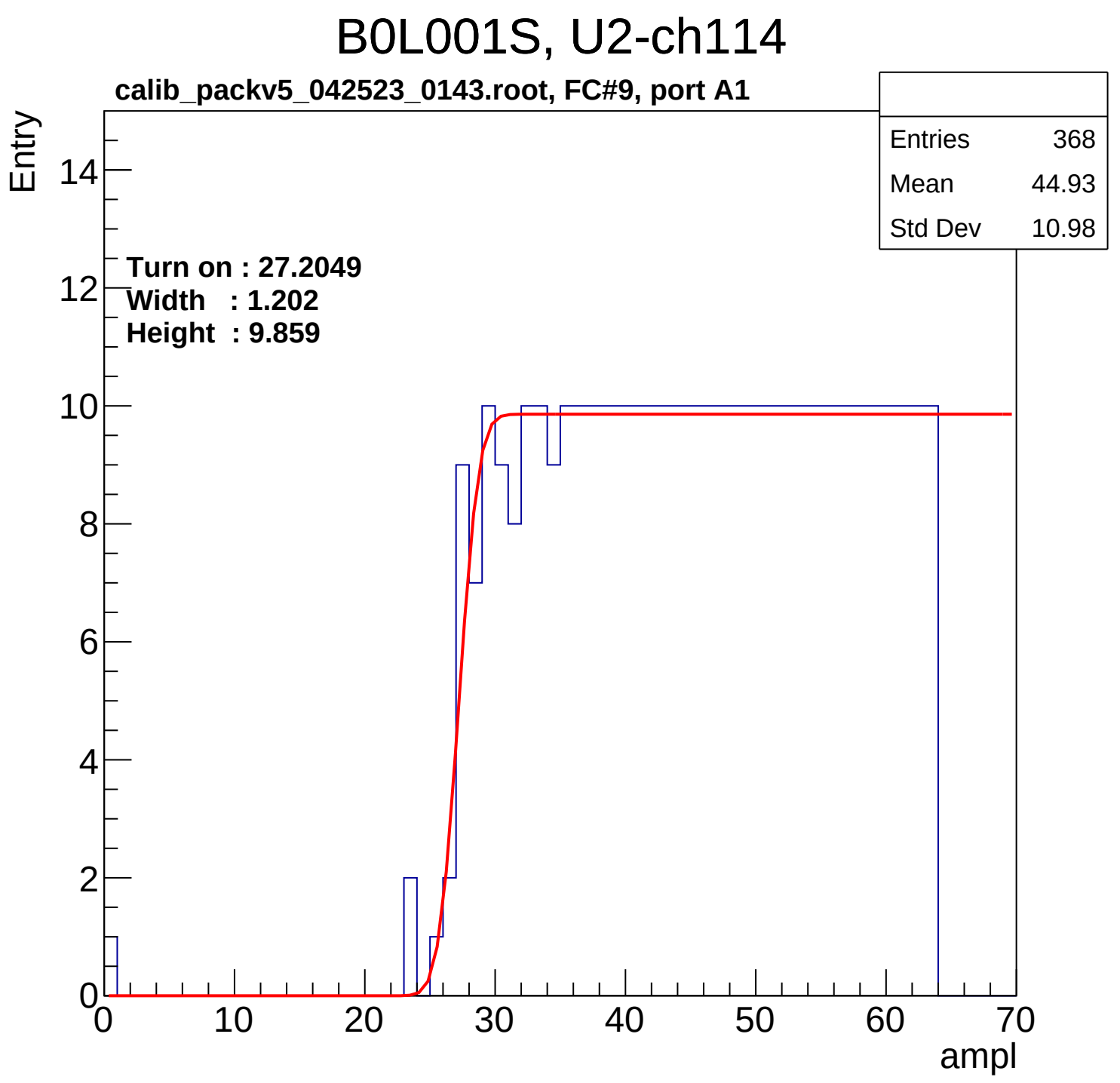
B0L001S, U2-ch114
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.93
Std Dev 10.98
Turn on : 27.2049
Width : 1.202
Height : 9.859
Entry
ampl
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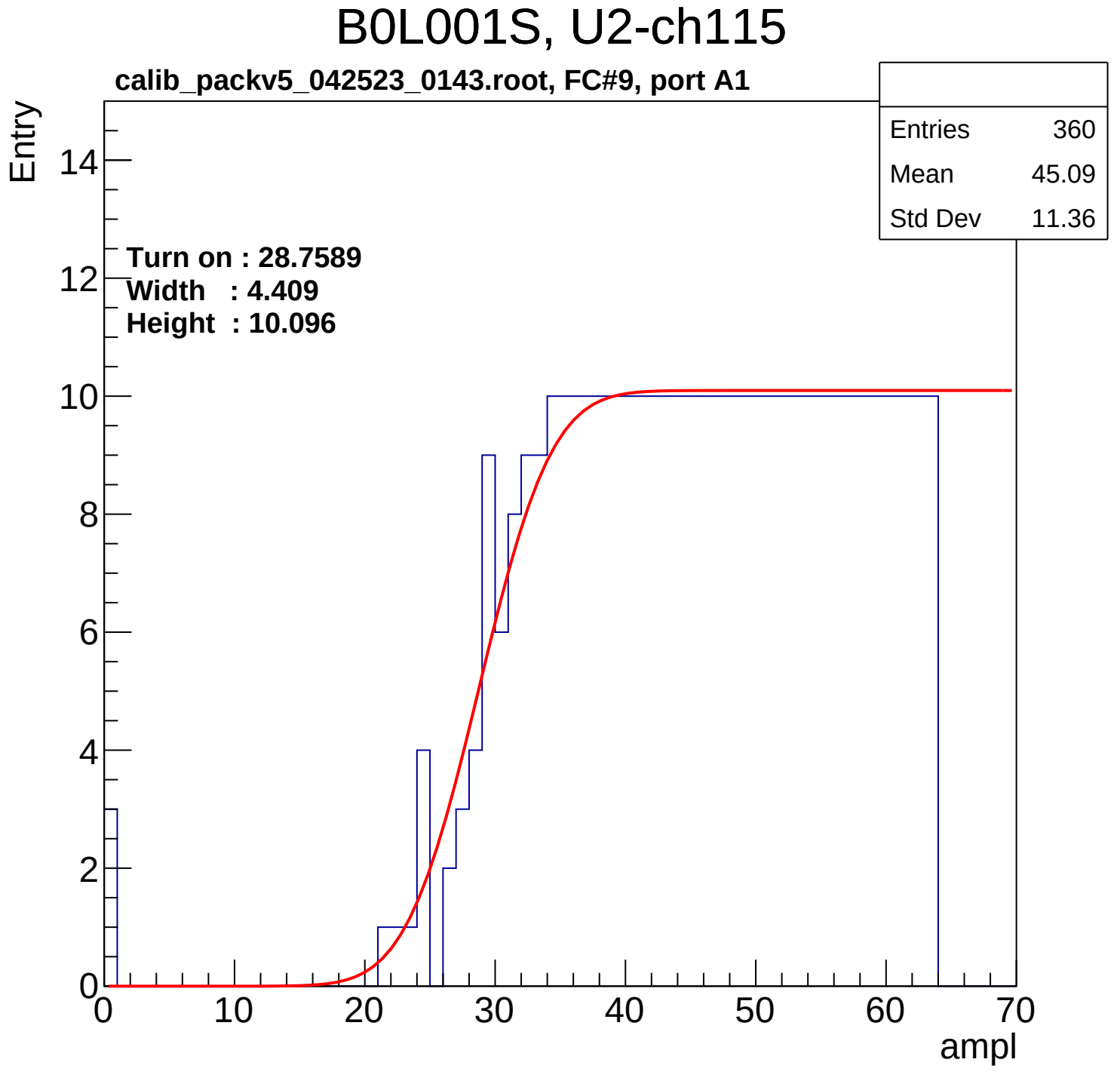
B0L001S, U2-ch115
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 45.09
Std Dev 11.36
Turn on : 28.7589
Width : 4.409
Height : 10.096
Entry
ampl
0
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4
6
8
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12
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10
20
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40
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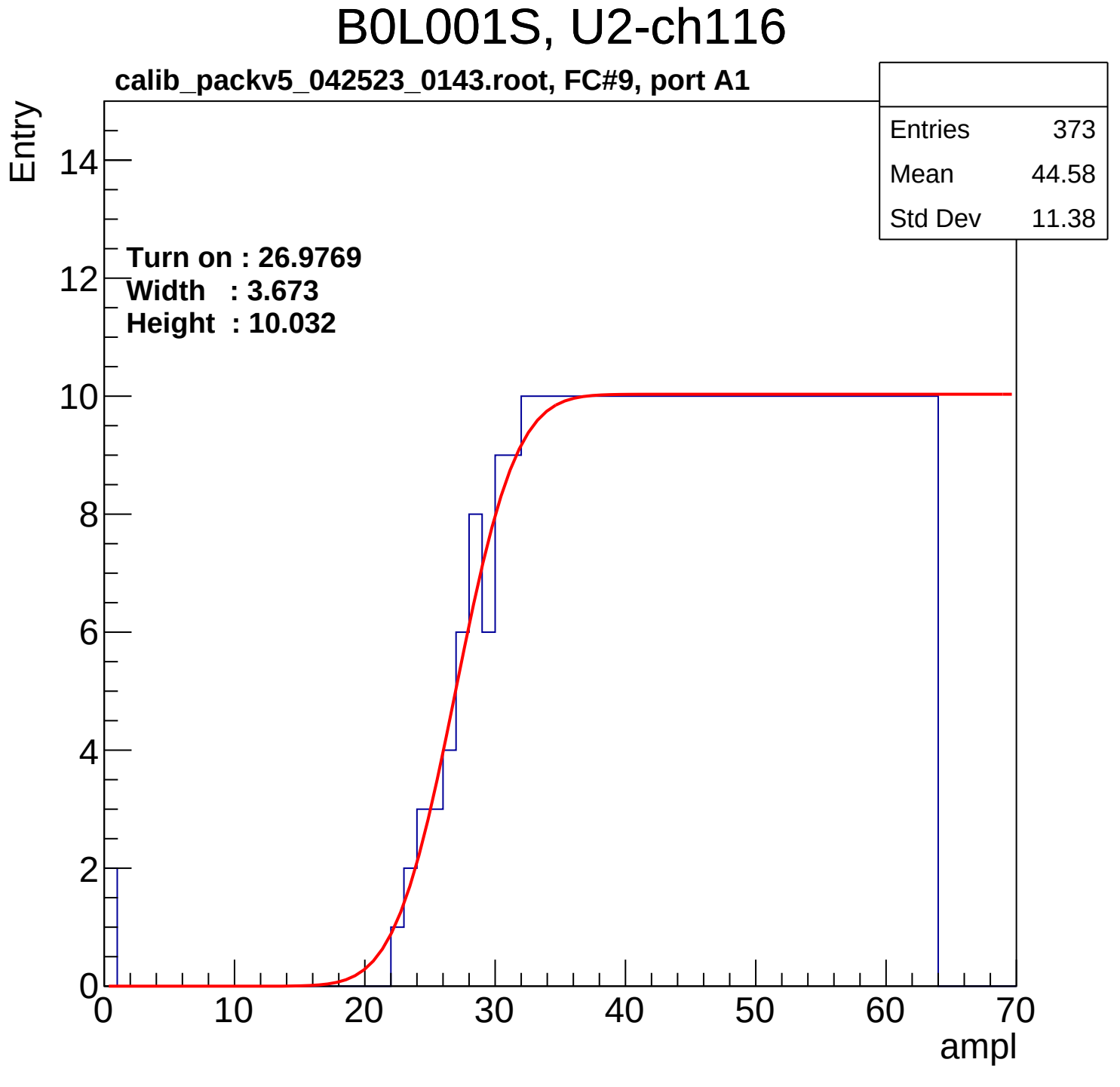
B0L001S, U2-ch116
calib_packv5_042523_0143.root, FC#9, port A1
Entries 373
Mean 44.58
Std Dev 11.38
Turn on : 26.9769
Width : 3.673
Height : 10.032
Entry
ampl
0
2
4
6
8
10
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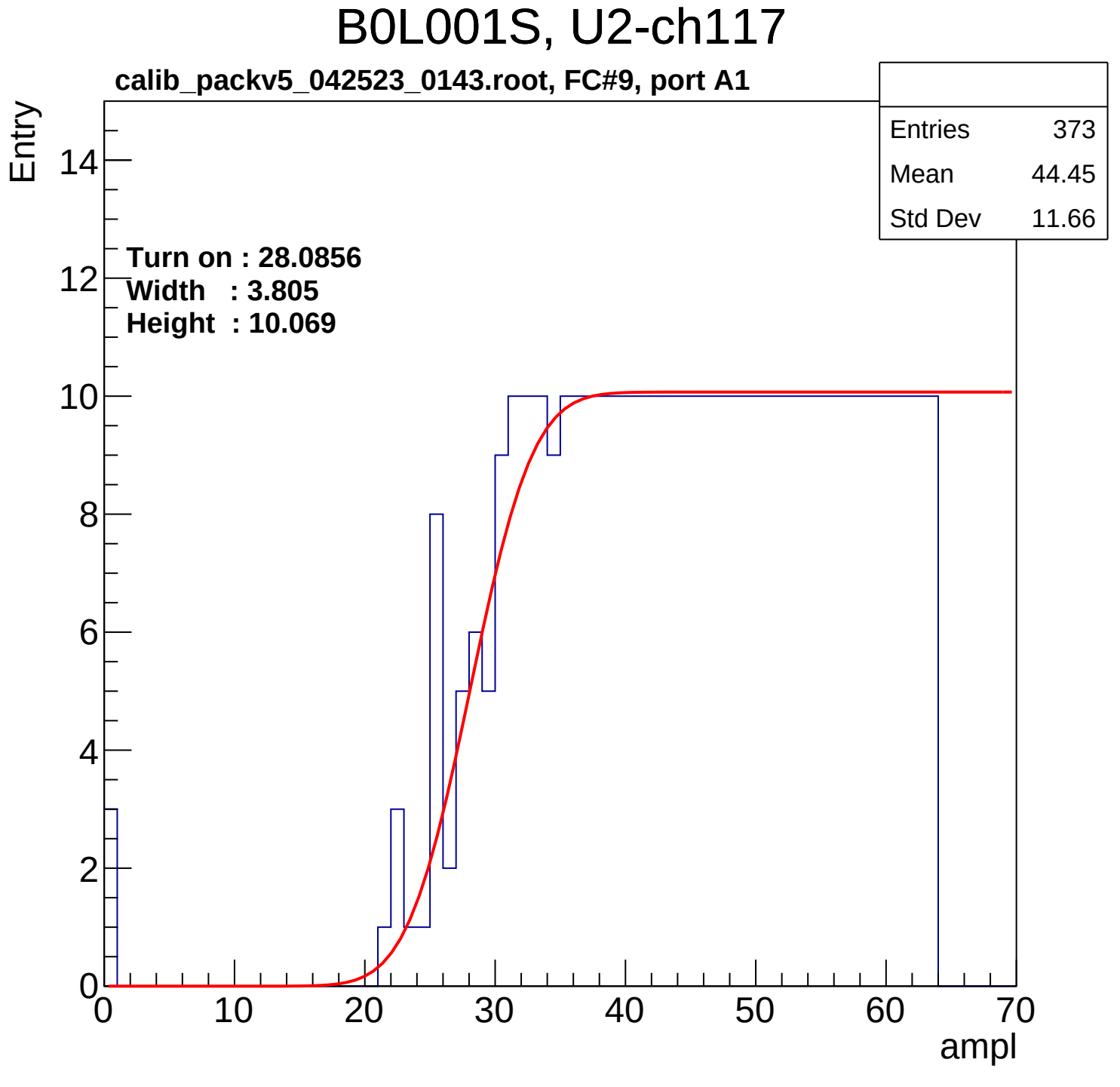
B0L001S, U2-ch117
calib_packv5_042523_0143.root, FC#9, port A1
Entries 373
Mean 44.45
Std Dev 11.66
Turn on : 28.0856
Width : 3.805
Height : 10.069
Entry
ampl
0
2
4
6
8
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12
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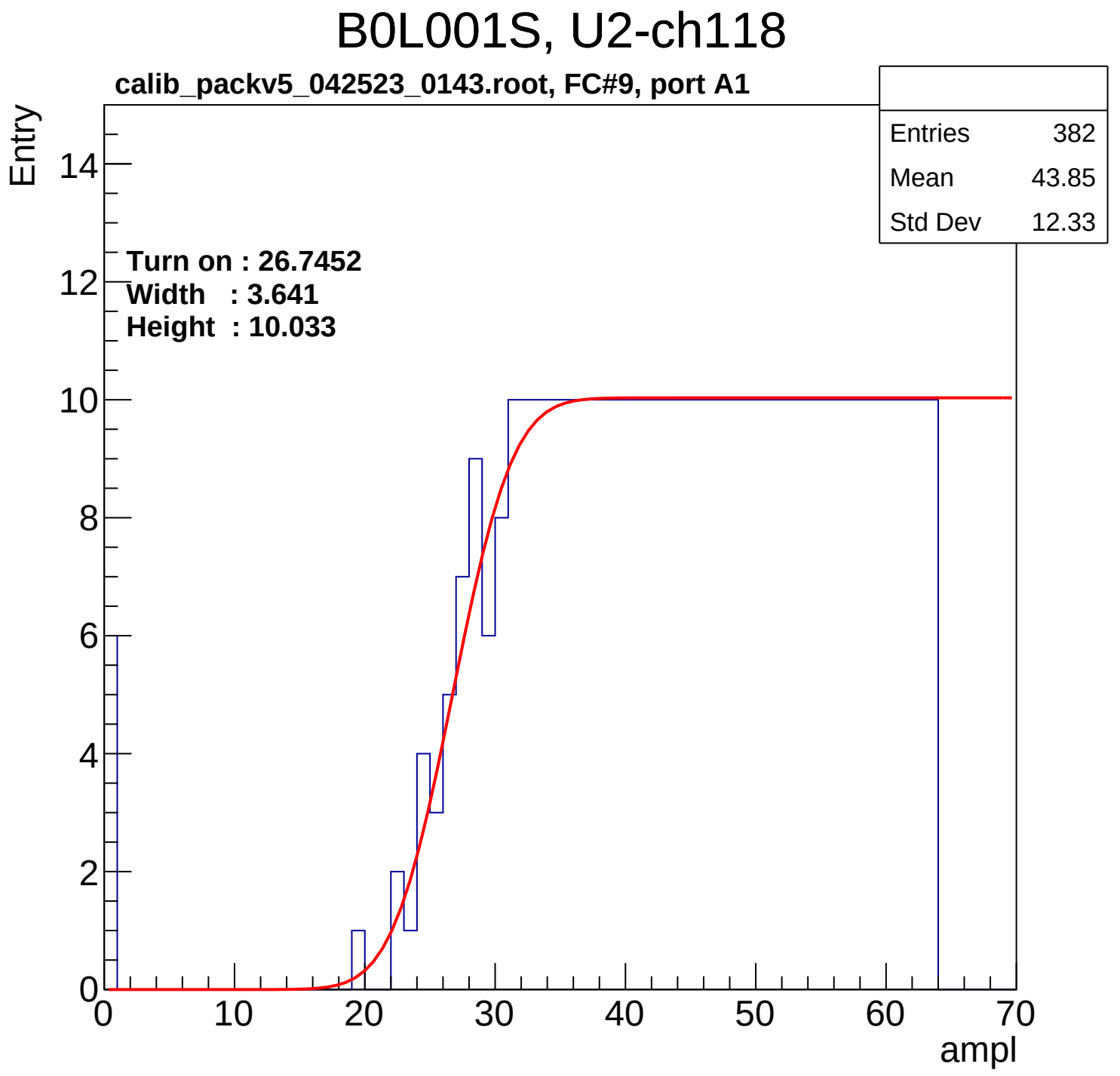
B0L001S, U2-ch118
calib_packv5_042523_0143.root, FC#9, port A1
Entries 382
Mean 43.85
Std Dev 12.33
Turn on : 26.7452
Width : 3.641
Height : 10.033
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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60
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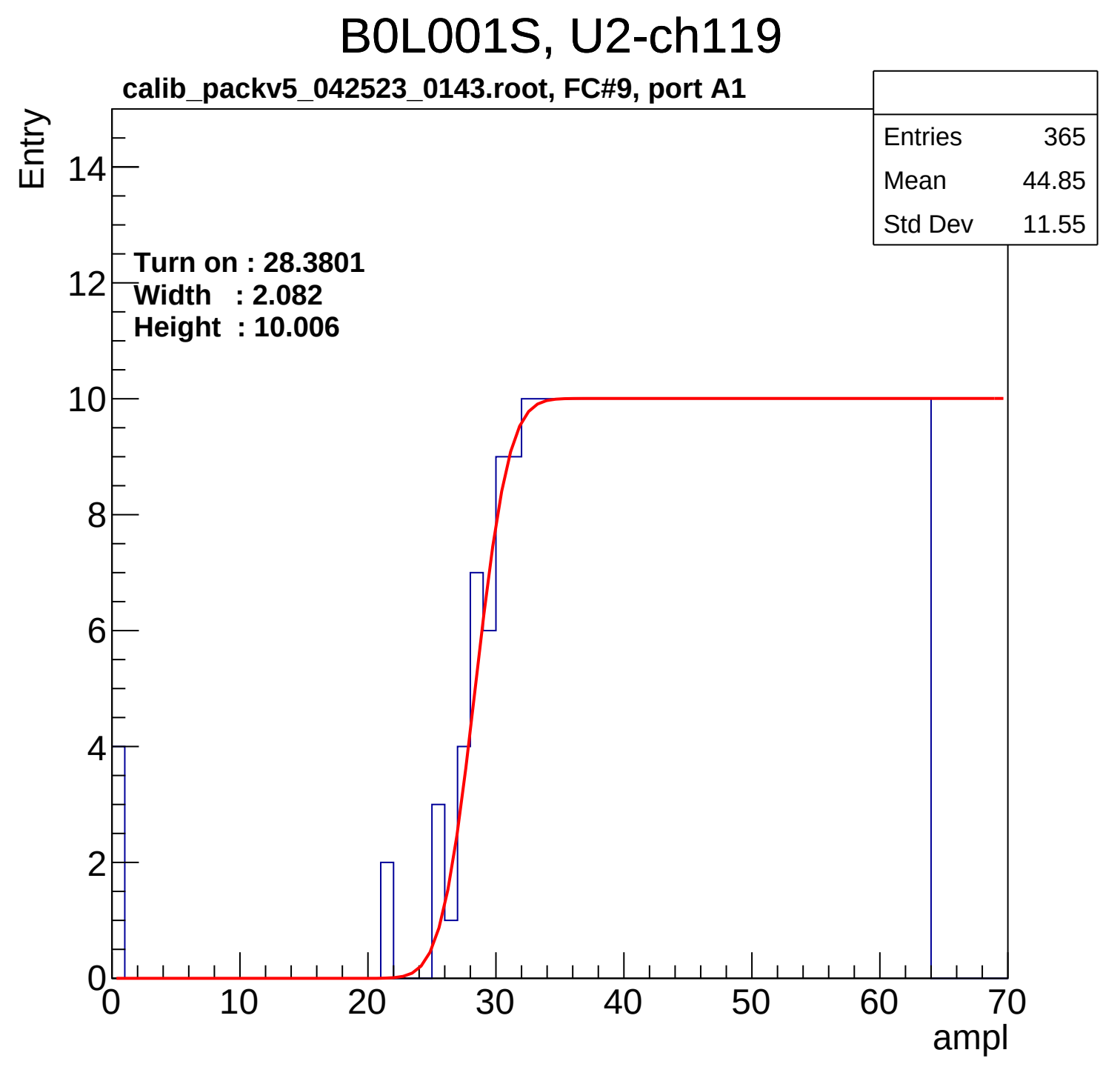
B0L001S, U2-ch119
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 44.85
Std Dev 11.55
Turn on : 28.3801
Width : 2.082
Height : 10.006
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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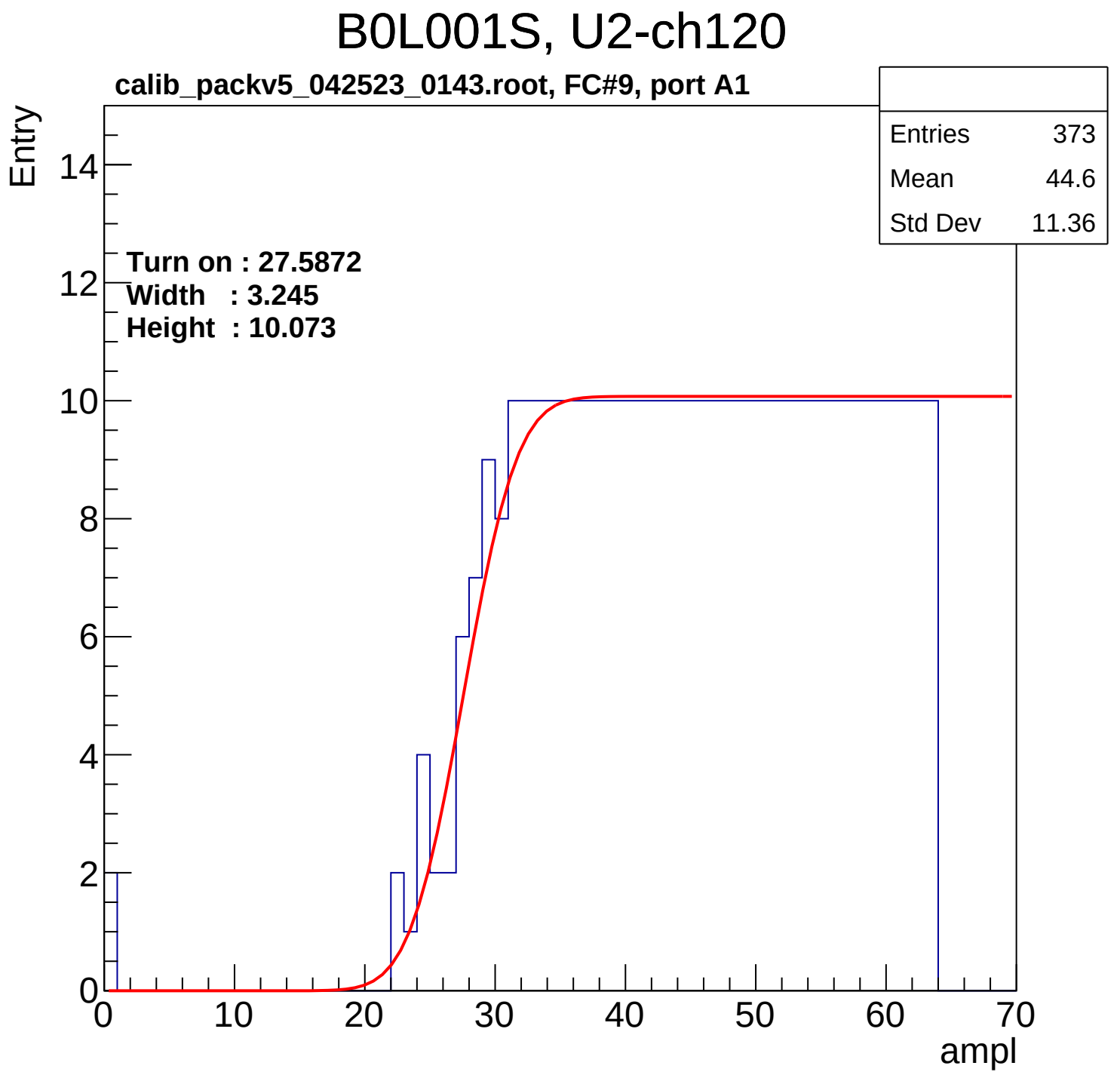
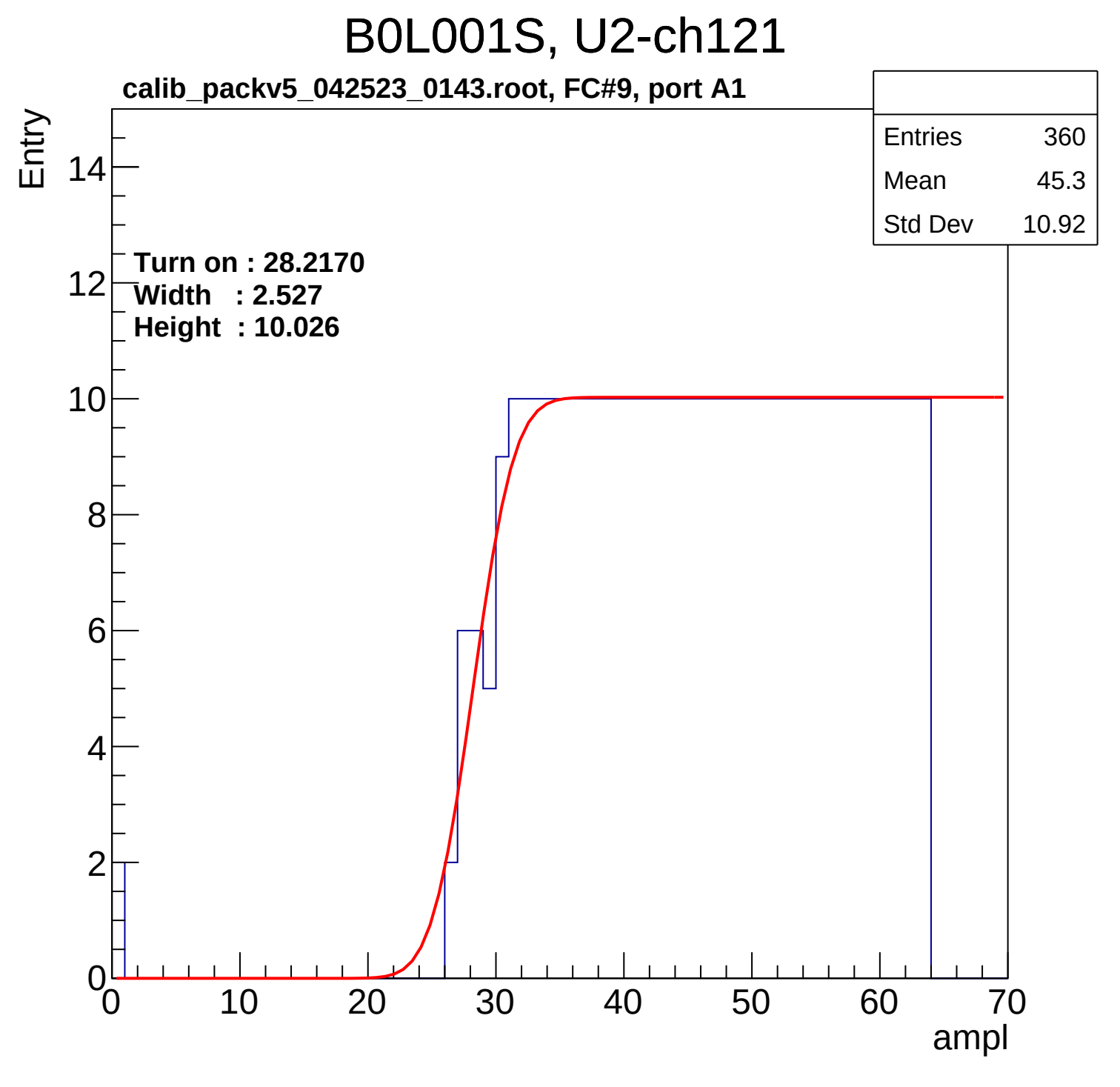
40
50
60
70


B0L001S, U2-ch120
calib_packv5_042523_0143.root, FC#9, port A1
Entries 373
Mean 44.6
Std Dev 11.36
Turn on : 27.5872
Width : 3.245
Height : 10.073
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U2-ch121
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 45.3
Std Dev 10.92
Turn on : 28.2170
Width : 2.527
Height : 10.026
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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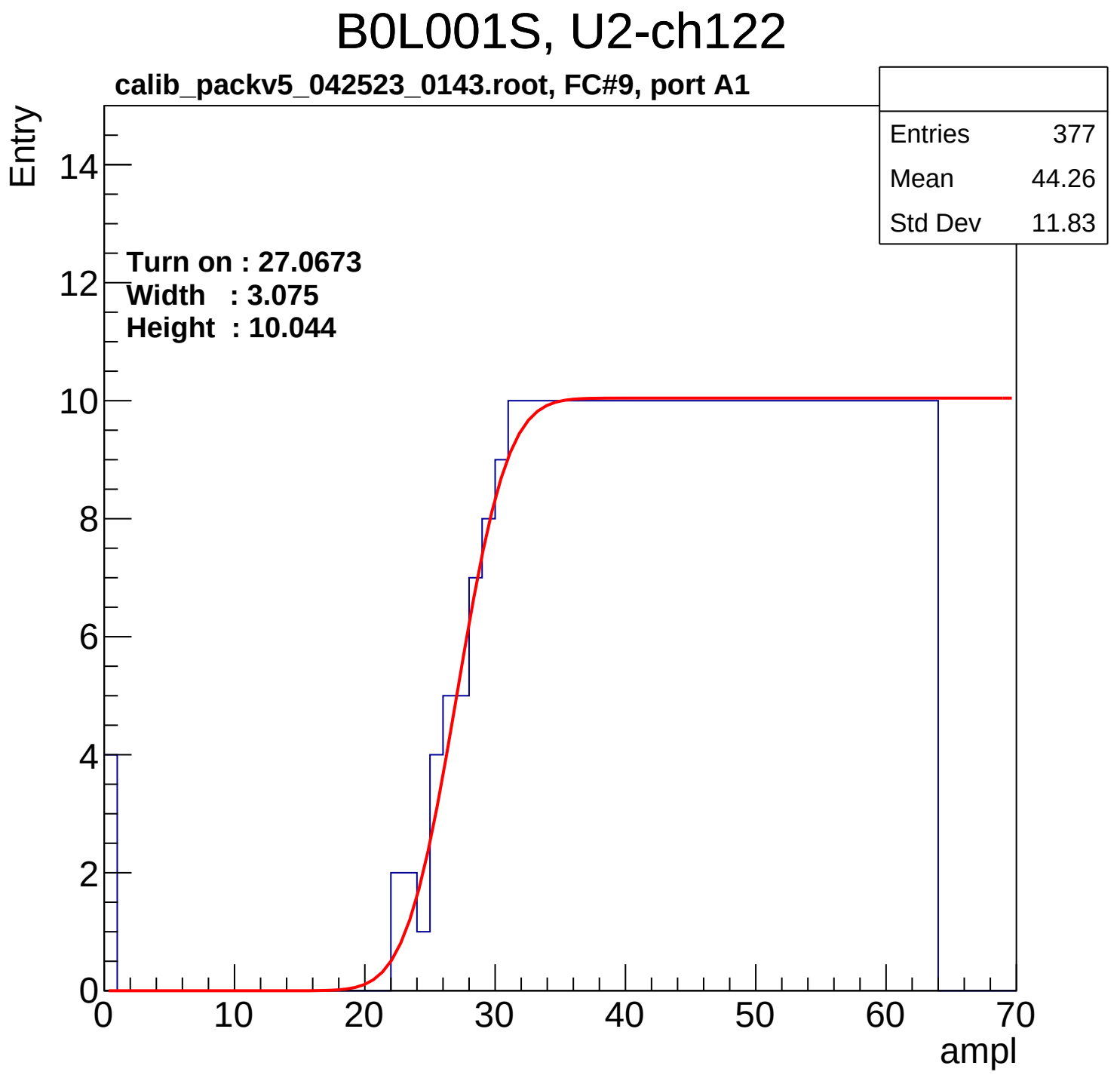
B0L001S, U2-ch122
calib_packv5_042523_0143.root, FC#9, port A1
Entries 377
Mean 44.26
Std Dev 11.83
Turn on : 27.0673
Width : 3.075
Height : 10.044
Entry
ampl
0
2
4
6
8
10
12
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0
10
20
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40
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60
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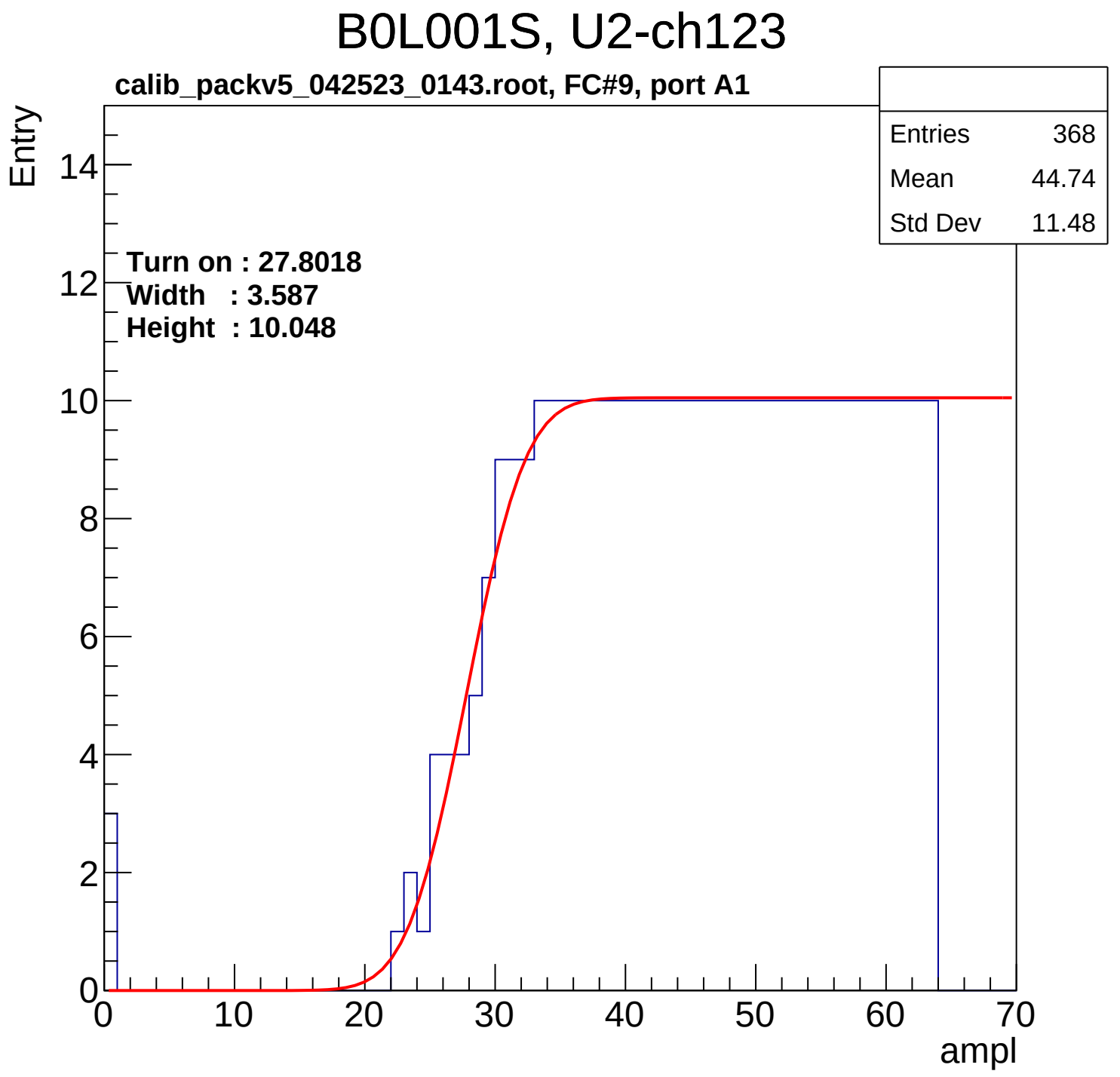
B0L001S, U2-ch123
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.74
Std Dev 11.48
Turn on : 27.8018
Width : 3.587
Height : 10.048
Entry
ampl
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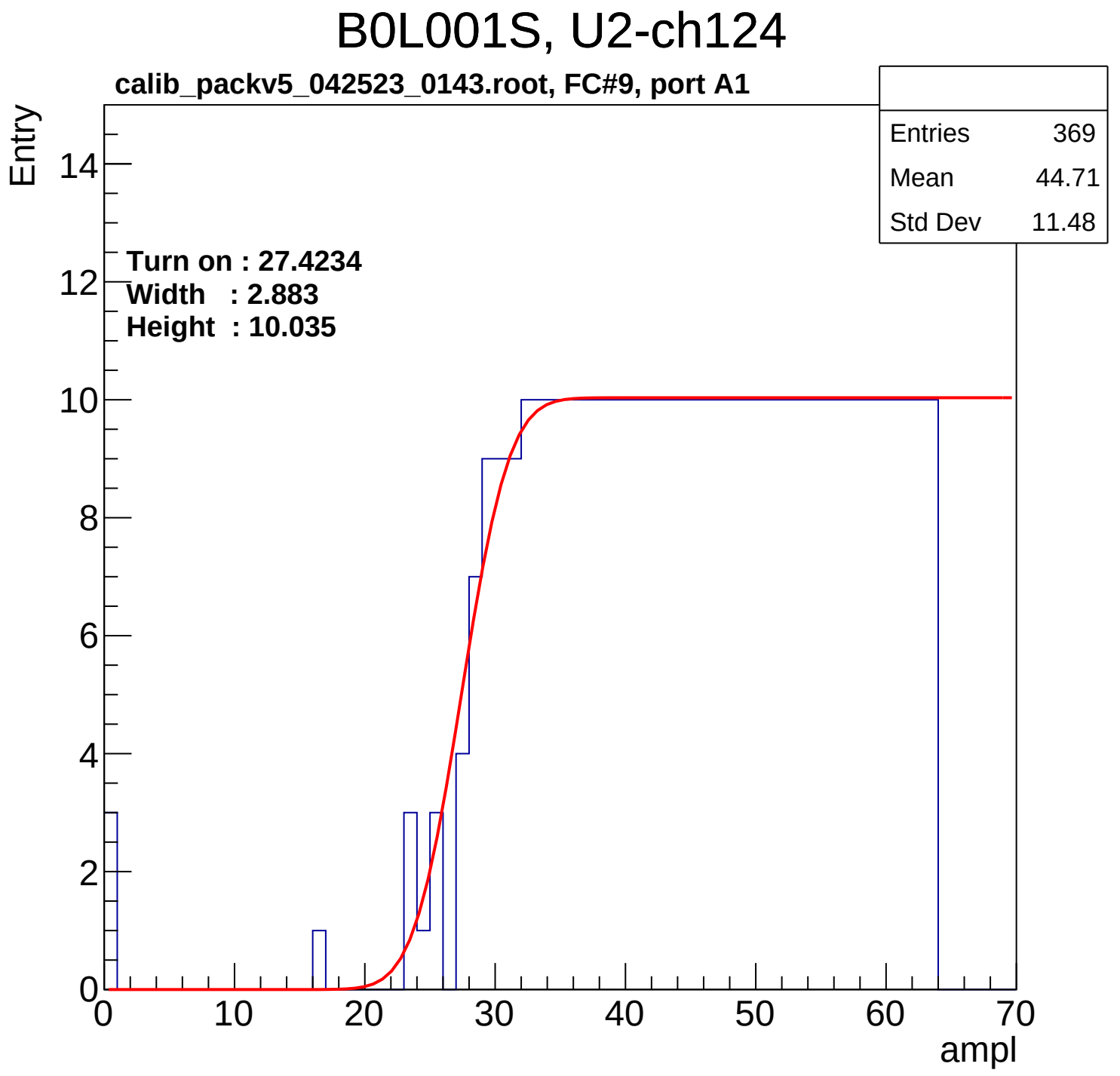
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U2-ch124
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.71
Std Dev 11.48
Turn on : 27.4234
Width : 2.883
Height : 10.035
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
30
40
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60
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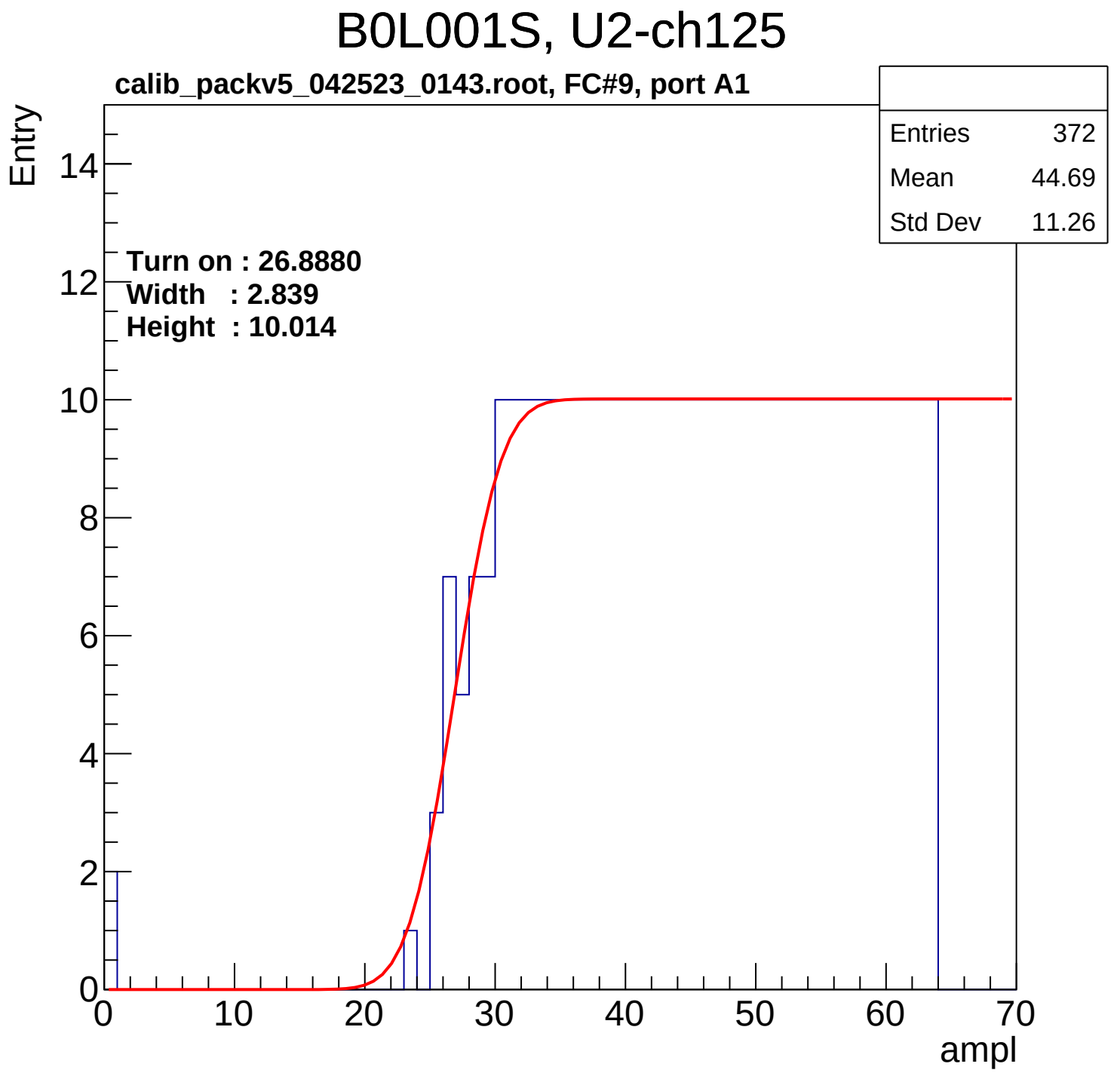
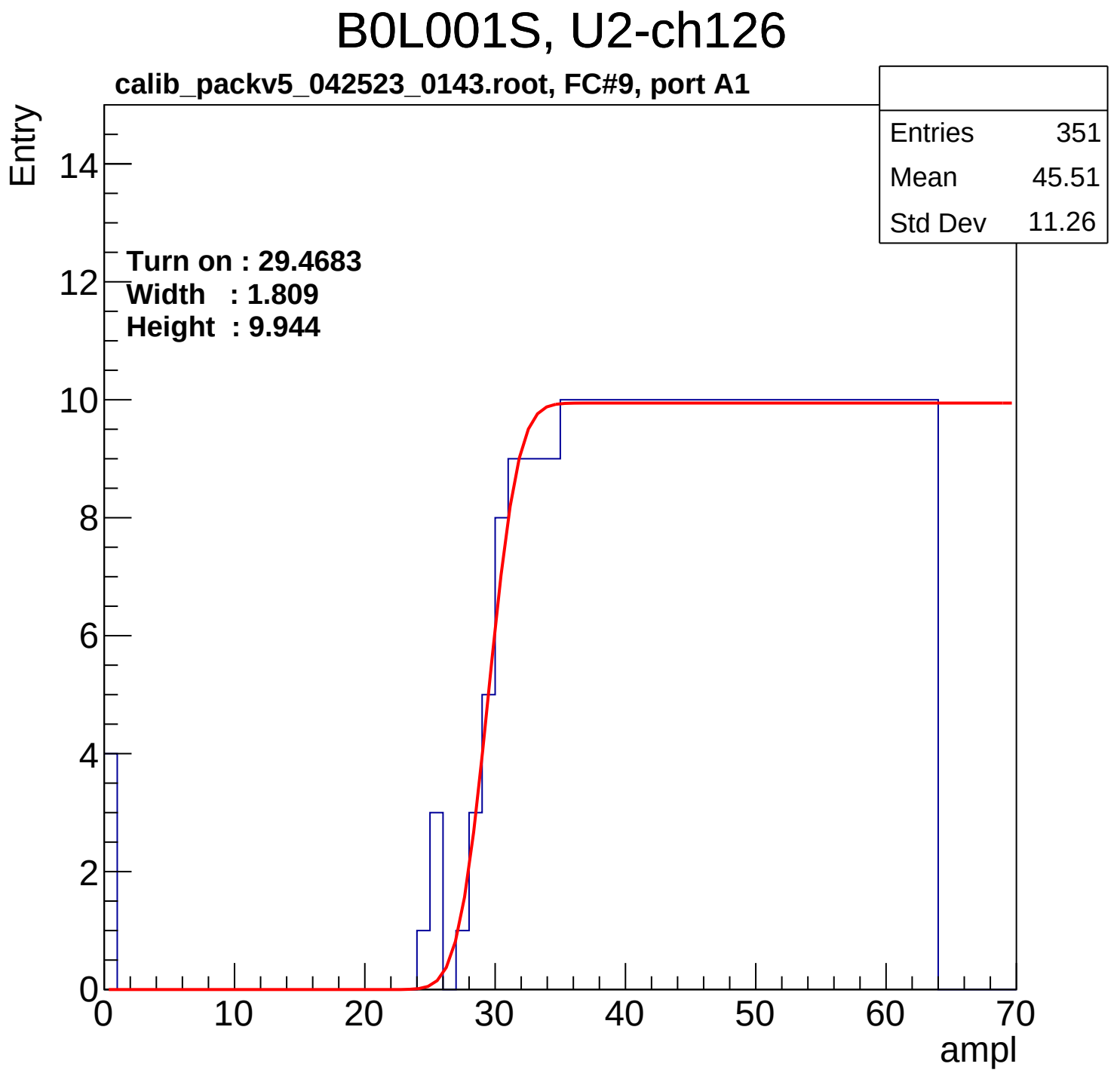

B0L001S, U2-ch125
calib_packv5_042523_0143.root, FC#9, port A1
Entries 372
Mean 44.69
Std Dev 11.26
Turn on : 26.8880
Width : 2.839
Height : 10.014
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U2-ch126
calib_packv5_042523_0143.root, FC#9, port A1
Entries 351
Mean 45.51
Std Dev 11.26
Turn on : 29.4683
Width : 1.809
Height : 9.944
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
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60
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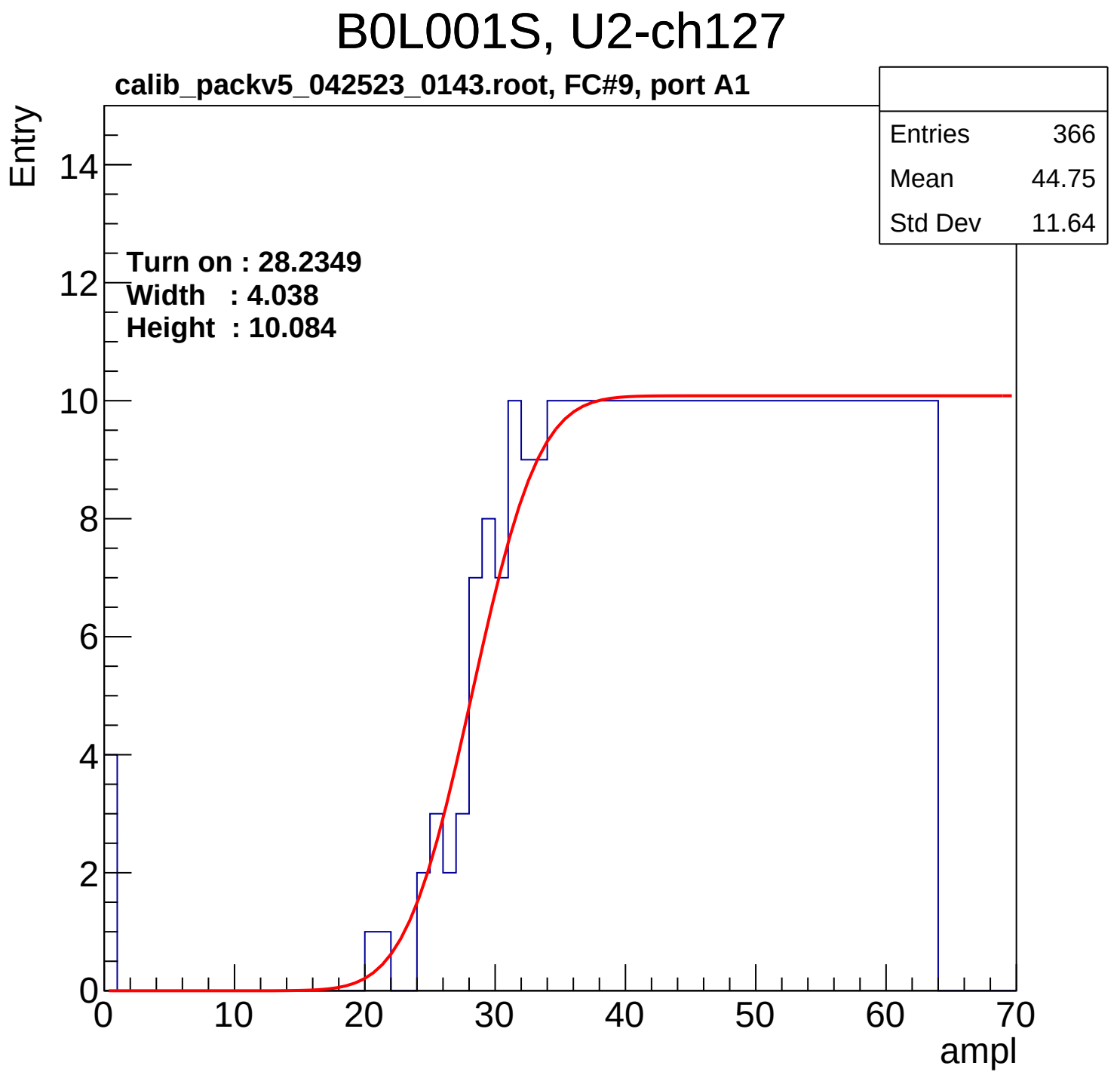
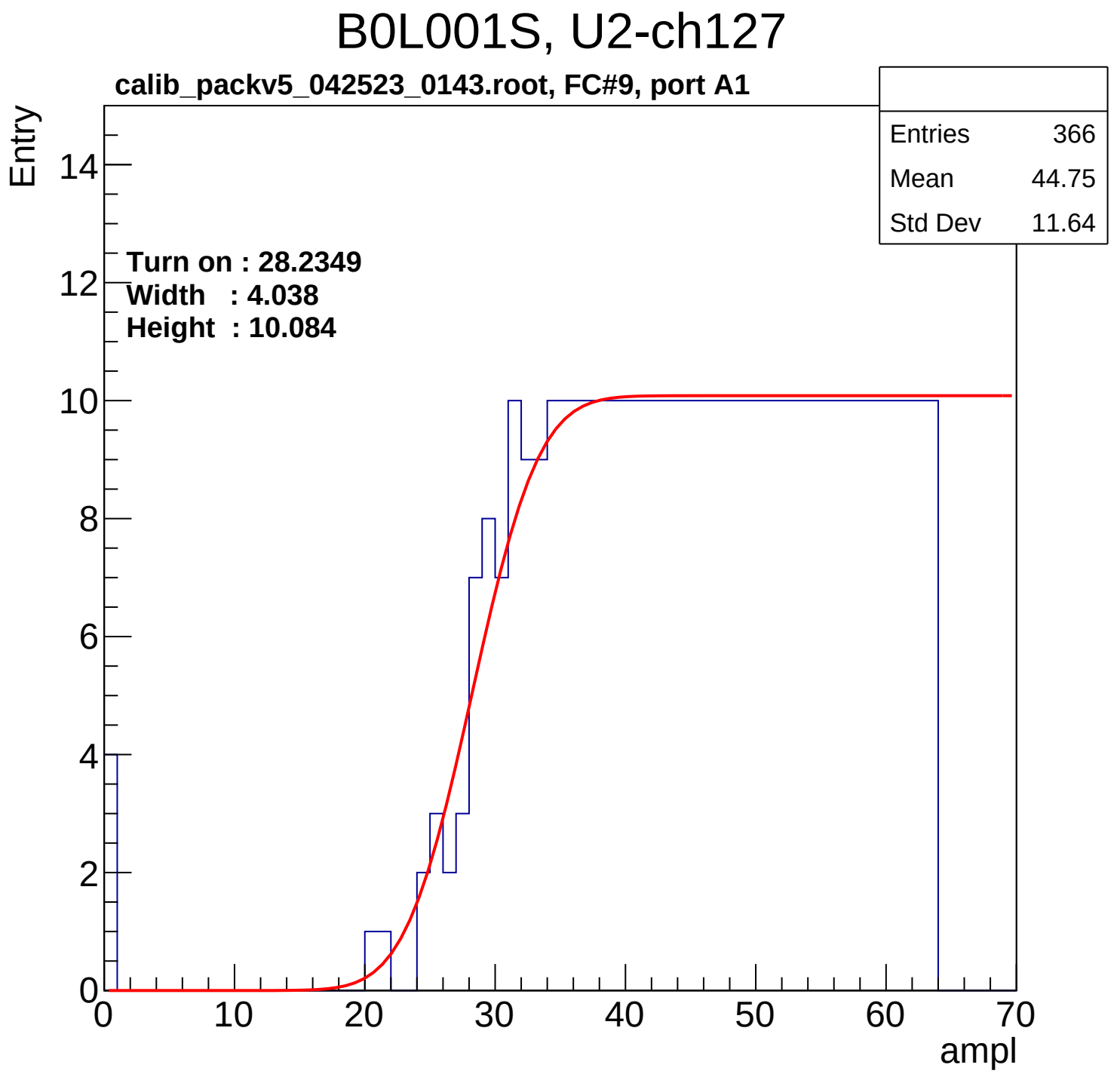

B0L001S, U2-ch127
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.75
Std Dev 11.64
Turn on : 28.2349
Width : 4.038
Height : 10.084
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U2-ch127
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.75
Std Dev 11.64
Turn on : 28.2349
Width : 4.038
Height : 10.084
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
30
40
50
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70