



# B0L001S, U2-ch0, adc0

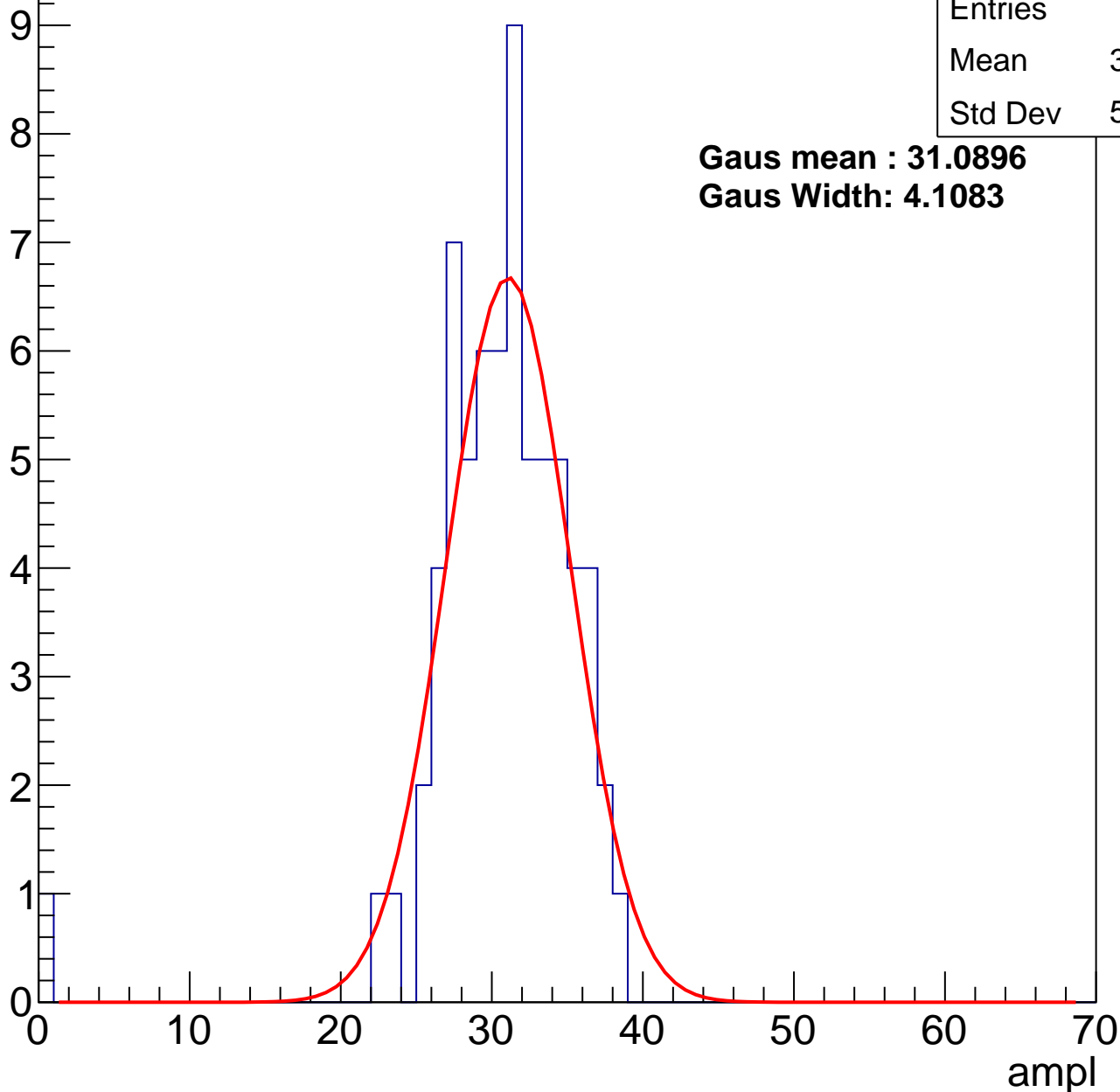
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 68    |
| Mean    | 30.18 |
| Std Dev | 5.107 |

**Gaus mean : 31.0896**

**Gaus Width: 4.1083**



# B0L001S, U2-ch0, adc1

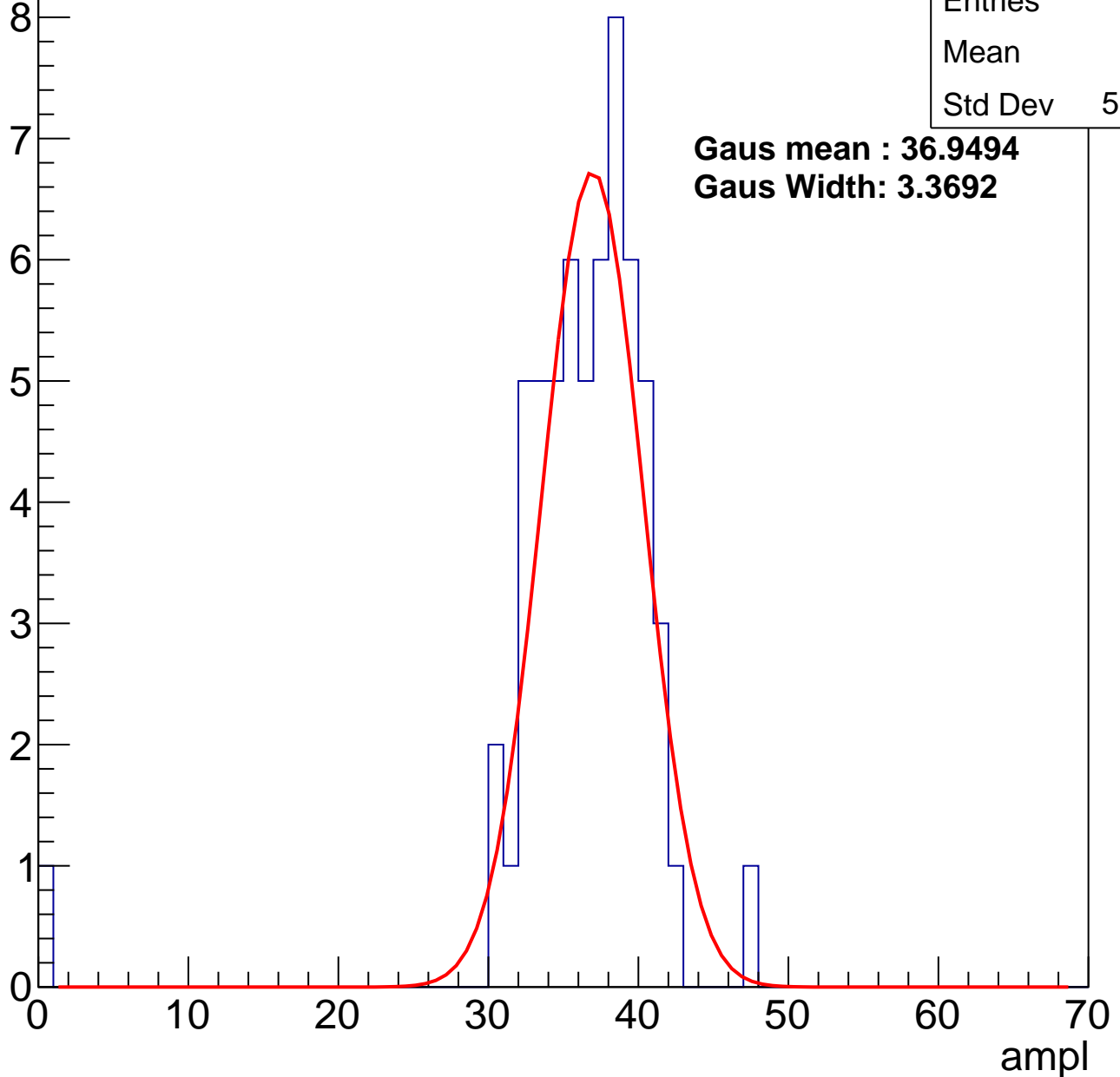
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 60    |
| Mean    | 35.8  |
| Std Dev | 5.694 |

**Gaus mean : 36.9494**

**Gaus Width: 3.3692**



# B0L001S, U2-ch0, adc2

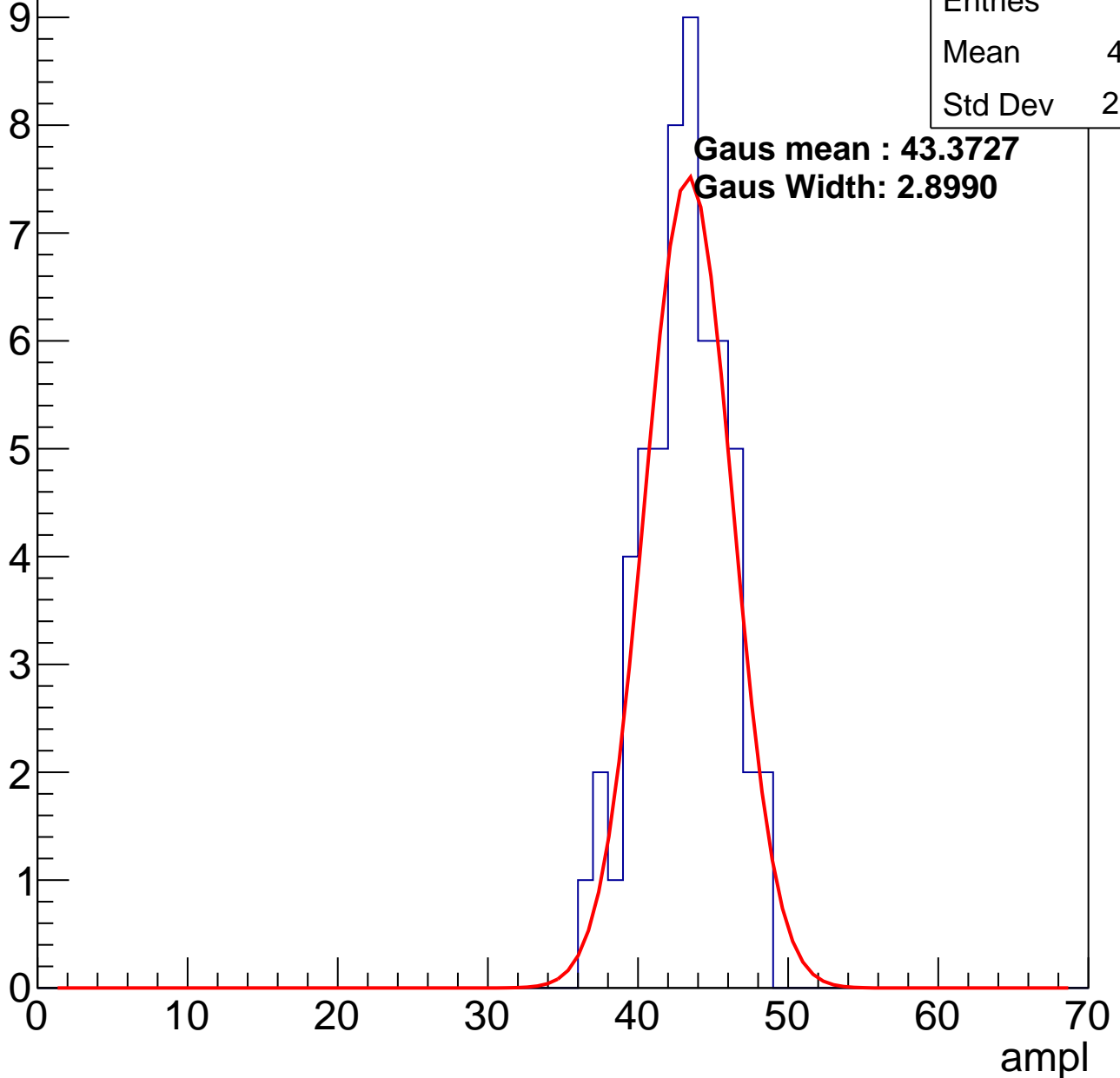
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 56    |
| Mean    | 42.61 |
| Std Dev | 2.775 |

**Gaus mean : 43.3727**

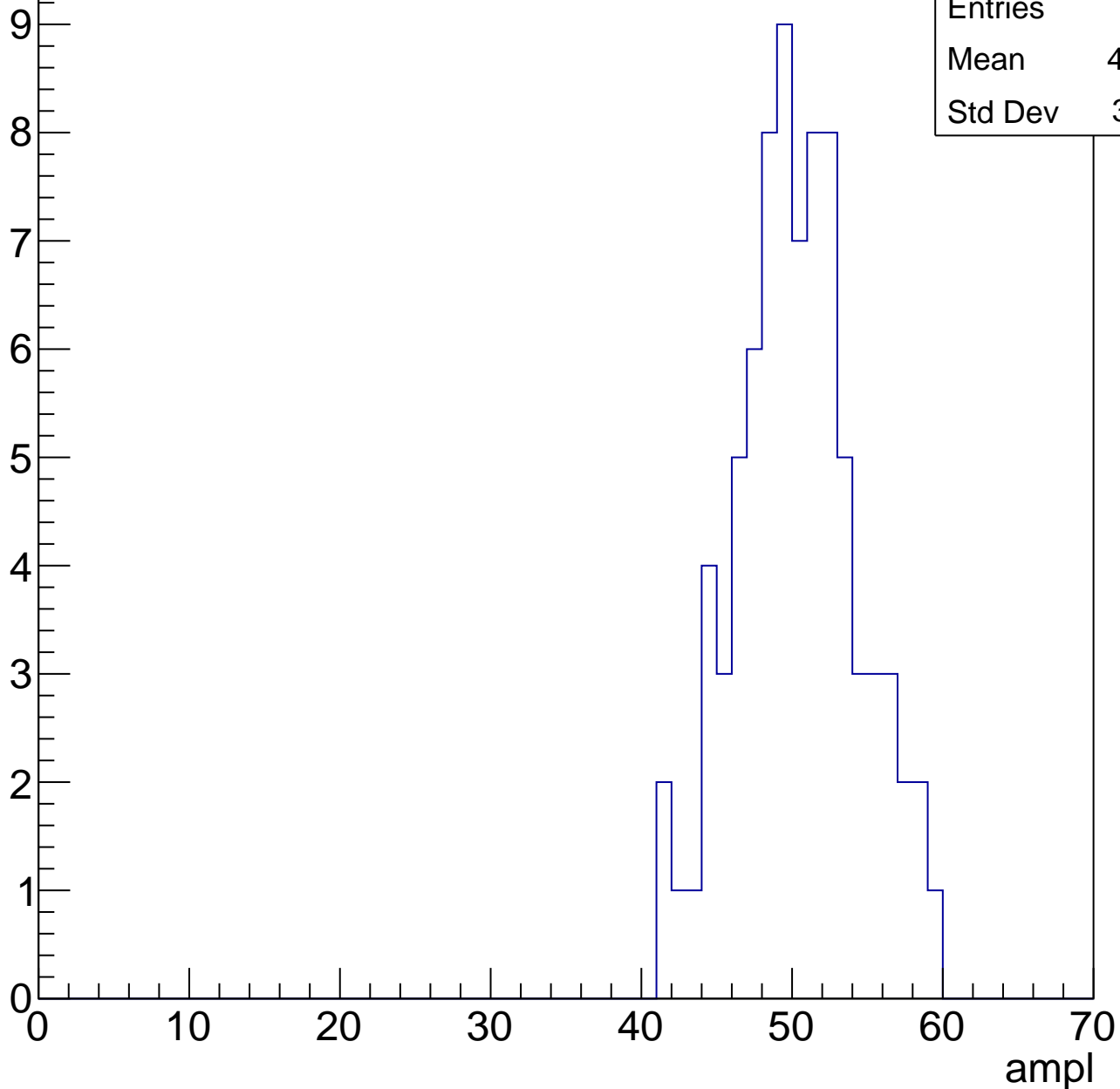
**Gaus Width: 2.8990**



# B0L001S, U2-ch0, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

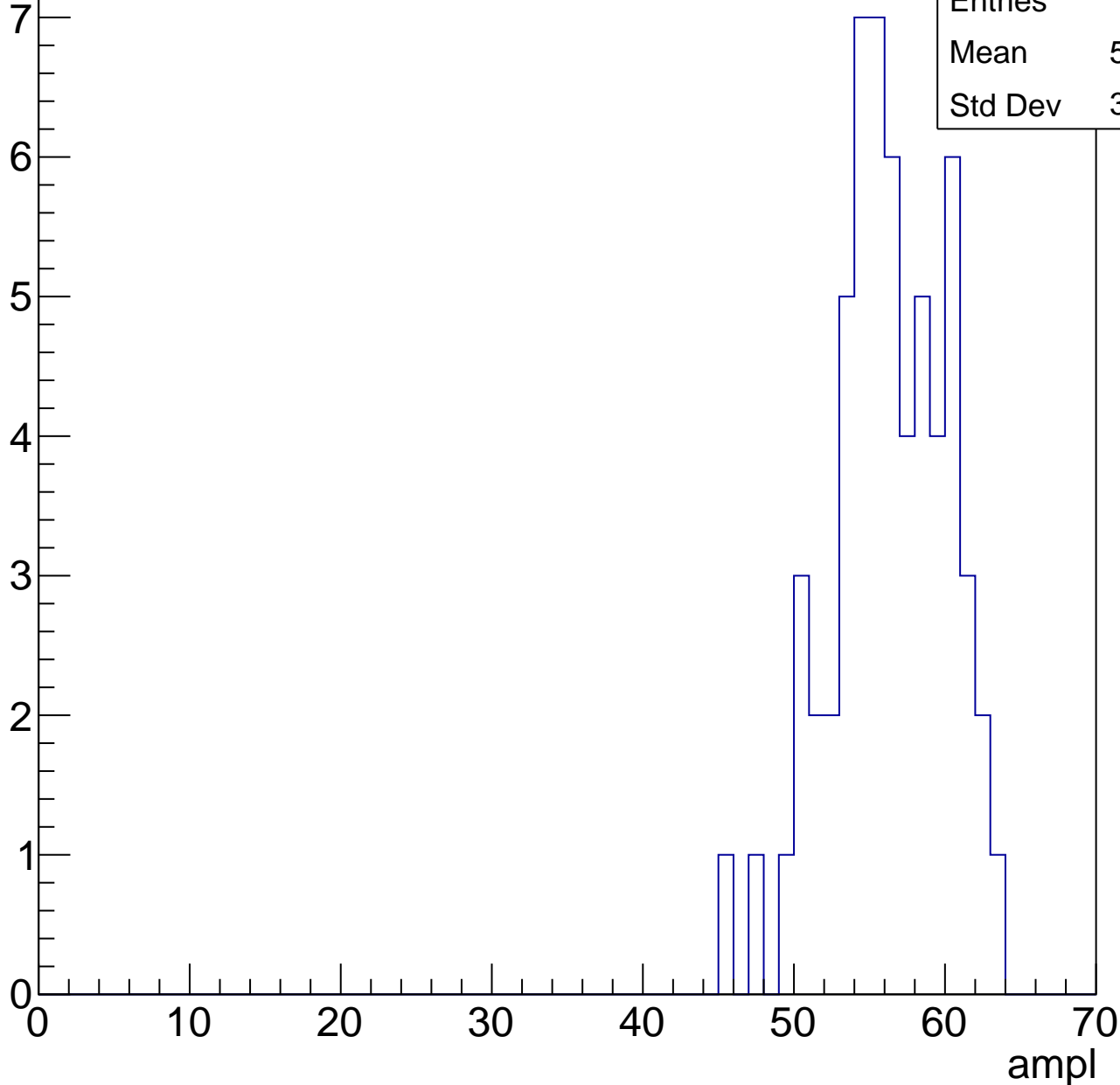


# B0L001S, U2-ch0, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 60    |
| Mean    | 55.75 |
| Std Dev | 3.806 |

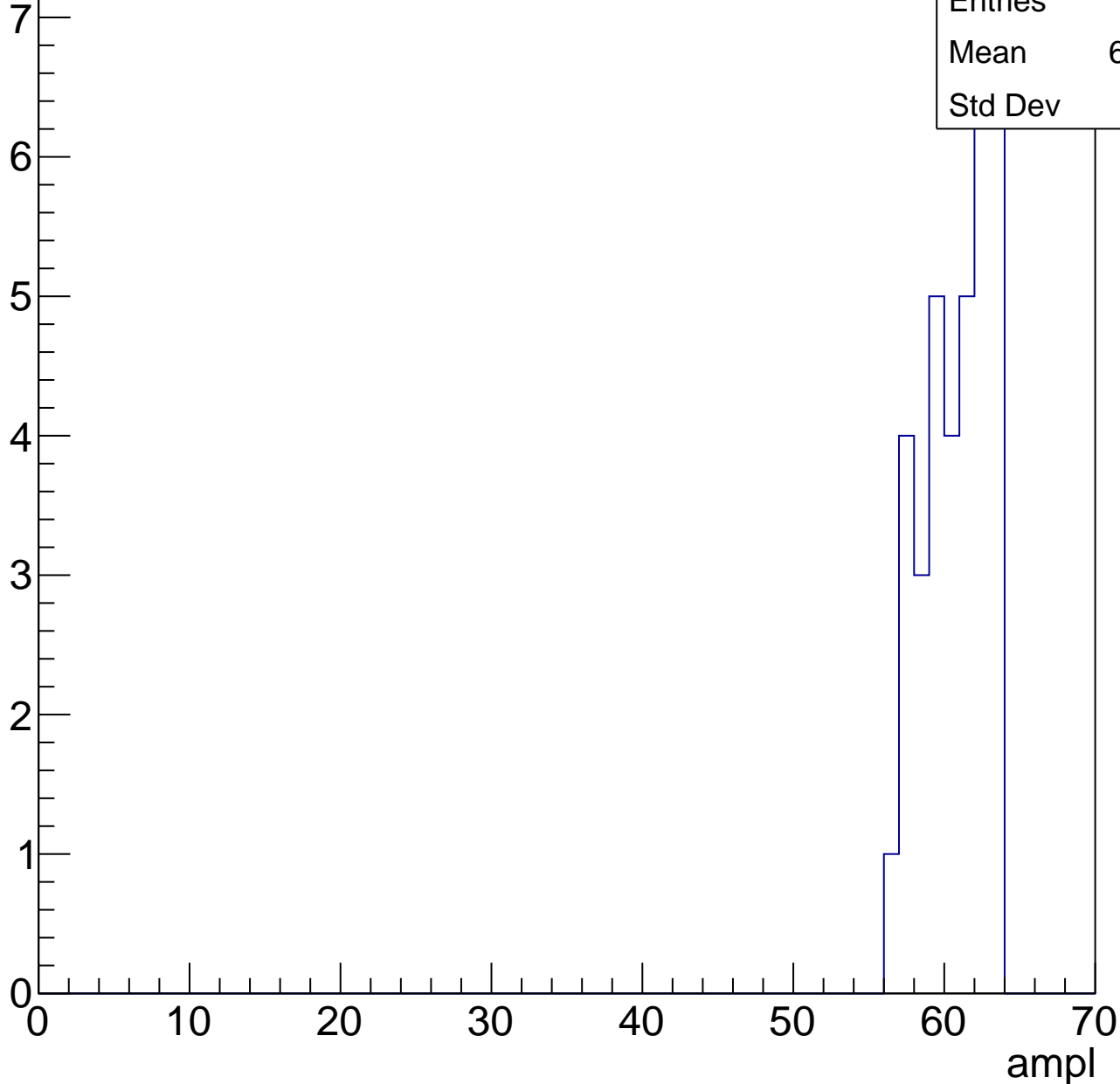


# B0L001S, U2-ch0, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 36    |
| Mean    | 60.36 |
| Std Dev | 2.11  |



# B0L001S, U2-ch0, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

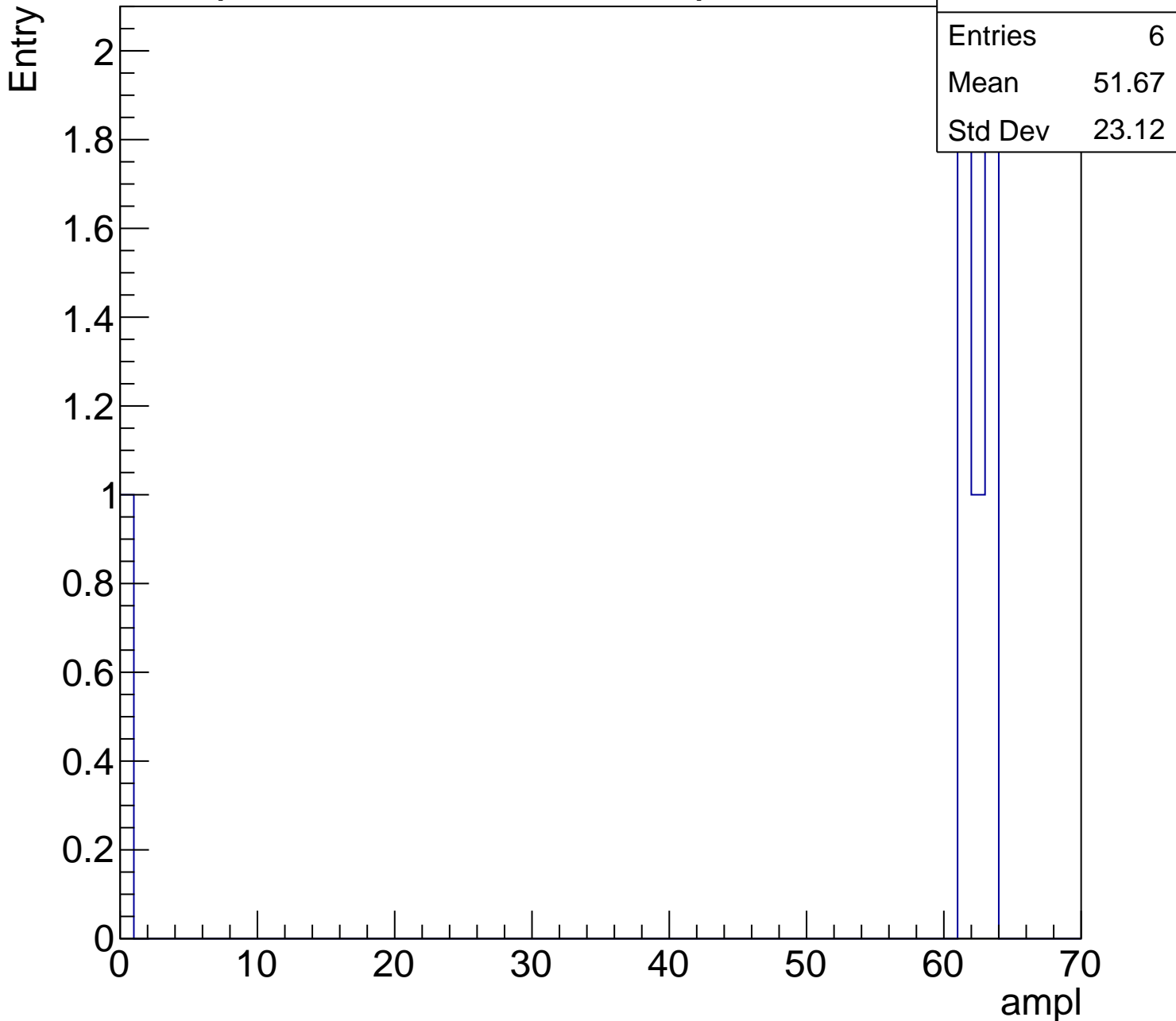
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

|         |       |
|---------|-------|
| Entries | 6     |
| Mean    | 51.67 |
| Std Dev | 23.12 |

0 10 20 30 40 50 60 70

ampl





# B0L001S, U2-ch0, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 0 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch1, adc0

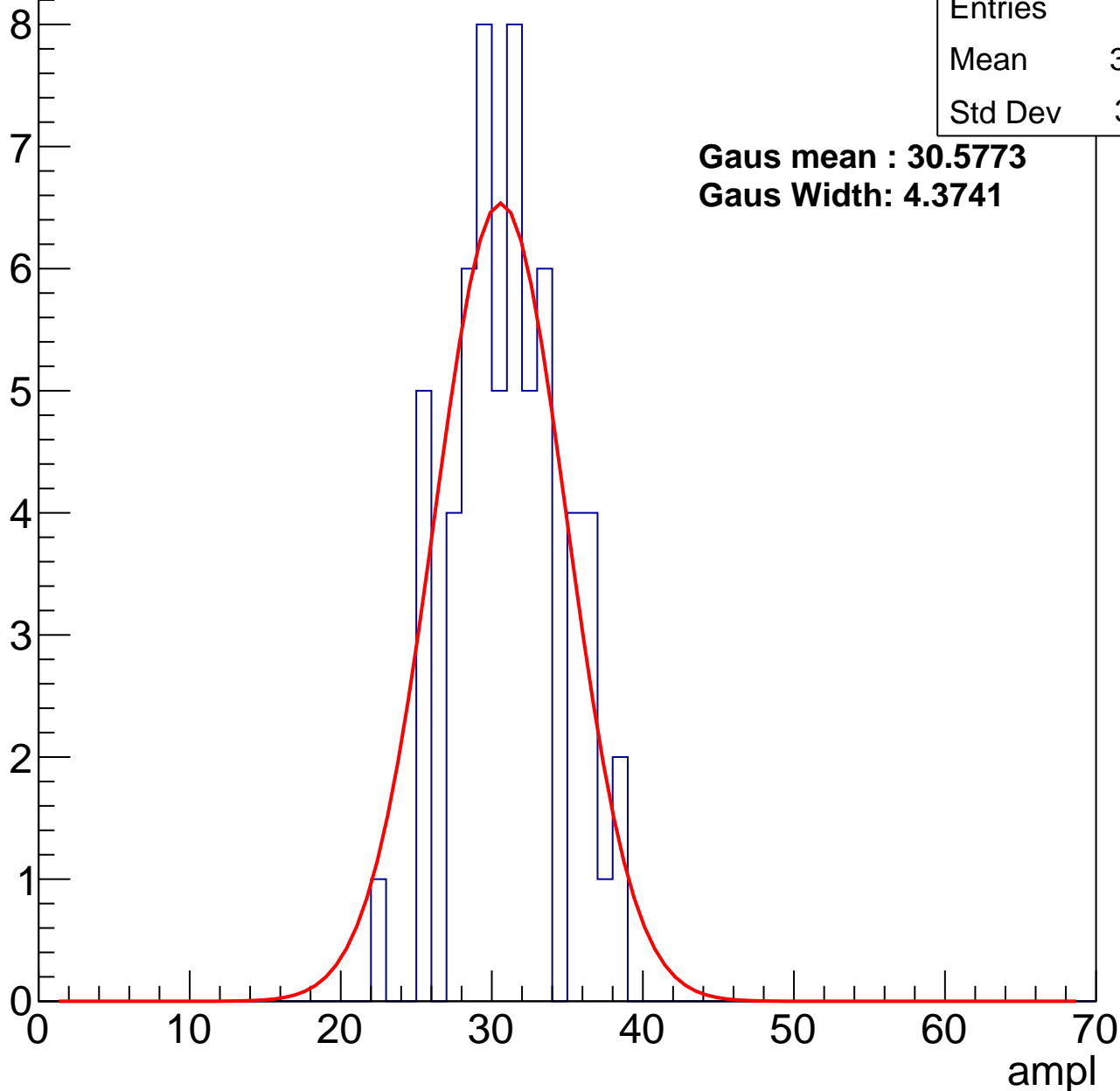
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 59    |
| Mean    | 30.64 |
| Std Dev | 3.531 |

**Gaus mean : 30.5773**

**Gaus Width: 4.3741**



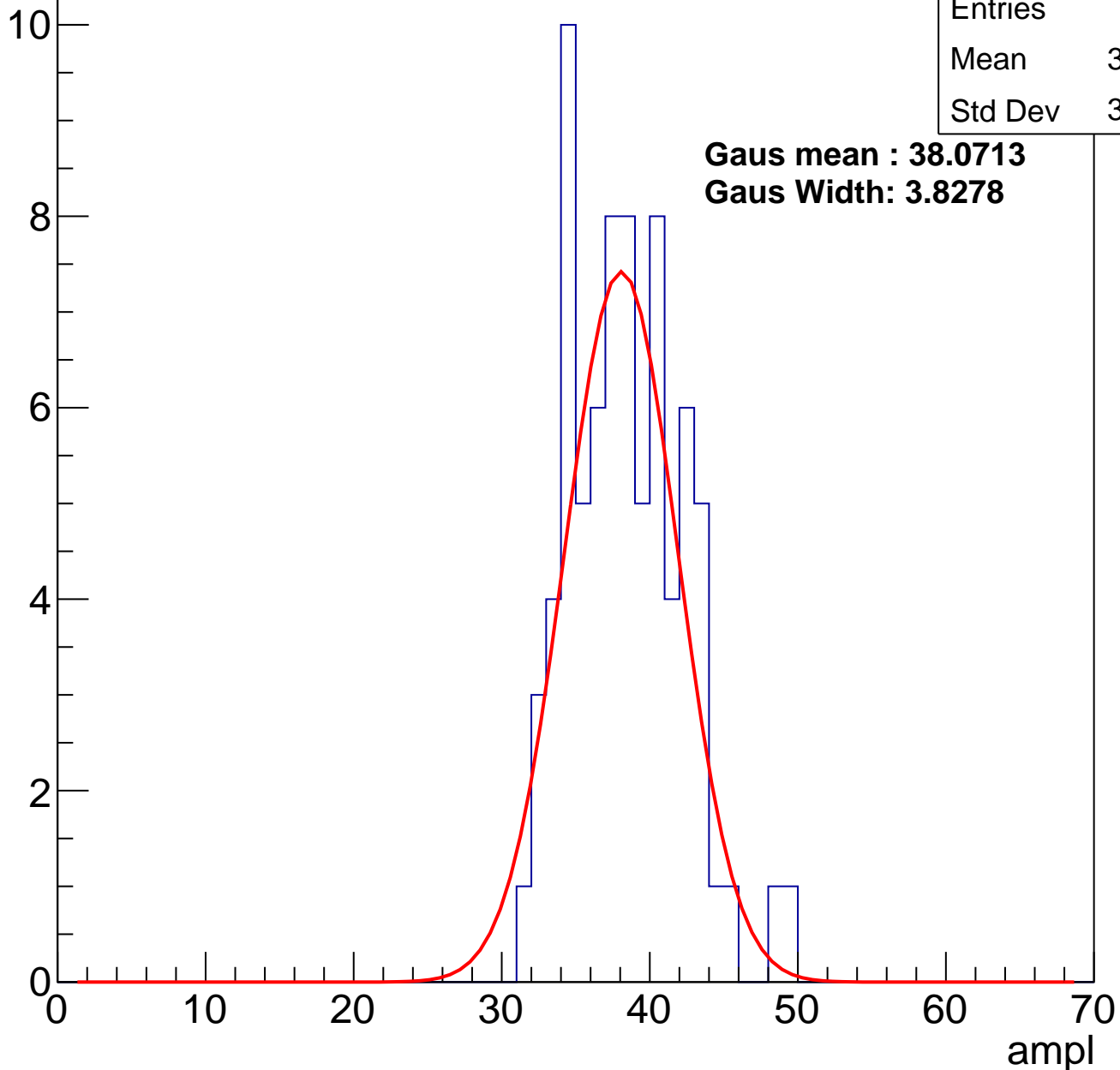
# B0L001S, U2-ch1, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 77    |
| Mean    | 37.95 |
| Std Dev | 3.769 |

**Gaus mean : 38.0713**  
**Gaus Width: 3.8278**

Entry



# B0L001S, U2-ch1, adc2

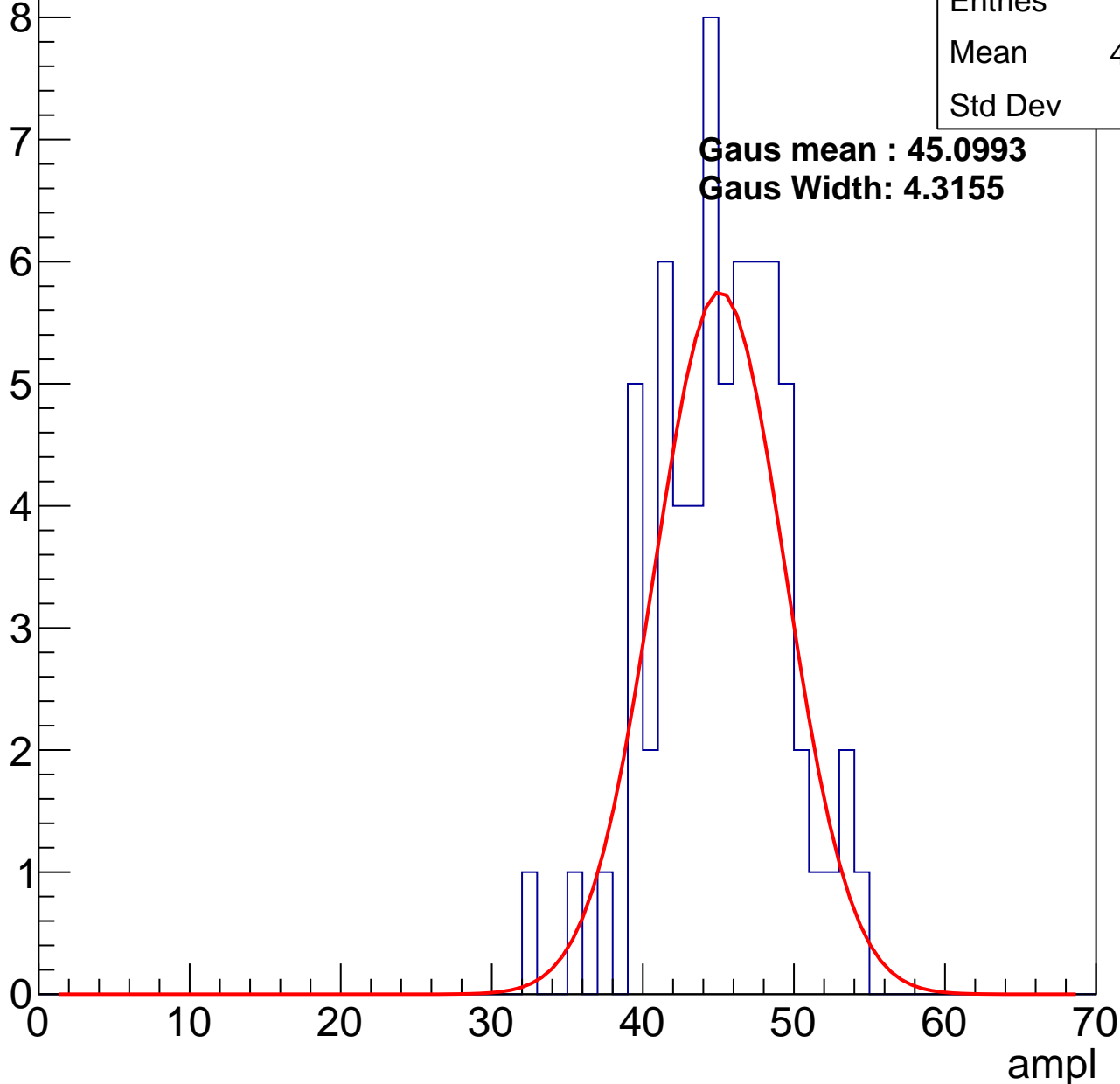
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 67    |
| Mean    | 44.72 |
| Std Dev | 4.27  |

**Gaus mean : 45.0993**

**Gaus Width: 4.3155**

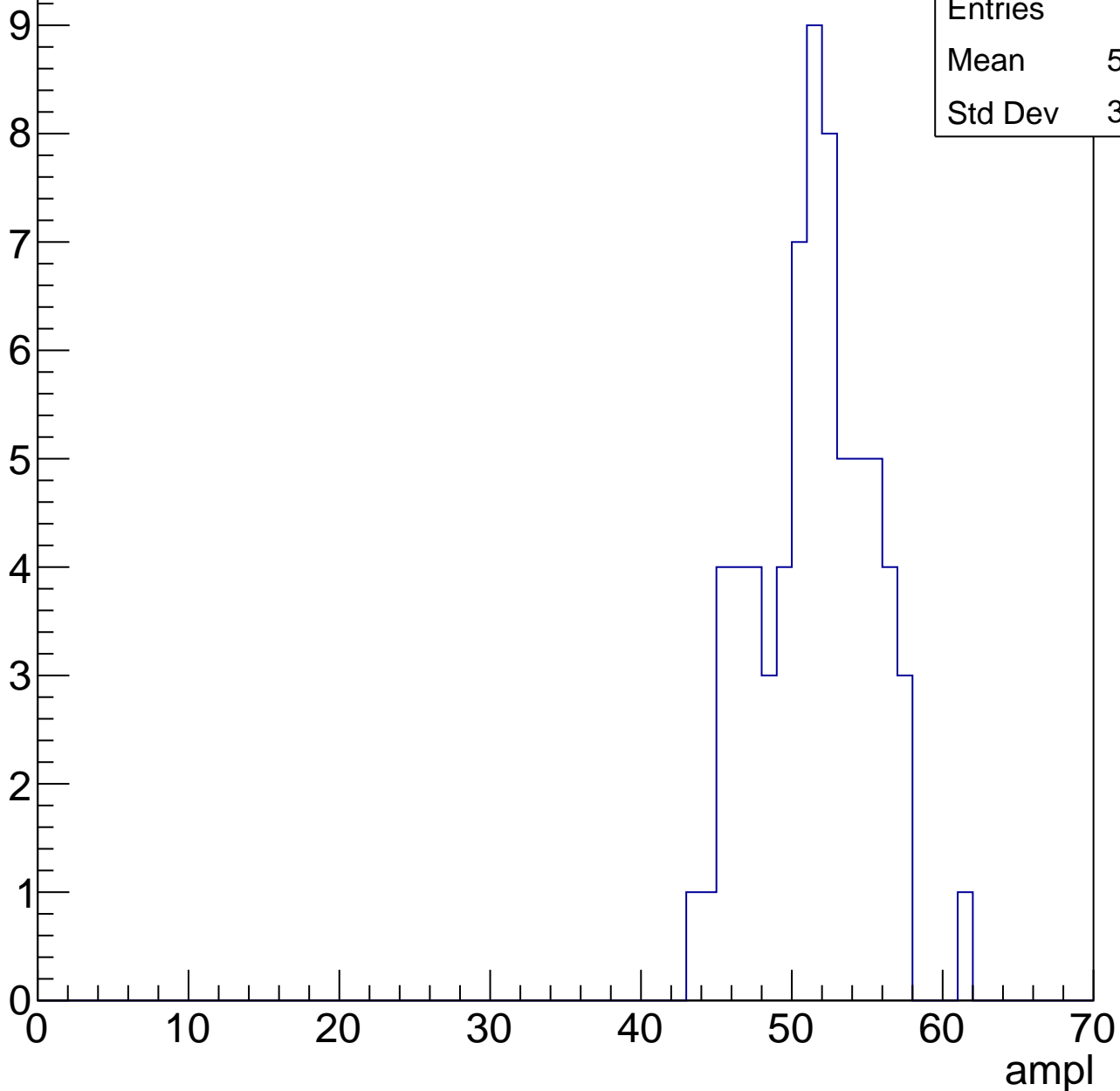


# B0L001S, U2-ch1, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 68    |
| Mean    | 51.03 |
| Std Dev | 3.702 |



# B0L001S, U2-ch1, adc4

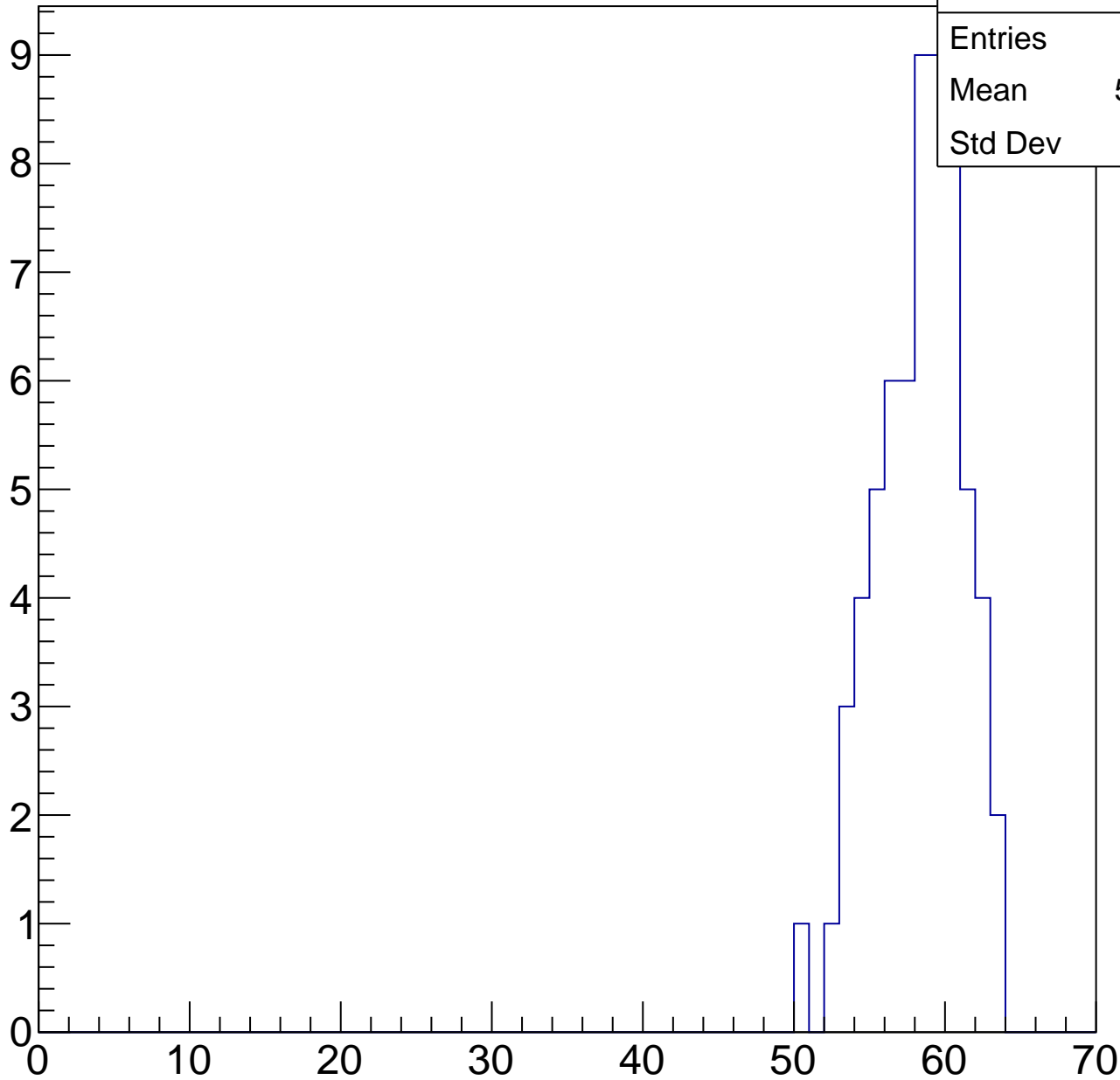
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

|         |       |
|---------|-------|
| Entries | 63    |
| Mean    | 57.81 |
| Std Dev | 2.85  |

ampl

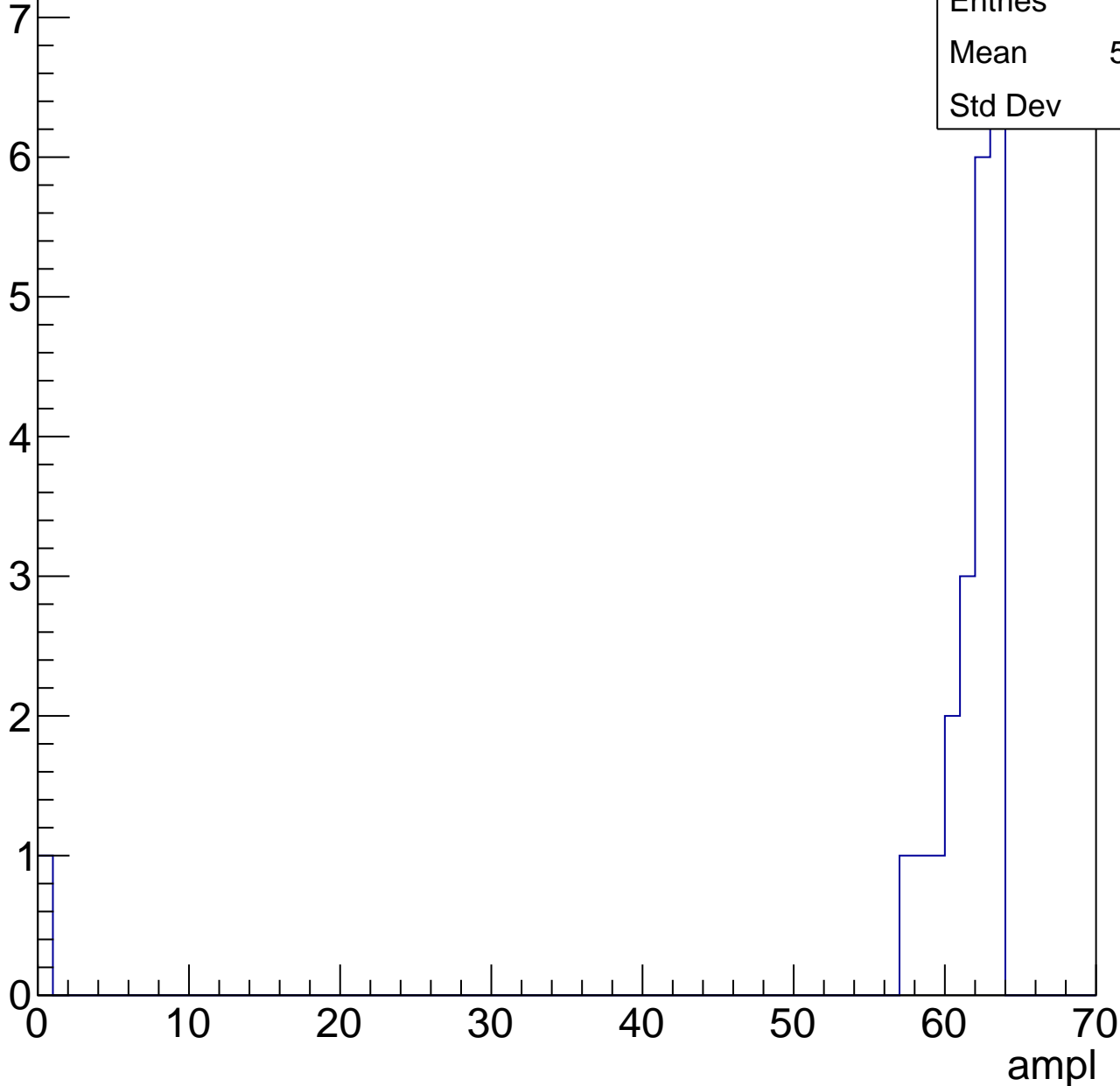


# B0L001S, U2-ch1, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 22    |
| Mean    | 58.64 |
| Std Dev | 12.9  |



# B0L001S, U2-ch1, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch1, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U2-ch2, adc0

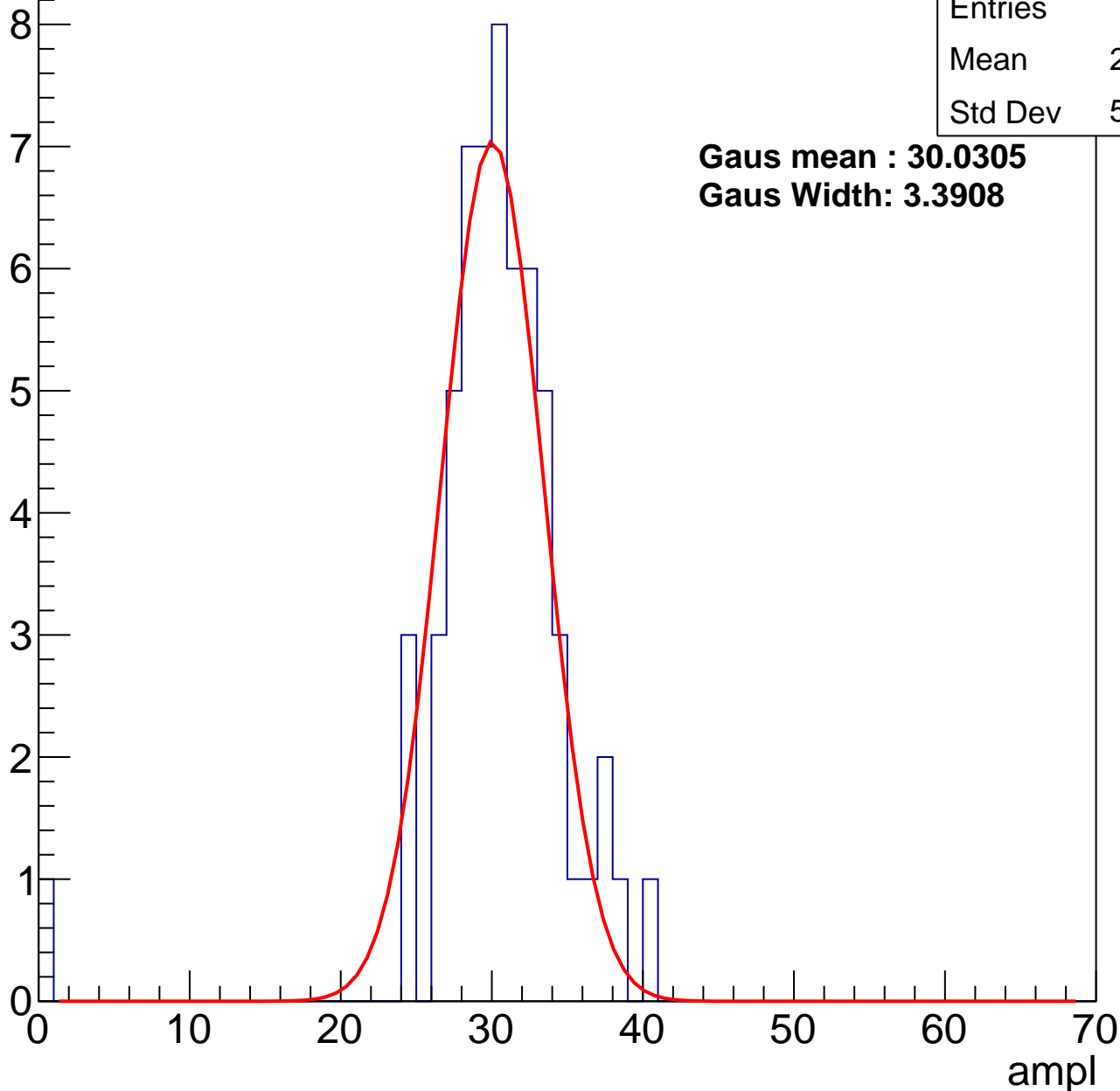
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 60    |
| Mean    | 29.87 |
| Std Dev | 5.133 |

**Gaus mean : 30.0305**

**Gaus Width: 3.3908**



# B0L001S, U2-ch2, adc1

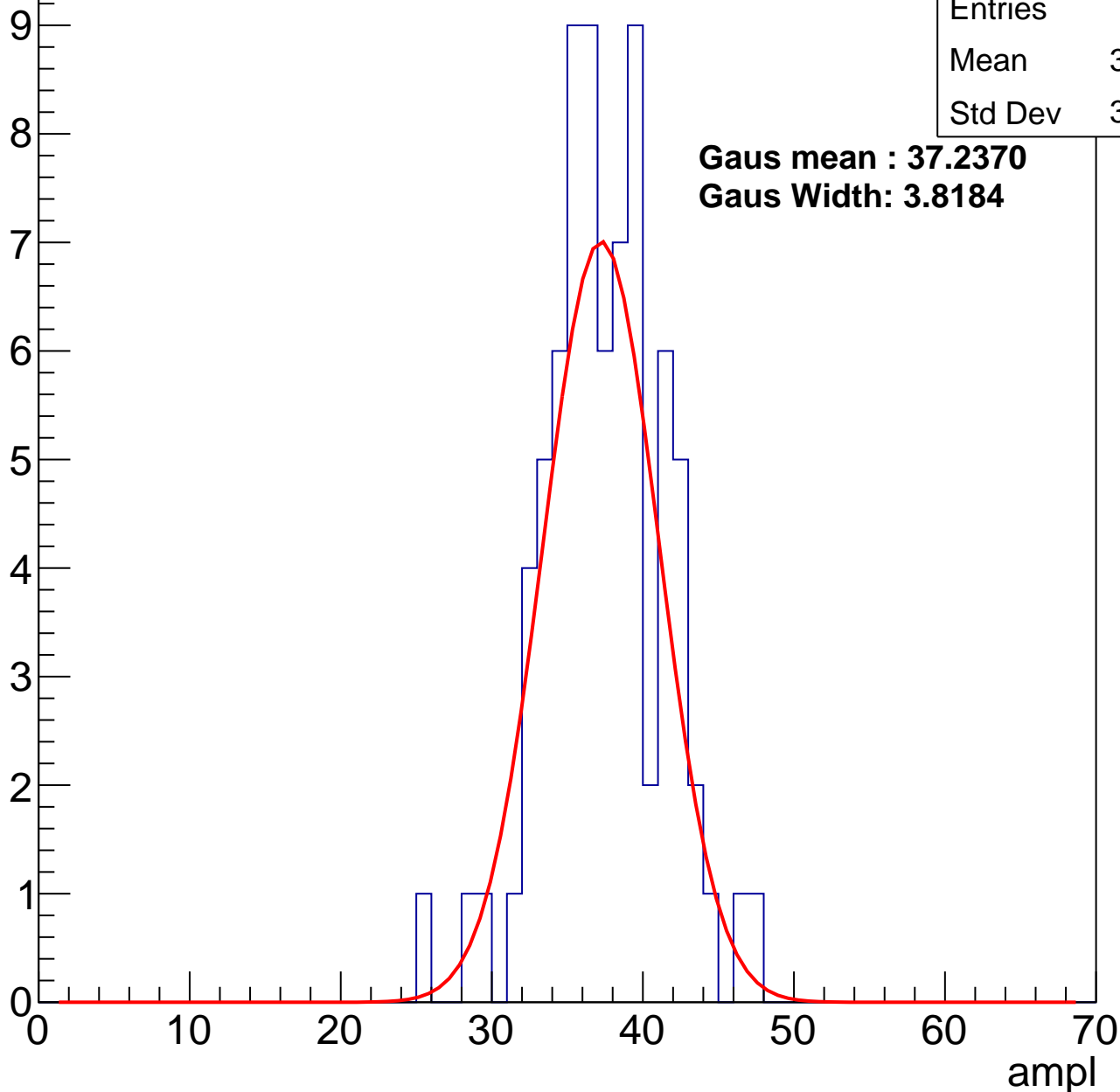
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 77    |
| Mean    | 36.97 |
| Std Dev | 3.928 |

**Gaus mean : 37.2370**

**Gaus Width: 3.8184**



# B0L001S, U2-ch2, adc2

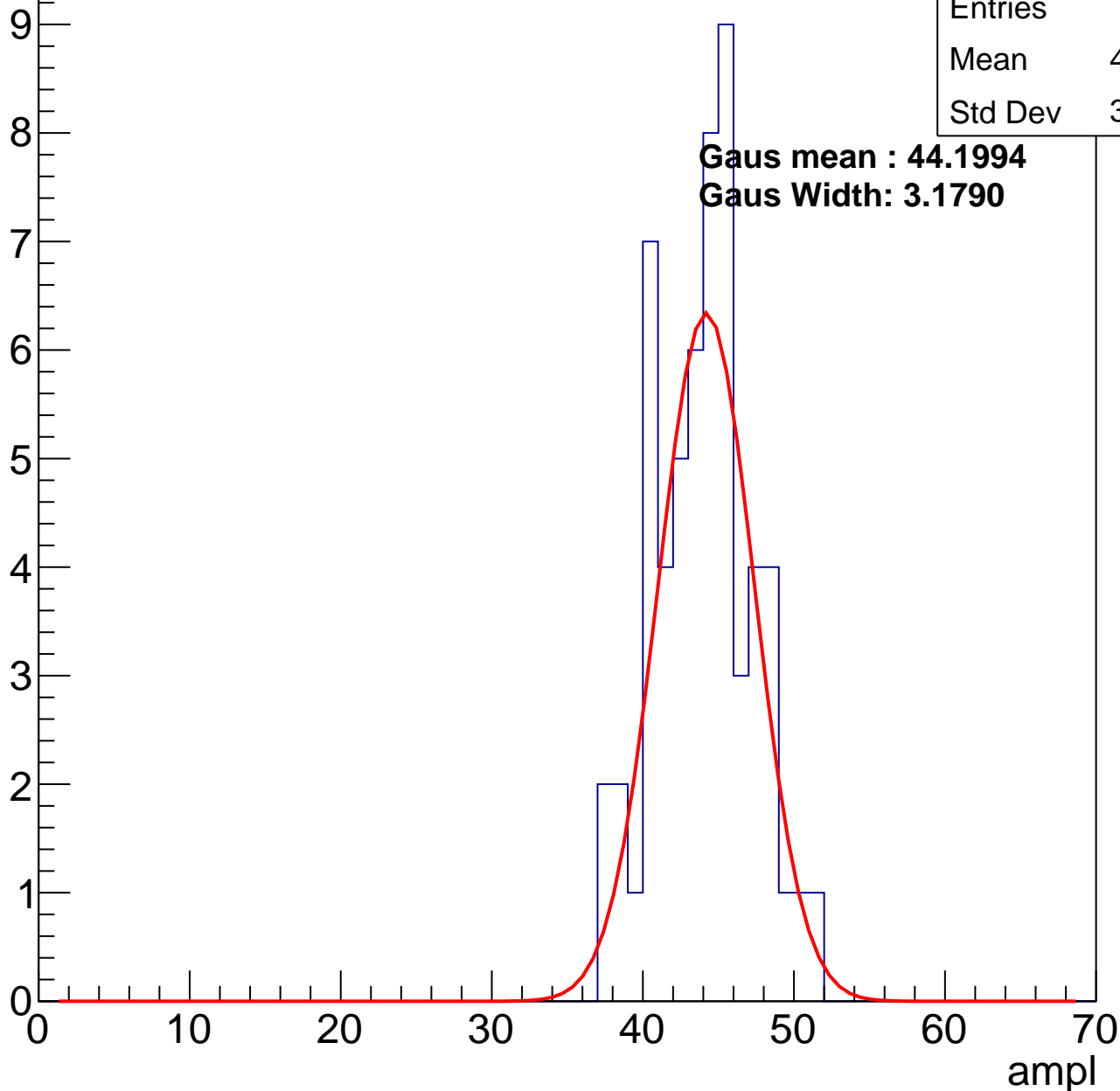
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 58    |
| Mean    | 43.55 |
| Std Dev | 3.185 |

**Gaus mean : 44.1994**

**Gaus Width: 3.1790**

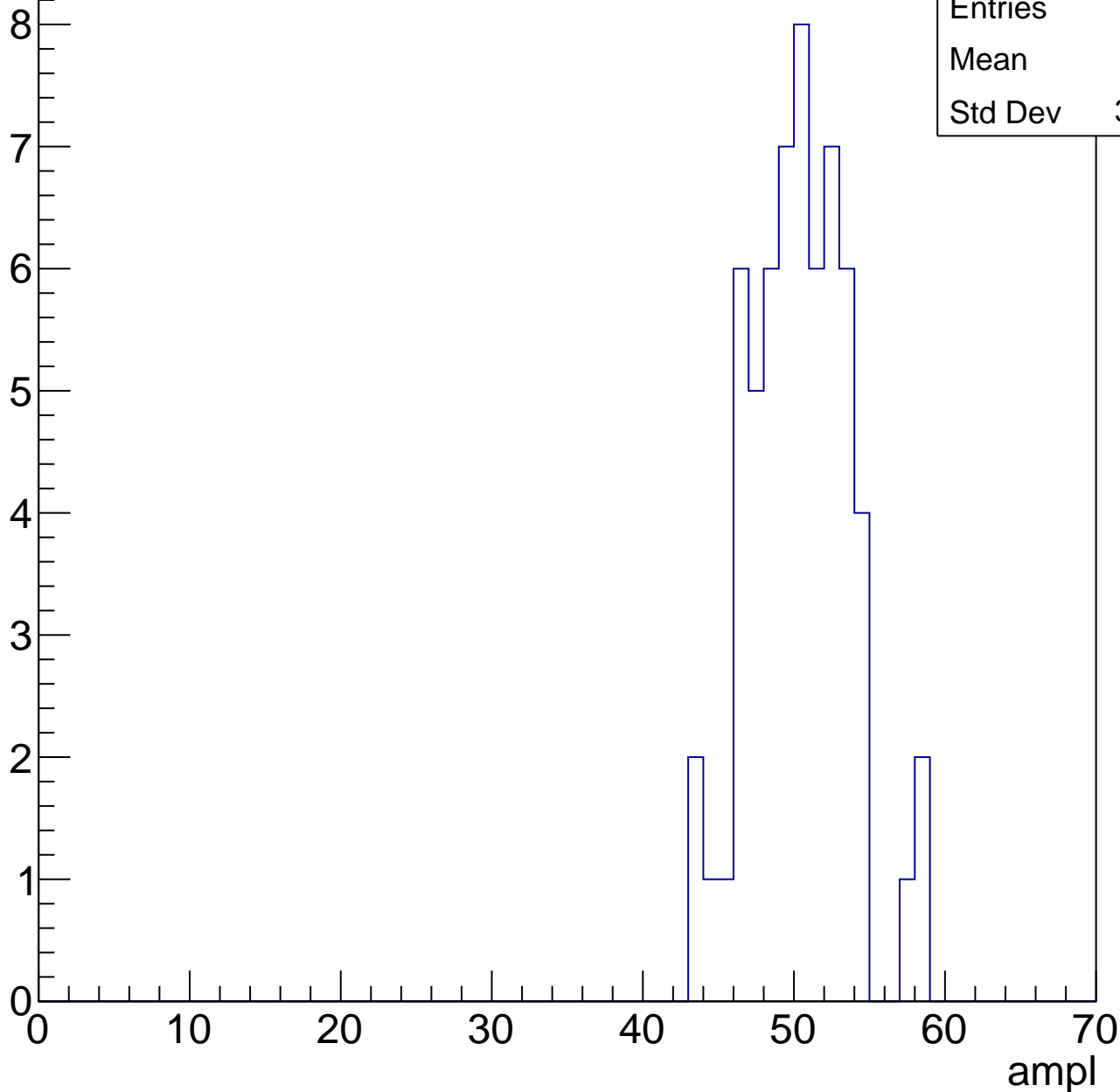


# B0L001S, U2-ch2, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

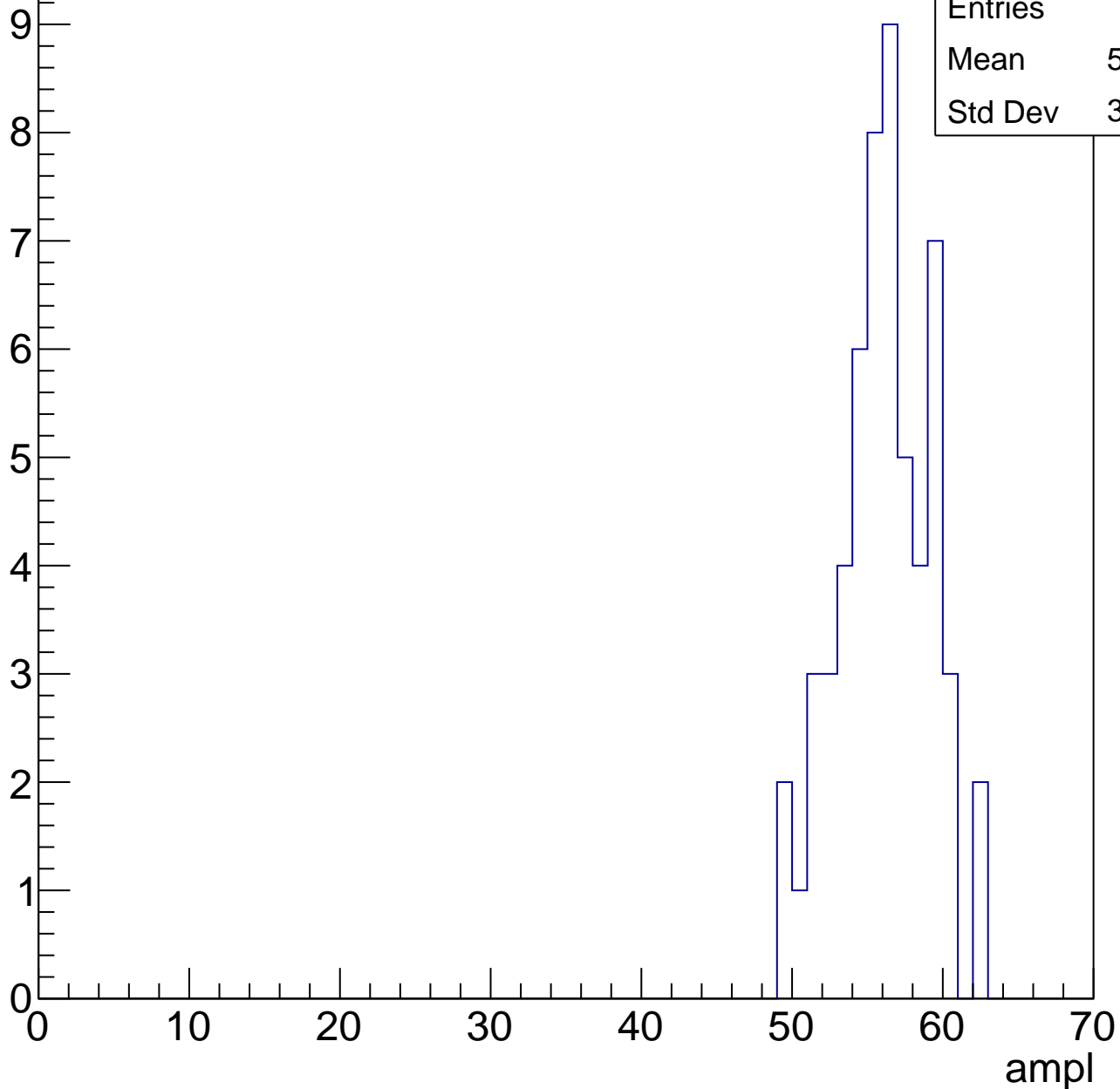
|         |       |
|---------|-------|
| Entries | 62    |
| Mean    | 49.9  |
| Std Dev | 3.261 |



# B0L001S, U2-ch2, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U2-ch2, adc5

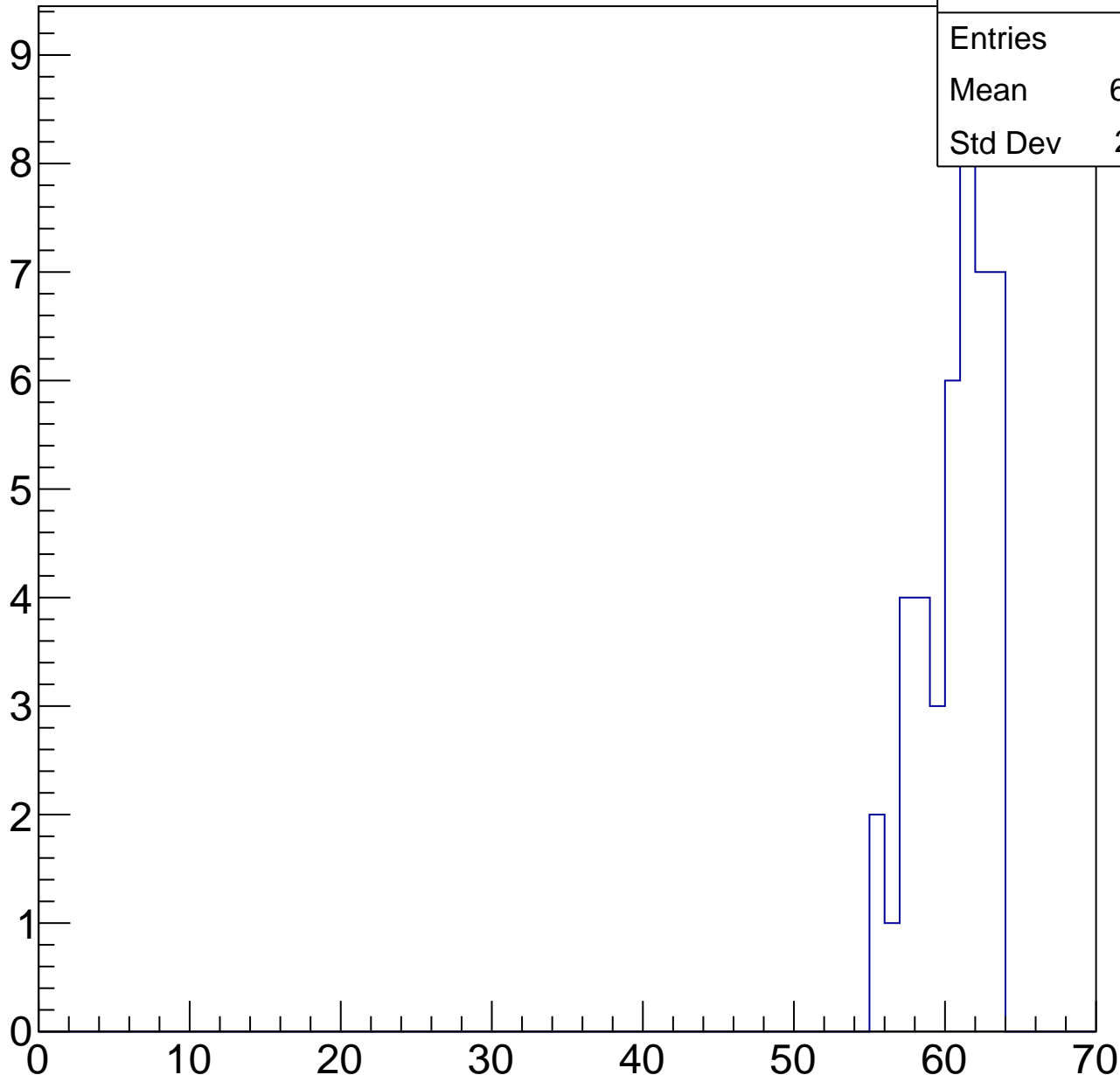
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

|         |       |
|---------|-------|
| Entries | 43    |
| Mean    | 60.16 |
| Std Dev | 2.261 |

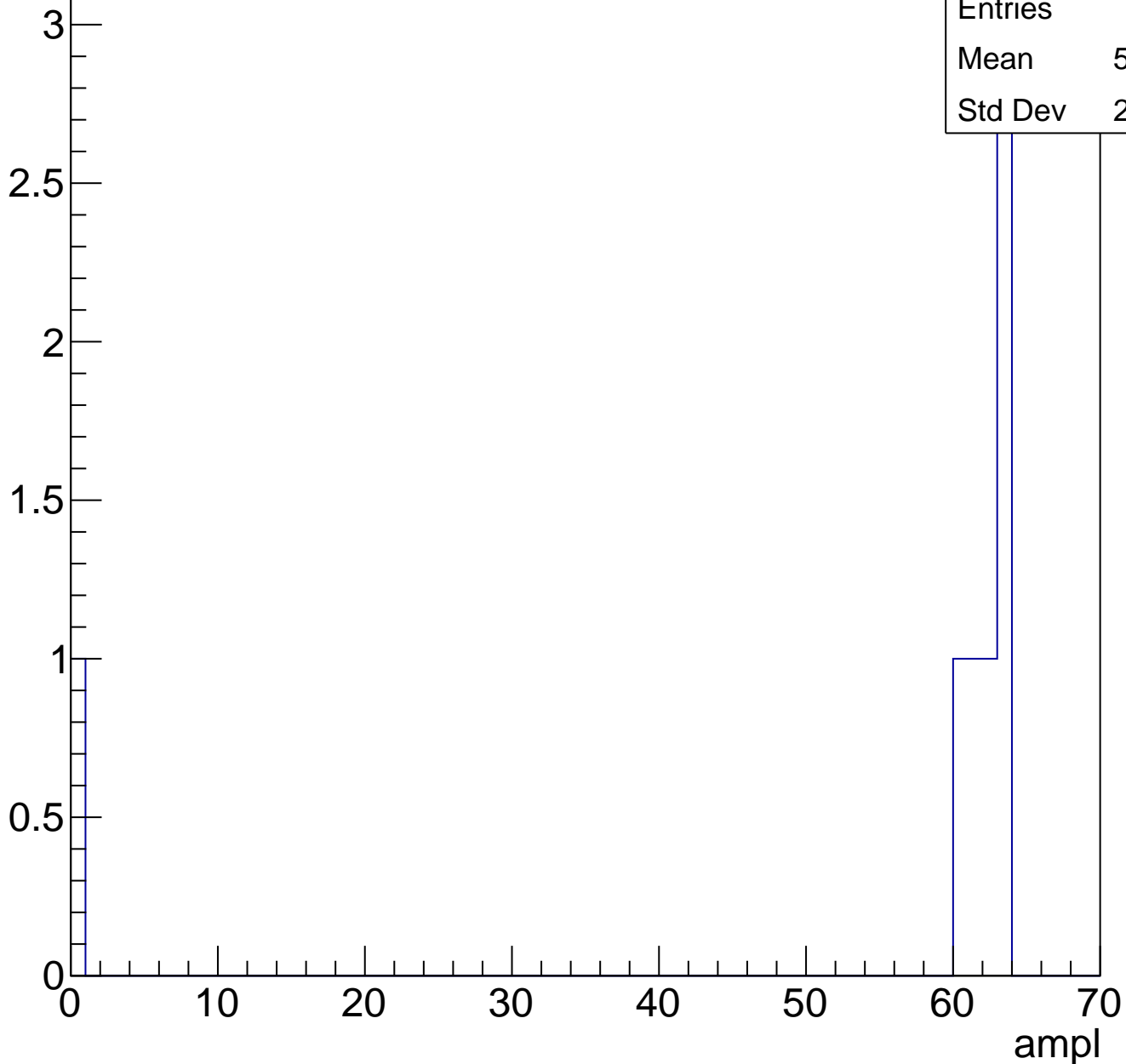
ampl



# B0L001S, U2-ch2, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch2, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 0 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch3, adc0

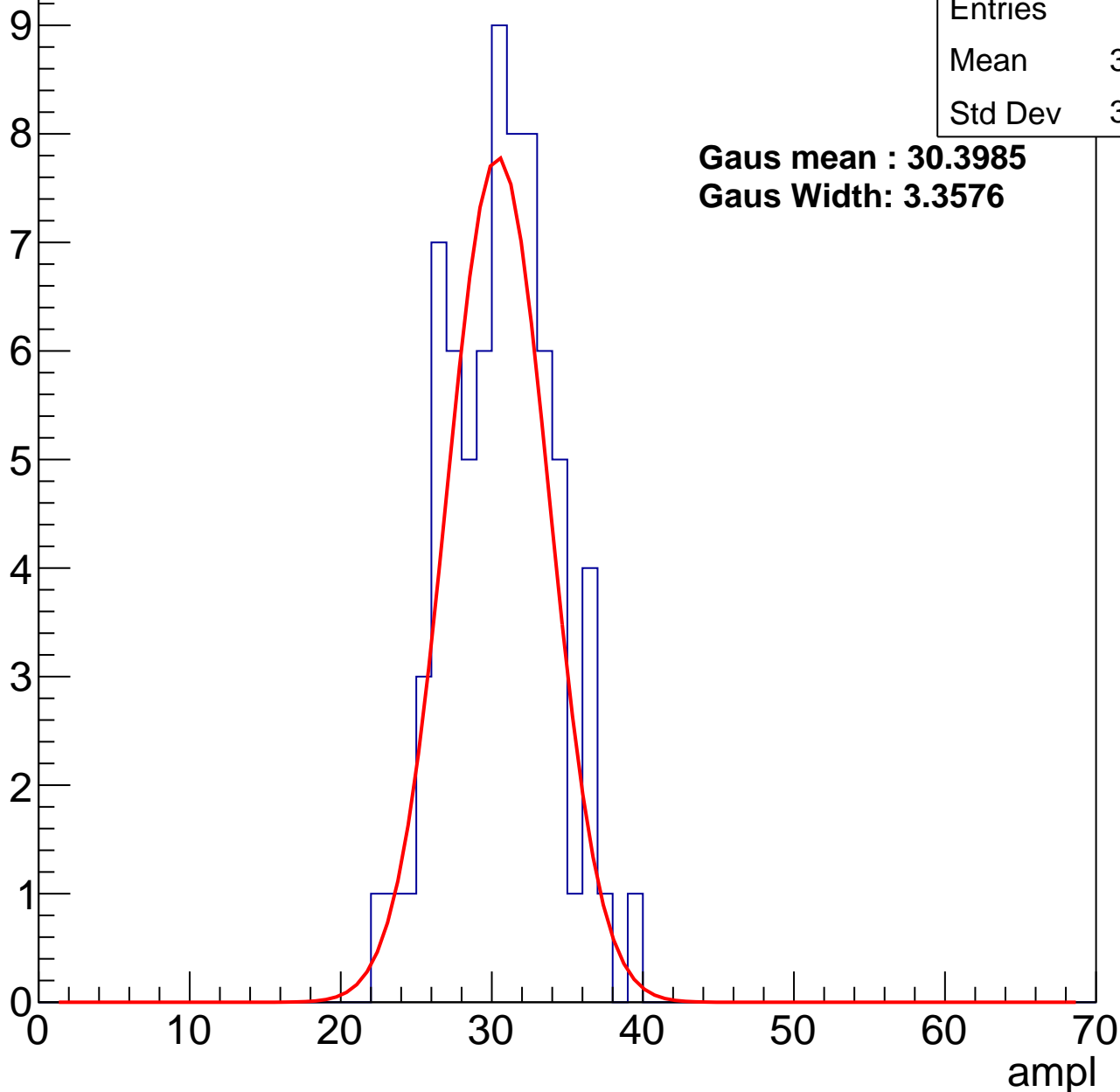
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 73    |
| Mean    | 30.12 |
| Std Dev | 3.488 |

**Gaus mean : 30.3985**

**Gaus Width: 3.3576**



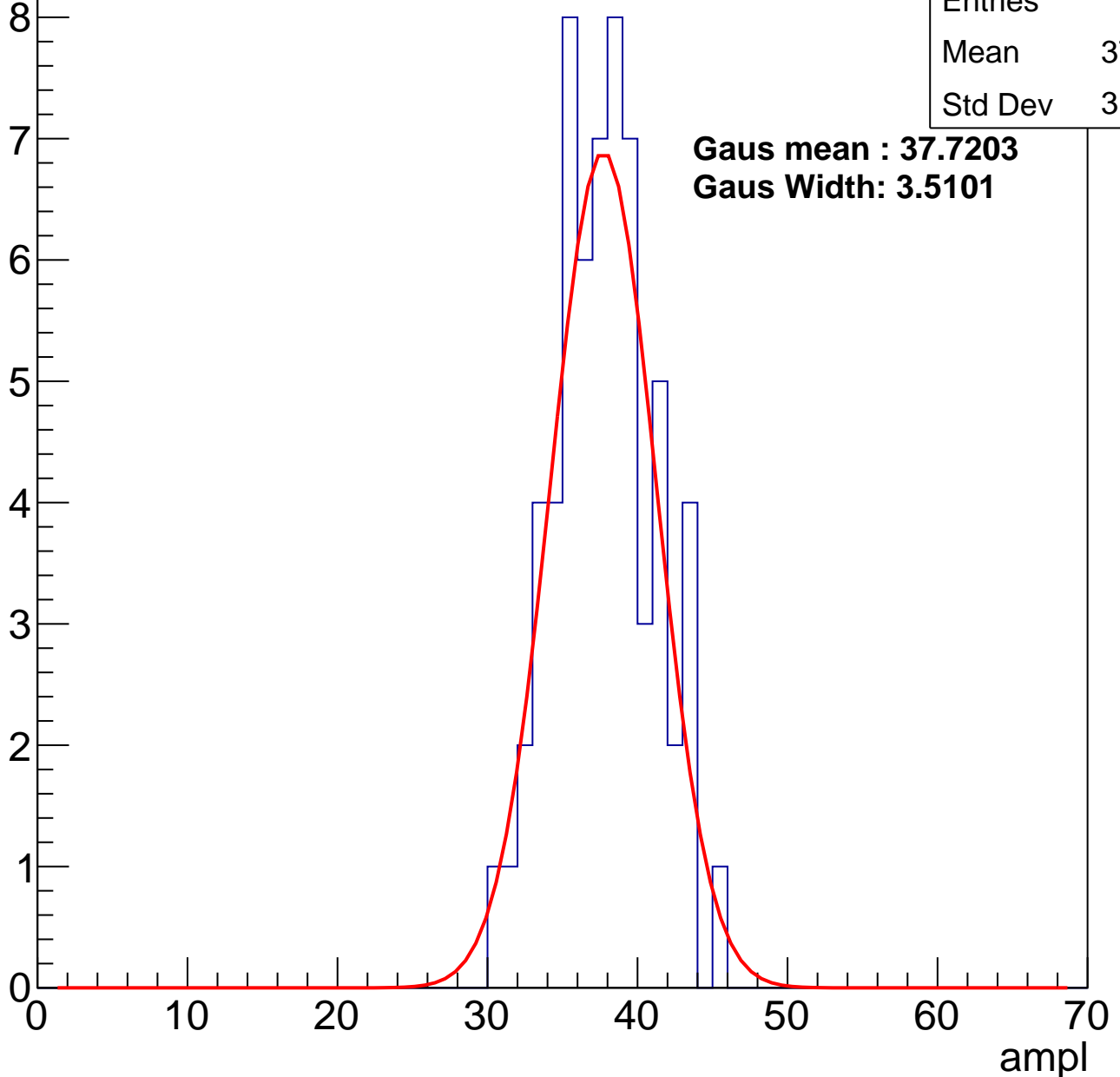
# B0L001S, U2-ch3, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 63    |
| Mean    | 37.32 |
| Std Dev | 3.255 |

**Gaus mean : 37.7203**  
**Gaus Width: 3.5101**



# B0L001S, U2-ch3, adc2

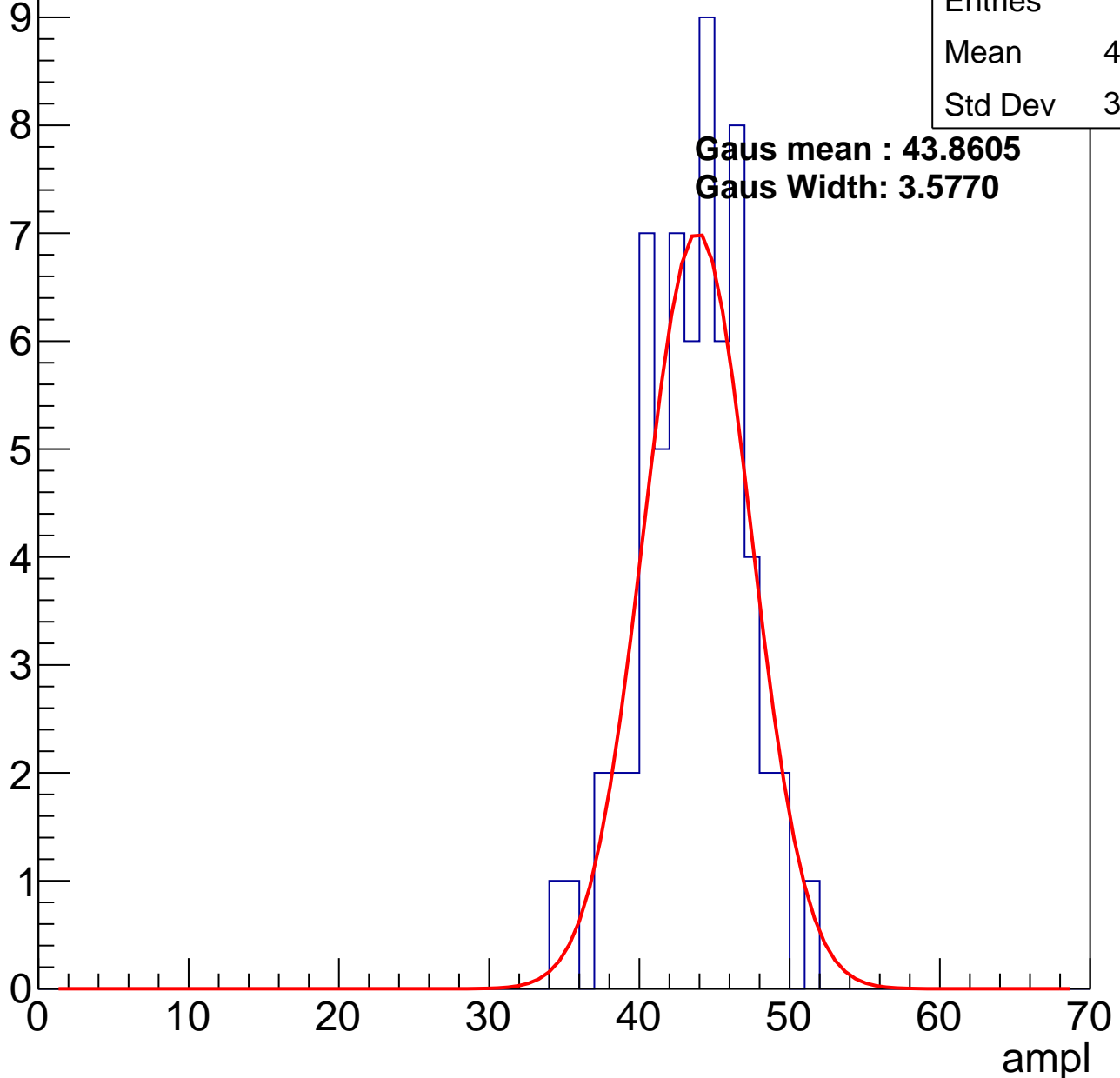
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 65    |
| Mean    | 43.09 |
| Std Dev | 3.382 |

**Gaus mean : 43.8605**

**Gaus Width: 3.5770**

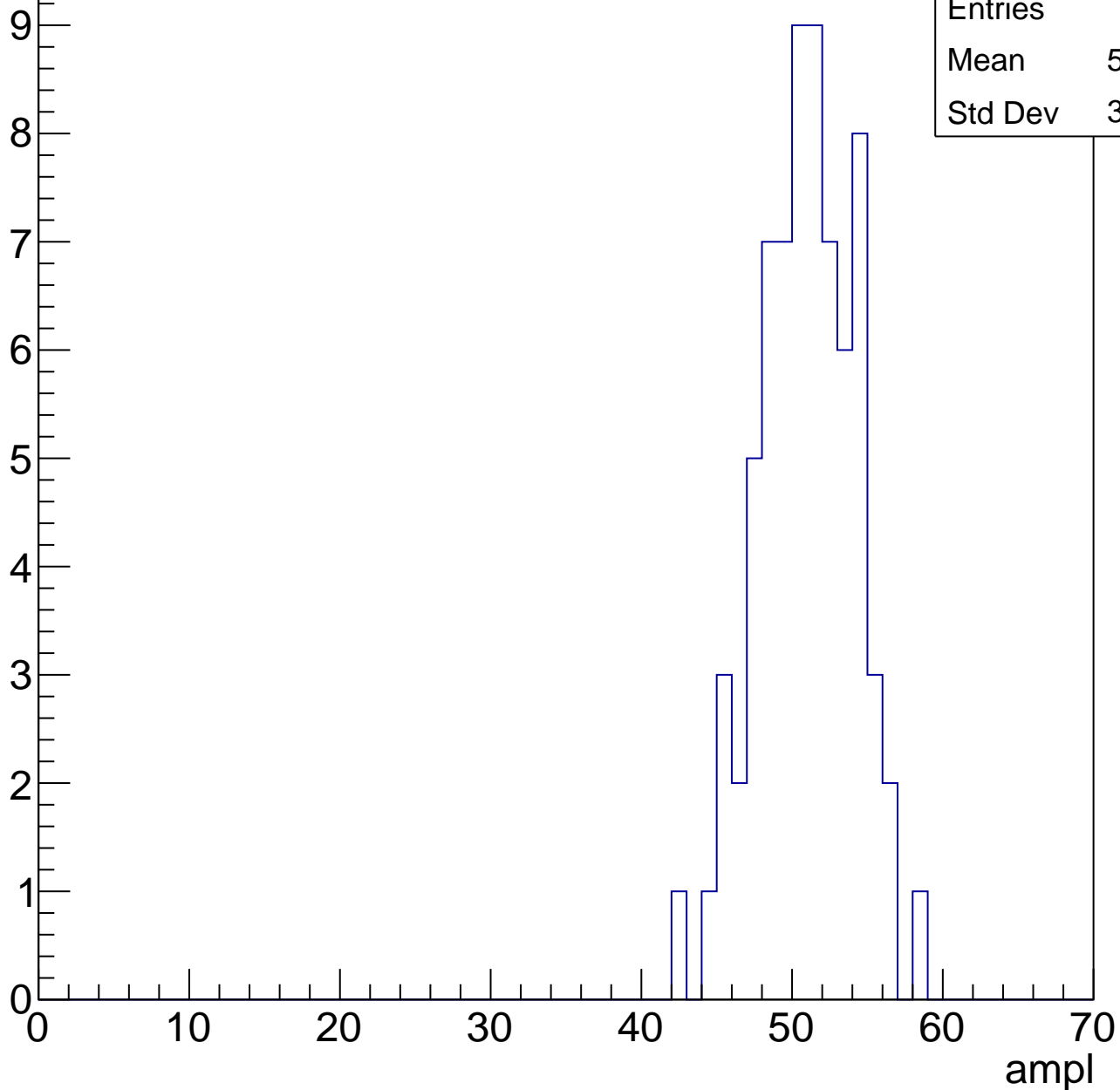


# B0L001S, U2-ch3, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

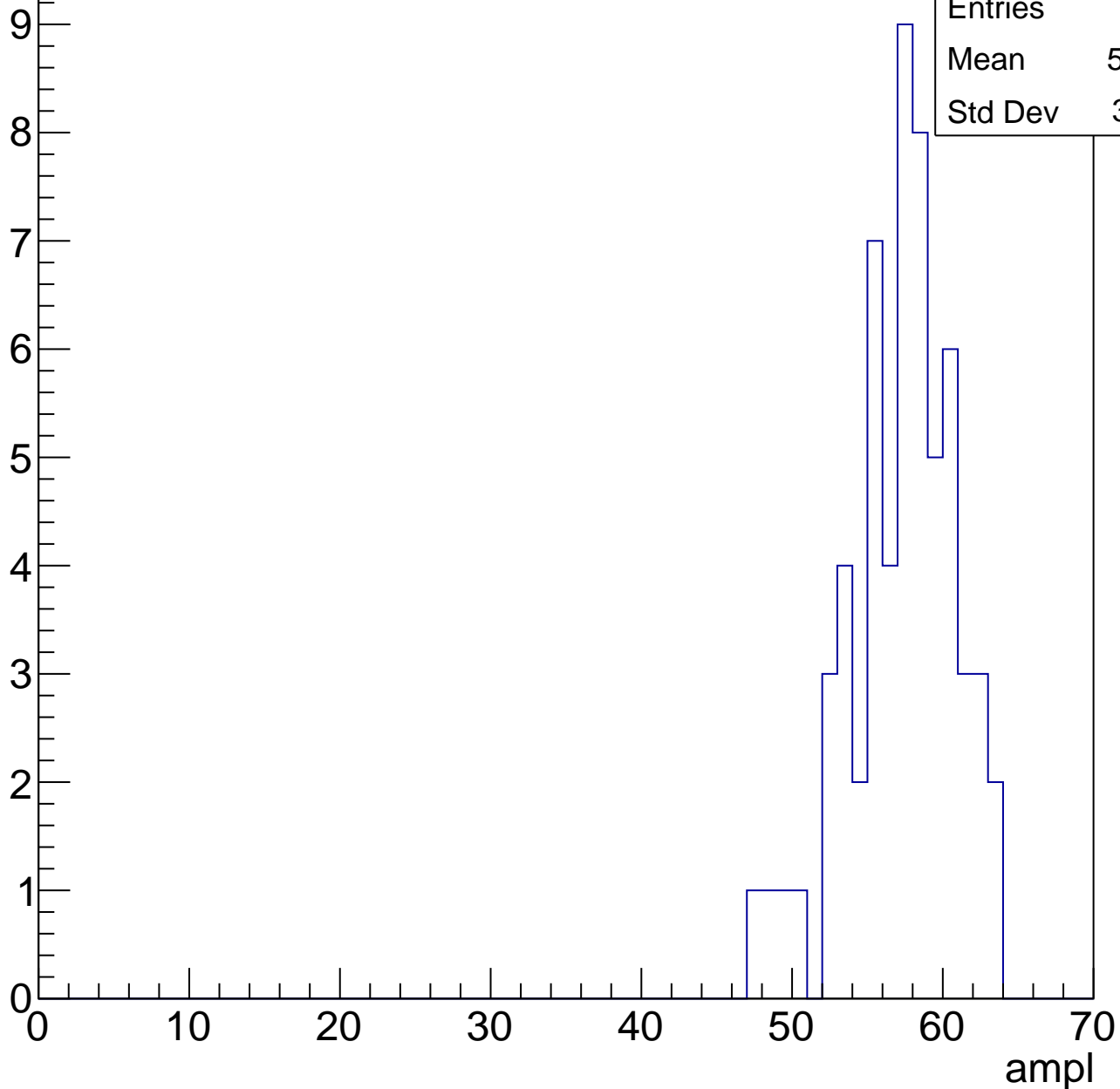
|         |       |
|---------|-------|
| Entries | 71    |
| Mean    | 50.49 |
| Std Dev | 3.139 |



# B0L001S, U2-ch3, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U2-ch3, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

7

6

5

4

3

2

1

0

0

10

20

30

40

50

60

70

ampl

|         |       |
|---------|-------|
| Entries | 33    |
| Mean    | 60.21 |
| Std Dev | 2.143 |

0

1

2

3

4

5

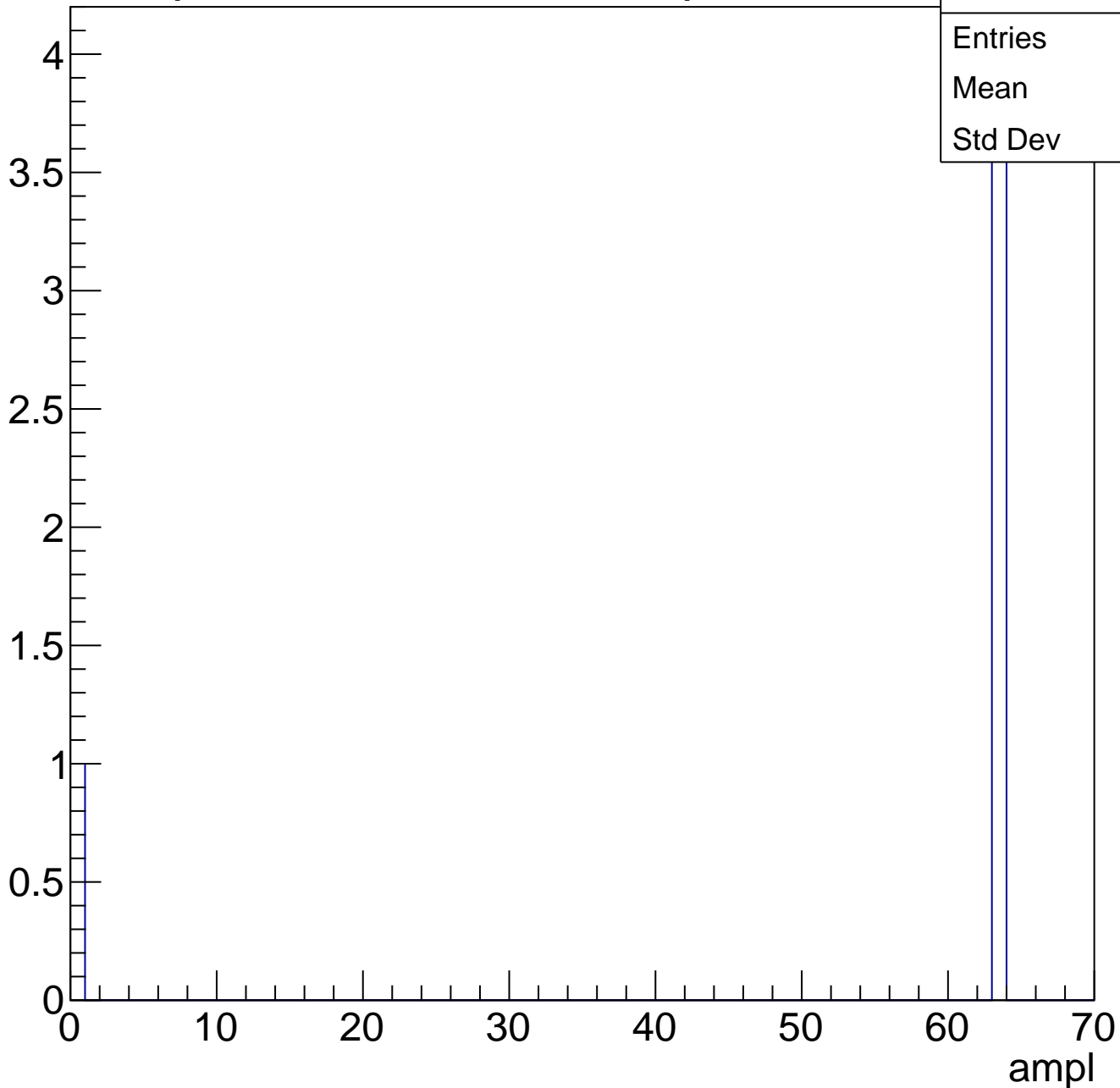
6

7

# B0L001S, U2-ch3, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch3, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 1 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch4, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 90    |
| Mean    | 29.41 |
| Std Dev | 8.452 |

**Gaus mean : 31.9718**

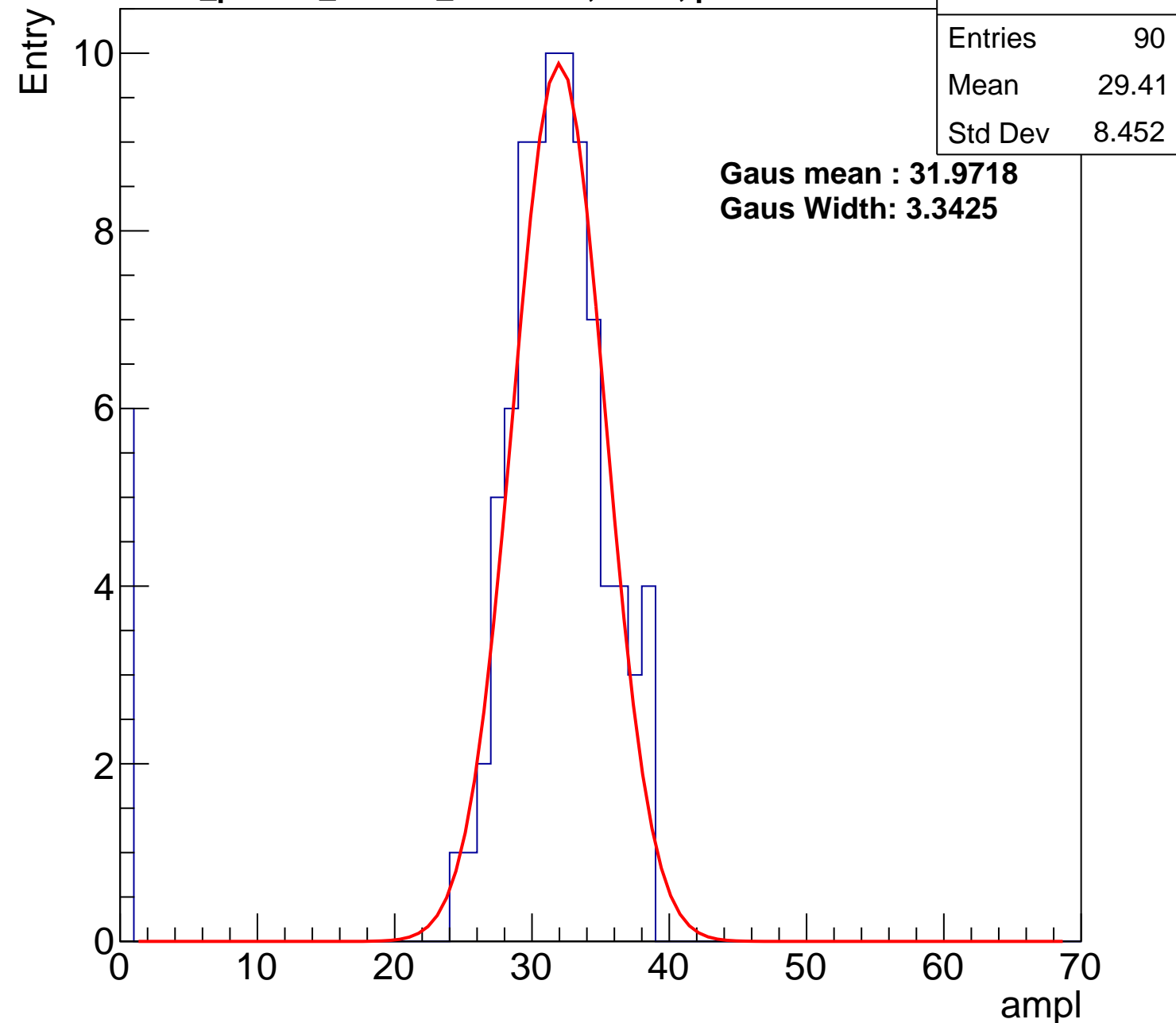
**Gaus Width: 3.3425**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U2-ch4, adc1

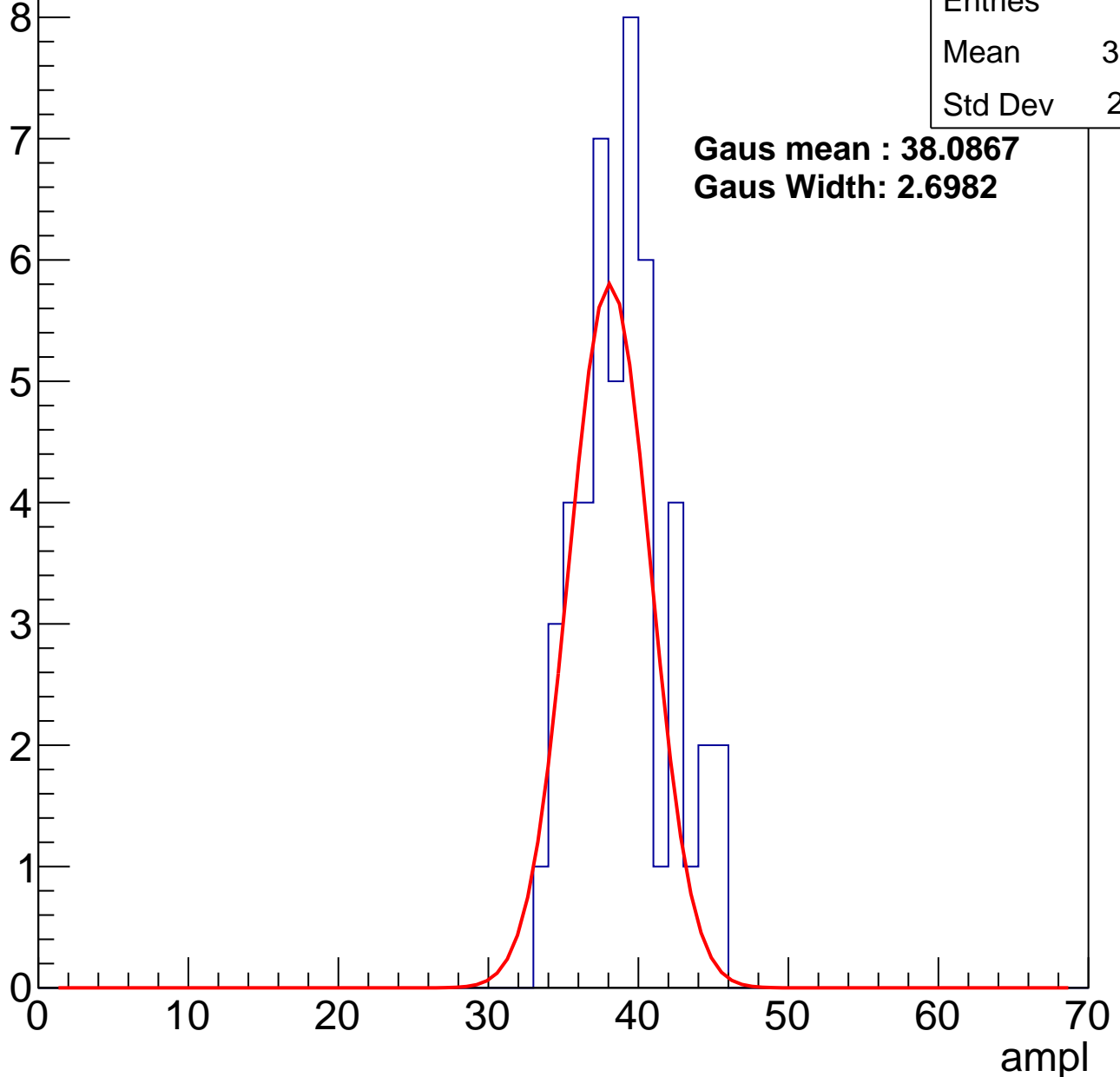
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 48    |
| Mean    | 38.54 |
| Std Dev | 2.951 |

**Gaus mean : 38.0867**

**Gaus Width: 2.6982**



# B0L001S, U2-ch4, adc2

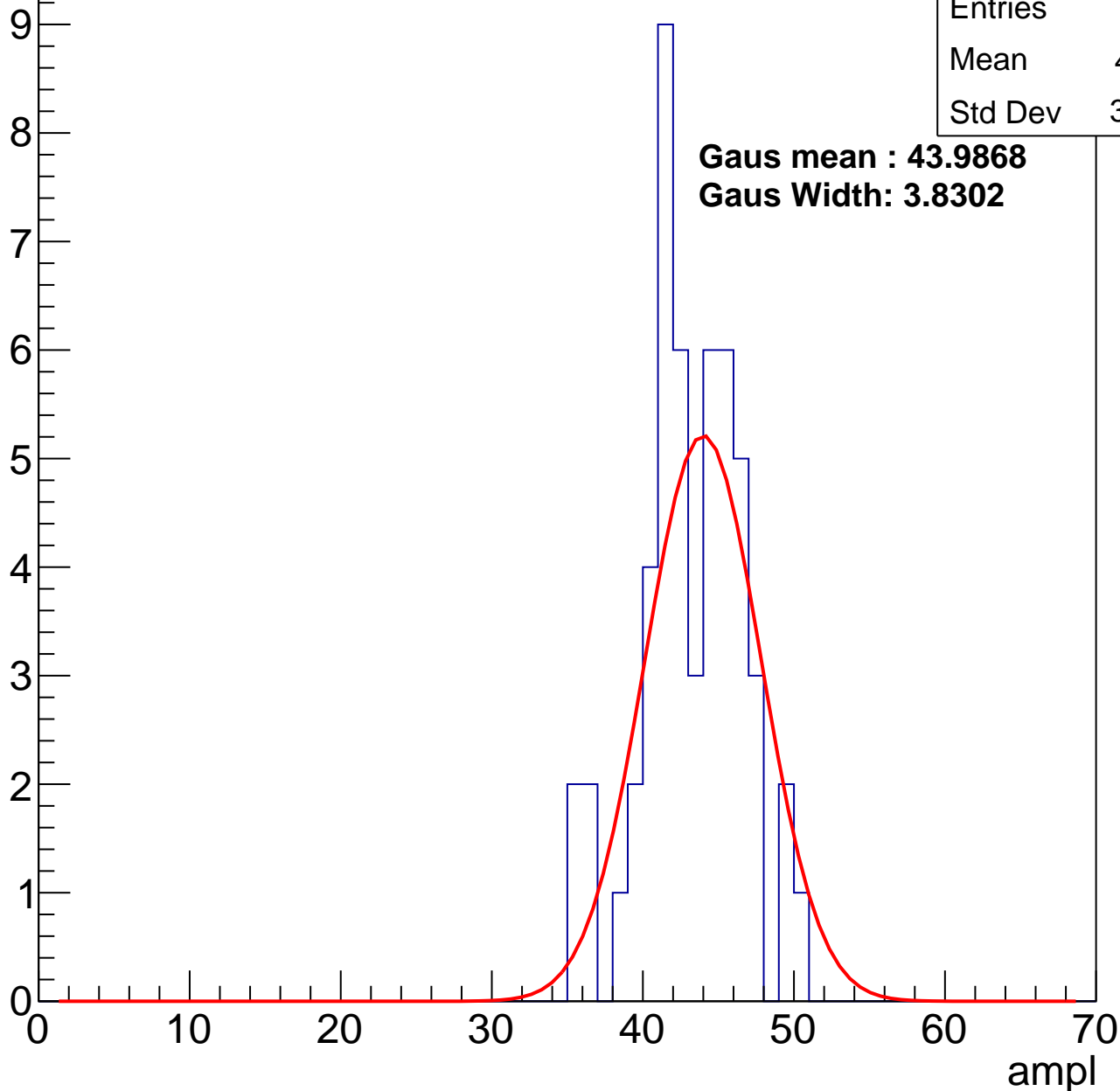
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 52    |
| Mean    | 42.71 |
| Std Dev | 3.399 |

**Gaus mean : 43.9868**

**Gaus Width: 3.8302**



# B0L001S, U2-ch4, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

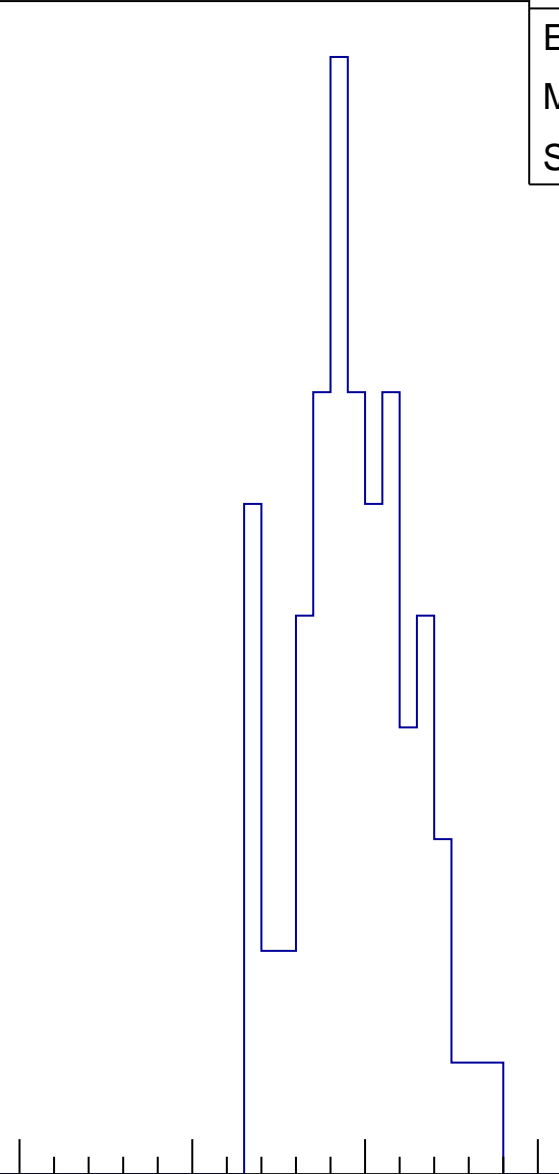
|         |       |
|---------|-------|
| Entries | 67    |
| Mean    | 48.93 |
| Std Dev | 3.356 |

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

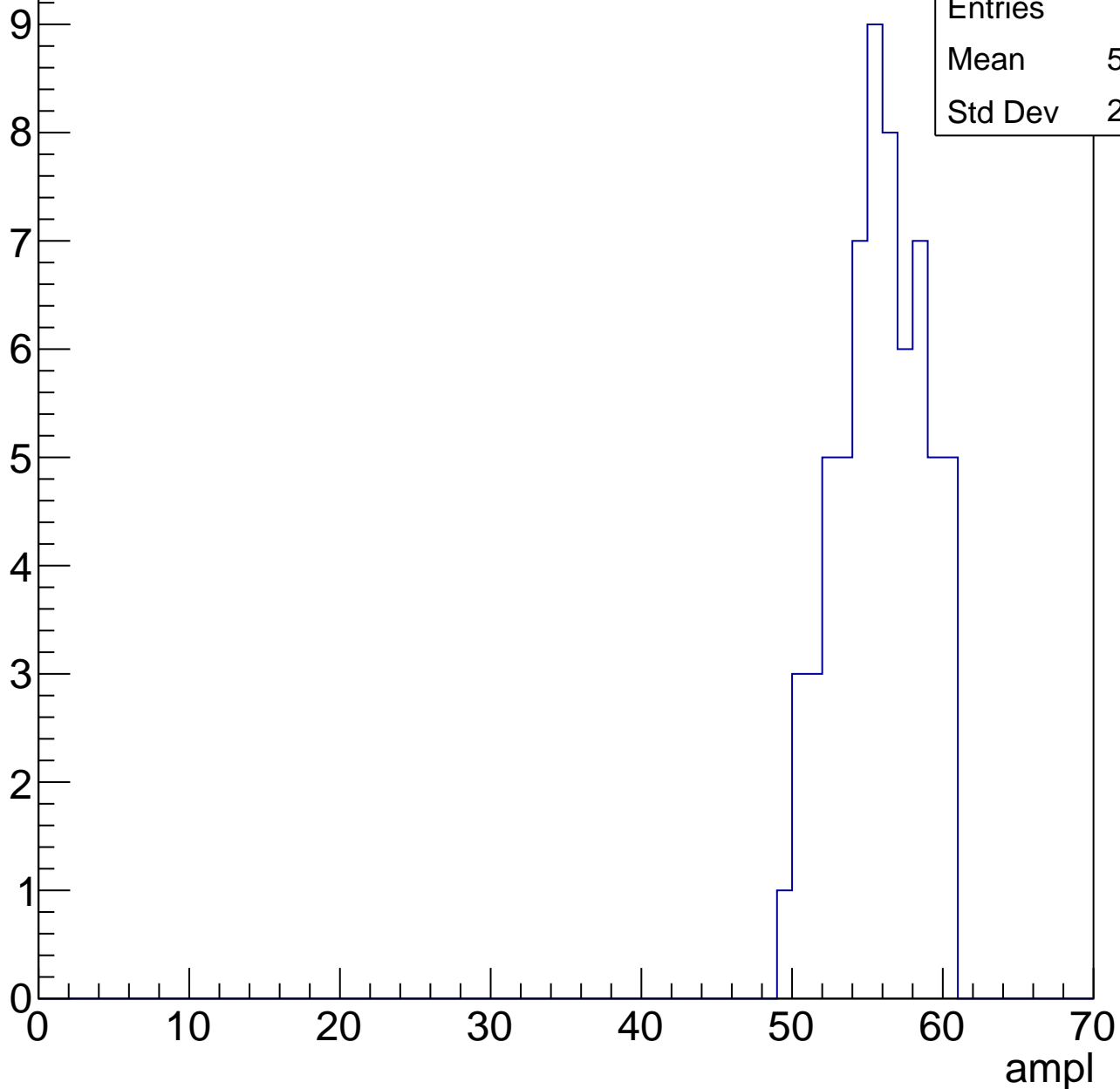
ampl



# B0L001S, U2-ch4, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



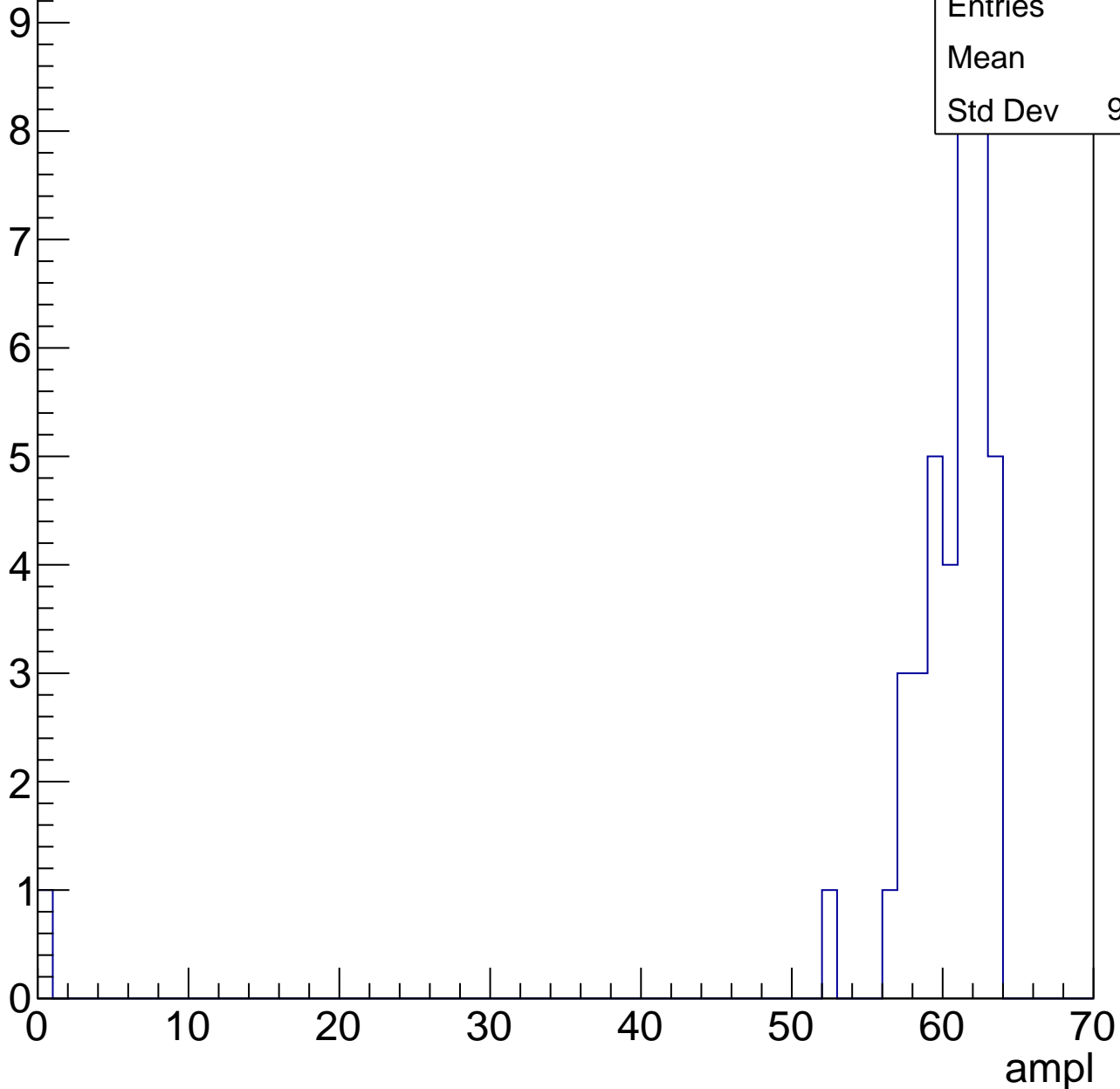
|         |       |
|---------|-------|
| Entries | 64    |
| Mean    | 55.33 |
| Std Dev | 2.862 |

# B0L001S, U2-ch4, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 40    |
| Mean    | 58.7  |
| Std Dev | 9.673 |

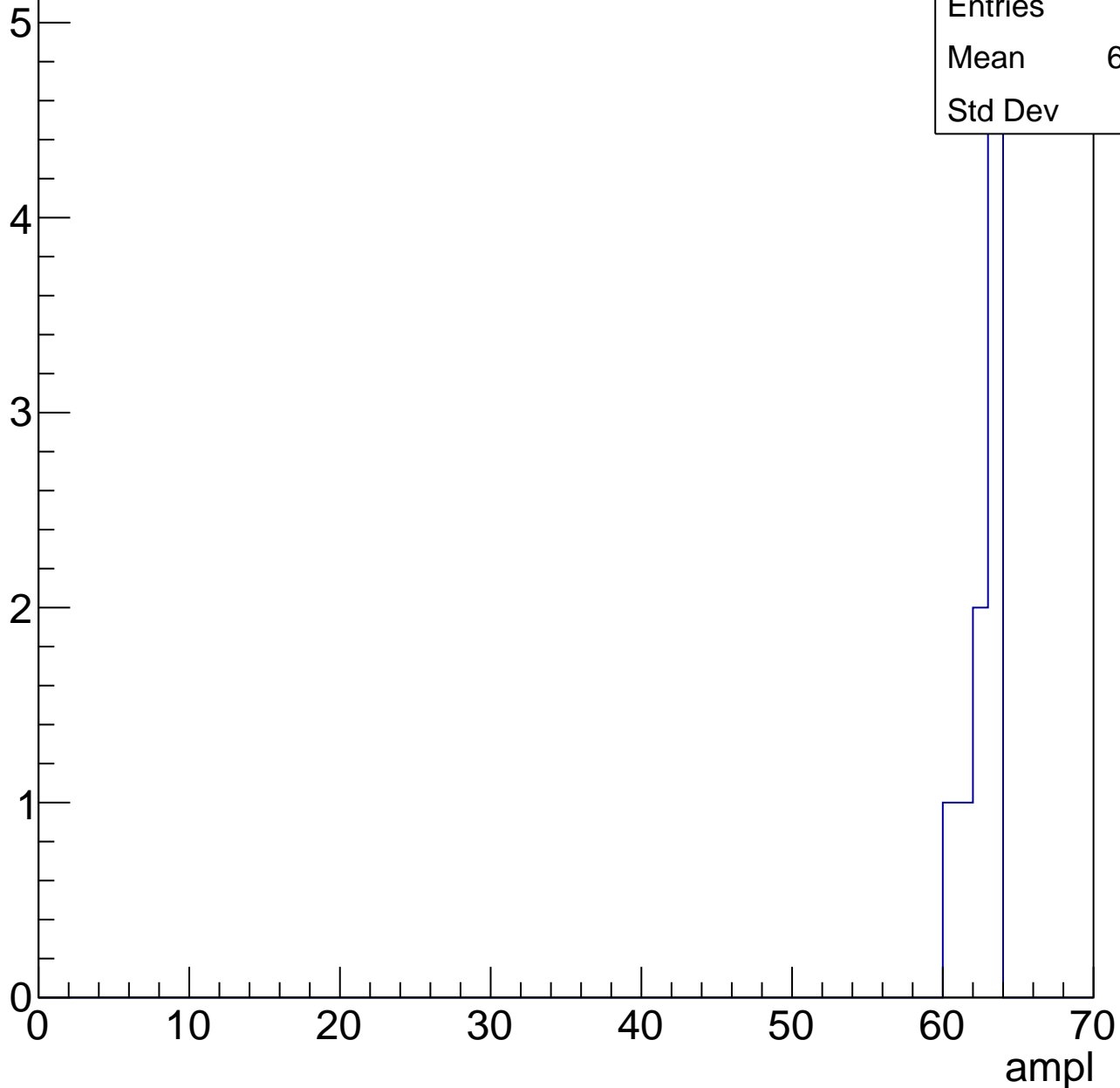


# B0L001S, U2-ch4, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 9     |
| Mean    | 62.22 |
| Std Dev | 1.03  |





# B0L001S, U2-ch4, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U2-ch5, adc0

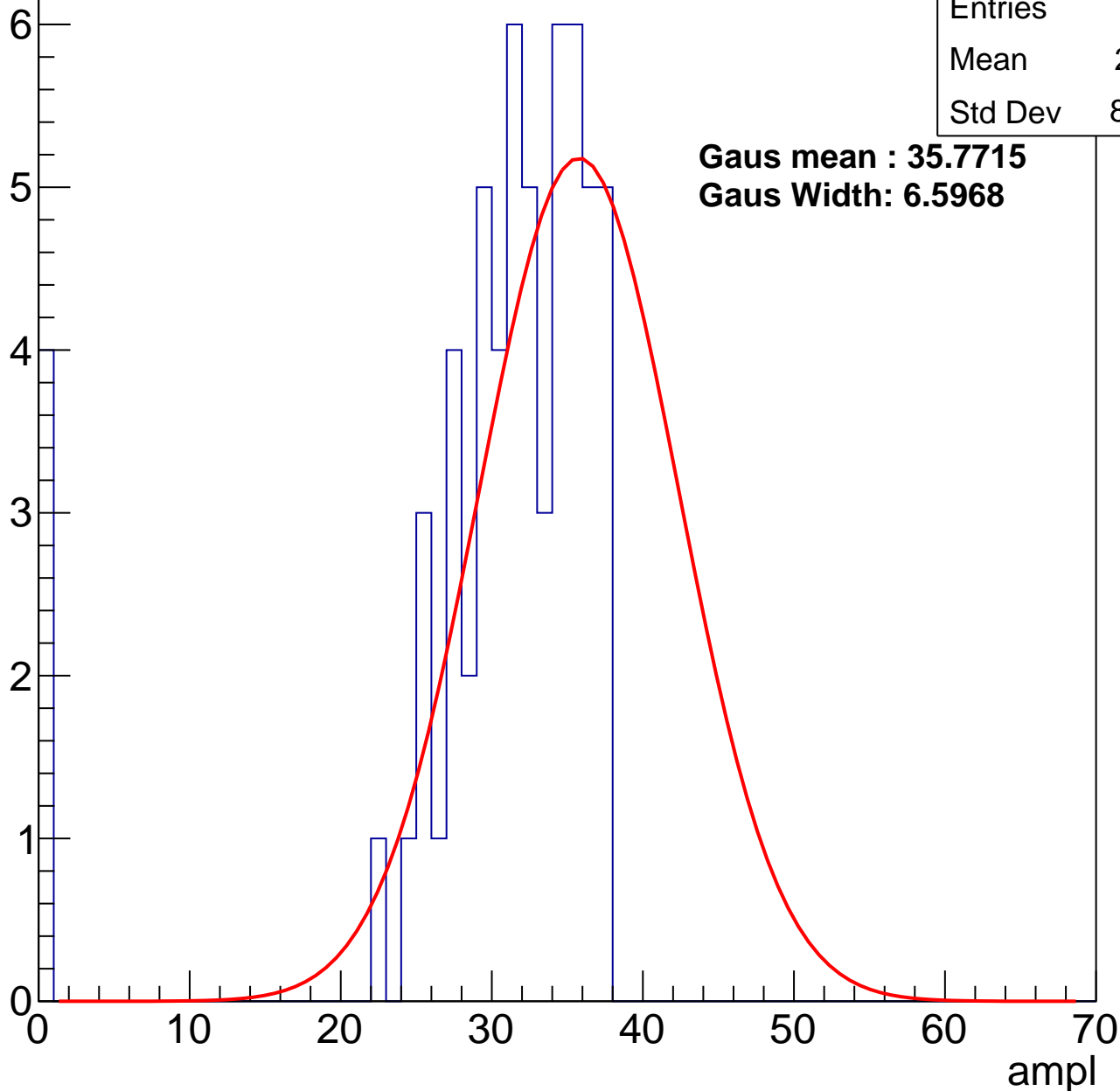
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 61    |
| Mean    | 29.51 |
| Std Dev | 8.636 |

**Gaus mean : 35.7715**

**Gaus Width: 6.5968**



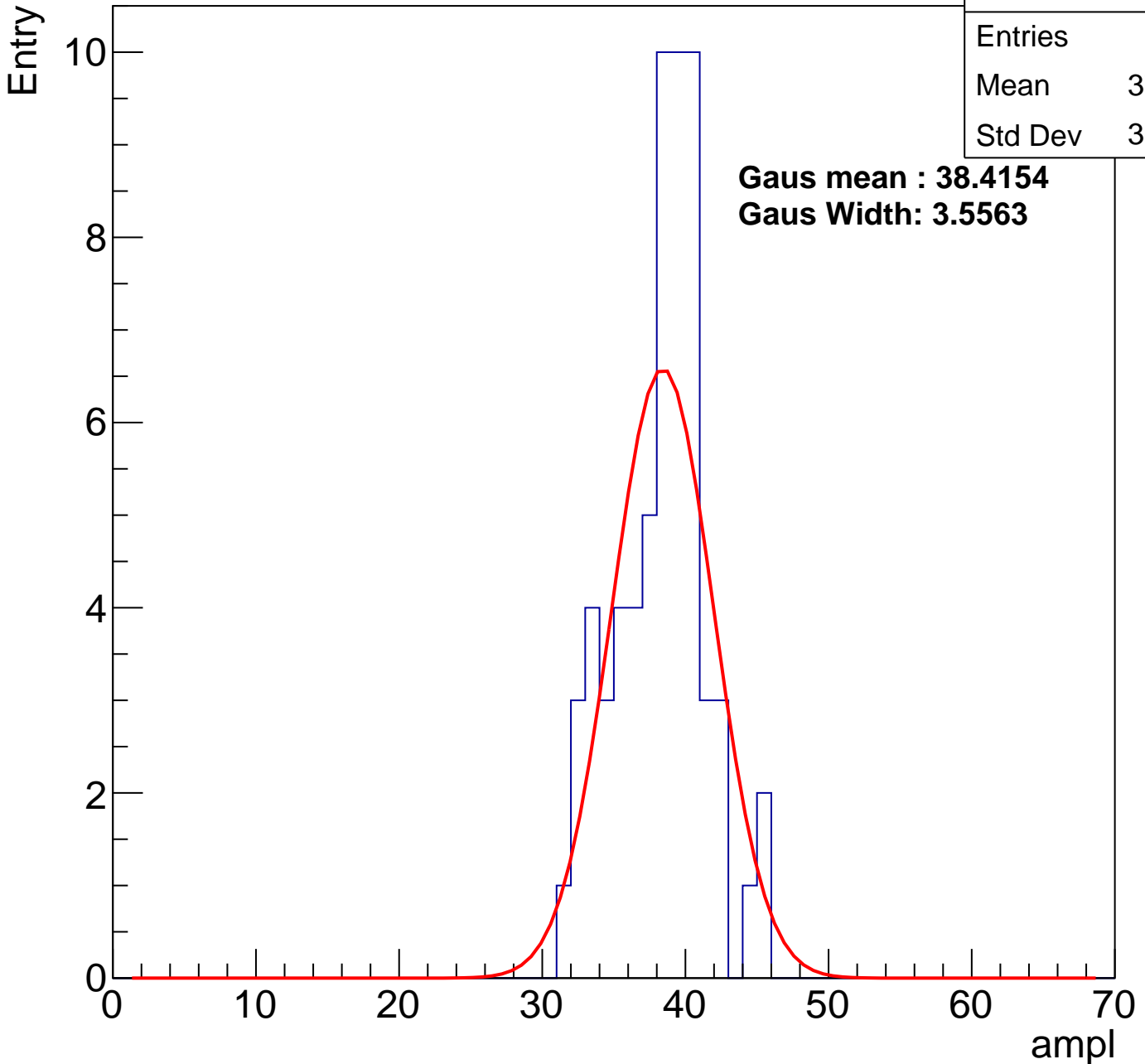
# B0L001S, U2-ch5, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 63    |
| Mean    | 37.83 |
| Std Dev | 3.135 |

**Gaus mean : 38.4154**

**Gaus Width: 3.5563**



# B0L001S, U2-ch5, adc2

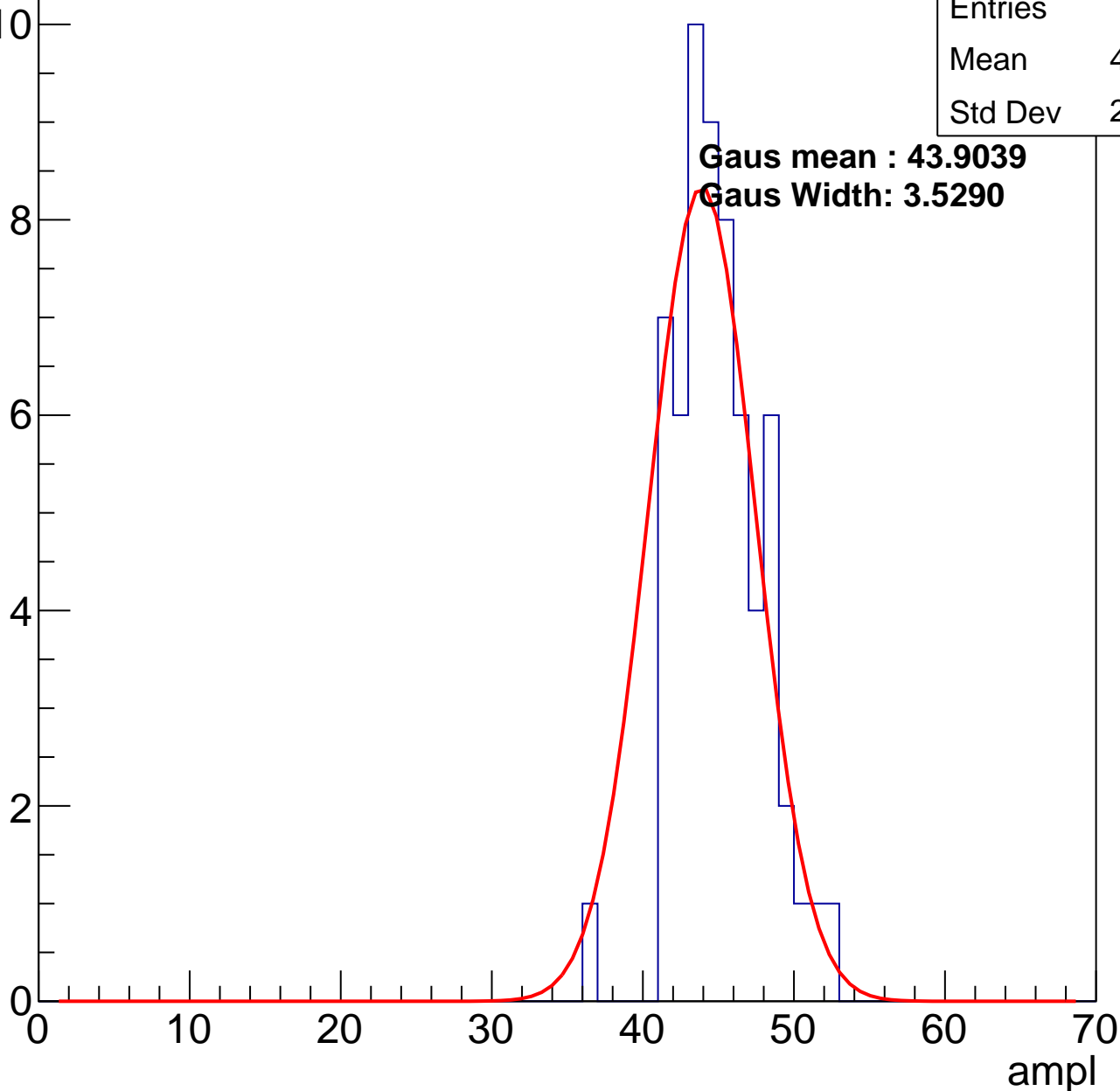
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 62    |
| Mean    | 44.58 |
| Std Dev | 2.849 |

**Gaus mean : 43.9039**

**Gaus Width: 3.5290**

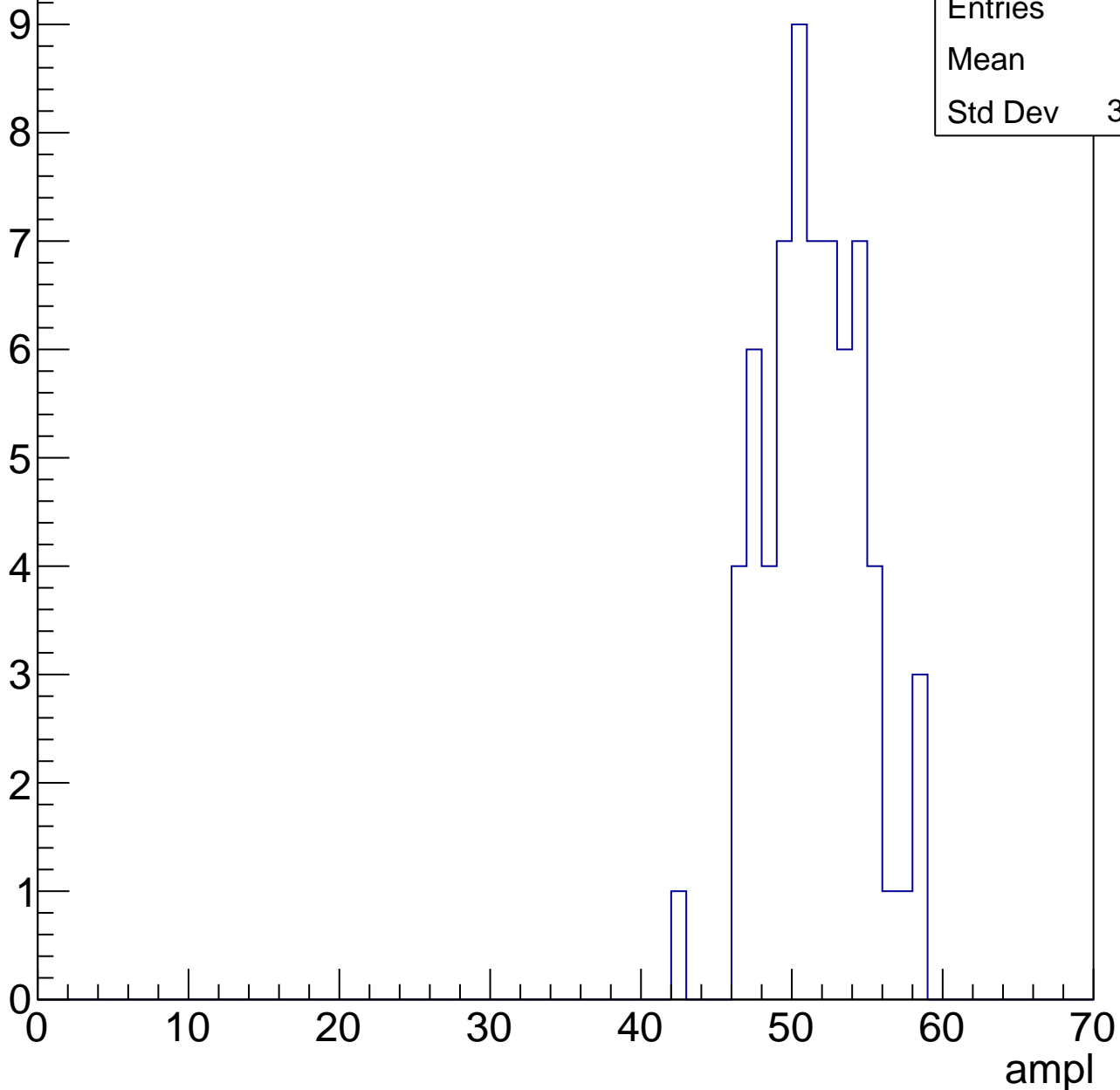


# B0L001S, U2-ch5, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 67    |
| Mean    | 51    |
| Std Dev | 3.269 |

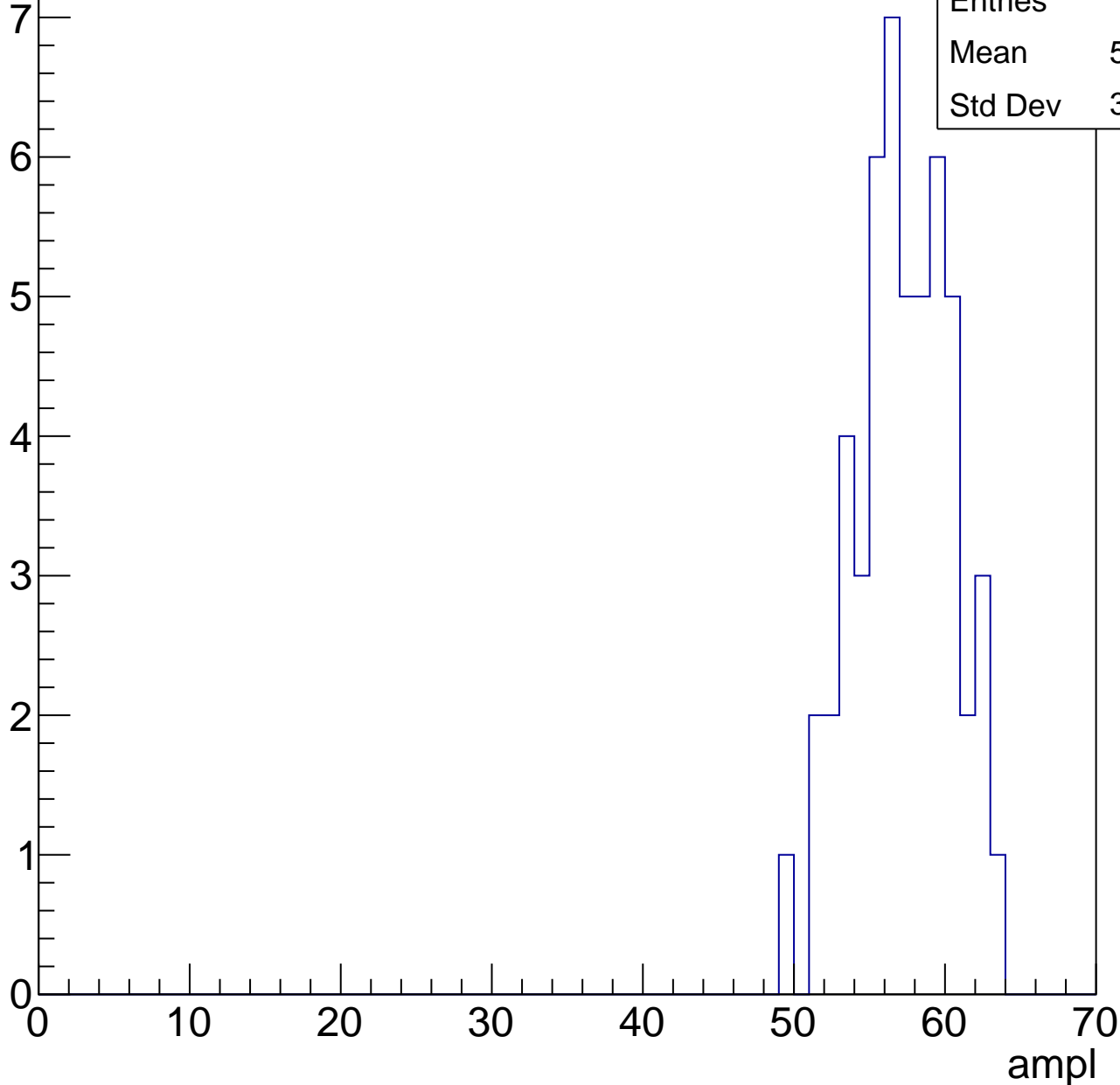


# B0L001S, U2-ch5, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 52    |
| Mean    | 56.75 |
| Std Dev | 3.168 |



# B0L001S, U2-ch5, adc5

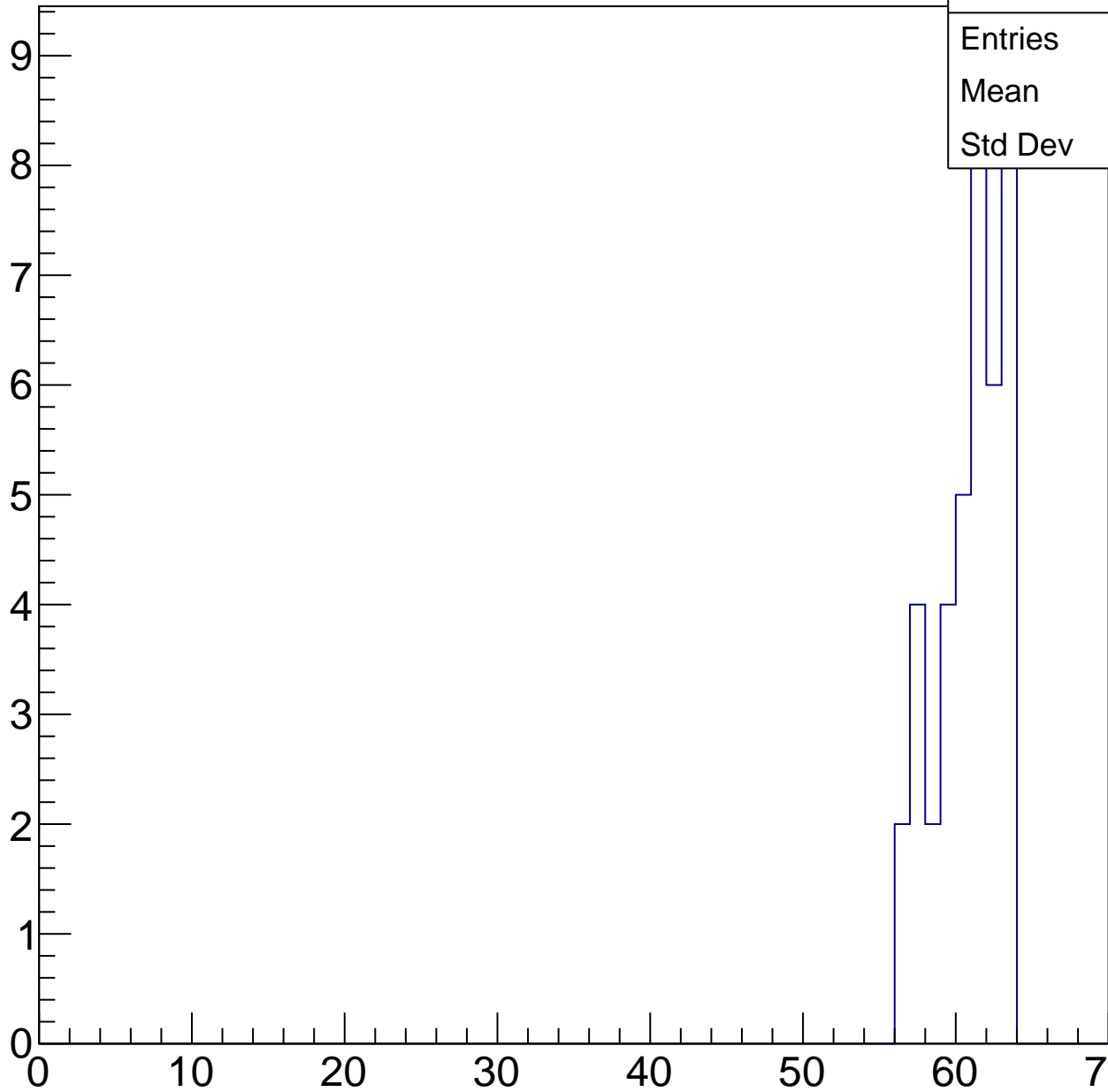
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

|         |       |
|---------|-------|
| Entries | 40    |
| Mean    | 60.48 |
| Std Dev | 2.145 |

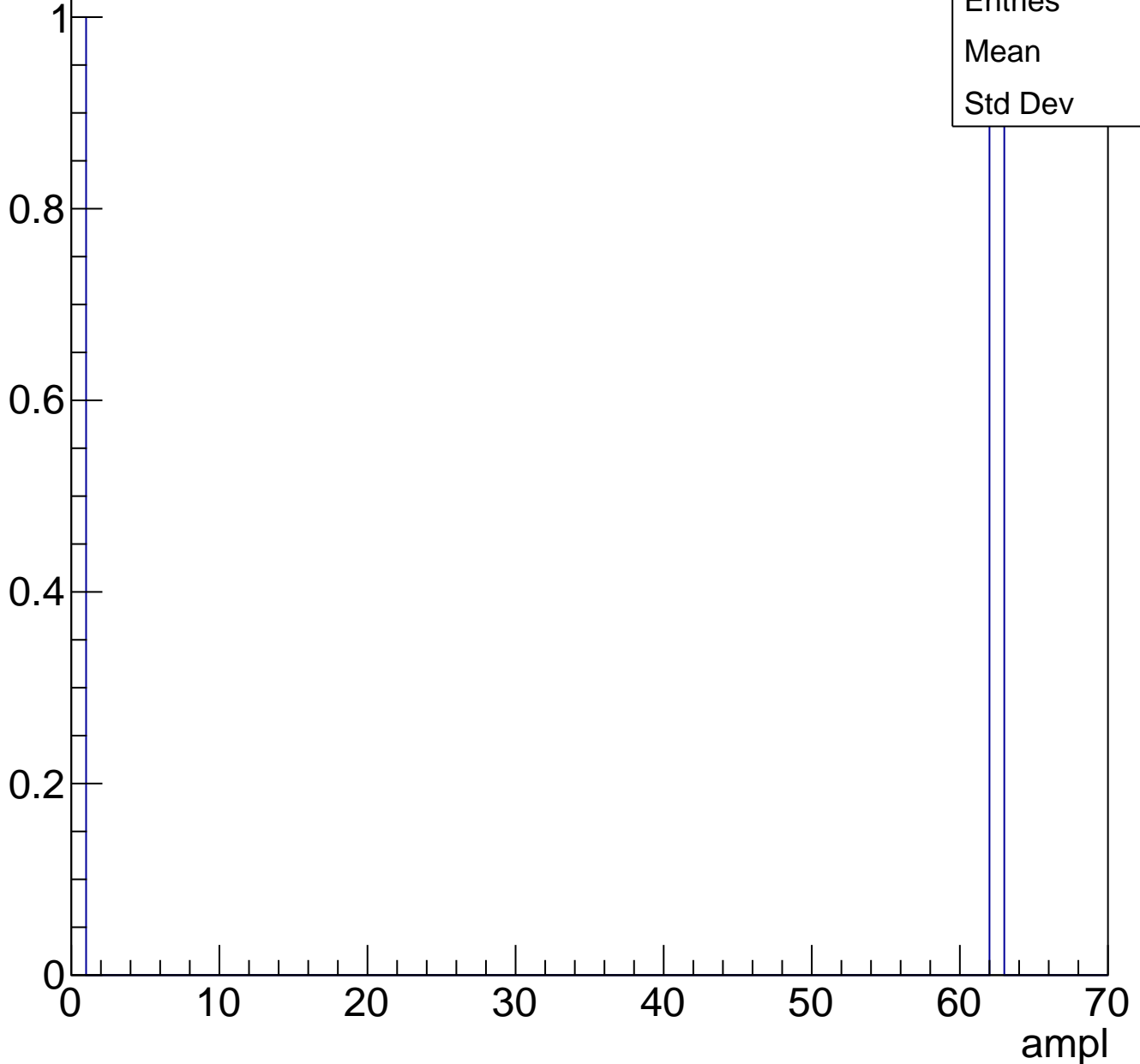
ampl



# B0L001S, U2-ch5, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch5, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 0 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch6, adc0

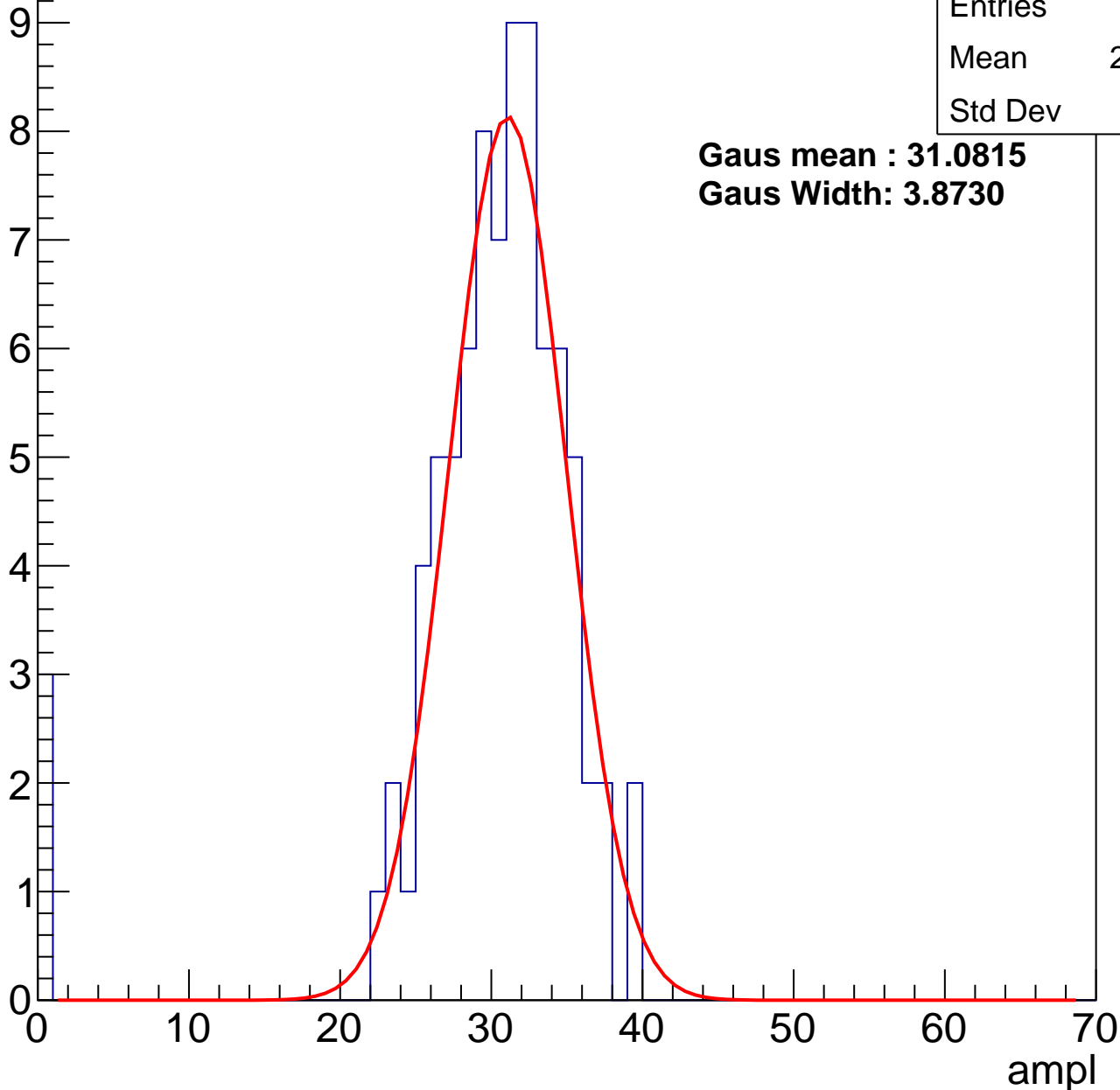
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 83    |
| Mean    | 29.34 |
| Std Dev | 6.74  |

**Gaus mean : 31.0815**

**Gaus Width: 3.8730**



# B0L001S, U2-ch6, adc1

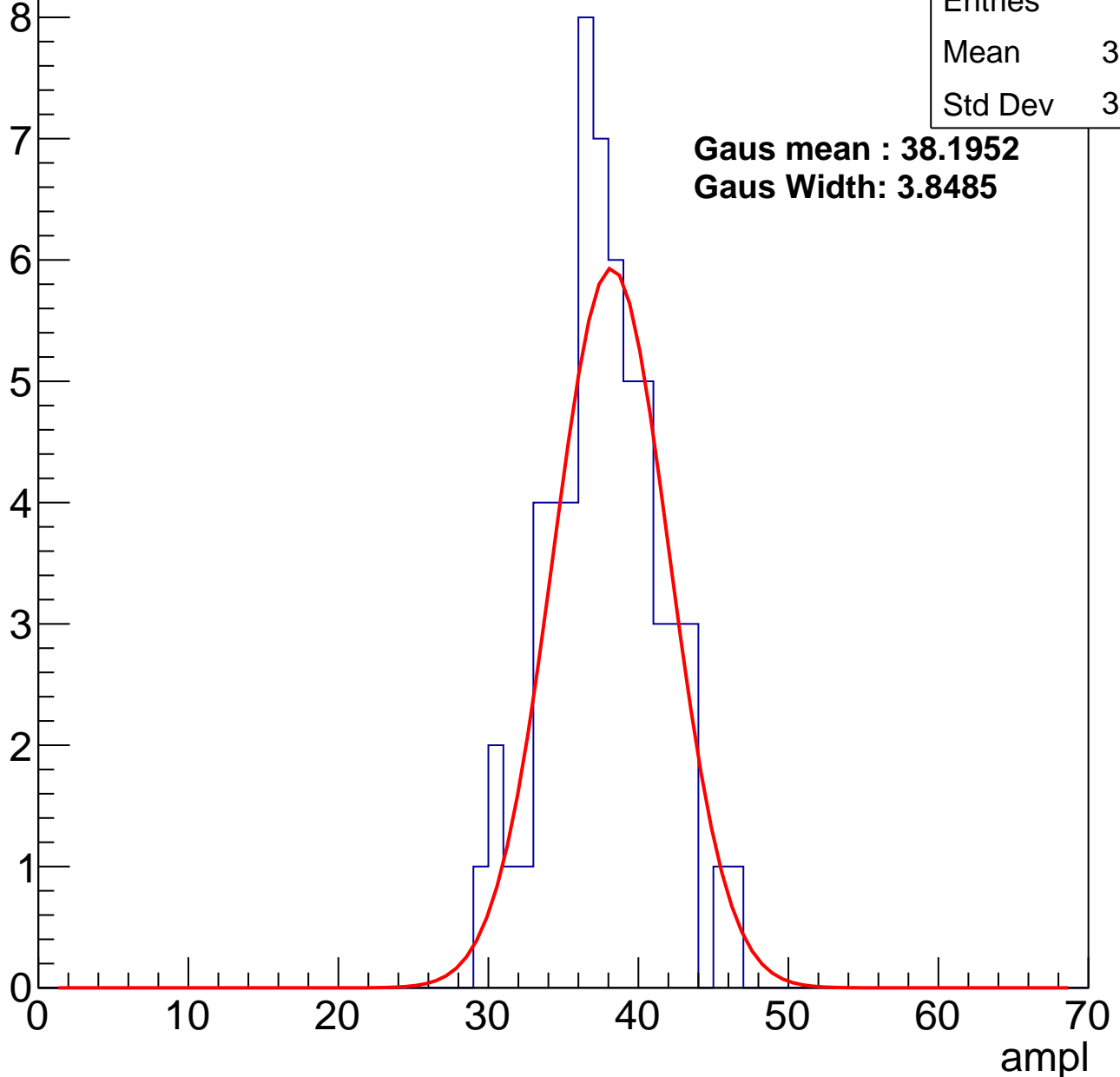
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 59    |
| Mean    | 37.27 |
| Std Dev | 3.658 |

**Gaus mean : 38.1952**

**Gaus Width: 3.8485**



# B0L001S, U2-ch6, adc2

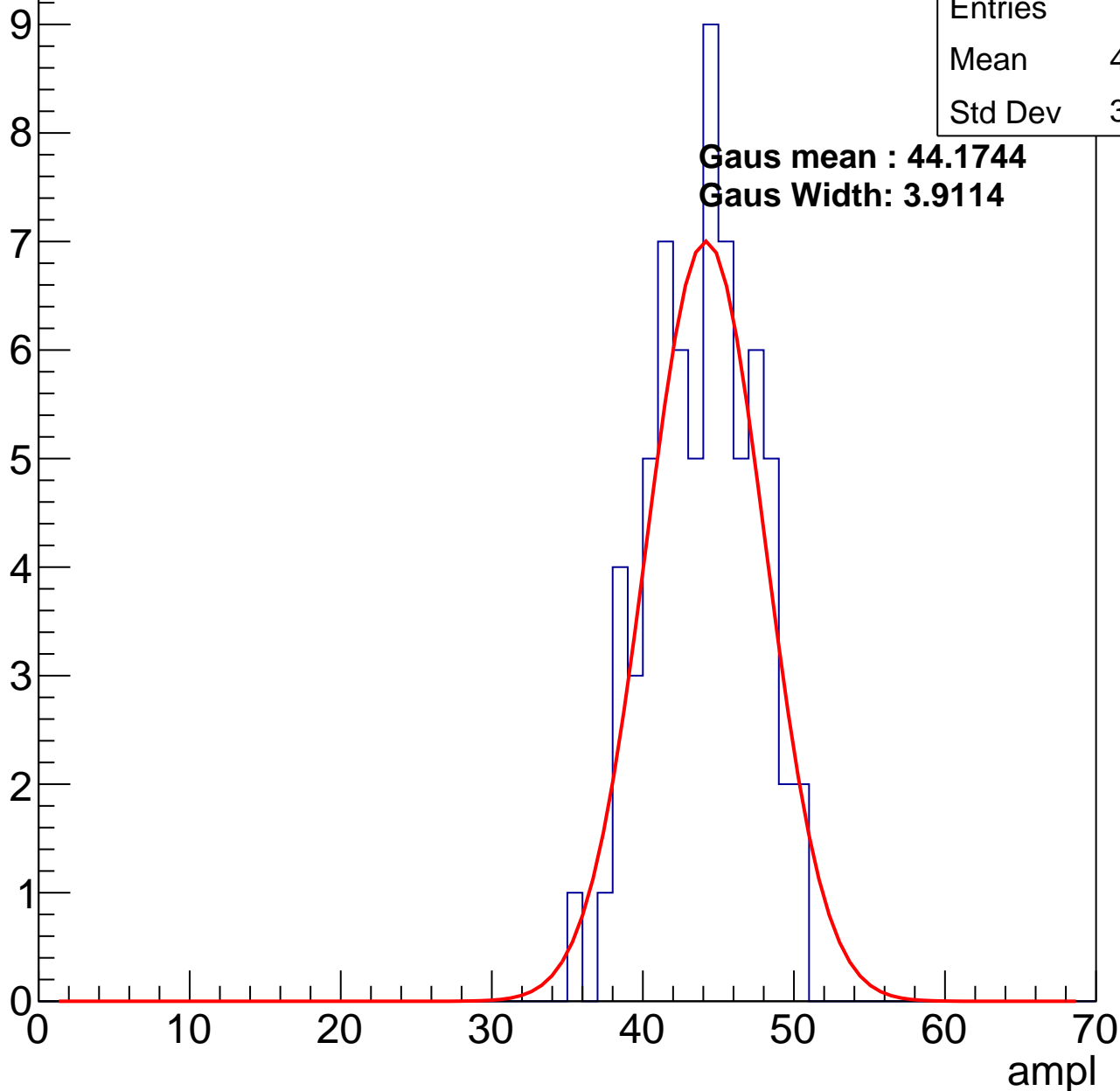
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 68    |
| Mean    | 43.47 |
| Std Dev | 3.398 |

**Gaus mean : 44.1744**

**Gaus Width: 3.9114**

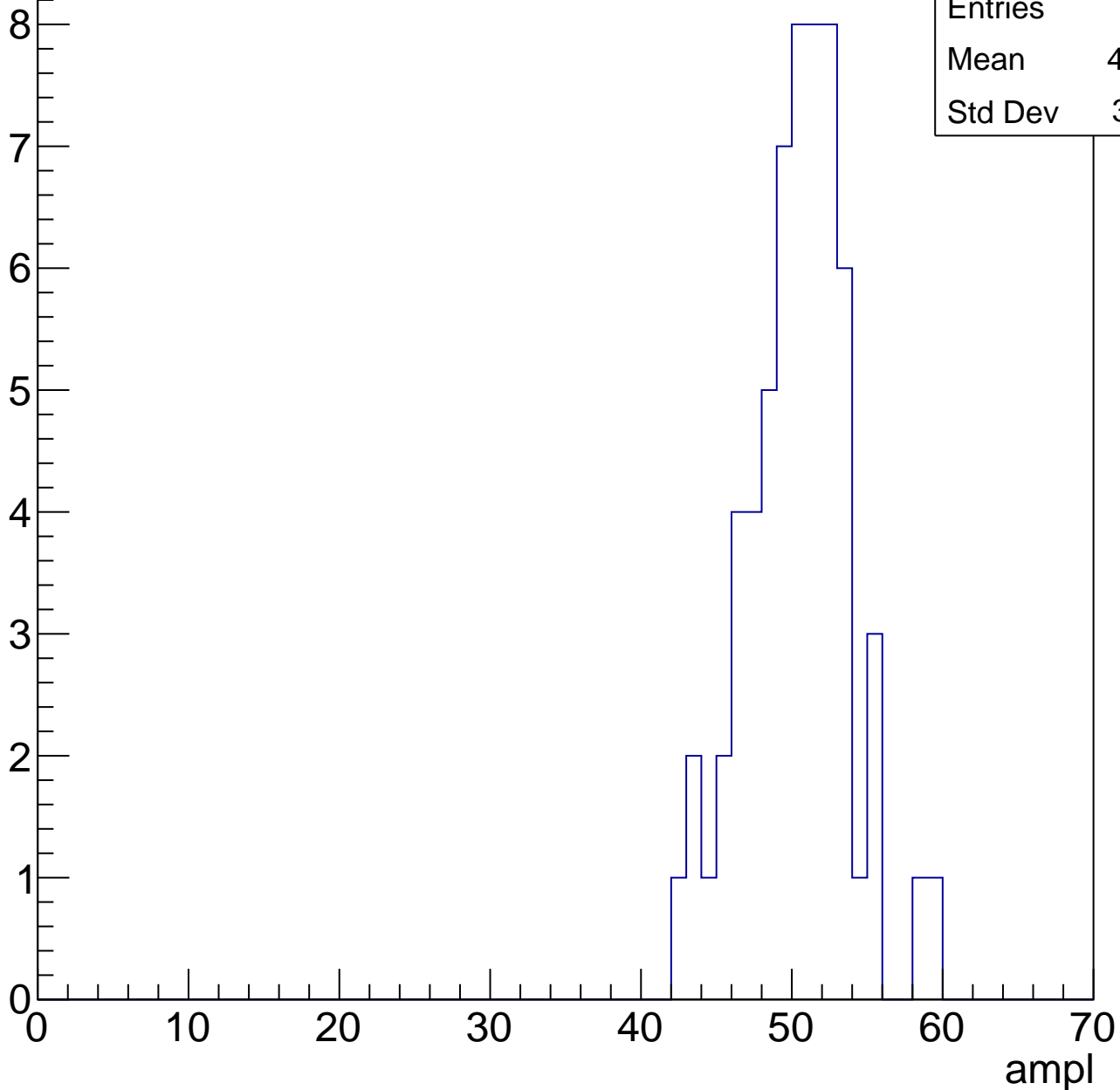


# B0L001S, U2-ch6, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 62    |
| Mean    | 49.92 |
| Std Dev | 3.371 |

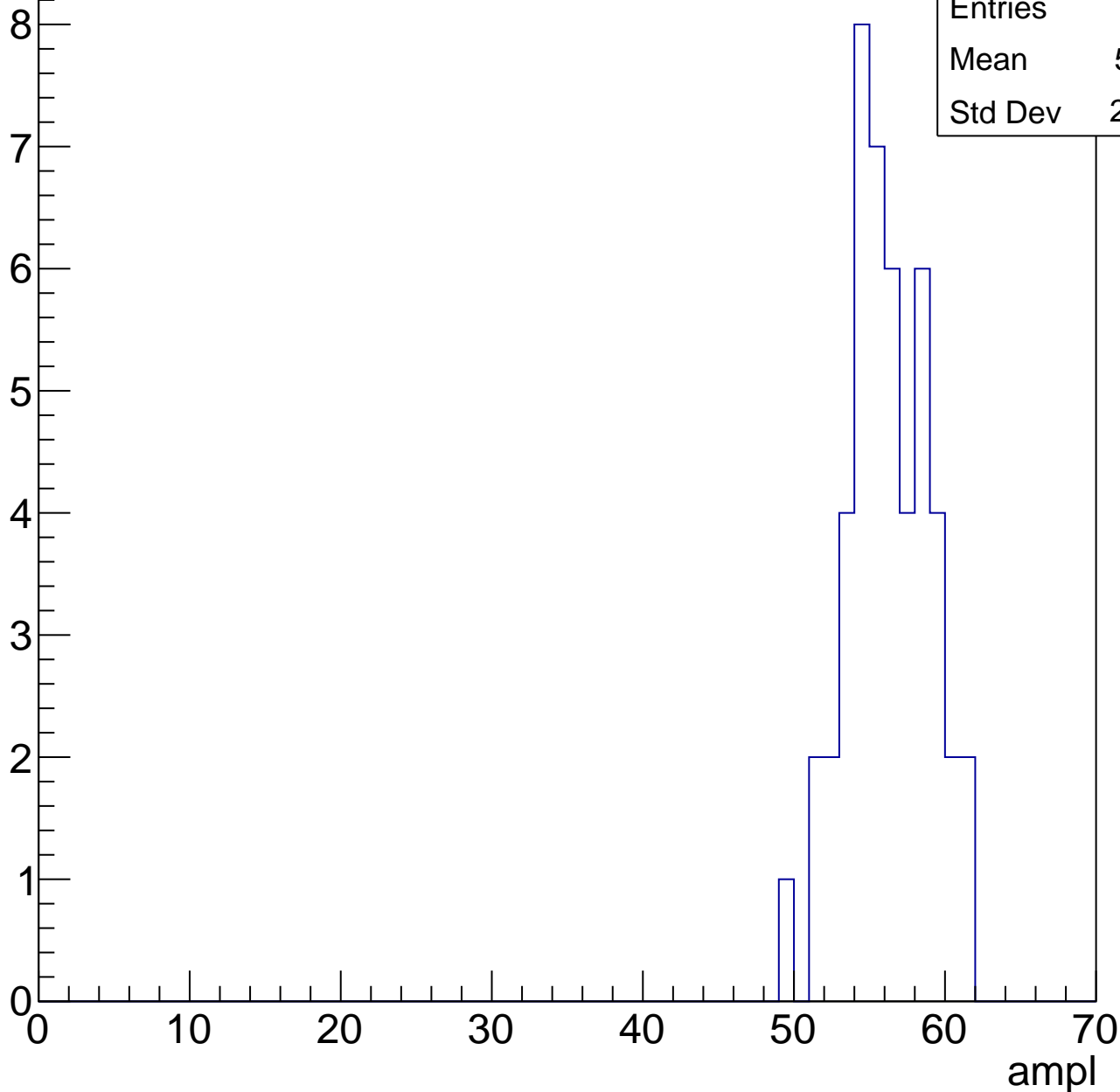


# B0L001S, U2-ch6, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 48    |
| Mean    | 55.71 |
| Std Dev | 2.692 |



# B0L001S, U2-ch6, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 52    |
| Mean    | 58.75 |
| Std Dev | 8.539 |

Entry

10

8

6

4

2

0

0

10

20

30

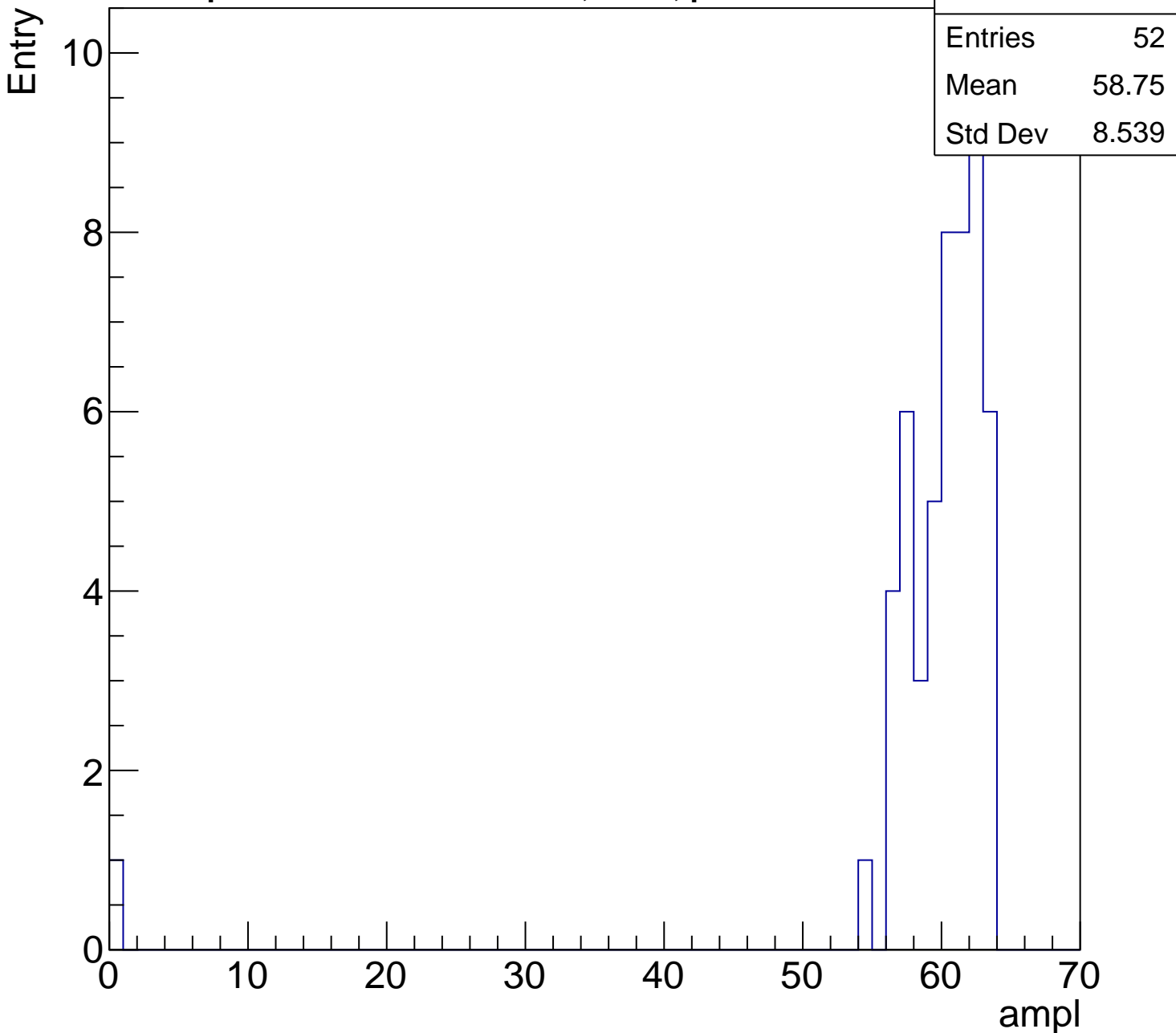
40

50

60

70

ampl



# B0L001S, U2-ch6, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch6, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 0 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch7, adc0

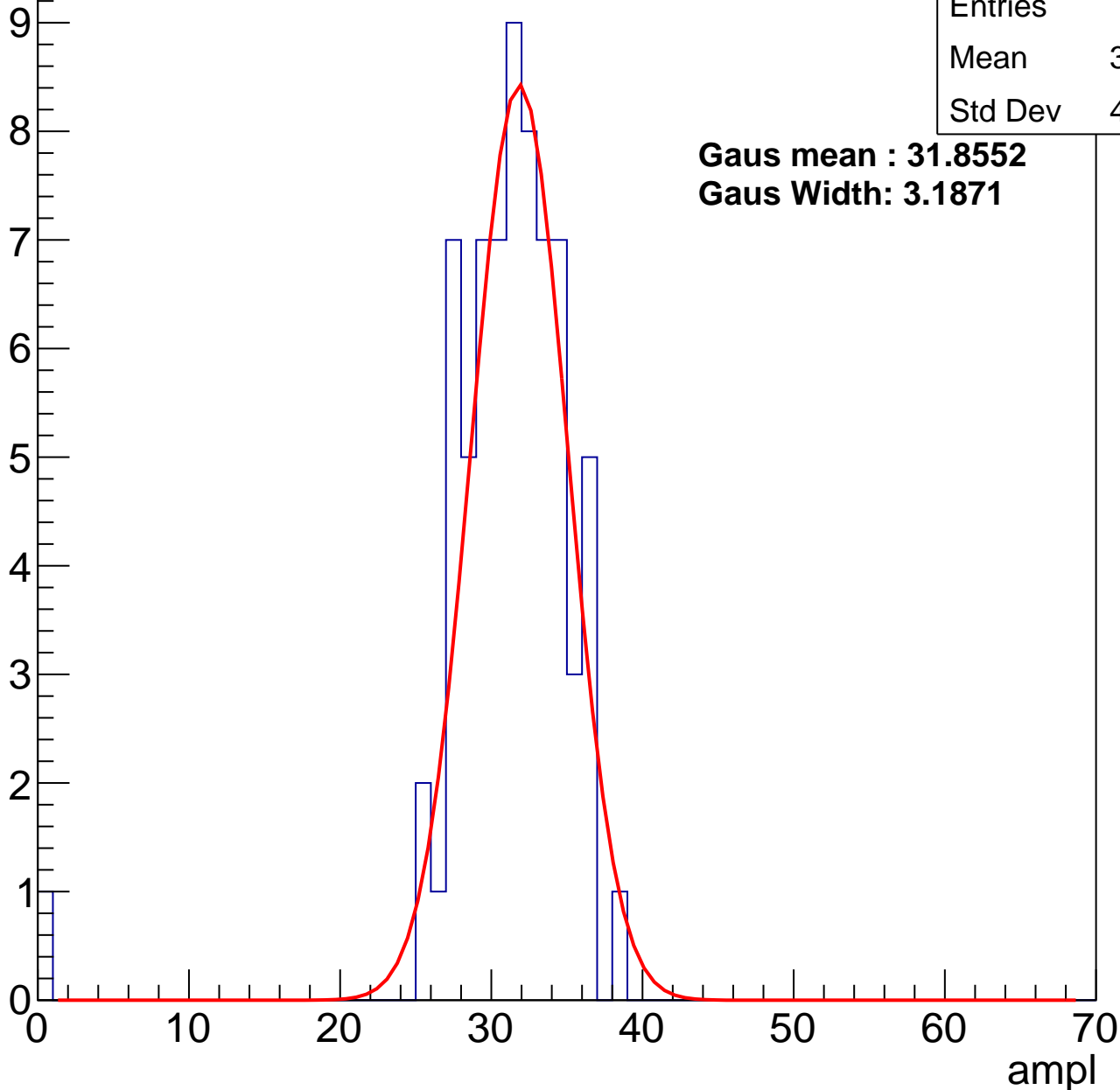
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 70    |
| Mean    | 30.64 |
| Std Dev | 4.724 |

**Gaus mean : 31.8552**

**Gaus Width: 3.1871**



# B0L001S, U2-ch7, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 69    |
| Mean    | 37.46 |
| Std Dev | 3.549 |

**Gaus mean : 38.0463**

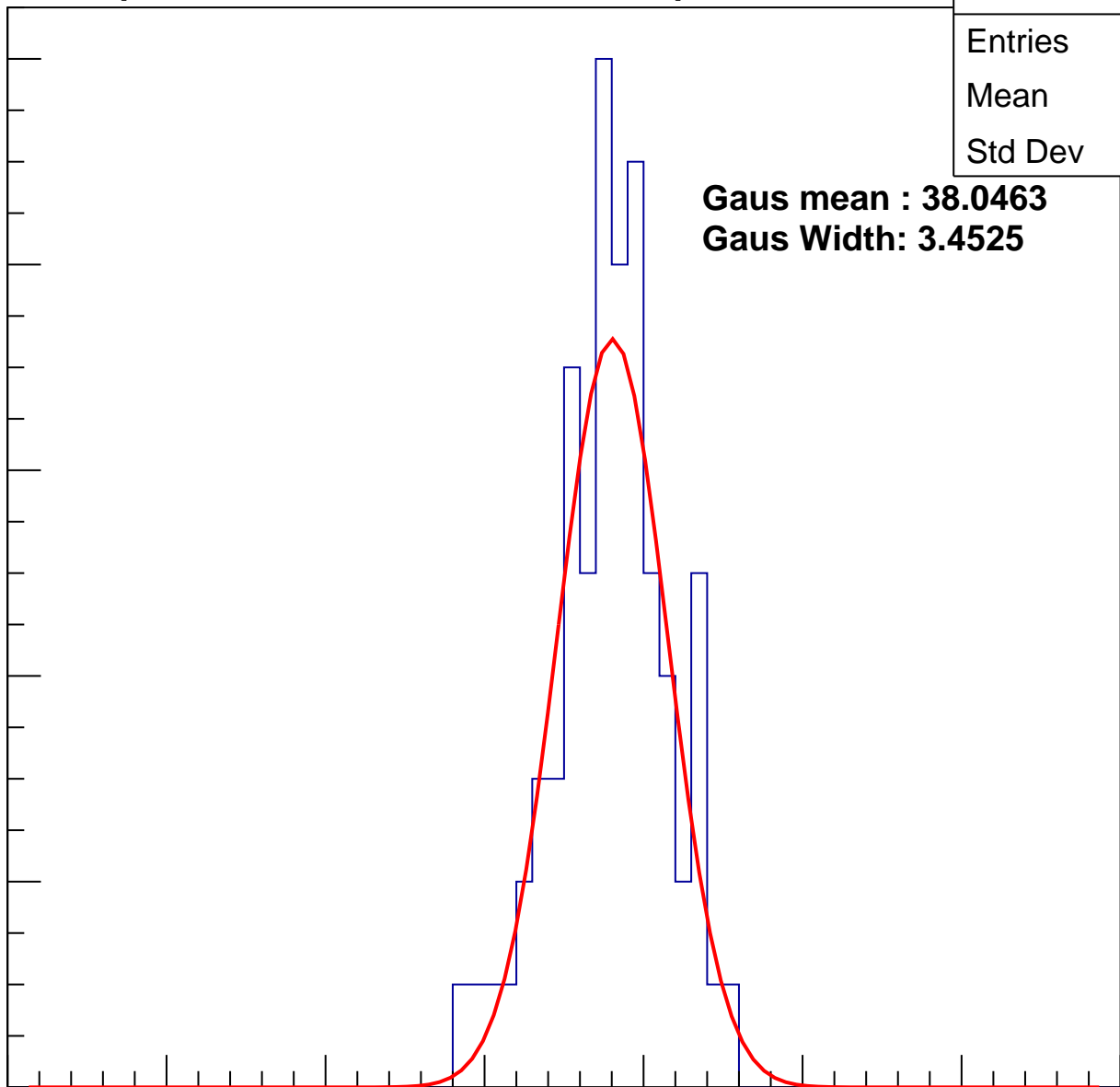
**Gaus Width: 3.4525**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U2-ch7, adc2

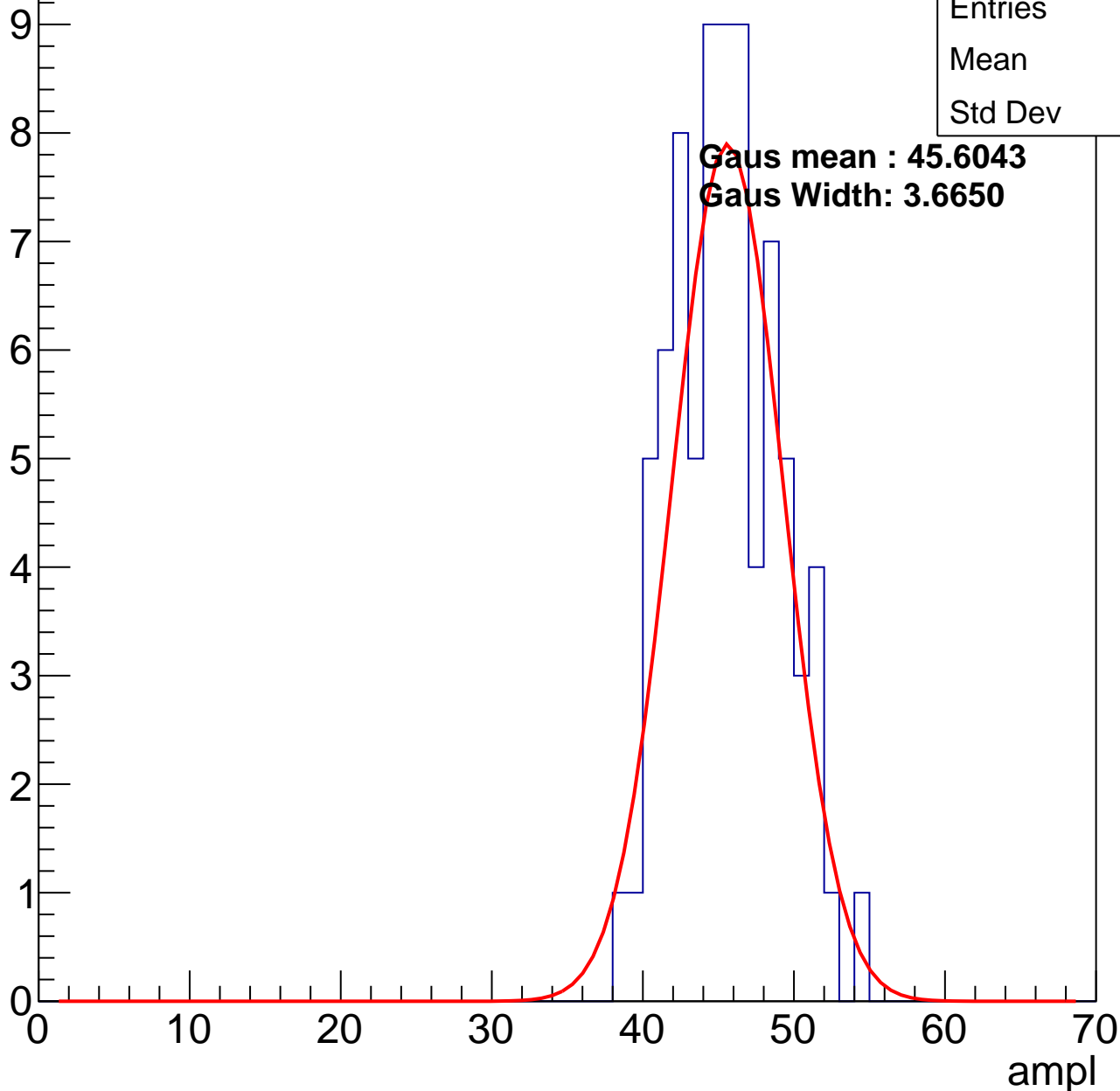
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |      |
|---------|------|
| Entries | 78   |
| Mean    | 45.1 |
| Std Dev | 3.44 |

**Gaus mean : 45.6043**

**Gaus Width: 3.6650**

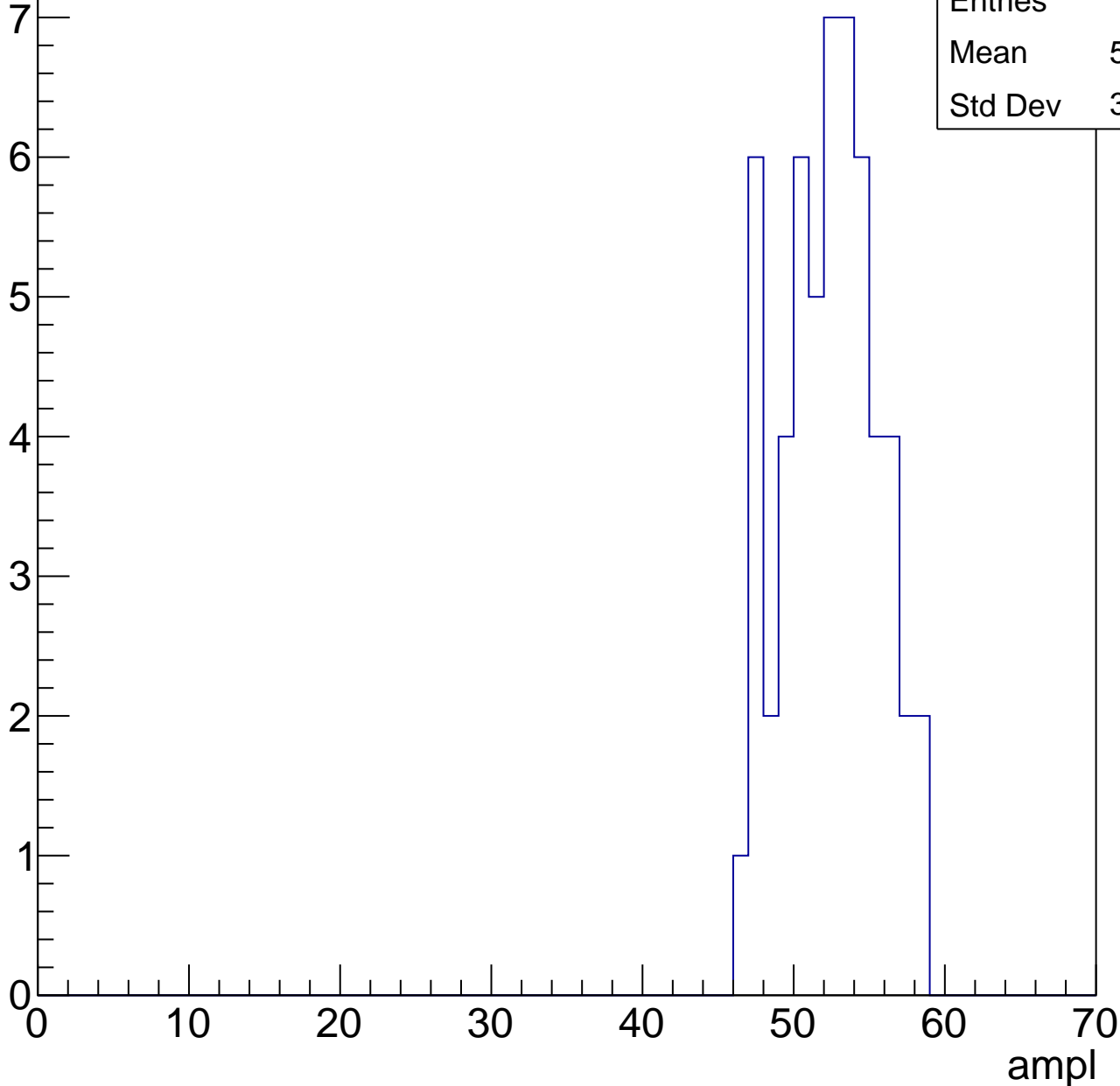


# B0L001S, U2-ch7, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 56    |
| Mean    | 51.93 |
| Std Dev | 3.093 |

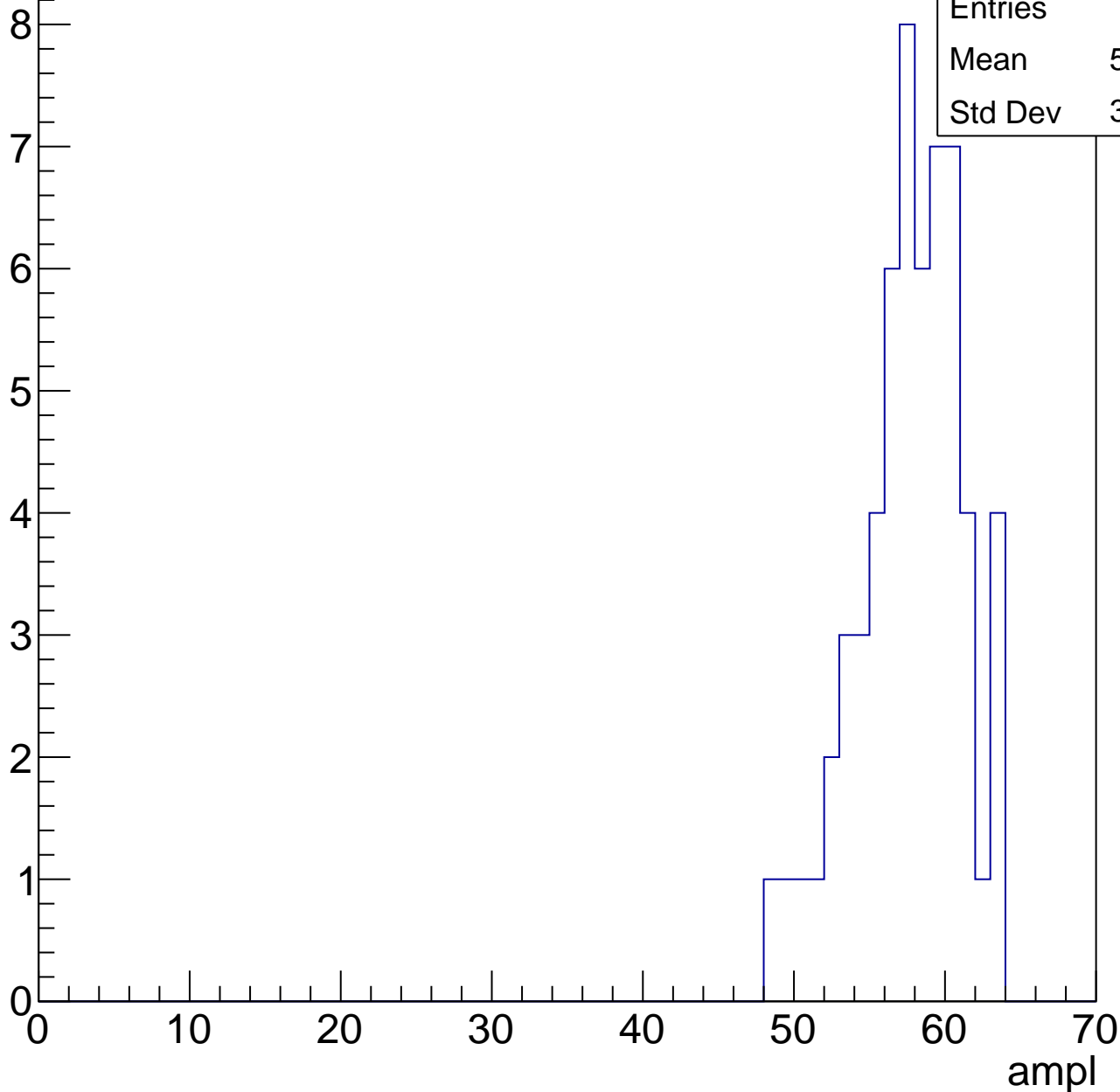


# B0L001S, U2-ch7, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 59    |
| Mean    | 57.19 |
| Std Dev | 3.457 |

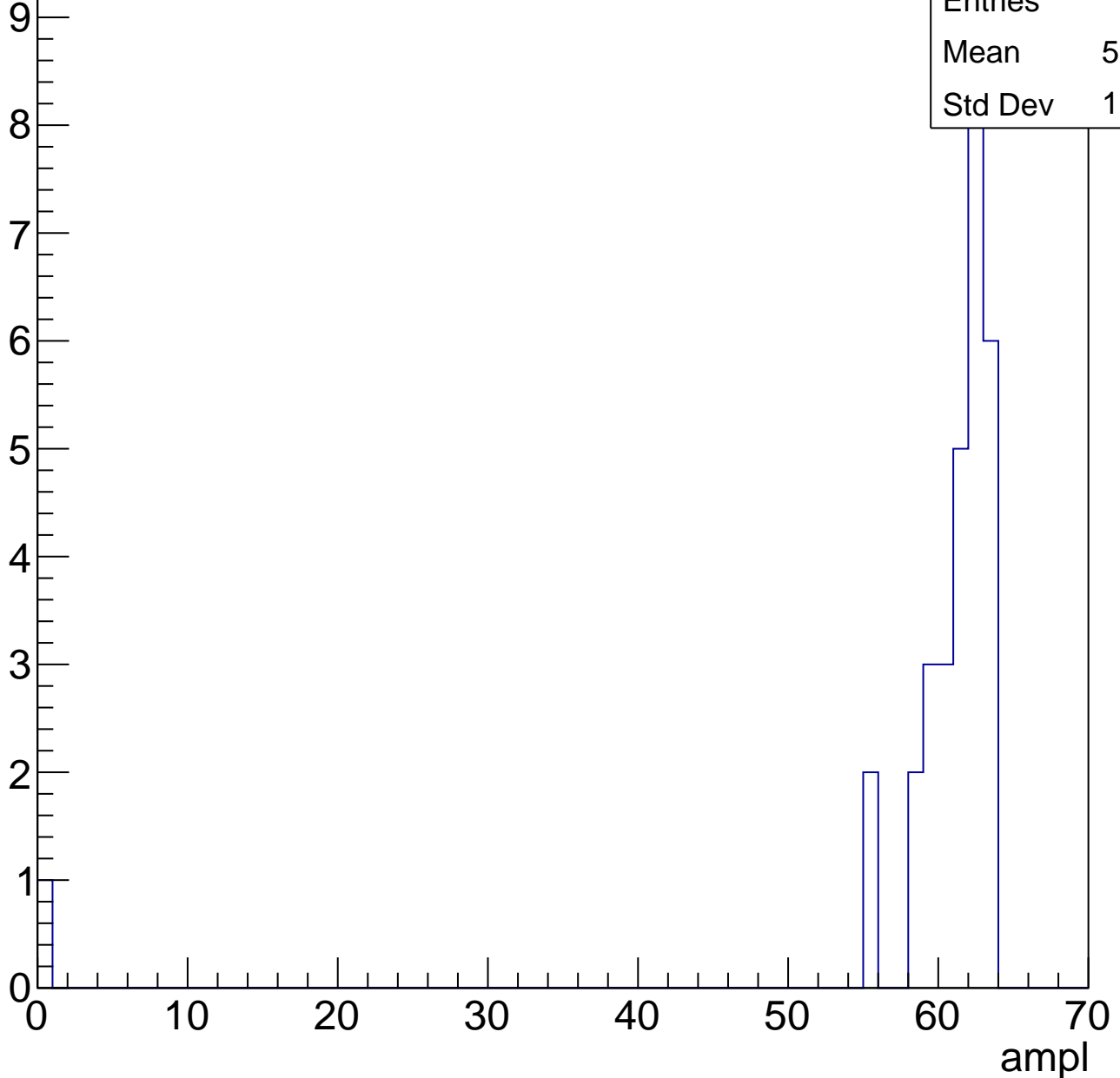


# B0L001S, U2-ch7, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

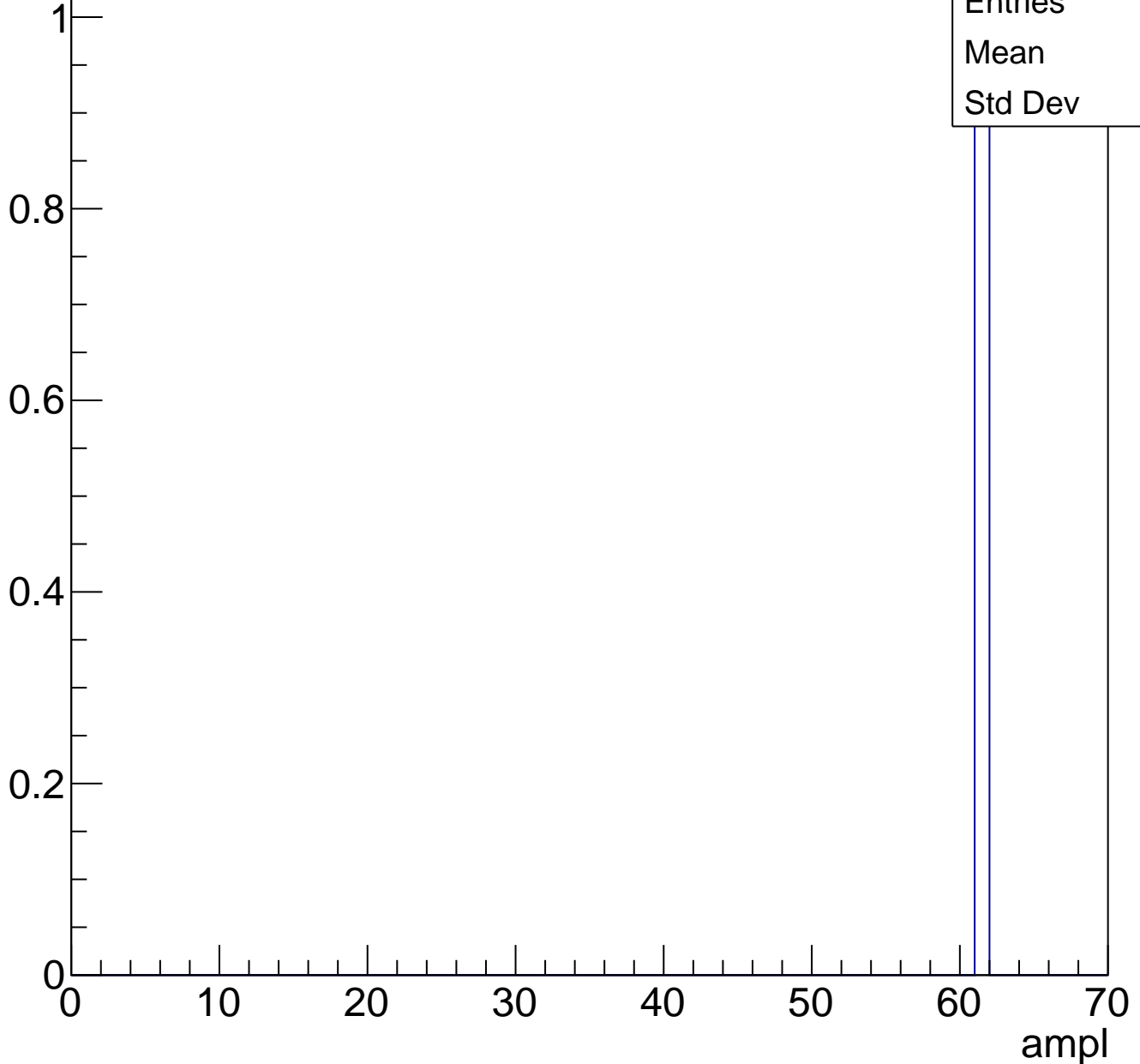
|         |       |
|---------|-------|
| Entries | 31    |
| Mean    | 58.84 |
| Std Dev | 10.95 |



# B0L001S, U2-ch7, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch7, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 1 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch8, adc0

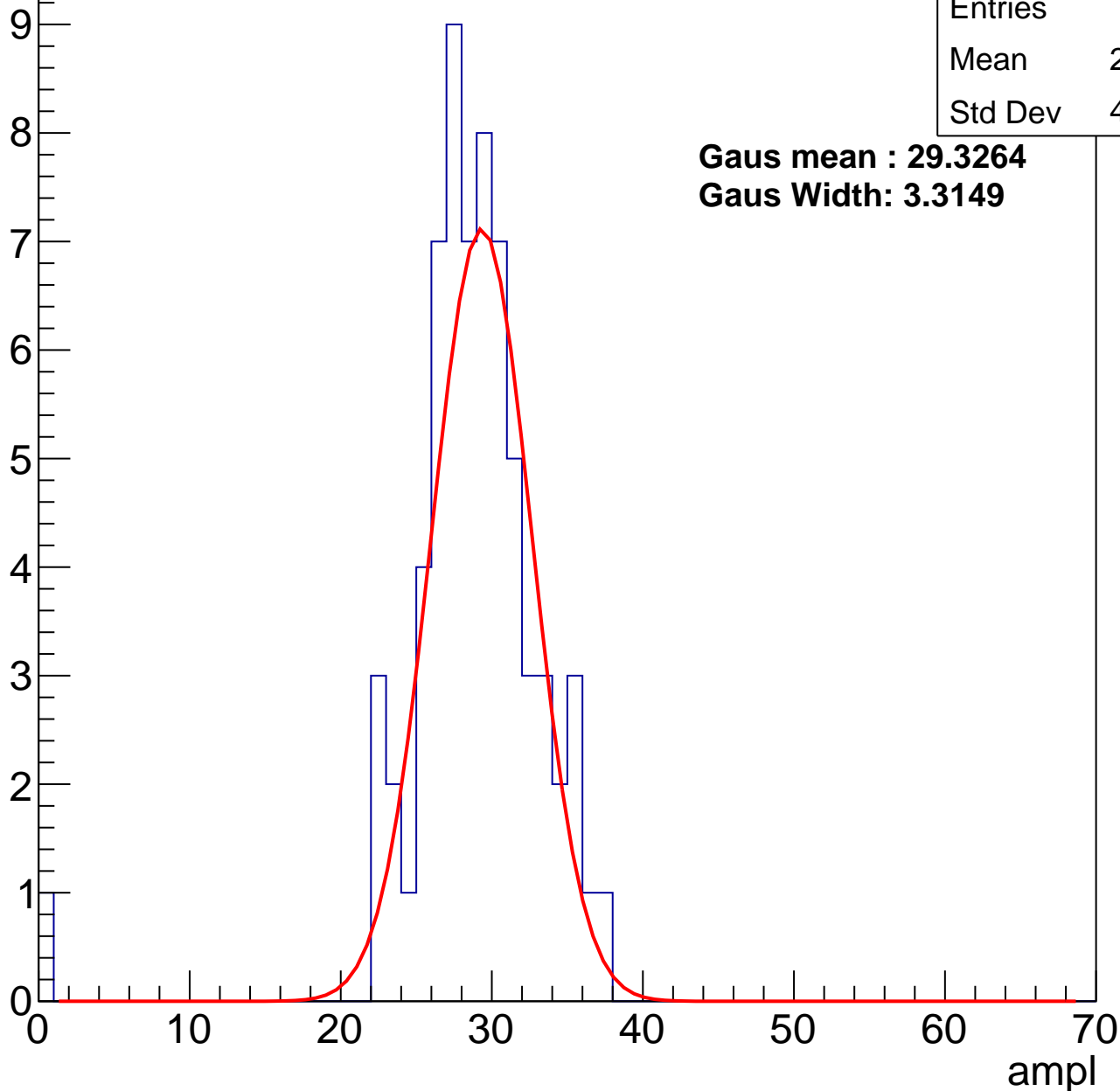
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 67    |
| Mean    | 28.28 |
| Std Dev | 4.877 |

**Gaus mean : 29.3264**

**Gaus Width: 3.3149**



# B0L001S, U2-ch8, adc1

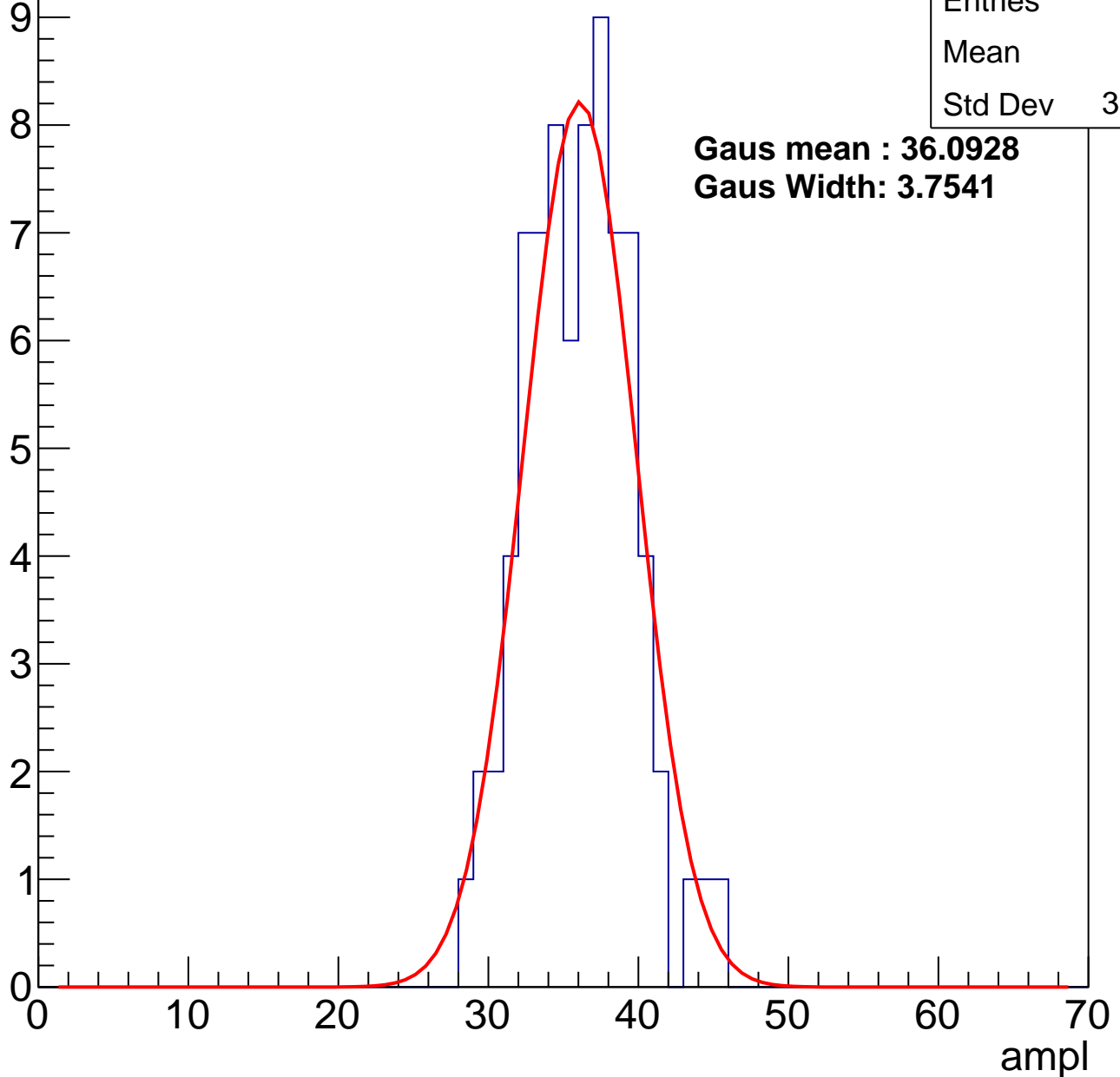
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 77    |
| Mean    | 35.6  |
| Std Dev | 3.499 |

**Gaus mean : 36.0928**

**Gaus Width: 3.7541**



# B0L001S, U2-ch8, adc2

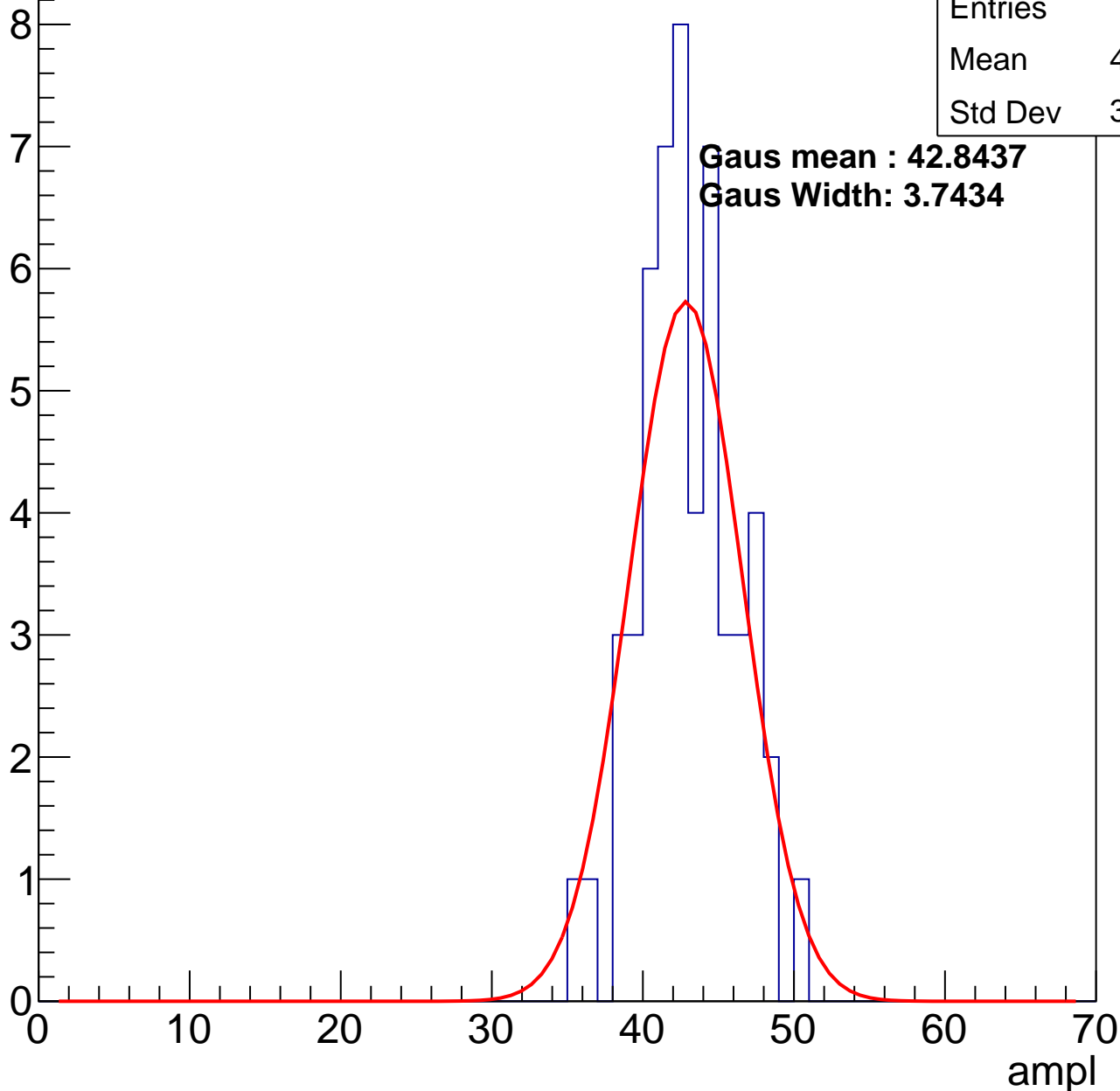
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 53    |
| Mean    | 42.49 |
| Std Dev | 3.136 |

**Gaus mean : 42.8437**

**Gaus Width: 3.7434**



# B0L001S, U2-ch8, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

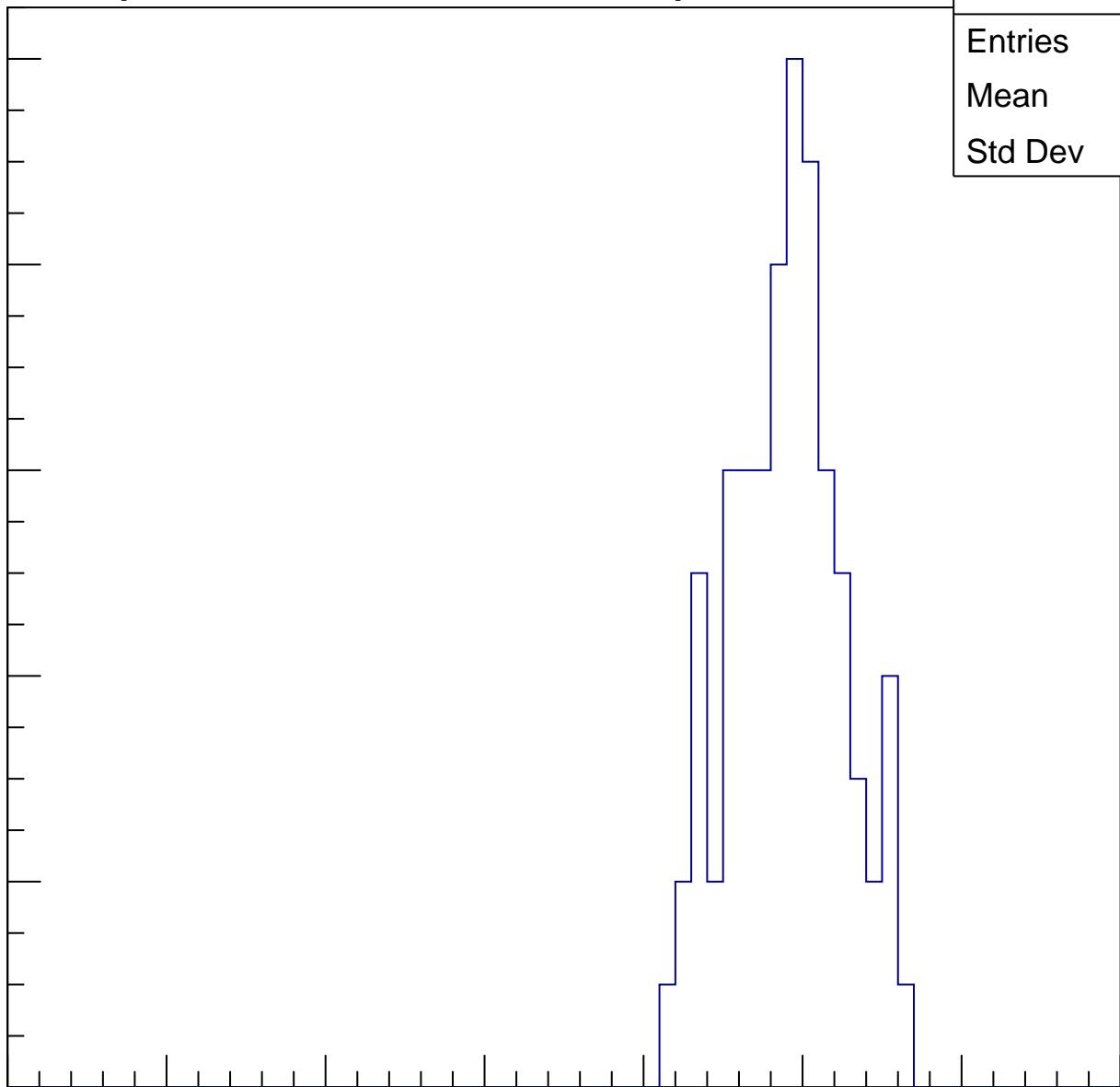
|         |       |
|---------|-------|
| Entries | 76    |
| Mean    | 48.54 |
| Std Dev | 3.492 |

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

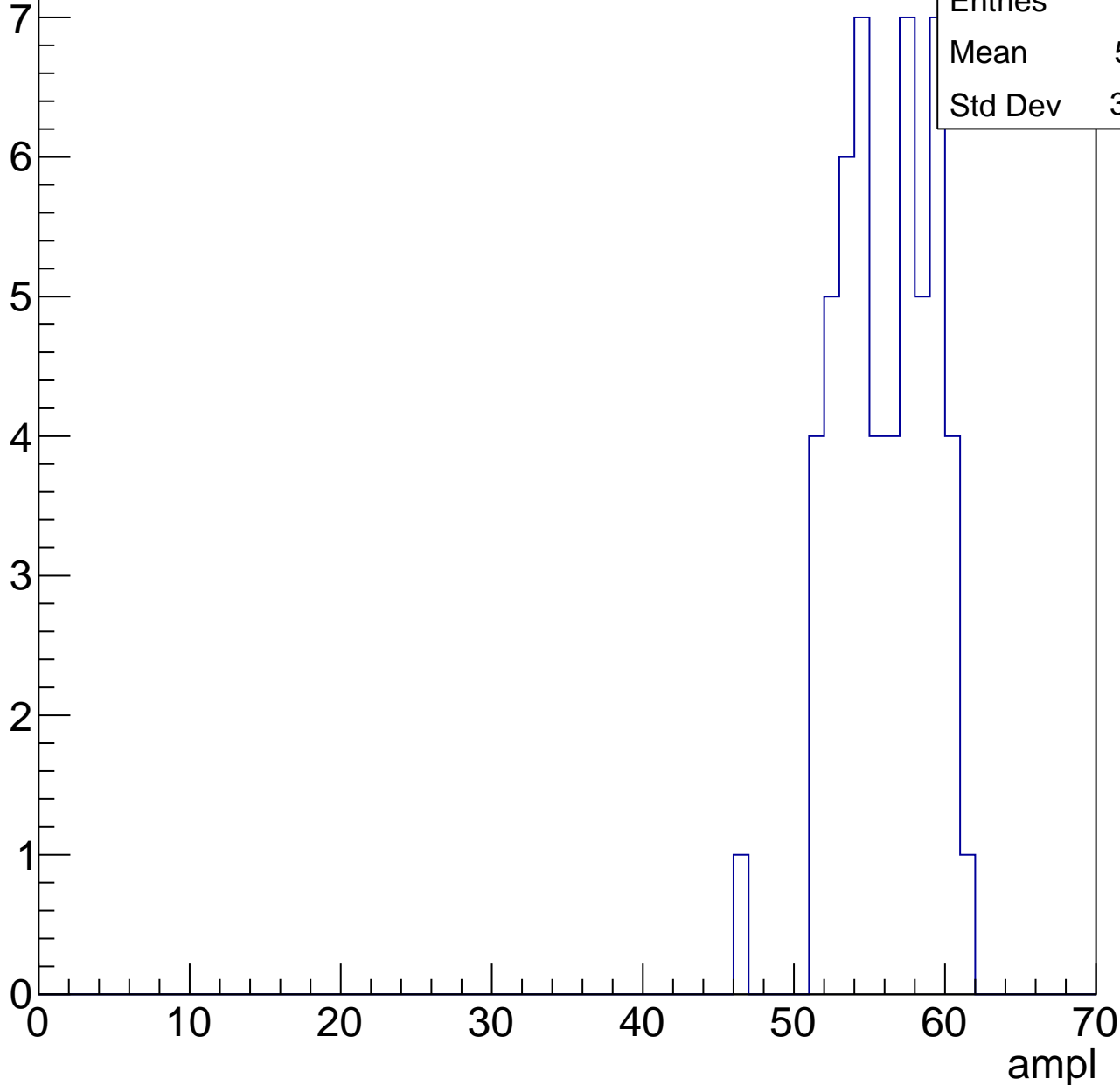
ampl



# B0L001S, U2-ch8, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |       |
|---------|-------|
| Entries | 55    |
| Mean    | 55.51 |
| Std Dev | 3.109 |

# B0L001S, U2-ch8, adc5

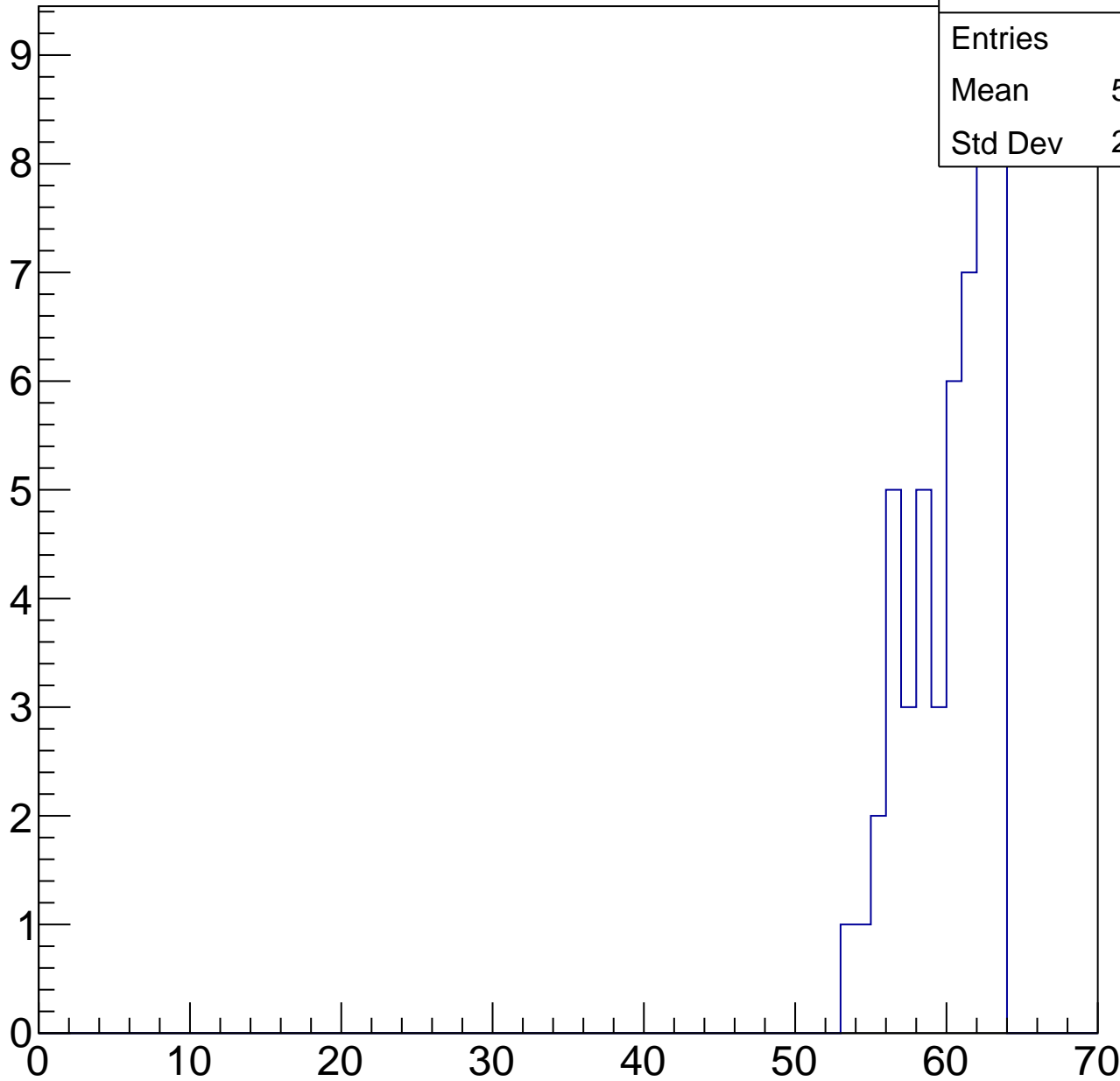
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

|         |       |
|---------|-------|
| Entries | 50    |
| Mean    | 59.68 |
| Std Dev | 2.738 |

ampl



# B0L001S, U2-ch8, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

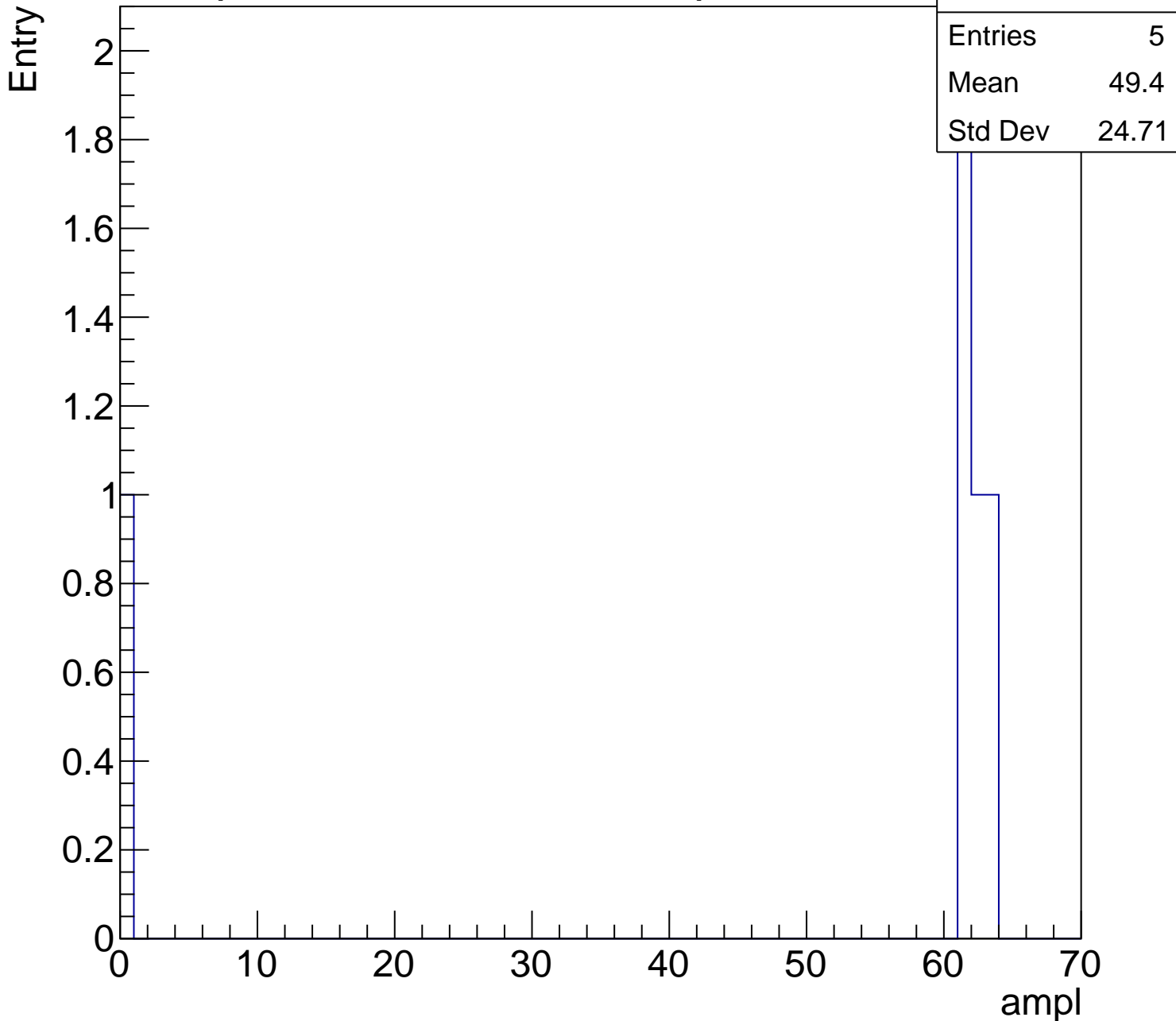
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

|         |       |
|---------|-------|
| Entries | 5     |
| Mean    | 49.4  |
| Std Dev | 24.71 |

0 10 20 30 40 50 60 70

ampl





# B0L001S, U2-ch8, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U2-ch9, adc0

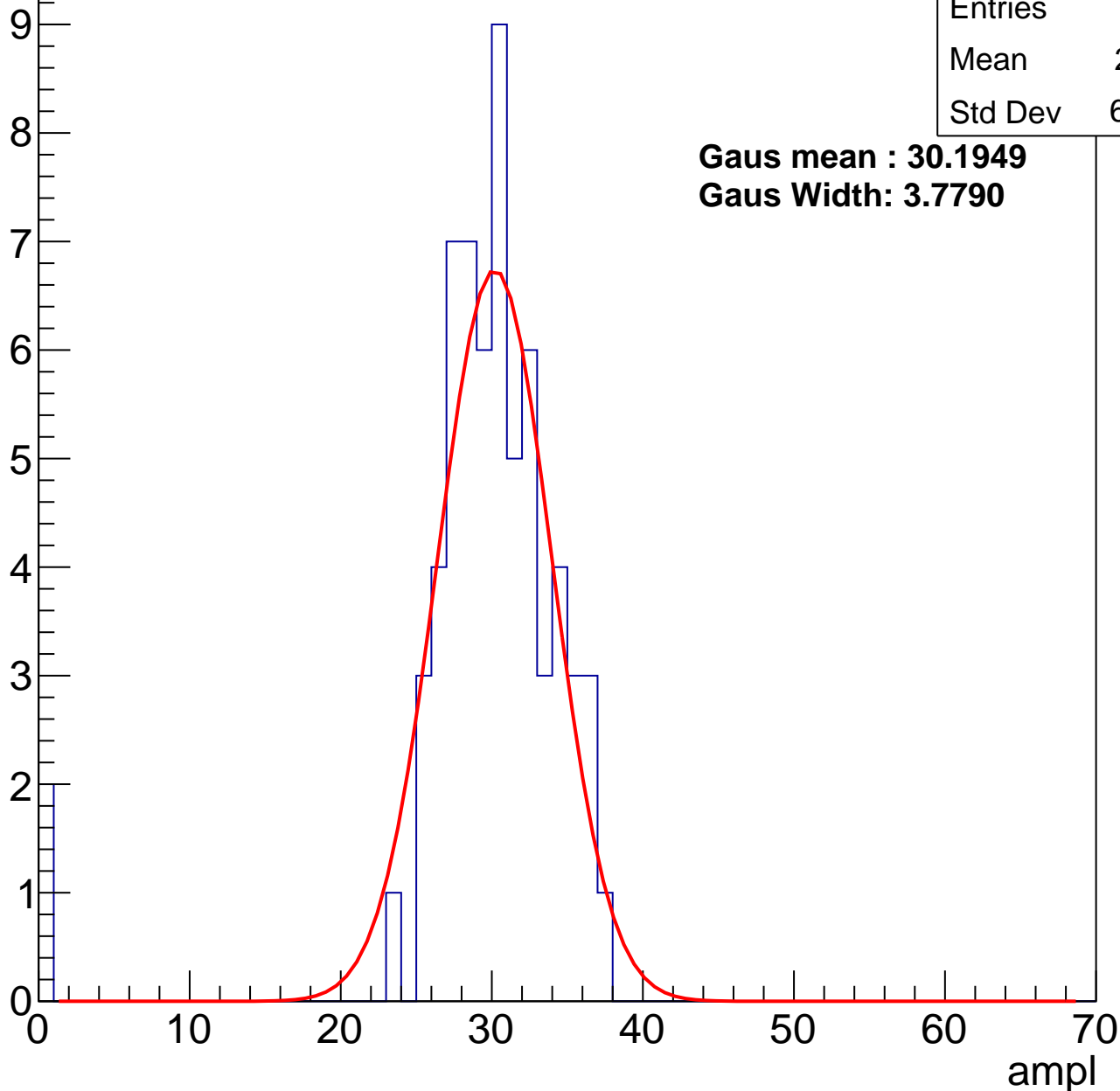
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 64    |
| Mean    | 29.11 |
| Std Dev | 6.106 |

**Gaus mean : 30.1949**

**Gaus Width: 3.7790**



# B0L001S, U2-ch9, adc1

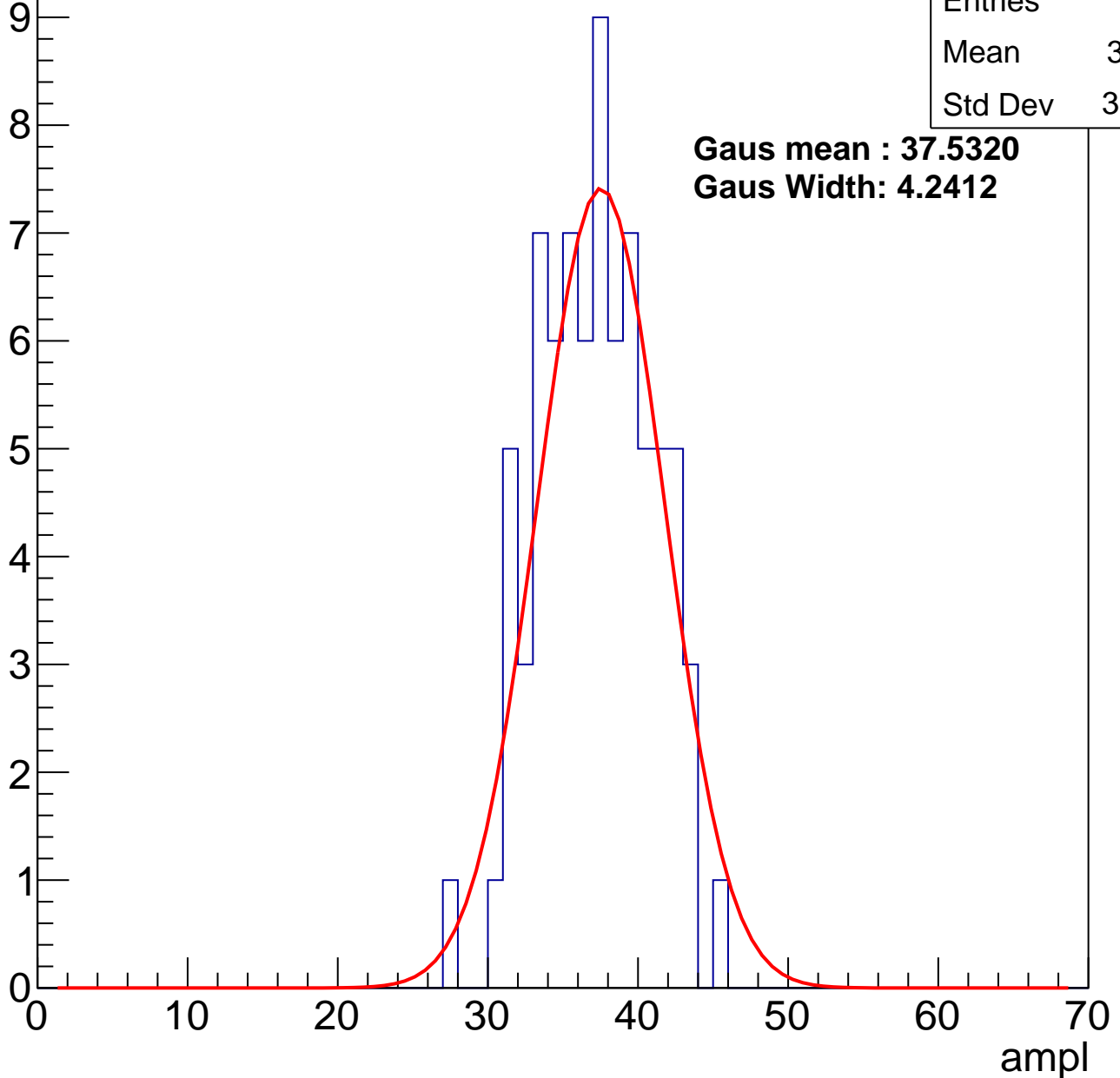
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 77    |
| Mean    | 36.71 |
| Std Dev | 3.699 |

**Gaus mean : 37.5320**

**Gaus Width: 4.2412**



# B0L001S, U2-ch9, adc2

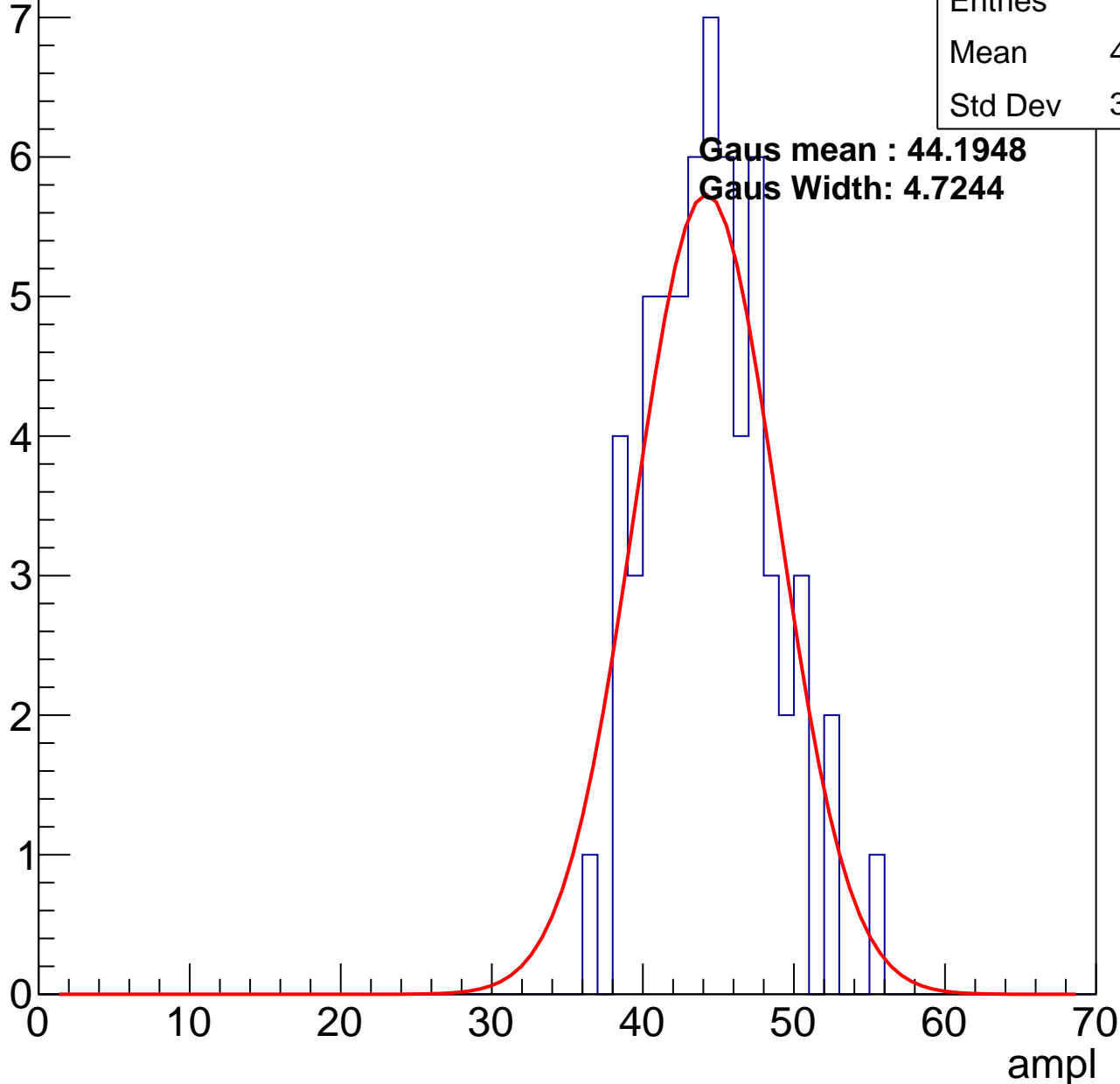
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 63    |
| Mean    | 44.02 |
| Std Dev | 3.914 |

**Gaus mean : 44.1948**

**Gaus Width: 4.7244**

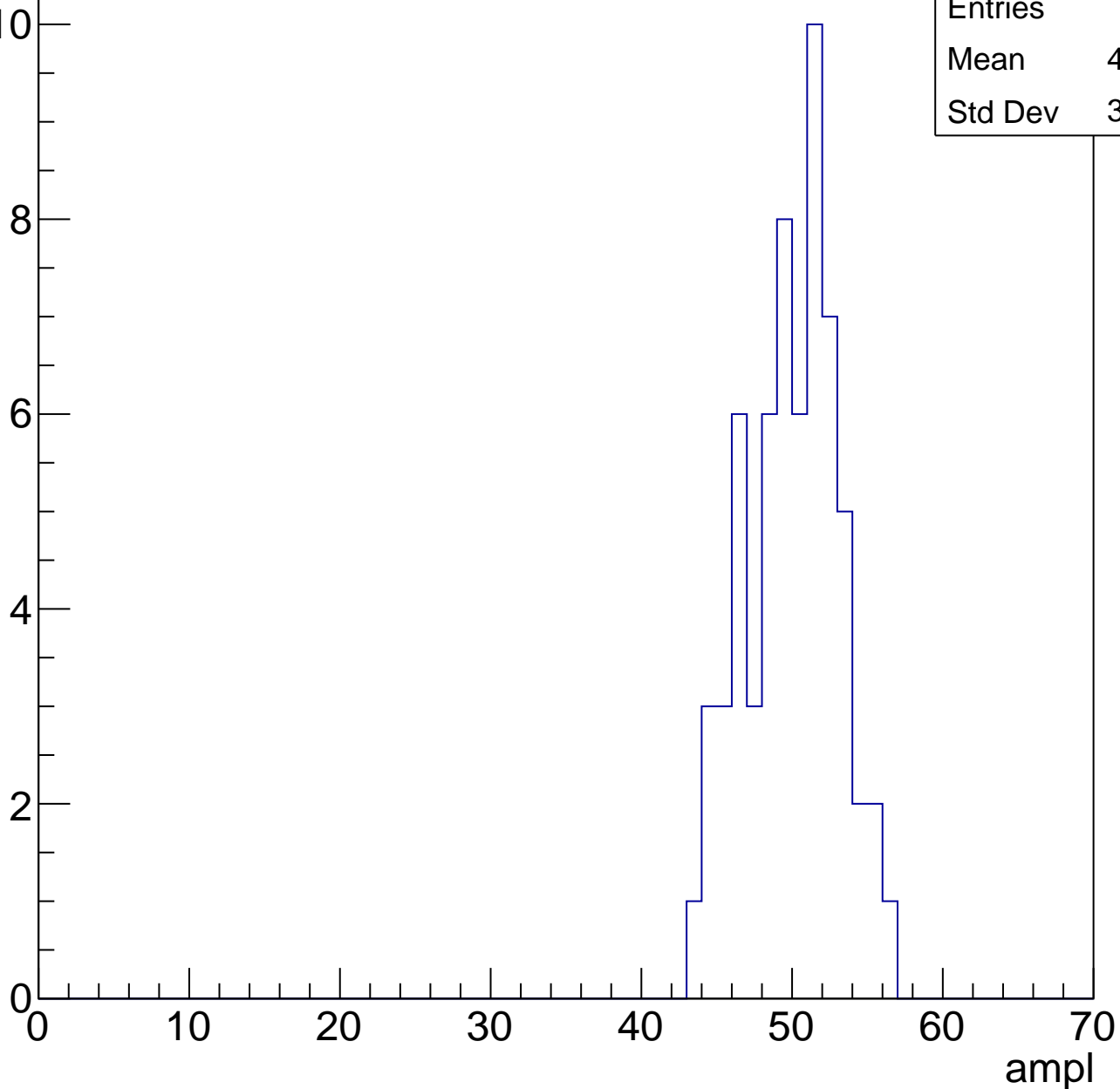


# B0L001S, U2-ch9, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 63    |
| Mean    | 49.52 |
| Std Dev | 3.018 |

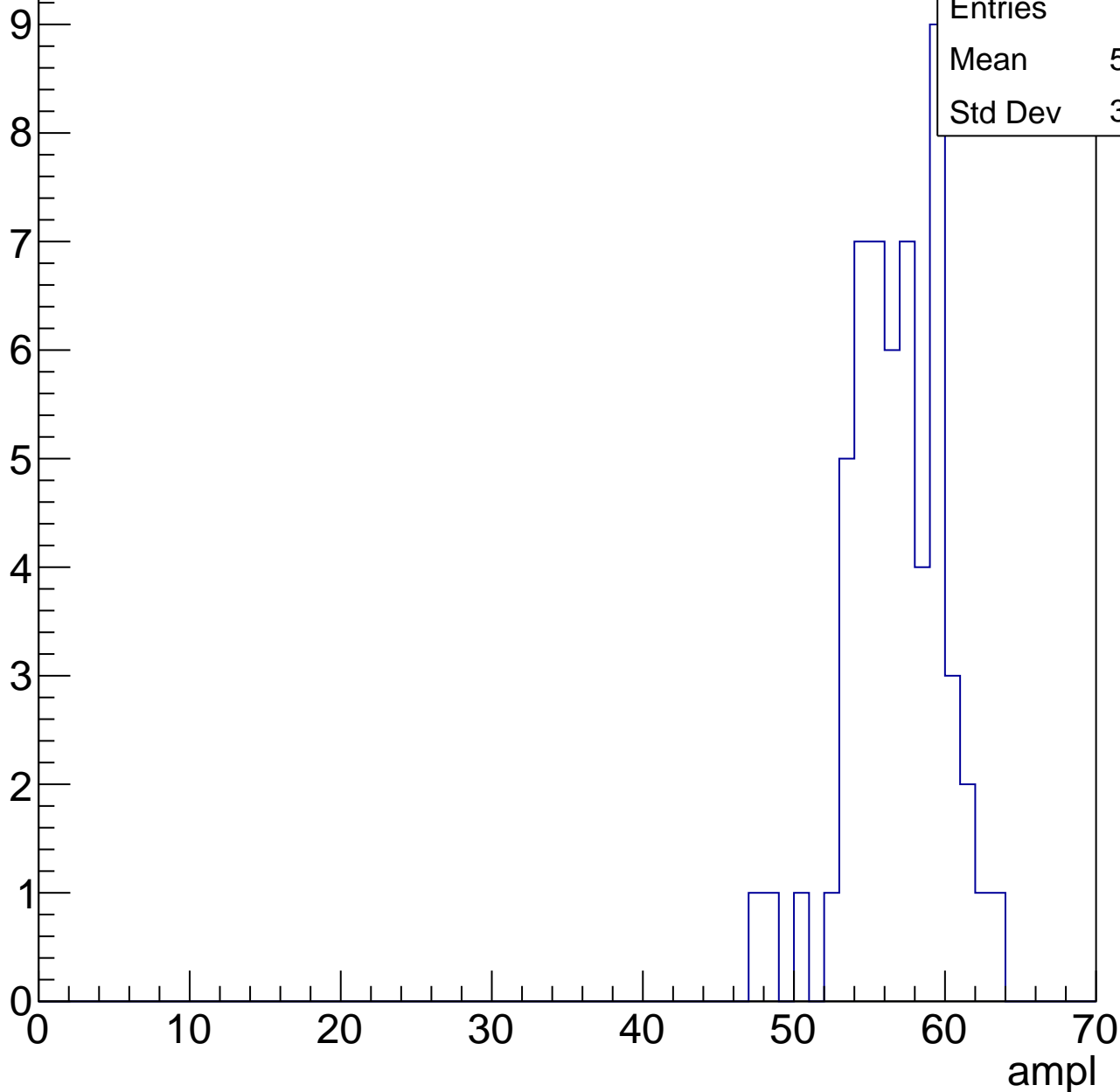


# B0L001S, U2-ch9, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 56    |
| Mean    | 56.25 |
| Std Dev | 3.164 |

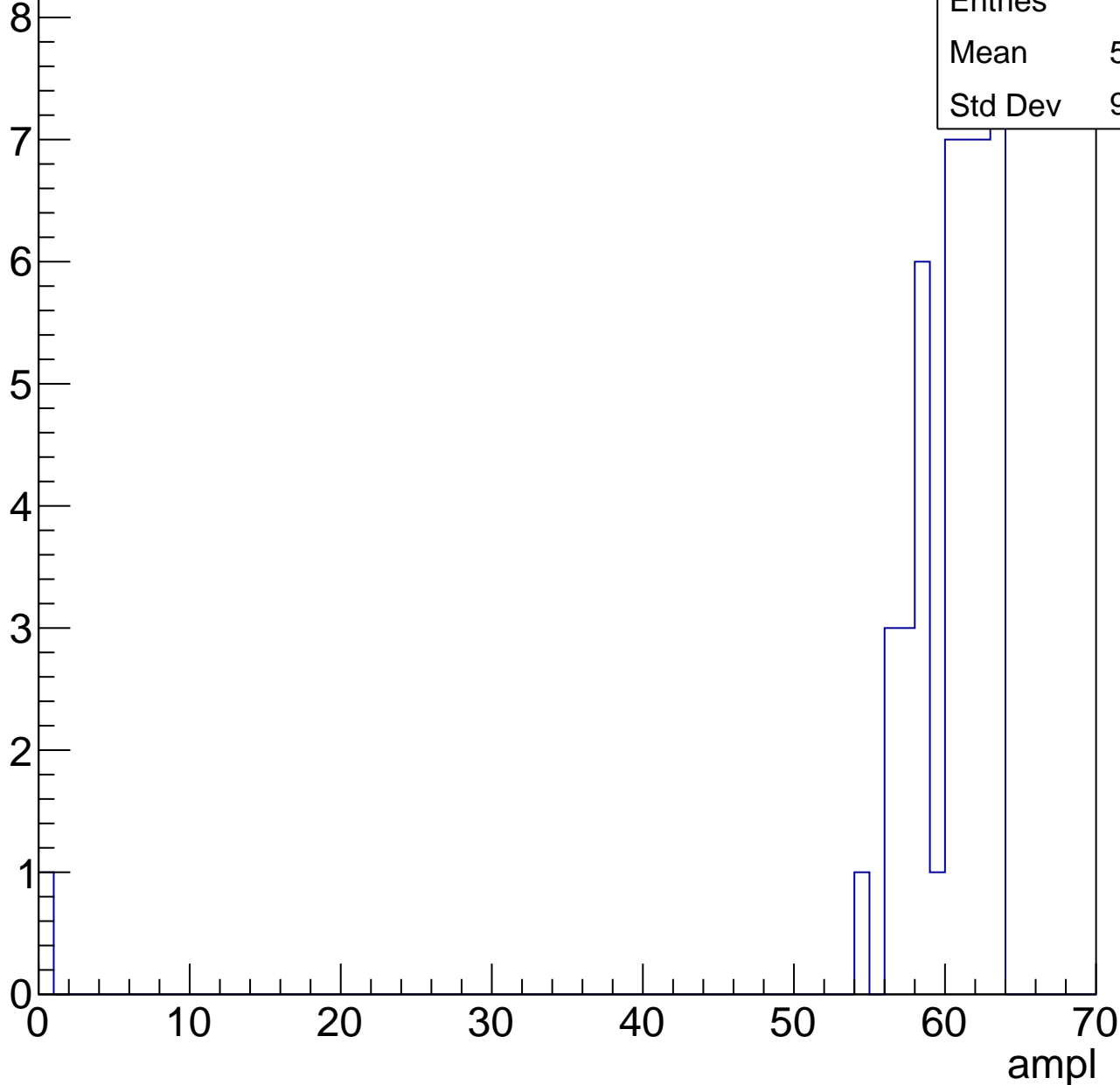


# B0L001S, U2-ch9, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 44    |
| Mean    | 58.75 |
| Std Dev | 9.262 |



# B0L001S, U2-ch9, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

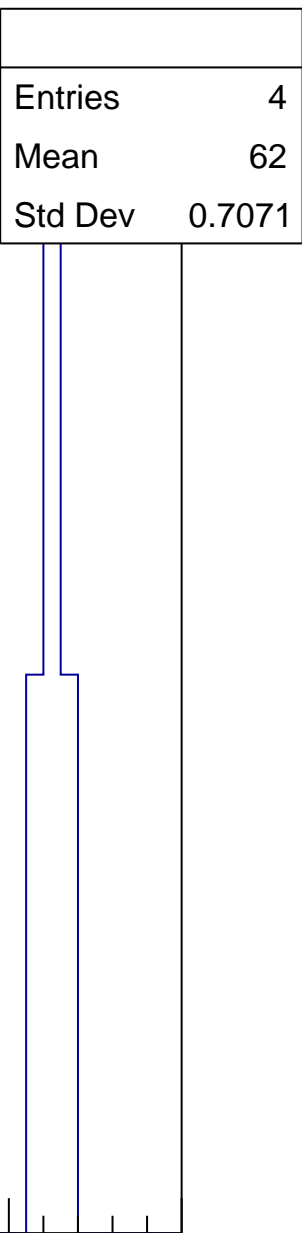
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

|         |        |
|---------|--------|
| Entries | 4      |
| Mean    | 62     |
| Std Dev | 0.7071 |

0 10 20 30 40 50 60 70

ampl





# B0L001S, U2-ch9, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 0 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch10, adc0

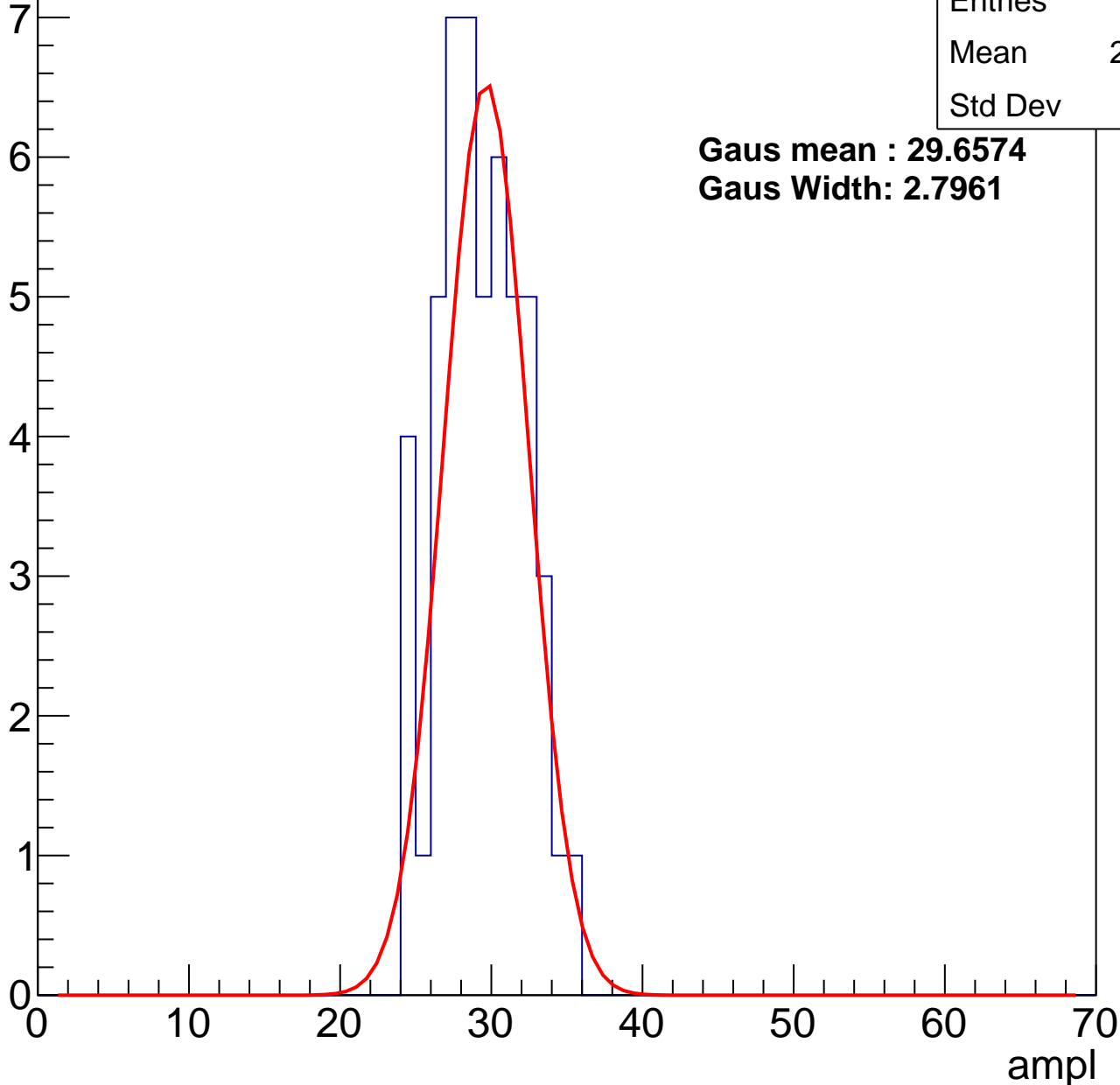
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 50    |
| Mean    | 28.88 |
| Std Dev | 2.74  |

**Gaus mean : 29.6574**

**Gaus Width: 2.7961**



# B0L001S, U2-ch10, adc1

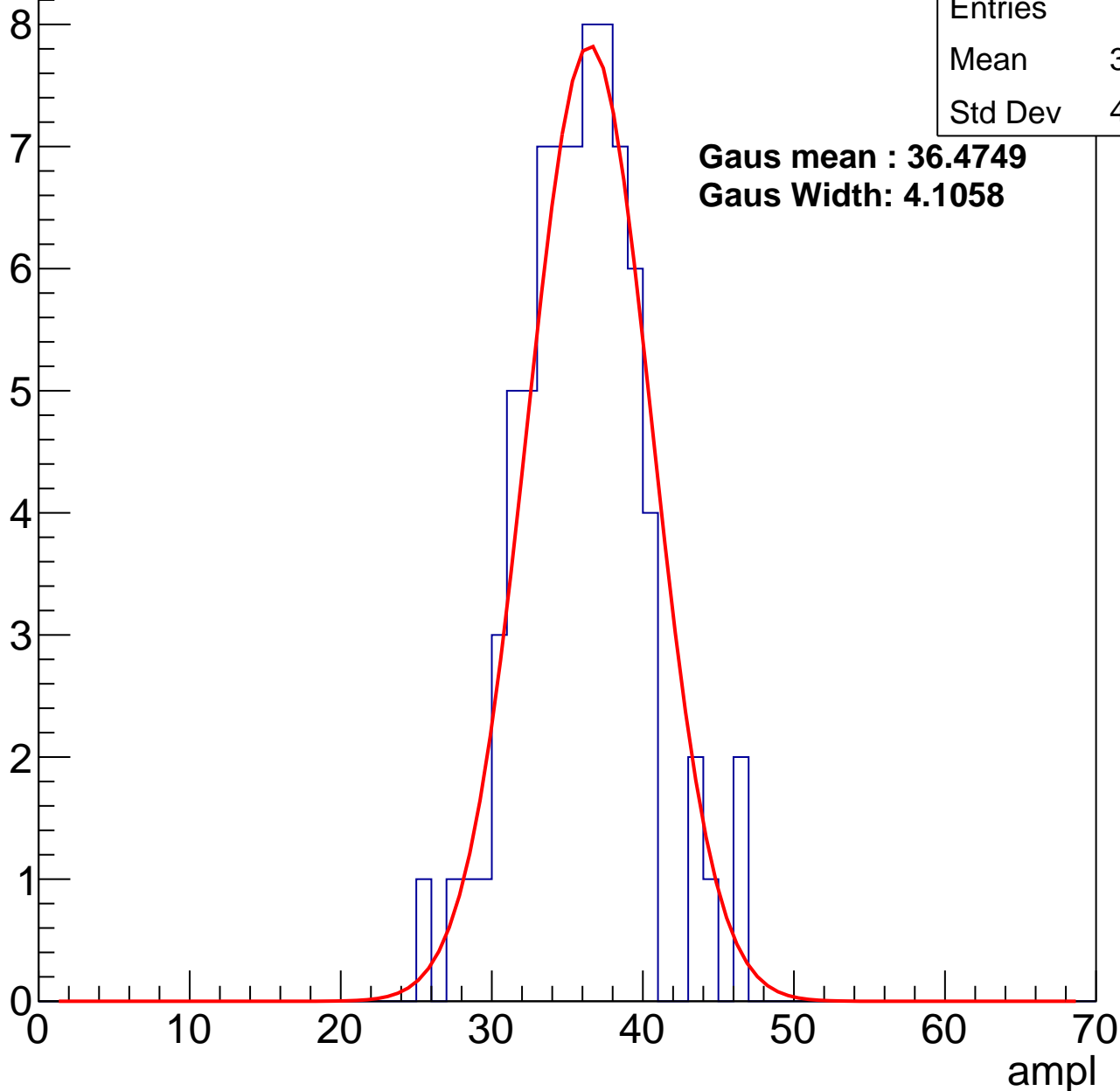
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 76    |
| Mean    | 35.45 |
| Std Dev | 4.005 |

**Gaus mean : 36.4749**

**Gaus Width: 4.1058**



# B0L001S, U2-ch10, adc2

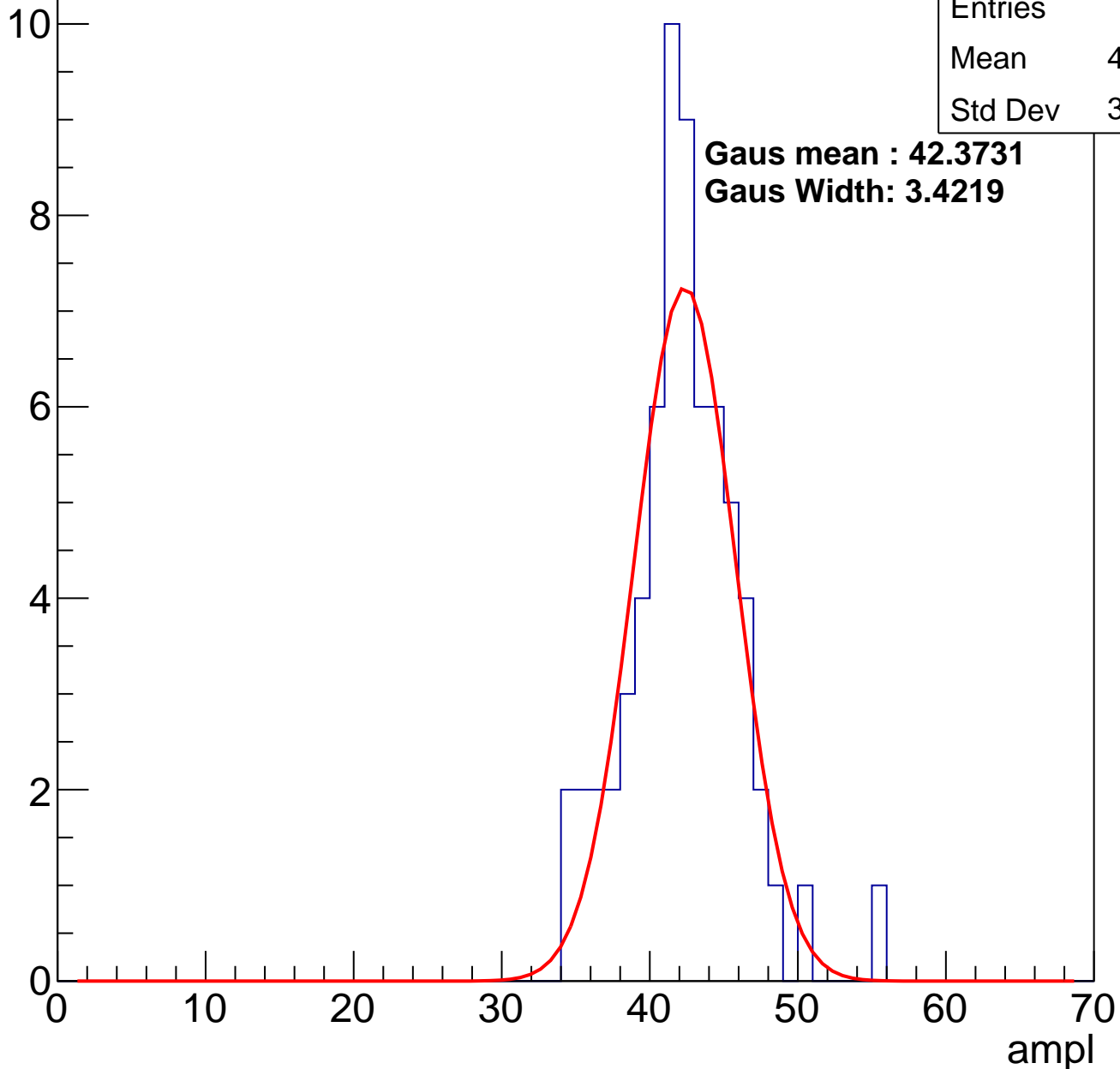
calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 66    |
| Mean    | 41.82 |
| Std Dev | 3.737 |

**Gaus mean : 42.3731**

**Gaus Width: 3.4219**

Entry

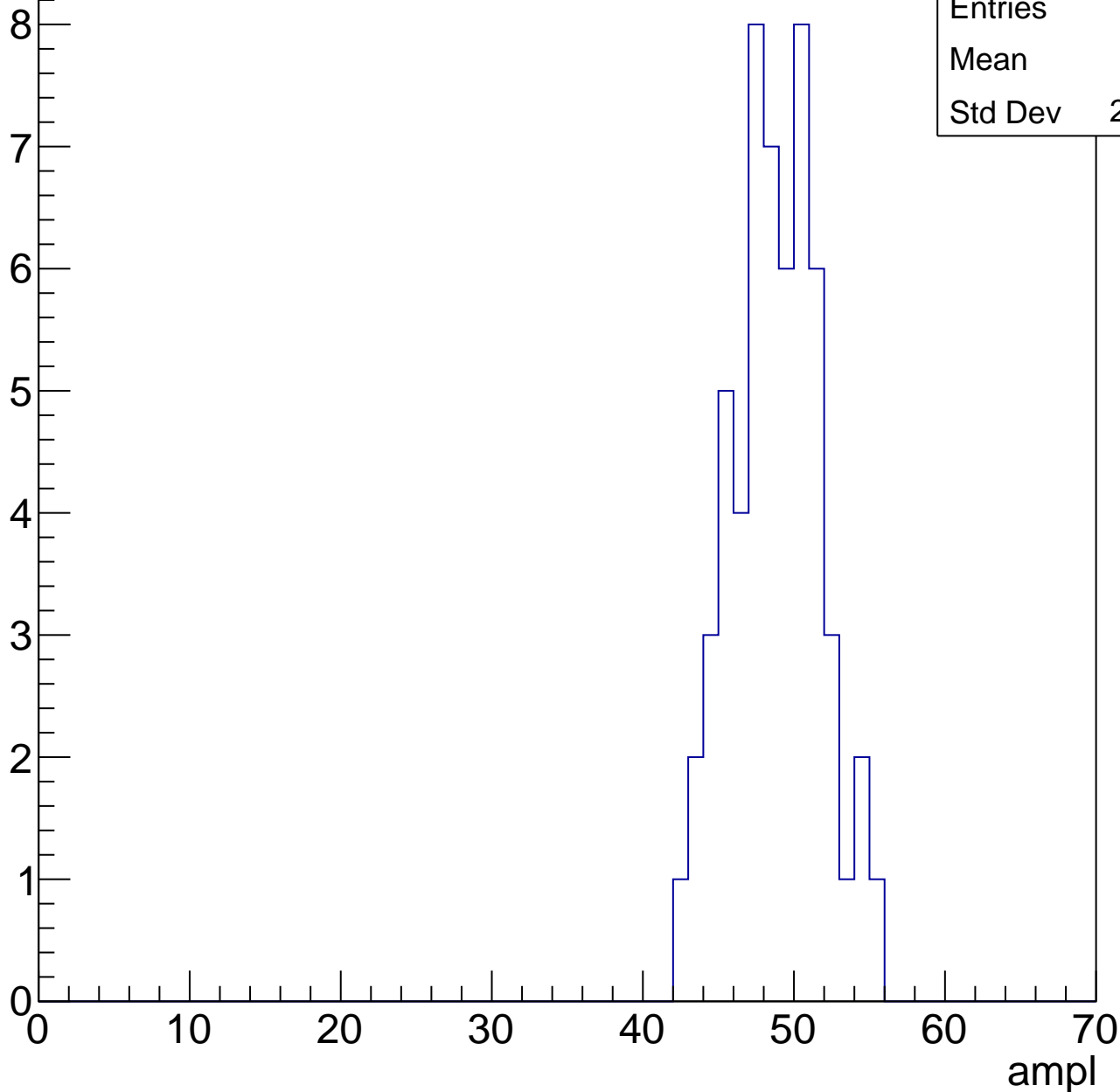


# B0L001S, U2-ch10, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 57    |
| Mean    | 48.3  |
| Std Dev | 2.914 |

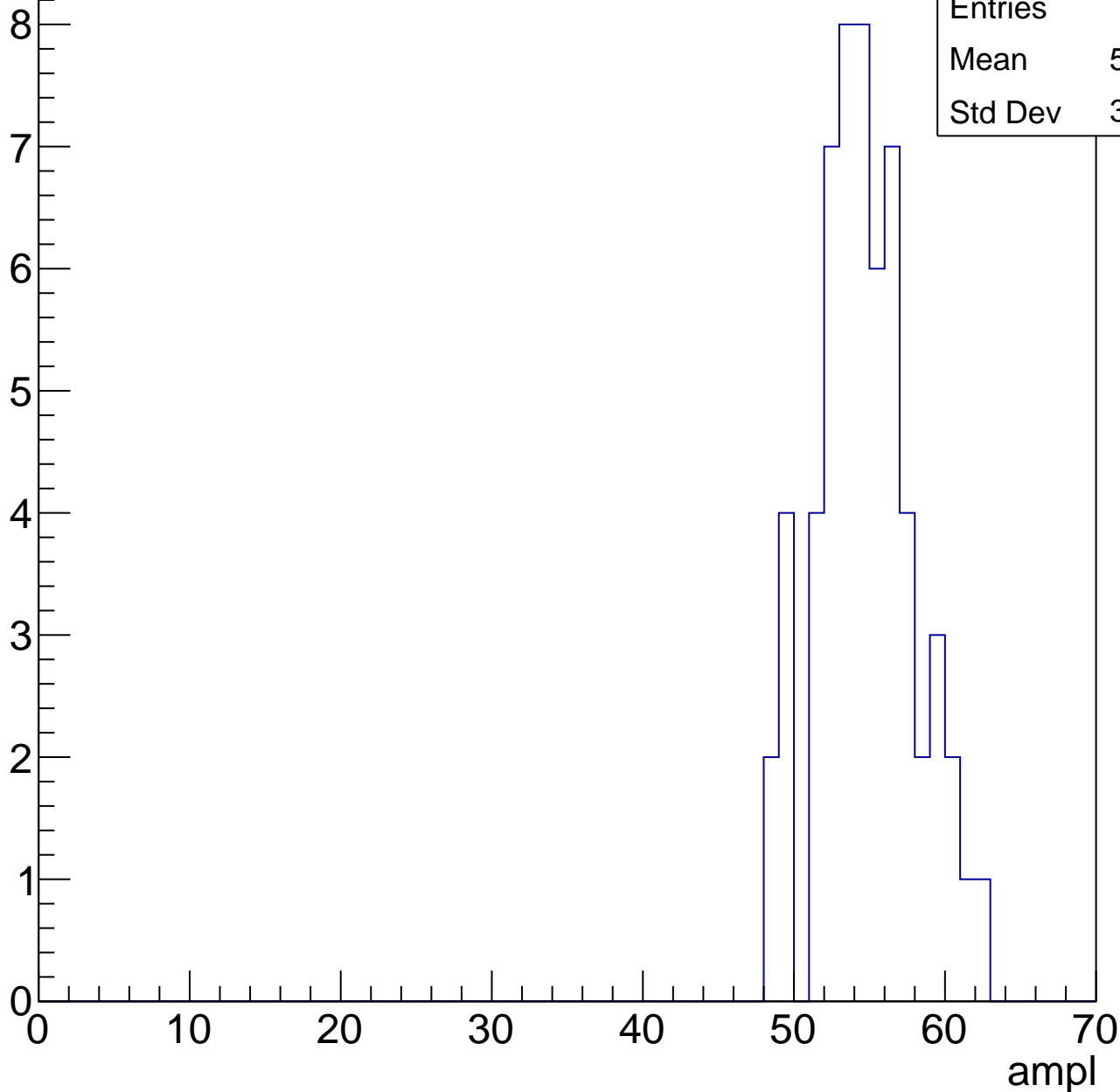


# B0L001S, U2-ch10, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

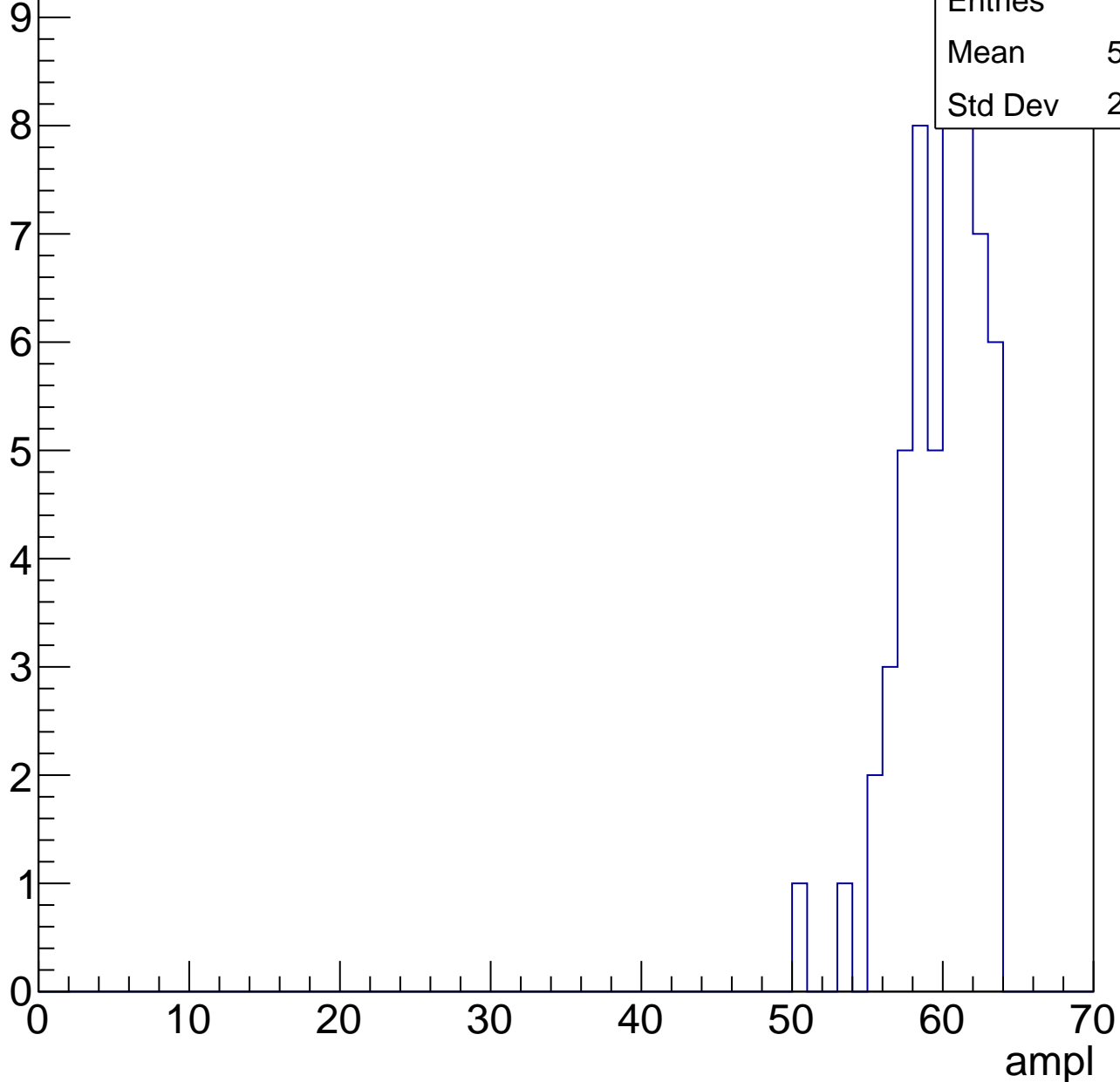
|         |       |
|---------|-------|
| Entries | 59    |
| Mean    | 54.27 |
| Std Dev | 3.193 |



# B0L001S, U2-ch10, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

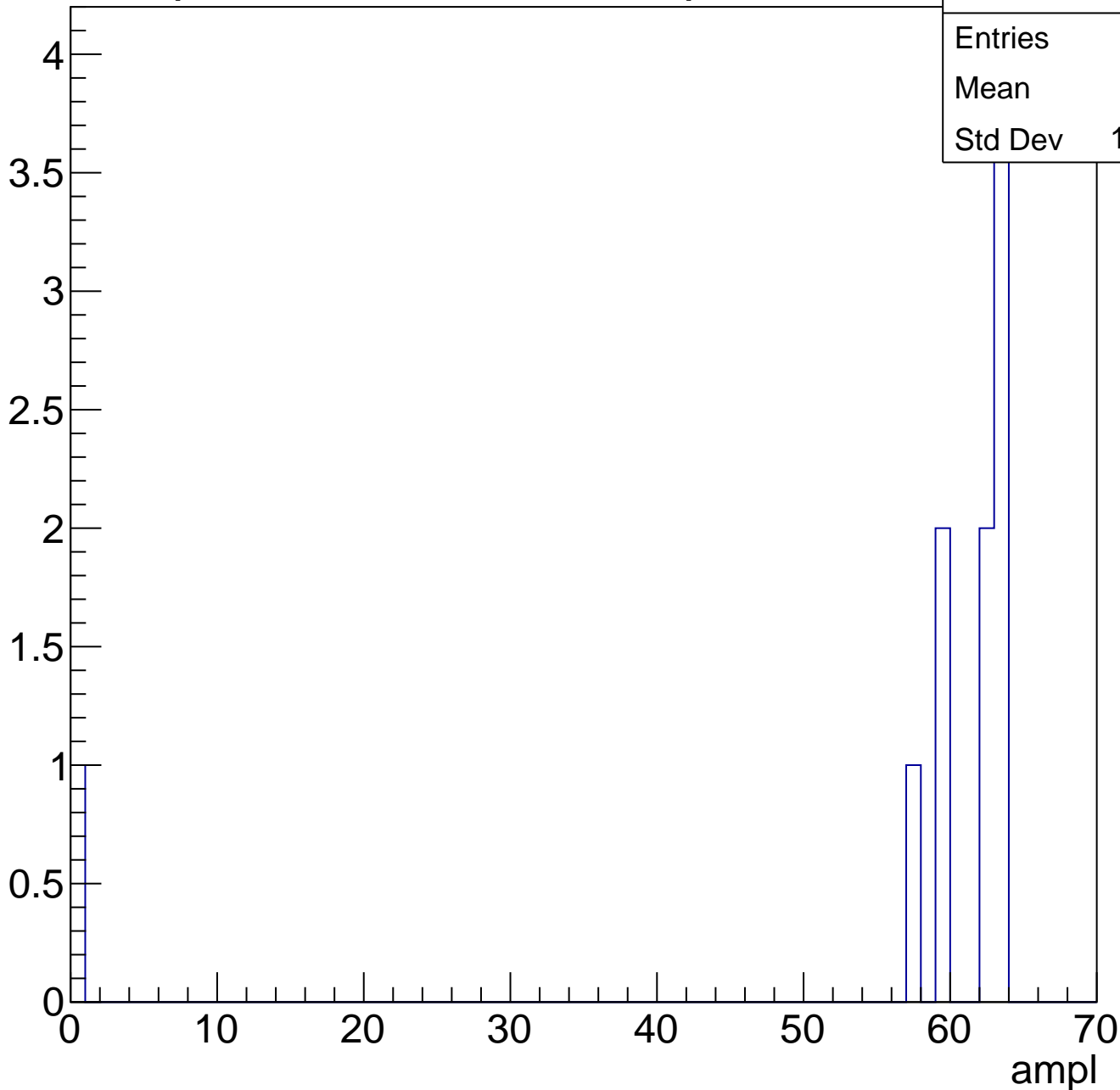
Entry



# B0L001S, U2-ch10, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch10, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 0 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch11, adc0

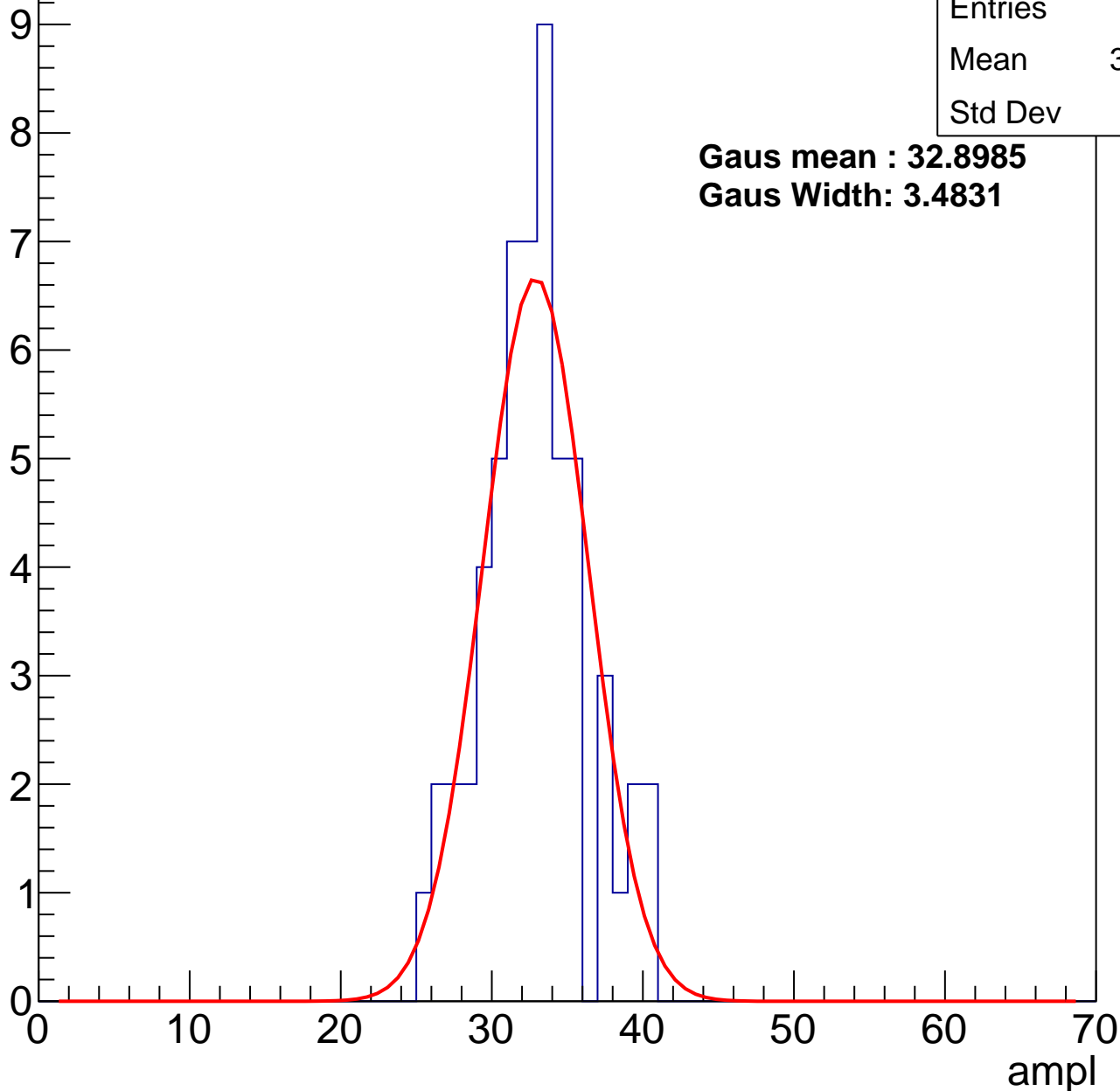
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 57    |
| Mean    | 32.33 |
| Std Dev | 3.43  |

**Gaus mean : 32.8985**

**Gaus Width: 3.4831**



# B0L001S, U2-ch11, adc1

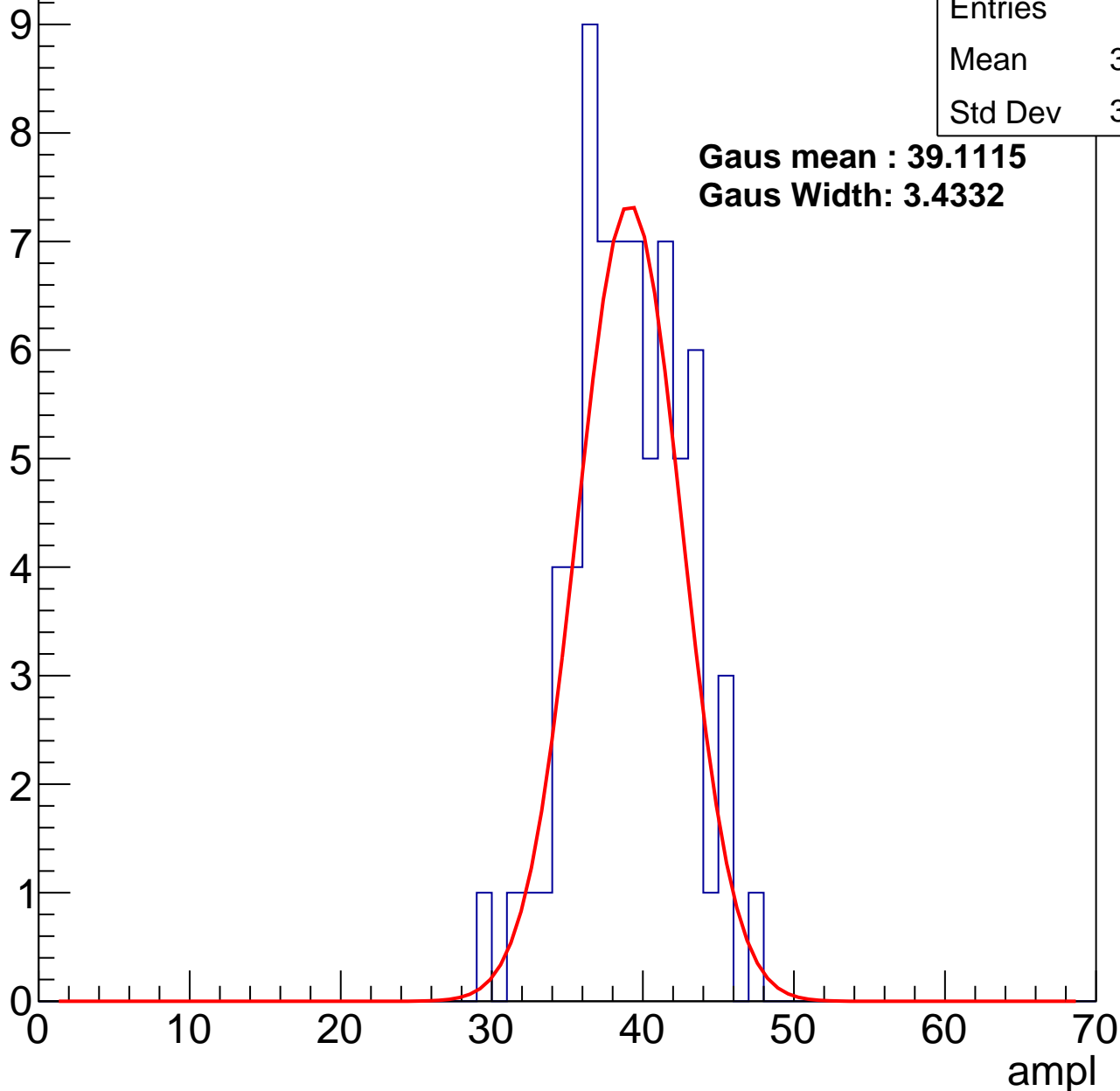
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 70    |
| Mean    | 38.63 |
| Std Dev | 3.566 |

**Gaus mean : 39.1115**

**Gaus Width: 3.4332**



# B0L001S, U2-ch11, adc2

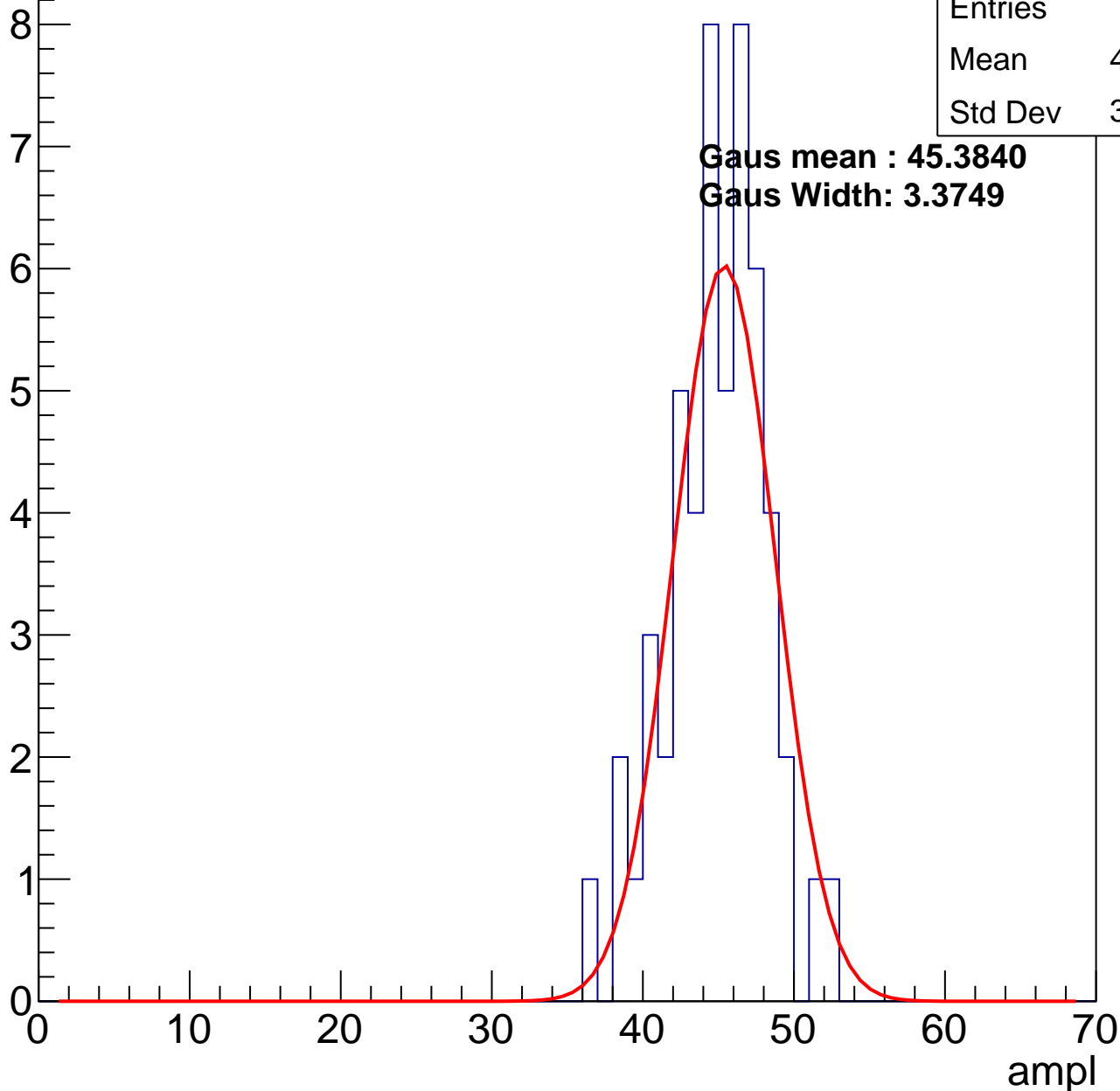
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 53    |
| Mean    | 44.43 |
| Std Dev | 3.248 |

**Gaus mean : 45.3840**

**Gaus Width: 3.3749**

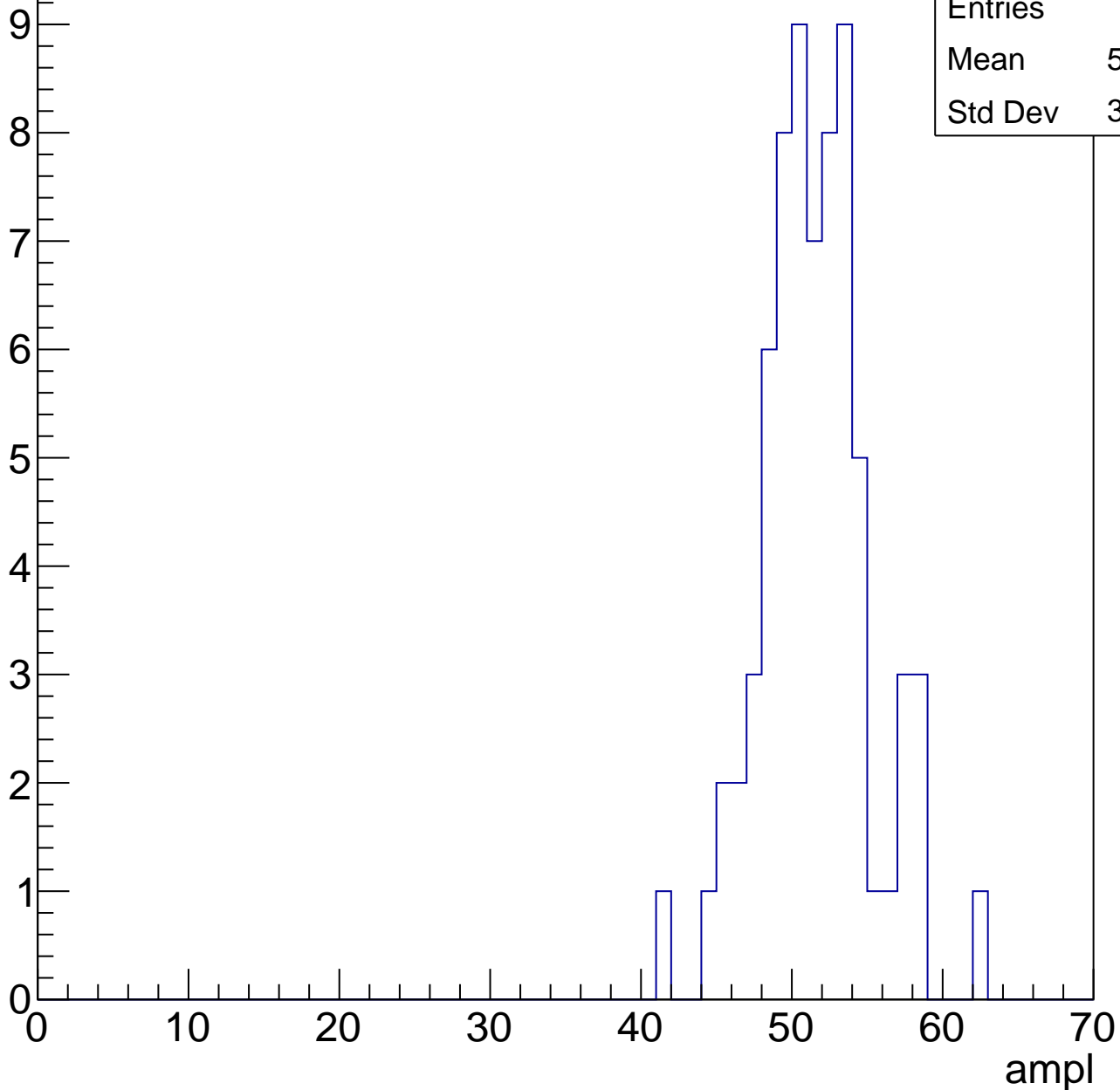


# B0L001S, U2-ch11, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 70    |
| Mean    | 51.09 |
| Std Dev | 3.624 |



# B0L001S, U2-ch11, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

70

ampl

|         |       |
|---------|-------|
| Entries | 67    |
| Mean    | 57.58 |
| Std Dev | 3.062 |

10

8

6

4

2

0

0

10

20

30

40

50

60

70

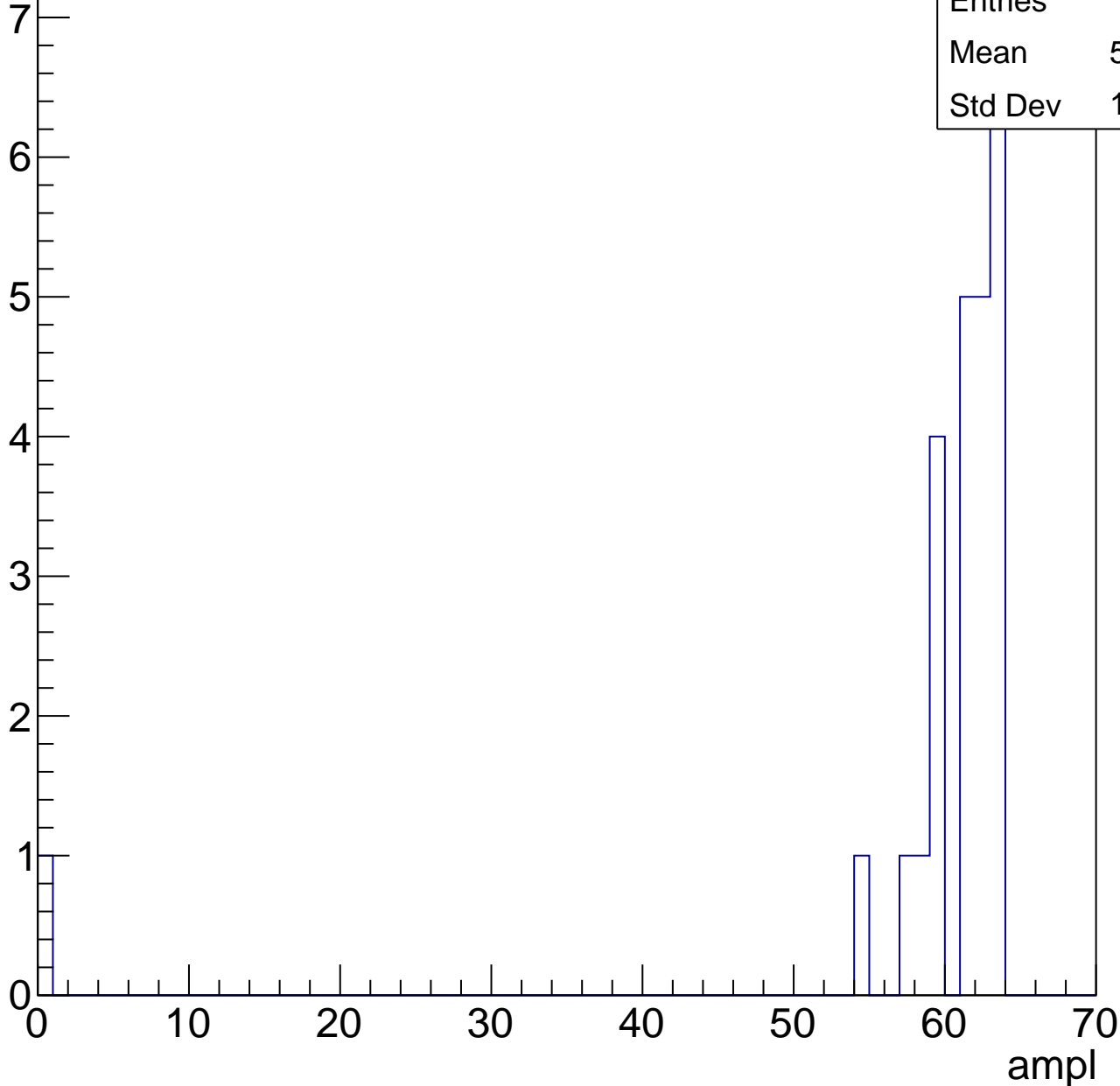
ampl

# B0L001S, U2-ch11, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 25    |
| Mean    | 58.44 |
| Std Dev | 12.13 |



# B0L001S, U2-ch11, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 0 |
| Mean    | 0 |
| Std Dev | 0 |



# B0L001S, U2-ch11, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U2-ch12, adc0

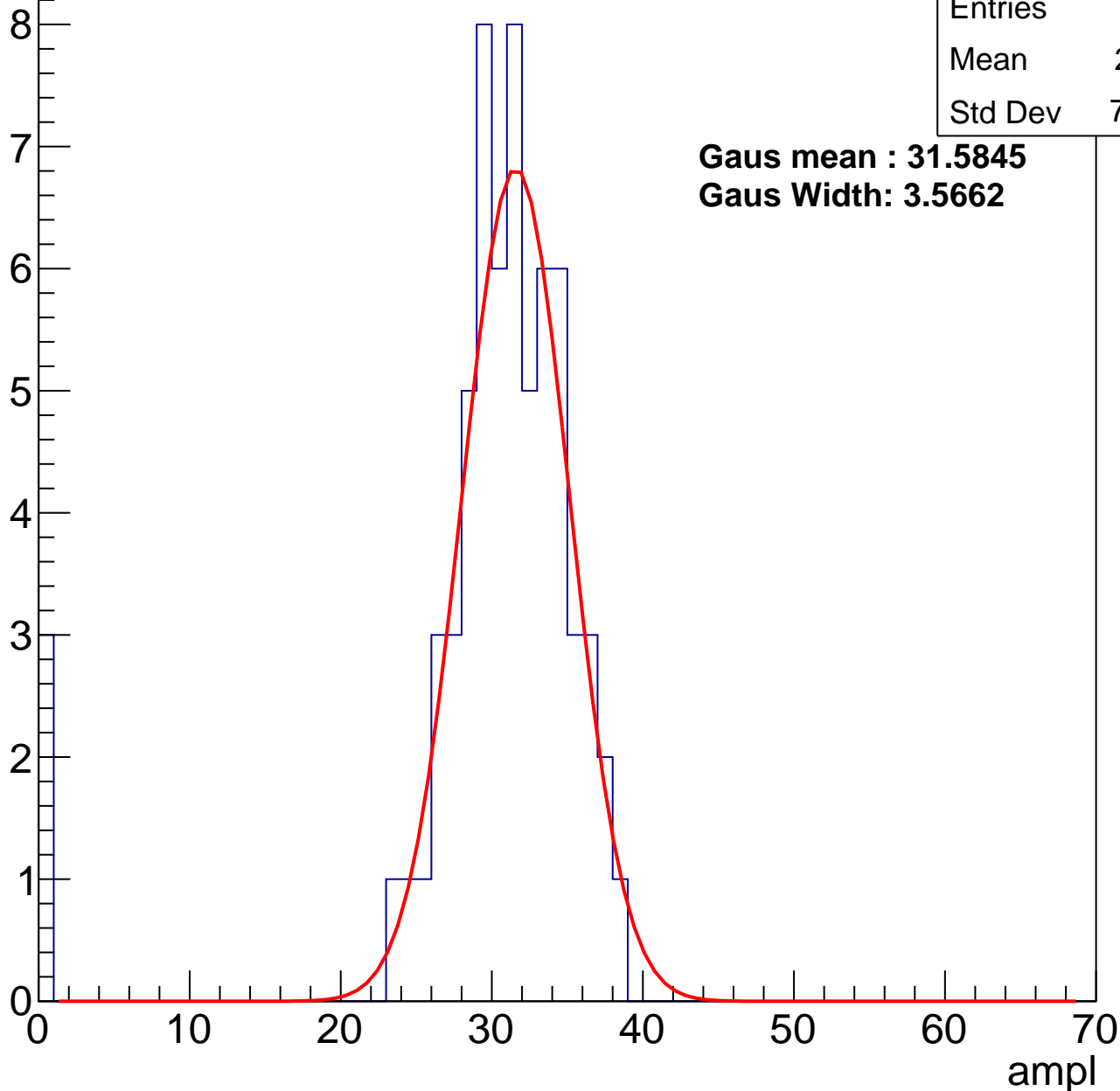
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 65    |
| Mean    | 29.51 |
| Std Dev | 7.254 |

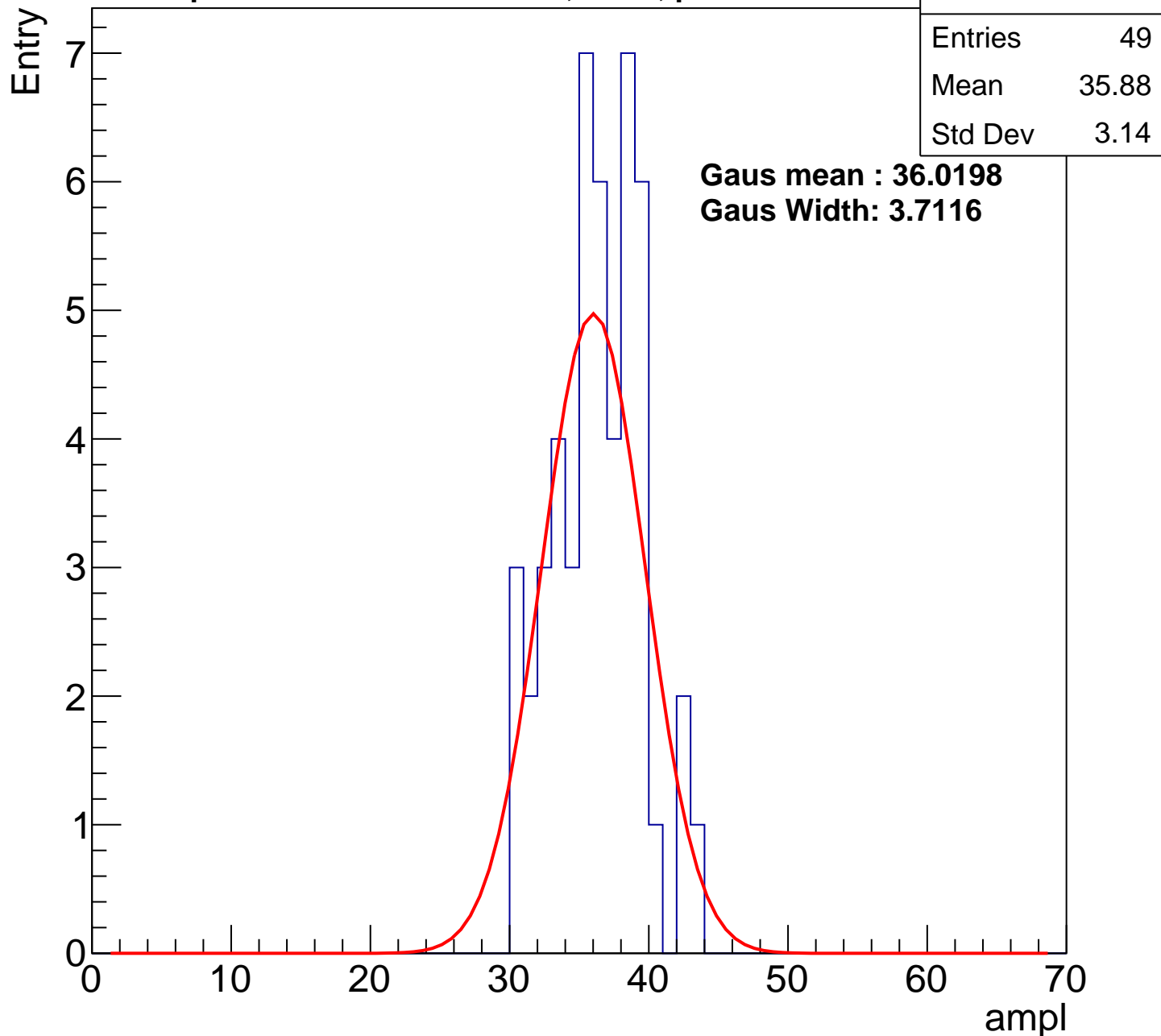
**Gaus mean : 31.5845**

**Gaus Width: 3.5662**



# B0L001S, U2-ch12, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U2-ch12, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 79    |
| Mean    | 42.82 |
| Std Dev | 3.61  |

**Gaus mean : 43.2079**

**Gaus Width: 3.4152**

Entry

10

8

6

4

2

0

0

10

20

30

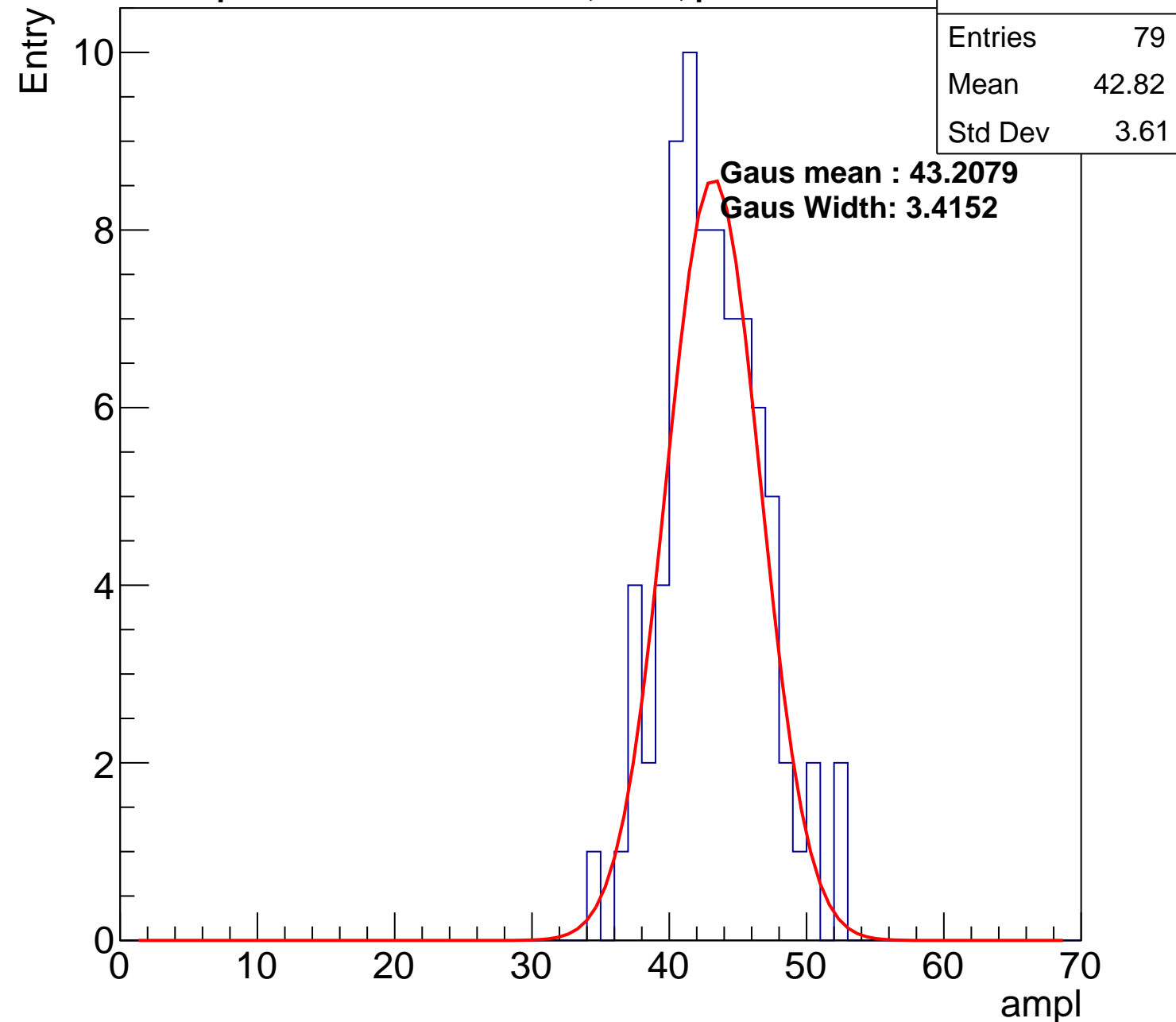
40

50

60

70

ampl

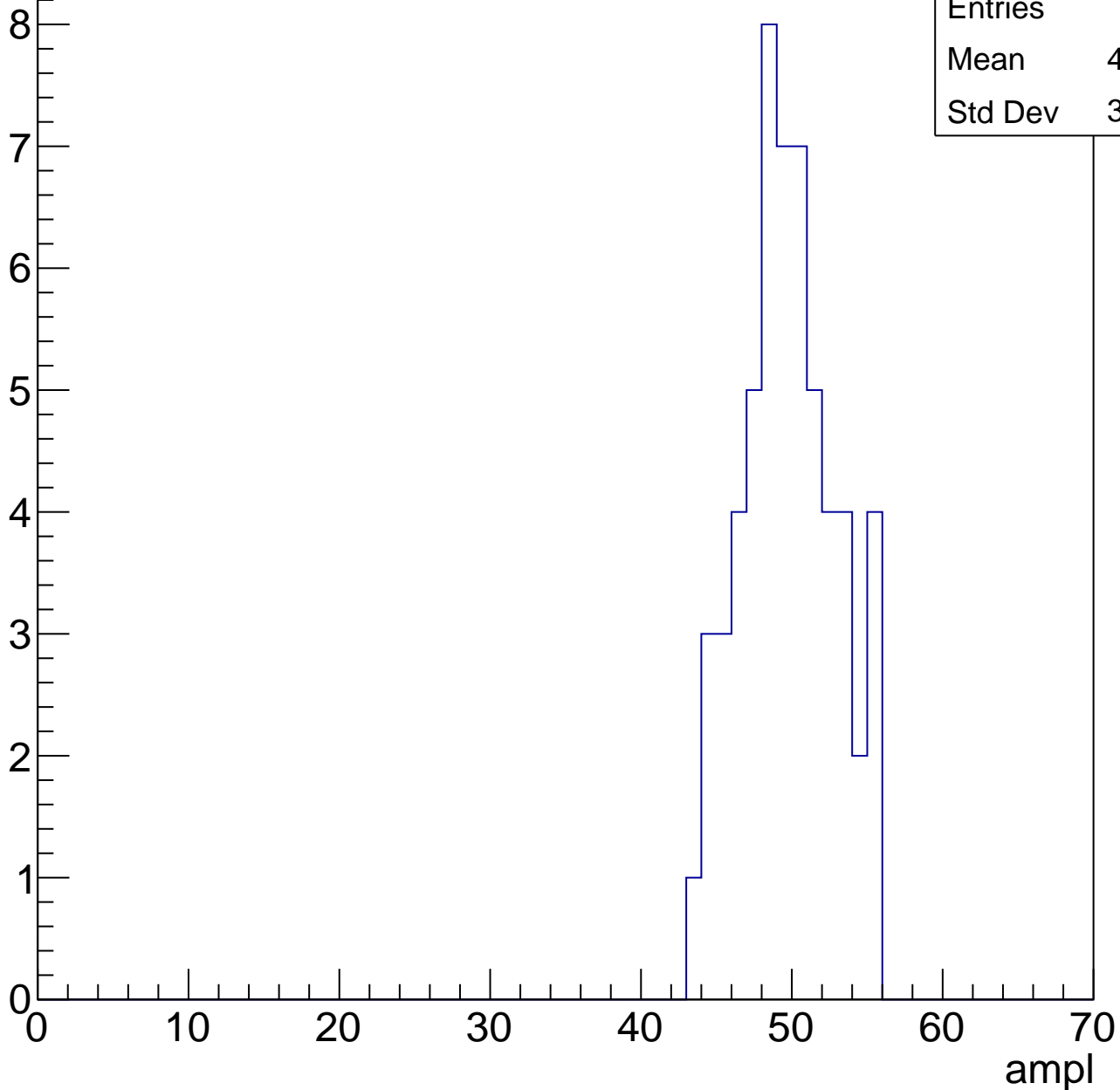


# B0L001S, U2-ch12, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 57    |
| Mean    | 49.28 |
| Std Dev | 3.077 |

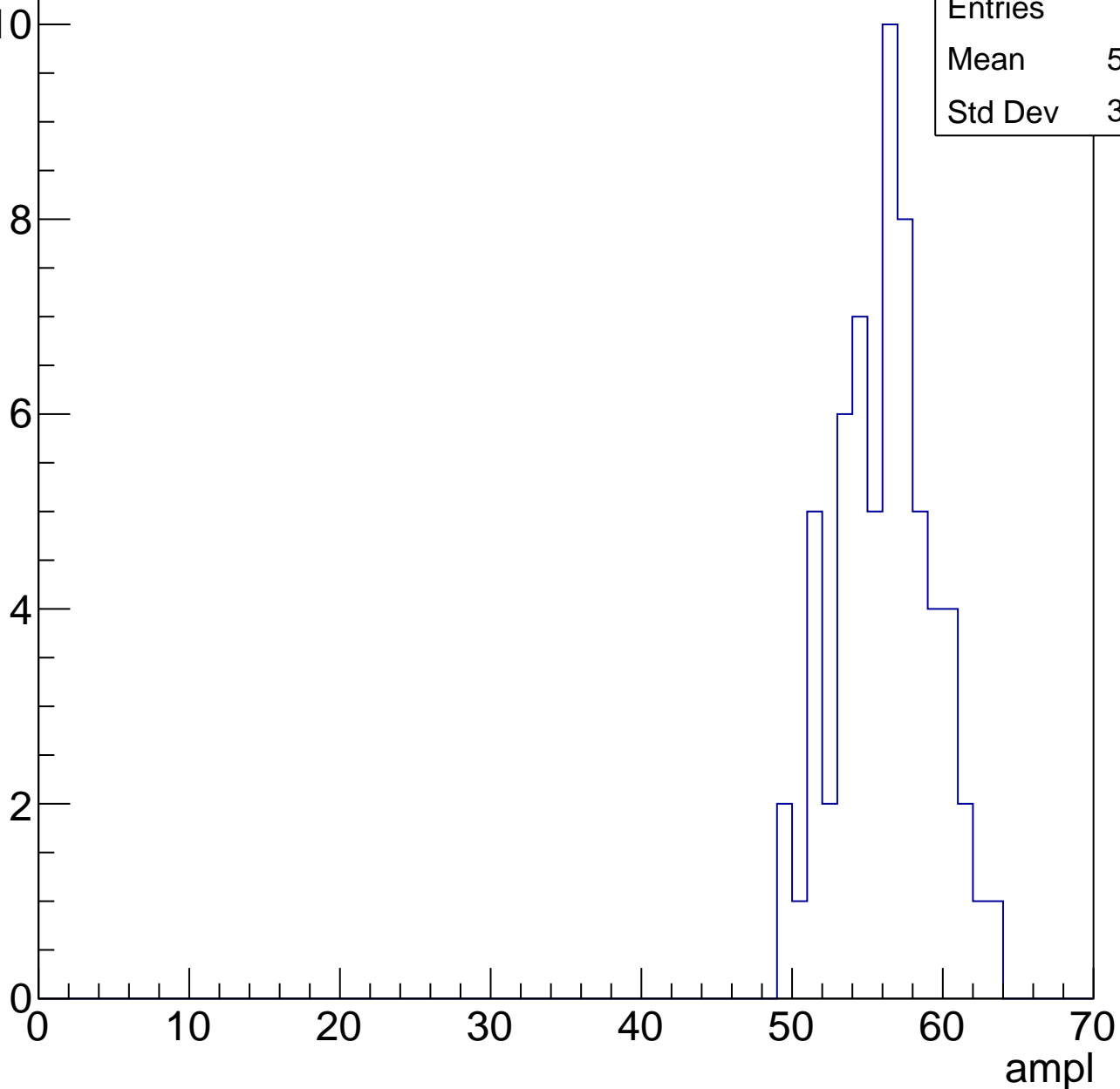


# B0L001S, U2-ch12, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 63    |
| Mean    | 55.67 |
| Std Dev | 3.172 |

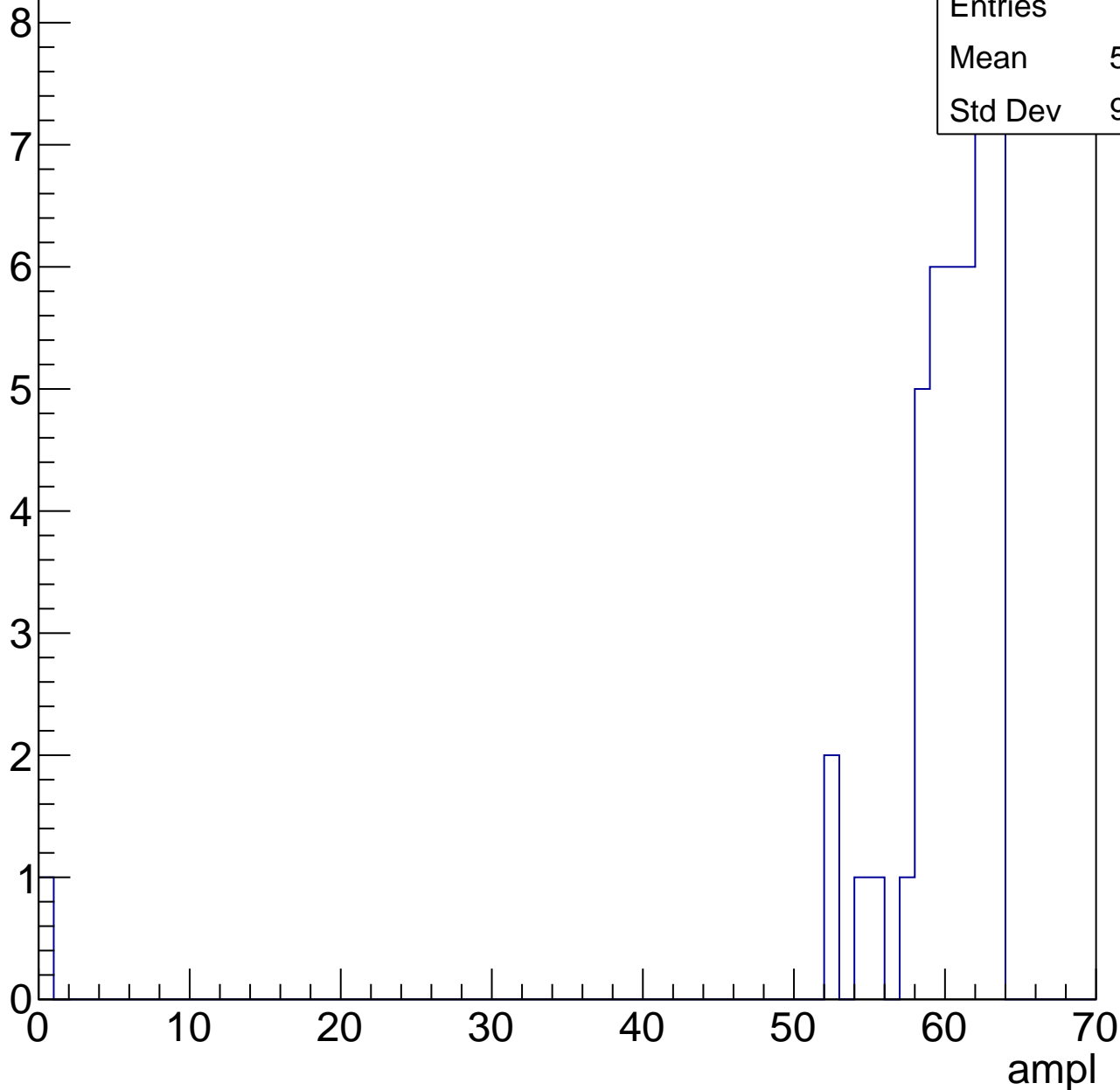


# B0L001S, U2-ch12, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

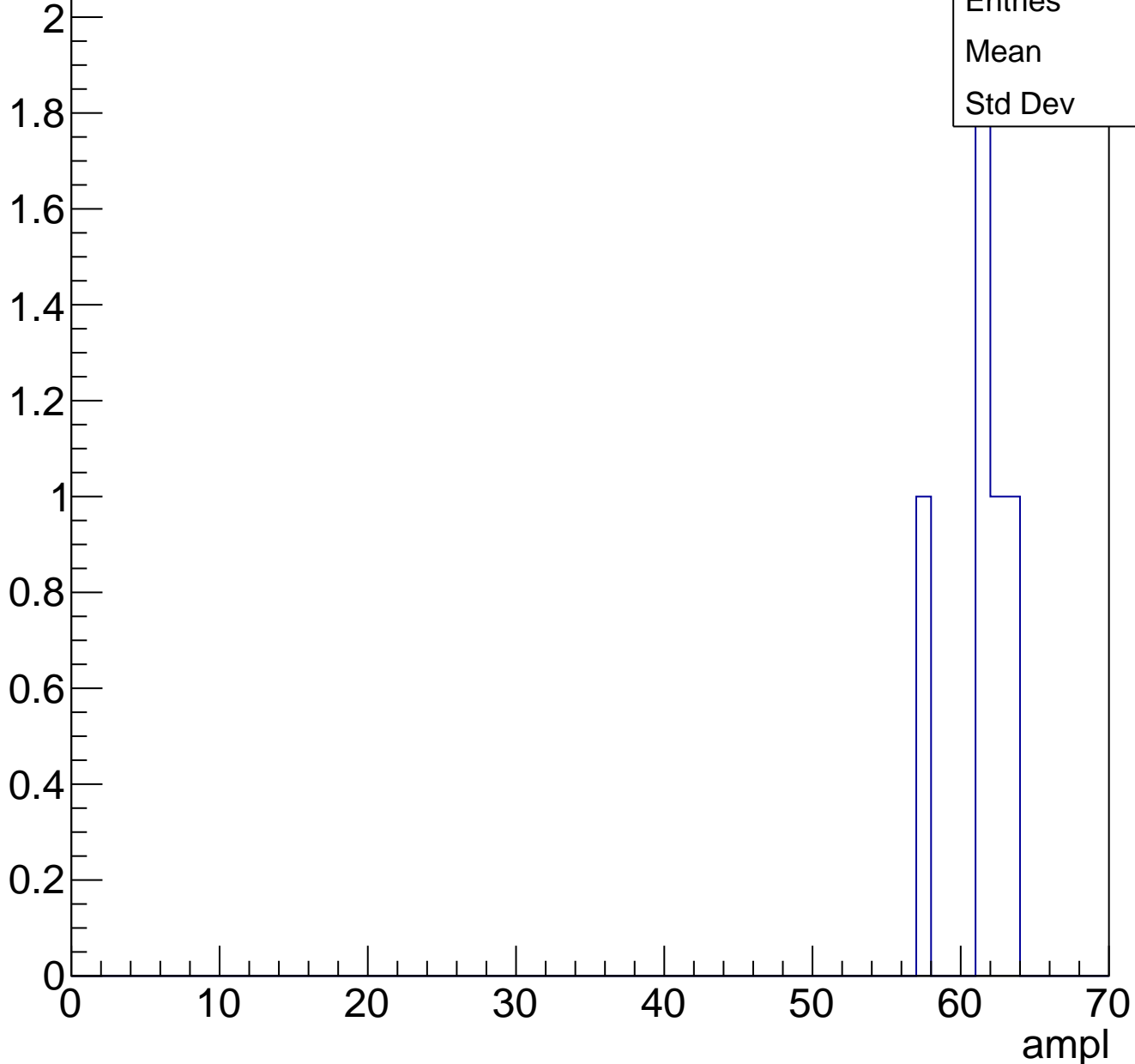
|         |       |
|---------|-------|
| Entries | 45    |
| Mean    | 58.67 |
| Std Dev | 9.254 |



# B0L001S, U2-ch12, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |      |
|---------|------|
| Entries | 5    |
| Mean    | 60.8 |
| Std Dev | 2.04 |



# B0L001S, U2-ch12, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 1 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch13, adc0

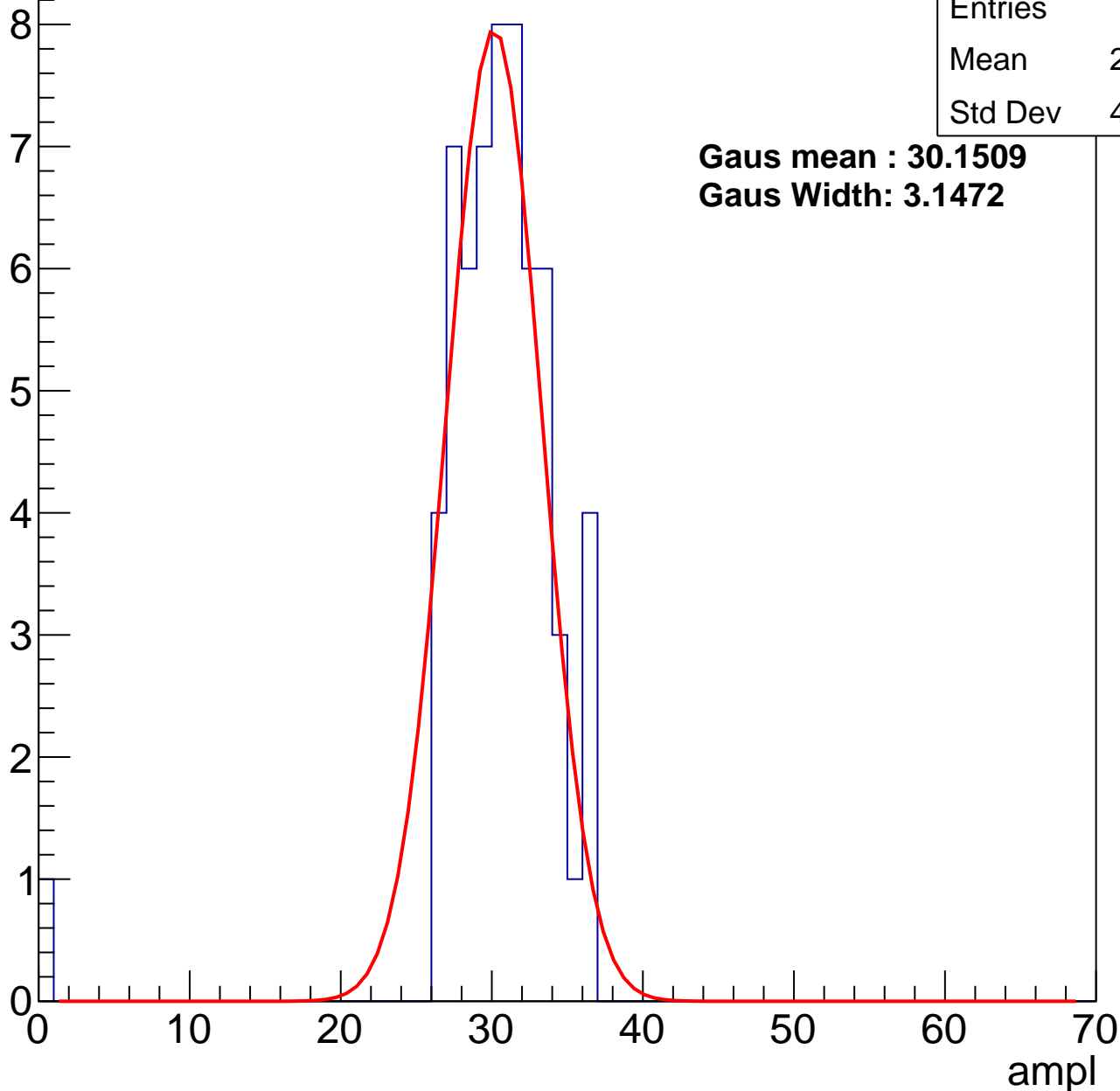
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 61    |
| Mean    | 29.89 |
| Std Dev | 4.722 |

**Gaus mean : 30.1509**

**Gaus Width: 3.1472**



# B0L001S, U2-ch13, adc1

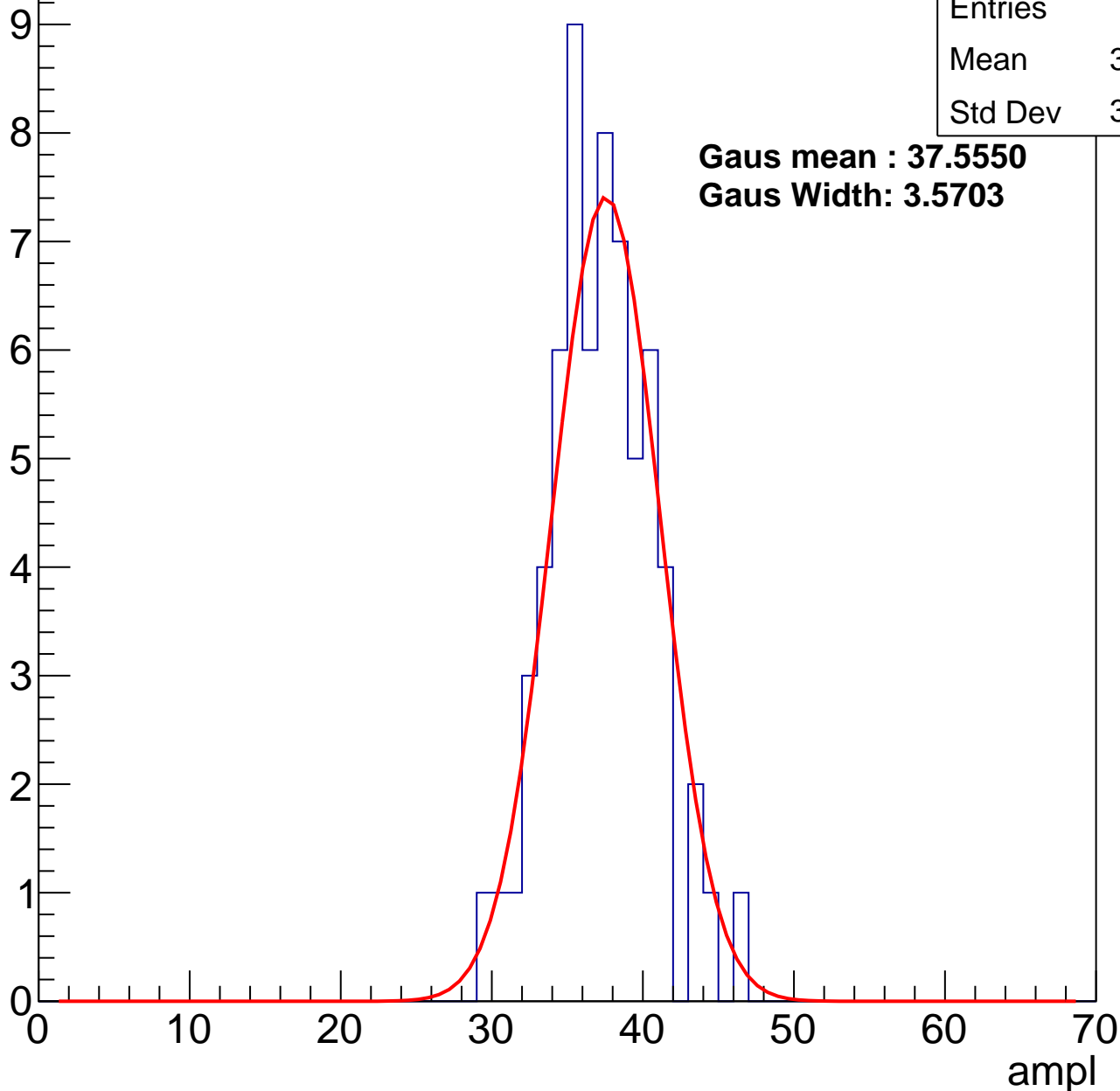
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 65    |
| Mean    | 36.77 |
| Std Dev | 3.346 |

**Gaus mean : 37.5550**

**Gaus Width: 3.5703**



# B0L001S, U2-ch13, adc2

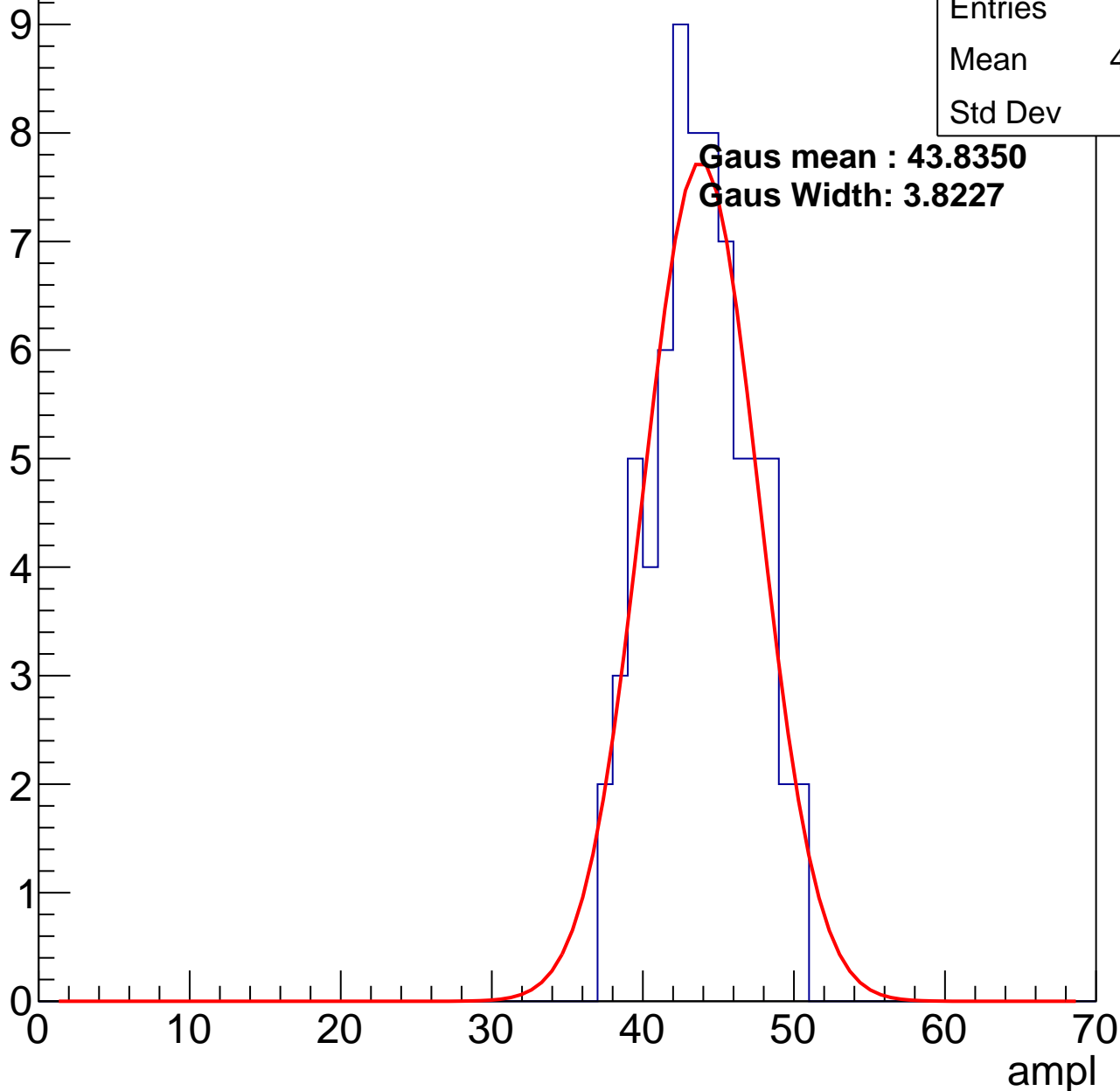
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 71    |
| Mean    | 43.39 |
| Std Dev | 3.23  |

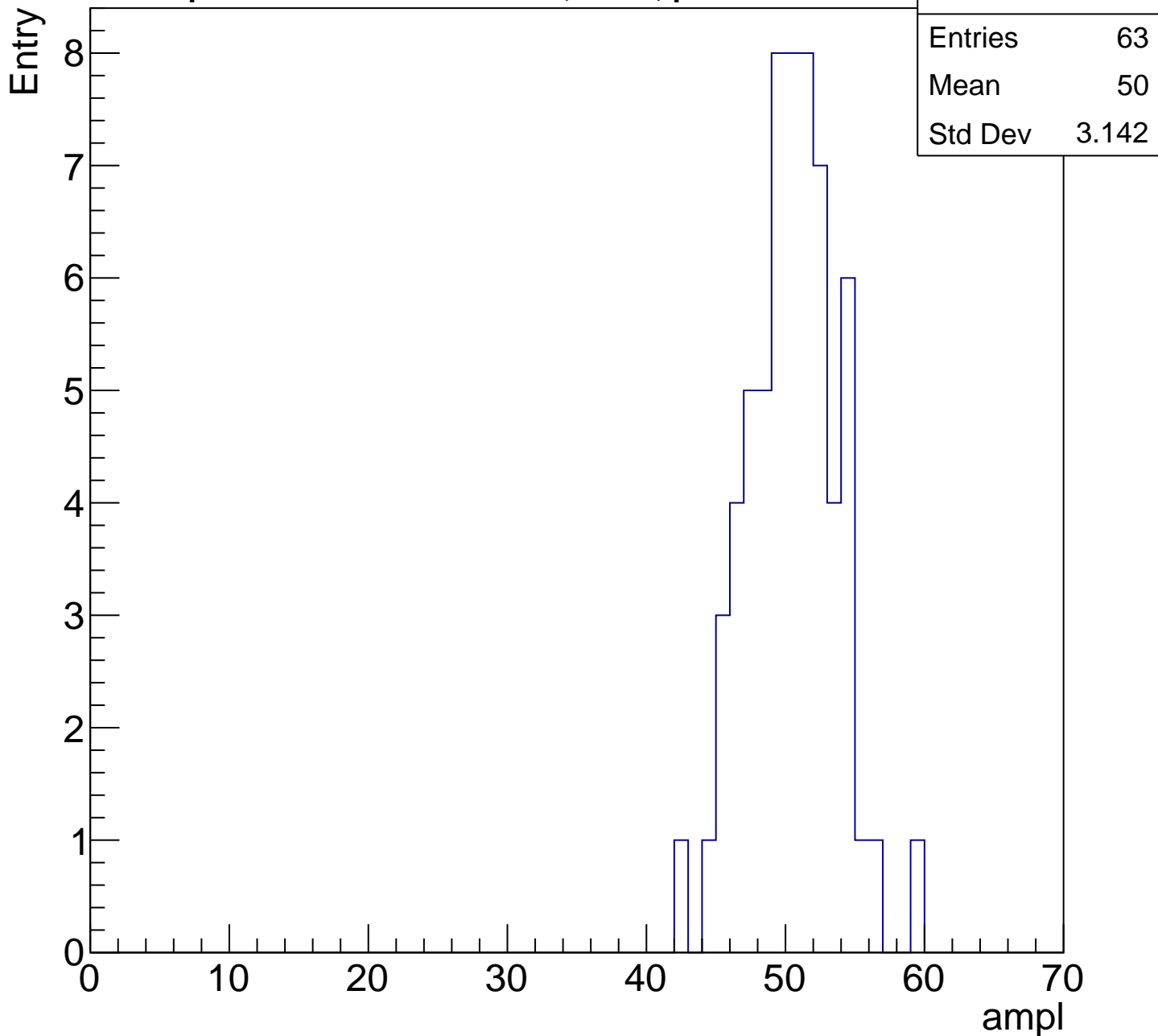
**Gaus mean : 43.8350**

**Gaus Width: 3.8227**



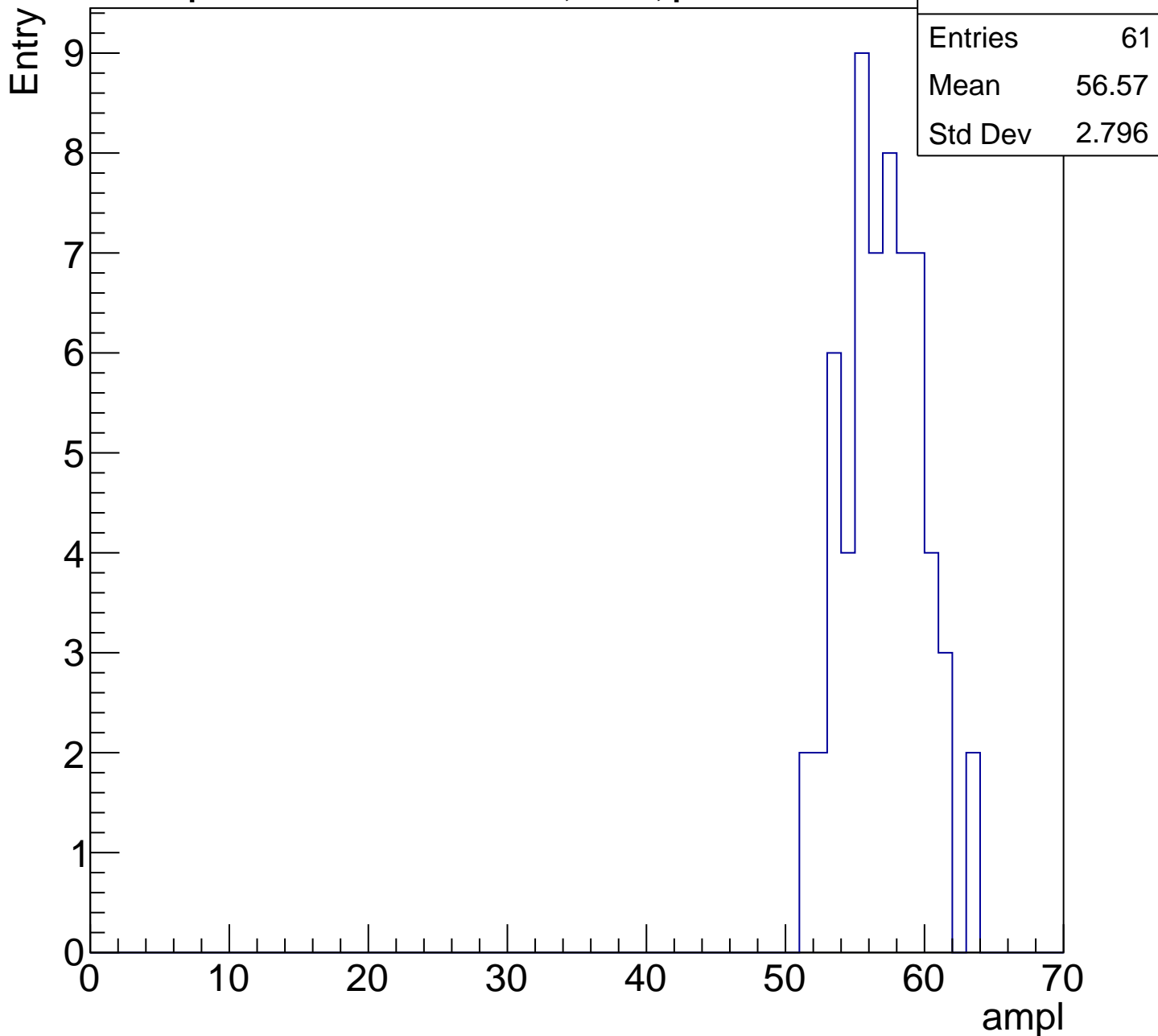
# B0L001S, U2-ch13, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U2-ch13, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

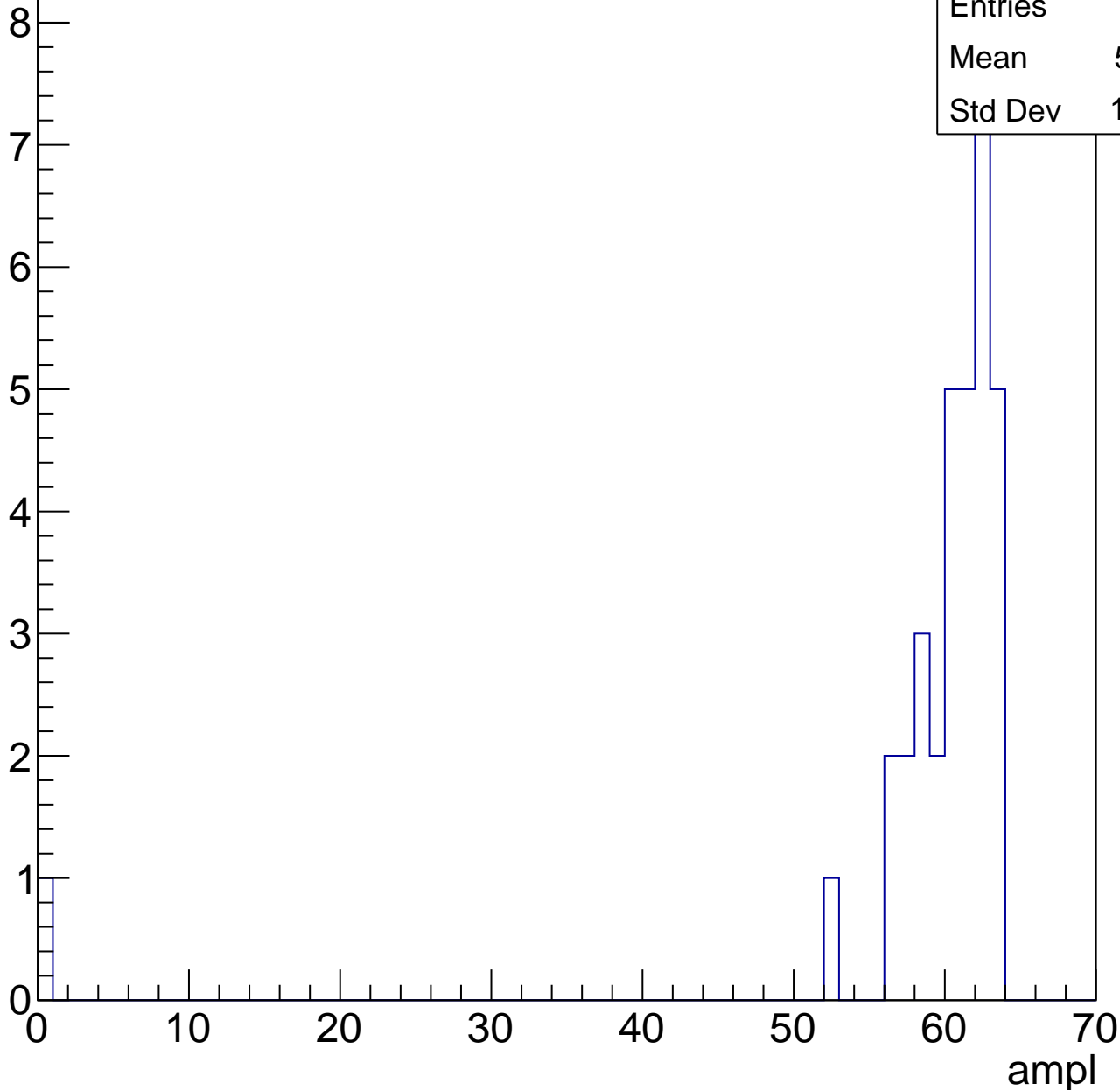


# B0L001S, U2-ch13, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

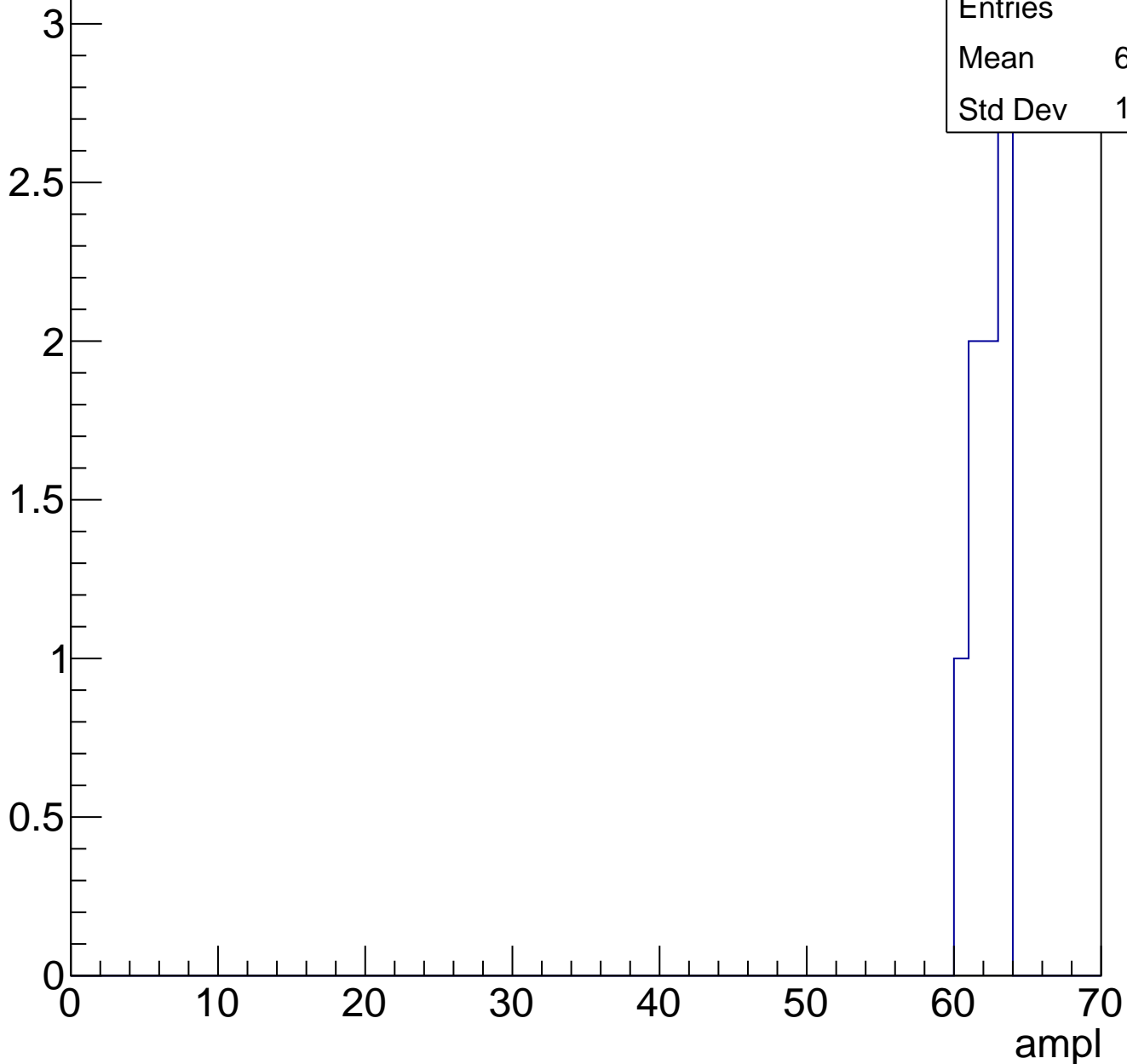
|         |       |
|---------|-------|
| Entries | 34    |
| Mean    | 58.41 |
| Std Dev | 10.47 |



# B0L001S, U2-ch13, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch13, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 1 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch14, adc0

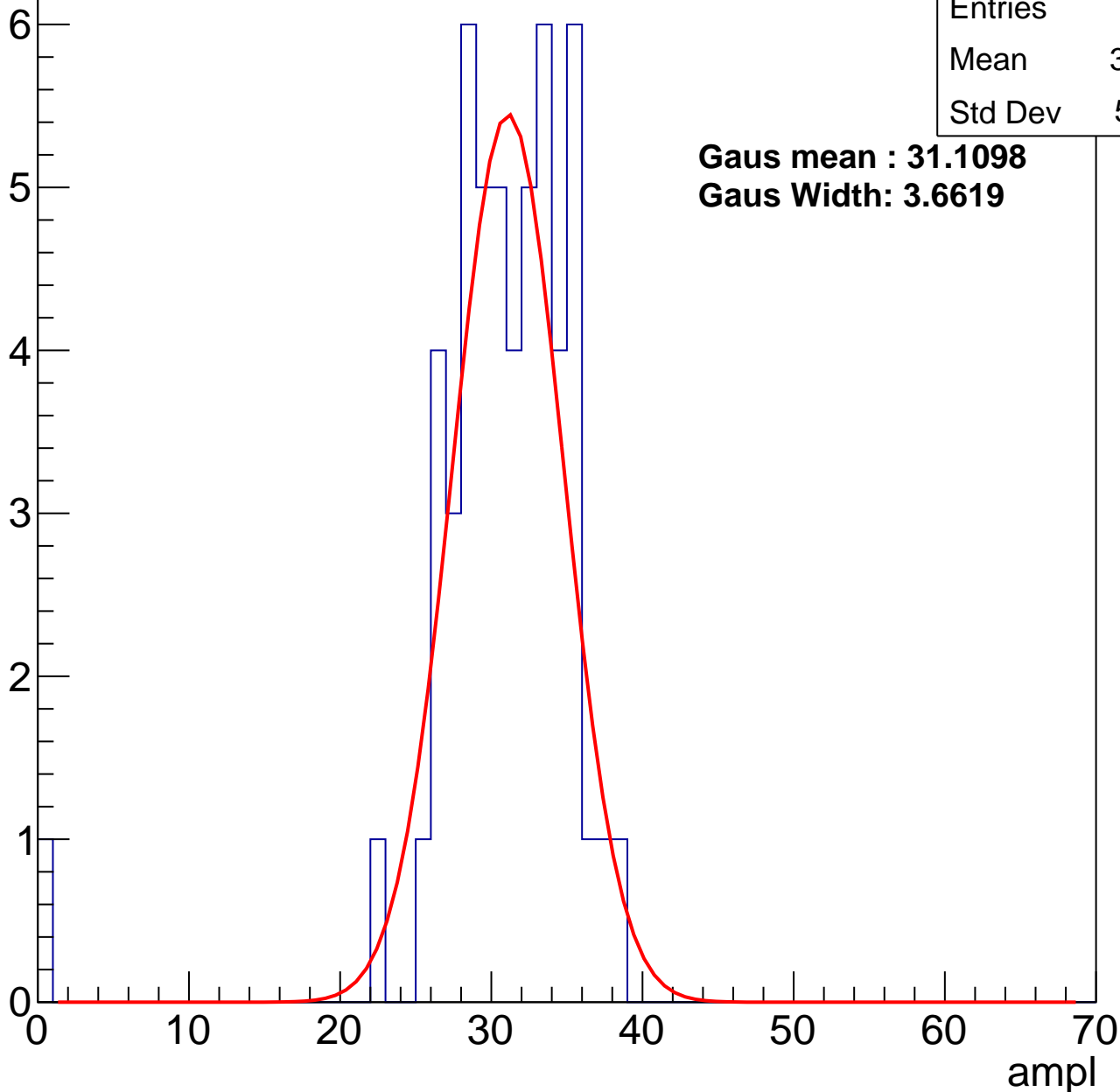
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 54    |
| Mean    | 30.26 |
| Std Dev | 5.351 |

**Gaus mean : 31.1098**

**Gaus Width: 3.6619**



# B0L001S, U2-ch14, adc1

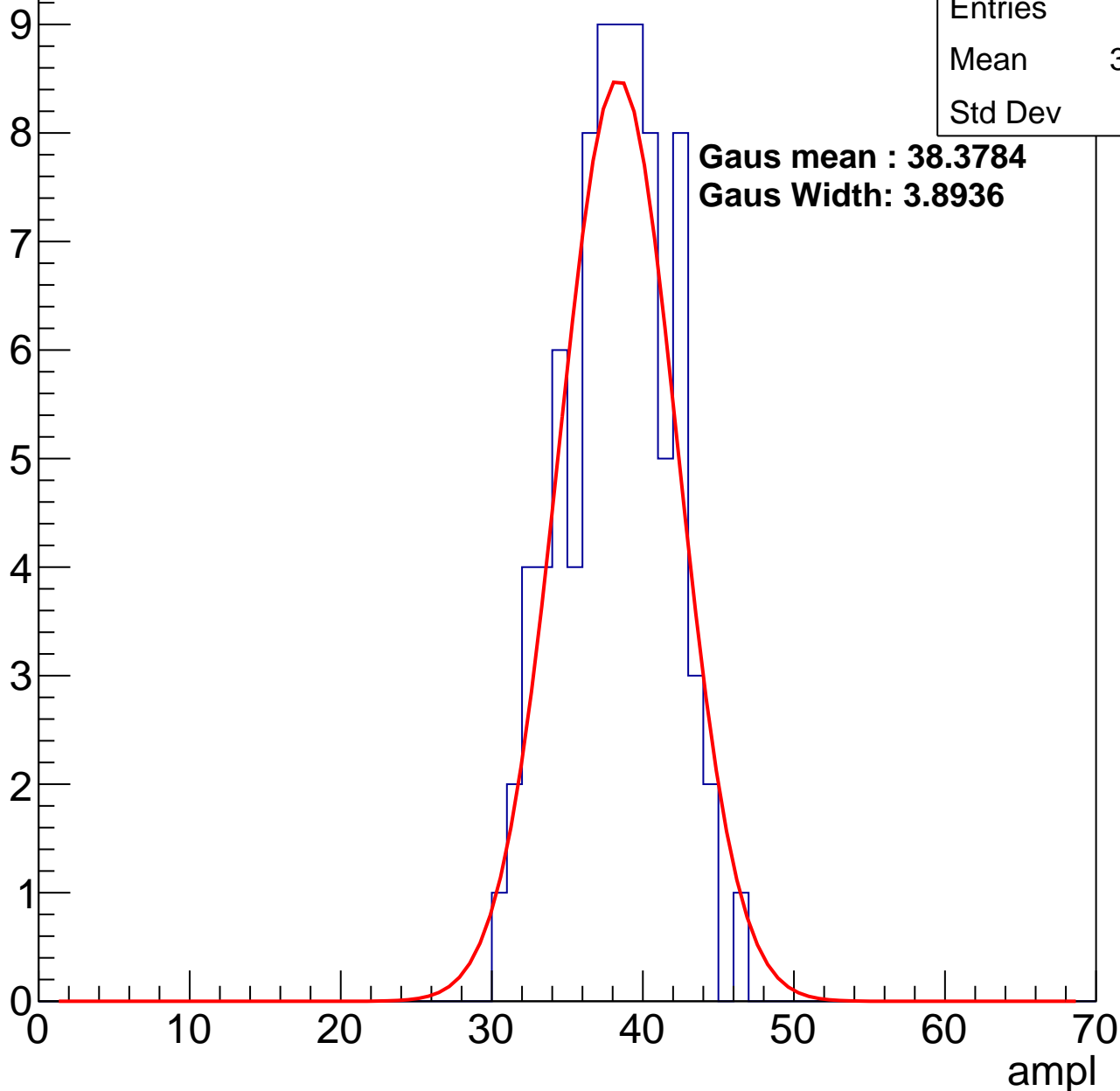
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 83    |
| Mean    | 37.76 |
| Std Dev | 3.47  |

**Gaus mean : 38.3784**

**Gaus Width: 3.8936**



# B0L001S, U2-ch14, adc2

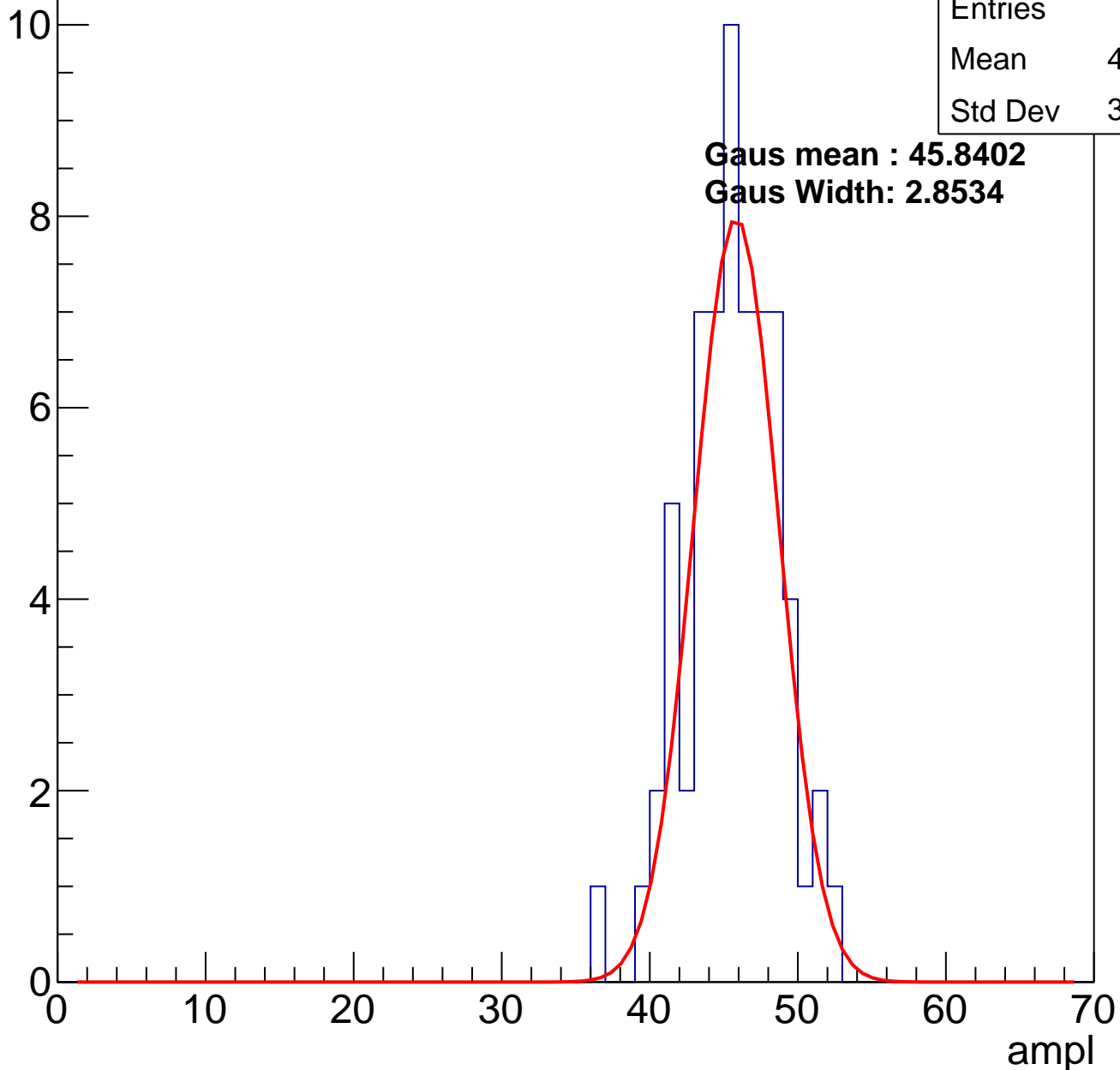
calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 64    |
| Mean    | 45.16 |
| Std Dev | 3.078 |

**Gaus mean : 45.8402**

**Gaus Width: 2.8534**

Entry

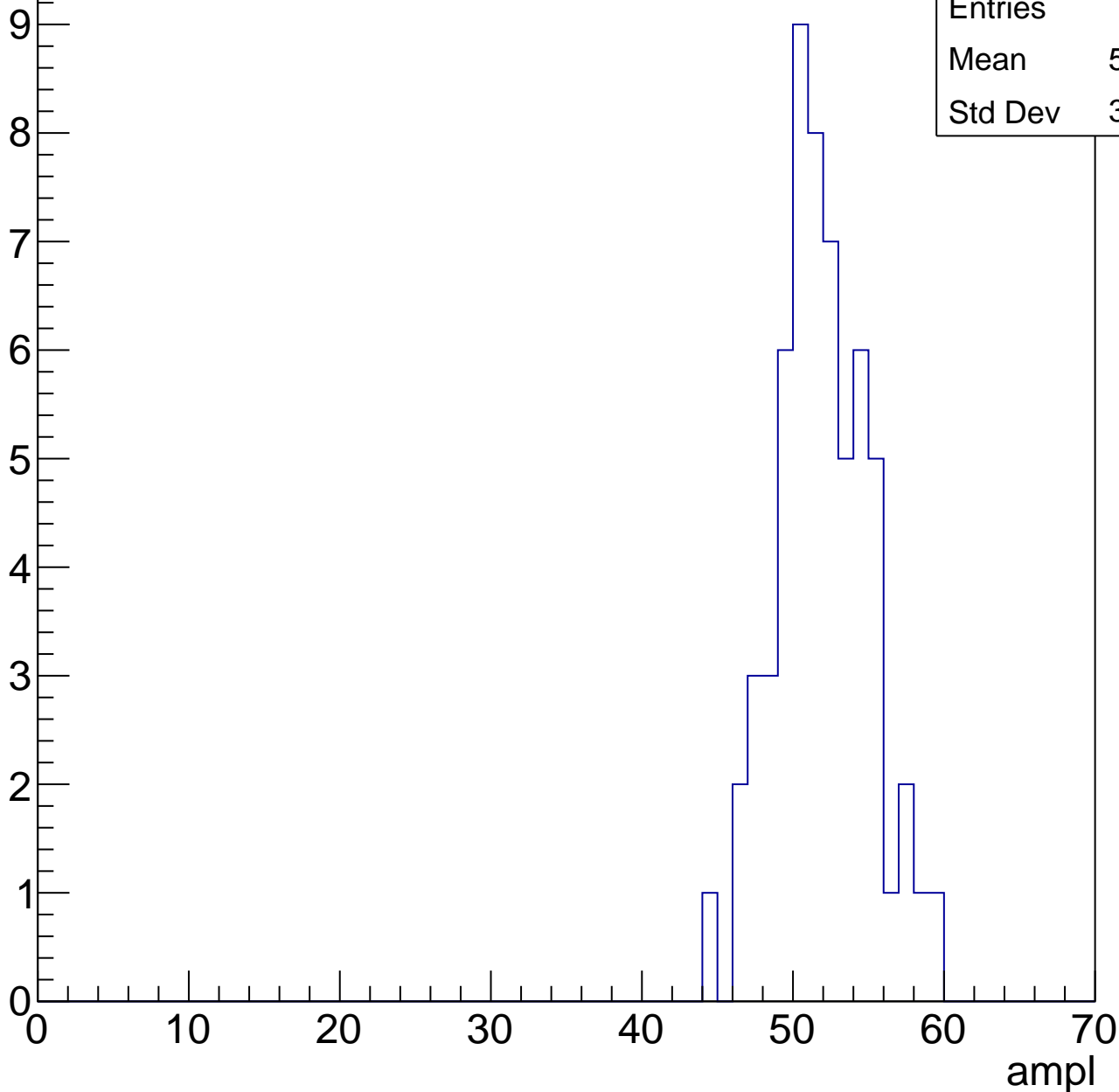


# B0L001S, U2-ch14, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

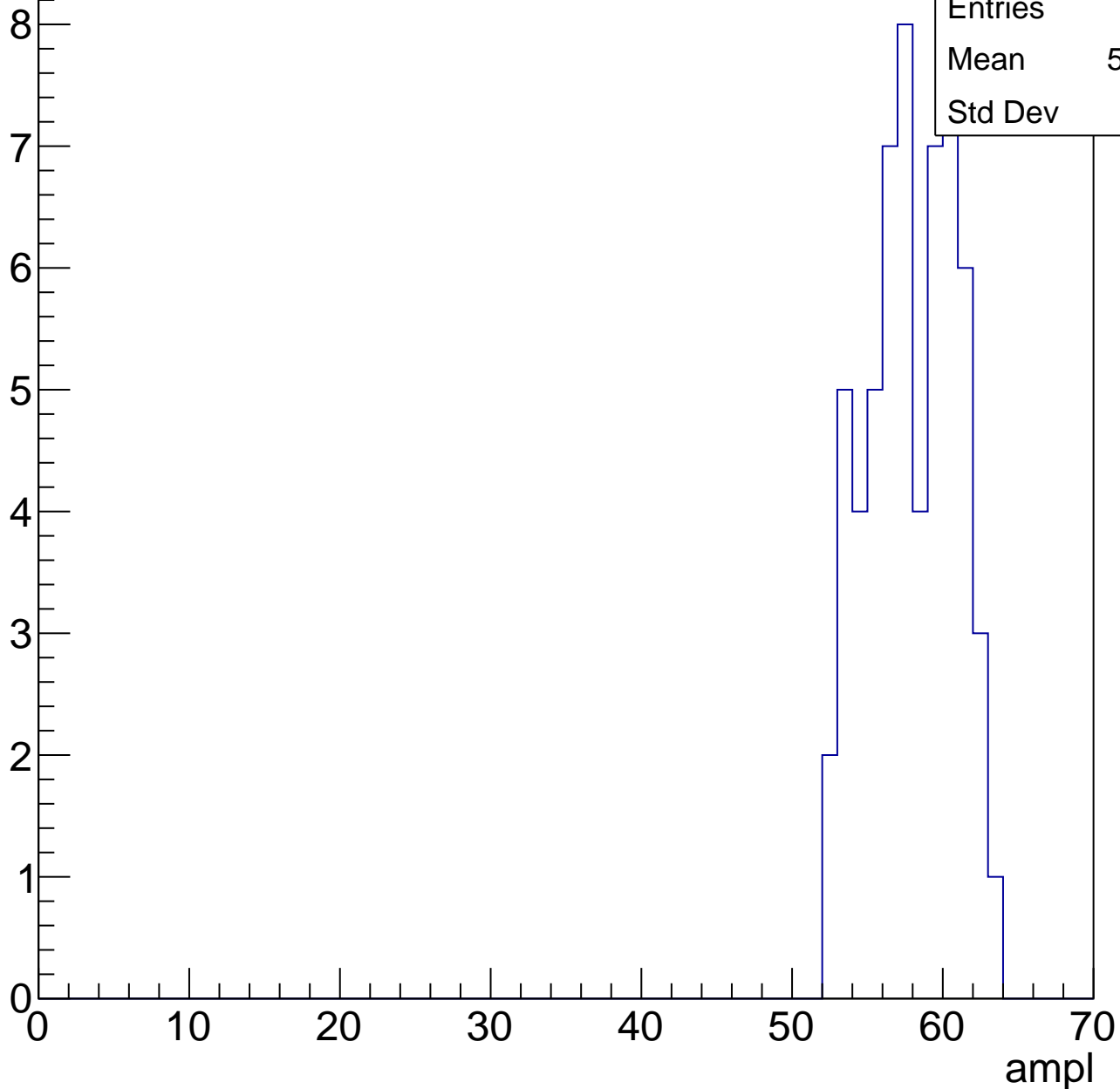
|         |       |
|---------|-------|
| Entries | 60    |
| Mean    | 51.47 |
| Std Dev | 3.068 |



# B0L001S, U2-ch14, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

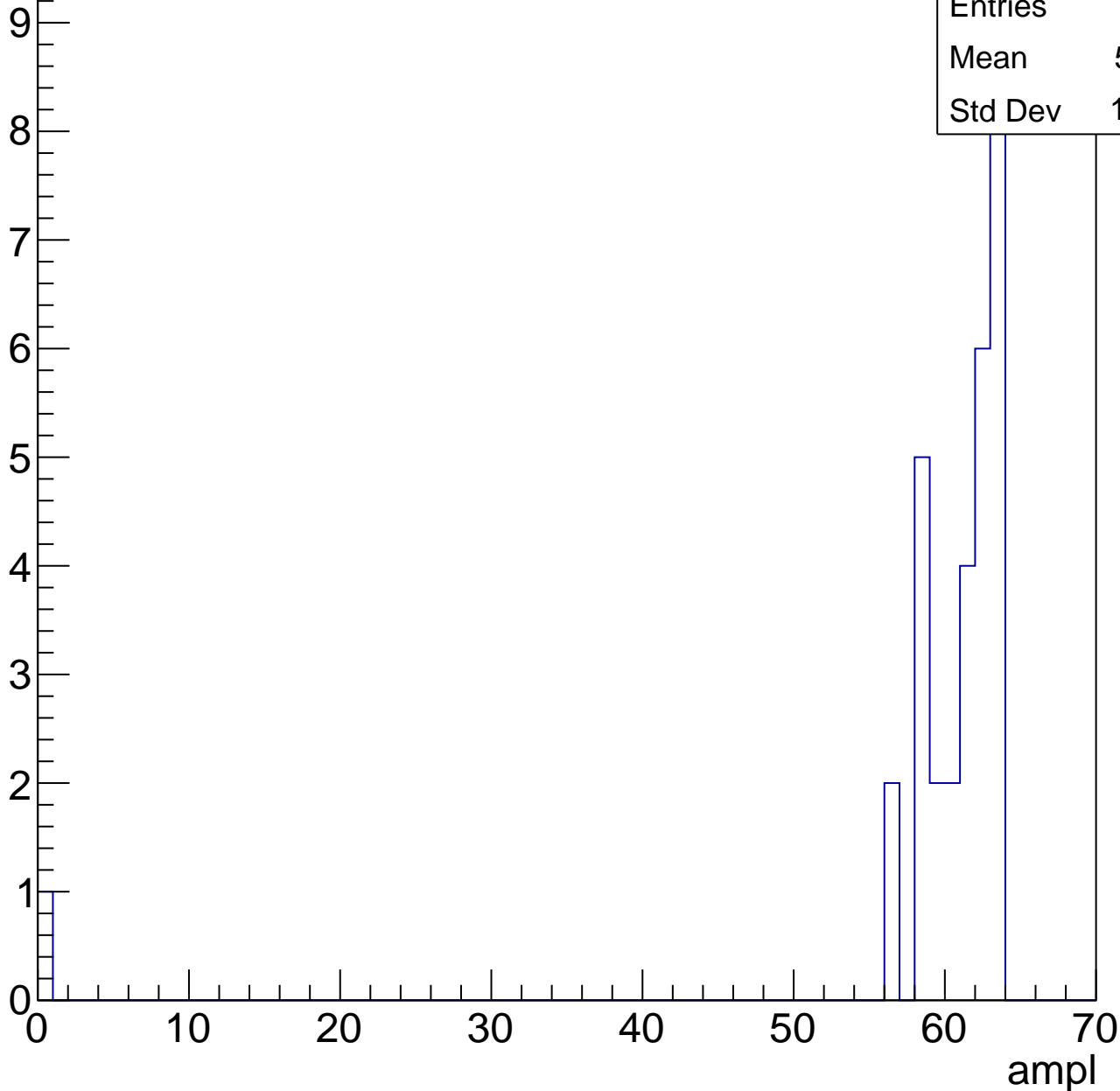


# B0L001S, U2-ch14, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 31    |
| Mean    | 58.81 |
| Std Dev | 10.95 |



# B0L001S, U2-ch14, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch14, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 1 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch15, adc0

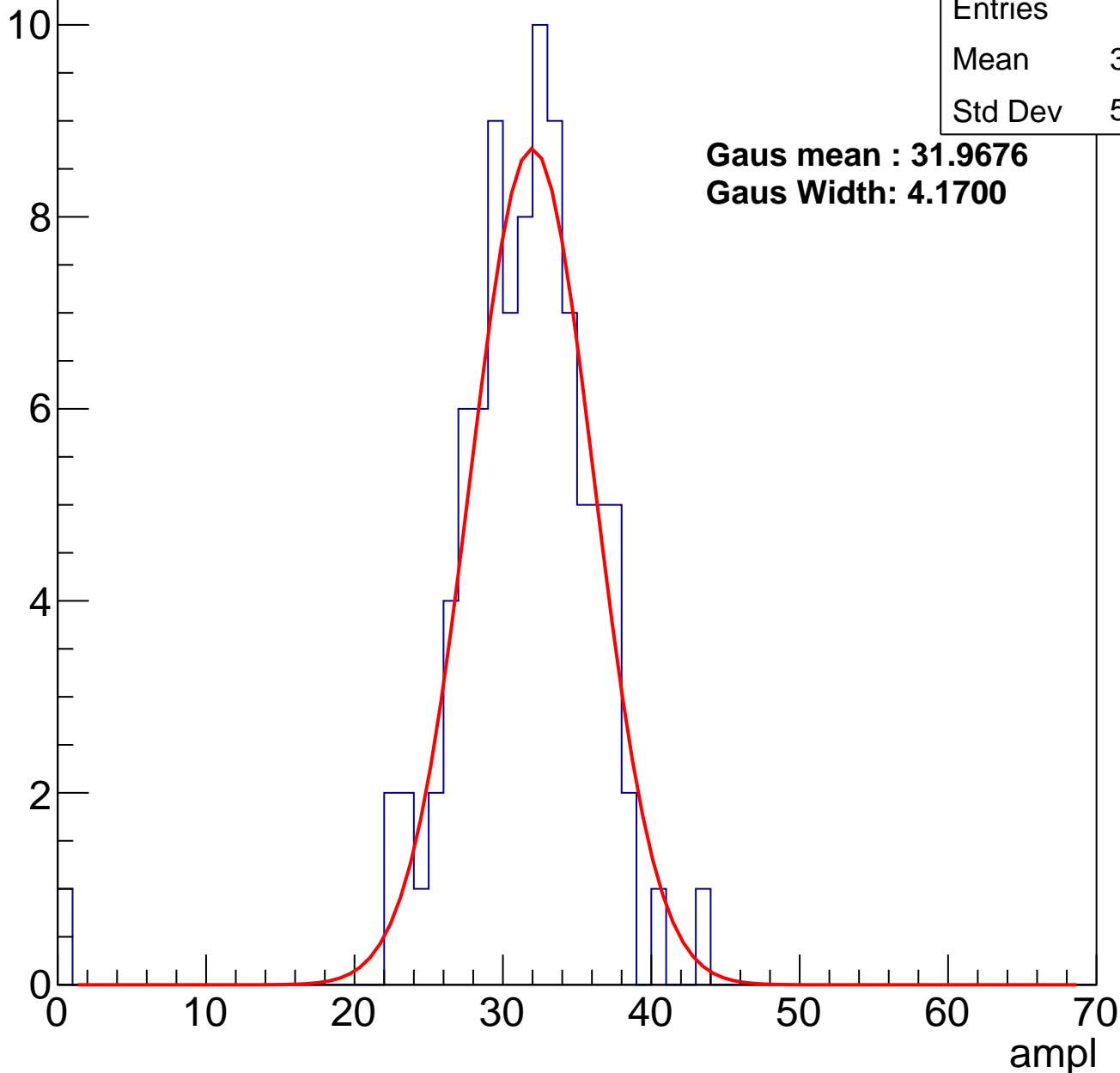
calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 93    |
| Mean    | 30.87 |
| Std Dev | 5.164 |

**Gaus mean : 31.9676**

**Gaus Width: 4.1700**

Entry



# B0L001S, U2-ch15, adc1

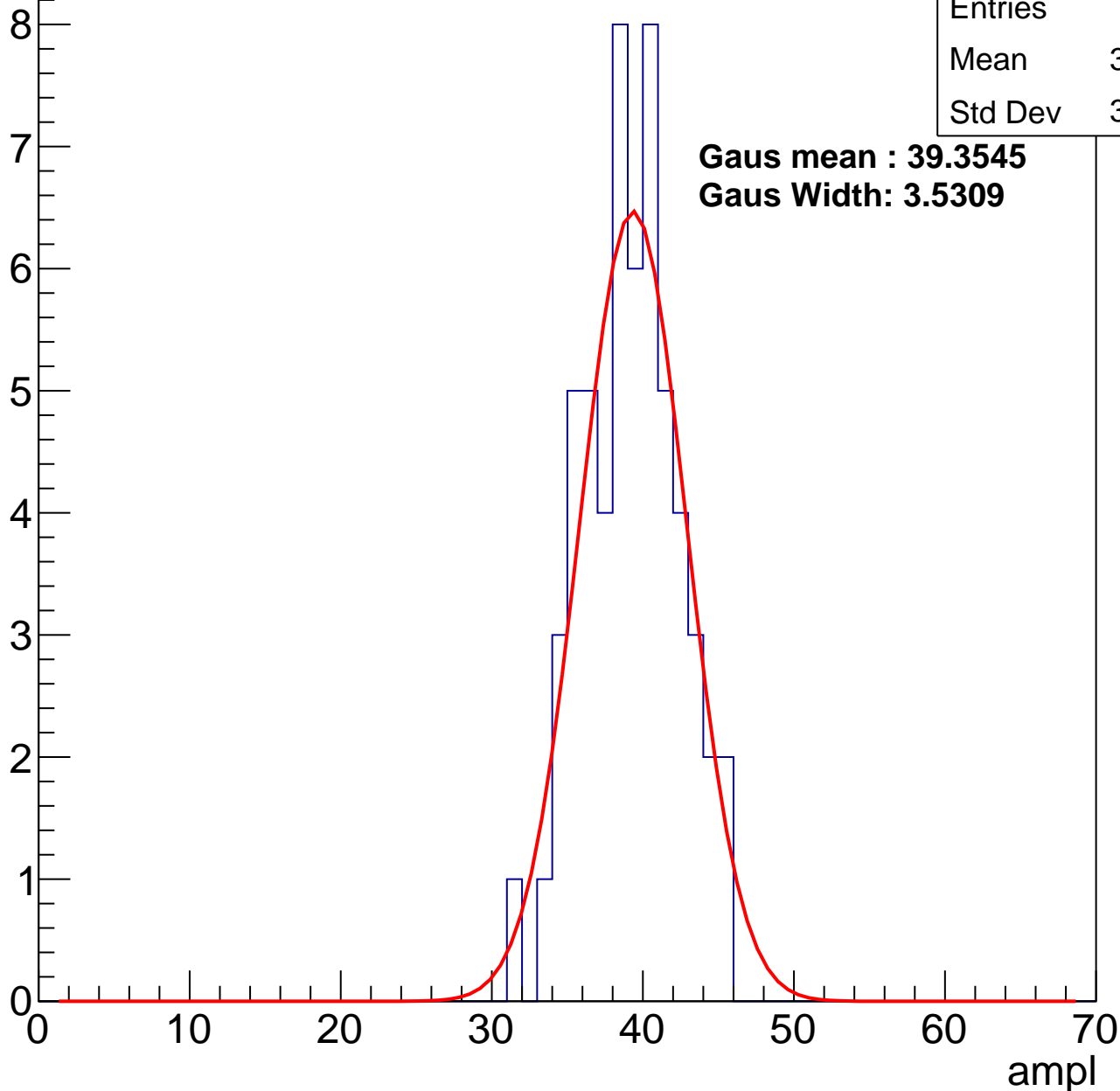
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 57    |
| Mean    | 38.72 |
| Std Dev | 3.116 |

**Gaus mean : 39.3545**

**Gaus Width: 3.5309**

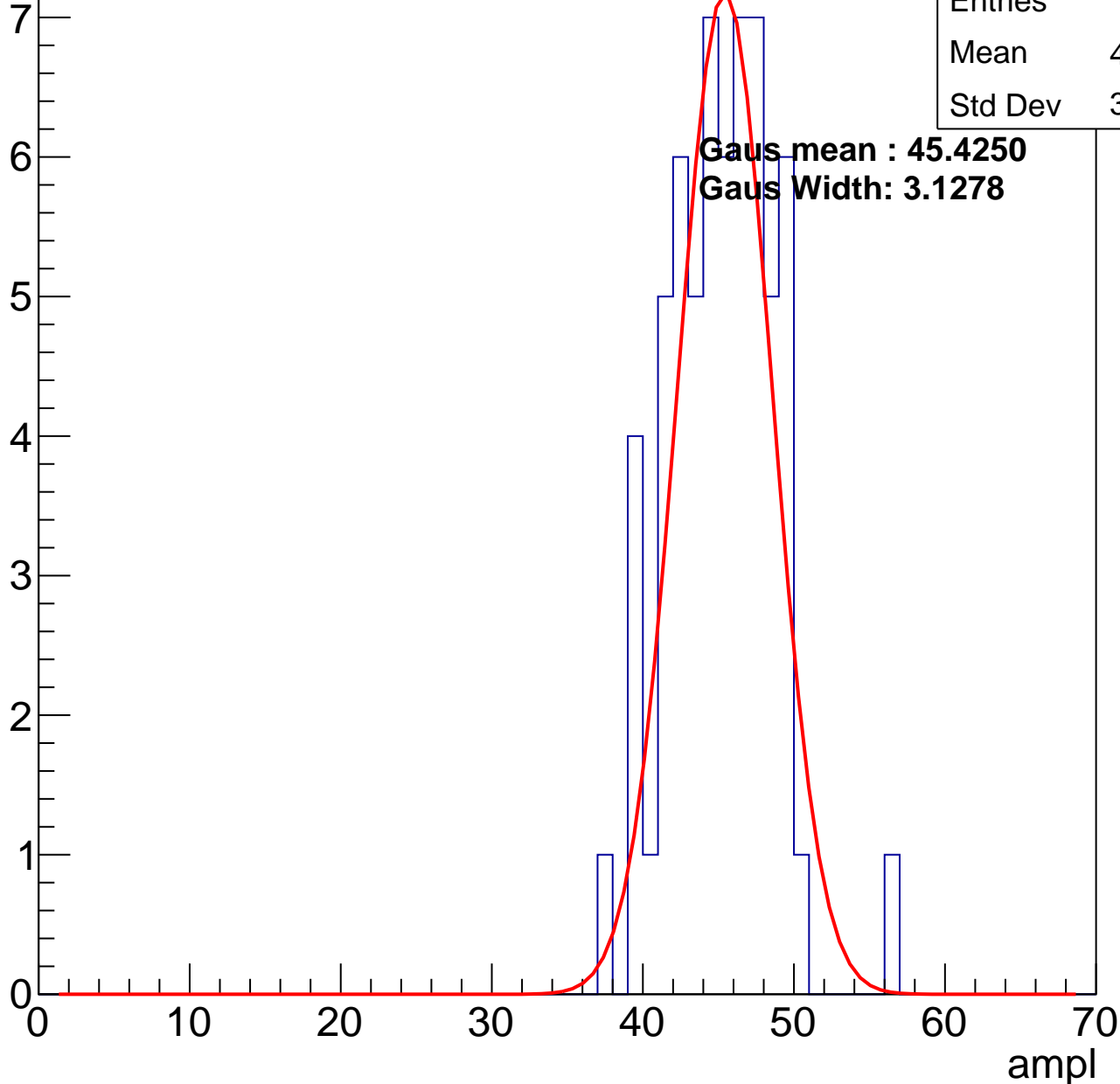


# B0L001S, U2-ch15, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 62    |
| Mean    | 44.74 |
| Std Dev | 3.388 |

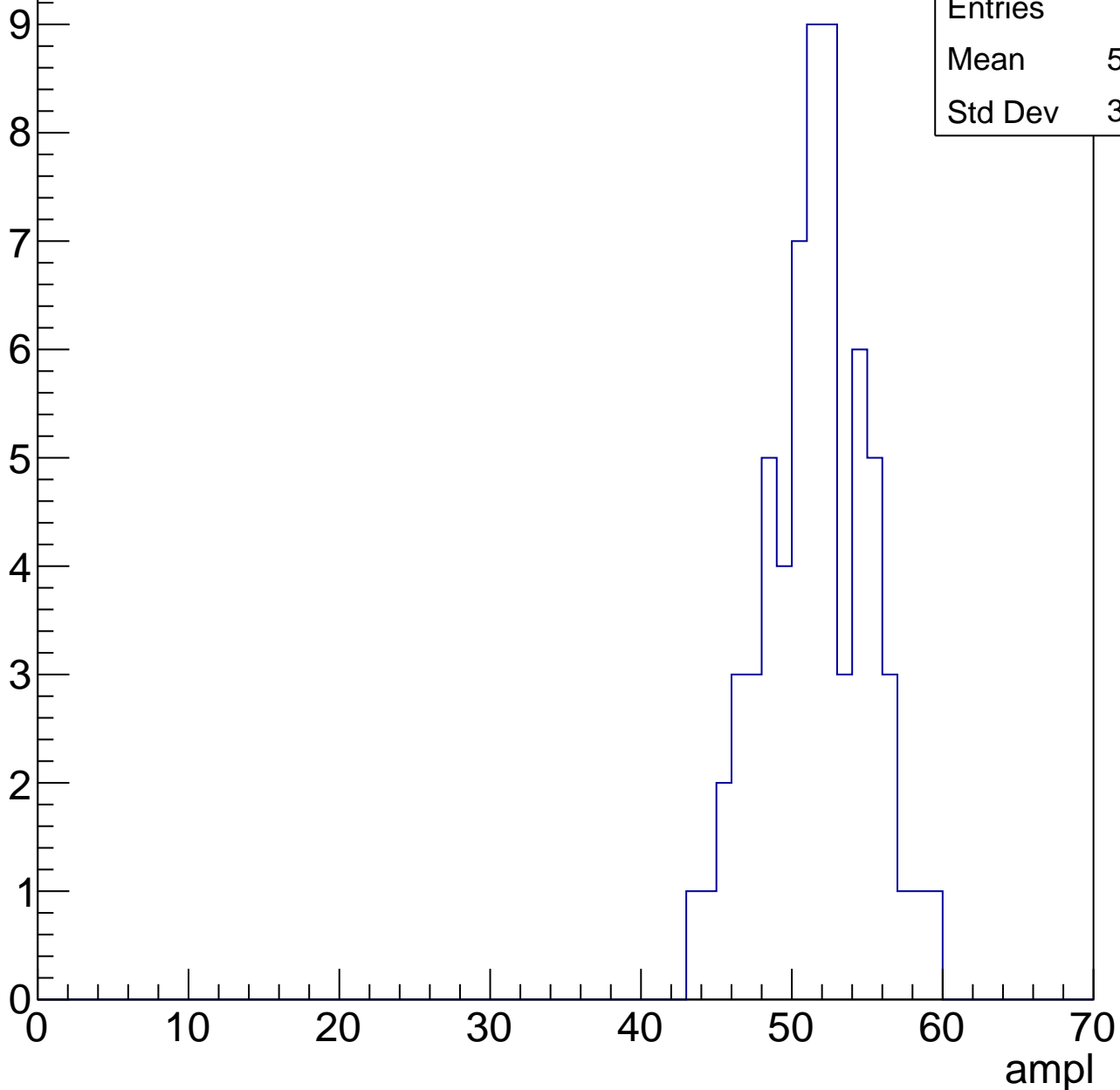


# B0L001S, U2-ch15, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 64    |
| Mean    | 51.08 |
| Std Dev | 3.434 |

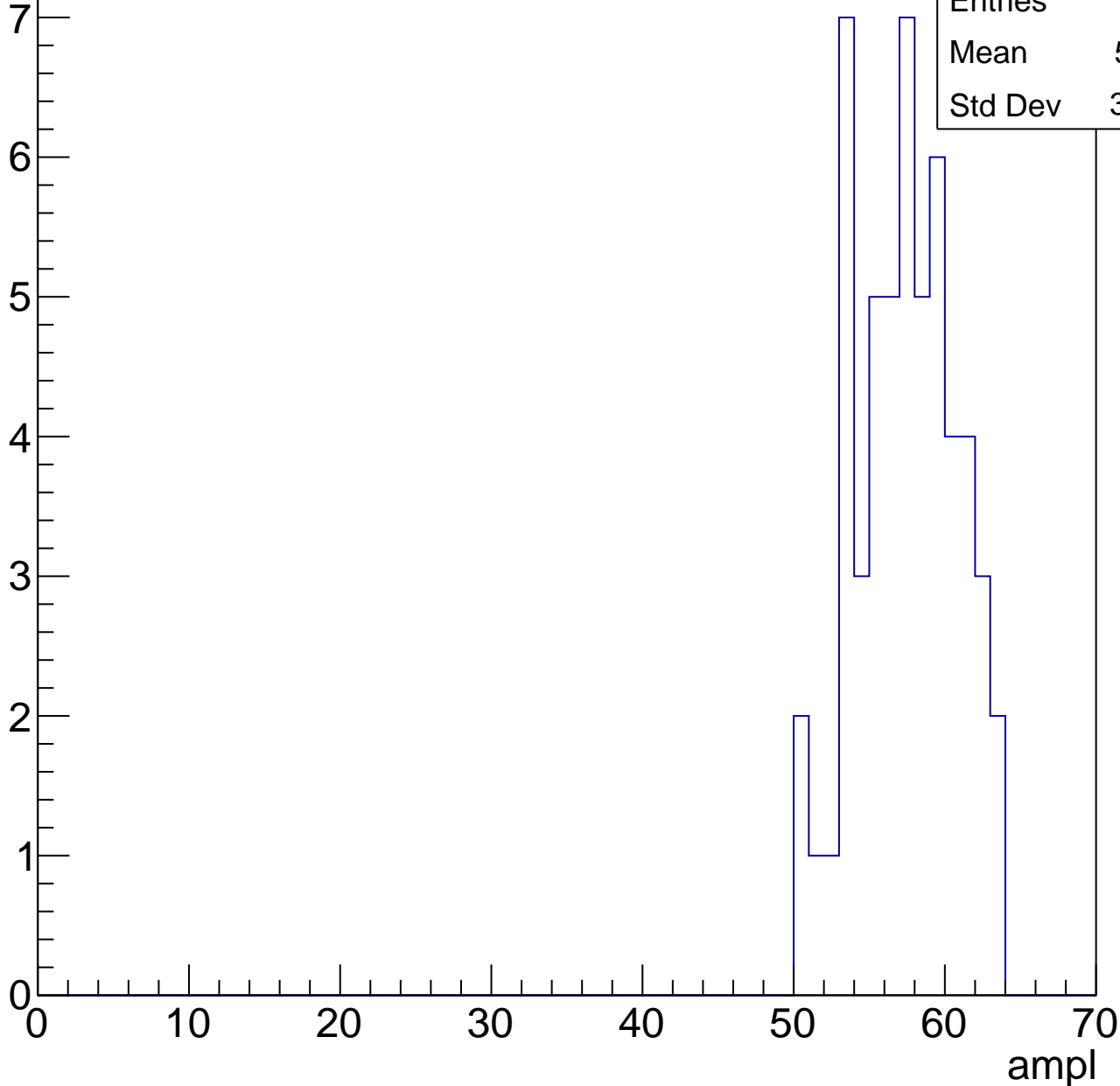


# B0L001S, U2-ch15, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

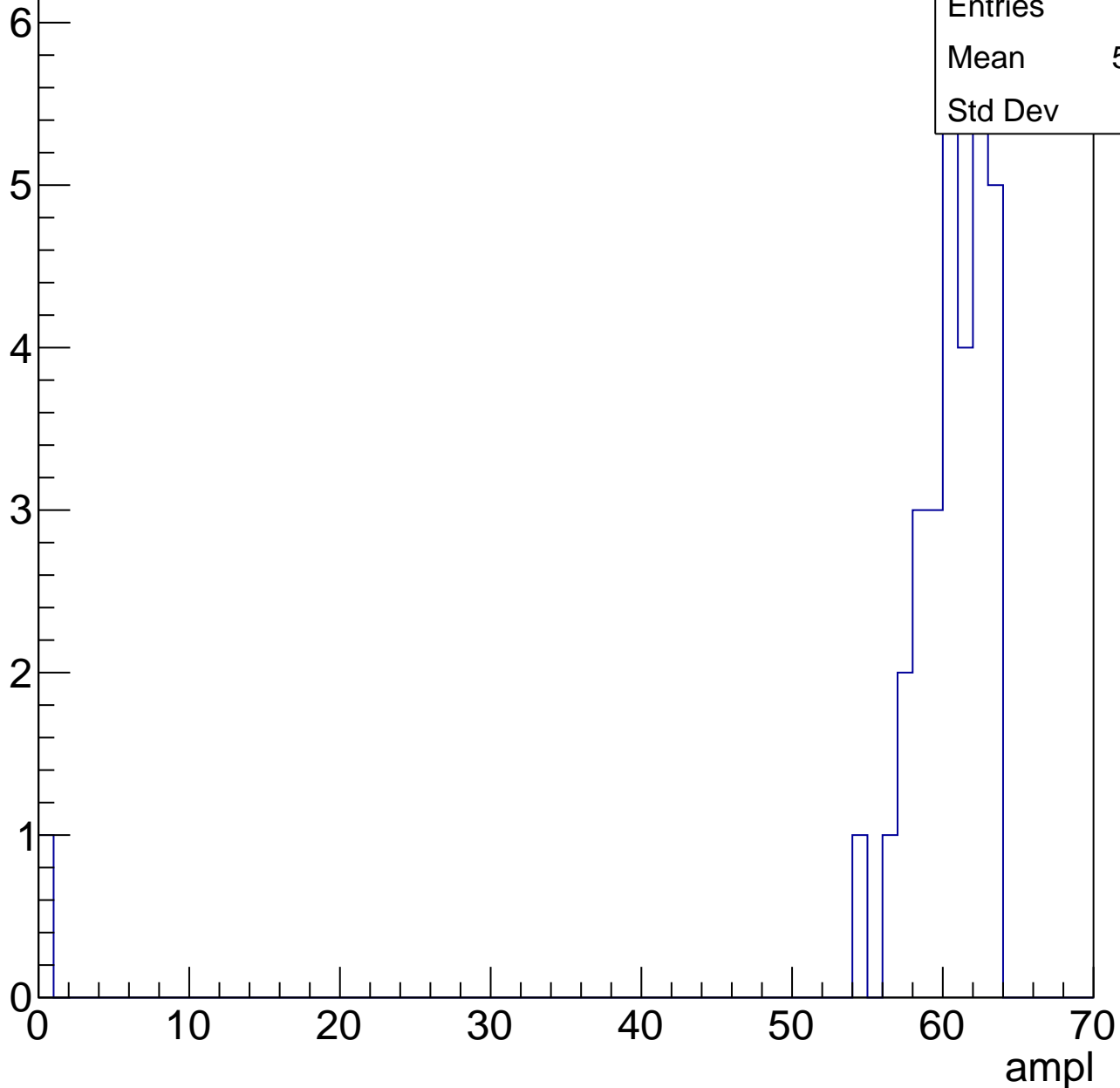
|         |       |
|---------|-------|
| Entries | 55    |
| Mean    | 56.91 |
| Std Dev | 3.299 |



# B0L001S, U2-ch15, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

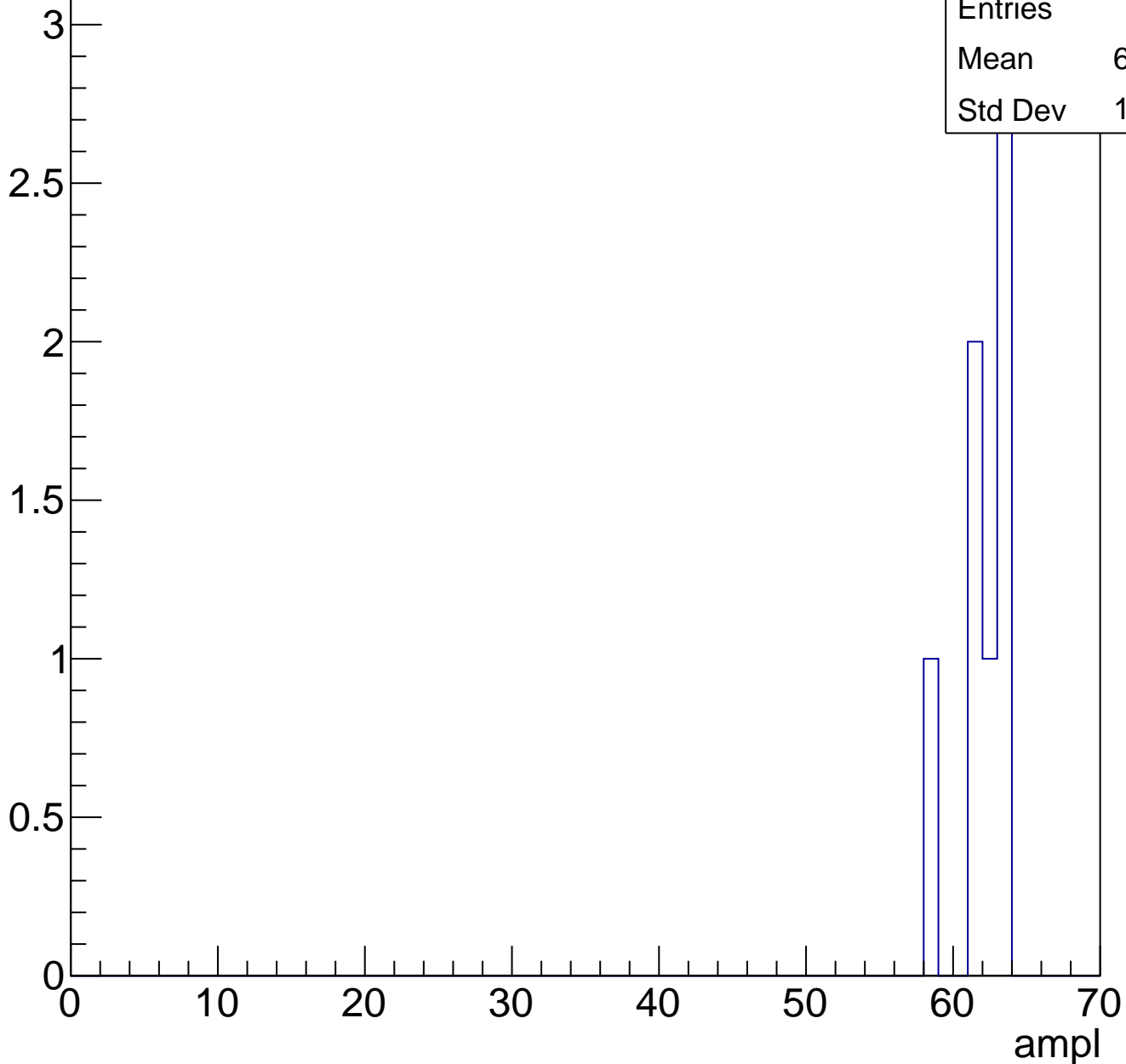
Entry



# B0L001S, U2-ch15, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch15, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U2-ch16, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 72    |
| Mean    | 30.51 |
| Std Dev | 4.964 |

**Gaus mean : 31.5907**

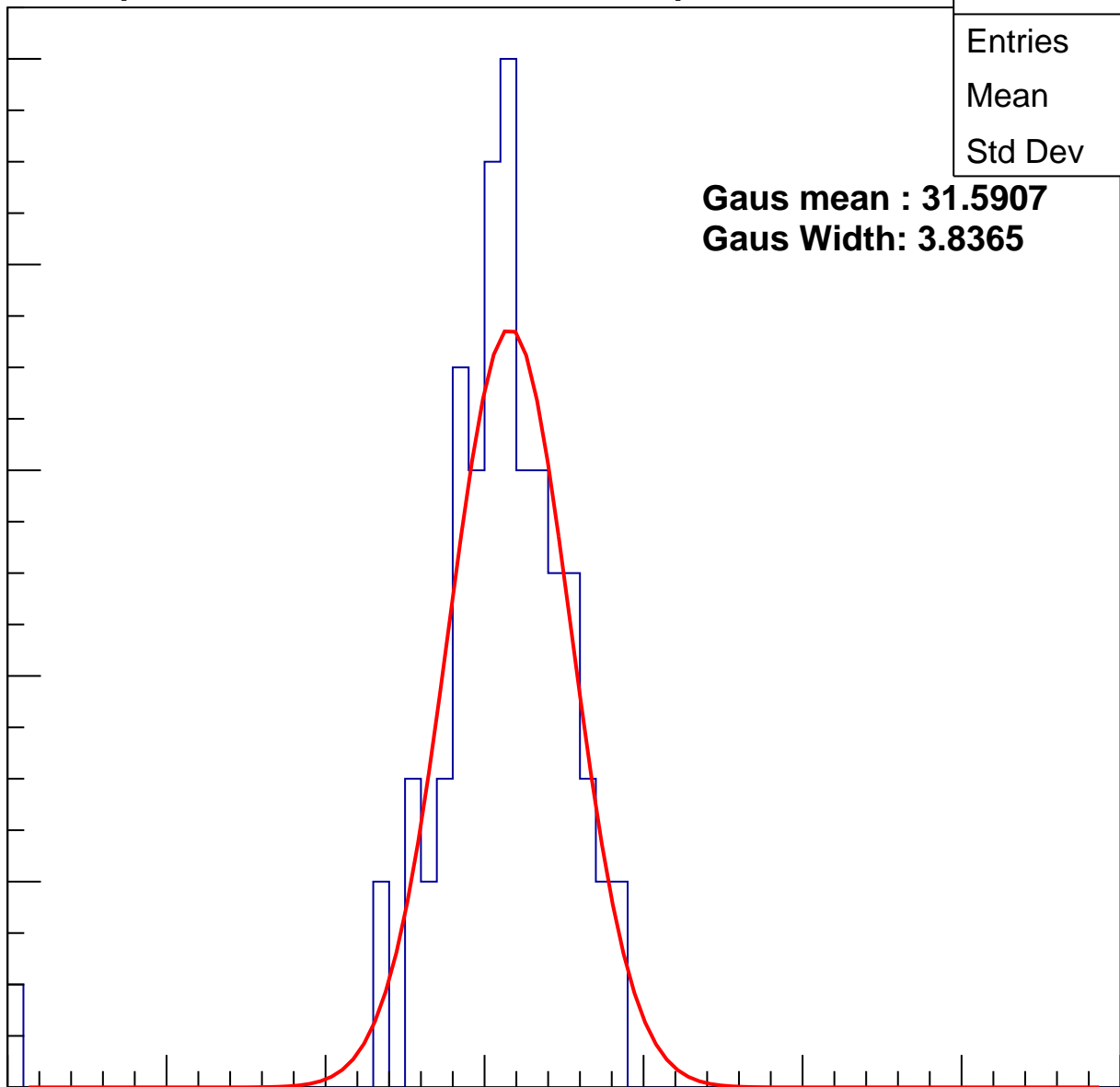
**Gaus Width: 3.8365**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U2-ch16, adc1

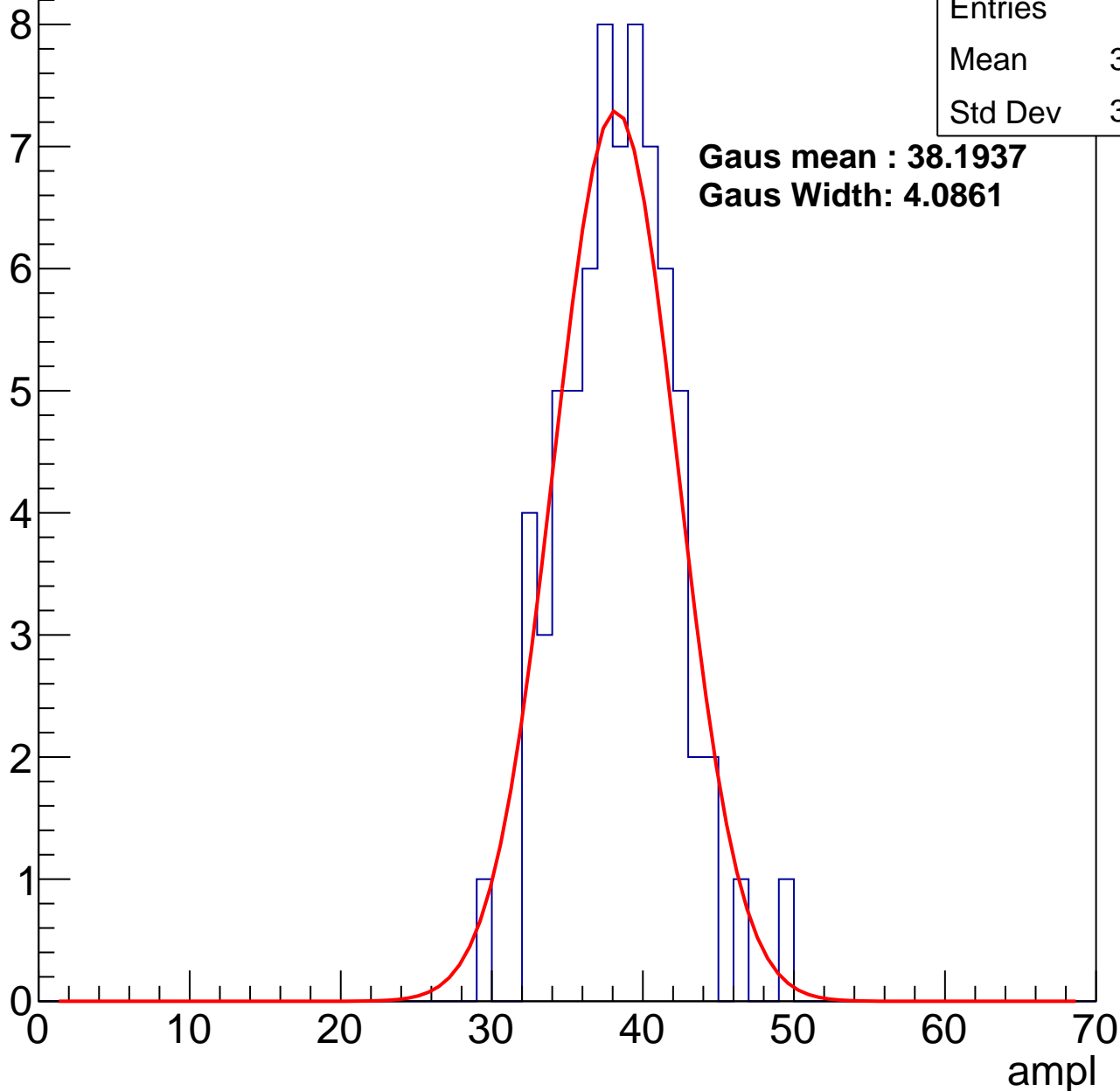
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 71    |
| Mean    | 37.97 |
| Std Dev | 3.627 |

**Gaus mean : 38.1937**

**Gaus Width: 4.0861**



# B0L001S, U2-ch16, adc2

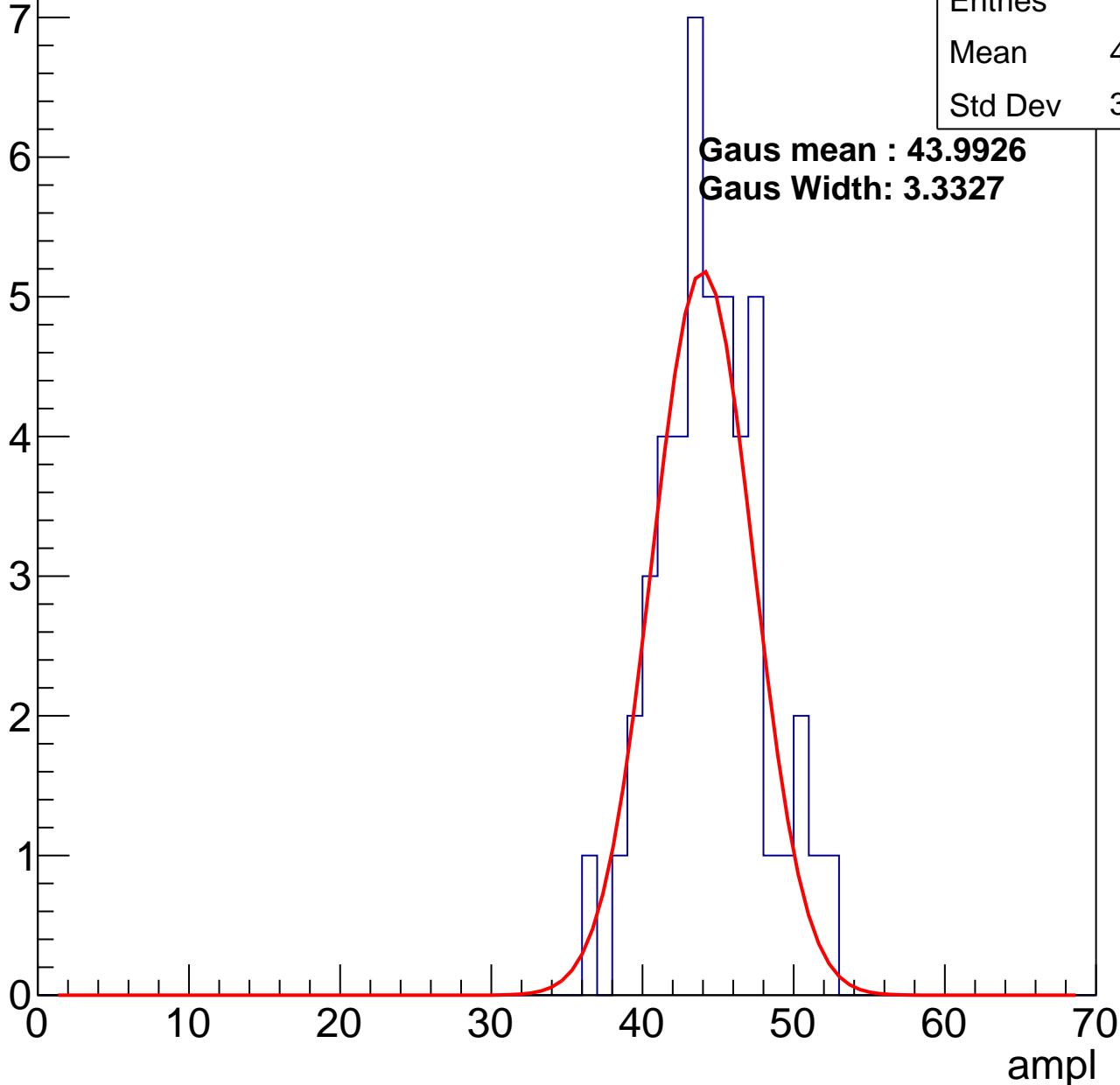
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 47    |
| Mean    | 44.02 |
| Std Dev | 3.418 |

**Gaus mean : 43.9926**

**Gaus Width: 3.3327**

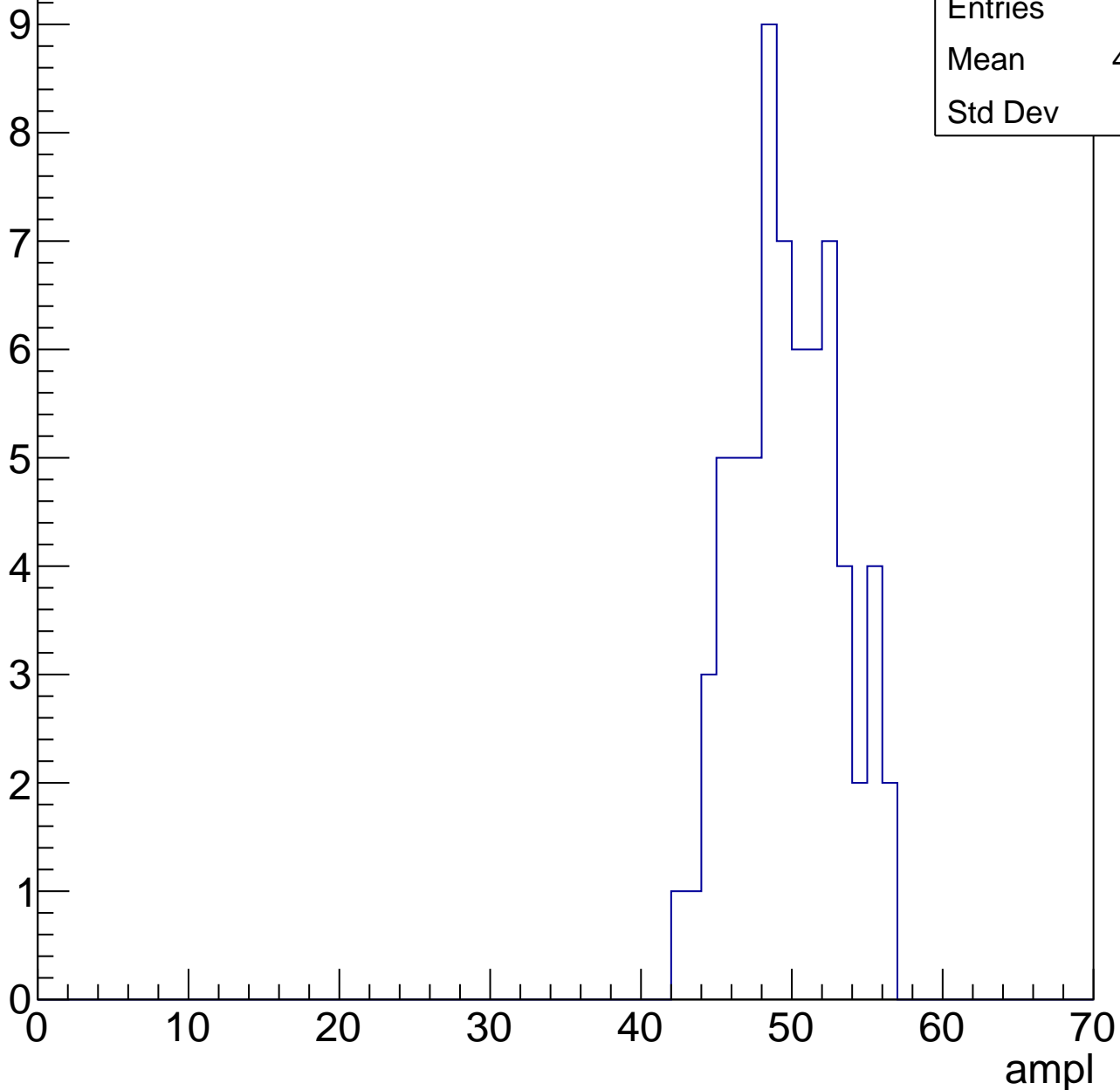


# B0L001S, U2-ch16, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

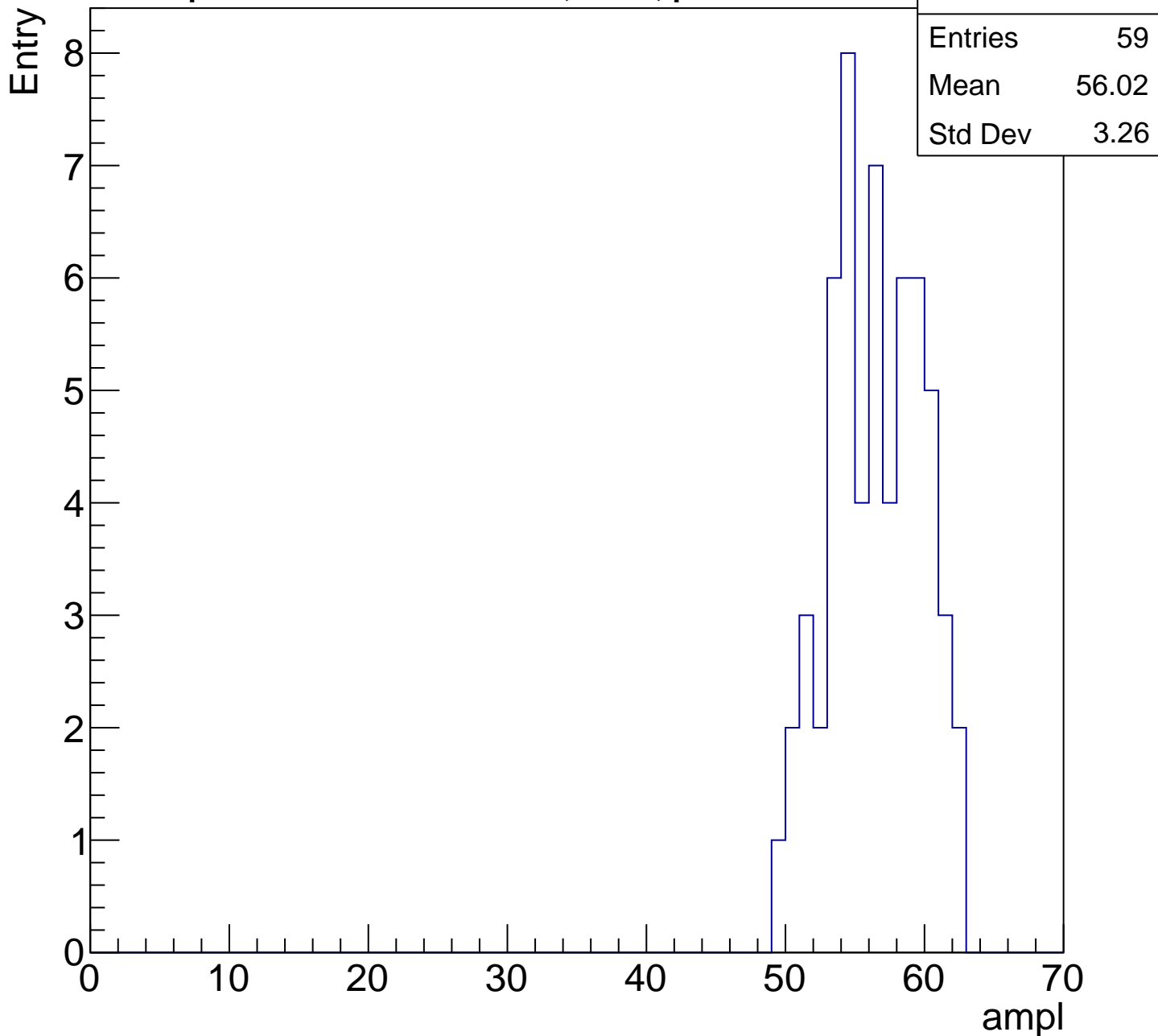
Entry

|         |       |
|---------|-------|
| Entries | 67    |
| Mean    | 49.31 |
| Std Dev | 3.36  |



# B0L001S, U2-ch16, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

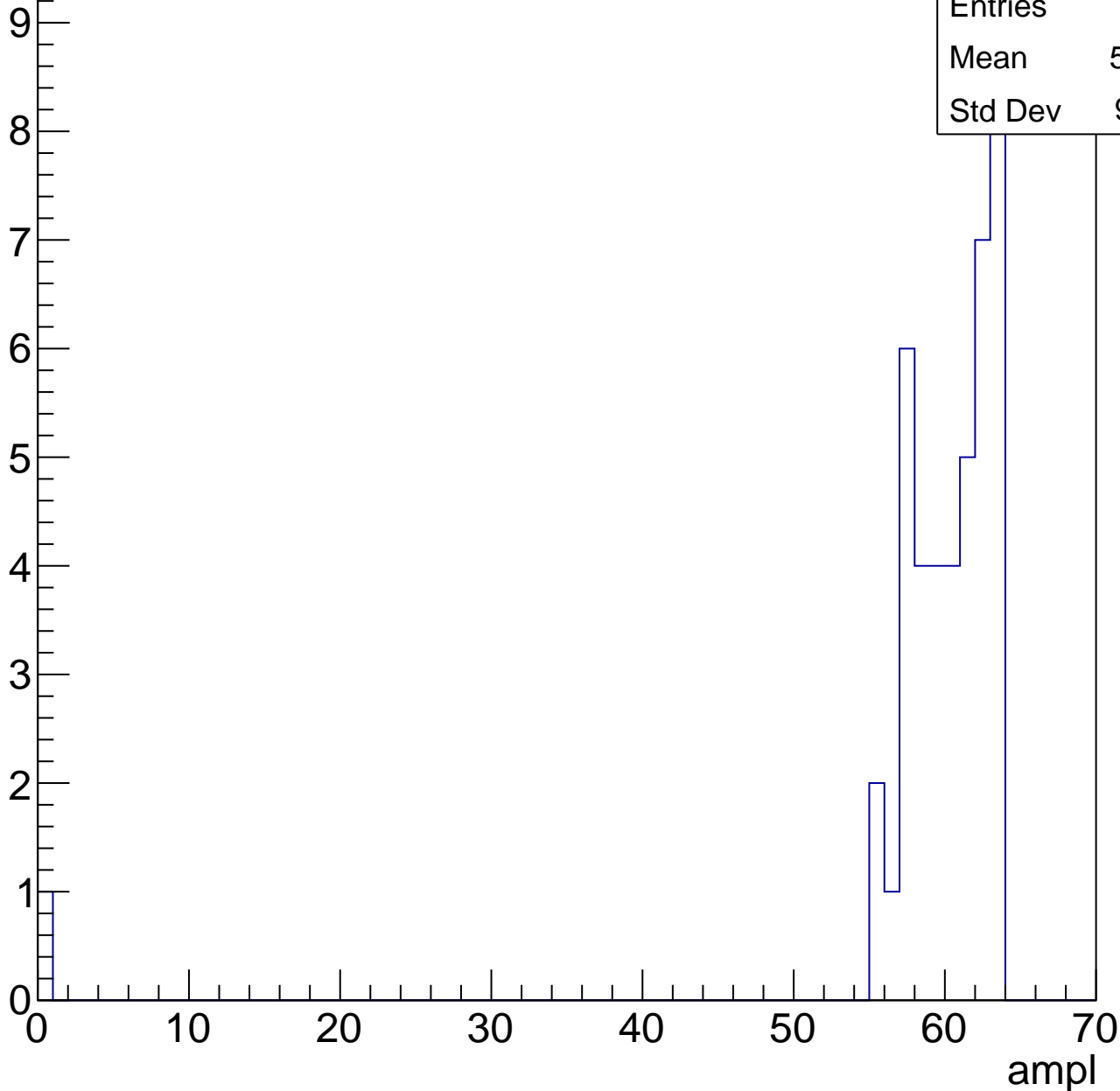


# B0L001S, U2-ch16, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

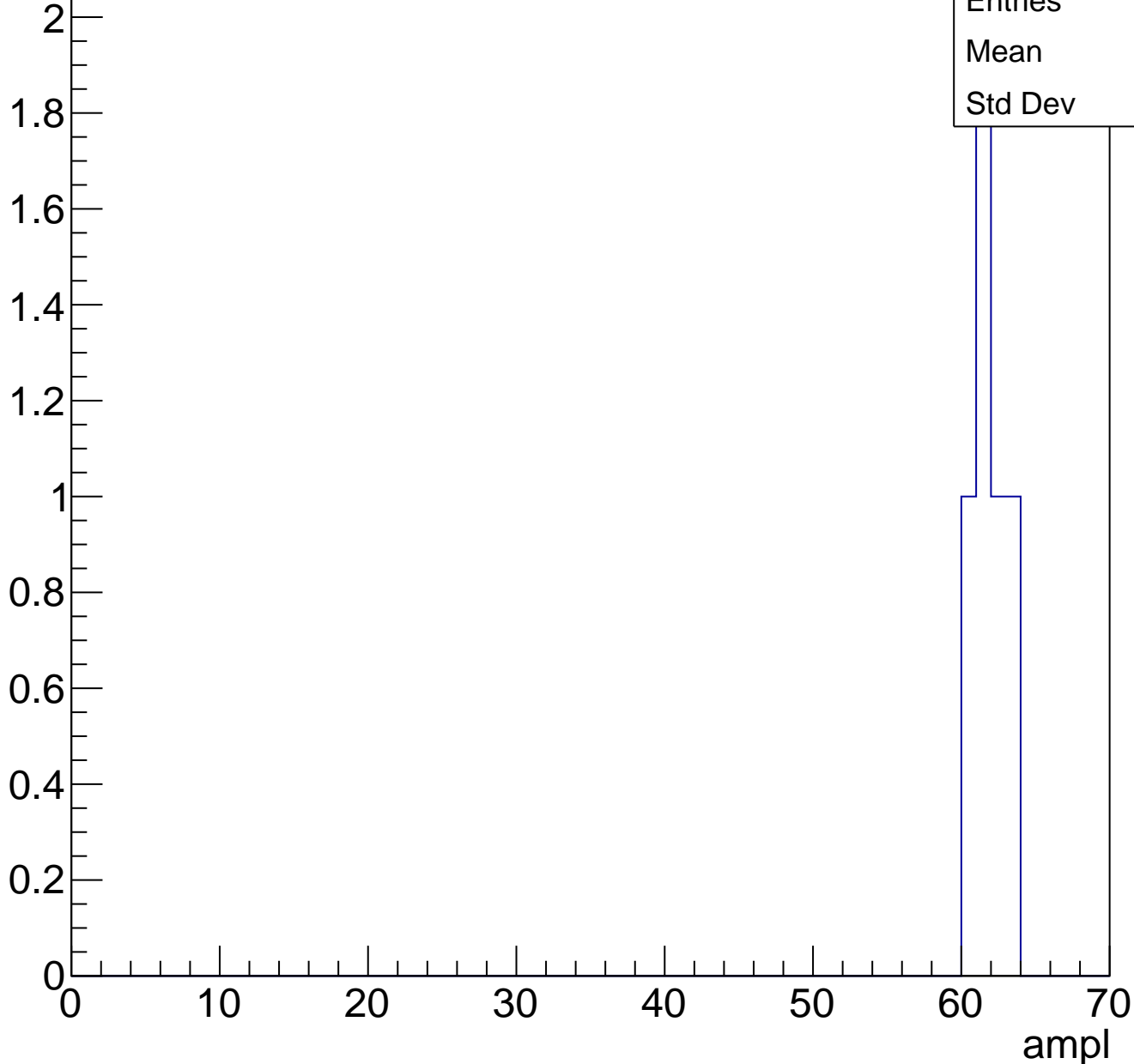
|         |       |
|---------|-------|
| Entries | 43    |
| Mean    | 58.65 |
| Std Dev | 9.371 |



# B0L001S, U2-ch16, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch16, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U2-ch17, adc0

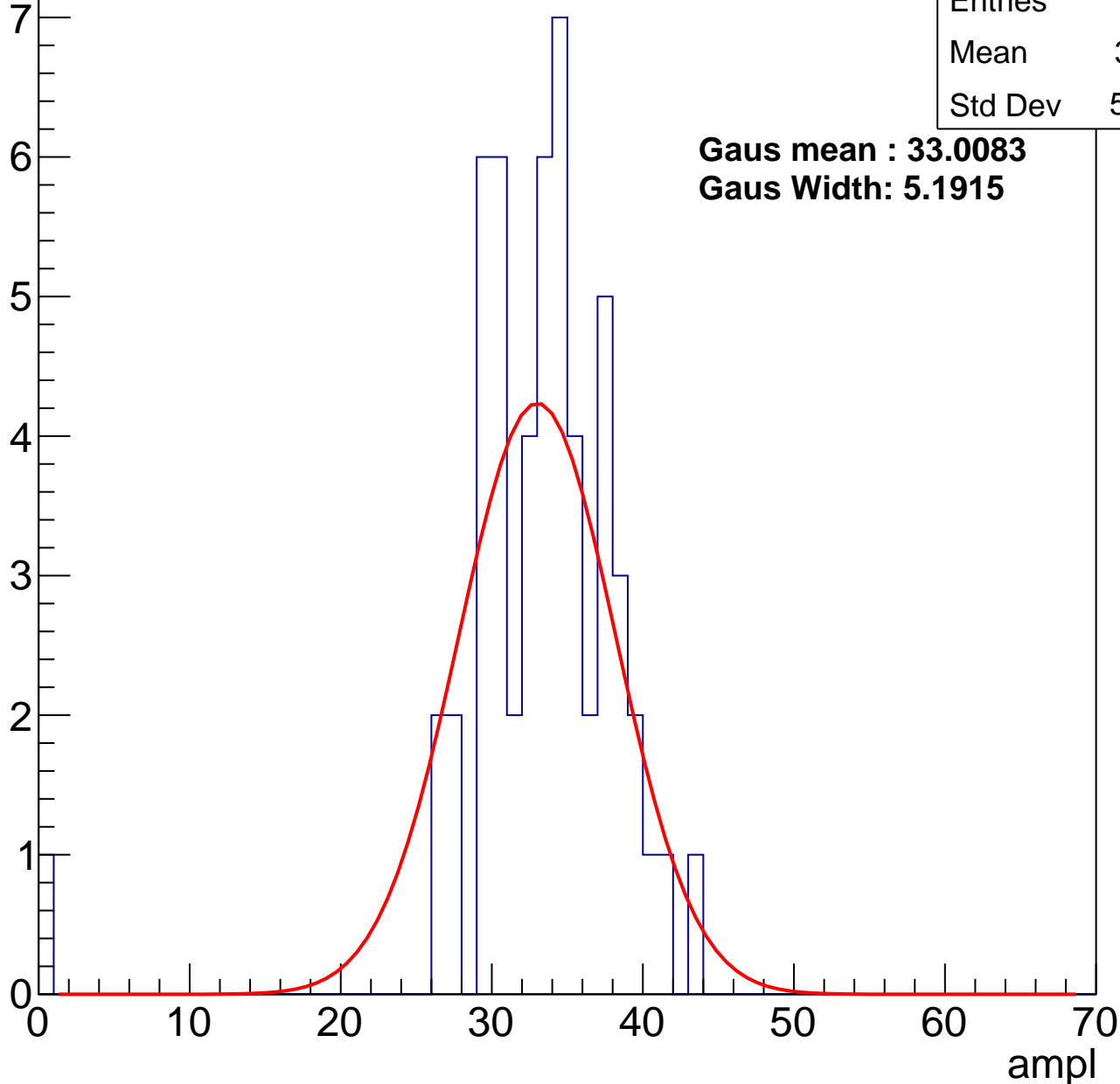
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 55    |
| Mean    | 32.71 |
| Std Dev | 5.873 |

**Gaus mean : 33.0083**

**Gaus Width: 5.1915**



# B0L001S, U2-ch17, adc1

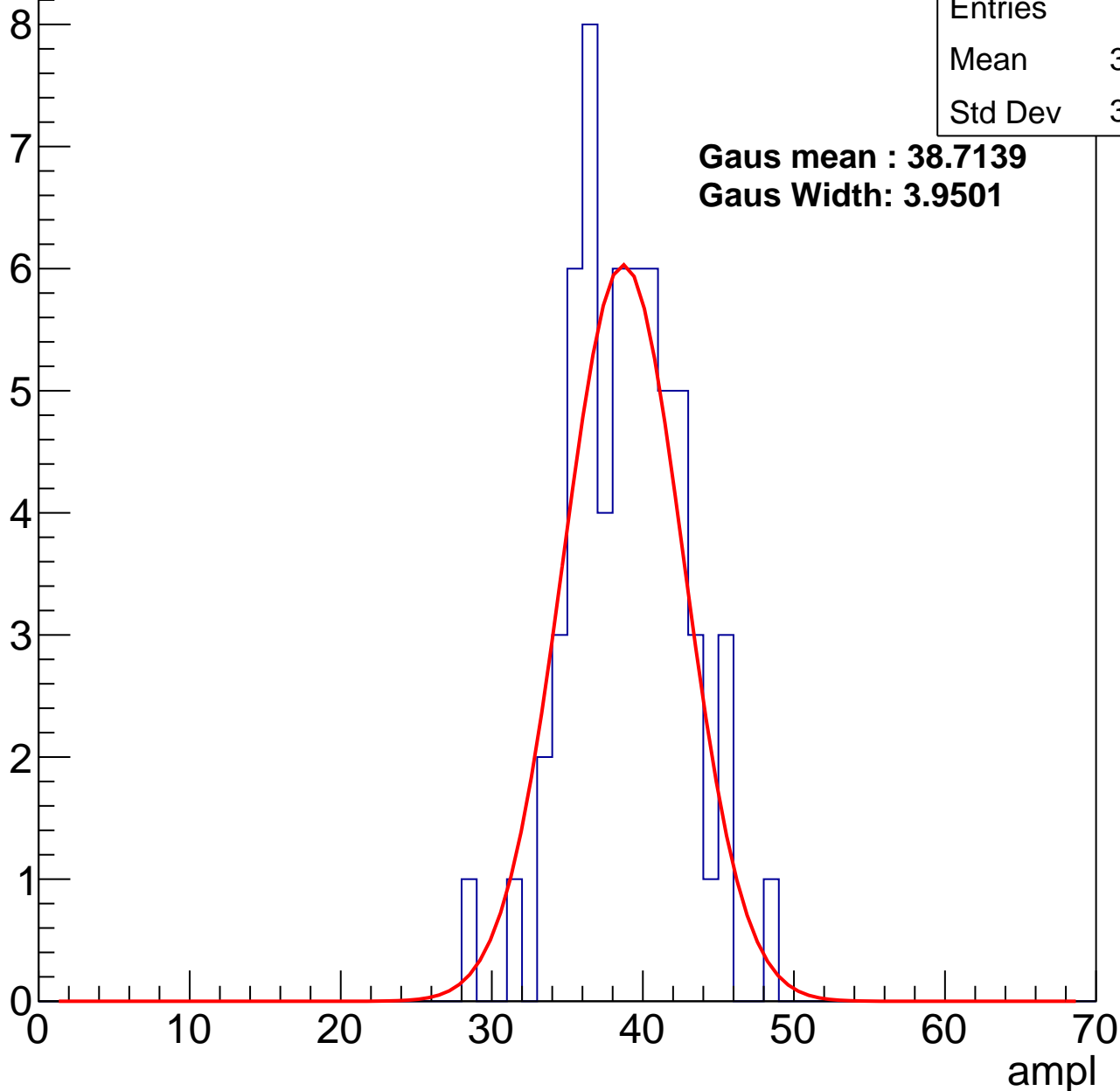
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 61    |
| Mean    | 38.46 |
| Std Dev | 3.705 |

**Gaus mean : 38.7139**

**Gaus Width: 3.9501**



# B0L001S, U2-ch17, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

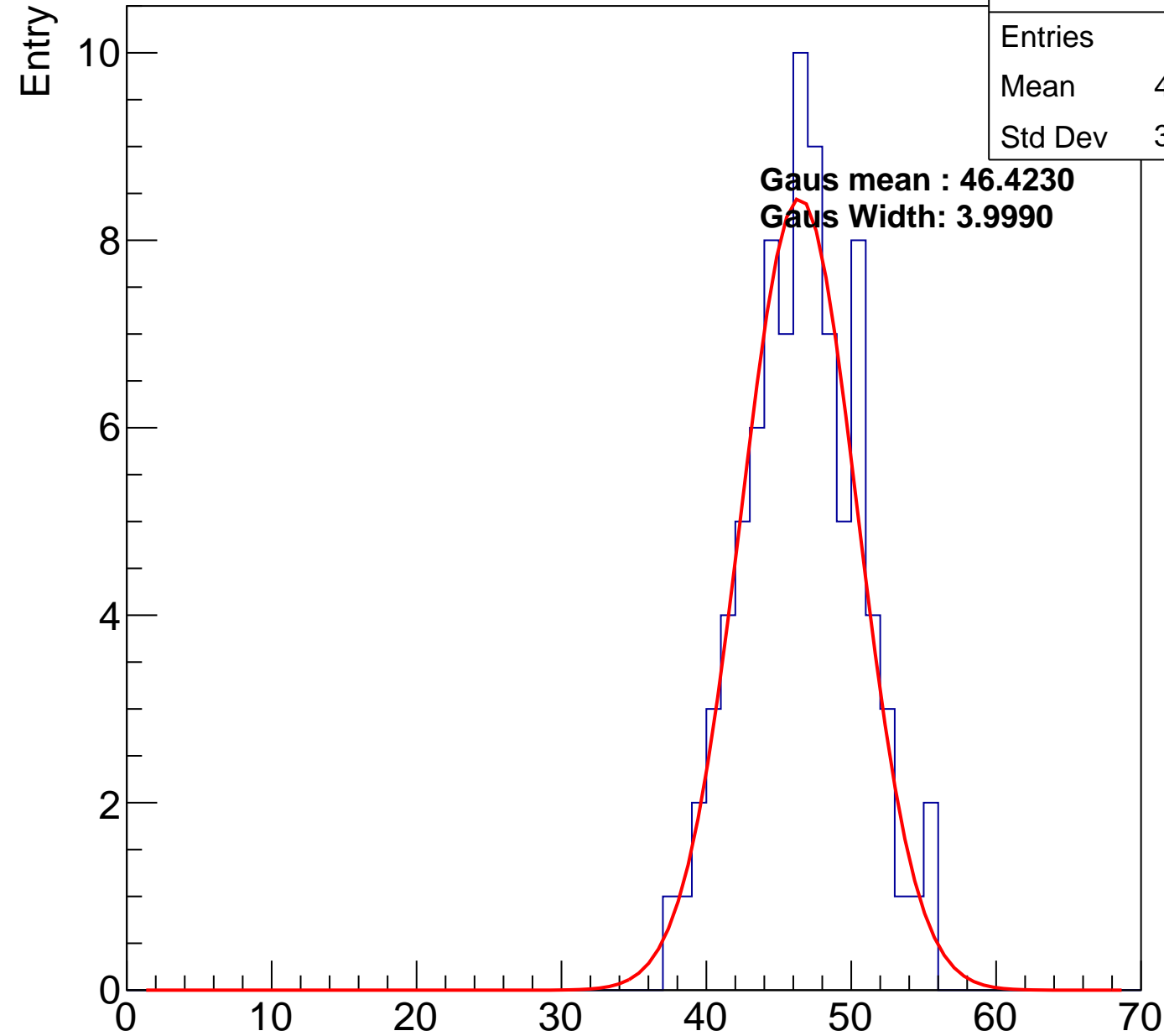
|         |       |
|---------|-------|
| Entries | 87    |
| Mean    | 46.13 |
| Std Dev | 3.889 |

**Gaus mean : 46.4230**

**Gaus Width: 3.9990**

10  
8  
6  
4  
2  
0

ampl

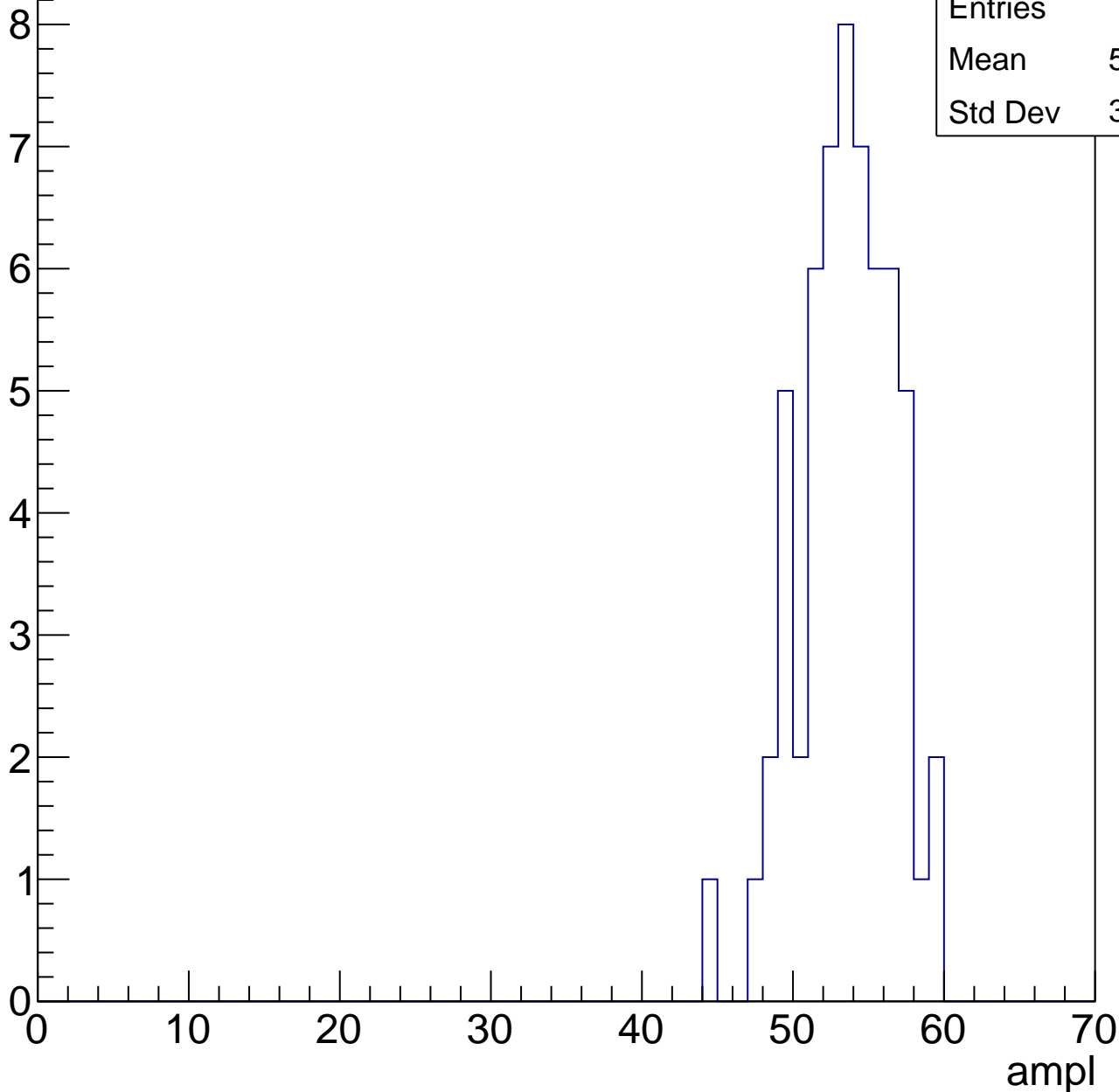


# B0L001S, U2-ch17, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 59    |
| Mean    | 53.07 |
| Std Dev | 3.075 |

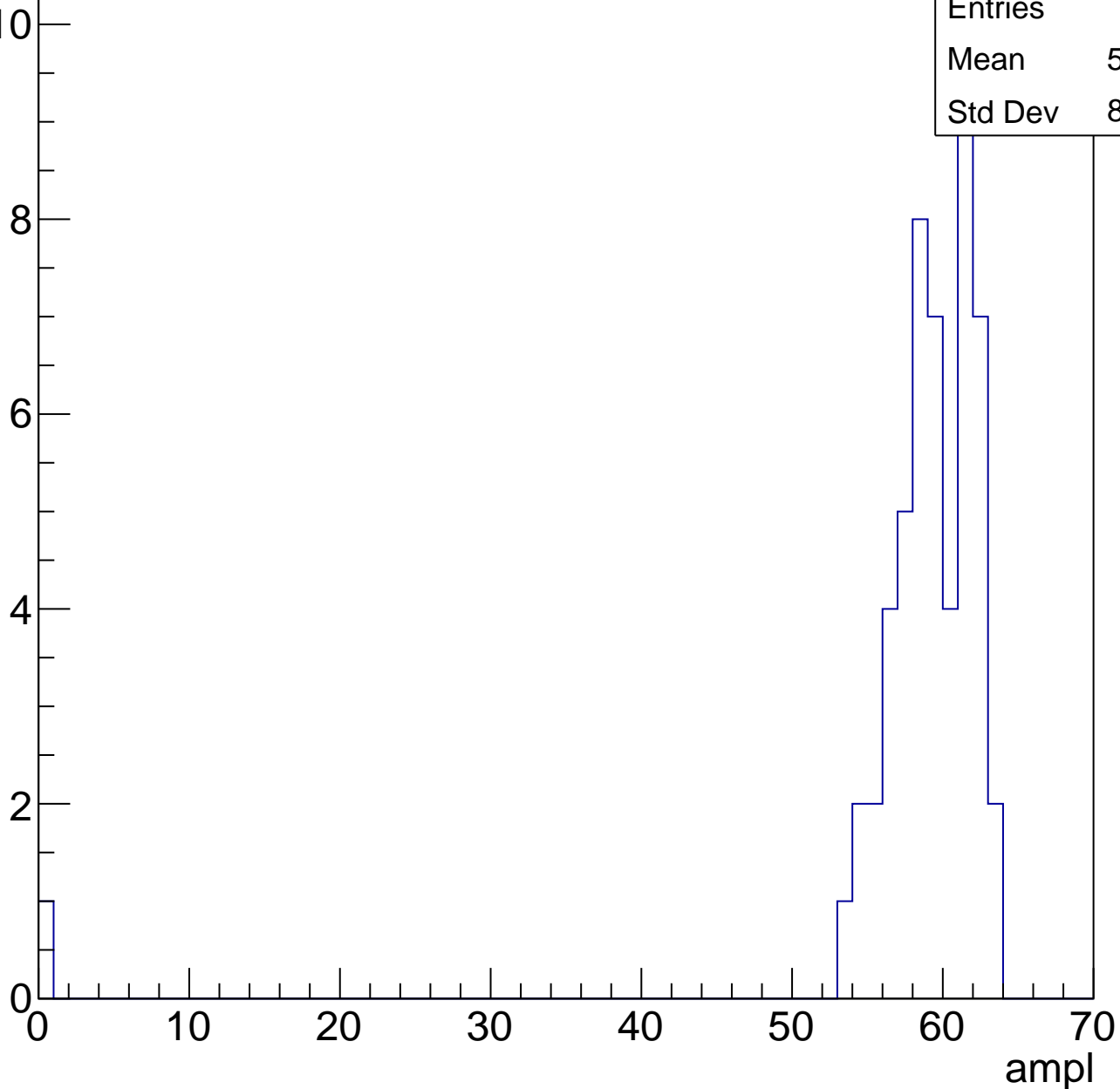


# B0L001S, U2-ch17, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 53    |
| Mean    | 57.87 |
| Std Dev | 8.394 |

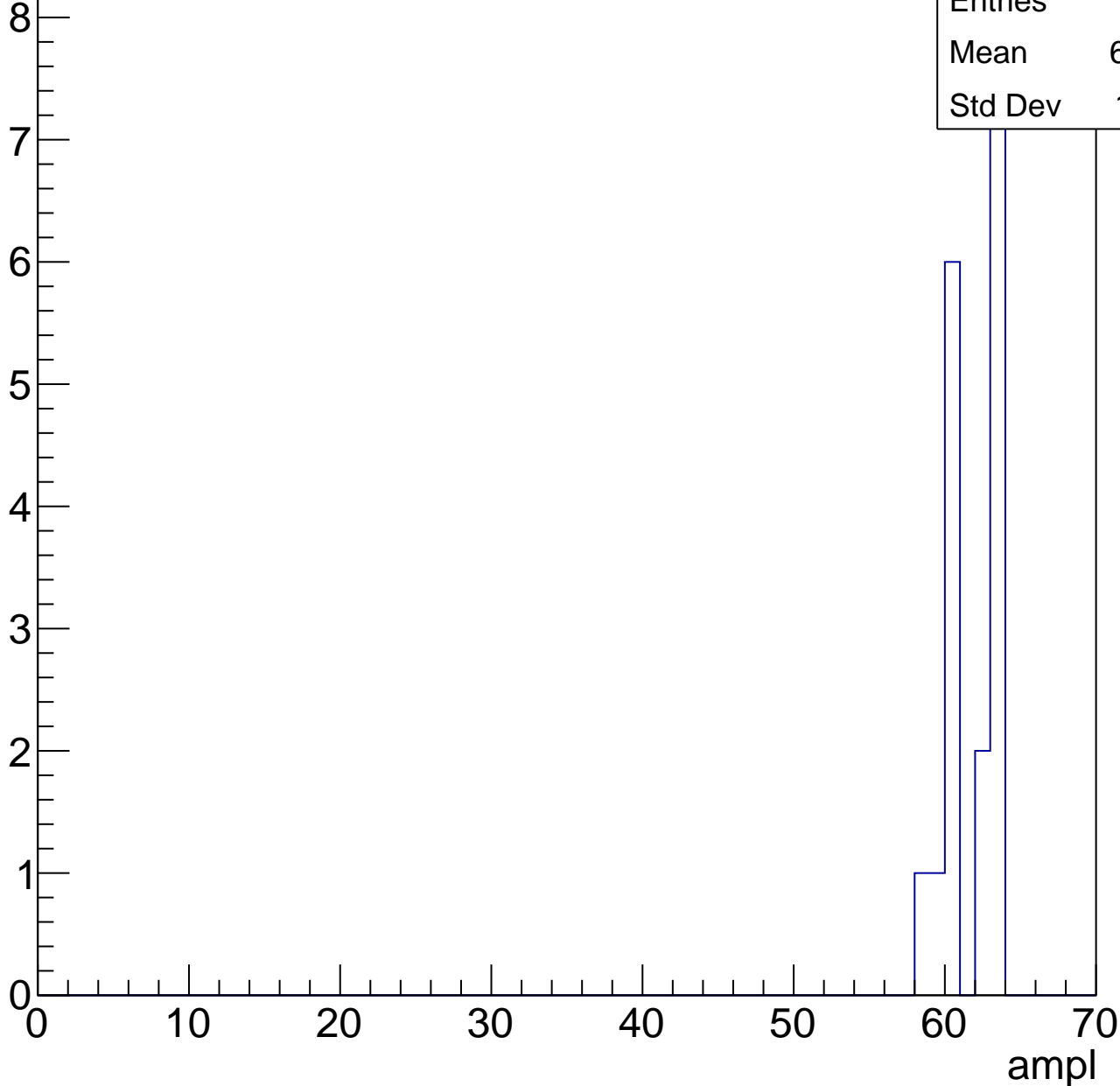


# B0L001S, U2-ch17, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 18    |
| Mean    | 61.39 |
| Std Dev | 1.671 |



# B0L001S, U2-ch17, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch17, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U2-ch18, adc0

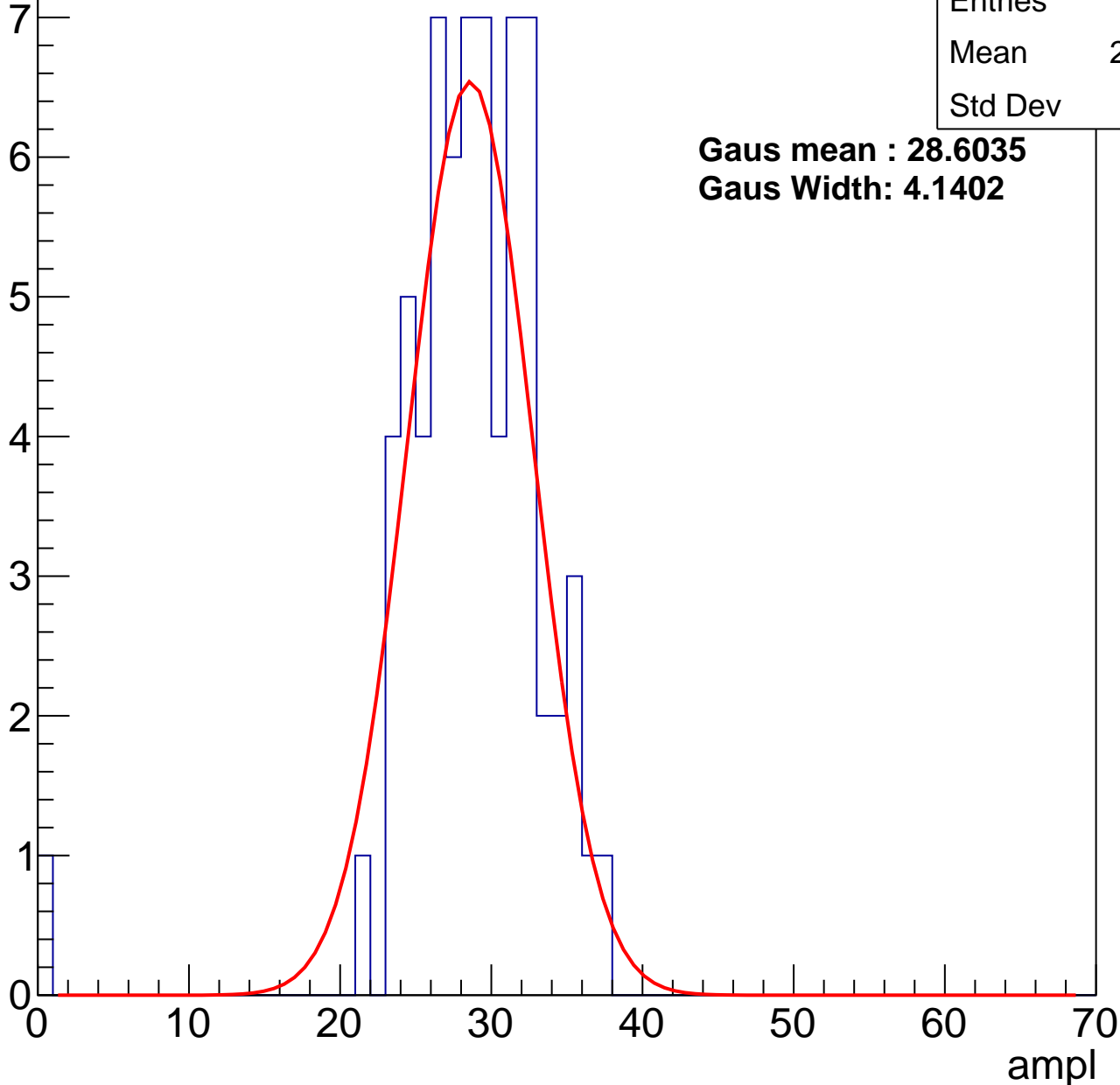
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 69    |
| Mean    | 28.25 |
| Std Dev | 4.95  |

**Gaus mean : 28.6035**

**Gaus Width: 4.1402**



# B0L001S, U2-ch18, adc1

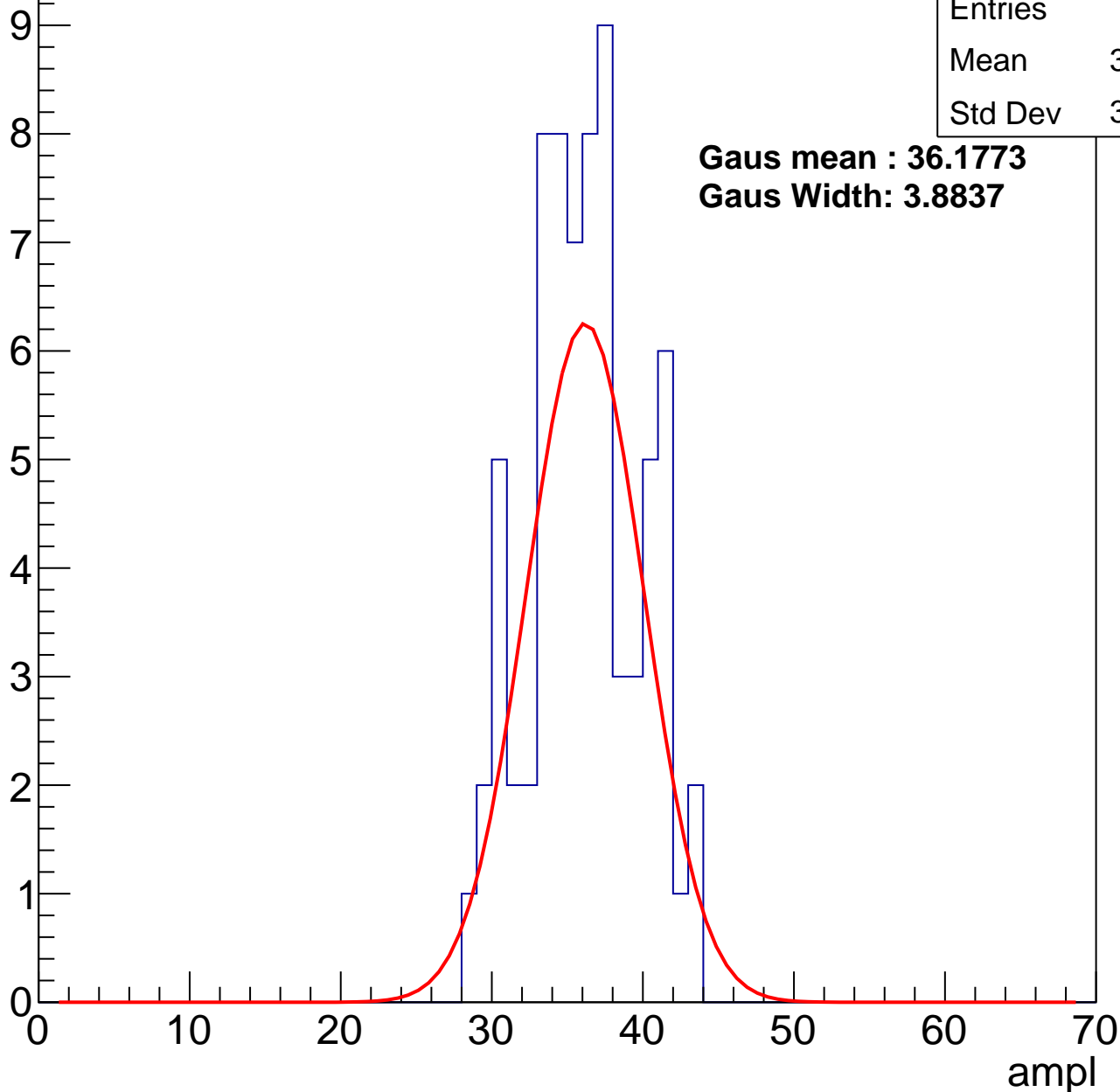
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 72    |
| Mean    | 35.68 |
| Std Dev | 3.613 |

**Gaus mean : 36.1773**

**Gaus Width: 3.8837**



# B0L001S, U2-ch18, adc2

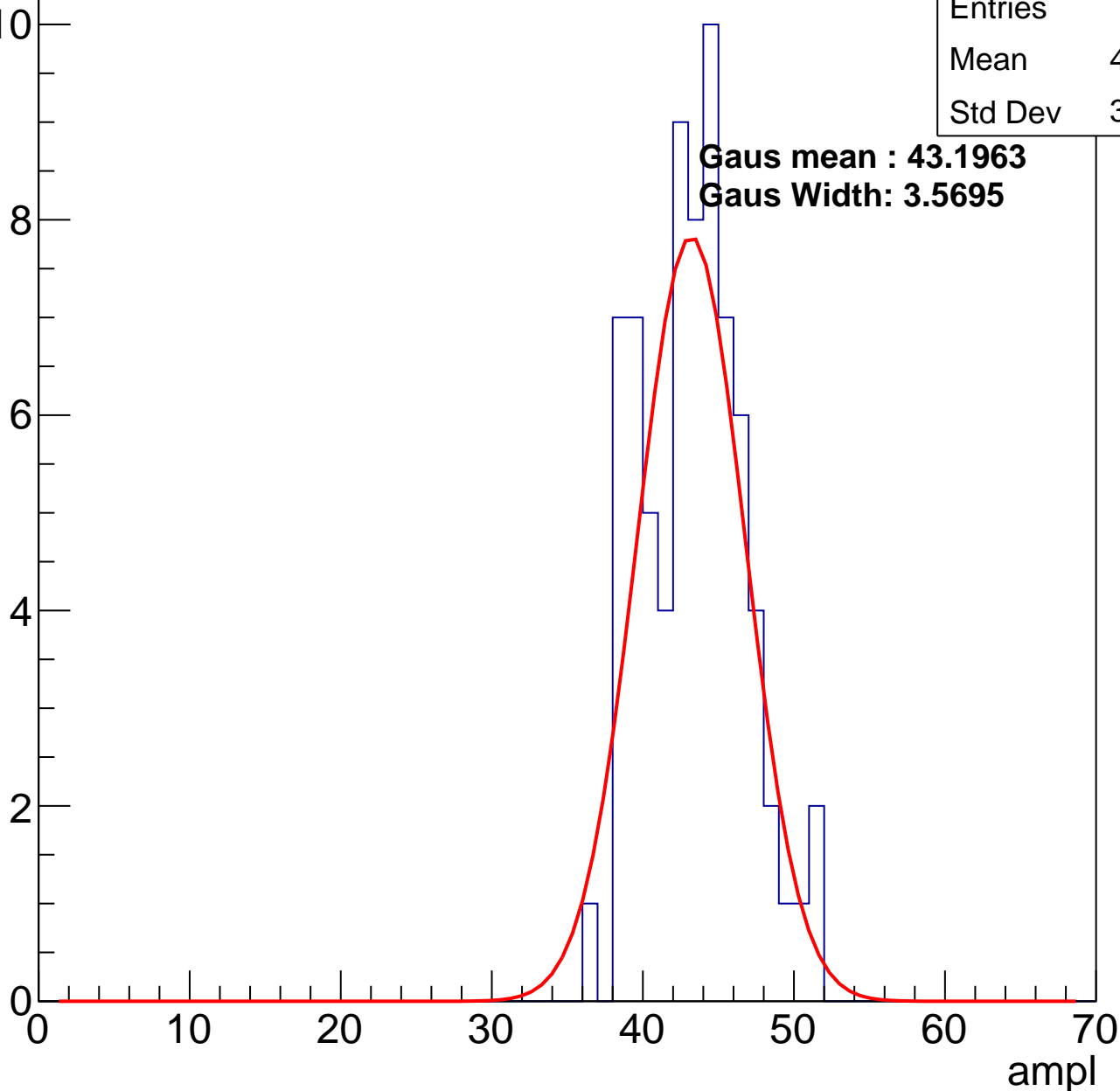
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 74    |
| Mean    | 42.93 |
| Std Dev | 3.338 |

**Gaus mean : 43.1963**

**Gaus Width: 3.5695**

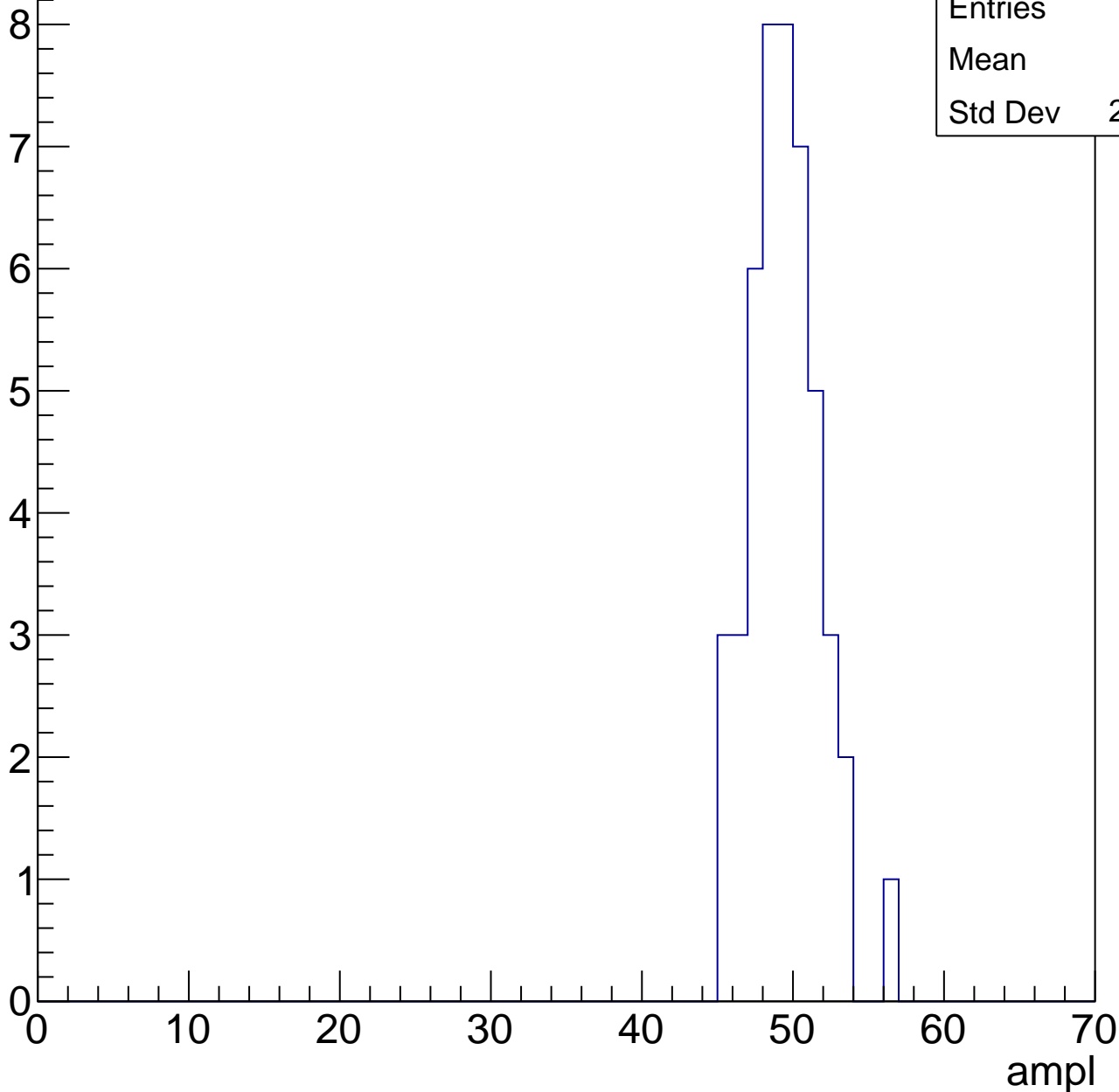


# B0L001S, U2-ch18, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 46    |
| Mean    | 49    |
| Std Dev | 2.294 |

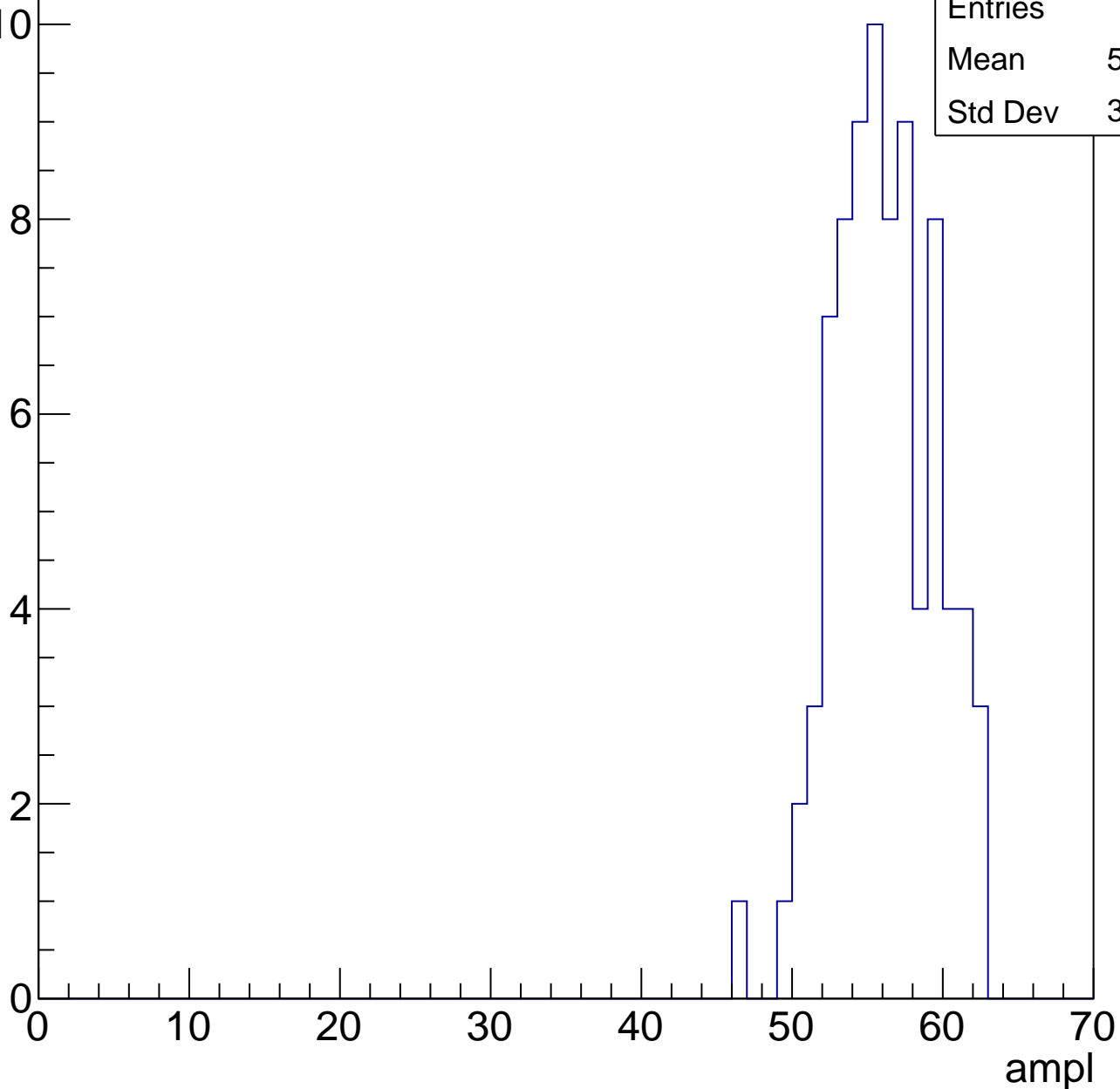


# B0L001S, U2-ch18, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 81    |
| Mean    | 55.64 |
| Std Dev | 3.305 |

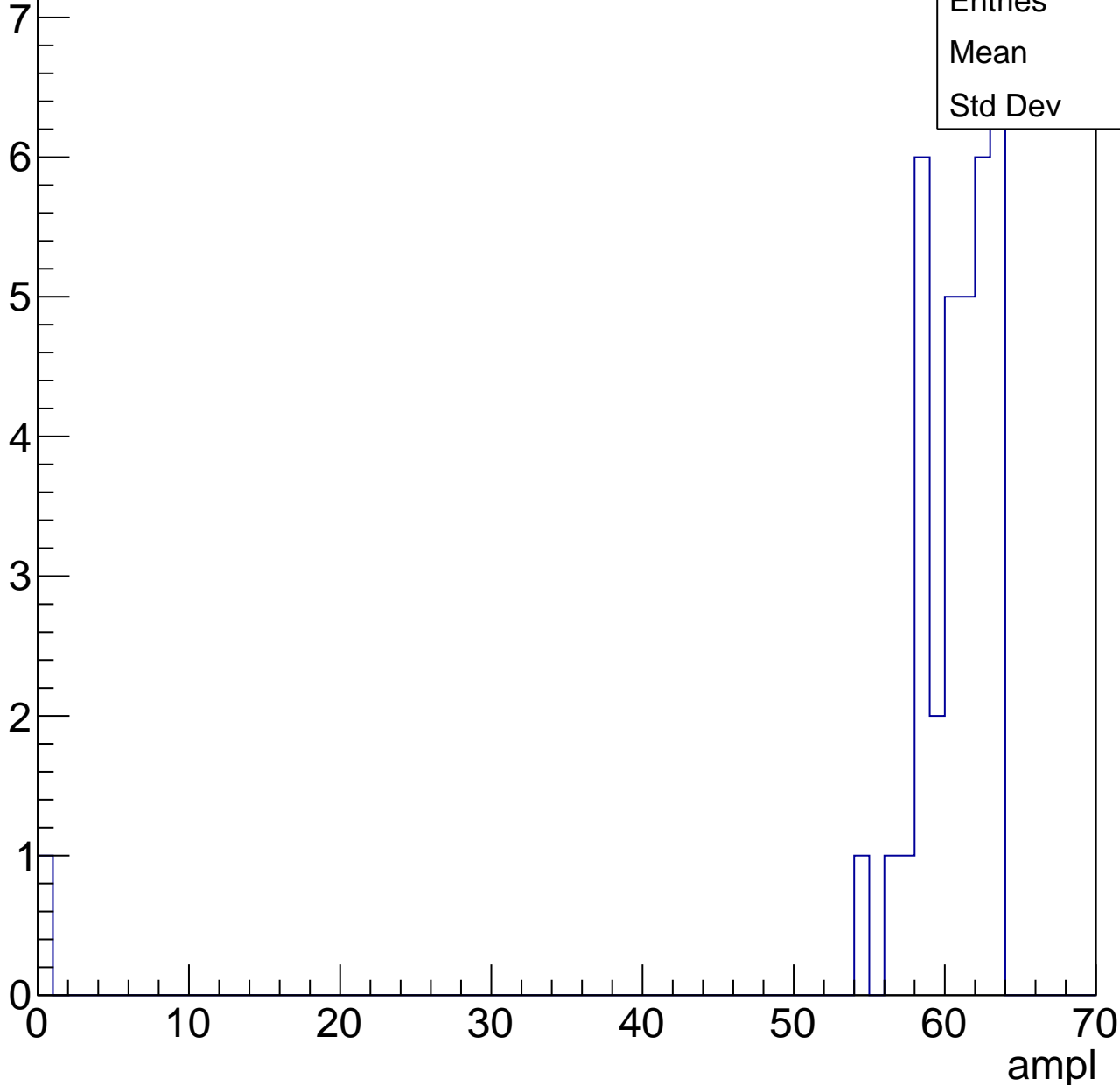


# B0L001S, U2-ch18, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |      |
|---------|------|
| Entries | 35   |
| Mean    | 58.6 |
| Std Dev | 10.3 |



# B0L001S, U2-ch18, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch18, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 1 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch19, adc0

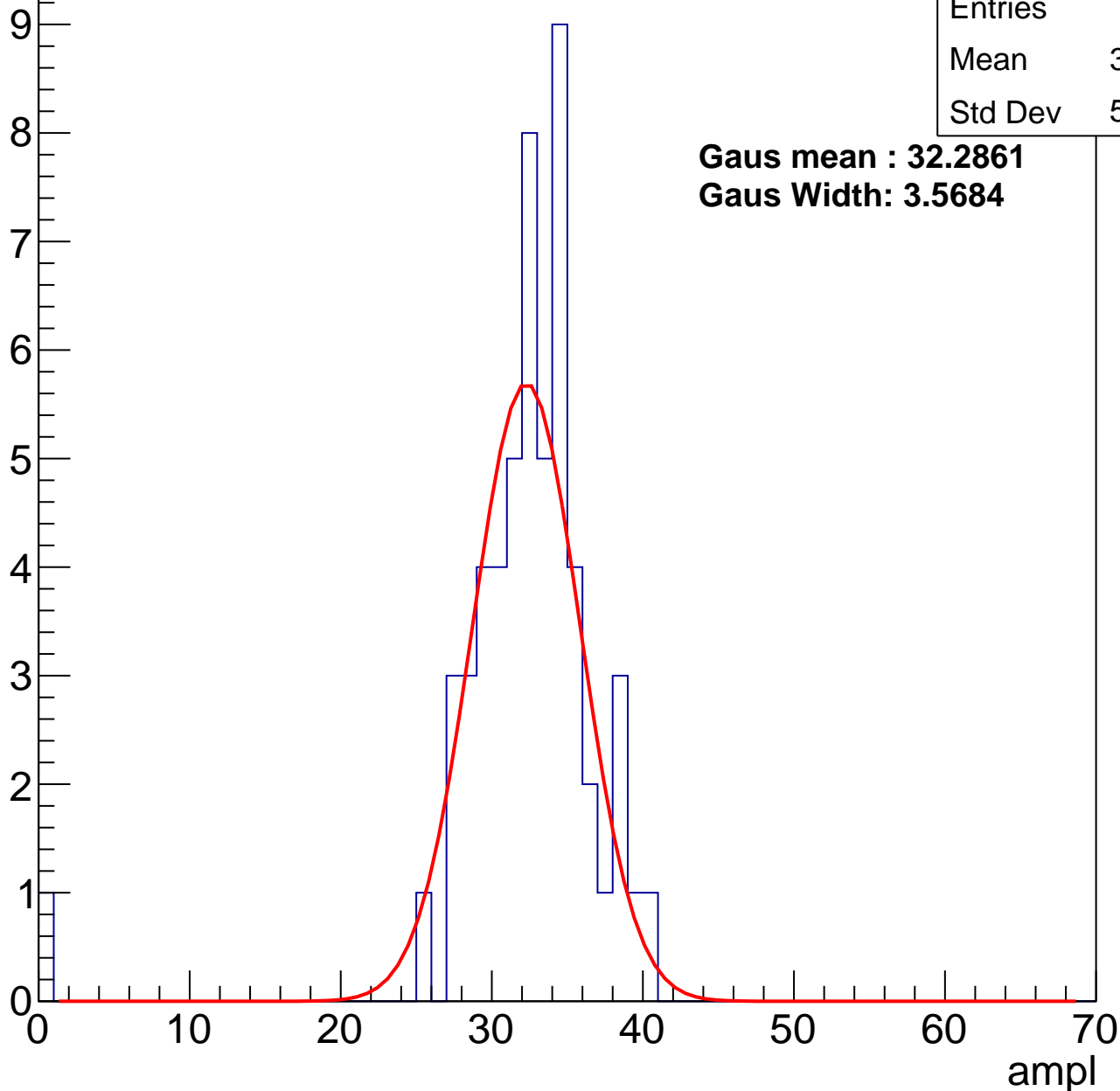
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 55    |
| Mean    | 31.82 |
| Std Dev | 5.404 |

**Gaus mean : 32.2861**

**Gaus Width: 3.5684**



# B0L001S, U2-ch19, adc1

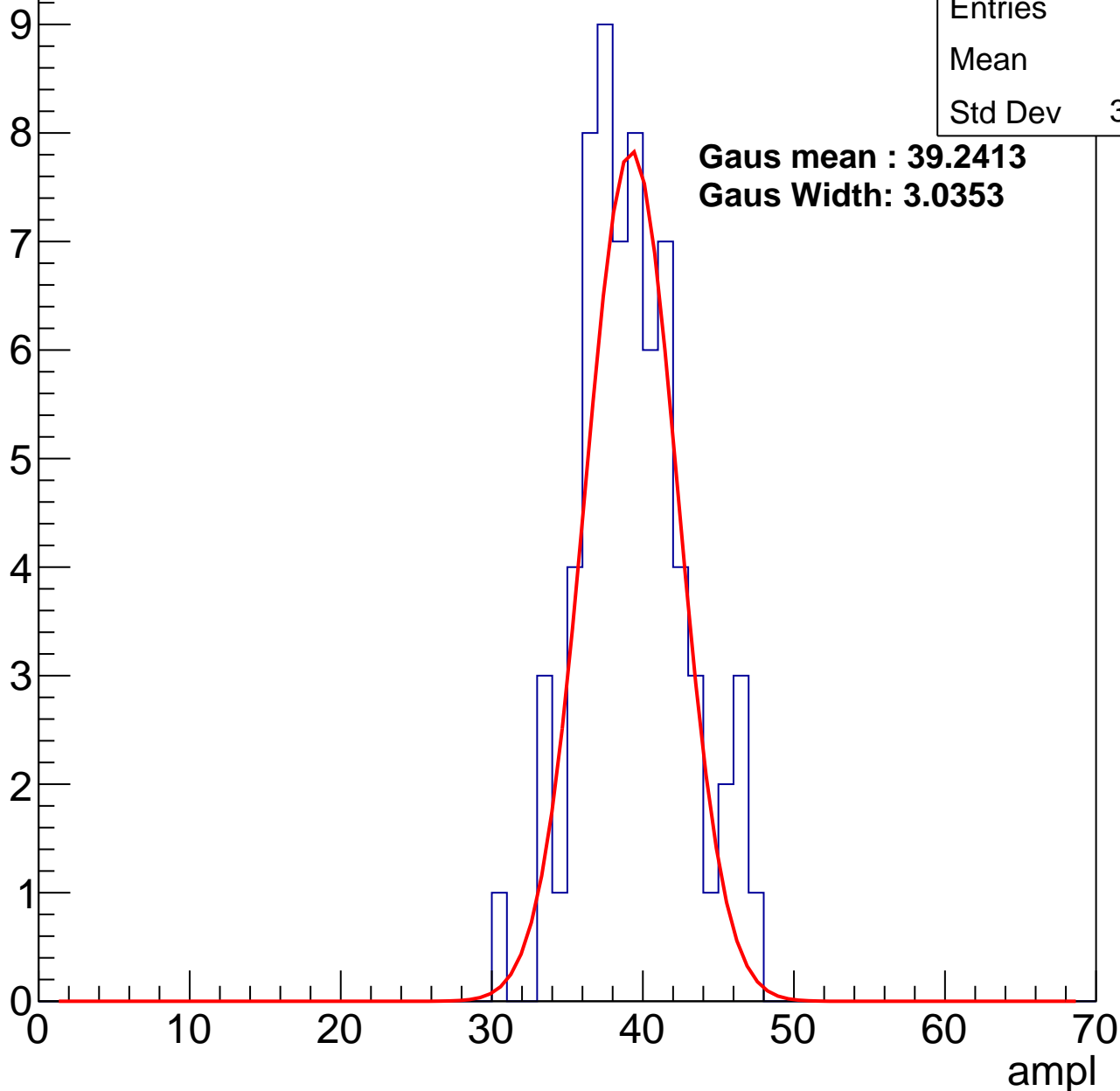
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 68    |
| Mean    | 38.9  |
| Std Dev | 3.469 |

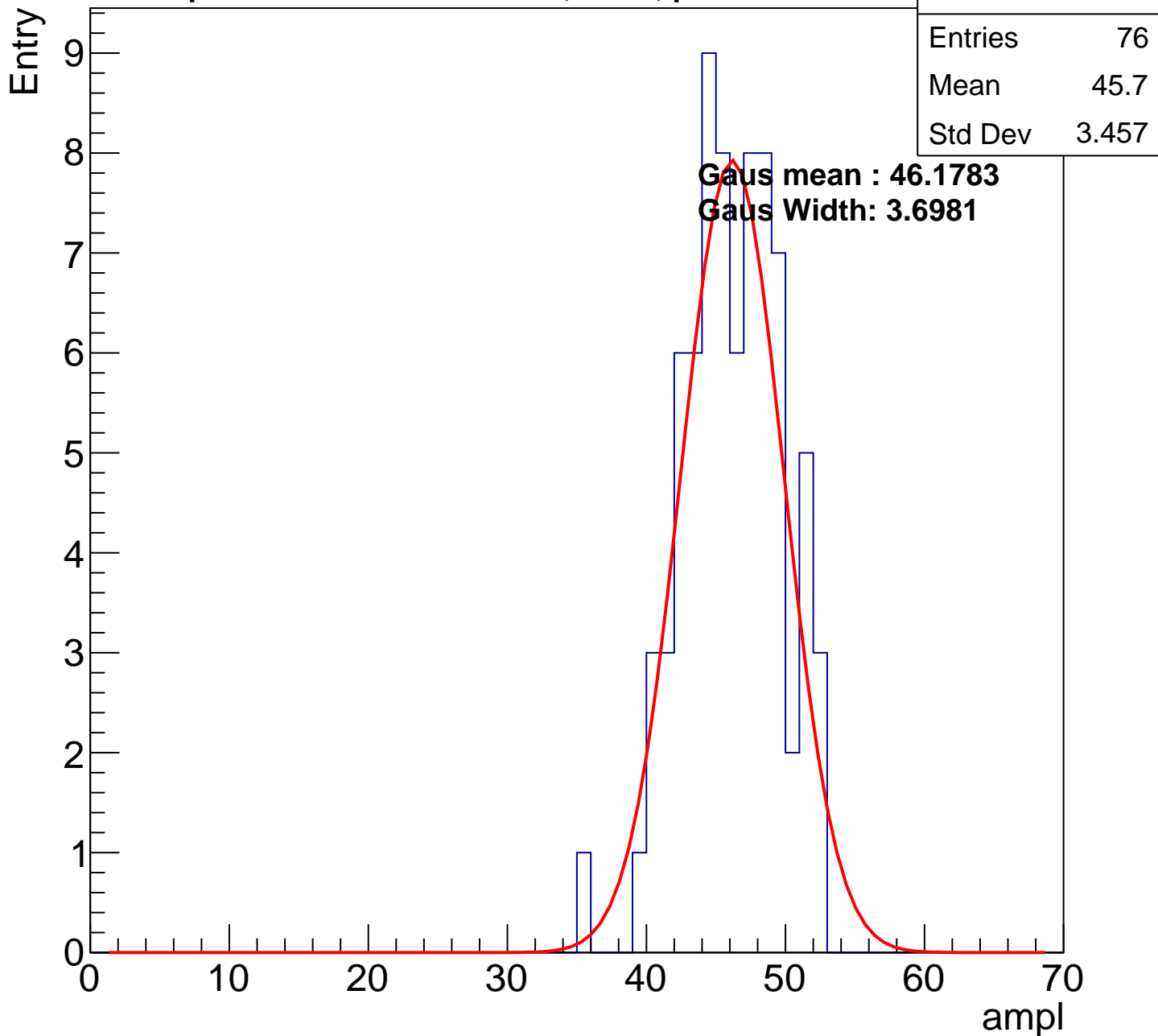
**Gaus mean : 39.2413**

**Gaus Width: 3.0353**



# B0L001S, U2-ch19, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U2-ch19, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

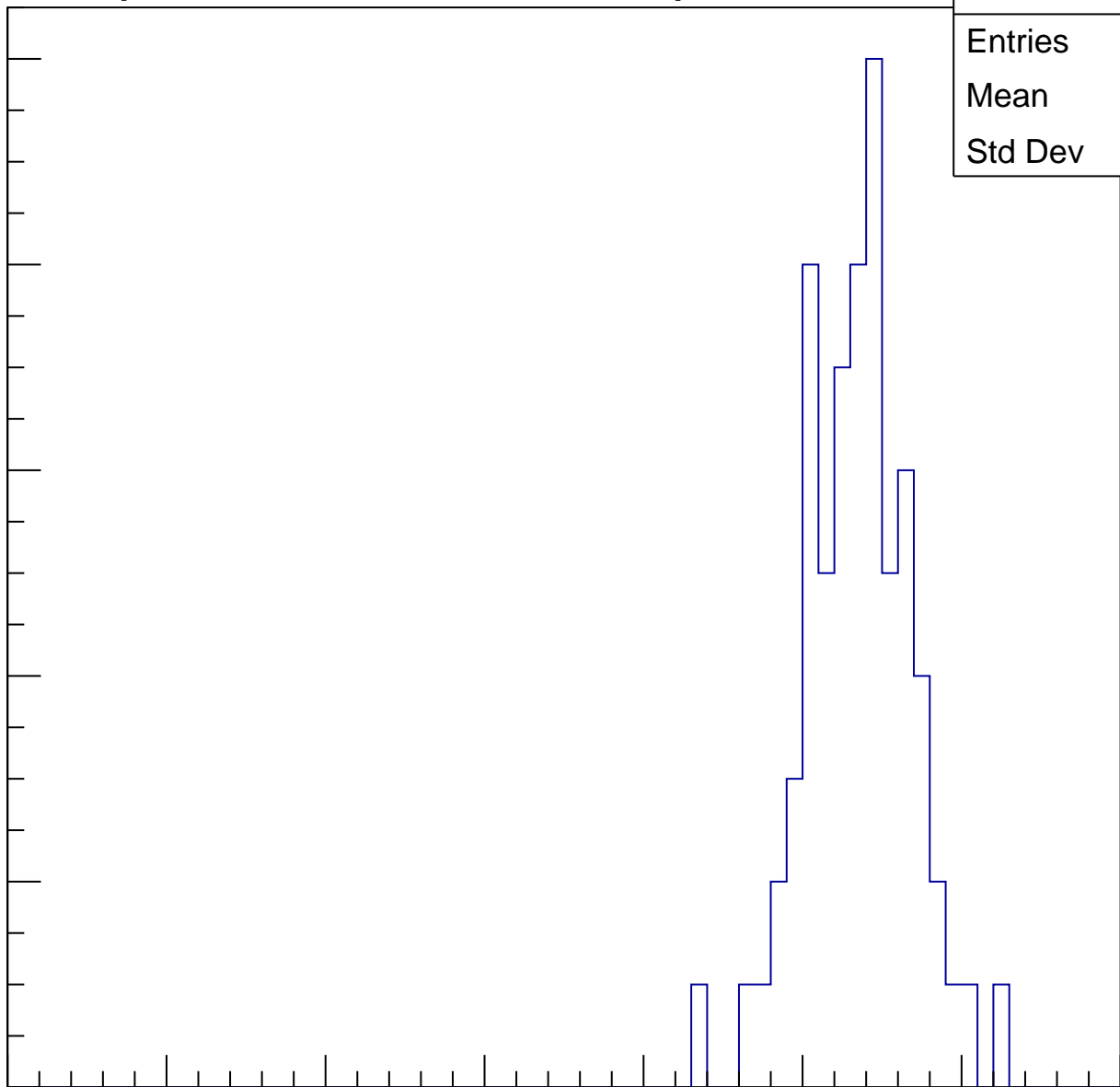
|         |       |
|---------|-------|
| Entries | 66    |
| Mean    | 53    |
| Std Dev | 3.362 |

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

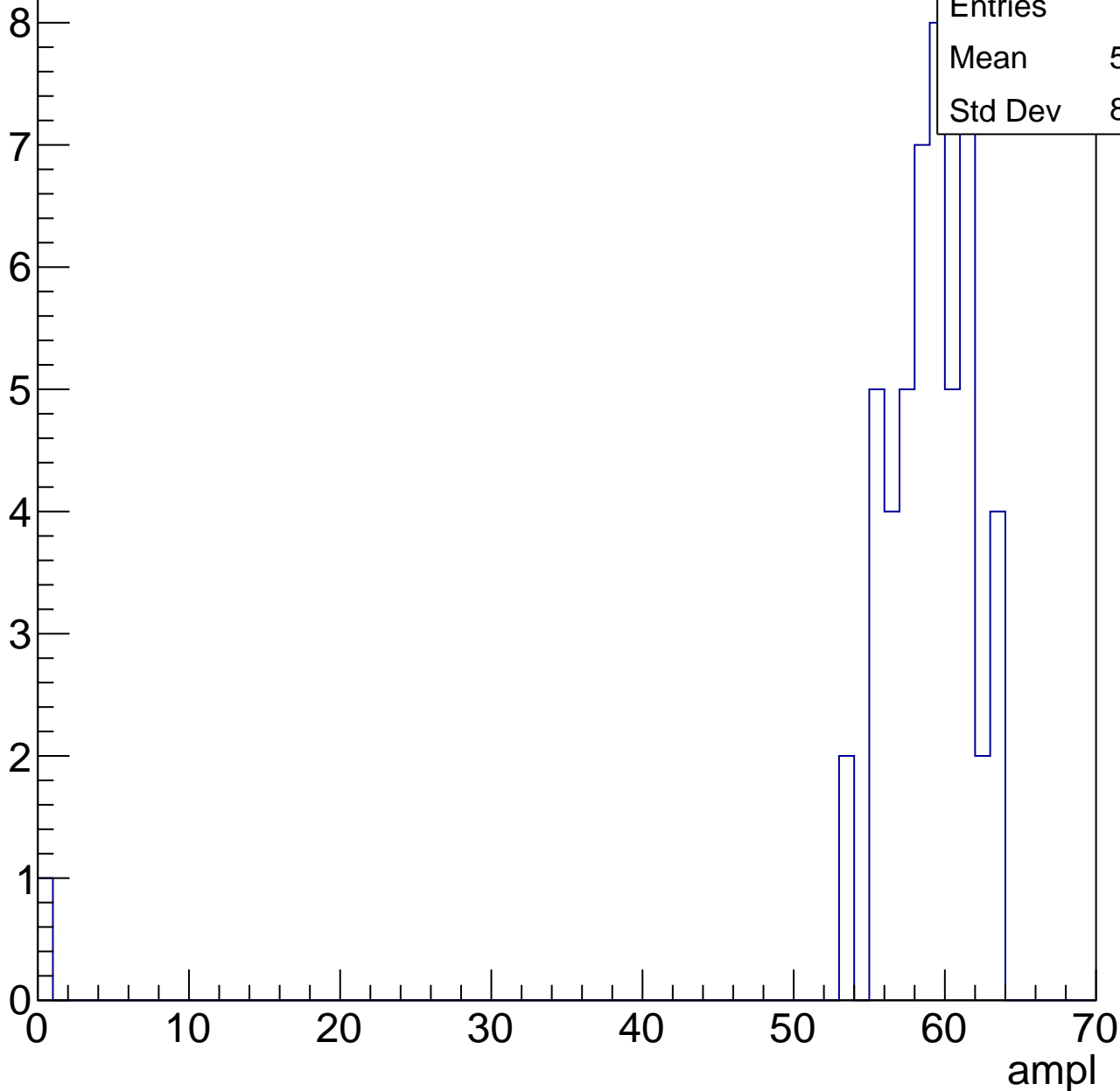


# B0L001S, U2-ch19, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 51    |
| Mean    | 57.49 |
| Std Dev | 8.516 |

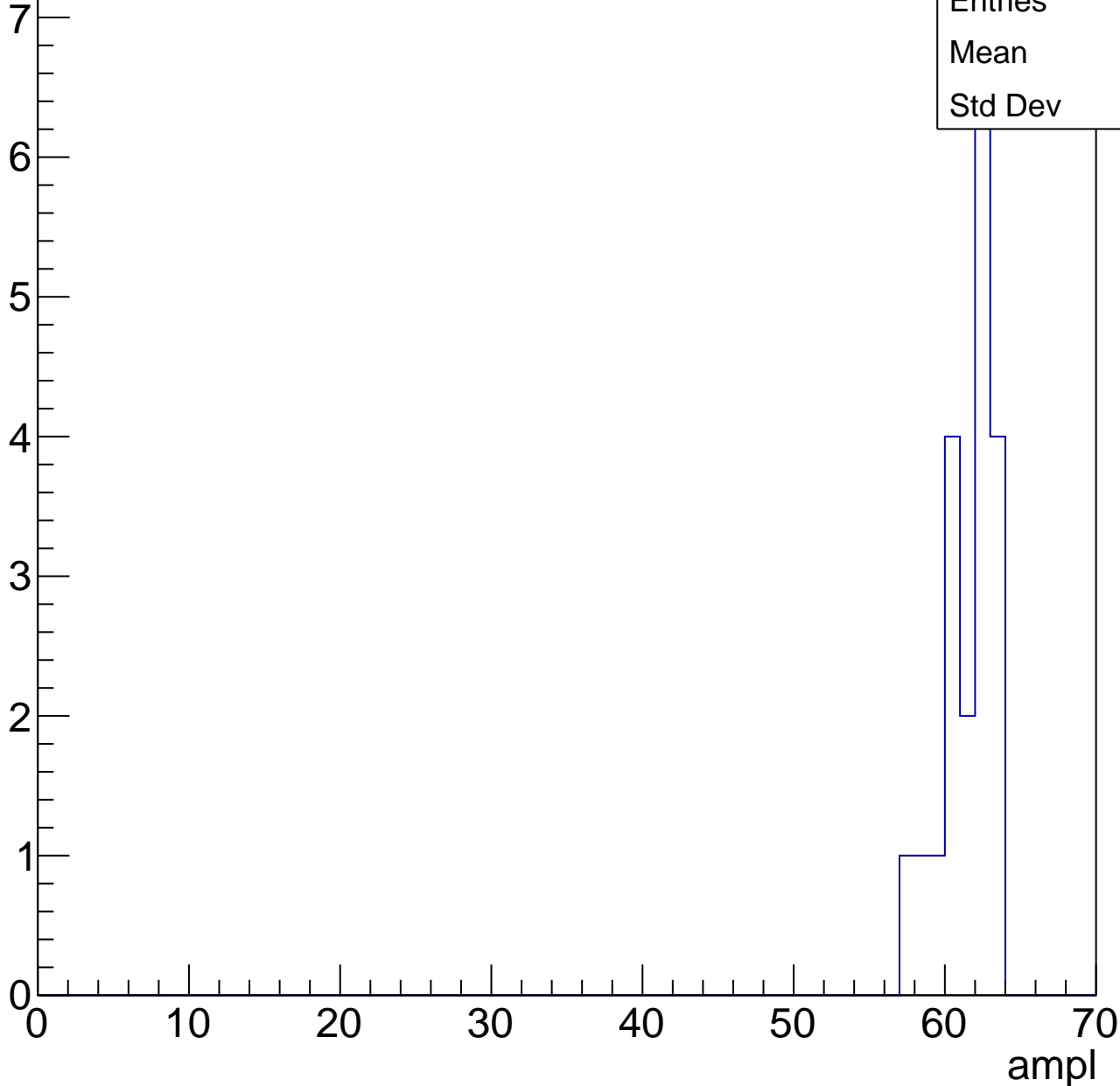


# B0L001S, U2-ch19, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |      |
|---------|------|
| Entries | 20   |
| Mean    | 61.1 |
| Std Dev | 1.67 |



# B0L001S, U2-ch19, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

|         |    |
|---------|----|
| Entries | 2  |
| Mean    | 63 |
| Std Dev | 0  |

ampl



# B0L001S, U2-ch19, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 0 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch20, adc0

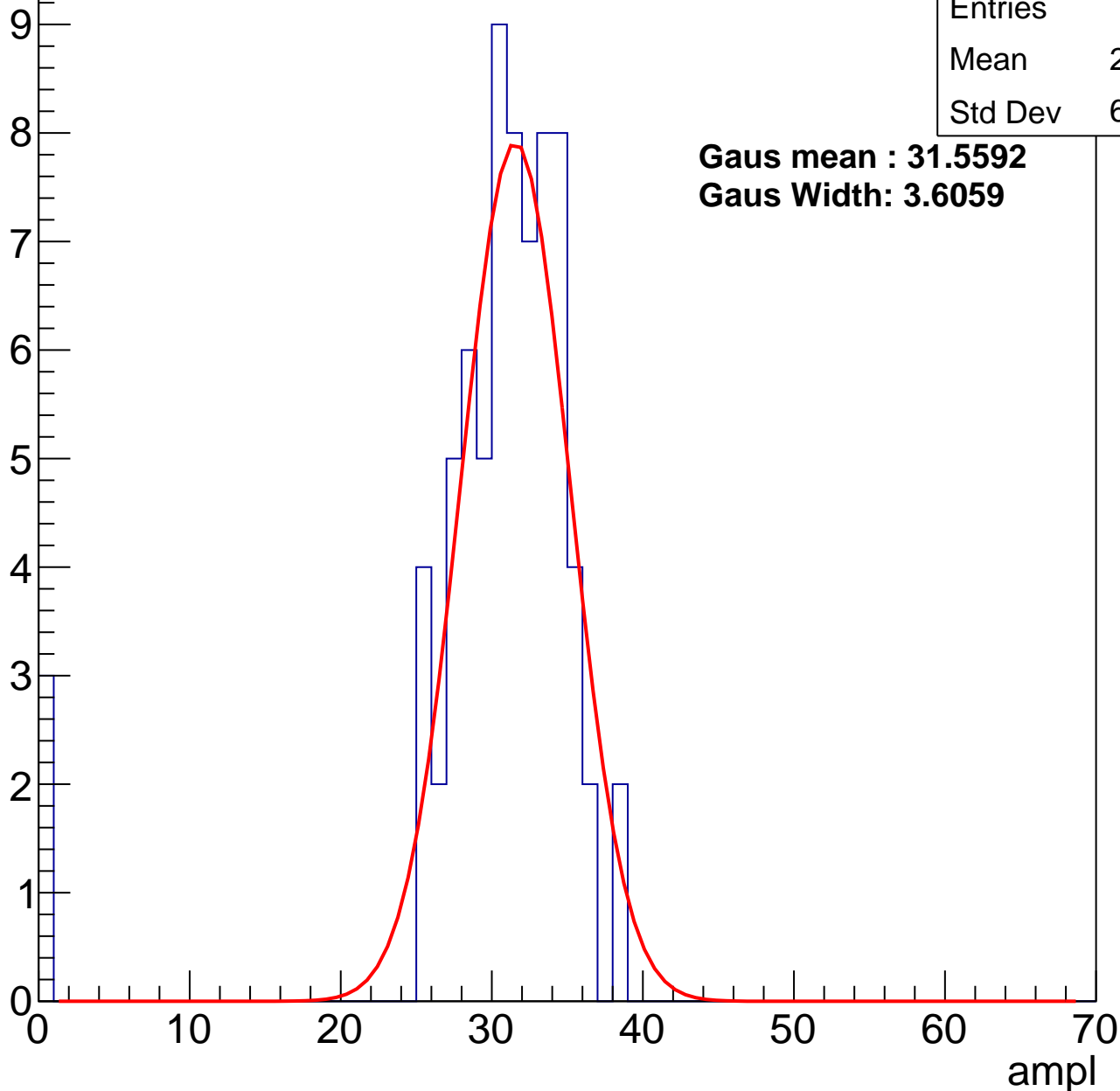
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 73    |
| Mean    | 29.67 |
| Std Dev | 6.859 |

**Gaus mean : 31.5592**

**Gaus Width: 3.6059**



# B0L001S, U2-ch20, adc1

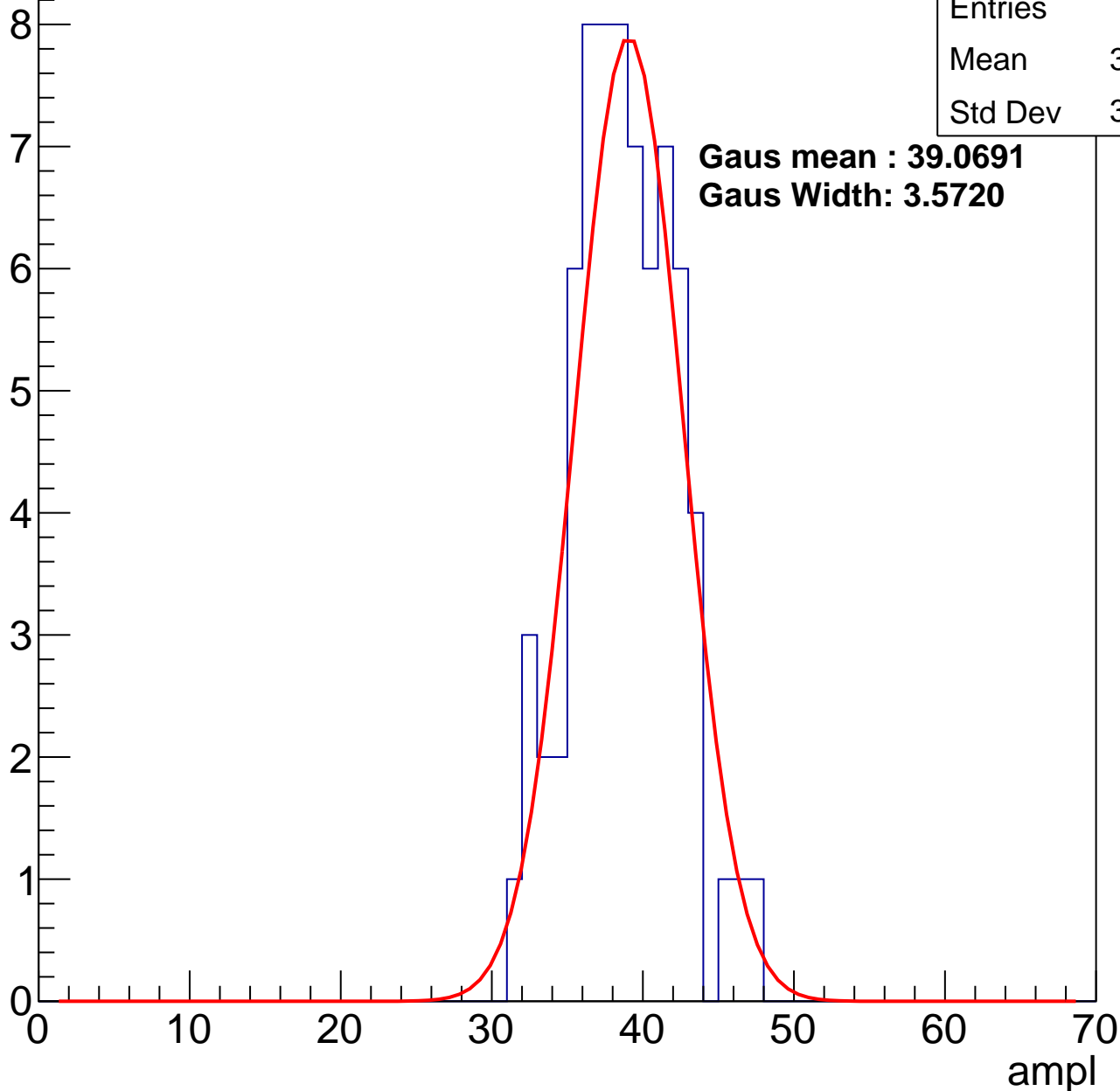
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 71    |
| Mean    | 38.32 |
| Std Dev | 3.377 |

**Gaus mean : 39.0691**

**Gaus Width: 3.5720**



# B0L001S, U2-ch20, adc2

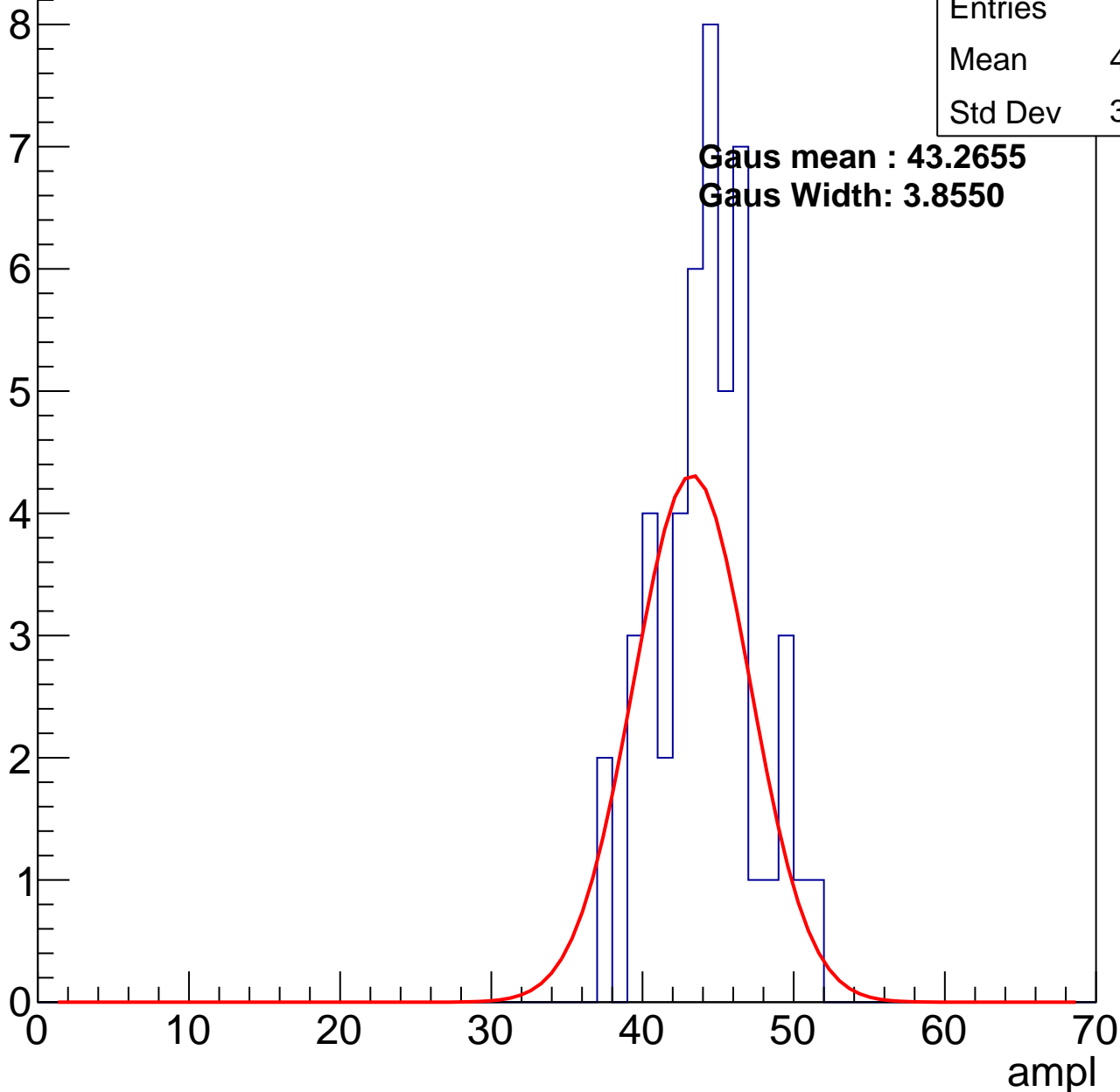
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 48    |
| Mean    | 43.77 |
| Std Dev | 3.203 |

**Gaus mean : 43.2655**

**Gaus Width: 3.8550**



# B0L001S, U2-ch20, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 68    |
| Mean    | 49.56 |
| Std Dev | 2.882 |

Entry

10

8

6

4

2

0

0

10

20

30

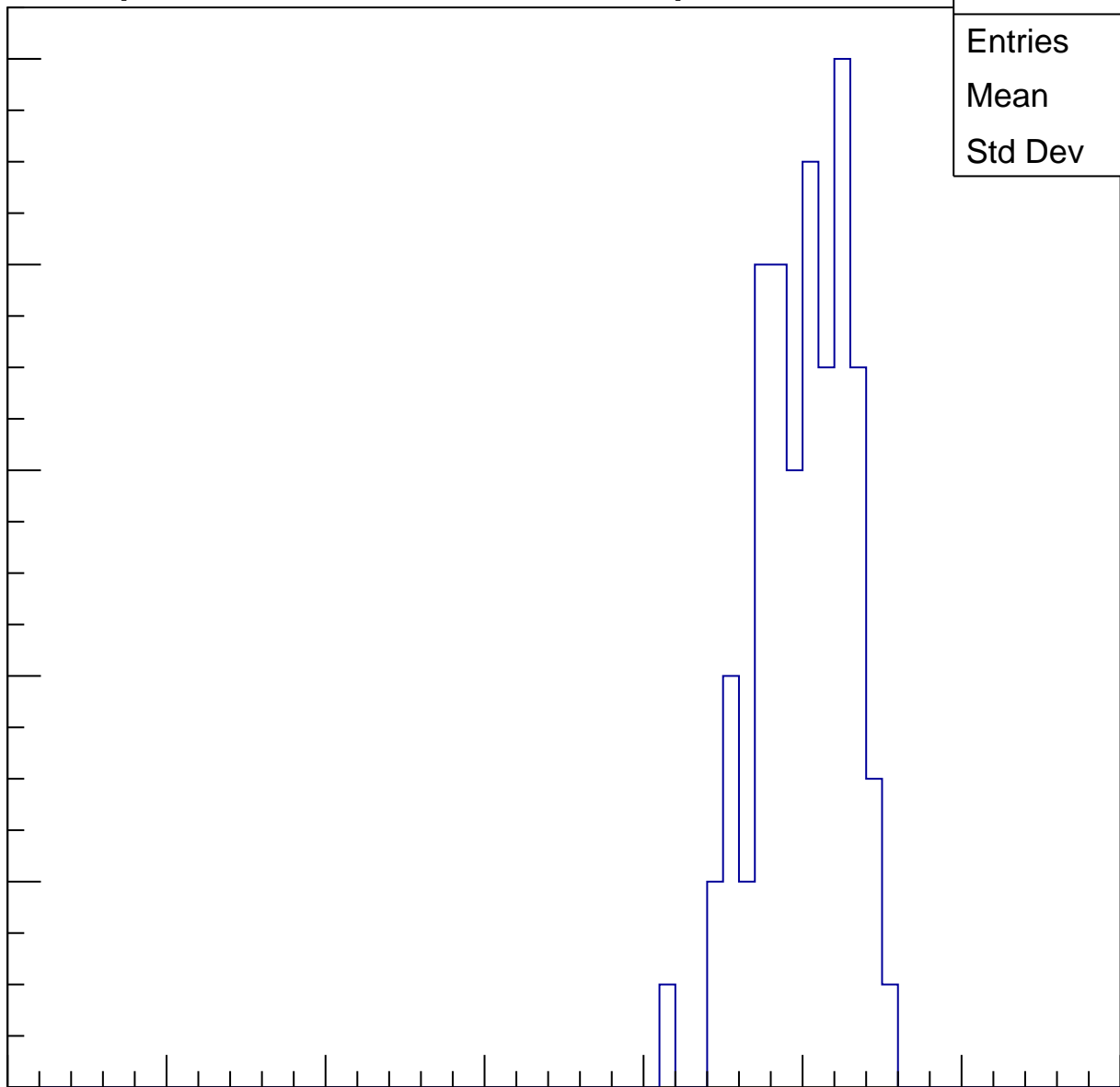
40

50

60

70

ampl



# B0L001S, U2-ch20, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

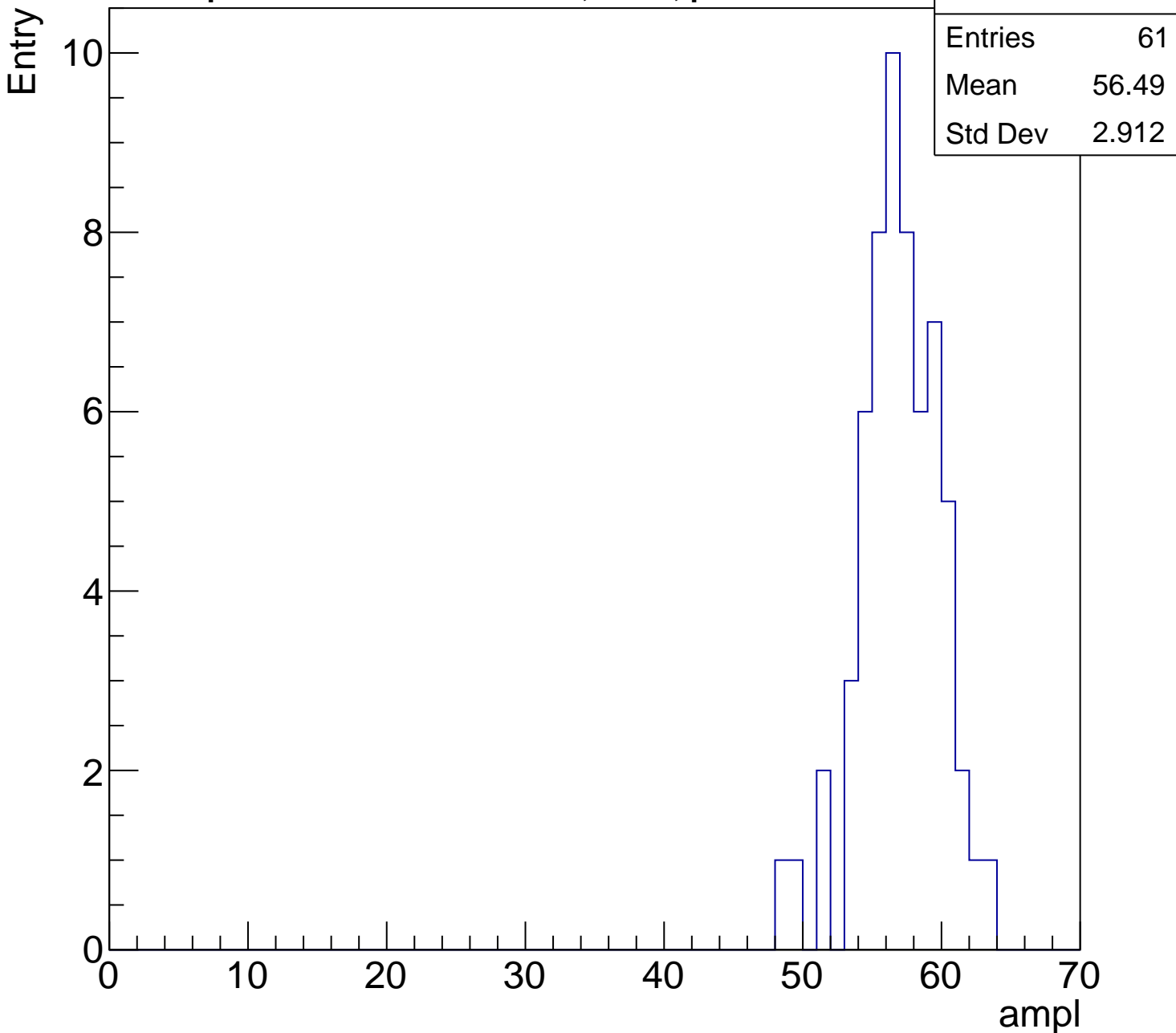
|         |       |
|---------|-------|
| Entries | 61    |
| Mean    | 56.49 |
| Std Dev | 2.912 |

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

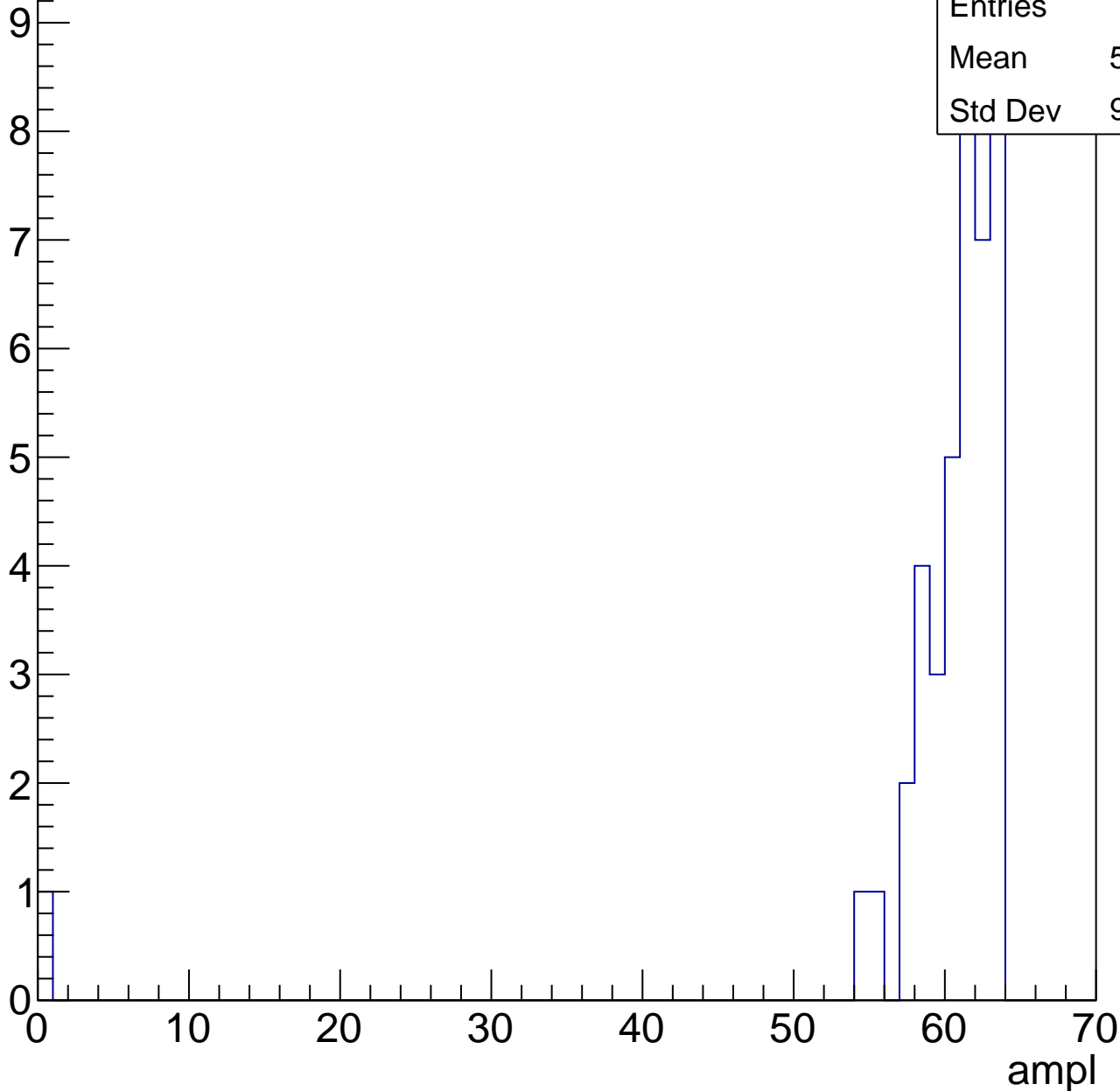


# B0L001S, U2-ch20, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 41    |
| Mean    | 59.05 |
| Std Dev | 9.599 |



# B0L001S, U2-ch20, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch20, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

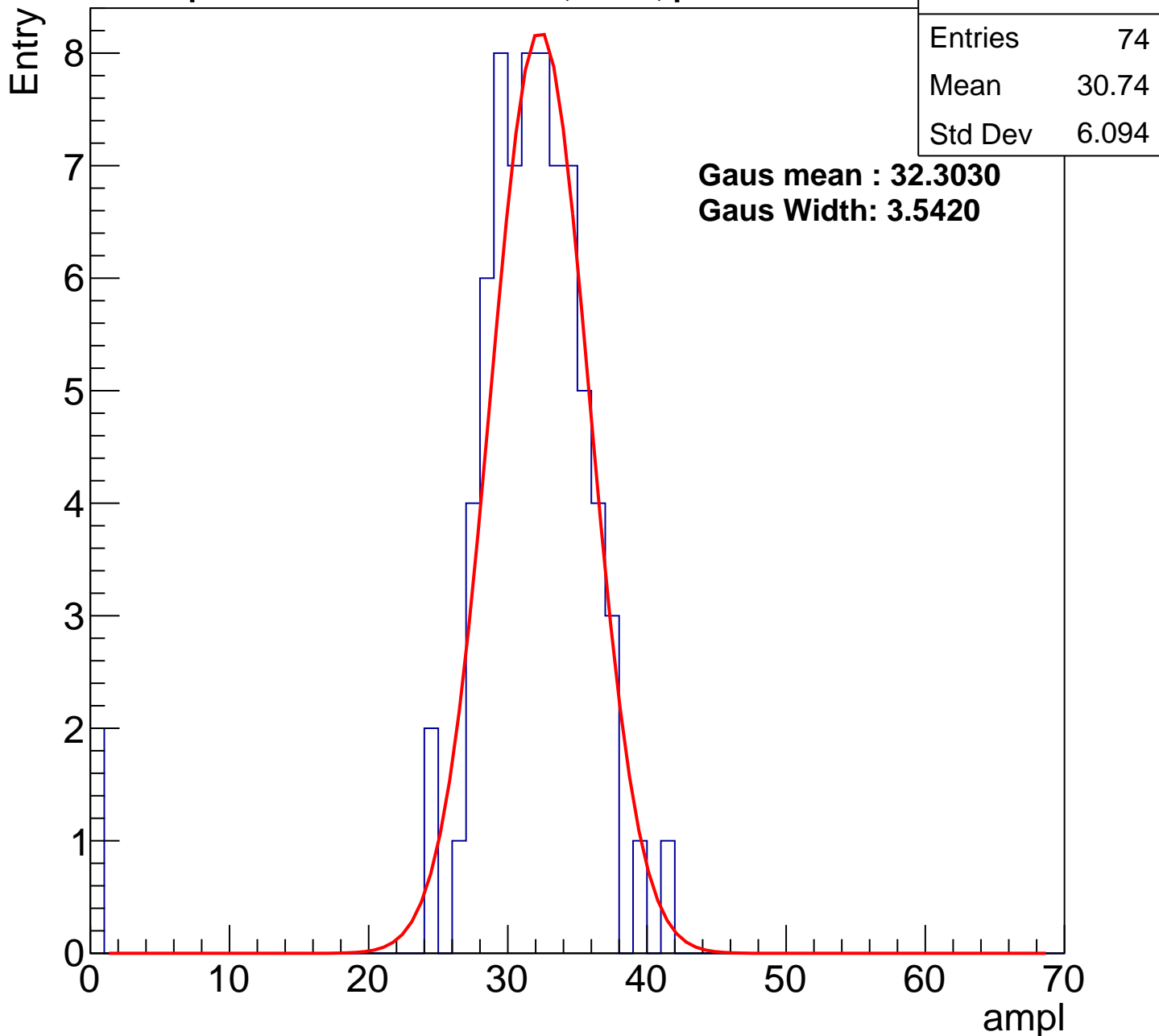
Entry



|         |   |
|---------|---|
| Entries | 0 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch21, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U2-ch21, adc1

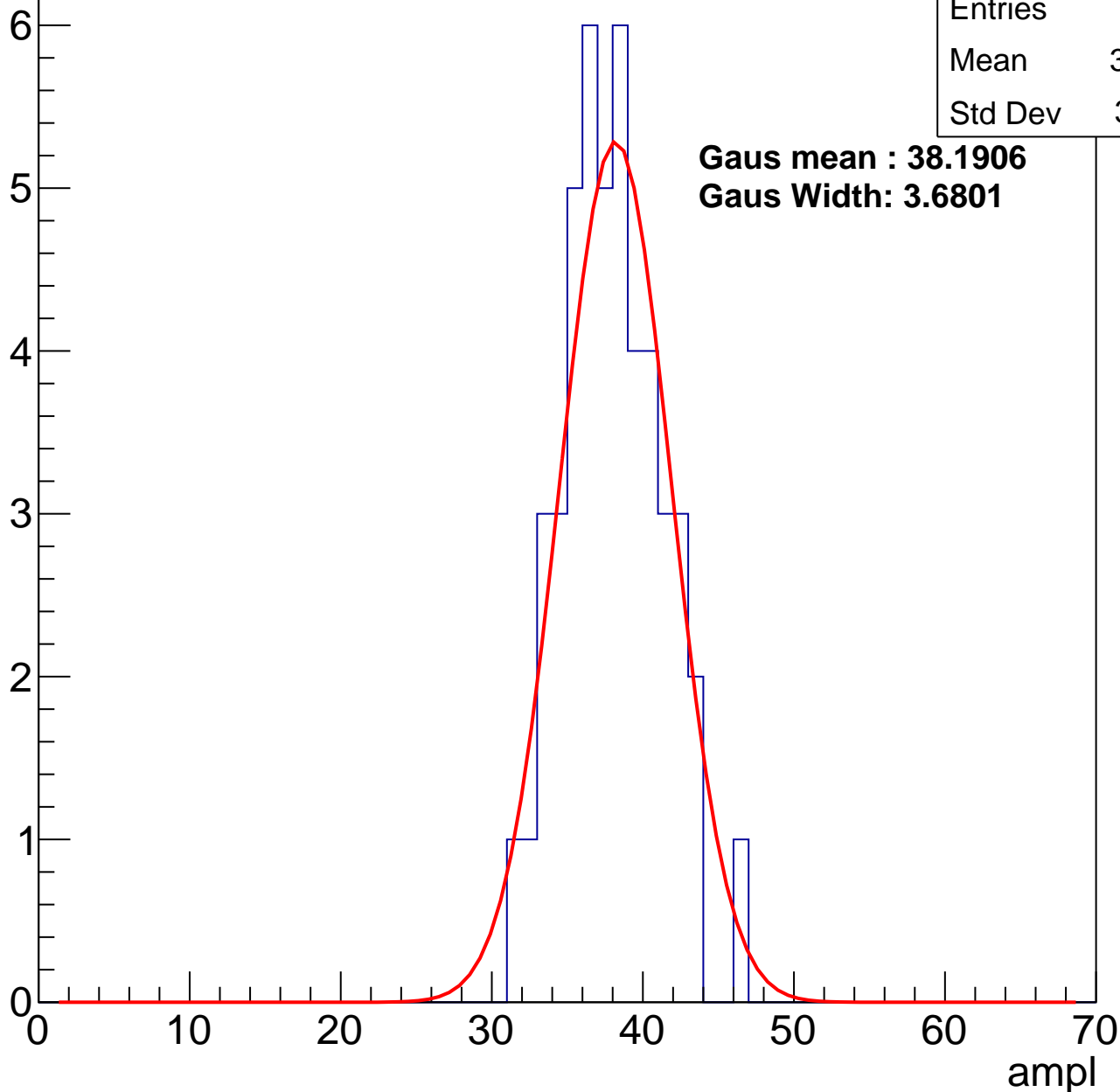
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 47    |
| Mean    | 37.55 |
| Std Dev | 3.201 |

**Gaus mean : 38.1906**

**Gaus Width: 3.6801**



# B0L001S, U2-ch21, adc2

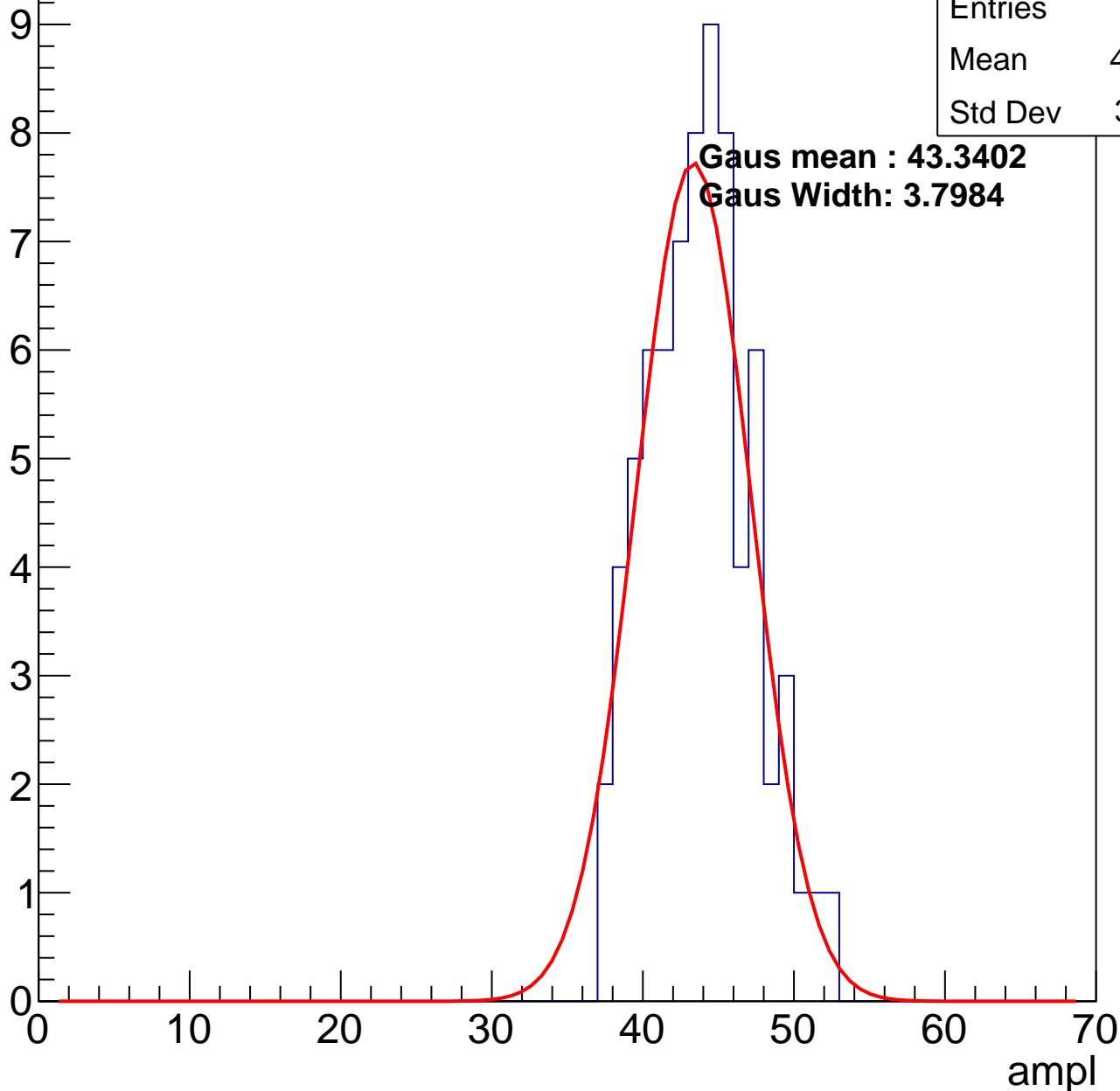
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 73    |
| Mean    | 43.33 |
| Std Dev | 3.421 |

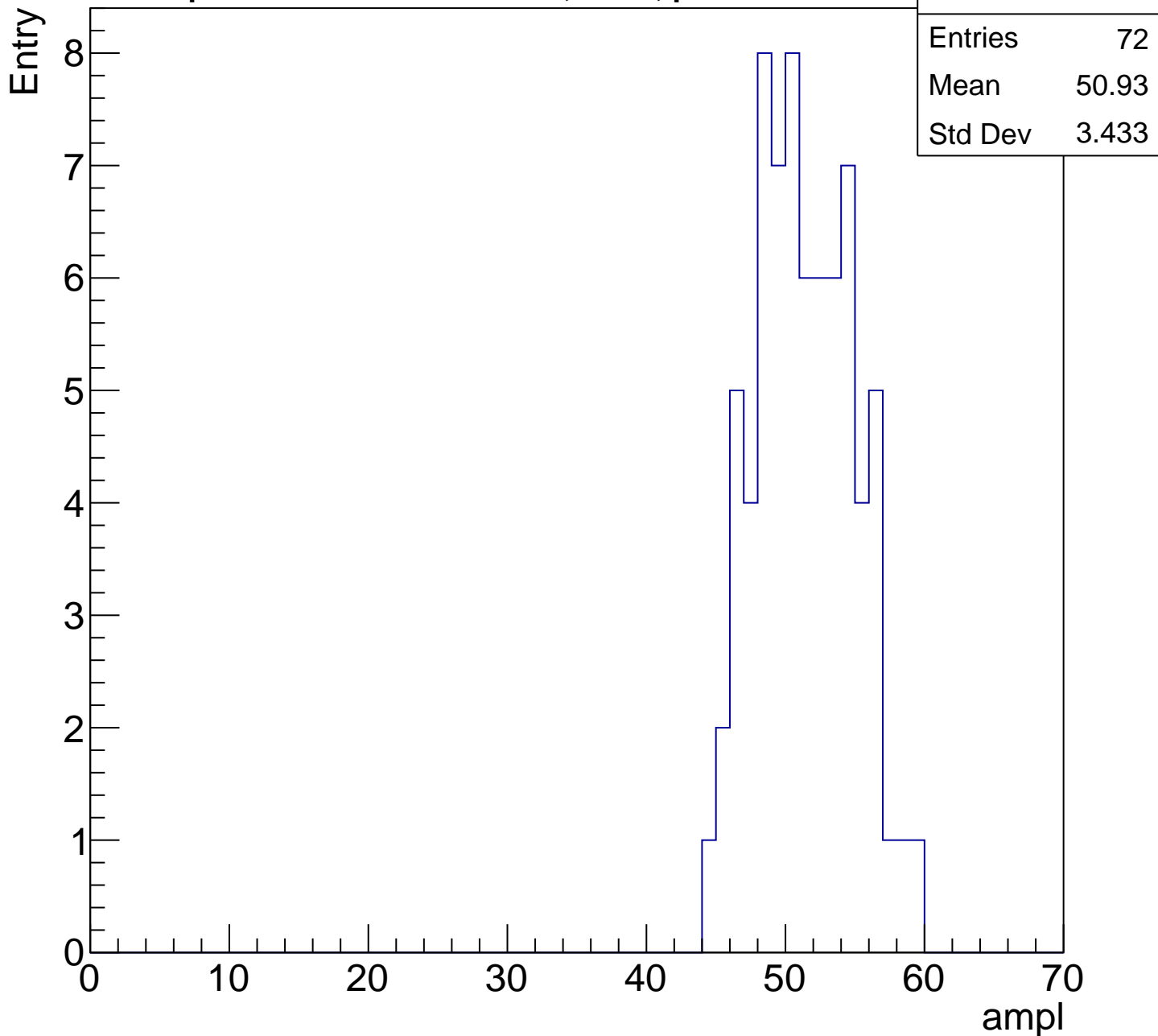
**Gaus mean : 43.3402**

**Gaus Width: 3.7984**



# B0L001S, U2-ch21, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

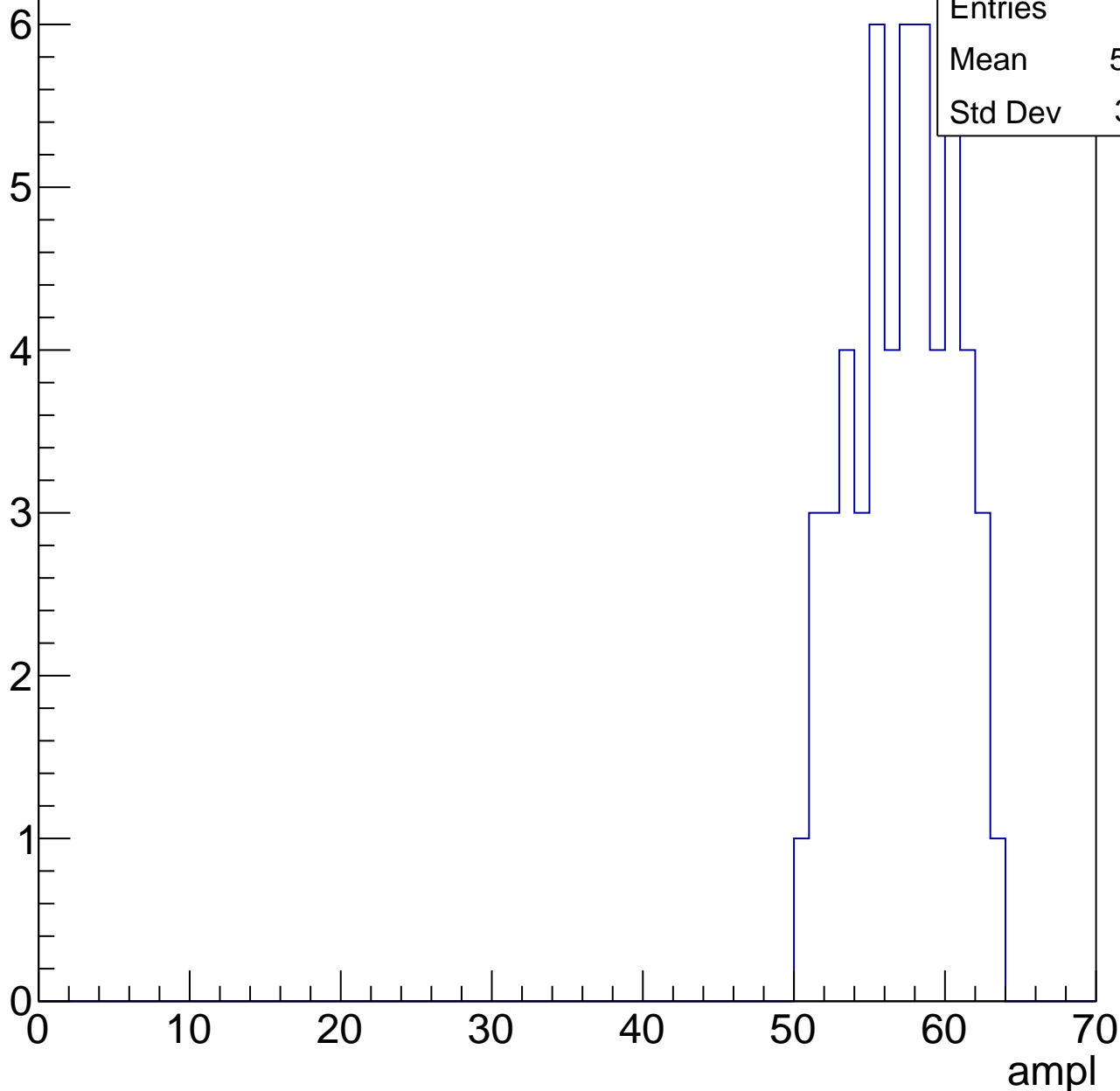


# B0L001S, U2-ch21, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 54    |
| Mean    | 56.78 |
| Std Dev | 3.331 |

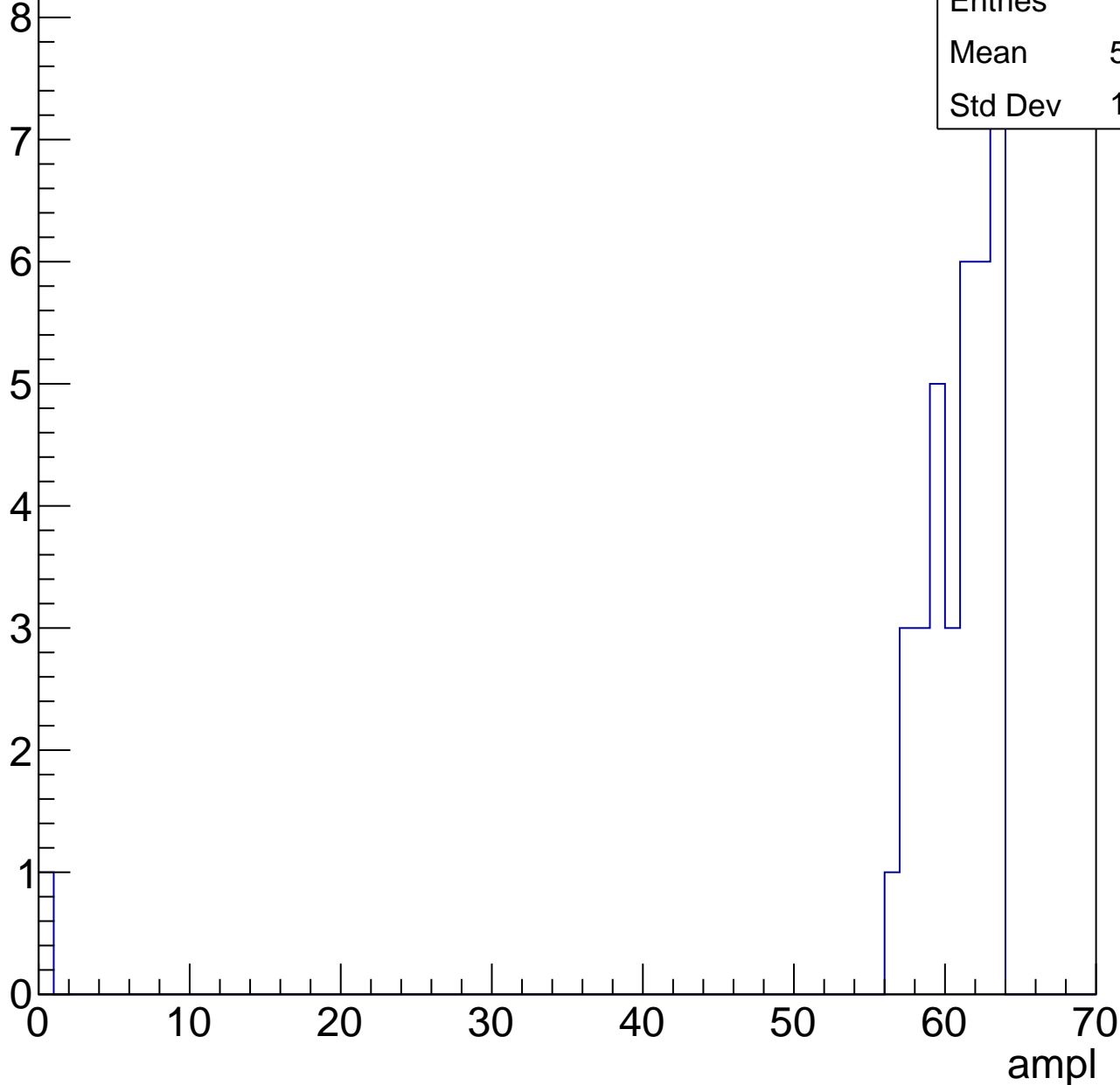


# B0L001S, U2-ch21, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 36    |
| Mean    | 58.83 |
| Std Dev | 10.16 |



# B0L001S, U2-ch21, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

|         |       |
|---------|-------|
| Entries | 3     |
| Mean    | 61.67 |
| Std Dev | 1.247 |

ampl

0 10 20 30 40 50 60 70



# B0L001S, U2-ch21, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 0 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch22, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 68    |
| Mean    | 28.53 |
| Std Dev | 6.95  |

**Gaus mean : 30.4650**

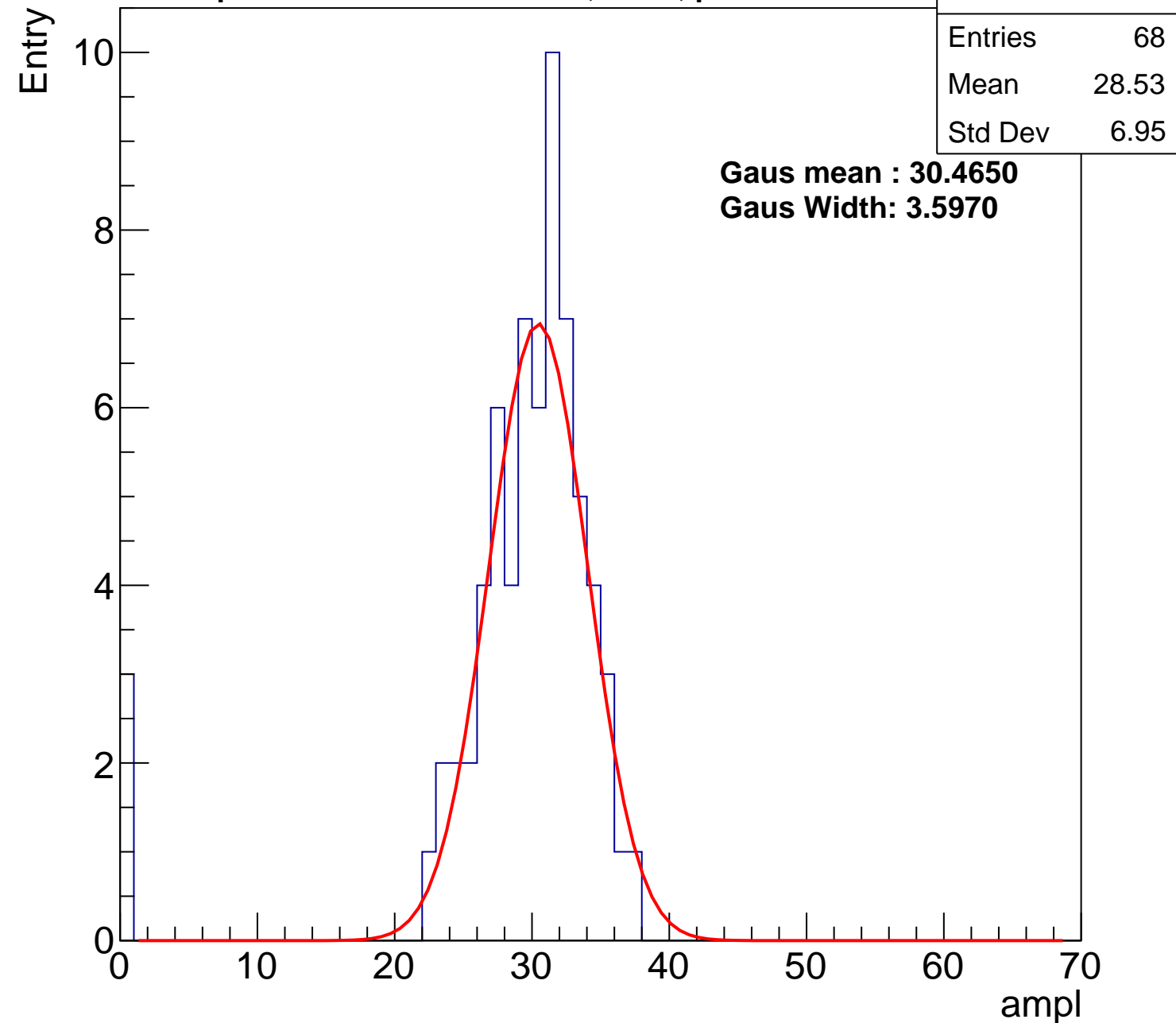
**Gaus Width: 3.5970**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



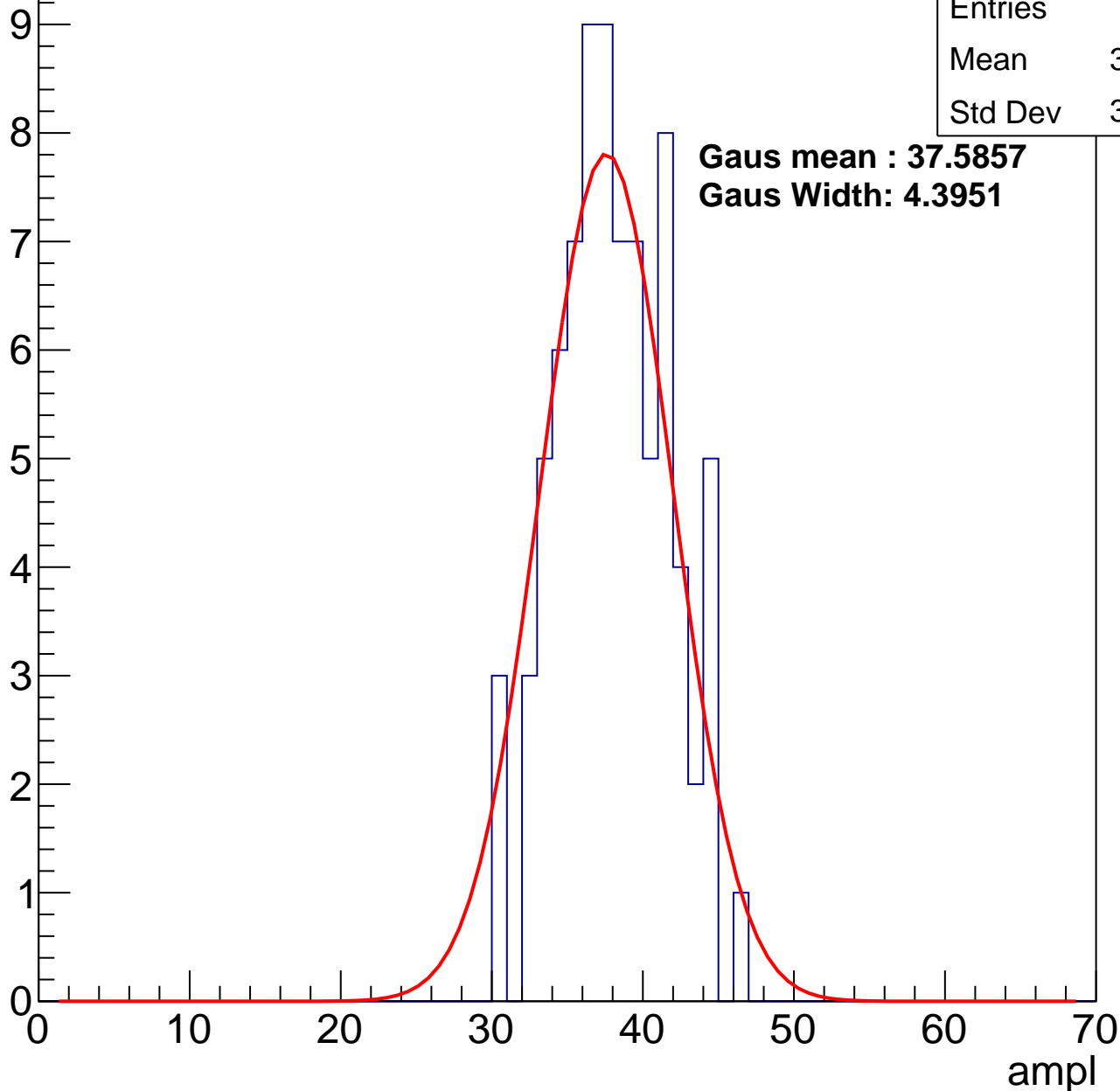
# B0L001S, U2-ch22, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 81    |
| Mean    | 37.58 |
| Std Dev | 3.637 |

**Gaus mean : 37.5857**  
**Gaus Width: 4.3951**



# B0L001S, U2-ch22, adc2

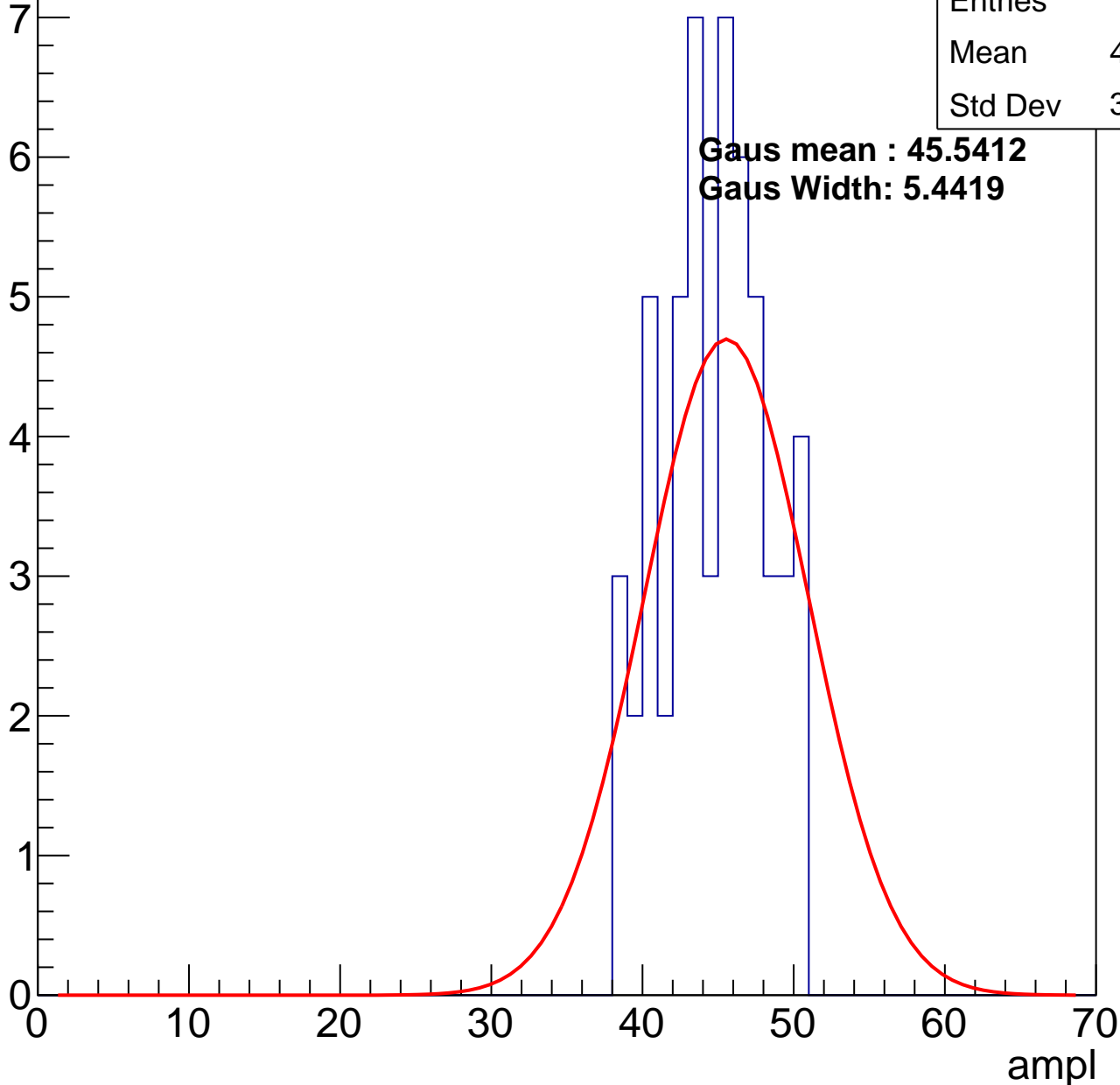
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 55    |
| Mean    | 44.25 |
| Std Dev | 3.364 |

**Gaus mean : 45.5412**

**Gaus Width: 5.4419**

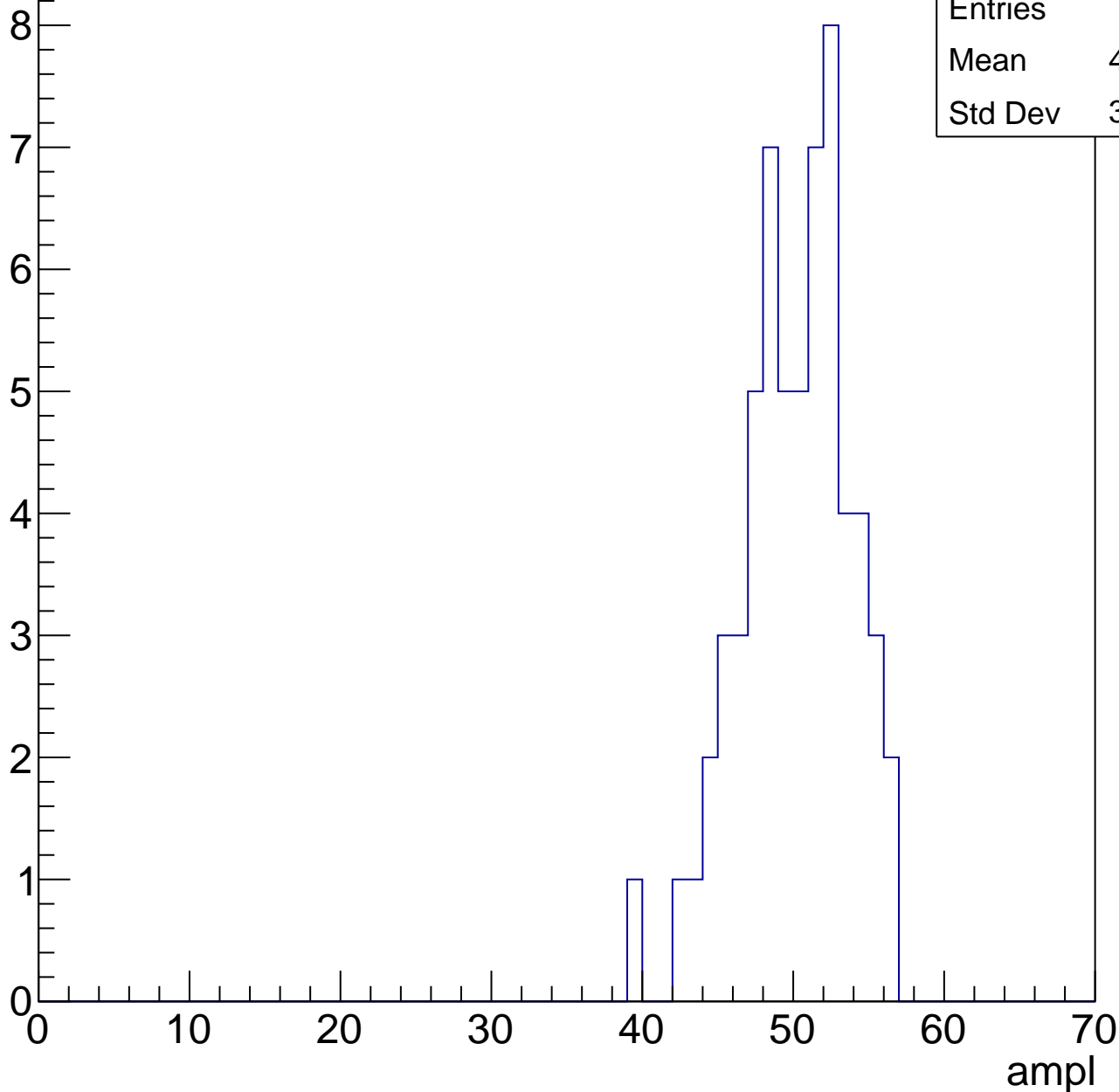


# B0L001S, U2-ch22, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

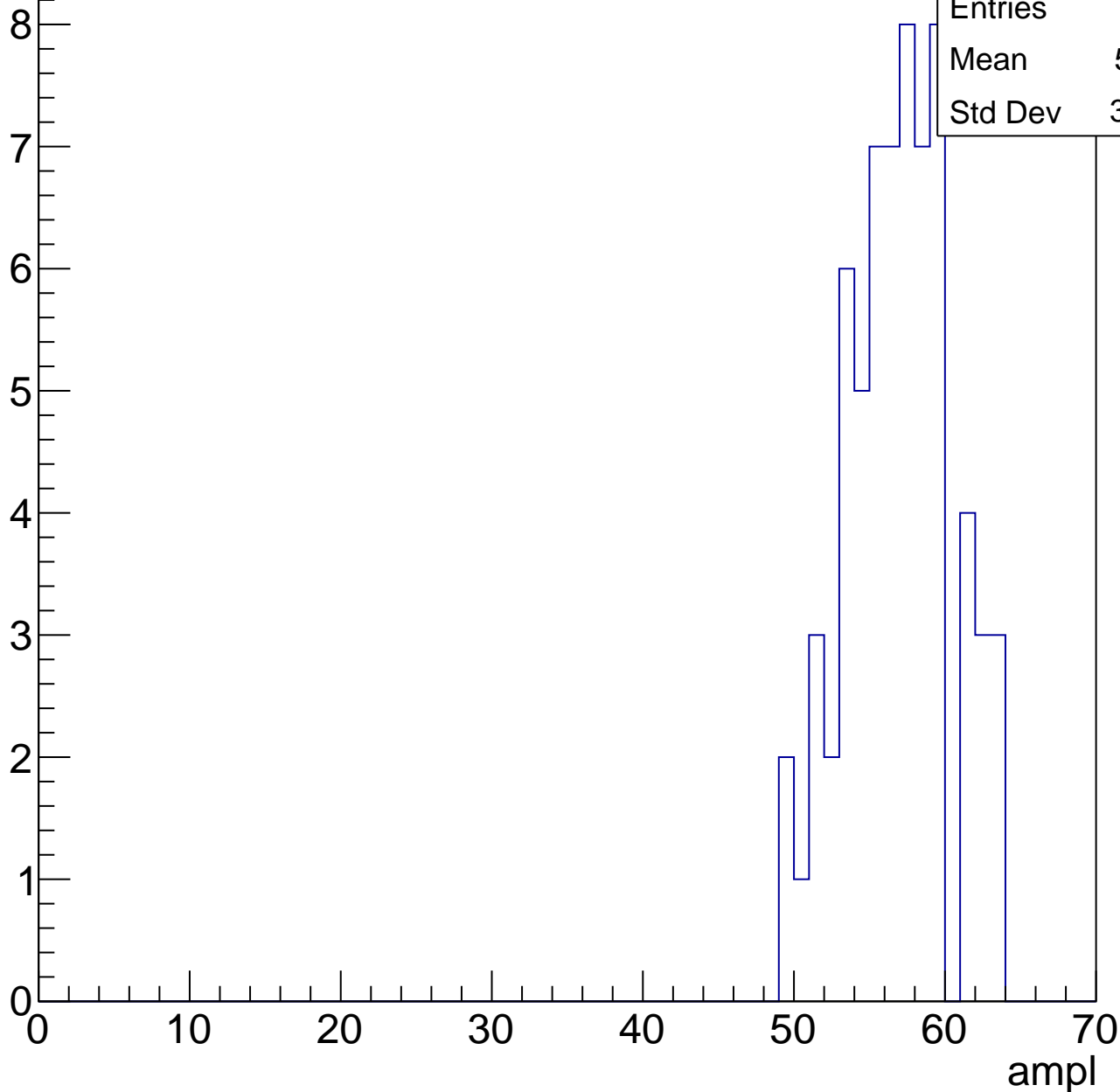
|         |       |
|---------|-------|
| Entries | 61    |
| Mean    | 49.66 |
| Std Dev | 3.589 |



# B0L001S, U2-ch22, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



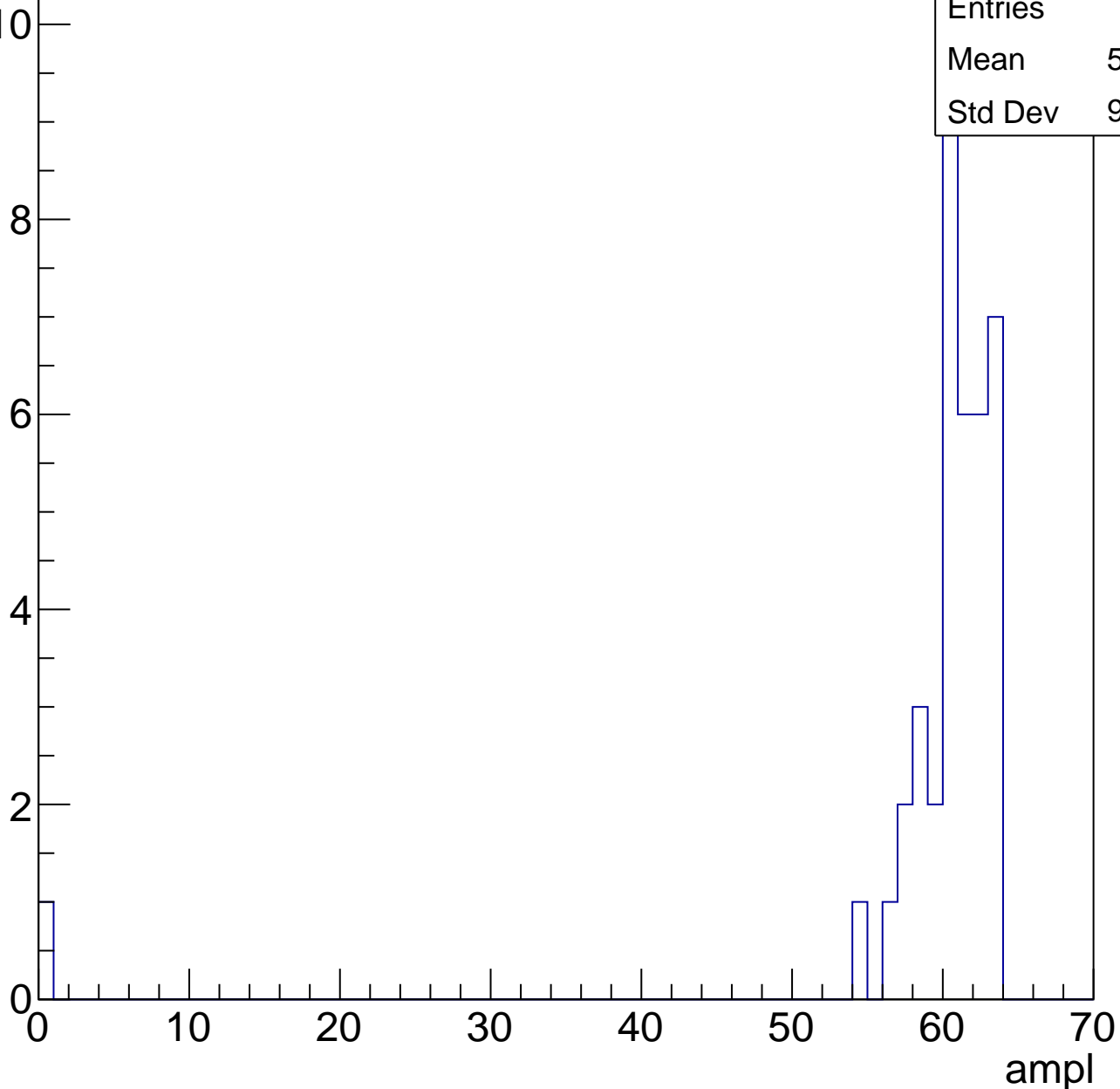
|         |       |
|---------|-------|
| Entries | 66    |
| Mean    | 56.41 |
| Std Dev | 3.424 |

# B0L001S, U2-ch22, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

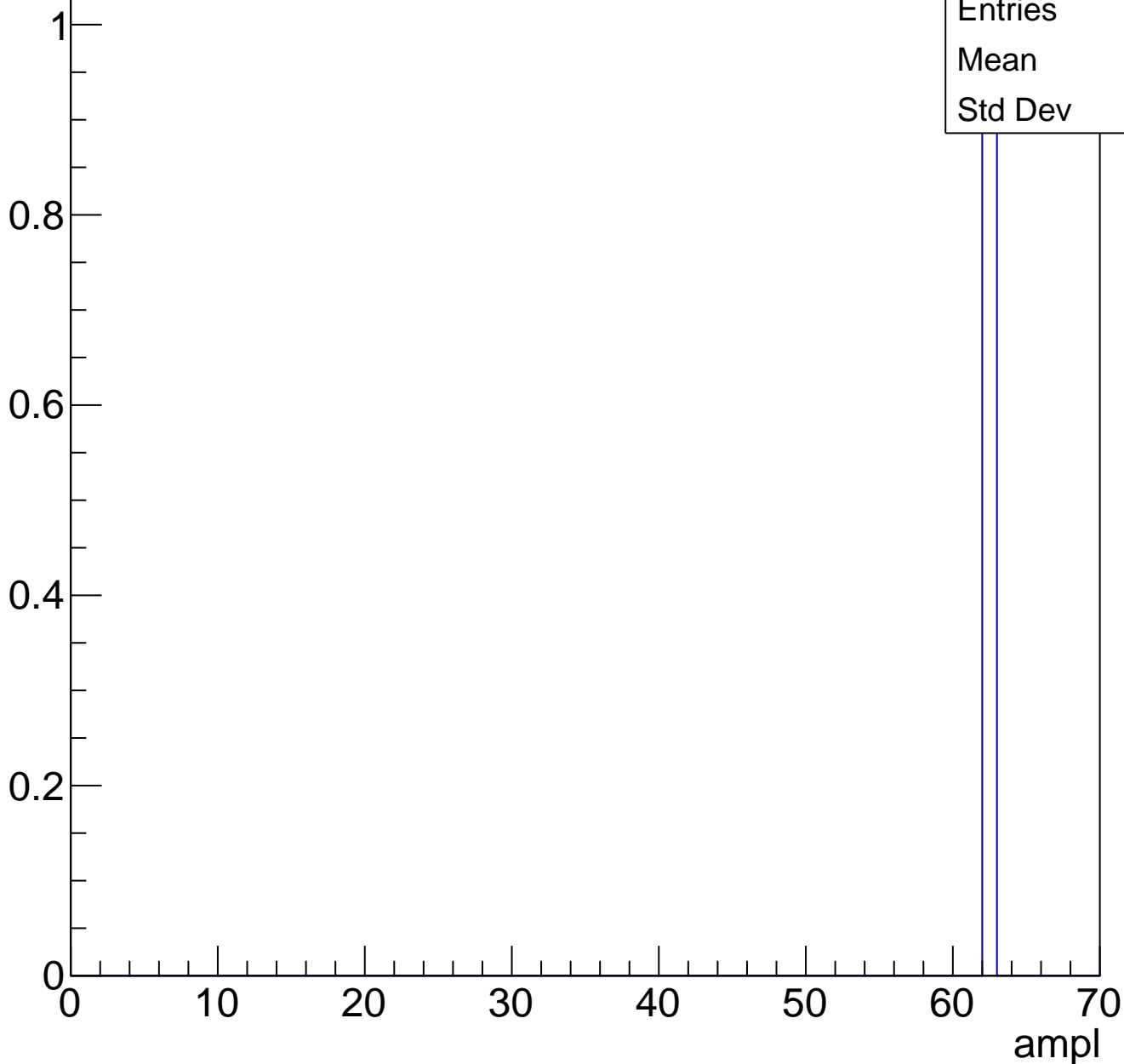
|         |       |
|---------|-------|
| Entries | 39    |
| Mean    | 58.85 |
| Std Dev | 9.773 |



# B0L001S, U2-ch22, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch22, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U2-ch23, adc0

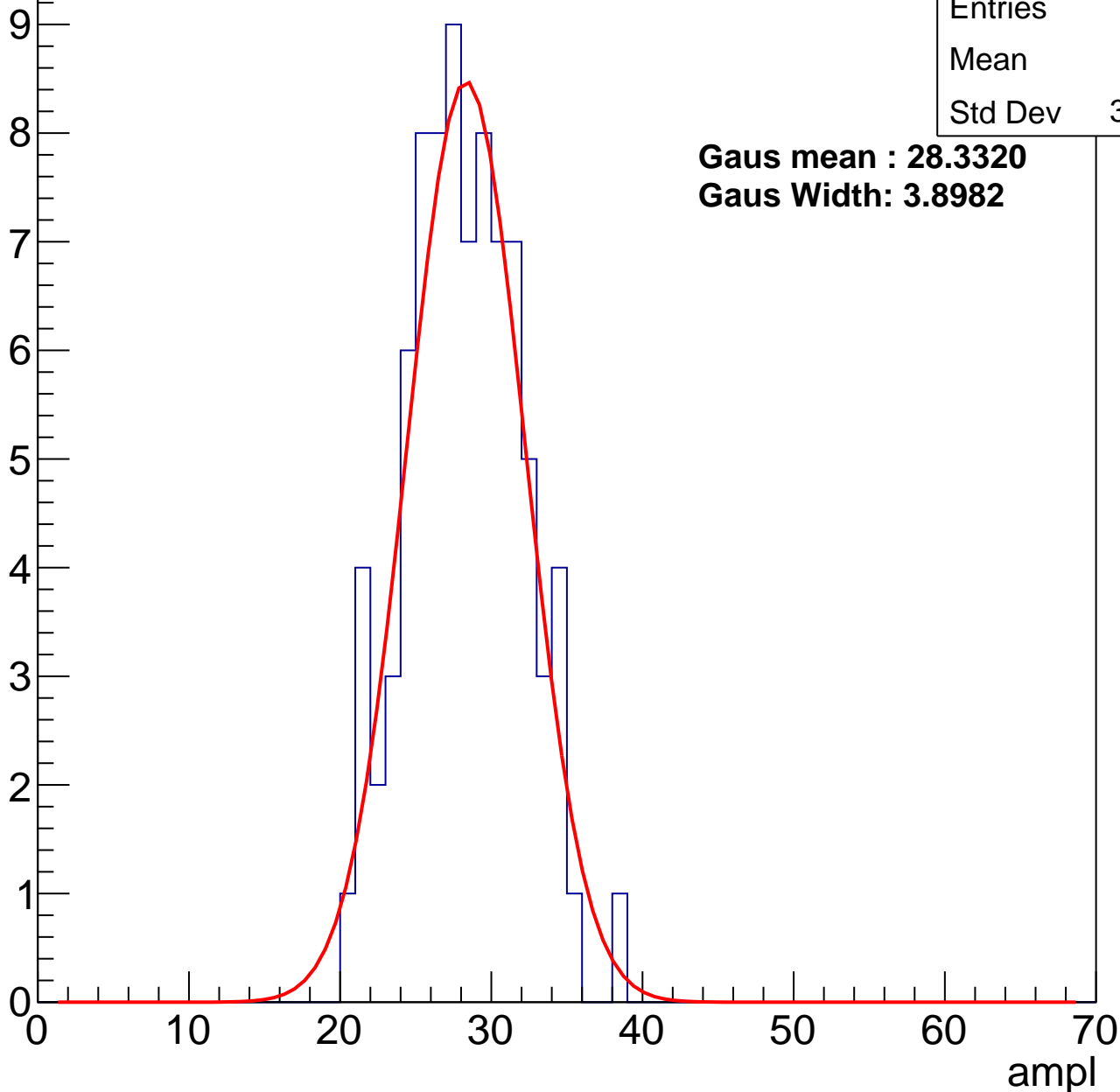
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 84    |
| Mean    | 27.8  |
| Std Dev | 3.715 |

**Gaus mean : 28.3320**

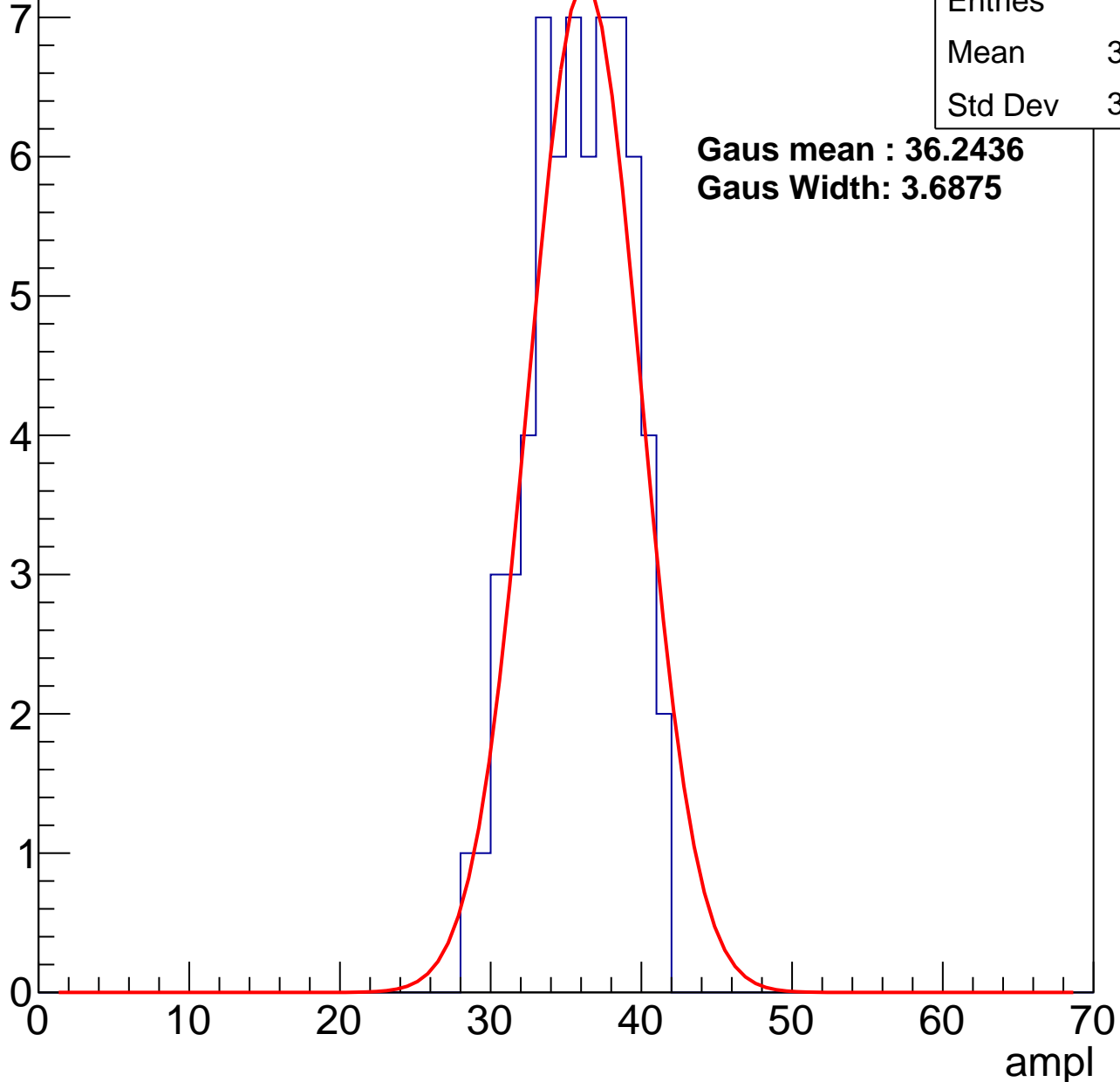
**Gaus Width: 3.8982**



# B0L001S, U2-ch23, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U2-ch23, adc2

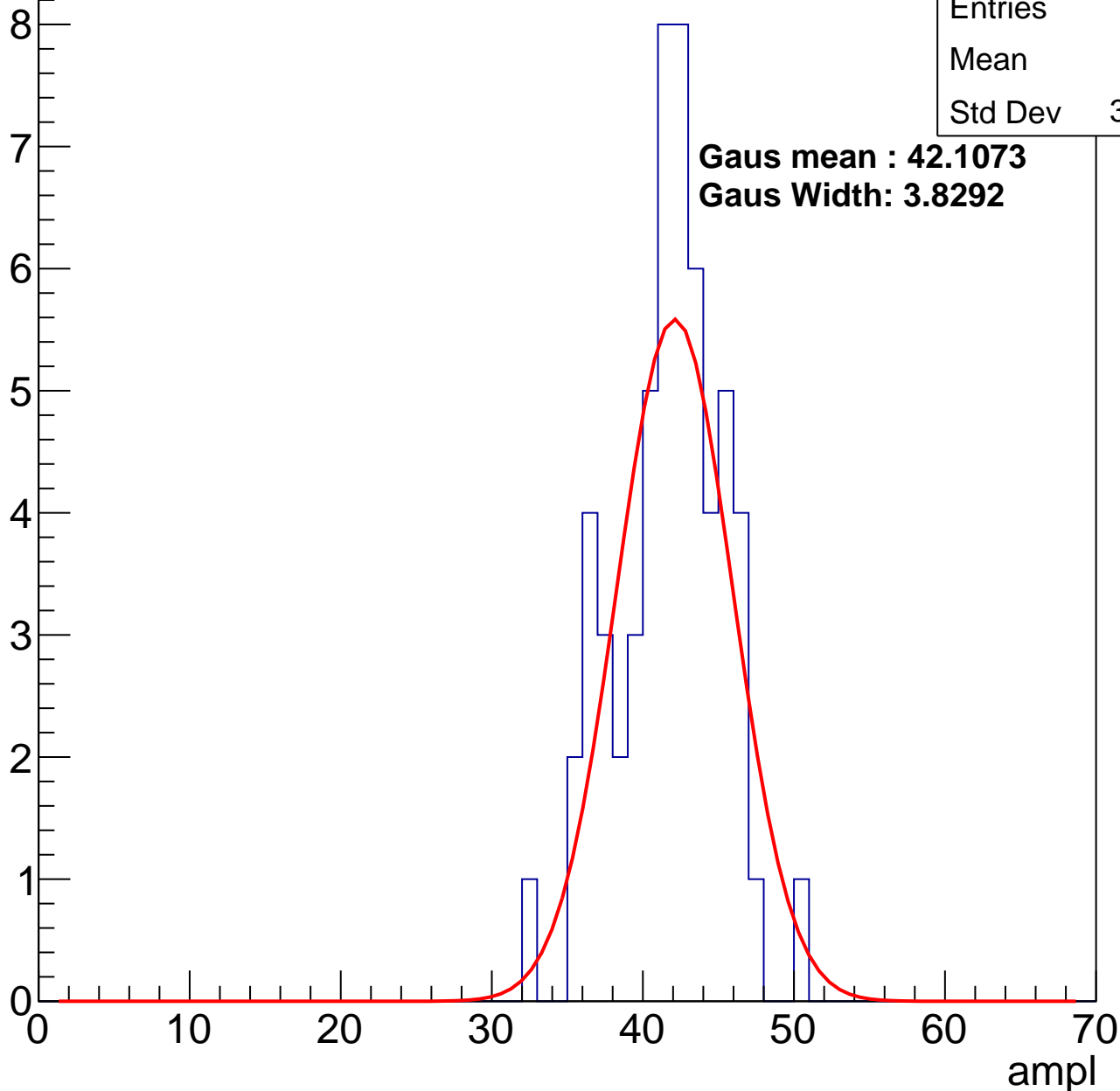
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 57    |
| Mean    | 41.3  |
| Std Dev | 3.494 |

**Gaus mean : 42.1073**

**Gaus Width: 3.8292**

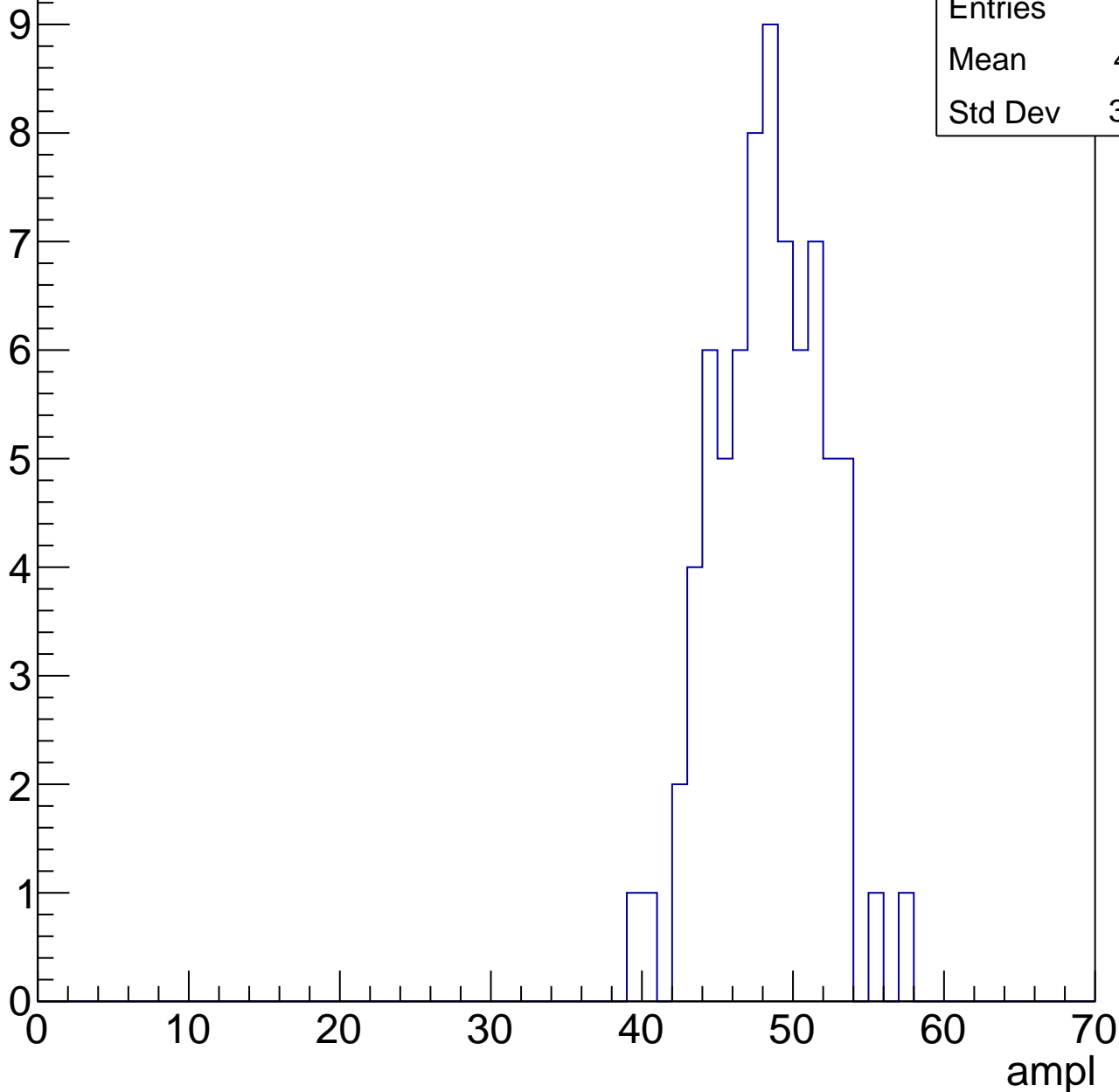


# B0L001S, U2-ch23, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 74    |
| Mean    | 47.91 |
| Std Dev | 3.523 |

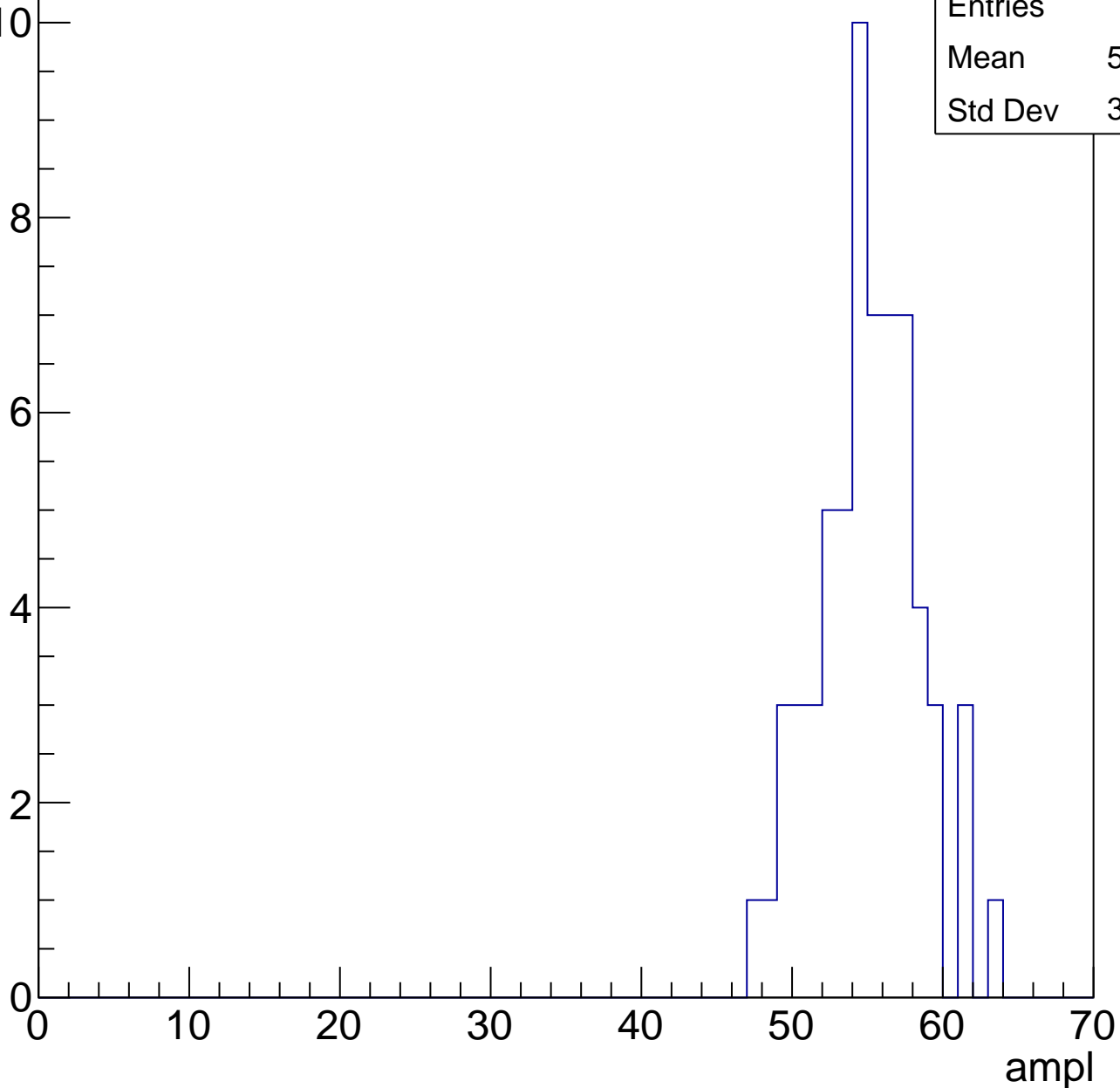


# B0L001S, U2-ch23, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

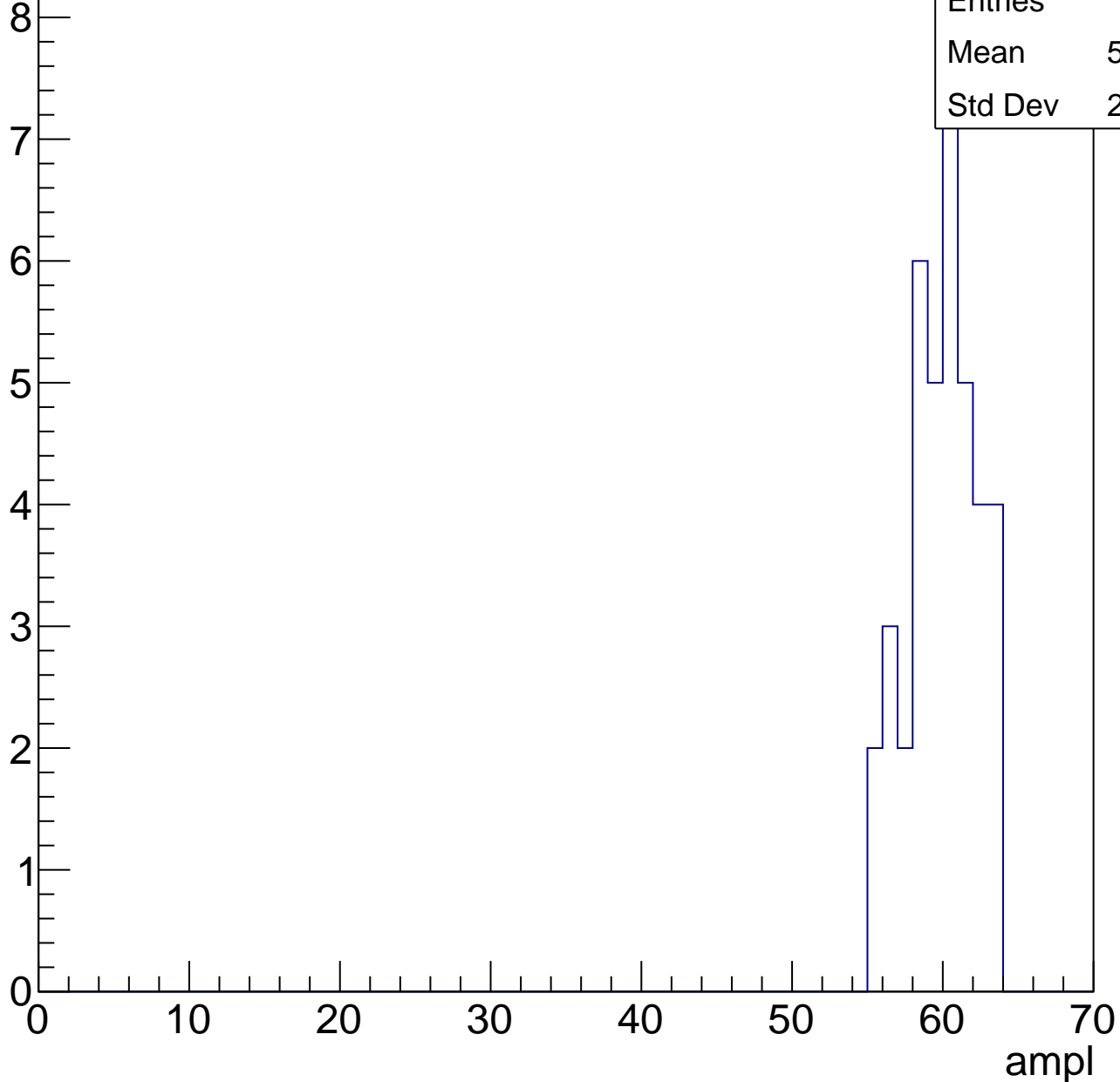
|         |       |
|---------|-------|
| Entries | 63    |
| Mean    | 54.62 |
| Std Dev | 3.335 |



# B0L001S, U2-ch23, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

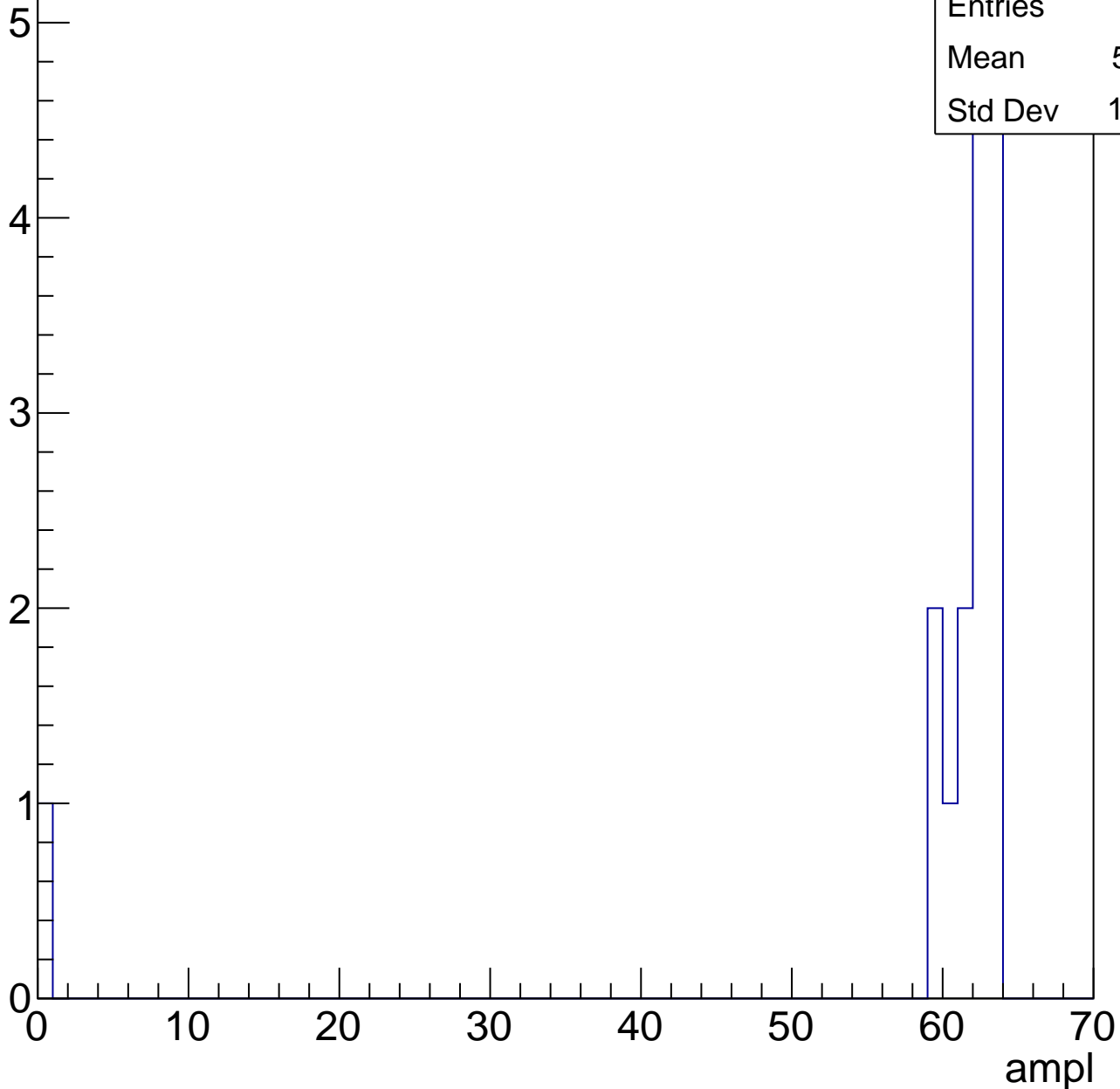


# B0L001S, U2-ch23, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 16    |
| Mean    | 57.81 |
| Std Dev | 14.98 |

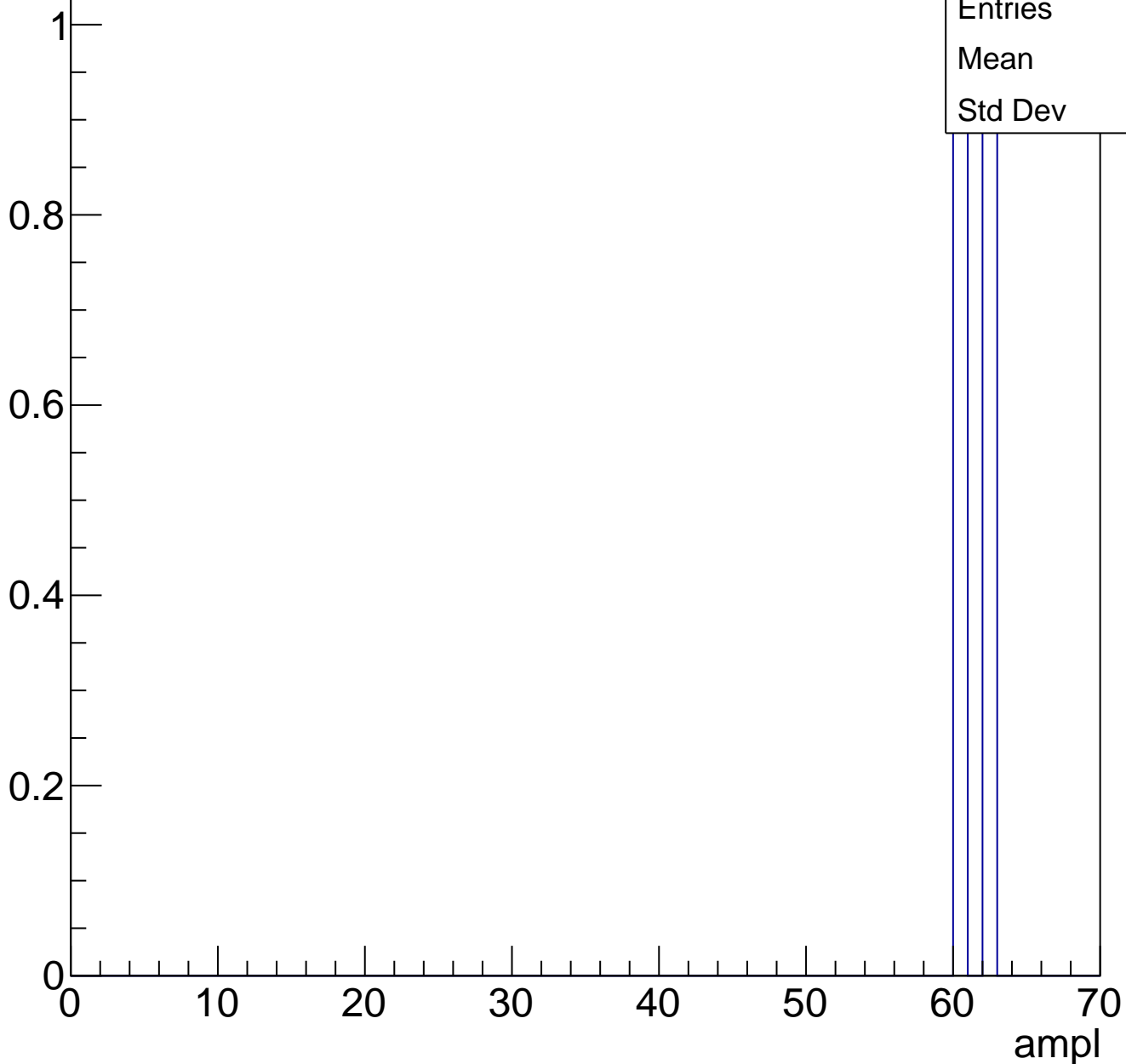




# B0L001S, U2-ch23, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U2-ch24, adc0

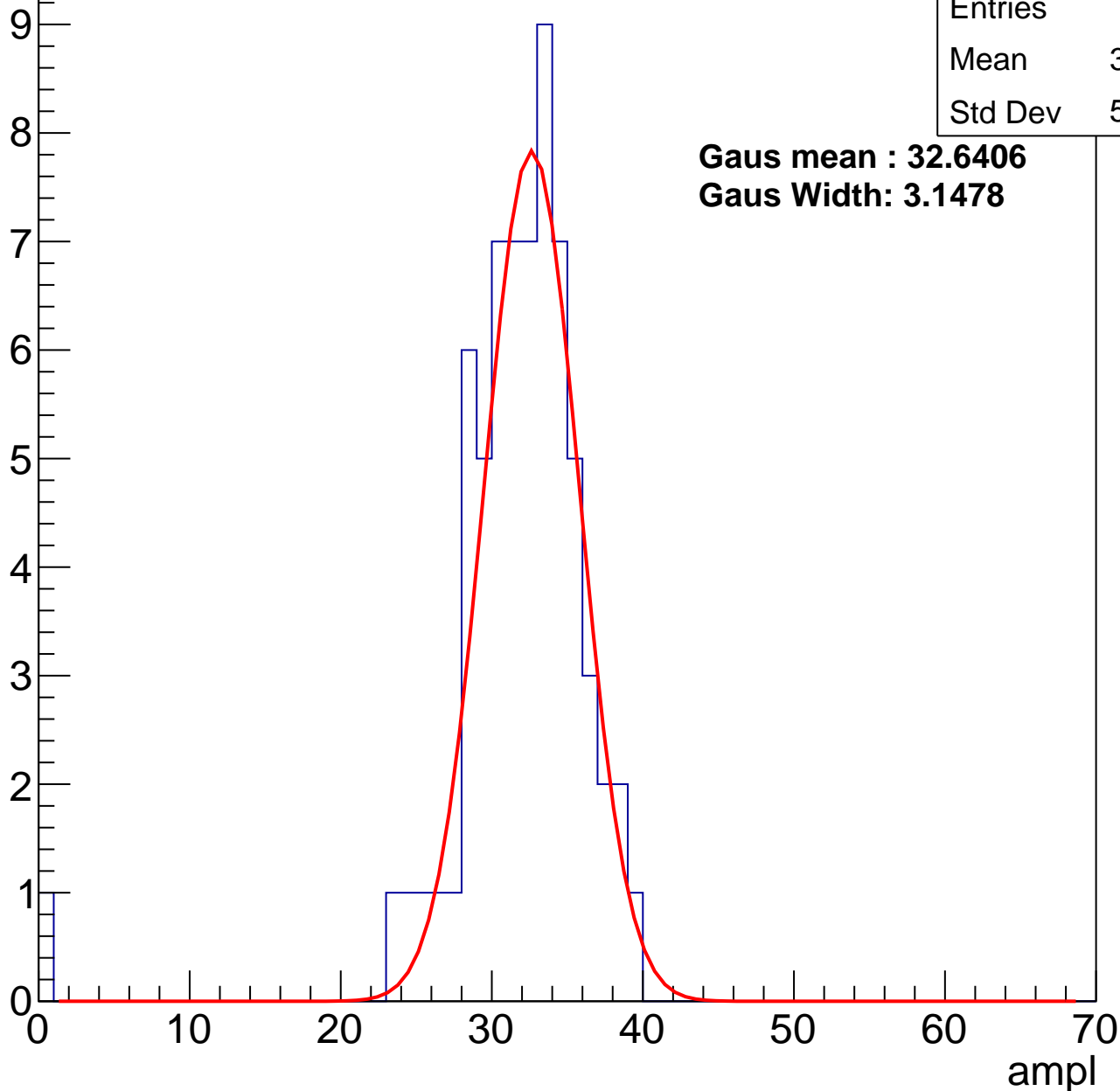
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 67    |
| Mean    | 31.28 |
| Std Dev | 5.069 |

**Gaus mean : 32.6406**

**Gaus Width: 3.1478**



# B0L001S, U2-ch24, adc1

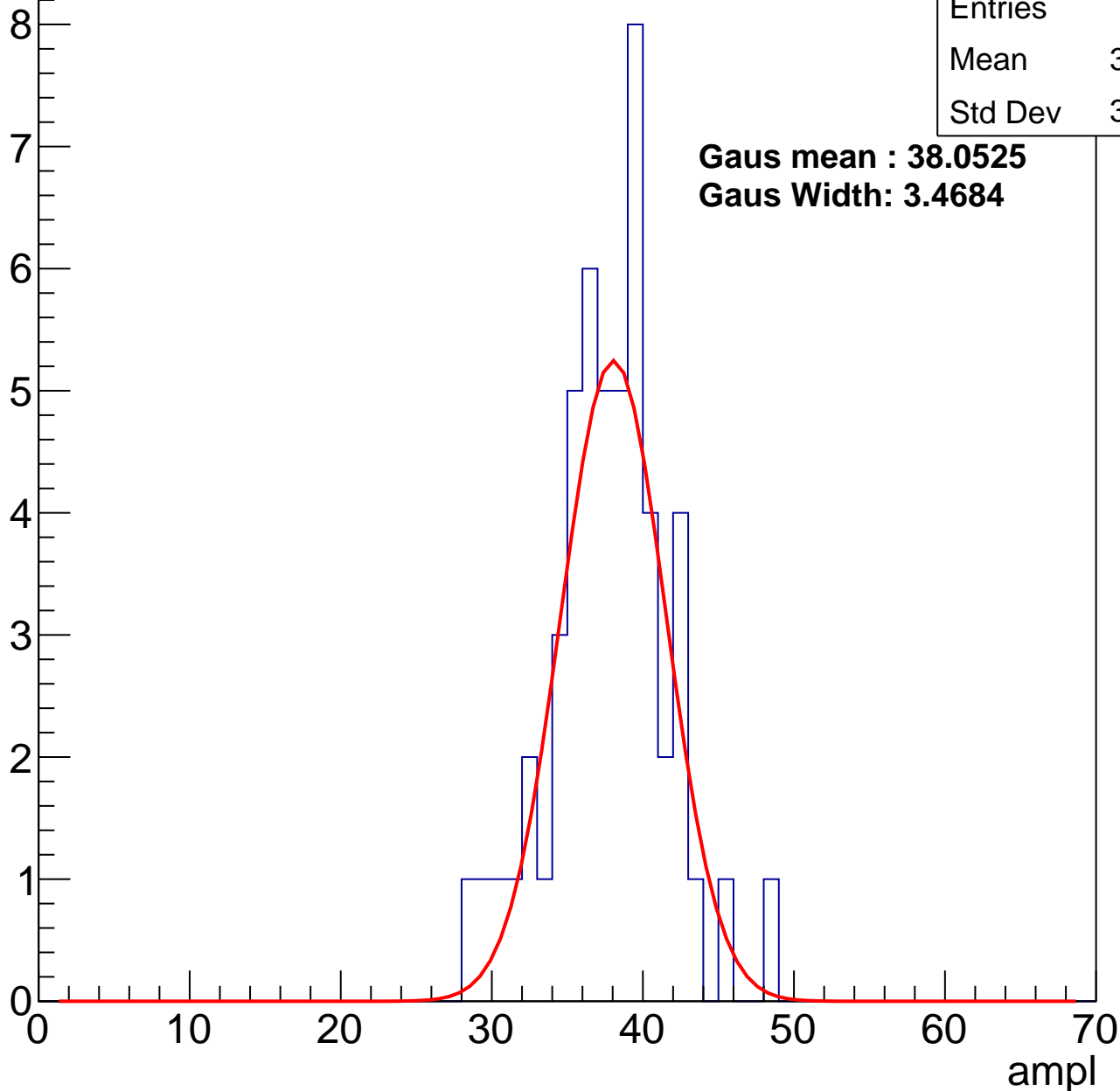
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 52    |
| Mean    | 37.33 |
| Std Dev | 3.847 |

**Gaus mean : 38.0525**

**Gaus Width: 3.4684**



# B0L001S, U2-ch24, adc2

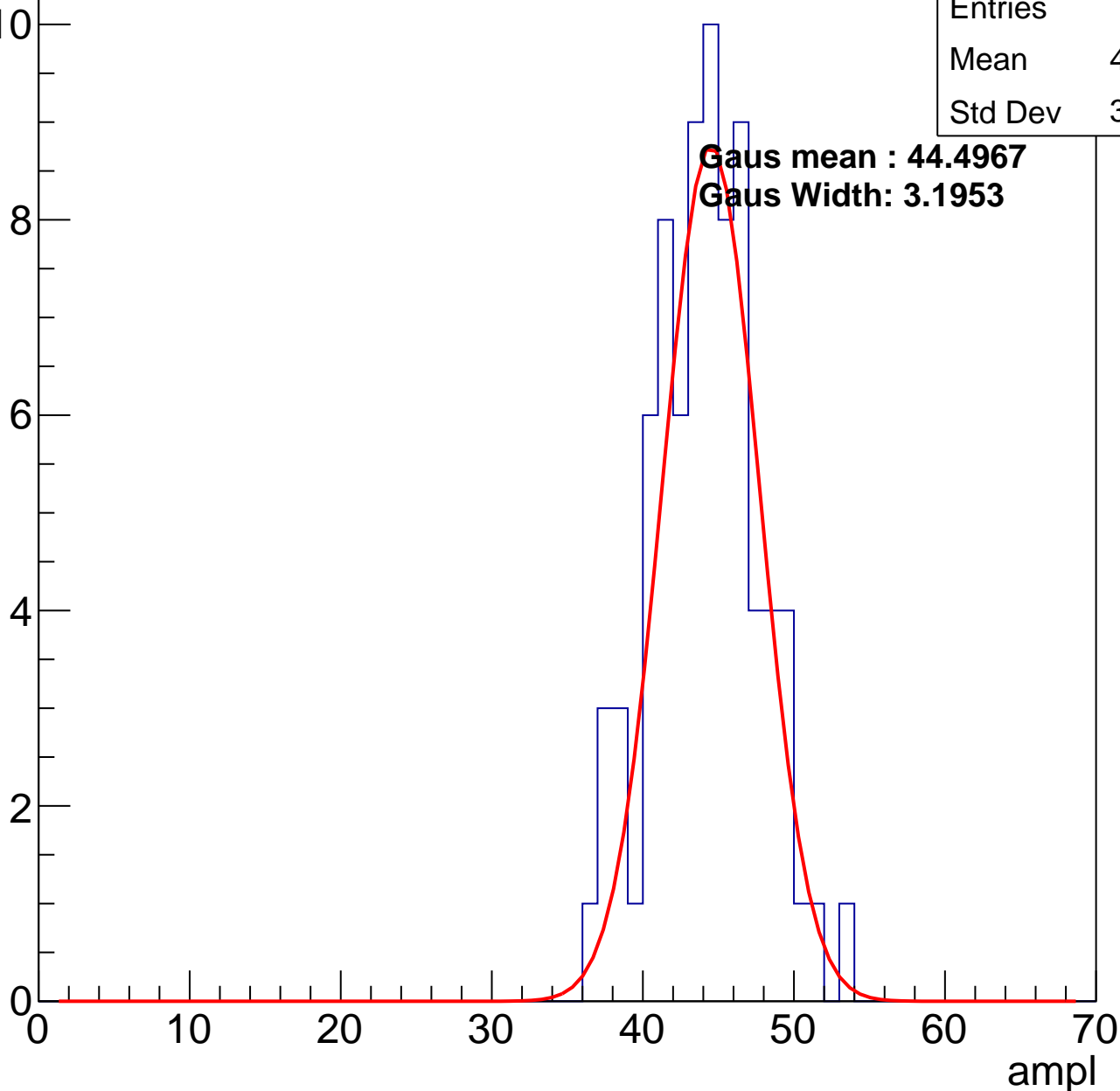
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 79    |
| Mean    | 43.68 |
| Std Dev | 3.462 |

**Gaus mean : 44.4967**

**Gaus Width: 3.1953**

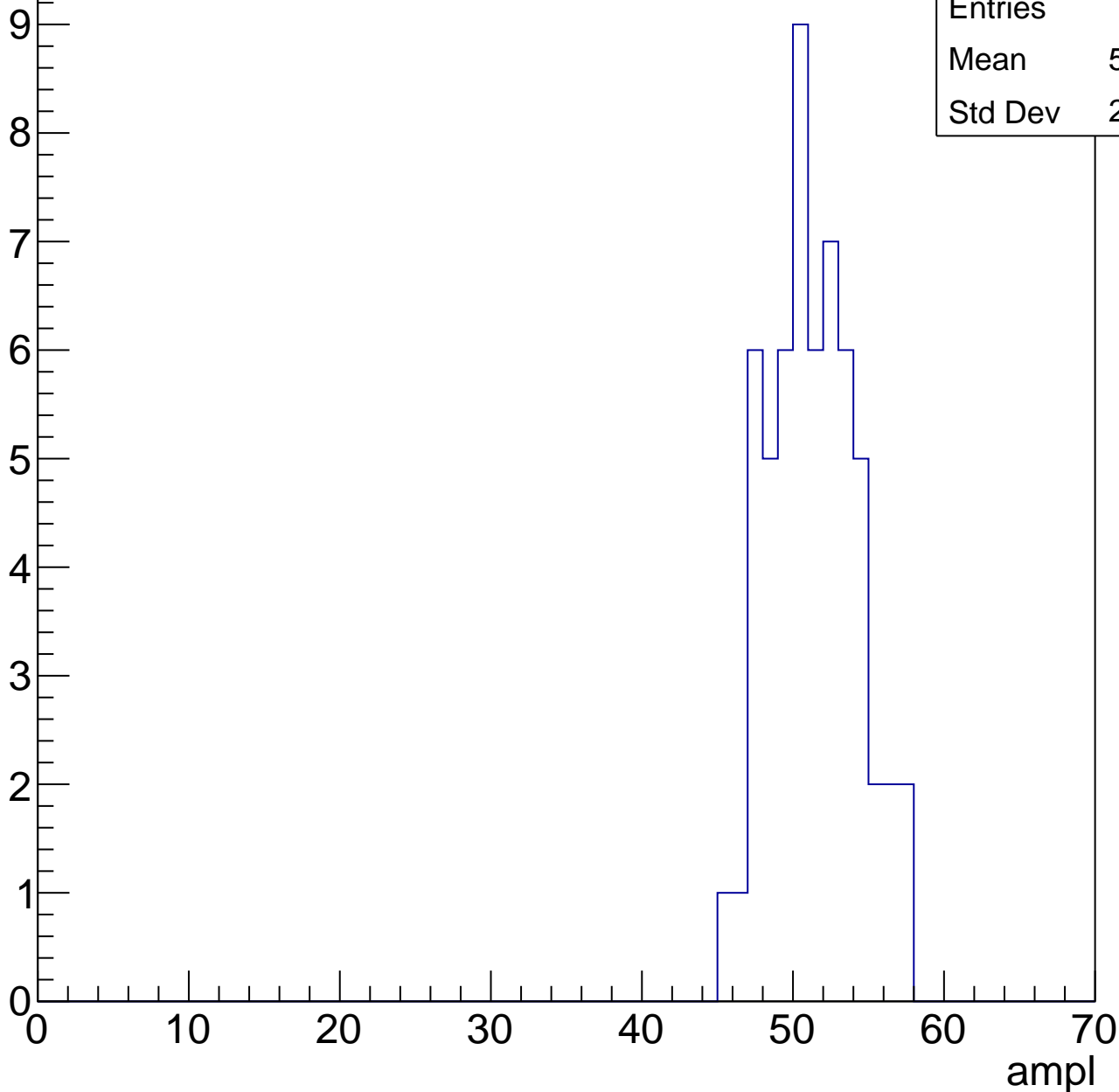


# B0L001S, U2-ch24, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 58    |
| Mean    | 50.88 |
| Std Dev | 2.829 |

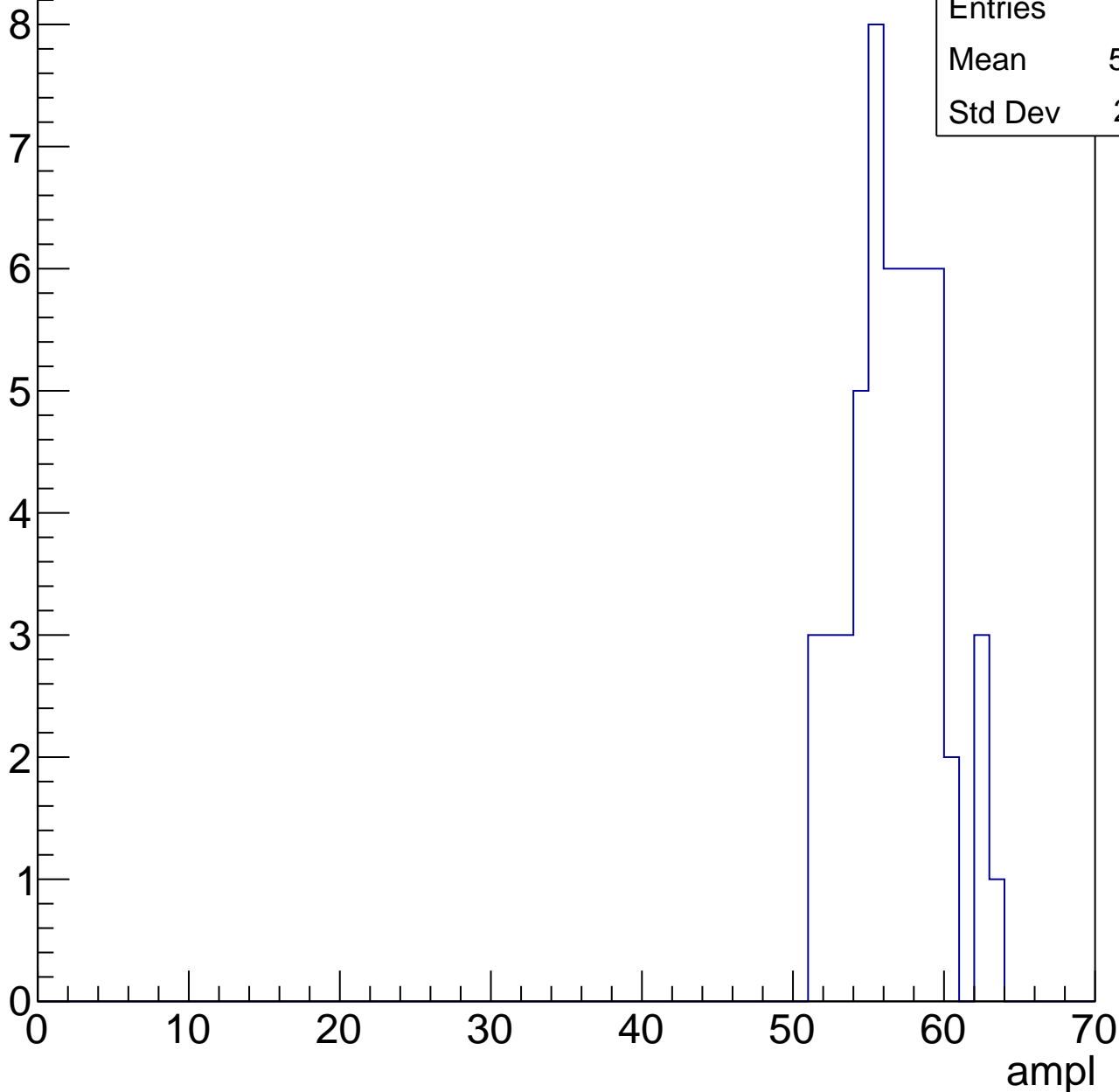


# B0L001S, U2-ch24, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 52    |
| Mean    | 56.29 |
| Std Dev | 2.931 |

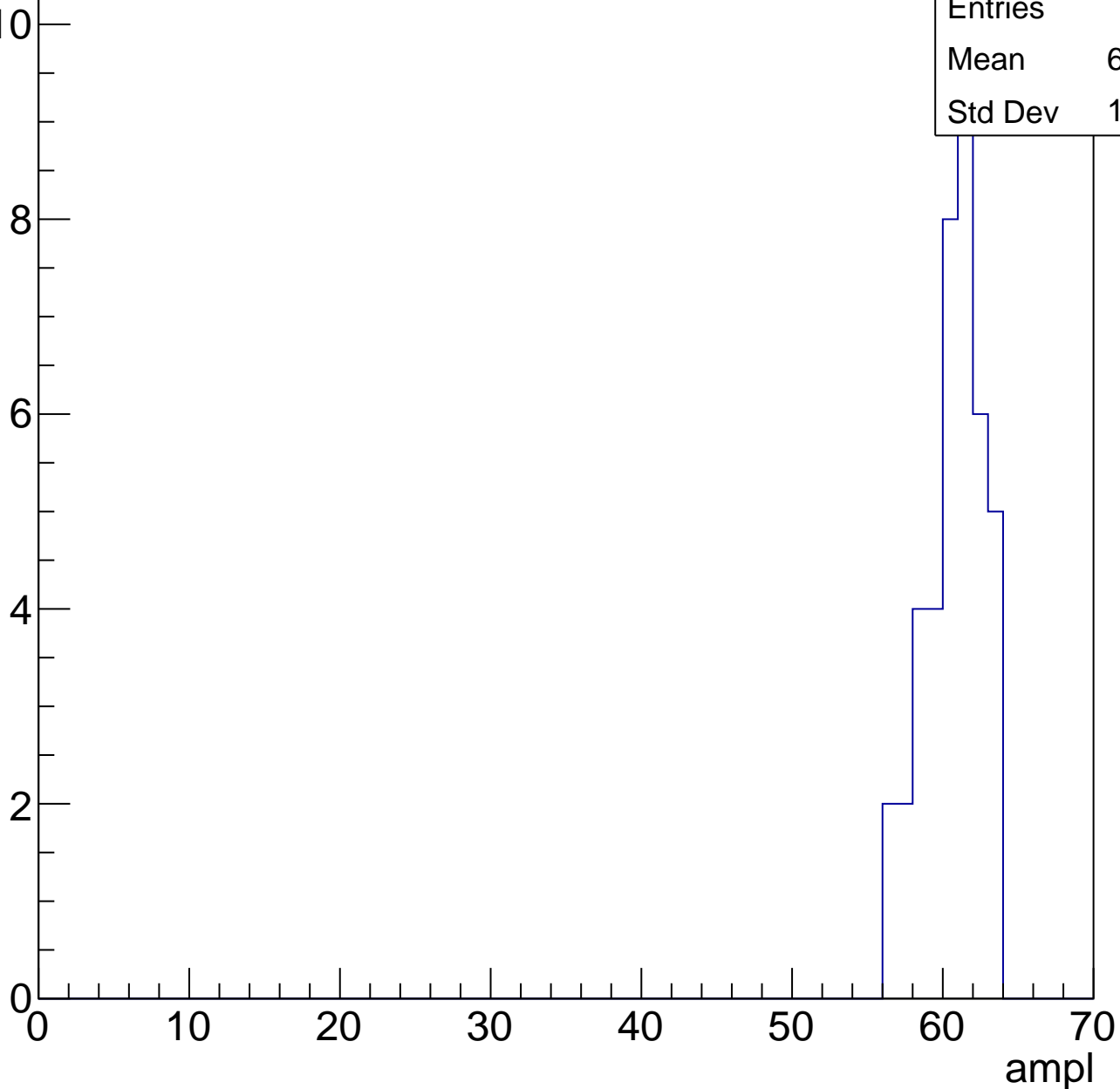


# B0L001S, U2-ch24, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

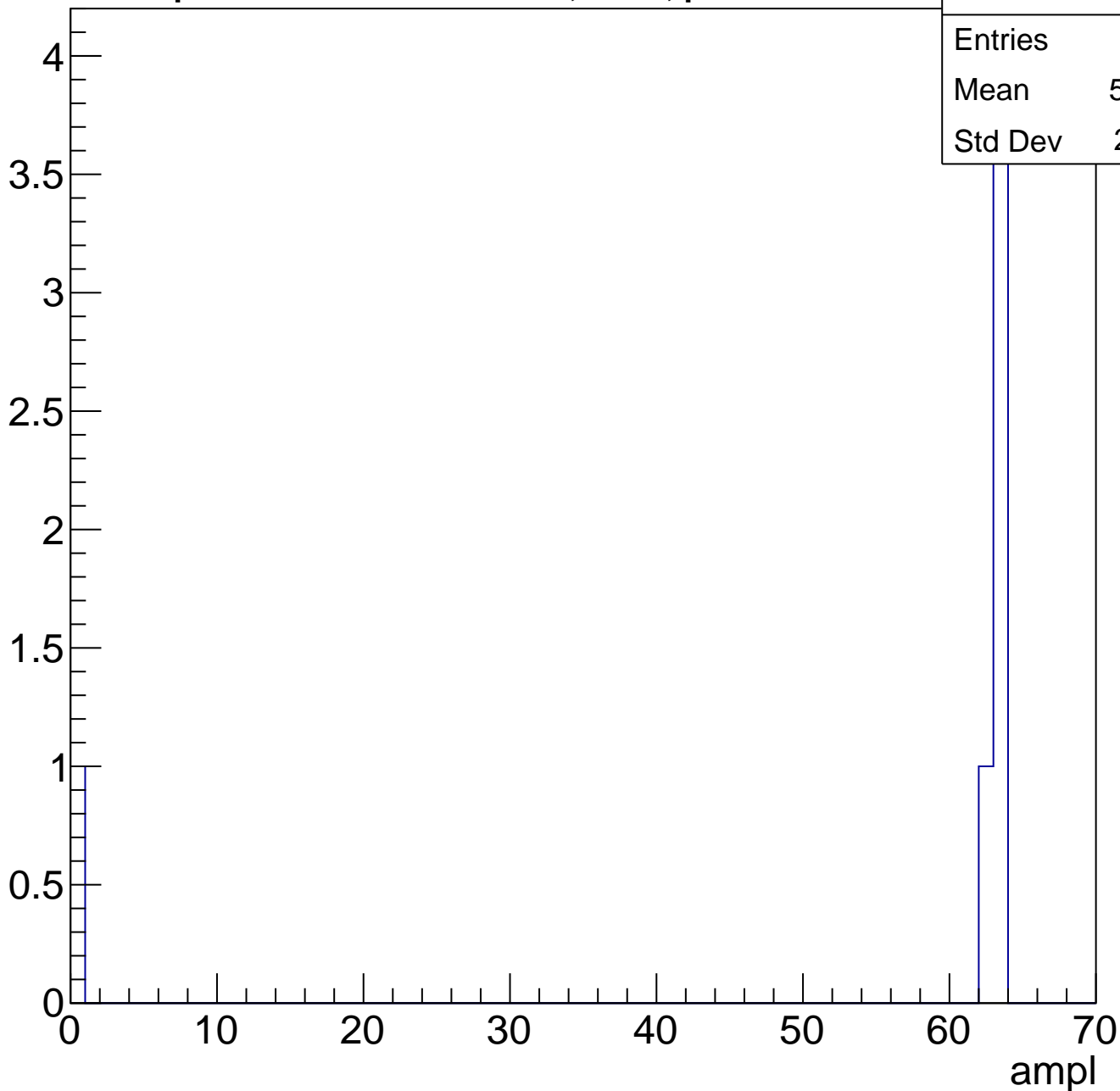
|         |       |
|---------|-------|
| Entries | 41    |
| Mean    | 60.27 |
| Std Dev | 1.887 |



# B0L001S, U2-ch24, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch24, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 1 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch25, adc0

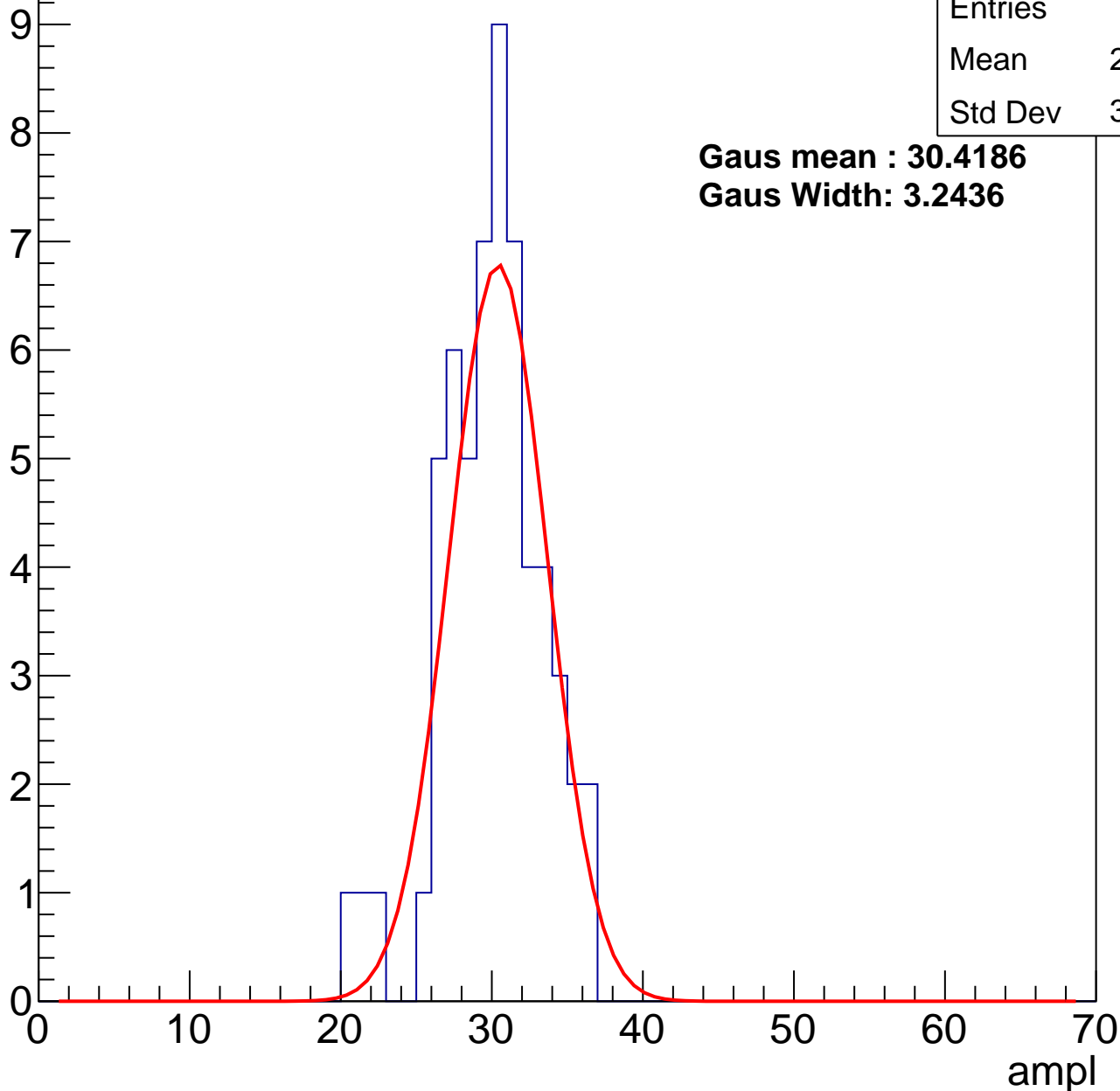
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 58    |
| Mean    | 29.55 |
| Std Dev | 3.343 |

**Gaus mean : 30.4186**

**Gaus Width: 3.2436**



# B0L001S, U2-ch25, adc1

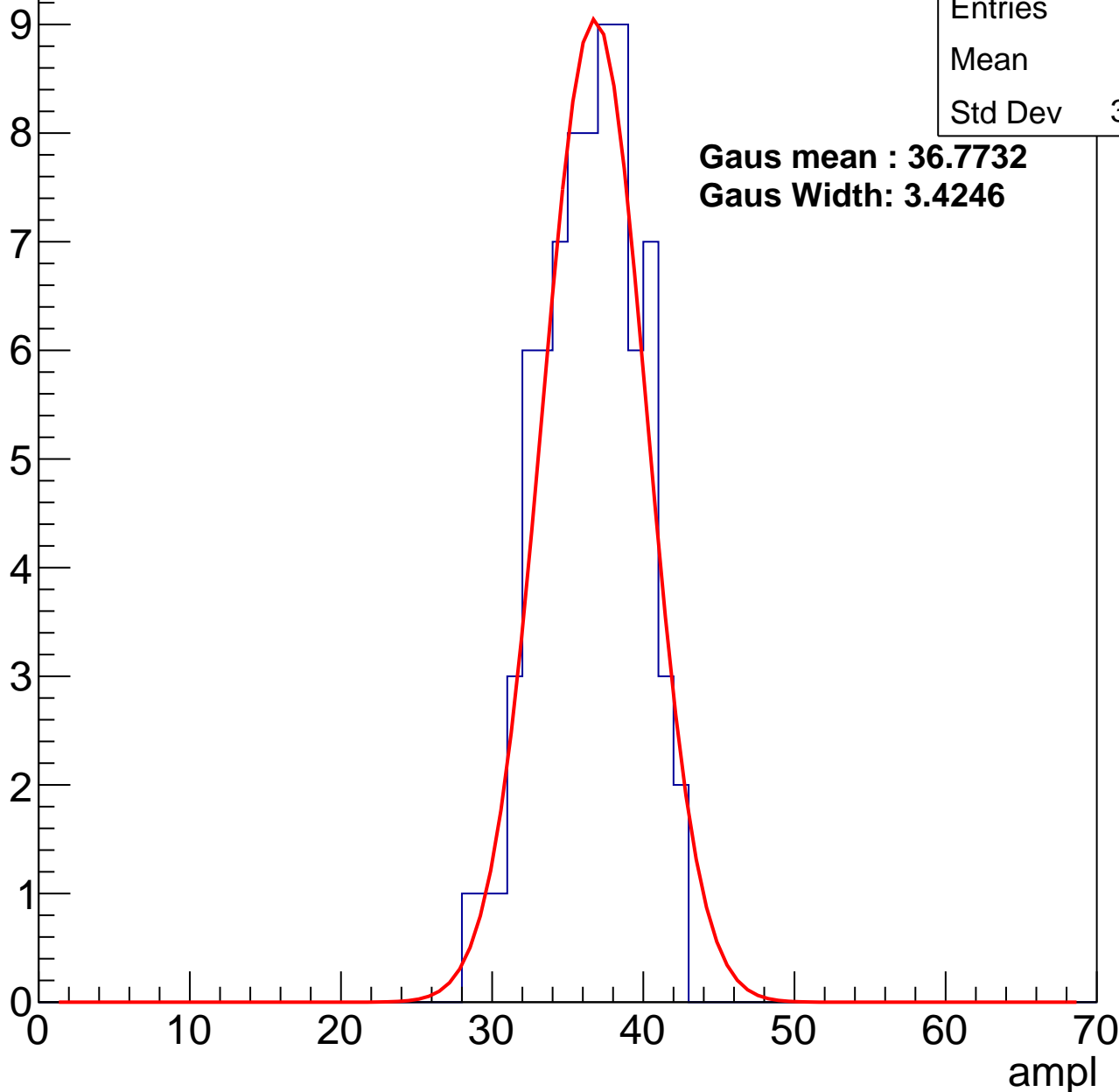
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 77    |
| Mean    | 36    |
| Std Dev | 3.158 |

**Gaus mean : 36.7732**

**Gaus Width: 3.4246**



# B0L001S, U2-ch25, adc2

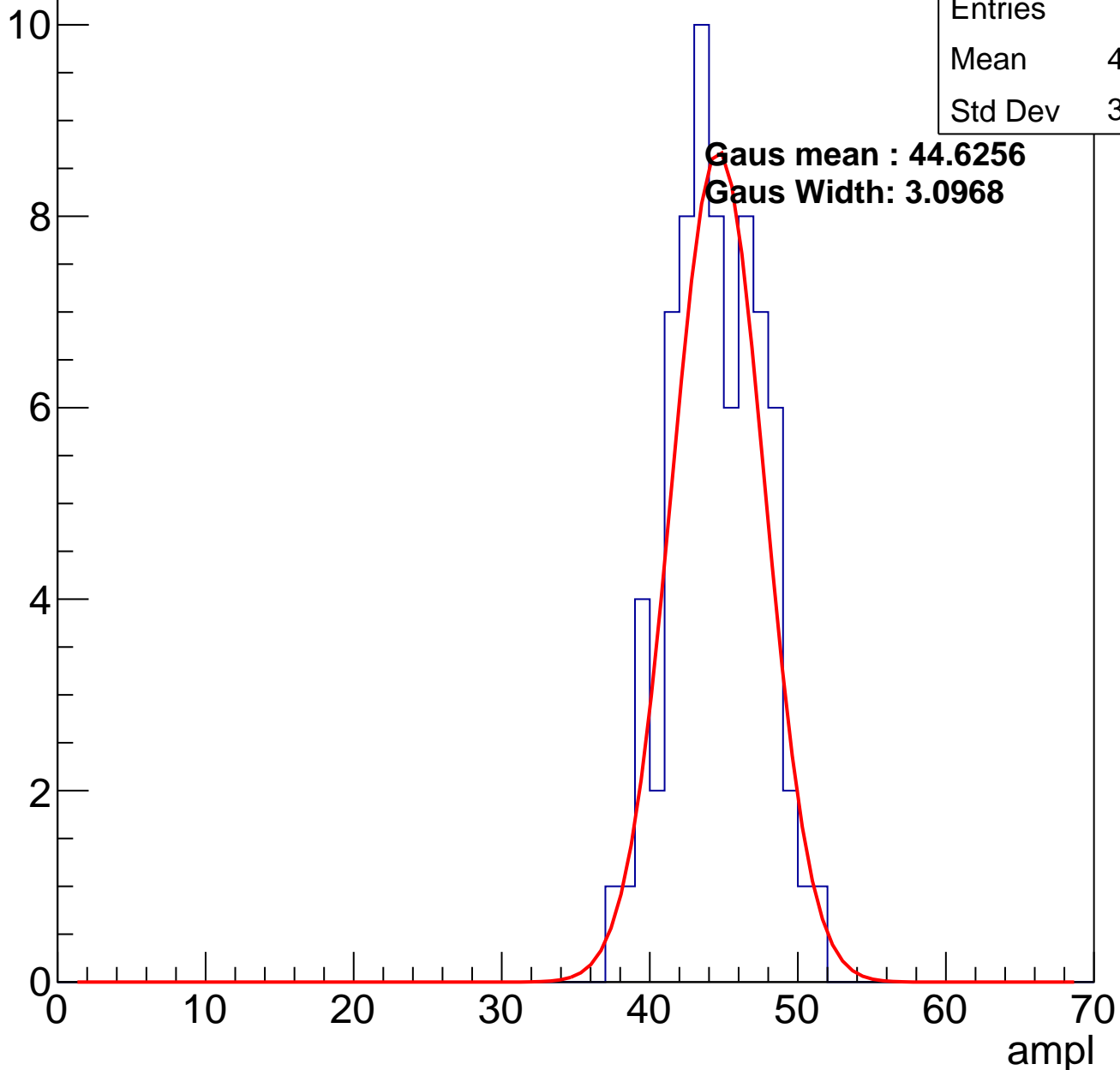
calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 72    |
| Mean    | 44.03 |
| Std Dev | 3.014 |

**Gaus mean : 44.6256**

**Gaus Width: 3.0968**

Entry

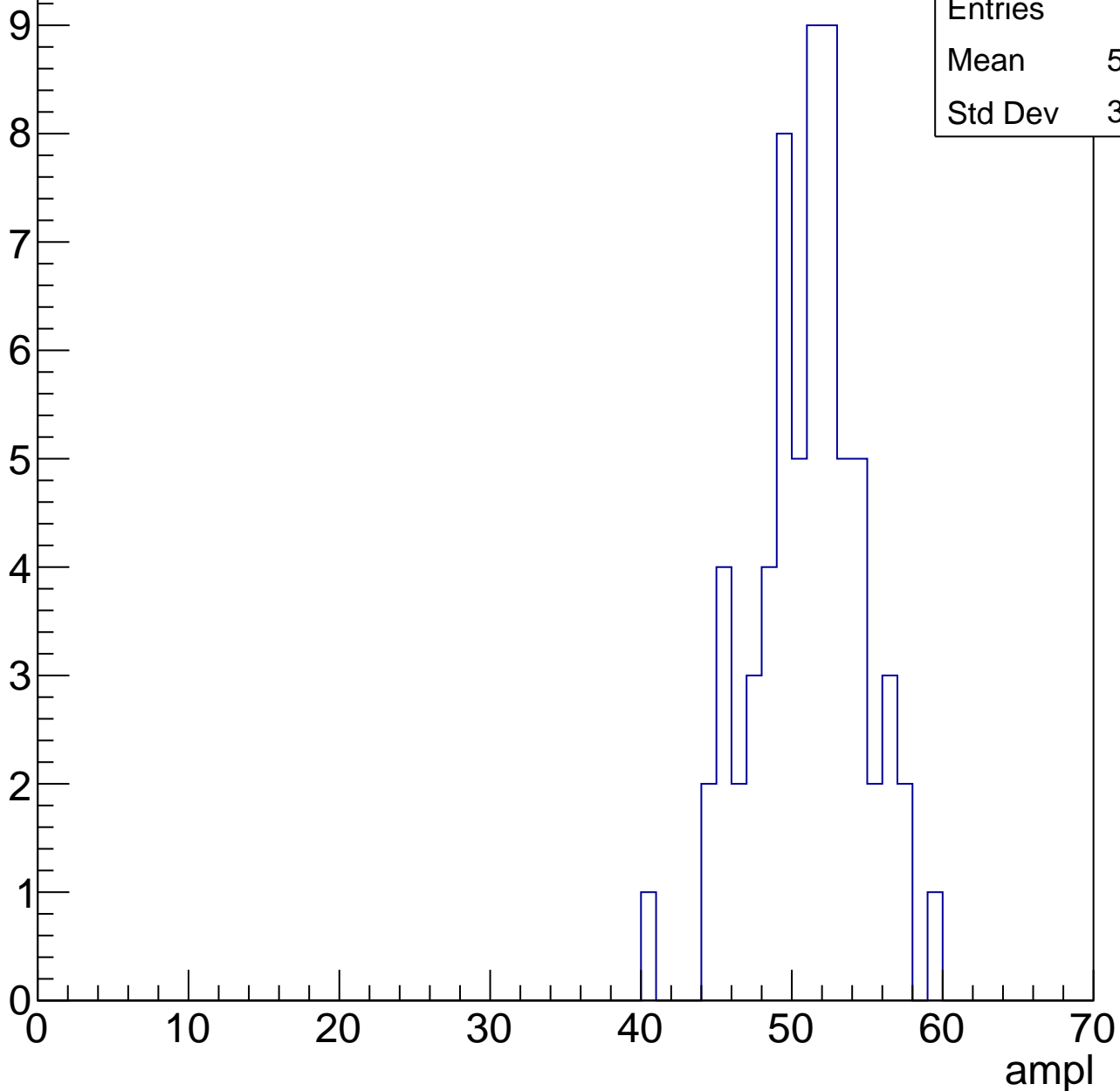


# B0L001S, U2-ch25, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 65    |
| Mean    | 50.58 |
| Std Dev | 3.594 |

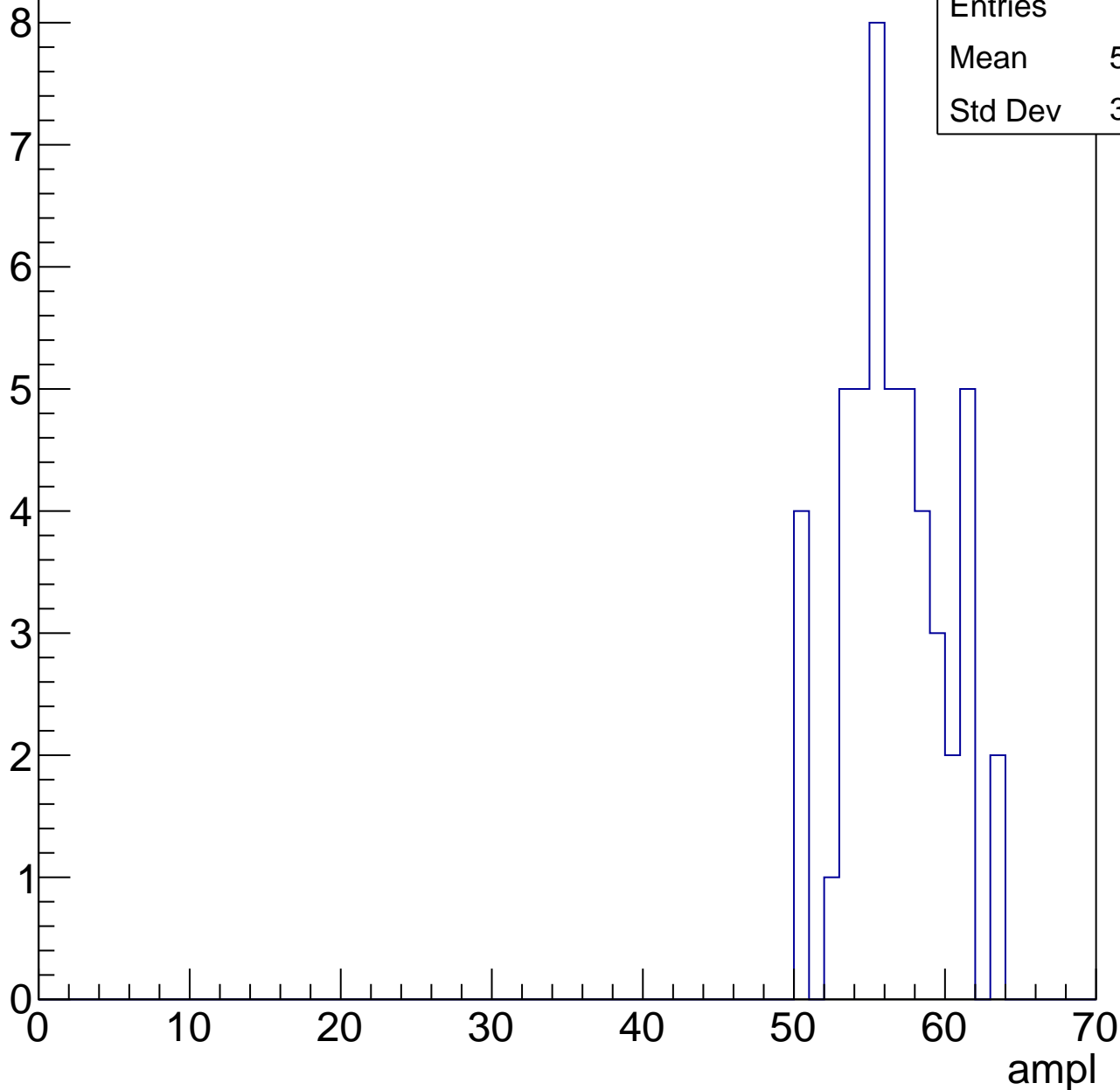


# B0L001S, U2-ch25, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 49    |
| Mean    | 56.16 |
| Std Dev | 3.303 |



# B0L001S, U2-ch25, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

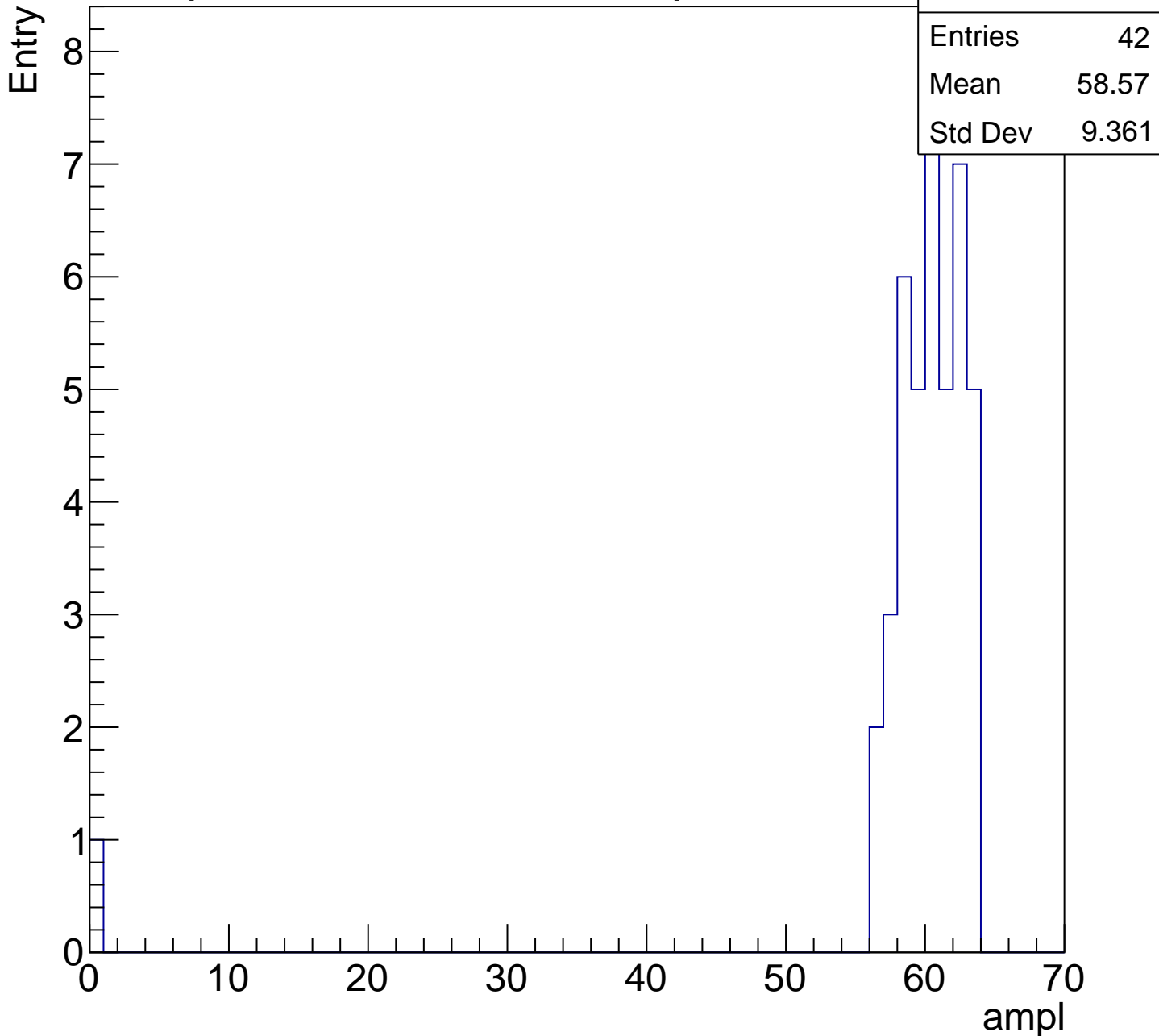
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

|         |       |
|---------|-------|
| Entries | 42    |
| Mean    | 58.57 |
| Std Dev | 9.361 |

ampl

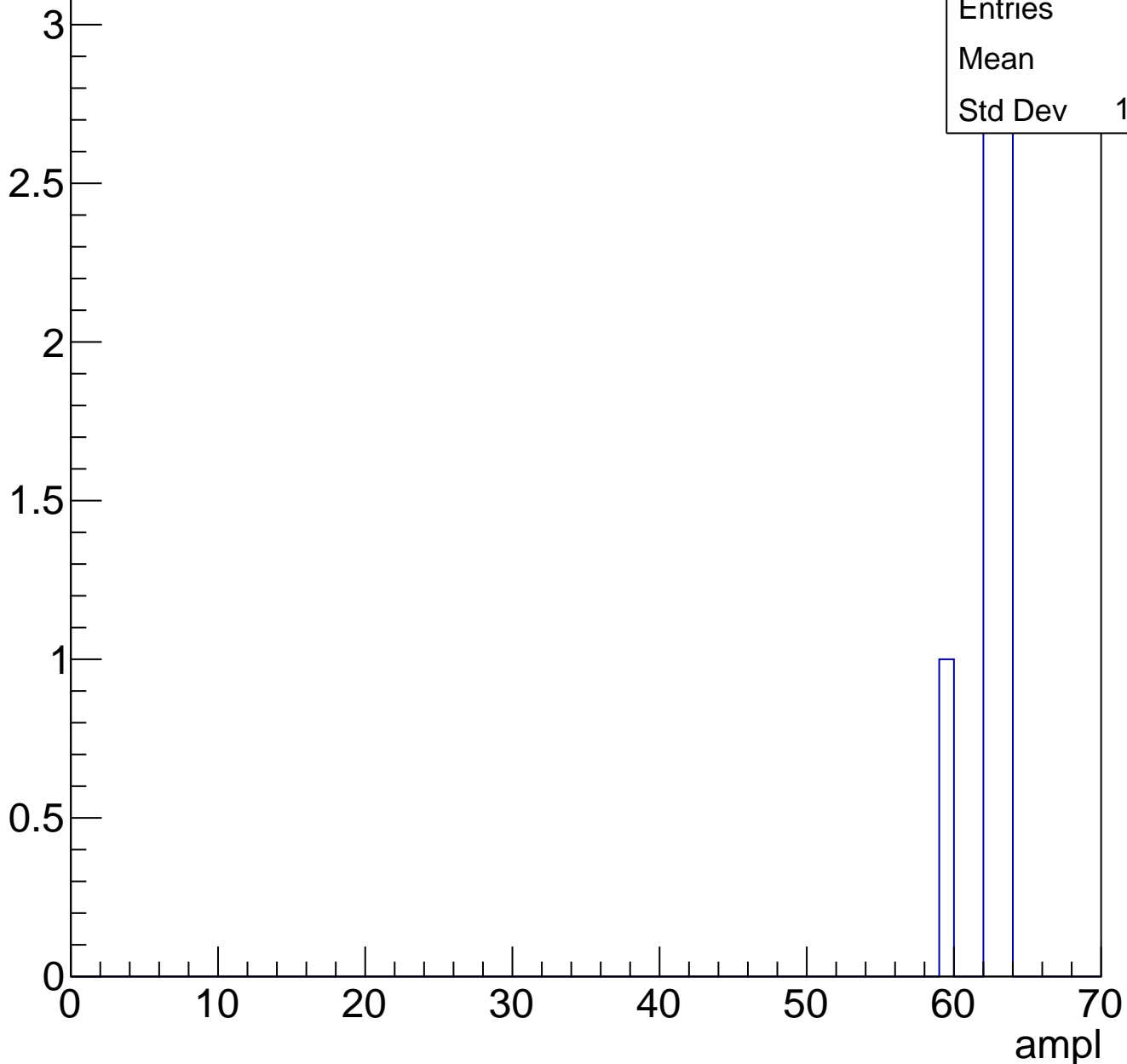
0 10 20 30 40 50 60 70



# B0L001S, U2-ch25, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch25, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 0 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch26, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 70    |
| Mean    | 29.61 |
| Std Dev | 3.322 |

**Gaus mean : 29.9606**

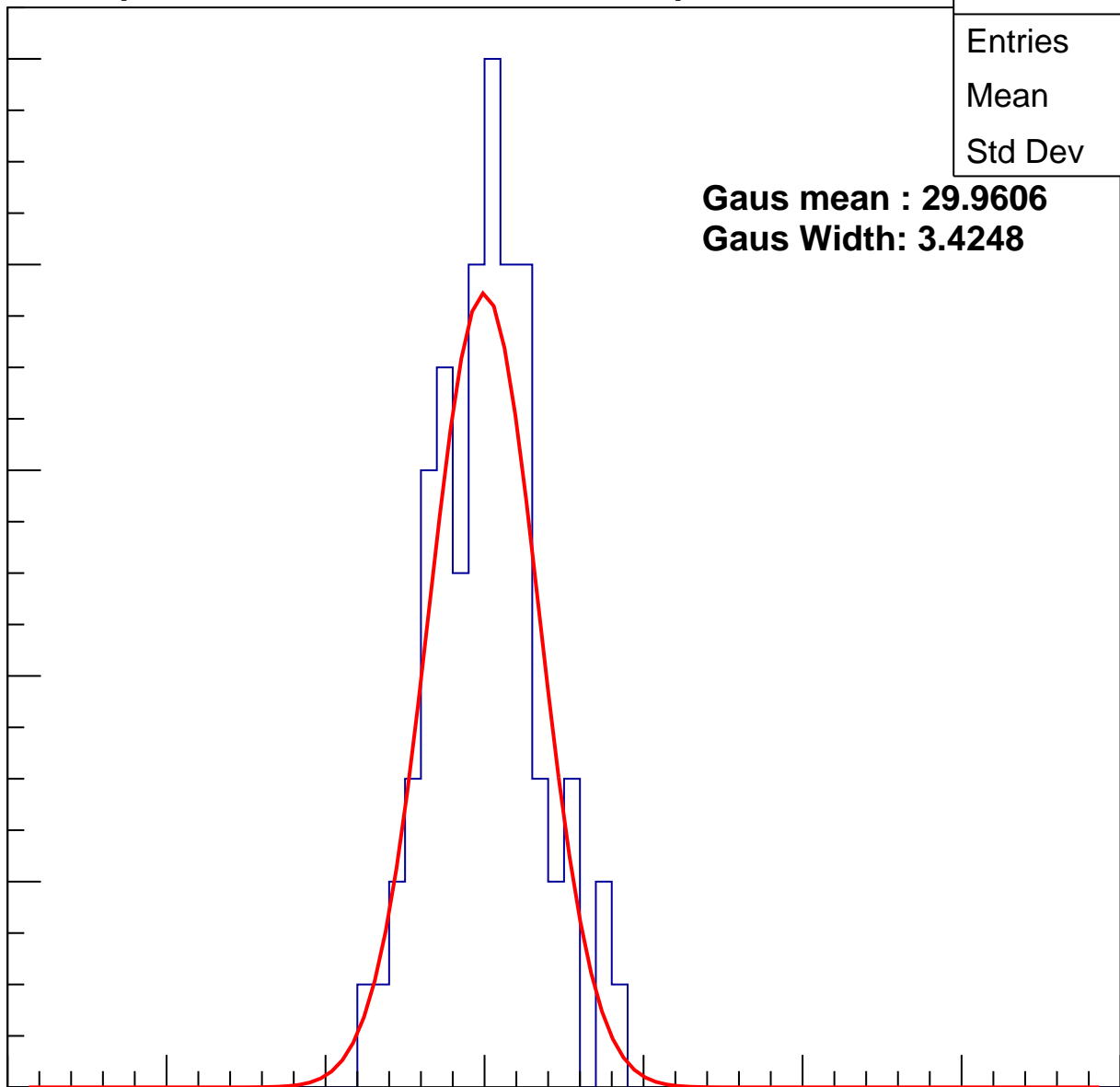
**Gaus Width: 3.4248**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U2-ch26, adc1

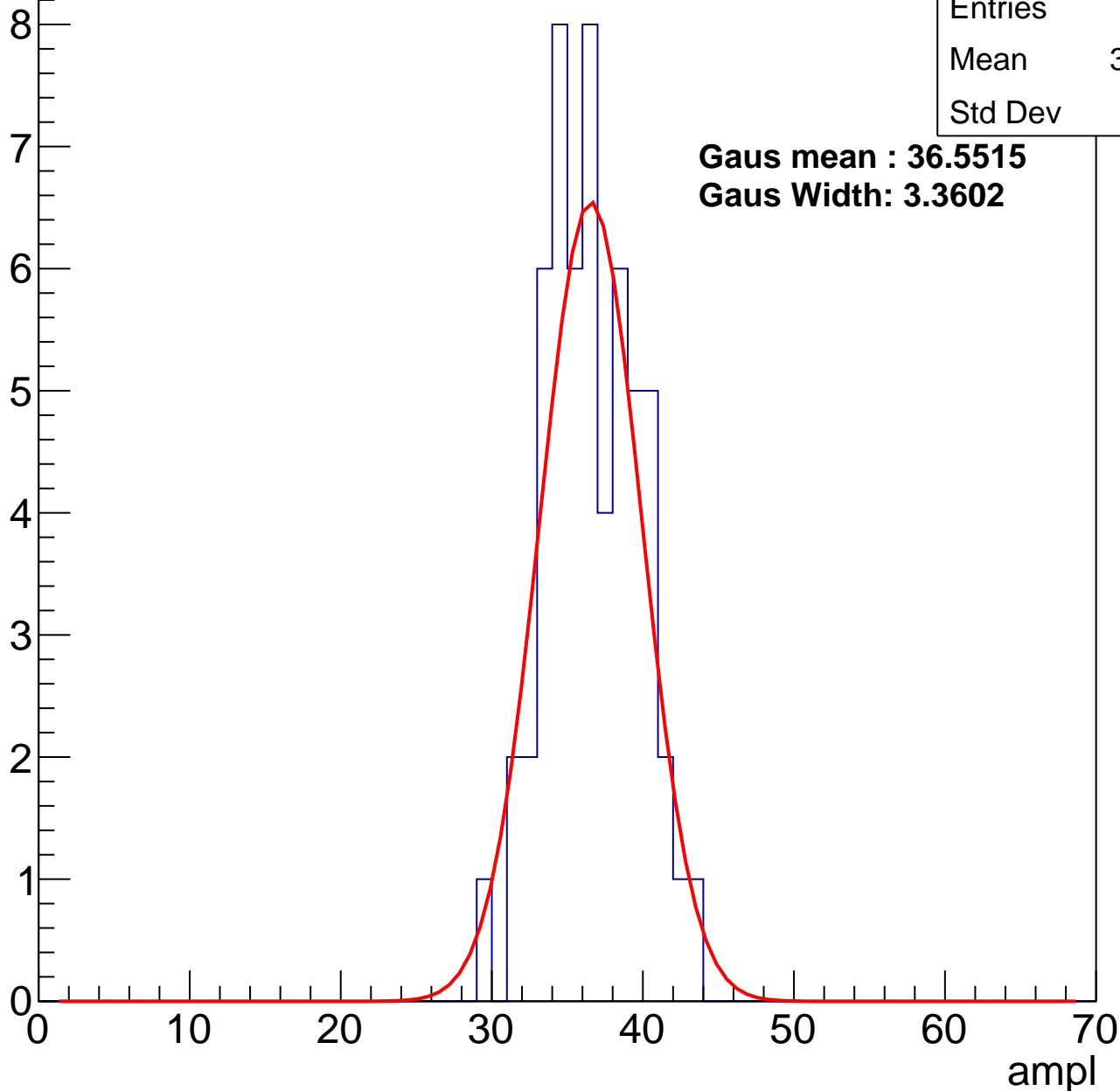
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 57    |
| Mean    | 36.16 |
| Std Dev | 2.99  |

**Gaus mean : 36.5515**

**Gaus Width: 3.3602**



# B0L001S, U2-ch26, adc2

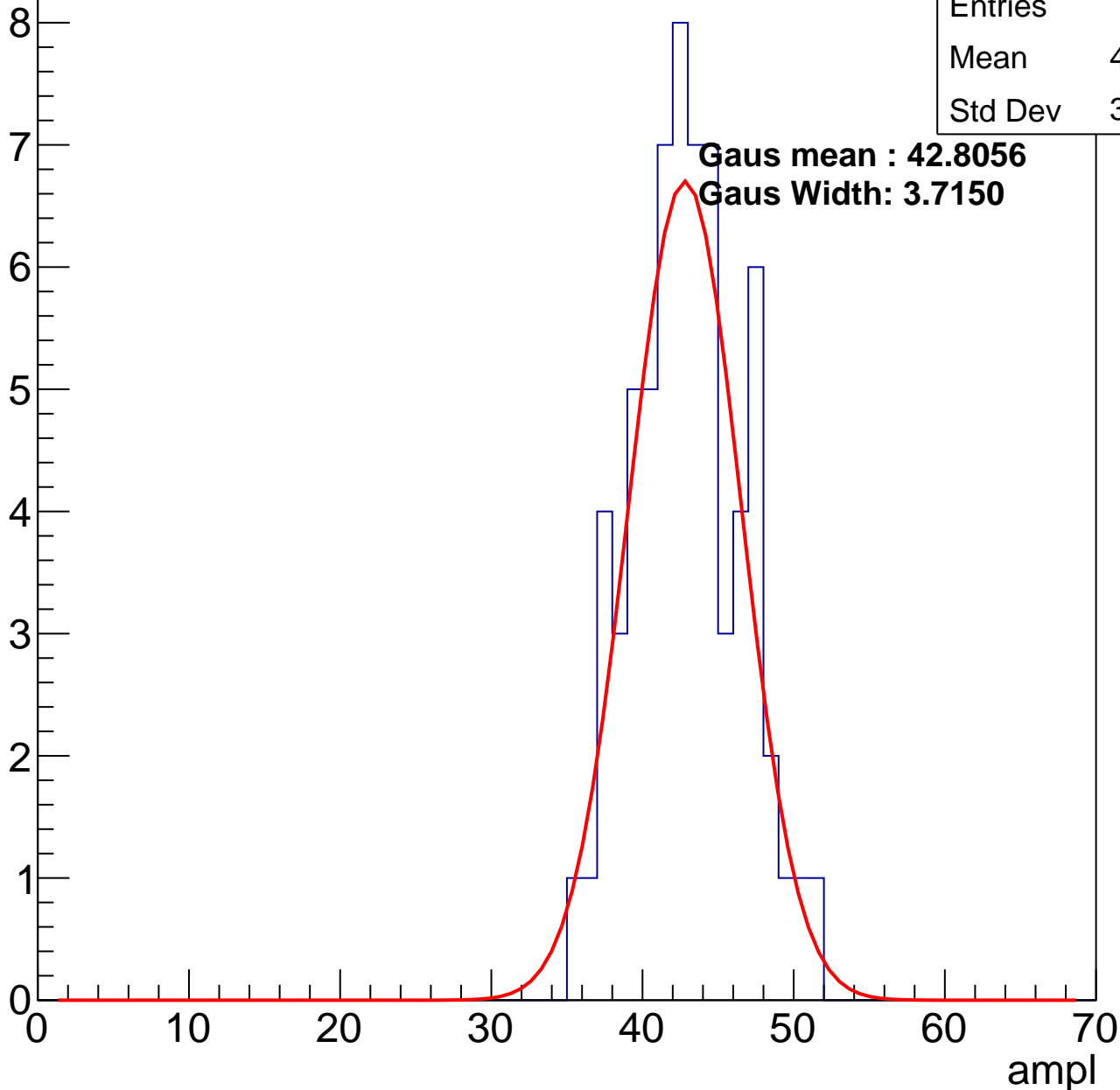
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 66    |
| Mean    | 42.53 |
| Std Dev | 3.543 |

**Gaus mean : 42.8056**

**Gaus Width: 3.7150**

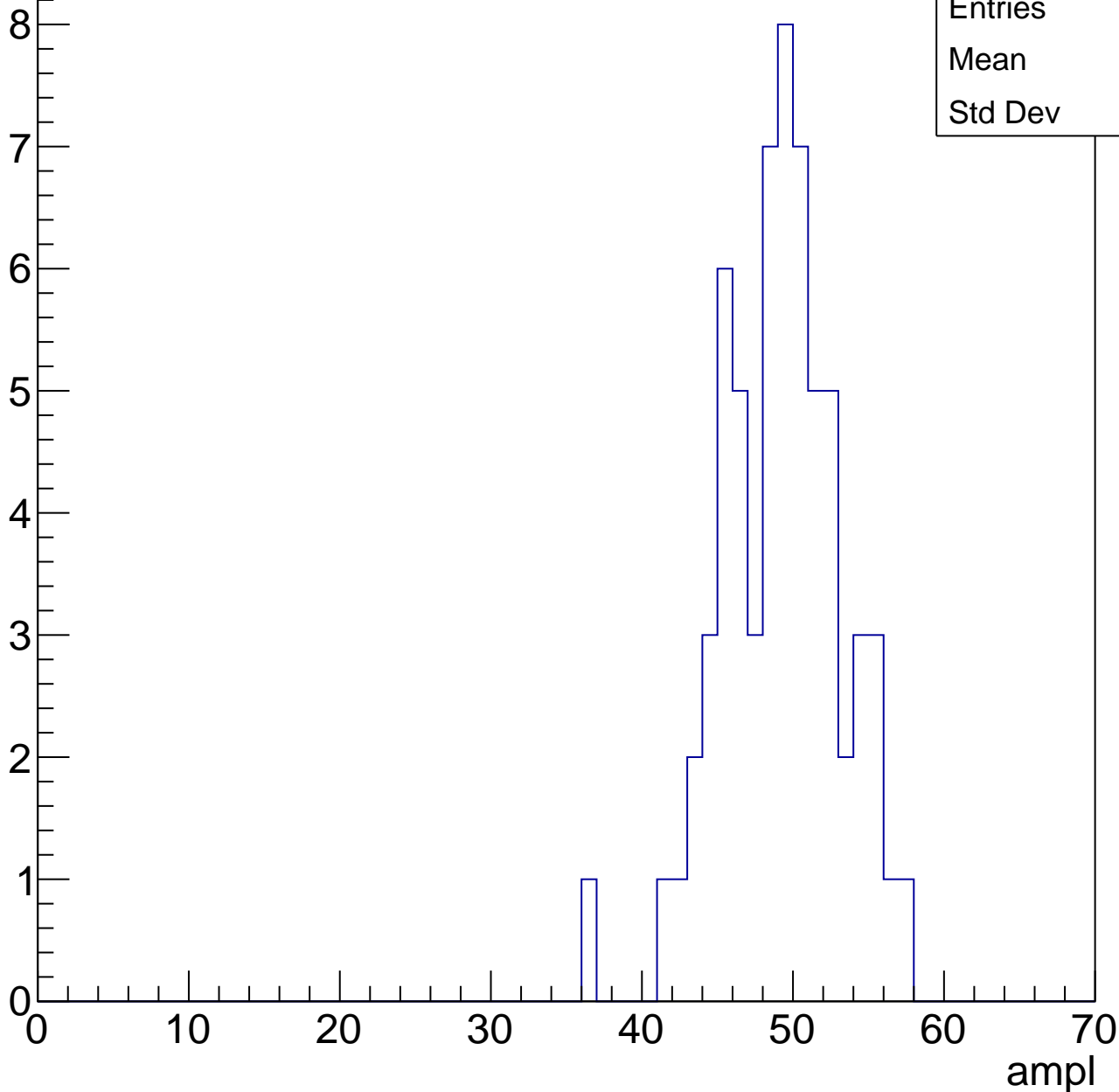


# B0L001S, U2-ch26, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |      |
|---------|------|
| Entries | 64   |
| Mean    | 48.7 |
| Std Dev | 3.92 |



# B0L001S, U2-ch26, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 70    |
| Mean    | 55.11 |
| Std Dev | 3.748 |

Entry

10

8

6

4

2

0

0

10

20

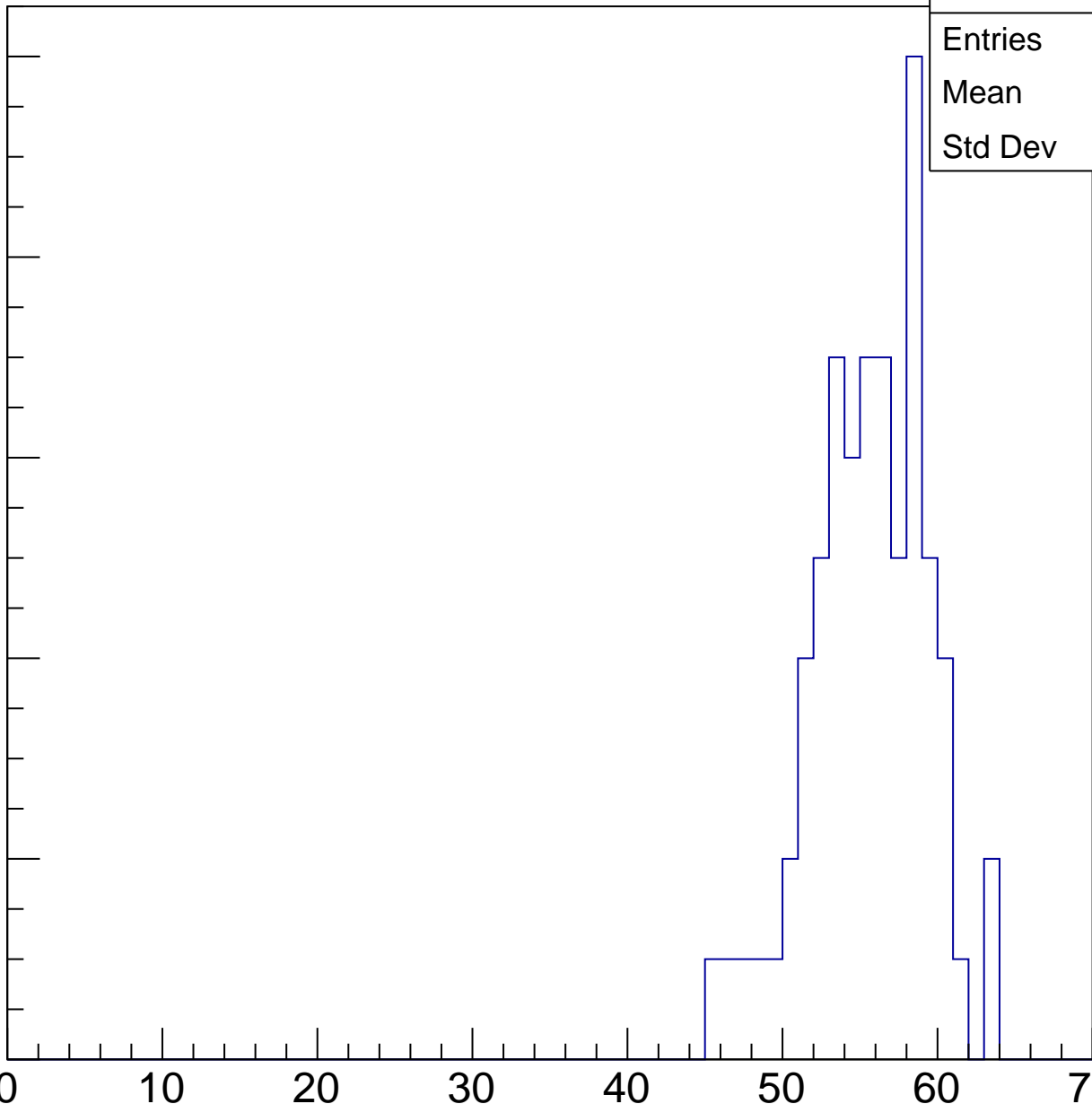
30

40

50

60

ampl

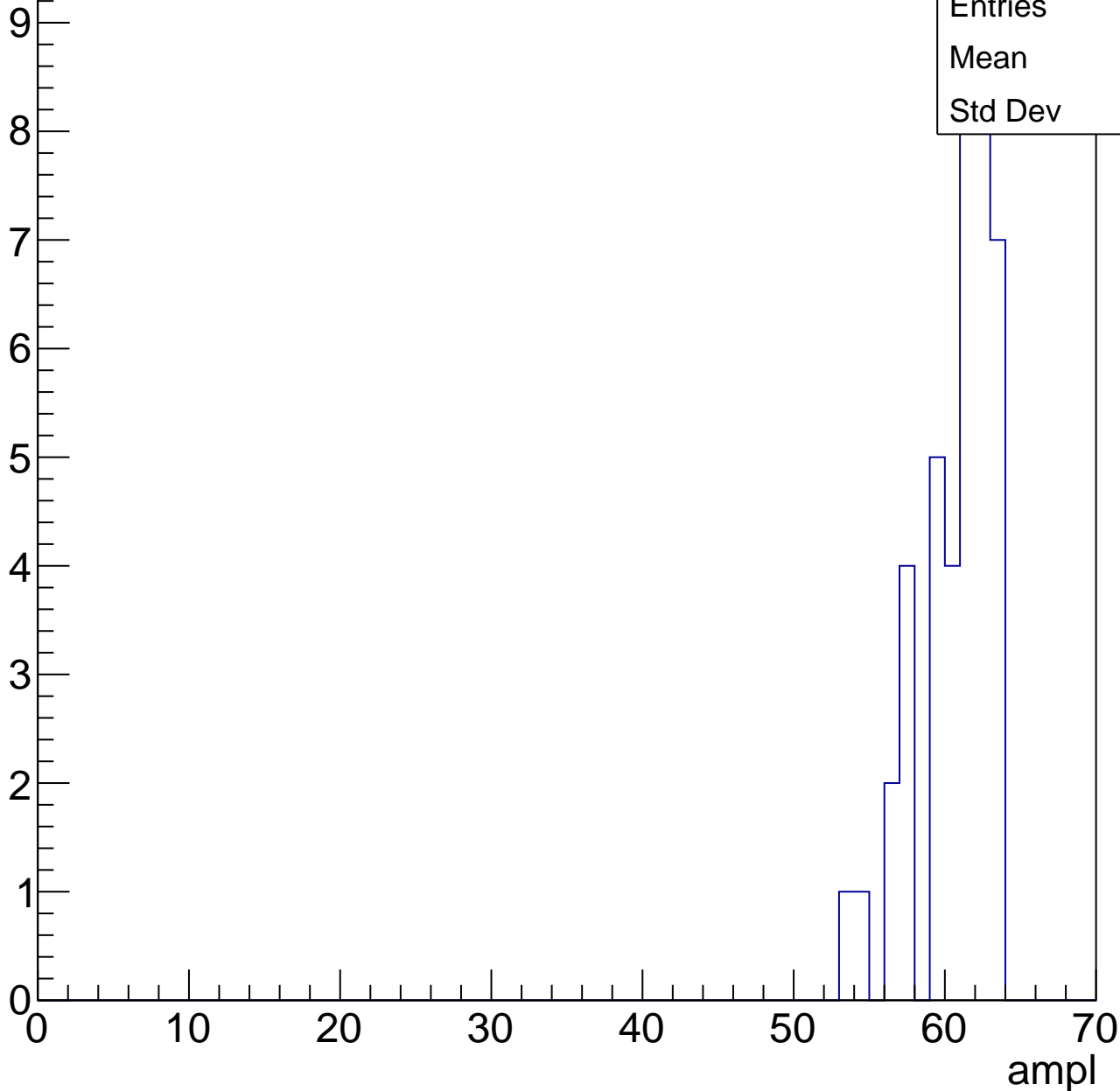


# B0L001S, U2-ch26, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |      |
|---------|------|
| Entries | 41   |
| Mean    | 60.2 |
| Std Dev | 2.52 |



# B0L001S, U2-ch26, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

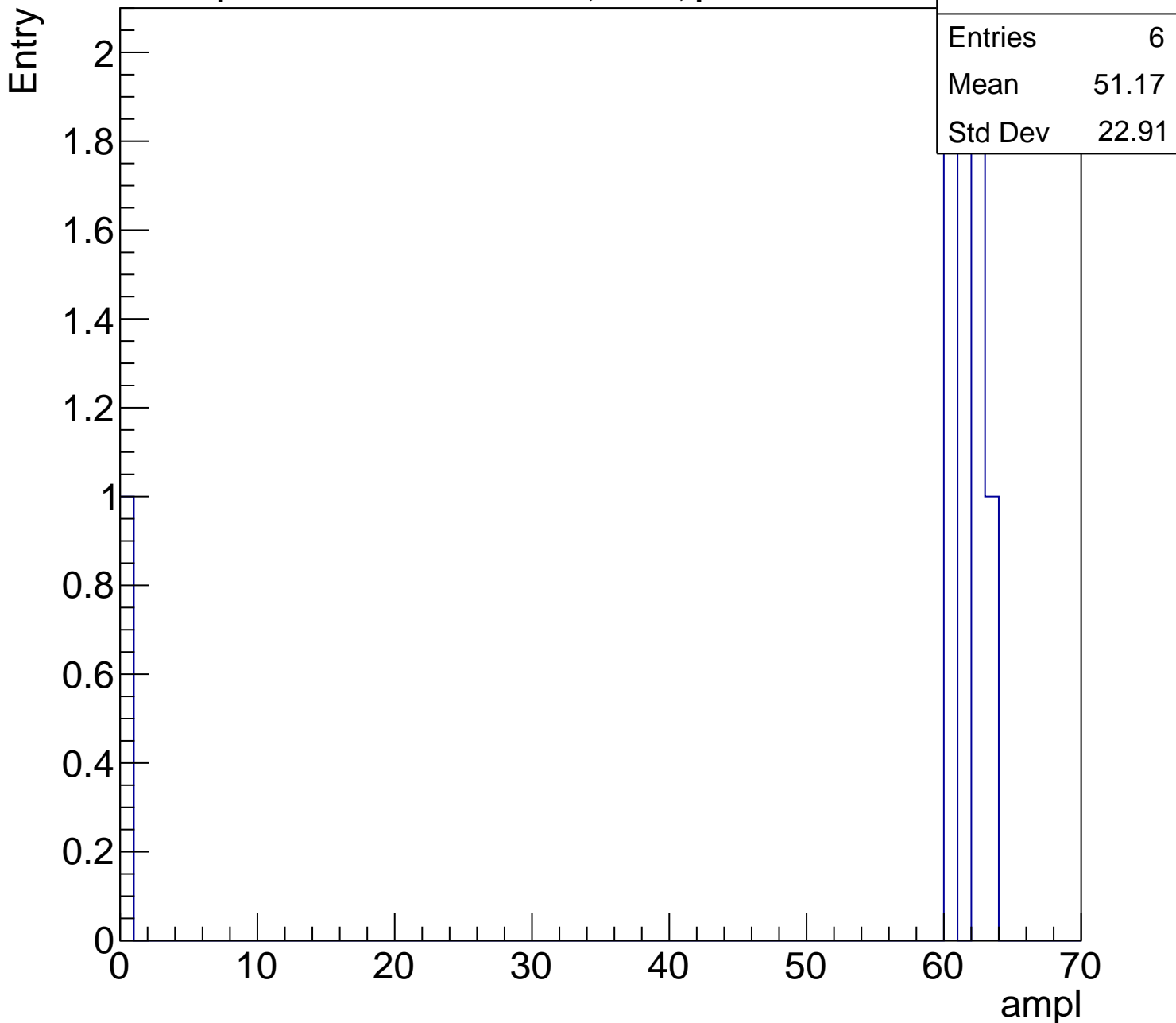
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

|         |       |
|---------|-------|
| Entries | 6     |
| Mean    | 51.17 |
| Std Dev | 22.91 |

0 10 20 30 40 50 60 70

ampl





# B0L001S, U2-ch26, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 1 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch27, adc0

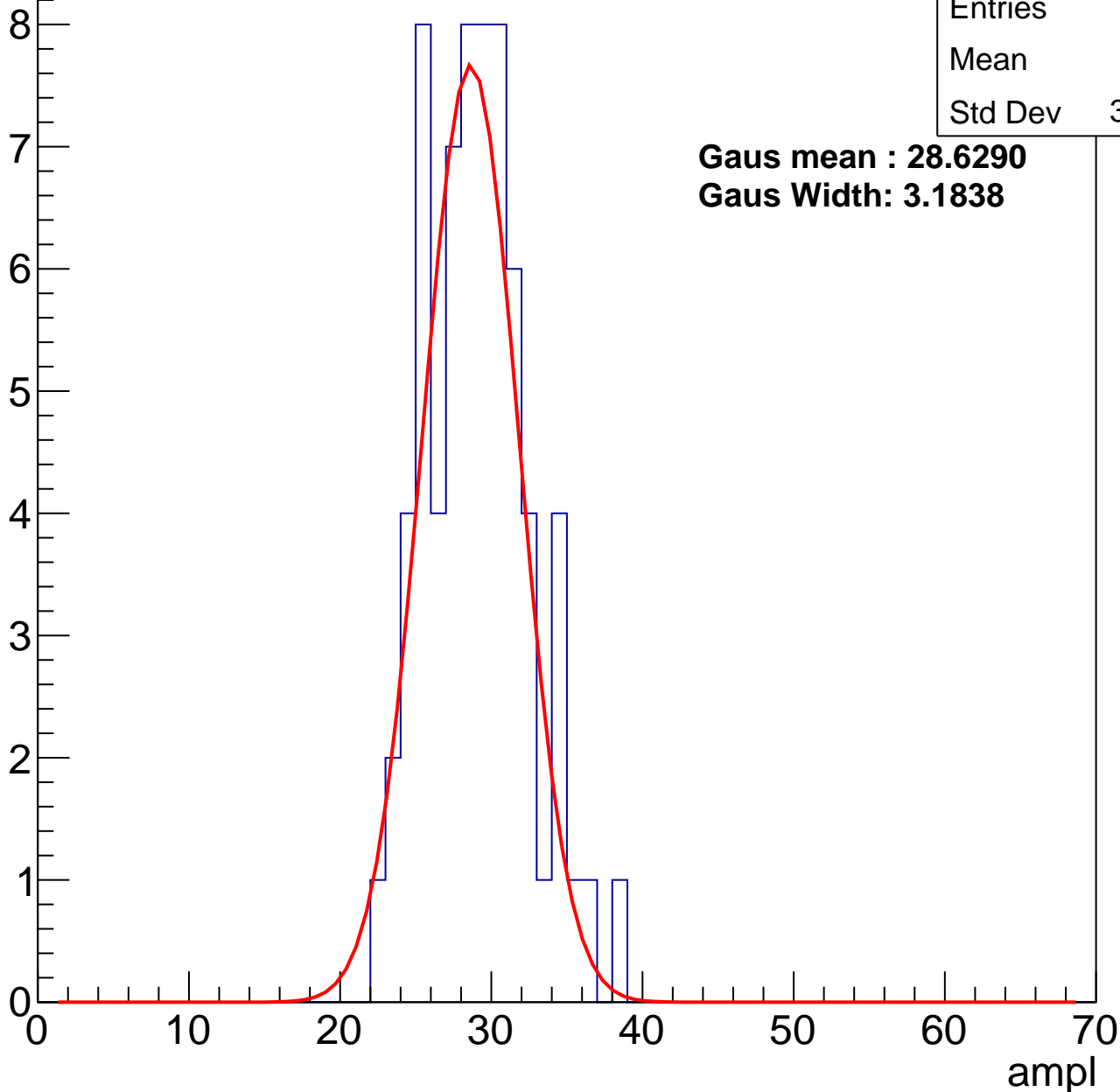
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 68    |
| Mean    | 28.6  |
| Std Dev | 3.344 |

**Gaus mean : 28.6290**

**Gaus Width: 3.1838**



# B0L001S, U2-ch27, adc1

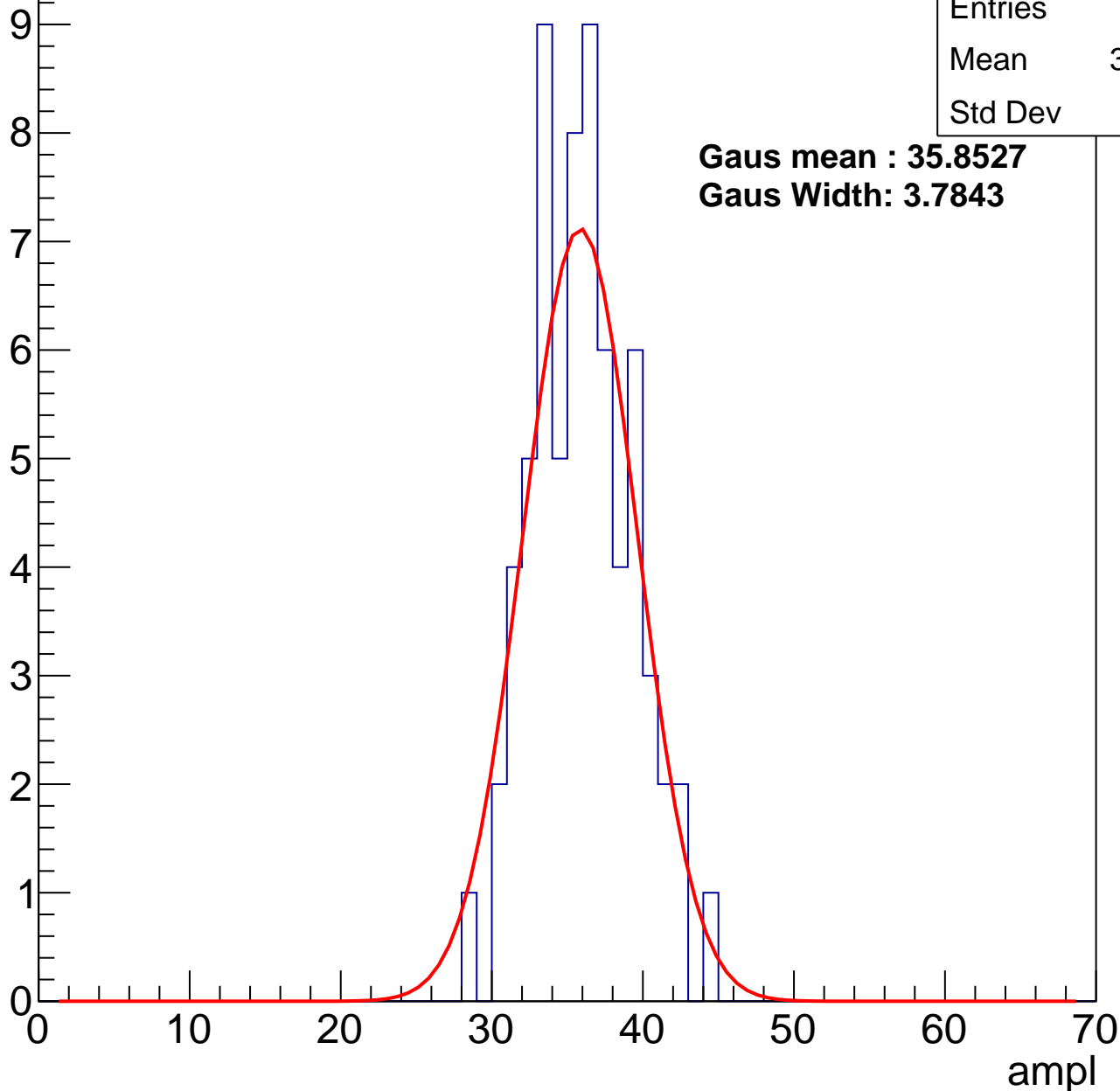
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 67    |
| Mean    | 35.54 |
| Std Dev | 3.28  |

**Gaus mean : 35.8527**

**Gaus Width: 3.7843**



# B0L001S, U2-ch27, adc2

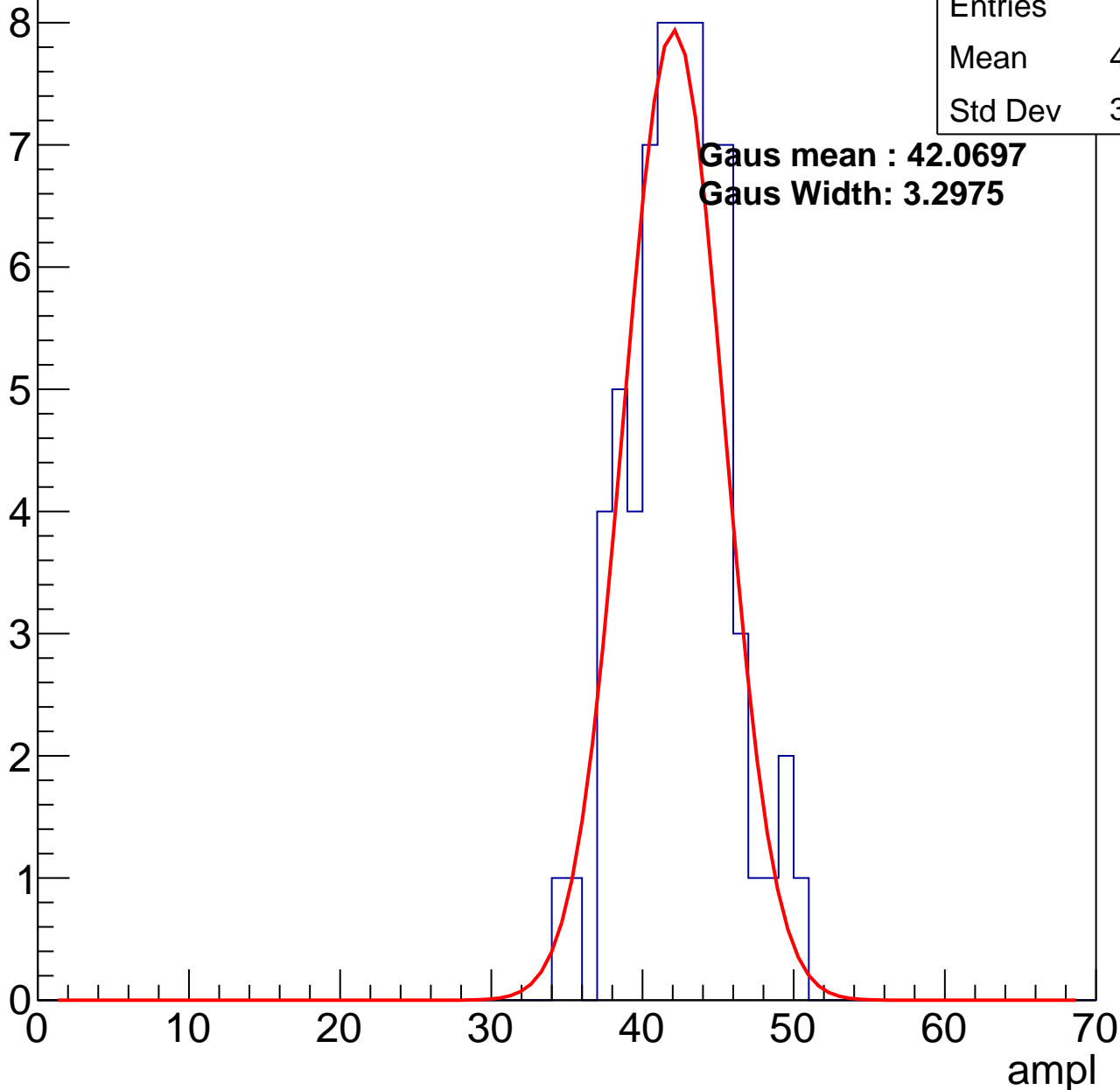
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 68    |
| Mean    | 41.99 |
| Std Dev | 3.288 |

**Gaus mean : 42.0697**

**Gaus Width: 3.2975**

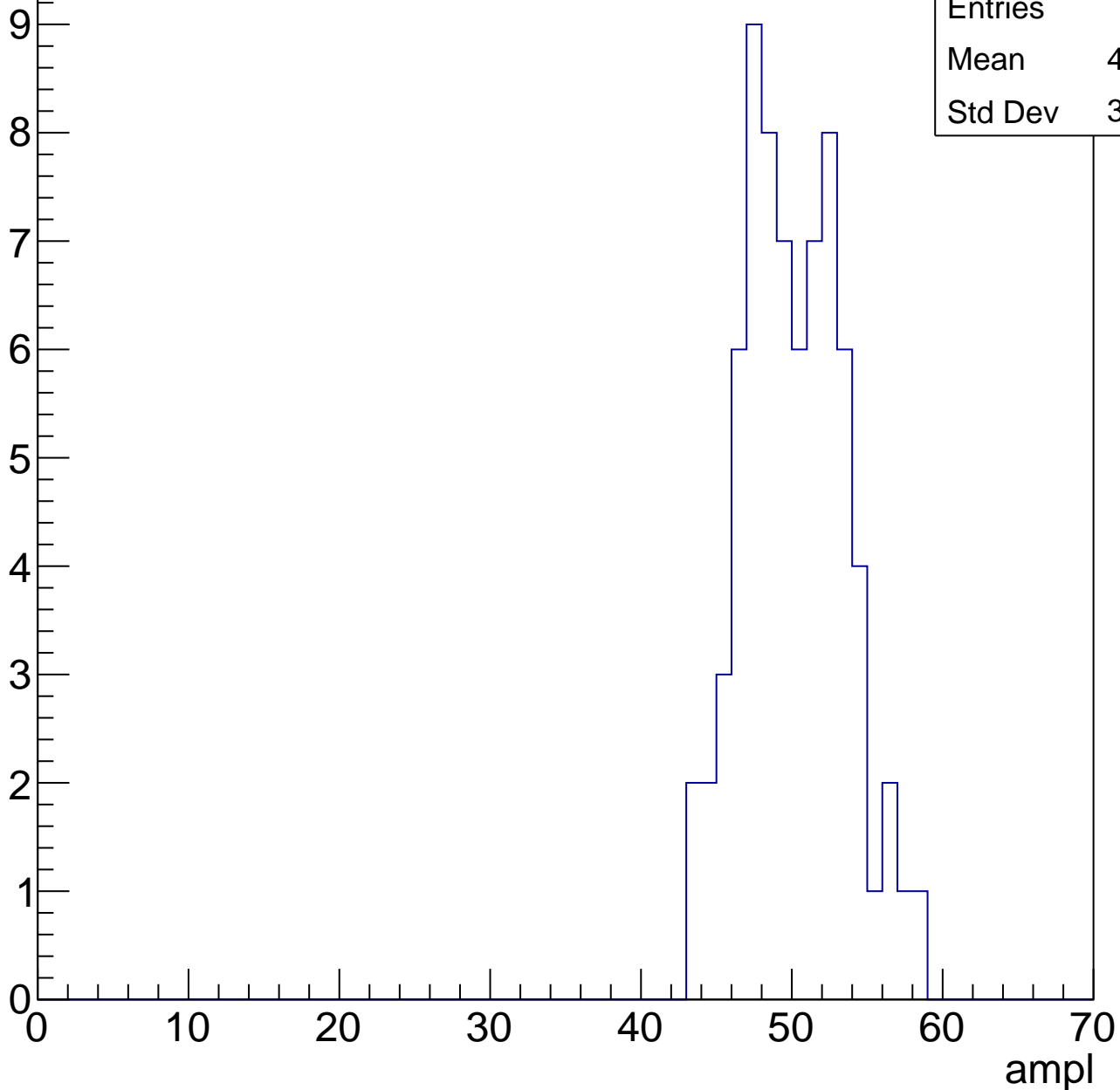


# B0L001S, U2-ch27, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 73    |
| Mean    | 49.64 |
| Std Dev | 3.349 |

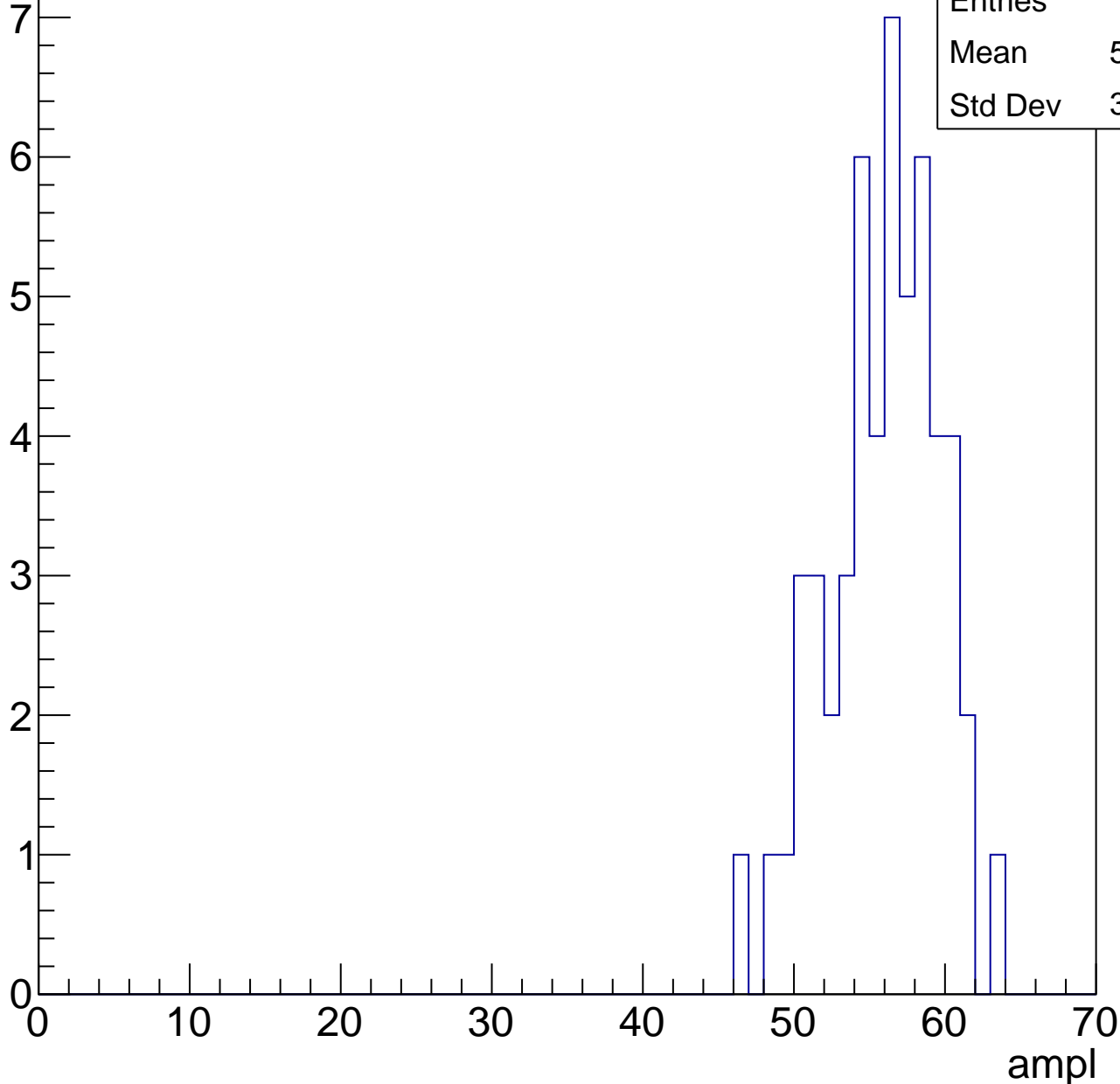


# B0L001S, U2-ch27, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 53    |
| Mean    | 55.45 |
| Std Dev | 3.622 |

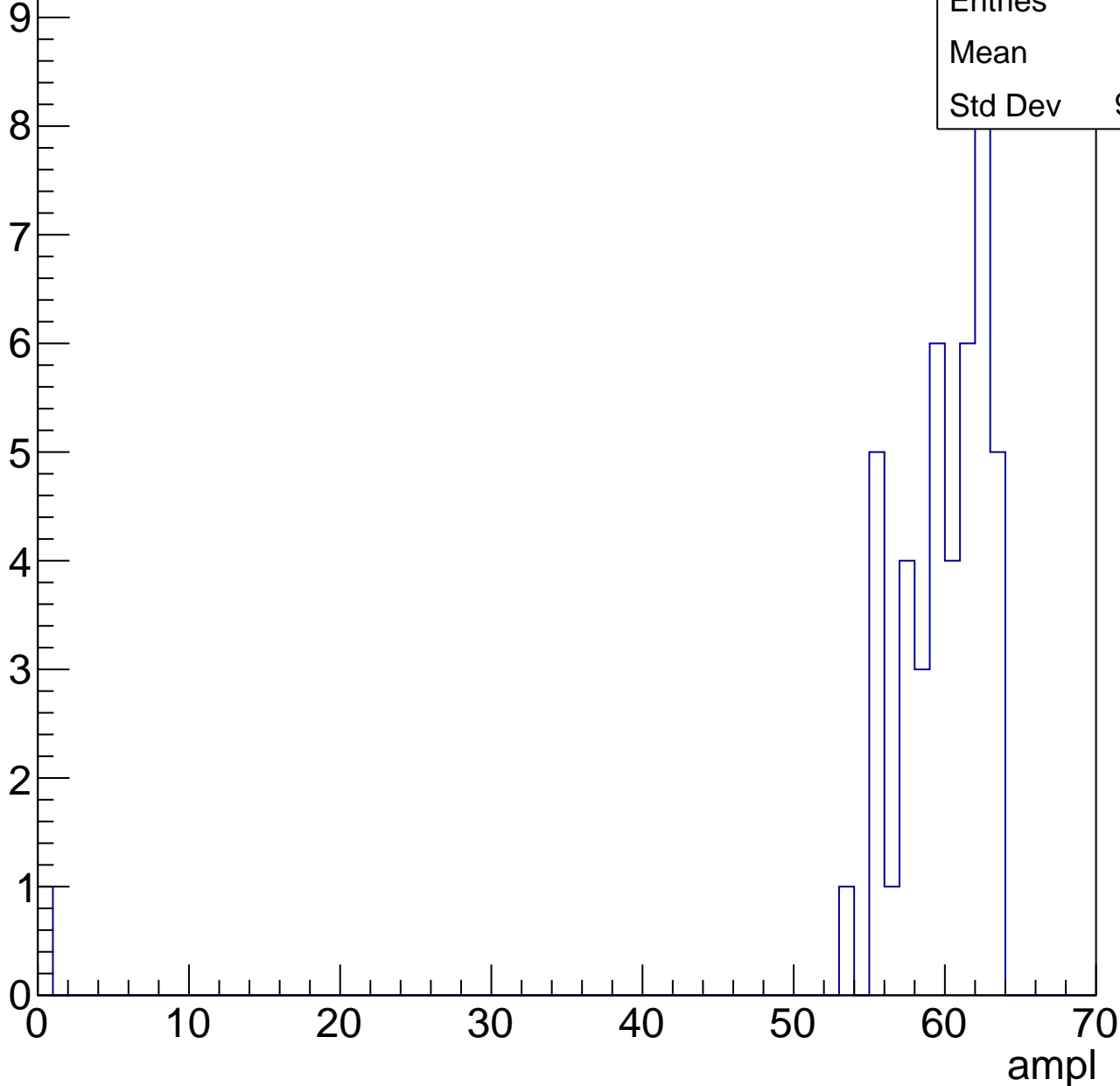


# B0L001S, U2-ch27, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

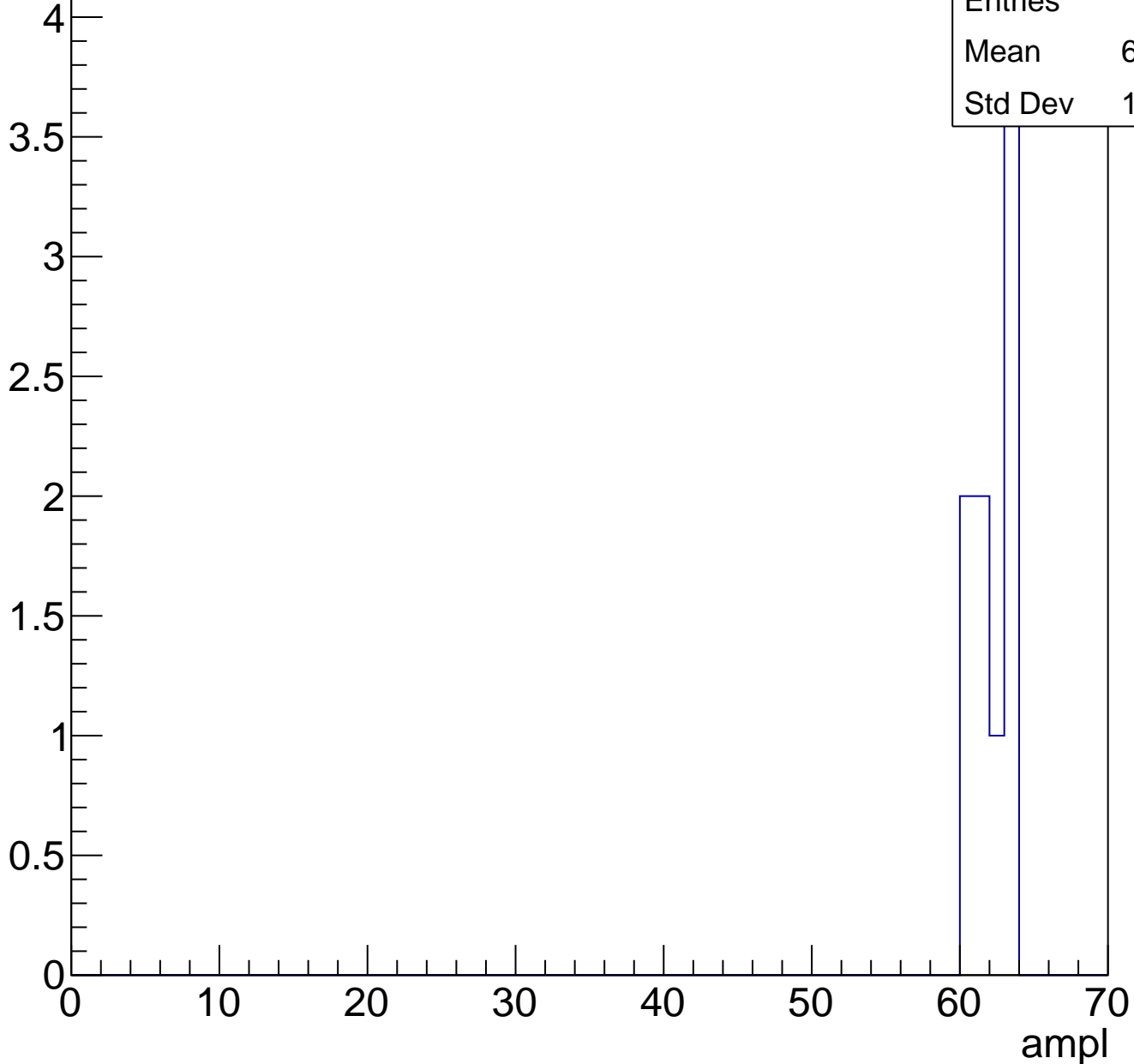
|         |       |
|---------|-------|
| Entries | 45    |
| Mean    | 58.2  |
| Std Dev | 9.171 |



# B0L001S, U2-ch27, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch27, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U2-ch28, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 59    |
| Mean    | 29.14 |
| Std Dev | 6.547 |

**Gaus mean : 30.3741**

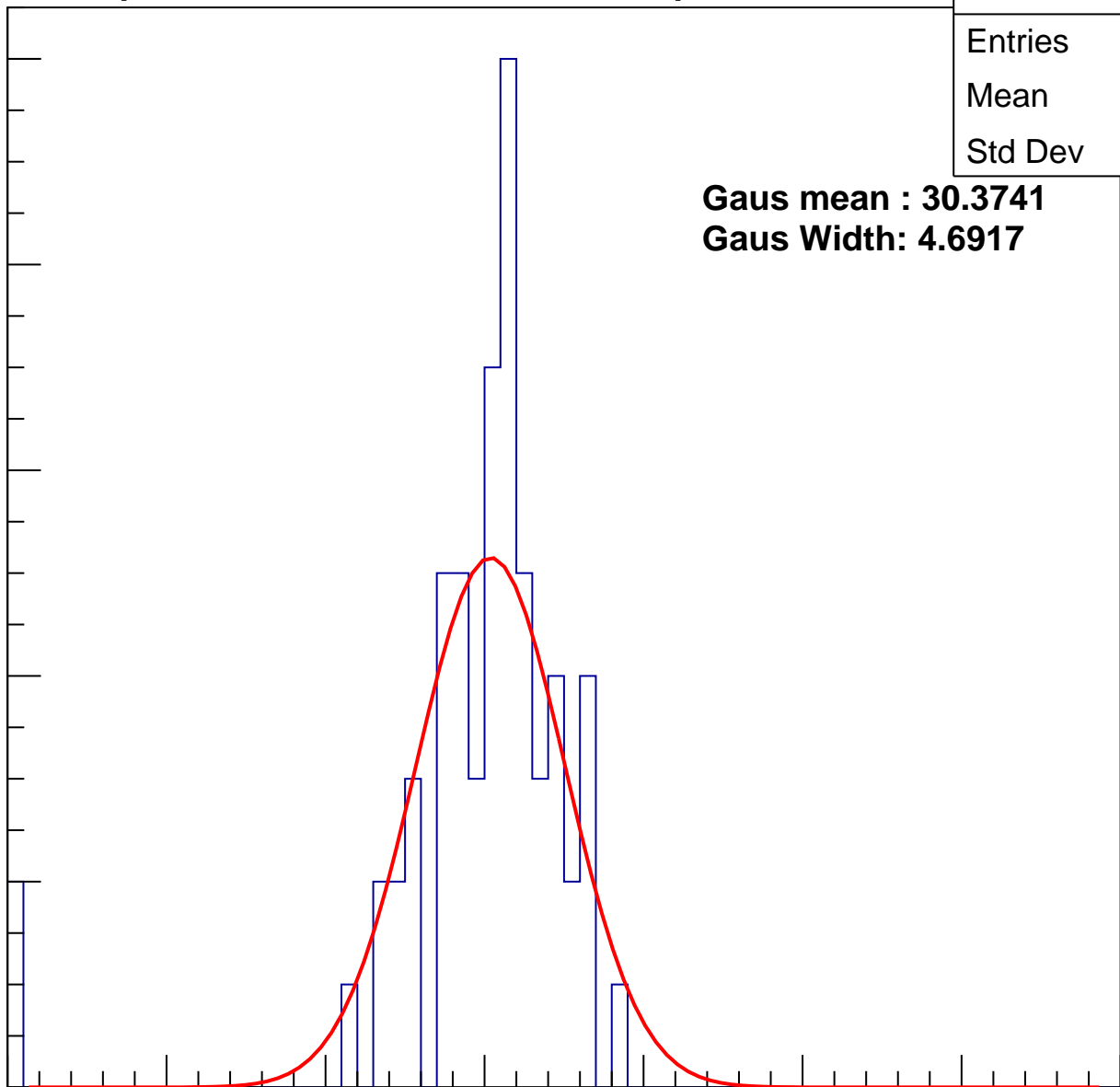
**Gaus Width: 4.6917**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U2-ch28, adc1

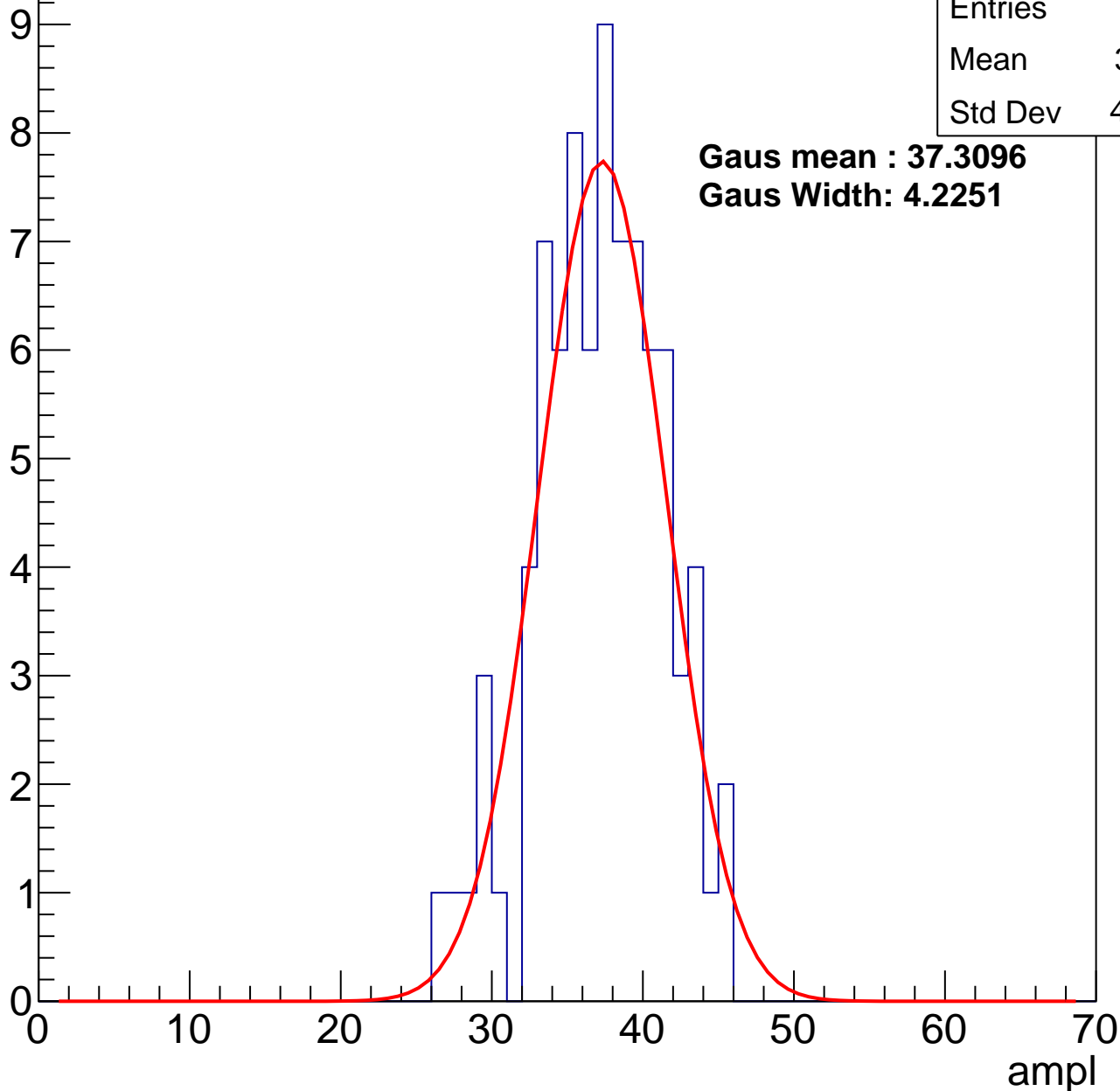
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 83    |
| Mean    | 36.71 |
| Std Dev | 4.138 |

**Gaus mean : 37.3096**

**Gaus Width: 4.2251**



# B0L001S, U2-ch28, adc2

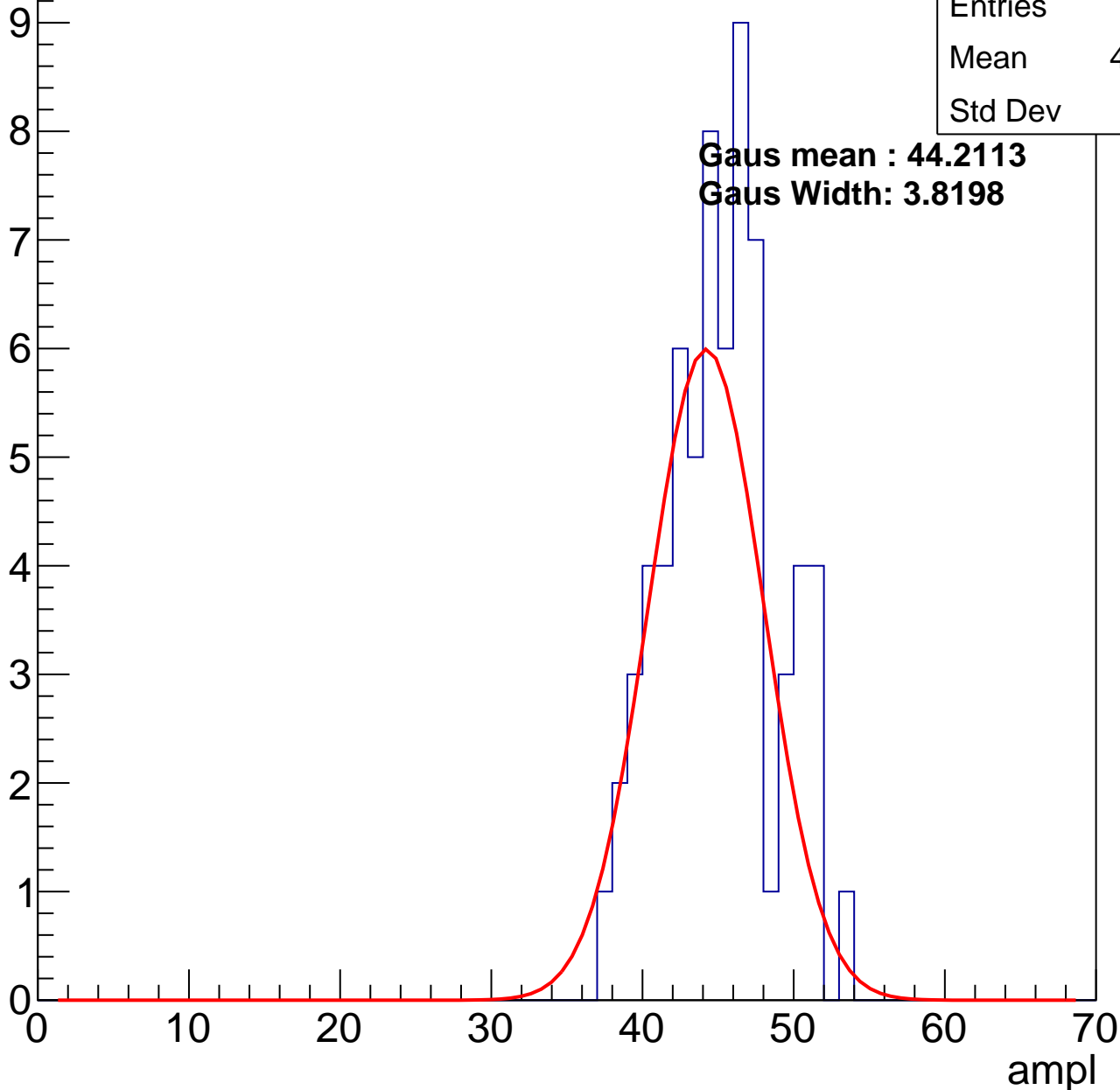
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 68    |
| Mean    | 44.68 |
| Std Dev | 3.66  |

**Gaus mean : 44.2113**

**Gaus Width: 3.8198**

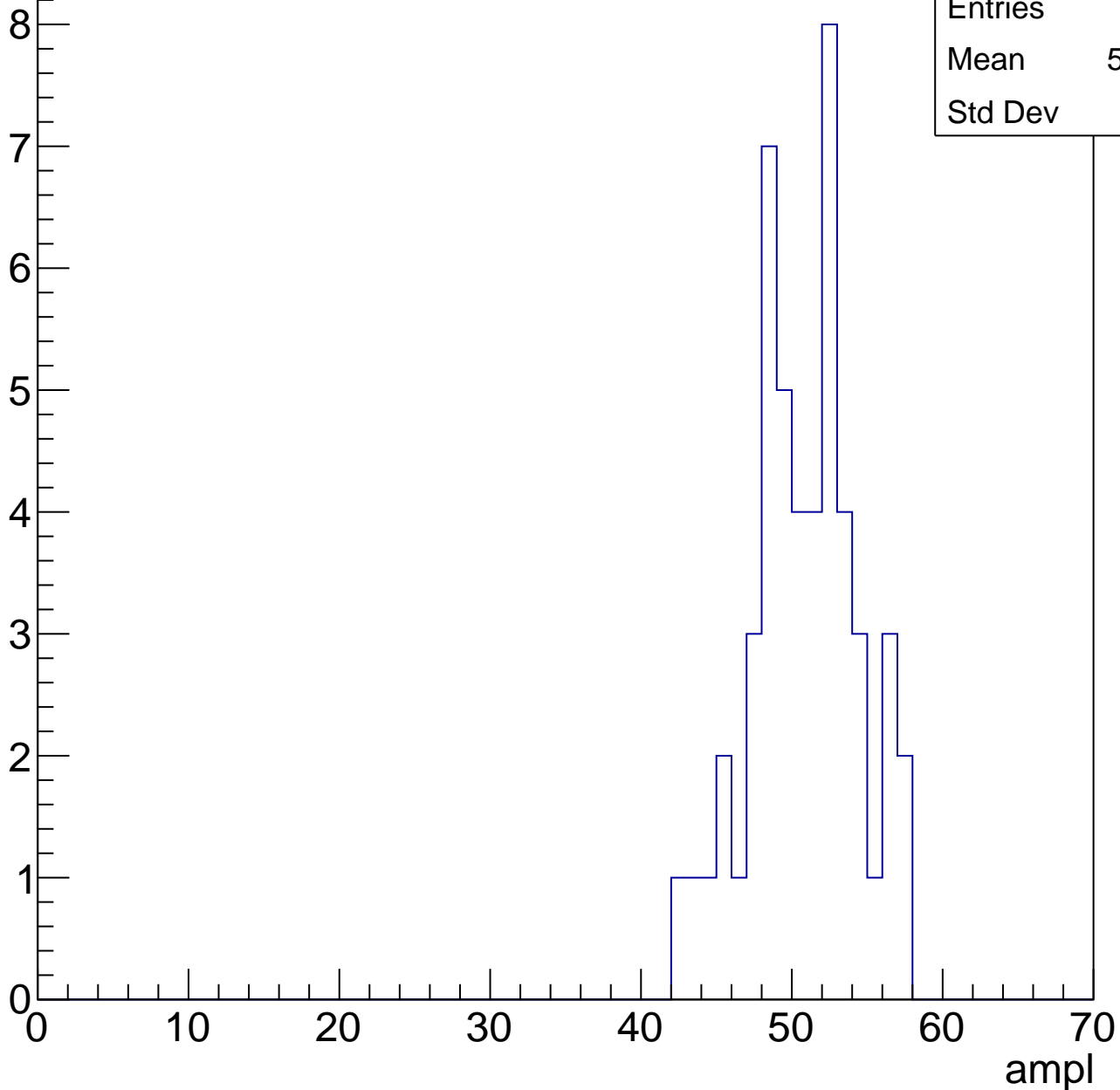


# B0L001S, U2-ch28, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

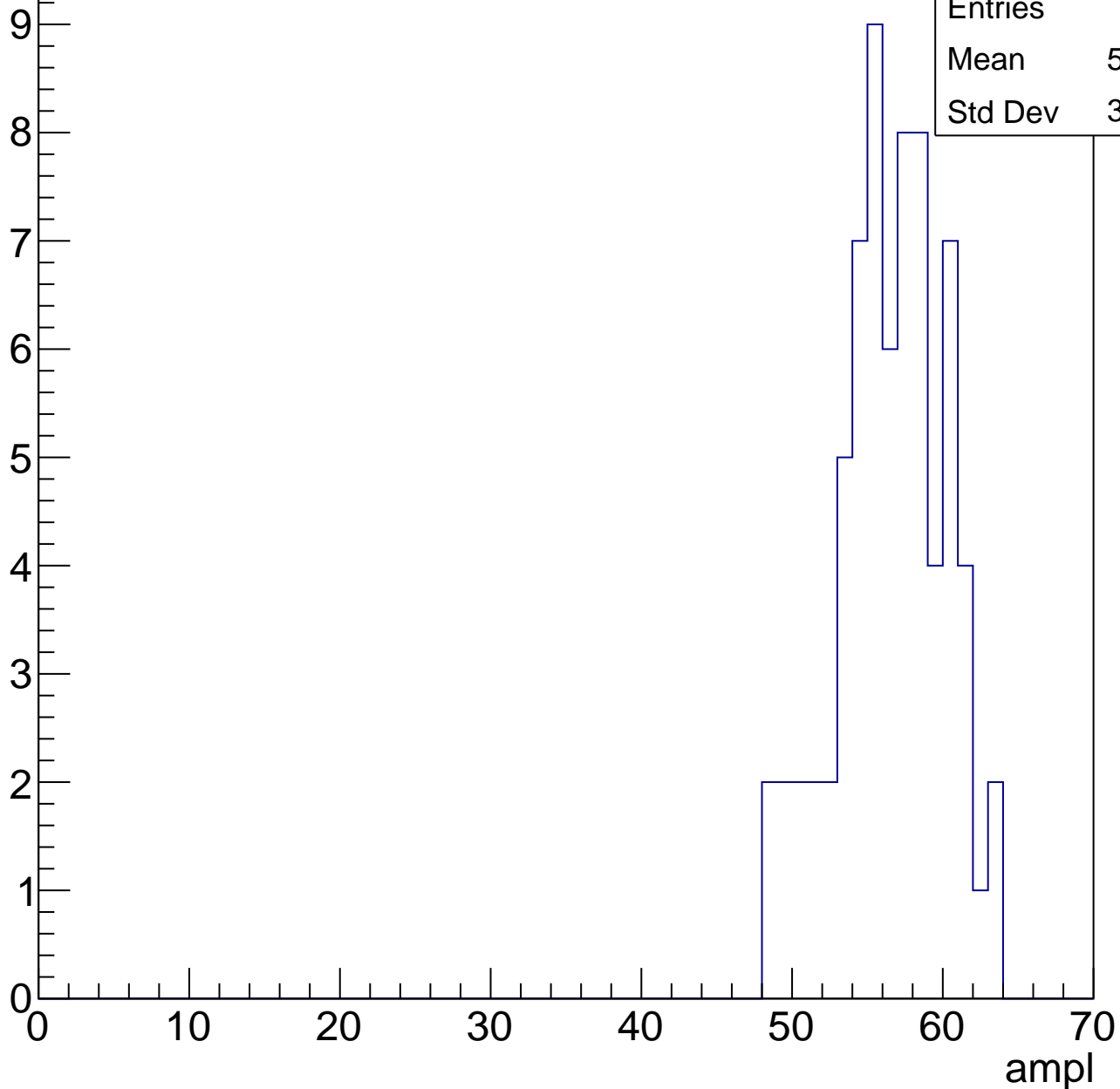
|         |       |
|---------|-------|
| Entries | 50    |
| Mean    | 50.36 |
| Std Dev | 3.52  |



# B0L001S, U2-ch28, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

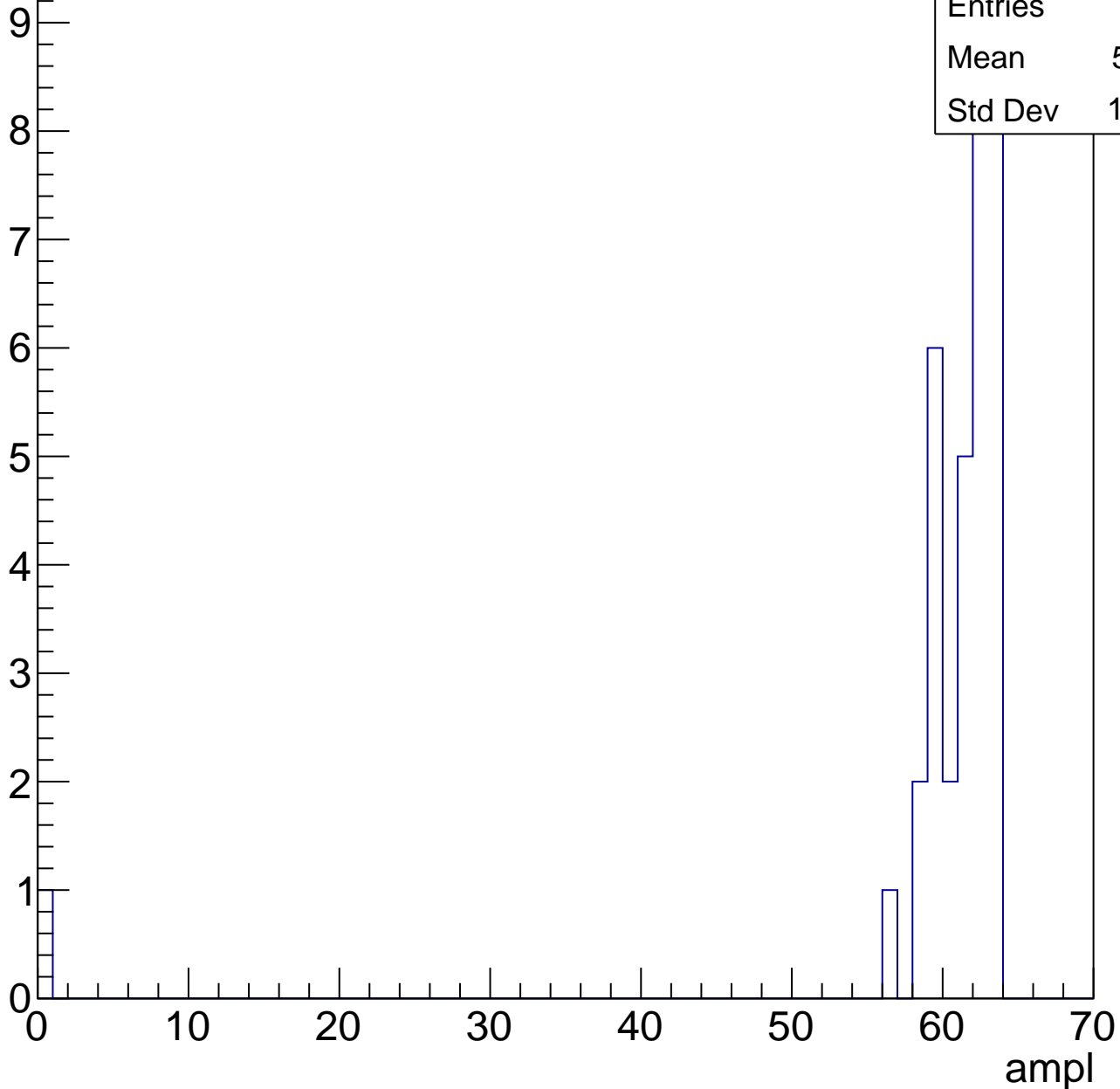


# B0L001S, U2-ch28, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

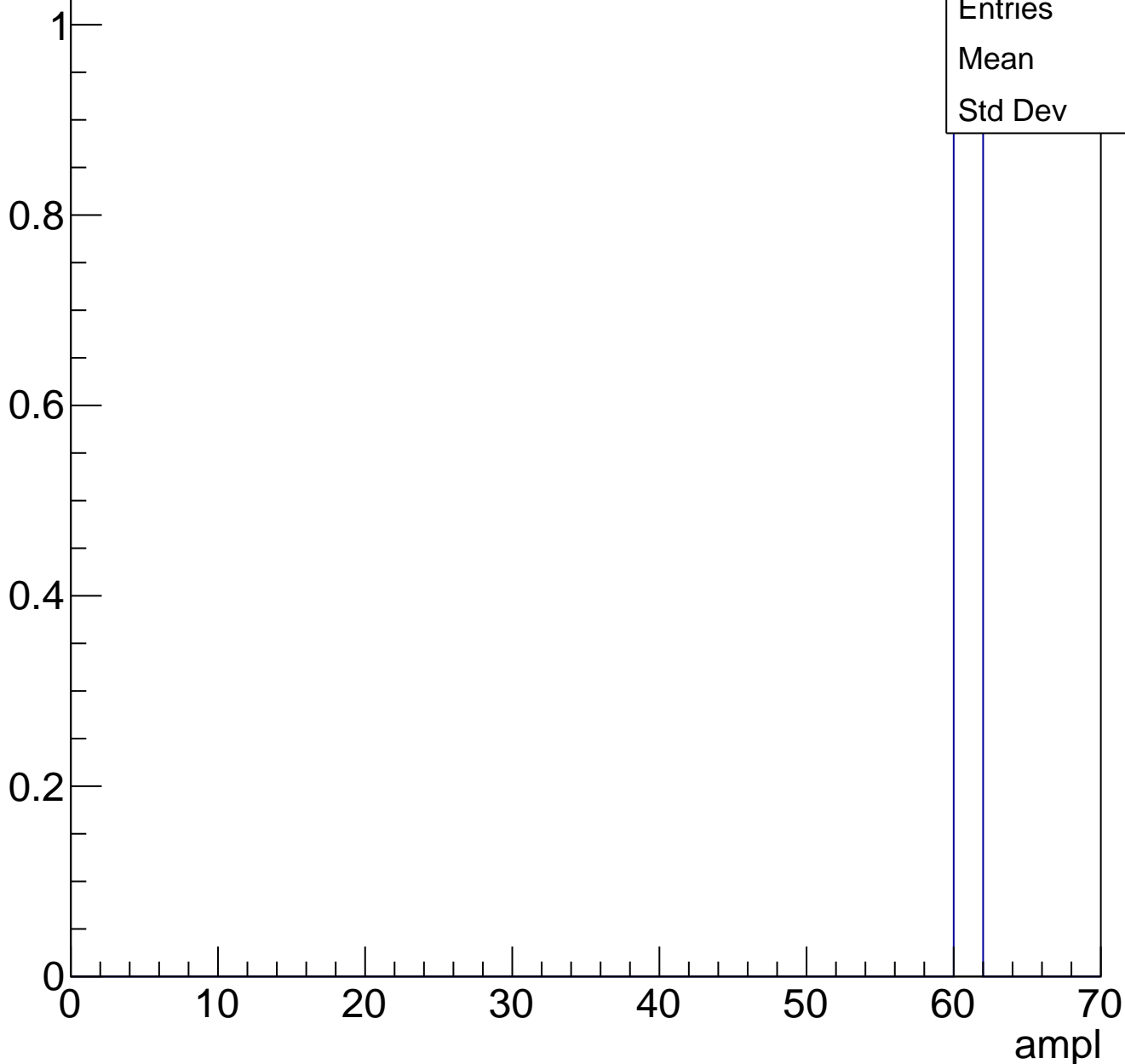
|         |       |
|---------|-------|
| Entries | 34    |
| Mean    | 59.21 |
| Std Dev | 10.46 |



# B0L001S, U2-ch28, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch28, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 1 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch29, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 70    |
| Mean    | 31.53 |
| Std Dev | 3.263 |

**Gaus mean : 32.0382**

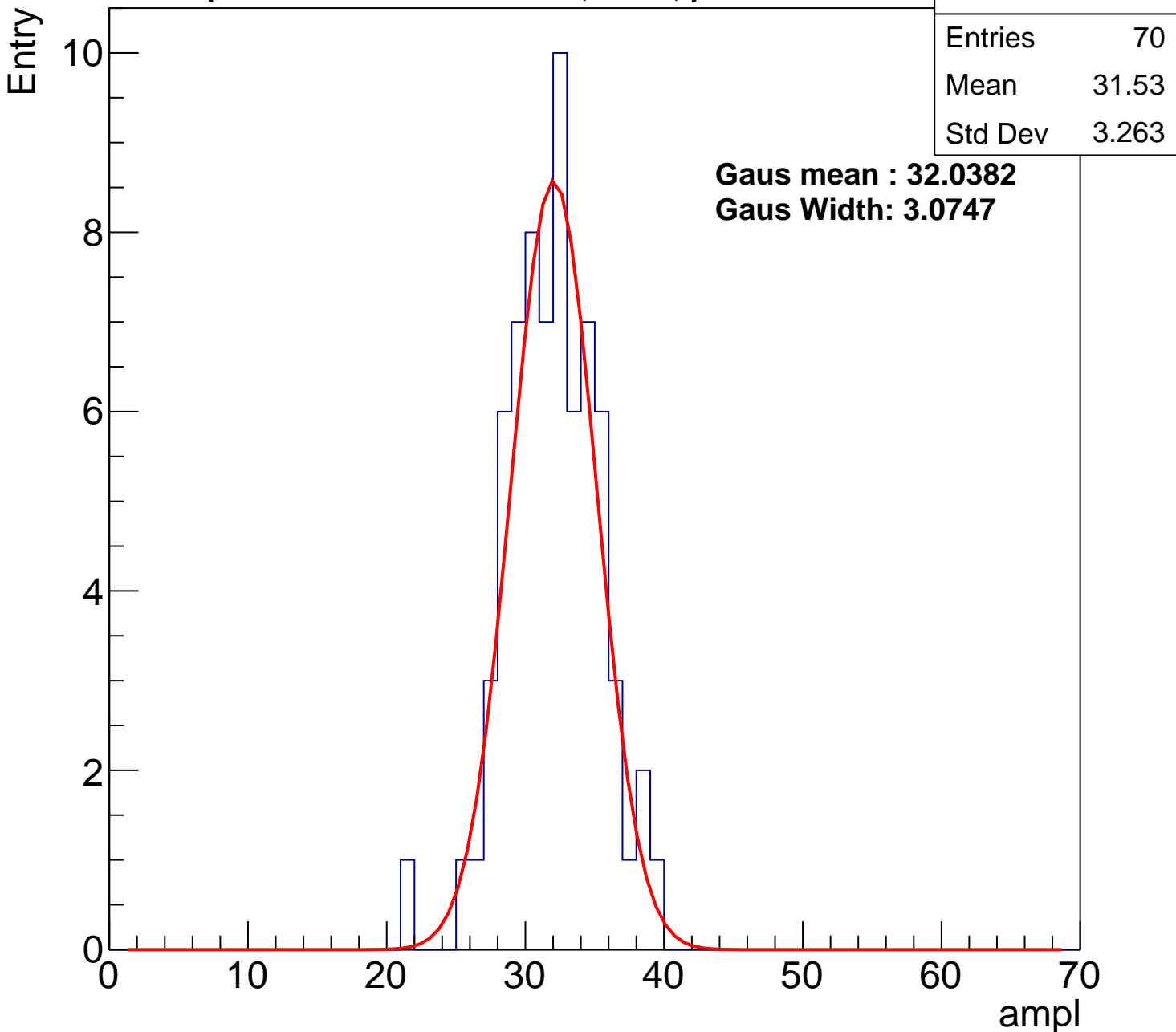
**Gaus Width: 3.0747**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U2-ch29, adc1

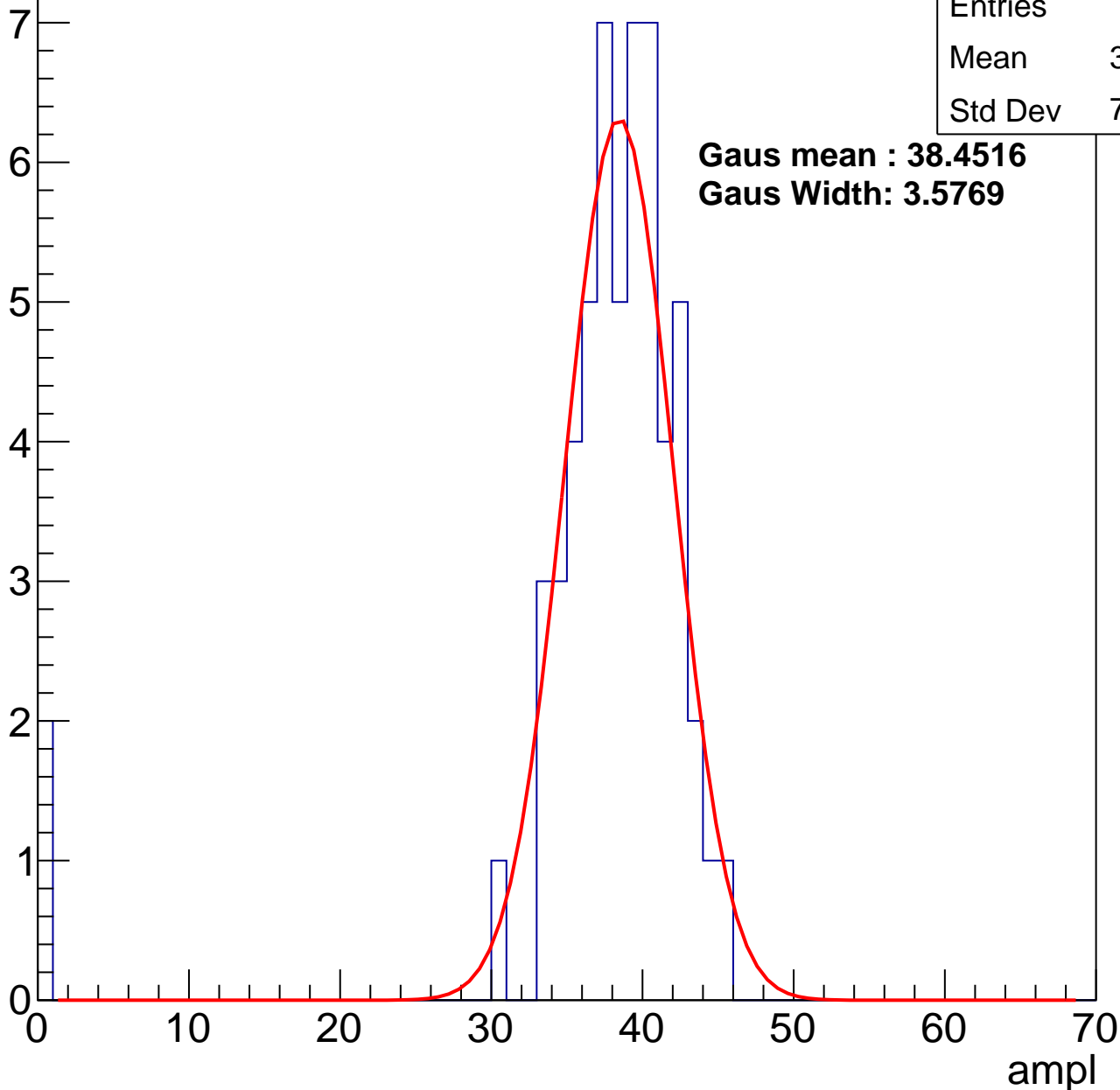
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 57    |
| Mean    | 36.88 |
| Std Dev | 7.669 |

**Gaus mean : 38.4516**

**Gaus Width: 3.5769**



# B0L001S, U2-ch29, adc2

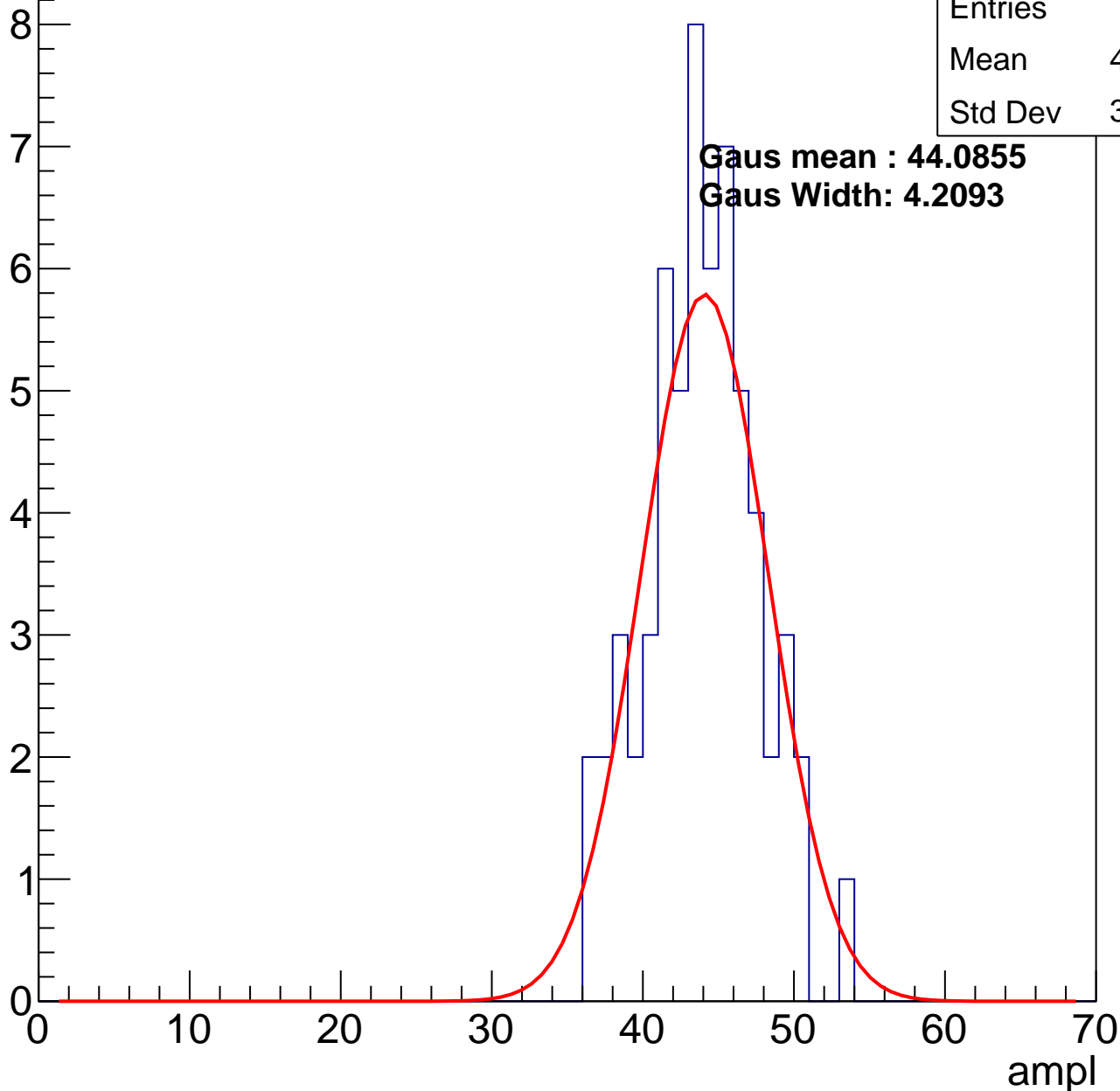
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 61    |
| Mean    | 43.46 |
| Std Dev | 3.665 |

**Gaus mean : 44.0855**

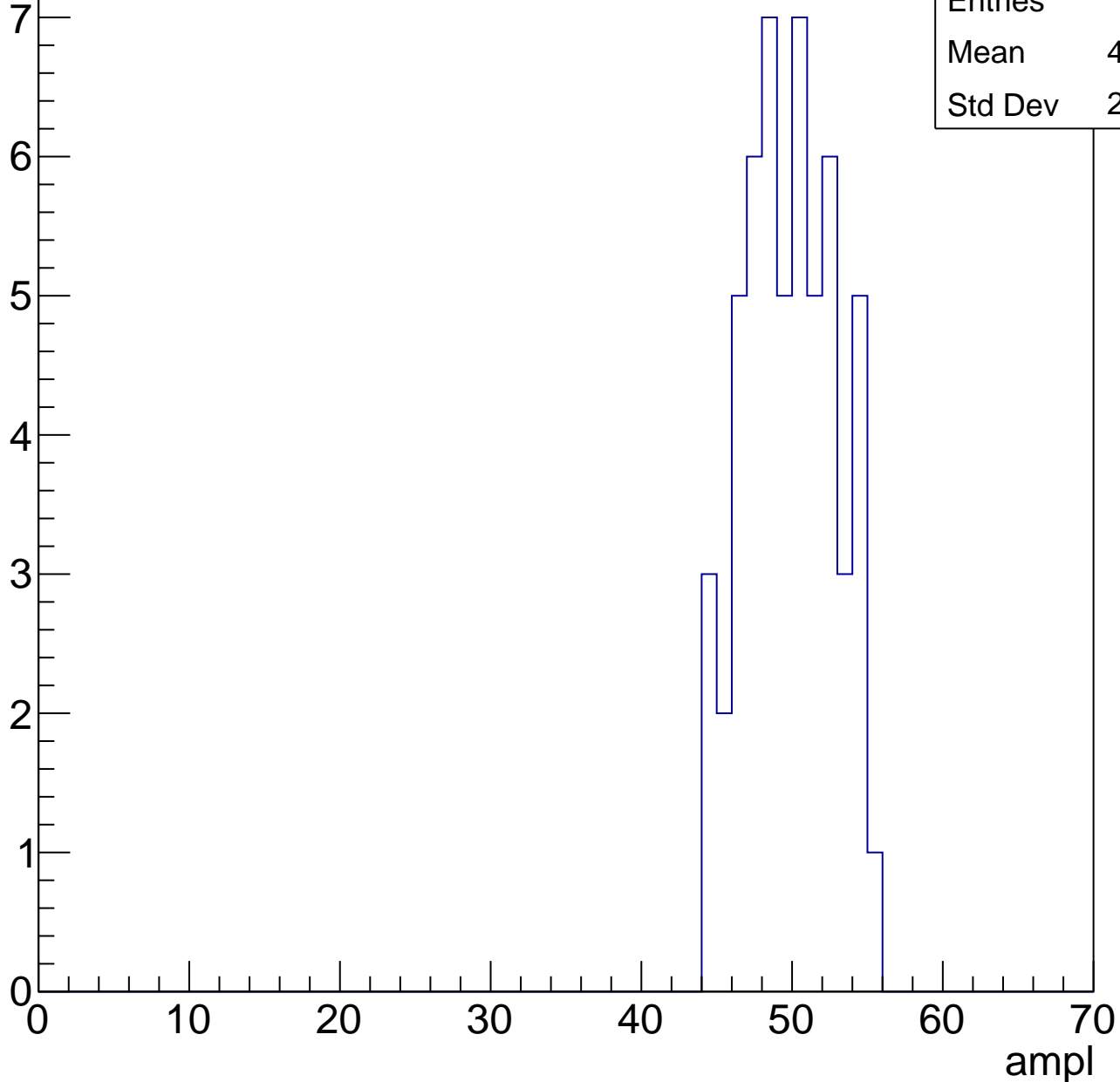
**Gaus Width: 4.2093**



# B0L001S, U2-ch29, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

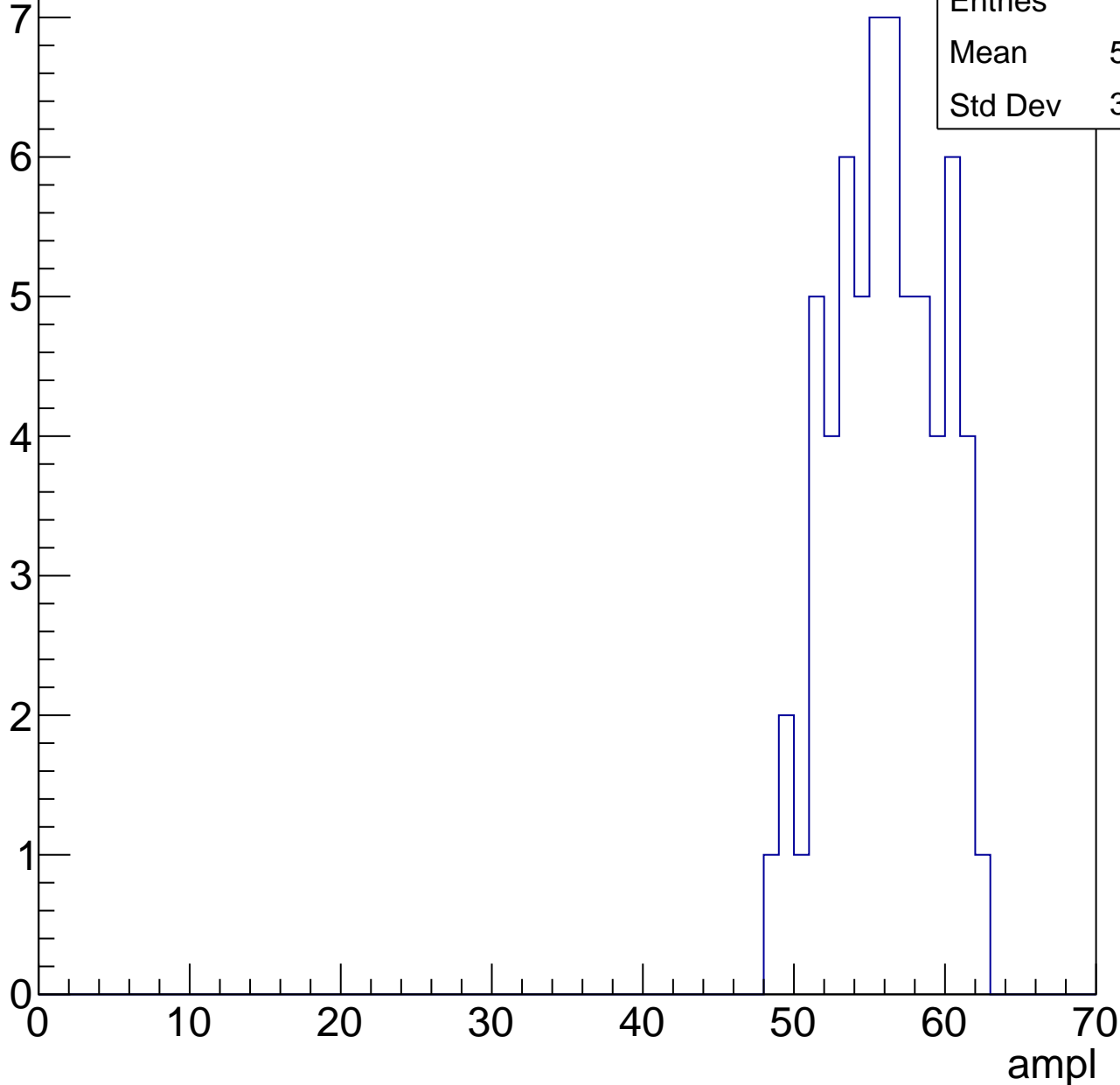


|         |       |
|---------|-------|
| Entries | 55    |
| Mean    | 49.38 |
| Std Dev | 2.908 |

# B0L001S, U2-ch29, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

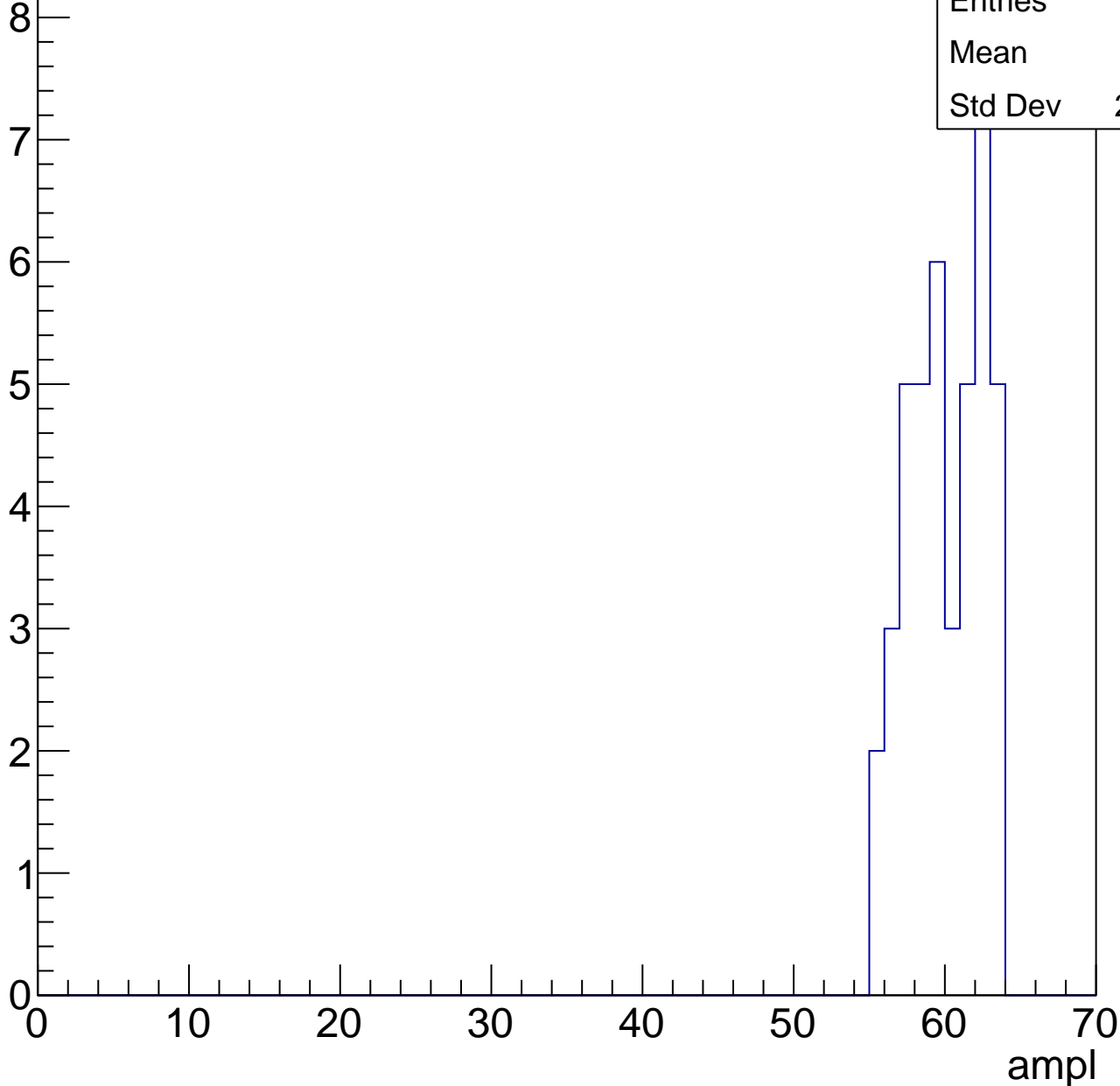


# B0L001S, U2-ch29, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 42    |
| Mean    | 59.6  |
| Std Dev | 2.411 |

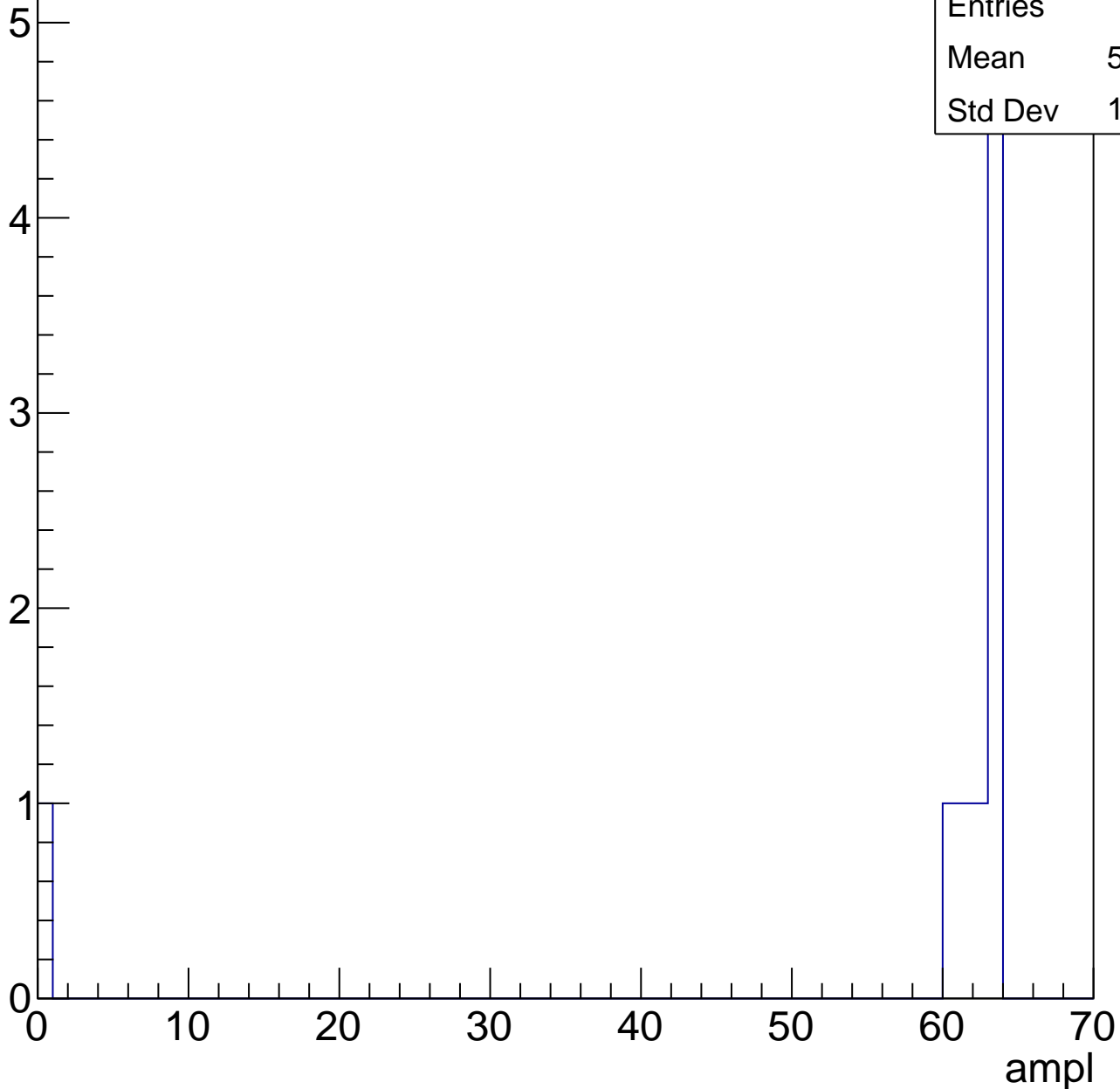


# B0L001S, U2-ch29, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 9     |
| Mean    | 55.33 |
| Std Dev | 19.59 |





# B0L001S, U2-ch29, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 4 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch30, adc0

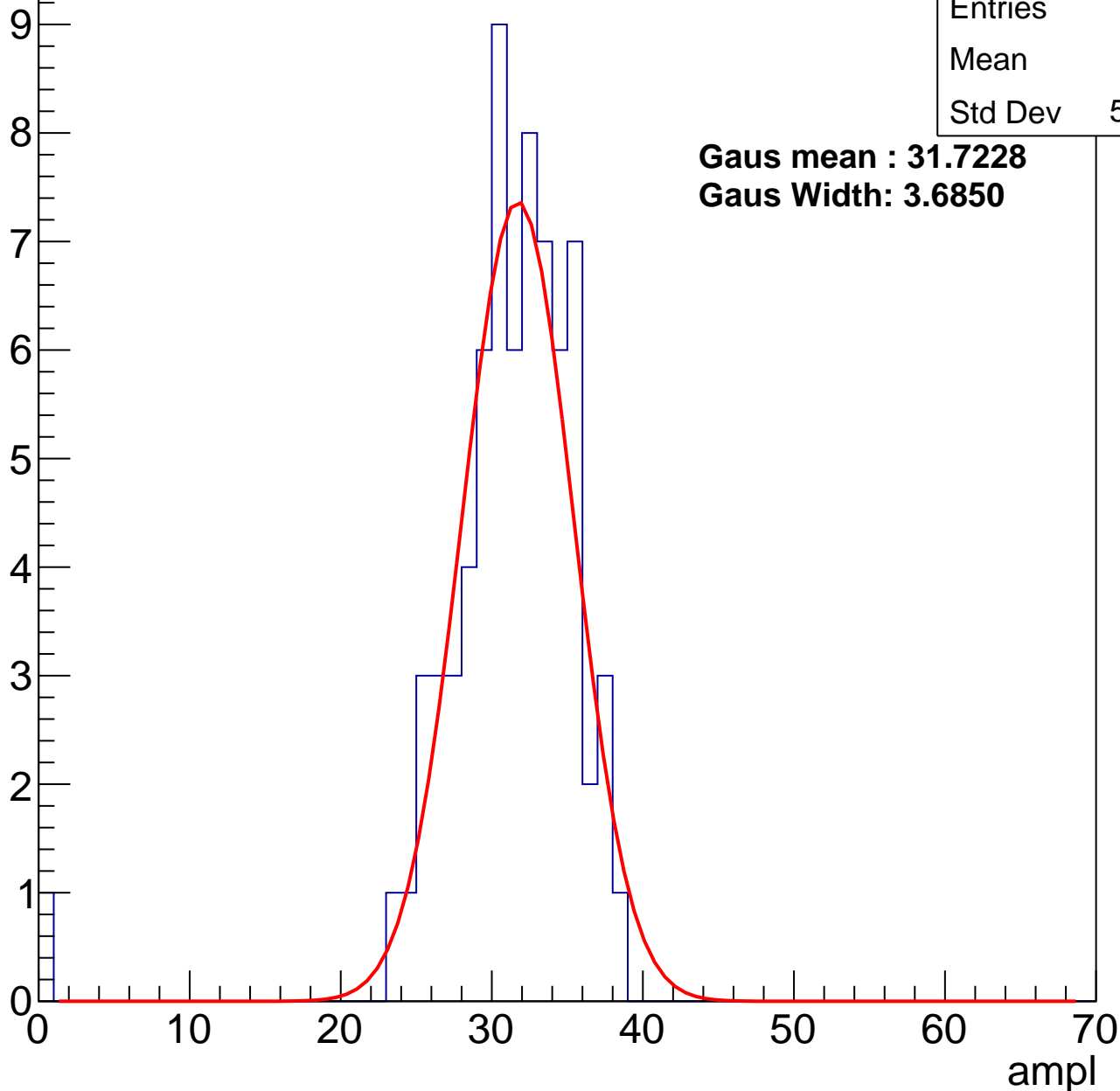
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 71    |
| Mean    | 30.7  |
| Std Dev | 5.003 |

**Gaus mean : 31.7228**

**Gaus Width: 3.6850**



# B0L001S, U2-ch30, adc1

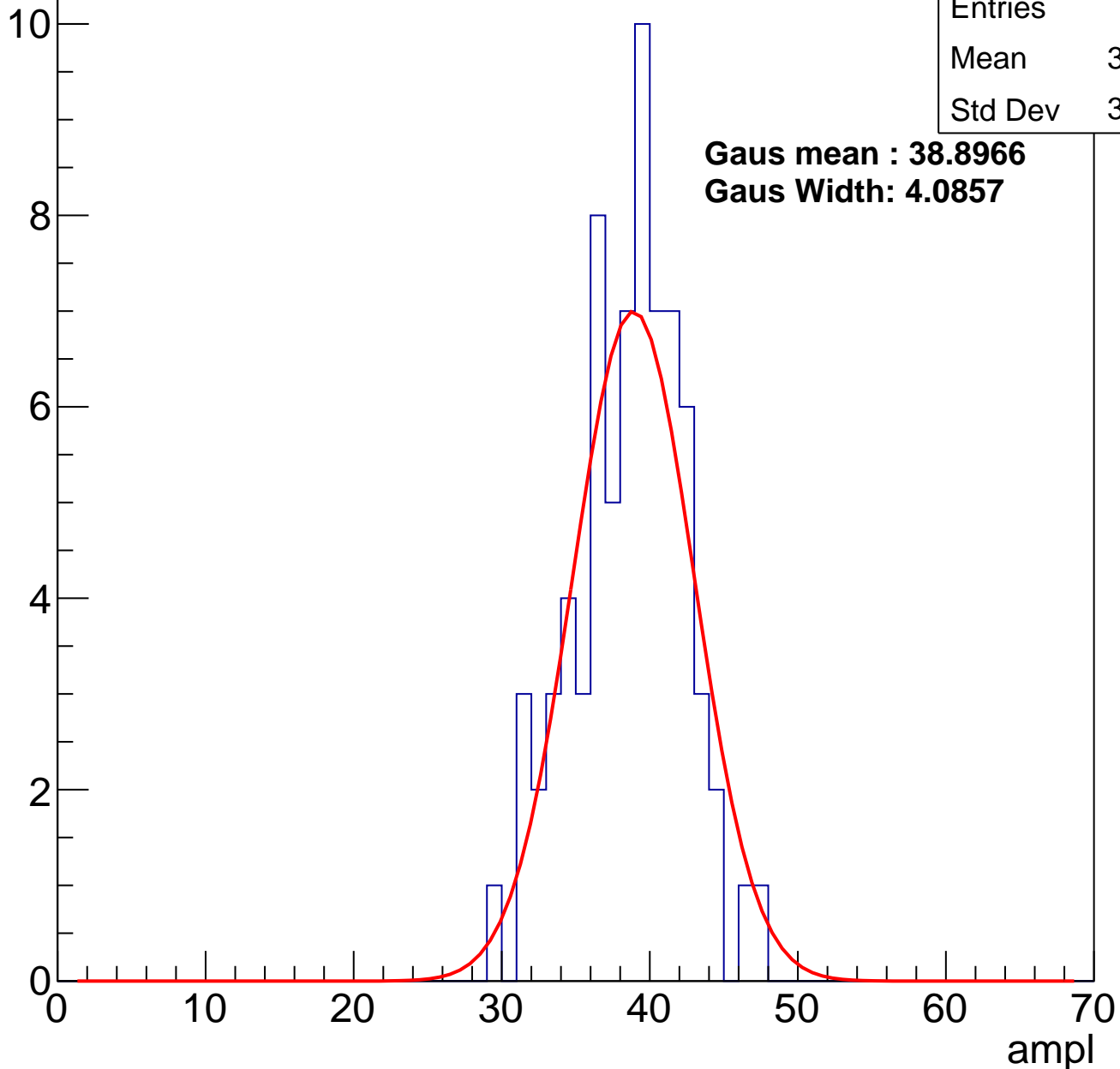
calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 73    |
| Mean    | 38.14 |
| Std Dev | 3.684 |

**Gaus mean : 38.8966**

**Gaus Width: 4.0857**

Entry



# B0L001S, U2-ch30, adc2

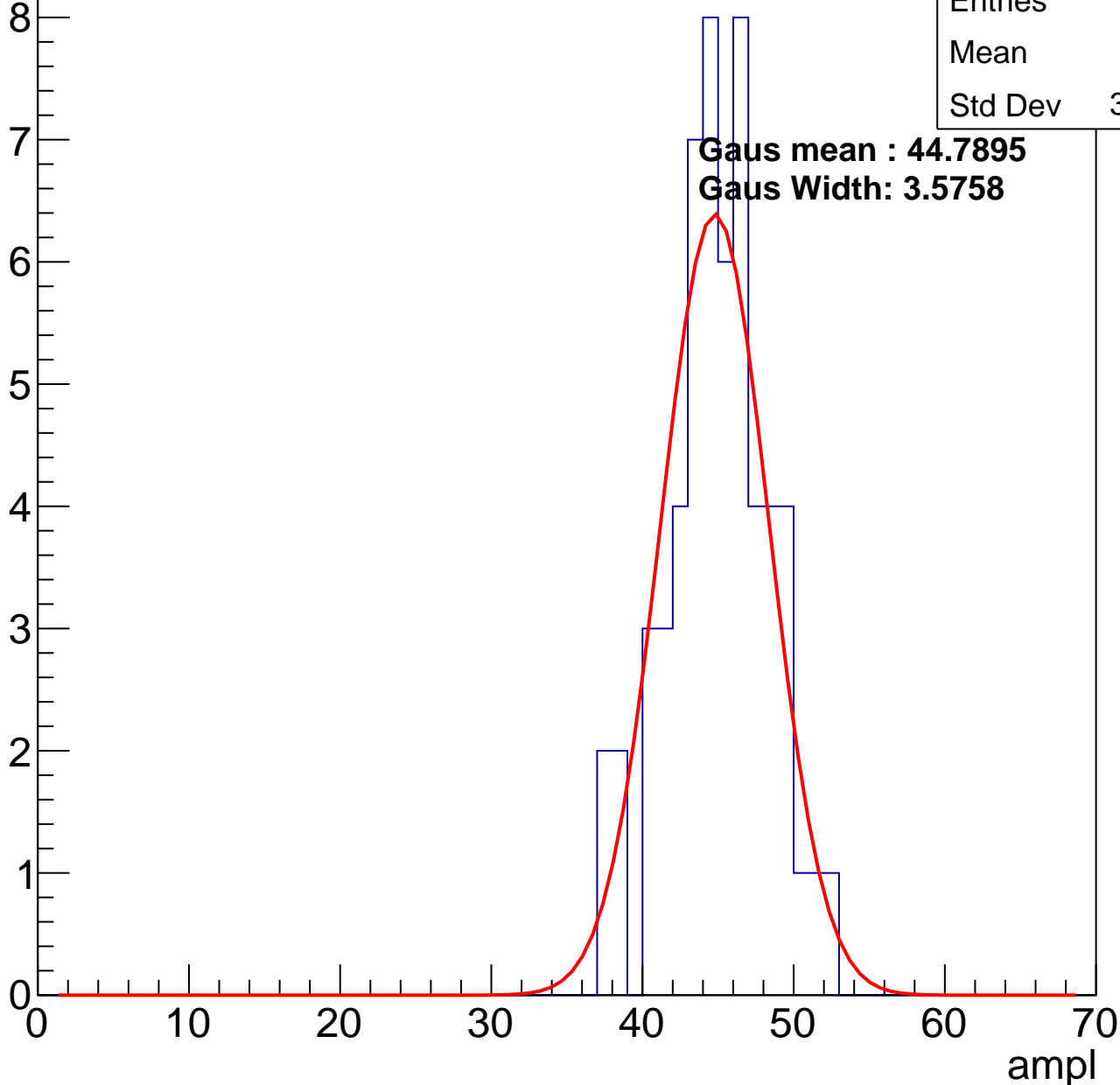
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 58    |
| Mean    | 44.5  |
| Std Dev | 3.323 |

**Gaus mean : 44.7895**

**Gaus Width: 3.5758**

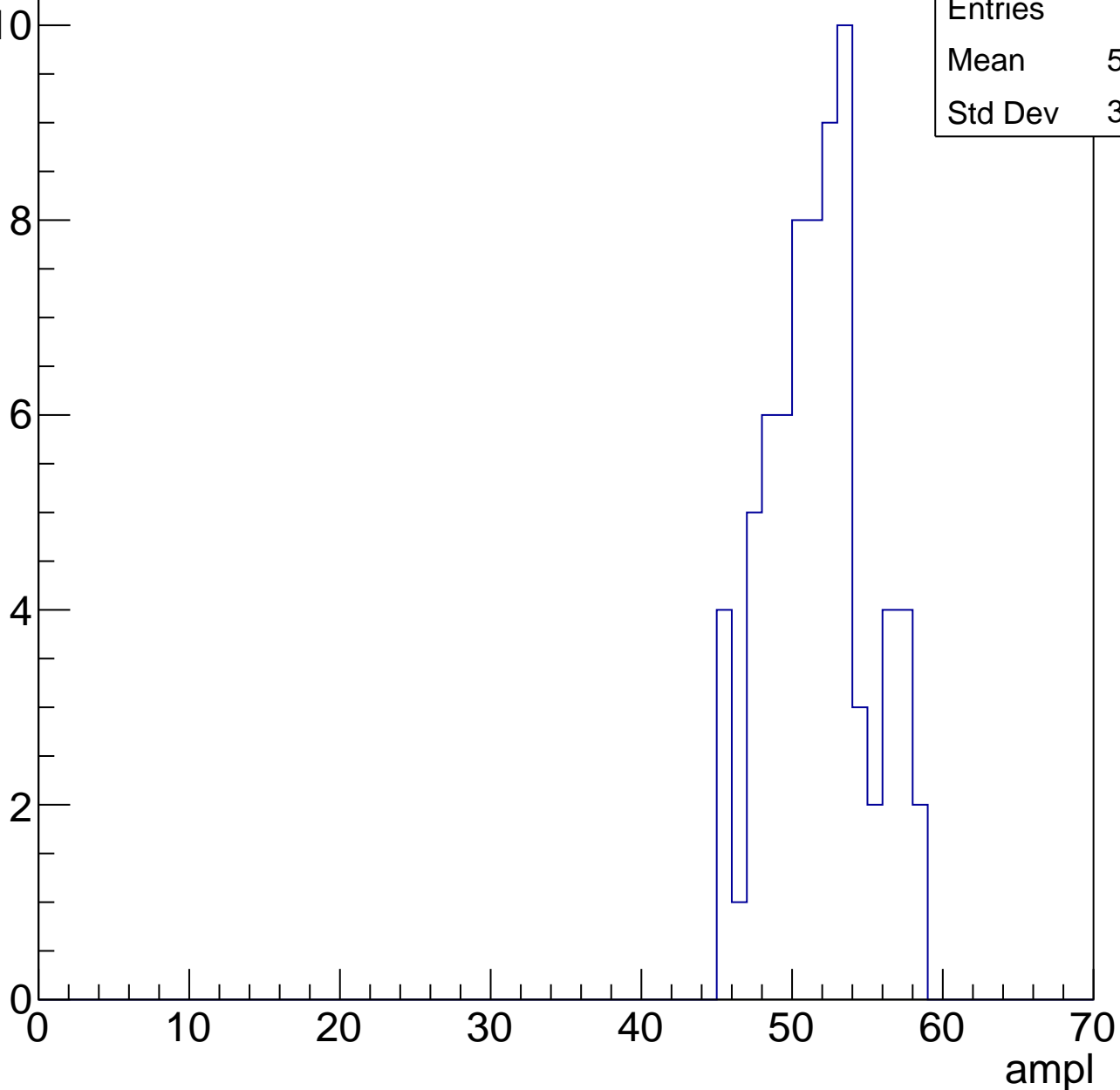


# B0L001S, U2-ch30, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 72    |
| Mean    | 51.24 |
| Std Dev | 3.293 |

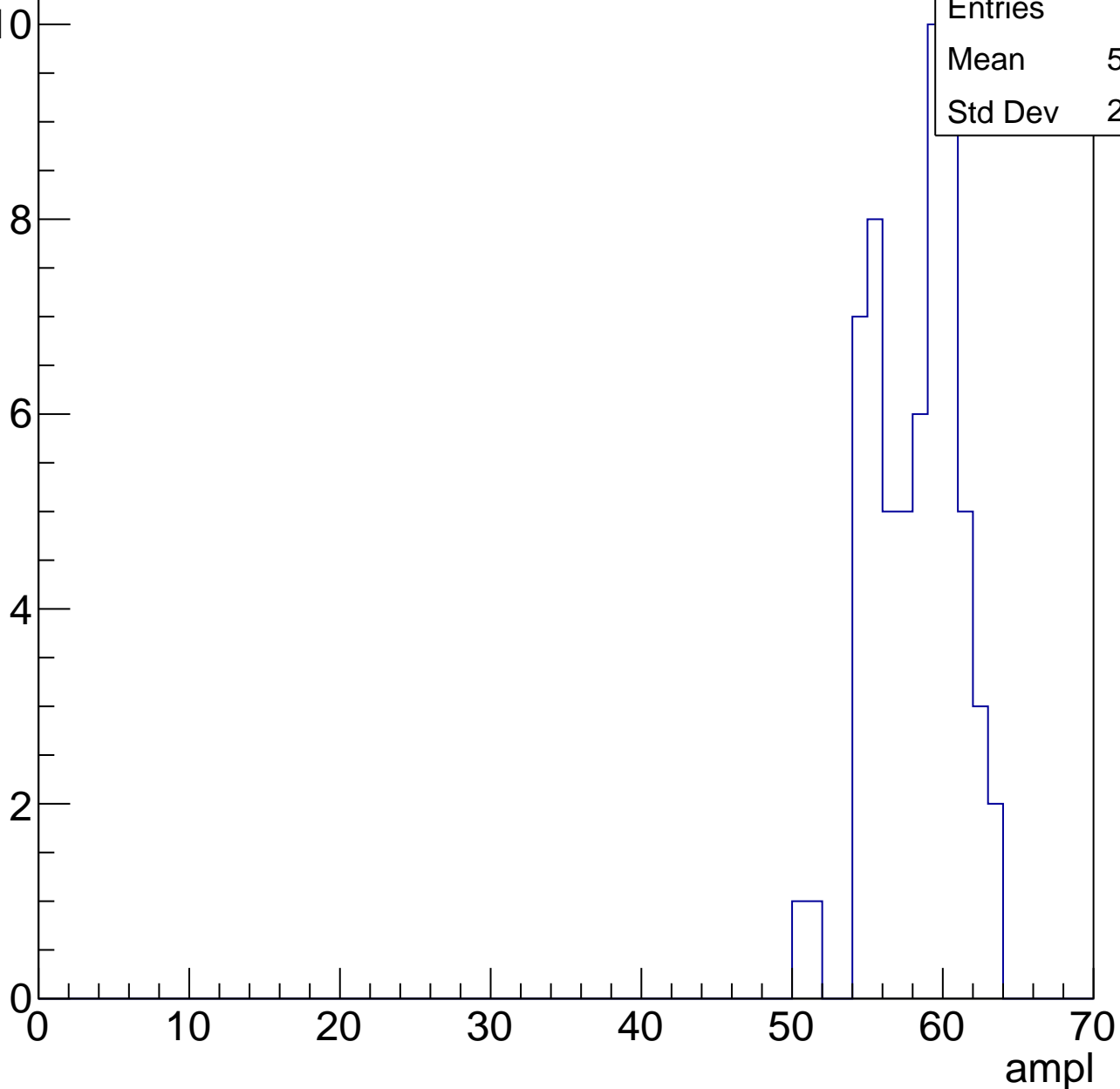


# B0L001S, U2-ch30, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 62    |
| Mean    | 57.73 |
| Std Dev | 2.858 |

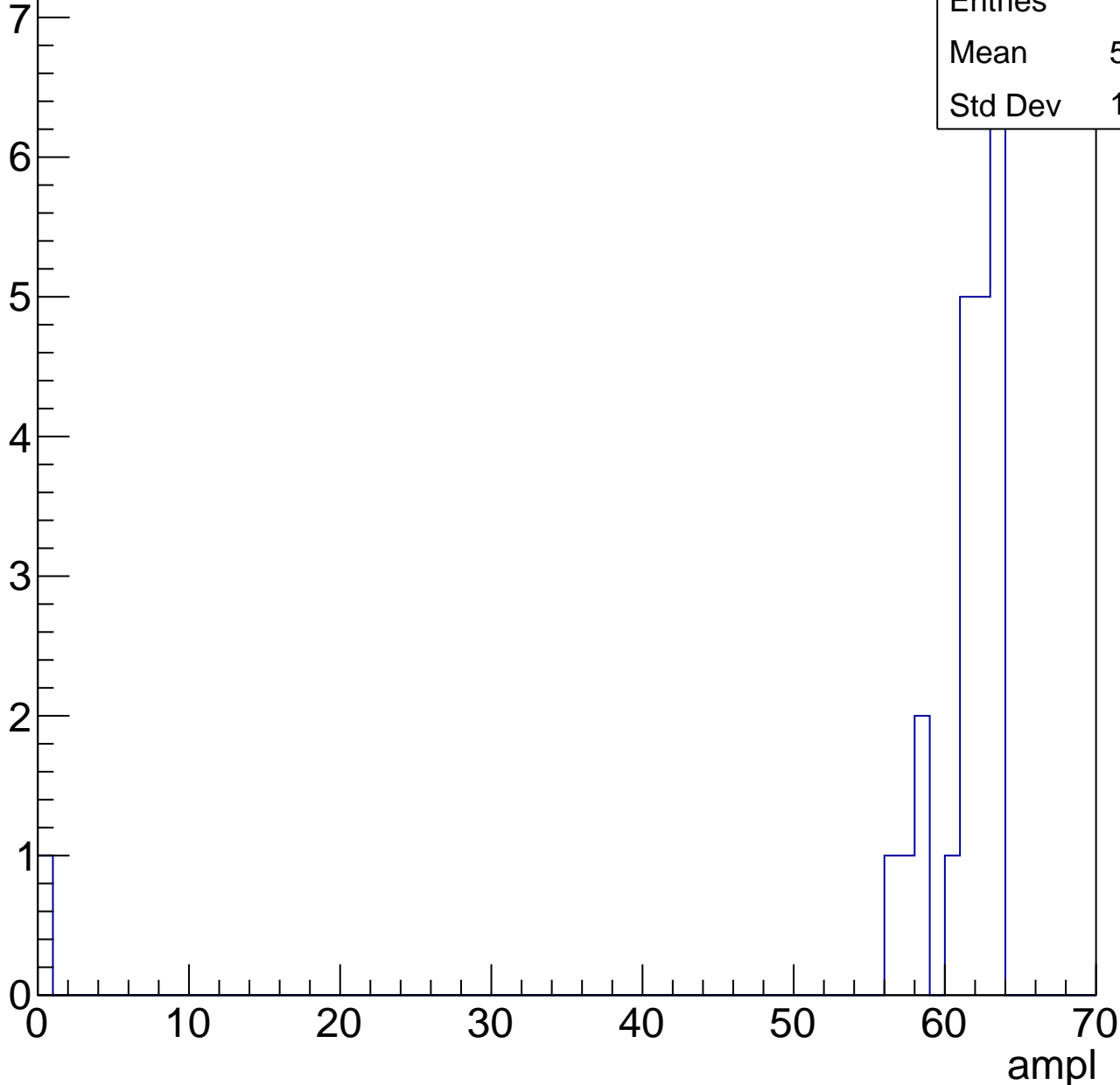


# B0L001S, U2-ch30, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 23    |
| Mean    | 58.48 |
| Std Dev | 12.63 |



# B0L001S, U2-ch30, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch30, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 0 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch31, adc0

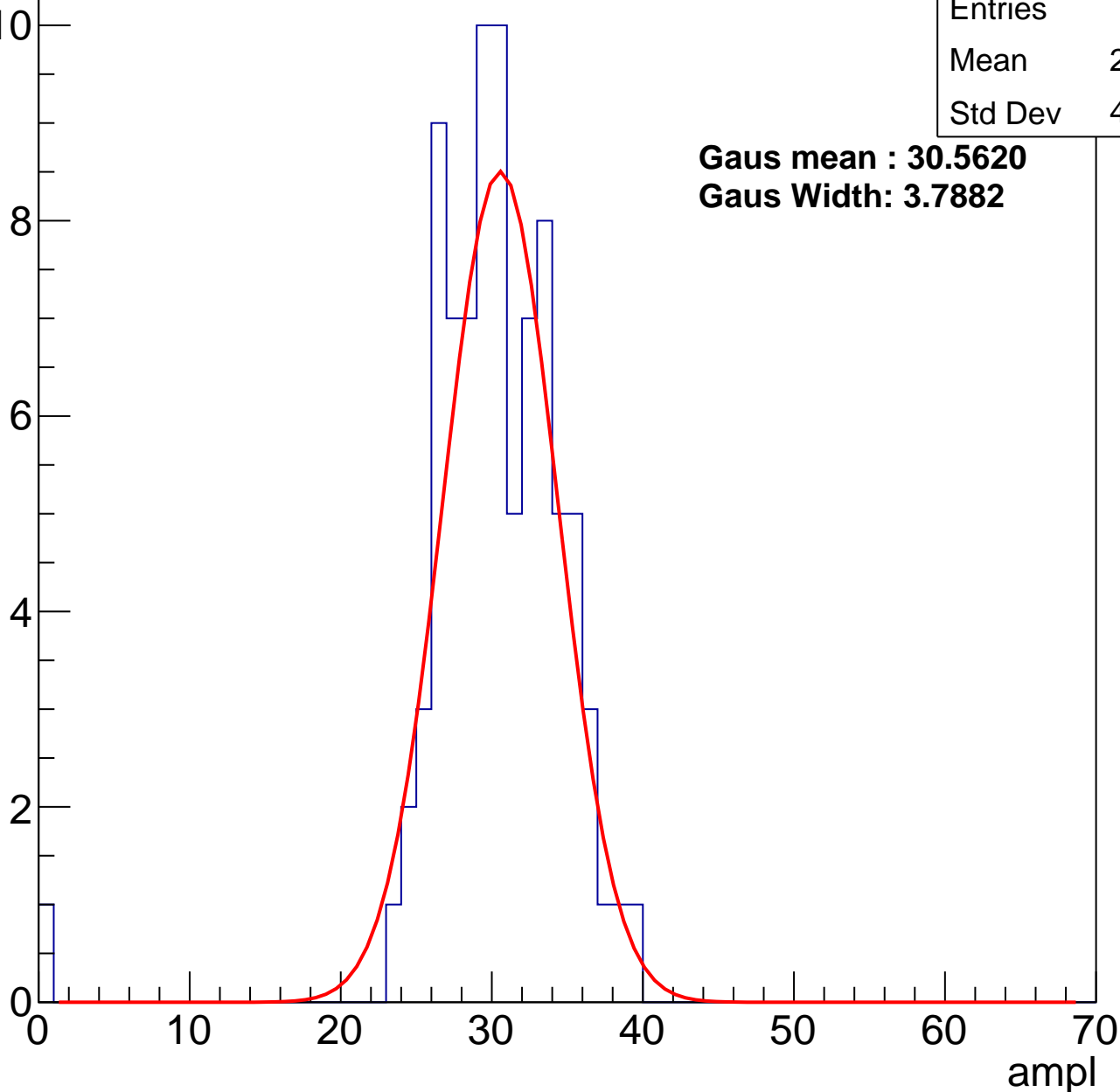
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 86    |
| Mean    | 29.83 |
| Std Dev | 4.762 |

**Gaus mean : 30.5620**

**Gaus Width: 3.7882**



# B0L001S, U2-ch31, adc1

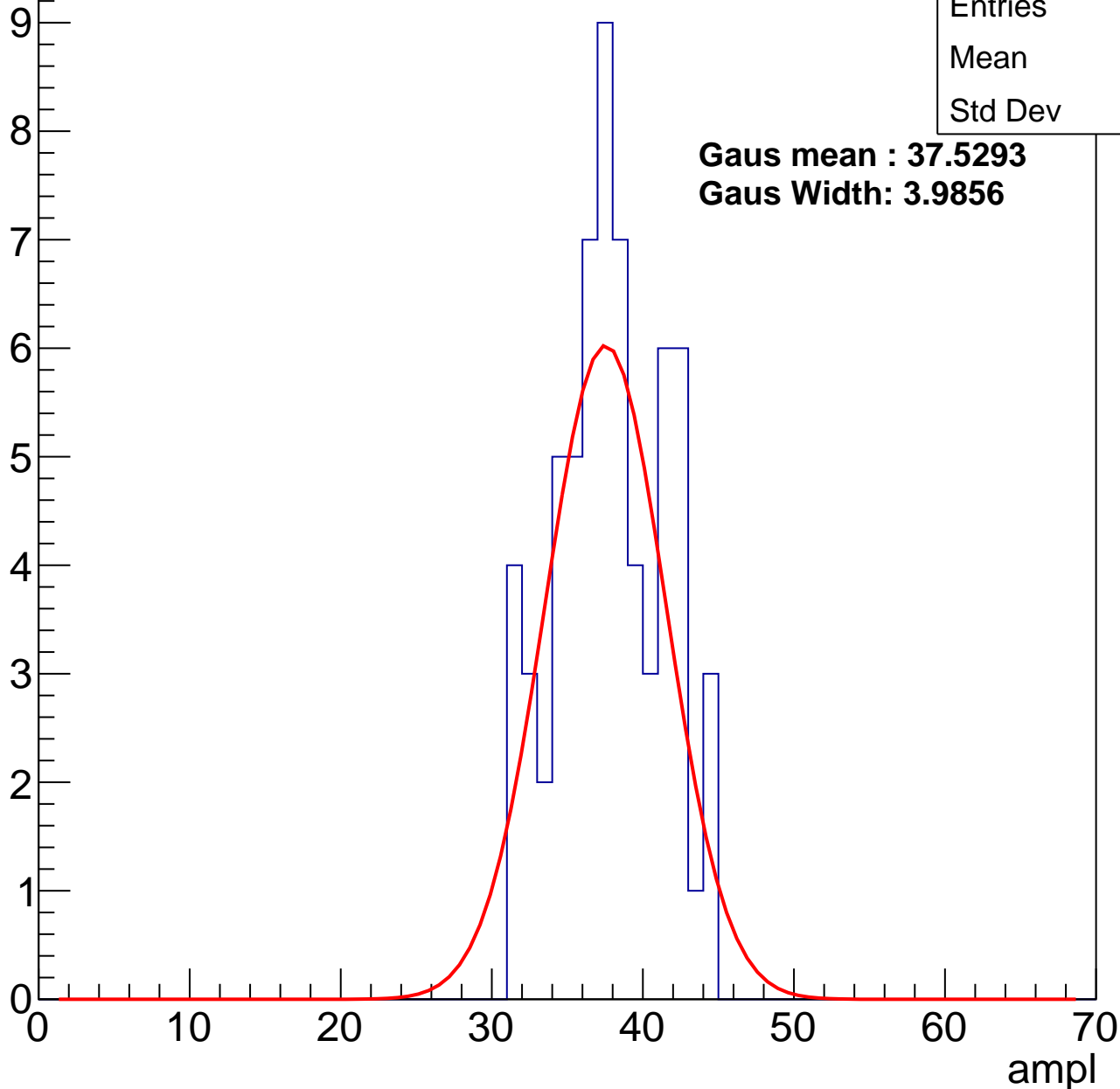
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |      |
|---------|------|
| Entries | 65   |
| Mean    | 37.4 |
| Std Dev | 3.49 |

**Gaus mean : 37.5293**

**Gaus Width: 3.9856**



# B0L001S, U2-ch31, adc2

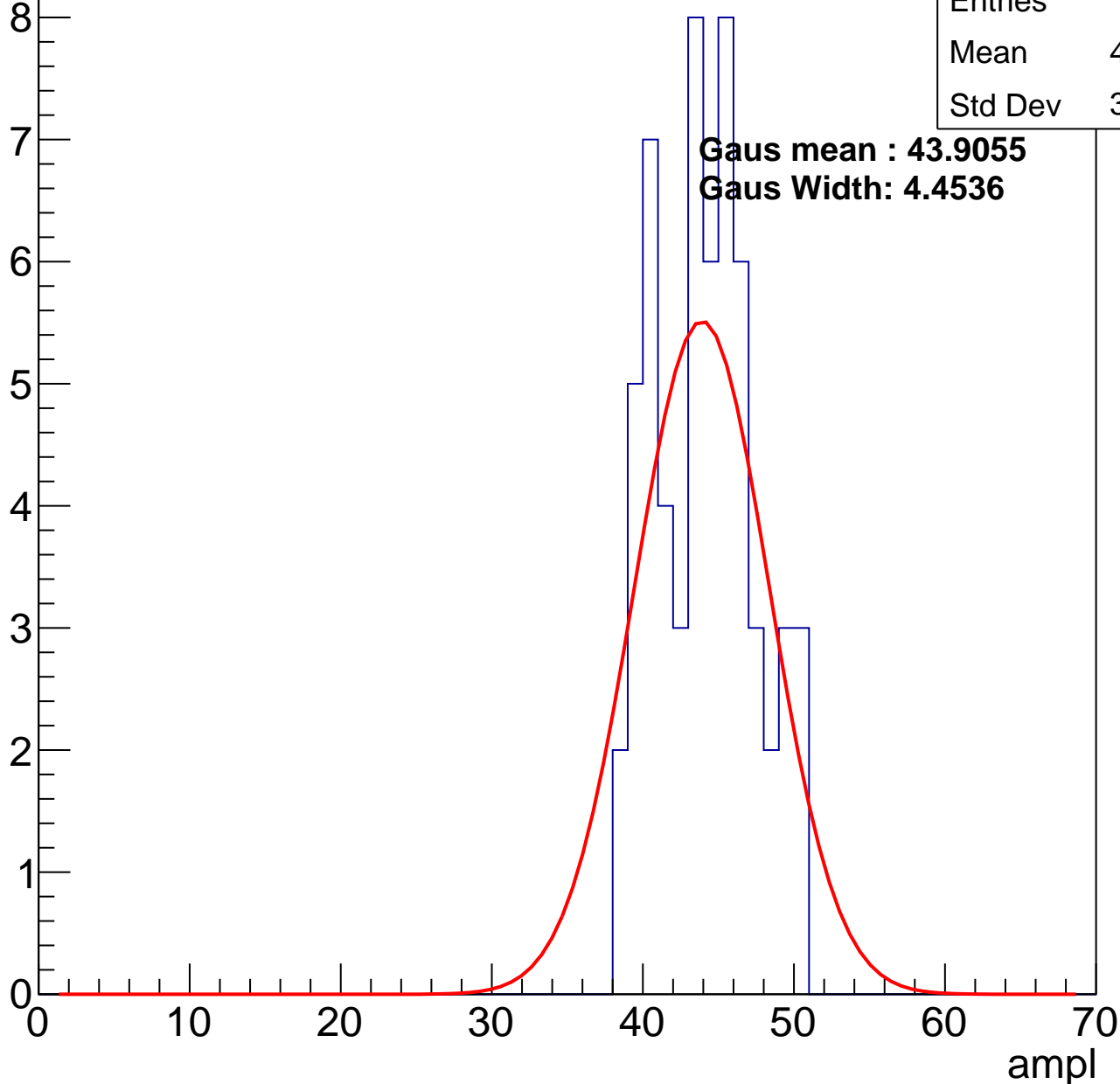
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 60    |
| Mean    | 43.65 |
| Std Dev | 3.245 |

**Gaus mean : 43.9055**

**Gaus Width: 4.4536**

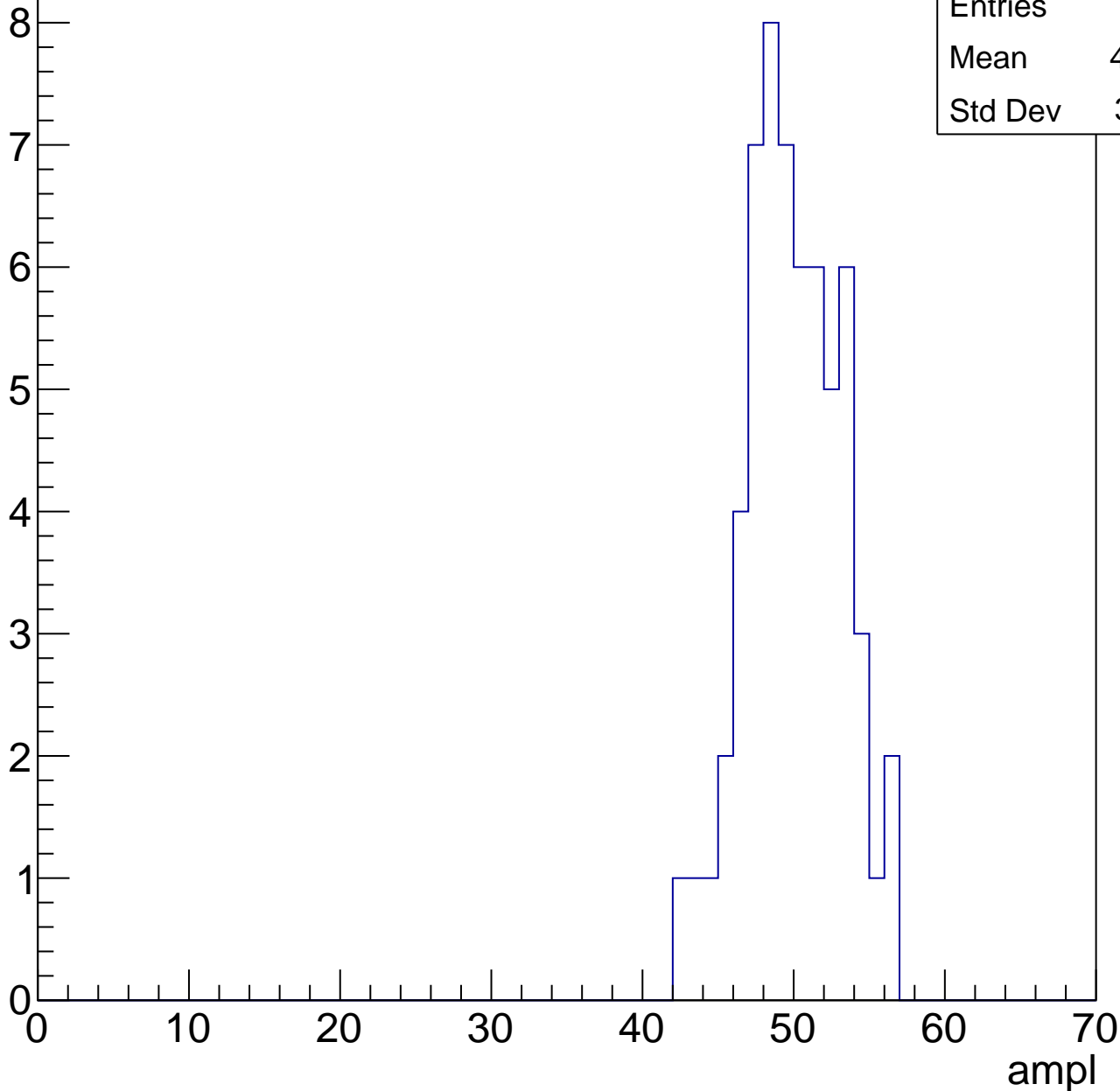


# B0L001S, U2-ch31, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 60    |
| Mean    | 49.53 |
| Std Dev | 3.101 |

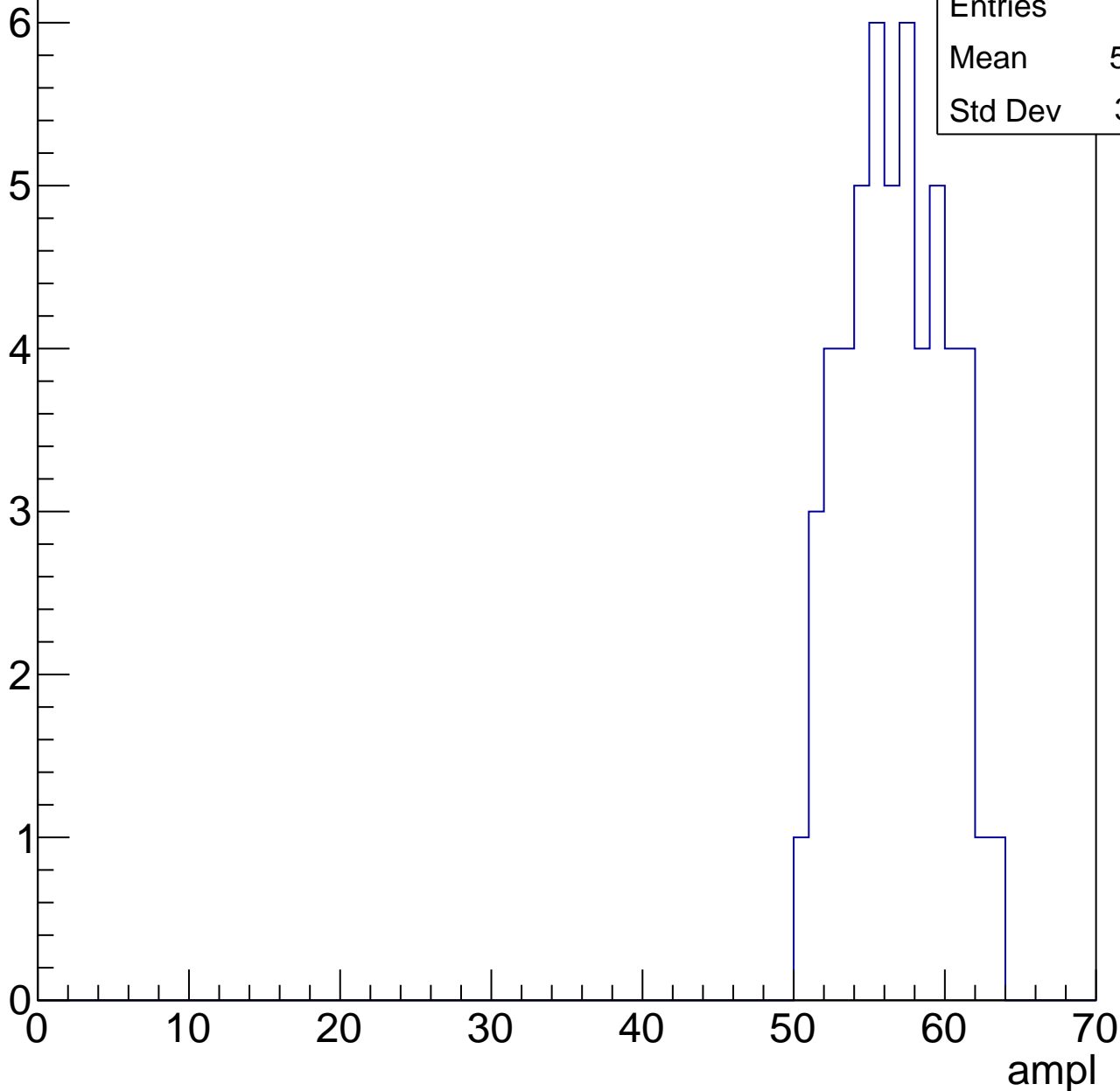


# B0L001S, U2-ch31, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 53    |
| Mean    | 56.25 |
| Std Dev | 3.221 |

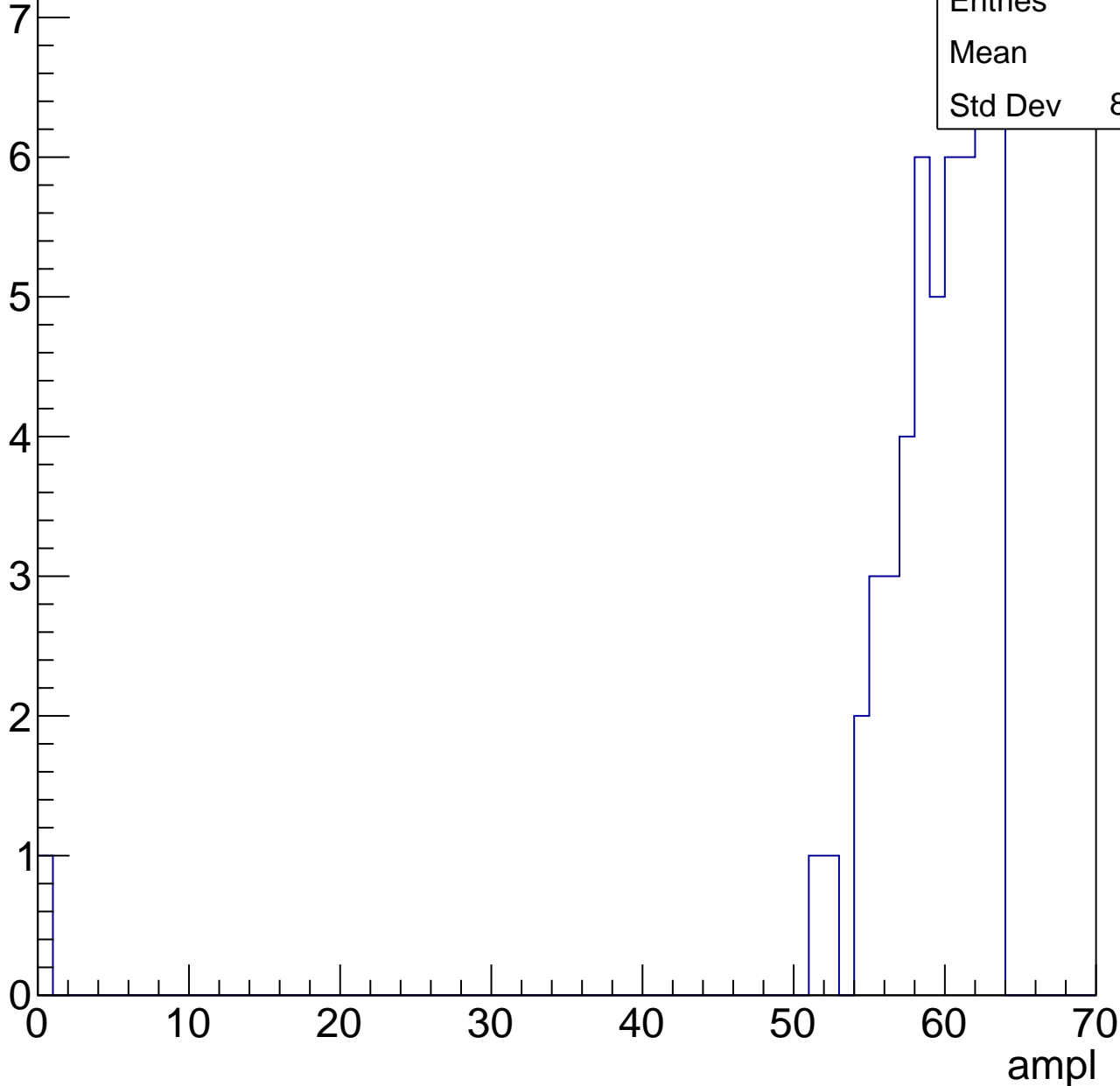


# B0L001S, U2-ch31, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 52    |
| Mean    | 58    |
| Std Dev | 8.654 |



# B0L001S, U2-ch31, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch31, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 2 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch32, adc0

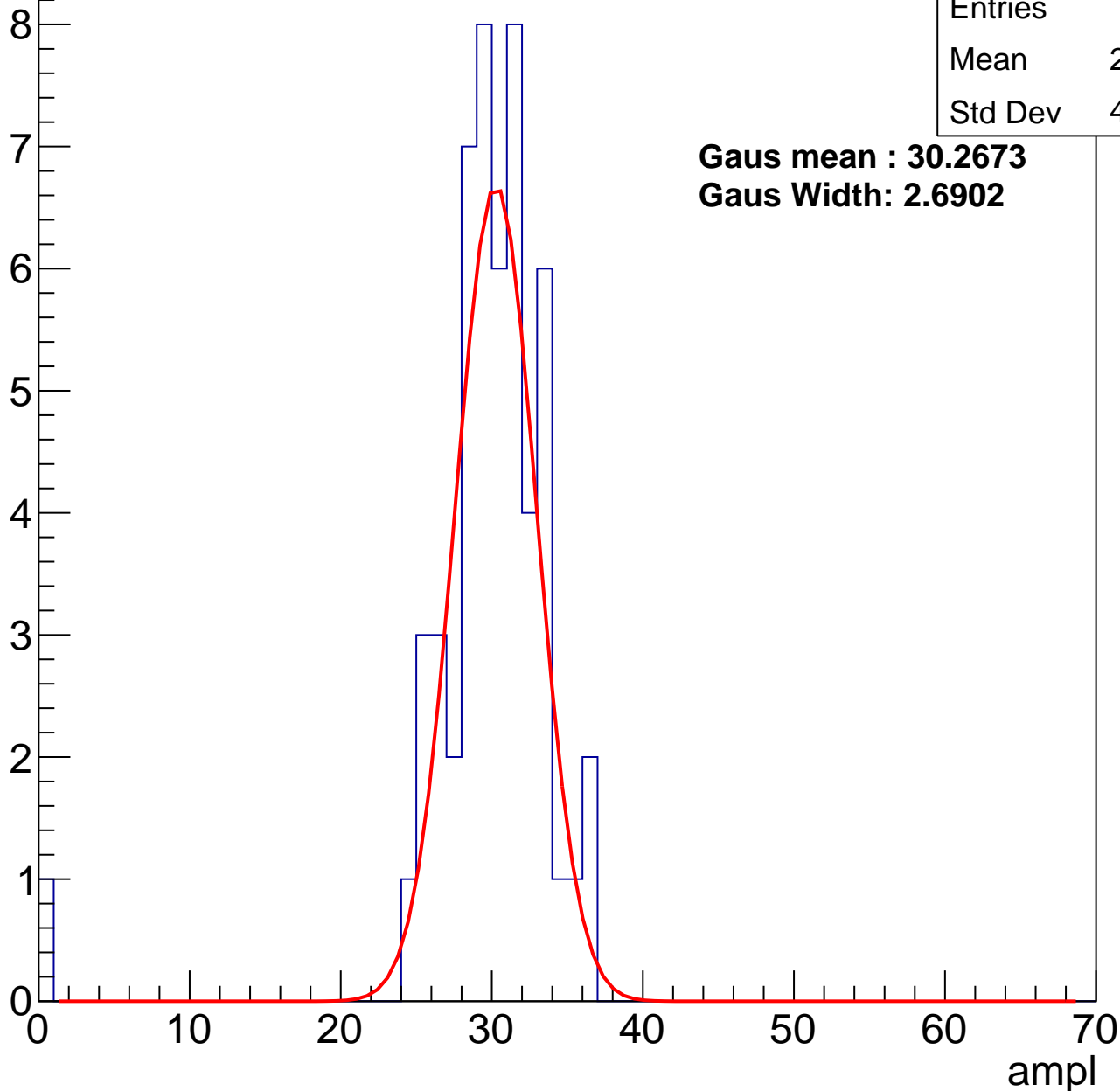
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 53    |
| Mean    | 29.32 |
| Std Dev | 4.913 |

**Gaus mean : 30.2673**

**Gaus Width: 2.6902**



# B0L001S, U2-ch32, adc1

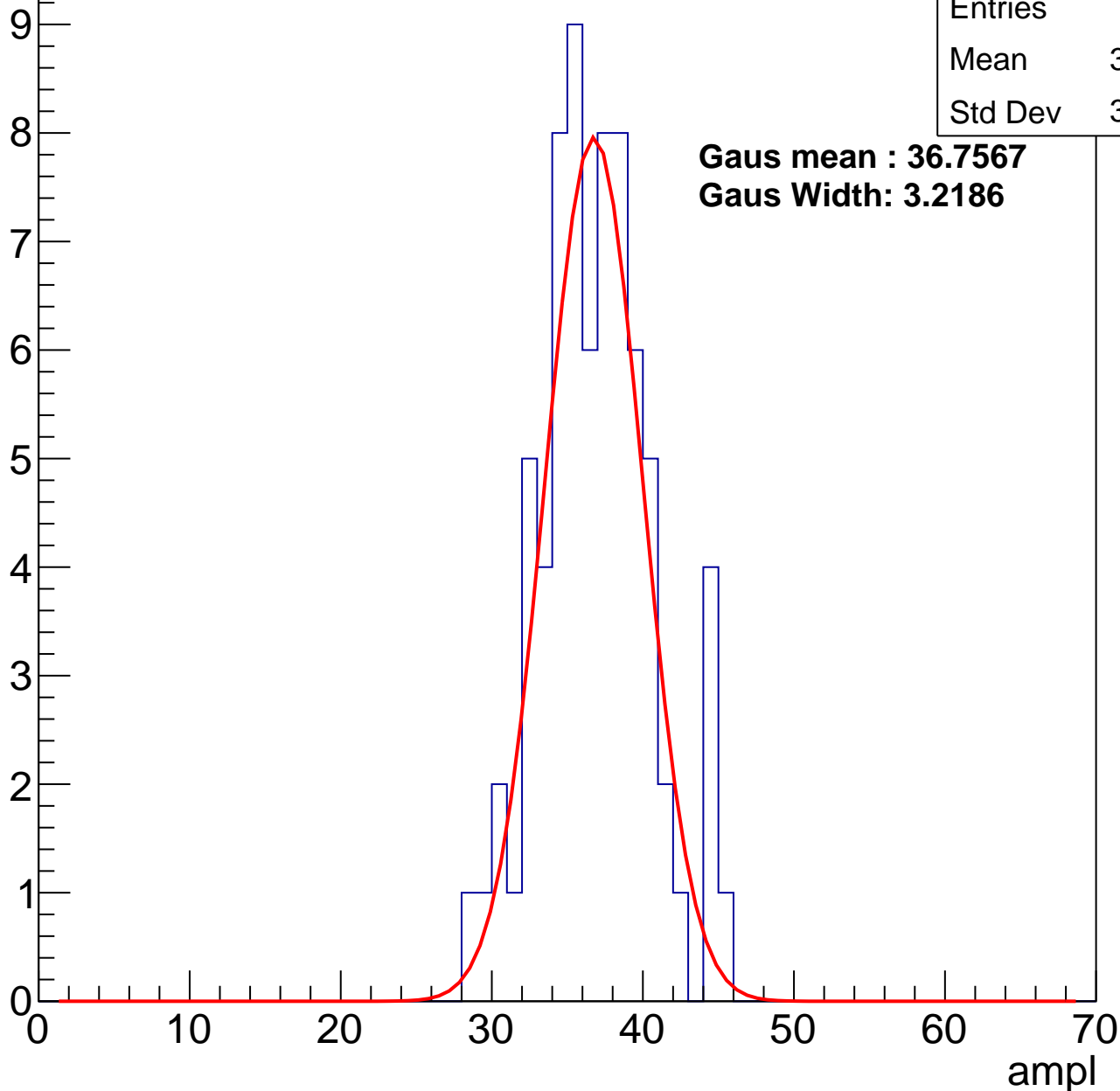
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 72    |
| Mean    | 36.42 |
| Std Dev | 3.635 |

**Gaus mean : 36.7567**

**Gaus Width: 3.2186**



# B0L001S, U2-ch32, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 69    |
| Mean    | 42.8  |
| Std Dev | 3.553 |

**Gaus mean : 42.9383**

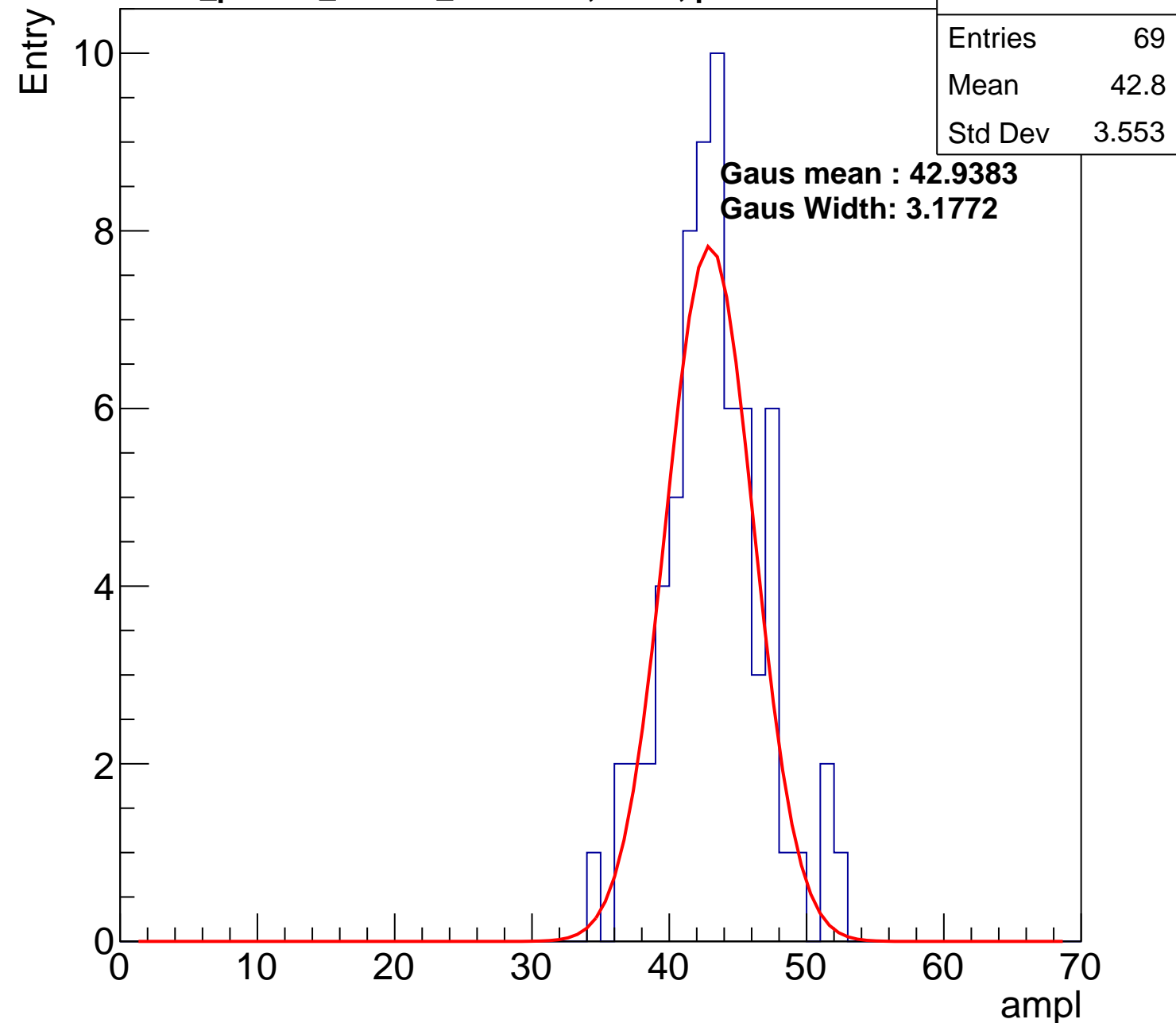
**Gaus Width: 3.1772**

Entry

10  
8  
6  
4  
2  
0

ampl

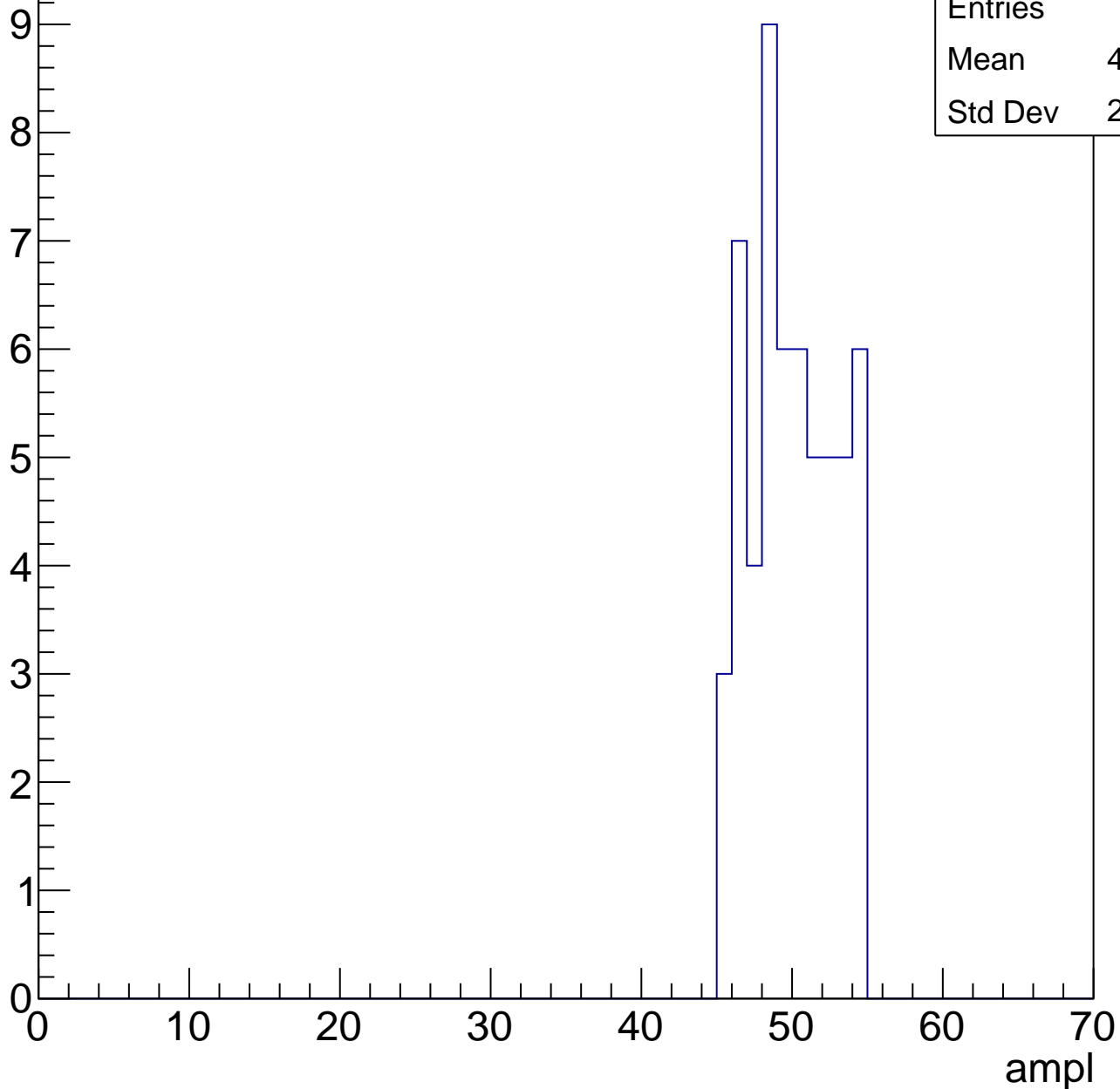
0 10 20 30 40 50 60 70



# B0L001S, U2-ch32, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

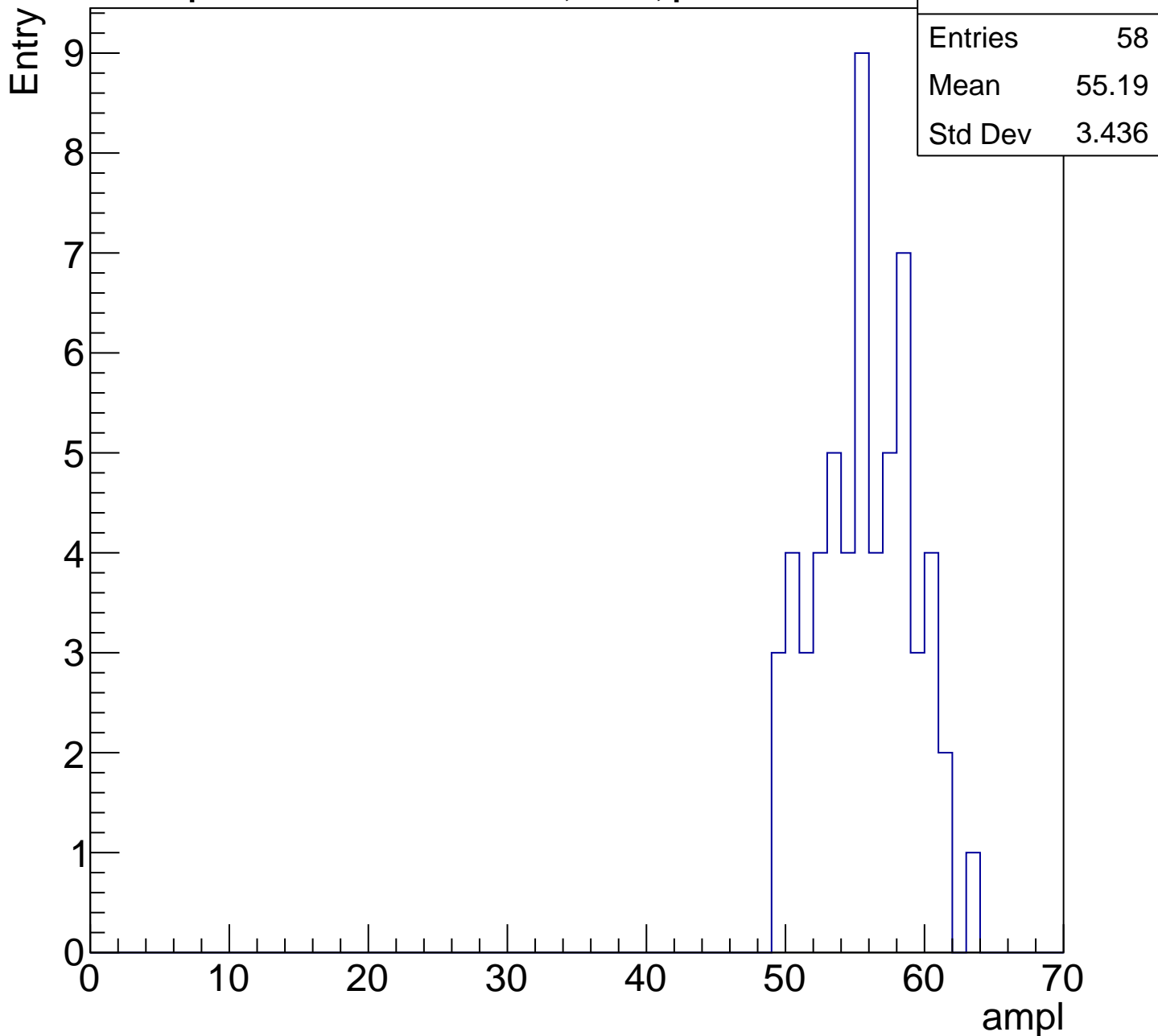
Entry



|         |       |
|---------|-------|
| Entries | 56    |
| Mean    | 49.55 |
| Std Dev | 2.738 |

# B0L001S, U2-ch32, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

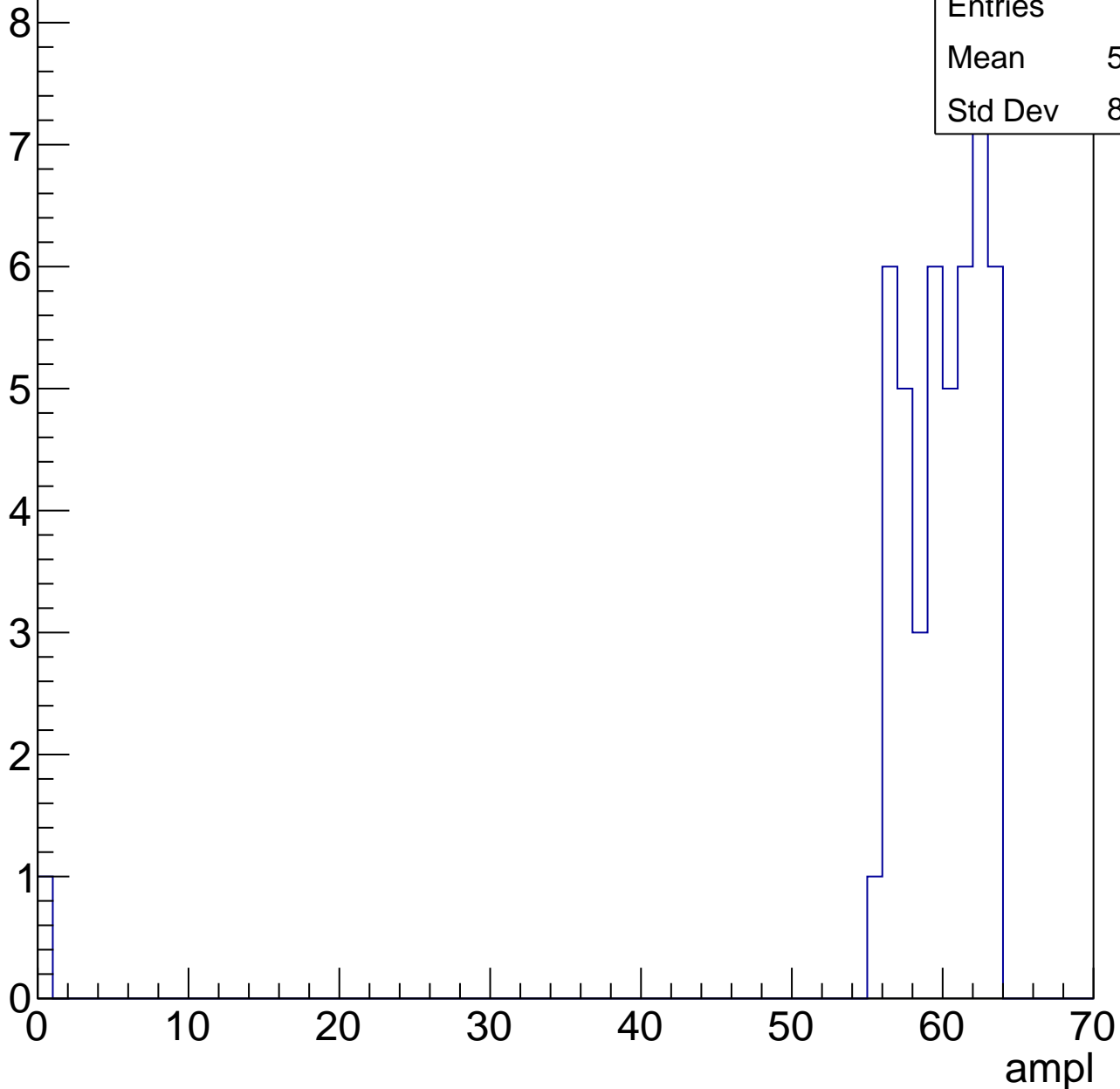


# B0L001S, U2-ch32, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

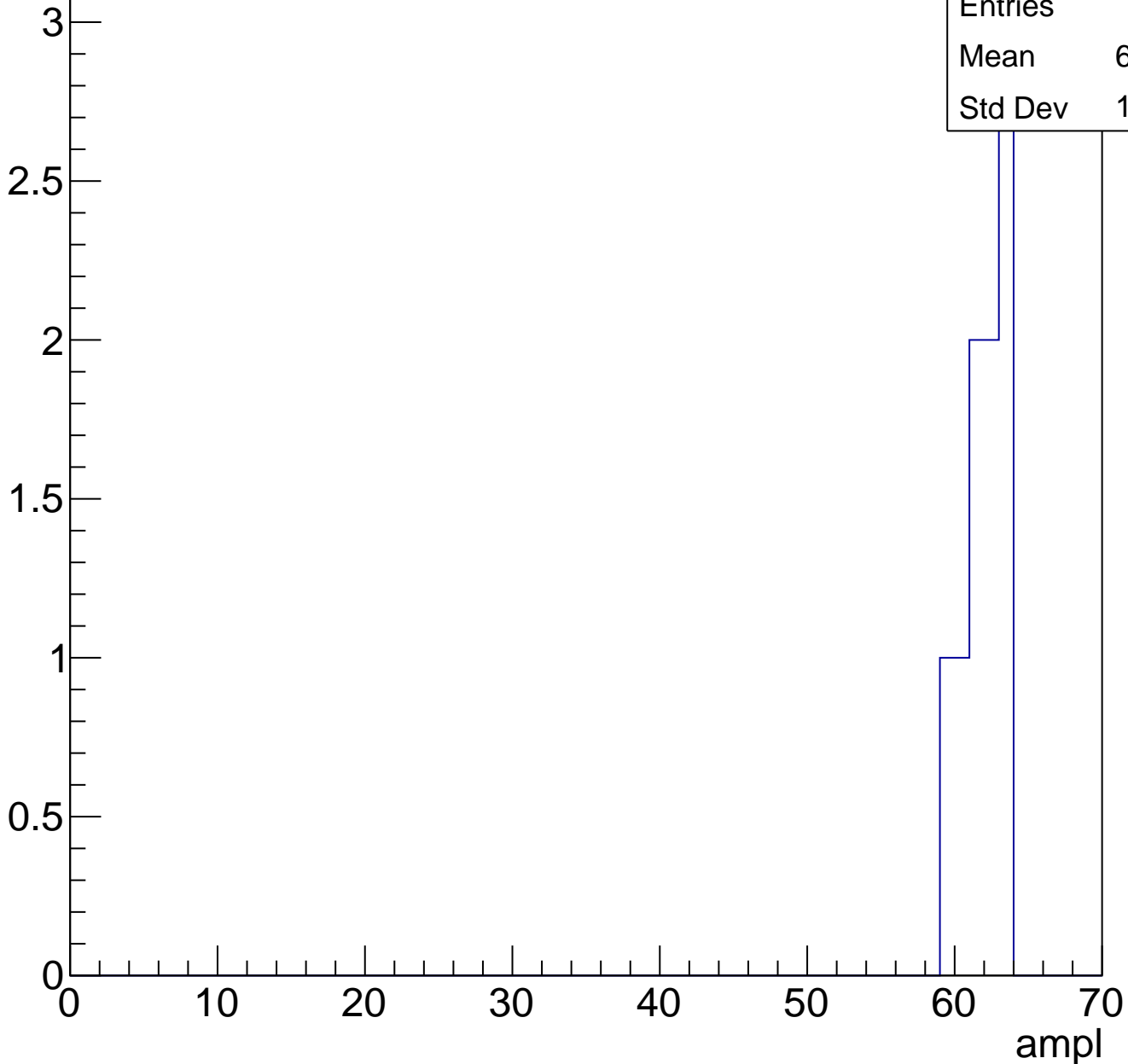
|         |       |
|---------|-------|
| Entries | 47    |
| Mean    | 58.38 |
| Std Dev | 8.936 |



# B0L001S, U2-ch32, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch32, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U2-ch33, adc0

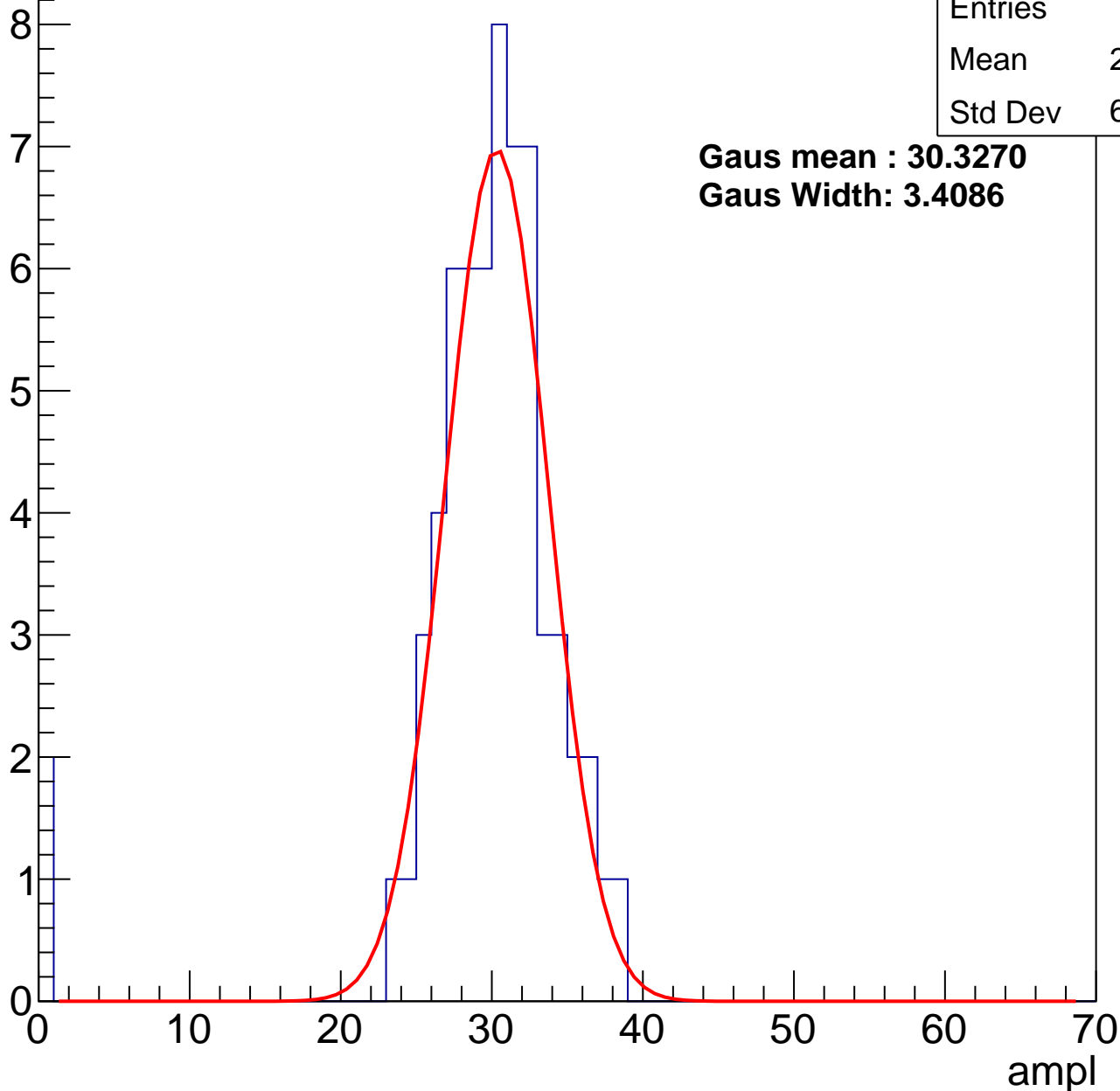
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 63    |
| Mean    | 29.03 |
| Std Dev | 6.164 |

**Gaus mean : 30.3270**

**Gaus Width: 3.4086**



# B0L001S, U2-ch33, adc1

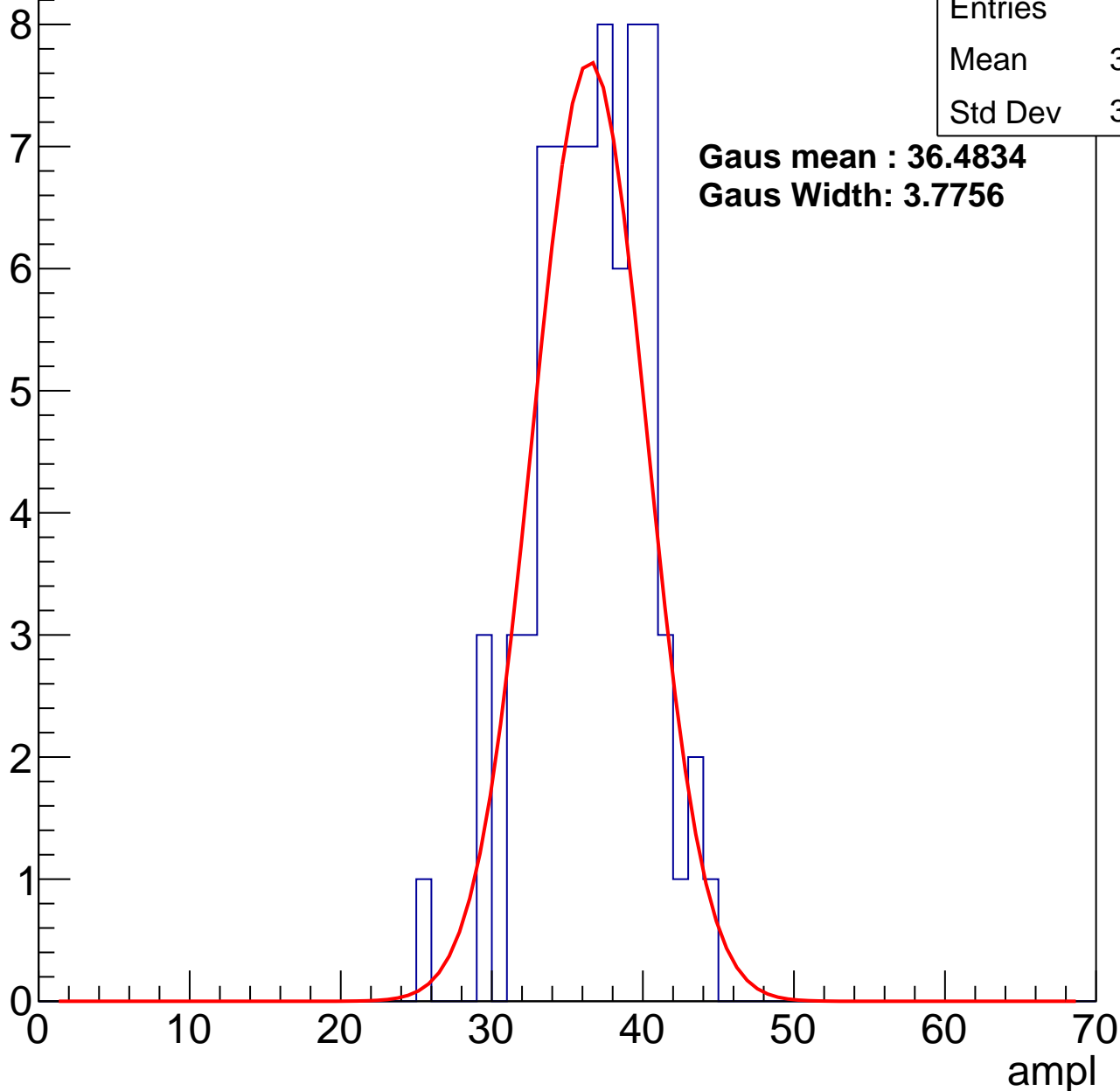
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 75    |
| Mean    | 36.24 |
| Std Dev | 3.633 |

**Gaus mean : 36.4834**

**Gaus Width: 3.7756**



# B0L001S, U2-ch33, adc2

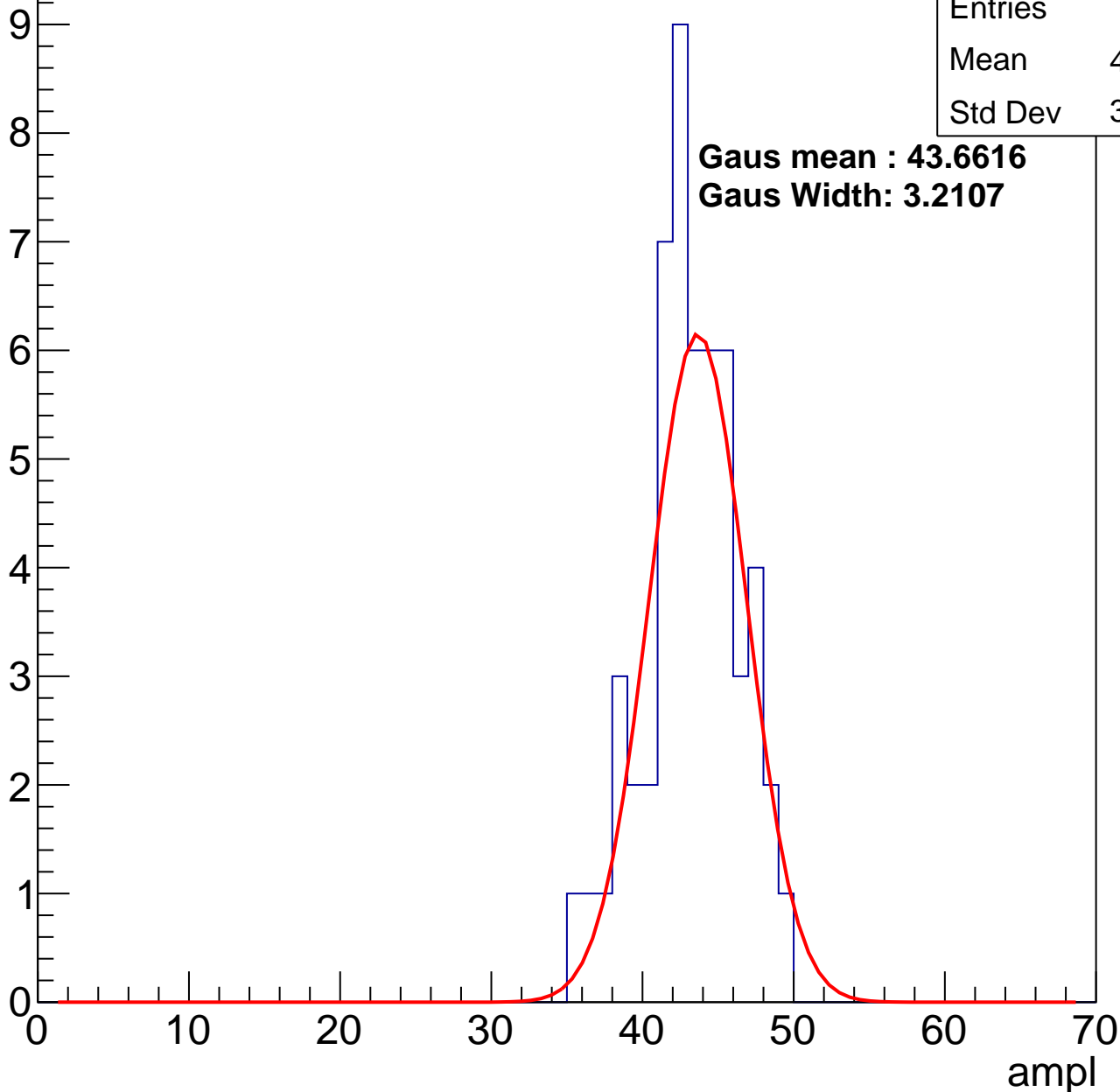
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 54    |
| Mean    | 42.74 |
| Std Dev | 3.086 |

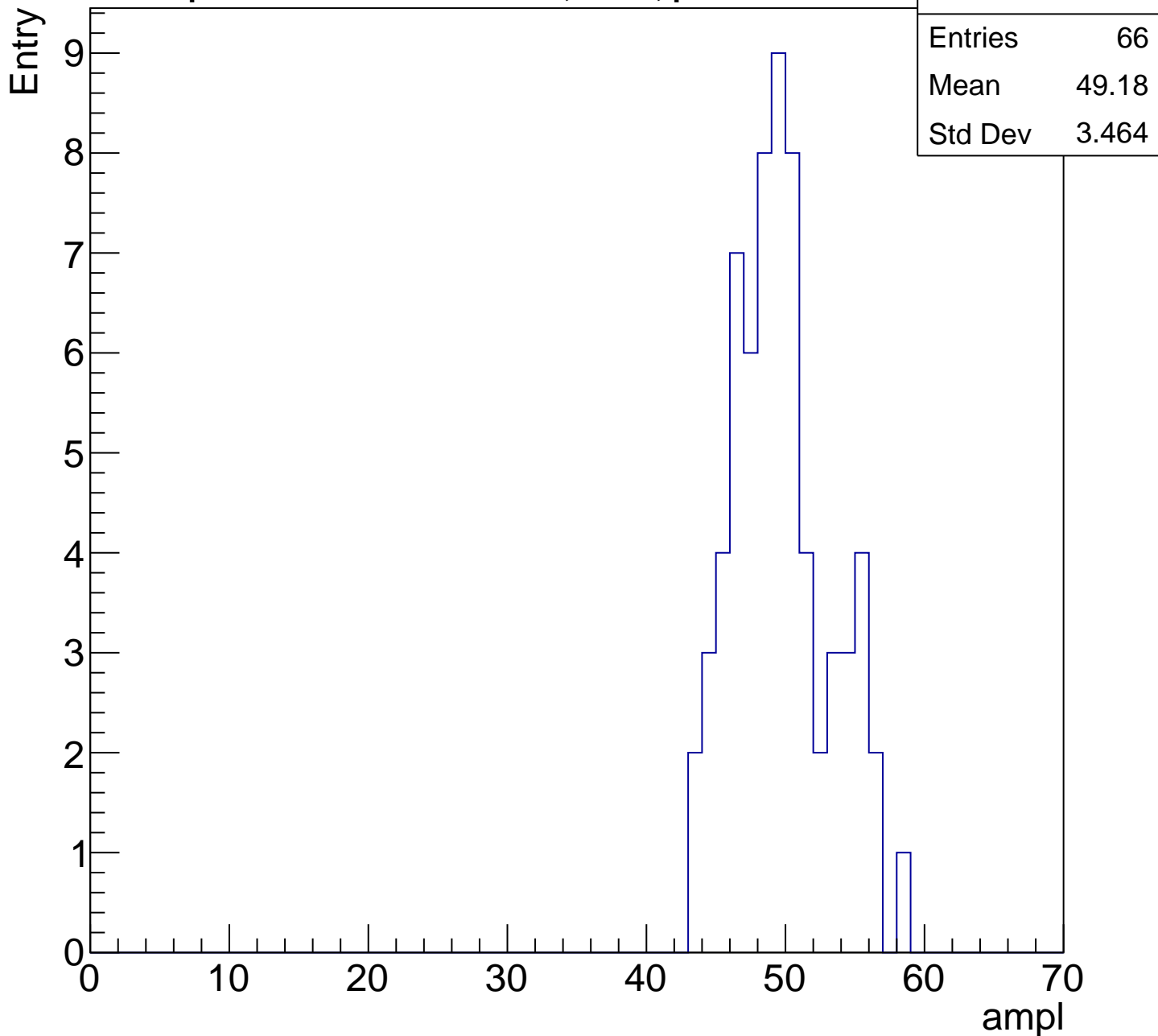
**Gaus mean : 43.6616**

**Gaus Width: 3.2107**



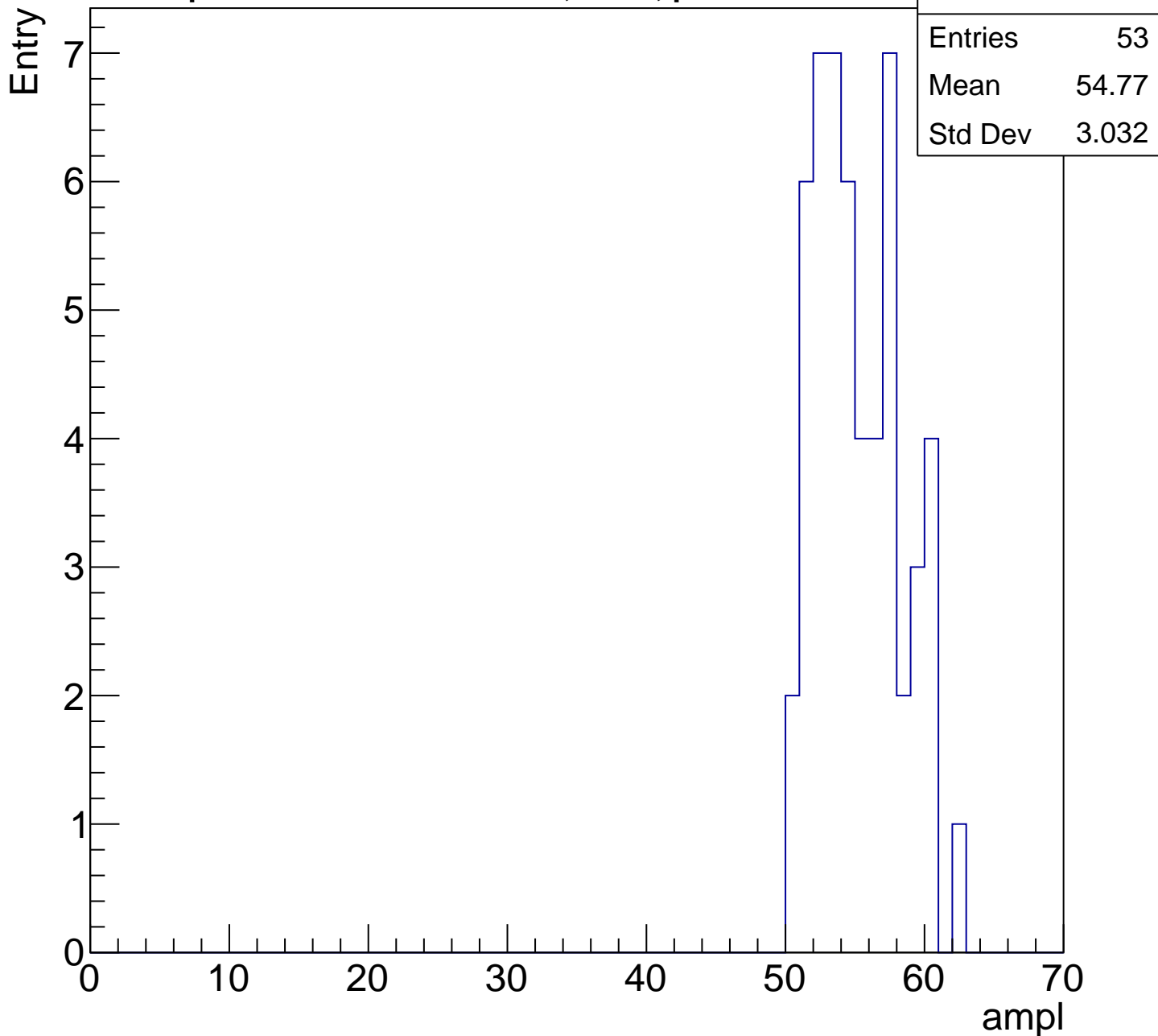
# B0L001S, U2-ch33, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U2-ch33, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

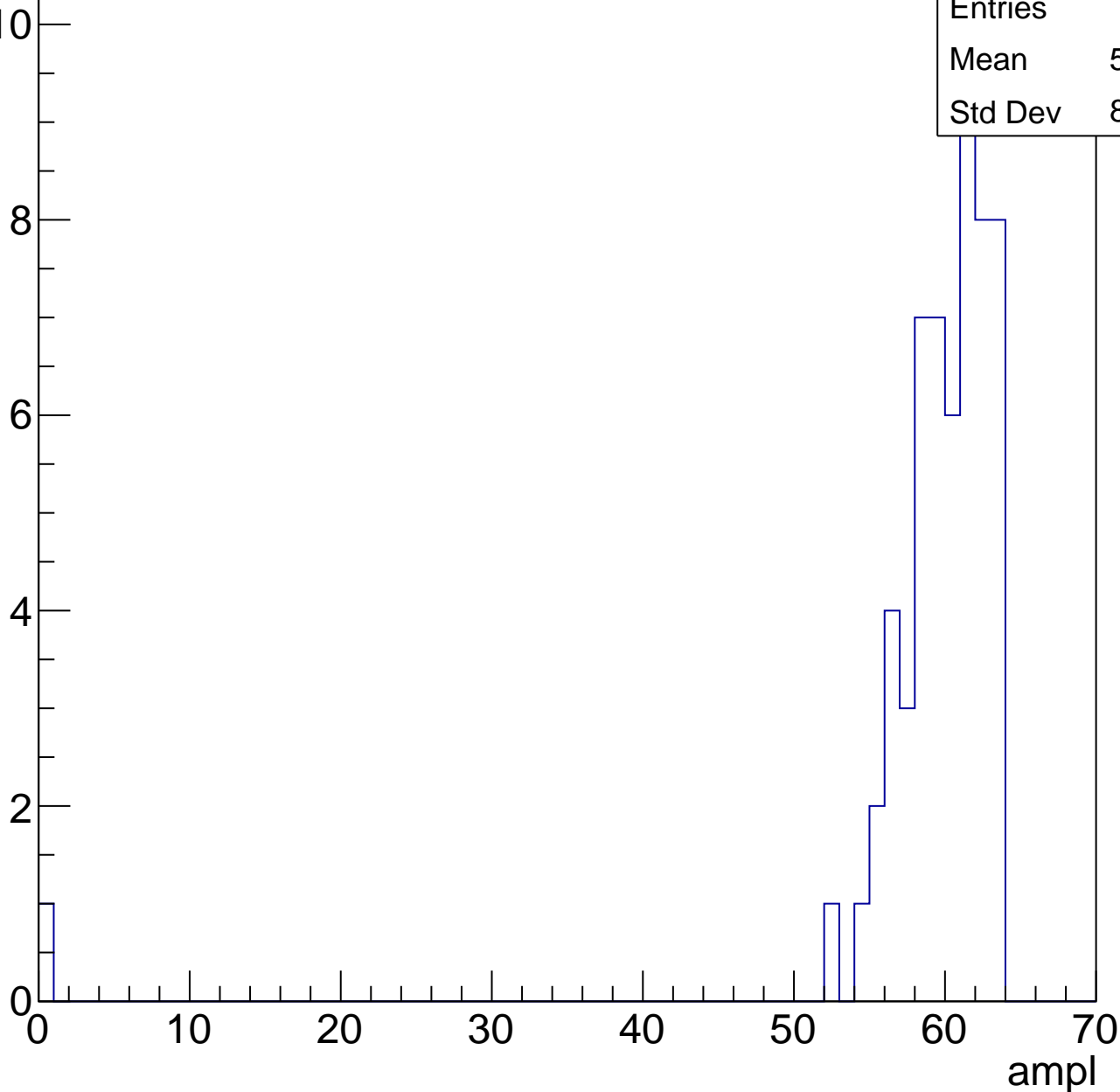


# B0L001S, U2-ch33, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 58    |
| Mean    | 58.62 |
| Std Dev | 8.179 |



# B0L001S, U2-ch33, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch33, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 1 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch34, adc0

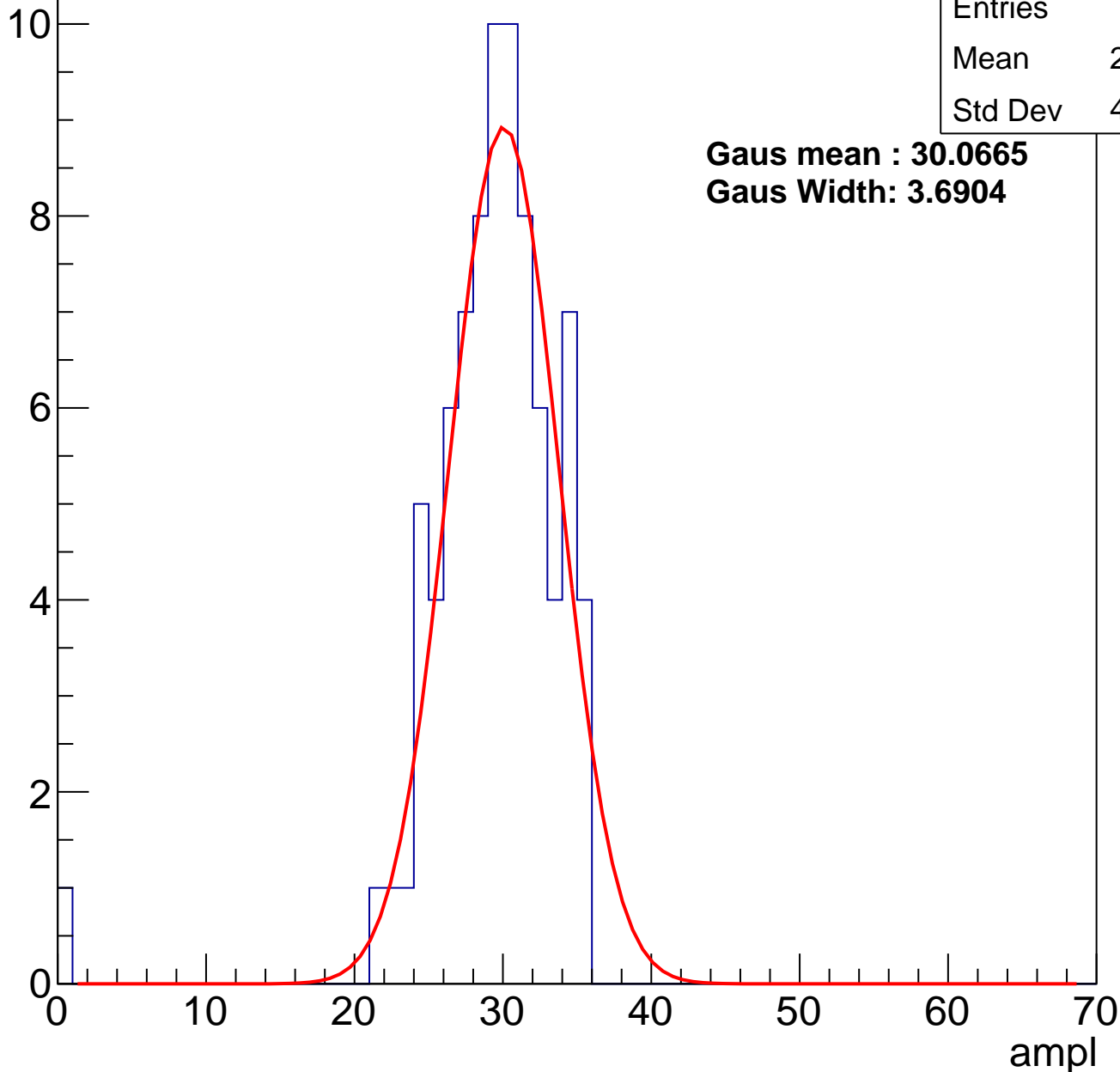
calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 83    |
| Mean    | 28.86 |
| Std Dev | 4.587 |

**Gaus mean : 30.0665**

**Gaus Width: 3.6904**

Entry



# B0L001S, U2-ch34, adc1

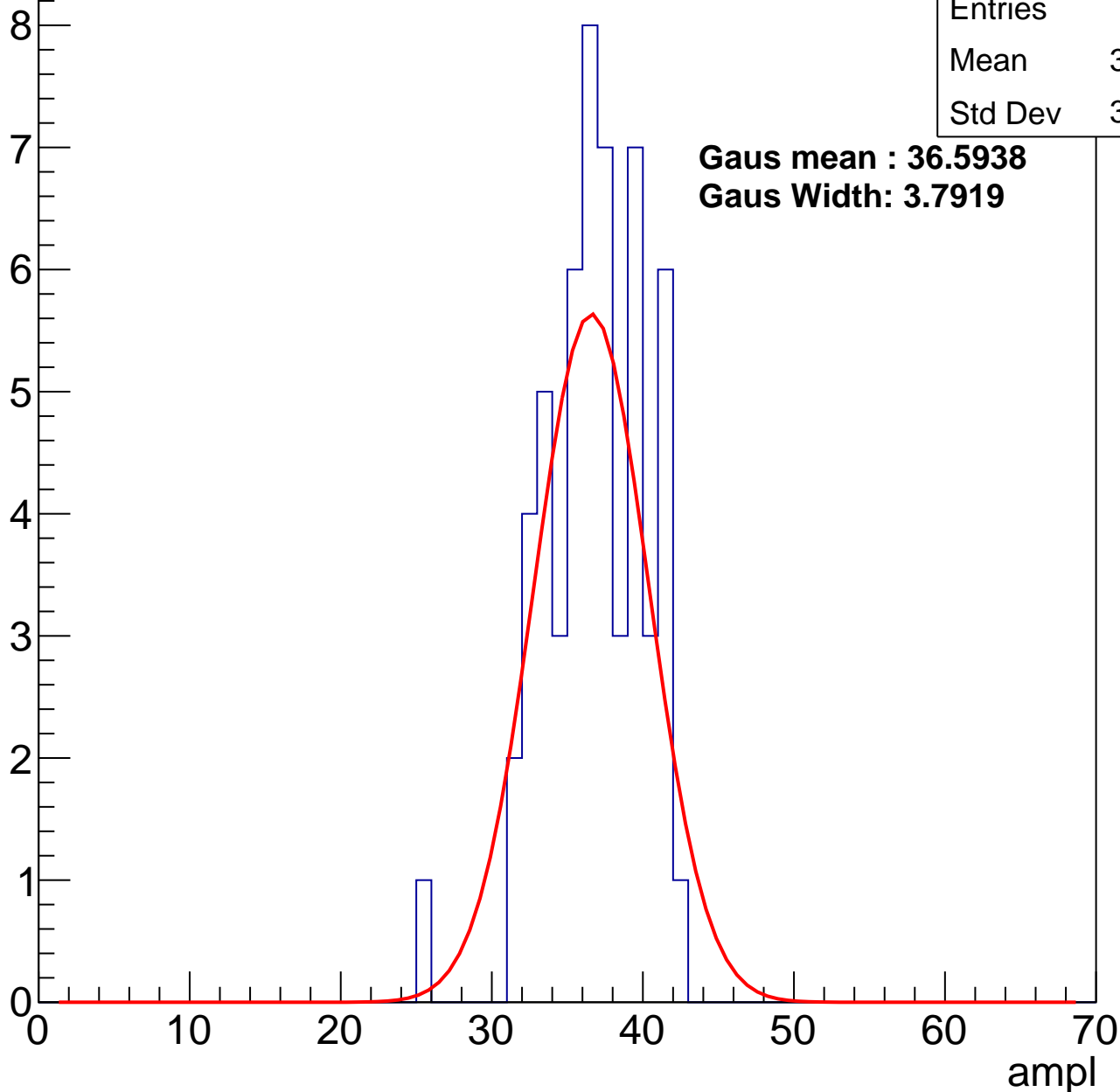
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 56    |
| Mean    | 36.32 |
| Std Dev | 3.296 |

**Gaus mean : 36.5938**

**Gaus Width: 3.7919**



# B0L001S, U2-ch34, adc2

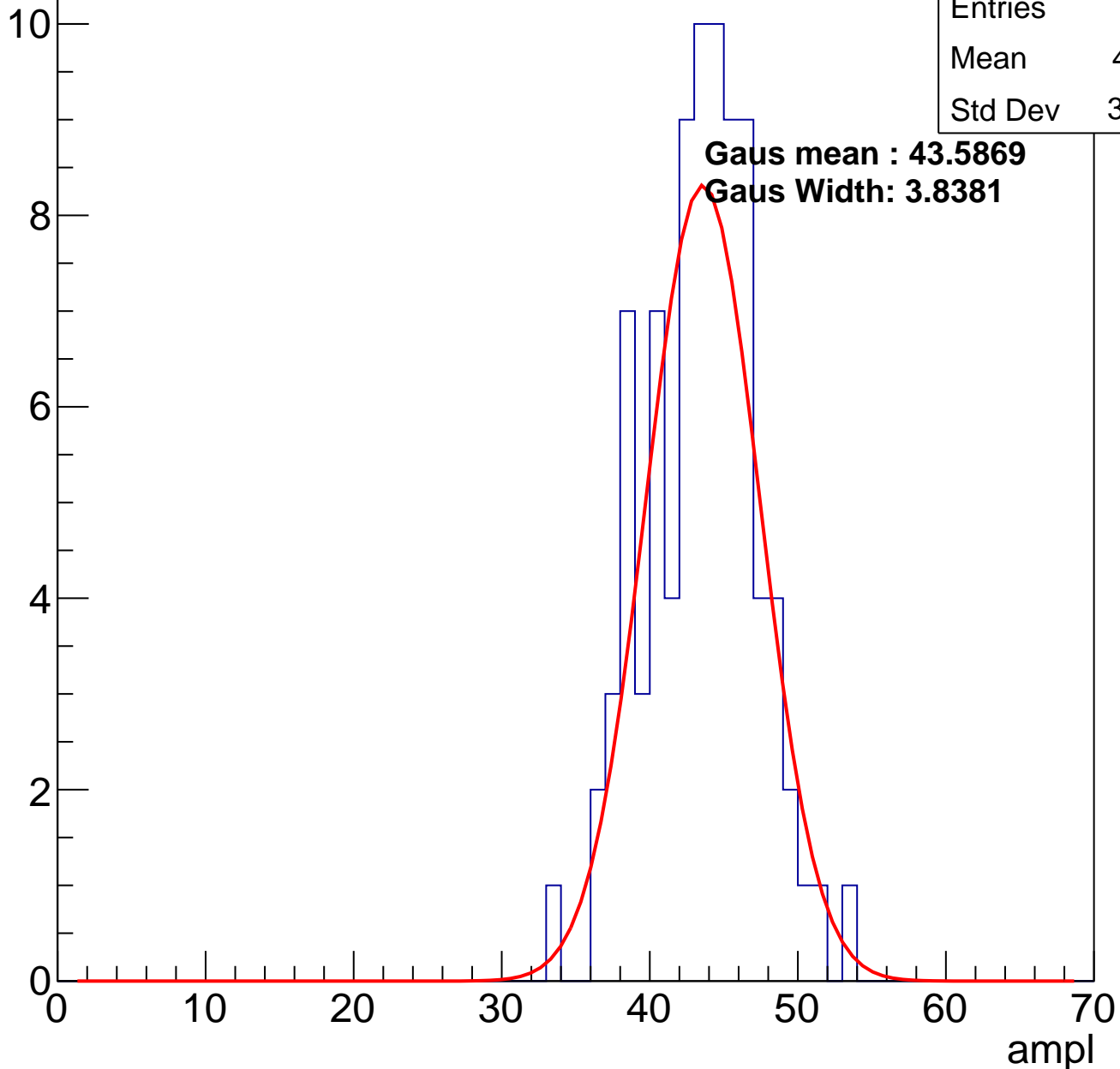
calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 87    |
| Mean    | 43.01 |
| Std Dev | 3.703 |

**Gaus mean : 43.5869**

**Gaus Width: 3.8381**

Entry

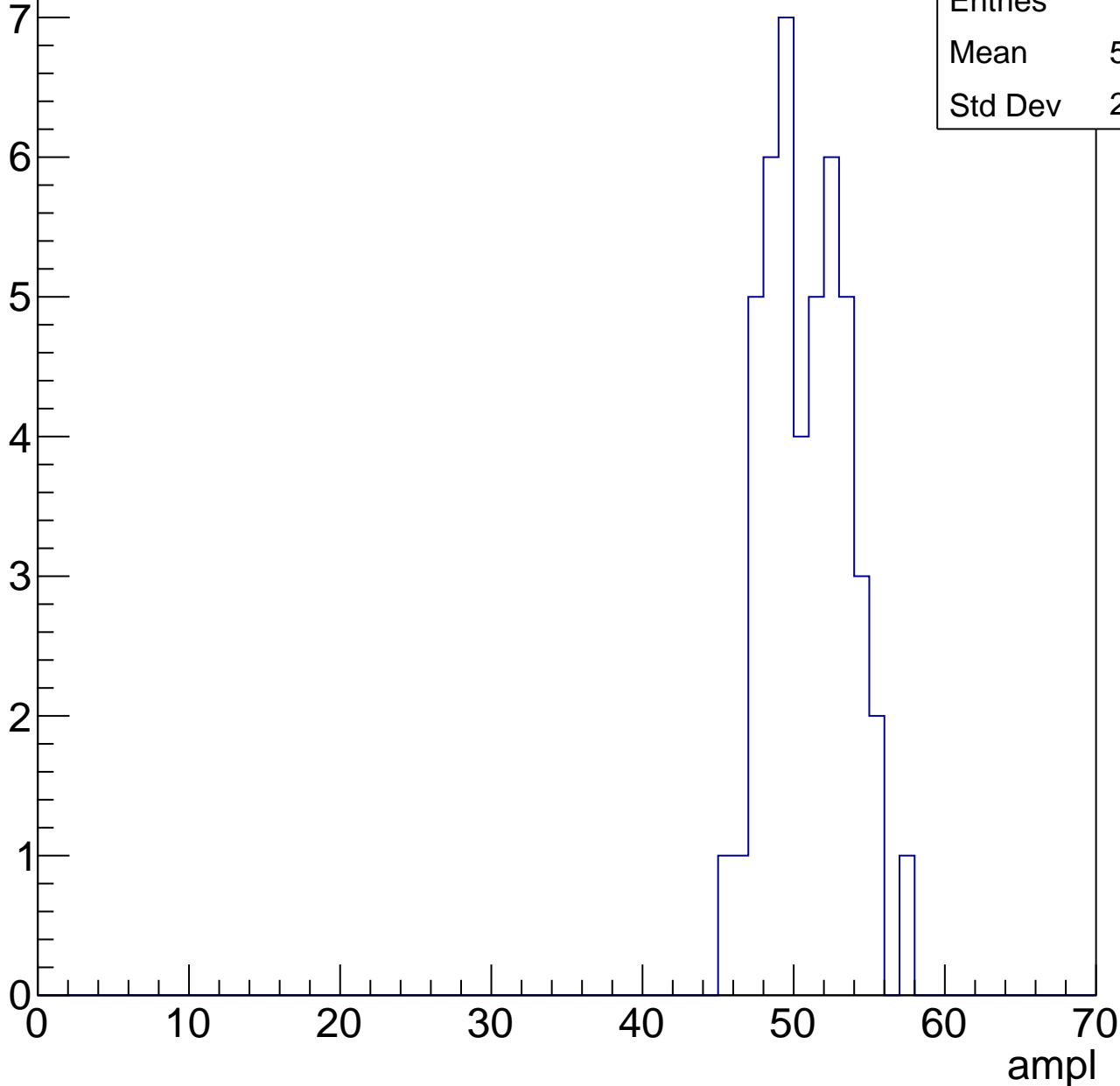


# B0L001S, U2-ch34, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 46    |
| Mean    | 50.39 |
| Std Dev | 2.682 |

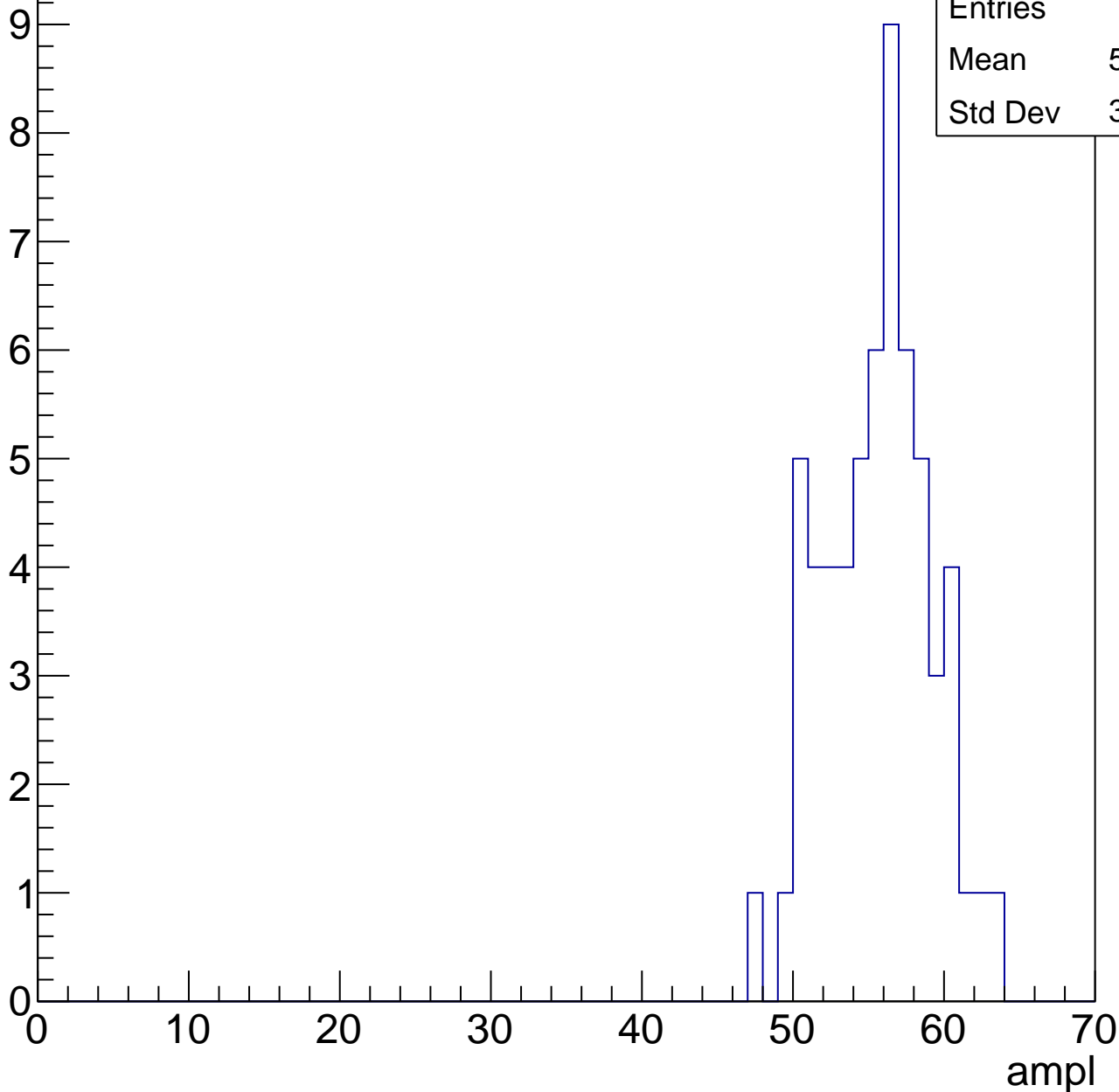


# B0L001S, U2-ch34, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 60    |
| Mean    | 55.15 |
| Std Dev | 3.463 |



# B0L001S, U2-ch34, adc5

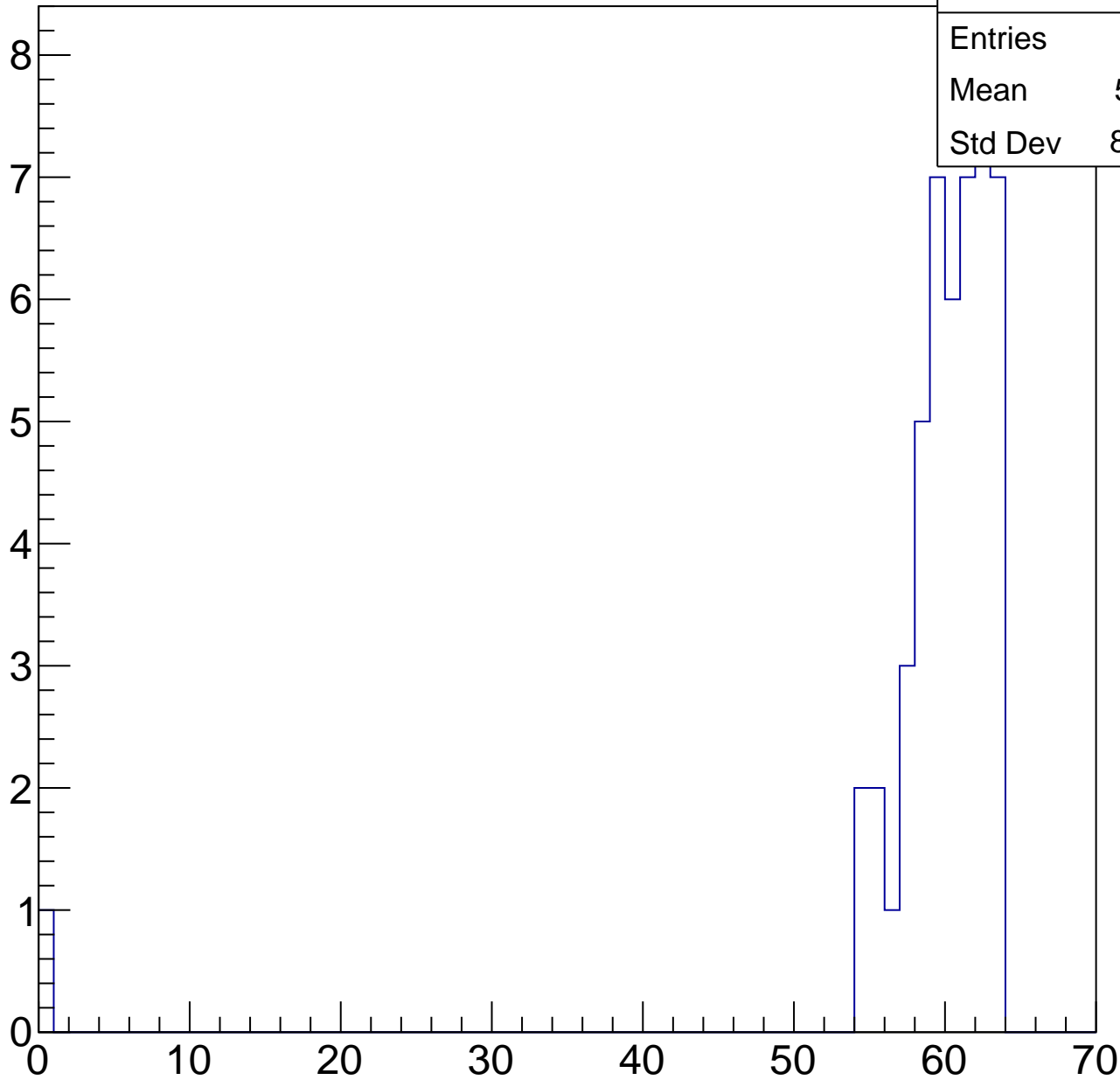
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

|         |       |
|---------|-------|
| Entries | 49    |
| Mean    | 58.61 |
| Std Dev | 8.806 |

ampl



# B0L001S, U2-ch34, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

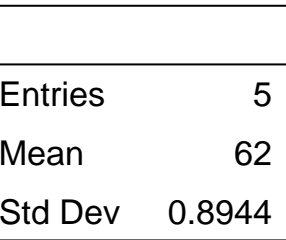
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

|         |        |
|---------|--------|
| Entries | 5      |
| Mean    | 62     |
| Std Dev | 0.8944 |

0 10 20 30 40 50 60 70

ampl





# B0L001S, U2-ch34, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U2-ch35, adc0

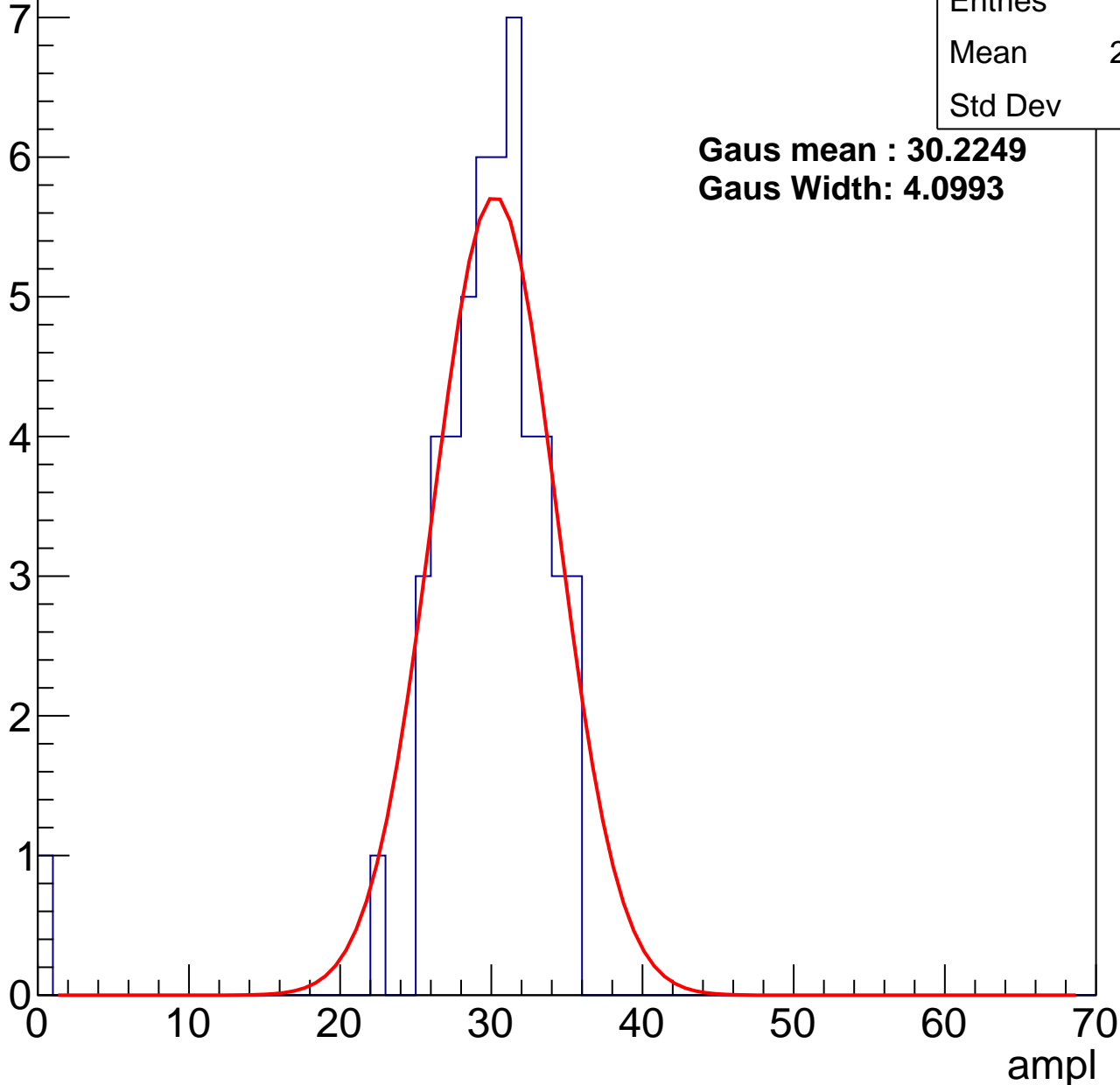
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 51    |
| Mean    | 29.16 |
| Std Dev | 5.07  |

**Gaus mean : 30.2249**

**Gaus Width: 4.0993**



# B0L001S, U2-ch35, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 79    |
| Mean    | 35.89 |
| Std Dev | 3.765 |

**Gaus mean : 36.5580**

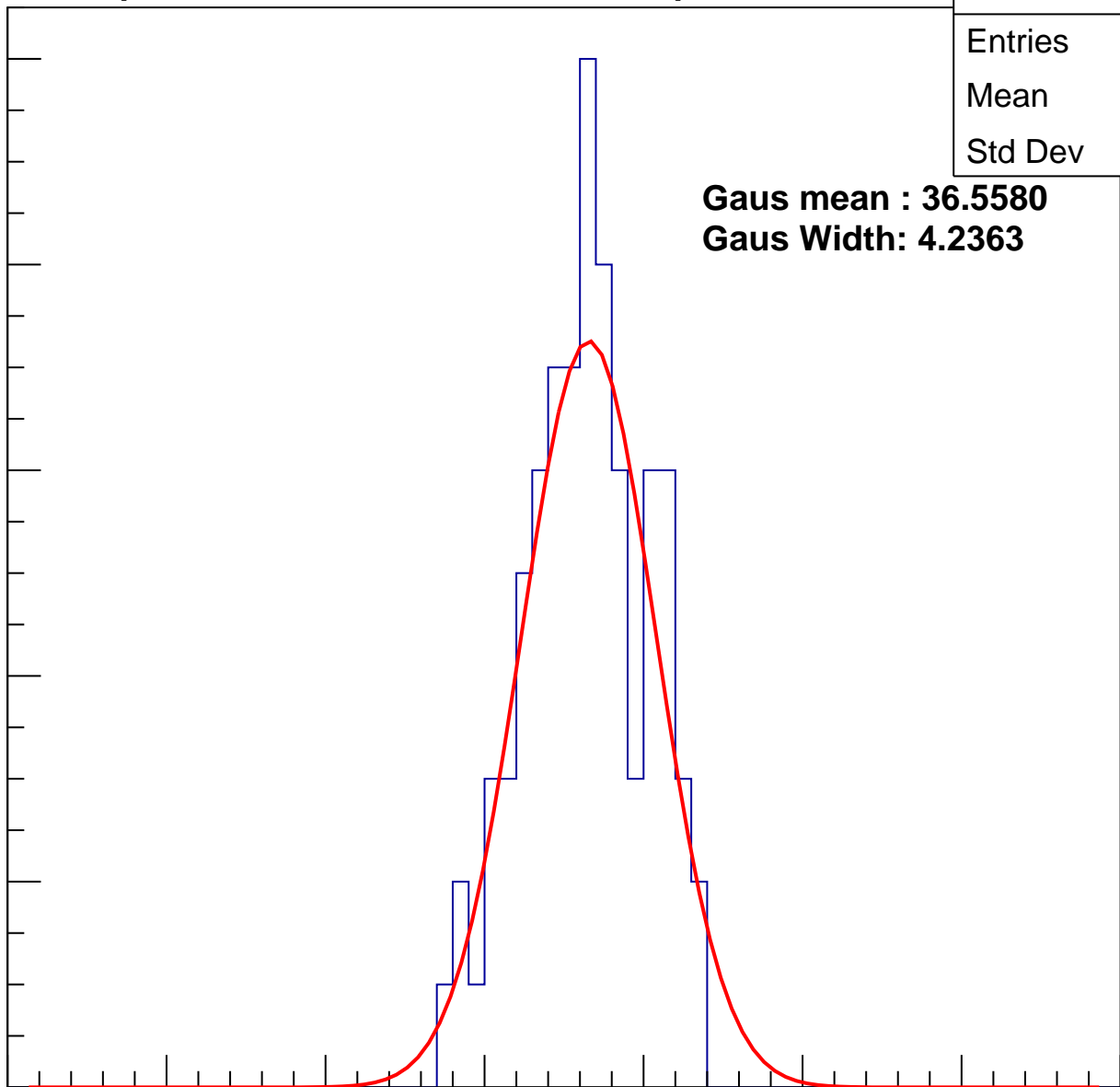
**Gaus Width: 4.2363**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U2-ch35, adc2

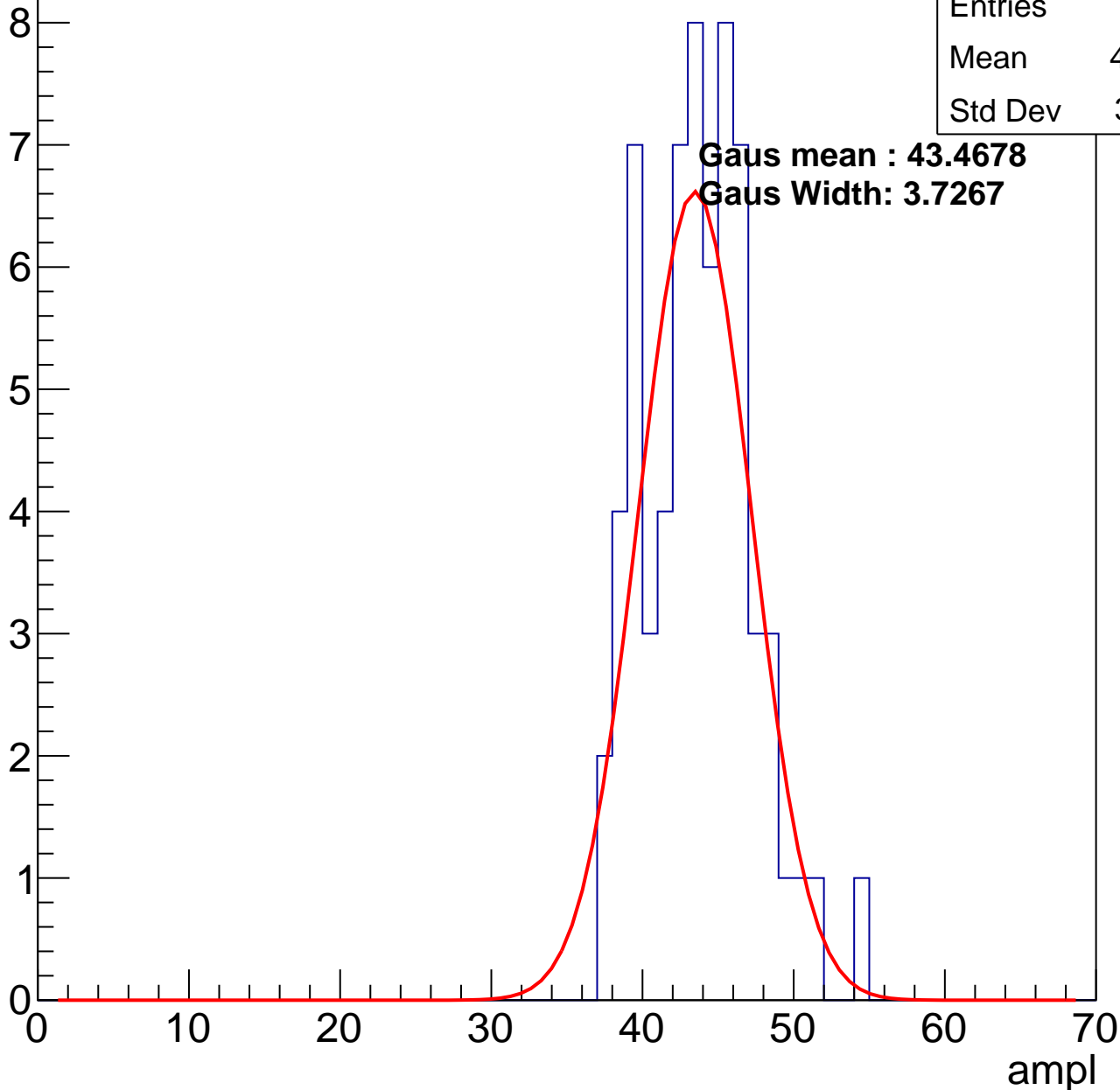
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 66    |
| Mean    | 43.27 |
| Std Dev | 3.531 |

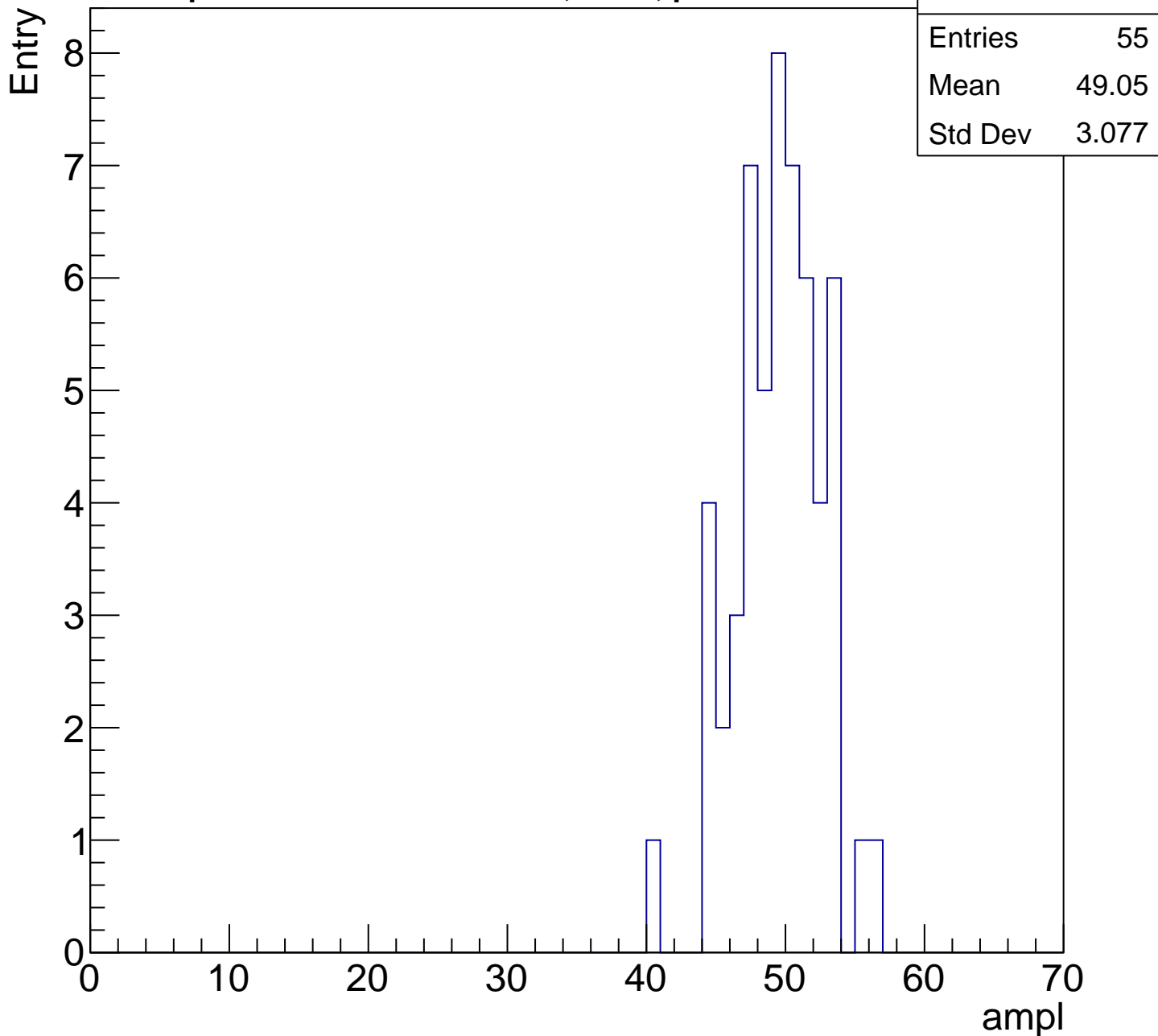
**Gaus mean : 43.4678**

**Gaus Width: 3.7267**



# B0L001S, U2-ch35, adc3

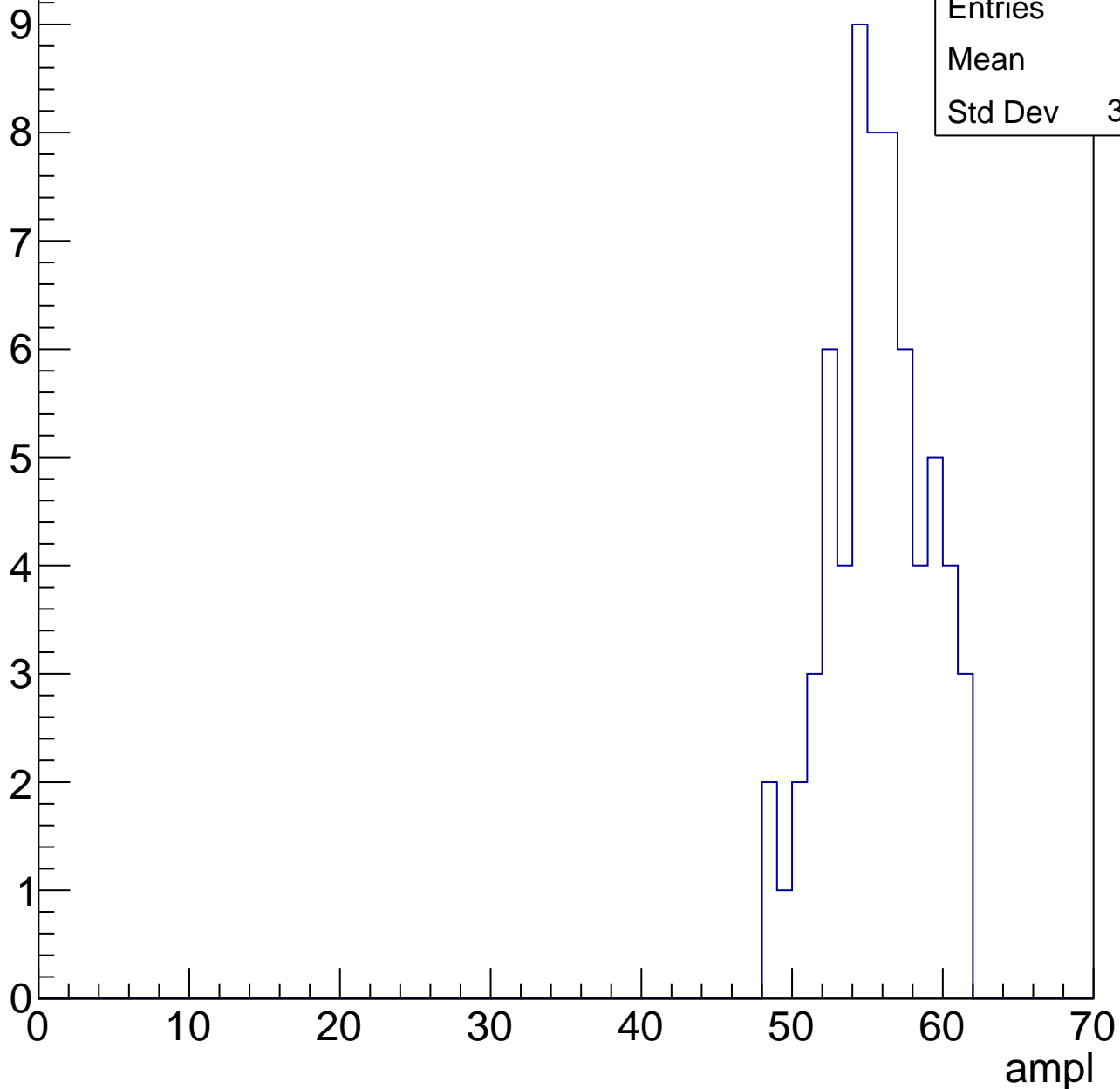
calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U2-ch35, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

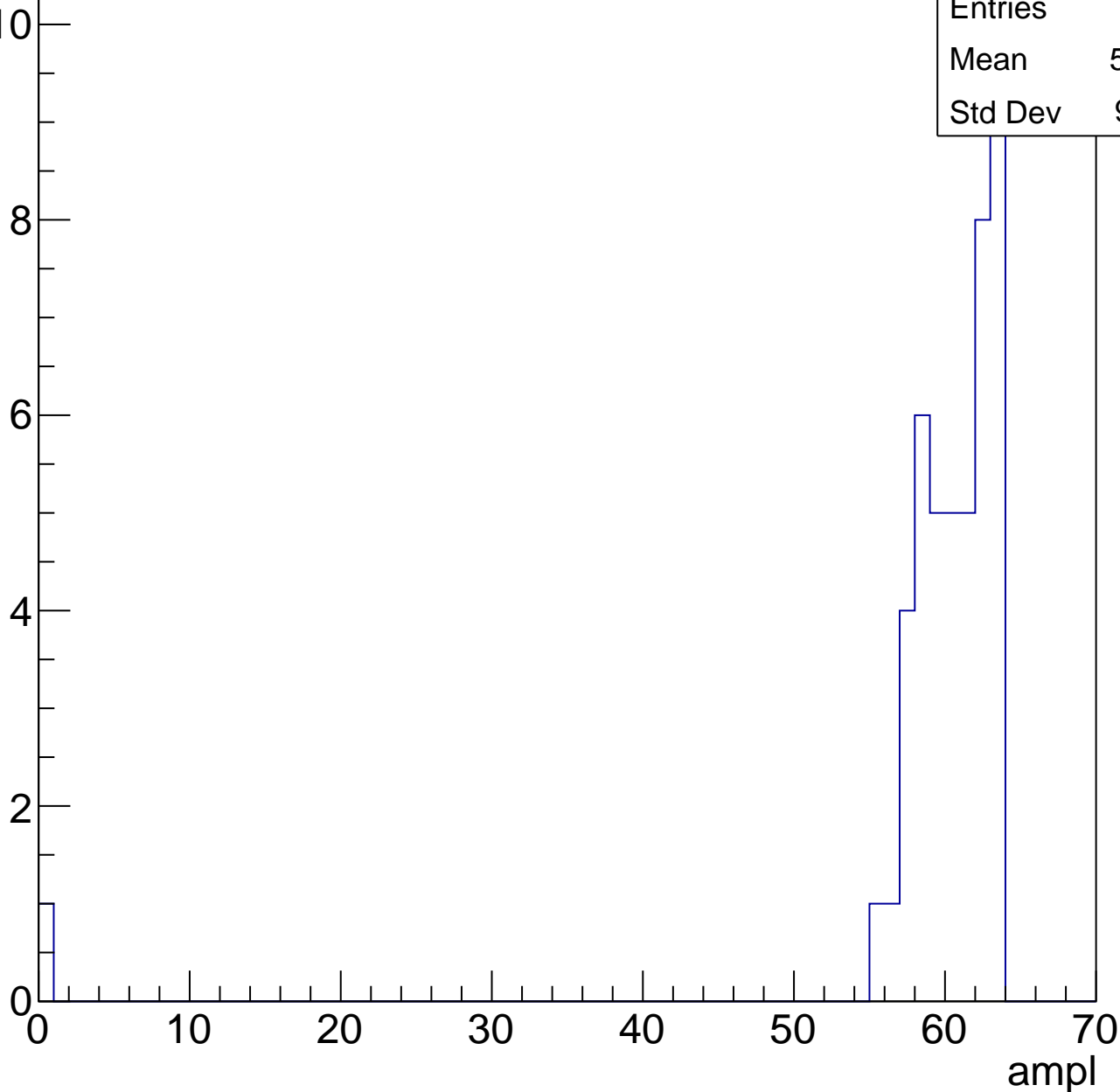


# B0L001S, U2-ch35, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 46    |
| Mean    | 58.98 |
| Std Dev | 9.071 |



# B0L001S, U2-ch35, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

|         |        |
|---------|--------|
| Entries | 5      |
| Mean    | 61.2   |
| Std Dev | 0.7483 |

ampl

0 10 20 30 40 50 60 70



# B0L001S, U2-ch35, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 1 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch36, adc0

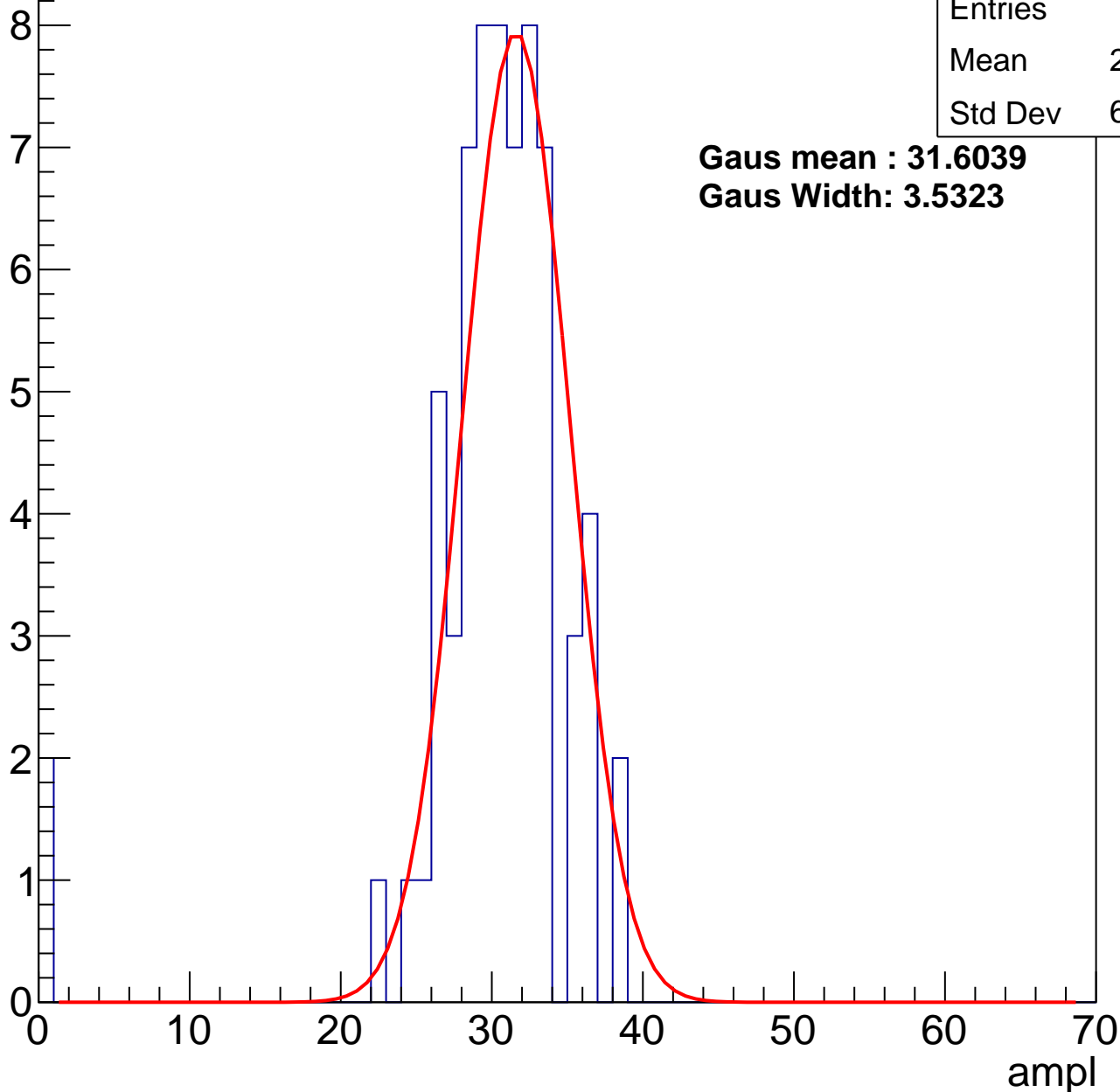
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 67    |
| Mean    | 29.54 |
| Std Dev | 6.112 |

**Gaus mean : 31.6039**

**Gaus Width: 3.5323**



# B0L001S, U2-ch36, adc1

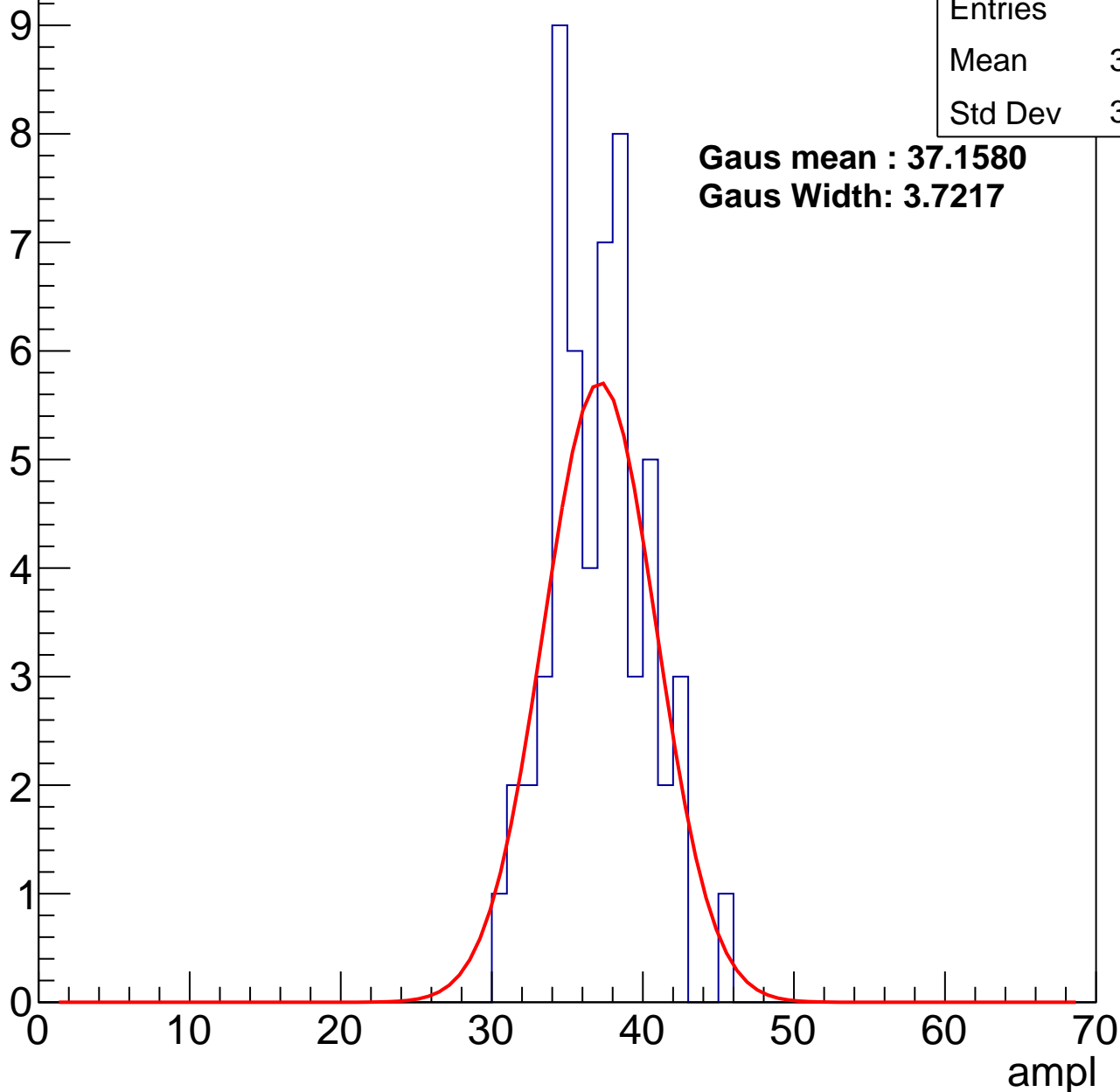
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 56    |
| Mean    | 36.57 |
| Std Dev | 3.144 |

**Gaus mean : 37.1580**

**Gaus Width: 3.7217**



# B0L001S, U2-ch36, adc2

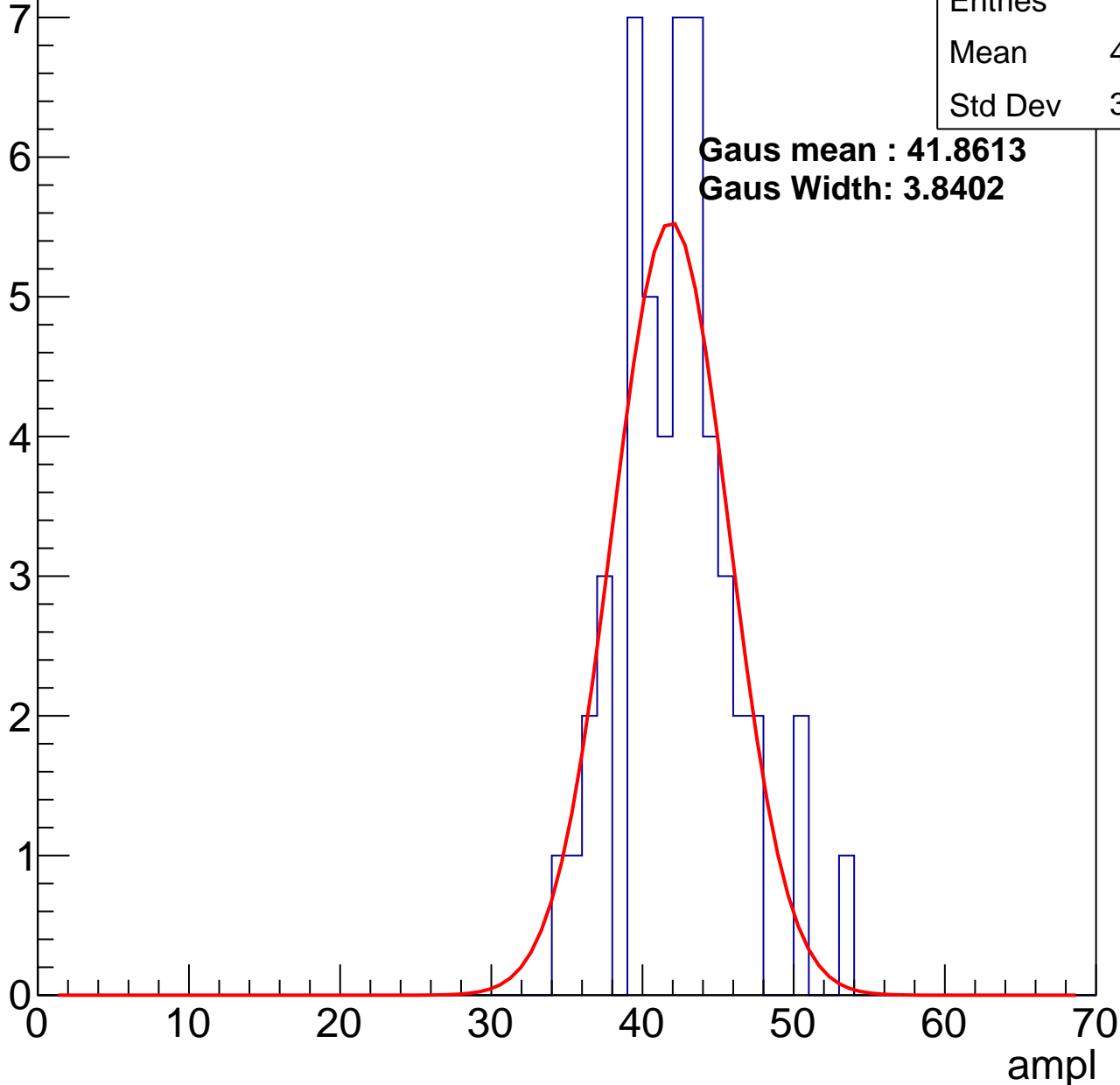
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 51    |
| Mean    | 41.84 |
| Std Dev | 3.775 |

**Gaus mean : 41.8613**

**Gaus Width: 3.8402**

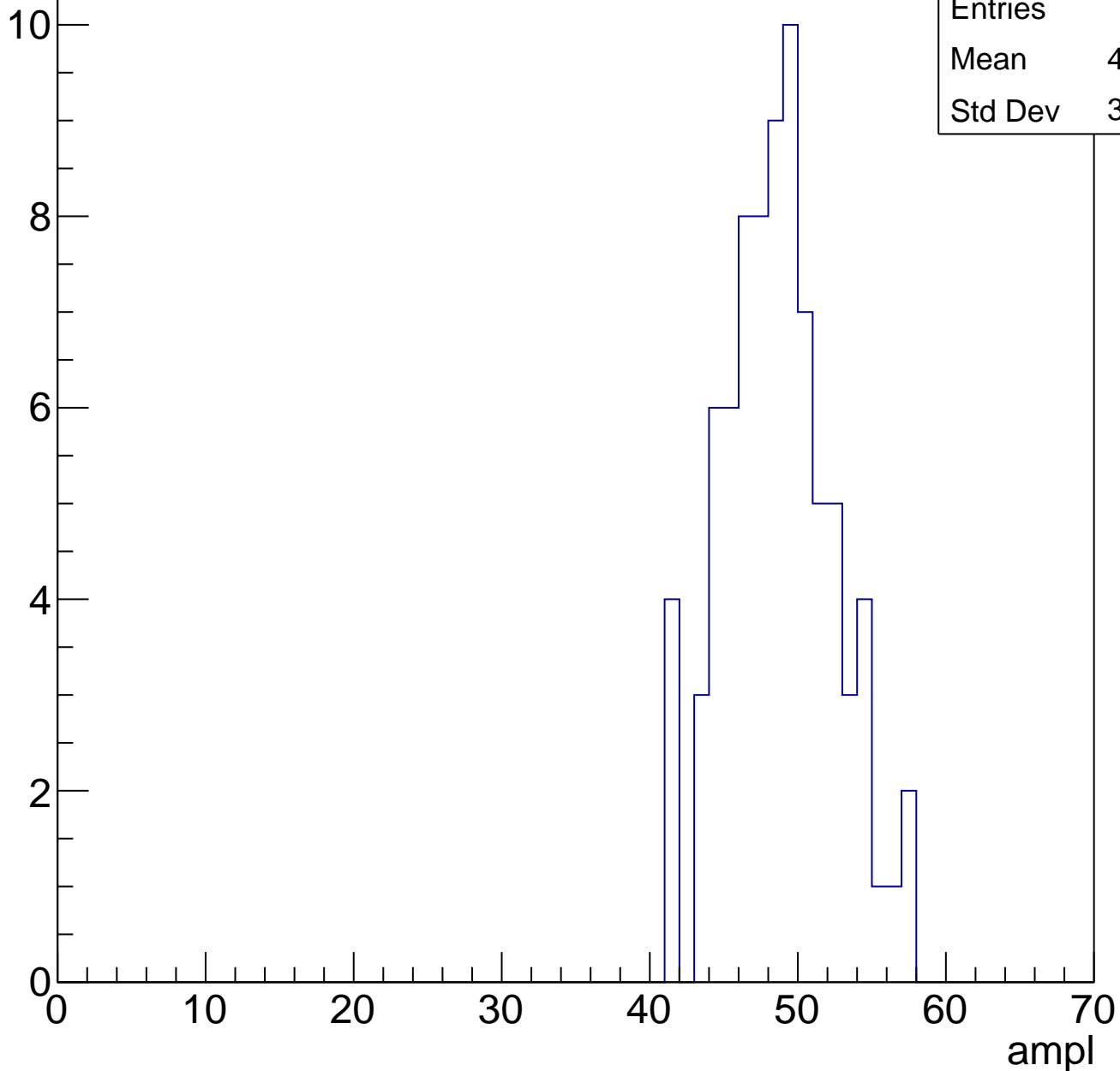


# B0L001S, U2-ch36, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 82    |
| Mean    | 48.27 |
| Std Dev | 3.683 |

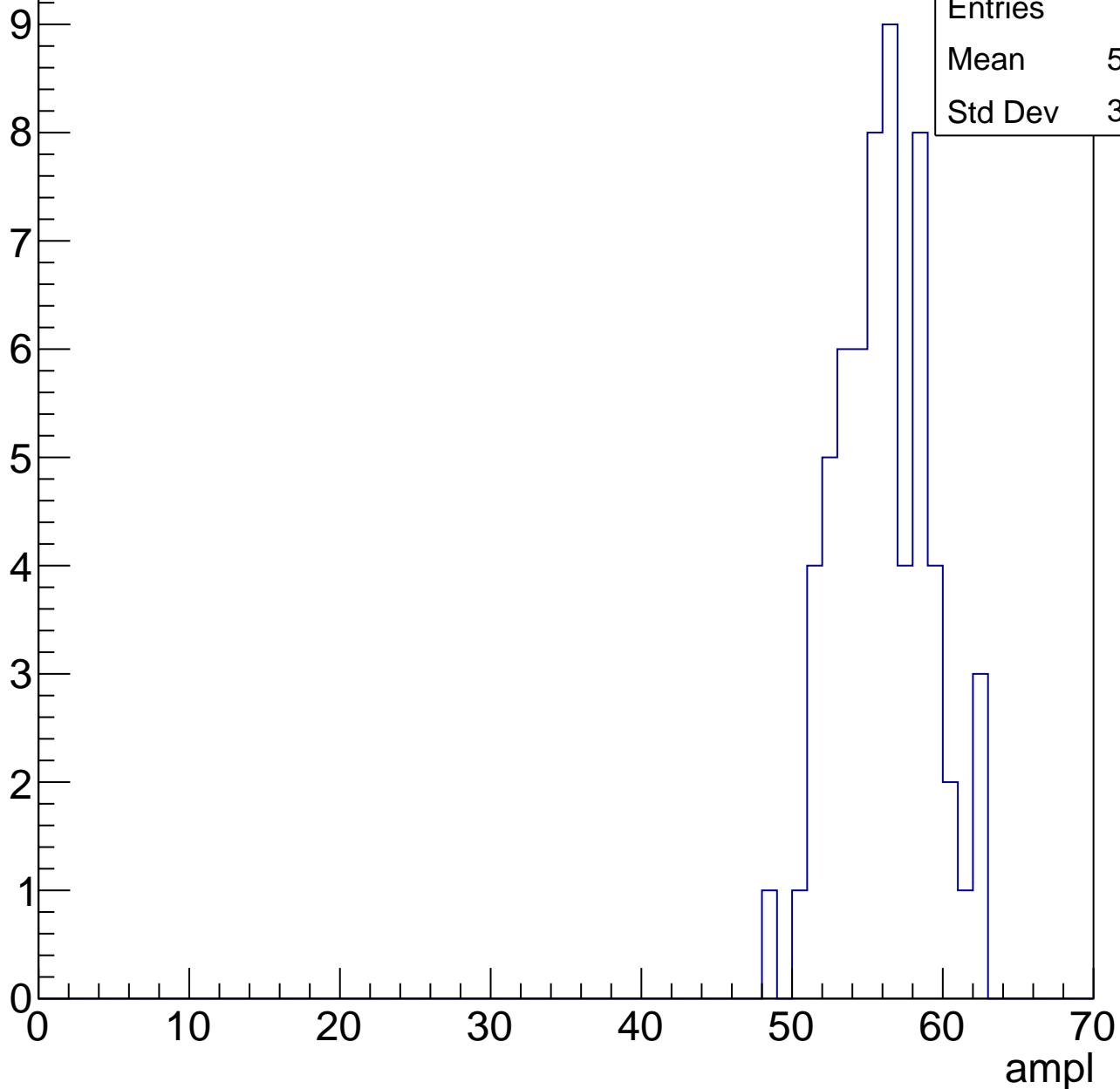
Entry



# B0L001S, U2-ch36, adc4

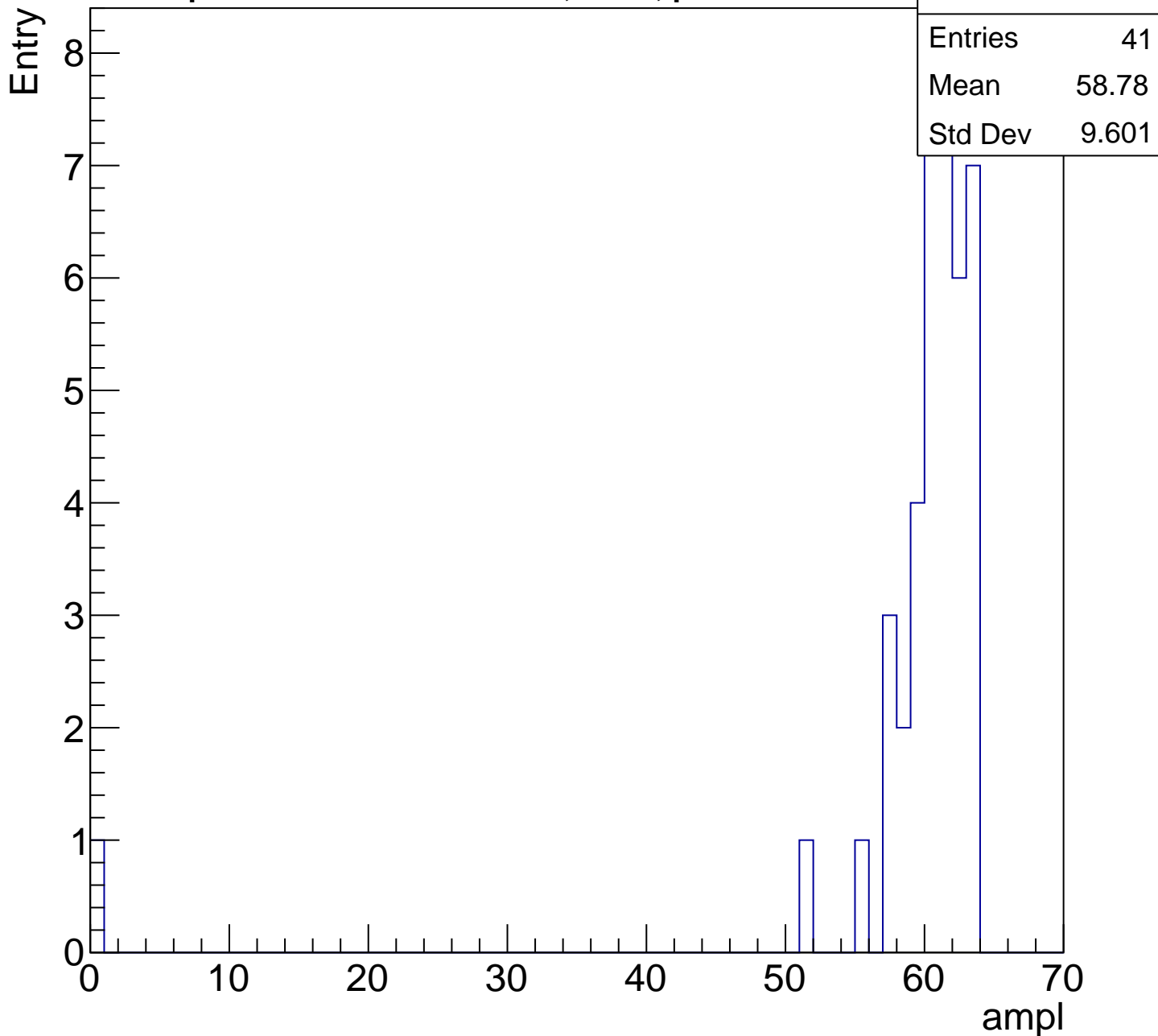
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U2-ch36, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U2-ch36, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries

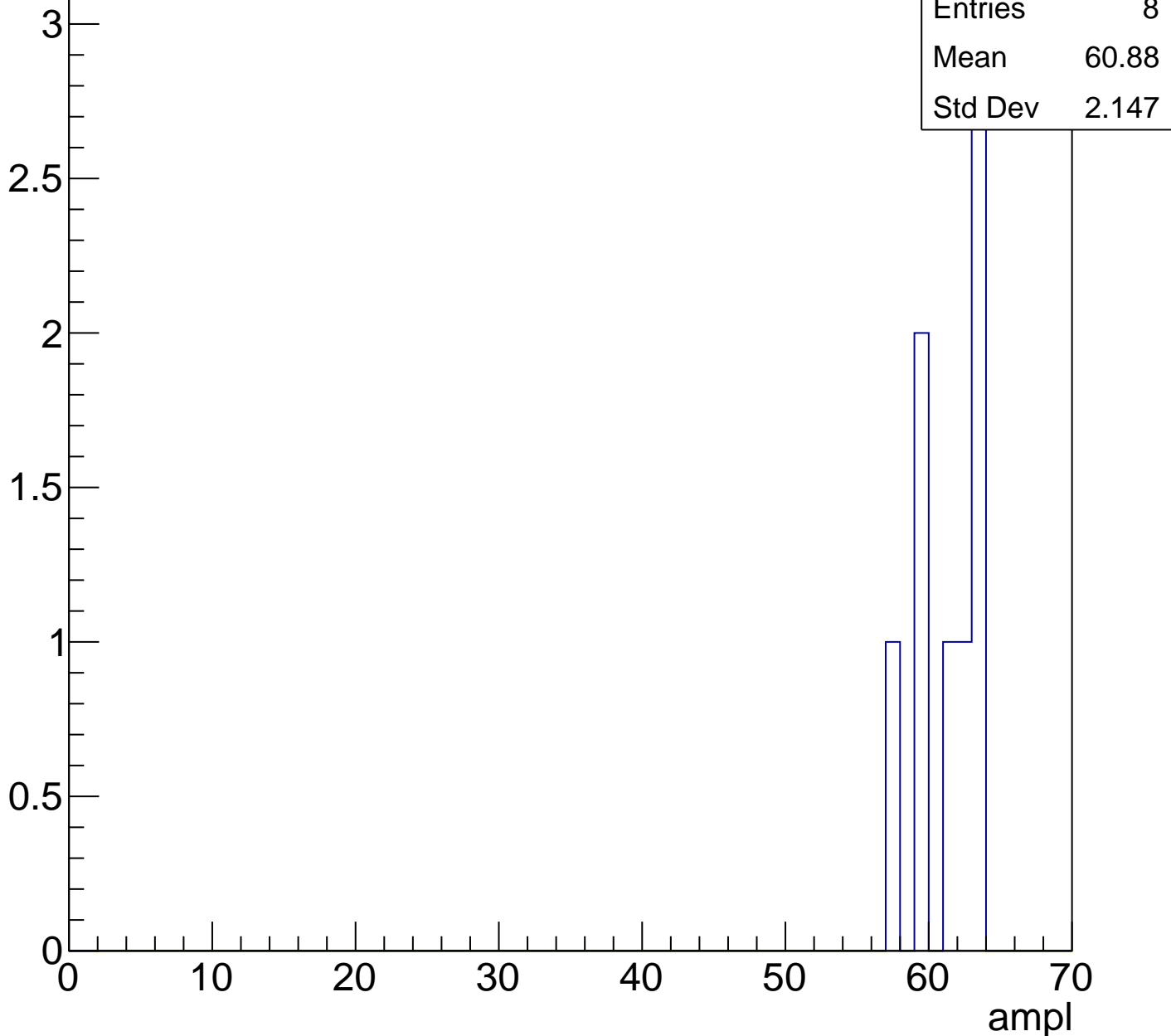
8

Mean

60.88

Std Dev

2.147





# B0L001S, U2-ch36, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 0 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch37, adc0

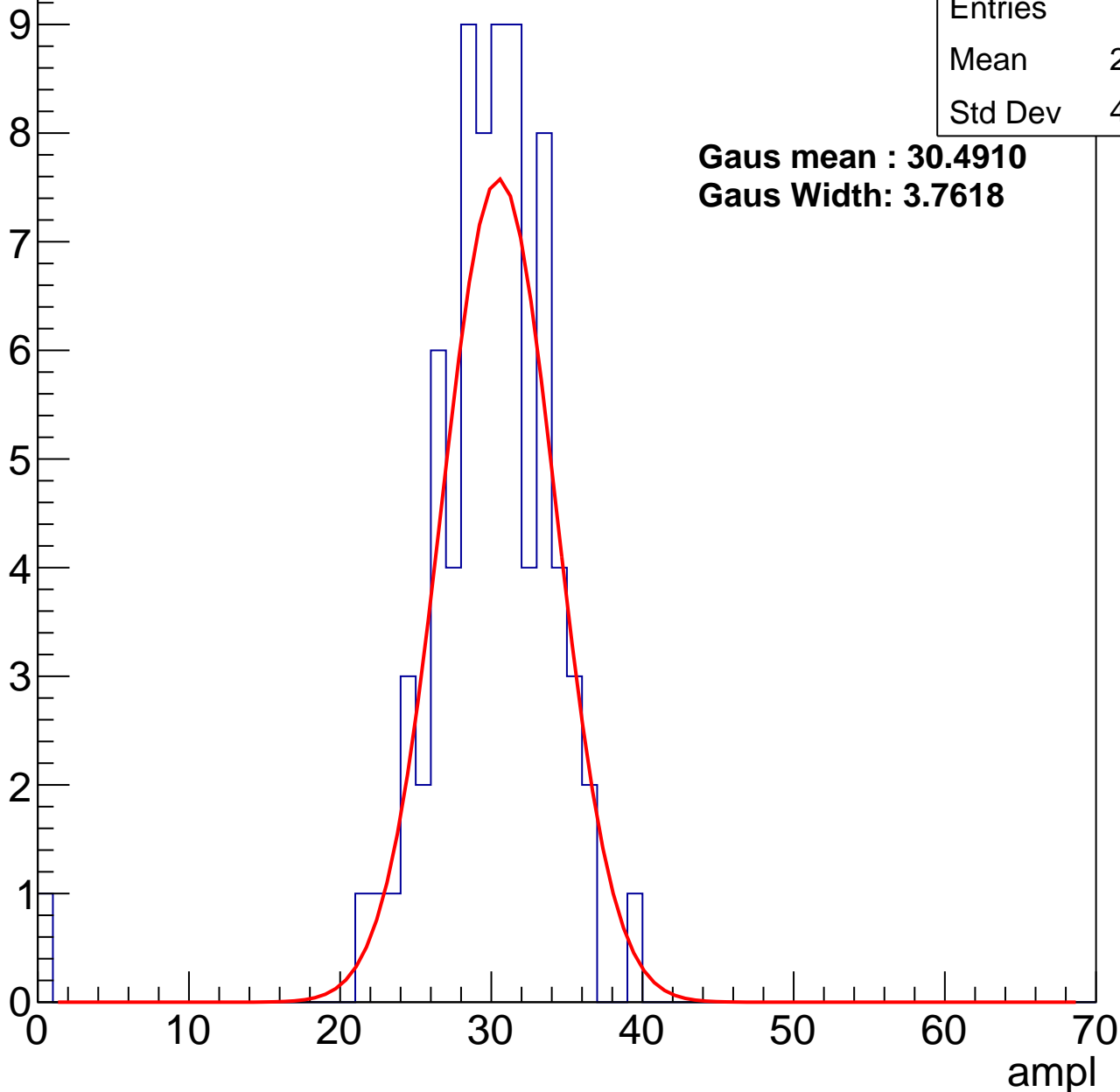
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 76    |
| Mean    | 29.33 |
| Std Dev | 4.843 |

**Gaus mean : 30.4910**

**Gaus Width: 3.7618**



# B0L001S, U2-ch37, adc1

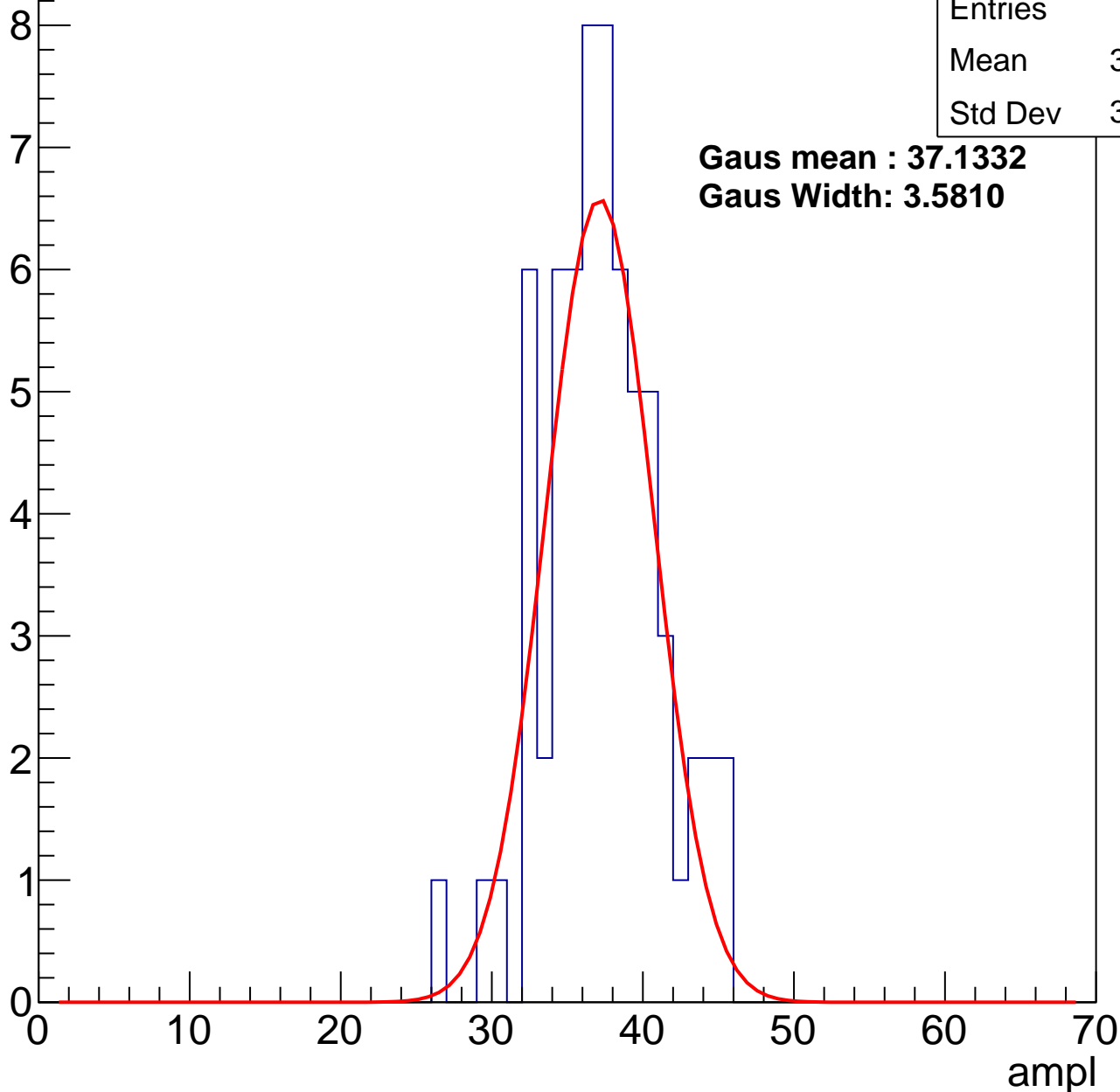
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 65    |
| Mean    | 36.82 |
| Std Dev | 3.806 |

**Gaus mean : 37.1332**

**Gaus Width: 3.5810**



# B0L001S, U2-ch37, adc2

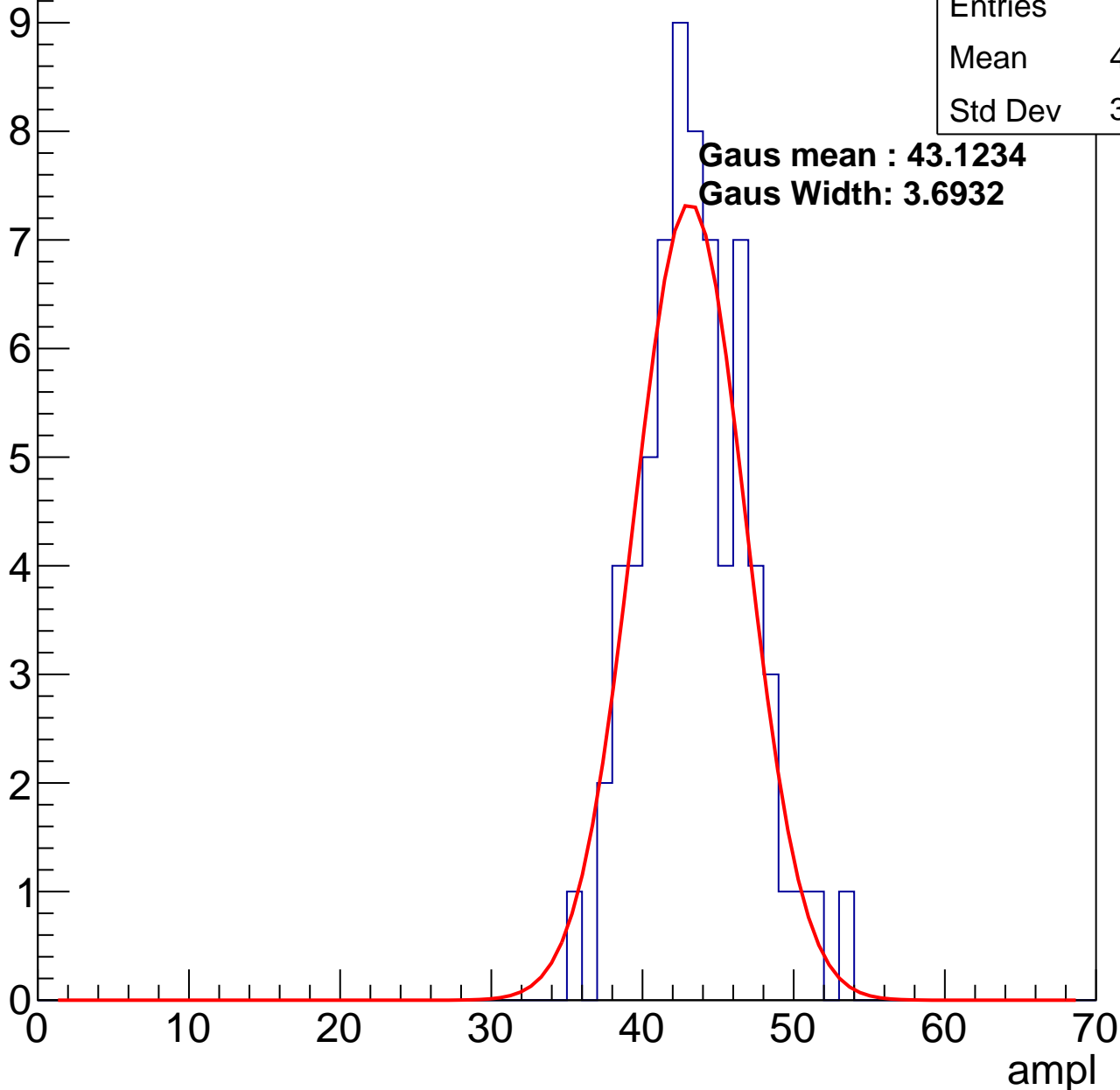
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 69    |
| Mean    | 43.06 |
| Std Dev | 3.522 |

**Gaus mean : 43.1234**

**Gaus Width: 3.6932**

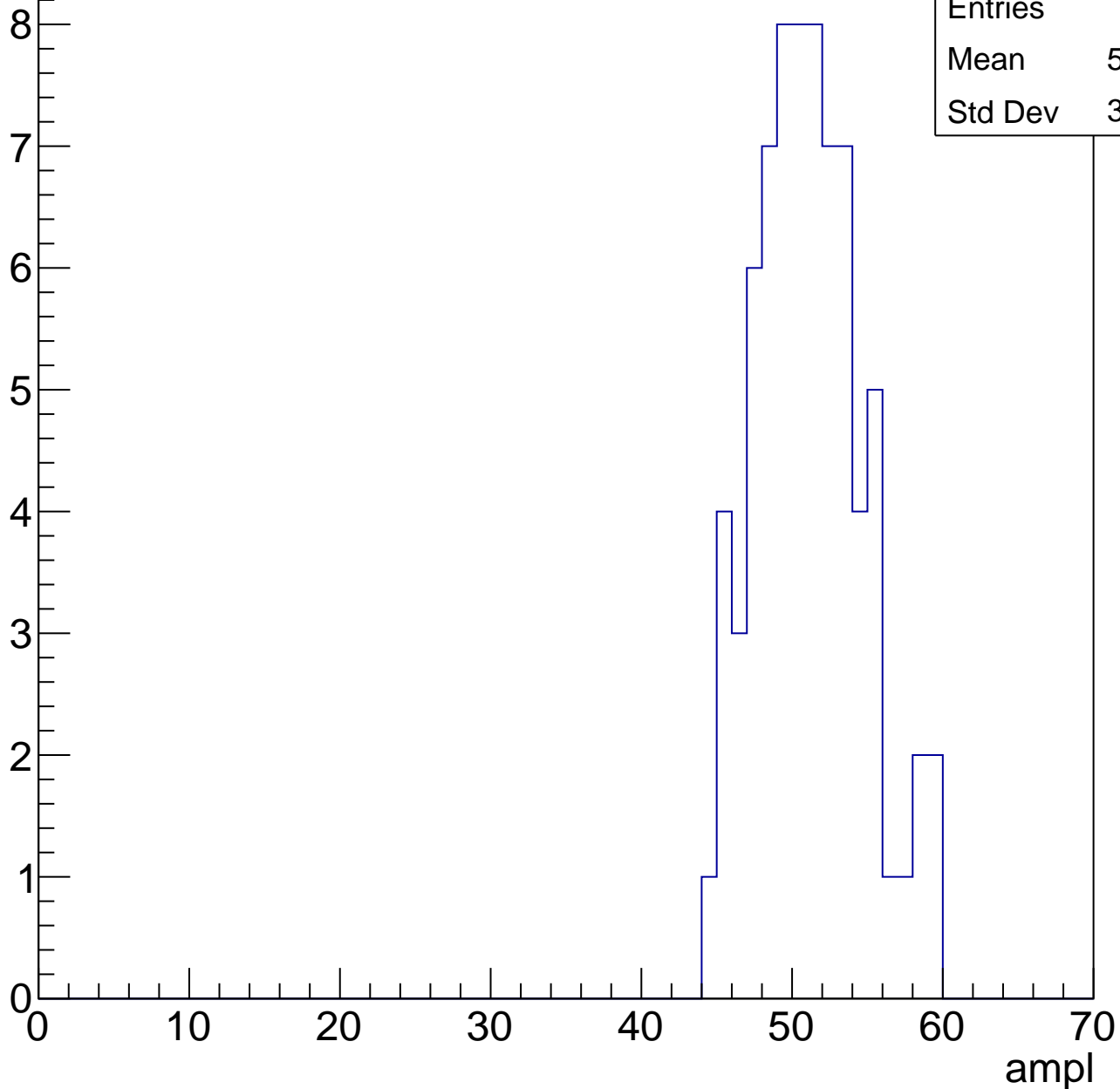


# B0L001S, U2-ch37, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 74    |
| Mean    | 50.72 |
| Std Dev | 3.486 |

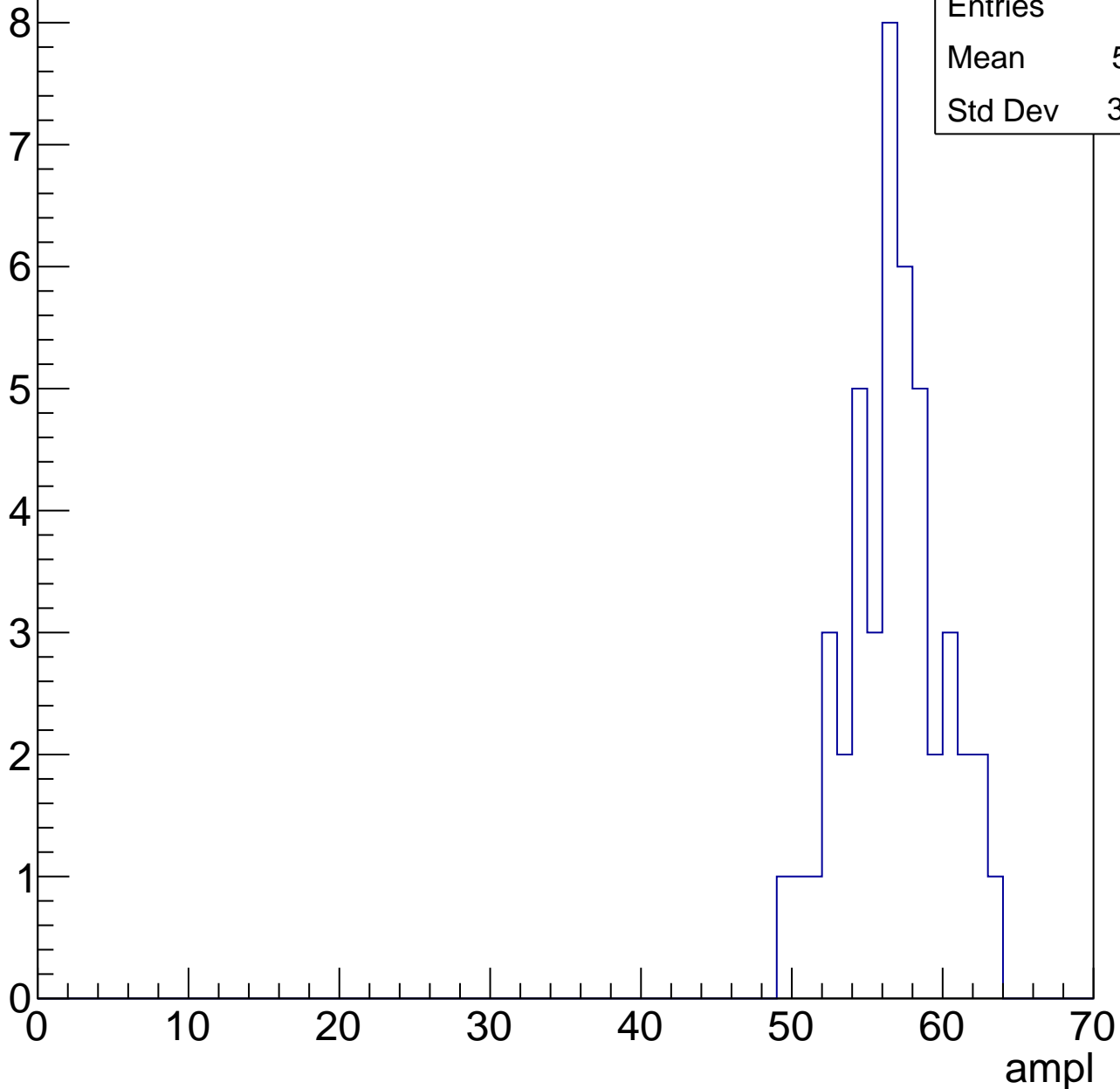


# B0L001S, U2-ch37, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

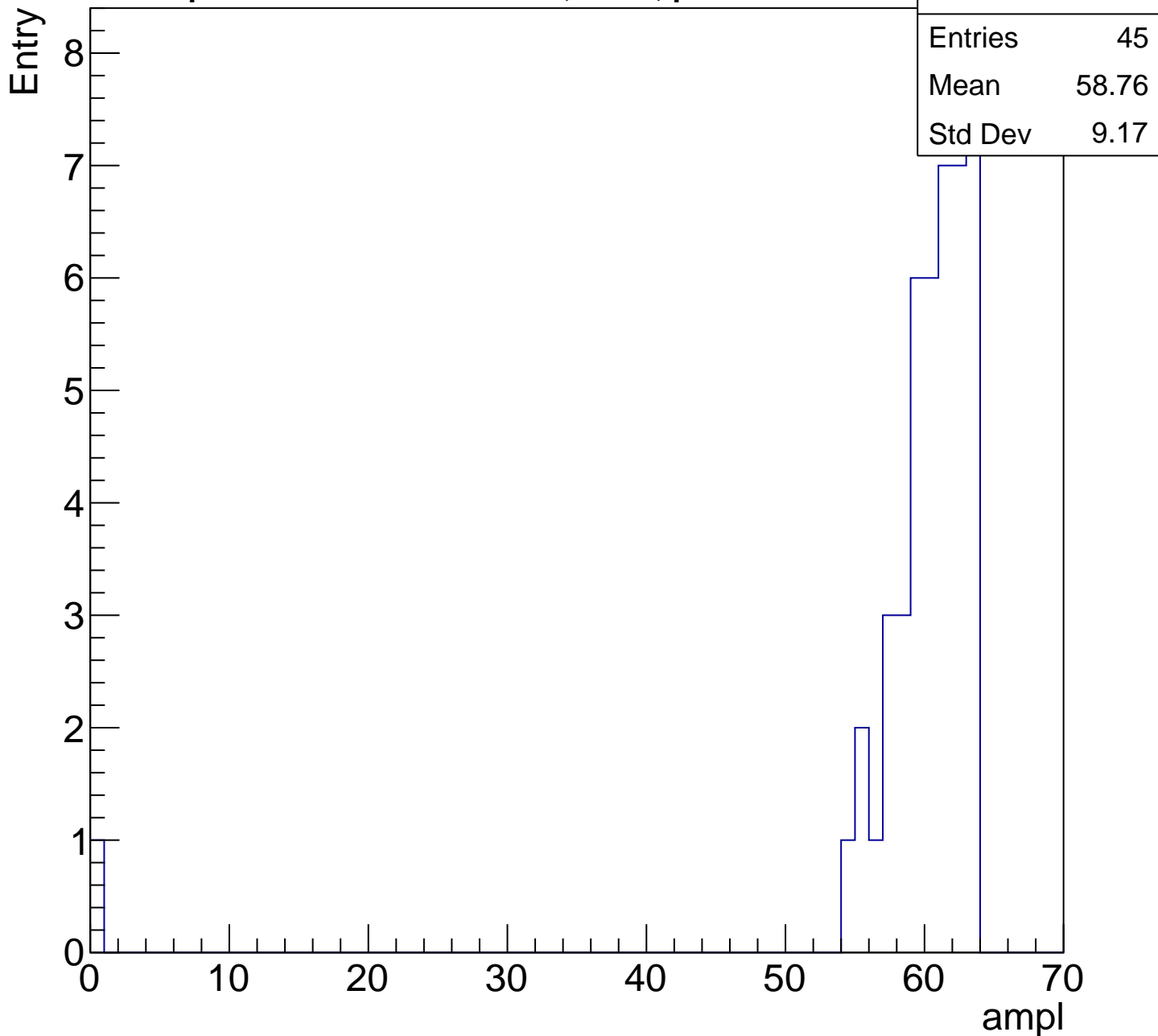
Entry

|         |       |
|---------|-------|
| Entries | 45    |
| Mean    | 56.31 |
| Std Dev | 3.189 |



# B0L001S, U2-ch37, adc5

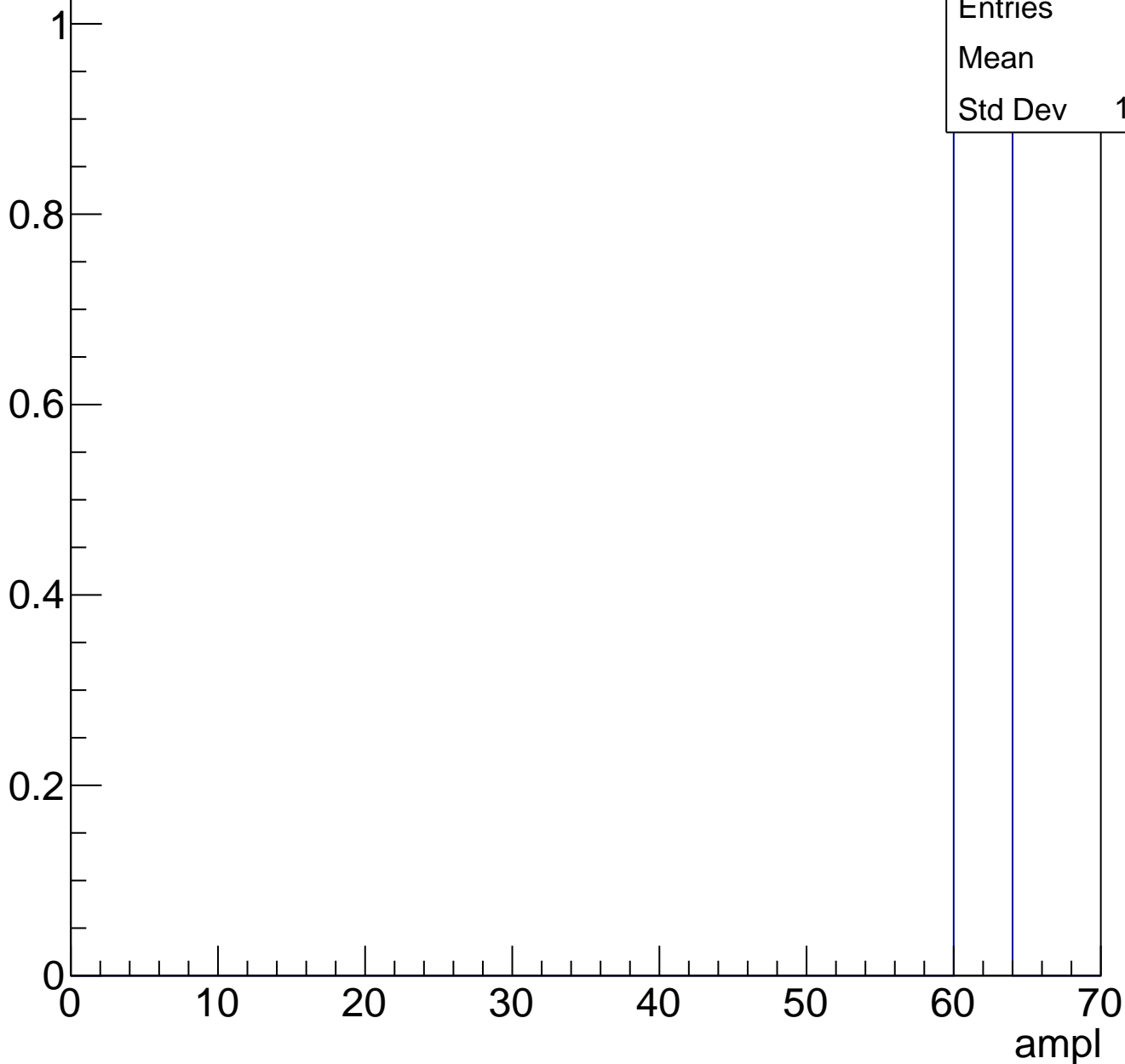
calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U2-ch37, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch37, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 0 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch38, adc0

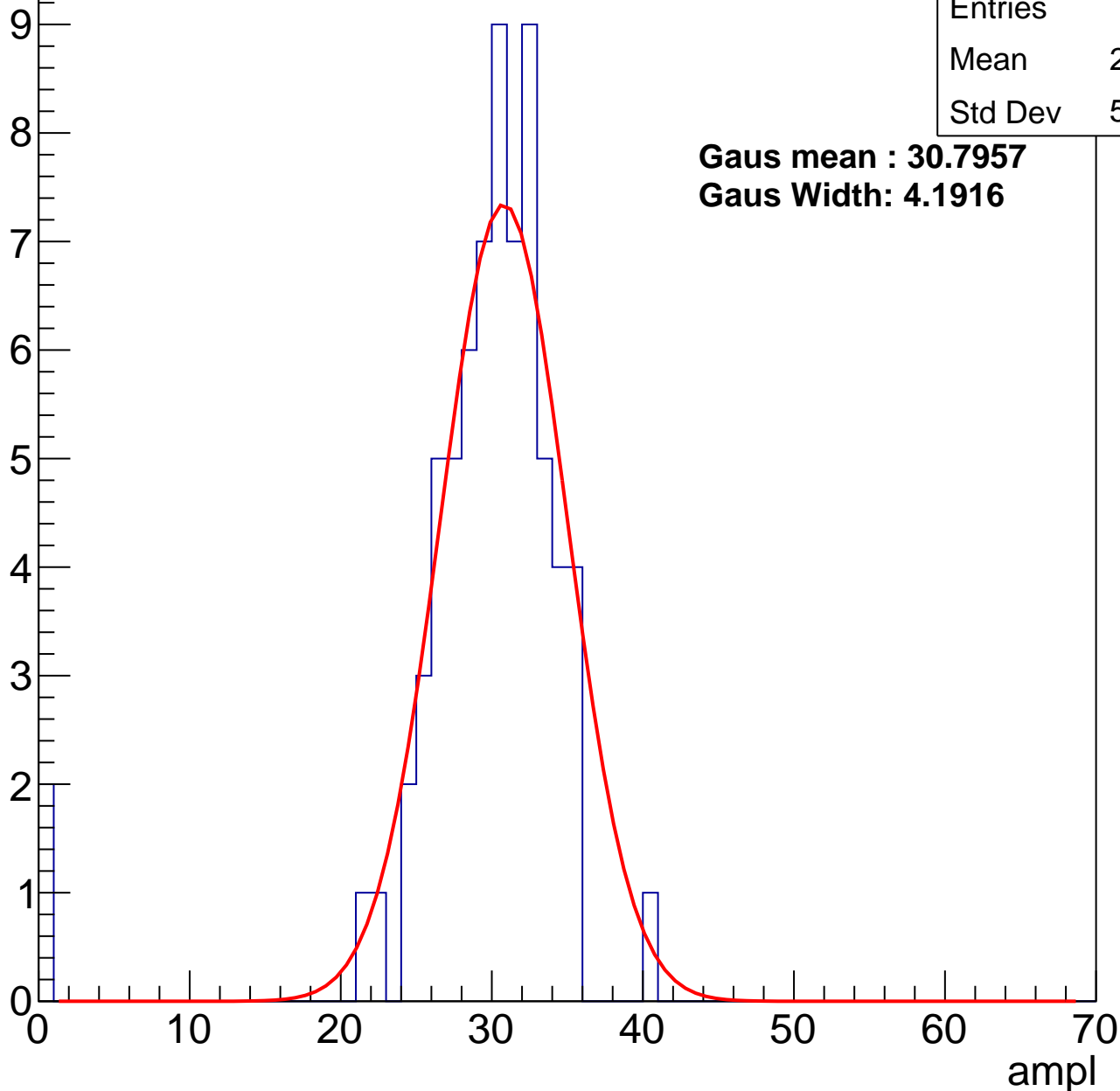
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 71    |
| Mean    | 28.99 |
| Std Dev | 5.966 |

**Gaus mean : 30.7957**

**Gaus Width: 4.1916**



# B0L001S, U2-ch38, adc1

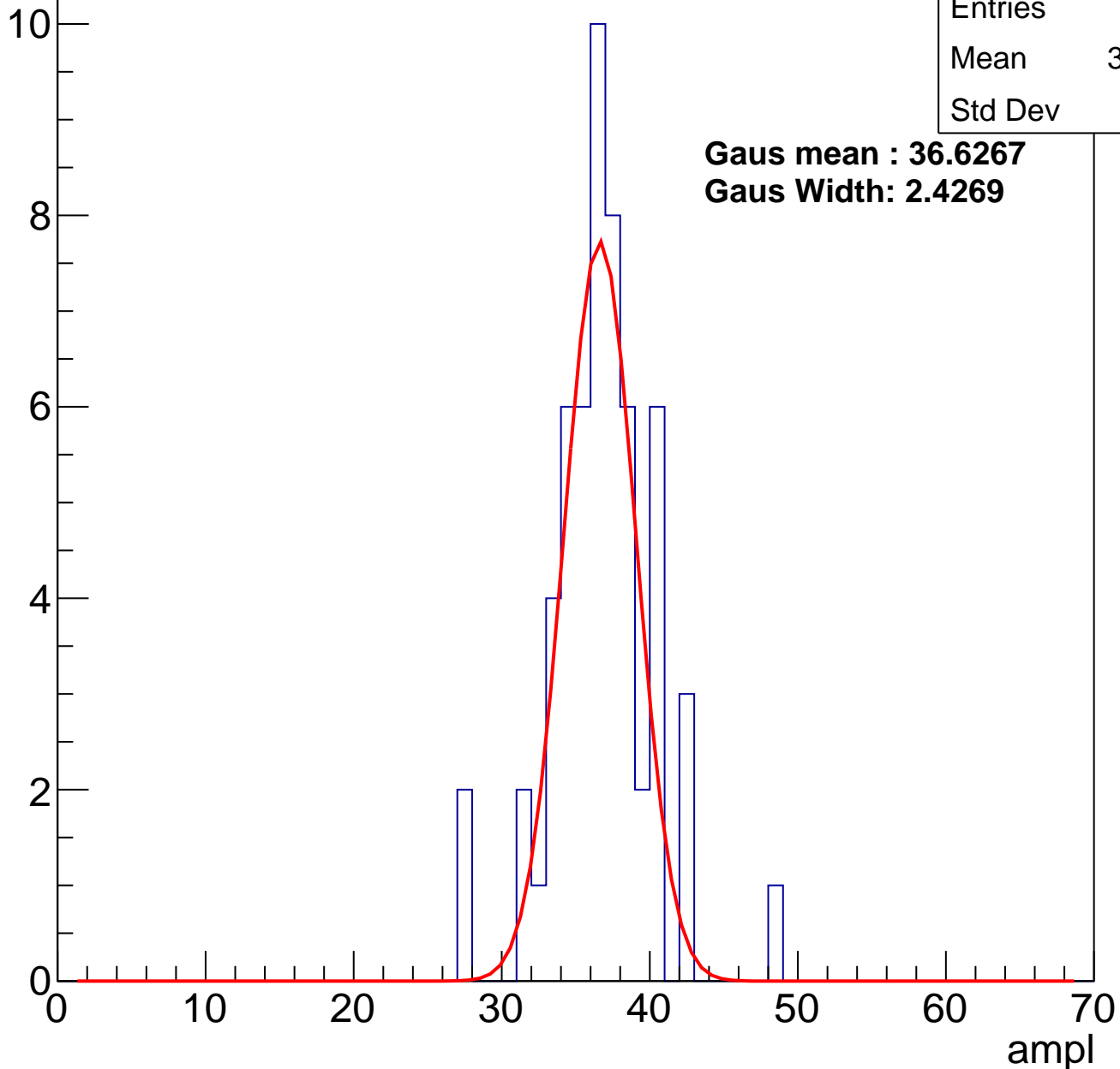
calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 57    |
| Mean    | 36.32 |
| Std Dev | 3.47  |

**Gaus mean : 36.6267**

**Gaus Width: 2.4269**

Entry



# B0L001S, U2-ch38, adc2

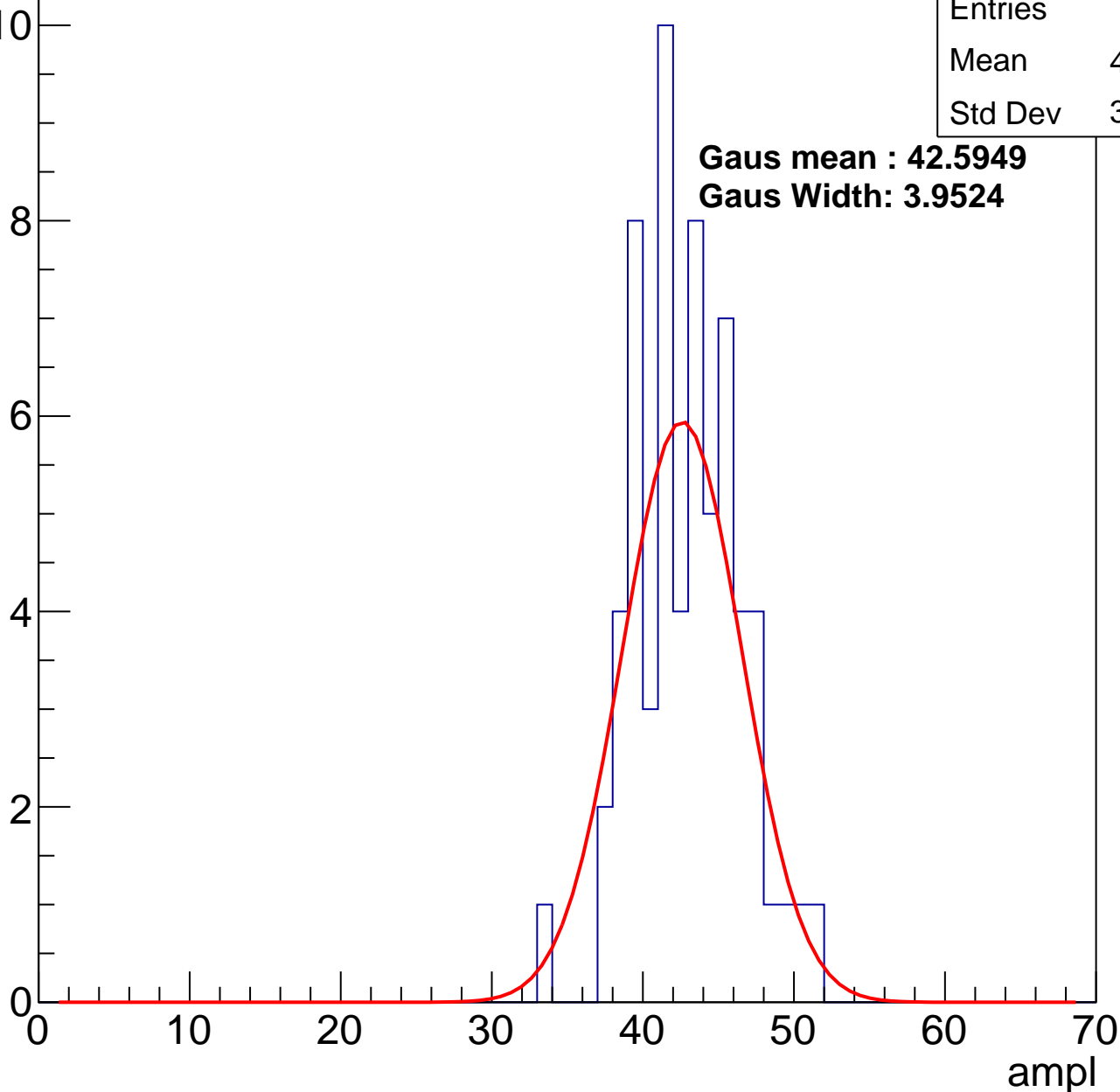
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 64    |
| Mean    | 42.47 |
| Std Dev | 3.446 |

**Gaus mean : 42.5949**

**Gaus Width: 3.9524**

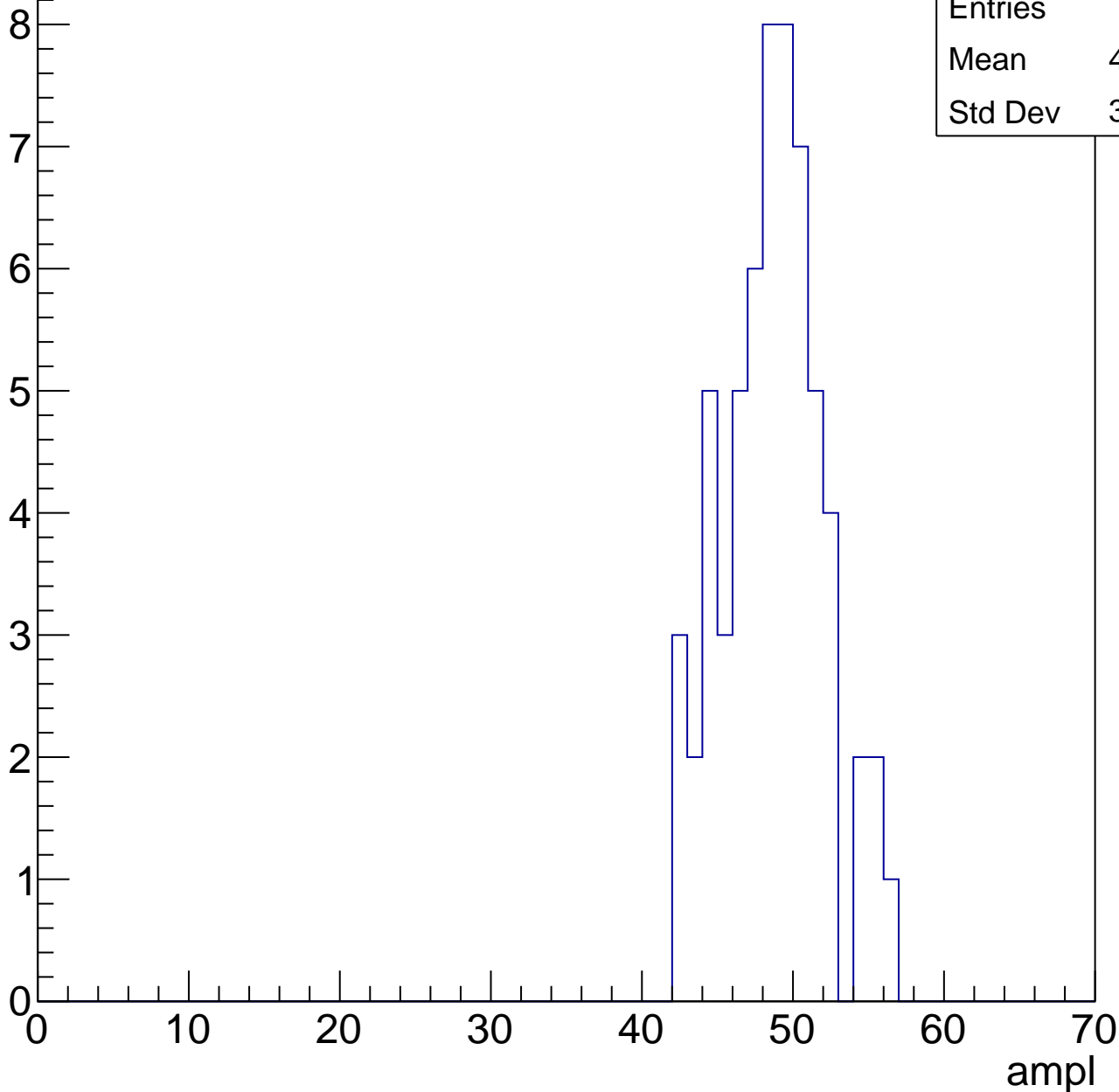


# B0L001S, U2-ch38, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 61    |
| Mean    | 48.23 |
| Std Dev | 3.306 |



# B0L001S, U2-ch38, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

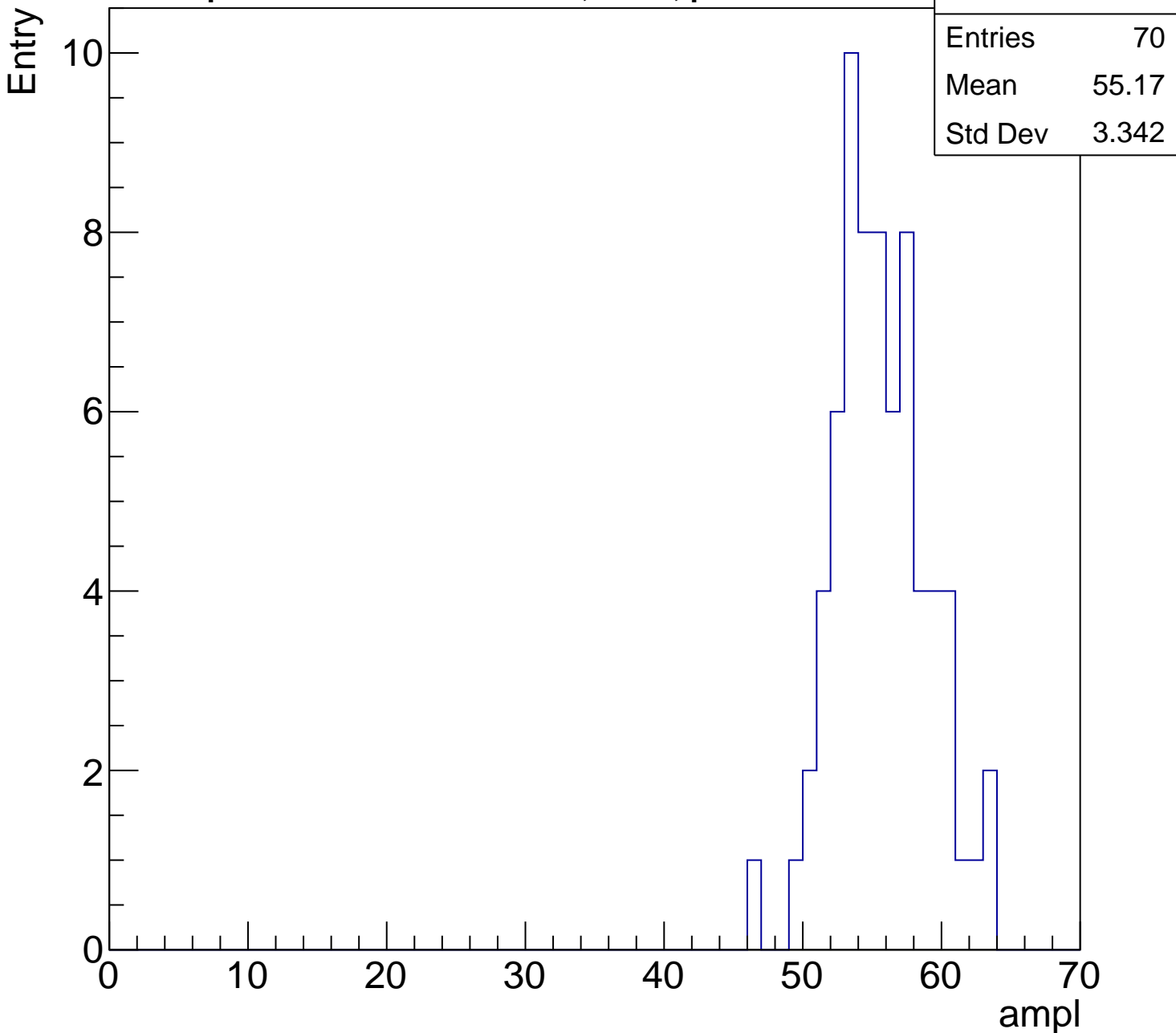
|         |       |
|---------|-------|
| Entries | 70    |
| Mean    | 55.17 |
| Std Dev | 3.342 |

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

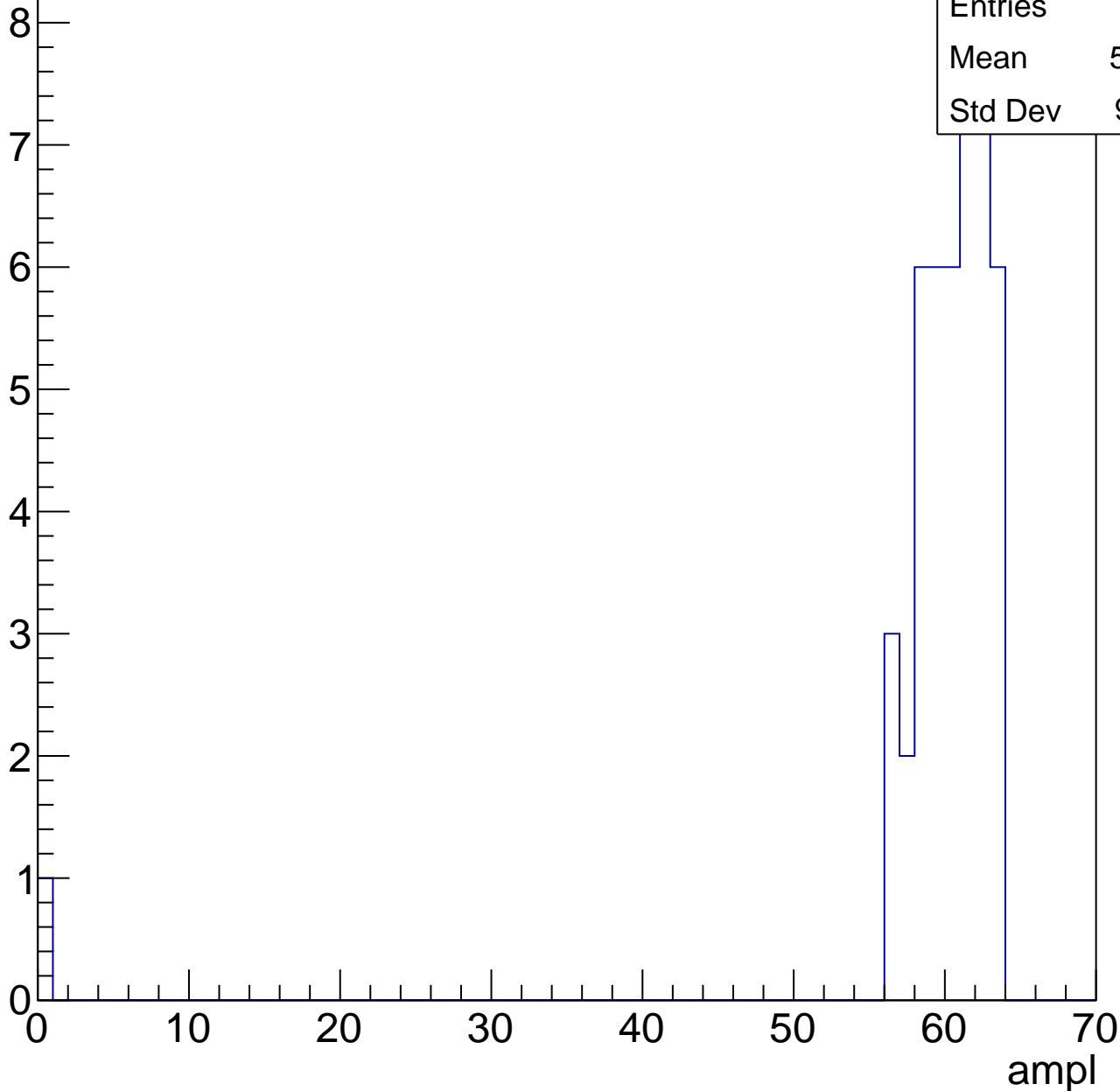


# B0L001S, U2-ch38, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

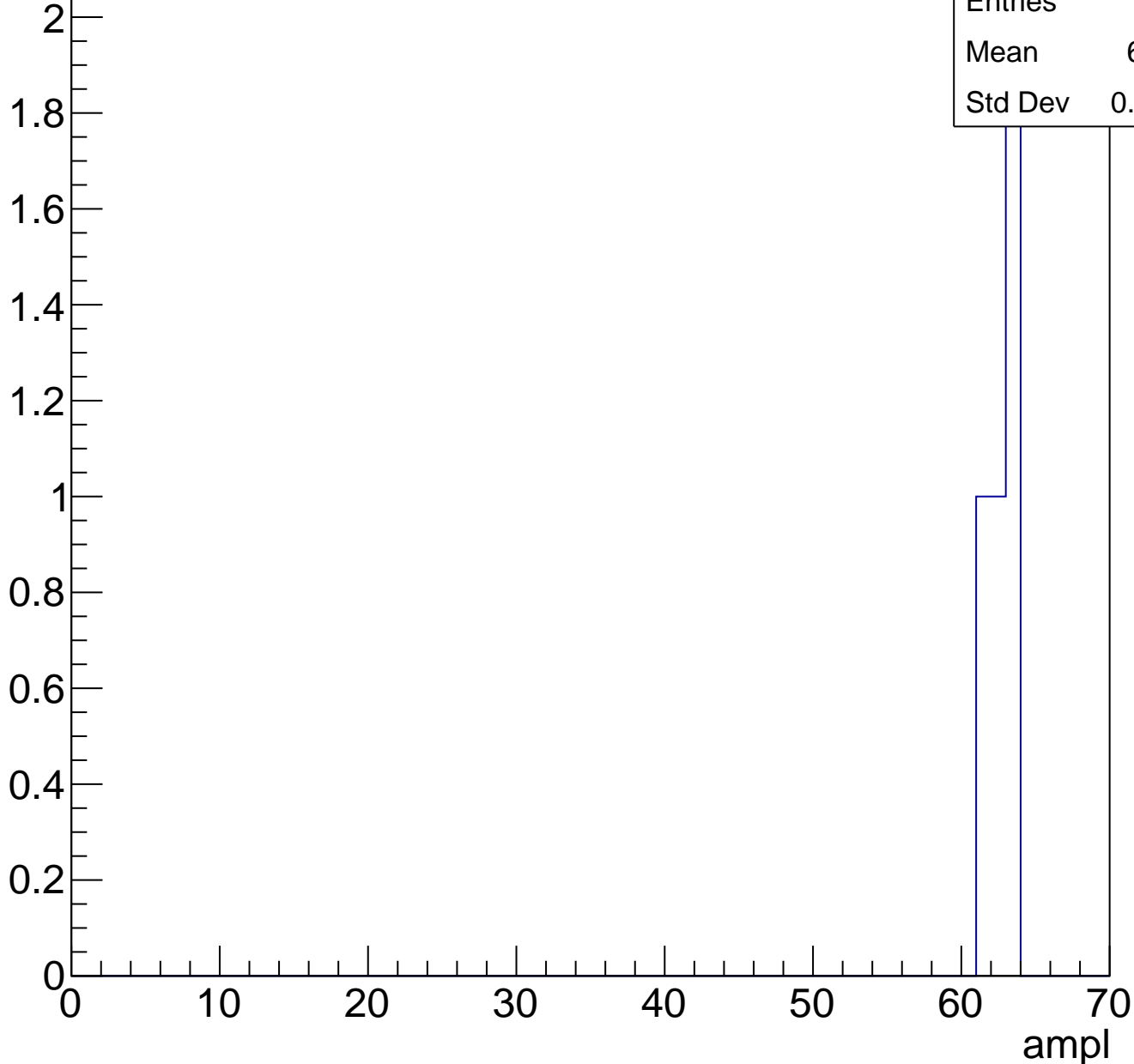
|         |       |
|---------|-------|
| Entries | 46    |
| Mean    | 58.83 |
| Std Dev | 9.001 |



# B0L001S, U2-ch38, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch38, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U2-ch39, adc0

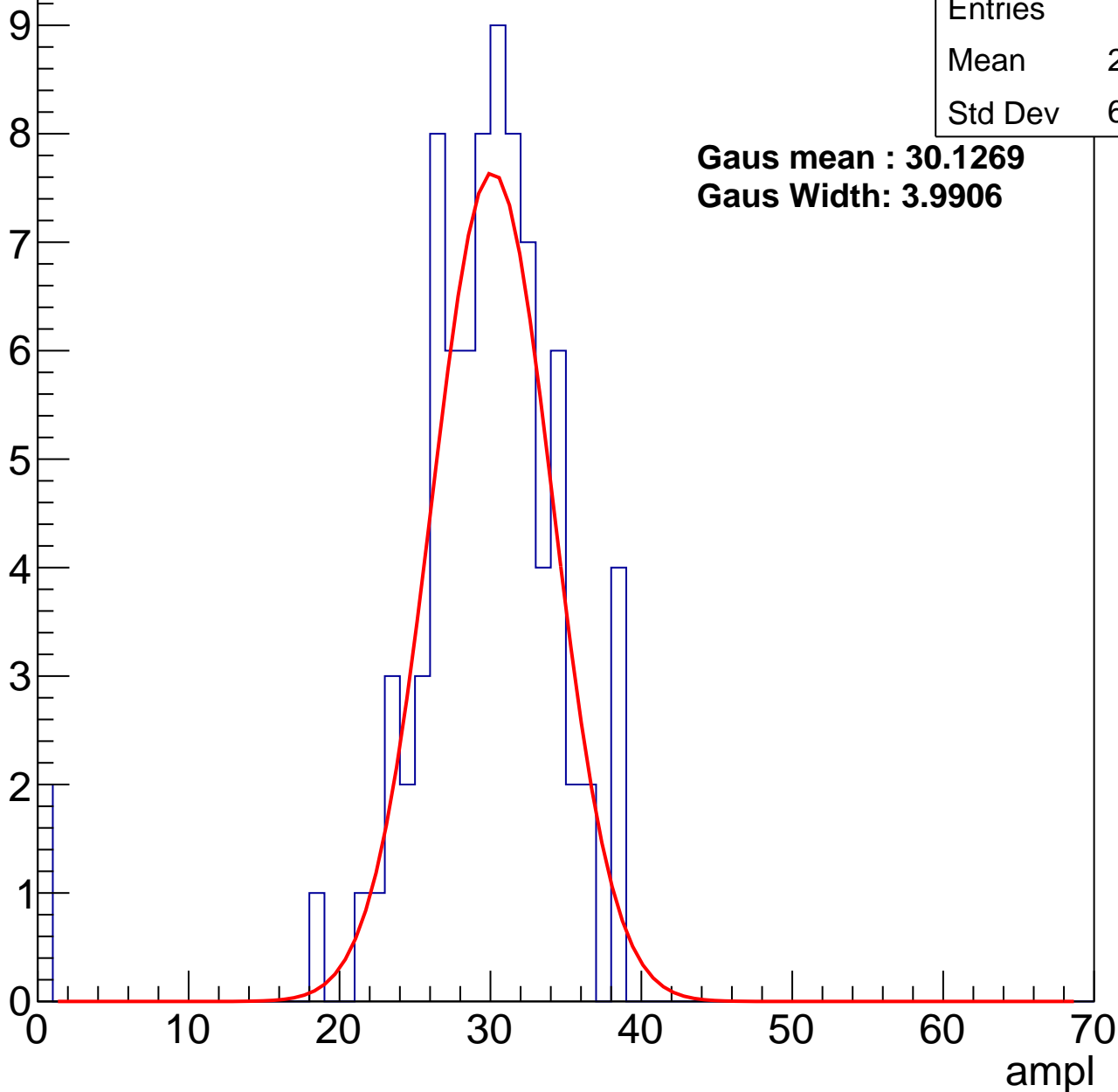
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 83    |
| Mean    | 28.86 |
| Std Dev | 6.046 |

**Gaus mean : 30.1269**

**Gaus Width: 3.9906**



# B0L001S, U2-ch39, adc1

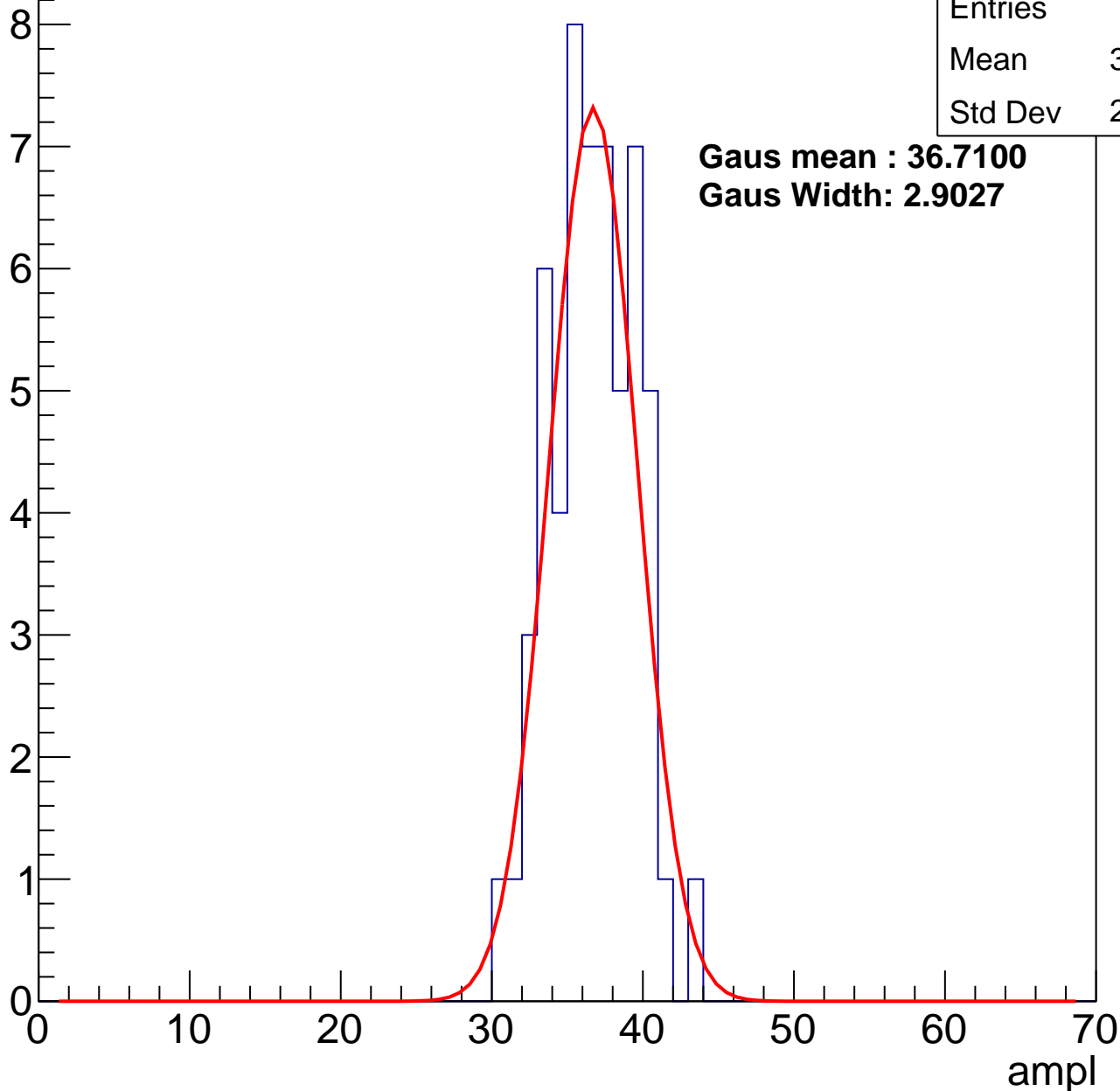
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 56    |
| Mean    | 36.23 |
| Std Dev | 2.765 |

**Gaus mean : 36.7100**

**Gaus Width: 2.9027**



# B0L001S, U2-ch39, adc2

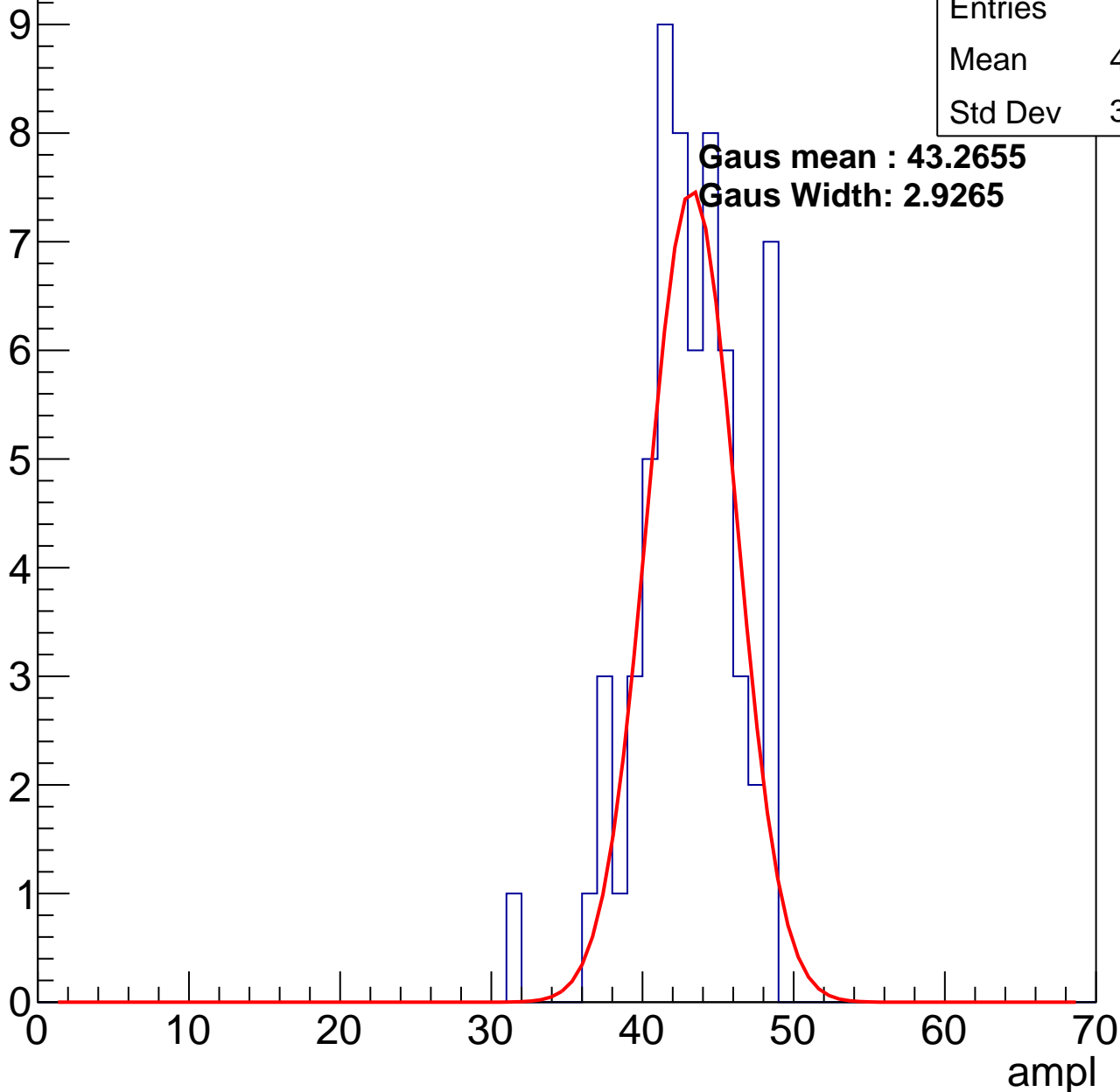
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 63    |
| Mean    | 42.63 |
| Std Dev | 3.382 |

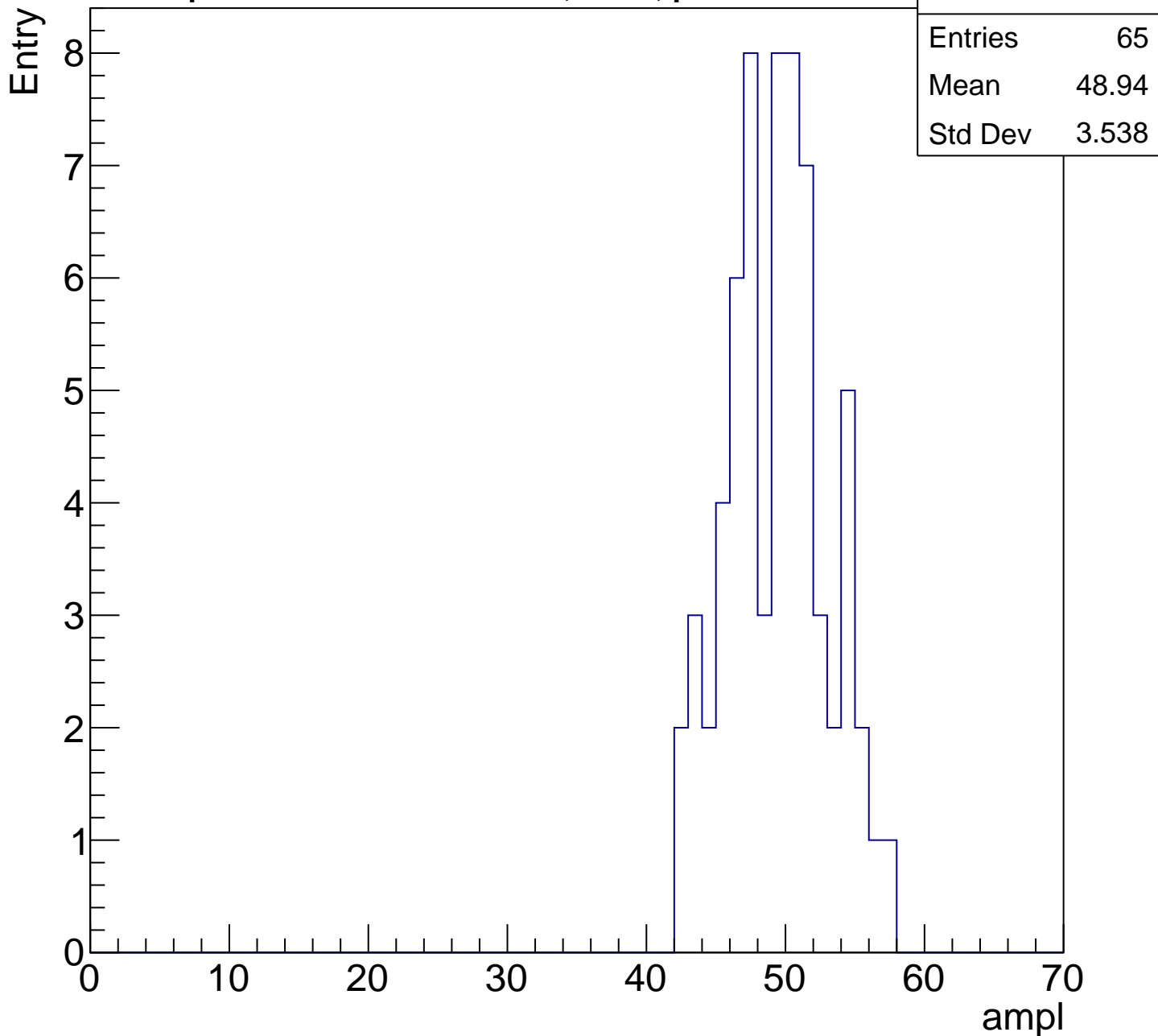
**Gaus mean : 43.2655**

**Gaus Width: 2.9265**



# B0L001S, U2-ch39, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U2-ch39, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

|         |       |
|---------|-------|
| Entries | 68    |
| Mean    | 55.19 |
| Std Dev | 3.2   |

ampl

0 10 20 30 40 50 60 70

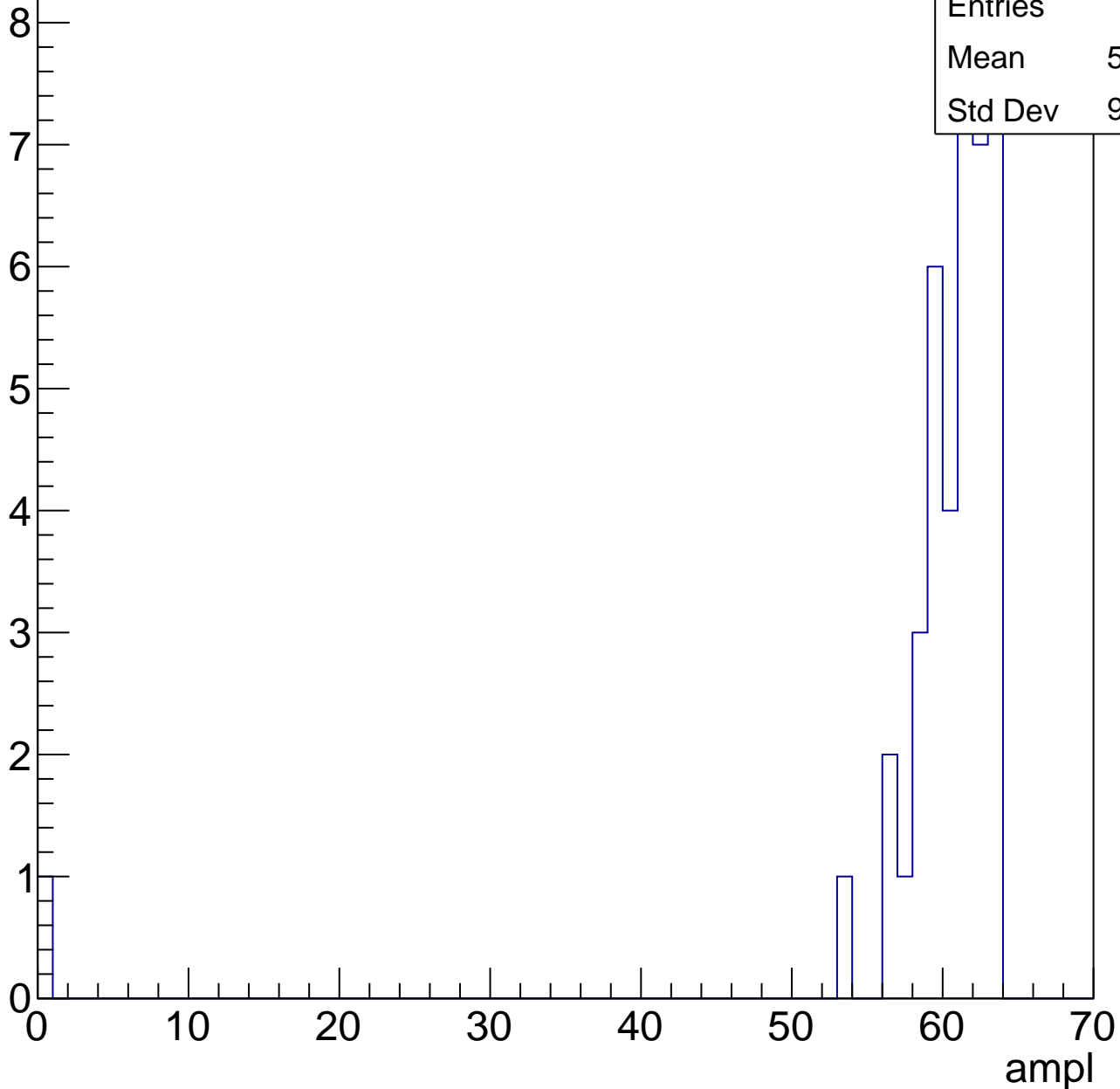
ampl

# B0L001S, U2-ch39, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 41    |
| Mean    | 58.93 |
| Std Dev | 9.588 |



# B0L001S, U2-ch39, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch39, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 0 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch40, adc0

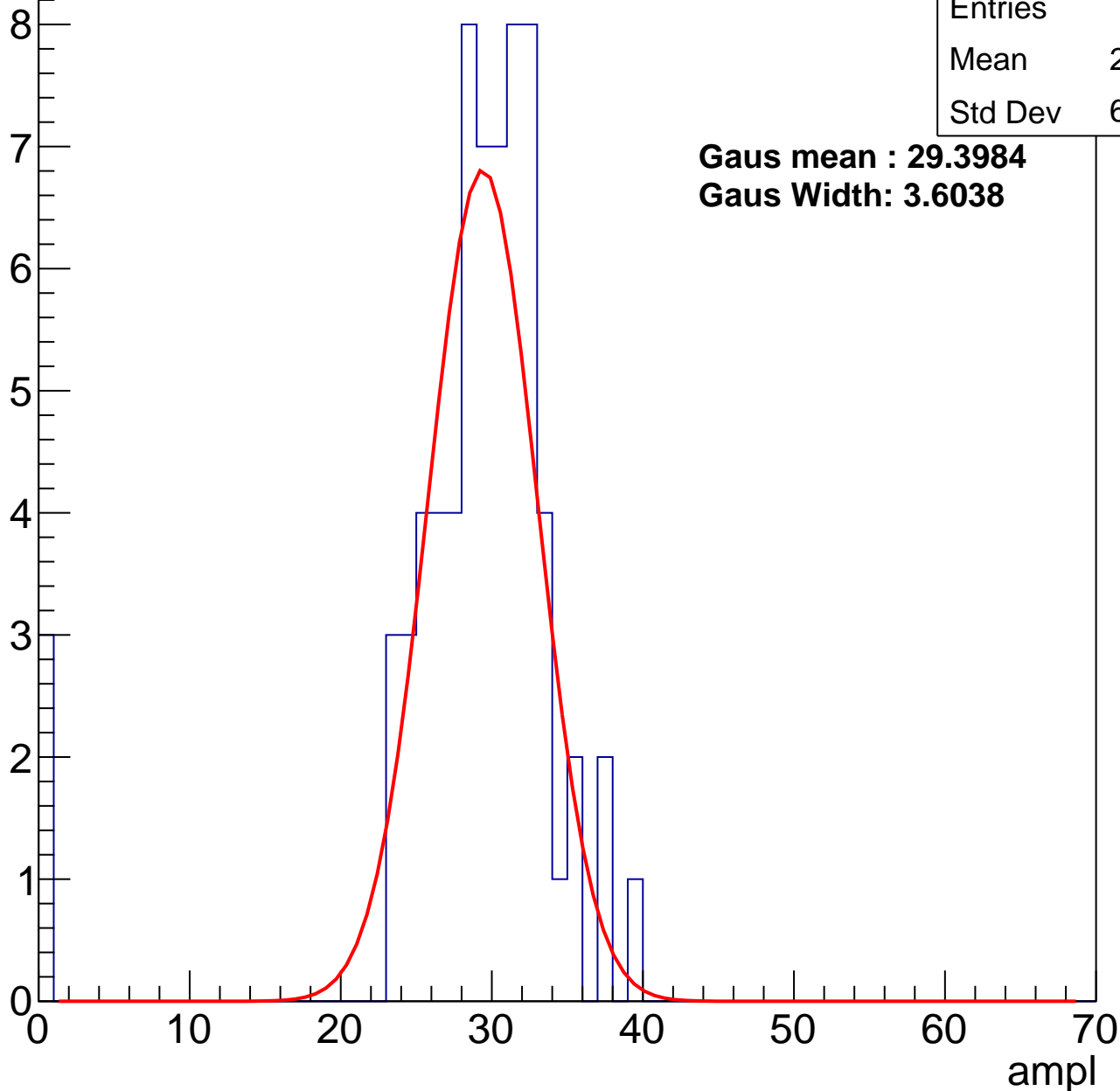
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 69    |
| Mean    | 28.16 |
| Std Dev | 6.896 |

**Gaus mean : 29.3984**

**Gaus Width: 3.6038**



# B0L001S, U2-ch40, adc1

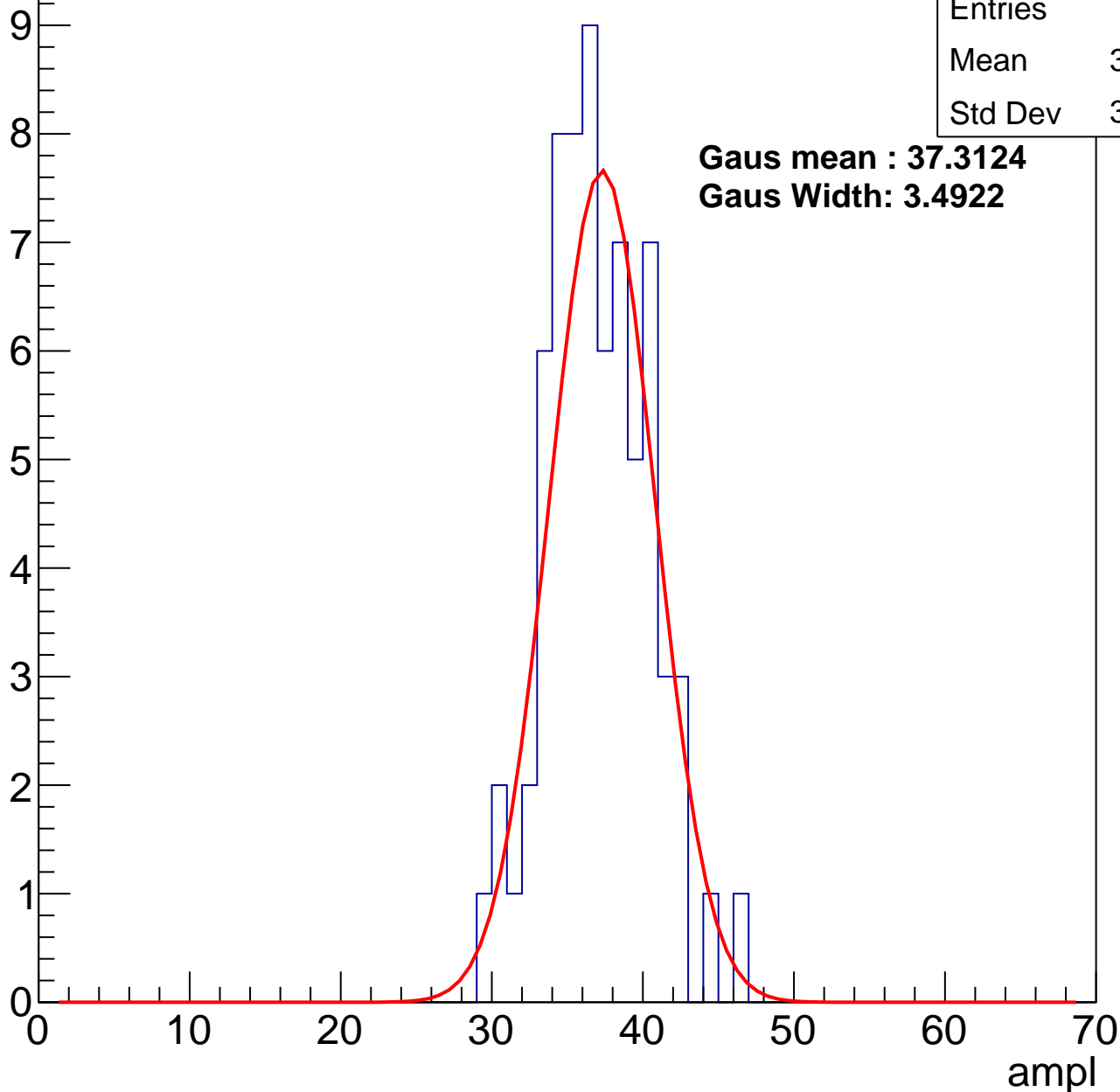
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 70    |
| Mean    | 36.57 |
| Std Dev | 3.353 |

**Gaus mean : 37.3124**

**Gaus Width: 3.4922**



# B0L001S, U2-ch40, adc2

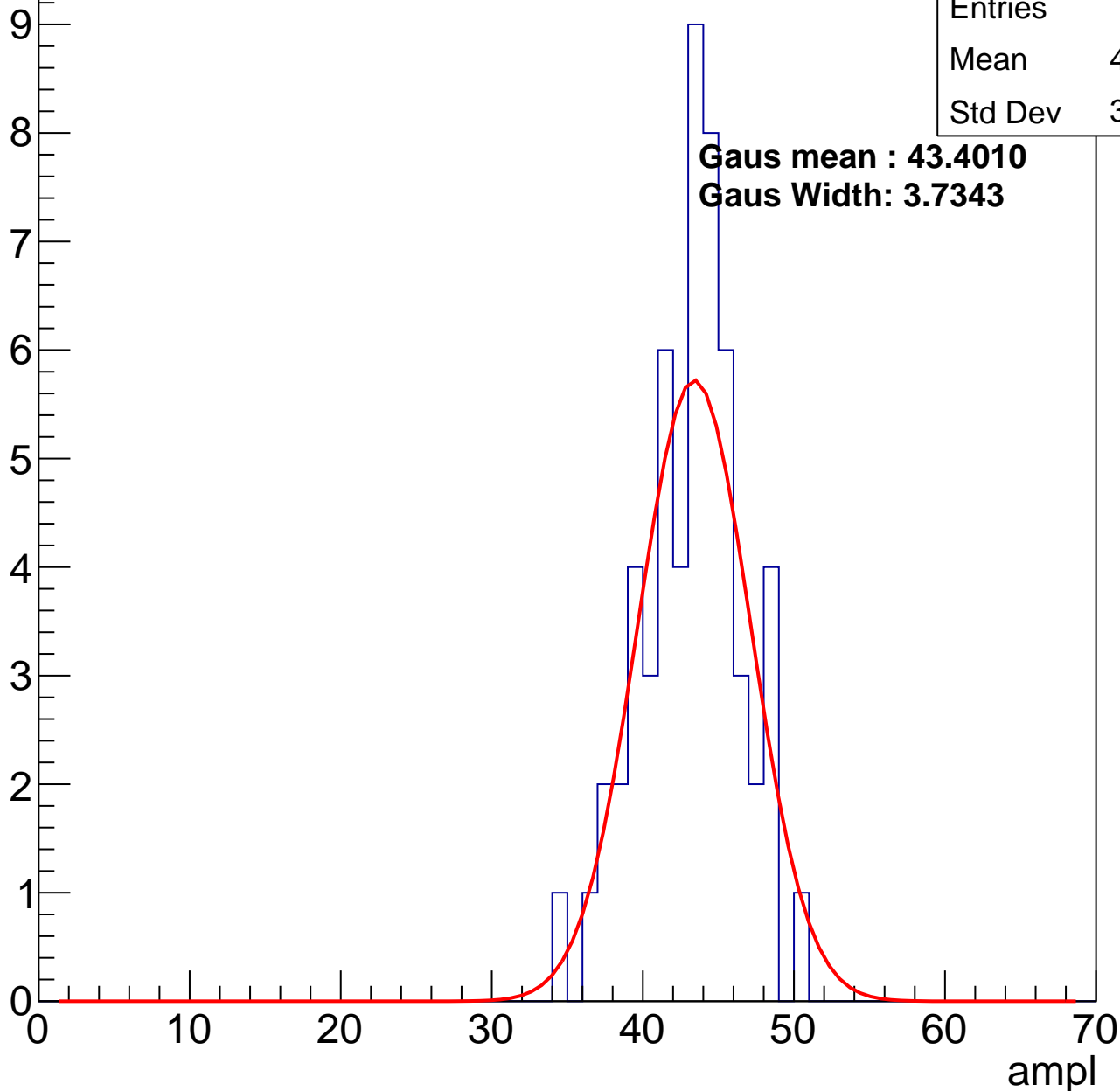
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 56    |
| Mean    | 42.73 |
| Std Dev | 3.292 |

**Gaus mean : 43.4010**

**Gaus Width: 3.7343**

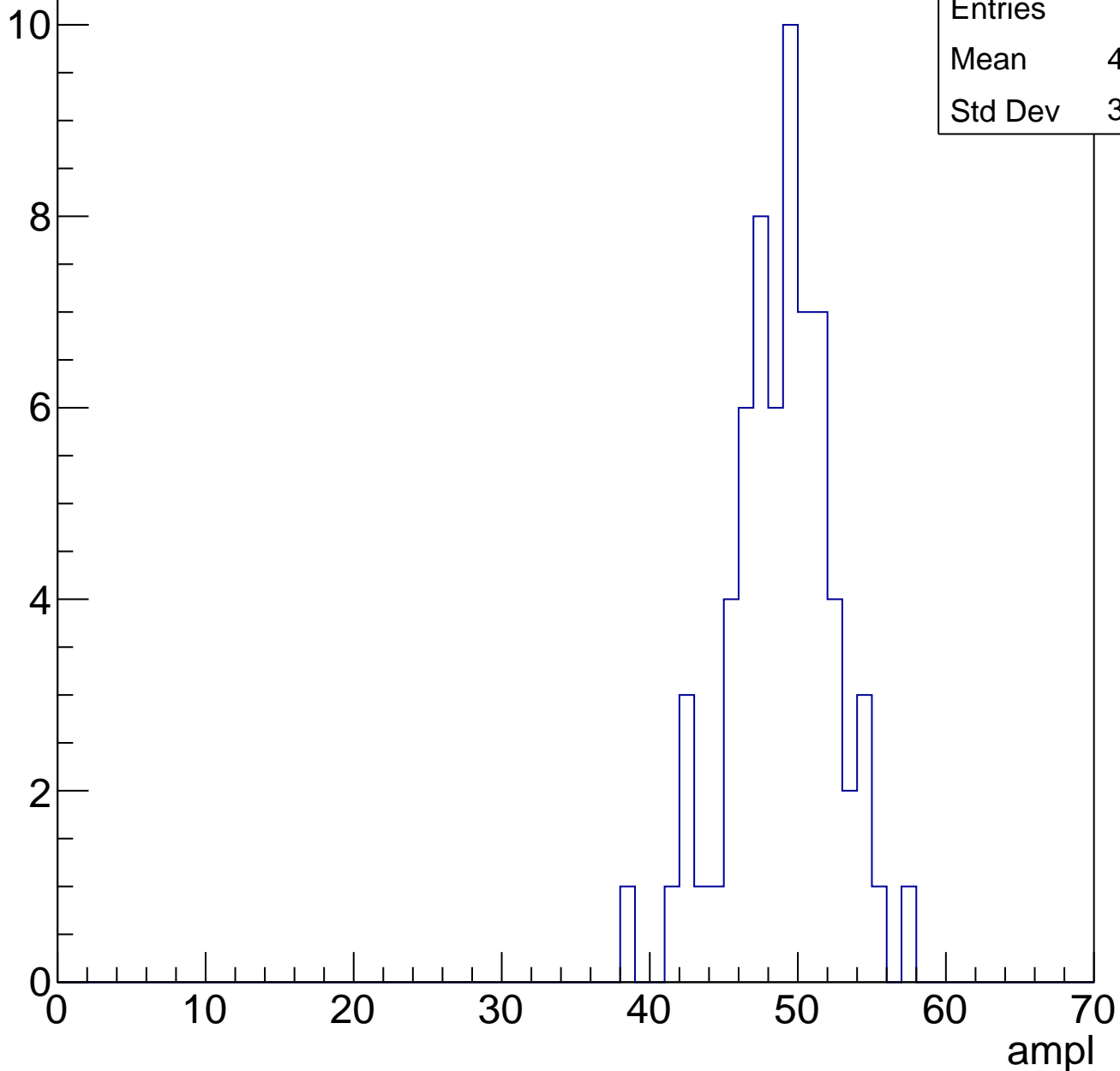


# B0L001S, U2-ch40, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

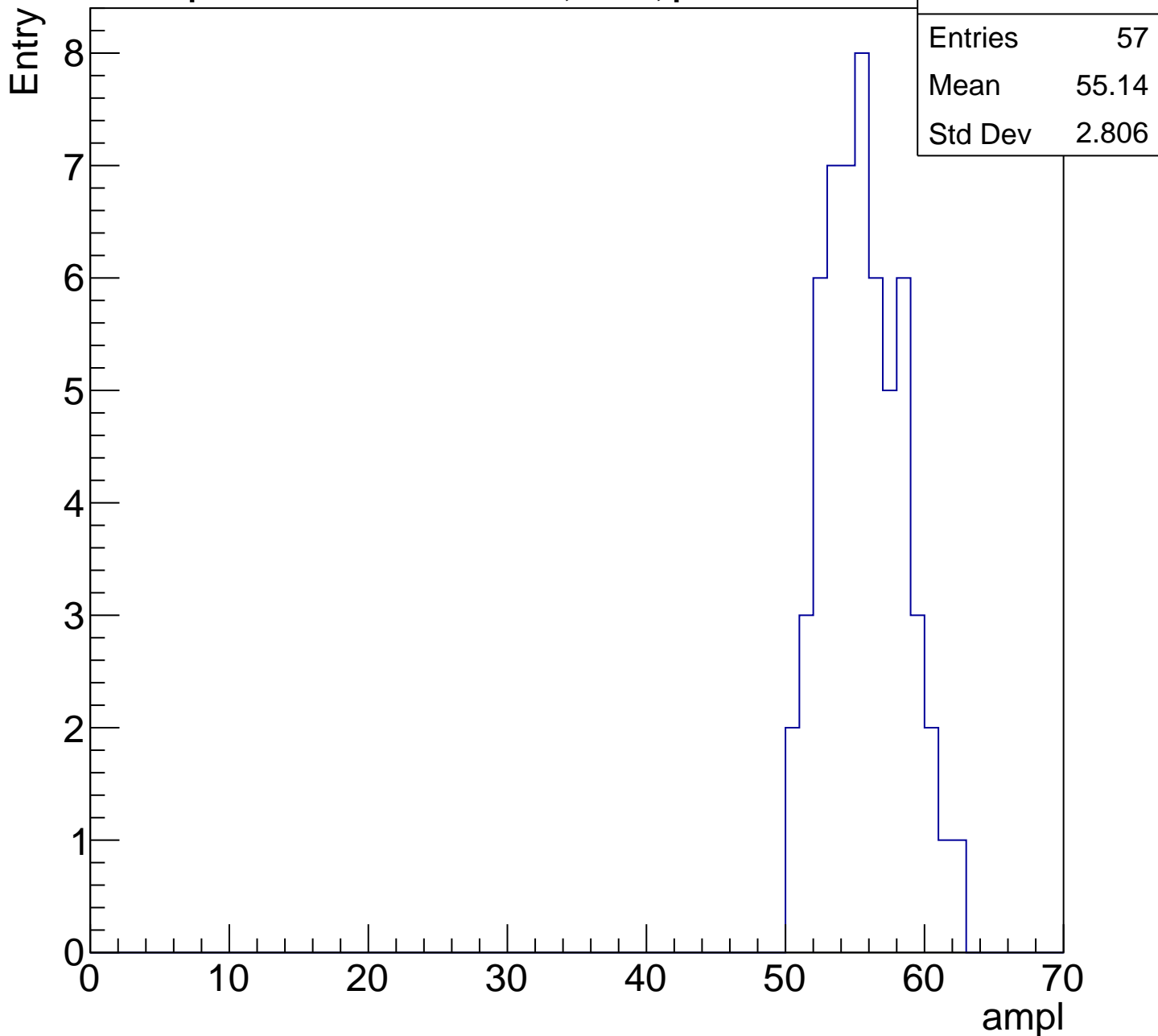
|         |       |
|---------|-------|
| Entries | 66    |
| Mean    | 48.44 |
| Std Dev | 3.495 |

Entry



# B0L001S, U2-ch40, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

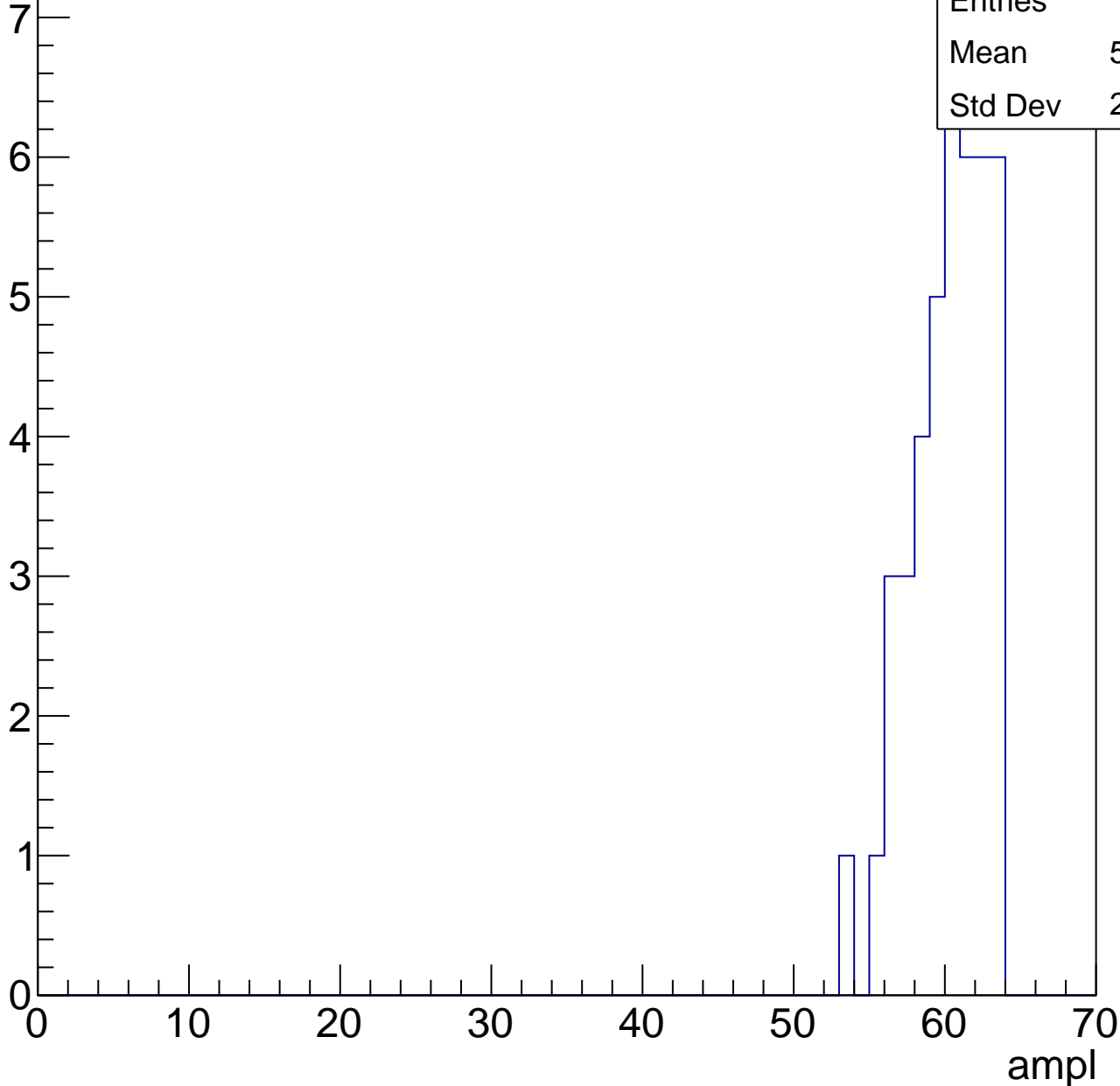


# B0L001S, U2-ch40, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

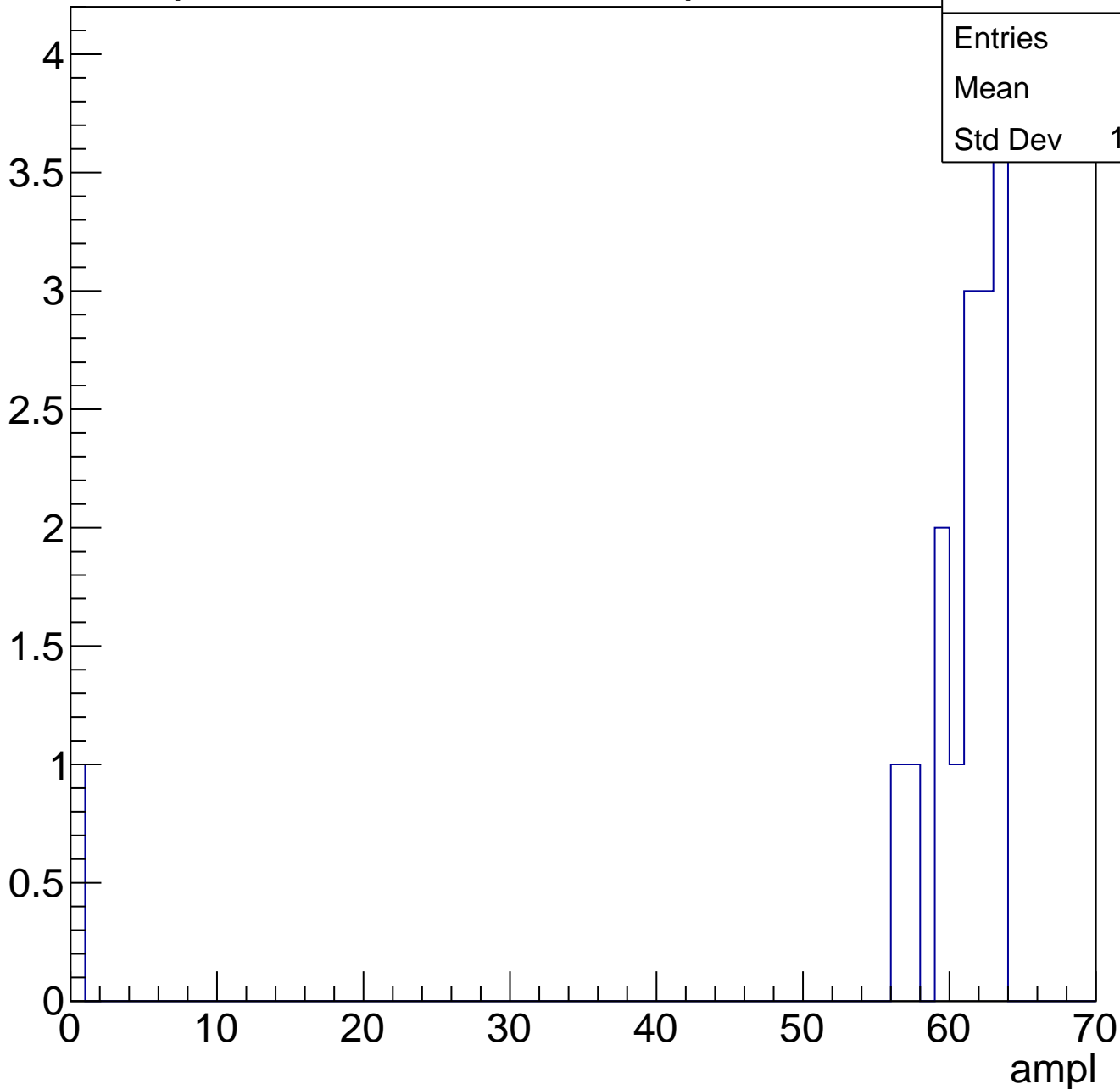
|         |       |
|---------|-------|
| Entries | 42    |
| Mean    | 59.76 |
| Std Dev | 2.448 |



# B0L001S, U2-ch40, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch40, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 1 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch41, adc0

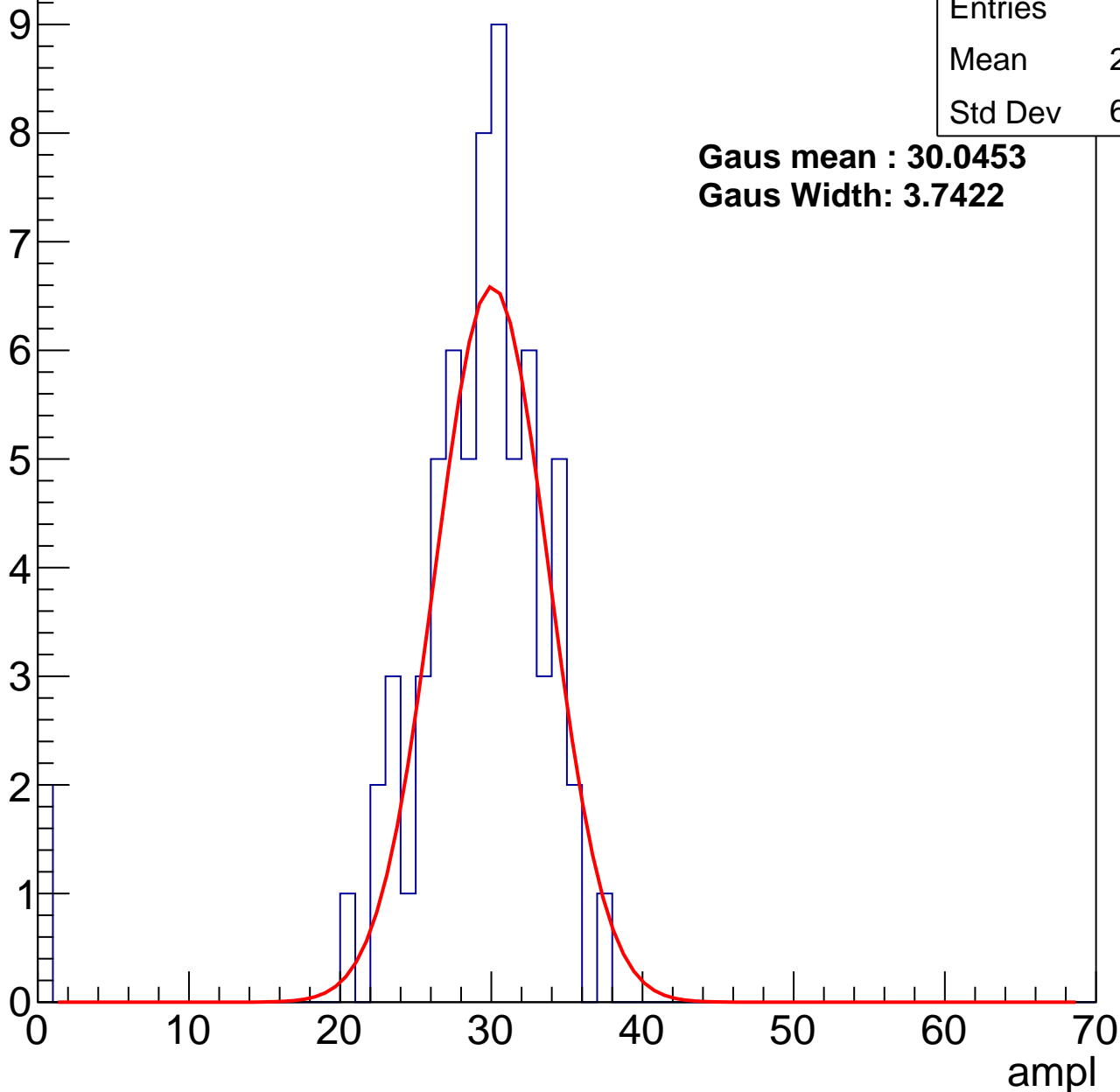
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 67    |
| Mean    | 28.19 |
| Std Dev | 6.065 |

**Gaus mean : 30.0453**

**Gaus Width: 3.7422**



# B0L001S, U2-ch41, adc1

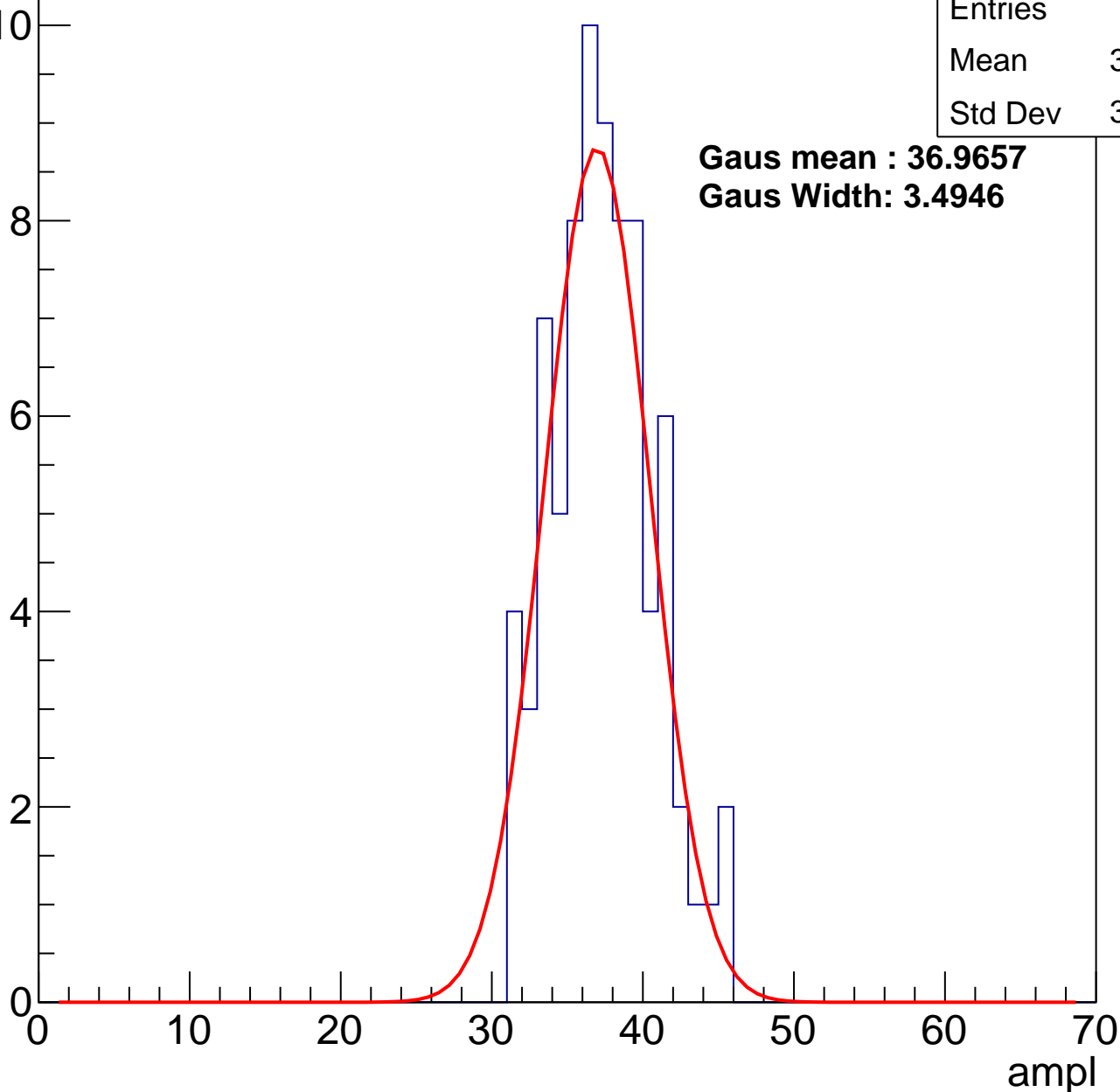
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 78    |
| Mean    | 36.88 |
| Std Dev | 3.305 |

**Gaus mean : 36.9657**

**Gaus Width: 3.4946**



# B0L001S, U2-ch41, adc2

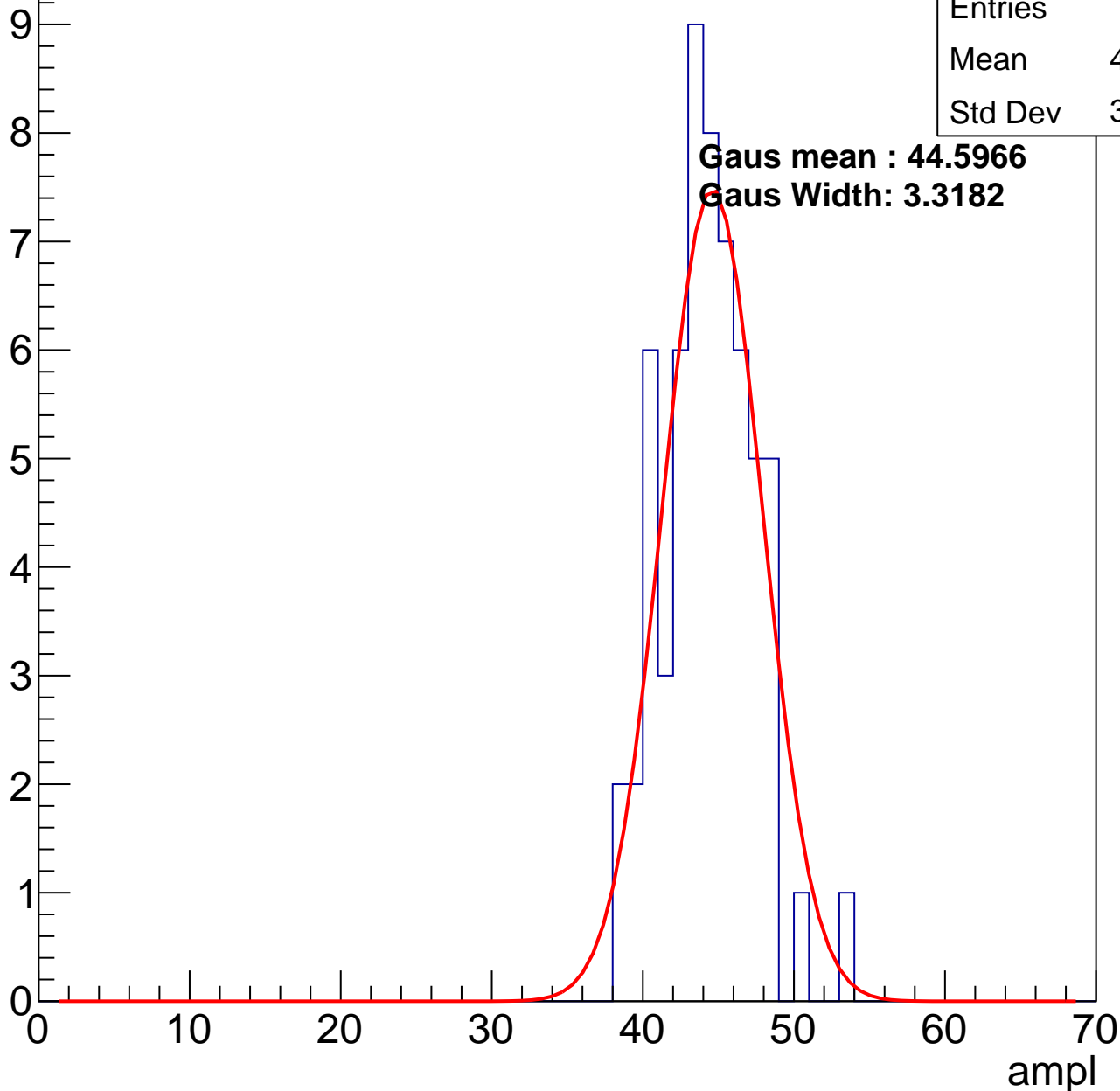
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 61    |
| Mean    | 43.89 |
| Std Dev | 3.003 |

**Gaus mean : 44.5966**

**Gaus Width: 3.3182**

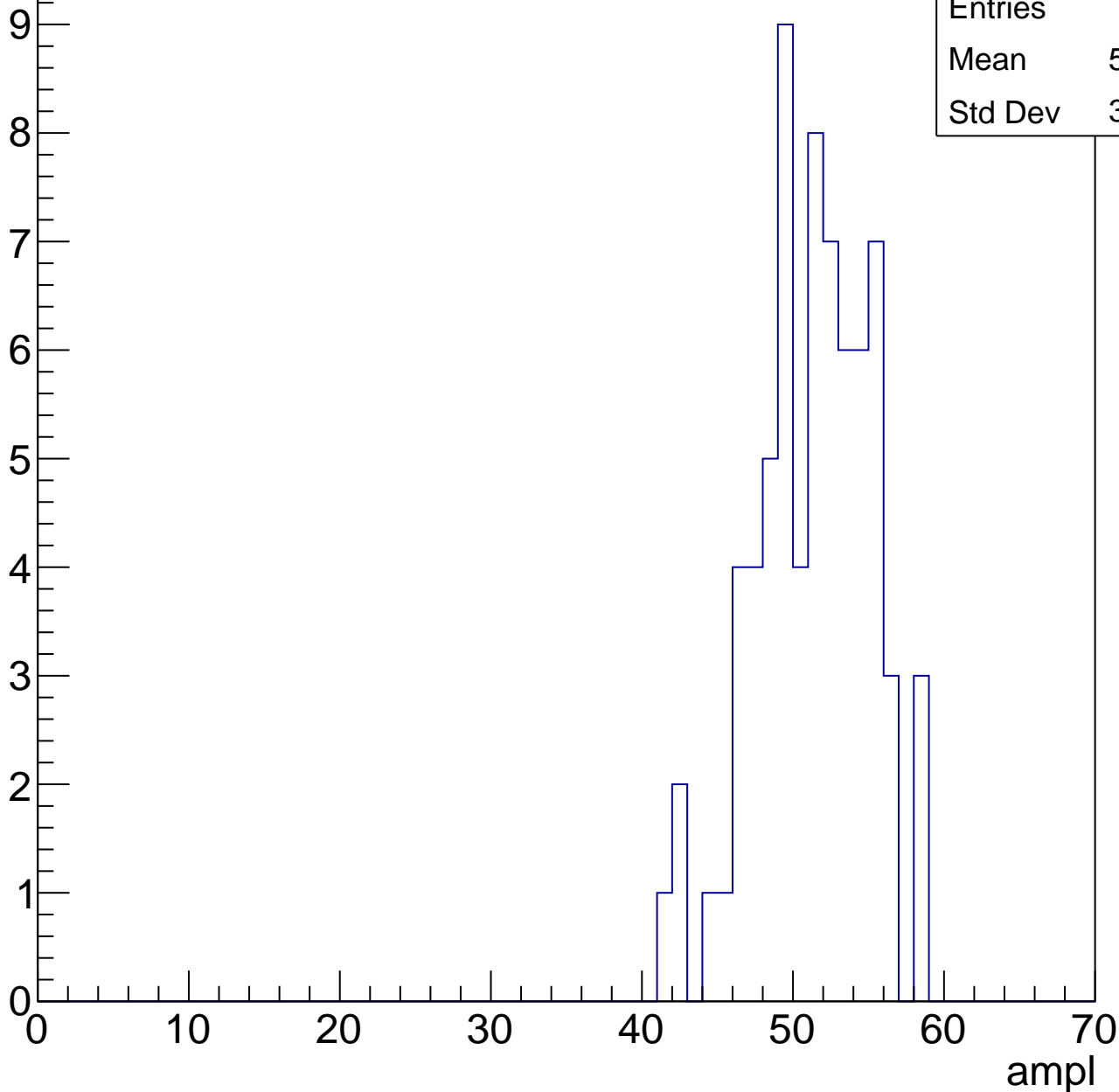


# B0L001S, U2-ch41, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 71    |
| Mean    | 50.82 |
| Std Dev | 3.777 |

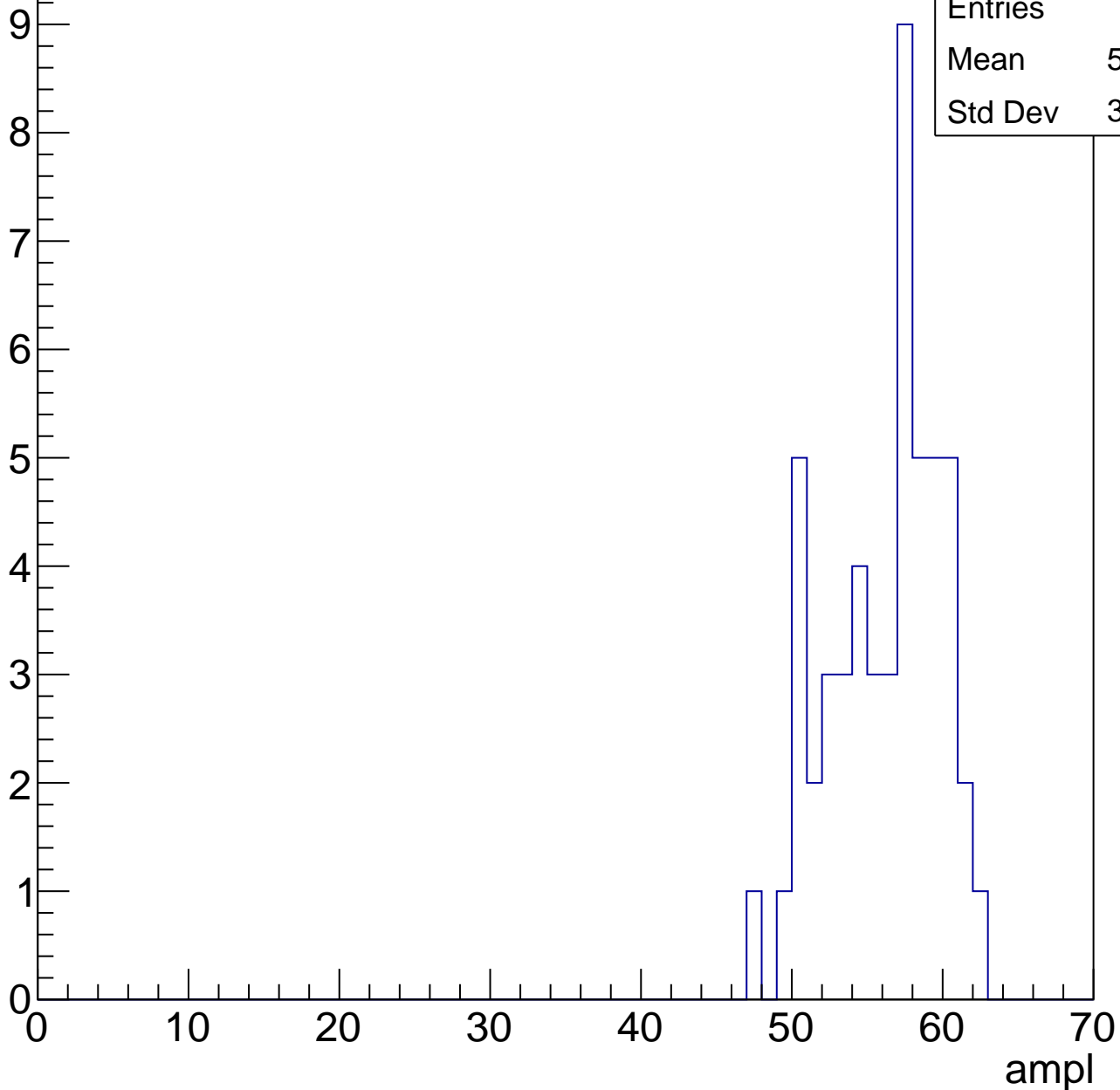


# B0L001S, U2-ch41, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 52    |
| Mean    | 55.65 |
| Std Dev | 3.637 |

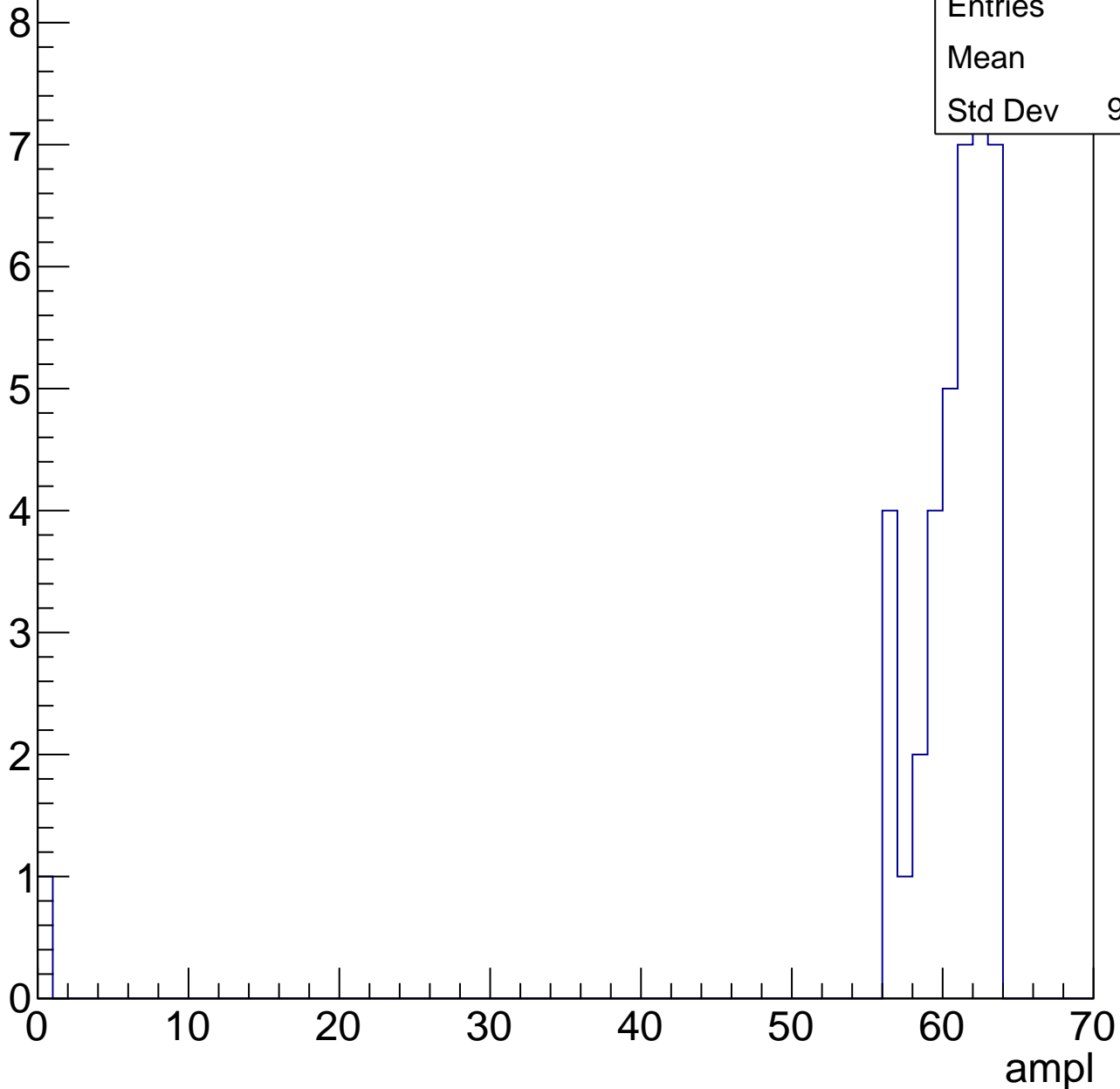


# B0L001S, U2-ch41, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

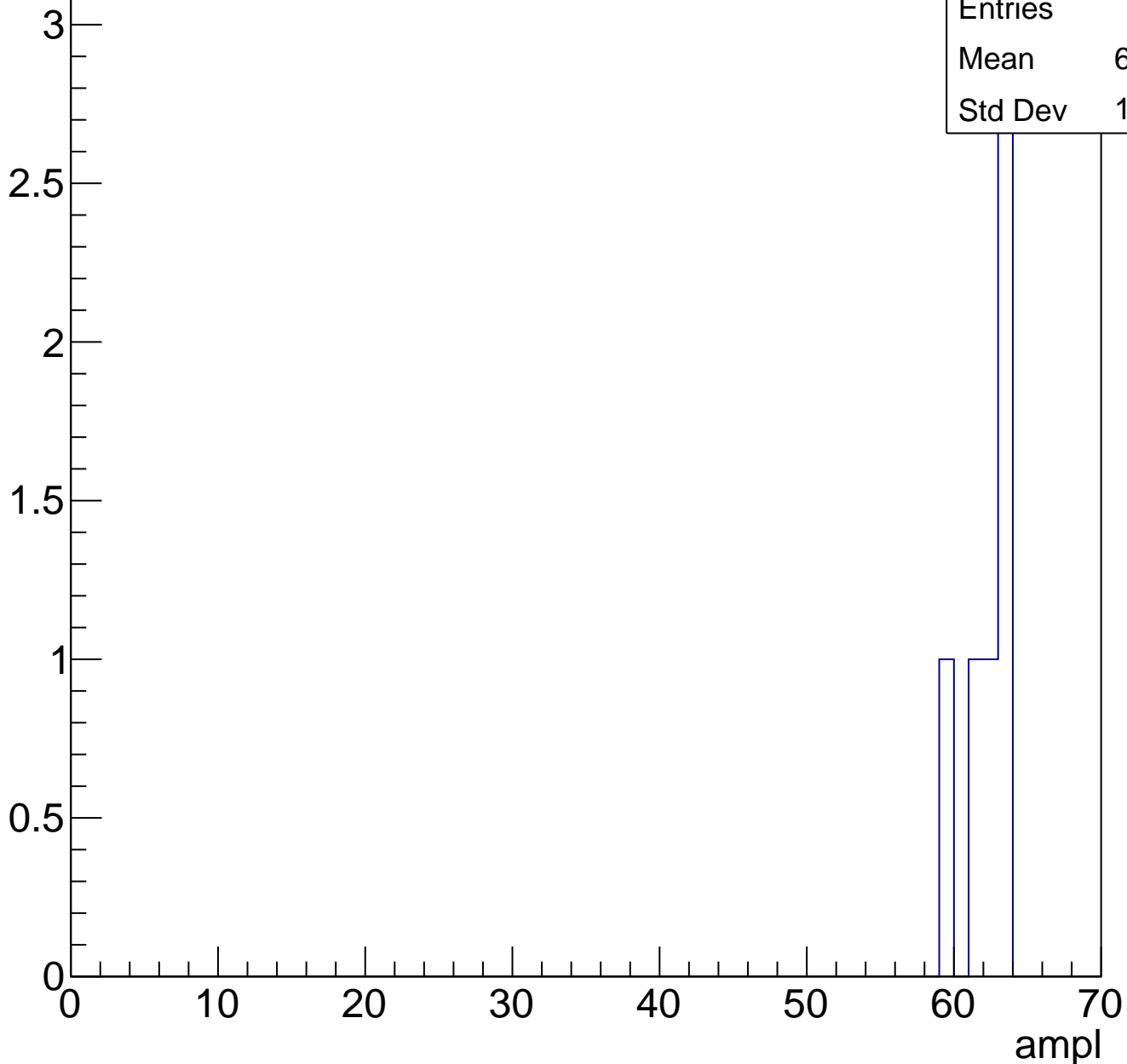
|         |       |
|---------|-------|
| Entries | 39    |
| Mean    | 58.9  |
| Std Dev | 9.792 |



# B0L001S, U2-ch41, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch41, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 0 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch42, adc0

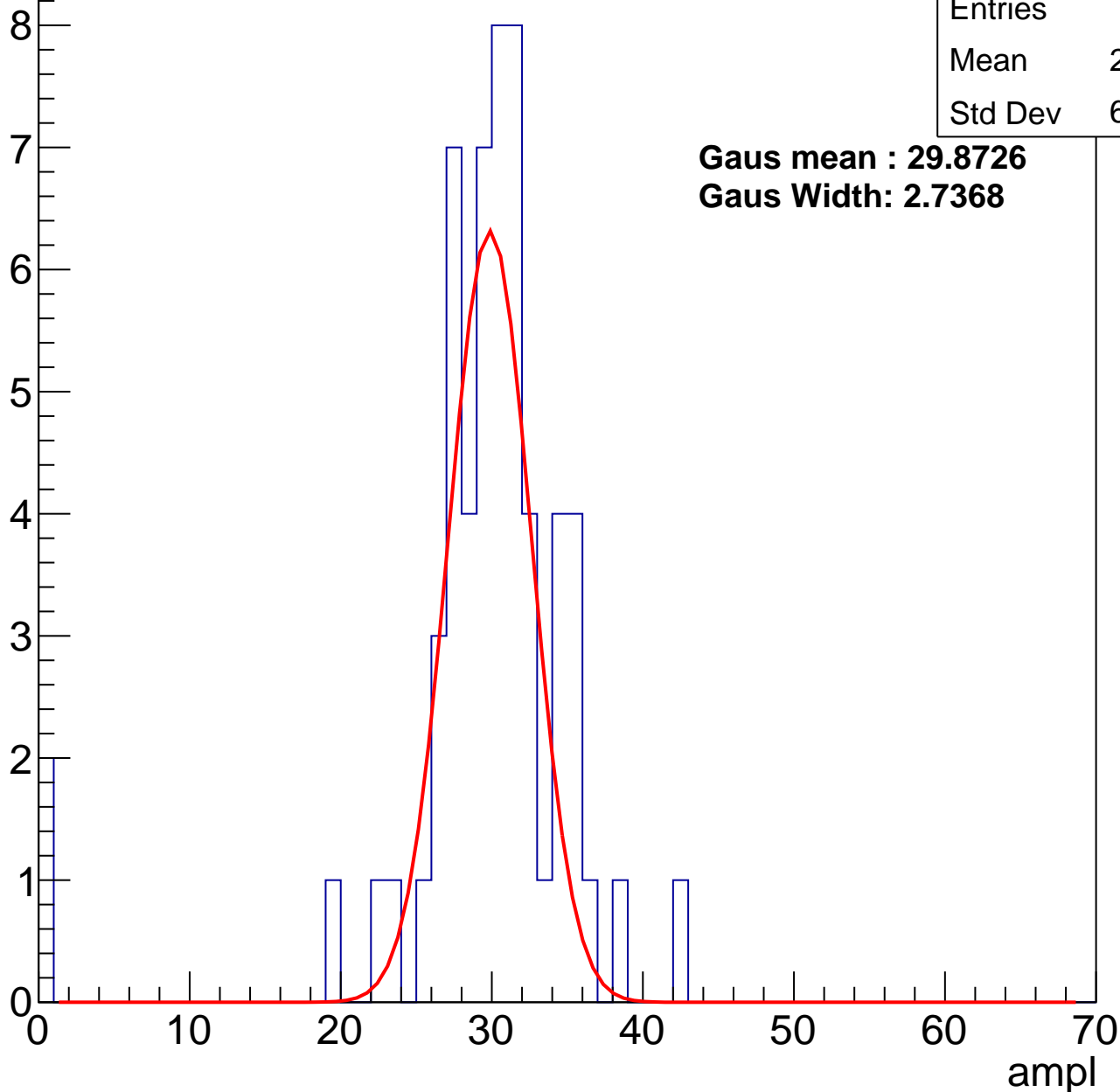
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 59    |
| Mean    | 29.02 |
| Std Dev | 6.609 |

**Gaus mean : 29.8726**

**Gaus Width: 2.7368**



# B0L001S, U2-ch42, adc1

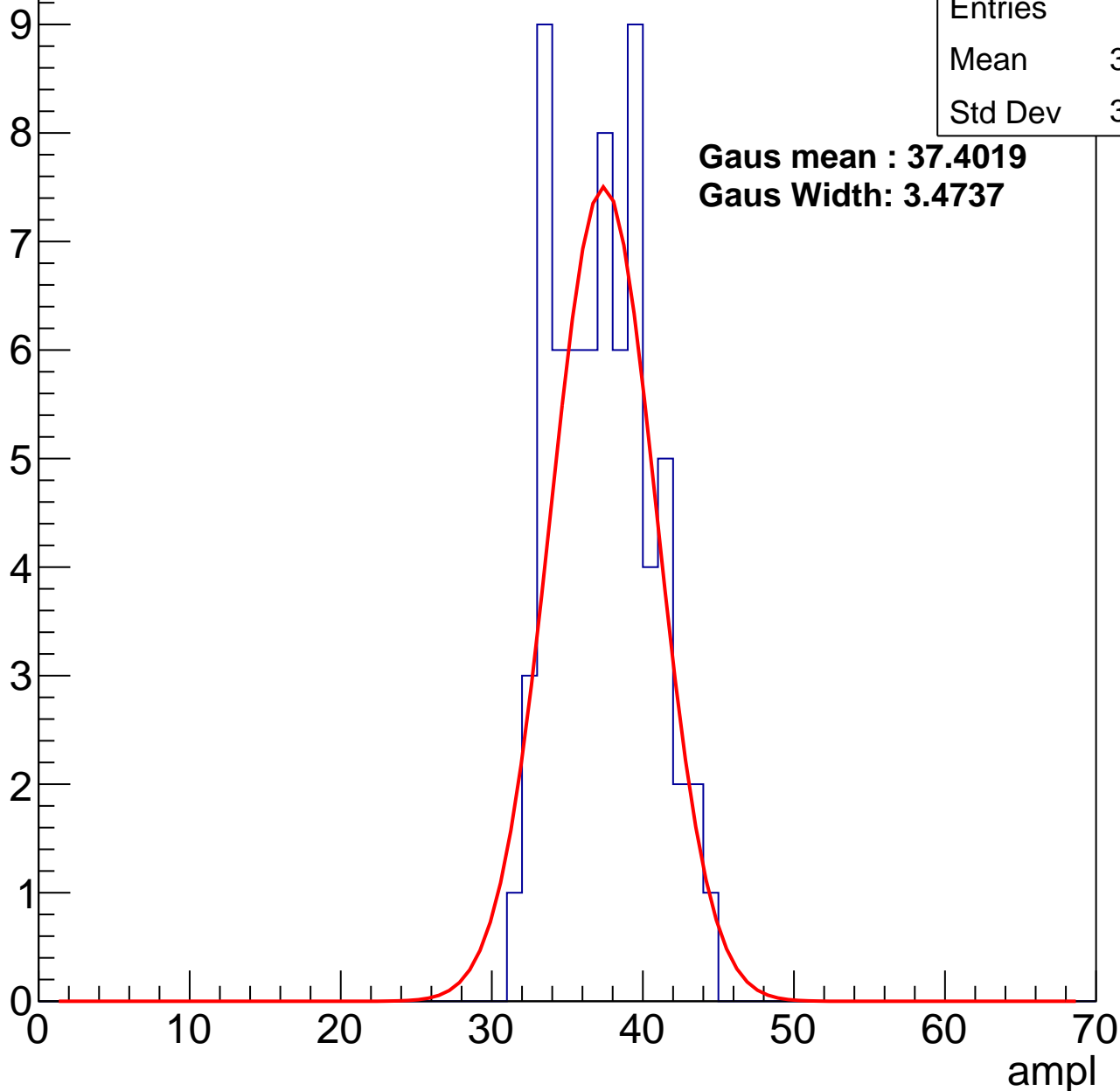
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 68    |
| Mean    | 36.88 |
| Std Dev | 3.132 |

**Gaus mean : 37.4019**

**Gaus Width: 3.4737**



# B0L001S, U2-ch42, adc2

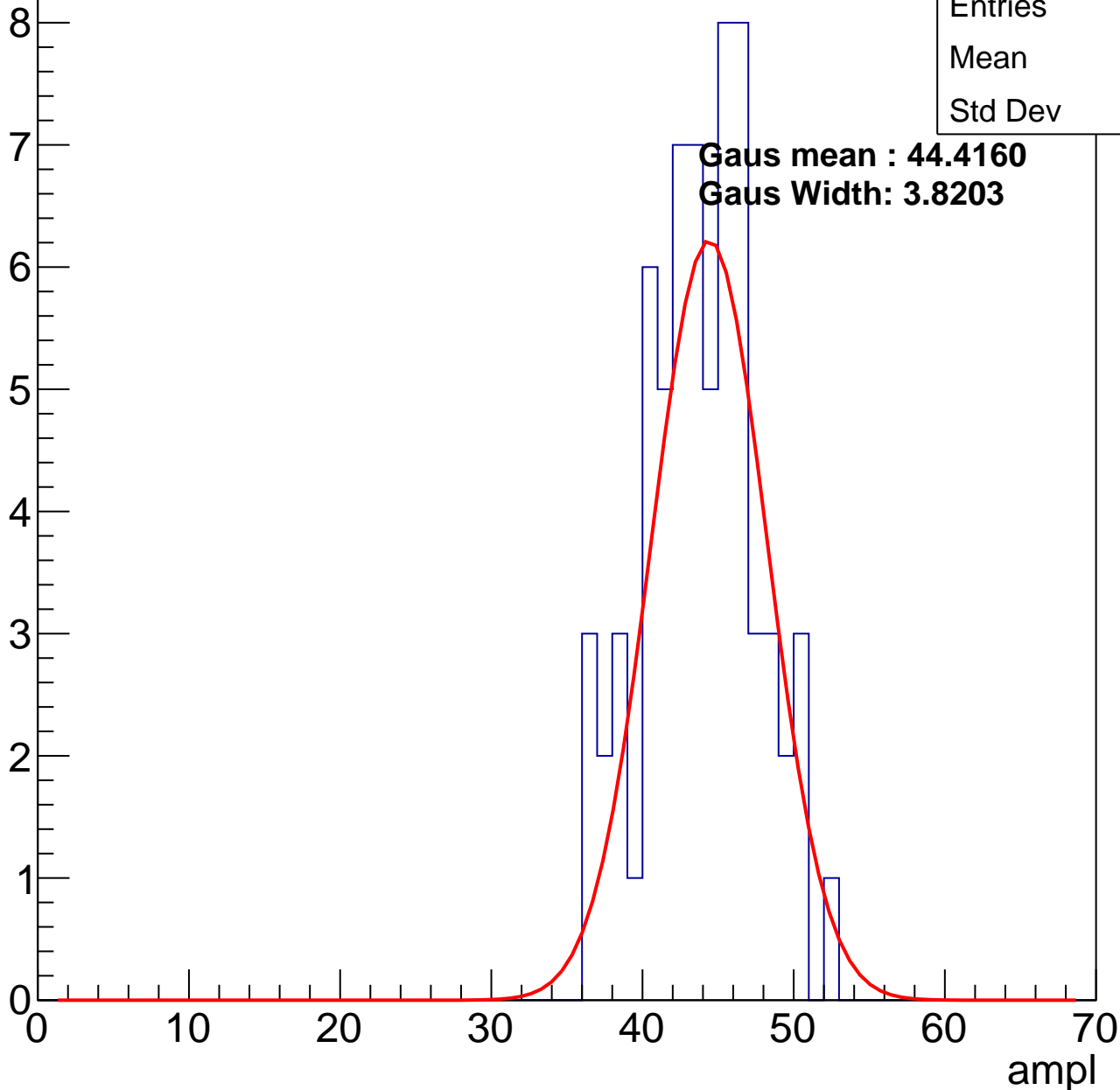
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |      |
|---------|------|
| Entries | 67   |
| Mean    | 43.4 |
| Std Dev | 3.69 |

**Gaus mean : 44.4160**

**Gaus Width: 3.8203**

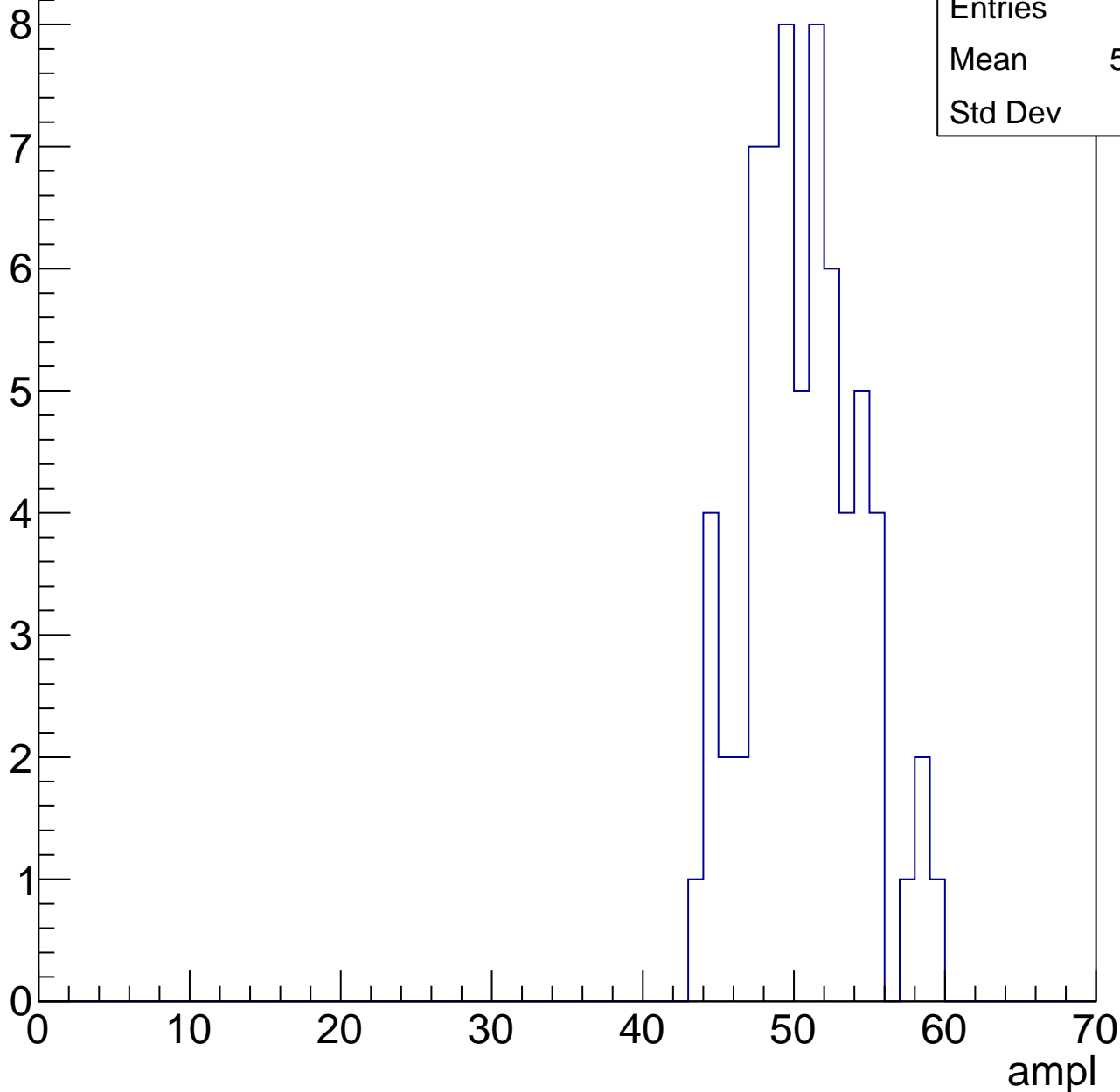


# B0L001S, U2-ch42, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 67    |
| Mean    | 50.18 |
| Std Dev | 3.62  |

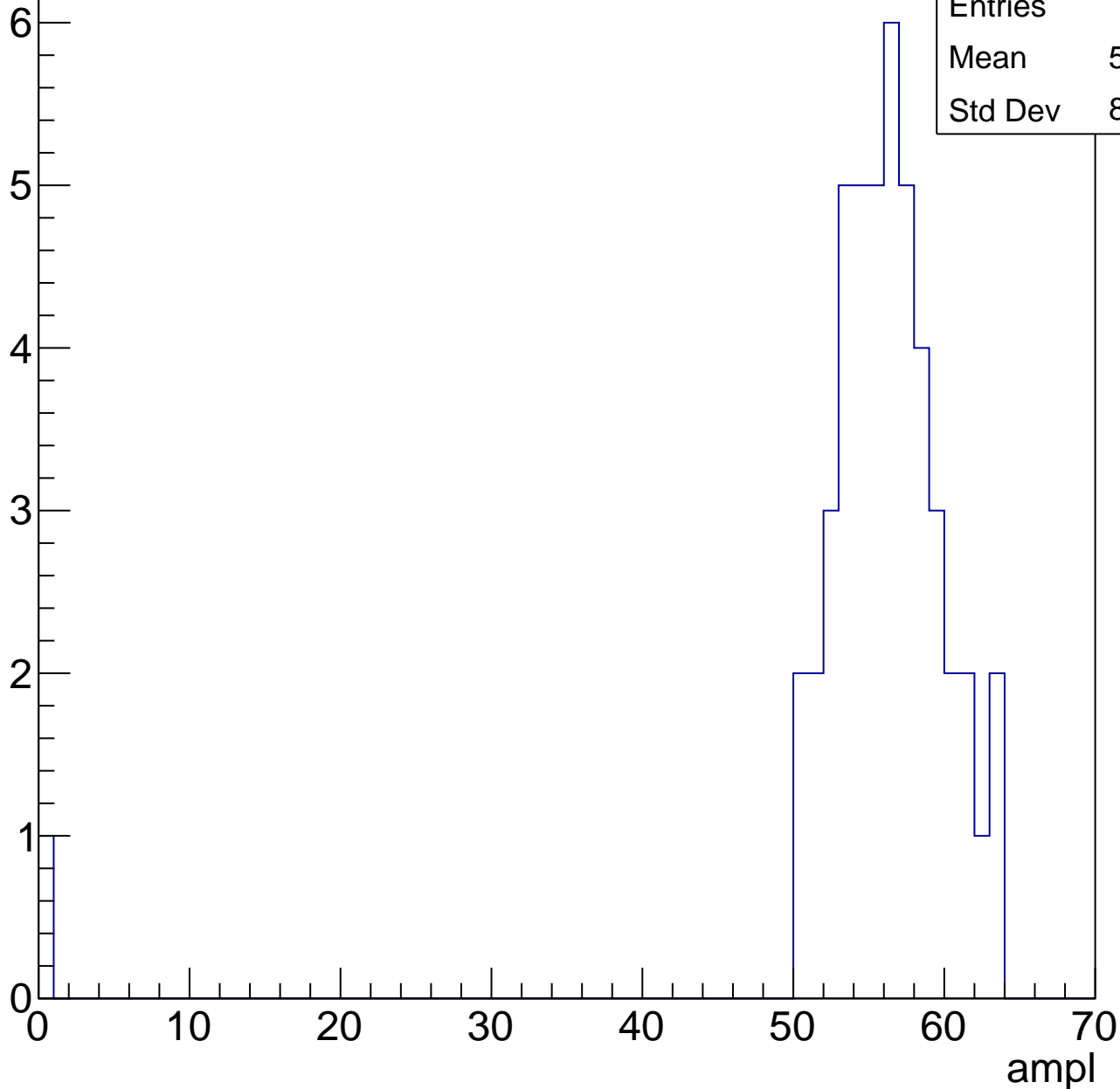


# B0L001S, U2-ch42, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 48    |
| Mean    | 54.75 |
| Std Dev | 8.618 |

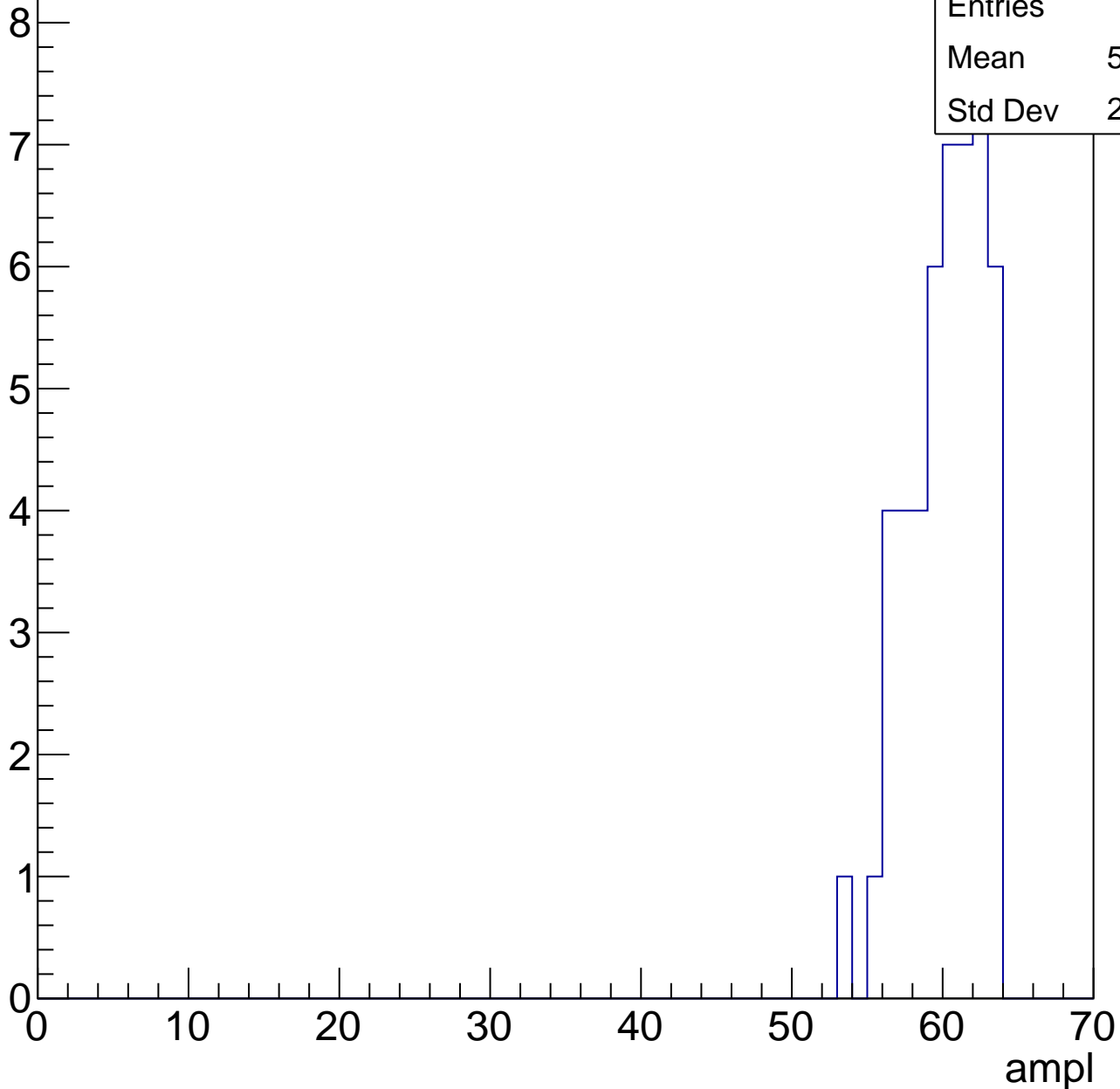


# B0L001S, U2-ch42, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 48    |
| Mean    | 59.73 |
| Std Dev | 2.439 |



# B0L001S, U2-ch42, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

0

10

20

30

40

50

60

70

ampl

|         |       |
|---------|-------|
| Entries | 5     |
| Mean    | 61.8  |
| Std Dev | 1.166 |



# B0L001S, U2-ch42, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U2-ch43, adc0

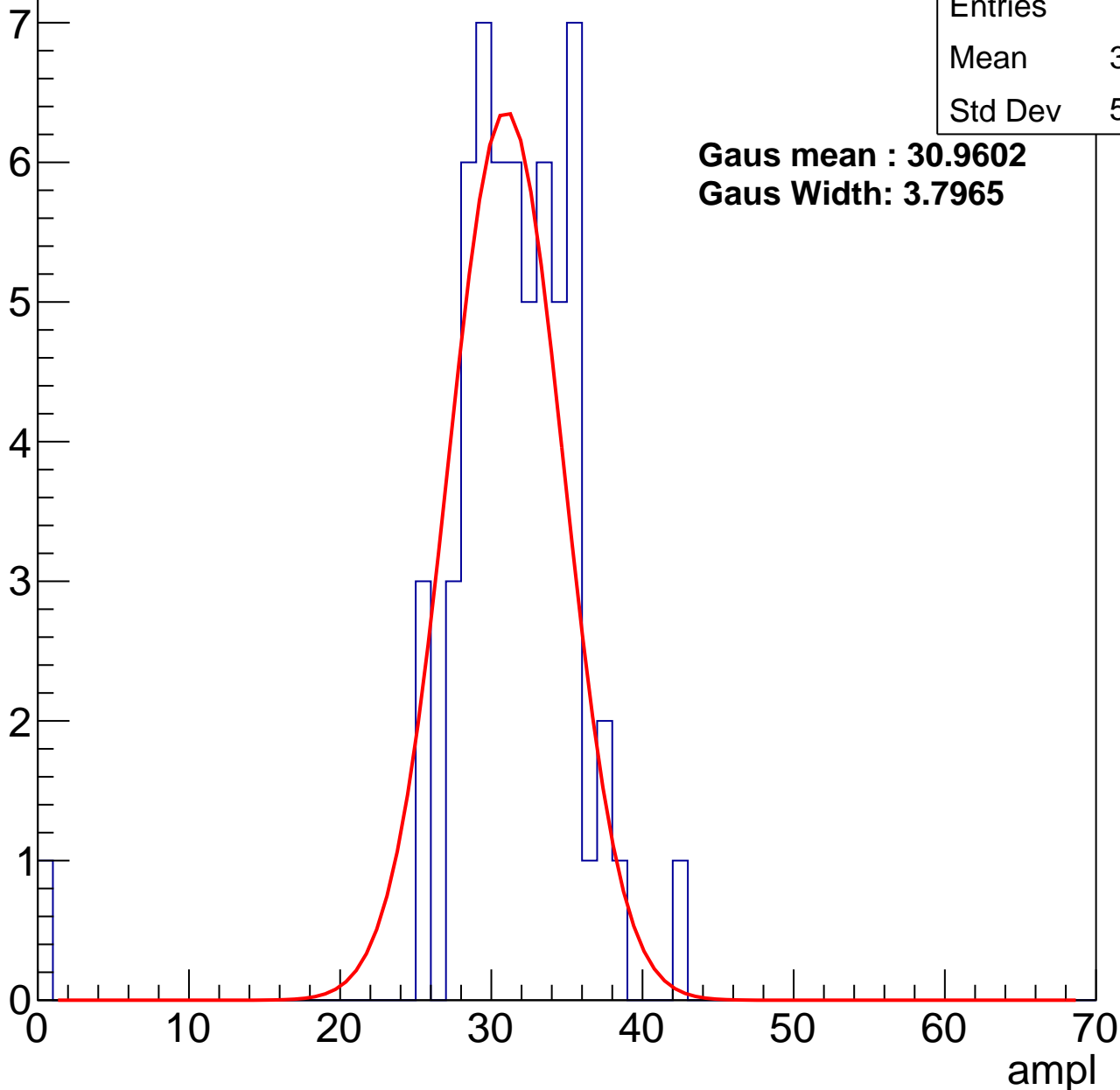
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 60    |
| Mean    | 30.93 |
| Std Dev | 5.256 |

**Gaus mean : 30.9602**

**Gaus Width: 3.7965**



# B0L001S, U2-ch43, adc1

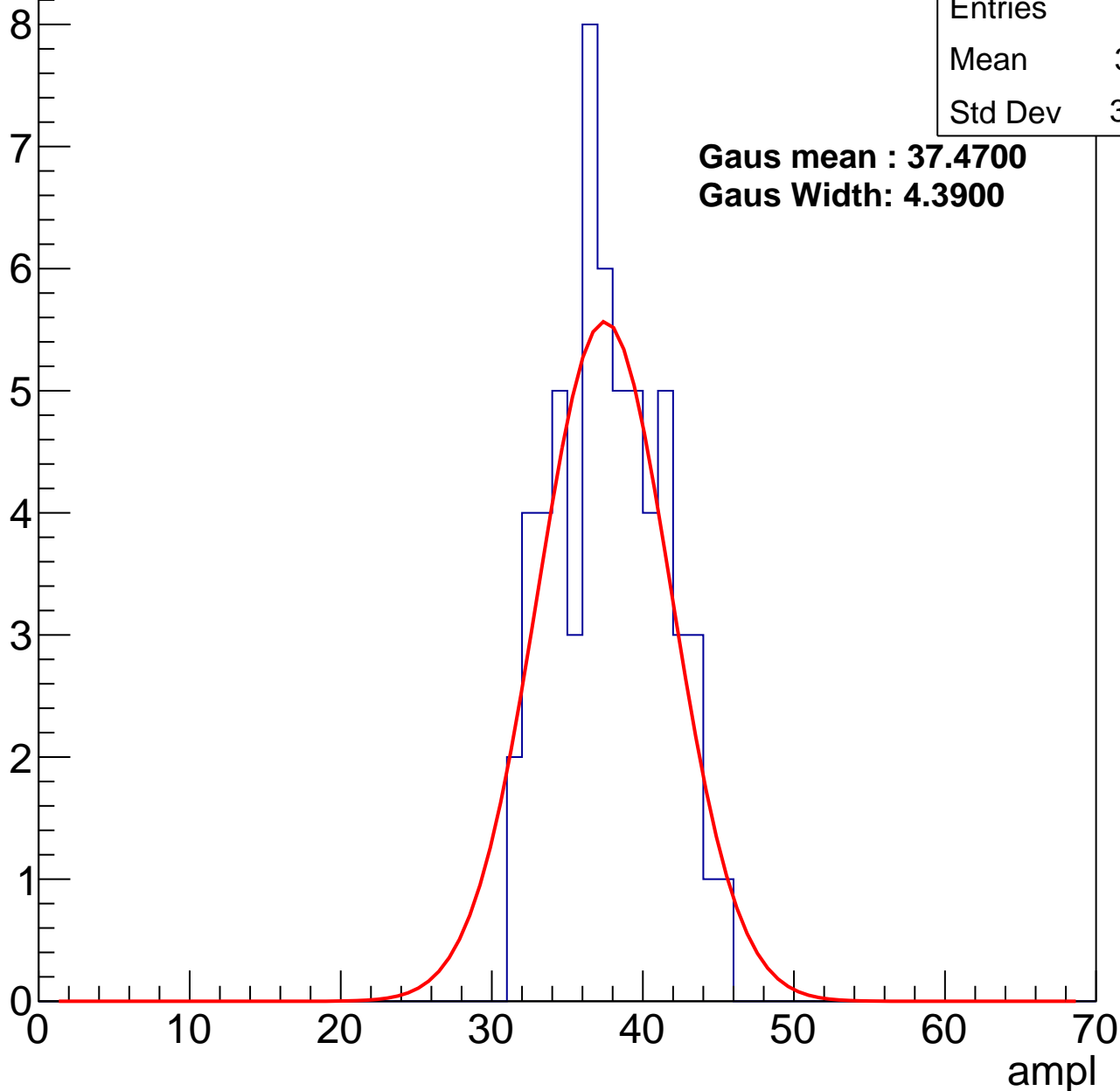
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 59    |
| Mean    | 37.31 |
| Std Dev | 3.524 |

**Gaus mean : 37.4700**

**Gaus Width: 4.3900**



# B0L001S, U2-ch43, adc2

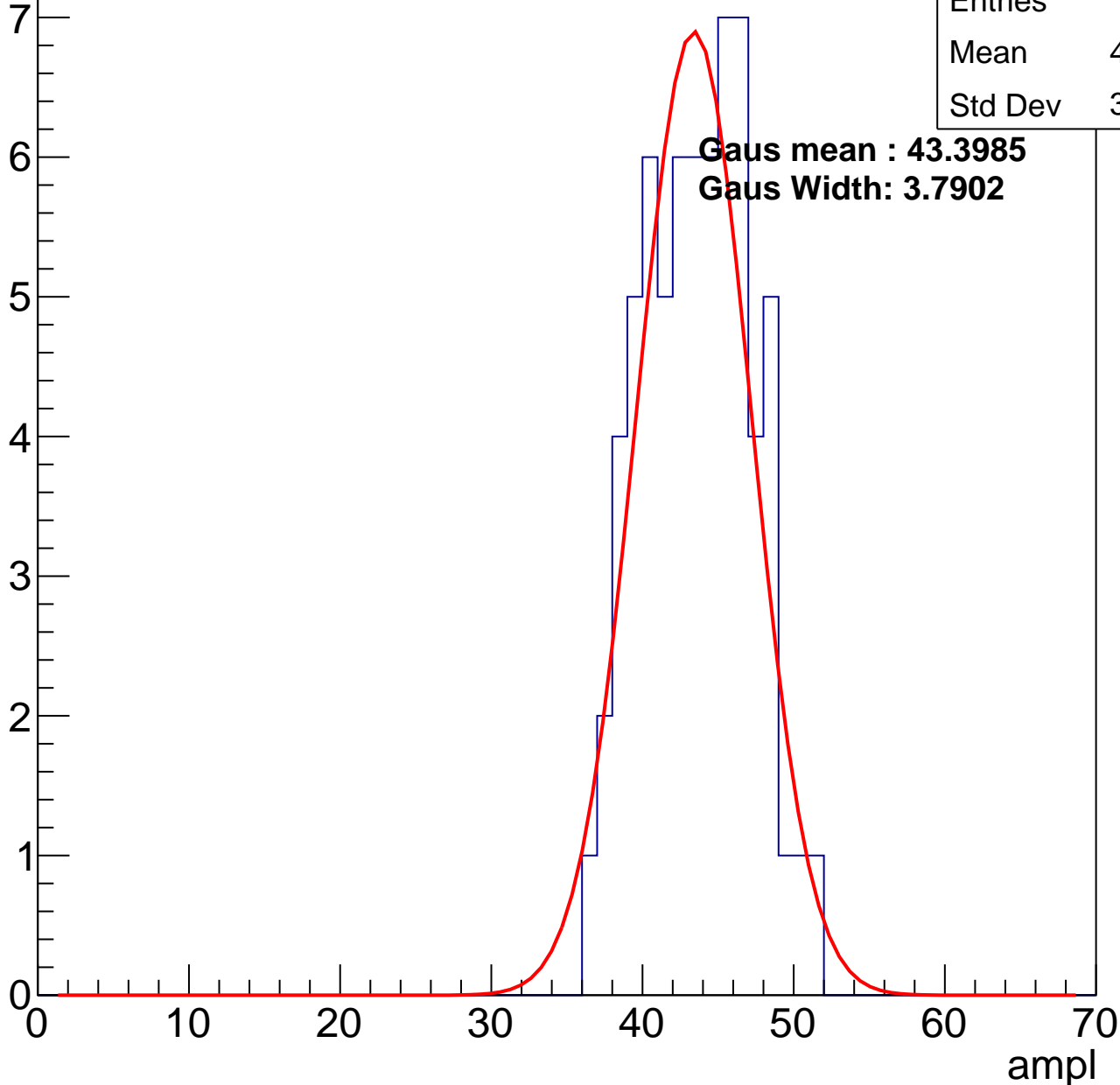
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 67    |
| Mean    | 43.15 |
| Std Dev | 3.487 |

**Gaus mean : 43.3985**

**Gaus Width: 3.7902**

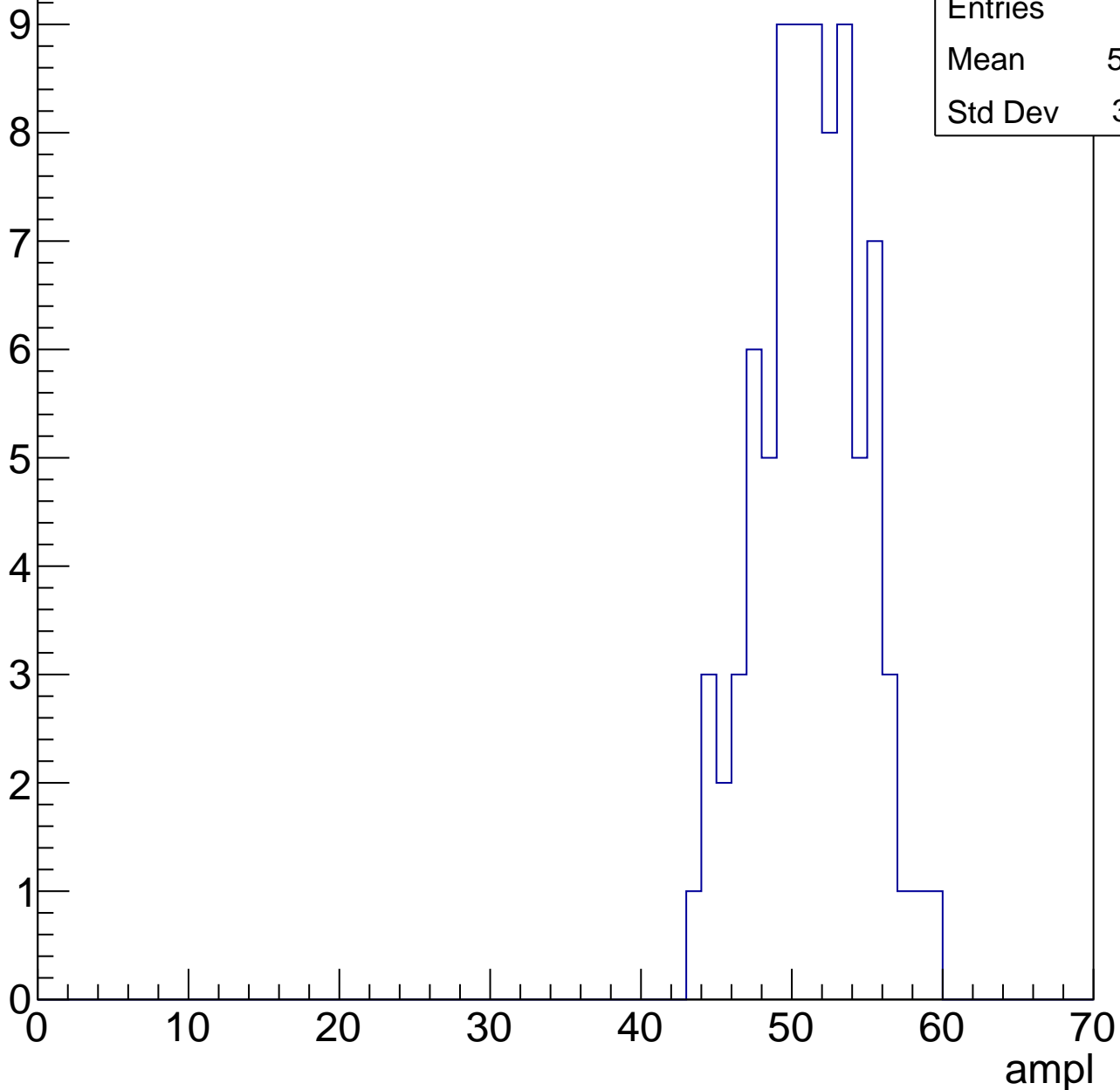


# B0L001S, U2-ch43, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

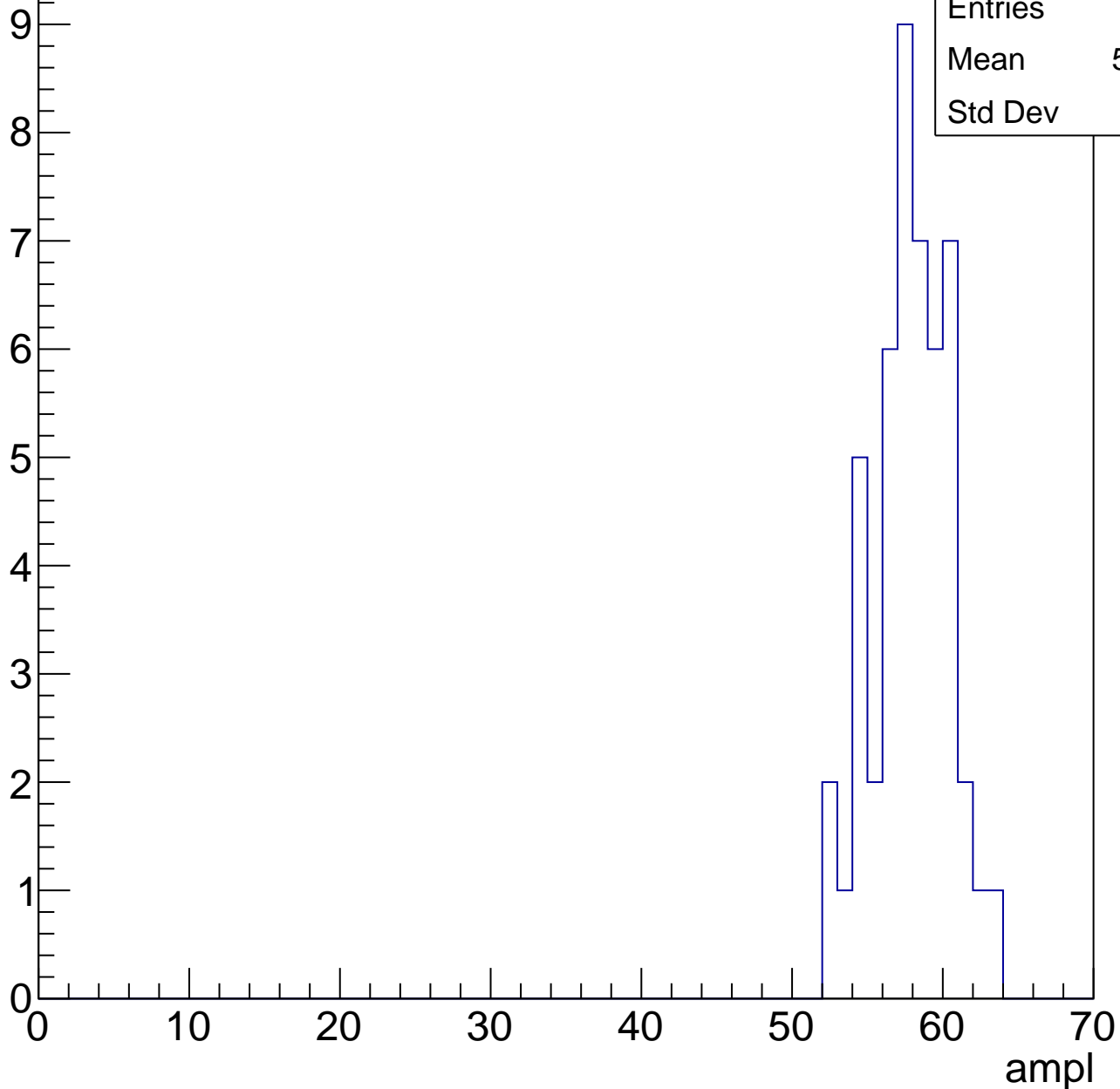
|         |       |
|---------|-------|
| Entries | 82    |
| Mean    | 50.79 |
| Std Dev | 3.431 |



# B0L001S, U2-ch43, adc4

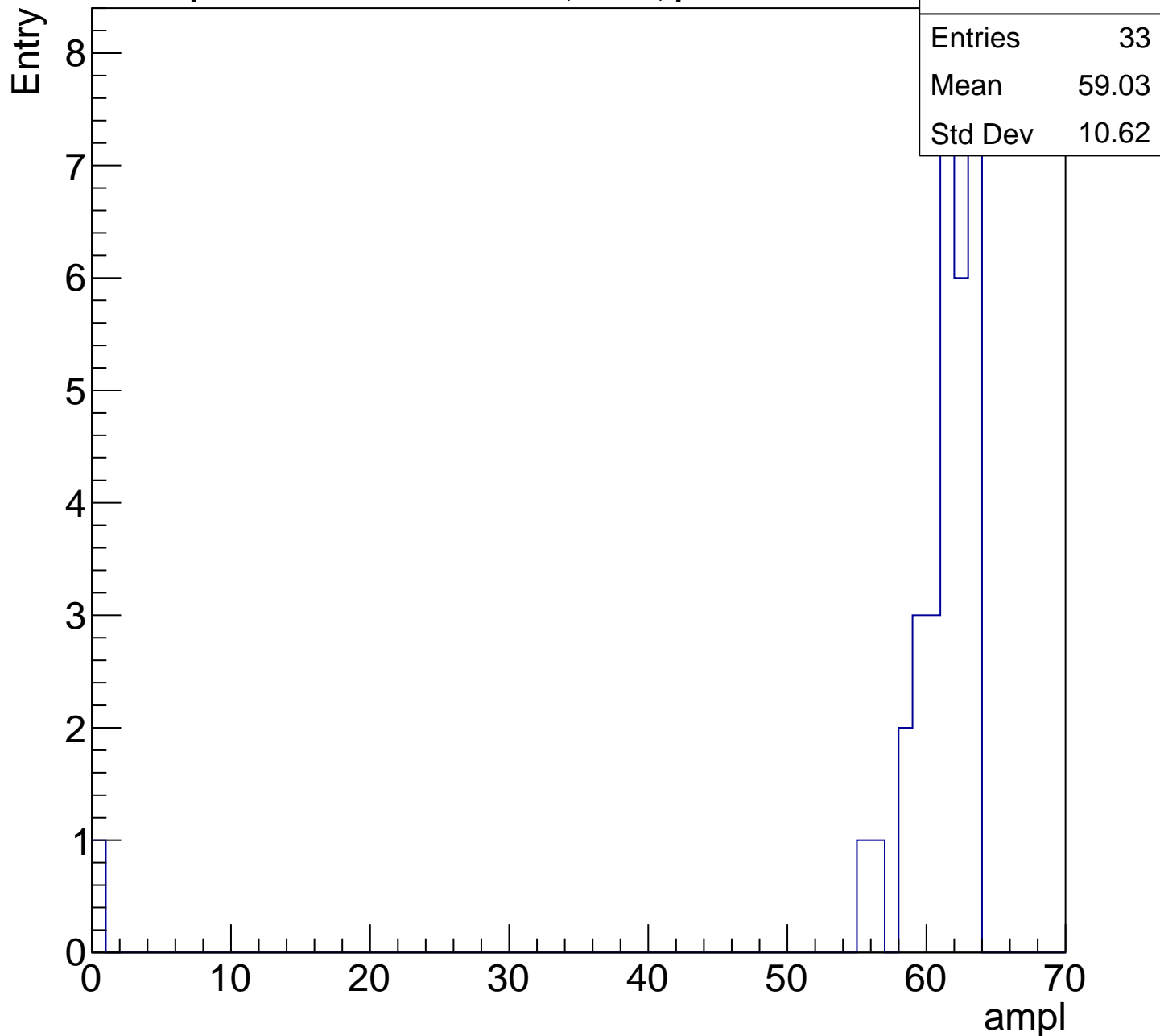
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U2-ch43, adc5

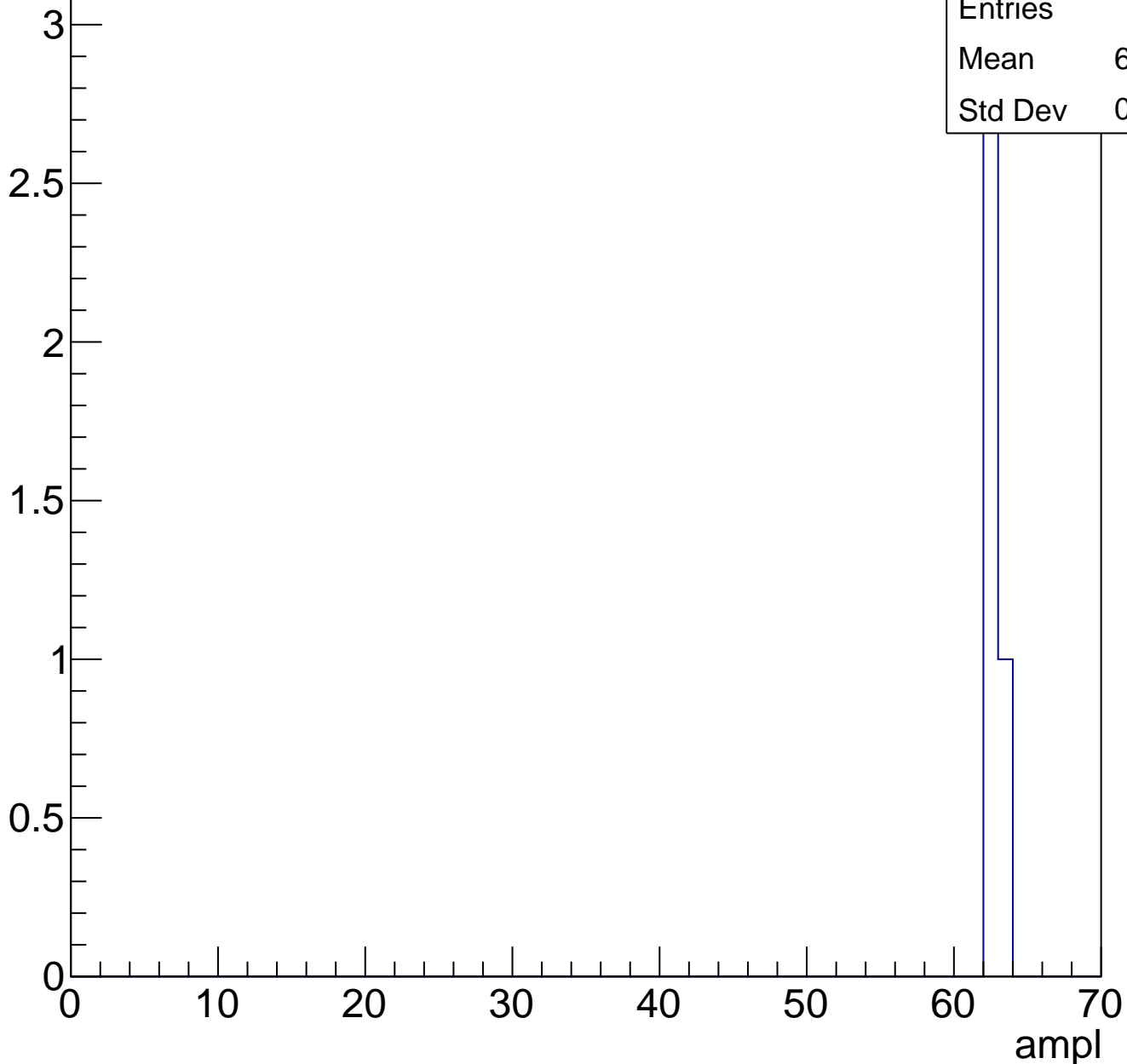
calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U2-ch43, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch43, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 3 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch44, adc0

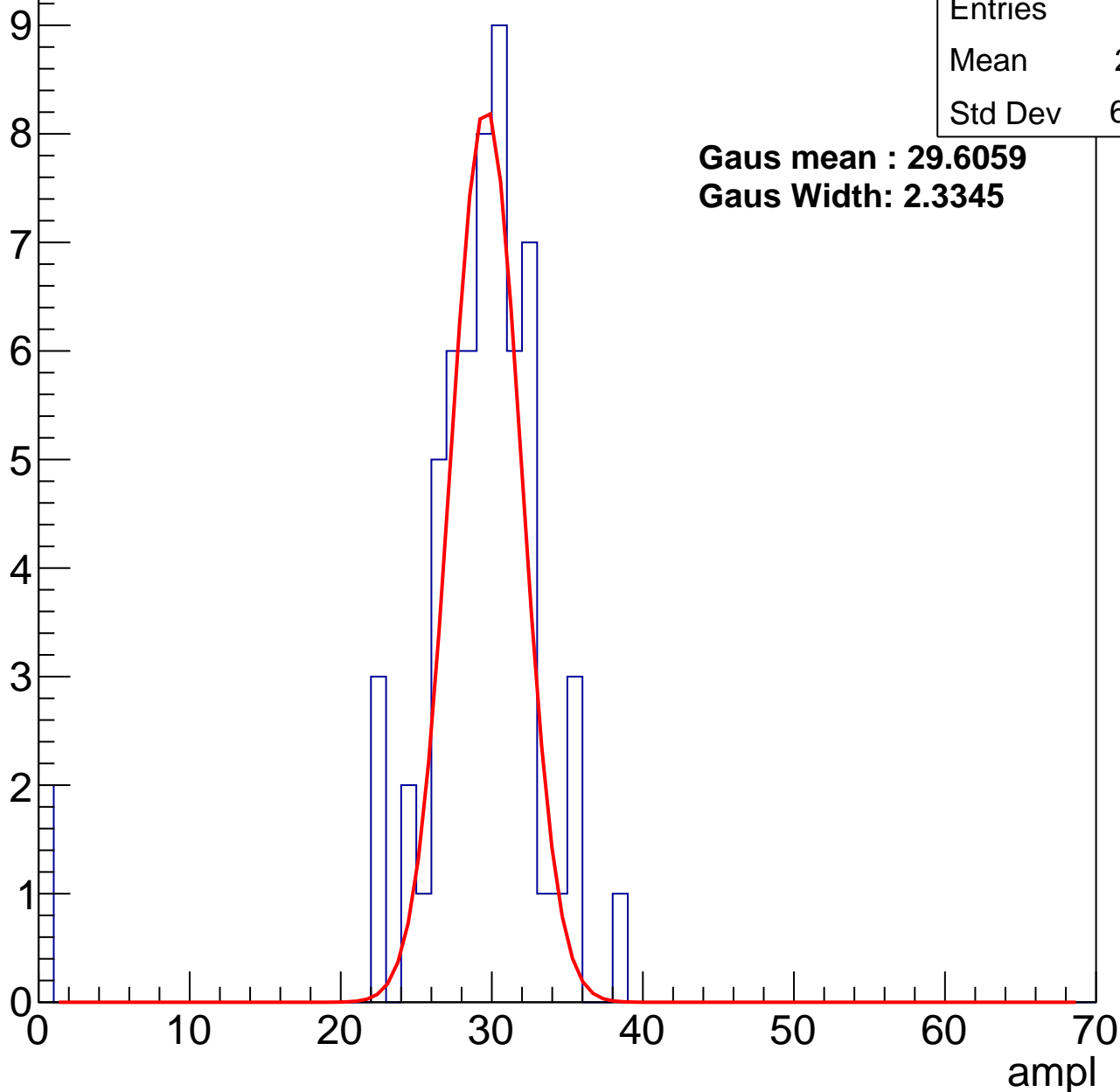
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 61    |
| Mean    | 28.21 |
| Std Dev | 6.084 |

**Gaus mean : 29.6059**

**Gaus Width: 2.3345**



# B0L001S, U2-ch44, adc1

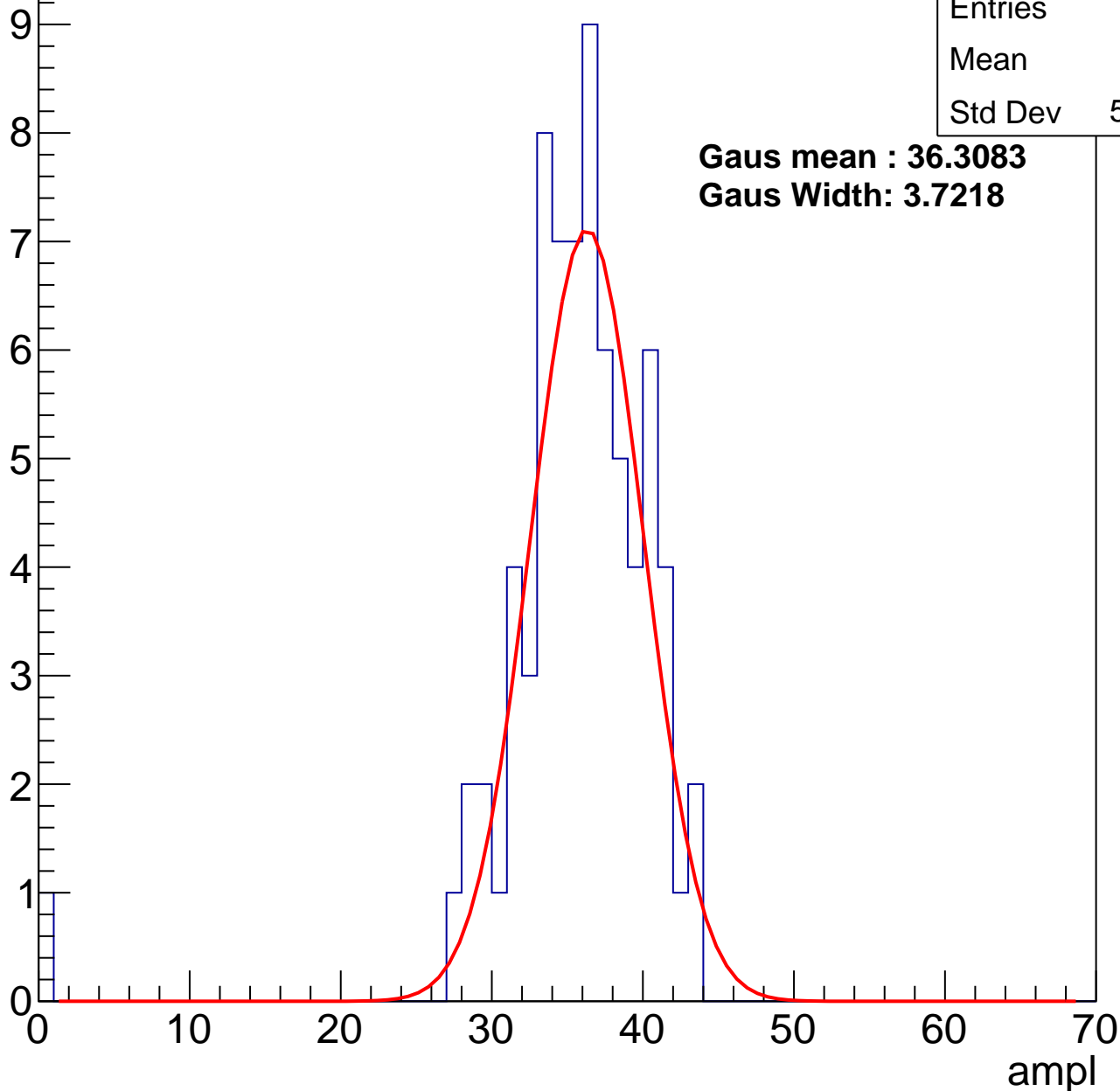
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 73    |
| Mean    | 35.1  |
| Std Dev | 5.522 |

**Gaus mean : 36.3083**

**Gaus Width: 3.7218**



# B0L001S, U2-ch44, adc2

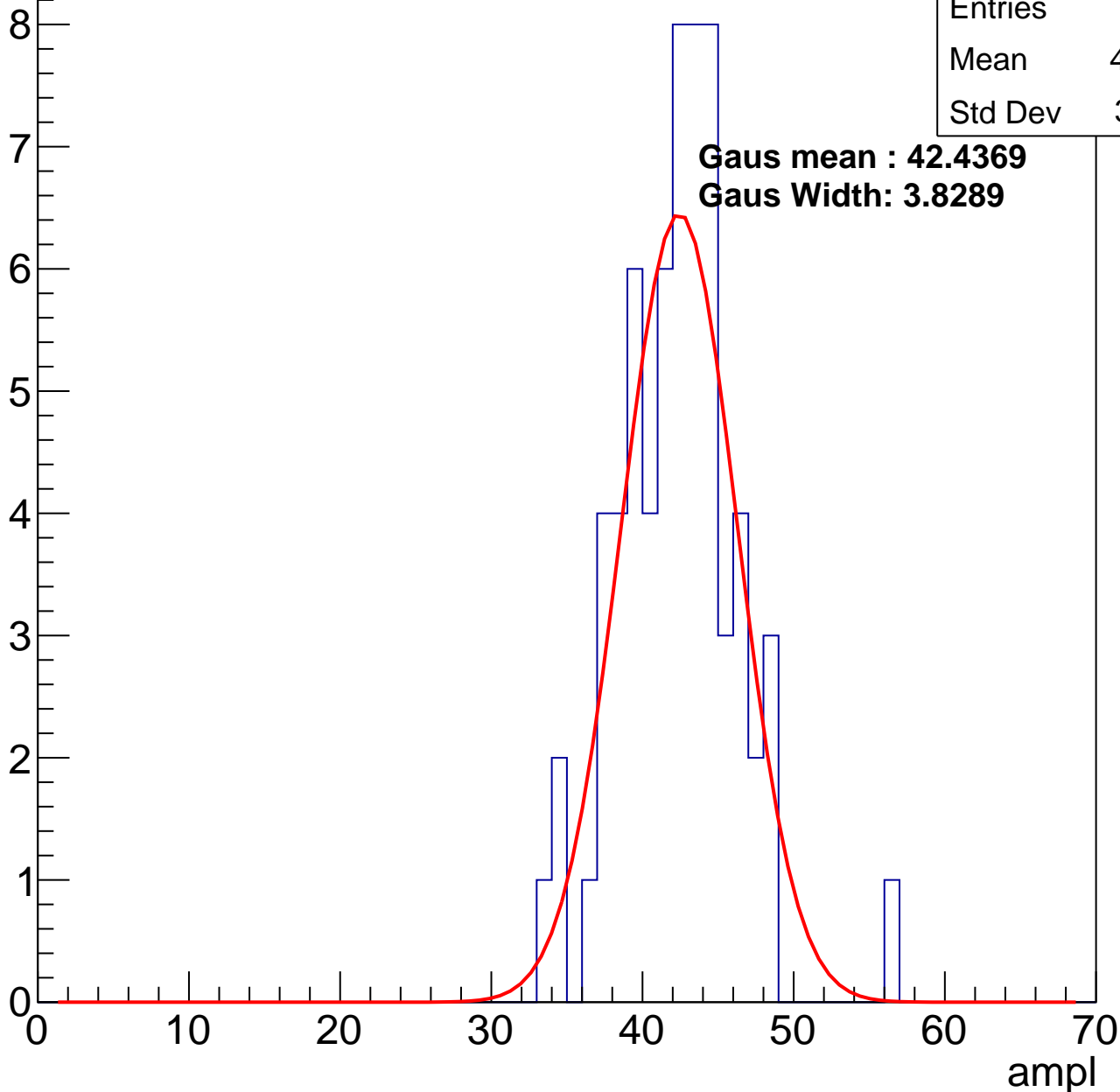
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 65    |
| Mean    | 41.88 |
| Std Dev | 3.861 |

**Gaus mean : 42.4369**

**Gaus Width: 3.8289**

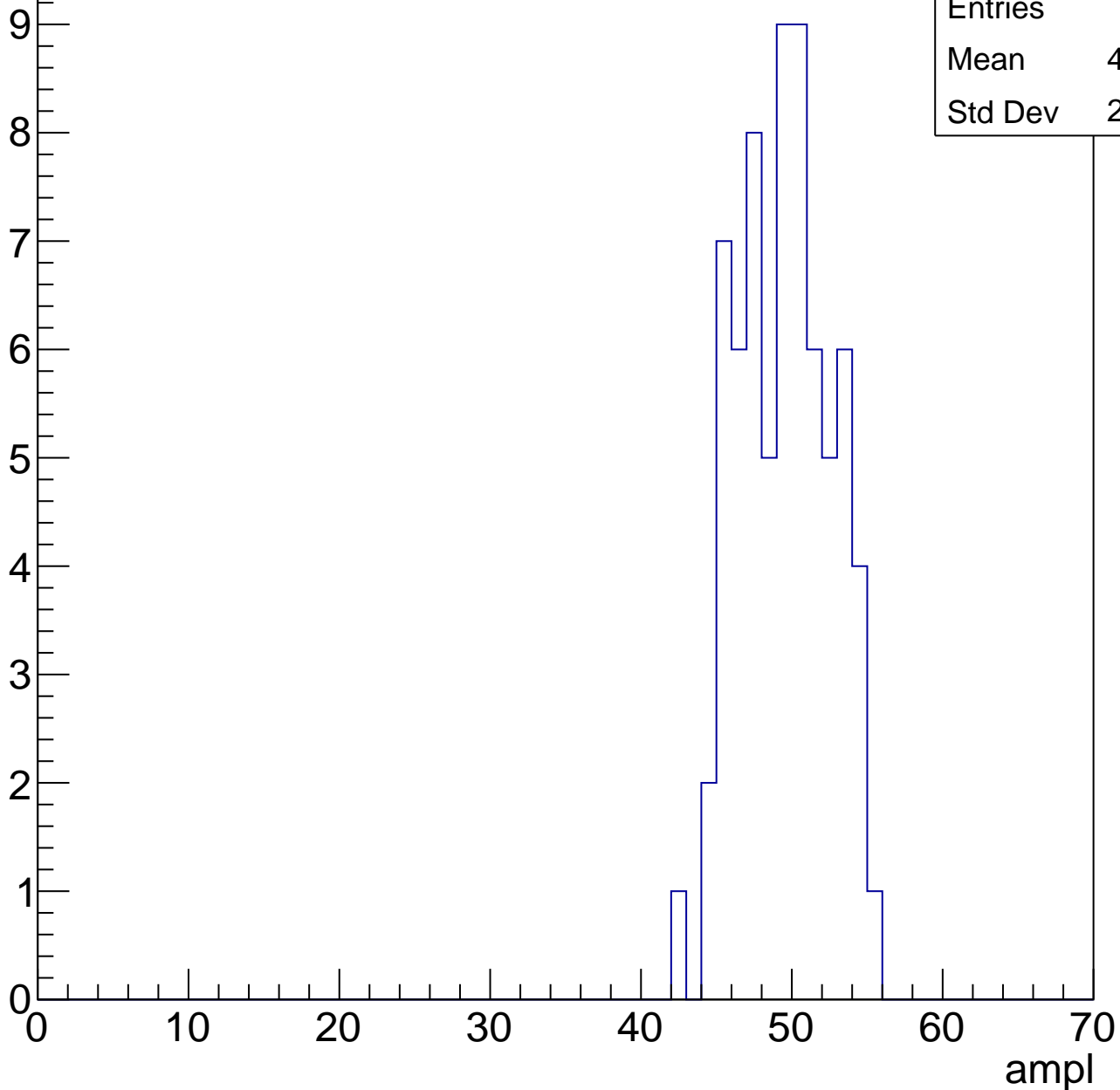


# B0L001S, U2-ch44, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

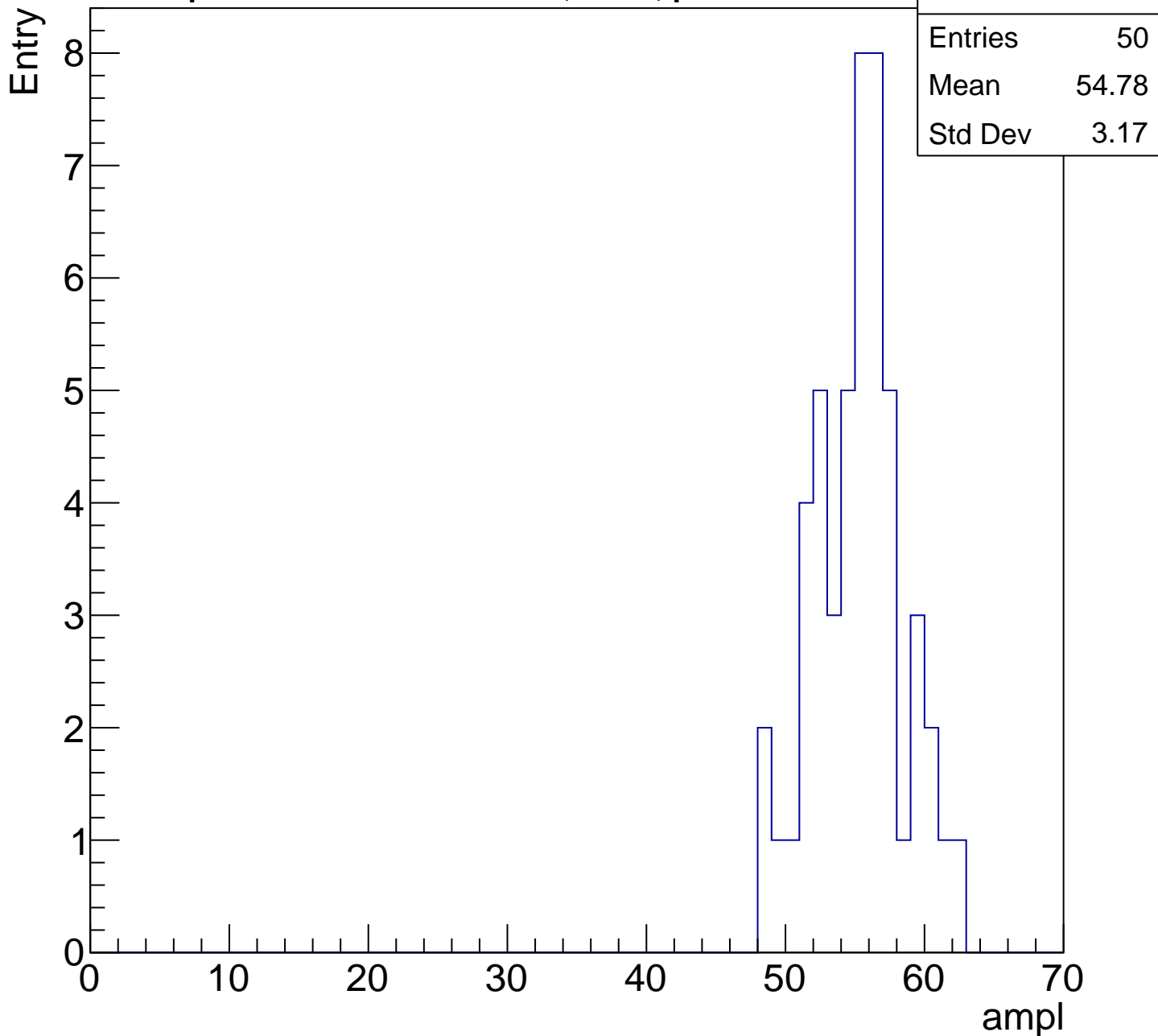
Entry

|         |       |
|---------|-------|
| Entries | 69    |
| Mean    | 49.03 |
| Std Dev | 2.978 |



# B0L001S, U2-ch44, adc4

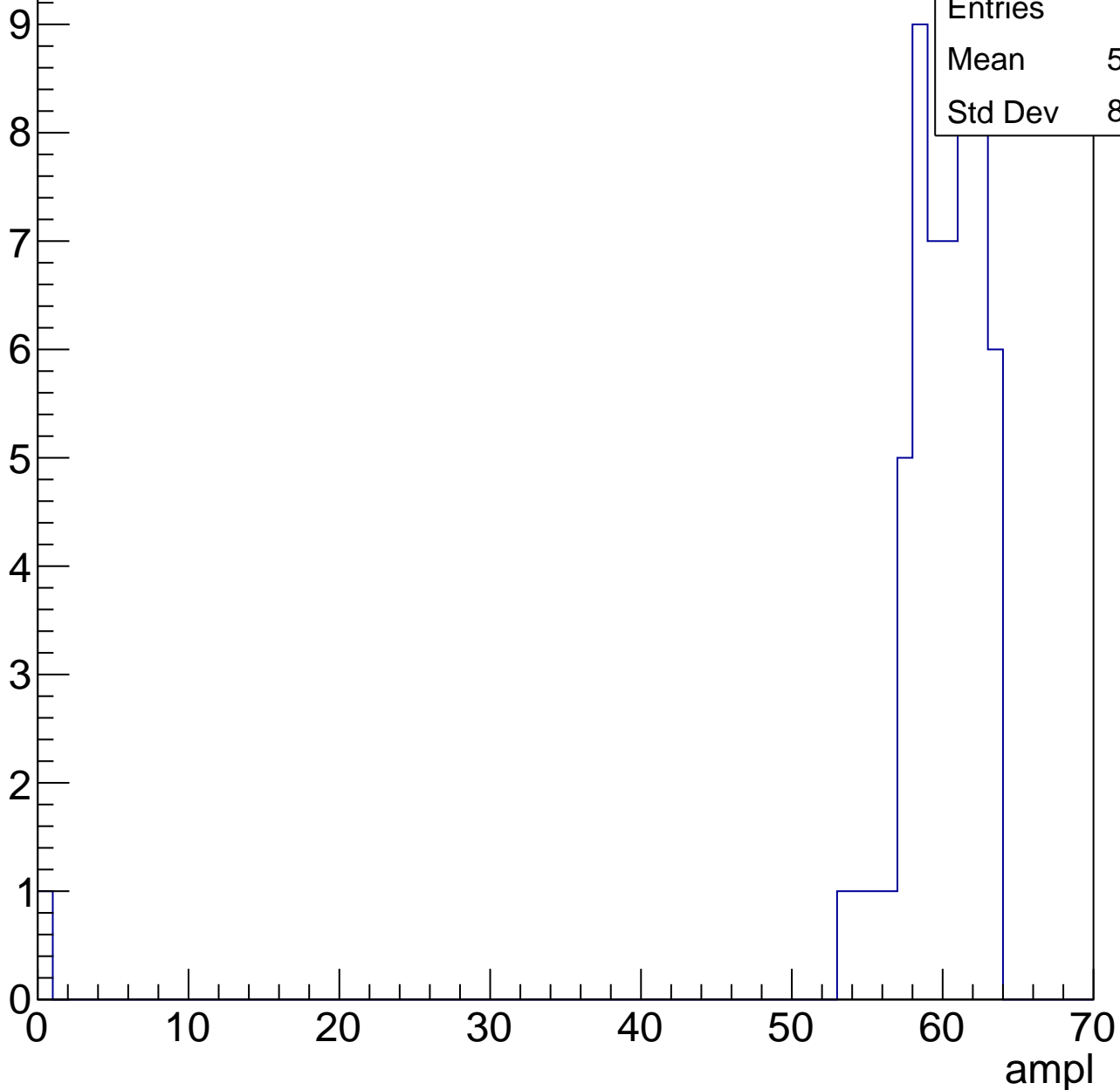
calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U2-ch44, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U2-ch44, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch44, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 4 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch45, adc0

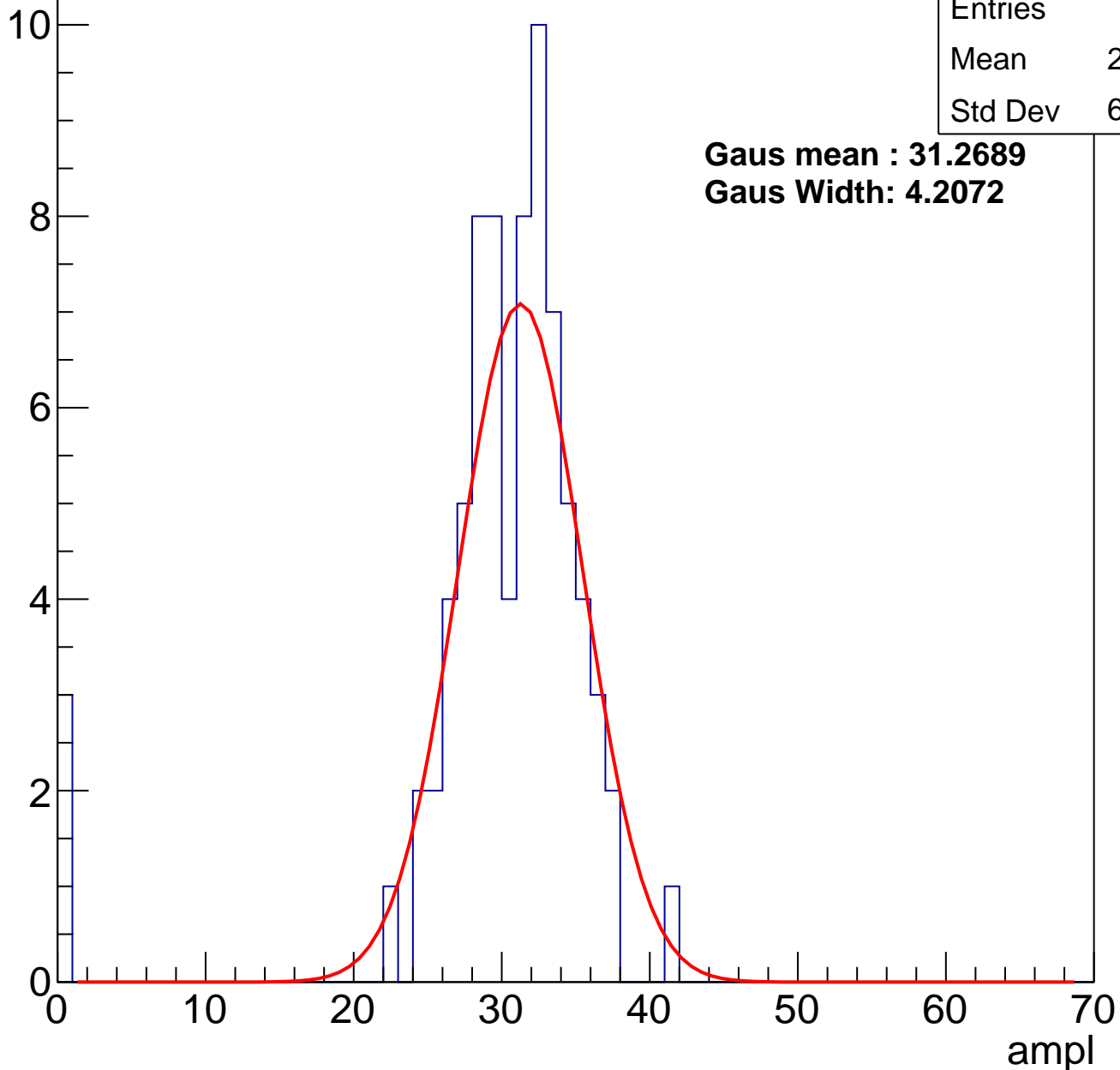
calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 77    |
| Mean    | 29.44 |
| Std Dev | 6.865 |

**Gaus mean : 31.2689**

**Gaus Width: 4.2072**

Entry



# B0L001S, U2-ch45, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 61    |
| Mean    | 37.54 |
| Std Dev | 3.438 |

**Gaus mean : 37.6005**

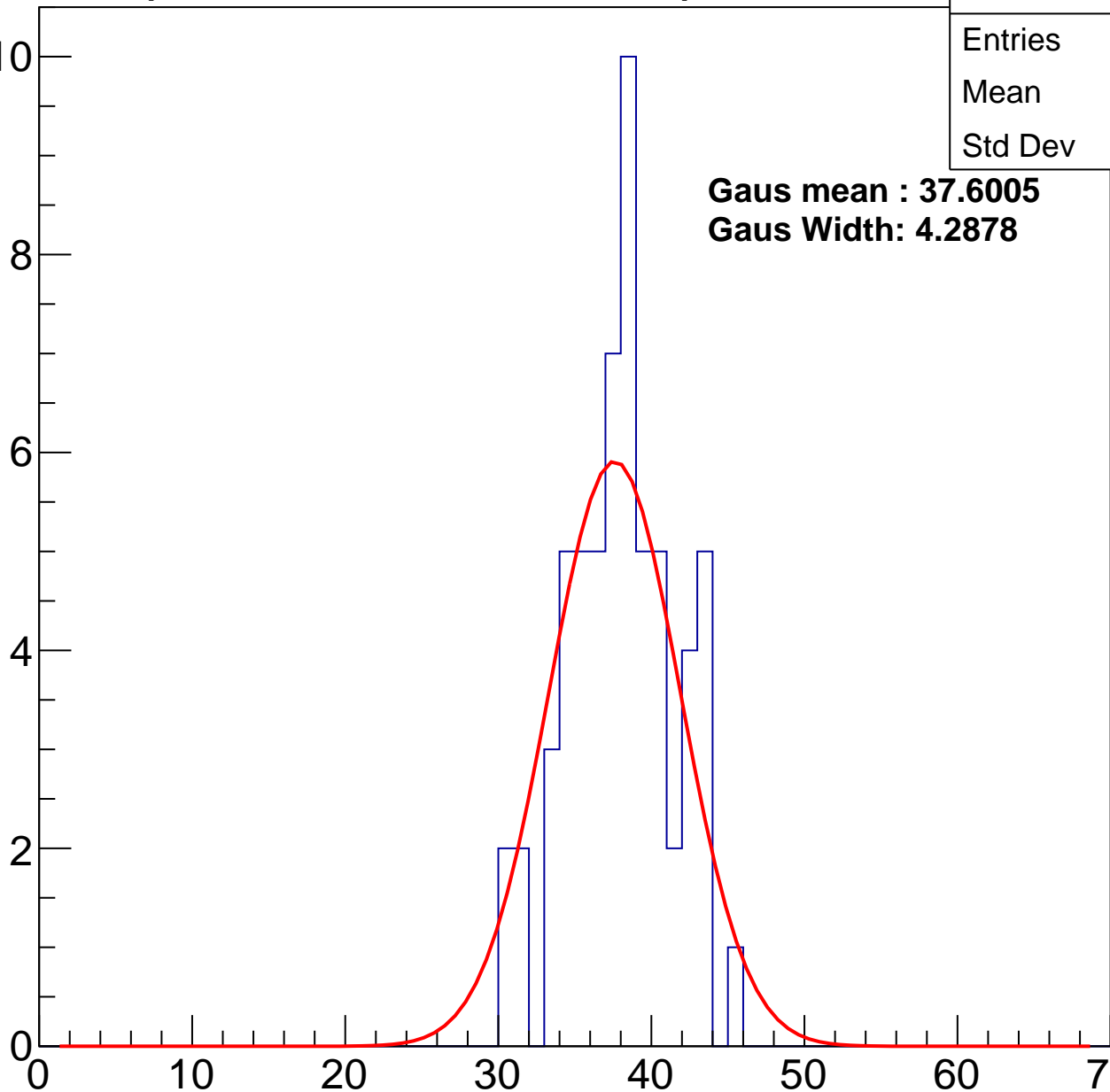
**Gaus Width: 4.2878**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B0L001S, U2-ch45, adc2

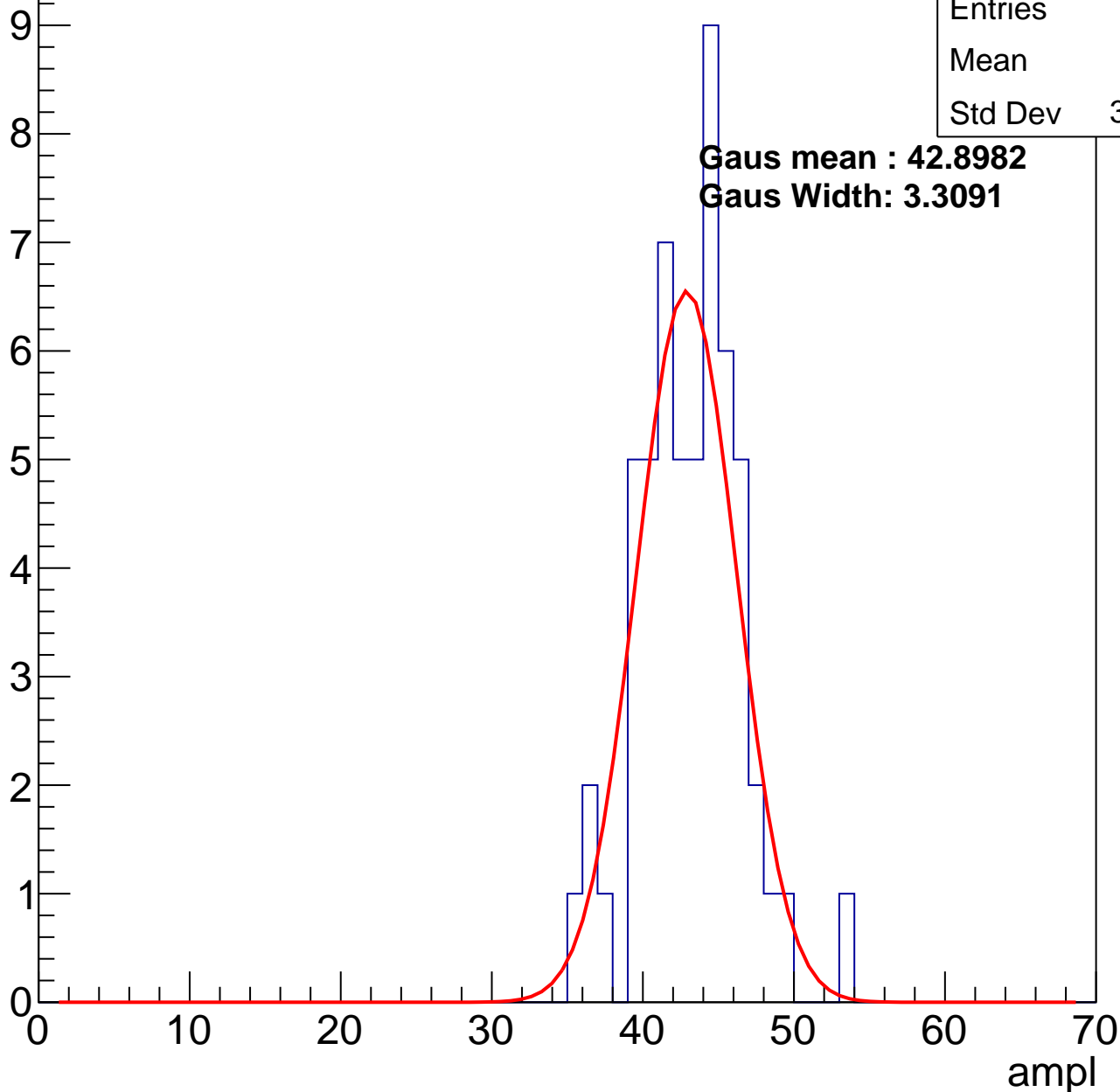
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 56    |
| Mean    | 42.7  |
| Std Dev | 3.332 |

**Gaus mean : 42.8982**

**Gaus Width: 3.3091**

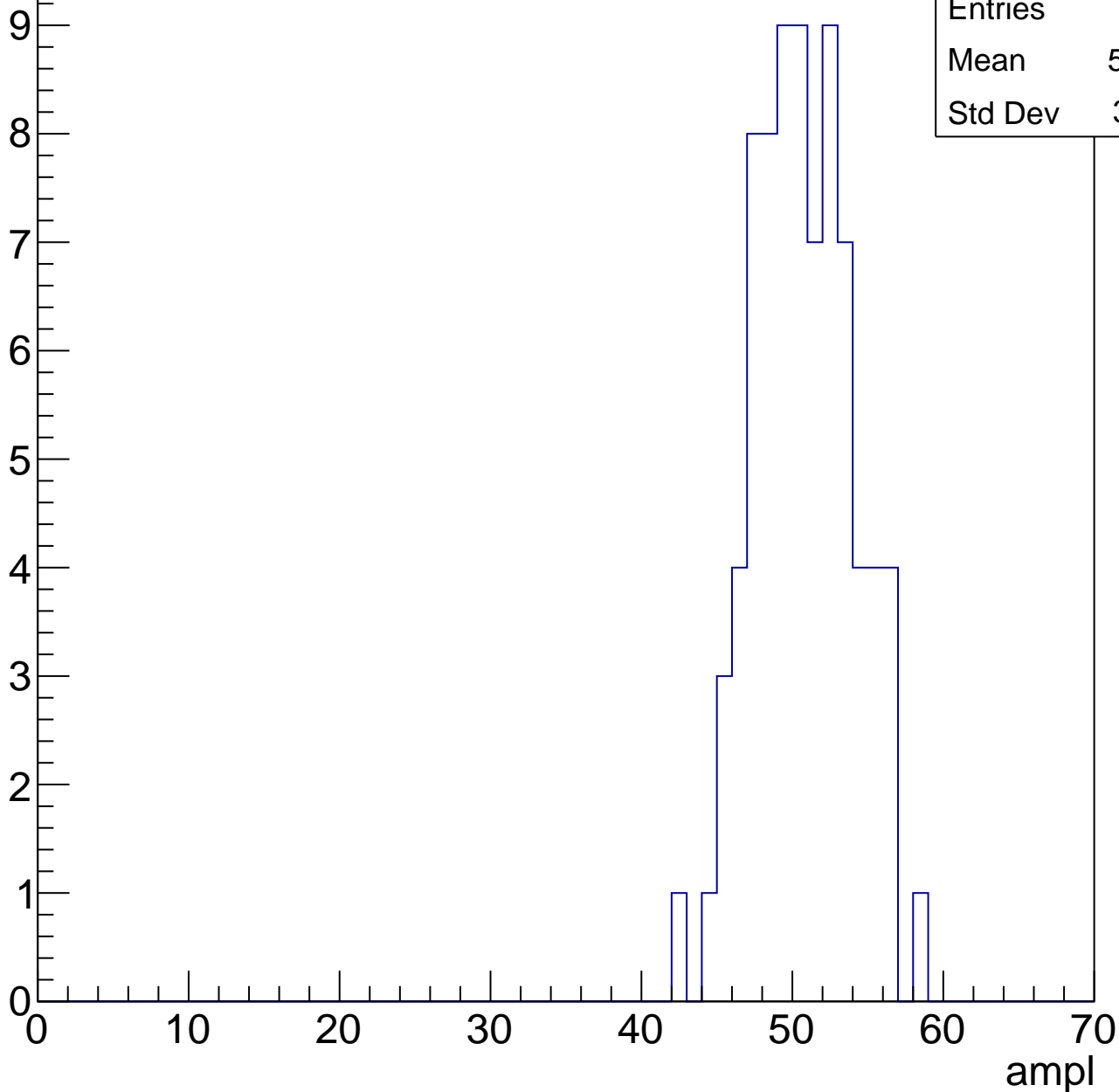


# B0L001S, U2-ch45, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 79    |
| Mean    | 50.25 |
| Std Dev | 3.231 |

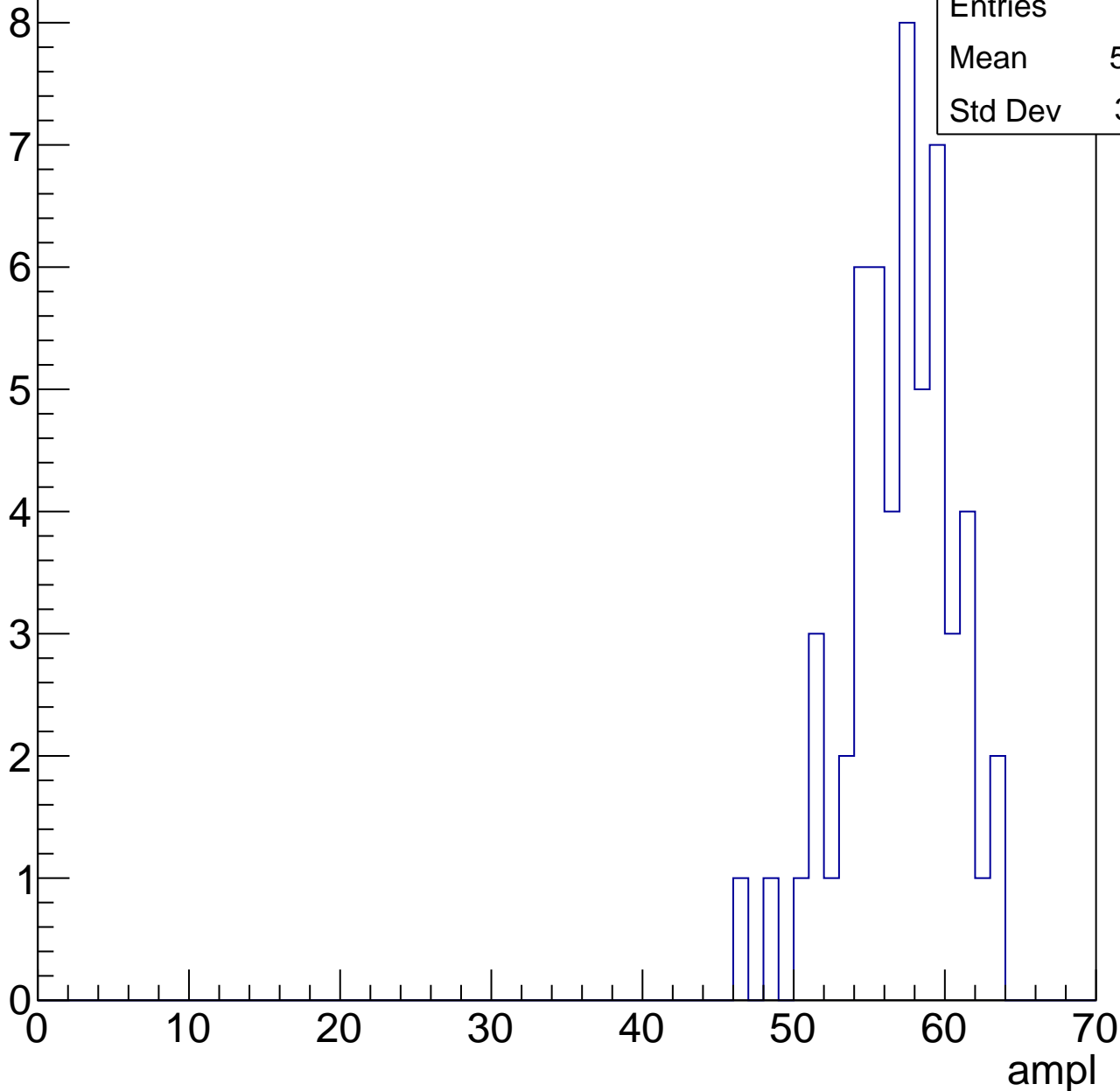


# B0L001S, U2-ch45, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 55    |
| Mean    | 56.44 |
| Std Dev | 3.571 |

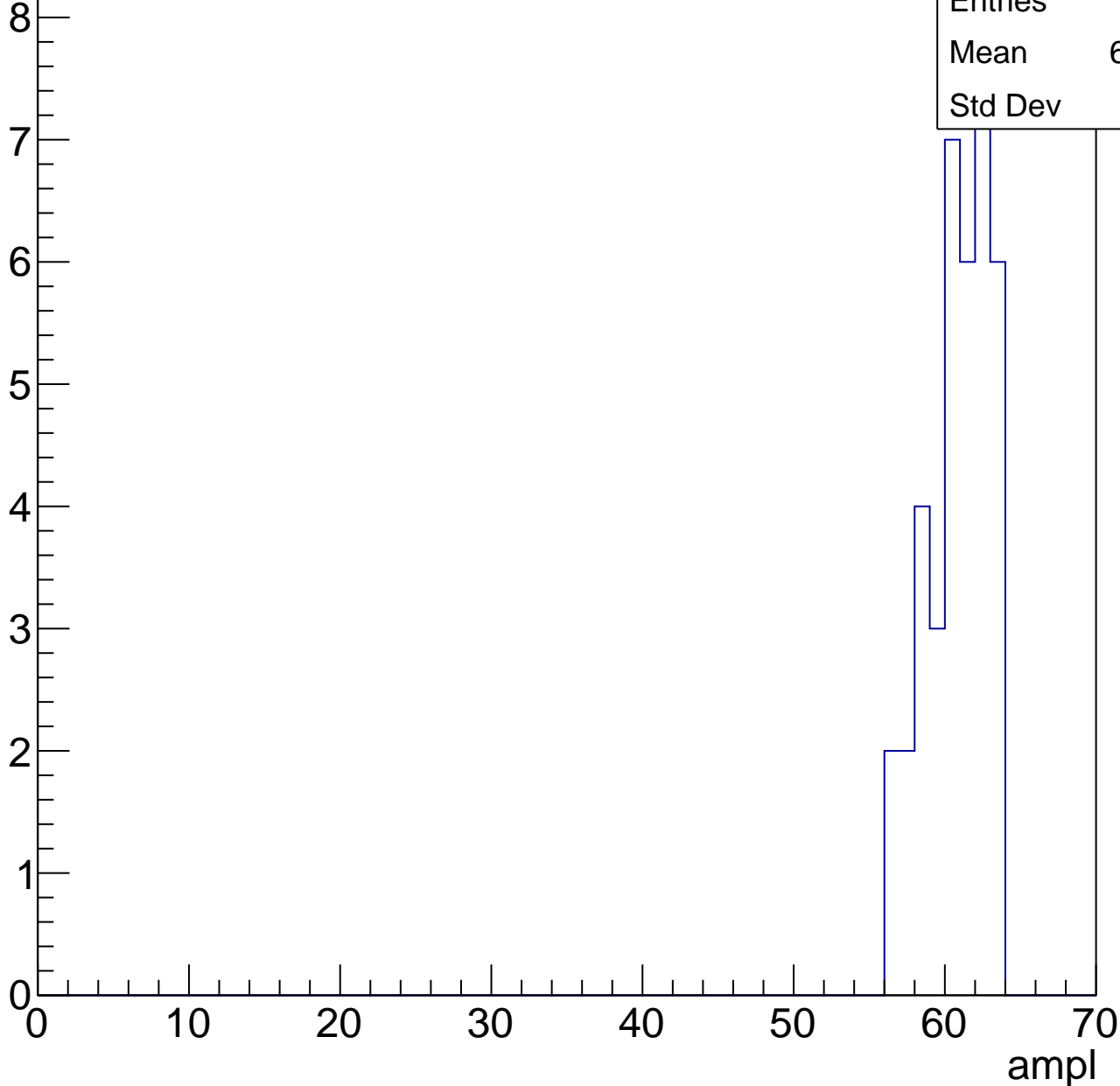


# B0L001S, U2-ch45, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

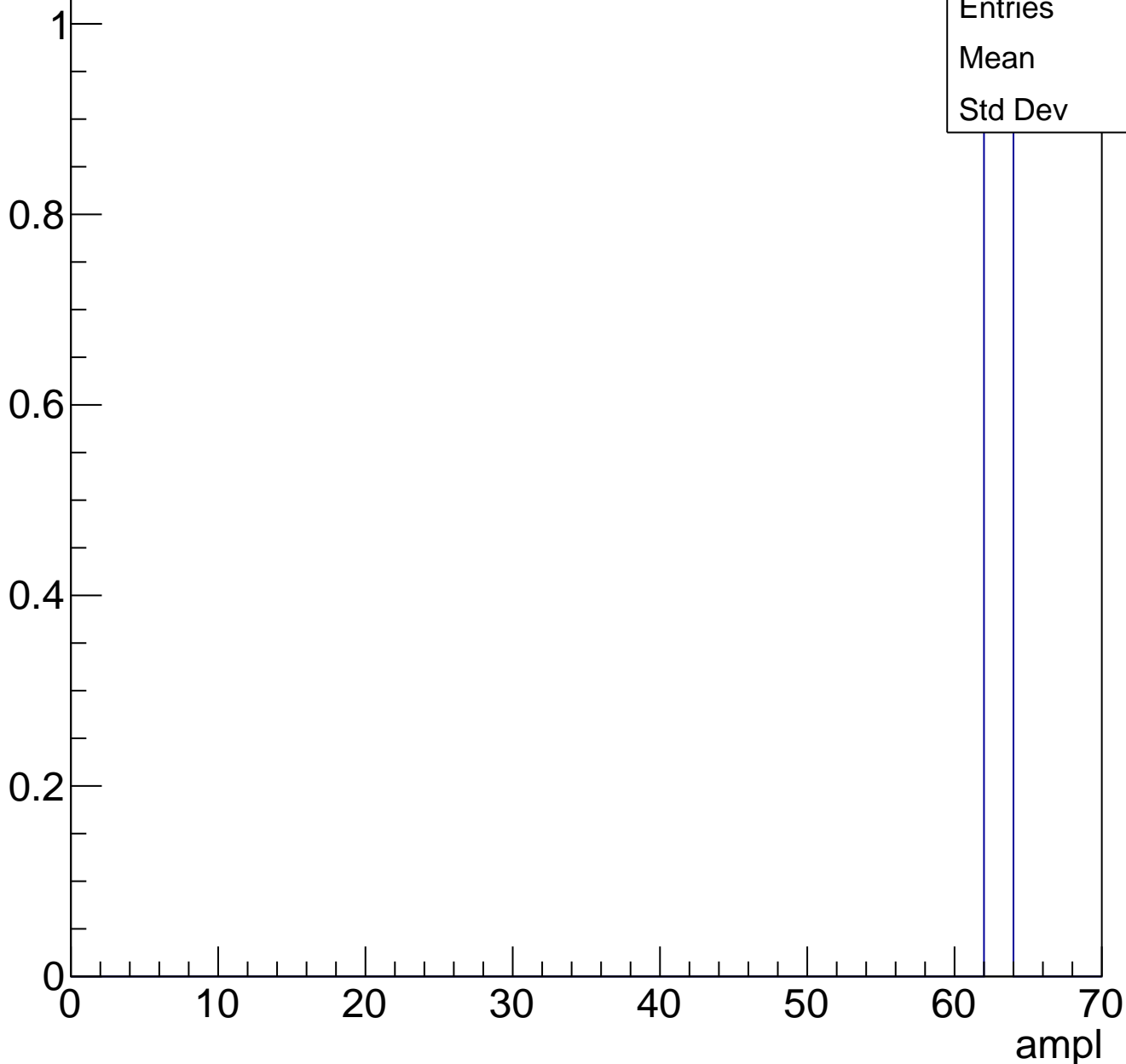
|         |       |
|---------|-------|
| Entries | 38    |
| Mean    | 60.39 |
| Std Dev | 2.02  |



# B0L001S, U2-ch45, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

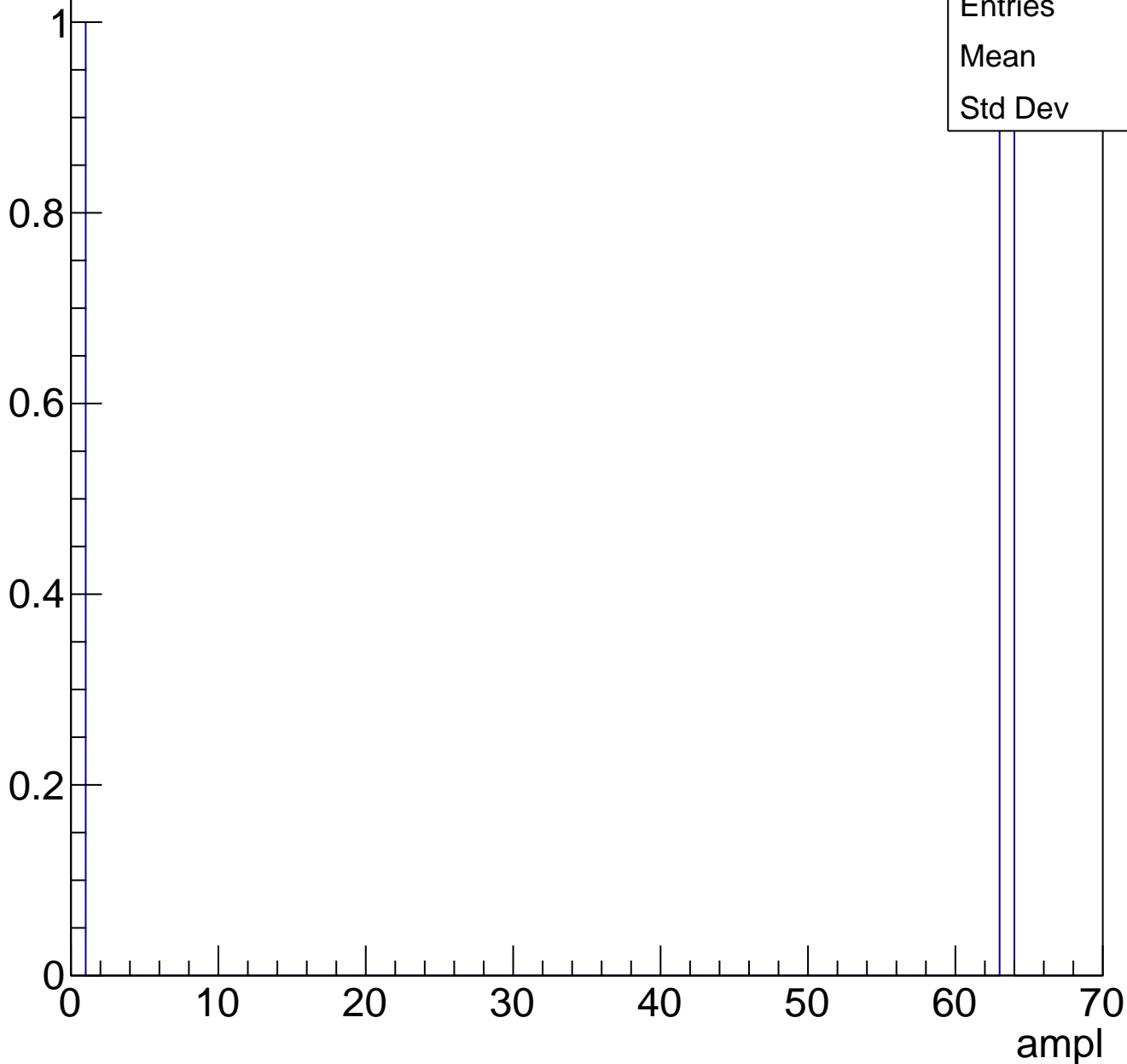




# B0L001S, U2-ch45, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U2-ch46, adc0

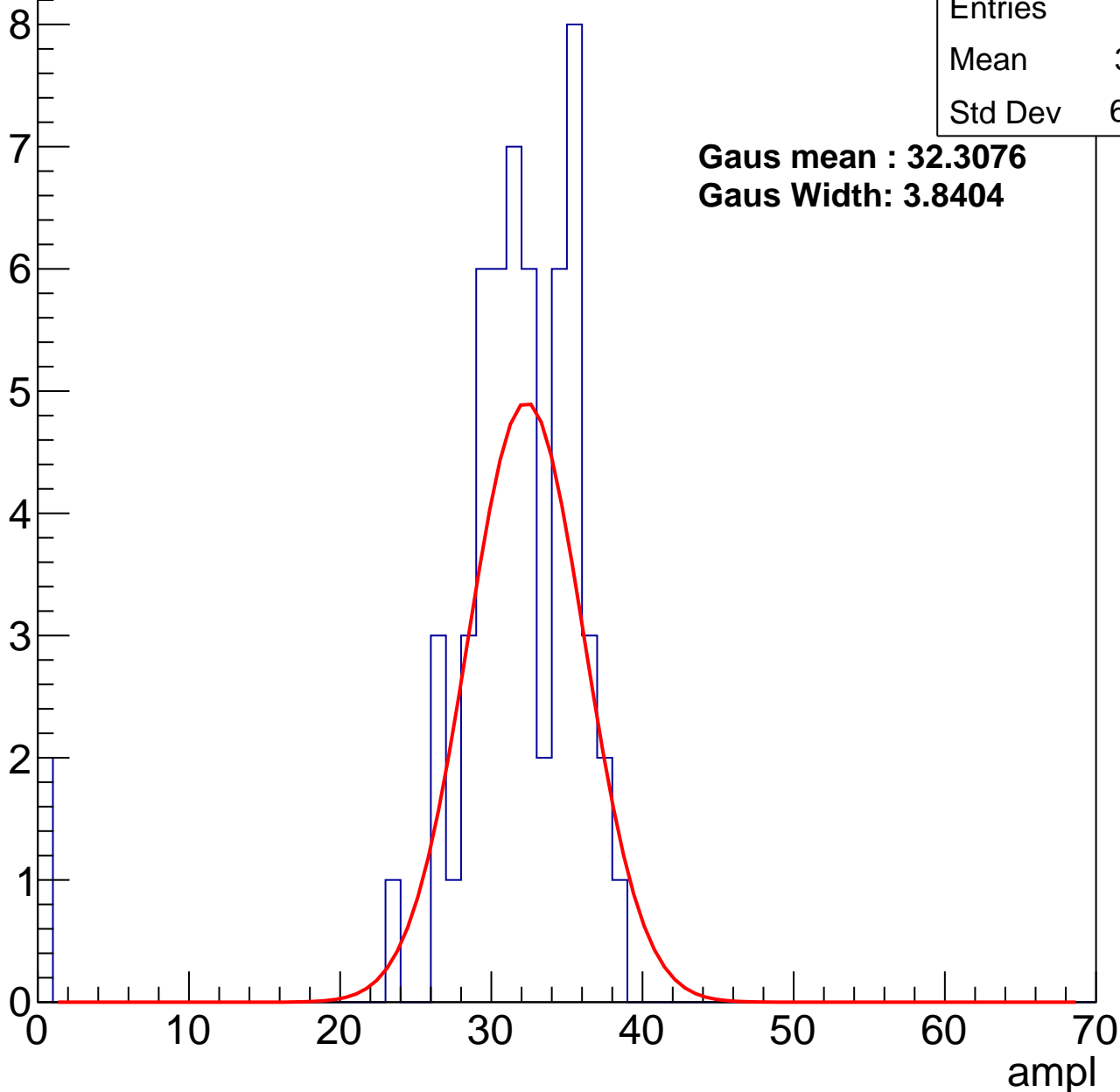
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 57    |
| Mean    | 30.61 |
| Std Dev | 6.646 |

**Gaus mean : 32.3076**

**Gaus Width: 3.8404**



# B0L001S, U2-ch46, adc1

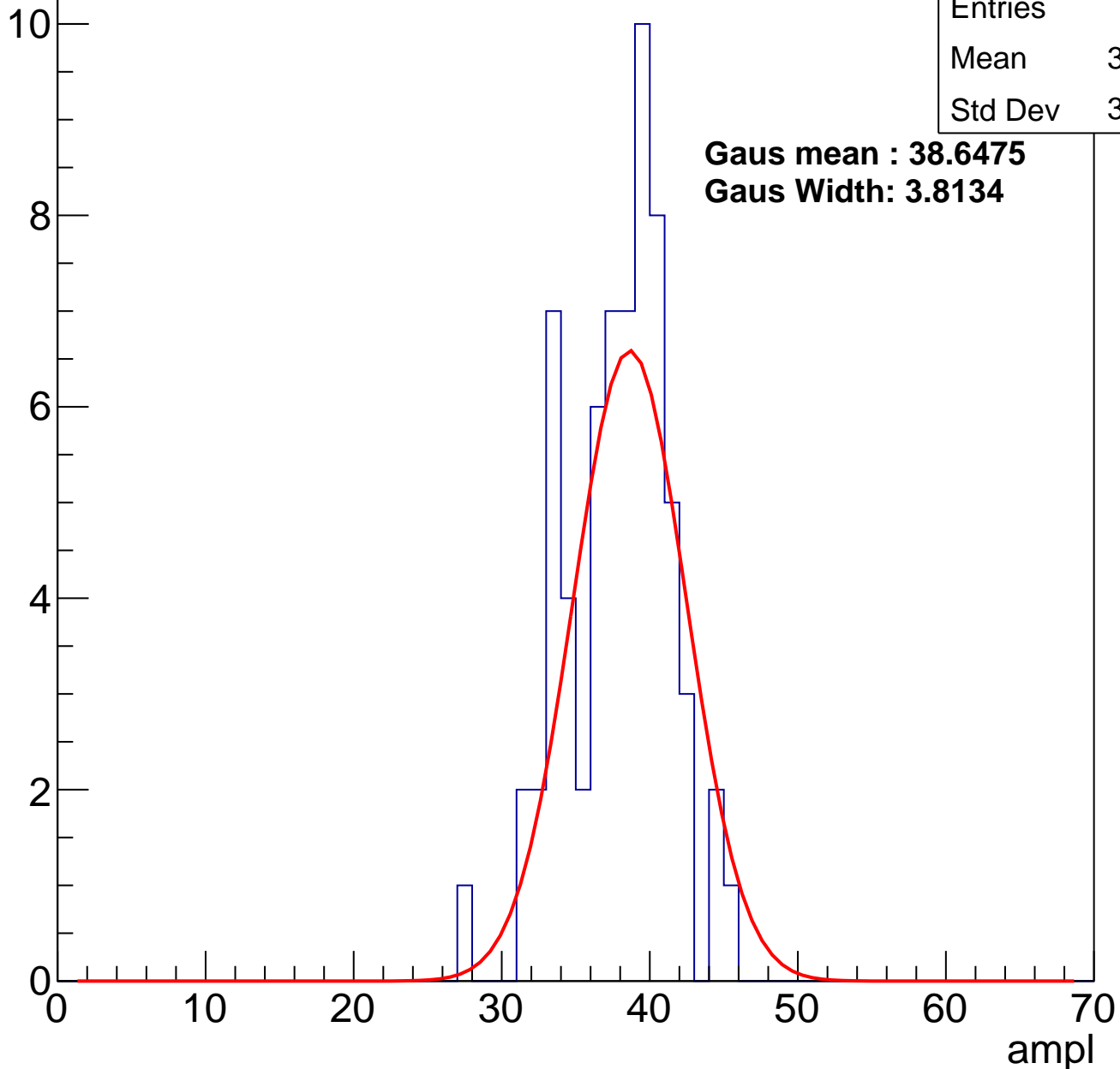
calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 67    |
| Mean    | 37.39 |
| Std Dev | 3.477 |

**Gaus mean : 38.6475**

**Gaus Width: 3.8134**

Entry



# B0L001S, U2-ch46, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 58    |
| Mean    | 43.93 |
| Std Dev | 2.993 |

**Gaus mean : 44.8006**

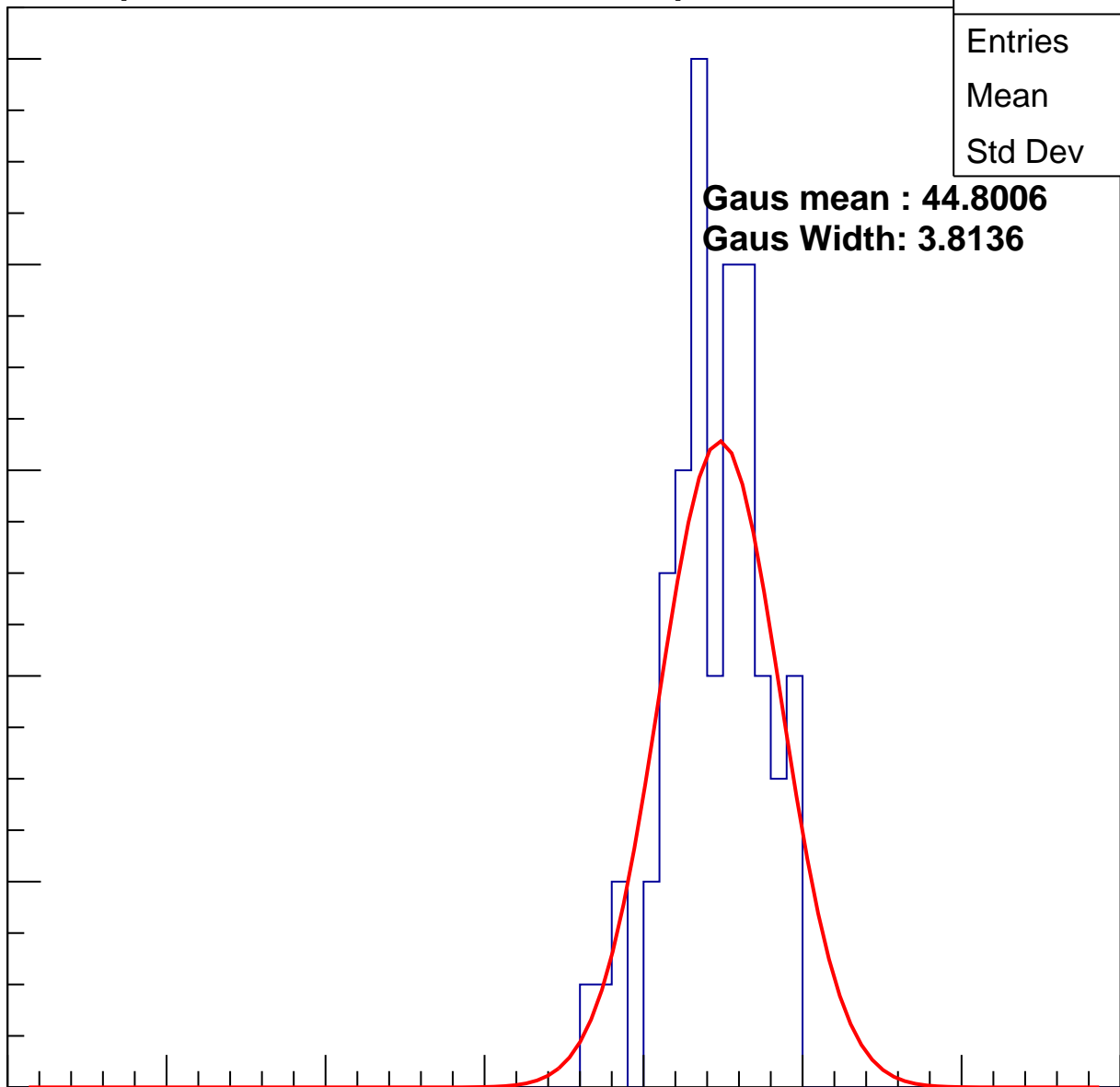
**Gaus Width: 3.8136**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

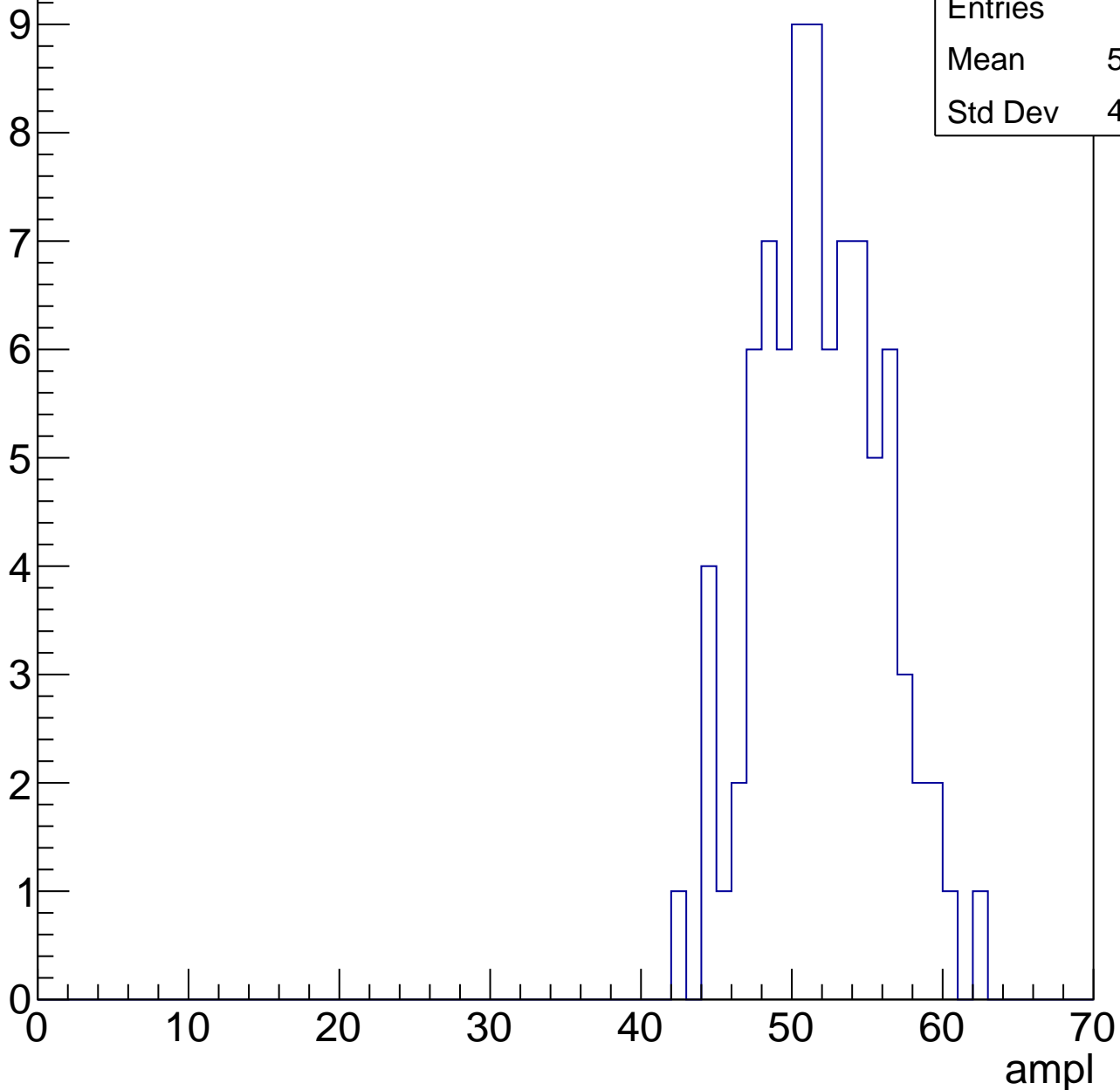


# B0L001S, U2-ch46, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 85    |
| Mean    | 51.47 |
| Std Dev | 4.057 |

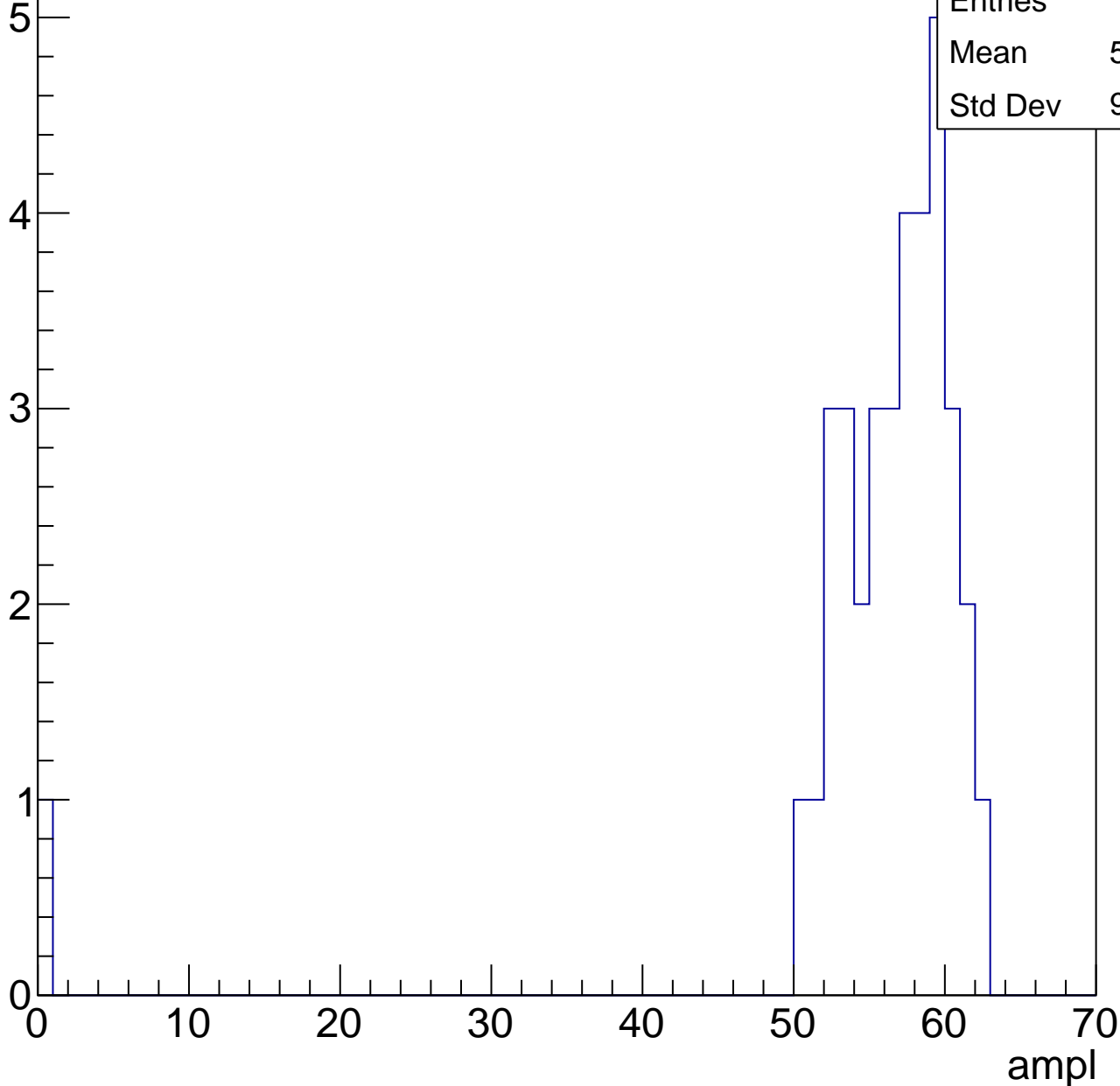


# B0L001S, U2-ch46, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 36    |
| Mean    | 54.89 |
| Std Dev | 9.772 |

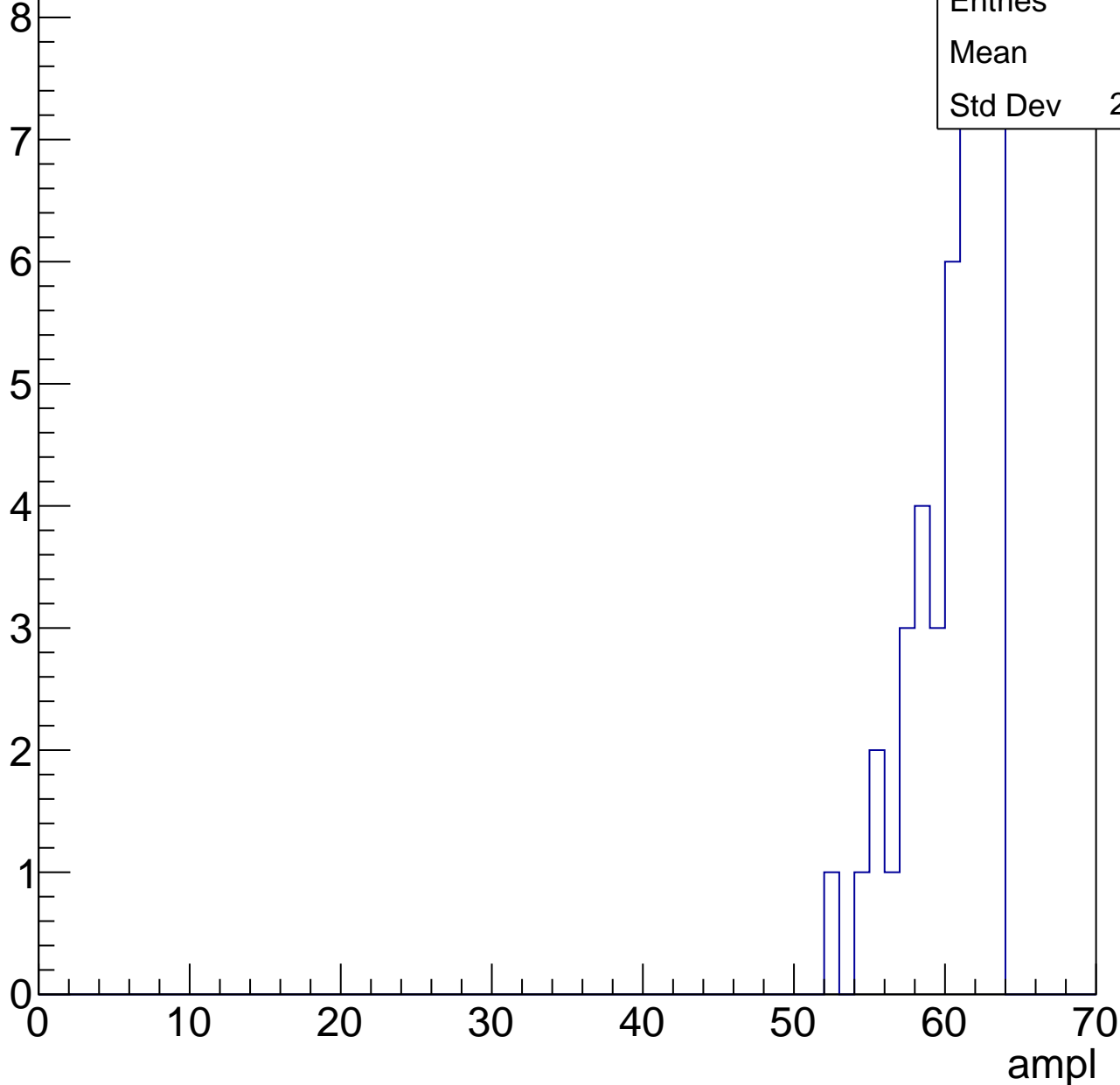


# B0L001S, U2-ch46, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 45    |
| Mean    | 60    |
| Std Dev | 2.683 |



# B0L001S, U2-ch46, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

|         |    |
|---------|----|
| Entries | 2  |
| Mean    | 63 |
| Std Dev | 0  |

0 10 20 30 40 50 60 70

ampl



# B0L001S, U2-ch46, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 0 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch47, adc0

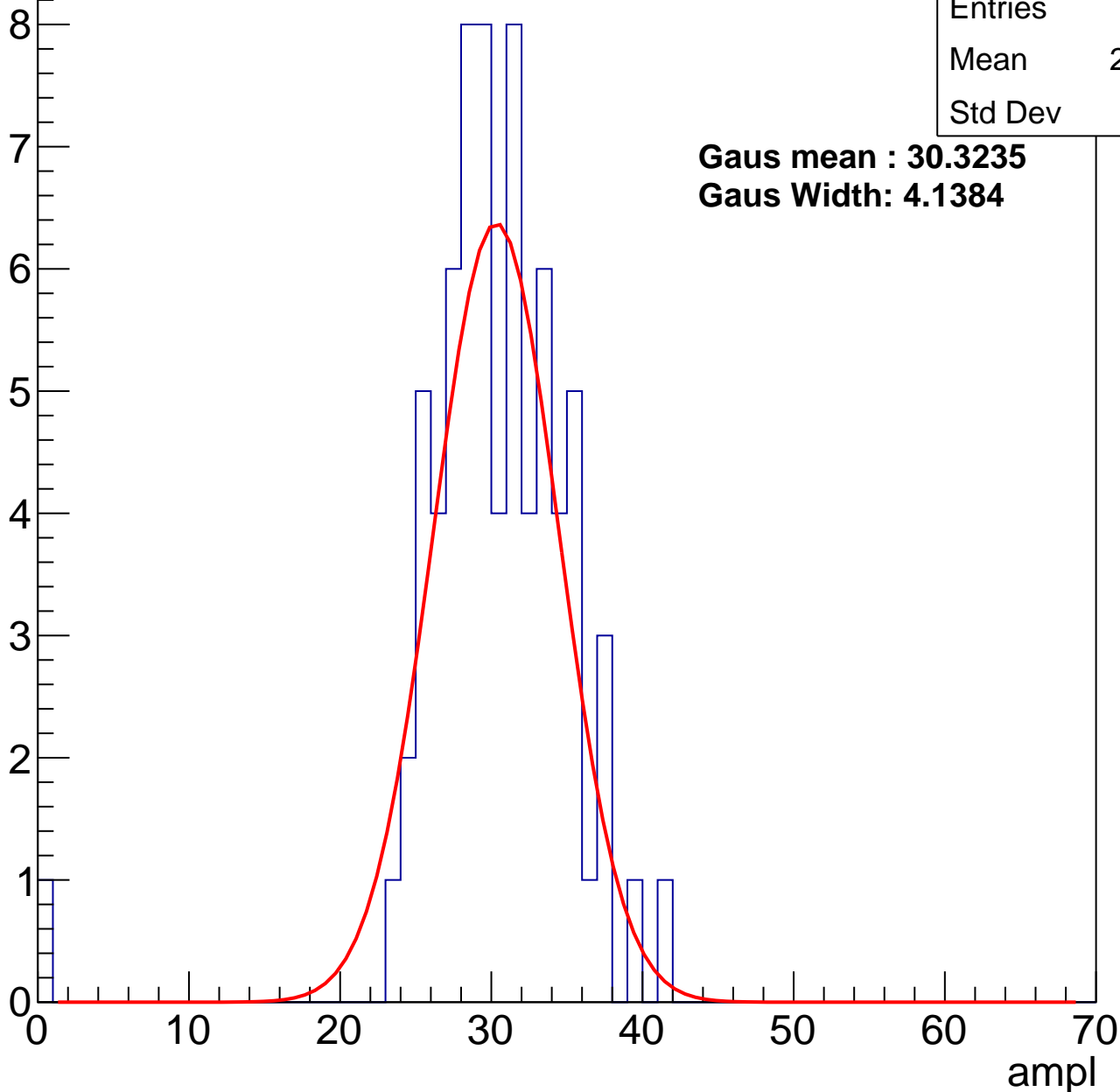
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 72    |
| Mean    | 29.86 |
| Std Dev | 5.21  |

**Gaus mean : 30.3235**

**Gaus Width: 4.1384**



# B0L001S, U2-ch47, adc1

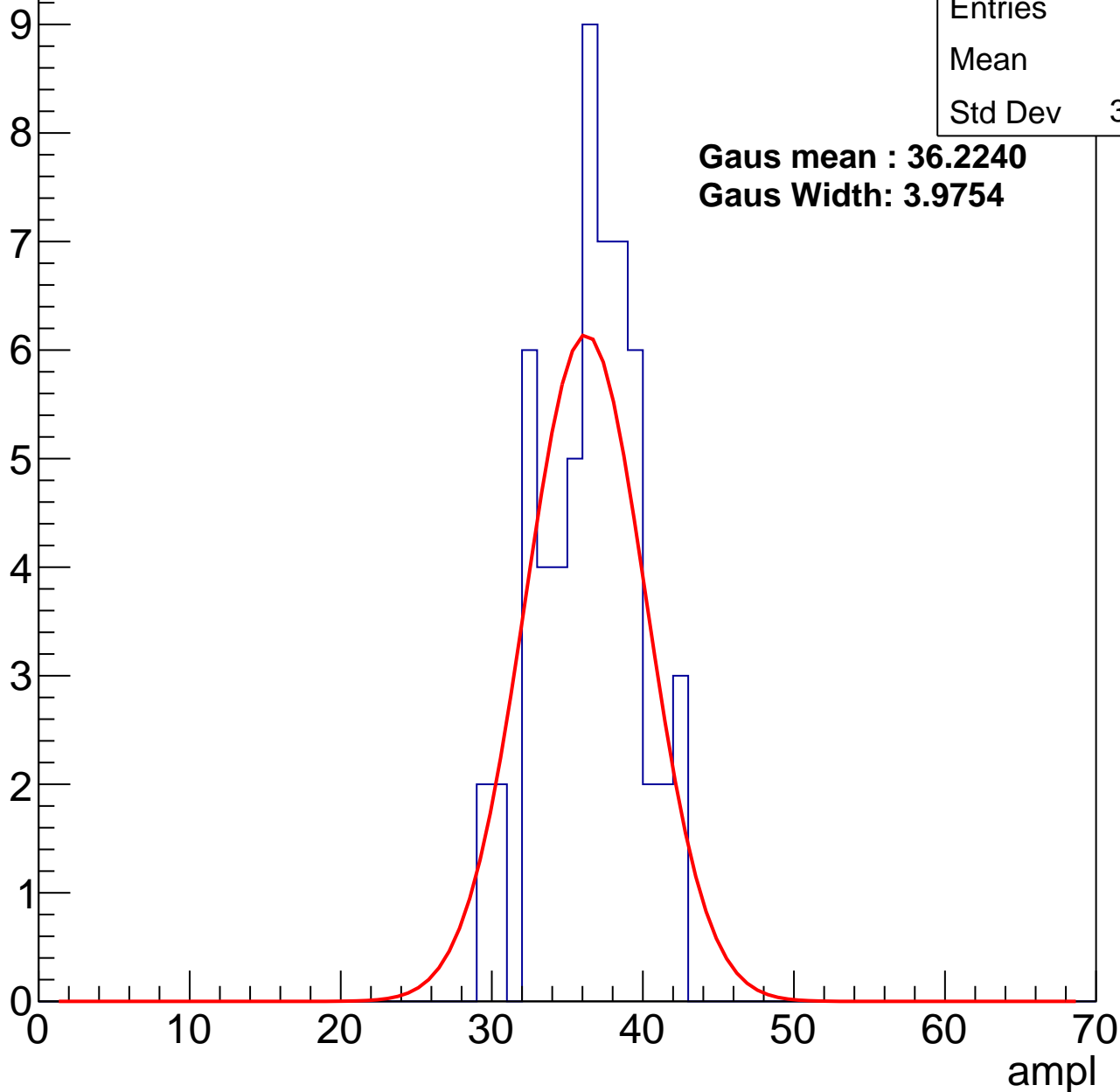
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 59    |
| Mean    | 36    |
| Std Dev | 3.194 |

**Gaus mean : 36.2240**

**Gaus Width: 3.9754**



# B0L001S, U2-ch47, adc2

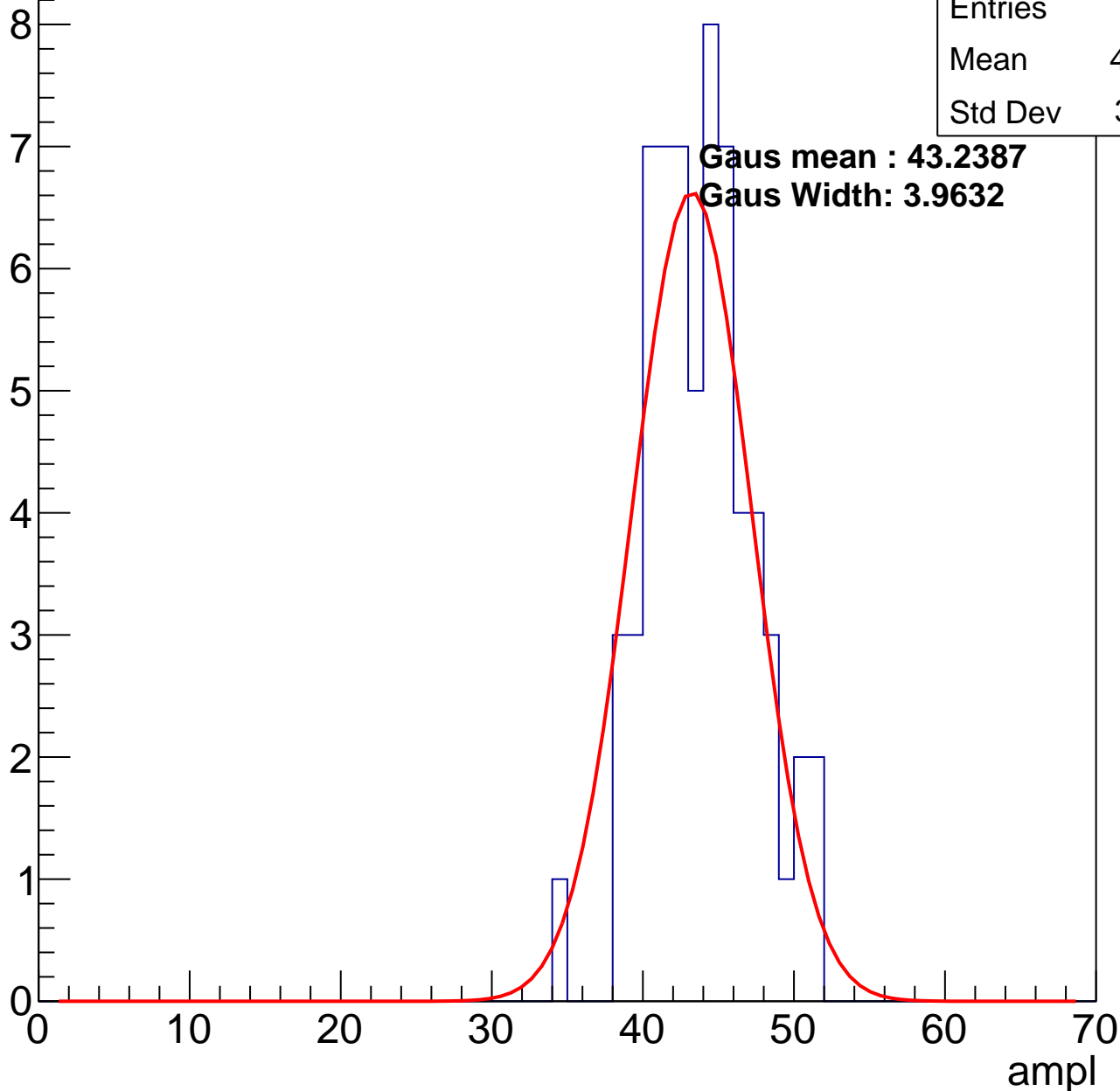
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 64    |
| Mean    | 43.36 |
| Std Dev | 3.461 |

**Gaus mean : 43.2387**

**Gaus Width: 3.9632**

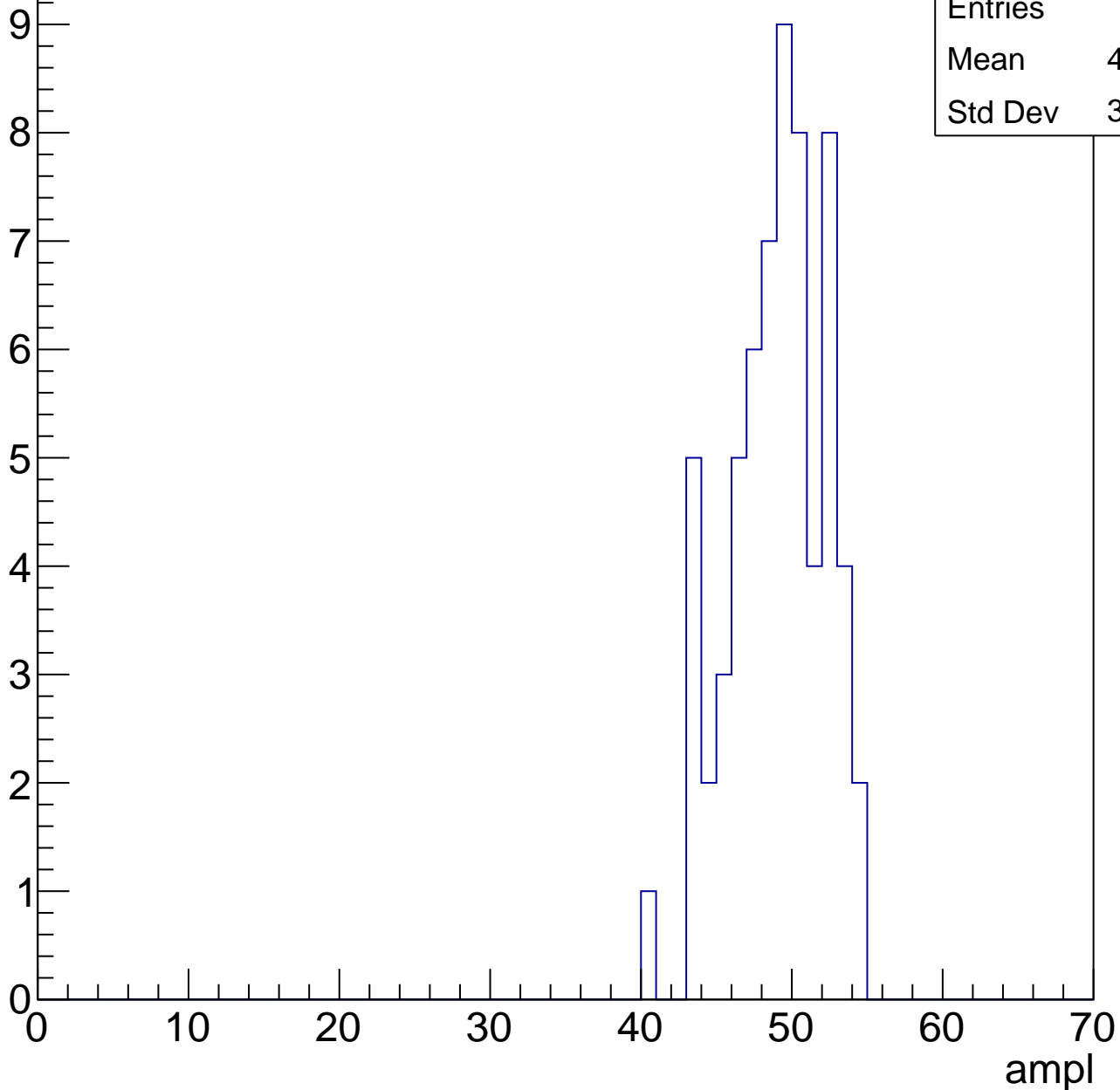


# B0L001S, U2-ch47, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

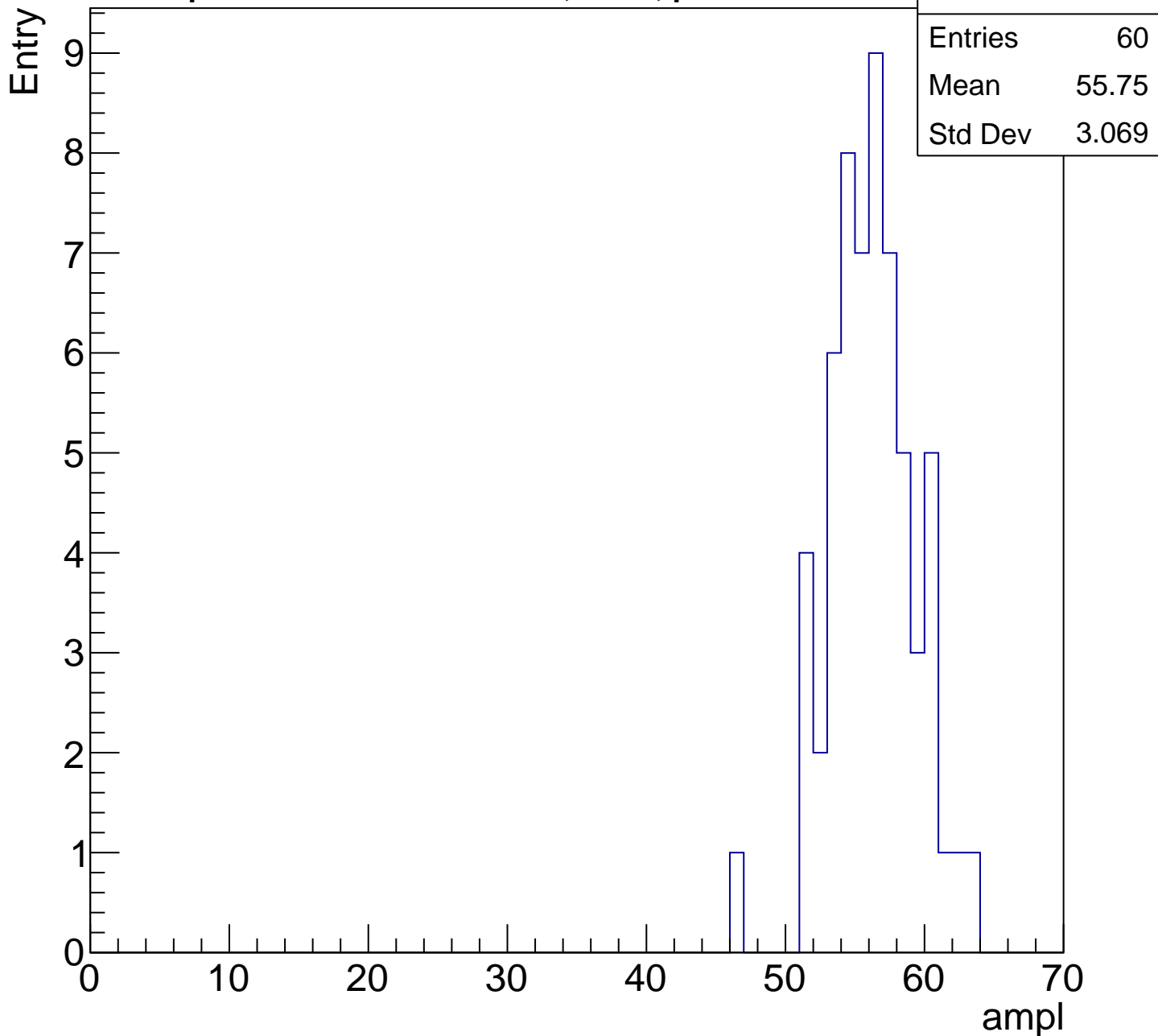
Entry

|         |       |
|---------|-------|
| Entries | 64    |
| Mean    | 48.55 |
| Std Dev | 3.142 |



# B0L001S, U2-ch47, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

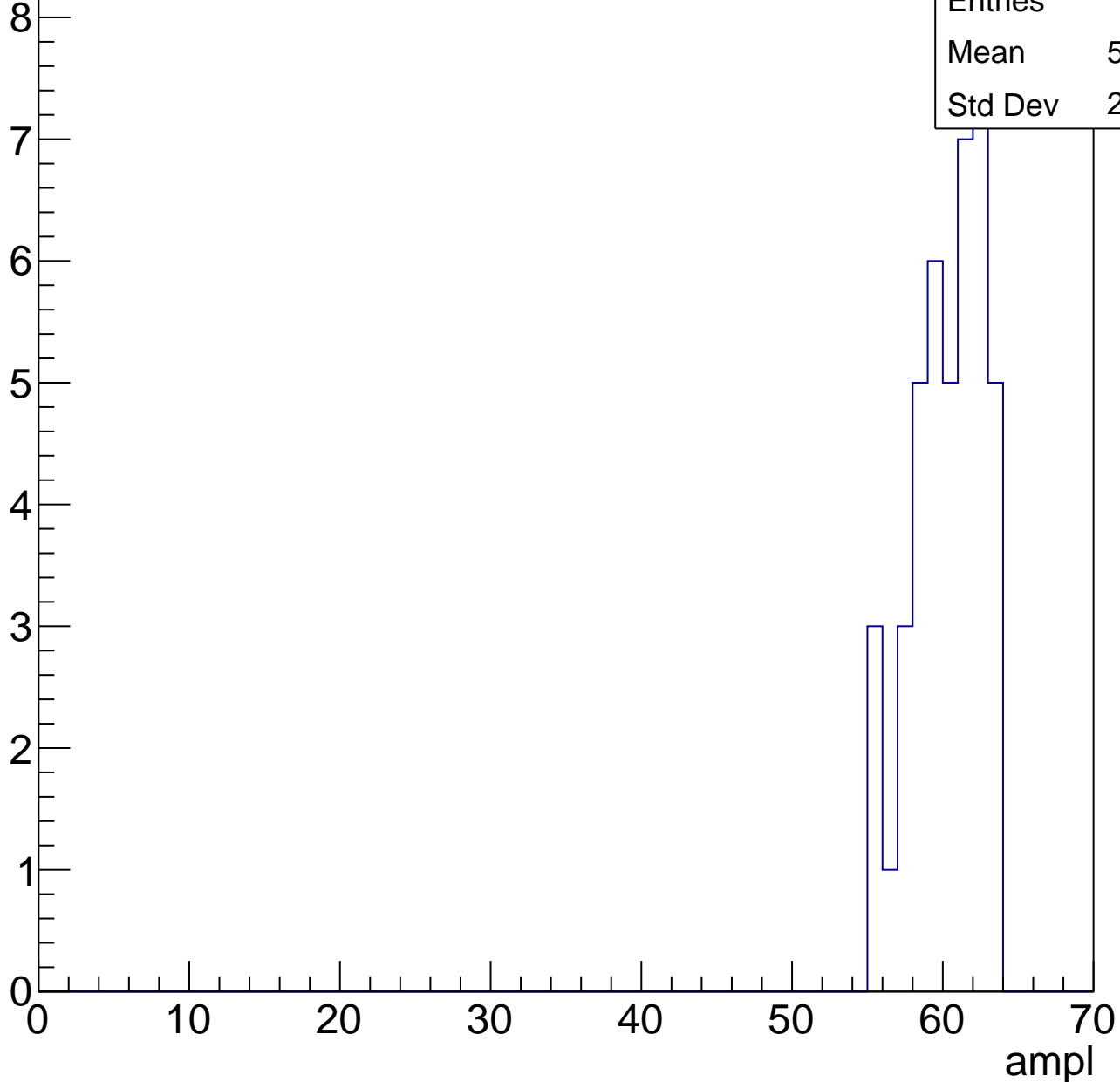


# B0L001S, U2-ch47, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

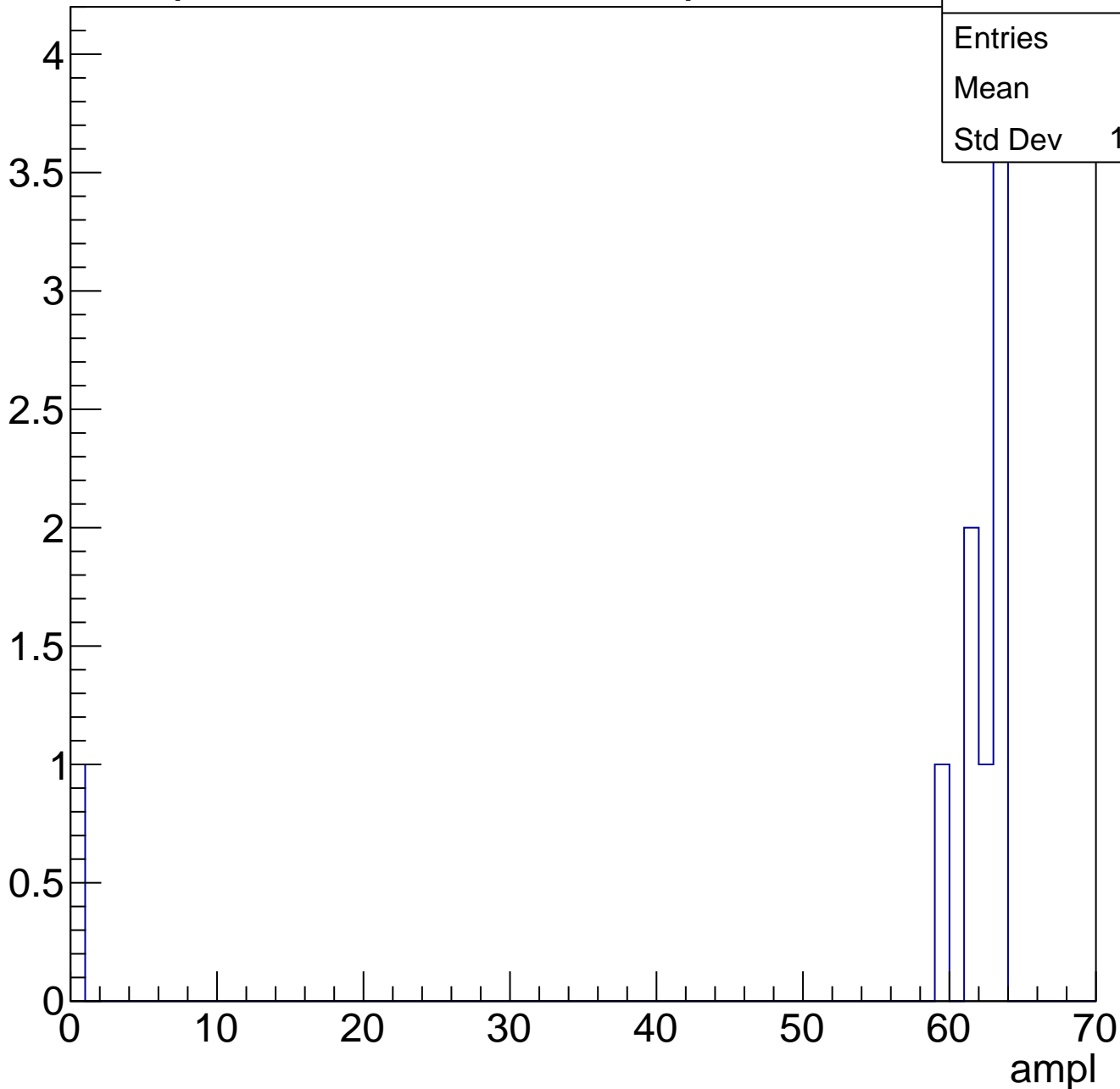
|         |       |
|---------|-------|
| Entries | 43    |
| Mean    | 59.86 |
| Std Dev | 2.298 |



# B0L001S, U2-ch47, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch47, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 0 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch48, adc0

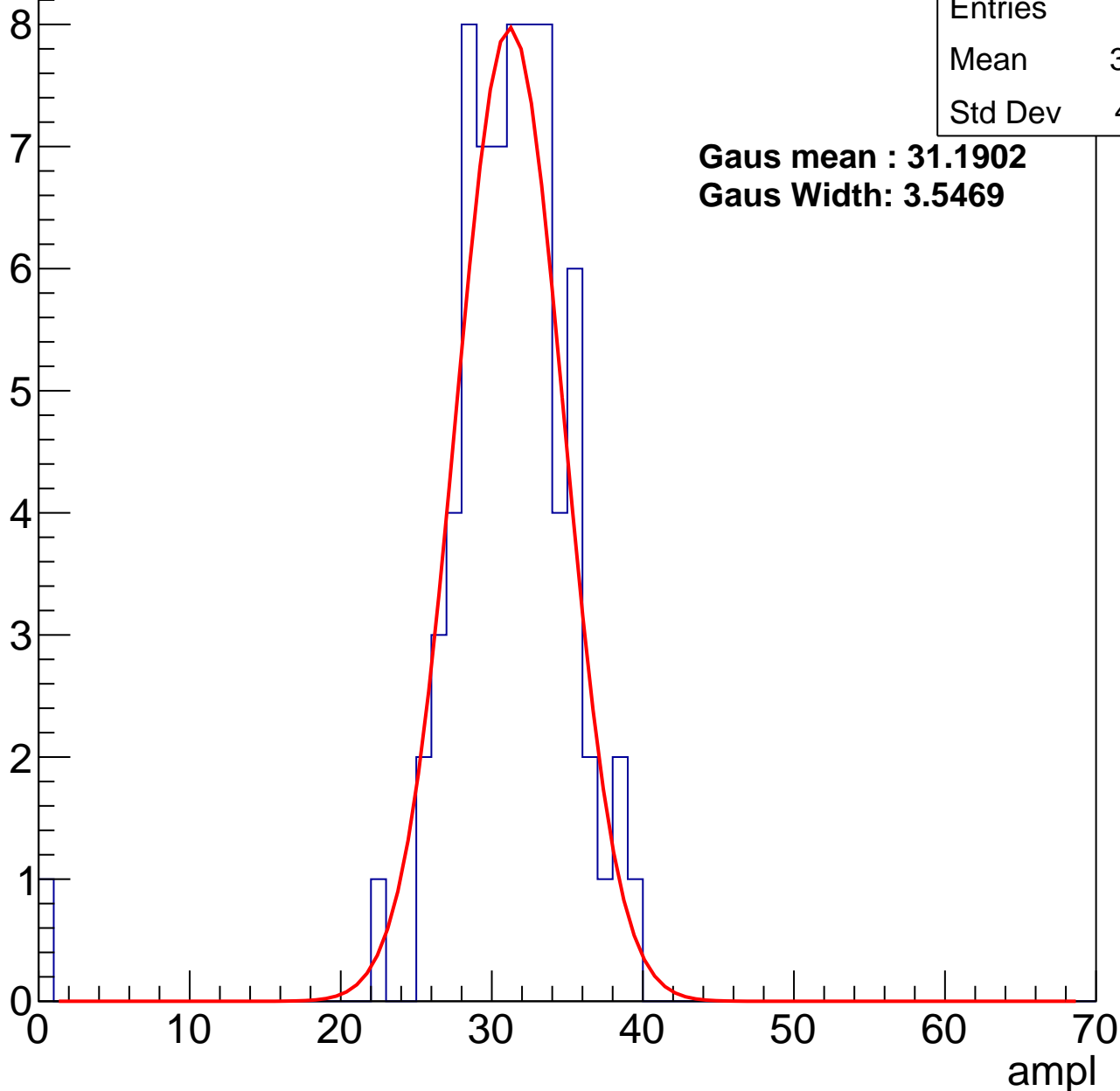
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 73    |
| Mean    | 30.59 |
| Std Dev | 4.921 |

**Gaus mean : 31.1902**

**Gaus Width: 3.5469**



# B0L001S, U2-ch48, adc1

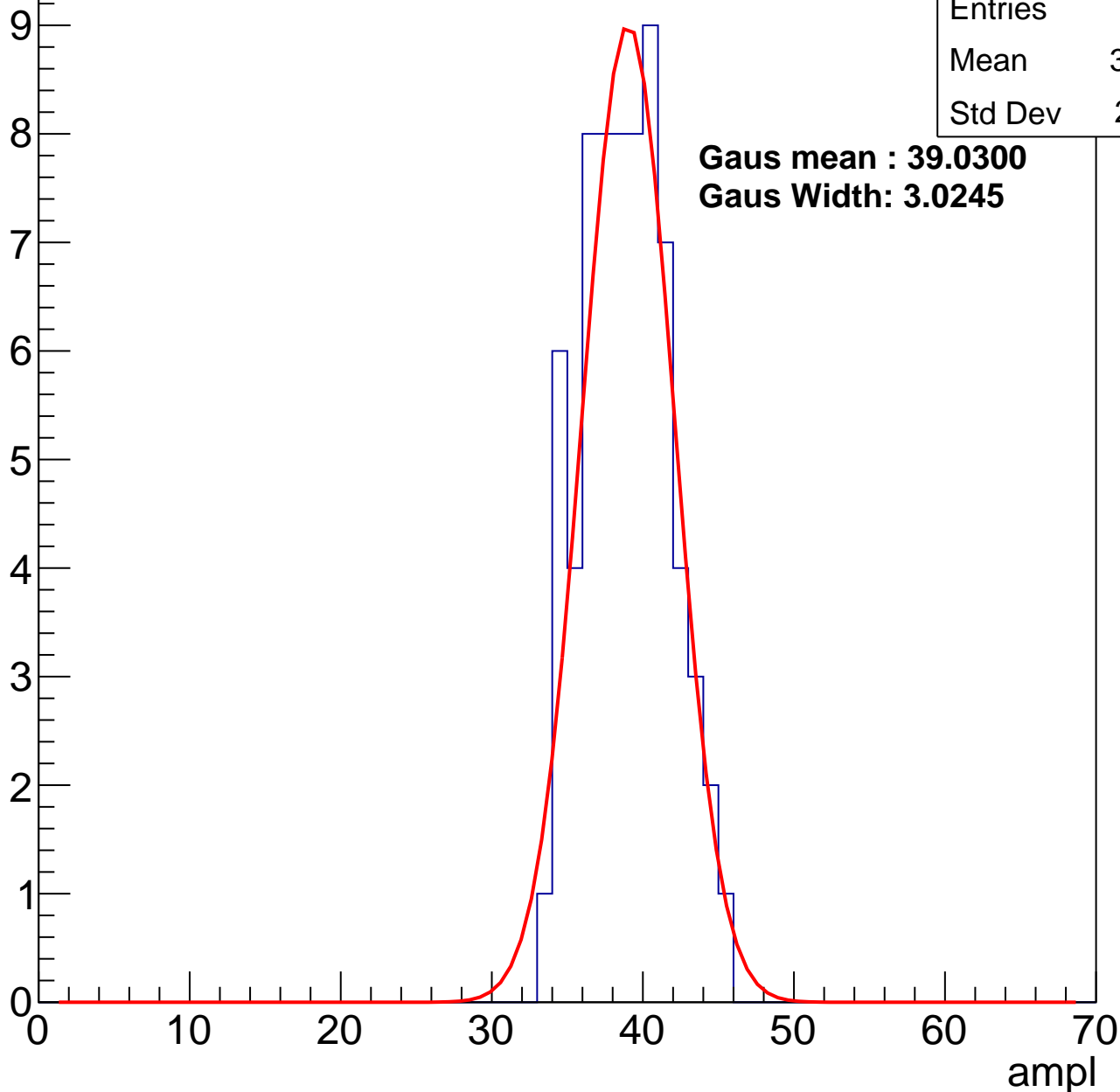
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 69    |
| Mean    | 38.46 |
| Std Dev | 2.821 |

**Gaus mean : 39.0300**

**Gaus Width: 3.0245**



# B0L001S, U2-ch48, adc2

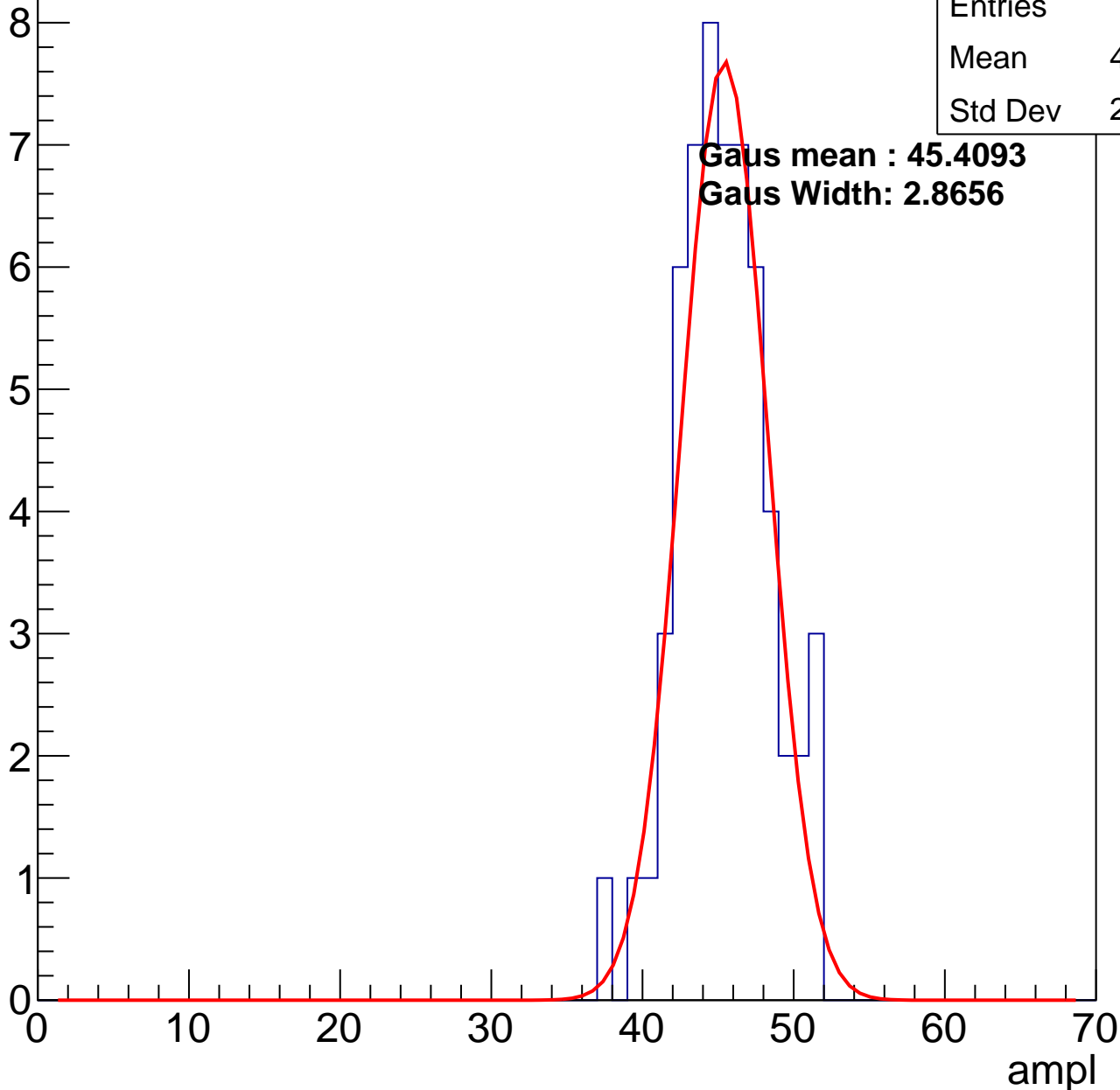
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 58    |
| Mean    | 44.93 |
| Std Dev | 2.993 |

**Gaus mean : 45.4093**

**Gaus Width: 2.8656**

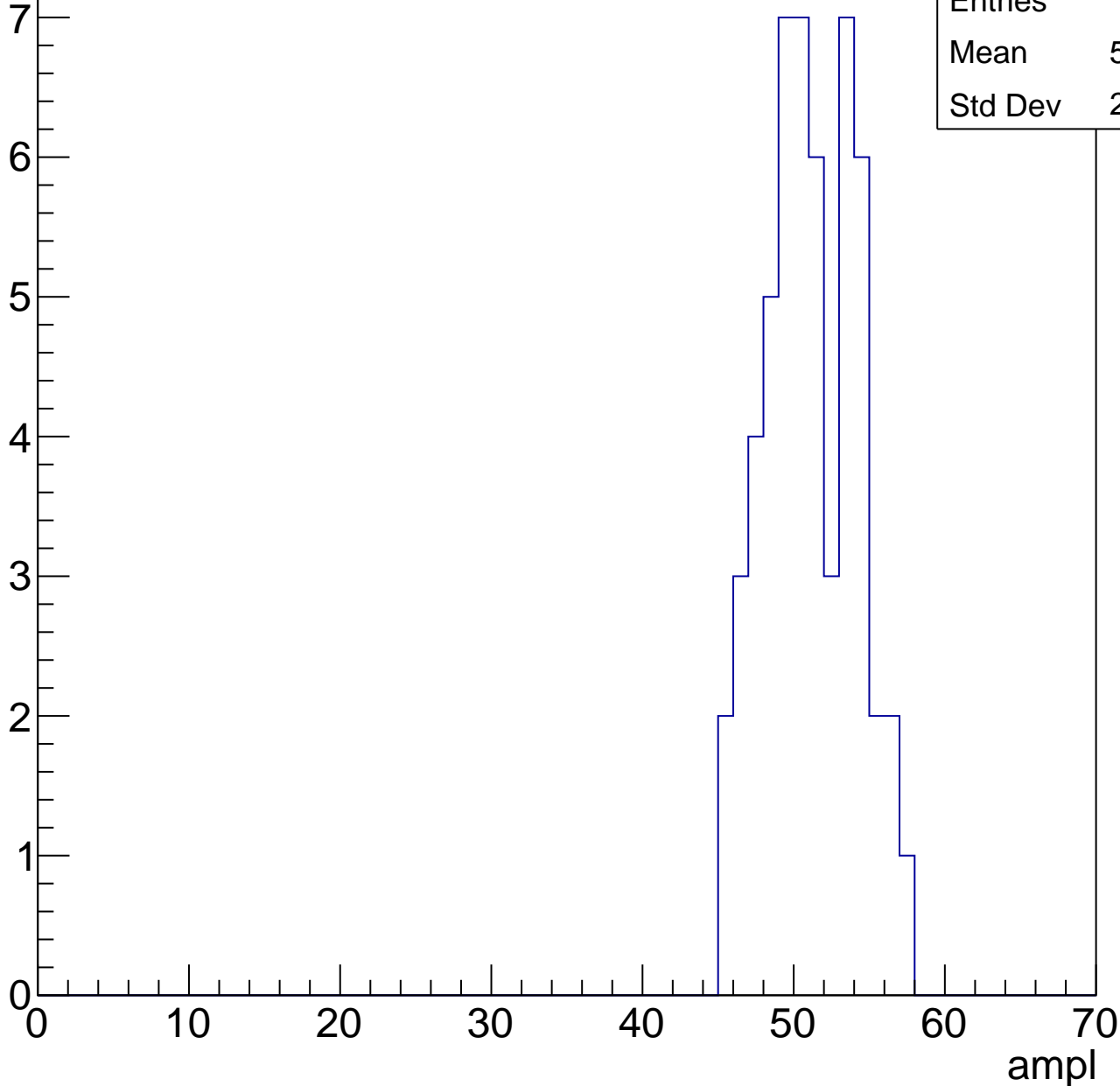


# B0L001S, U2-ch48, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

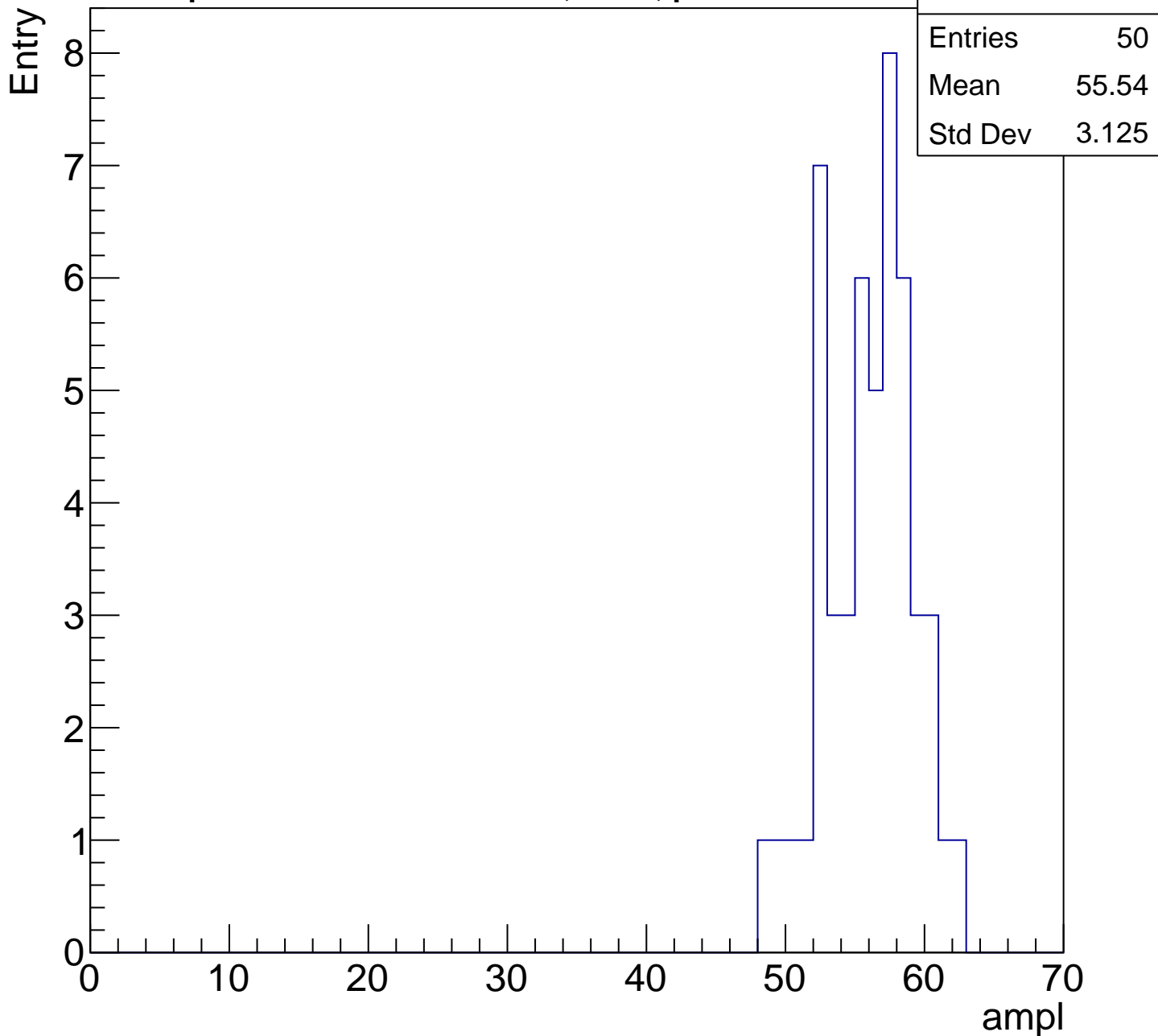
Entry

|         |       |
|---------|-------|
| Entries | 55    |
| Mean    | 50.64 |
| Std Dev | 2.975 |



# B0L001S, U2-ch48, adc4

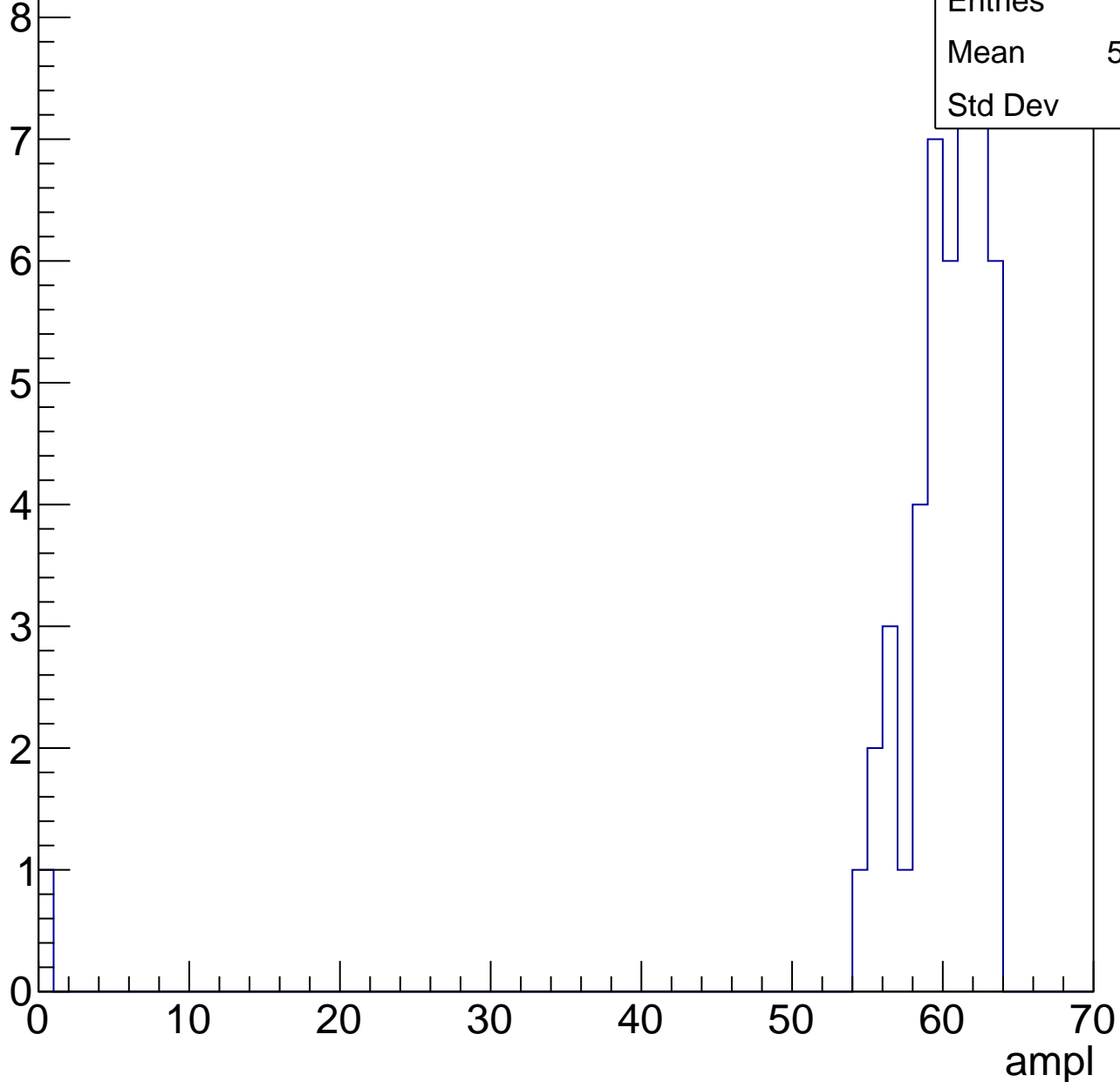
calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U2-ch48, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U2-ch48, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch48, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U2-ch49, adc0

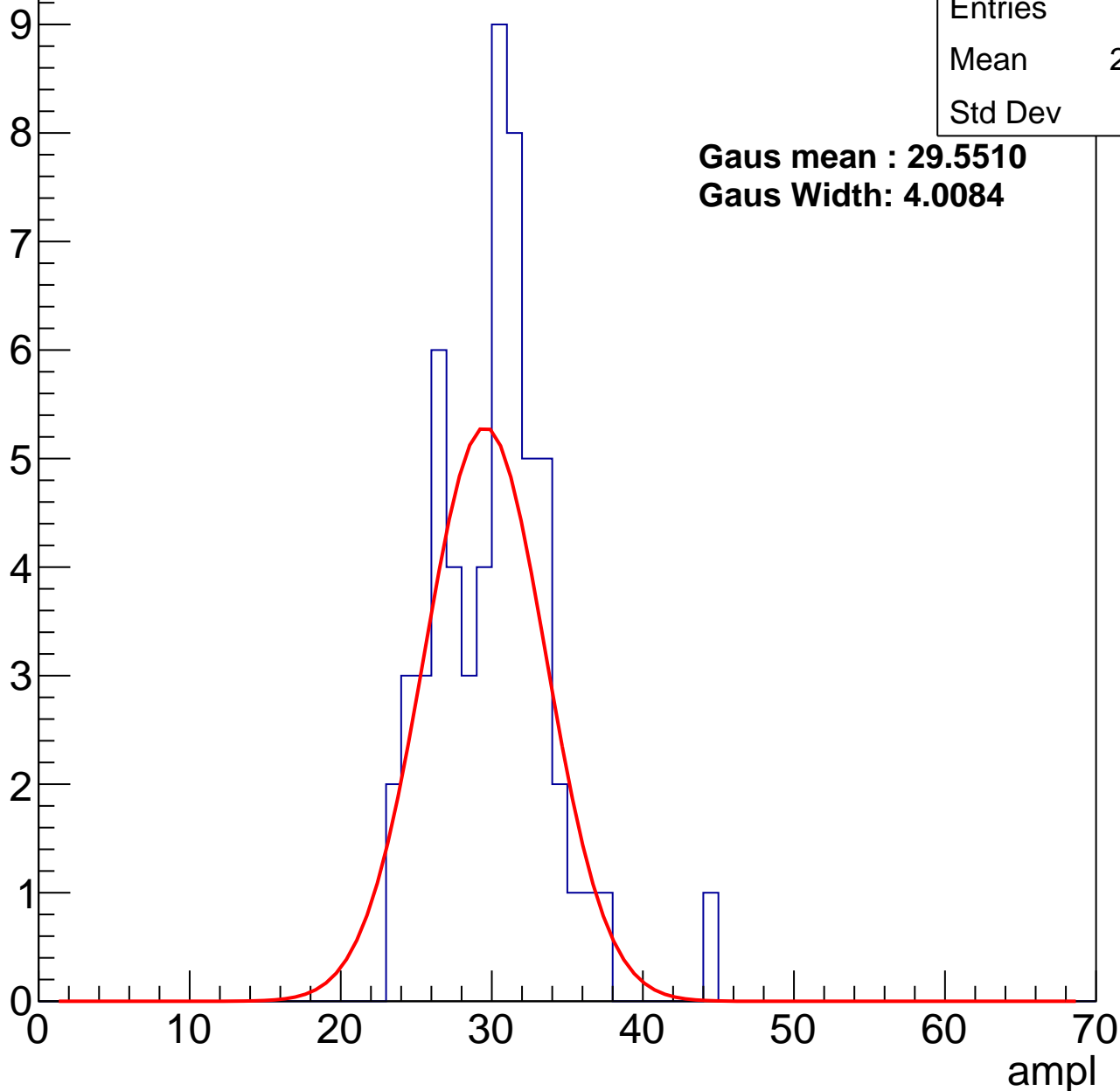
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 58    |
| Mean    | 29.66 |
| Std Dev | 3.79  |

**Gaus mean : 29.5510**

**Gaus Width: 4.0084**



# B0L001S, U2-ch49, adc1

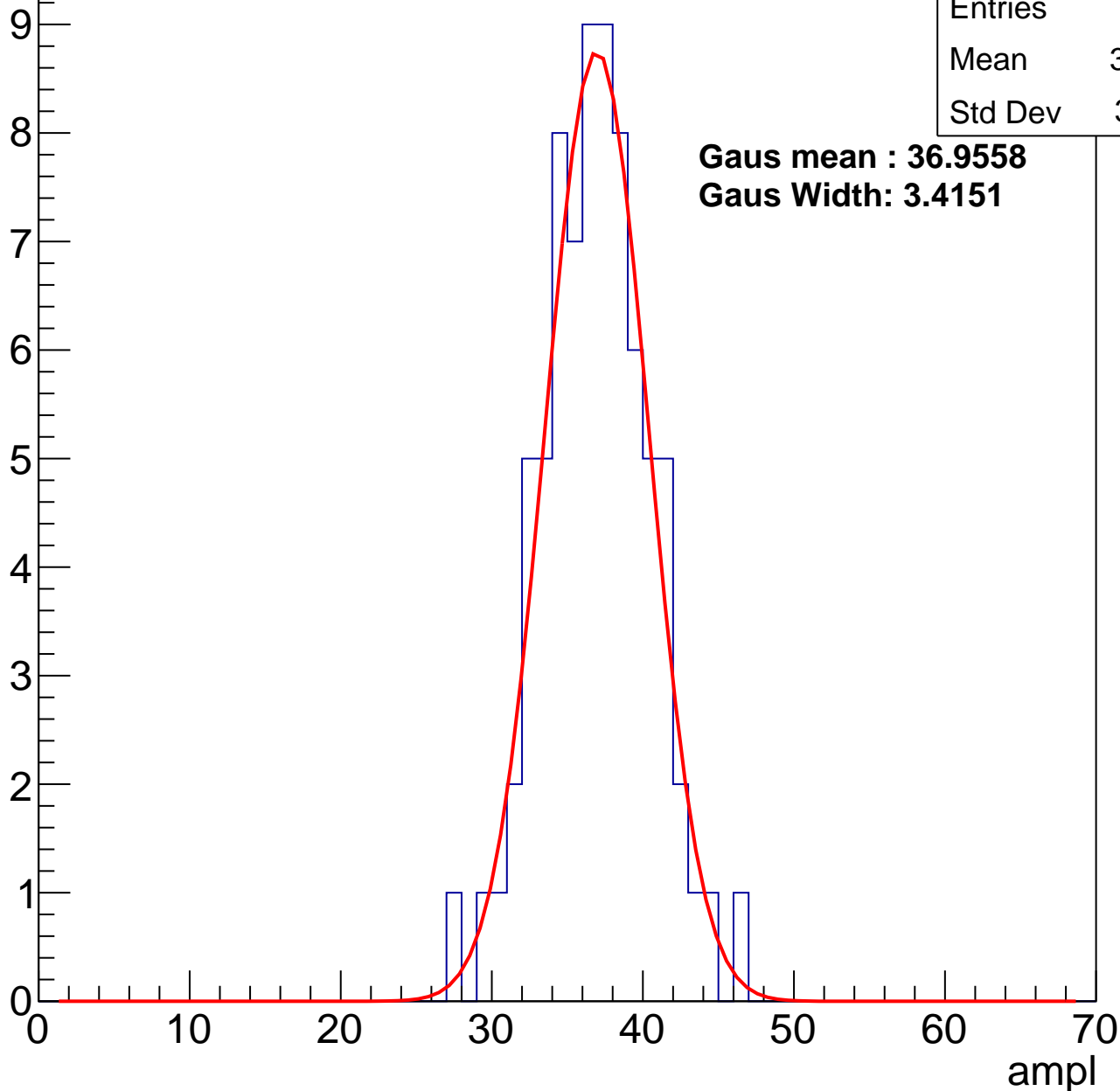
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 77    |
| Mean    | 36.45 |
| Std Dev | 3.511 |

**Gaus mean : 36.9558**

**Gaus Width: 3.4151**



# B0L001S, U2-ch49, adc2

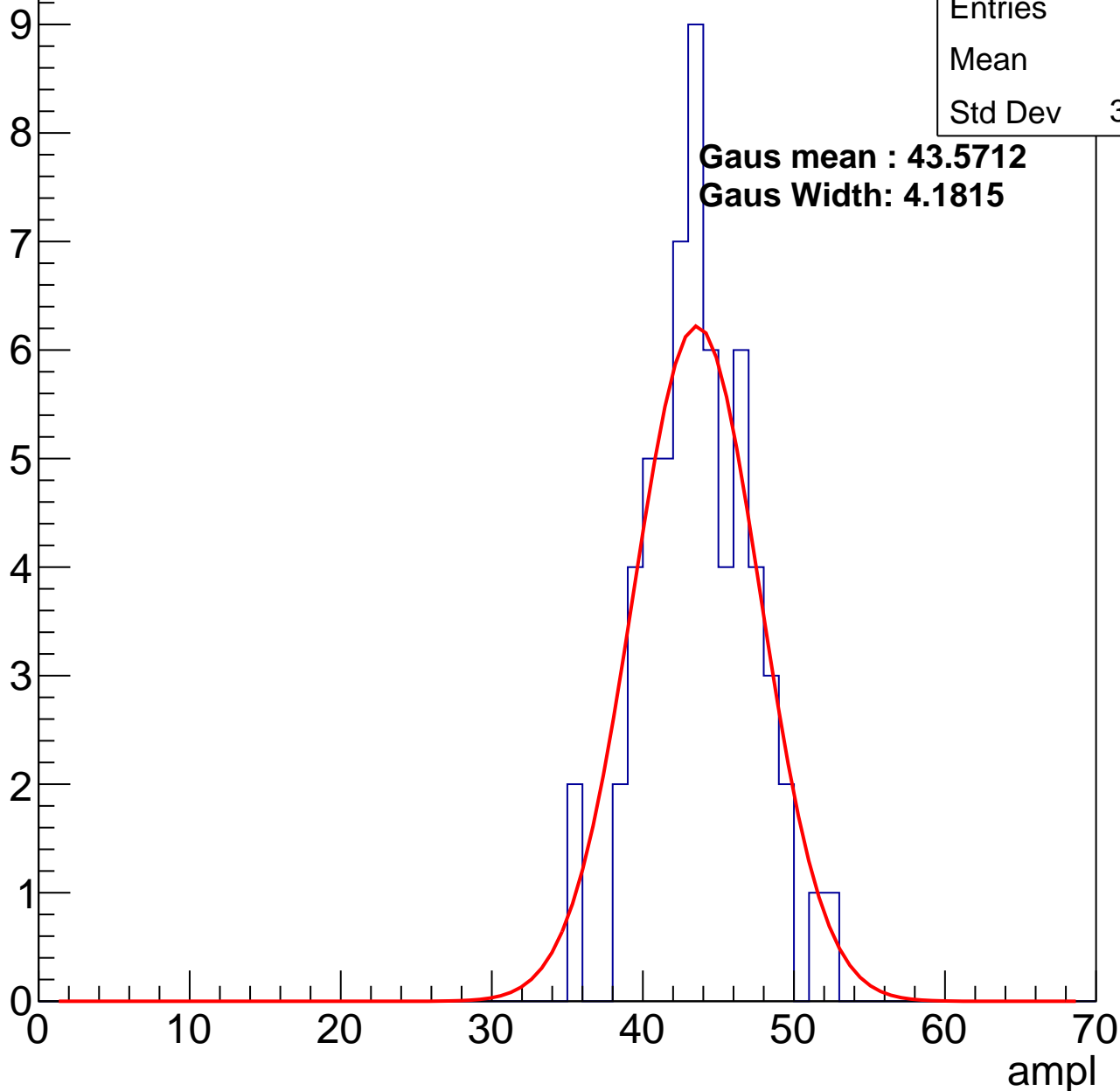
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 61    |
| Mean    | 43.3  |
| Std Dev | 3.485 |

**Gaus mean : 43.5712**

**Gaus Width: 4.1815**

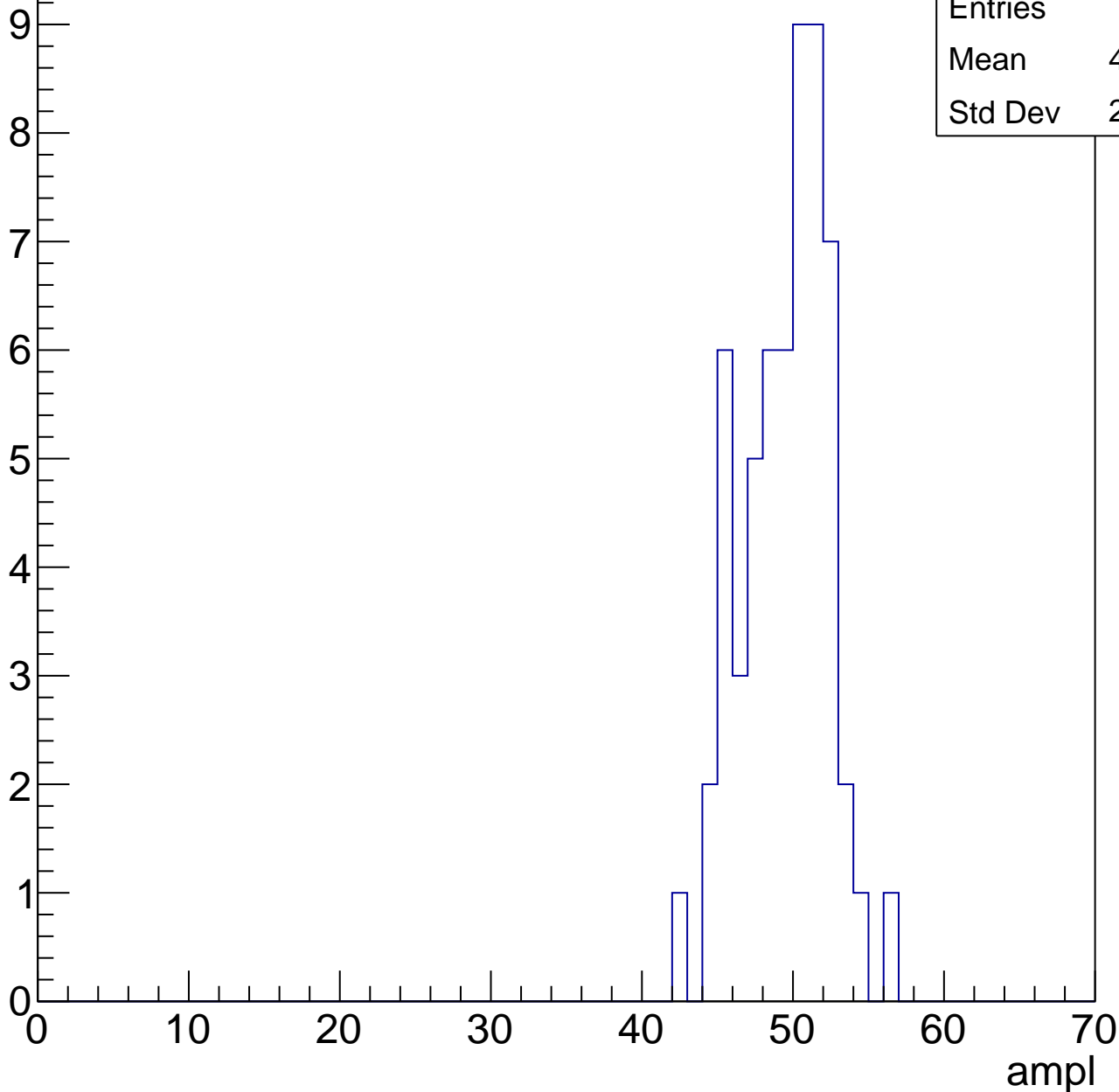


# B0L001S, U2-ch49, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 58    |
| Mean    | 49.03 |
| Std Dev | 2.822 |

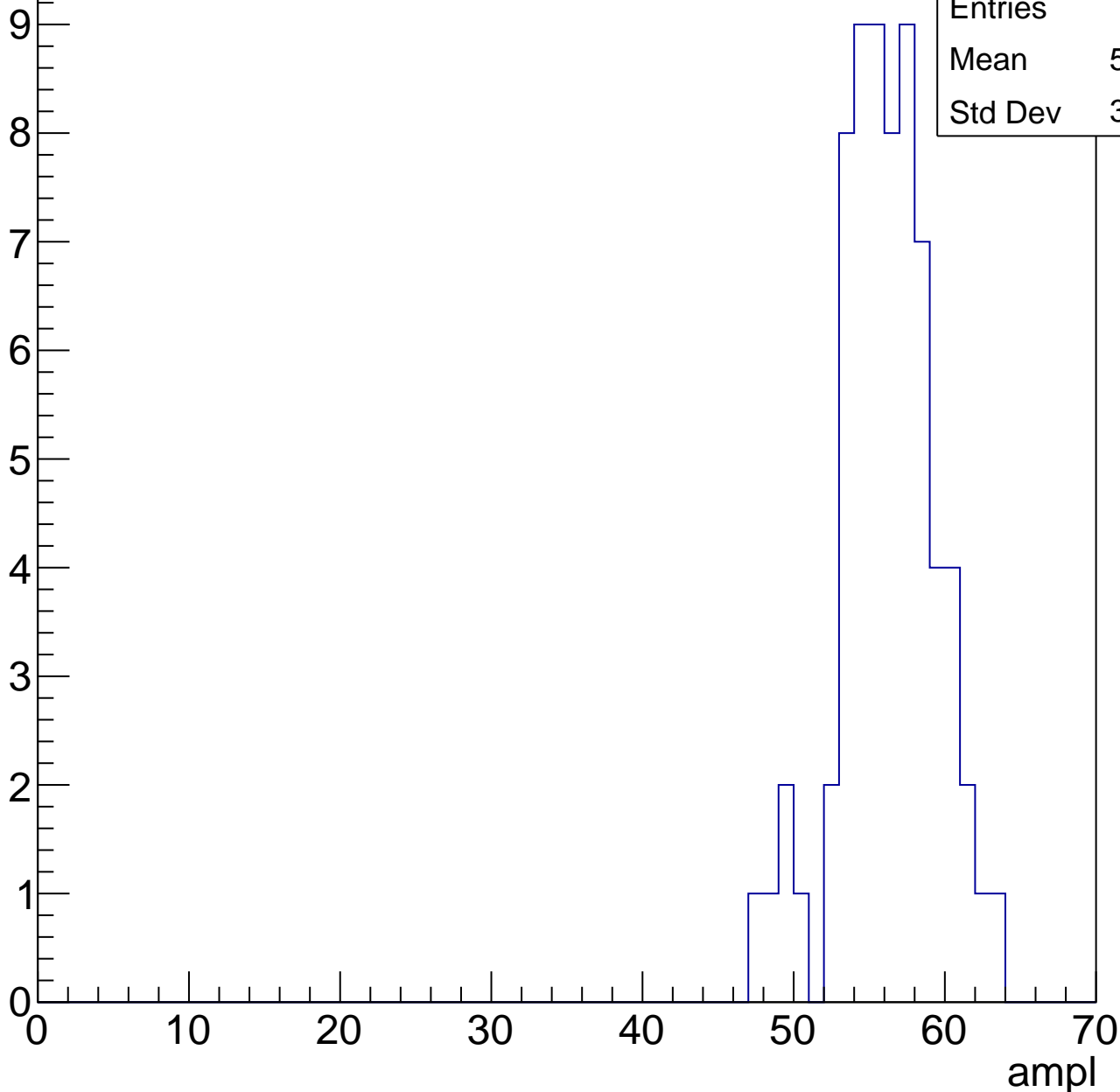


# B0L001S, U2-ch49, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 69    |
| Mean    | 55.68 |
| Std Dev | 3.169 |

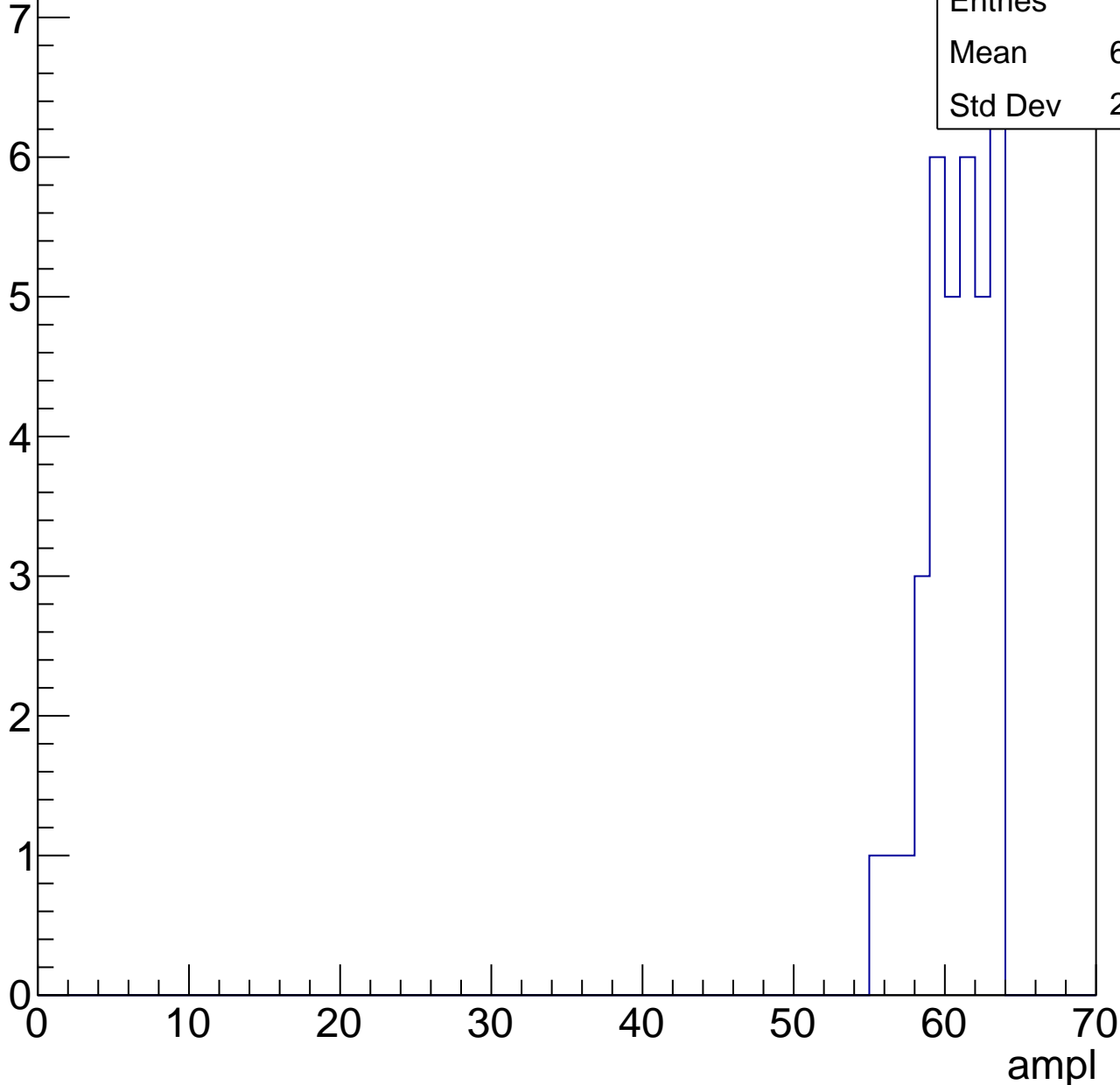


# B0L001S, U2-ch49, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

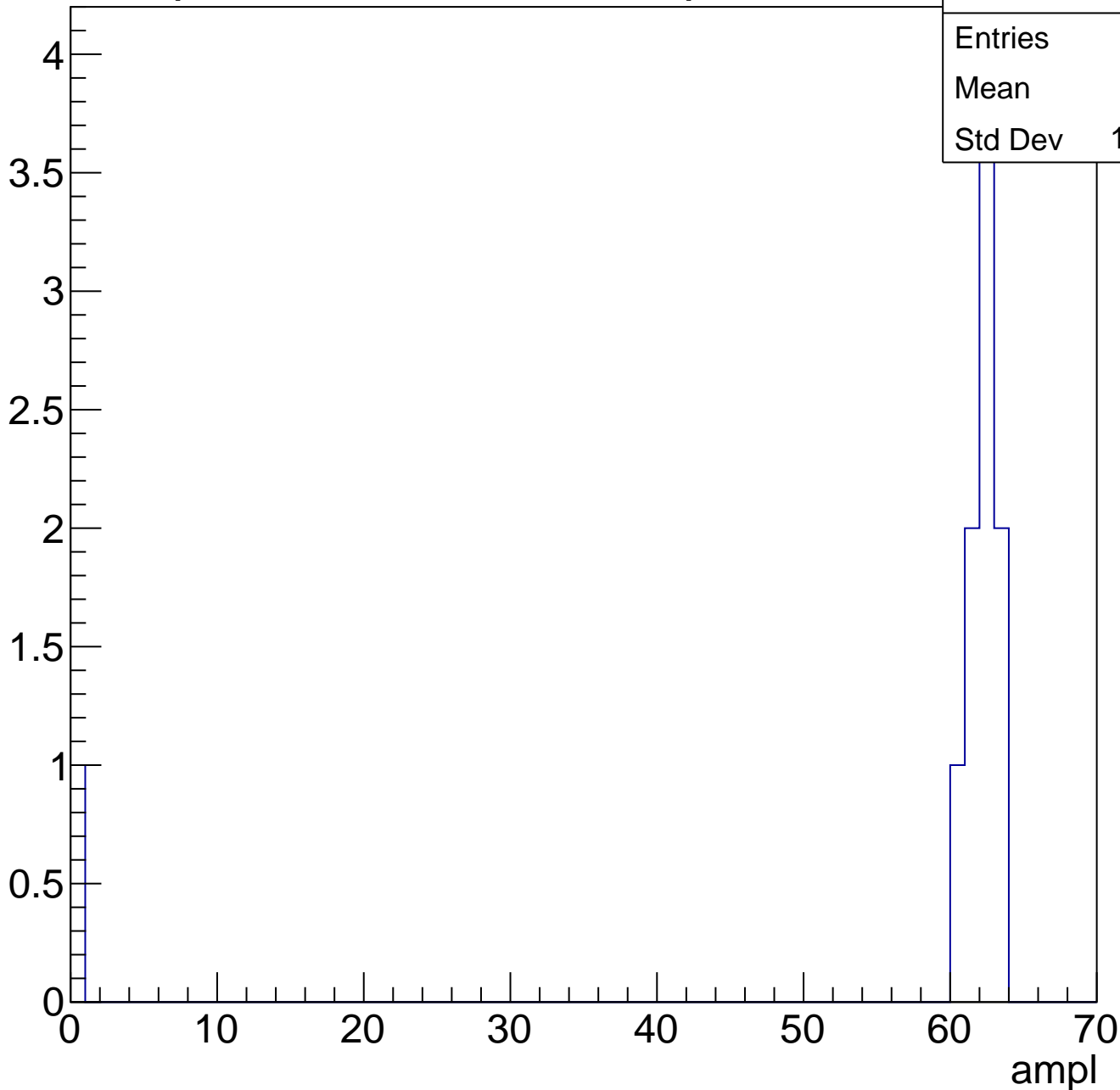
|         |       |
|---------|-------|
| Entries | 35    |
| Mean    | 60.37 |
| Std Dev | 2.085 |



# B0L001S, U2-ch49, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch49, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 1 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch50, adc0

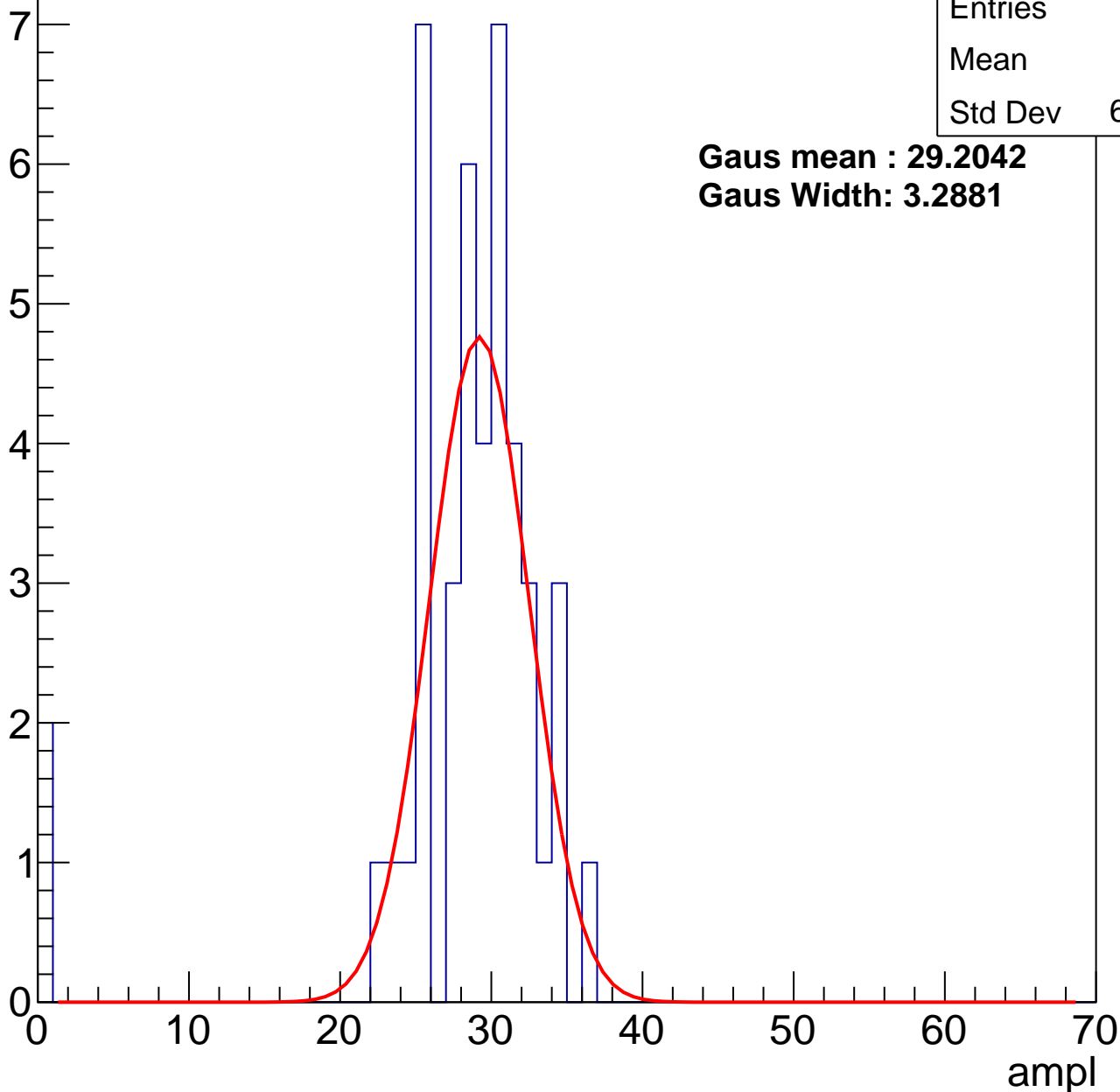
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 44    |
| Mean    | 27.5  |
| Std Dev | 6.764 |

**Gaus mean : 29.2042**

**Gaus Width: 3.2881**



# B0L001S, U2-ch50, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 76    |
| Mean    | 34.33 |
| Std Dev | 5.305 |

**Gaus mean : 35.2187**

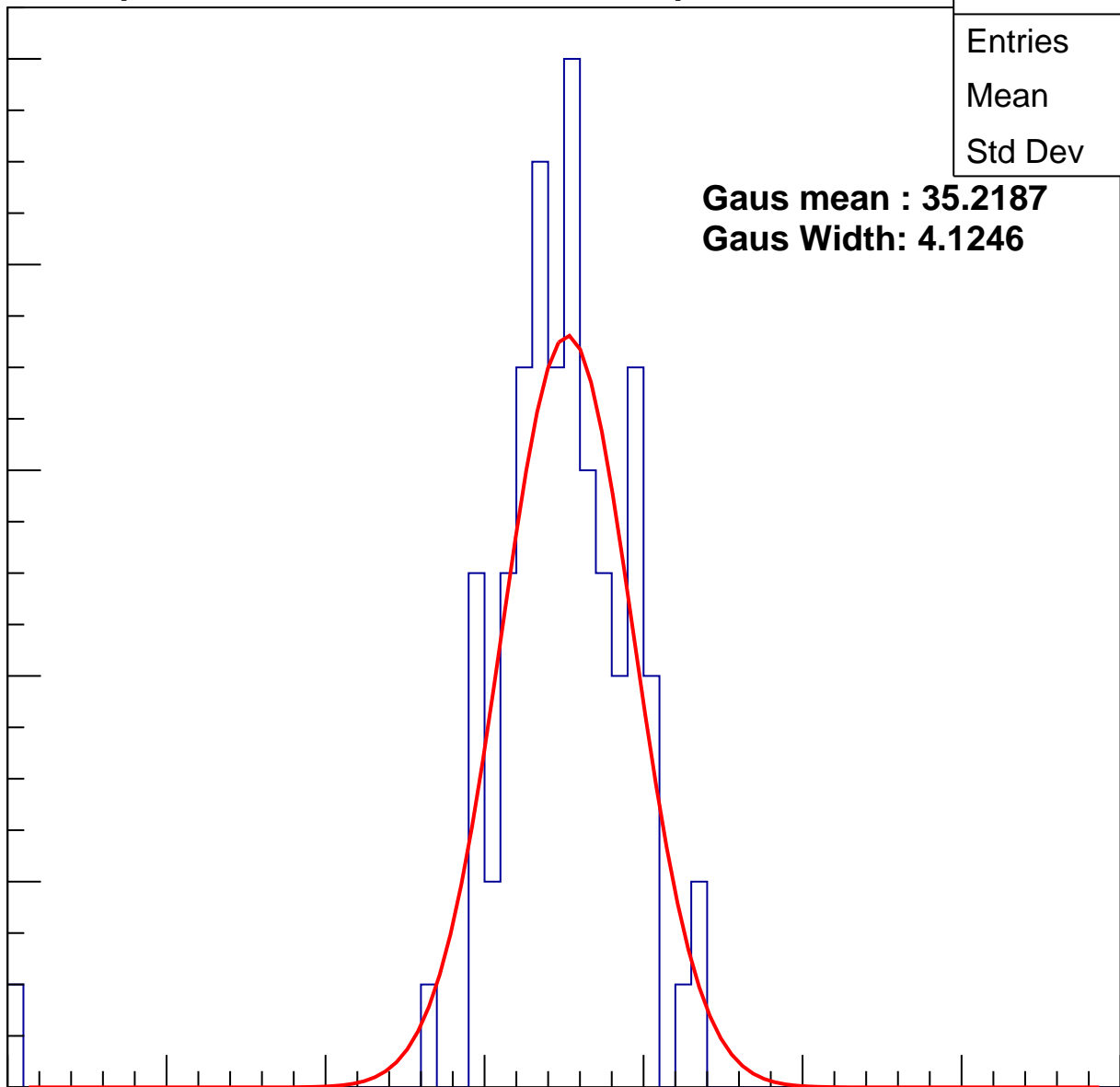
**Gaus Width: 4.1246**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B0L001S, U2-ch50, adc2

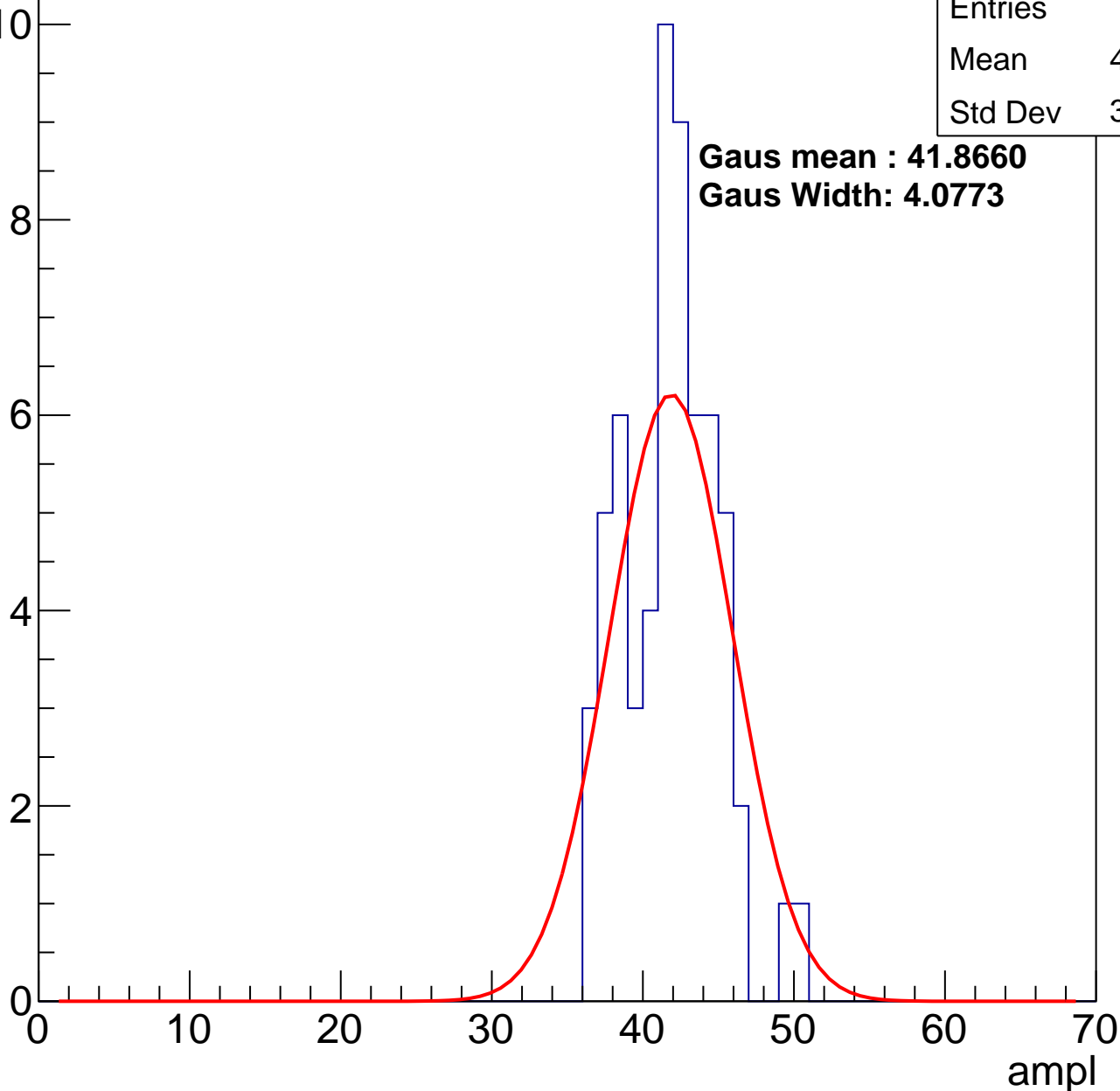
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 61    |
| Mean    | 41.38 |
| Std Dev | 3.079 |

**Gaus mean : 41.8660**

**Gaus Width: 4.0773**



# B0L001S, U2-ch50, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

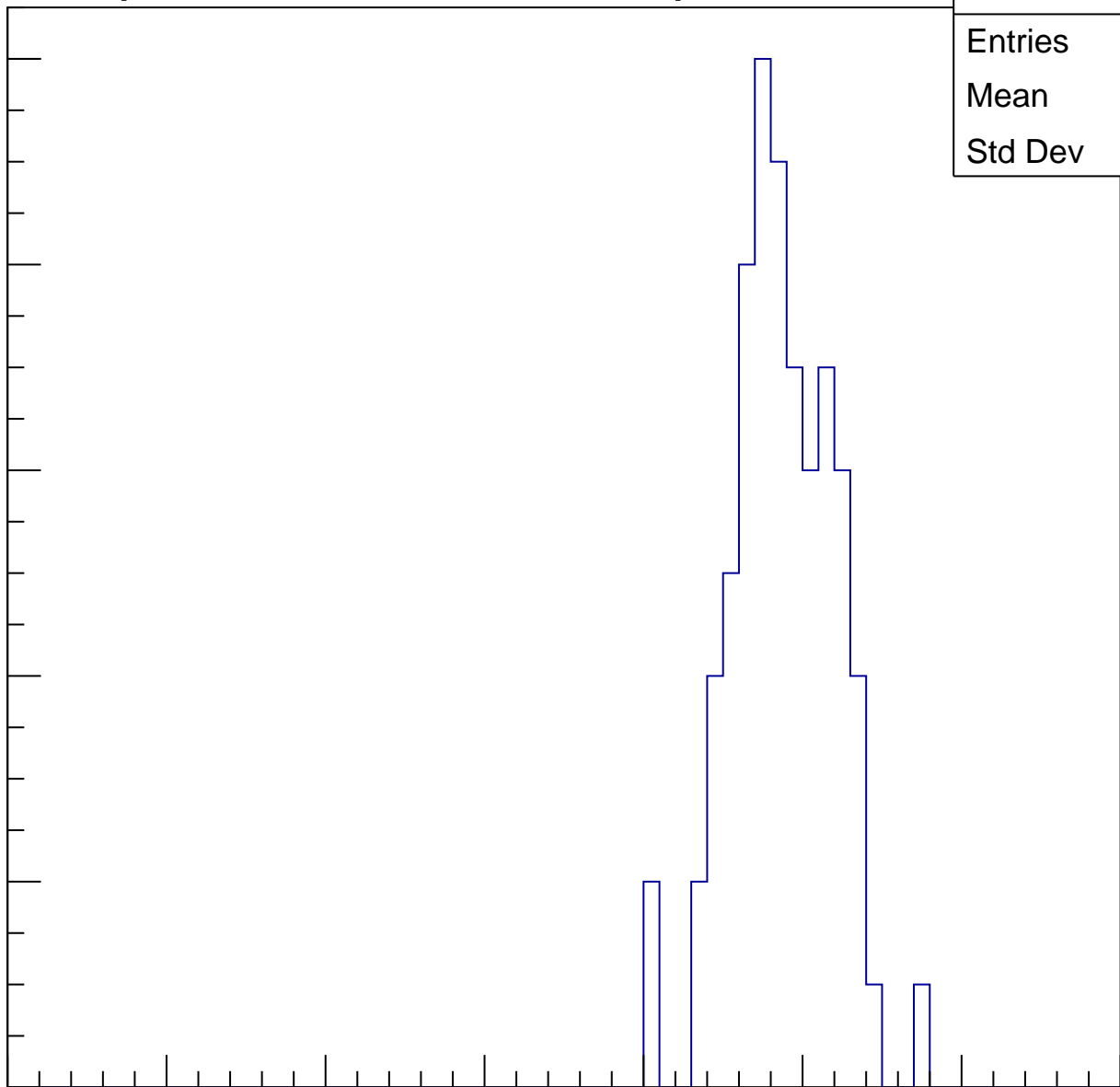
|         |       |
|---------|-------|
| Entries | 72    |
| Mean    | 48.22 |
| Std Dev | 3.189 |

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

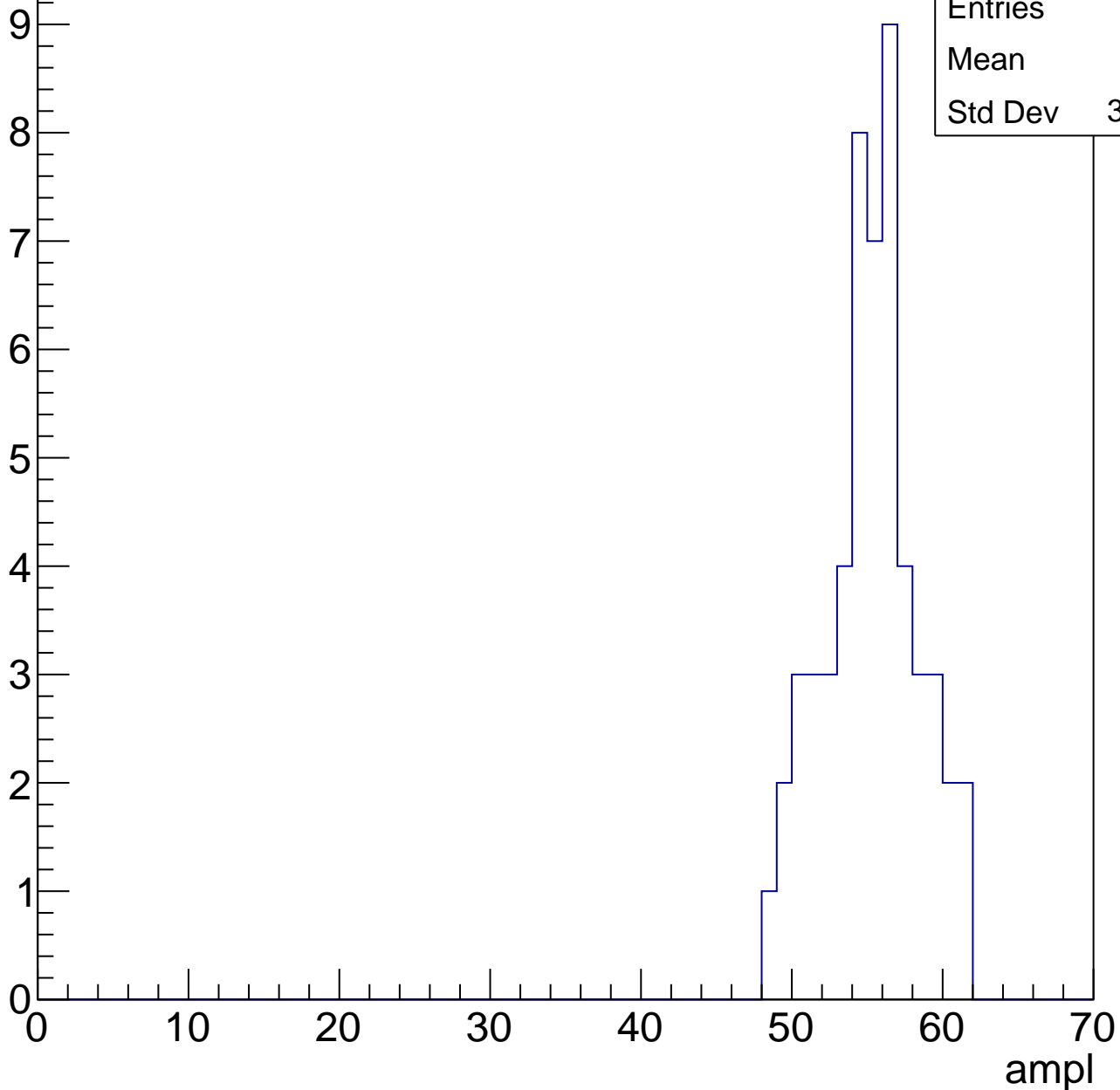


# B0L001S, U2-ch50, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

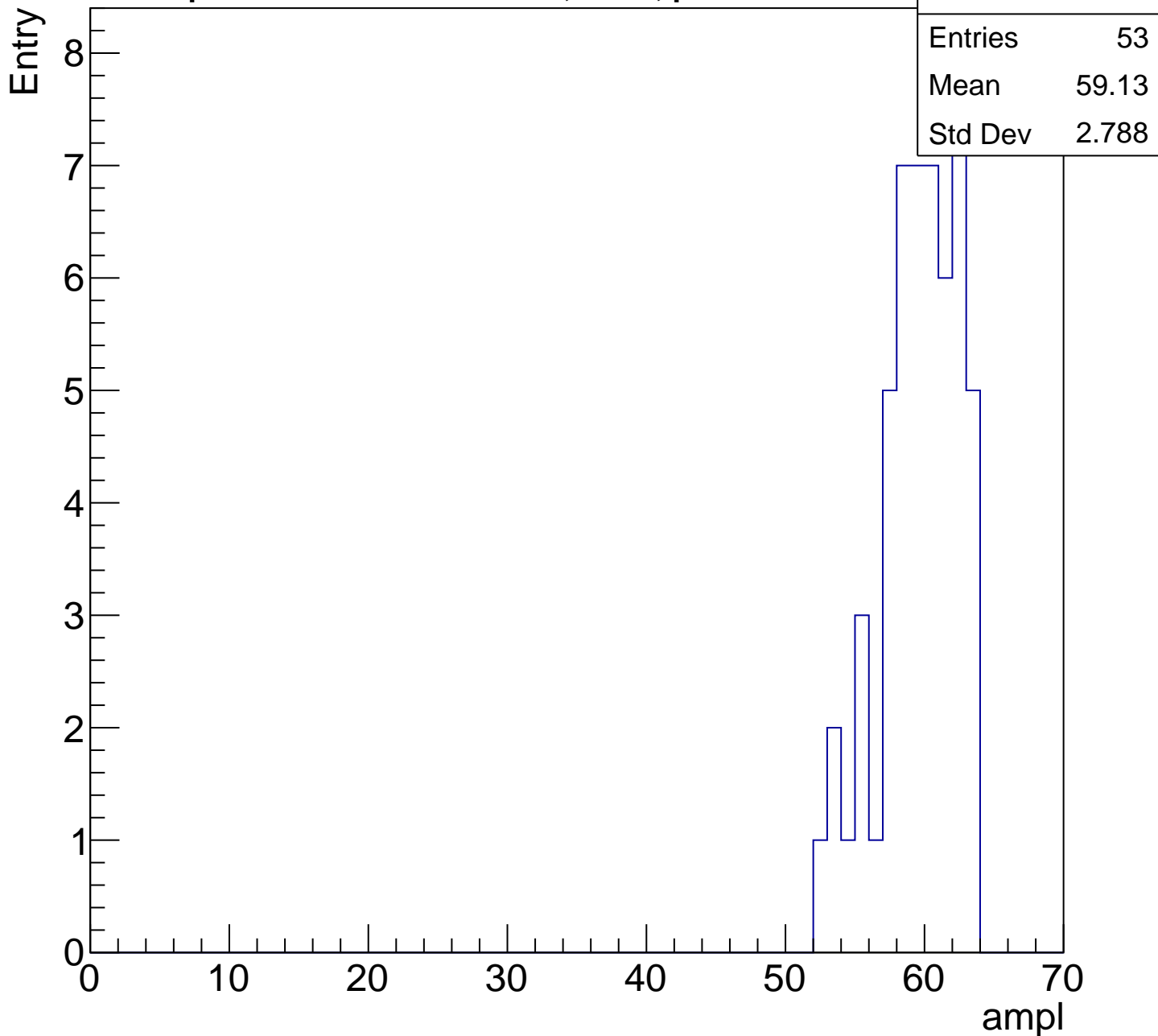
Entry

|         |       |
|---------|-------|
| Entries | 54    |
| Mean    | 54.8  |
| Std Dev | 3.087 |



# B0L001S, U2-ch50, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

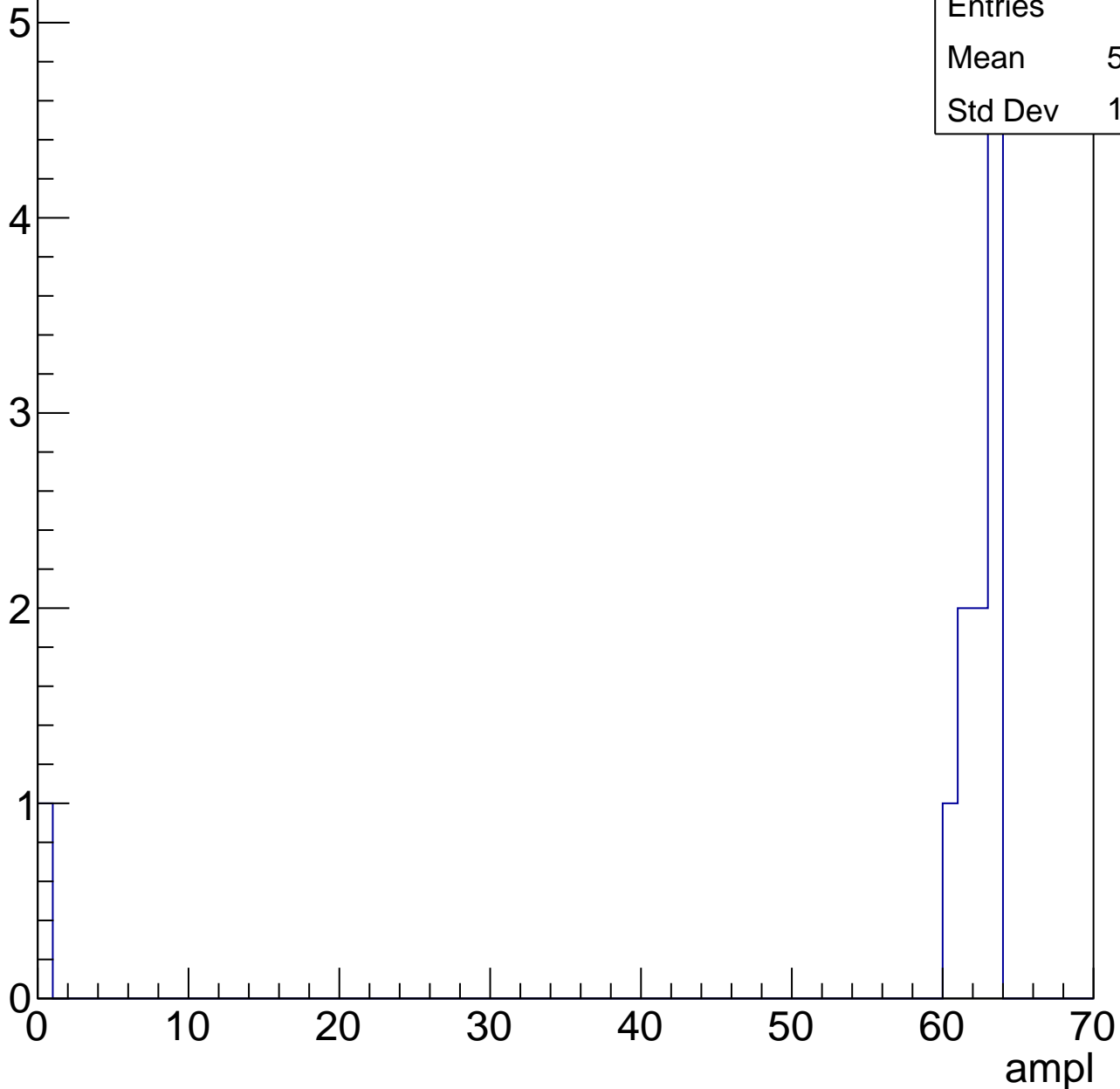


# B0L001S, U2-ch50, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 11    |
| Mean    | 56.45 |
| Std Dev | 17.88 |





# B0L001S, U2-ch50, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 1 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch51, adc0

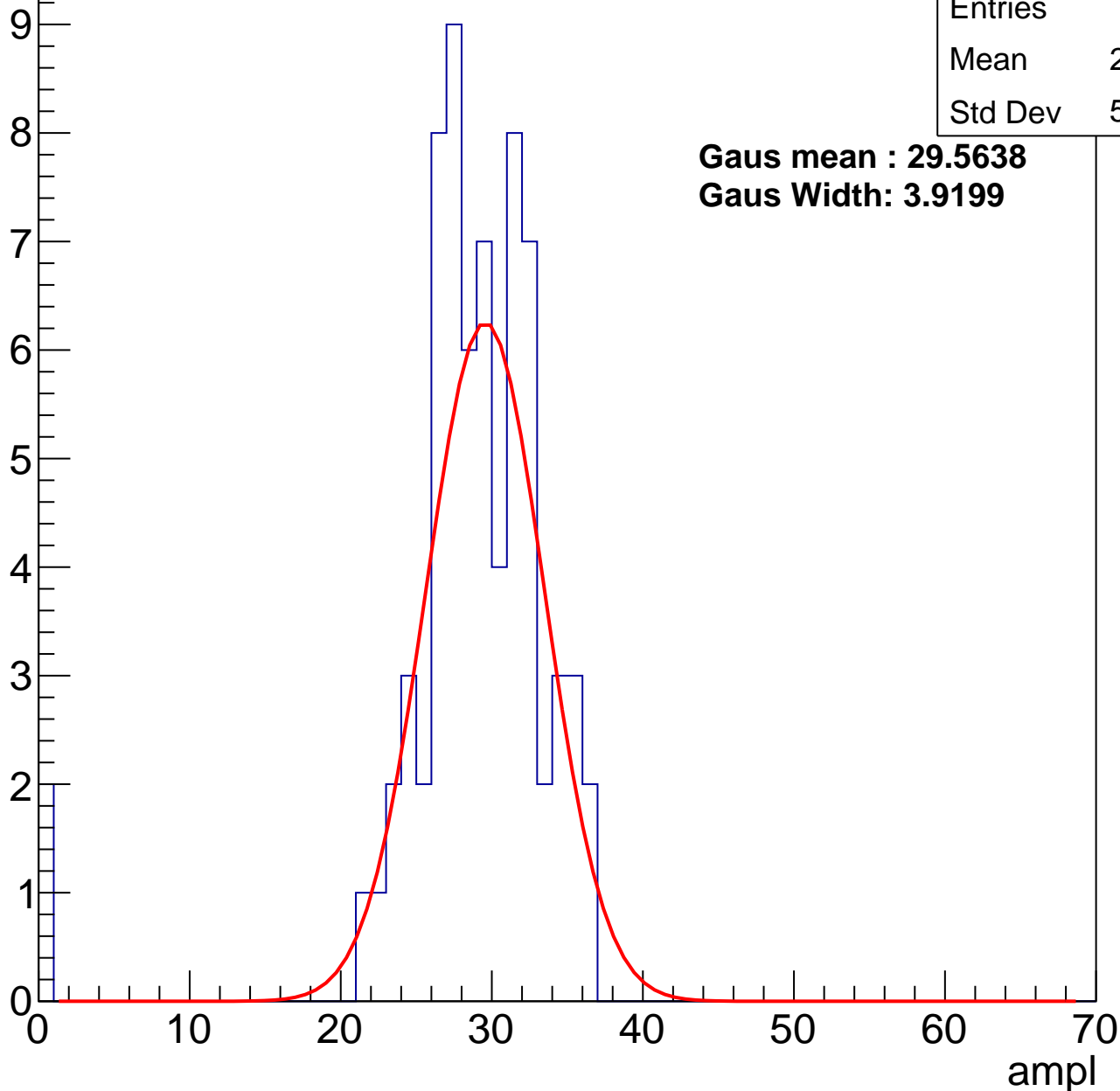
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 70    |
| Mean    | 28.14 |
| Std Dev | 5.914 |

**Gaus mean : 29.5638**

**Gaus Width: 3.9199**



# B0L001S, U2-ch51, adc1

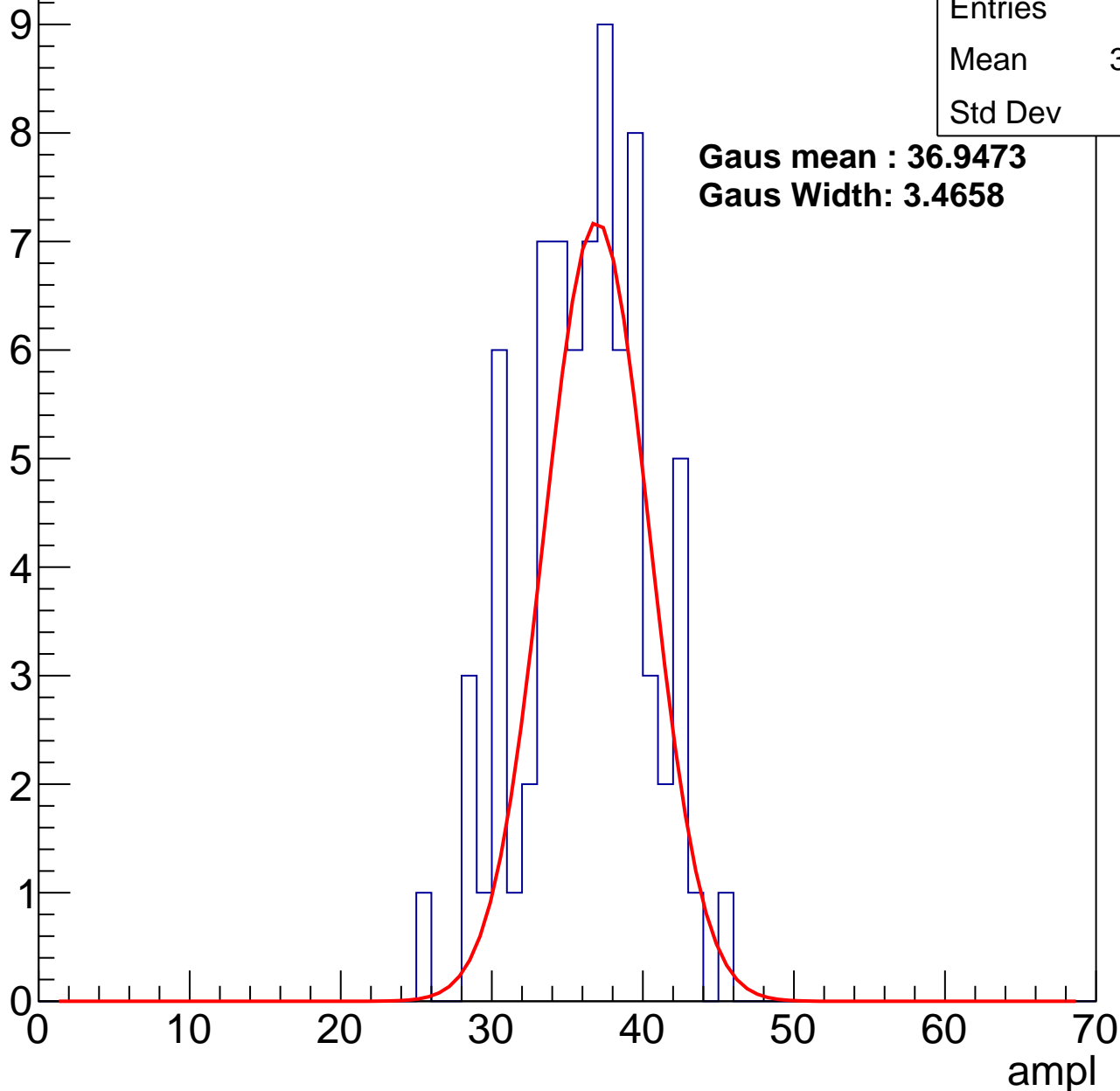
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 76    |
| Mean    | 35.75 |
| Std Dev | 4.04  |

**Gaus mean : 36.9473**

**Gaus Width: 3.4658**



# B0L001S, U2-ch51, adc2

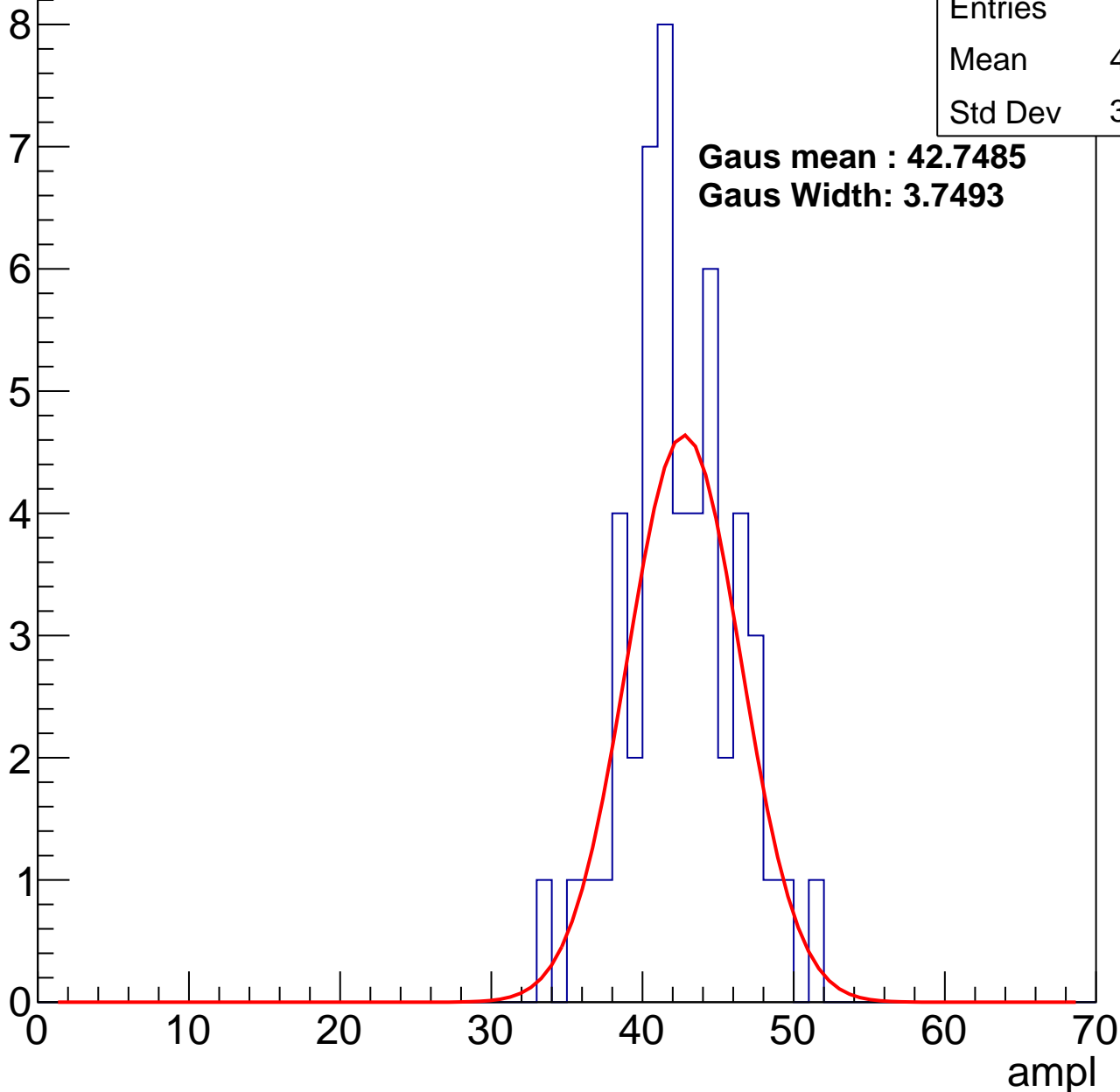
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 51    |
| Mean    | 42.08 |
| Std Dev | 3.597 |

**Gaus mean : 42.7485**

**Gaus Width: 3.7493**

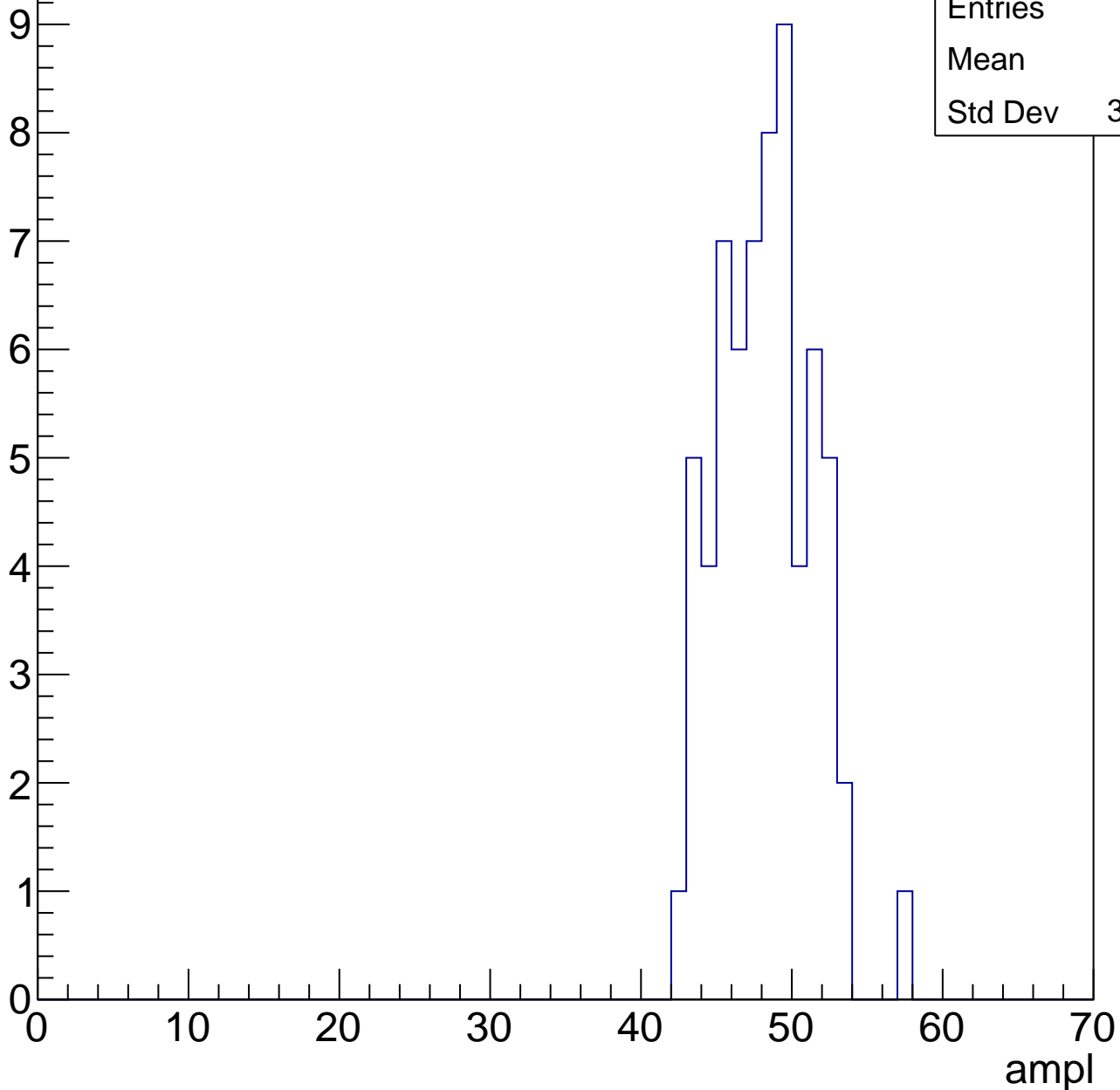


# B0L001S, U2-ch51, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 65    |
| Mean    | 47.8  |
| Std Dev | 3.054 |



# B0L001S, U2-ch51, adc4

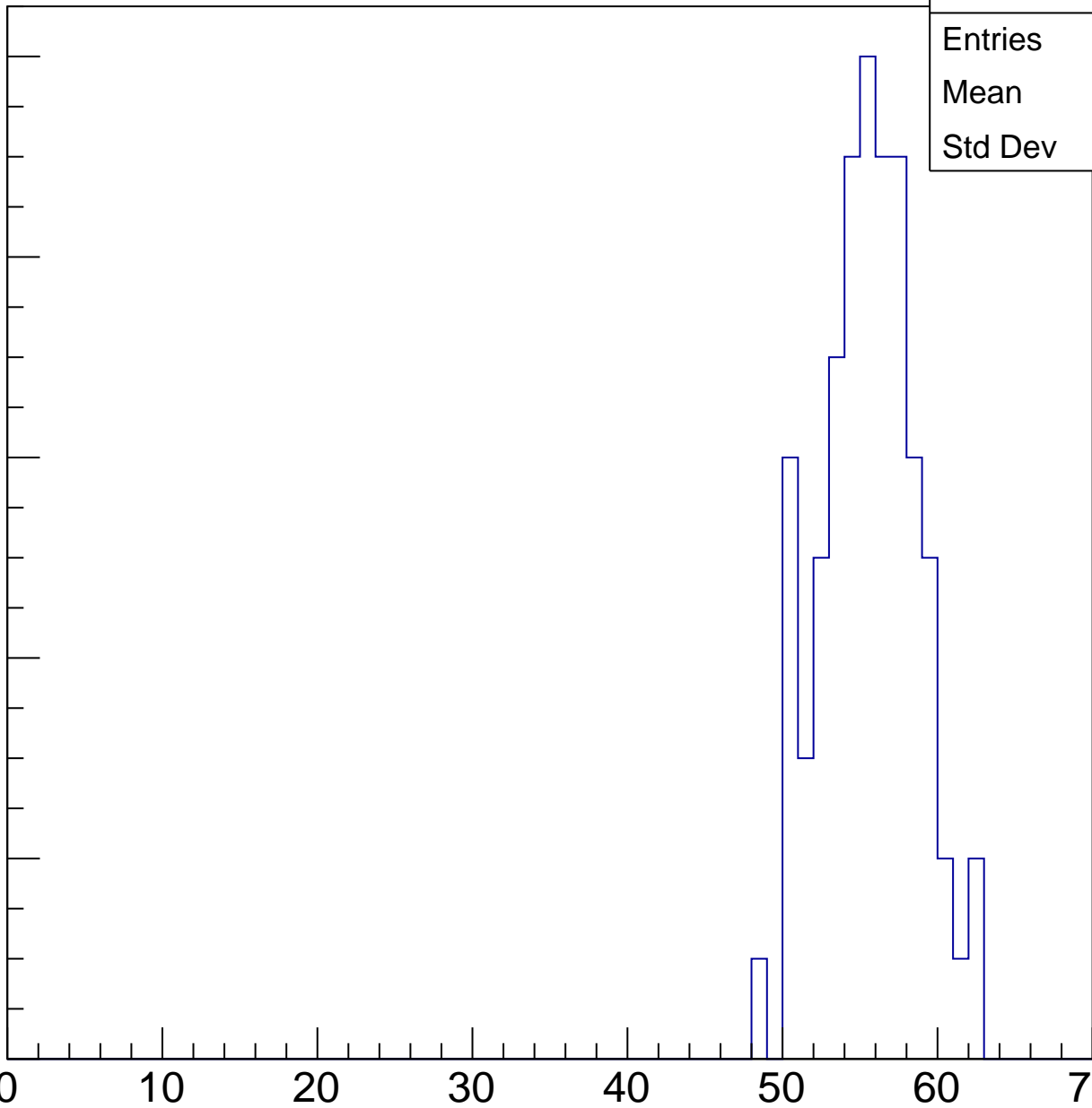
calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 75    |
| Mean    | 55.11 |
| Std Dev | 3.036 |

Entry

10  
8  
6  
4  
2  
0

ampl

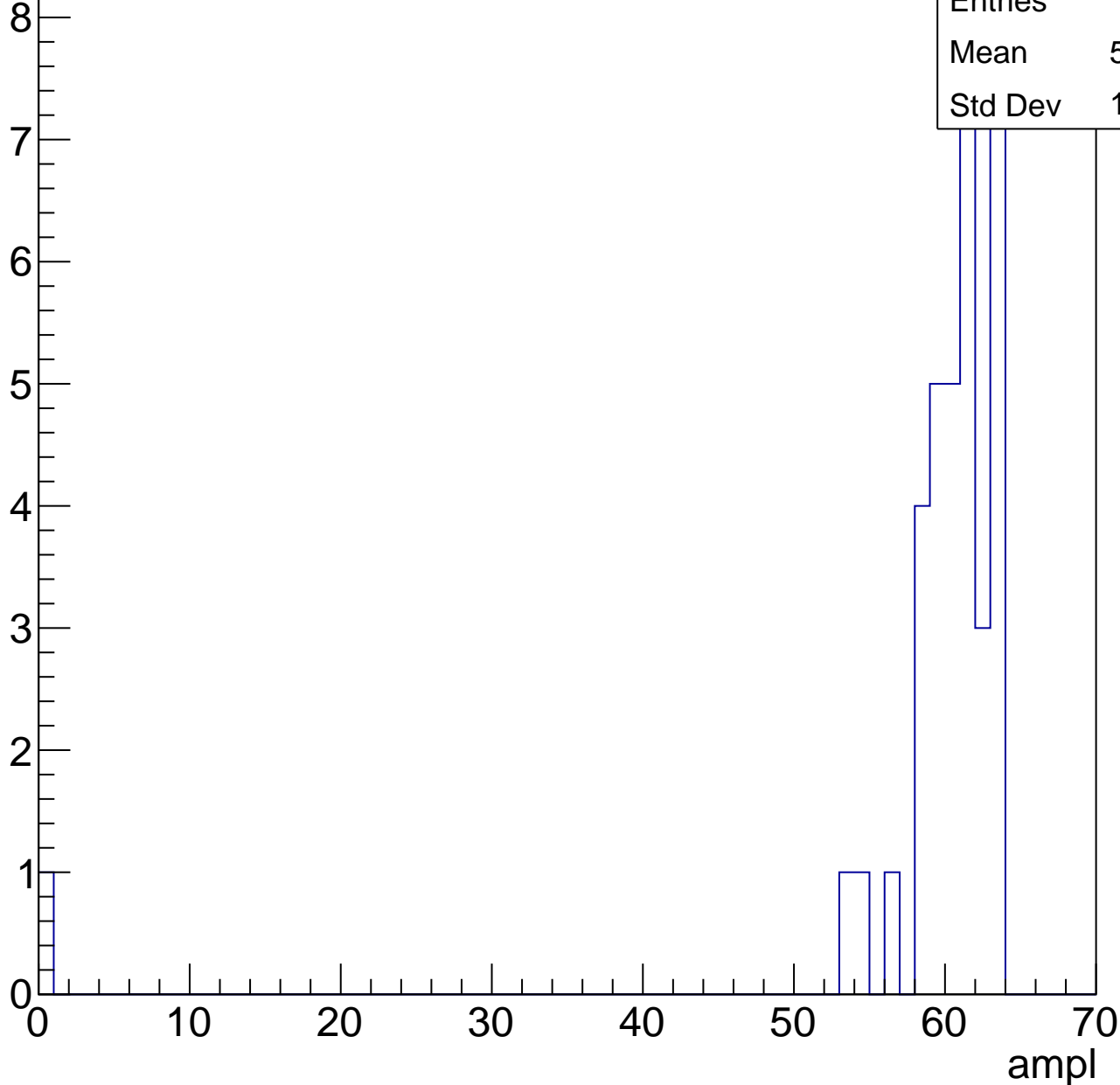


# B0L001S, U2-ch51, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

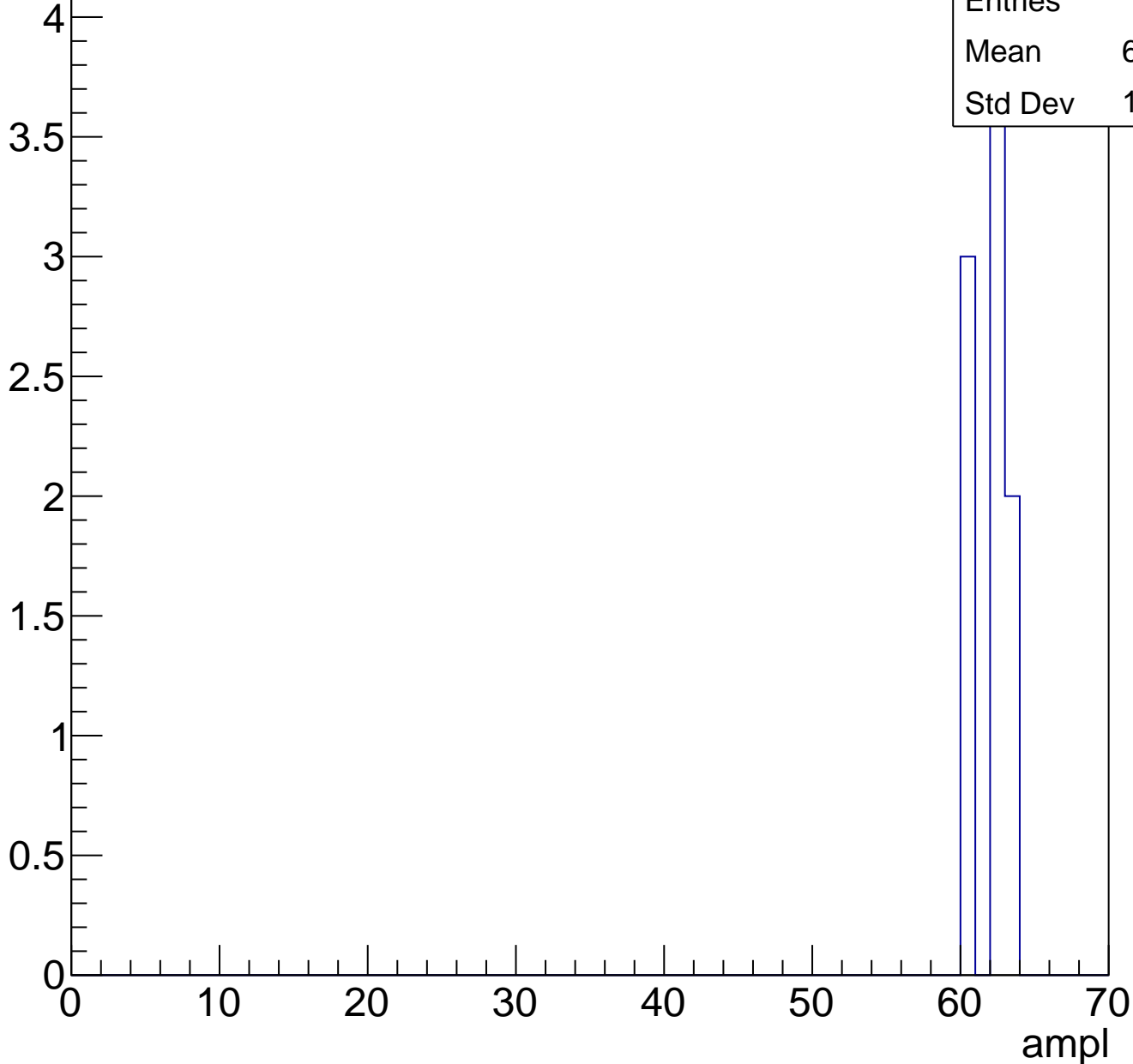
|         |       |
|---------|-------|
| Entries | 37    |
| Mean    | 58.59 |
| Std Dev | 10.06 |



# B0L001S, U2-ch51, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

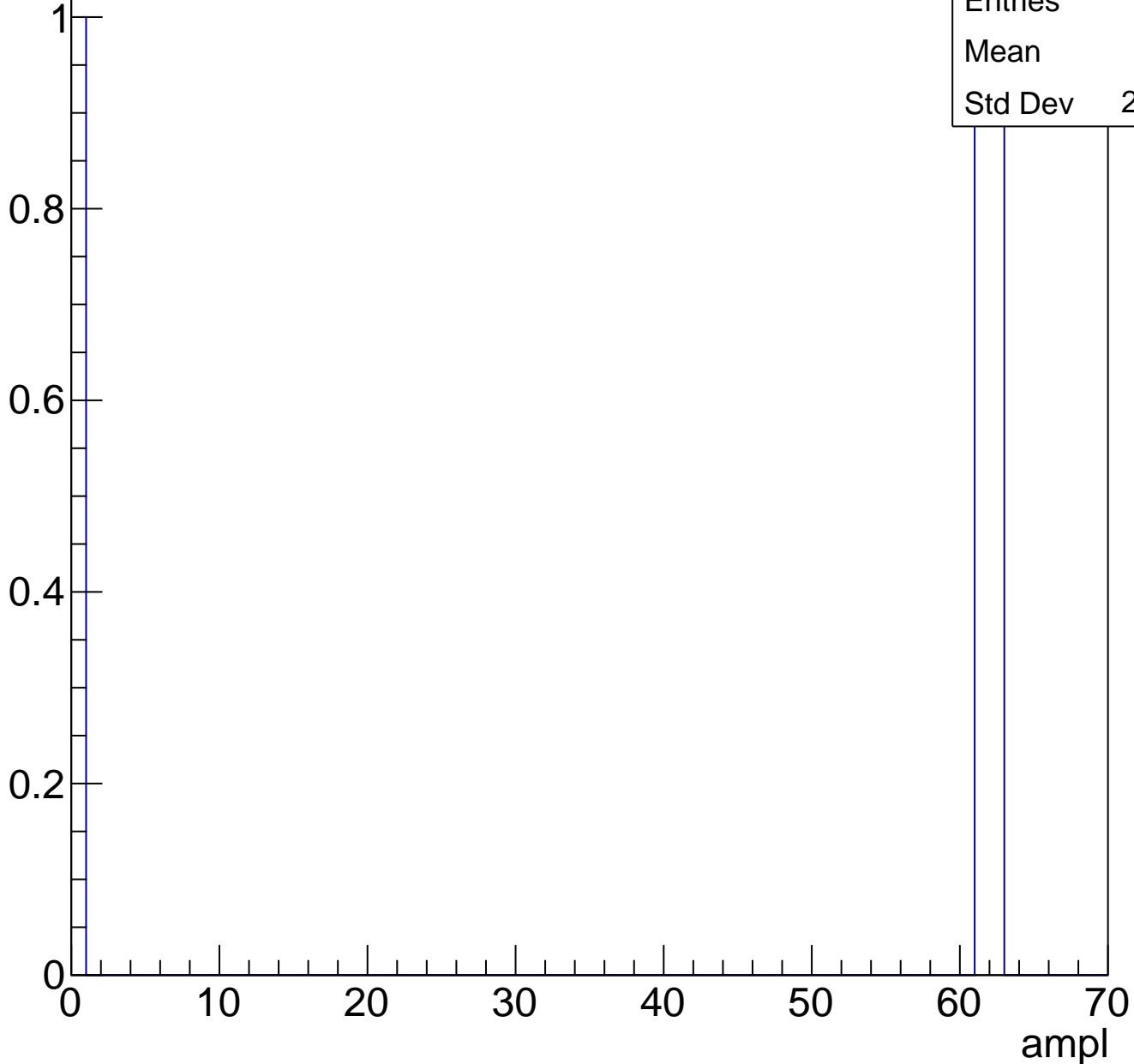




# B0L001S, U2-ch51, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U2-ch52, adc0

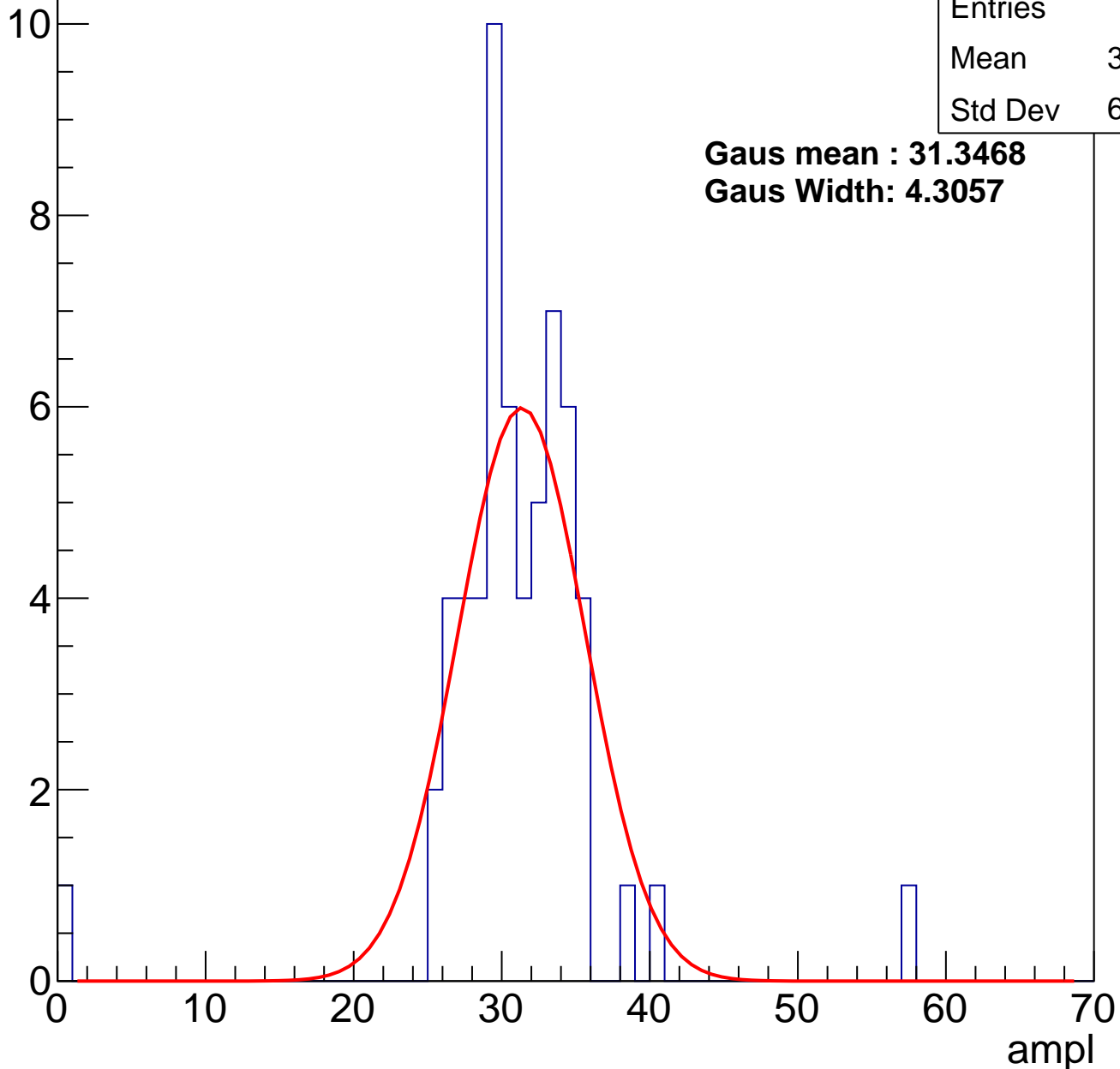
calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 60    |
| Mean    | 30.63 |
| Std Dev | 6.094 |

**Gaus mean : 31.3468**

**Gaus Width: 4.3057**

Entry



# B0L001S, U2-ch52, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 81    |
| Mean    | 37.53 |
| Std Dev | 3.732 |

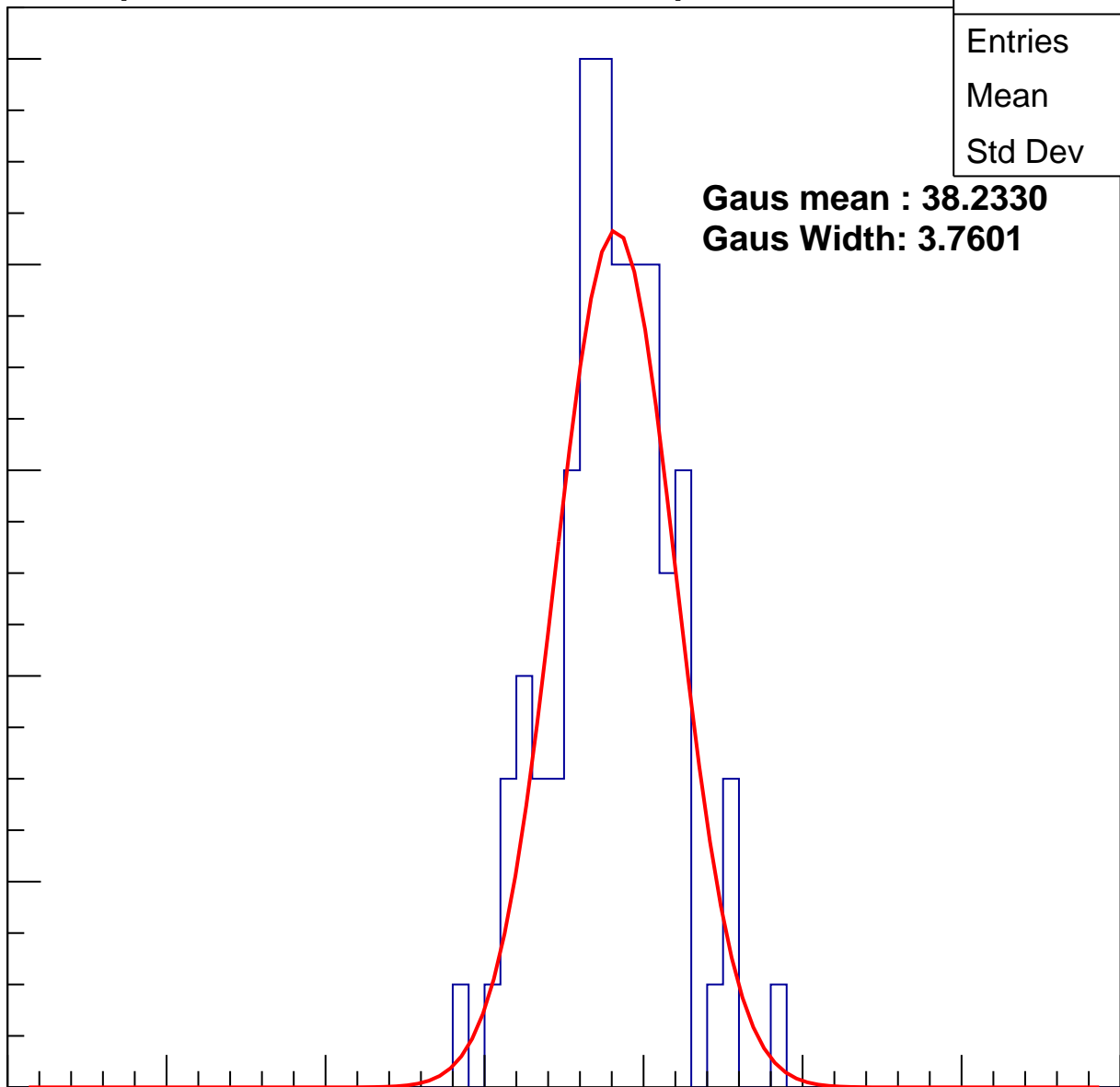
**Gaus mean : 38.2330**  
**Gaus Width: 3.7601**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B0L001S, U2-ch52, adc2

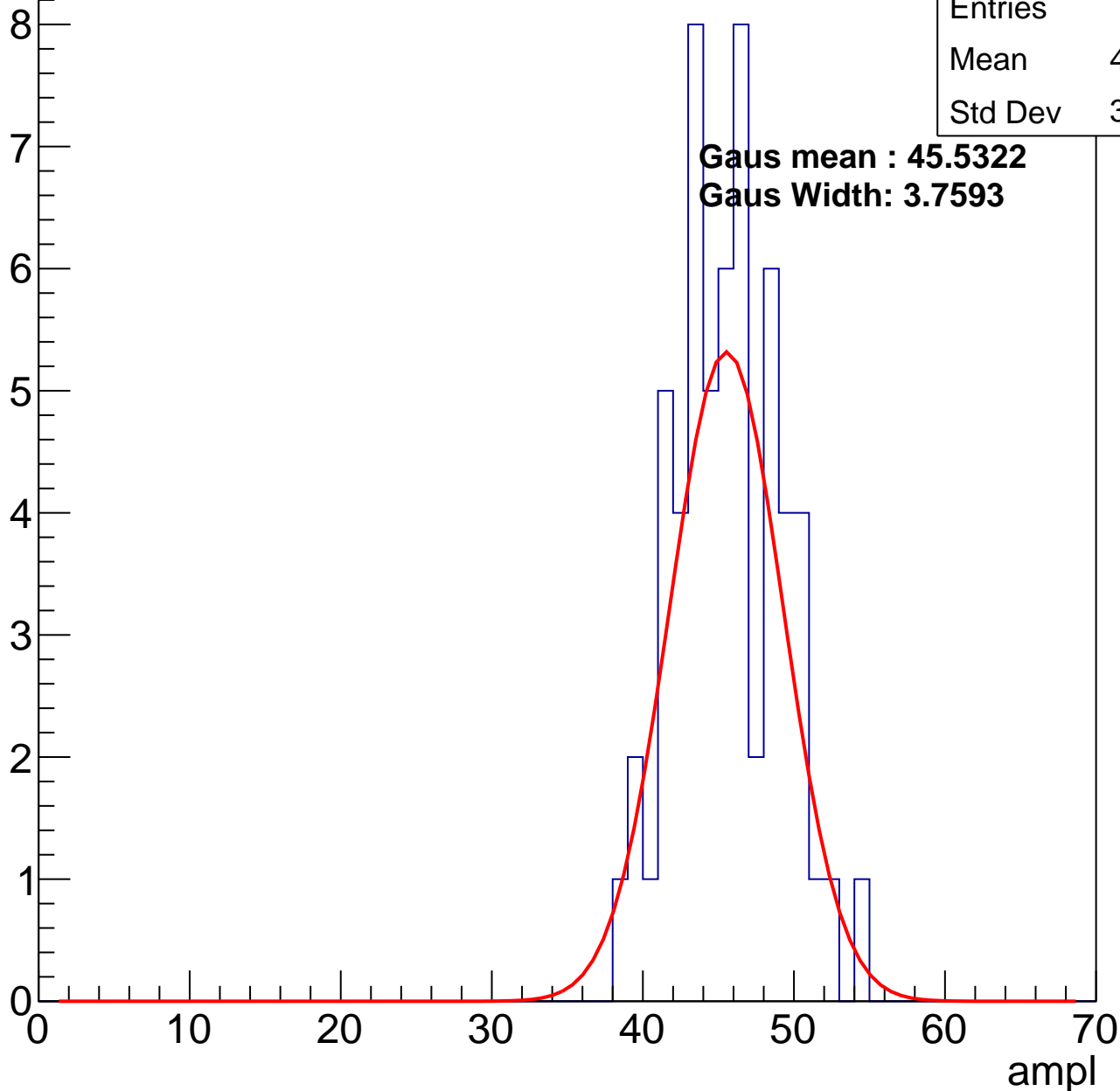
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 59    |
| Mean    | 45.19 |
| Std Dev | 3.437 |

**Gaus mean : 45.5322**

**Gaus Width: 3.7593**

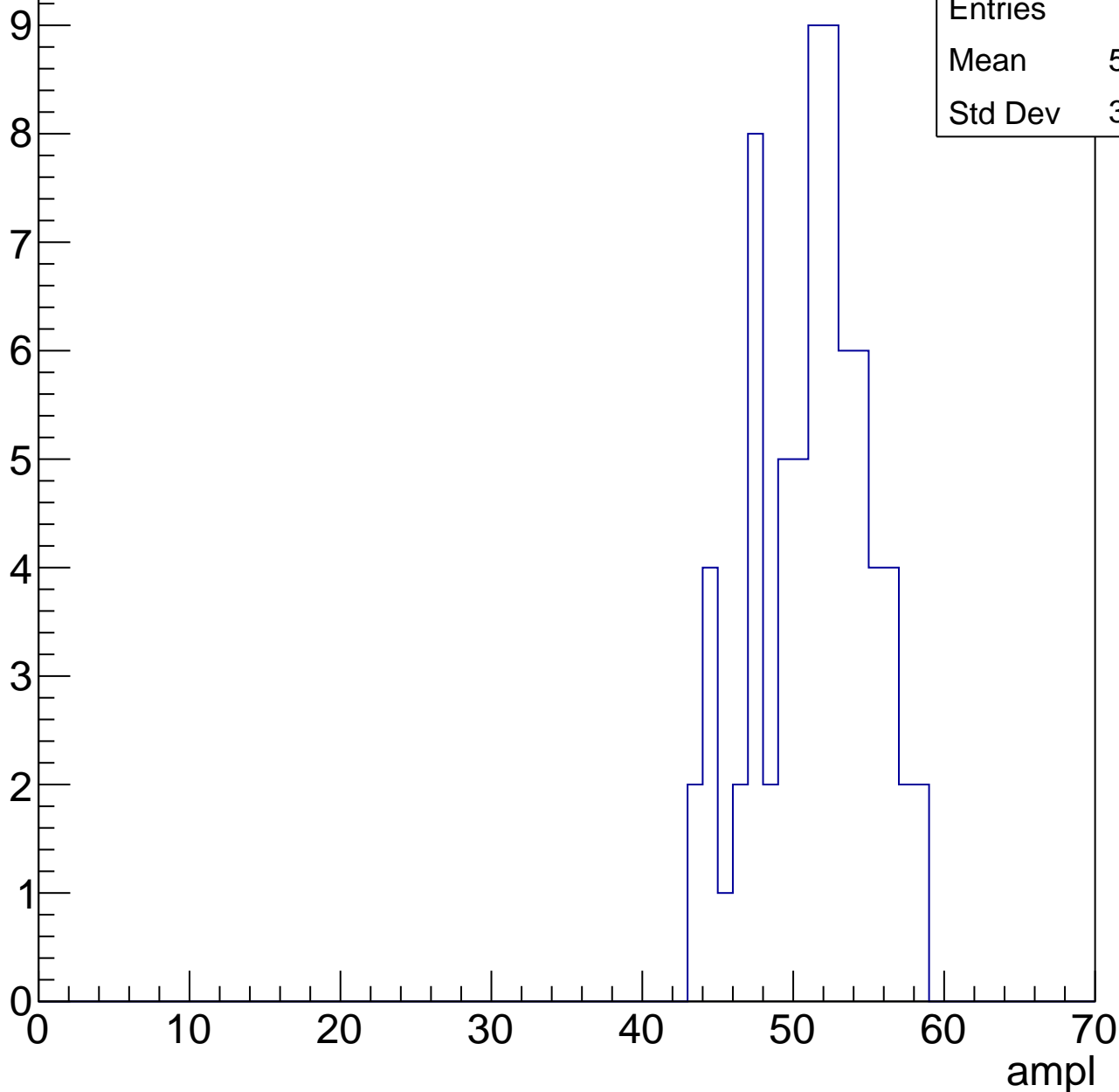


# B0L001S, U2-ch52, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 71    |
| Mean    | 50.83 |
| Std Dev | 3.753 |

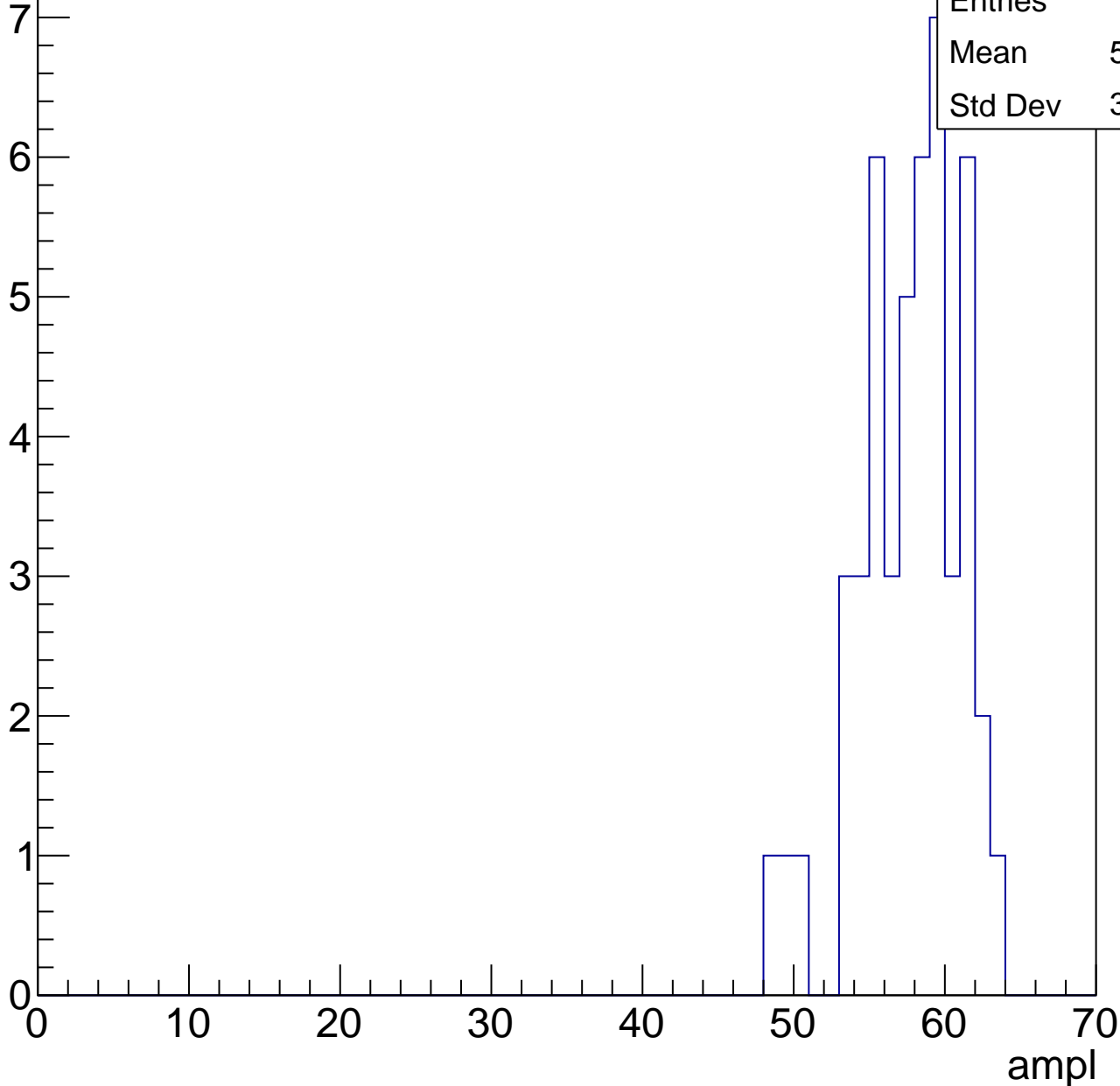


# B0L001S, U2-ch52, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

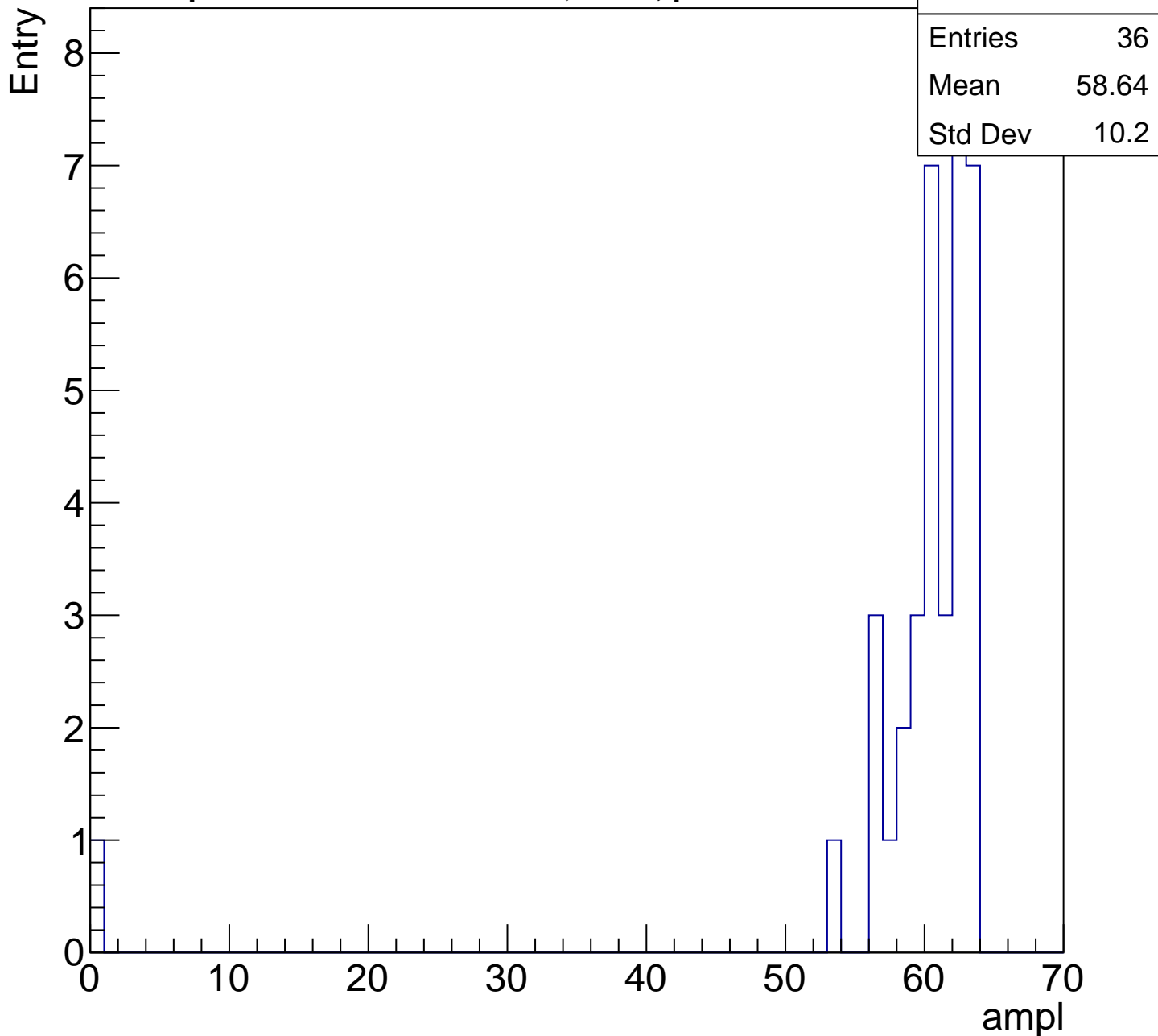
Entry

|         |       |
|---------|-------|
| Entries | 48    |
| Mean    | 57.19 |
| Std Dev | 3.346 |



# B0L001S, U2-ch52, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U2-ch52, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

|         |       |
|---------|-------|
| Entries | 4     |
| Mean    | 61    |
| Std Dev | 2.449 |

ampl

0 10 20 30 40 50 60 70



# B0L001S, U2-ch52, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 0 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch53, adc0

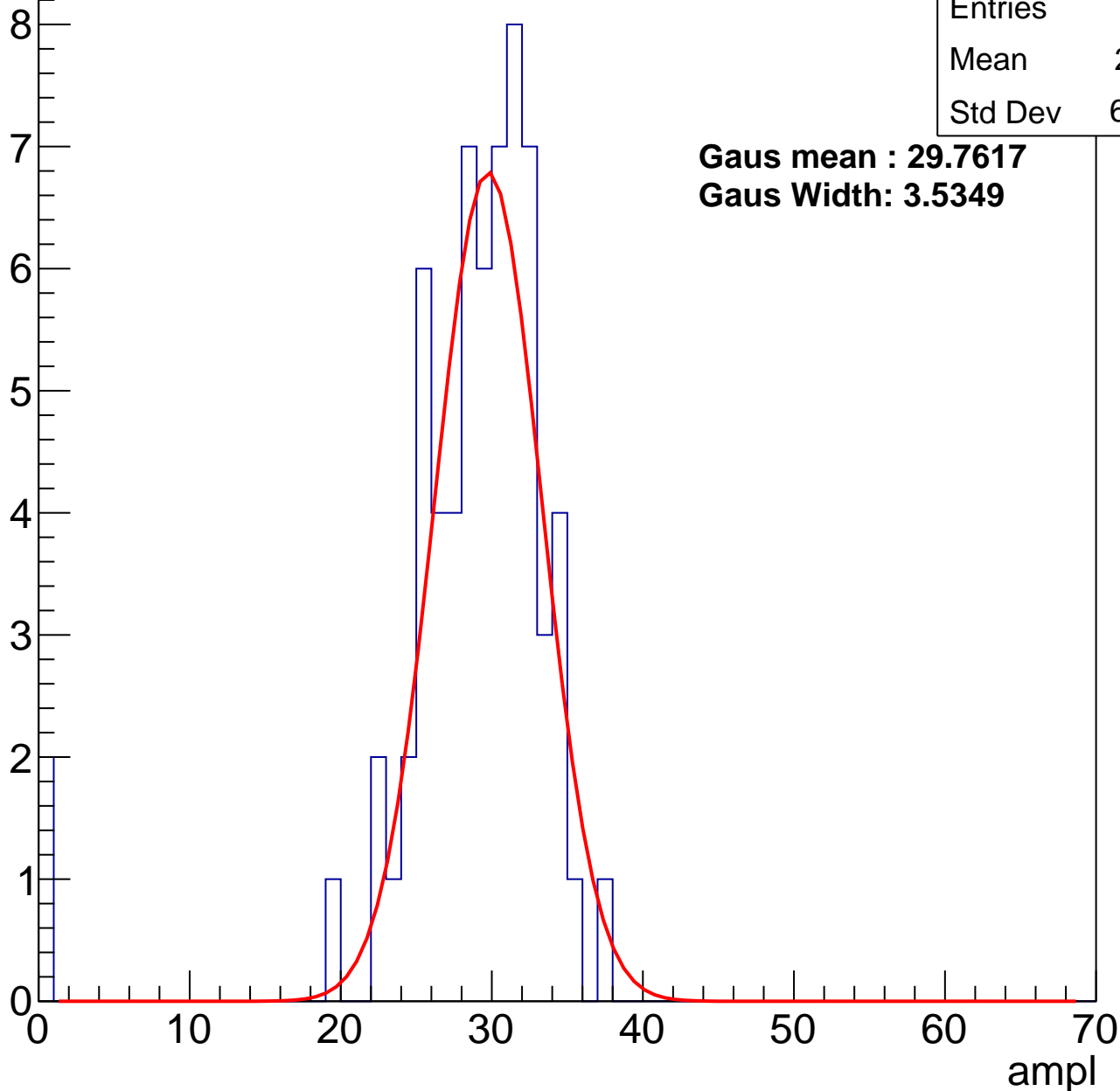
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 66    |
| Mean    | 28.11 |
| Std Dev | 6.053 |

**Gaus mean : 29.7617**

**Gaus Width: 3.5349**



# B0L001S, U2-ch53, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 64    |
| Mean    | 35.66 |
| Std Dev | 3.088 |

**Gaus mean : 36.0357**

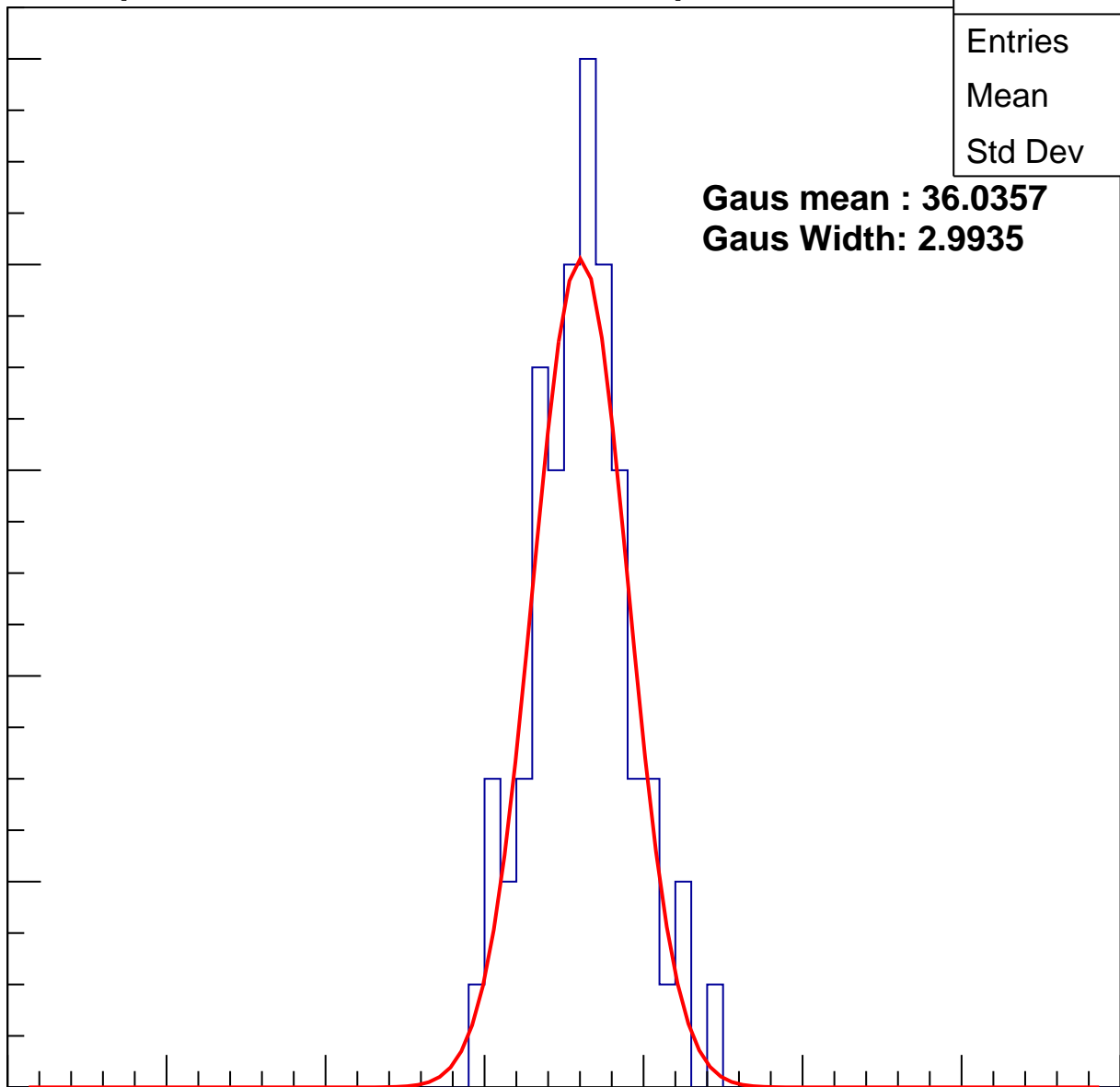
**Gaus Width: 2.9935**

Entry

10  
8  
6  
4  
2  
0

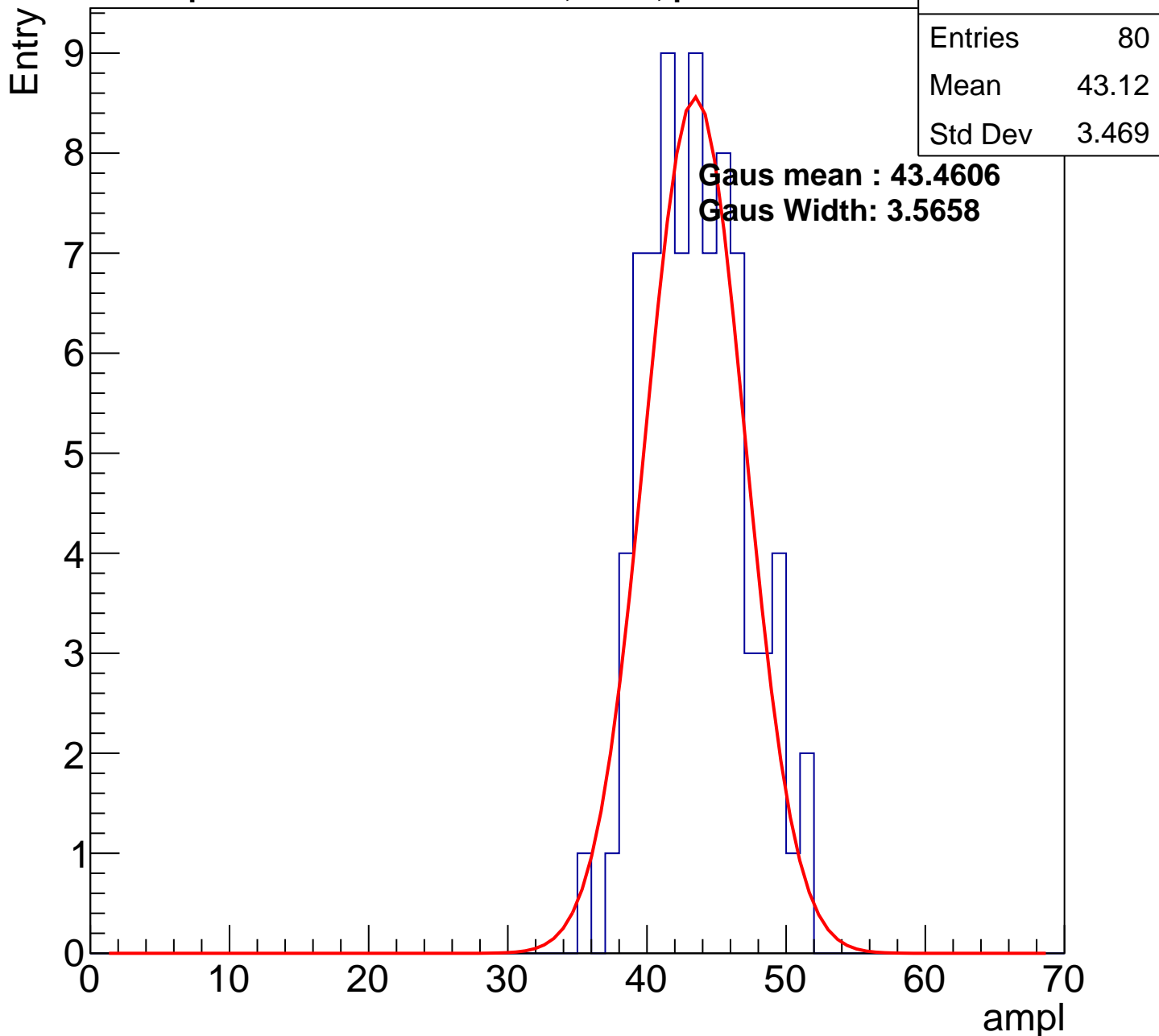
0 10 20 30 40 50 60 70

ampl



# B0L001S, U2-ch53, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

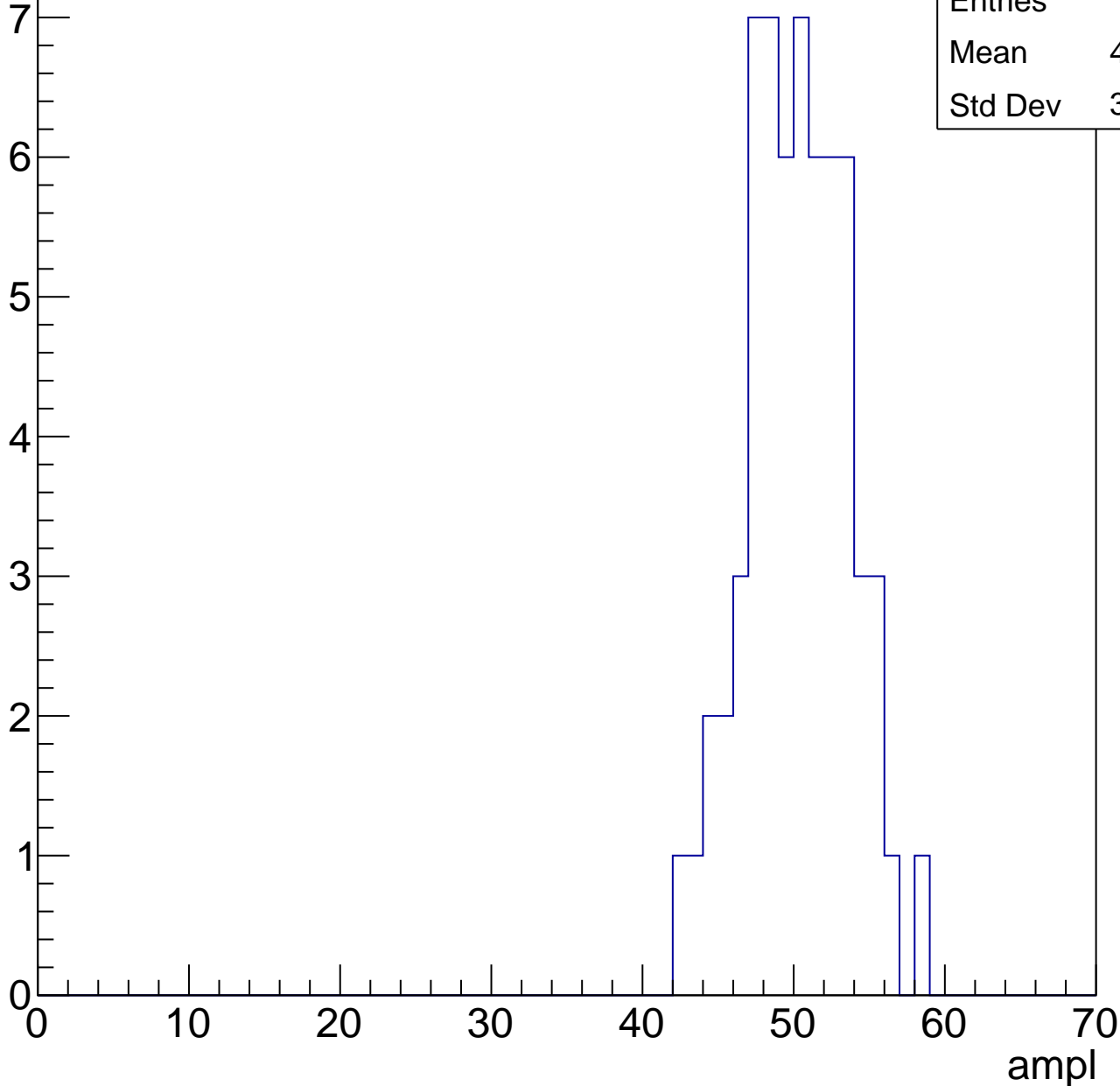


# B0L001S, U2-ch53, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 62    |
| Mean    | 49.79 |
| Std Dev | 3.322 |

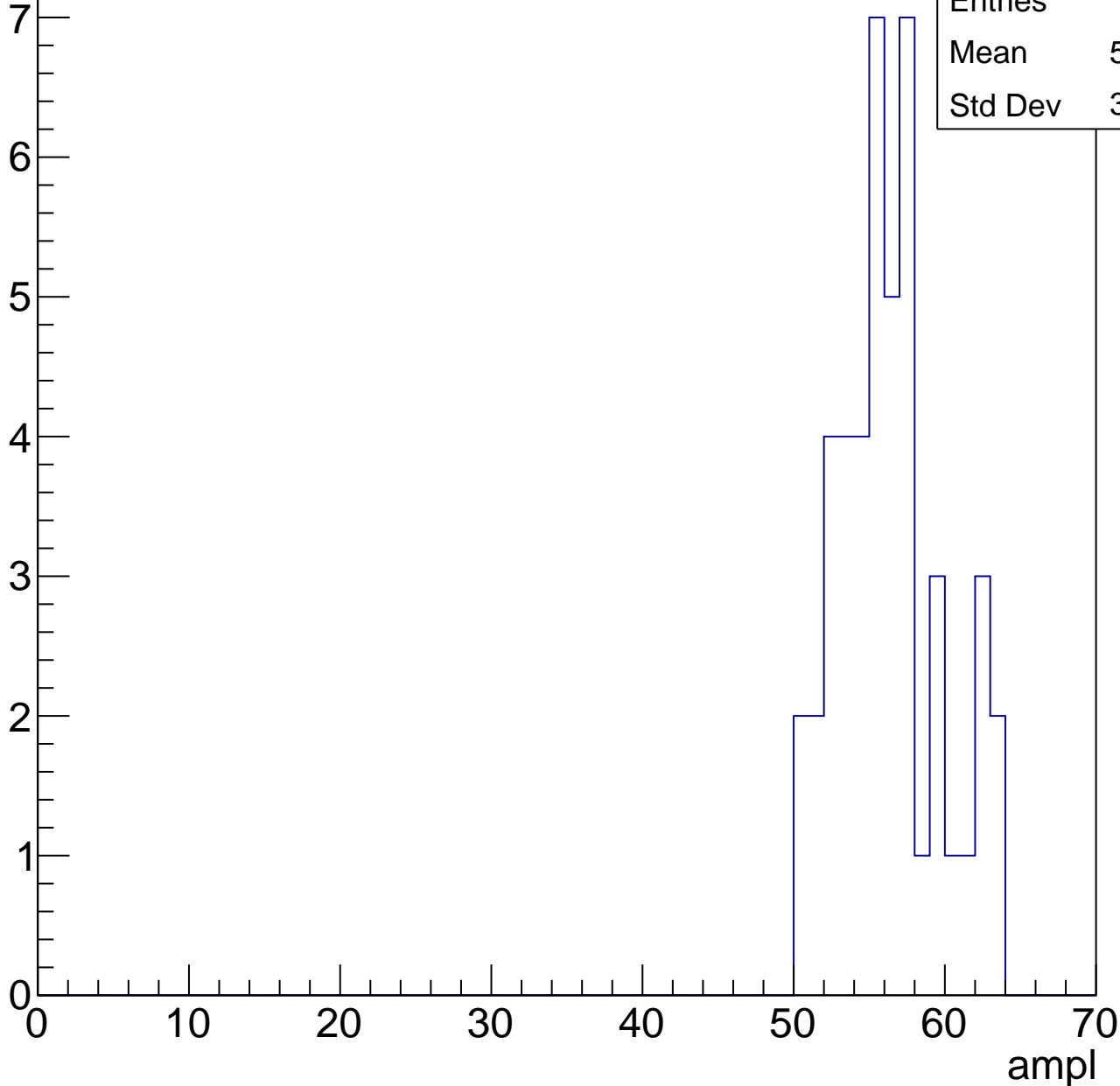


# B0L001S, U2-ch53, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 46    |
| Mean    | 55.87 |
| Std Dev | 3.392 |

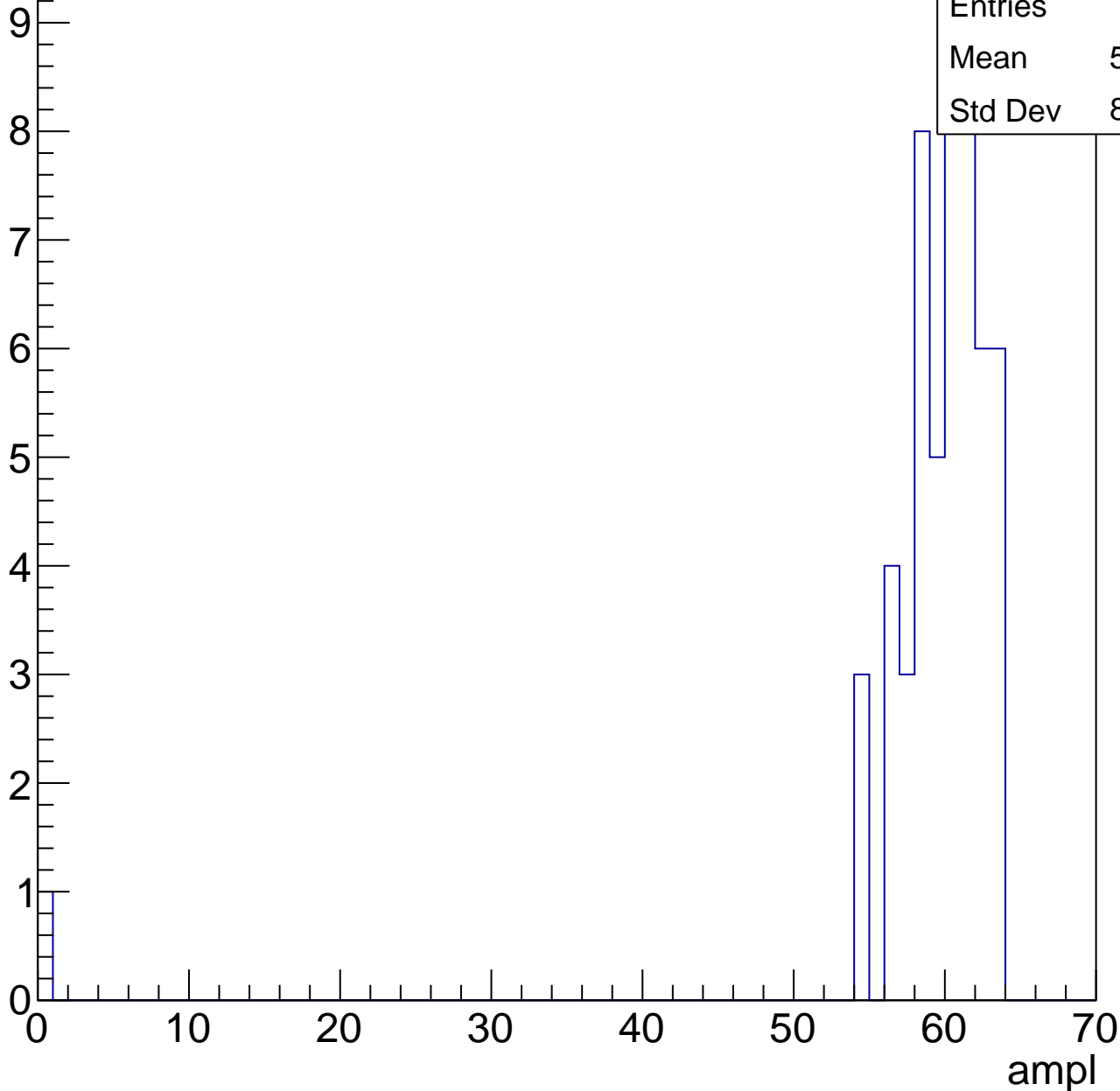


# B0L001S, U2-ch53, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

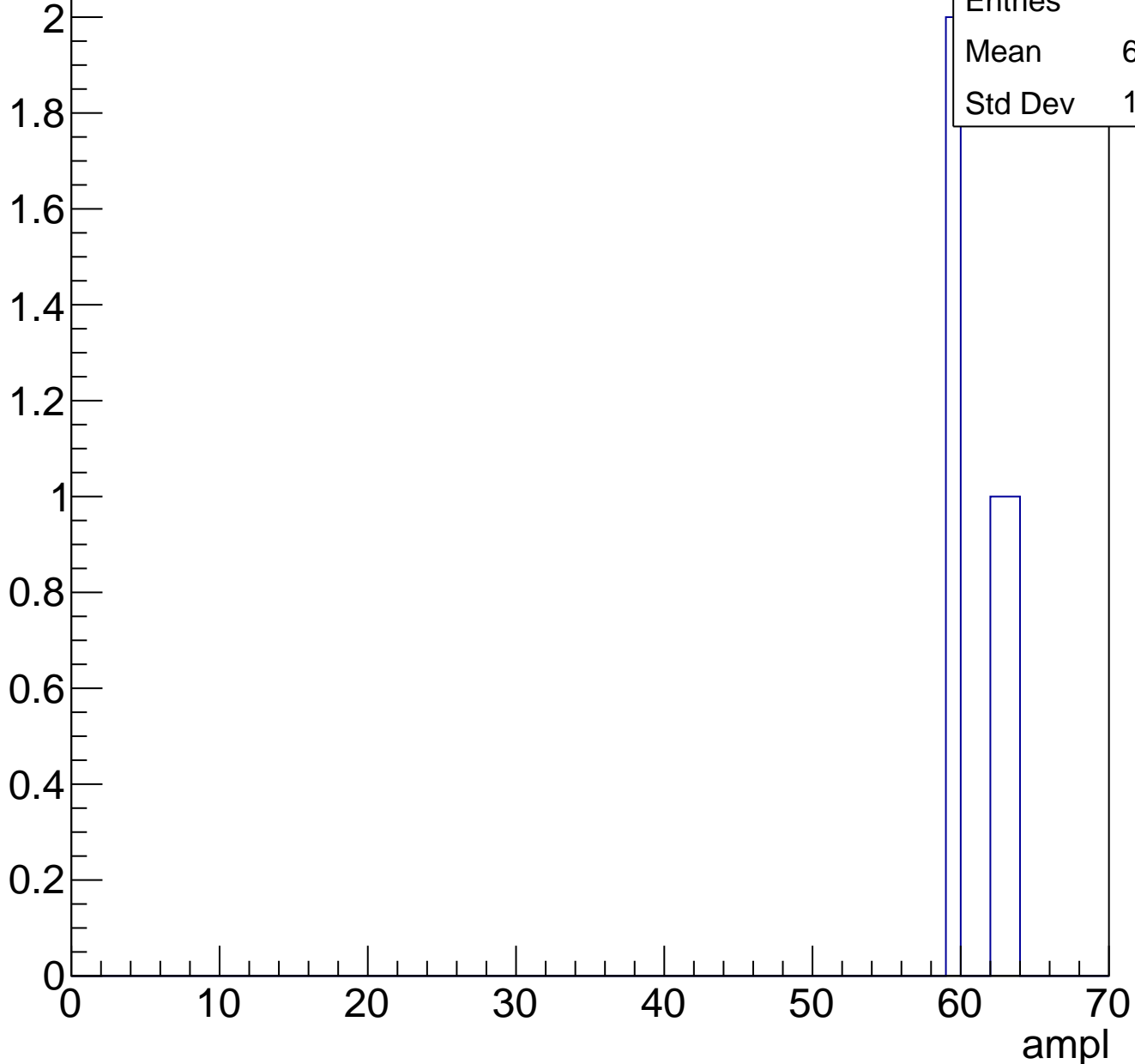
|         |       |
|---------|-------|
| Entries | 54    |
| Mean    | 58.43 |
| Std Dev | 8.377 |



# B0L001S, U2-ch53, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |       |
|---------|-------|
| Entries | 4     |
| Mean    | 60.75 |
| Std Dev | 1.785 |



# B0L001S, U2-ch53, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U2-ch54, adc0

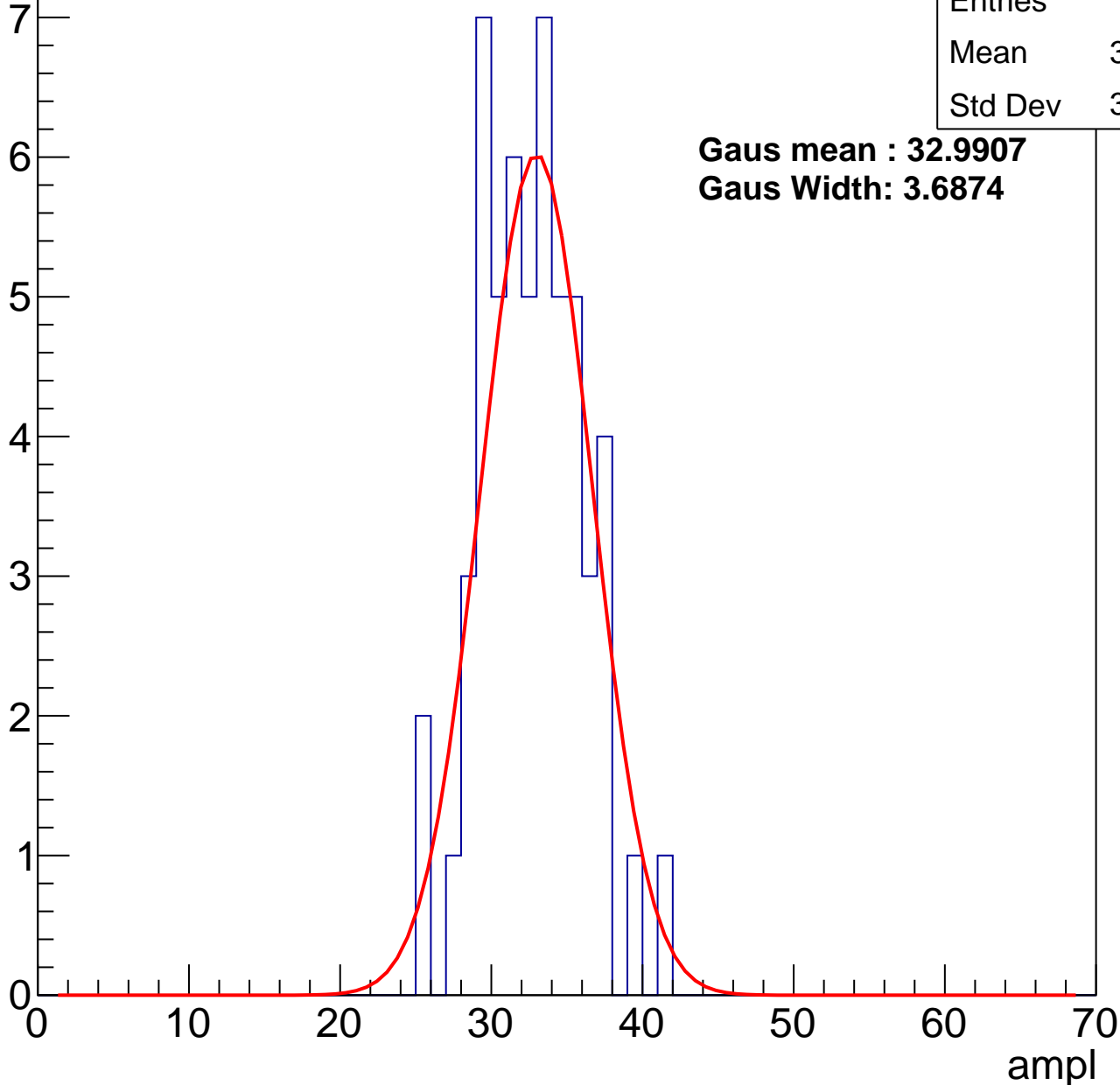
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 55    |
| Mean    | 32.22 |
| Std Dev | 3.323 |

**Gaus mean : 32.9907**

**Gaus Width: 3.6874**



# B0L001S, U2-ch54, adc1

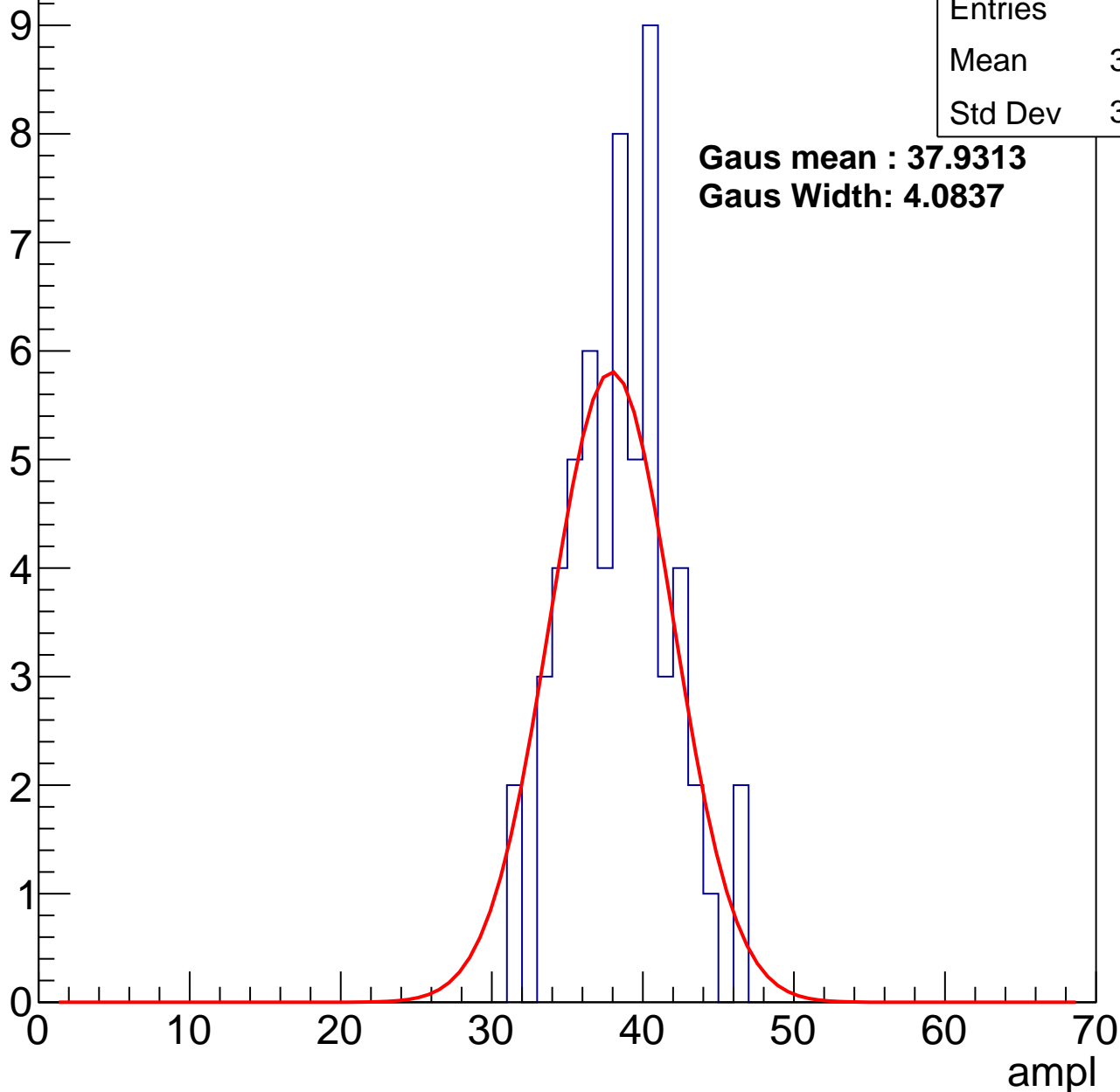
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 58    |
| Mean    | 38.07 |
| Std Dev | 3.362 |

**Gaus mean : 37.9313**

**Gaus Width: 4.0837**



# B0L001S, U2-ch54, adc2

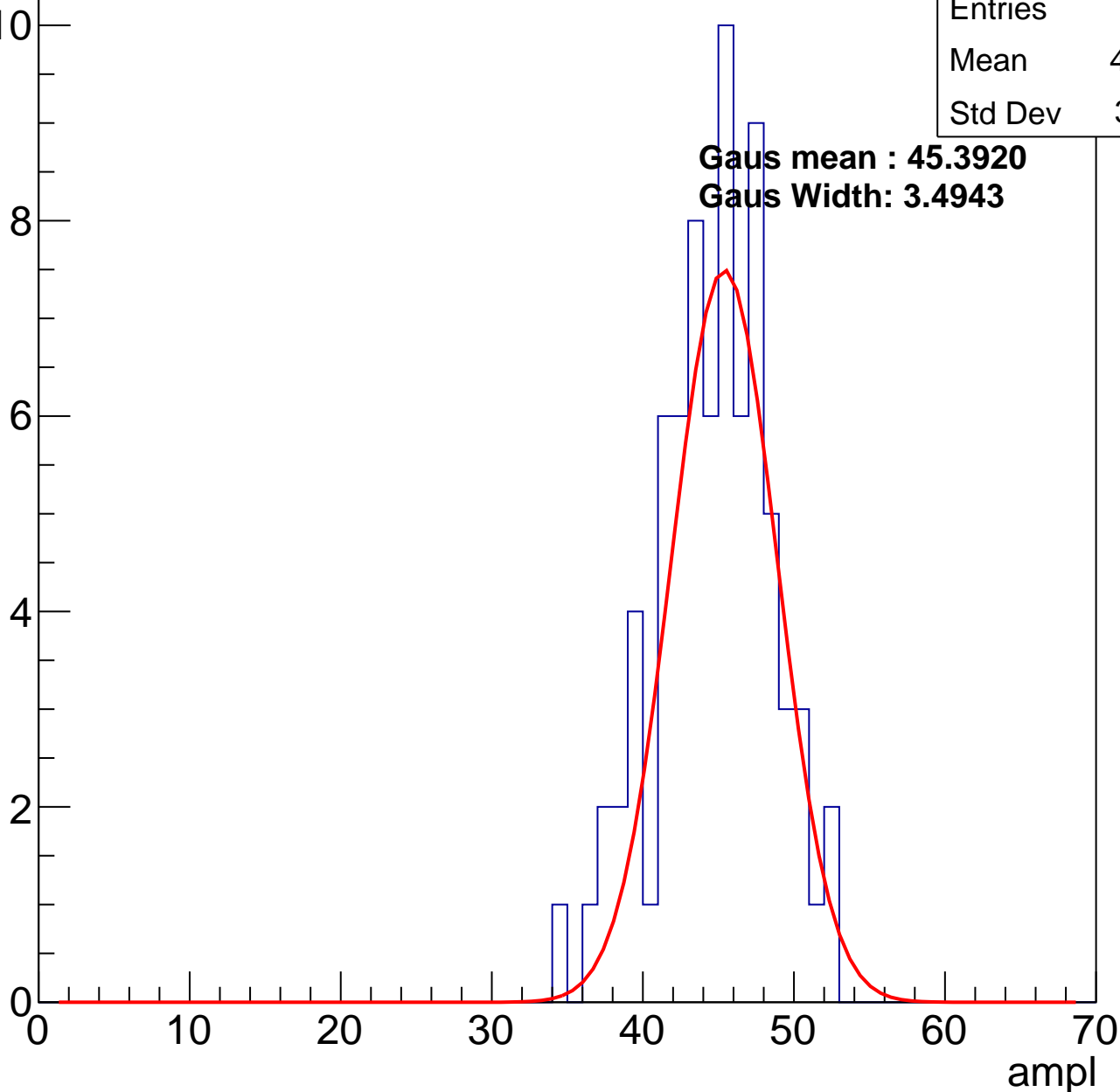
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 76    |
| Mean    | 44.25 |
| Std Dev | 3.781 |

**Gaus mean : 45.3920**

**Gaus Width: 3.4943**

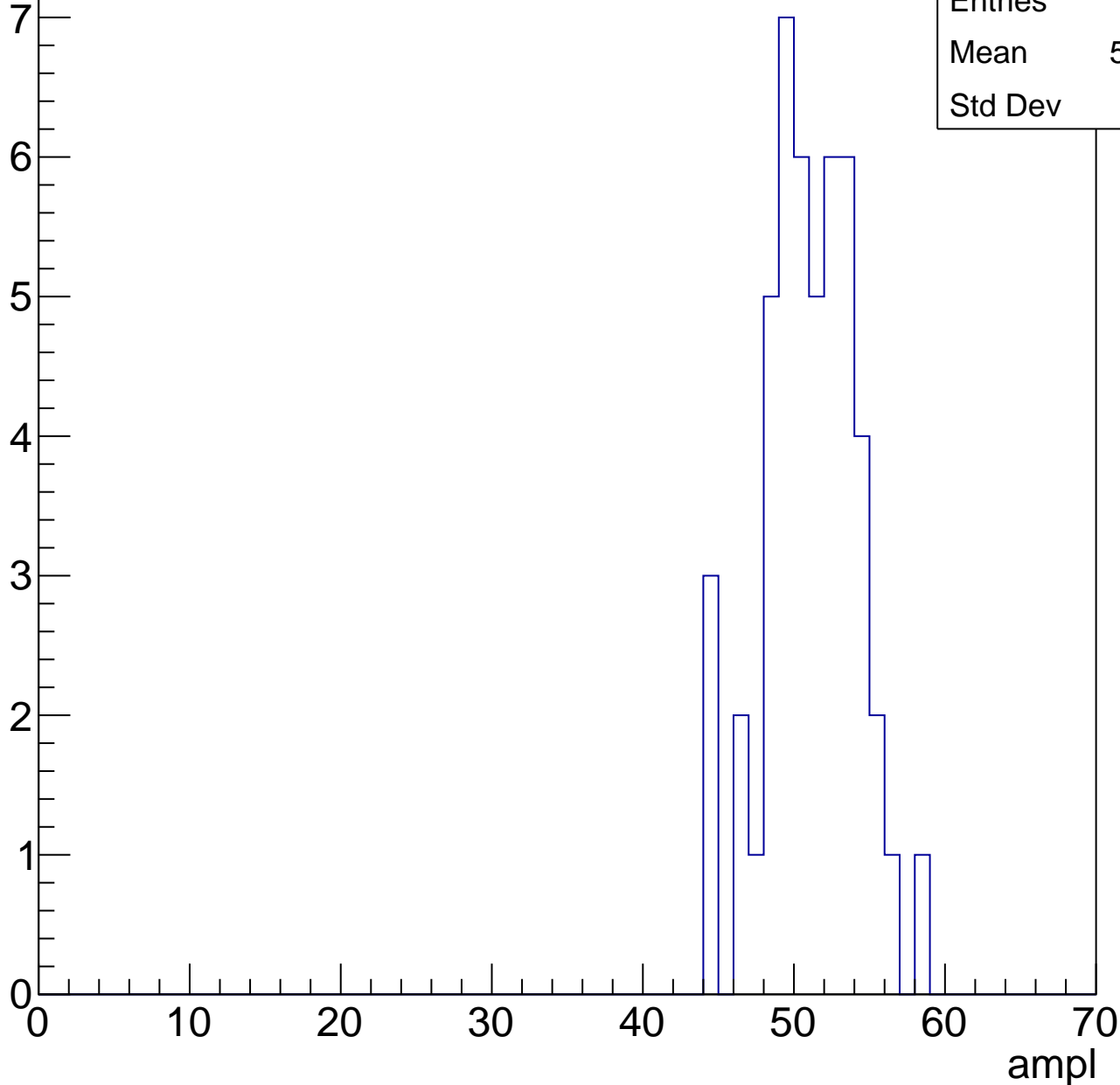


# B0L001S, U2-ch54, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

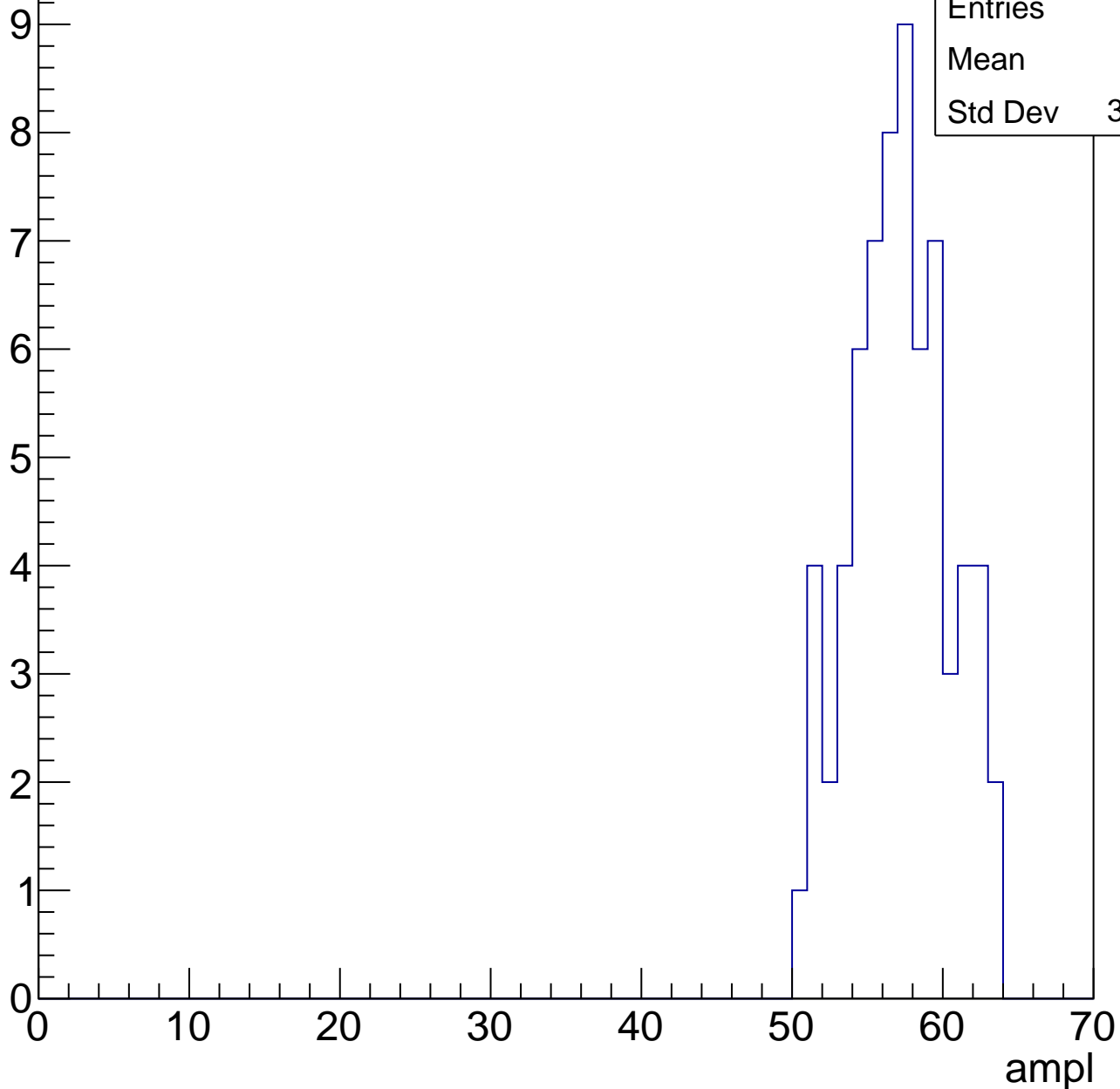
|         |       |
|---------|-------|
| Entries | 49    |
| Mean    | 50.59 |
| Std Dev | 3.05  |



# B0L001S, U2-ch54, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

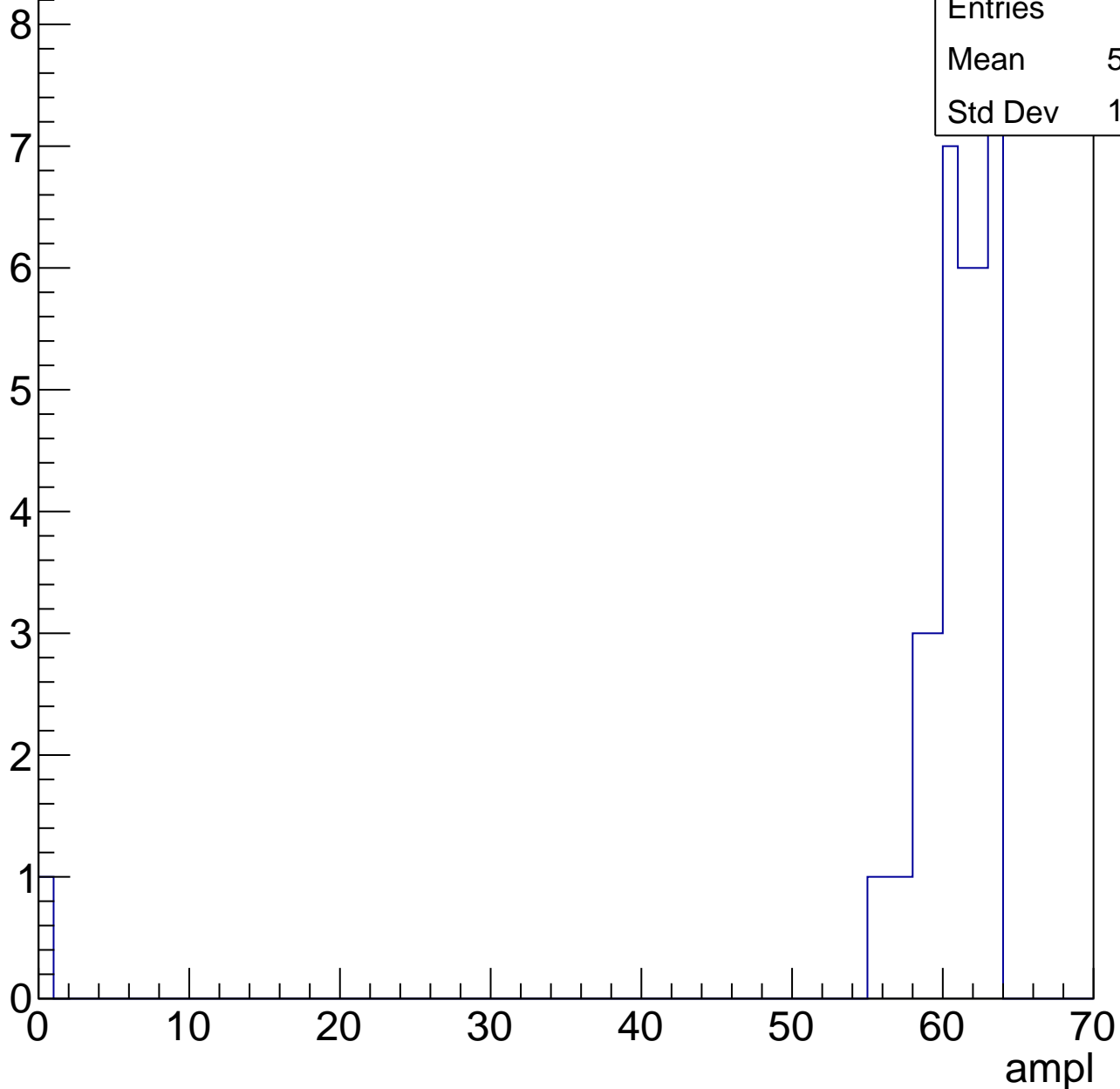
Entry



# B0L001S, U2-ch54, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U2-ch54, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 0 |
| Mean    | 0 |
| Std Dev | 0 |



# B0L001S, U2-ch54, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 2 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch55, adc0

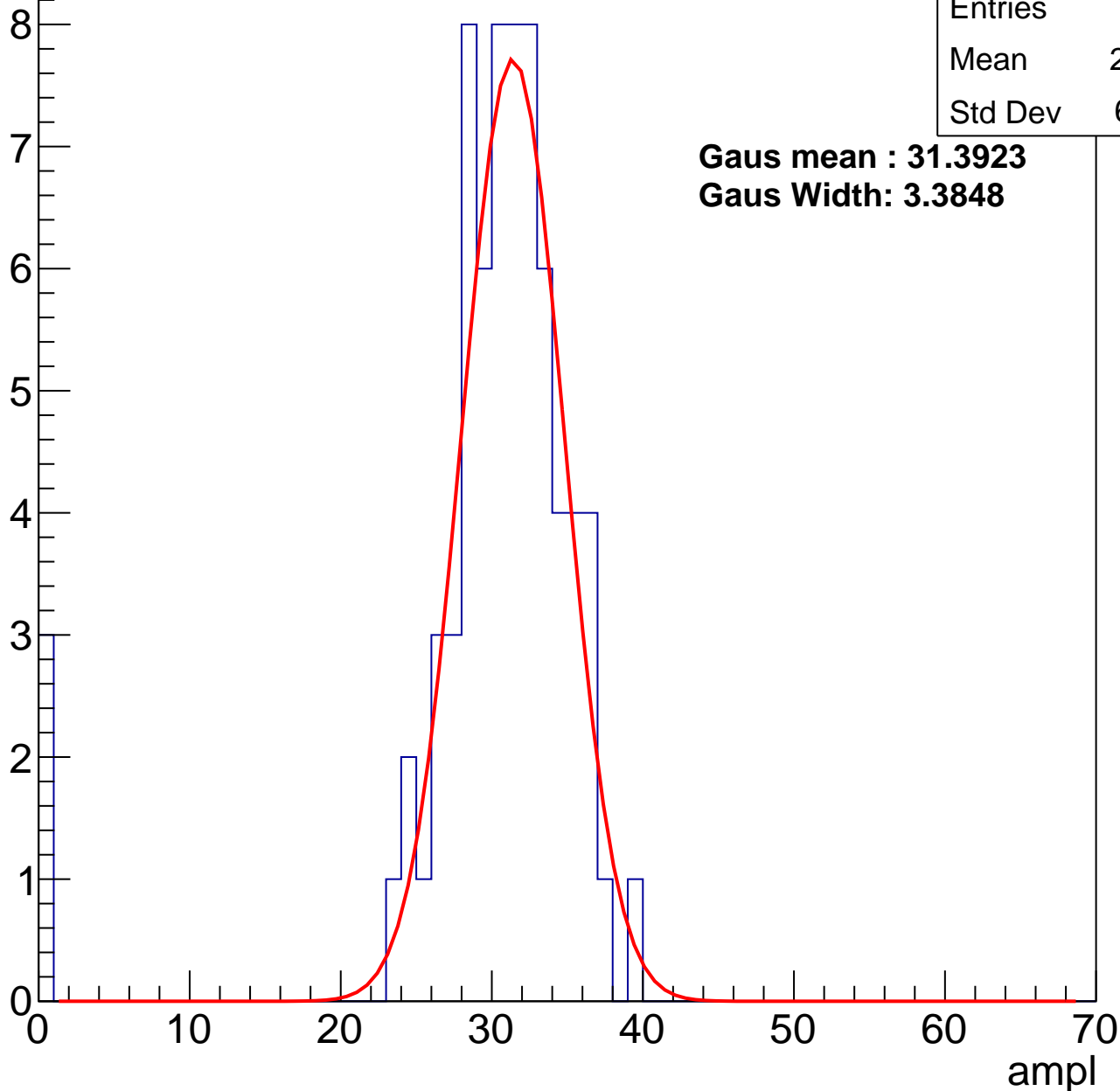
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 71    |
| Mean    | 29.45 |
| Std Dev | 6.991 |

**Gaus mean : 31.3923**

**Gaus Width: 3.3848**



# B0L001S, U2-ch55, adc1

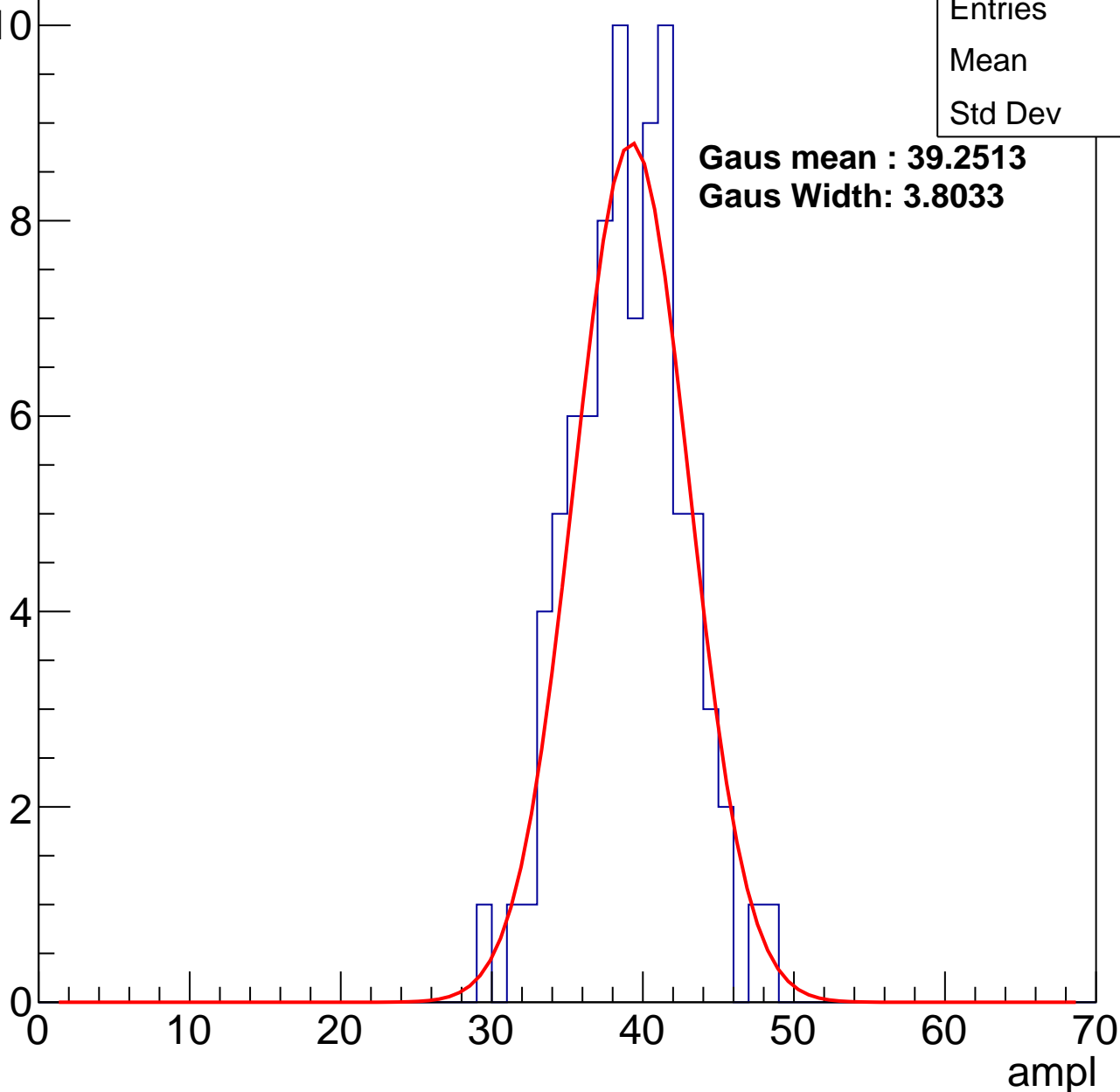
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |      |
|---------|------|
| Entries | 85   |
| Mean    | 38.6 |
| Std Dev | 3.64 |

**Gaus mean : 39.2513**

**Gaus Width: 3.8033**



# B0L001S, U2-ch55, adc2

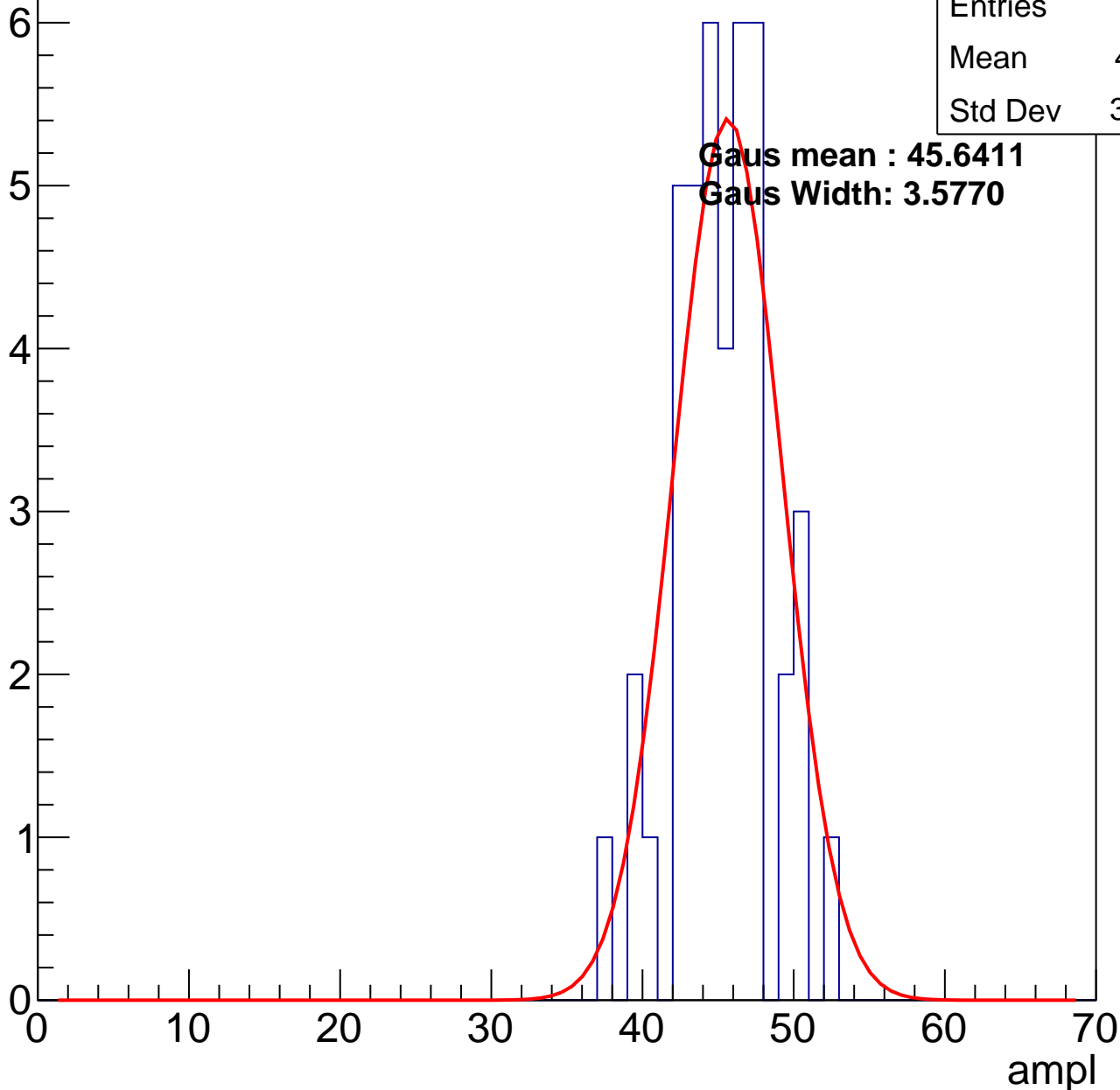
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 42    |
| Mean    | 44.81 |
| Std Dev | 3.149 |

**Gaus mean : 45.6411**

**Gaus Width: 3.5770**

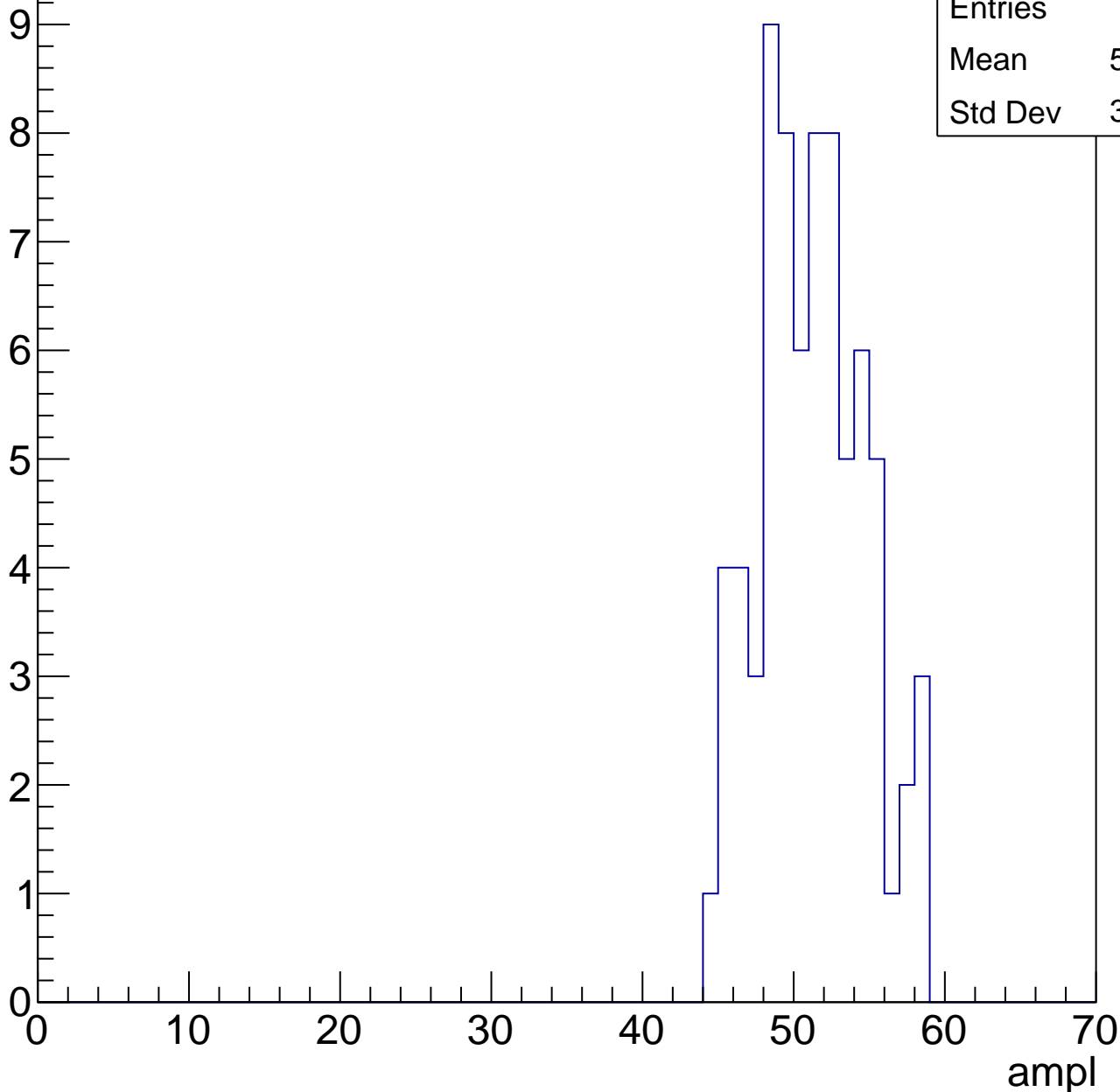


# B0L001S, U2-ch55, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 73    |
| Mean    | 50.75 |
| Std Dev | 3.435 |

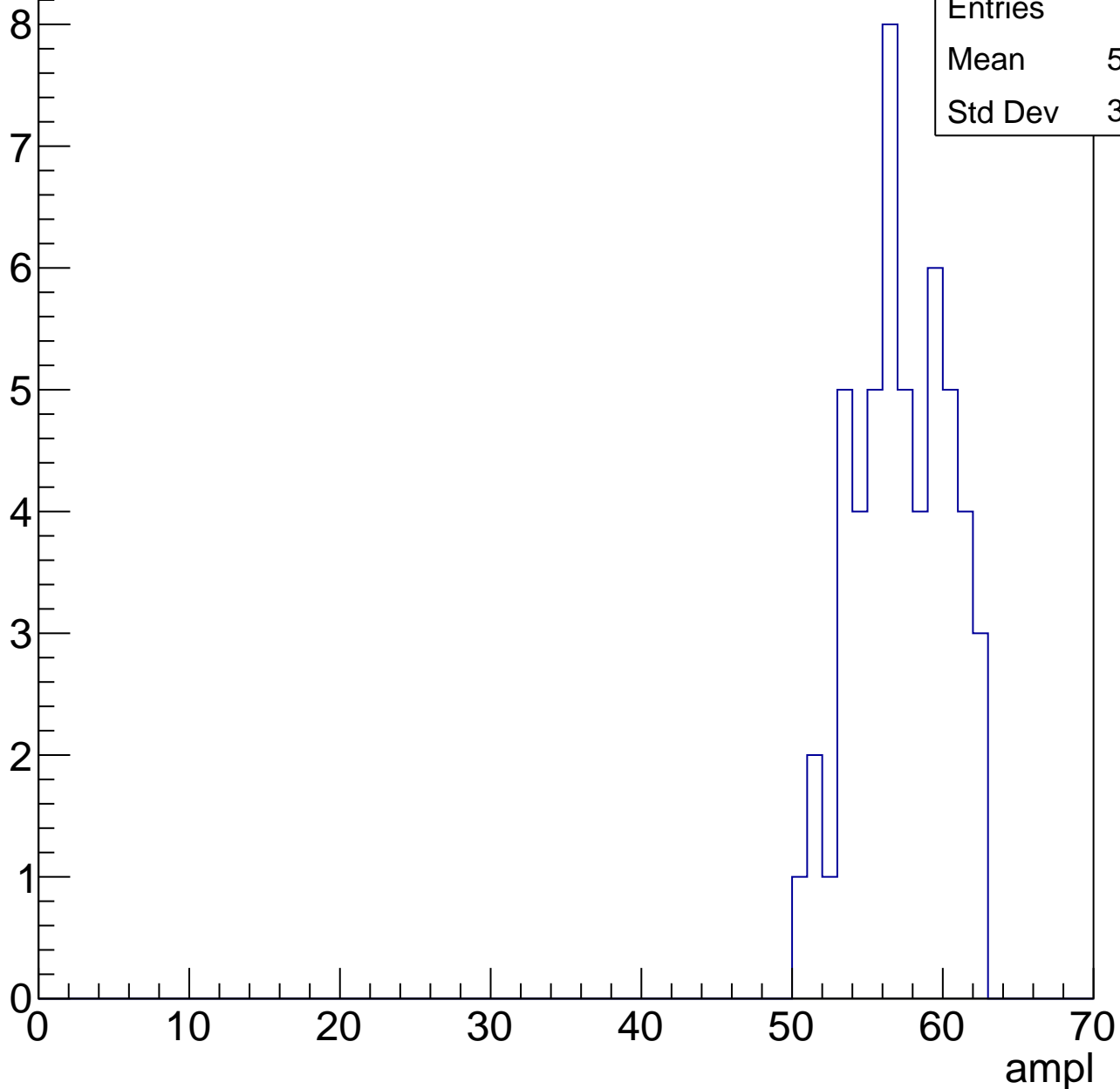


# B0L001S, U2-ch55, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 53    |
| Mean    | 56.77 |
| Std Dev | 3.069 |

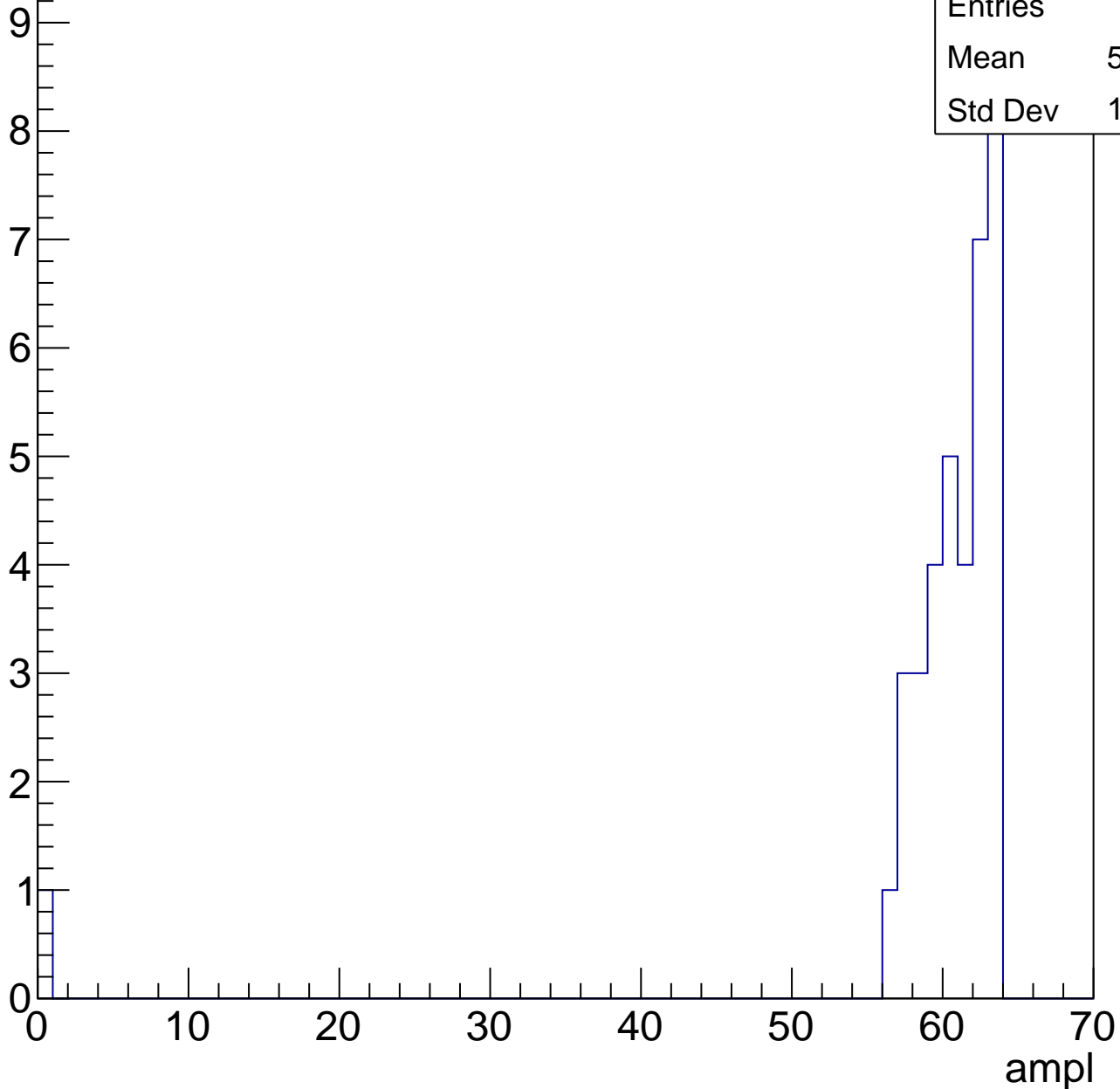


# B0L001S, U2-ch55, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 37    |
| Mean    | 58.97 |
| Std Dev | 10.04 |



# B0L001S, U2-ch55, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch55, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U2-ch56, adc0

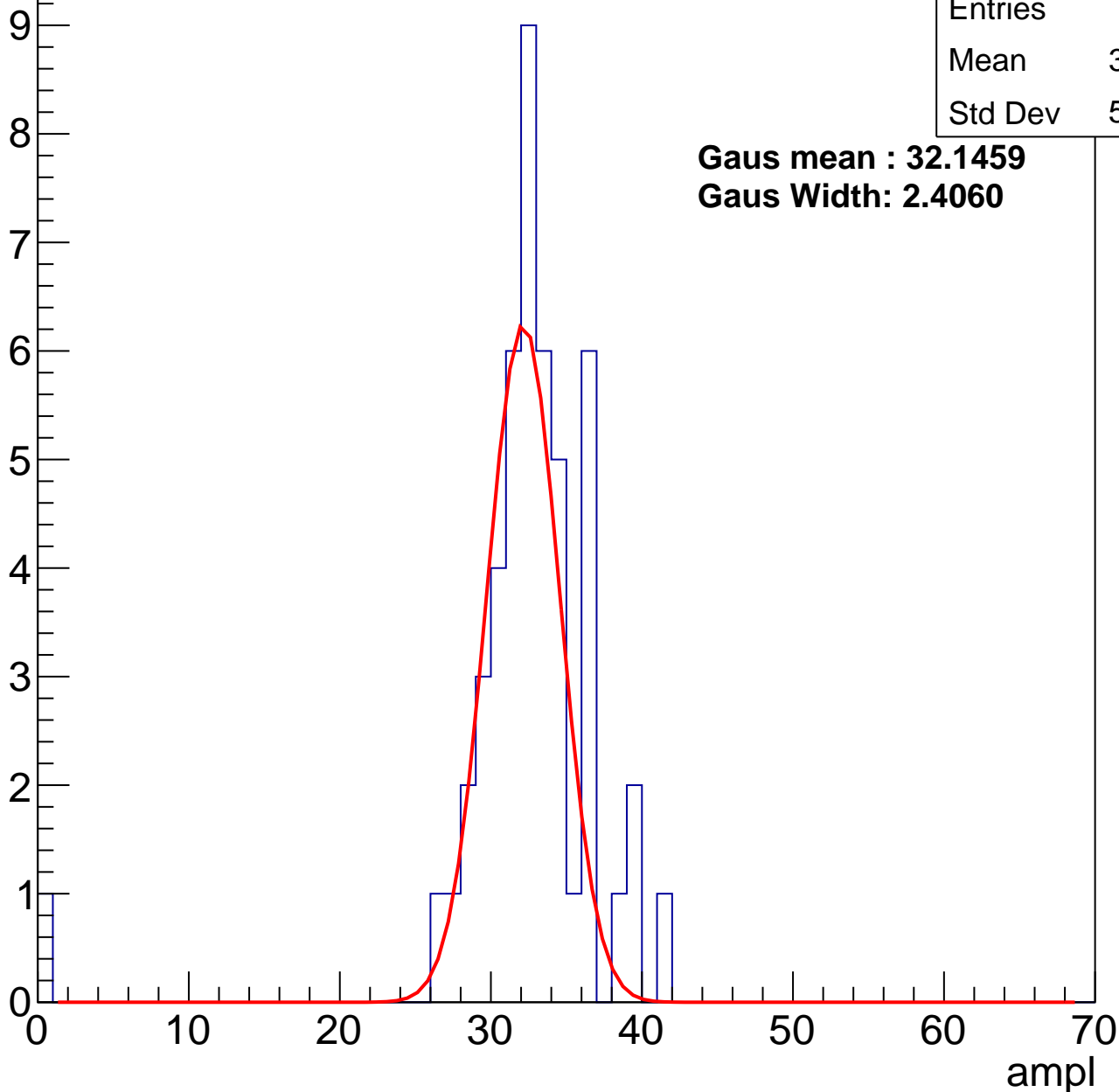
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 49    |
| Mean    | 31.96 |
| Std Dev | 5.555 |

**Gaus mean : 32.1459**

**Gaus Width: 2.4060**



# B0L001S, U2-ch56, adc1

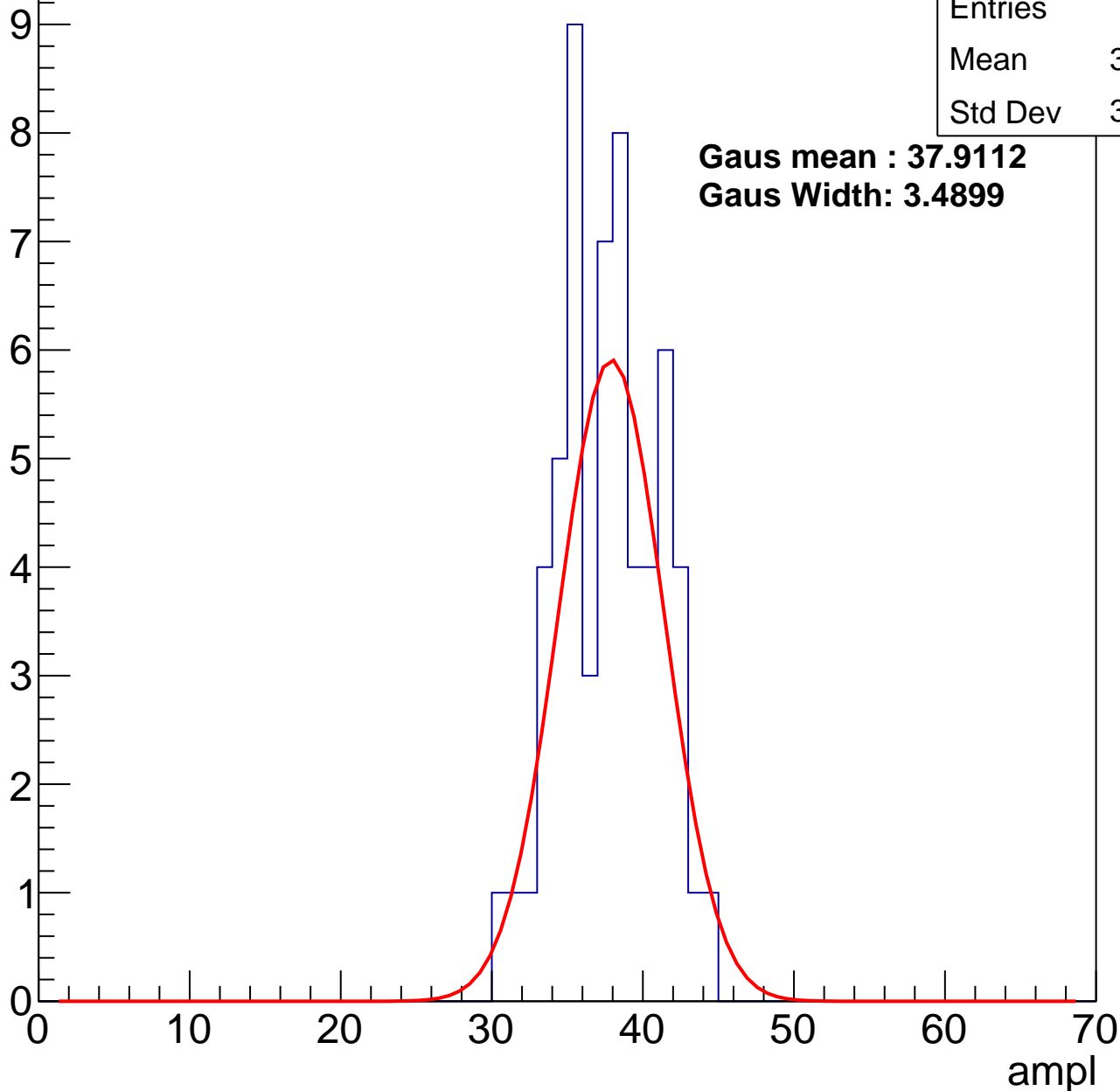
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 59    |
| Mean    | 37.25 |
| Std Dev | 3.176 |

**Gaus mean : 37.9112**

**Gaus Width: 3.4899**



# B0L001S, U2-ch56, adc2

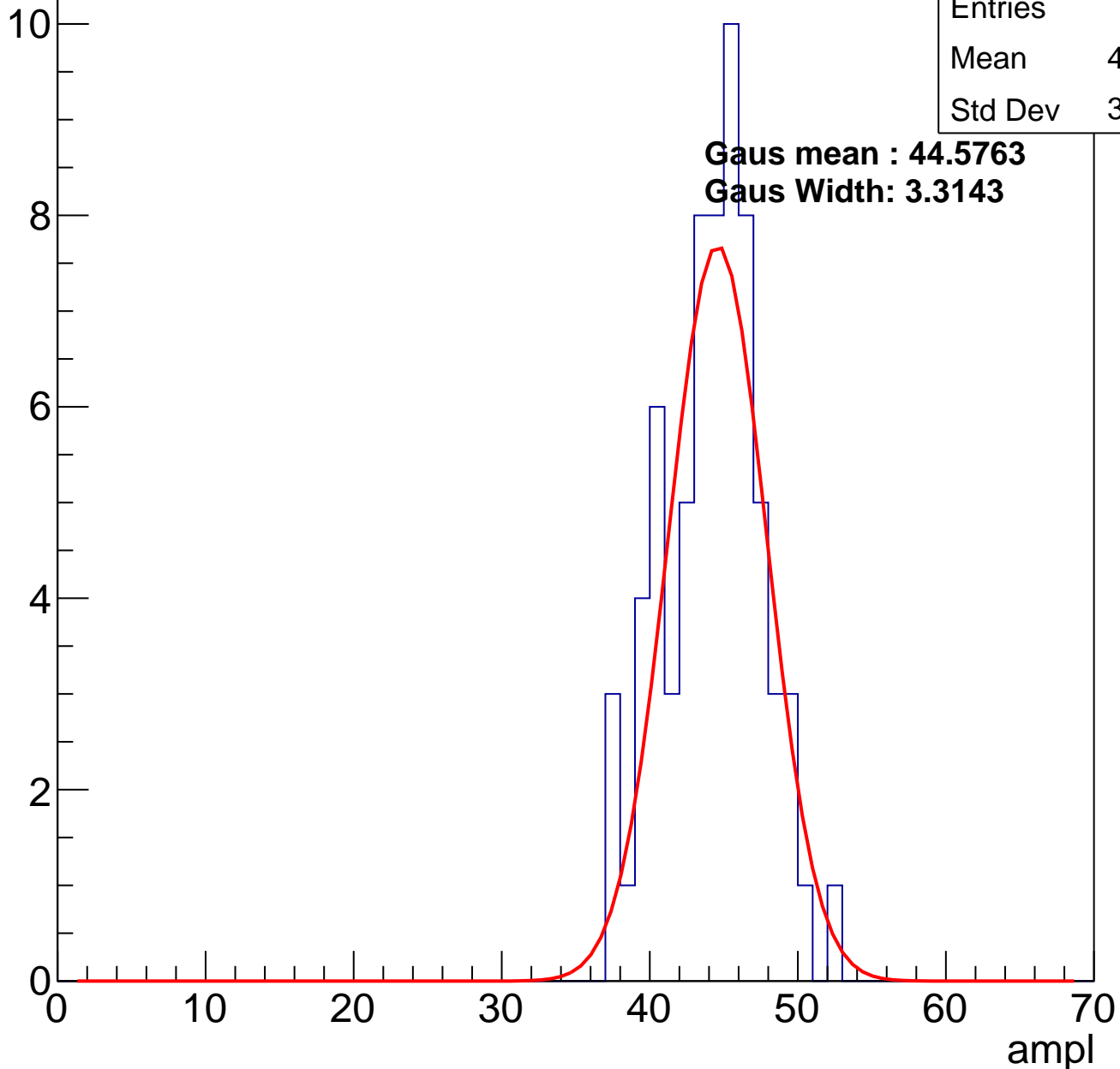
calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 69    |
| Mean    | 43.77 |
| Std Dev | 3.275 |

**Gaus mean : 44.5763**

**Gaus Width: 3.3143**

Entry

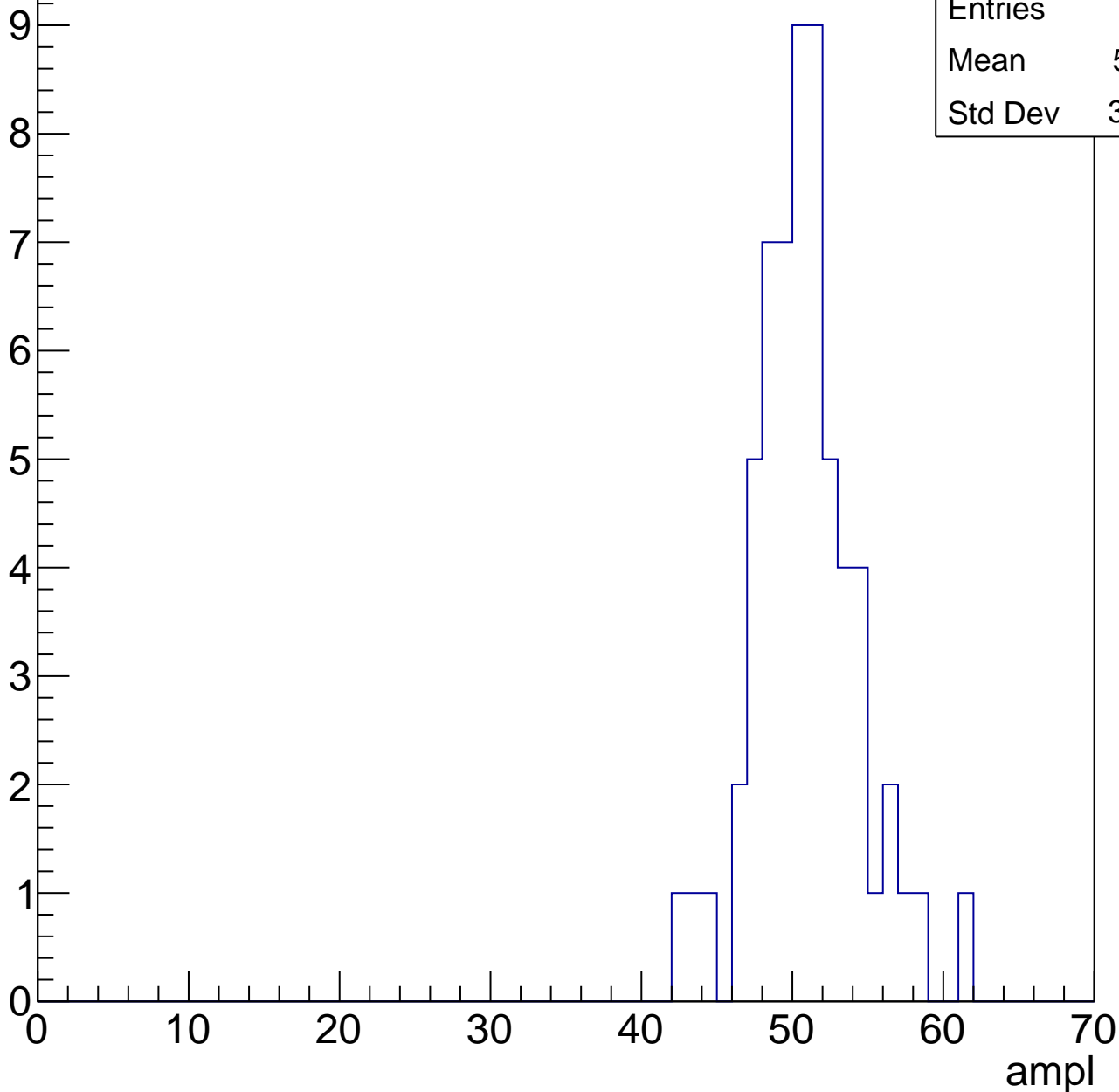


# B0L001S, U2-ch56, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 61    |
| Mean    | 50.41 |
| Std Dev | 3.413 |

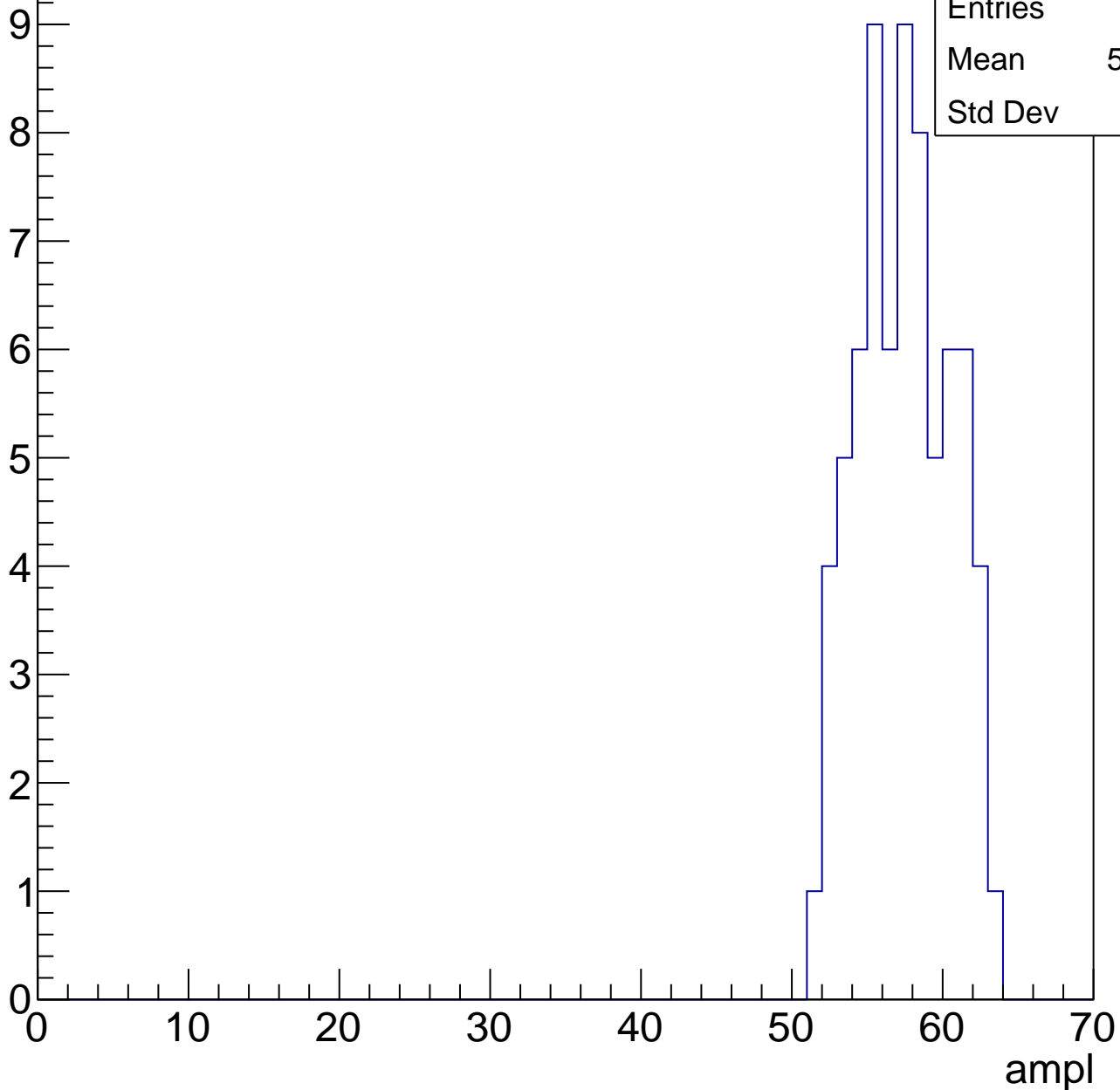


# B0L001S, U2-ch56, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 70    |
| Mean    | 56.97 |
| Std Dev | 2.99  |

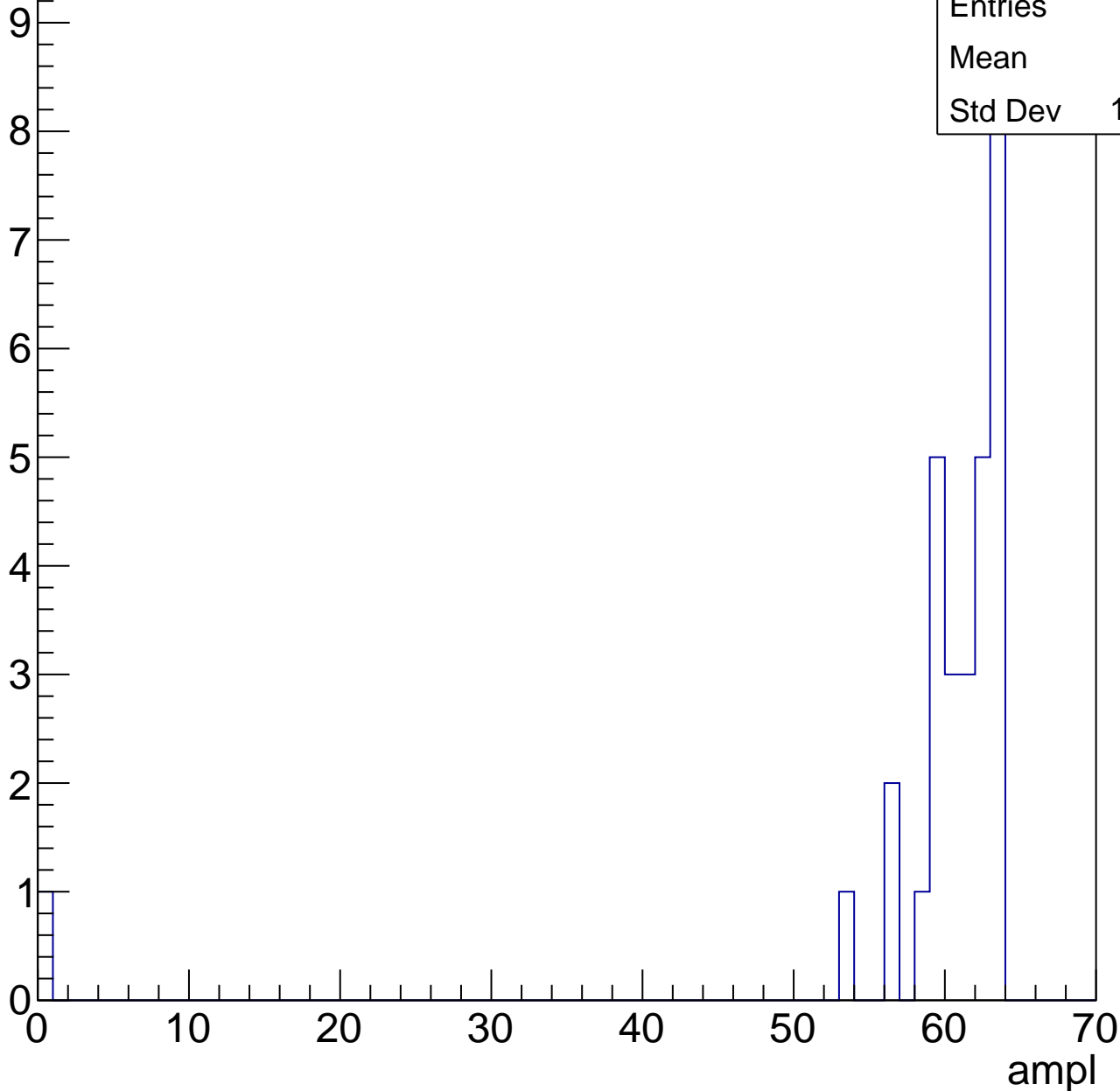


# B0L001S, U2-ch56, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

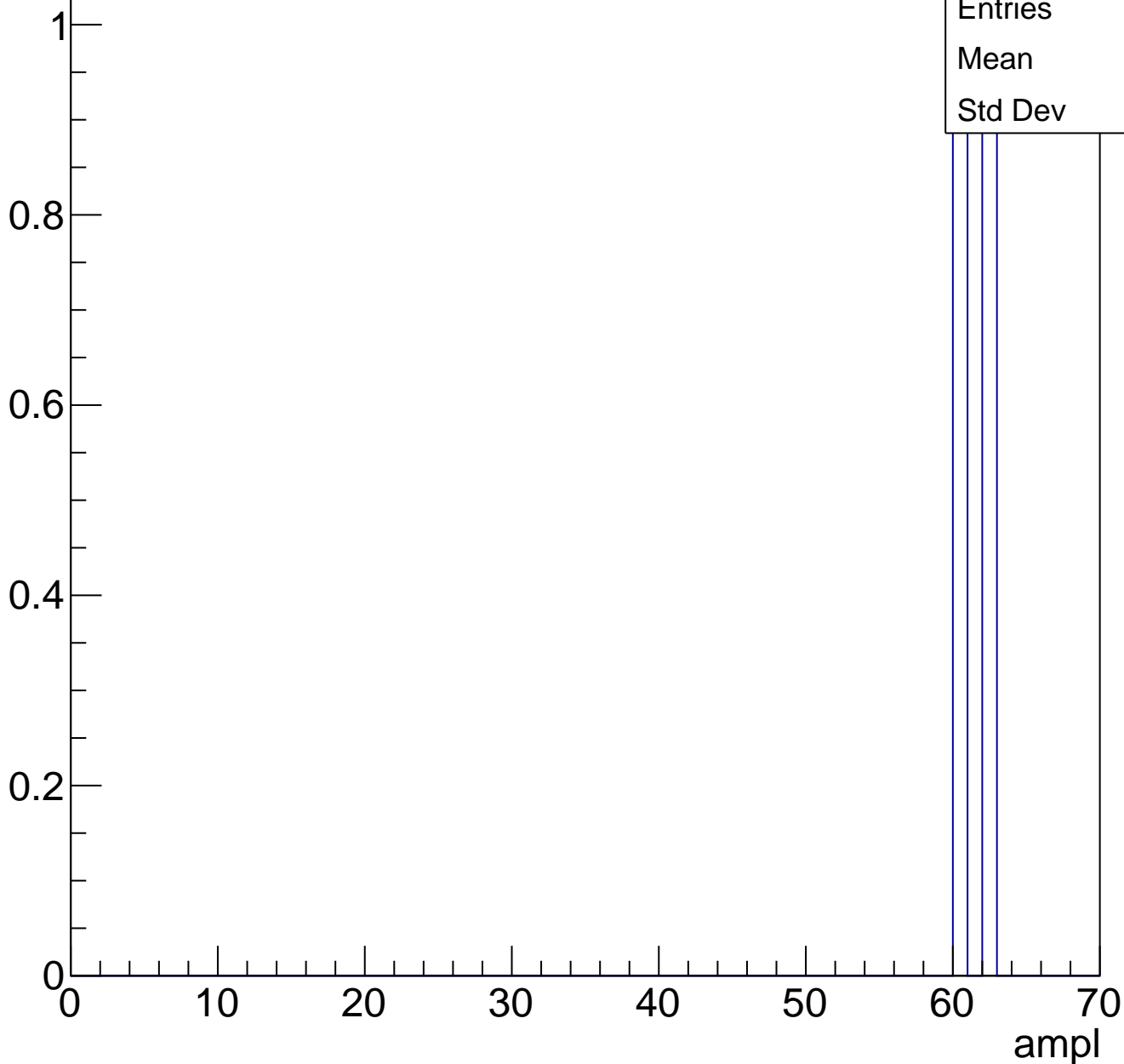
|         |       |
|---------|-------|
| Entries | 30    |
| Mean    | 58.6  |
| Std Dev | 11.16 |



# B0L001S, U2-ch56, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

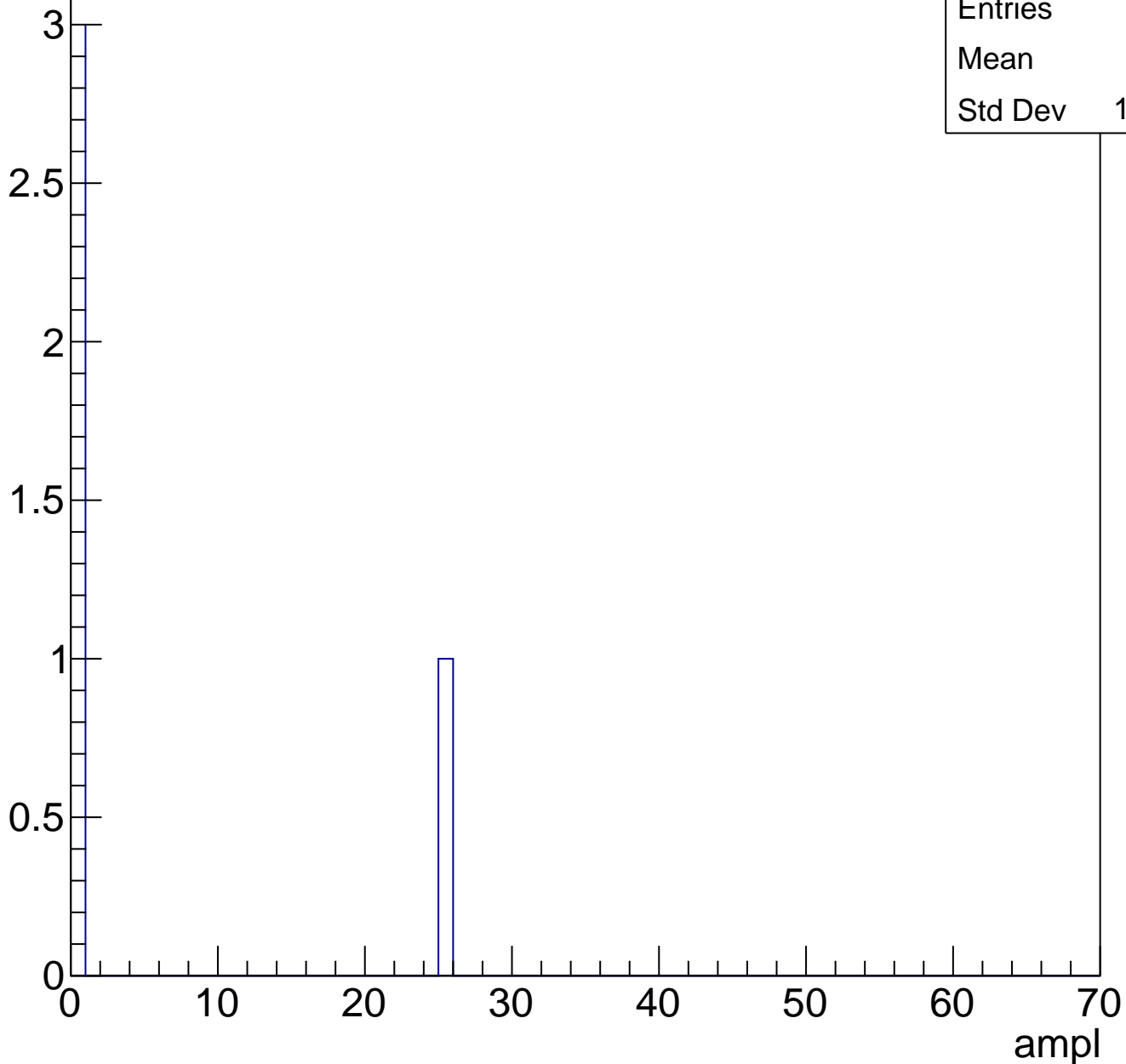




# B0L001S, U2-ch56, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U2-ch57, adc0

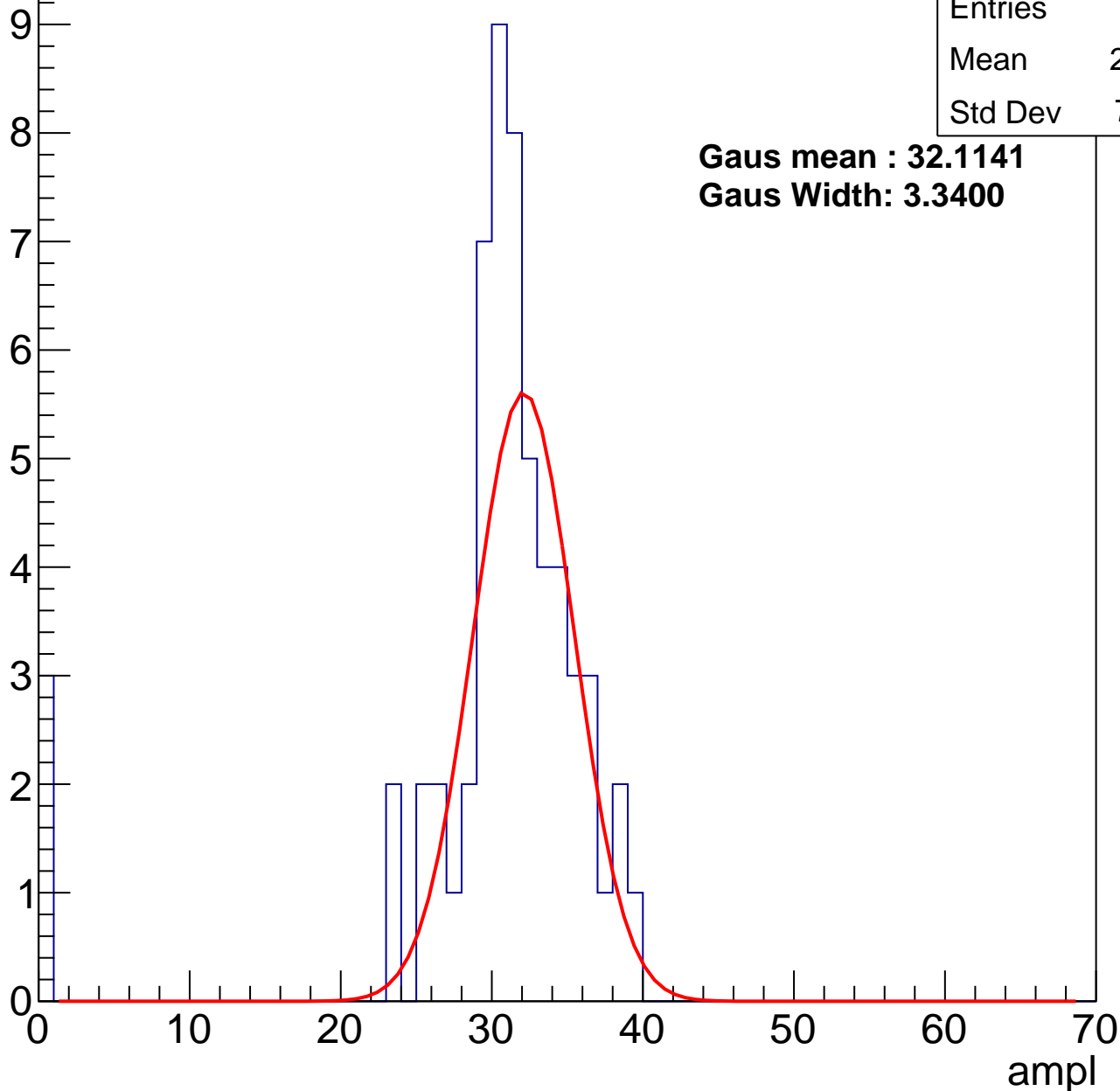
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 59    |
| Mean    | 29.58 |
| Std Dev | 7.661 |

**Gaus mean : 32.1141**

**Gaus Width: 3.3400**



# B0L001S, U2-ch57, adc1

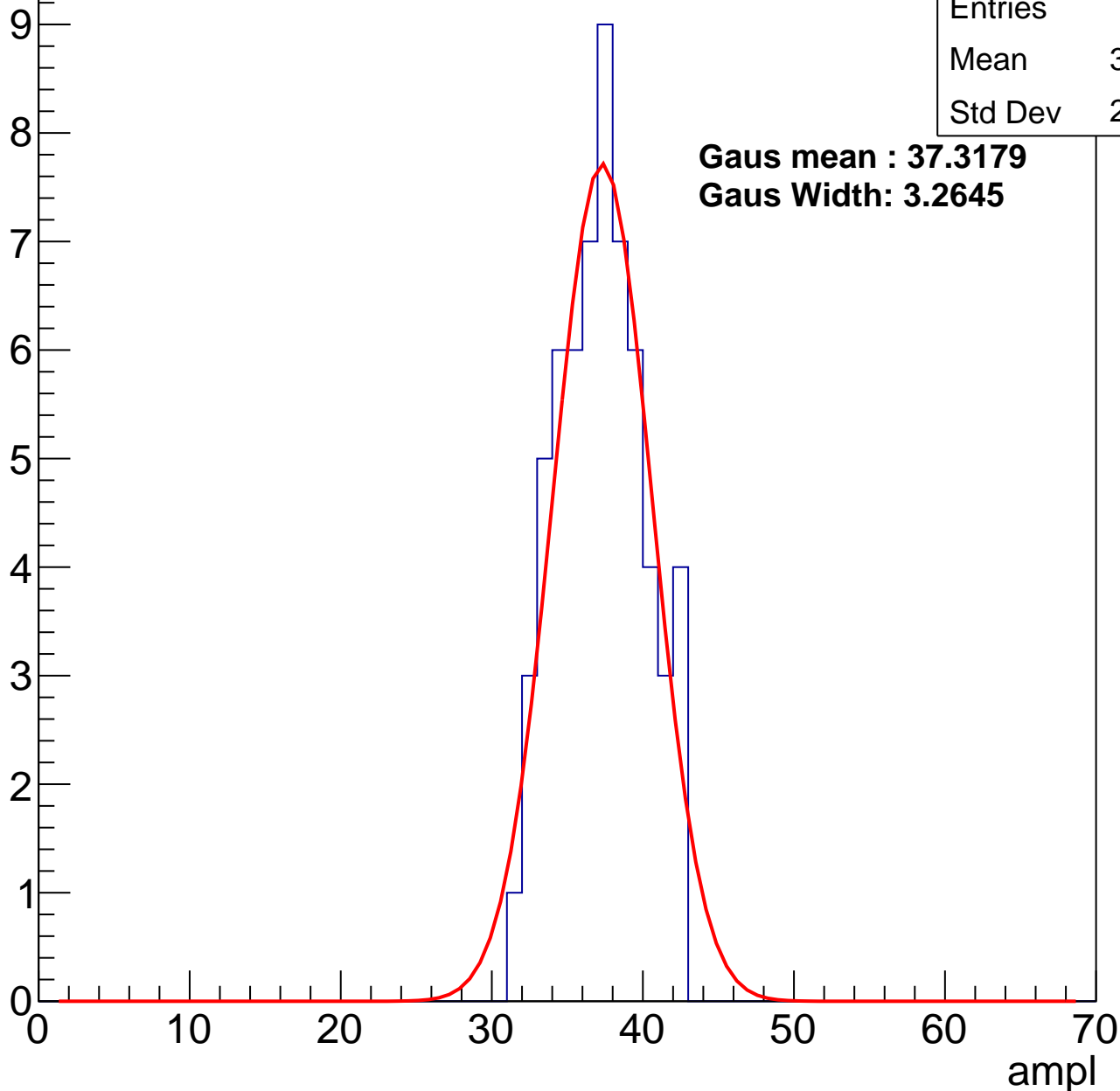
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 61    |
| Mean    | 36.75 |
| Std Dev | 2.826 |

**Gaus mean : 37.3179**

**Gaus Width: 3.2645**



# B0L001S, U2-ch57, adc2

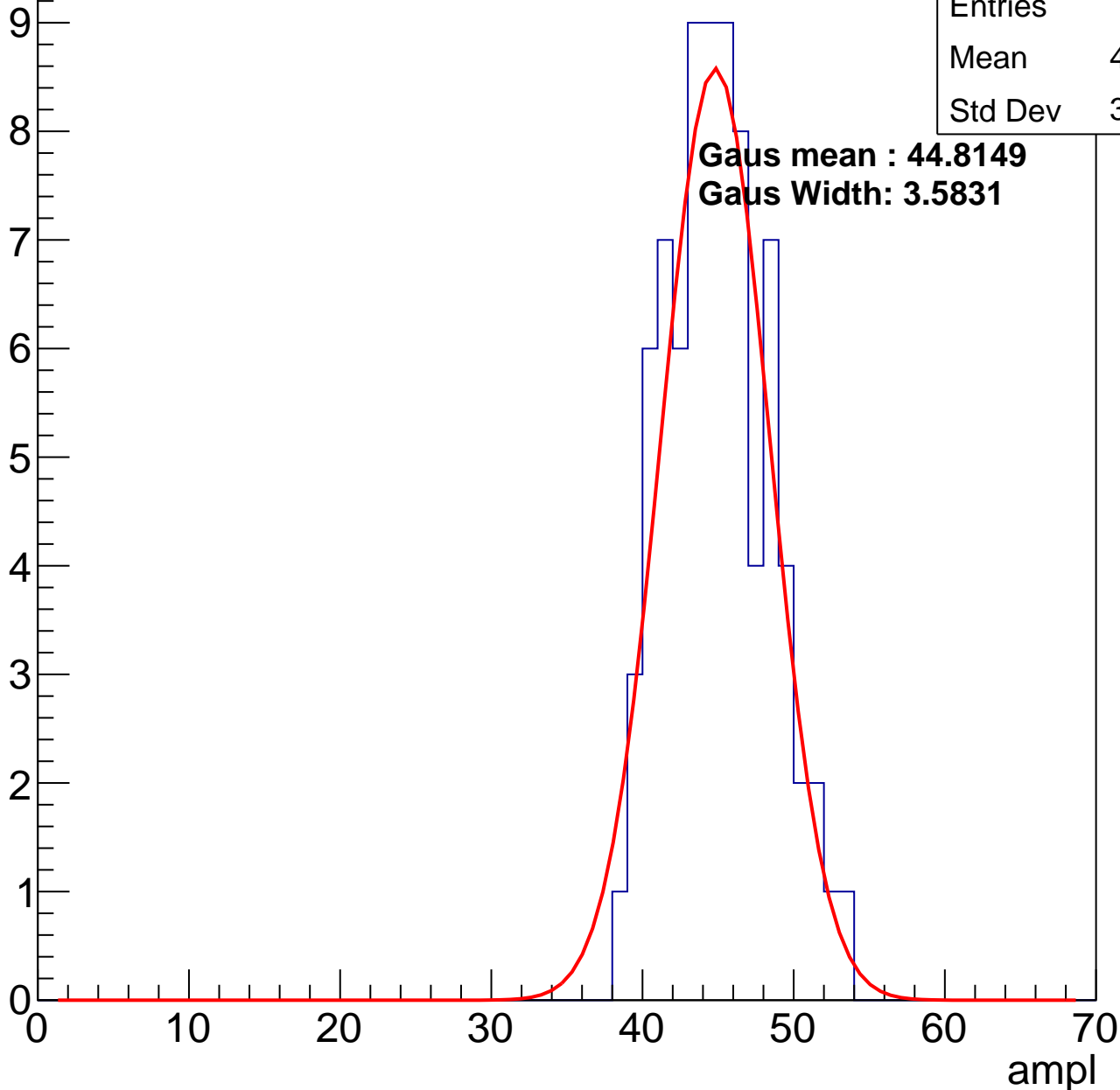
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 79    |
| Mean    | 44.52 |
| Std Dev | 3.348 |

**Gaus mean : 44.8149**

**Gaus Width: 3.5831**

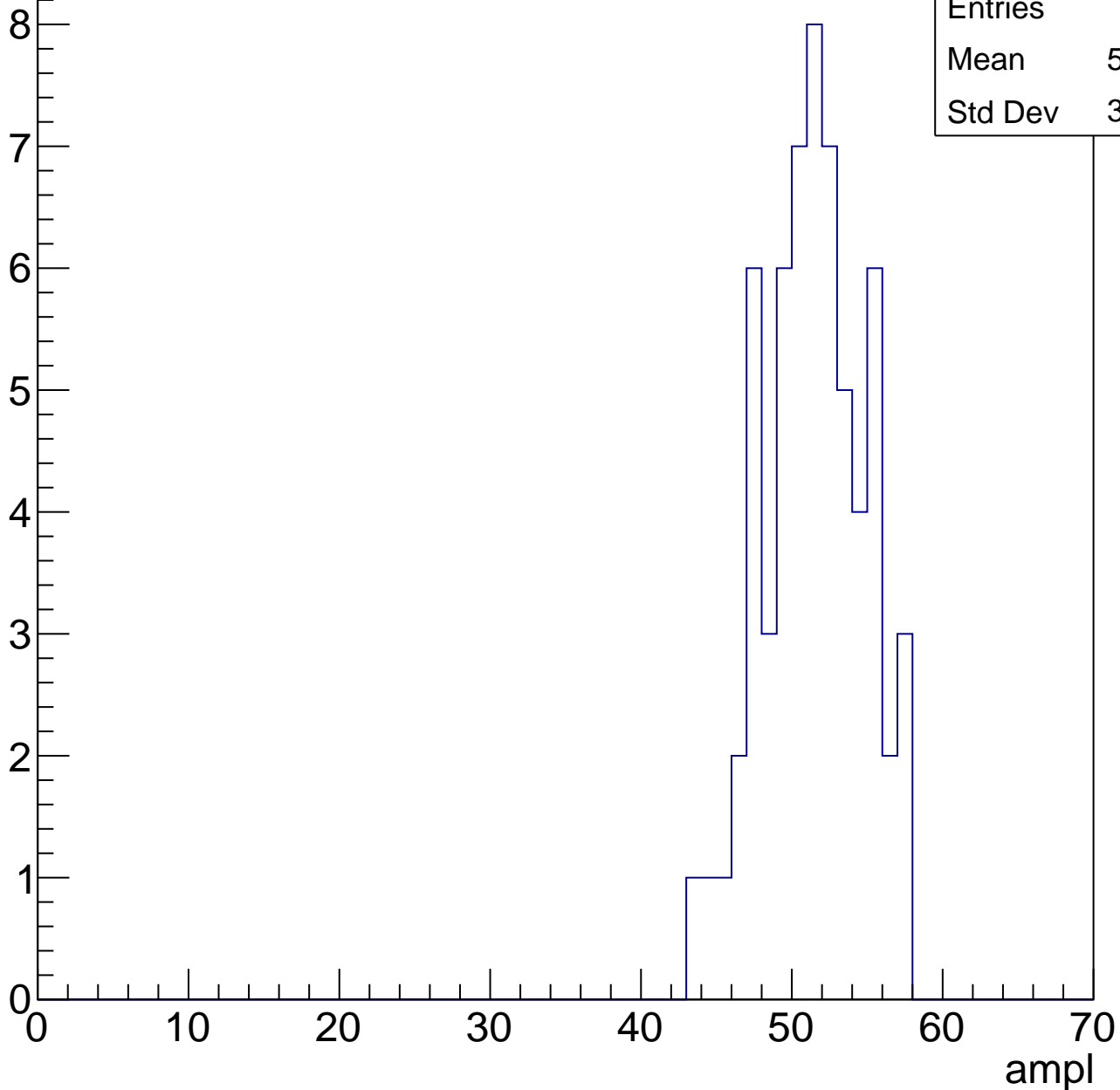


# B0L001S, U2-ch57, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

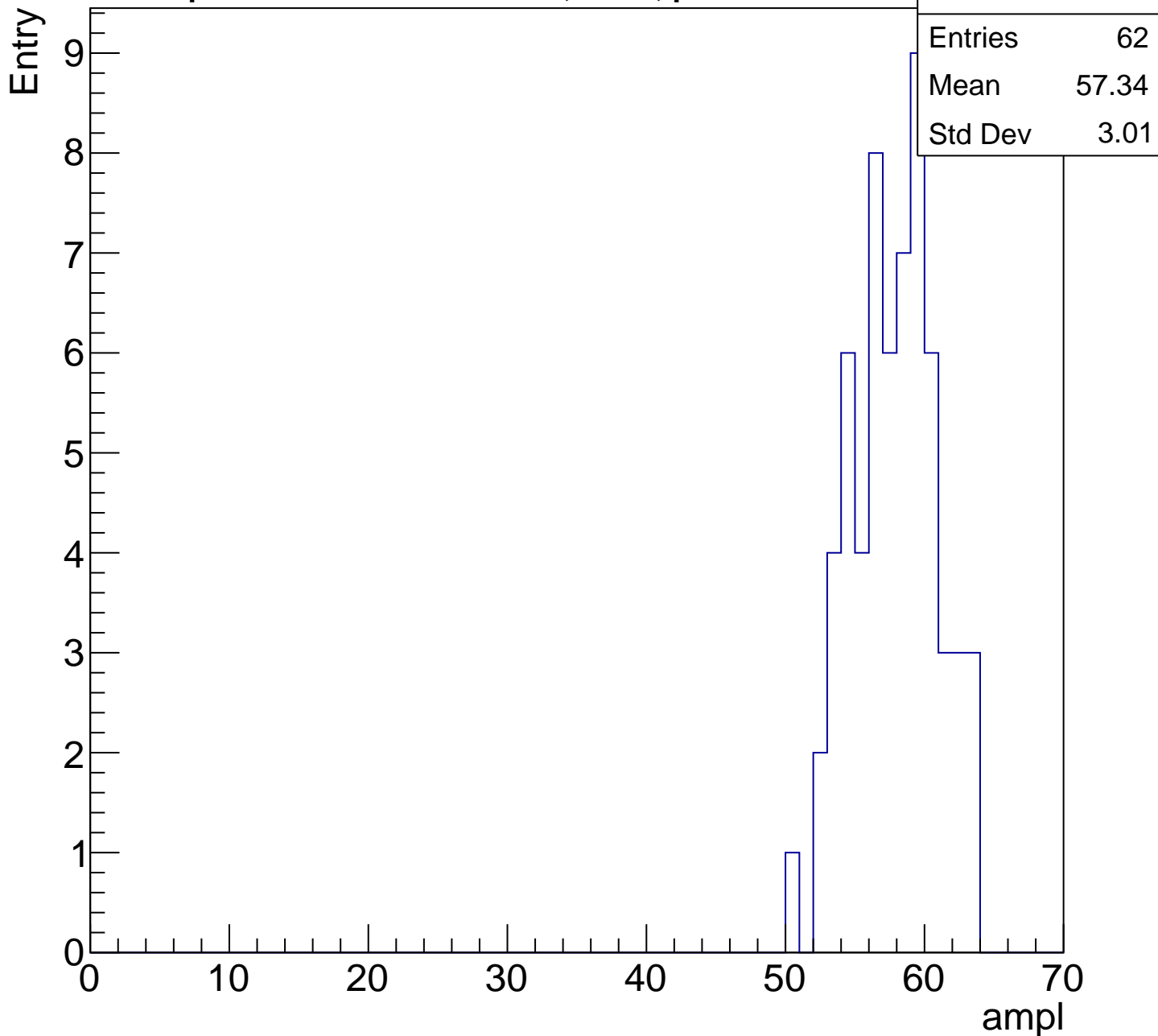
Entry

|         |       |
|---------|-------|
| Entries | 62    |
| Mean    | 50.97 |
| Std Dev | 3.287 |



# B0L001S, U2-ch57, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

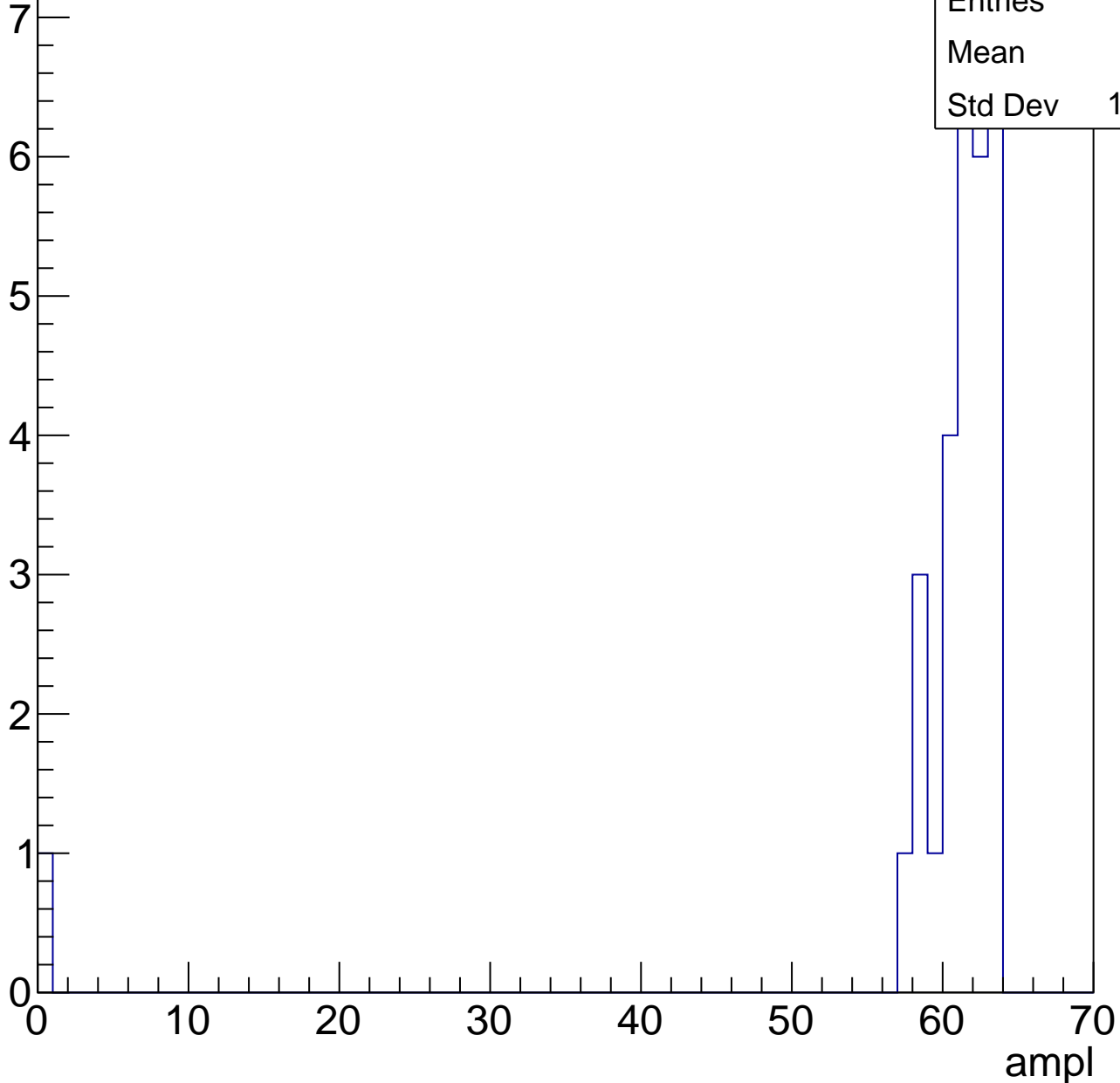


# B0L001S, U2-ch57, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 30    |
| Mean    | 59    |
| Std Dev | 11.08 |



# B0L001S, U2-ch57, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

1

Mean

62

Std Dev

0



# B0L001S, U2-ch57, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 0 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch58, adc0

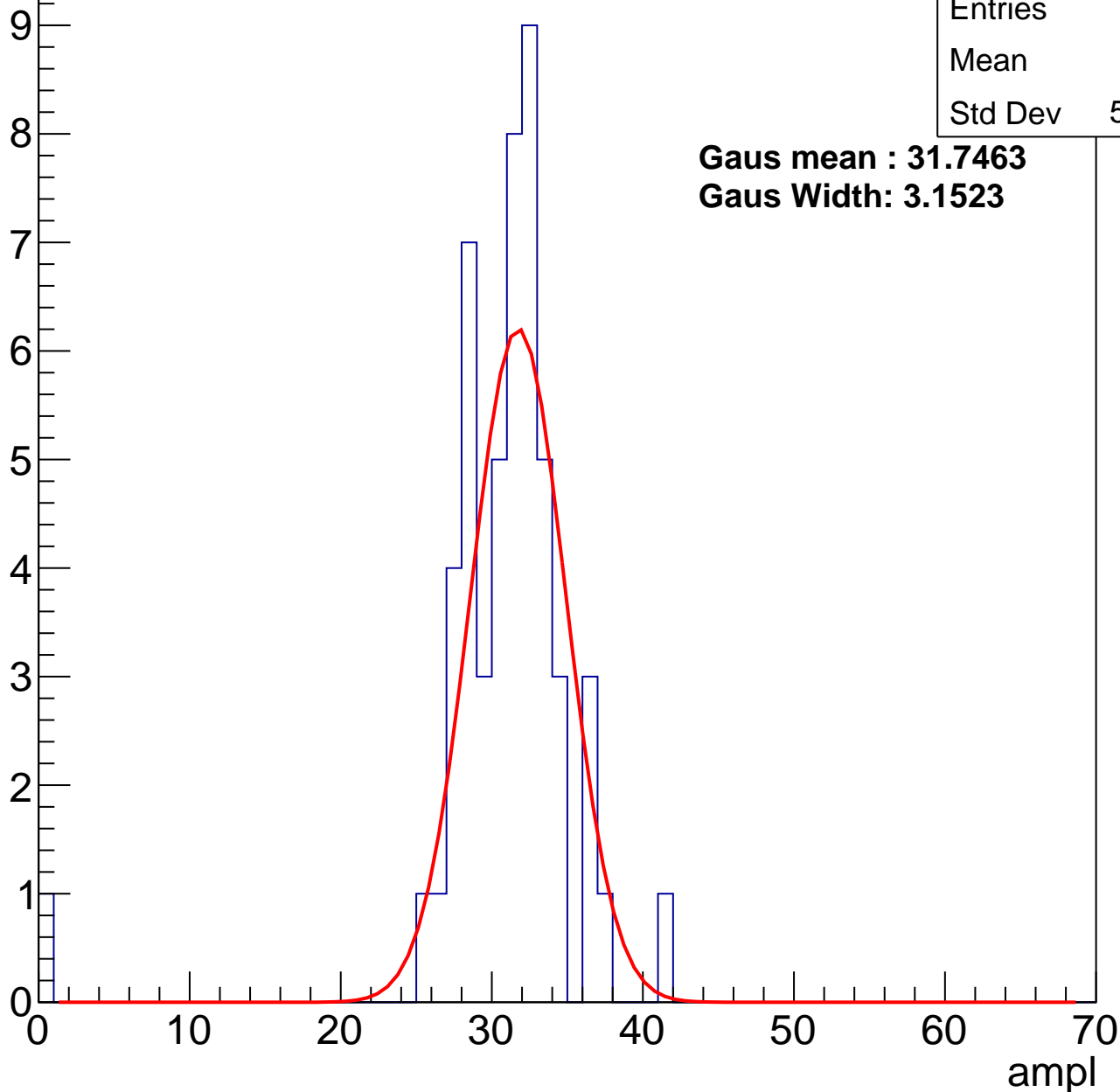
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 52    |
| Mean    | 30.4  |
| Std Dev | 5.216 |

**Gaus mean : 31.7463**

**Gaus Width: 3.1523**



# B0L001S, U2-ch58, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |      |
|---------|------|
| Entries | 60   |
| Mean    | 36.8 |
| Std Dev | 3.37 |

**Gaus mean : 37.3431**

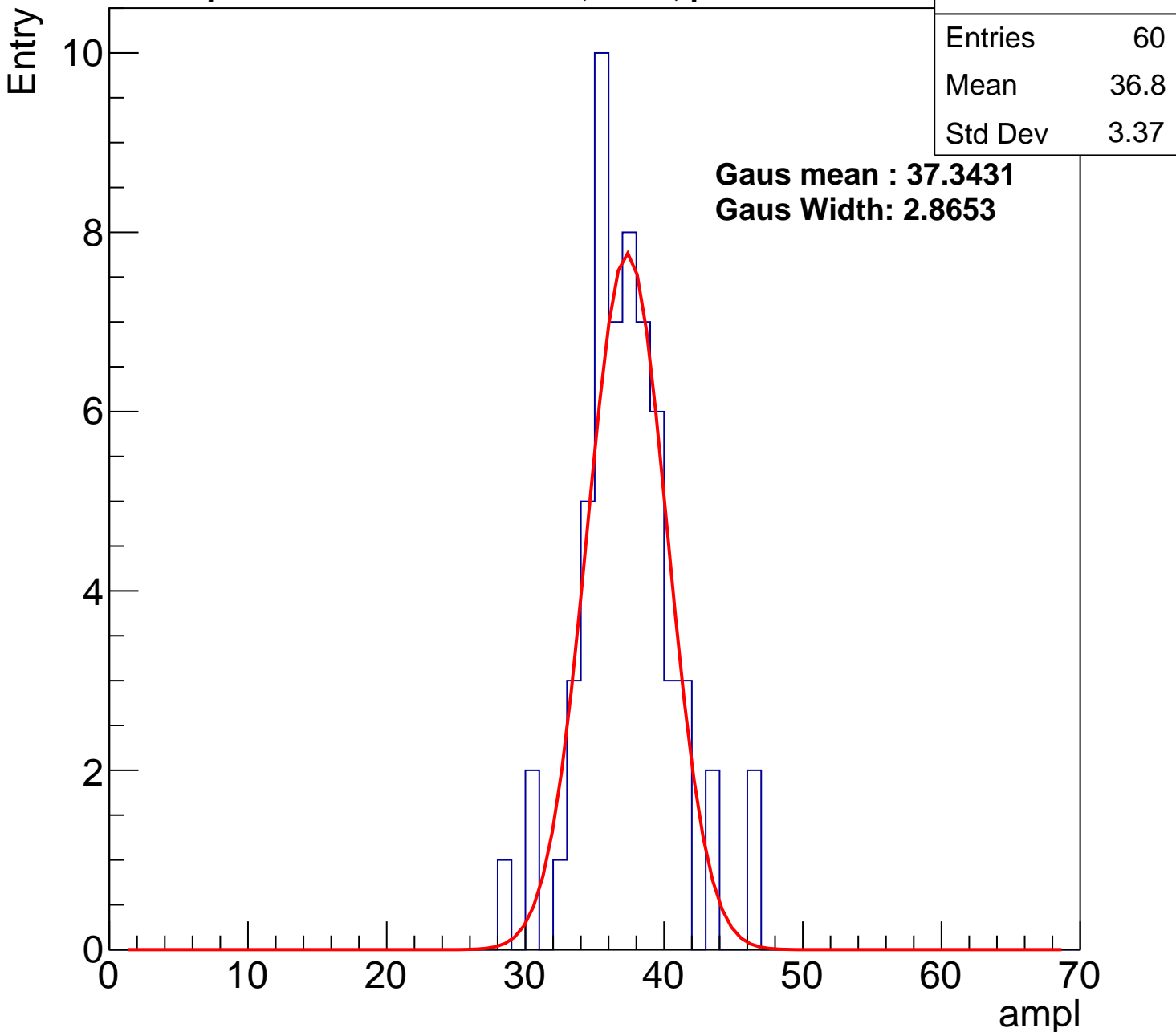
**Gaus Width: 2.8653**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B0L001S, U2-ch58, adc2

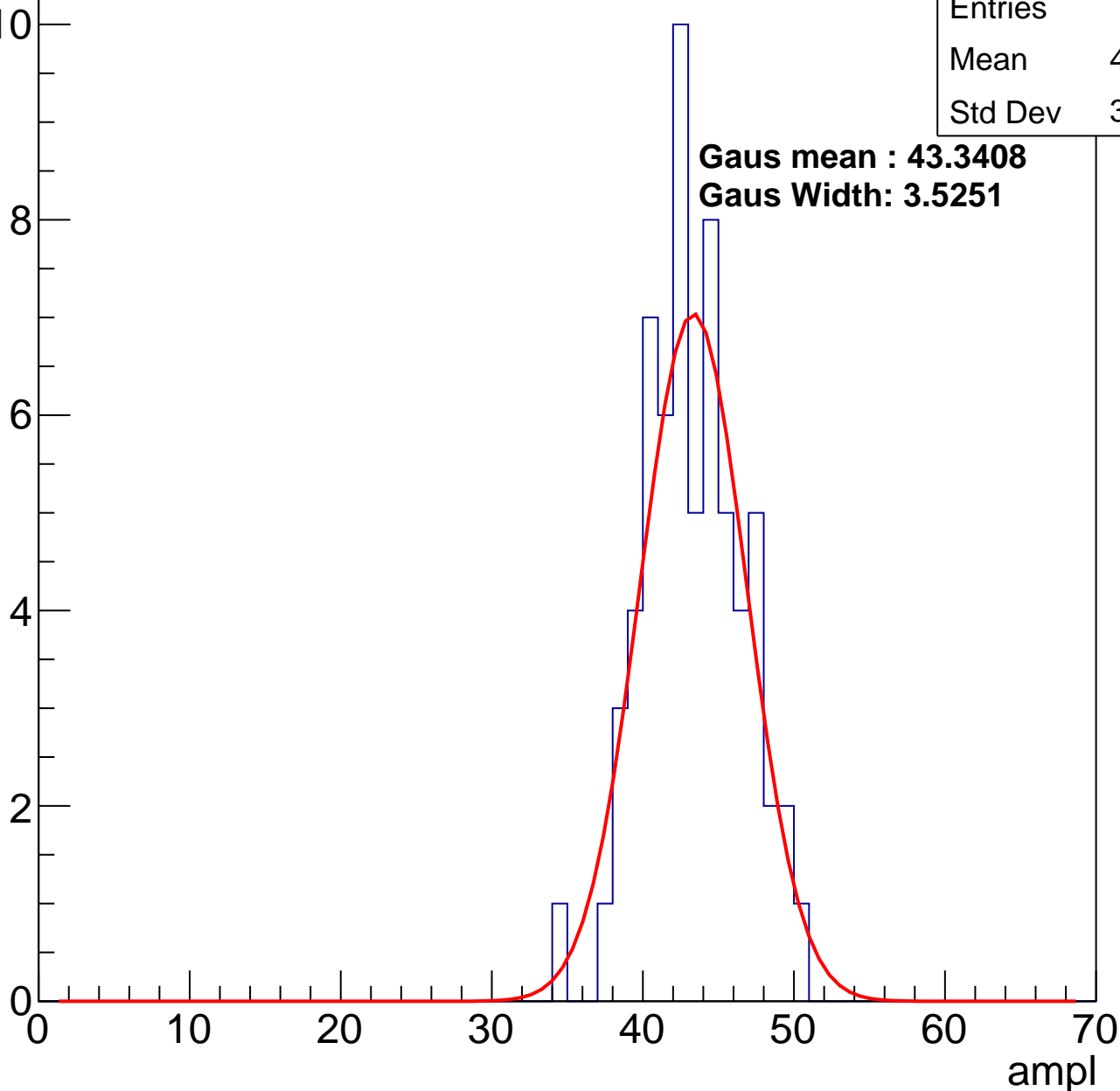
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 64    |
| Mean    | 42.84 |
| Std Dev | 3.227 |

**Gaus mean : 43.3408**

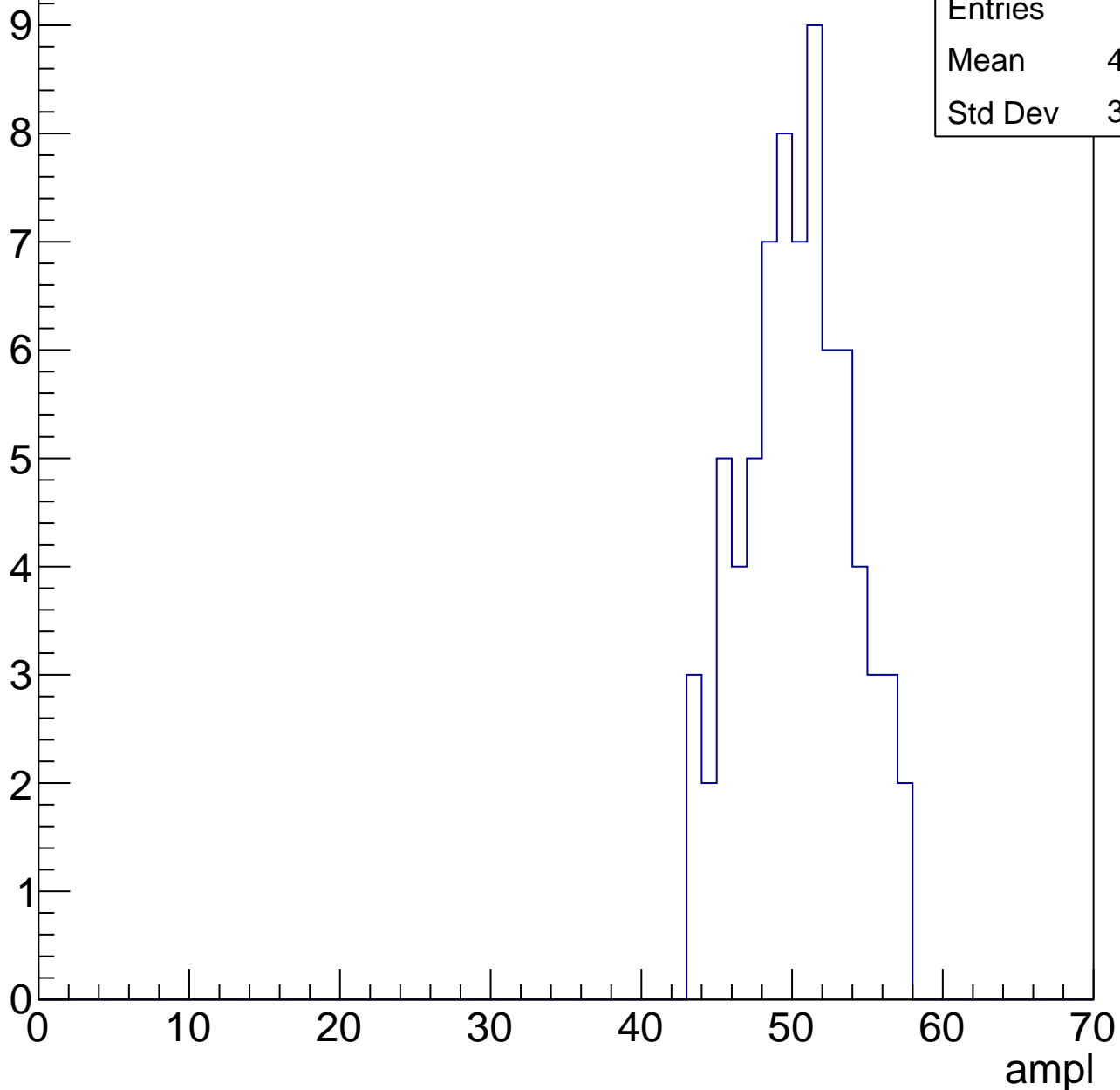
**Gaus Width: 3.5251**



# B0L001S, U2-ch58, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

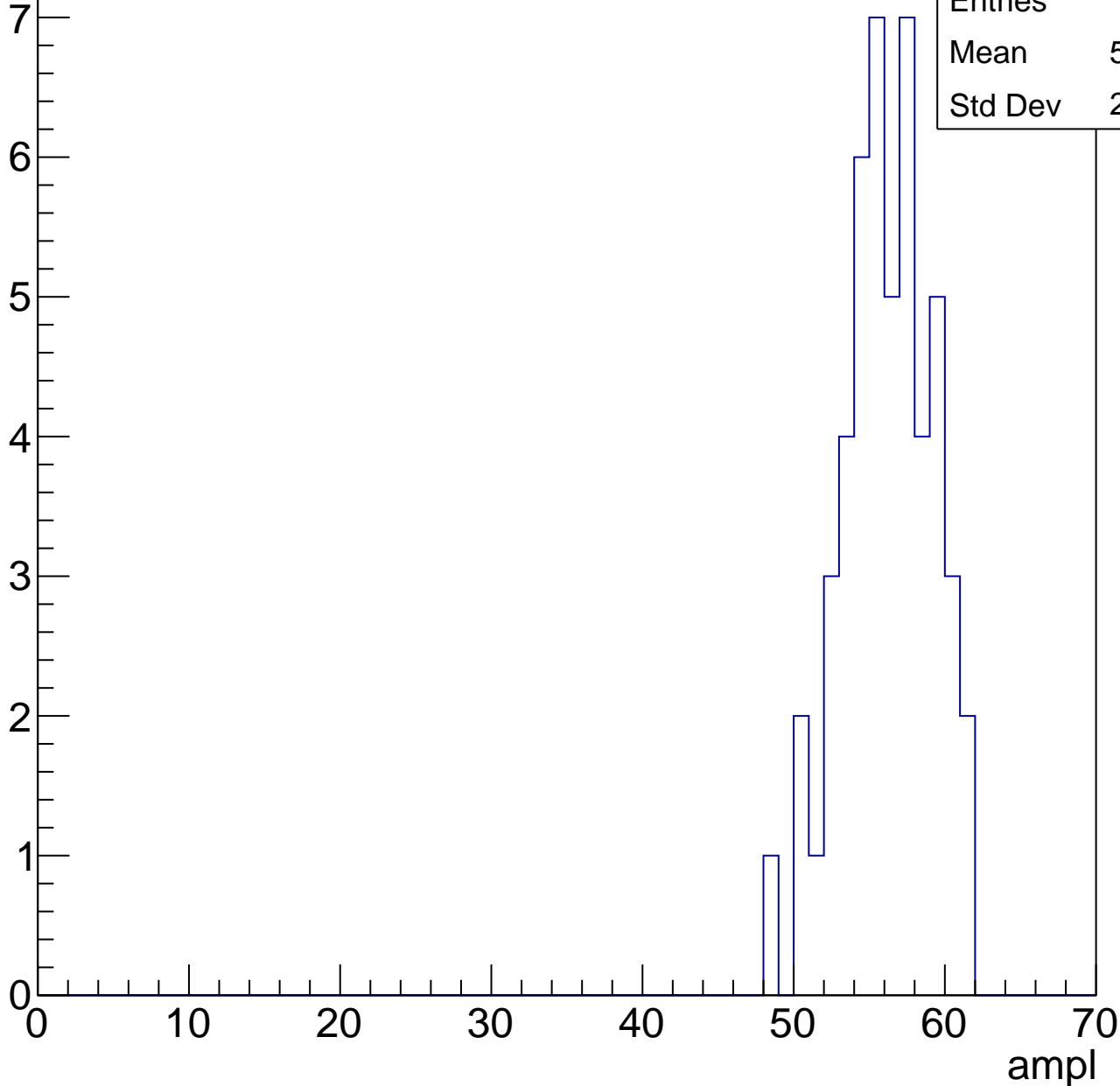


# B0L001S, U2-ch58, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 50    |
| Mean    | 55.68 |
| Std Dev | 2.956 |

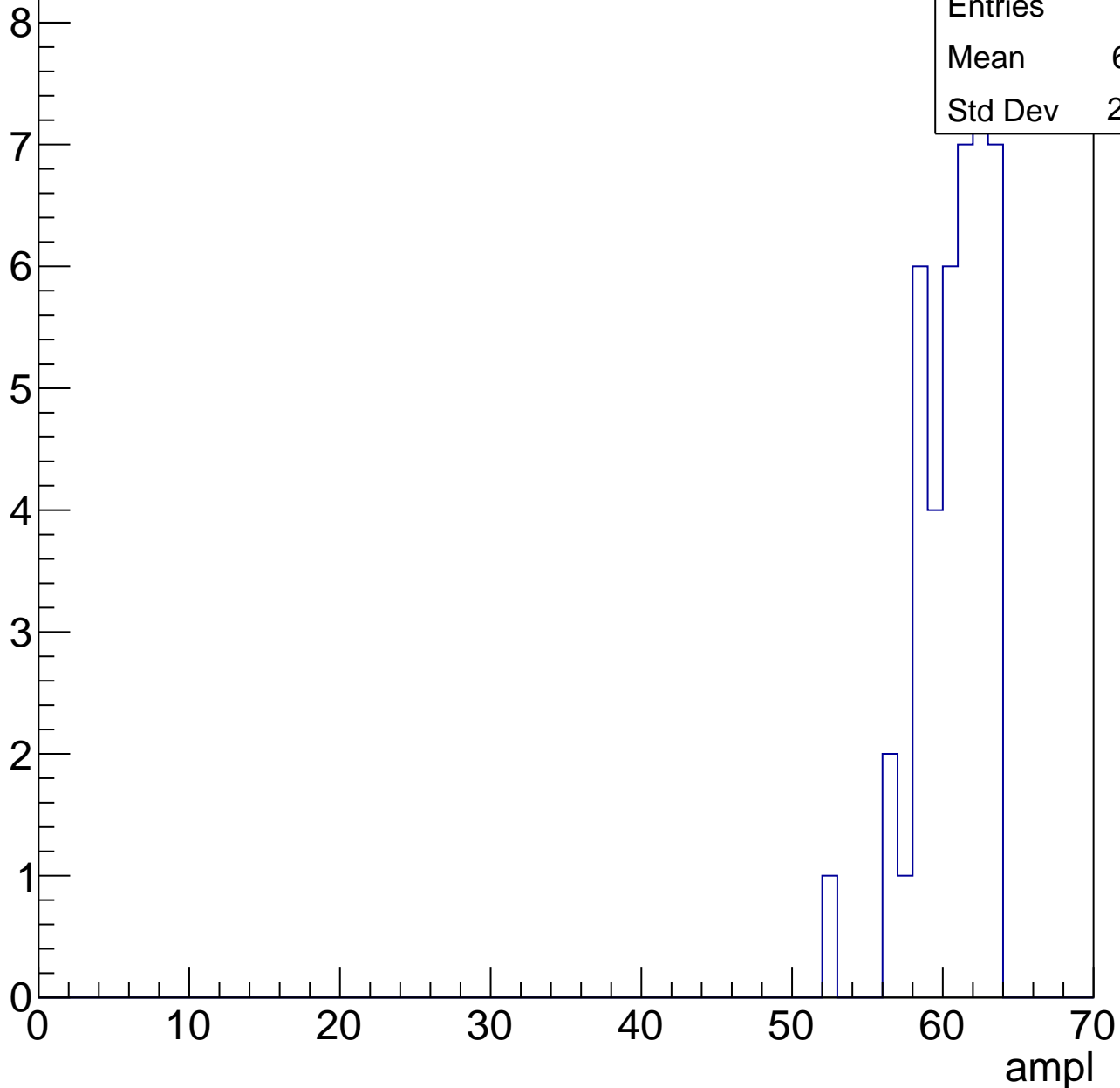


# B0L001S, U2-ch58, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

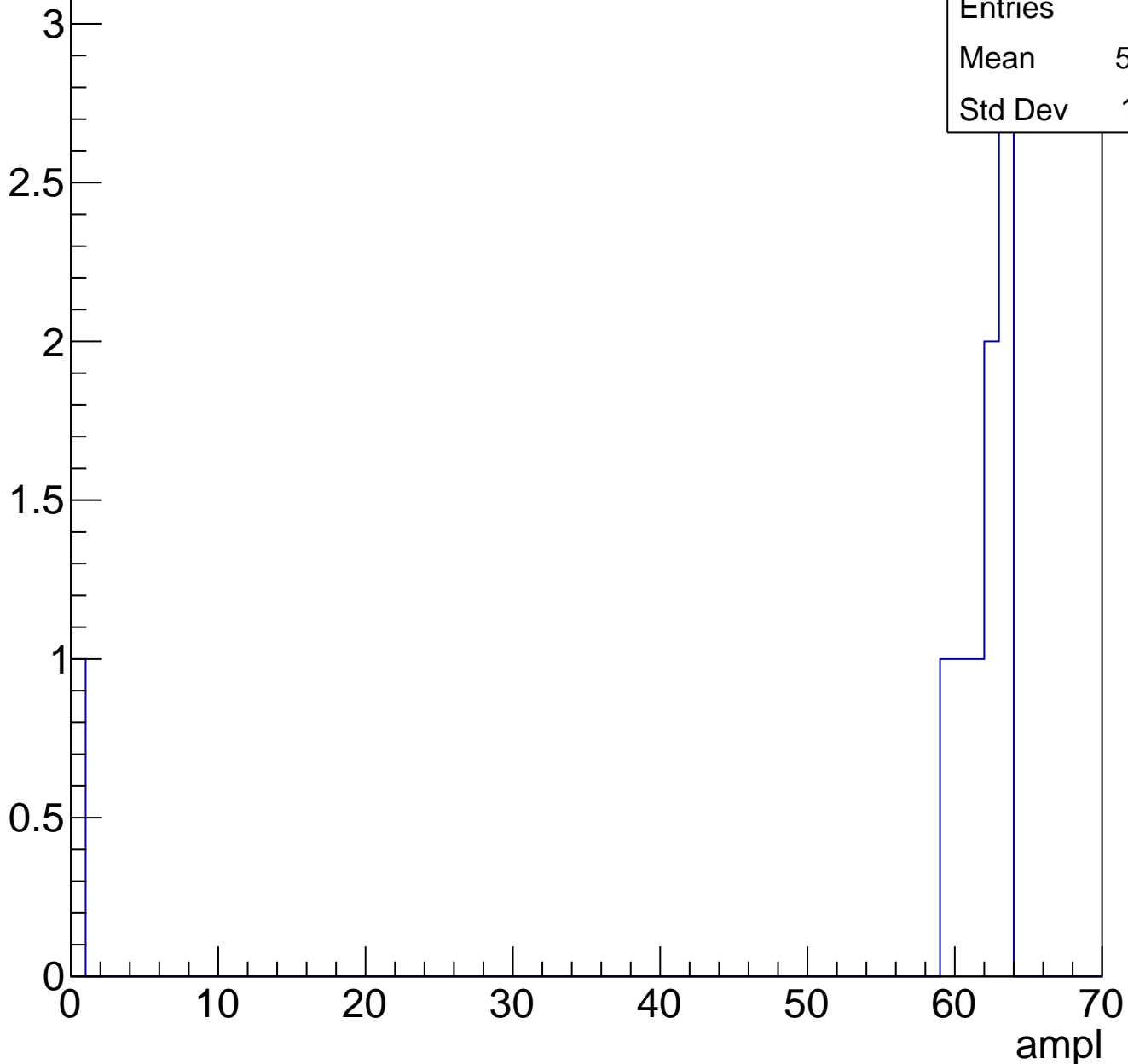
|         |       |
|---------|-------|
| Entries | 42    |
| Mean    | 60.21 |
| Std Dev | 2.356 |



# B0L001S, U2-ch58, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch58, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U2-ch59, adc0

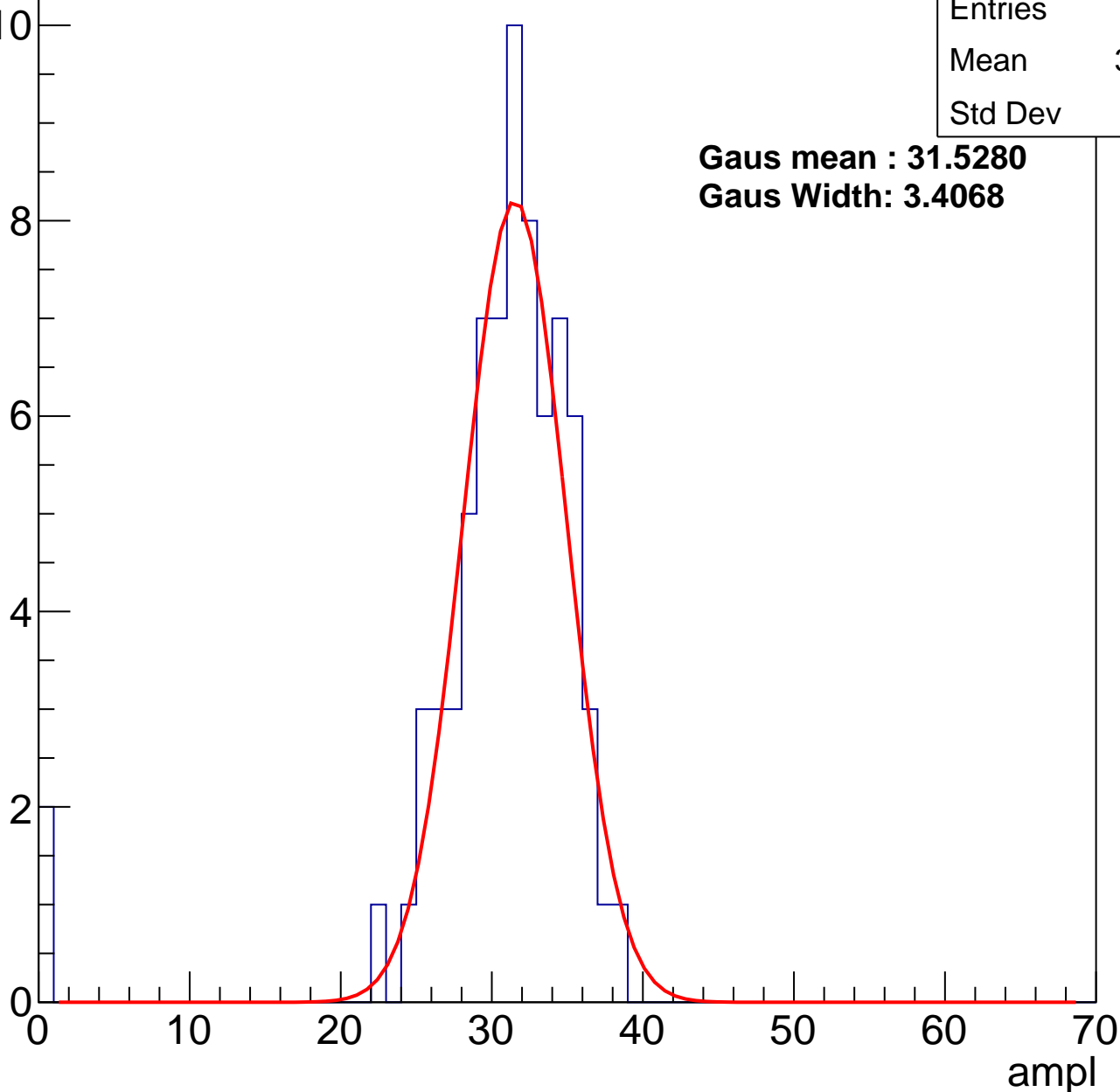
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 74    |
| Mean    | 30.11 |
| Std Dev | 5.99  |

**Gaus mean : 31.5280**

**Gaus Width: 3.4068**



# B0L001S, U2-ch59, adc1

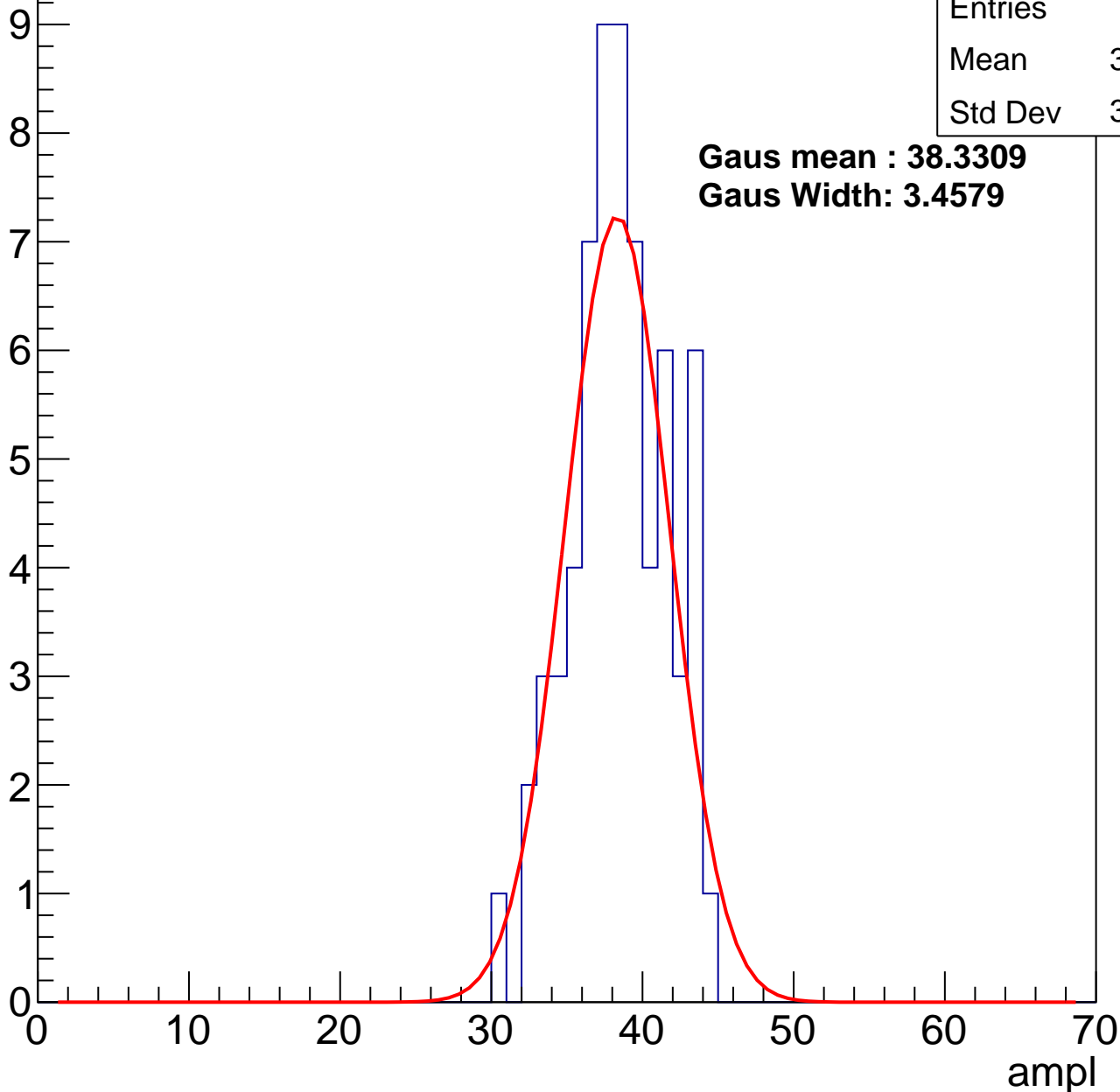
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 65    |
| Mean    | 37.98 |
| Std Dev | 3.145 |

**Gaus mean : 38.3309**

**Gaus Width: 3.4579**



# B0L001S, U2-ch59, adc2

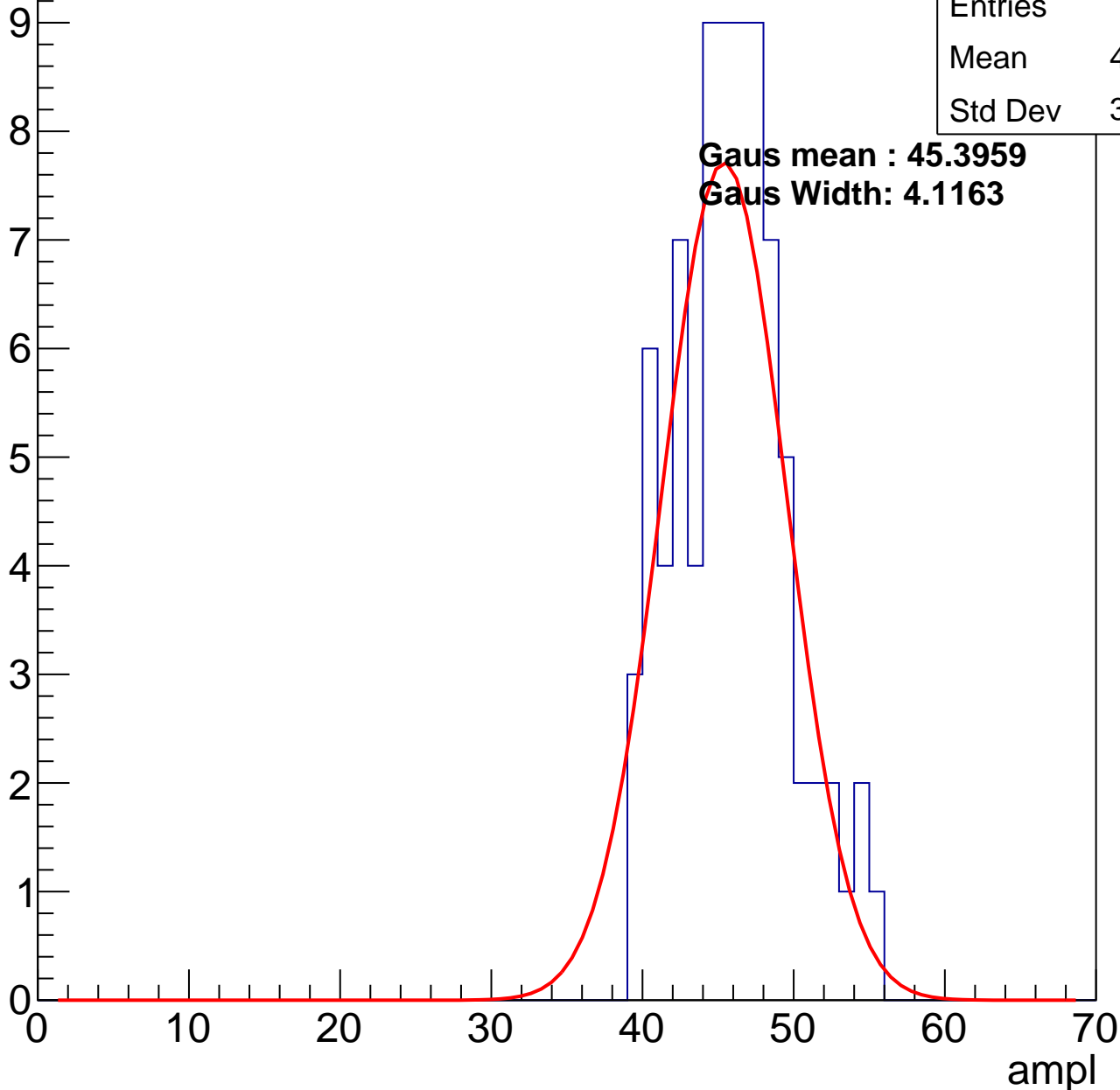
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 82    |
| Mean    | 45.46 |
| Std Dev | 3.706 |

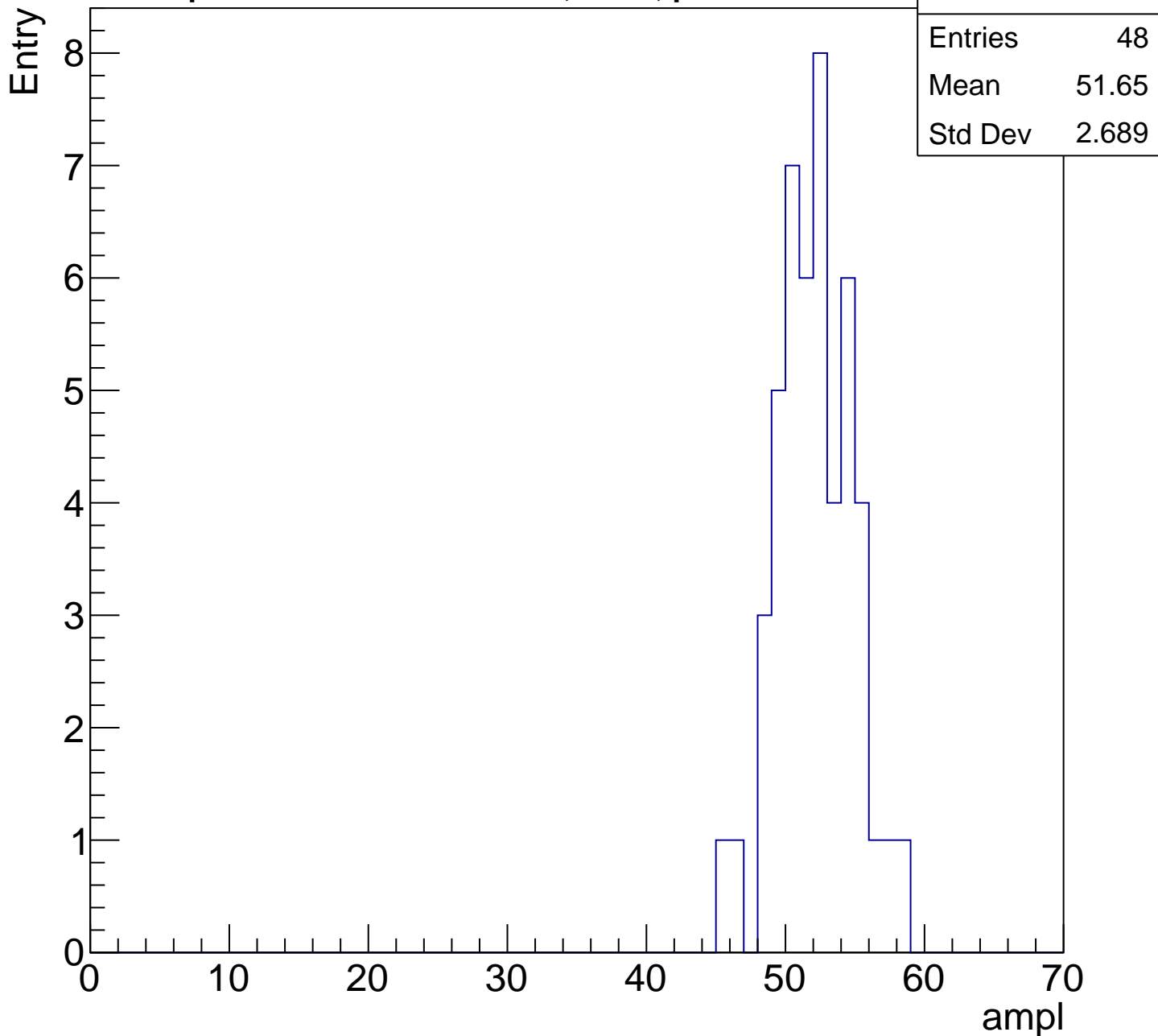
**Gaus mean : 45.3959**

**Gaus Width: 4.1163**



# B0L001S, U2-ch59, adc3

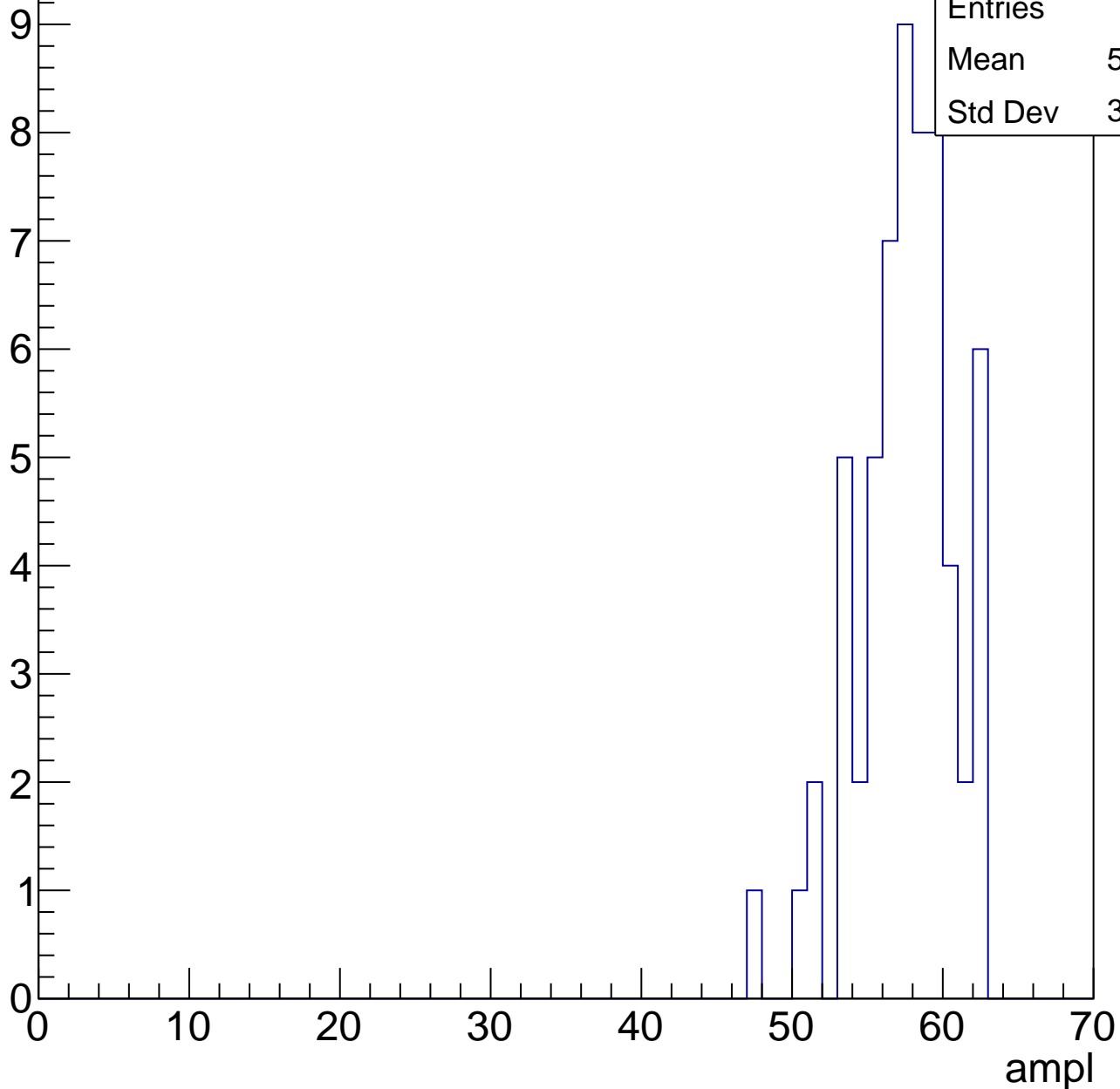
calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U2-ch59, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

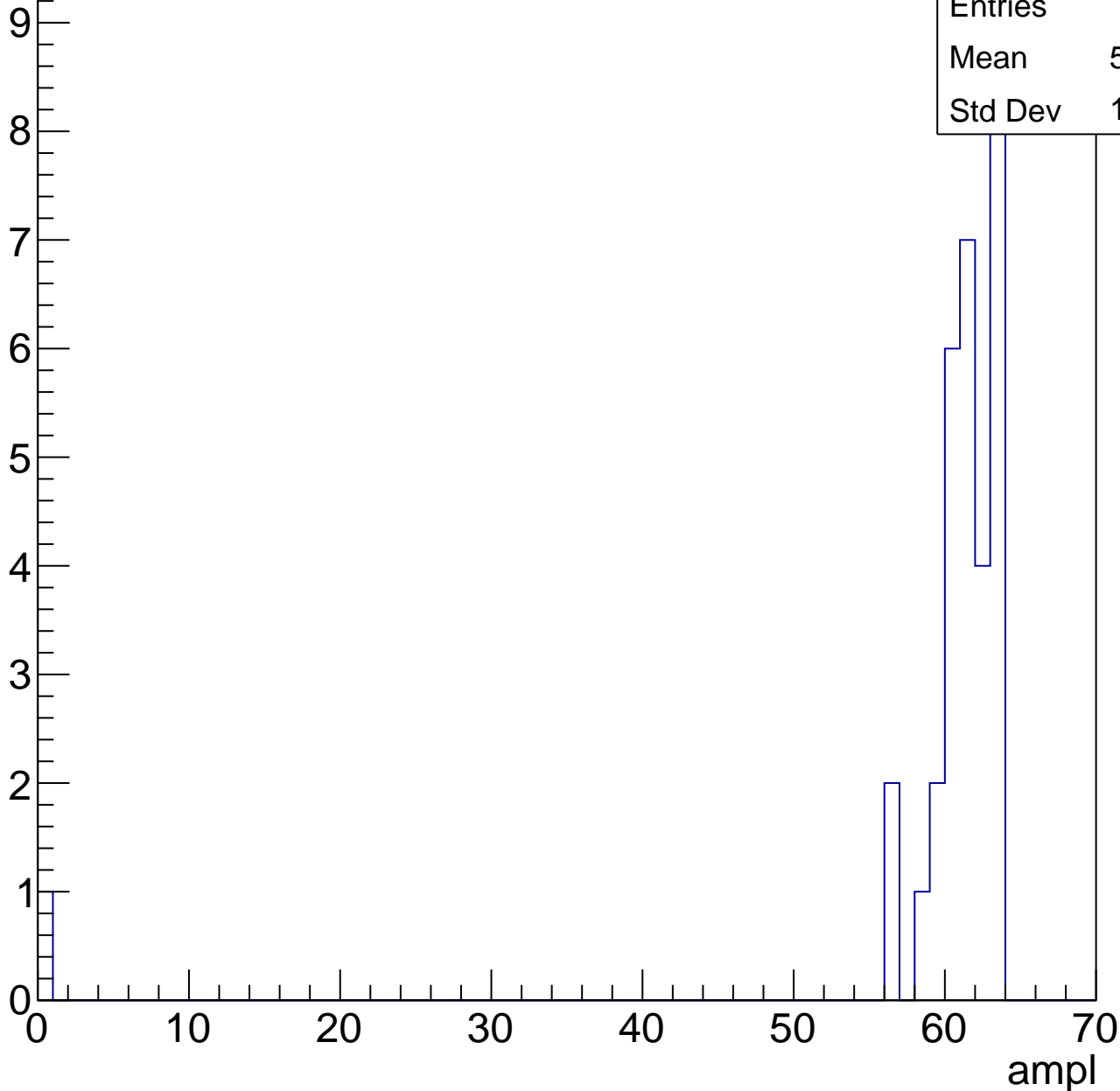


# B0L001S, U2-ch59, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

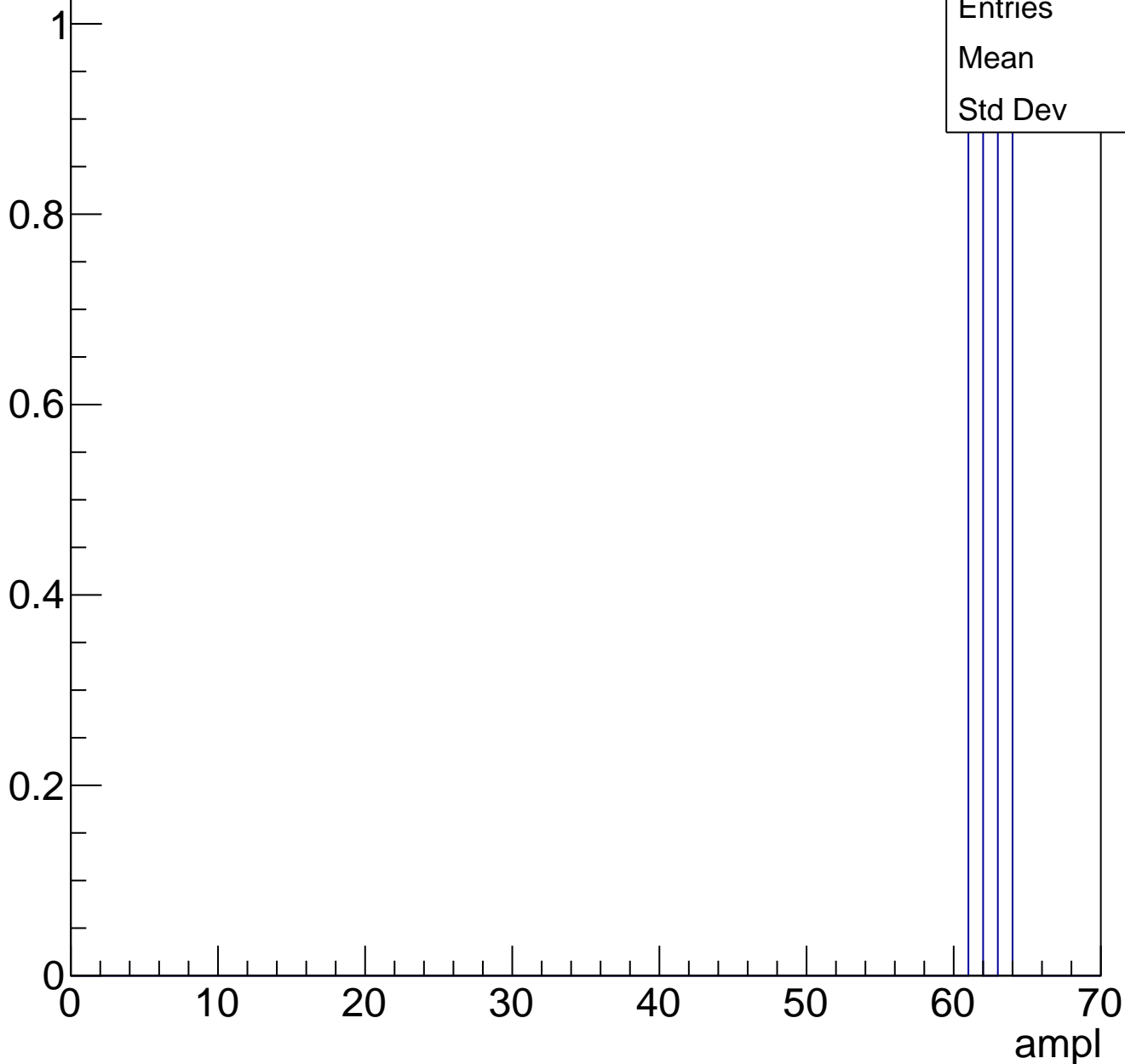
|         |       |
|---------|-------|
| Entries | 32    |
| Mean    | 59.06 |
| Std Dev | 10.77 |



# B0L001S, U2-ch59, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch59, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 0 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch60, adc0

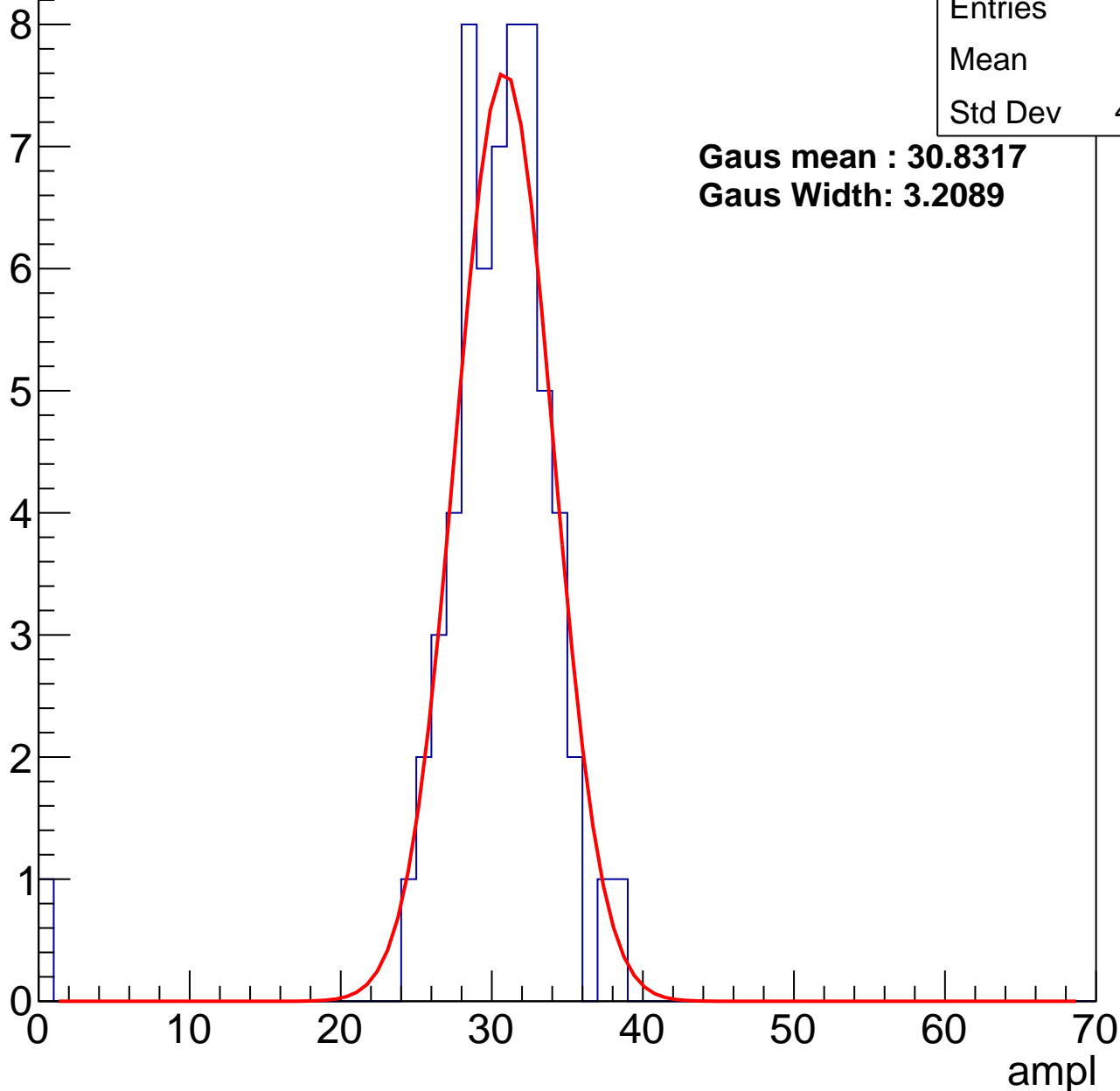
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 61    |
| Mean    | 29.8  |
| Std Dev | 4.821 |

**Gaus mean : 30.8317**

**Gaus Width: 3.2089**



# B0L001S, U2-ch60, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 73    |
| Mean    | 36.97 |
| Std Dev | 3.269 |

**Gaus mean : 37.2187**

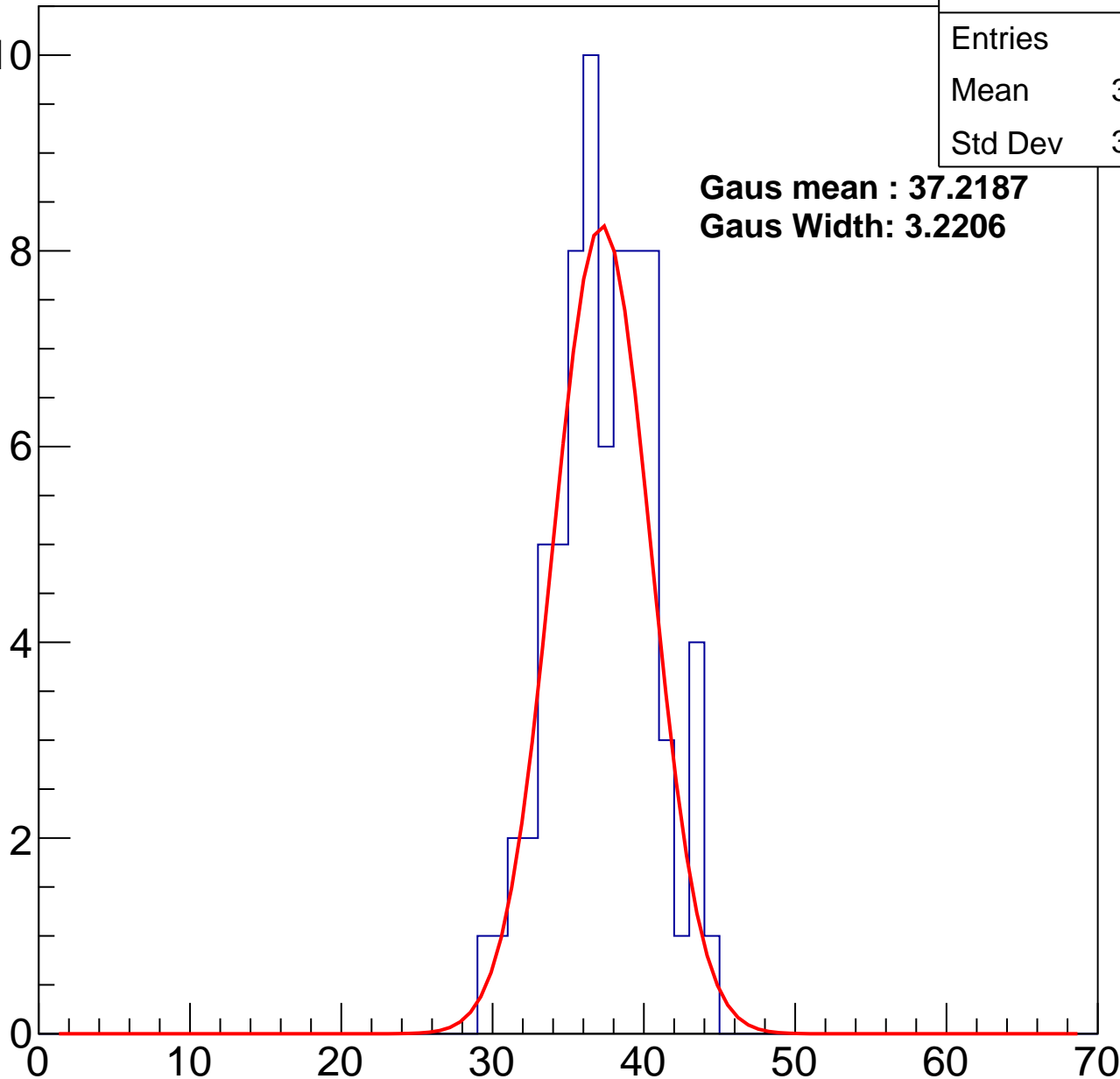
**Gaus Width: 3.2206**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B0L001S, U2-ch60, adc2

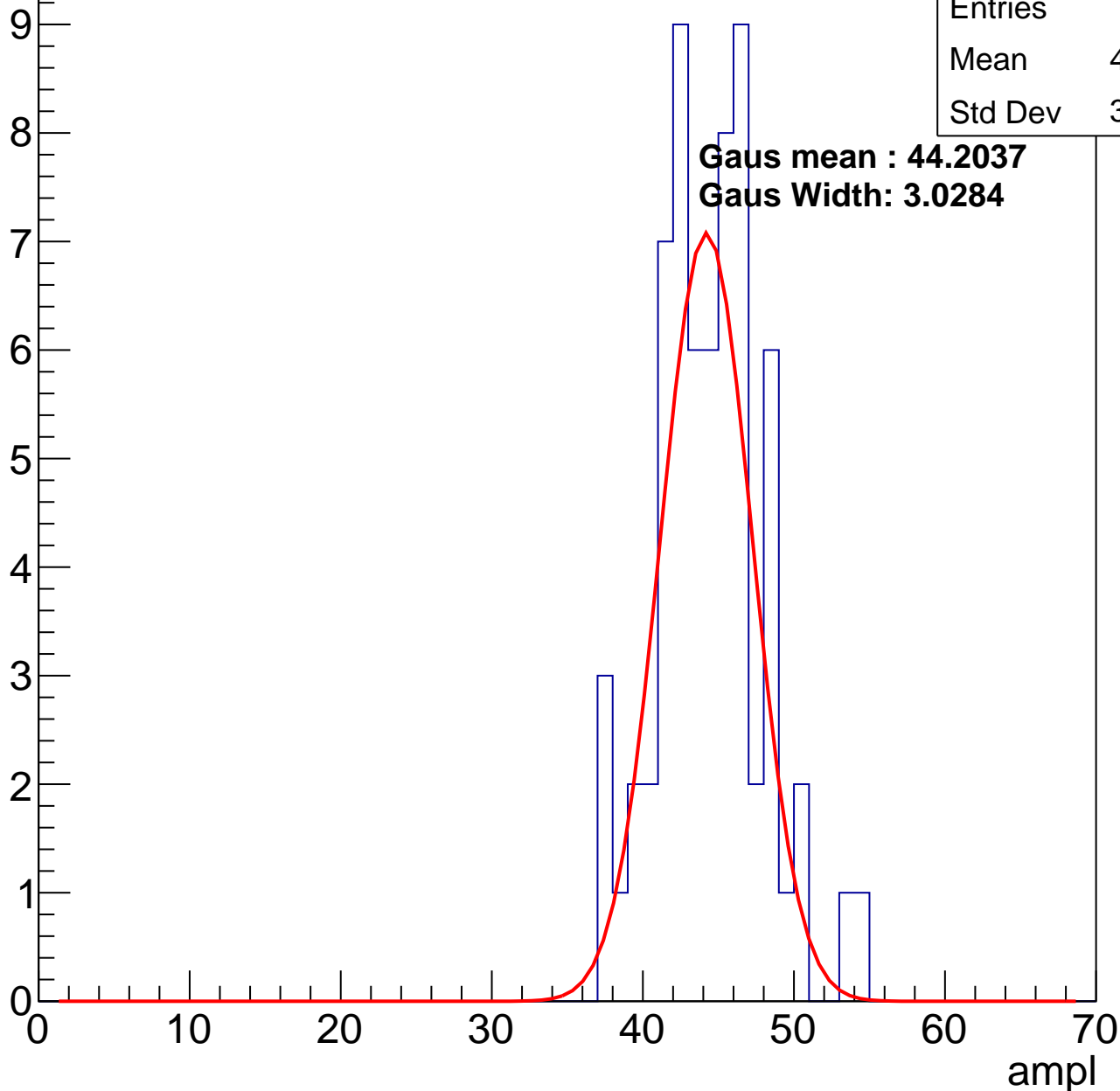
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 66    |
| Mean    | 44.03 |
| Std Dev | 3.494 |

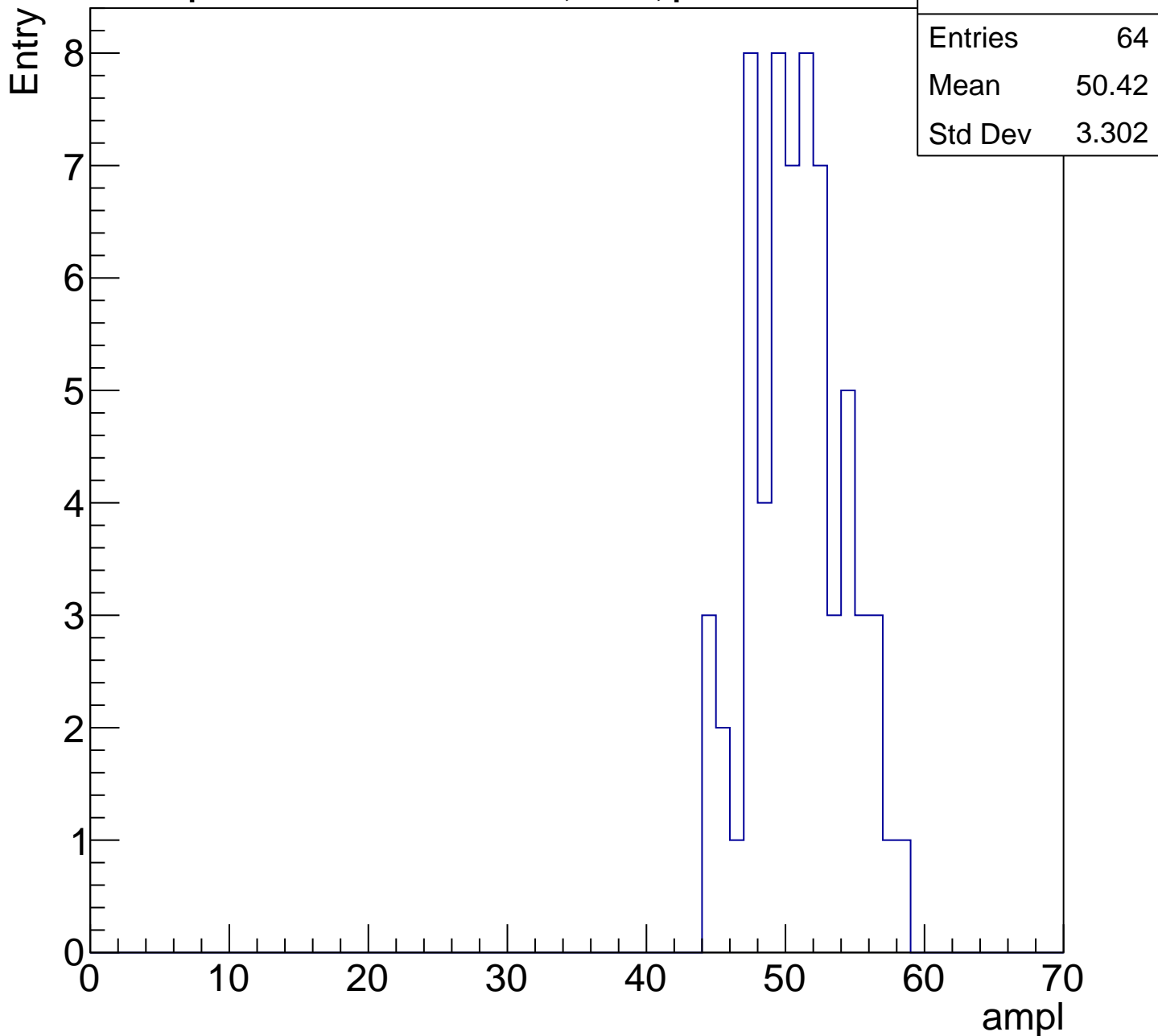
**Gaus mean : 44.2037**

**Gaus Width: 3.0284**



# B0L001S, U2-ch60, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

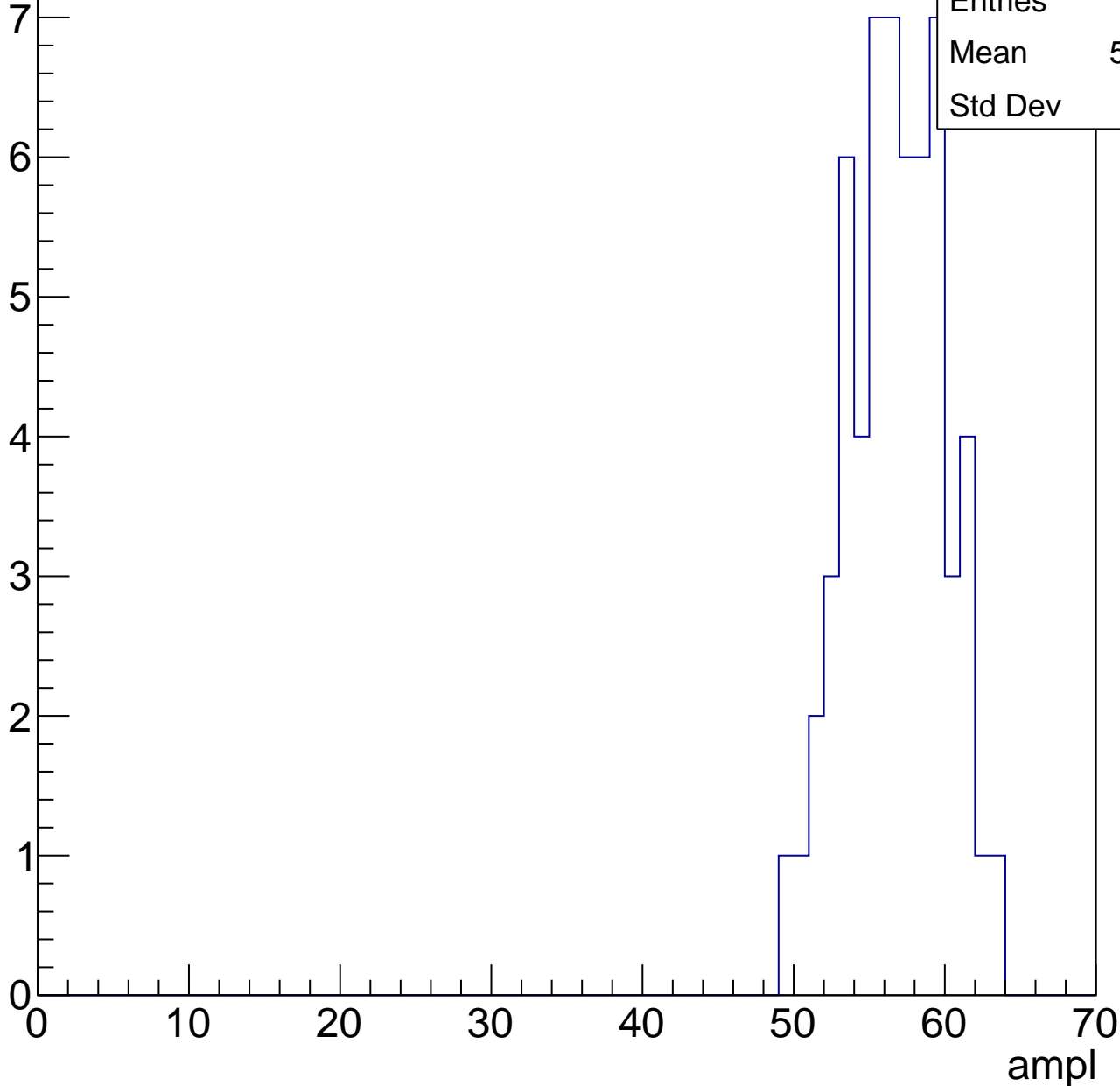


# B0L001S, U2-ch60, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

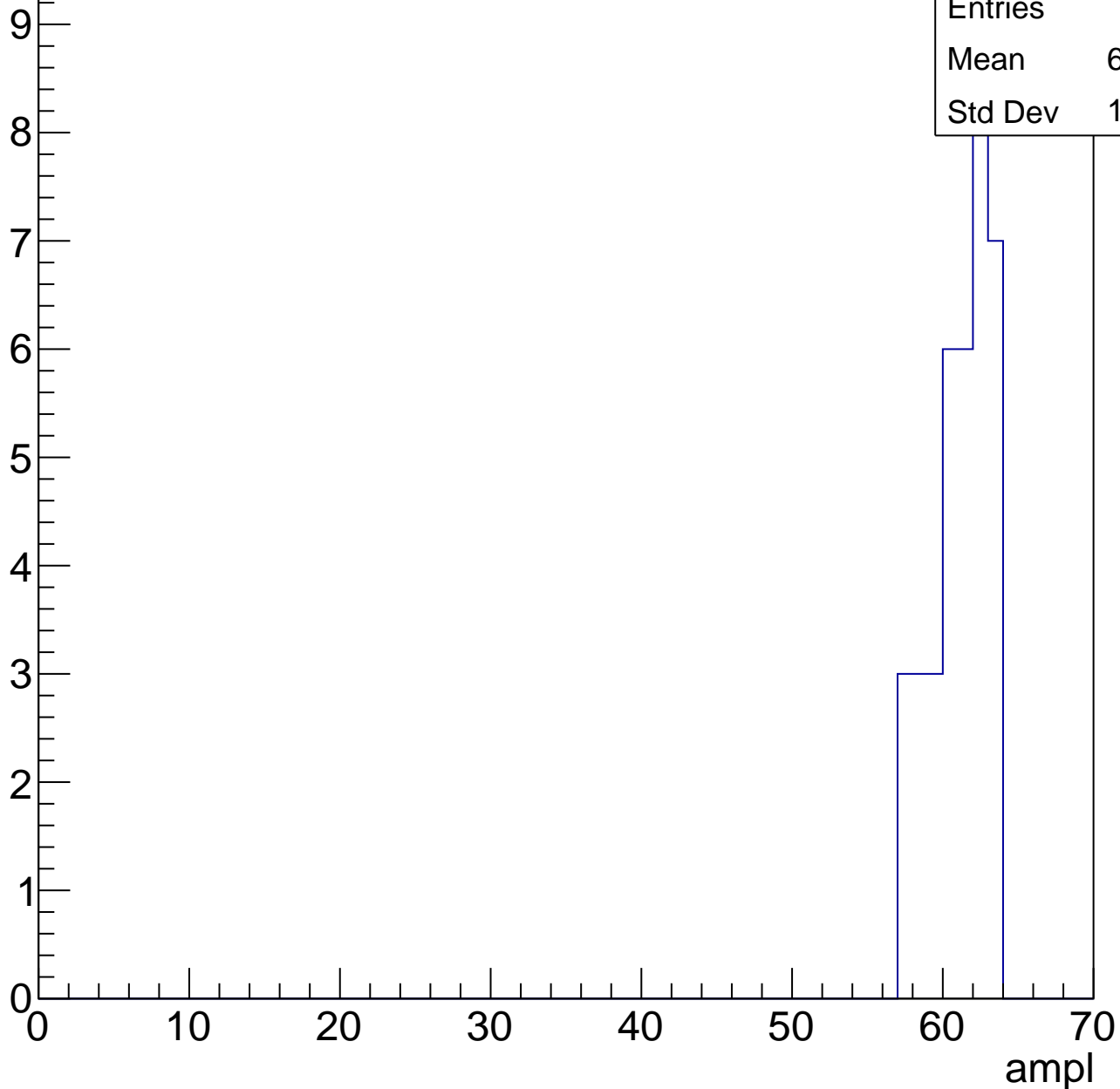
|         |       |
|---------|-------|
| Entries | 59    |
| Mean    | 56.27 |
| Std Dev | 3.14  |



# B0L001S, U2-ch60, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

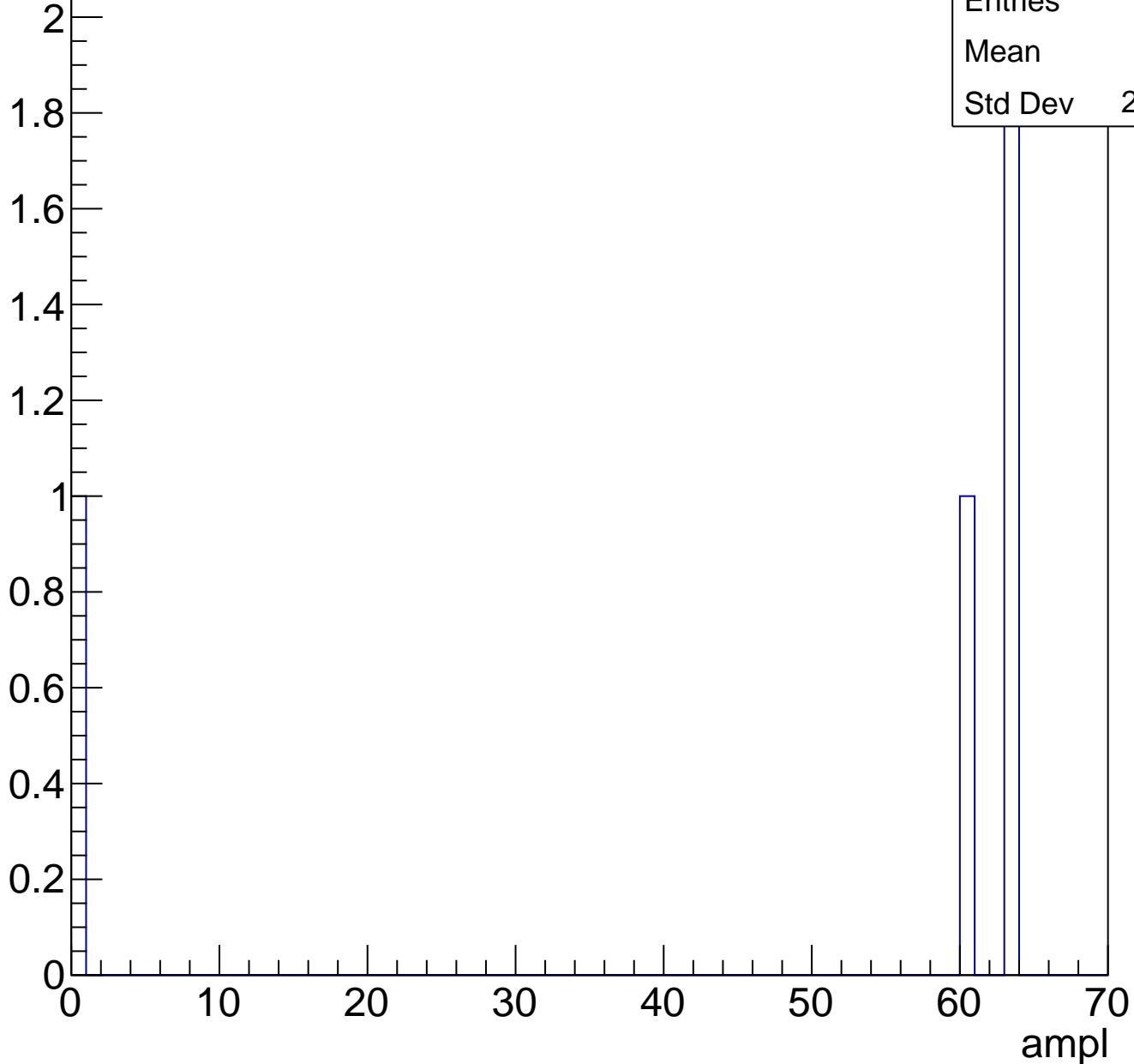
Entry



# B0L001S, U2-ch60, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch60, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 0 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch61, adc0

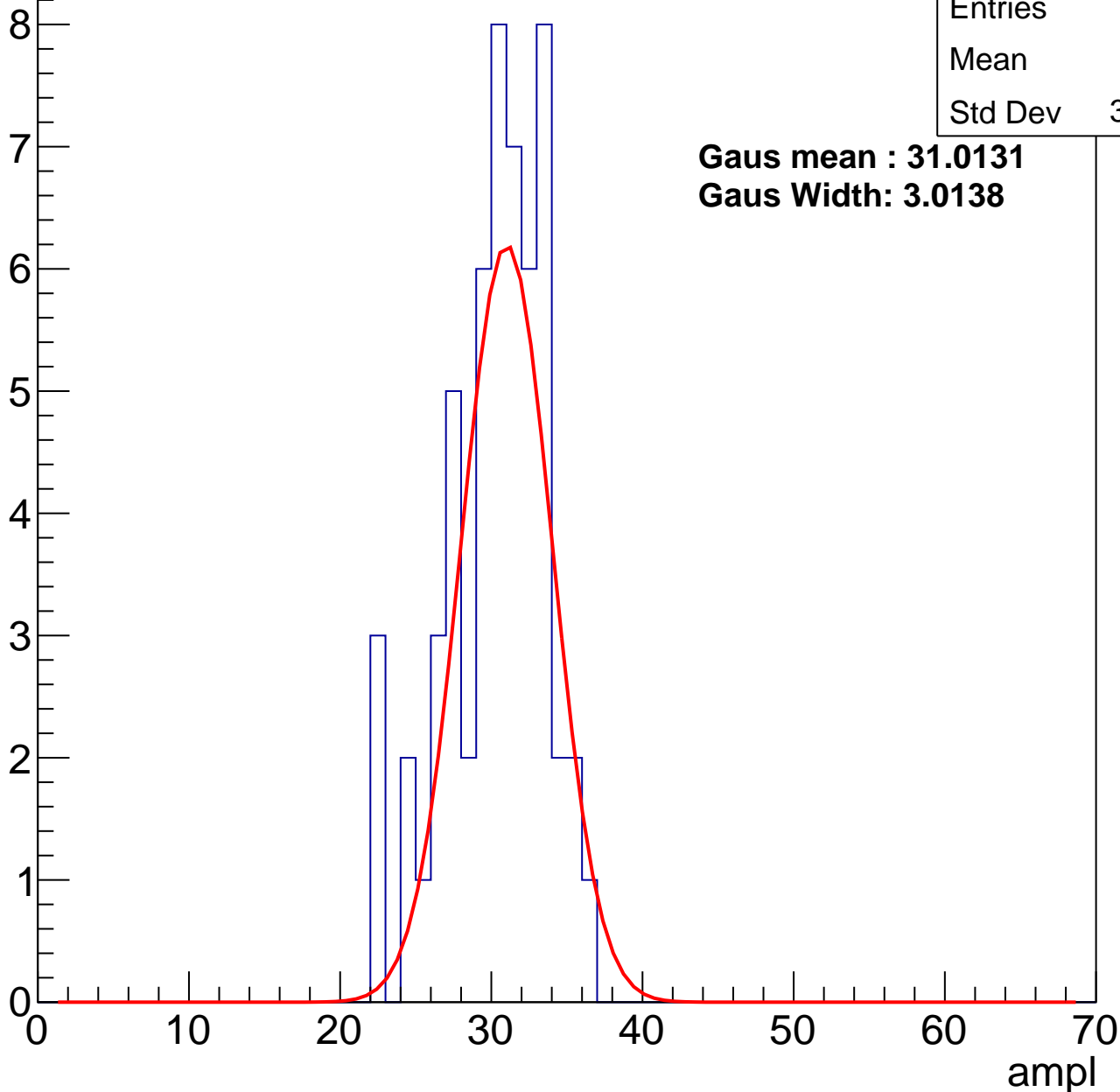
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 56    |
| Mean    | 29.8  |
| Std Dev | 3.313 |

**Gaus mean : 31.0131**

**Gaus Width: 3.0138**



# B0L001S, U2-ch61, adc1

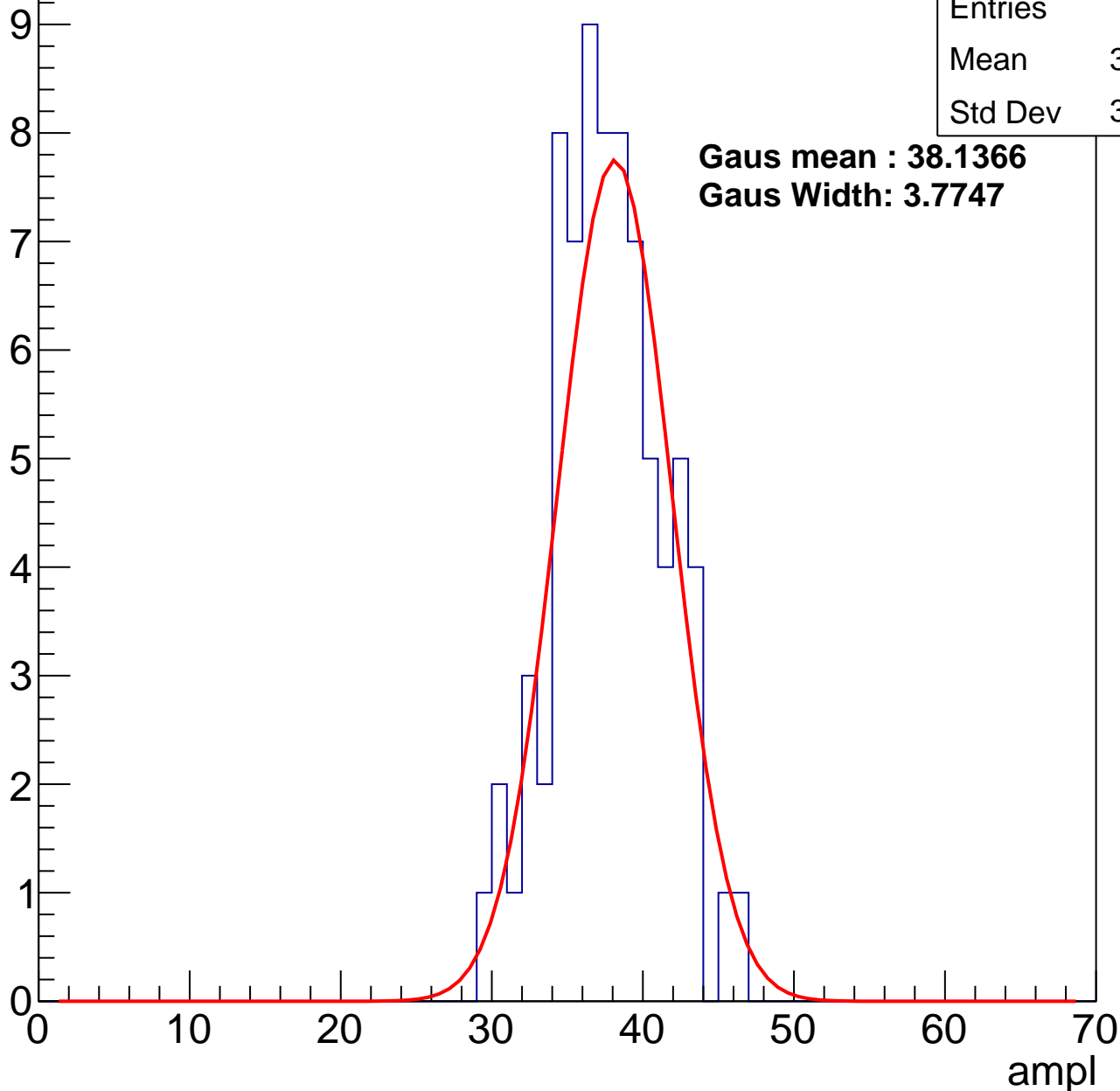
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 76    |
| Mean    | 37.28 |
| Std Dev | 3.567 |

**Gaus mean : 38.1366**

**Gaus Width: 3.7747**



# B0L001S, U2-ch61, adc2

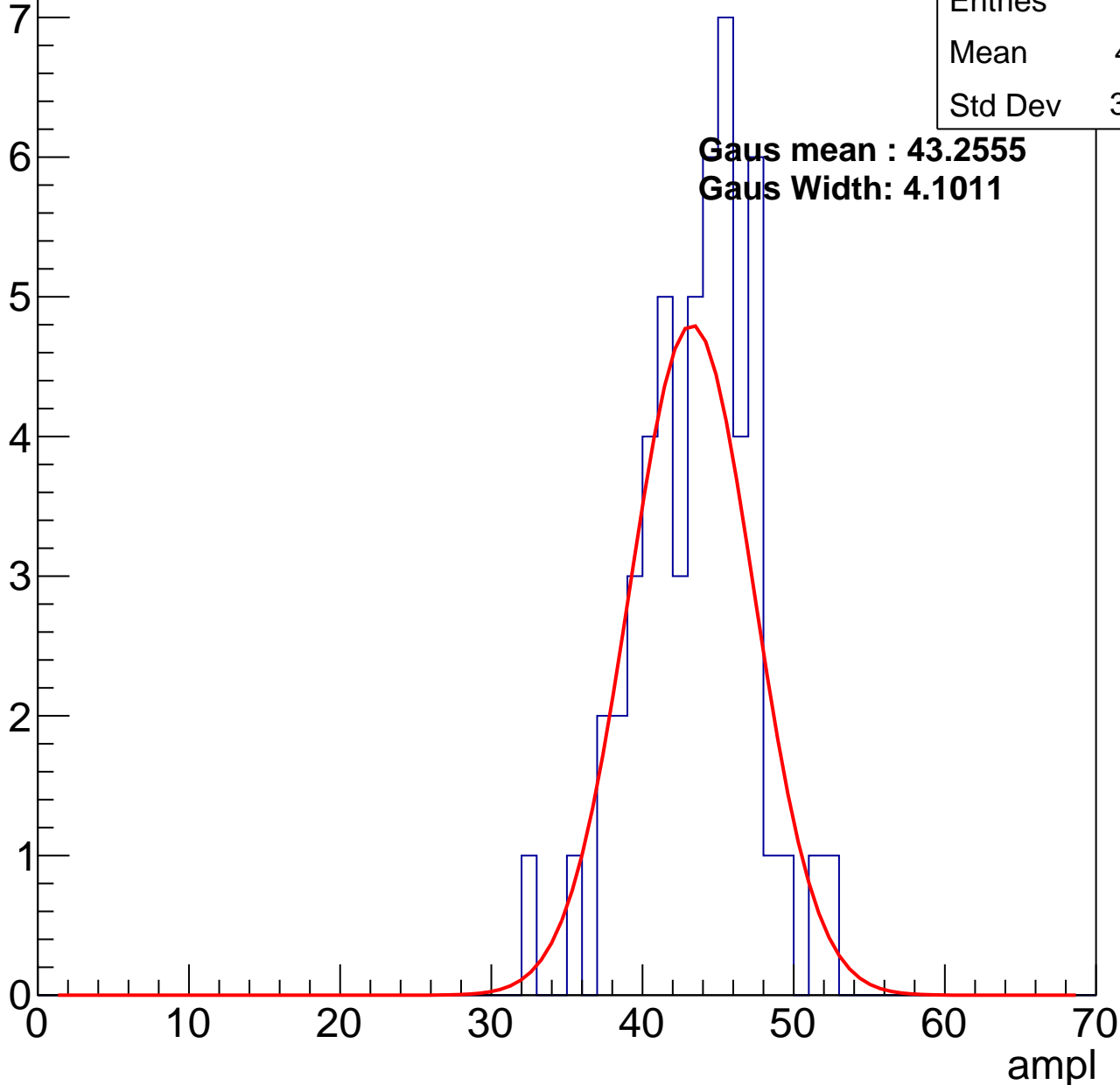
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 53    |
| Mean    | 43.11 |
| Std Dev | 3.849 |

**Gaus mean : 43.2555**

**Gaus Width: 4.1011**

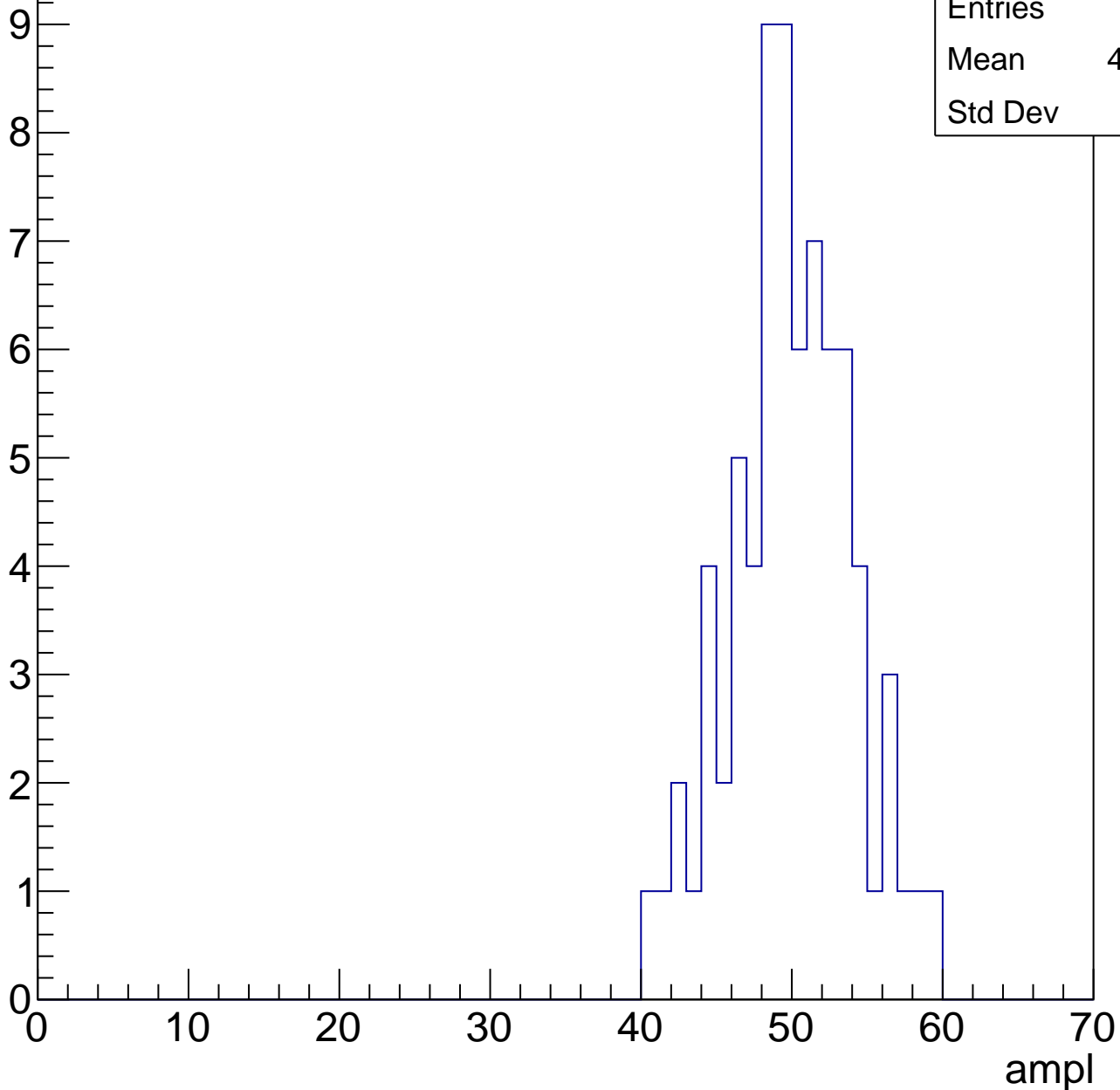


# B0L001S, U2-ch61, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 74    |
| Mean    | 49.53 |
| Std Dev | 3.98  |

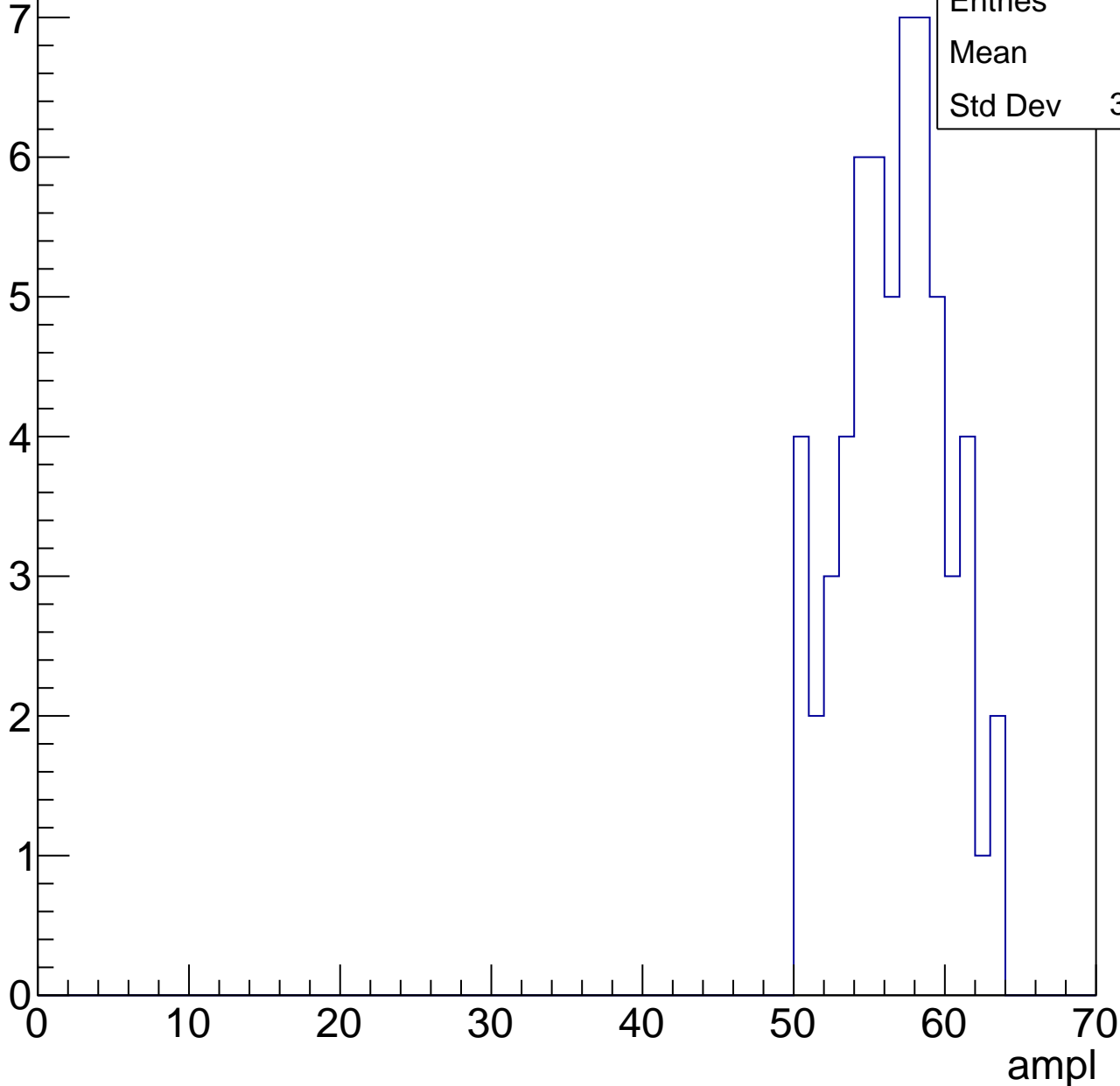


# B0L001S, U2-ch61, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

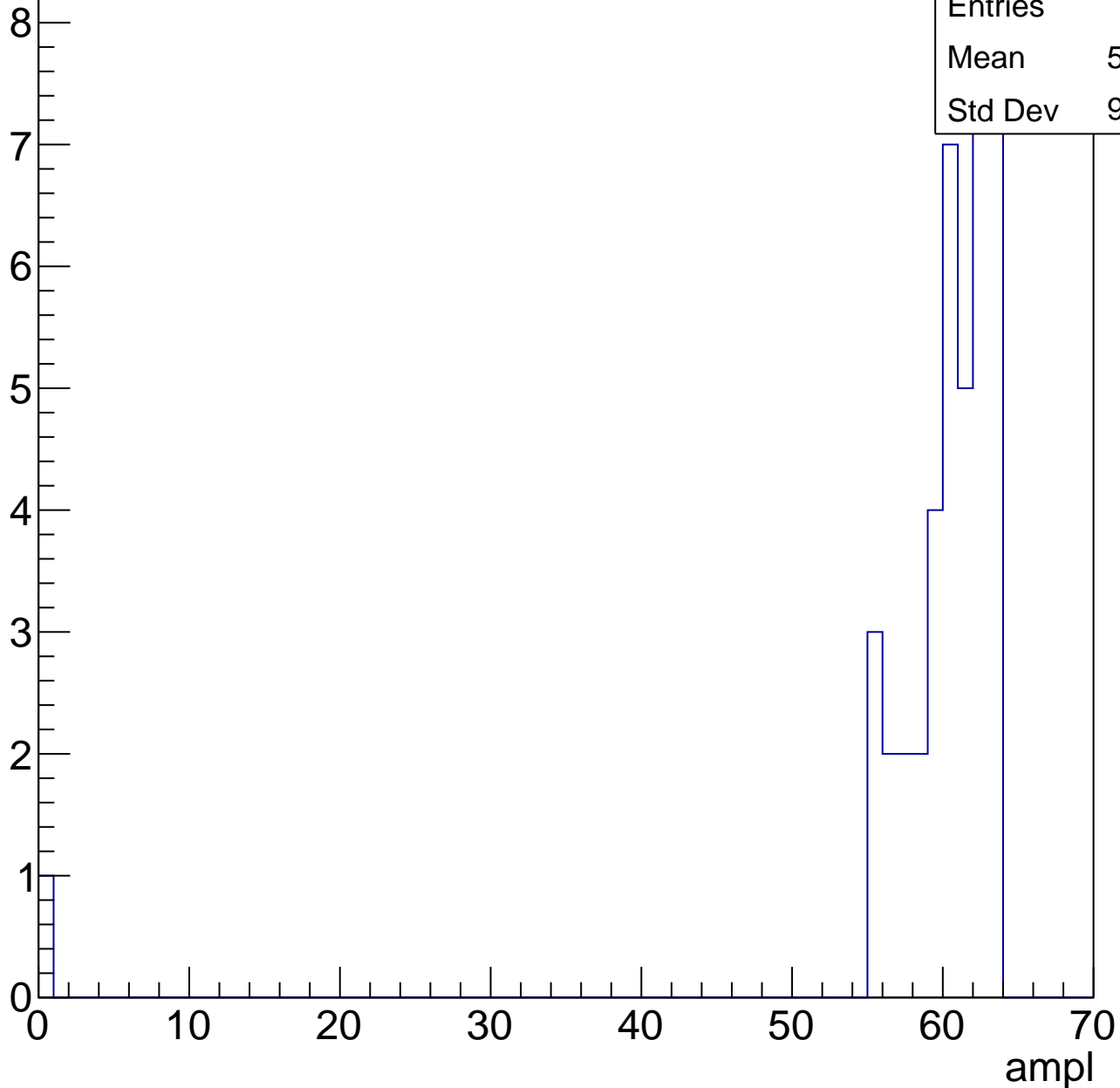
|         |       |
|---------|-------|
| Entries | 59    |
| Mean    | 56.2  |
| Std Dev | 3.364 |



# B0L001S, U2-ch61, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U2-ch61, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch61, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 0 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch62, adc0

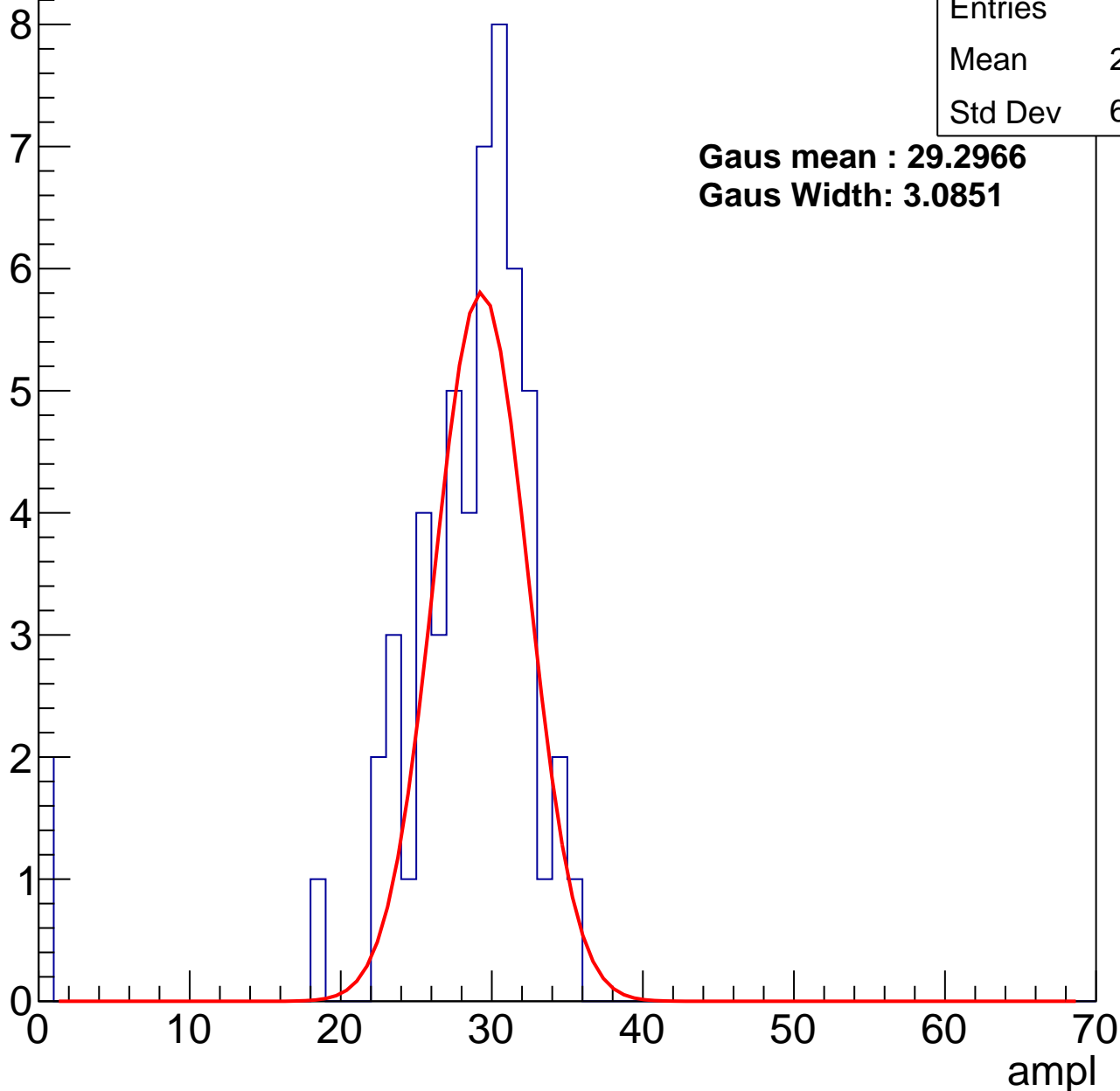
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 55    |
| Mean    | 27.36 |
| Std Dev | 6.297 |

**Gaus mean : 29.2966**

**Gaus Width: 3.0851**



# B0L001S, U2-ch62, adc1

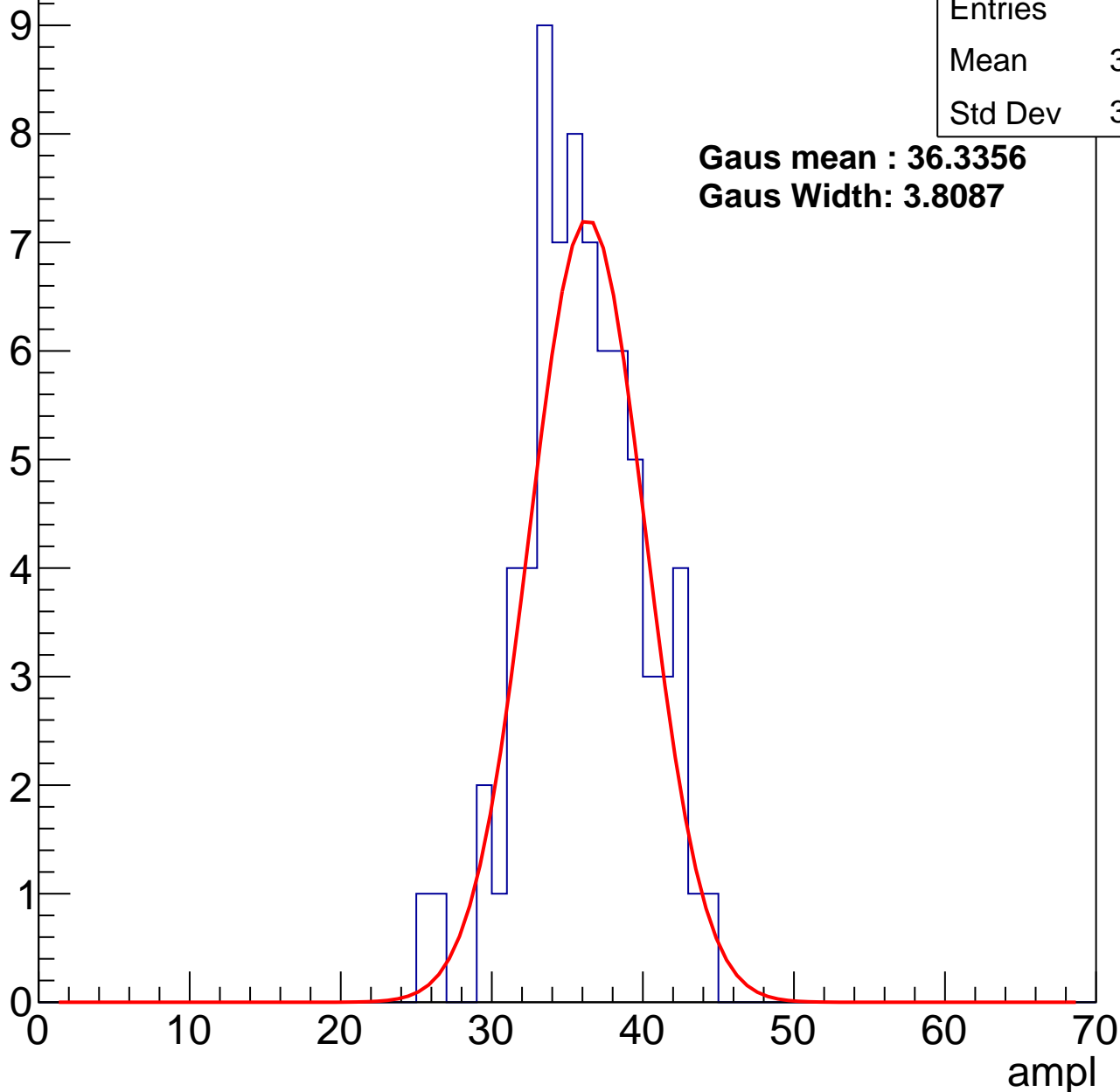
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 73    |
| Mean    | 35.63 |
| Std Dev | 3.848 |

**Gaus mean : 36.3356**

**Gaus Width: 3.8087**



# B0L001S, U2-ch62, adc2

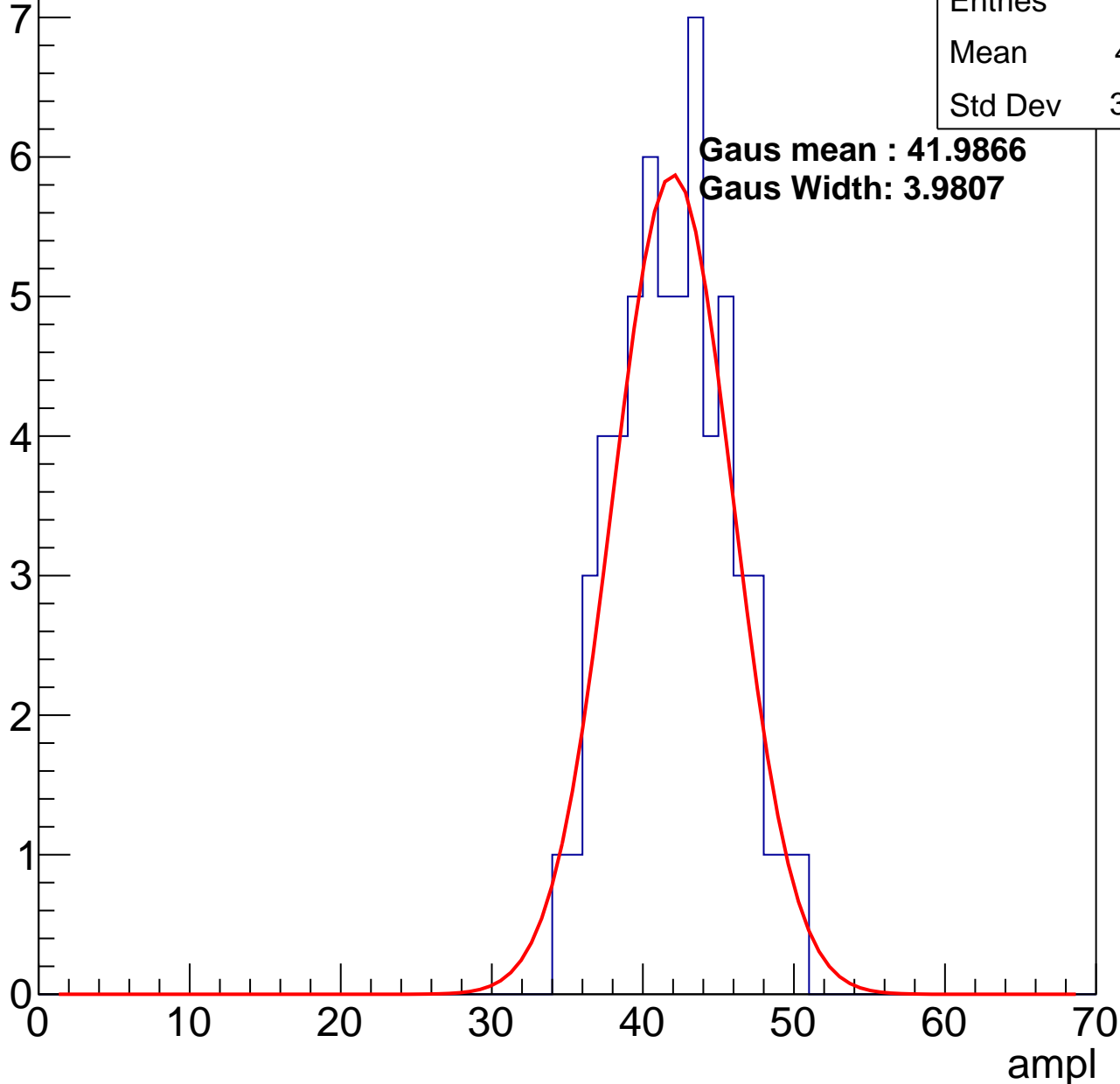
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 59    |
| Mean    | 41.61 |
| Std Dev | 3.659 |

**Gaus mean : 41.9866**

**Gaus Width: 3.9807**

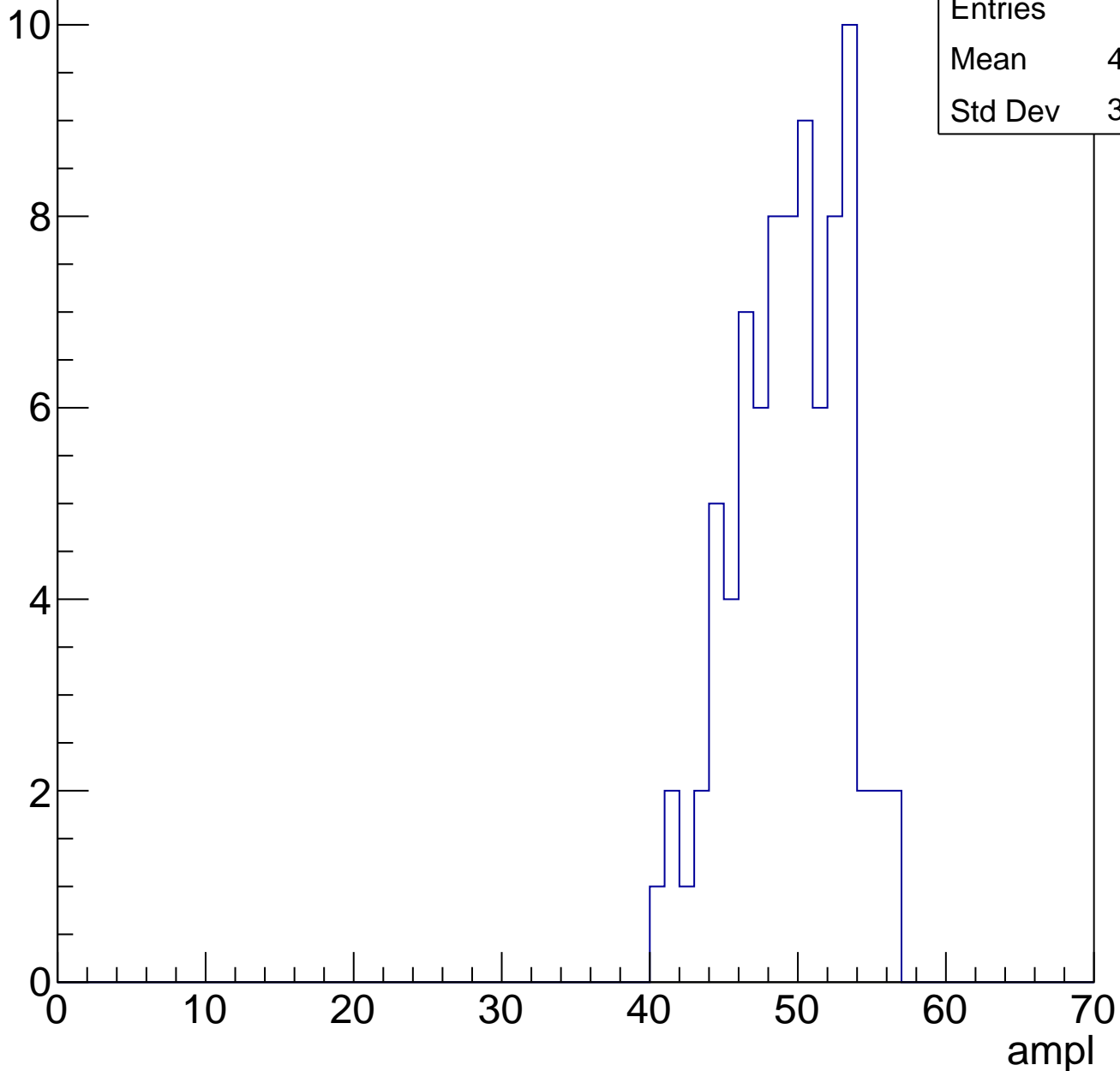


# B0L001S, U2-ch62, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 83    |
| Mean    | 48.94 |
| Std Dev | 3.638 |

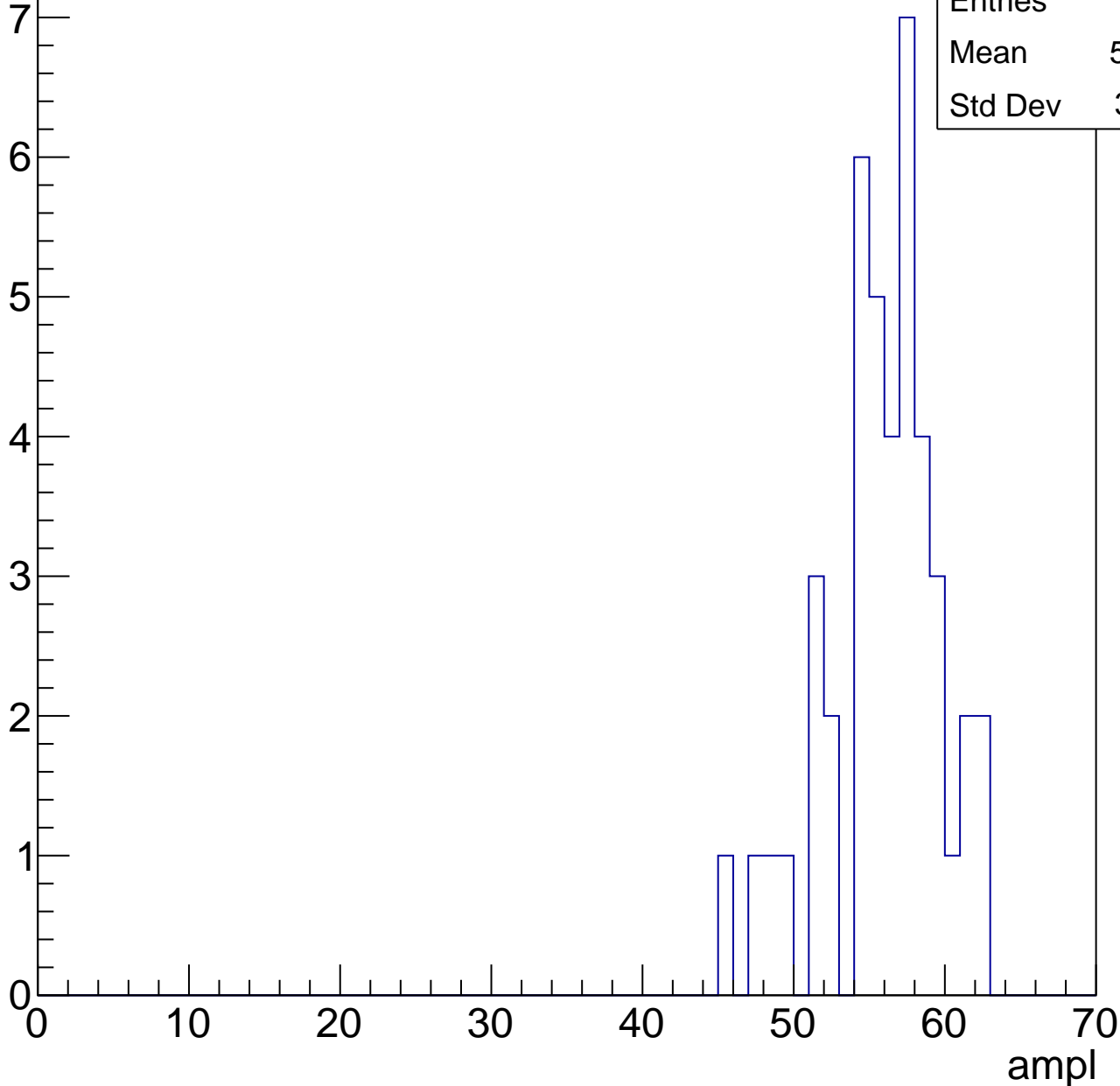


# B0L001S, U2-ch62, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 43    |
| Mean    | 55.42 |
| Std Dev | 3.811 |



# B0L001S, U2-ch62, adc5

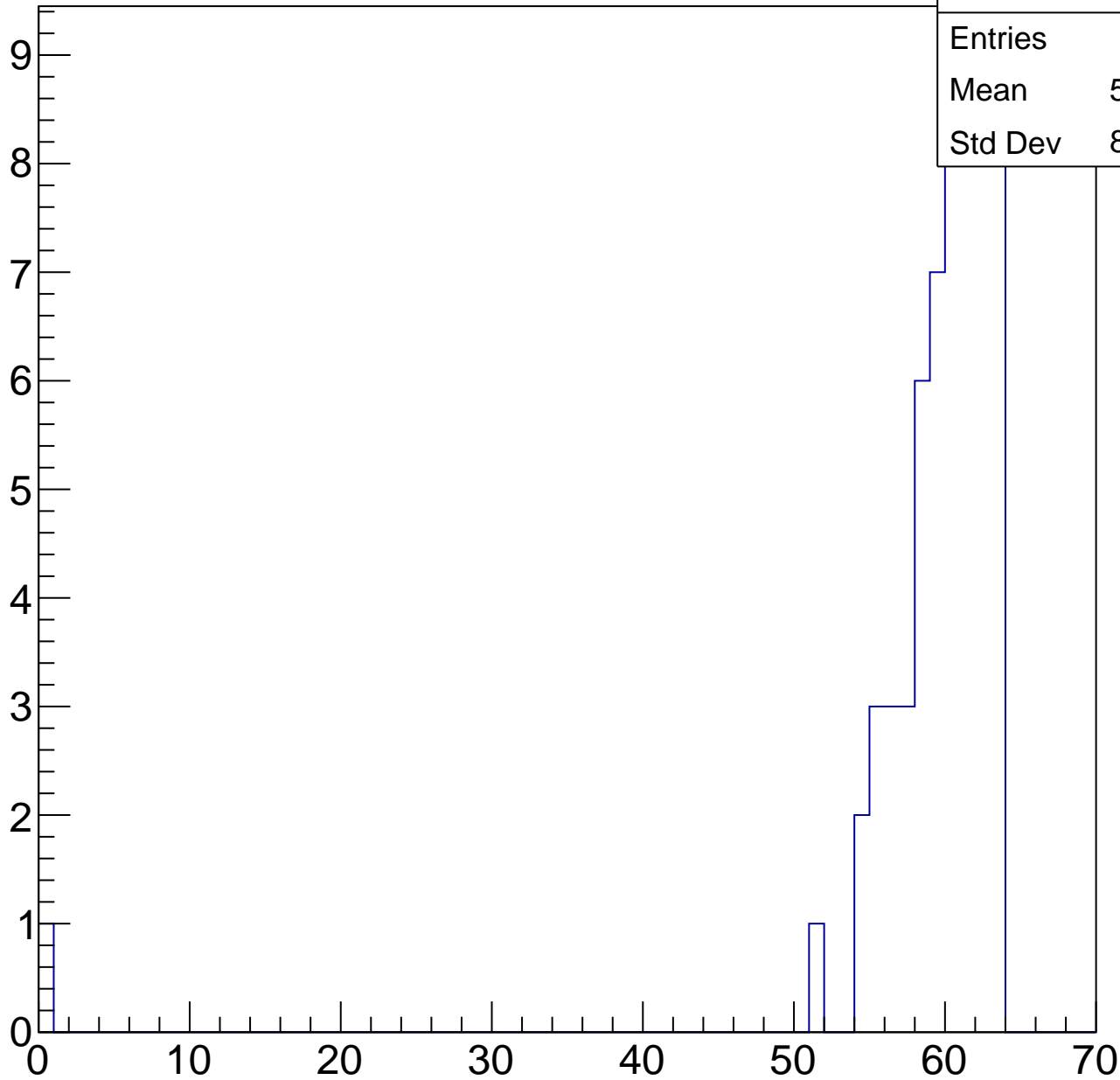
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

|         |       |
|---------|-------|
| Entries | 60    |
| Mean    | 58.58 |
| Std Dev | 8.098 |

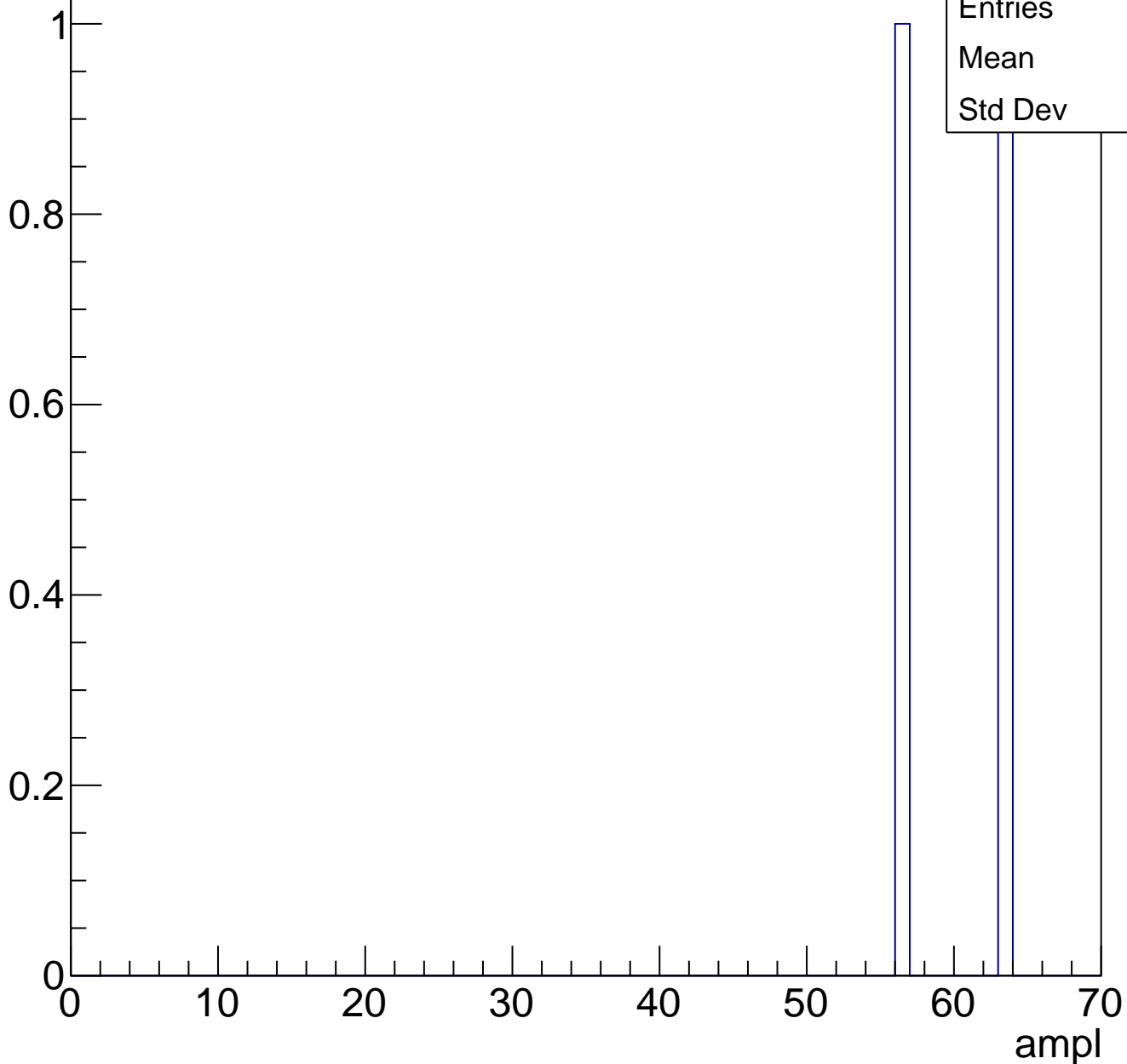
ampl



# B0L001S, U2-ch62, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch62, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 1 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch63, adc0

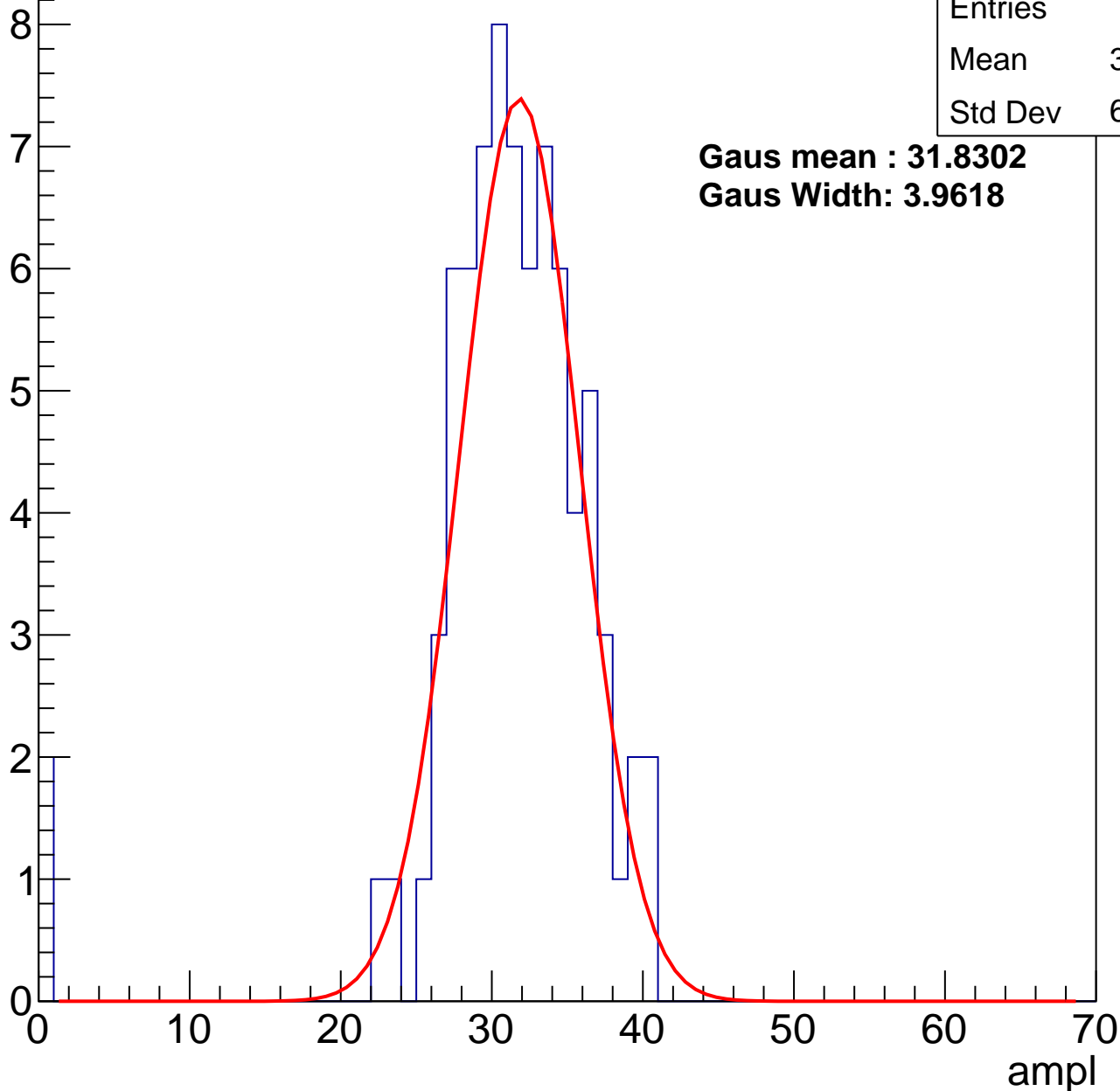
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 78    |
| Mean    | 30.67 |
| Std Dev | 6.283 |

**Gaus mean : 31.8302**

**Gaus Width: 3.9618**



# B0L001S, U2-ch63, adc1

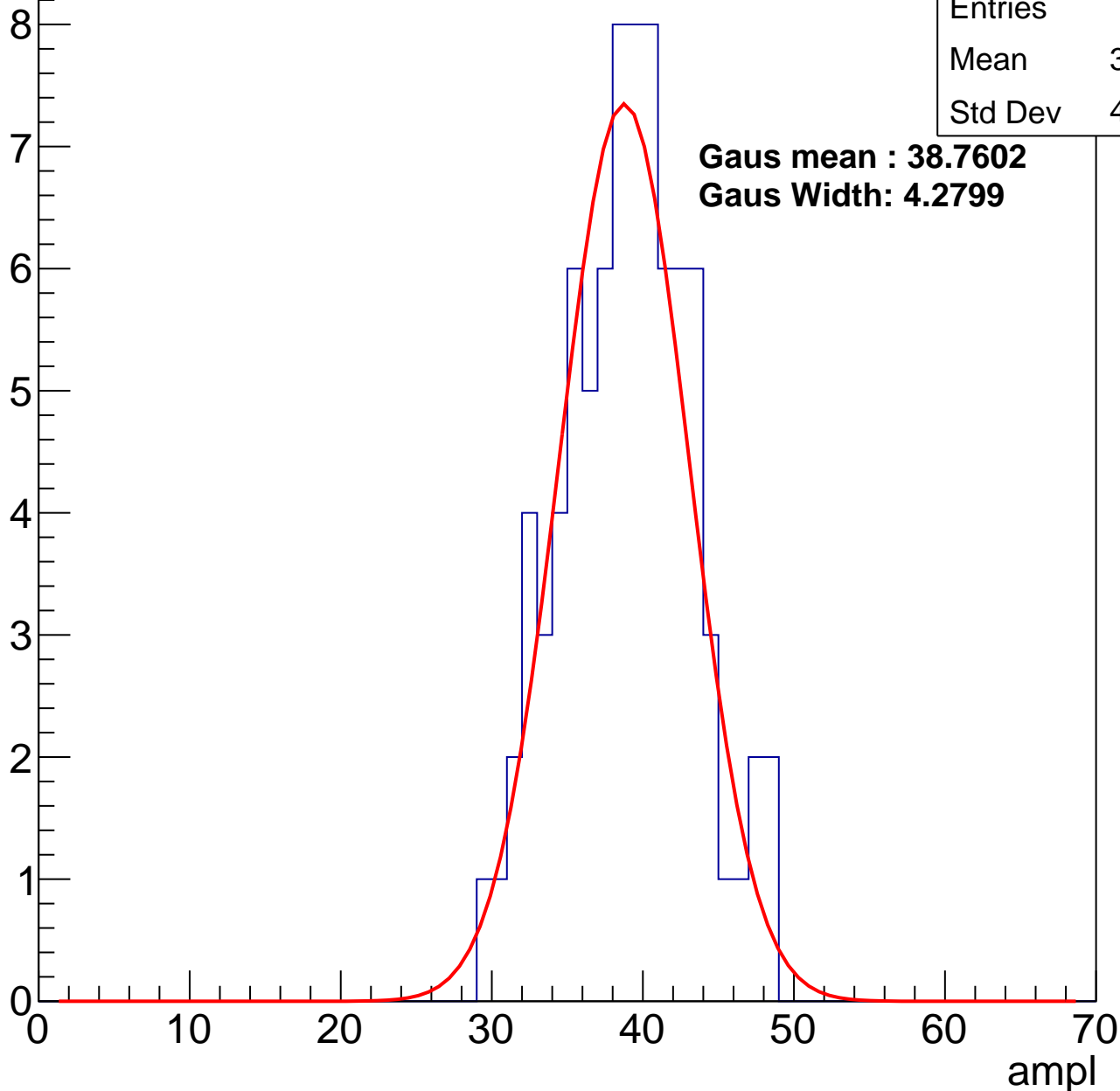
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 83    |
| Mean    | 38.57 |
| Std Dev | 4.255 |

**Gaus mean : 38.7602**

**Gaus Width: 4.2799**



# B0L001S, U2-ch63, adc2

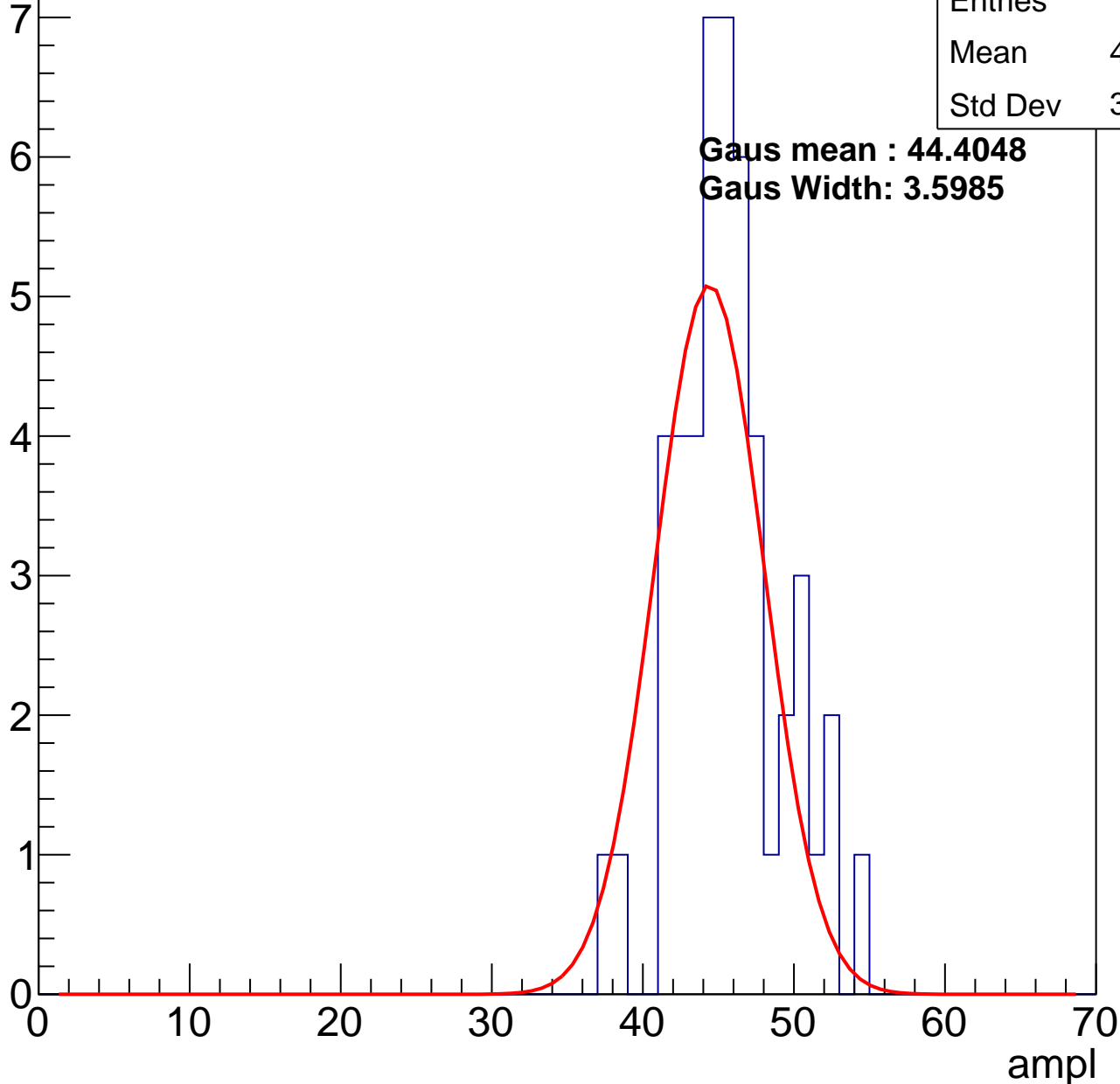
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 48    |
| Mean    | 45.23 |
| Std Dev | 3.495 |

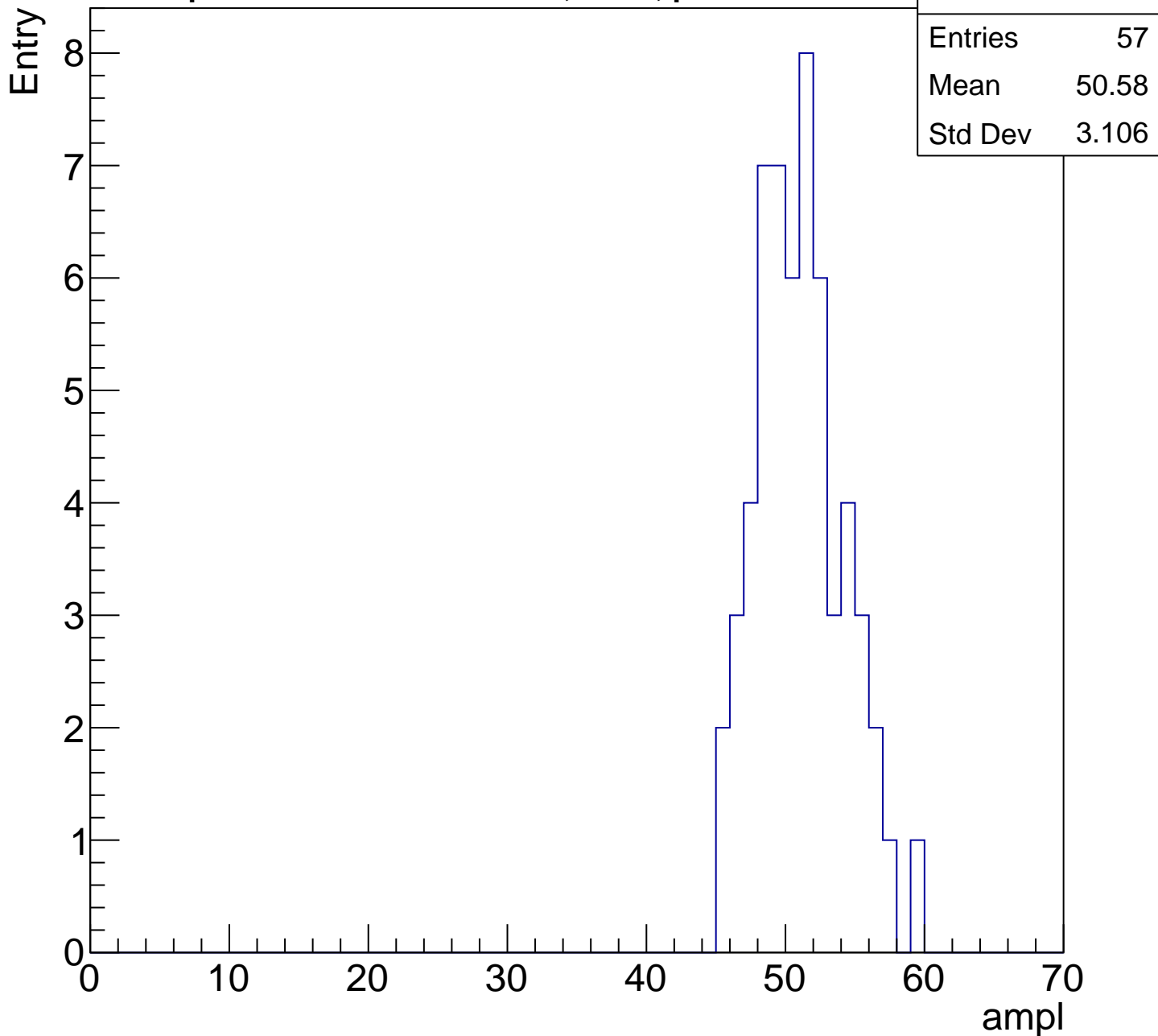
**Gaus mean : 44.4048**

**Gaus Width: 3.5985**



# B0L001S, U2-ch63, adc3

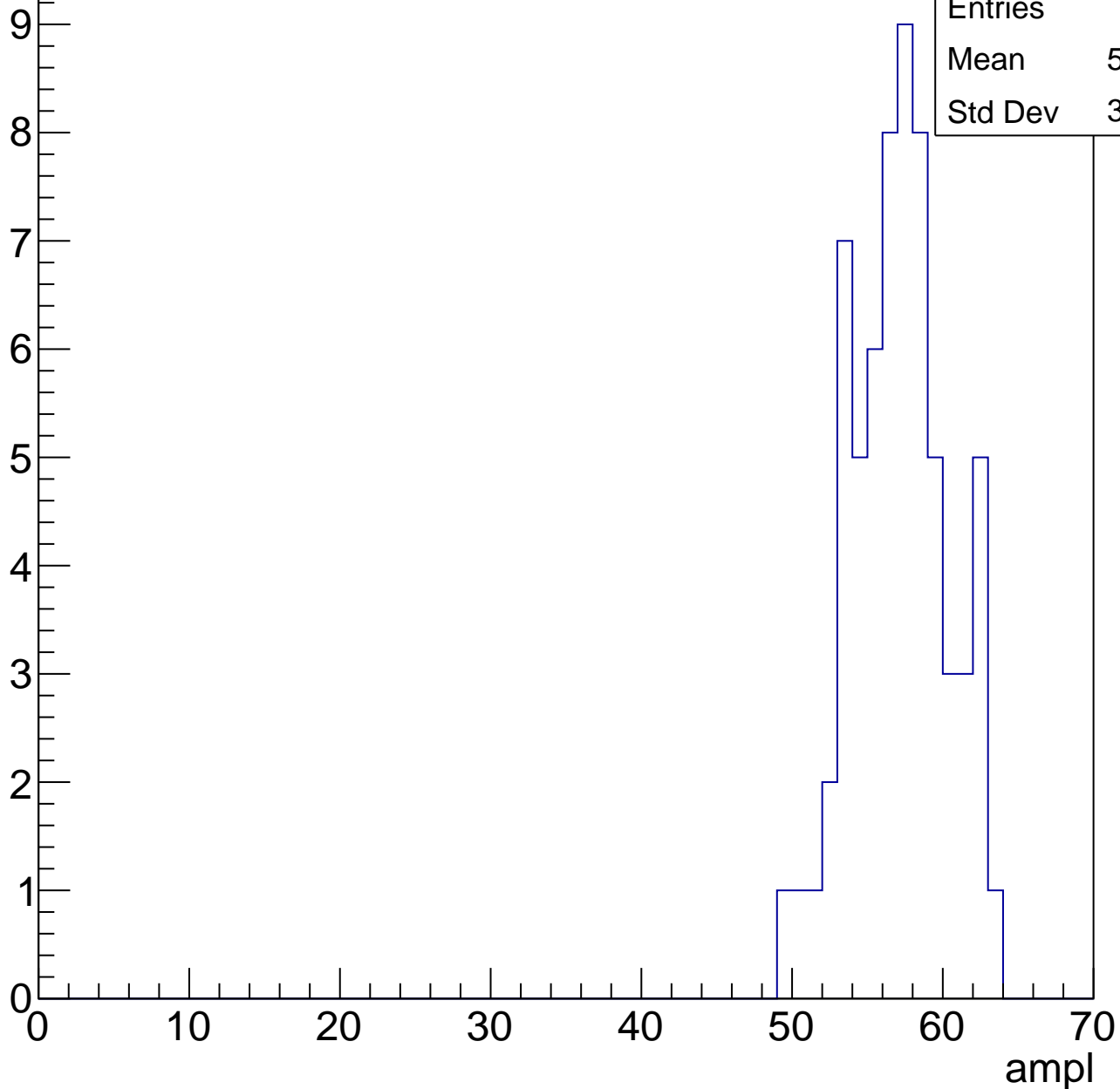
calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U2-ch63, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U2-ch63, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

7

6

5

4

3

2

1

0

|         |       |
|---------|-------|
| Entries | 32    |
| Mean    | 60.75 |
| Std Dev | 1.837 |

10

20

30

40

50

60

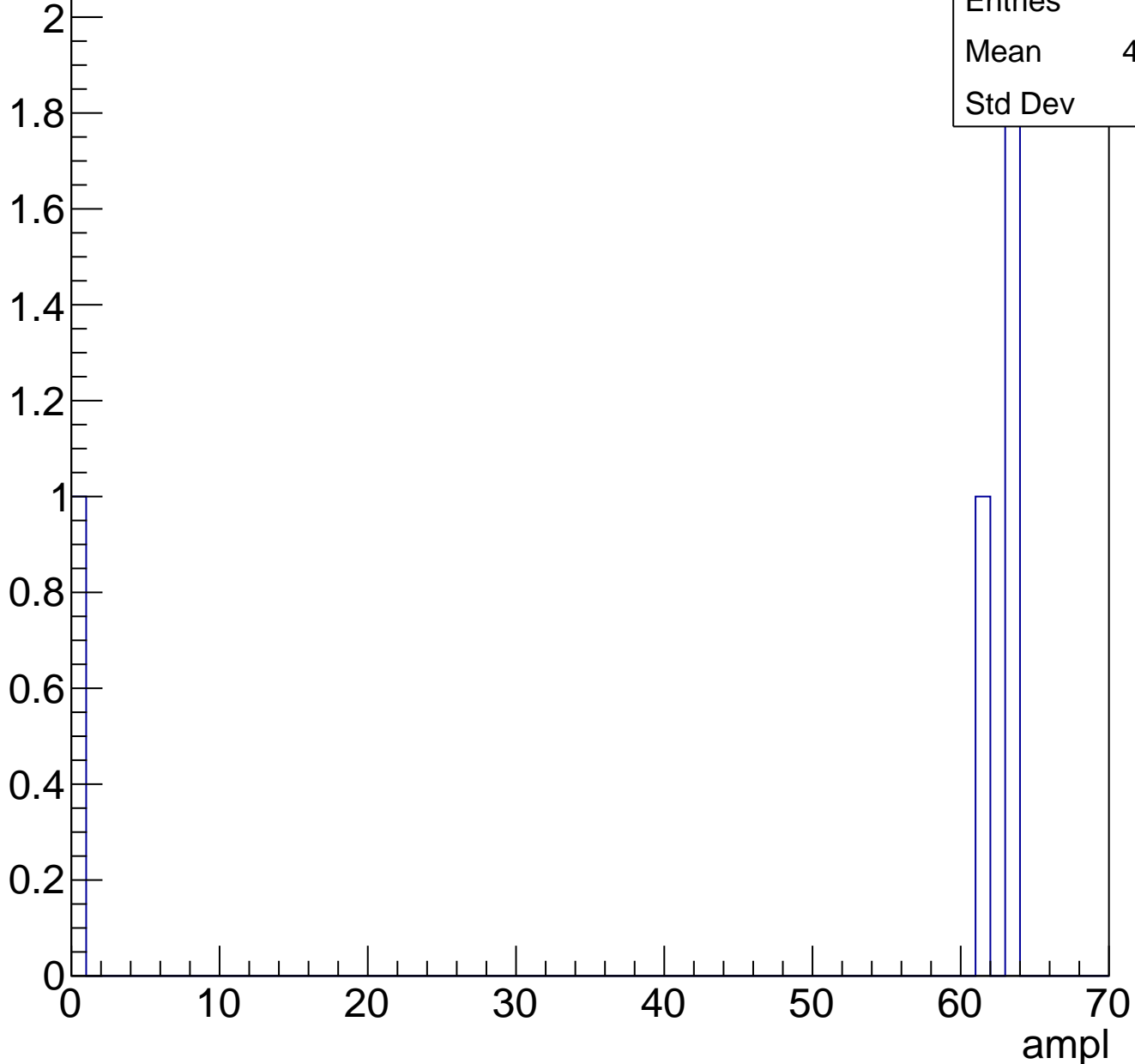
70

ampl

# B0L001S, U2-ch63, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |       |
|---------|-------|
| Entries | 4     |
| Mean    | 46.75 |
| Std Dev | 27    |



# B0L001S, U2-ch63, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 1 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch64, adc0

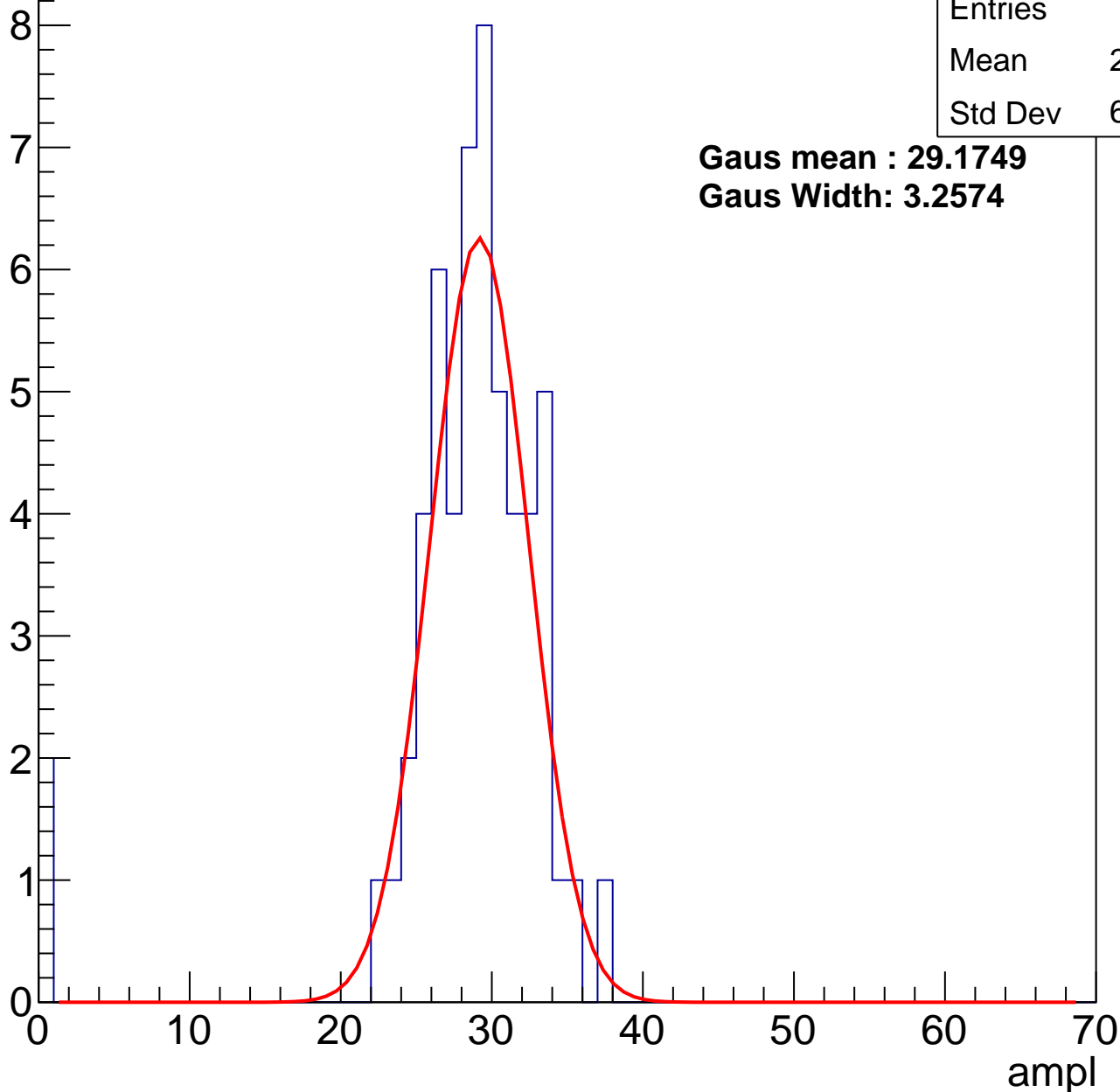
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 56    |
| Mean    | 27.82 |
| Std Dev | 6.185 |

**Gaus mean : 29.1749**

**Gaus Width: 3.2574**



# B0L001S, U2-ch64, adc1

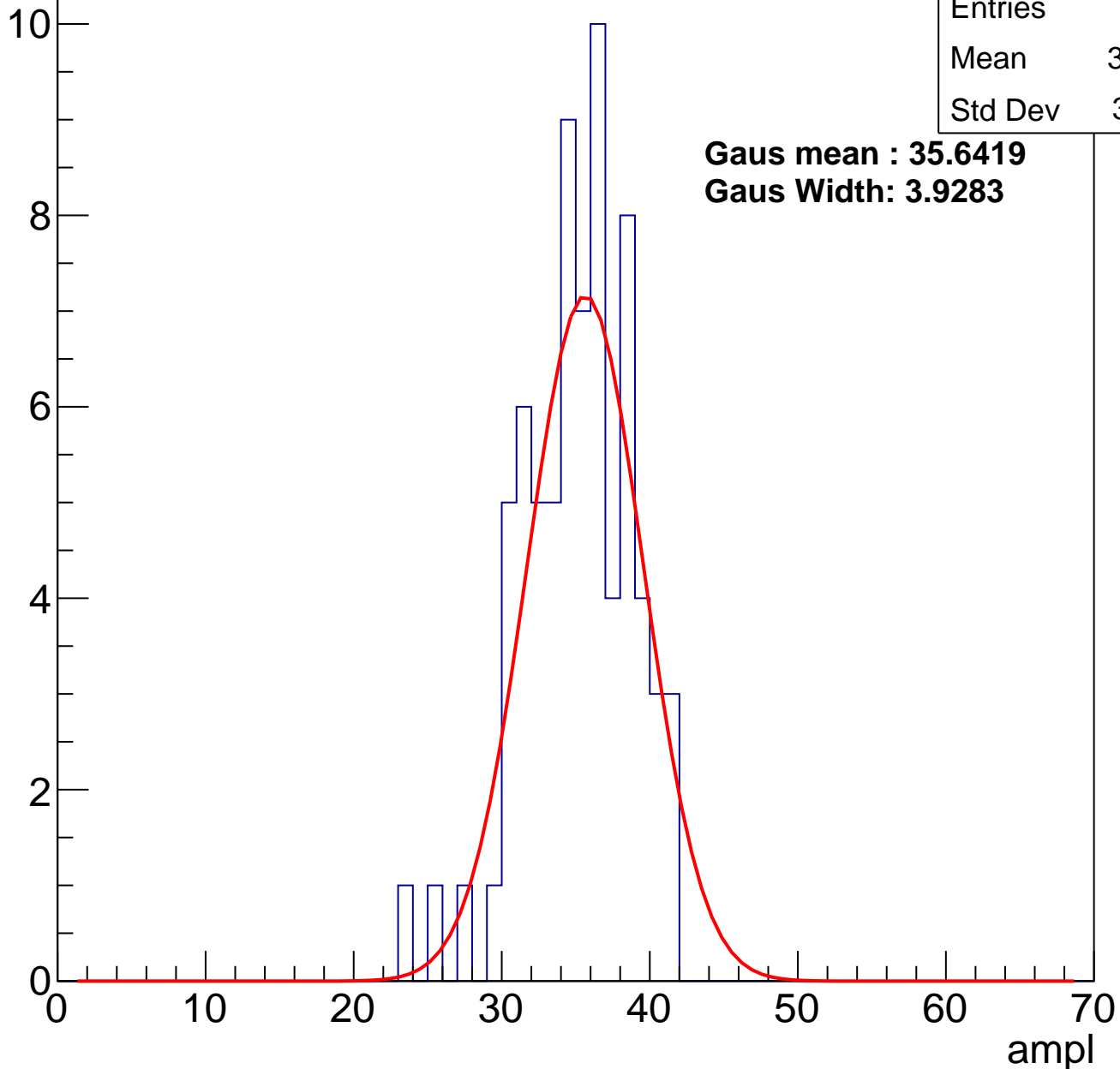
calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 73    |
| Mean    | 34.62 |
| Std Dev | 3.651 |

**Gaus mean : 35.6419**

**Gaus Width: 3.9283**

Entry



# B0L001S, U2-ch64, adc2

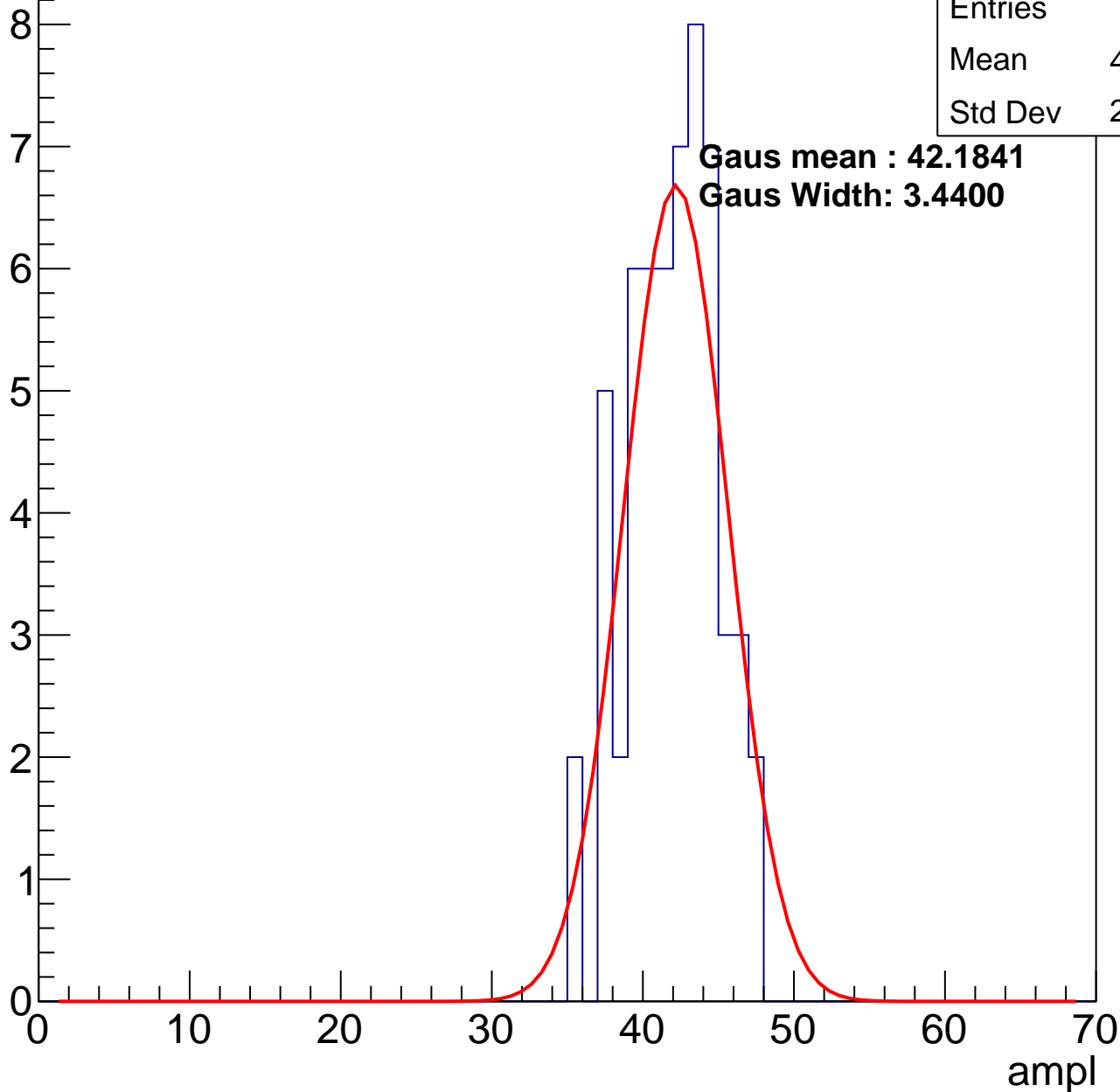
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 57    |
| Mean    | 41.47 |
| Std Dev | 2.915 |

**Gaus mean : 42.1841**

**Gaus Width: 3.4400**

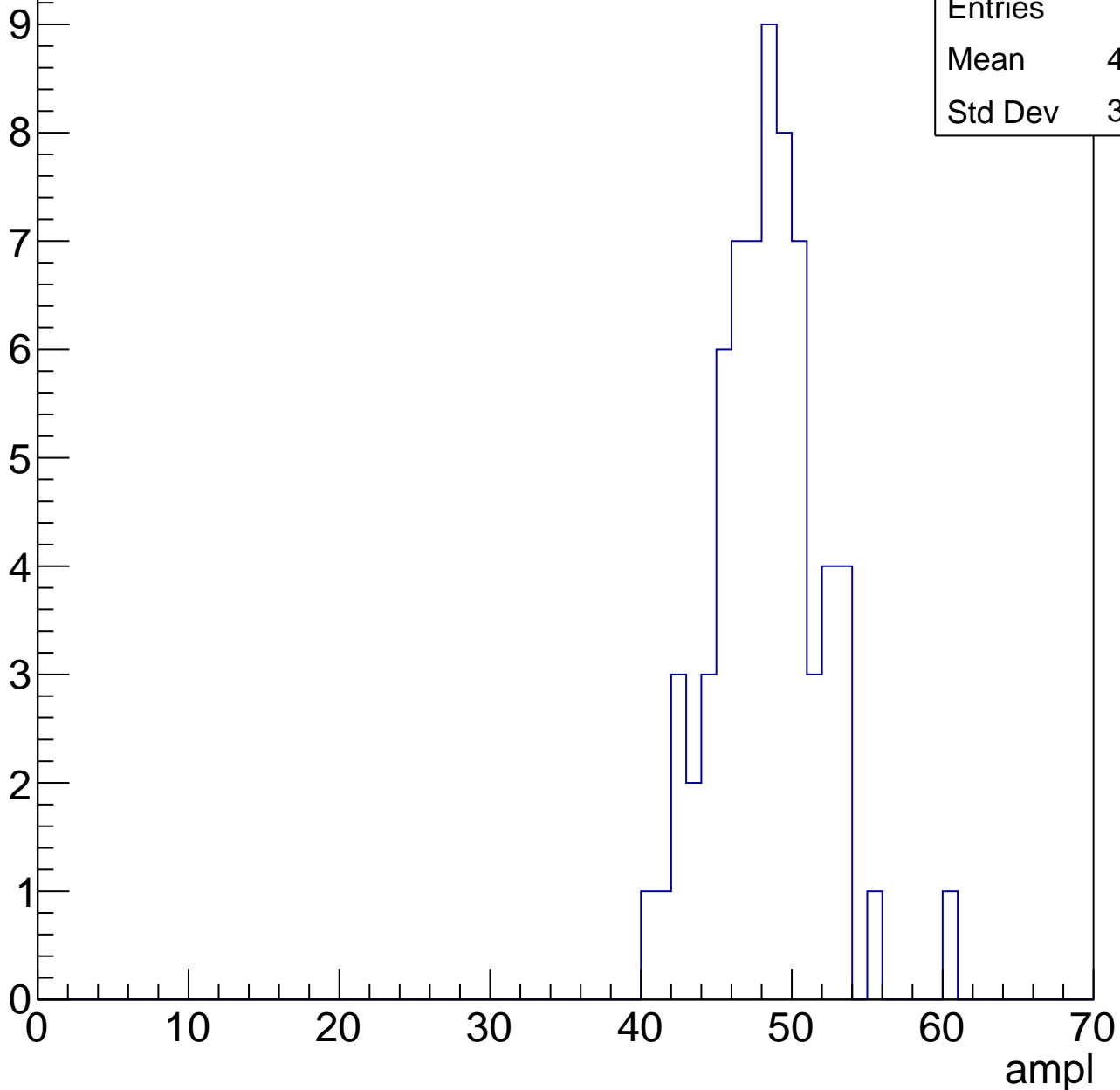


# B0L001S, U2-ch64, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 67    |
| Mean    | 47.88 |
| Std Dev | 3.513 |

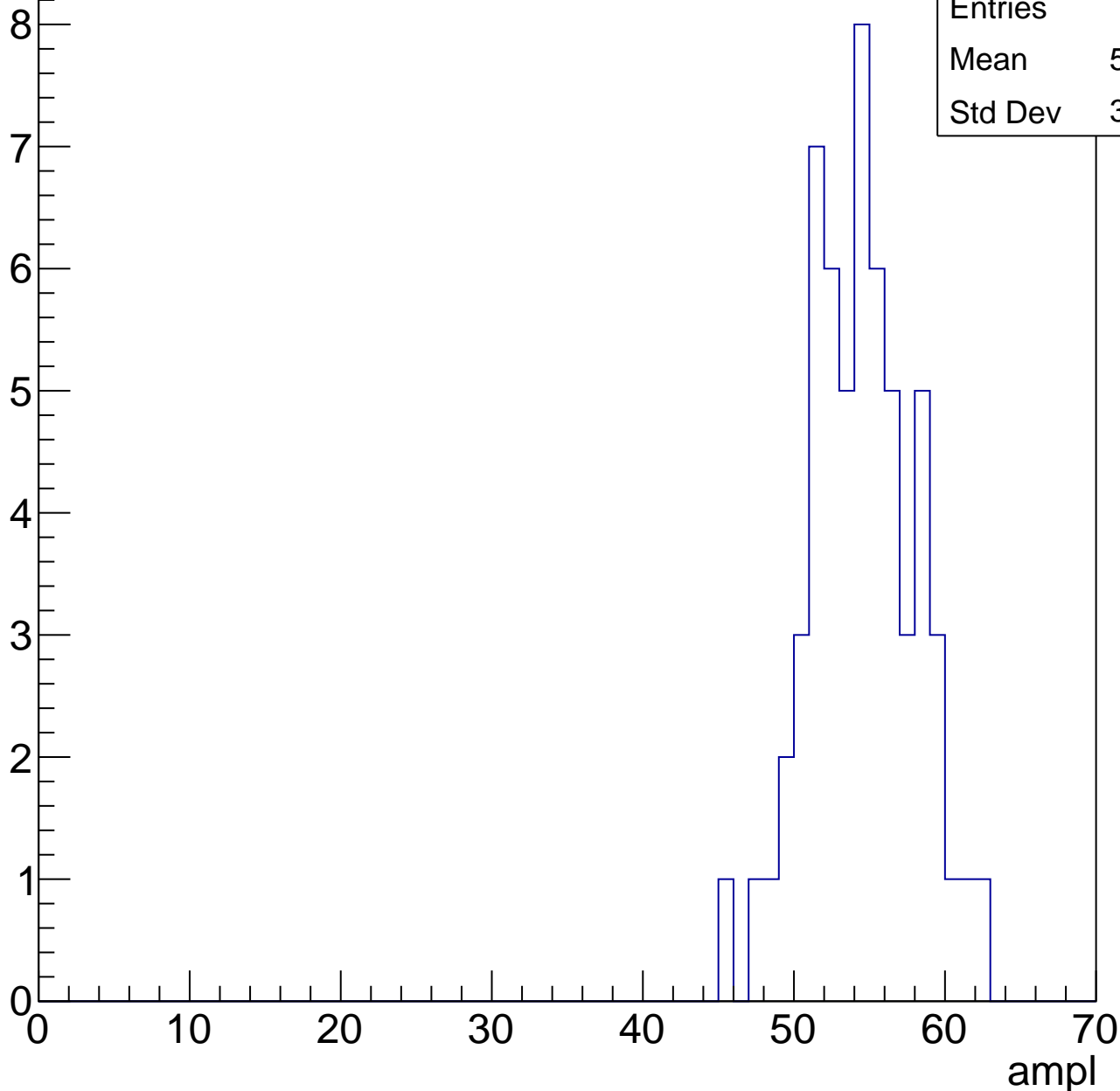


# B0L001S, U2-ch64, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 59    |
| Mean    | 53.98 |
| Std Dev | 3.476 |



# B0L001S, U2-ch64, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

7

6

5

4

3

2

1

0

|         |       |
|---------|-------|
| Entries | 49    |
| Mean    | 57.53 |
| Std Dev | 8.713 |

ampl

0

10

20

30

40

50

60

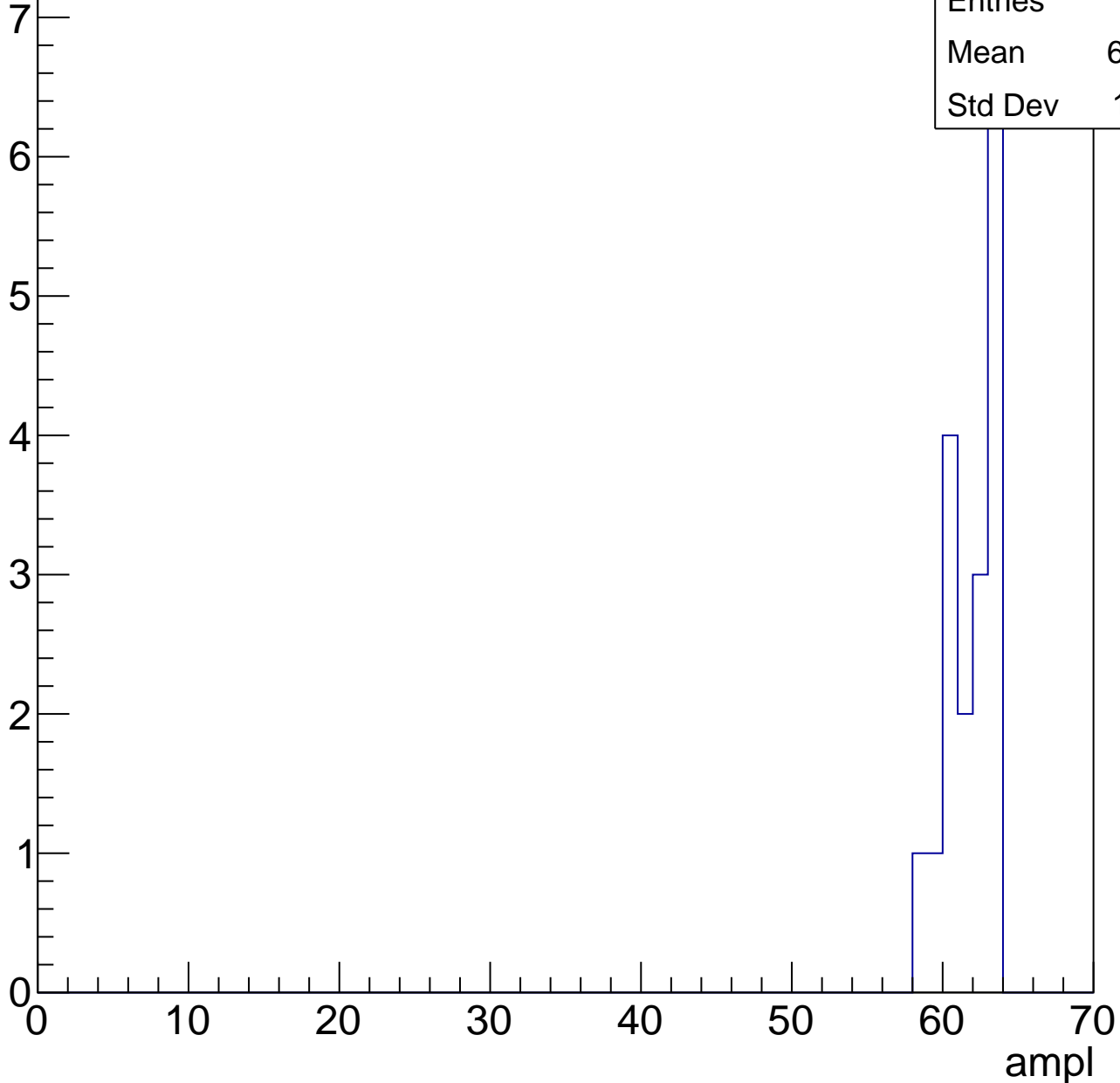
70

# B0L001S, U2-ch64, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 18    |
| Mean    | 61.44 |
| Std Dev | 1.571 |





# B0L001S, U2-ch64, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U2-ch65, adc0

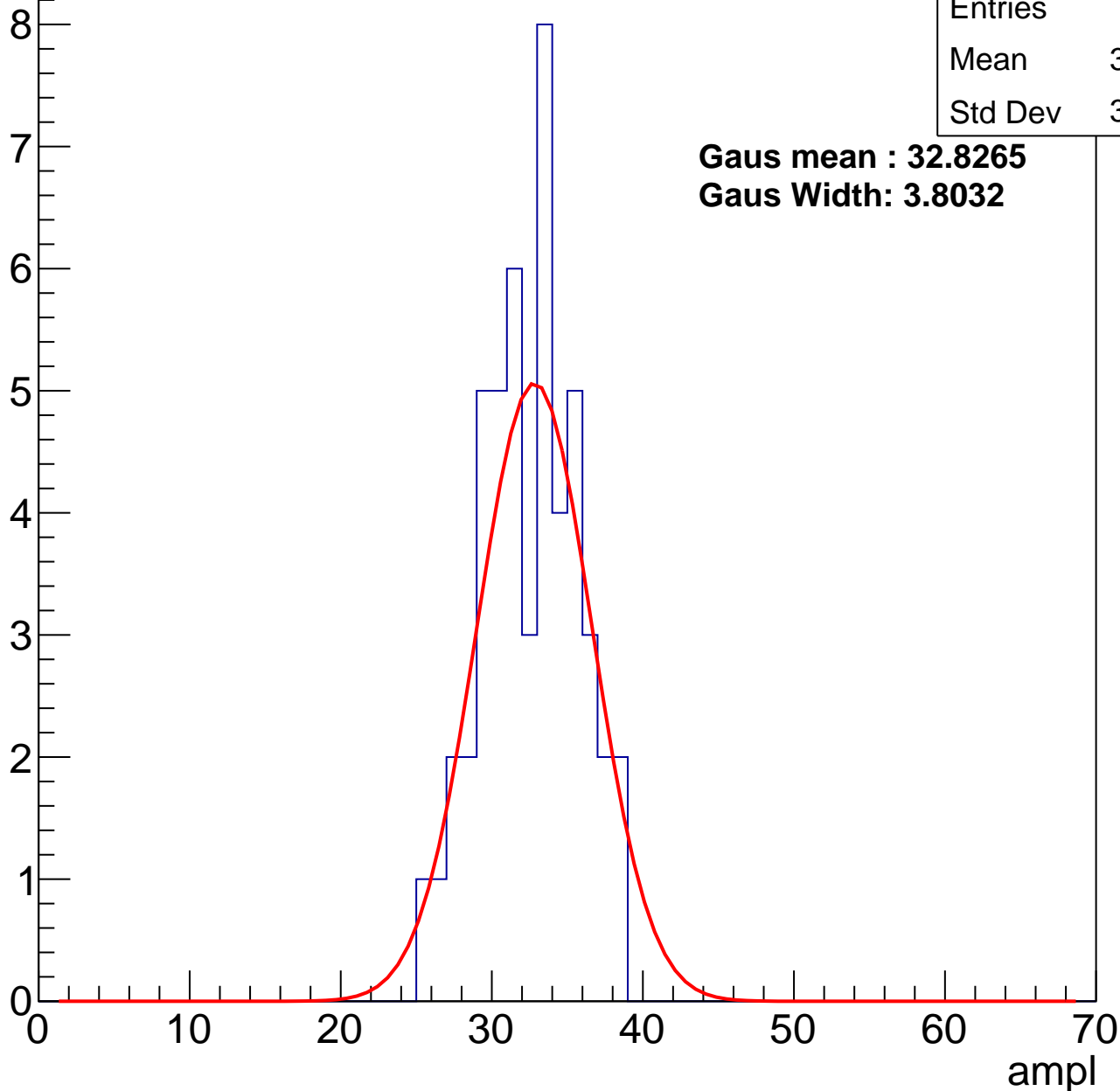
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 49    |
| Mean    | 32.06 |
| Std Dev | 3.119 |

**Gaus mean : 32.8265**

**Gaus Width: 3.8032**



# B0L001S, U2-ch65, adc1

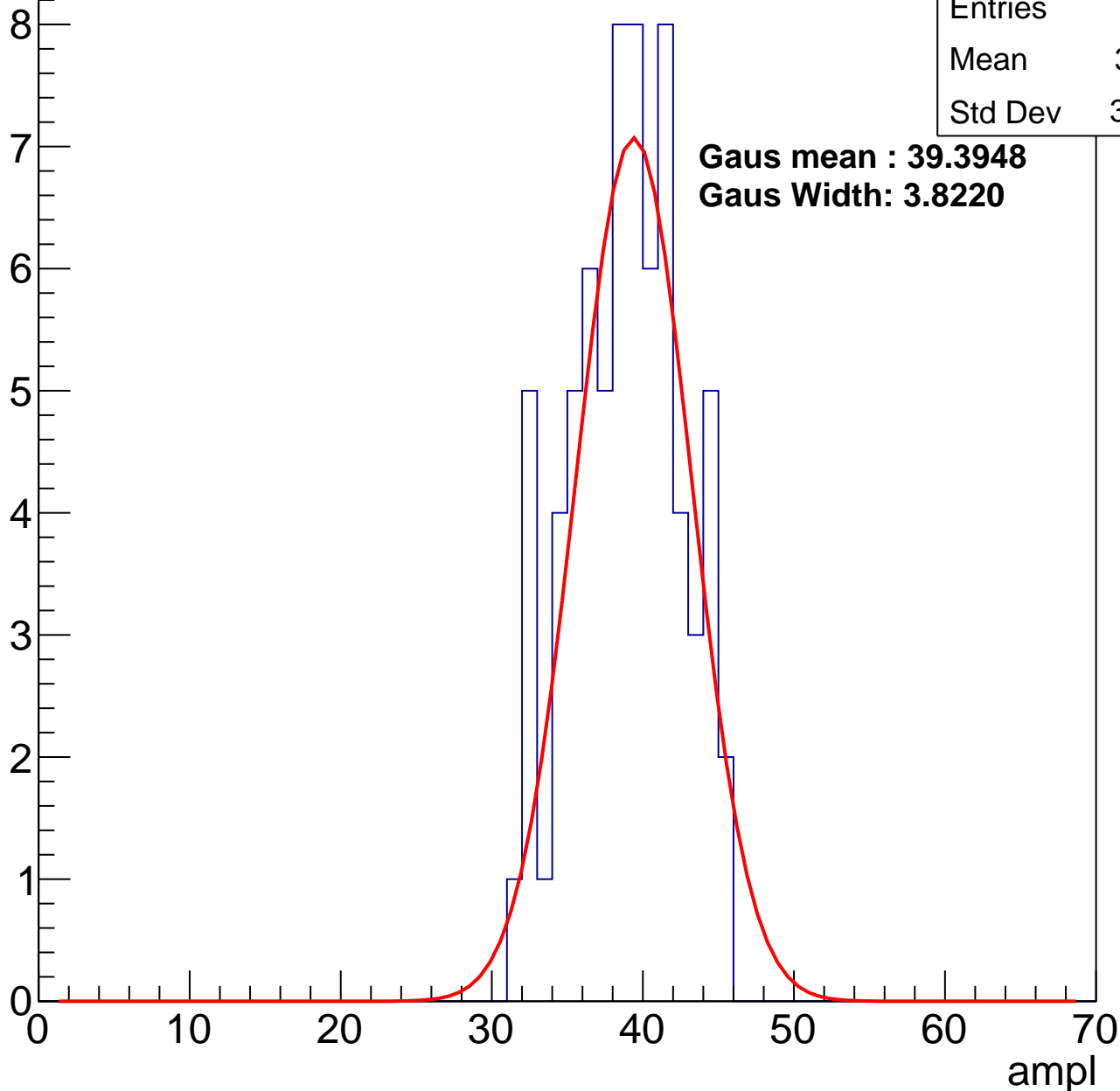
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 71    |
| Mean    | 38.41 |
| Std Dev | 3.563 |

**Gaus mean : 39.3948**

**Gaus Width: 3.8220**



# B0L001S, U2-ch65, adc2

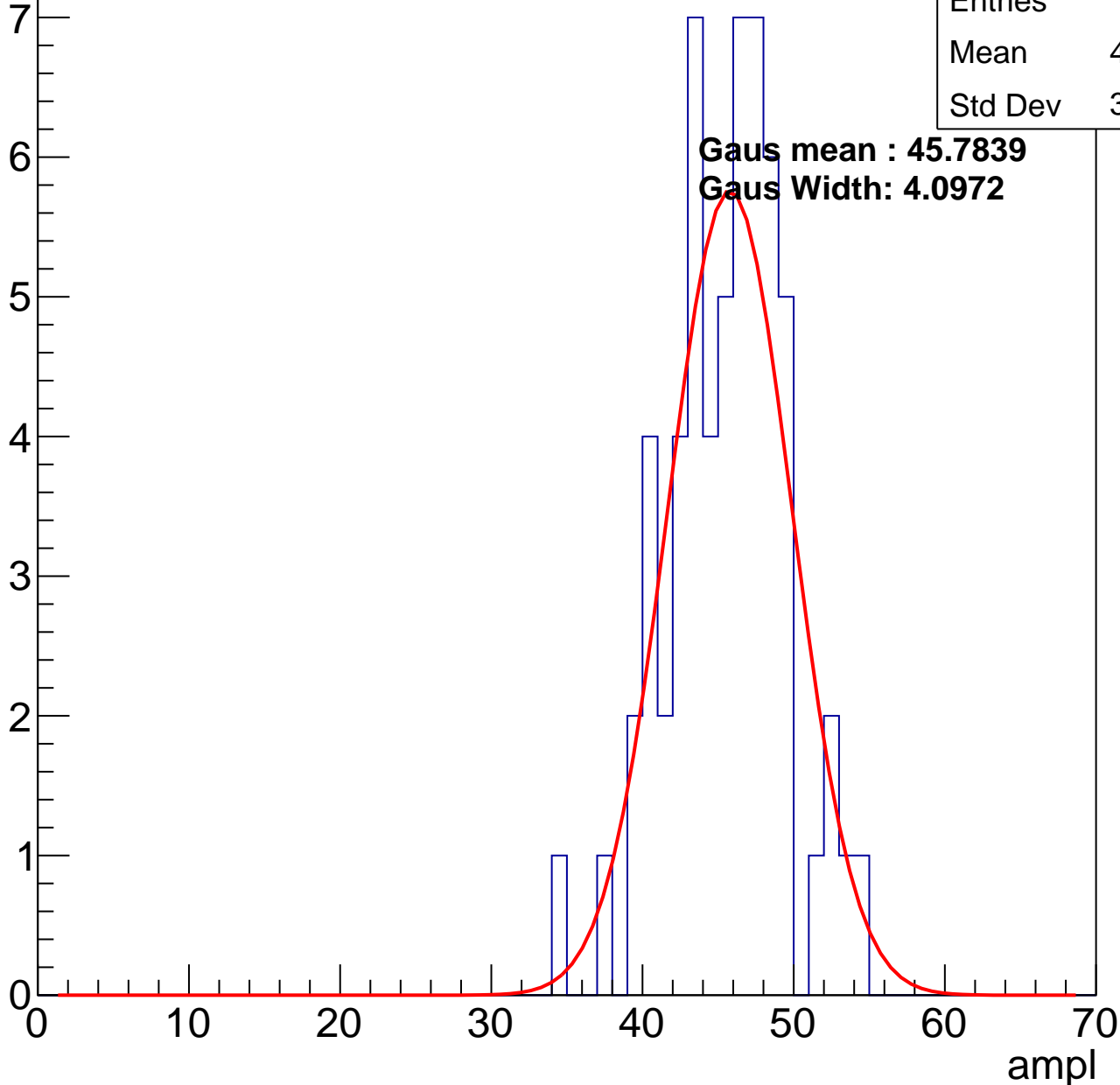
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 60    |
| Mean    | 45.12 |
| Std Dev | 3.882 |

**Gaus mean : 45.7839**

**Gaus Width: 4.0972**

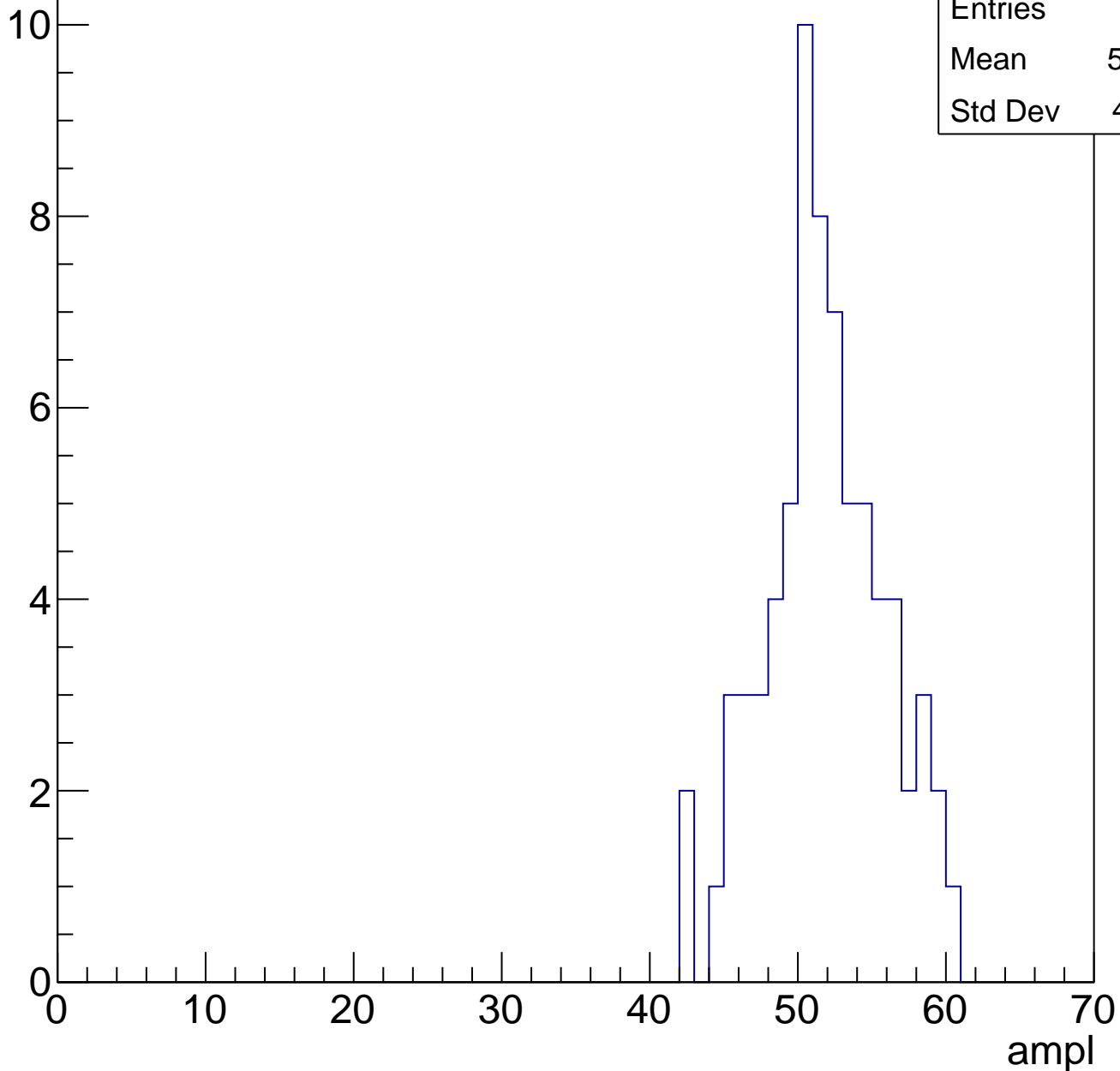


# B0L001S, U2-ch65, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 72    |
| Mean    | 51.33 |
| Std Dev | 4.021 |

Entry

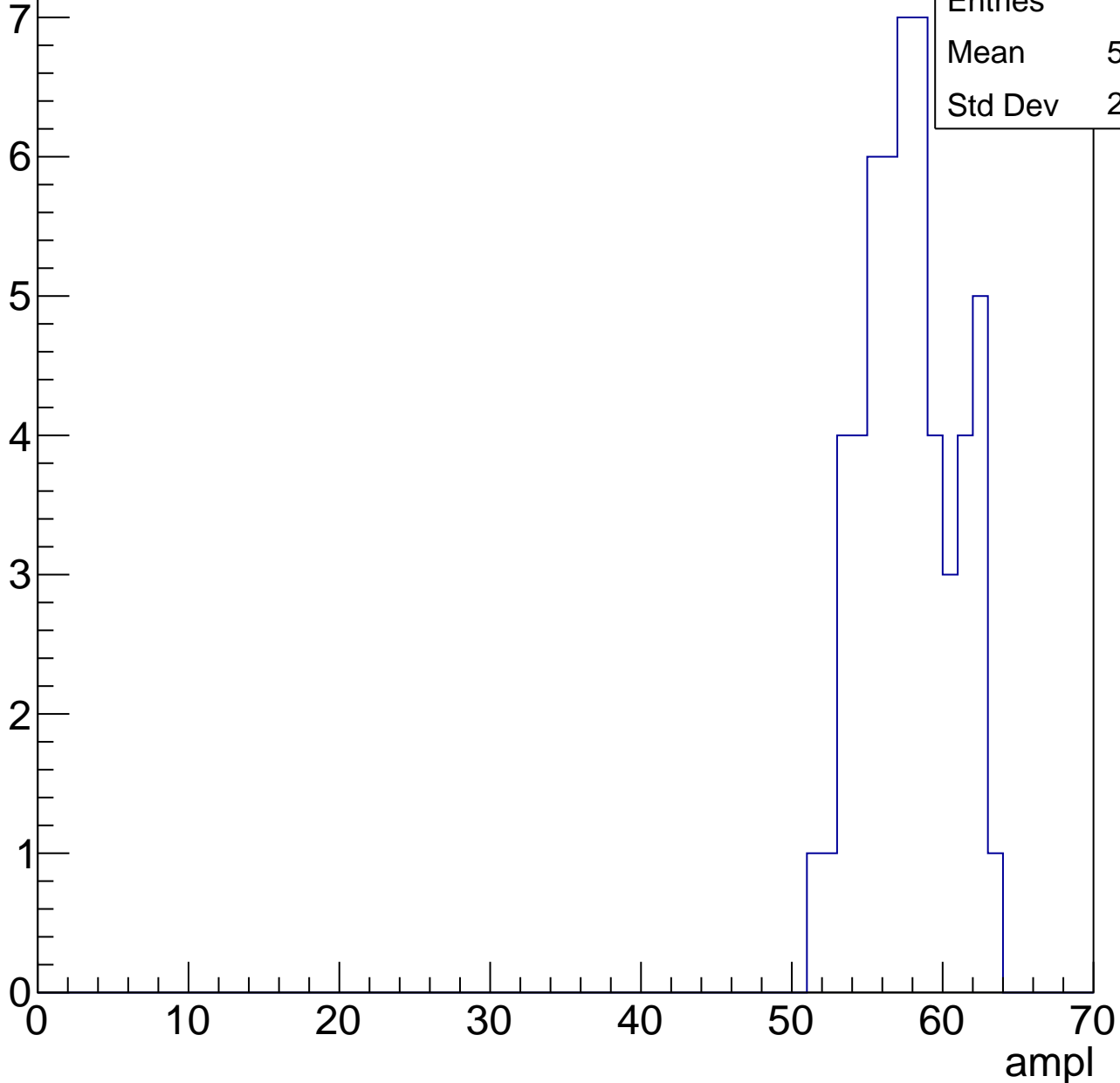


# B0L001S, U2-ch65, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 53    |
| Mean    | 57.26 |
| Std Dev | 2.953 |

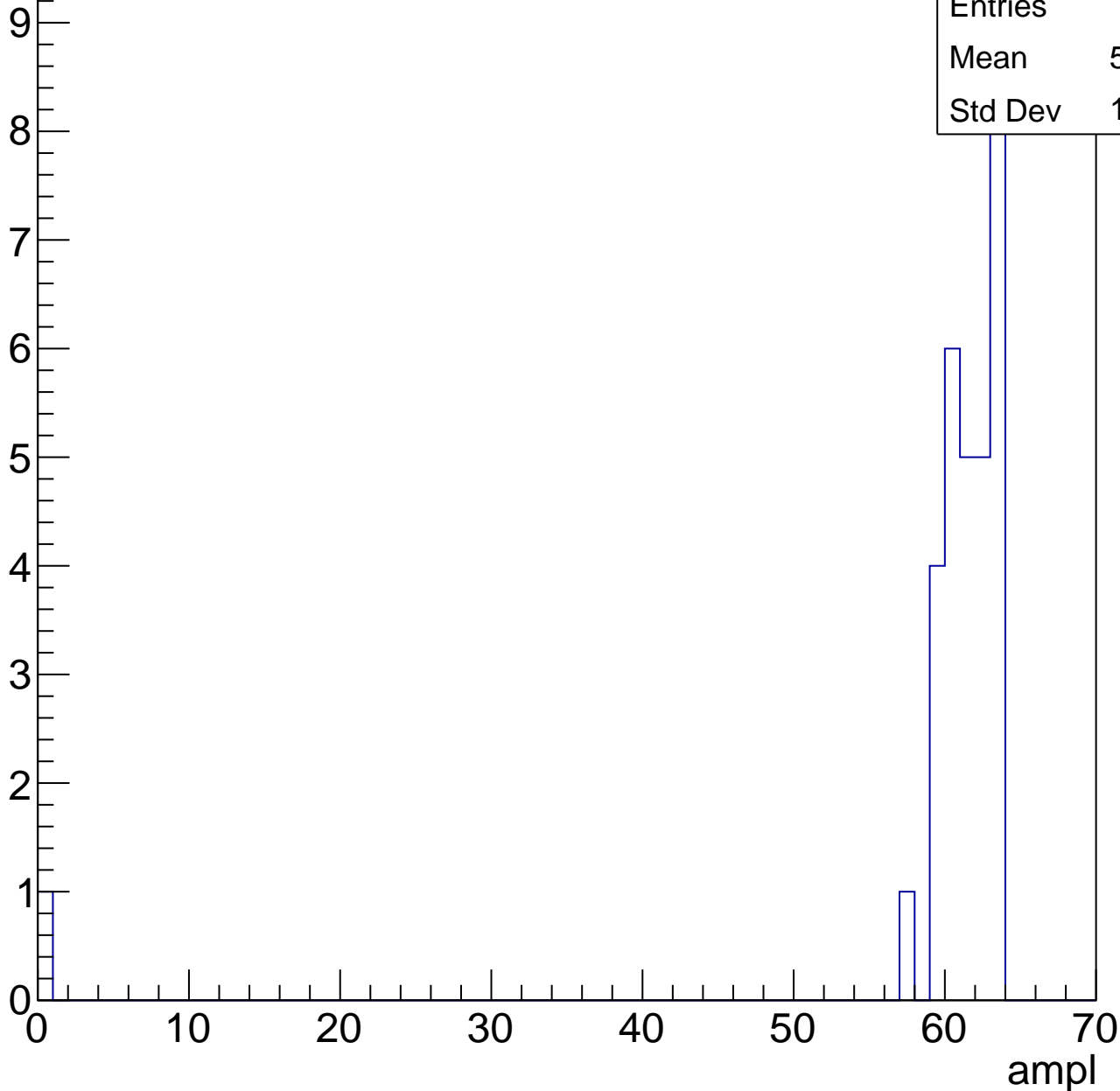


# B0L001S, U2-ch65, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 31    |
| Mean    | 59.19 |
| Std Dev | 10.92 |



# B0L001S, U2-ch65, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch65, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U2-ch66, adc0

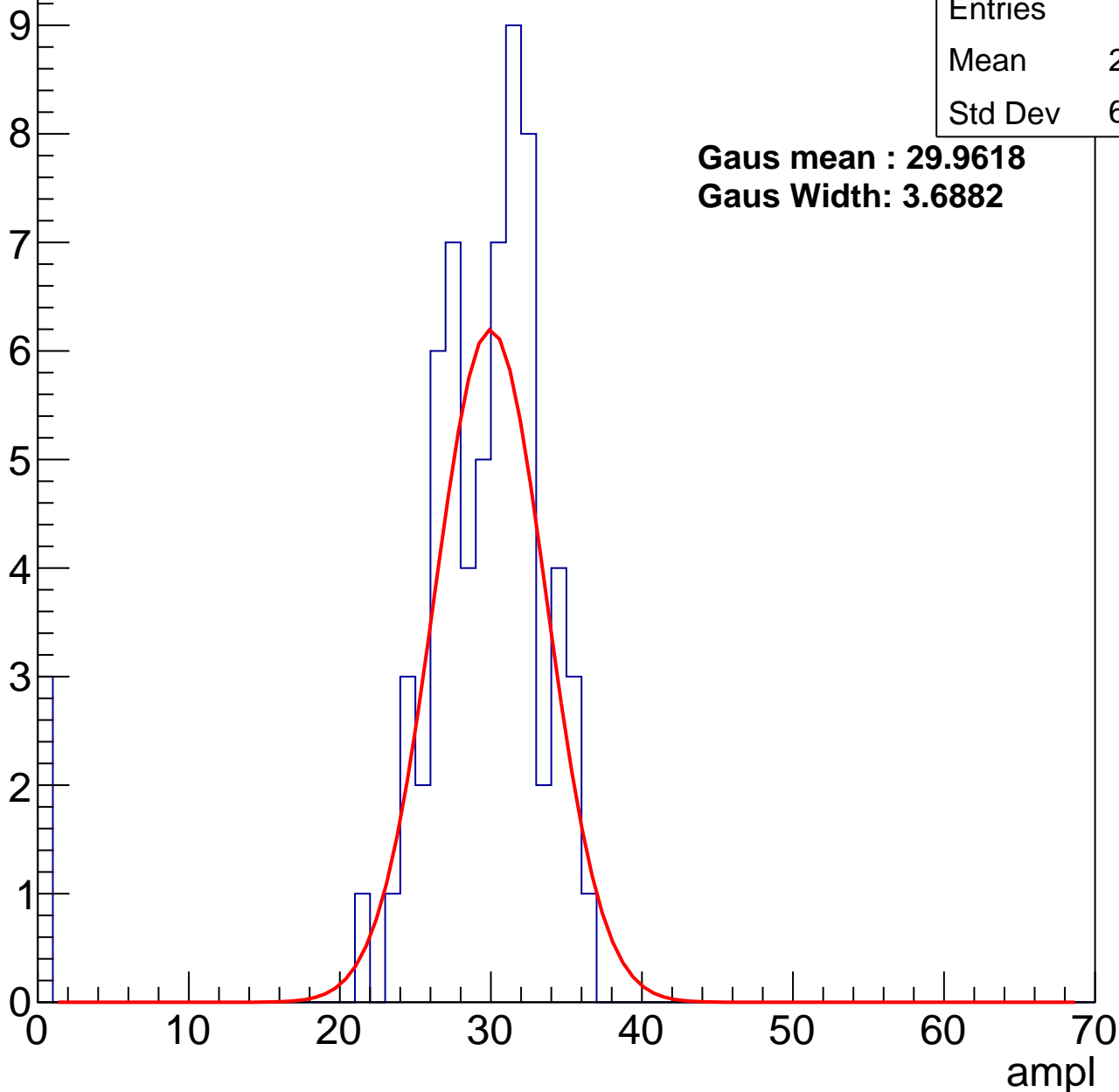
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 66    |
| Mean    | 28.12 |
| Std Dev | 6.929 |

**Gaus mean : 29.9618**

**Gaus Width: 3.6882**



# B0L001S, U2-ch66, adc1

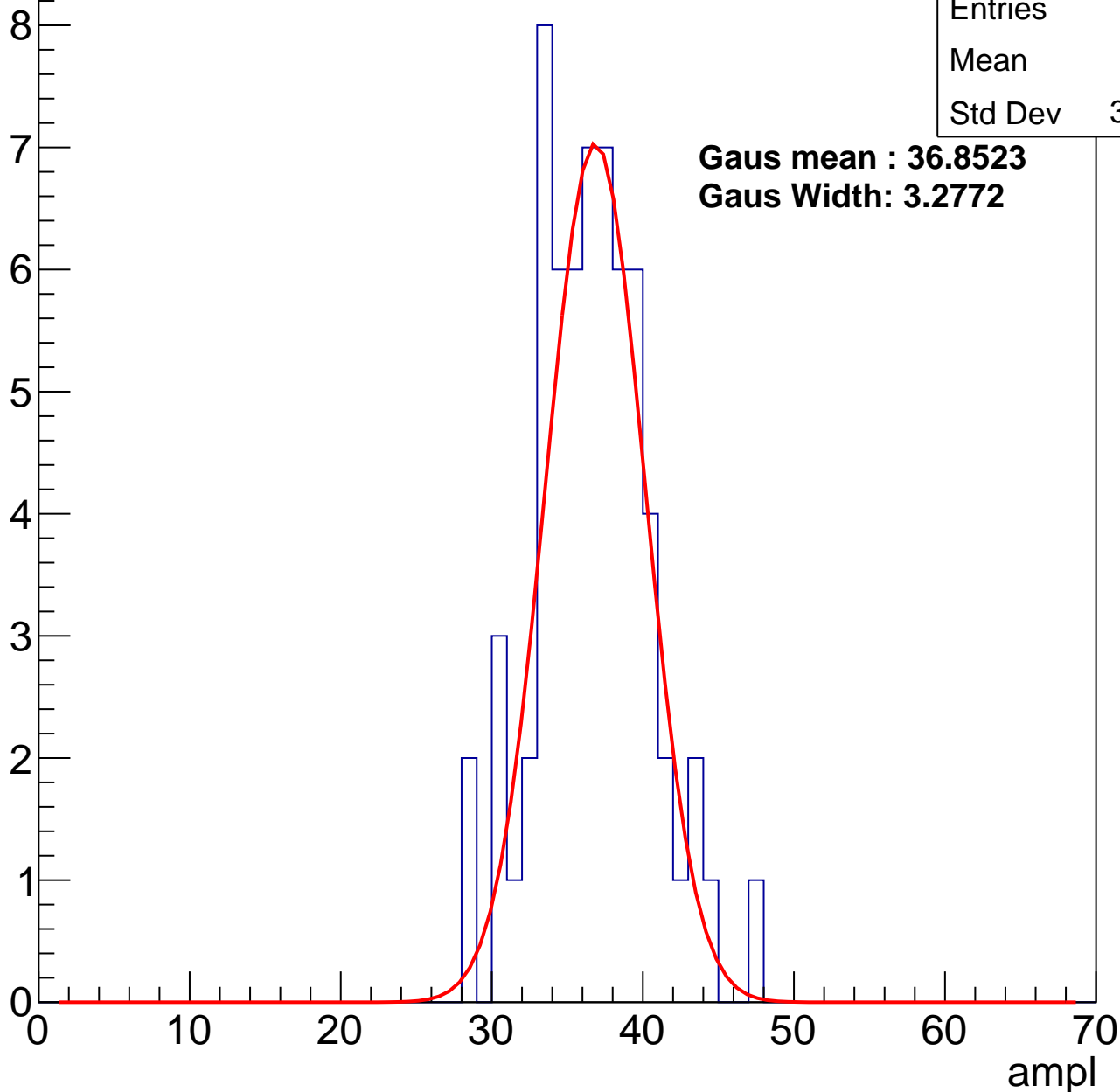
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 65    |
| Mean    | 36.2  |
| Std Dev | 3.742 |

**Gaus mean : 36.8523**

**Gaus Width: 3.2772**



# B0L001S, U2-ch66, adc2

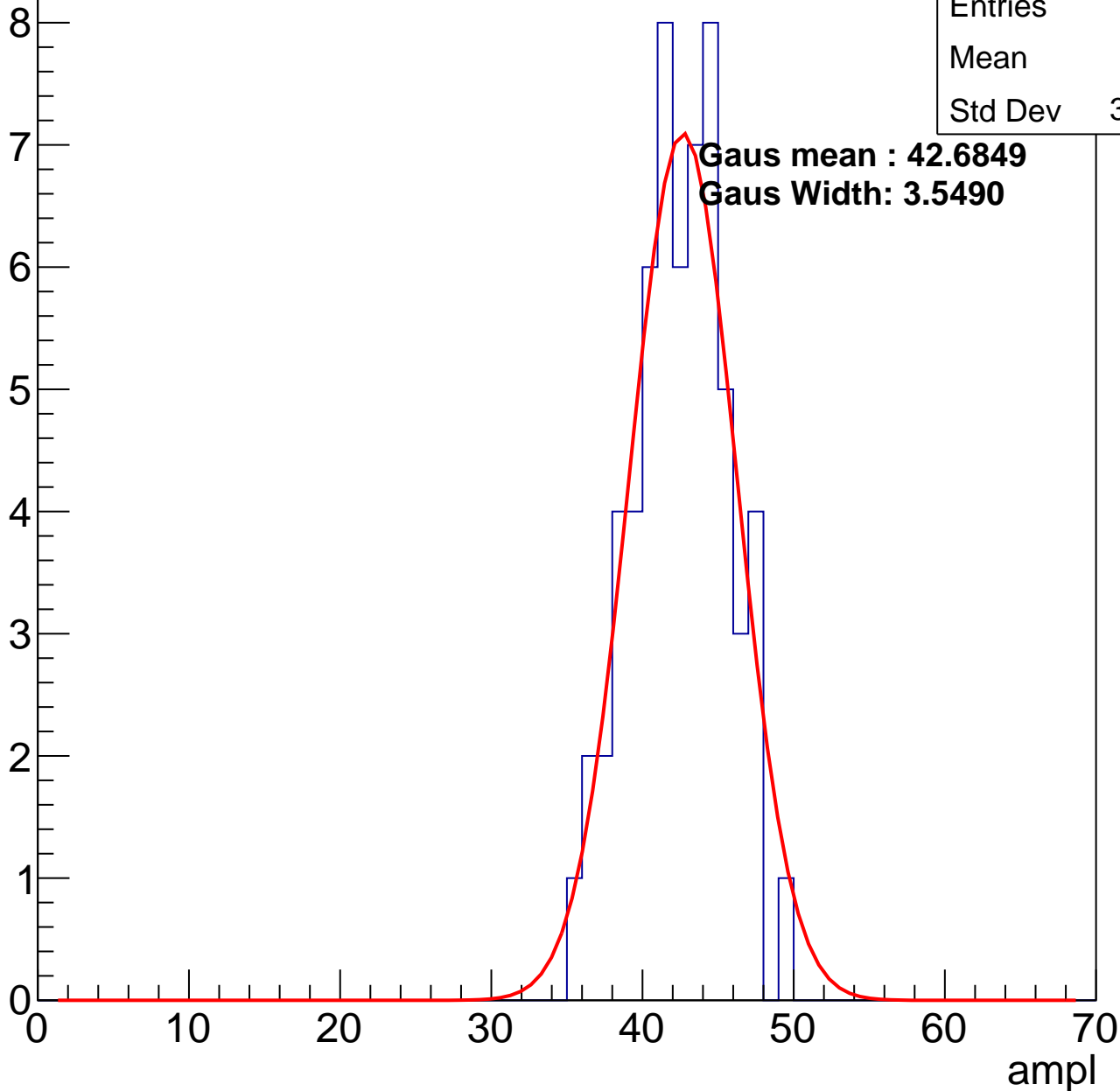
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 61    |
| Mean    | 42    |
| Std Dev | 3.094 |

**Gaus mean : 42.6849**

**Gaus Width: 3.5490**

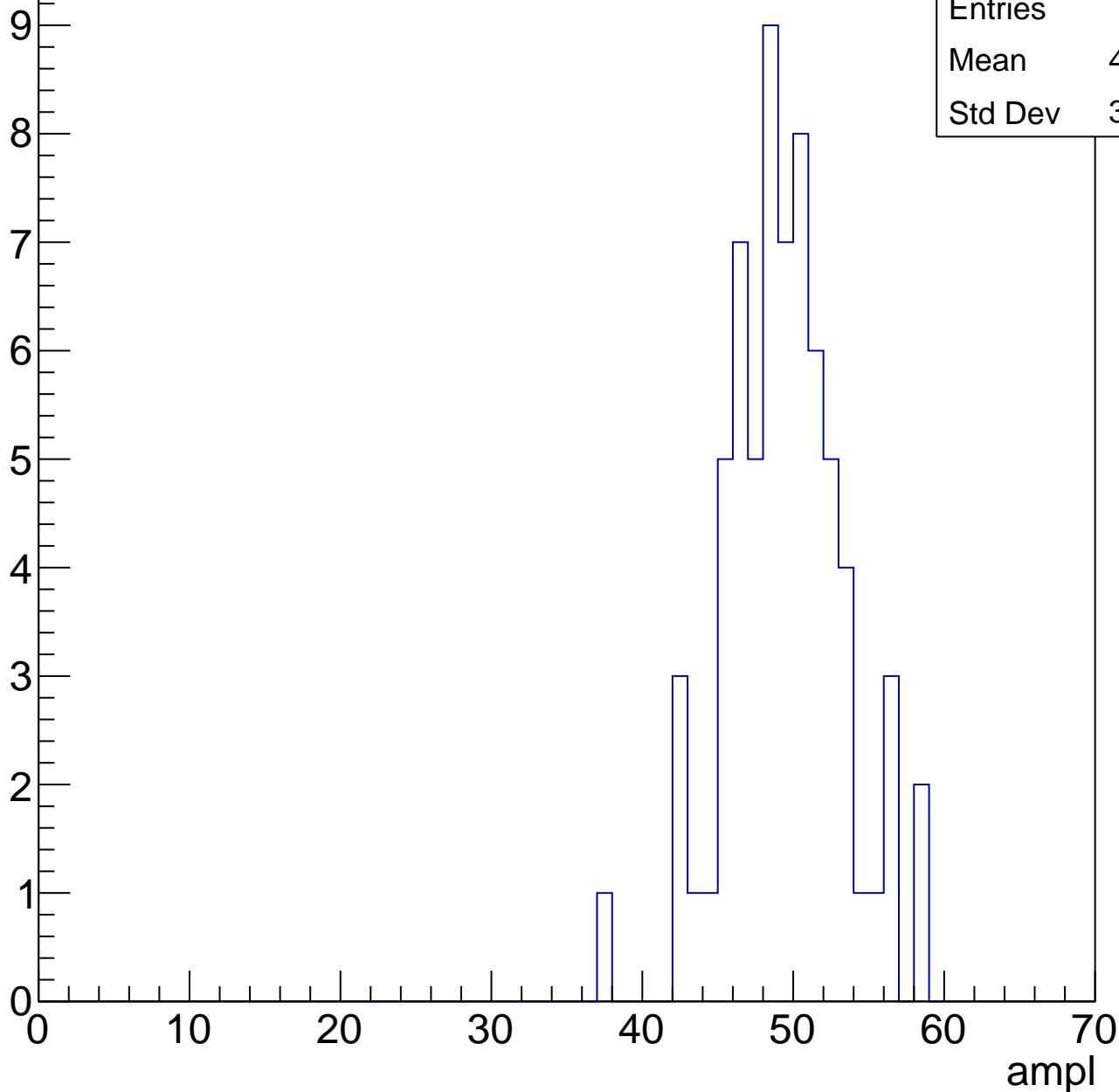


# B0L001S, U2-ch66, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

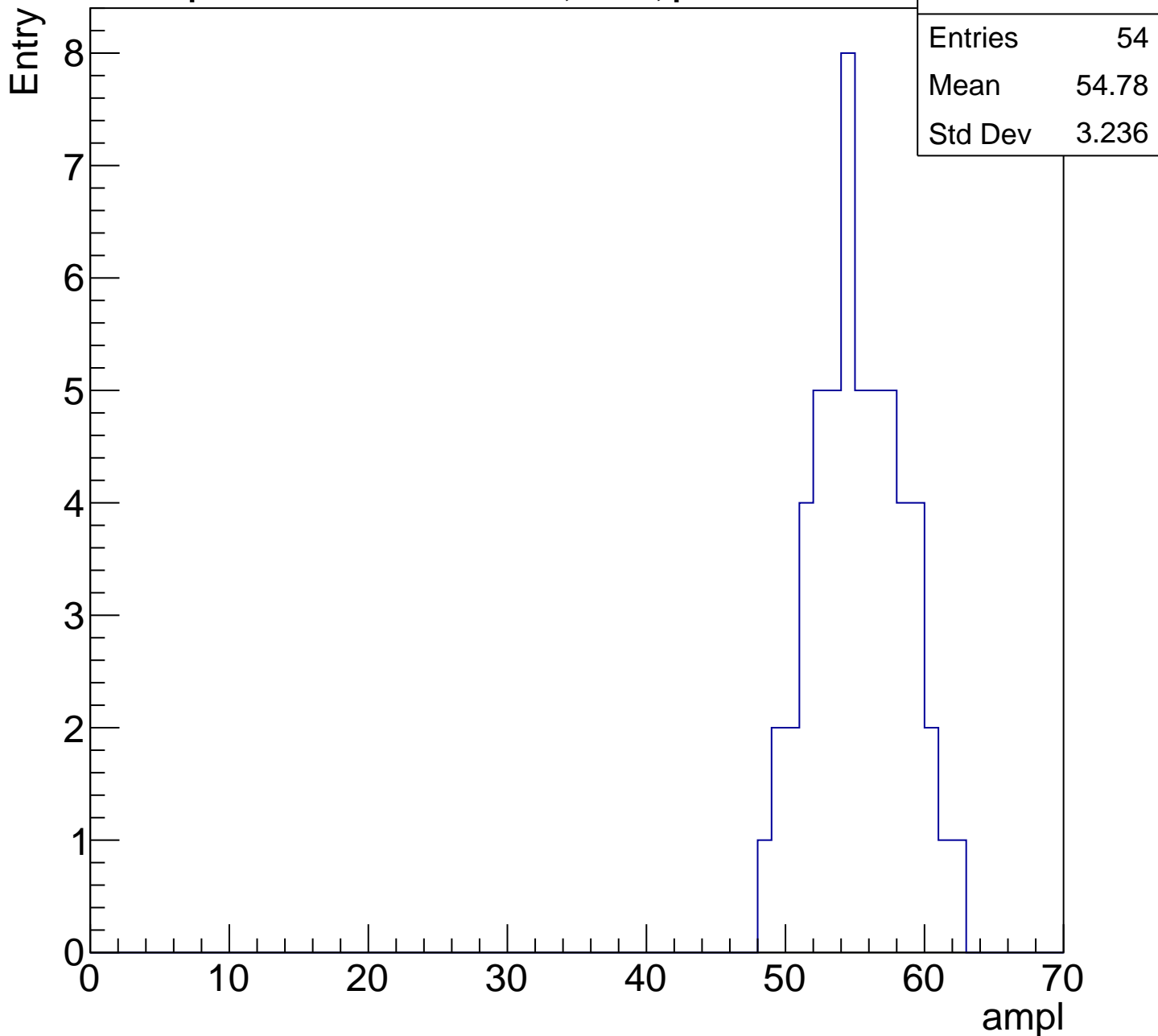
Entry

|         |       |
|---------|-------|
| Entries | 69    |
| Mean    | 48.96 |
| Std Dev | 3.873 |



# B0L001S, U2-ch66, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

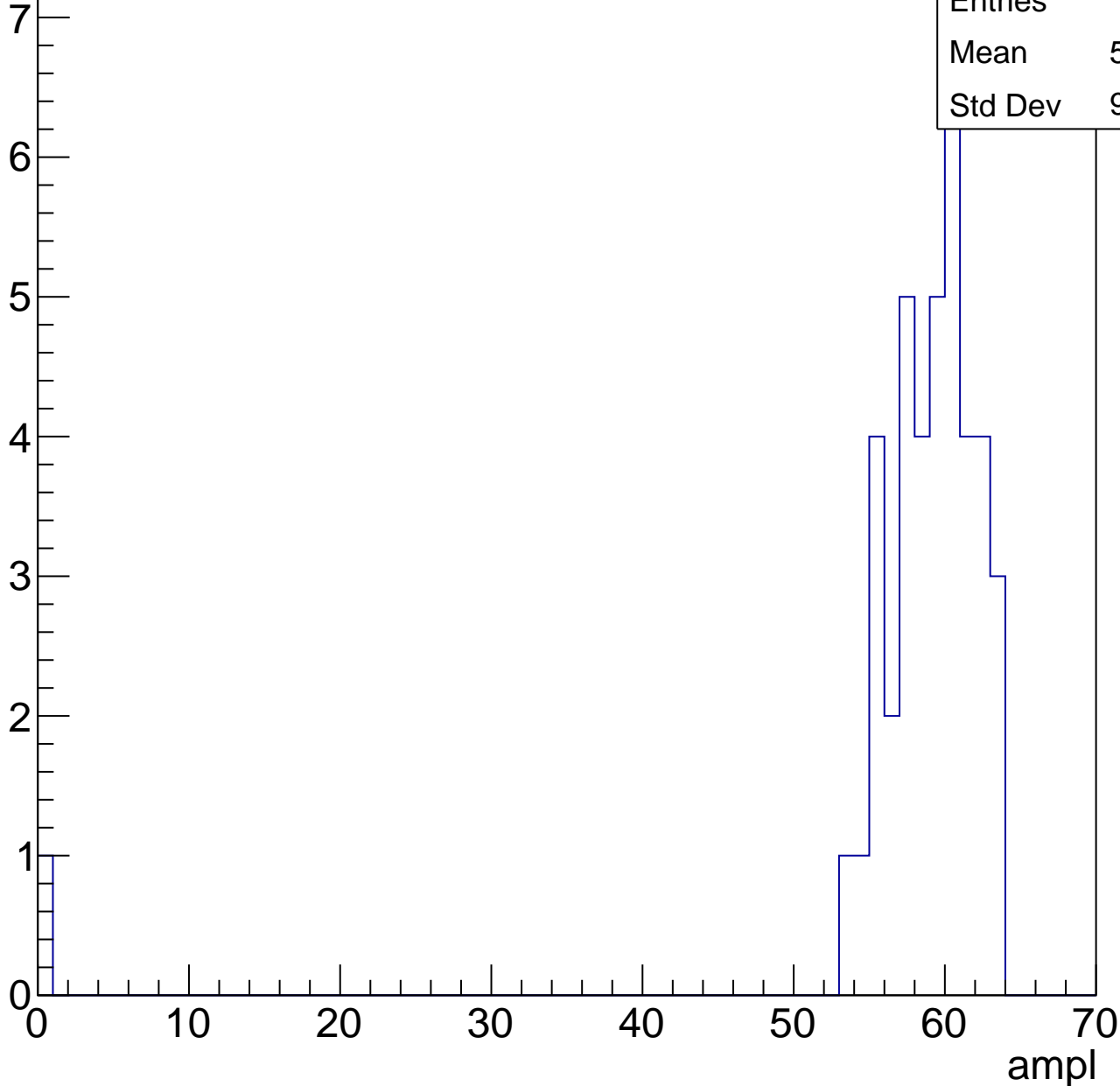


# B0L001S, U2-ch66, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

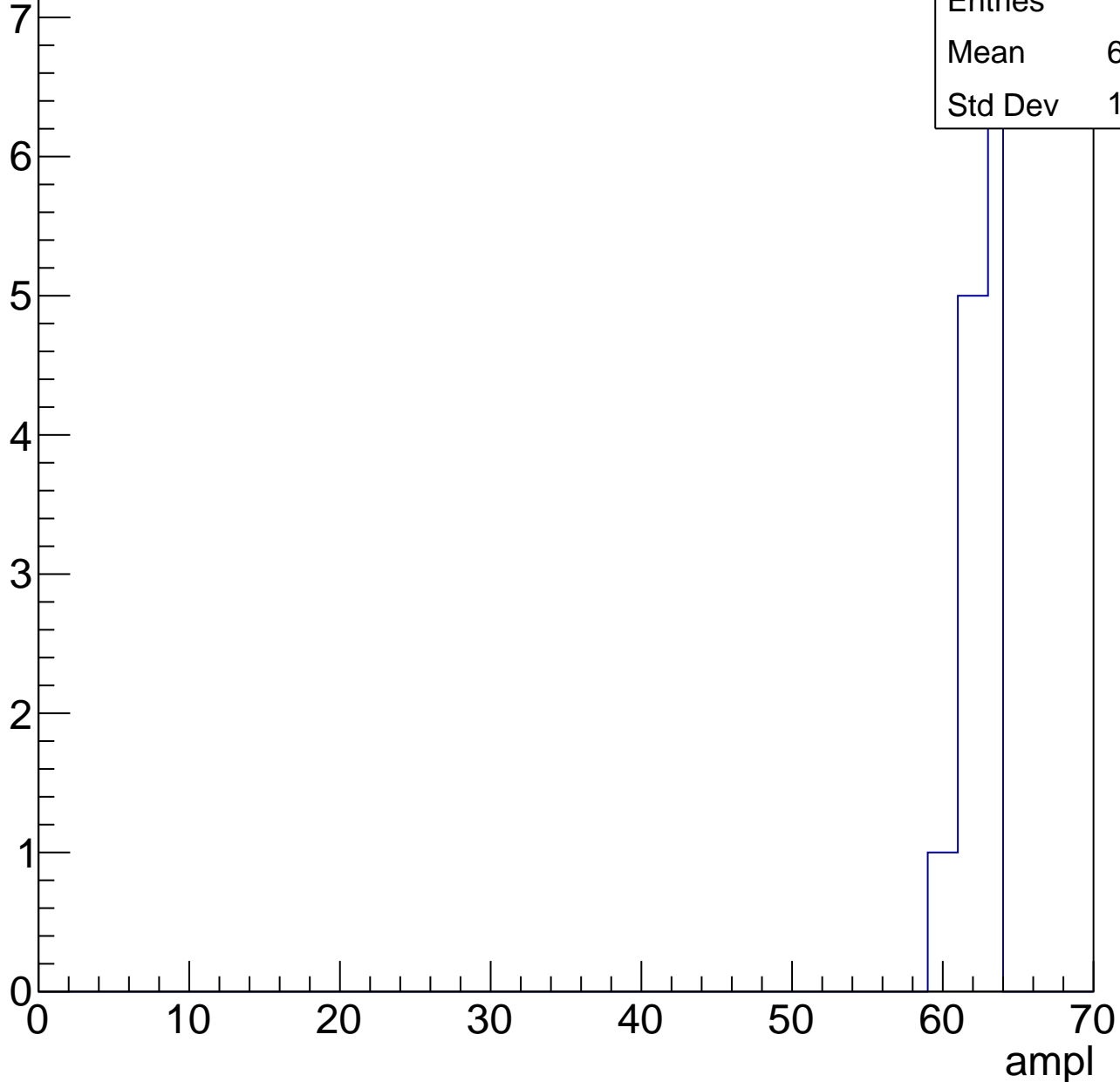
|         |       |
|---------|-------|
| Entries | 41    |
| Mean    | 57.37 |
| Std Dev | 9.429 |



# B0L001S, U2-ch66, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch66, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 1 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch67, adc0

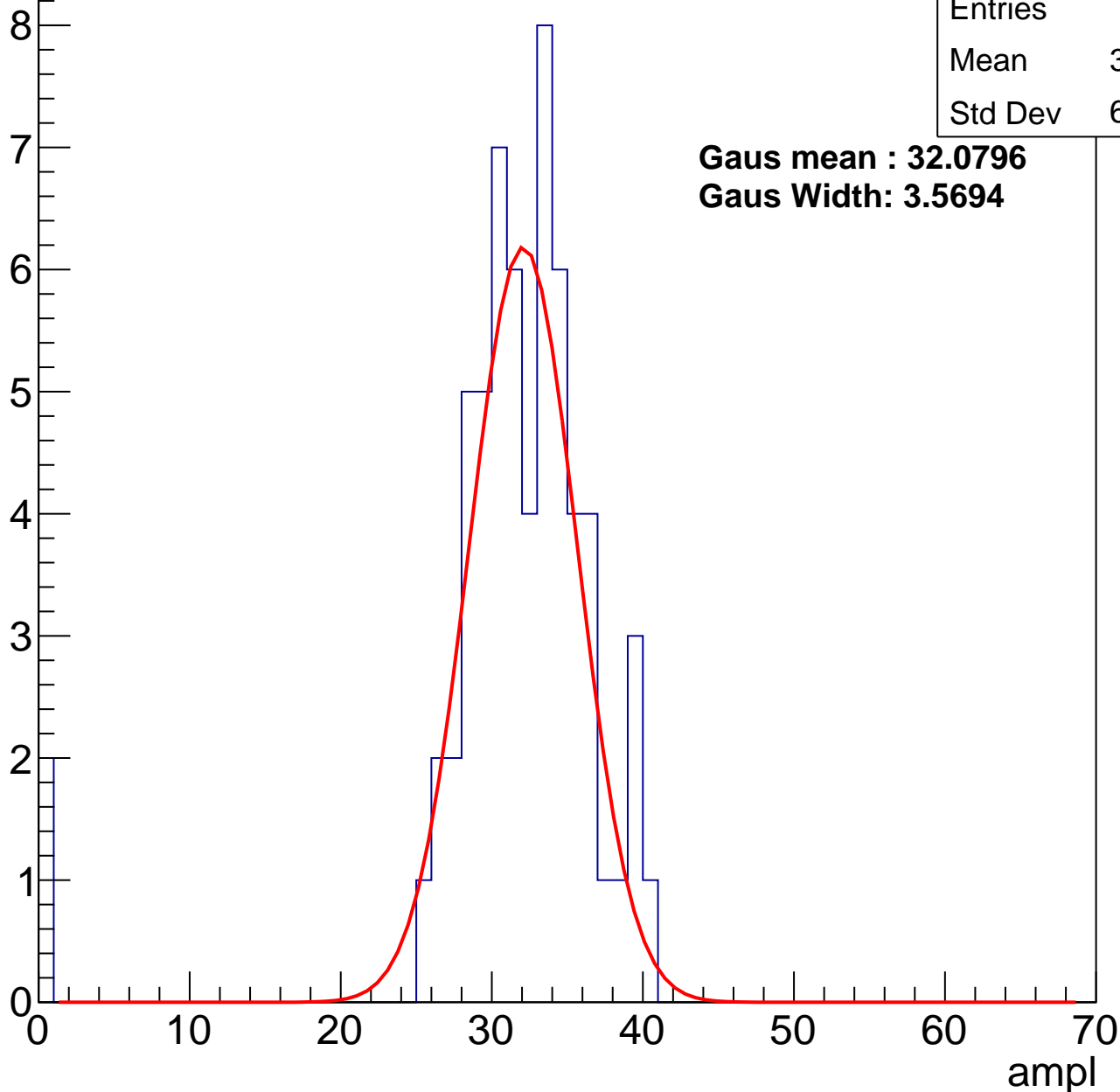
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 62    |
| Mean    | 31.03 |
| Std Dev | 6.628 |

**Gaus mean : 32.0796**

**Gaus Width: 3.5694**



# B0L001S, U2-ch67, adc1

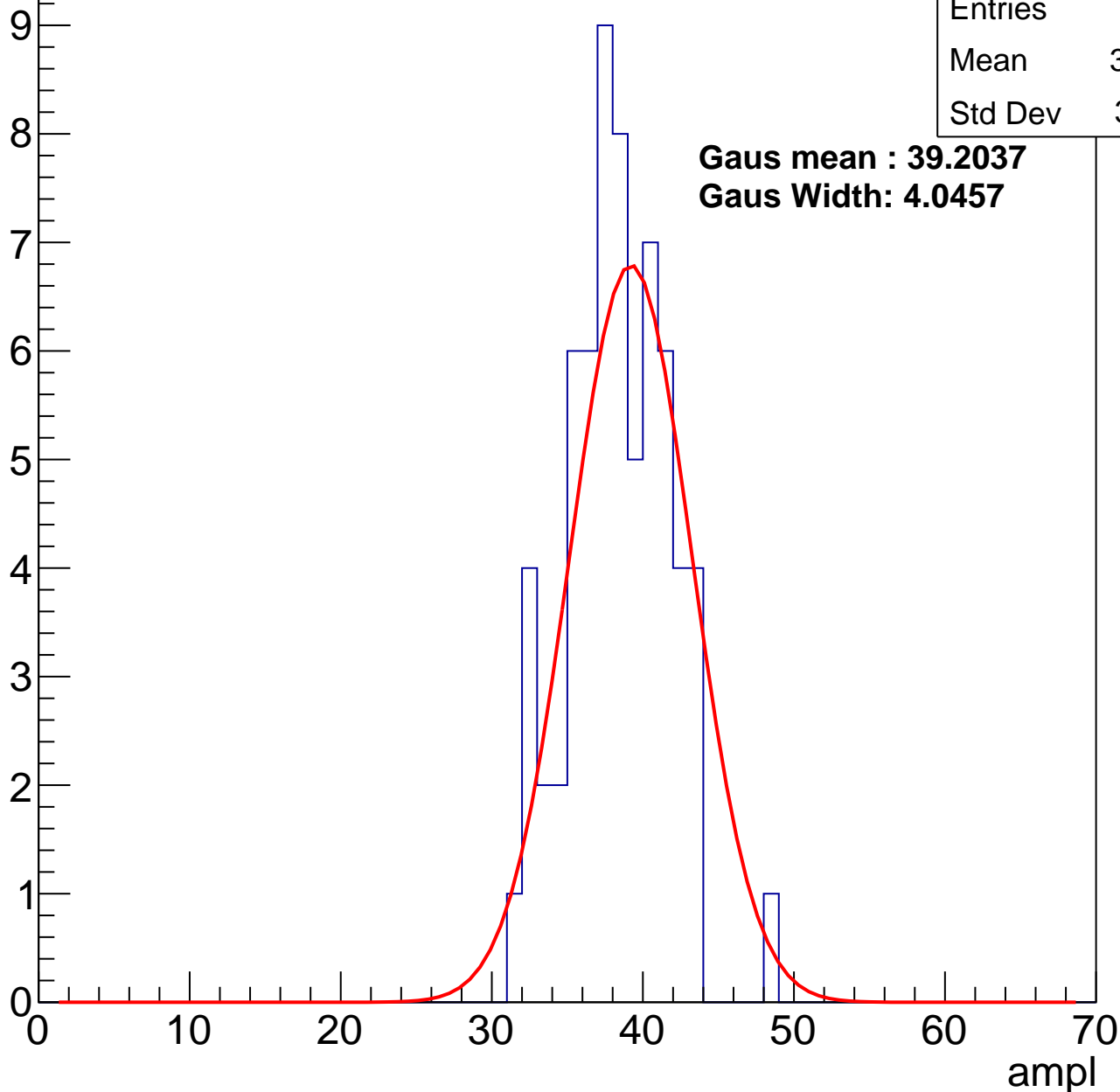
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 65    |
| Mean    | 37.92 |
| Std Dev | 3.311 |

**Gaus mean : 39.2037**

**Gaus Width: 4.0457**



# B0L001S, U2-ch67, adc2

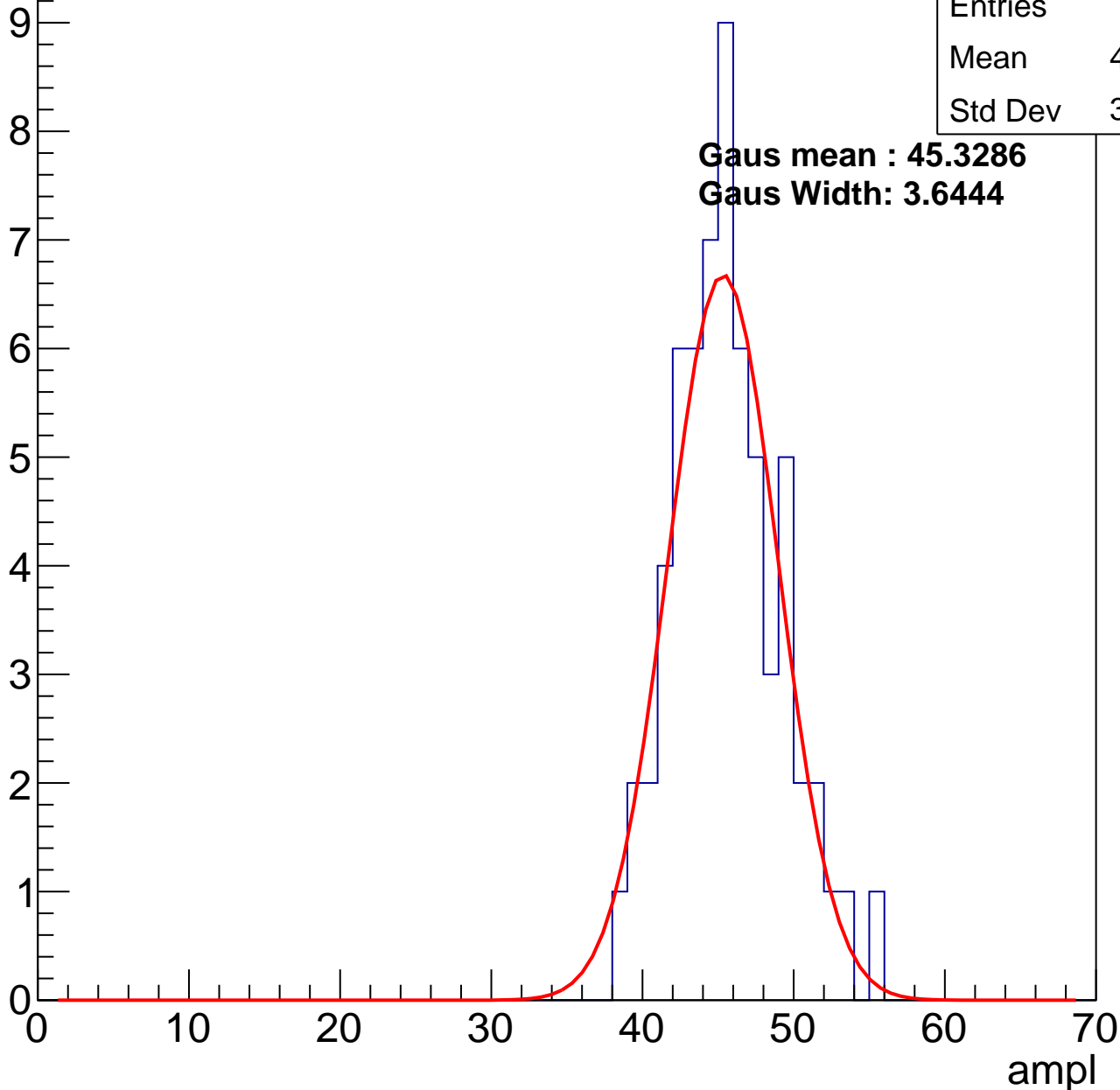
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 63    |
| Mean    | 45.16 |
| Std Dev | 3.533 |

**Gaus mean : 45.3286**

**Gaus Width: 3.6444**

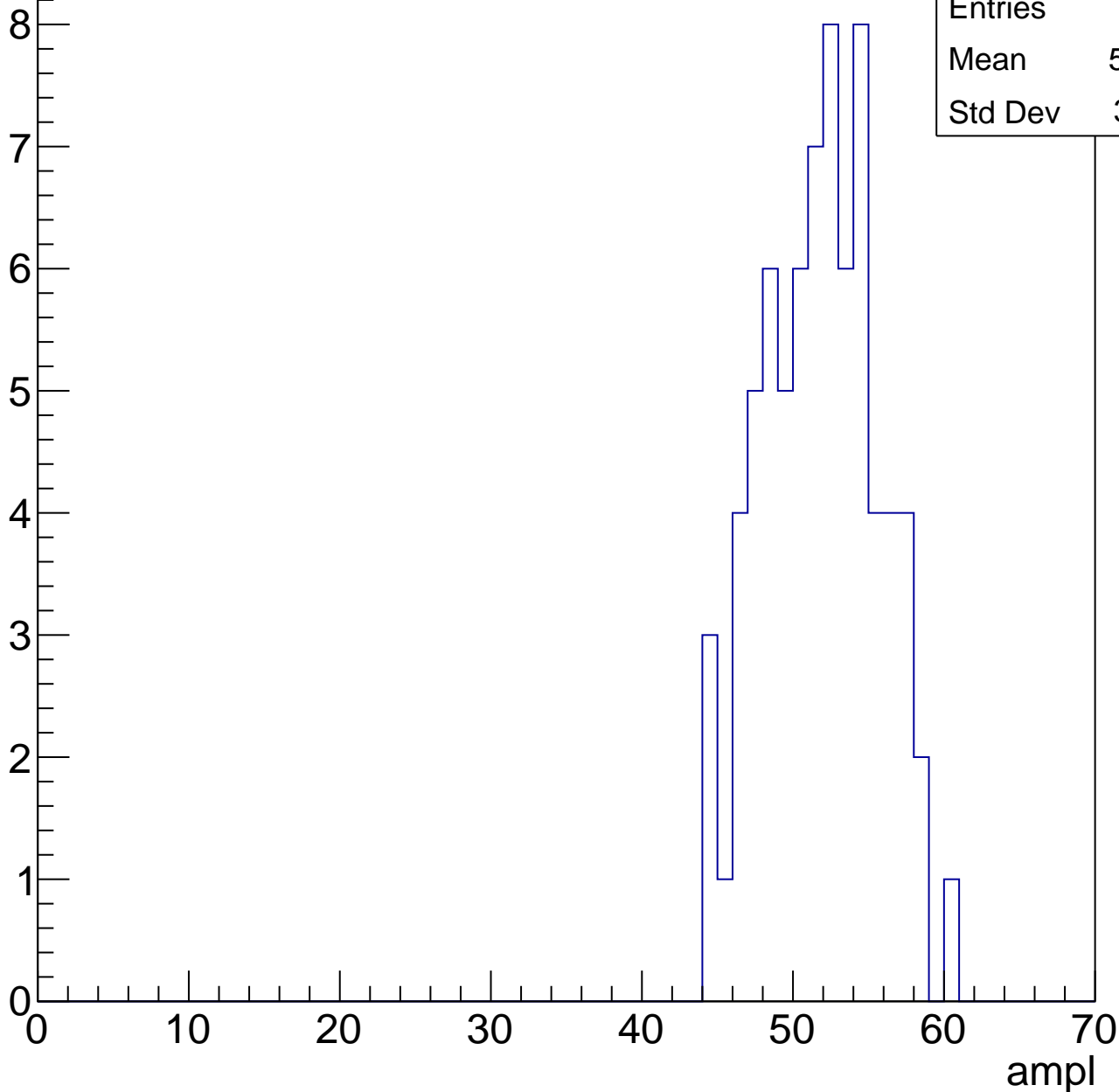


# B0L001S, U2-ch67, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 74    |
| Mean    | 51.35 |
| Std Dev | 3.721 |

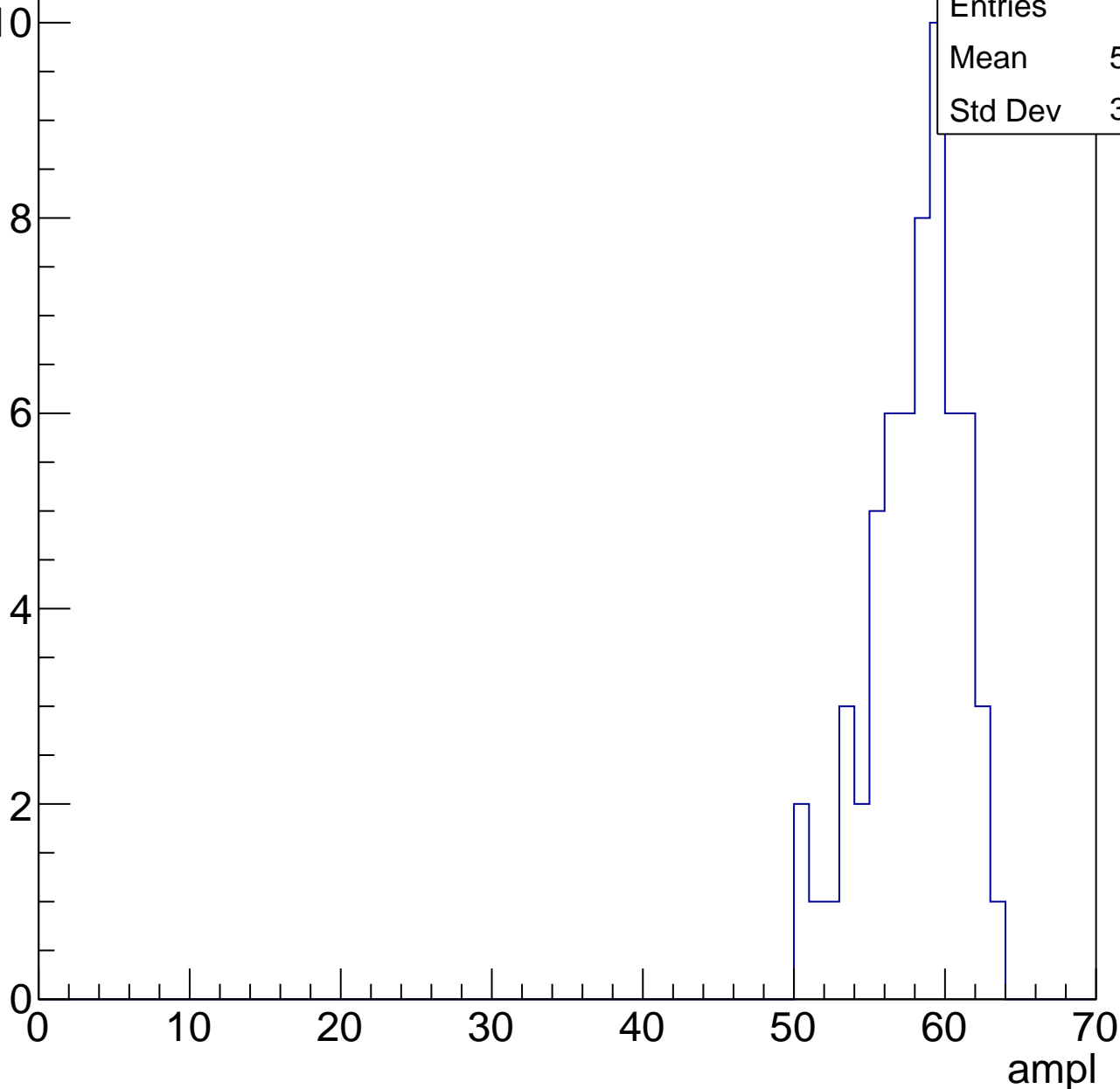


# B0L001S, U2-ch67, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 60    |
| Mean    | 57.53 |
| Std Dev | 3.008 |

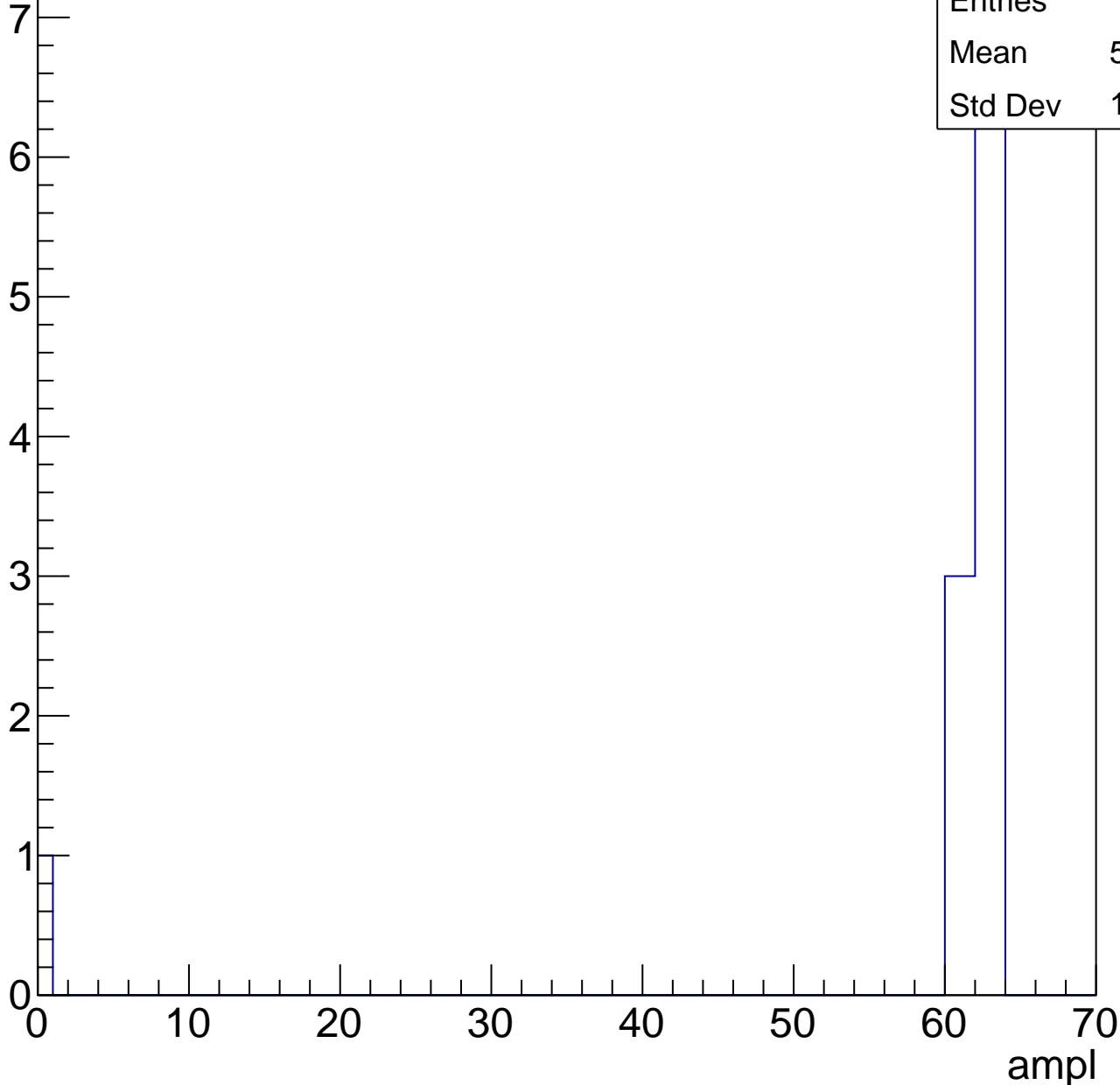


# B0L001S, U2-ch67, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 21    |
| Mean    | 58.95 |
| Std Dev | 13.22 |



# B0L001S, U2-ch67, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch67, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 1 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch68, adc0

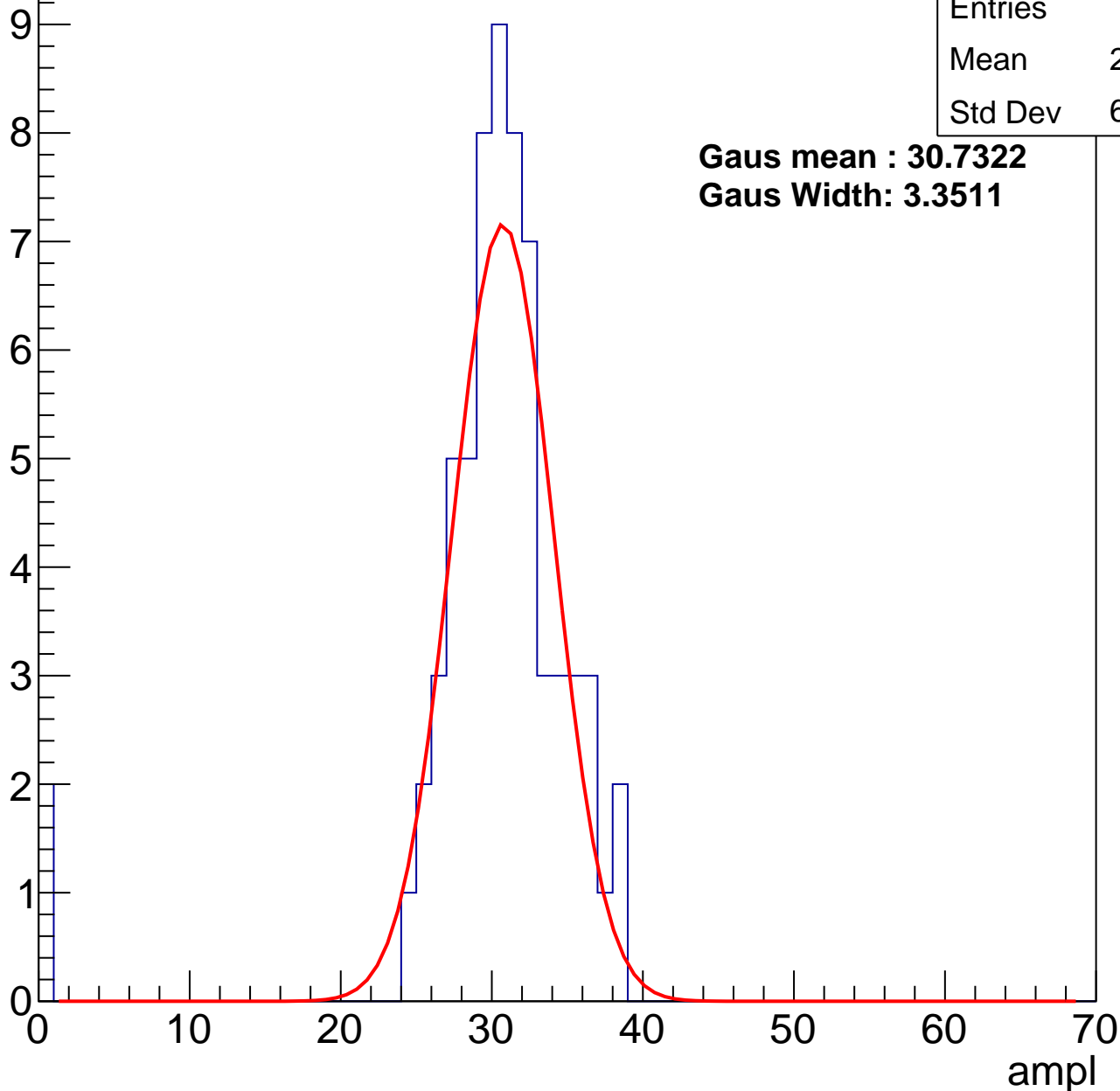
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 65    |
| Mean    | 29.66 |
| Std Dev | 6.165 |

**Gaus mean : 30.7322**

**Gaus Width: 3.3511**



# B0L001S, U2-ch68, adc1

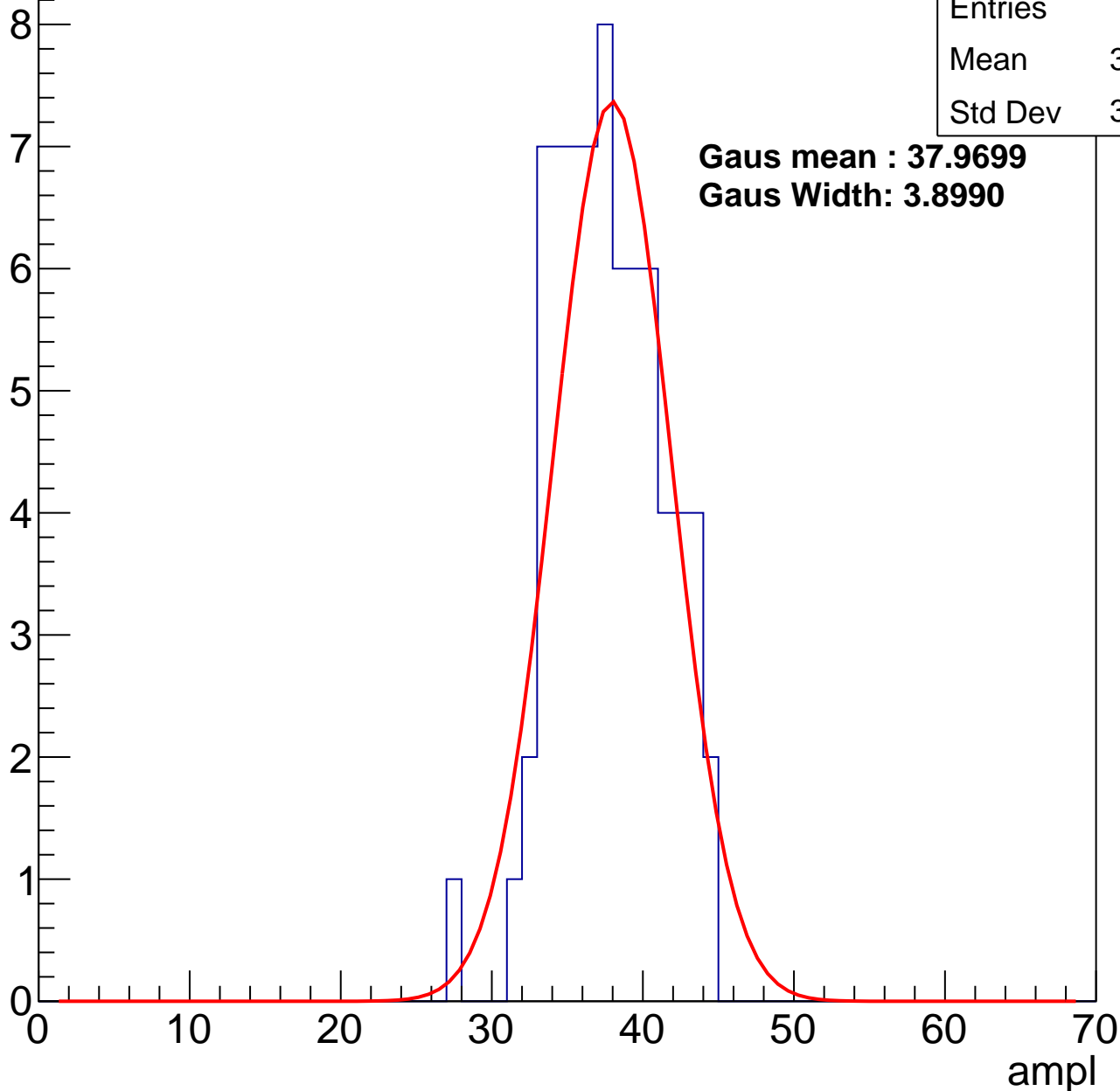
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 72    |
| Mean    | 37.19 |
| Std Dev | 3.503 |

**Gaus mean : 37.9699**

**Gaus Width: 3.8990**



# B0L001S, U2-ch68, adc2

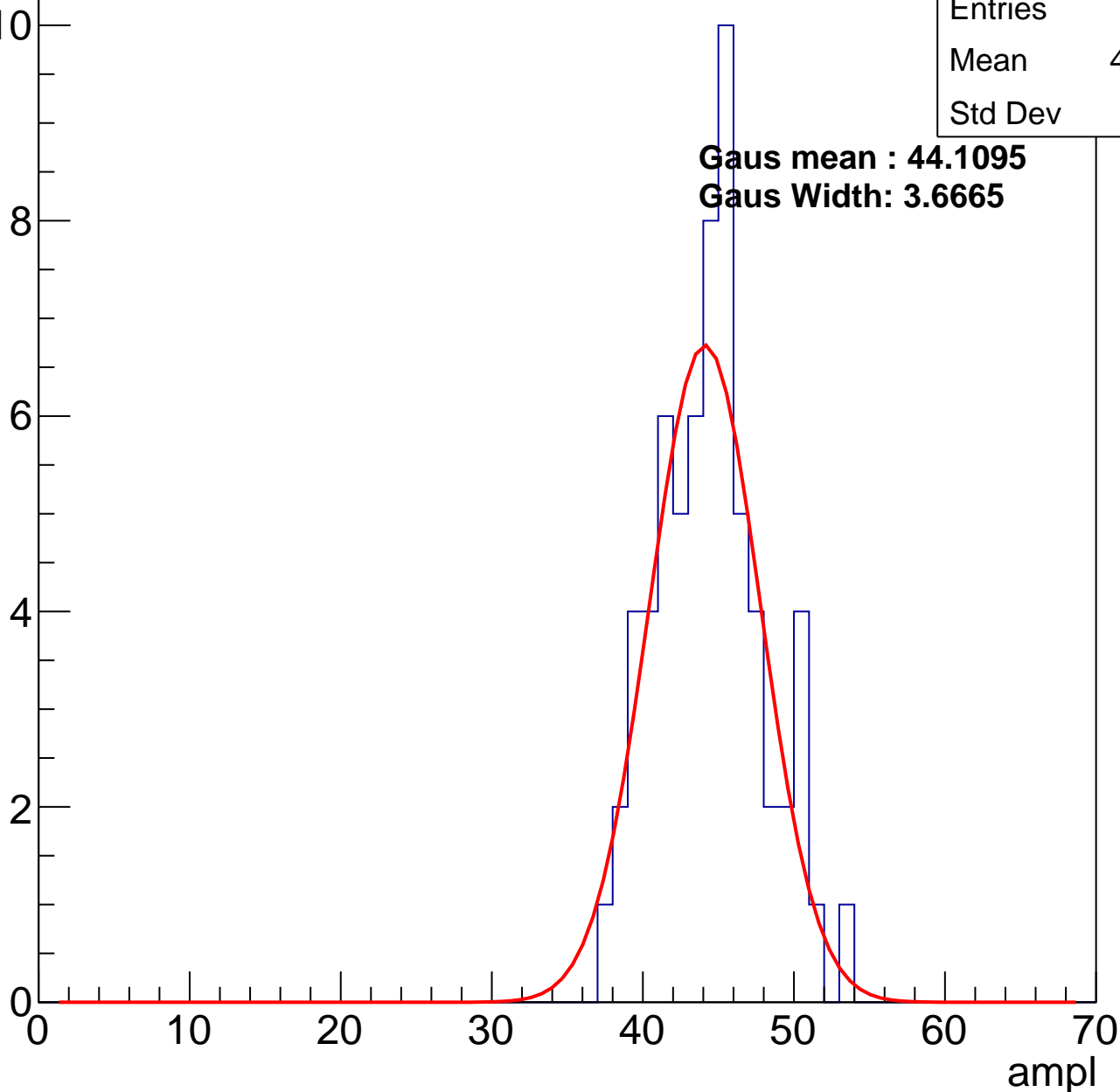
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 65    |
| Mean    | 44.02 |
| Std Dev | 3.48  |

**Gaus mean : 44.1095**

**Gaus Width: 3.6665**

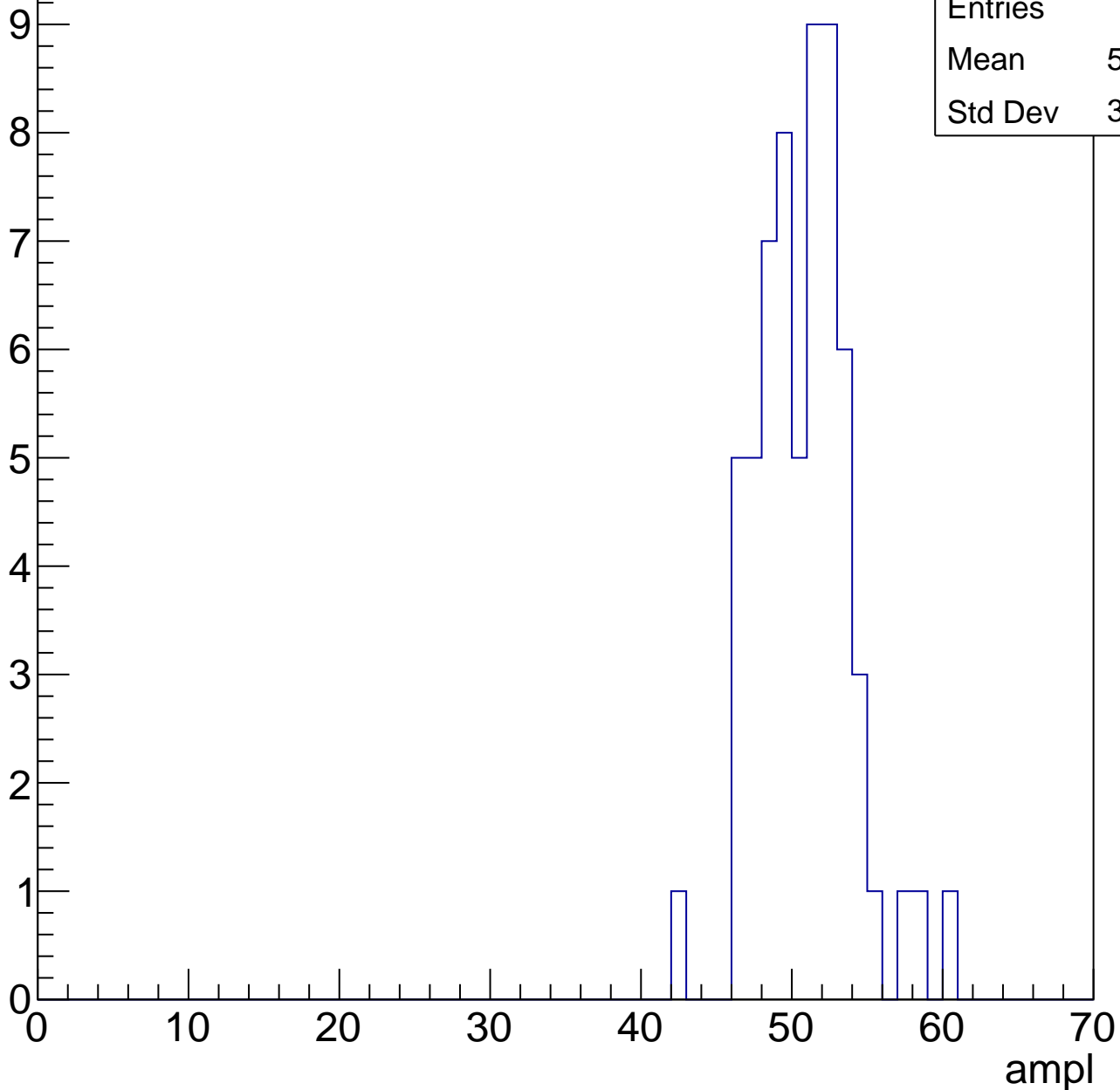


# B0L001S, U2-ch68, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

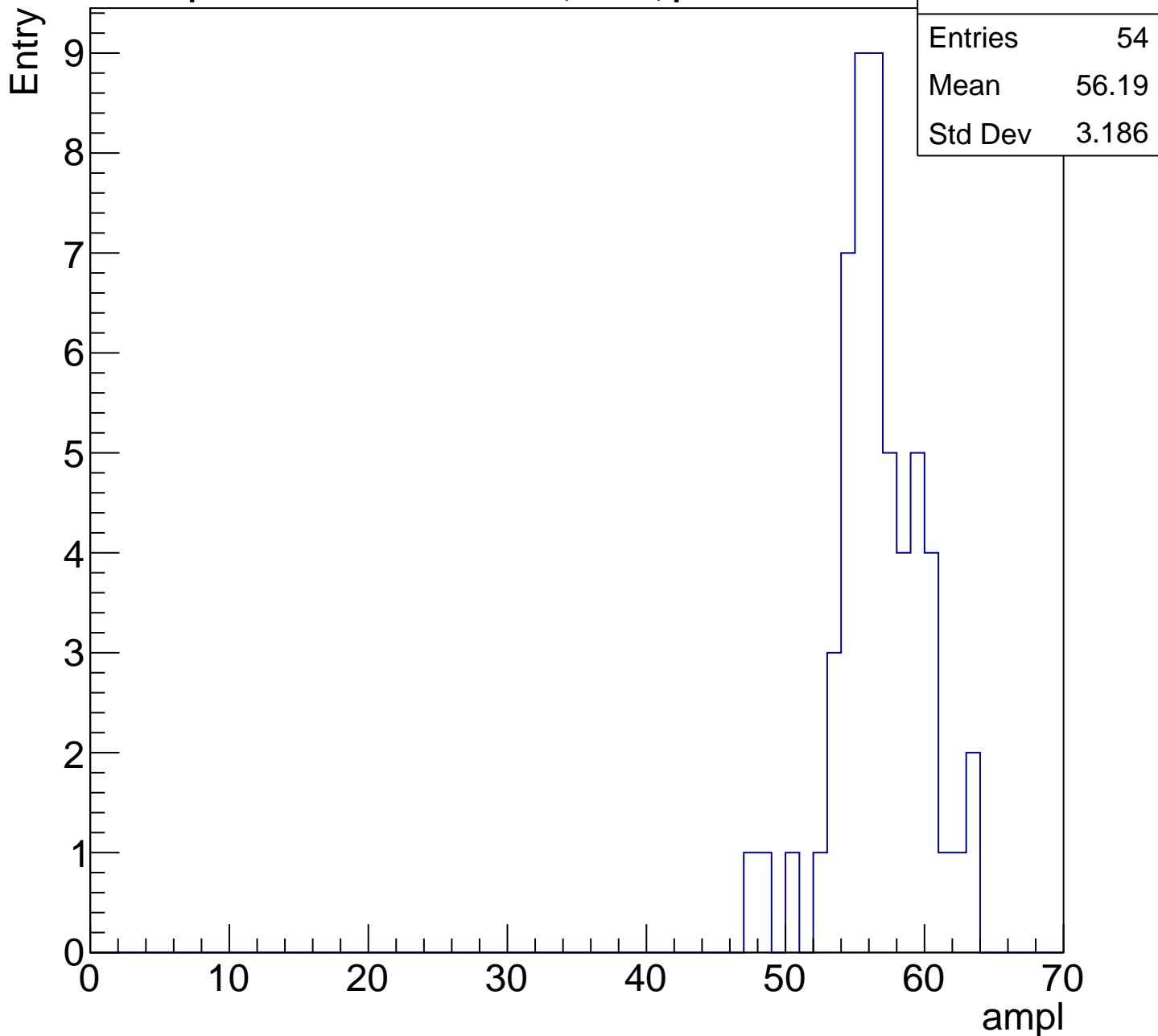
Entry

|         |       |
|---------|-------|
| Entries | 62    |
| Mean    | 50.35 |
| Std Dev | 3.117 |



# B0L001S, U2-ch68, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

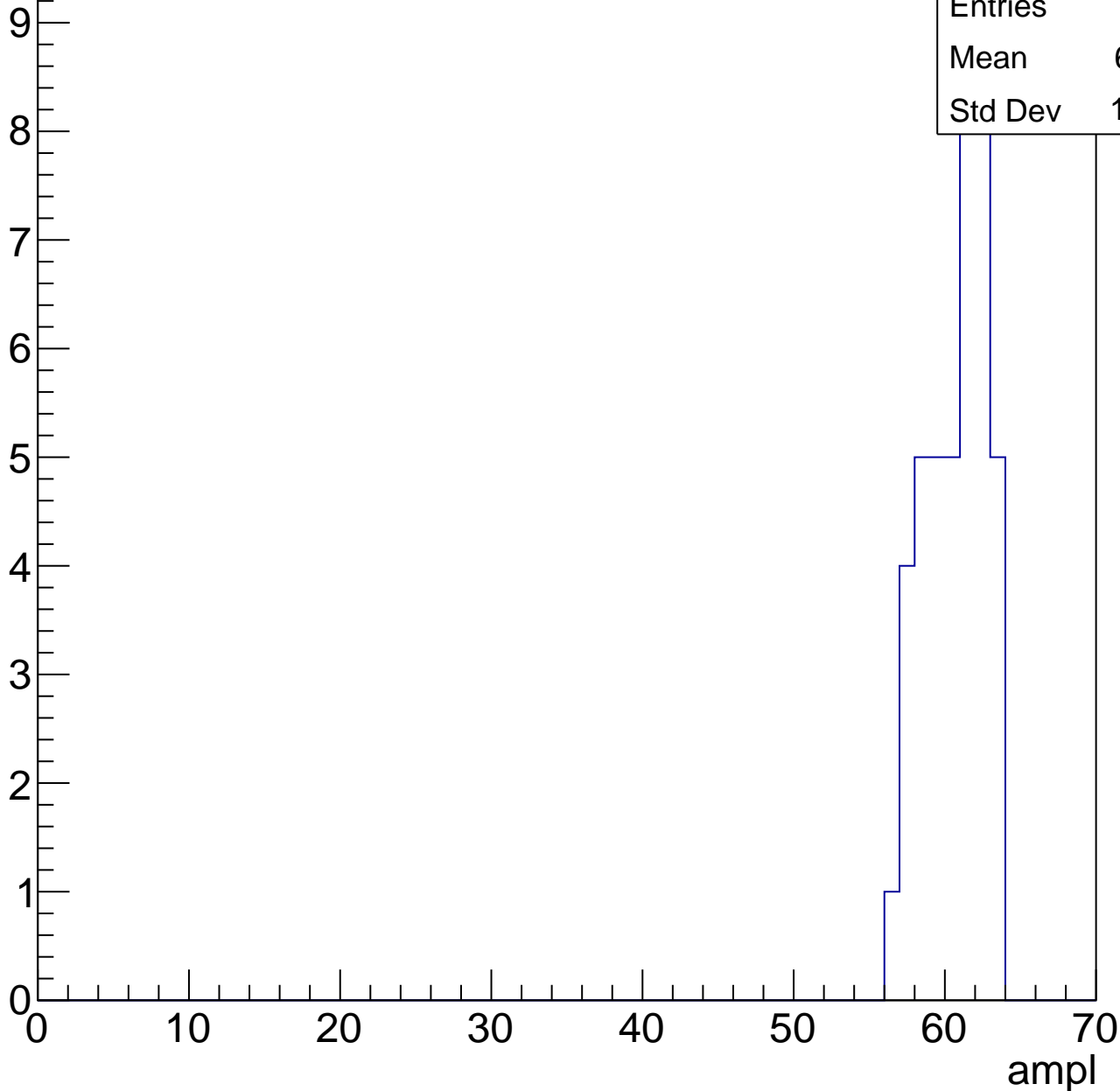


# B0L001S, U2-ch68, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

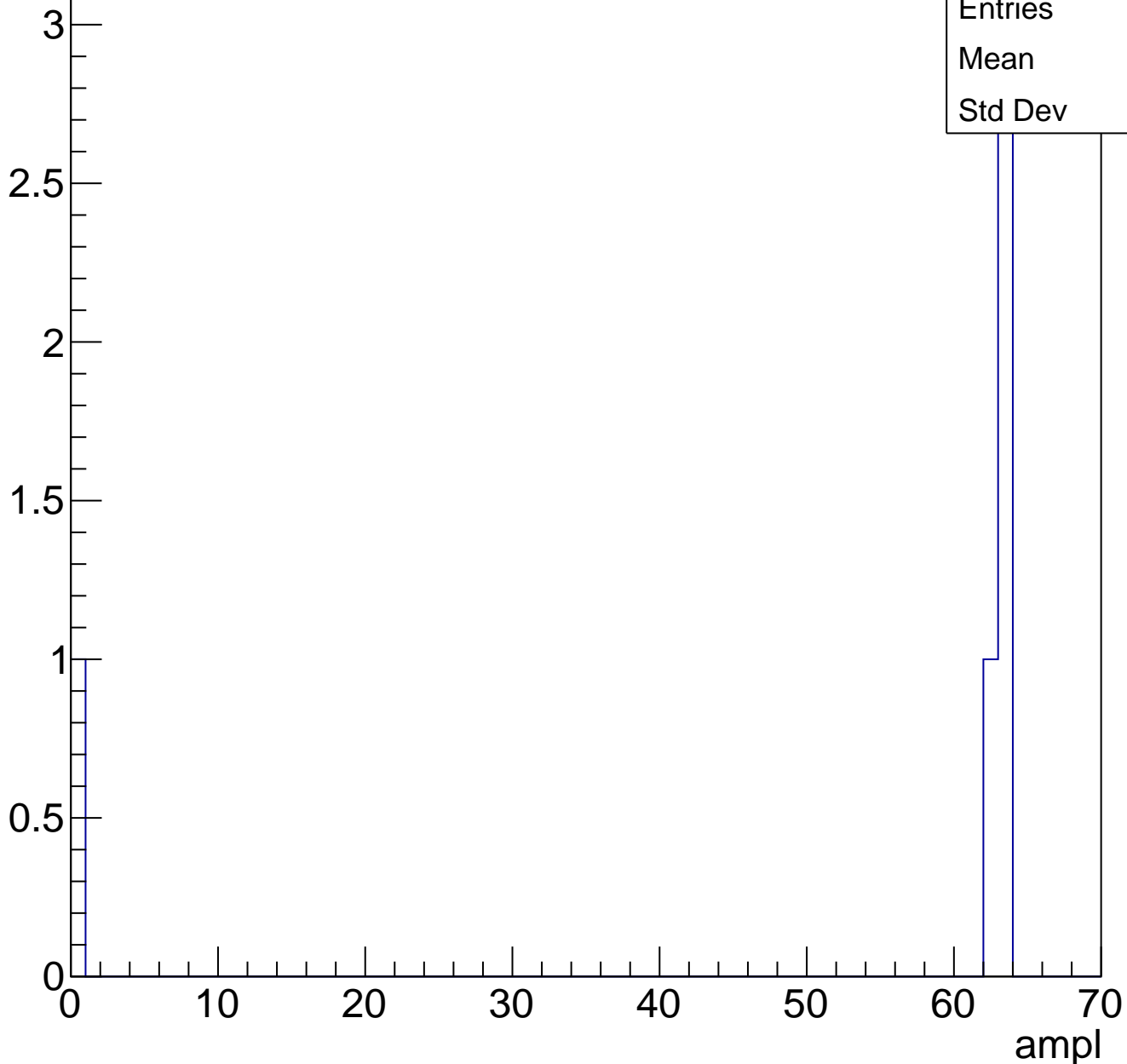
|         |       |
|---------|-------|
| Entries | 42    |
| Mean    | 60.21 |
| Std Dev | 1.958 |



# B0L001S, U2-ch68, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch68, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 1 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch69, adc0

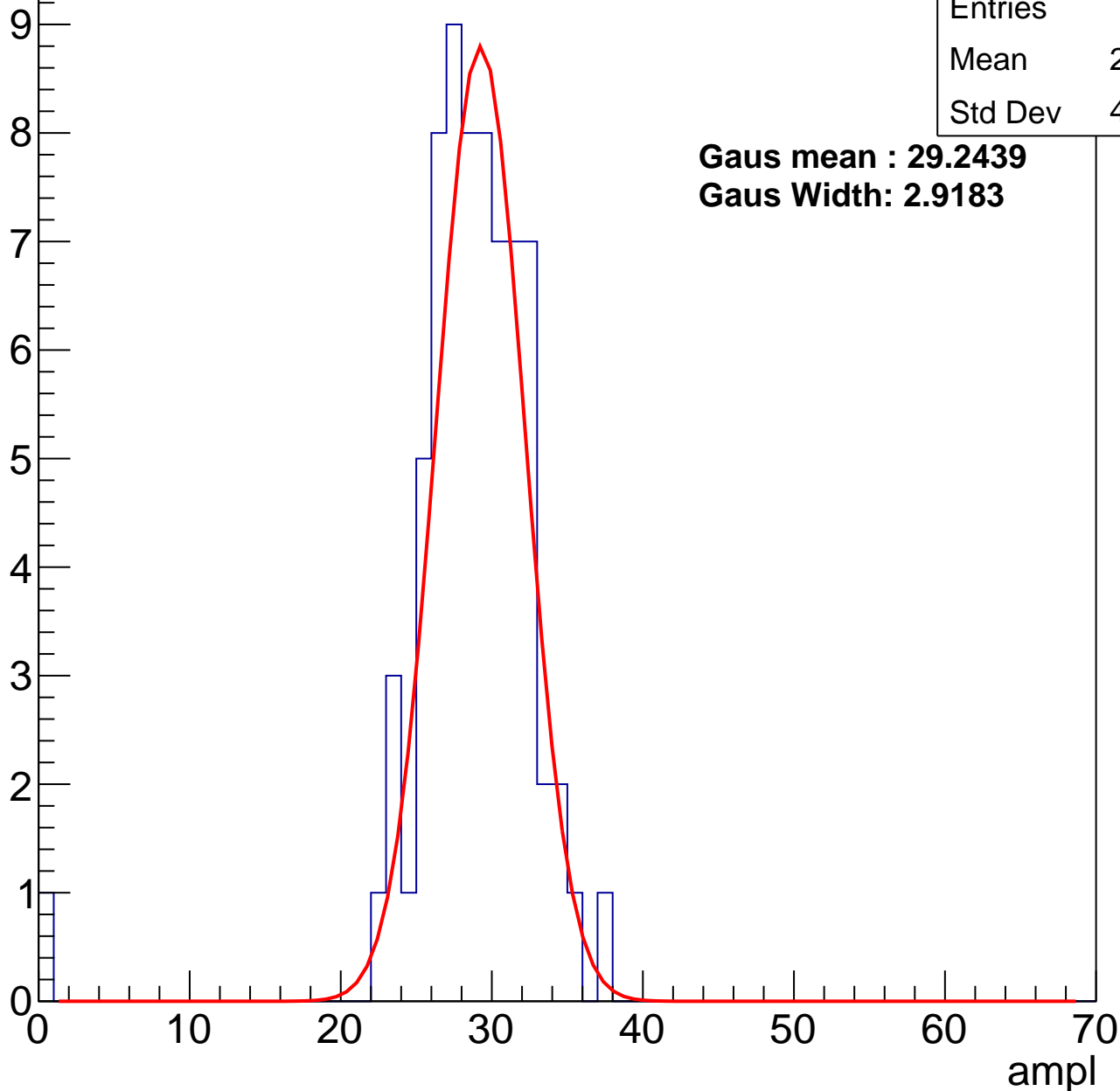
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 71    |
| Mean    | 28.23 |
| Std Dev | 4.529 |

**Gaus mean : 29.2439**

**Gaus Width: 2.9183**



# B0L001S, U2-ch69, adc1

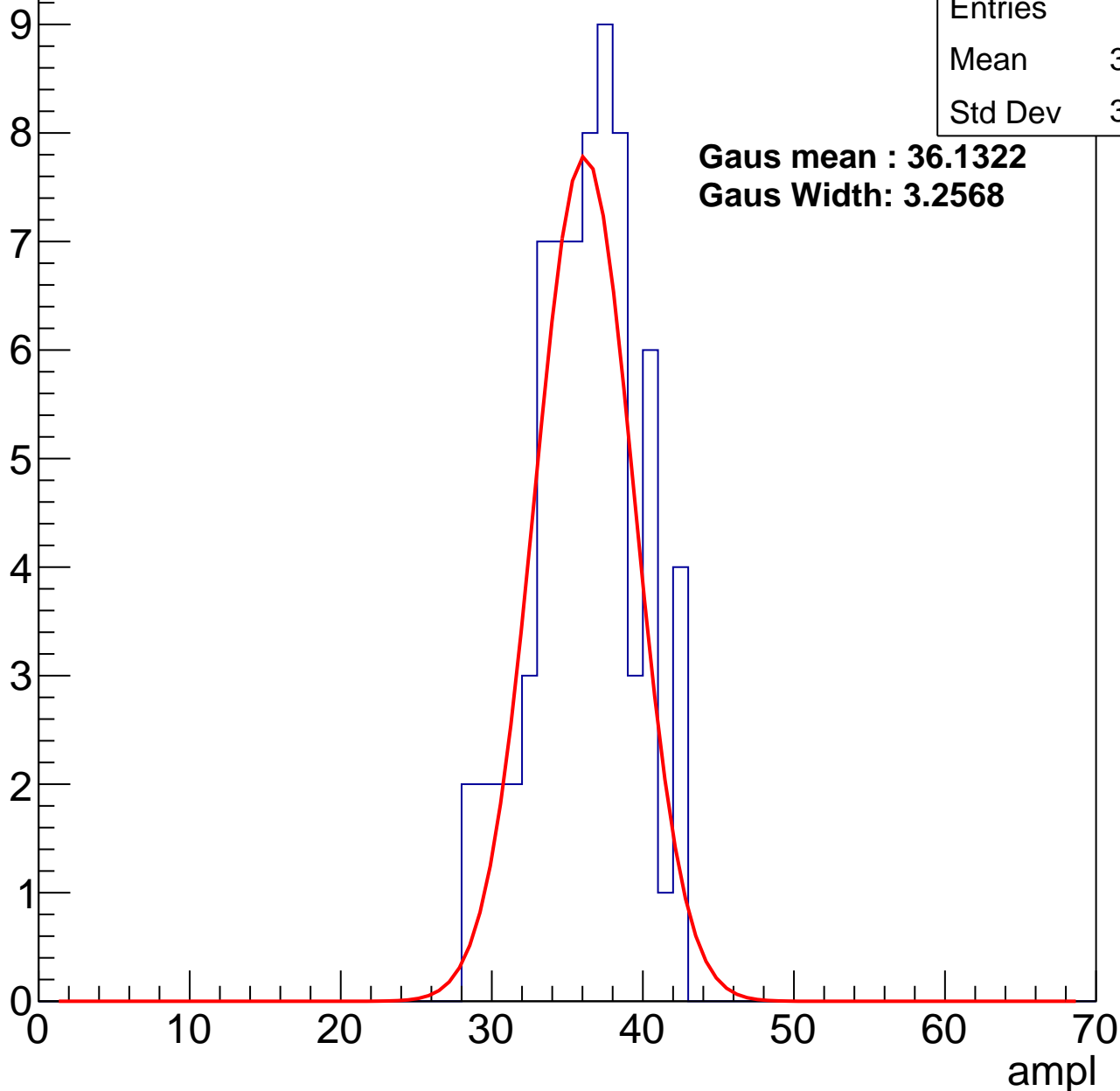
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 71    |
| Mean    | 35.73 |
| Std Dev | 3.402 |

**Gaus mean : 36.1322**

**Gaus Width: 3.2568**



# B0L001S, U2-ch69, adc2

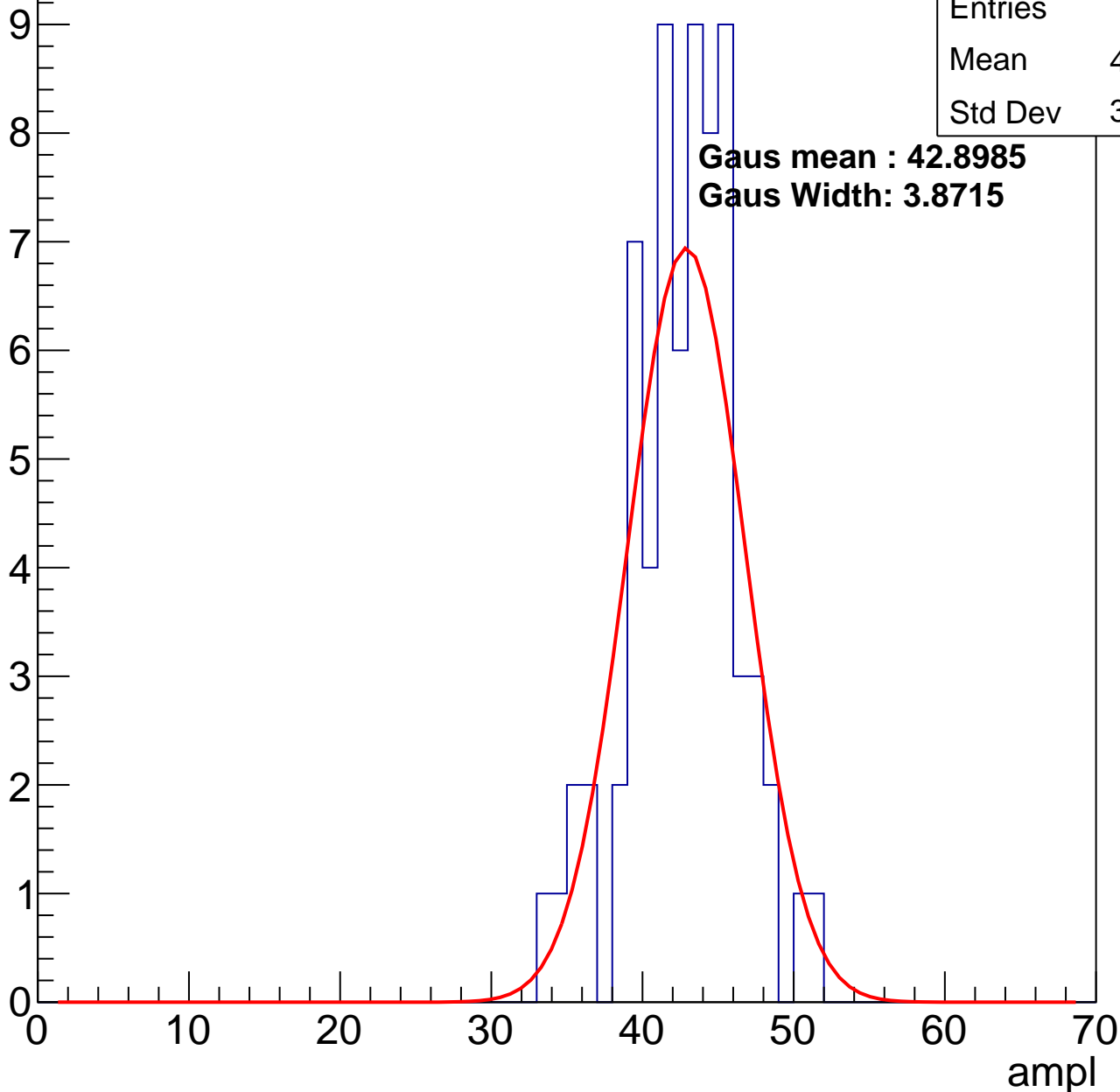
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 70    |
| Mean    | 42.27 |
| Std Dev | 3.569 |

**Gaus mean : 42.8985**

**Gaus Width: 3.8715**

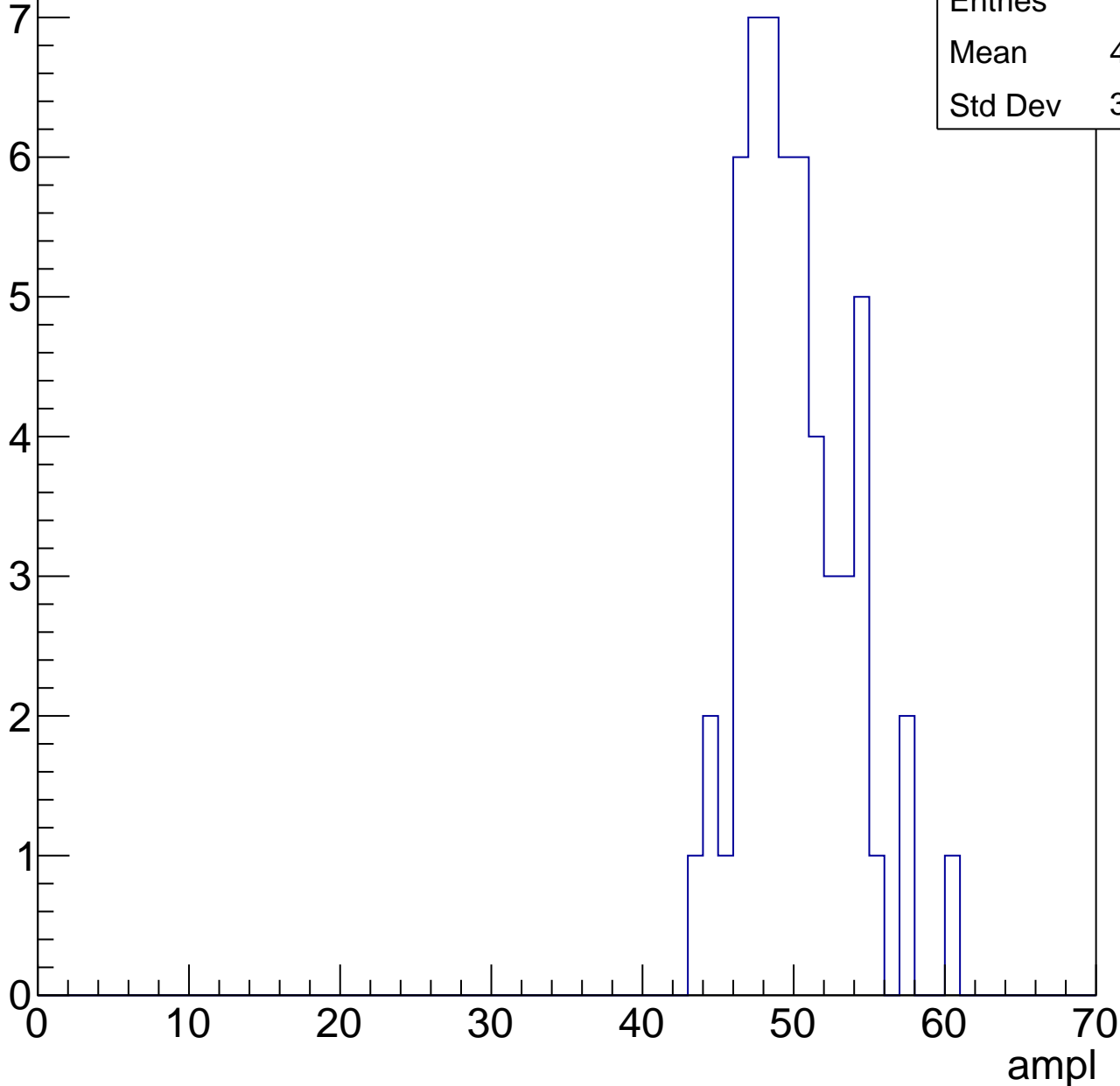


# B0L001S, U2-ch69, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

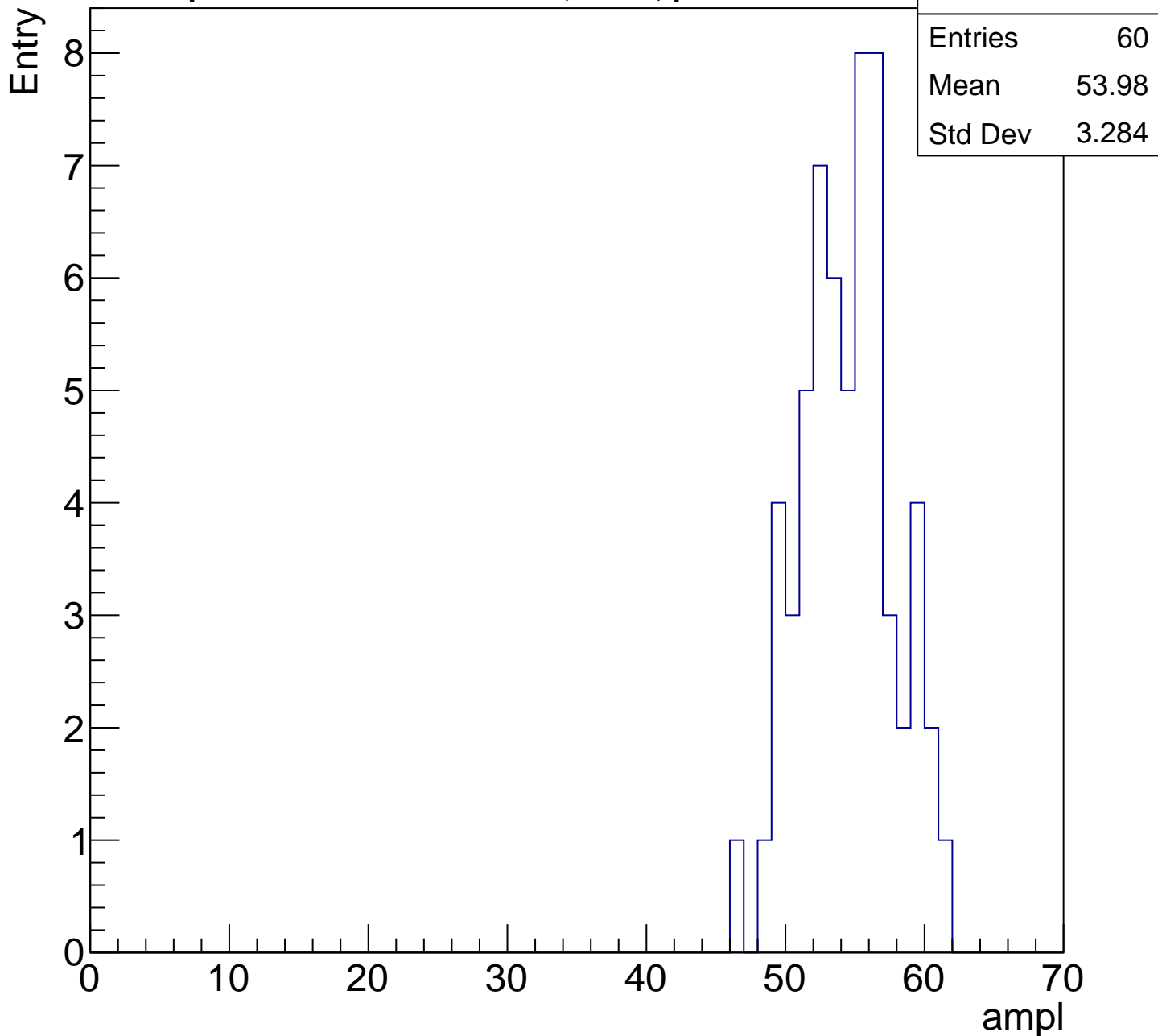
Entry

|         |       |
|---------|-------|
| Entries | 55    |
| Mean    | 49.62 |
| Std Dev | 3.508 |



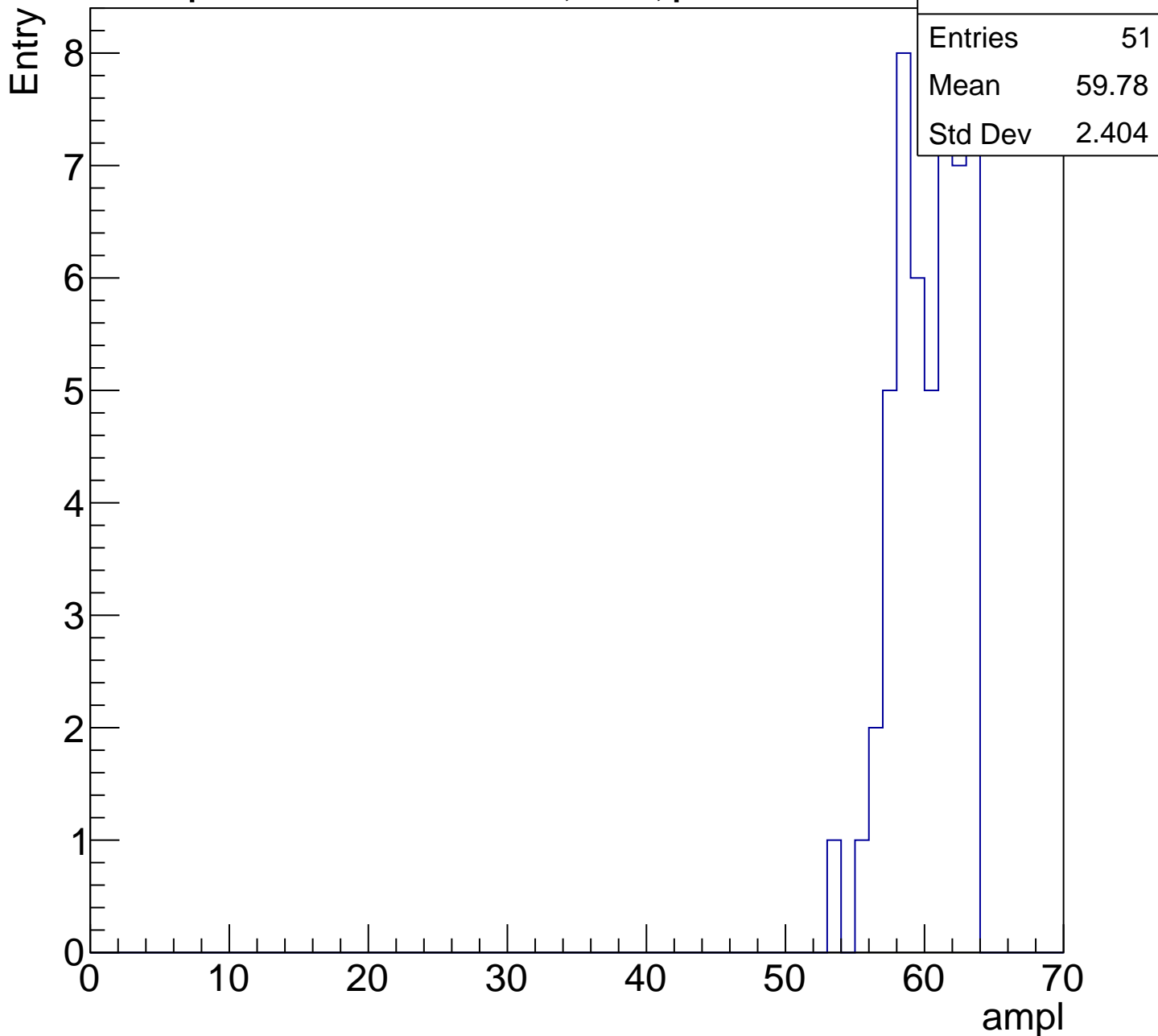
# B0L001S, U2-ch69, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U2-ch69, adc5

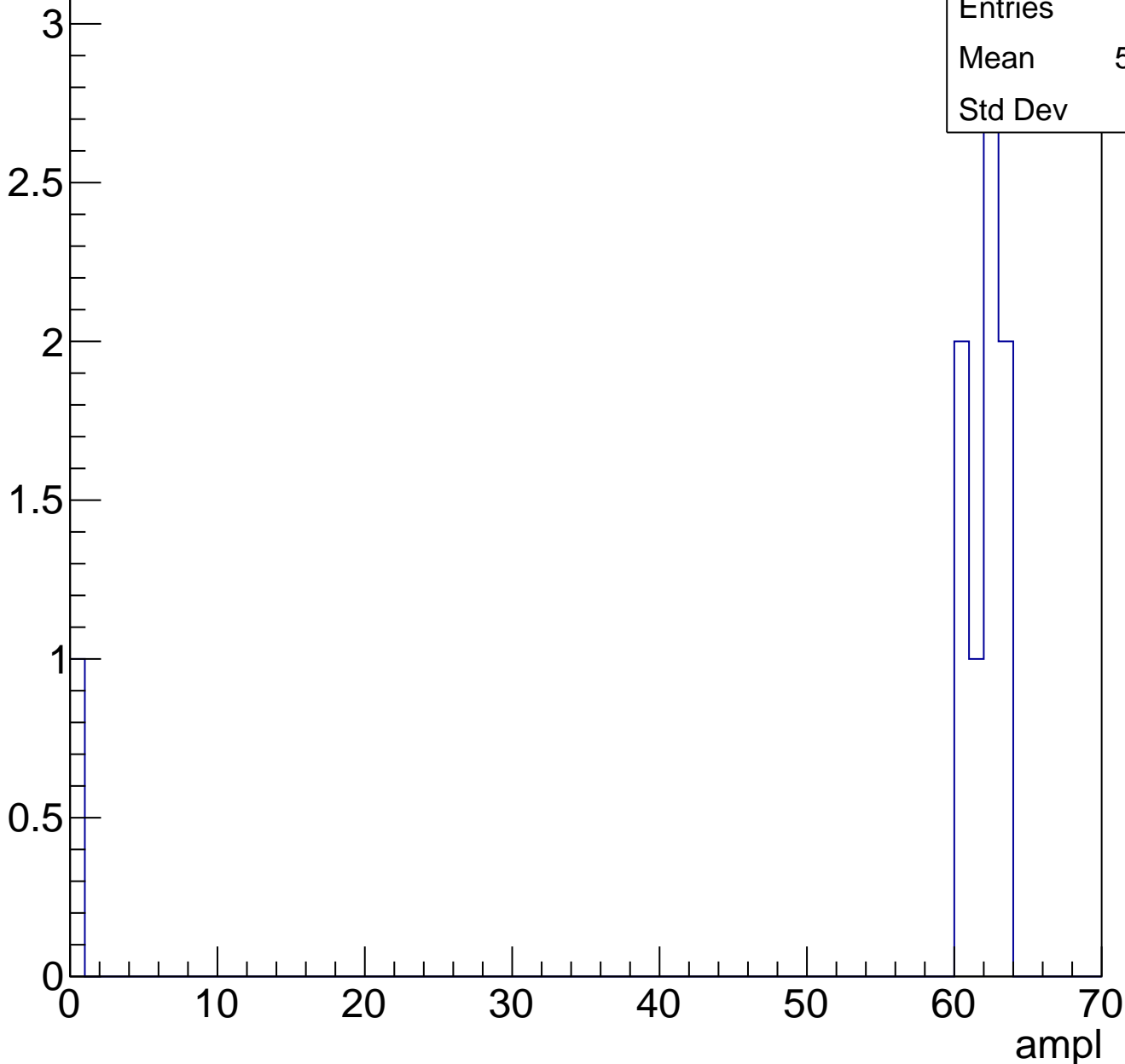
calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U2-ch69, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch69, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 2 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch70, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

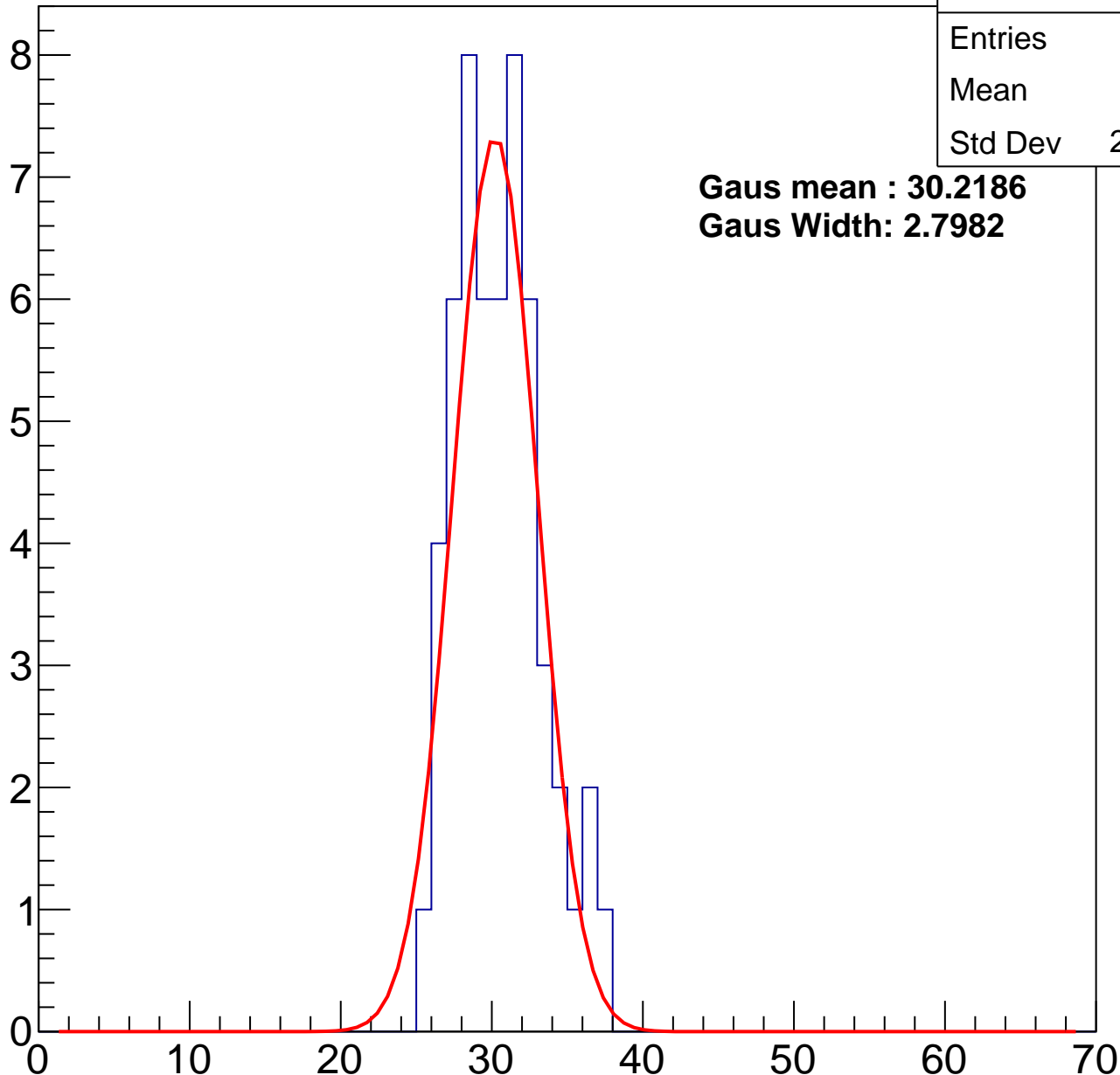
8  
7  
6  
5  
4  
3  
2  
1  
0

|         |       |
|---------|-------|
| Entries | 54    |
| Mean    | 30    |
| Std Dev | 2.782 |

**Gaus mean : 30.2186**

**Gaus Width: 2.7982**

ampl



# B0L001S, U2-ch70, adc1

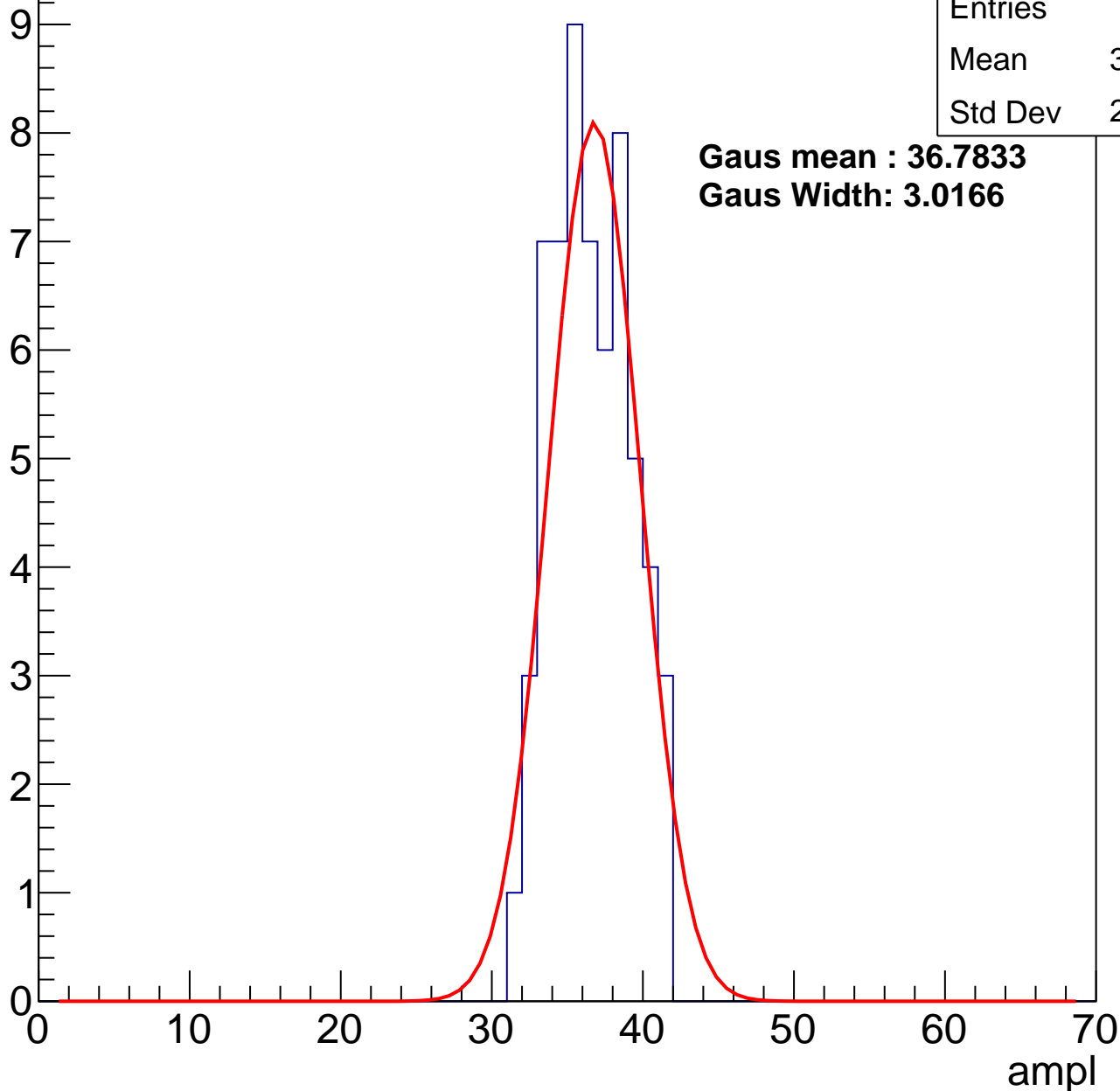
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 60    |
| Mean    | 36.12 |
| Std Dev | 2.563 |

**Gaus mean : 36.7833**

**Gaus Width: 3.0166**



# B0L001S, U2-ch70, adc2

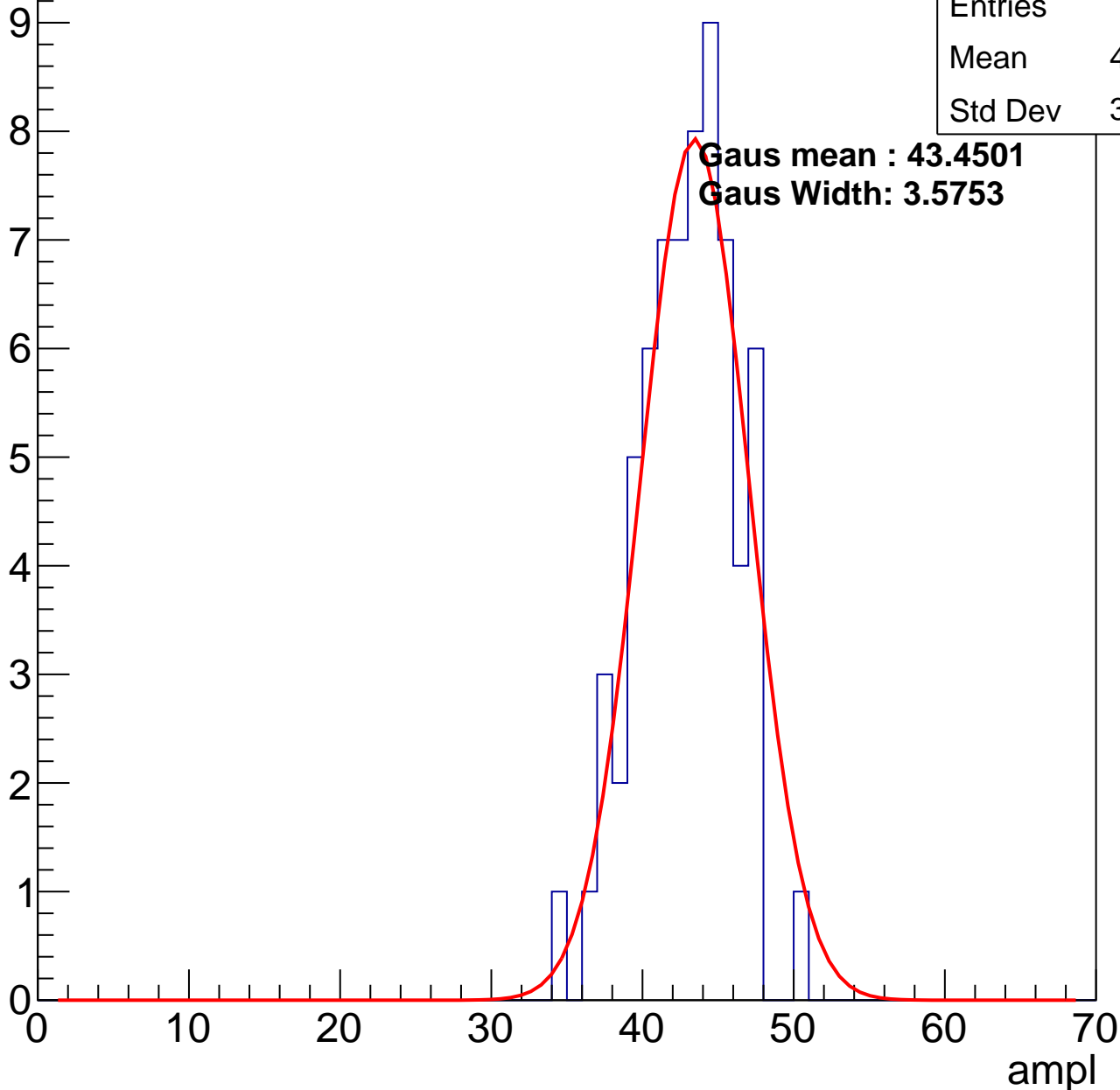
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 67    |
| Mean    | 42.45 |
| Std Dev | 3.126 |

**Gaus mean : 43.4501**

**Gaus Width: 3.5753**



# B0L001S, U2-ch70, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

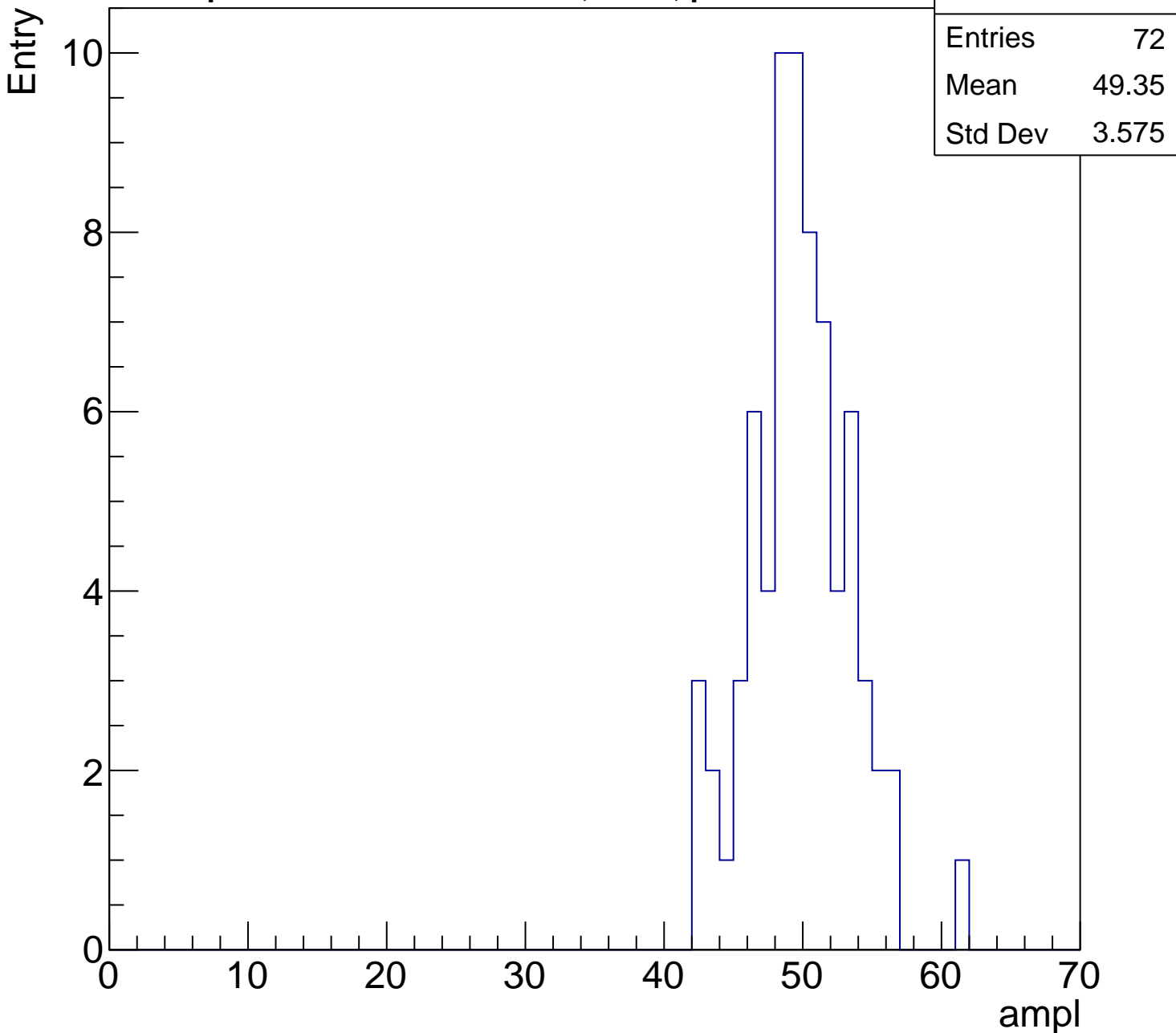
|         |       |
|---------|-------|
| Entries | 72    |
| Mean    | 49.35 |
| Std Dev | 3.575 |

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

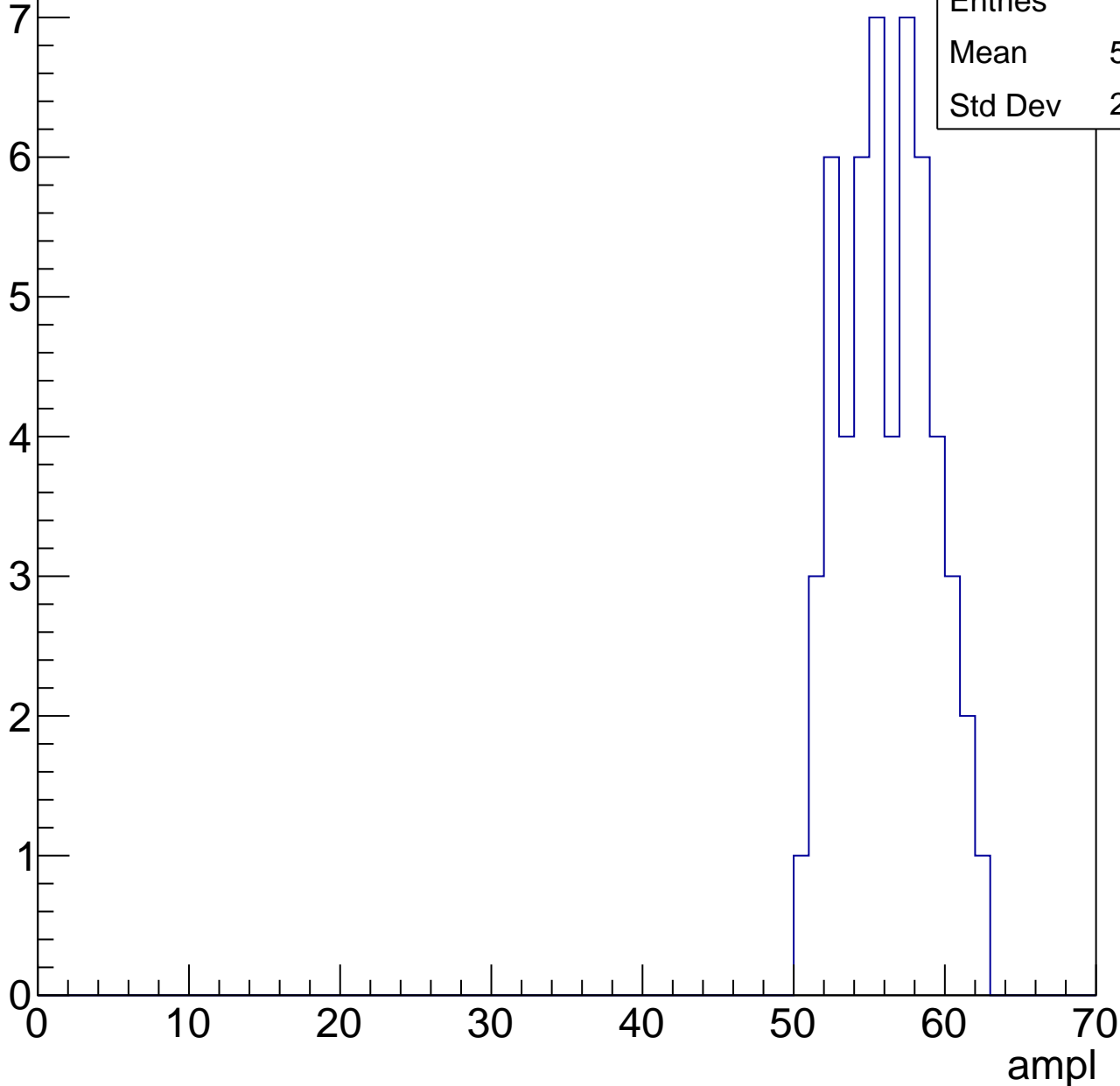


# B0L001S, U2-ch70, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

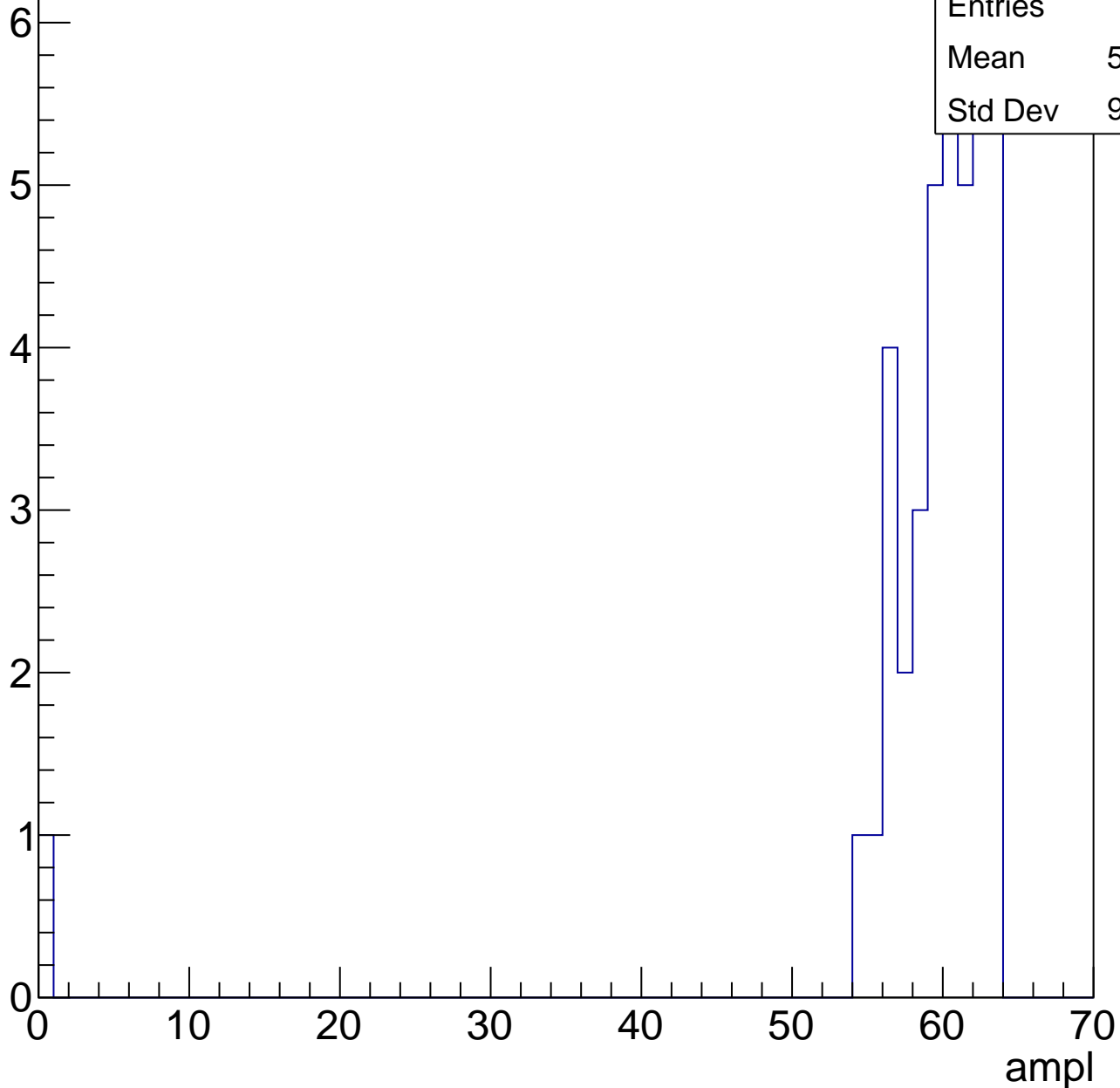
|         |       |
|---------|-------|
| Entries | 54    |
| Mean    | 55.69 |
| Std Dev | 2.949 |



# B0L001S, U2-ch70, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

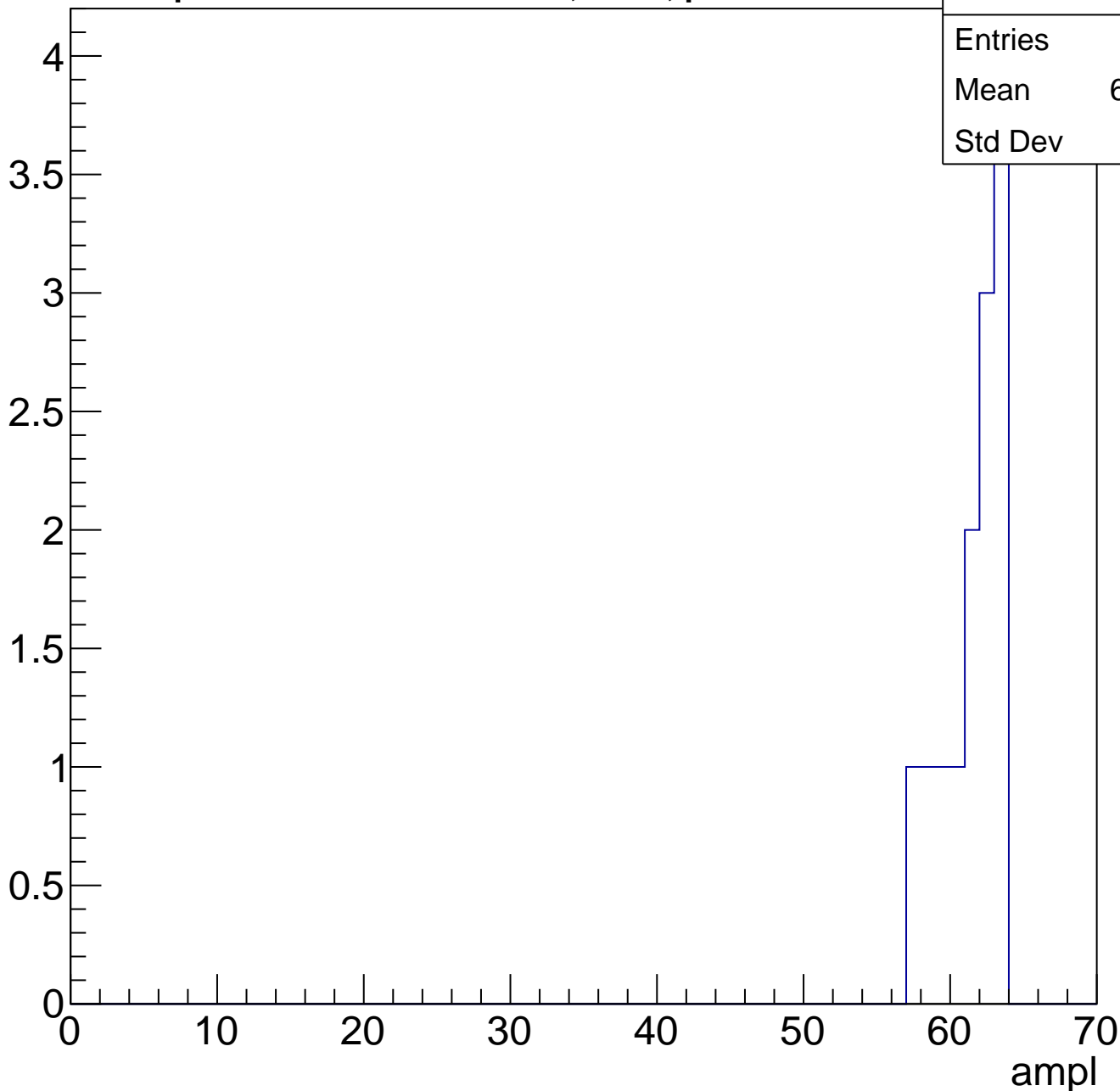
Entry



# B0L001S, U2-ch70, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch70, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 0 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch71, adc0

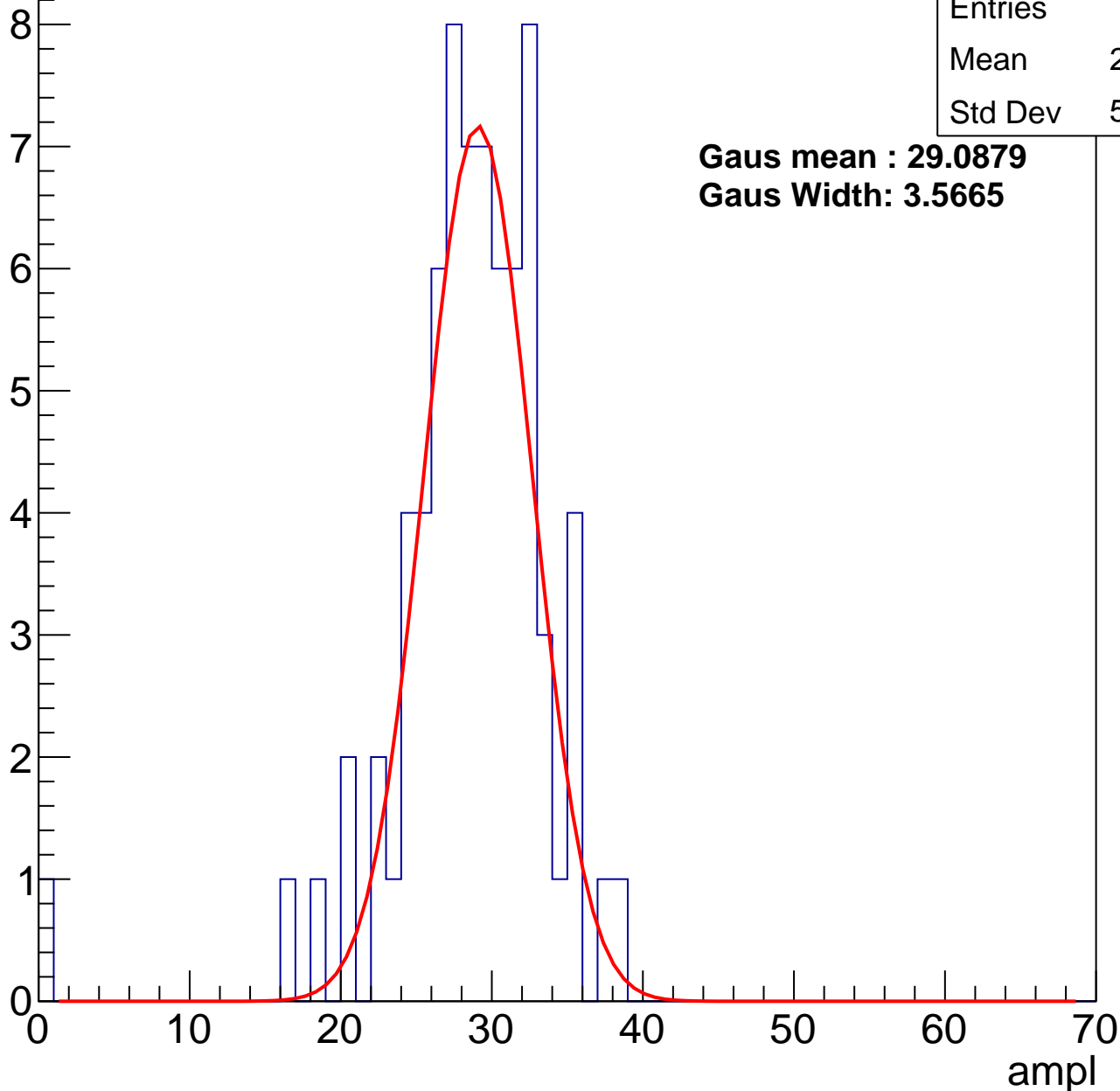
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 74    |
| Mean    | 28.08 |
| Std Dev | 5.309 |

**Gaus mean : 29.0879**

**Gaus Width: 3.5665**



# B0L001S, U2-ch71, adc1

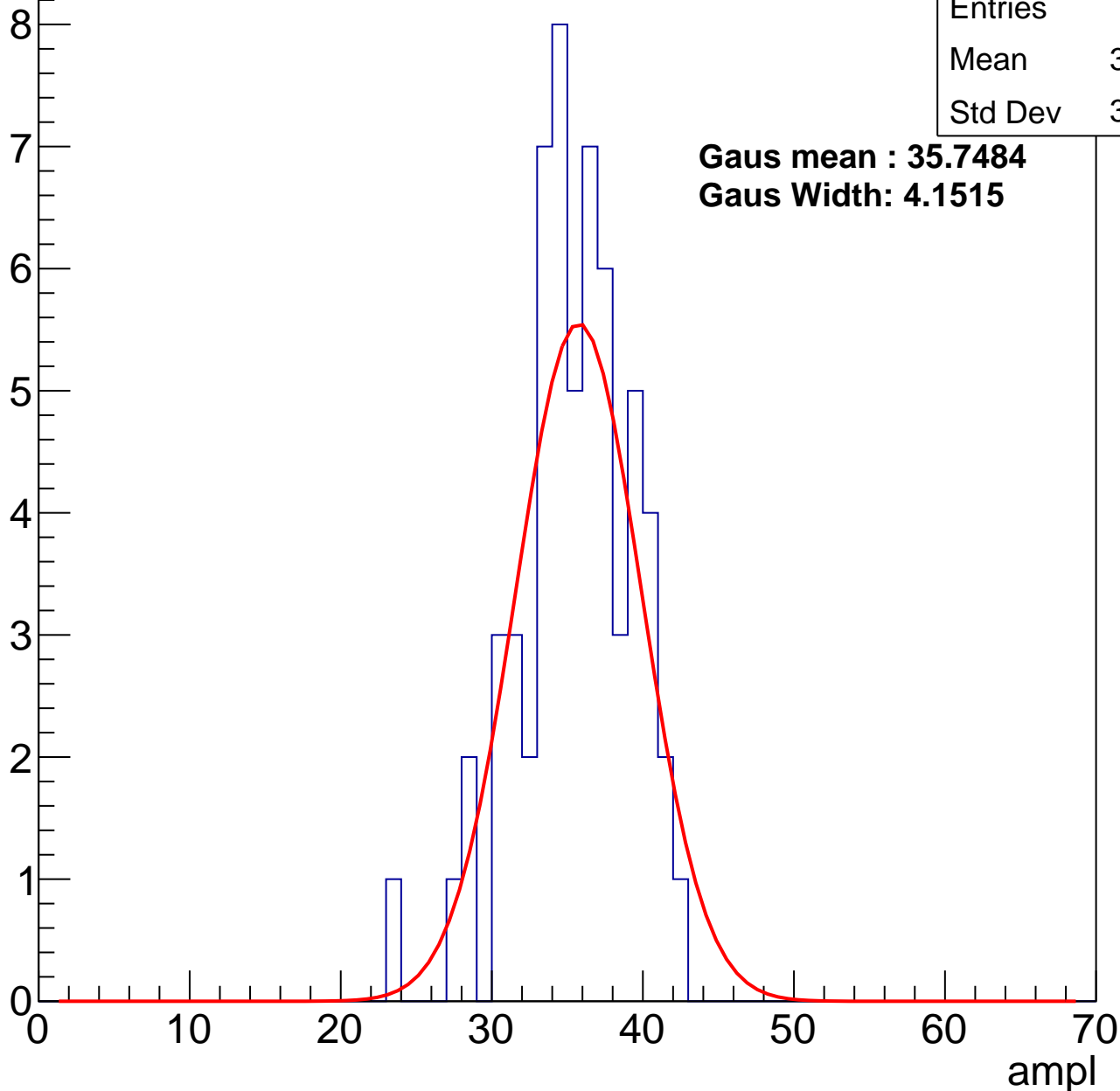
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 60    |
| Mean    | 34.97 |
| Std Dev | 3.746 |

**Gaus mean : 35.7484**

**Gaus Width: 4.1515**



# B0L001S, U2-ch71, adc2

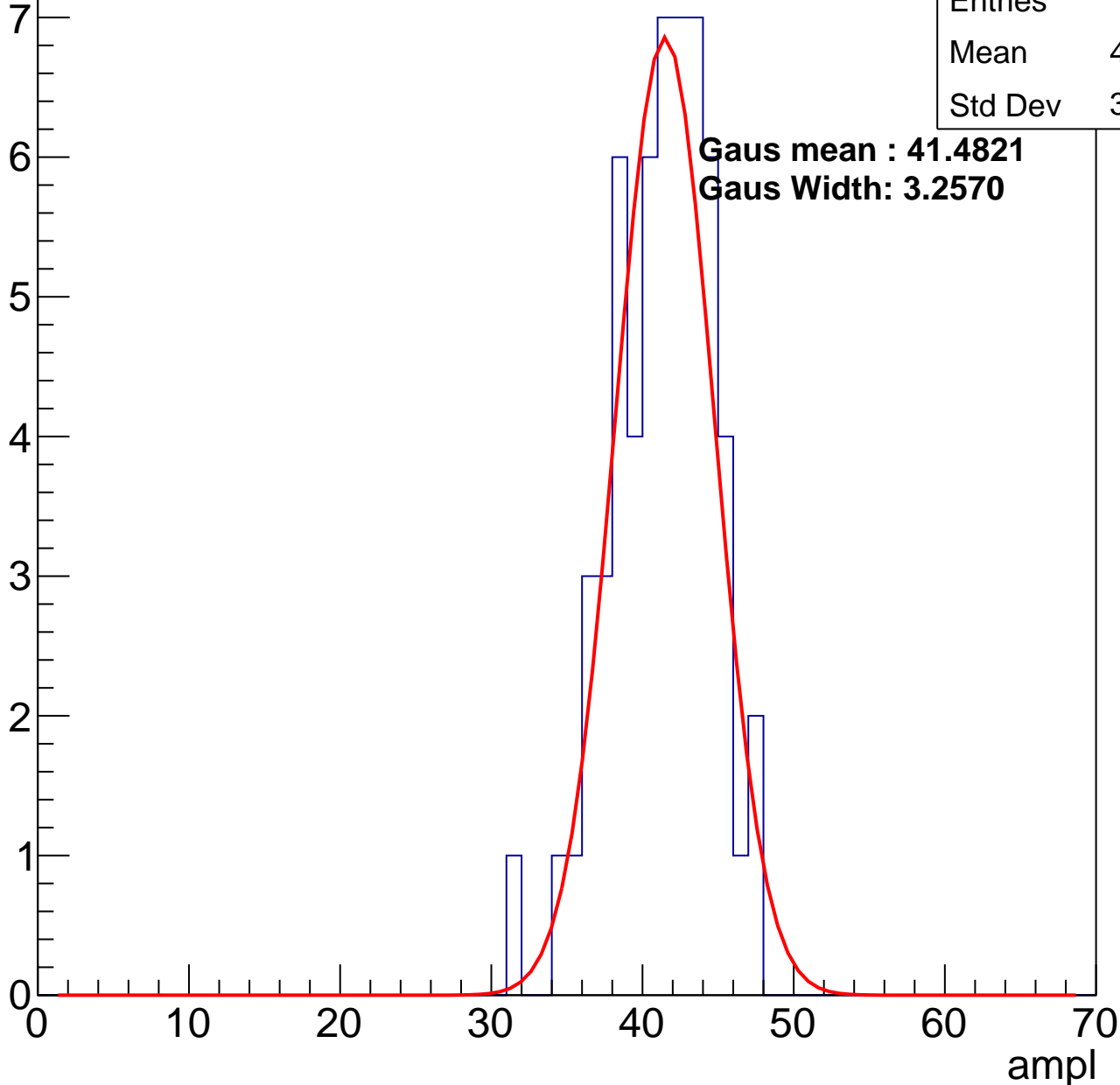
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 59    |
| Mean    | 40.83 |
| Std Dev | 3.274 |

**Gaus mean : 41.4821**

**Gaus Width: 3.2570**

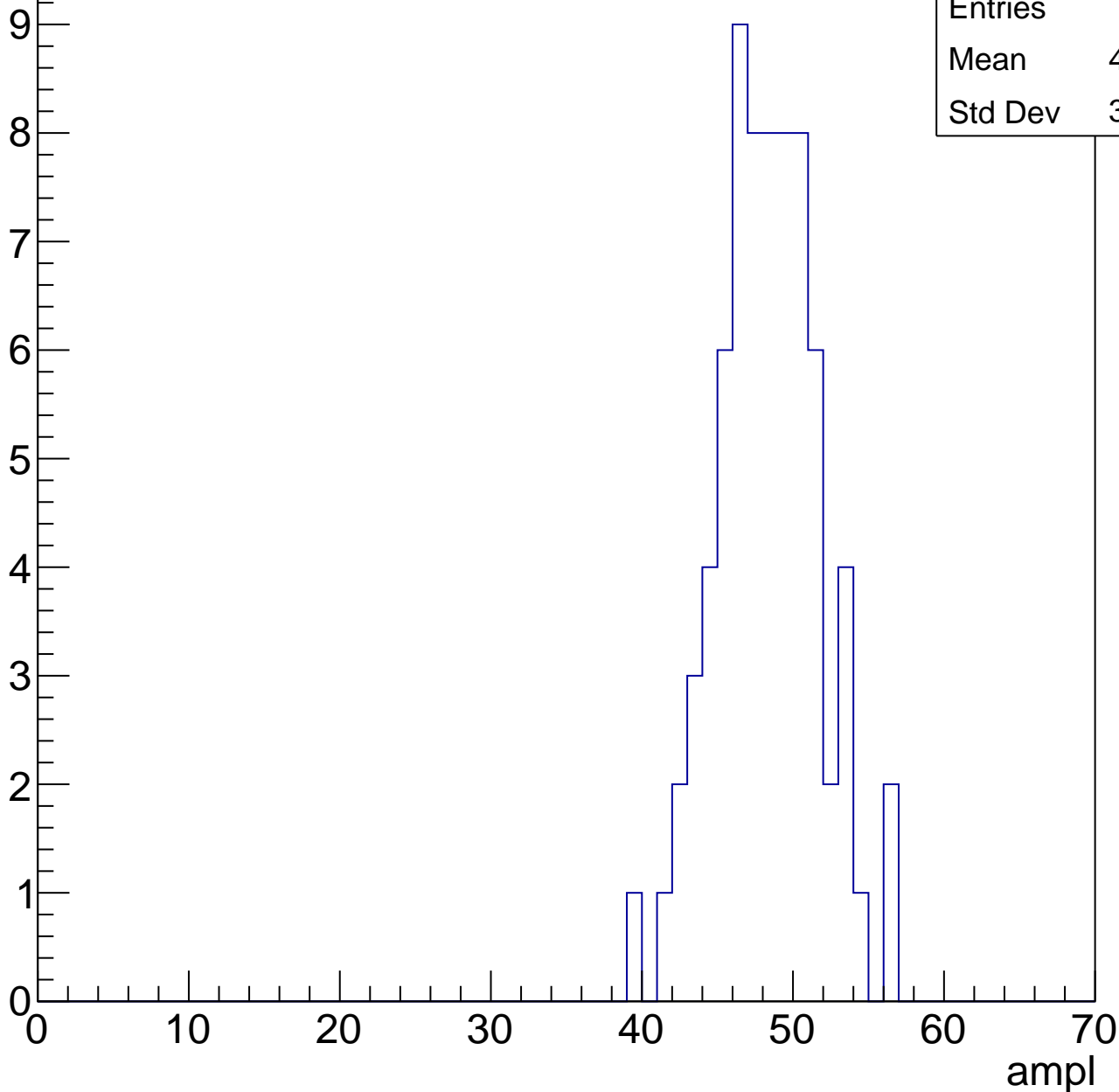


# B0L001S, U2-ch71, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 73    |
| Mean    | 47.85 |
| Std Dev | 3.367 |

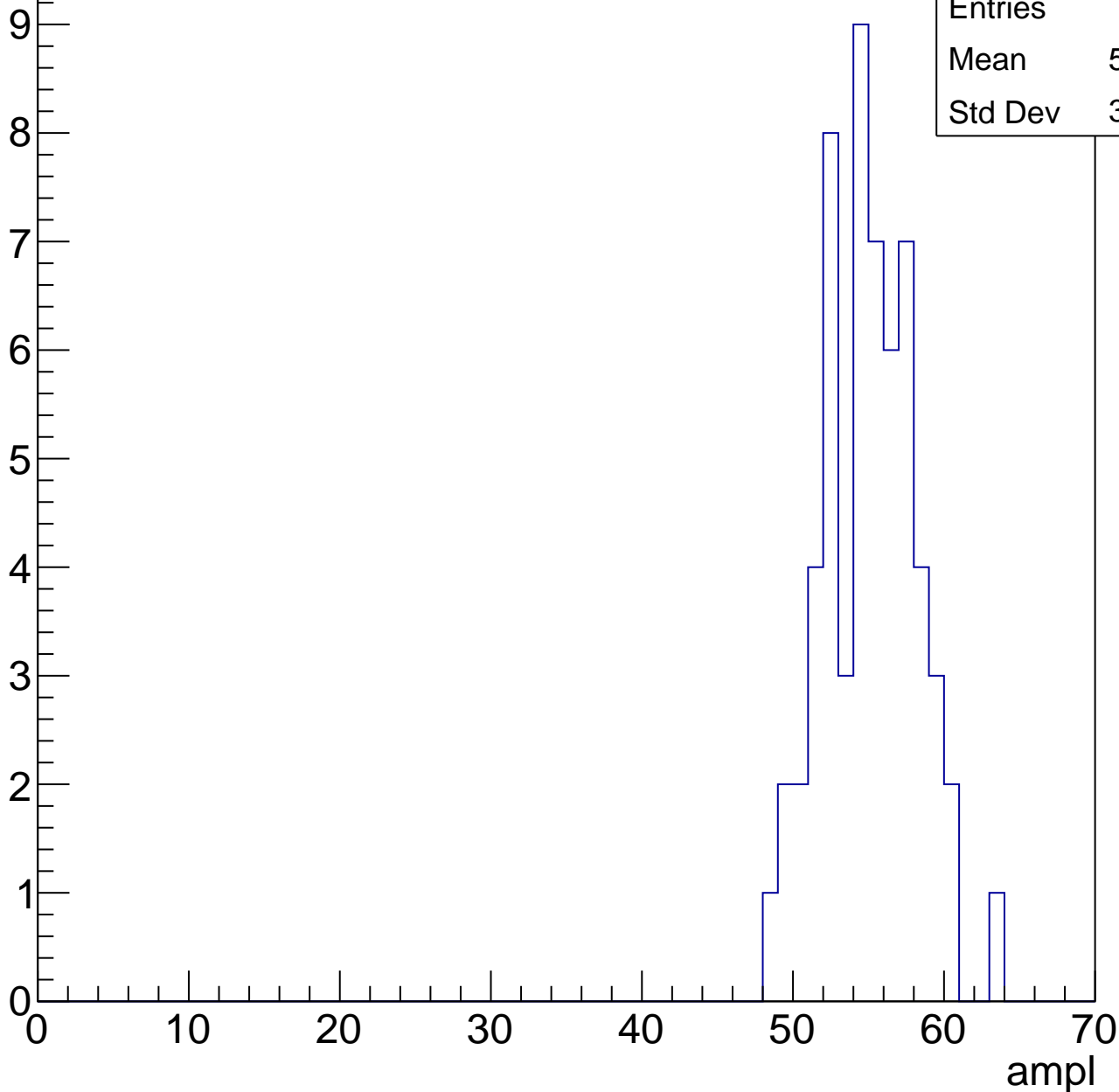


# B0L001S, U2-ch71, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 59    |
| Mean    | 54.63 |
| Std Dev | 3.058 |

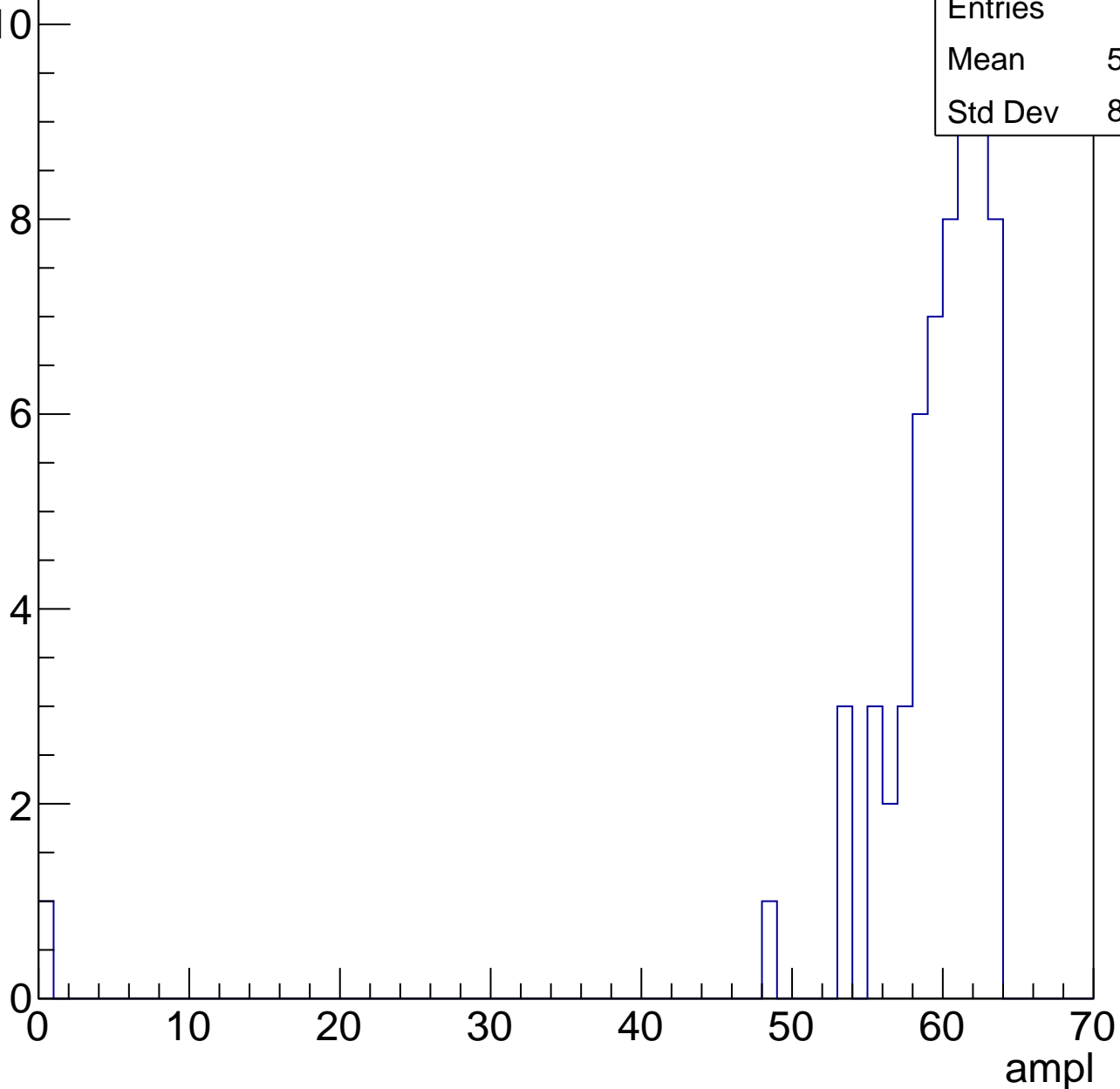


# B0L001S, U2-ch71, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 61    |
| Mean    | 58.49 |
| Std Dev | 8.133 |



# B0L001S, U2-ch71, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |    |
|---------|----|
| Entries | 1  |
| Mean    | 63 |
| Std Dev | 0  |



# B0L001S, U2-ch71, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |       |
|---------|-------|
| Entries | 3     |
| Mean    | 20.67 |
| Std Dev | 29.23 |

# B0L001S, U2-ch72, adc0

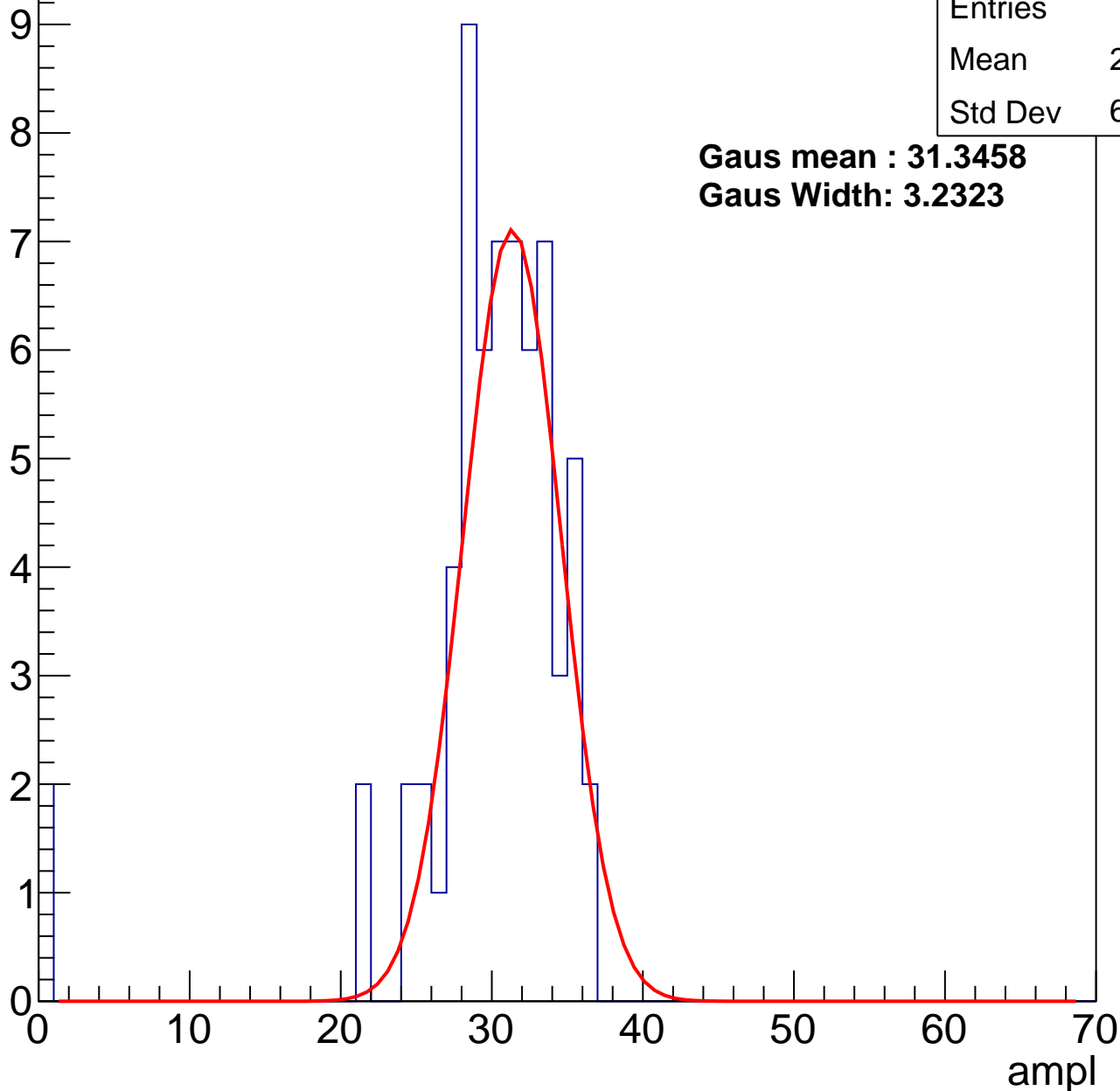
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 65    |
| Mean    | 29.22 |
| Std Dev | 6.173 |

**Gaus mean : 31.3458**

**Gaus Width: 3.2323**



# B0L001S, U2-ch72, adc1

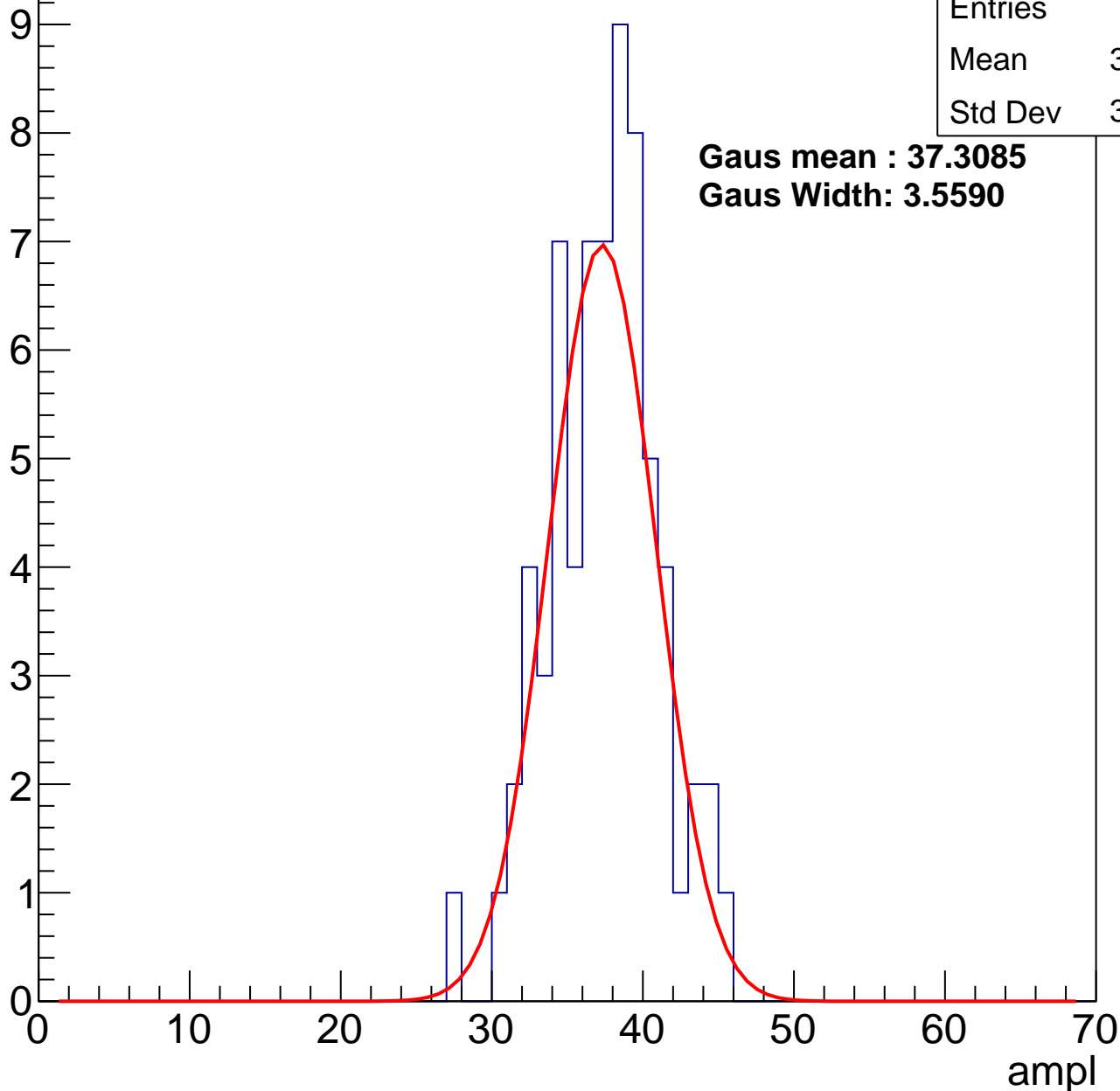
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 68    |
| Mean    | 36.97 |
| Std Dev | 3.564 |

**Gaus mean : 37.3085**

**Gaus Width: 3.5590**



# B0L001S, U2-ch72, adc2

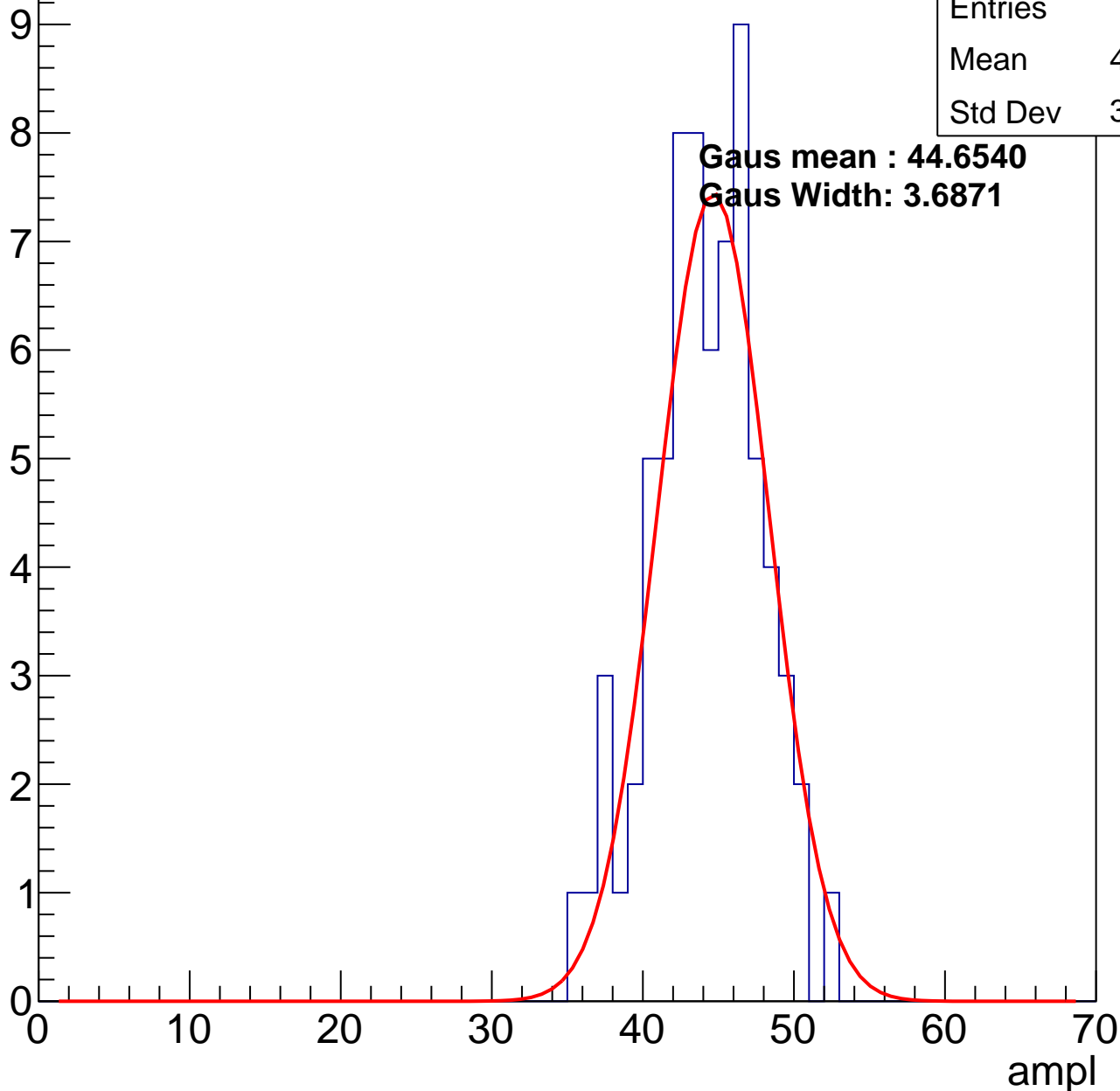
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 71    |
| Mean    | 43.69 |
| Std Dev | 3.559 |

**Gaus mean : 44.6540**

**Gaus Width: 3.6871**

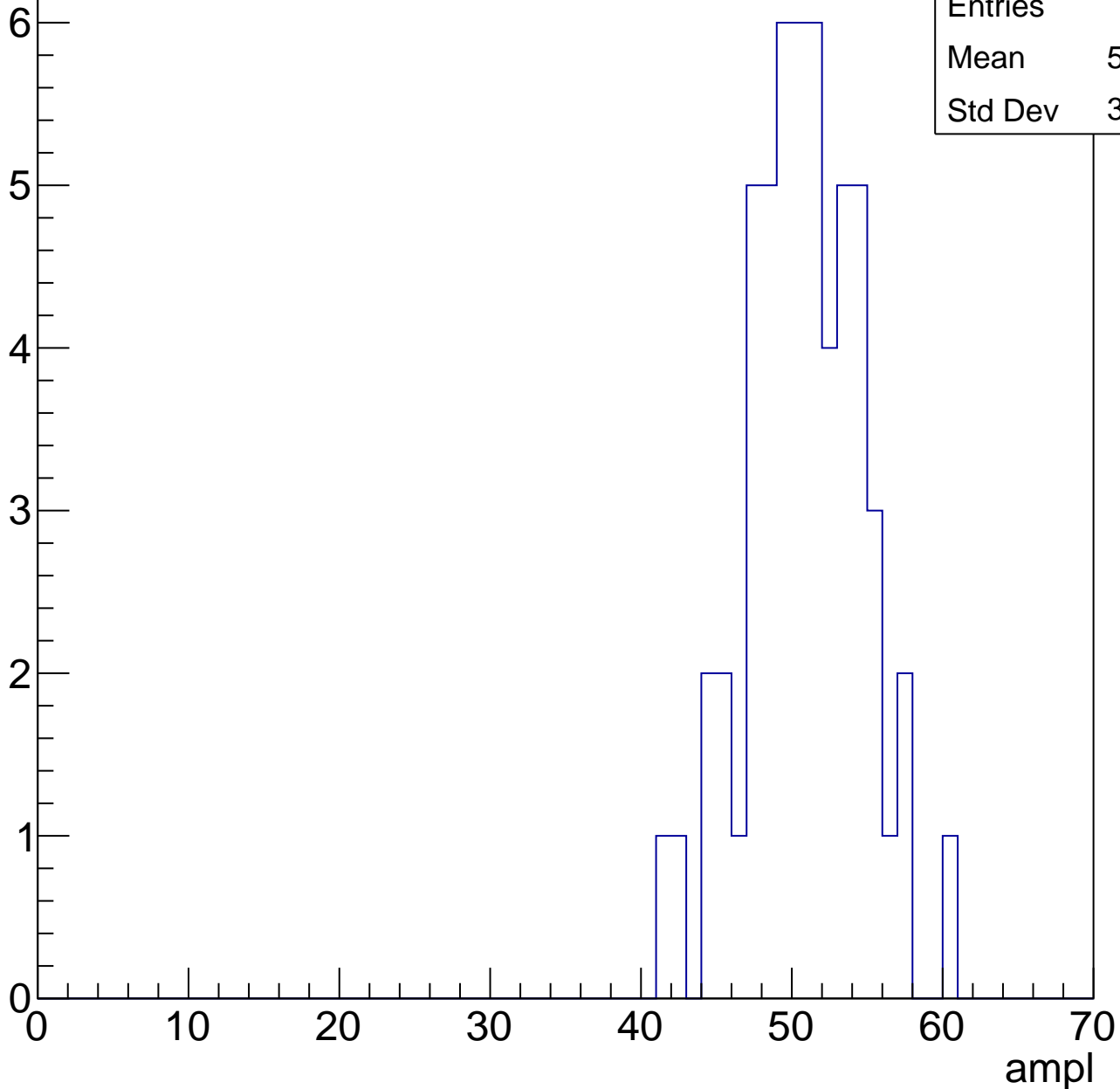


# B0L001S, U2-ch72, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 56    |
| Mean    | 50.36 |
| Std Dev | 3.786 |

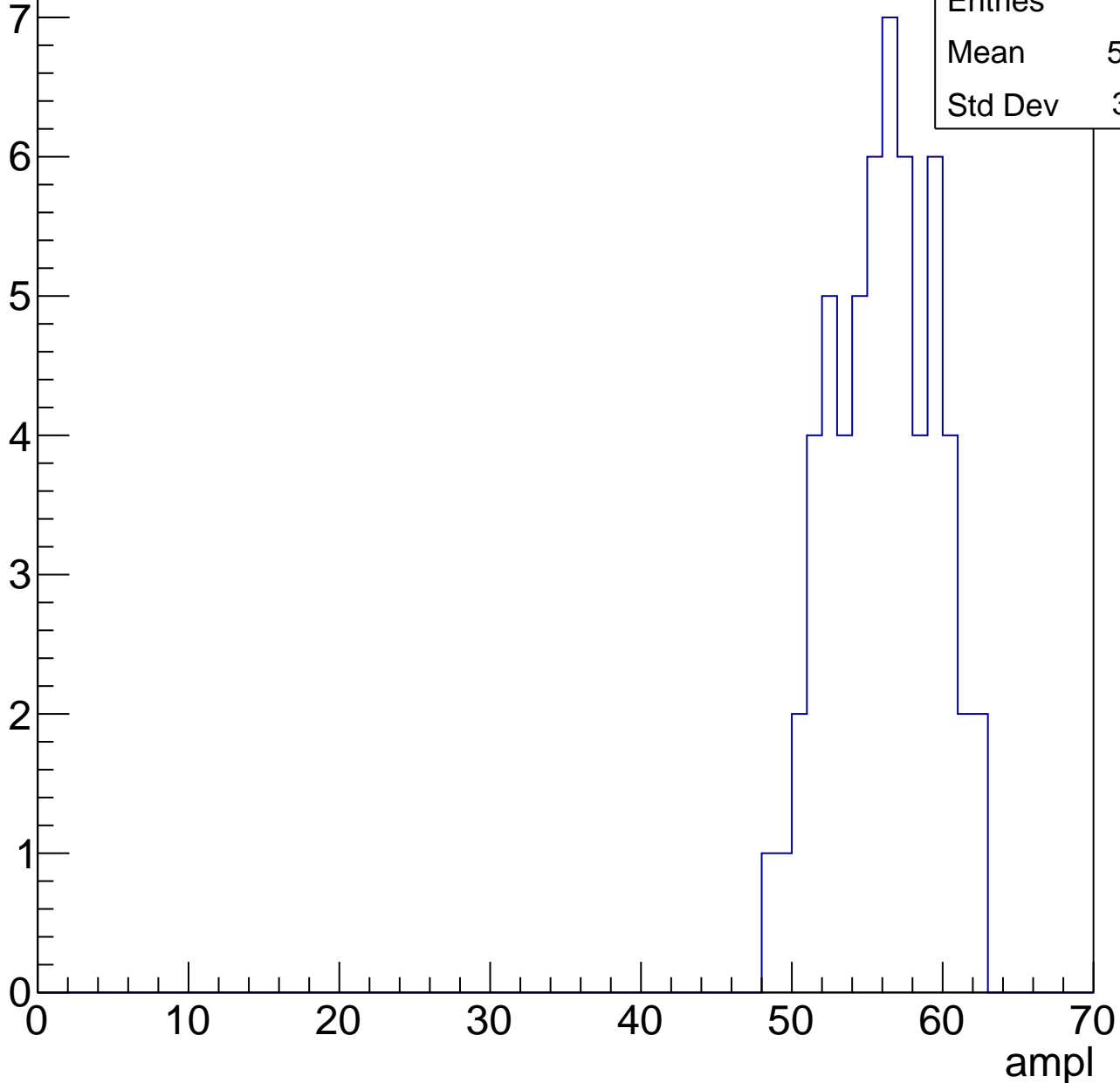


# B0L001S, U2-ch72, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 59    |
| Mean    | 55.58 |
| Std Dev | 3.391 |

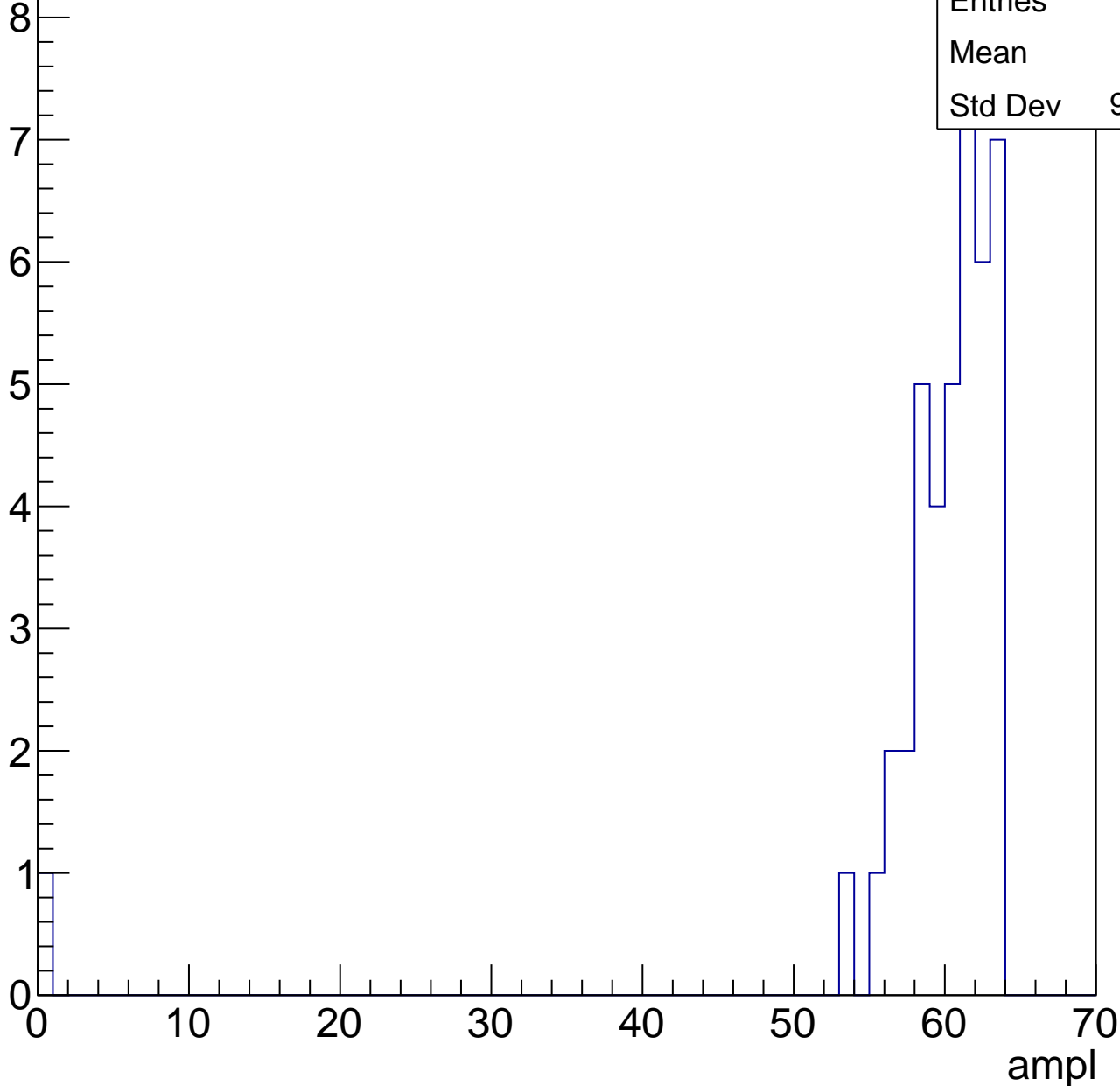


# B0L001S, U2-ch72, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

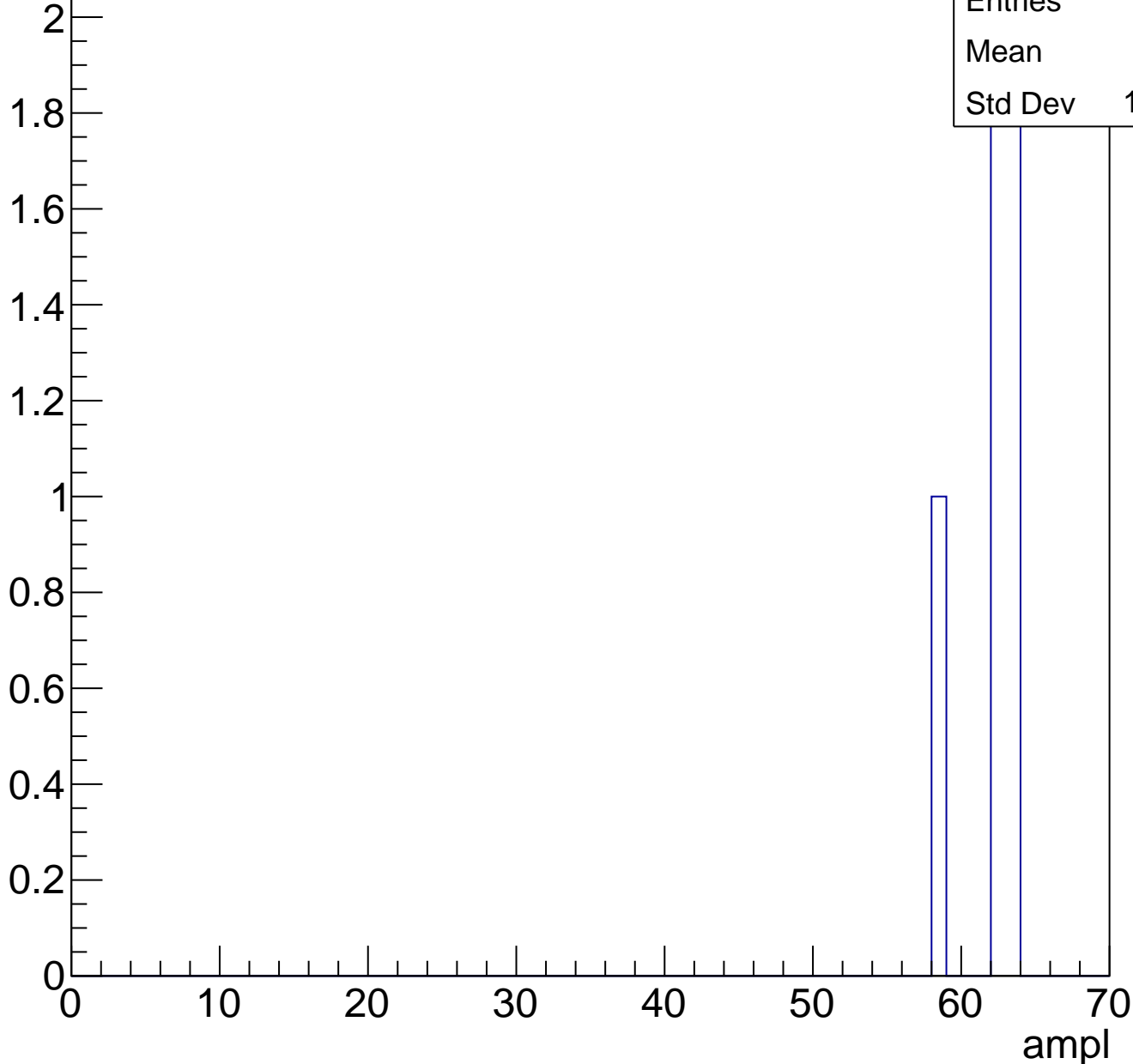
|         |       |
|---------|-------|
| Entries | 42    |
| Mean    | 58.6  |
| Std Dev | 9.462 |



# B0L001S, U2-ch72, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch72, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U2-ch73, adc0

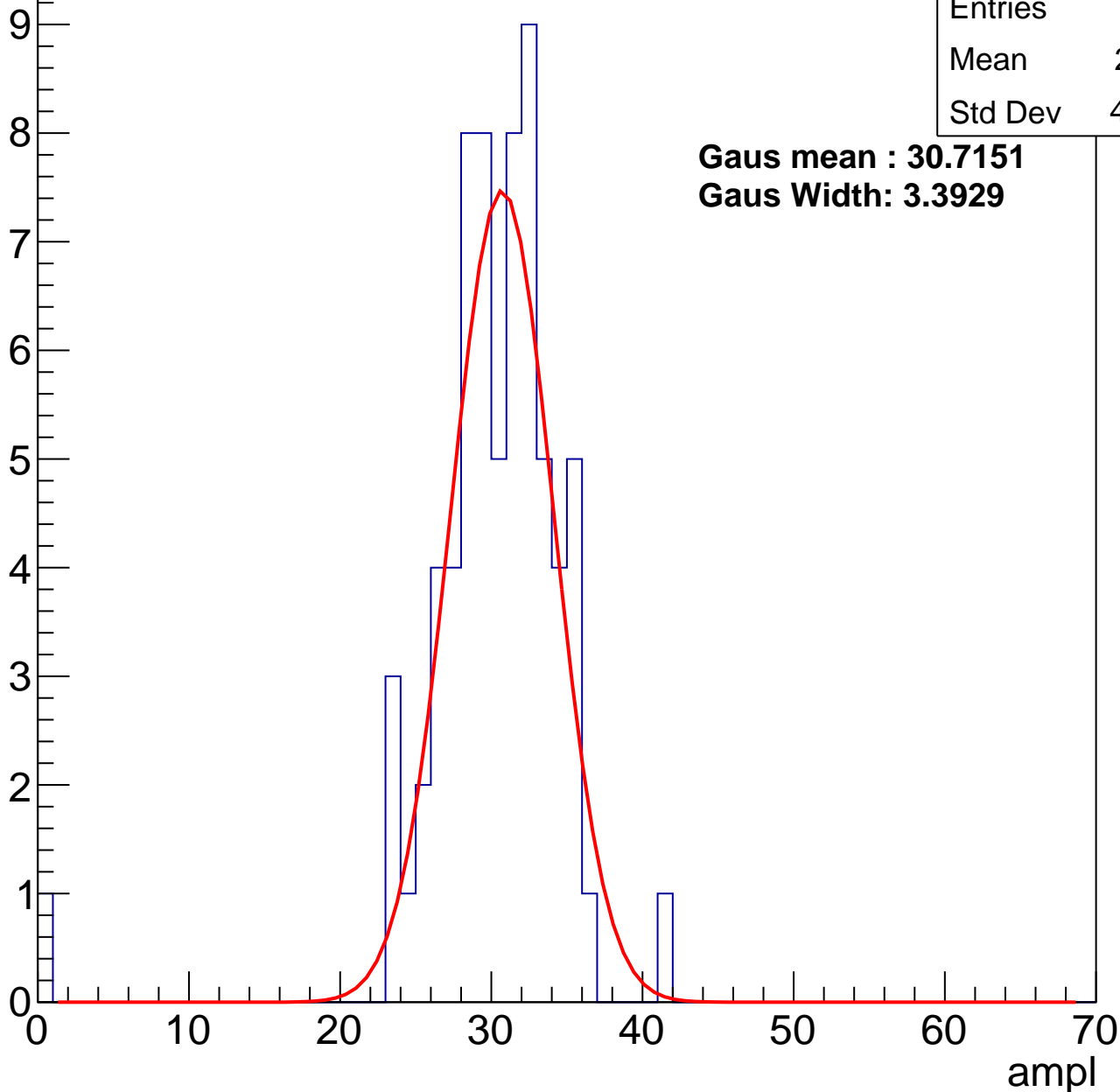
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 69    |
| Mean    | 29.71 |
| Std Dev | 4.967 |

**Gaus mean : 30.7151**

**Gaus Width: 3.3929**



# B0L001S, U2-ch73, adc1

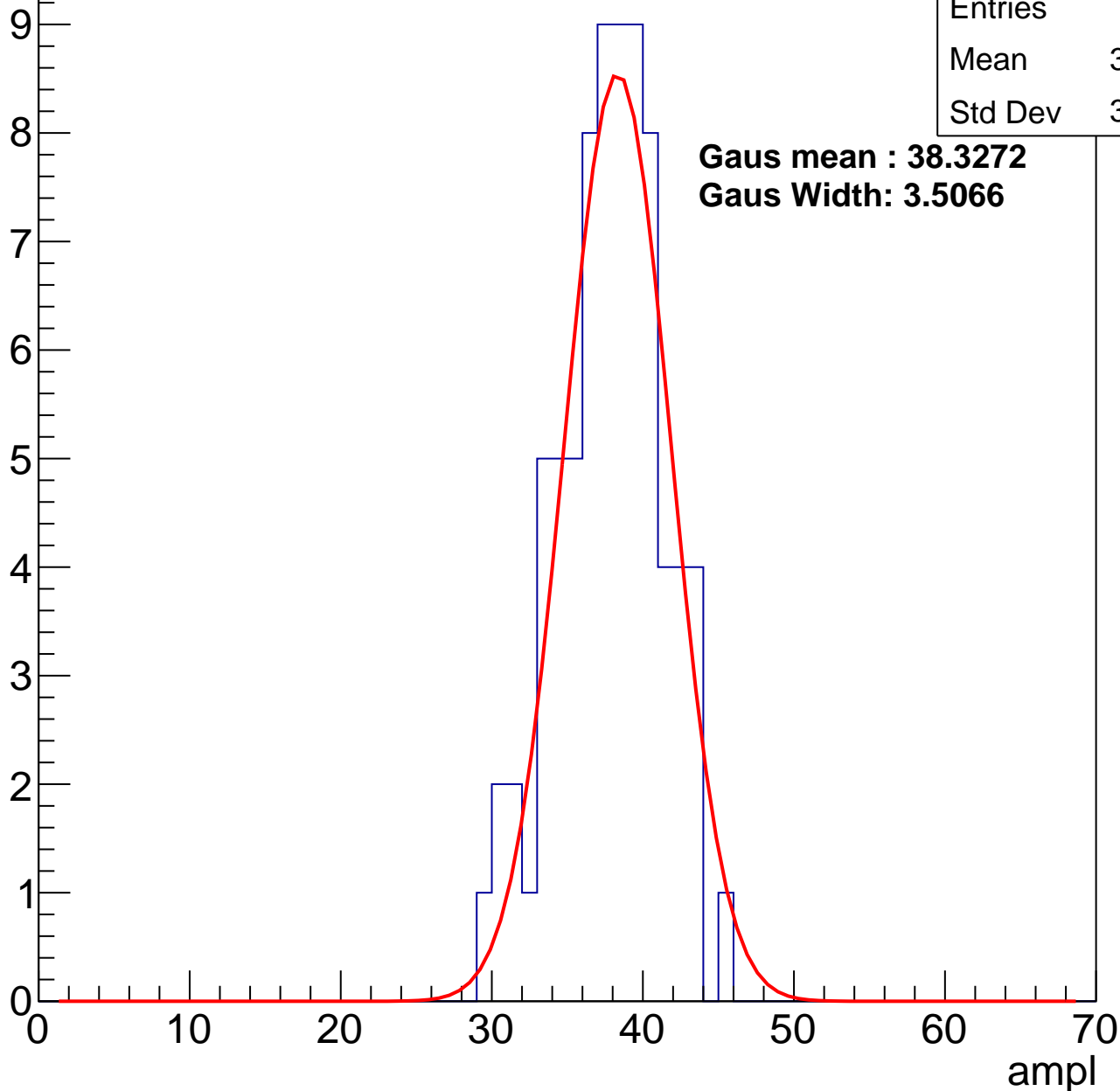
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 77    |
| Mean    | 37.35 |
| Std Dev | 3.403 |

**Gaus mean : 38.3272**

**Gaus Width: 3.5066**



# B0L001S, U2-ch73, adc2

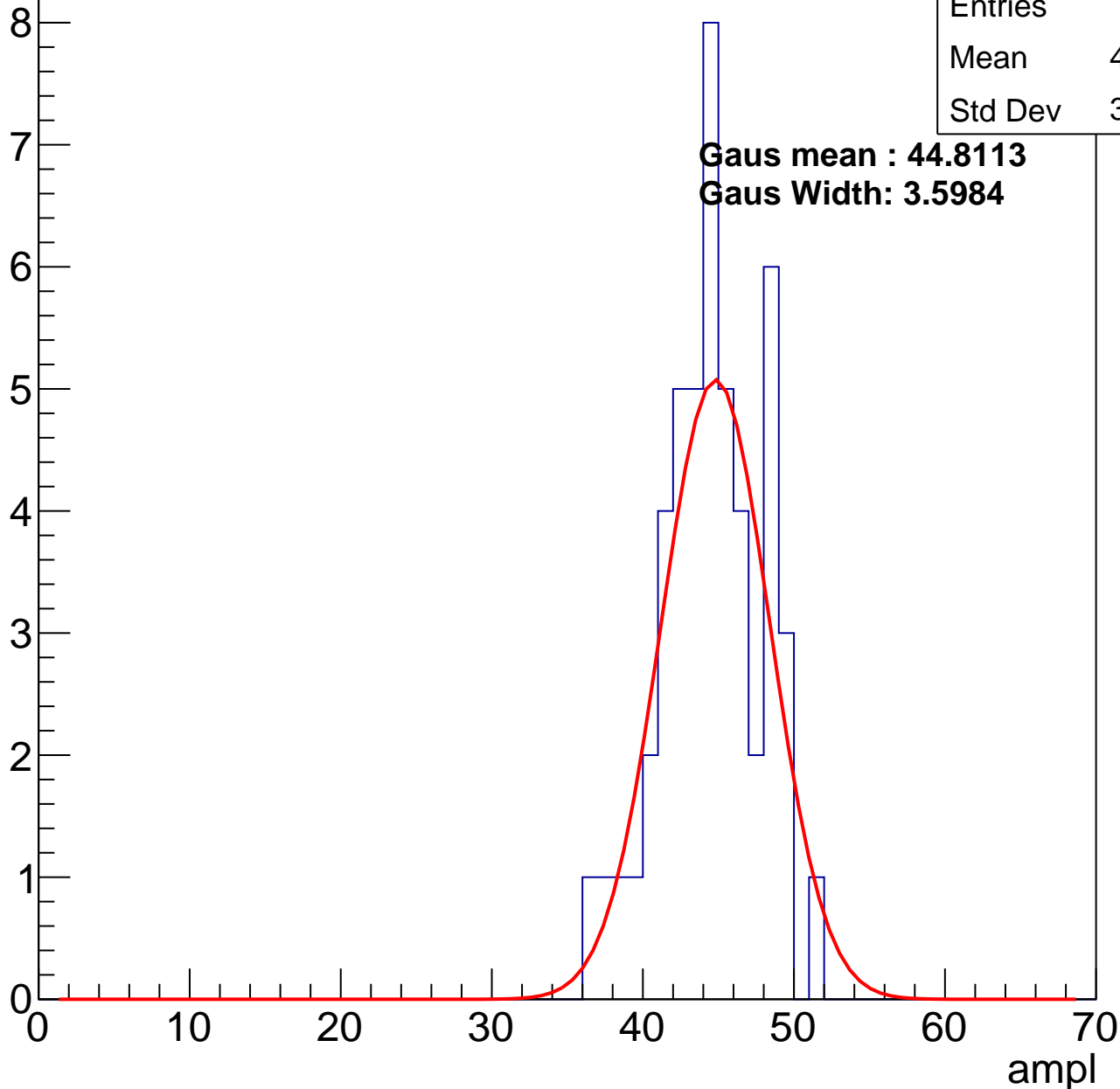
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 49    |
| Mean    | 44.08 |
| Std Dev | 3.275 |

**Gaus mean : 44.8113**

**Gaus Width: 3.5984**

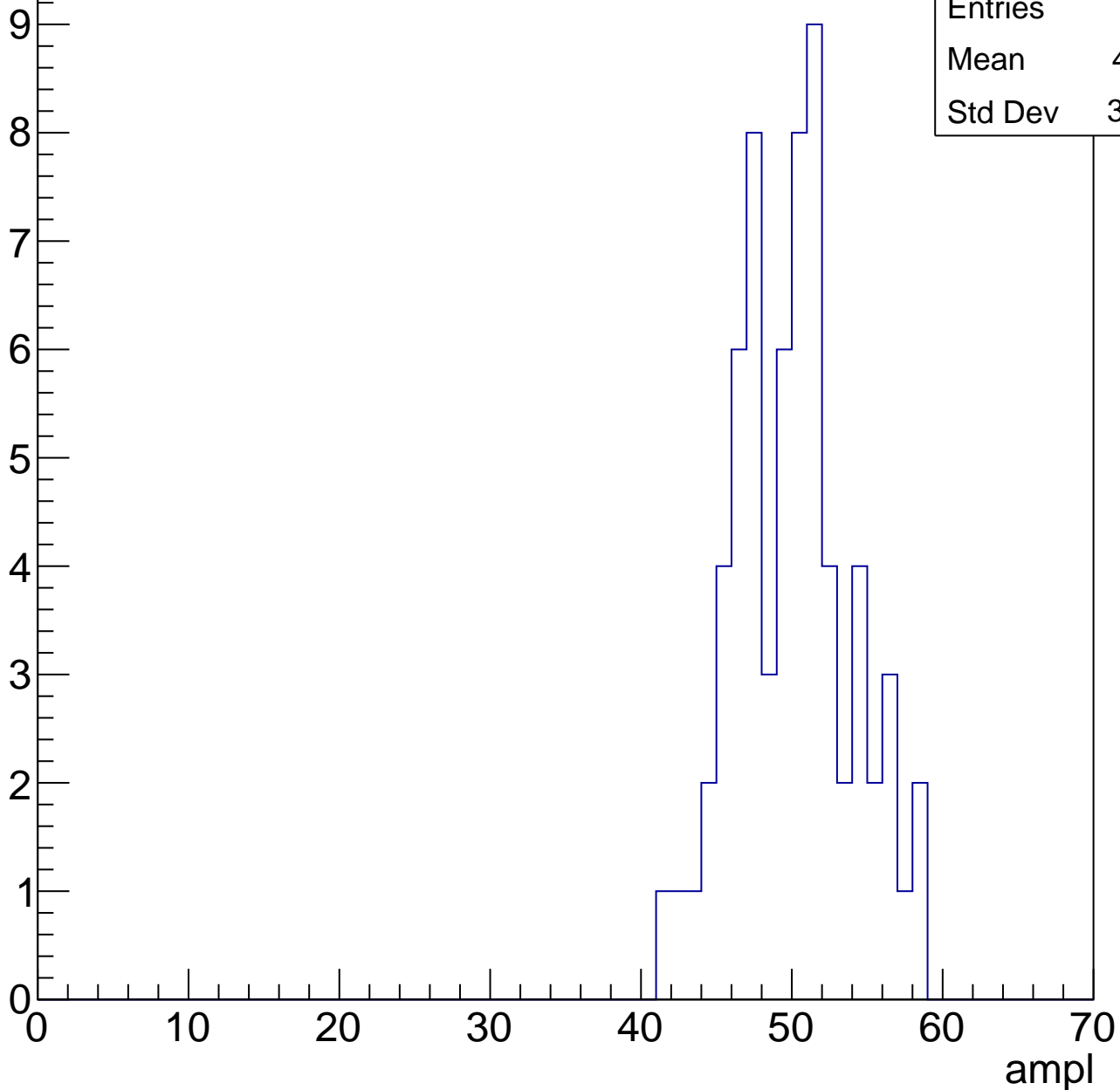


# B0L001S, U2-ch73, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

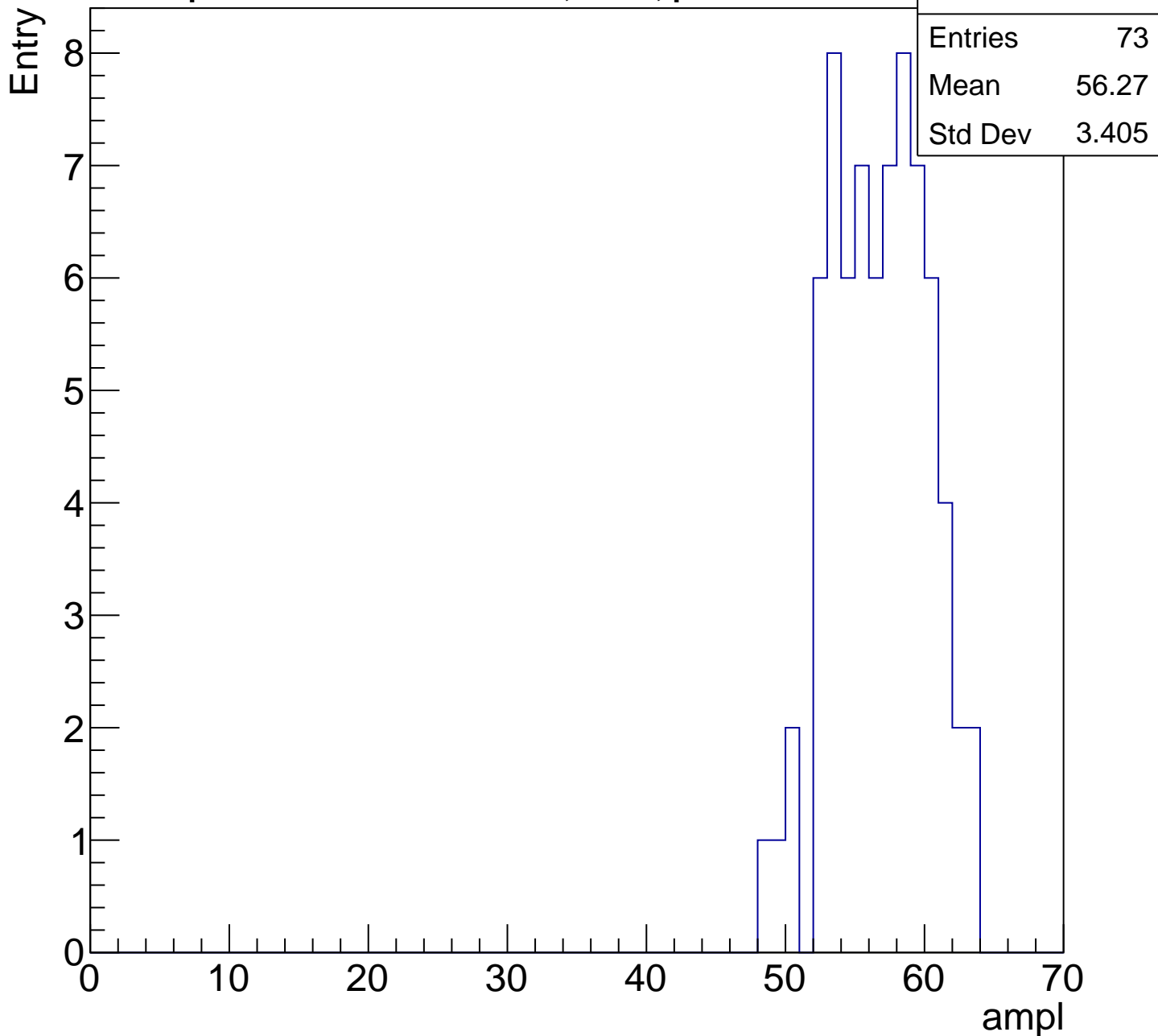
Entry

|         |       |
|---------|-------|
| Entries | 67    |
| Mean    | 49.61 |
| Std Dev | 3.832 |



# B0L001S, U2-ch73, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

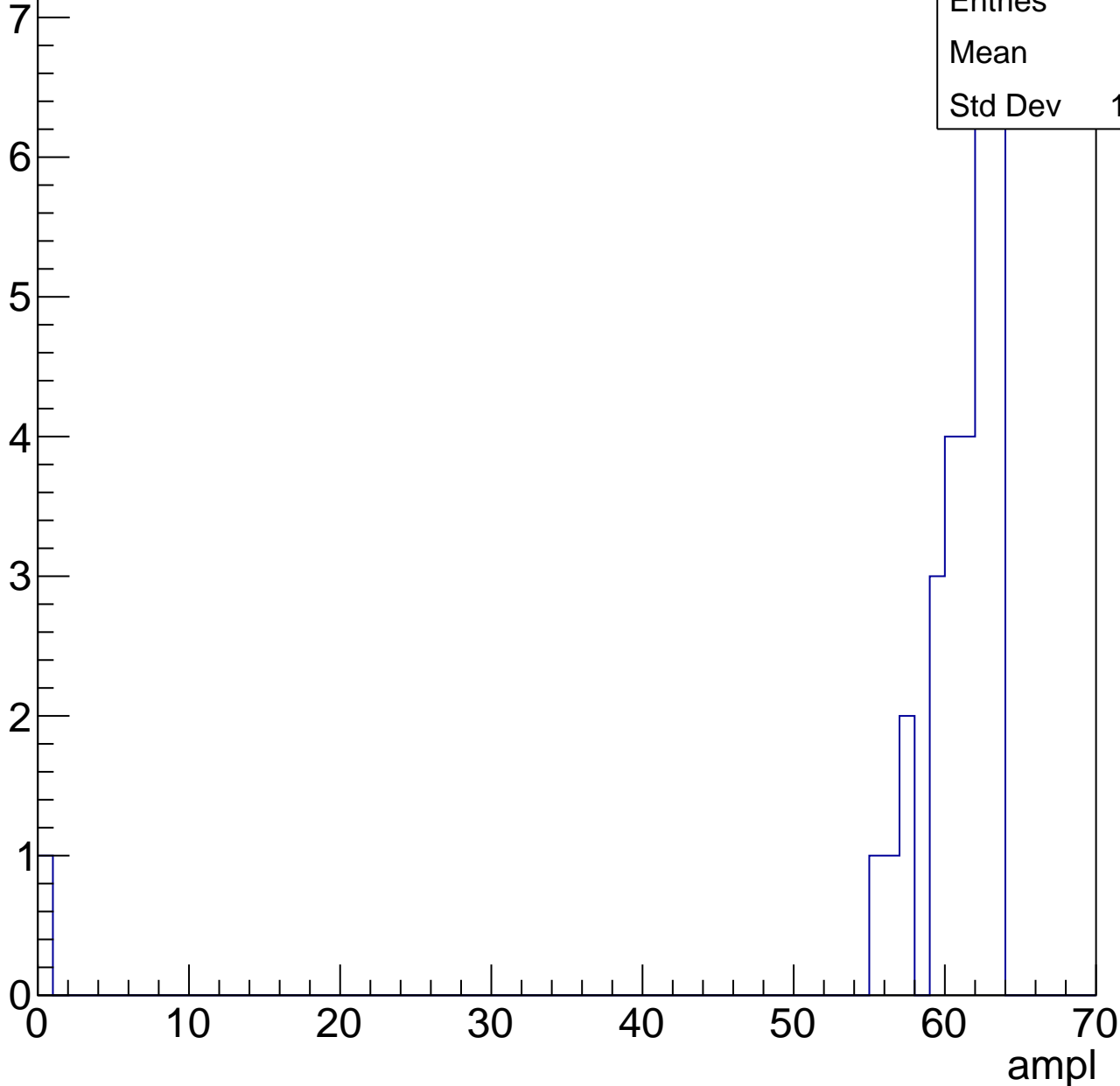


# B0L001S, U2-ch73, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

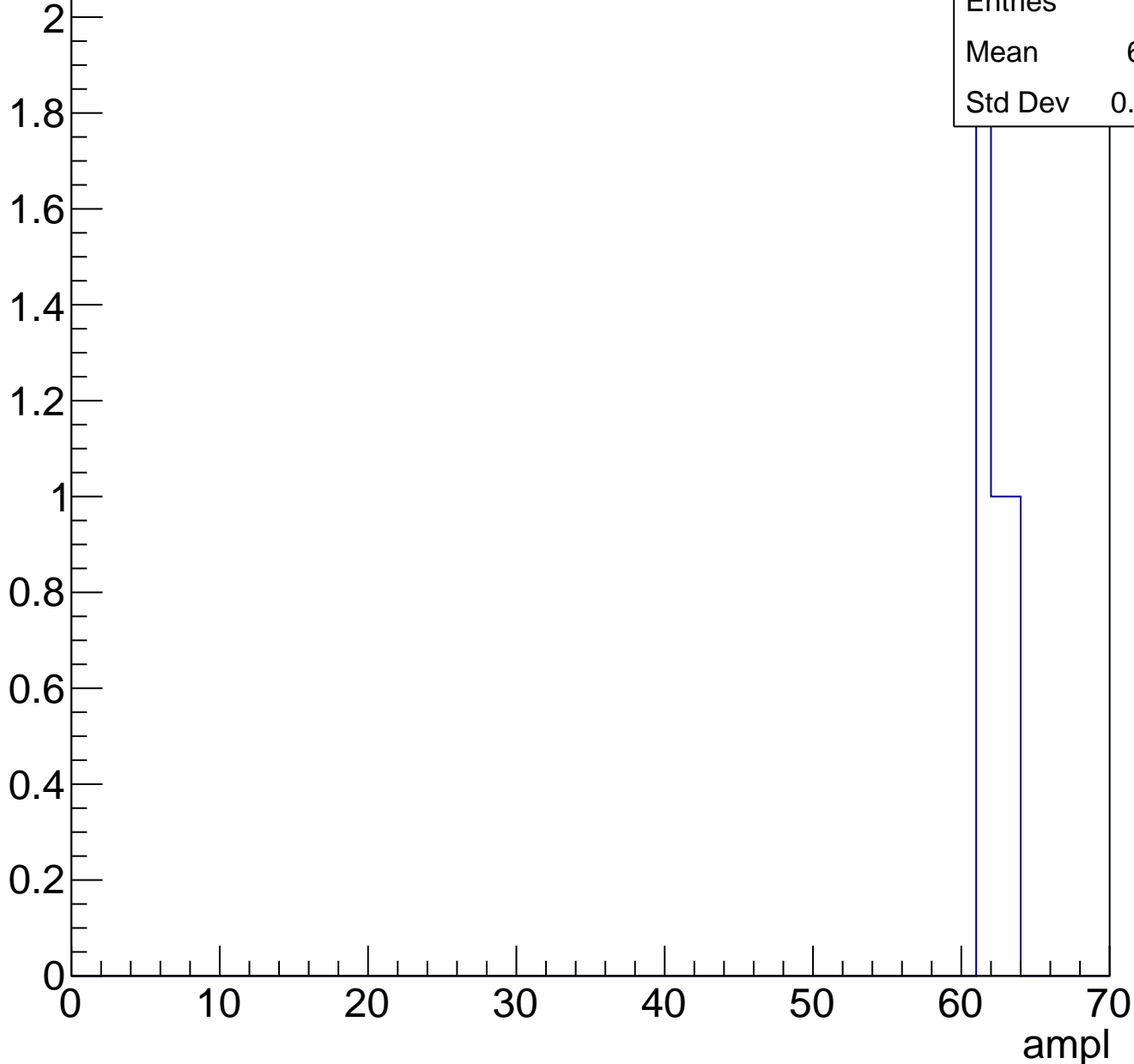
|         |       |
|---------|-------|
| Entries | 30    |
| Mean    | 58.7  |
| Std Dev | 11.12 |



# B0L001S, U2-ch73, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch73, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 0 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch74, adc0

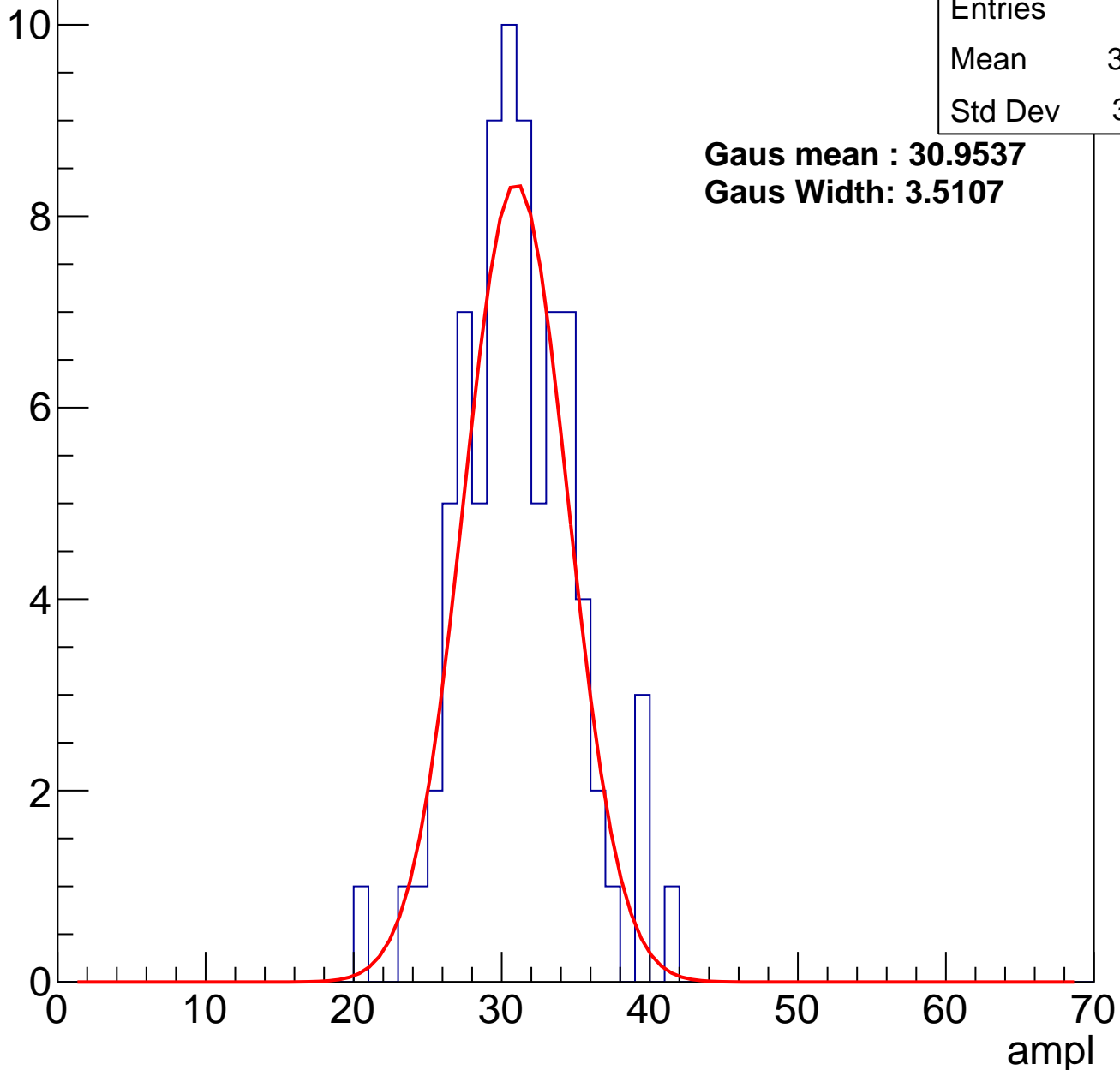
calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 80    |
| Mean    | 30.65 |
| Std Dev | 3.811 |

**Gaus mean : 30.9537**

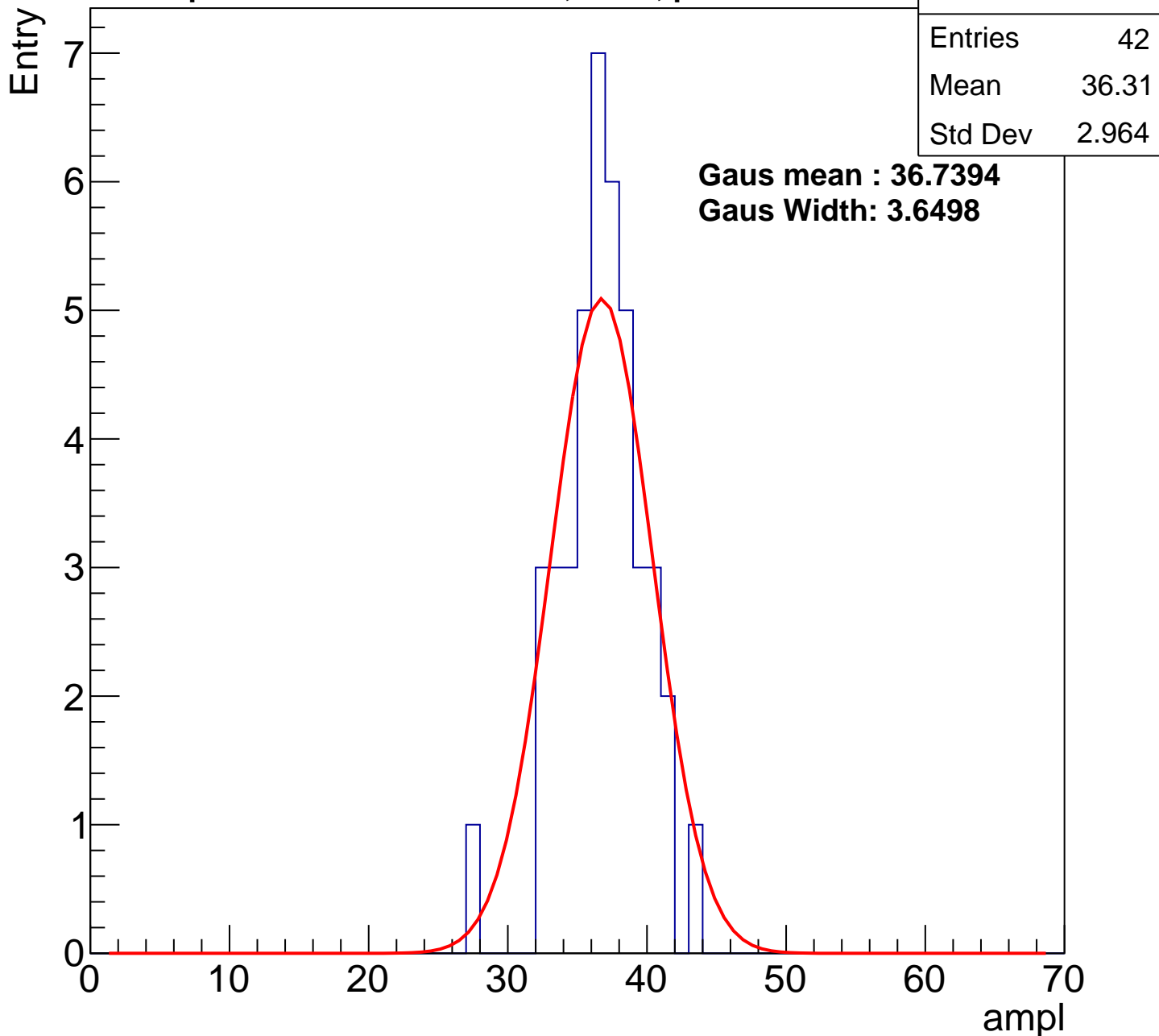
**Gaus Width: 3.5107**

Entry



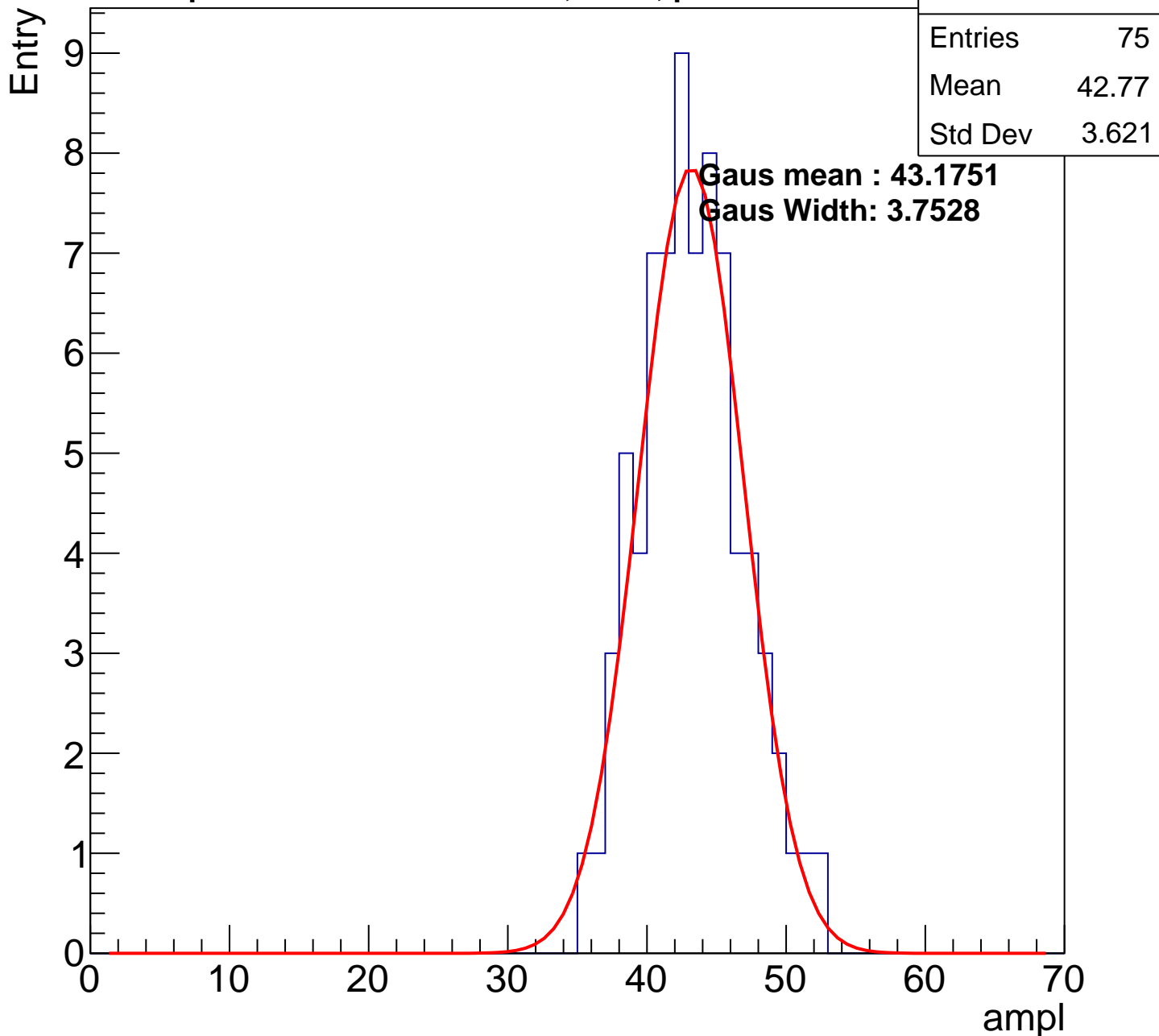
# B0L001S, U2-ch74, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U2-ch74, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

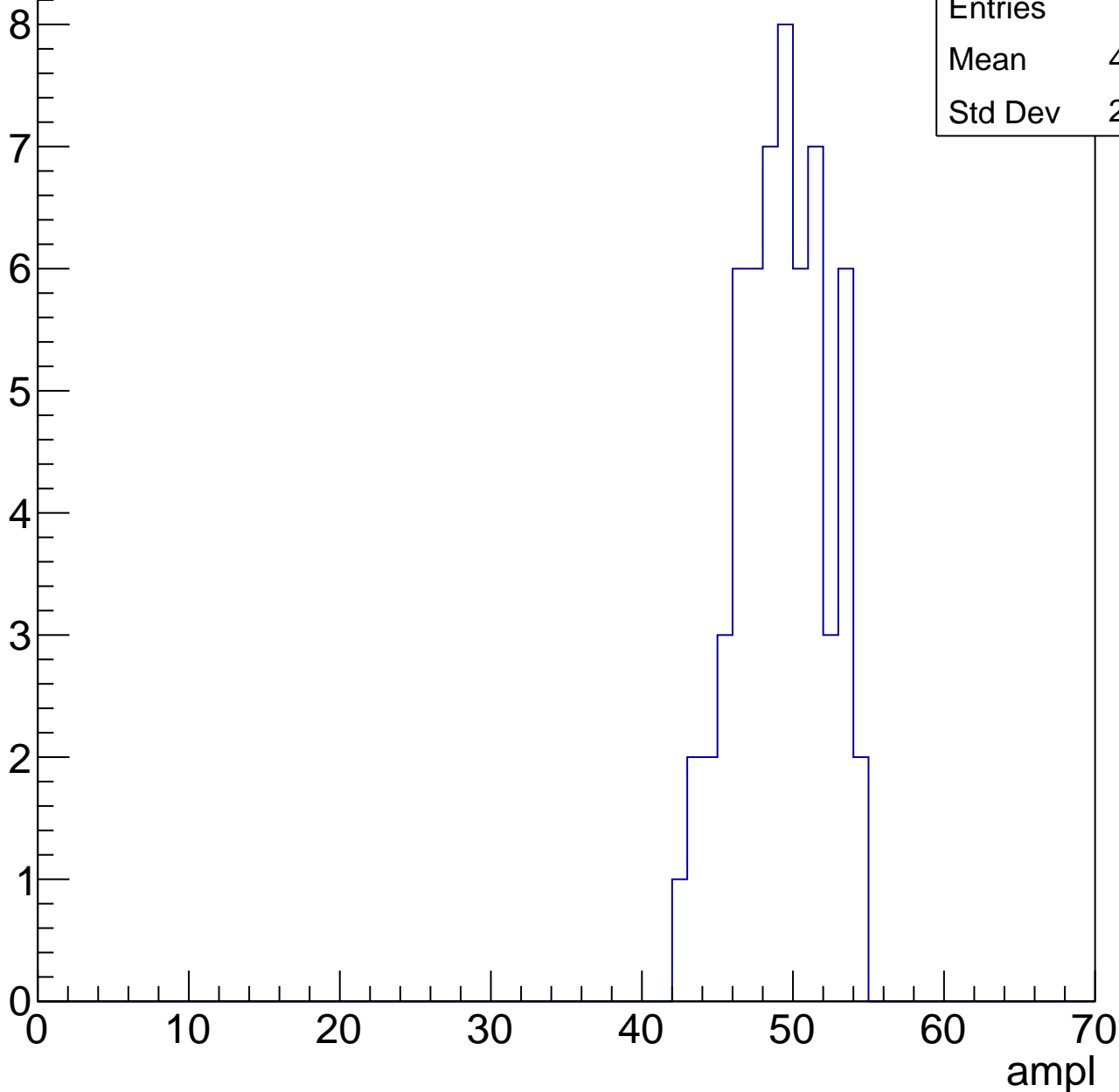


# B0L001S, U2-ch74, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

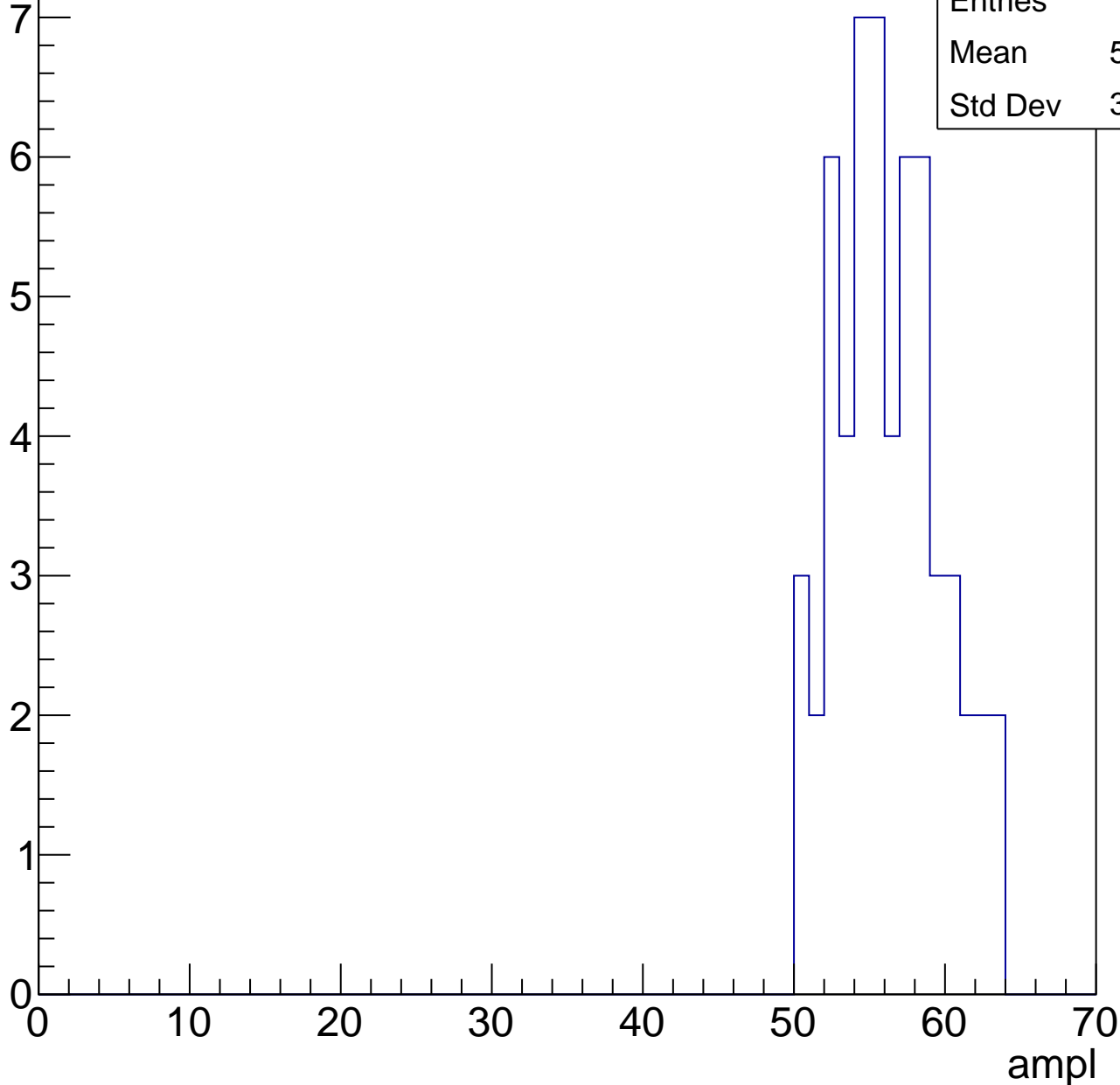
|         |       |
|---------|-------|
| Entries | 59    |
| Mean    | 48.75 |
| Std Dev | 2.932 |



# B0L001S, U2-ch74, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

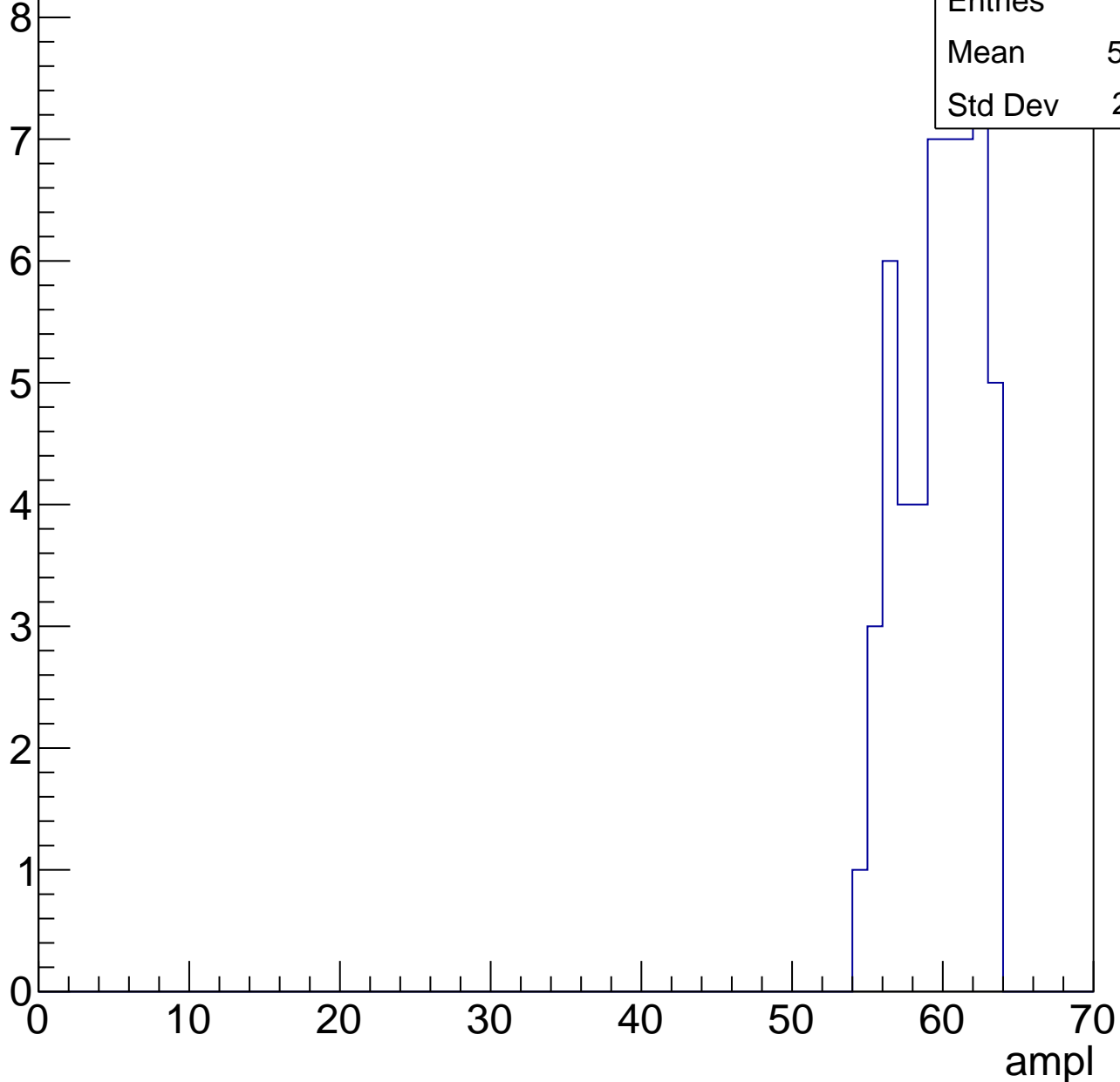


|         |       |
|---------|-------|
| Entries | 57    |
| Mean    | 55.82 |
| Std Dev | 3.372 |

# B0L001S, U2-ch74, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

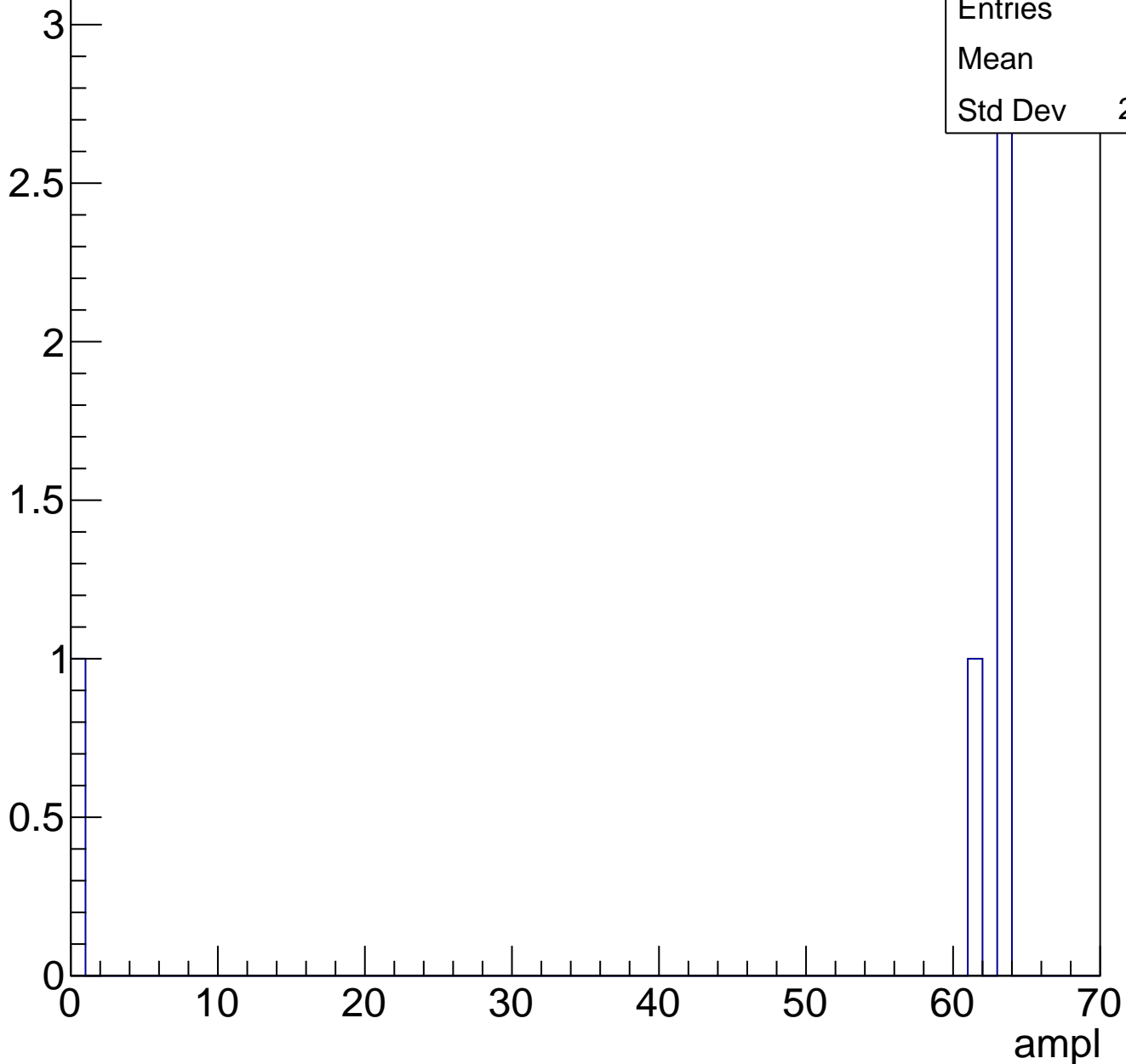
Entry



# B0L001S, U2-ch74, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch74, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U2-ch75, adc0

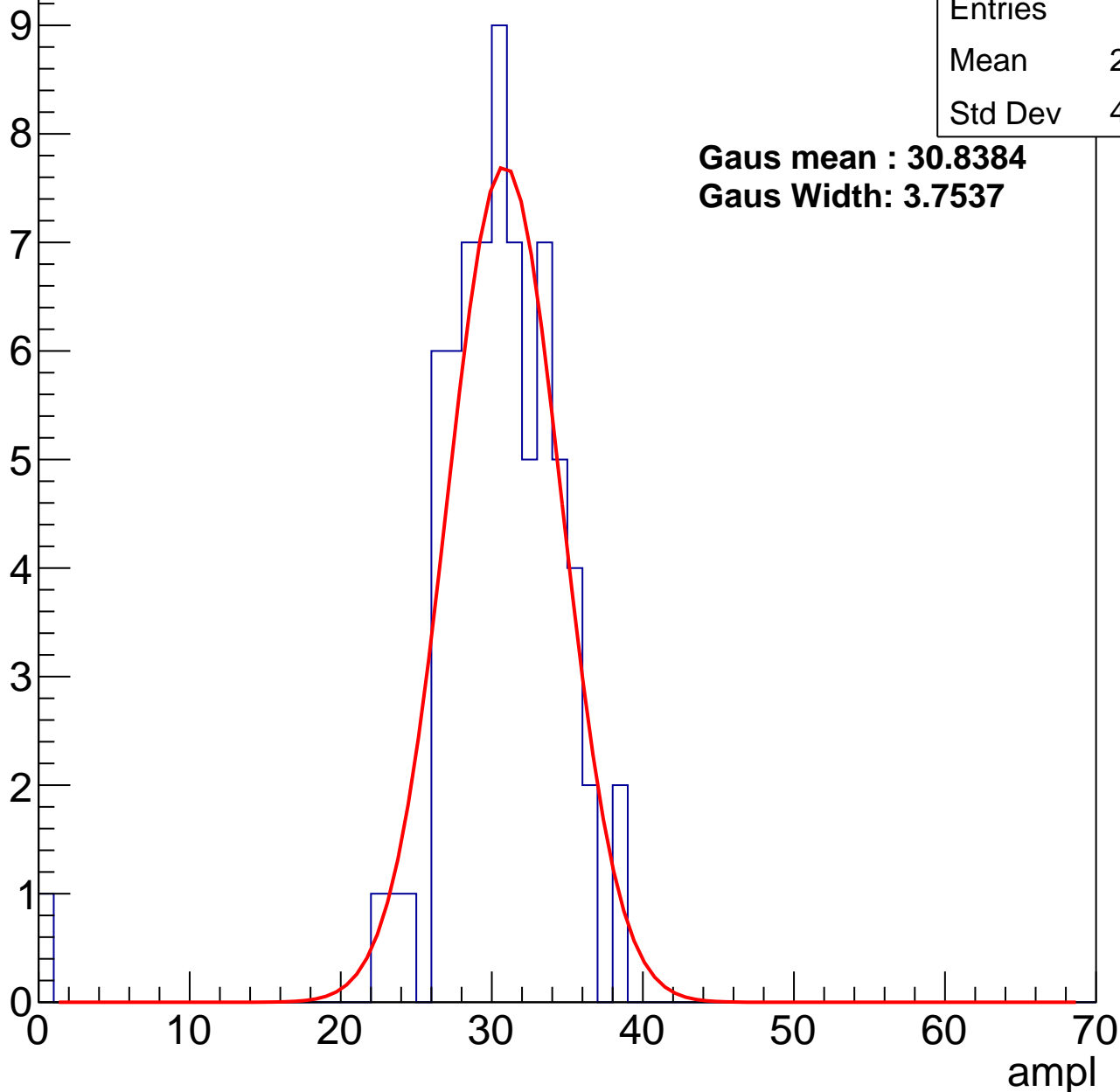
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 71    |
| Mean    | 29.89 |
| Std Dev | 4.898 |

**Gaus mean : 30.8384**

**Gaus Width: 3.7537**



# B0L001S, U2-ch75, adc1

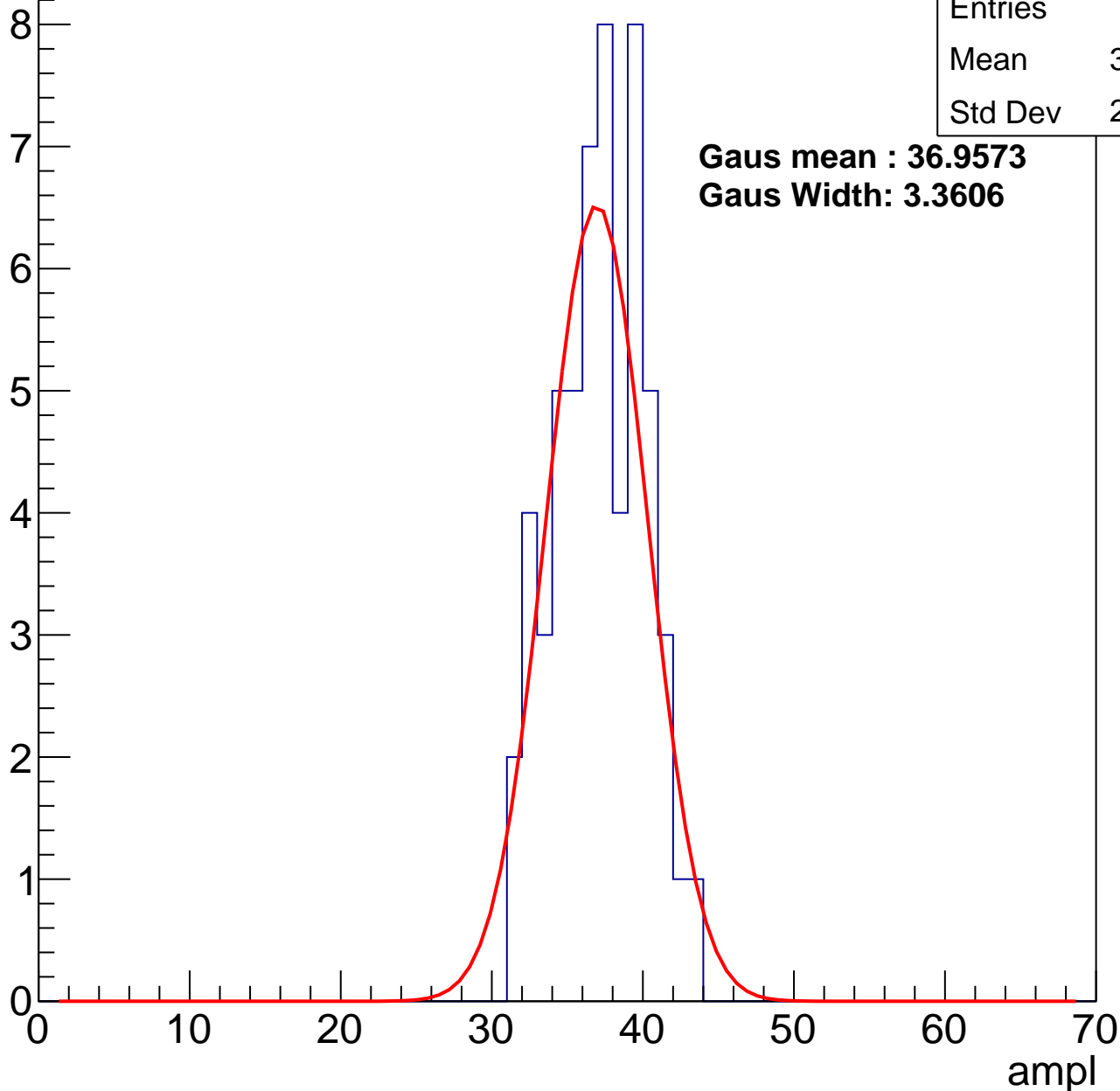
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 56    |
| Mean    | 36.68 |
| Std Dev | 2.916 |

**Gaus mean : 36.9573**

**Gaus Width: 3.3606**



# B0L001S, U2-ch75, adc2

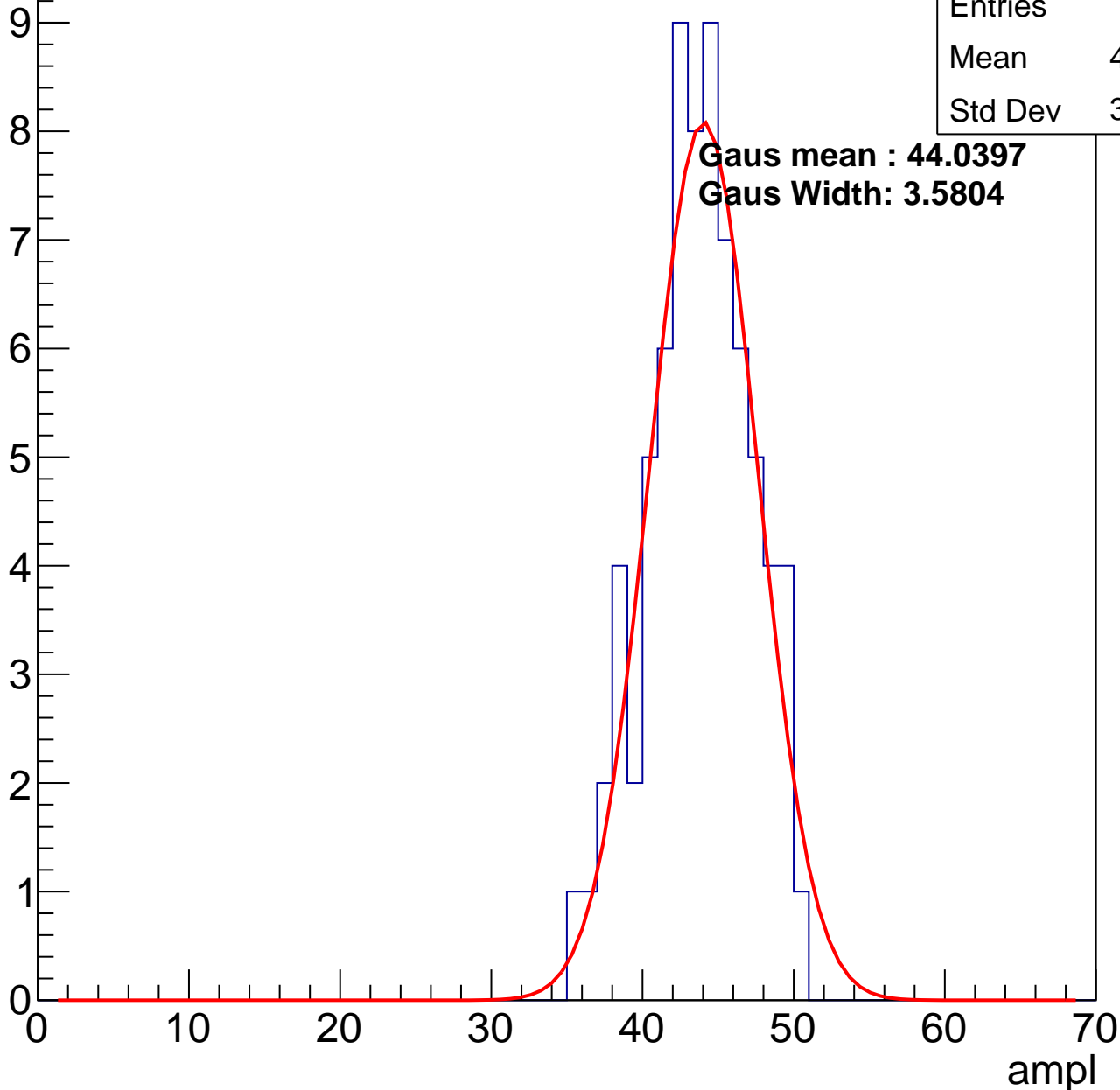
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 74    |
| Mean    | 43.28 |
| Std Dev | 3.395 |

**Gaus mean : 44.0397**

**Gaus Width: 3.5804**

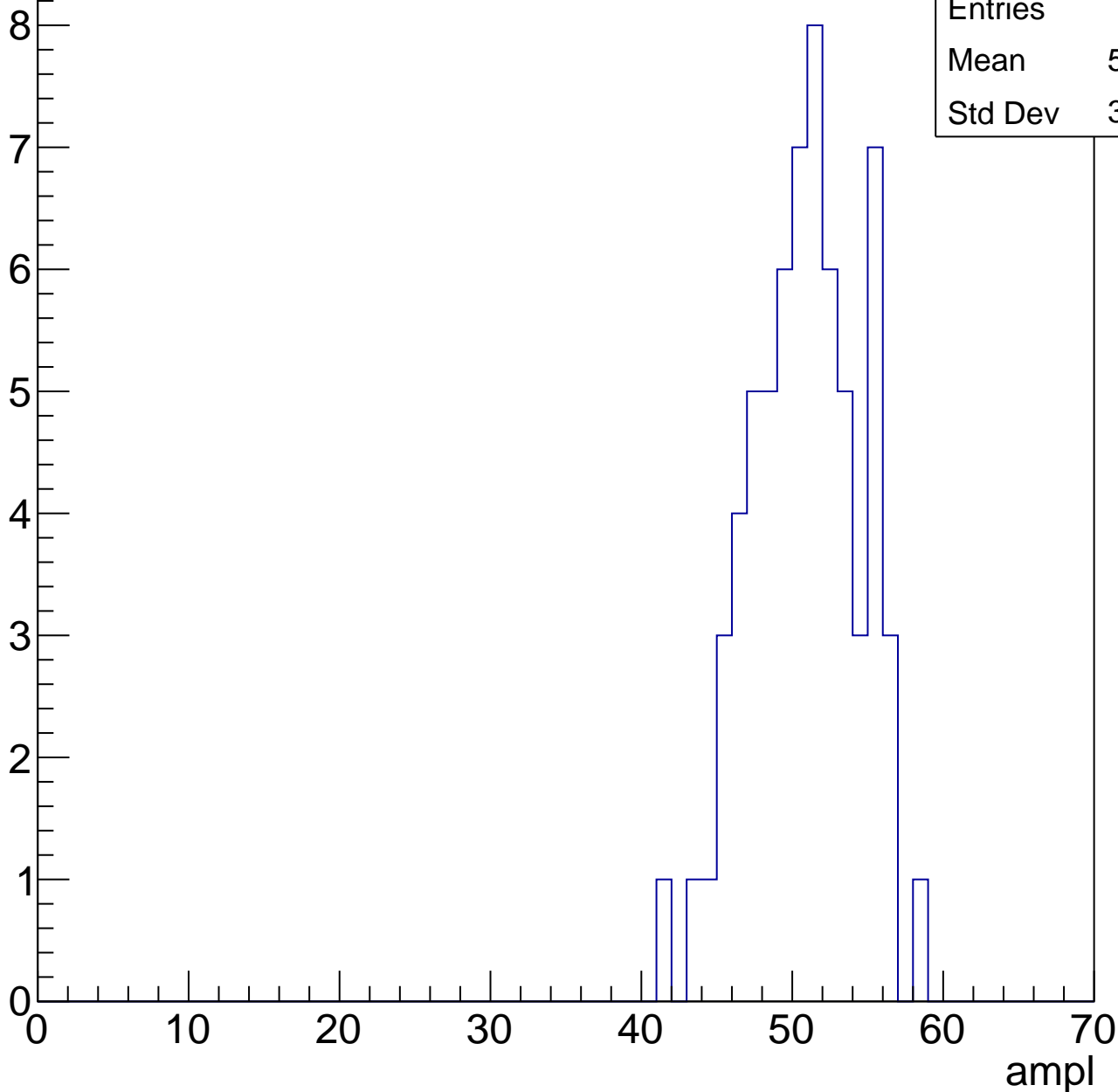


# B0L001S, U2-ch75, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 66    |
| Mean    | 50.36 |
| Std Dev | 3.566 |



# B0L001S, U2-ch75, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

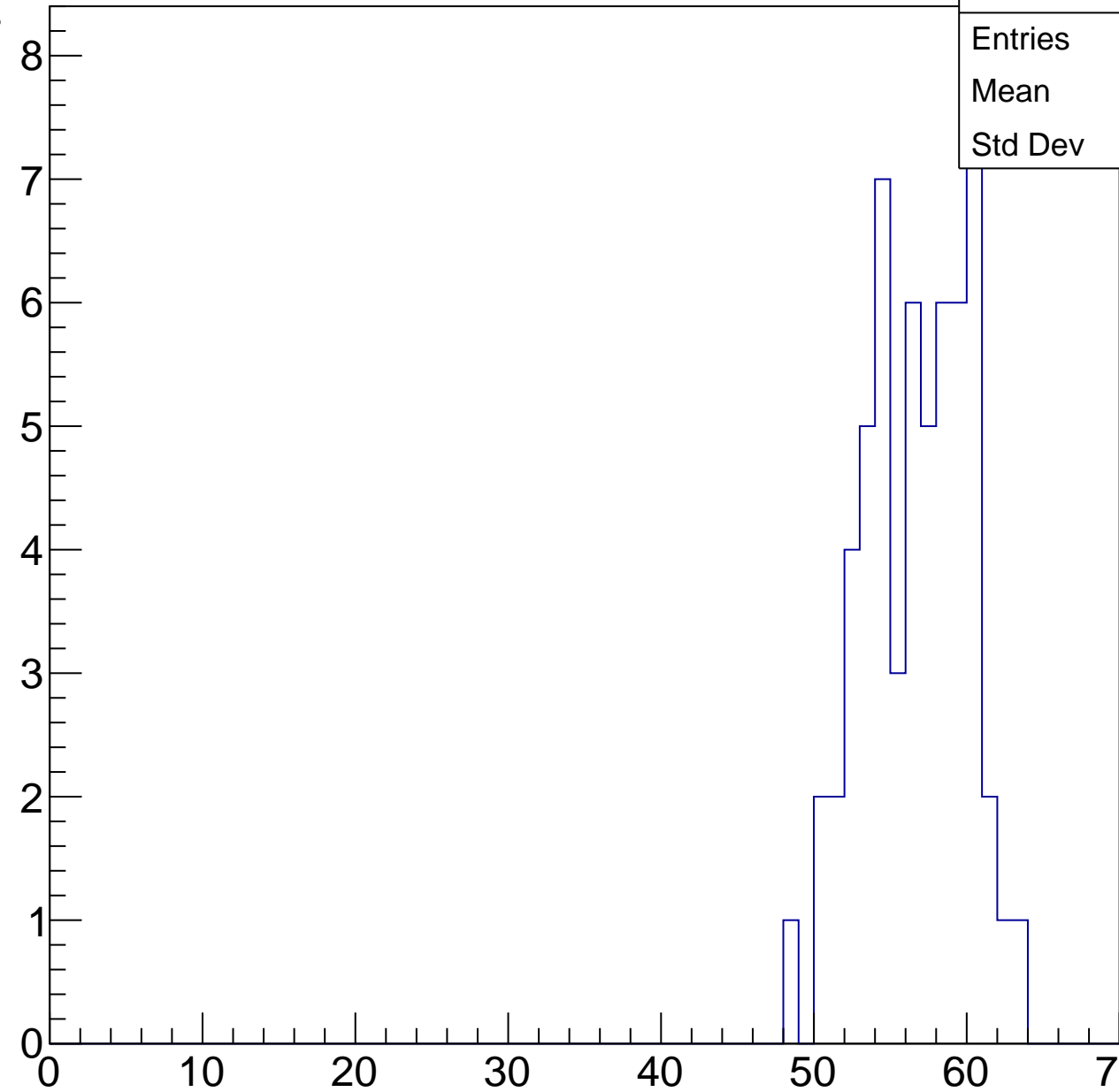
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

|         |       |
|---------|-------|
| Entries | 59    |
| Mean    | 56.2  |
| Std Dev | 3.369 |

ampl

0 10 20 30 40 50 60 70

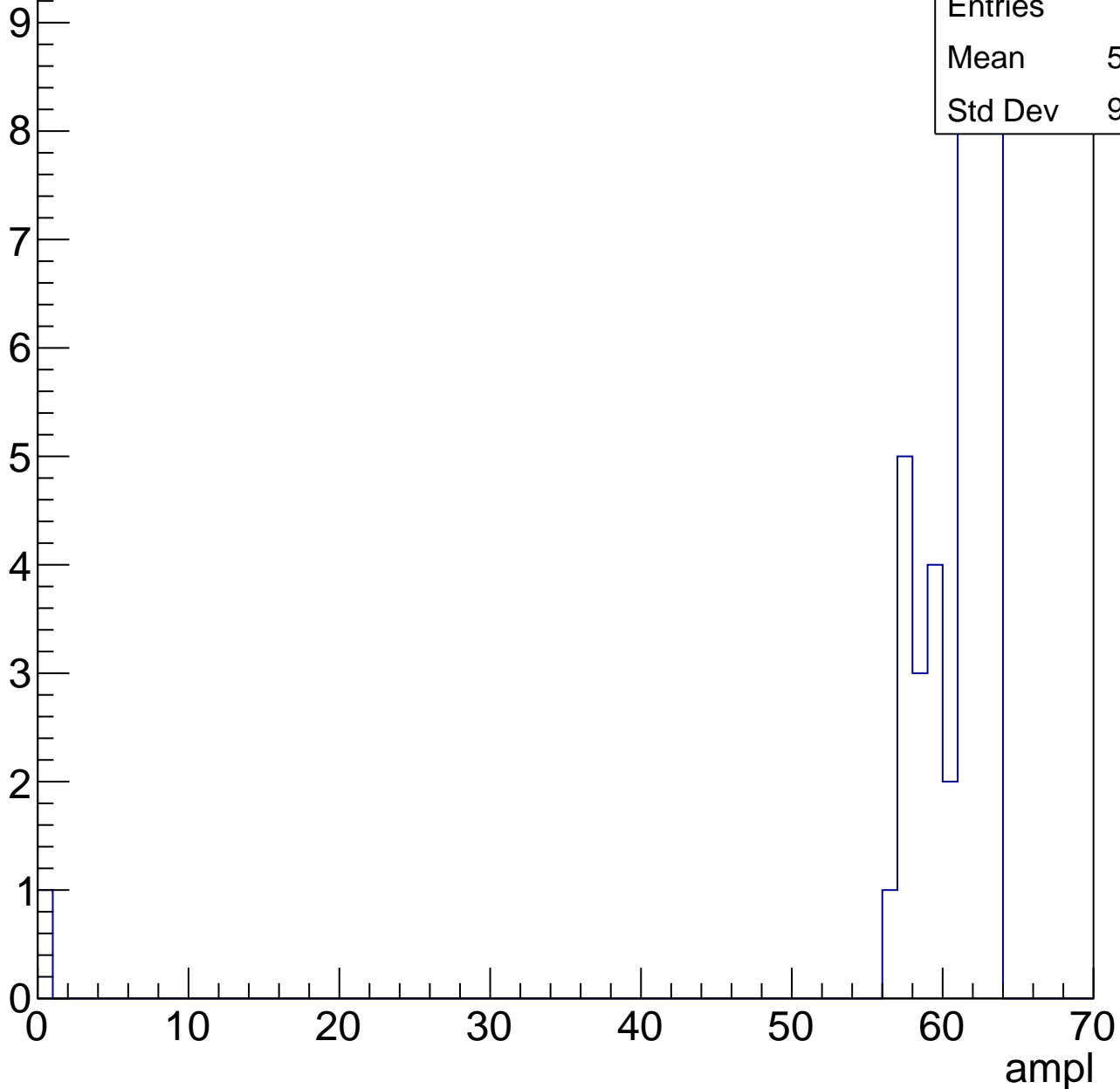


# B0L001S, U2-ch75, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 42    |
| Mean    | 59.14 |
| Std Dev | 9.476 |



# B0L001S, U2-ch75, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 0 |
| Mean    | 0 |
| Std Dev | 0 |



# B0L001S, U2-ch75, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U2-ch76, adc0

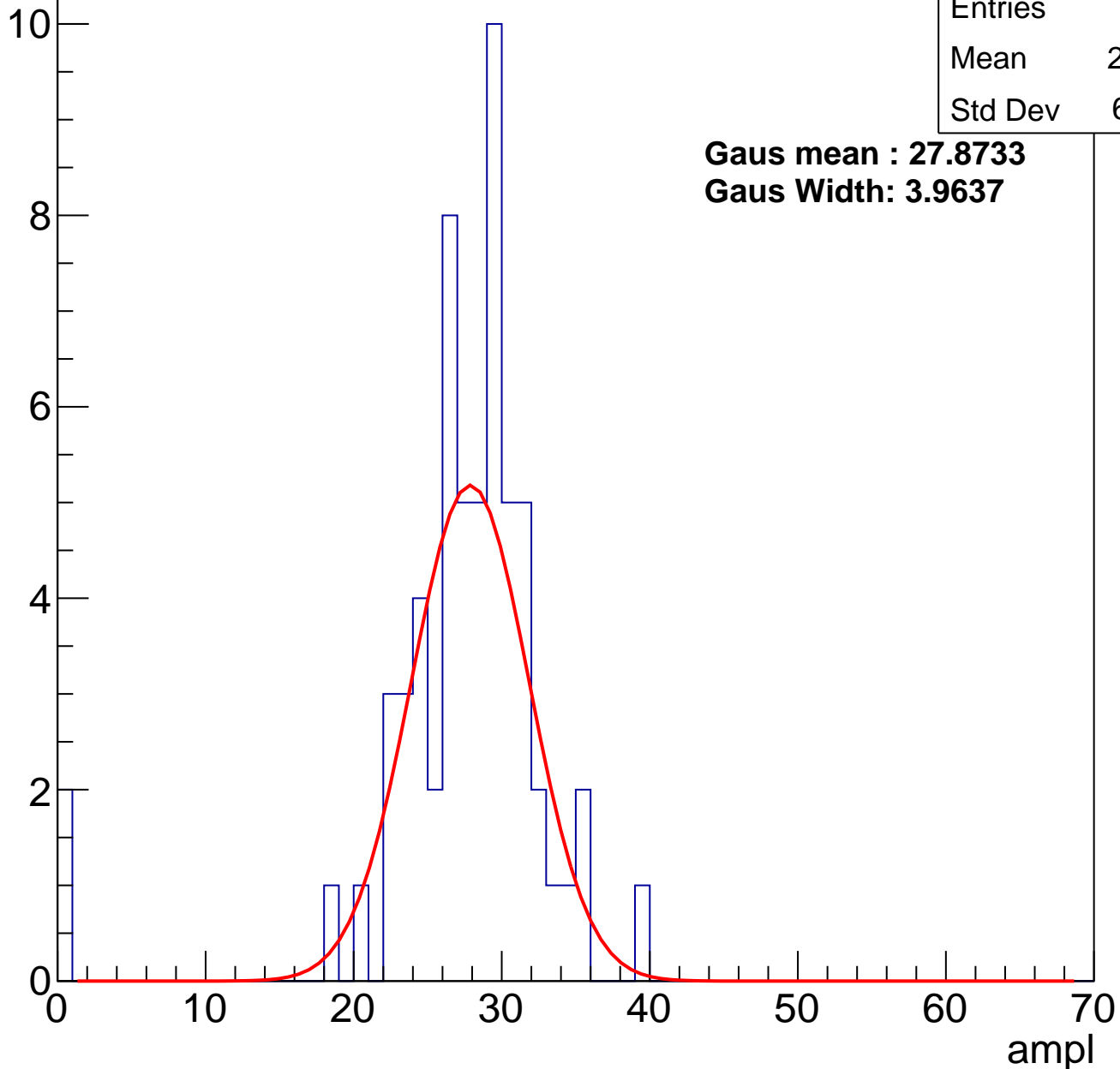
calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 61    |
| Mean    | 26.84 |
| Std Dev | 6.191 |

**Gaus mean : 27.8733**

**Gaus Width: 3.9637**

Entry



# B0L001S, U2-ch76, adc1

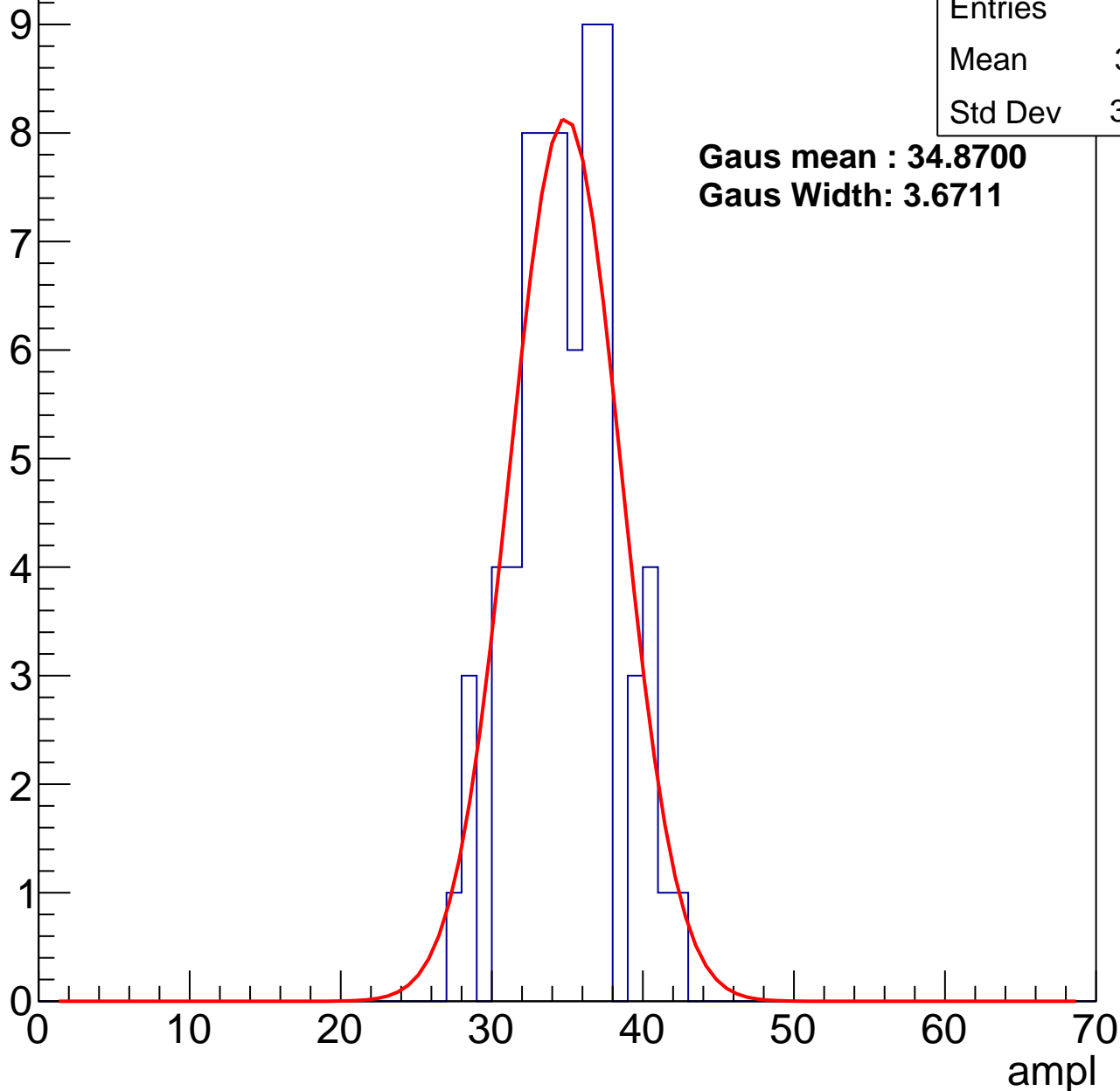
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 69    |
| Mean    | 34.41 |
| Std Dev | 3.276 |

**Gaus mean : 34.8700**

**Gaus Width: 3.6711**



# B0L001S, U2-ch76, adc2

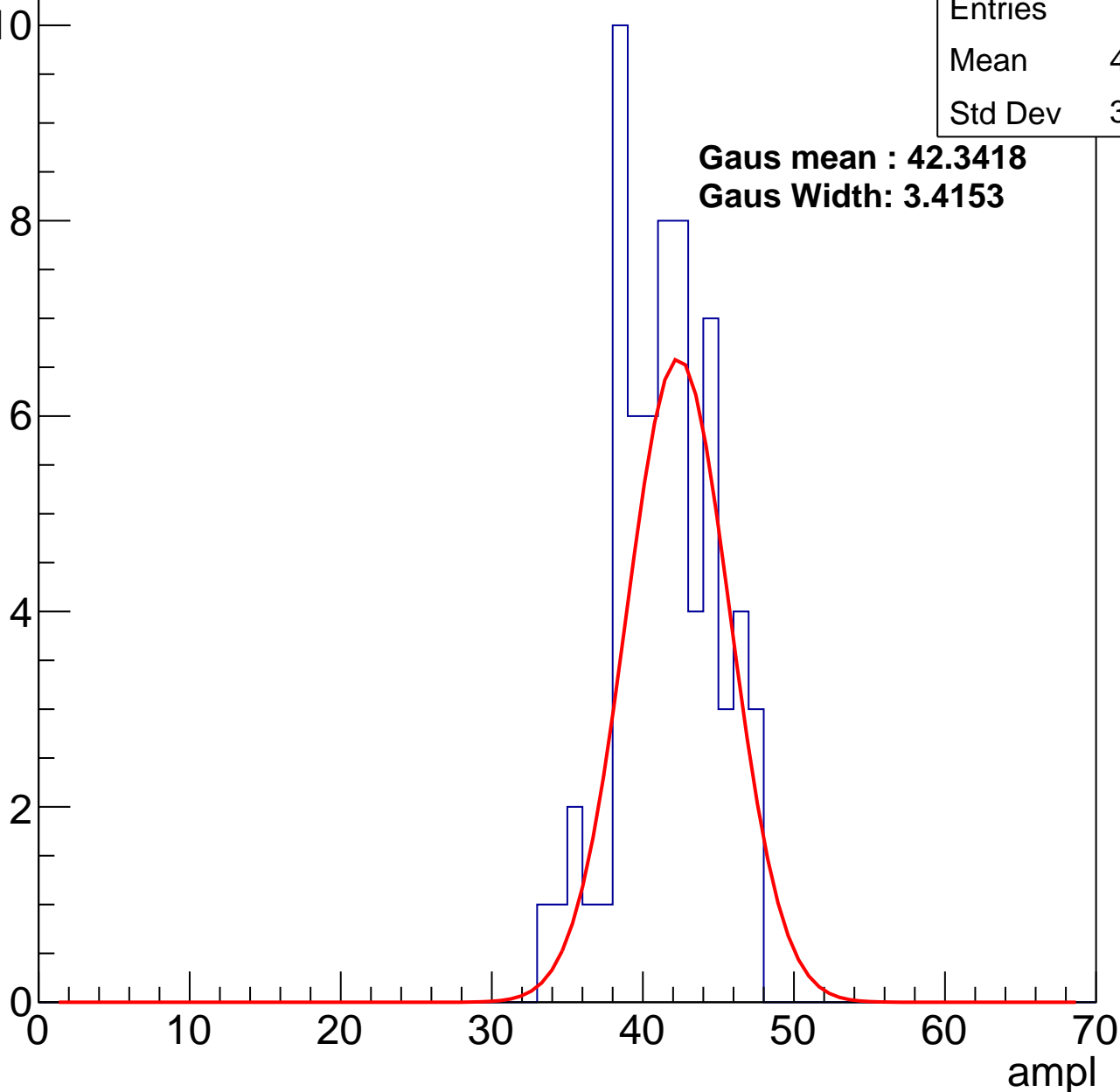
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 65    |
| Mean    | 41.05 |
| Std Dev | 3.255 |

**Gaus mean : 42.3418**

**Gaus Width: 3.4153**



# B0L001S, U2-ch76, adc3

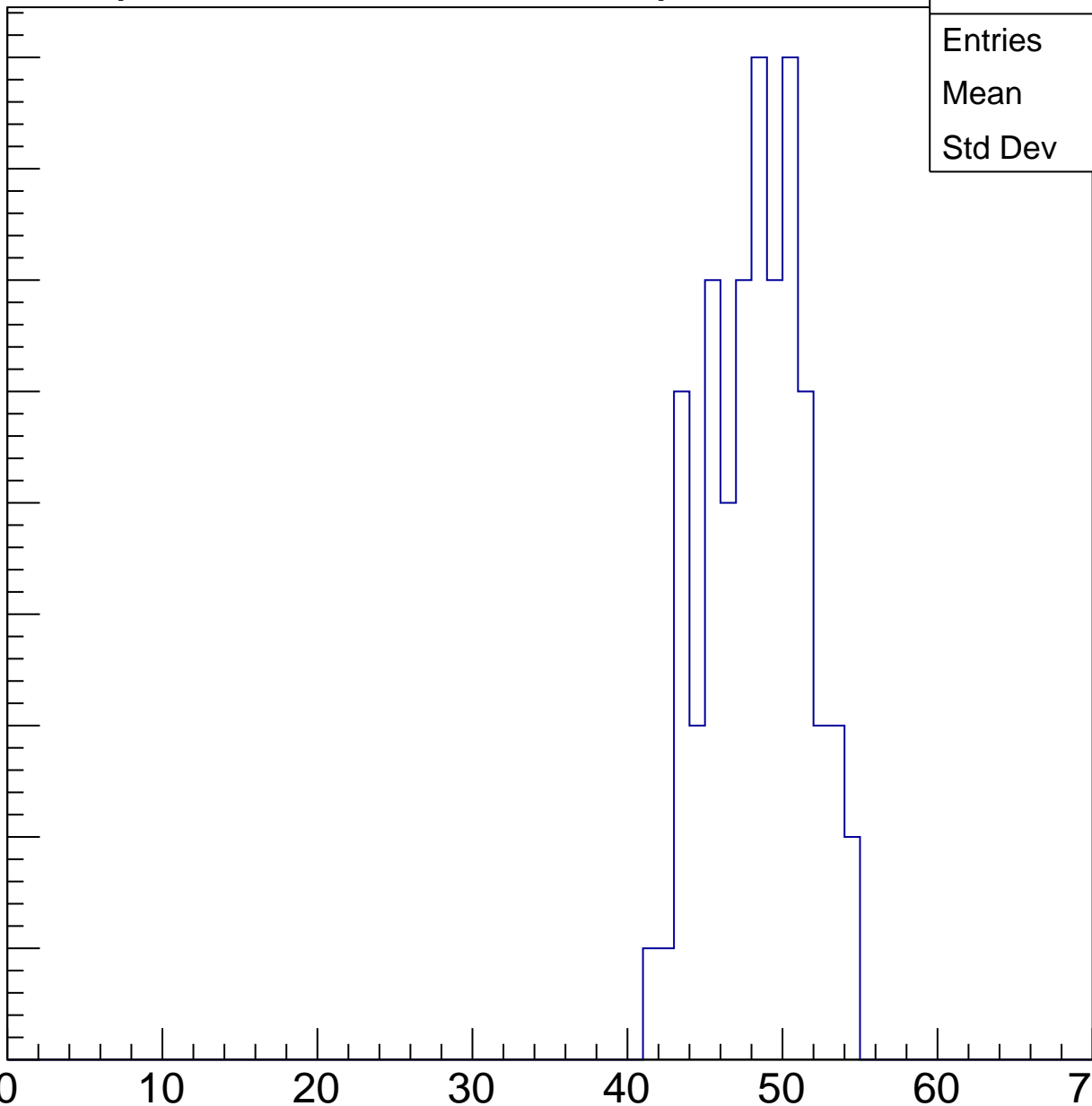
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

|         |       |
|---------|-------|
| Entries | 69    |
| Mean    | 47.84 |
| Std Dev | 3.1   |

ampl

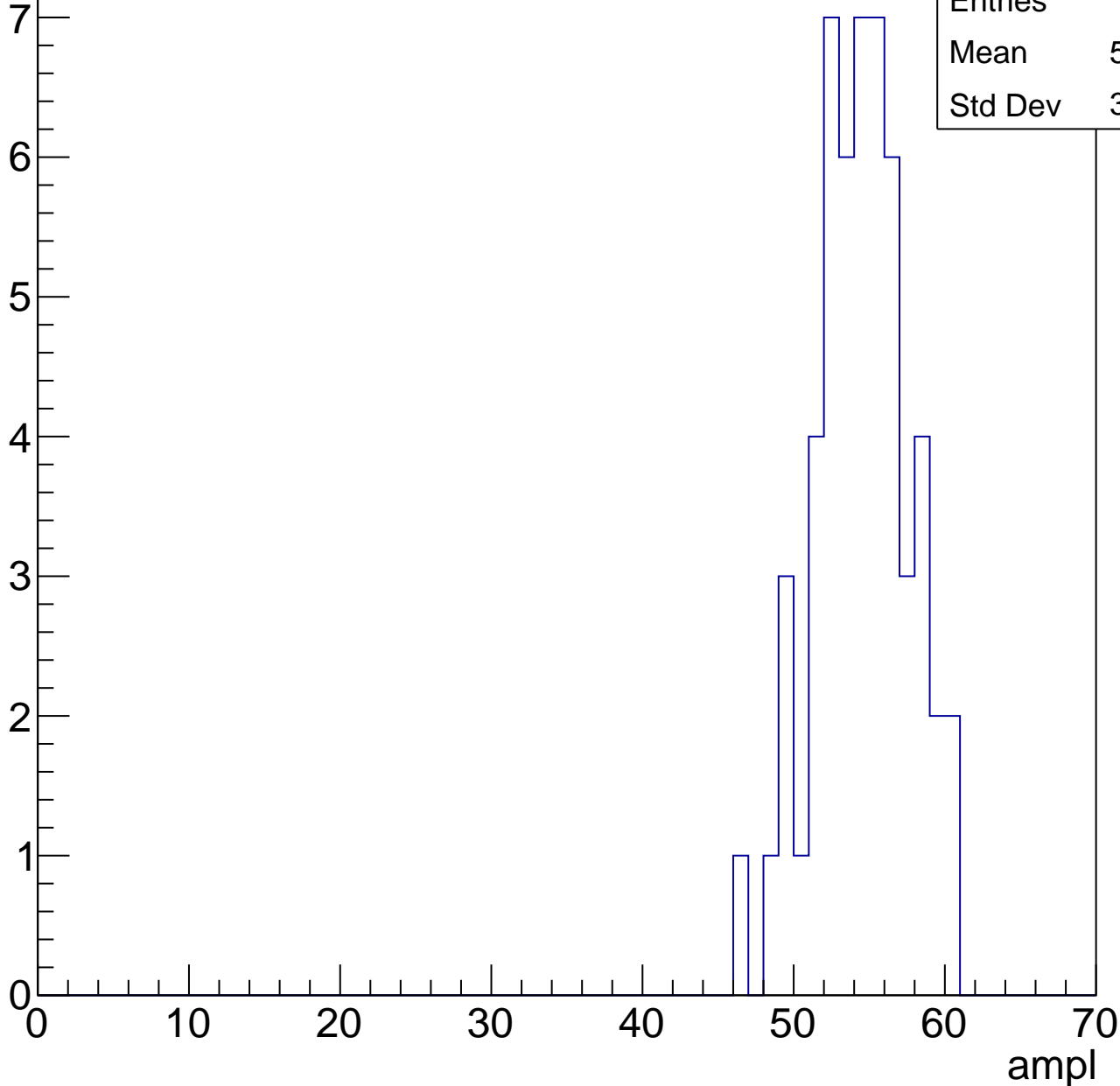


# B0L001S, U2-ch76, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

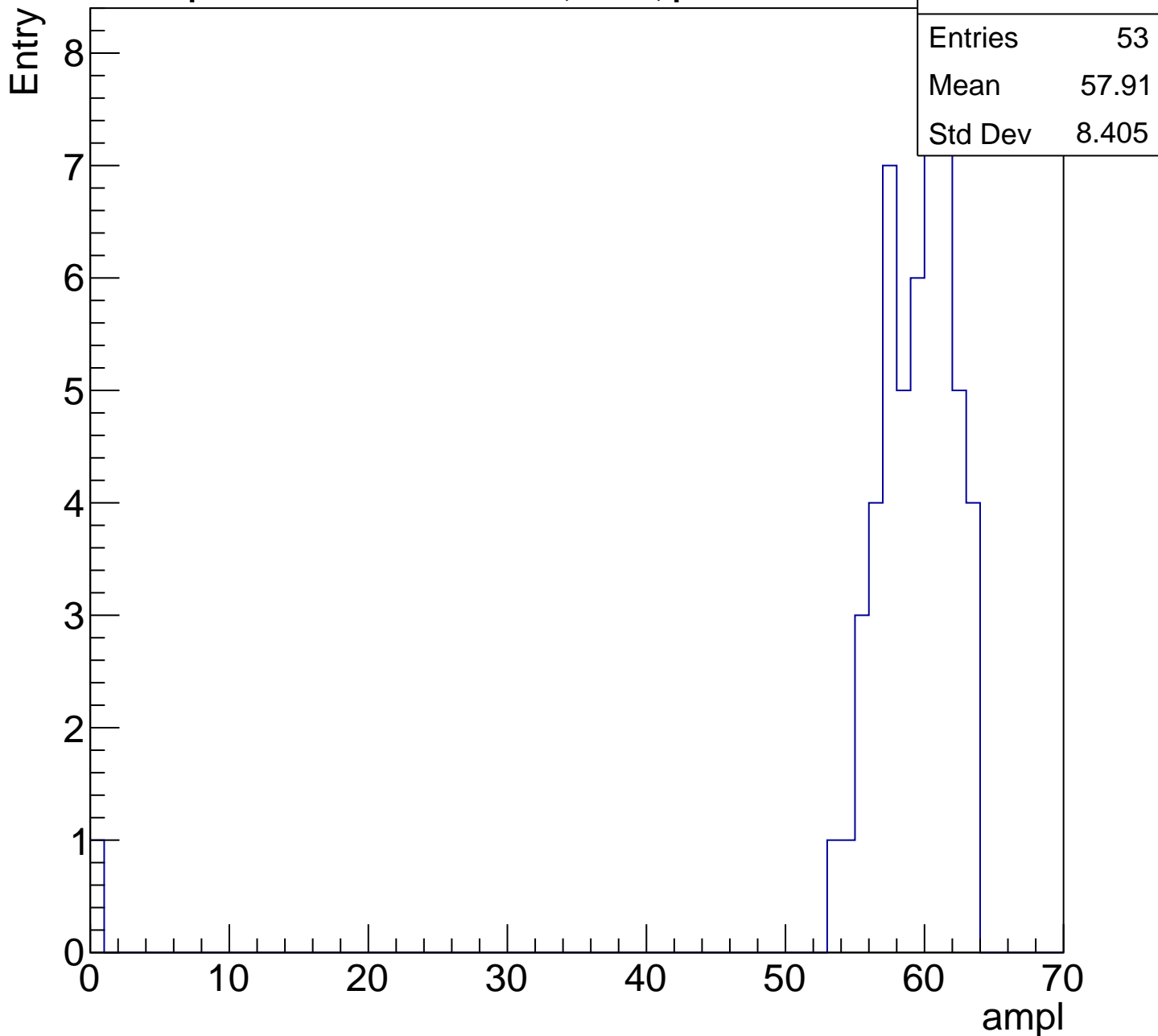
Entry

|         |       |
|---------|-------|
| Entries | 54    |
| Mean    | 54.02 |
| Std Dev | 3.058 |



# B0L001S, U2-ch76, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

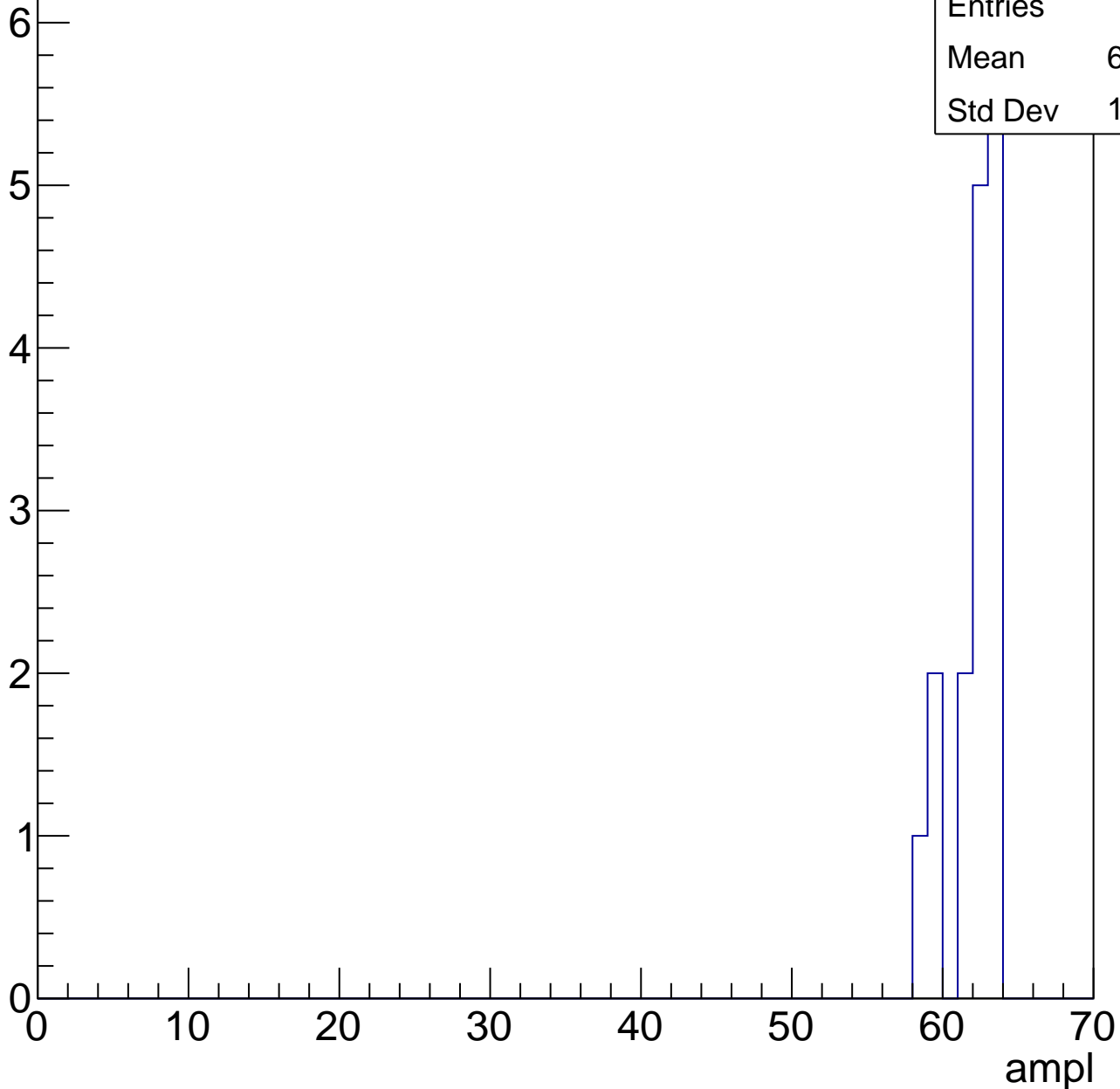


# B0L001S, U2-ch76, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 16    |
| Mean    | 61.62 |
| Std Dev | 1.576 |





# B0L001S, U2-ch76, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U2-ch77, adc0

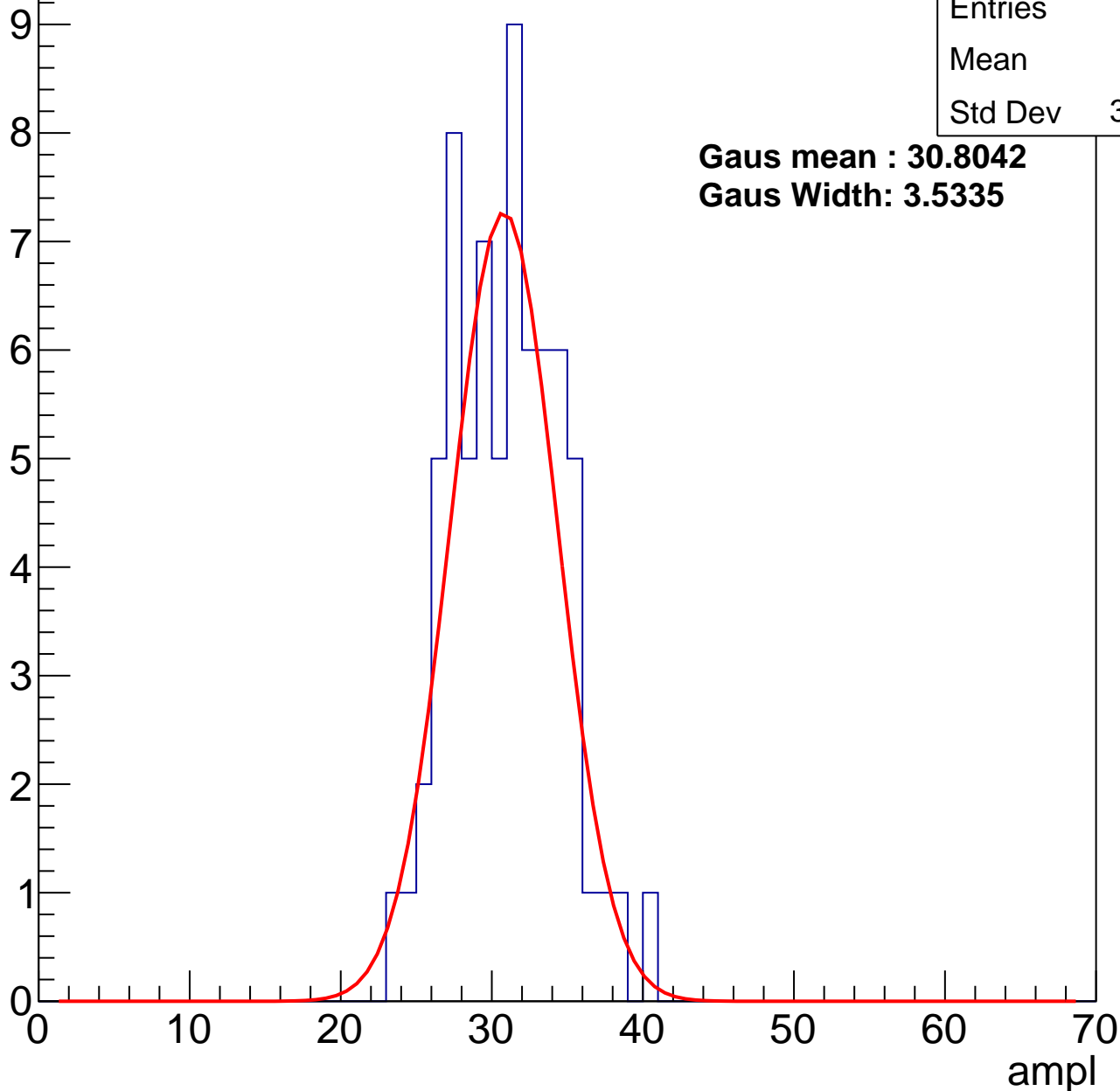
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 70    |
| Mean    | 30.5  |
| Std Dev | 3.492 |

**Gaus mean : 30.8042**

**Gaus Width: 3.5335**



# B0L001S, U2-ch77, adc1

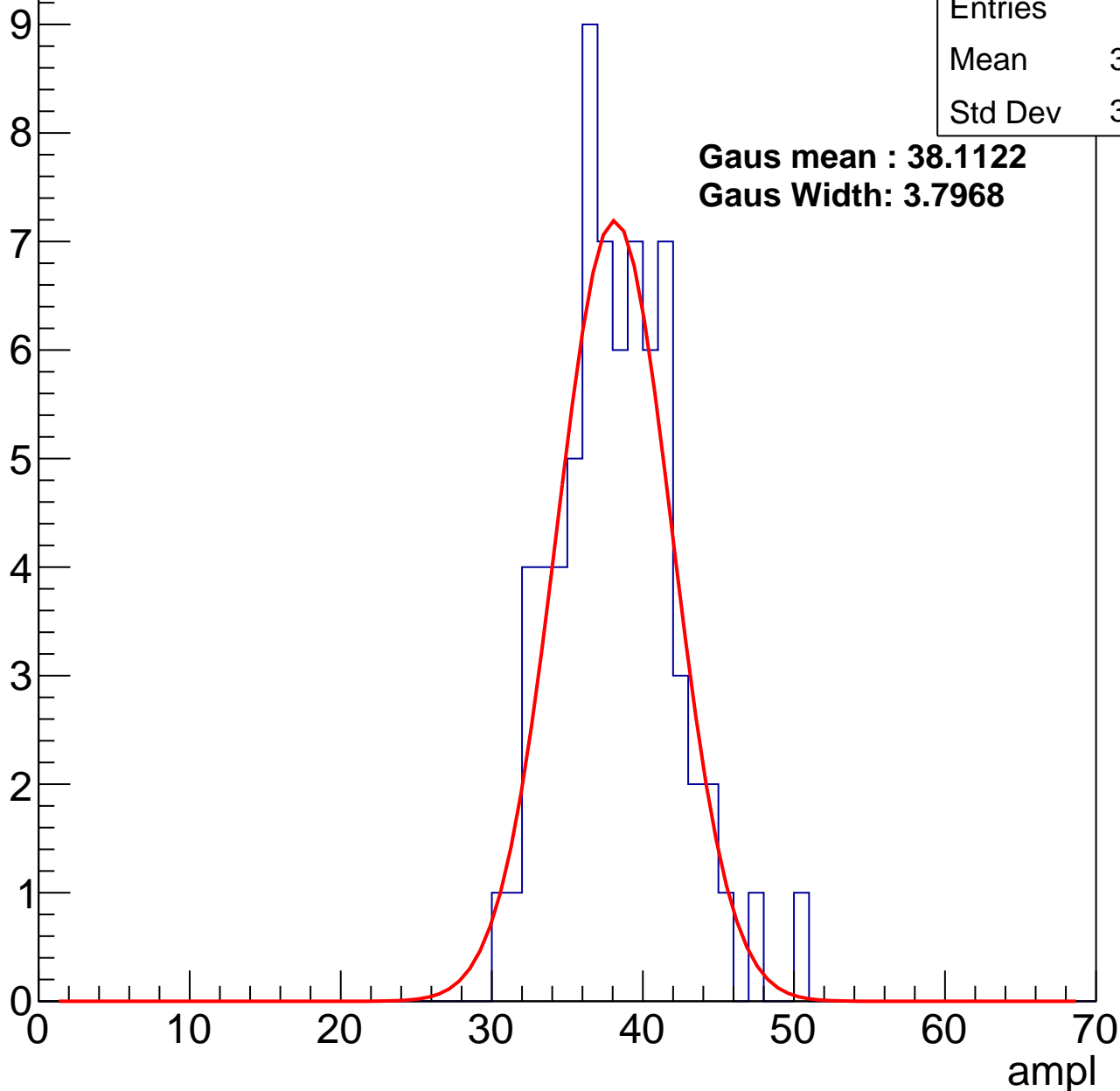
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 71    |
| Mean    | 37.82 |
| Std Dev | 3.836 |

**Gaus mean : 38.1122**

**Gaus Width: 3.7968**



# B0L001S, U2-ch77, adc2

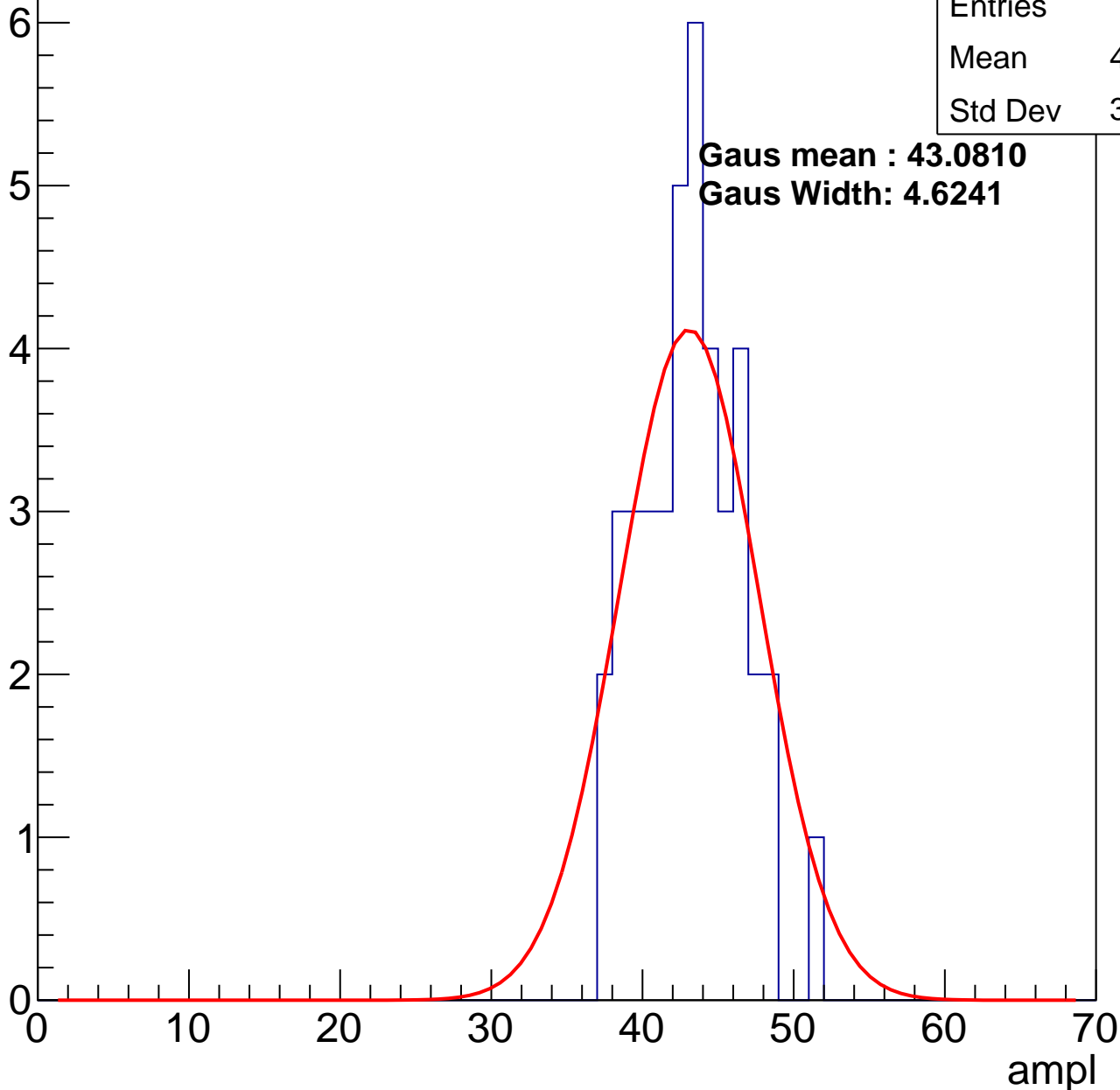
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 41    |
| Mean    | 42.73 |
| Std Dev | 3.254 |

**Gaus mean : 43.0810**

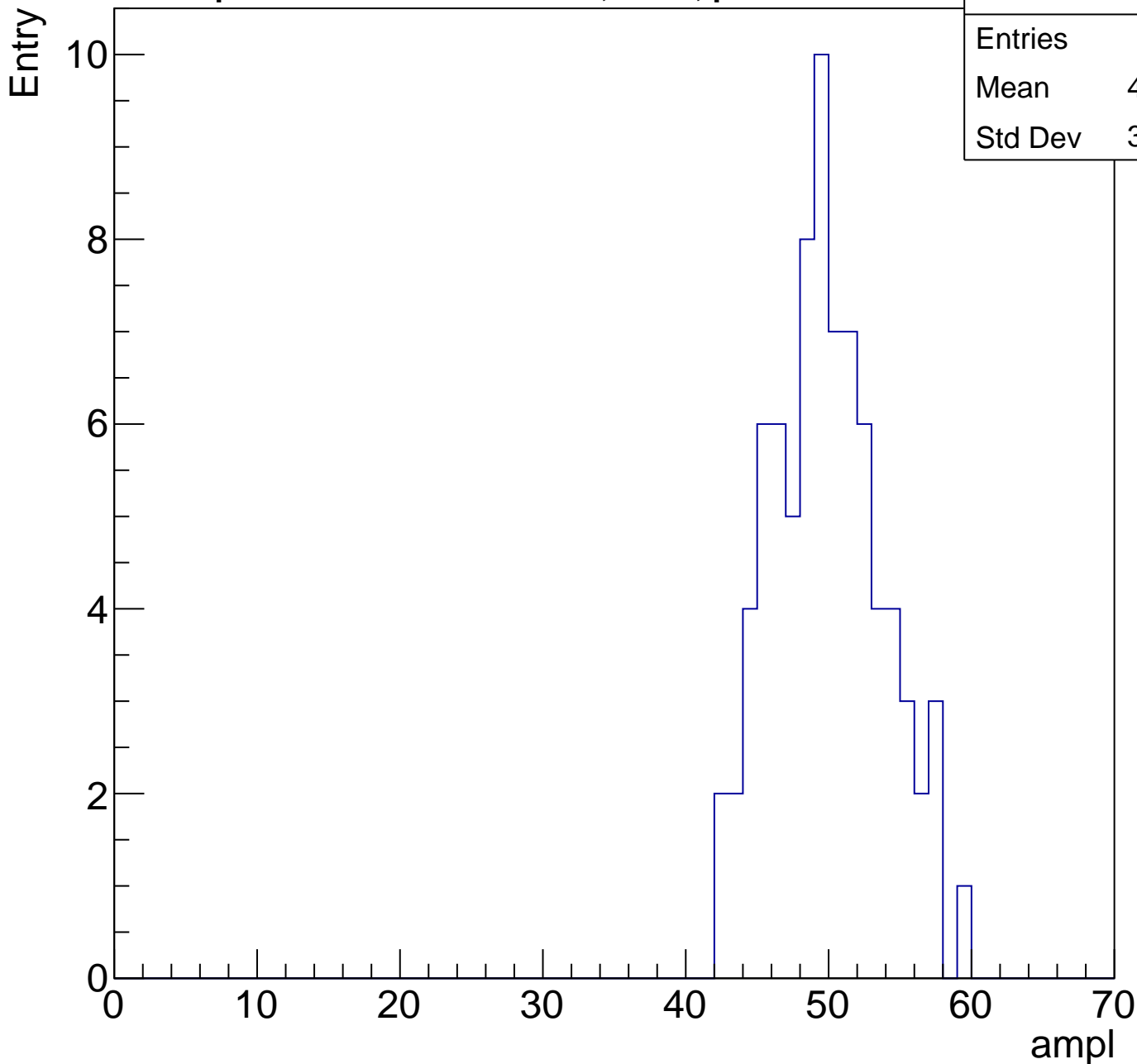
**Gaus Width: 4.6241**



# B0L001S, U2-ch77, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 80    |
| Mean    | 49.44 |
| Std Dev | 3.847 |

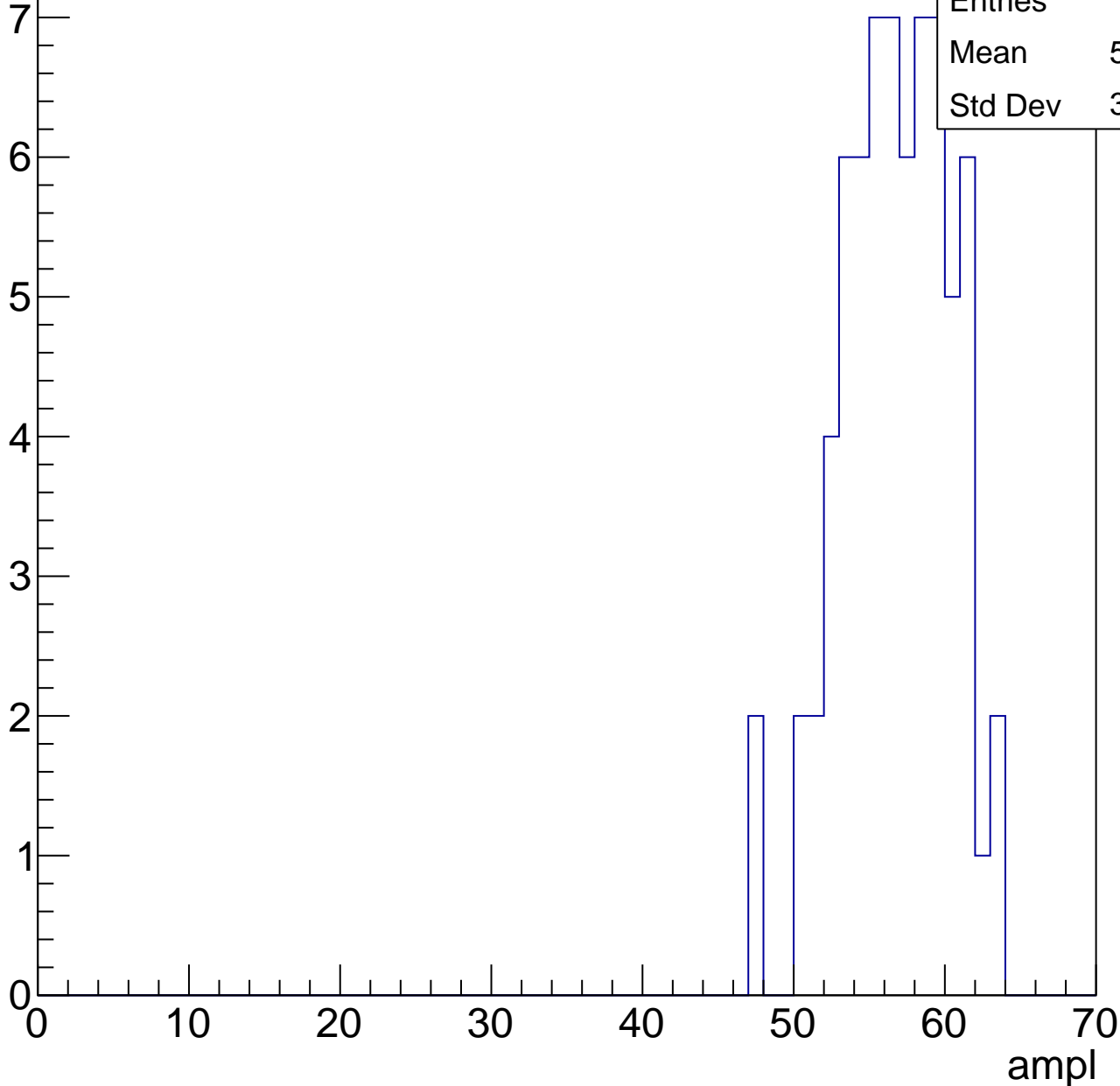


# B0L001S, U2-ch77, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 70    |
| Mean    | 56.26 |
| Std Dev | 3.564 |

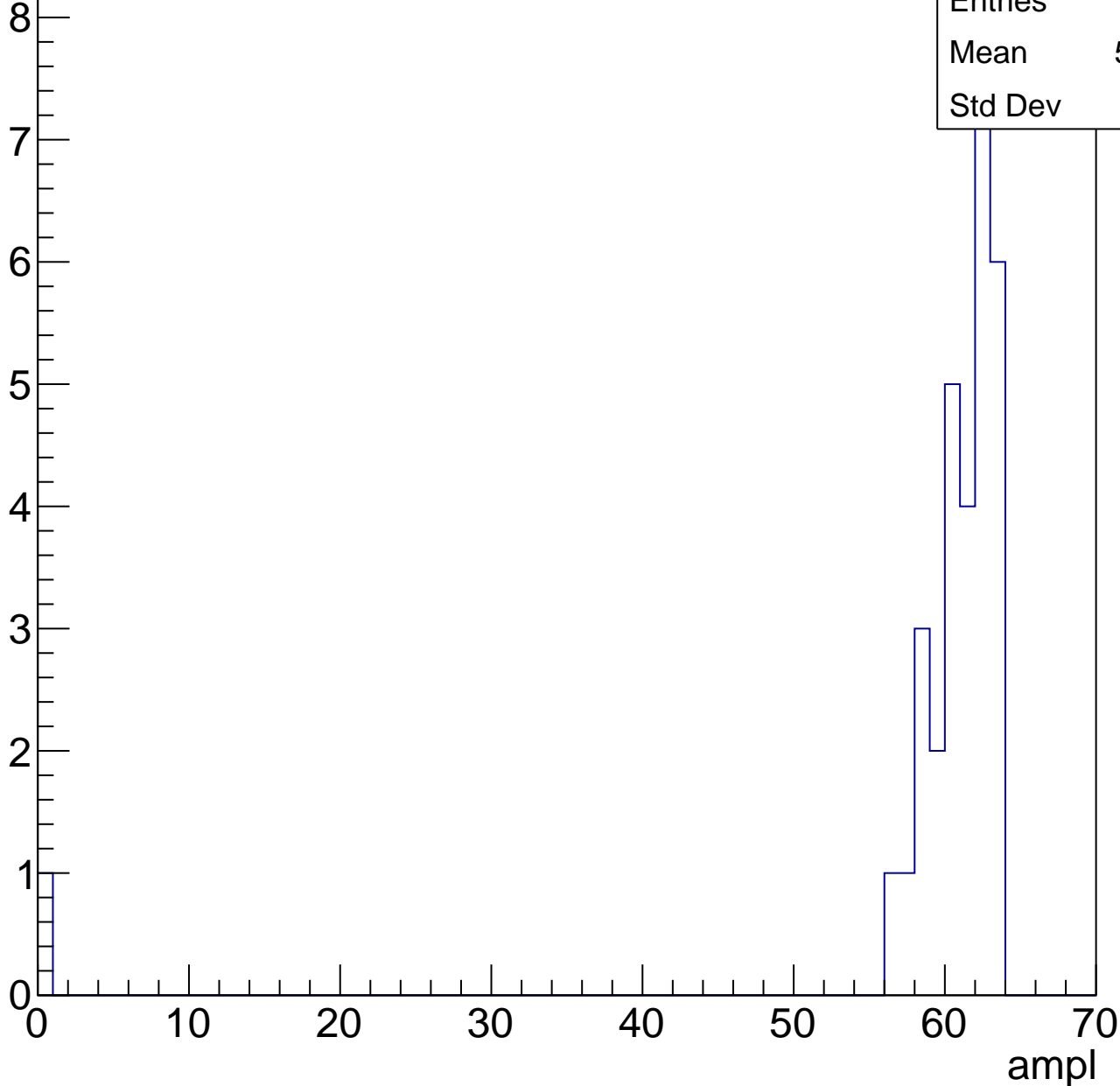


# B0L001S, U2-ch77, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 31    |
| Mean    | 58.81 |
| Std Dev | 10.9  |



# B0L001S, U2-ch77, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

|         |        |
|---------|--------|
| Entries | 3      |
| Mean    | 62.67  |
| Std Dev | 0.4714 |

ampl

0 10 20 30 40 50 60 70



# B0L001S, U2-ch77, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U2-ch78, adc0

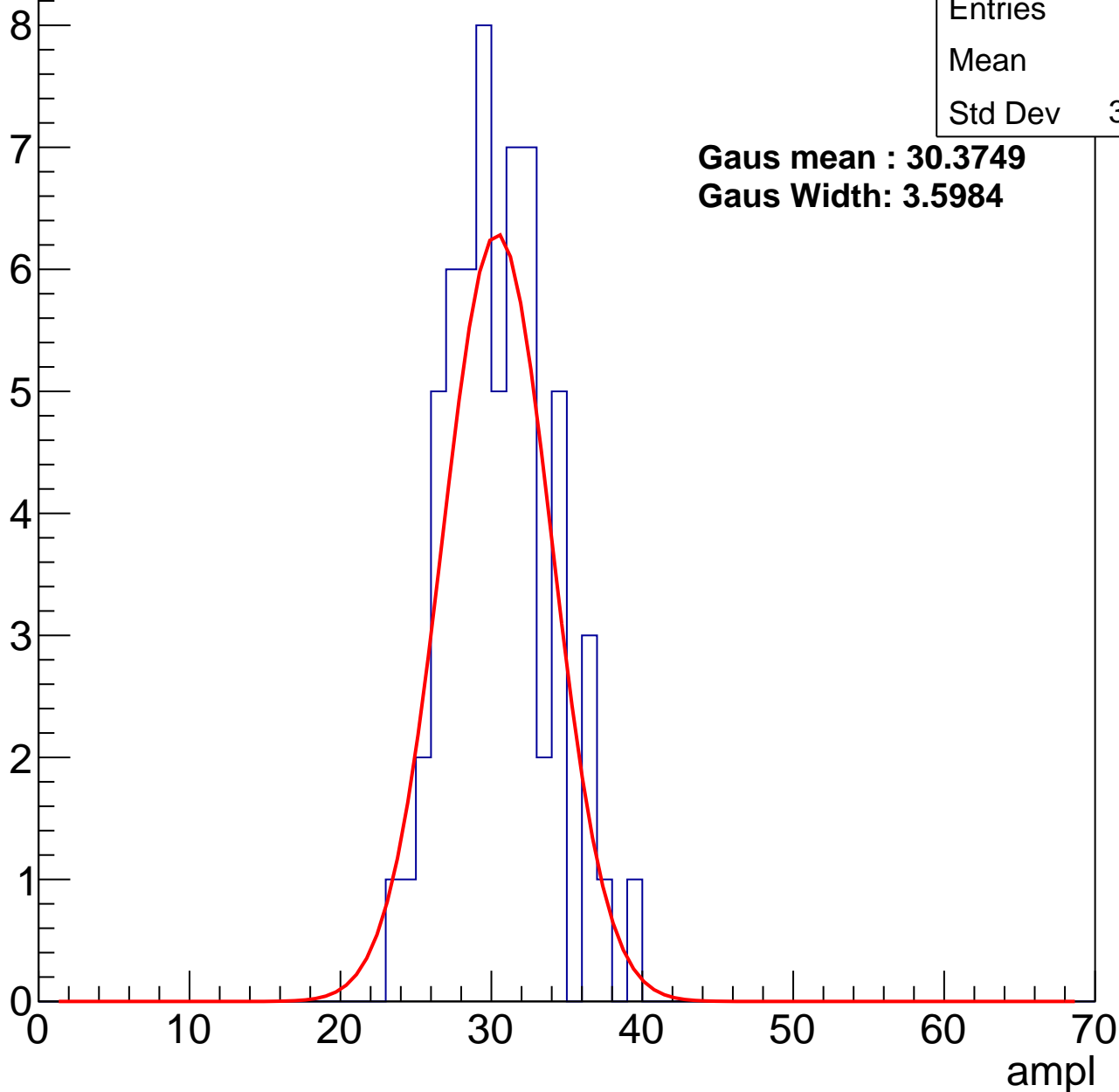
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 60    |
| Mean    | 30    |
| Std Dev | 3.347 |

**Gaus mean : 30.3749**

**Gaus Width: 3.5984**



# B0L001S, U2-ch78, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 79    |
| Mean    | 36.82 |
| Std Dev | 4.034 |

**Gaus mean : 36.6292**

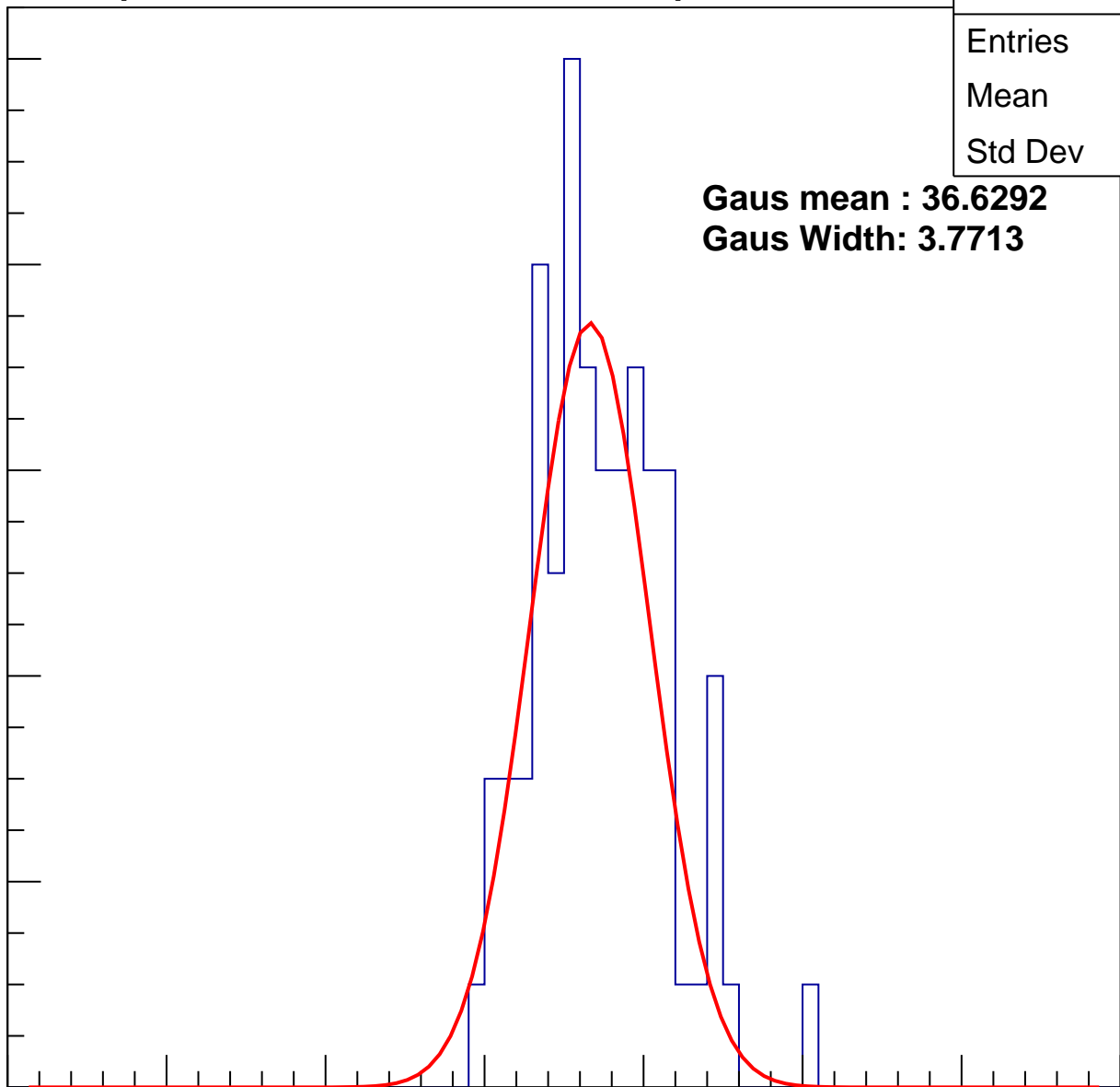
**Gaus Width: 3.7713**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U2-ch78, adc2

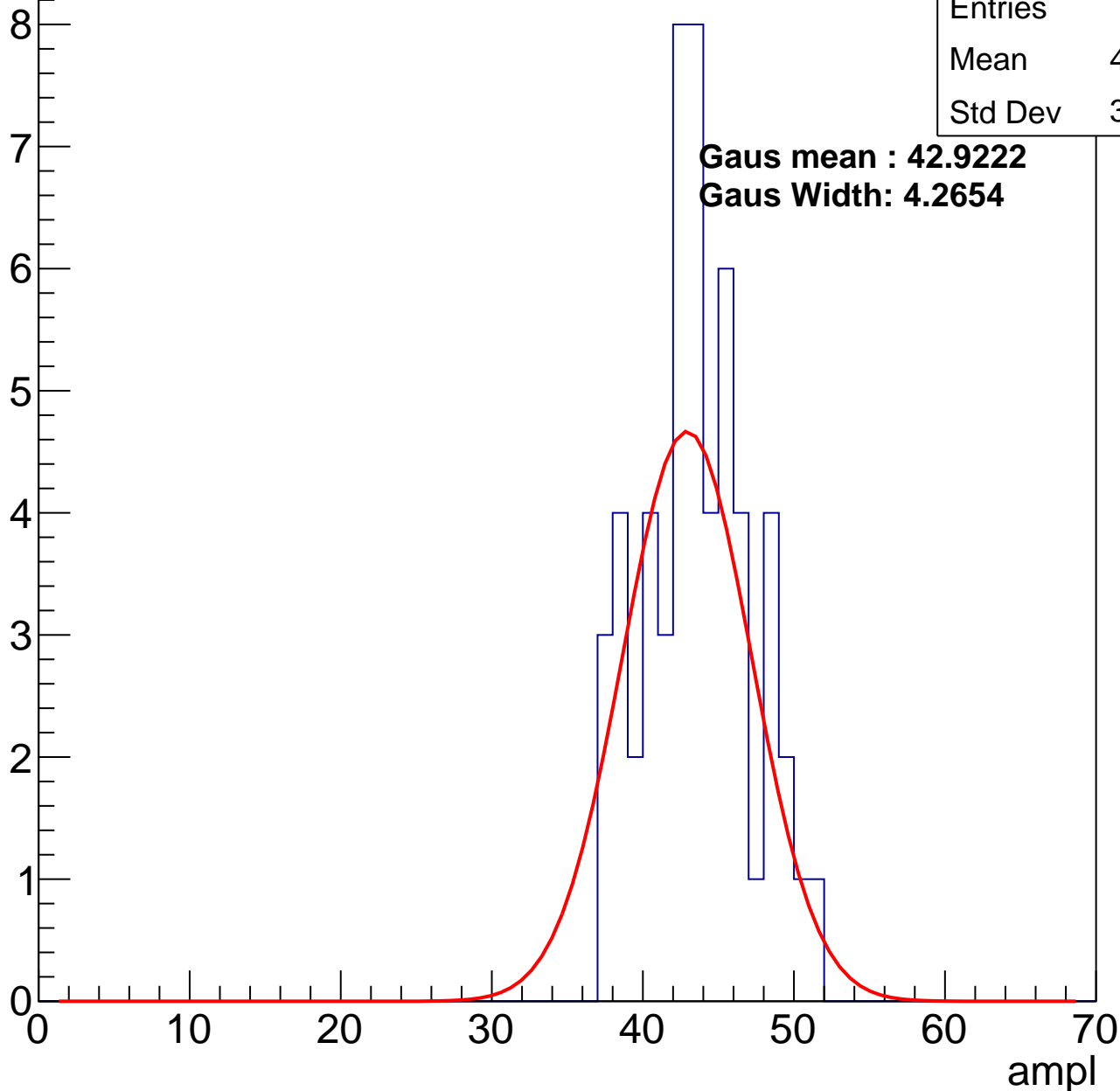
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 55    |
| Mean    | 43.13 |
| Std Dev | 3.464 |

**Gaus mean : 42.9222**

**Gaus Width: 4.2654**

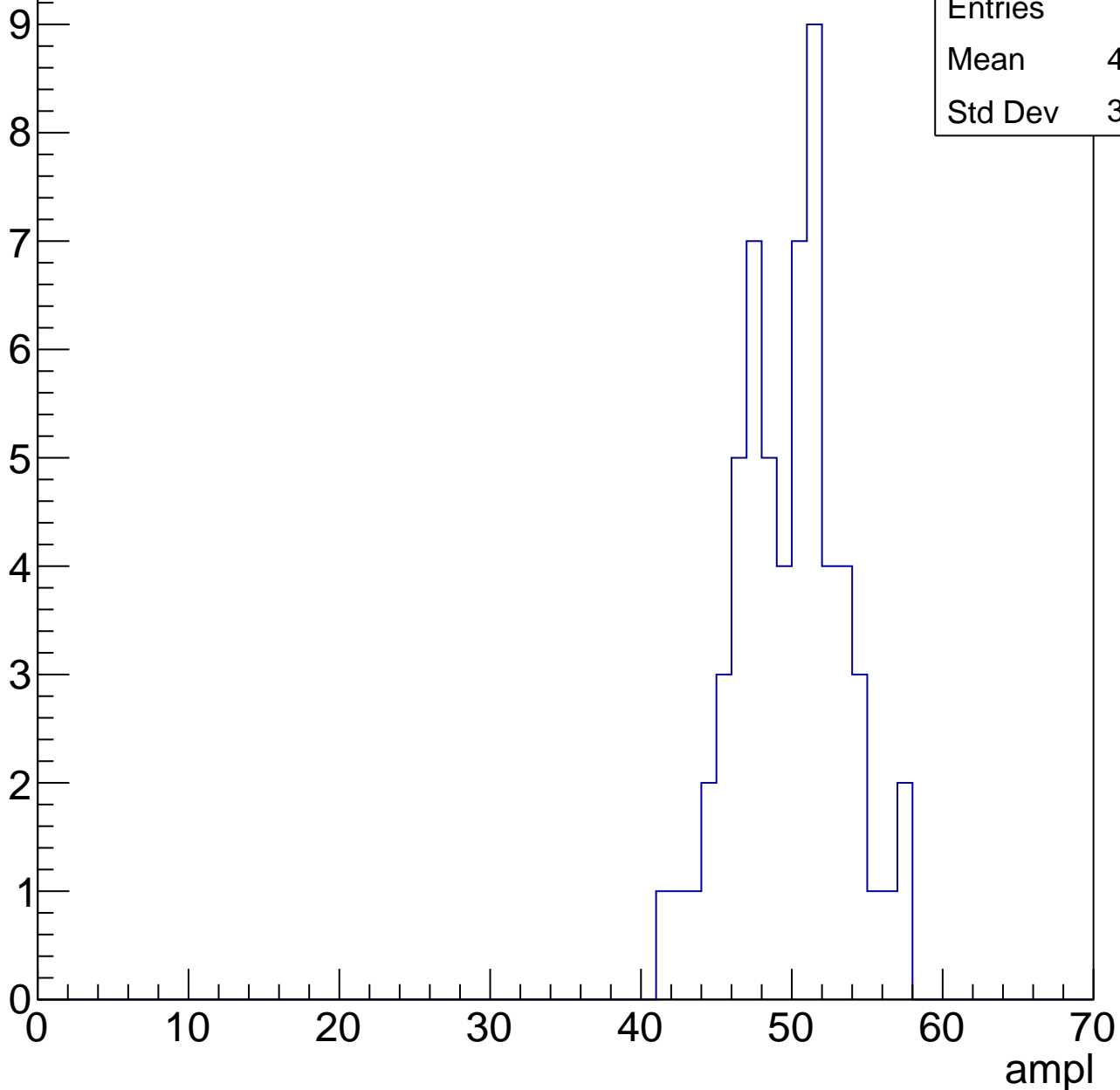


# B0L001S, U2-ch78, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 60    |
| Mean    | 49.33 |
| Std Dev | 3.534 |

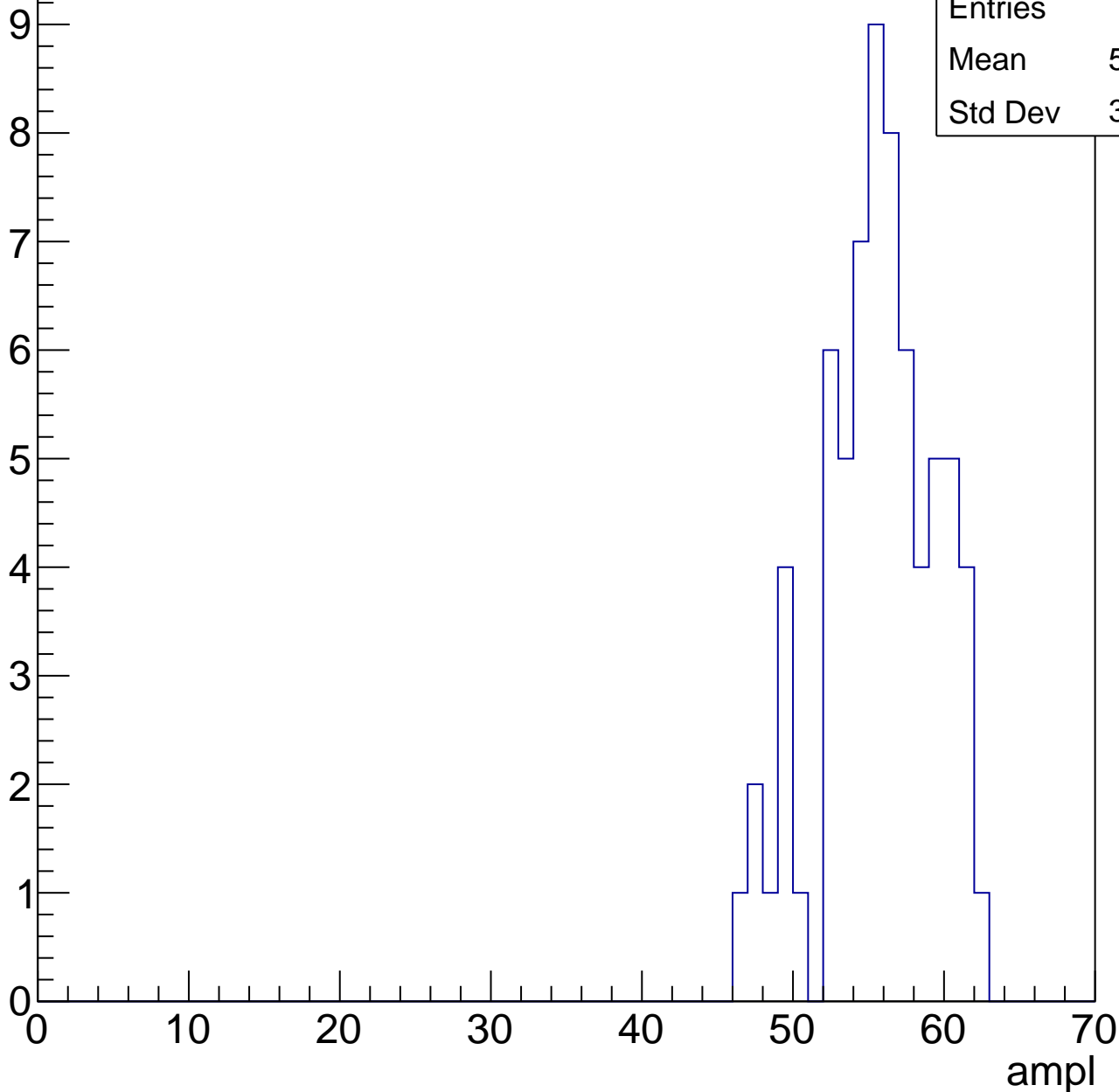


# B0L001S, U2-ch78, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 69    |
| Mean    | 55.17 |
| Std Dev | 3.753 |

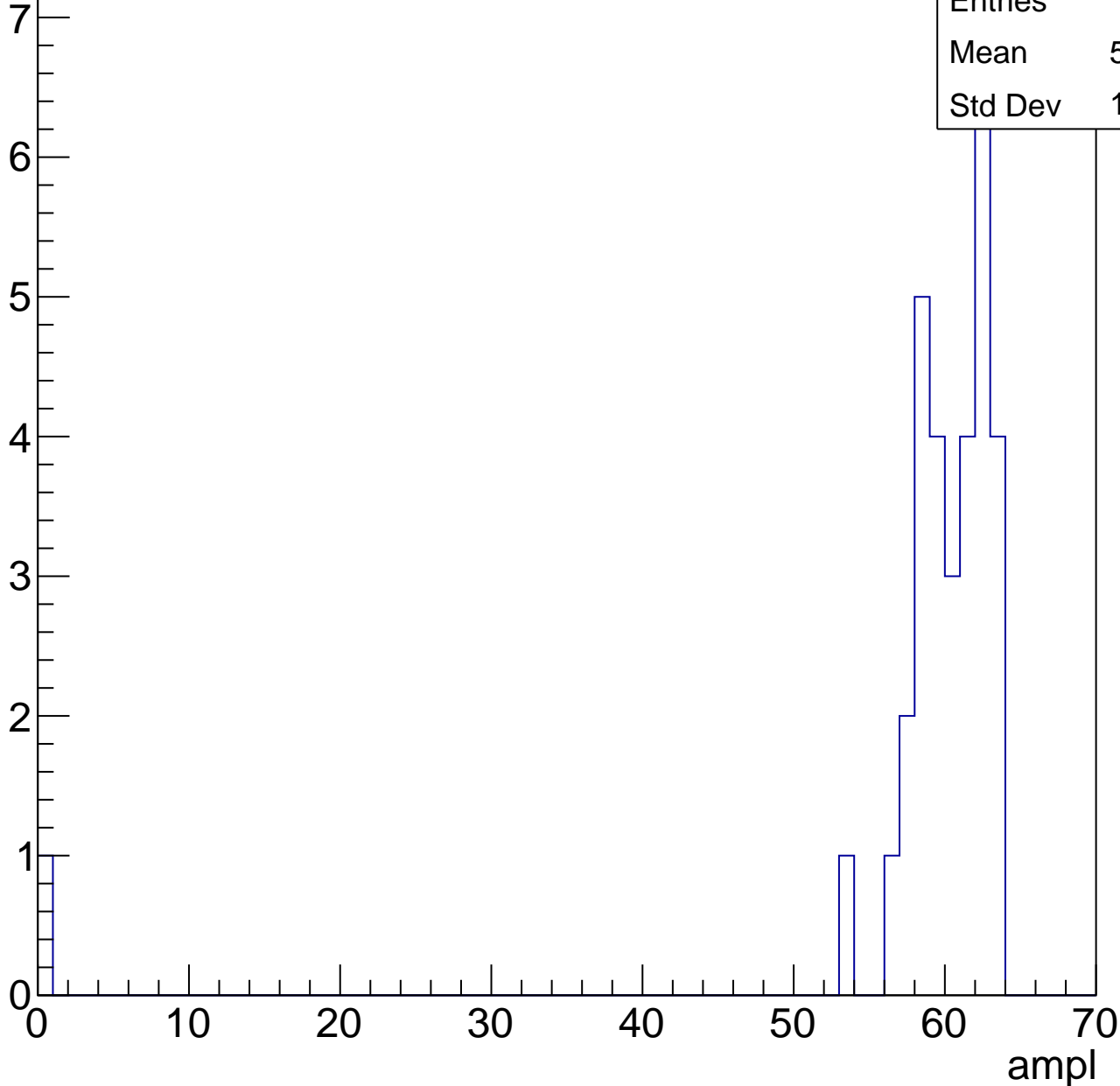


# B0L001S, U2-ch78, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 32    |
| Mean    | 58.09 |
| Std Dev | 10.69 |

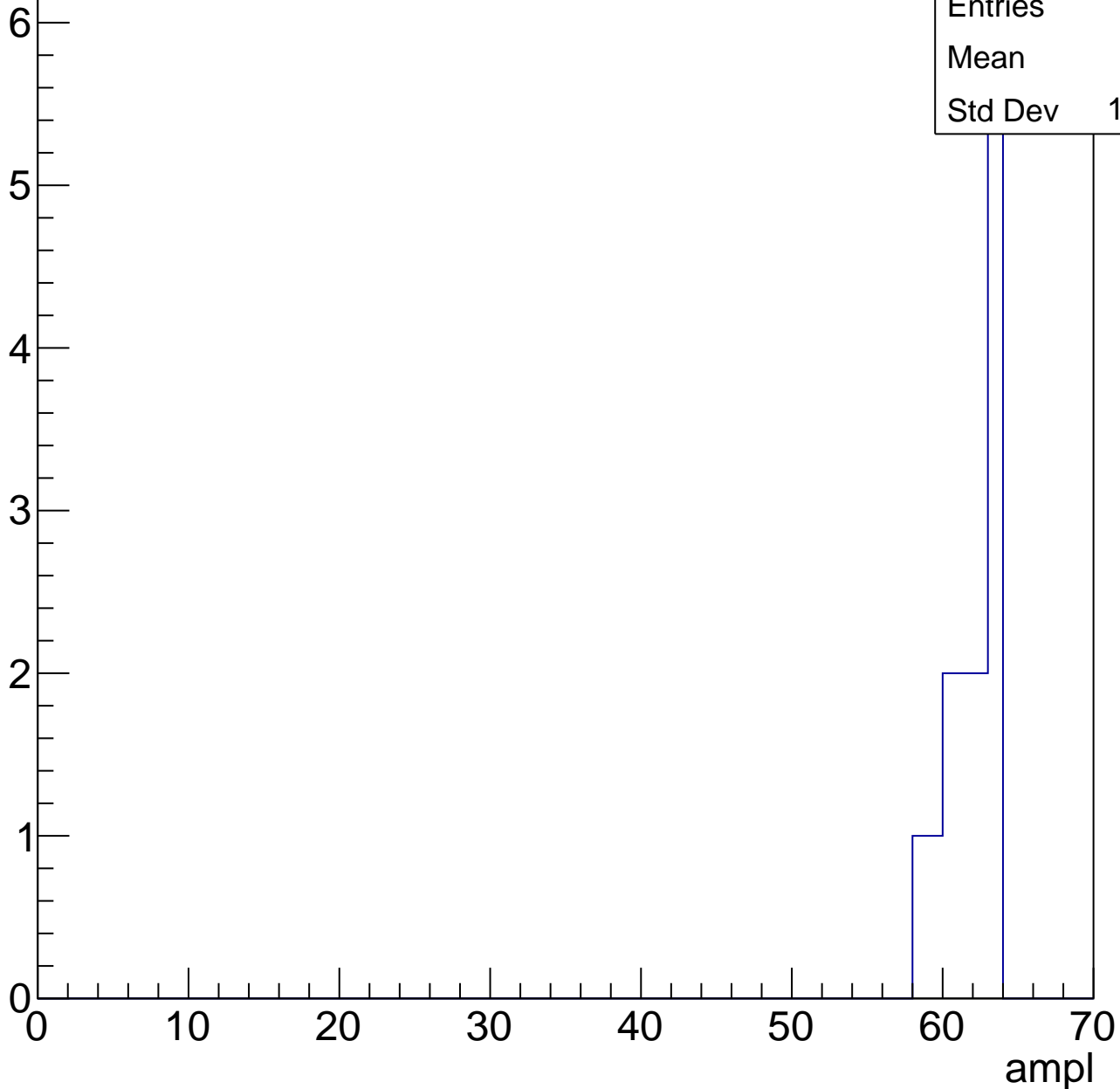


# B0L001S, U2-ch78, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 14    |
| Mean    | 61.5  |
| Std Dev | 1.637 |





# B0L001S, U2-ch78, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 0 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch79, adc0

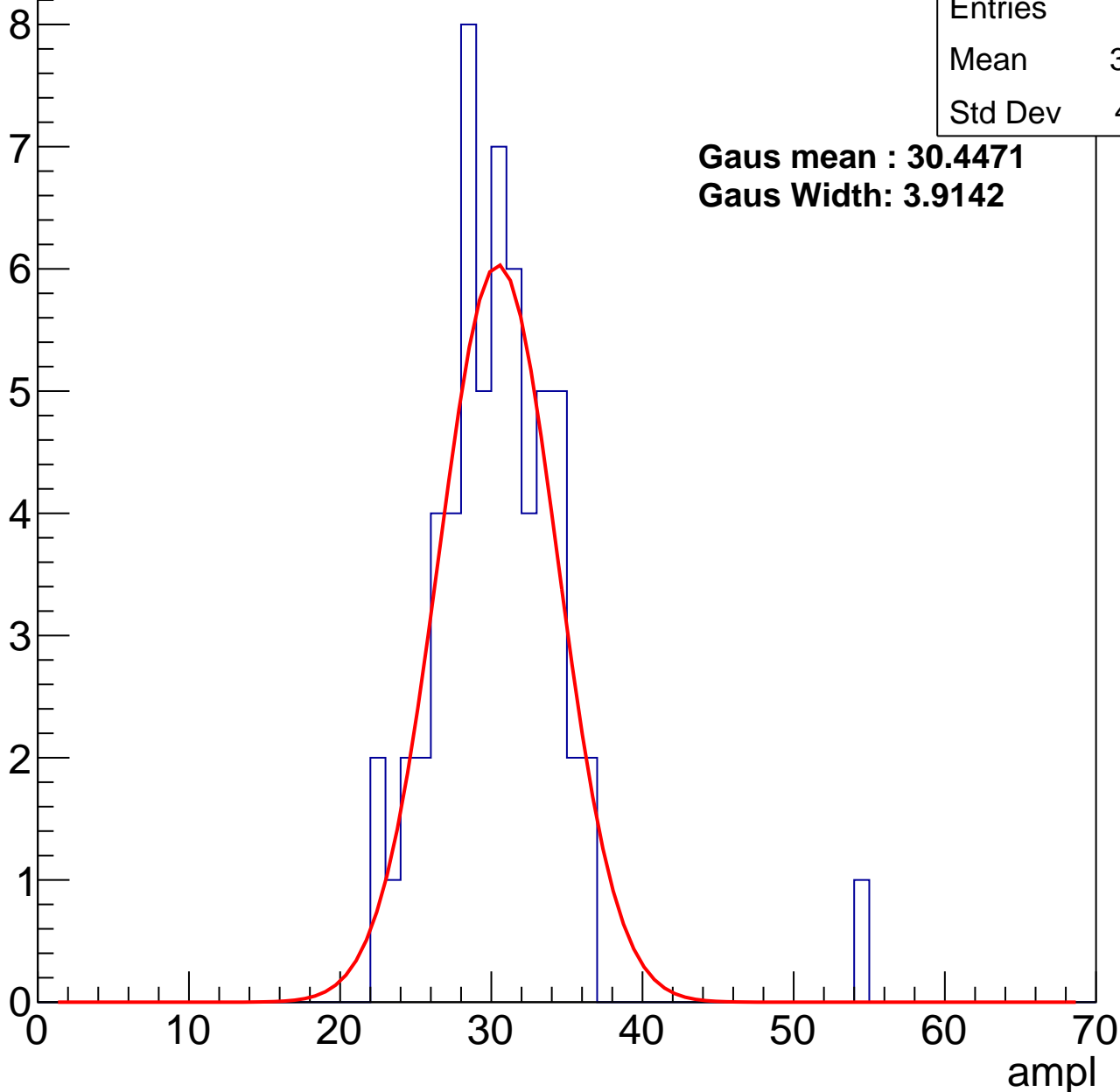
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 60    |
| Mean    | 30.02 |
| Std Dev | 4.621 |

**Gaus mean : 30.4471**

**Gaus Width: 3.9142**



# B0L001S, U2-ch79, adc1

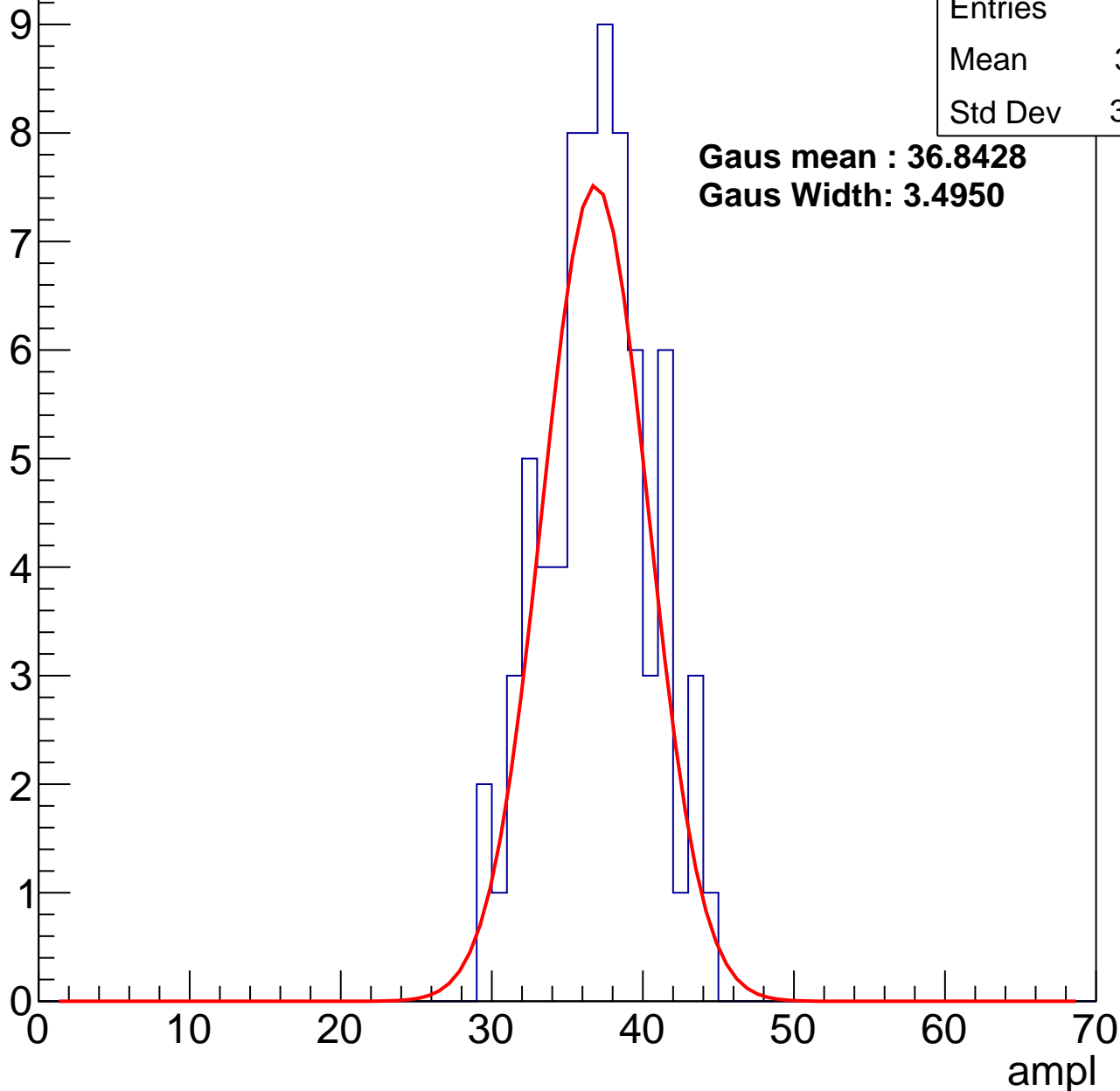
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 72    |
| Mean    | 36.51 |
| Std Dev | 3.476 |

**Gaus mean : 36.8428**

**Gaus Width: 3.4950**



# B0L001S, U2-ch79, adc2

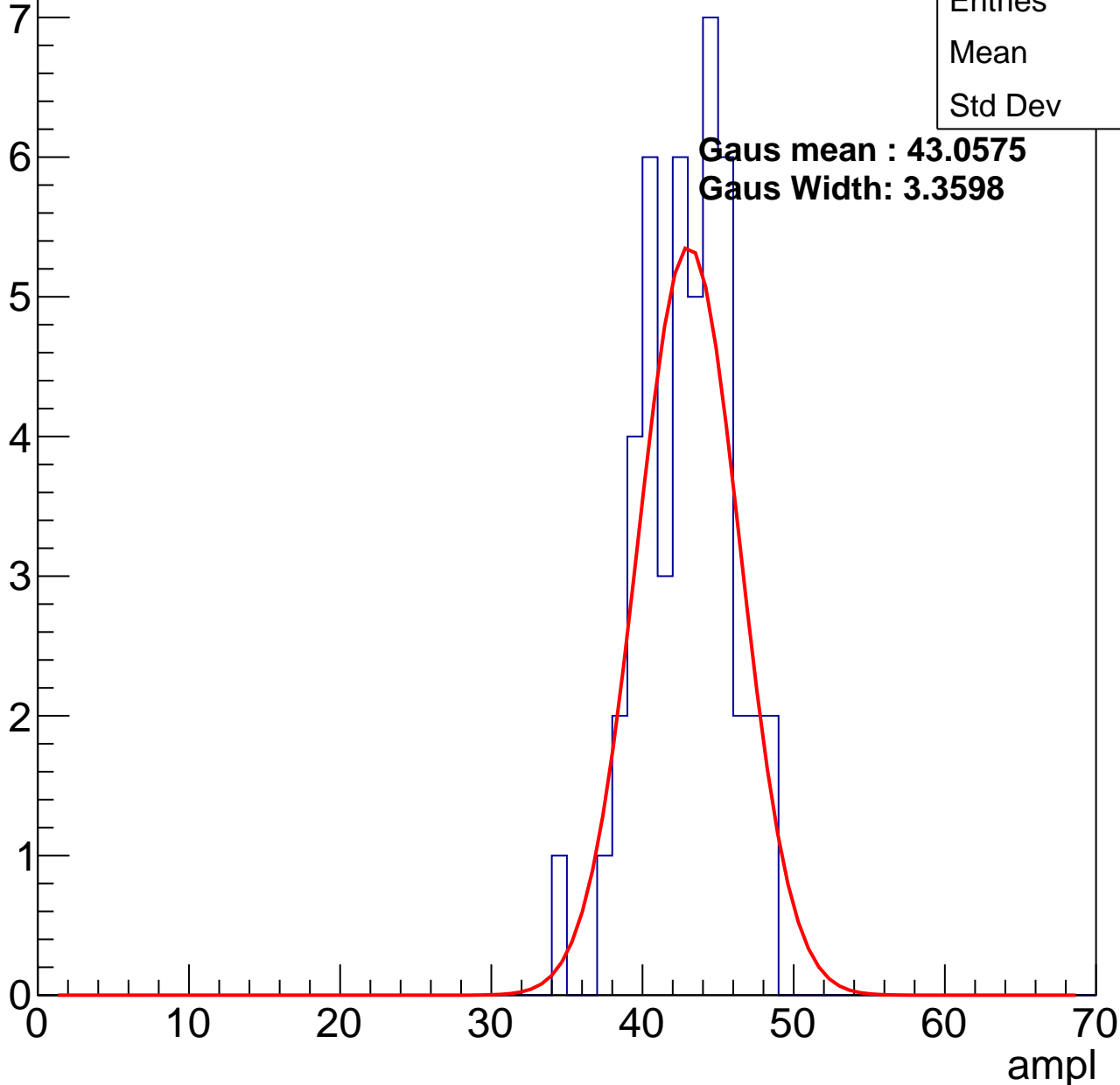
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |      |
|---------|------|
| Entries | 47   |
| Mean    | 42.4 |
| Std Dev | 2.98 |

**Gaus mean : 43.0575**

**Gaus Width: 3.3598**



# B0L001S, U2-ch79, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

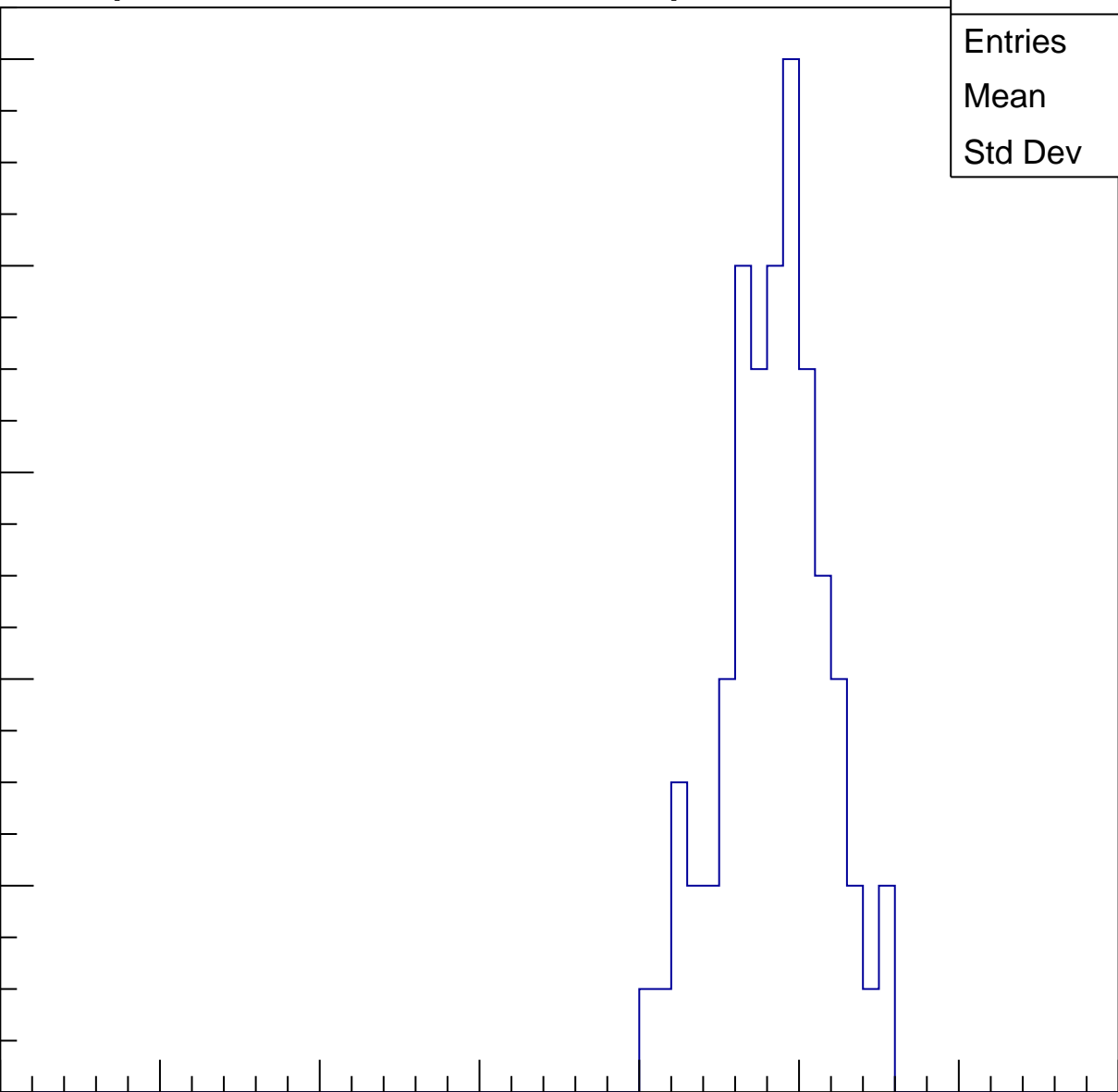
|         |       |
|---------|-------|
| Entries | 67    |
| Mean    | 47.99 |
| Std Dev | 3.253 |

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

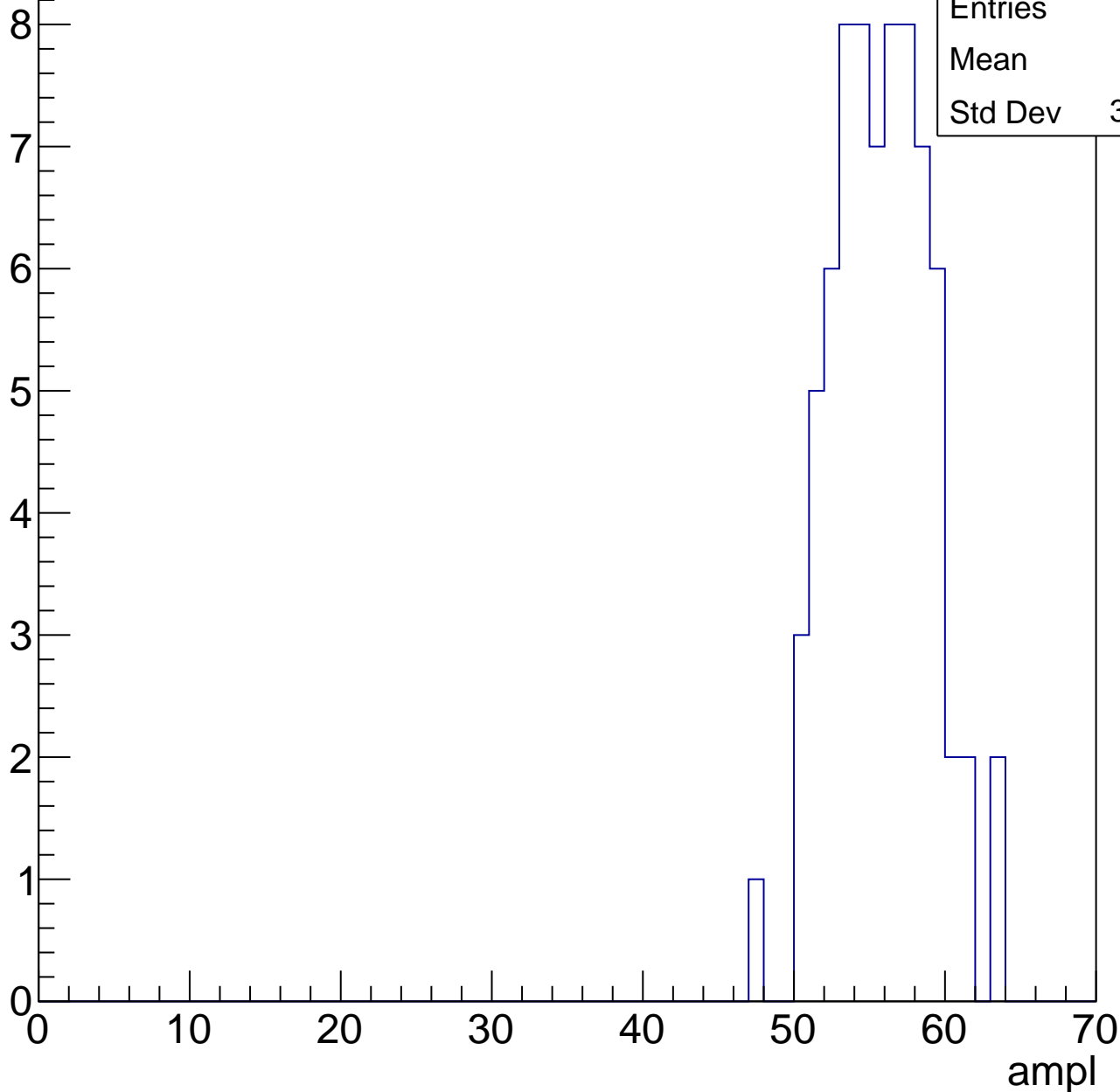


# B0L001S, U2-ch79, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 73    |
| Mean    | 55.3  |
| Std Dev | 3.217 |



# B0L001S, U2-ch79, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

|         |       |
|---------|-------|
| Entries | 43    |
| Mean    | 59.02 |
| Std Dev | 9.337 |

ampl

0 10 20 30 40 50 60 70

0

1

2

3

4

5

6

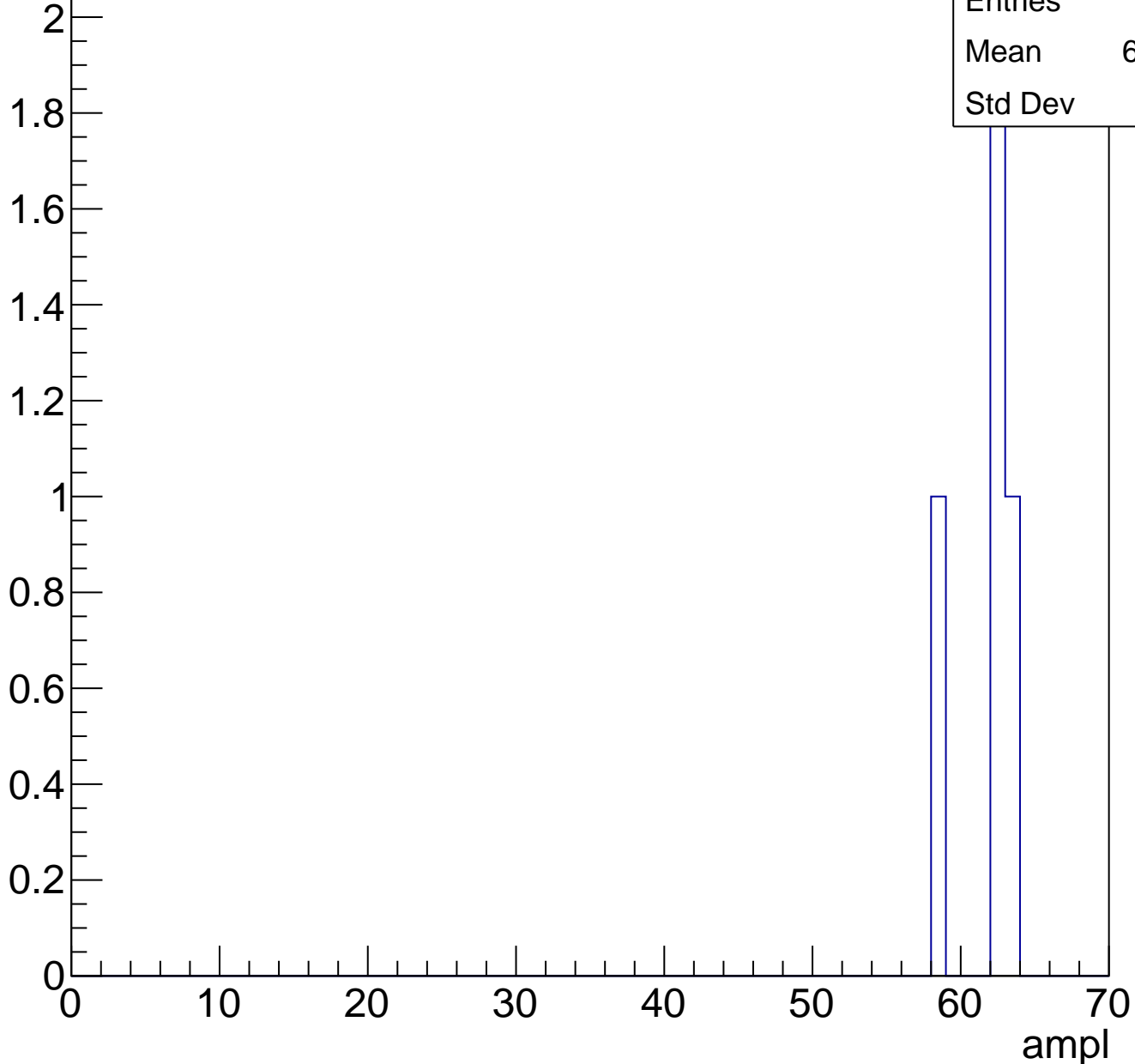
7

8

# B0L001S, U2-ch79, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch79, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 2 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch80, adc0

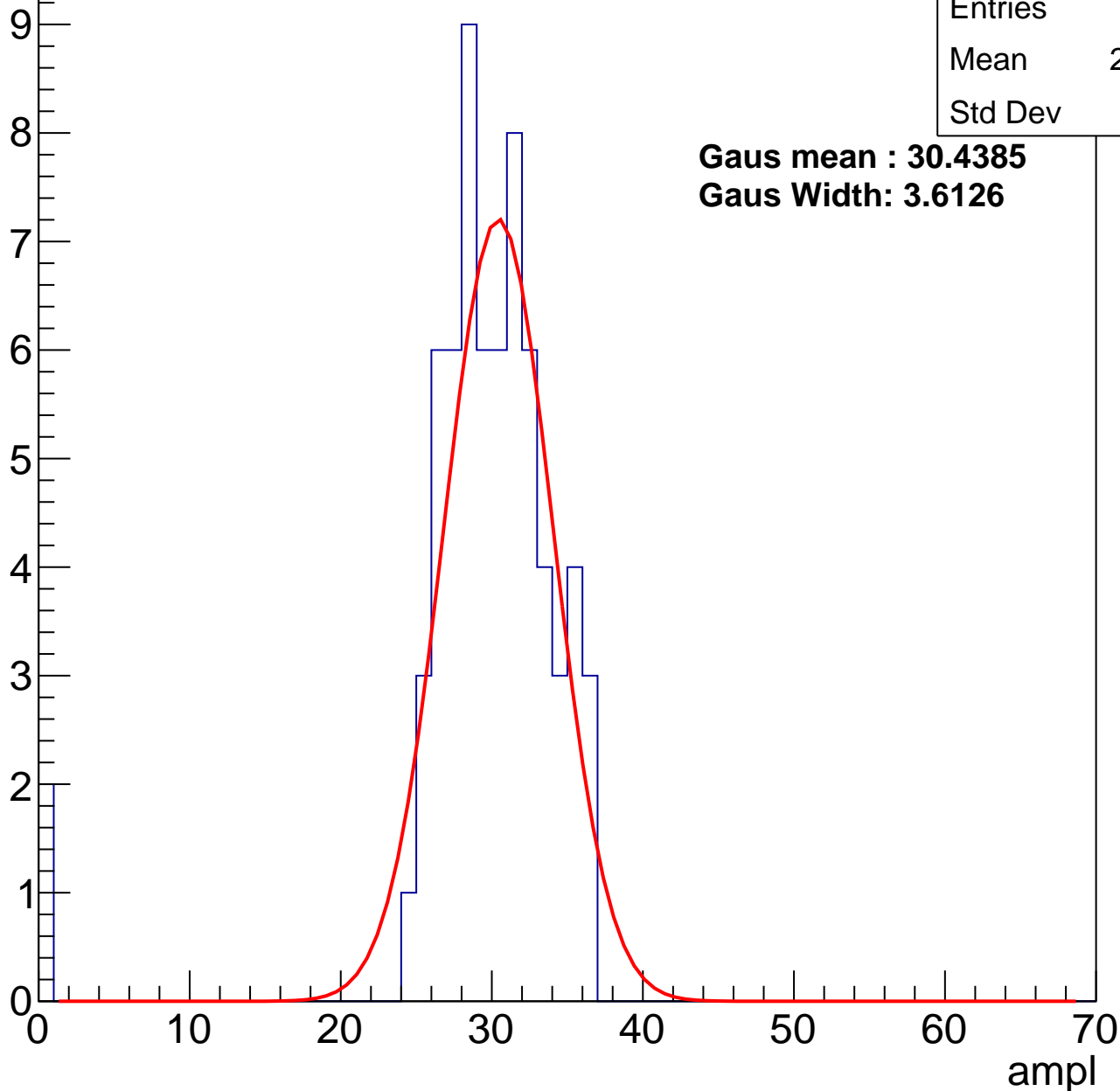
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 67    |
| Mean    | 29.03 |
| Std Dev | 5.94  |

**Gaus mean : 30.4385**

**Gaus Width: 3.6126**



# B0L001S, U2-ch80, adc1

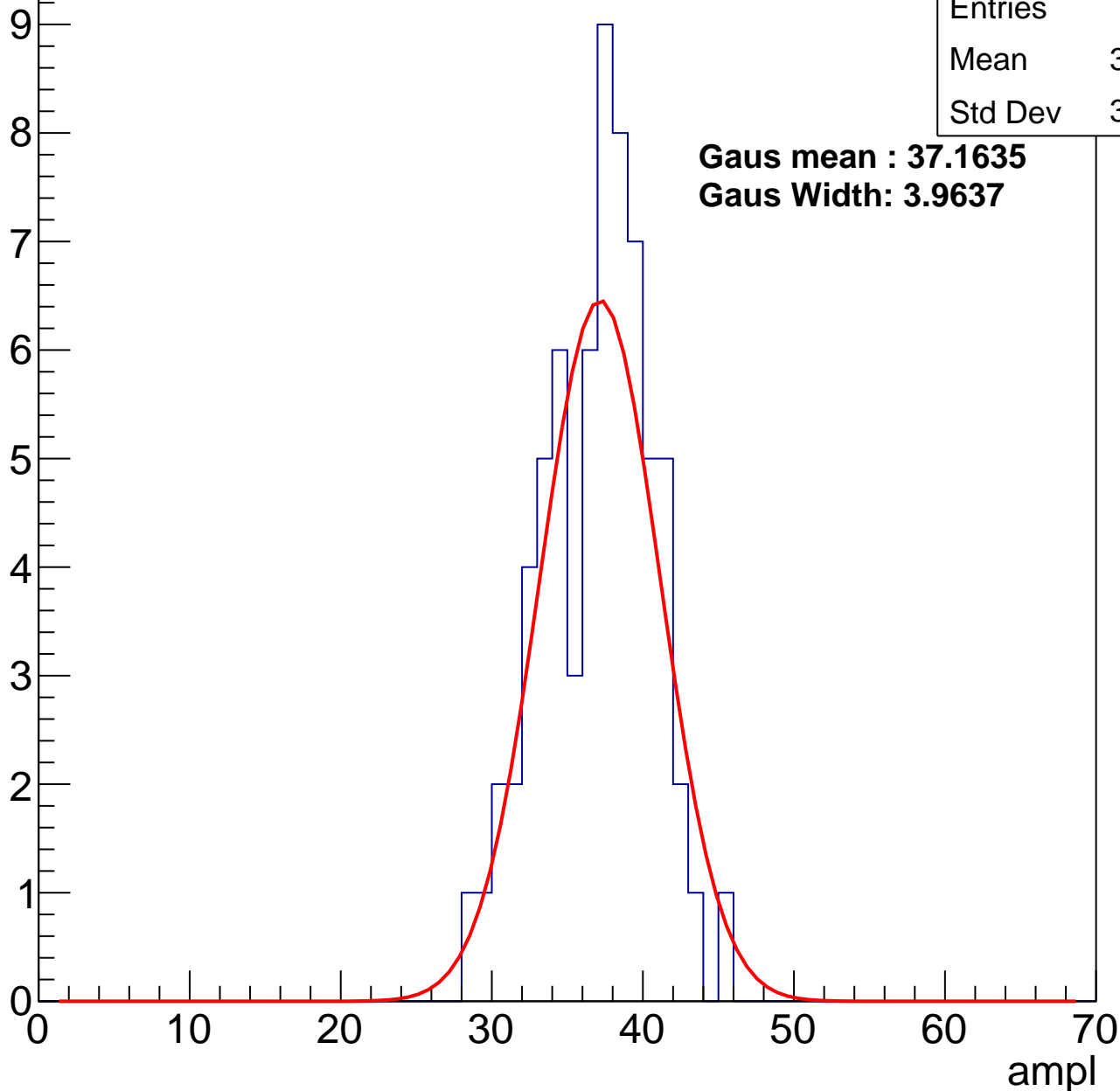
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 68    |
| Mean    | 36.53 |
| Std Dev | 3.562 |

**Gaus mean : 37.1635**

**Gaus Width: 3.9637**



# B0L001S, U2-ch80, adc2

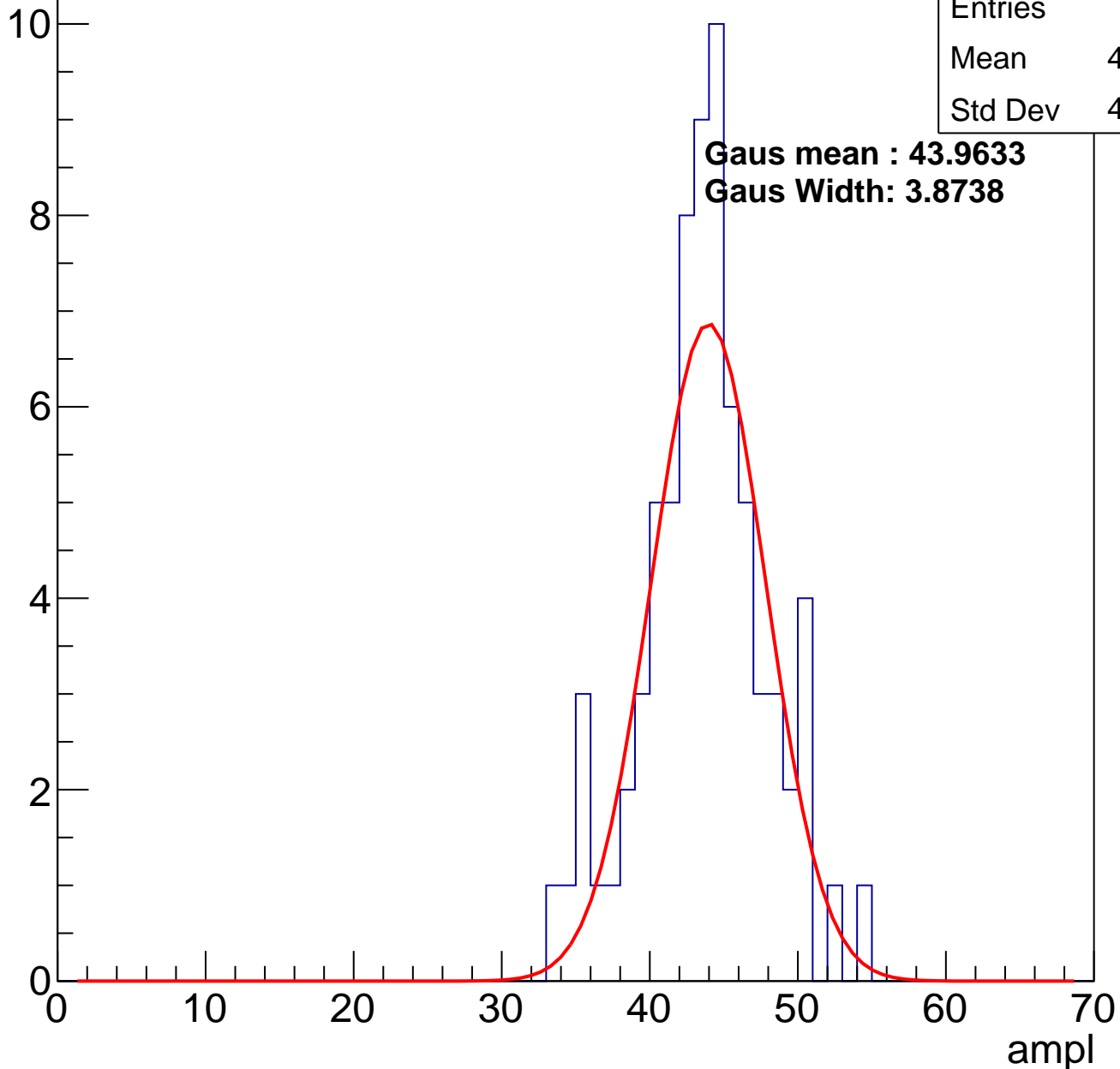
calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 74    |
| Mean    | 43.18 |
| Std Dev | 4.189 |

**Gaus mean : 43.9633**

**Gaus Width: 3.8738**

Entry

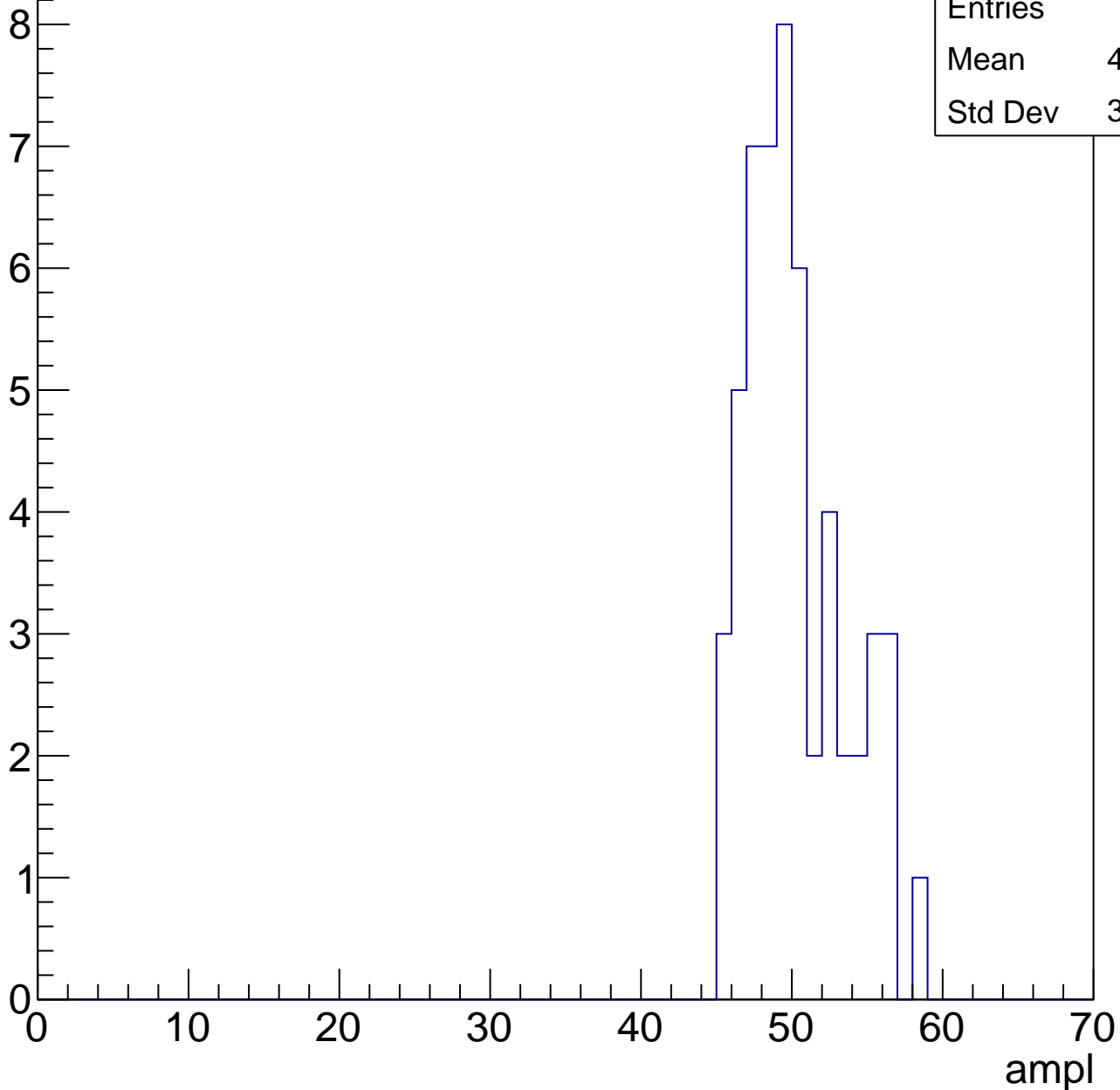


# B0L001S, U2-ch80, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

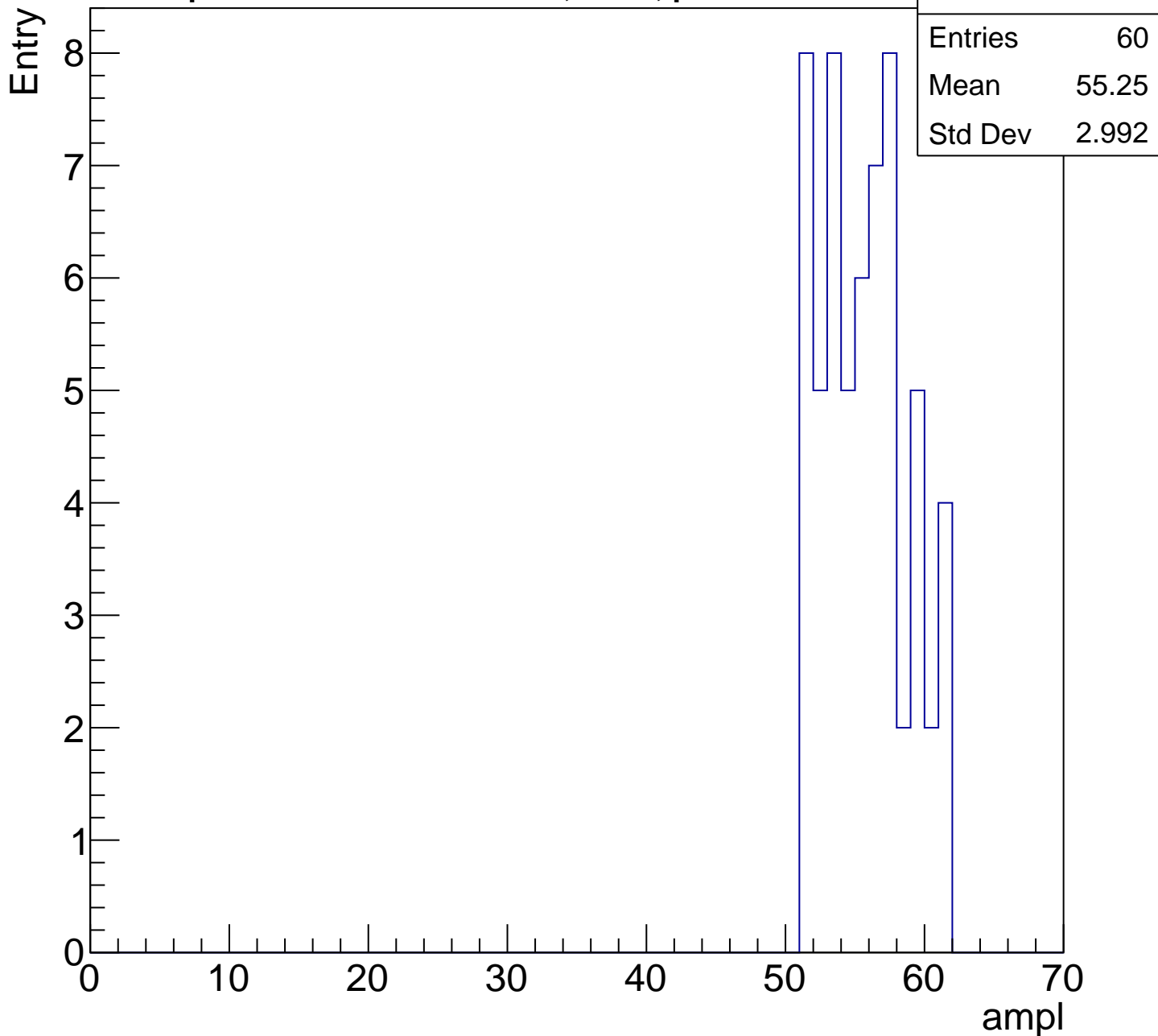
Entry

|         |       |
|---------|-------|
| Entries | 53    |
| Mean    | 49.75 |
| Std Dev | 3.267 |



# B0L001S, U2-ch80, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

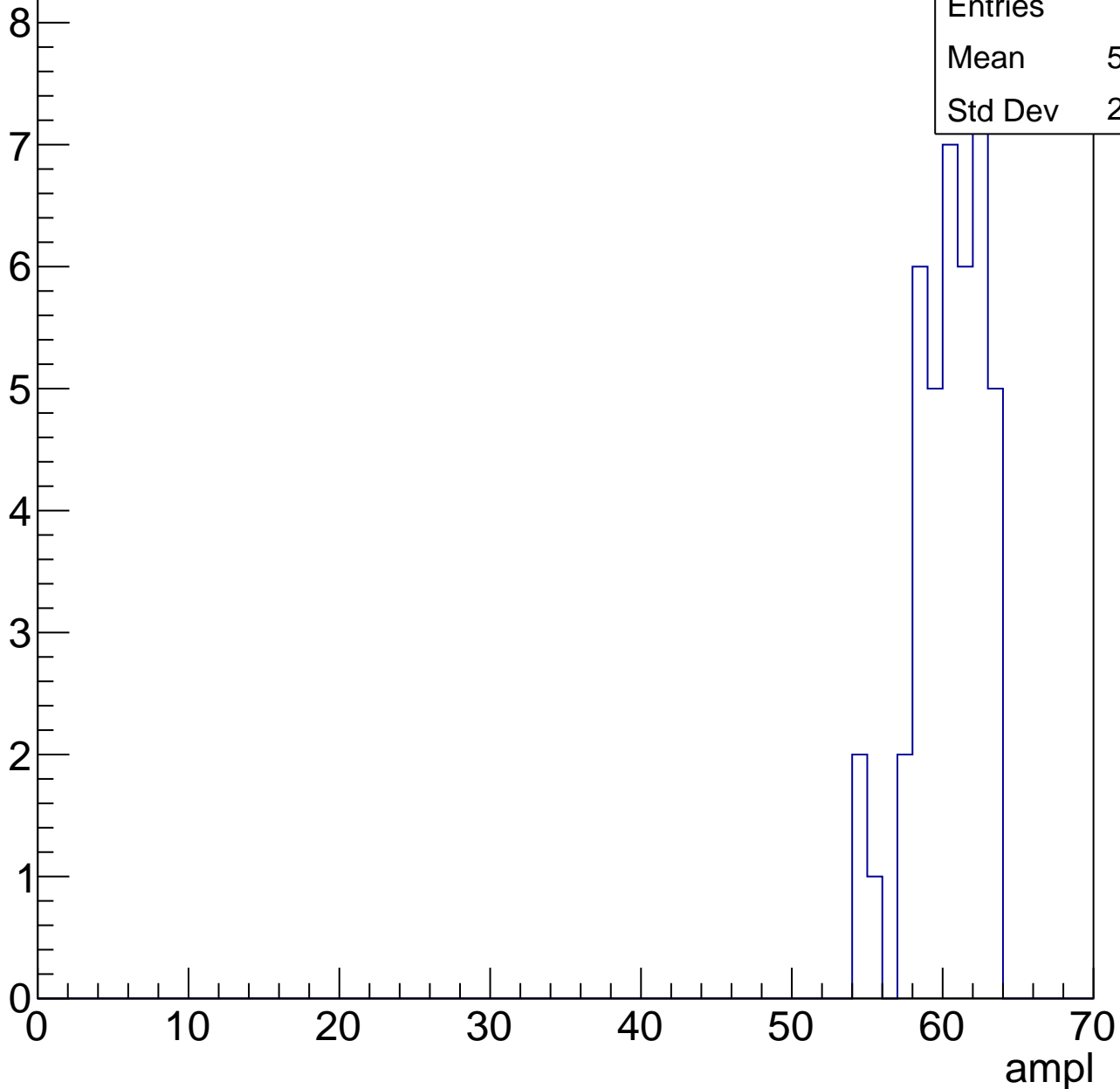


# B0L001S, U2-ch80, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

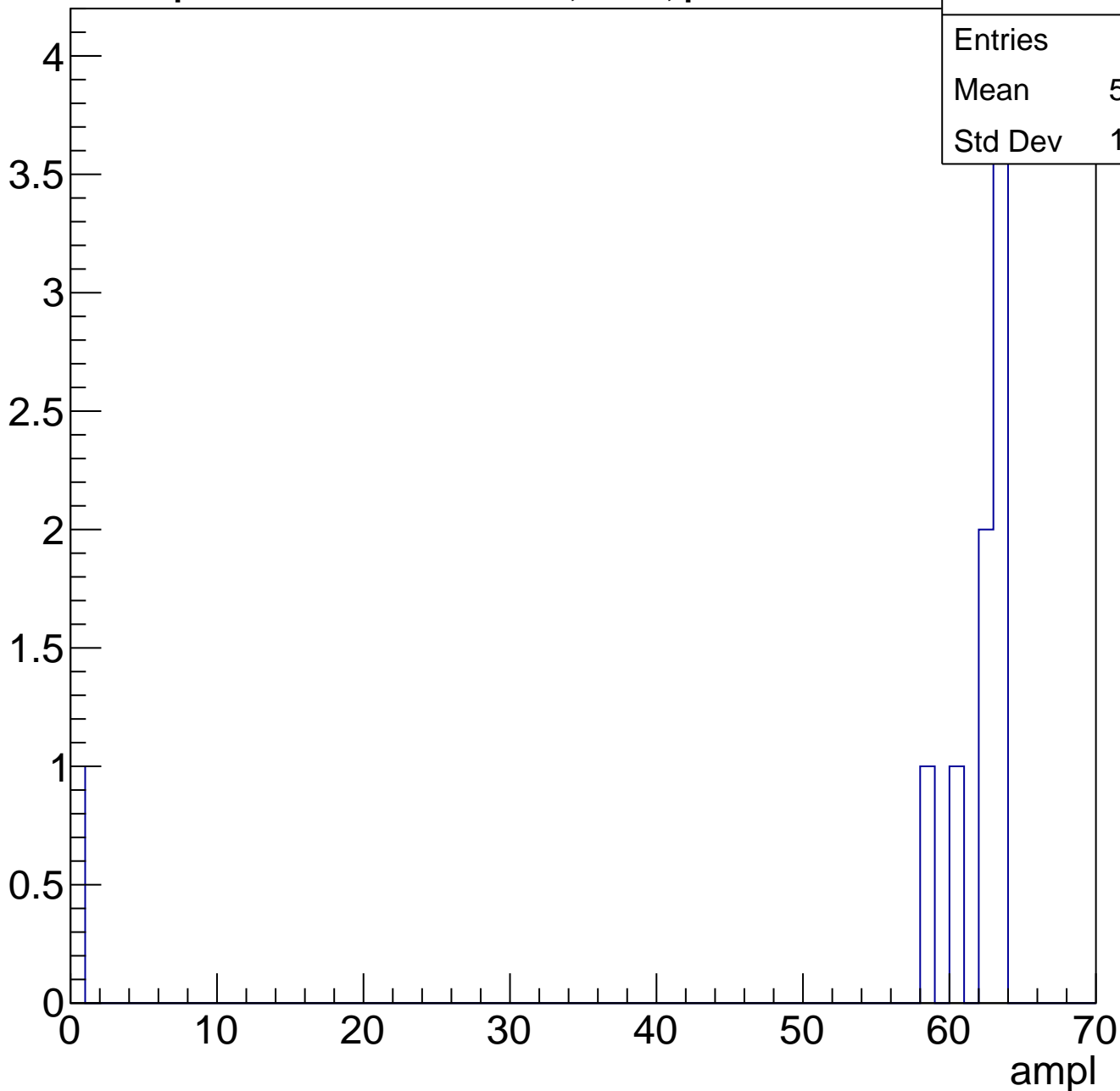
|         |       |
|---------|-------|
| Entries | 42    |
| Mean    | 59.93 |
| Std Dev | 2.324 |



# B0L001S, U2-ch80, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch80, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U2-ch81, adc0

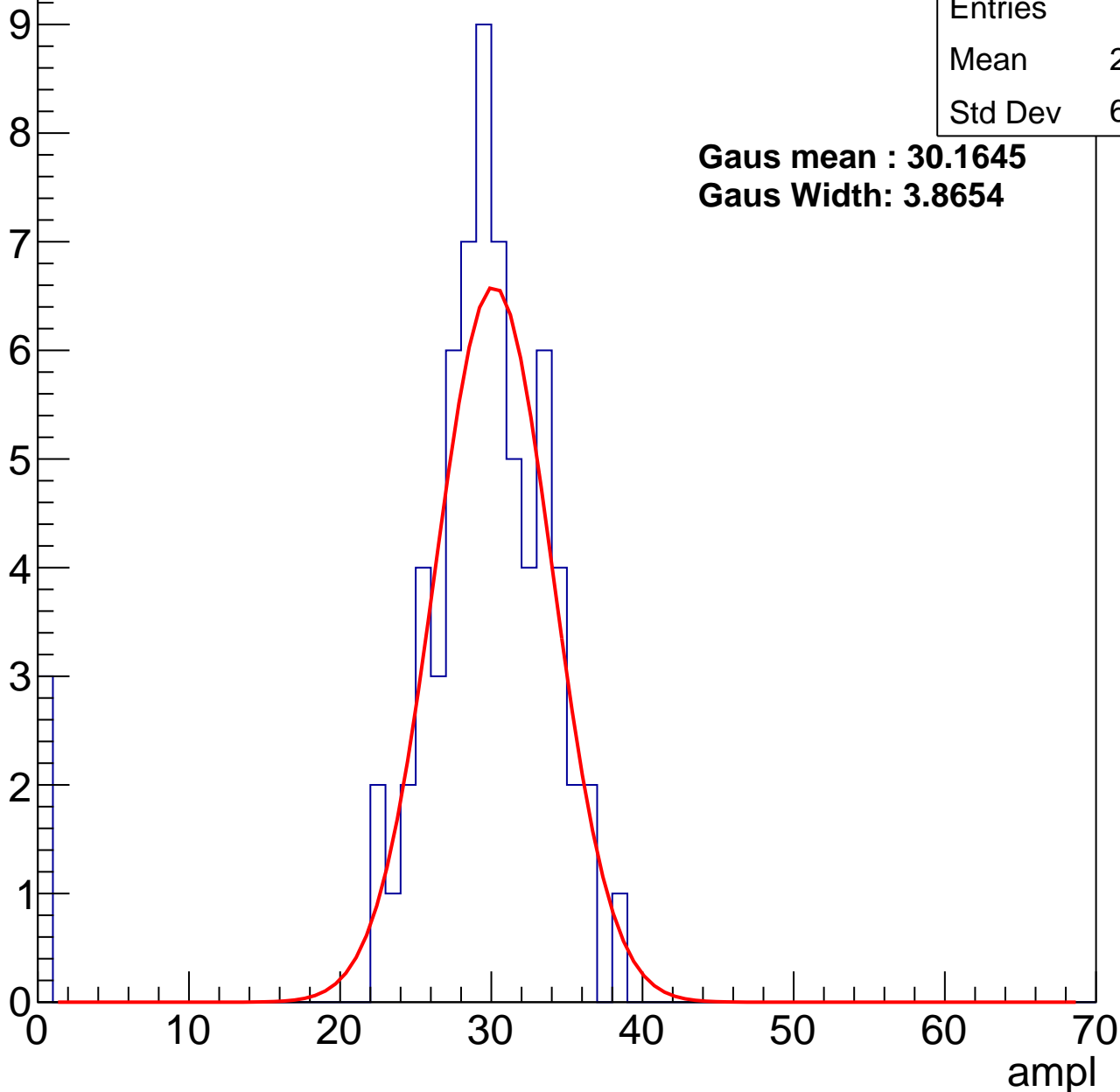
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 68    |
| Mean    | 28.22 |
| Std Dev | 6.964 |

**Gaus mean : 30.1645**

**Gaus Width: 3.8654**



# B0L001S, U2-ch81, adc1

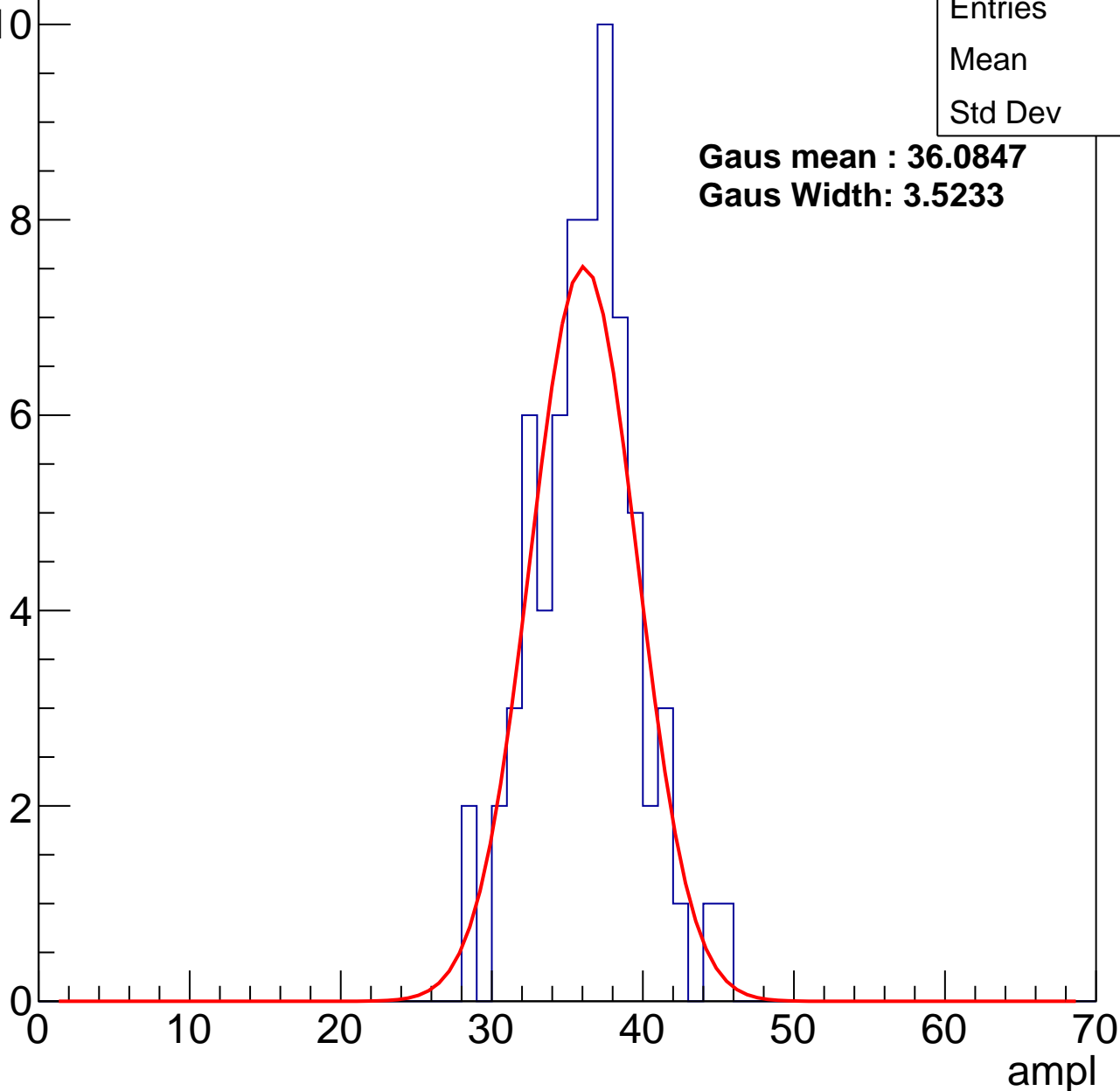
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |      |
|---------|------|
| Entries | 69   |
| Mean    | 35.8 |
| Std Dev | 3.42 |

**Gaus mean : 36.0847**

**Gaus Width: 3.5233**



# B0L001S, U2-ch81, adc2

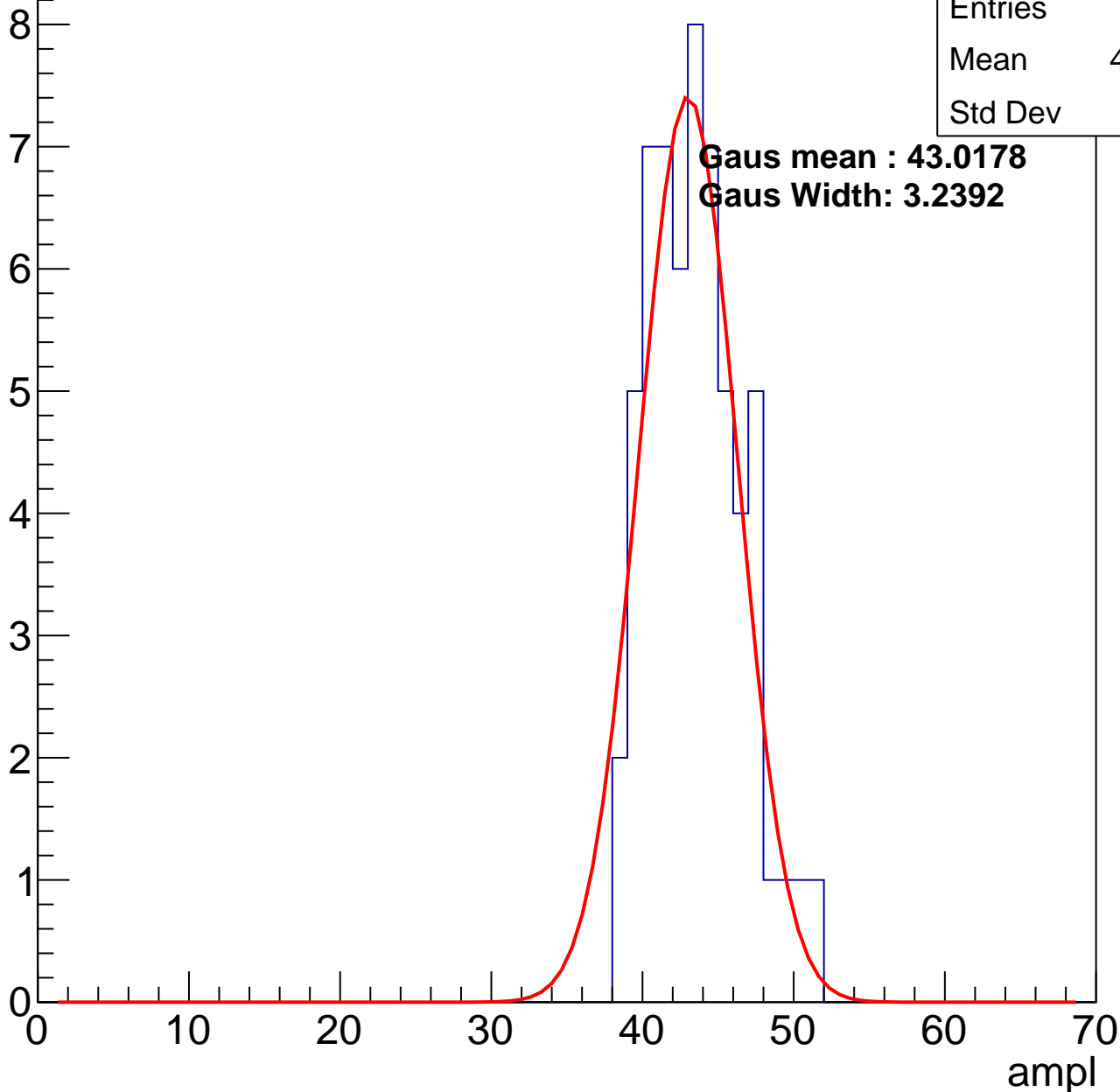
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 60    |
| Mean    | 43.07 |
| Std Dev | 3.01  |

**Gaus mean : 43.0178**

**Gaus Width: 3.2392**

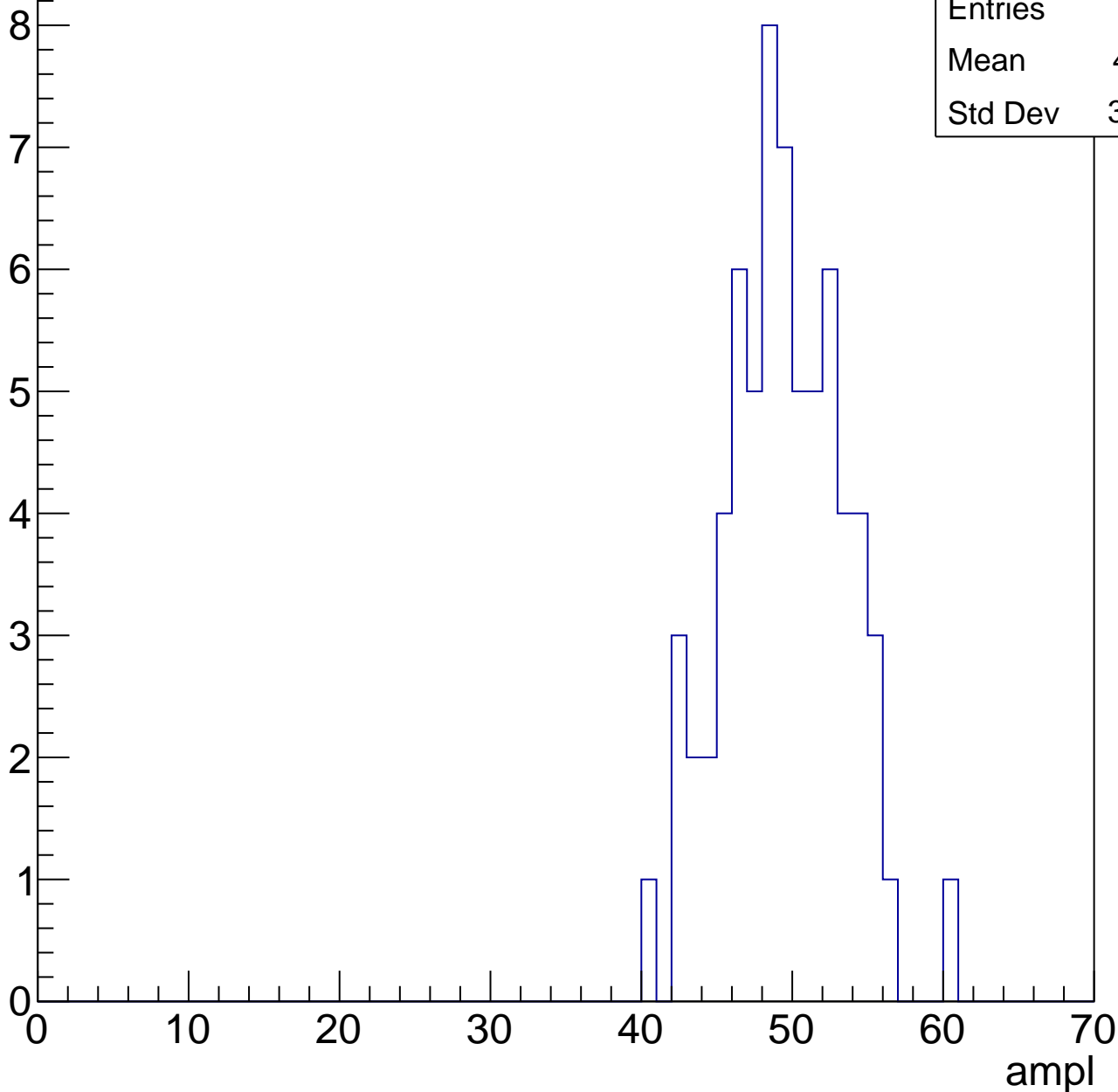


# B0L001S, U2-ch81, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

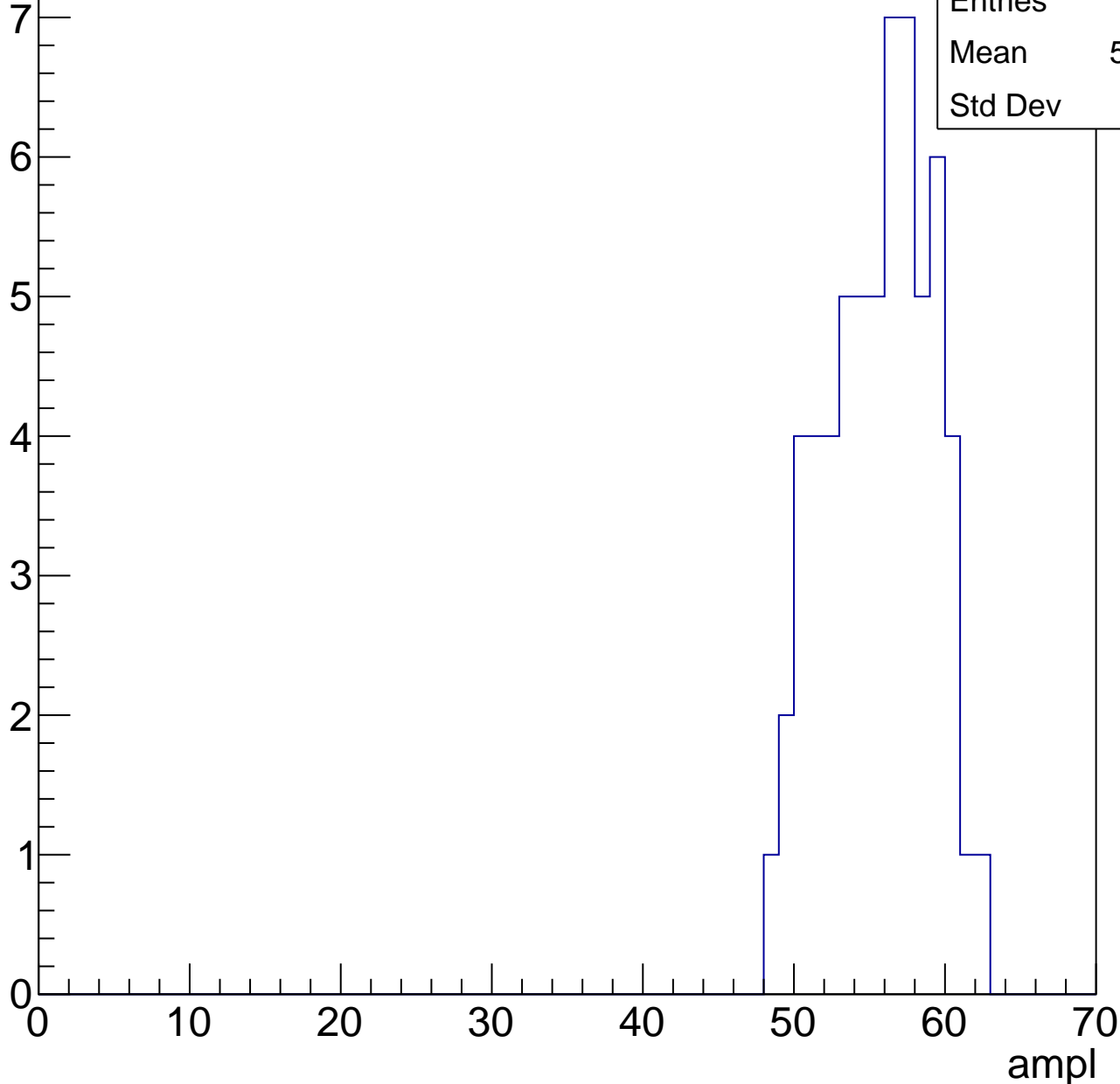
|         |       |
|---------|-------|
| Entries | 67    |
| Mean    | 49.01 |
| Std Dev | 3.896 |



# B0L001S, U2-ch81, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |       |
|---------|-------|
| Entries | 61    |
| Mean    | 55.18 |
| Std Dev | 3.4   |

# B0L001S, U2-ch81, adc5

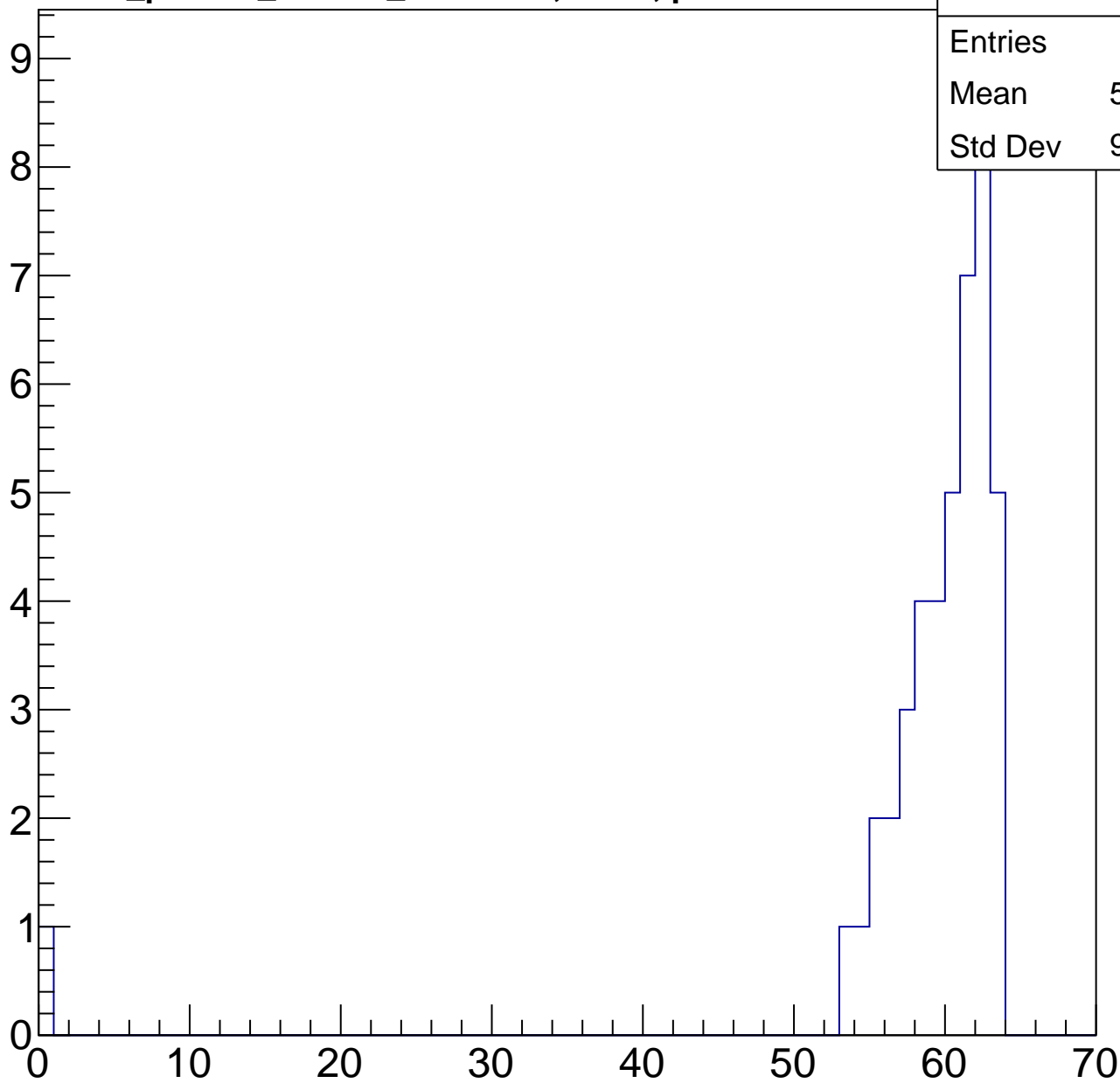
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

|         |       |
|---------|-------|
| Entries | 44    |
| Mean    | 58.36 |
| Std Dev | 9.274 |

ampl

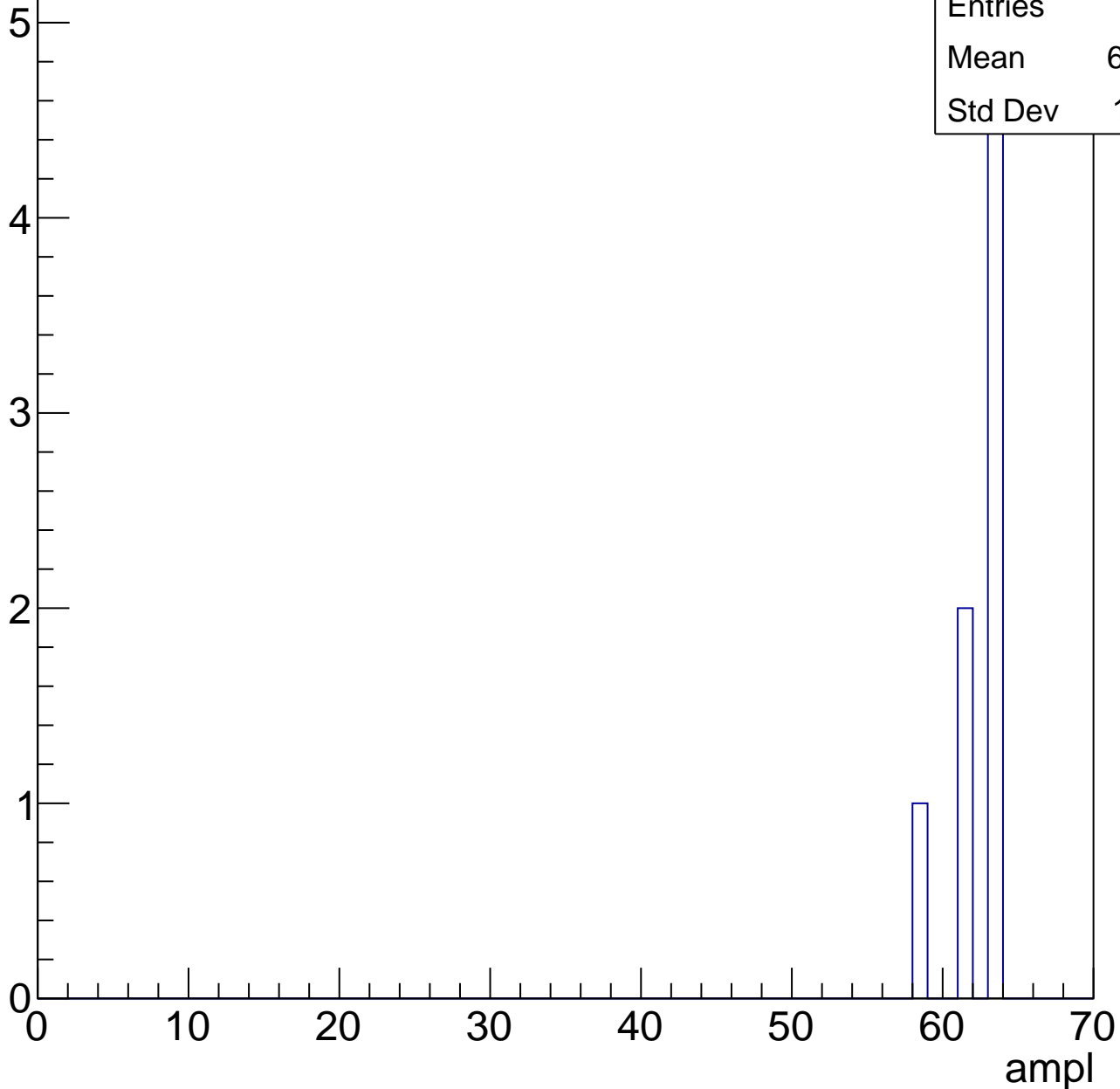


# B0L001S, U2-ch81, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 8     |
| Mean    | 61.88 |
| Std Dev | 1.691 |





# B0L001S, U2-ch81, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U2-ch82, adc0

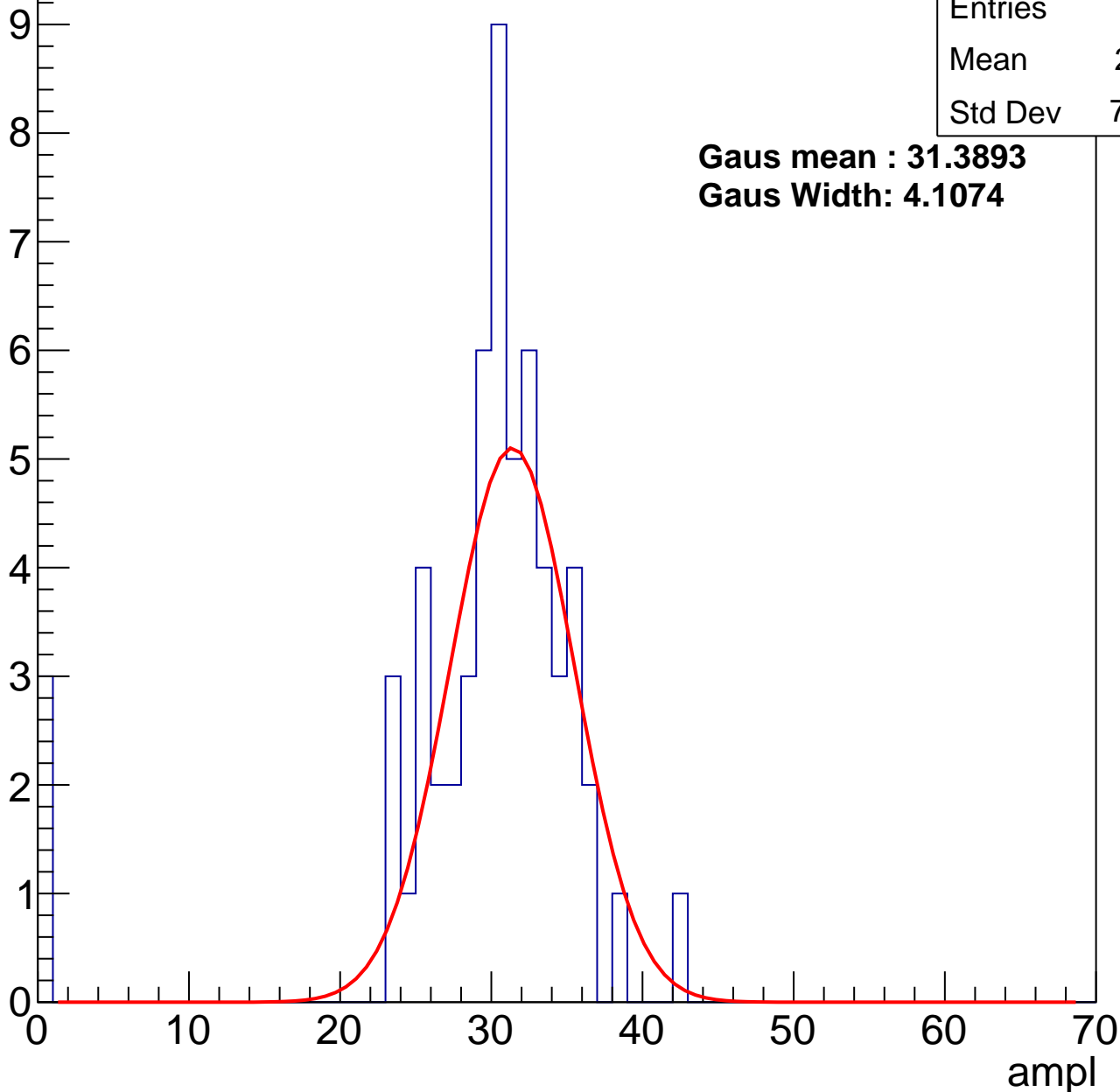
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 59    |
| Mean    | 28.81 |
| Std Dev | 7.659 |

**Gaus mean : 31.3893**

**Gaus Width: 4.1074**



# B0L001S, U2-ch82, adc1

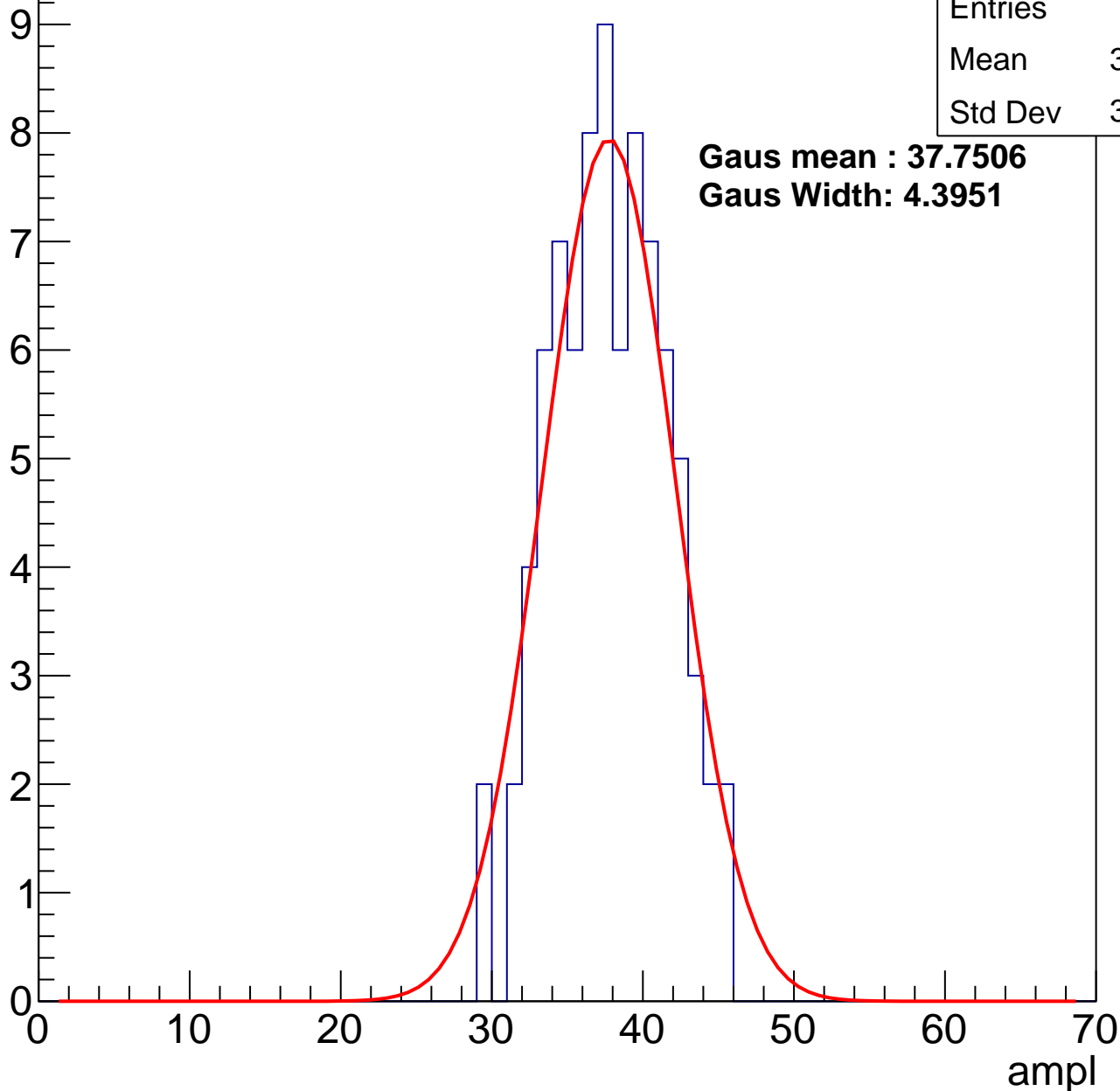
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 83    |
| Mean    | 37.33 |
| Std Dev | 3.703 |

**Gaus mean : 37.7506**

**Gaus Width: 4.3951**



# B0L001S, U2-ch82, adc2

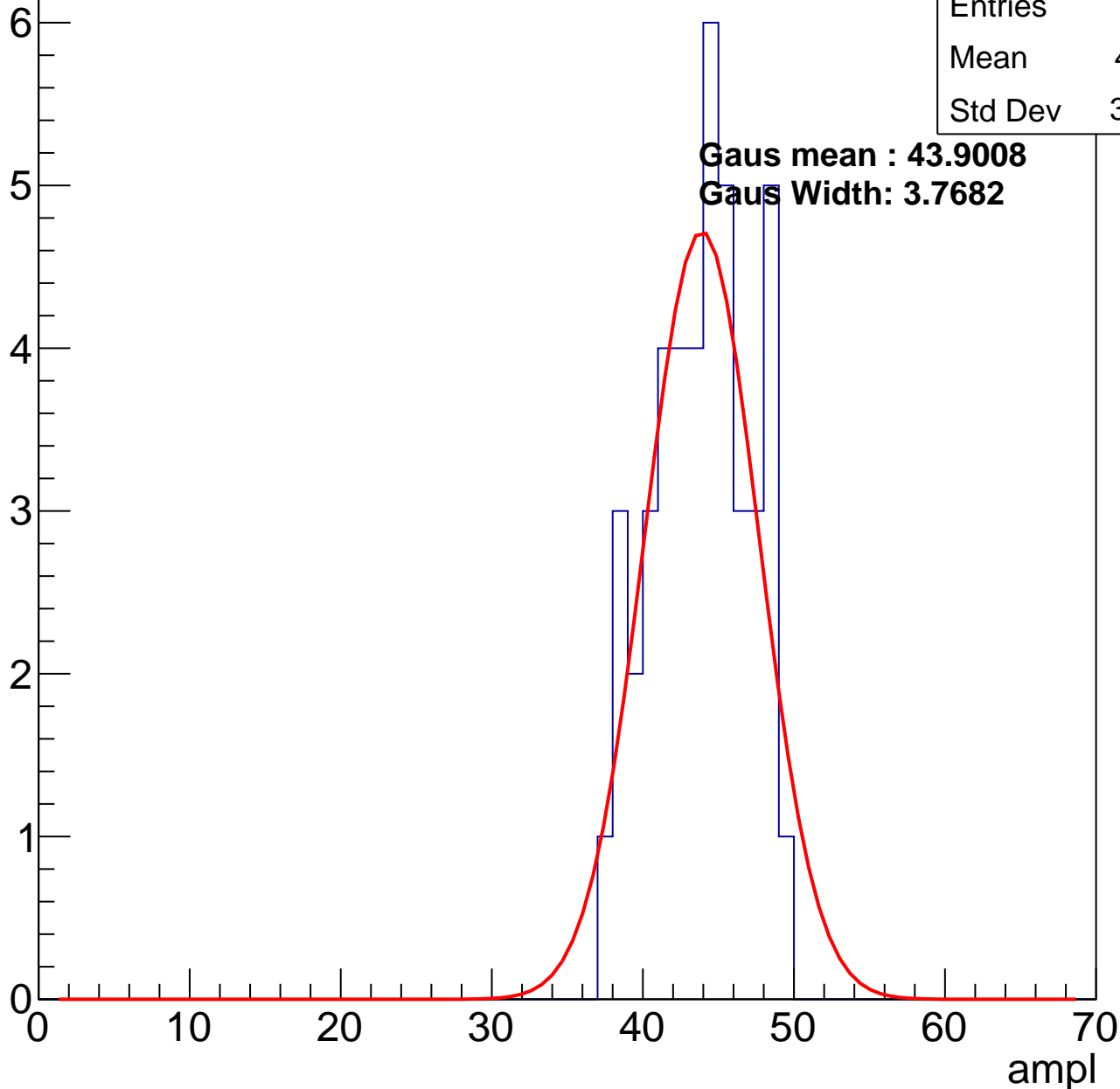
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 44    |
| Mean    | 43.41 |
| Std Dev | 3.179 |

**Gaus mean : 43.9008**

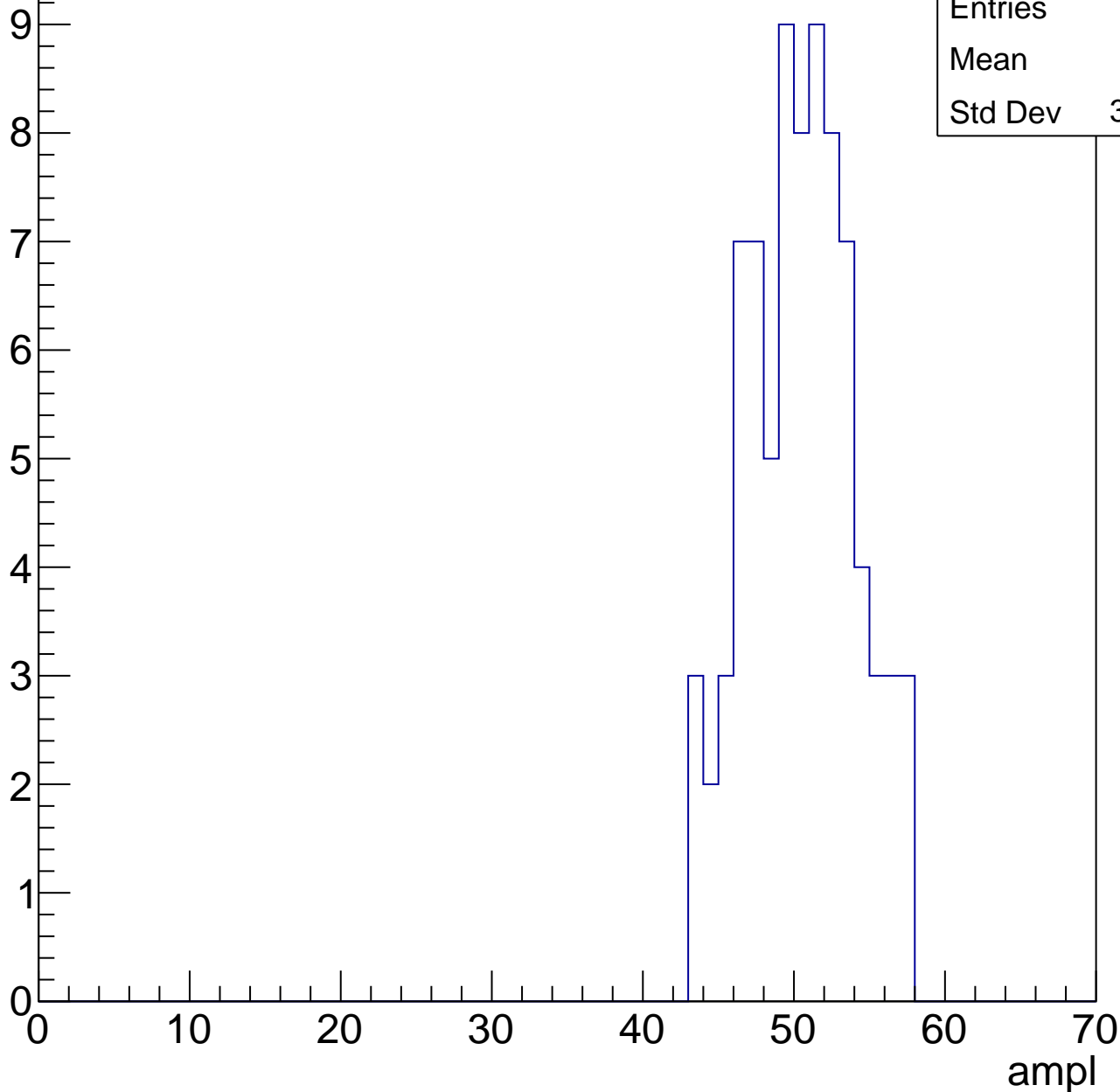
**Gaus Width: 3.7682**



# B0L001S, U2-ch82, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

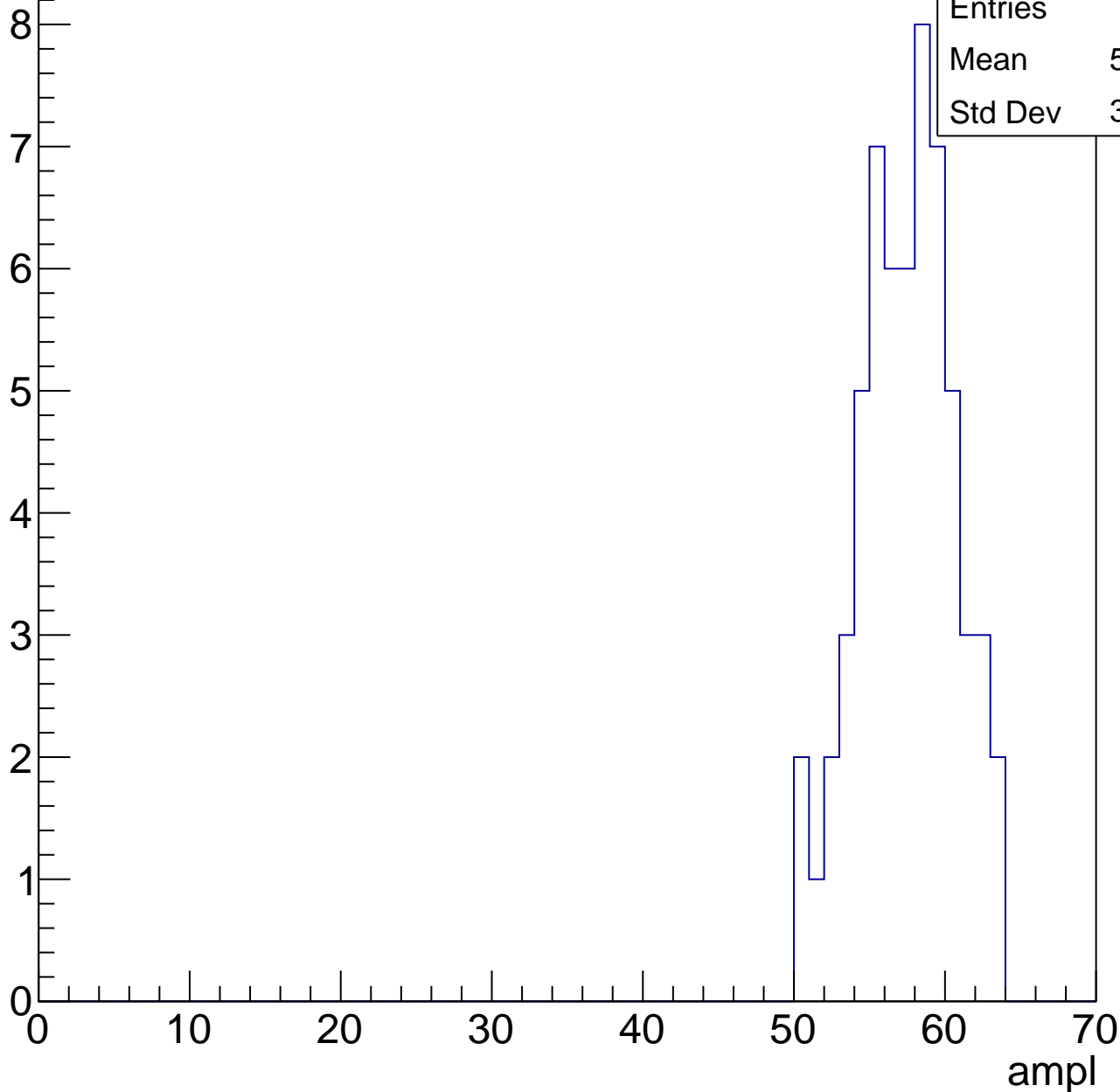


# B0L001S, U2-ch82, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 60    |
| Mean    | 56.98 |
| Std Dev | 3.128 |

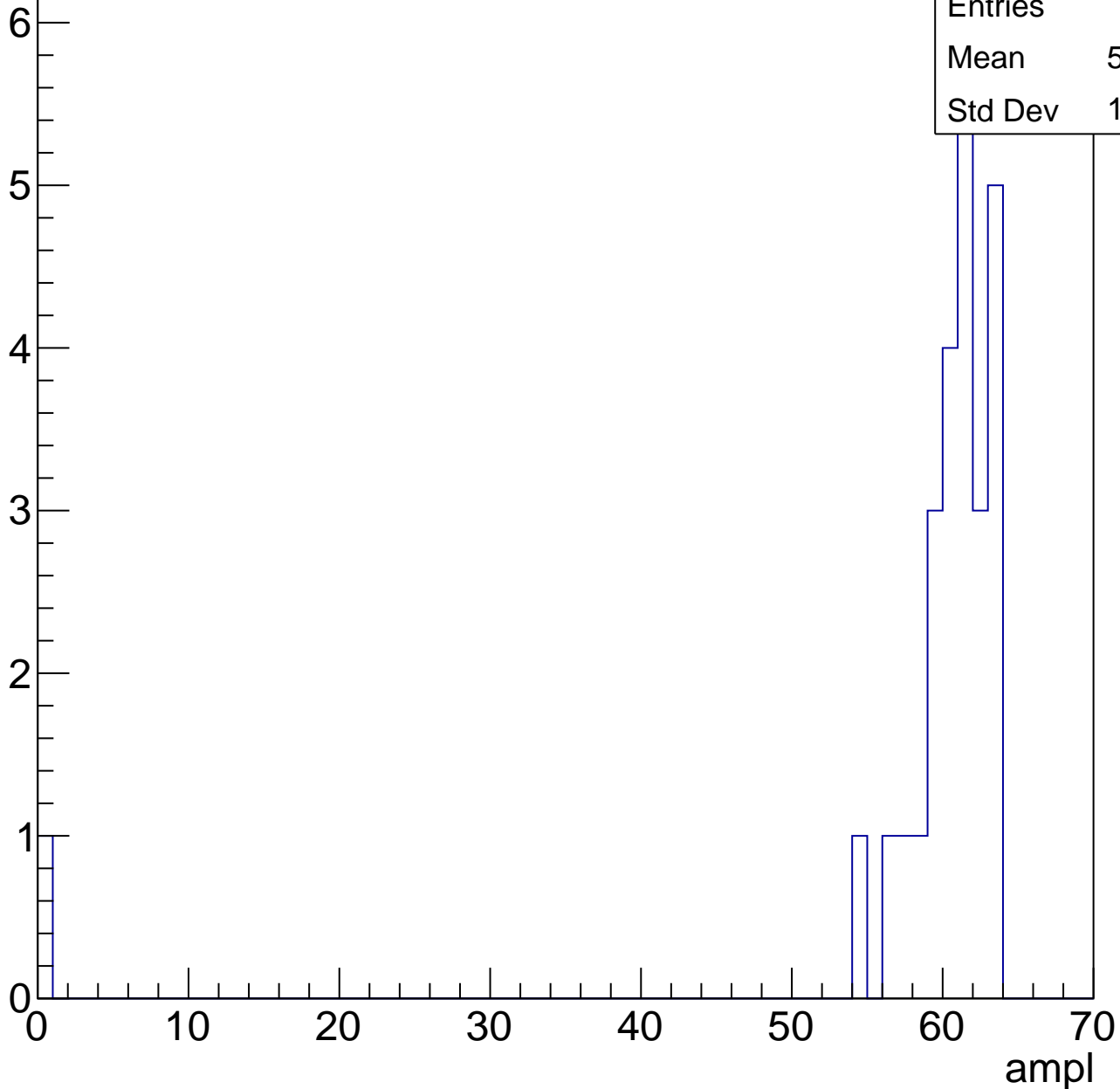


# B0L001S, U2-ch82, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

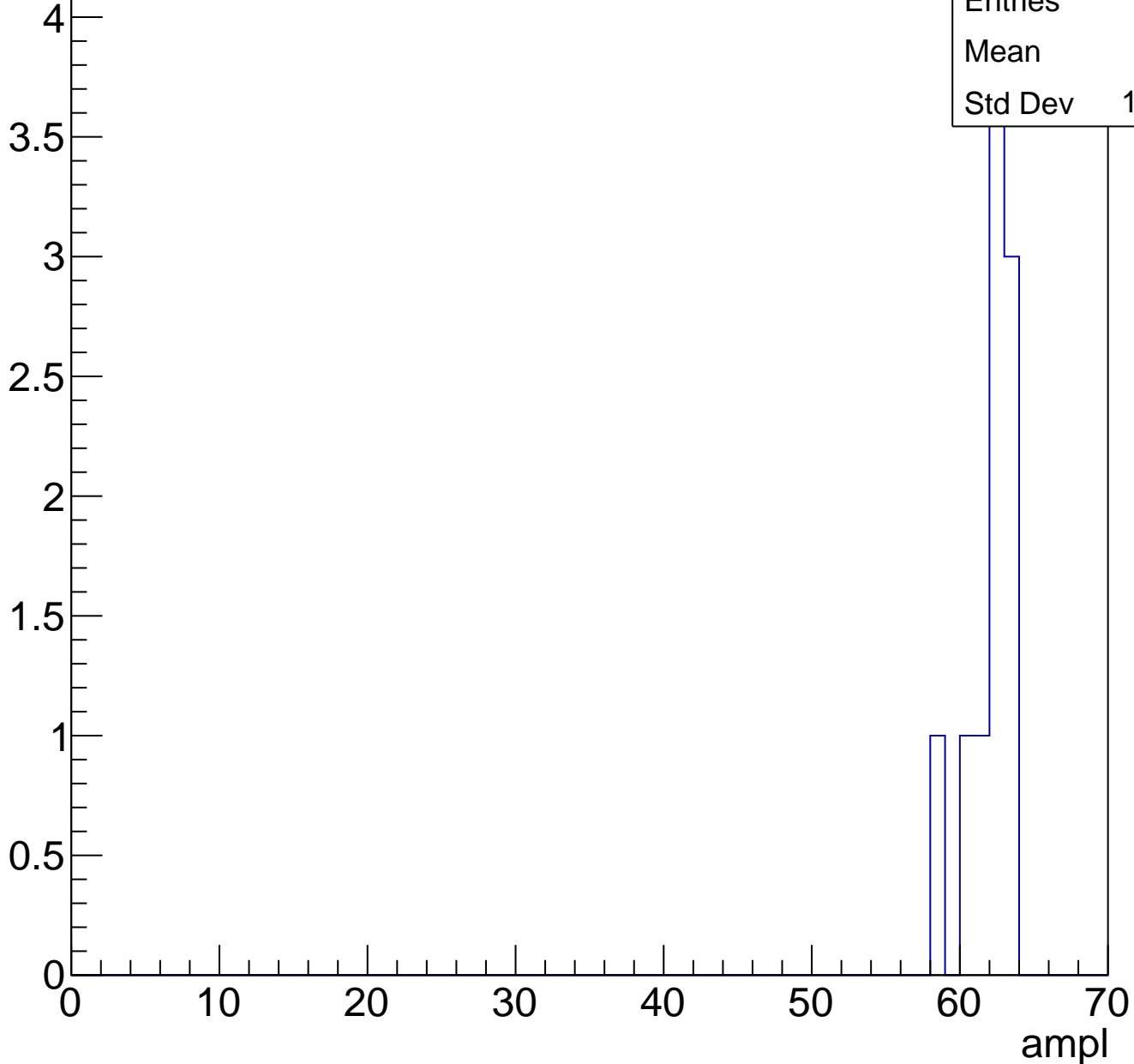
|         |       |
|---------|-------|
| Entries | 26    |
| Mean    | 58.04 |
| Std Dev | 11.82 |



# B0L001S, U2-ch82, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch82, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 0 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch83, adc0

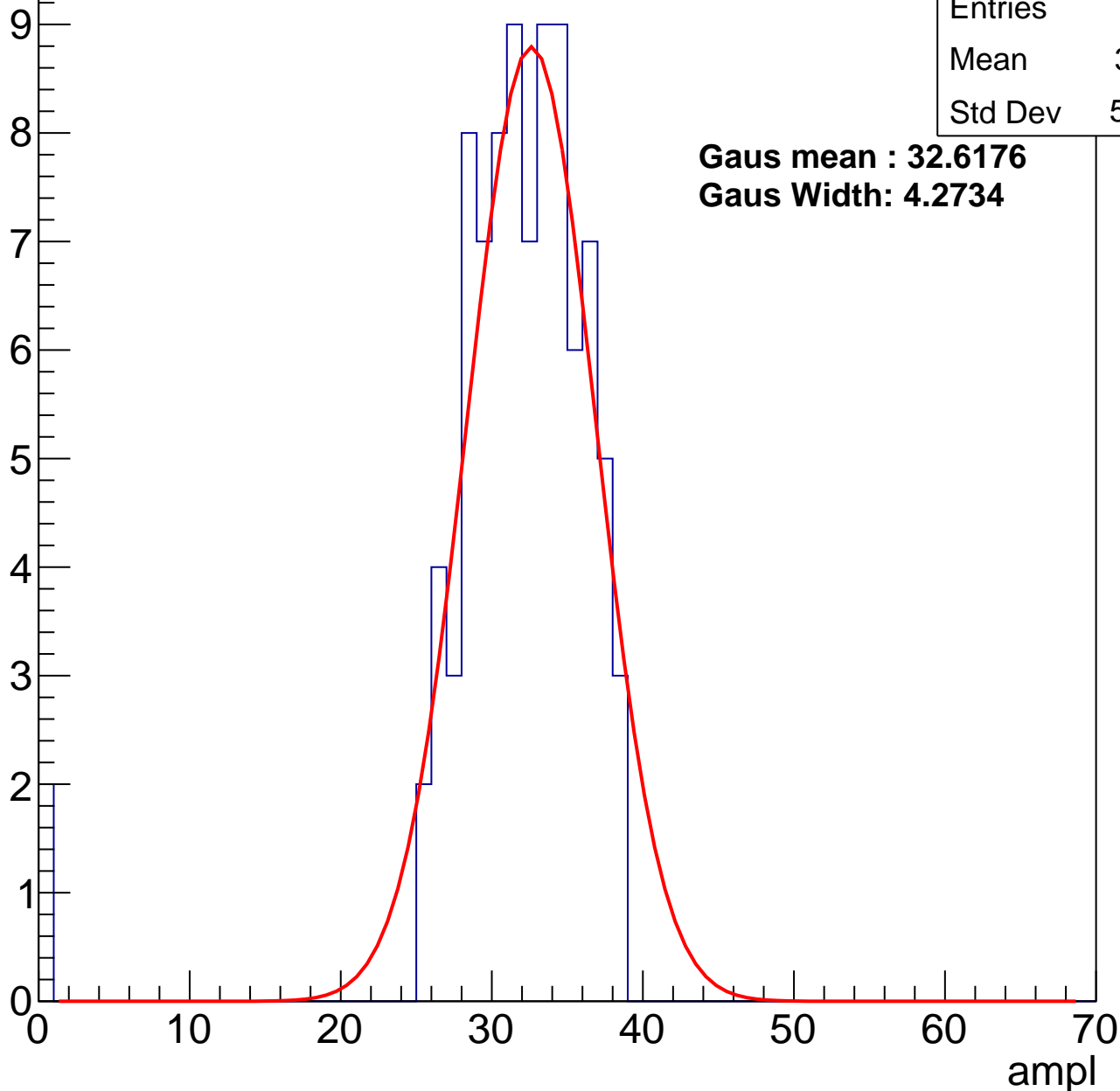
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 89    |
| Mean    | 31.11 |
| Std Dev | 5.778 |

**Gaus mean : 32.6176**

**Gaus Width: 4.2734**



# B0L001S, U2-ch83, adc1

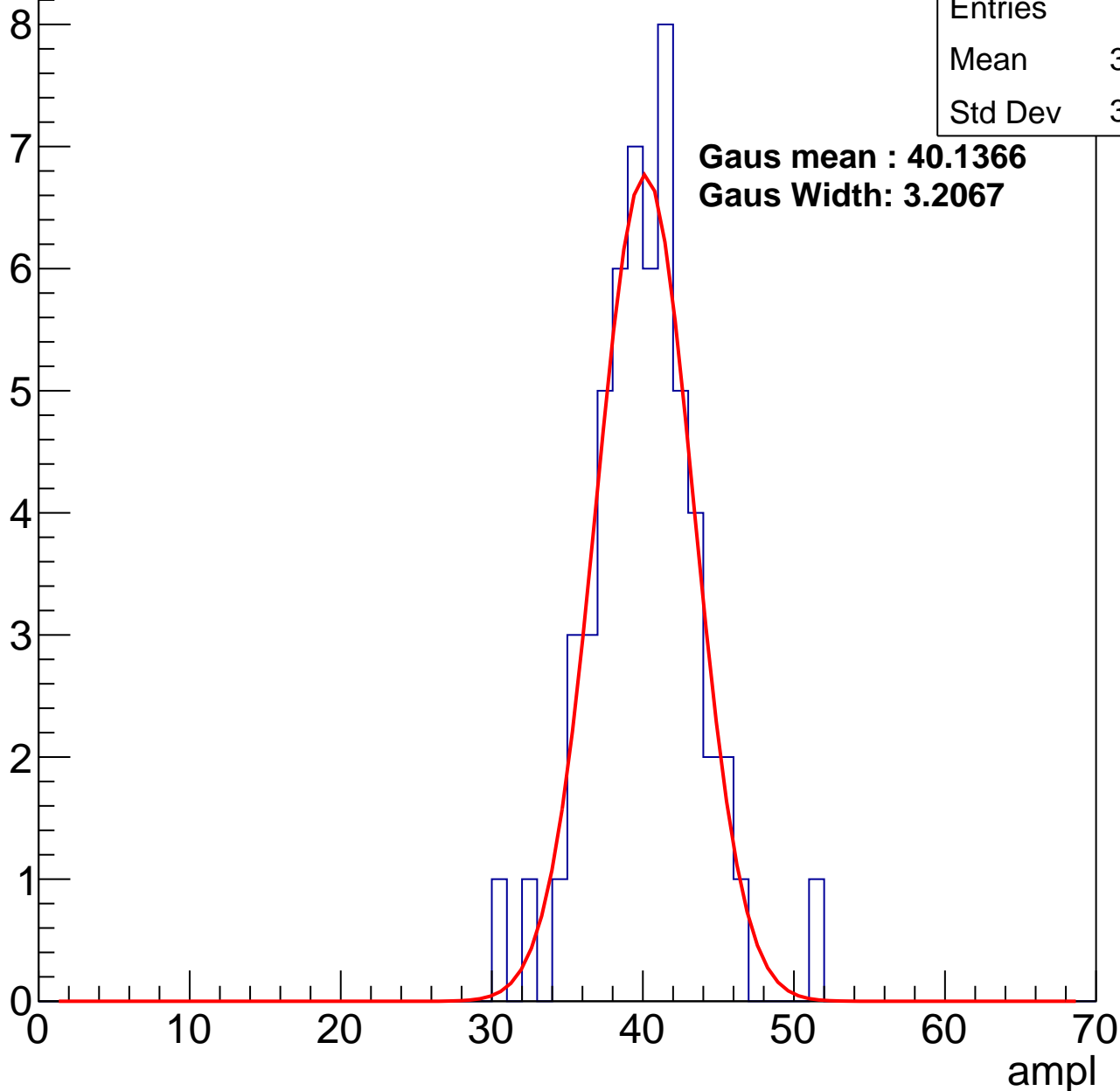
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 56    |
| Mean    | 39.64 |
| Std Dev | 3.523 |

**Gaus mean : 40.1366**

**Gaus Width: 3.2067**



# B0L001S, U2-ch83, adc2

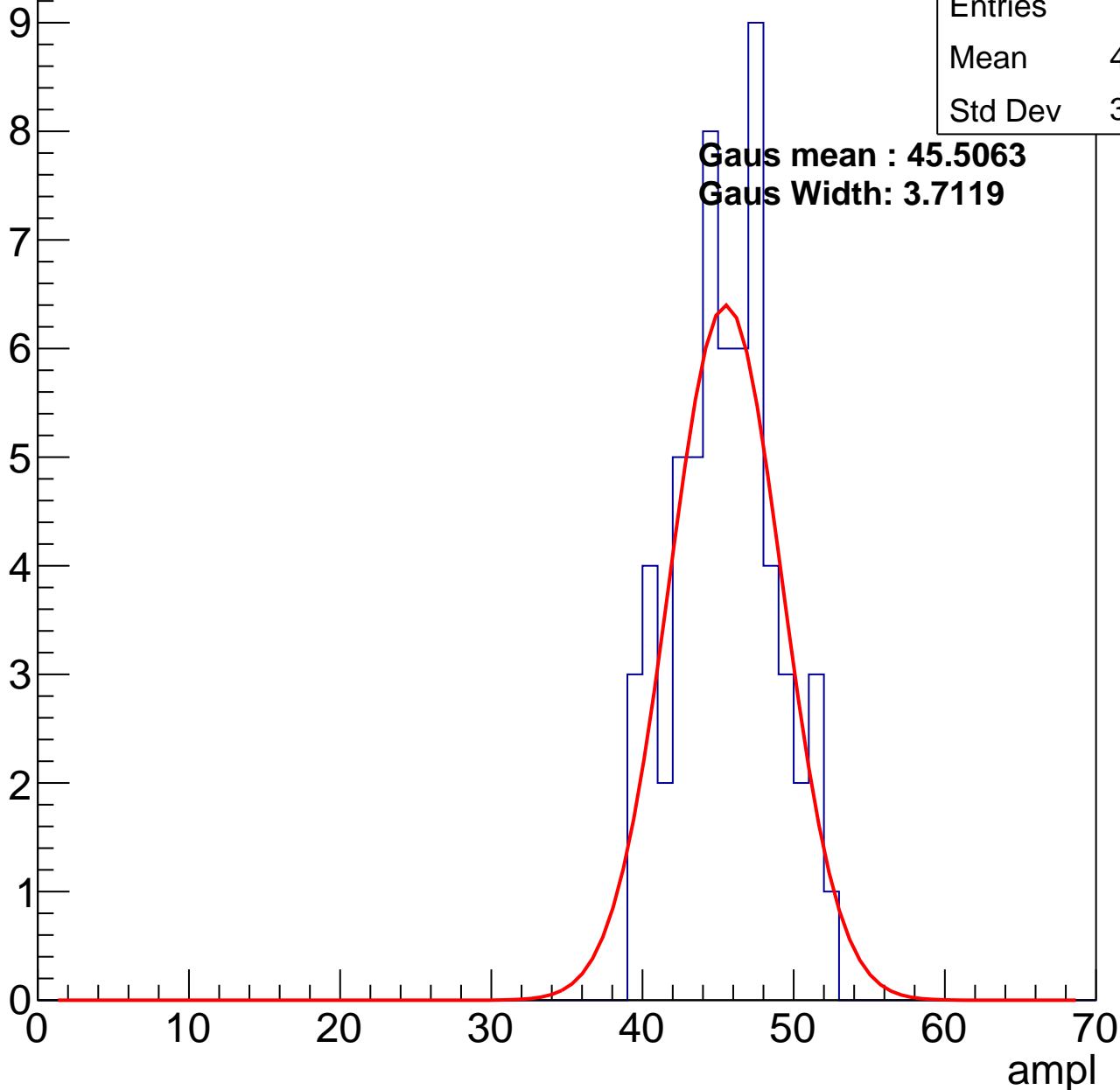
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 61    |
| Mean    | 45.07 |
| Std Dev | 3.254 |

**Gaus mean : 45.5063**

**Gaus Width: 3.7119**

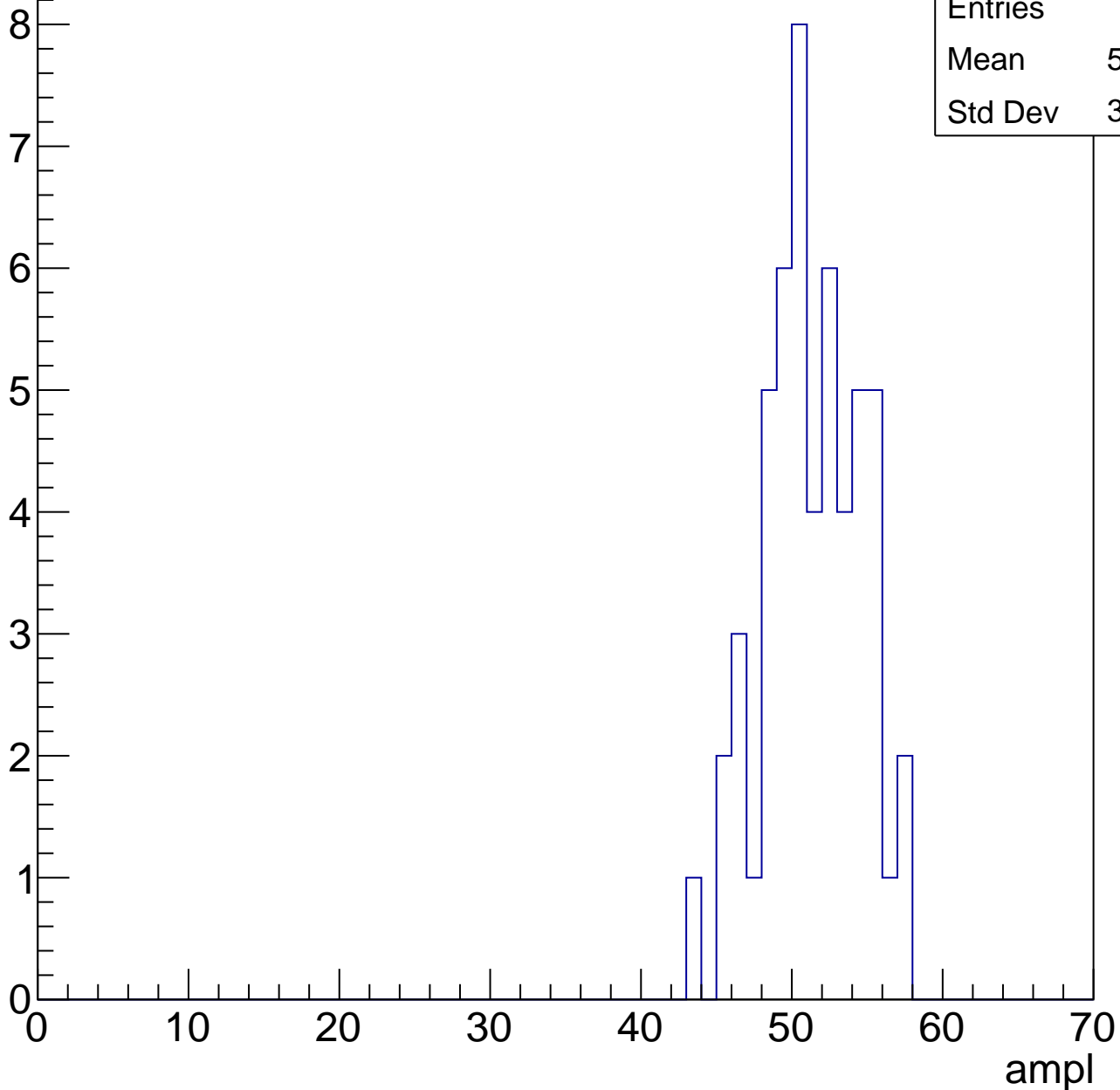


# B0L001S, U2-ch83, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

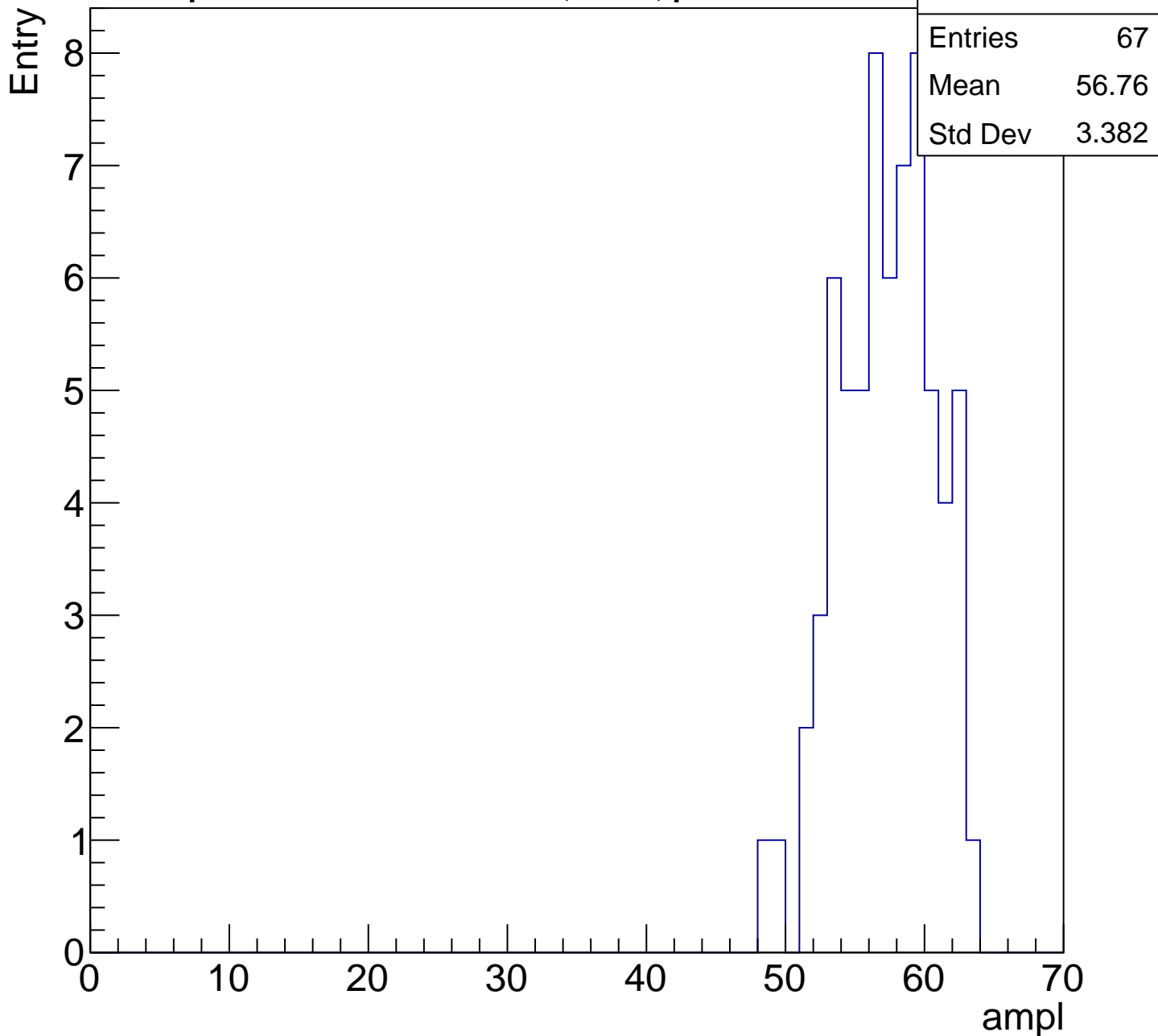
Entry

|         |       |
|---------|-------|
| Entries | 53    |
| Mean    | 50.85 |
| Std Dev | 3.212 |



# B0L001S, U2-ch83, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

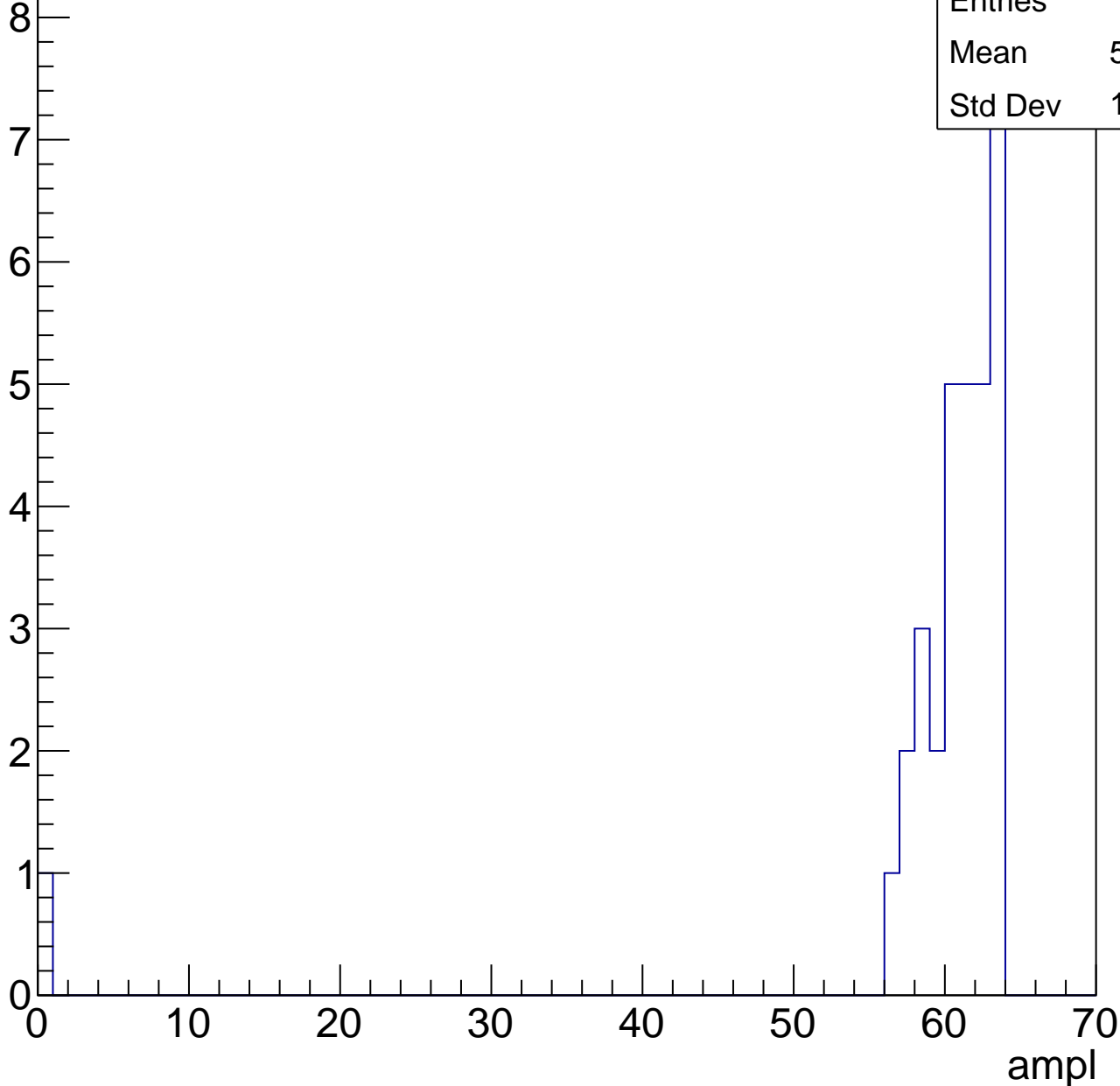


# B0L001S, U2-ch83, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

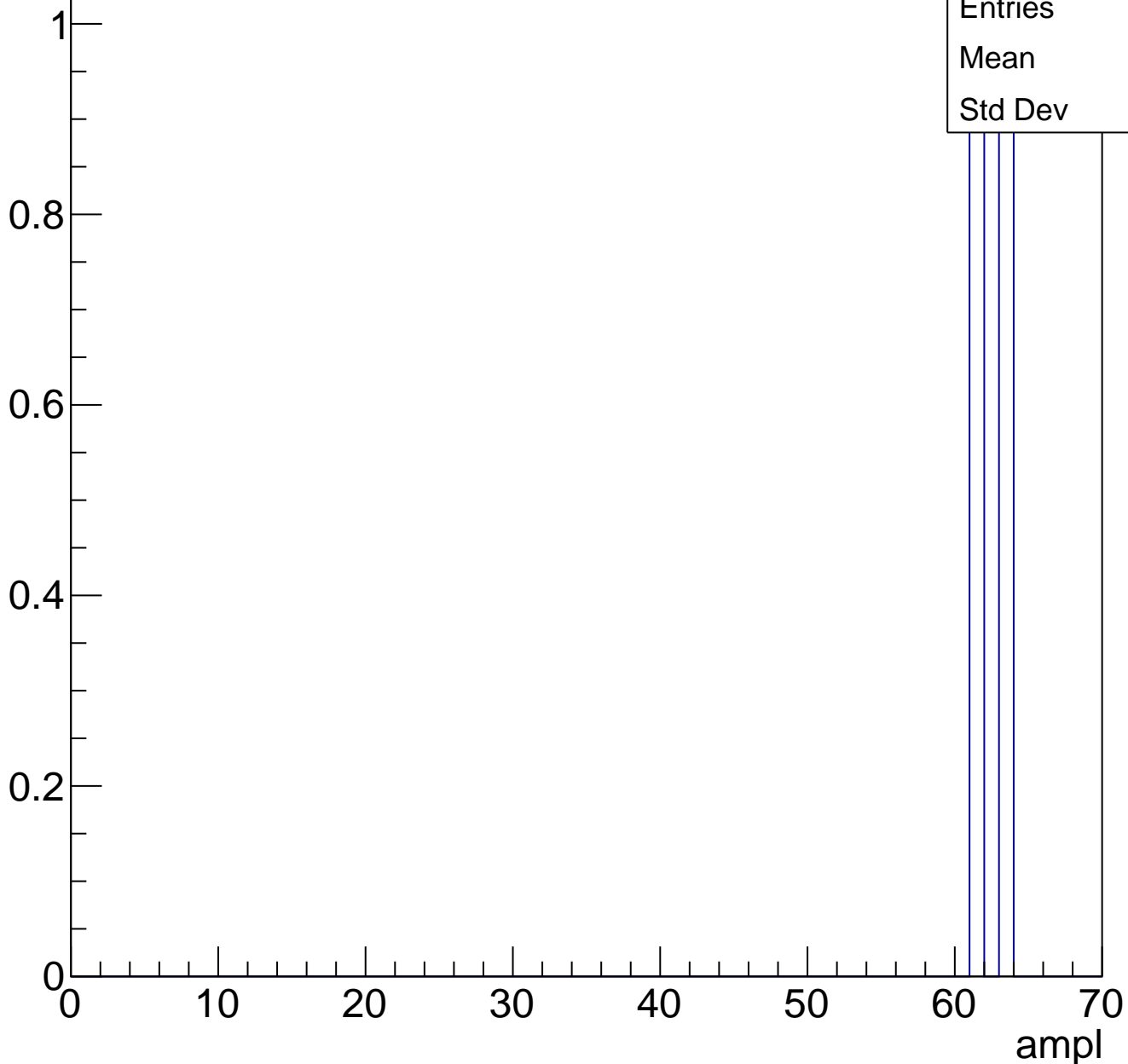
|         |       |
|---------|-------|
| Entries | 32    |
| Mean    | 58.78 |
| Std Dev | 10.75 |



# B0L001S, U2-ch83, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch83, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 0 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch84, adc0

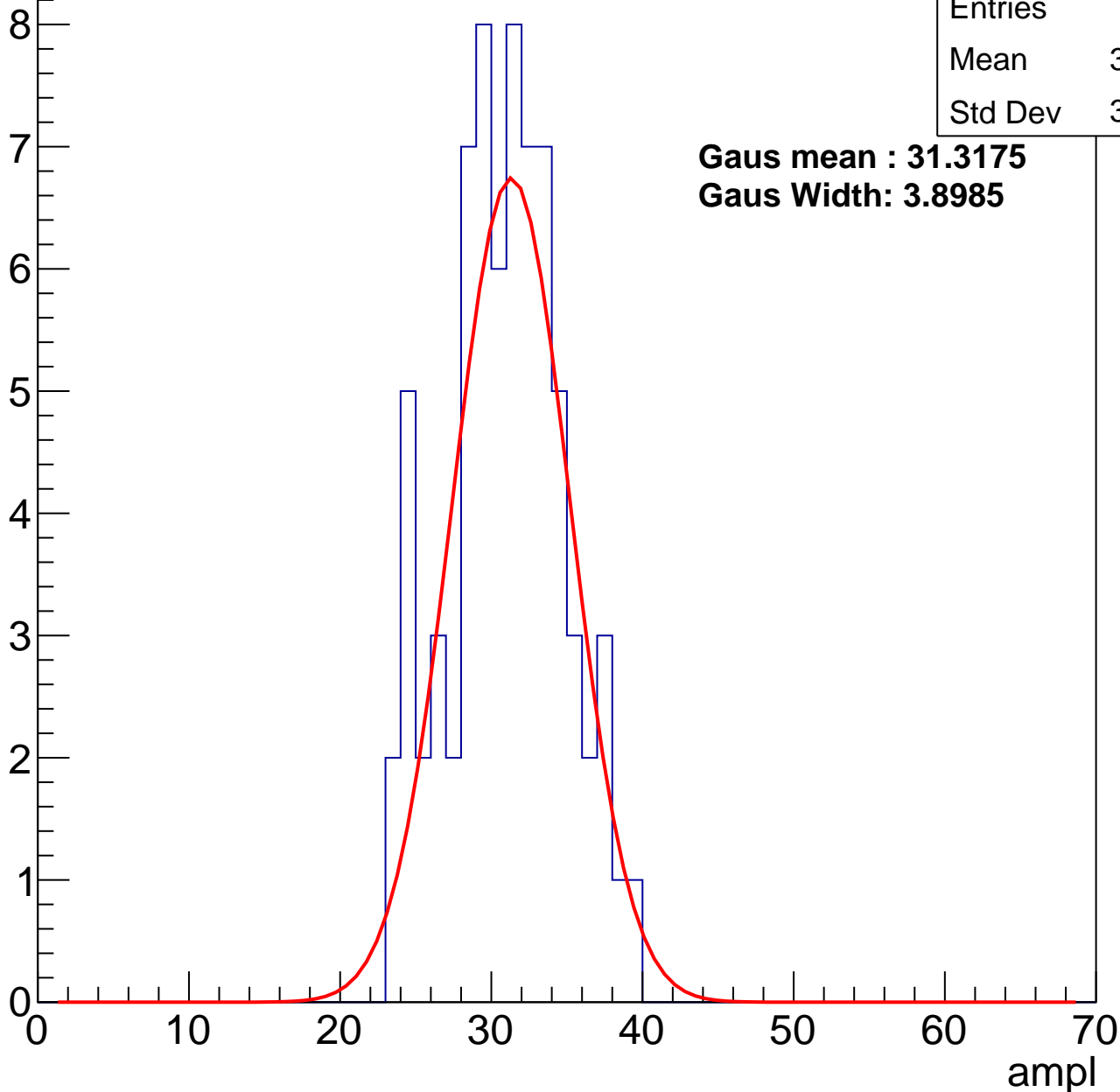
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 72    |
| Mean    | 30.47 |
| Std Dev | 3.786 |

**Gaus mean : 31.3175**

**Gaus Width: 3.8985**



# B0L001S, U2-ch84, adc1

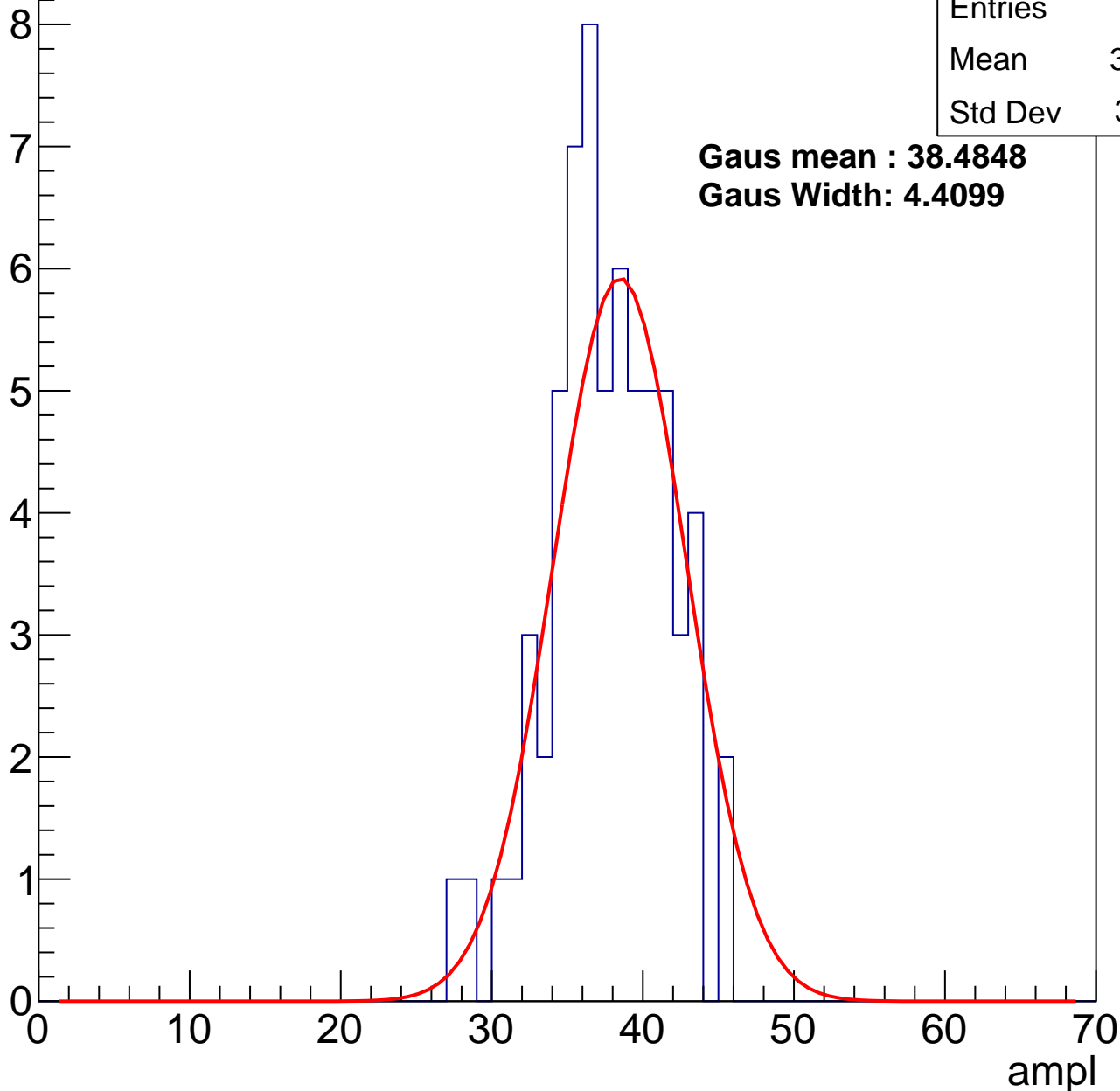
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 64    |
| Mean    | 37.22 |
| Std Dev | 3.851 |

**Gaus mean : 38.4848**

**Gaus Width: 4.4099**



# B0L001S, U2-ch84, adc2

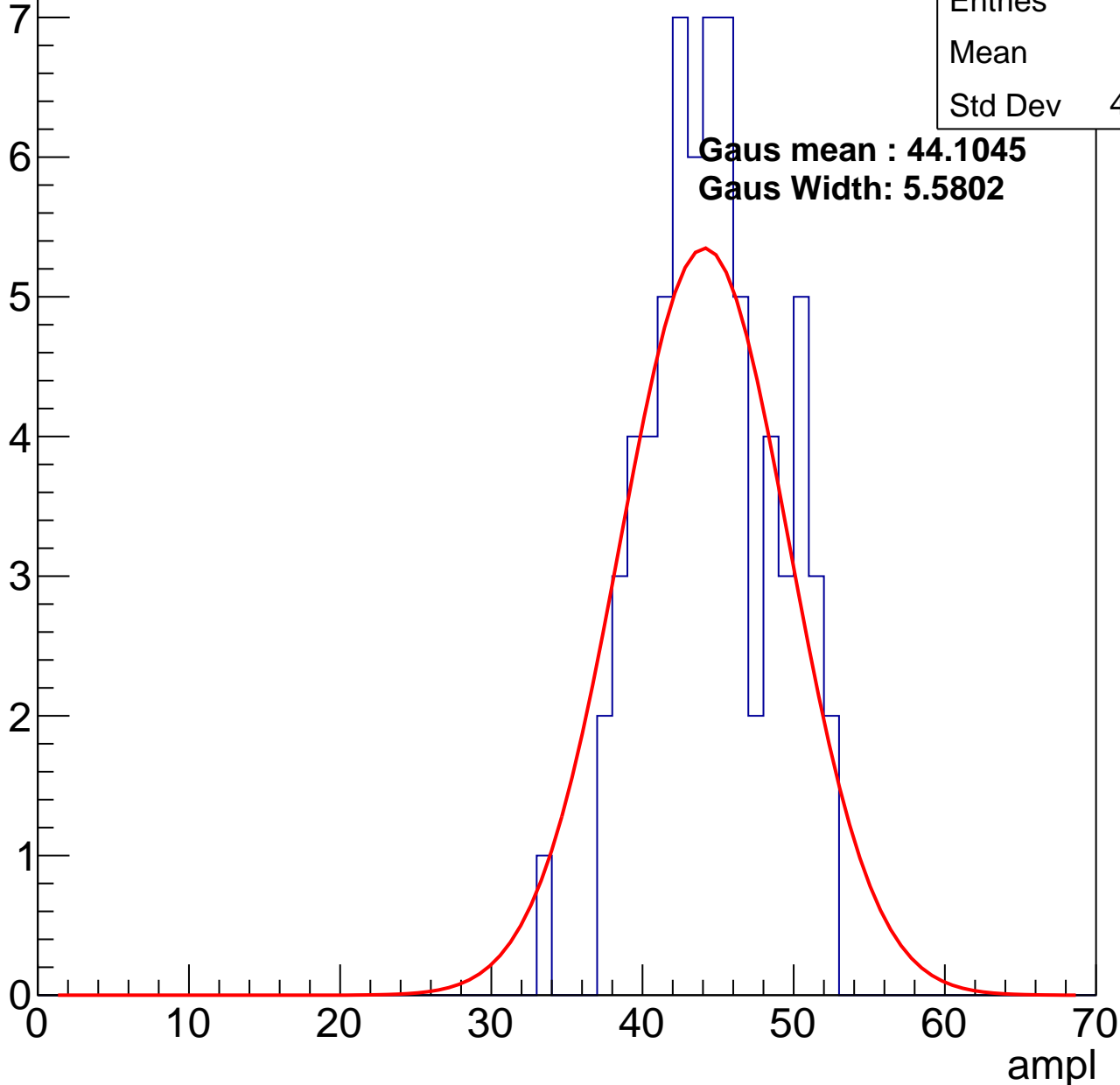
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 70    |
| Mean    | 44.1  |
| Std Dev | 4.155 |

**Gaus mean : 44.1045**

**Gaus Width: 5.5802**

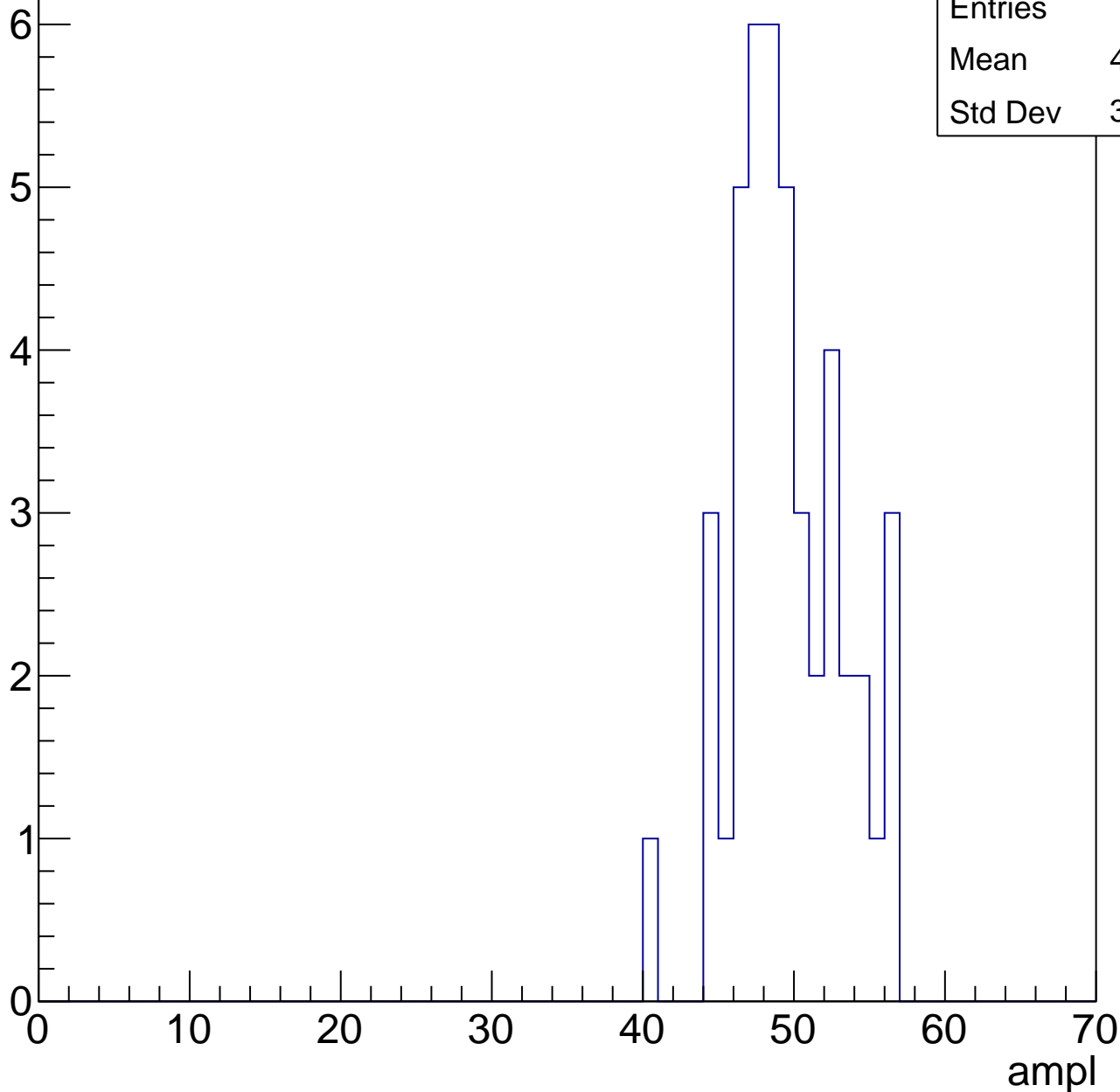


# B0L001S, U2-ch84, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

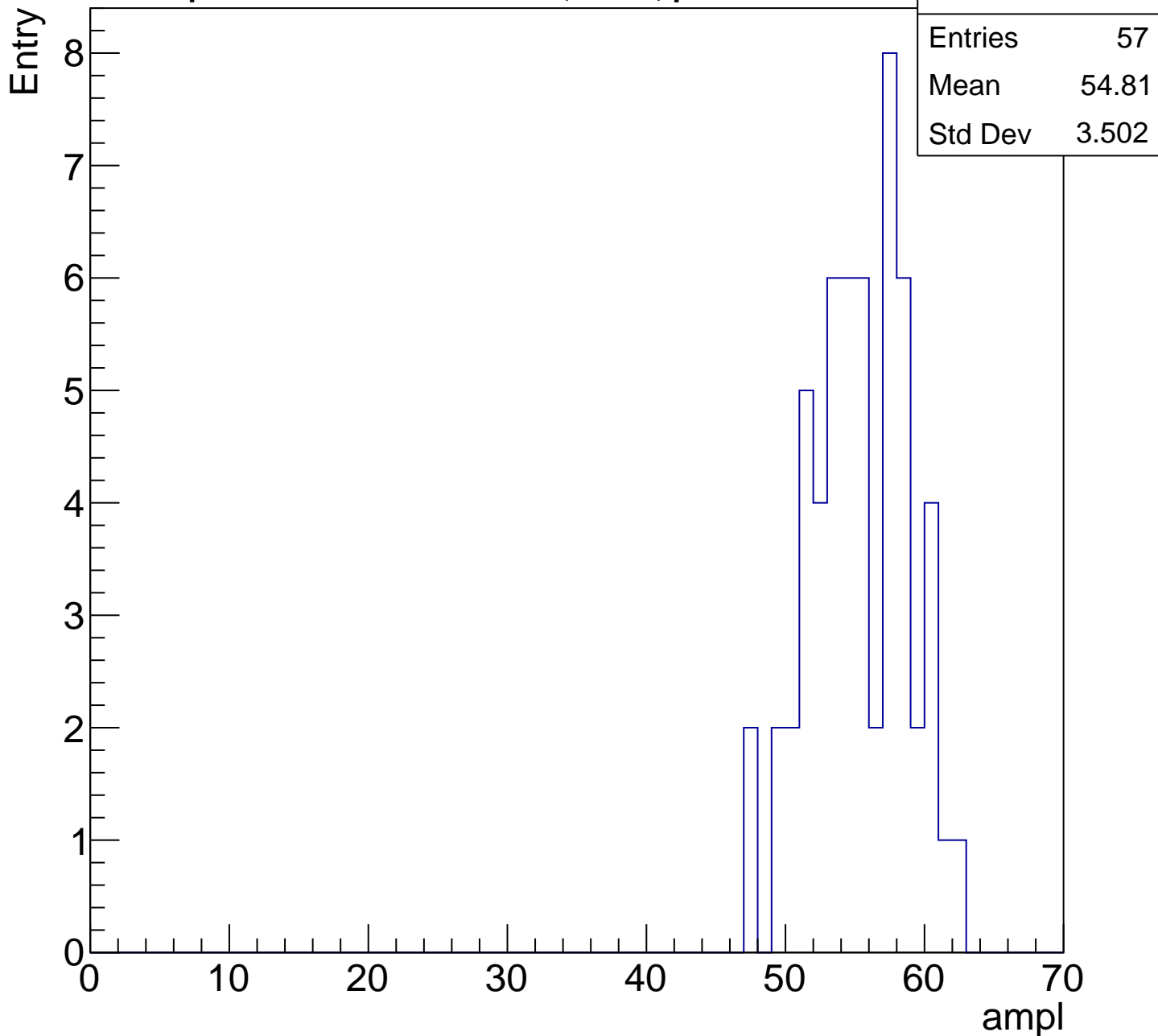
Entry

|         |       |
|---------|-------|
| Entries | 44    |
| Mean    | 49.07 |
| Std Dev | 3.564 |



# B0L001S, U2-ch84, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U2-ch84, adc5

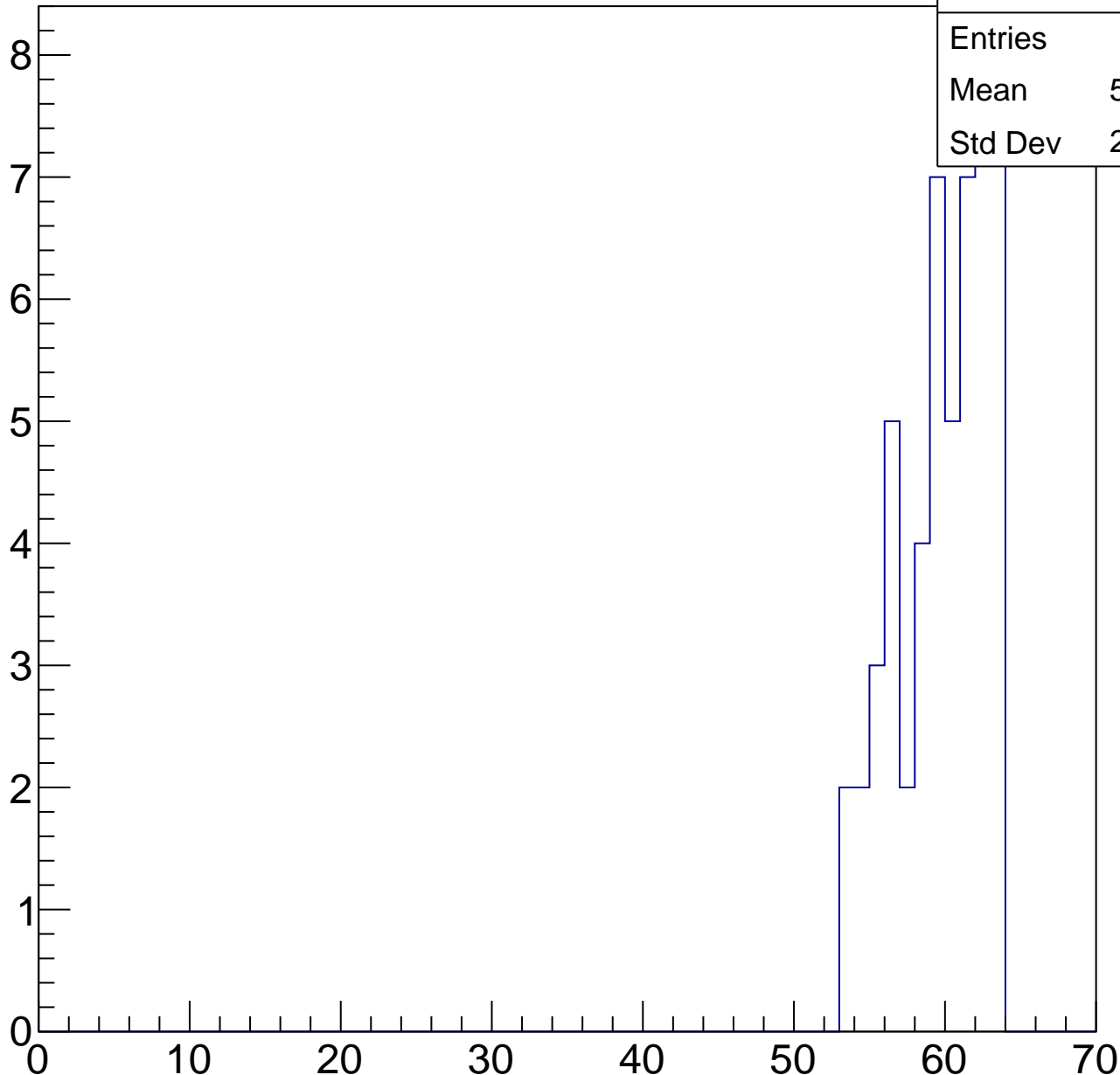
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

|         |       |
|---------|-------|
| Entries | 53    |
| Mean    | 59.34 |
| Std Dev | 2.926 |

ampl



# B0L001S, U2-ch84, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

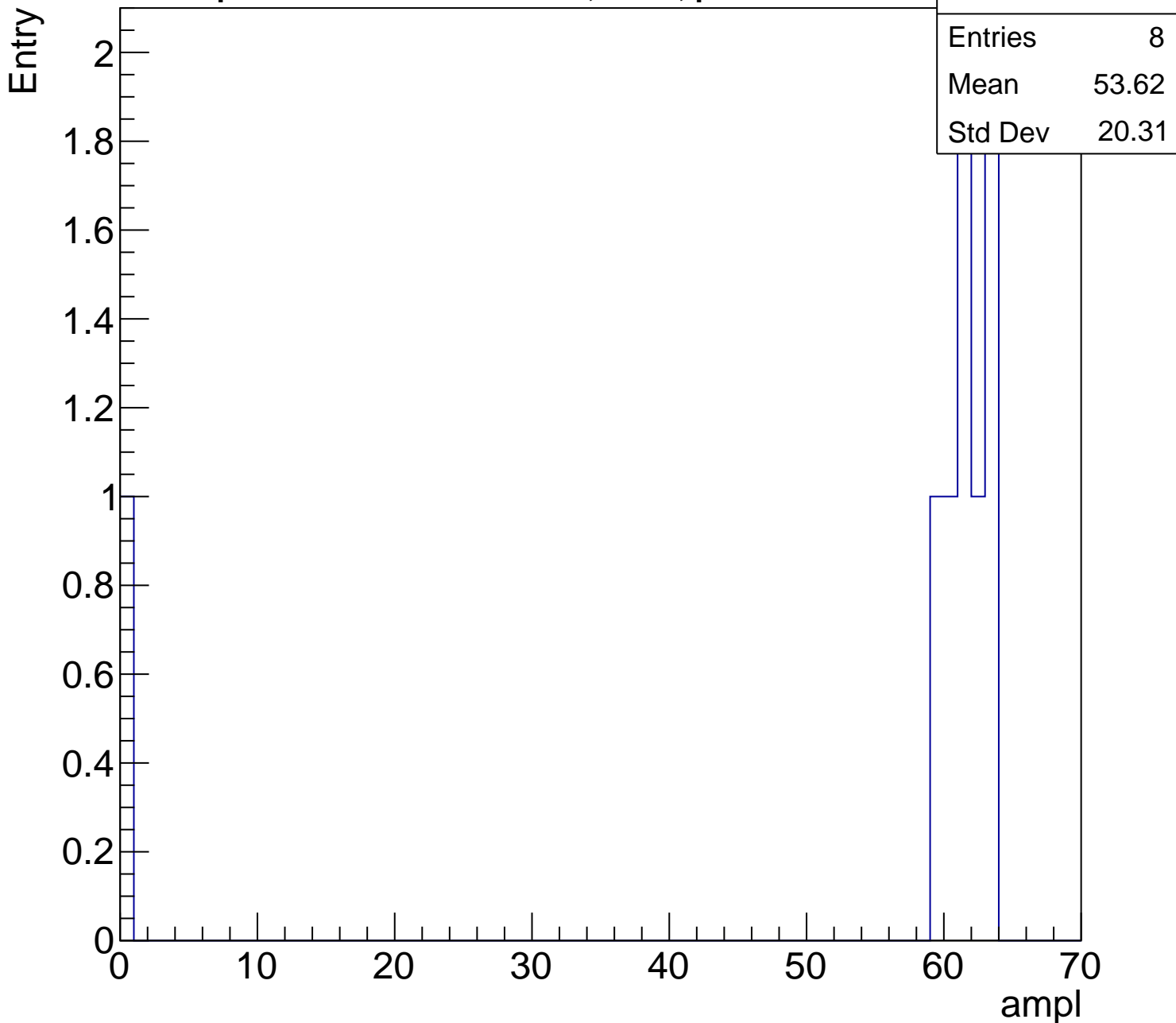
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

|         |       |
|---------|-------|
| Entries | 8     |
| Mean    | 53.62 |
| Std Dev | 20.31 |

ampl

0 10 20 30 40 50 60 70





# B0L001S, U2-ch84, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 1 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch85, adc0

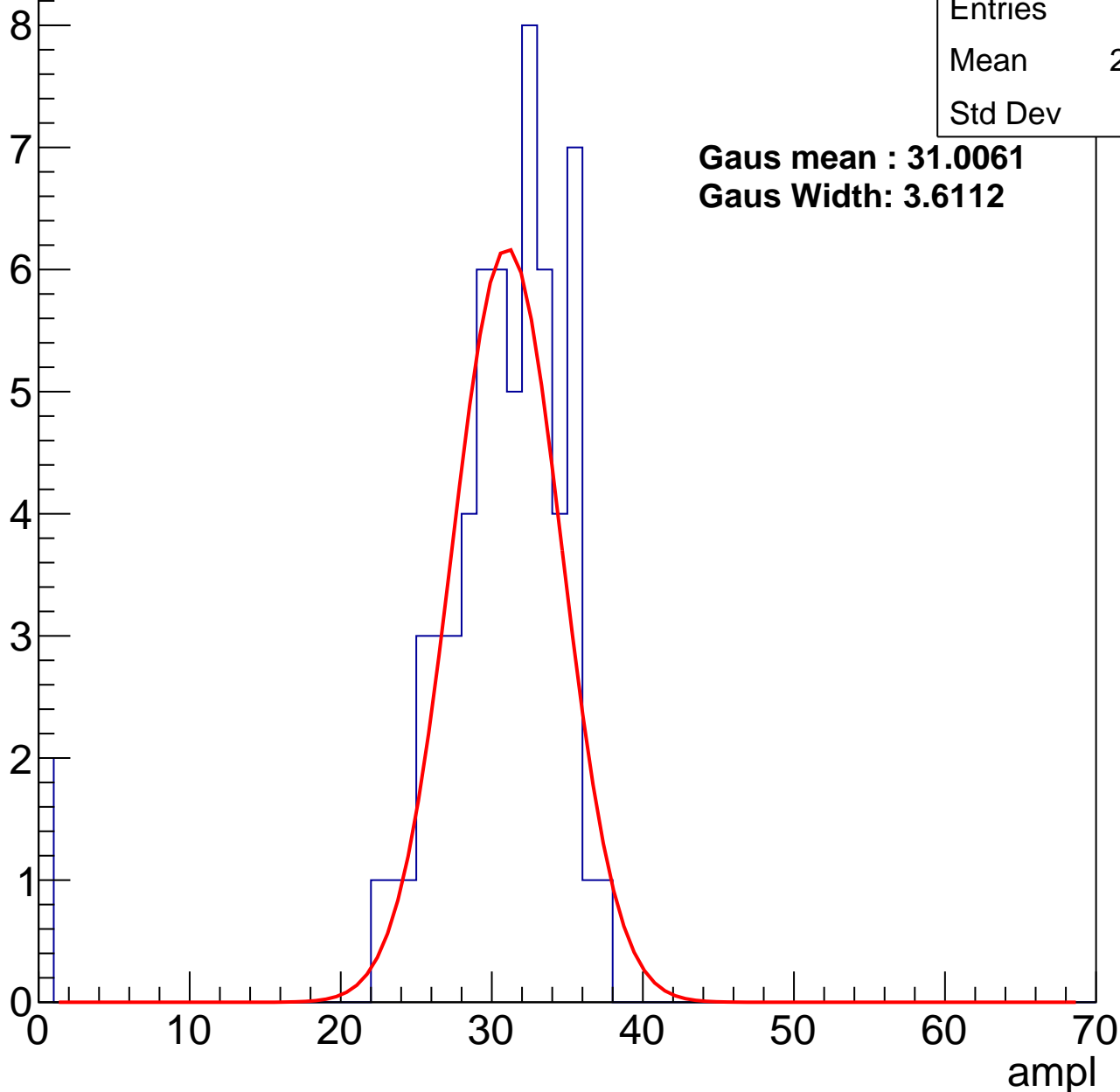
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 62    |
| Mean    | 29.55 |
| Std Dev | 6.38  |

**Gaus mean : 31.0061**

**Gaus Width: 3.6112**



# B0L001S, U2-ch85, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 79    |
| Mean    | 37.91 |
| Std Dev | 3.53  |

**Gaus mean : 38.7764**

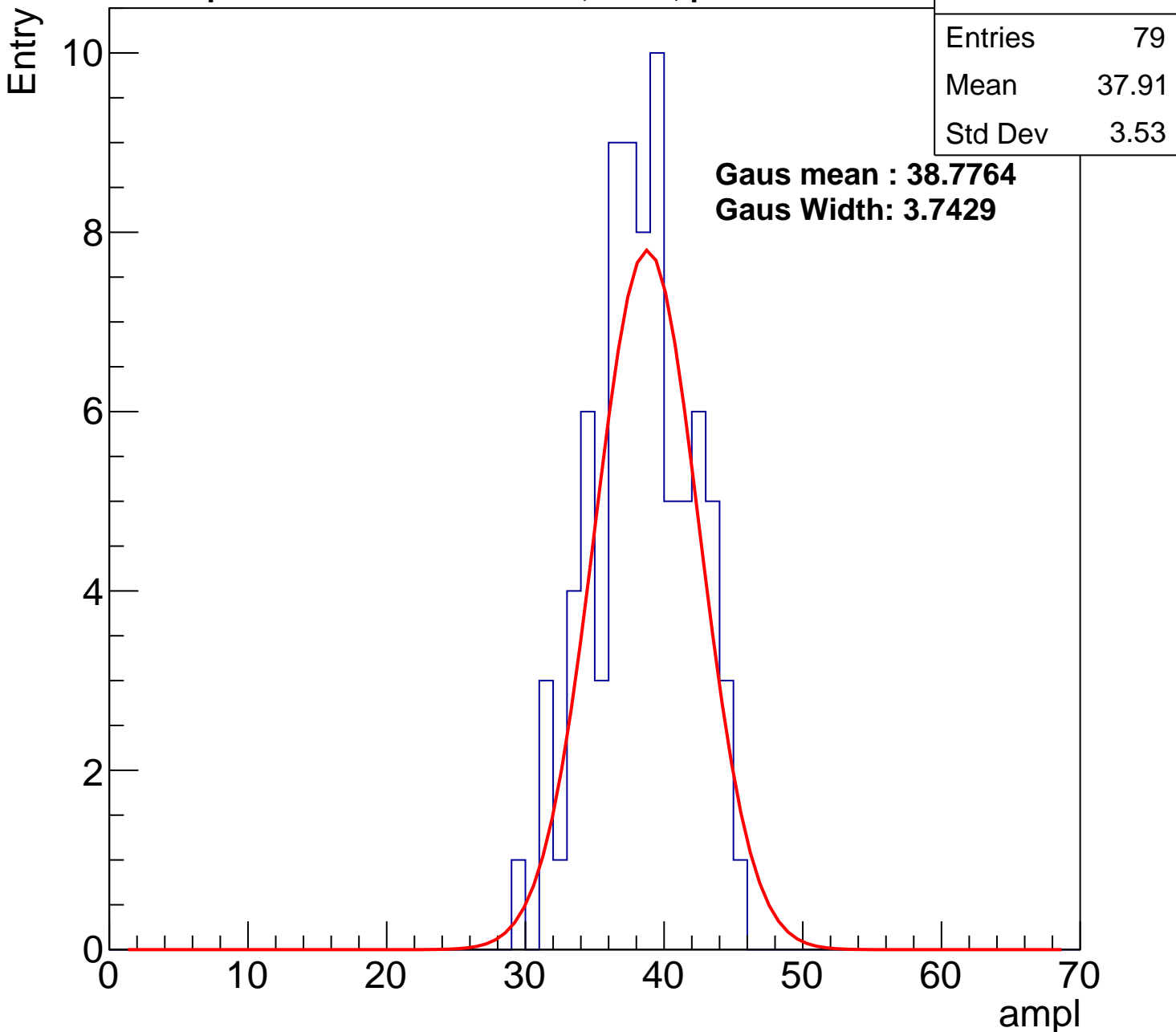
**Gaus Width: 3.7429**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B0L001S, U2-ch85, adc2

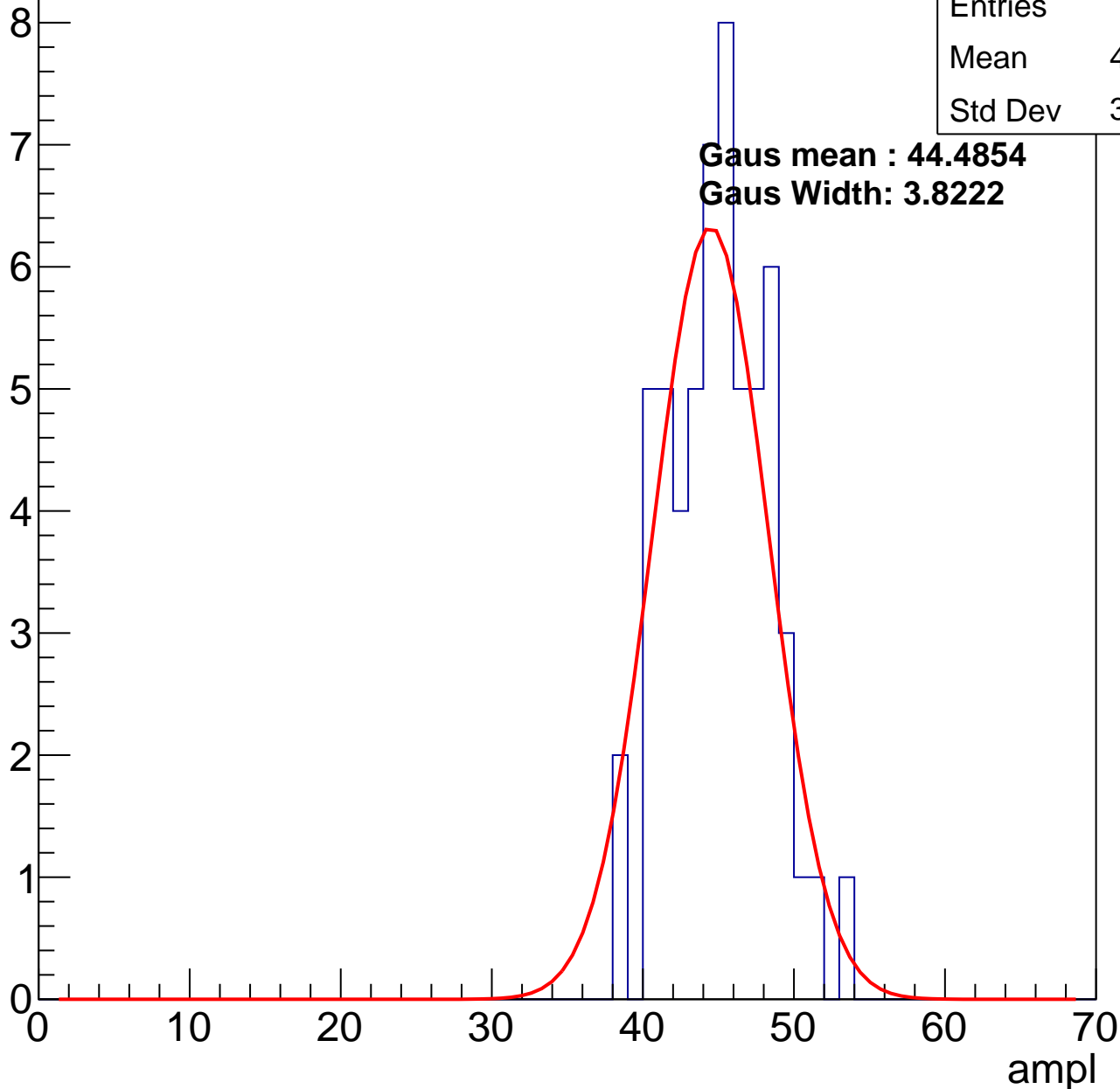
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 58    |
| Mean    | 44.59 |
| Std Dev | 3.238 |

**Gaus mean : 44.4854**

**Gaus Width: 3.8222**

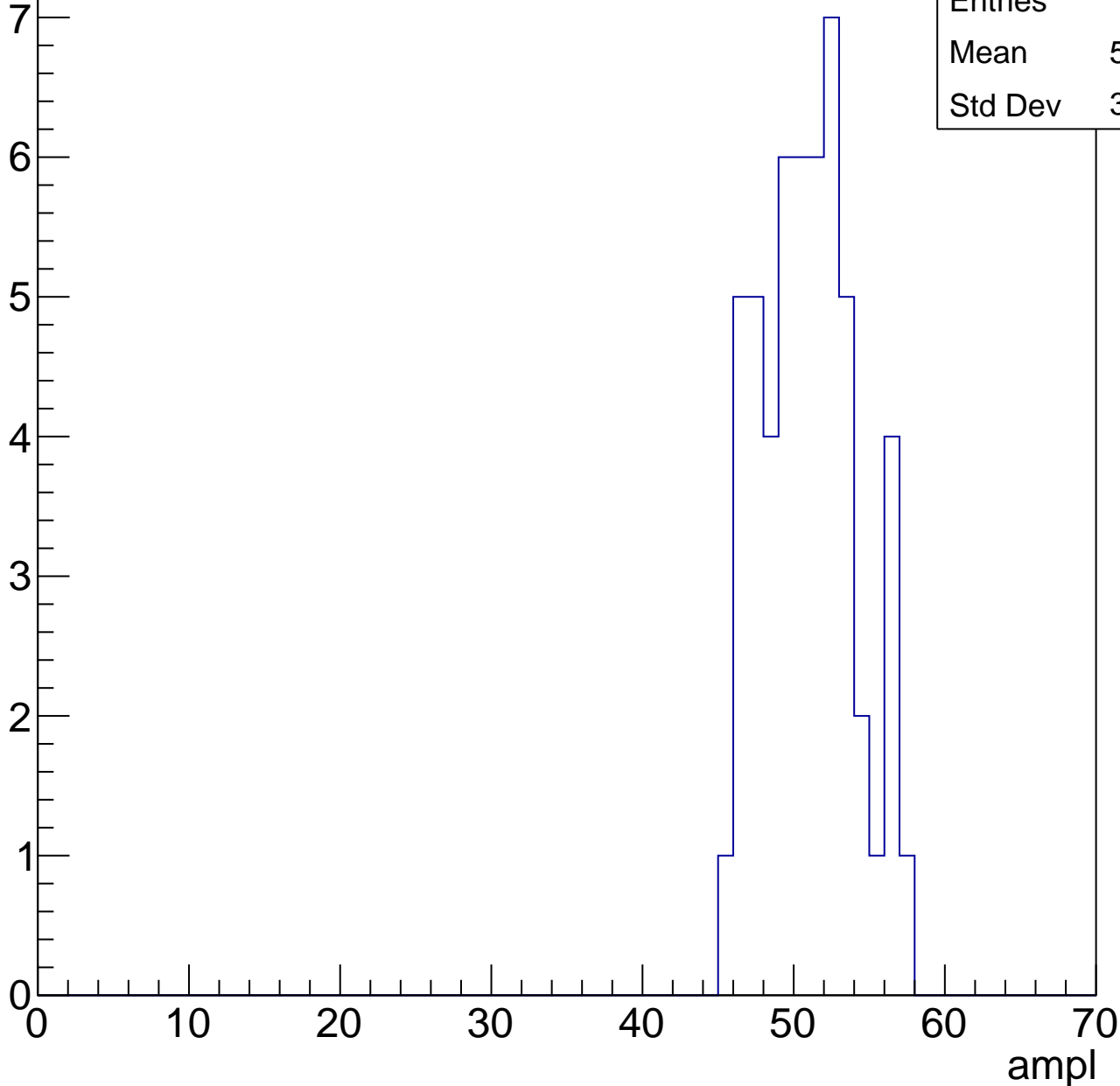


# B0L001S, U2-ch85, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

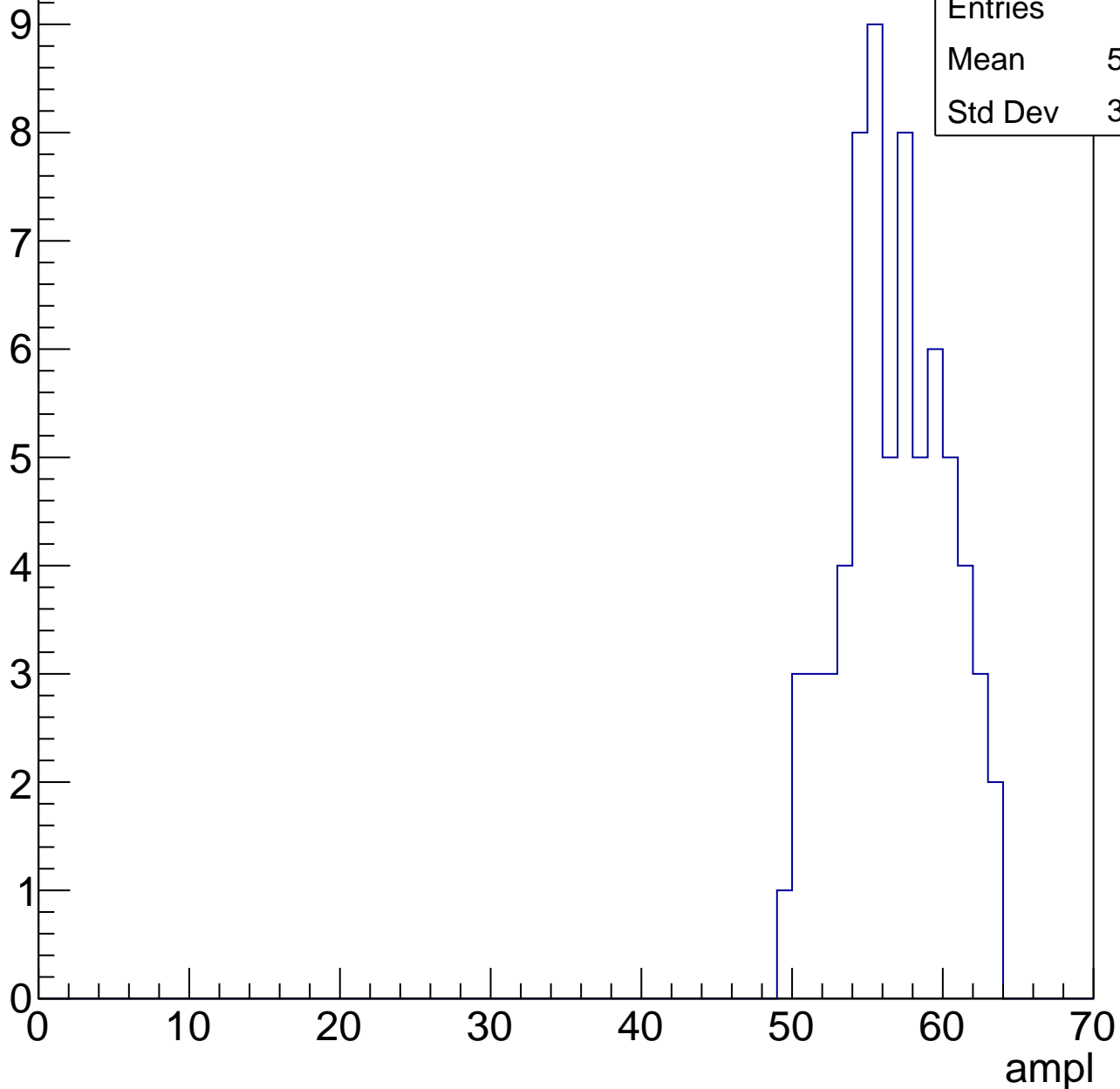
|         |       |
|---------|-------|
| Entries | 53    |
| Mean    | 50.47 |
| Std Dev | 3.038 |



# B0L001S, U2-ch85, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



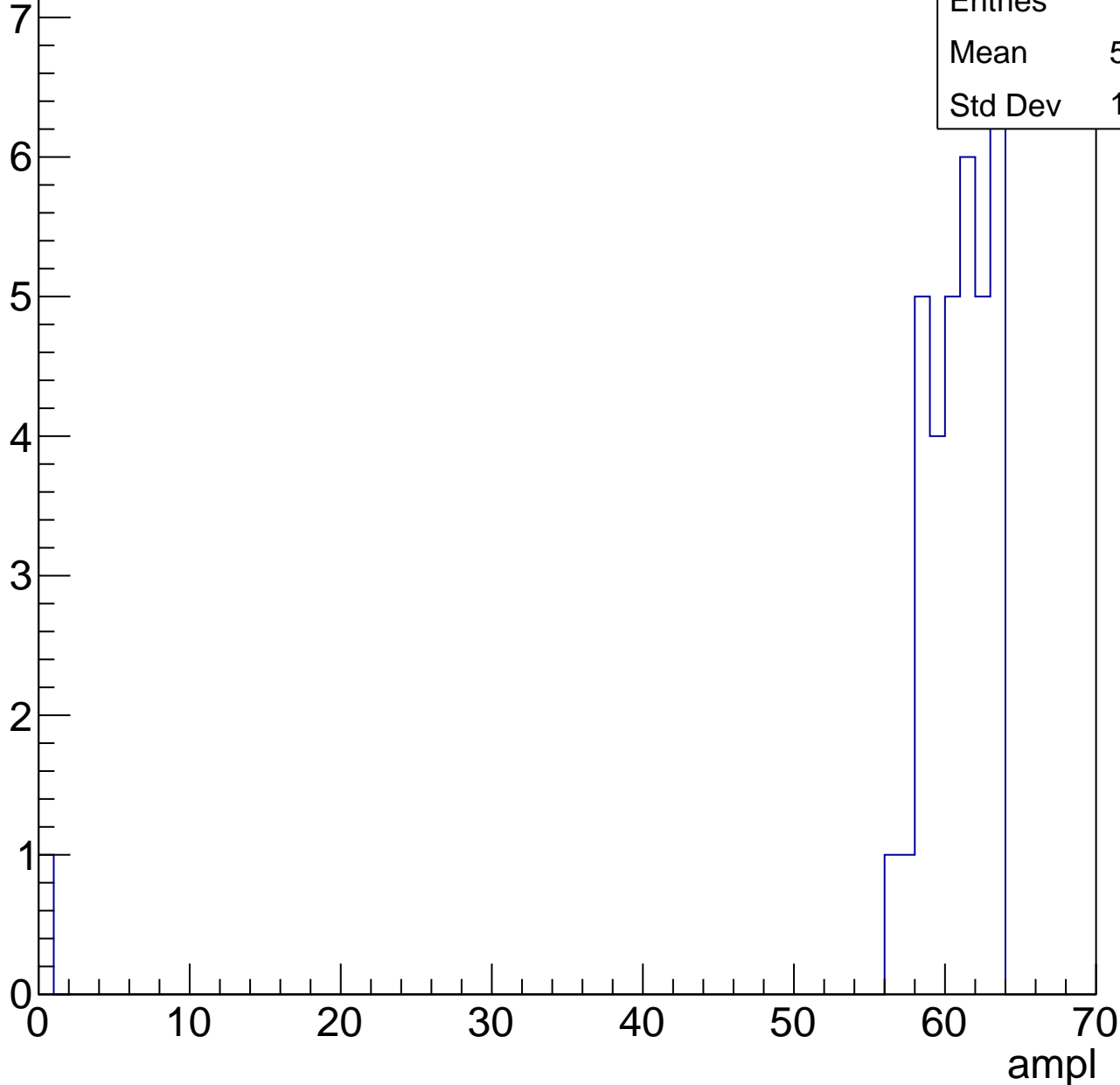
|         |       |
|---------|-------|
| Entries | 69    |
| Mean    | 56.28 |
| Std Dev | 3.447 |

# B0L001S, U2-ch85, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 35    |
| Mean    | 58.74 |
| Std Dev | 10.26 |



# B0L001S, U2-ch85, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch85, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 1 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch86, adc0

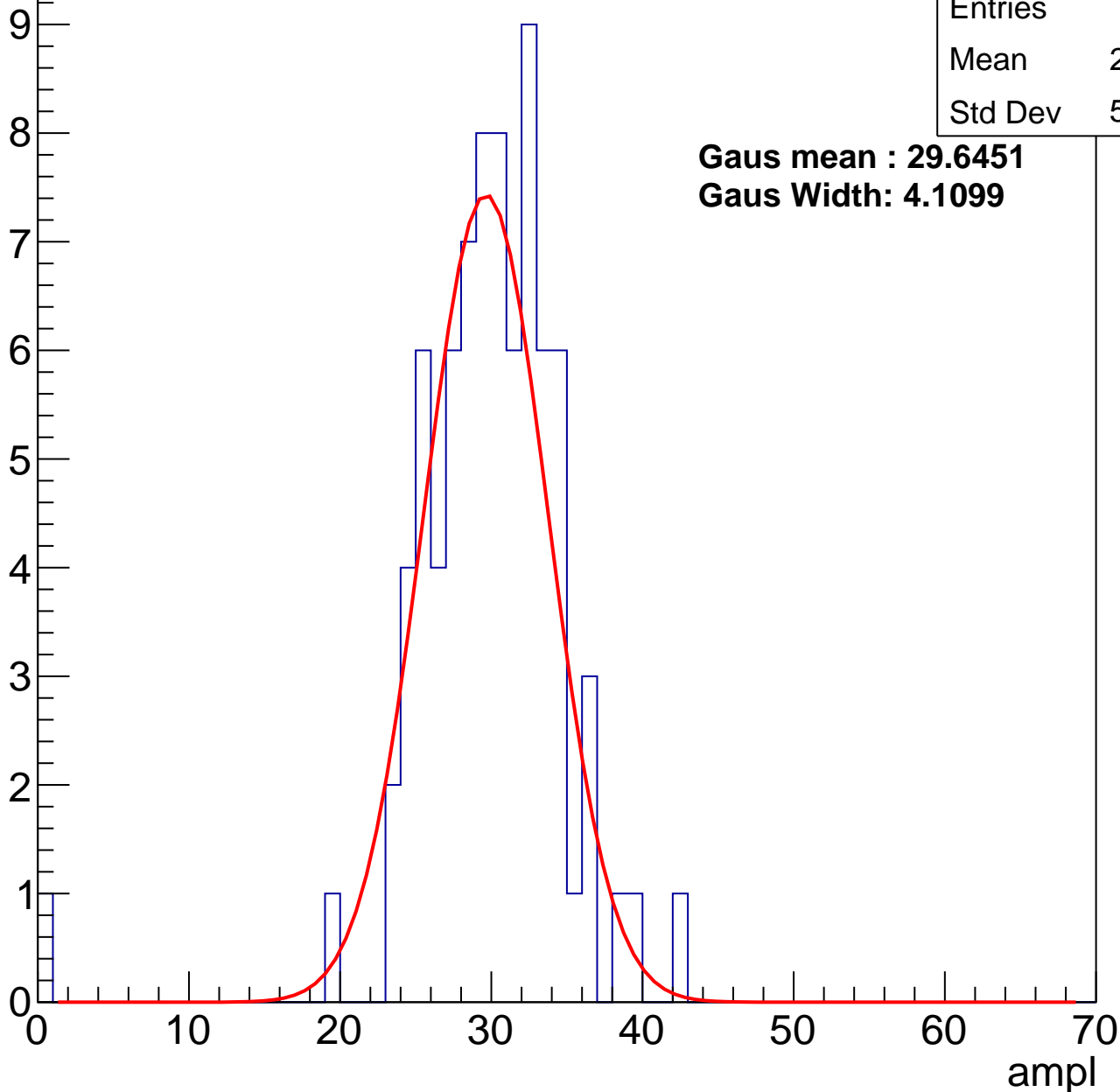
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 81    |
| Mean    | 29.42 |
| Std Dev | 5.156 |

**Gaus mean : 29.6451**

**Gaus Width: 4.1099**



# B0L001S, U2-ch86, adc1

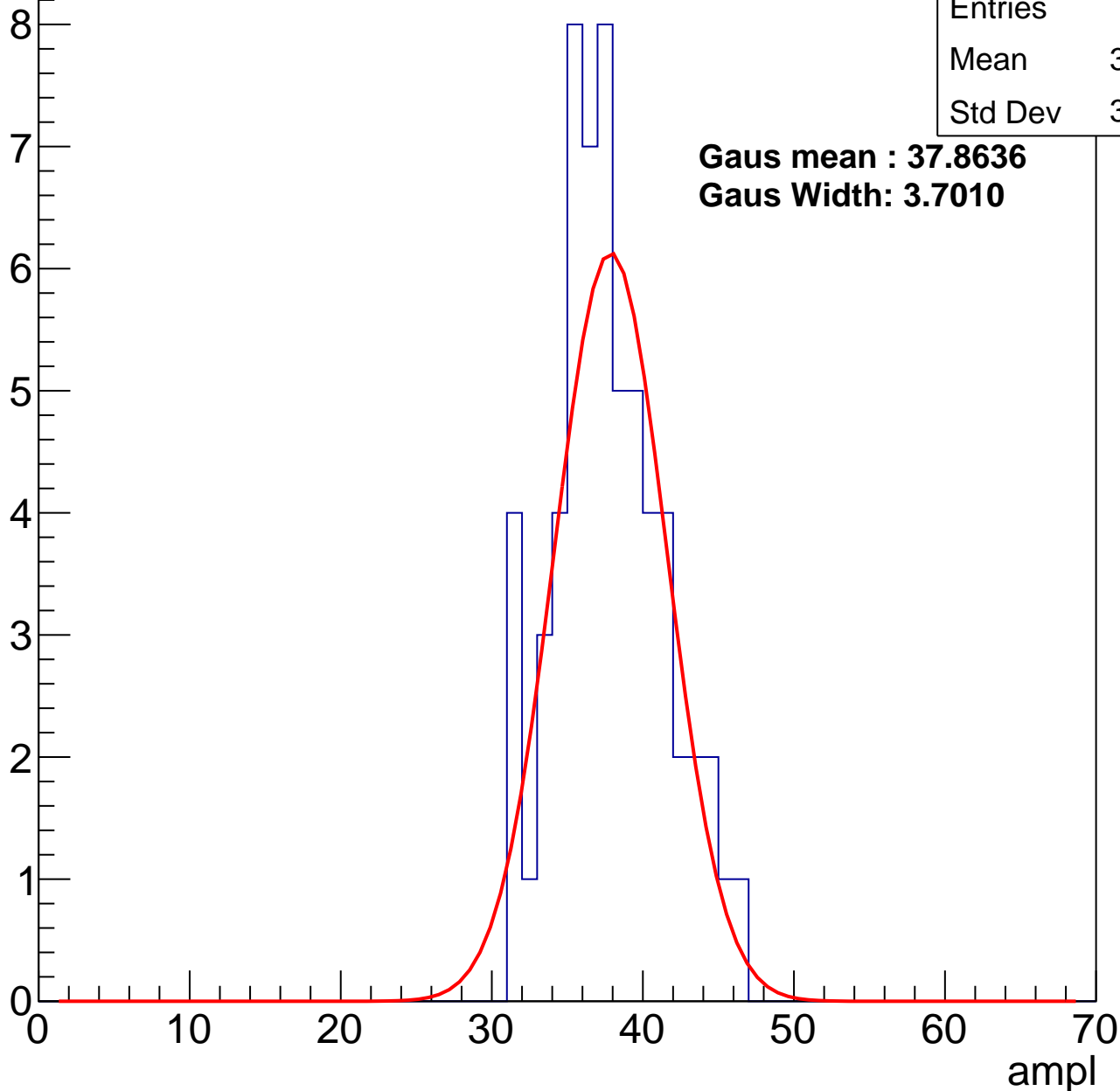
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 61    |
| Mean    | 37.33 |
| Std Dev | 3.565 |

**Gaus mean : 37.8636**

**Gaus Width: 3.7010**



# B0L001S, U2-ch86, adc2

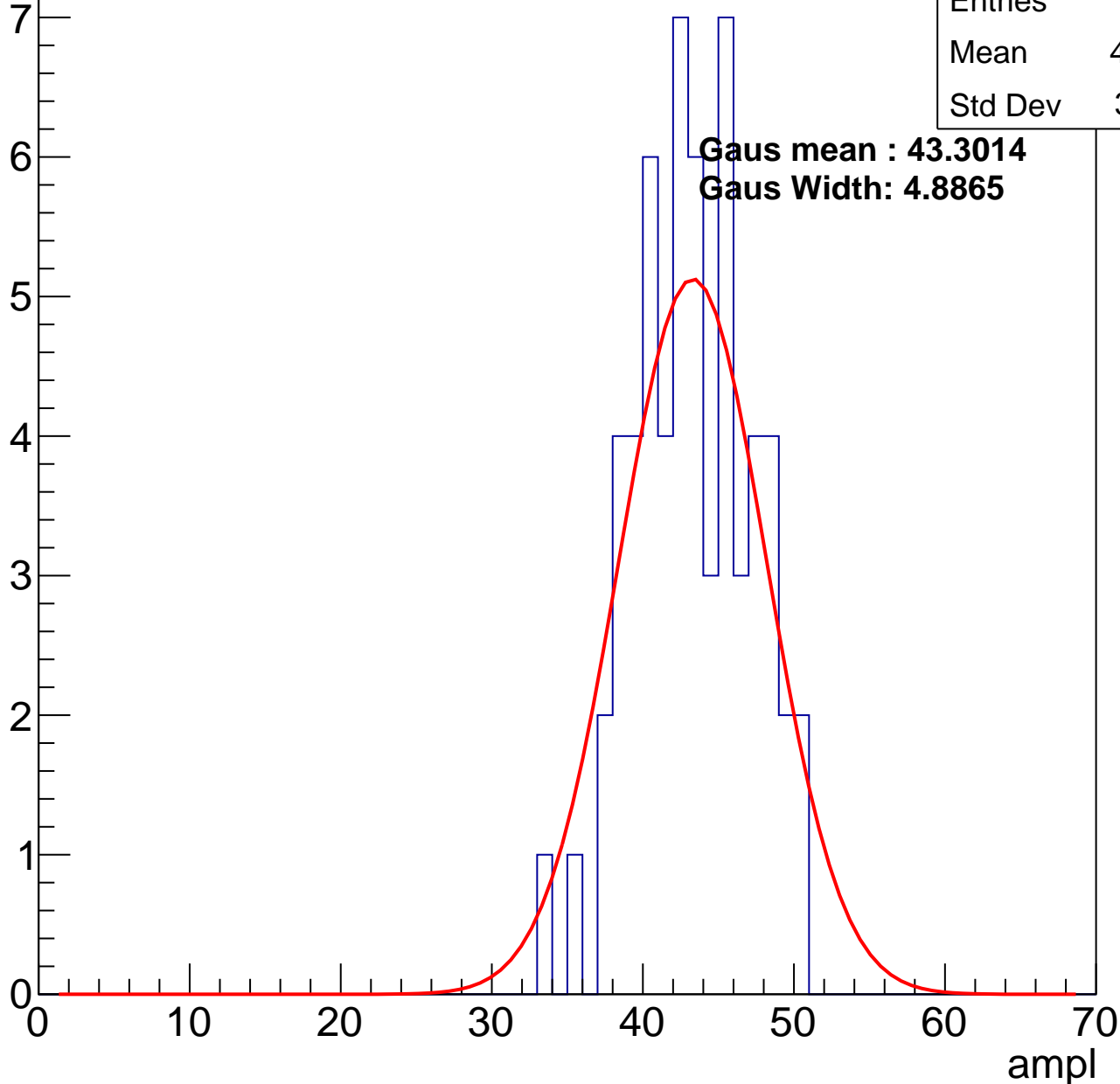
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 60    |
| Mean    | 42.82 |
| Std Dev | 3.801 |

**Gaus mean : 43.3014**

**Gaus Width: 4.8865**

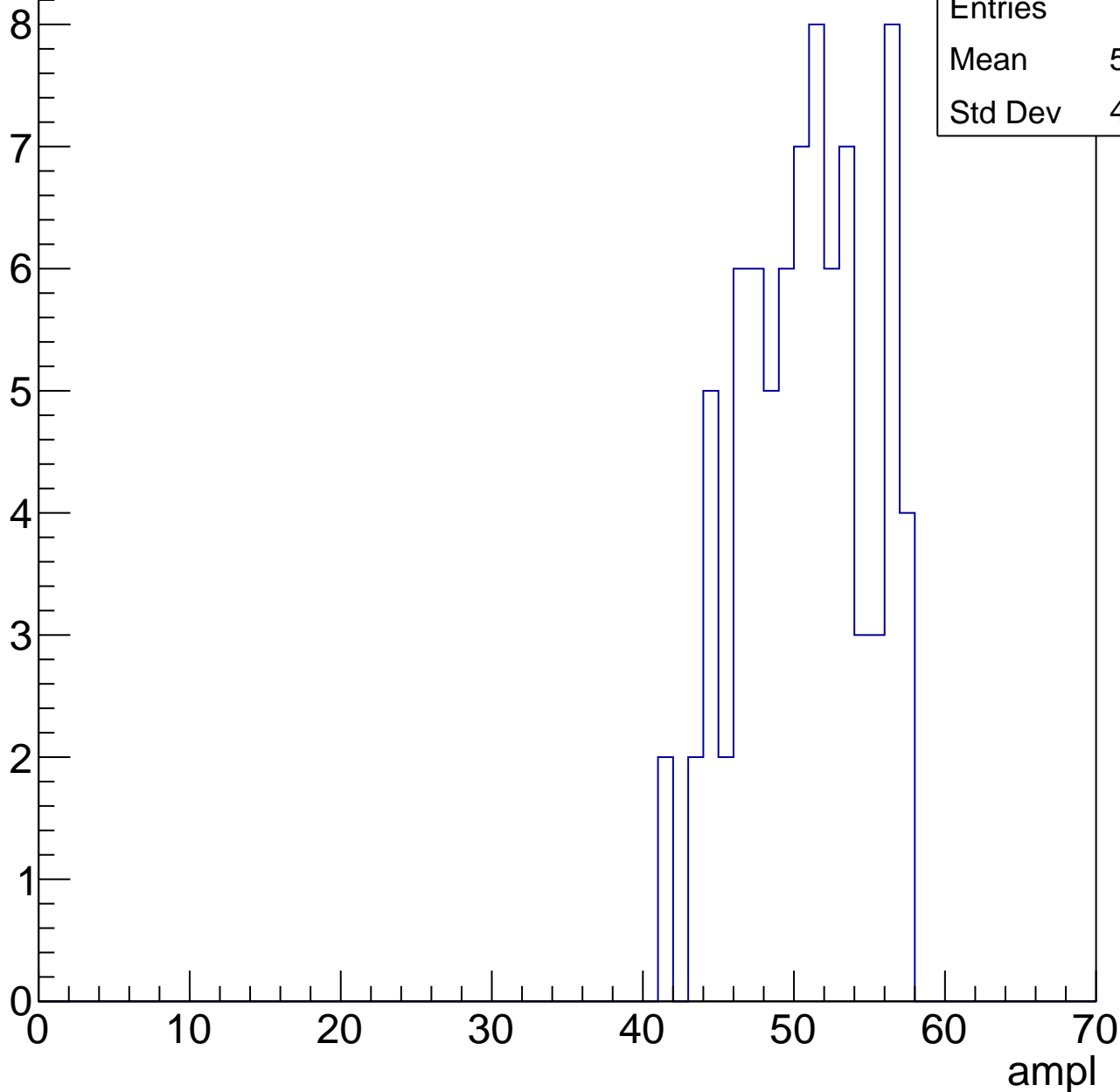


# B0L001S, U2-ch86, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 80    |
| Mean    | 50.17 |
| Std Dev | 4.132 |

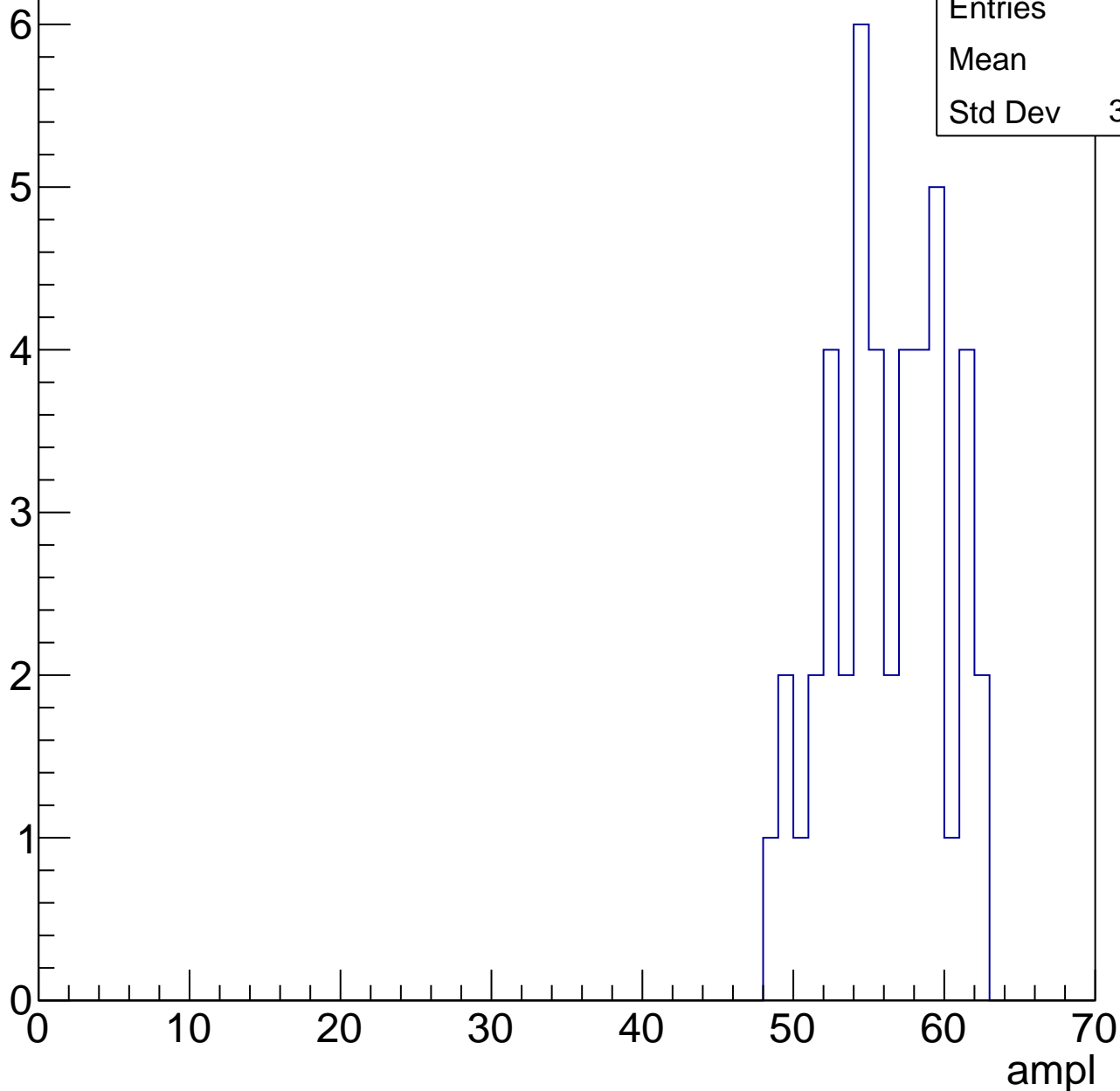


# B0L001S, U2-ch86, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 44    |
| Mean    | 55.7  |
| Std Dev | 3.715 |



# B0L001S, U2-ch86, adc5

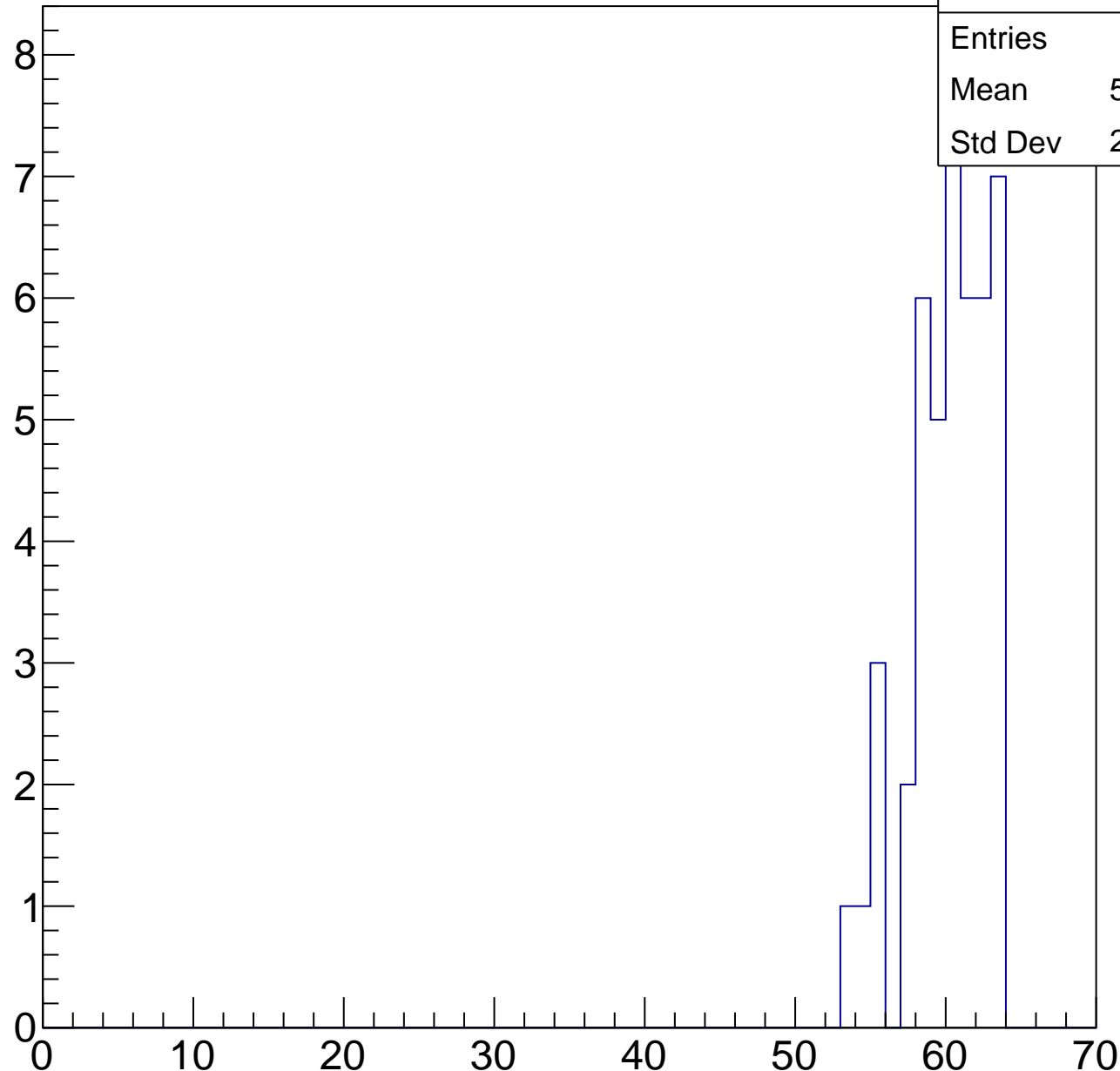
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

|         |       |
|---------|-------|
| Entries | 45    |
| Mean    | 59.73 |
| Std Dev | 2.568 |

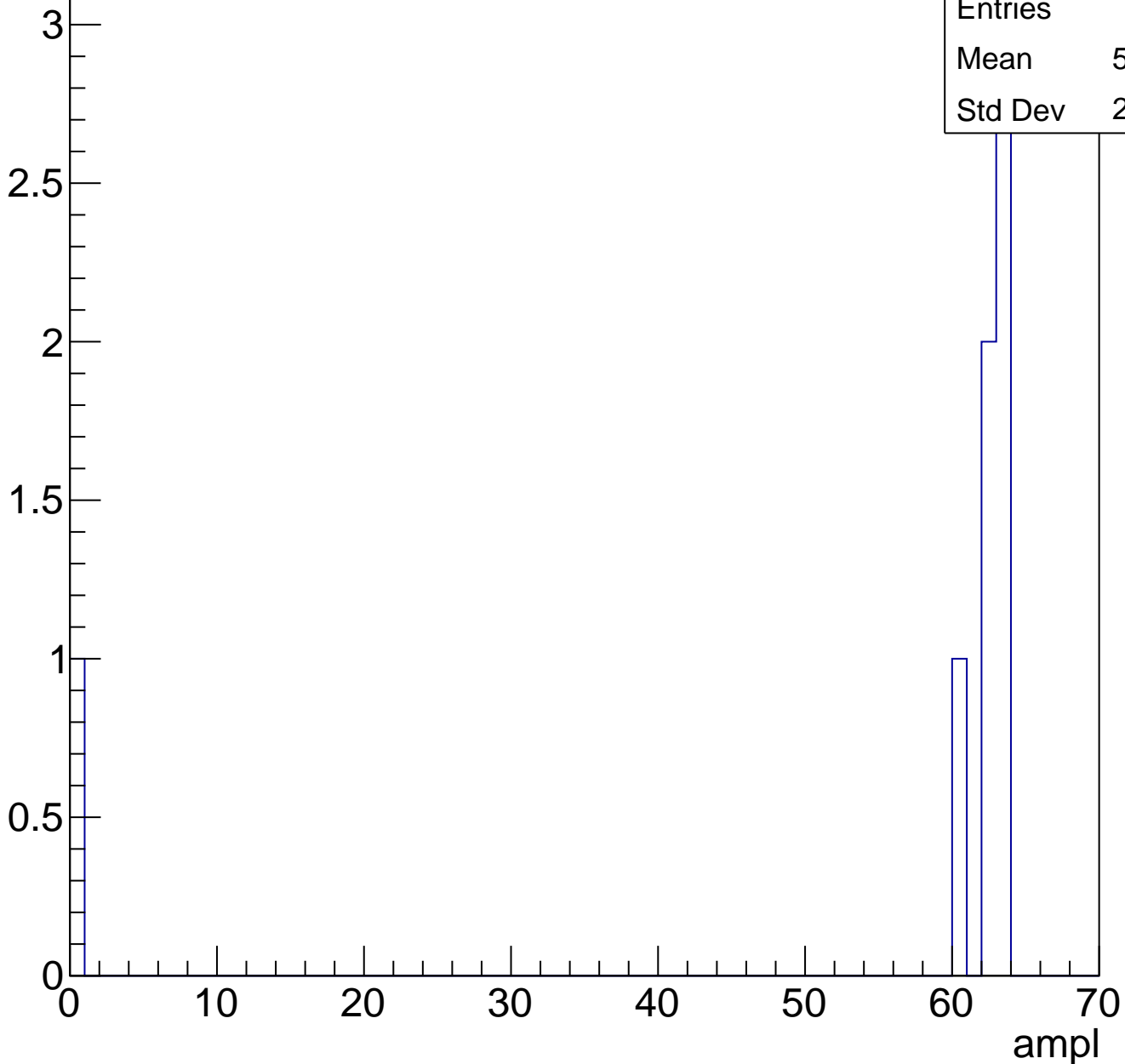
ampl



# B0L001S, U2-ch86, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch86, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U2-ch87, adc0

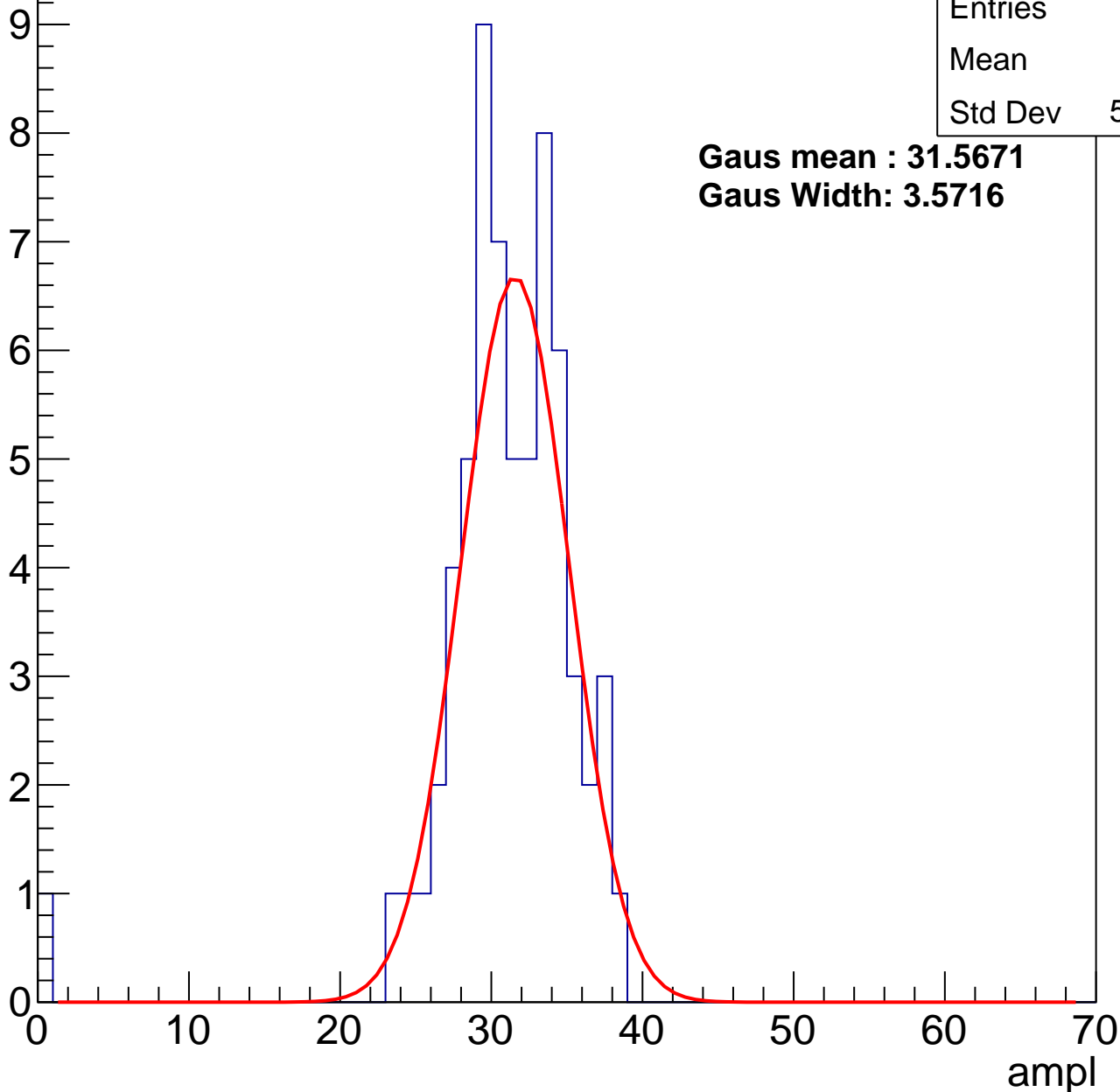
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 64    |
| Mean    | 30.5  |
| Std Dev | 5.065 |

**Gaus mean : 31.5671**

**Gaus Width: 3.5716**



# B0L001S, U2-ch87, adc1

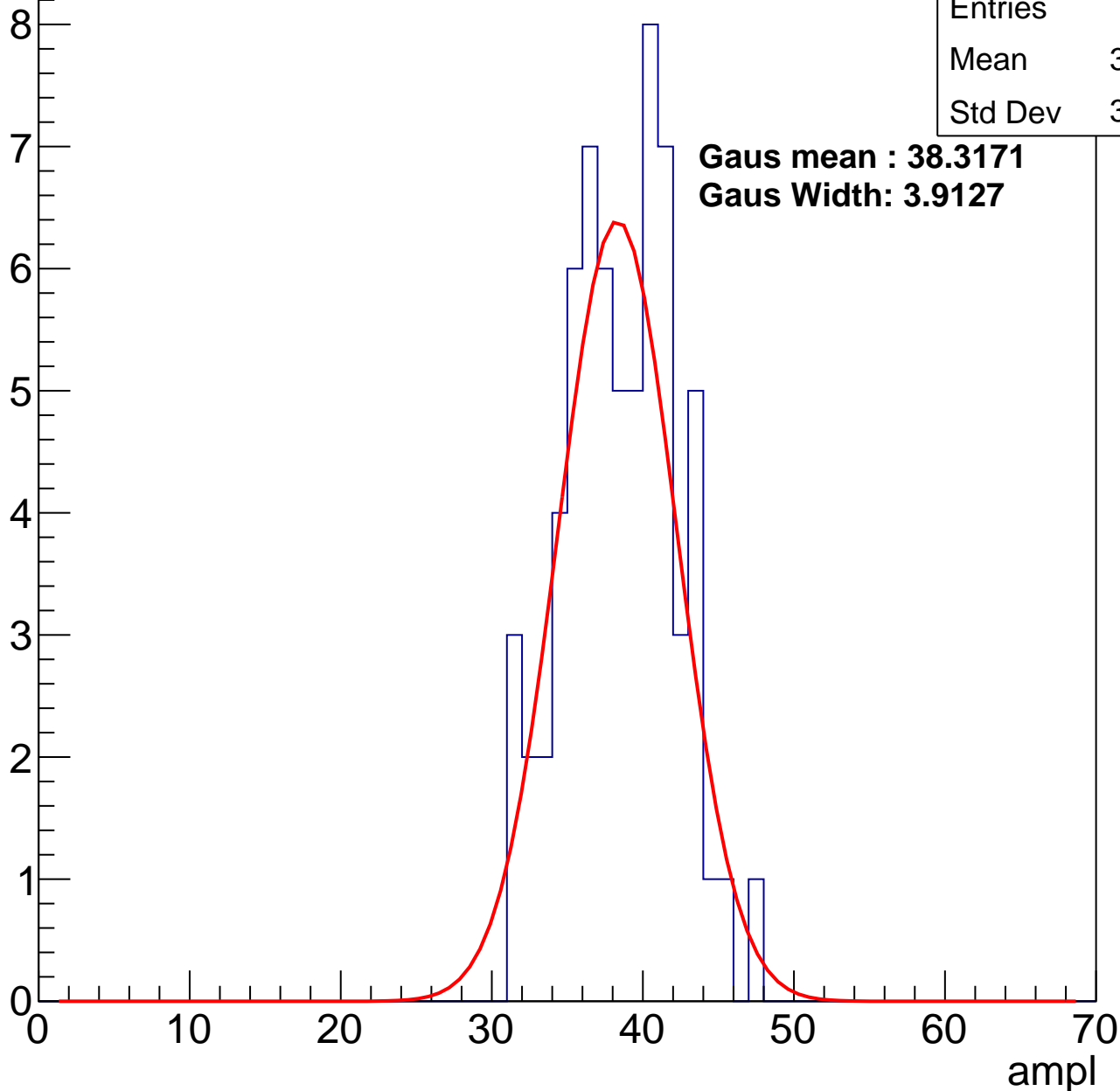
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 66    |
| Mean    | 38.06 |
| Std Dev | 3.609 |

**Gaus mean : 38.3171**

**Gaus Width: 3.9127**



# B0L001S, U2-ch87, adc2

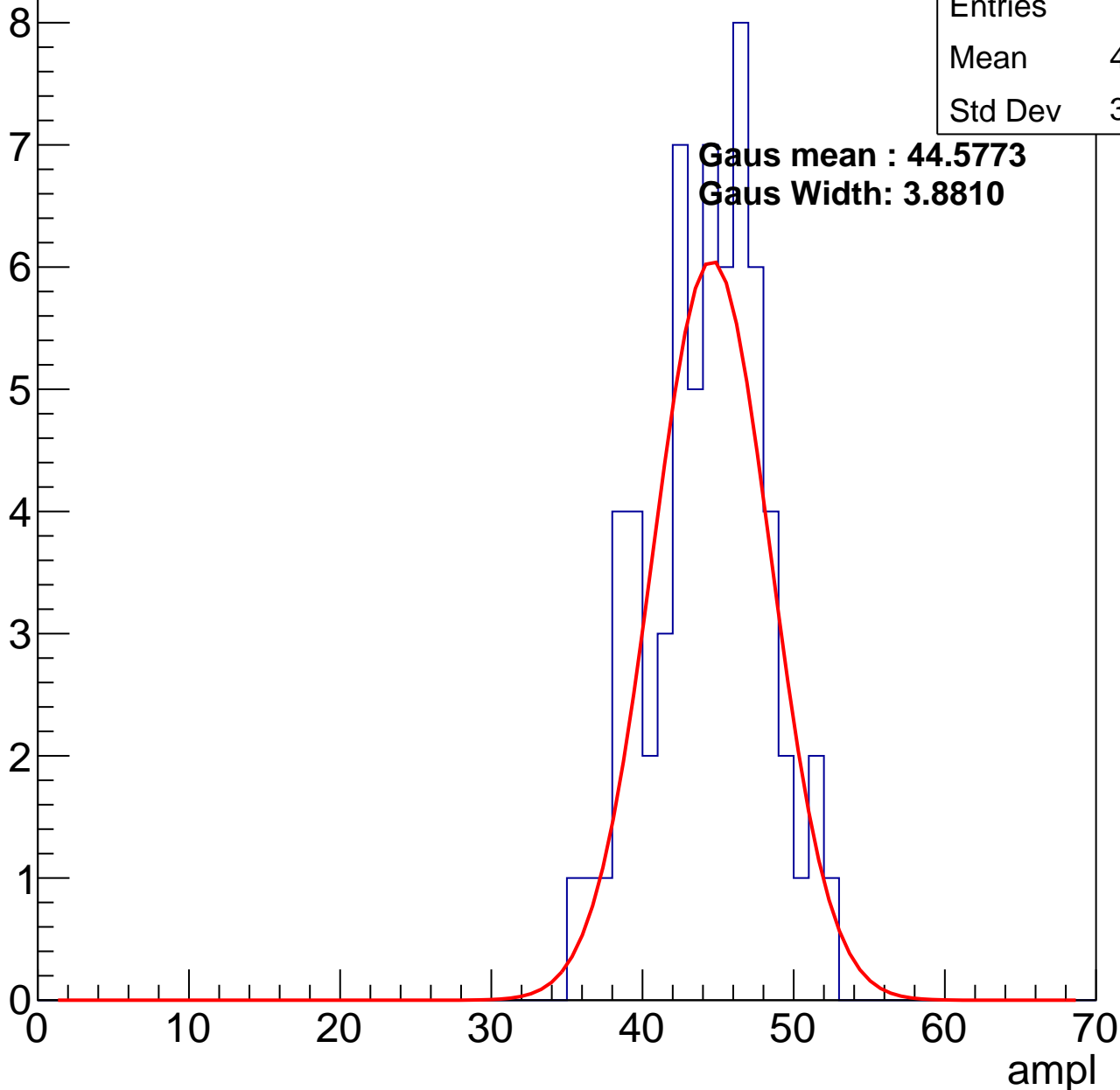
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 65    |
| Mean    | 43.85 |
| Std Dev | 3.788 |

**Gaus mean : 44.5773**

**Gaus Width: 3.8810**

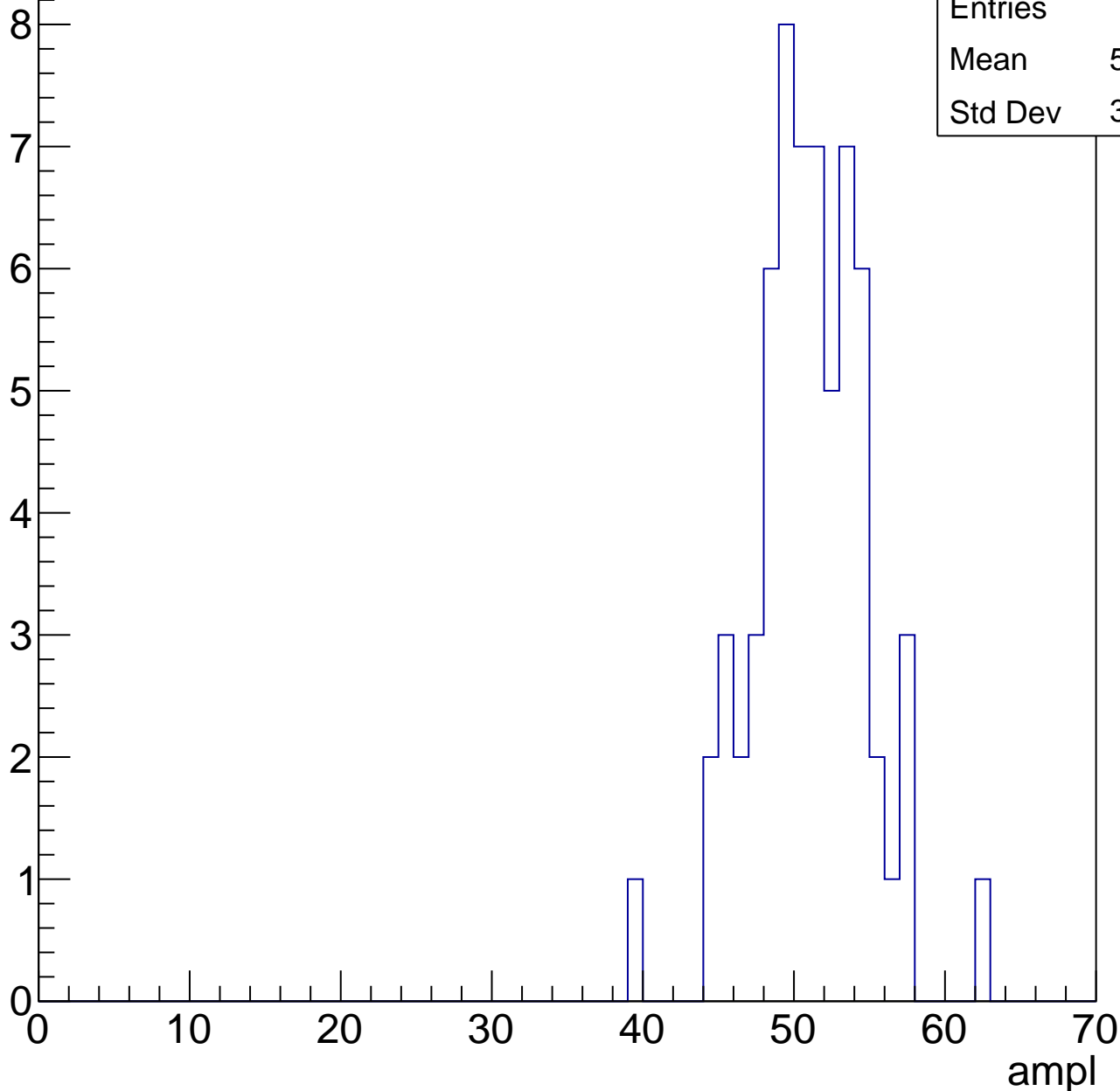


# B0L001S, U2-ch87, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

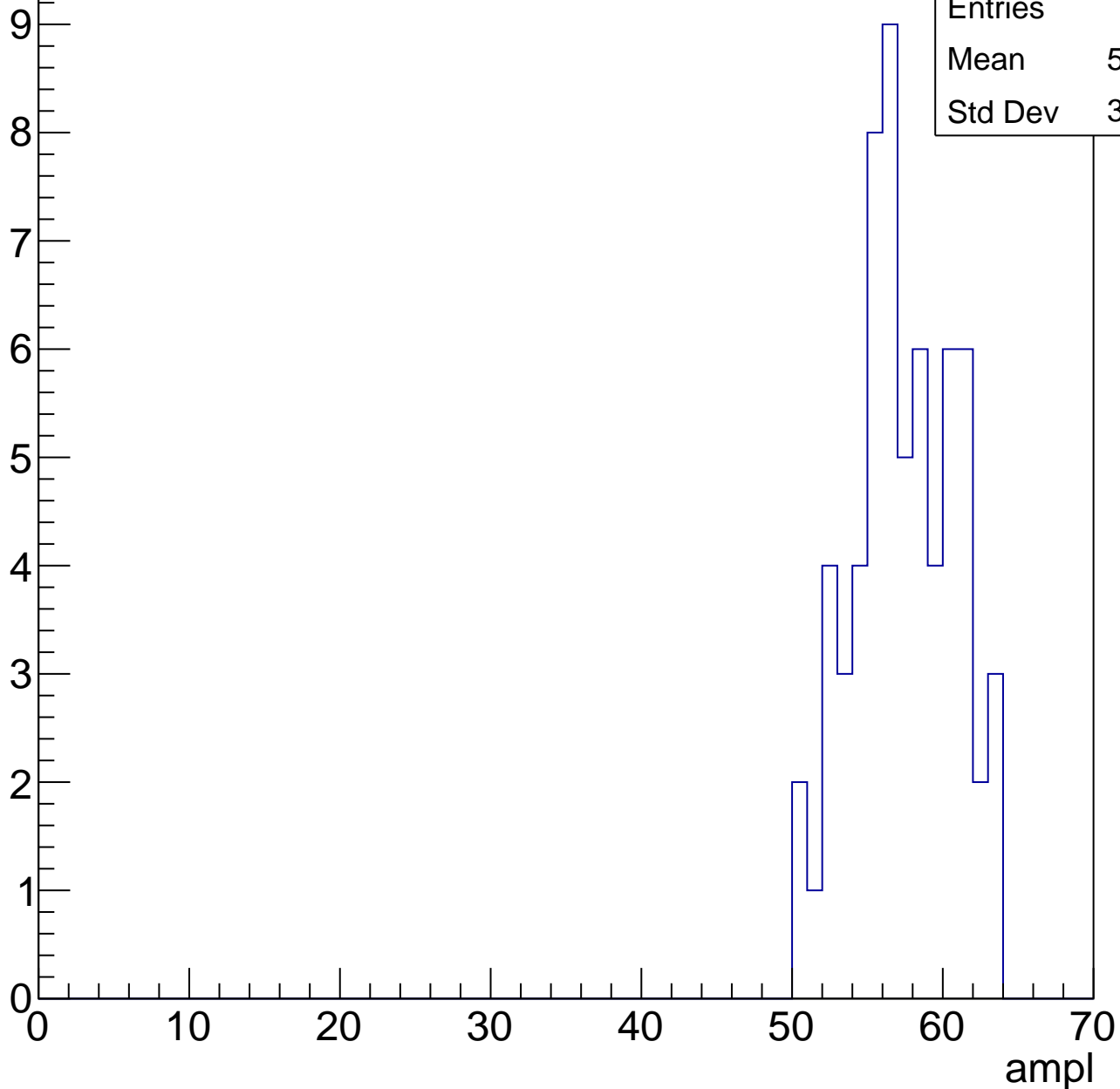
|         |       |
|---------|-------|
| Entries | 64    |
| Mean    | 50.56 |
| Std Dev | 3.754 |



# B0L001S, U2-ch87, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

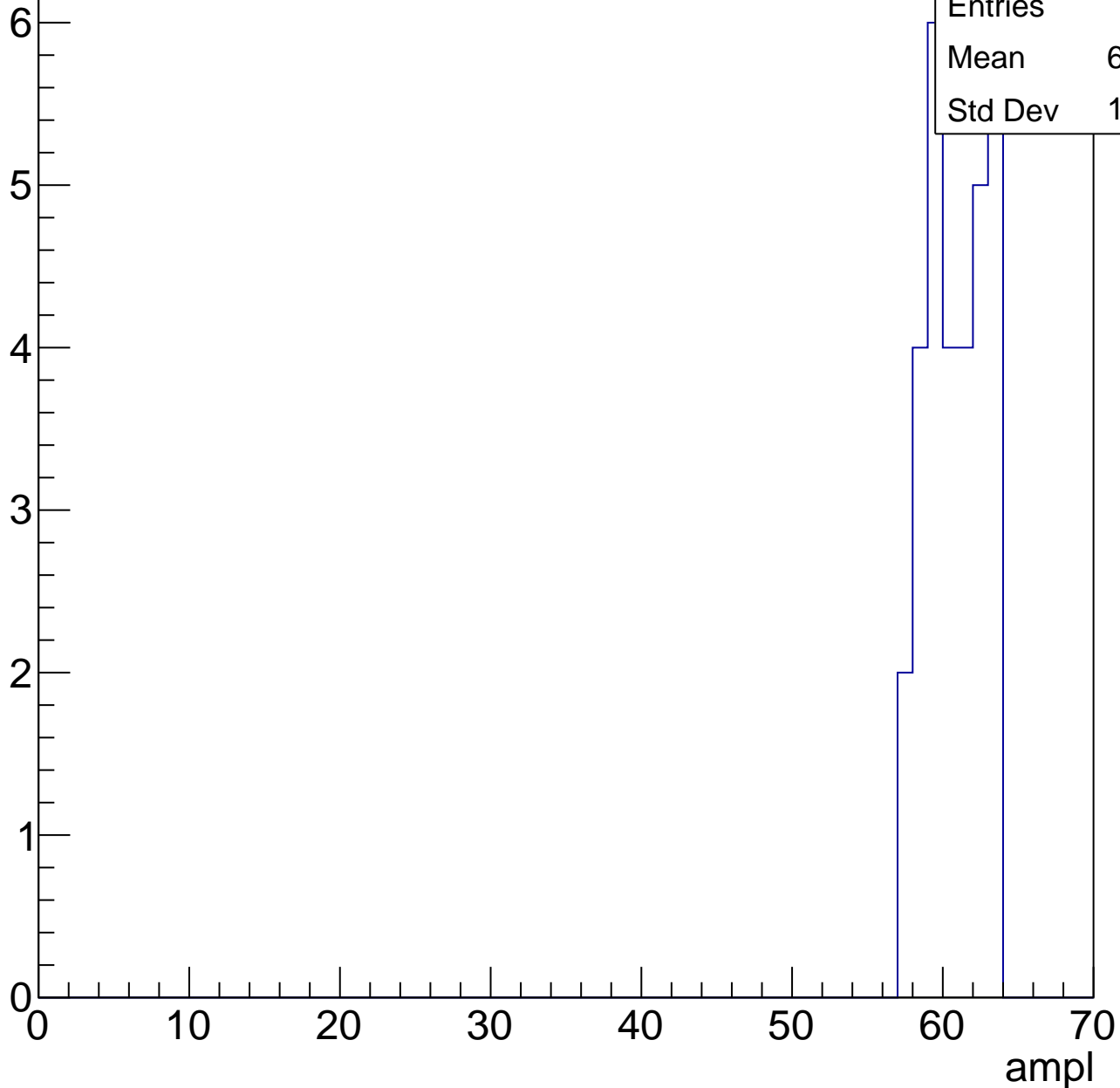


|         |       |
|---------|-------|
| Entries | 63    |
| Mean    | 56.92 |
| Std Dev | 3.306 |

# B0L001S, U2-ch87, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

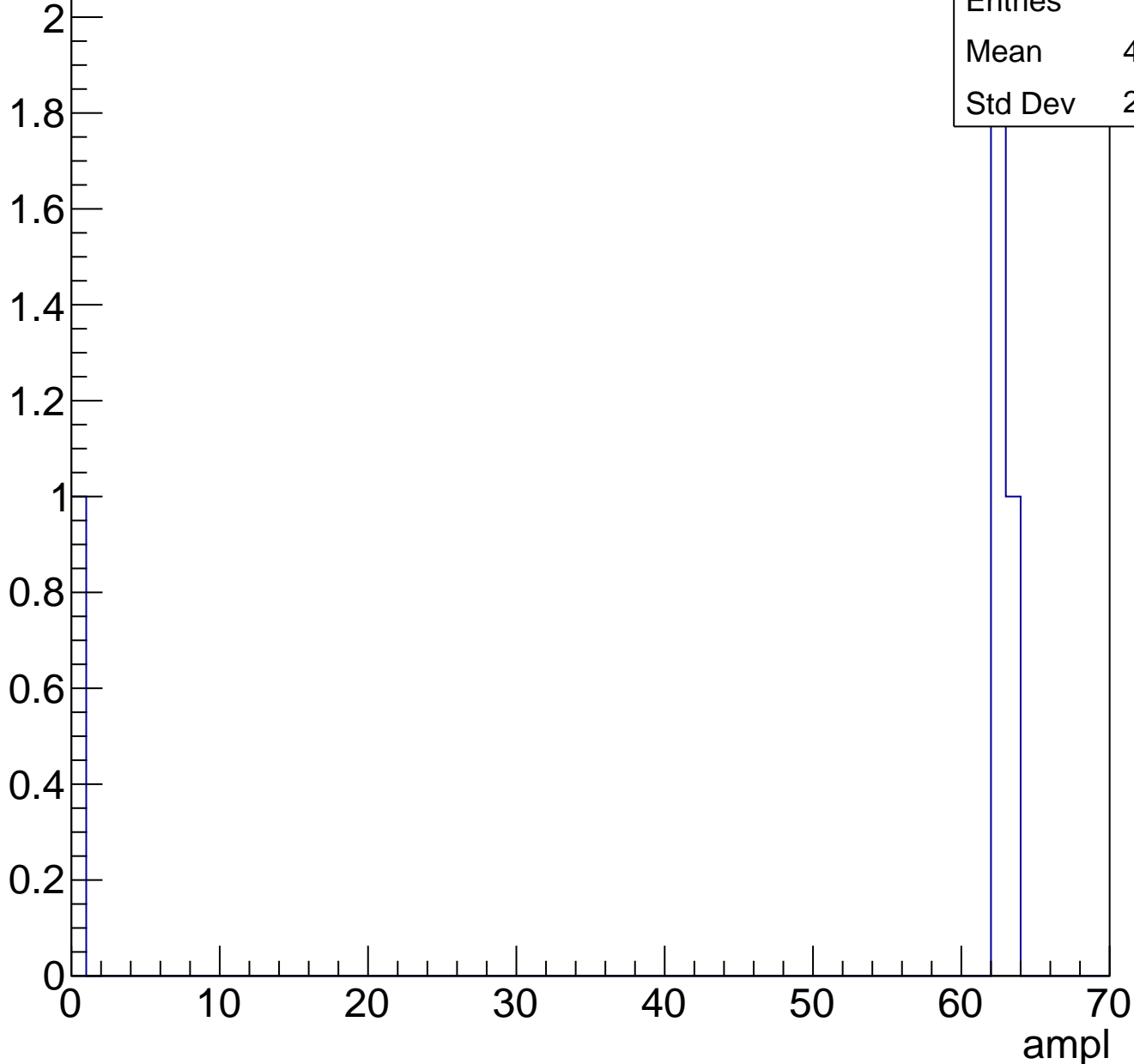
Entry



# B0L001S, U2-ch87, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch87, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 0 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch88, adc0

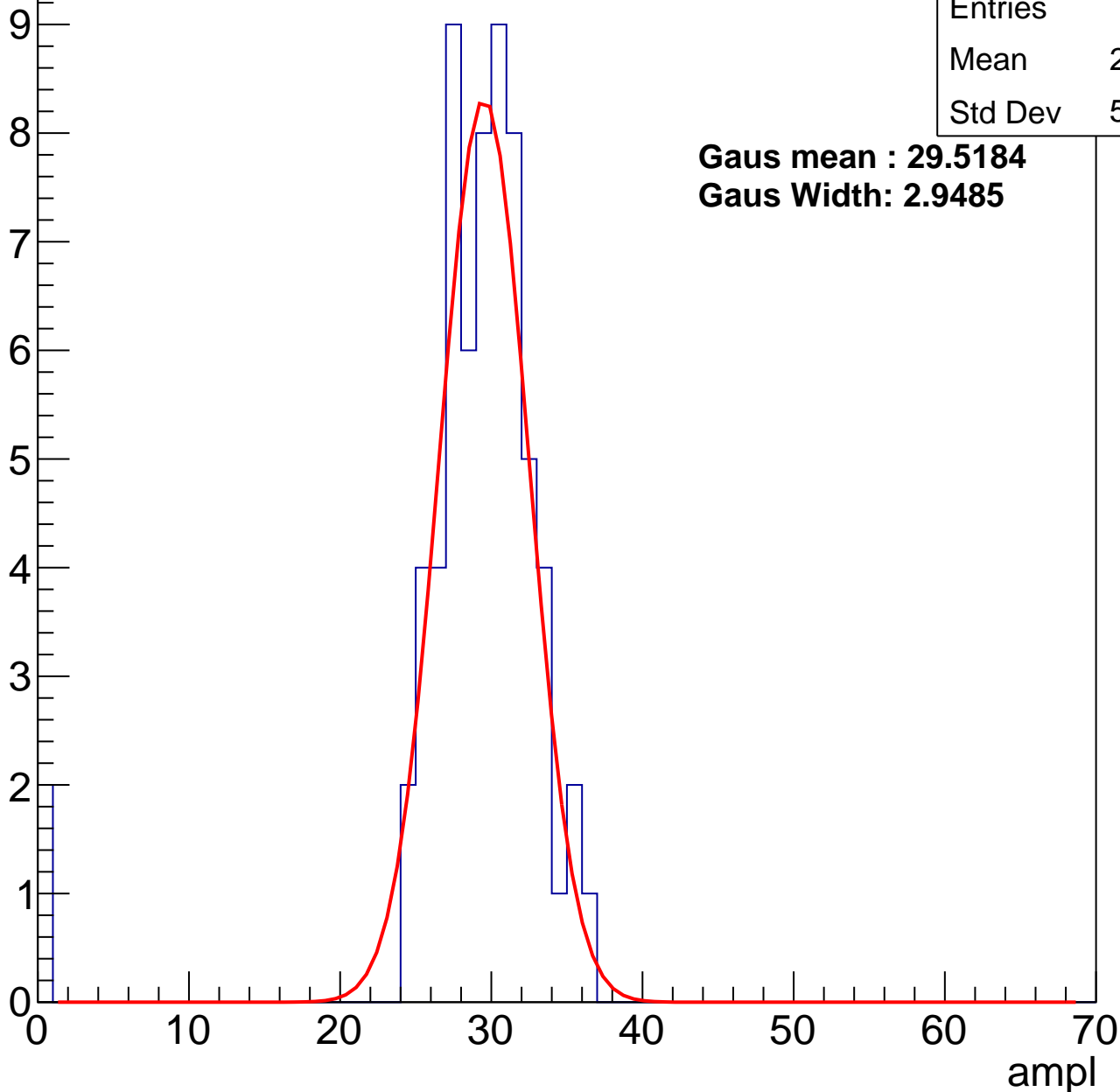
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 65    |
| Mean    | 28.38 |
| Std Dev | 5.745 |

**Gaus mean : 29.5184**

**Gaus Width: 2.9485**



# B0L001S, U2-ch88, adc1

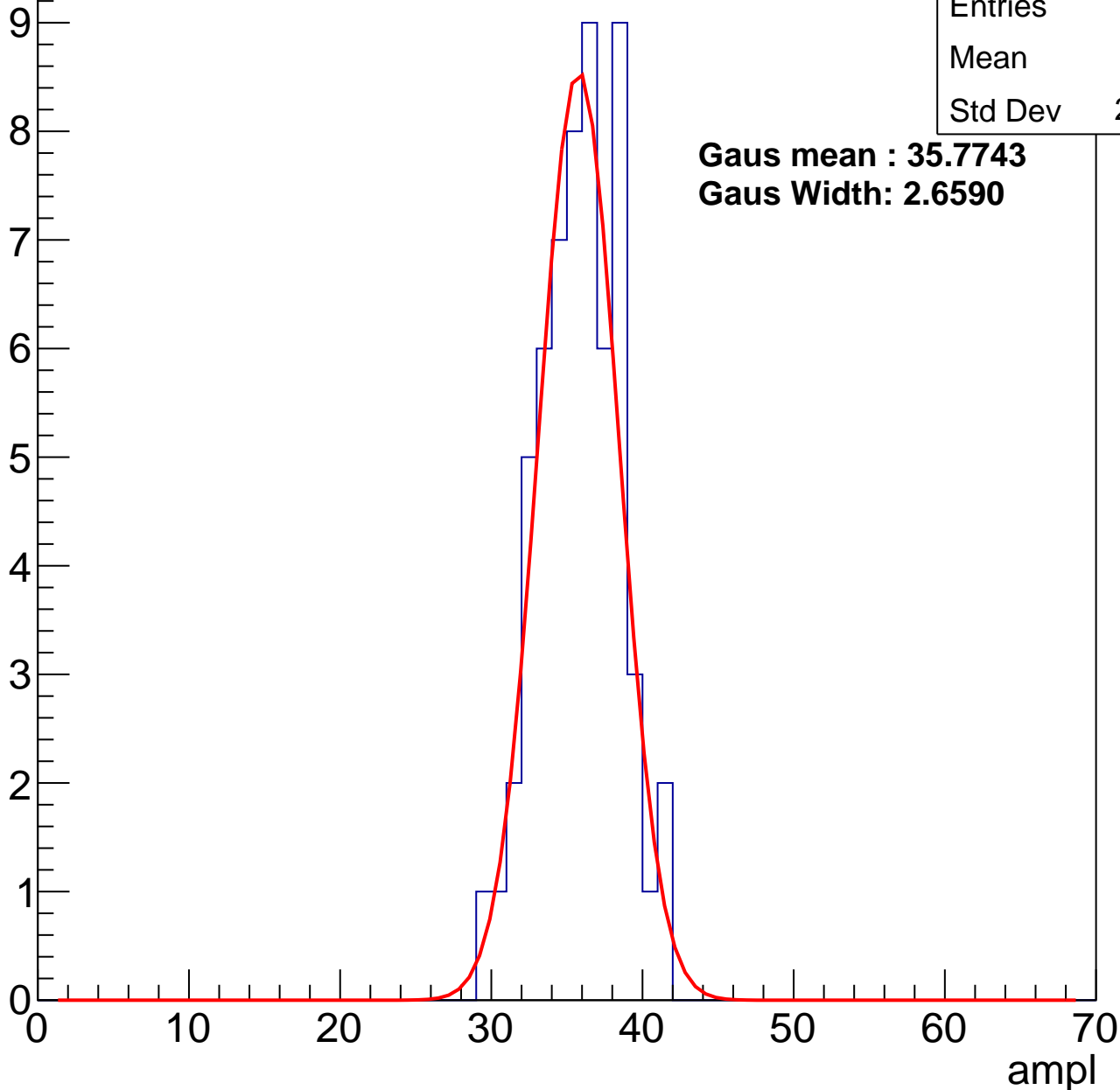
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 60    |
| Mean    | 35.4  |
| Std Dev | 2.641 |

**Gaus mean : 35.7743**

**Gaus Width: 2.6590**



# B0L001S, U2-ch88, adc2

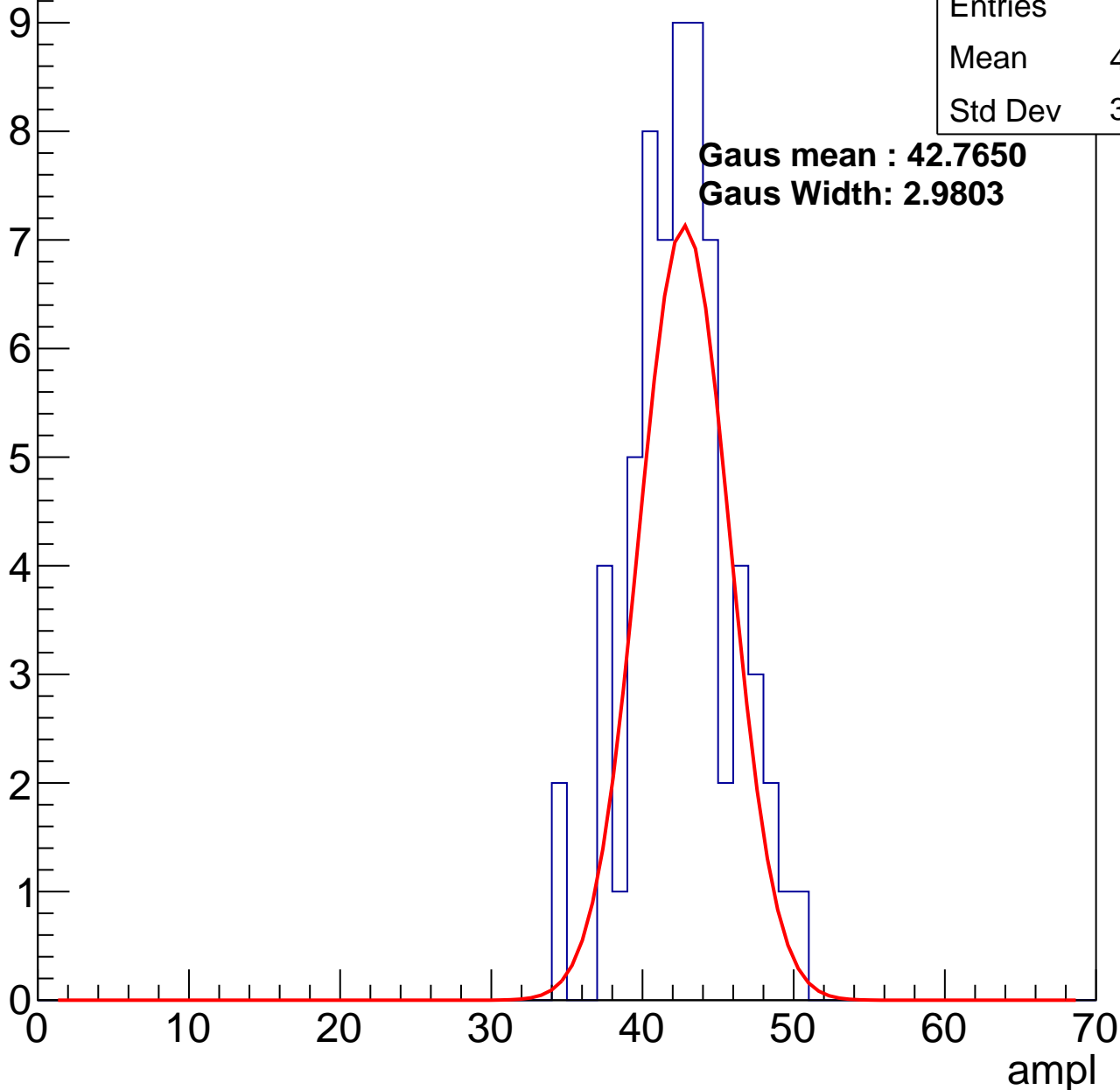
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 65    |
| Mean    | 42.14 |
| Std Dev | 3.295 |

**Gaus mean : 42.7650**

**Gaus Width: 2.9803**

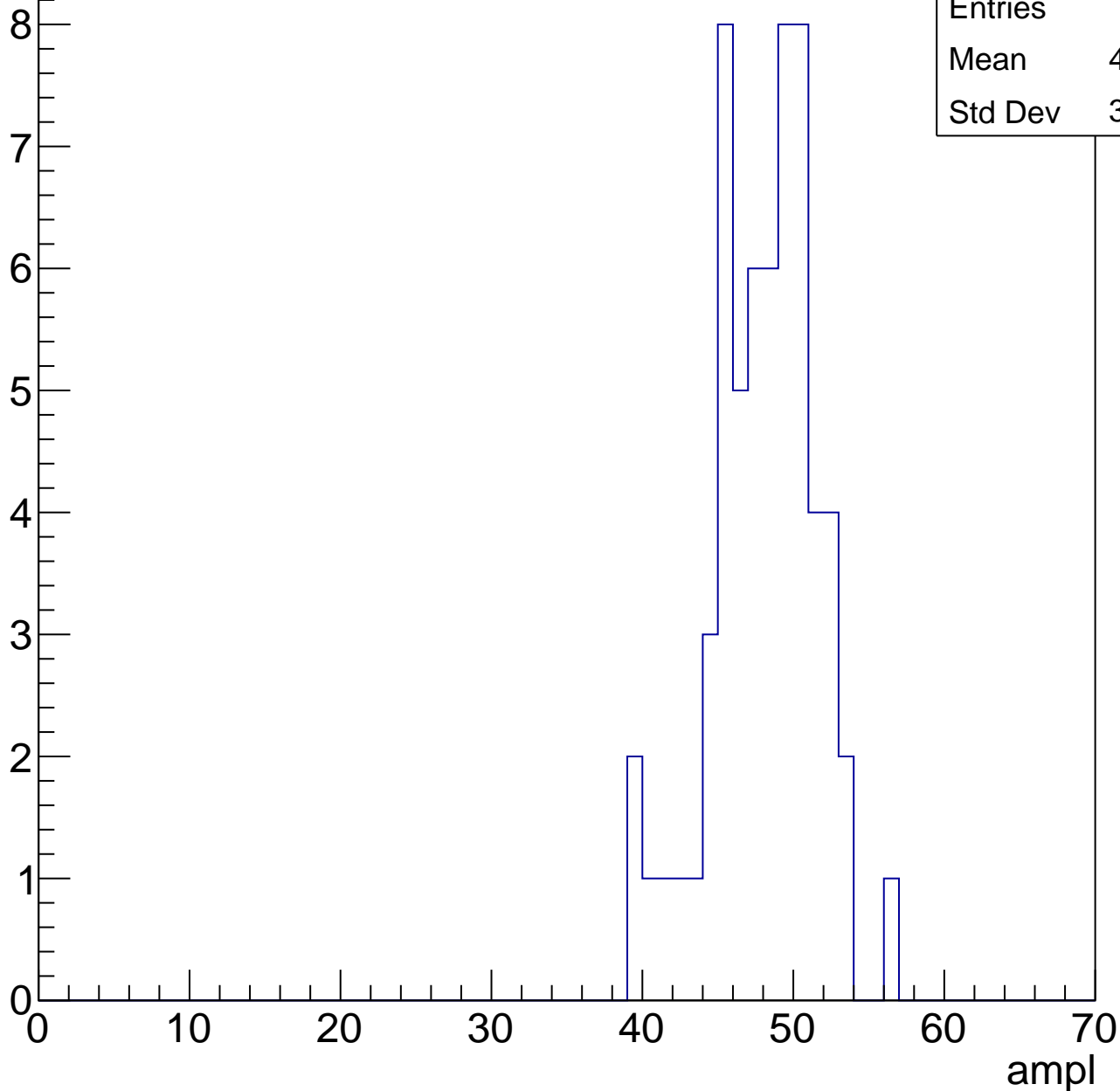


# B0L001S, U2-ch88, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 61    |
| Mean    | 47.57 |
| Std Dev | 3.447 |

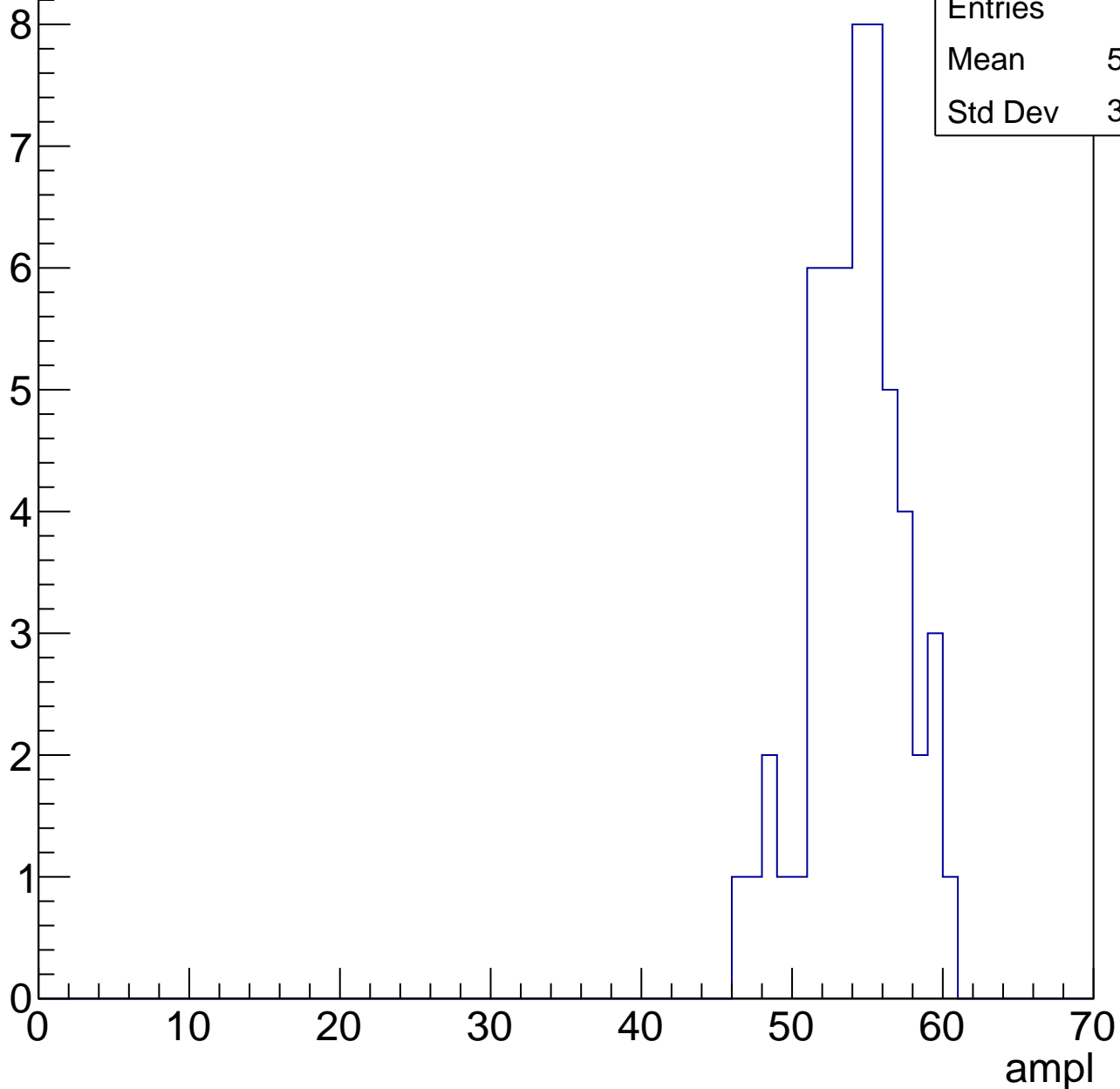


# B0L001S, U2-ch88, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

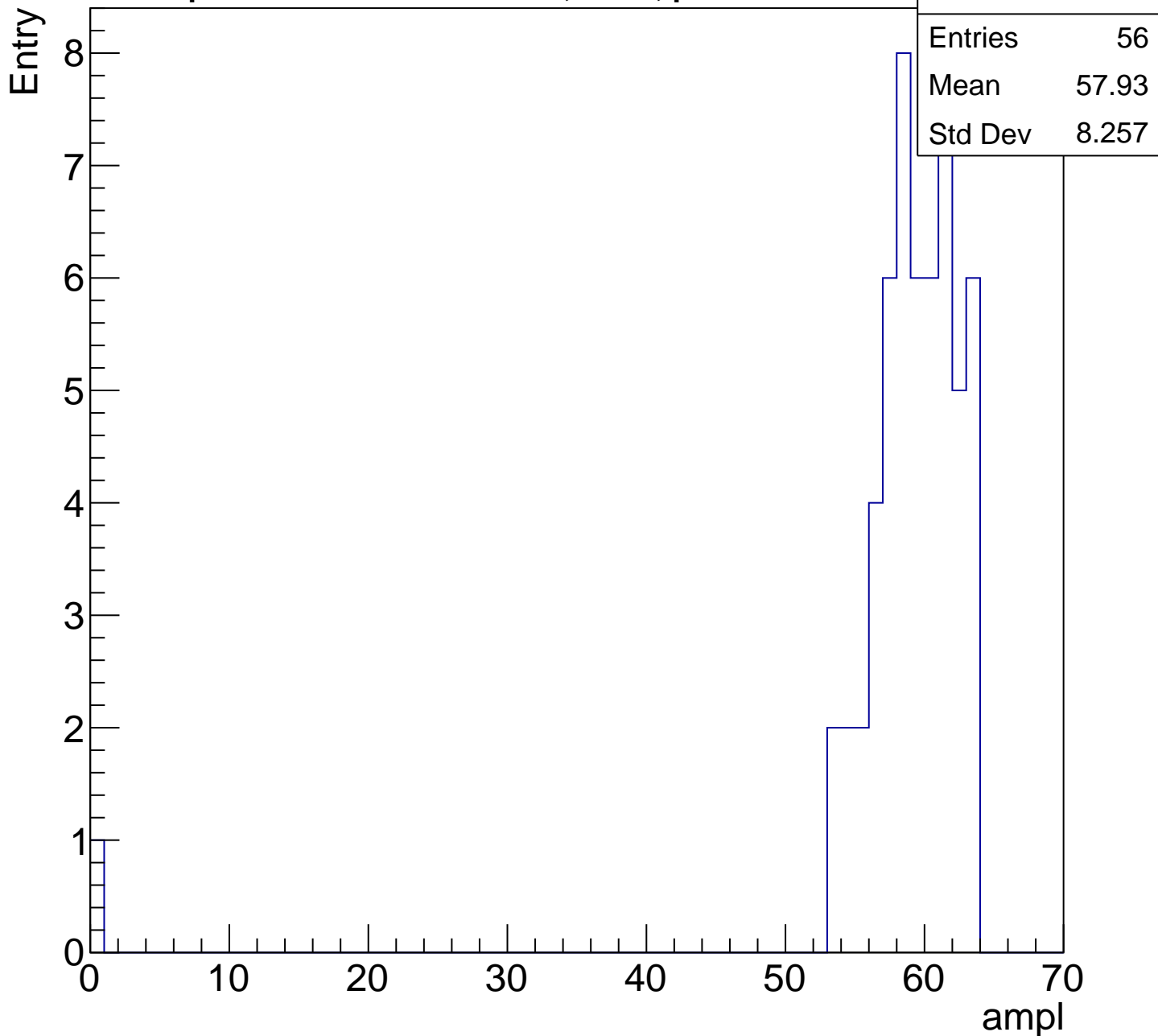
Entry

|         |       |
|---------|-------|
| Entries | 55    |
| Mean    | 53.76 |
| Std Dev | 3.057 |



# B0L001S, U2-ch88, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

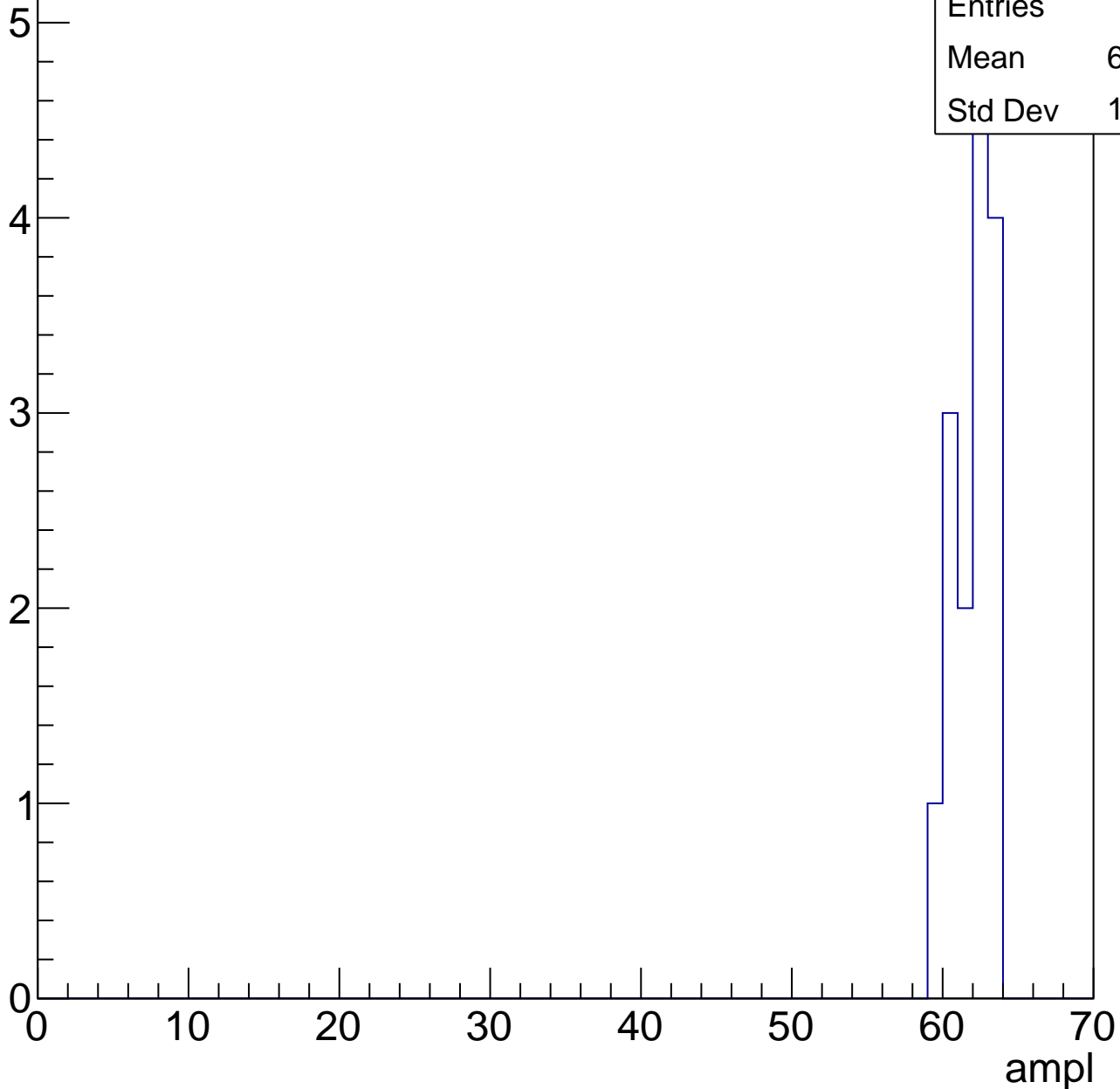


# B0L001S, U2-ch88, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 15    |
| Mean    | 61.53 |
| Std Dev | 1.258 |





# B0L001S, U2-ch88, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 0 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch89, adc0

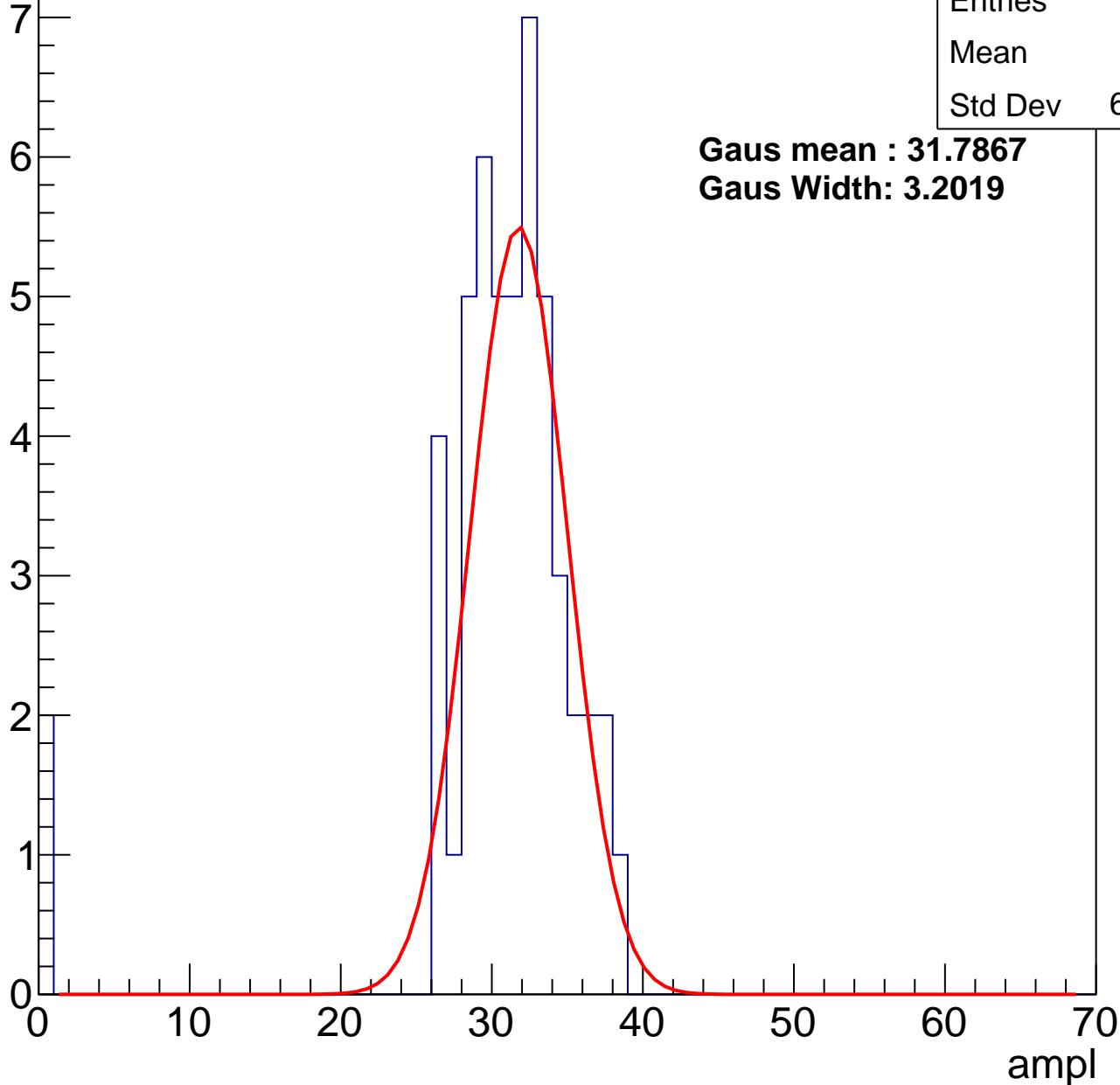
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 50    |
| Mean    | 29.9  |
| Std Dev | 6.795 |

**Gaus mean : 31.7867**

**Gaus Width: 3.2019**



# B0L001S, U2-ch89, adc1

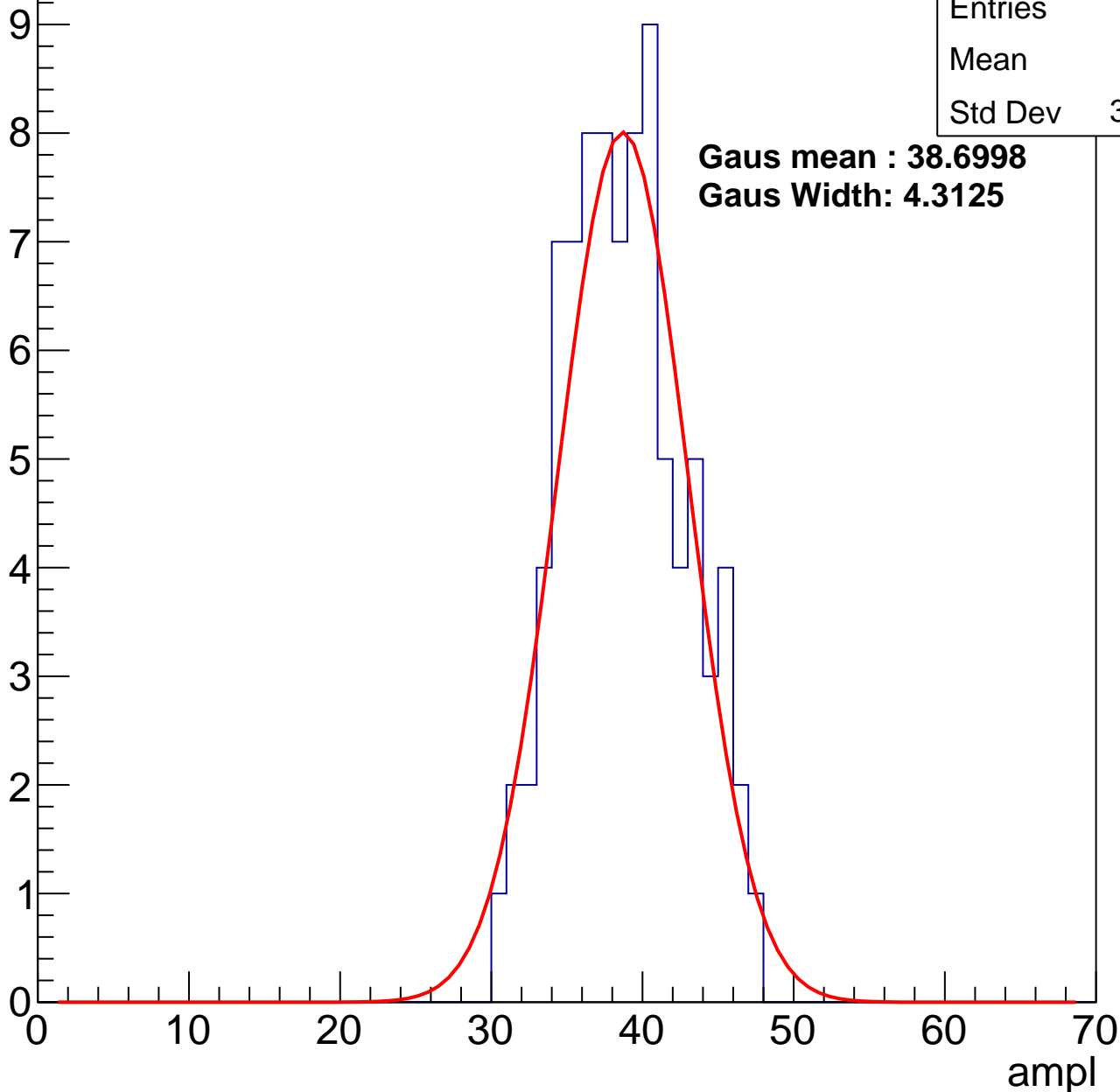
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 87    |
| Mean    | 38.3  |
| Std Dev | 3.913 |

**Gaus mean : 38.6998**

**Gaus Width: 4.3125**



# B0L001S, U2-ch89, adc2

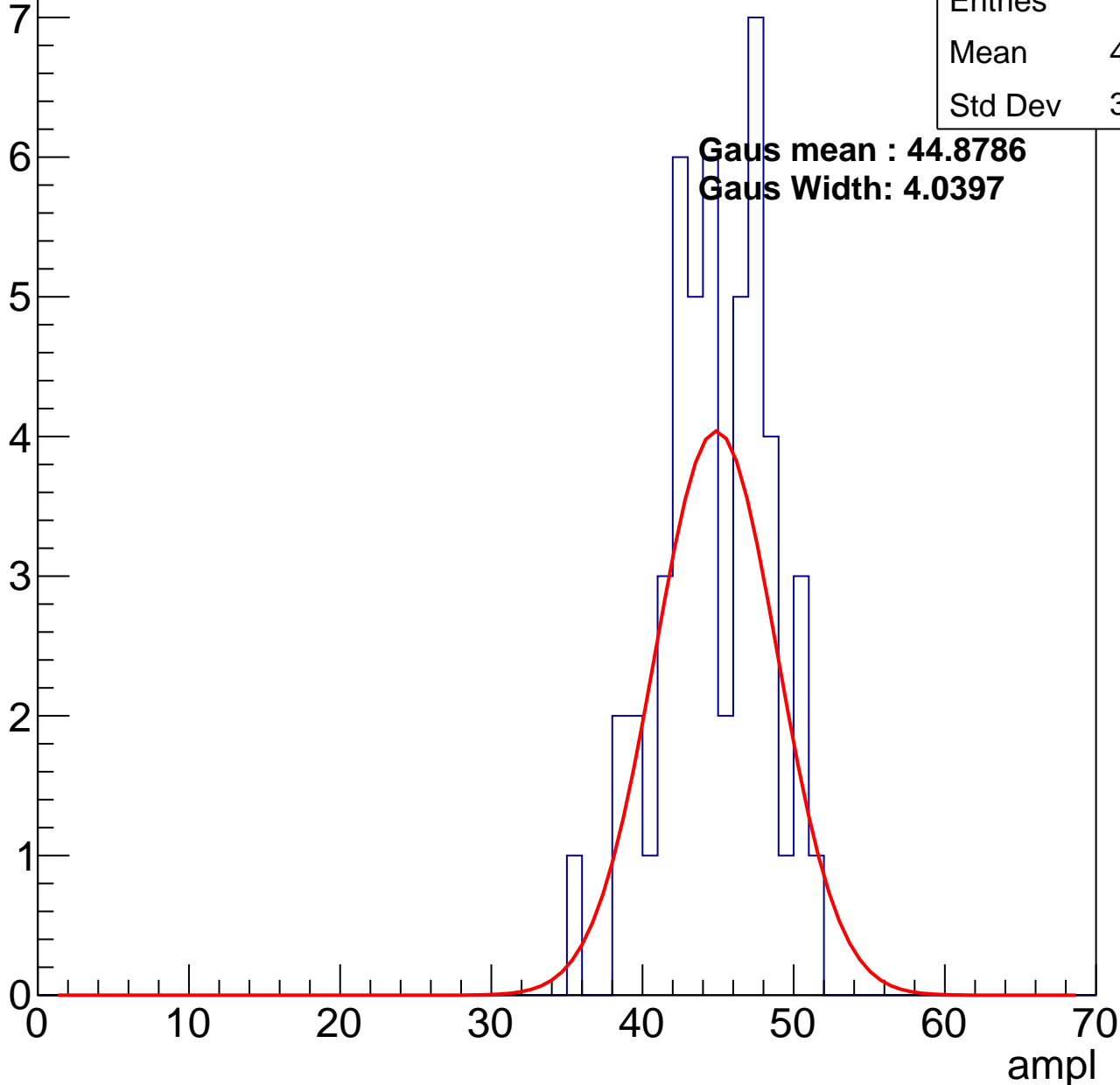
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 49    |
| Mean    | 44.37 |
| Std Dev | 3.497 |

**Gaus mean : 44.8786**

**Gaus Width: 4.0397**

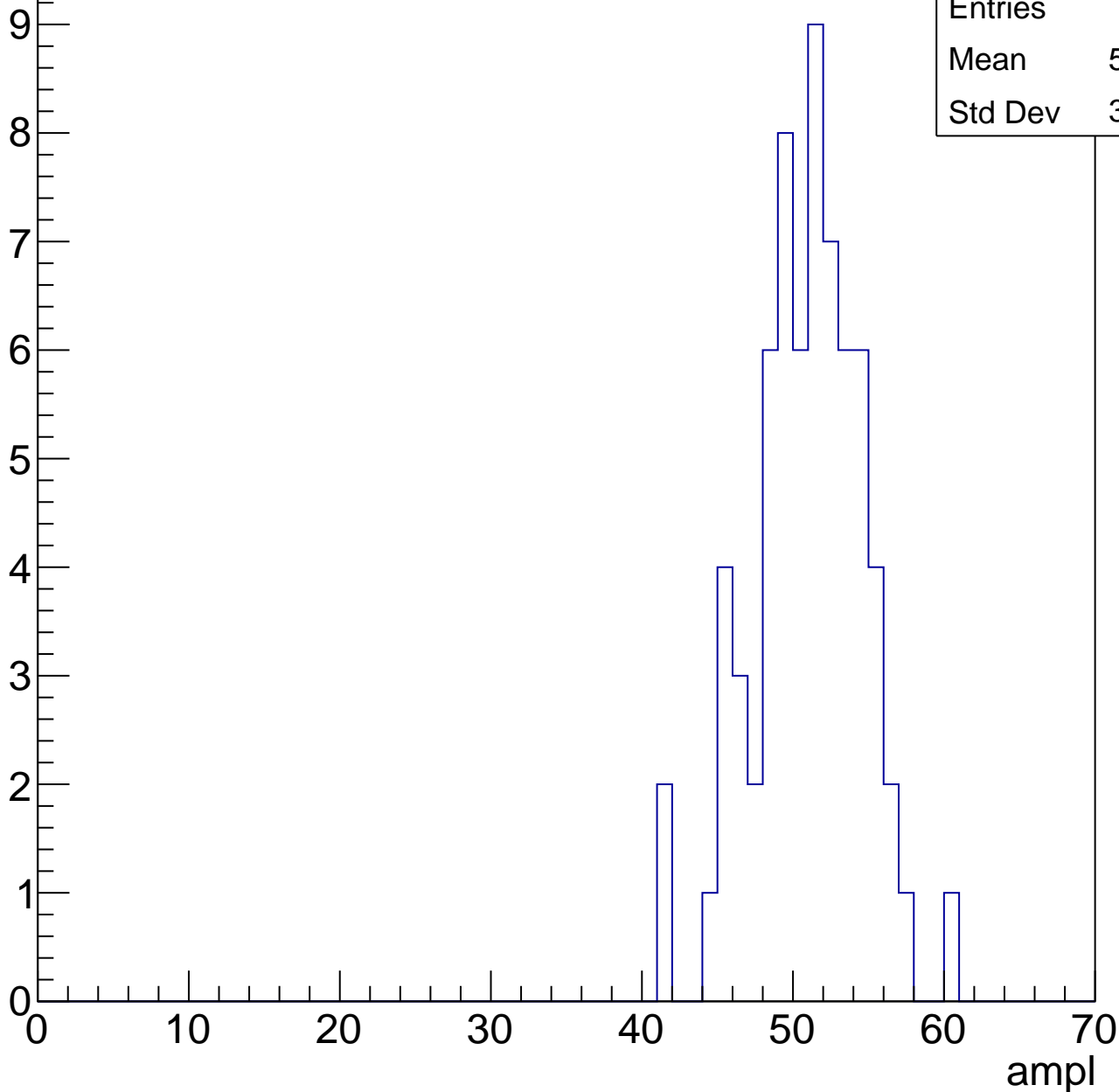


# B0L001S, U2-ch89, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

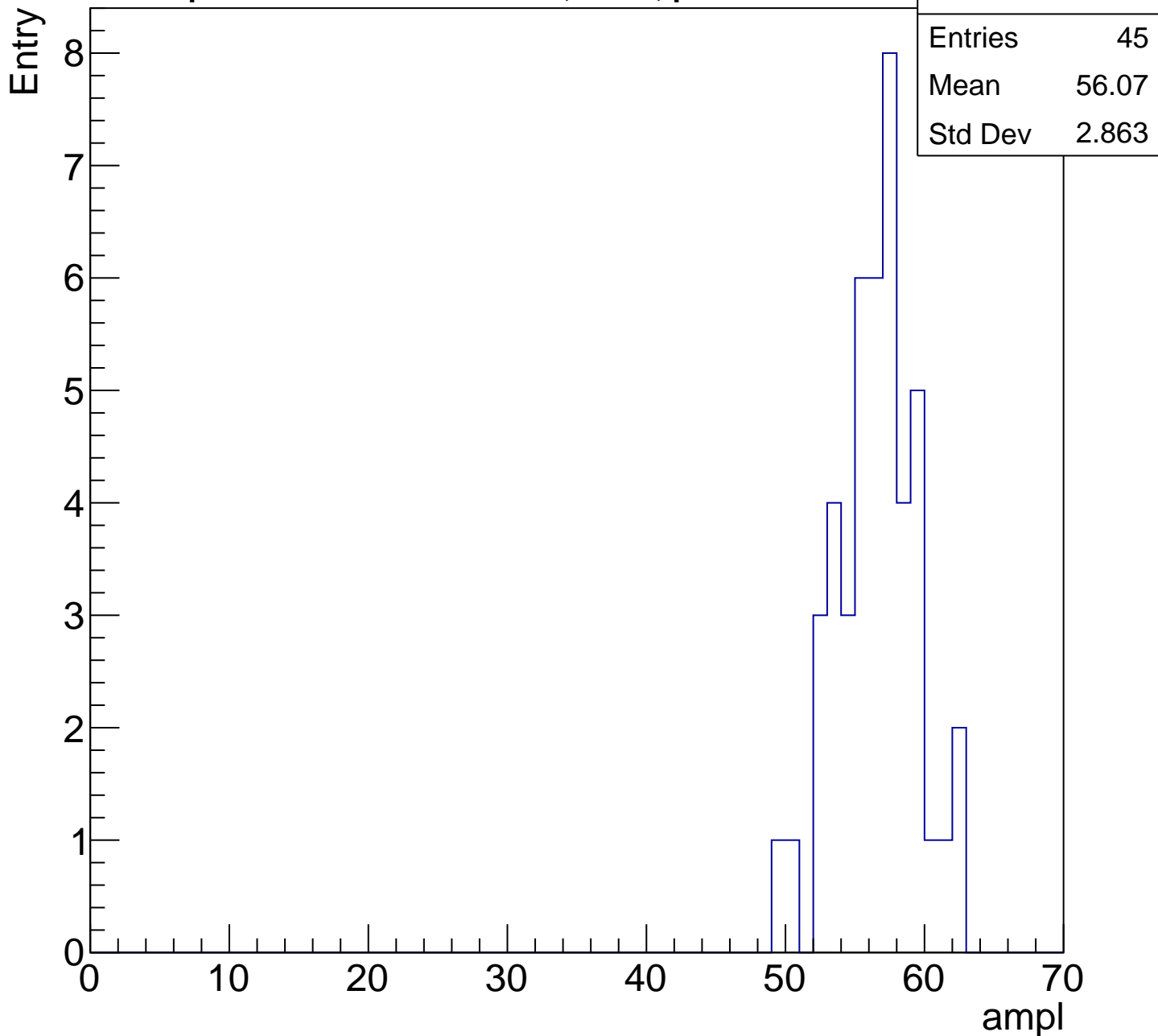
Entry

|         |       |
|---------|-------|
| Entries | 68    |
| Mean    | 50.47 |
| Std Dev | 3.616 |



# B0L001S, U2-ch89, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U2-ch89, adc5

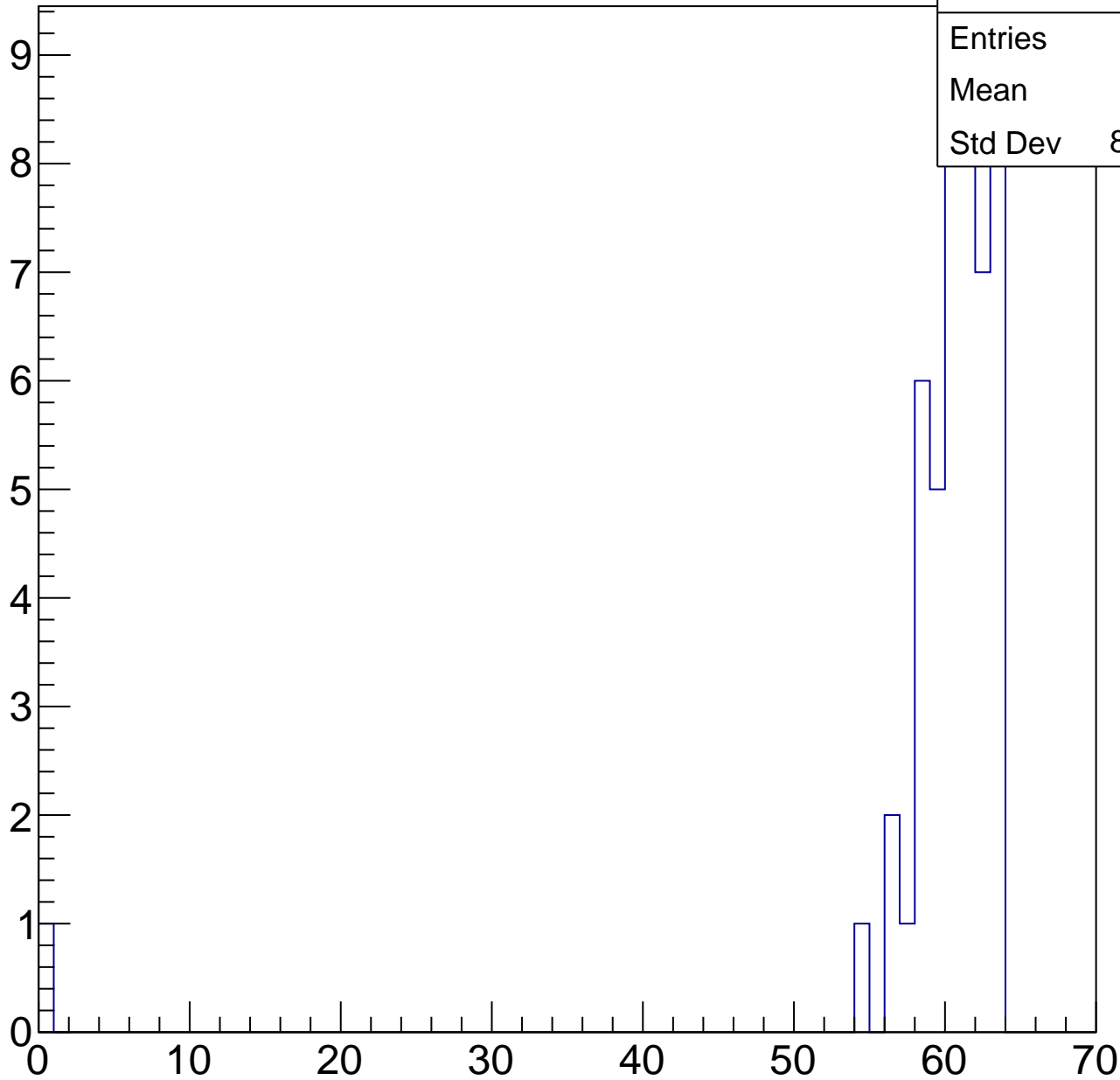
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

|         |       |
|---------|-------|
| Entries | 49    |
| Mean    | 59.1  |
| Std Dev | 8.788 |

ampl



# B0L001S, U2-ch89, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch89, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 0 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch90, adc0

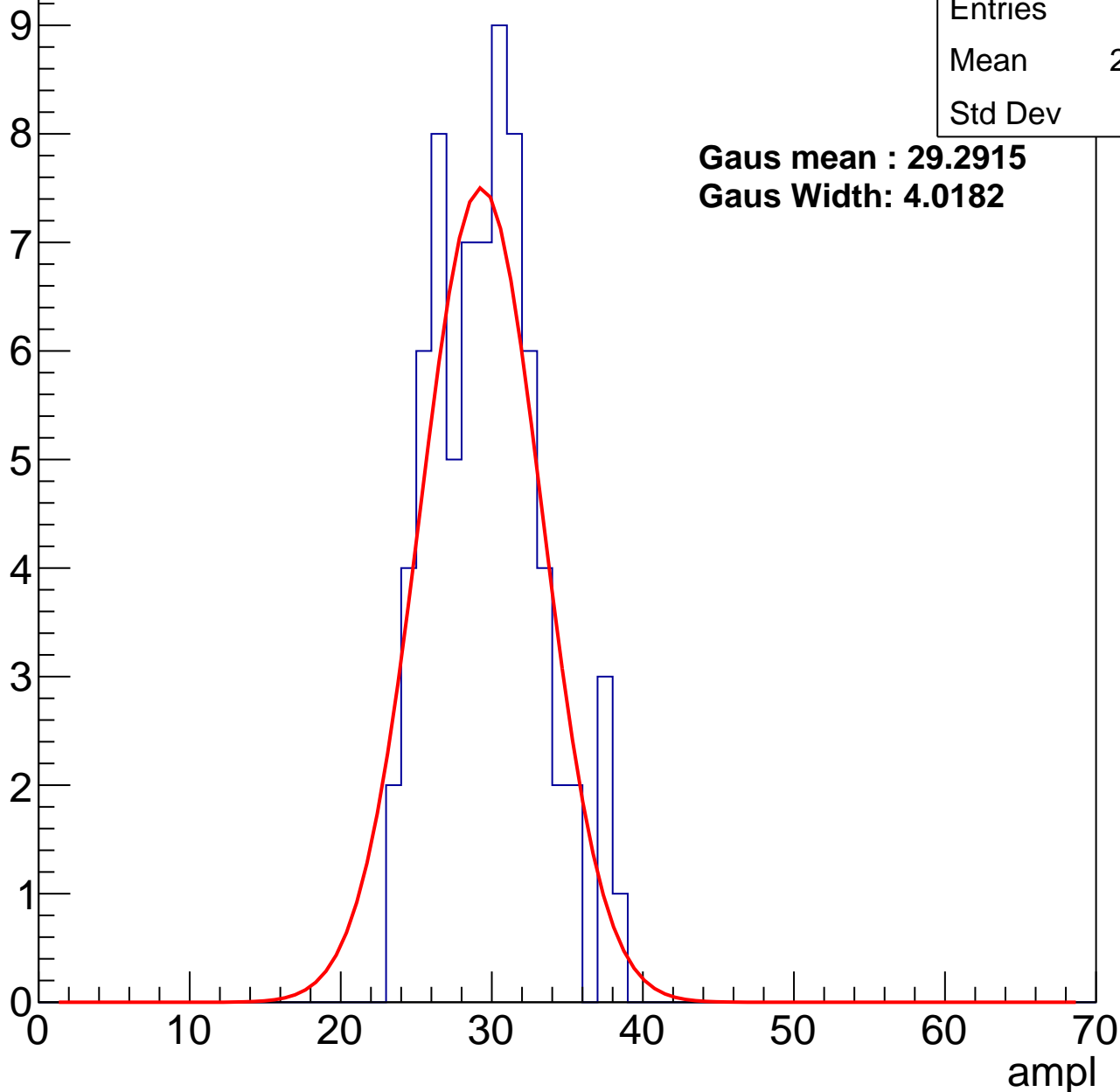
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 74    |
| Mean    | 29.23 |
| Std Dev | 3.52  |

**Gaus mean : 29.2915**

**Gaus Width: 4.0182**



# B0L001S, U2-ch90, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 64    |
| Mean    | 35.8  |
| Std Dev | 3.322 |

**Gaus mean : 36.6378**

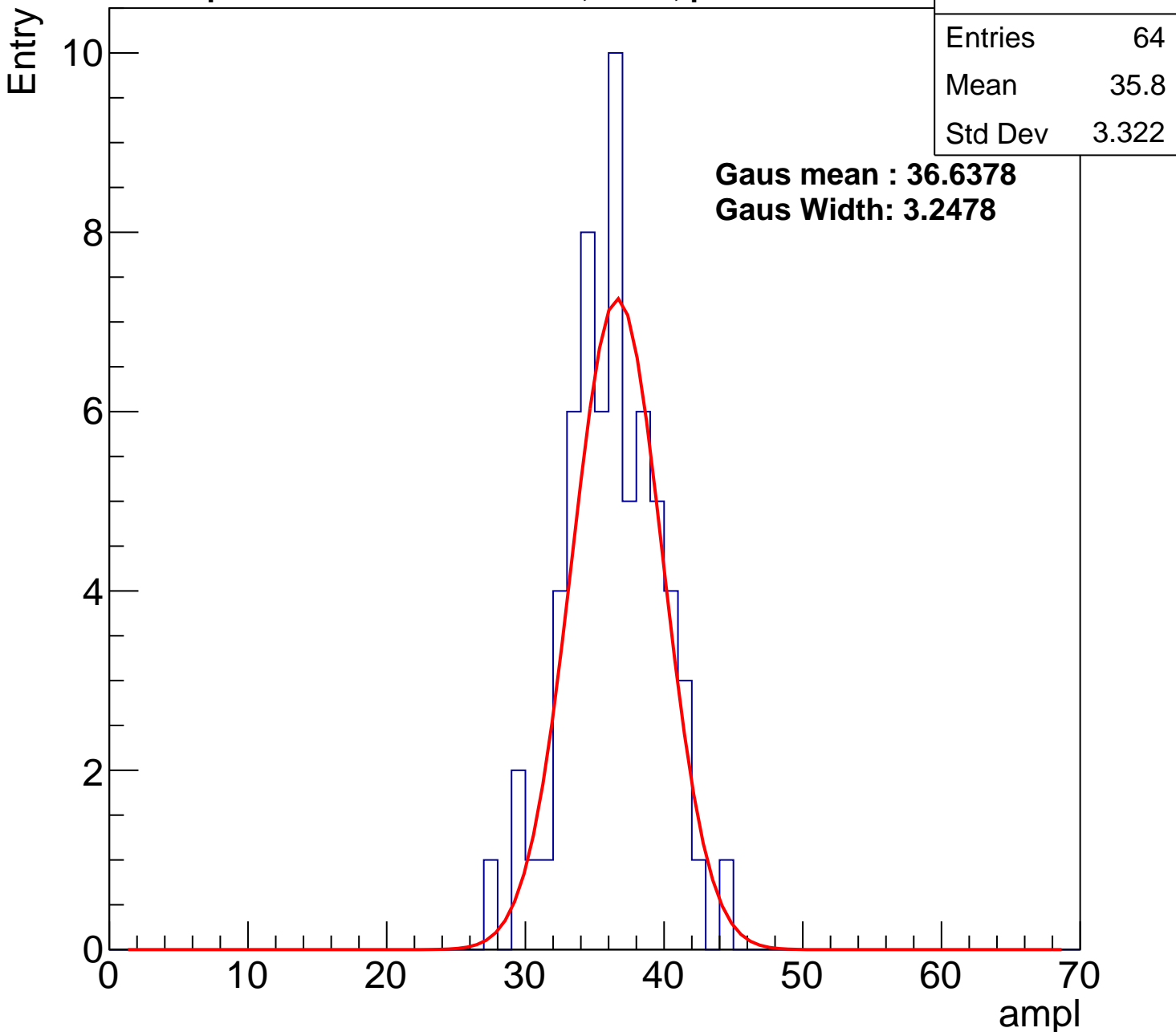
**Gaus Width: 3.2478**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B0L001S, U2-ch90, adc2

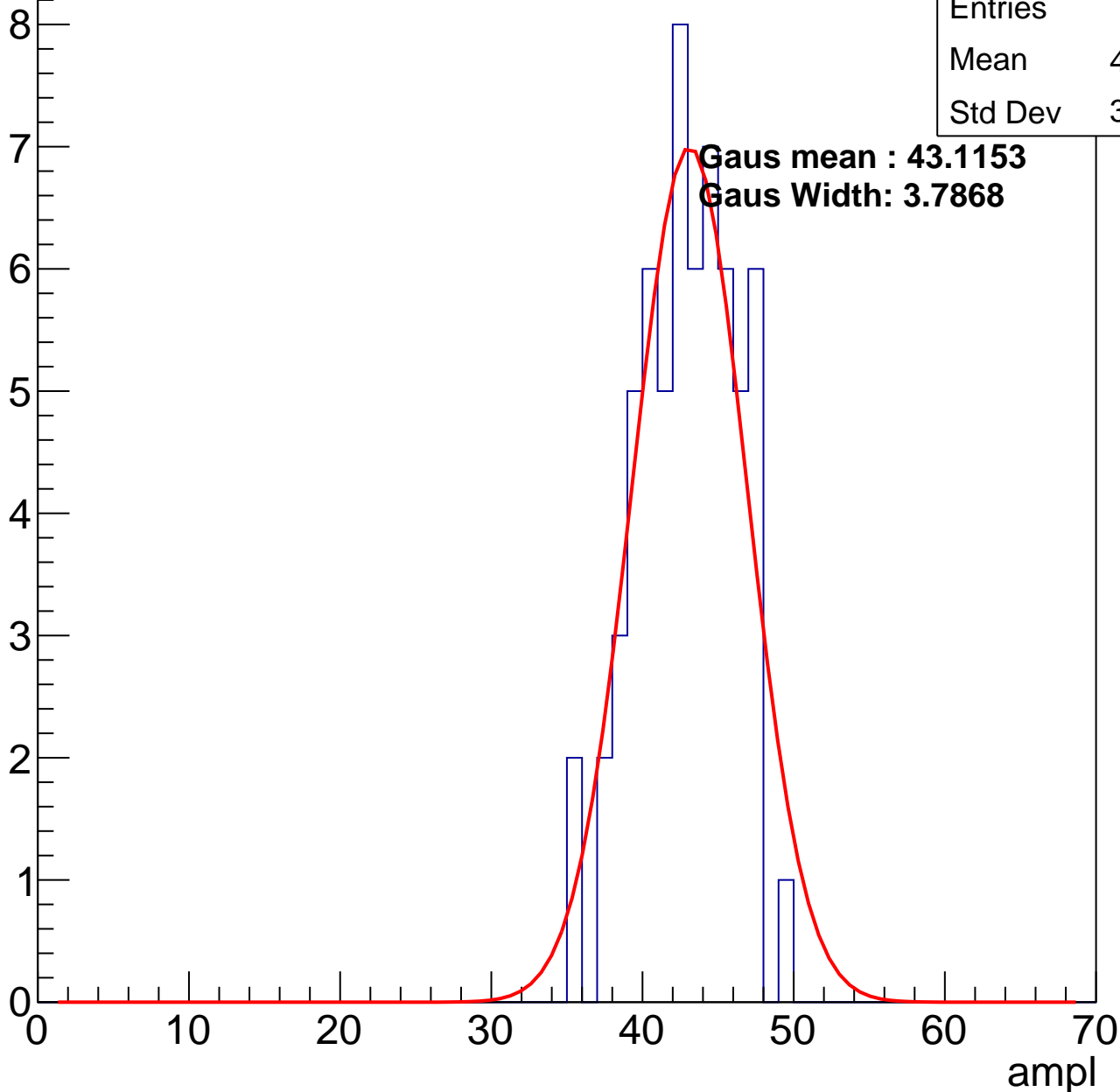
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 62    |
| Mean    | 42.44 |
| Std Dev | 3.176 |

**Gaus mean : 43.1153**

**Gaus Width: 3.7868**

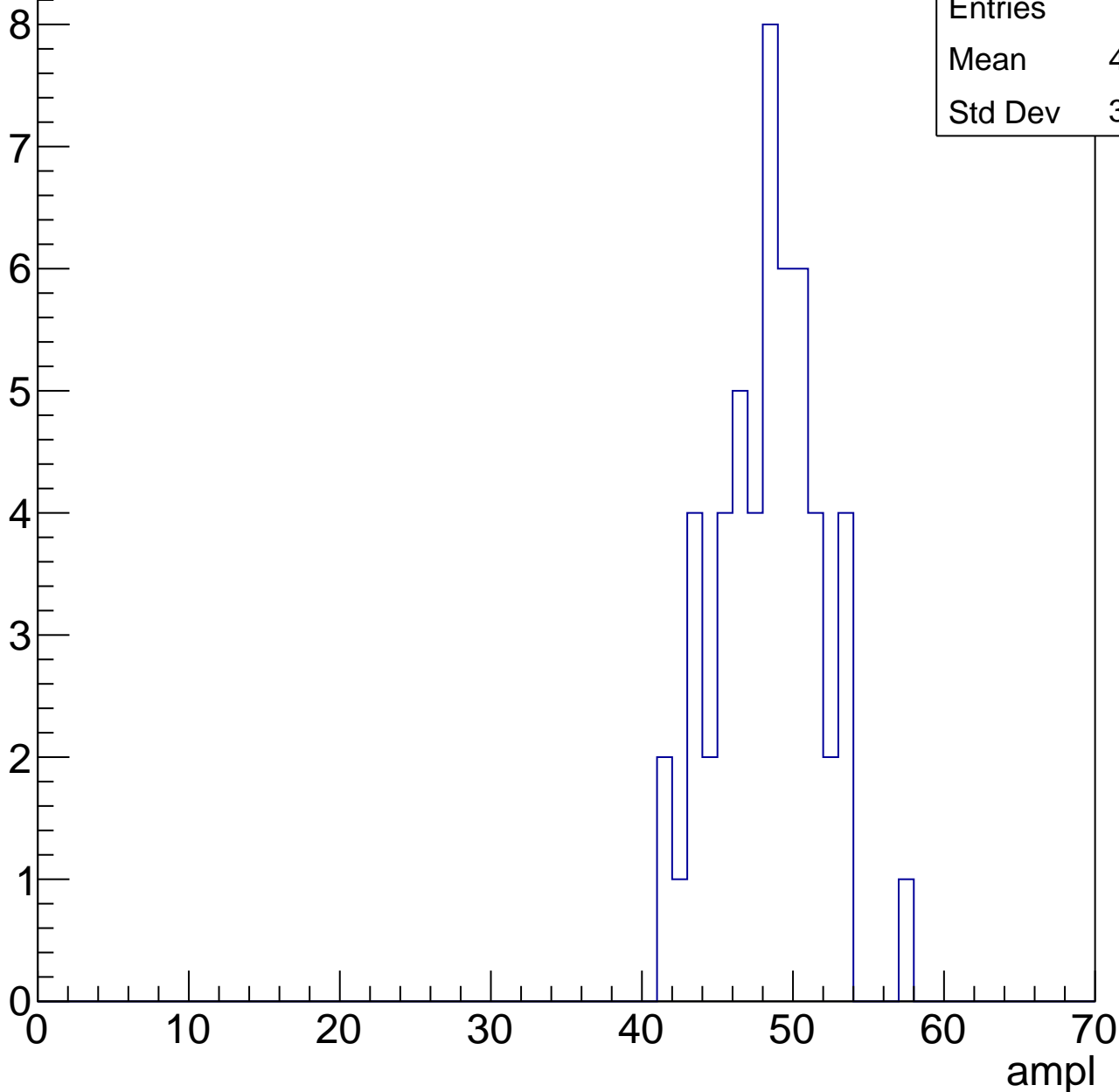


# B0L001S, U2-ch90, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 53    |
| Mean    | 47.87 |
| Std Dev | 3.376 |

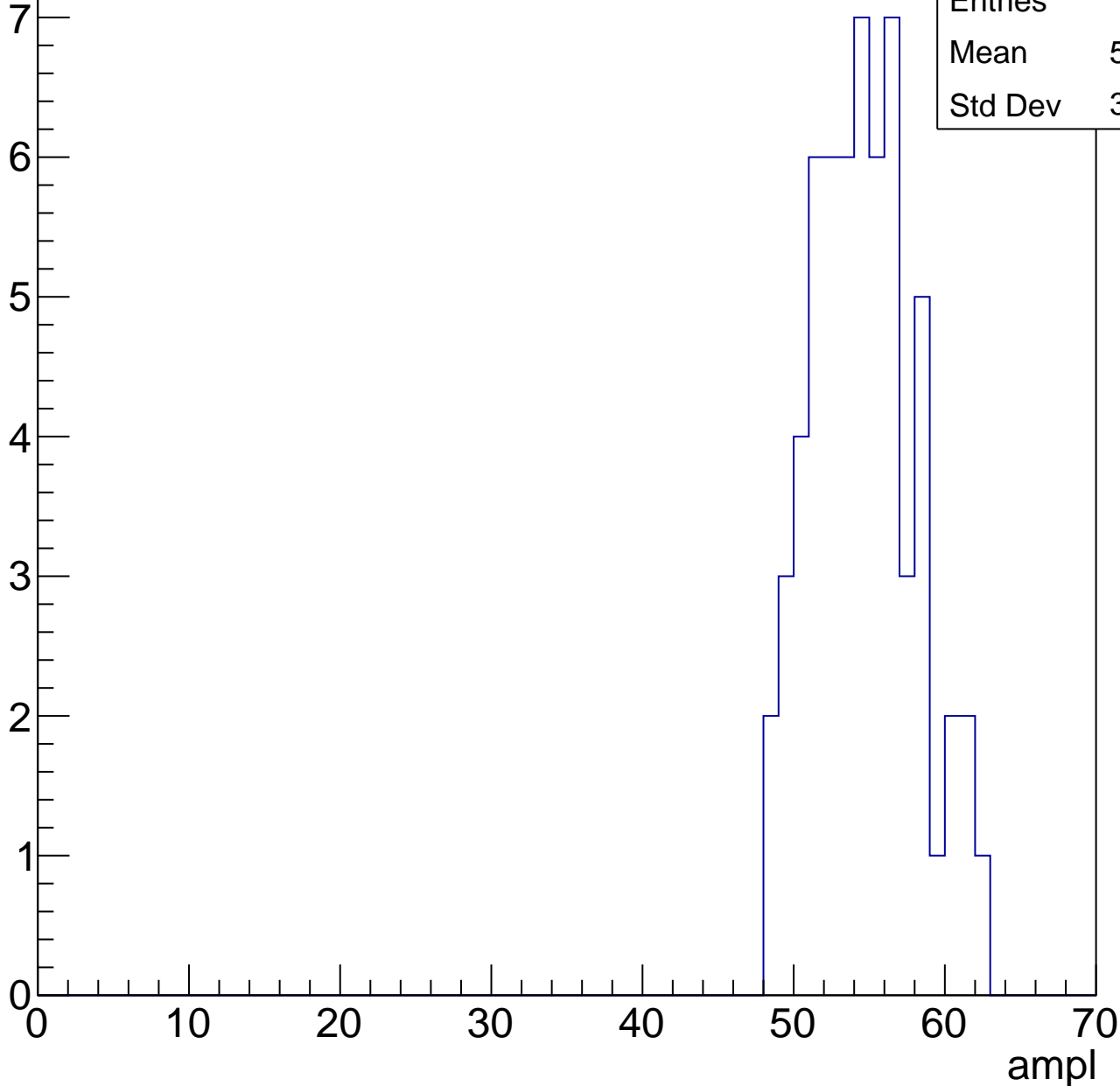


# B0L001S, U2-ch90, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

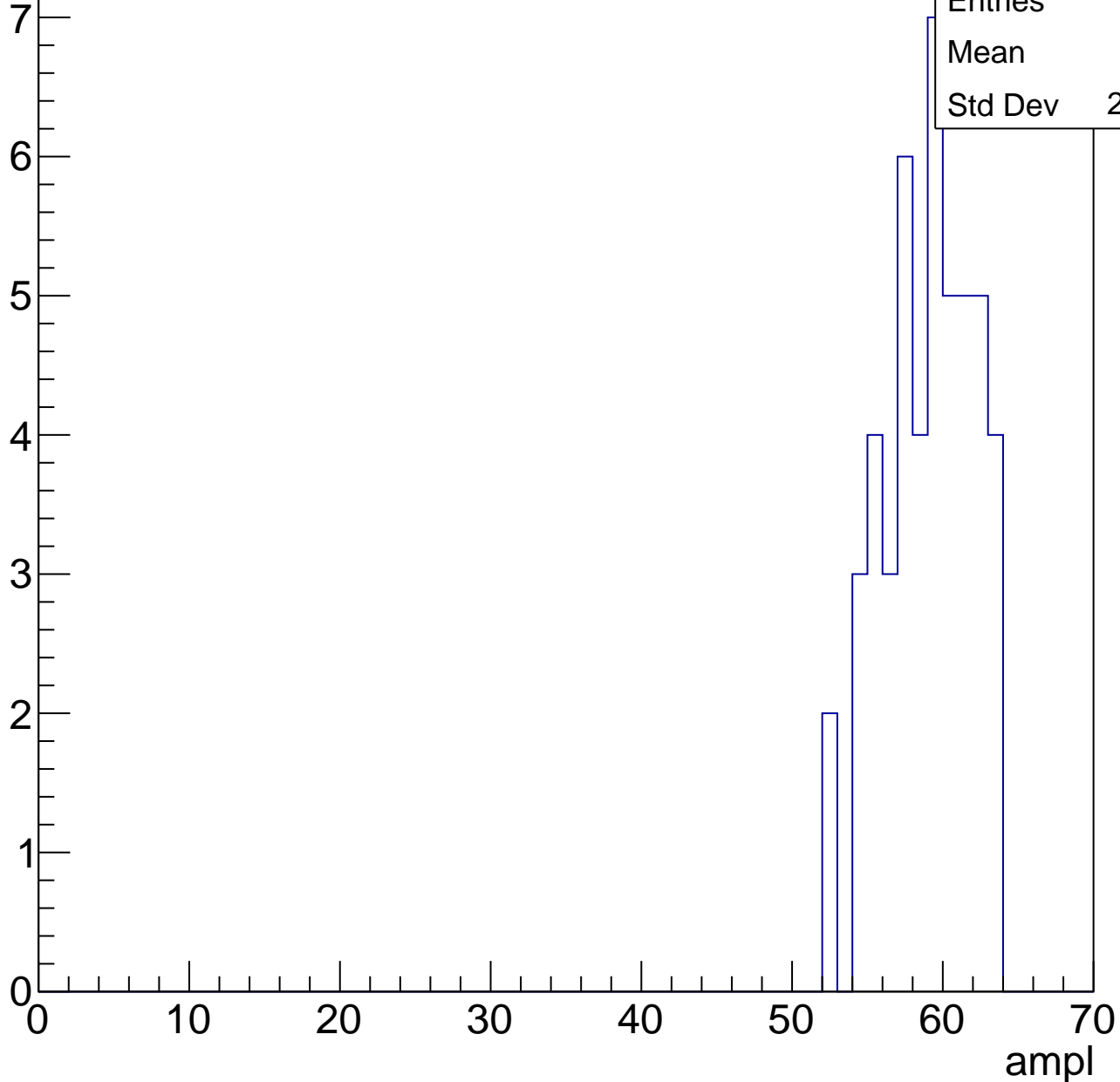
|         |       |
|---------|-------|
| Entries | 61    |
| Mean    | 54.15 |
| Std Dev | 3.372 |



# B0L001S, U2-ch90, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

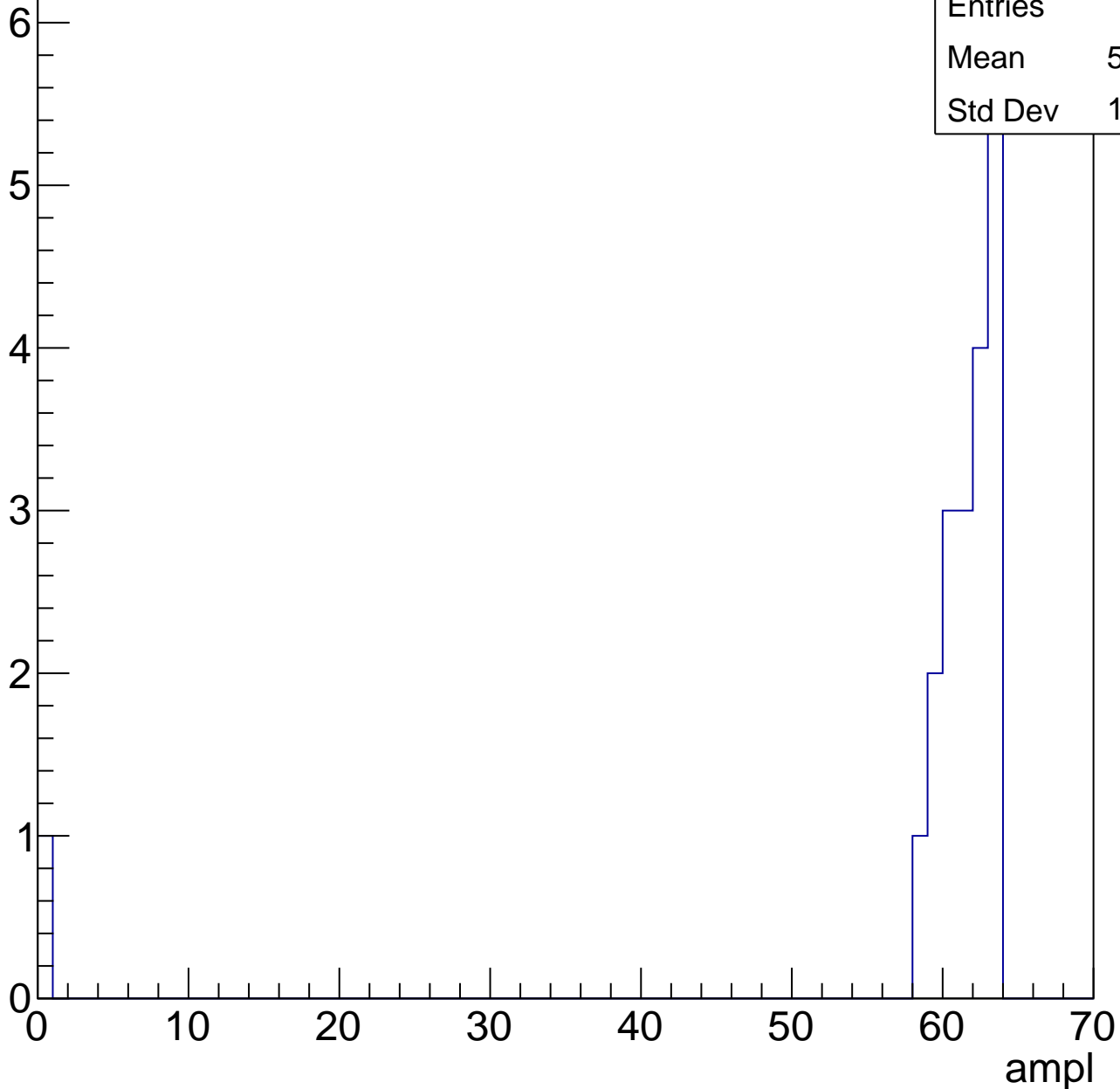


# B0L001S, U2-ch90, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 20    |
| Mean    | 58.25 |
| Std Dev | 13.45 |





# B0L001S, U2-ch90, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 0 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch91, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 75    |
| Mean    | 29.84 |
| Std Dev | 5.031 |

**Gaus mean : 30.8676**

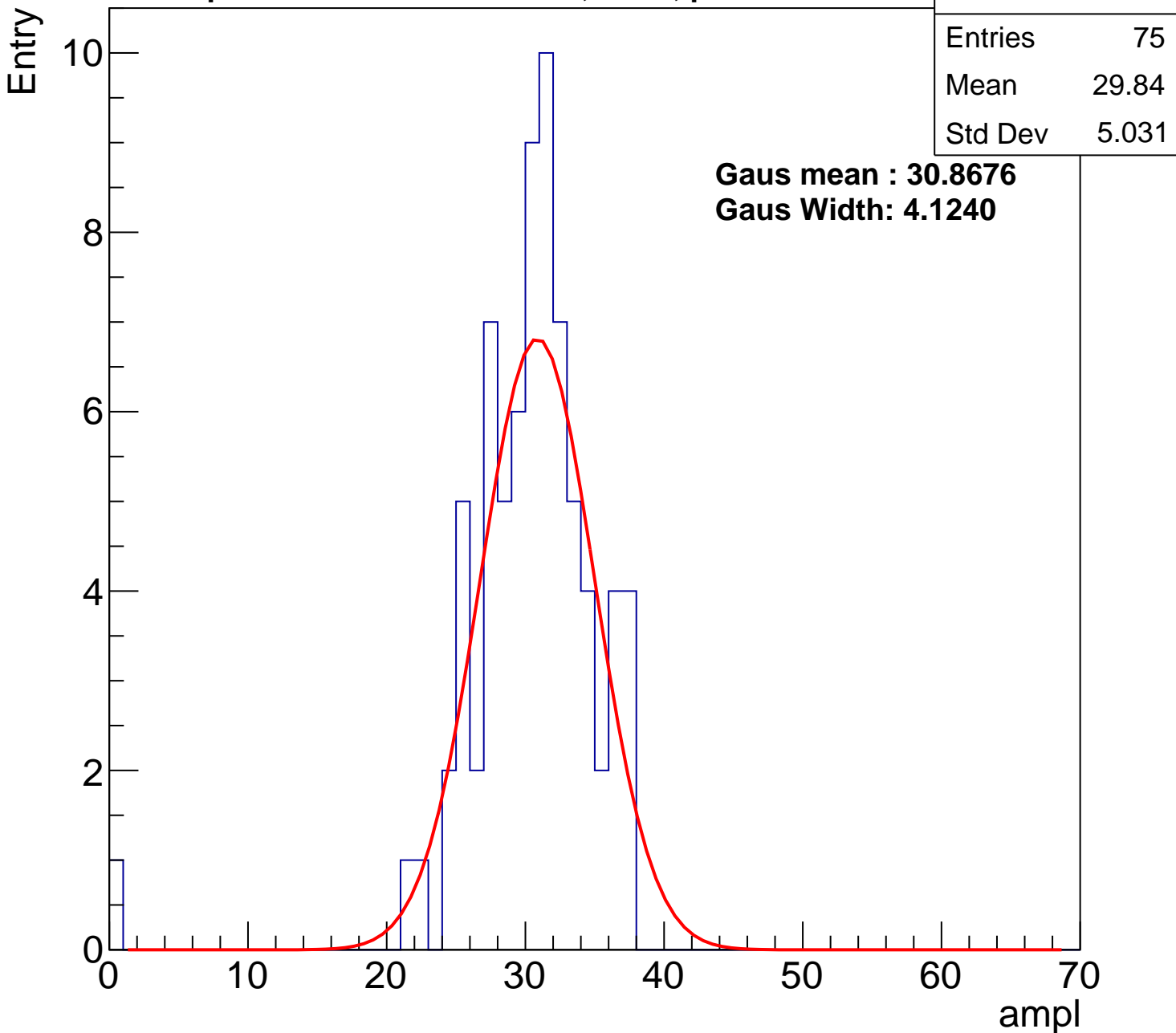
**Gaus Width: 4.1240**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U2-ch91, adc1

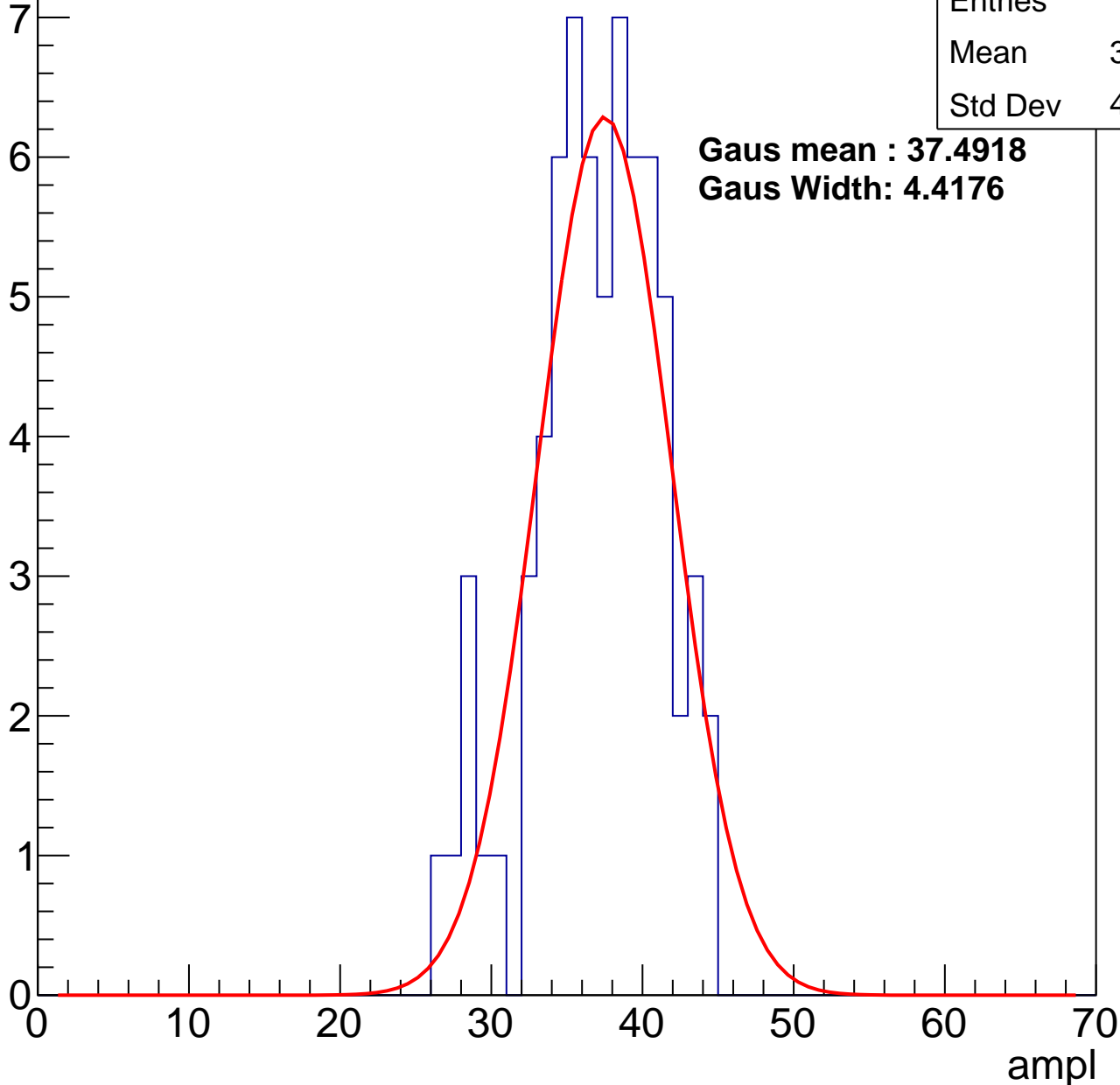
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 69    |
| Mean    | 36.52 |
| Std Dev | 4.186 |

**Gaus mean : 37.4918**

**Gaus Width: 4.4176**



# B0L001S, U2-ch91, adc2

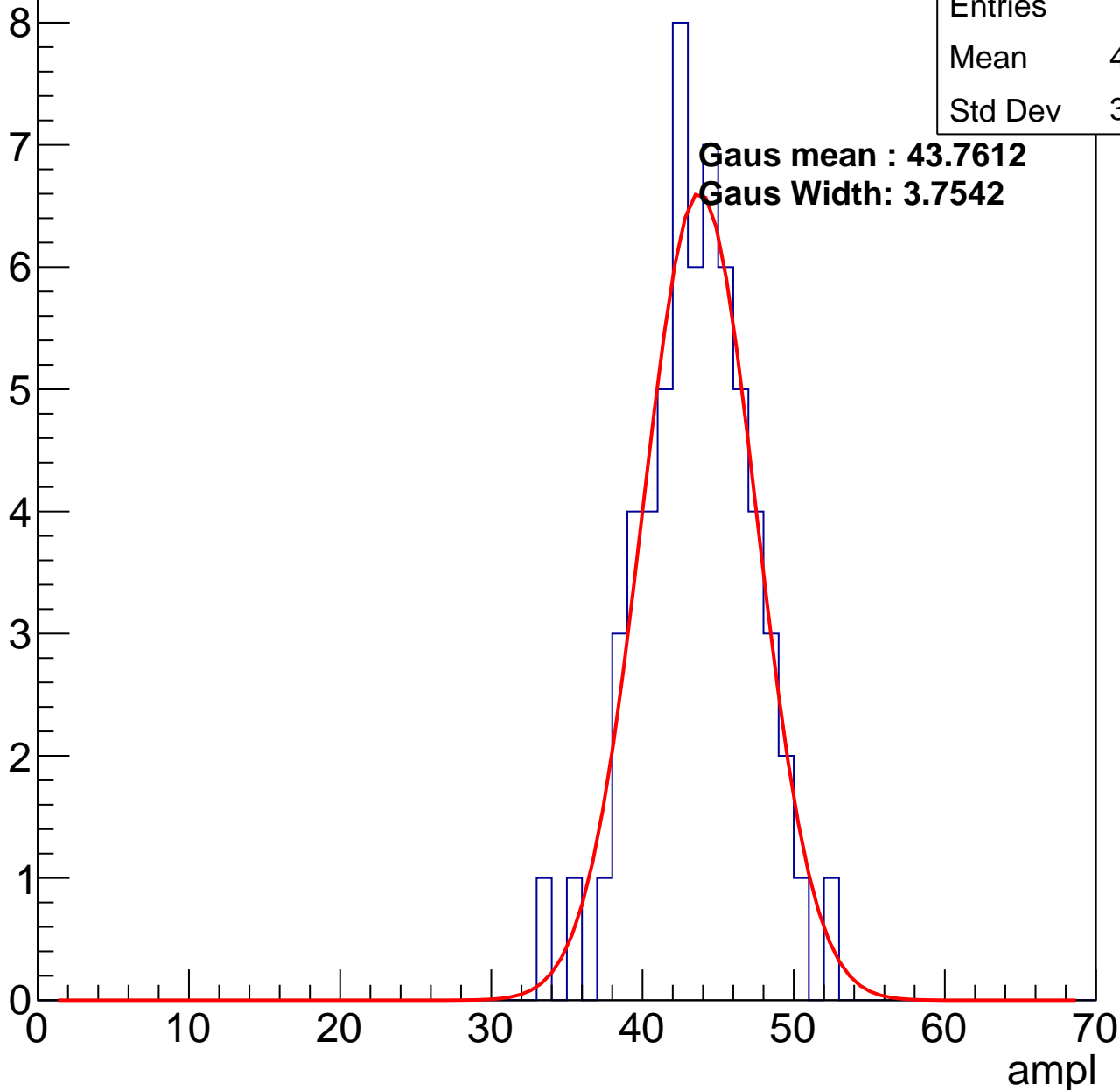
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 62    |
| Mean    | 43.13 |
| Std Dev | 3.634 |

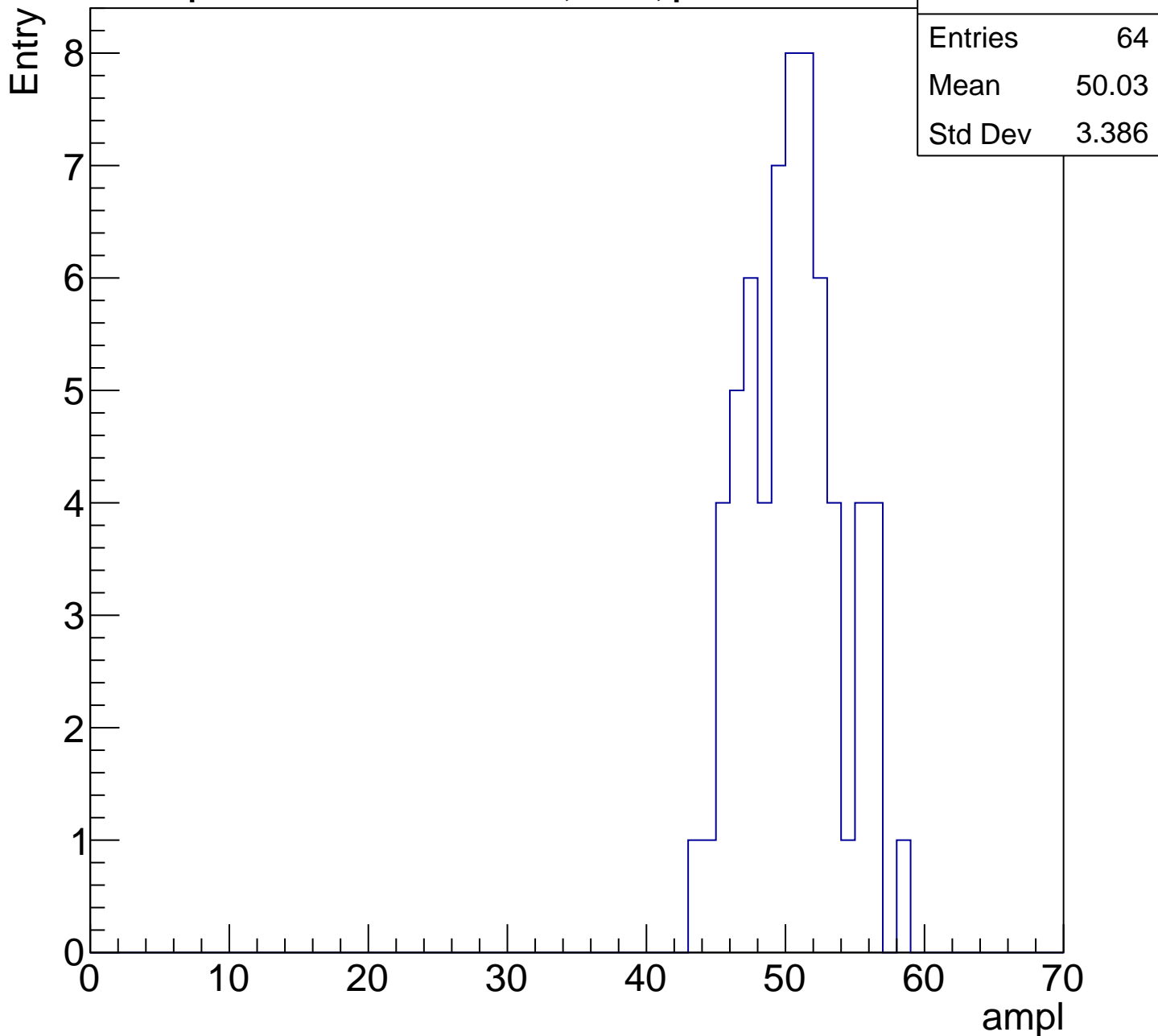
**Gaus mean : 43.7612**

**Gaus Width: 3.7542**



# B0L001S, U2-ch91, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

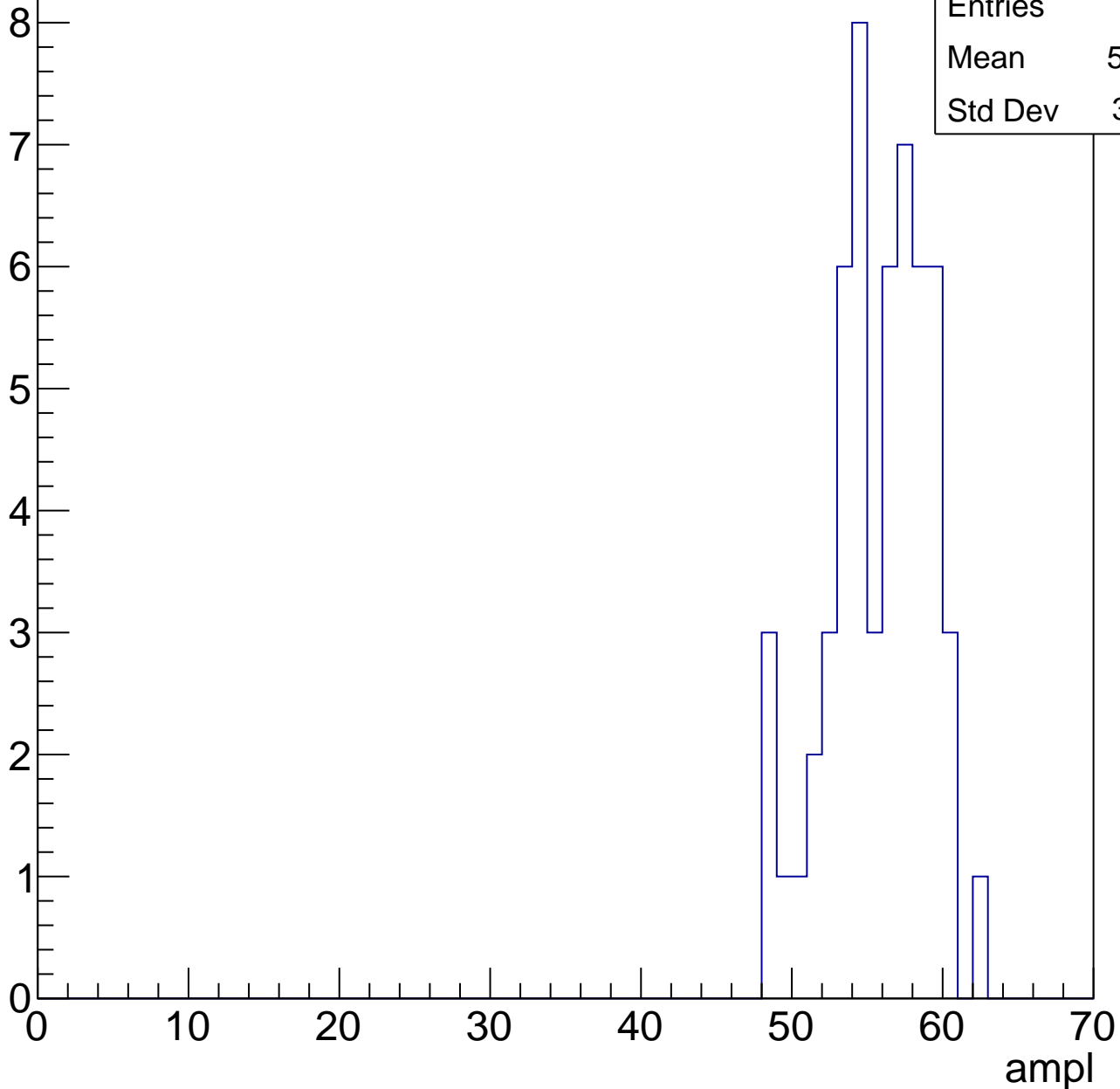


# B0L001S, U2-ch91, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

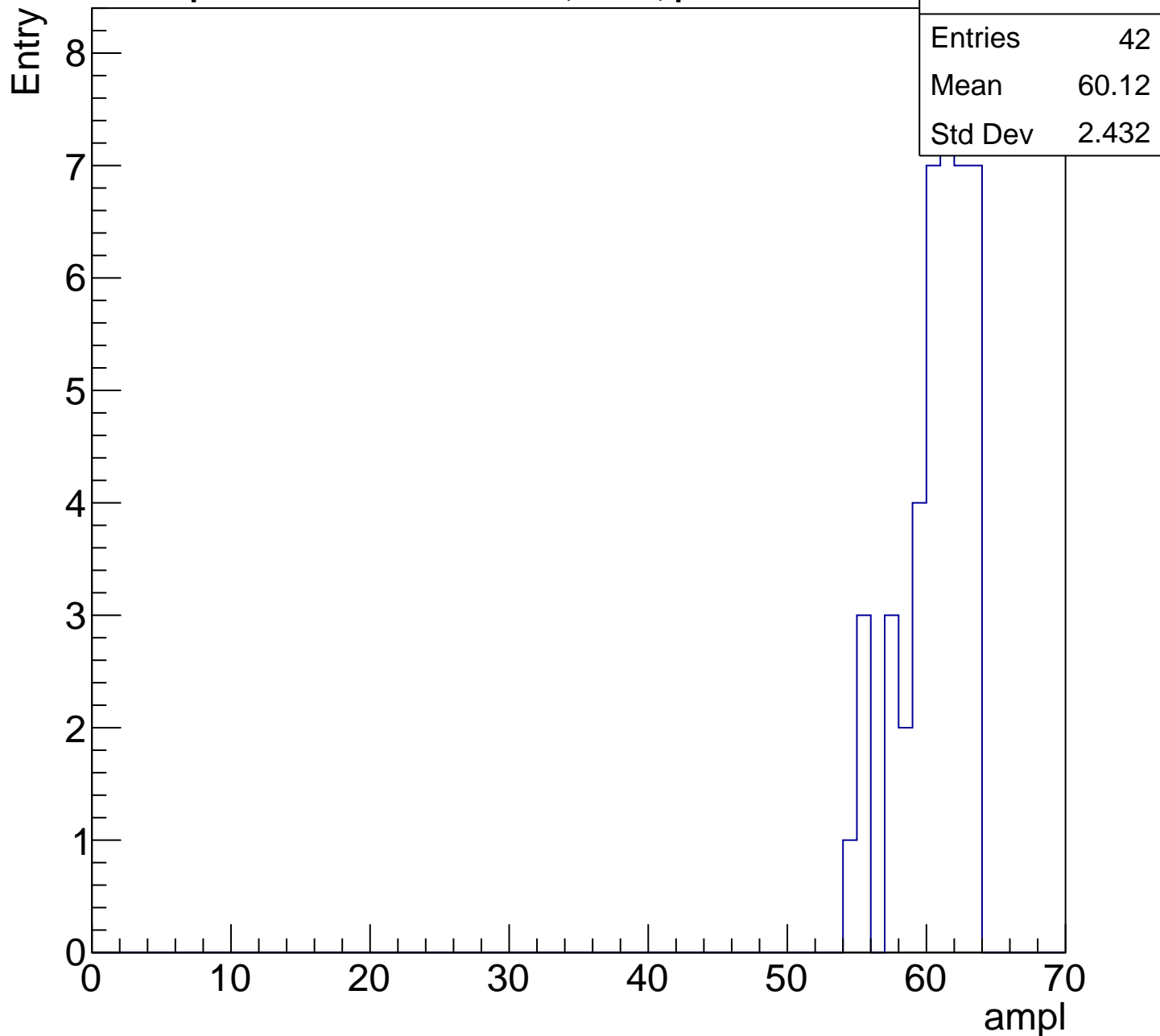
Entry

|         |       |
|---------|-------|
| Entries | 56    |
| Mean    | 55.27 |
| Std Dev | 3.281 |



# B0L001S, U2-ch91, adc5

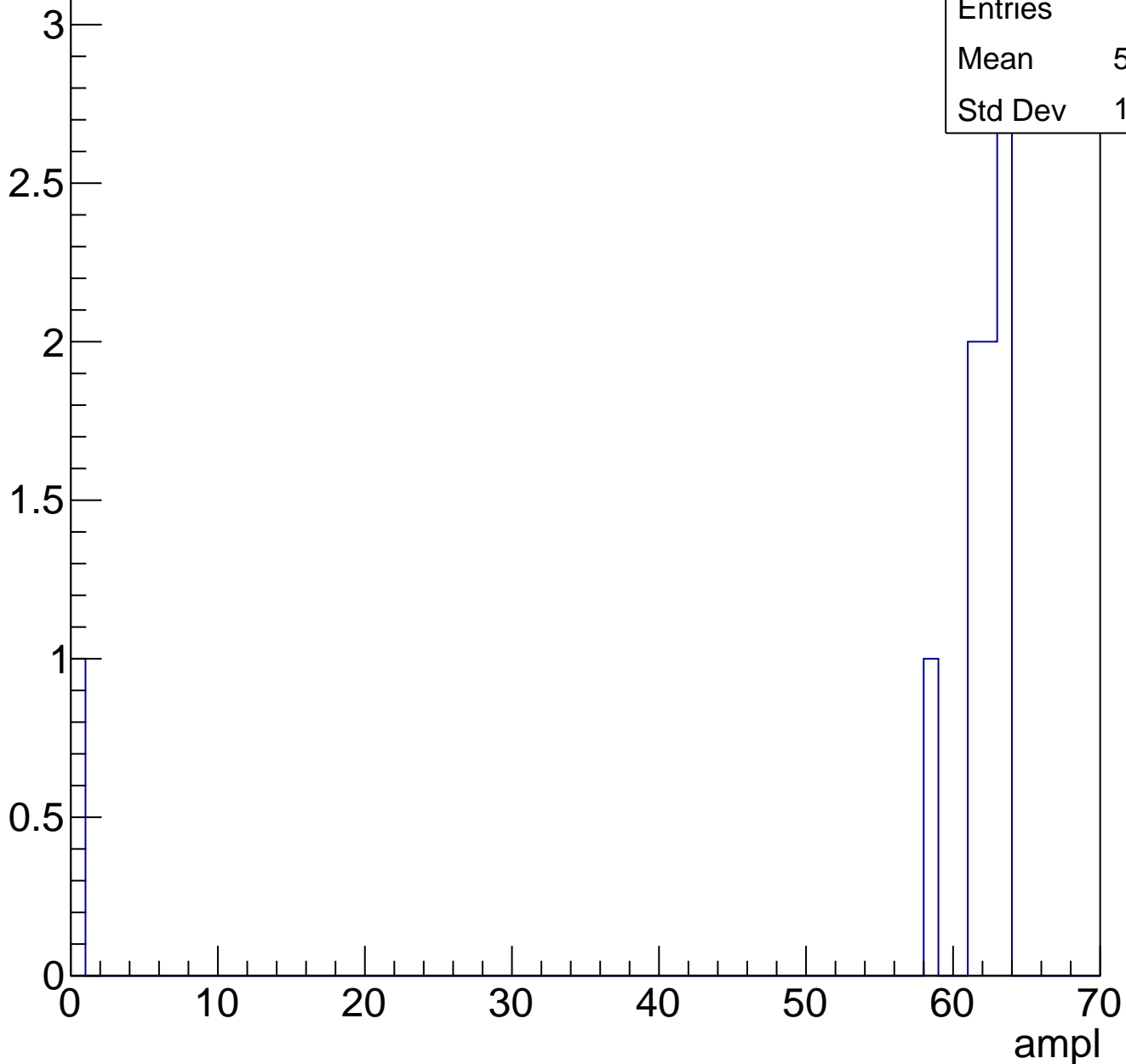
calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U2-ch91, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch91, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 0 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch92, adc0

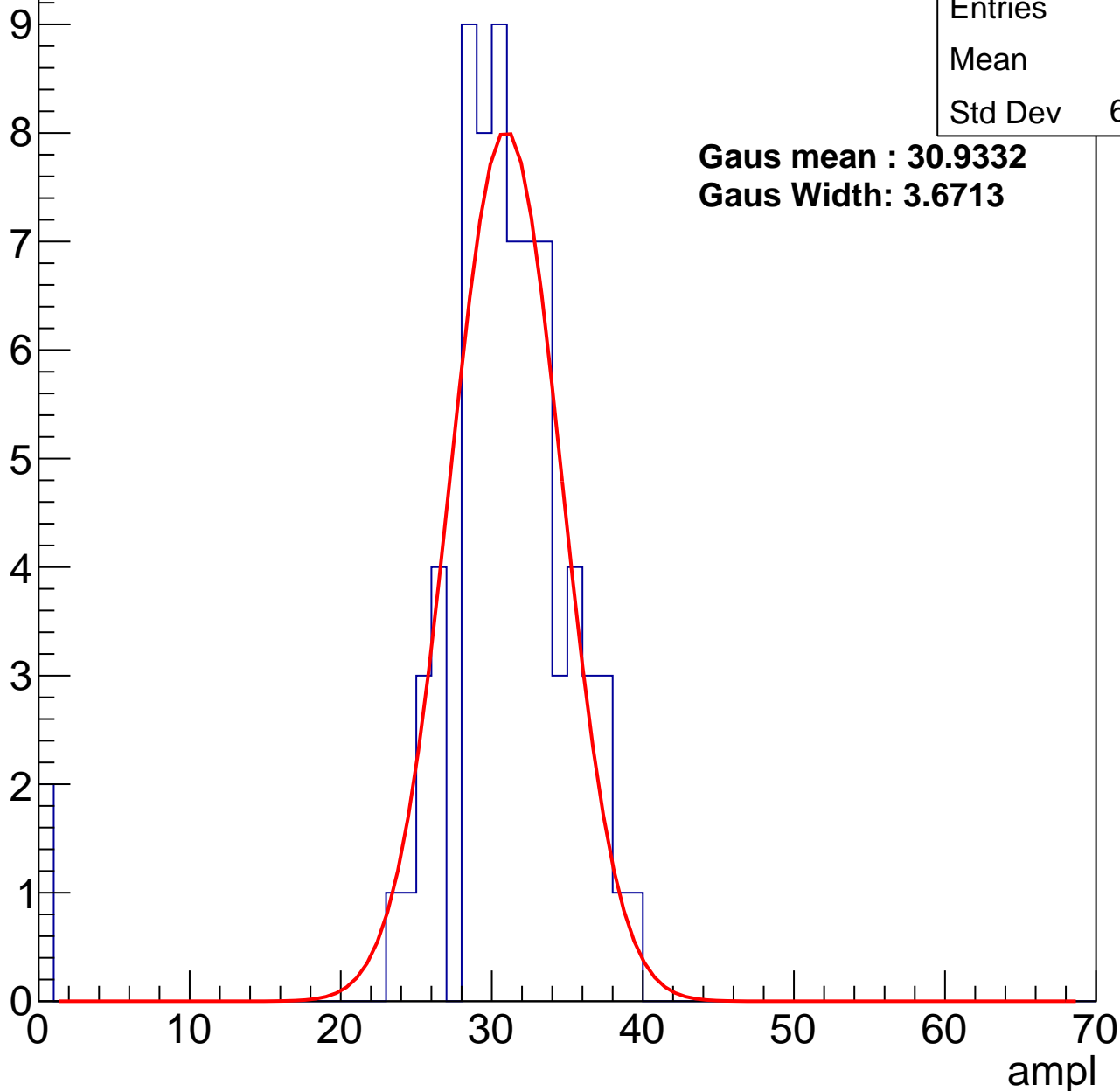
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 73    |
| Mean    | 30    |
| Std Dev | 6.097 |

**Gaus mean : 30.9332**

**Gaus Width: 3.6713**



# B0L001S, U2-ch92, adc1

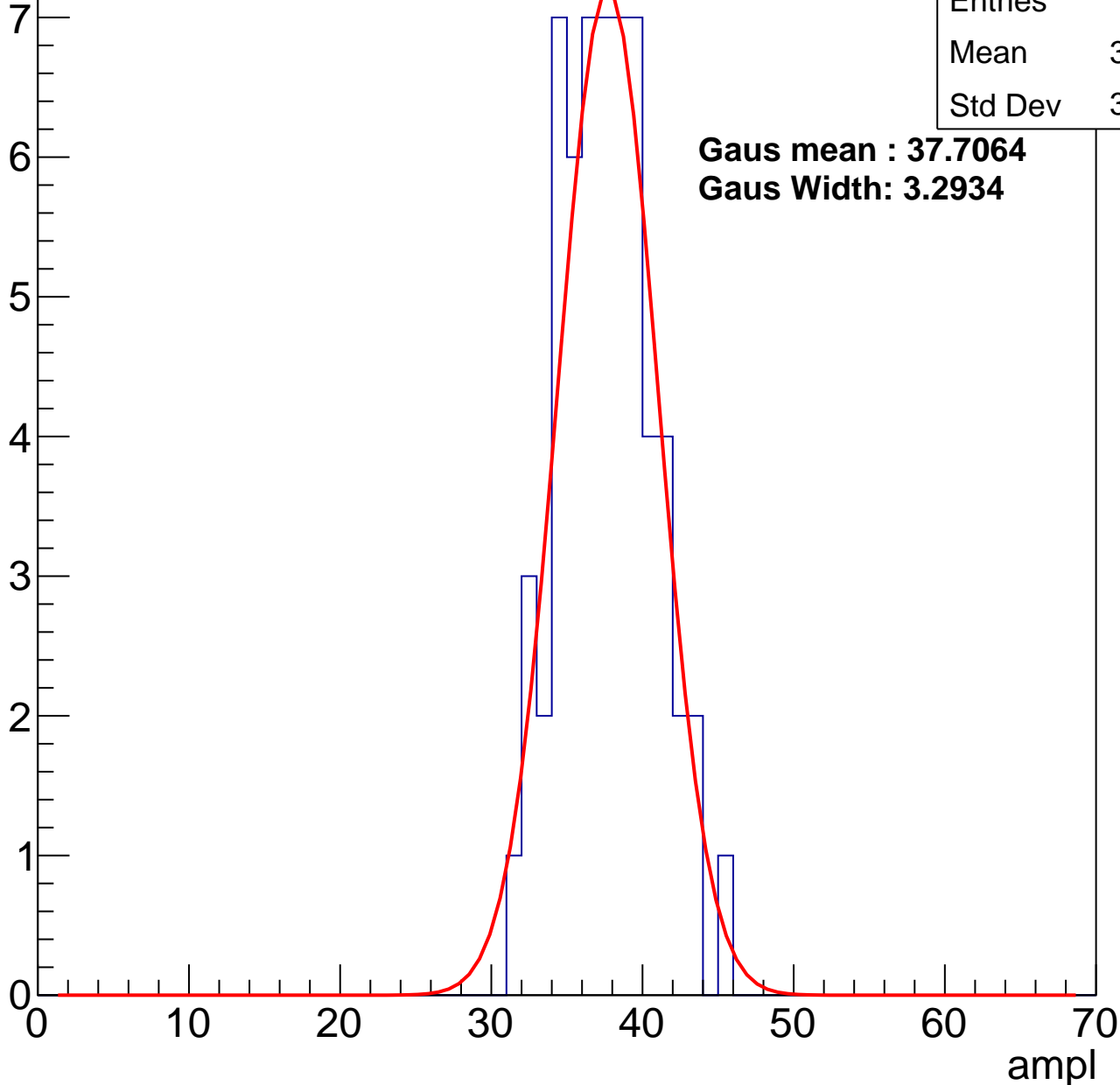
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 60    |
| Mean    | 37.17 |
| Std Dev | 3.045 |

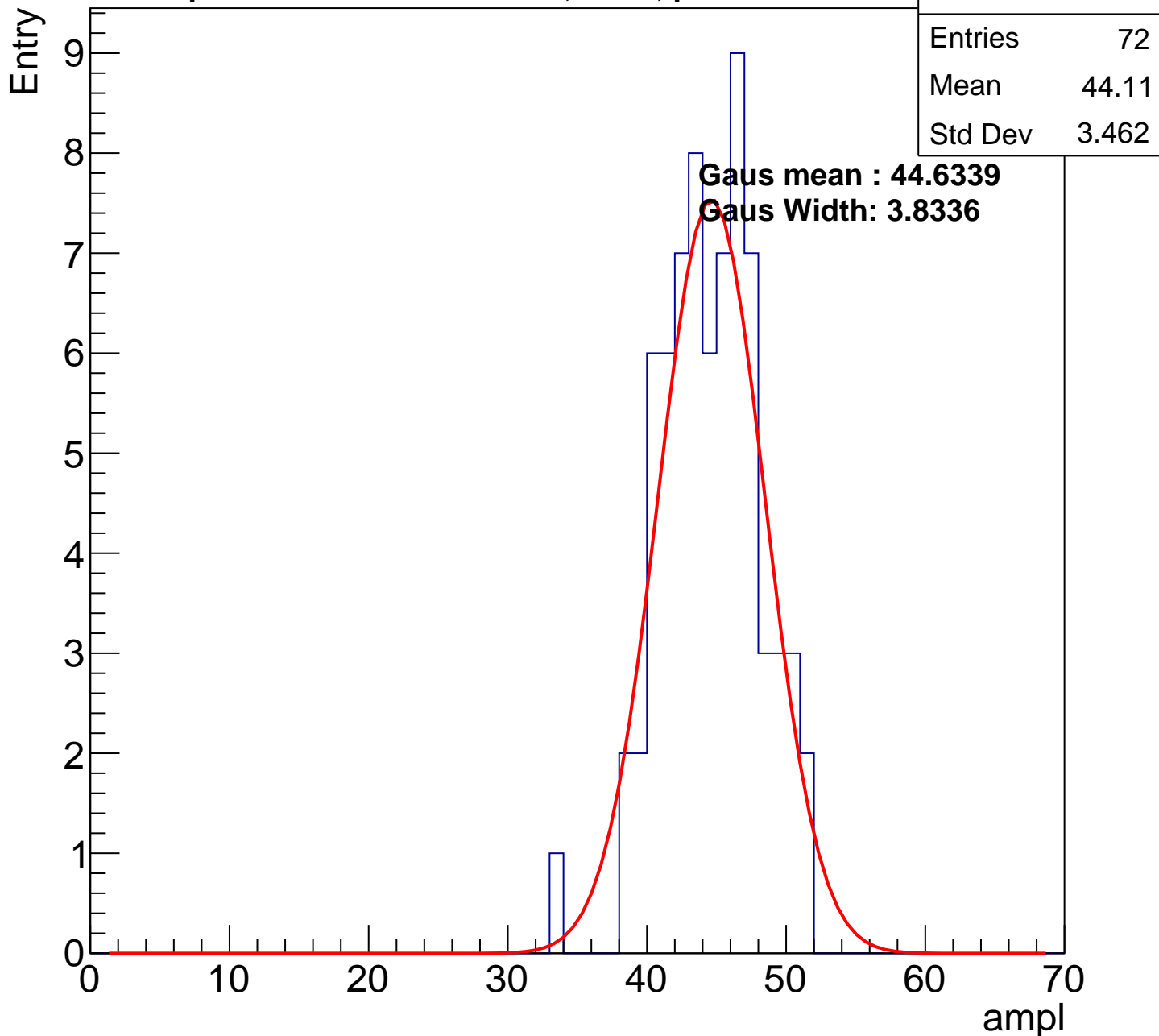
**Gaus mean : 37.7064**

**Gaus Width: 3.2934**



# B0L001S, U2-ch92, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

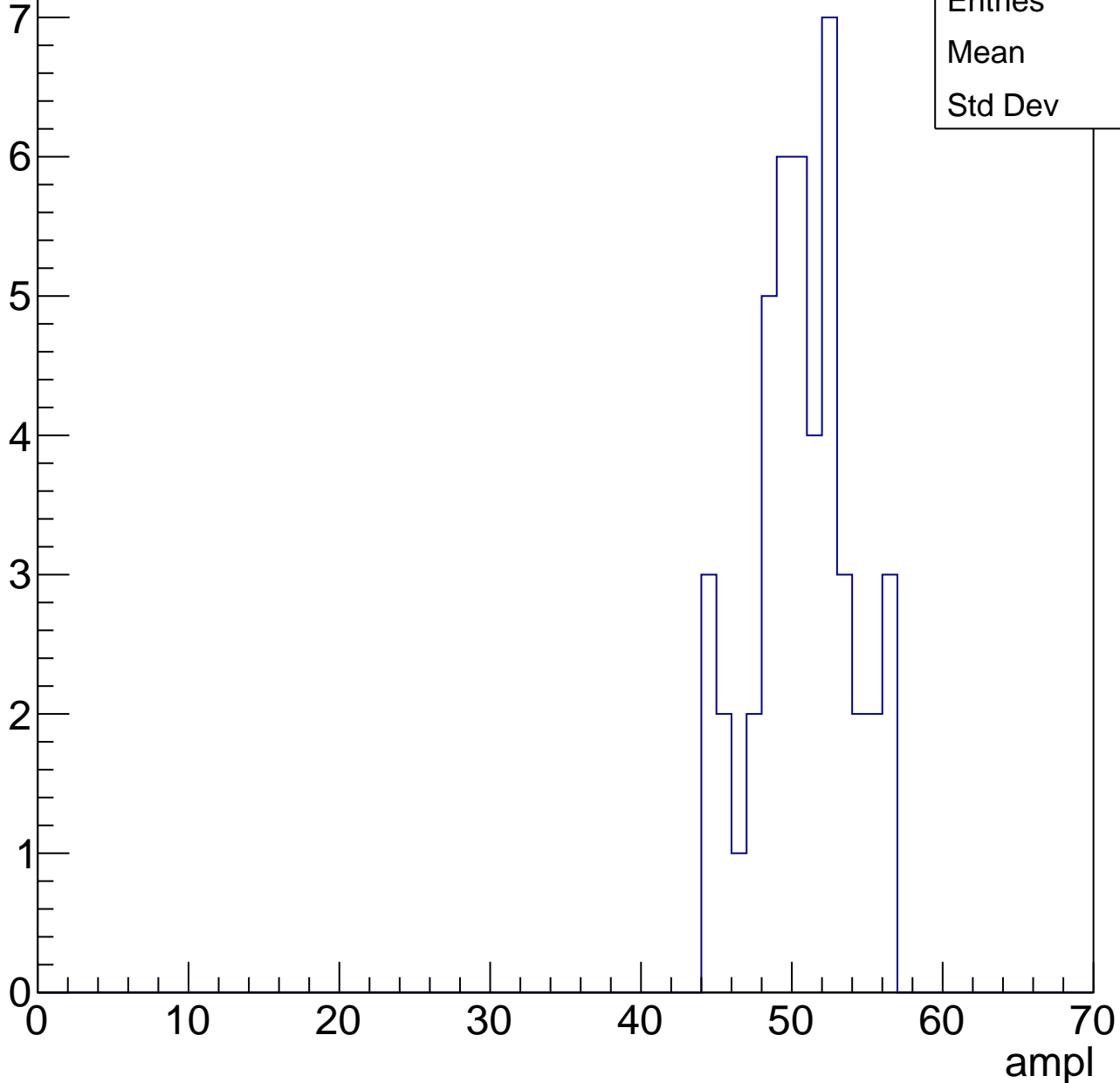


# B0L001S, U2-ch92, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |      |
|---------|------|
| Entries | 46   |
| Mean    | 50.2 |
| Std Dev | 3.18 |

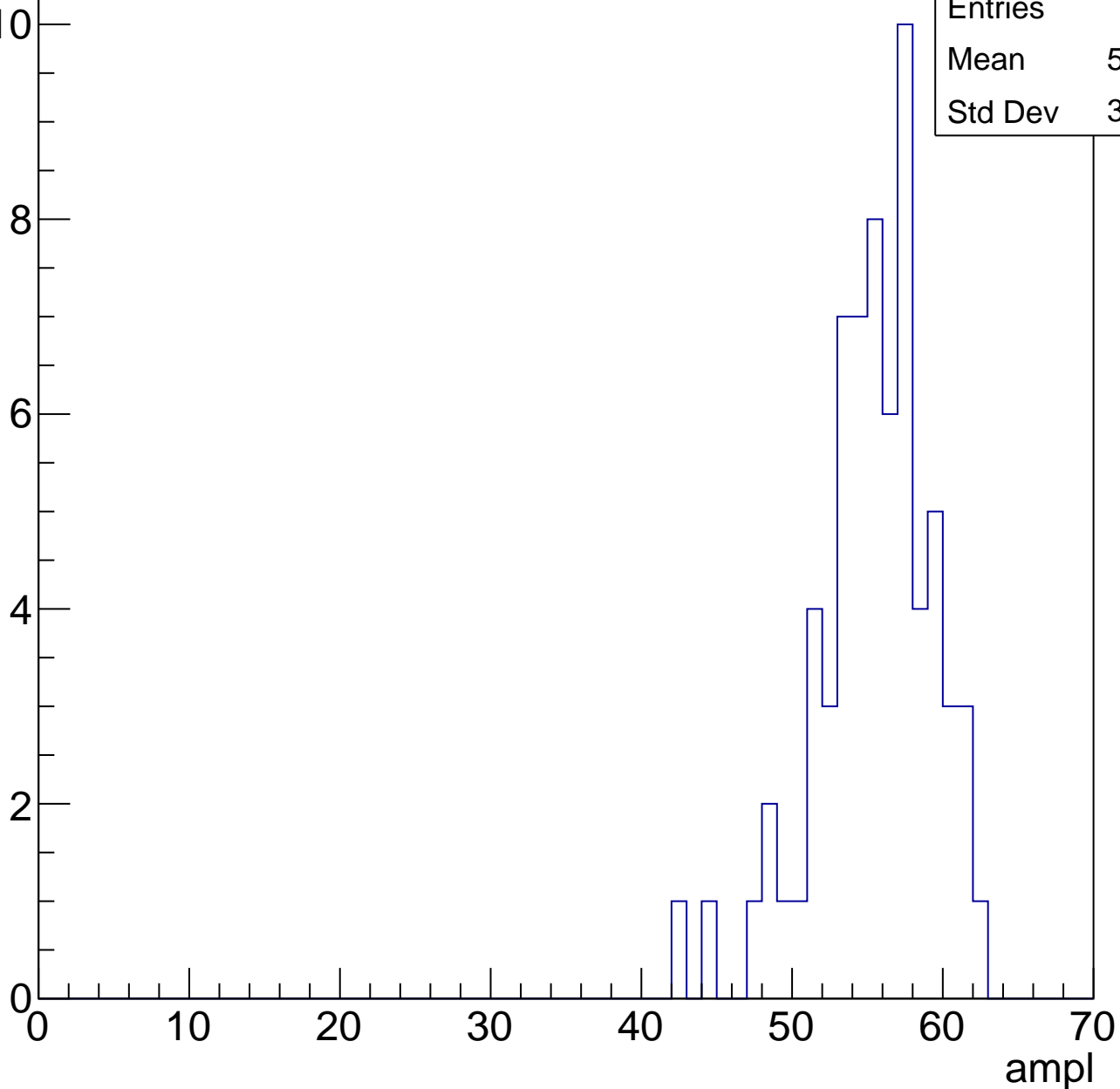


# B0L001S, U2-ch92, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 68    |
| Mean    | 54.93 |
| Std Dev | 3.897 |

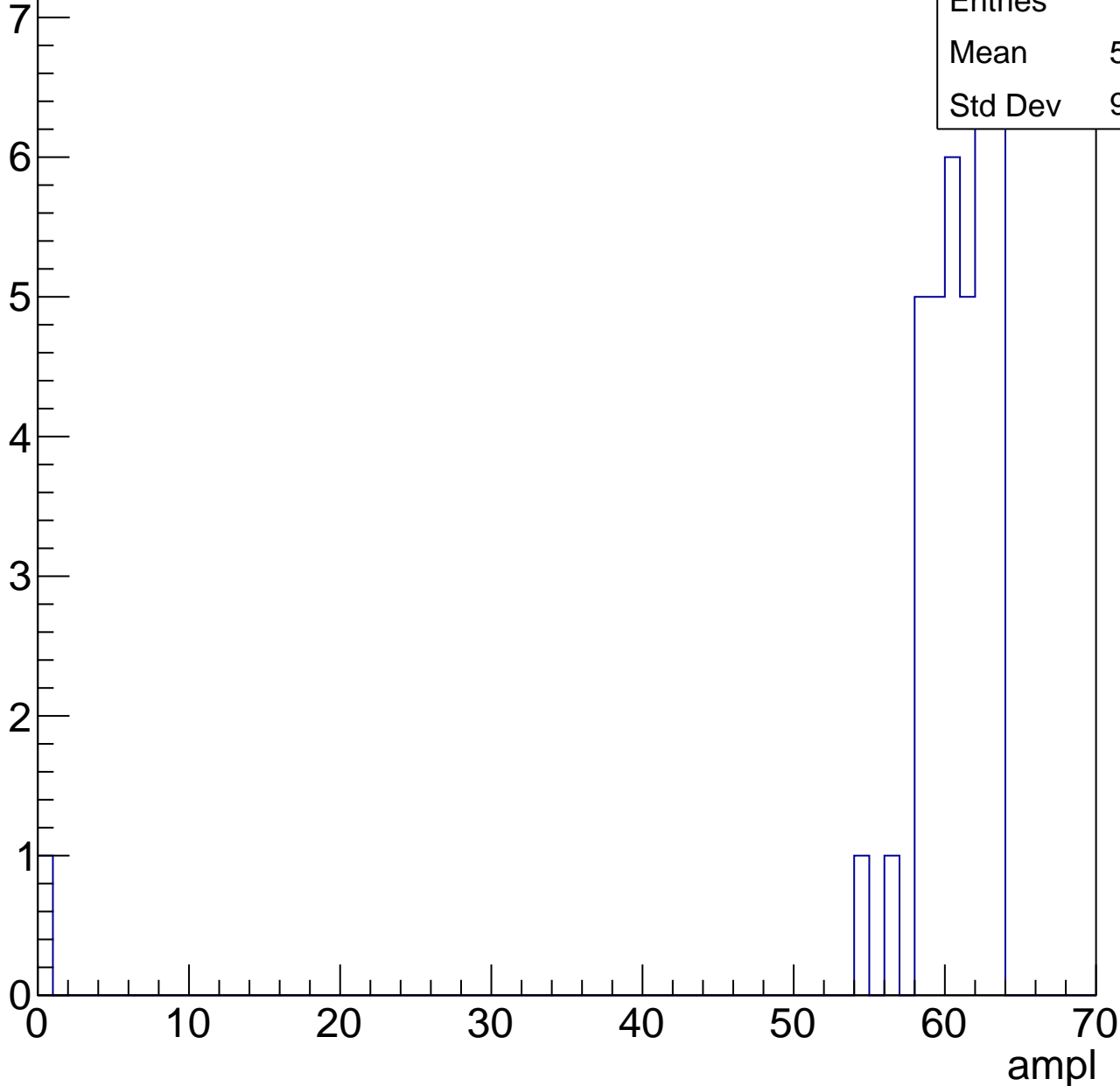


# B0L001S, U2-ch92, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

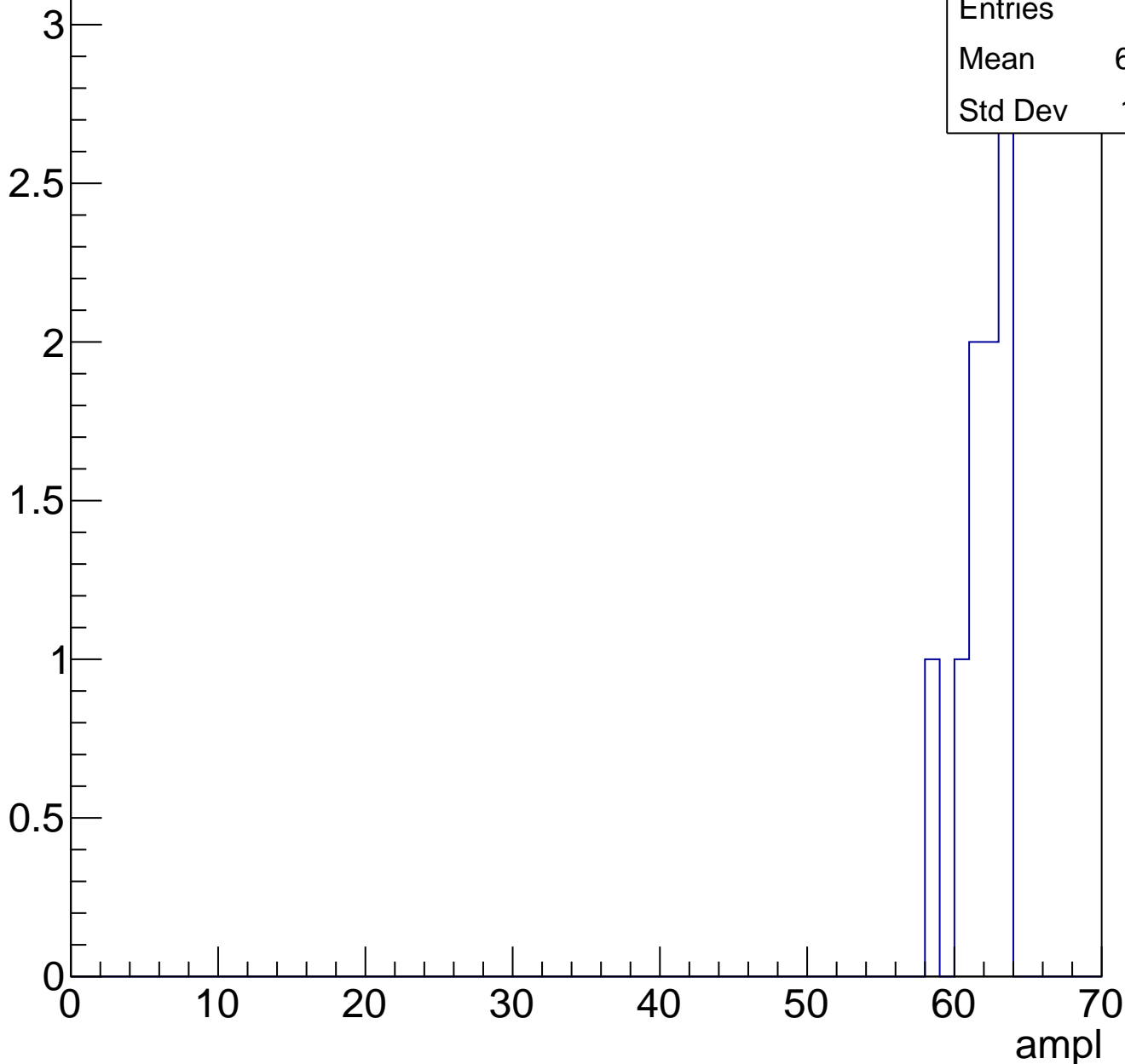
|         |       |
|---------|-------|
| Entries | 38    |
| Mean    | 58.82 |
| Std Dev | 9.894 |



# B0L001S, U2-ch92, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch92, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 2 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch93, adc0

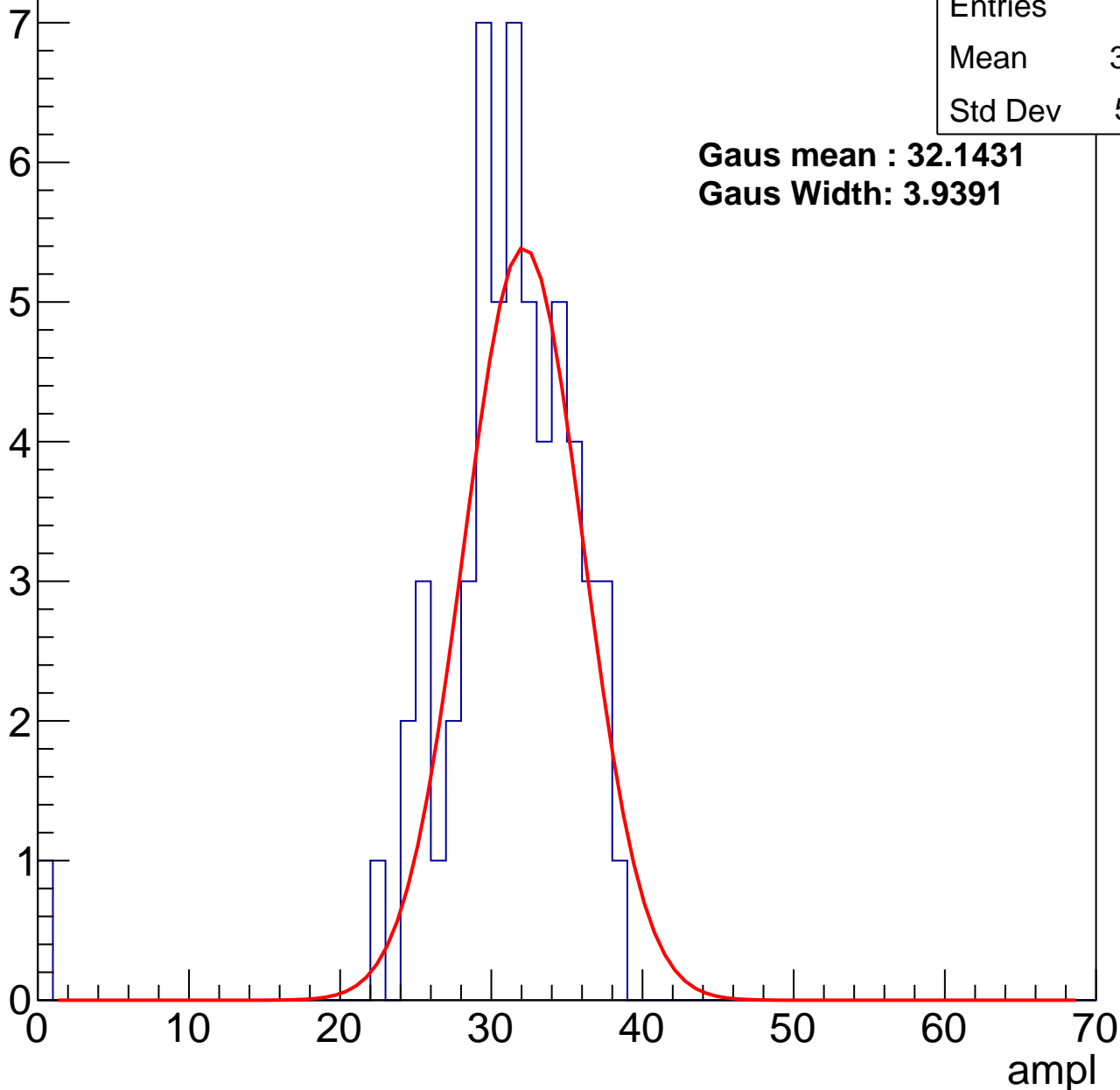
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 57    |
| Mean    | 30.49 |
| Std Dev | 5.481 |

**Gaus mean : 32.1431**

**Gaus Width: 3.9391**



# B0L001S, U2-ch93, adc1

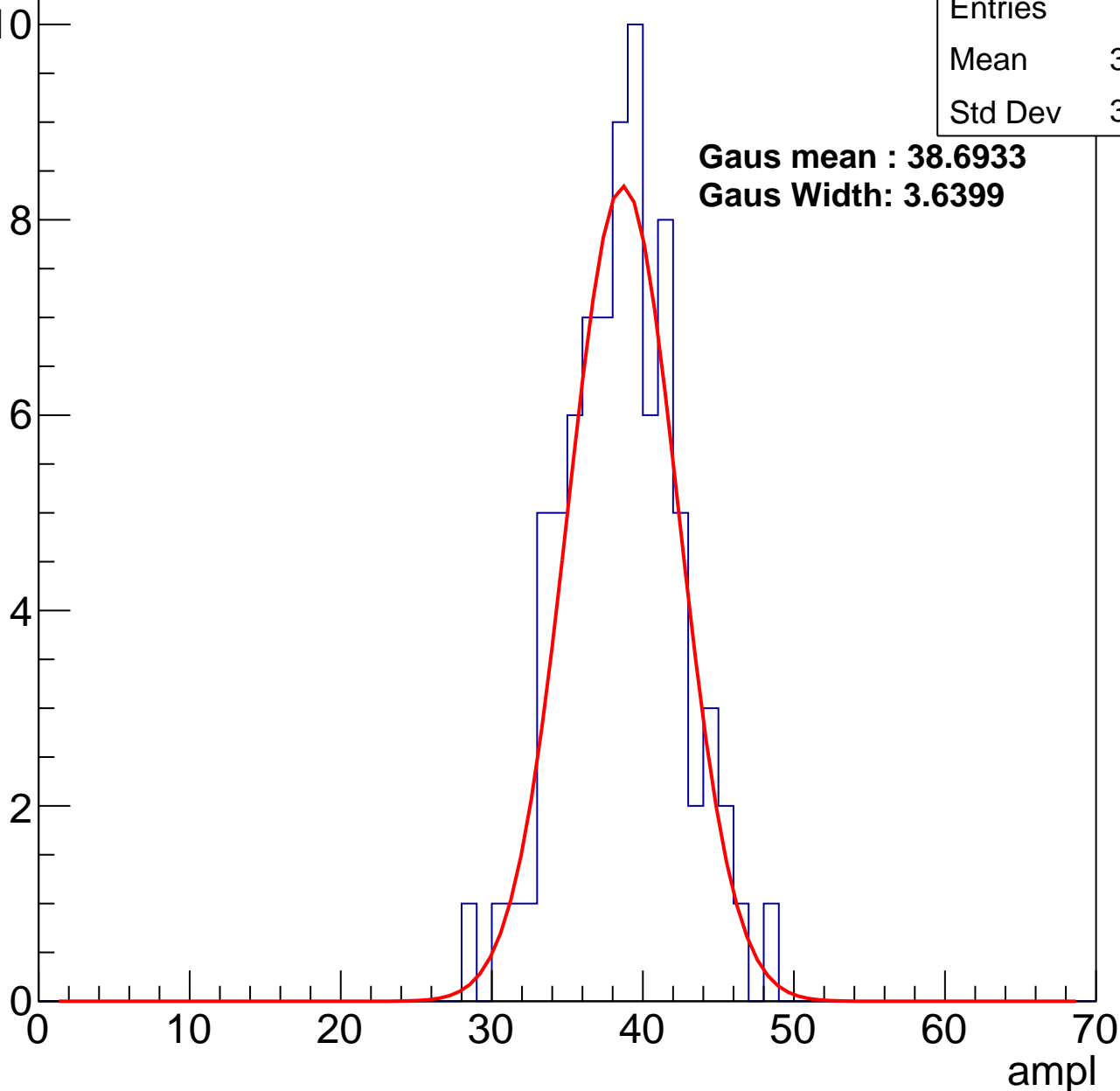
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 81    |
| Mean    | 38.14 |
| Std Dev | 3.764 |

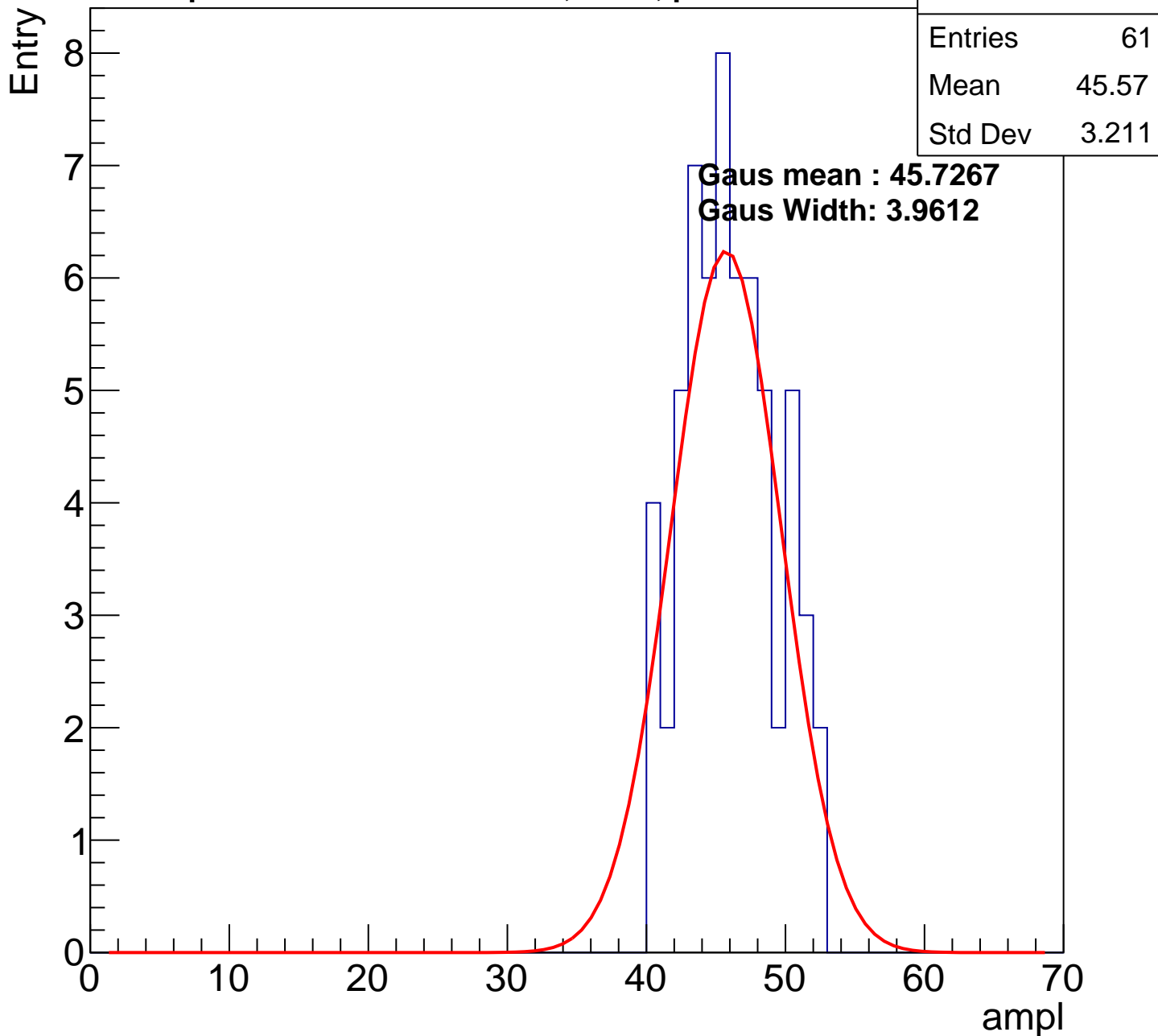
**Gaus mean : 38.6933**

**Gaus Width: 3.6399**



# B0L001S, U2-ch93, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

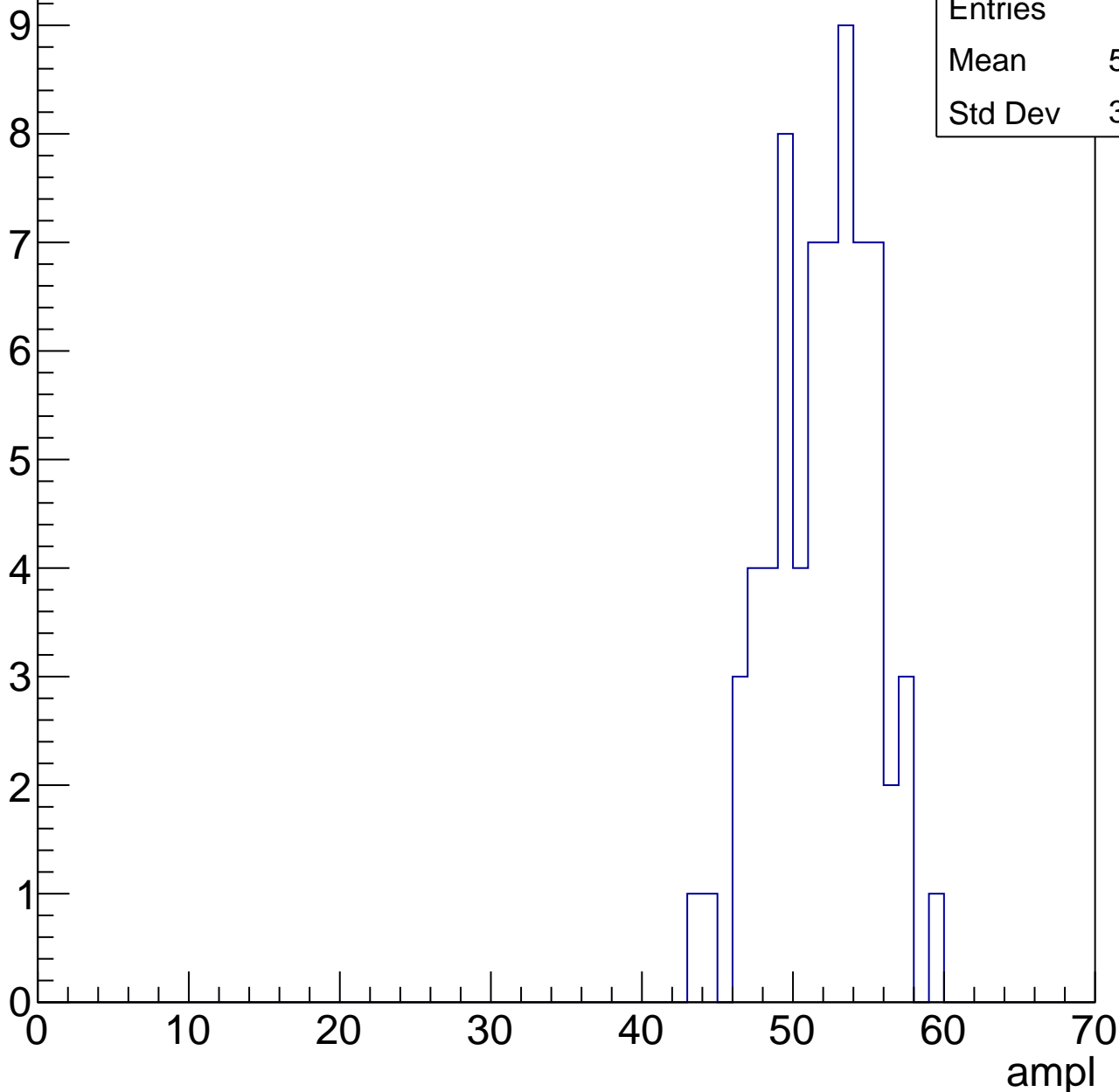


# B0L001S, U2-ch93, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

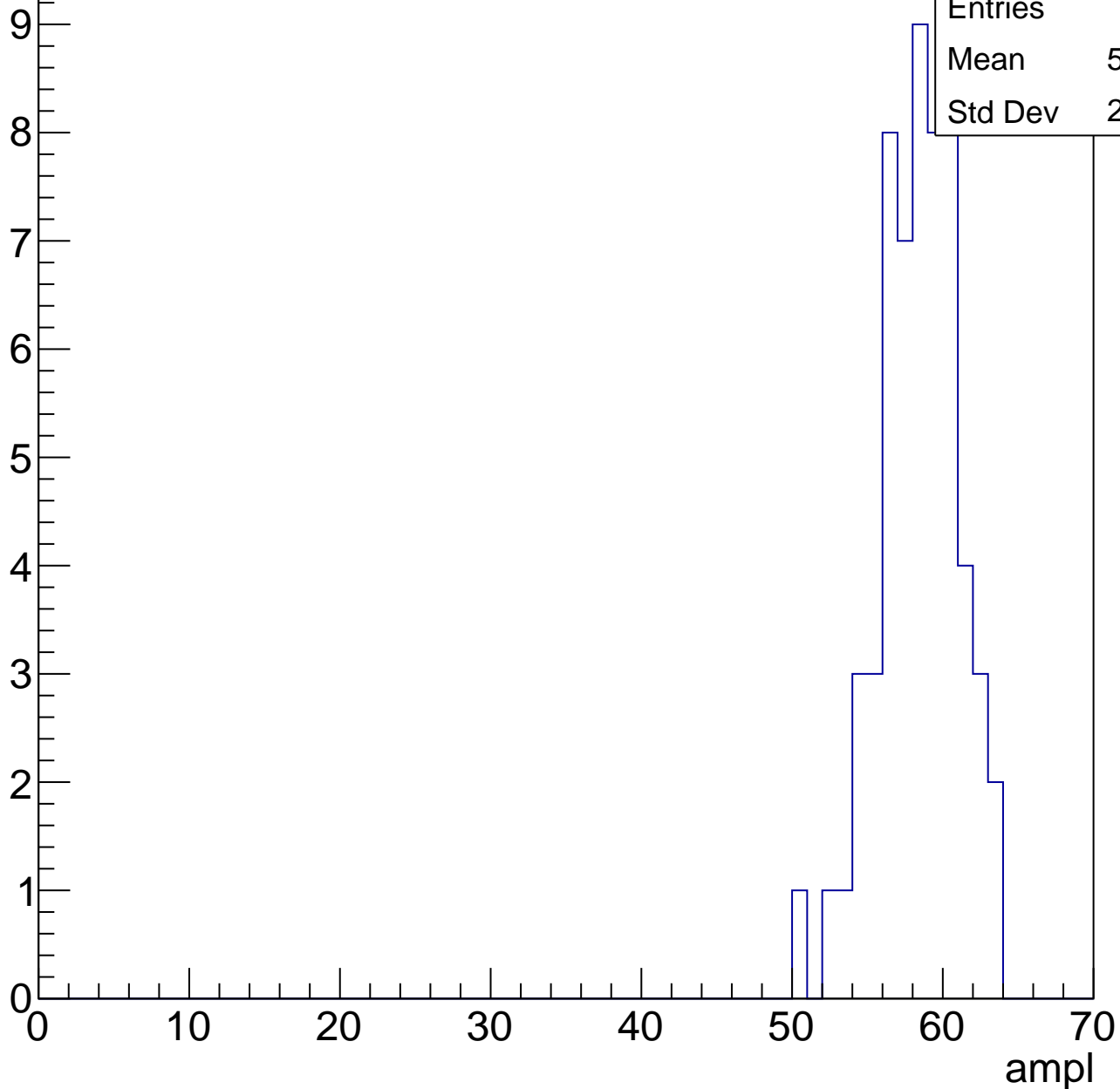
|         |       |
|---------|-------|
| Entries | 68    |
| Mean    | 51.47 |
| Std Dev | 3.319 |



# B0L001S, U2-ch93, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

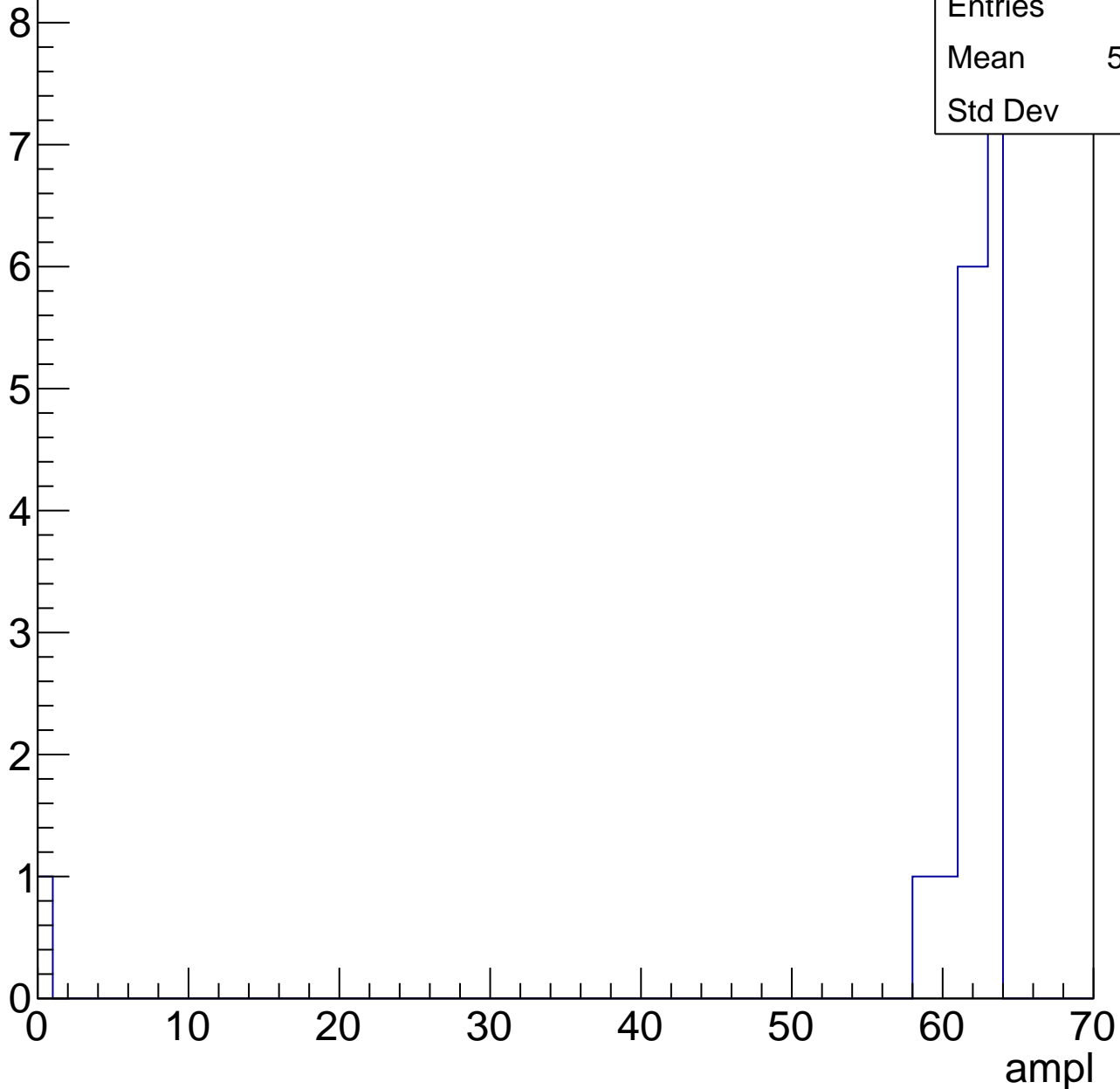


# B0L001S, U2-ch93, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

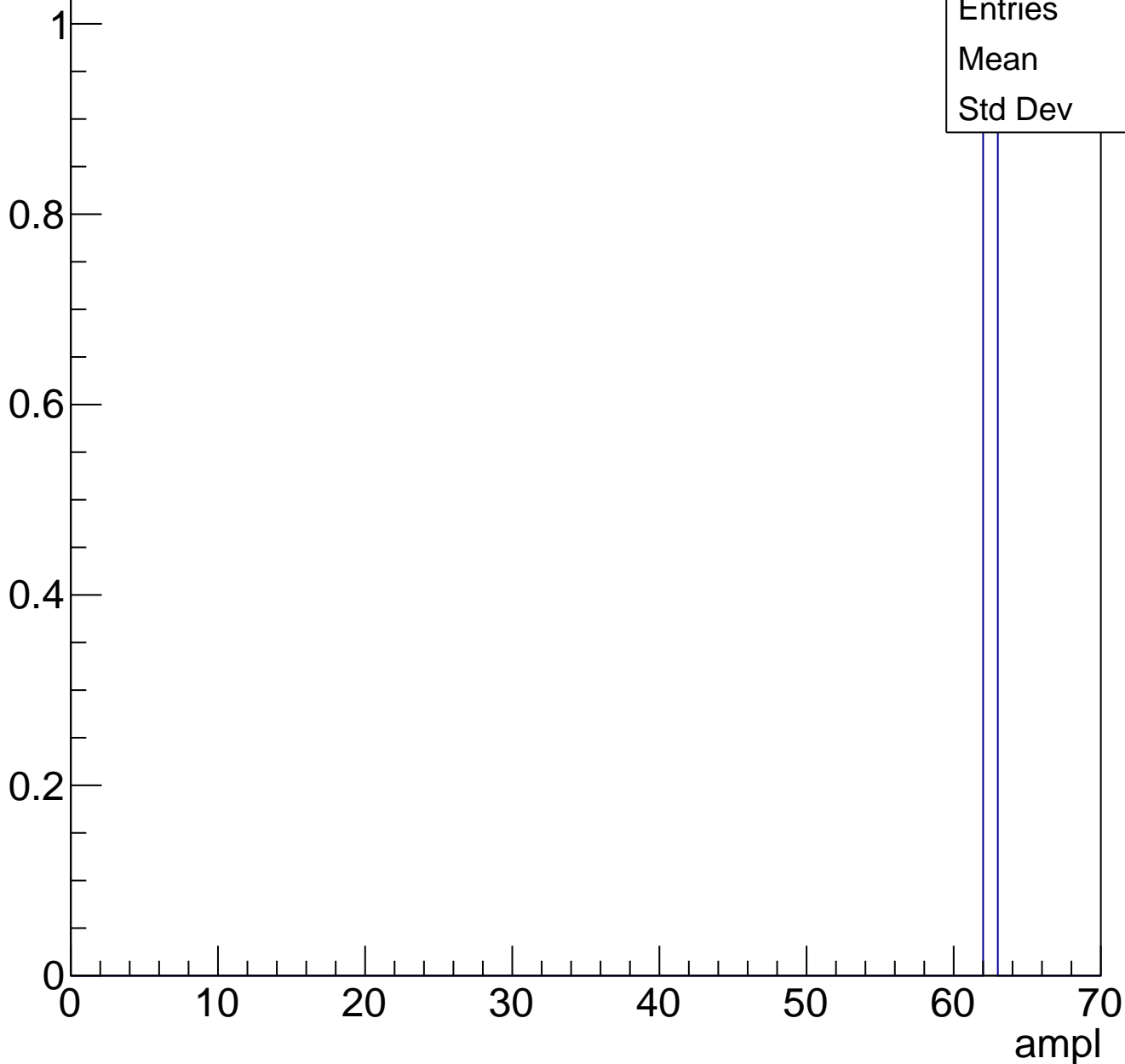
|         |       |
|---------|-------|
| Entries | 24    |
| Mean    | 59.12 |
| Std Dev | 12.4  |



# B0L001S, U2-ch93, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch93, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 1 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch94, adc0

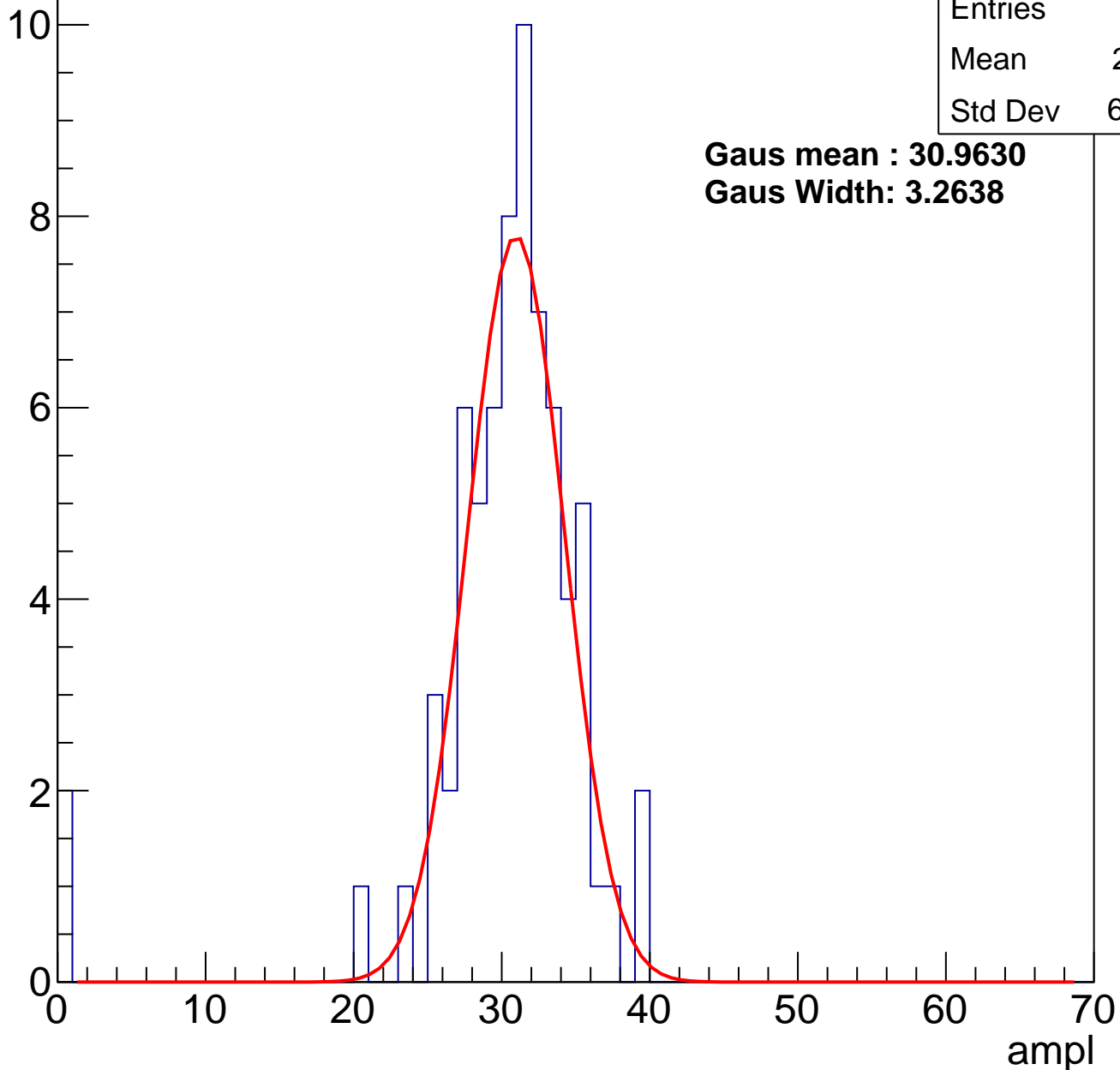
calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 70    |
| Mean    | 29.71 |
| Std Dev | 6.162 |

**Gaus mean : 30.9630**

**Gaus Width: 3.2638**

Entry



# B0L001S, U2-ch94, adc1

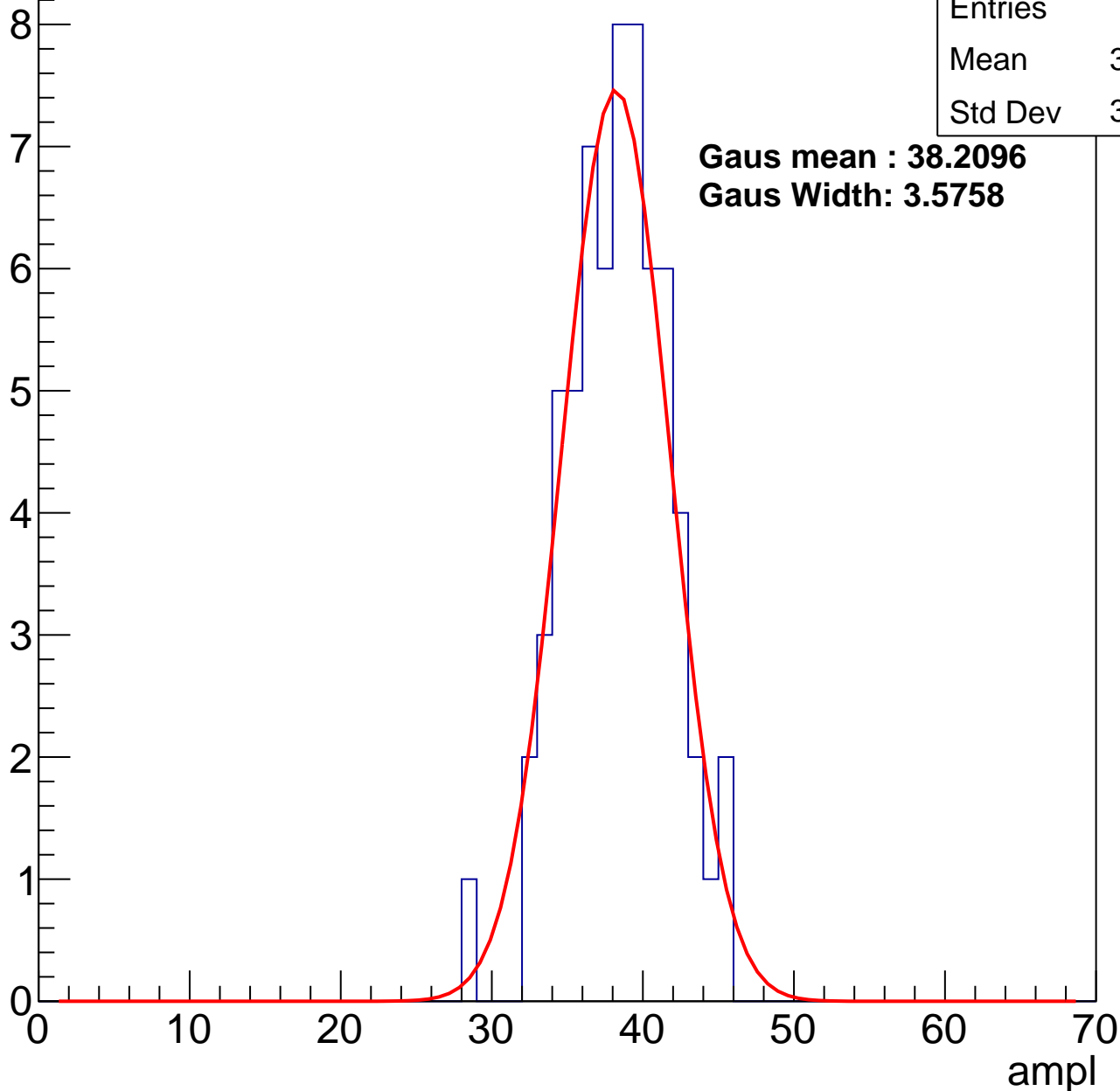
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 66    |
| Mean    | 37.88 |
| Std Dev | 3.346 |

**Gaus mean : 38.2096**

**Gaus Width: 3.5758**



# B0L001S, U2-ch94, adc2

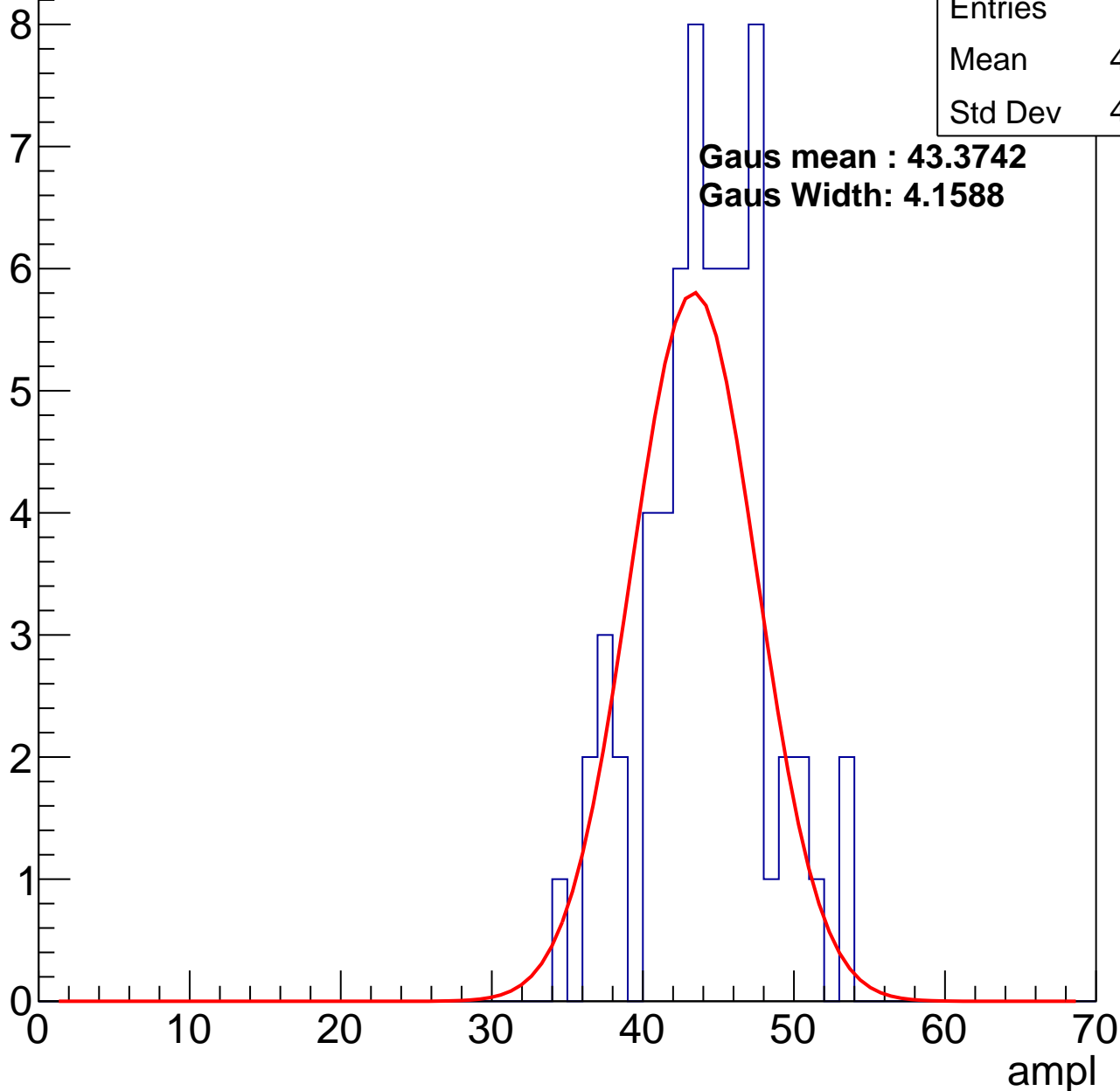
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 64    |
| Mean    | 43.78 |
| Std Dev | 4.006 |

**Gaus mean : 43.3742**

**Gaus Width: 4.1588**

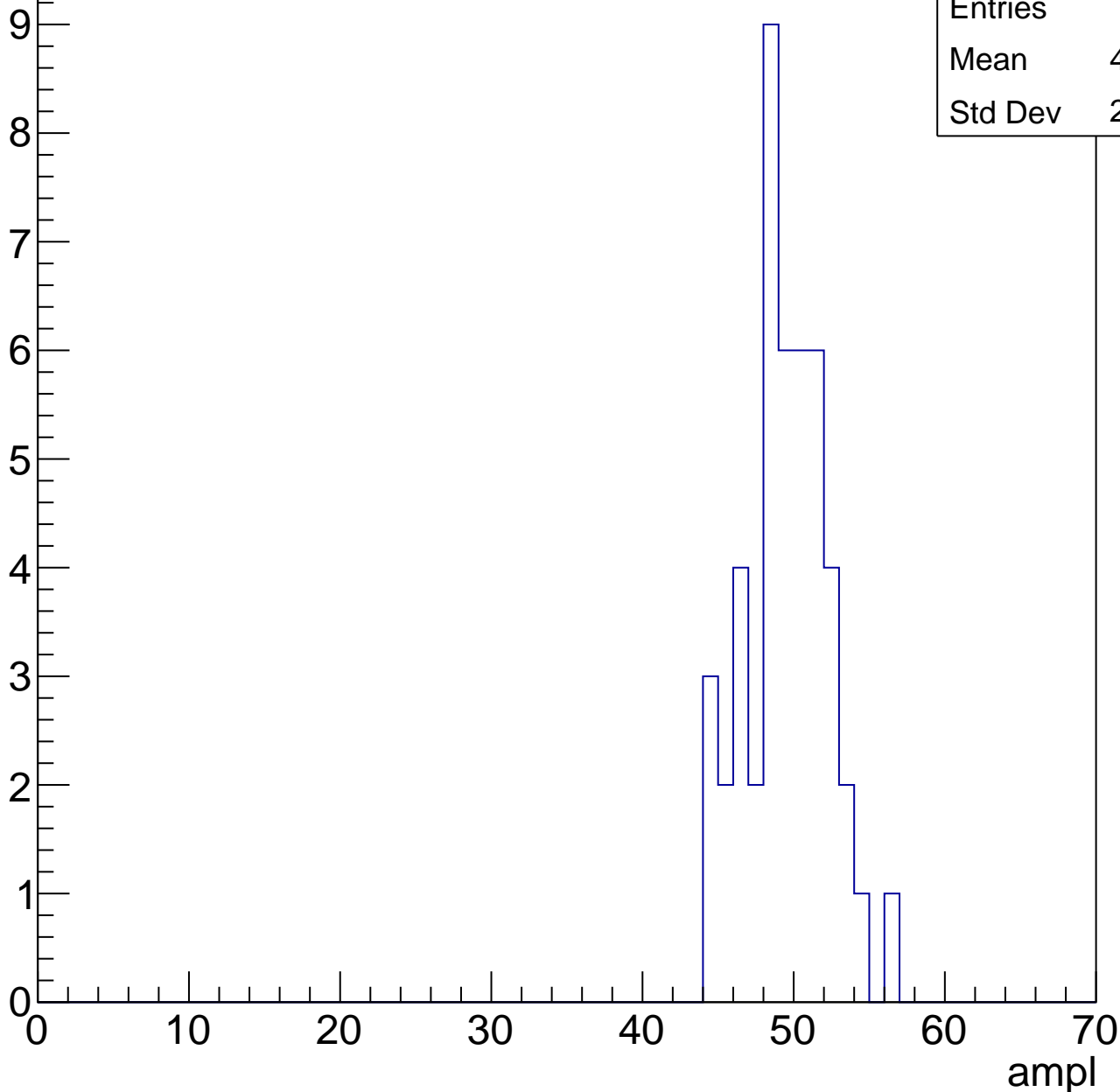


# B0L001S, U2-ch94, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 46    |
| Mean    | 49.04 |
| Std Dev | 2.686 |



# B0L001S, U2-ch94, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

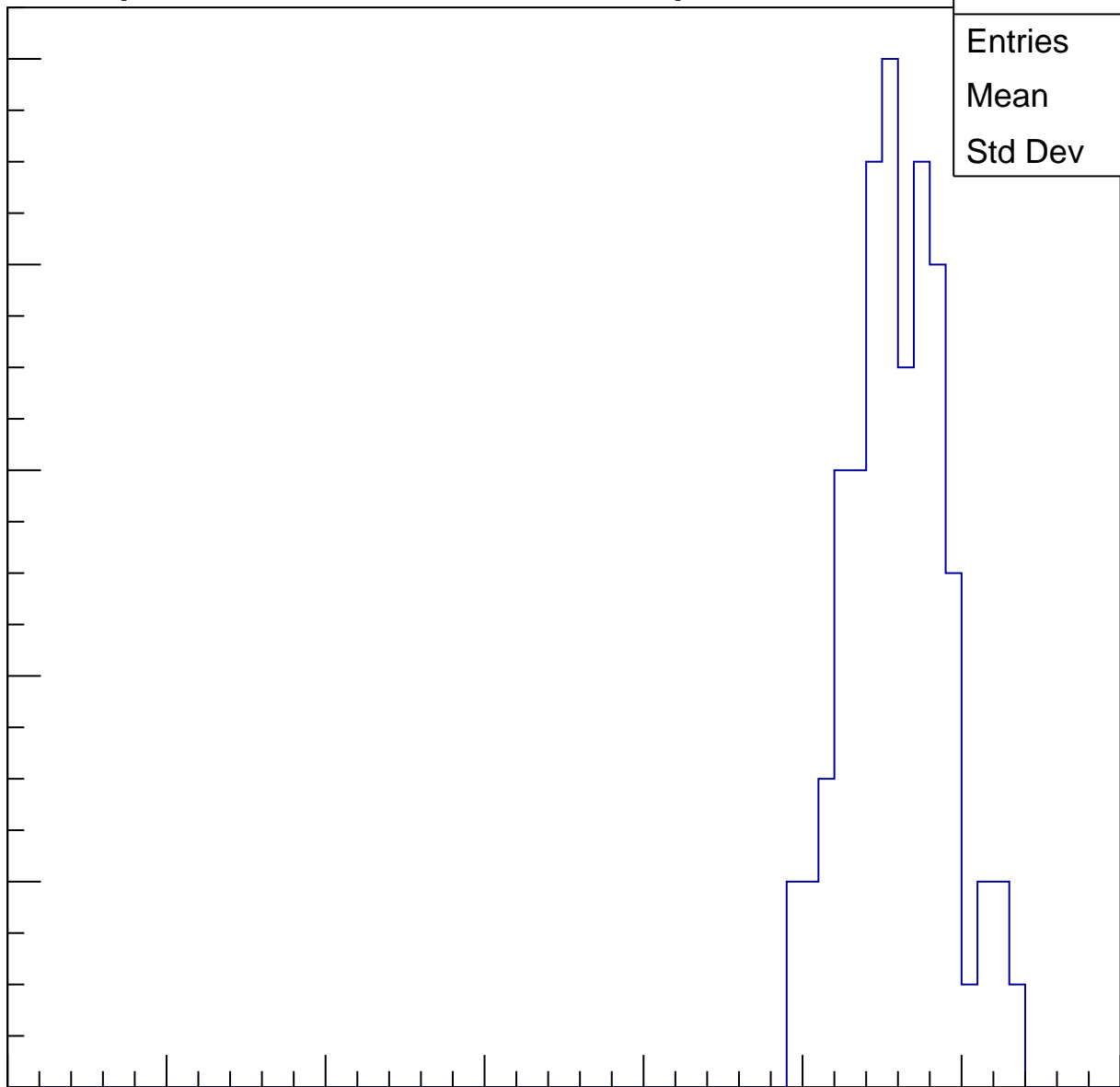
|         |       |
|---------|-------|
| Entries | 73    |
| Mean    | 55.48 |
| Std Dev | 3.084 |

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

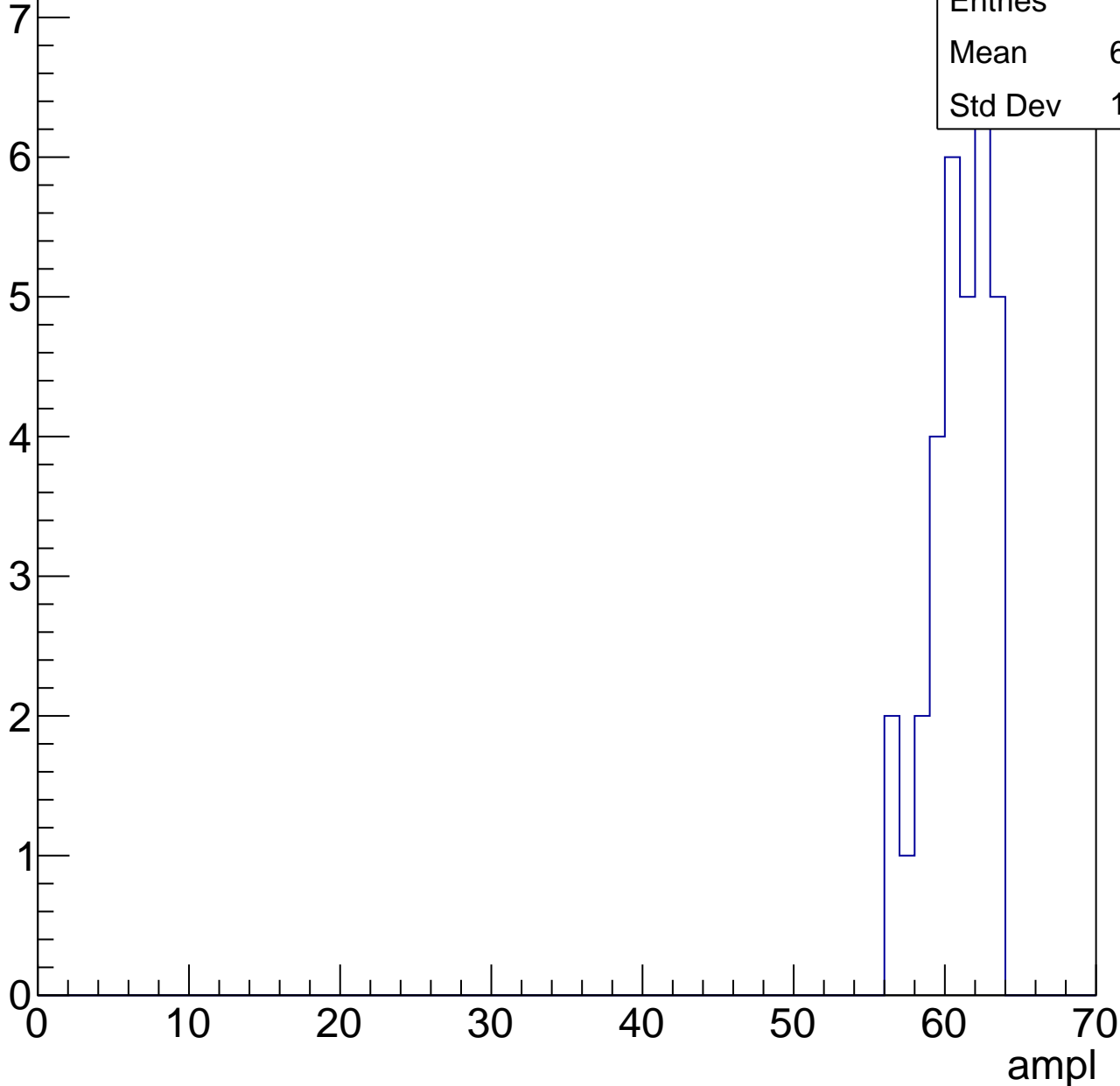


# B0L001S, U2-ch94, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

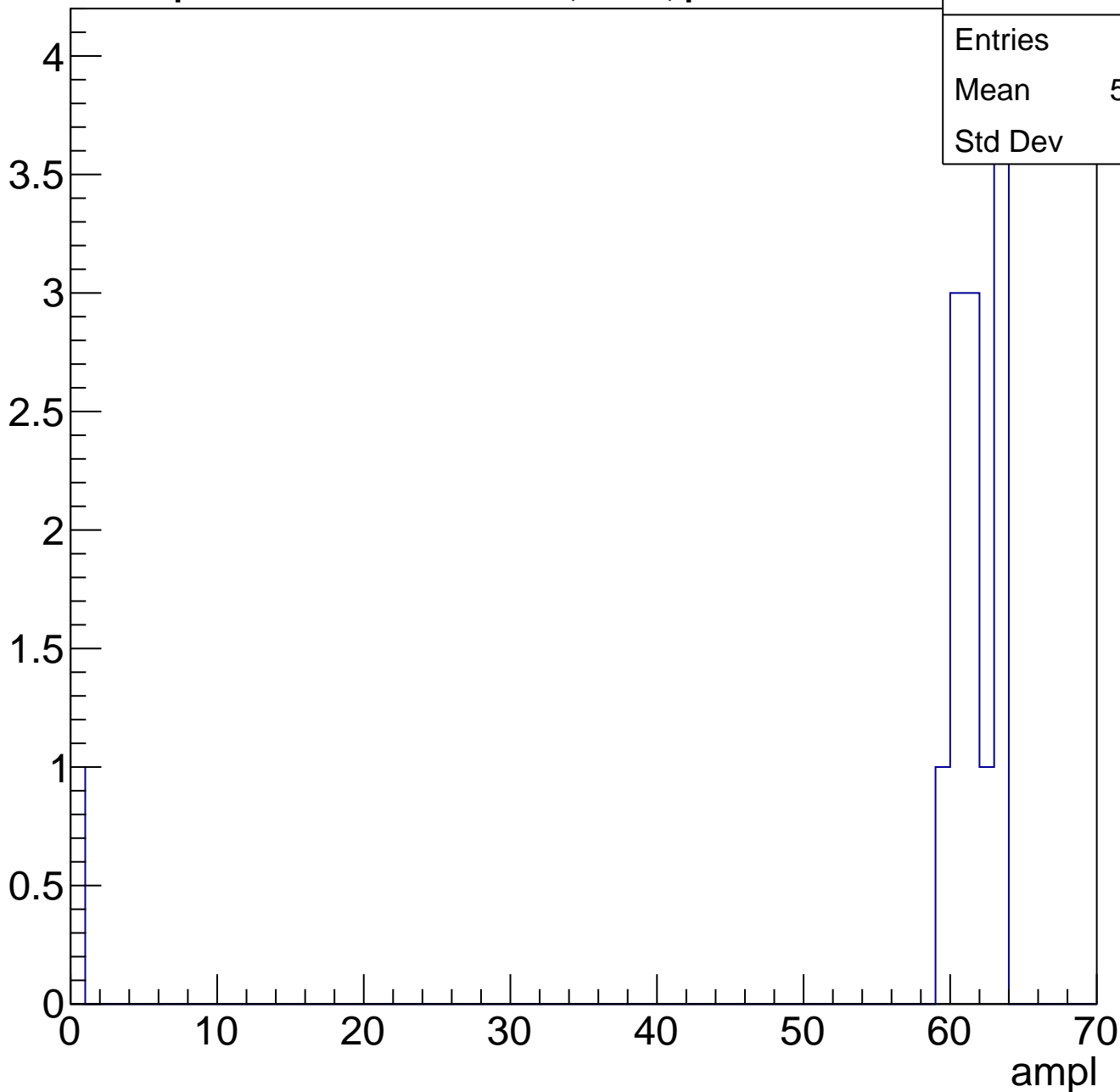
|         |       |
|---------|-------|
| Entries | 32    |
| Mean    | 60.47 |
| Std Dev | 1.968 |



# B0L001S, U2-ch94, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch94, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 0 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch95, adc0

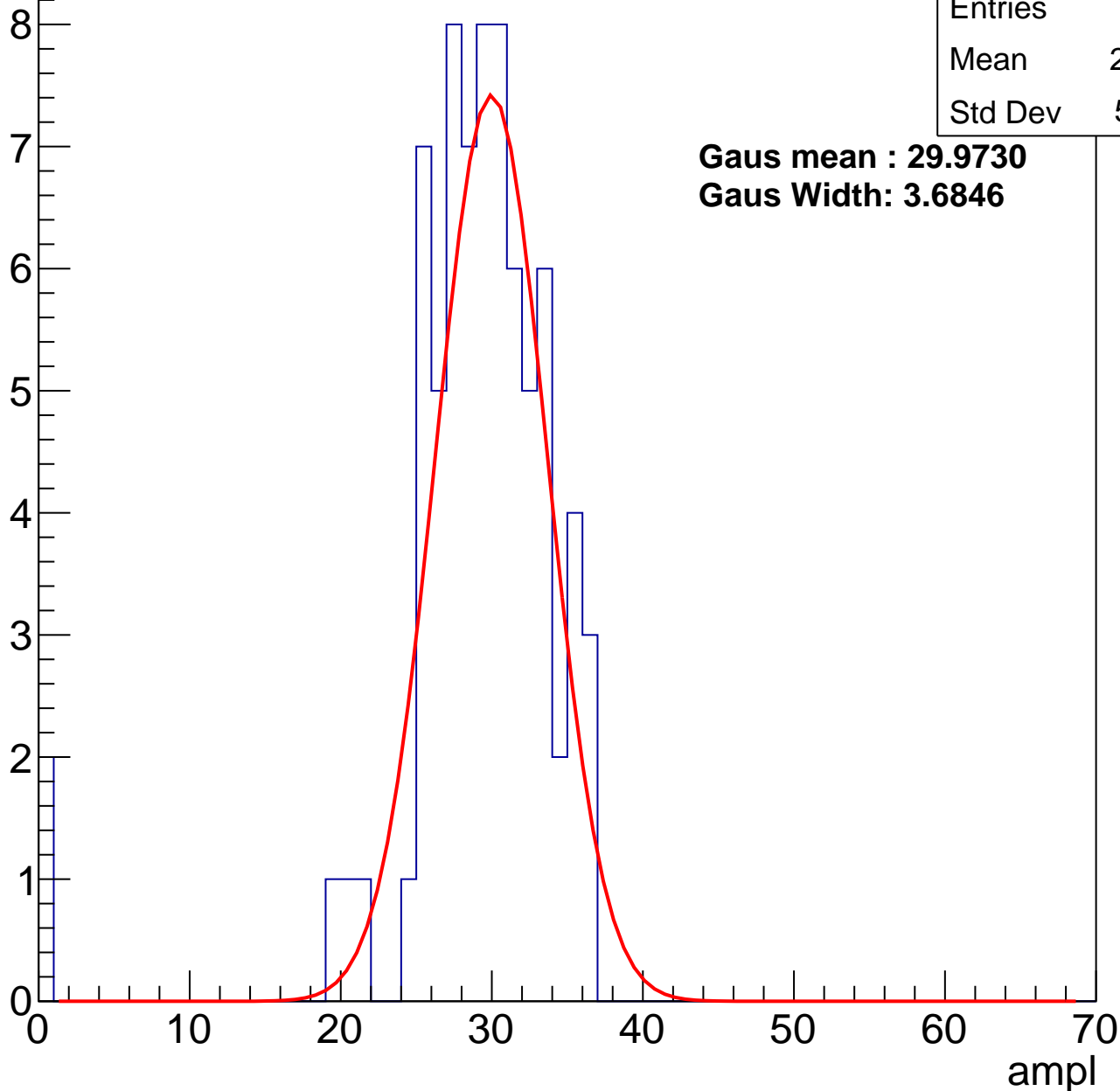
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 75    |
| Mean    | 28.44 |
| Std Dev | 5.931 |

**Gaus mean : 29.9730**

**Gaus Width: 3.6846**



# B0L001S, U2-ch95, adc1

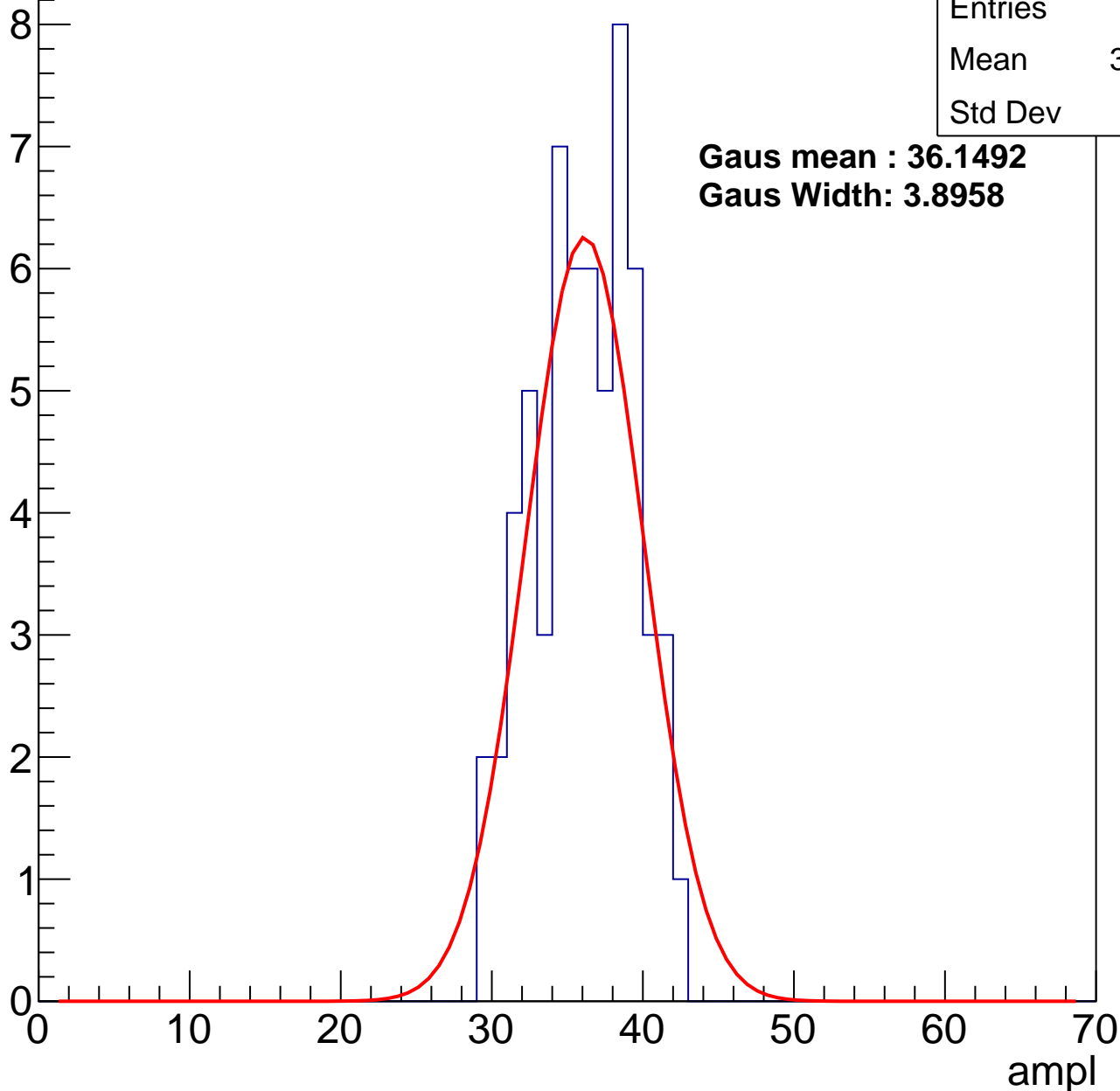
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 61    |
| Mean    | 35.62 |
| Std Dev | 3.27  |

**Gaus mean : 36.1492**

**Gaus Width: 3.8958**



# B0L001S, U2-ch95, adc2

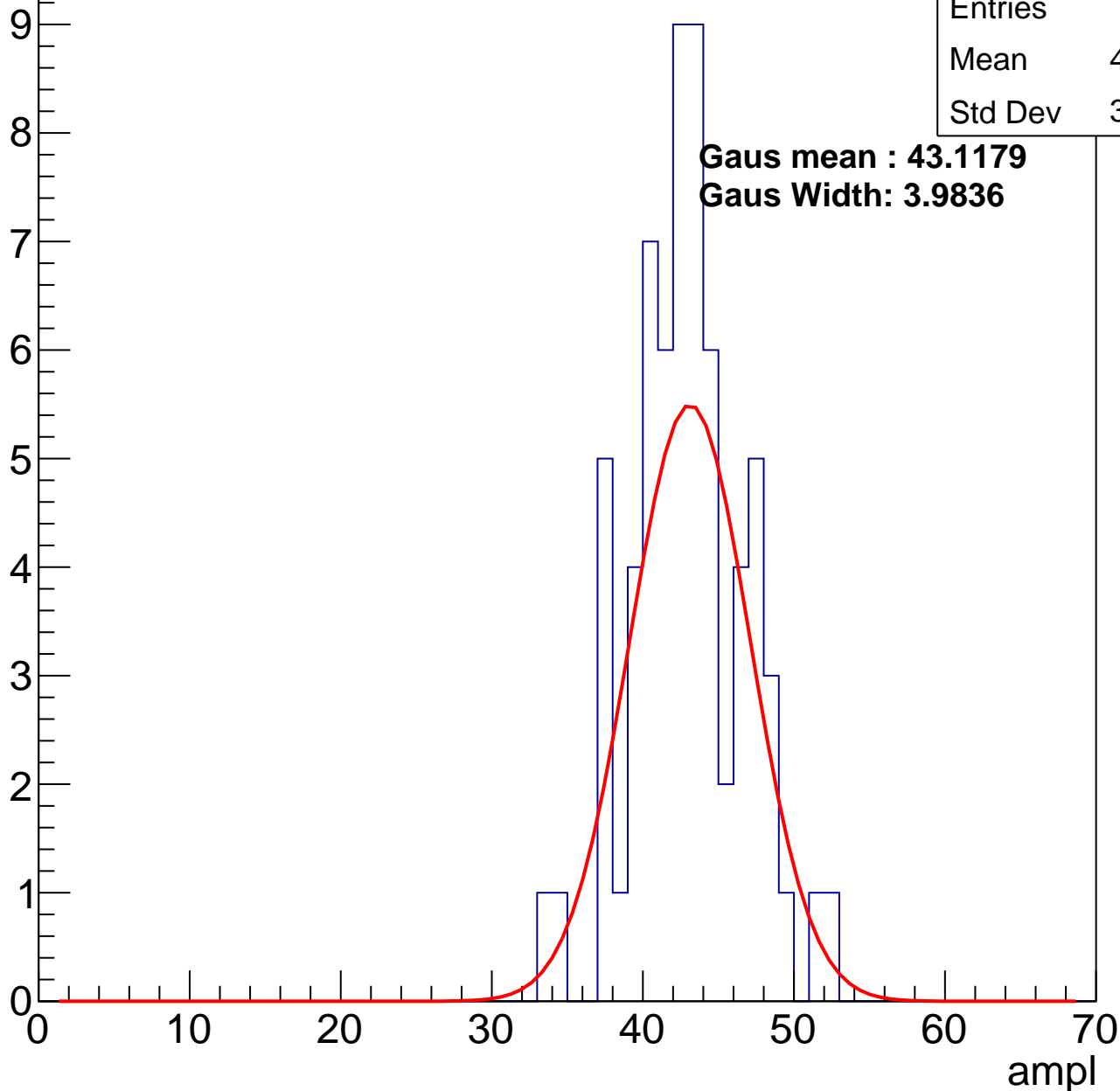
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 66    |
| Mean    | 42.52 |
| Std Dev | 3.726 |

**Gaus mean : 43.1179**

**Gaus Width: 3.9836**

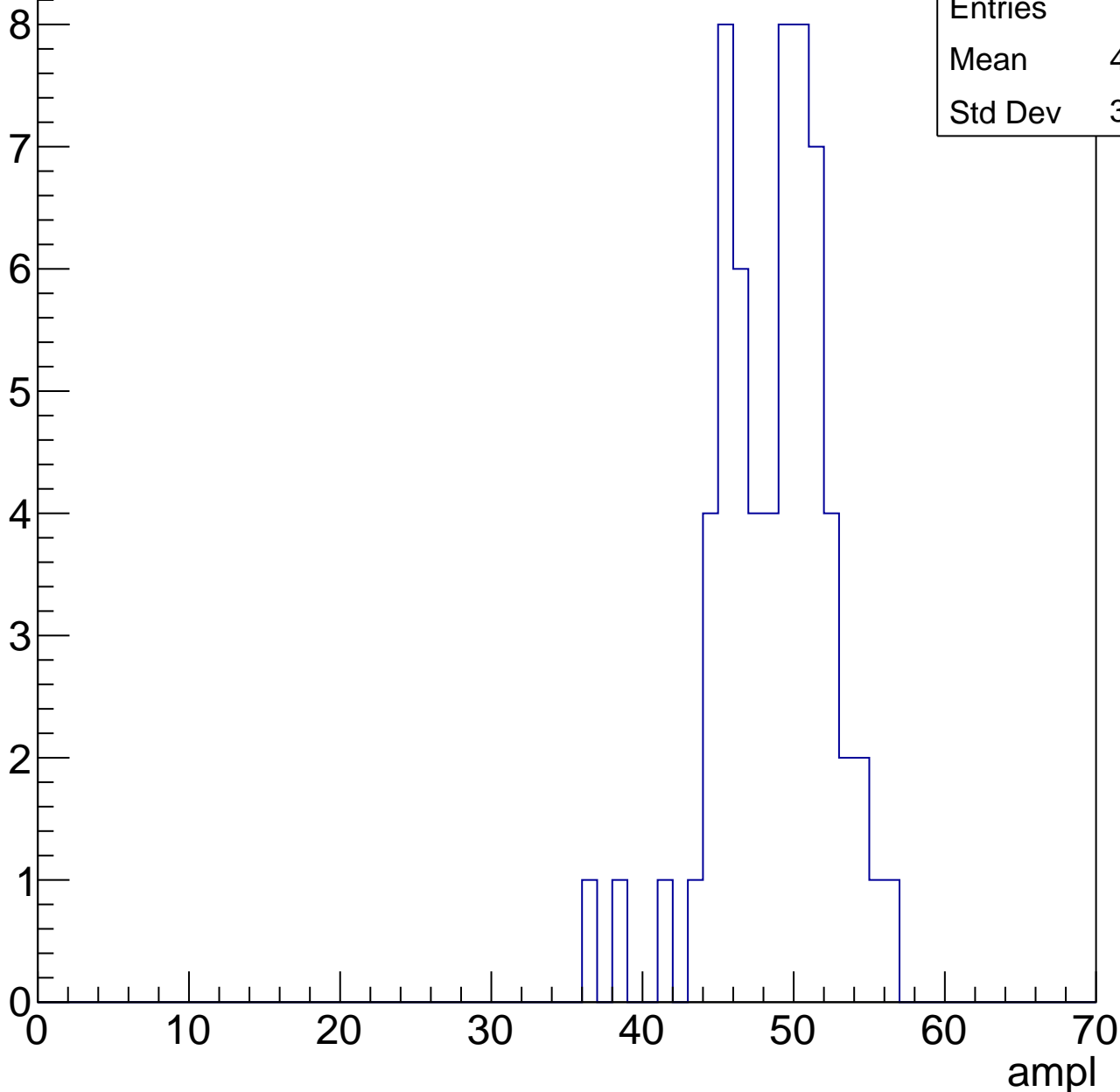


# B0L001S, U2-ch95, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

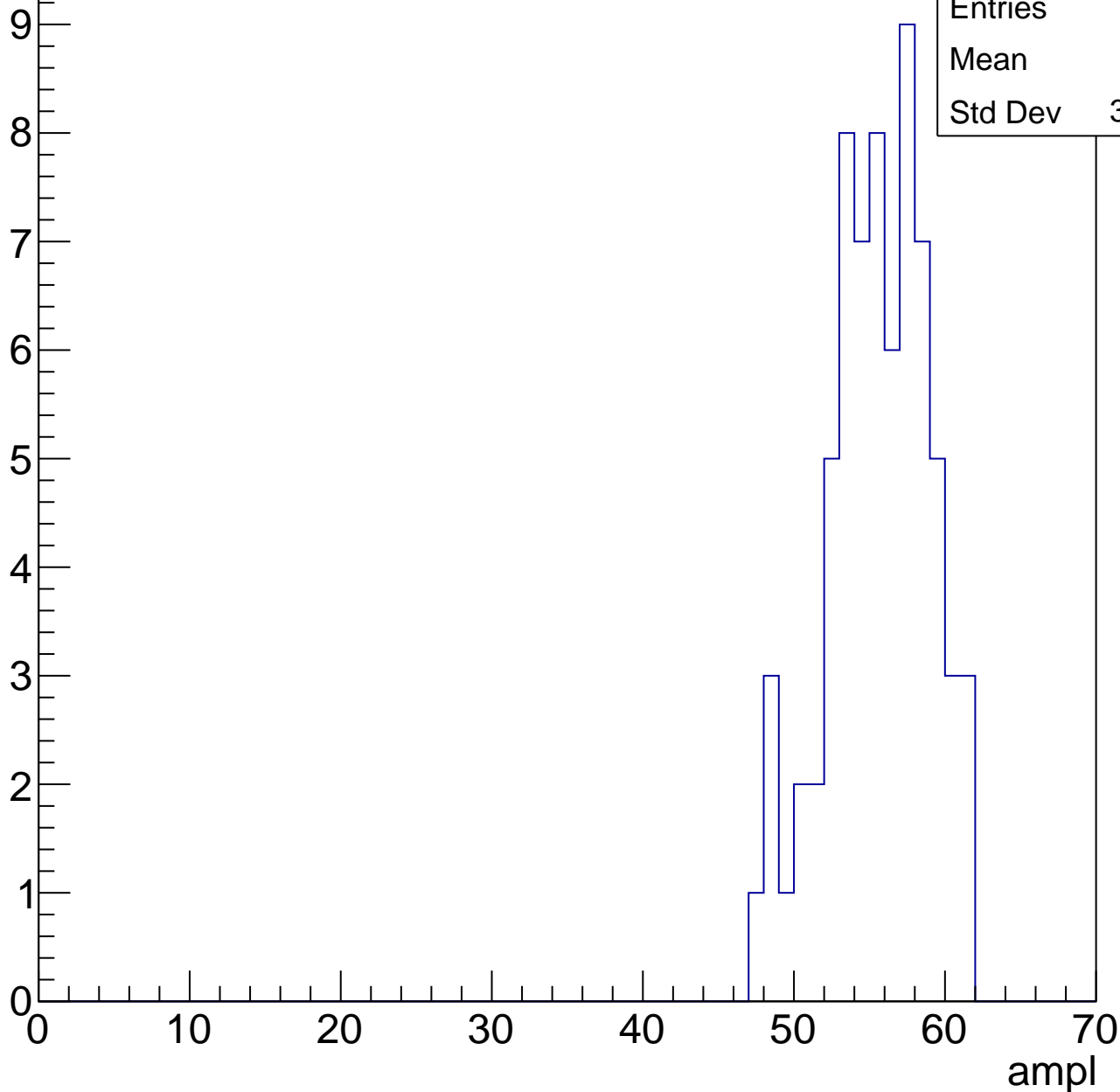
|         |       |
|---------|-------|
| Entries | 63    |
| Mean    | 48.13 |
| Std Dev | 3.744 |



# B0L001S, U2-ch95, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

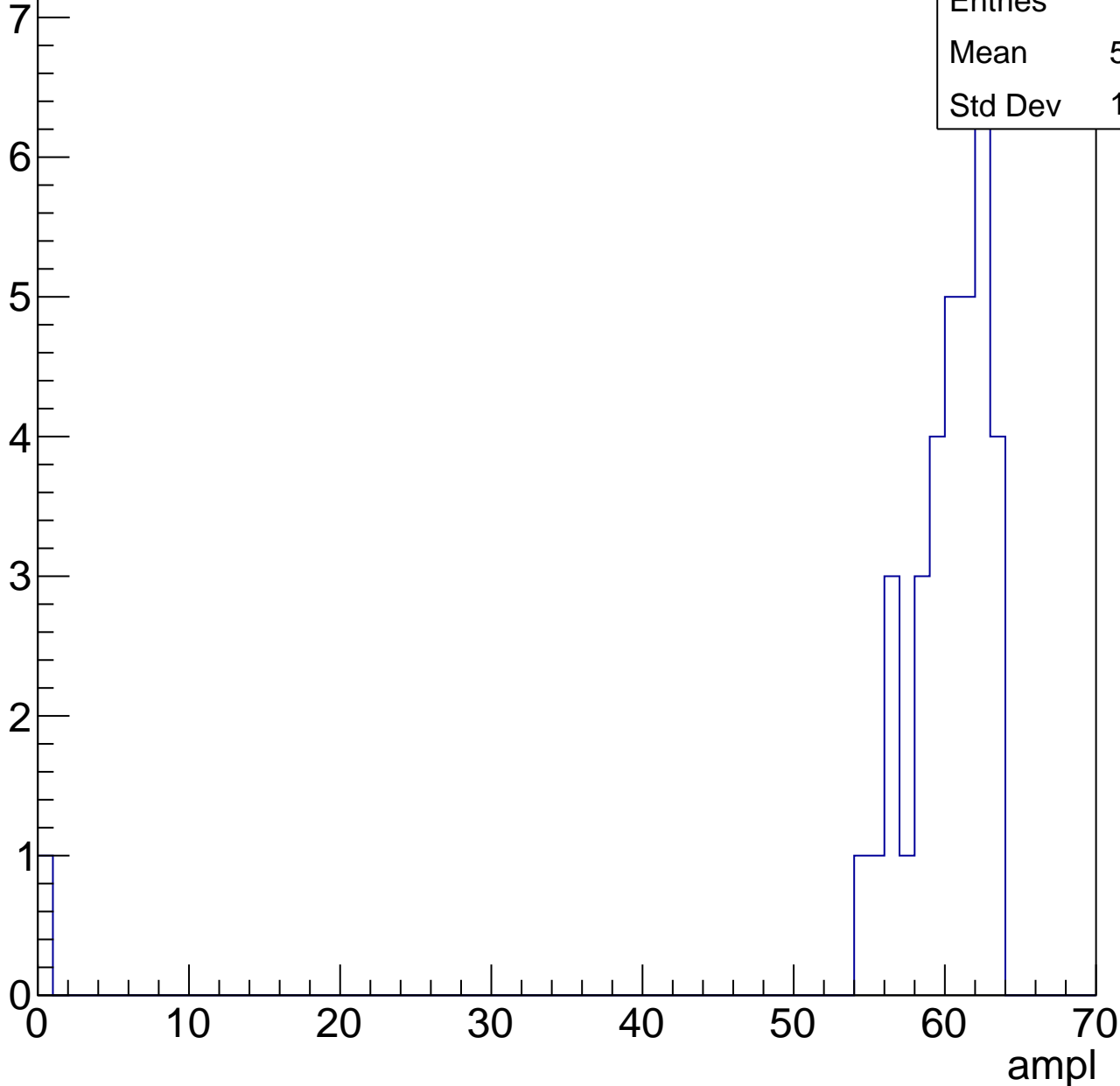


# B0L001S, U2-ch95, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 35    |
| Mean    | 58.14 |
| Std Dev | 10.26 |

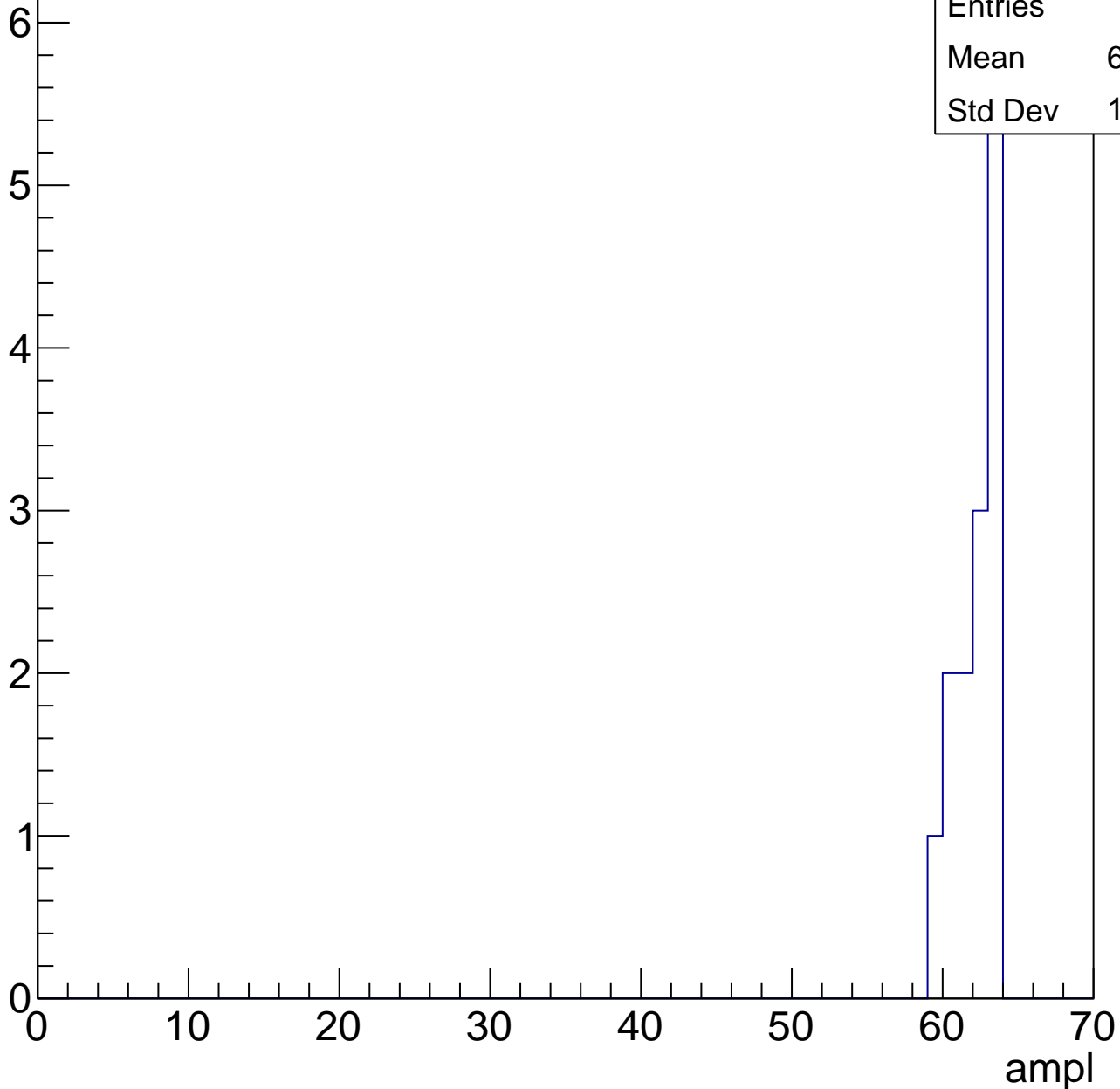


# B0L001S, U2-ch95, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 14    |
| Mean    | 61.79 |
| Std Dev | 1.319 |





# B0L001S, U2-ch95, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U2-ch96, adc0

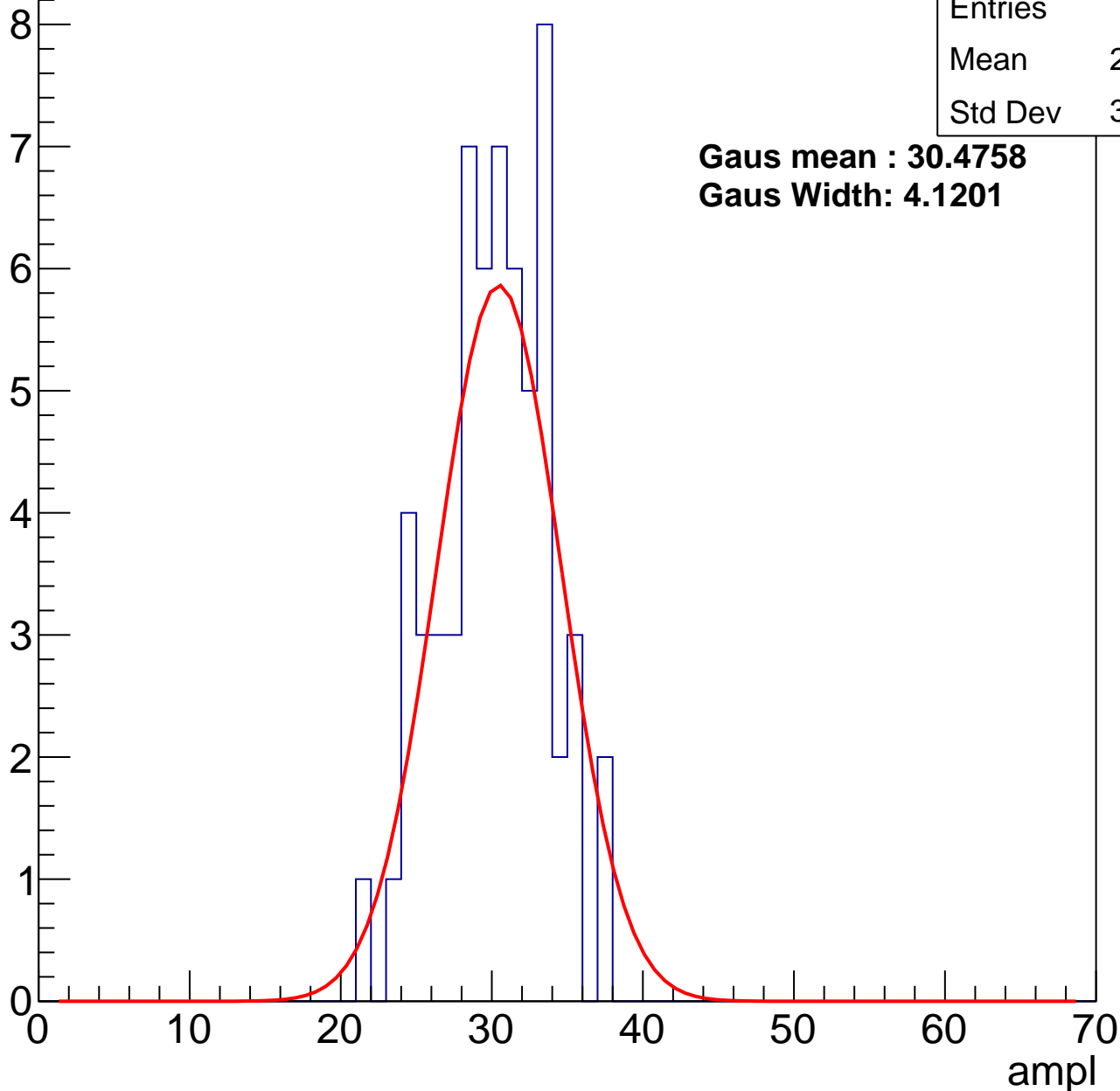
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 61    |
| Mean    | 29.69 |
| Std Dev | 3.518 |

**Gaus mean : 30.4758**

**Gaus Width: 4.1201**



# B0L001S, U2-ch96, adc1

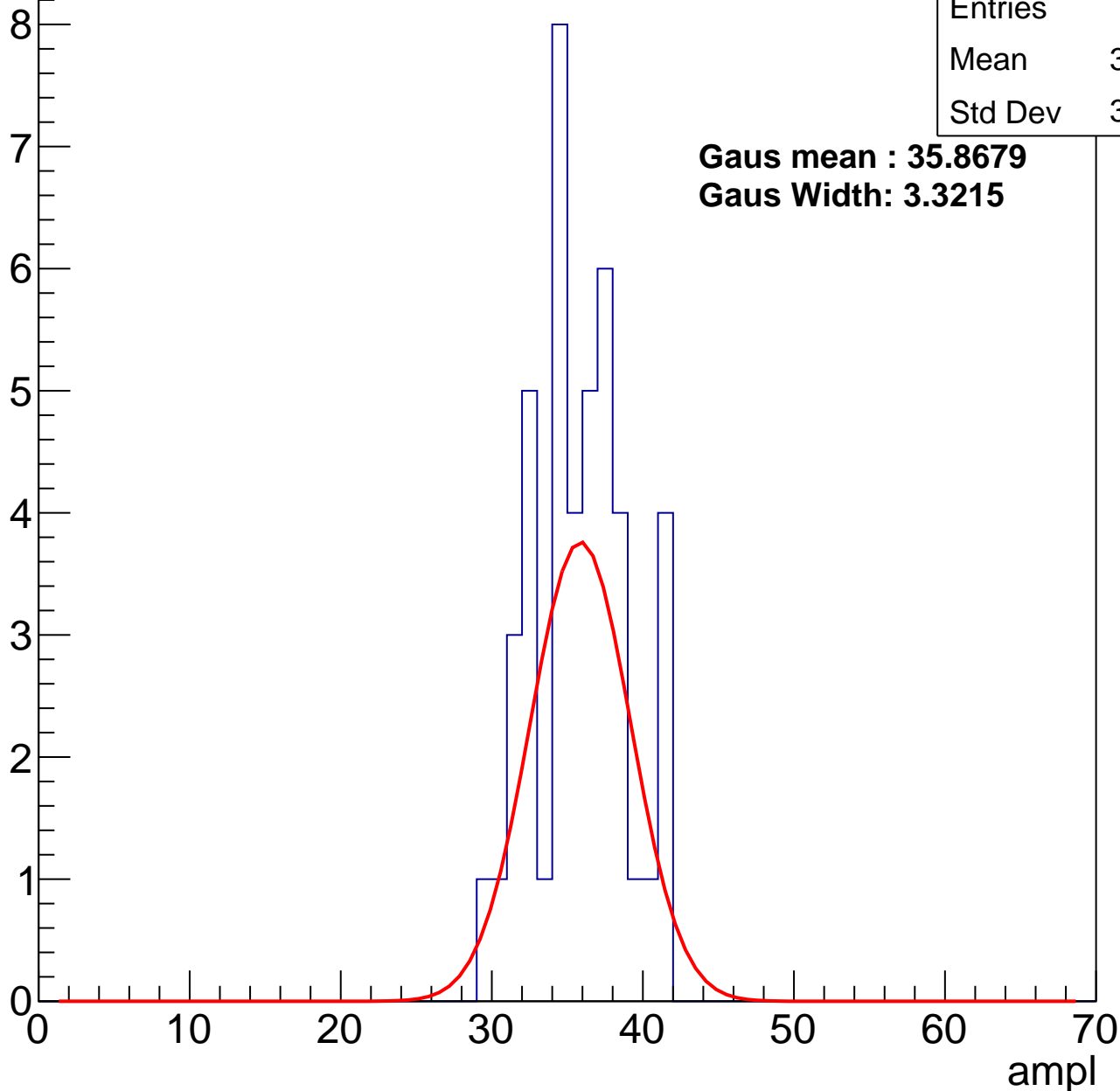
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 44    |
| Mean    | 35.32 |
| Std Dev | 3.058 |

**Gaus mean : 35.8679**

**Gaus Width: 3.3215**



# B0L001S, U2-ch96, adc2

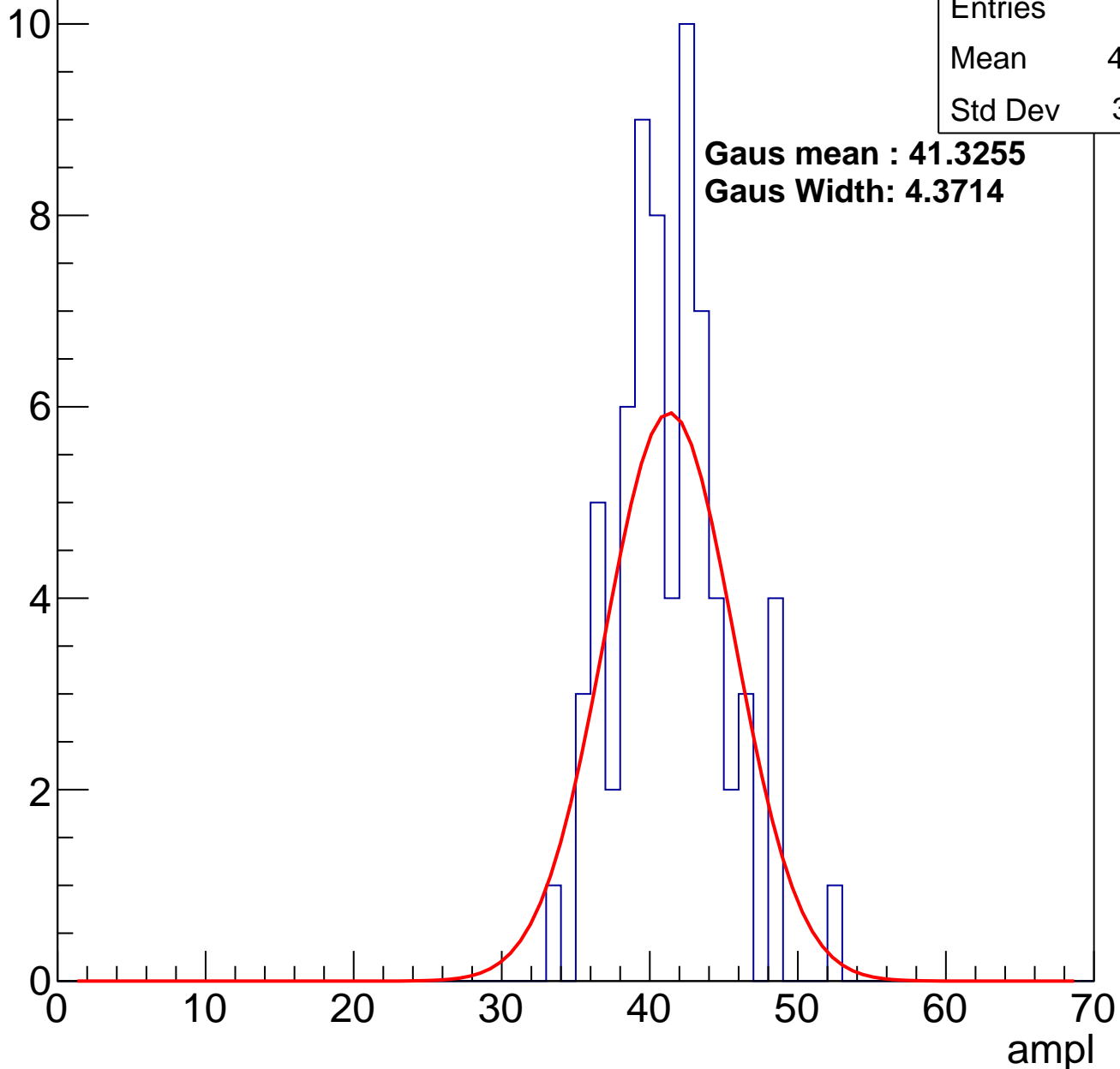
calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 69    |
| Mean    | 40.93 |
| Std Dev | 3.661 |

**Gaus mean : 41.3255**

**Gaus Width: 4.3714**

Entry

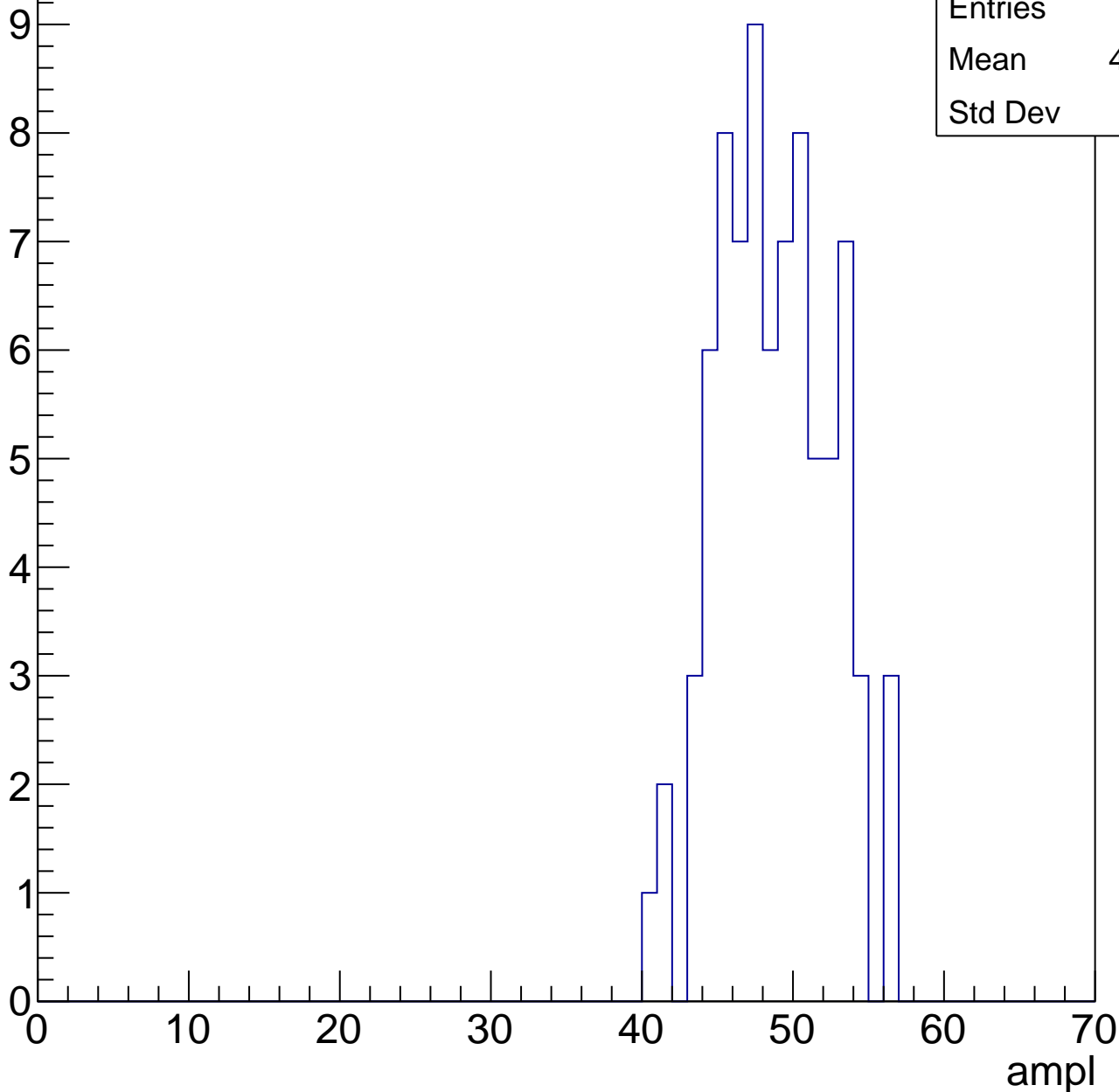


# B0L001S, U2-ch96, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 80    |
| Mean    | 48.34 |
| Std Dev | 3.66  |

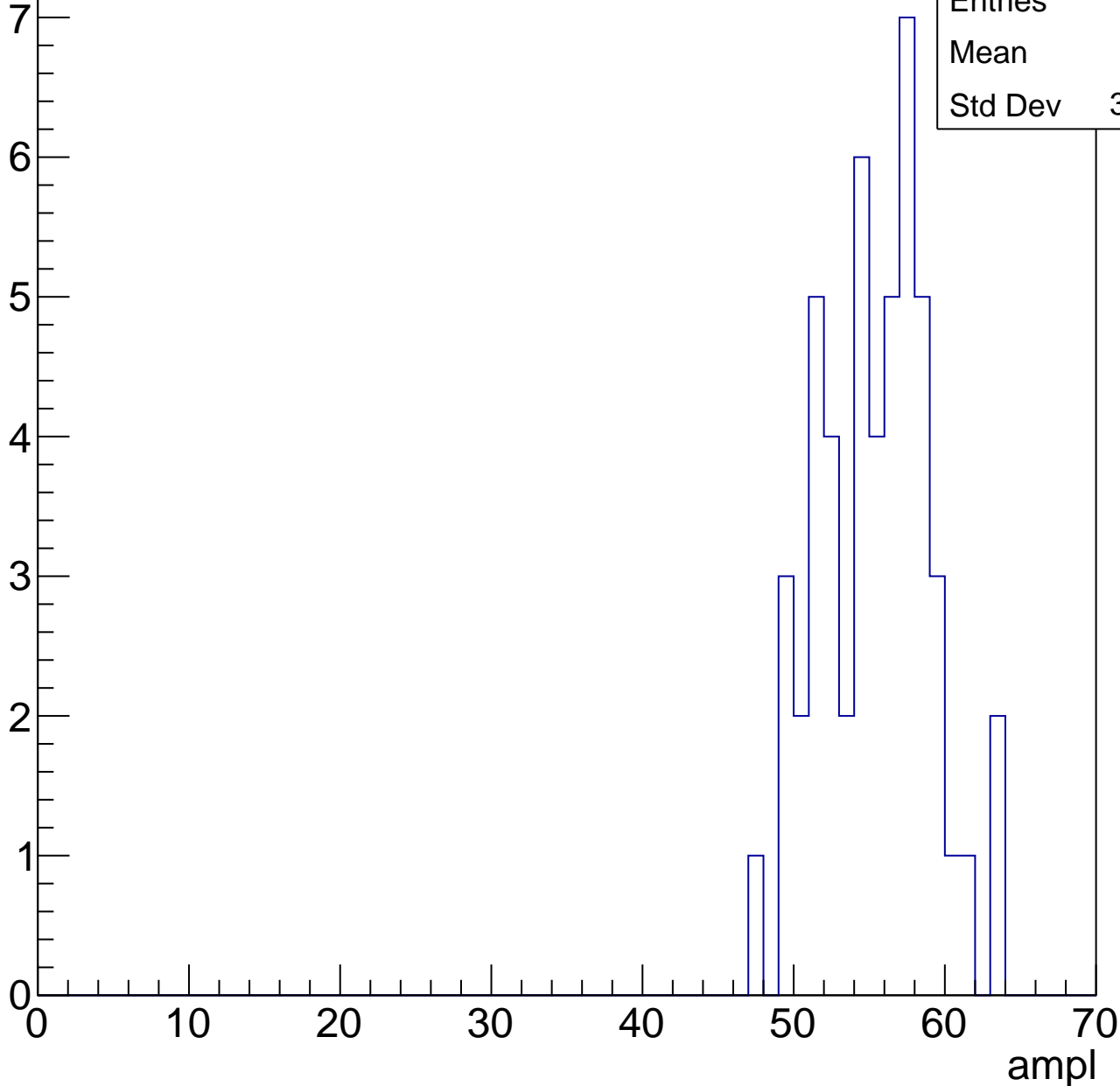


# B0L001S, U2-ch96, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 51    |
| Mean    | 54.9  |
| Std Dev | 3.615 |

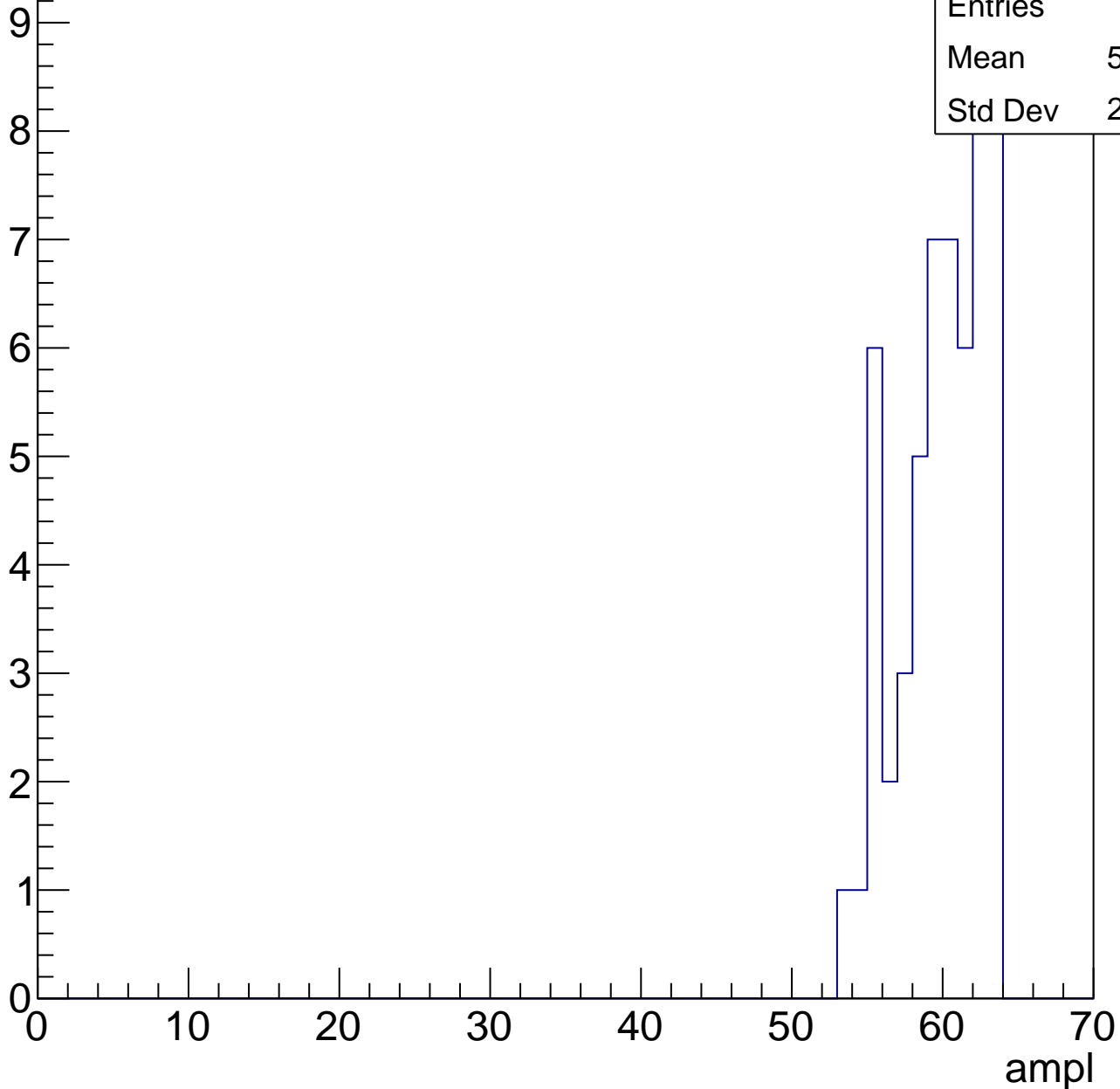


# B0L001S, U2-ch96, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

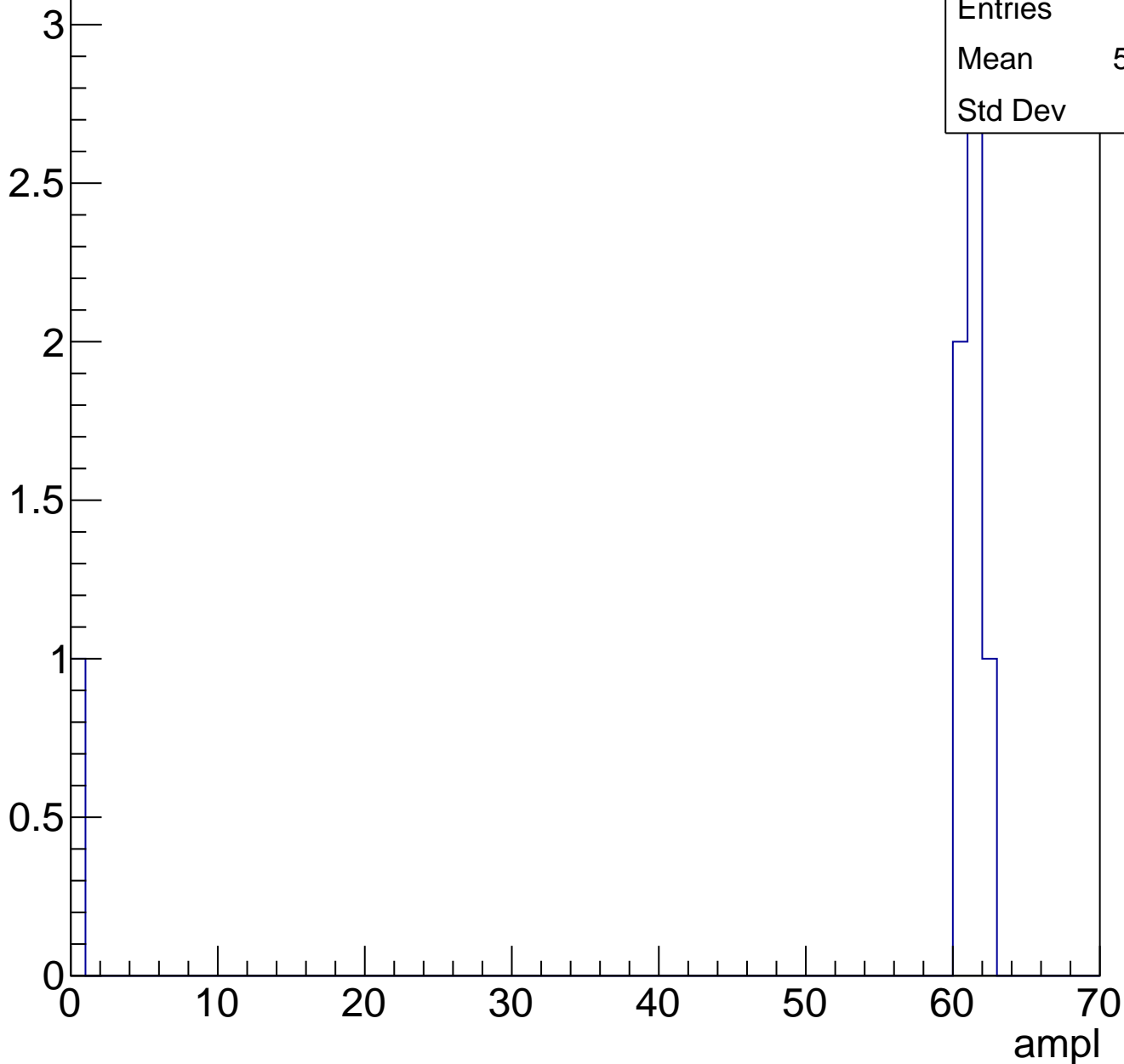
|         |       |
|---------|-------|
| Entries | 55    |
| Mean    | 59.47 |
| Std Dev | 2.762 |



# B0L001S, U2-ch96, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch96, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 0 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch97, adc0

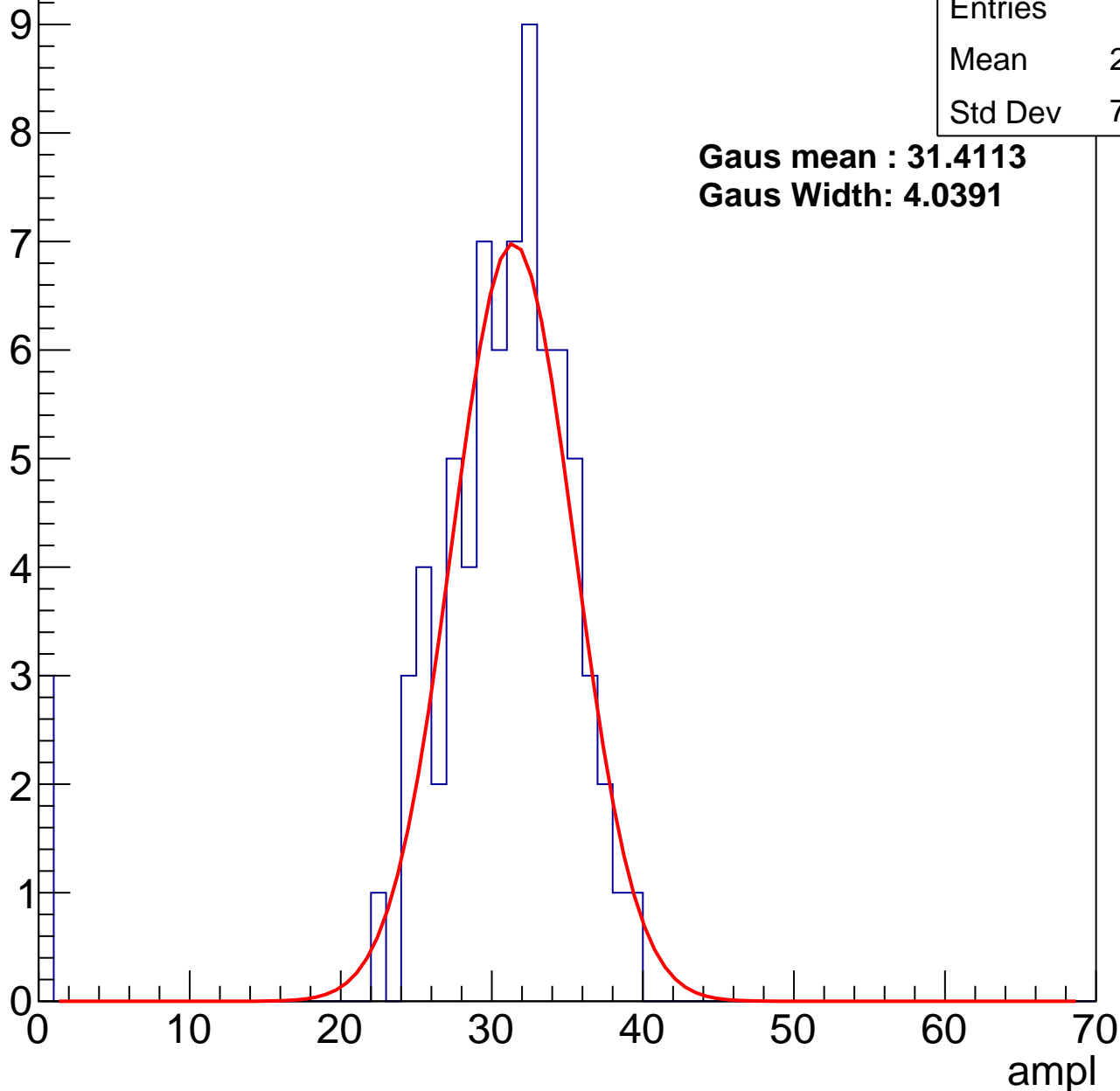
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 75    |
| Mean    | 29.56 |
| Std Dev | 7.049 |

**Gaus mean : 31.4113**

**Gaus Width: 4.0391**



# B0L001S, U2-ch97, adc1

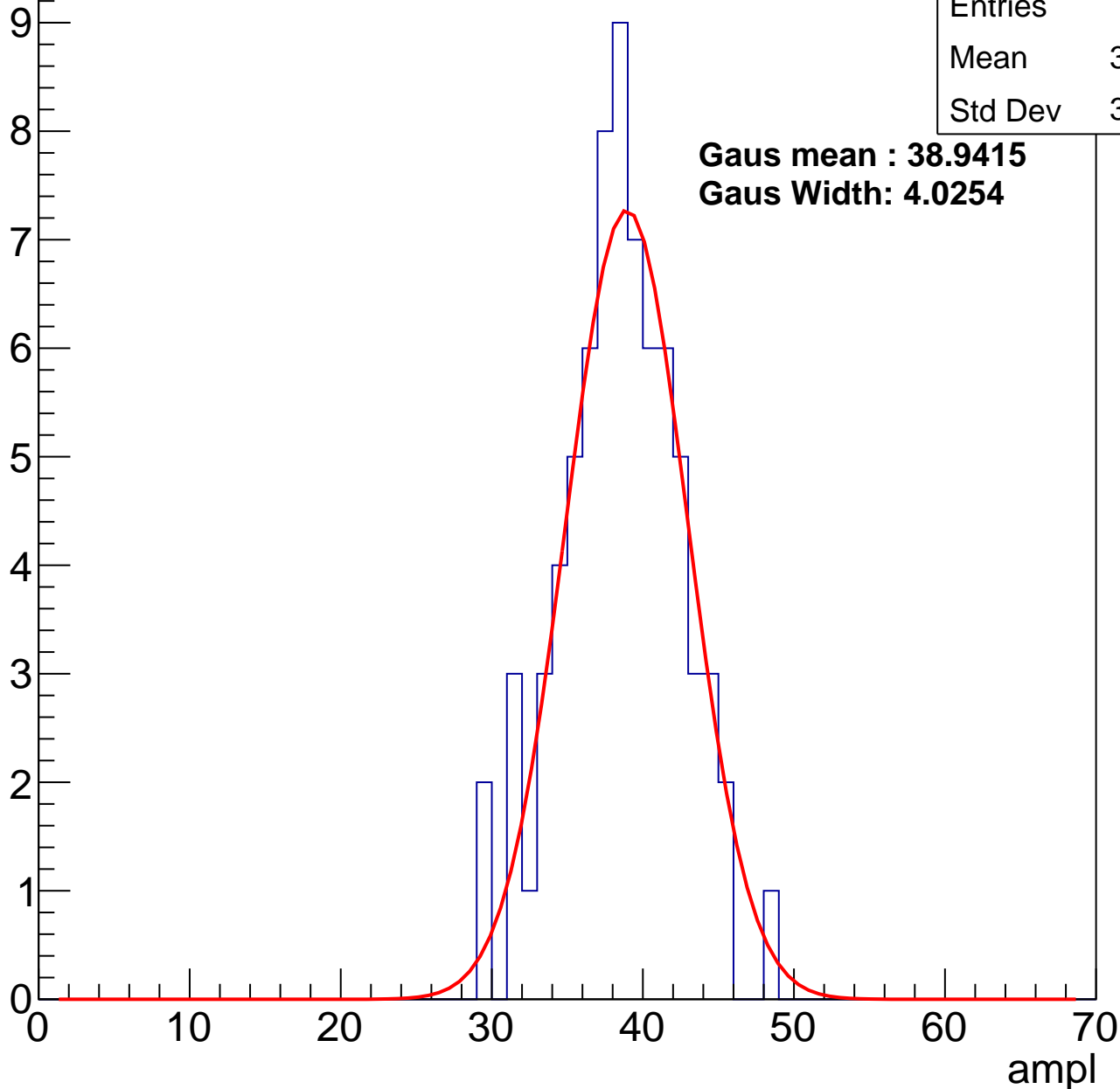
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 74    |
| Mean    | 38.04 |
| Std Dev | 3.868 |

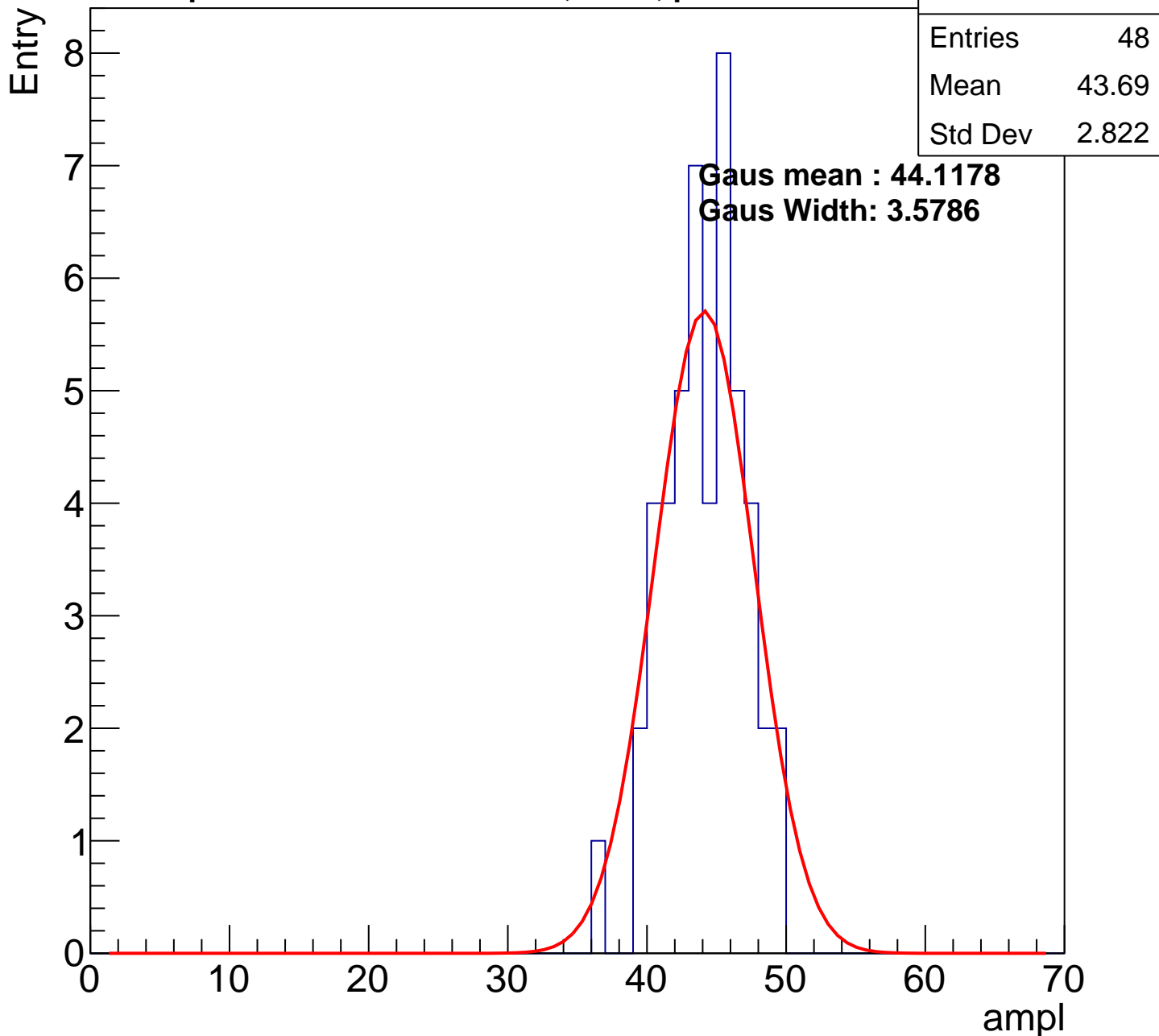
**Gaus mean : 38.9415**

**Gaus Width: 4.0254**



# B0L001S, U2-ch97, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

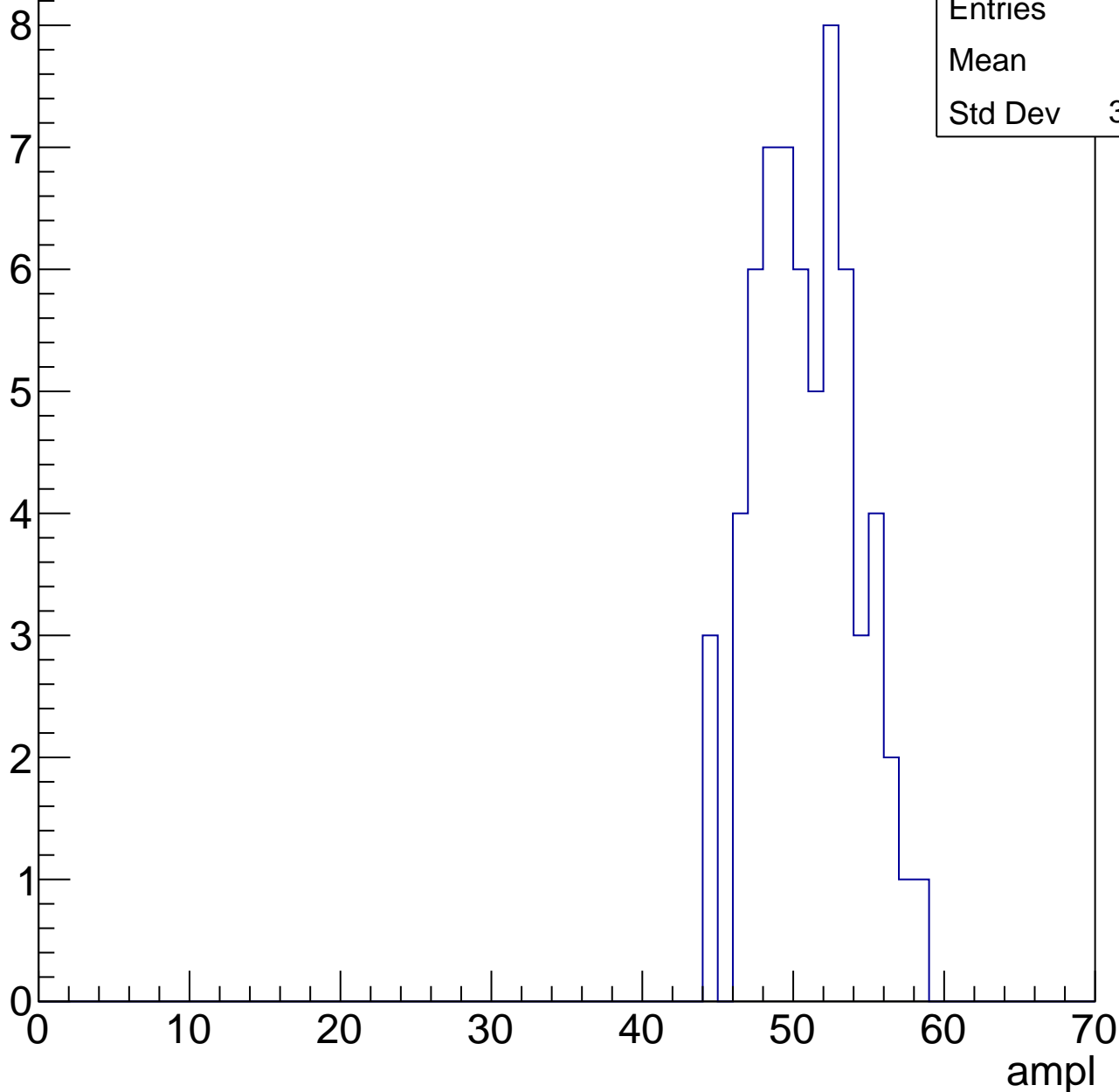


# B0L001S, U2-ch97, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

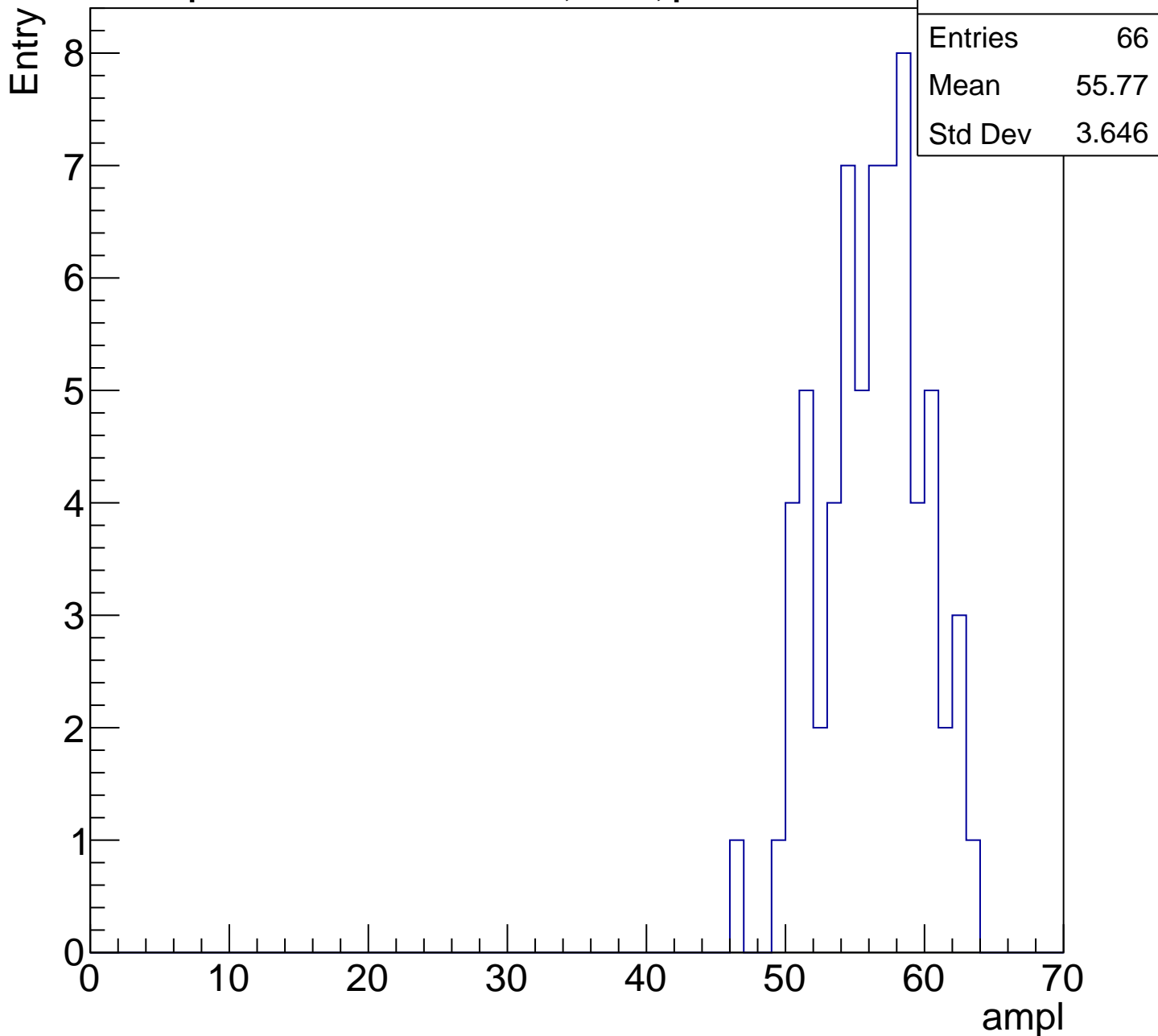
Entry

|         |       |
|---------|-------|
| Entries | 63    |
| Mean    | 50.4  |
| Std Dev | 3.273 |



# B0L001S, U2-ch97, adc4

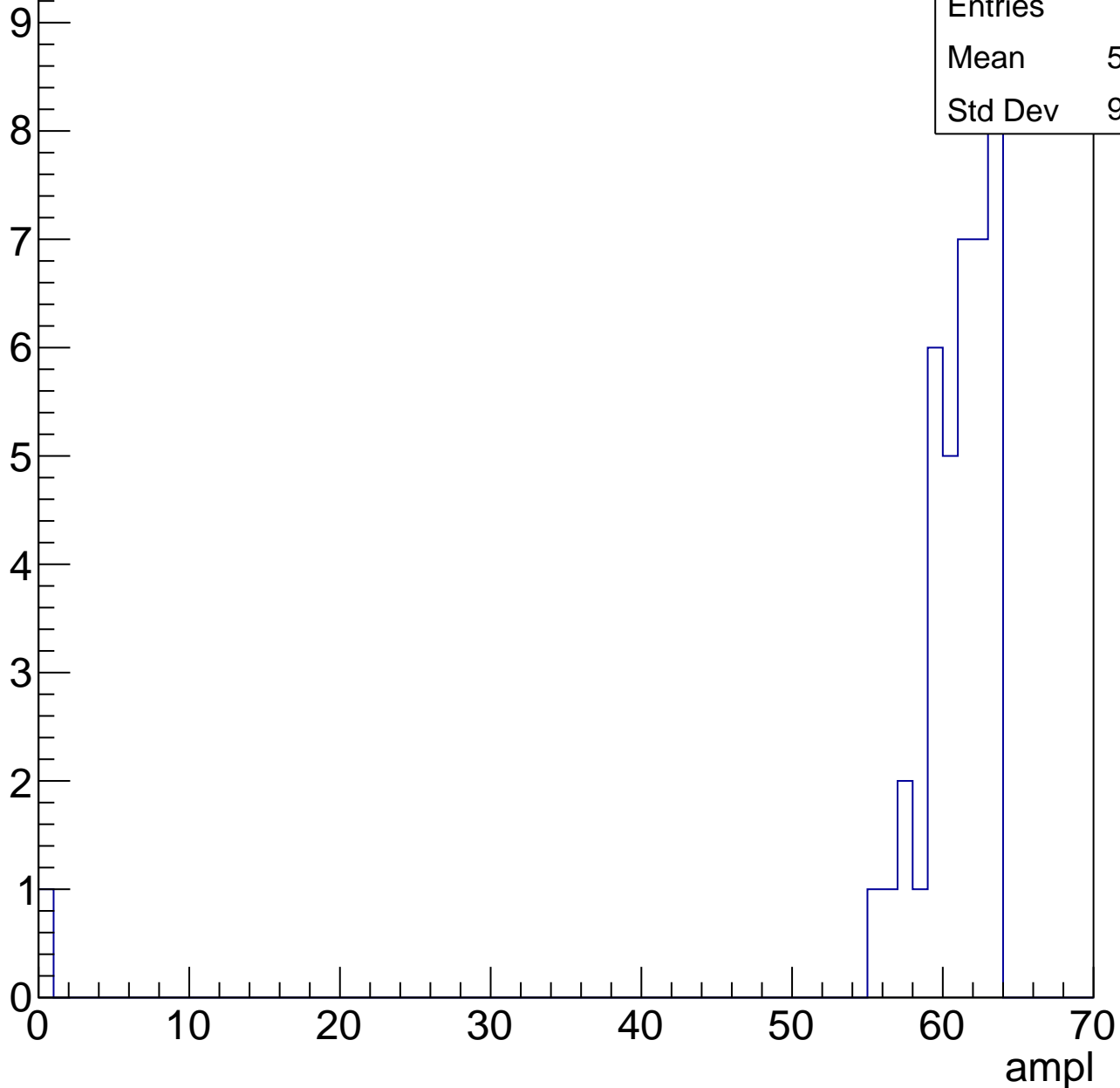
calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U2-ch97, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U2-ch97, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch97, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

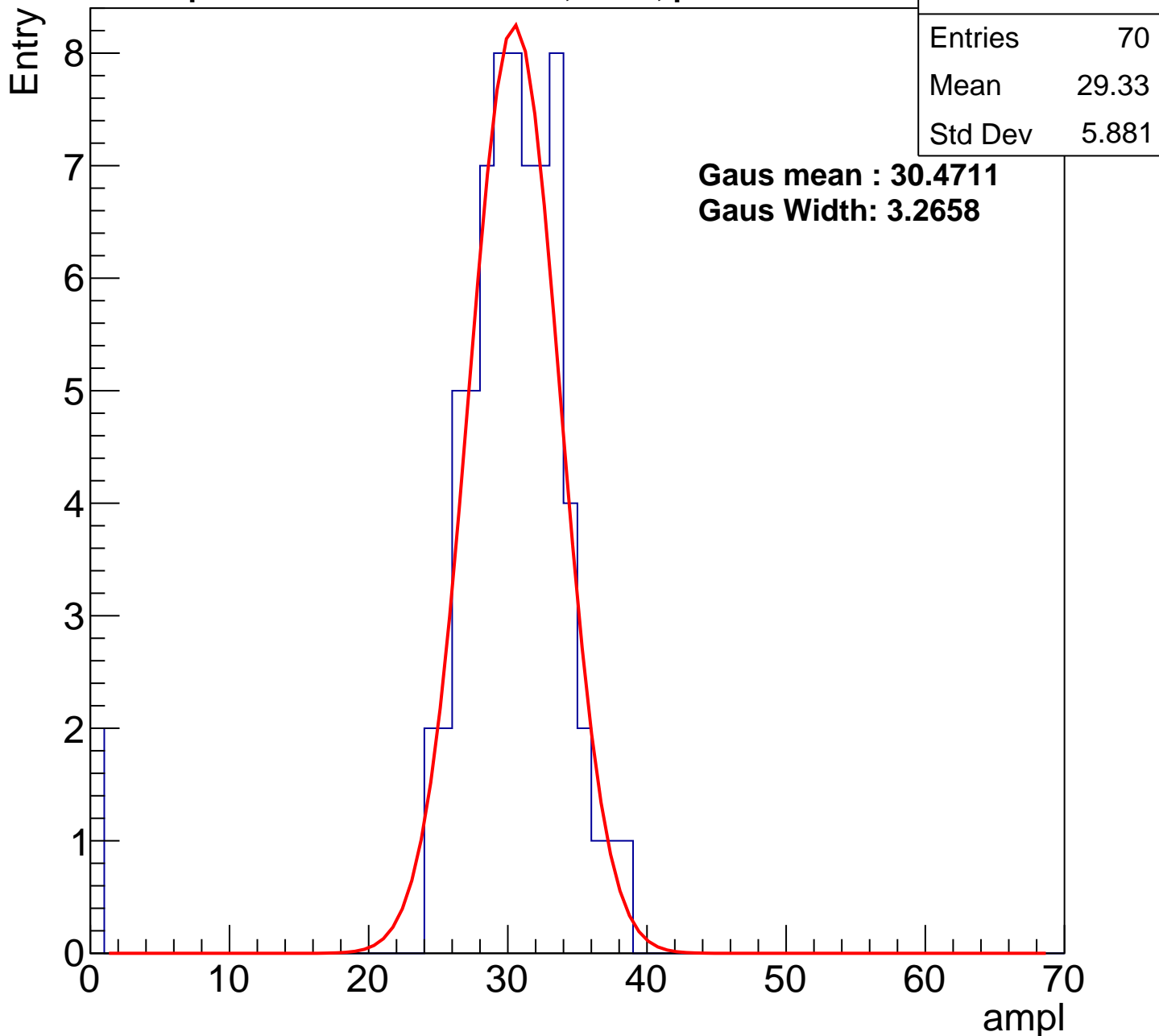
Entry



|         |   |
|---------|---|
| Entries | 0 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch98, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U2-ch98, adc1

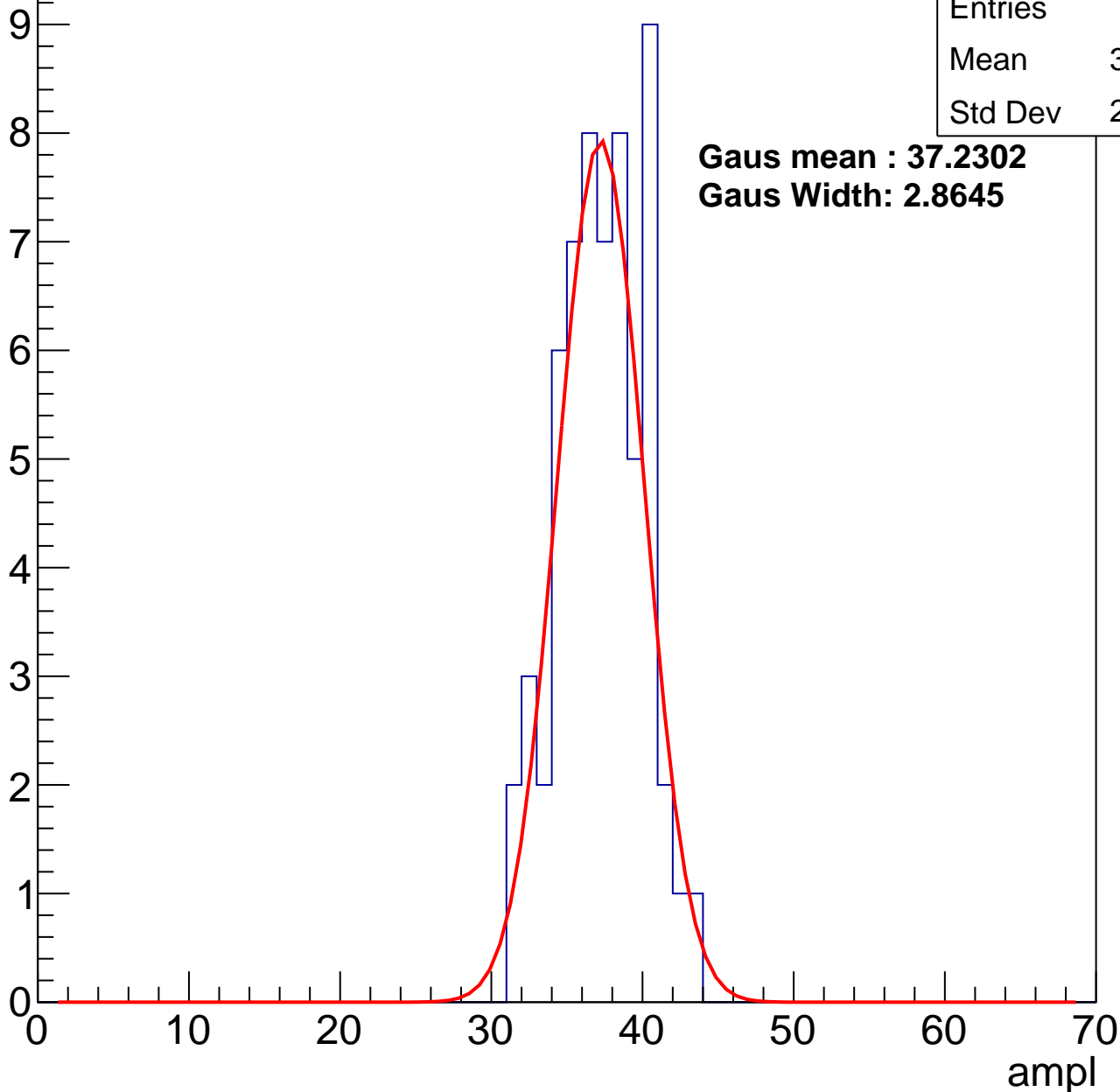
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 61    |
| Mean    | 36.82 |
| Std Dev | 2.773 |

**Gaus mean : 37.2302**

**Gaus Width: 2.8645**



# B0L001S, U2-ch98, adc2

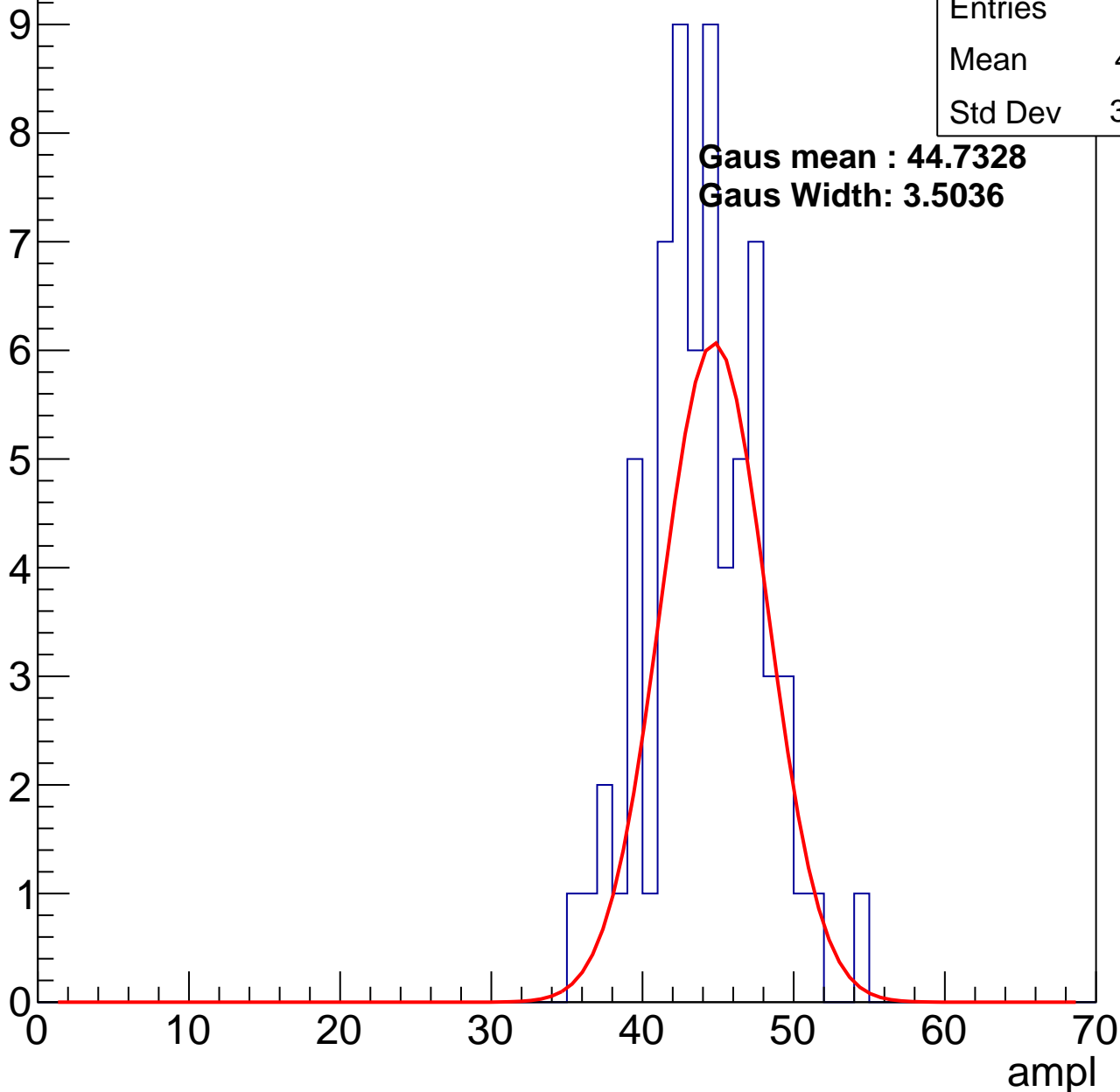
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 67    |
| Mean    | 43.61 |
| Std Dev | 3.685 |

**Gaus mean : 44.7328**

**Gaus Width: 3.5036**

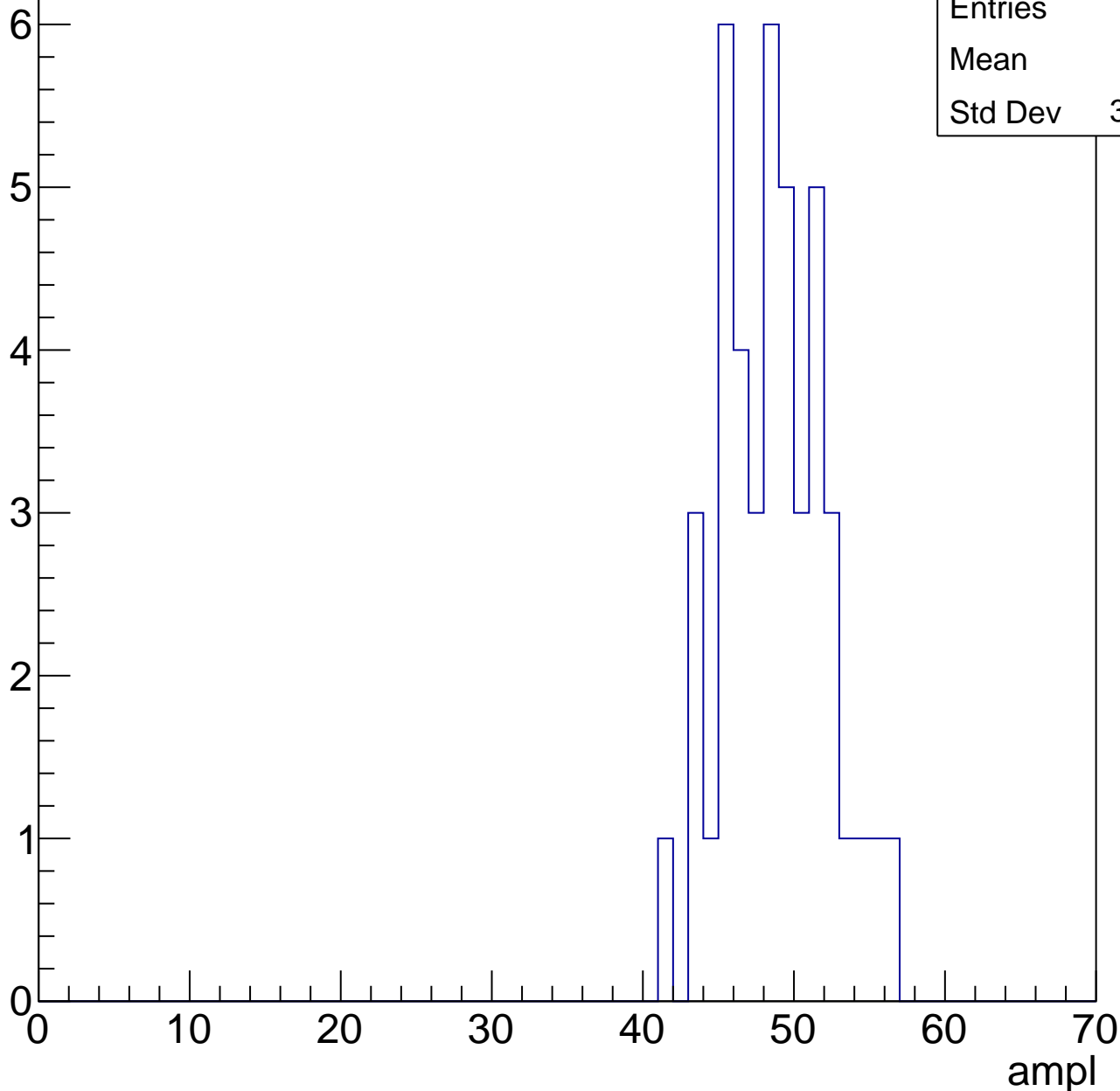


# B0L001S, U2-ch98, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 44    |
| Mean    | 48.2  |
| Std Dev | 3.355 |

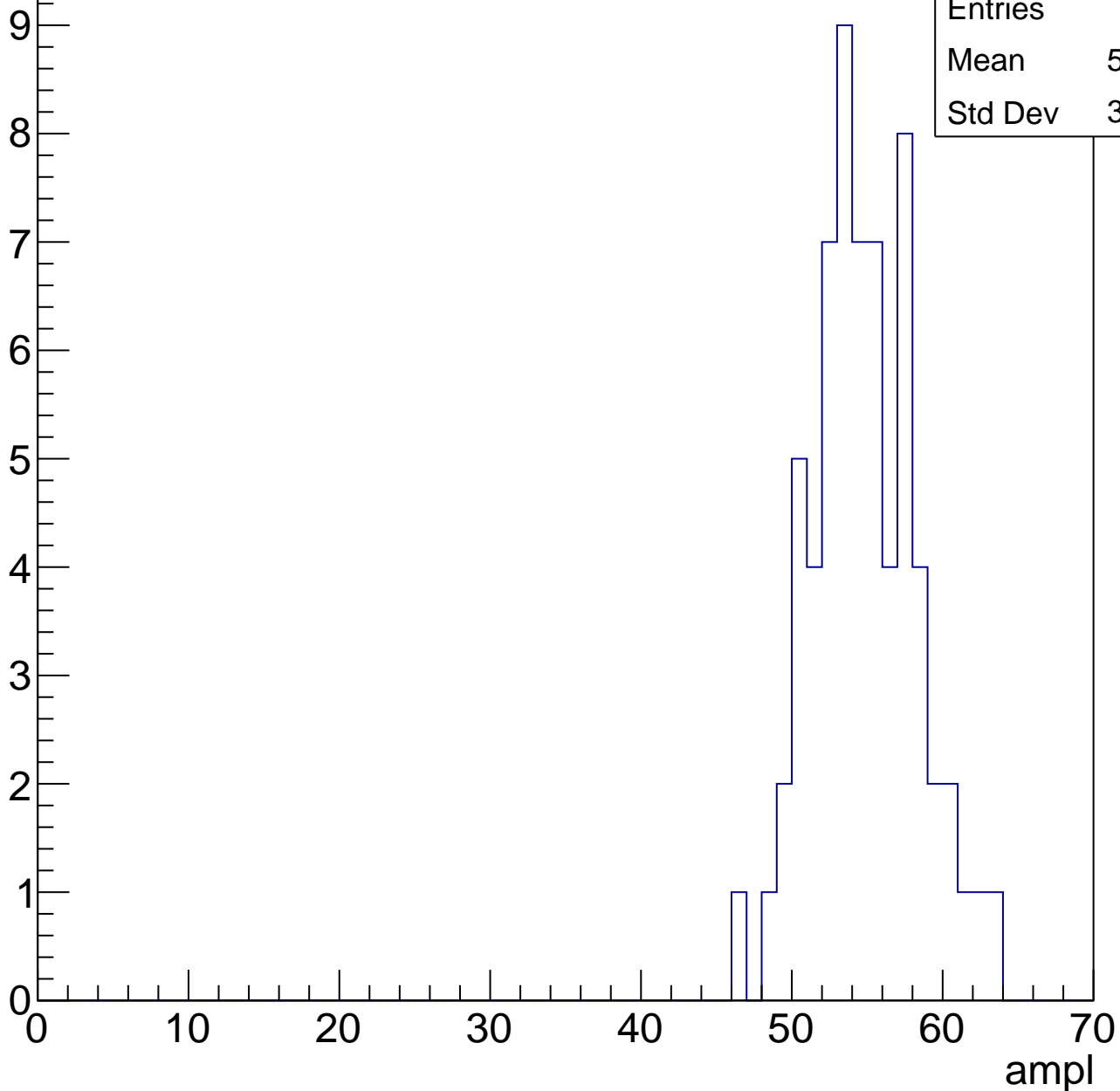


# B0L001S, U2-ch98, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 66    |
| Mean    | 54.33 |
| Std Dev | 3.417 |

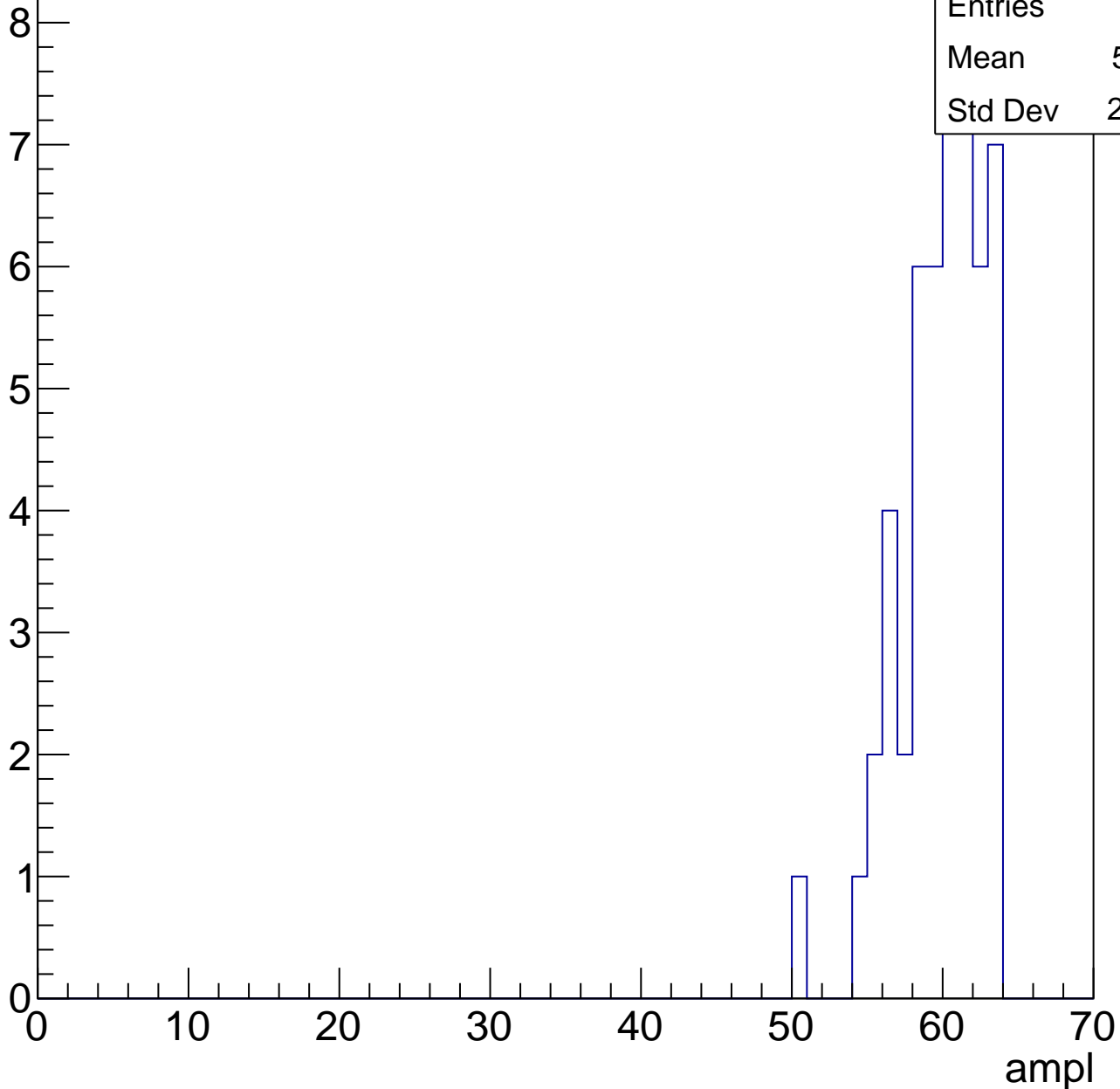


# B0L001S, U2-ch98, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

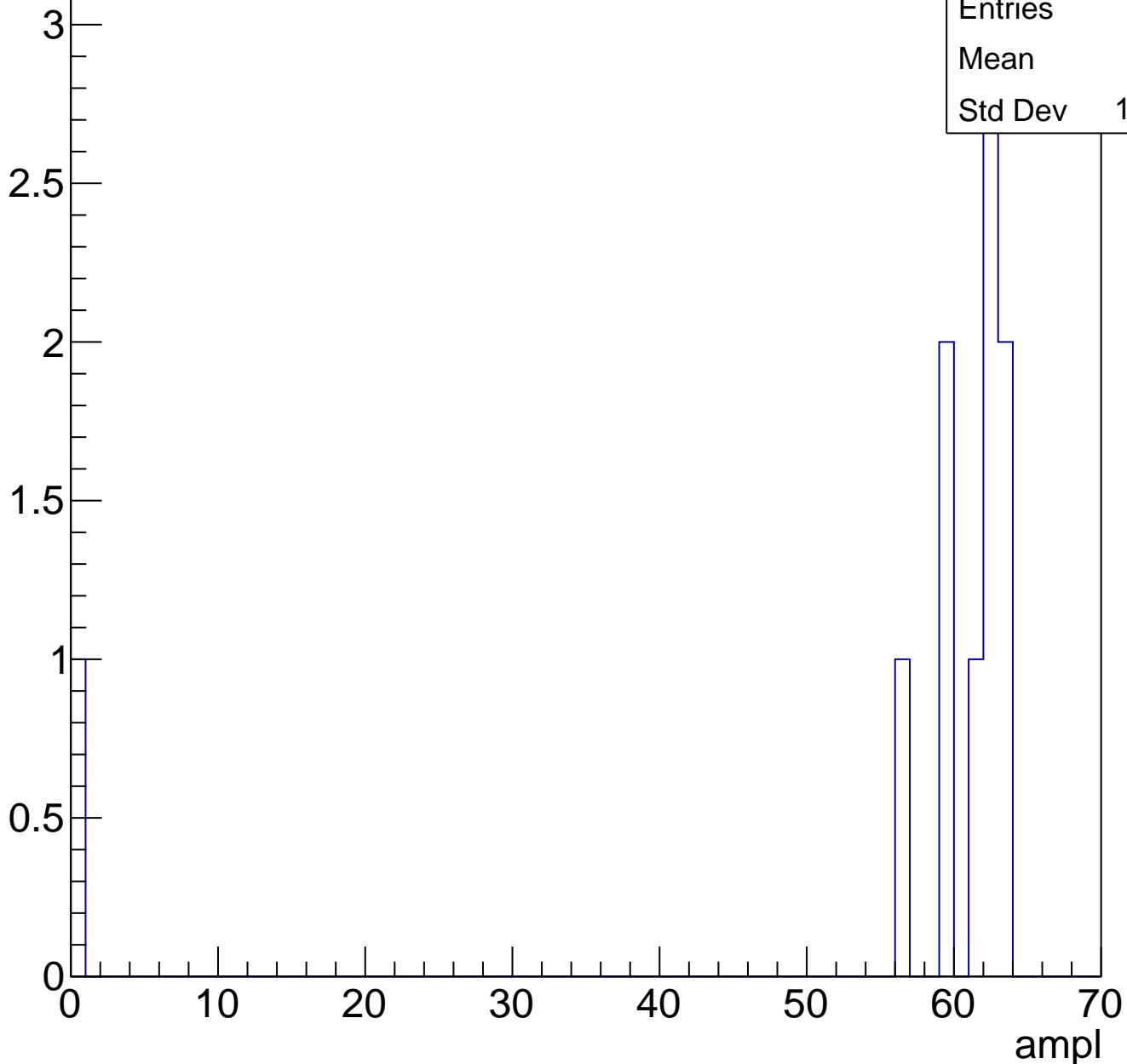
|         |       |
|---------|-------|
| Entries | 51    |
| Mean    | 59.51 |
| Std Dev | 2.732 |



# B0L001S, U2-ch98, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |       |
|---------|-------|
| Entries | 10    |
| Mean    | 54.7  |
| Std Dev | 18.35 |



# B0L001S, U2-ch98, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 0 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch99, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 81    |
| Mean    | 30.75 |
| Std Dev | 6.153 |

**Gaus mean : 31.2651**

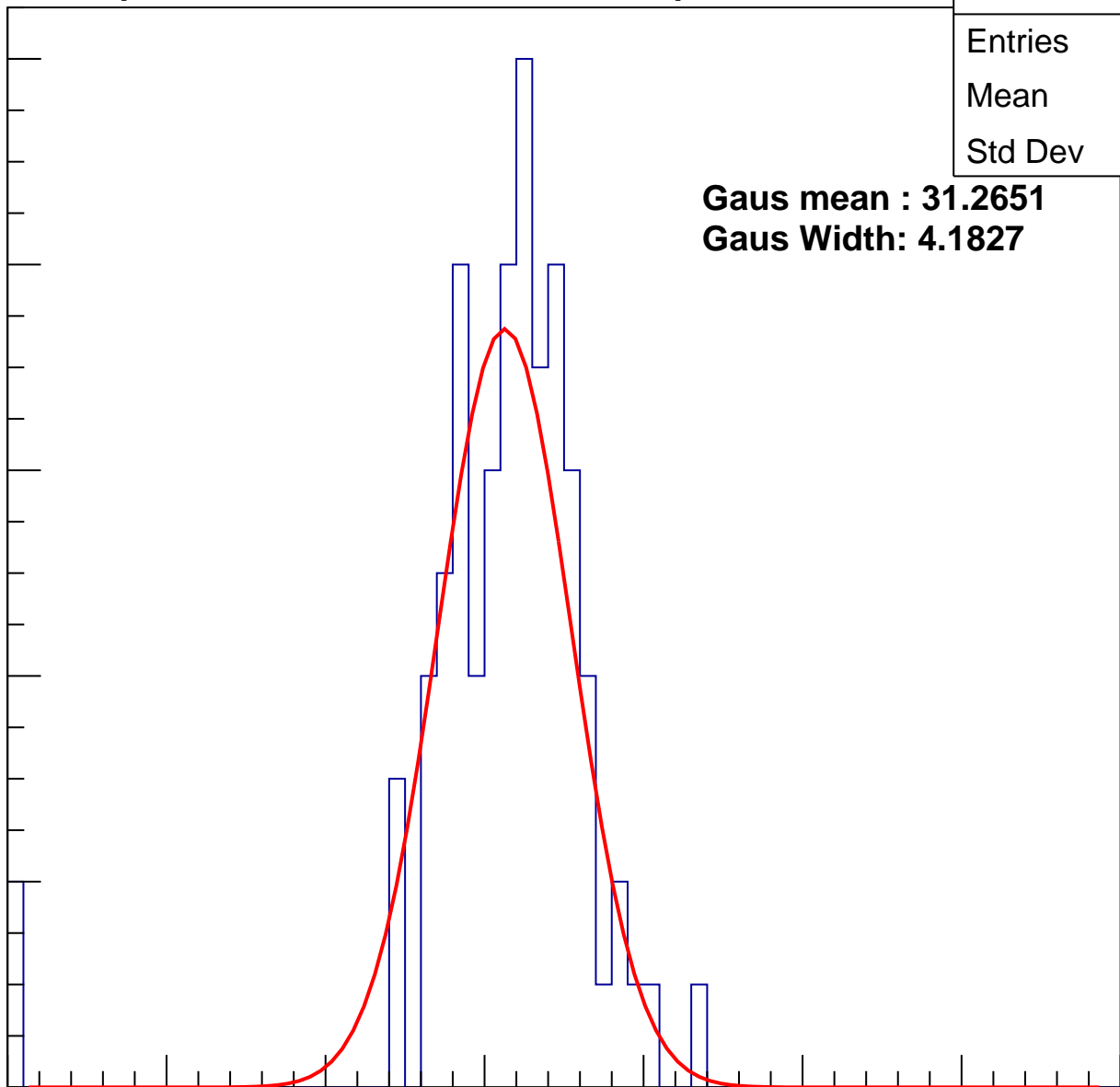
**Gaus Width: 4.1827**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U2-ch99, adc1

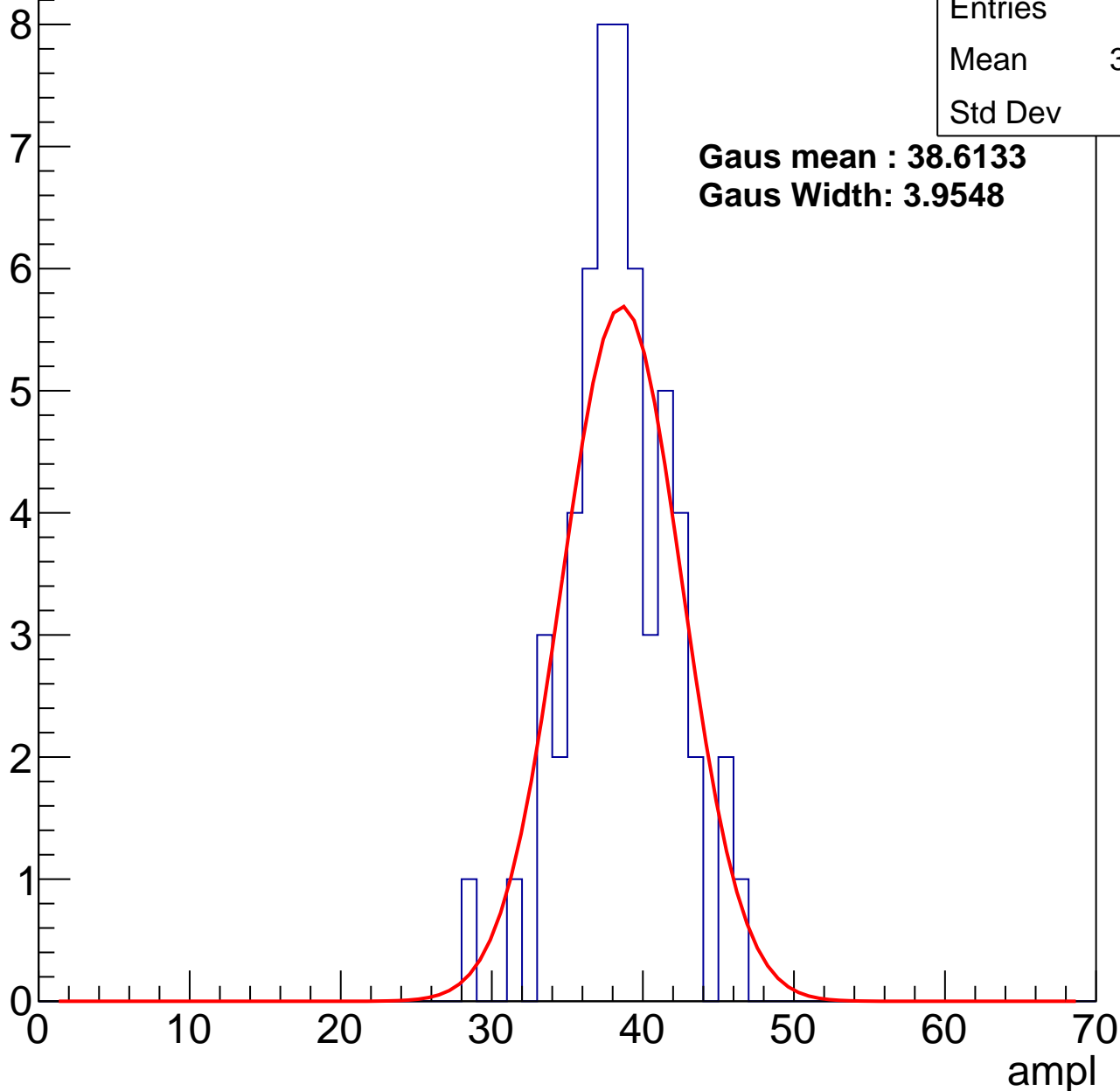
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 56    |
| Mean    | 38.05 |
| Std Dev | 3.44  |

**Gaus mean : 38.6133**

**Gaus Width: 3.9548**



# B0L001S, U2-ch99, adc2

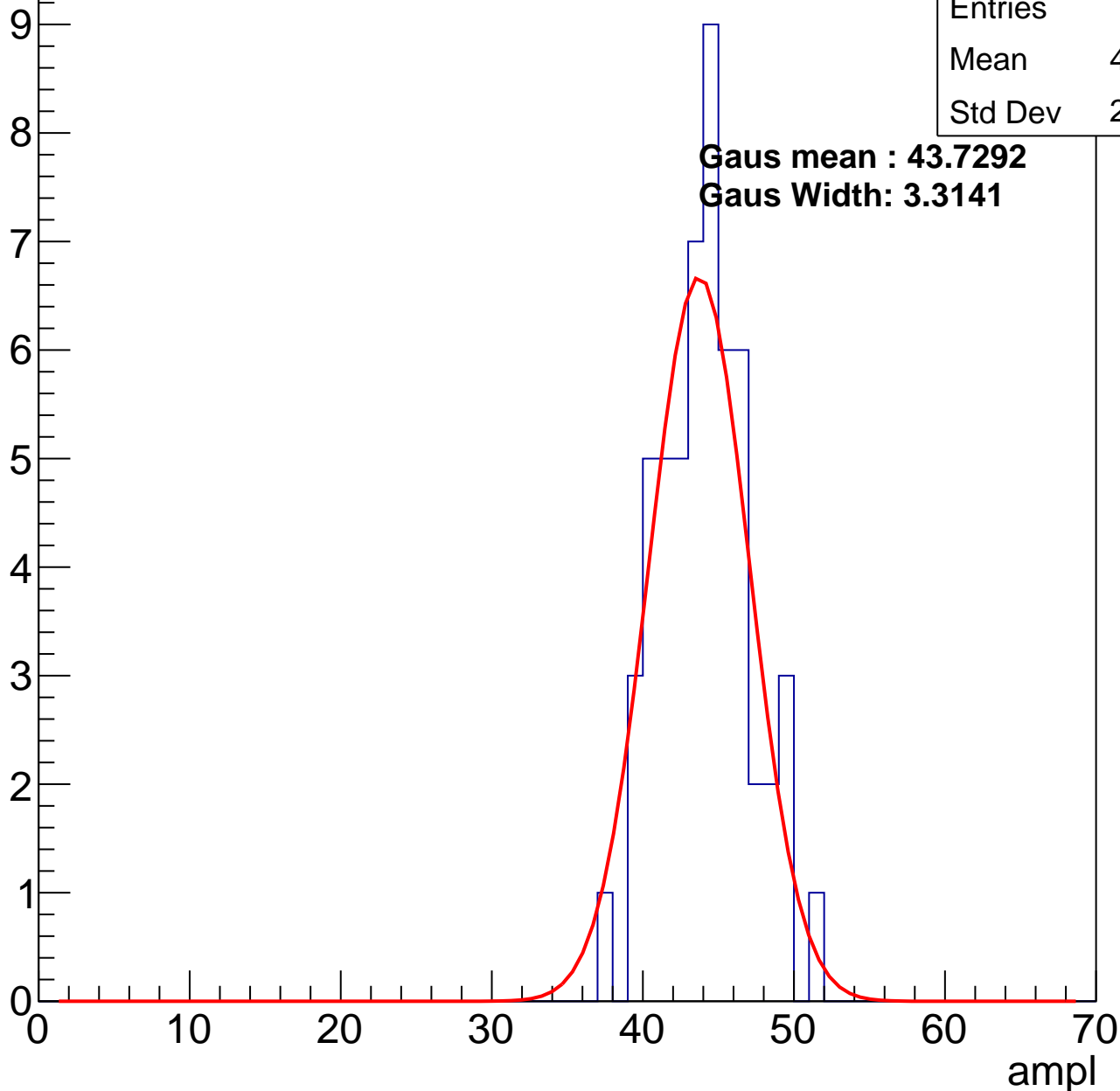
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 55    |
| Mean    | 43.64 |
| Std Dev | 2.932 |

**Gaus mean : 43.7292**

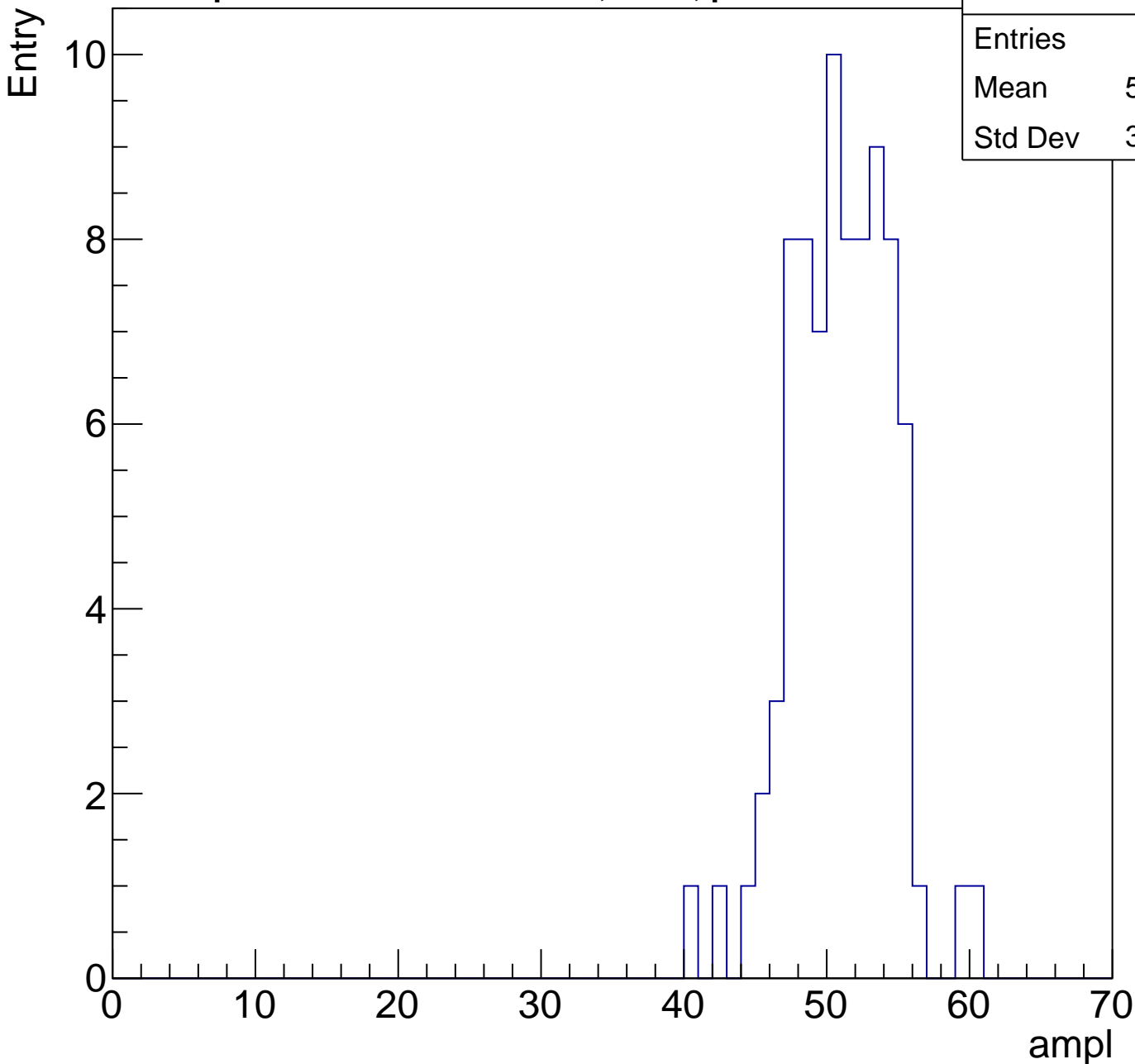
**Gaus Width: 3.3141**



# B0L001S, U2-ch99, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 83    |
| Mean    | 50.54 |
| Std Dev | 3.472 |

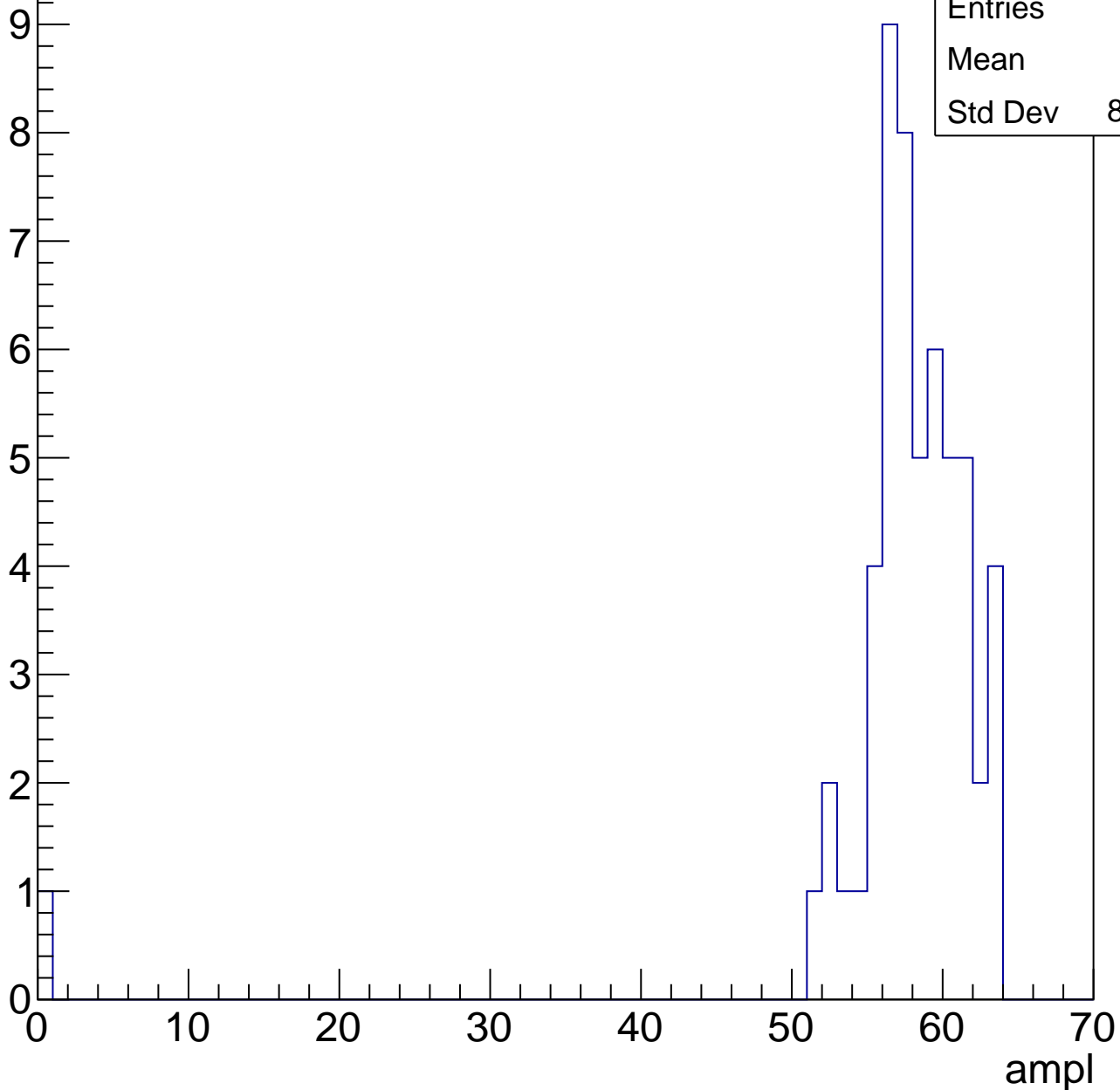


# B0L001S, U2-ch99, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 54    |
| Mean    | 56.8  |
| Std Dev | 8.312 |

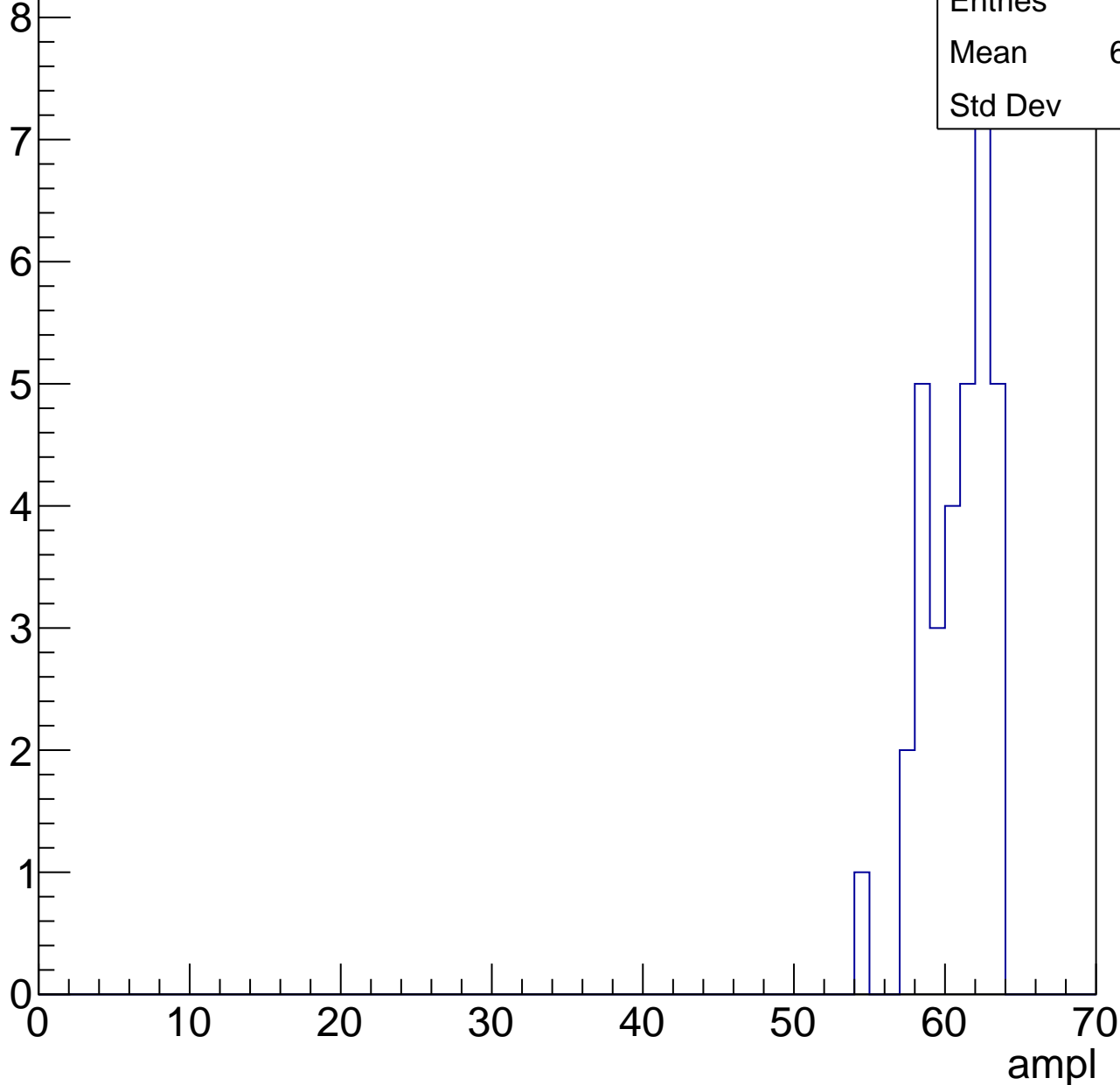


# B0L001S, U2-ch99, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 33    |
| Mean    | 60.33 |
| Std Dev | 2.17  |



# B0L001S, U2-ch99, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 0 |
| Mean    | 0 |
| Std Dev | 0 |



# B0L001S, U2-ch99, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U2-ch100, adc0

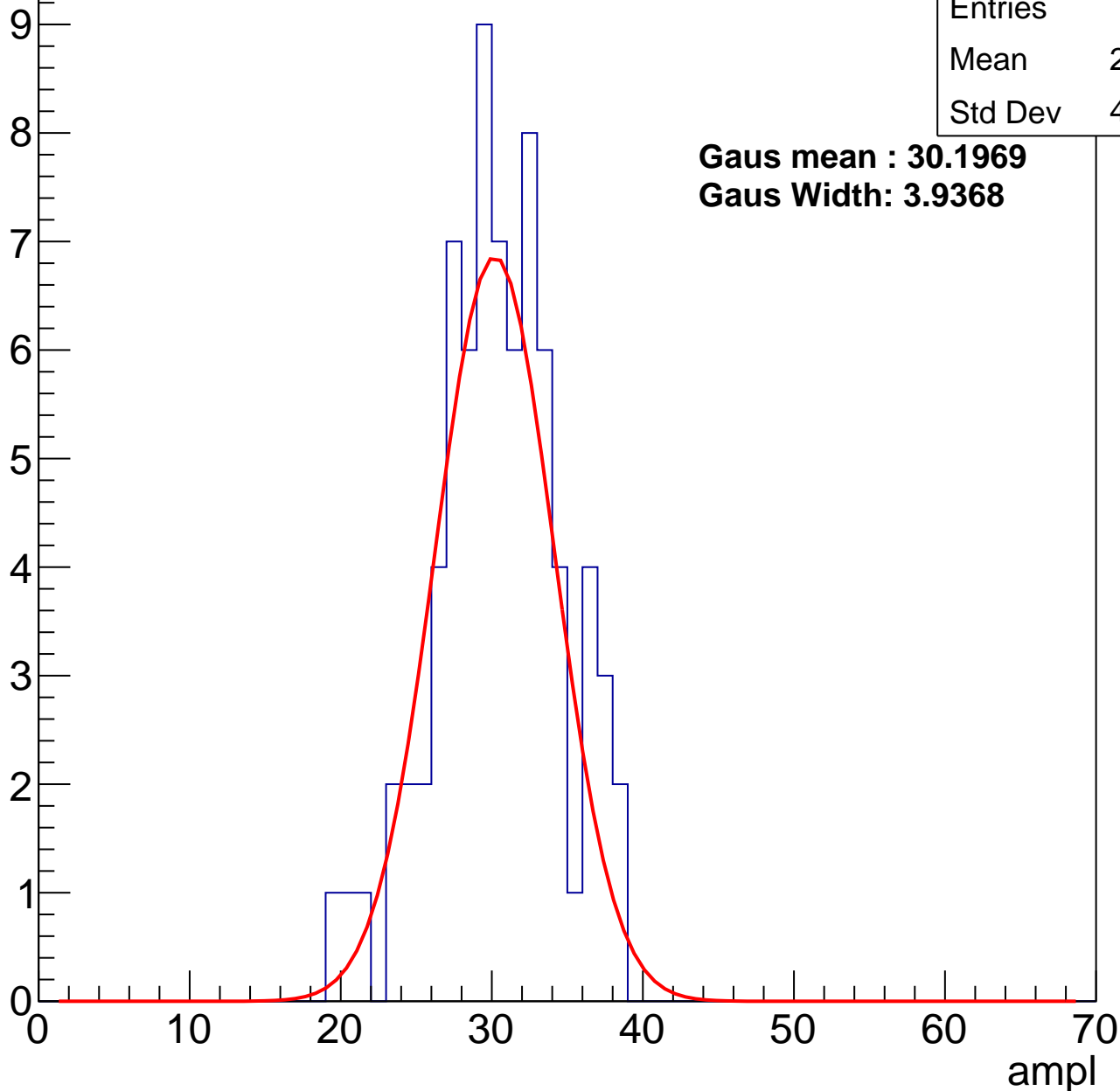
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 76    |
| Mean    | 29.97 |
| Std Dev | 4.107 |

**Gaus mean : 30.1669**

**Gaus Width: 3.9368**



# B0L001S, U2-ch100, adc1

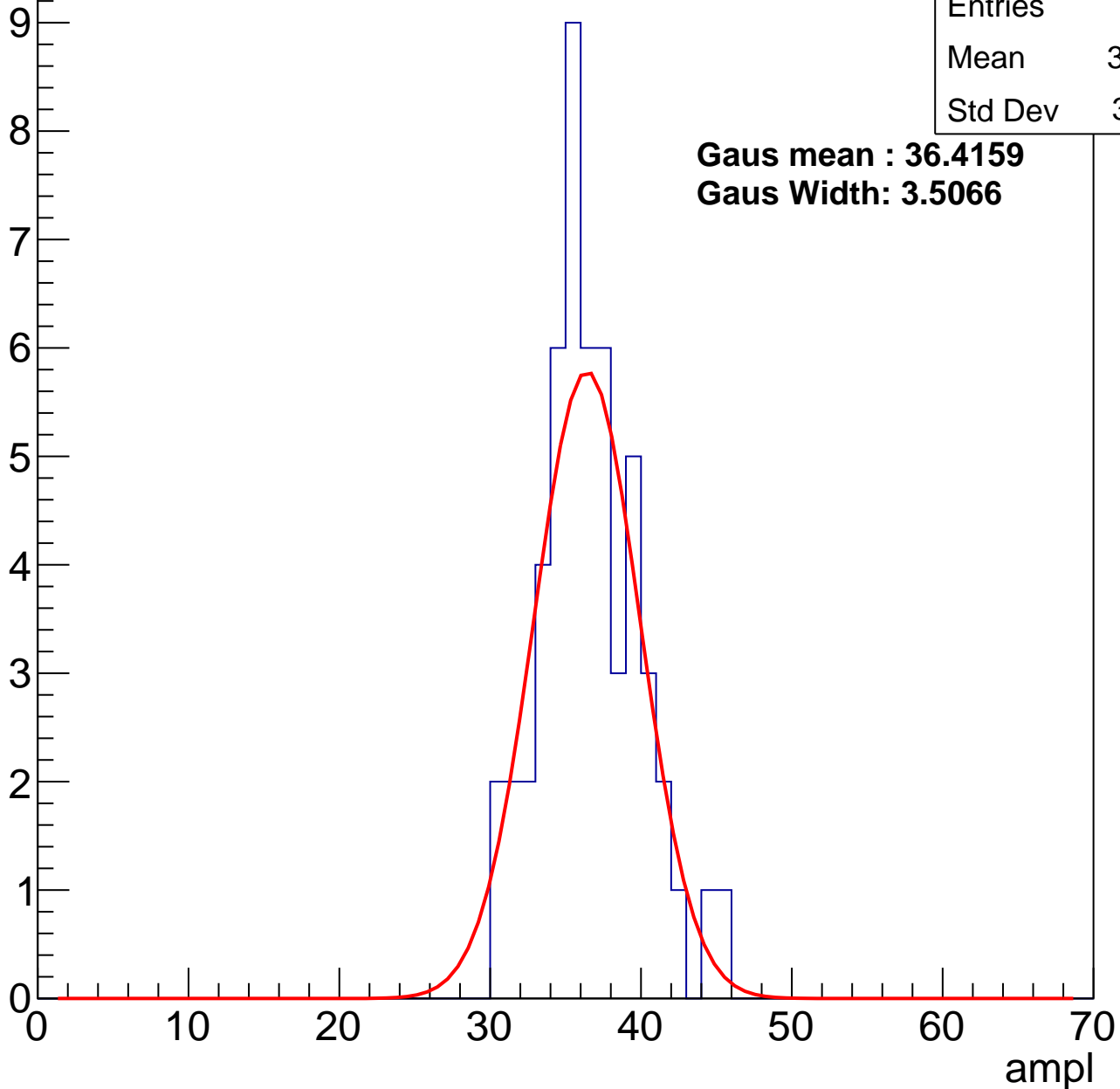
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 53    |
| Mean    | 36.17 |
| Std Dev | 3.261 |

**Gaus mean : 36.4159**

**Gaus Width: 3.5066**



# B0L001S, U2-ch100, adc2

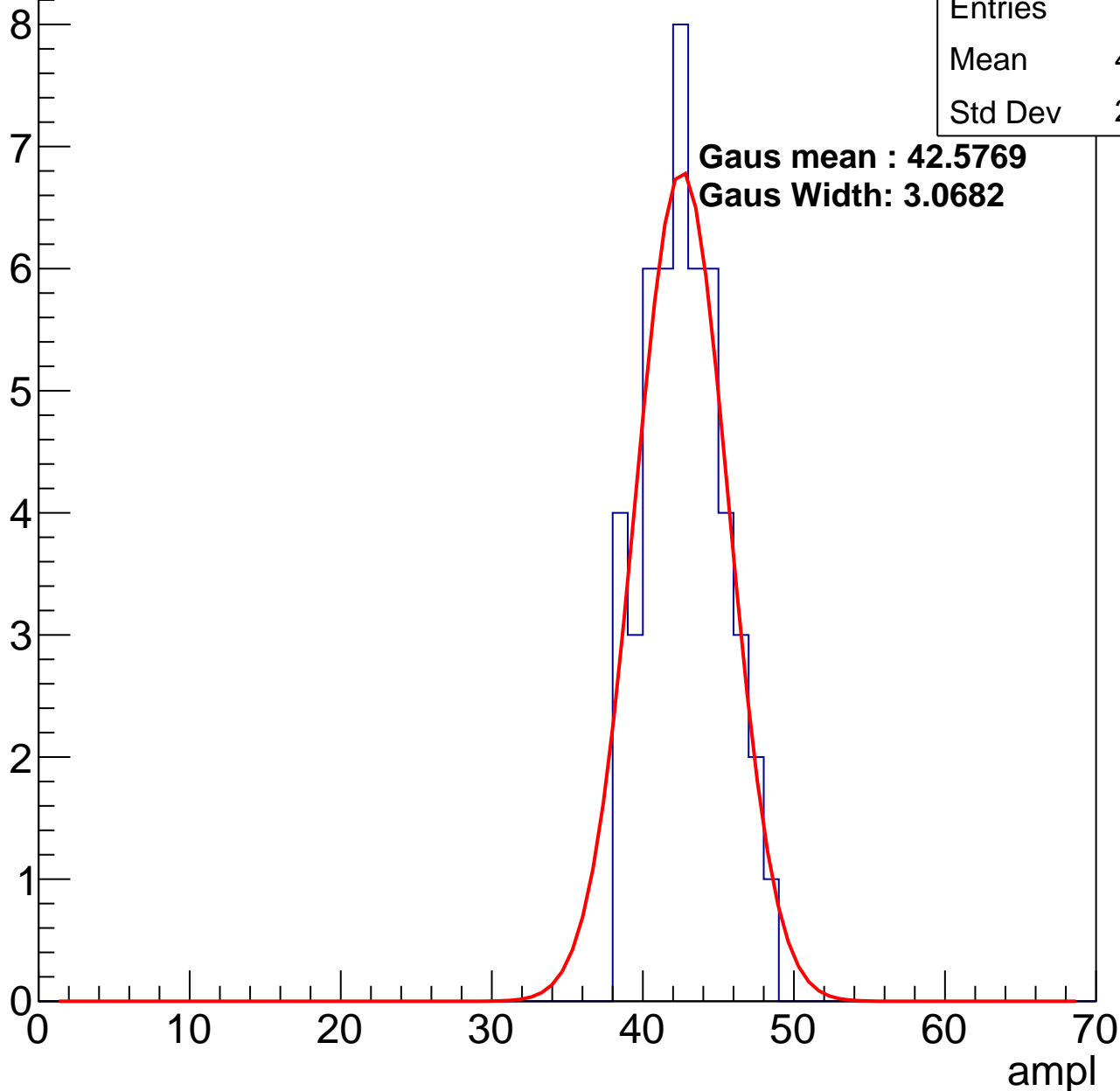
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 49    |
| Mean    | 42.31 |
| Std Dev | 2.541 |

**Gaus mean : 42.5769**

**Gaus Width: 3.0682**

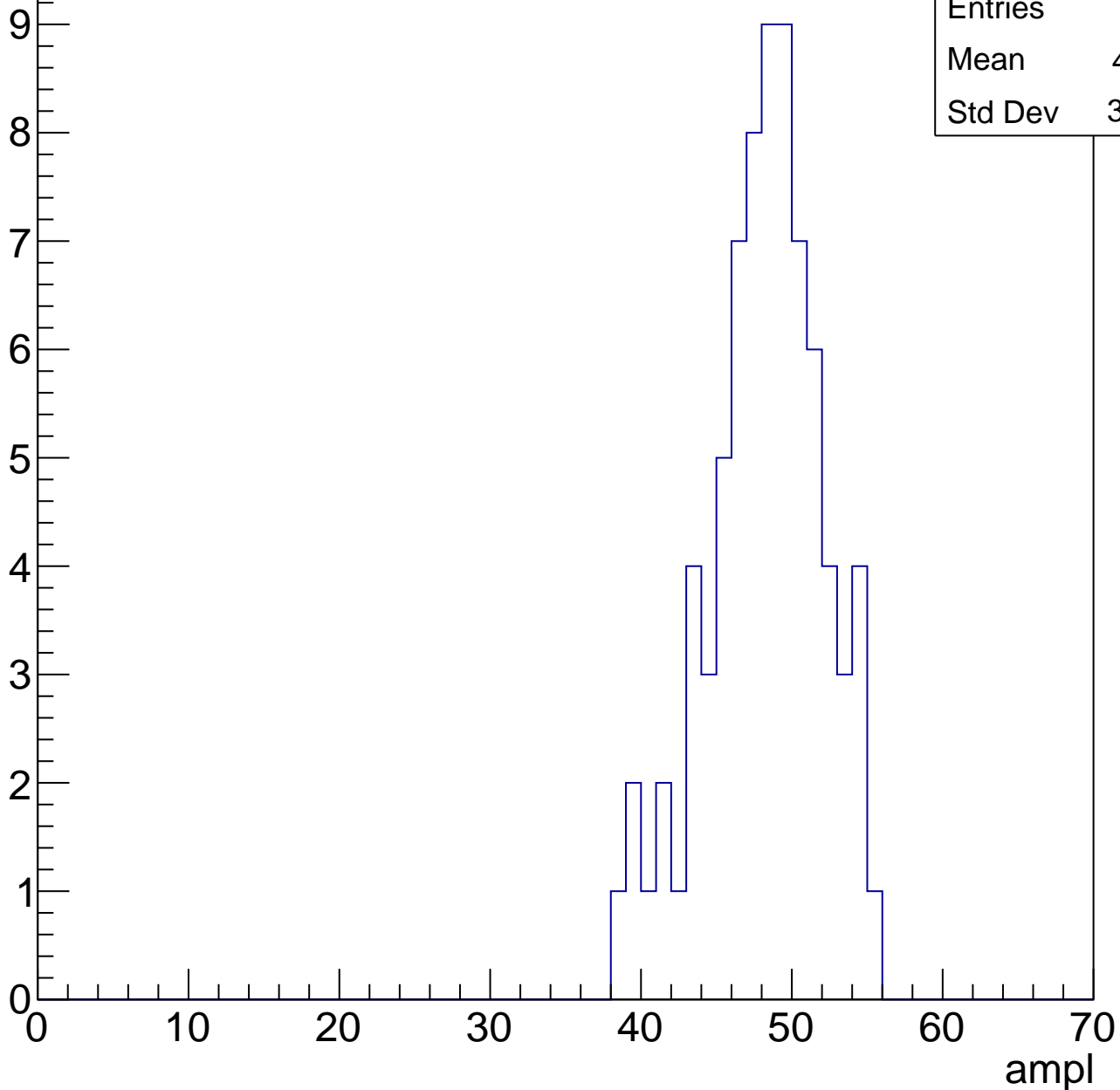


# B0L001S, U2-ch100, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 77    |
| Mean    | 47.71 |
| Std Dev | 3.789 |

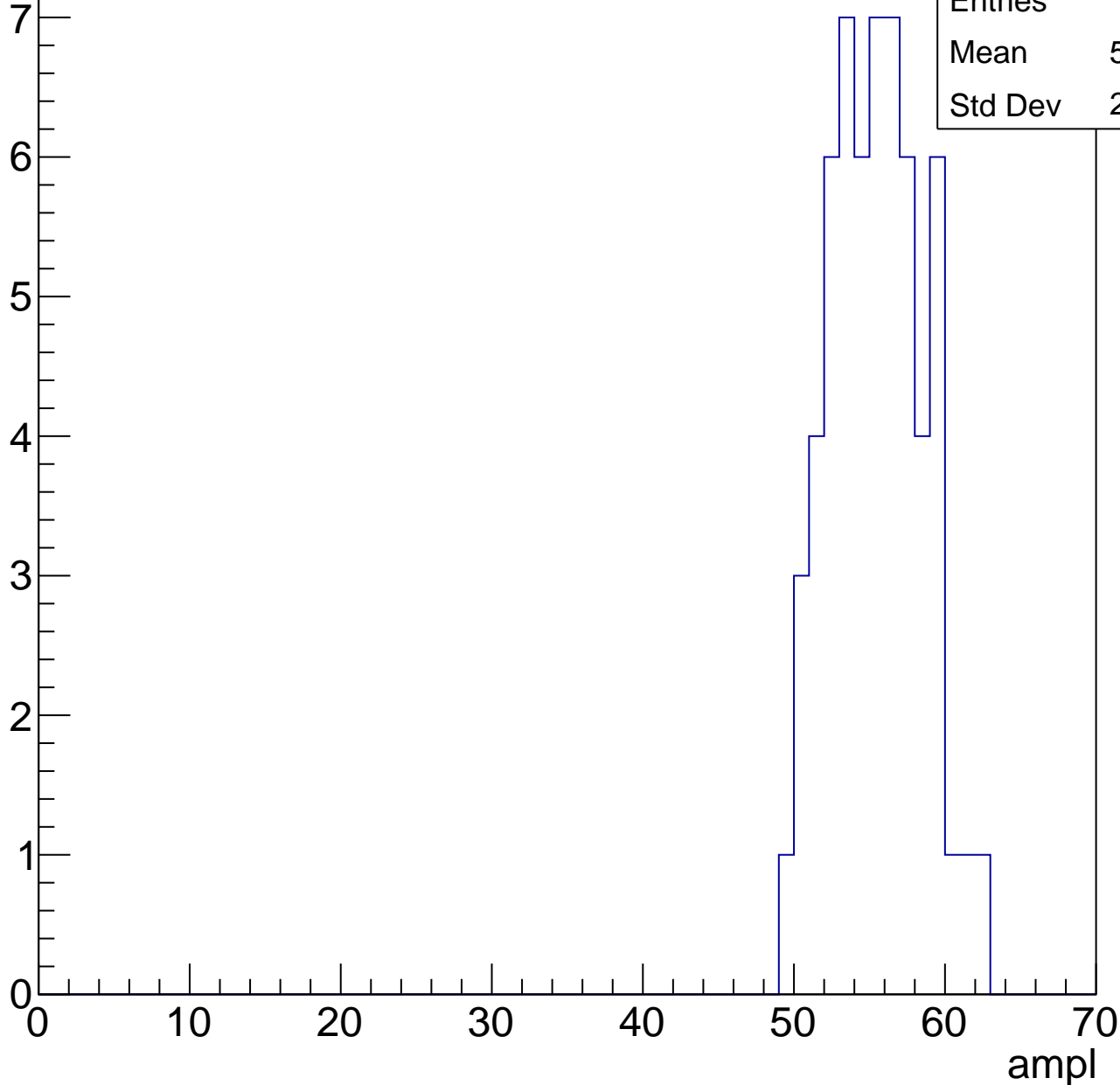


# B0L001S, U2-ch100, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 60    |
| Mean    | 54.97 |
| Std Dev | 2.989 |

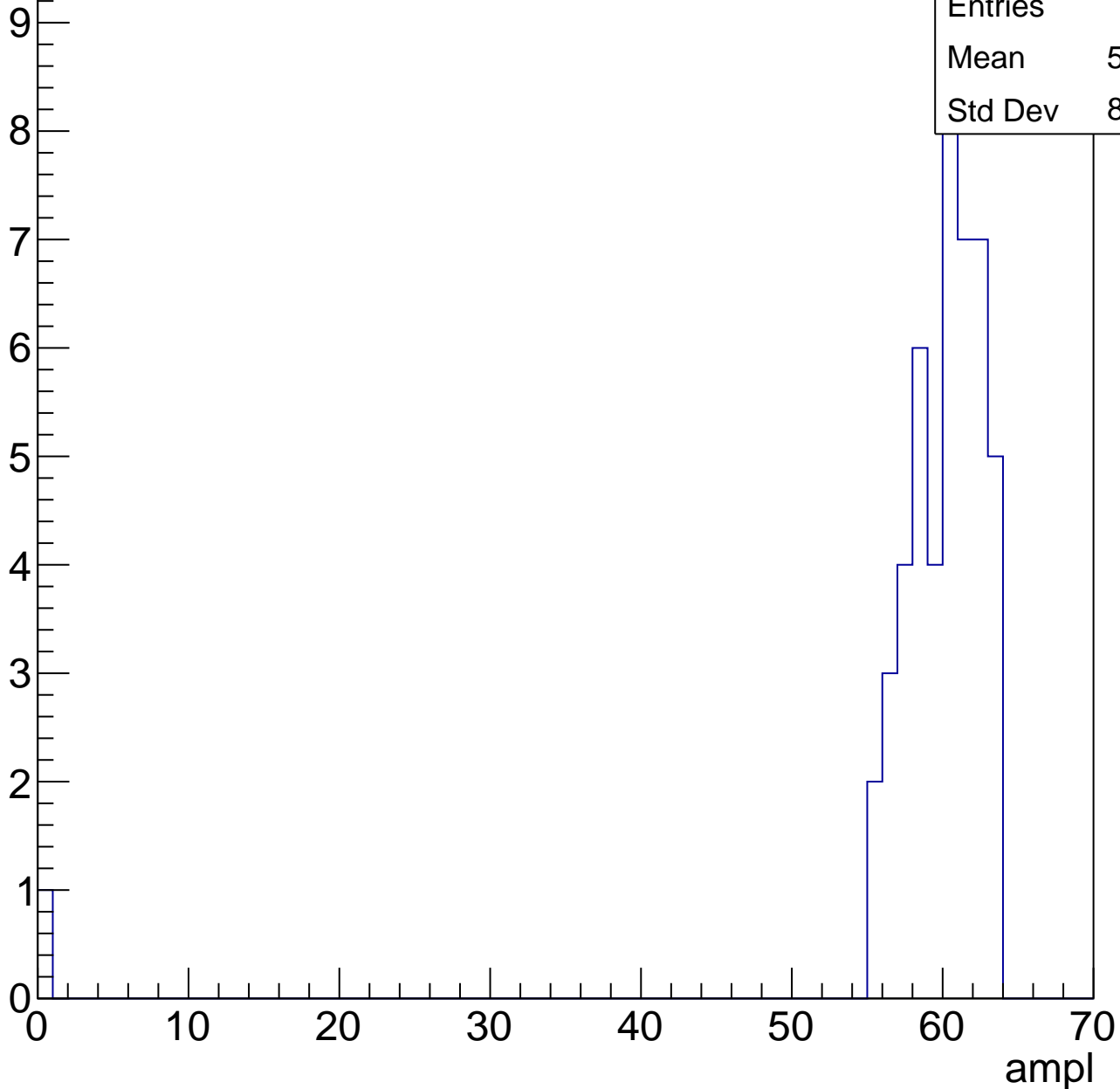


# B0L001S, U2-ch100, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 48    |
| Mean    | 58.46 |
| Std Dev | 8.813 |

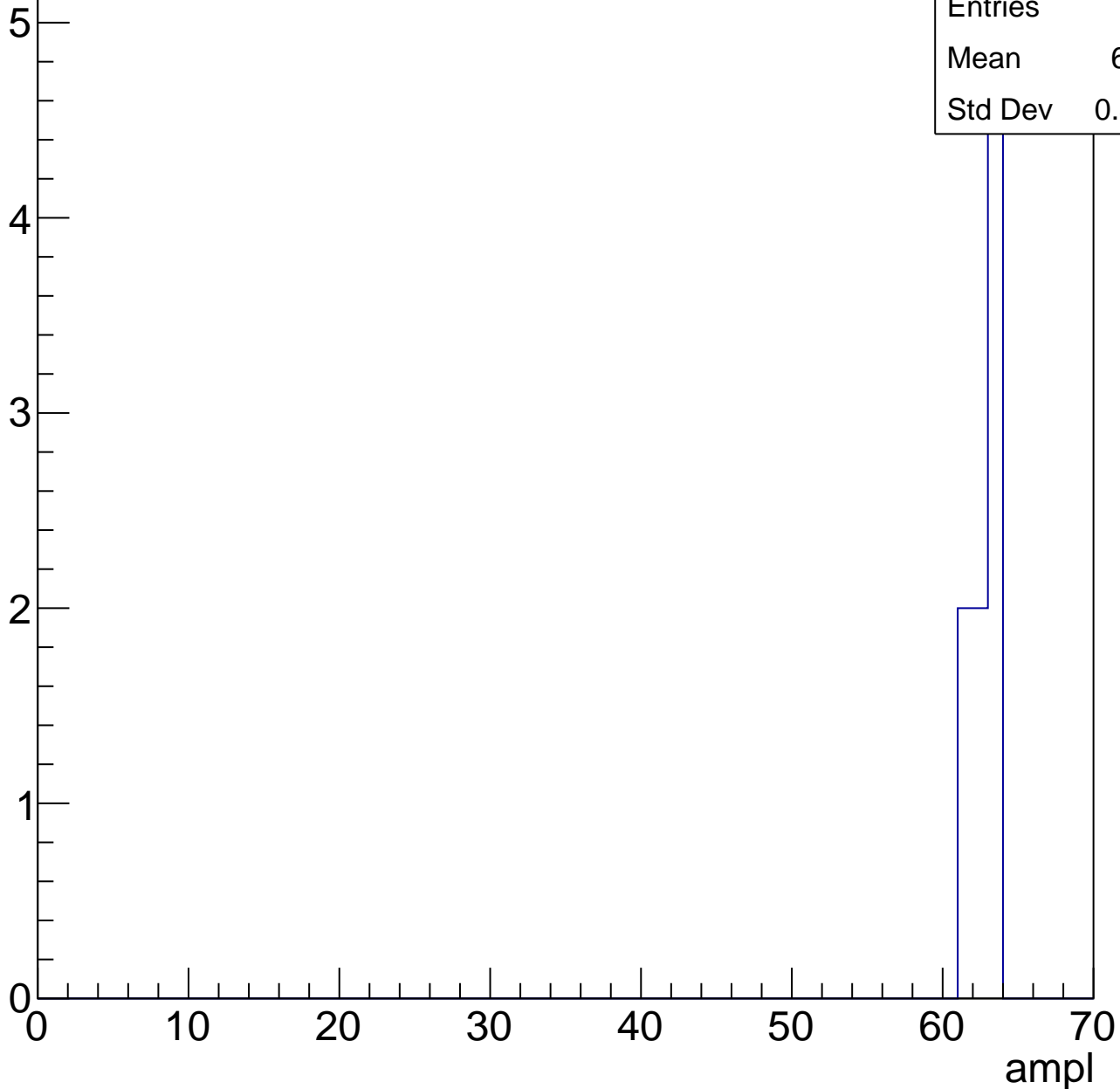


# B0L001S, U2-ch100, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |        |
|---------|--------|
| Entries | 9      |
| Mean    | 62.33  |
| Std Dev | 0.8165 |





# B0L001S, U2-ch100, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U2-ch101, adc0

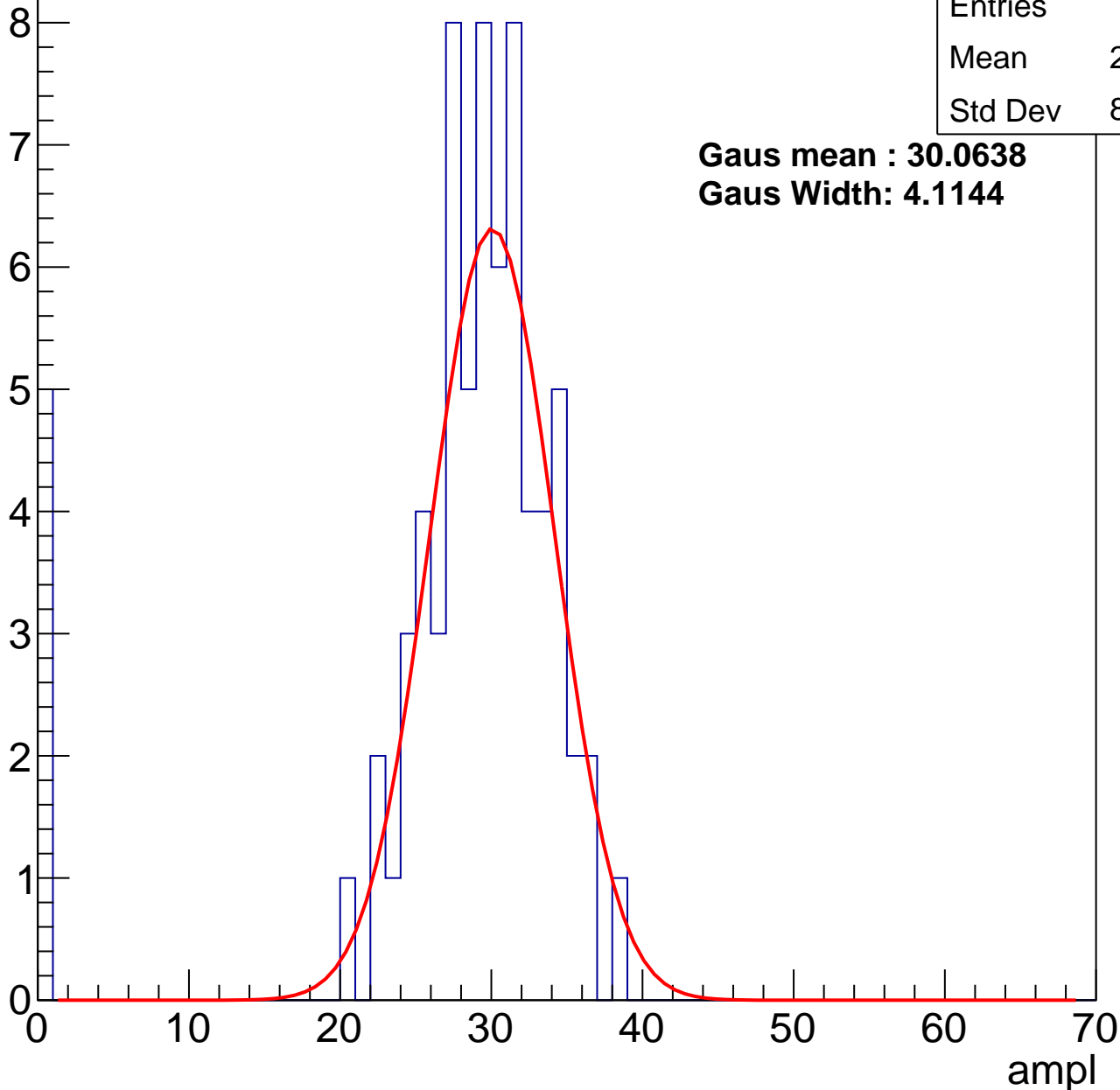
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 72    |
| Mean    | 27.26 |
| Std Dev | 8.266 |

**Gaus mean : 30.0638**

**Gaus Width: 4.1144**



# B0L001S, U2-ch101, adc1

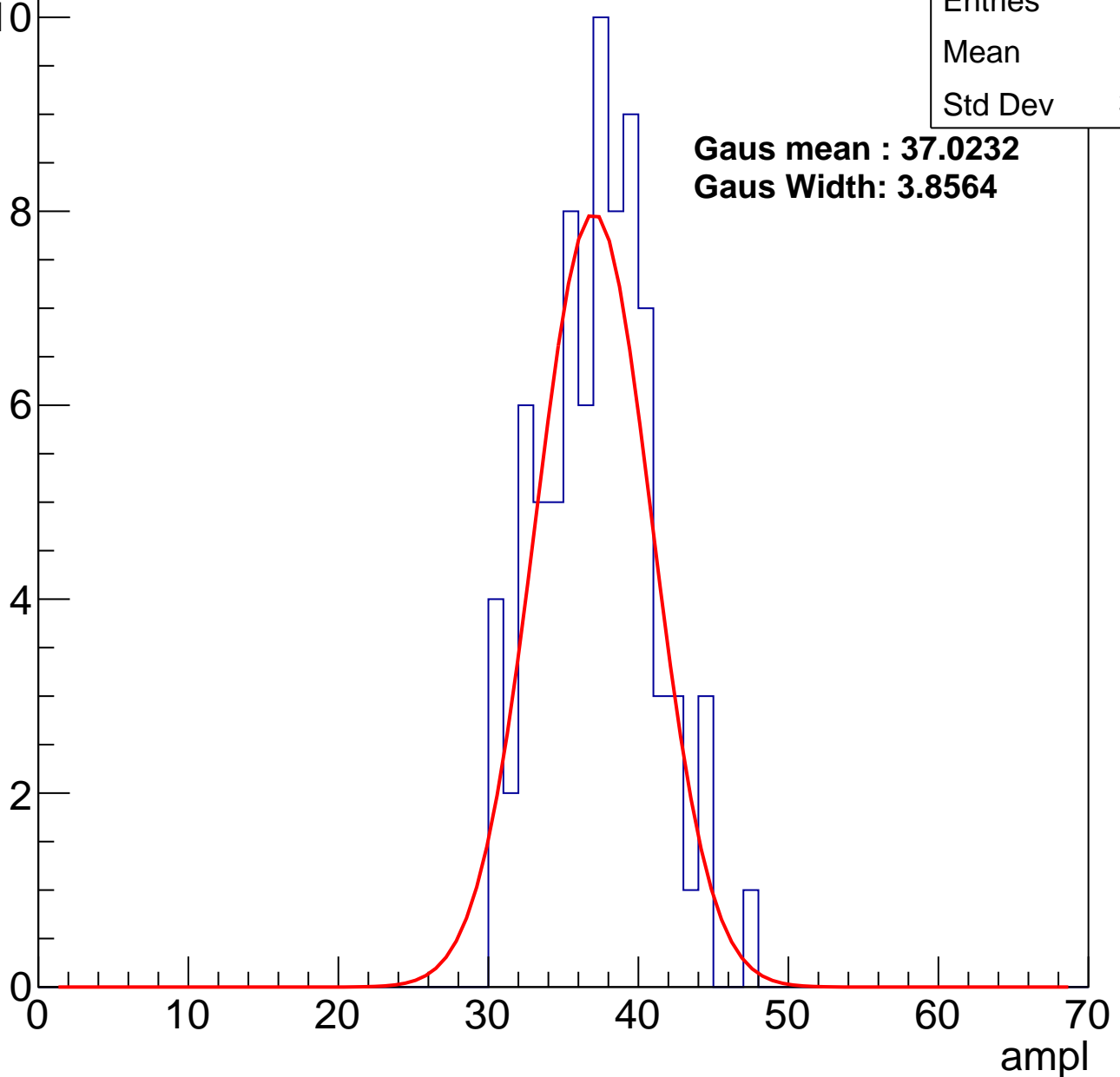
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |      |
|---------|------|
| Entries | 81   |
| Mean    | 36.8 |
| Std Dev | 3.67 |

**Gaus mean : 37.0232**

**Gaus Width: 3.8564**



# B0L001S, U2-ch101, adc2

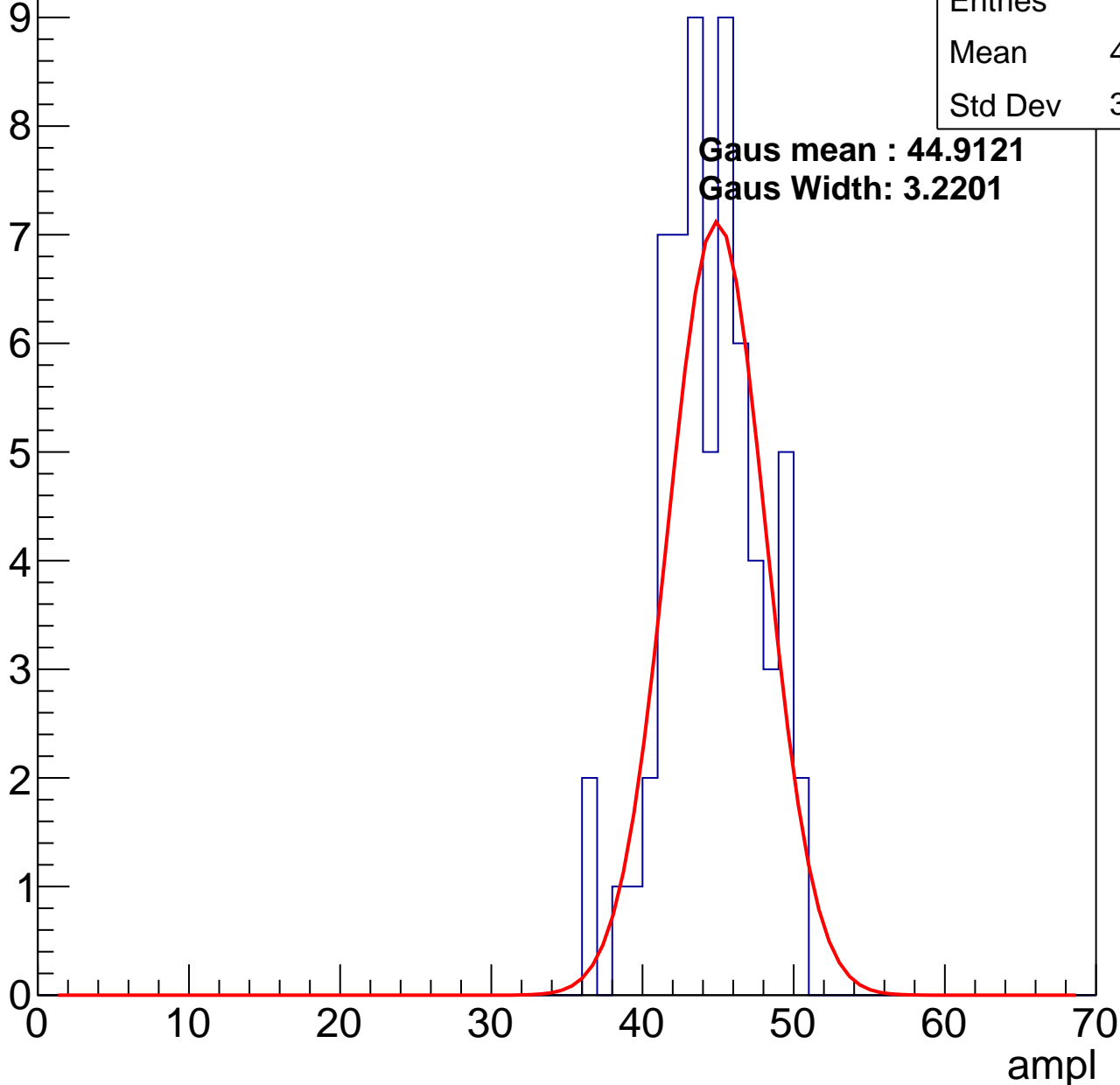
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 63    |
| Mean    | 44.05 |
| Std Dev | 3.174 |

**Gaus mean : 44.9121**

**Gaus Width: 3.2201**

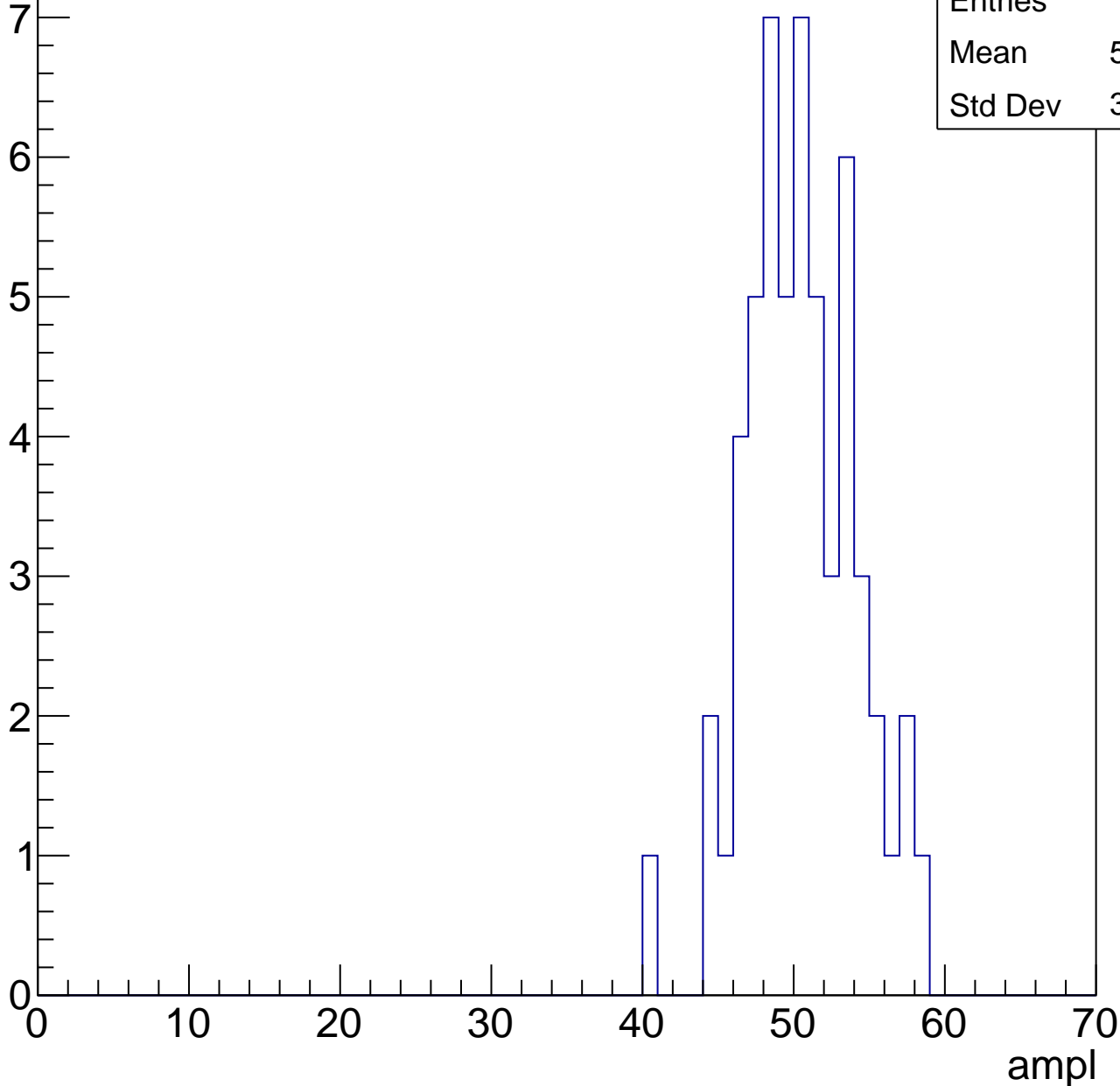


# B0L001S, U2-ch101, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 55    |
| Mean    | 50.04 |
| Std Dev | 3.583 |

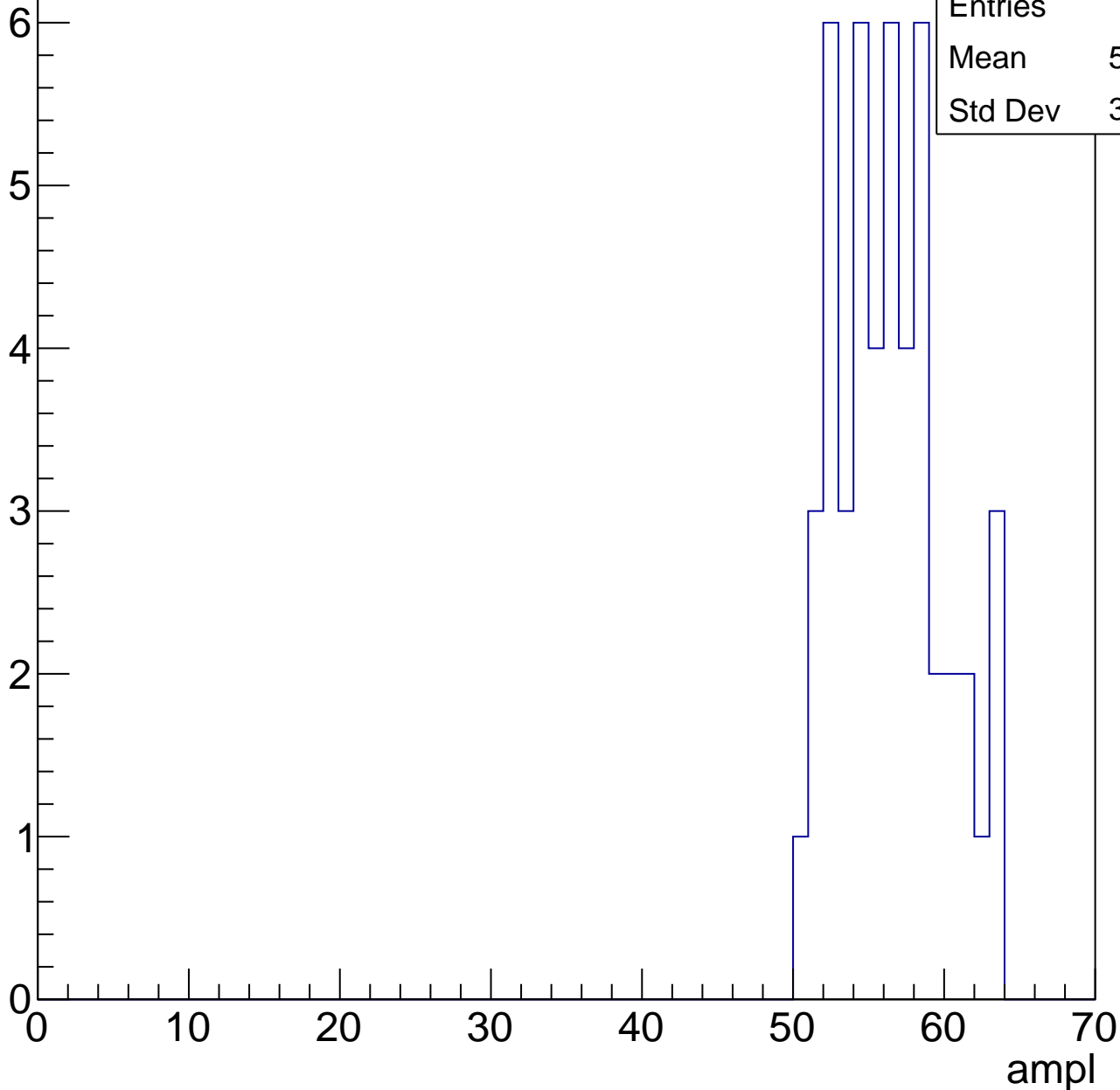


# B0L001S, U2-ch101, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

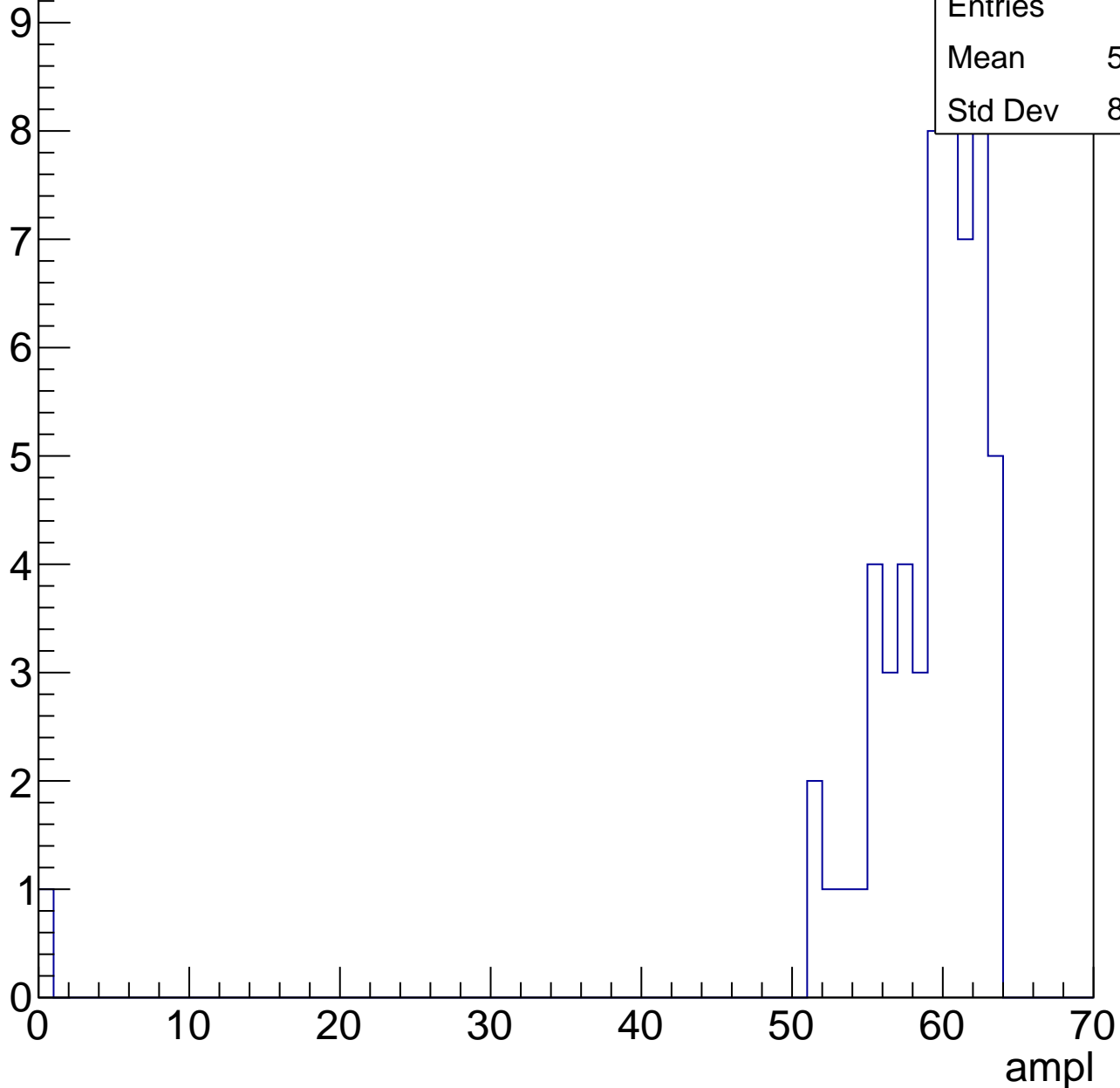
|         |       |
|---------|-------|
| Entries | 49    |
| Mean    | 55.94 |
| Std Dev | 3.419 |



# B0L001S, U2-ch101, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |       |
|---------|-------|
| Entries | 57    |
| Mean    | 57.95 |
| Std Dev | 8.338 |

# B0L001S, U2-ch101, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch101, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U2-ch102, adc0

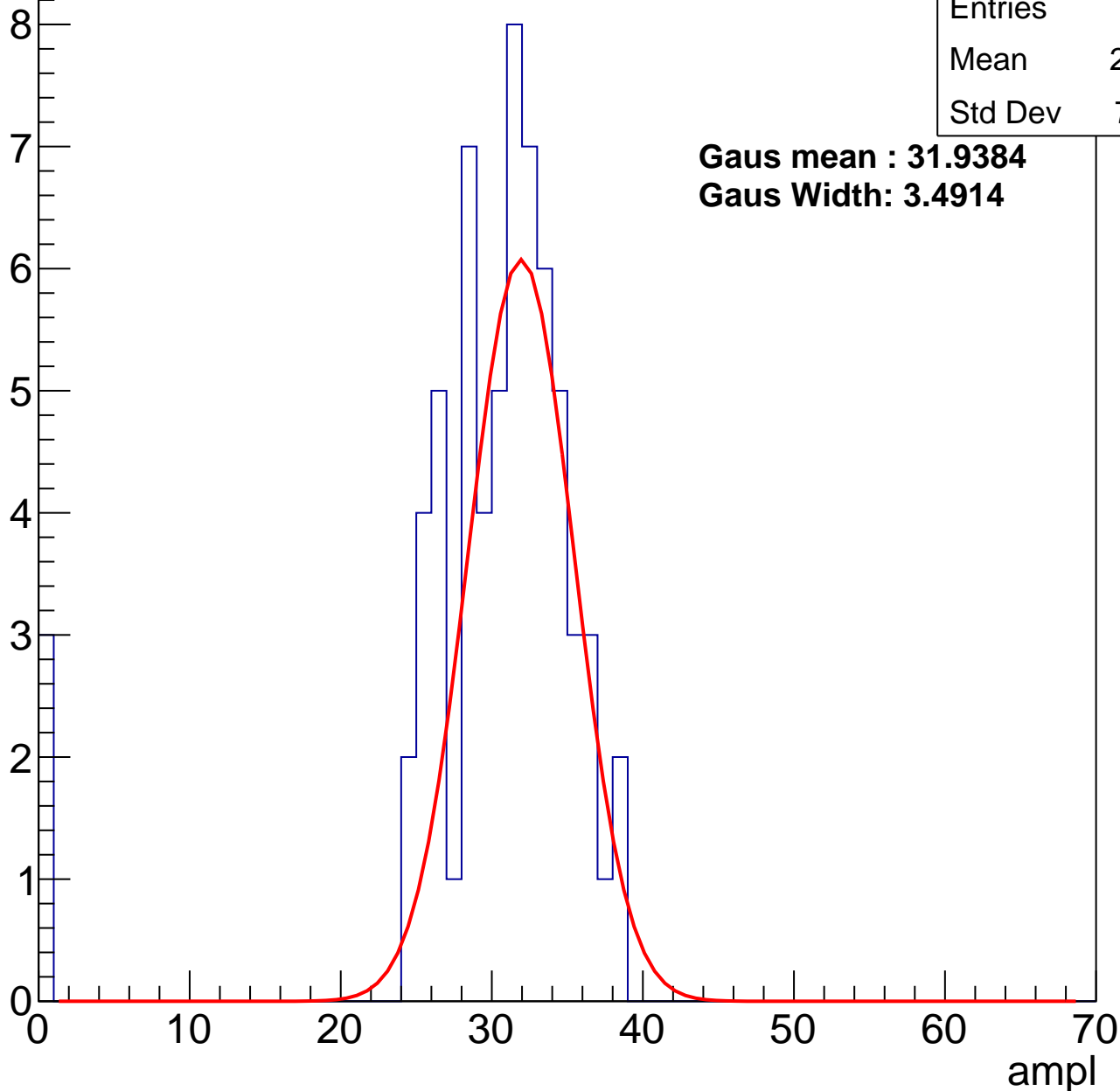
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 66    |
| Mean    | 29.29 |
| Std Dev | 7.271 |

**Gaus mean : 31.9384**

**Gaus Width: 3.4914**

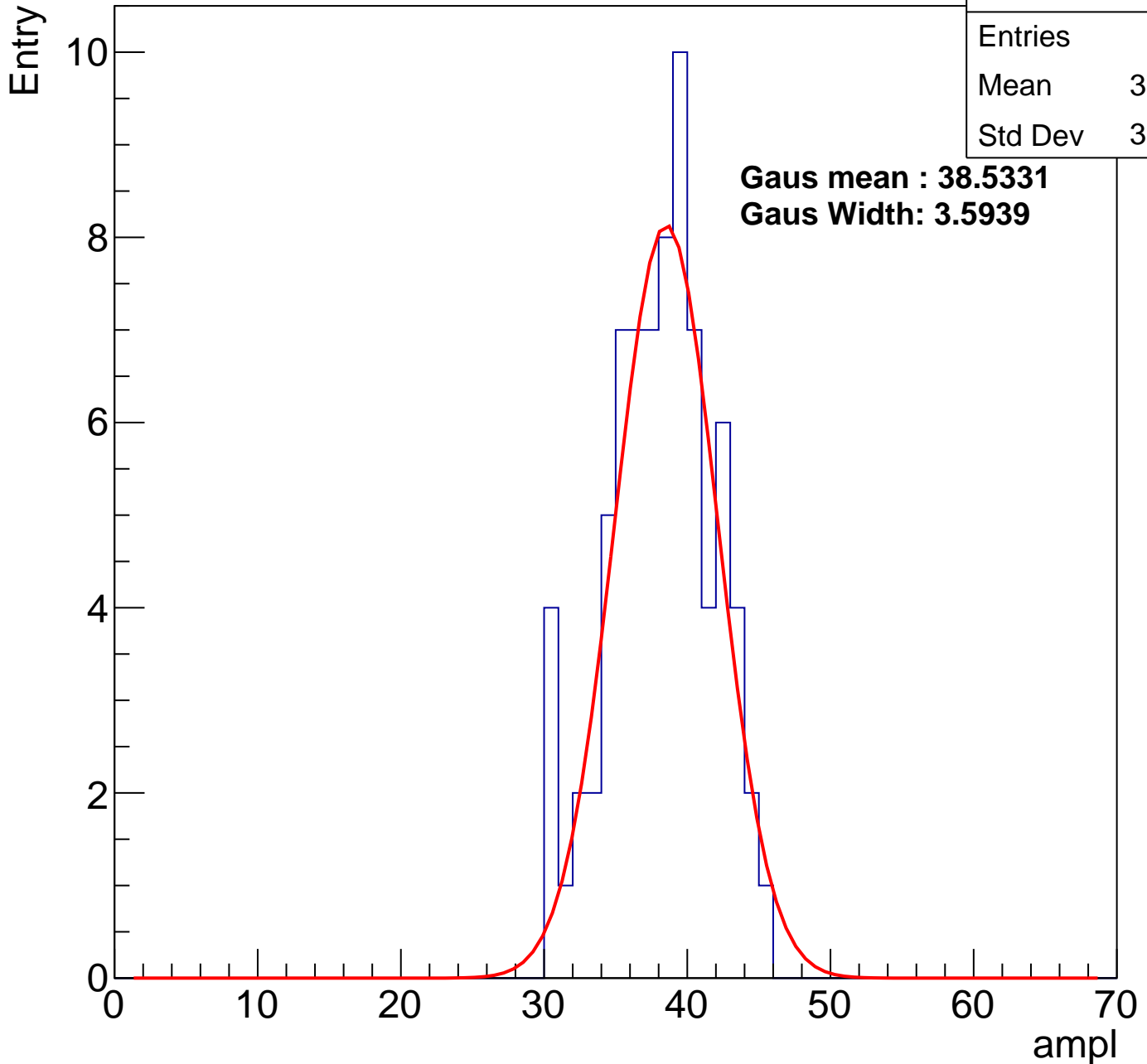


# B0L001S, U2-ch102, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 77    |
| Mean    | 37.69 |
| Std Dev | 3.583 |

**Gaus mean : 38.5331**  
**Gaus Width: 3.5939**



# B0L001S, U2-ch102, adc2

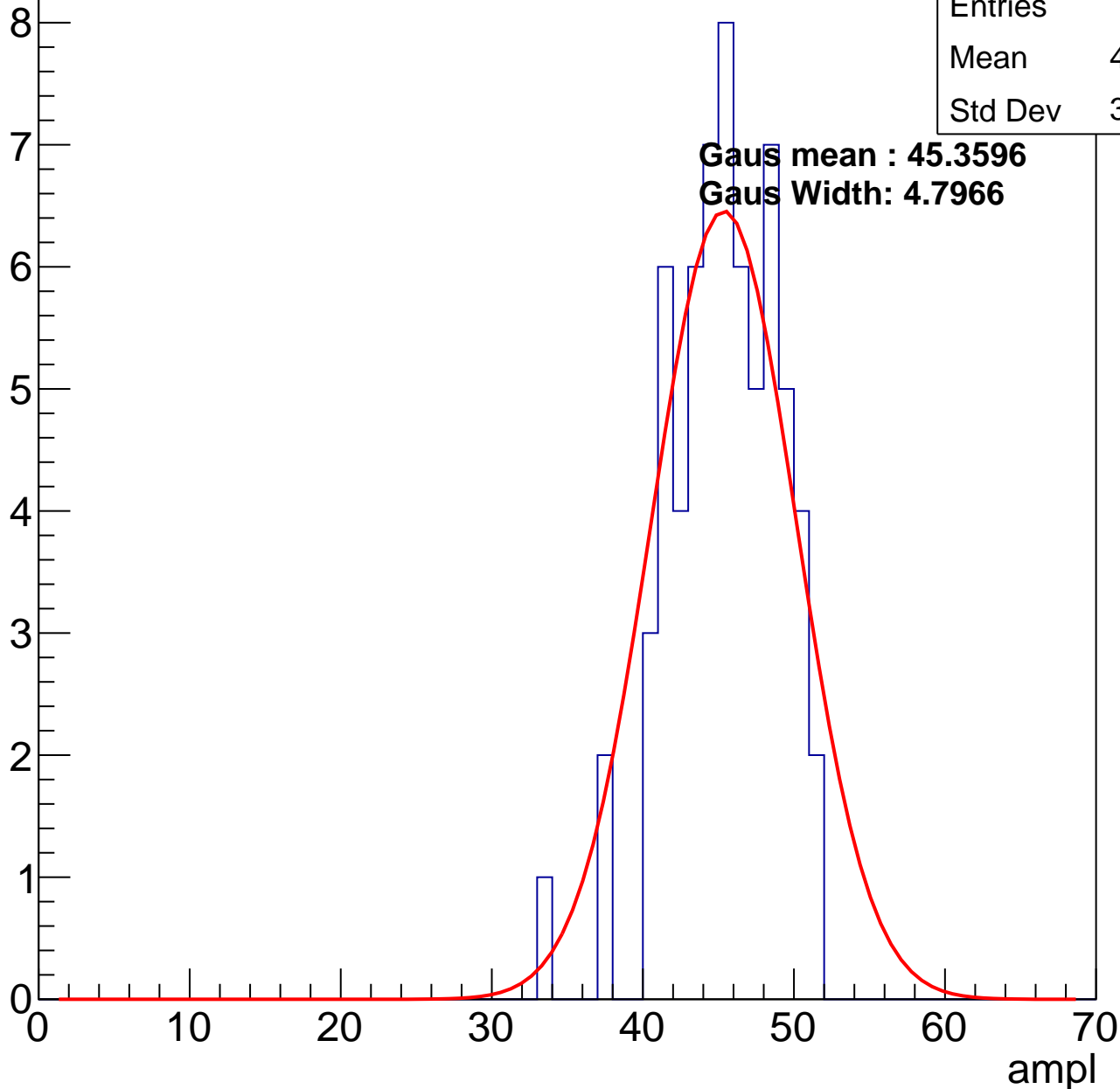
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 66    |
| Mean    | 44.86 |
| Std Dev | 3.588 |

Gaus mean : 45.3596

Gaus Width: 4.7966

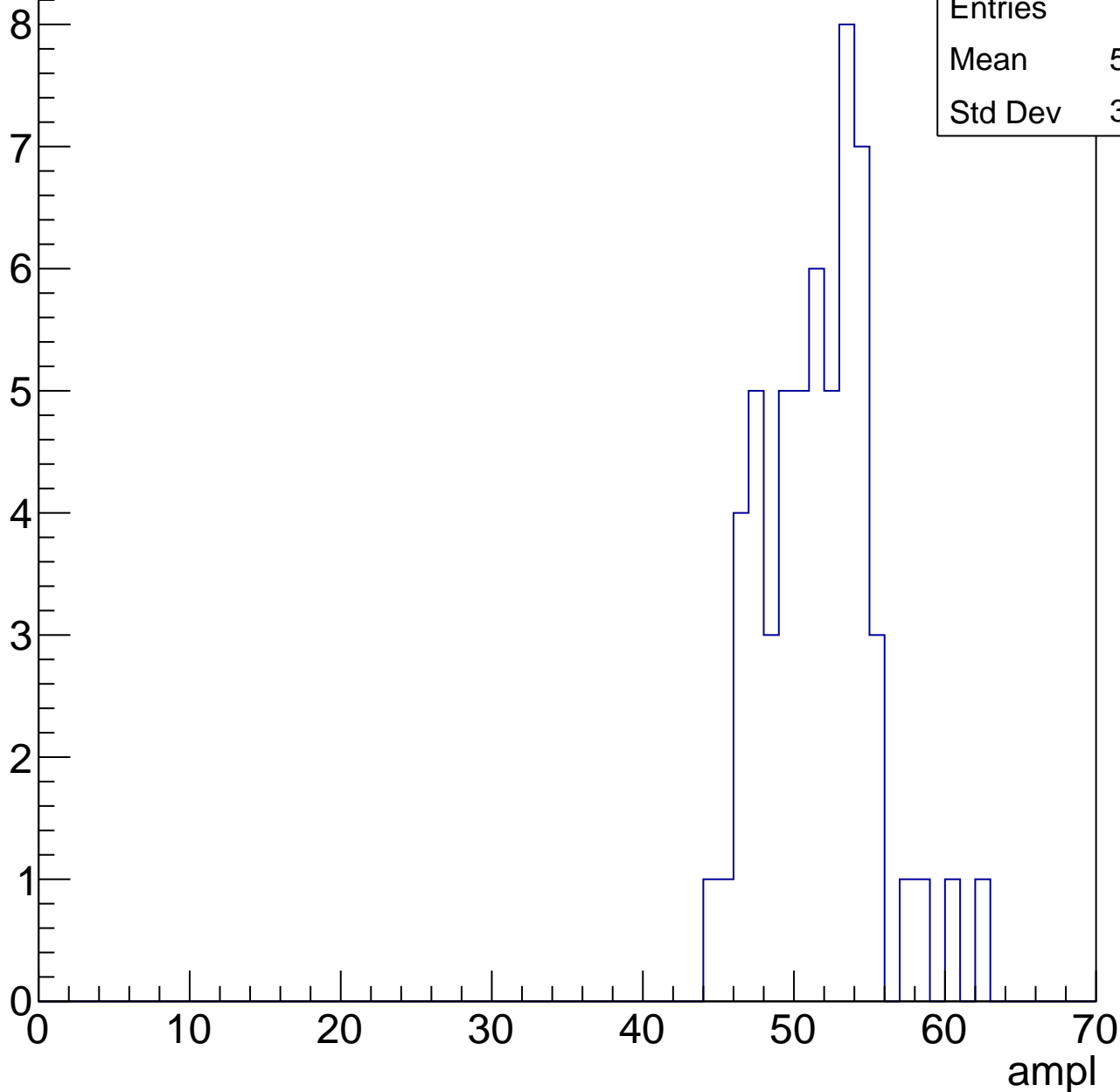


# B0L001S, U2-ch102, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

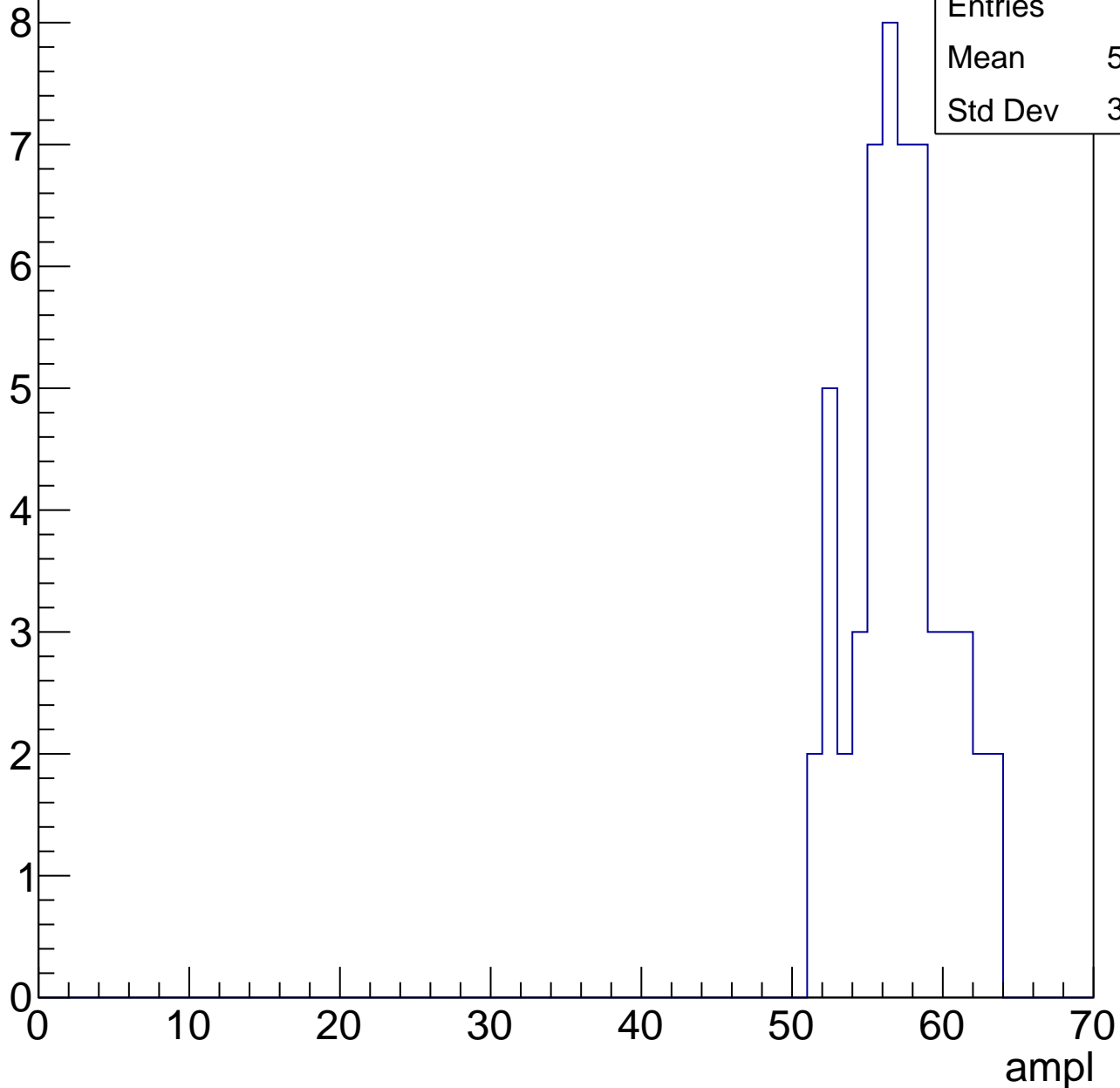
|         |       |
|---------|-------|
| Entries | 57    |
| Mean    | 51.18 |
| Std Dev | 3.628 |



# B0L001S, U2-ch102, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |       |
|---------|-------|
| Entries | 54    |
| Mean    | 56.63 |
| Std Dev | 3.045 |

# B0L001S, U2-ch102, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

7  
6  
5  
4  
3  
2  
1  
0

|         |       |
|---------|-------|
| Entries | 41    |
| Mean    | 58.63 |
| Std Dev | 9.599 |

ampl

0

10

20

30

40

50

60

70

# B0L001S, U2-ch102, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch102, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 0 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch103, adc0

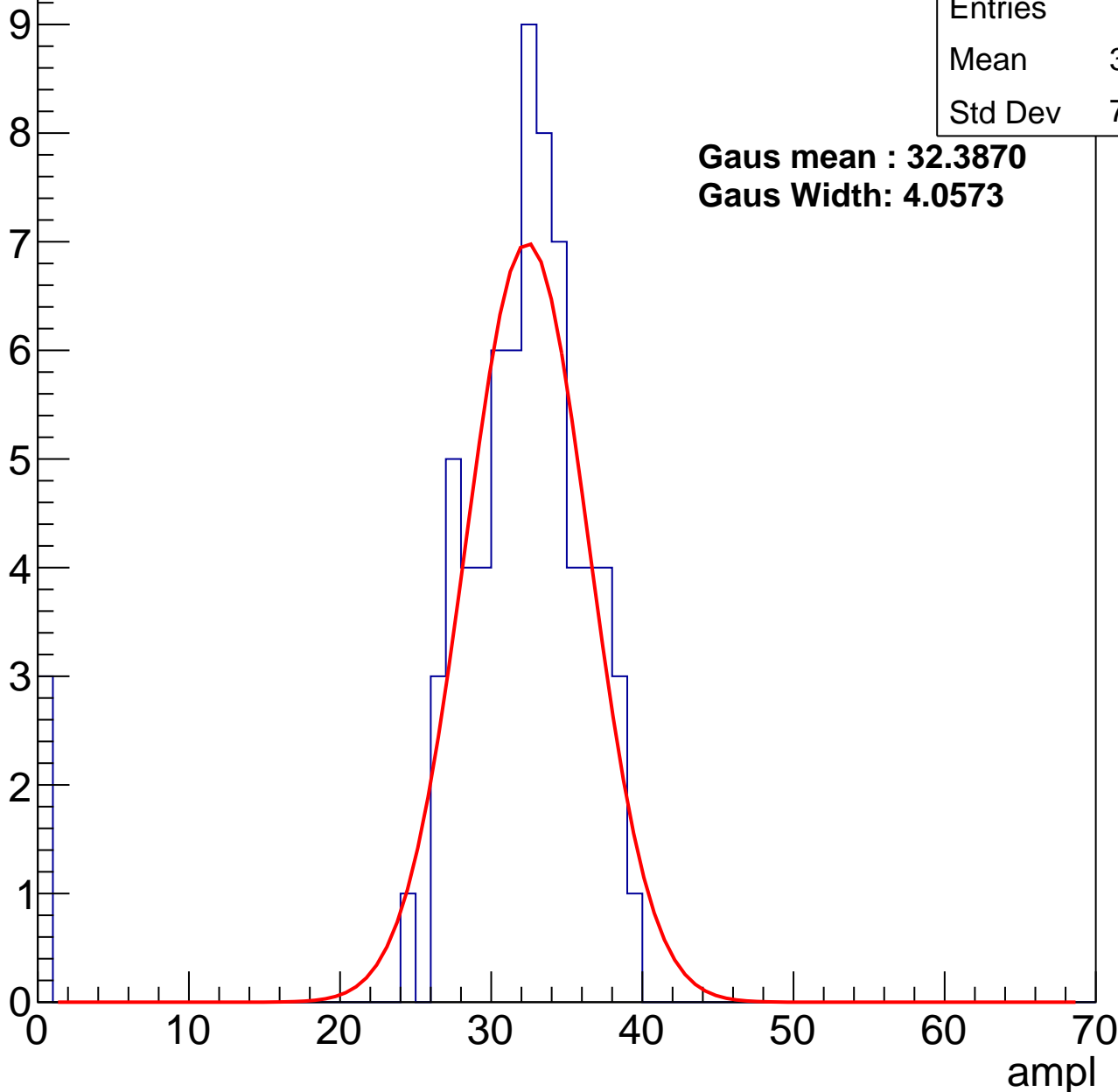
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 72    |
| Mean    | 30.64 |
| Std Dev | 7.225 |

**Gaus mean : 32.3870**

**Gaus Width: 4.0573**



# B0L001S, U2-ch103, adc1

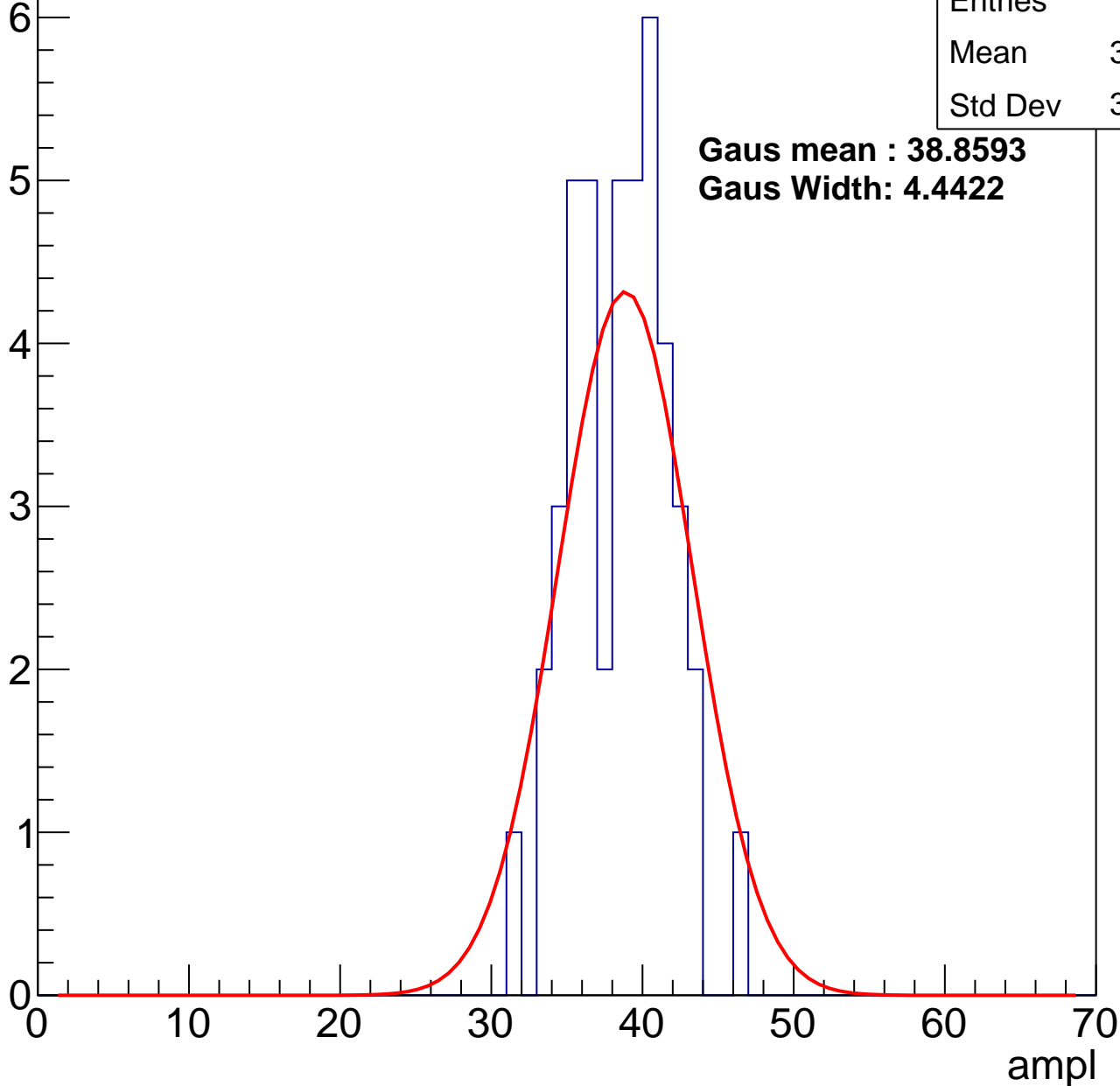
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 44    |
| Mean    | 38.07 |
| Std Dev | 3.165 |

**Gaus mean : 38.8593**

**Gaus Width: 4.4422**



# B0L001S, U2-ch103, adc2

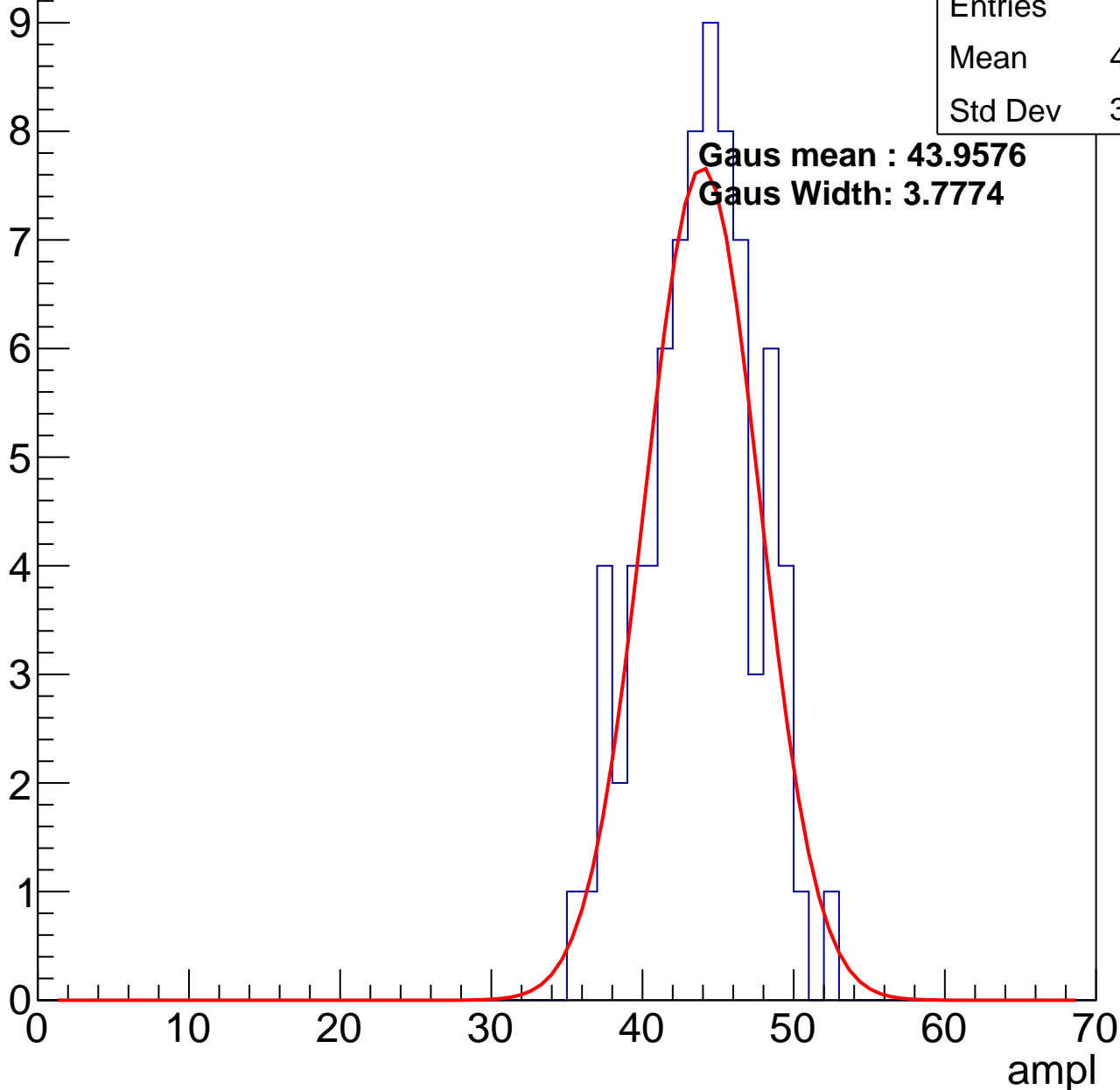
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 76    |
| Mean    | 43.42 |
| Std Dev | 3.628 |

**Gaus mean : 43.9576**

**Gaus Width: 3.7774**

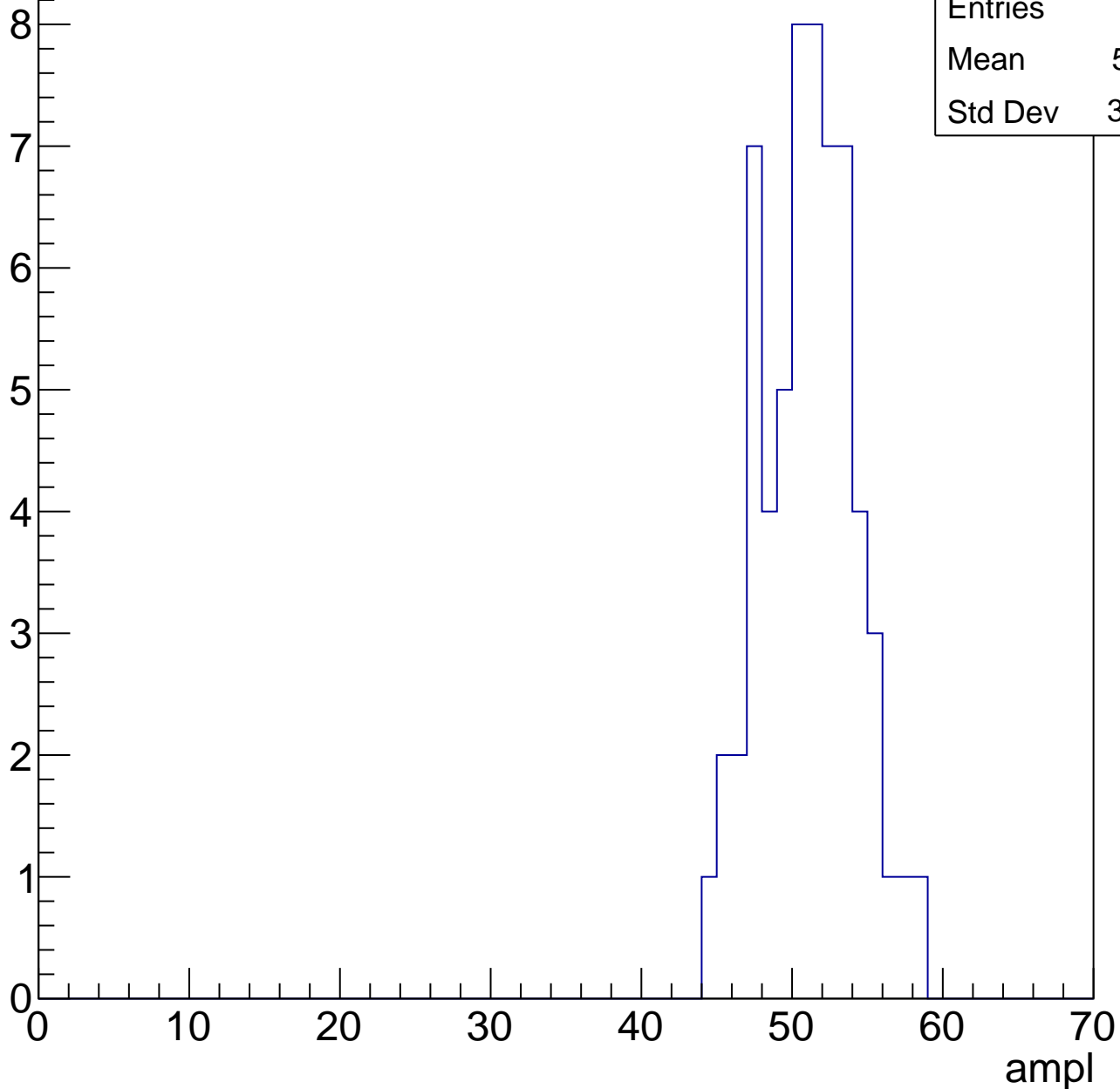


# B0L001S, U2-ch103, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 61    |
| Mean    | 50.61 |
| Std Dev | 3.048 |

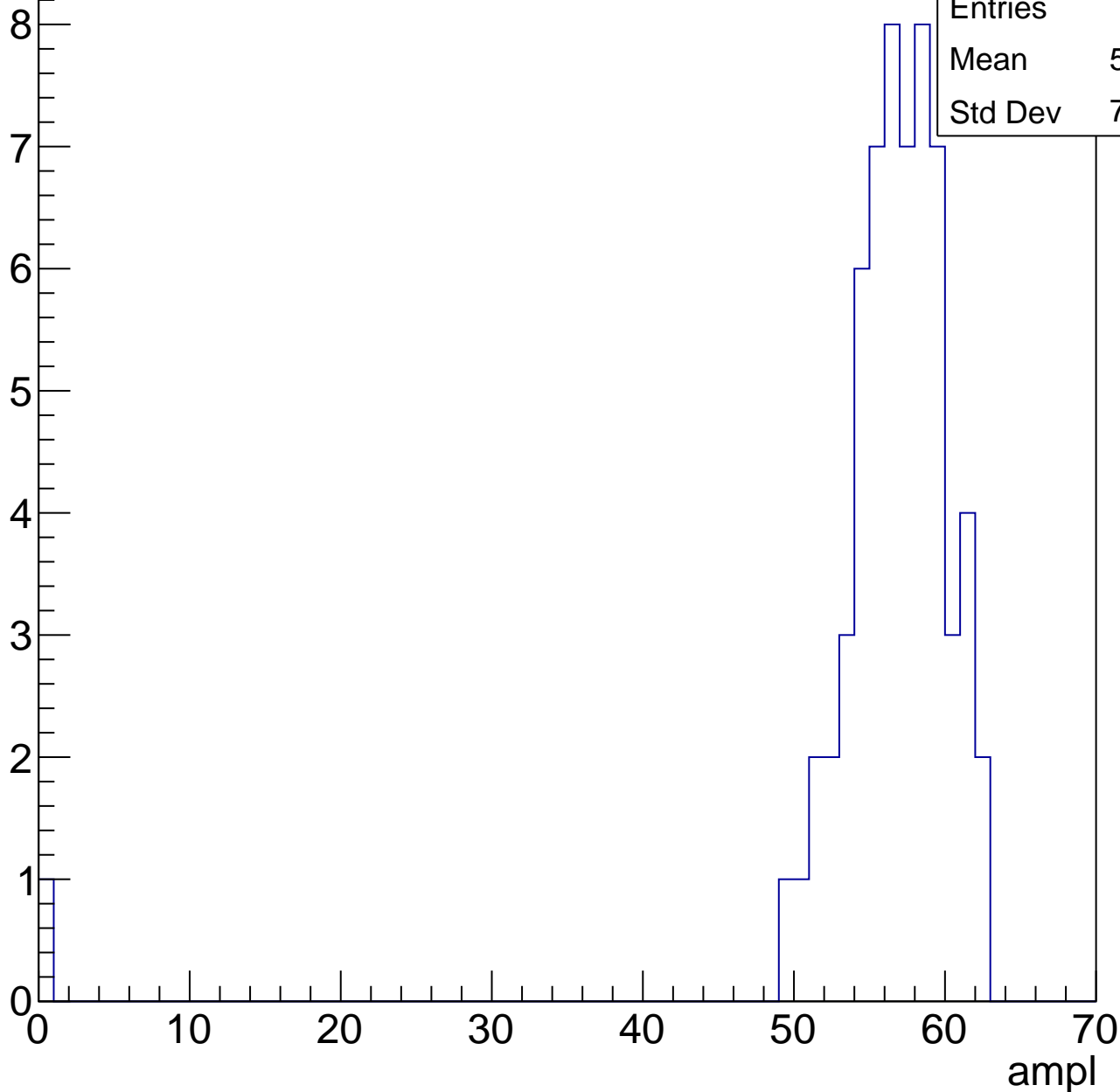


# B0L001S, U2-ch103, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

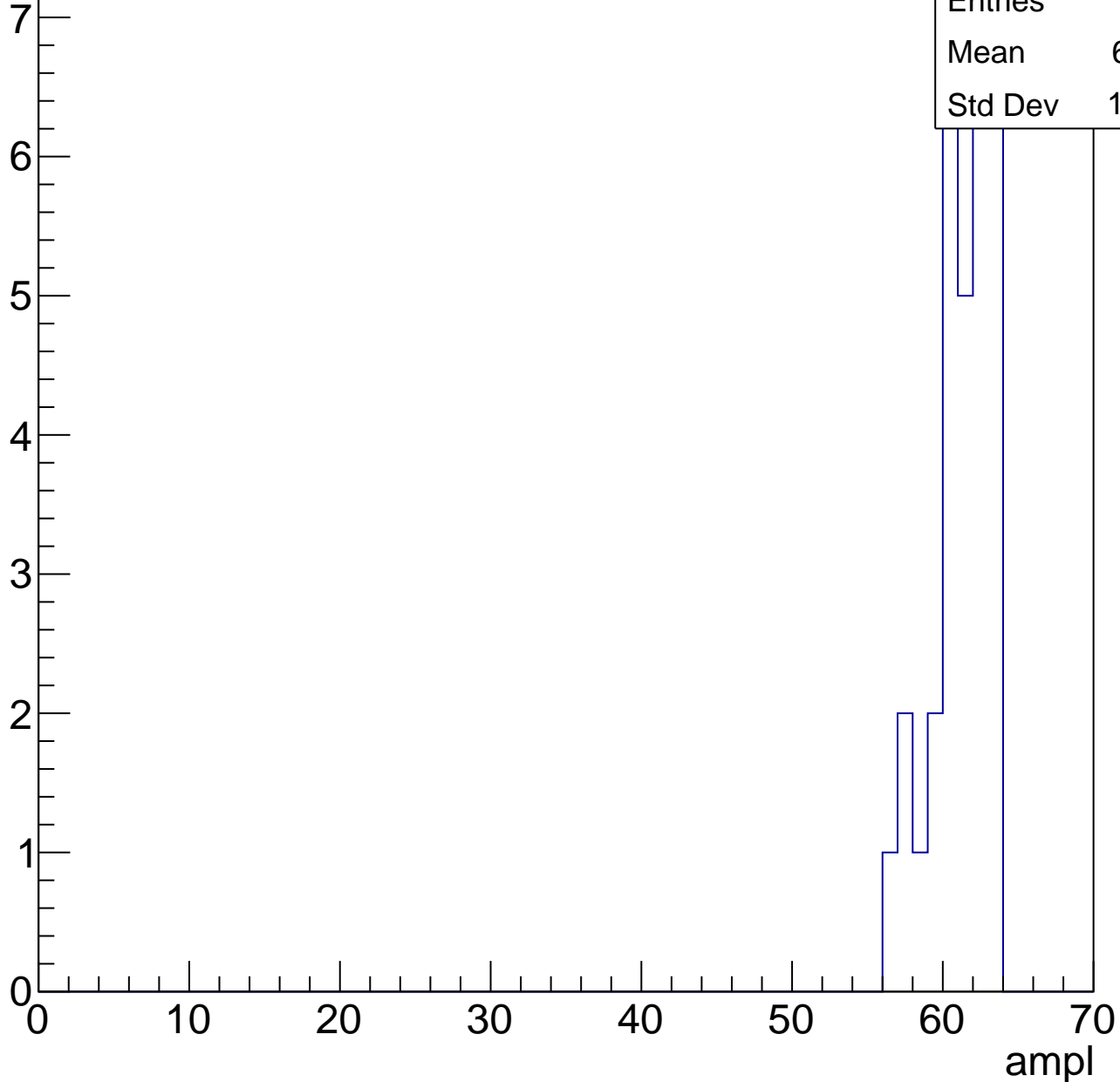
|         |       |
|---------|-------|
| Entries | 62    |
| Mean    | 55.56 |
| Std Dev | 7.695 |



# B0L001S, U2-ch103, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

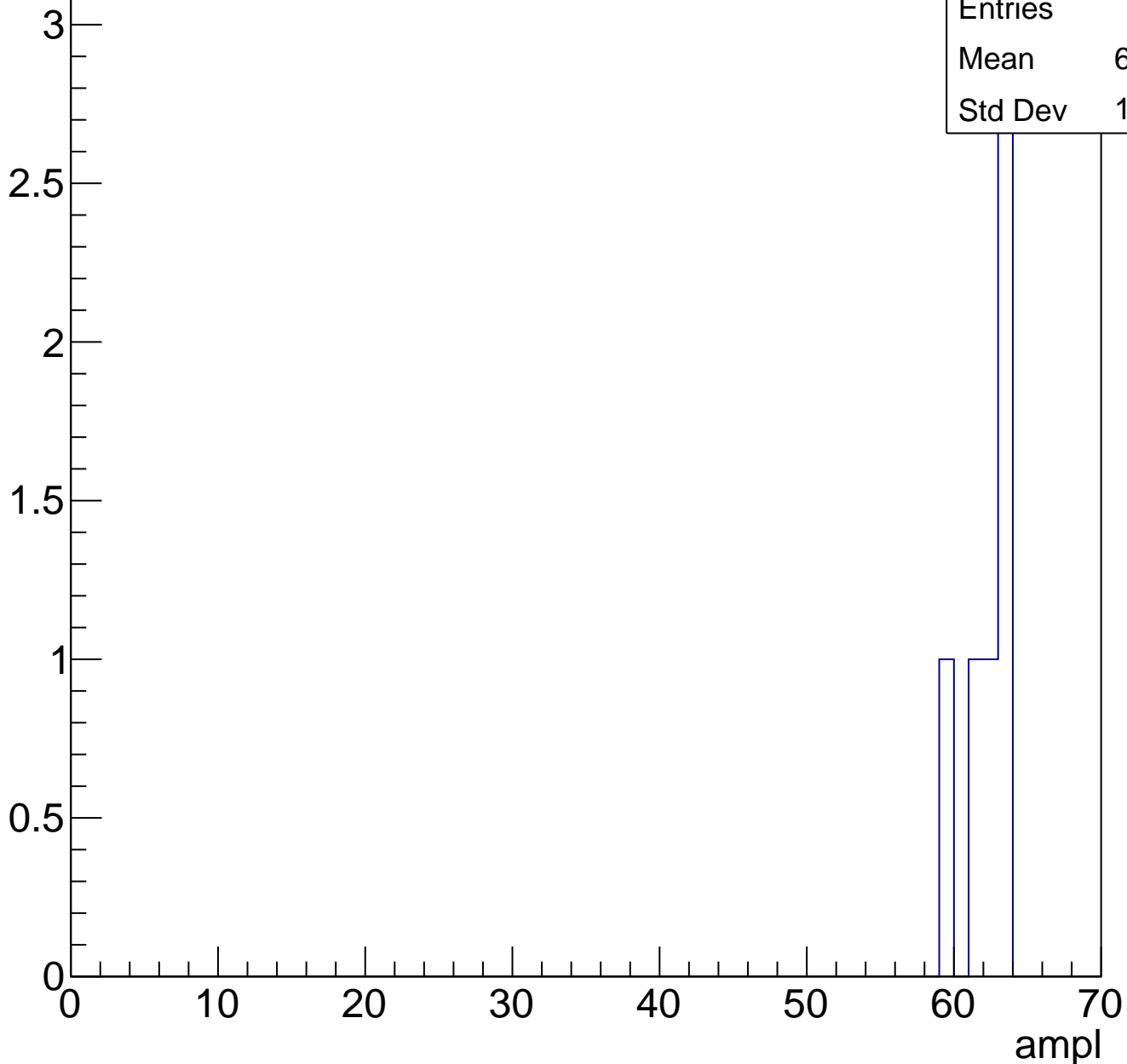
Entry



# B0L001S, U2-ch103, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |       |
|---------|-------|
| Entries | 6     |
| Mean    | 61.83 |
| Std Dev | 1.462 |



# B0L001S, U2-ch103, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 1 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch104, adc0

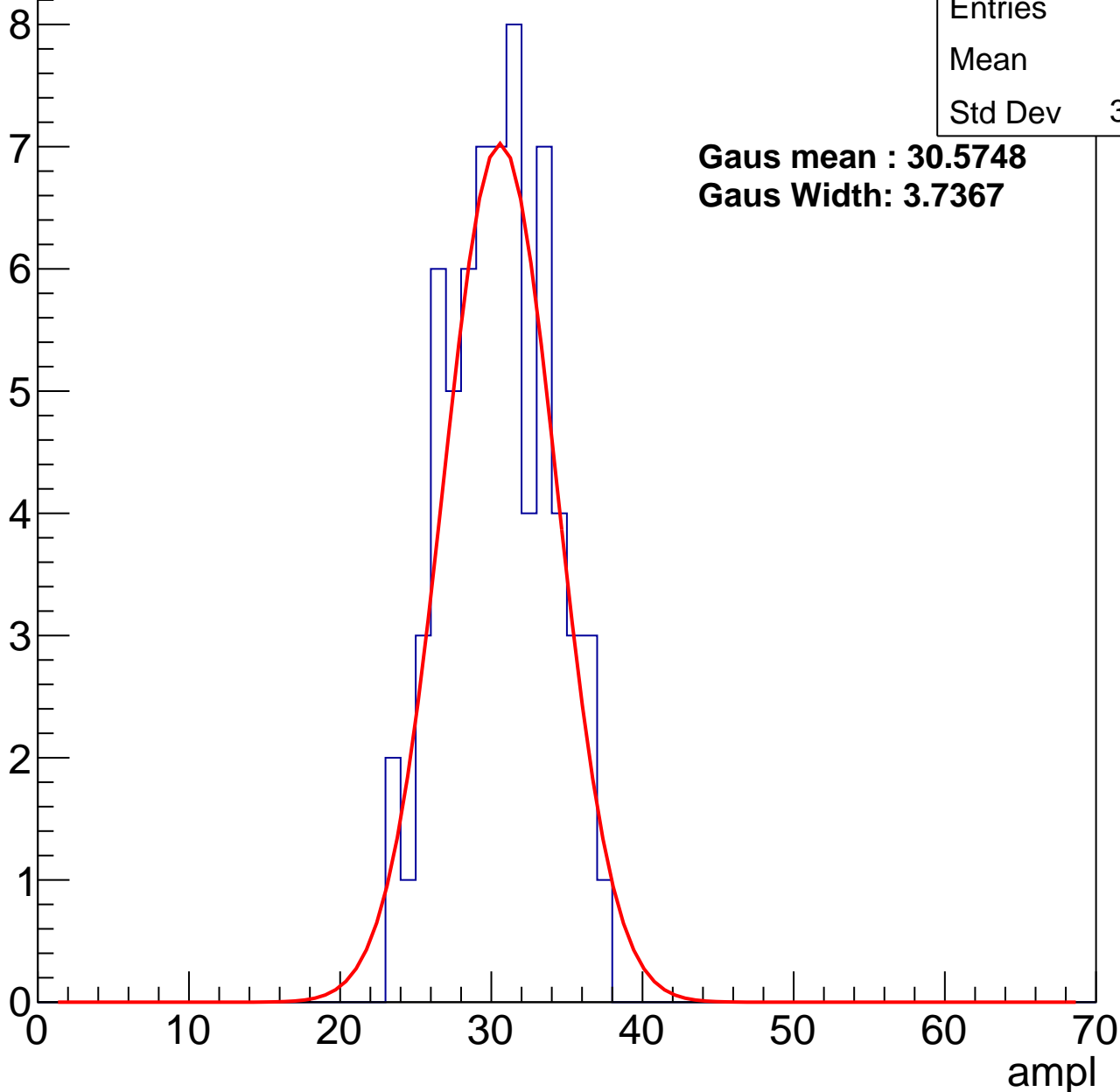
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 67    |
| Mean    | 30    |
| Std Dev | 3.377 |

**Gaus mean : 30.5748**

**Gaus Width: 3.7367**



# B0L001S, U2-ch104, adc1

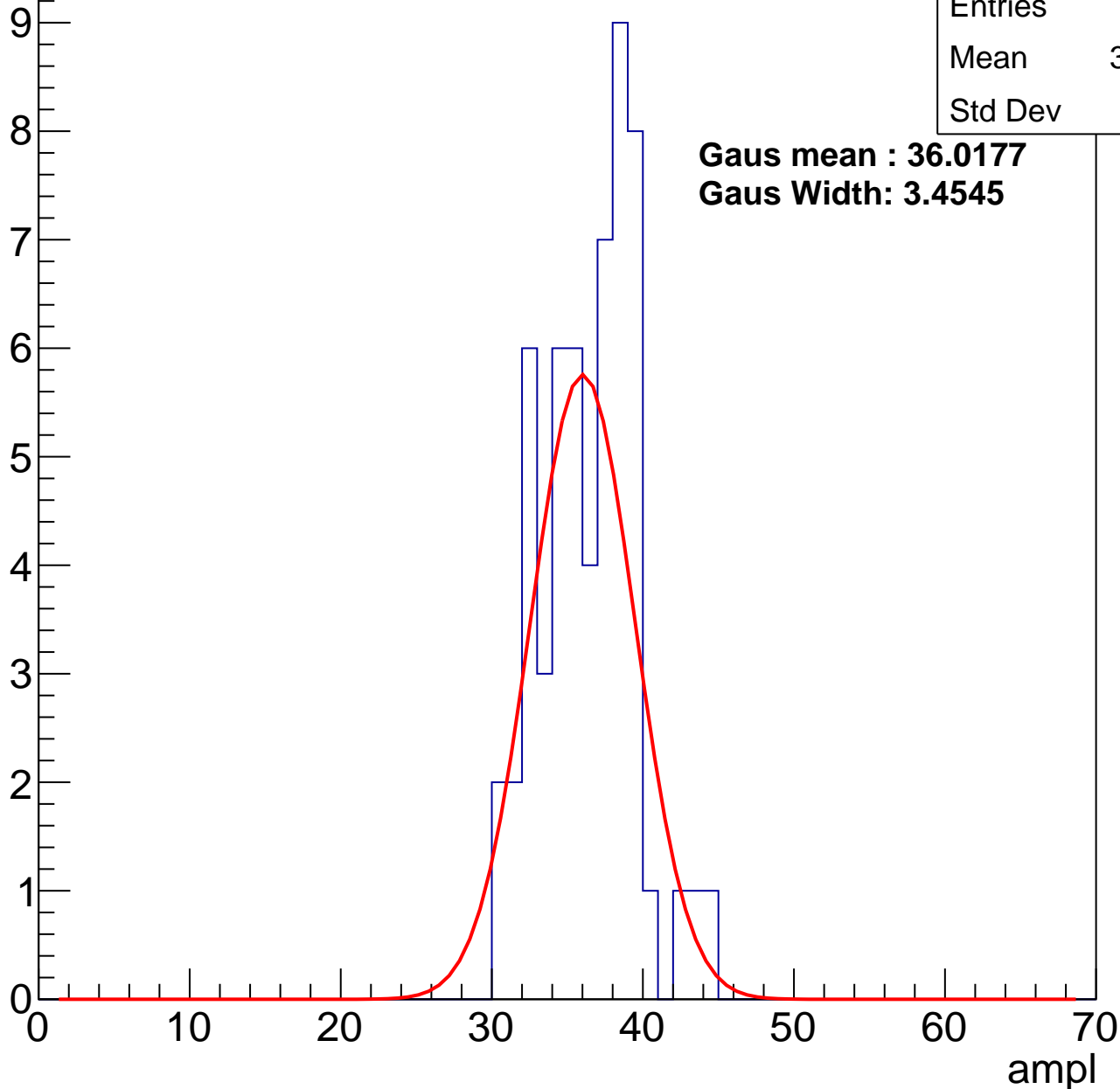
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 57    |
| Mean    | 36.02 |
| Std Dev | 3.12  |

**Gaus mean : 36.0177**

**Gaus Width: 3.4545**



# B0L001S, U2-ch104, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 60    |
| Mean    | 42.1  |
| Std Dev | 3.234 |

**Gaus mean : 43.0597**

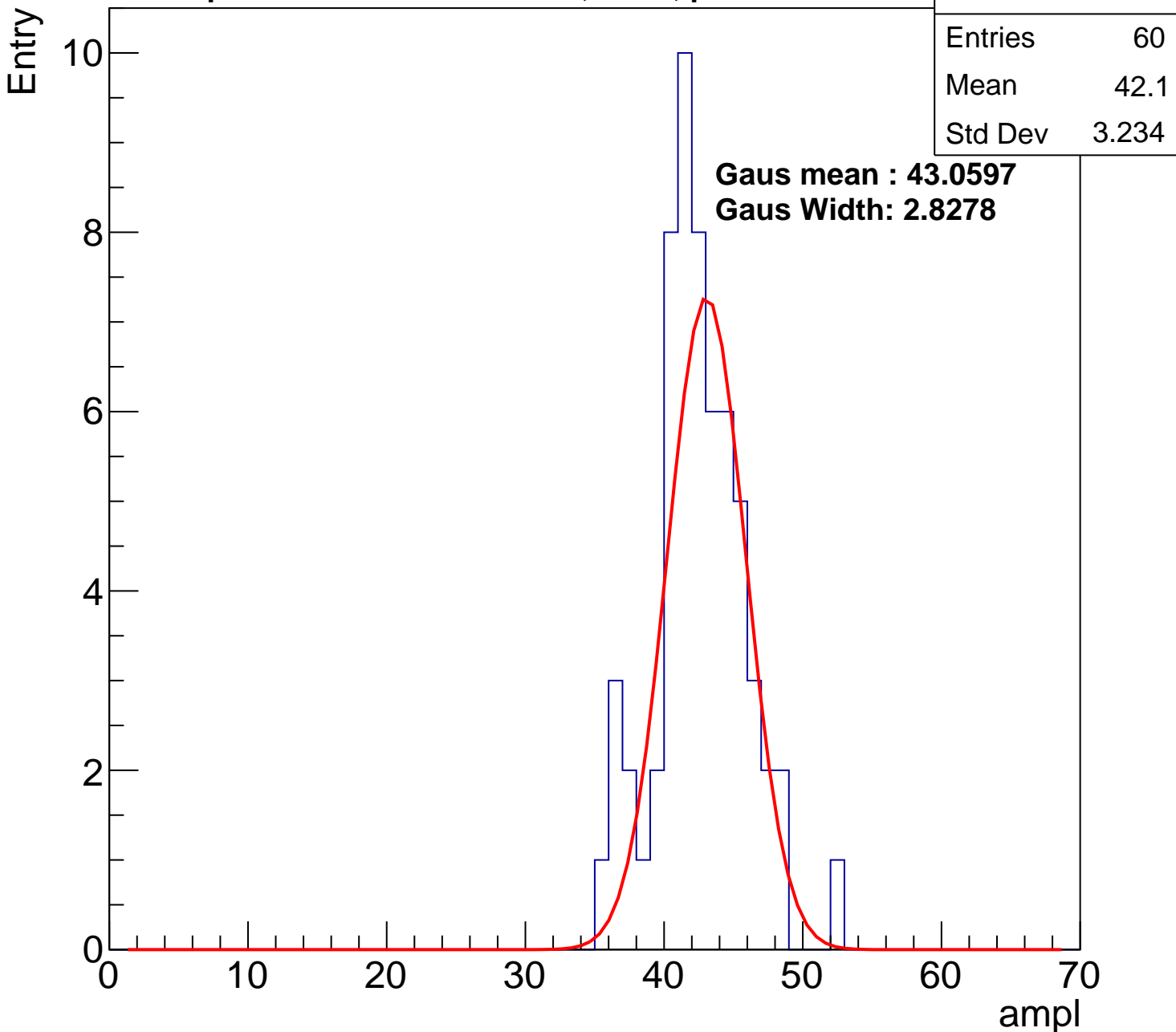
**Gaus Width: 2.8278**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

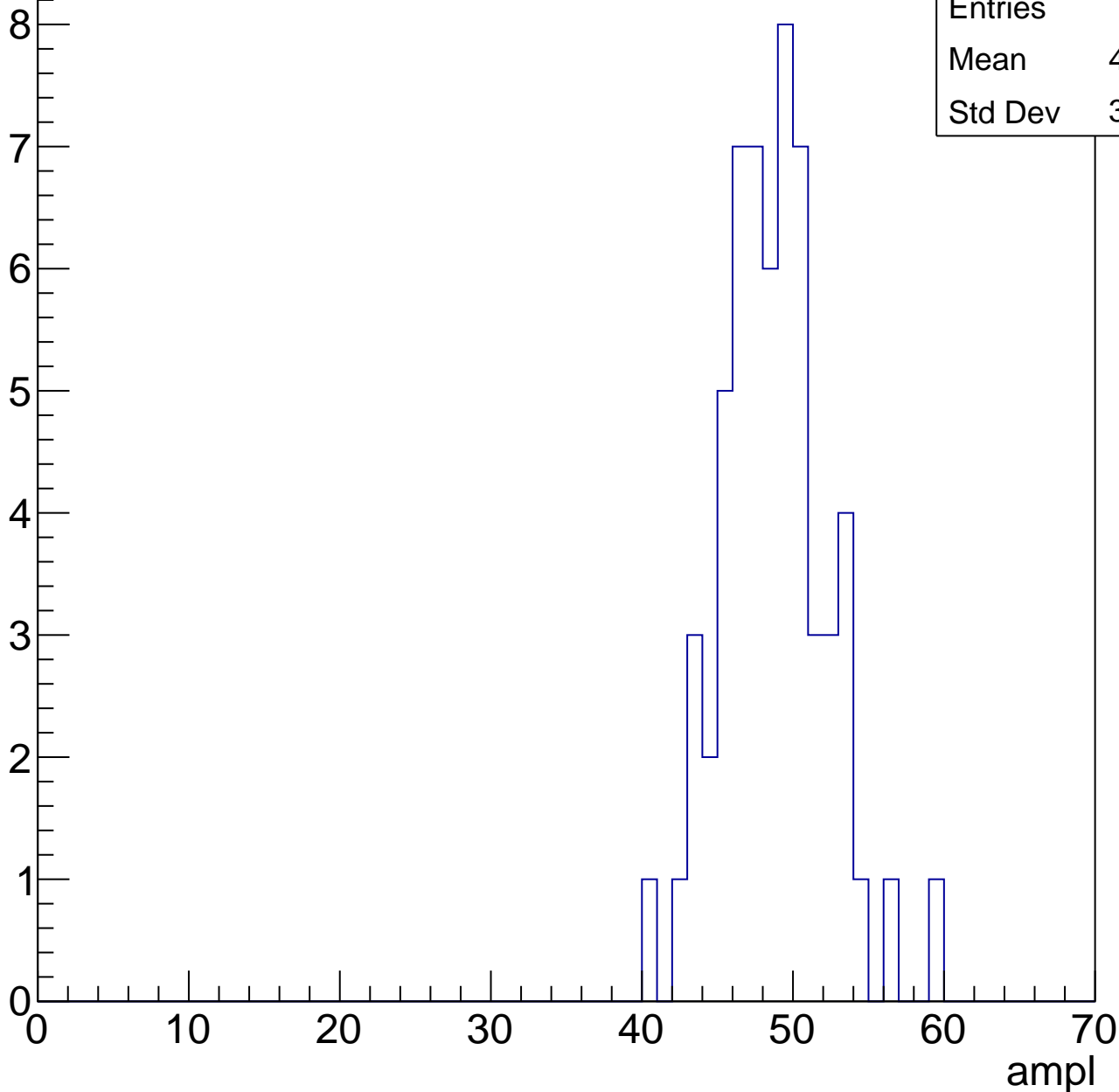


# B0L001S, U2-ch104, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 60    |
| Mean    | 48.25 |
| Std Dev | 3.453 |

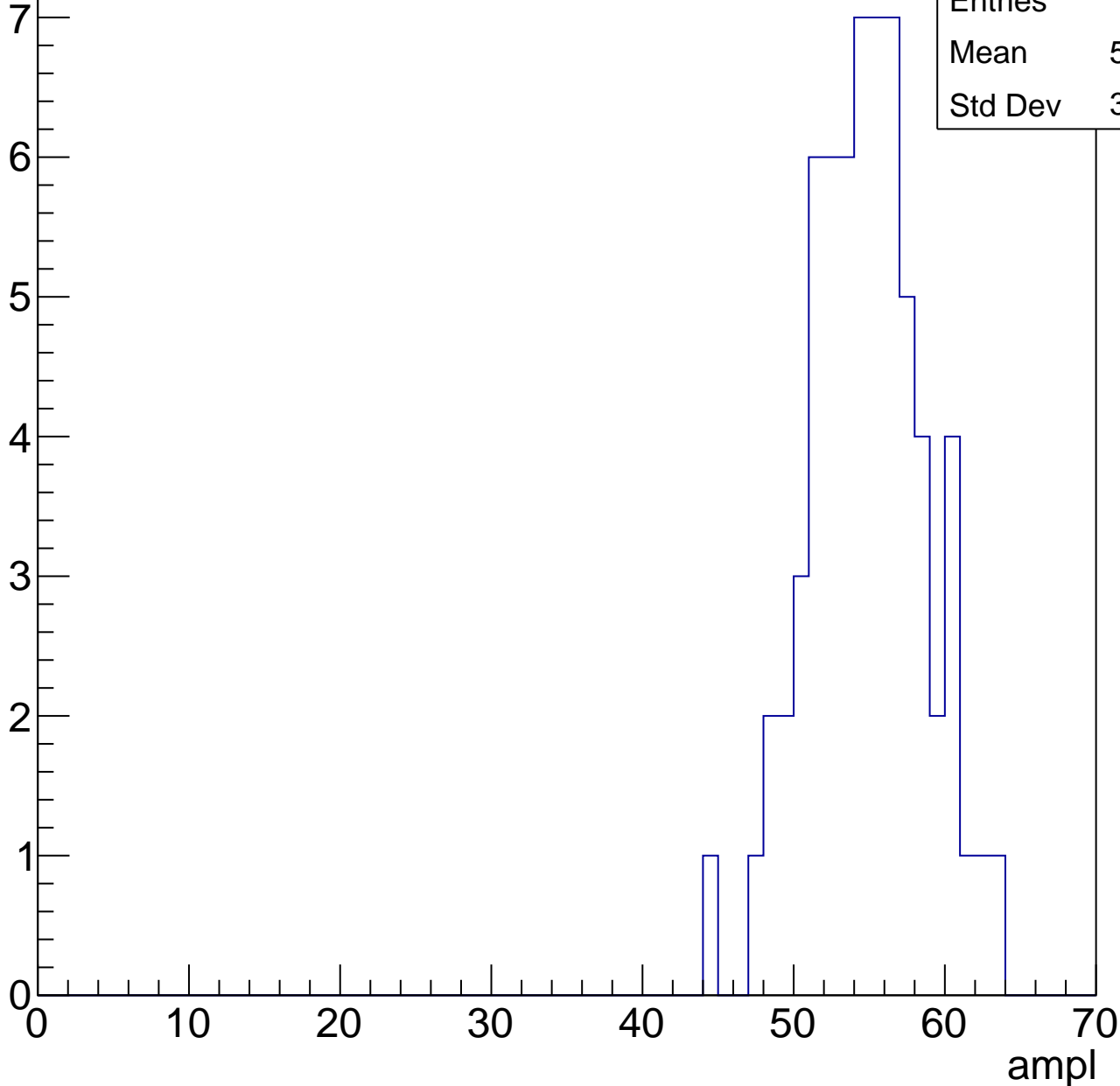


# B0L001S, U2-ch104, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 66    |
| Mean    | 54.35 |
| Std Dev | 3.748 |

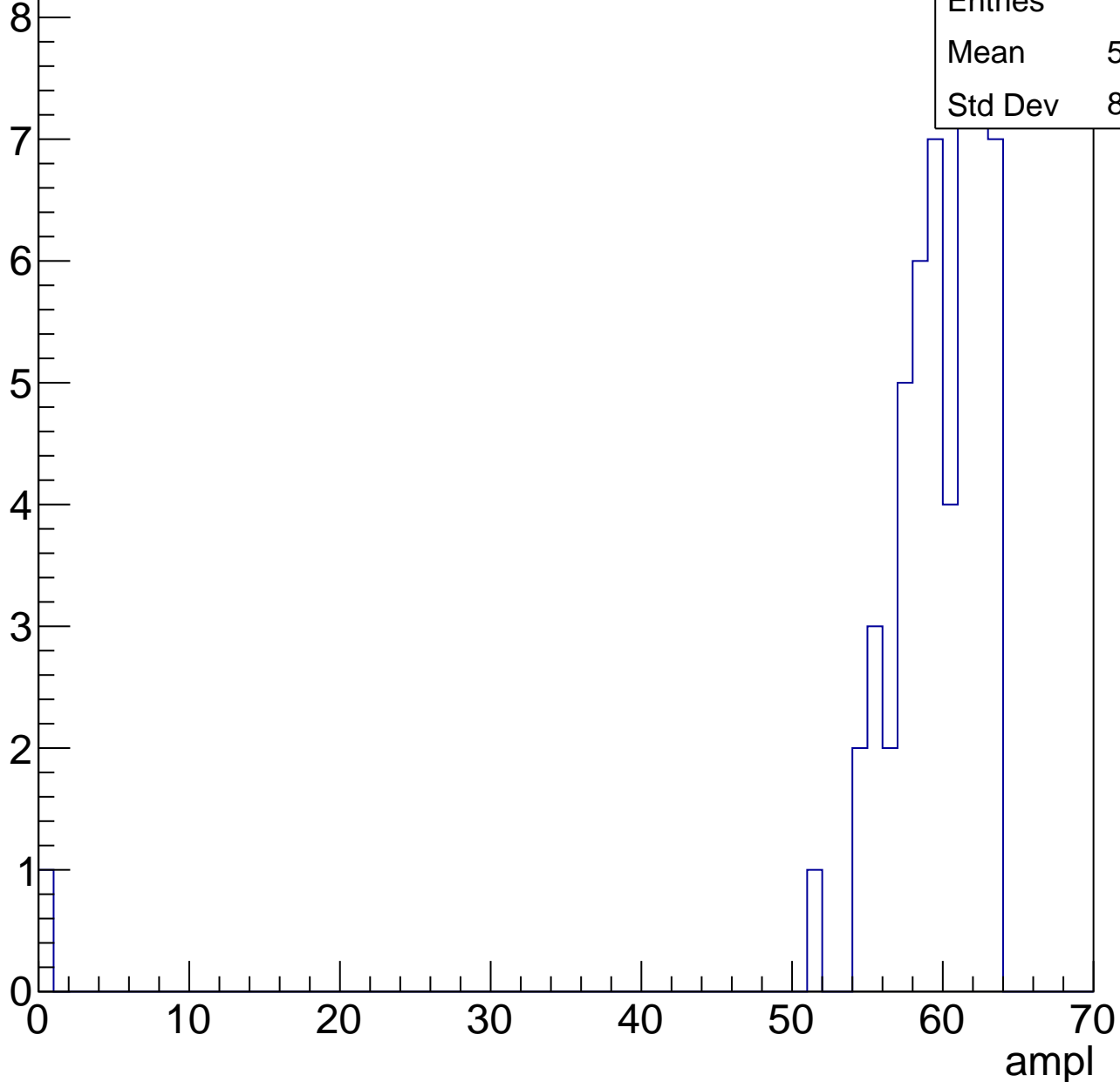


# B0L001S, U2-ch104, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 54    |
| Mean    | 58.28 |
| Std Dev | 8.475 |



# B0L001S, U2-ch104, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

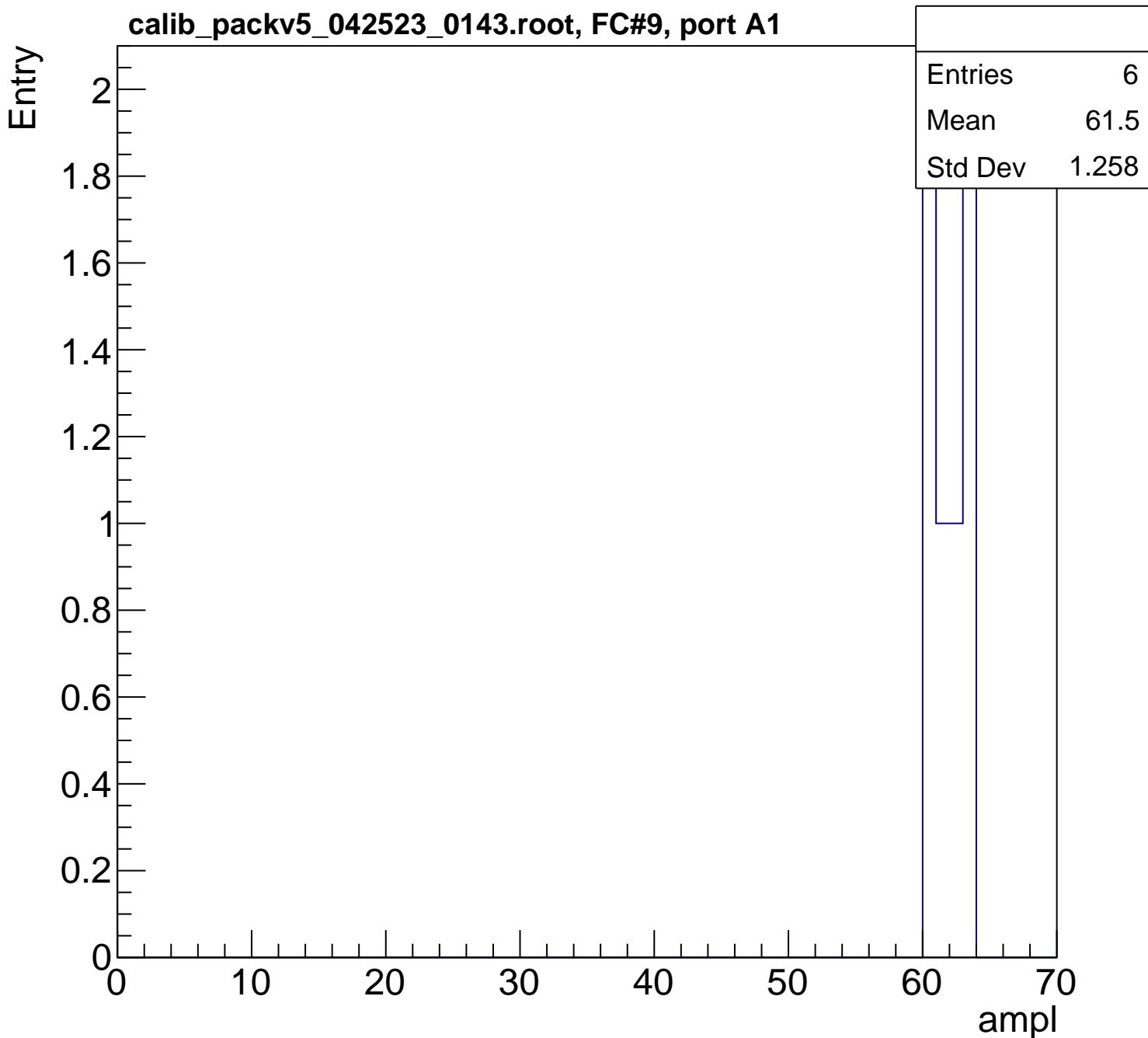
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

|         |       |
|---------|-------|
| Entries | 6     |
| Mean    | 61.5  |
| Std Dev | 1.258 |

0 10 20 30 40 50 60 70

ampl





# B0L001S, U2-ch104, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |     |
|---------|-----|
| Entries | 2   |
| Mean    | 9.5 |
| Std Dev | 9.5 |

# B0L001S, U2-ch105, adc0

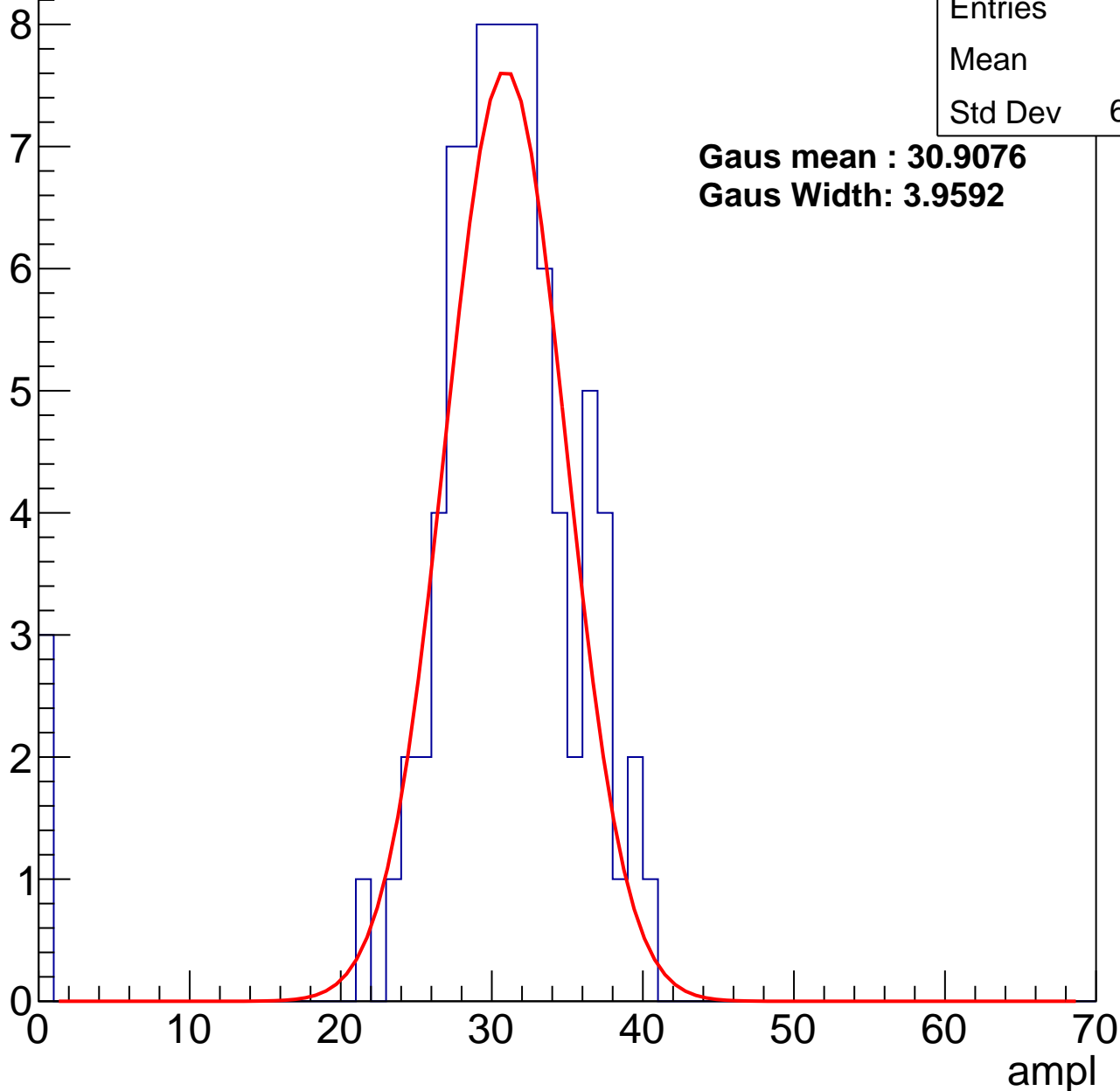
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 84    |
| Mean    | 29.7  |
| Std Dev | 6.916 |

**Gaus mean : 30.9076**

**Gaus Width: 3.9592**



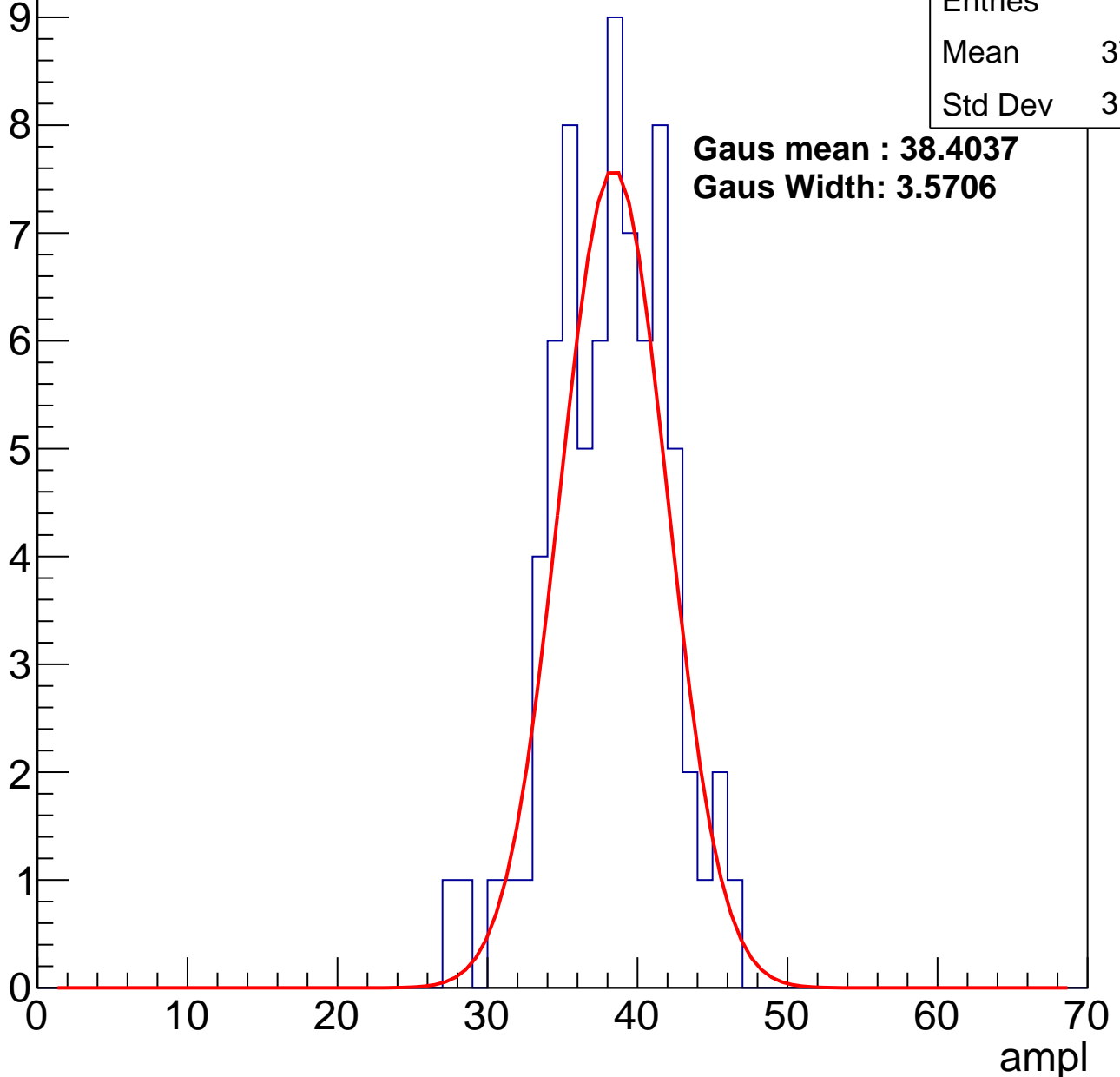
# B0L001S, U2-ch105, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 75    |
| Mean    | 37.67 |
| Std Dev | 3.806 |

**Gaus mean : 38.4037**  
**Gaus Width: 3.5706**



# B0L001S, U2-ch105, adc2

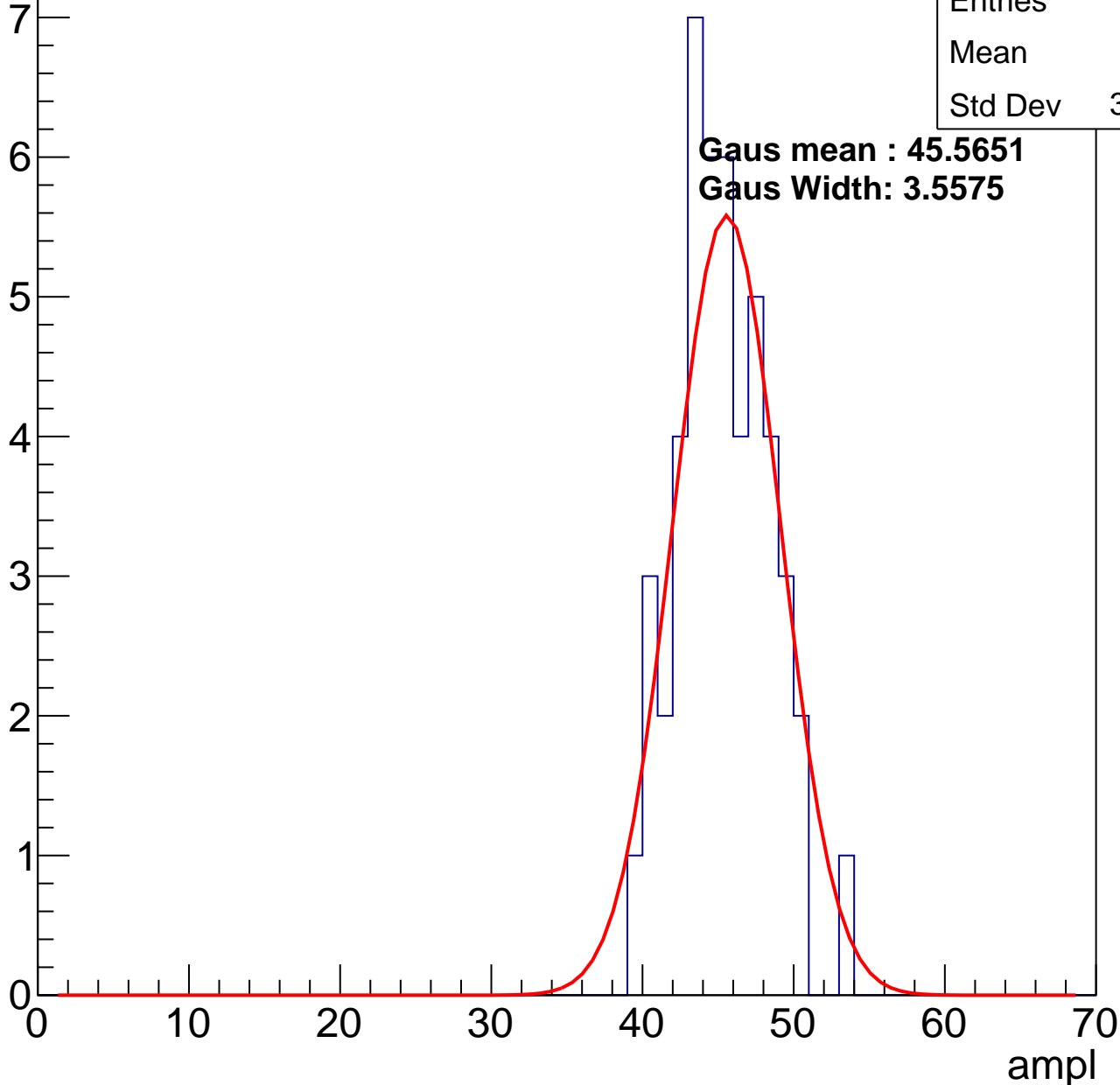
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 48    |
| Mean    | 44.9  |
| Std Dev | 3.009 |

**Gaus mean : 45.5651**

**Gaus Width: 3.5575**



# B0L001S, U2-ch105, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 79    |
| Mean    | 50.87 |
| Std Dev | 3.924 |

Entry

10

8

6

4

2

0

0

10

20

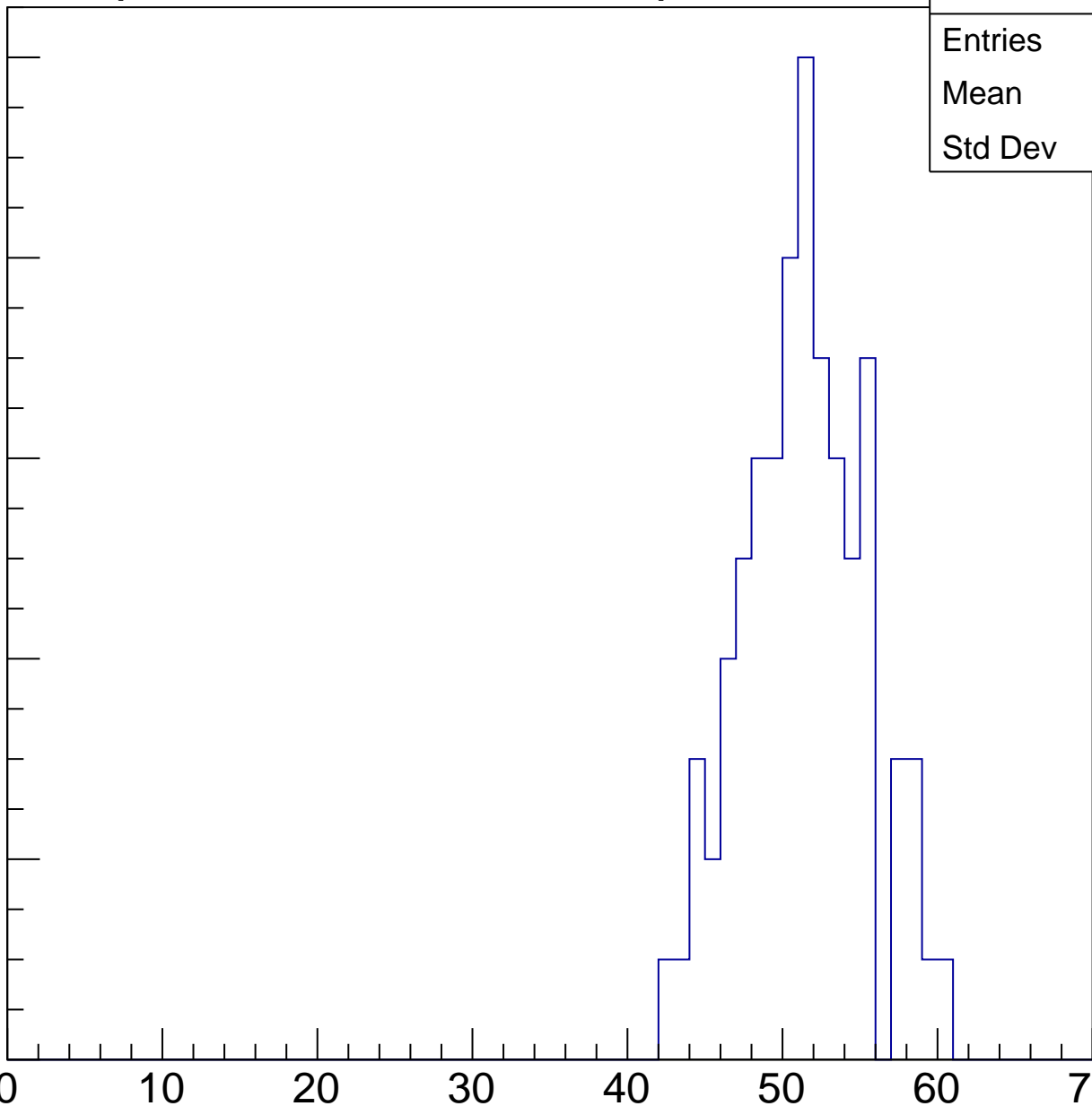
30

40

50

60

ampl

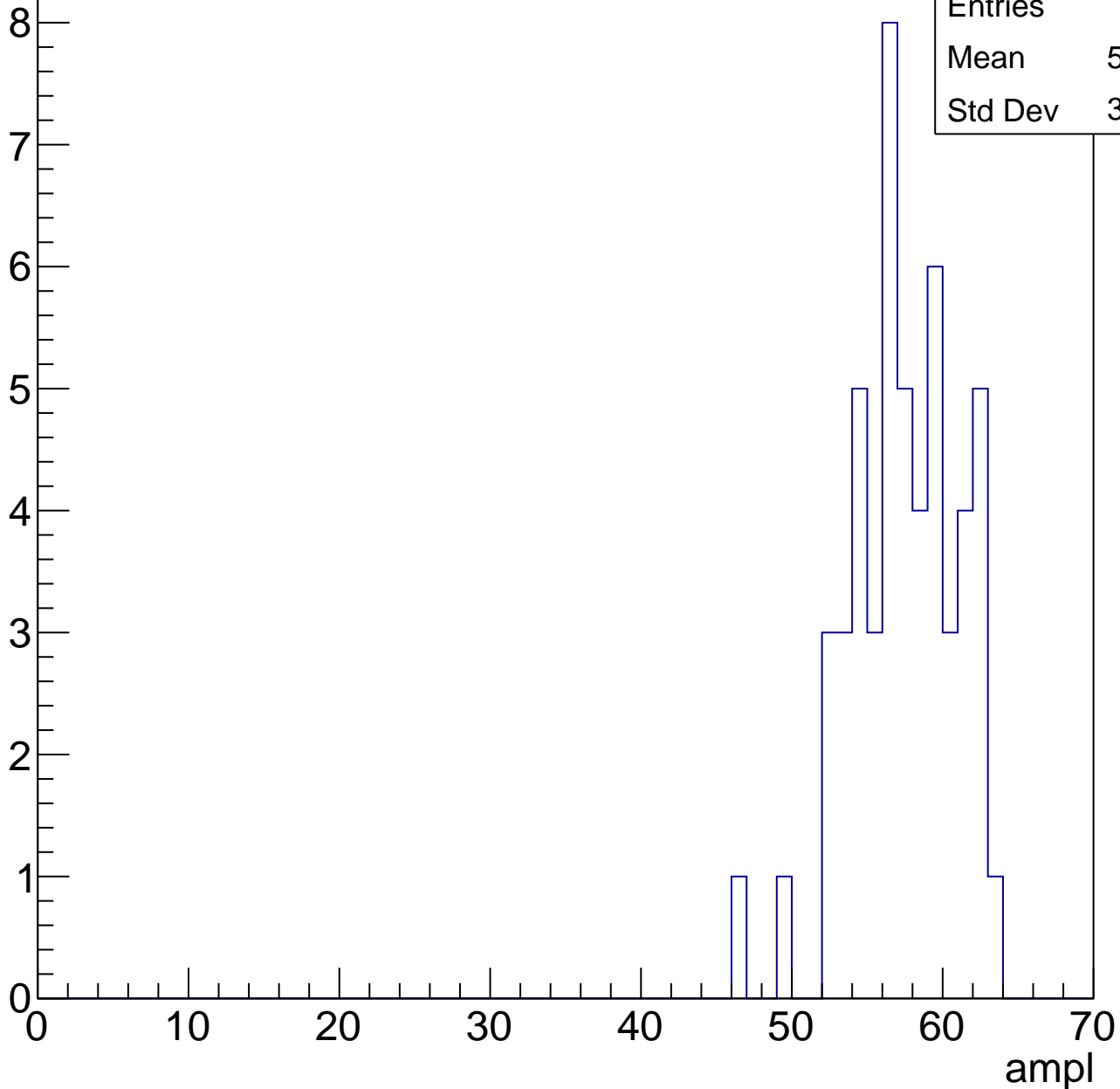


# B0L001S, U2-ch105, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 52    |
| Mean    | 56.94 |
| Std Dev | 3.543 |

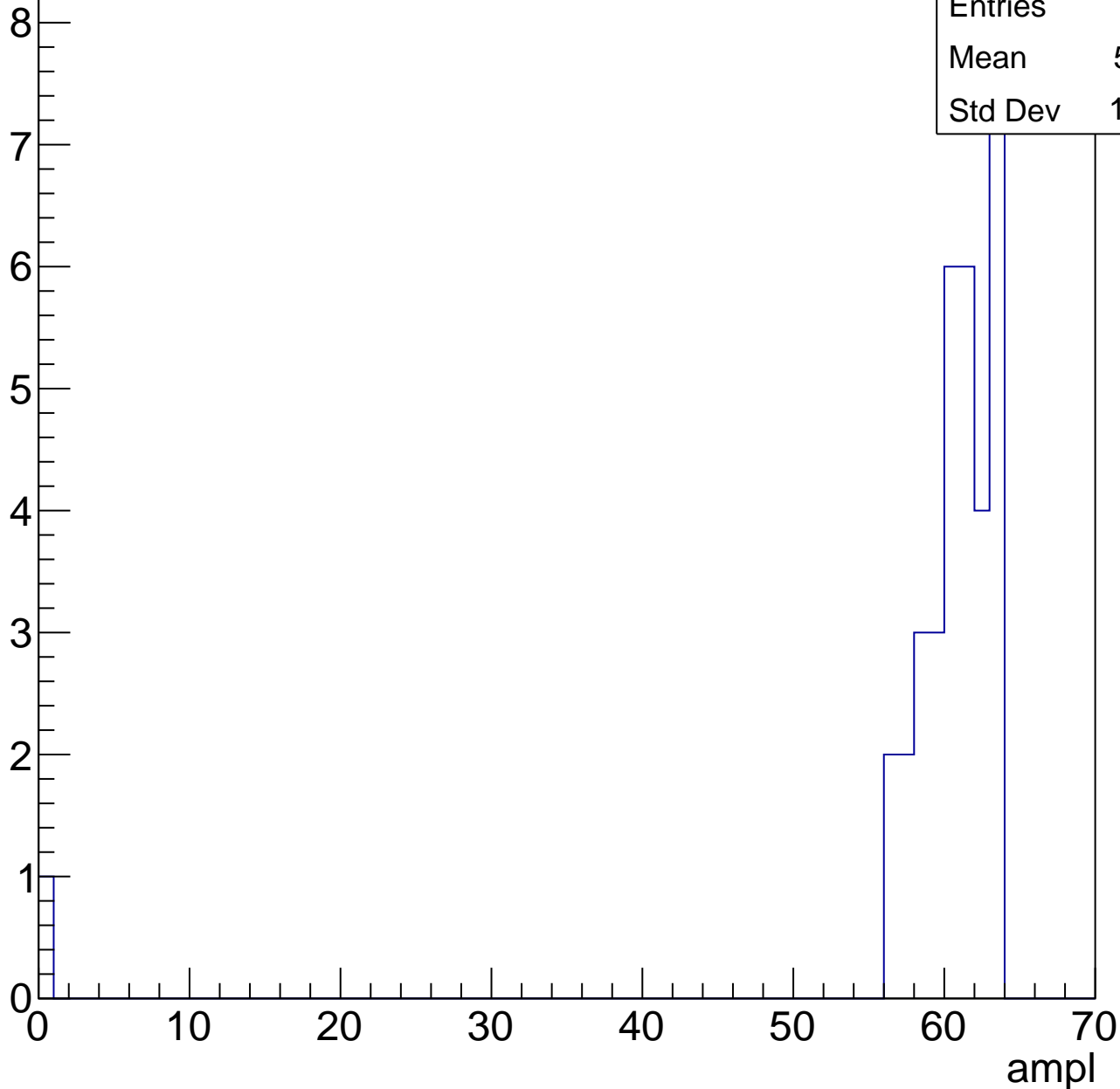


# B0L001S, U2-ch105, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 35    |
| Mean    | 58.71 |
| Std Dev | 10.28 |



# B0L001S, U2-ch105, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch105, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 0 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch106, adc0

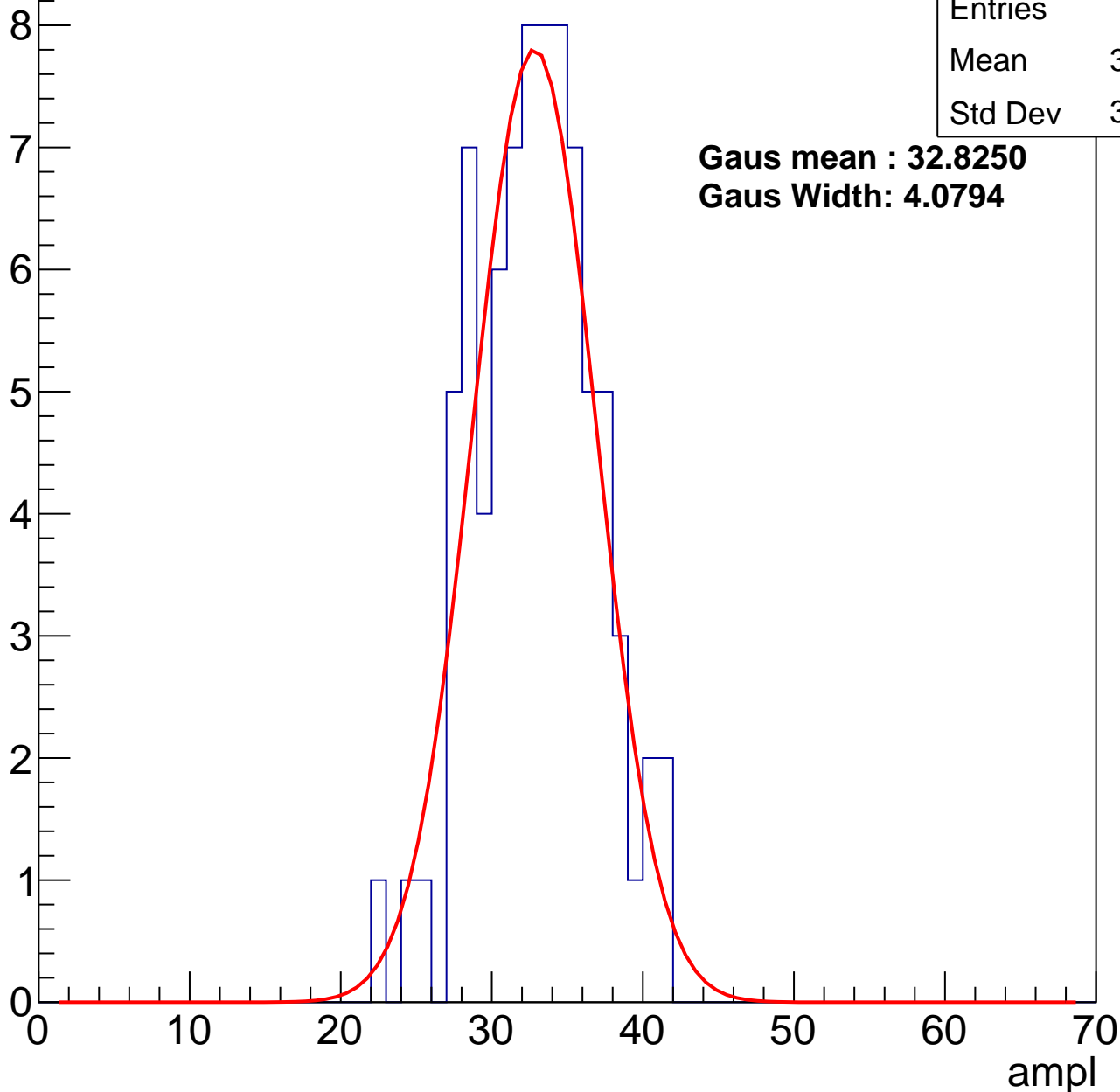
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 81    |
| Mean    | 32.49 |
| Std Dev | 3.932 |

**Gaus mean : 32.8250**

**Gaus Width: 4.0794**



# B0L001S, U2-ch106, adc1

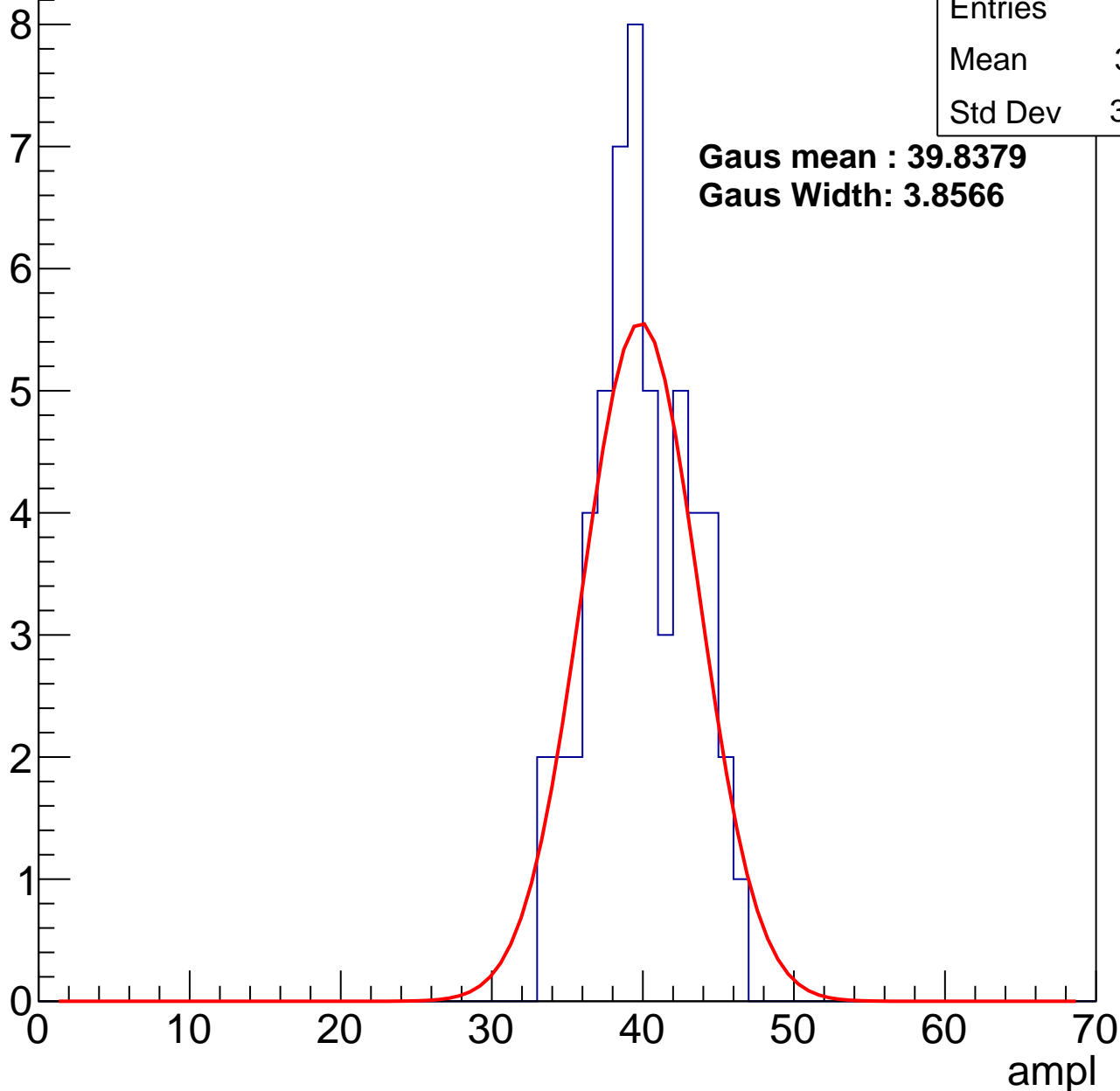
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 54    |
| Mean    | 39.41 |
| Std Dev | 3.206 |

**Gaus mean : 39.8379**

**Gaus Width: 3.8566**



# B0L001S, U2-ch106, adc2

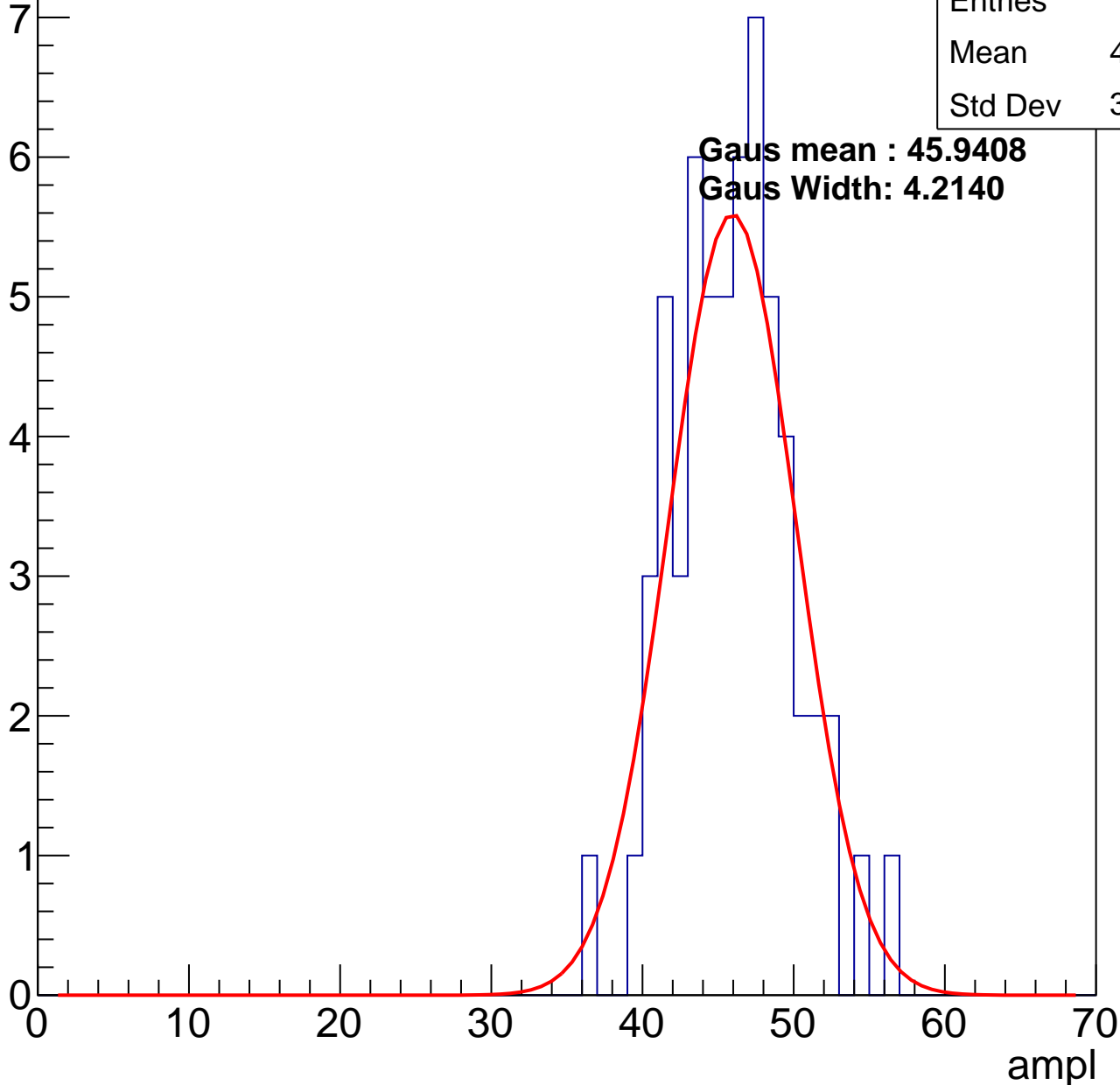
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 59    |
| Mean    | 45.53 |
| Std Dev | 3.855 |

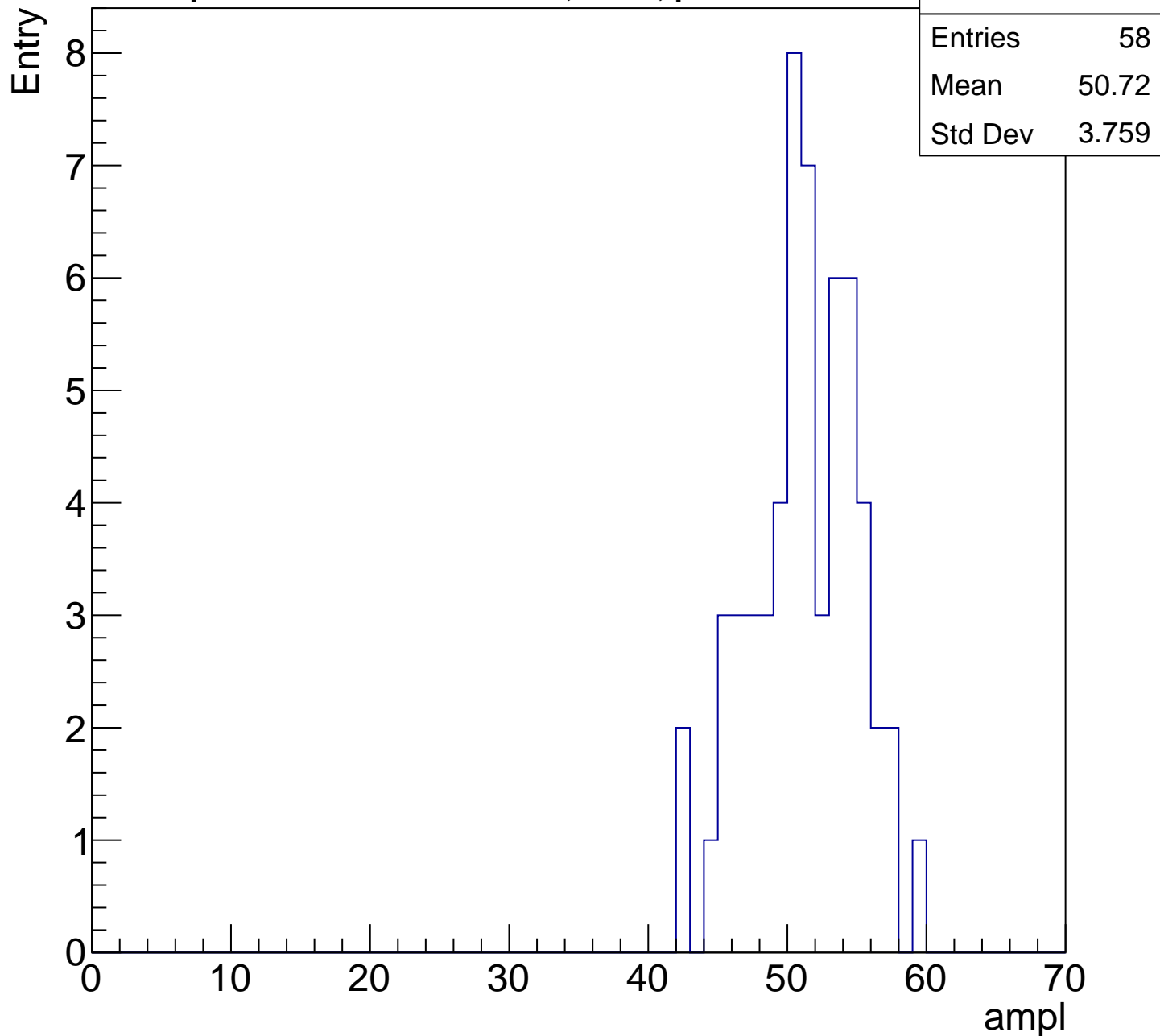
**Gaus mean : 45.9408**

**Gaus Width: 4.2140**



# B0L001S, U2-ch106, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

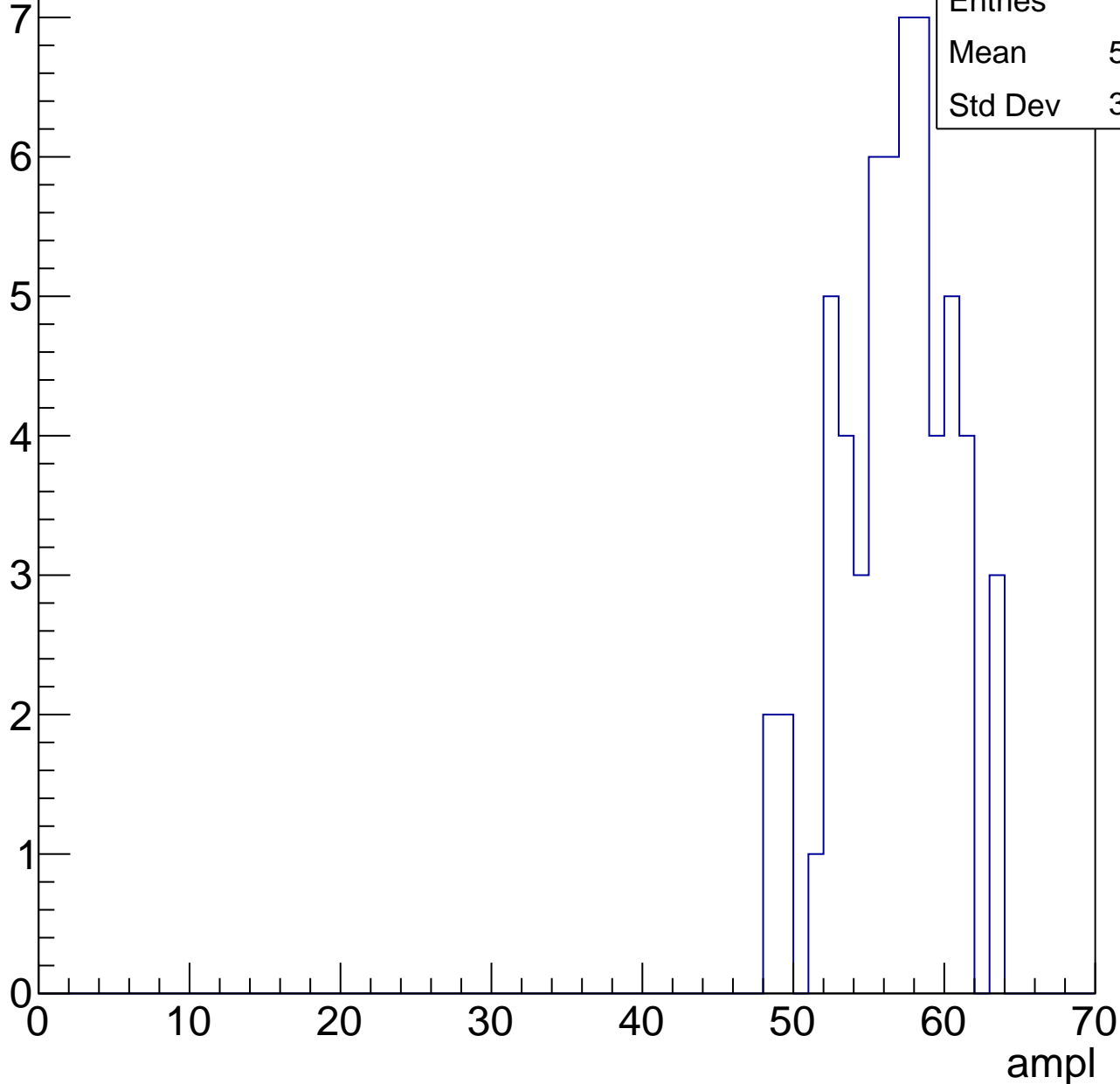


# B0L001S, U2-ch106, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 59    |
| Mean    | 56.25 |
| Std Dev | 3.634 |

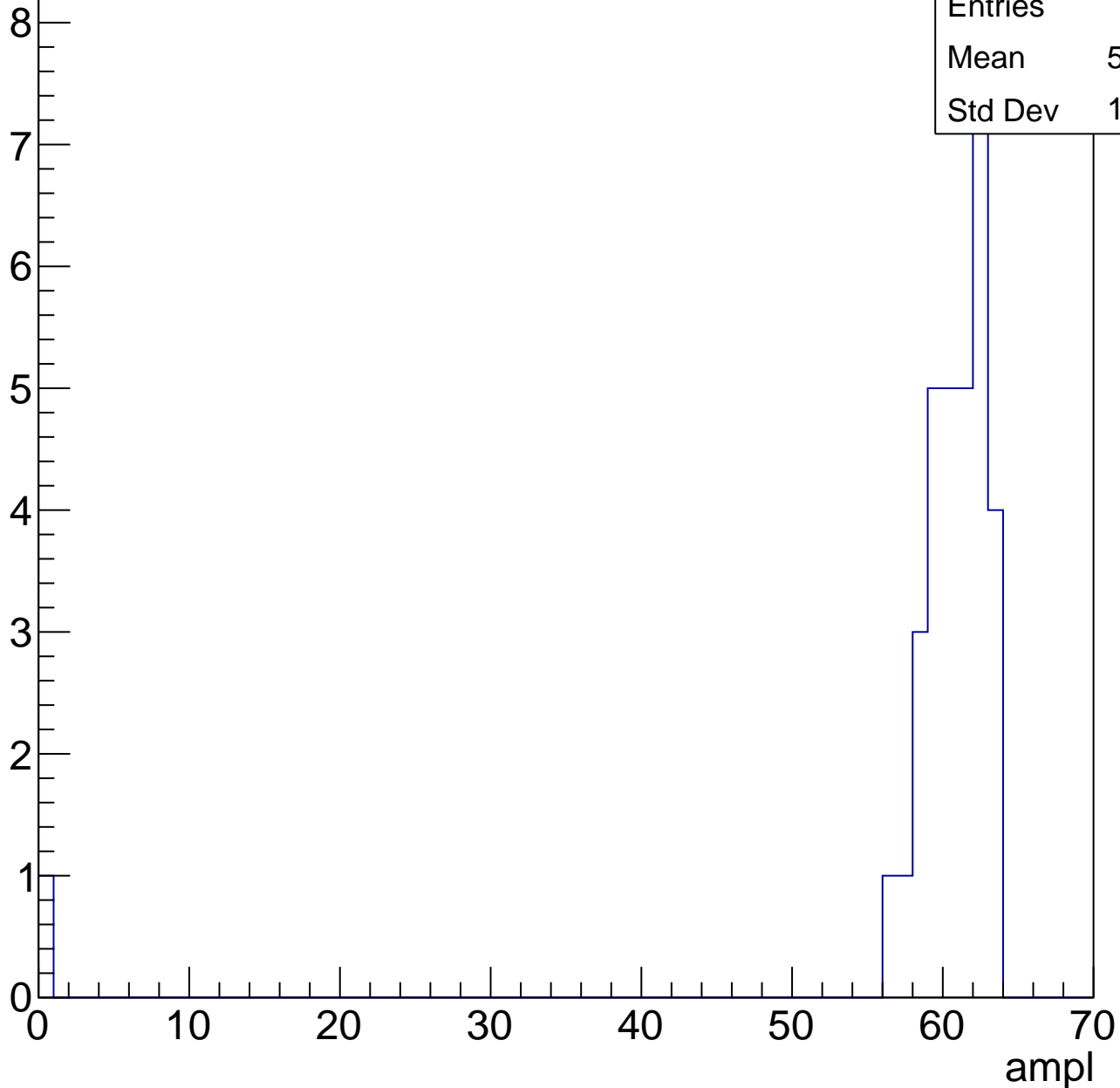


# B0L001S, U2-ch106, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 33    |
| Mean    | 58.64 |
| Std Dev | 10.52 |



# B0L001S, U2-ch106, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch106, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 0 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch107, adc0

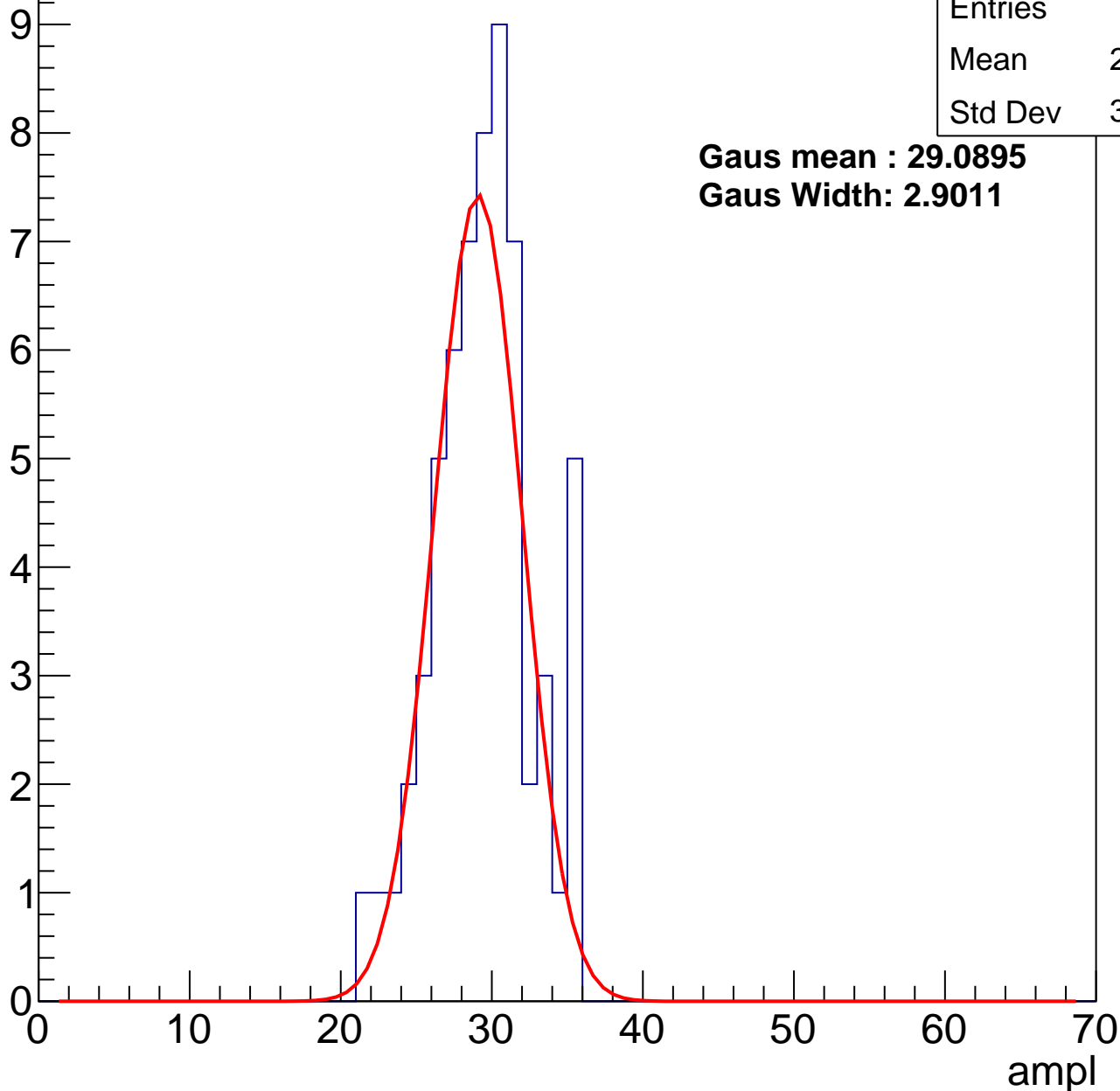
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 61    |
| Mean    | 28.98 |
| Std Dev | 3.216 |

**Gaus mean : 29.0895**

**Gaus Width: 2.9011**



# B0L001S, U2-ch107, adc1

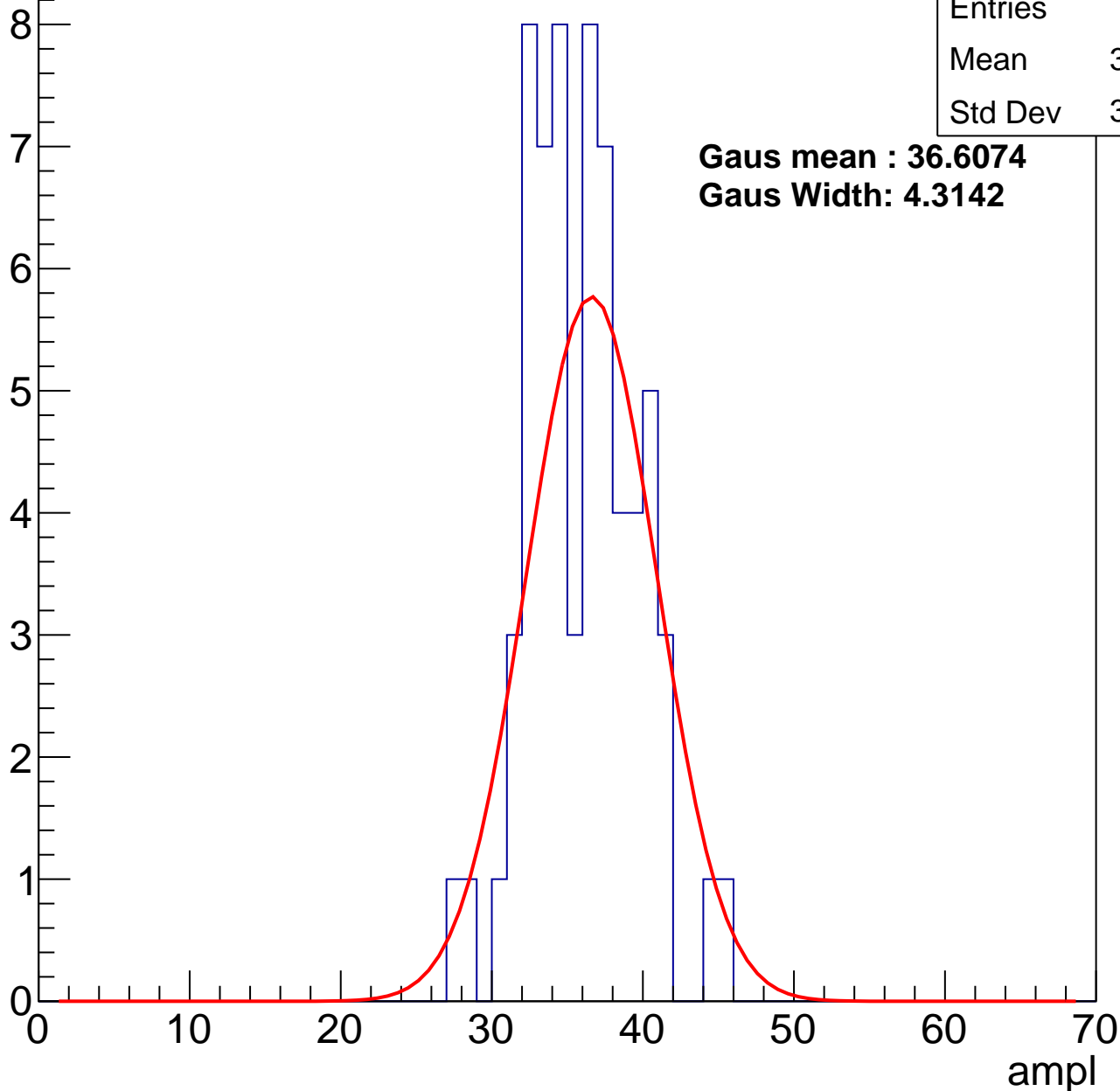
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 65    |
| Mean    | 35.52 |
| Std Dev | 3.565 |

**Gaus mean : 36.6074**

**Gaus Width: 4.3142**



# B0L001S, U2-ch107, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 76    |
| Mean    | 42.34 |
| Std Dev | 4.172 |

**Gaus mean : 42.2257**

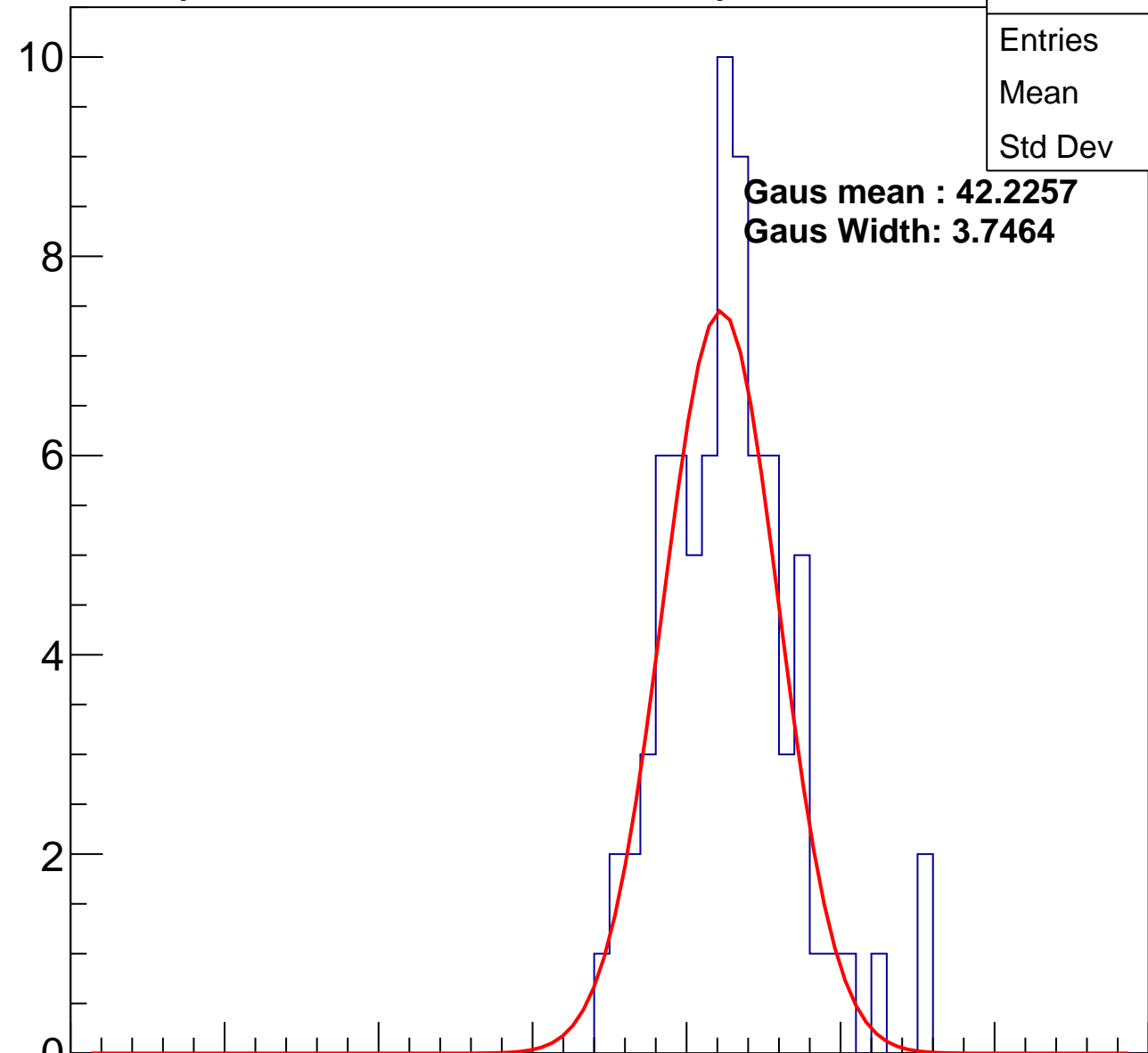
**Gaus Width: 3.7464**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

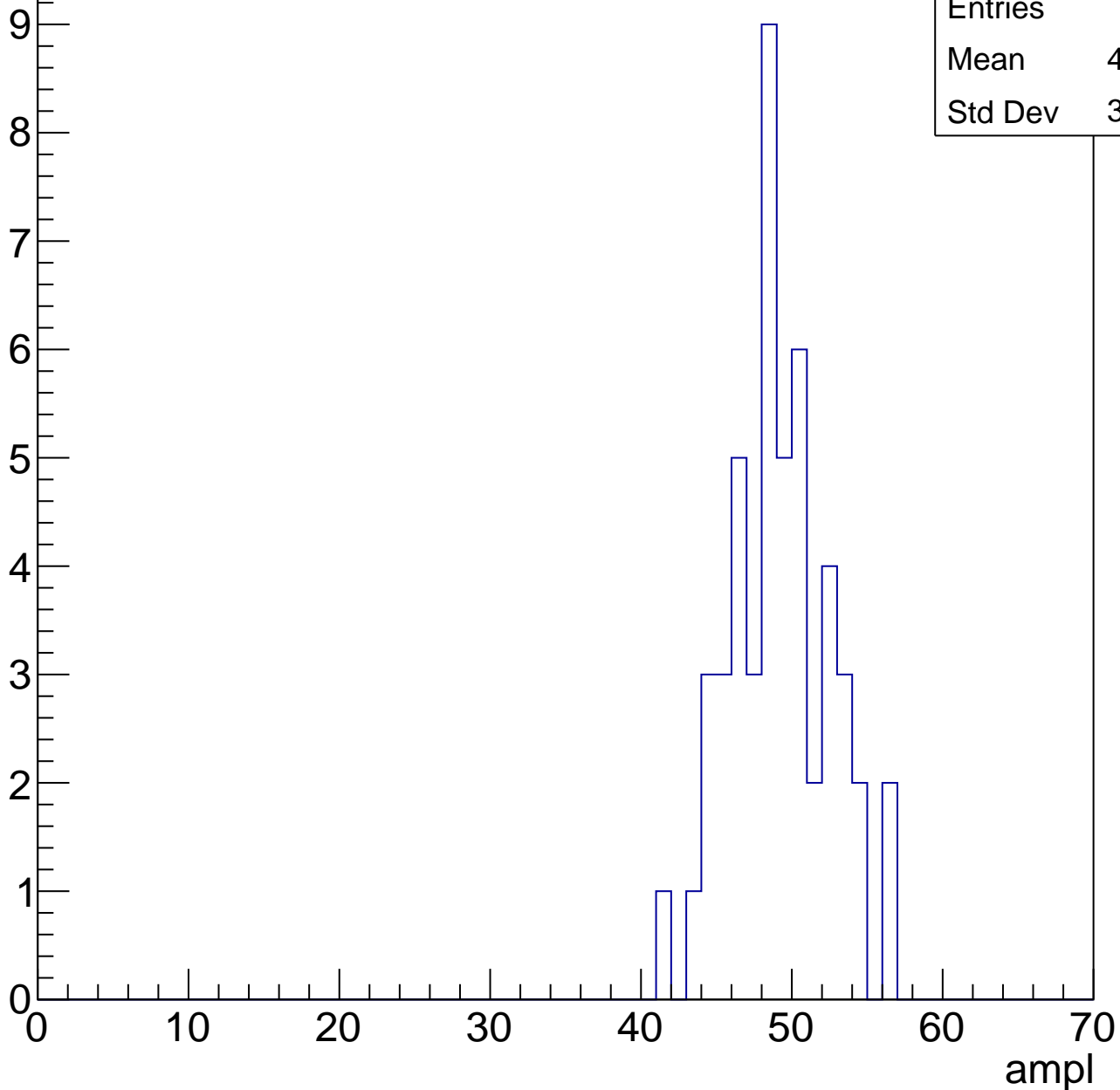


# B0L001S, U2-ch107, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 49    |
| Mean    | 48.73 |
| Std Dev | 3.294 |

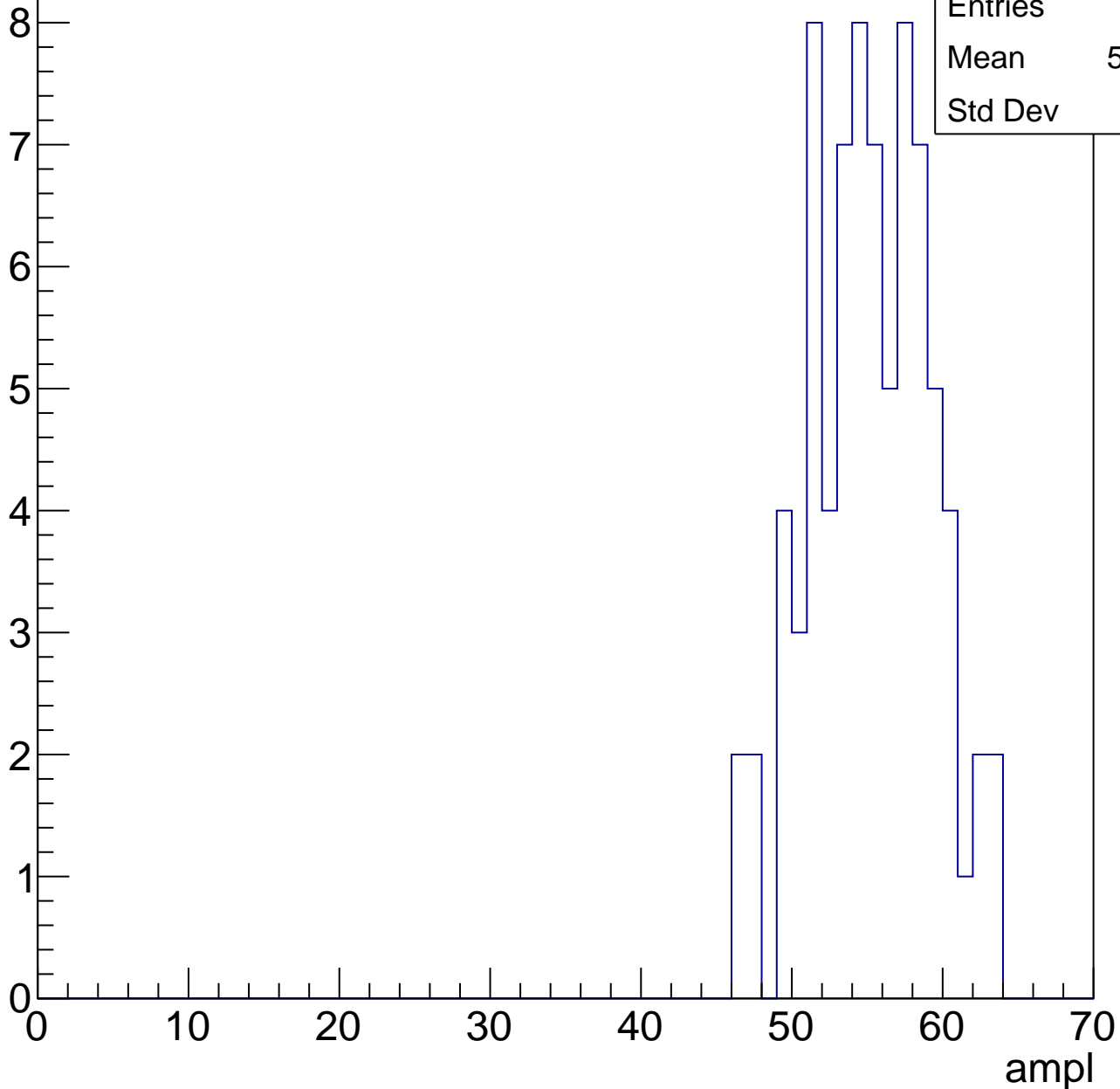


# B0L001S, U2-ch107, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 79    |
| Mean    | 54.73 |
| Std Dev | 3.97  |

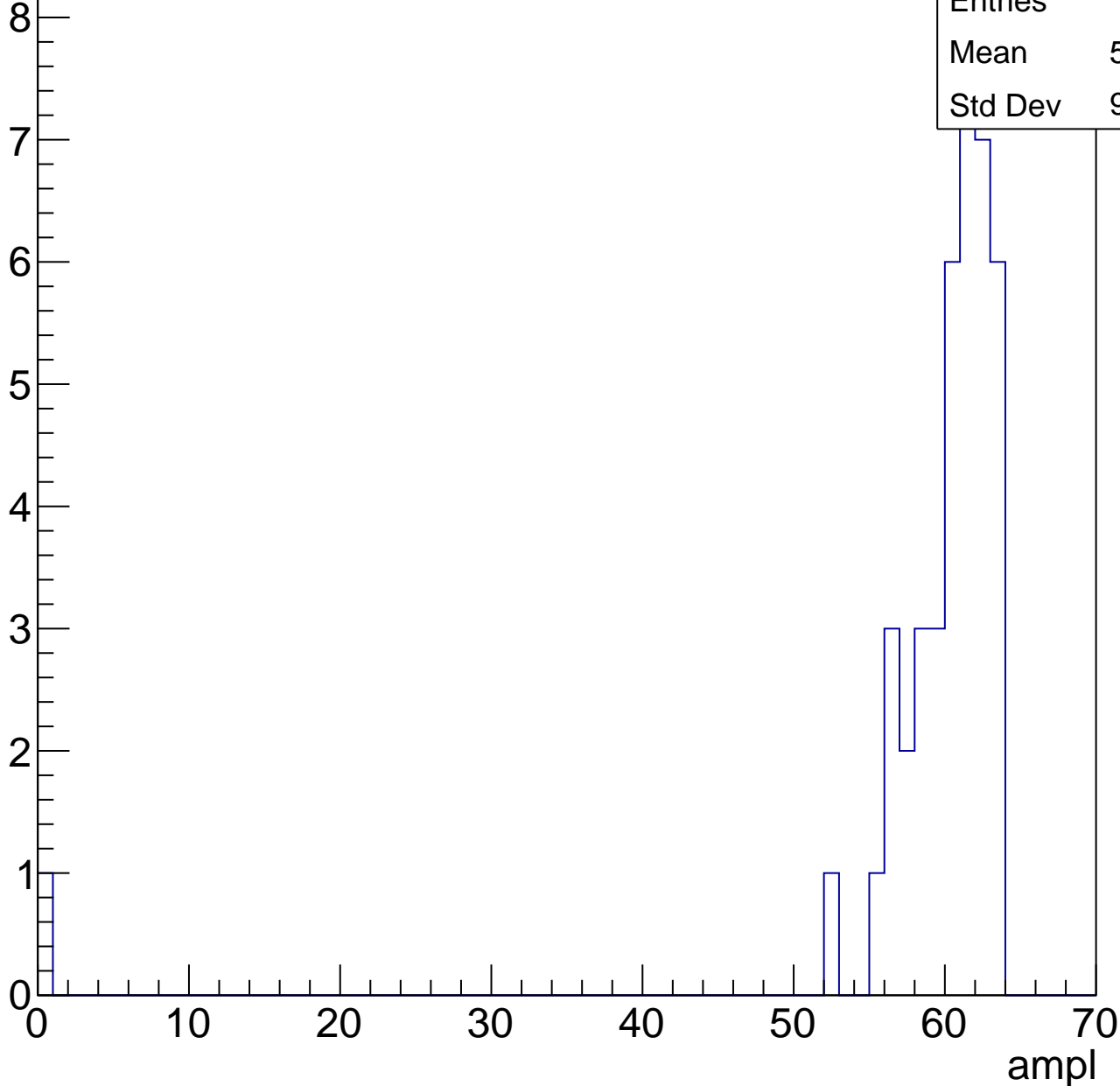


# B0L001S, U2-ch107, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 41    |
| Mean    | 58.54 |
| Std Dev | 9.592 |



# B0L001S, U2-ch107, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

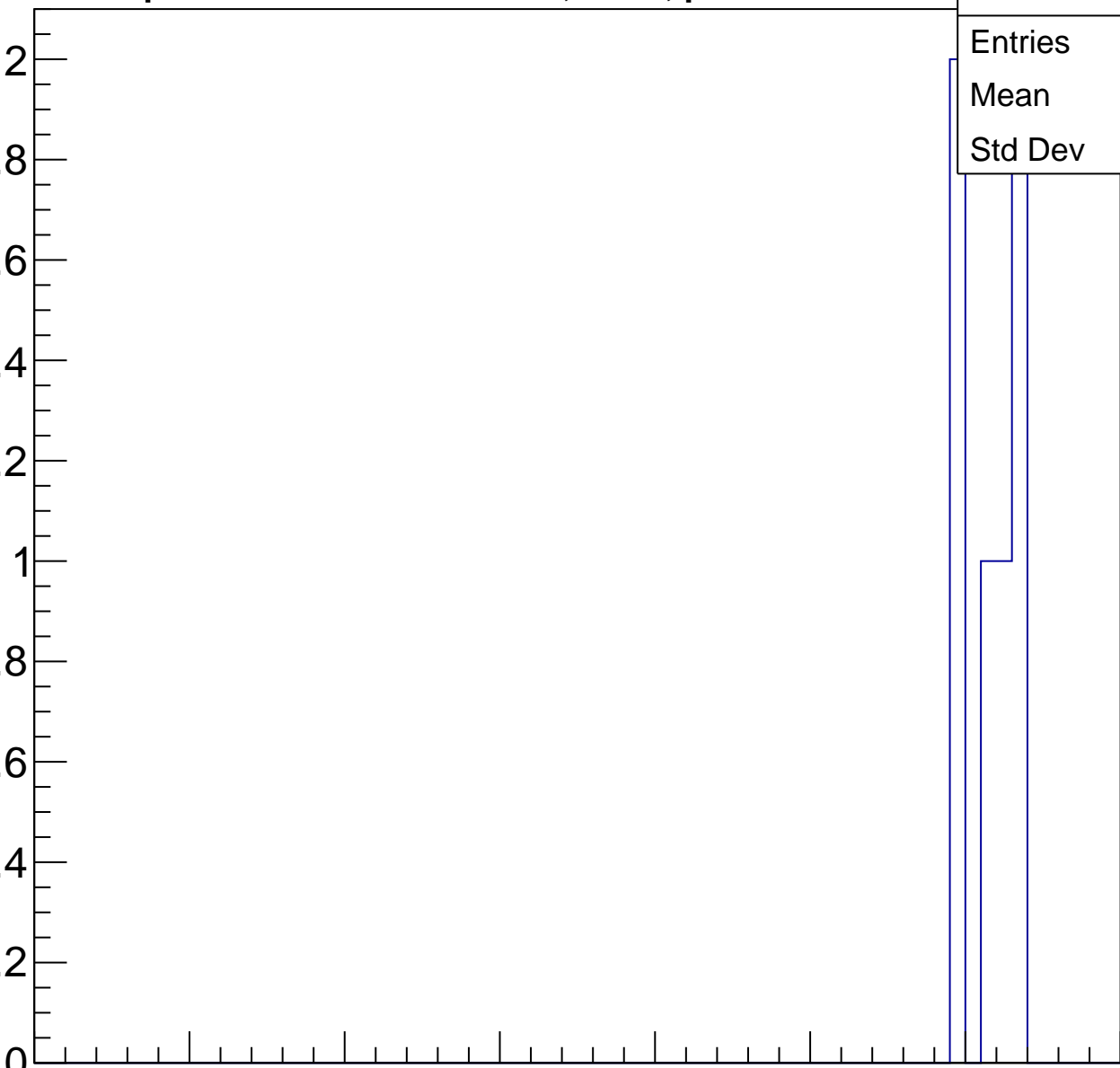
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

|         |       |
|---------|-------|
| Entries | 6     |
| Mean    | 61.17 |
| Std Dev | 1.675 |

0 10 20 30 40 50 60 70

ampl





# B0L001S, U2-ch107, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U2-ch108, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 79    |
| Mean    | 29.62 |
| Std Dev | 7.764 |

**Gaus mean : 31.8518**

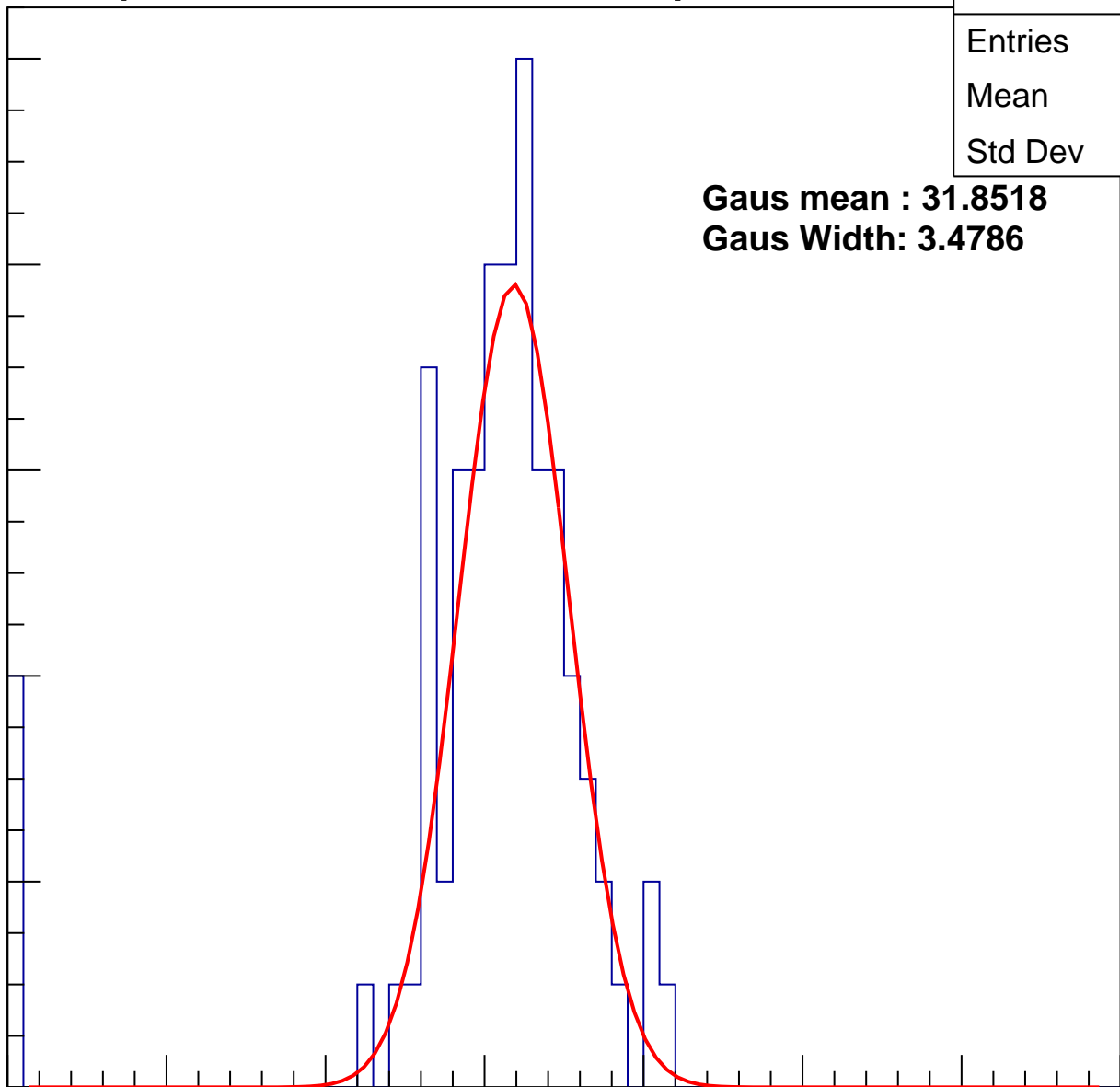
**Gaus Width: 3.4786**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



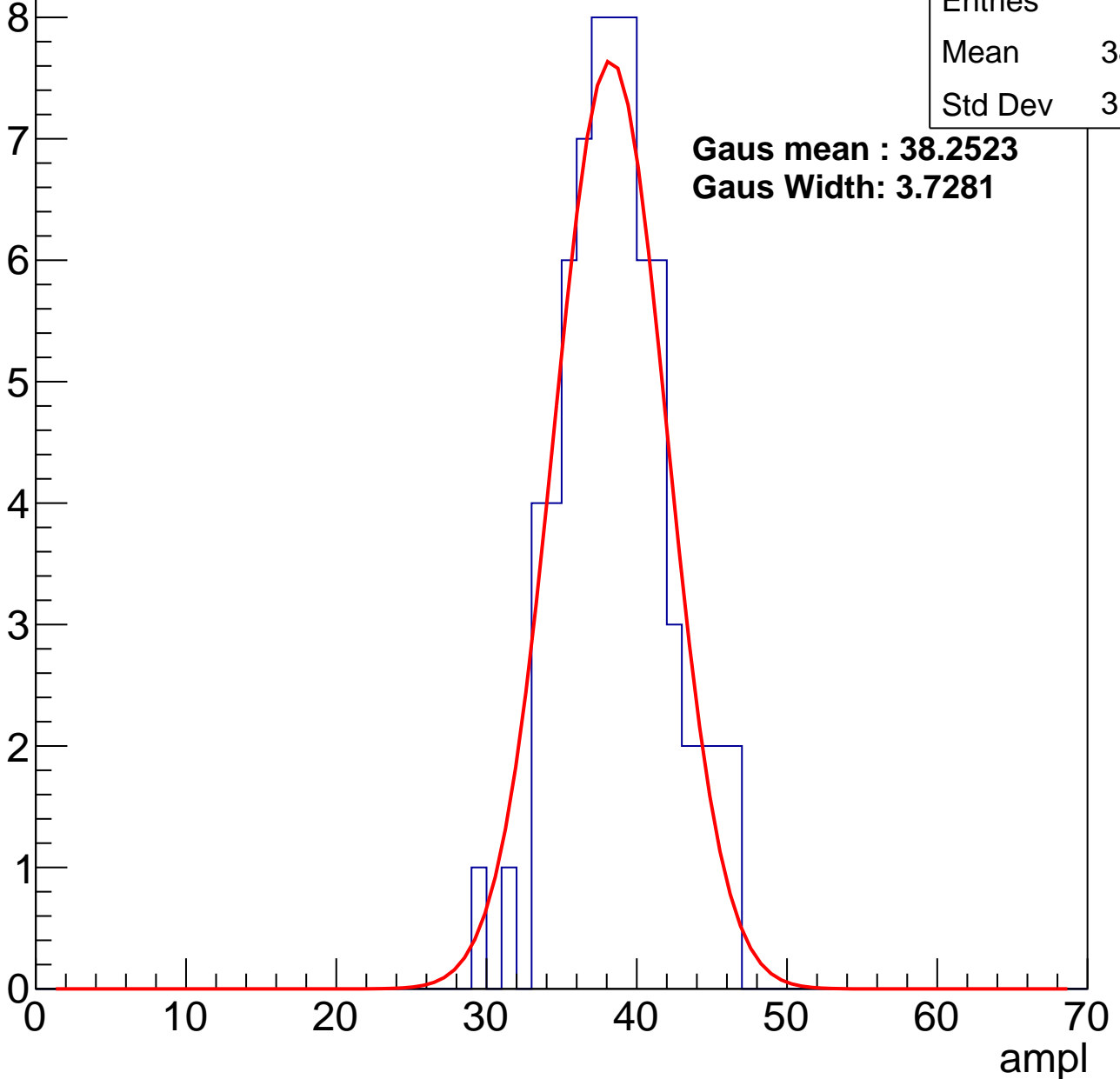
# B0L001S, U2-ch108, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 70    |
| Mean    | 38.14 |
| Std Dev | 3.514 |

**Gaus mean : 38.2523**  
**Gaus Width: 3.7281**



# B0L001S, U2-ch108, adc2

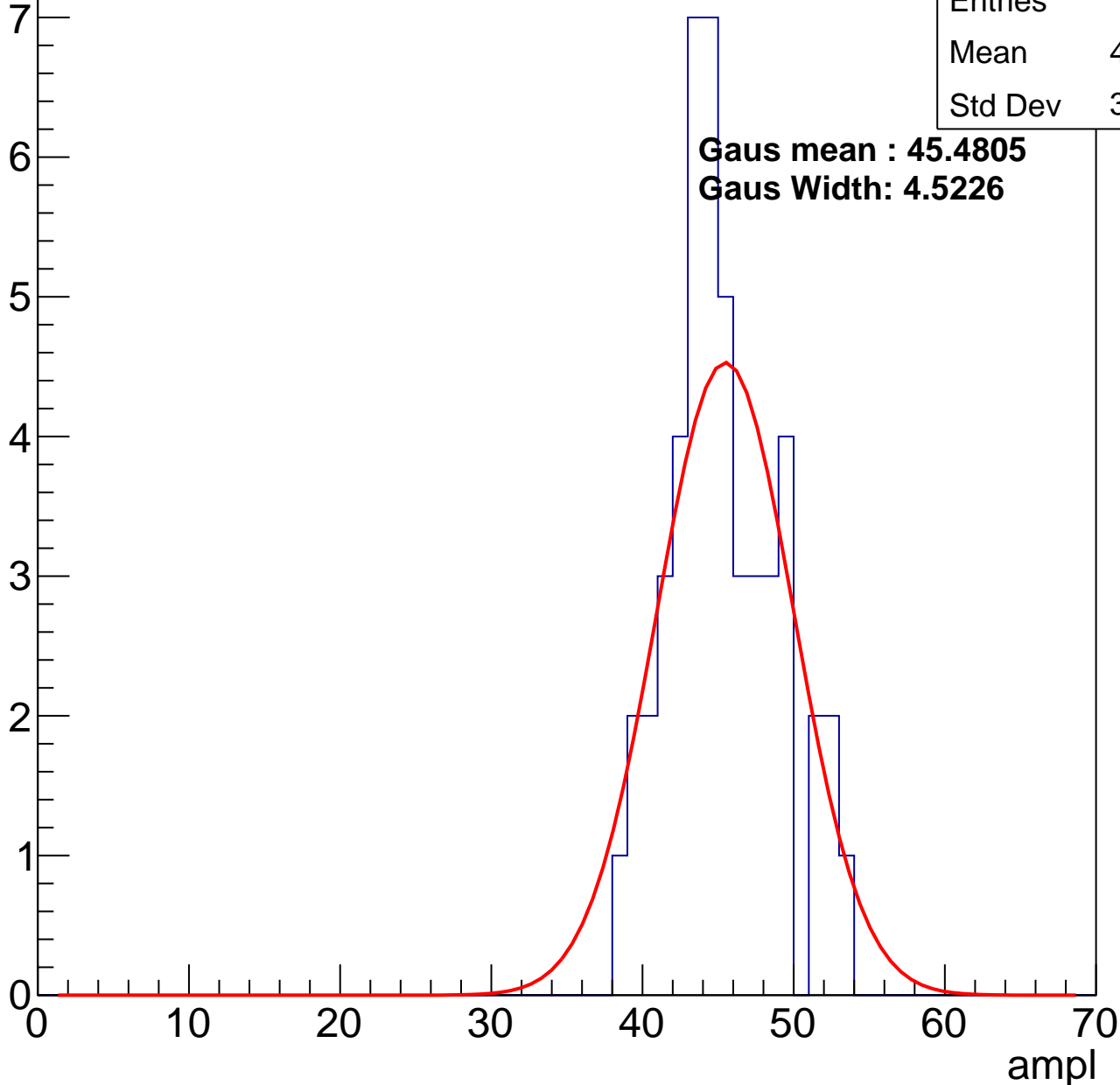
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 49    |
| Mean    | 44.88 |
| Std Dev | 3.584 |

**Gaus mean : 45.4805**

**Gaus Width: 4.5226**

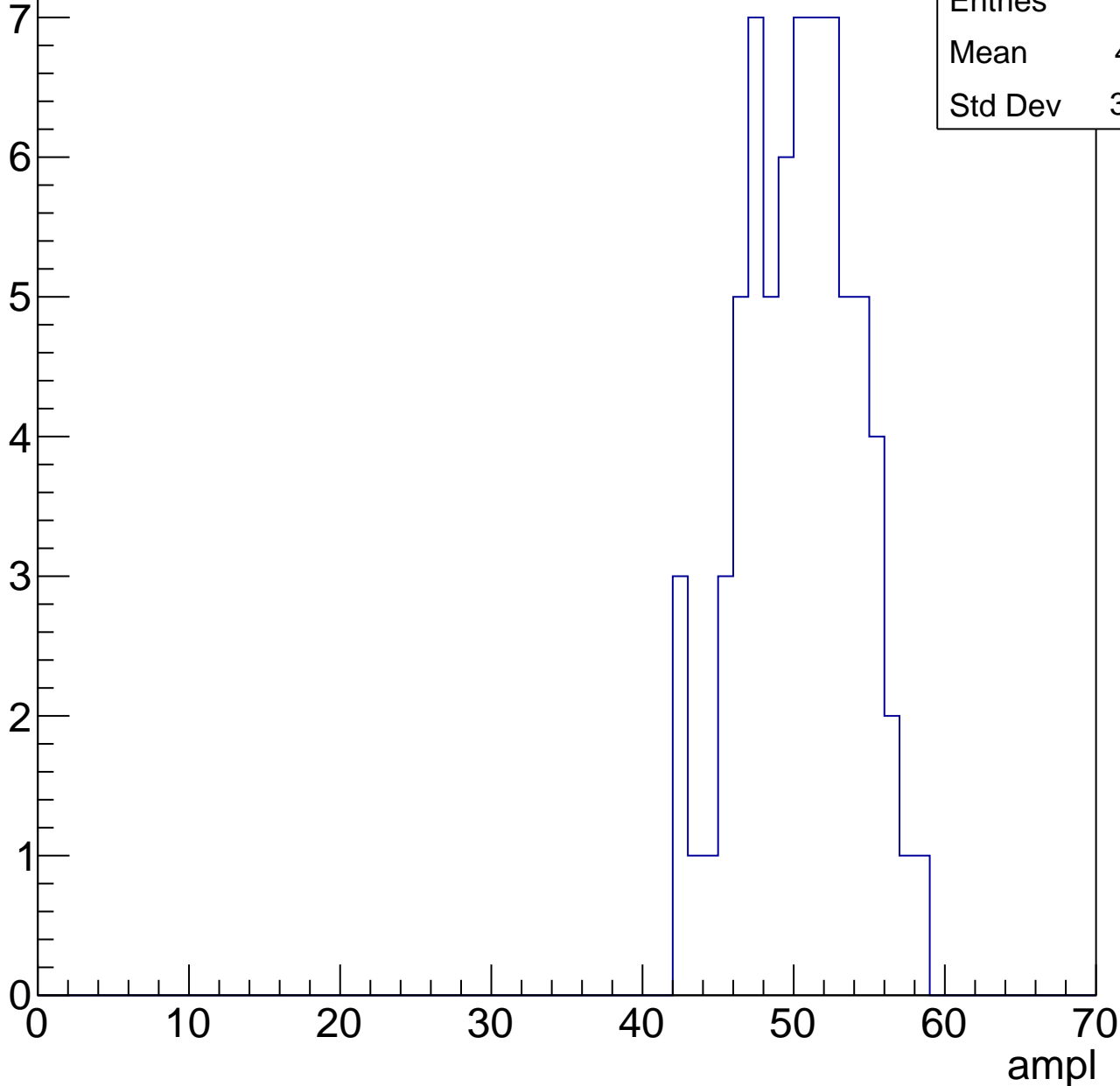


# B0L001S, U2-ch108, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 70    |
| Mean    | 49.91 |
| Std Dev | 3.714 |

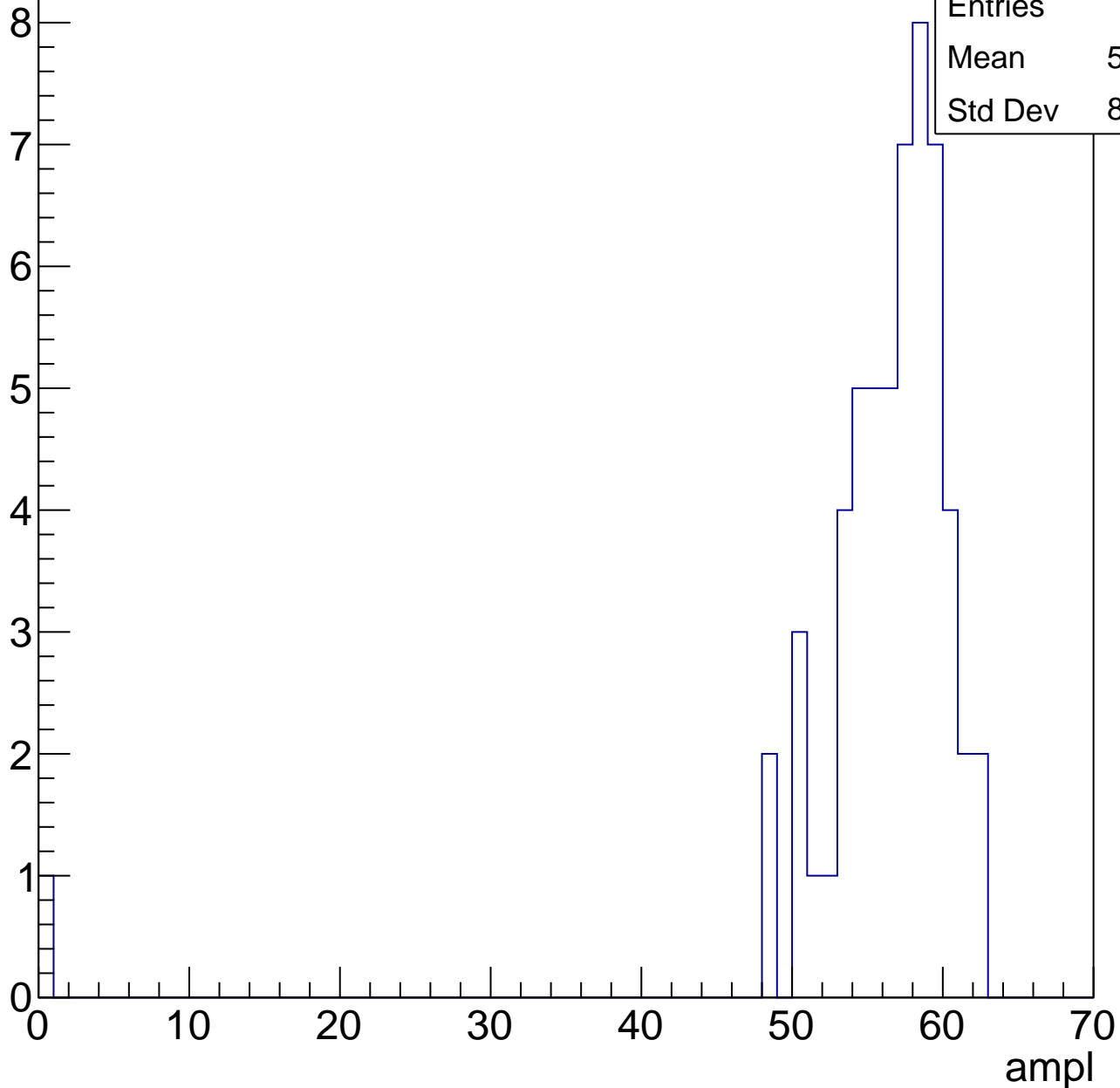


# B0L001S, U2-ch108, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 57    |
| Mean    | 55.23 |
| Std Dev | 8.087 |



# B0L001S, U2-ch108, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

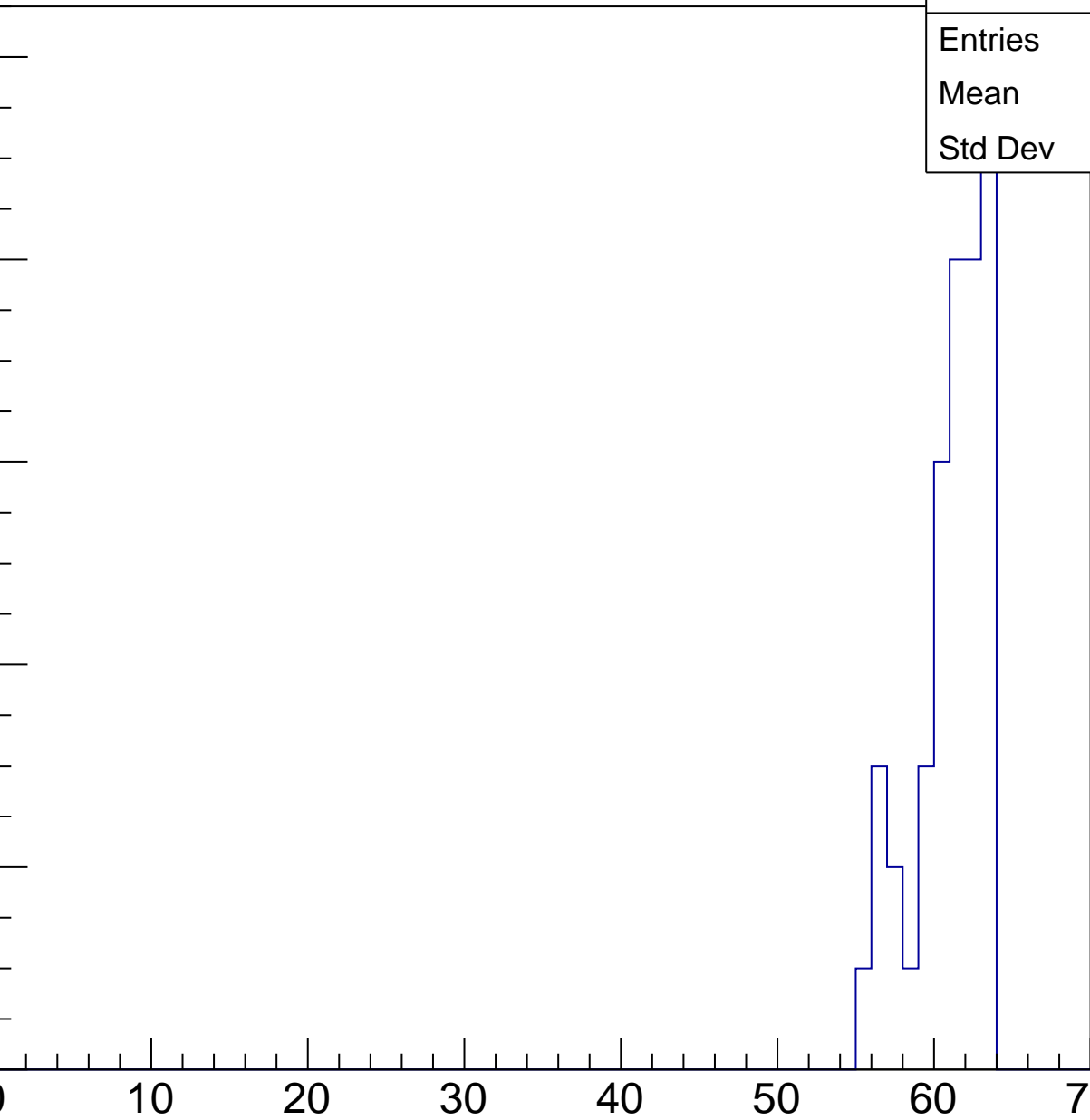
|         |       |
|---------|-------|
| Entries | 42    |
| Mean    | 60.62 |
| Std Dev | 2.246 |

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B0L001S, U2-ch108, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 0 |
| Mean    | 0 |
| Std Dev | 0 |



# B0L001S, U2-ch108, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 2 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch109, adc0

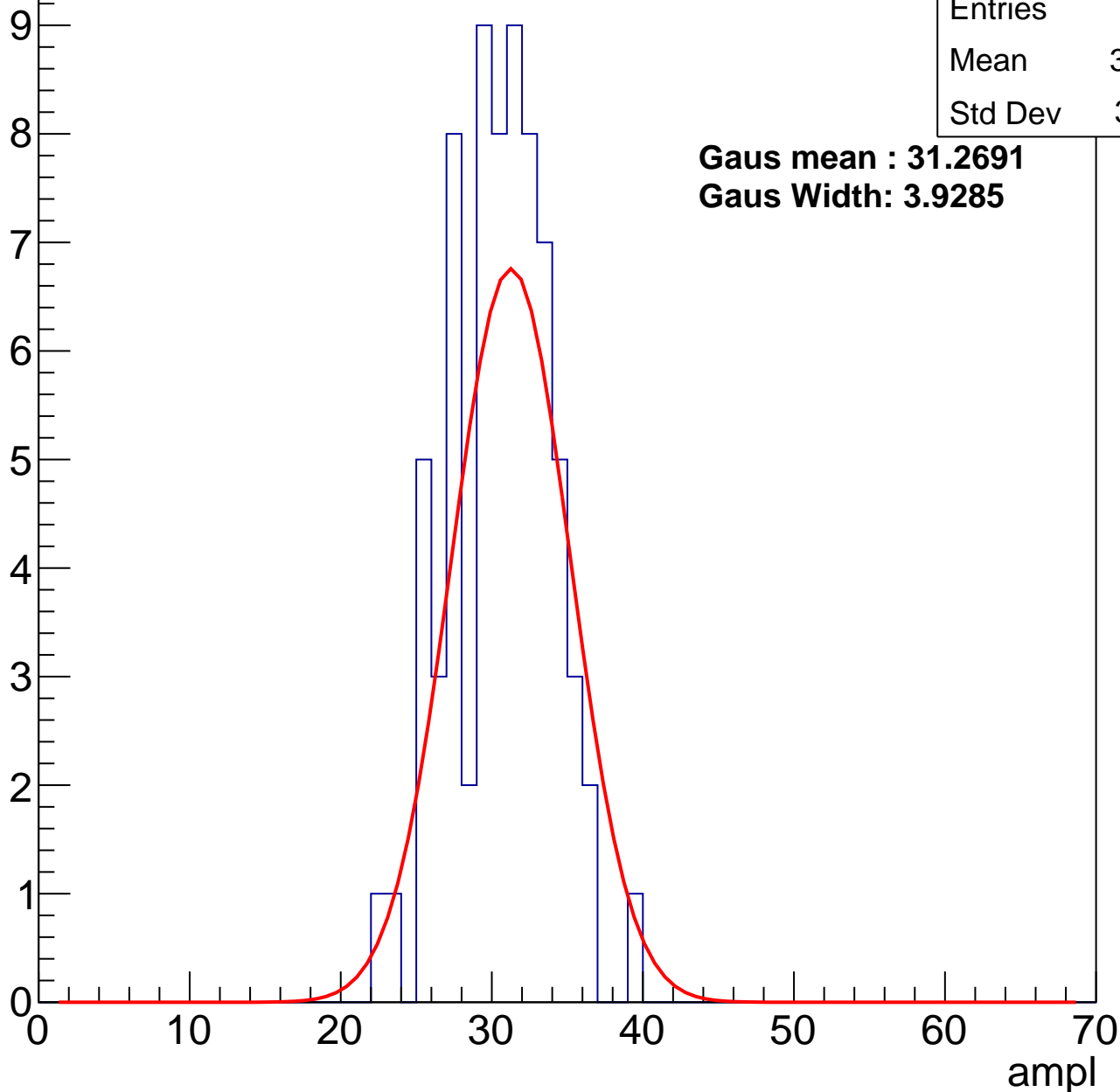
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 72    |
| Mean    | 30.18 |
| Std Dev | 3.301 |

**Gaus mean : 31.2691**

**Gaus Width: 3.9285**



# B0L001S, U2-ch109, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 80    |
| Mean    | 38.14 |
| Std Dev | 3.545 |

**Gaus mean : 38.5471**

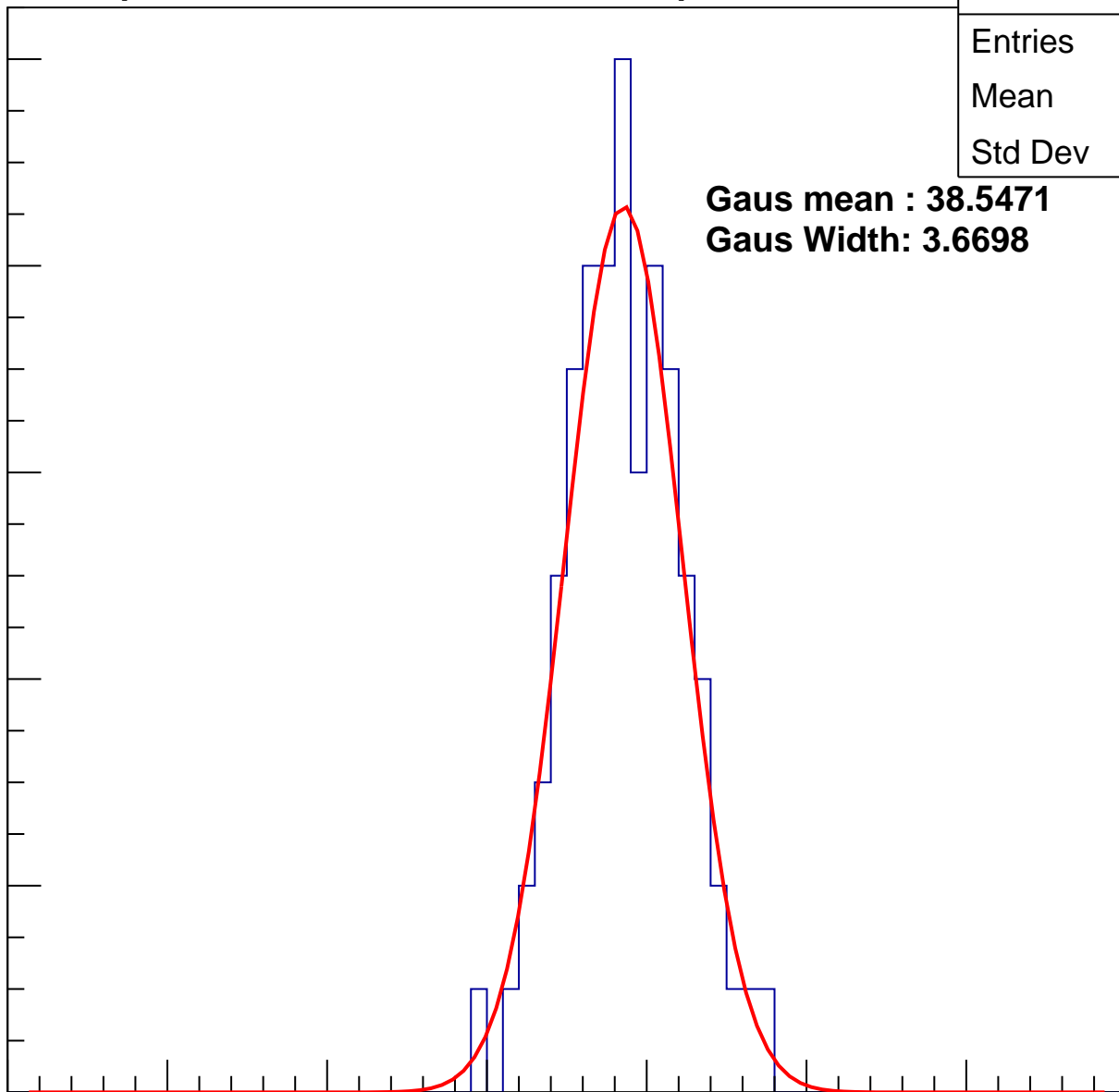
**Gaus Width: 3.6698**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B0L001S, U2-ch109, adc2

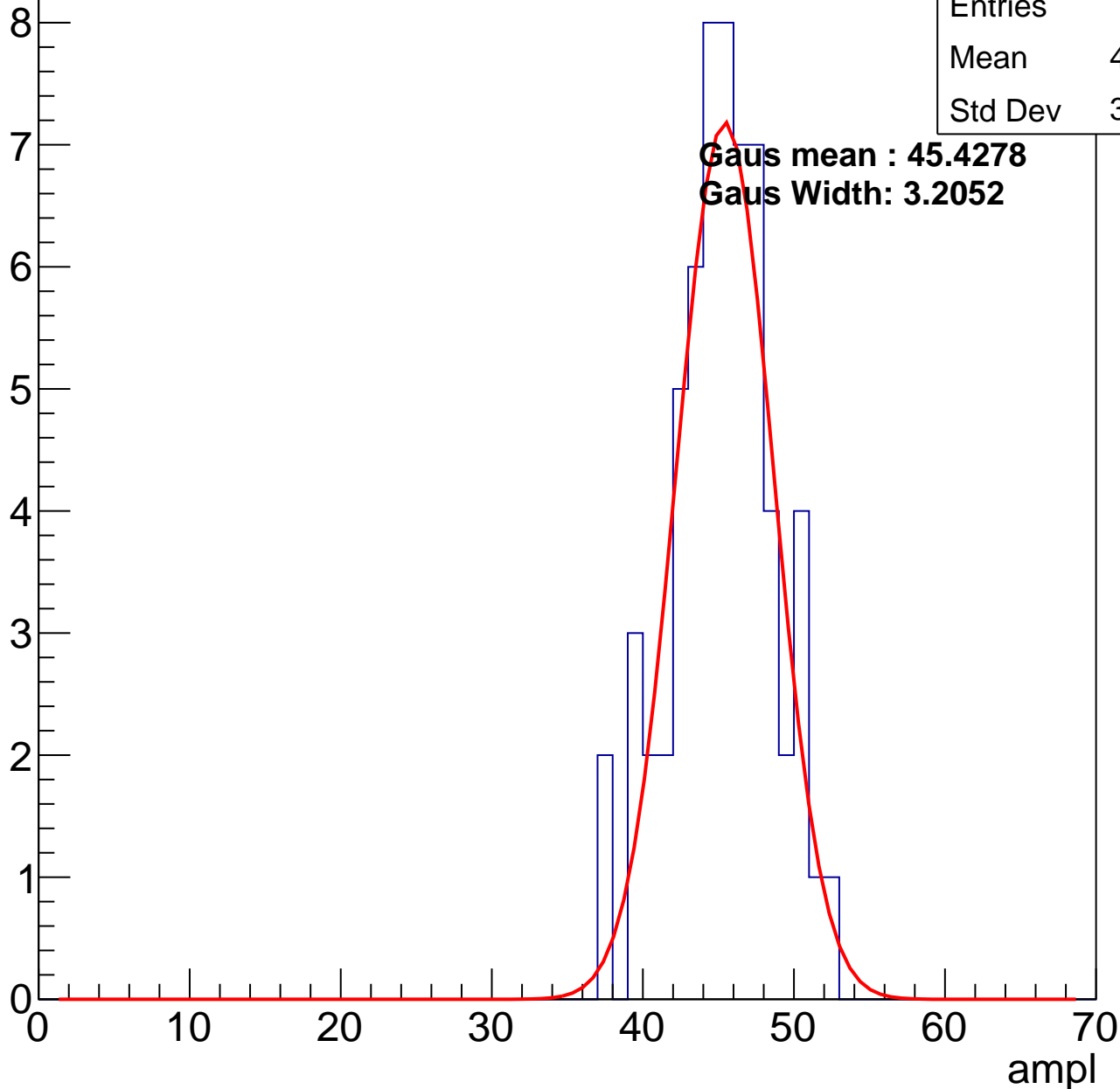
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 62    |
| Mean    | 44.79 |
| Std Dev | 3.312 |

**Gaus mean : 45.4278**

**Gaus Width: 3.2052**

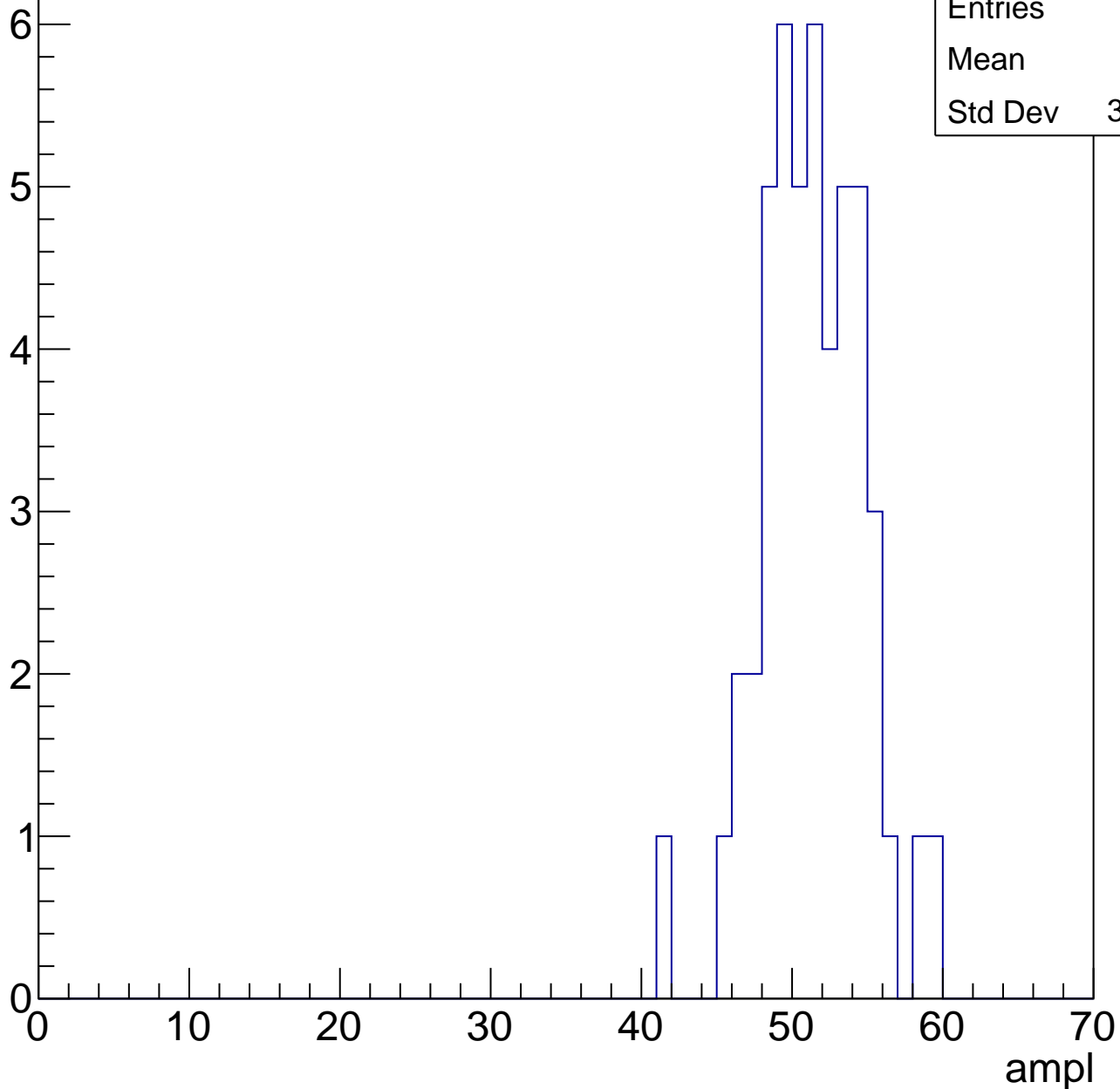


# B0L001S, U2-ch109, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 48    |
| Mean    | 50.9  |
| Std Dev | 3.374 |

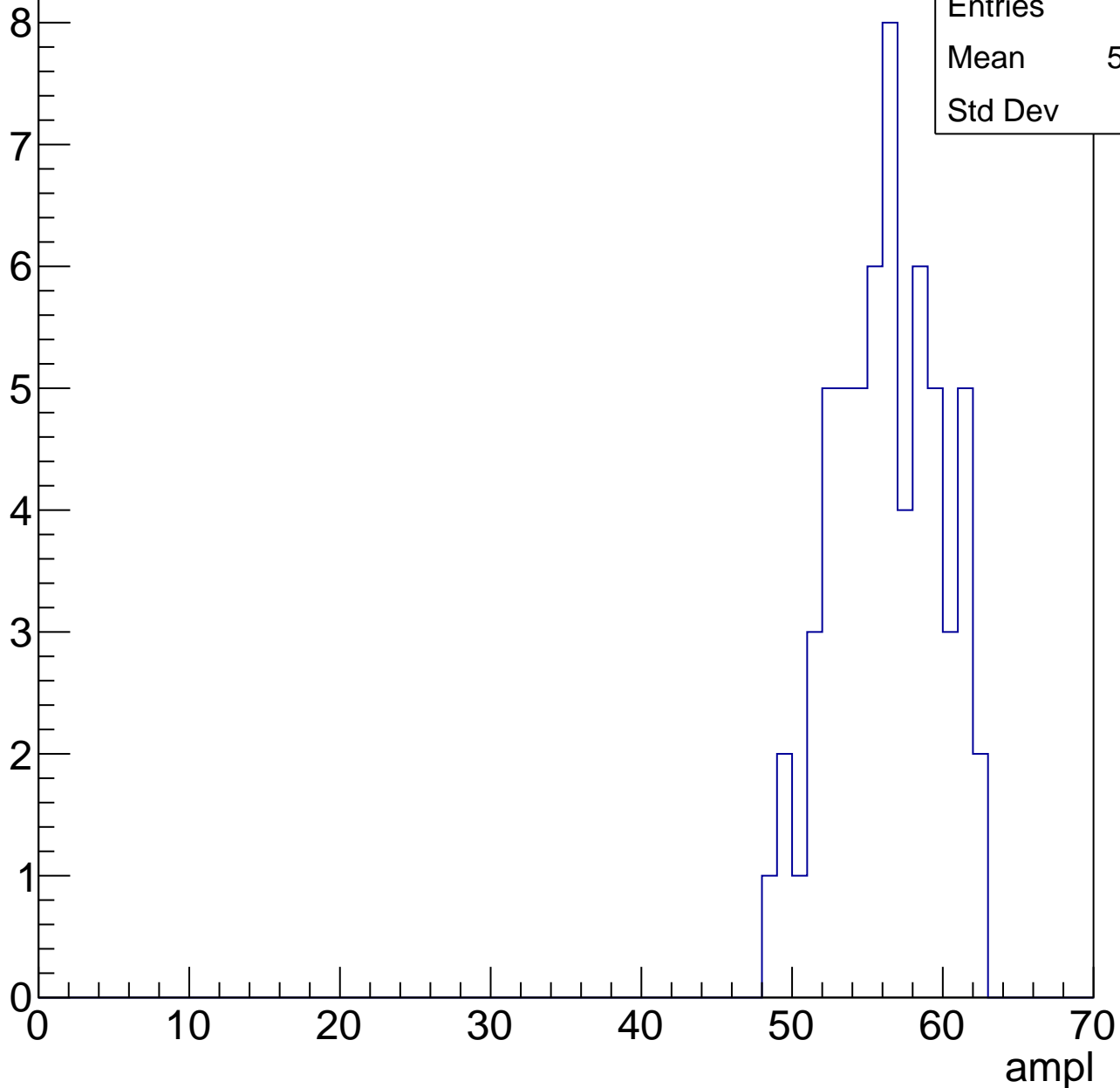


# B0L001S, U2-ch109, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

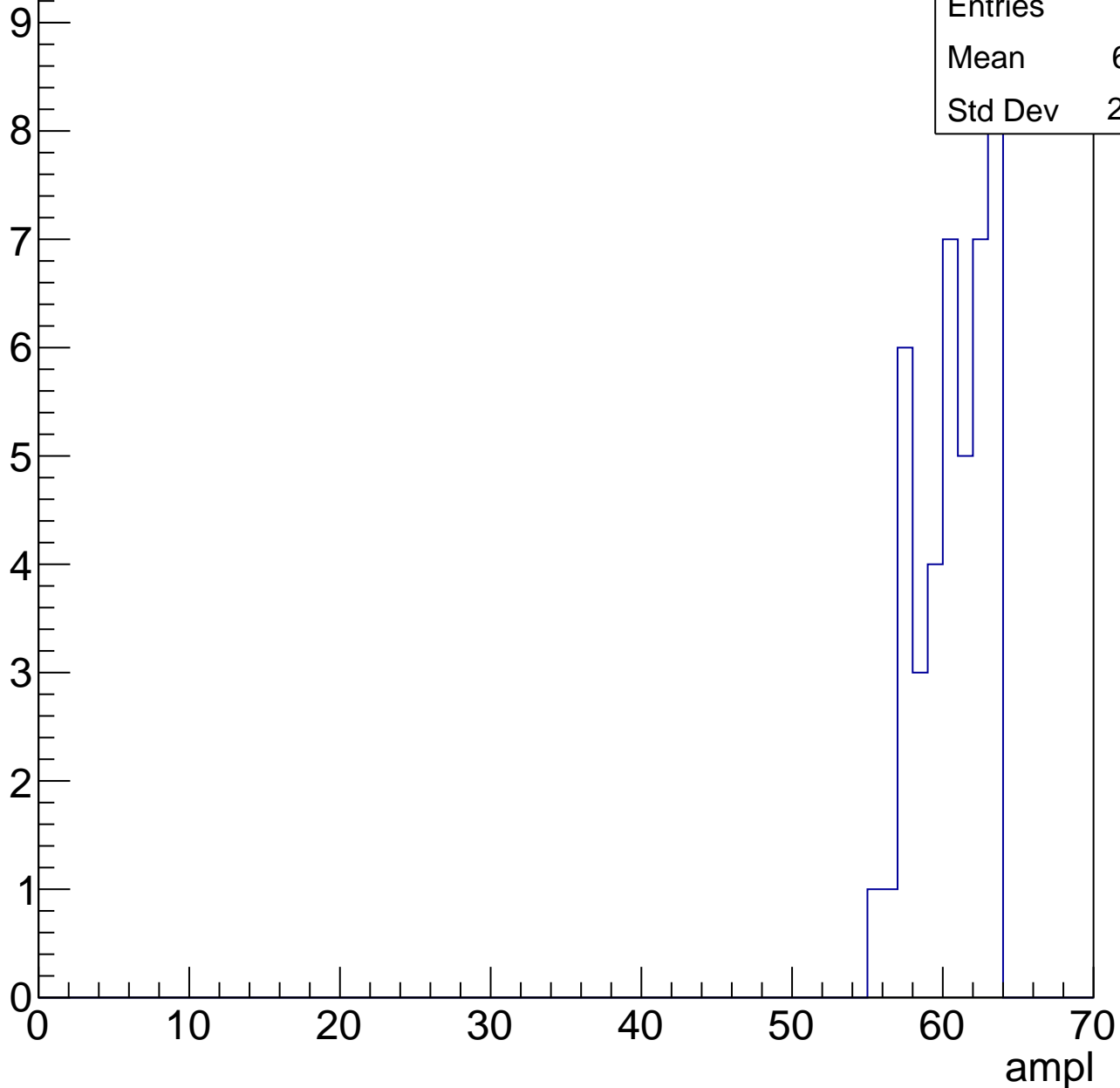
|         |       |
|---------|-------|
| Entries | 61    |
| Mean    | 55.77 |
| Std Dev | 3.48  |



# B0L001S, U2-ch109, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

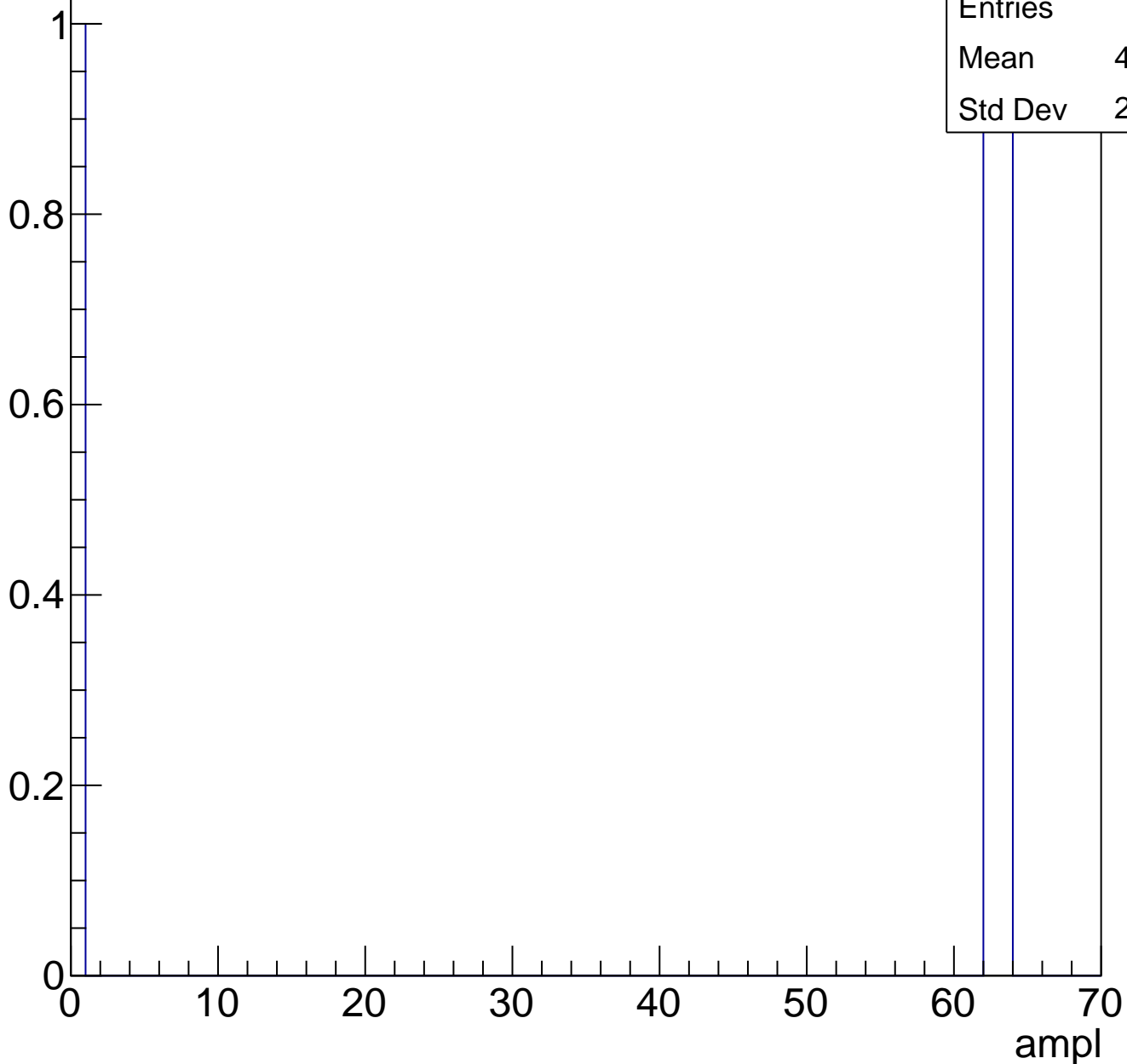
Entry



# B0L001S, U2-ch109, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch109, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 1 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch110, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 77    |
| Mean    | 28.36 |
| Std Dev | 3.941 |

**Gaus mean : 29.2188**

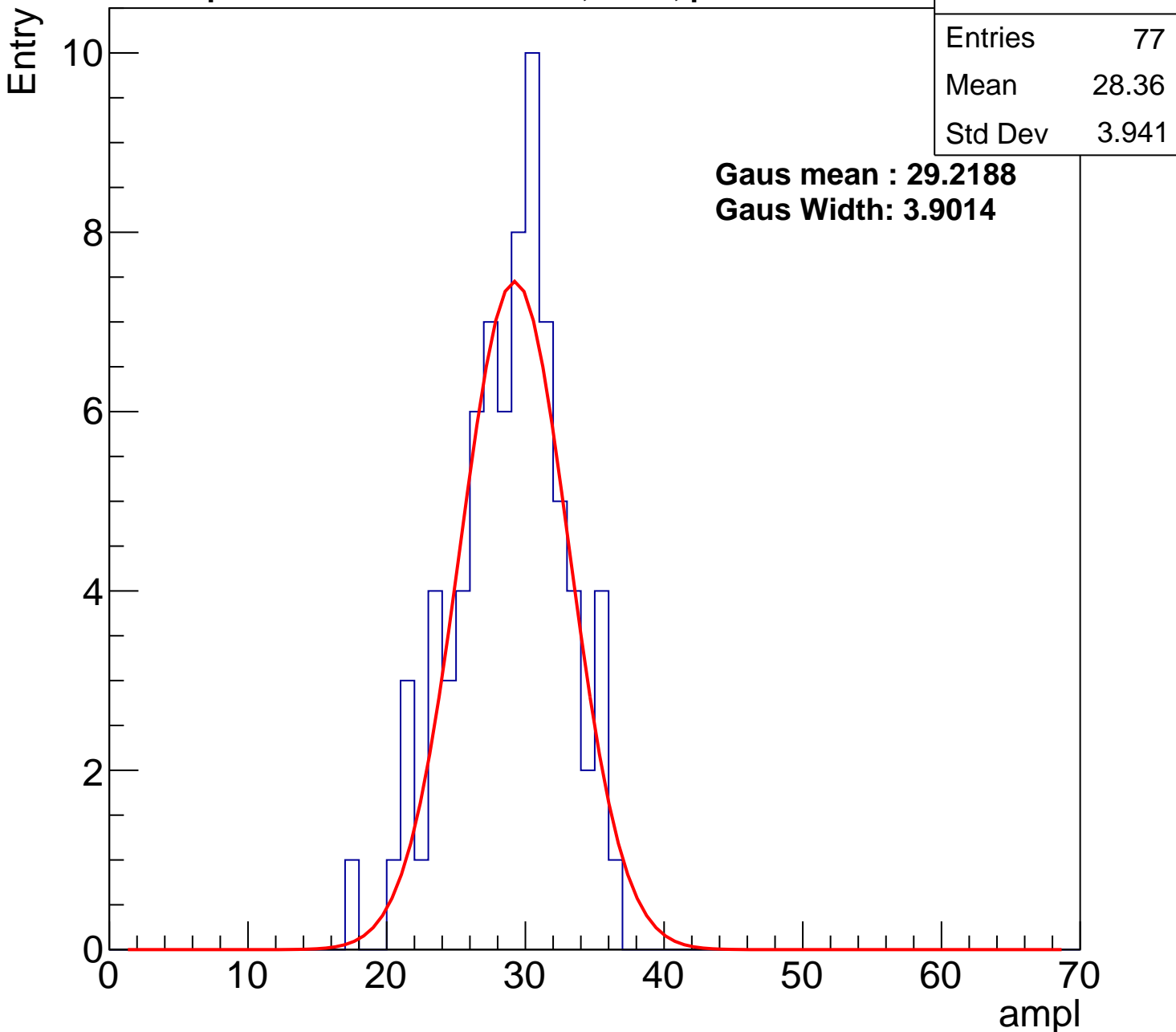
**Gaus Width: 3.9014**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U2-ch110, adc1

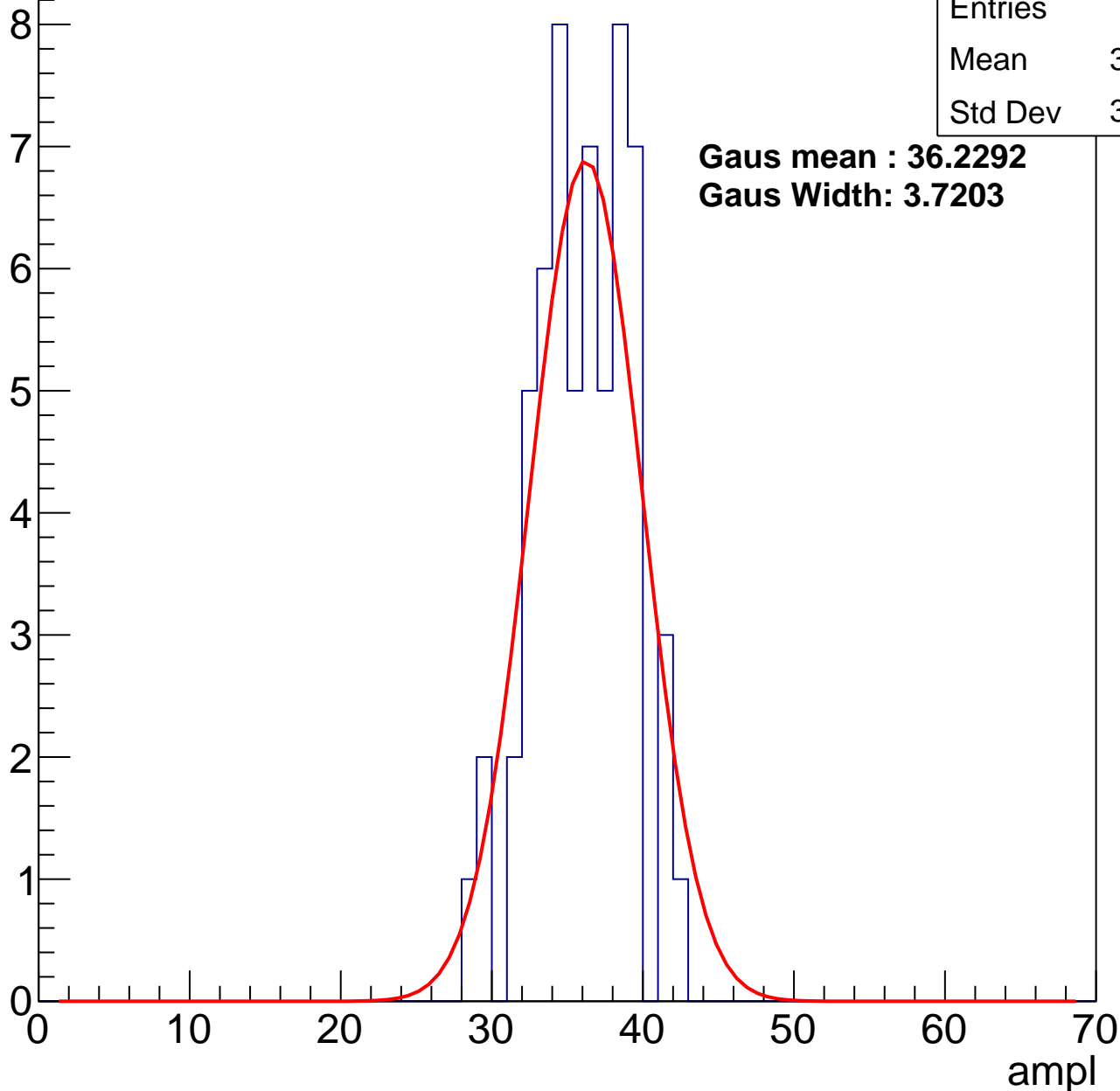
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 60    |
| Mean    | 35.53 |
| Std Dev | 3.112 |

**Gaus mean : 36.2292**

**Gaus Width: 3.7203**



# B0L001S, U2-ch110, adc2

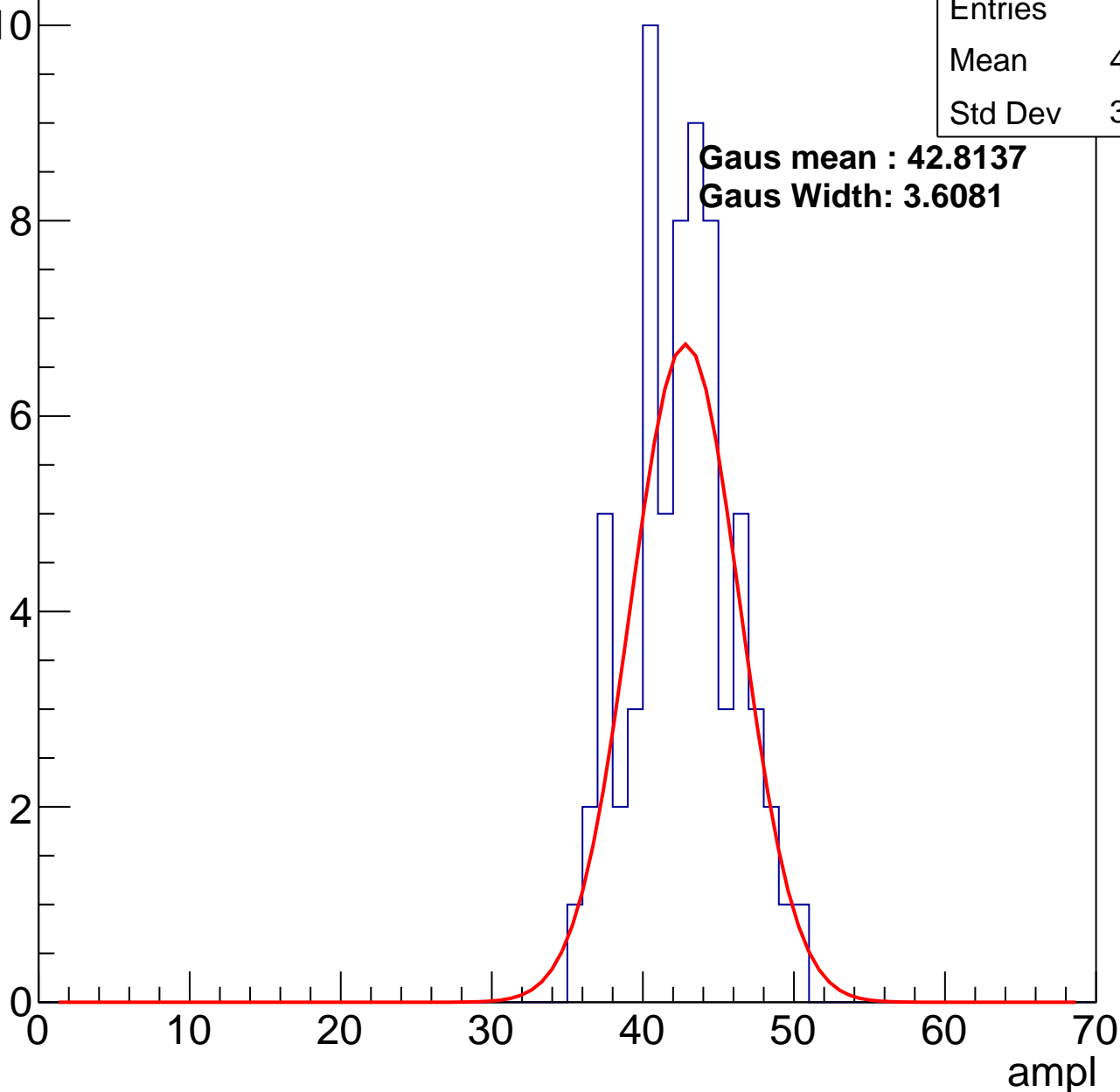
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 68    |
| Mean    | 42.15 |
| Std Dev | 3.335 |

**Gaus mean : 42.8137**

**Gaus Width: 3.6081**

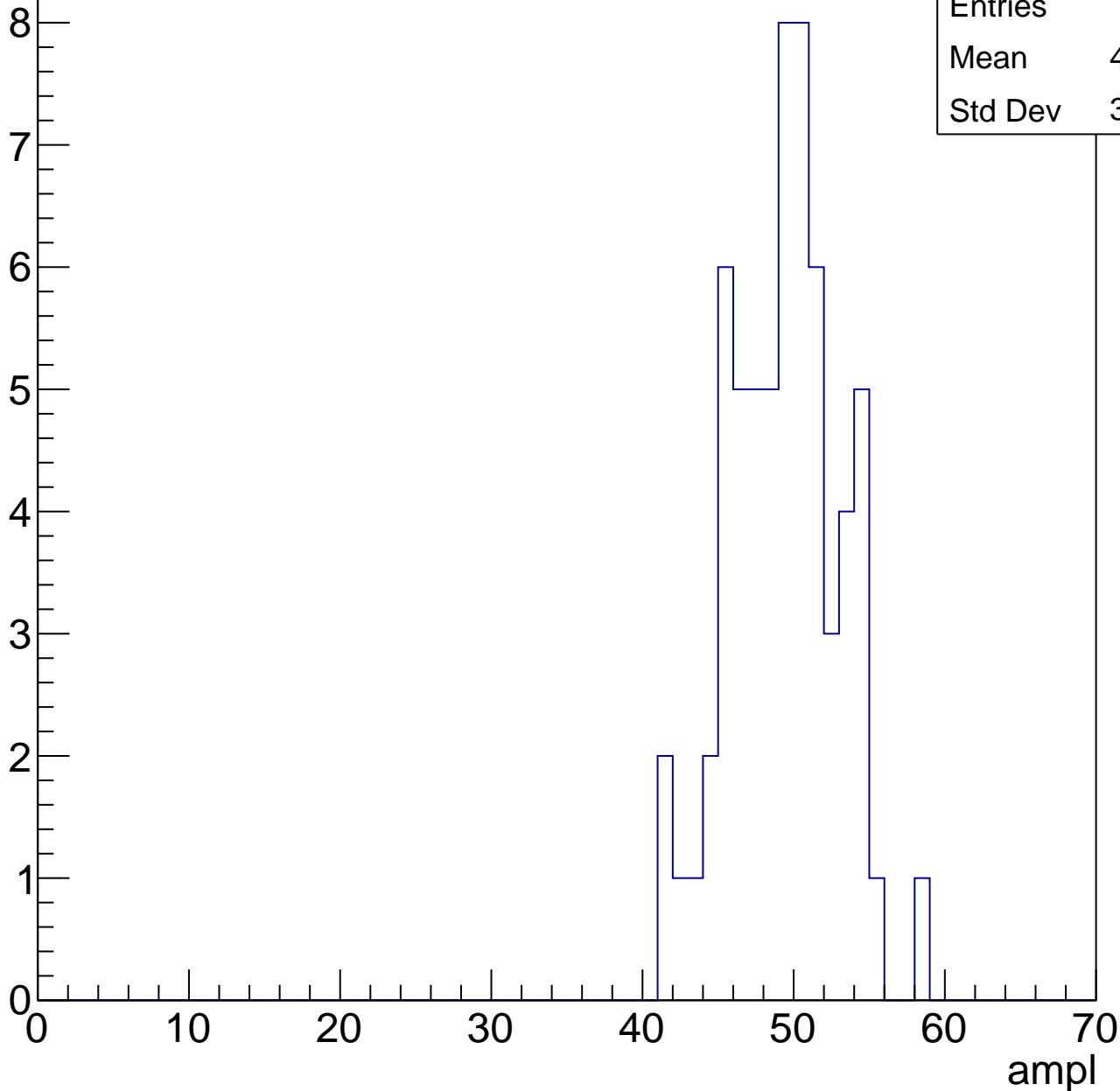


# B0L001S, U2-ch110, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 63    |
| Mean    | 48.87 |
| Std Dev | 3.548 |

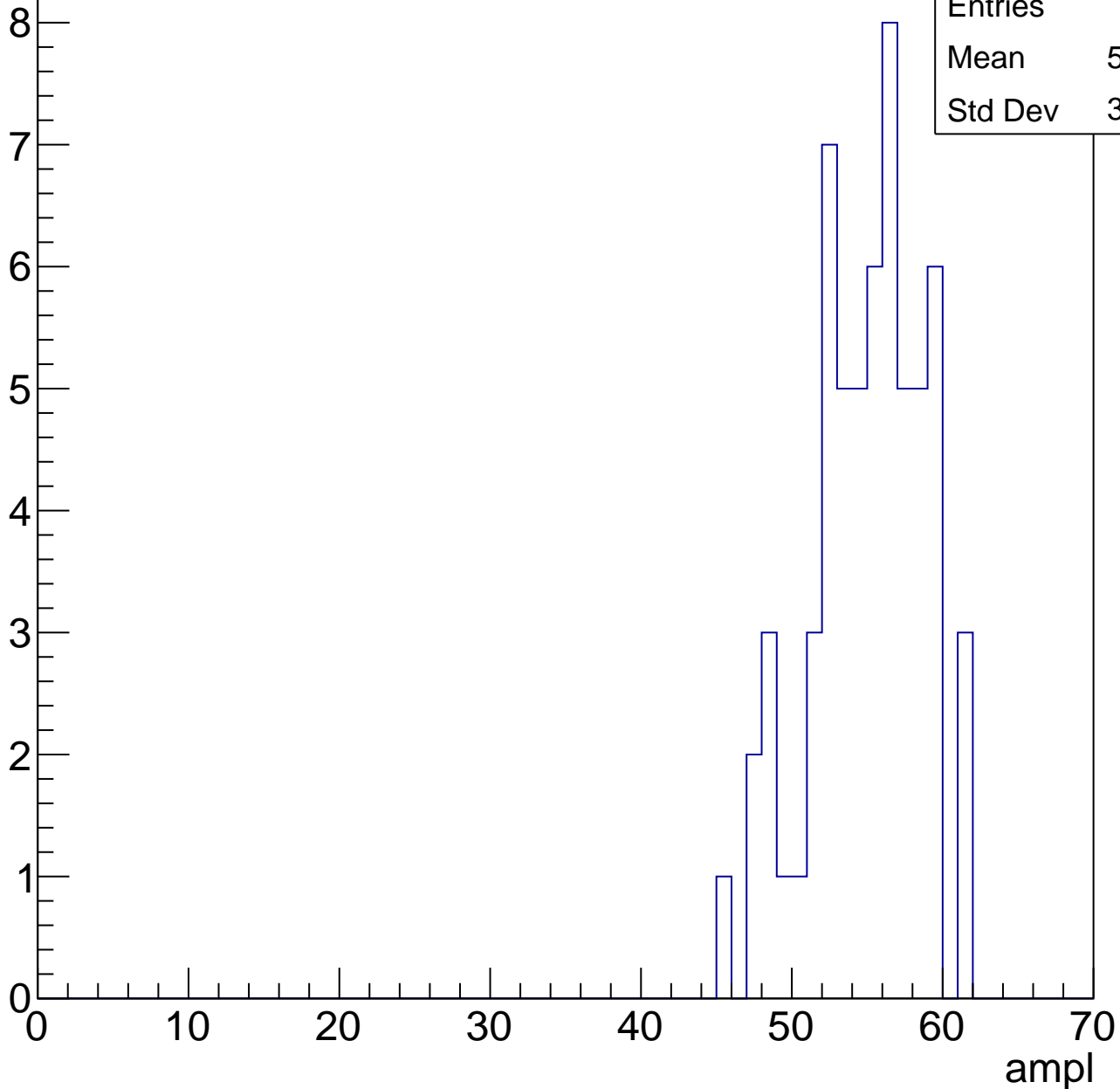


# B0L001S, U2-ch110, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 61    |
| Mean    | 54.49 |
| Std Dev | 3.696 |



# B0L001S, U2-ch110, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

10

Entries 48

Mean 59.4

Std Dev 2.782

8

6

4

2

0

0

10

20

30

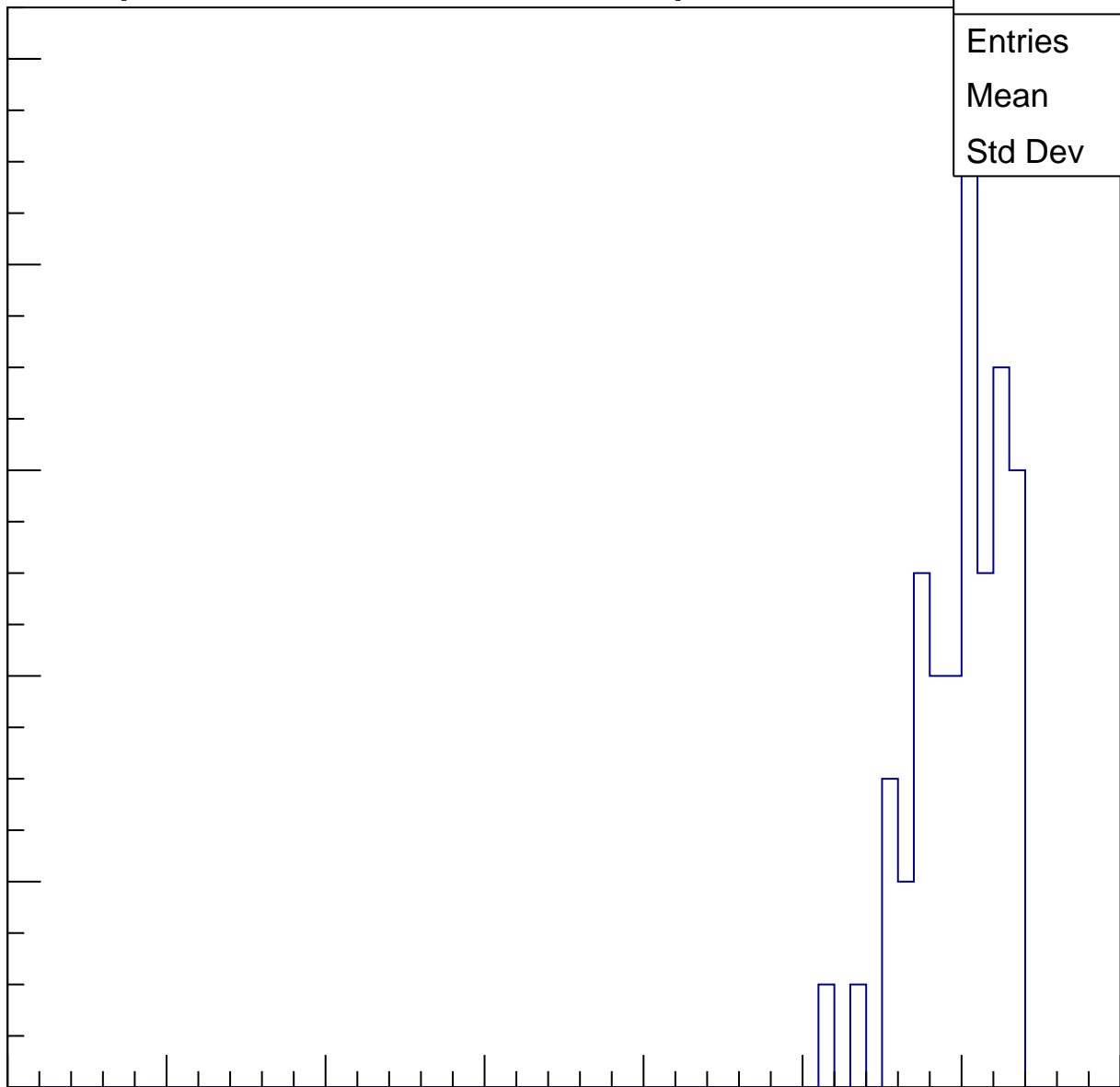
40

50

60

70

ampl



# B0L001S, U2-ch110, adc6

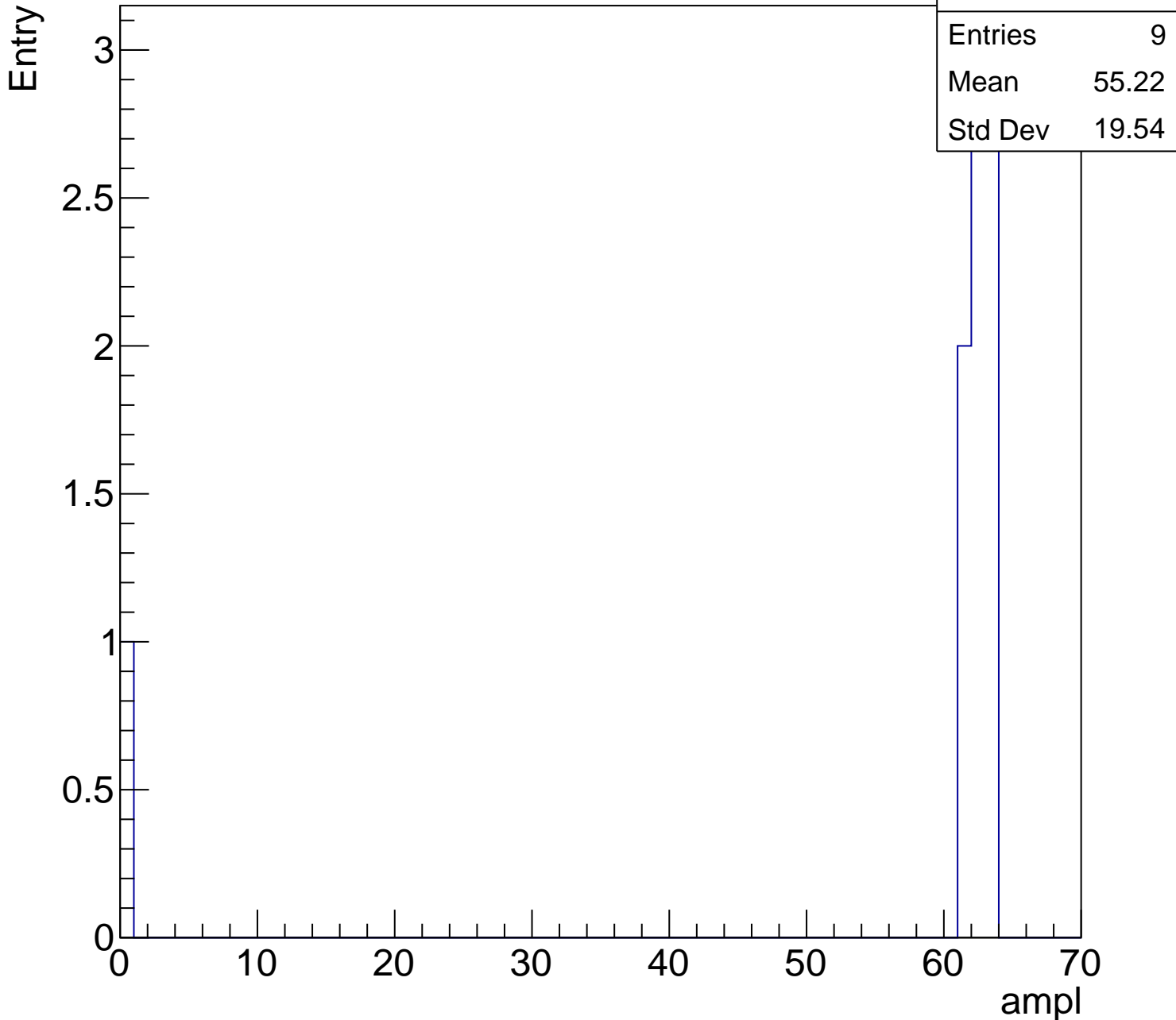
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

3  
2.5  
2  
1.5  
1  
0.5  
0

|         |       |
|---------|-------|
| Entries | 9     |
| Mean    | 55.22 |
| Std Dev | 19.54 |

ampl





# B0L001S, U2-ch110, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U2-ch111, adc0

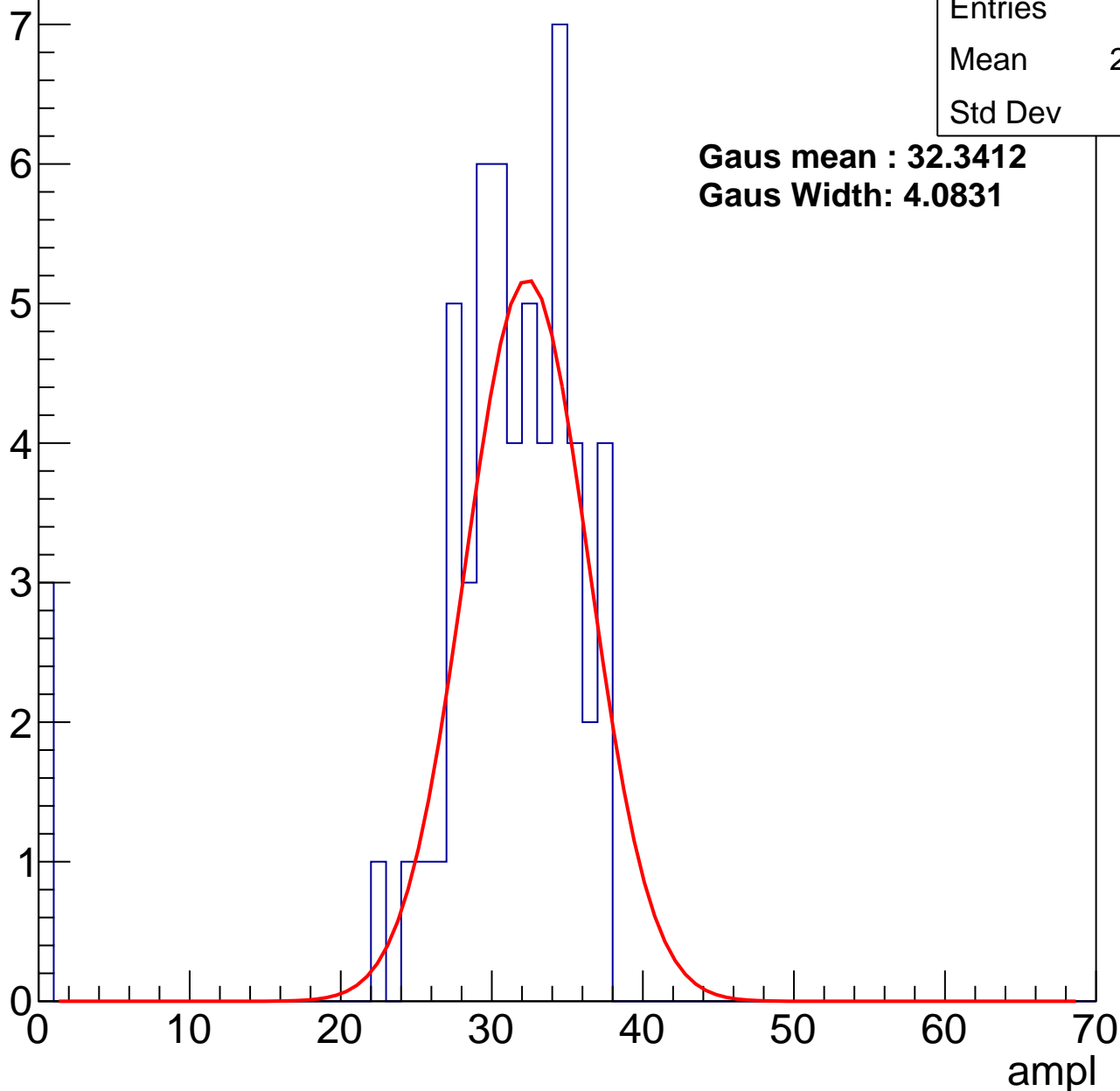
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 57    |
| Mean    | 29.54 |
| Std Dev | 7.76  |

**Gaus mean : 32.3412**

**Gaus Width: 4.0831**



# B0L001S, U2-ch111, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 75    |
| Mean    | 37.43 |
| Std Dev | 5.579 |

**Gaus mean : 38.2529**

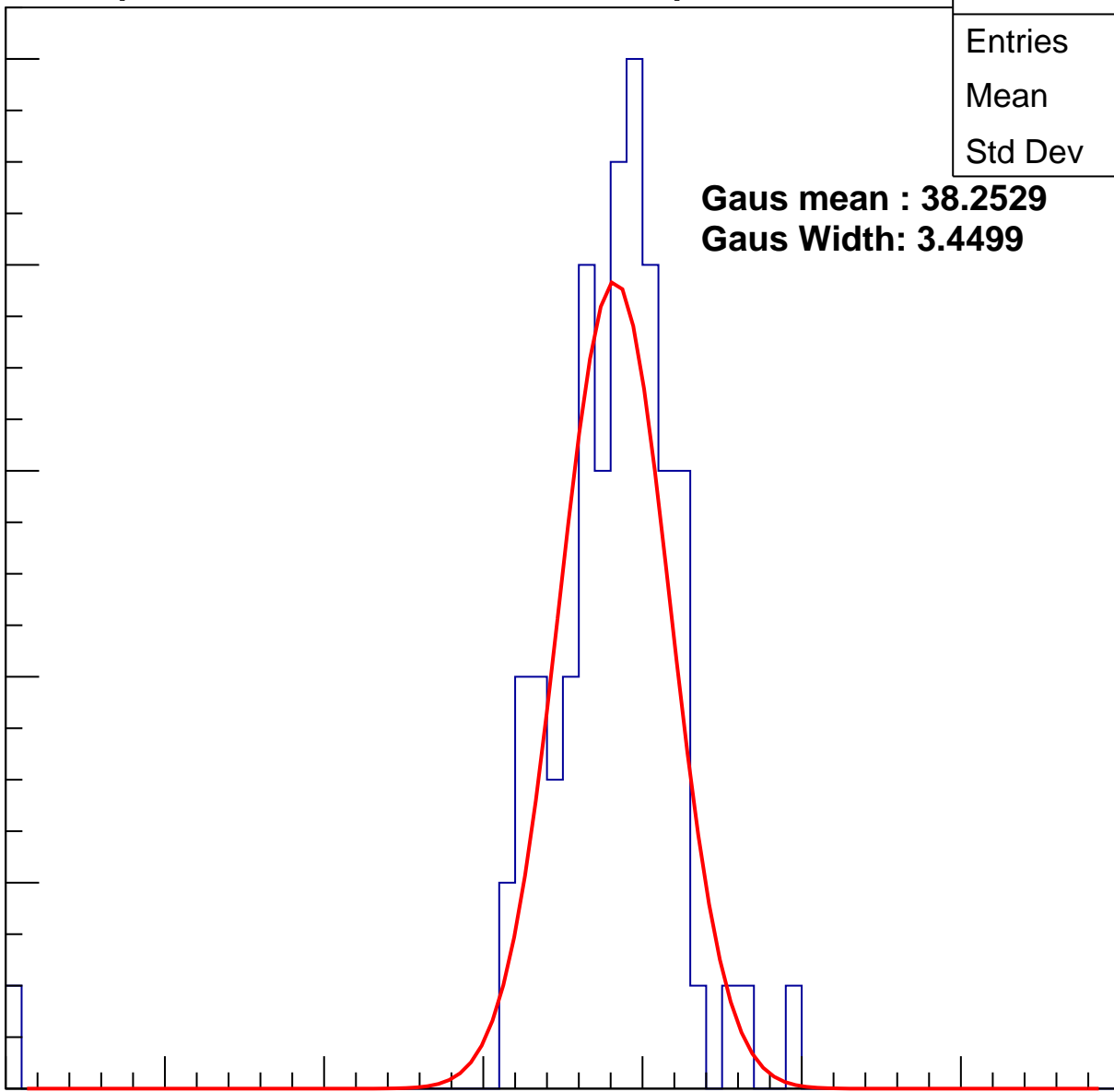
**Gaus Width: 3.4499**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B0L001S, U2-ch111, adc2

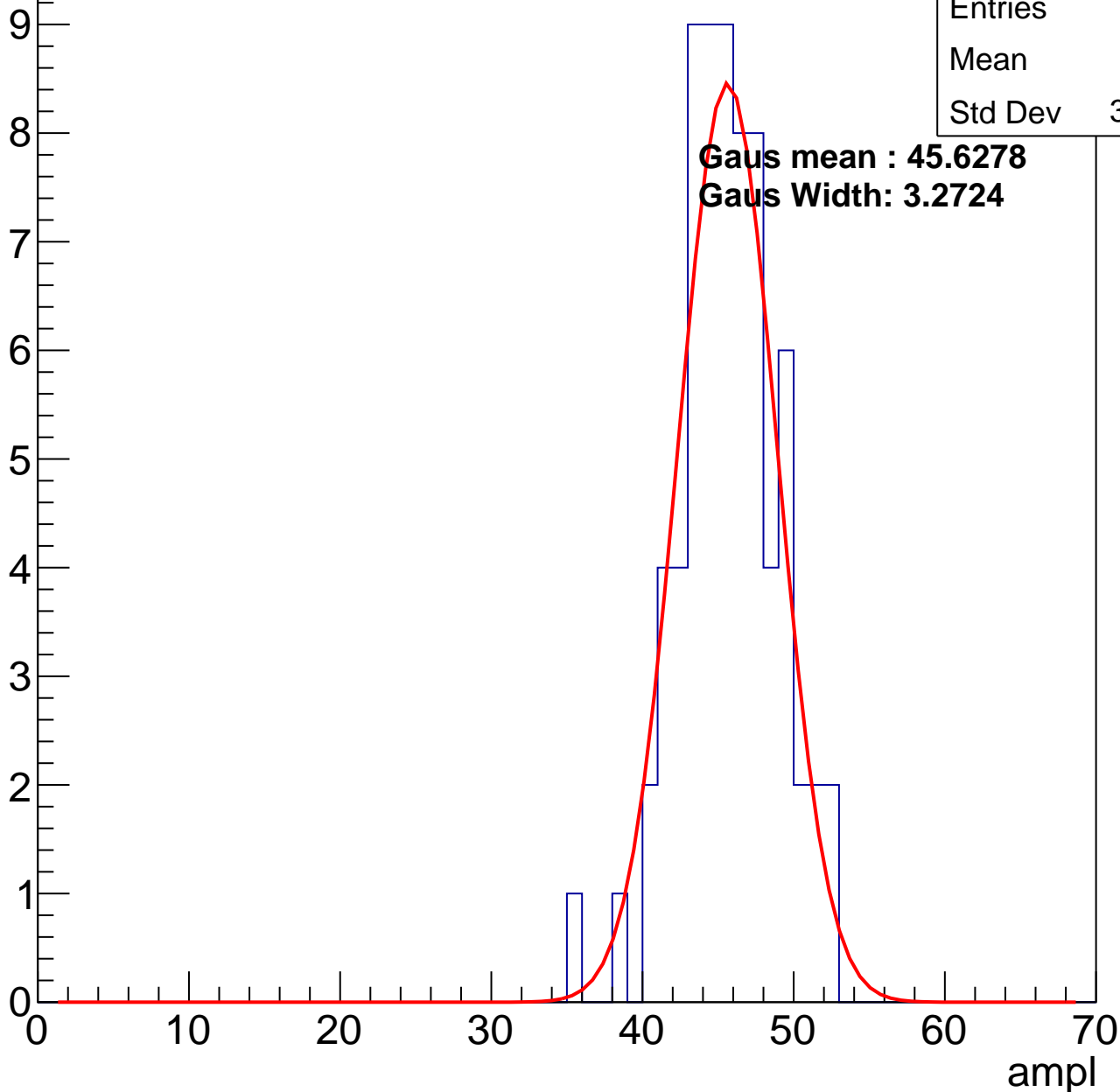
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 71    |
| Mean    | 45.2  |
| Std Dev | 3.214 |

**Gaus mean : 45.6278**

**Gaus Width: 3.2724**

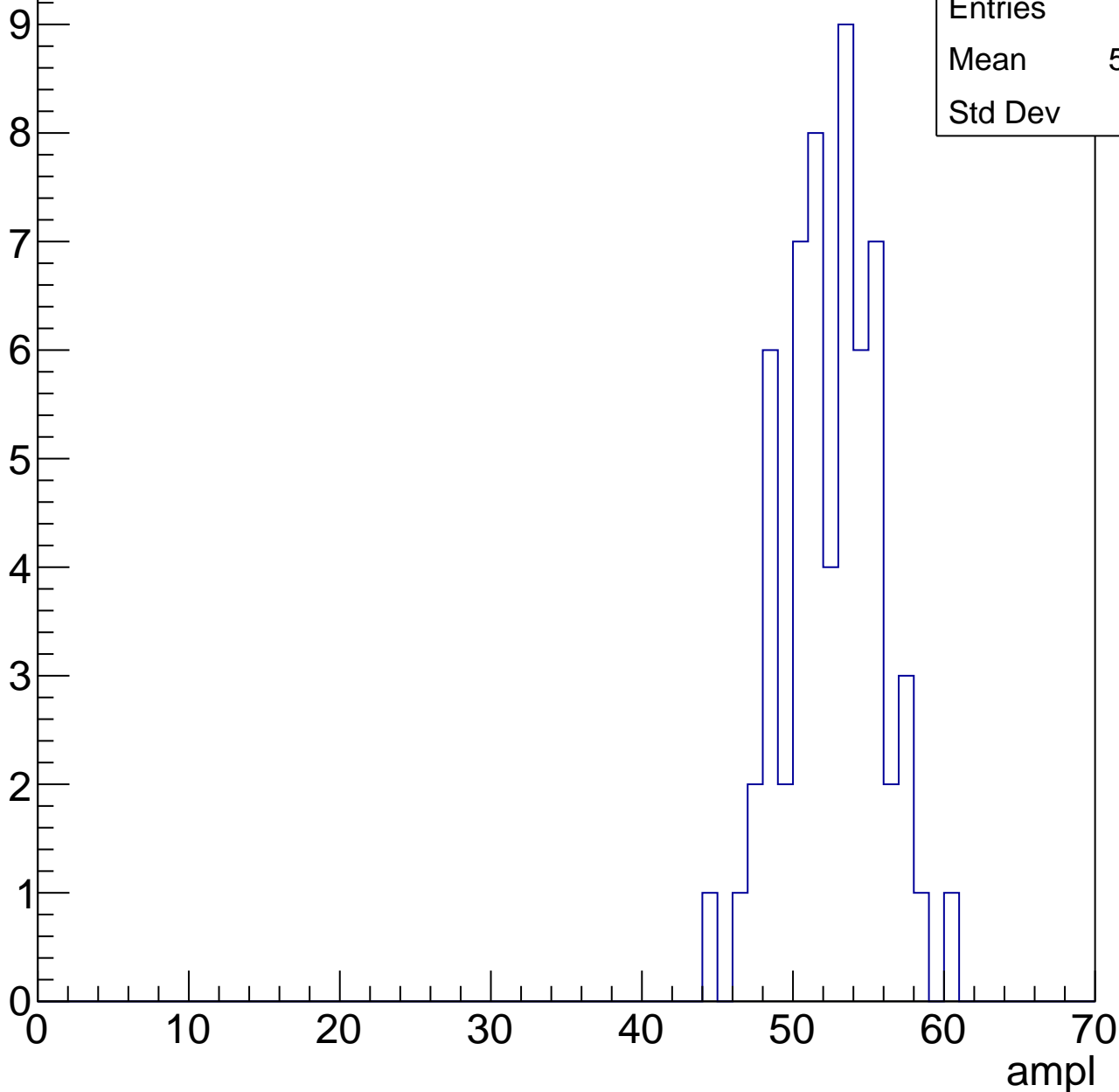


# B0L001S, U2-ch111, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 60    |
| Mean    | 52.05 |
| Std Dev | 3.17  |

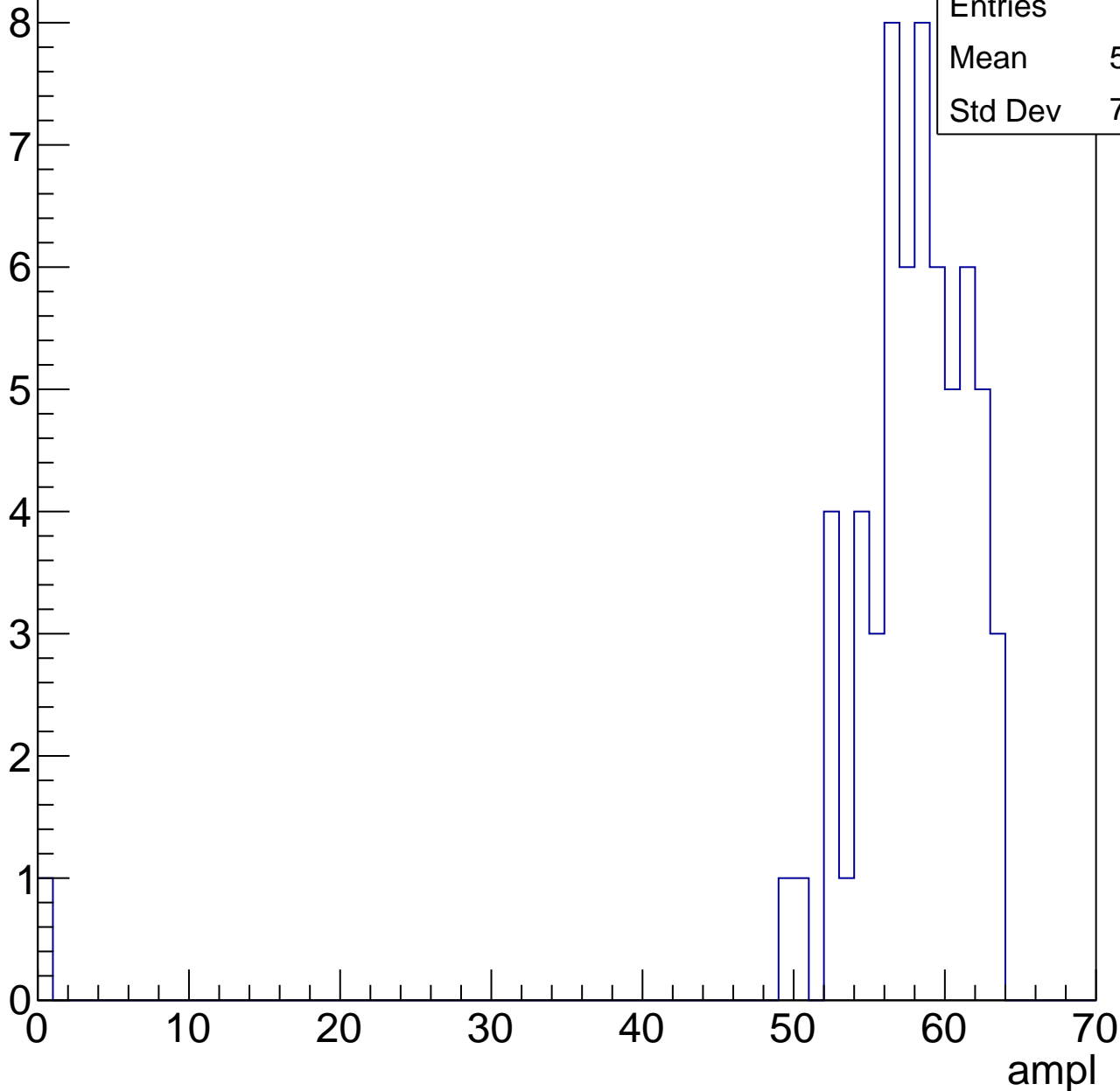


# B0L001S, U2-ch111, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 62    |
| Mean    | 56.68 |
| Std Dev | 7.965 |

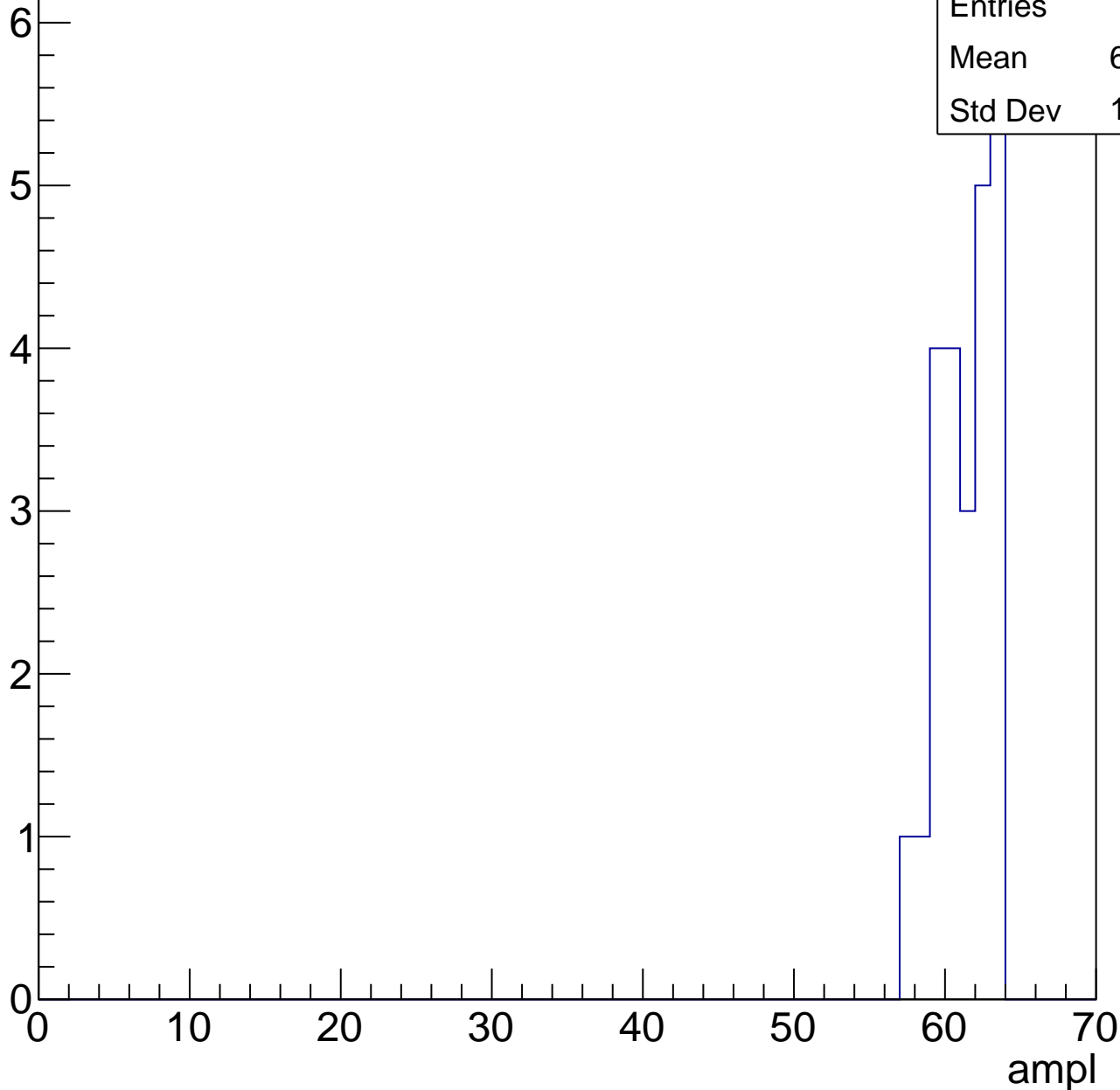


# B0L001S, U2-ch111, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 24    |
| Mean    | 60.92 |
| Std Dev | 1.754 |



# B0L001S, U2-ch111, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch111, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 1 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch112, adc0

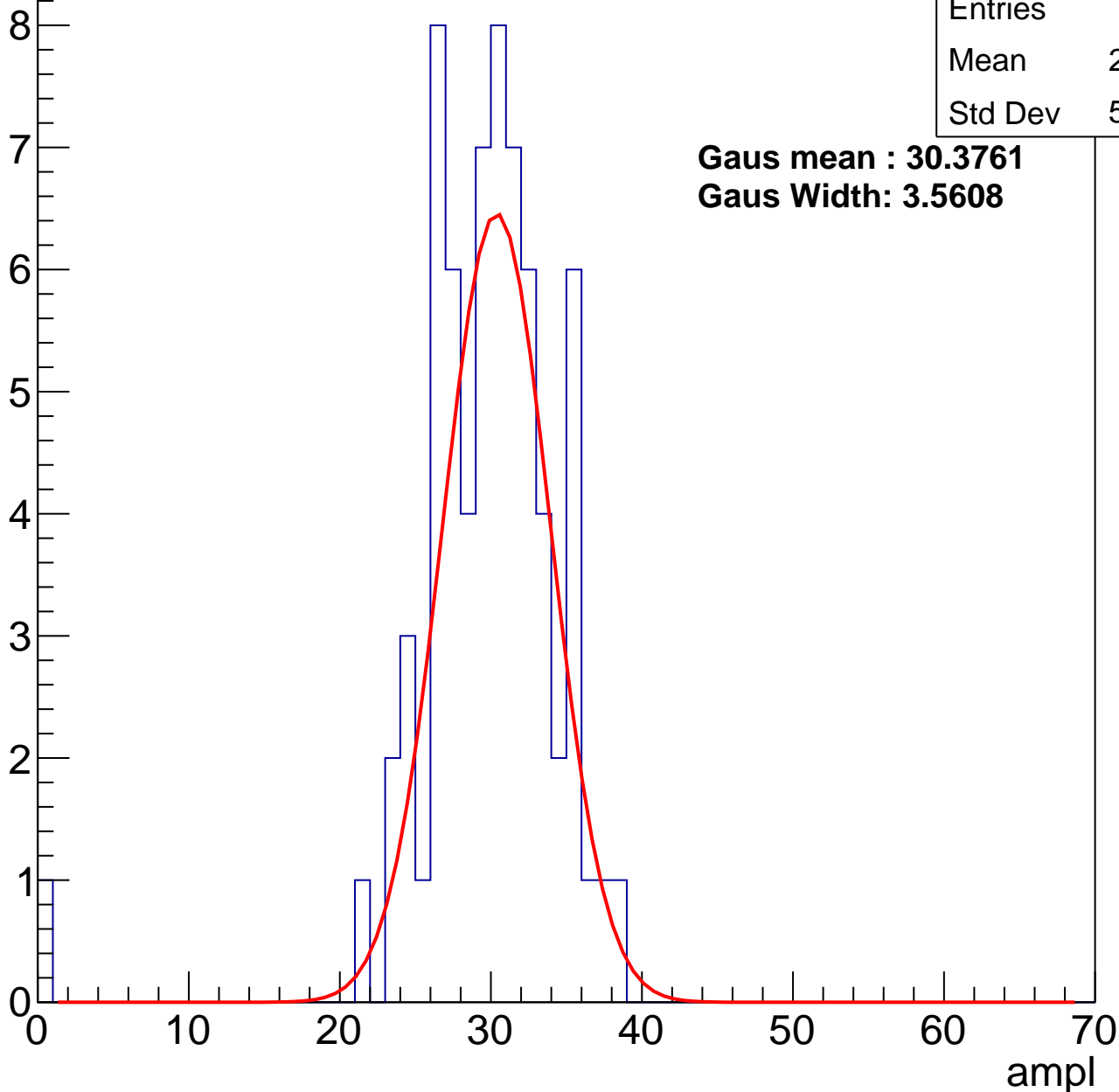
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 69    |
| Mean    | 29.26 |
| Std Dev | 5.075 |

**Gaus mean : 30.3761**

**Gaus Width: 3.5608**



# B0L001S, U2-ch112, adc1

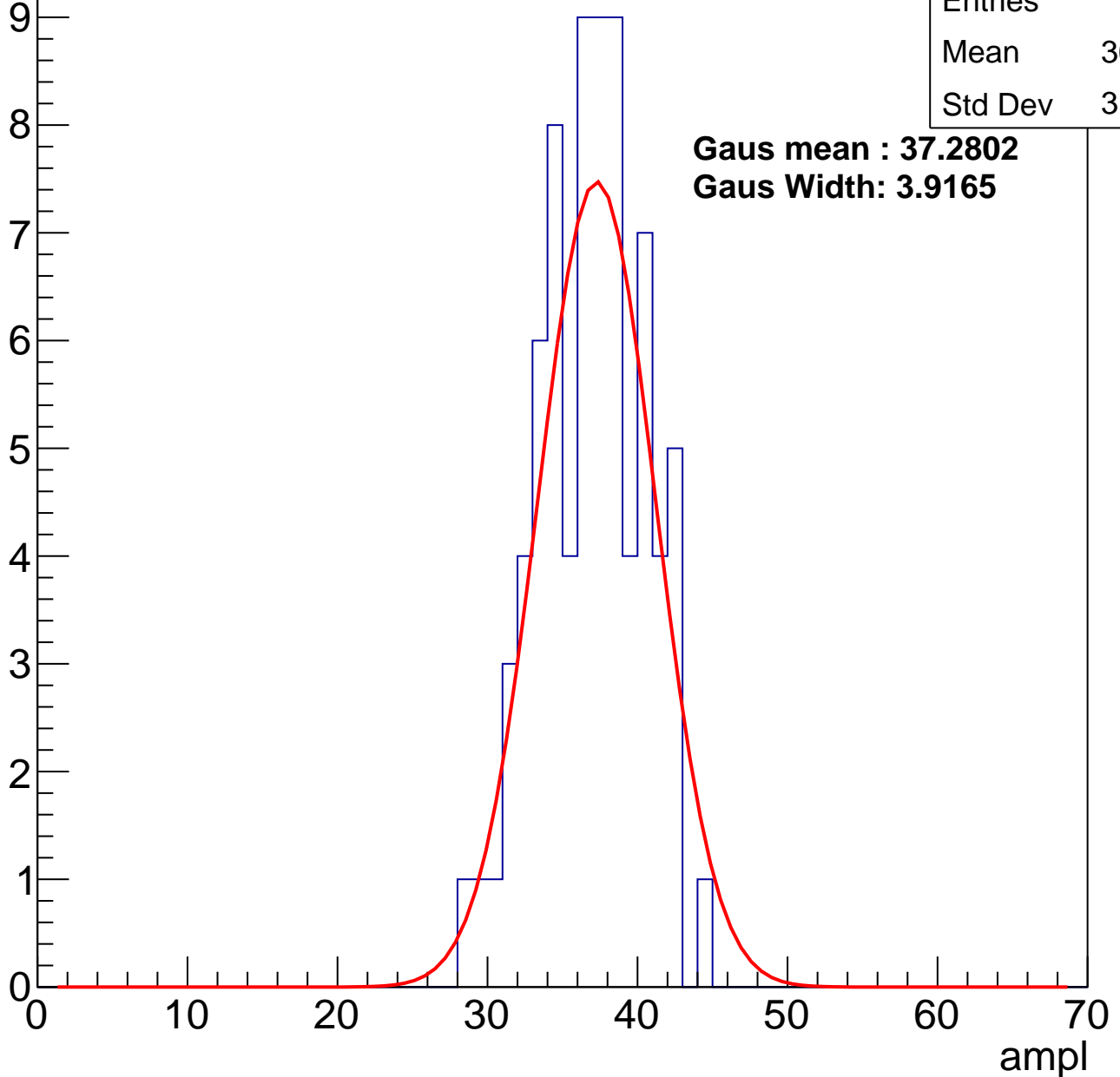
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 76    |
| Mean    | 36.46 |
| Std Dev | 3.439 |

**Gaus mean : 37.2802**

**Gaus Width: 3.9165**



# B0L001S, U2-ch112, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 64    |
| Mean    | 43.97 |
| Std Dev | 2.979 |

**Gaus mean : 43.3406**

**Gaus Width: 3.4819**

Entry

10

8

6

4

2

0

0

10

20

30

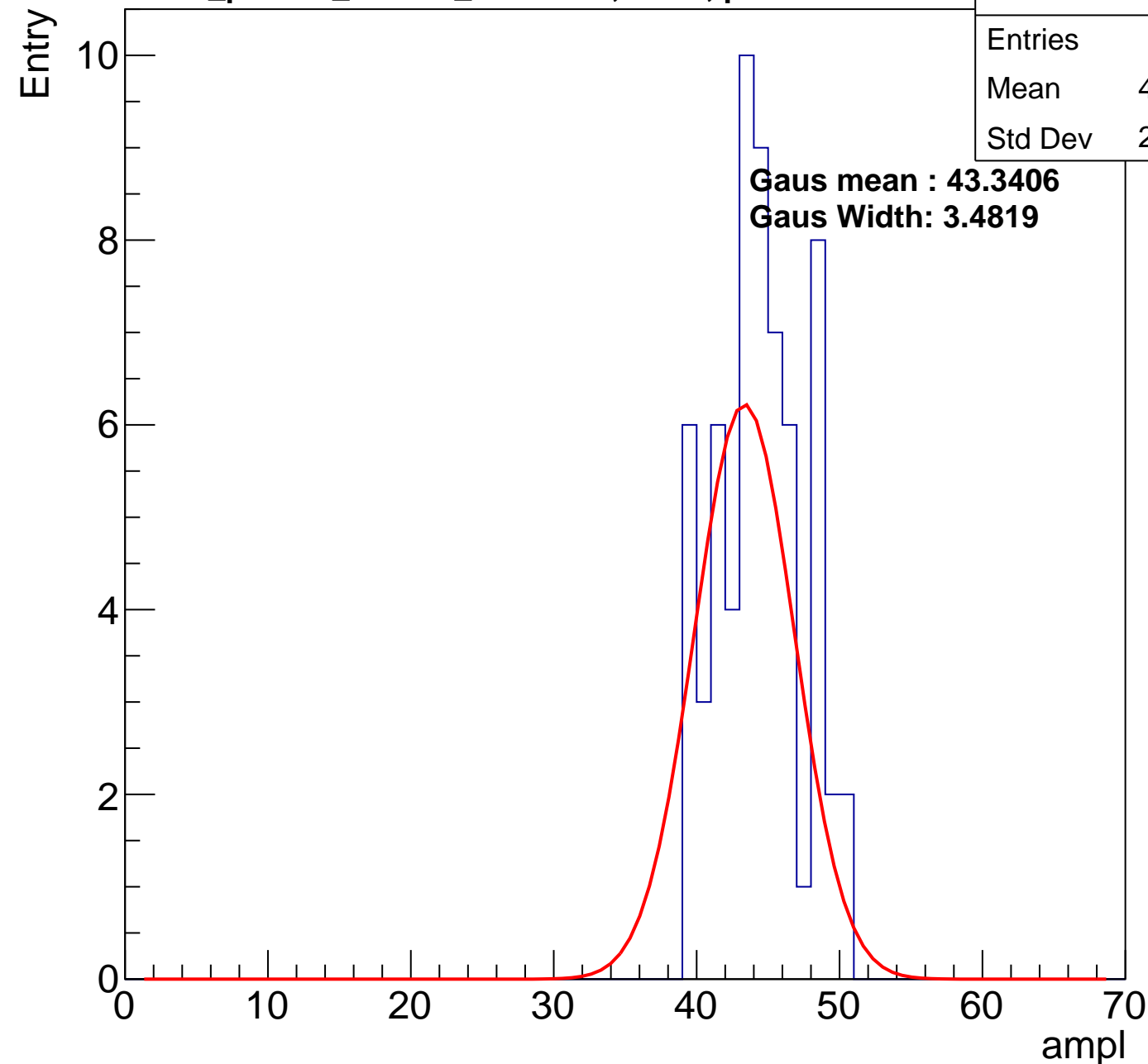
40

50

60

70

ampl

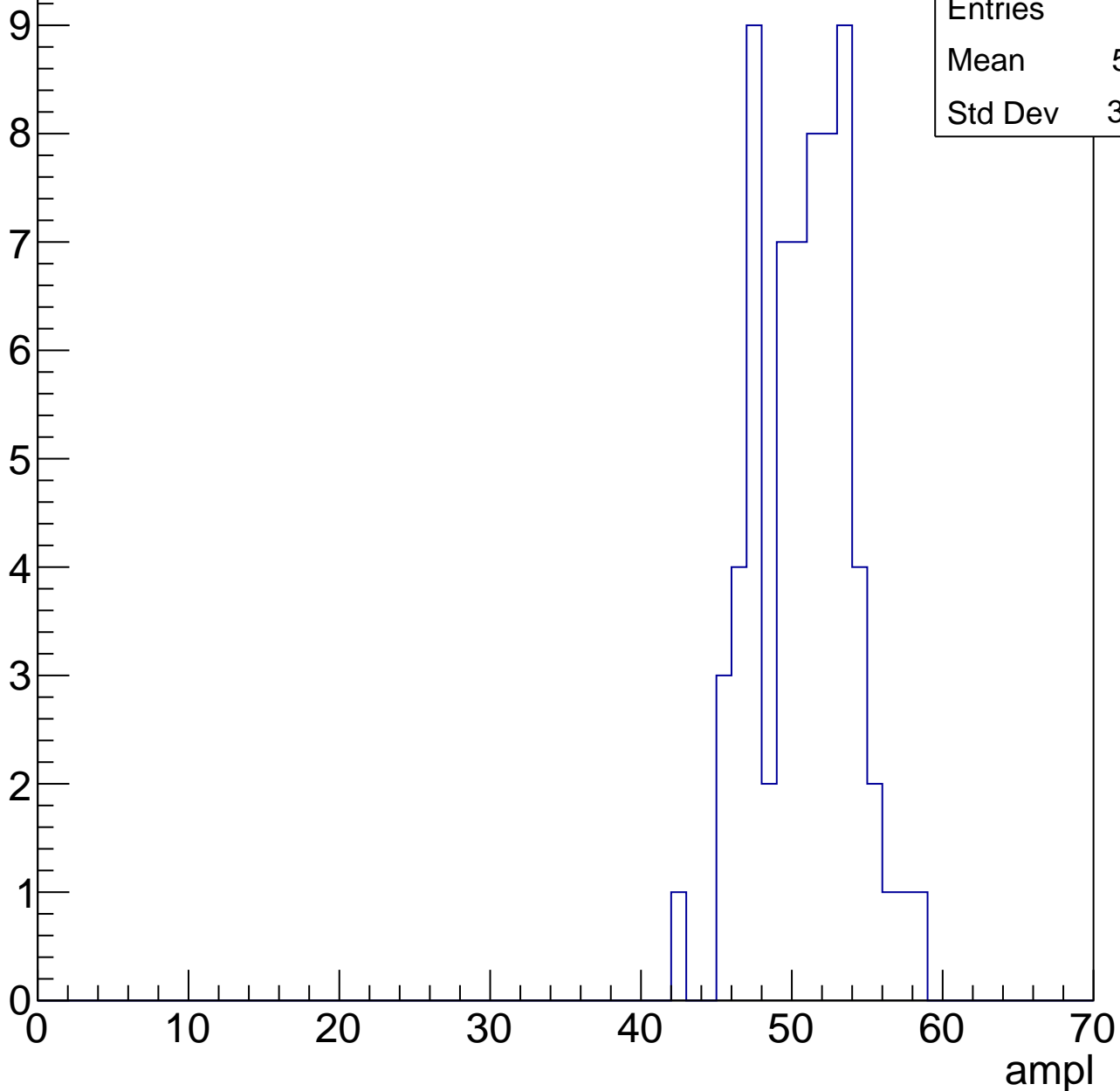


# B0L001S, U2-ch112, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 67    |
| Mean    | 50.31 |
| Std Dev | 3.177 |

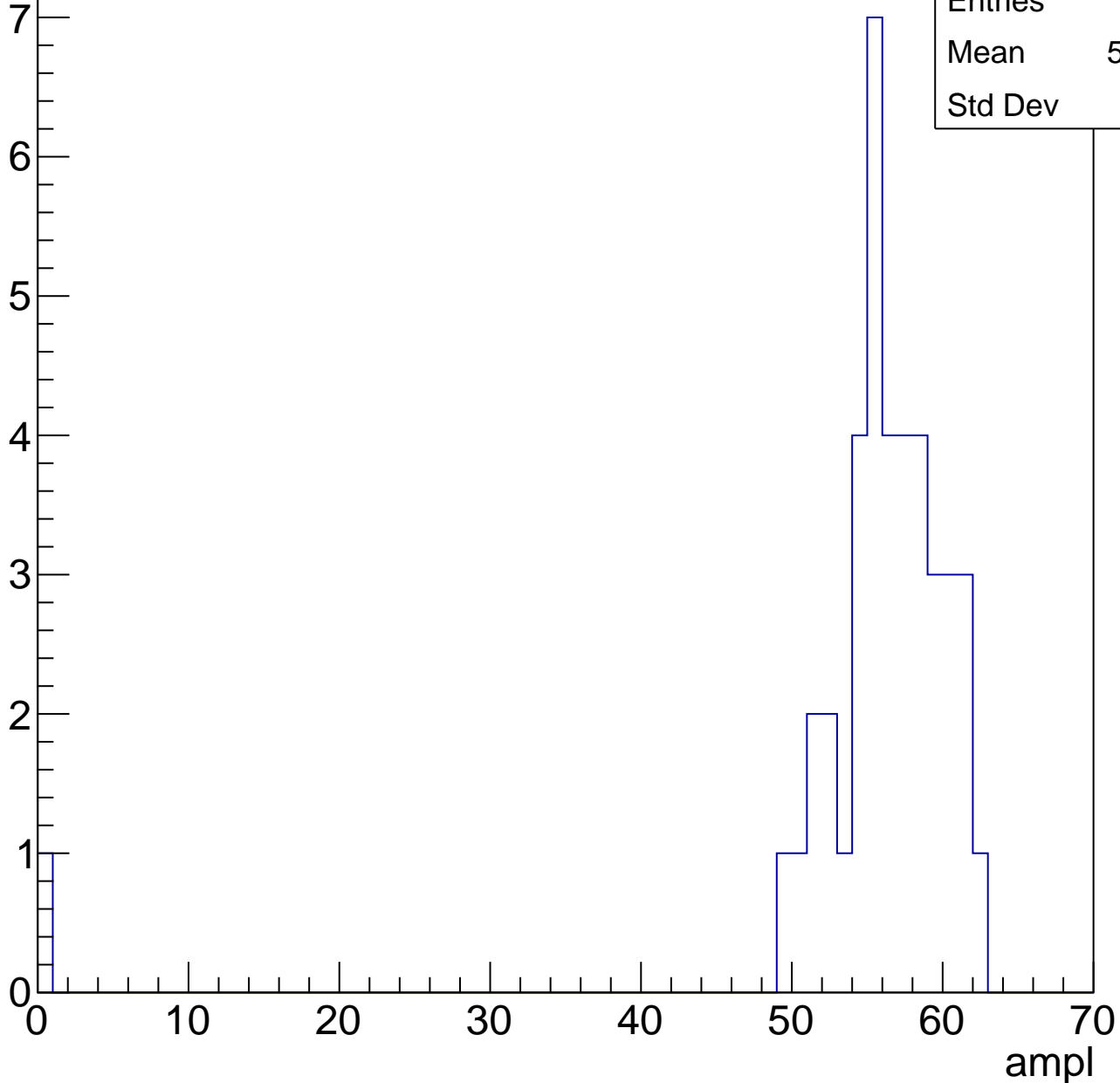


# B0L001S, U2-ch112, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 41    |
| Mean    | 54.76 |
| Std Dev | 9.21  |



# B0L001S, U2-ch112, adc5

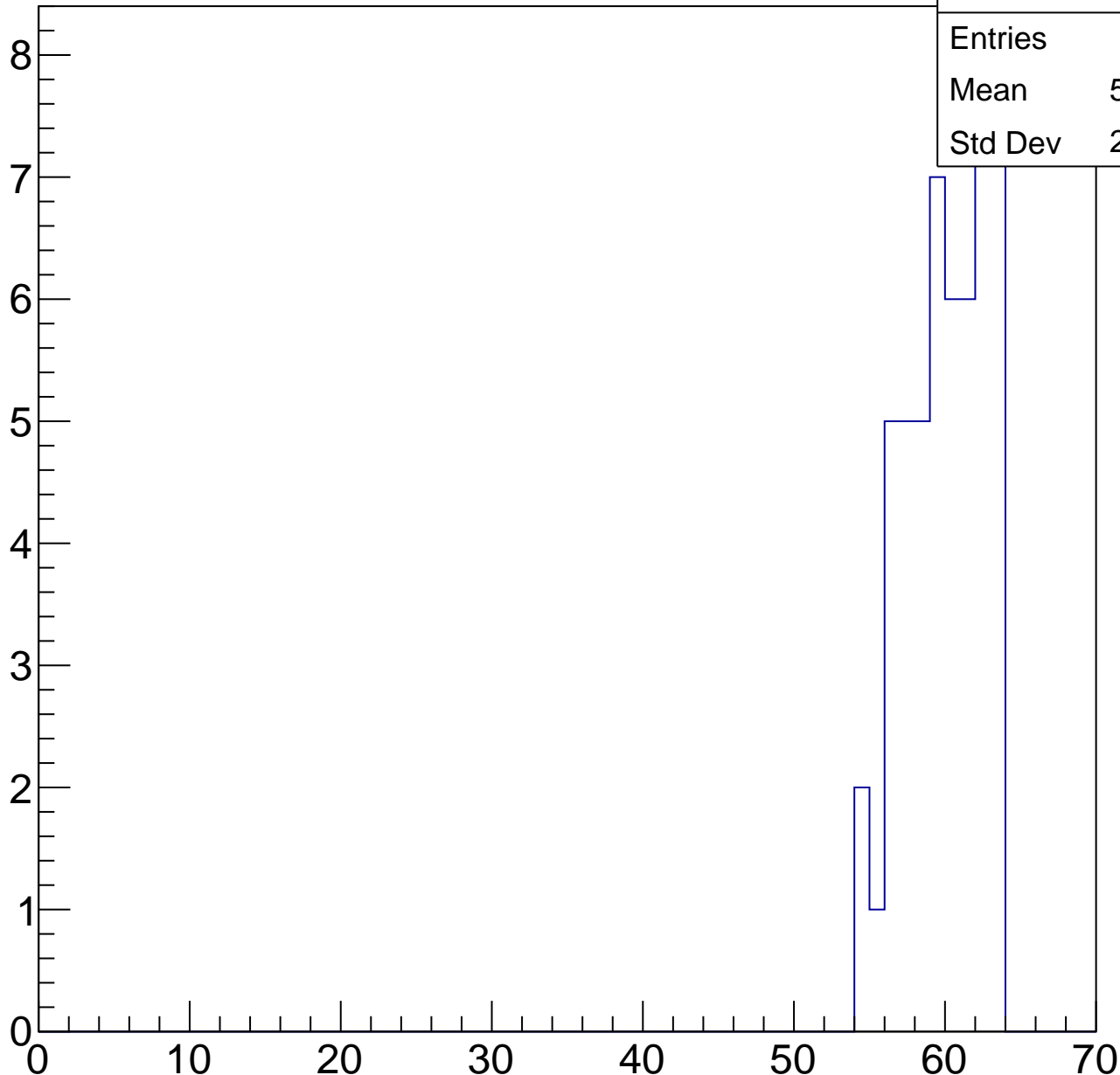
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

|         |       |
|---------|-------|
| Entries | 53    |
| Mean    | 59.57 |
| Std Dev | 2.566 |

ampl



# B0L001S, U2-ch112, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch112, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 1 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch113, adc0

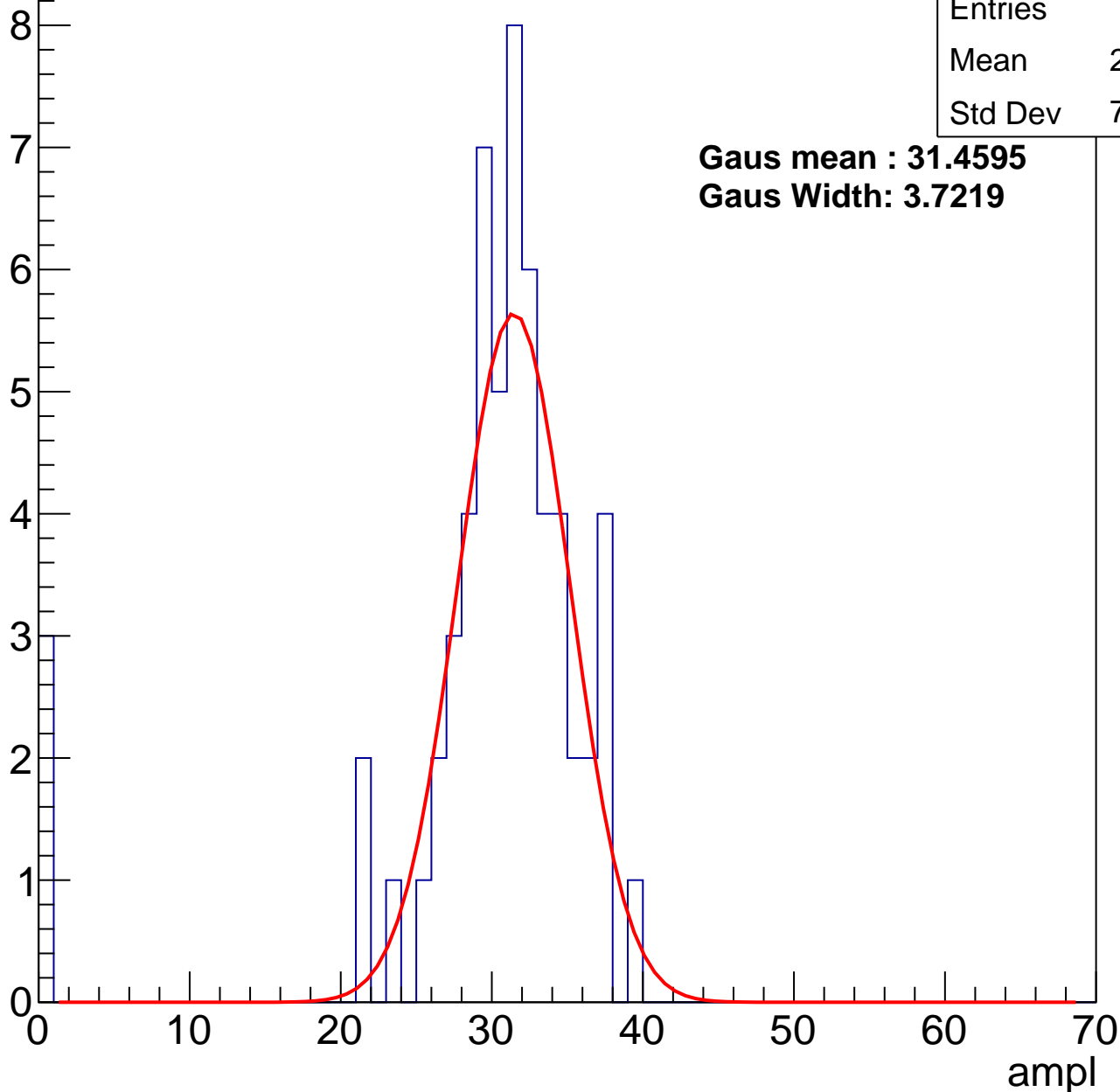
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 59    |
| Mean    | 29.24 |
| Std Dev | 7.718 |

**Gaus mean : 31.4595**

**Gaus Width: 3.7219**



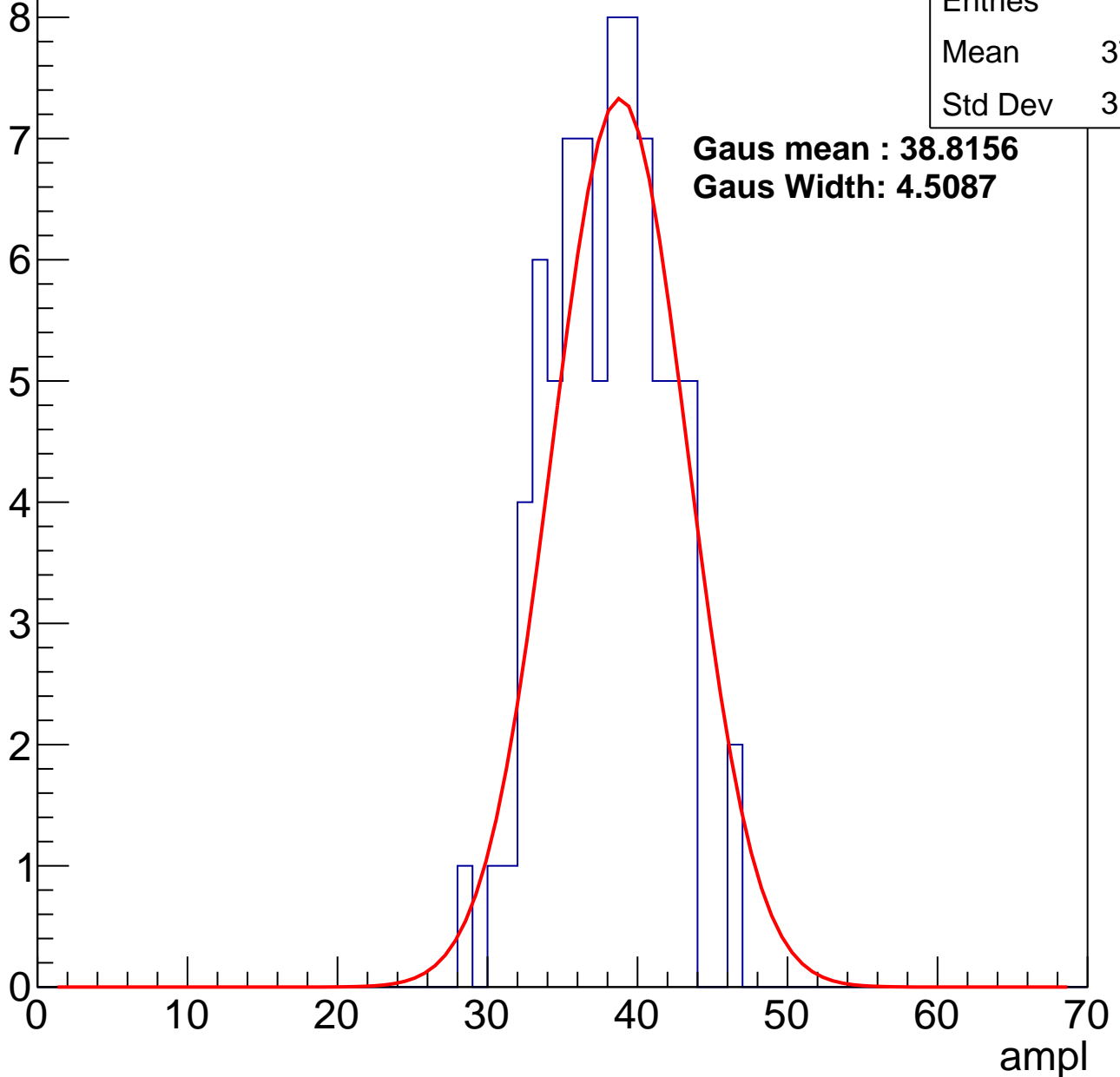
# B0L001S, U2-ch113, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 77    |
| Mean    | 37.47 |
| Std Dev | 3.737 |

**Gaus mean : 38.8156**  
**Gaus Width: 4.5087**



# B0L001S, U2-ch113, adc2

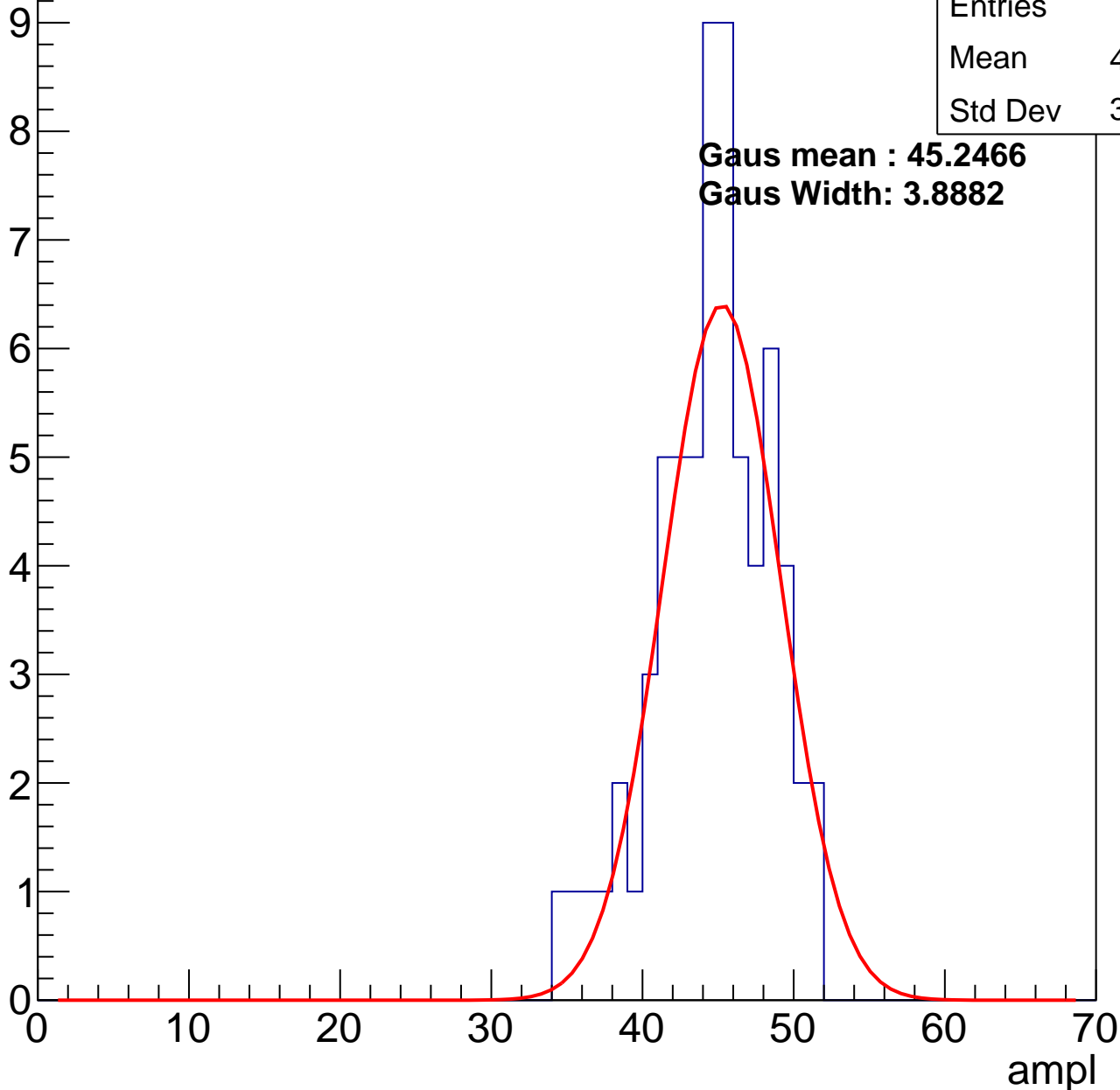
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 66    |
| Mean    | 44.12 |
| Std Dev | 3.772 |

**Gaus mean : 45.2466**

**Gaus Width: 3.8882**

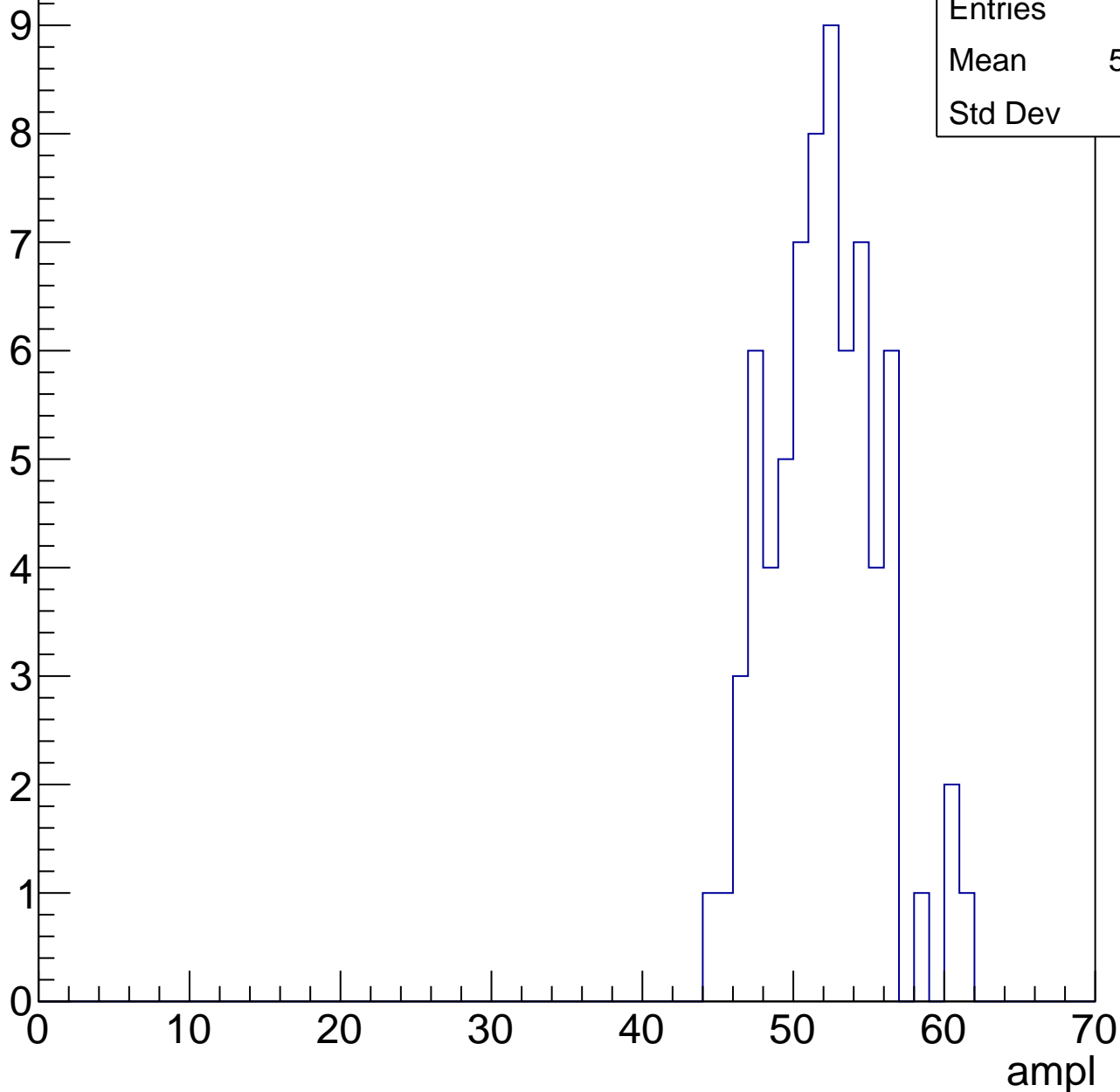


# B0L001S, U2-ch113, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 71    |
| Mean    | 51.59 |
| Std Dev | 3.59  |



# B0L001S, U2-ch113, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

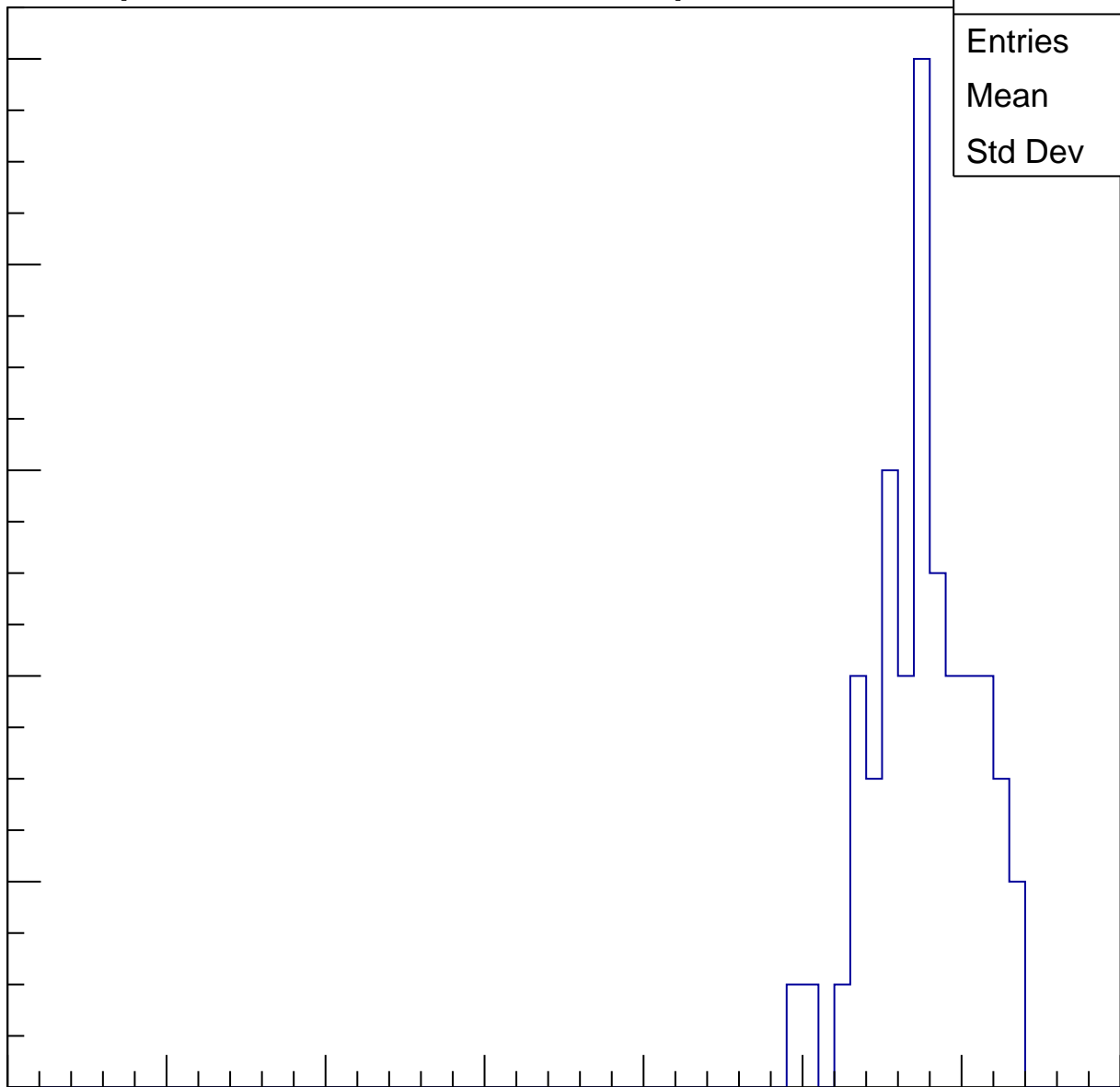
|         |       |
|---------|-------|
| Entries | 52    |
| Mean    | 57.13 |
| Std Dev | 3.175 |

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

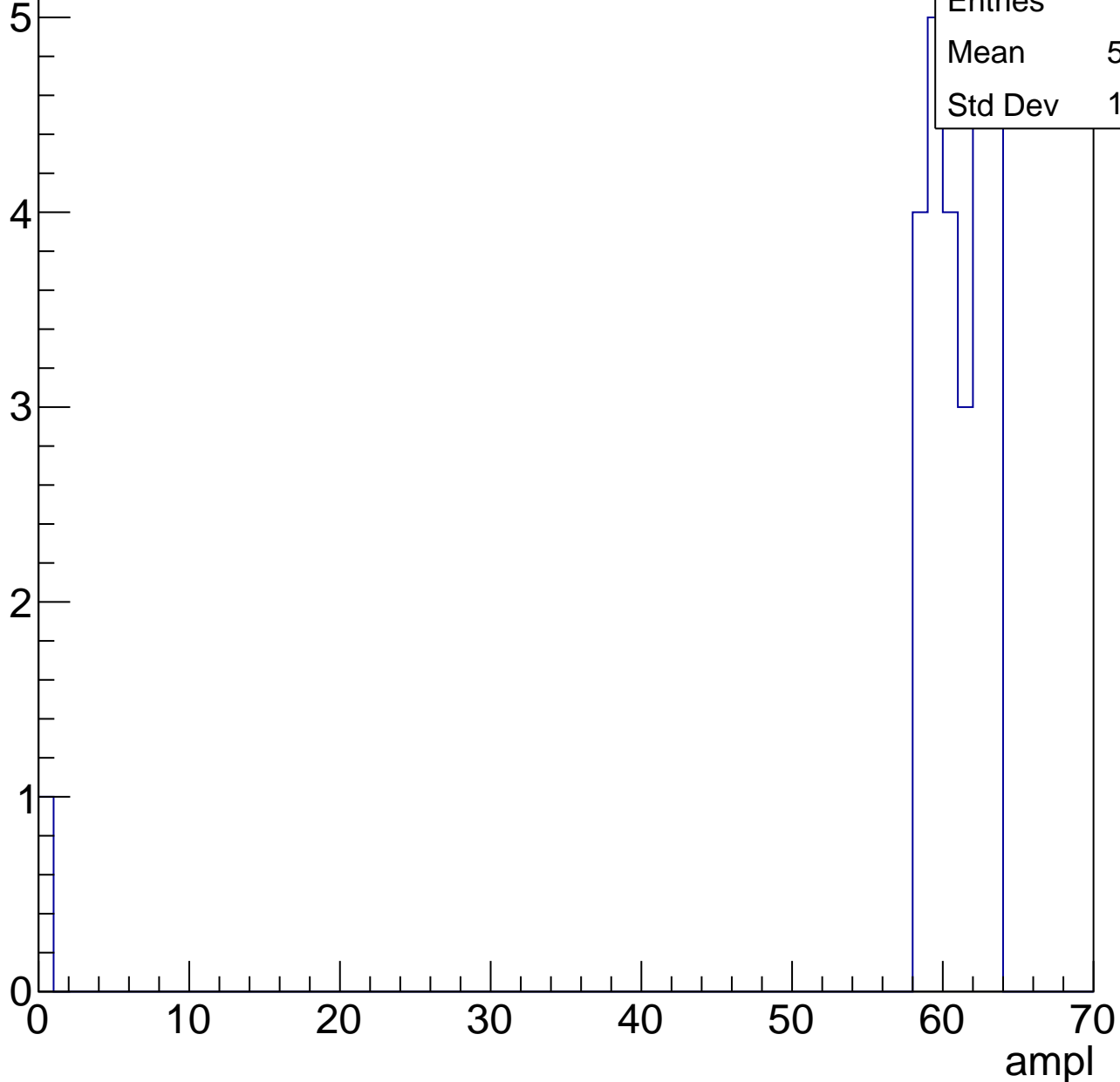
ampl



# B0L001S, U2-ch113, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

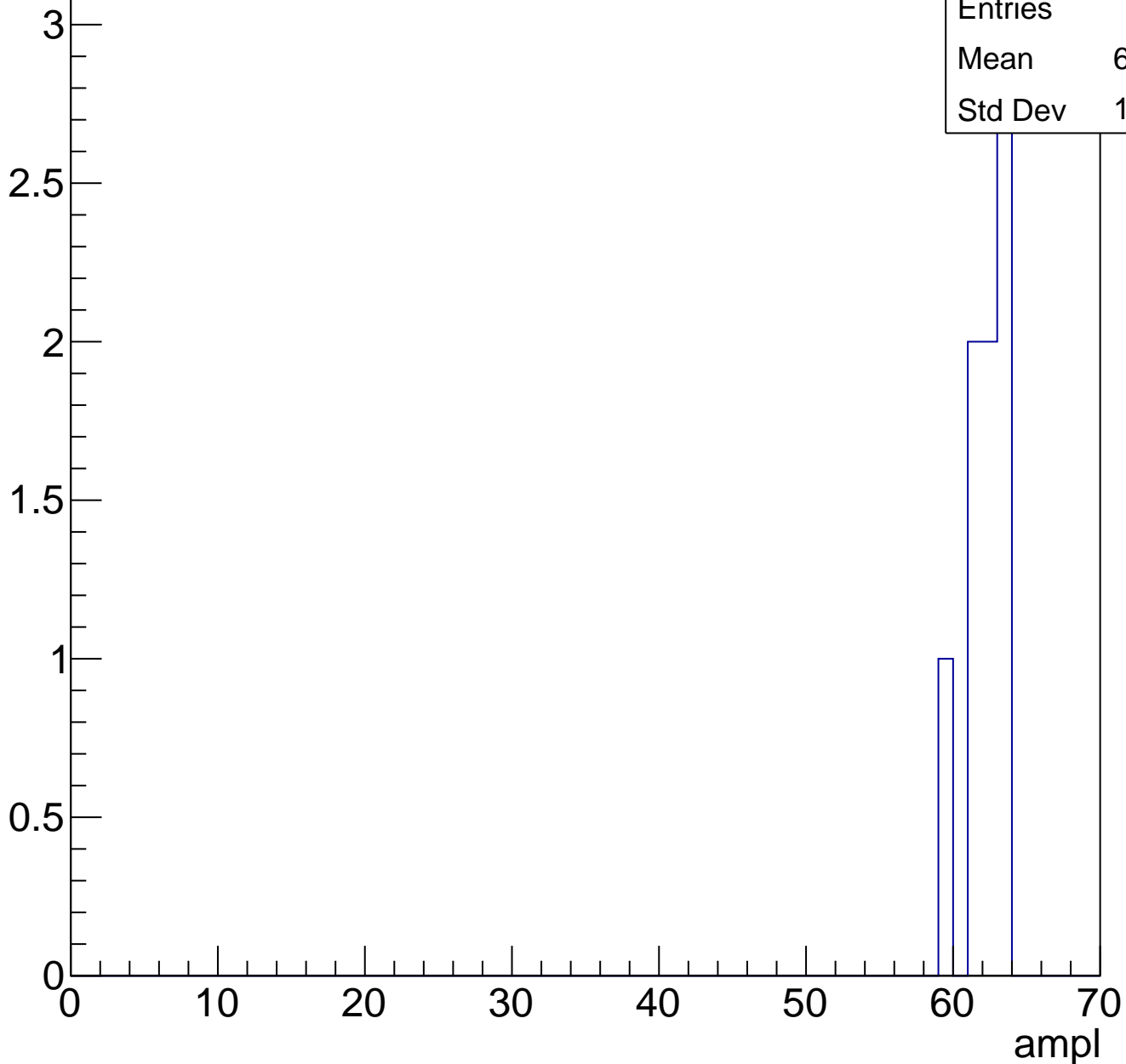
Entry



# B0L001S, U2-ch113, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch113, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 2 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch114, adc0

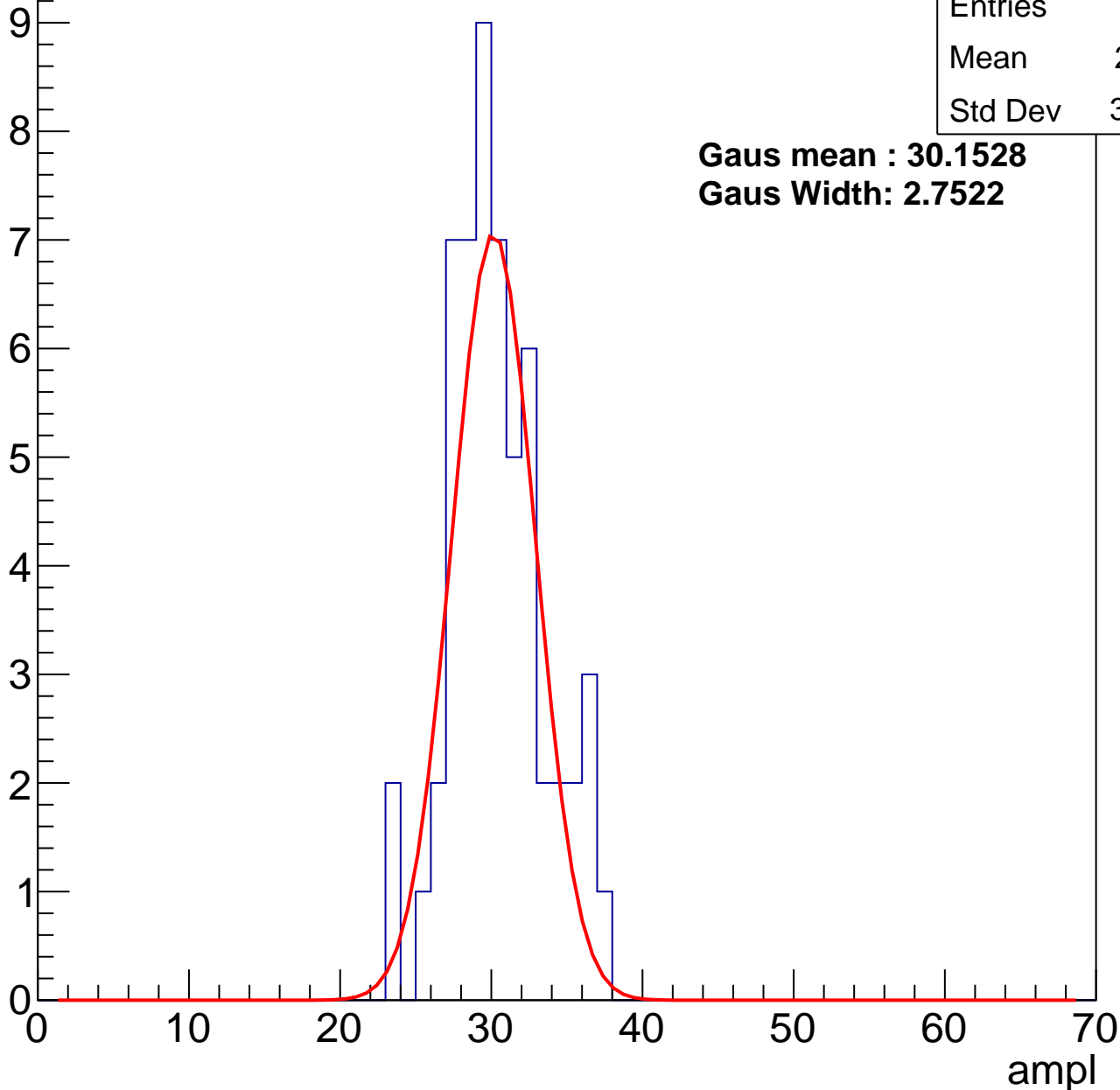
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 56    |
| Mean    | 29.91 |
| Std Dev | 3.107 |

**Gaus mean : 30.1528**

**Gaus Width: 2.7522**



# B0L001S, U2-ch114, adc1

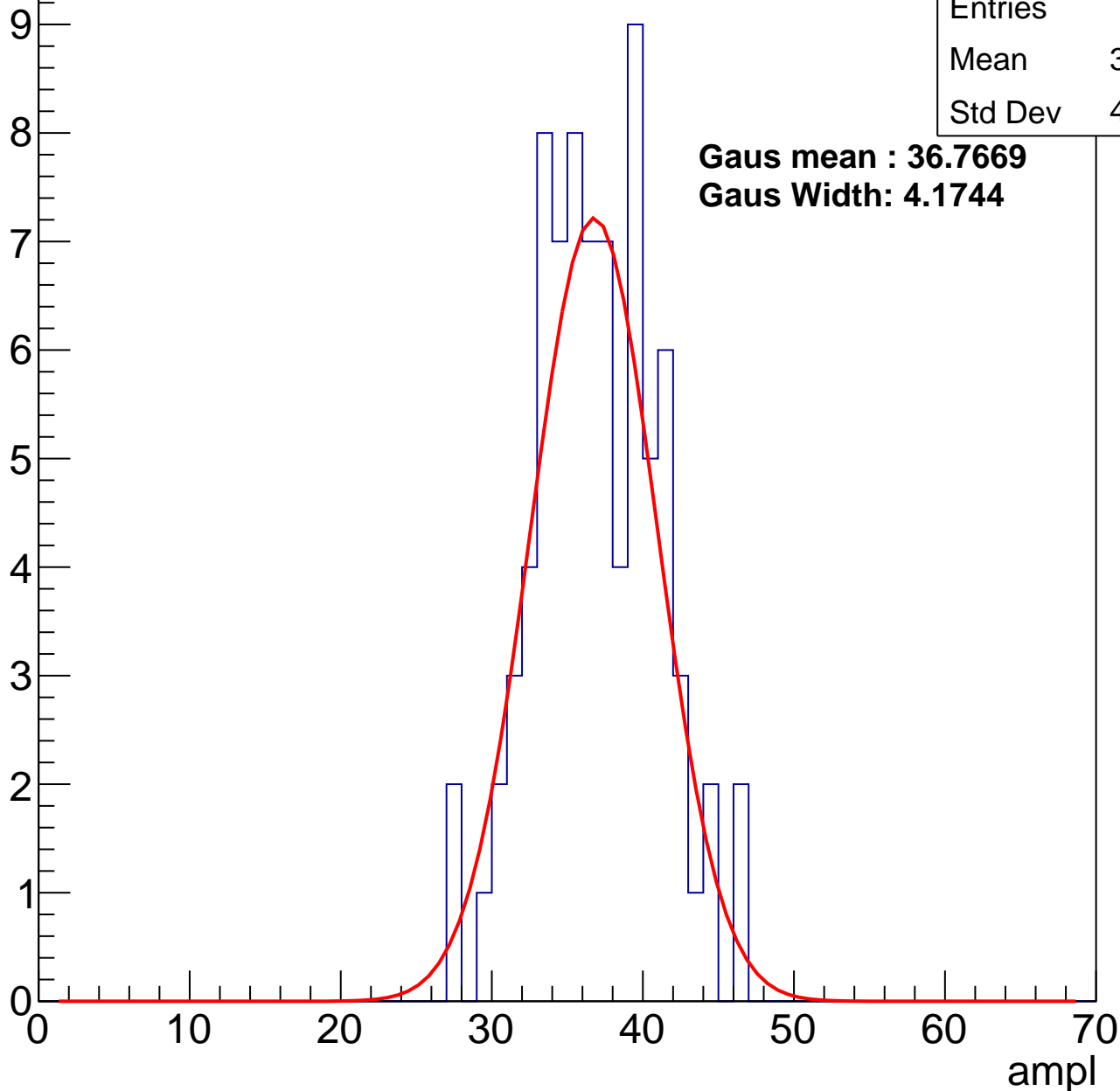
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 81    |
| Mean    | 36.48 |
| Std Dev | 4.052 |

**Gaus mean : 36.7669**

**Gaus Width: 4.1744**

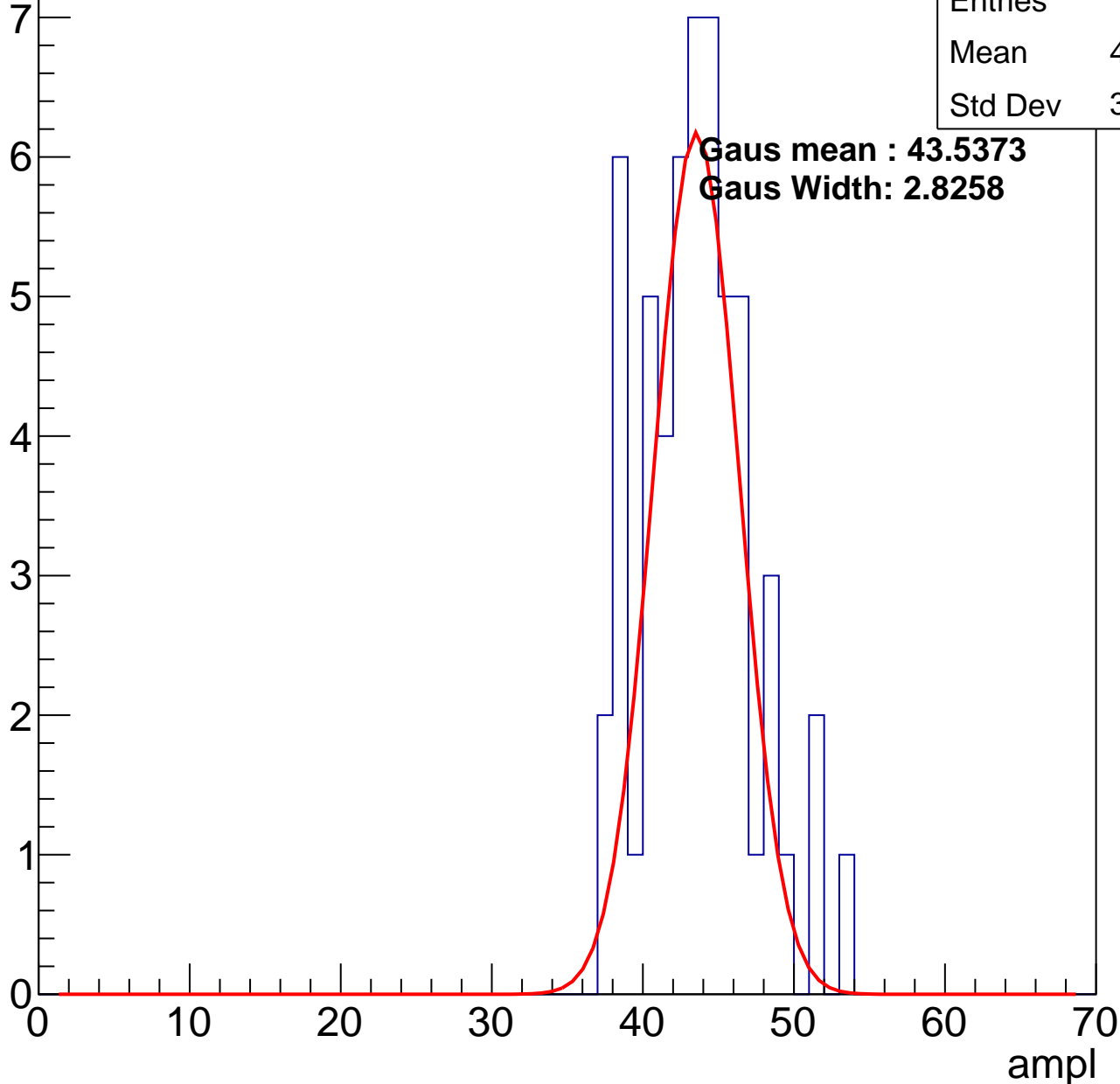


# B0L001S, U2-ch114, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 56    |
| Mean    | 43.14 |
| Std Dev | 3.613 |

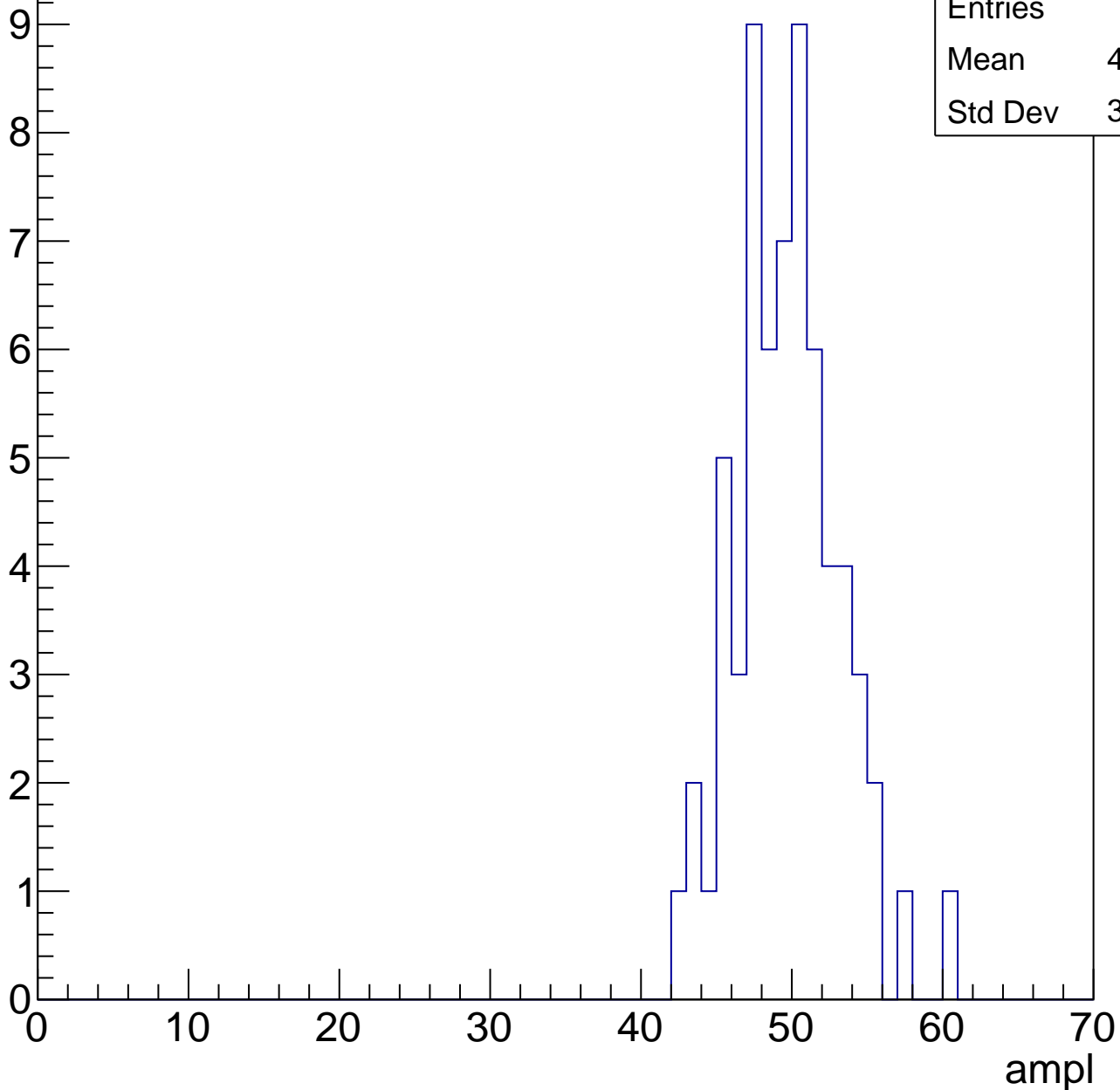


# B0L001S, U2-ch114, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 64    |
| Mean    | 49.28 |
| Std Dev | 3.435 |

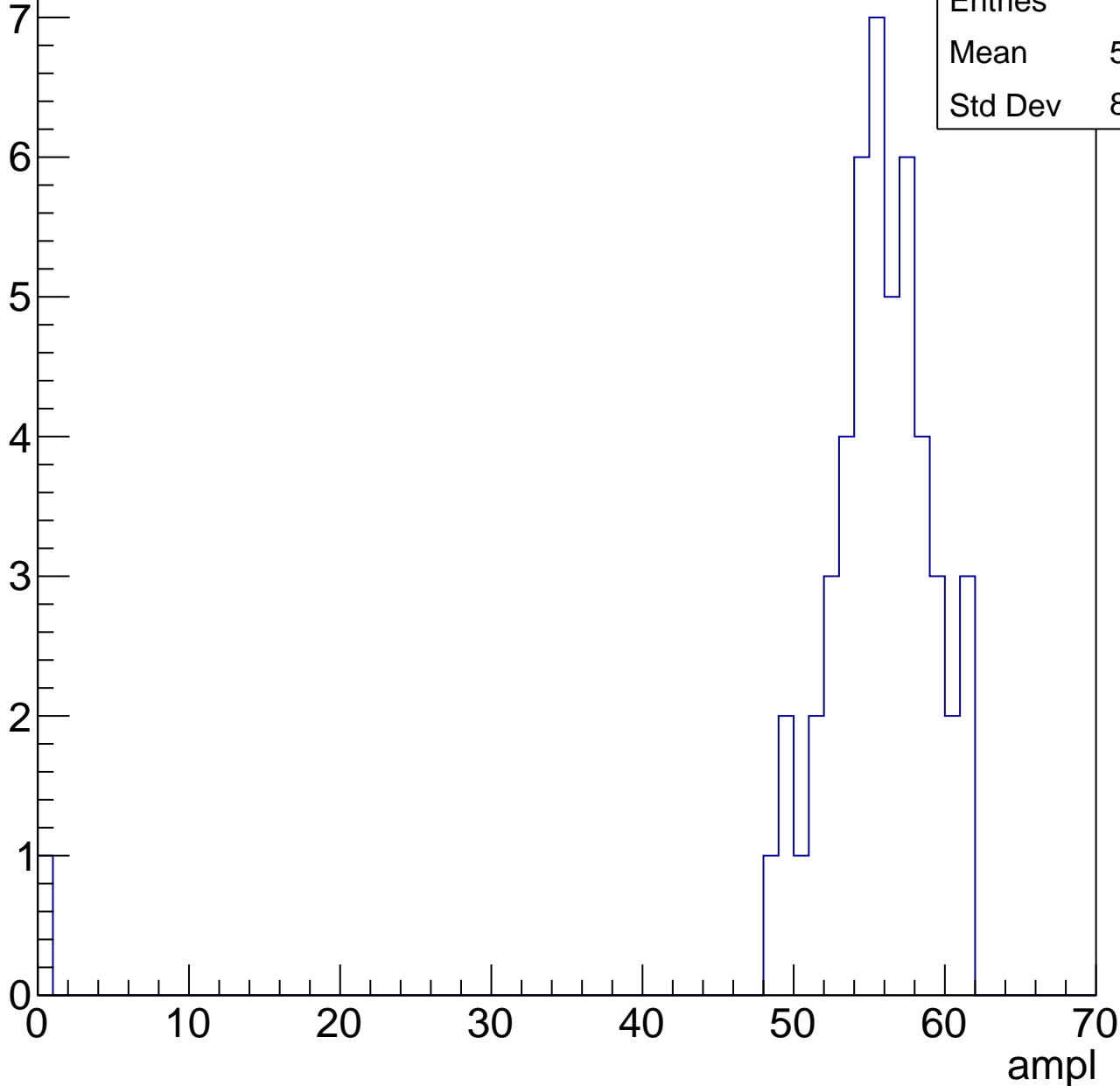


# B0L001S, U2-ch114, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 50    |
| Mean    | 54.18 |
| Std Dev | 8.354 |

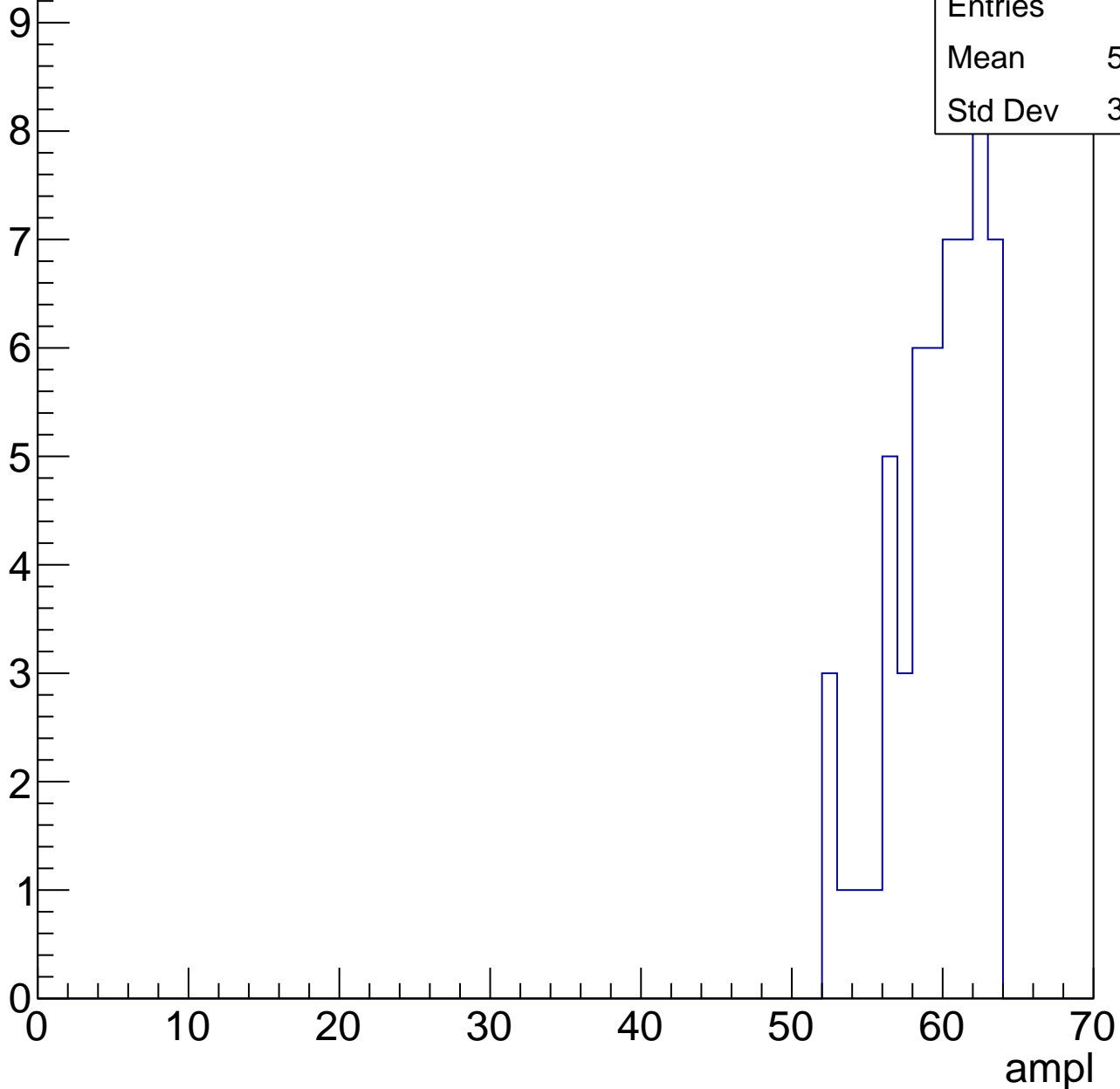


# B0L001S, U2-ch114, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 56    |
| Mean    | 59.23 |
| Std Dev | 3.024 |



# B0L001S, U2-ch114, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch114, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 0 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch115, adc0

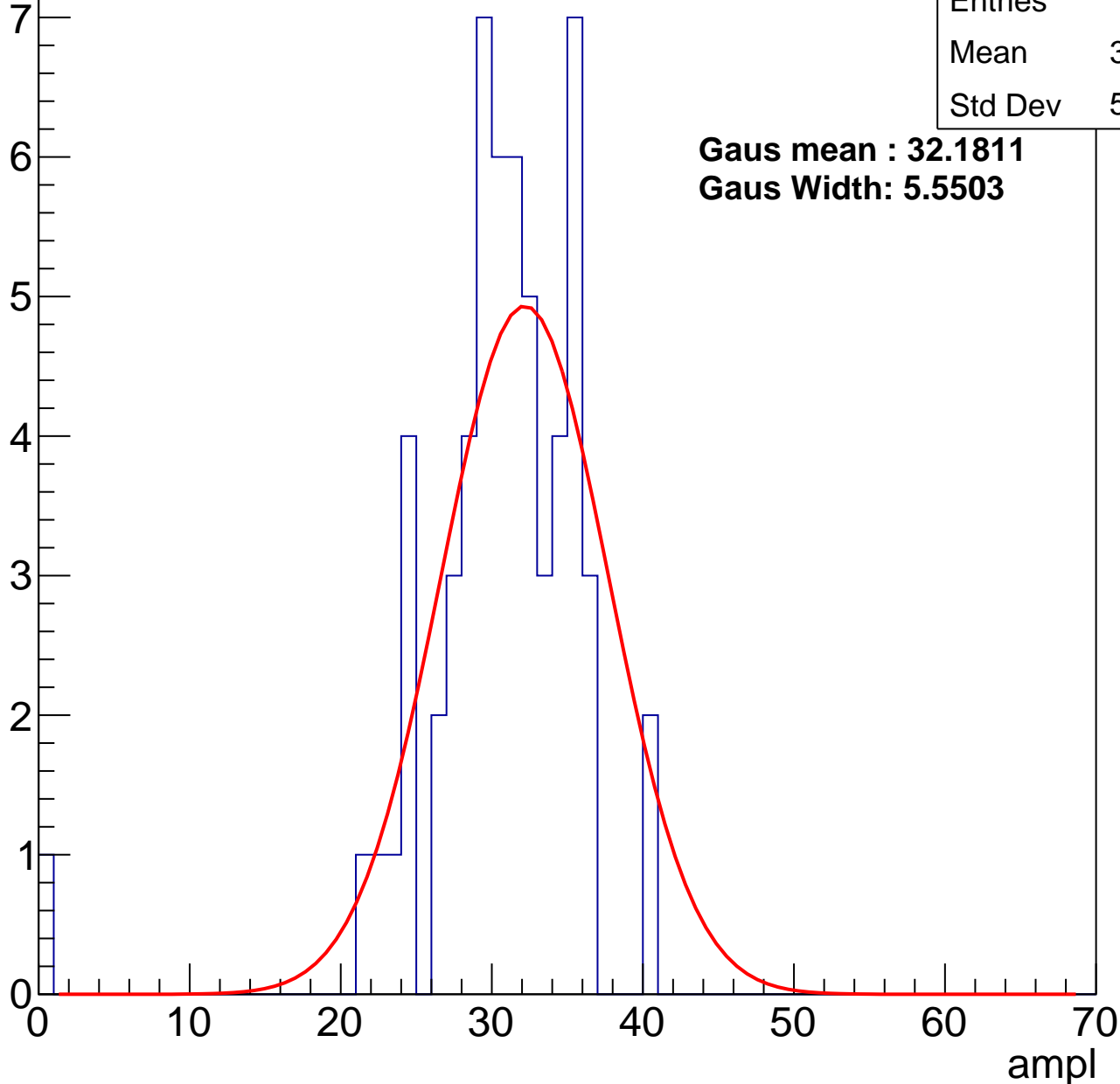
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 60    |
| Mean    | 30.07 |
| Std Dev | 5.656 |

**Gaus mean : 32.1811**

**Gaus Width: 5.5503**



# B0L001S, U2-ch115, adc1

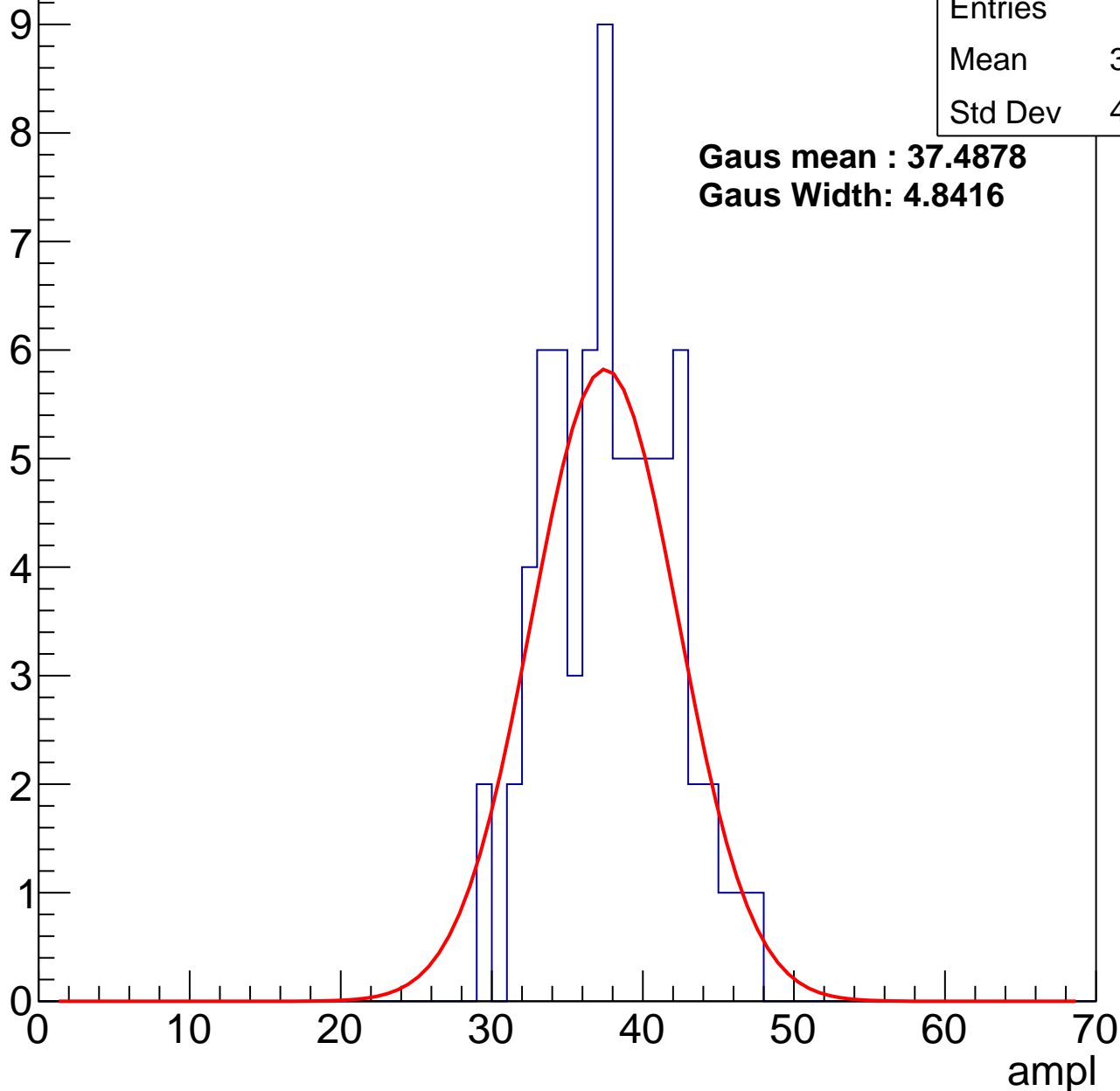
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 71    |
| Mean    | 37.44 |
| Std Dev | 4.058 |

**Gaus mean : 37.4878**

**Gaus Width: 4.8416**



# B0L001S, U2-ch115, adc2

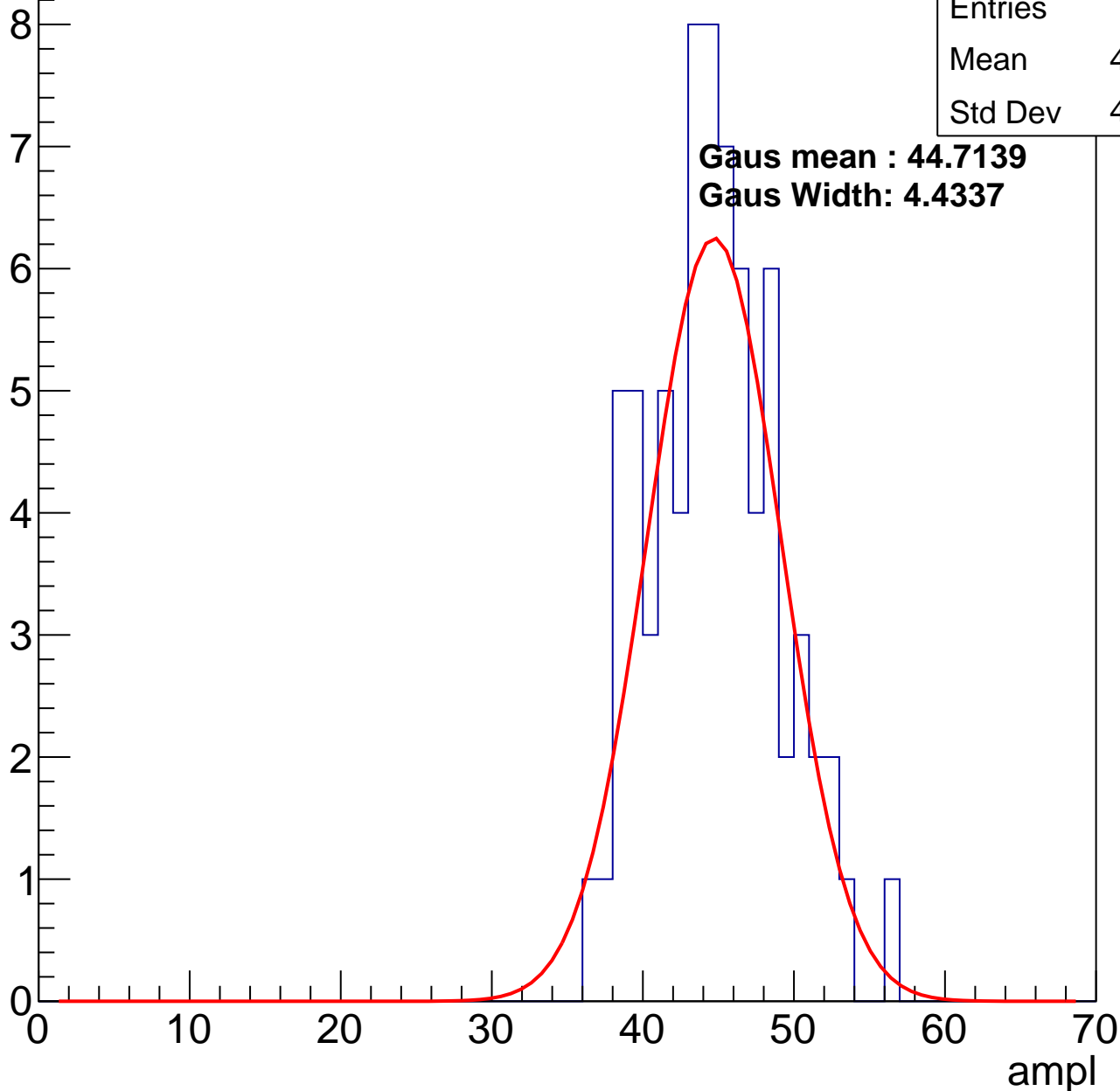
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 74    |
| Mean    | 44.28 |
| Std Dev | 4.193 |

**Gaus mean : 44.7139**

**Gaus Width: 4.4337**

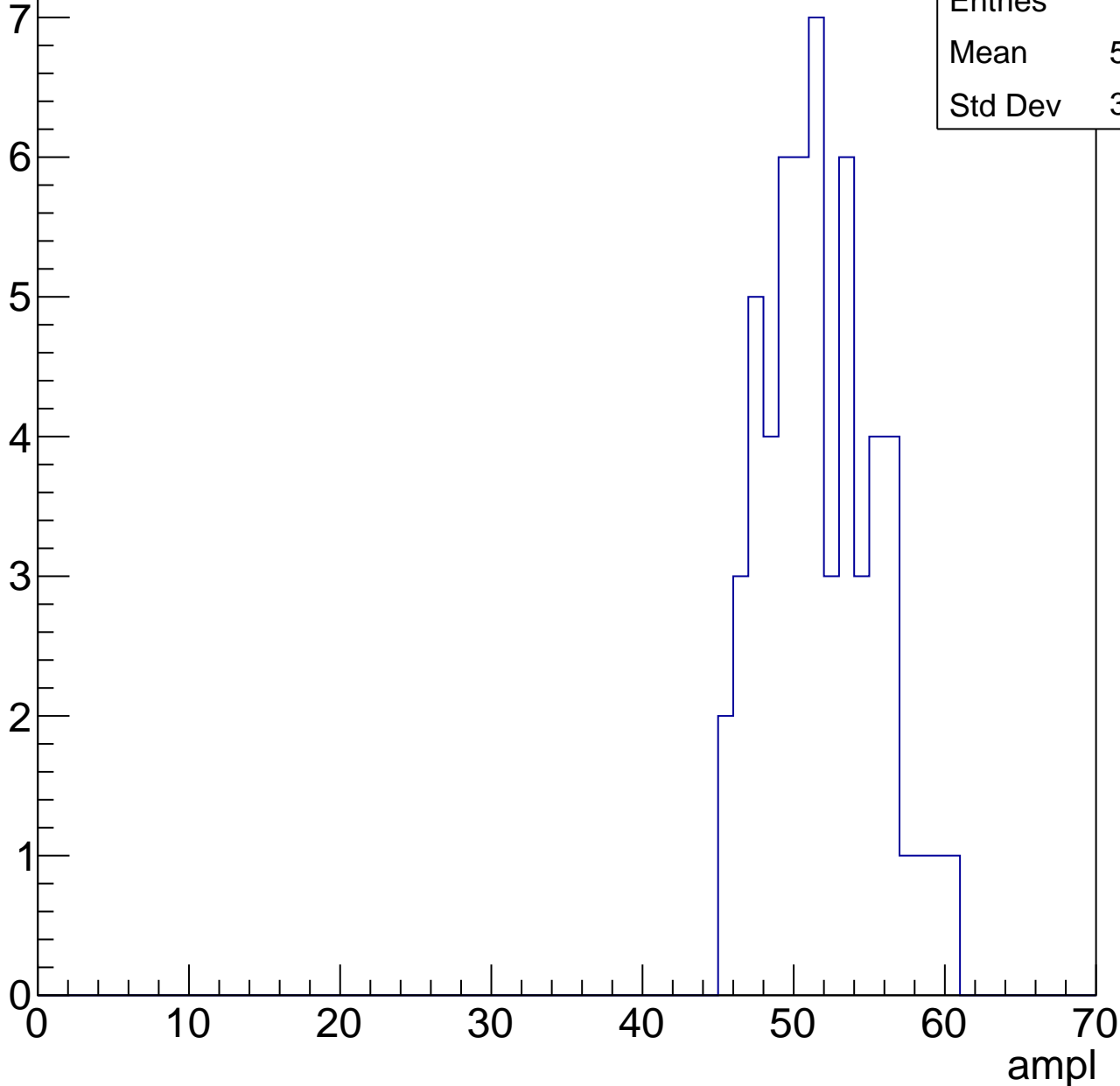


# B0L001S, U2-ch115, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 57    |
| Mean    | 51.23 |
| Std Dev | 3.598 |

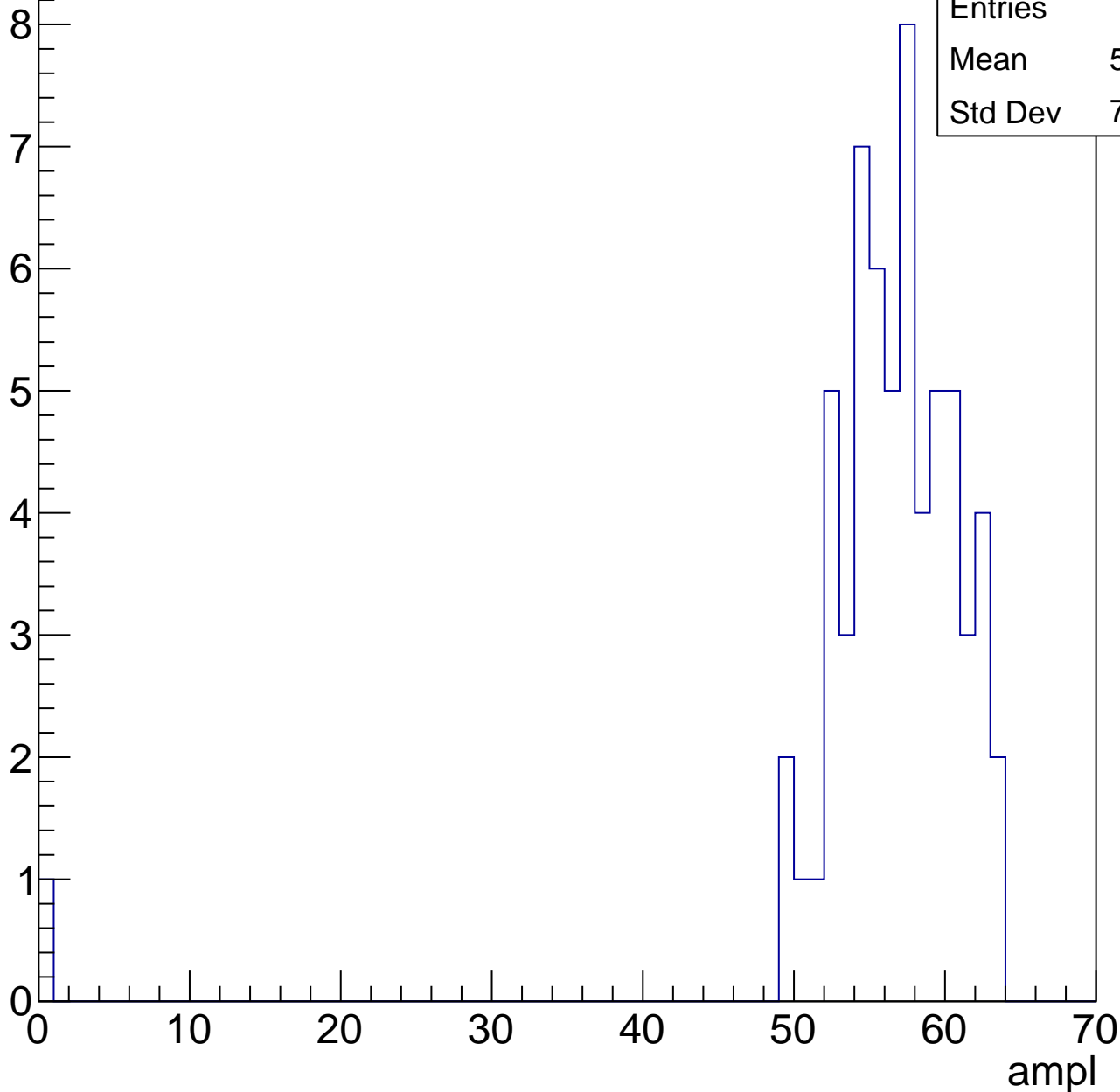


# B0L001S, U2-ch115, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

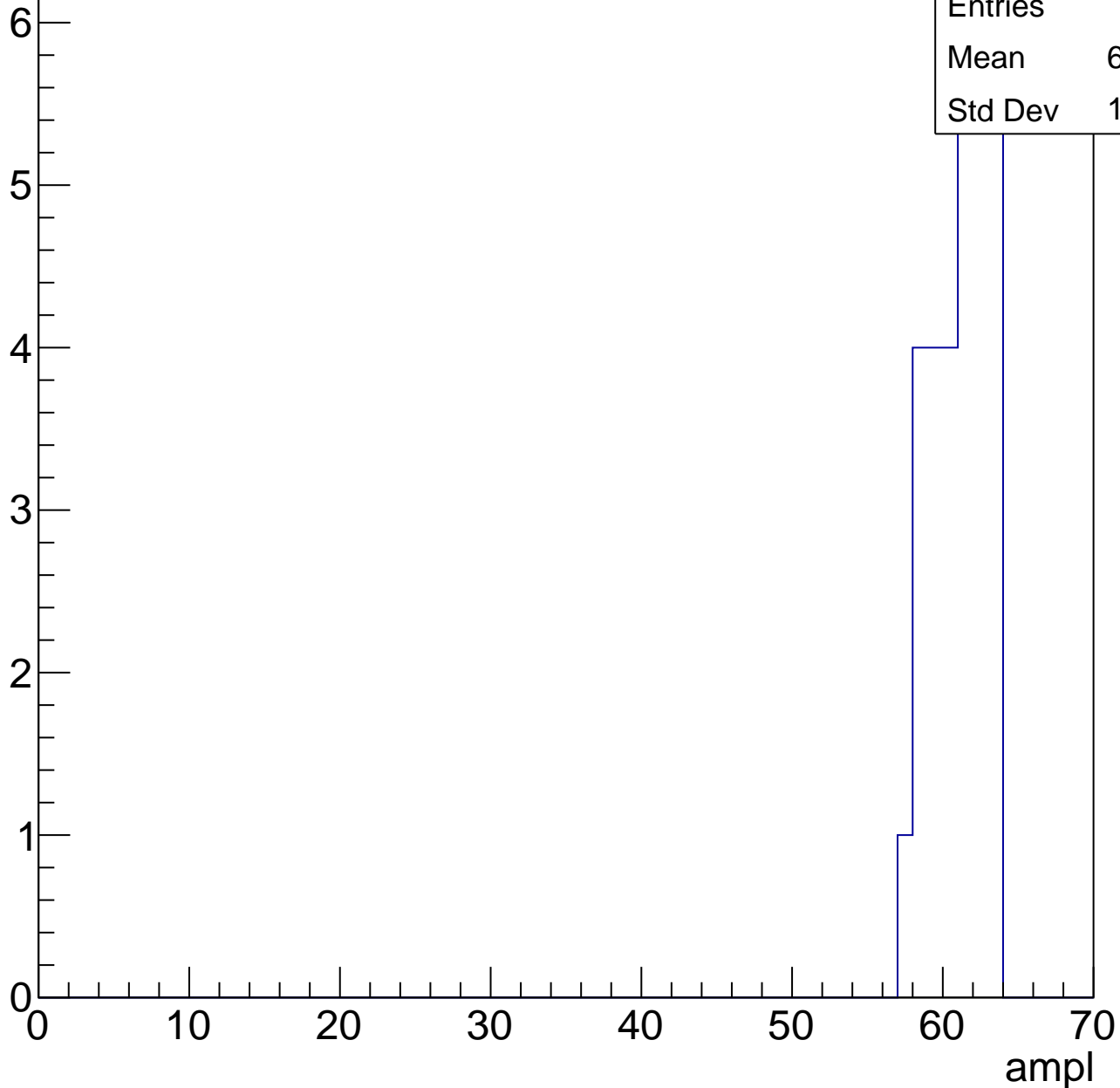
|         |       |
|---------|-------|
| Entries | 62    |
| Mean    | 55.58 |
| Std Dev | 7.922 |



# B0L001S, U2-ch115, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

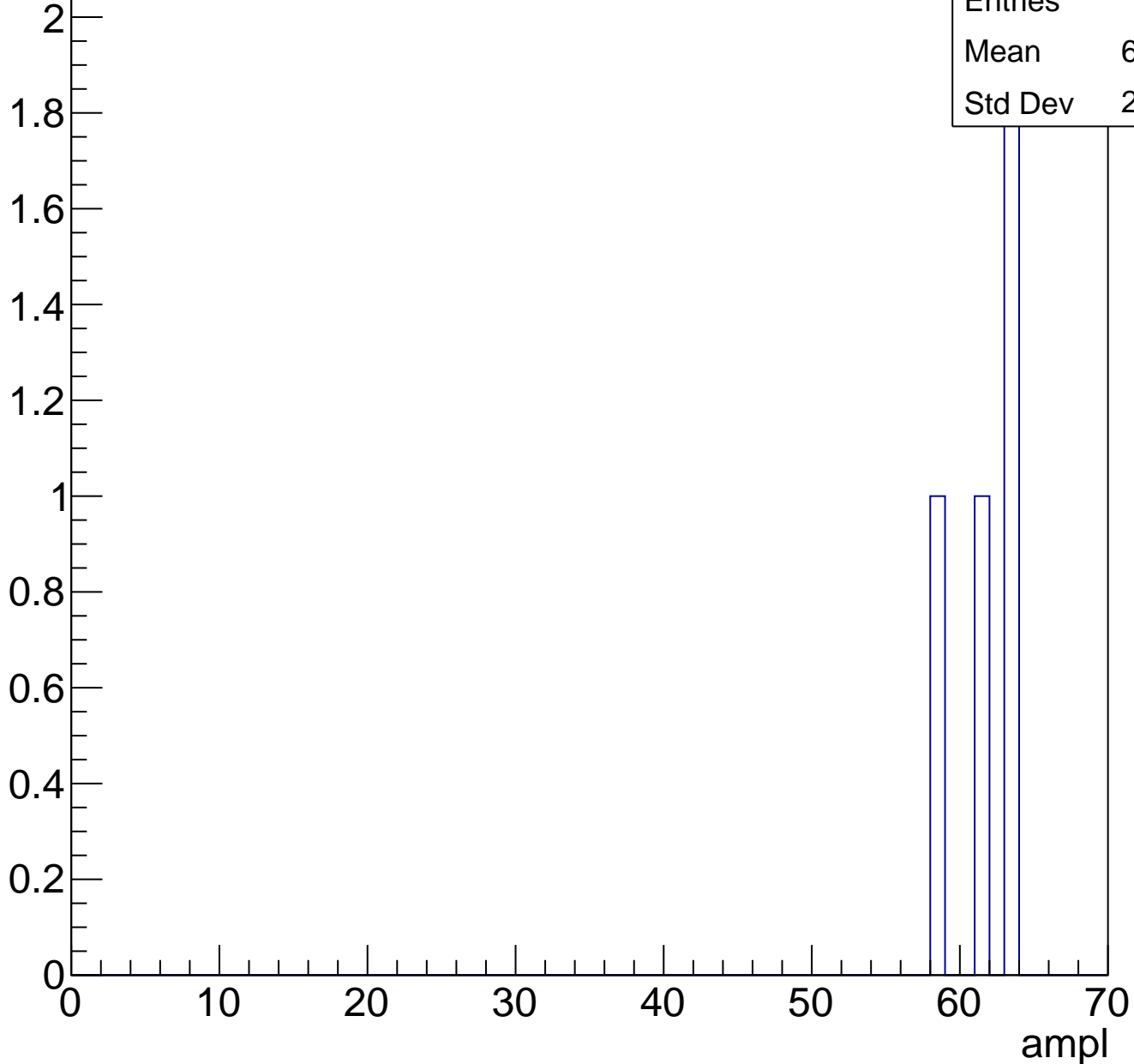
Entry



# B0L001S, U2-ch115, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch115, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 1 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch116, adc0

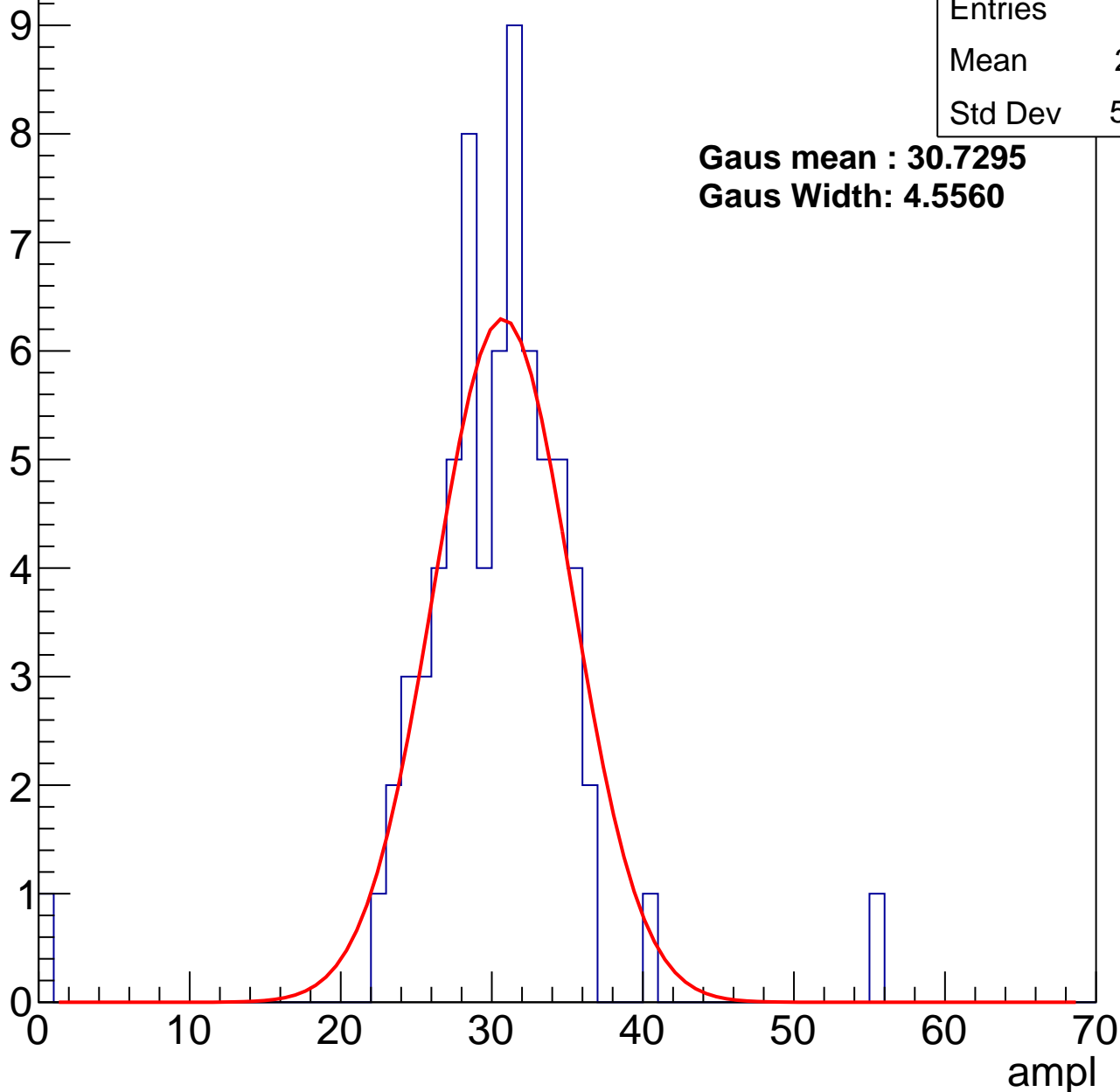
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 70    |
| Mean    | 29.81 |
| Std Dev | 5.907 |

**Gaus mean : 30.7295**

**Gaus Width: 4.5560**



# B0L001S, U2-ch116, adc1

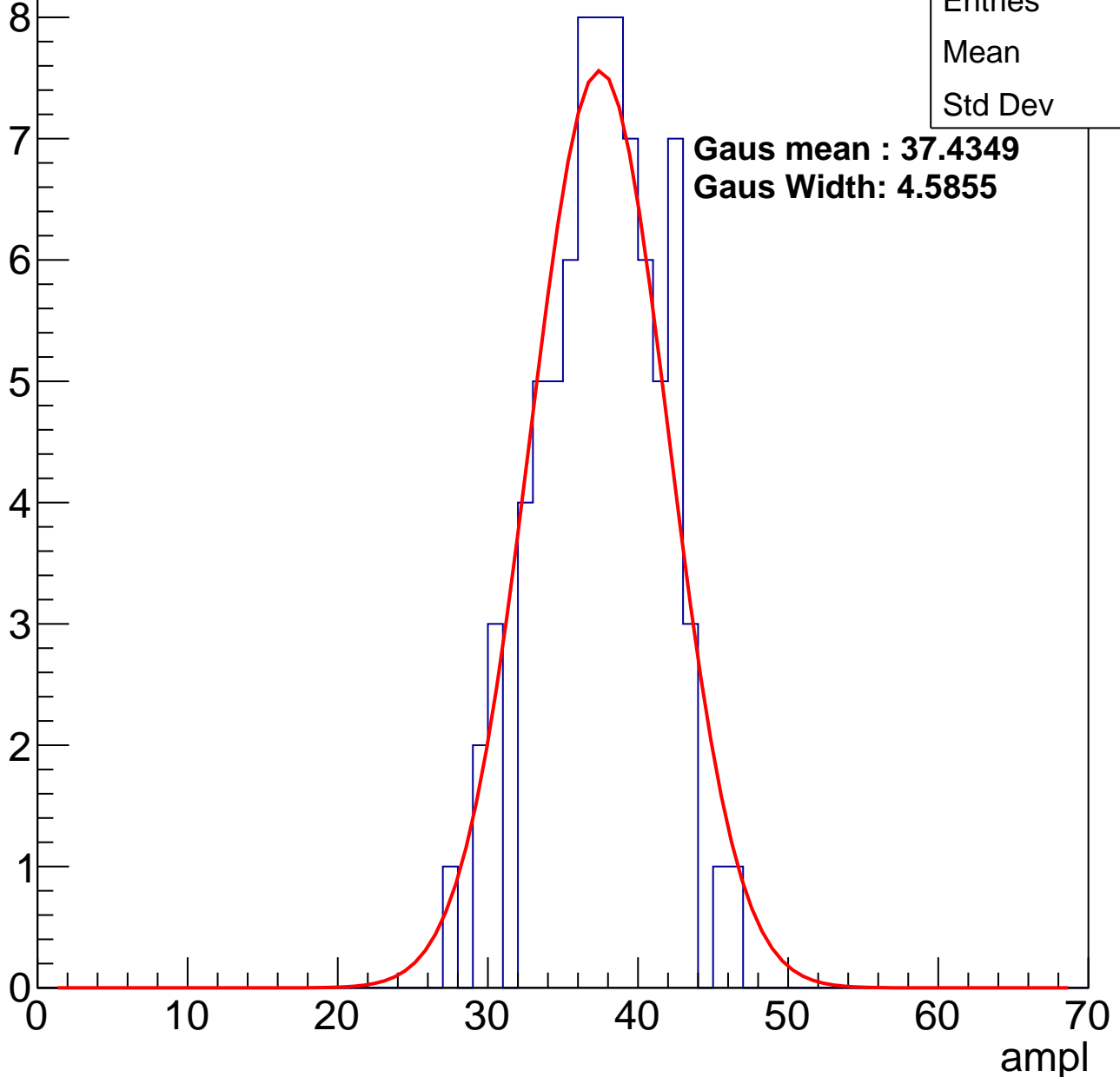
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |      |
|---------|------|
| Entries | 80   |
| Mean    | 37.1 |
| Std Dev | 3.92 |

**Gaus mean : 37.4349**

**Gaus Width: 4.5855**



# B0L001S, U2-ch116, adc2

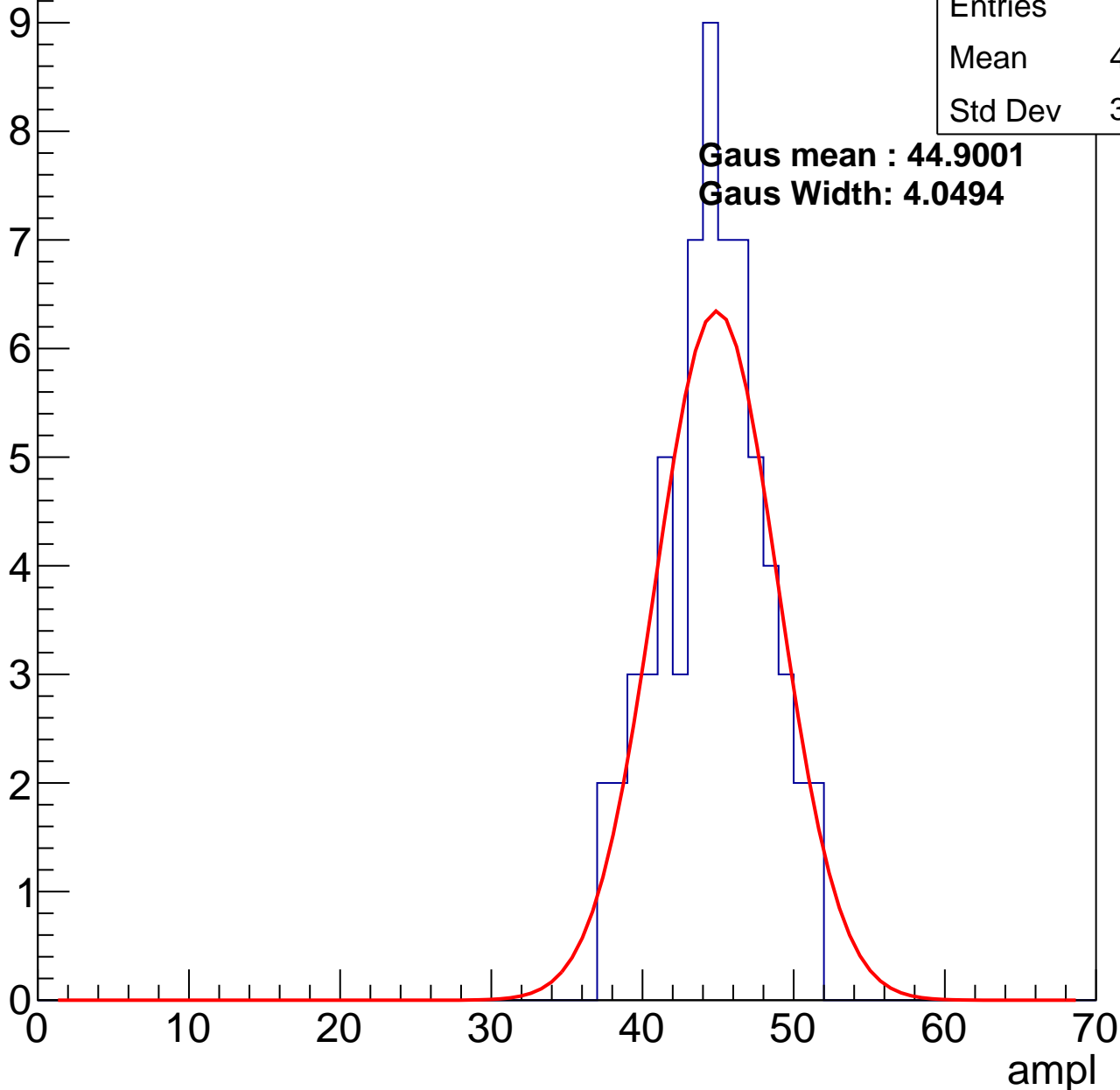
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 64    |
| Mean    | 44.19 |
| Std Dev | 3.409 |

**Gaus mean : 44.9001**

**Gaus Width: 4.0494**

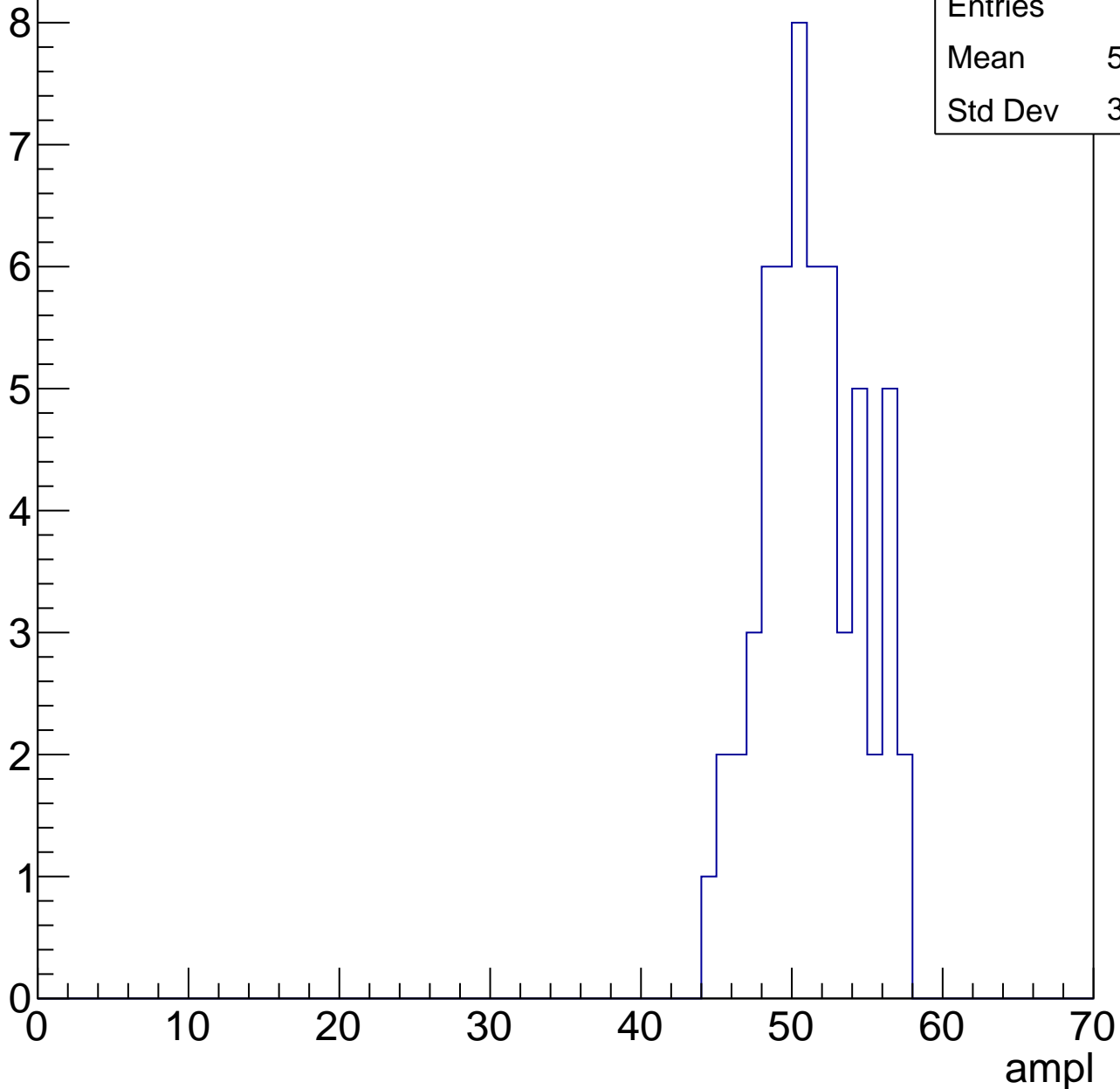


# B0L001S, U2-ch116, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 57    |
| Mean    | 50.88 |
| Std Dev | 3.234 |

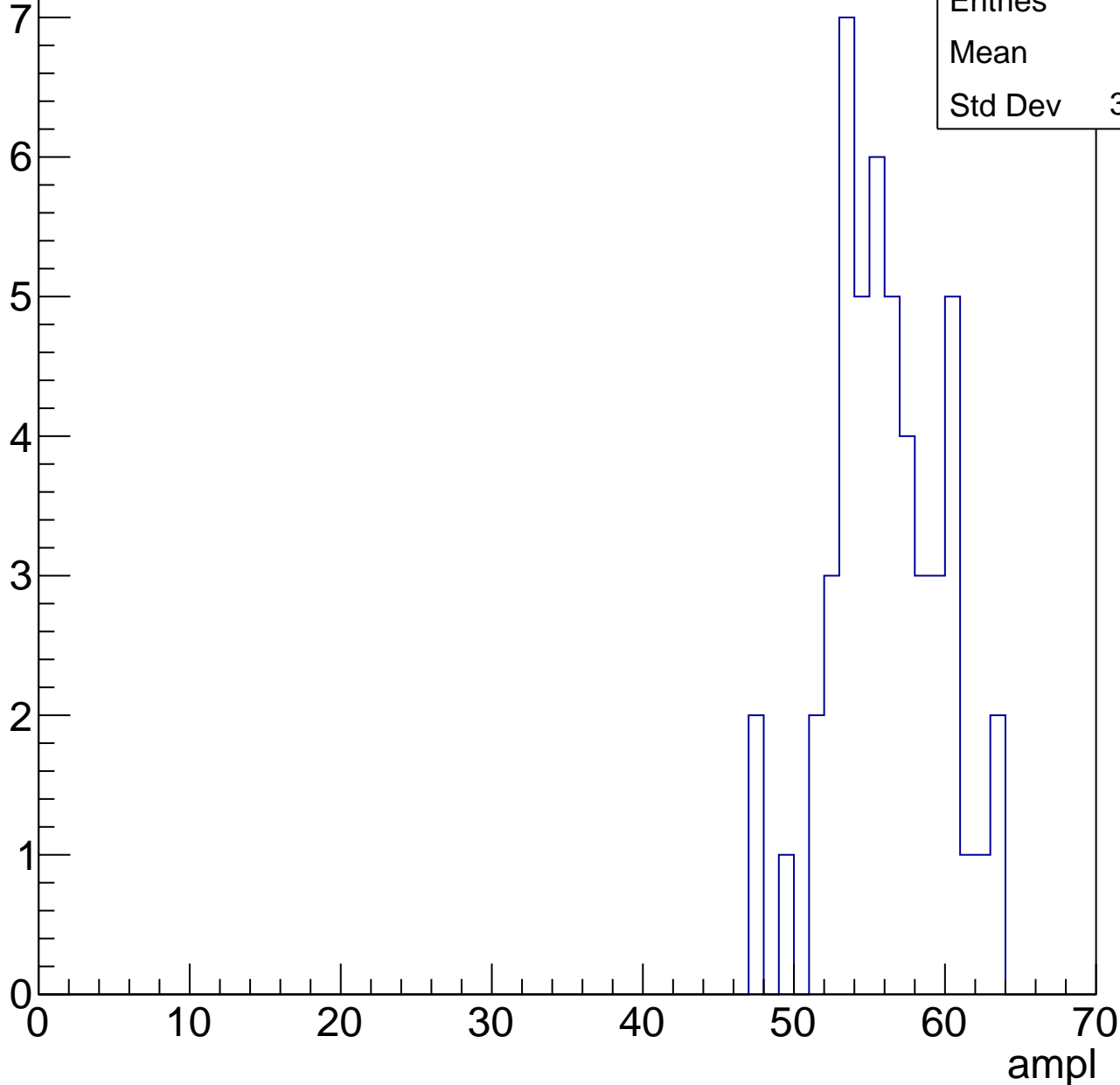


# B0L001S, U2-ch116, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 50    |
| Mean    | 55.6  |
| Std Dev | 3.666 |

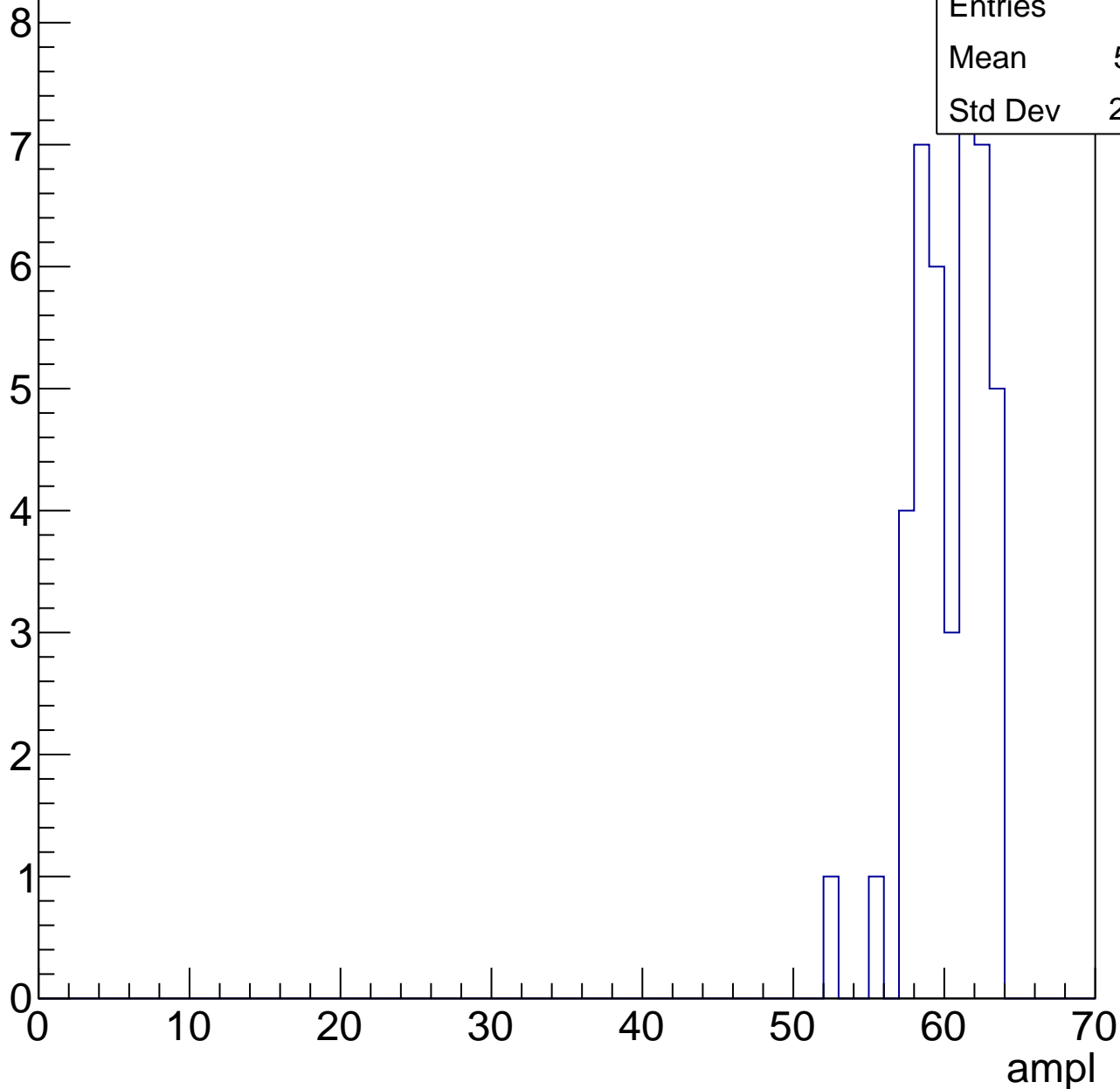


# B0L001S, U2-ch116, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

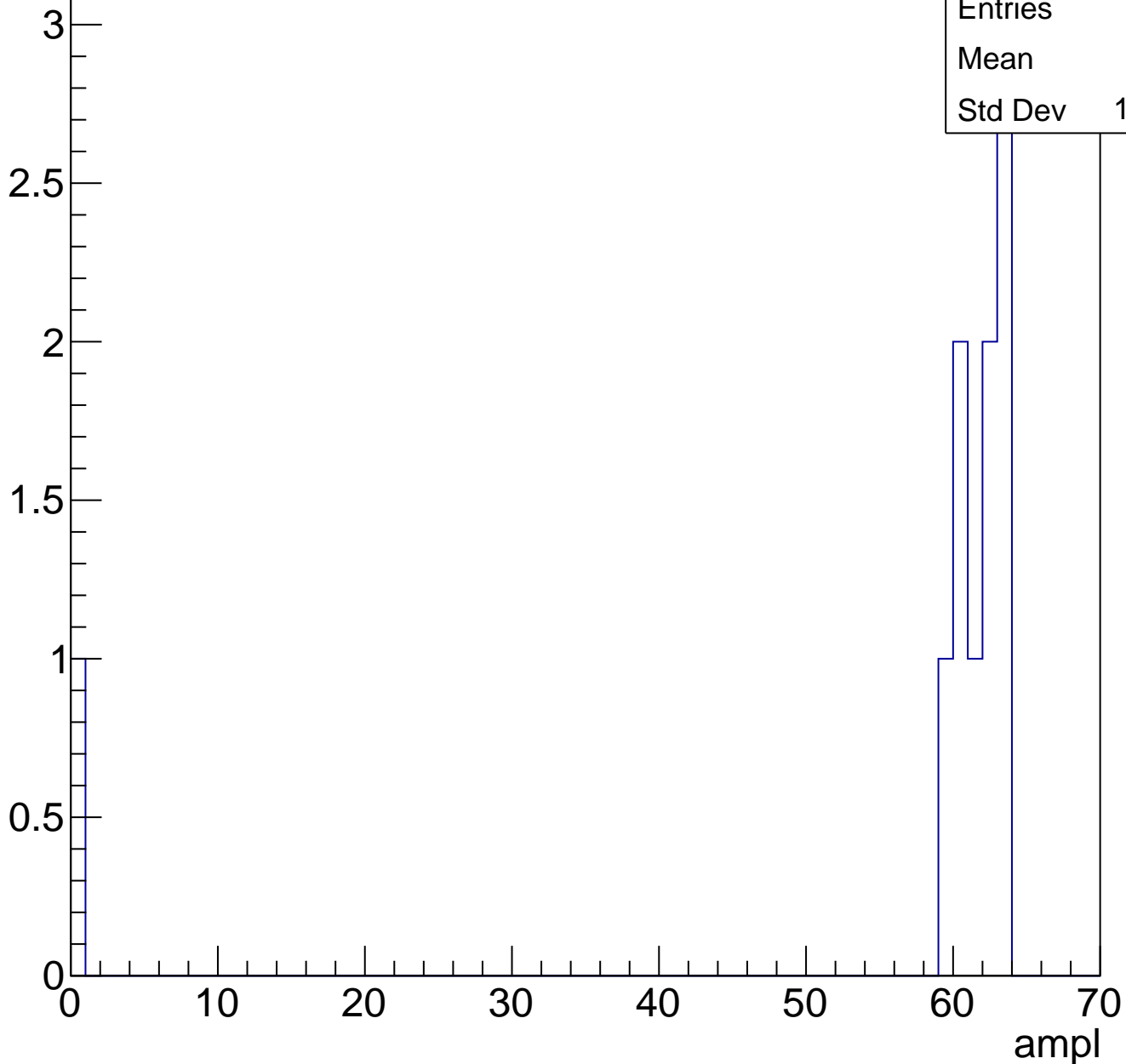
|         |       |
|---------|-------|
| Entries | 42    |
| Mean    | 59.81 |
| Std Dev | 2.383 |



# B0L001S, U2-ch116, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch116, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 0 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch117, adc0

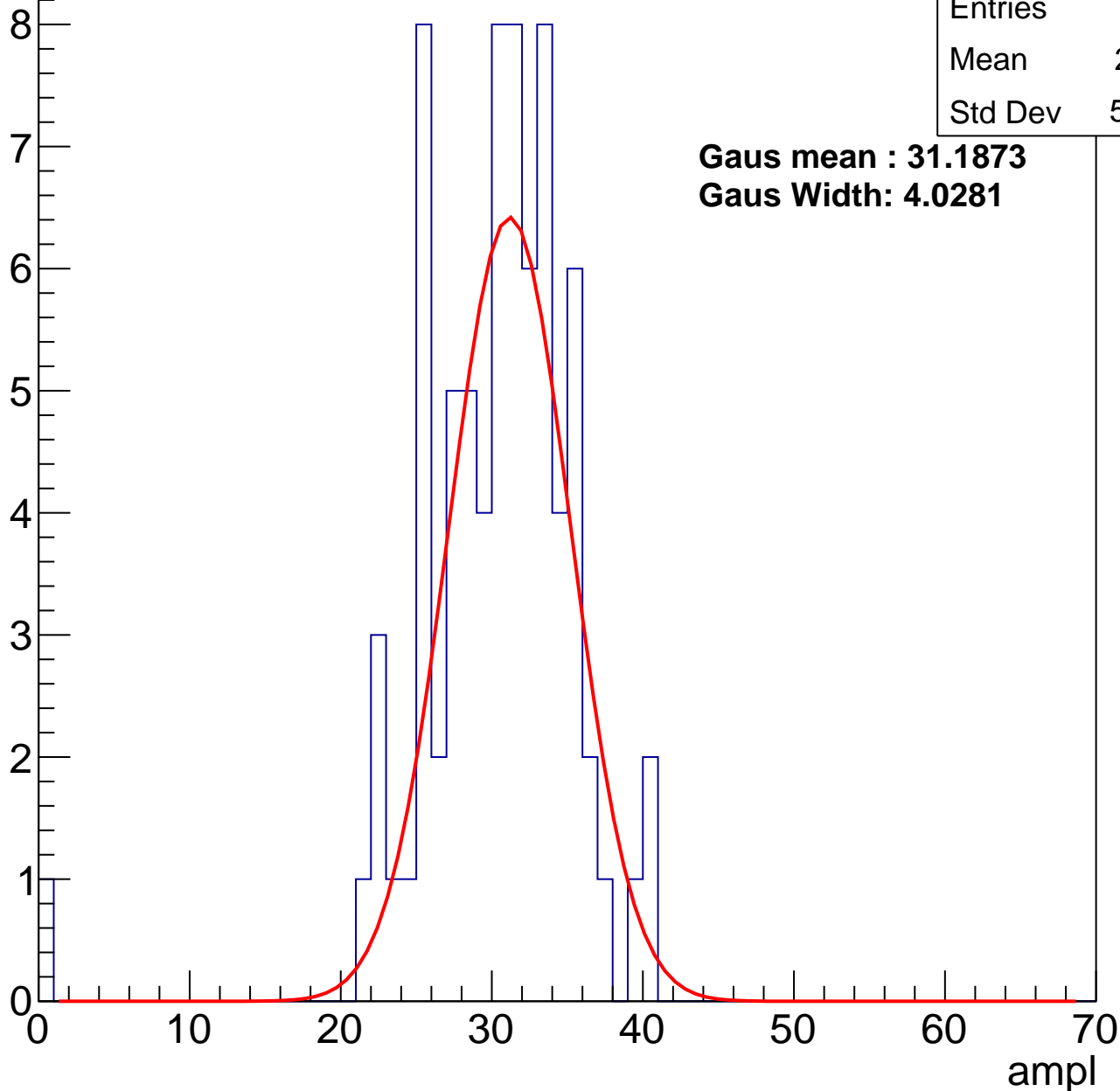
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 77    |
| Mean    | 29.81 |
| Std Dev | 5.437 |

**Gaus mean : 31.1873**

**Gaus Width: 4.0281**

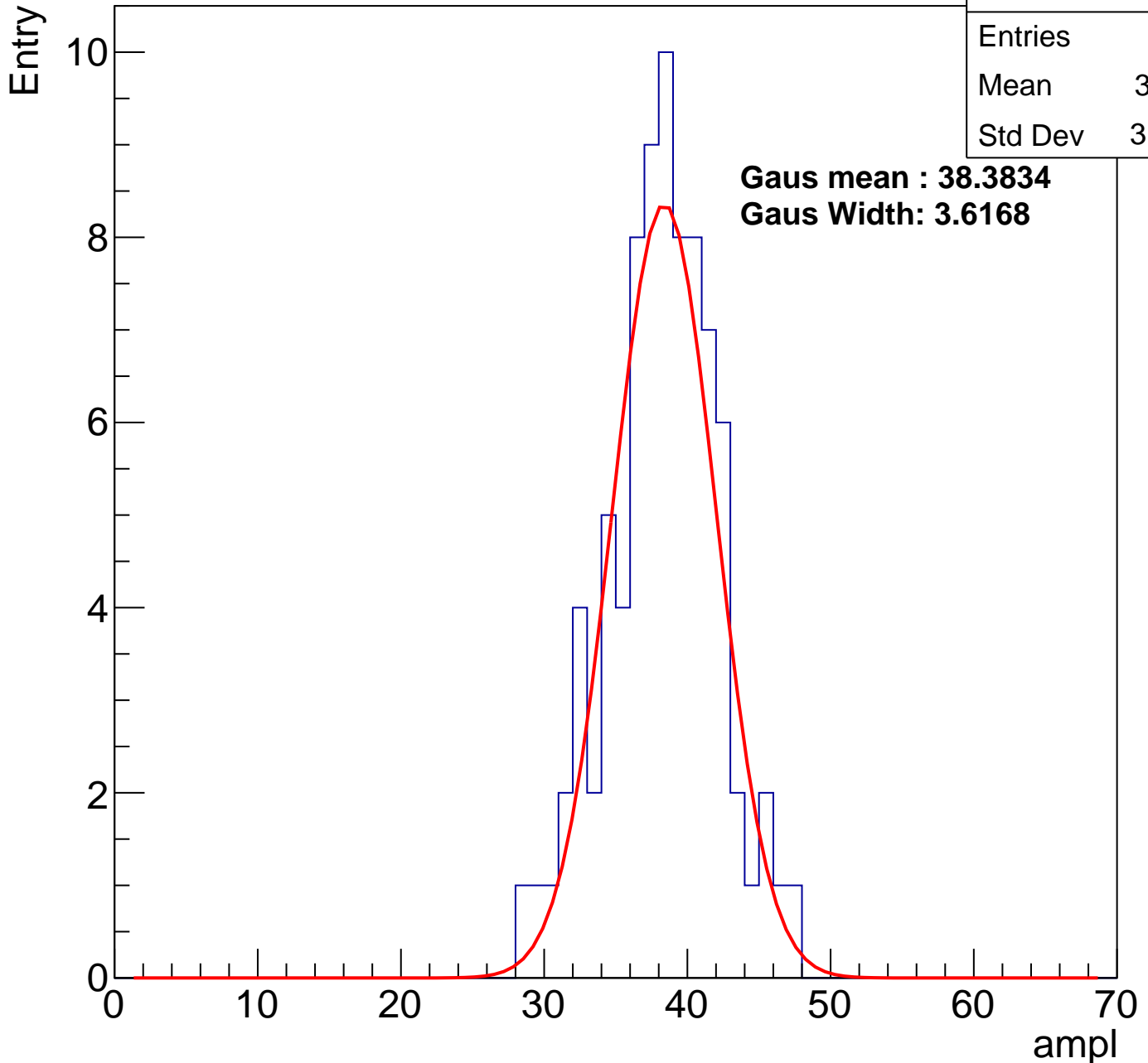


# B0L001S, U2-ch117, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 83    |
| Mean    | 37.81 |
| Std Dev | 3.832 |

**Gaus mean : 38.3834**  
**Gaus Width: 3.6168**



# B0L001S, U2-ch117, adc2

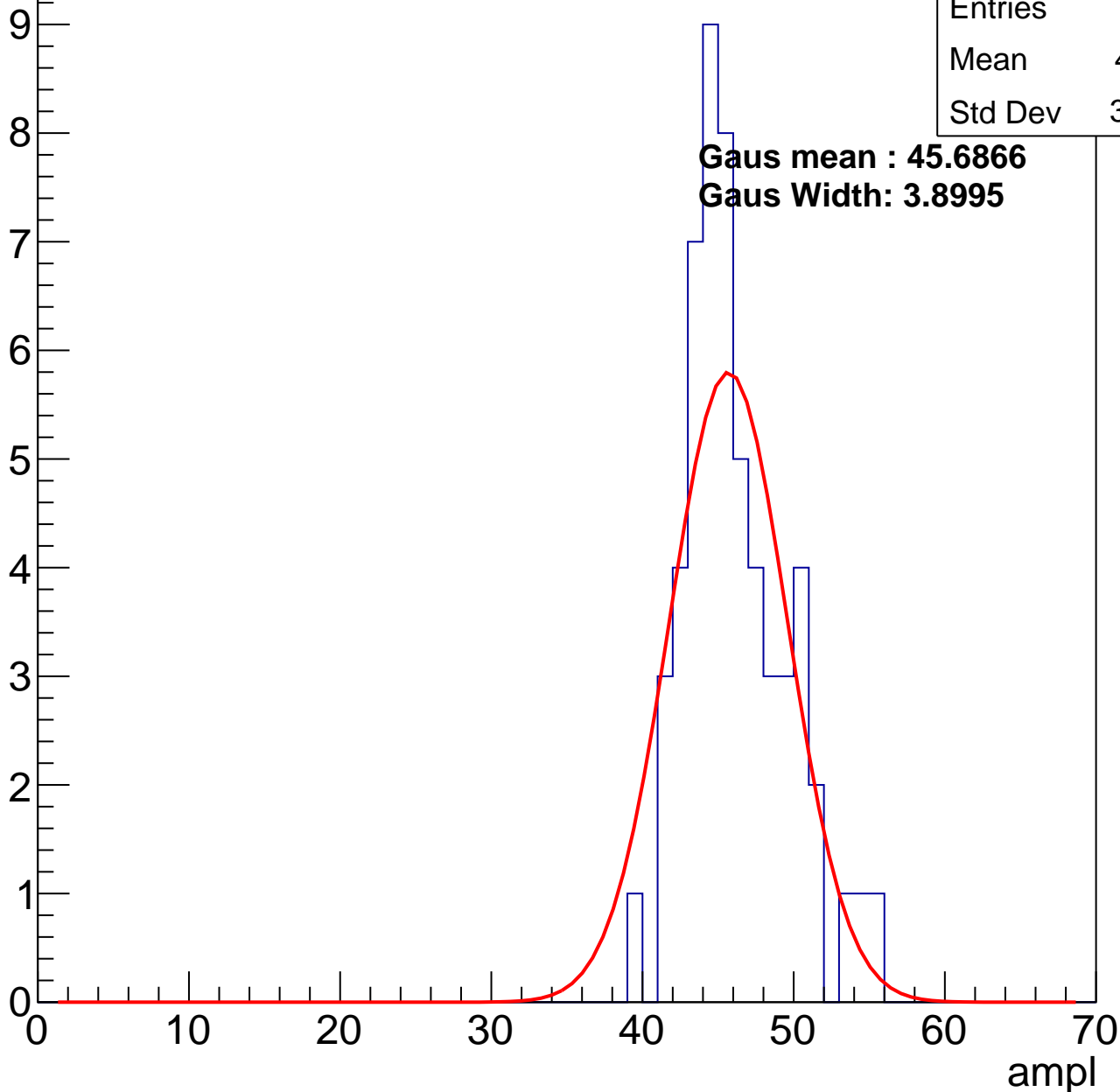
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 56    |
| Mean    | 45.71 |
| Std Dev | 3.384 |

**Gaus mean : 45.6866**

**Gaus Width: 3.8995**

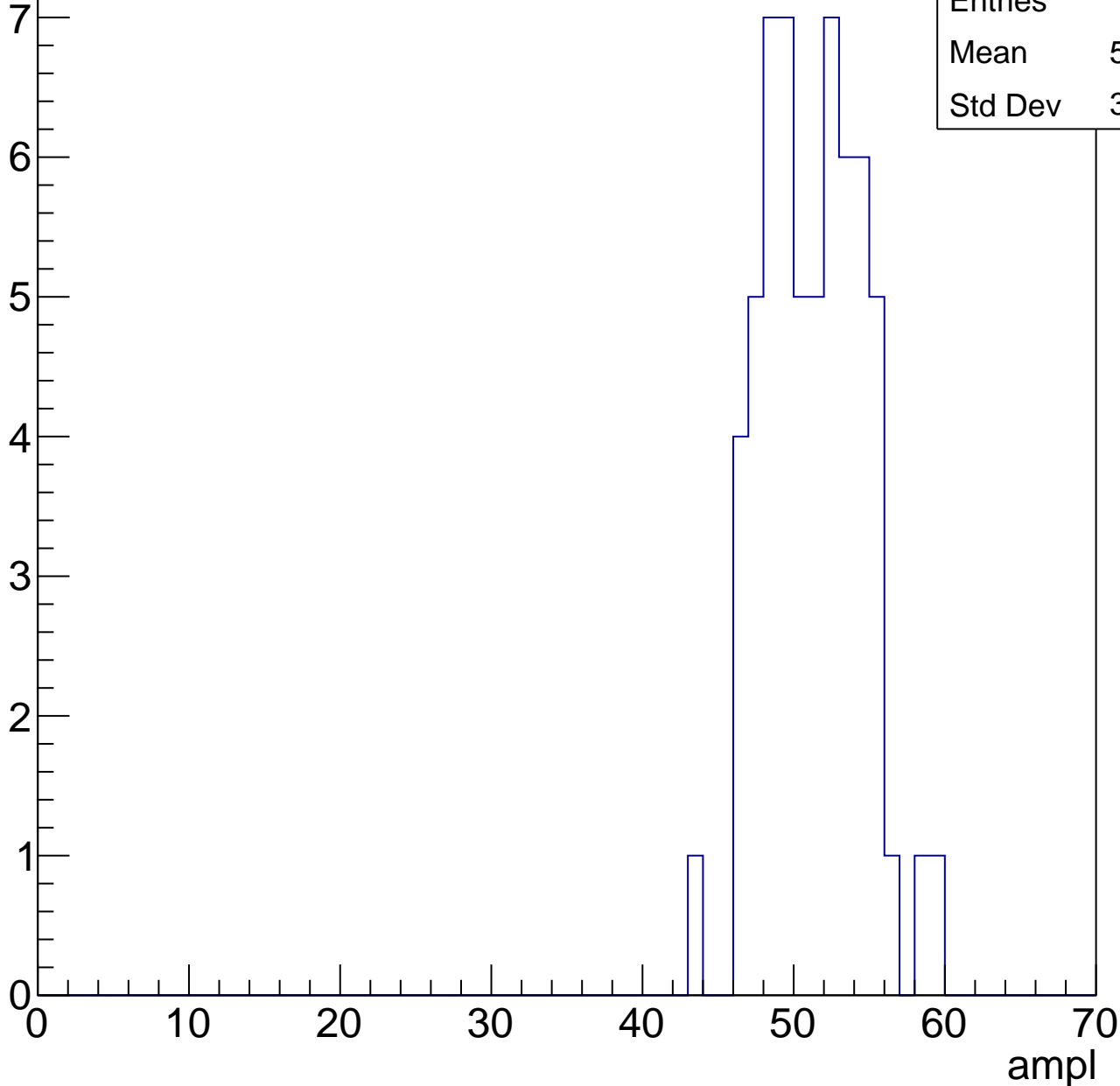


# B0L001S, U2-ch117, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 61    |
| Mean    | 50.82 |
| Std Dev | 3.242 |

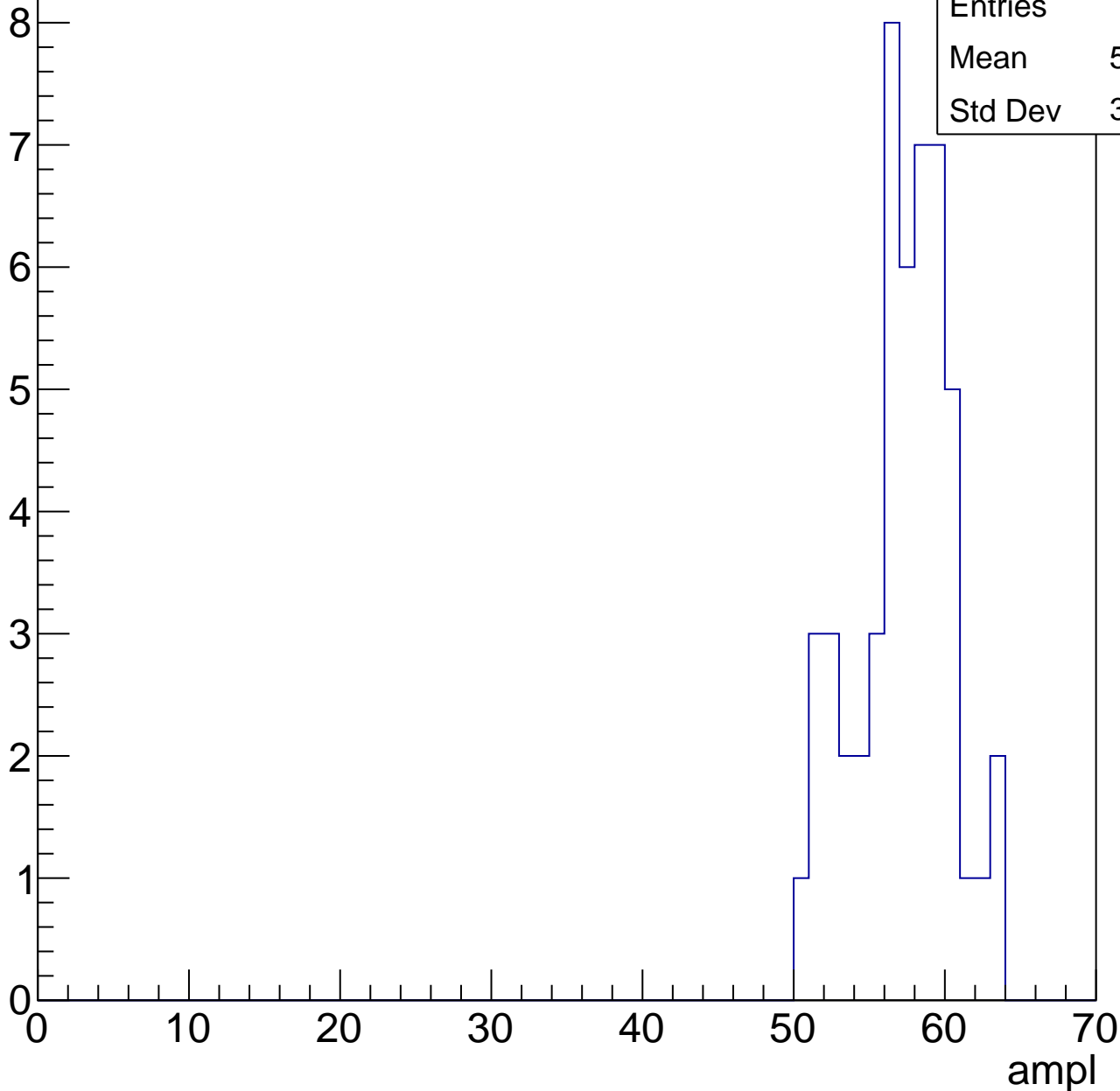


# B0L001S, U2-ch117, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 51    |
| Mean    | 56.78 |
| Std Dev | 3.108 |

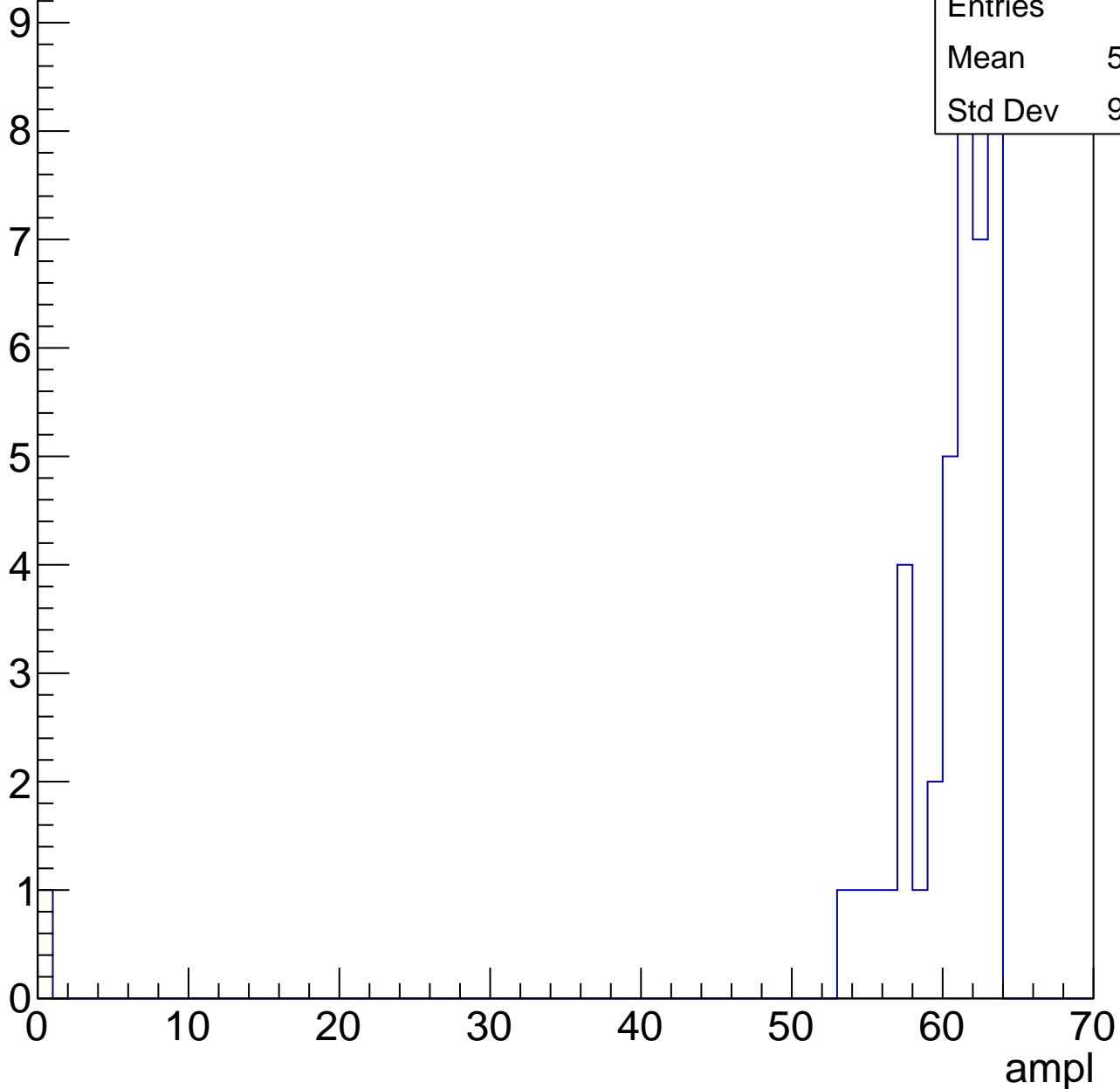


# B0L001S, U2-ch117, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

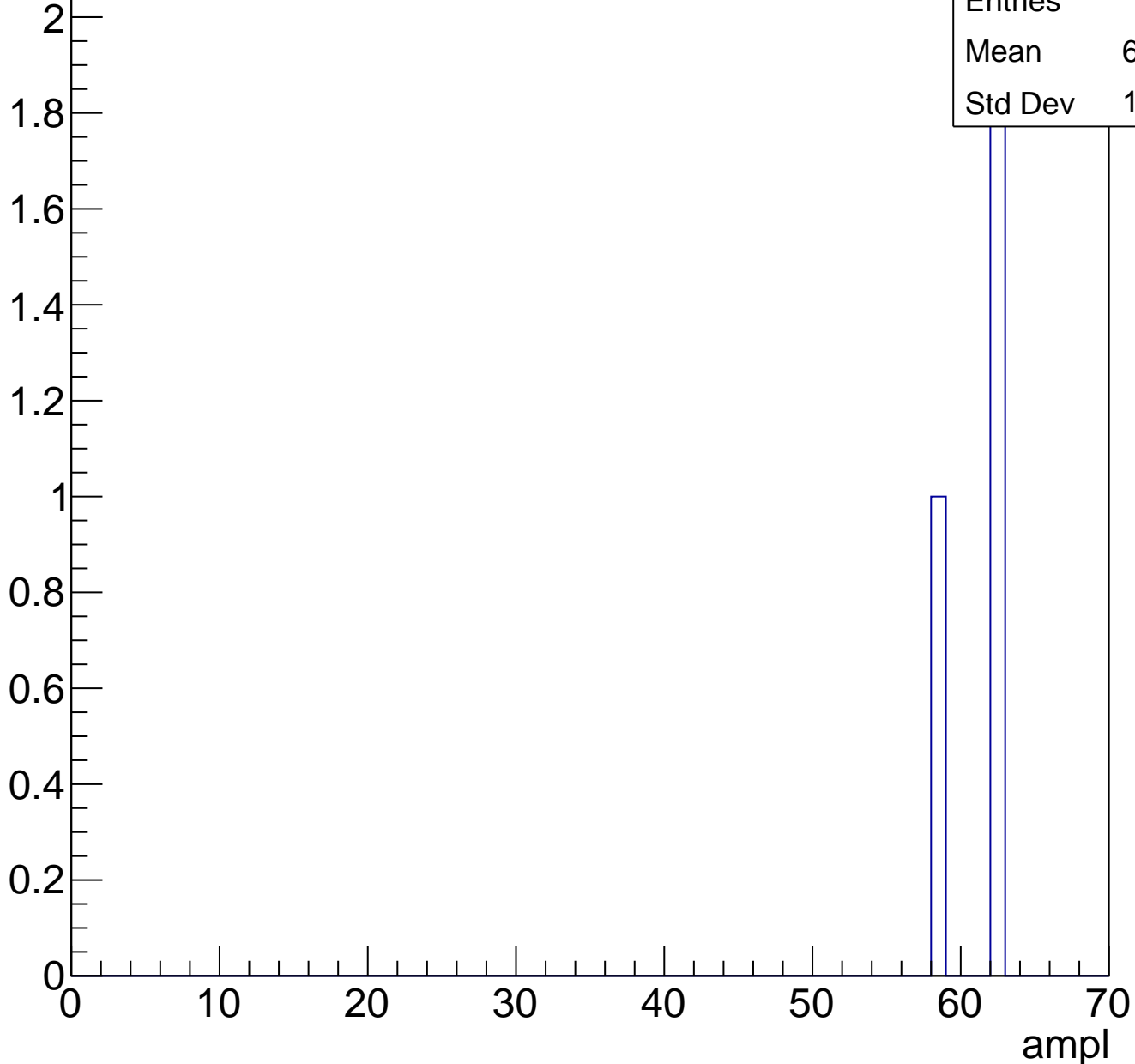
|         |       |
|---------|-------|
| Entries | 41    |
| Mean    | 58.76 |
| Std Dev | 9.644 |



# B0L001S, U2-ch117, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch117, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 1 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch118, adc0

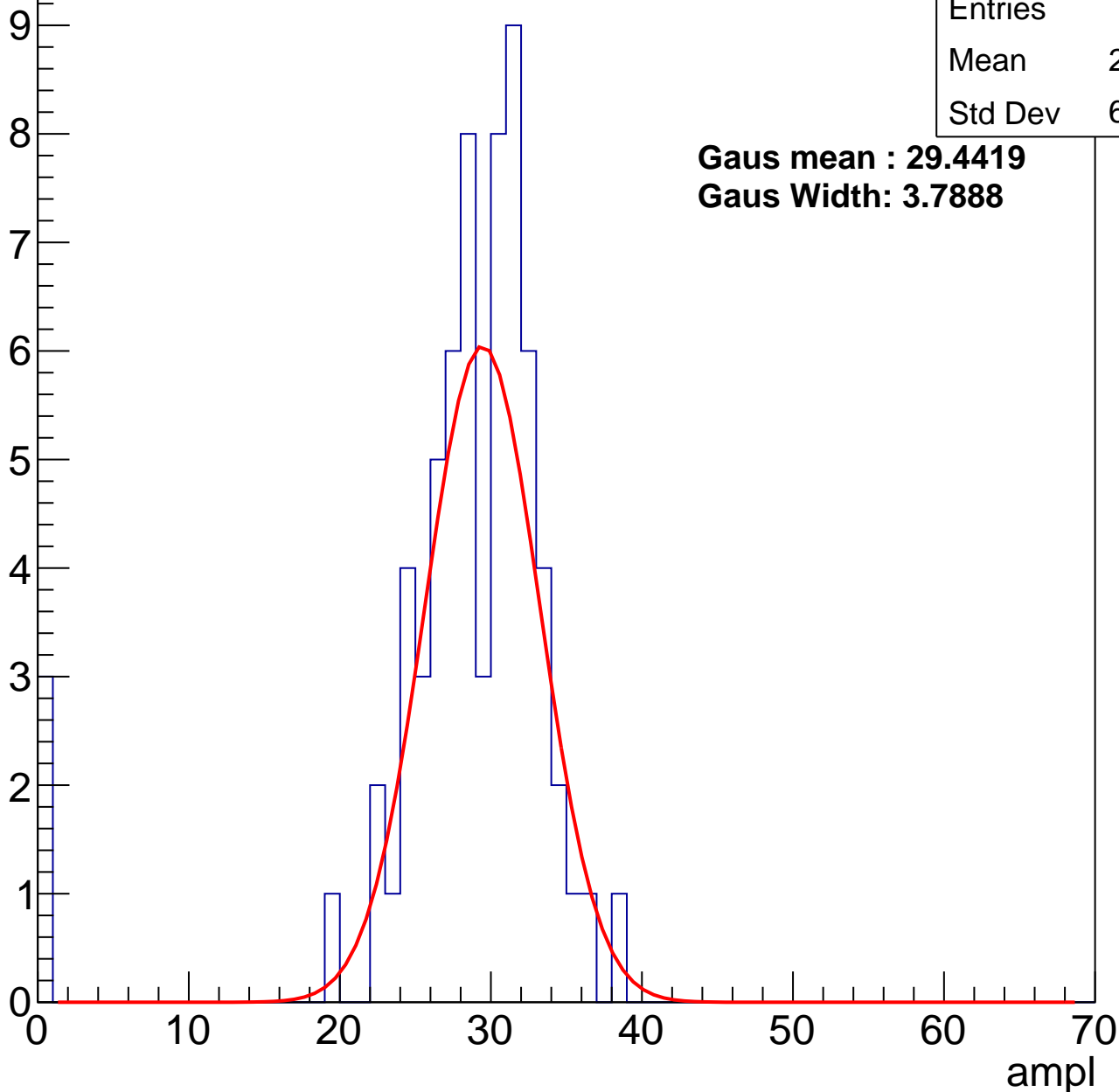
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 68    |
| Mean    | 27.65 |
| Std Dev | 6.898 |

**Gaus mean : 29.4419**

**Gaus Width: 3.7888**



# B0L001S, U2-ch118, adc1

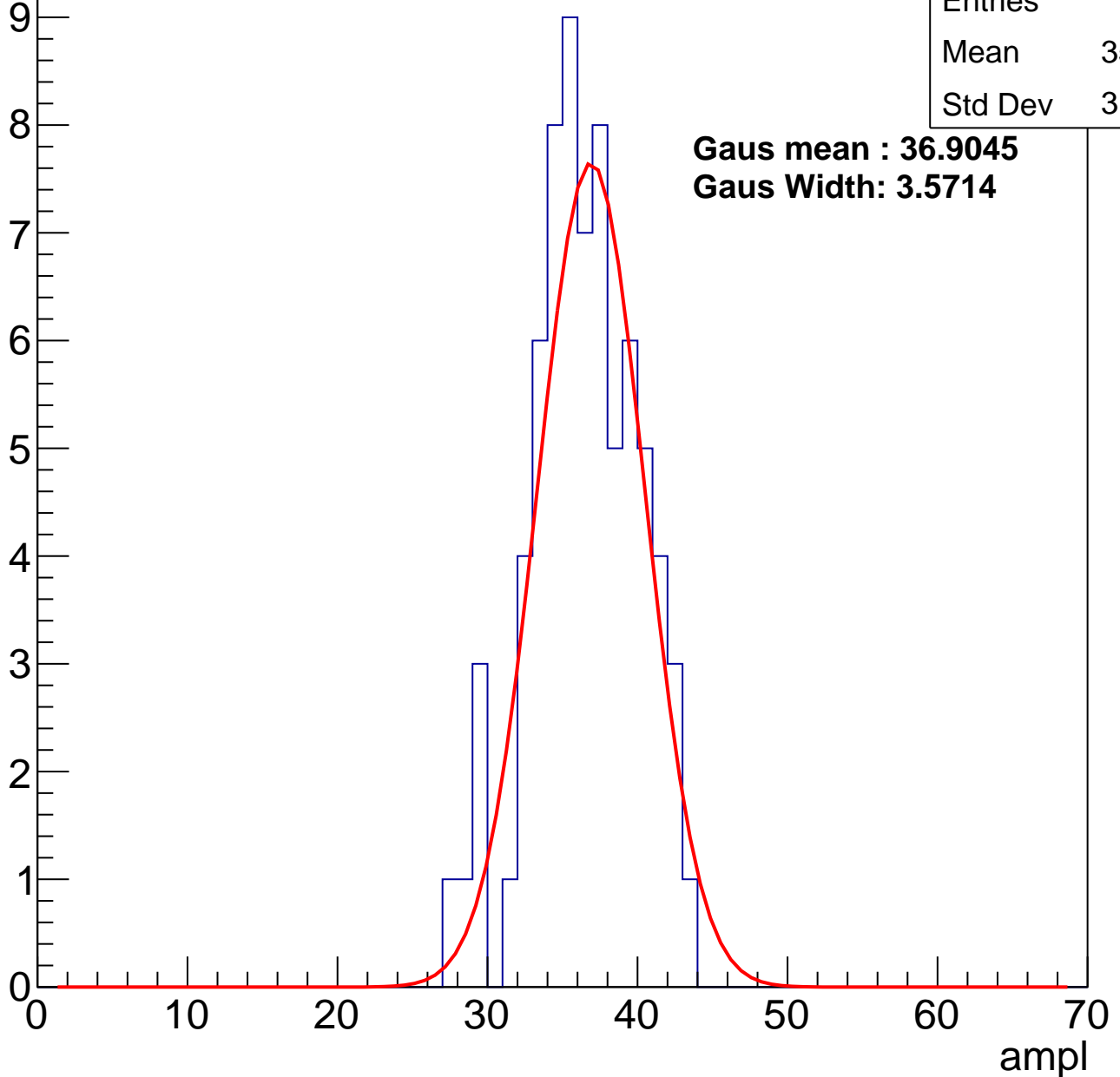
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 72    |
| Mean    | 35.99 |
| Std Dev | 3.526 |

**Gaus mean : 36.9045**

**Gaus Width: 3.5714**



# B0L001S, U2-ch118, adc2

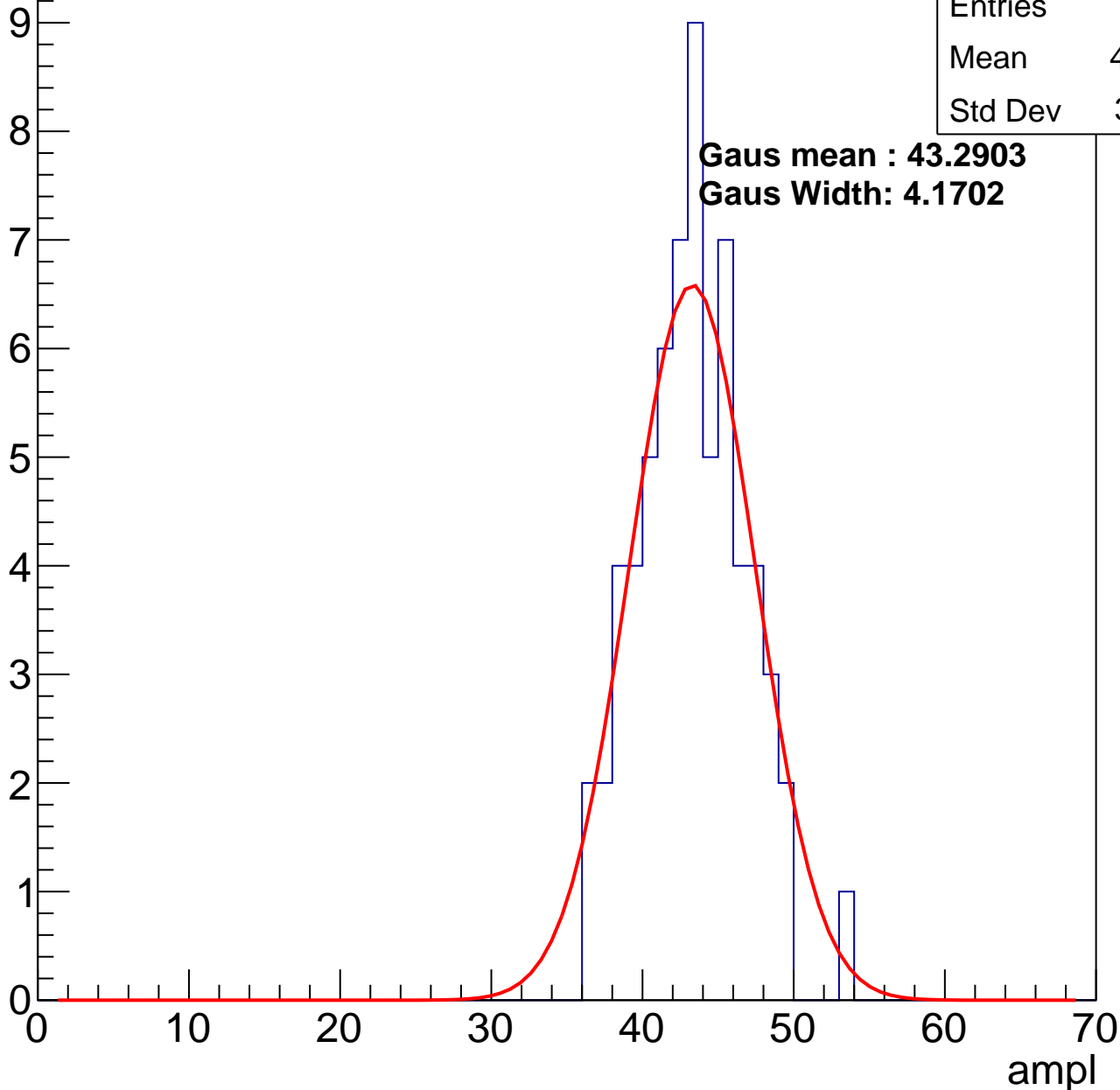
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 65    |
| Mean    | 42.82 |
| Std Dev | 3.481 |

**Gaus mean : 43.2903**

**Gaus Width: 4.1702**

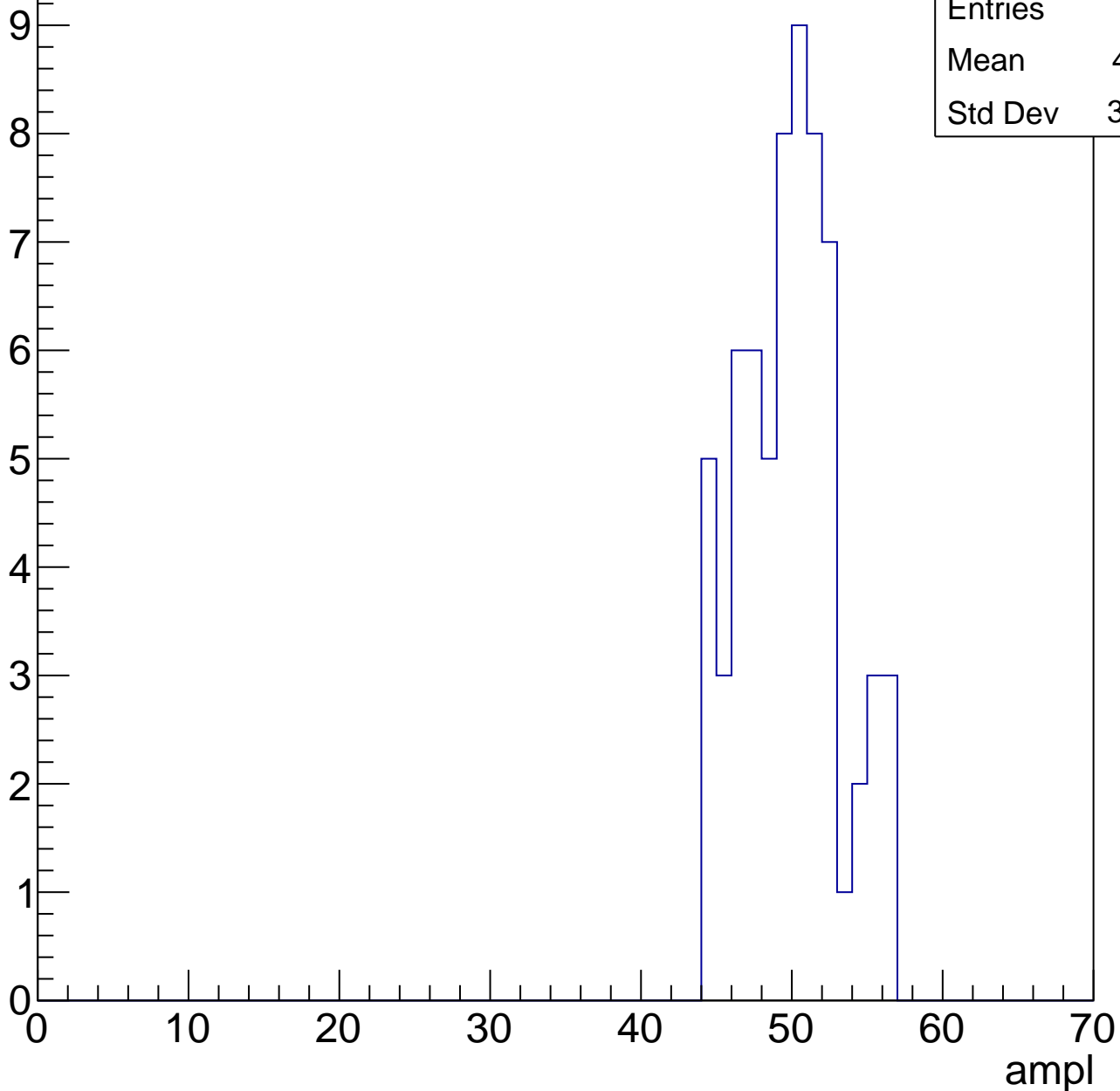


# B0L001S, U2-ch118, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 66    |
| Mean    | 49.41 |
| Std Dev | 3.186 |

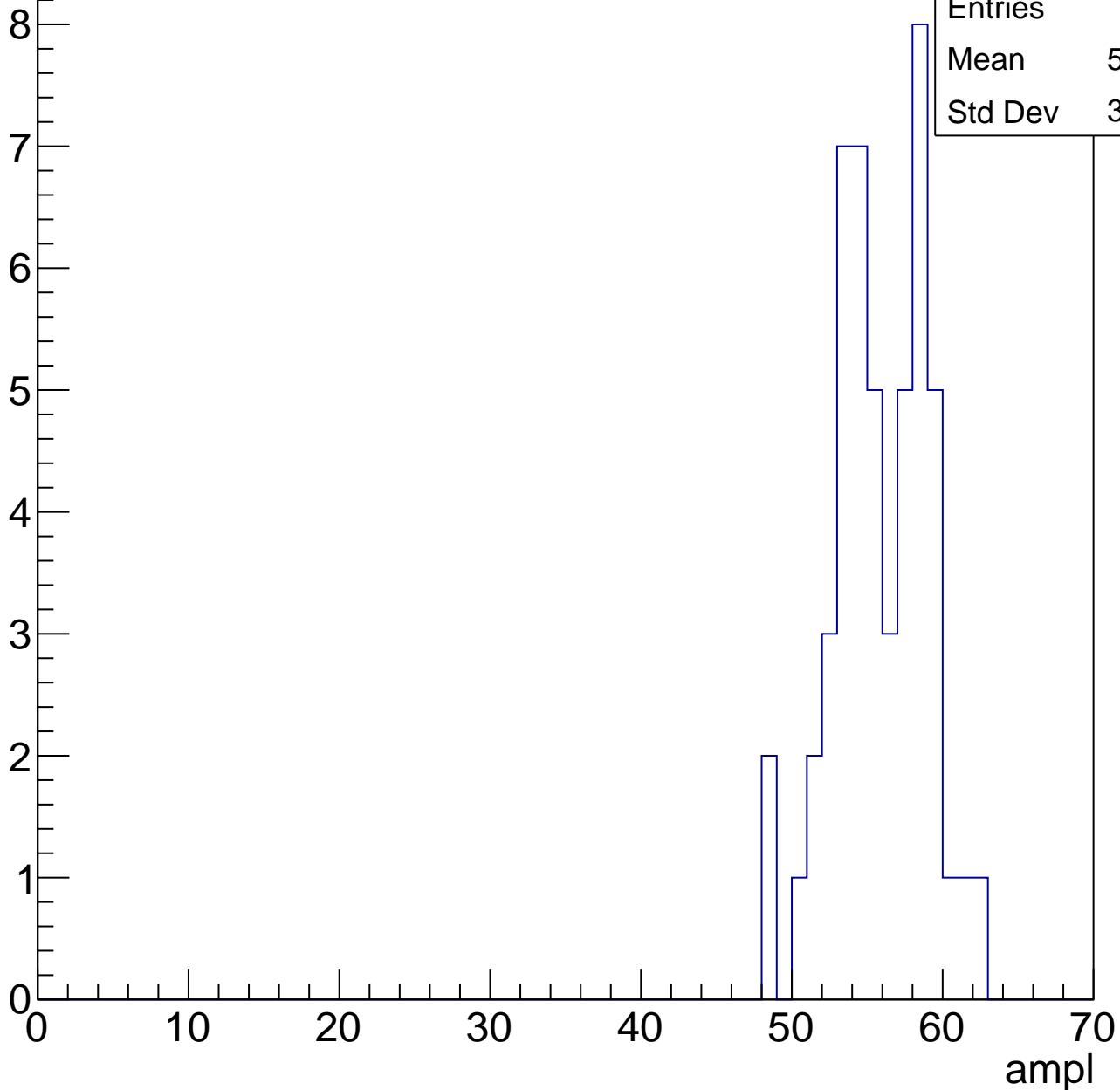


# B0L001S, U2-ch118, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 51    |
| Mean    | 55.35 |
| Std Dev | 3.117 |



# B0L001S, U2-ch118, adc5

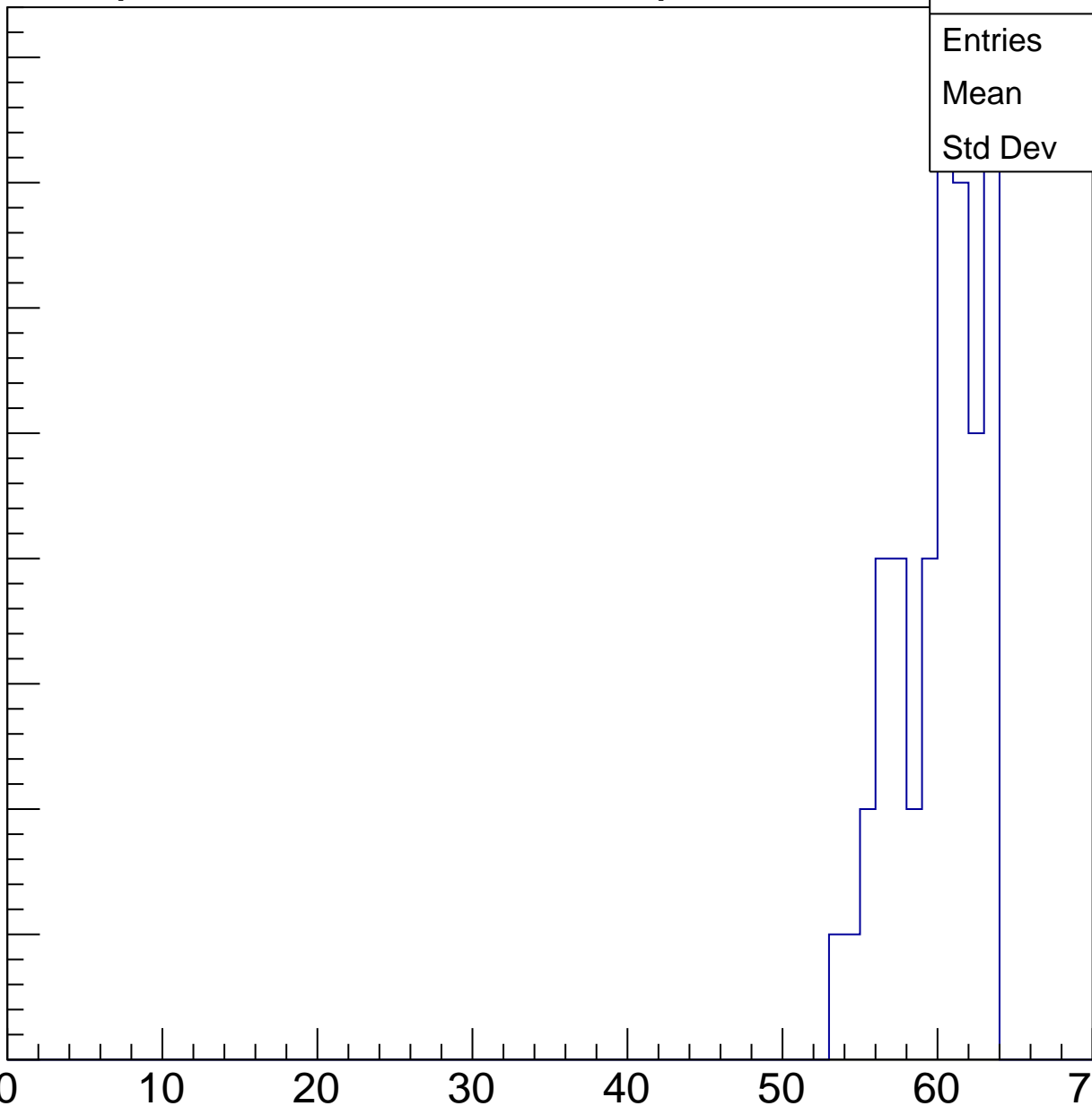
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

|         |       |
|---------|-------|
| Entries | 46    |
| Mean    | 59.61 |
| Std Dev | 2.715 |

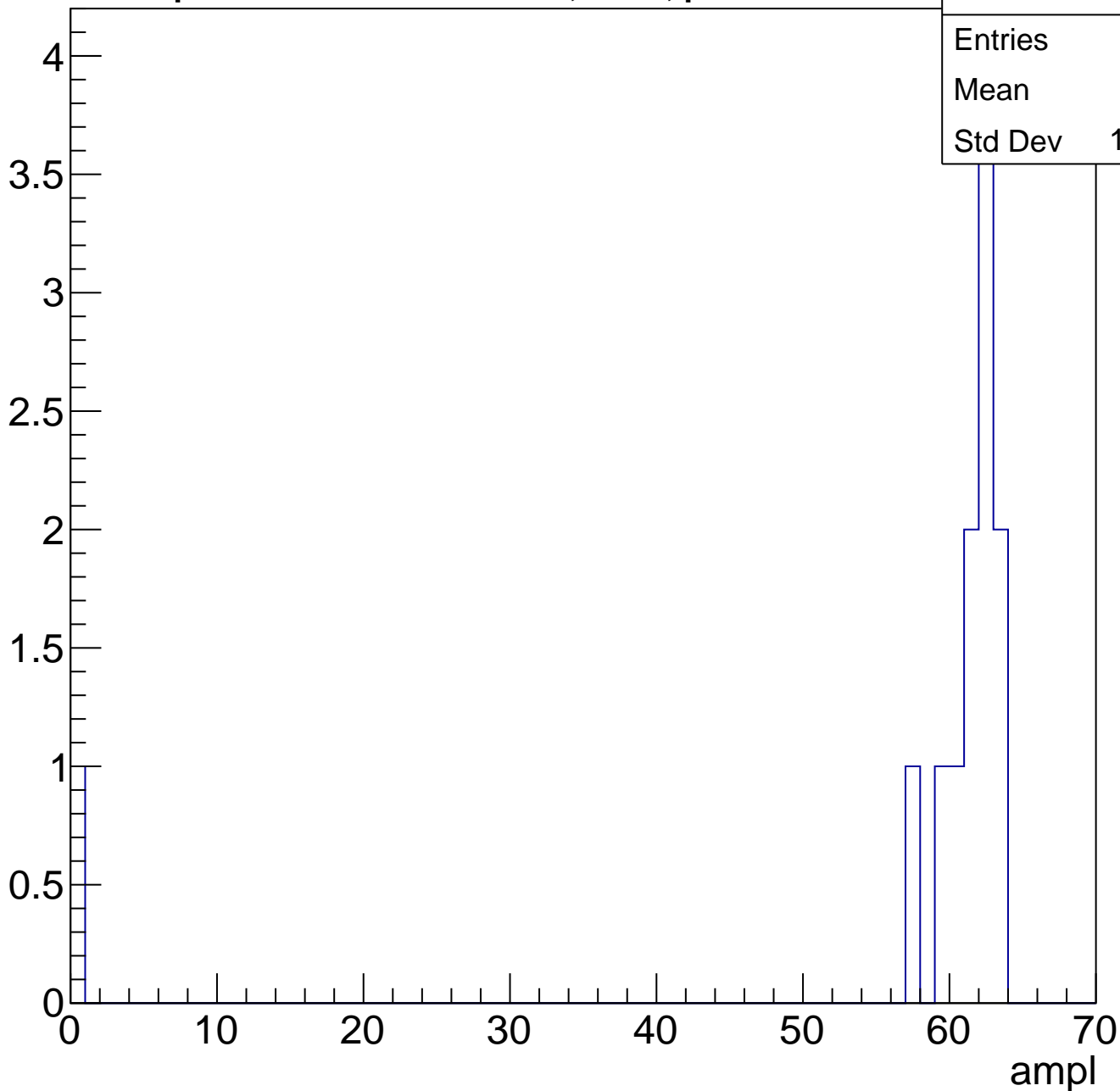
ampl



# B0L001S, U2-ch118, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch118, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 2 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch119, adc0

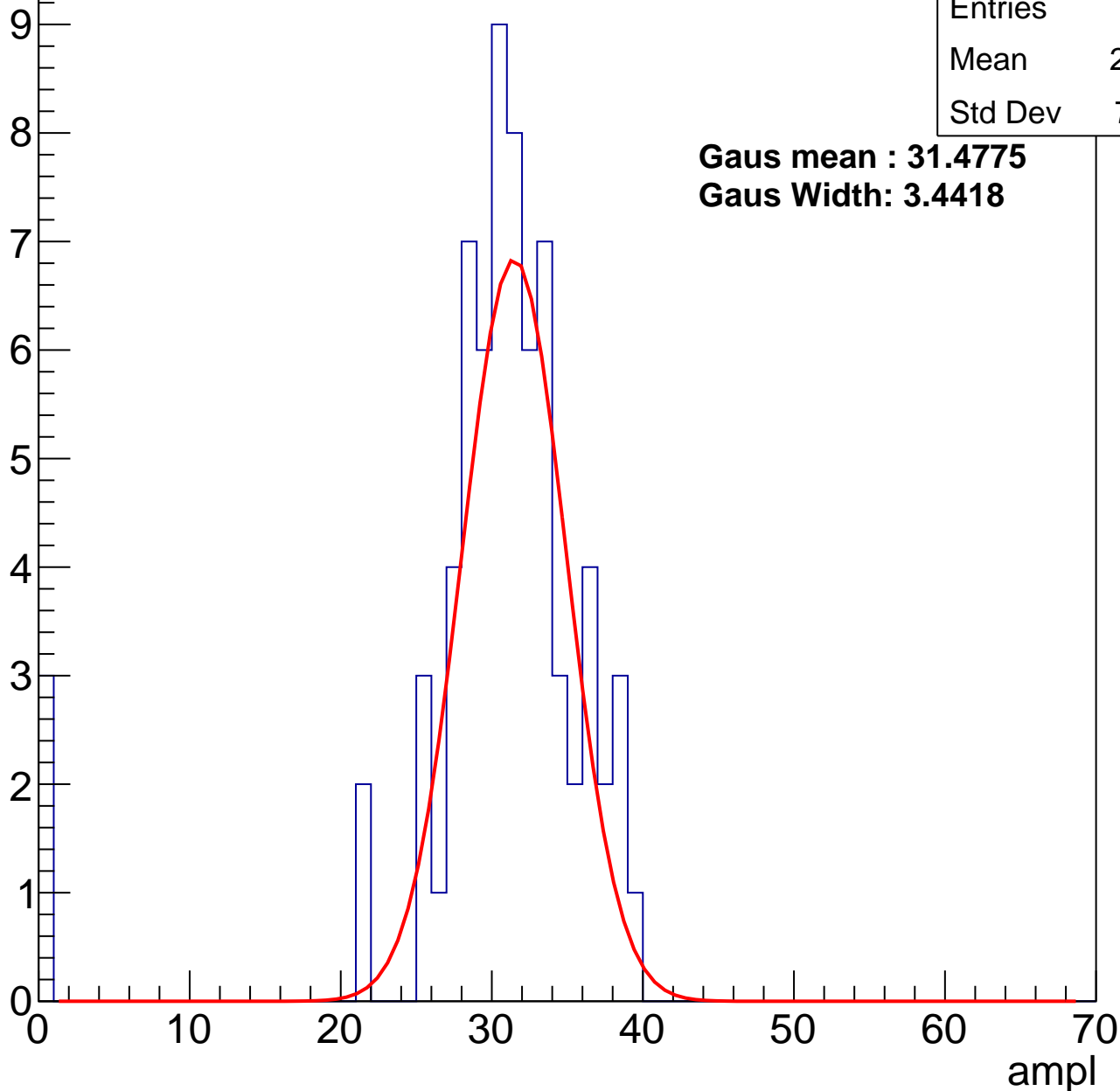
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 71    |
| Mean    | 29.65 |
| Std Dev | 7.241 |

**Gaus mean : 31.4775**

**Gaus Width: 3.4418**



# B0L001S, U2-ch119, adc1

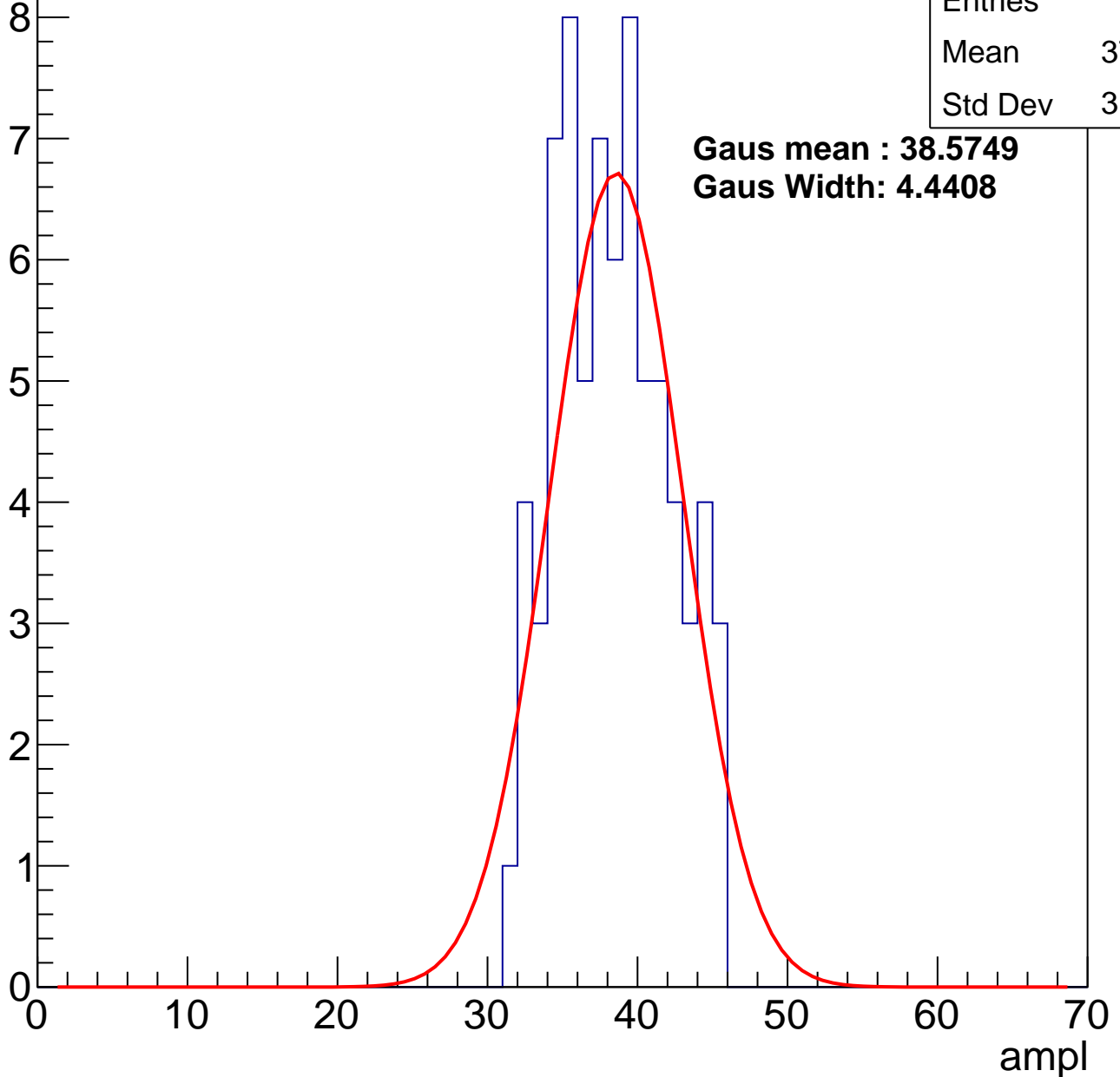
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 73    |
| Mean    | 37.92 |
| Std Dev | 3.667 |

**Gaus mean : 38.5749**

**Gaus Width: 4.4408**



# B0L001S, U2-ch119, adc2

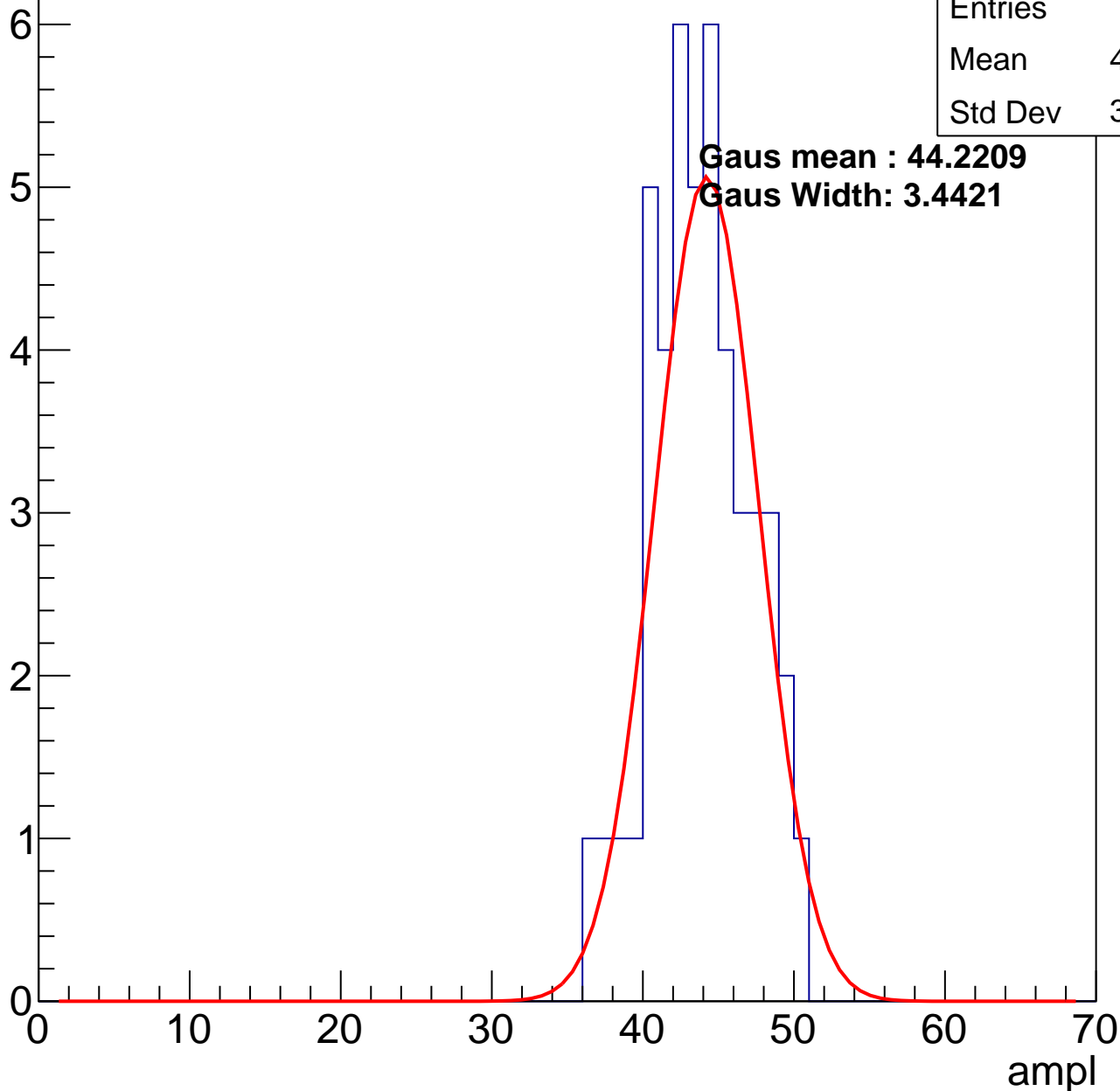
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 46    |
| Mean    | 43.39 |
| Std Dev | 3.227 |

**Gaus mean : 44.2209**

**Gaus Width: 3.4421**

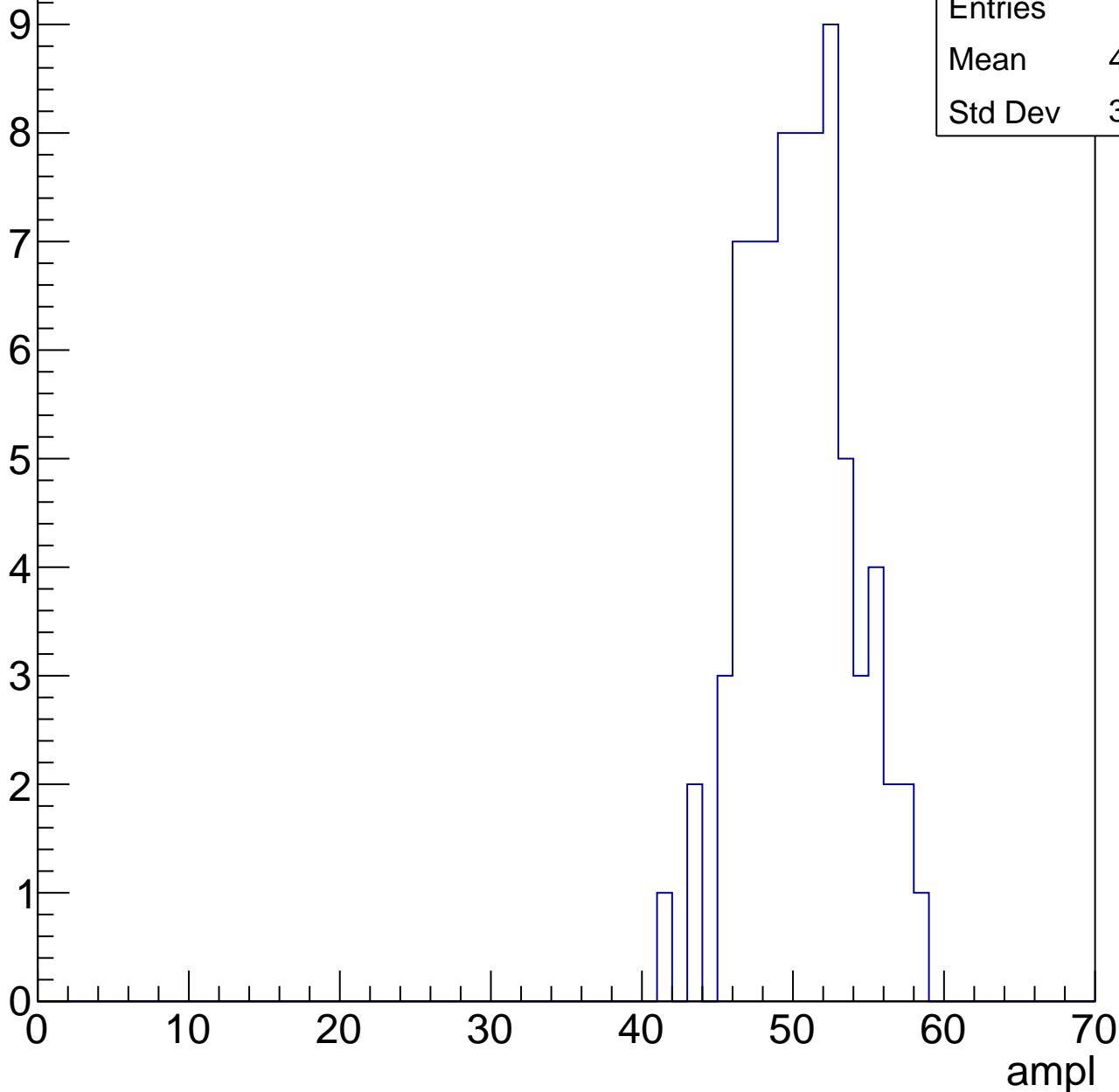


# B0L001S, U2-ch119, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 77    |
| Mean    | 49.97 |
| Std Dev | 3.486 |



# B0L001S, U2-ch119, adc4

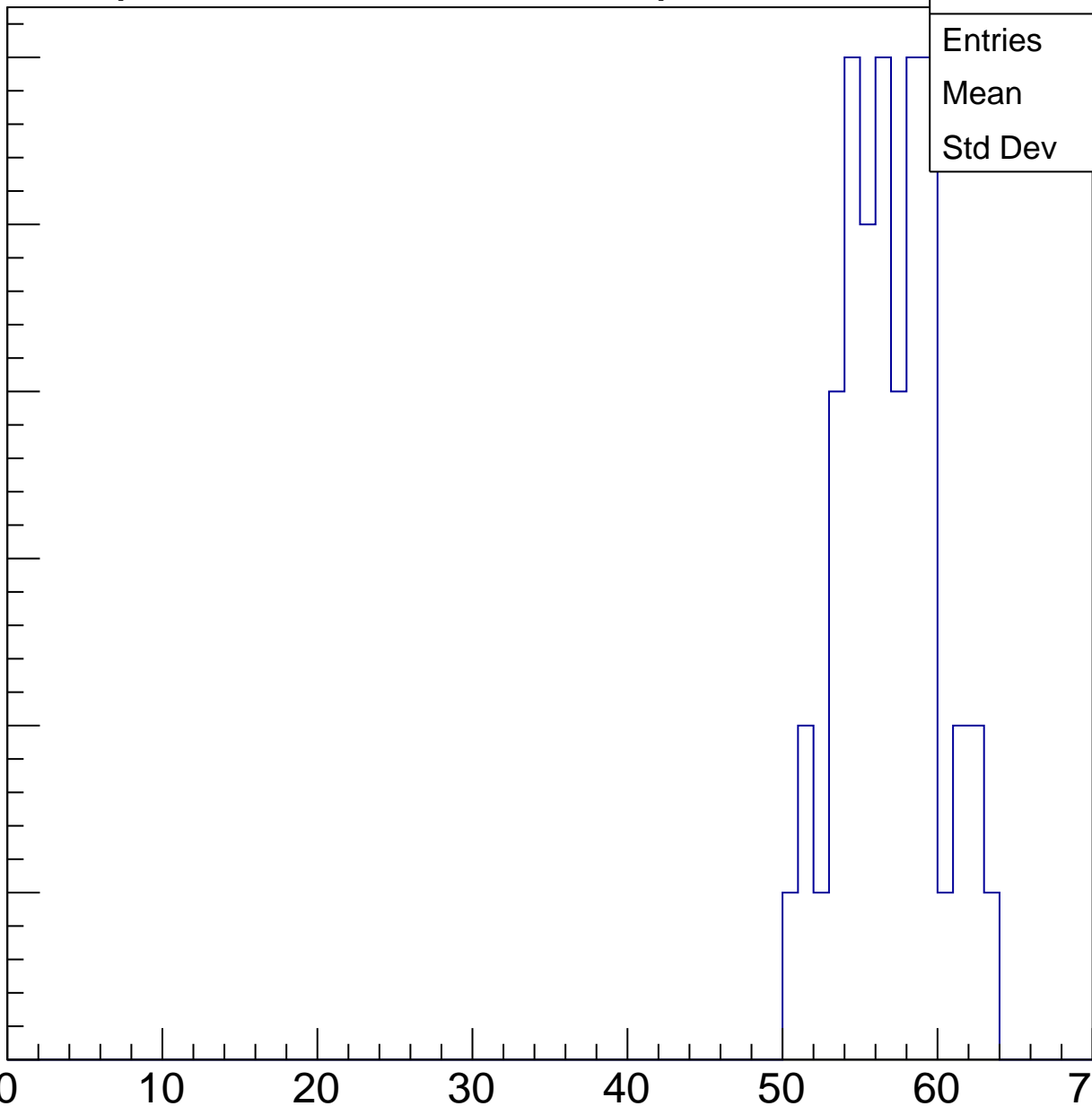
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

6  
5  
4  
3  
2  
1  
0

|         |       |
|---------|-------|
| Entries | 47    |
| Mean    | 56.38 |
| Std Dev | 3.022 |

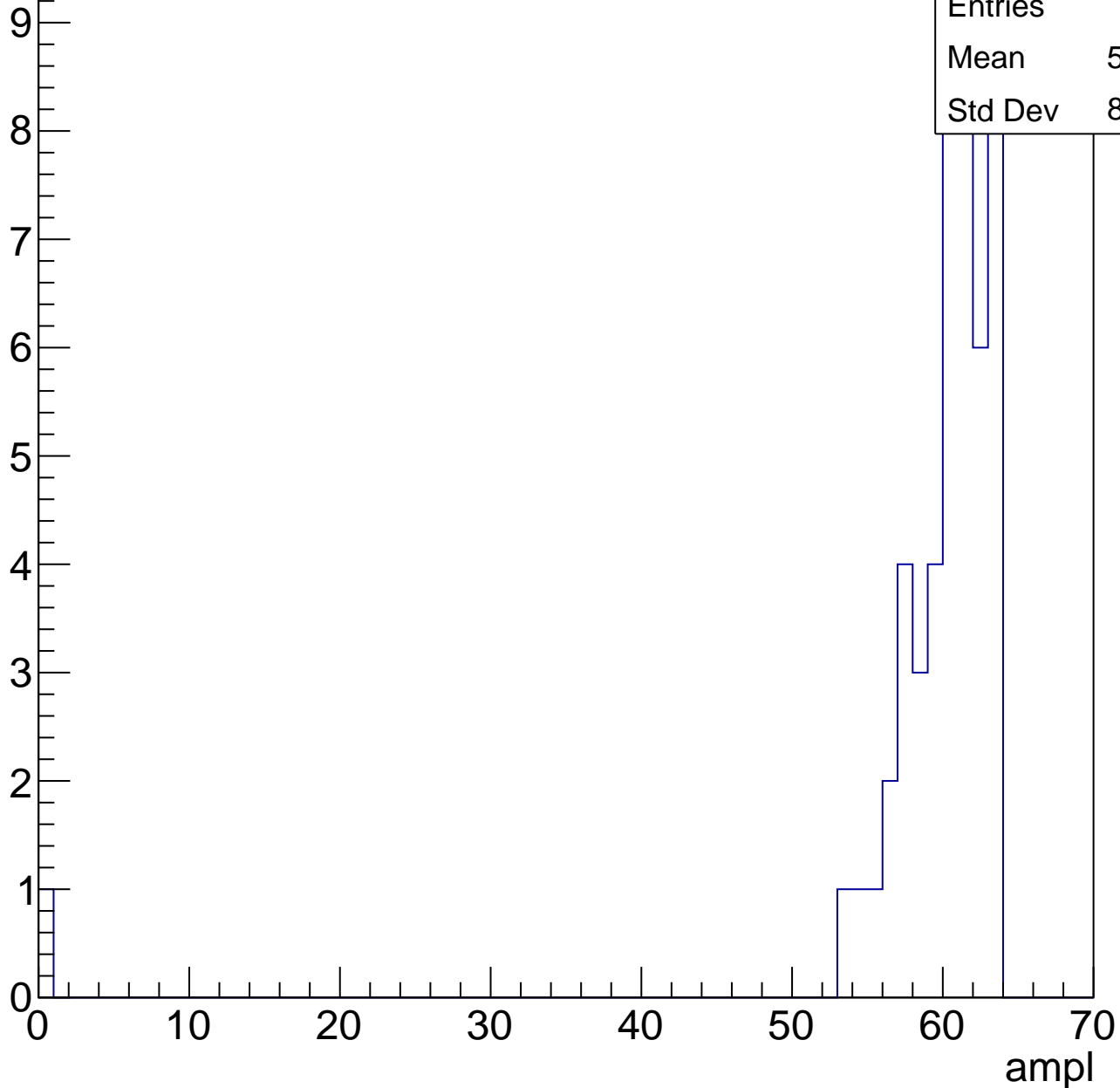
ampl



# B0L001S, U2-ch119, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U2-ch119, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

|         |        |
|---------|--------|
| Entries | 3      |
| Mean    | 62.33  |
| Std Dev | 0.4714 |

ampl





# B0L001S, U2-ch119, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 0 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch120, adc0

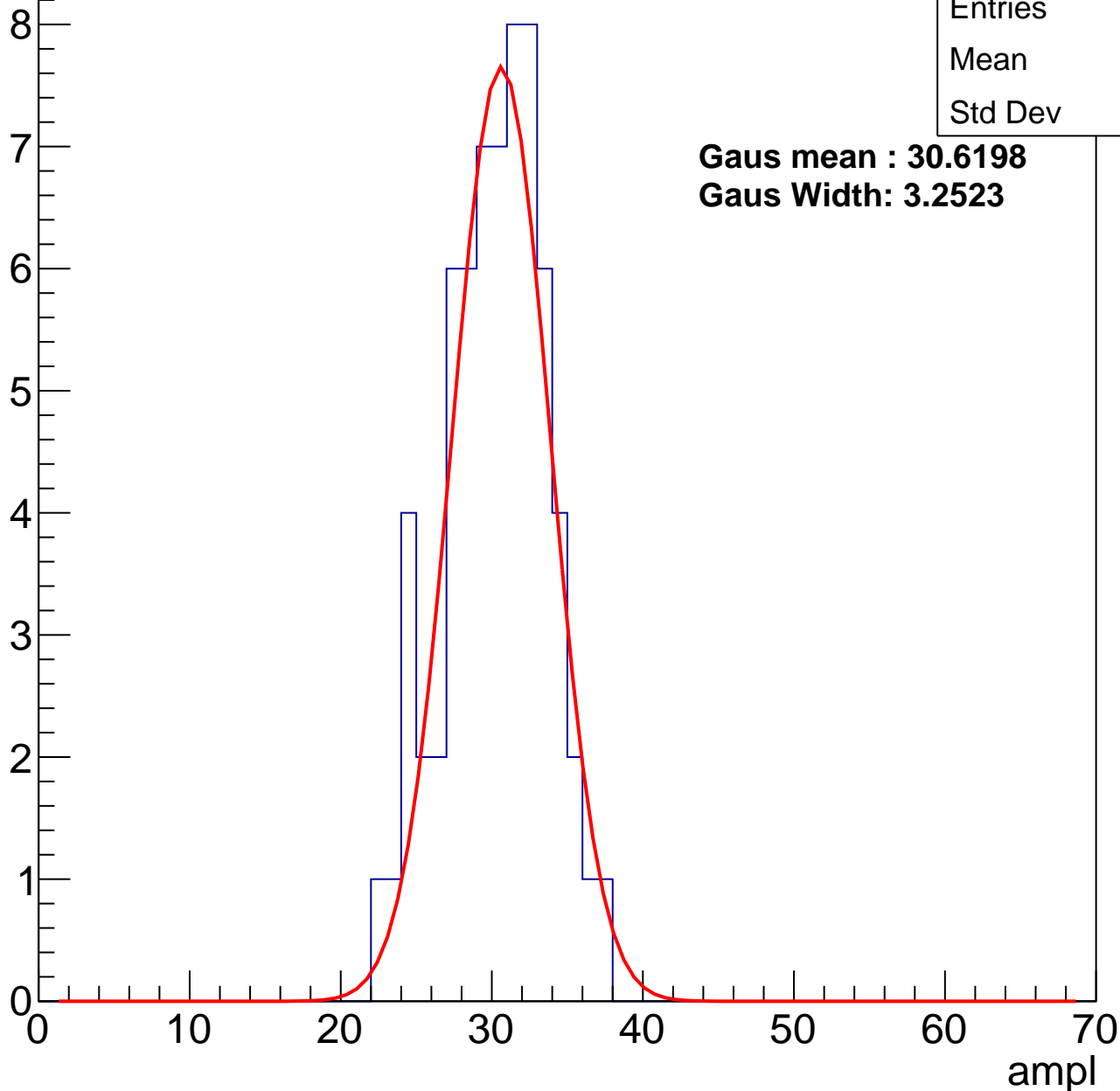
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |      |
|---------|------|
| Entries | 66   |
| Mean    | 29.8 |
| Std Dev | 3.29 |

**Gaus mean : 30.6198**

**Gaus Width: 3.2523**



# B0L001S, U2-ch120, adc1

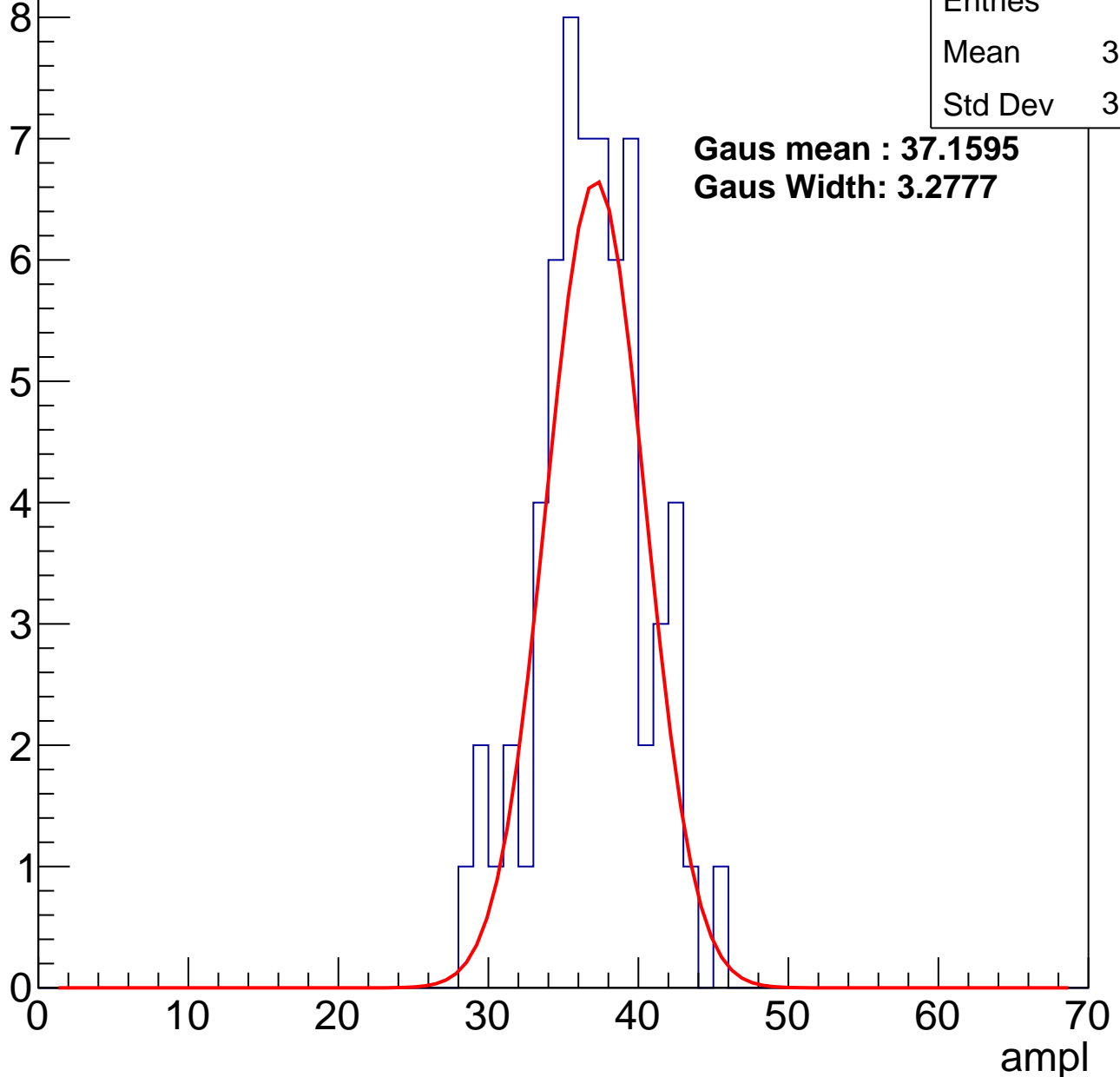
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 63    |
| Mean    | 36.46 |
| Std Dev | 3.549 |

**Gaus mean : 37.1595**

**Gaus Width: 3.2777**



# B0L001S, U2-ch120, adc2

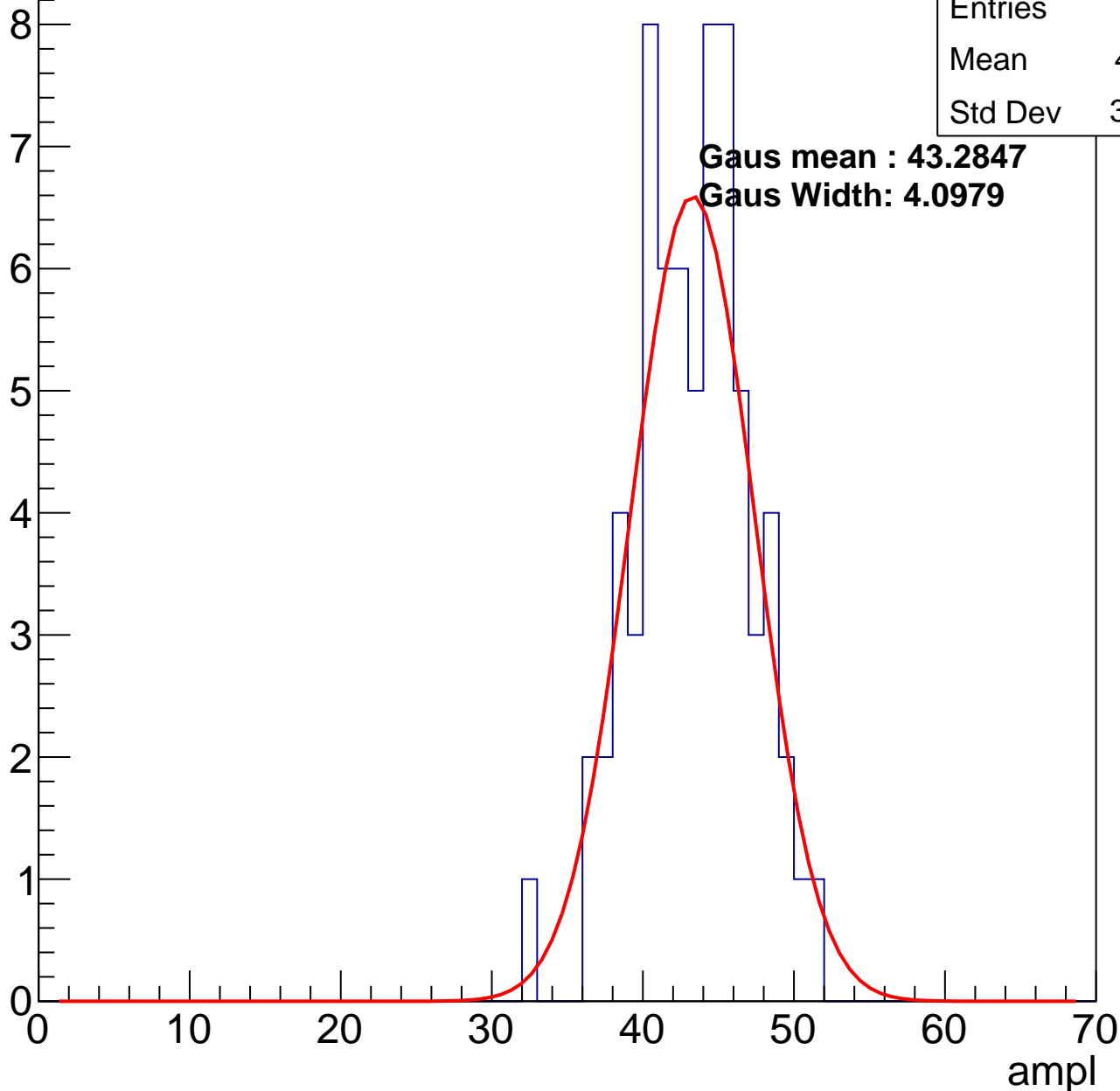
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 69    |
| Mean    | 42.81 |
| Std Dev | 3.723 |

**Gaus mean : 43.2847**

**Gaus Width: 4.0979**

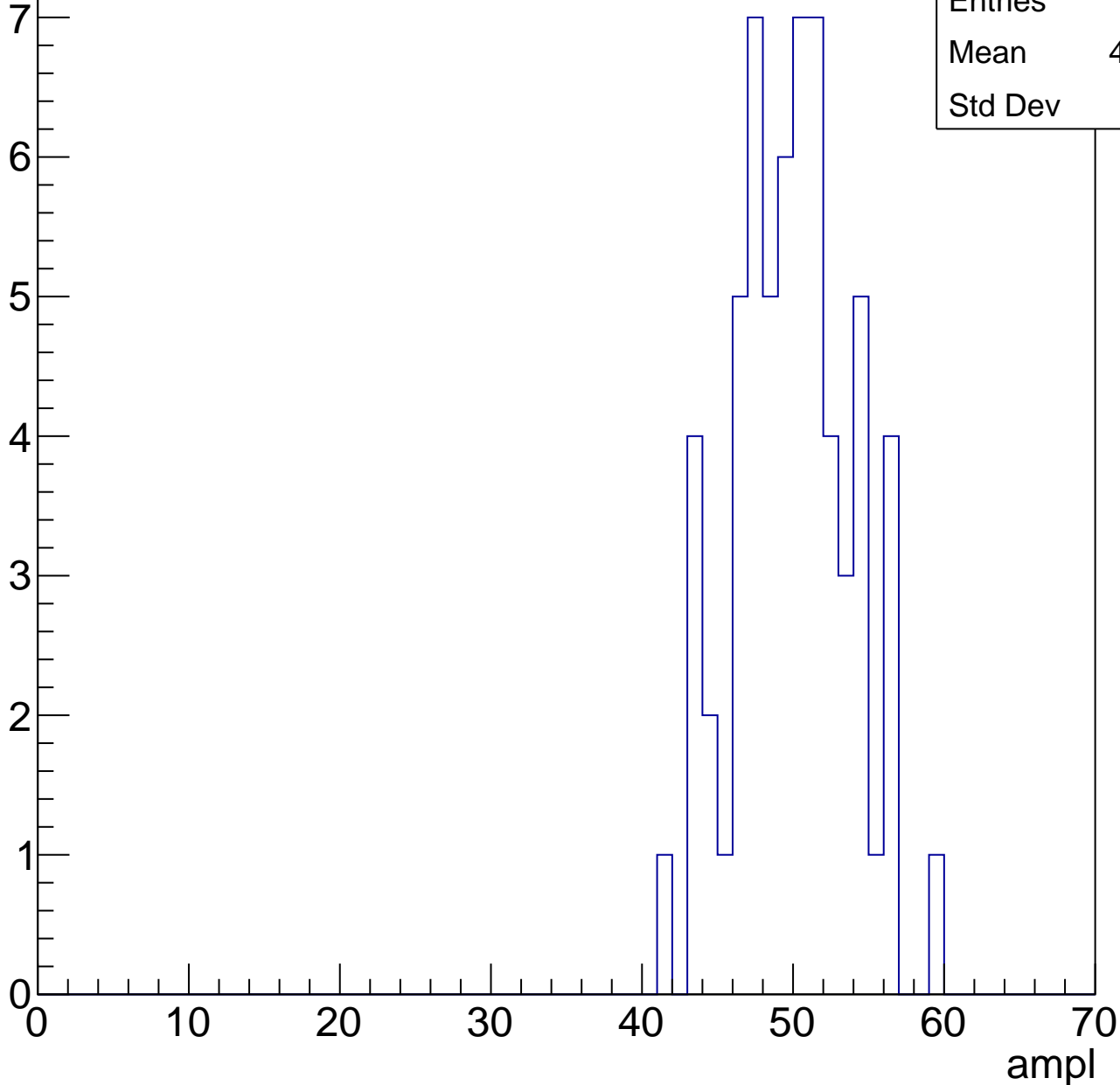


# B0L001S, U2-ch120, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

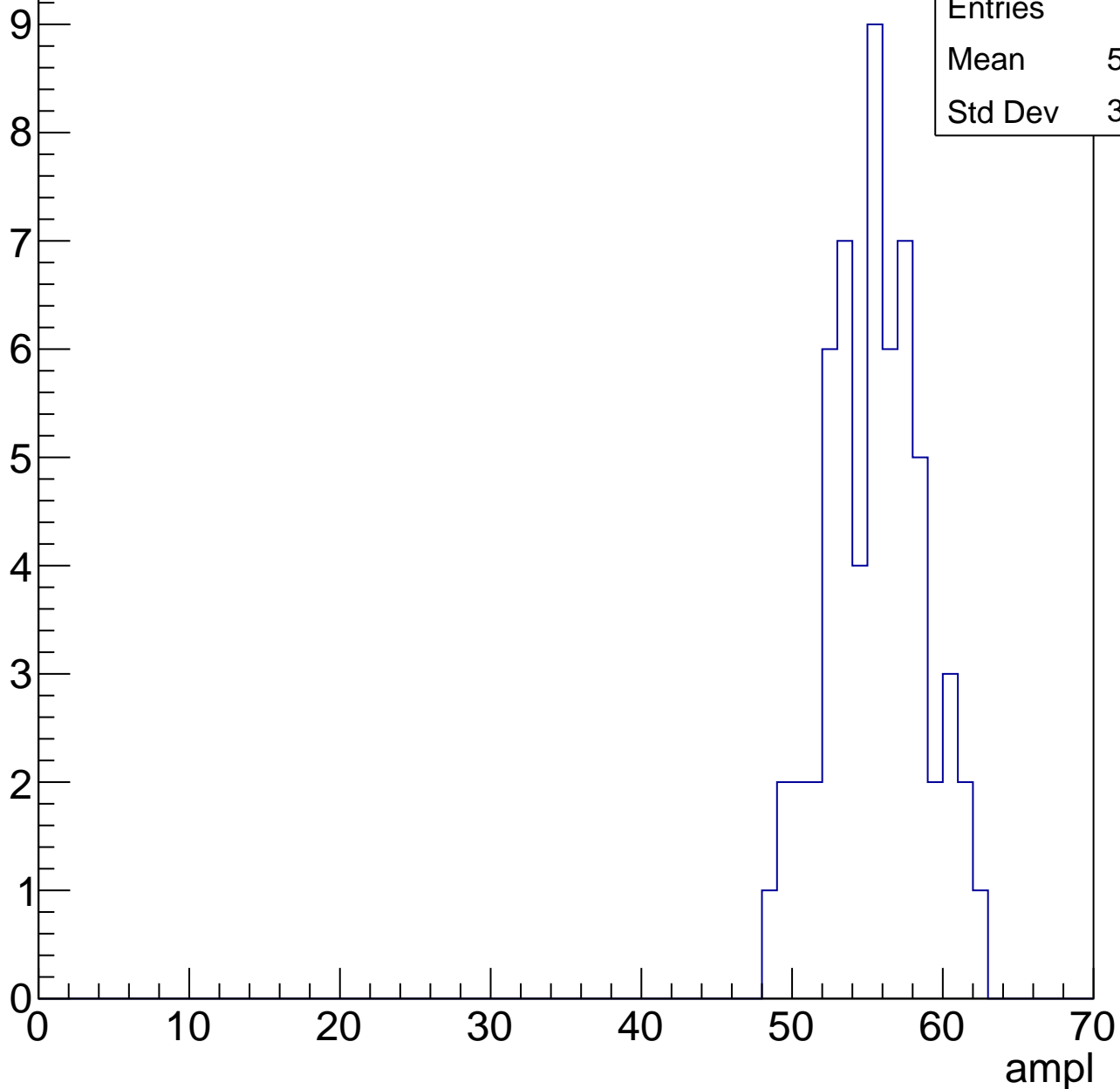
|         |       |
|---------|-------|
| Entries | 63    |
| Mean    | 49.54 |
| Std Dev | 3.8   |



# B0L001S, U2-ch120, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

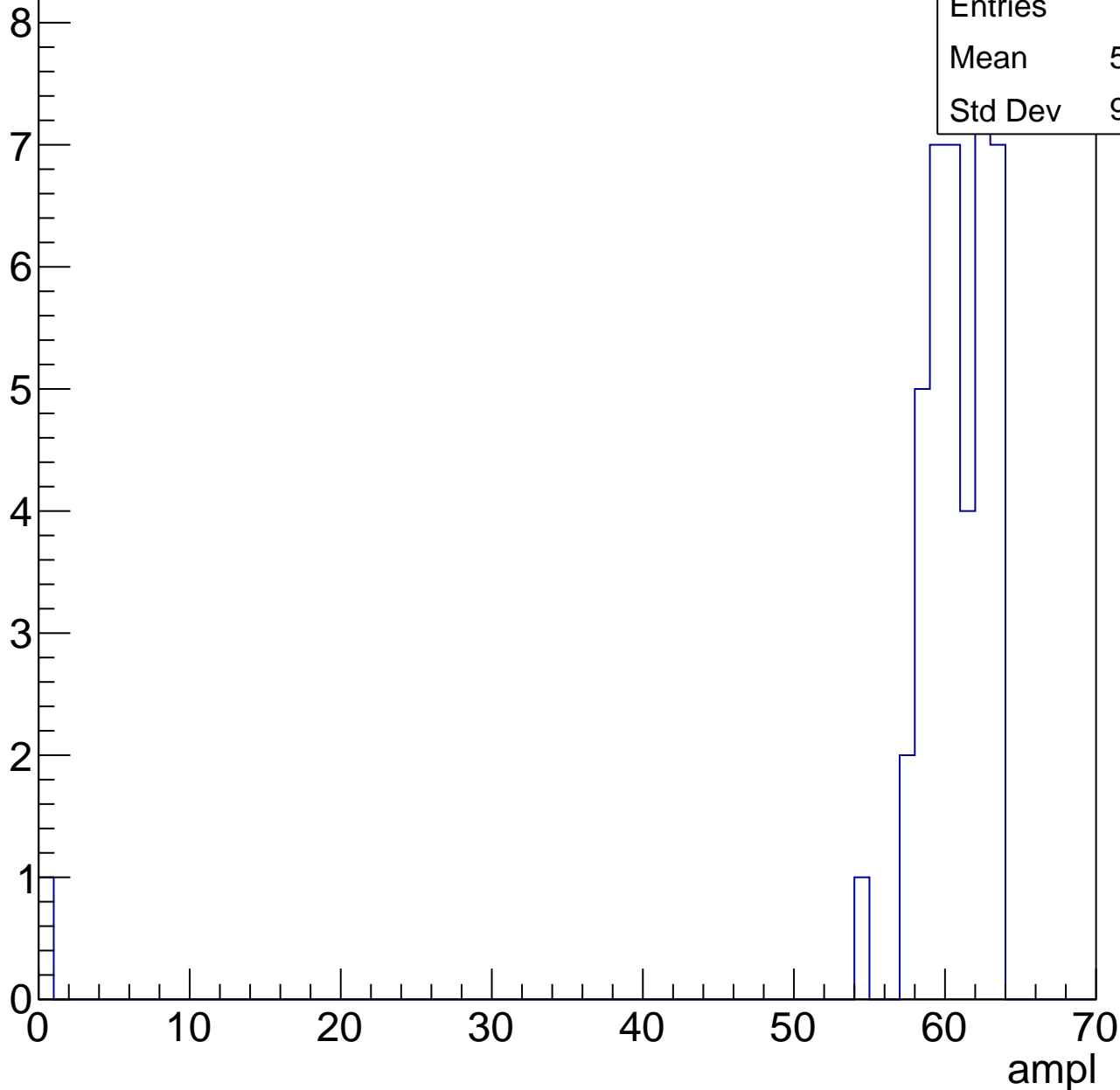


# B0L001S, U2-ch120, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

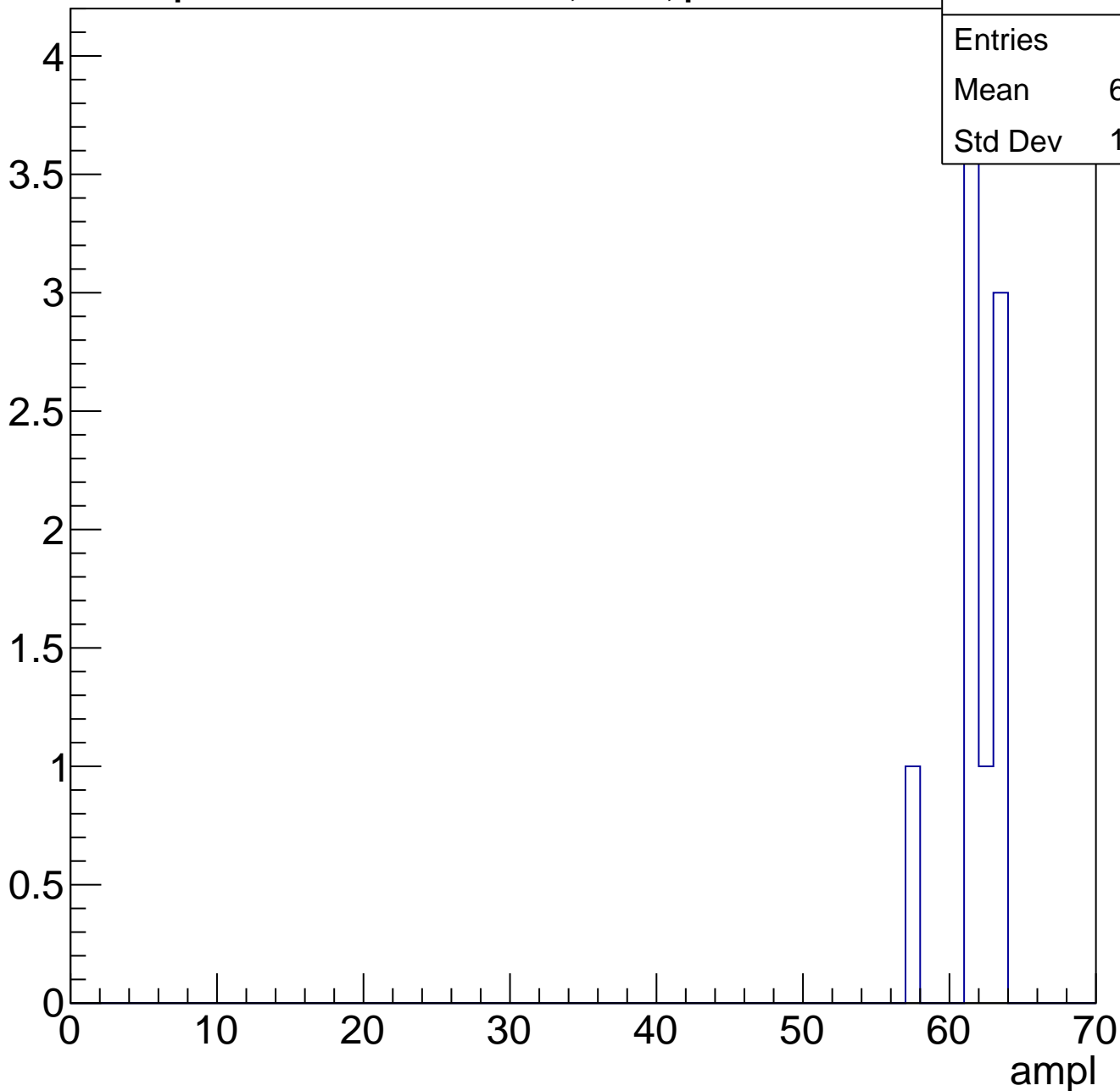
|         |       |
|---------|-------|
| Entries | 42    |
| Mean    | 58.86 |
| Std Dev | 9.418 |



# B0L001S, U2-ch120, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch120, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |    |
|---------|----|
| Entries | 2  |
| Mean    | 11 |
| Std Dev | 11 |

# B0L001S, U2-ch121, adc0

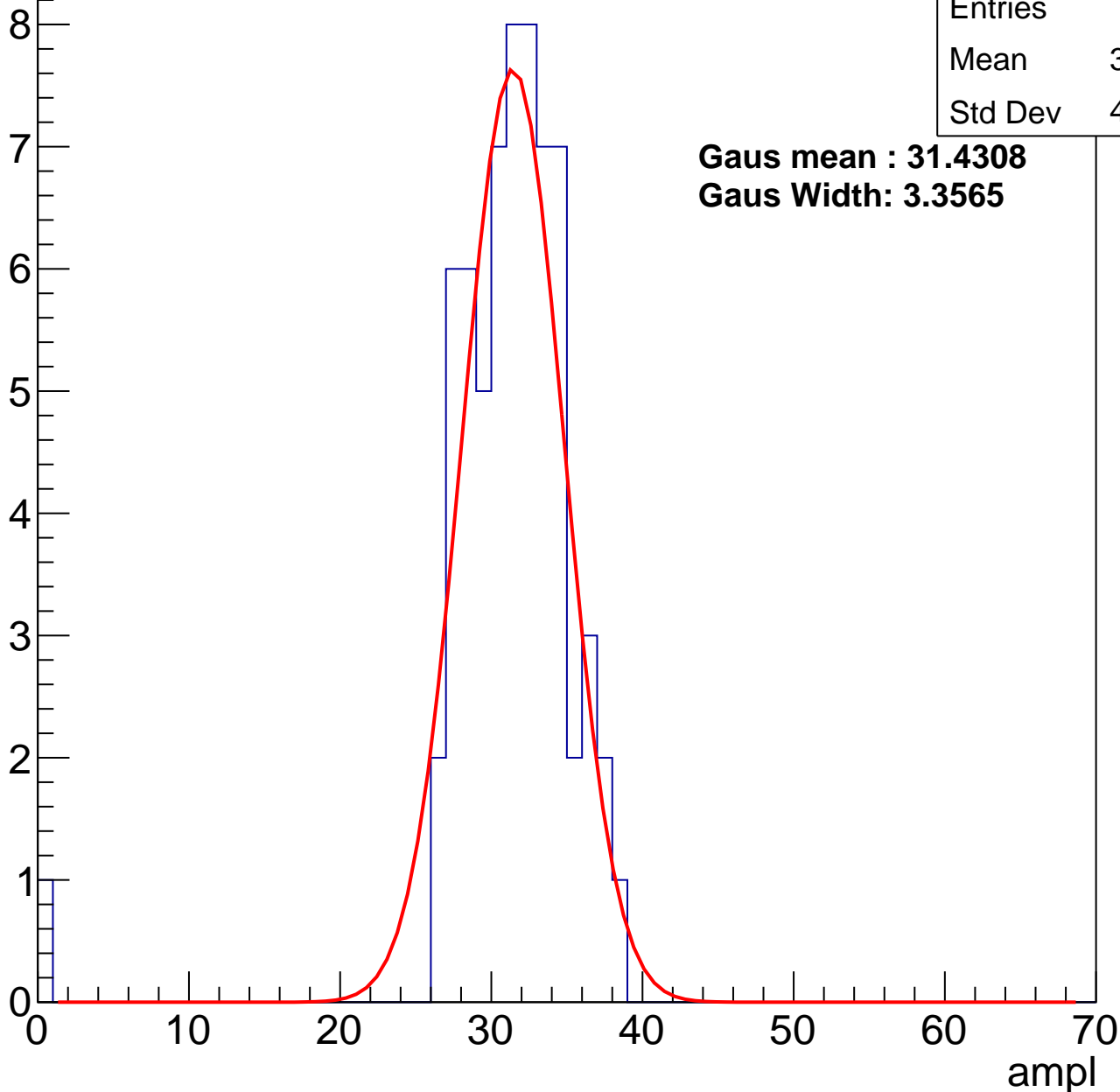
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 65    |
| Mean    | 30.77 |
| Std Dev | 4.822 |

**Gaus mean : 31.4308**

**Gaus Width: 3.3565**



# B0L001S, U2-ch121, adc1

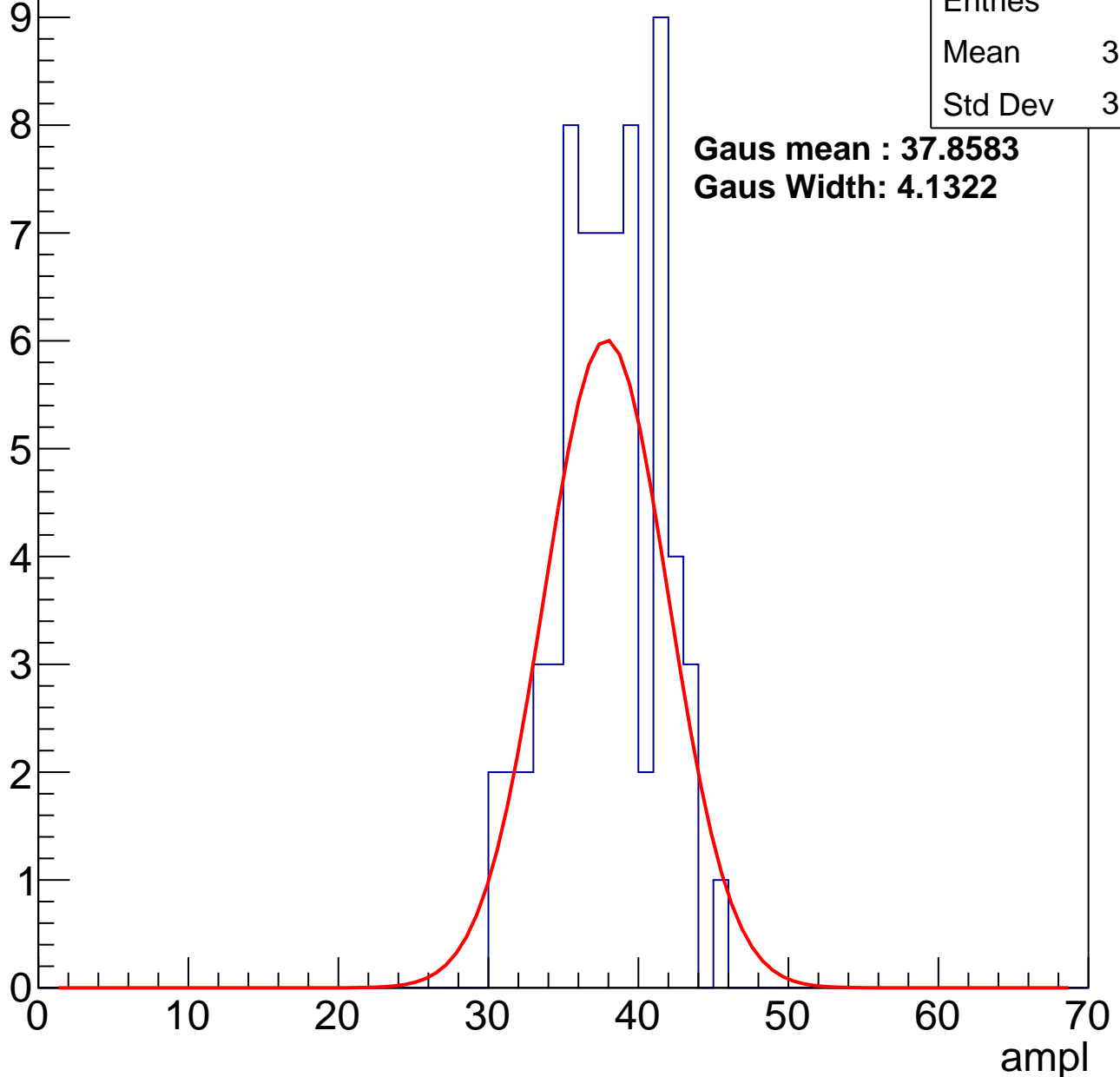
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 68    |
| Mean    | 37.46 |
| Std Dev | 3.415 |

**Gaus mean : 37.8583**

**Gaus Width: 4.1322**



# B0L001S, U2-ch121, adc2

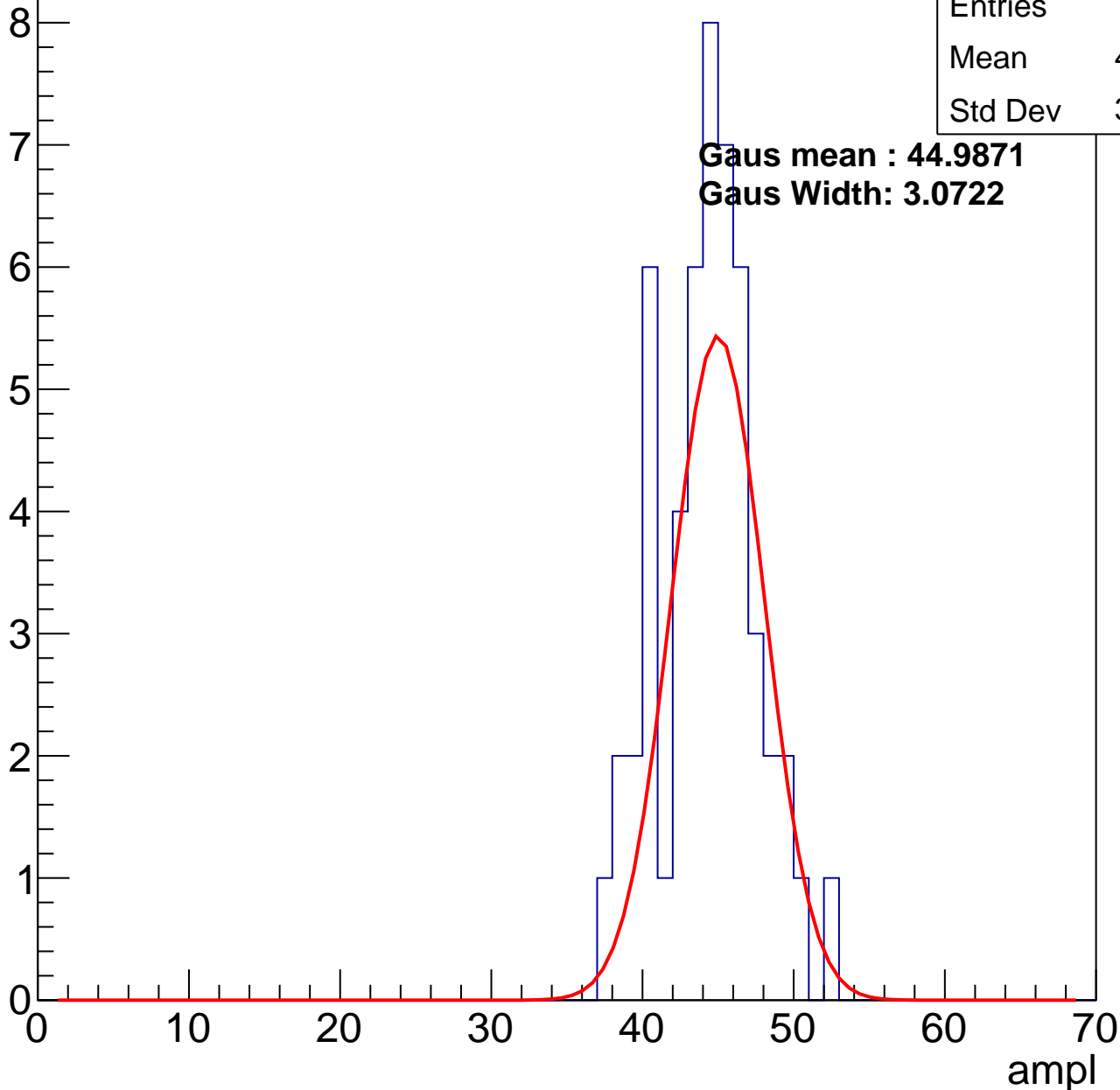
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 52    |
| Mean    | 43.81 |
| Std Dev | 3.211 |

**Gaus mean : 44.9871**

**Gaus Width: 3.0722**

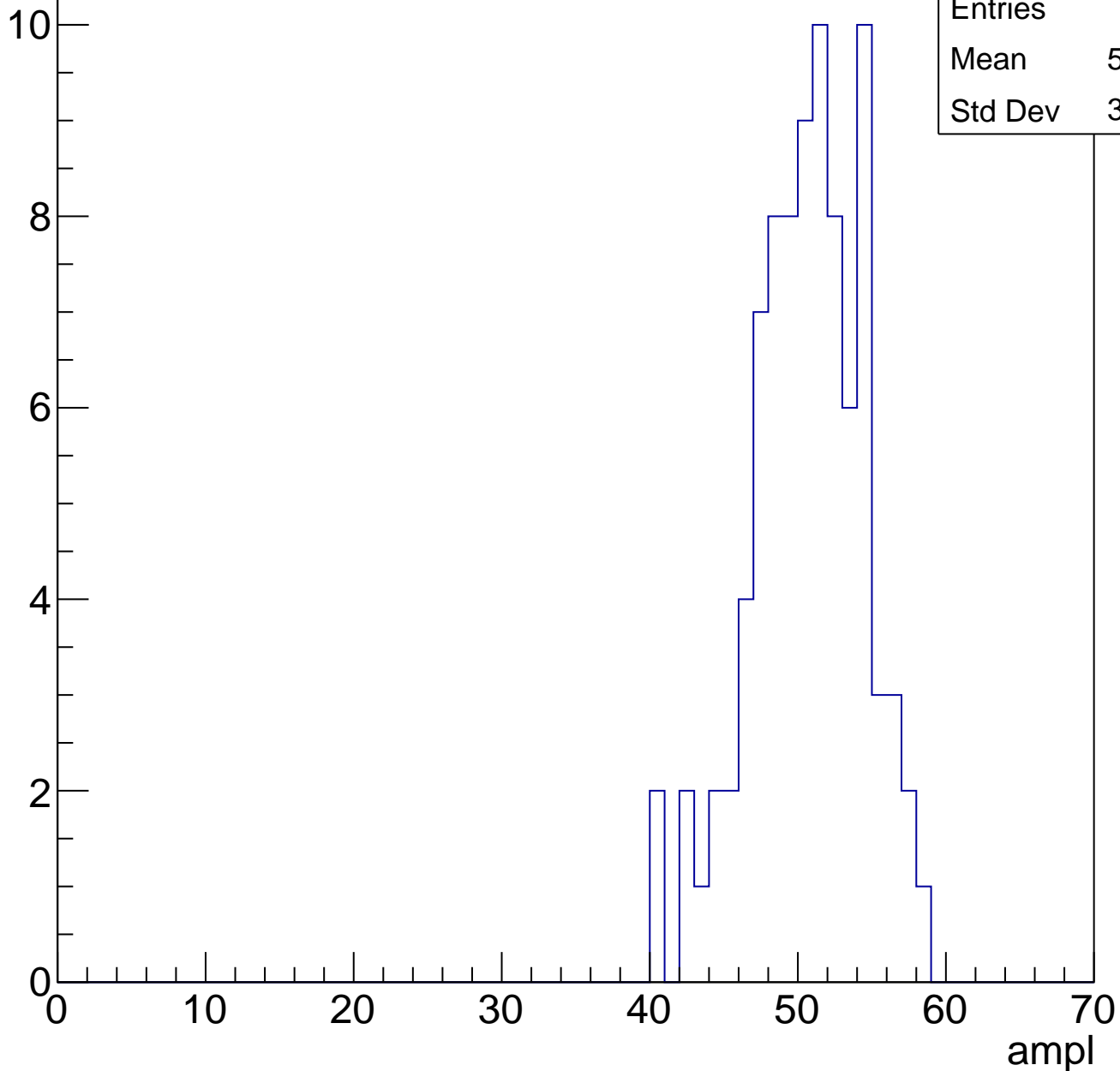


# B0L001S, U2-ch121, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 88    |
| Mean    | 50.15 |
| Std Dev | 3.792 |

Entry

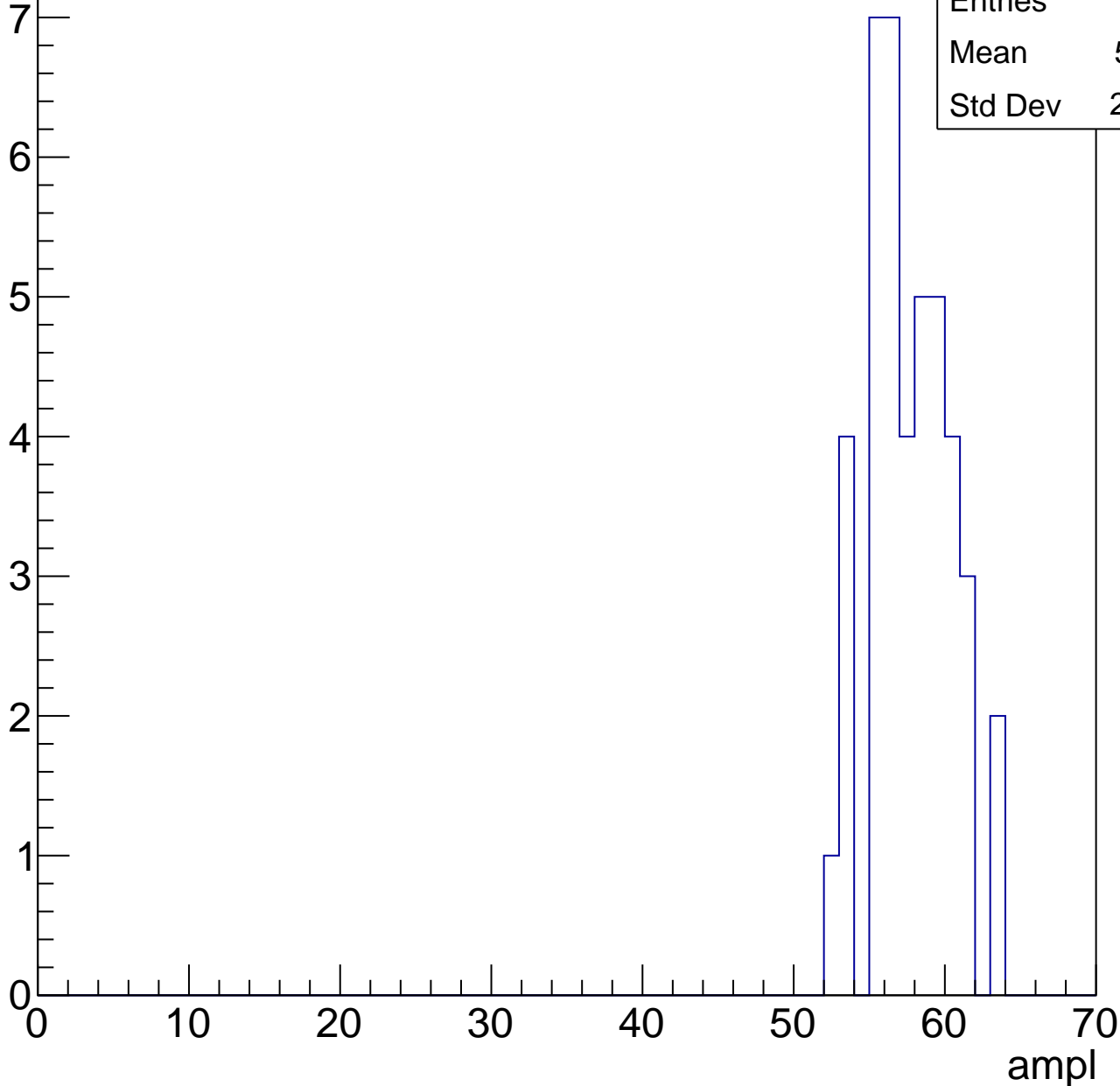


# B0L001S, U2-ch121, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 42    |
| Mean    | 57.21 |
| Std Dev | 2.686 |

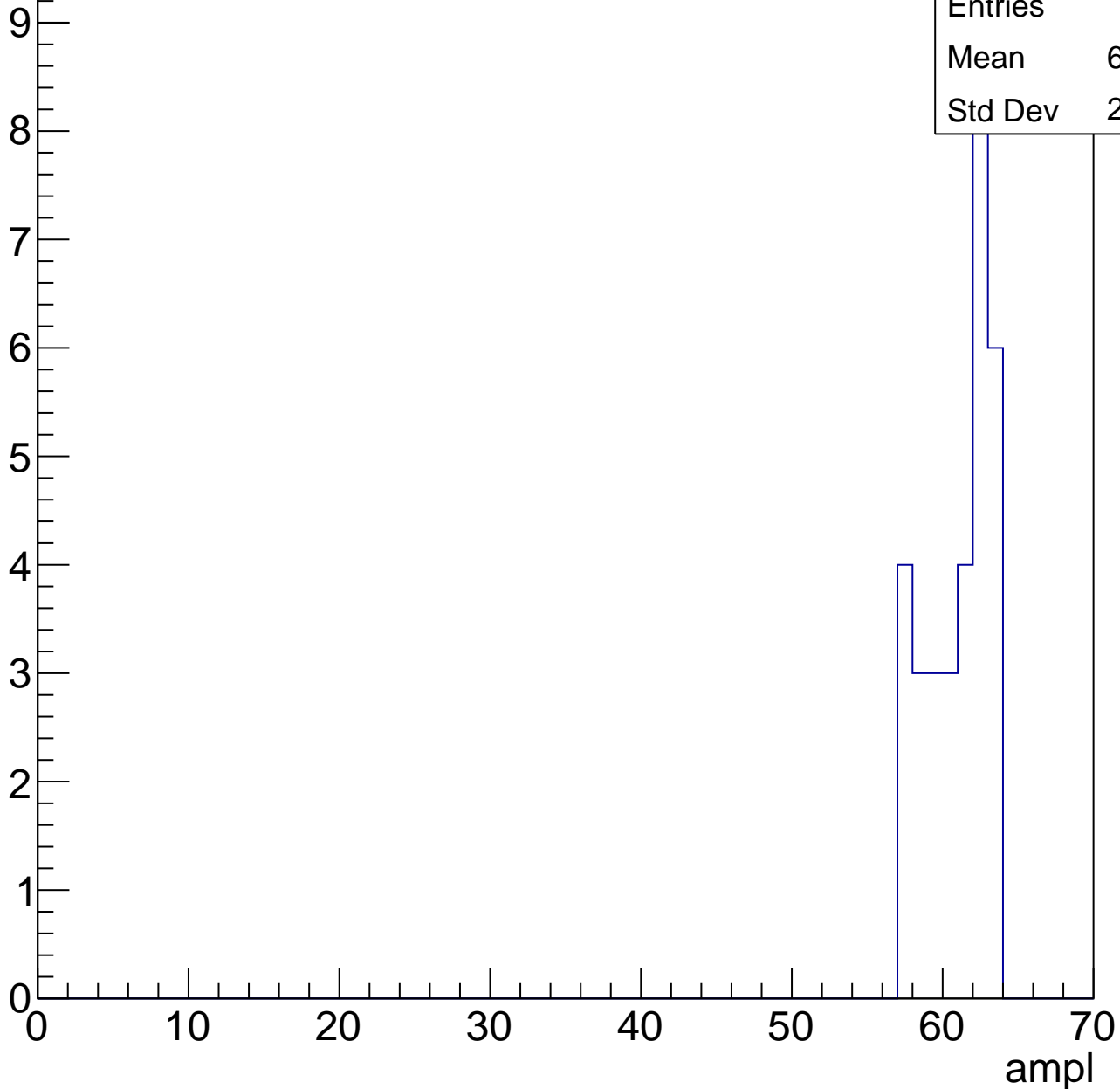


# B0L001S, U2-ch121, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

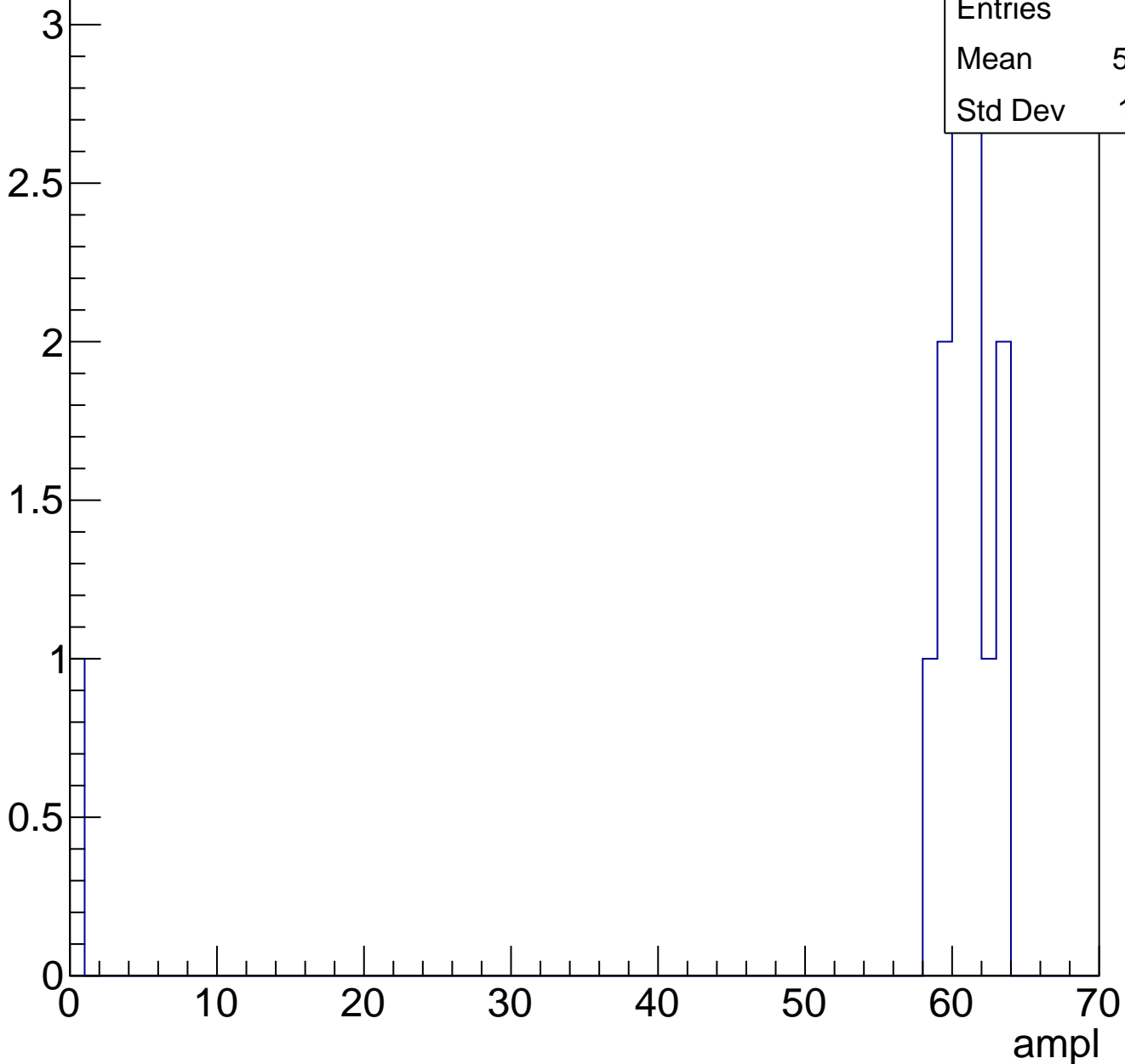
|         |       |
|---------|-------|
| Entries | 32    |
| Mean    | 60.59 |
| Std Dev | 2.044 |



# B0L001S, U2-ch121, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch121, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 0 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch122, adc0

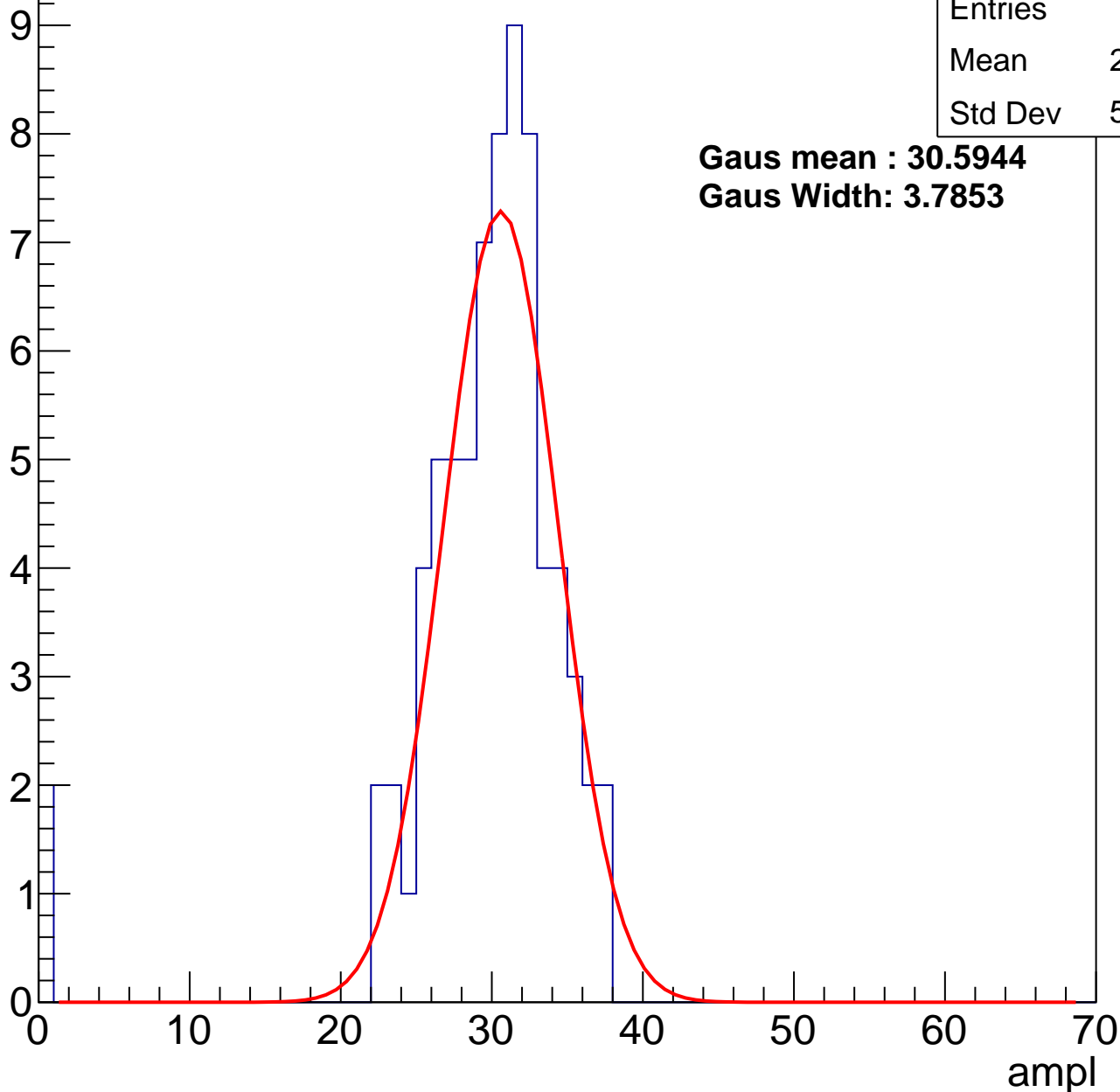
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 73    |
| Mean    | 28.99 |
| Std Dev | 5.997 |

**Gaus mean : 30.5944**

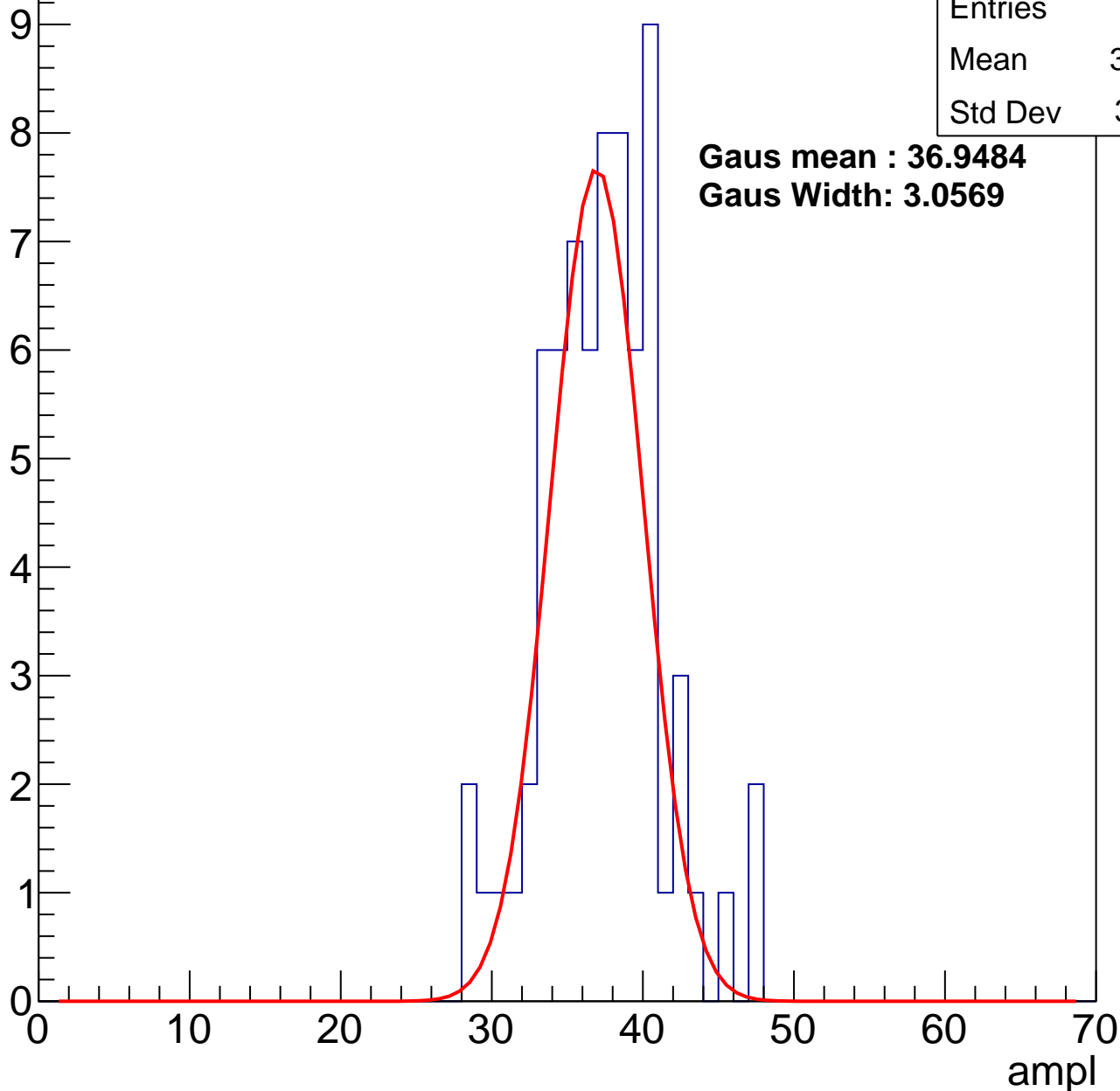
**Gaus Width: 3.7853**



# B0L001S, U2-ch122, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U2-ch122, adc2

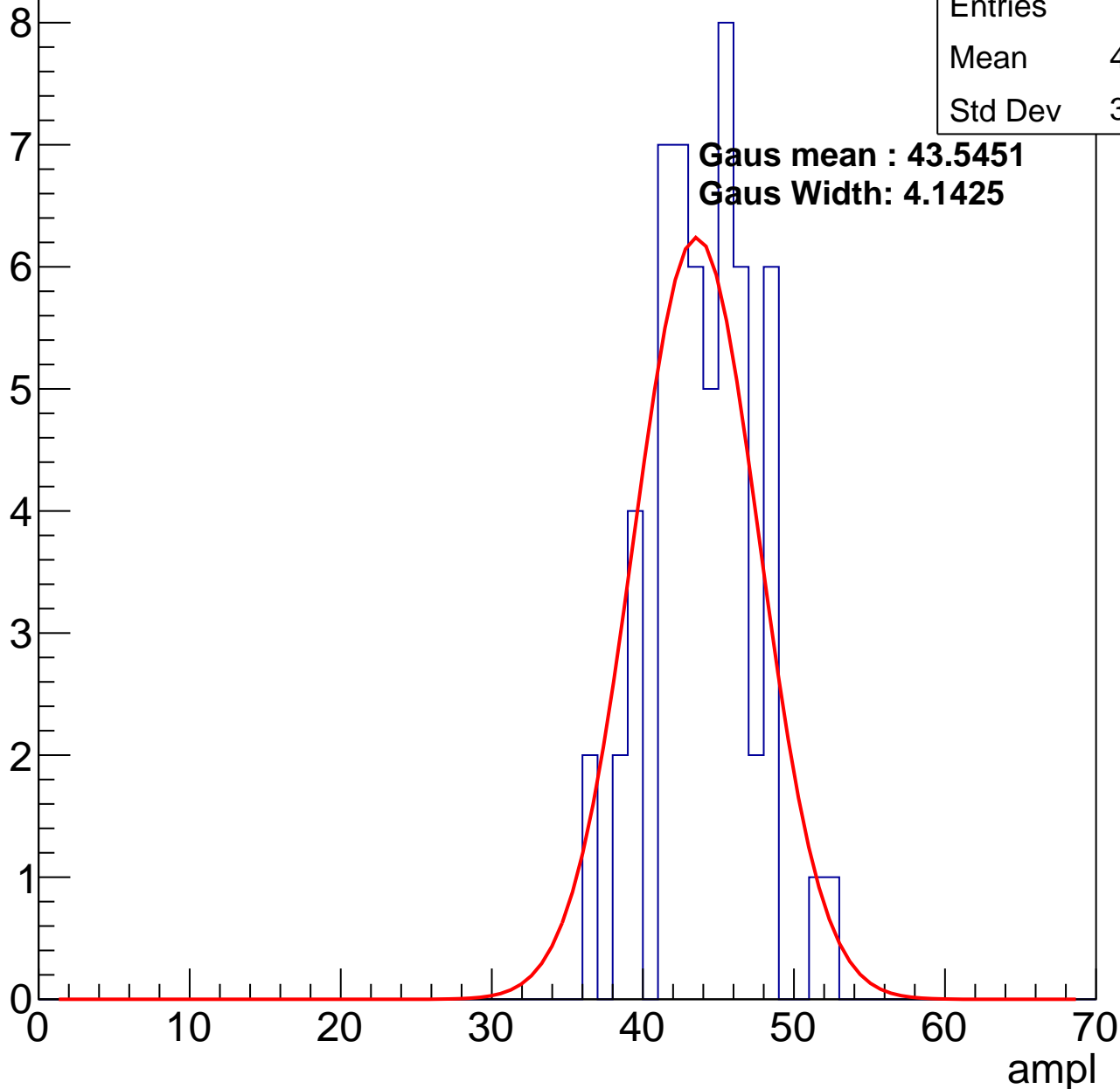
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 57    |
| Mean    | 43.58 |
| Std Dev | 3.366 |

**Gaus mean : 43.5451**

**Gaus Width: 4.1425**

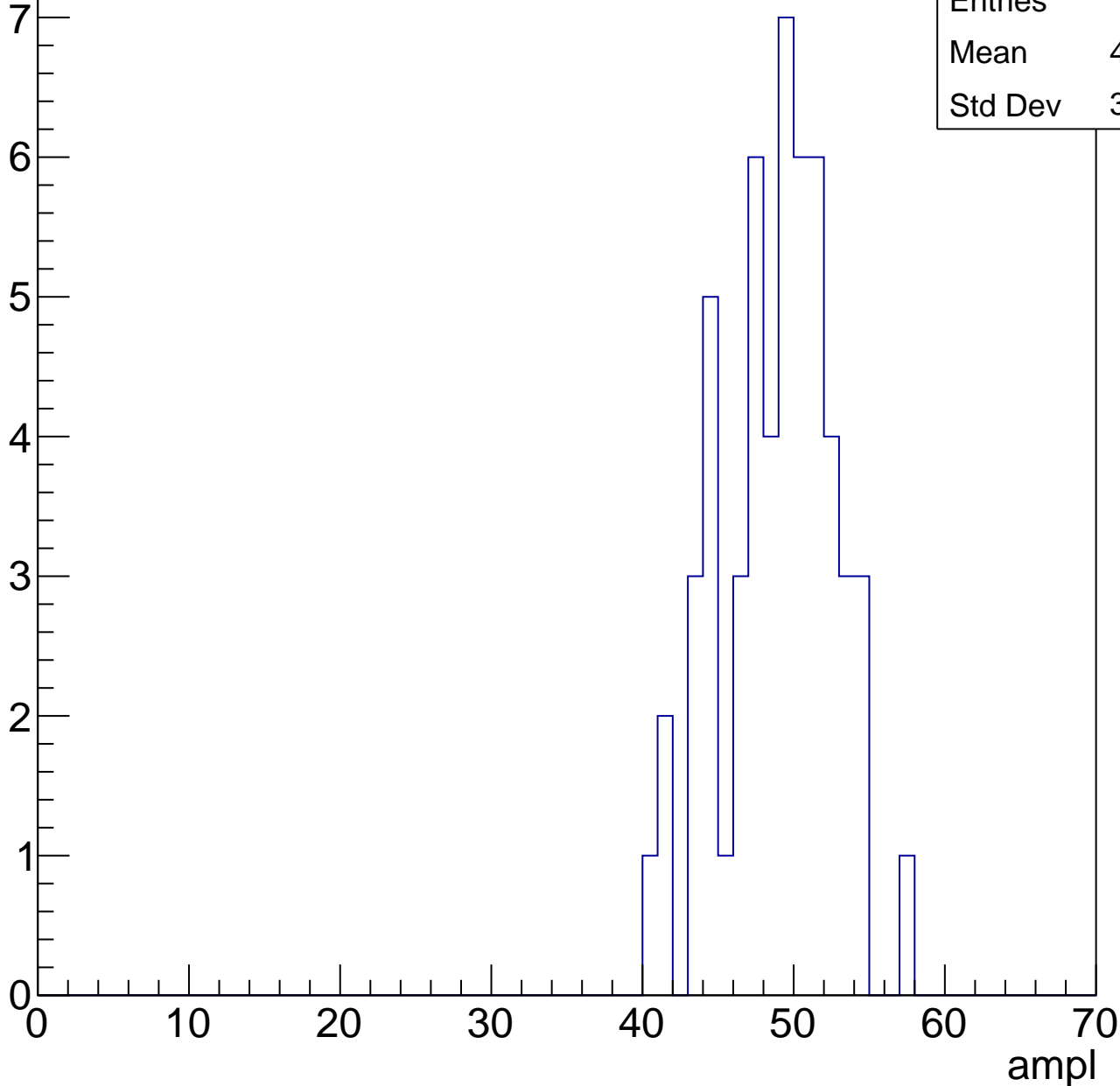


# B0L001S, U2-ch122, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 55    |
| Mean    | 48.42 |
| Std Dev | 3.686 |

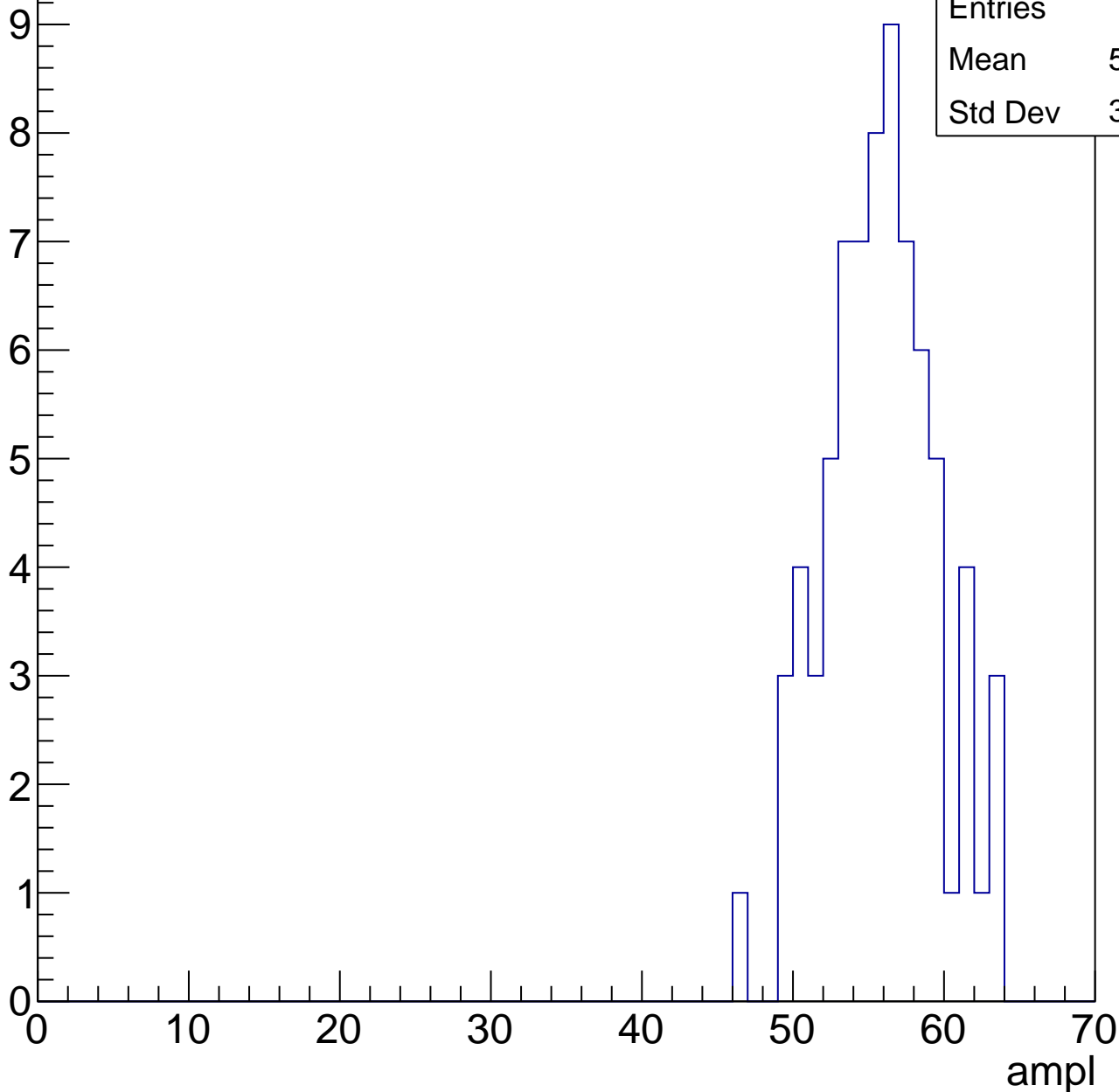


# B0L001S, U2-ch122, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 74    |
| Mean    | 55.35 |
| Std Dev | 3.656 |



# B0L001S, U2-ch122, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

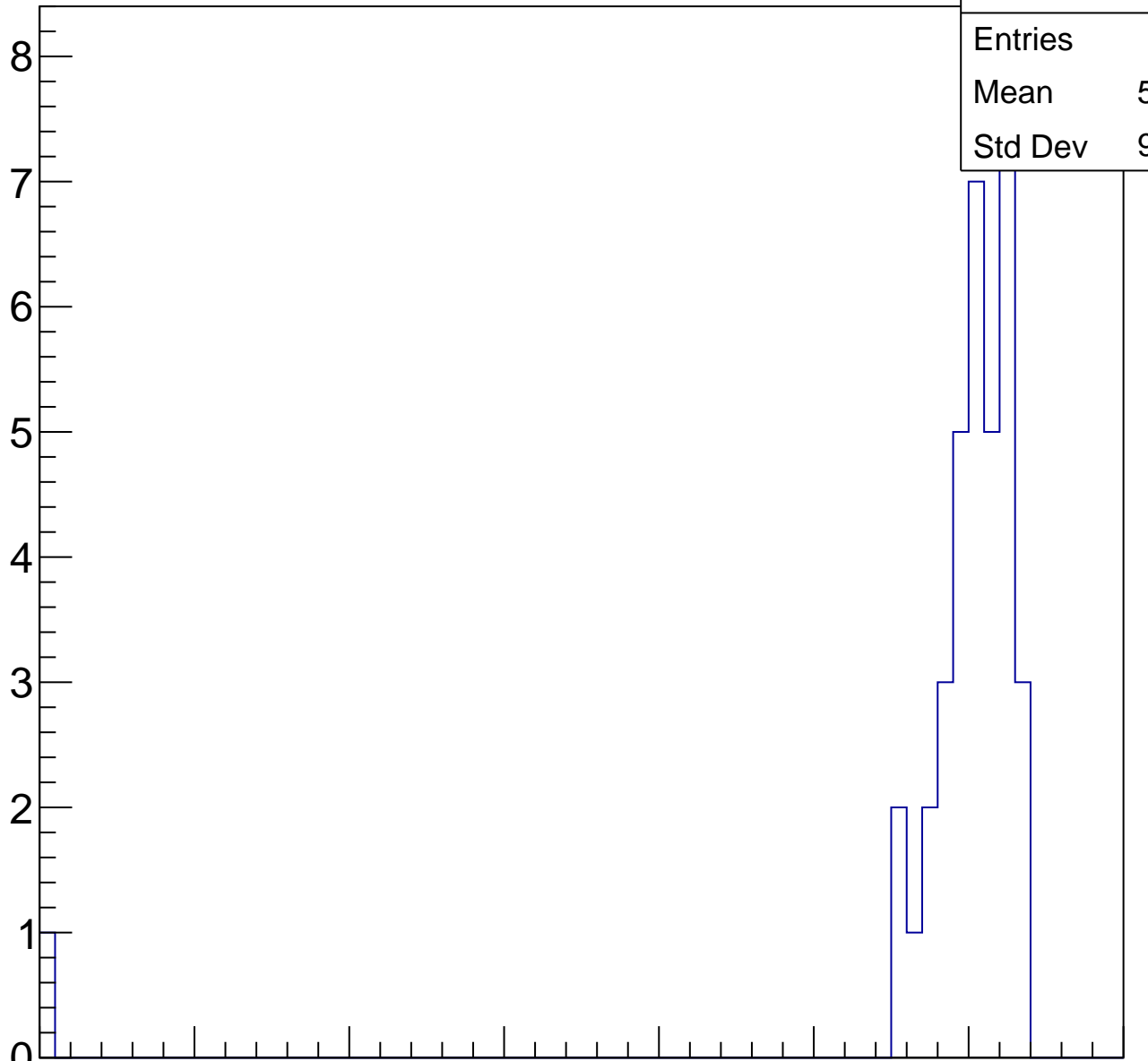
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

|         |       |
|---------|-------|
| Entries | 37    |
| Mean    | 58.35 |
| Std Dev | 9.952 |

ampl

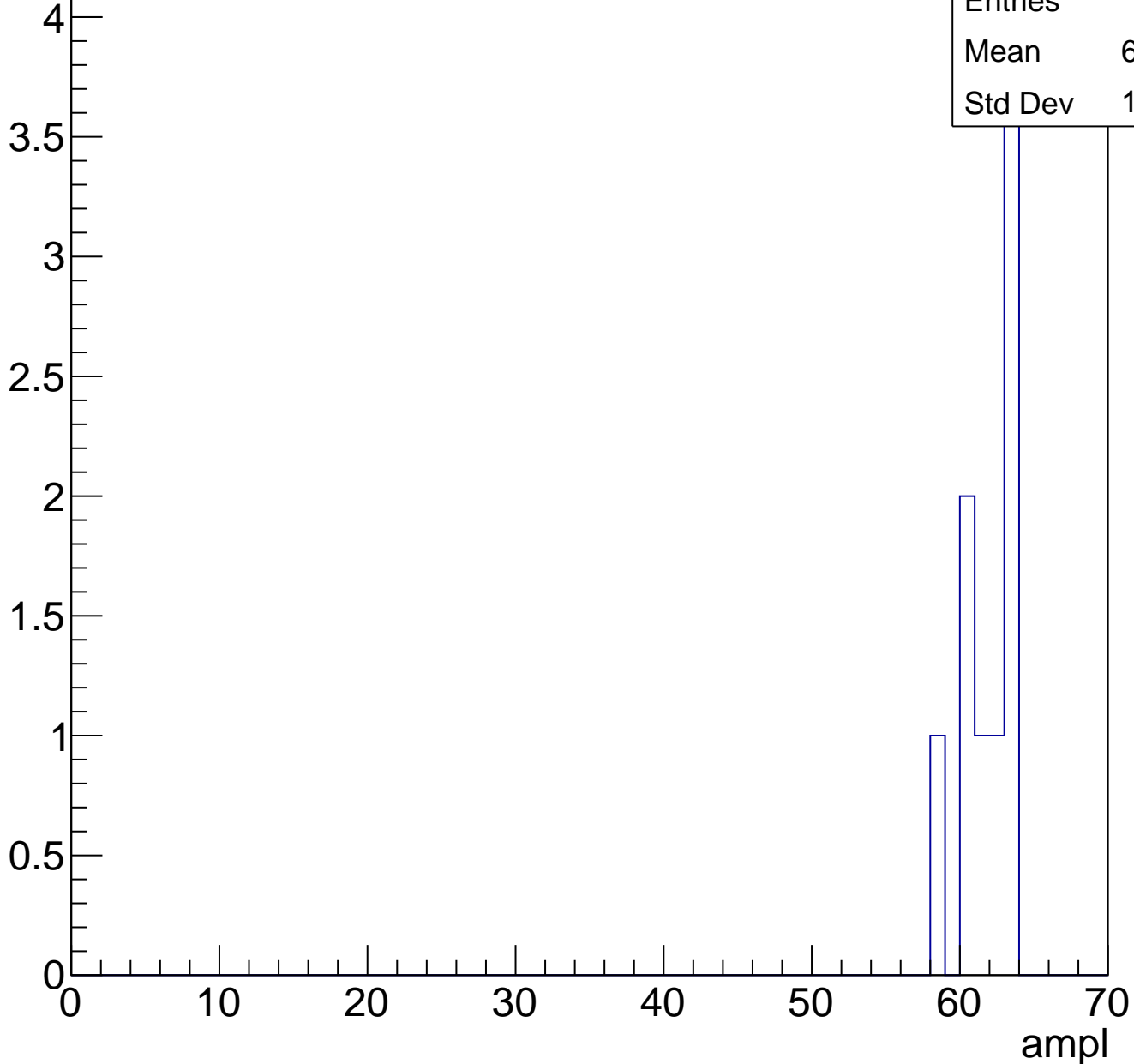
0 10 20 30 40 50 60 70



# B0L001S, U2-ch122, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch122, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 1 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch123, adc0

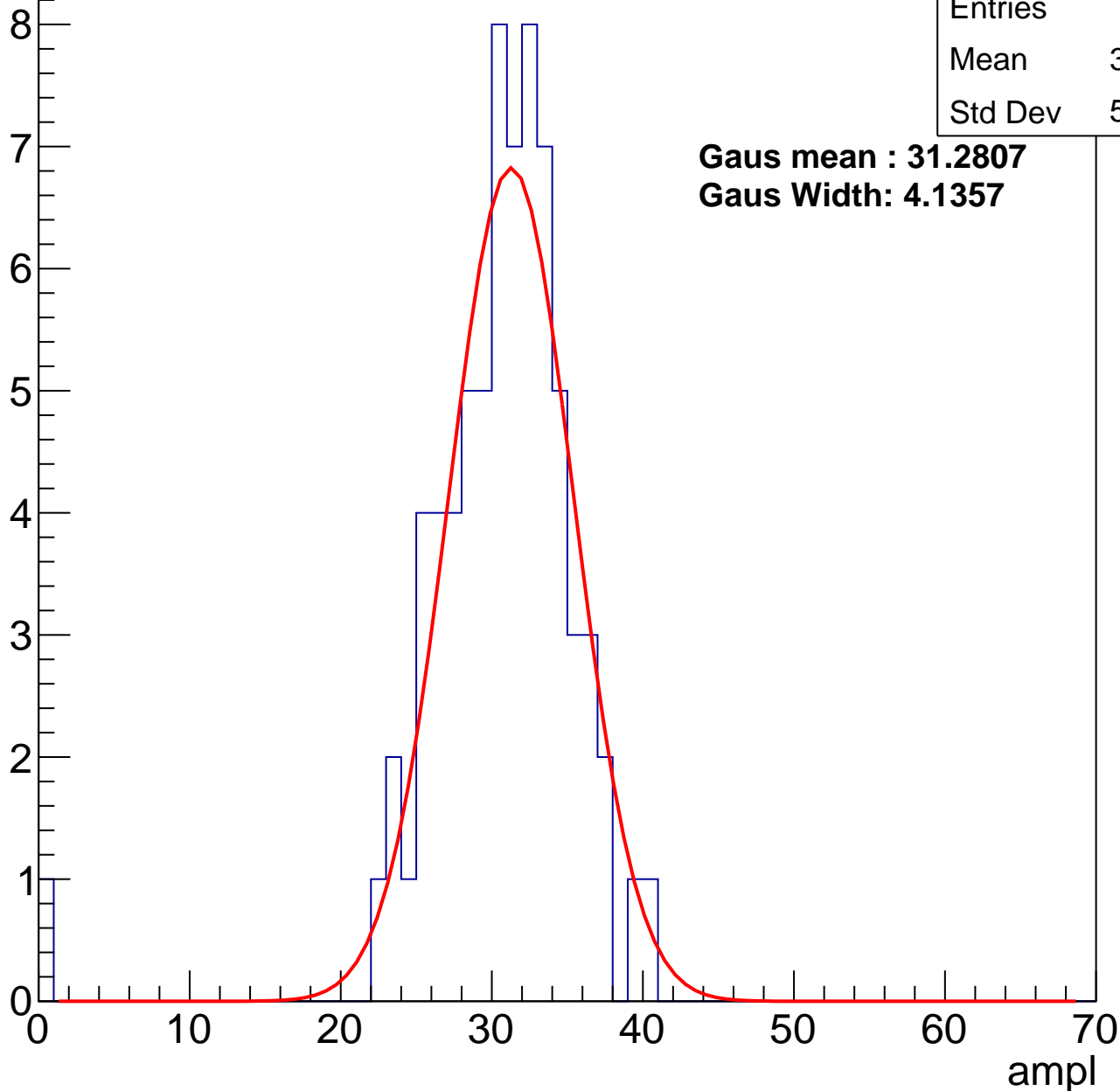
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 72    |
| Mean    | 30.12 |
| Std Dev | 5.225 |

**Gaus mean : 31.2807**

**Gaus Width: 4.1357**



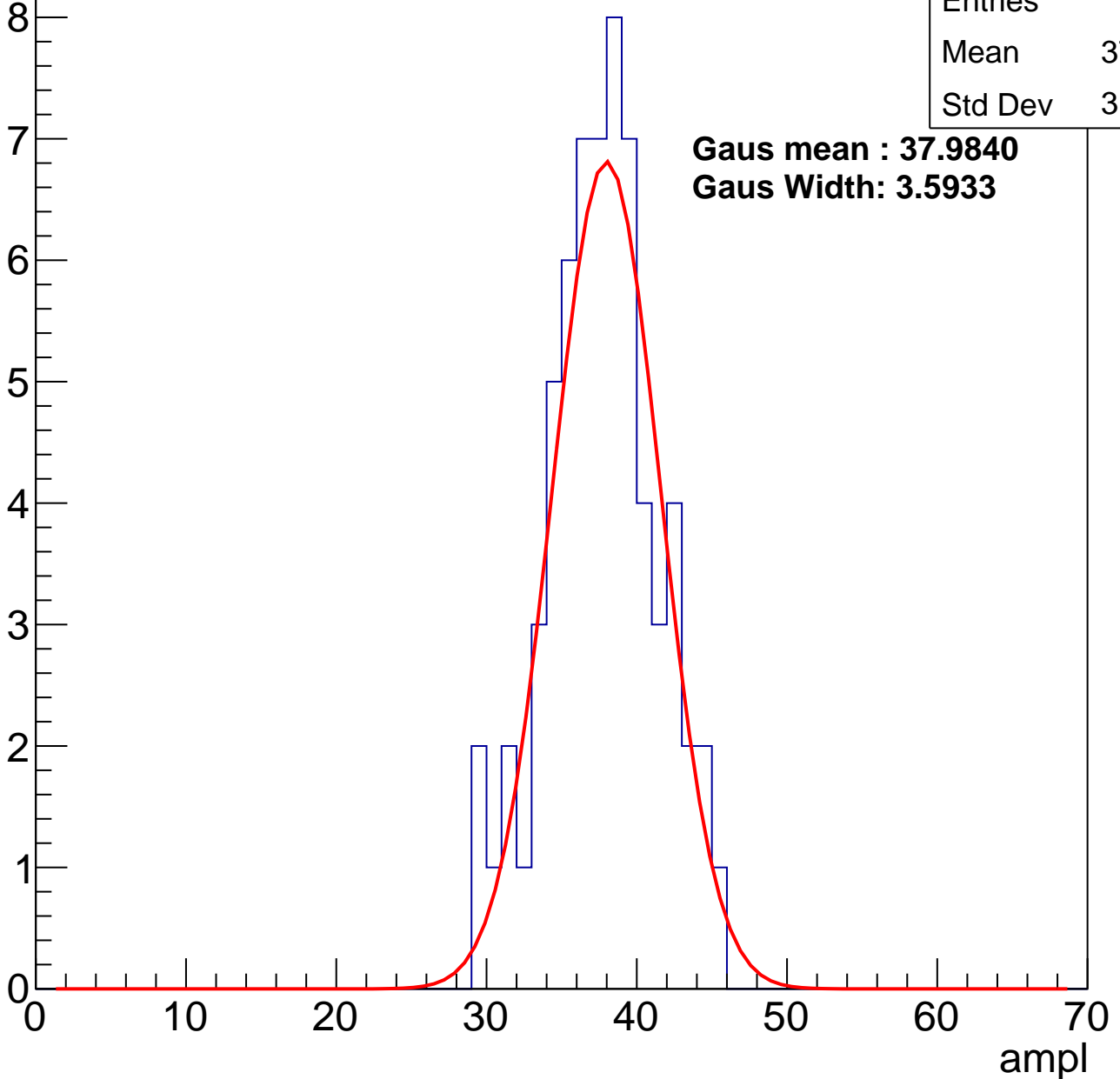
# B0L001S, U2-ch123, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 65    |
| Mean    | 37.22 |
| Std Dev | 3.614 |

**Gaus mean : 37.9840**  
**Gaus Width: 3.5933**



# B0L001S, U2-ch123, adc2

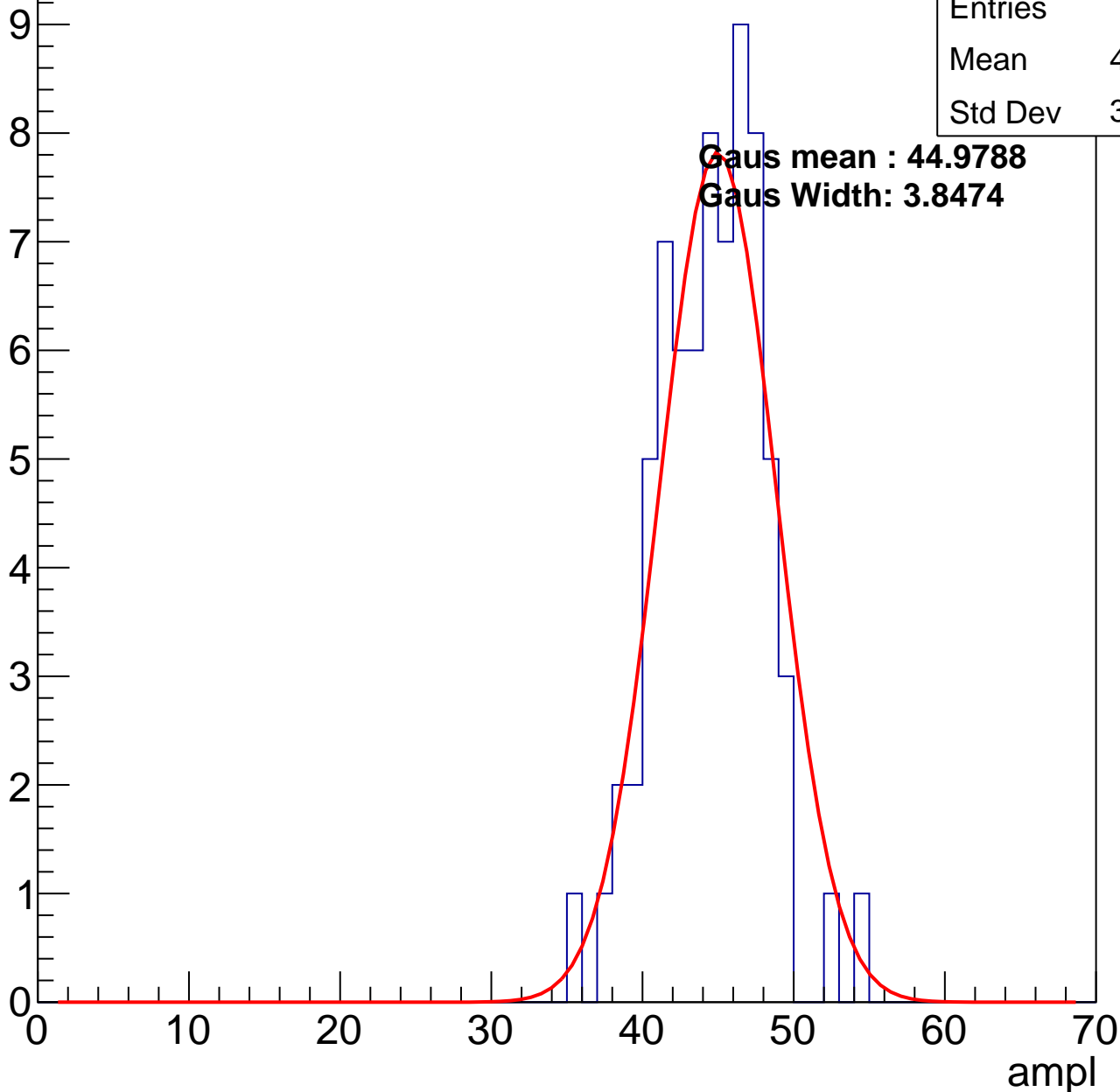
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 72    |
| Mean    | 44.07 |
| Std Dev | 3.453 |

**Gaus mean : 44.9788**

**Gaus Width: 3.8474**

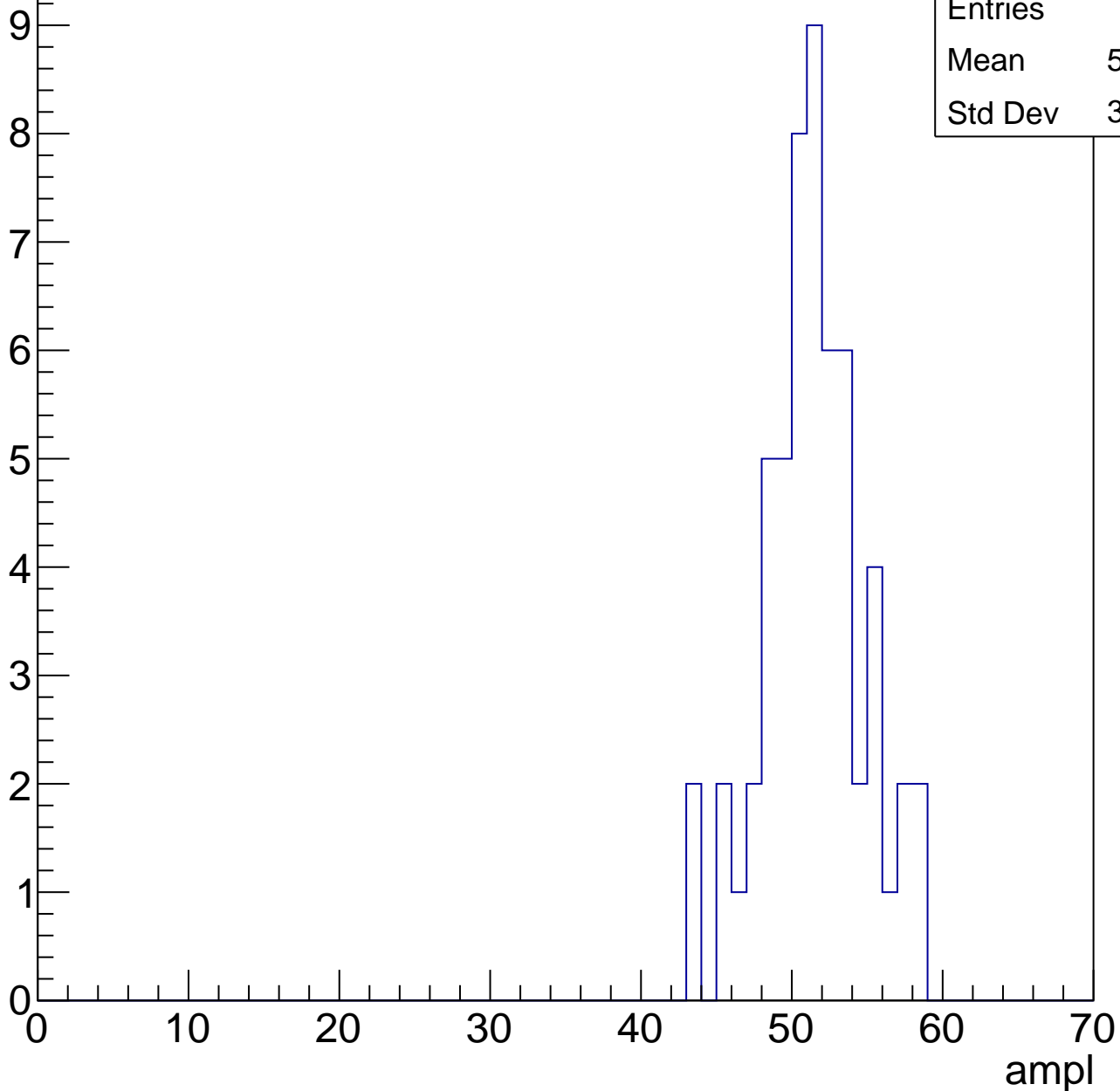


# B0L001S, U2-ch123, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 57    |
| Mean    | 50.95 |
| Std Dev | 3.343 |

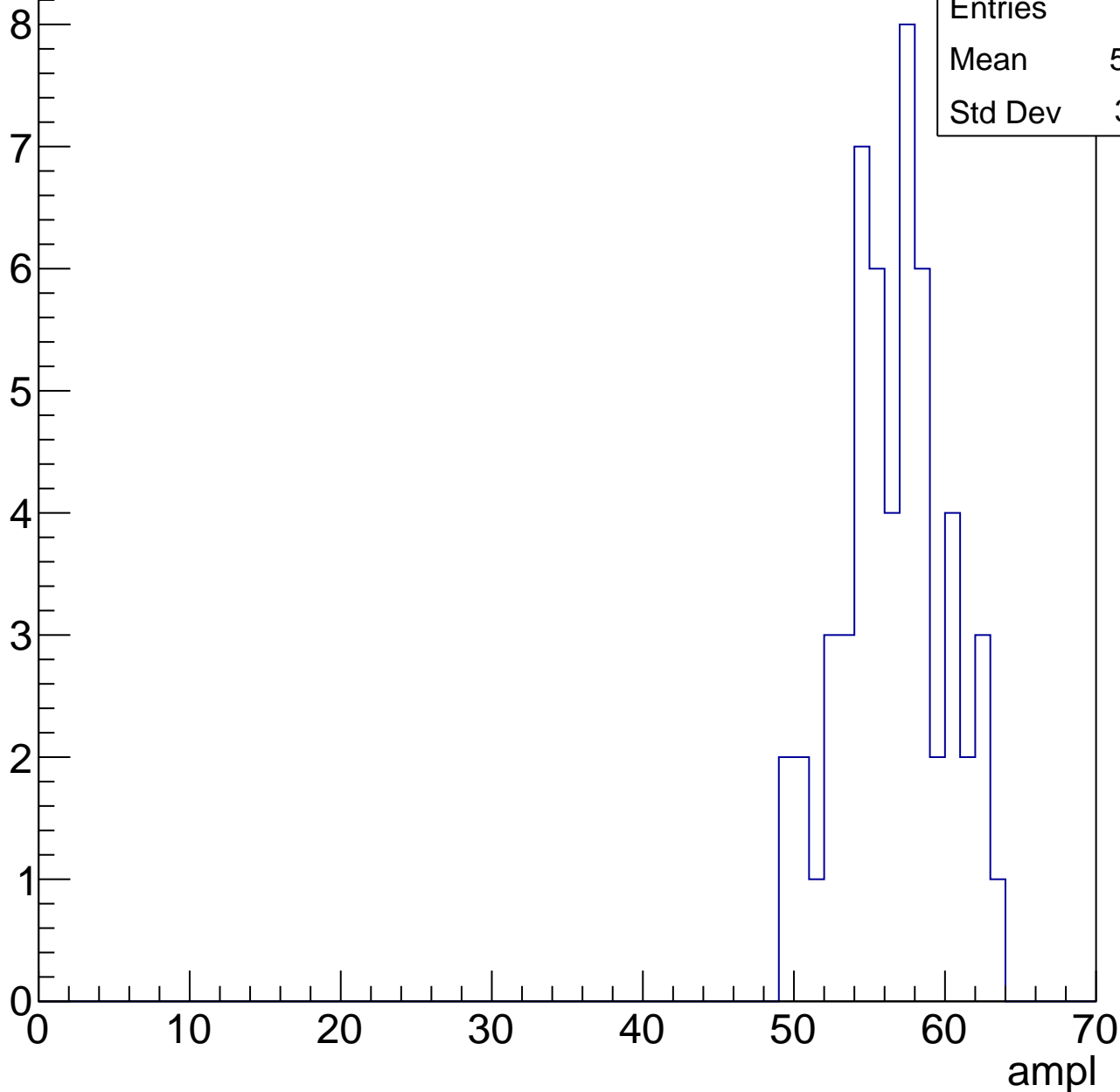


# B0L001S, U2-ch123, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

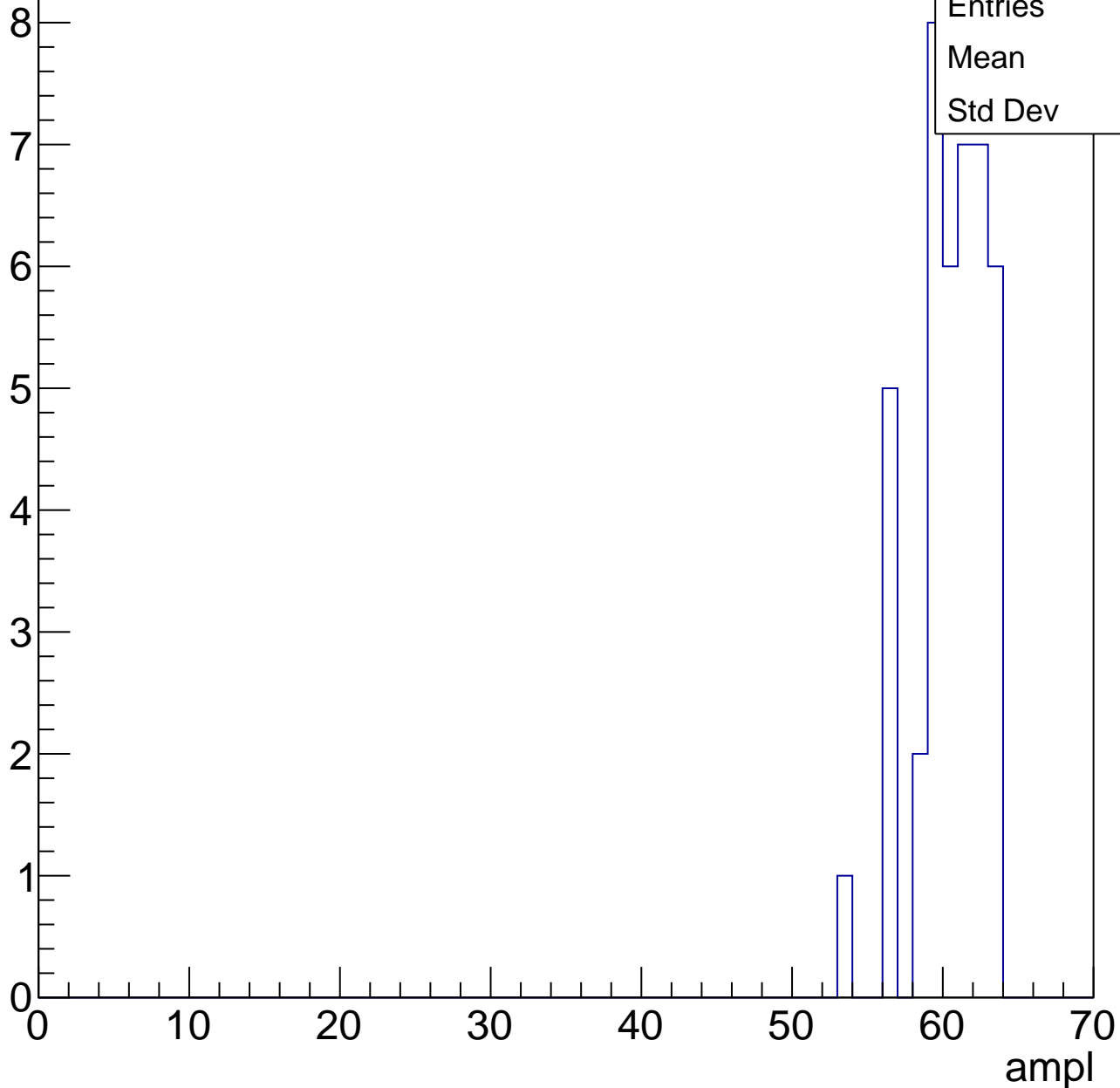
|         |       |
|---------|-------|
| Entries | 54    |
| Mean    | 56.09 |
| Std Dev | 3.401 |



# B0L001S, U2-ch123, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

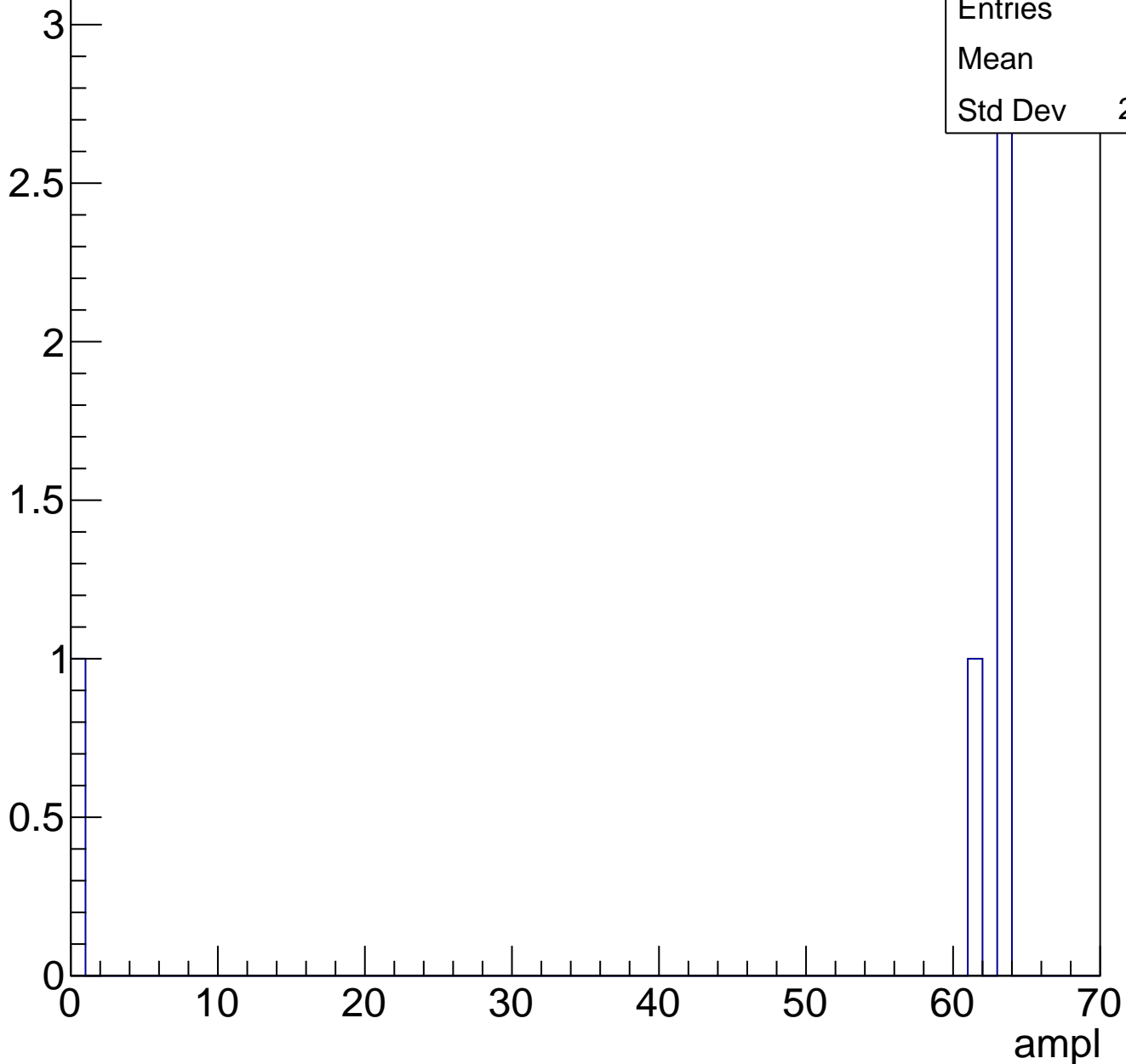
Entry



# B0L001S, U2-ch123, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch123, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U2-ch124, adc0

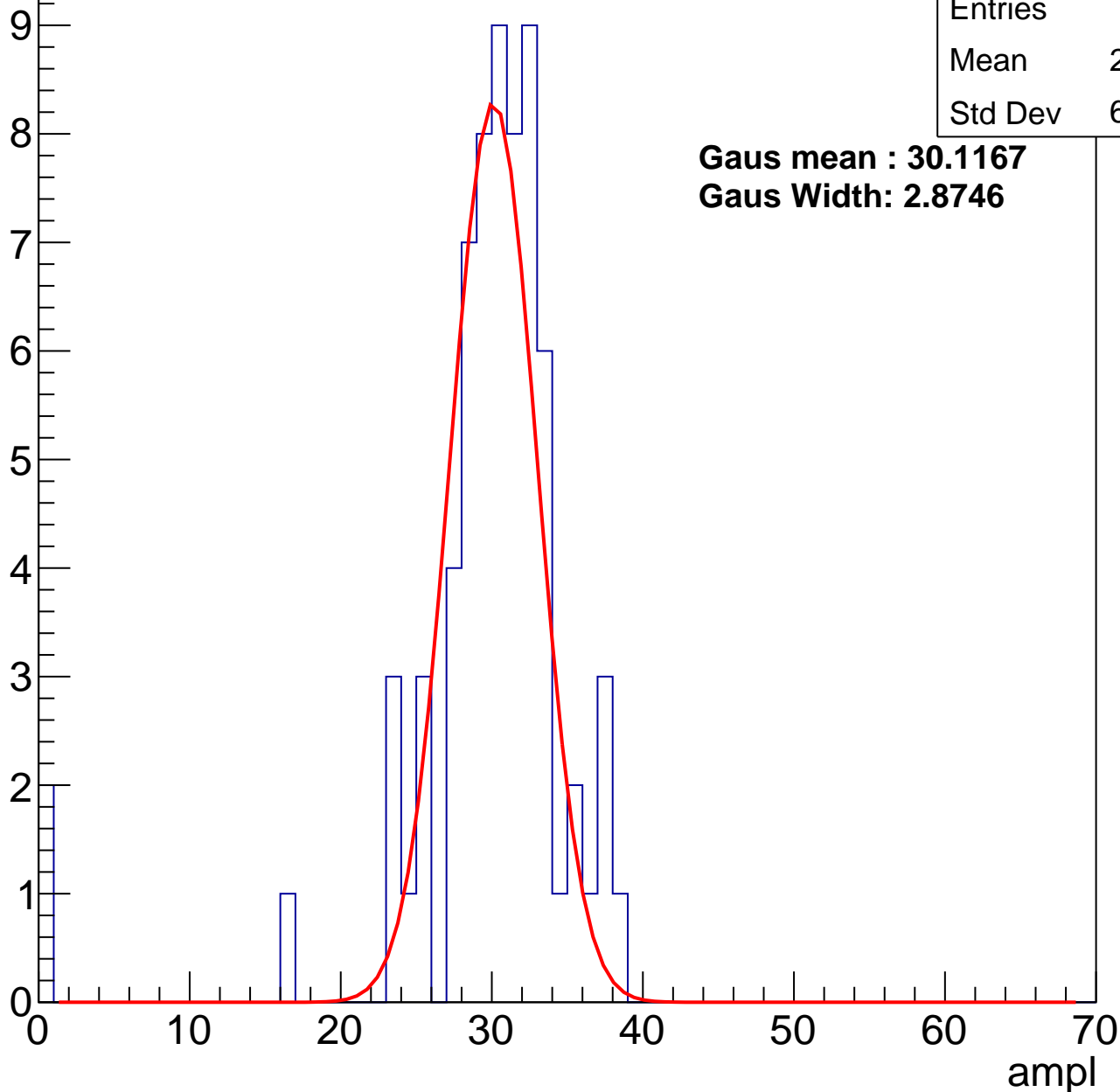
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 69    |
| Mean    | 29.17 |
| Std Dev | 6.244 |

**Gaus mean : 30.1167**

**Gaus Width: 2.8746**



# B0L001S, U2-ch124, adc1

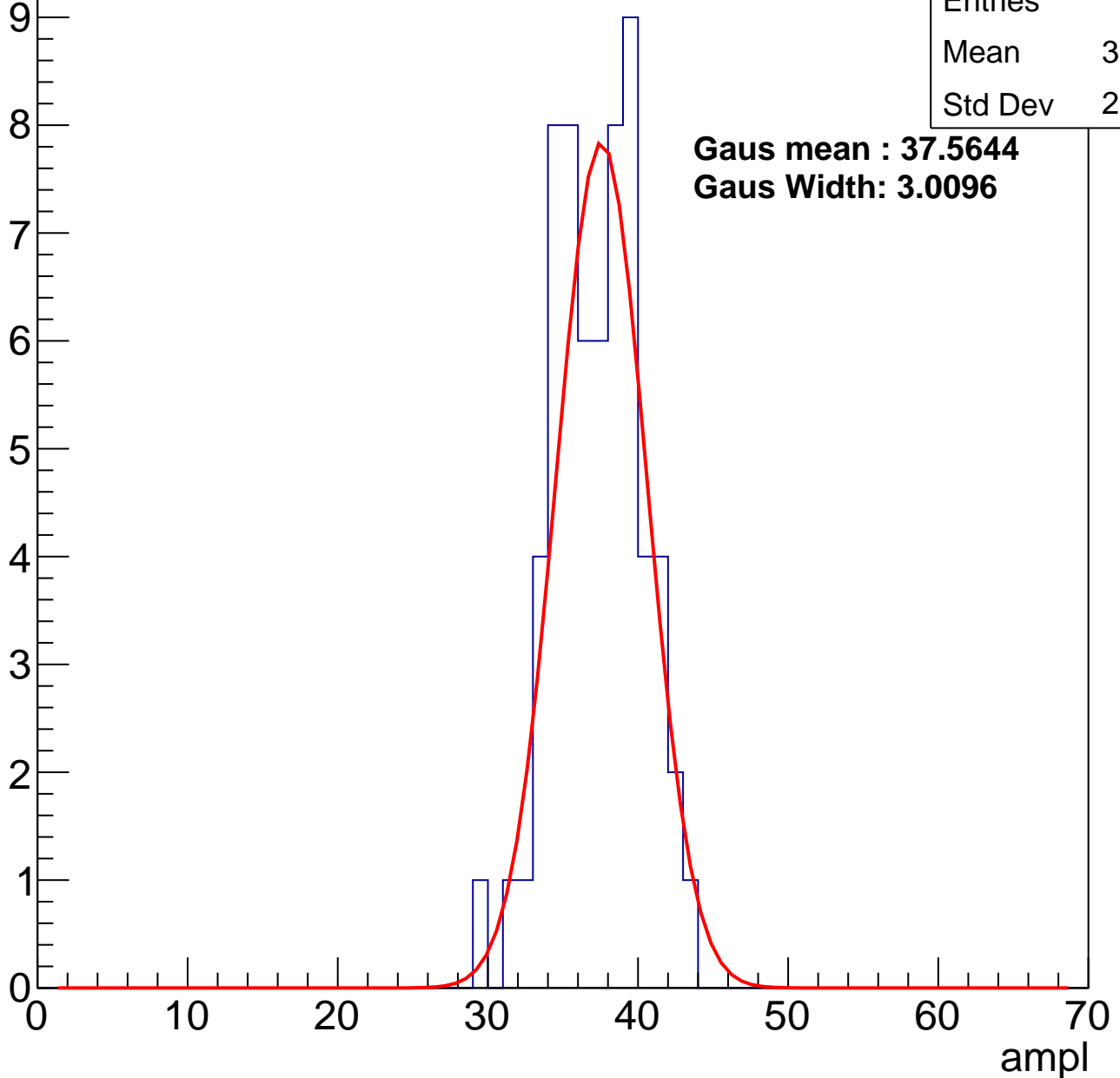
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 63    |
| Mean    | 36.83 |
| Std Dev | 2.892 |

**Gaus mean : 37.5644**

**Gaus Width: 3.0096**



# B0L001S, U2-ch124, adc2

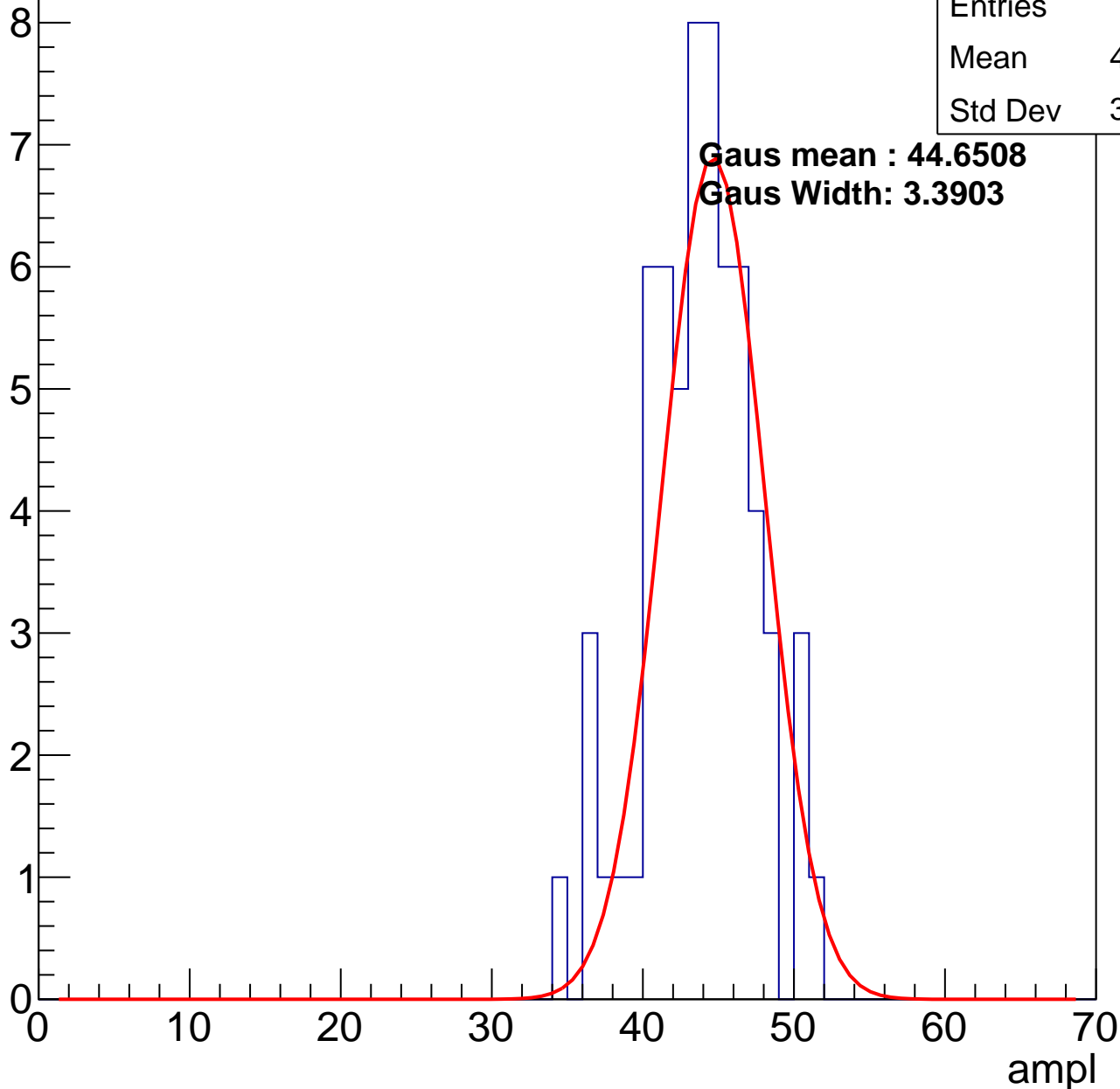
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 63    |
| Mean    | 43.29 |
| Std Dev | 3.605 |

**Gaus mean : 44.6508**

**Gaus Width: 3.3903**



# B0L001S, U2-ch124, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

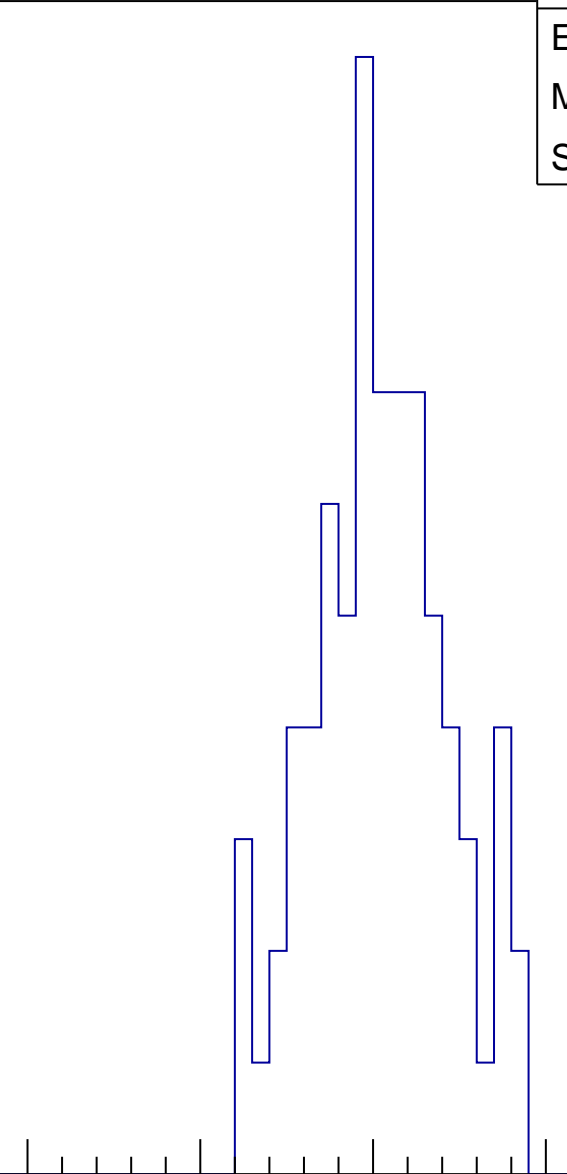
|         |       |
|---------|-------|
| Entries | 75    |
| Mean    | 50    |
| Std Dev | 3.899 |

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

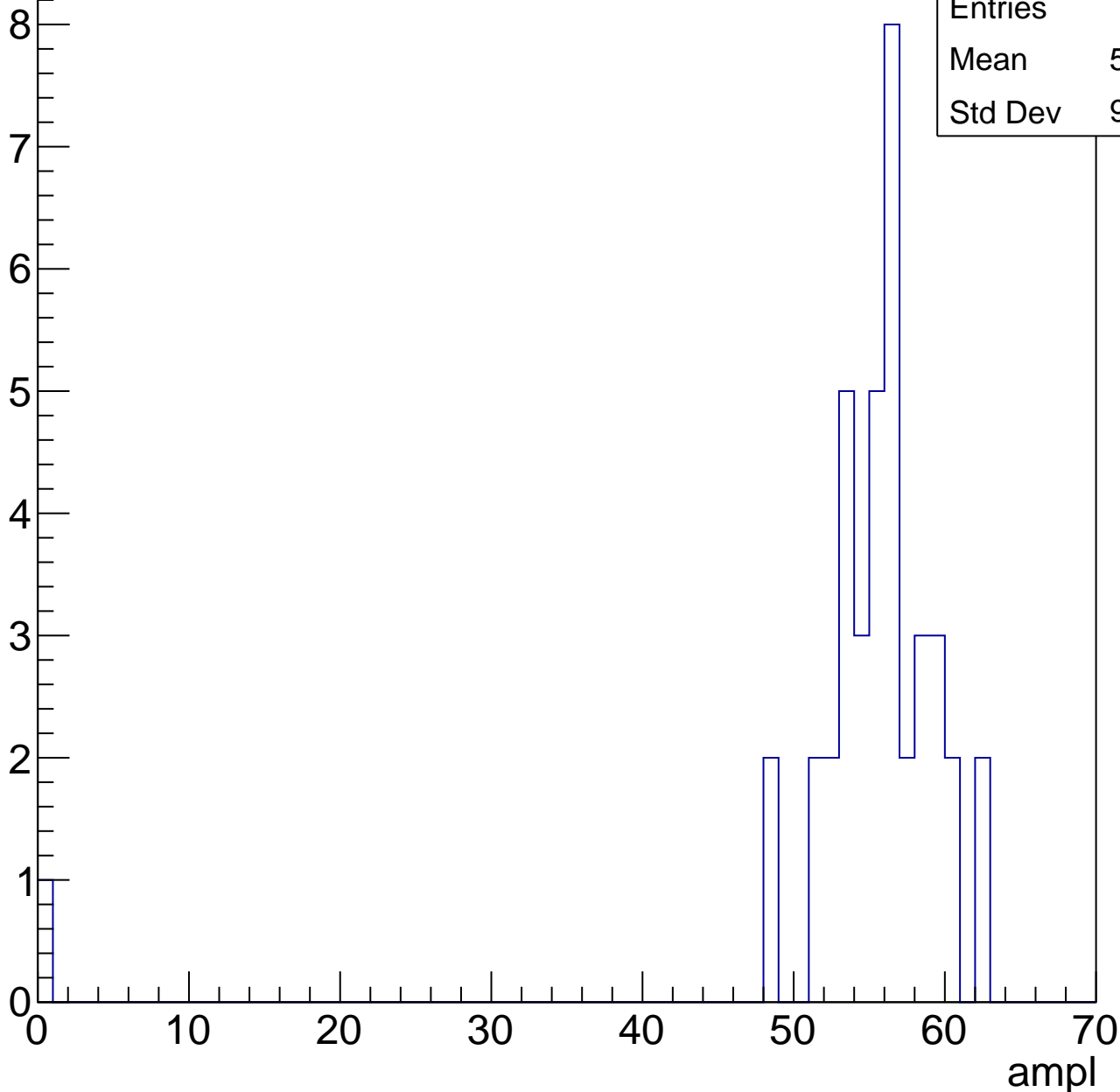


# B0L001S, U2-ch124, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 40    |
| Mean    | 54.02 |
| Std Dev | 9.215 |

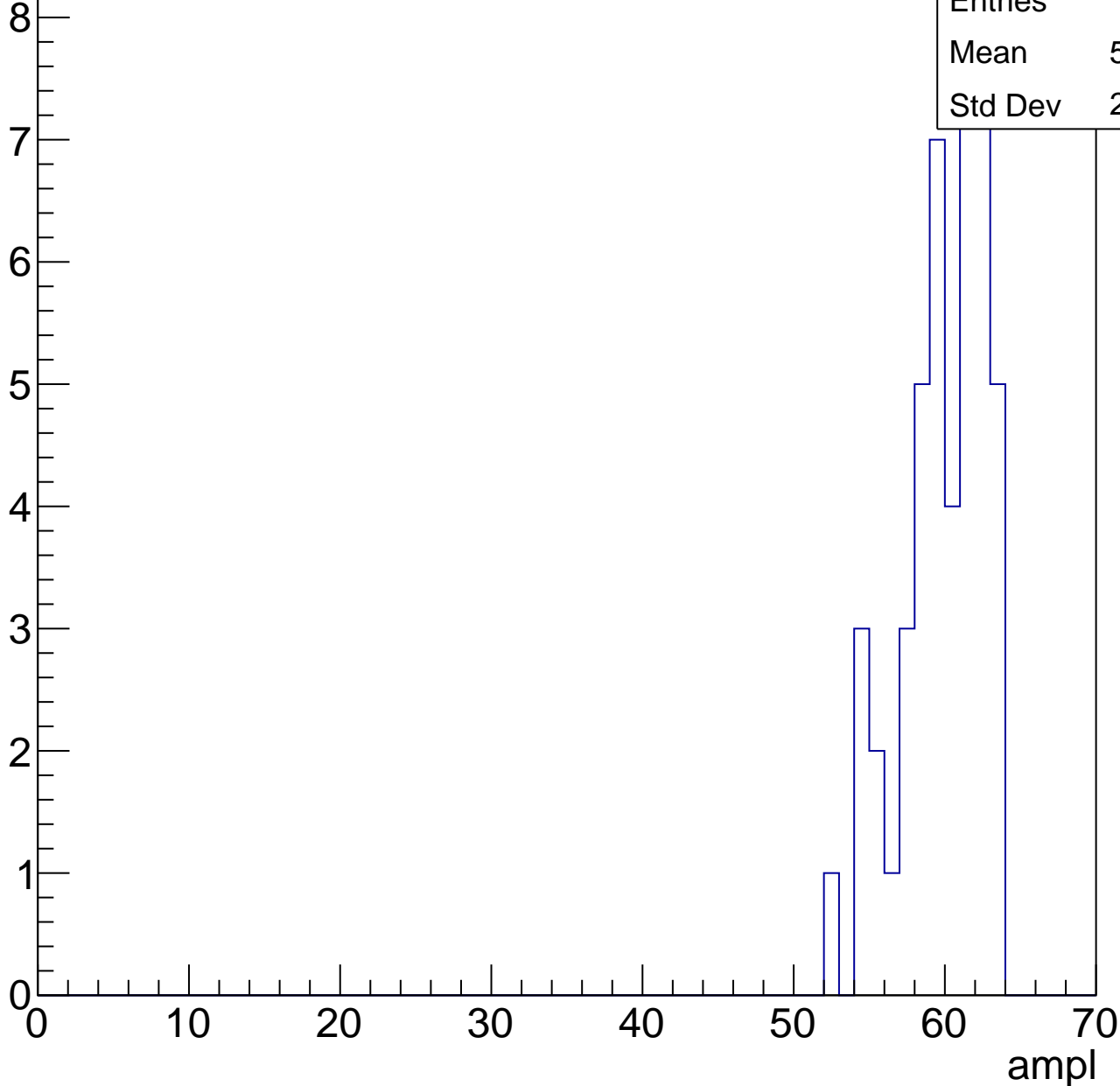


# B0L001S, U2-ch124, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 47    |
| Mean    | 59.43 |
| Std Dev | 2.773 |

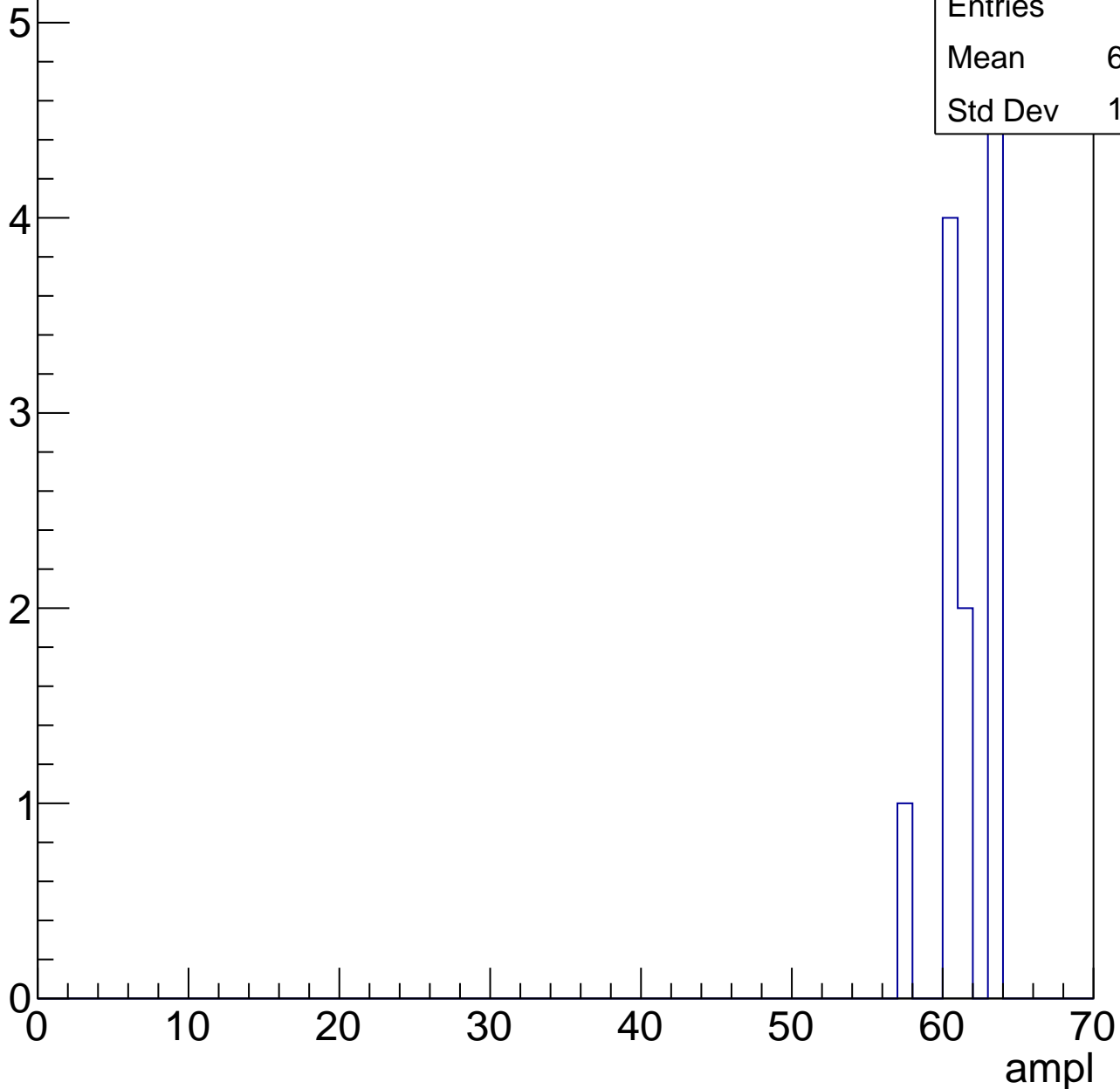


# B0L001S, U2-ch124, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 12    |
| Mean    | 61.17 |
| Std Dev | 1.818 |





# B0L001S, U2-ch124, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 0 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch125, adc0

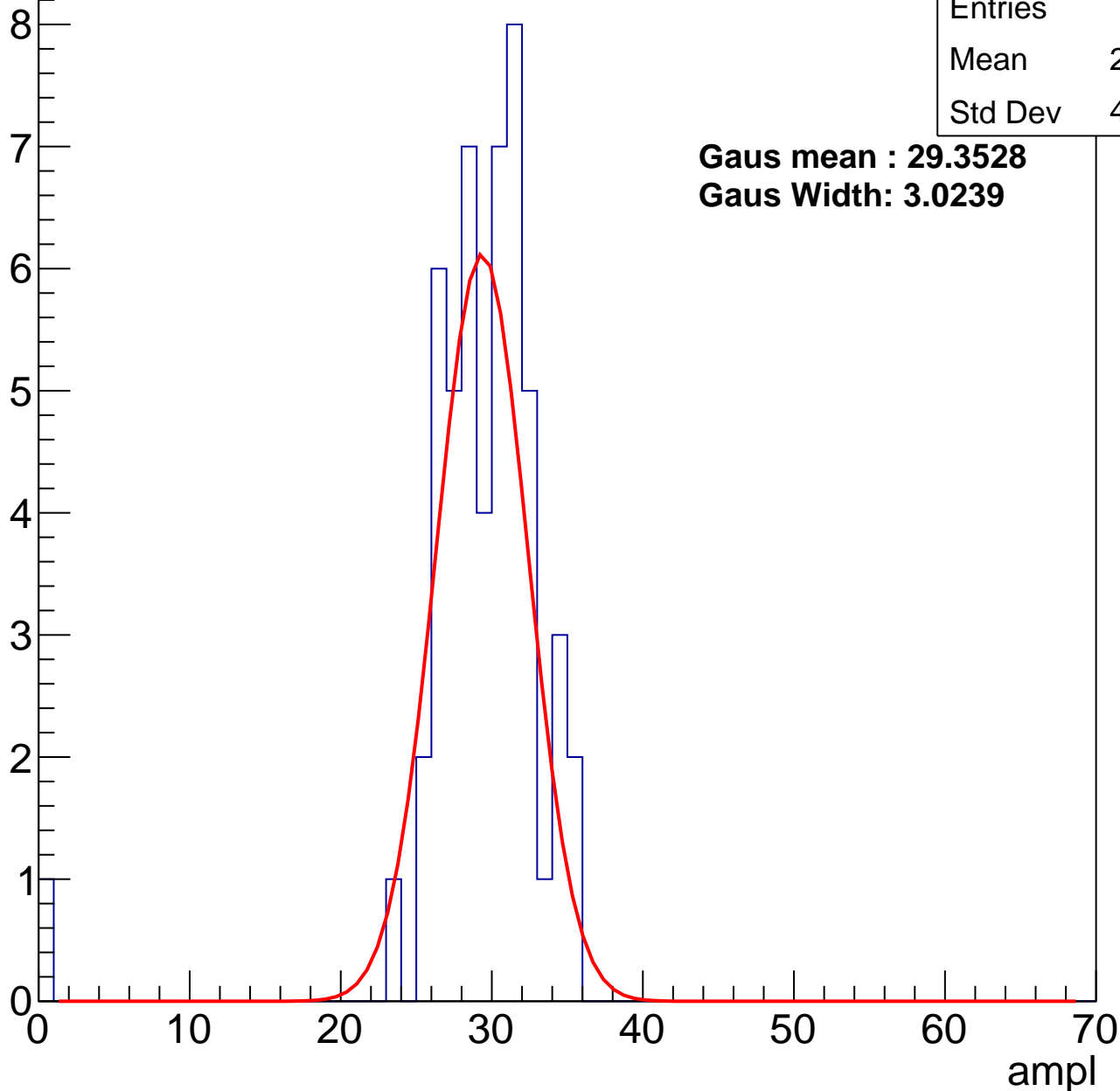
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 52    |
| Mean    | 28.83 |
| Std Dev | 4.874 |

**Gaus mean : 29.3528**

**Gaus Width: 3.0239**

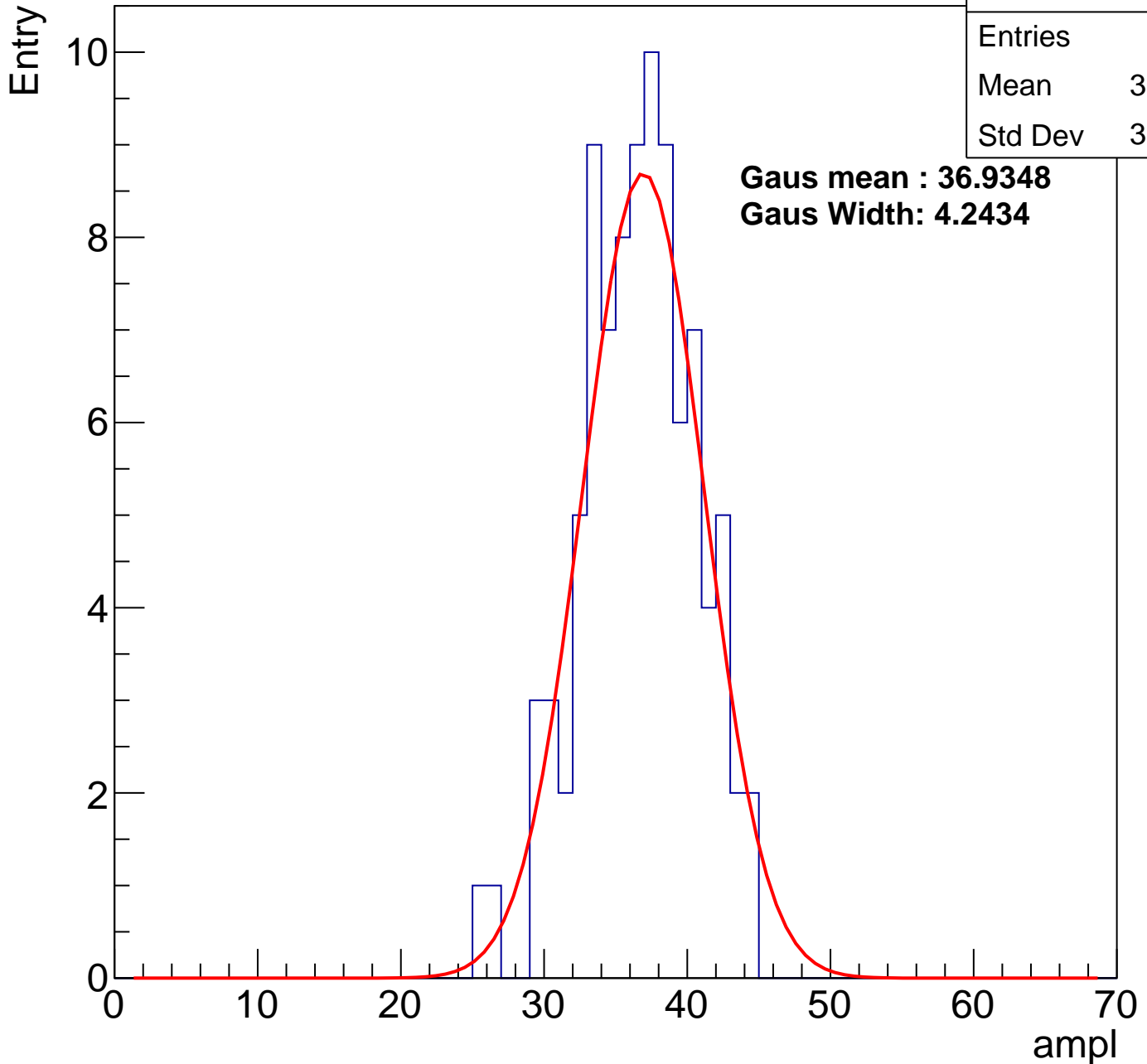


# B0L001S, U2-ch125, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

|         |       |
|---------|-------|
| Entries | 93    |
| Mean    | 36.16 |
| Std Dev | 3.933 |

**Gaus mean : 36.9348**  
**Gaus Width: 4.2434**



# B0L001S, U2-ch125, adc2

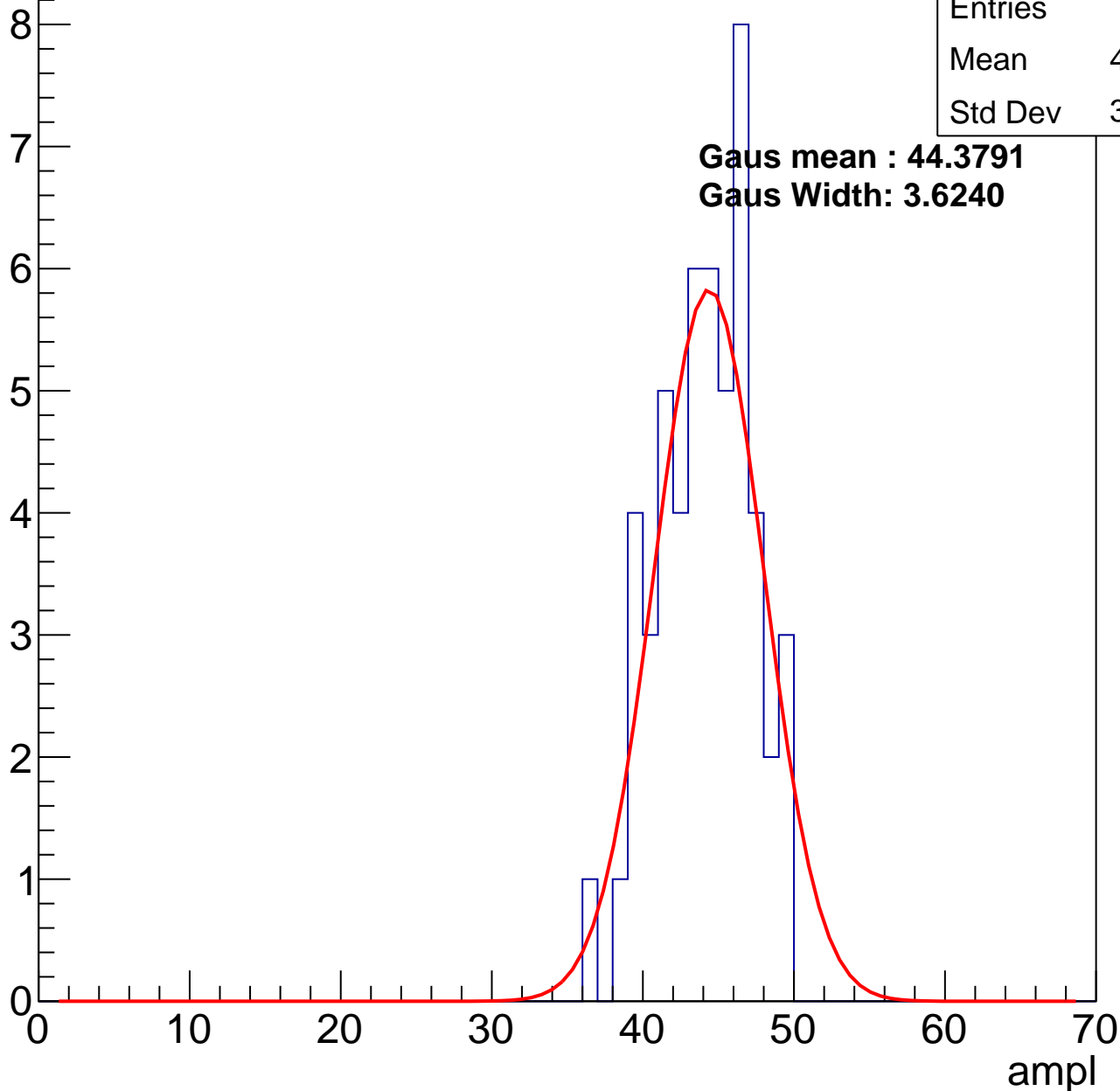
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 52    |
| Mean    | 43.63 |
| Std Dev | 3.064 |

**Gaus mean : 44.3791**

**Gaus Width: 3.6240**

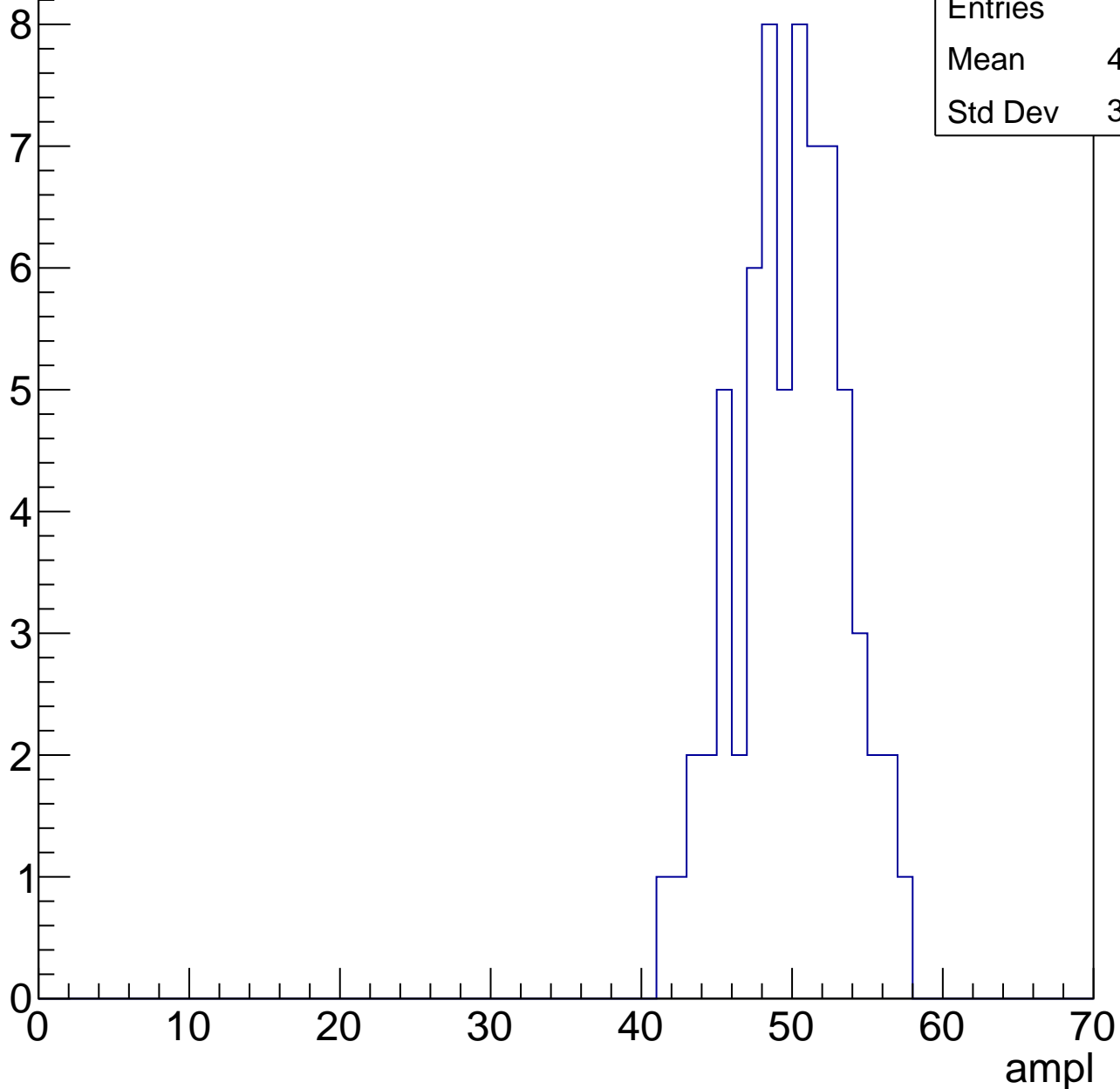


# B0L001S, U2-ch125, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 67    |
| Mean    | 49.43 |
| Std Dev | 3.542 |

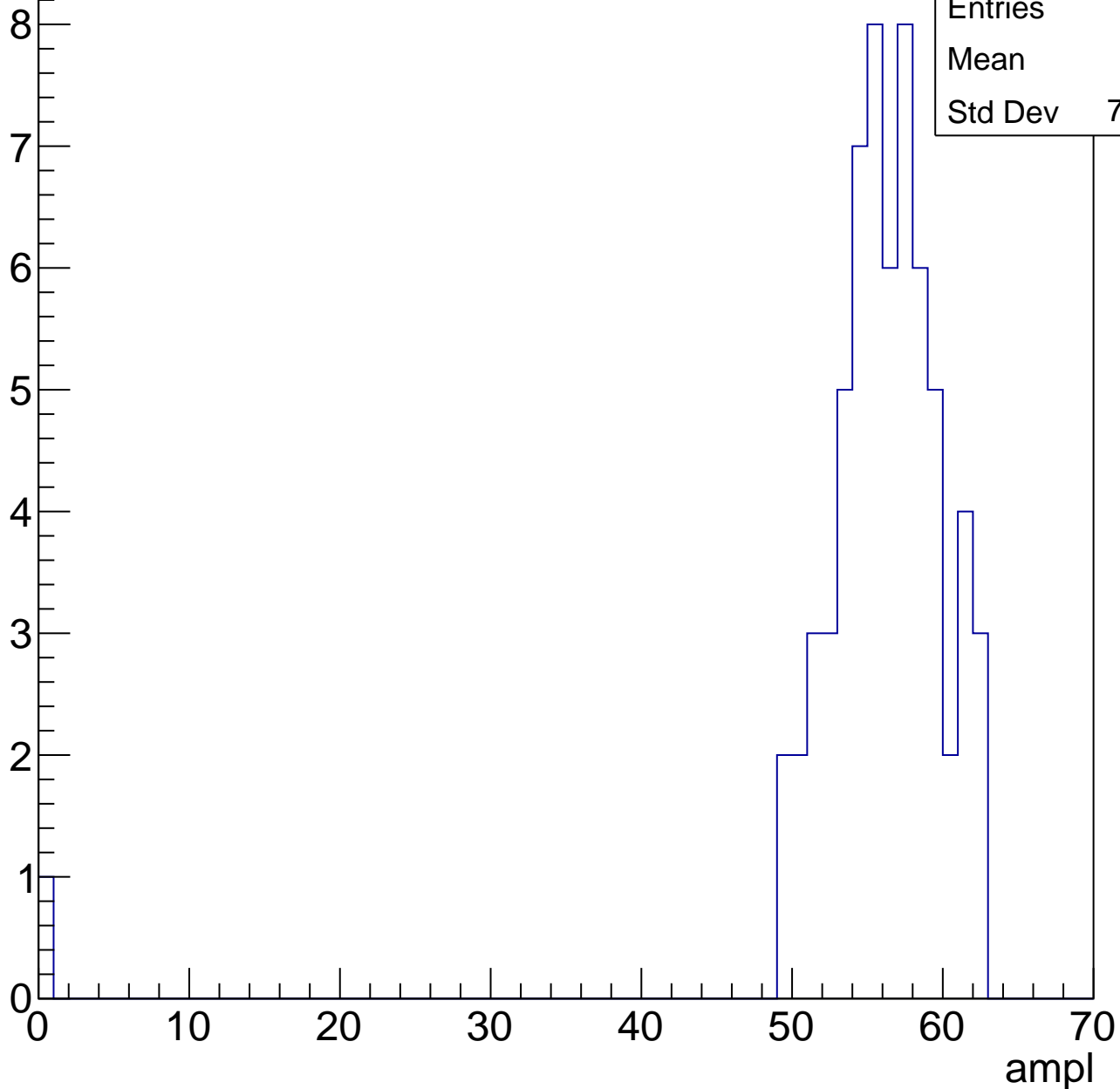


# B0L001S, U2-ch125, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 65    |
| Mean    | 55    |
| Std Dev | 7.608 |



# B0L001S, U2-ch125, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

7

6

5

4

3

2

1

0

|         |       |
|---------|-------|
| Entries | 36    |
| Mean    | 60.28 |
| Std Dev | 1.967 |

ampl

10

20

30

40

50

60

70

# B0L001S, U2-ch125, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch125, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U2-ch126, adc0

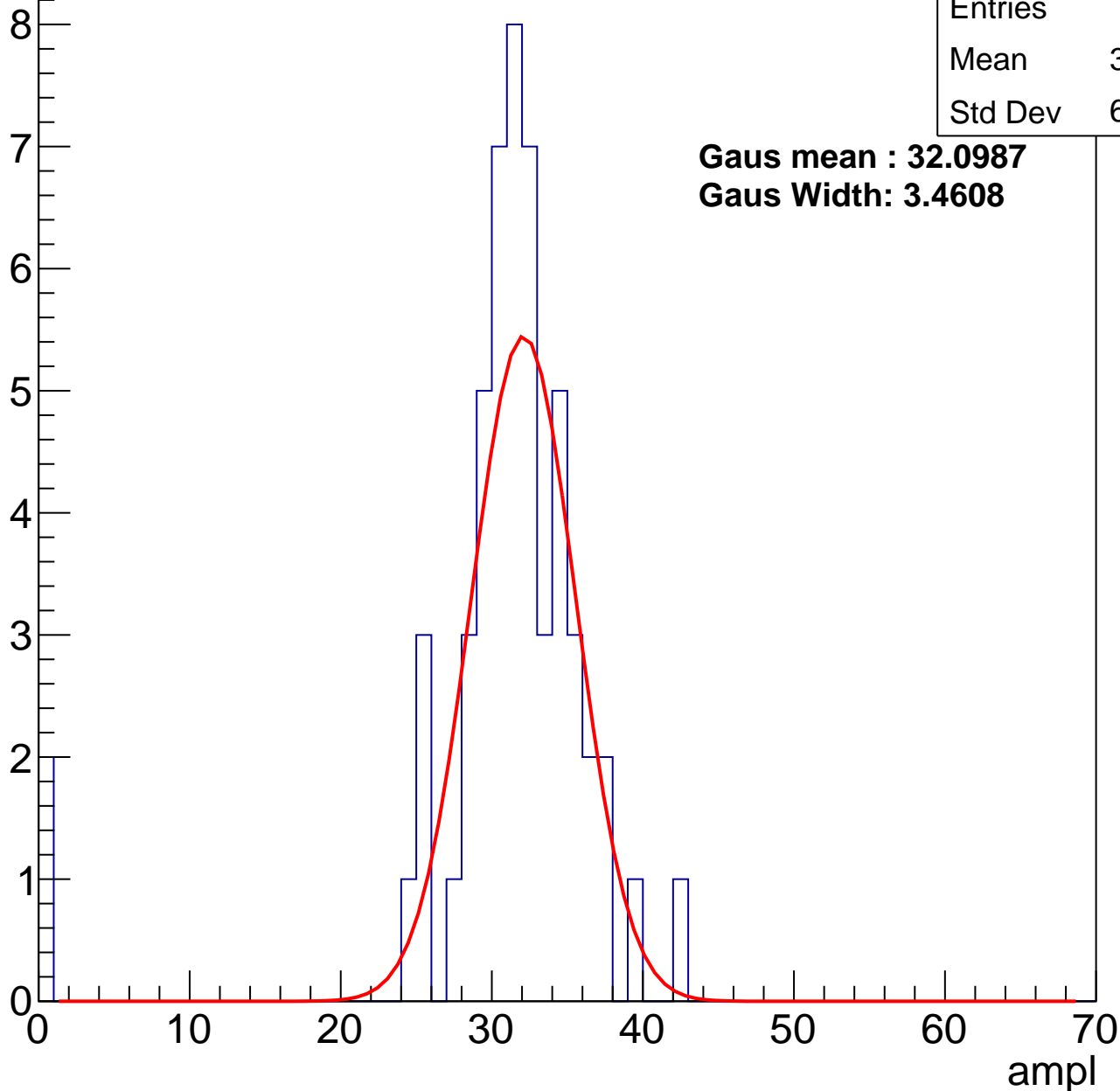
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 54    |
| Mean    | 30.33 |
| Std Dev | 6.864 |

**Gaus mean : 32.0987**

**Gaus Width: 3.4608**



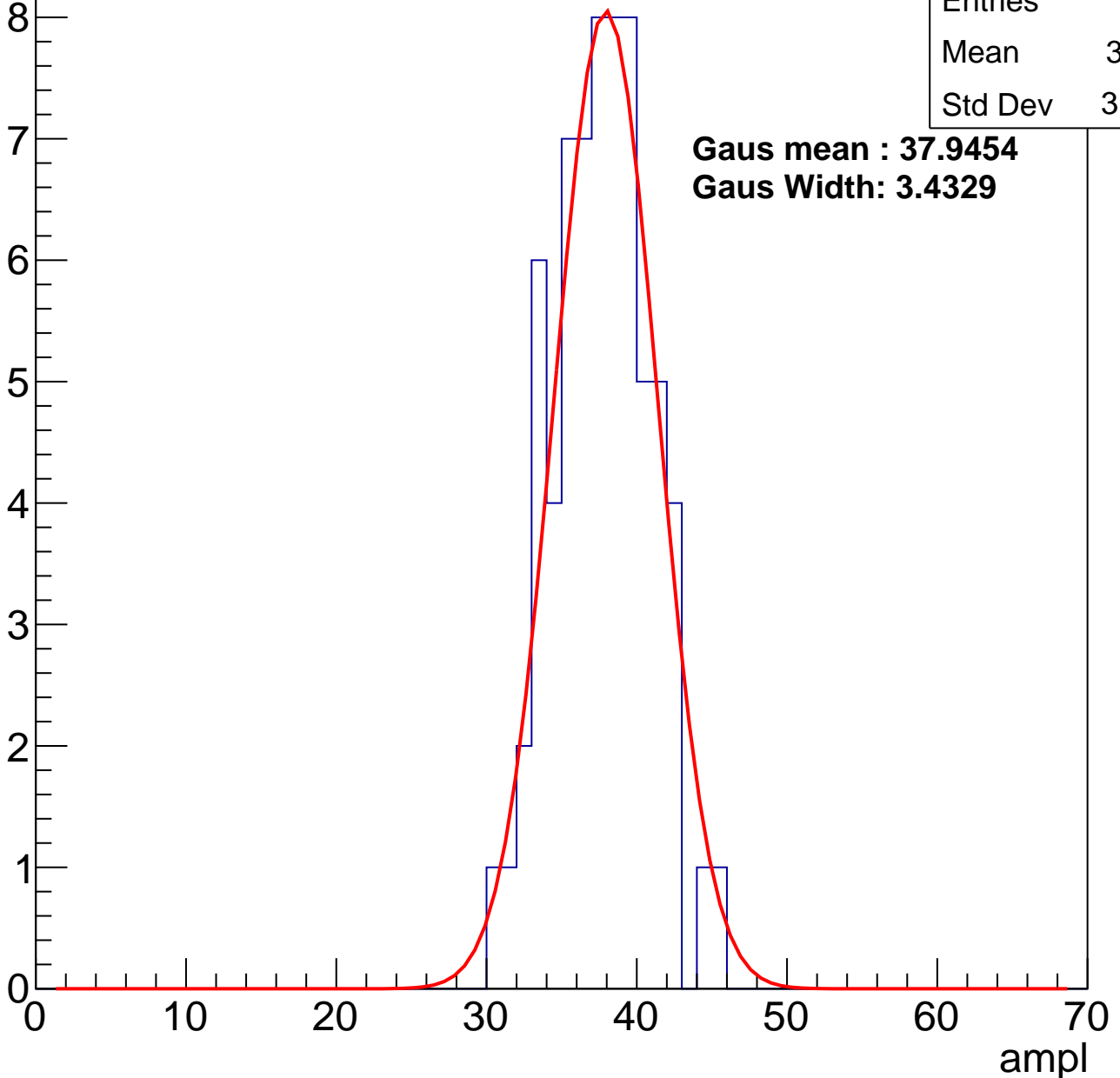
# B0L001S, U2-ch126, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 68    |
| Mean    | 37.21 |
| Std Dev | 3.156 |

**Gaus mean : 37.9454**  
**Gaus Width: 3.4329**



# B0L001S, U2-ch126, adc2

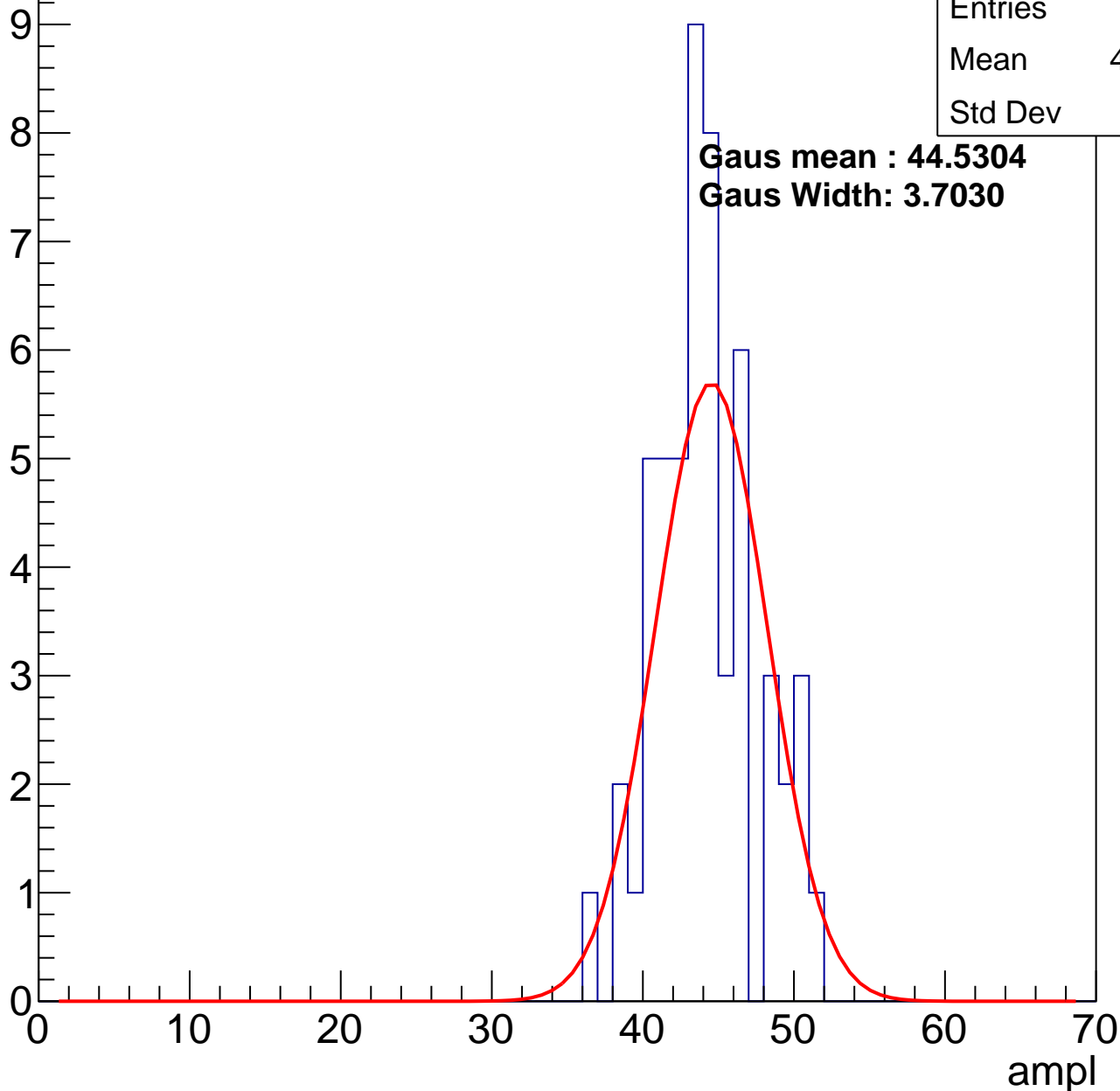
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 54    |
| Mean    | 43.69 |
| Std Dev | 3.31  |

**Gaus mean : 44.5304**

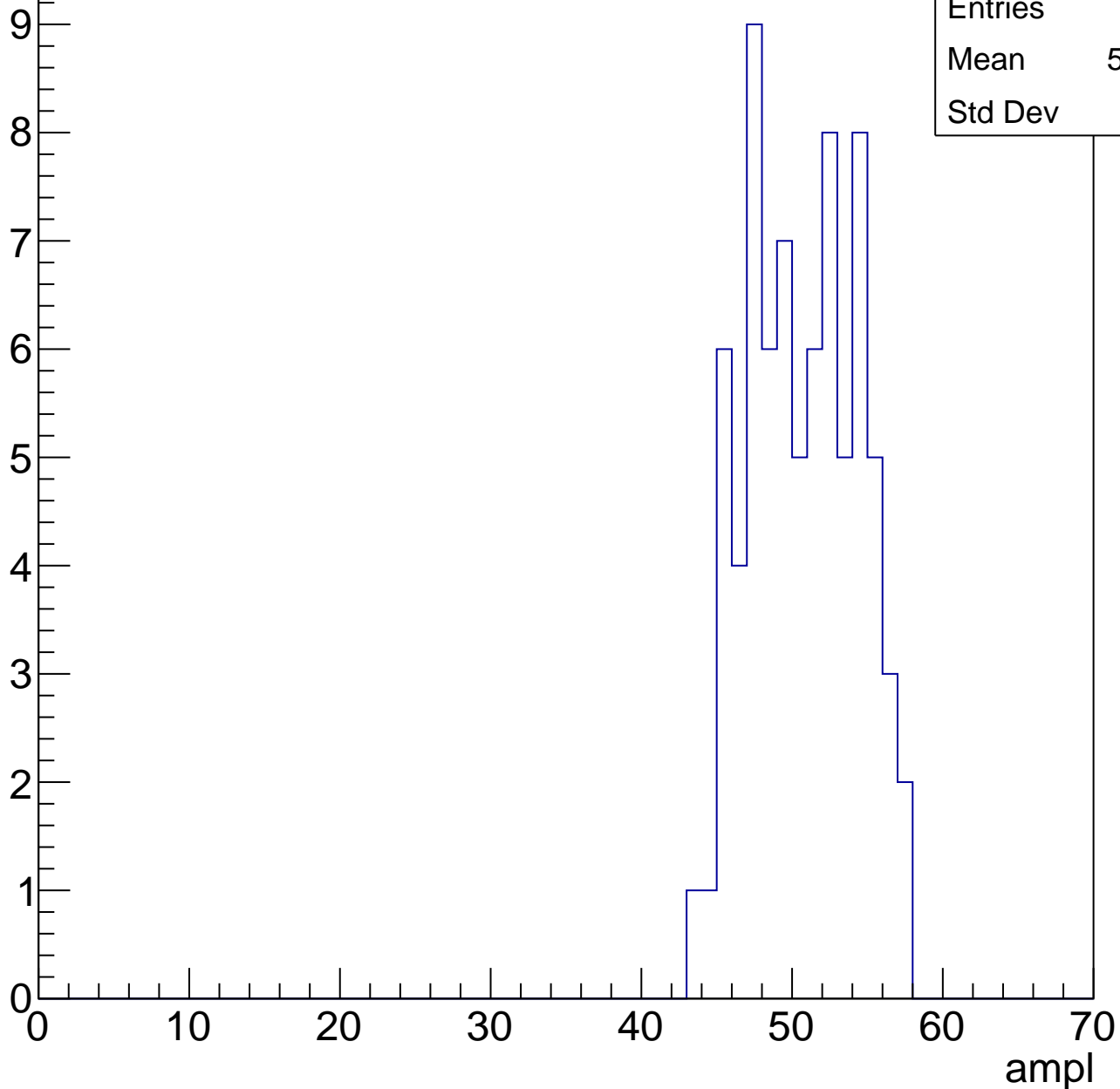
**Gaus Width: 3.7030**



# B0L001S, U2-ch126, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

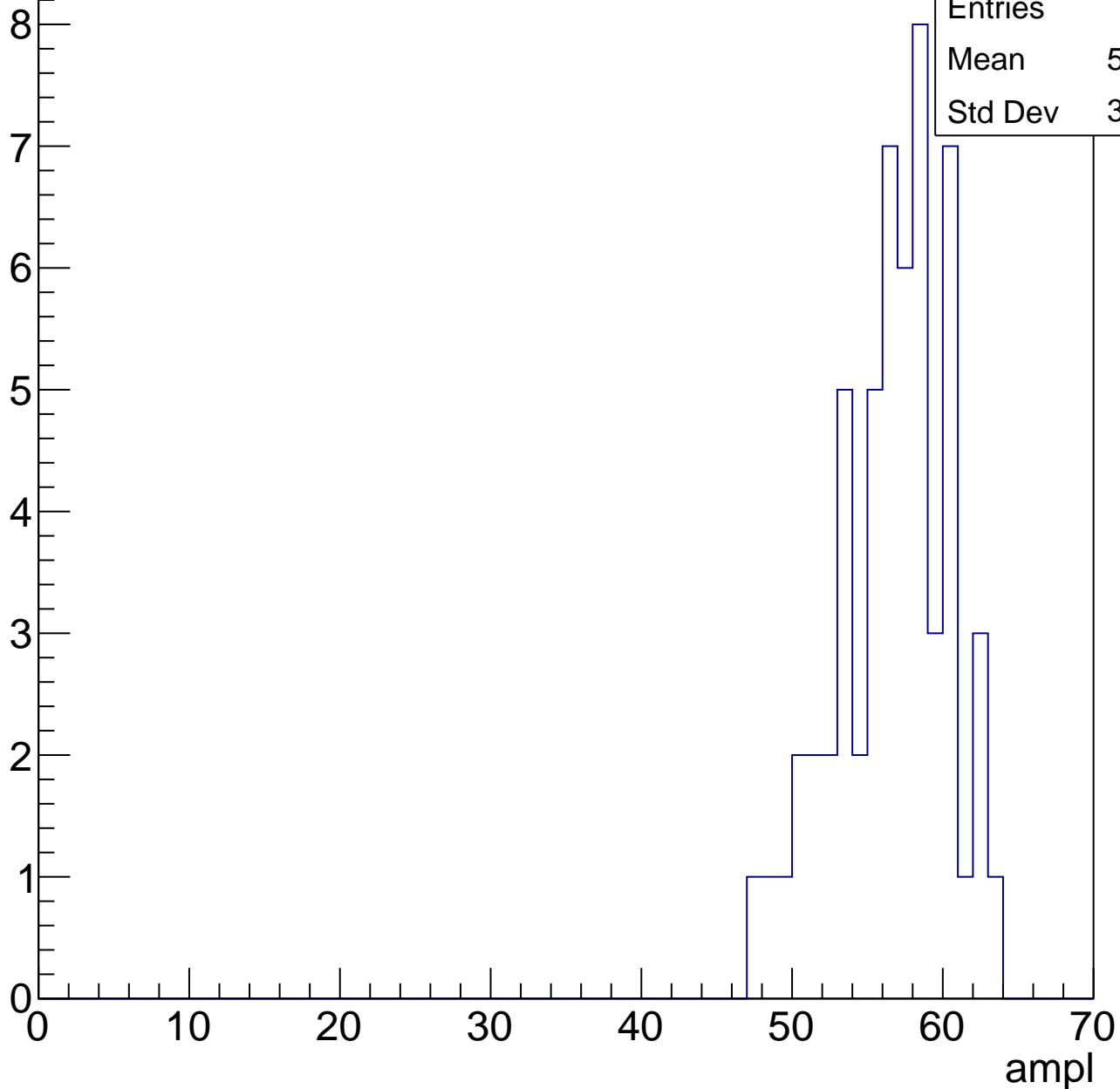
Entry



# B0L001S, U2-ch126, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

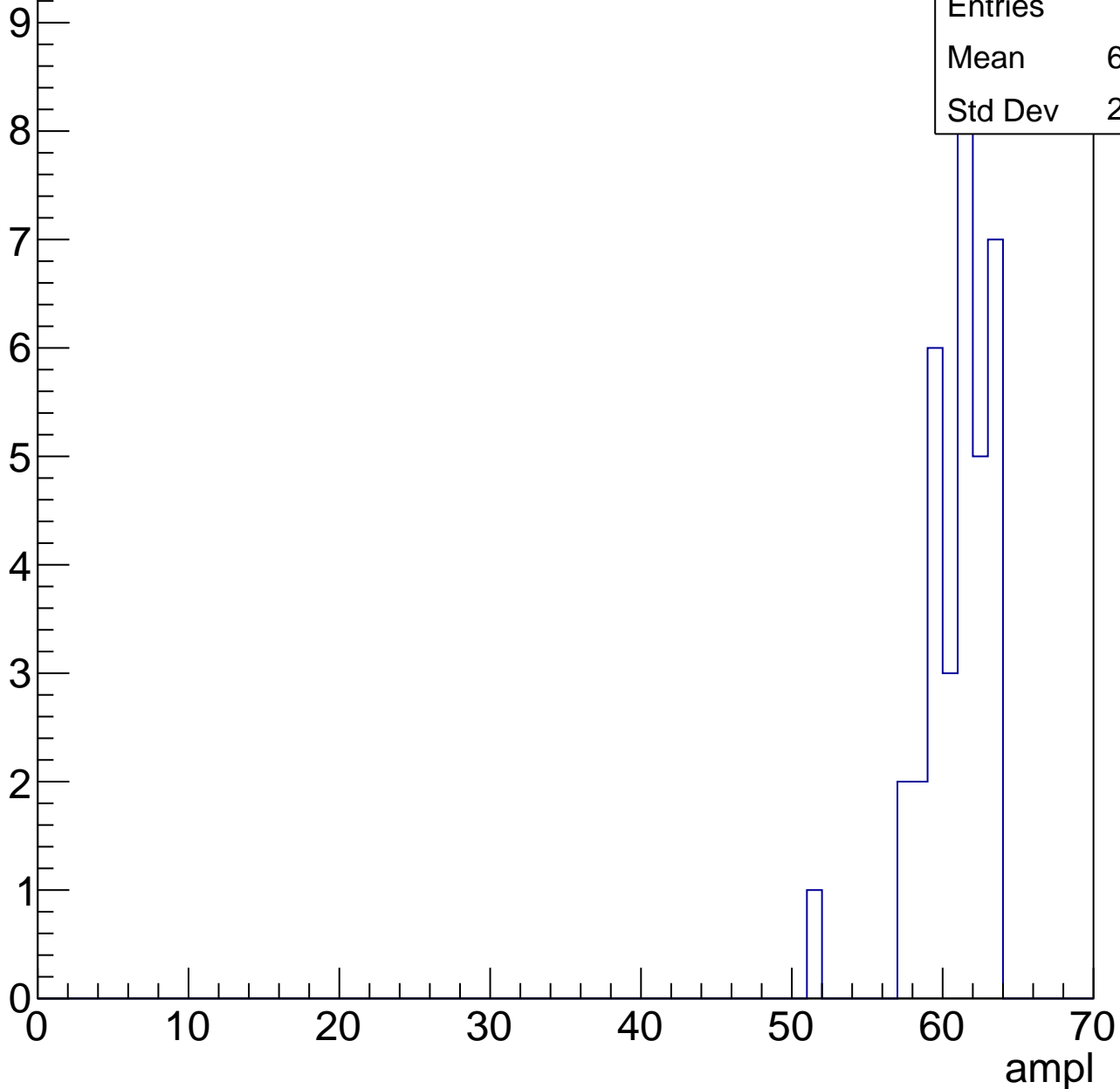


# B0L001S, U2-ch126, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

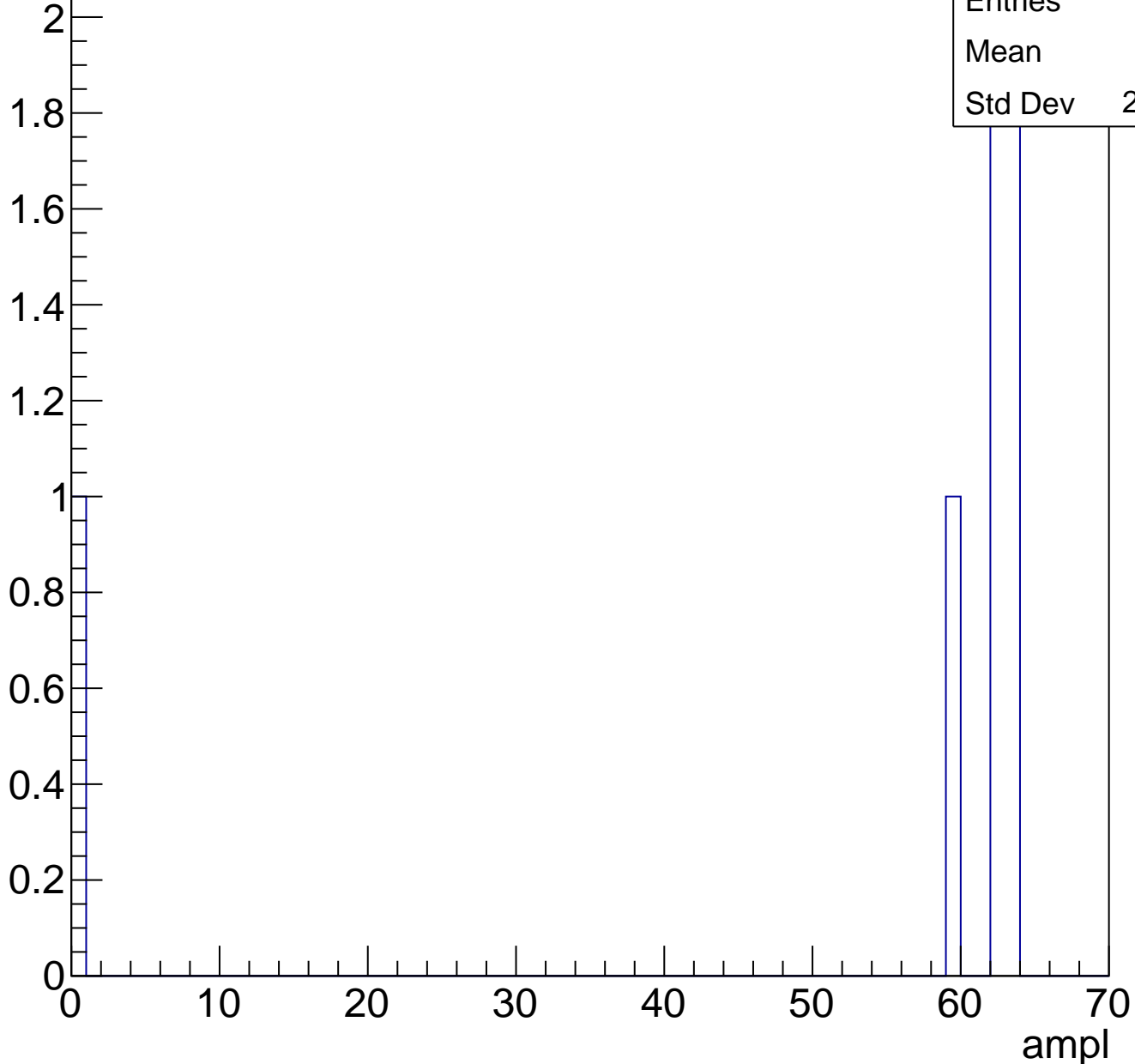
|         |       |
|---------|-------|
| Entries | 35    |
| Mean    | 60.43 |
| Std Dev | 2.382 |



# B0L001S, U2-ch126, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch126, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U2-ch127, adc0

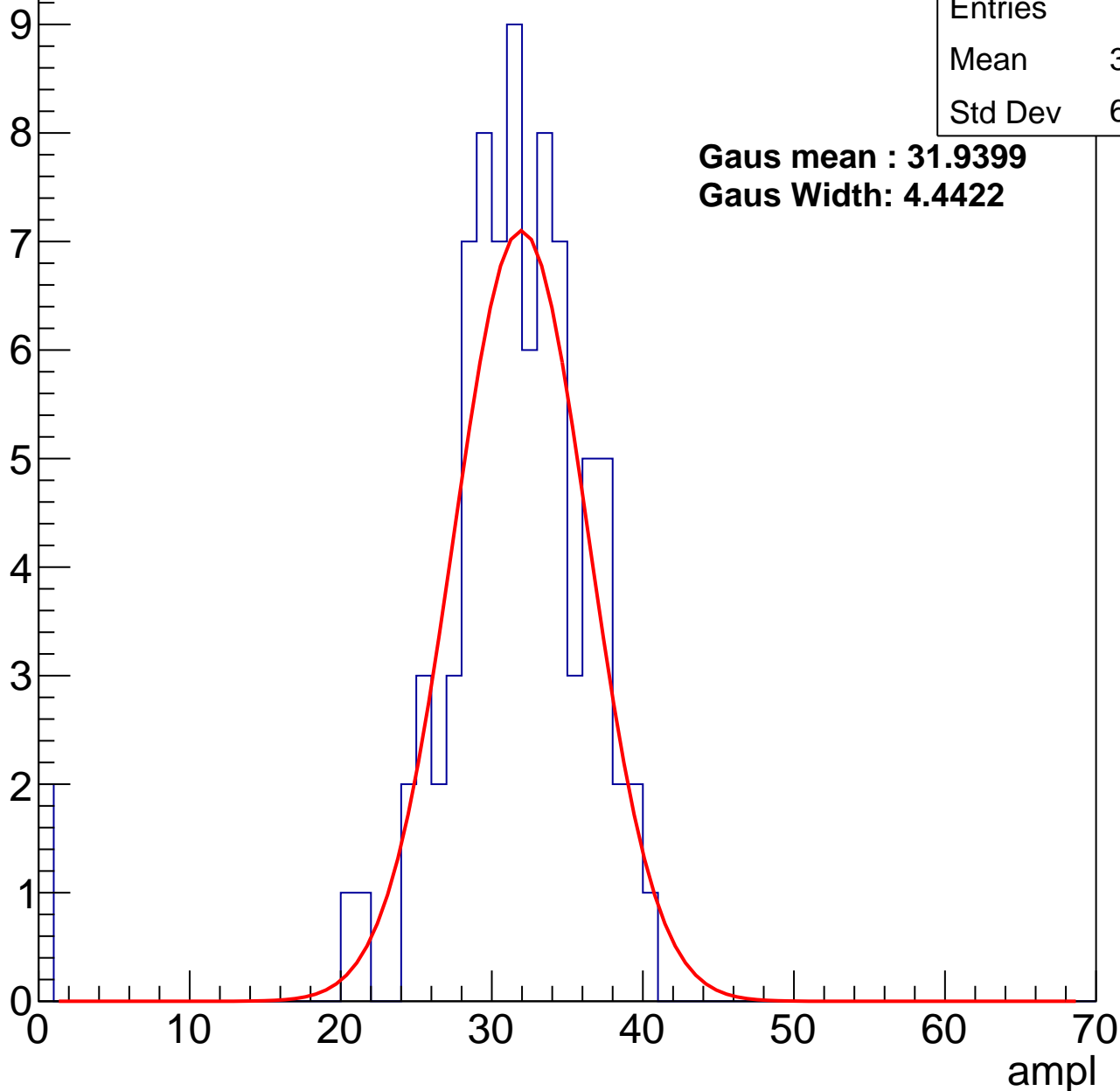
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 84    |
| Mean    | 30.62 |
| Std Dev | 6.266 |

**Gaus mean : 31.9399**

**Gaus Width: 4.4422**



# B0L001S, U2-ch127, adc1

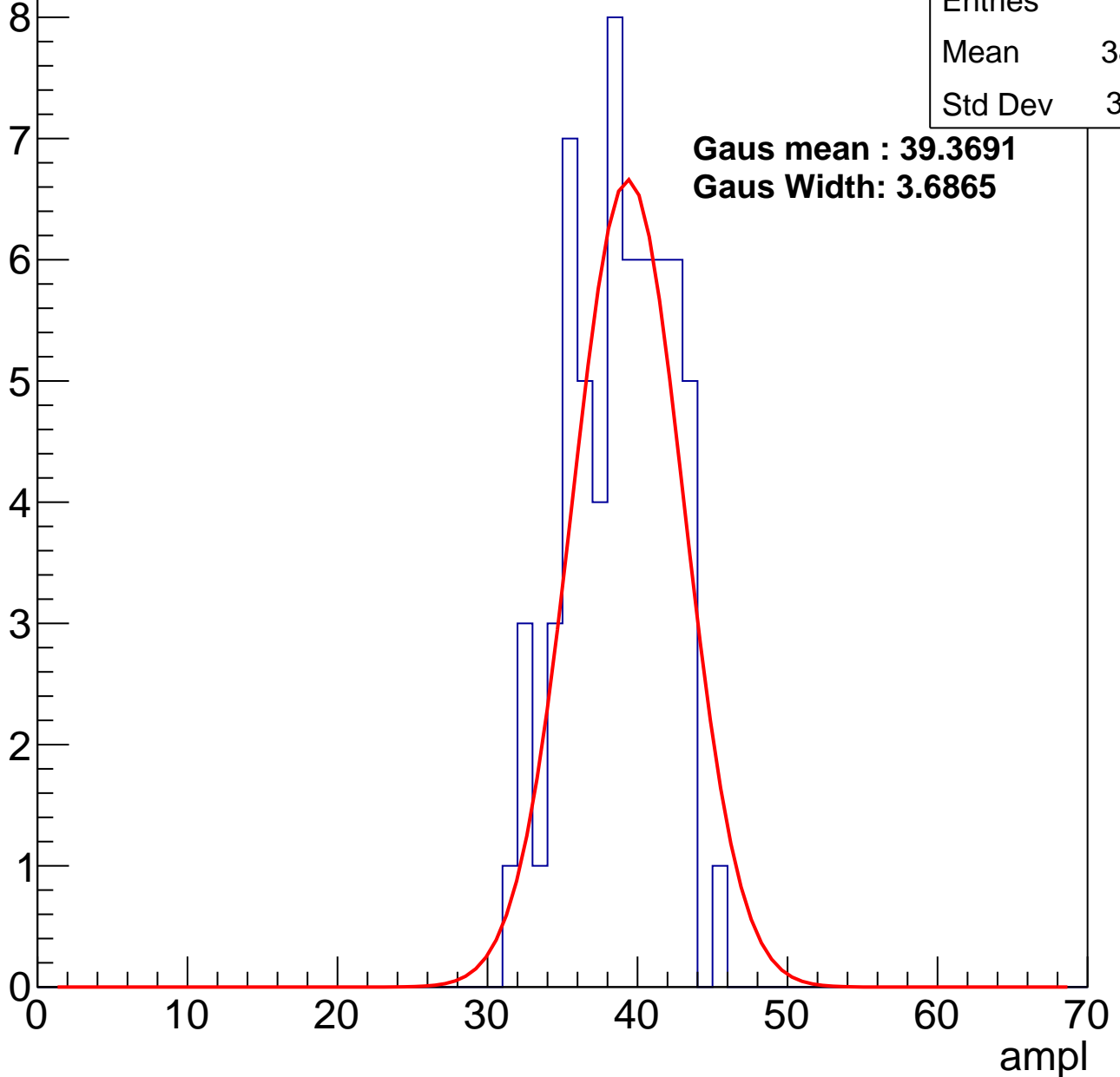
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 62    |
| Mean    | 38.24 |
| Std Dev | 3.281 |

**Gaus mean : 39.3691**

**Gaus Width: 3.6865**



# B0L001S, U2-ch127, adc2

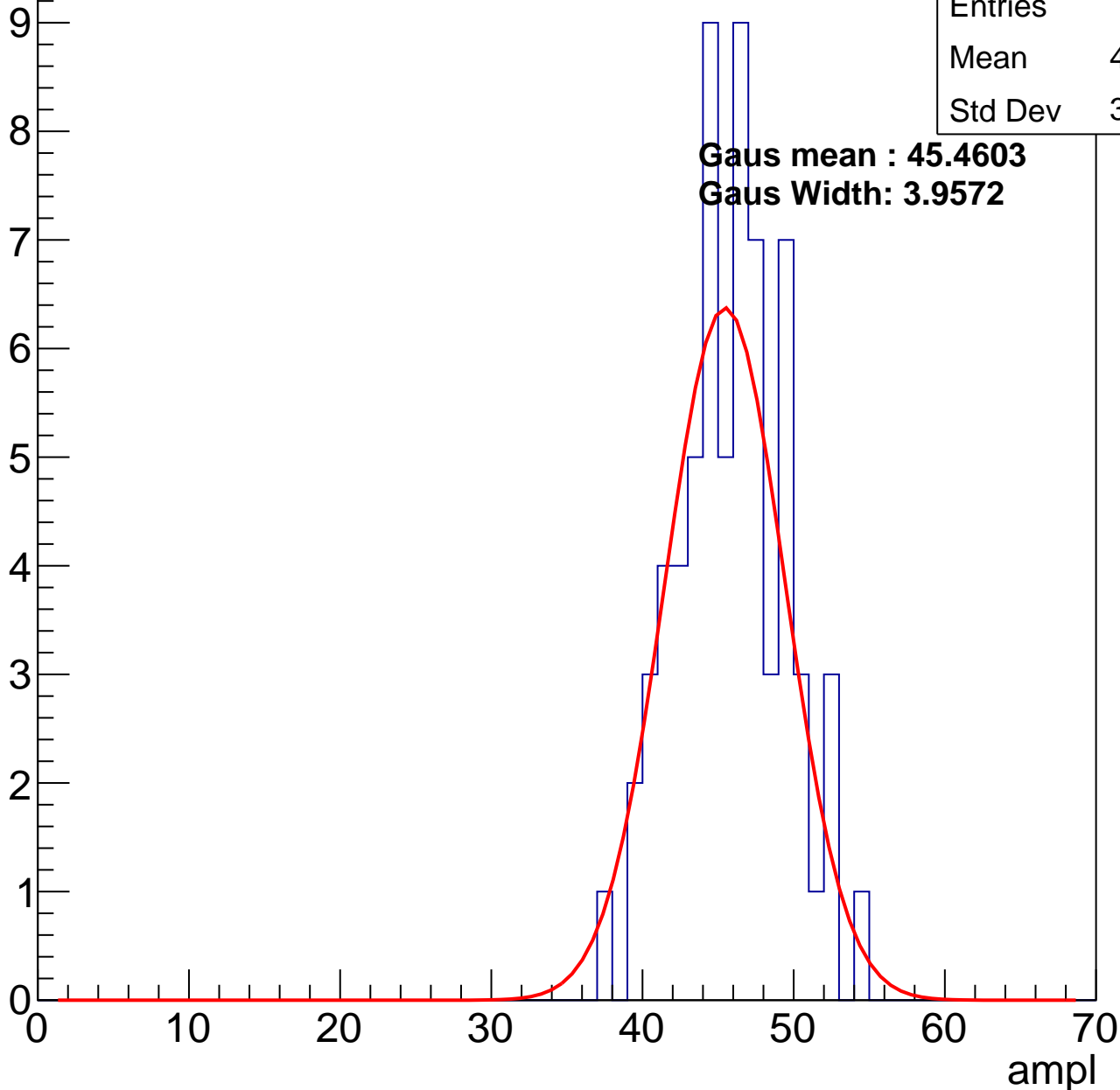
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 67    |
| Mean    | 45.43 |
| Std Dev | 3.546 |

**Gaus mean : 45.4603**

**Gaus Width: 3.9572**

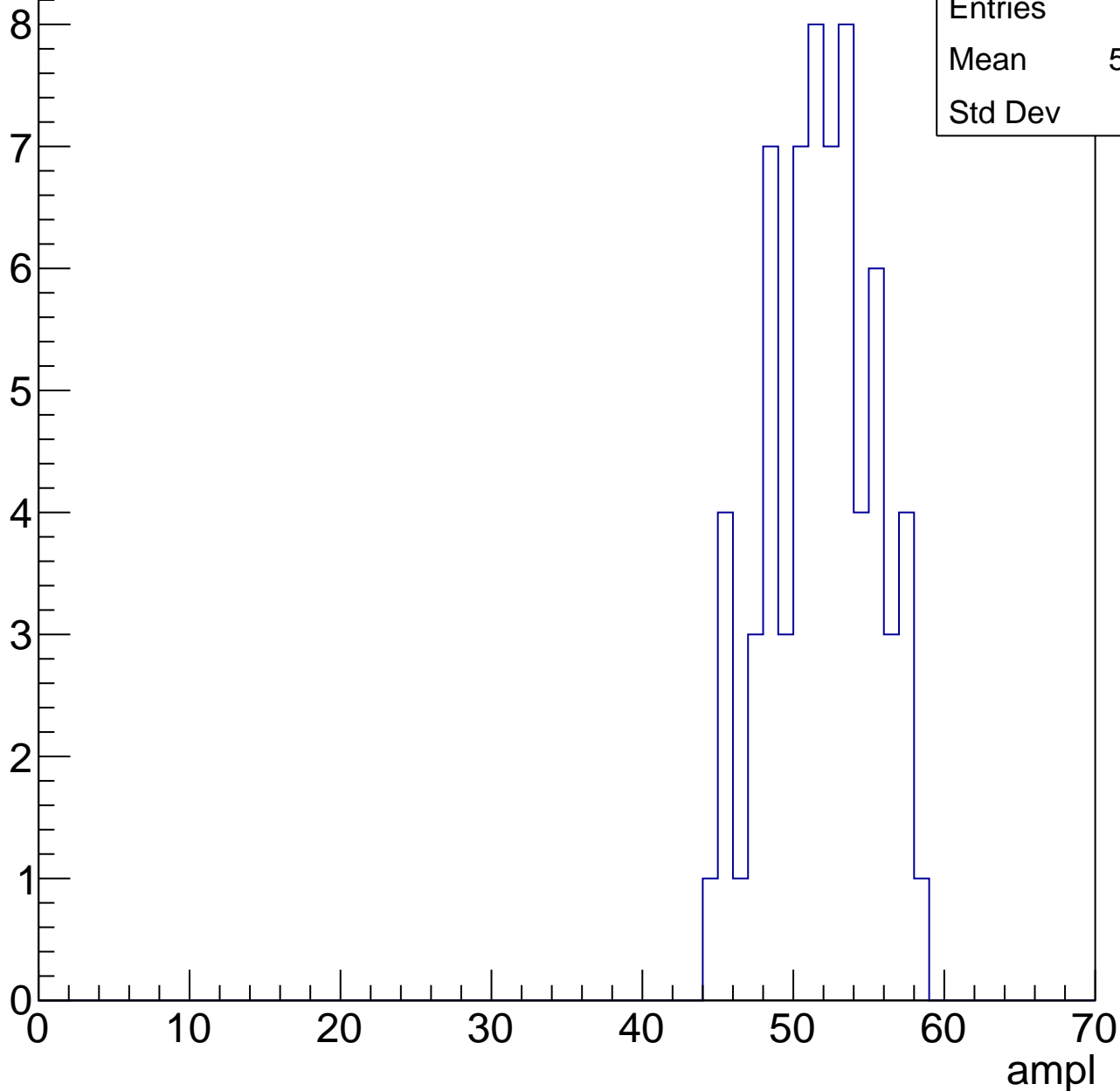


# B0L001S, U2-ch127, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

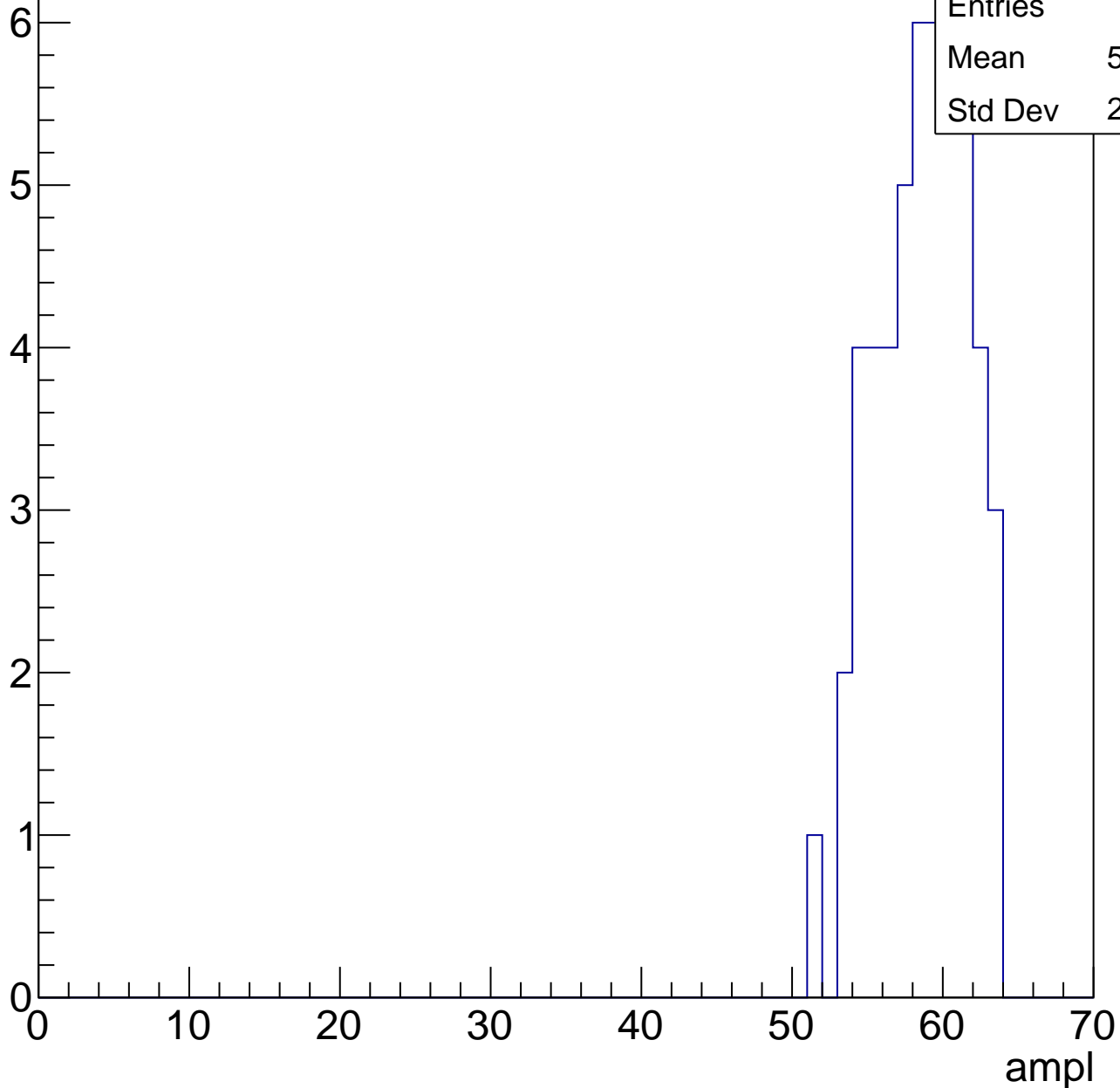
|         |       |
|---------|-------|
| Entries | 67    |
| Mean    | 51.34 |
| Std Dev | 3.41  |



# B0L001S, U2-ch127, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



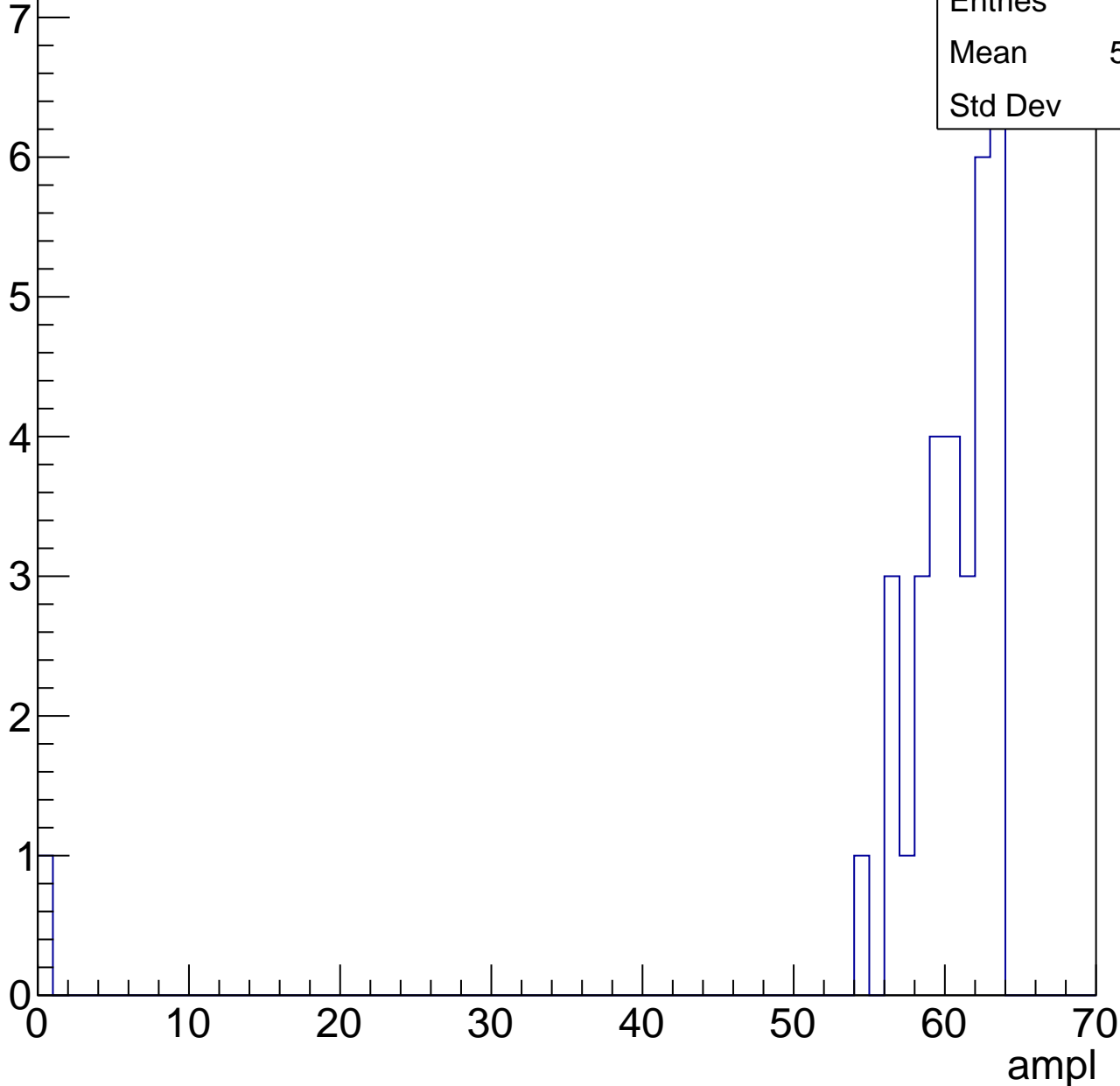
|         |       |
|---------|-------|
| Entries | 51    |
| Mean    | 58.18 |
| Std Dev | 2.942 |

# B0L001S, U2-ch127, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

|         |       |
|---------|-------|
| Entries | 33    |
| Mean    | 58.33 |
| Std Dev | 10.6  |



# B0L001S, U2-ch127, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U2-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



|         |   |
|---------|---|
| Entries | 1 |
| Mean    | 0 |
| Std Dev | 0 |

# B0L001S, U2-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

