



# B1L103S, U21-ch0, adc0

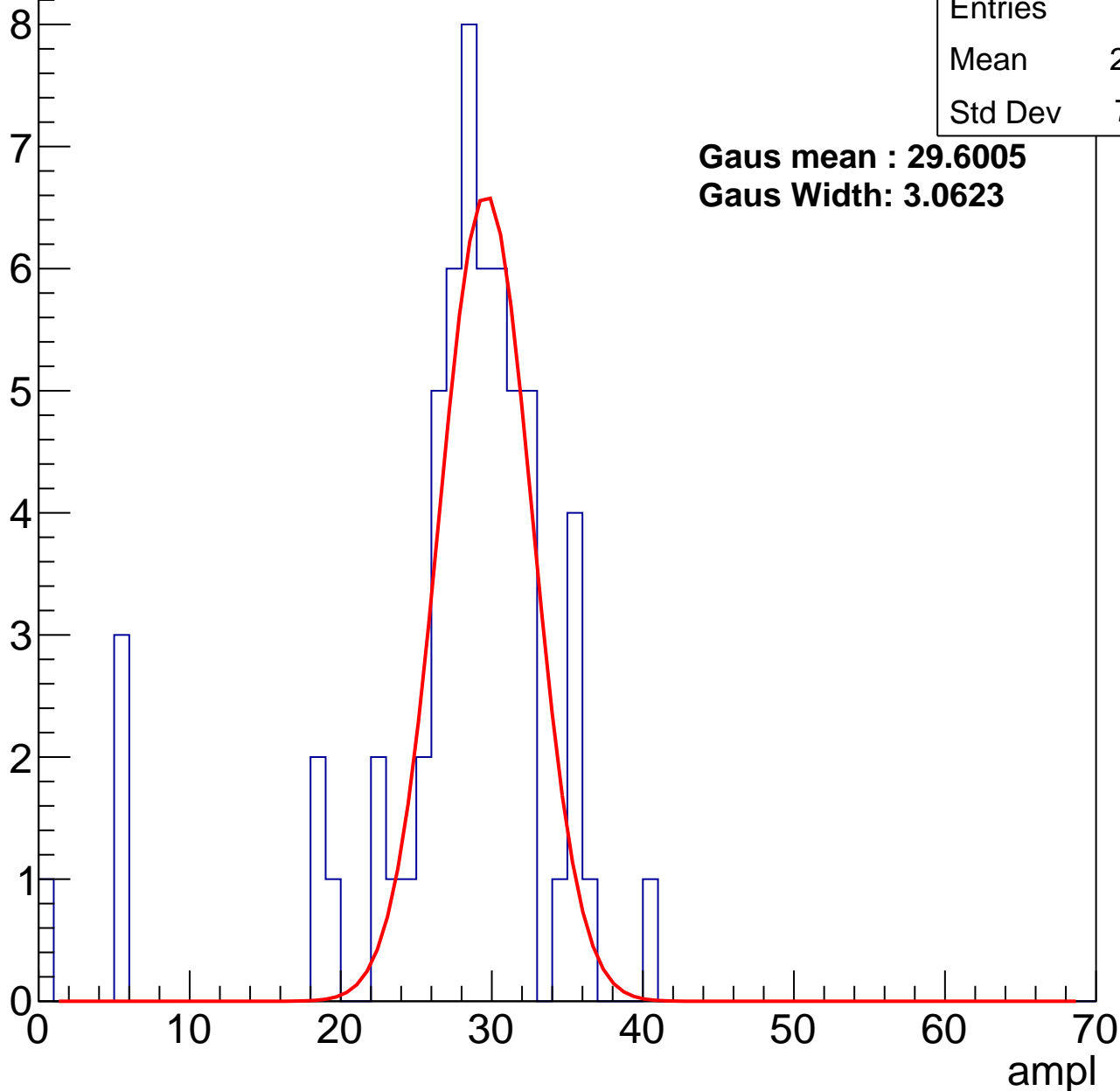
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	26.98
Std Dev	7.401

**Gaus mean : 29.6005**

**Gaus Width: 3.0623**



# B1L103S, U21-ch0, adc1

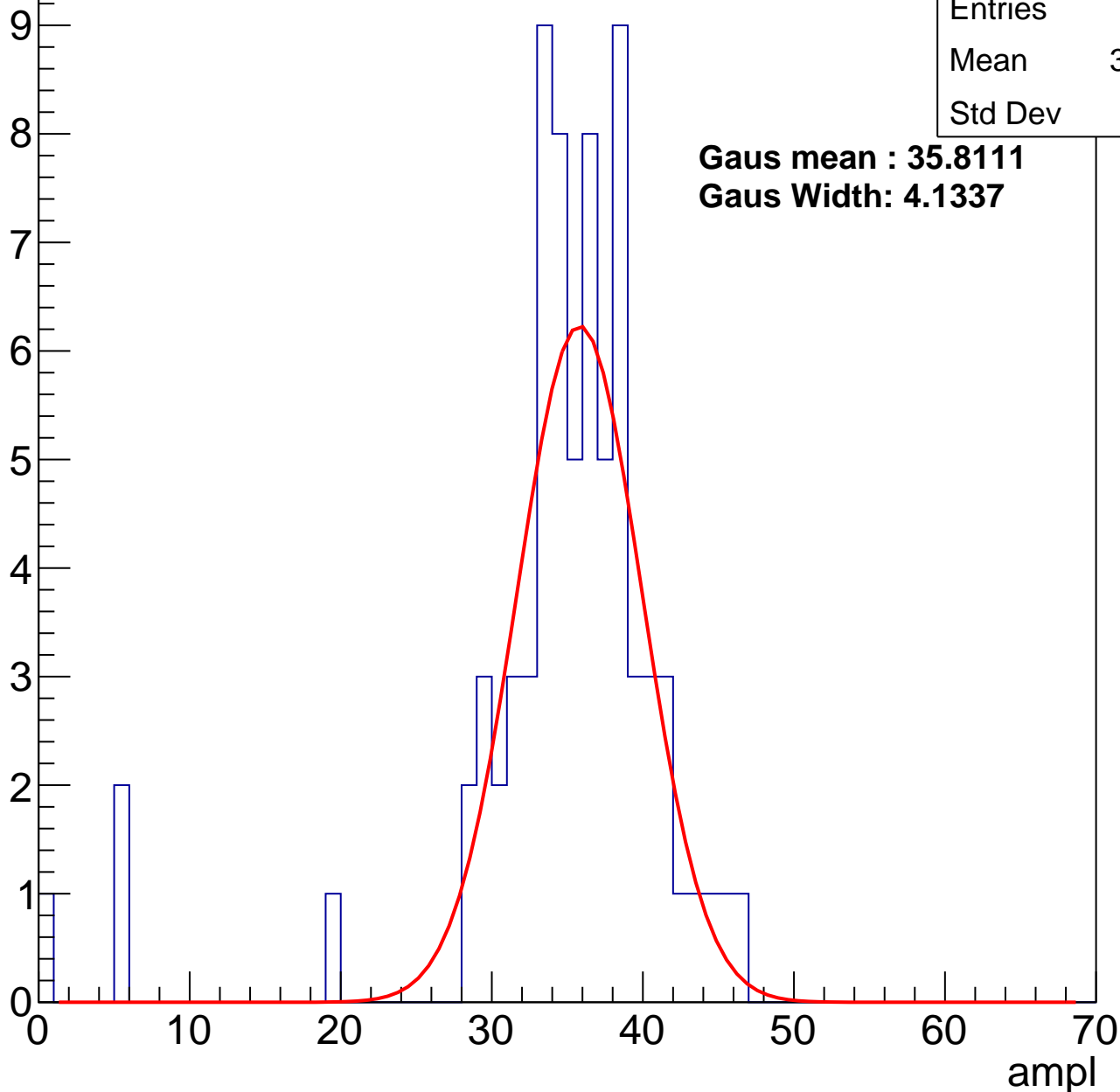
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	34.13
Std Dev	7.62

**Gaus mean : 35.8111**

**Gaus Width: 4.1337**



# B1L103S, U21-ch0, adc2

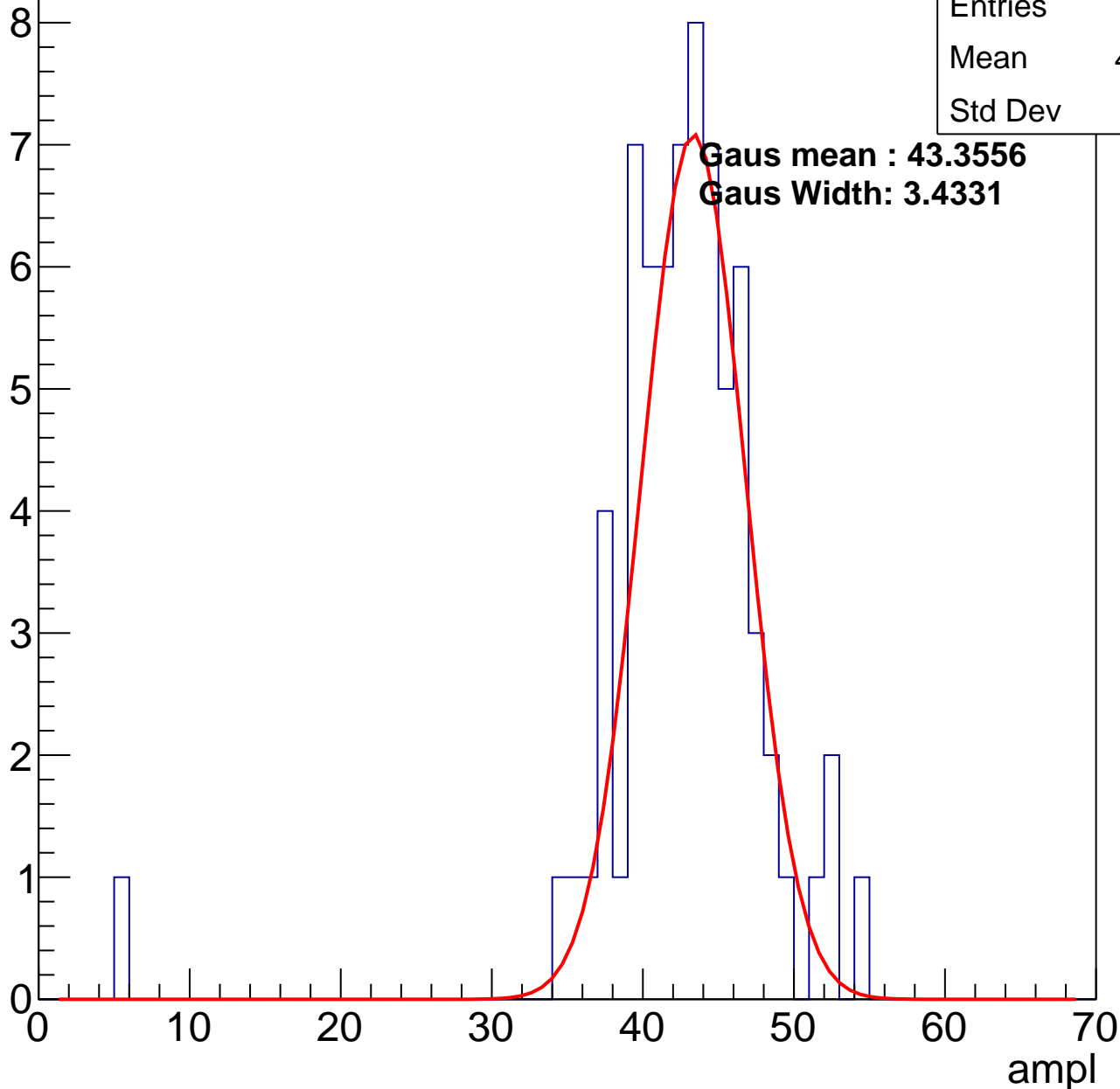
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	42.21
Std Dev	5.96

**Gaus mean : 43.3556**

**Gaus Width: 3.4331**

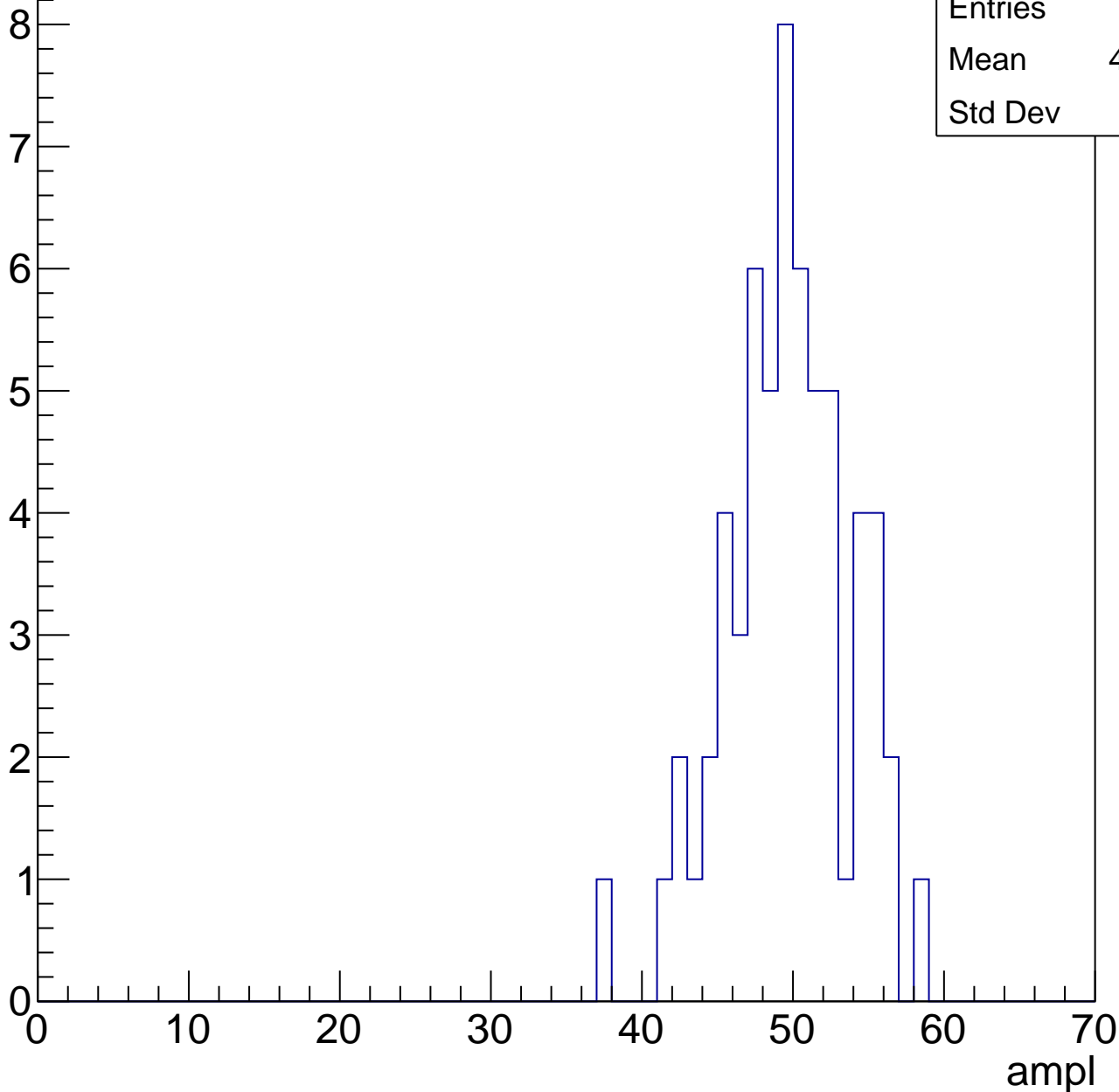


# B1L103S, U21-ch0, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	49.16
Std Dev	4.09

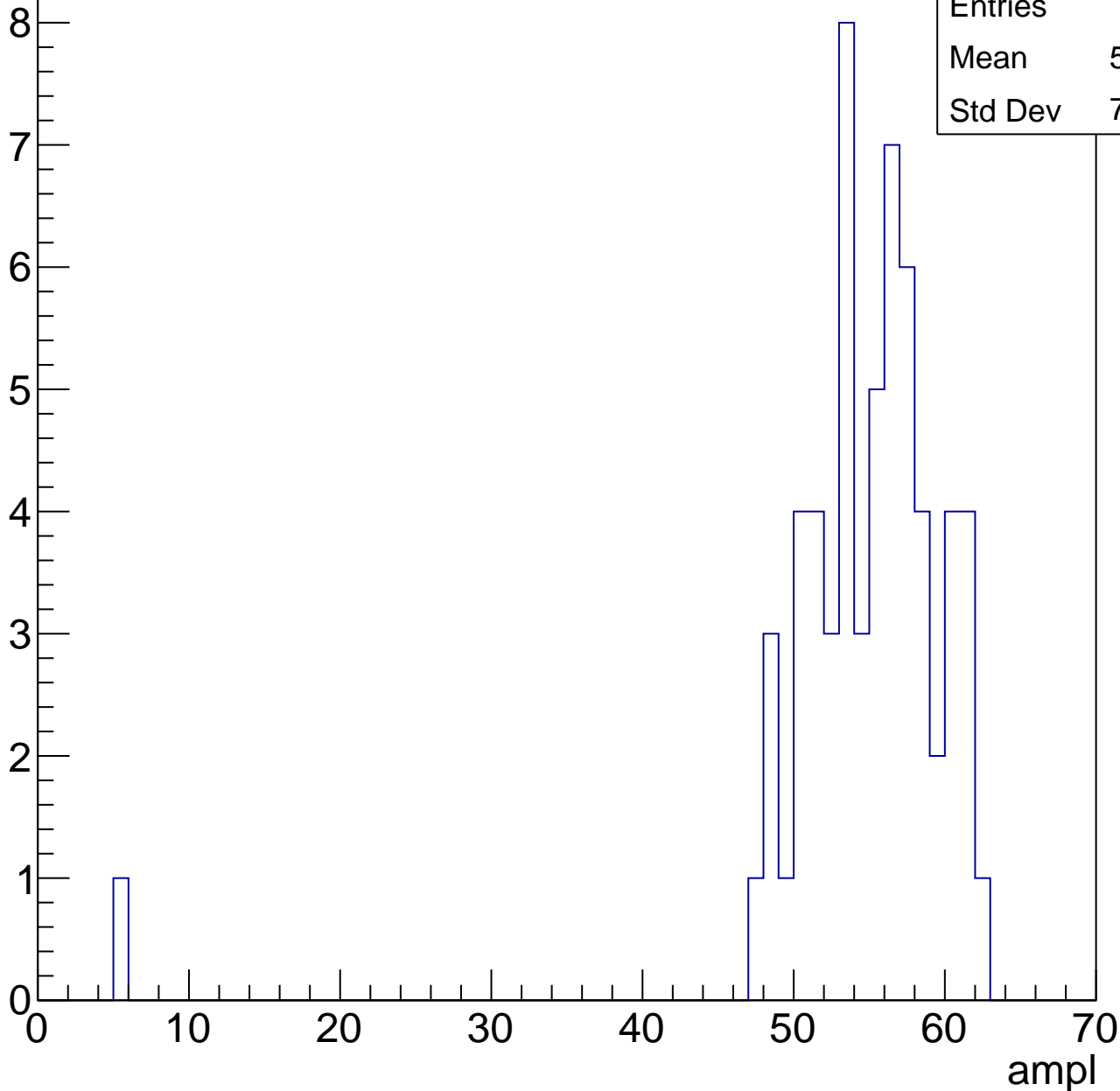


# B1L103S, U21-ch0, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	54.03
Std Dev	7.364

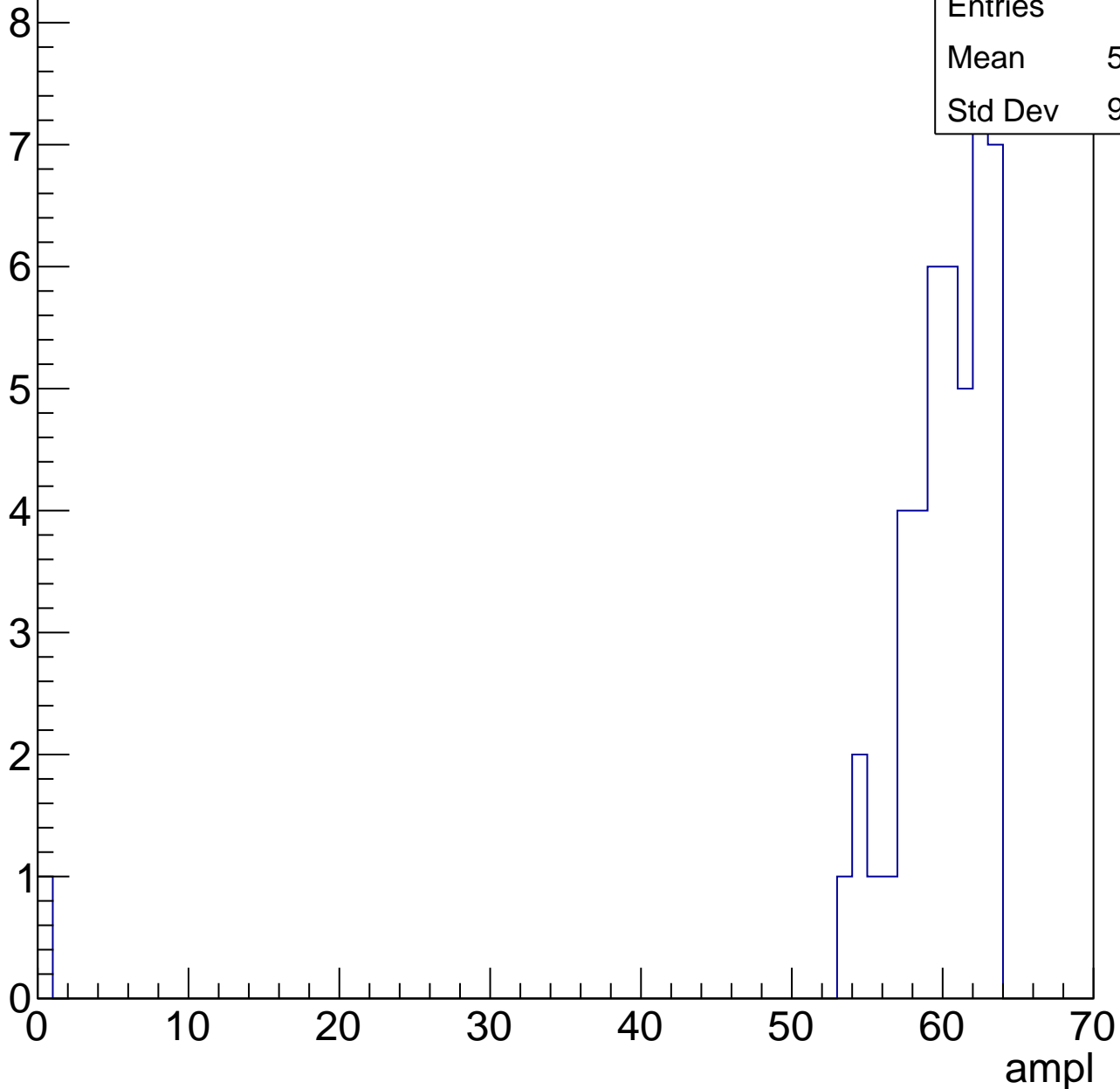


# B1L103S, U21-ch0, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

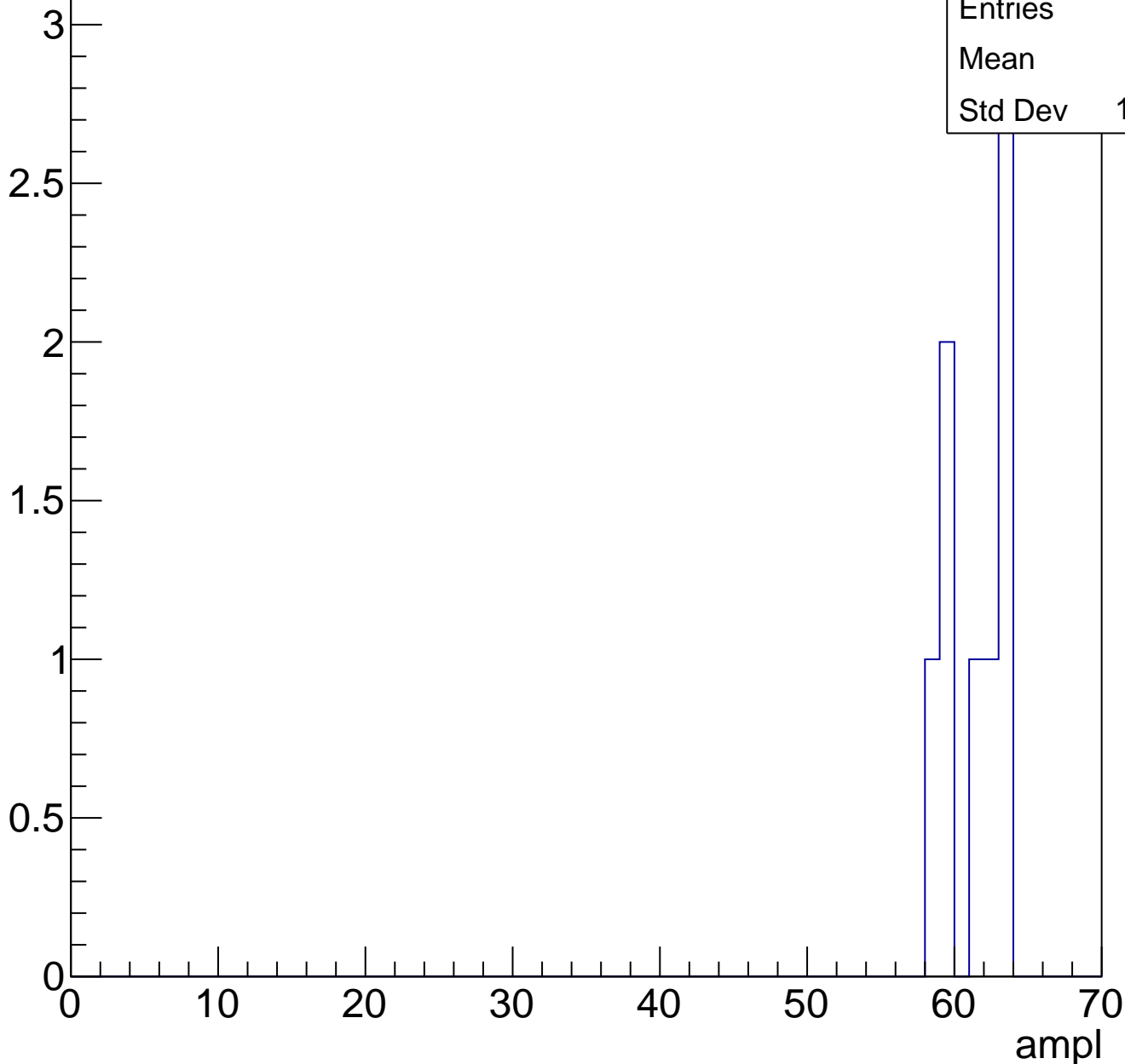
Entries	46
Mean	58.43
Std Dev	9.098



# B1L103S, U21-ch0, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U21-ch0, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U21-ch1, adc0

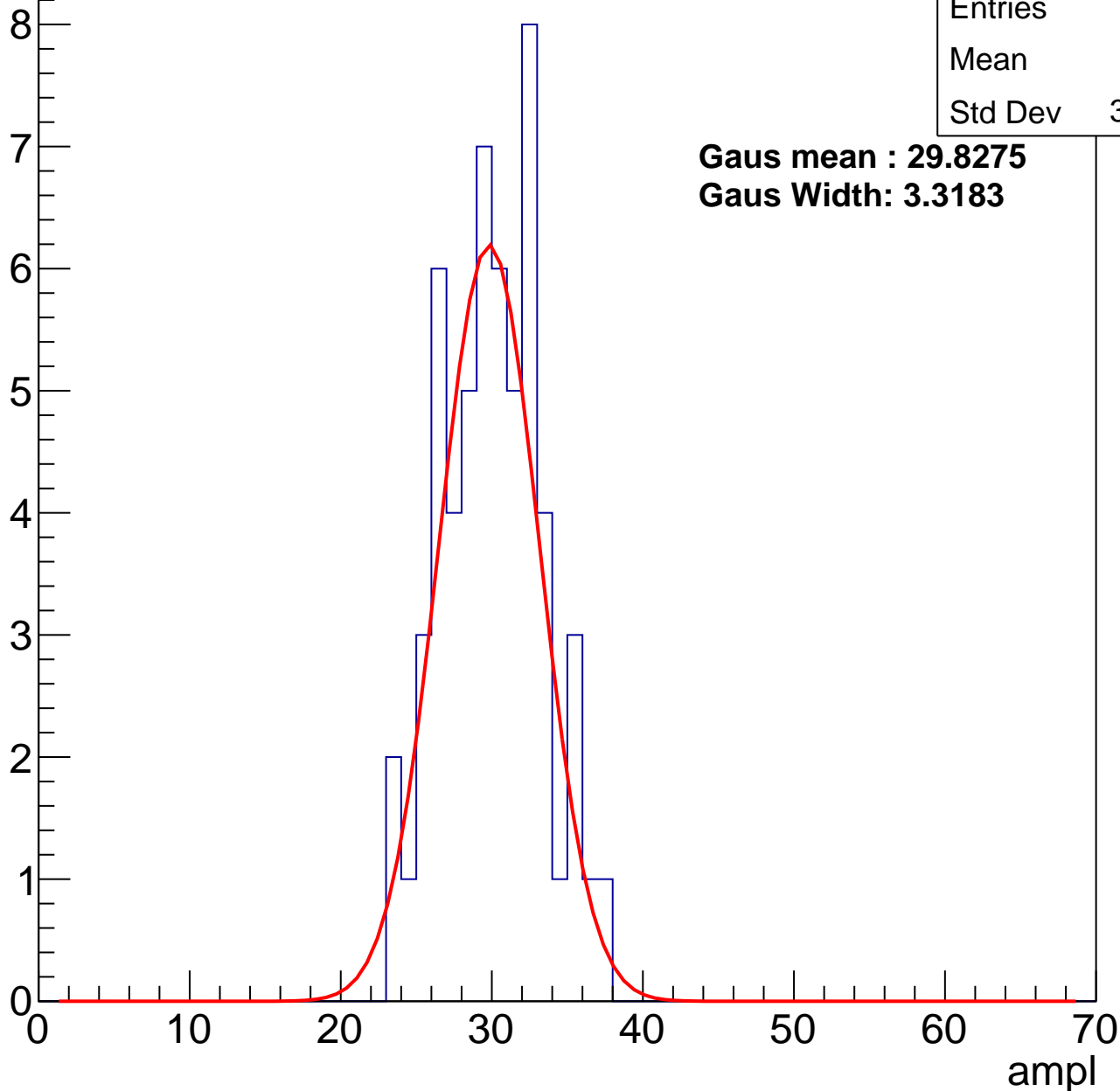
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	29.6
Std Dev	3.265

**Gaus mean : 29.8275**

**Gaus Width: 3.3183**



# B1L103S, U21-ch1, adc1

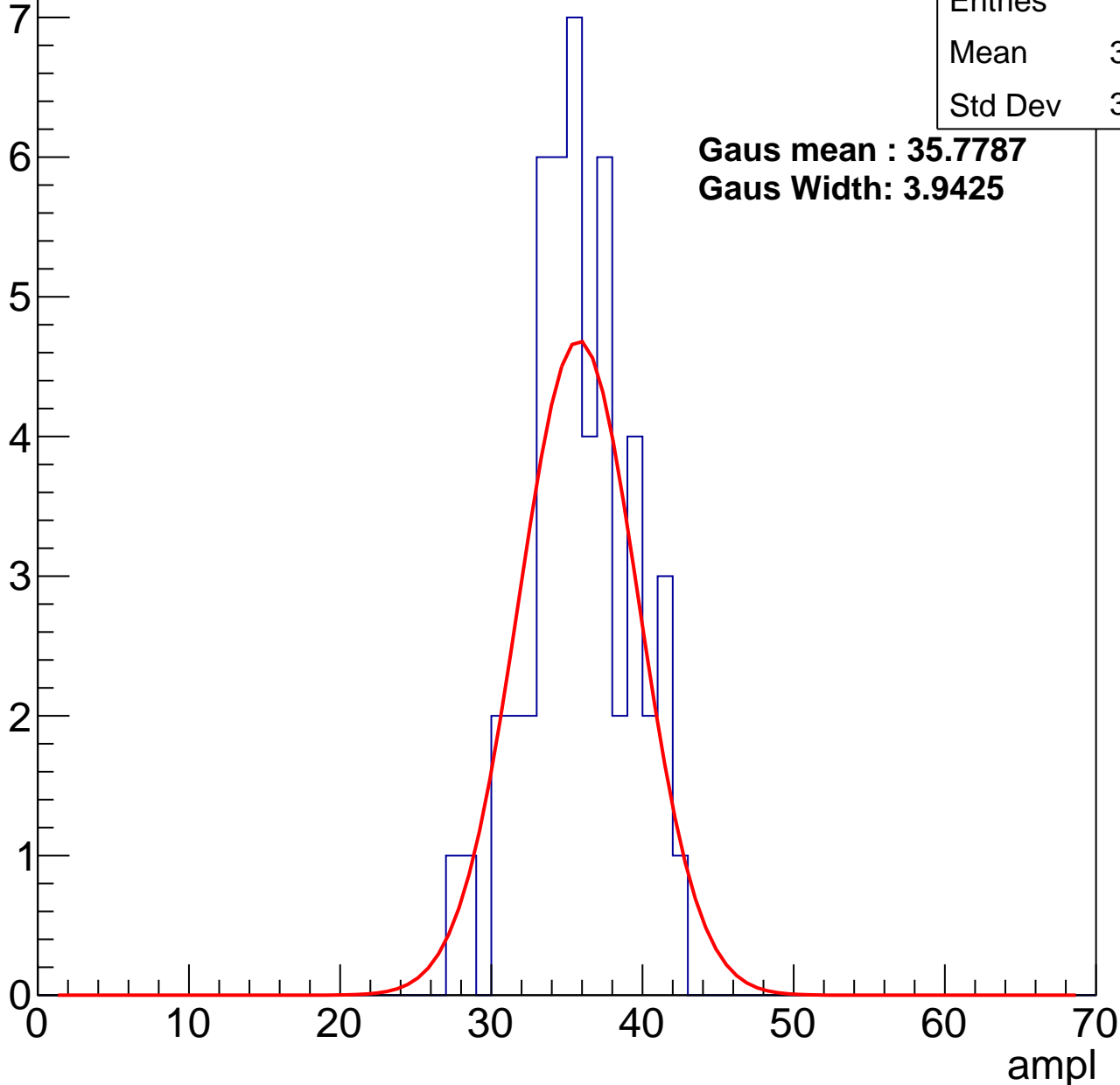
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	35.33
Std Dev	3.365

**Gaus mean : 35.7787**

**Gaus Width: 3.9425**



# B1L103S, U21-ch1, adc2

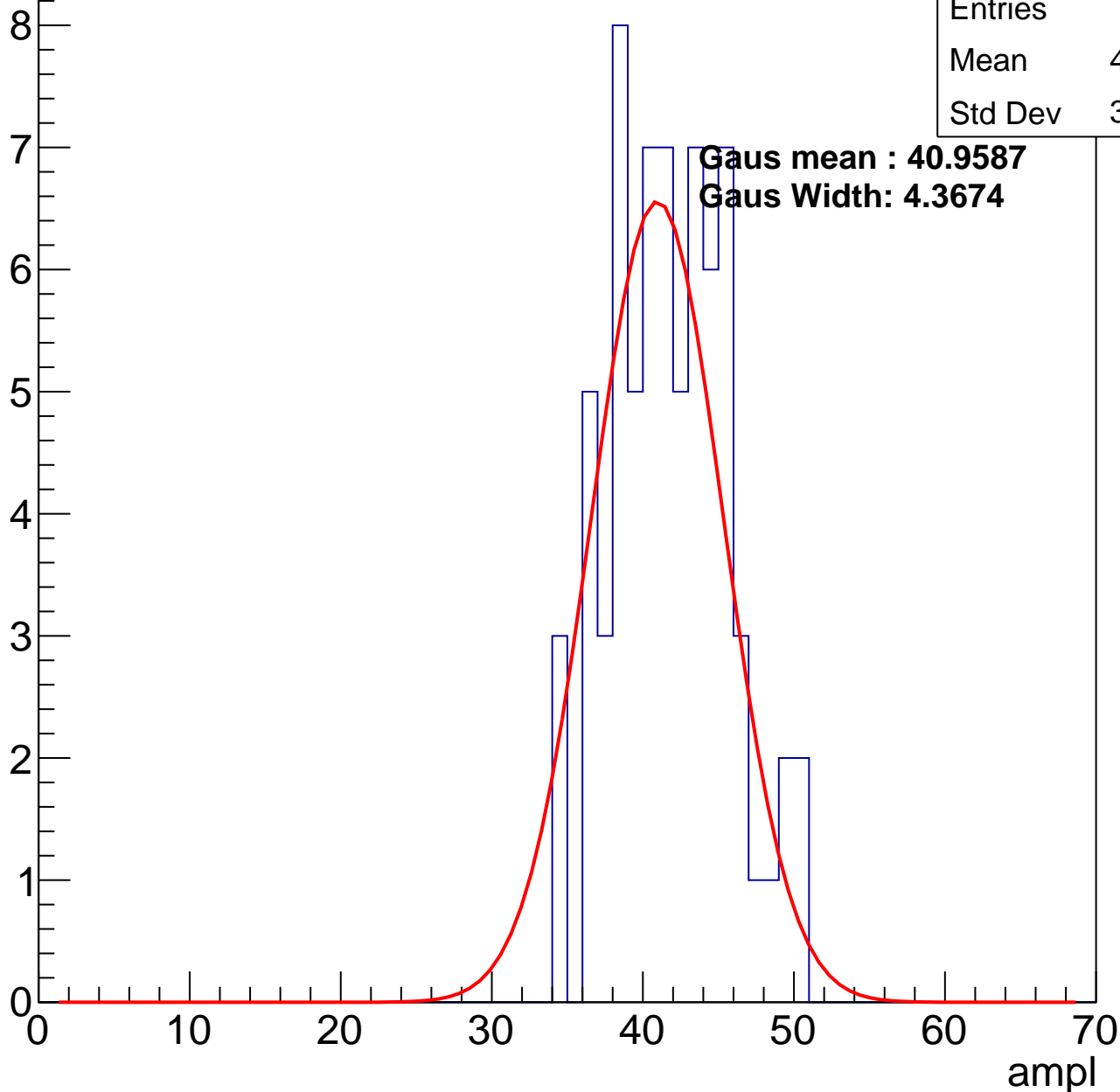
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	41.39
Std Dev	3.832

**Gaus mean : 40.9587**

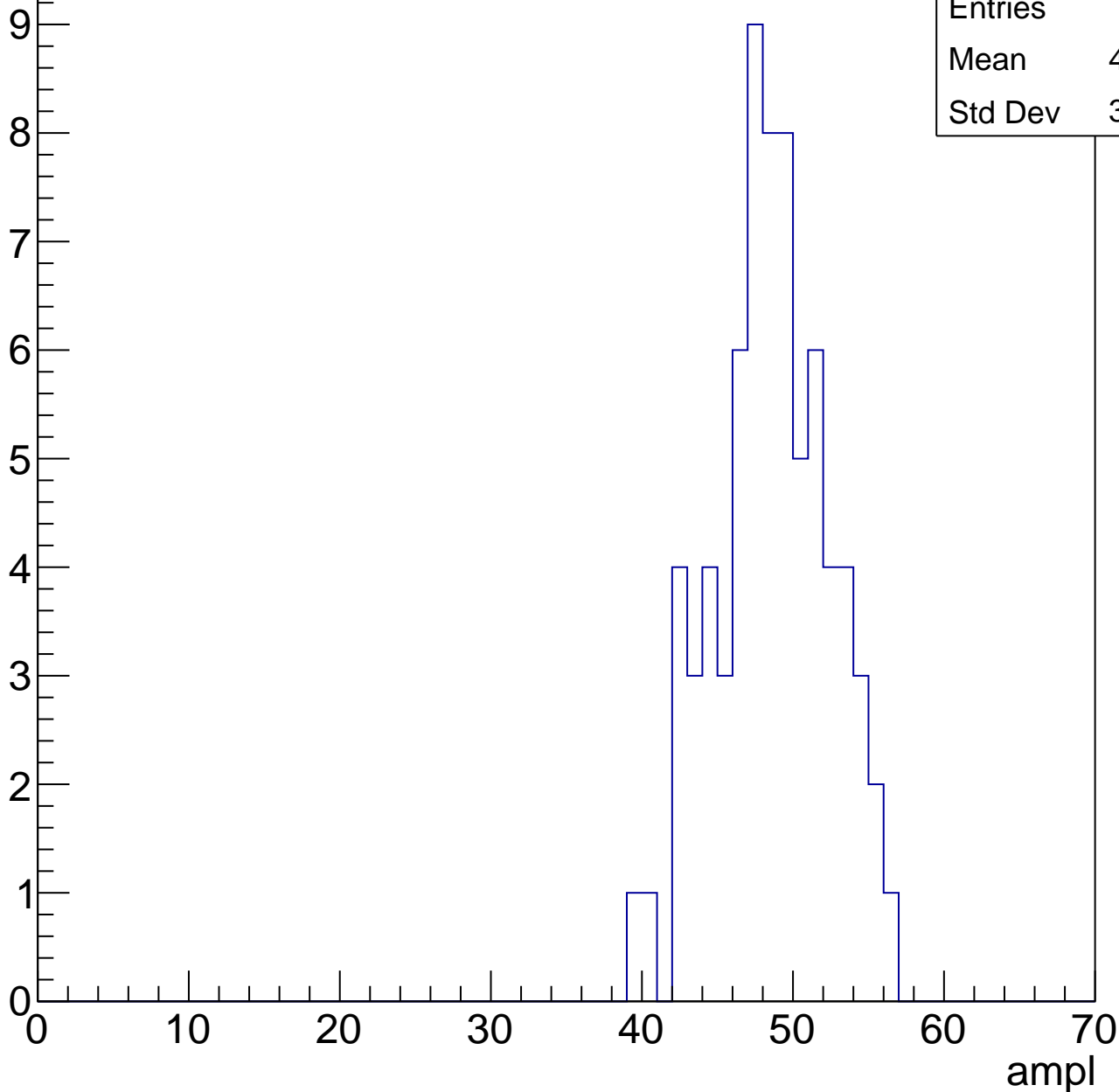
**Gaus Width: 4.3674**



# B1L103S, U21-ch1, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

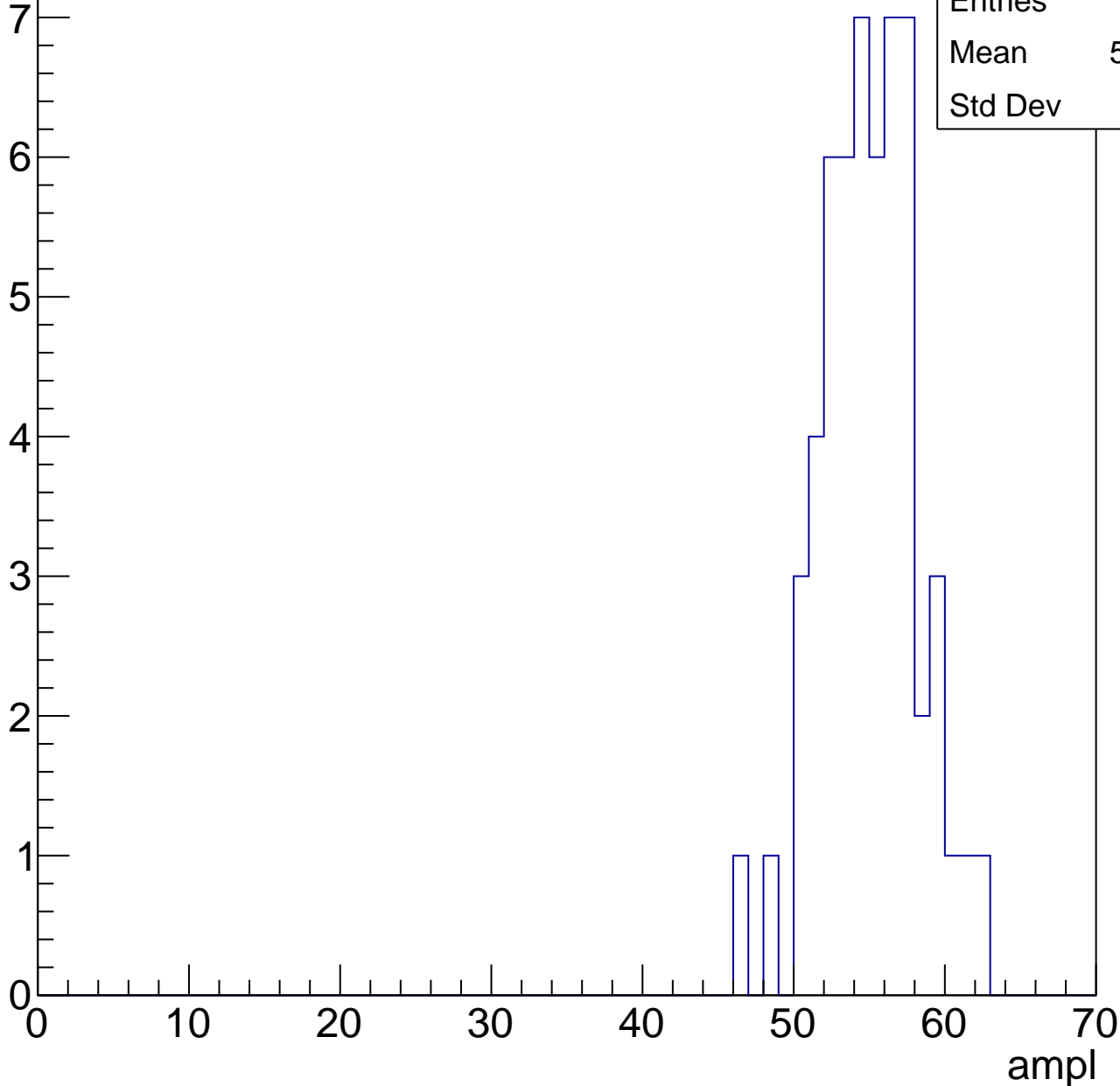


# B1L103S, U21-ch1, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	54.52
Std Dev	3.14



# B1L103S, U21-ch1, adc5

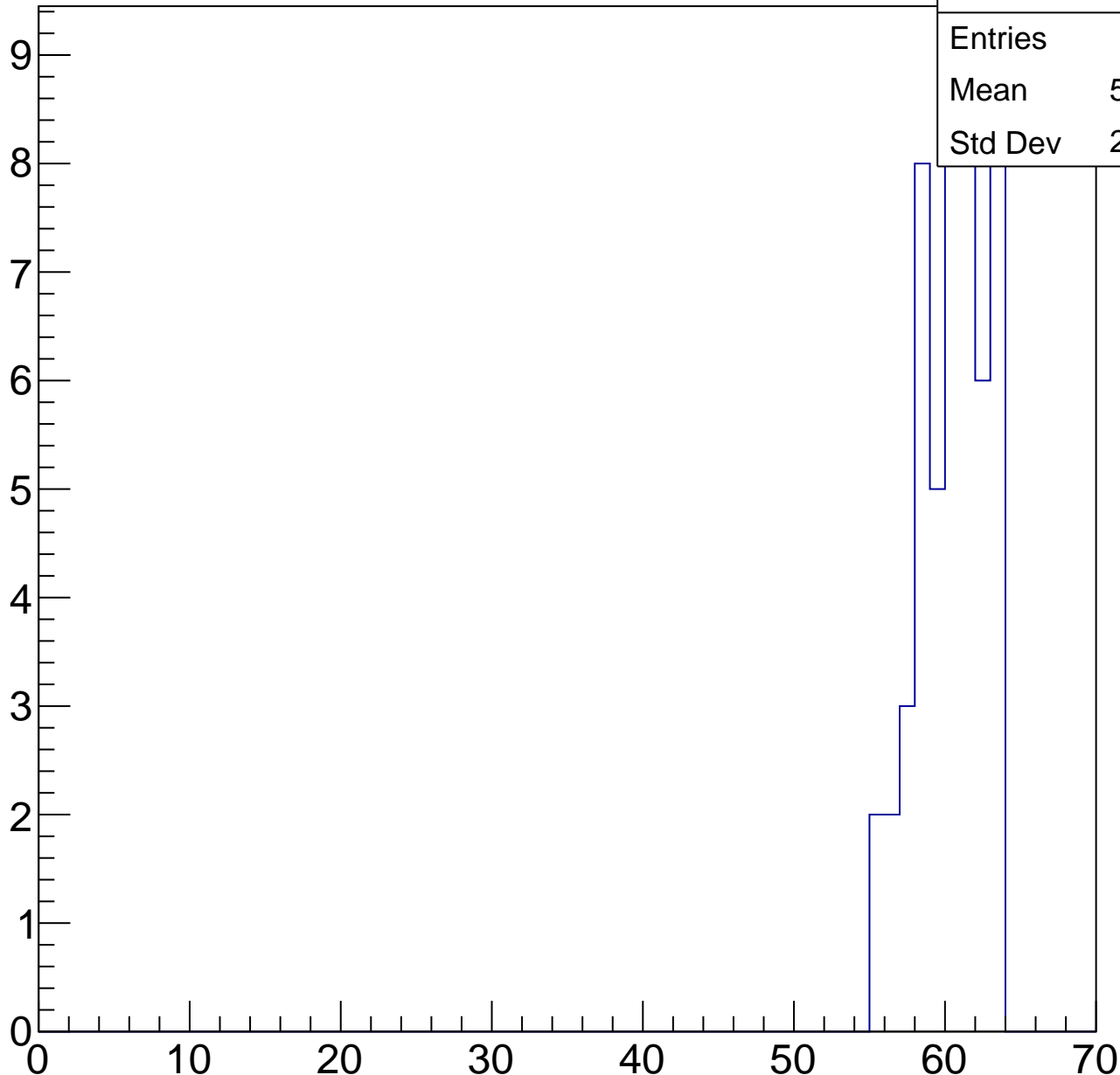
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	51
Mean	59.94
Std Dev	2.218

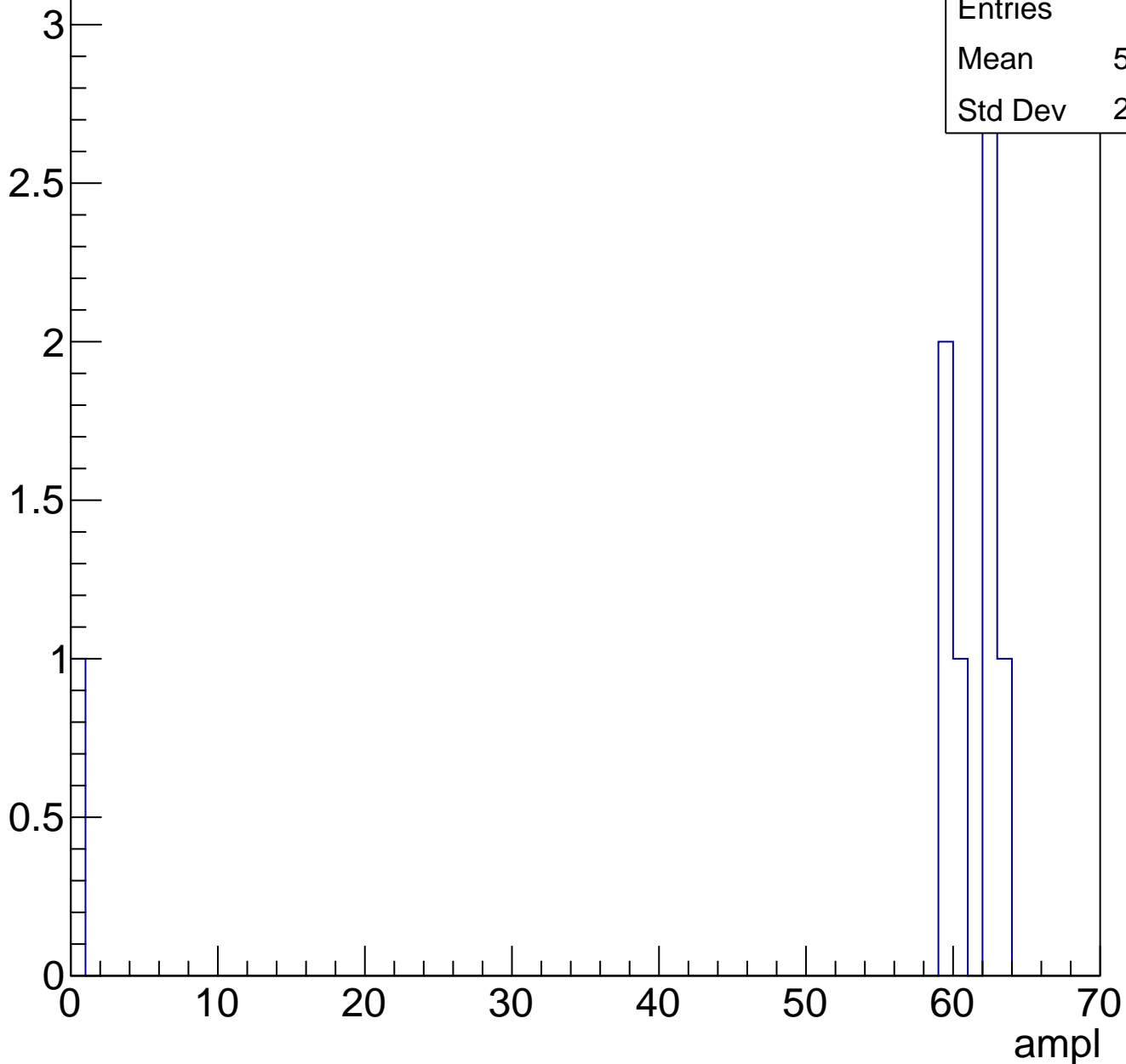
ampl



# B1L103S, U21-ch1, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U21-ch1, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

1

Mean

63

Std Dev

0

# B1L103S, U21-ch2, adc0

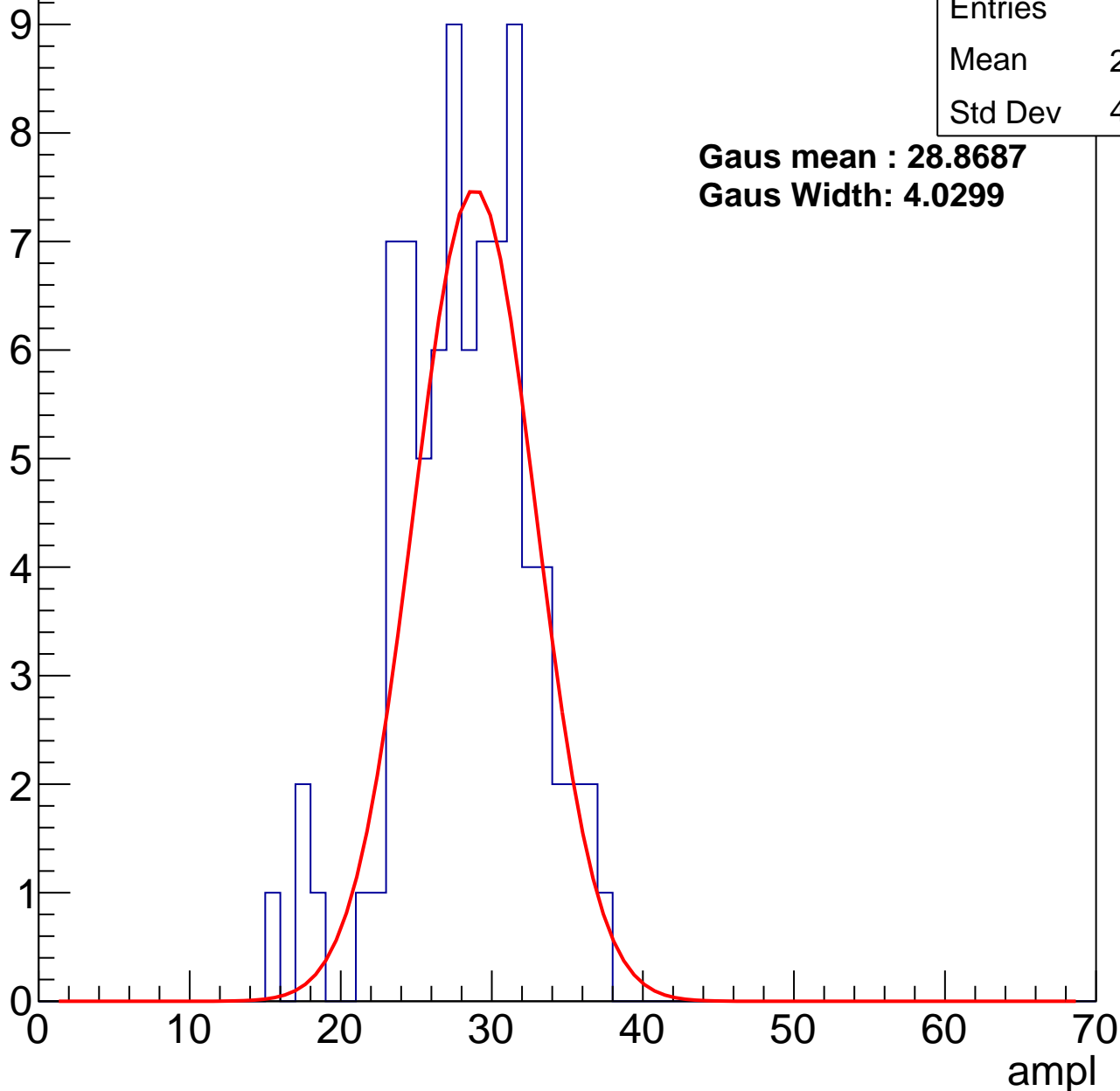
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	84
Mean	27.74
Std Dev	4.384

**Gaus mean : 28.8687**

**Gaus Width: 4.0299**



# B1L103S, U21-ch2, adc1

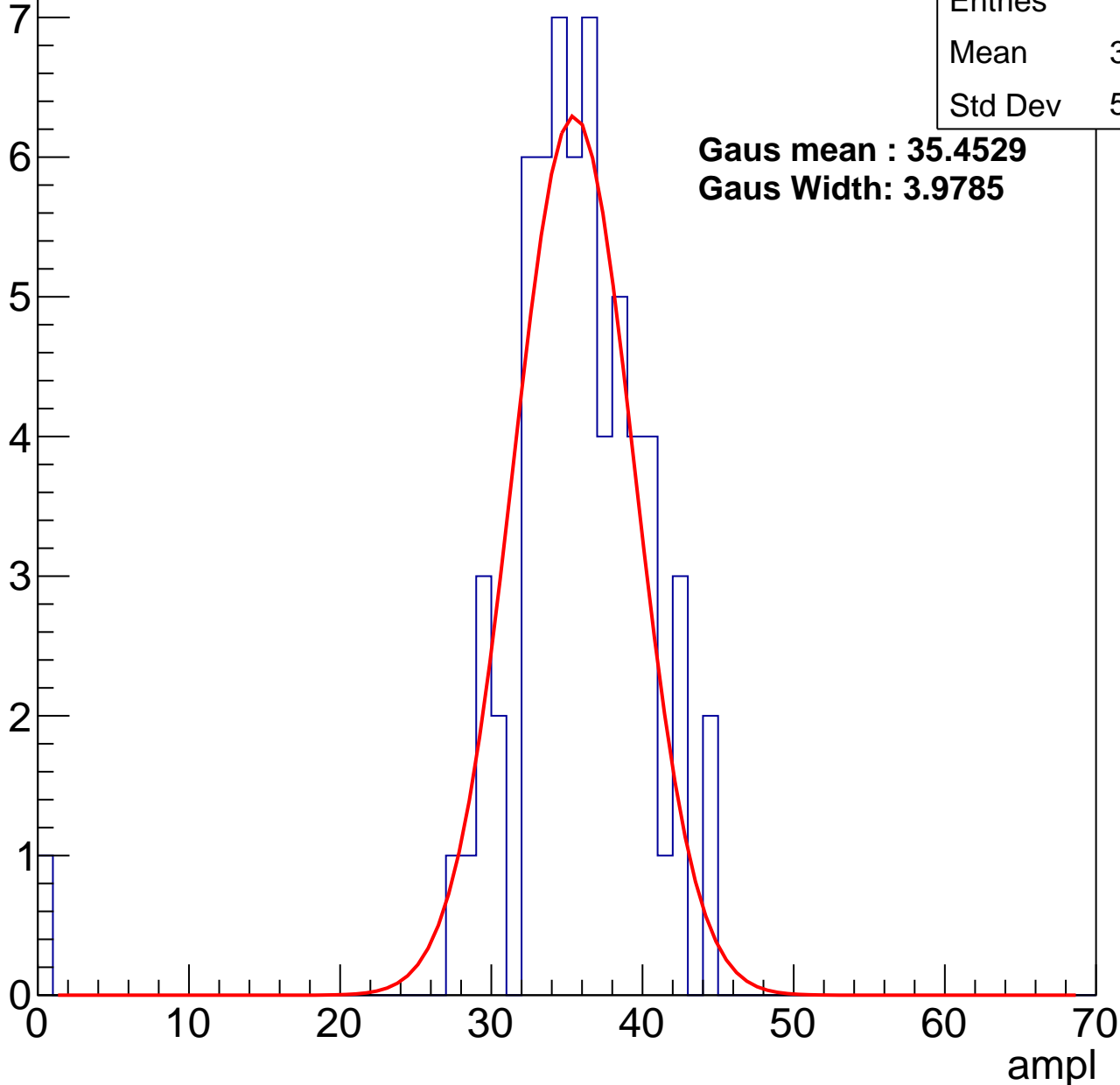
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	34.94
Std Dev	5.852

**Gaus mean : 35.4529**

**Gaus Width: 3.9785**



# B1L103S, U21-ch2, adc2

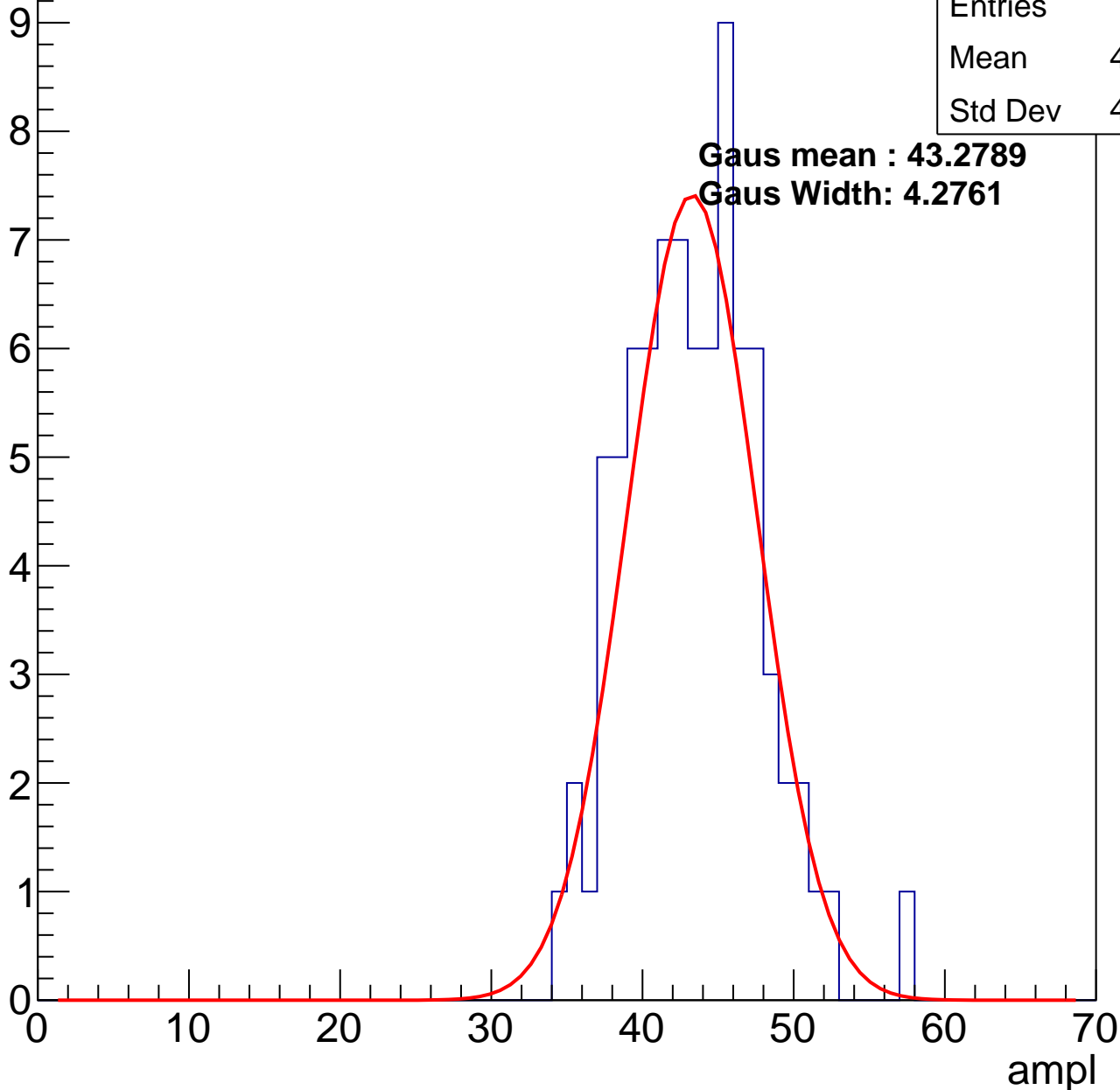
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	83
Mean	42.86
Std Dev	4.285

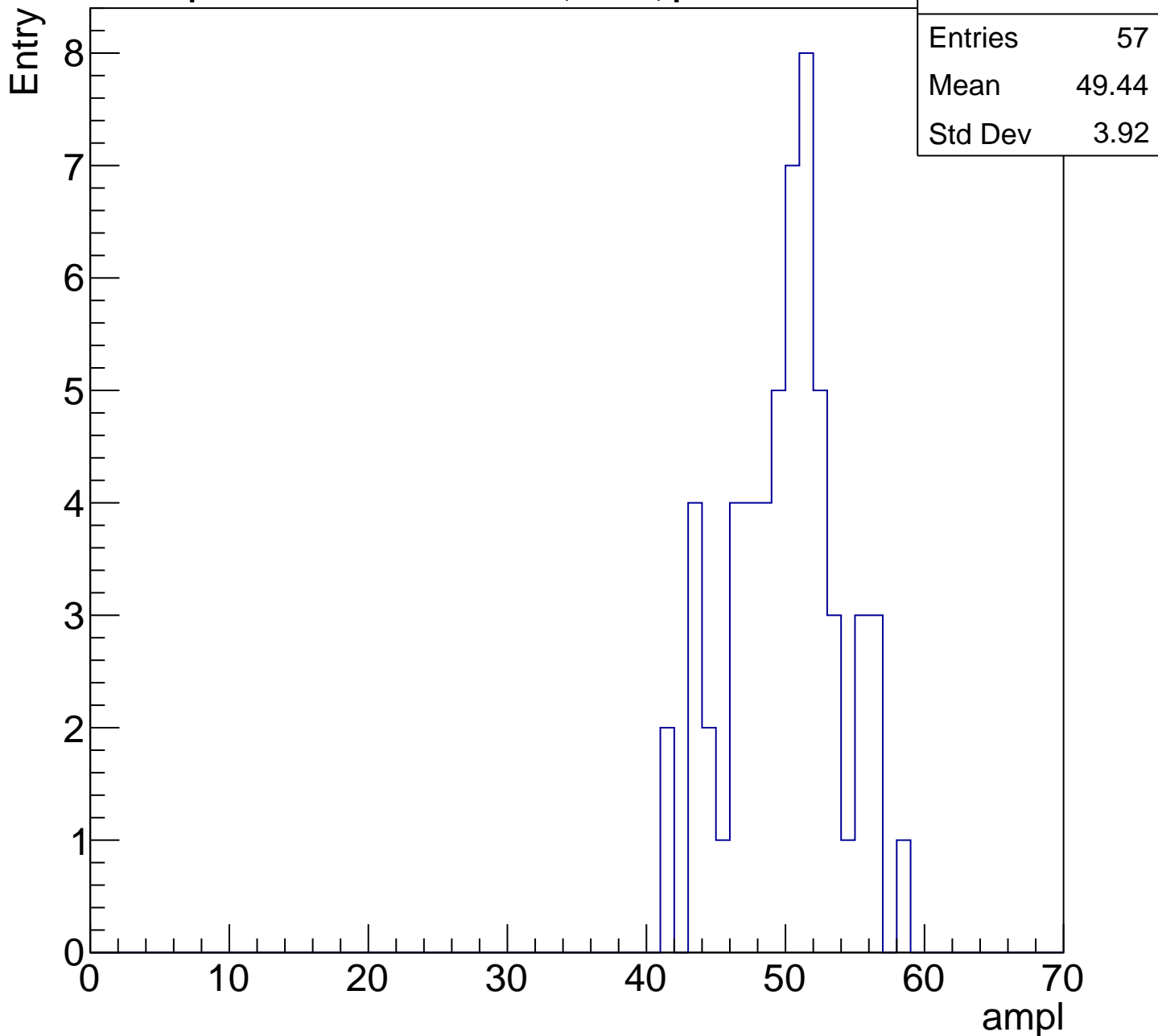
**Gaus mean : 43.2789**

**Gaus Width: 4.2761**



# B1L103S, U21-ch2, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

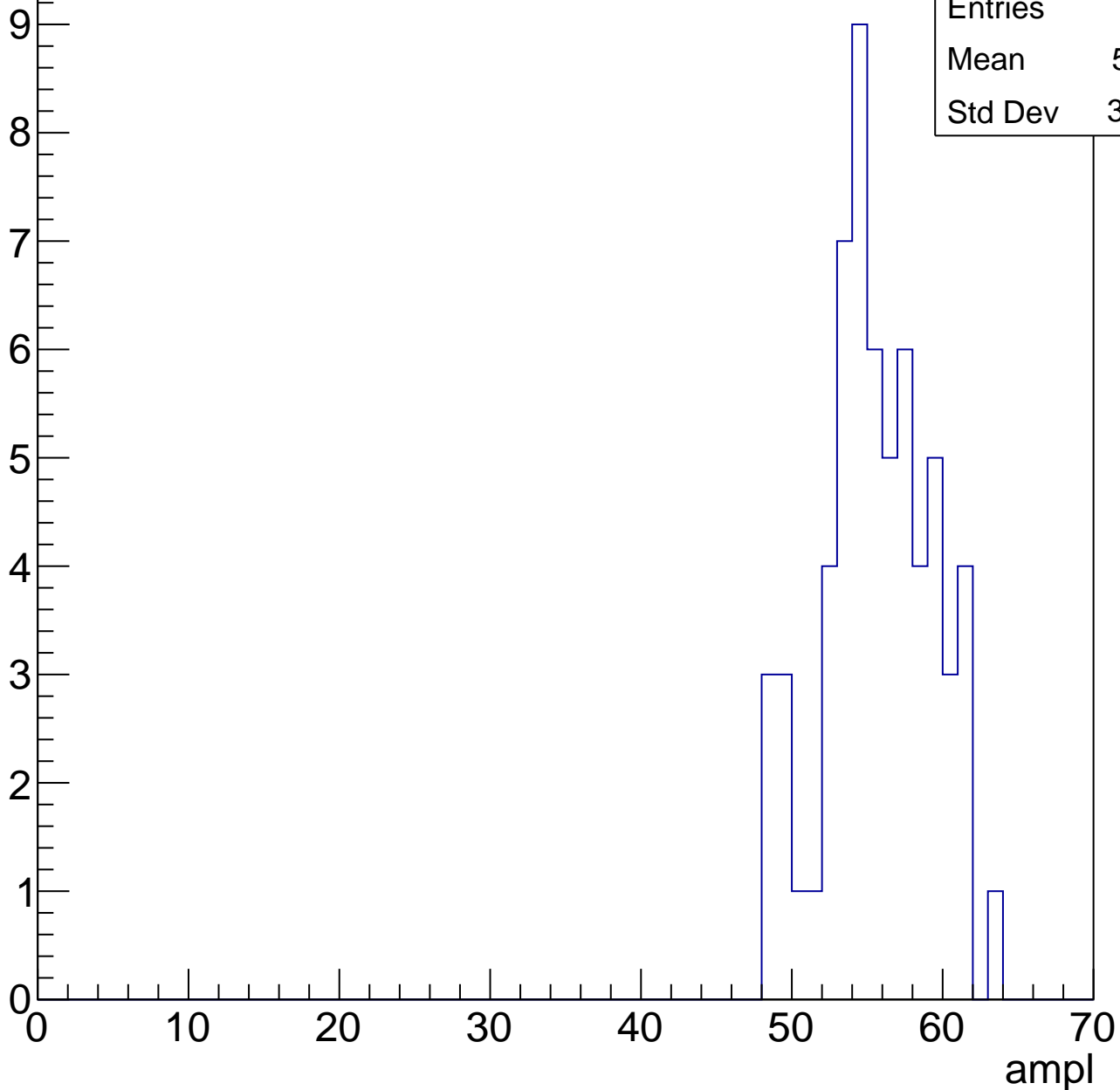


# B1L103S, U21-ch2, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	55.21
Std Dev	3.579

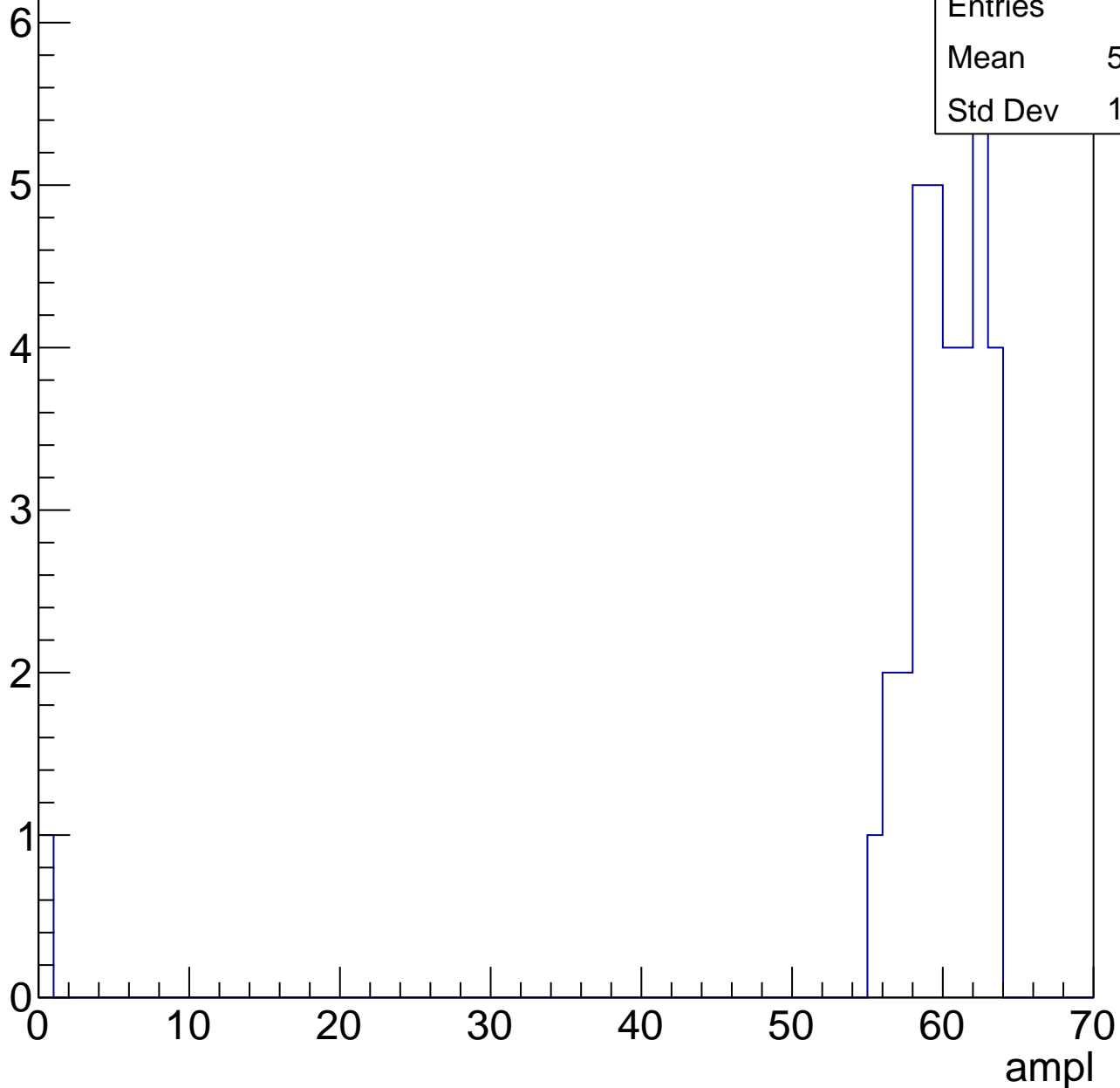


# B1L103S, U21-ch2, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	34
Mean	58.06
Std Dev	10.34

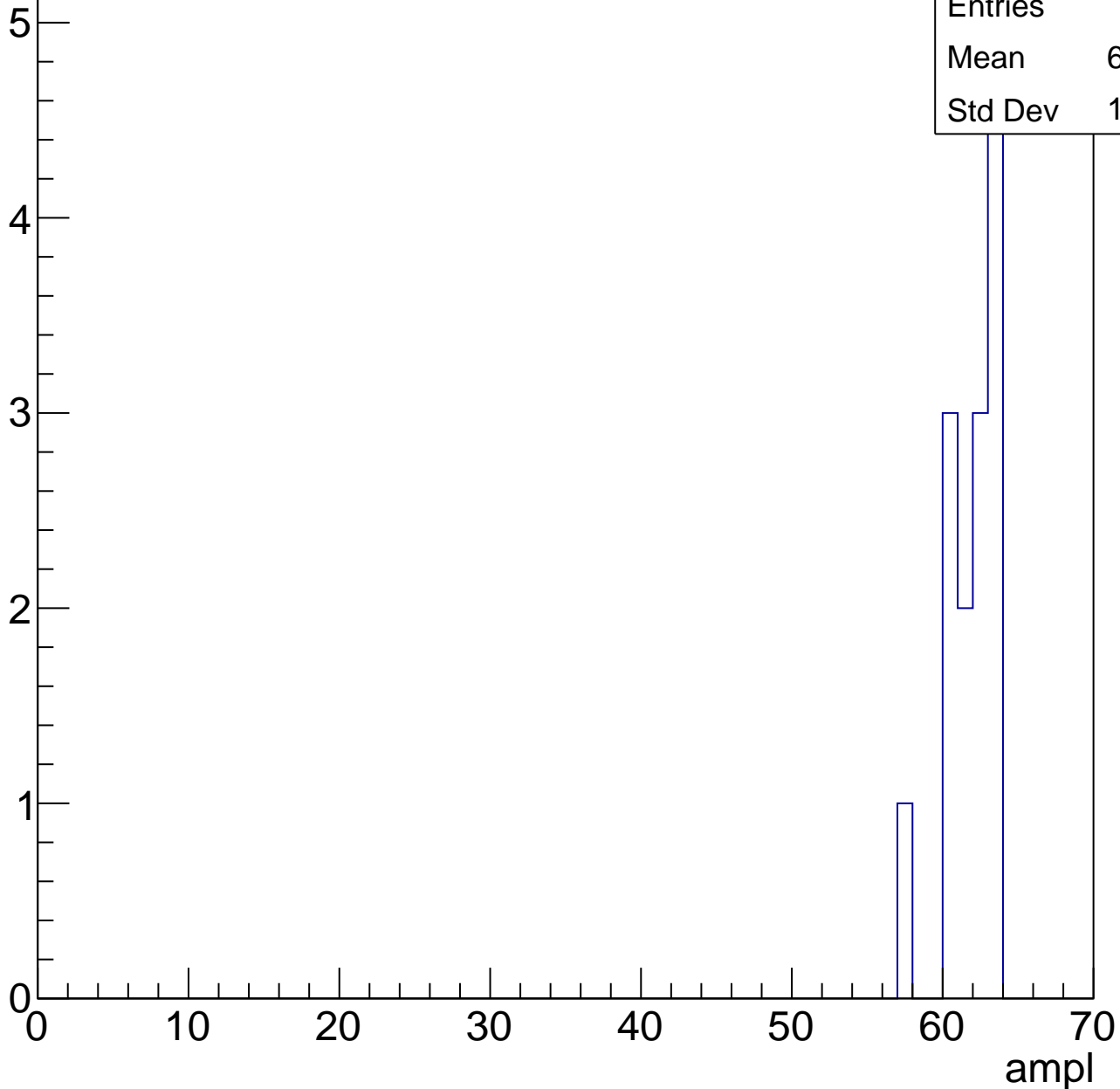


# B1L103S, U21-ch2, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	14
Mean	61.43
Std Dev	1.678

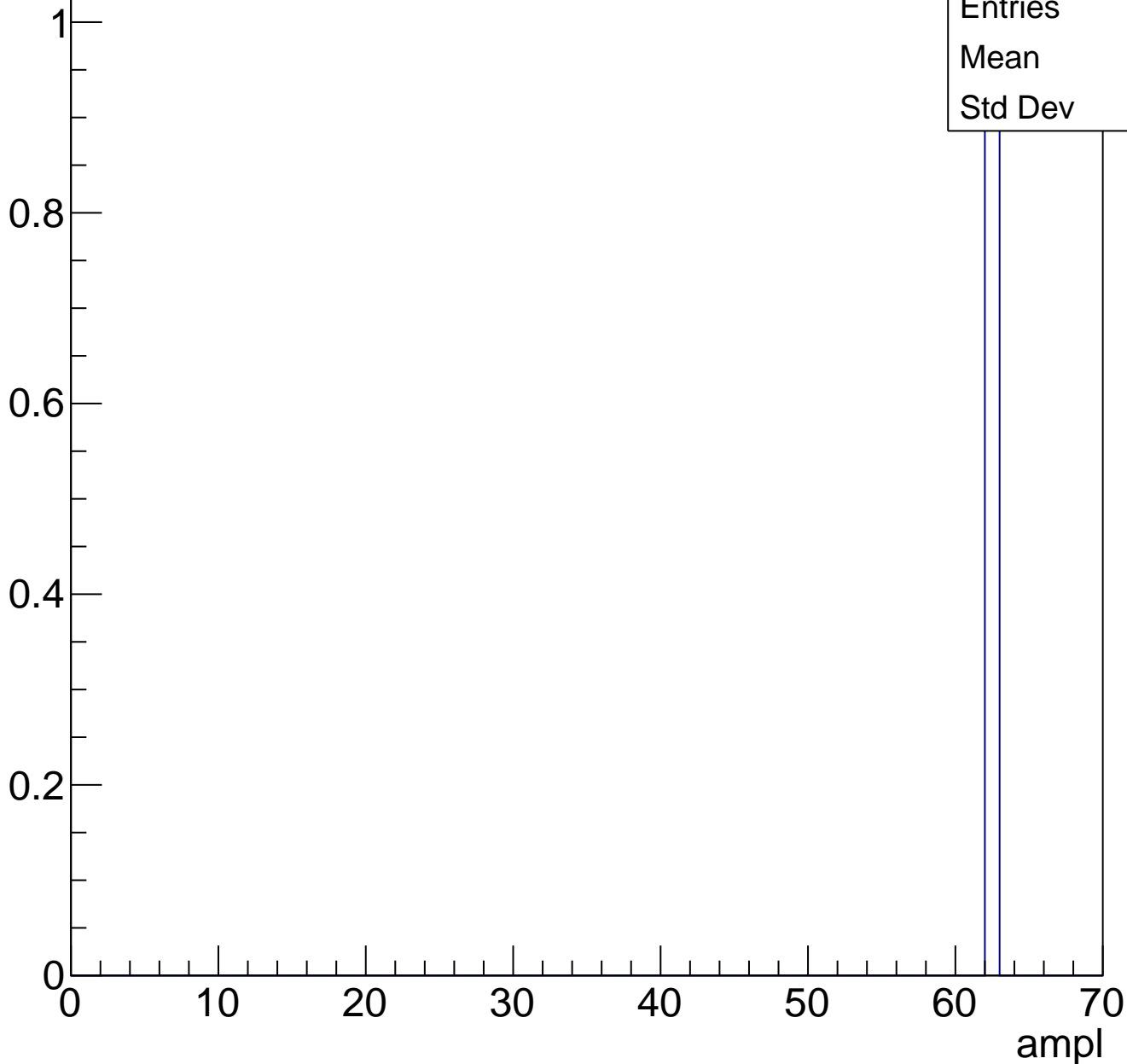




# B1L103S, U21-ch2, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U21-ch3, adc0

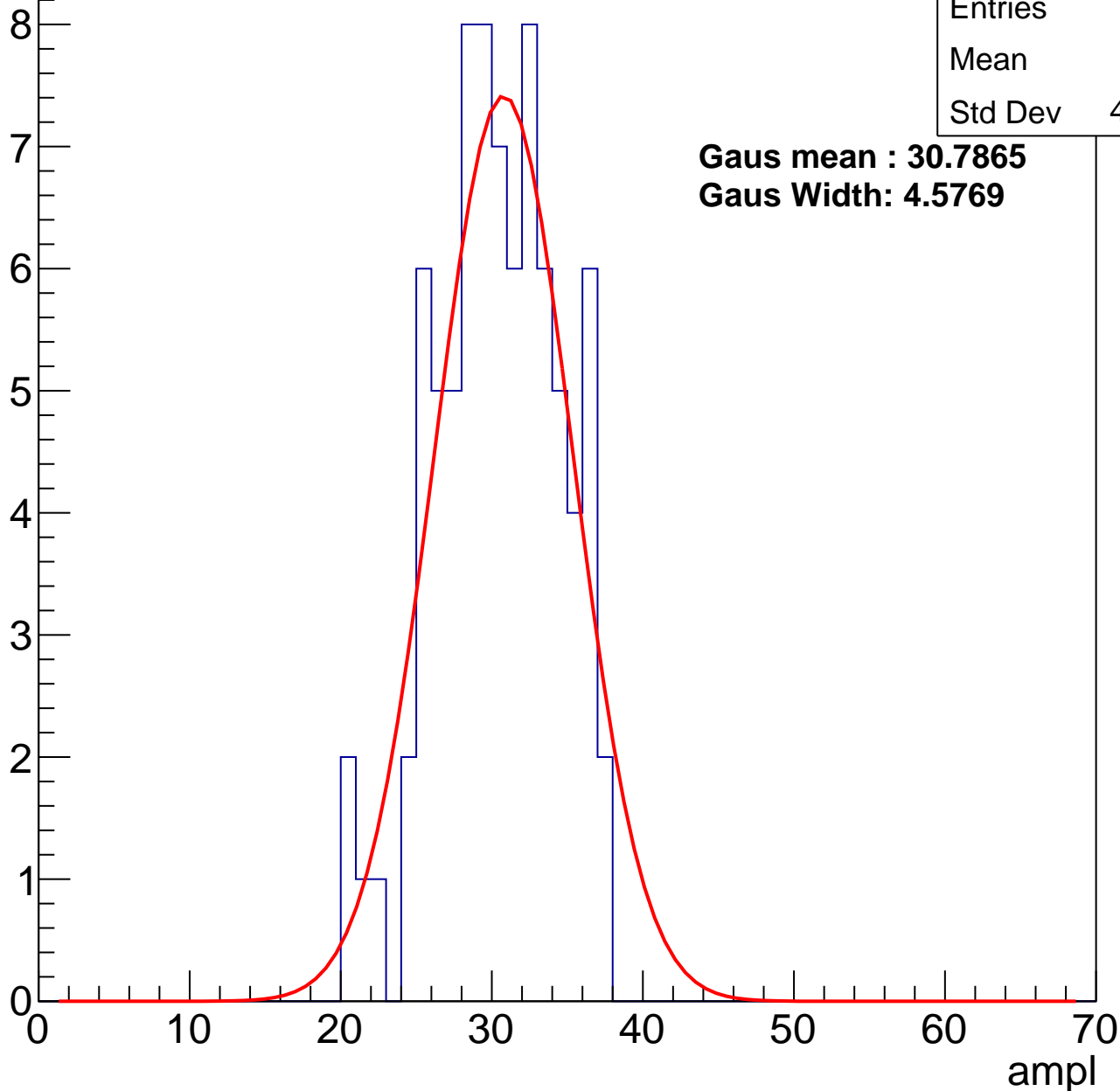
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	82
Mean	29.9
Std Dev	4.008

**Gaus mean : 30.7865**

**Gaus Width: 4.5769**



# B1L103S, U21-ch3, adc1

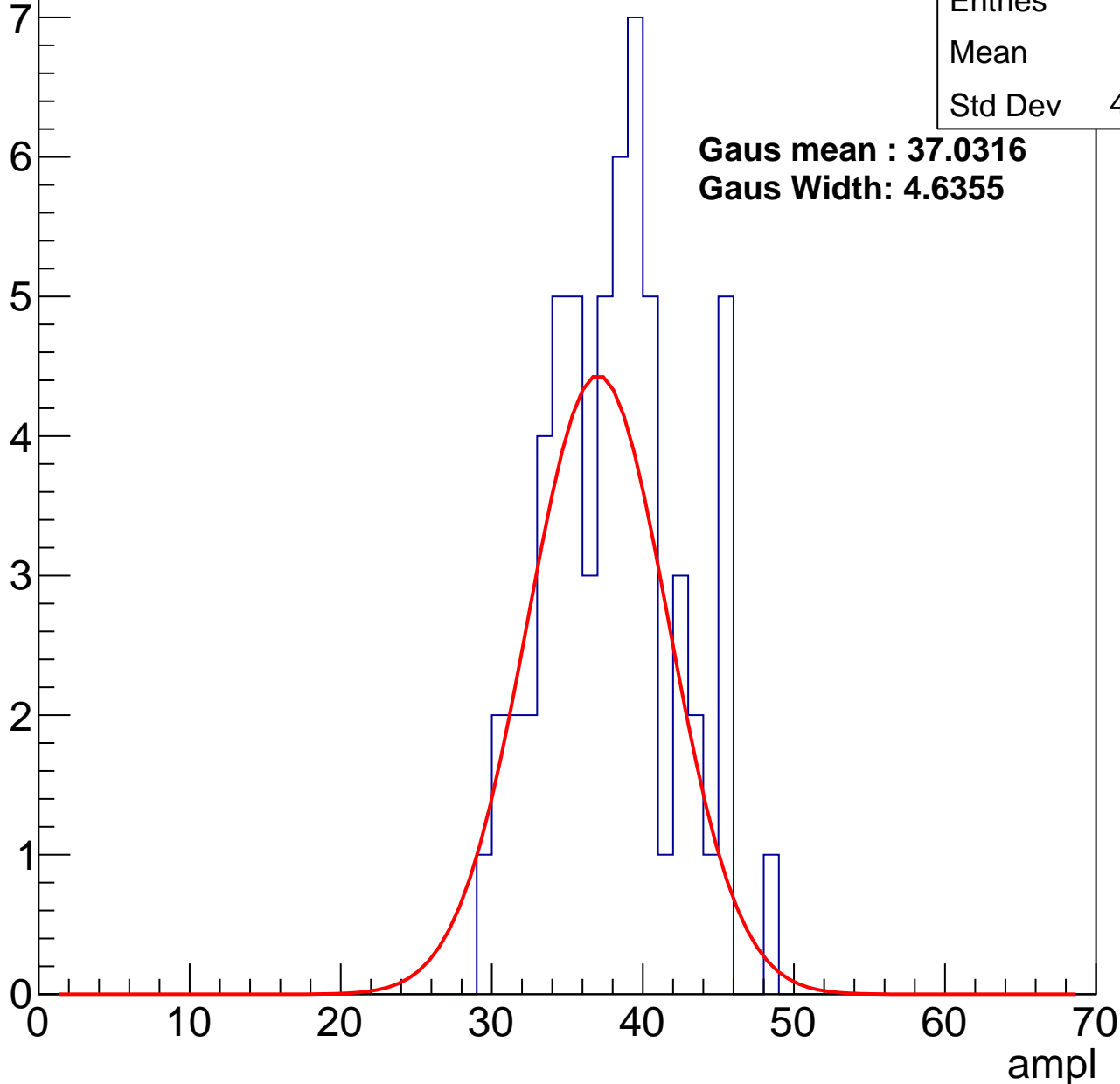
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	37.6
Std Dev	4.333

**Gaus mean : 37.0316**

**Gaus Width: 4.6355**



# B1L103S, U21-ch3, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	85
Mean	43.84
Std Dev	3.937

**Gaus mean : 44.0675**

**Gaus Width: 4.2578**

10

8

6

4

2

0

0

10

20

30

40

50

60

70

ampl

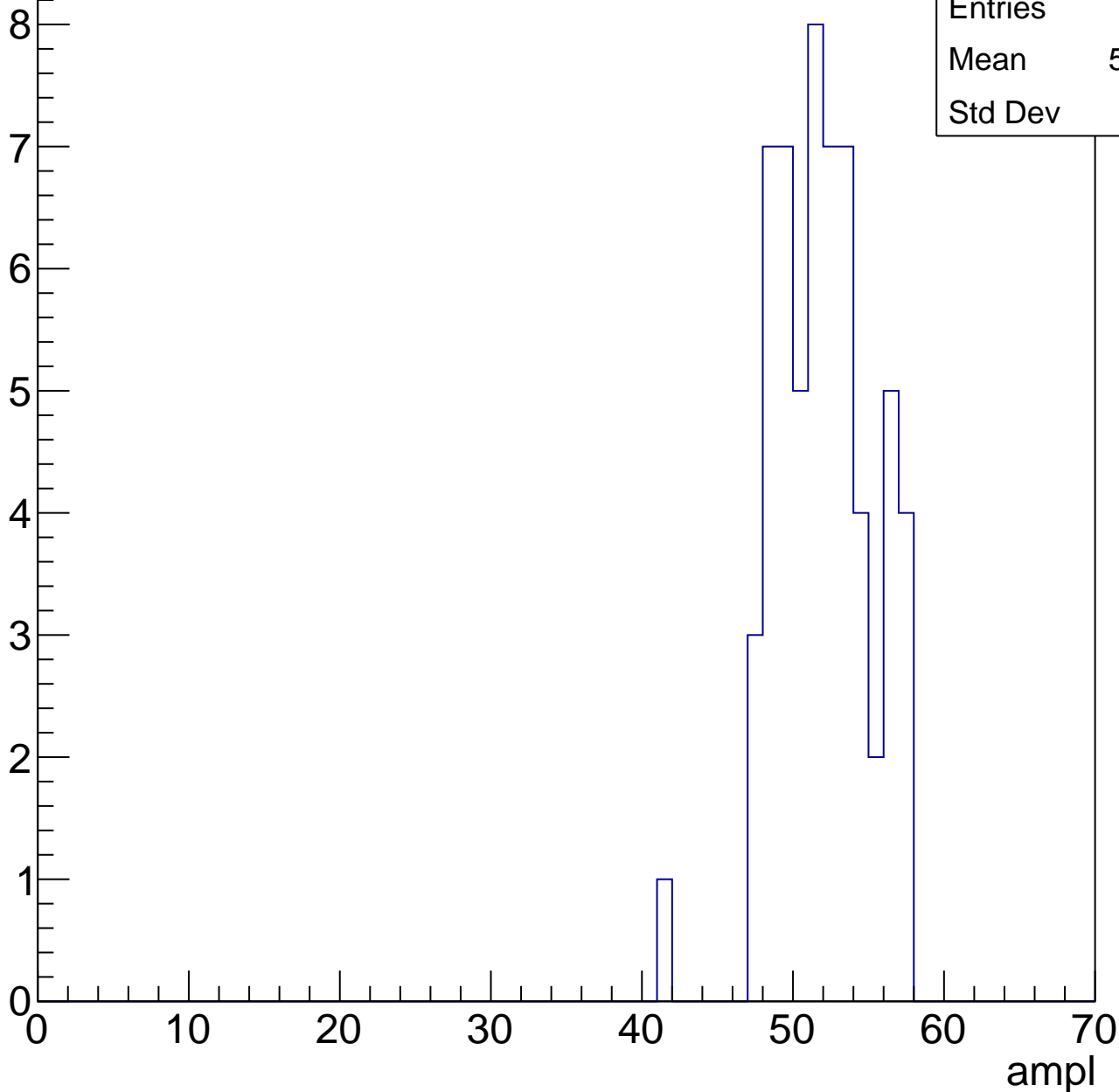


# B1L103S, U21-ch3, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

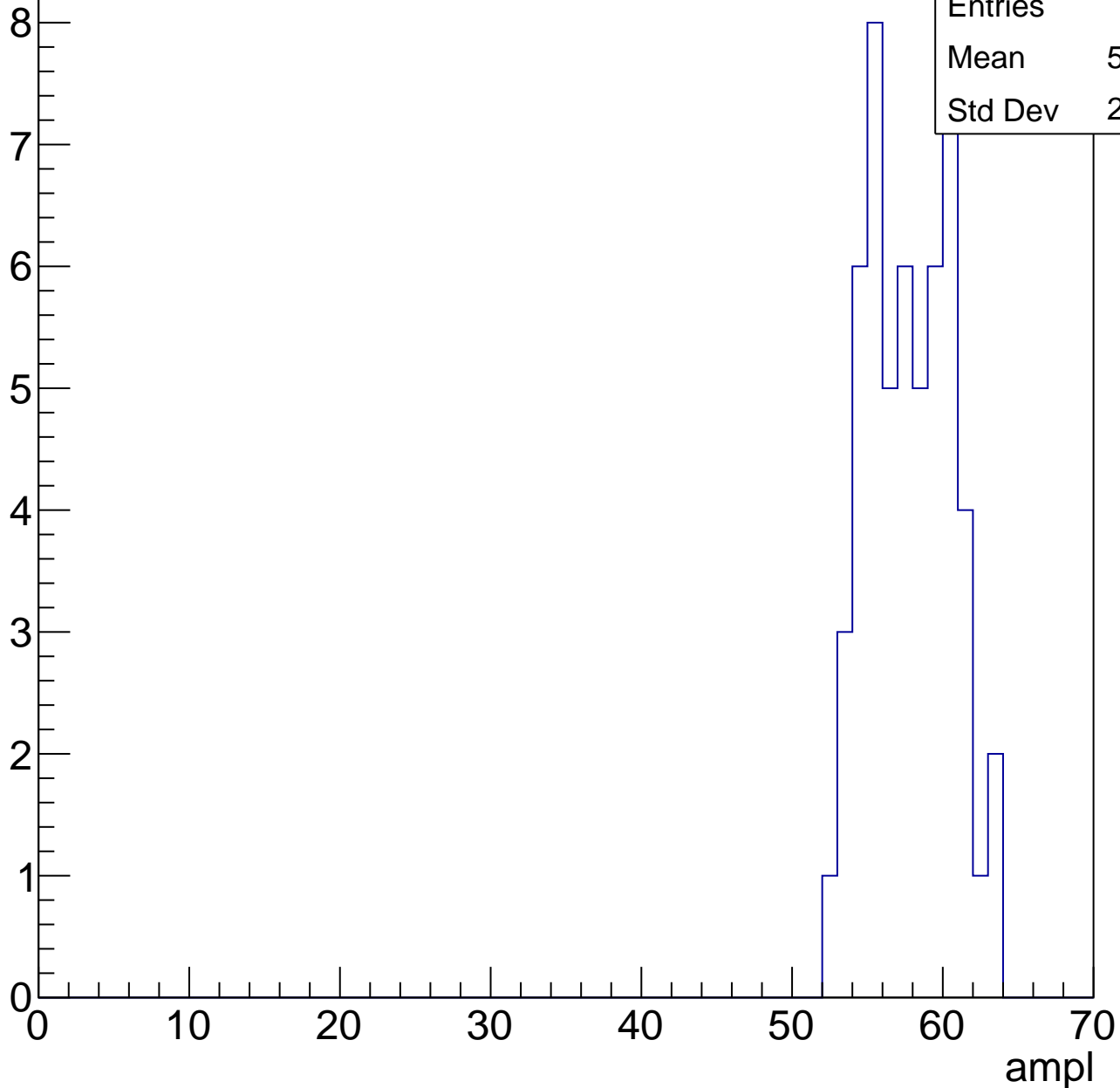
Entries	60
Mean	51.47
Std Dev	3.17



# B1L103S, U21-ch3, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



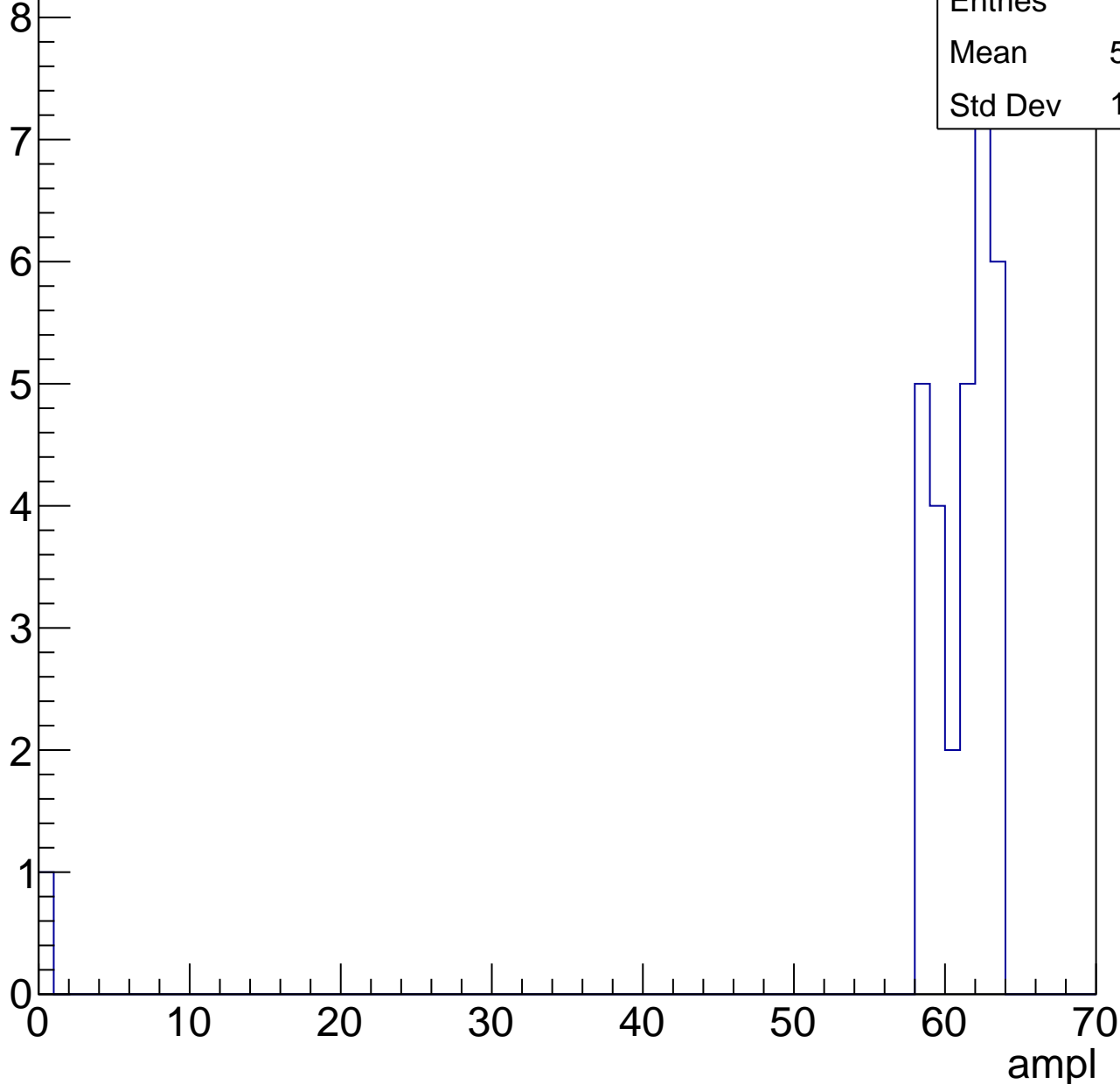
Entries	55
Mean	57.33
Std Dev	2.764

# B1L103S, U21-ch3, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	31
Mean	58.87
Std Dev	10.89



# B1L103S, U21-ch3, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U21-ch3, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U21-ch4, adc0

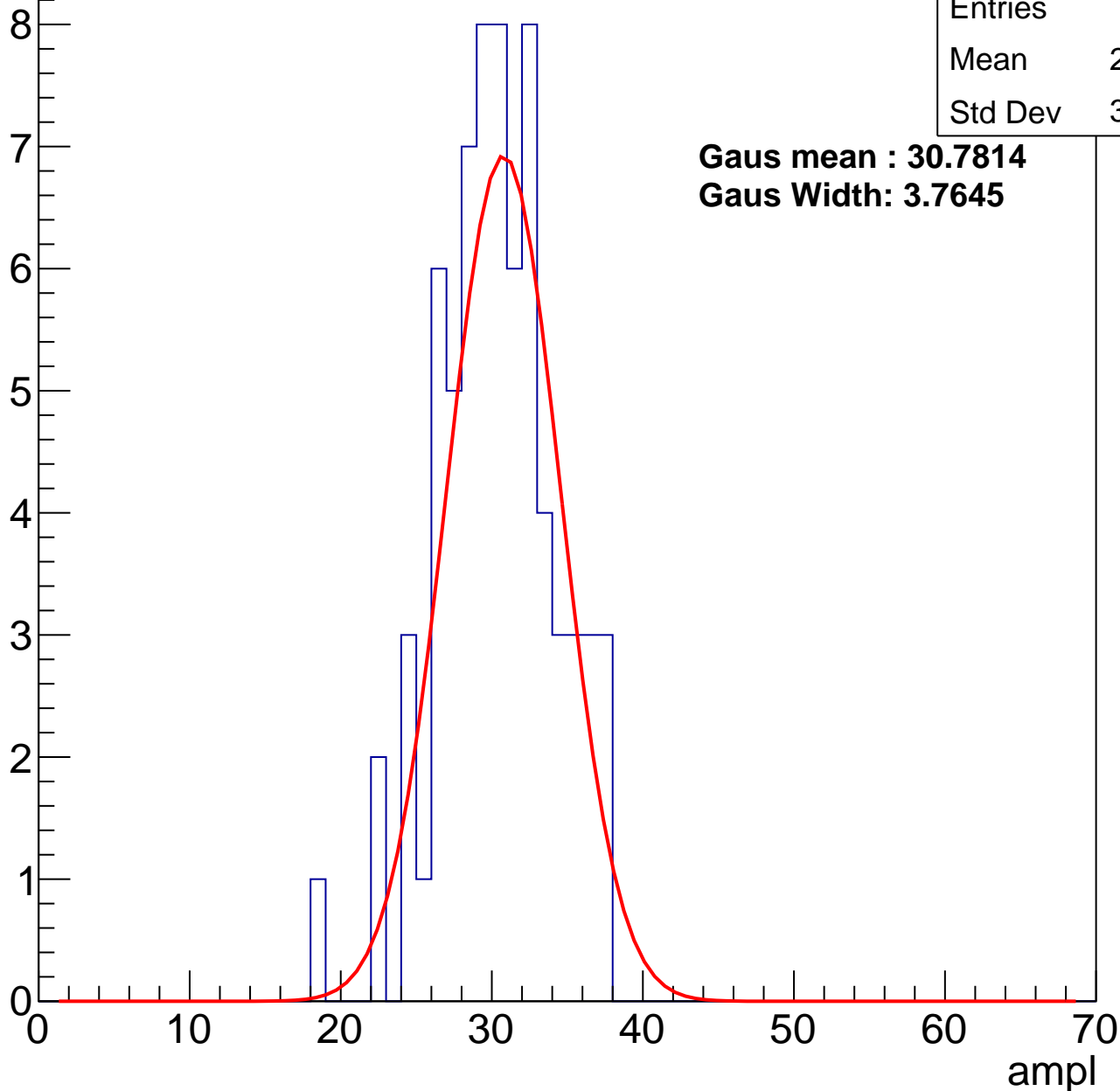
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	29.83
Std Dev	3.812

**Gaus mean : 30.7814**

**Gaus Width: 3.7645**



# B1L103S, U21-ch4, adc1

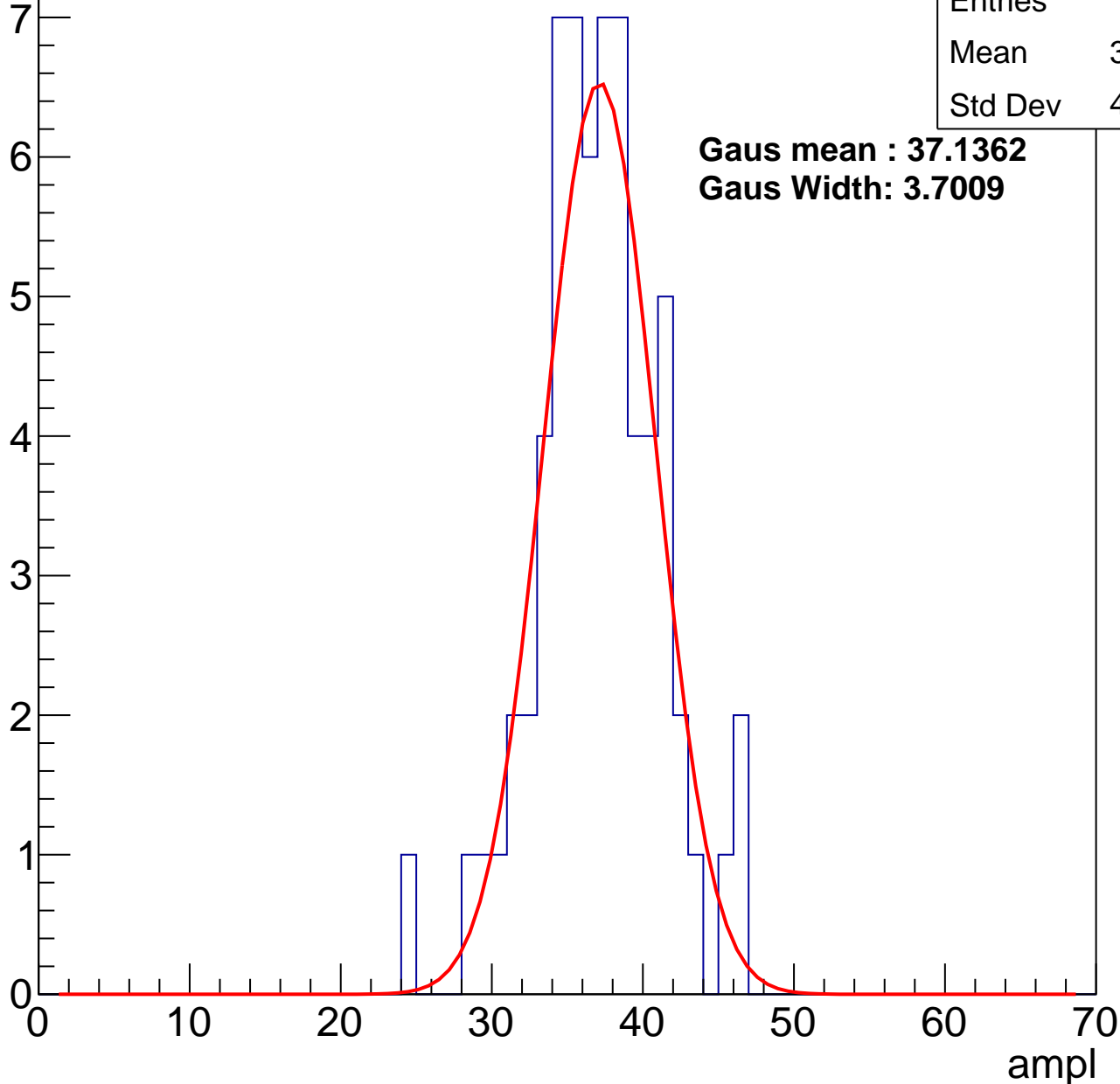
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	36.58
Std Dev	4.087

**Gaus mean : 37.1362**

**Gaus Width: 3.7009**



# B1L103S, U21-ch4, adc2

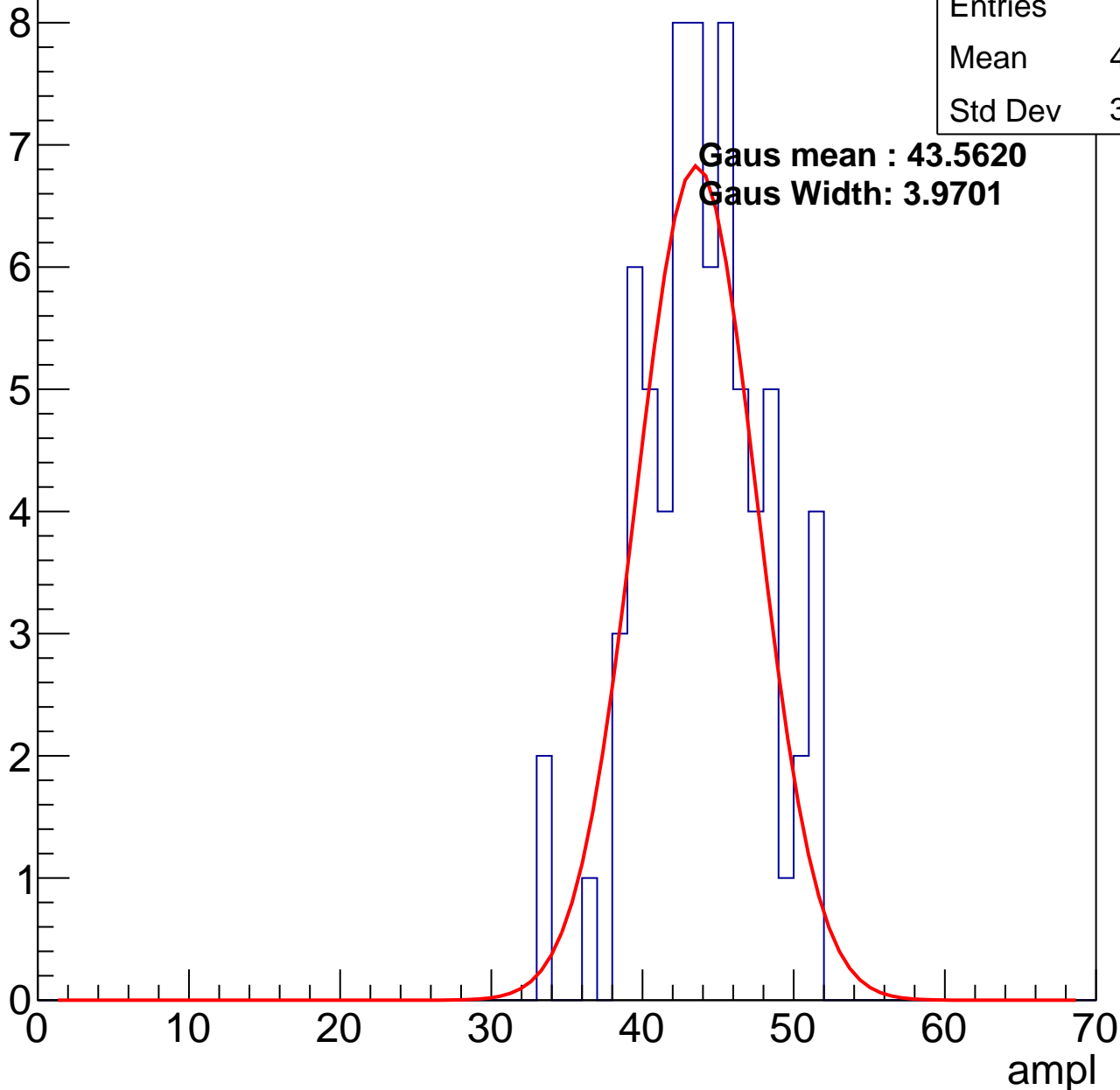
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	43.46
Std Dev	3.972

**Gaus mean : 43.5620**

**Gaus Width: 3.9701**

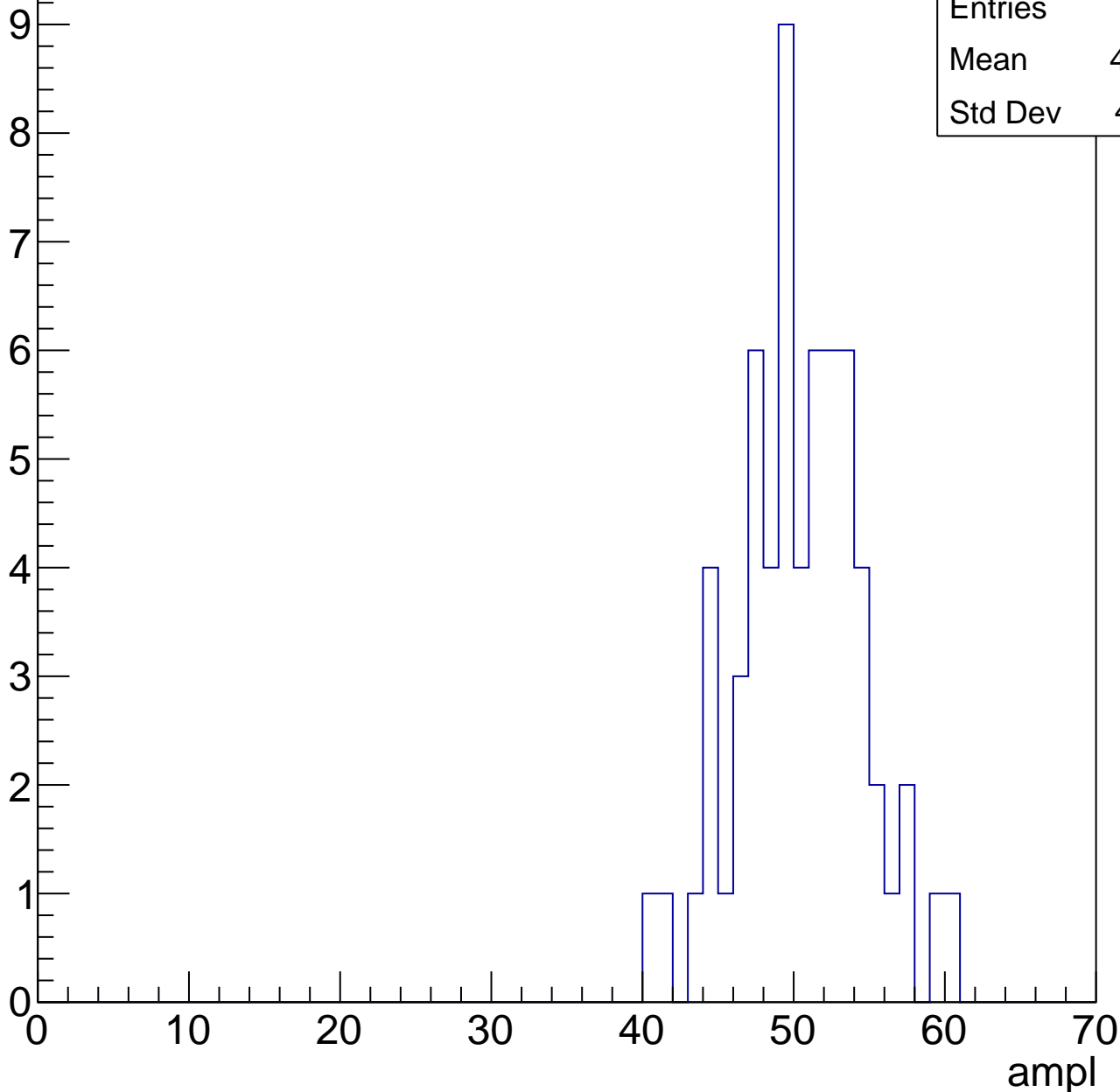


# B1L103S, U21-ch4, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	49.98
Std Dev	4.061

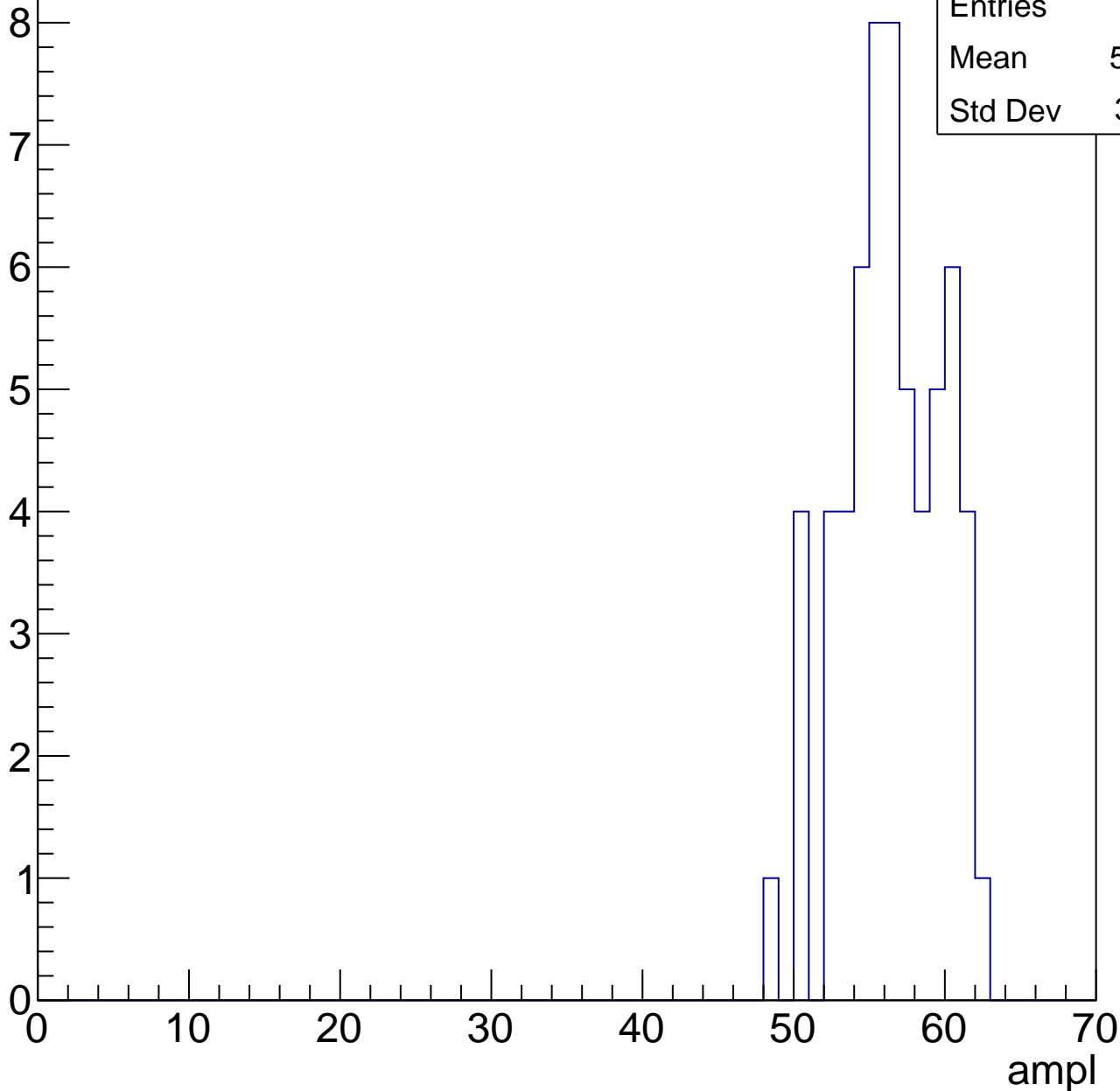


# B1L103S, U21-ch4, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	55.97
Std Dev	3.261

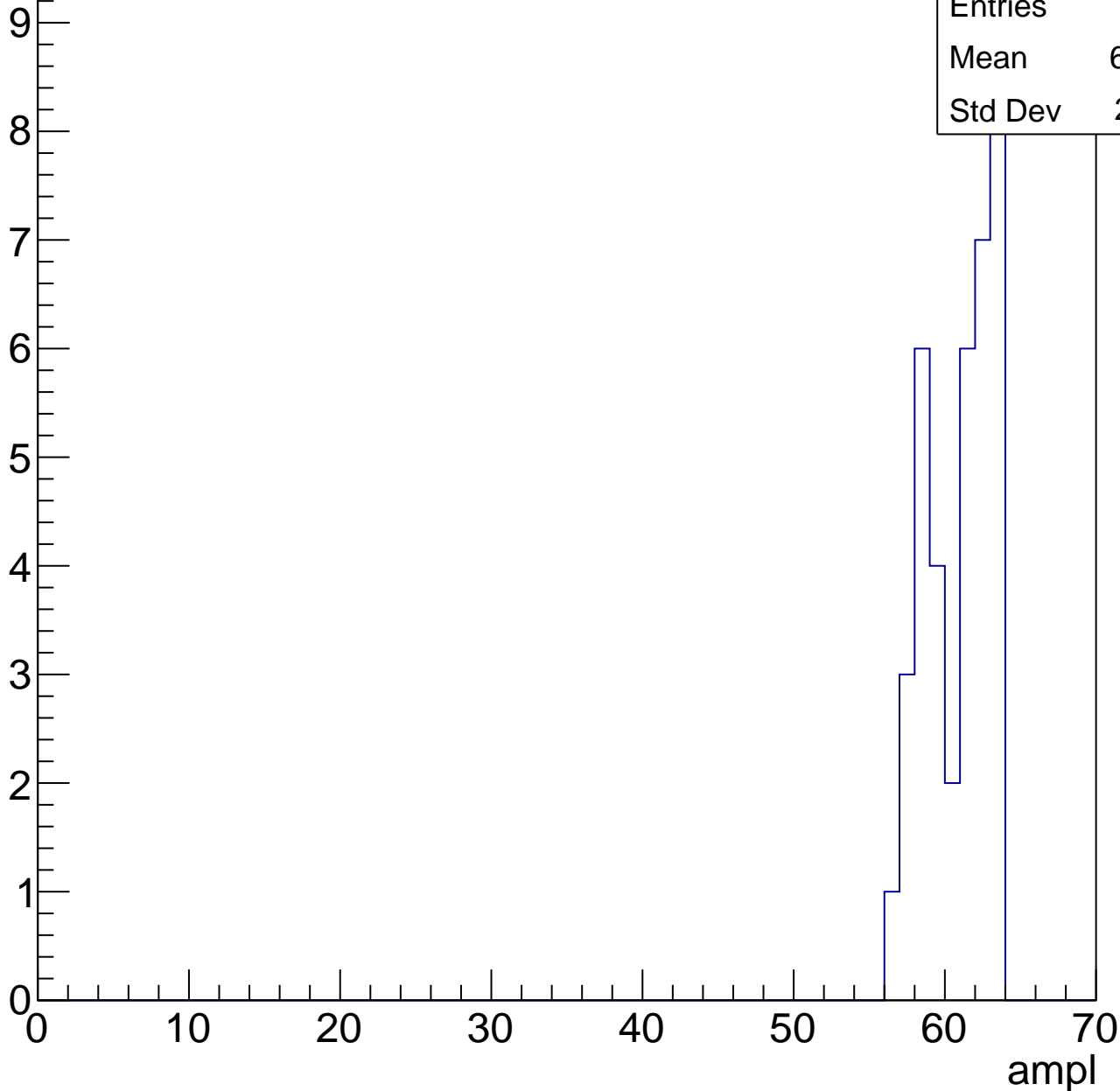


# B1L103S, U21-ch4, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

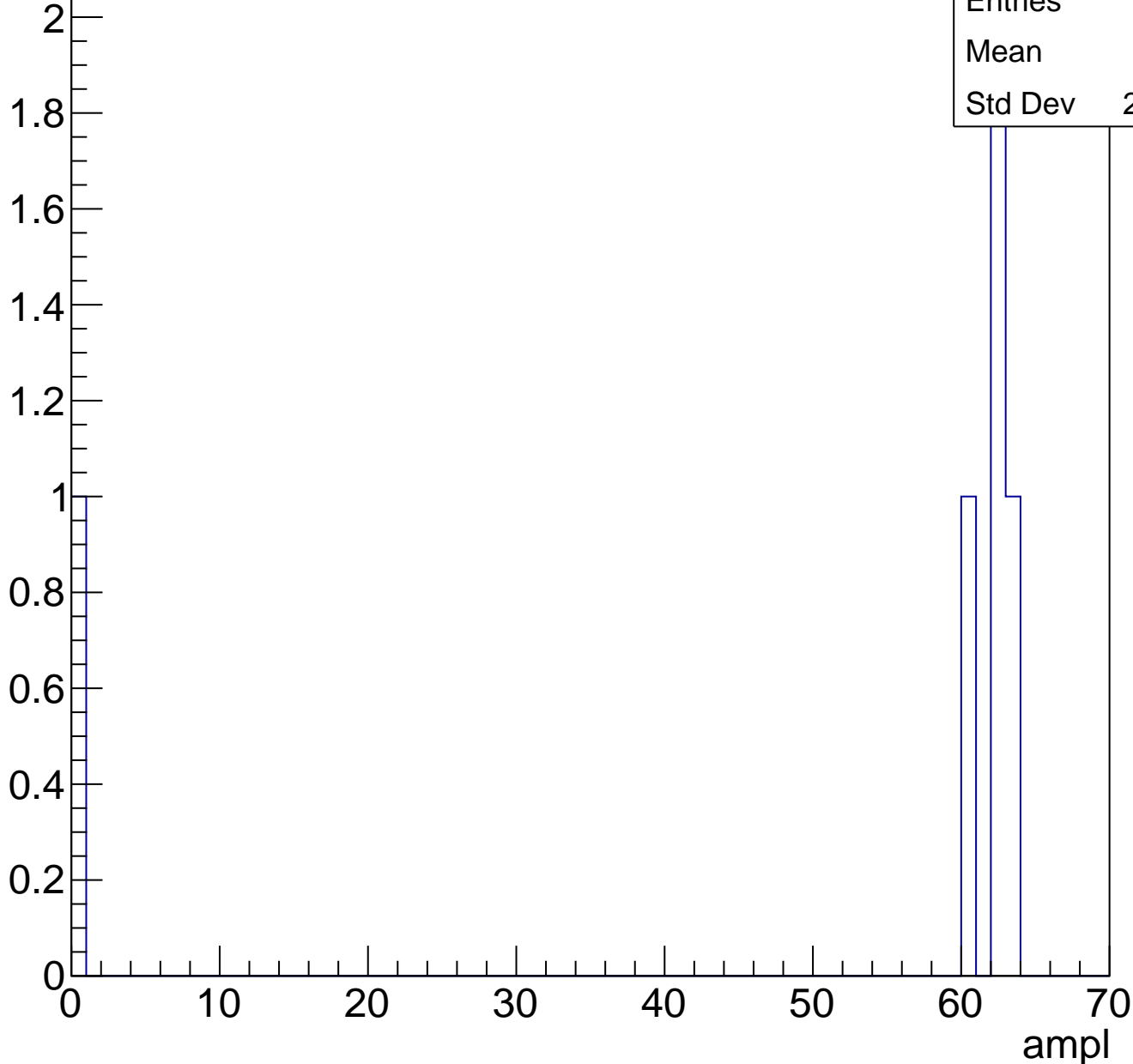
Entries	38
Mean	60.47
Std Dev	2.161



# B1L103S, U21-ch4, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U21-ch4, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U21-ch5, adc0

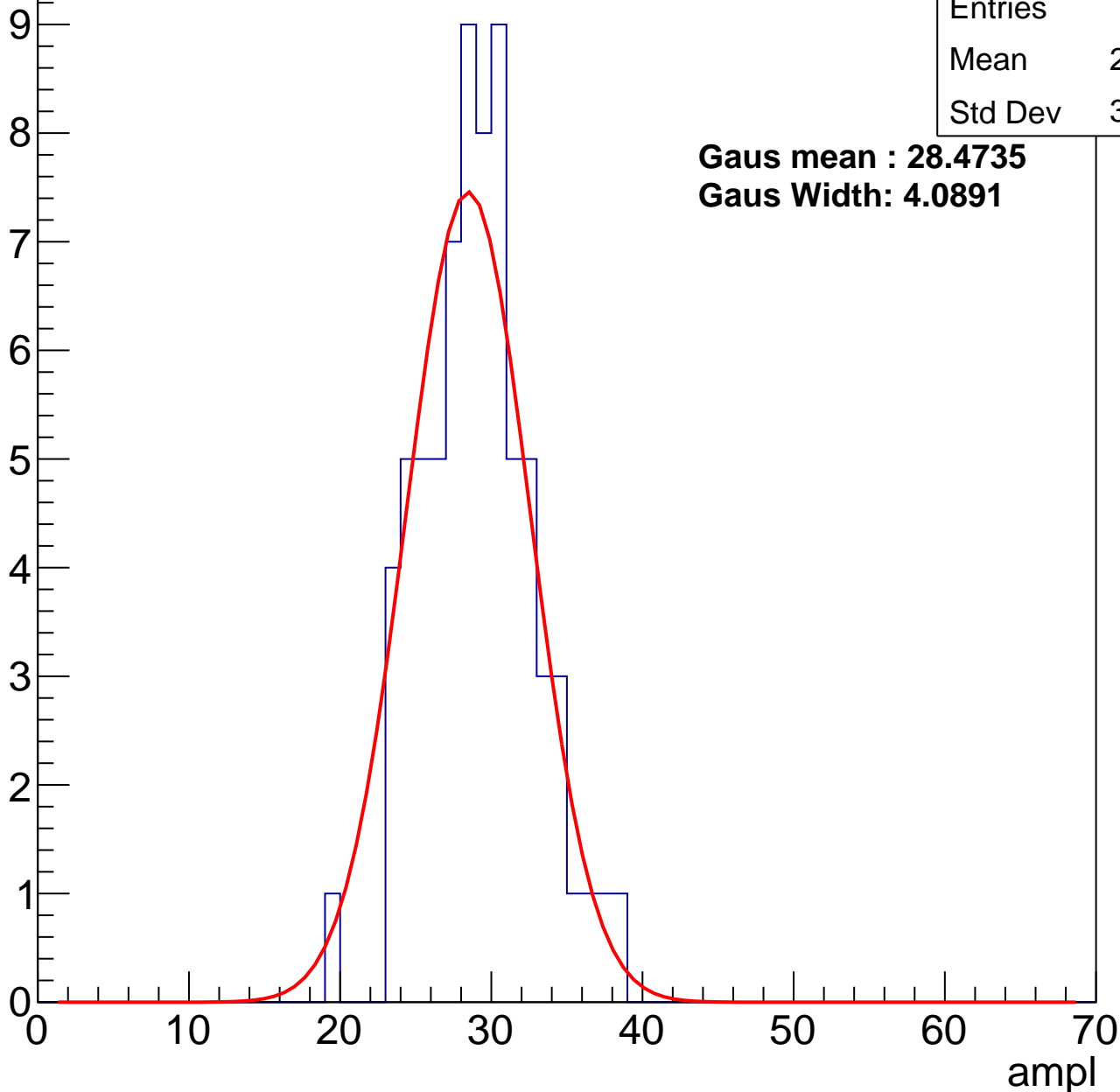
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	28.64
Std Dev	3.605

**Gaus mean : 28.4735**

**Gaus Width: 4.0891**



# B1L103S, U21-ch5, adc1

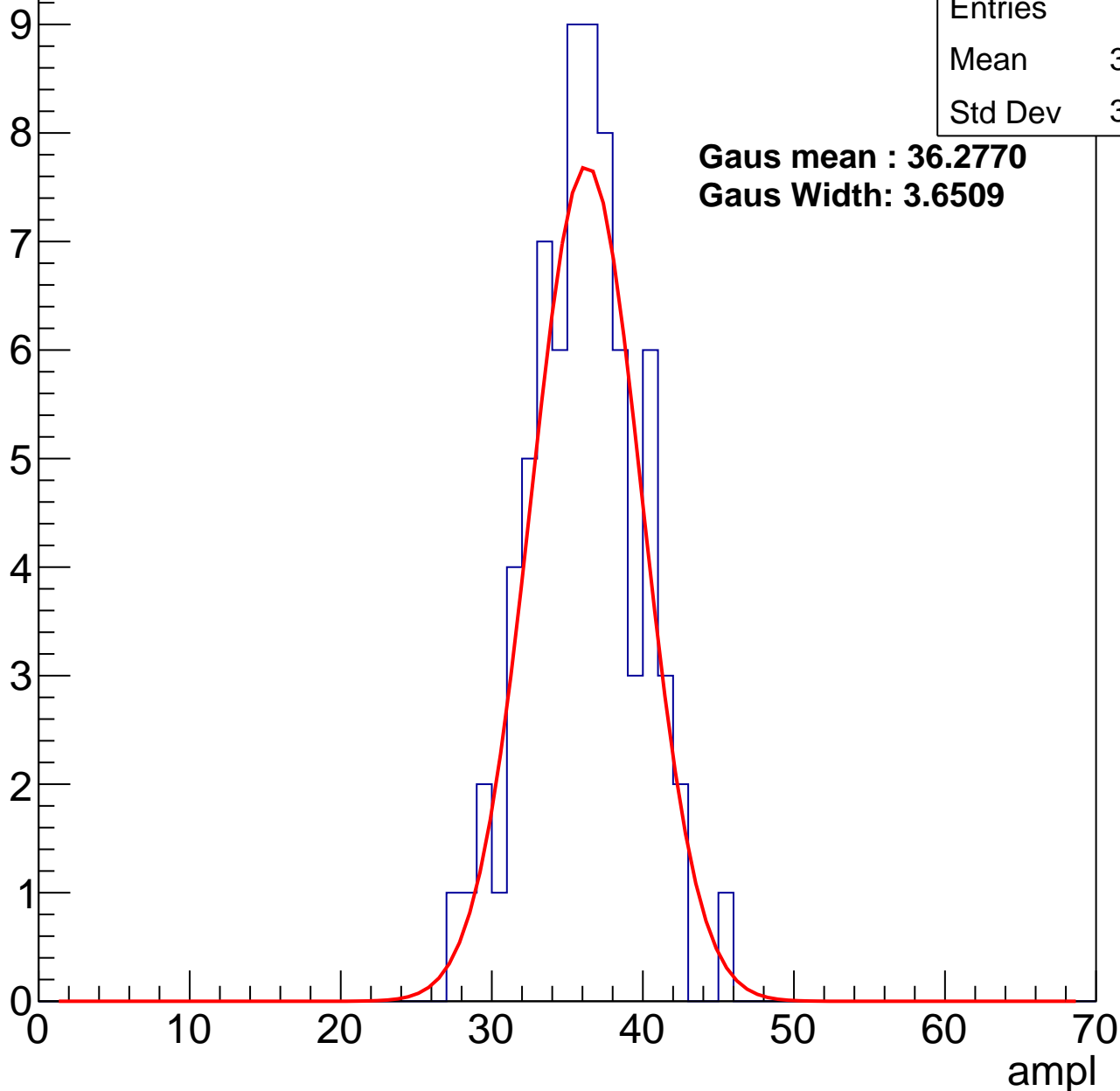
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	35.59
Std Dev	3.537

**Gaus mean : 36.2770**

**Gaus Width: 3.6509**



# B1L103S, U21-ch5, adc2

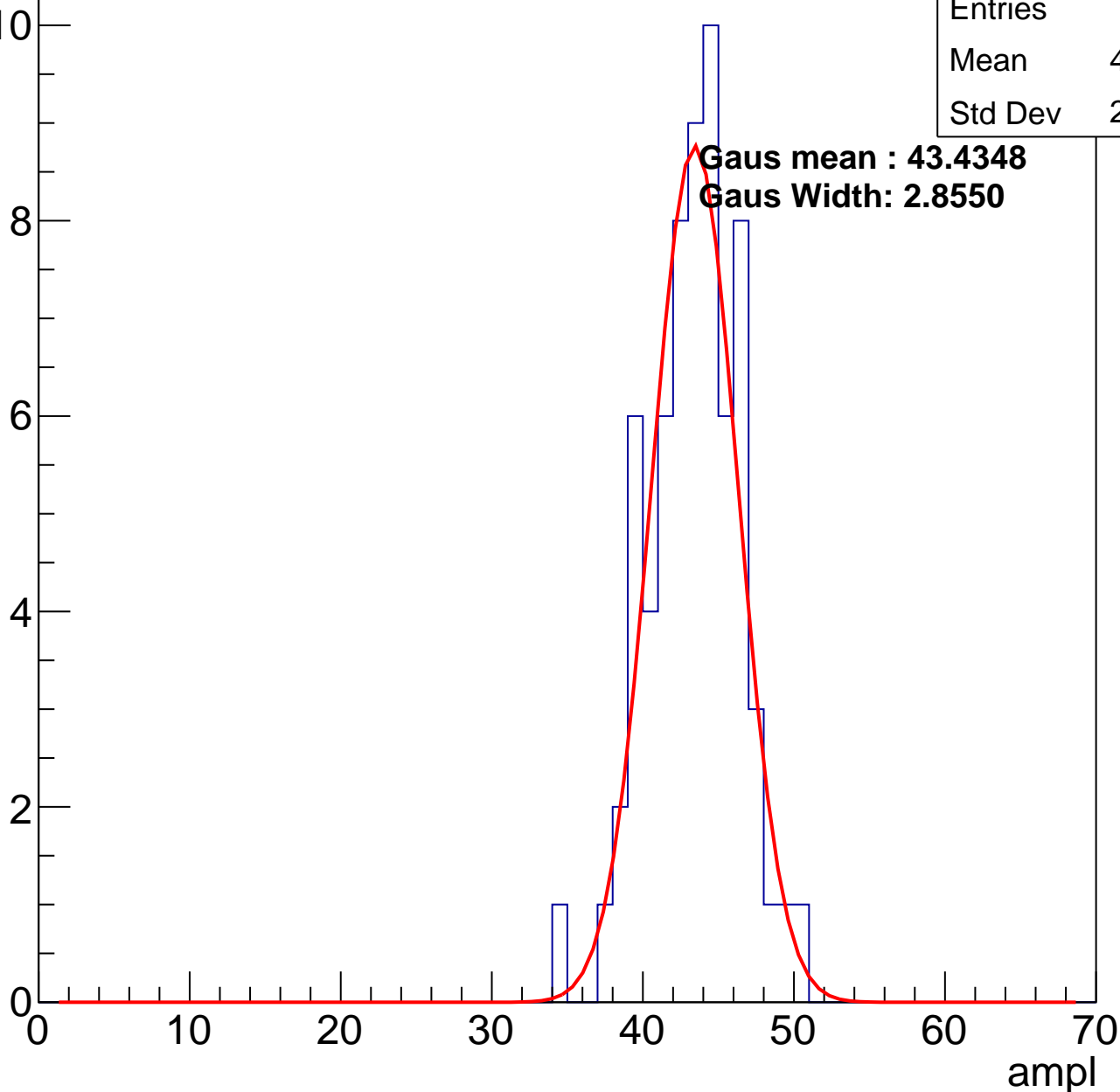
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	42.93
Std Dev	2.979

**Gaus mean : 43.4348**

**Gaus Width: 2.8550**

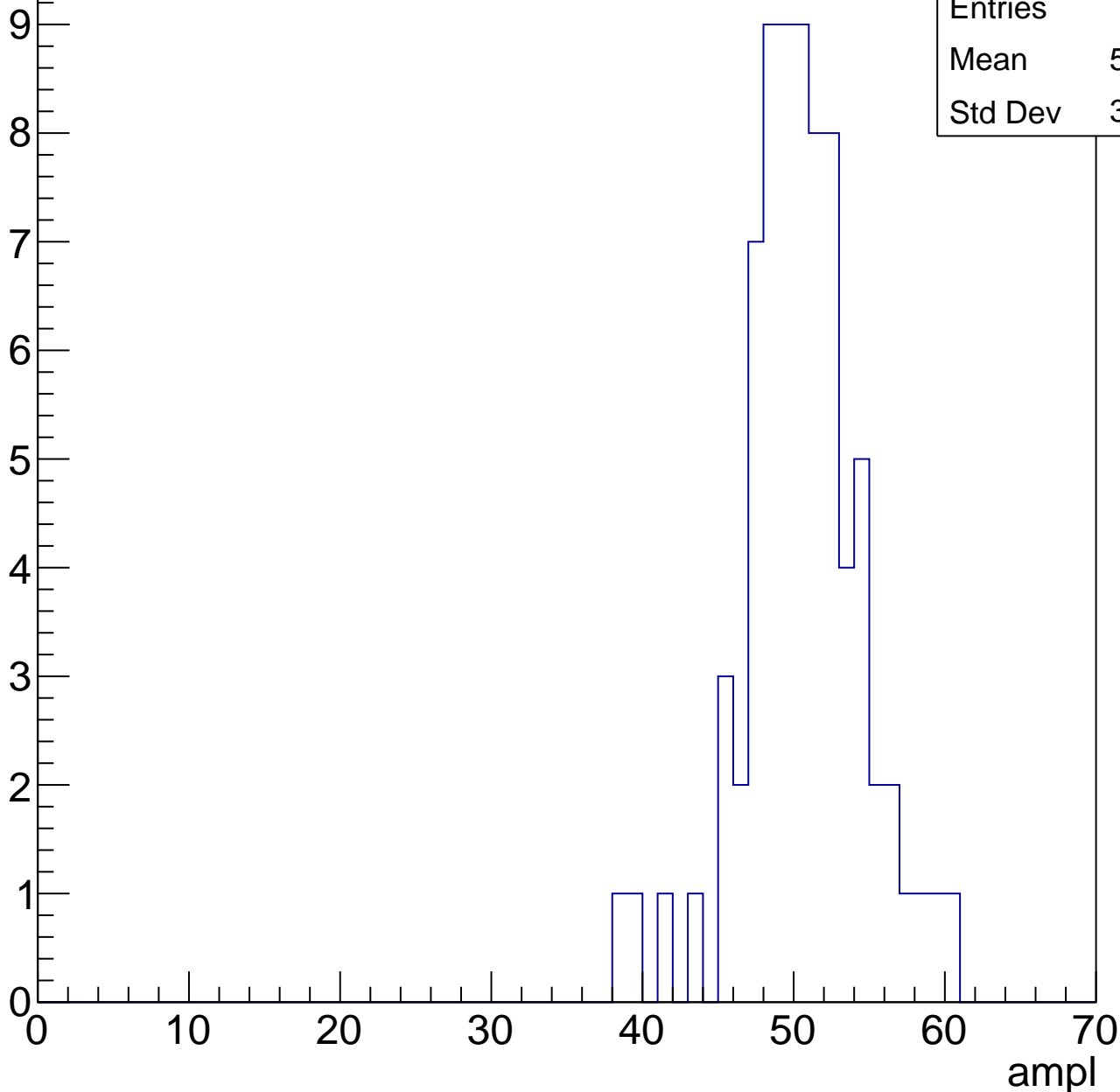


# B1L103S, U21-ch5, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

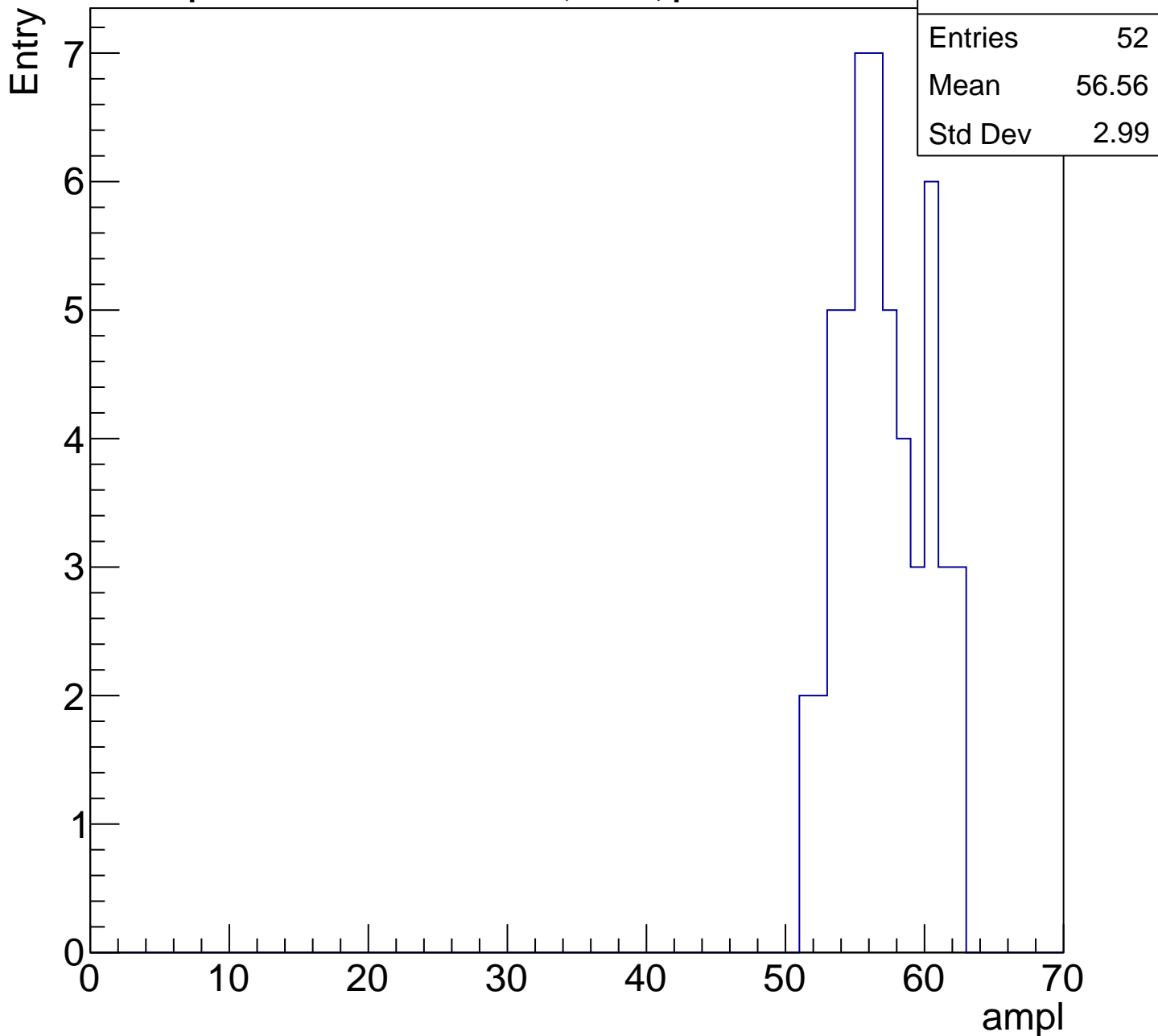
Entry

Entries	76
Mean	50.03
Std Dev	3.944



# B1L103S, U21-ch5, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

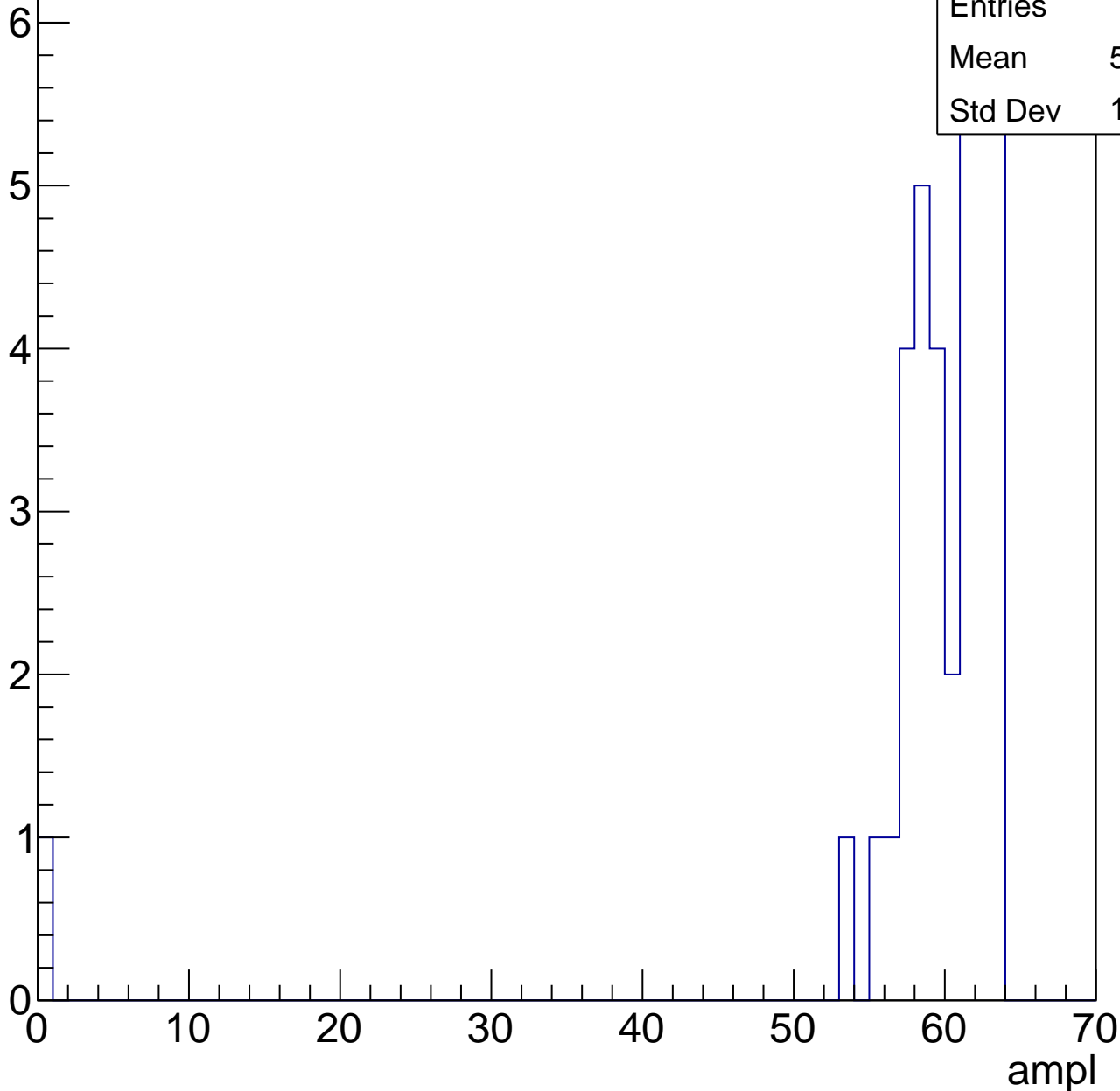


# B1L103S, U21-ch5, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

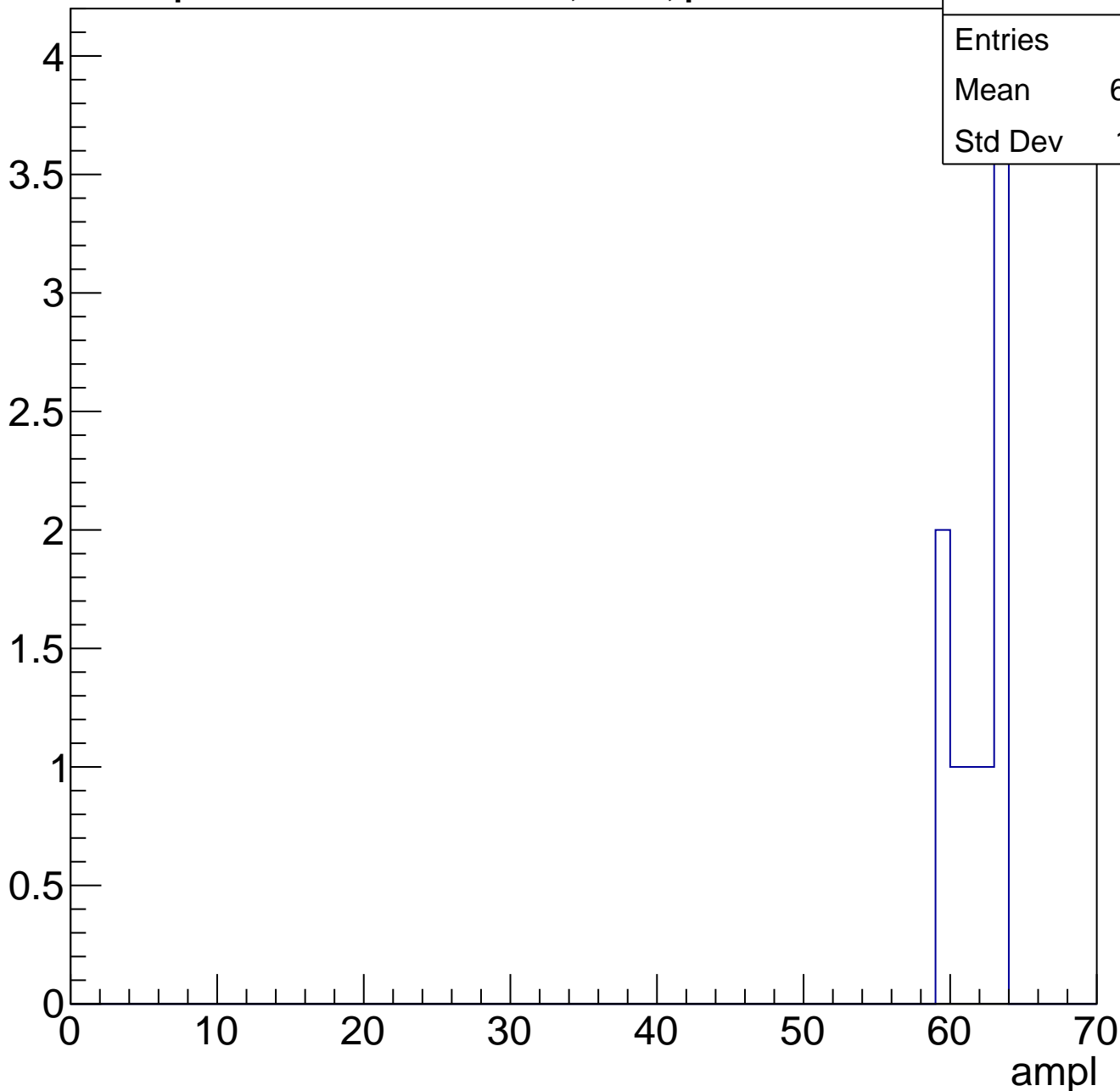
Entries	37
Mean	58.22
Std Dev	10.02



# B1L103S, U21-ch5, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U21-ch5, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U21-ch6, adc0

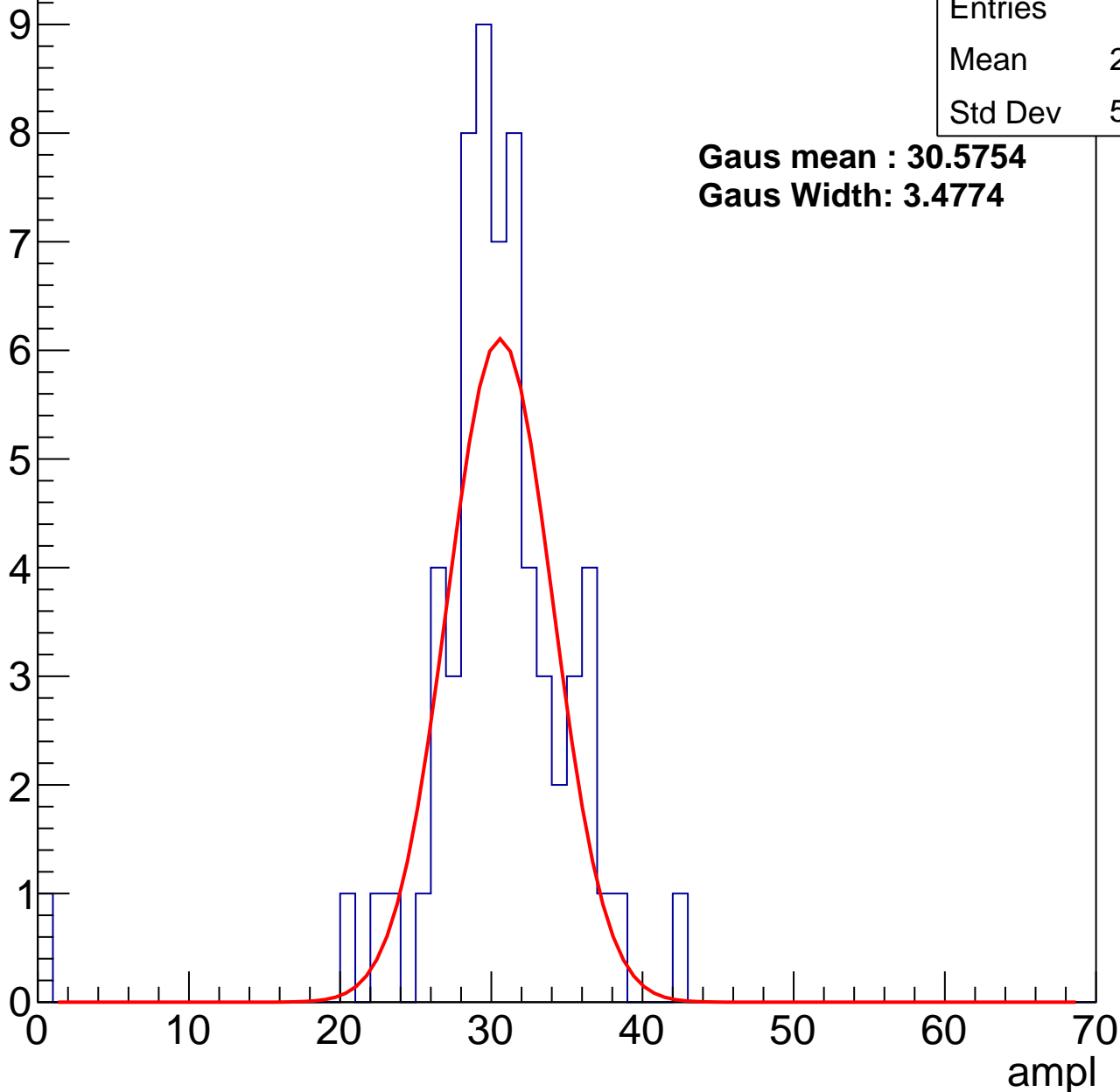
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	29.83
Std Dev	5.385

**Gaus mean : 30.5754**

**Gaus Width: 3.4774**



# B1L103S, U21-ch6, adc1

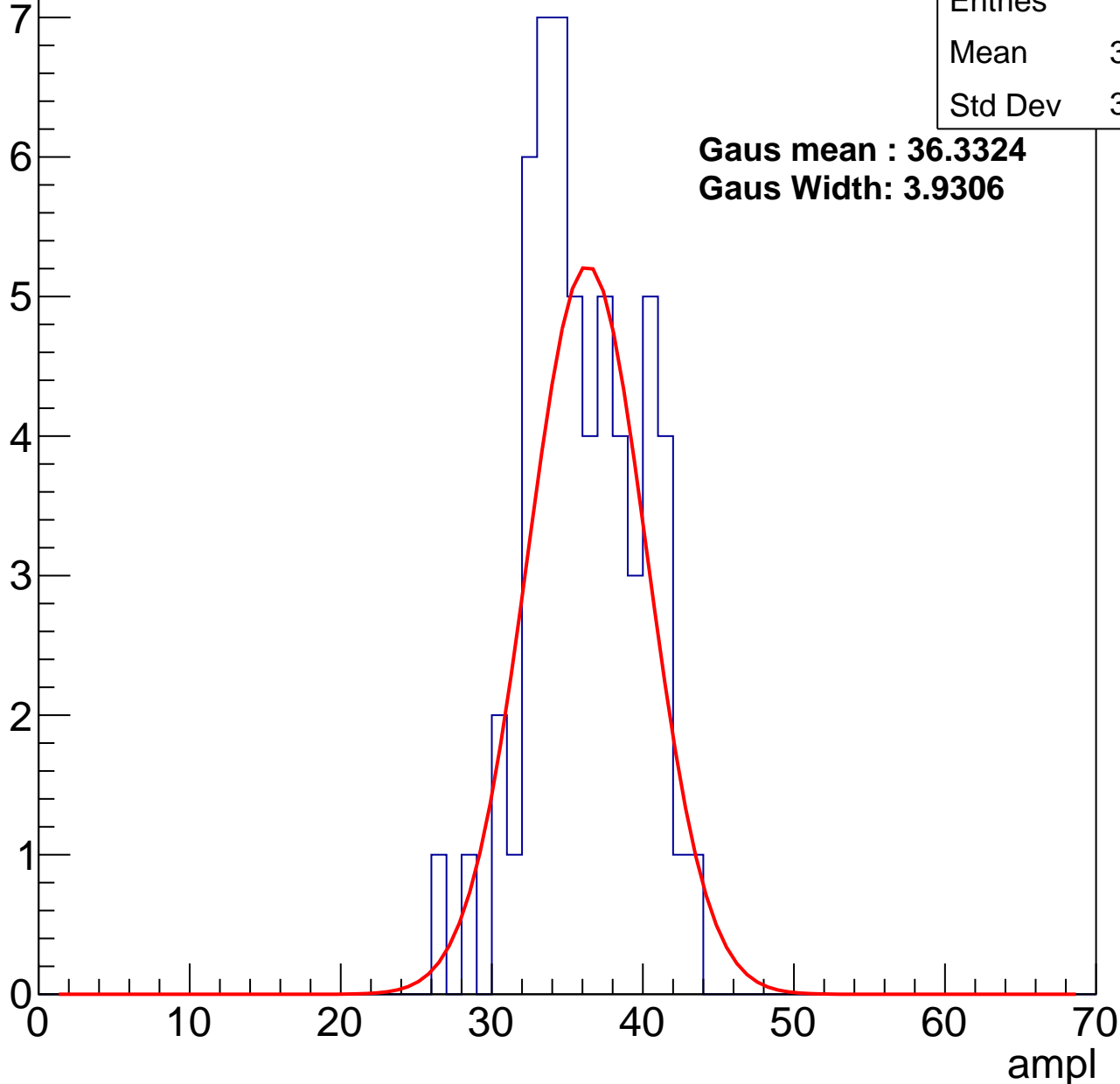
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	35.58
Std Dev	3.642

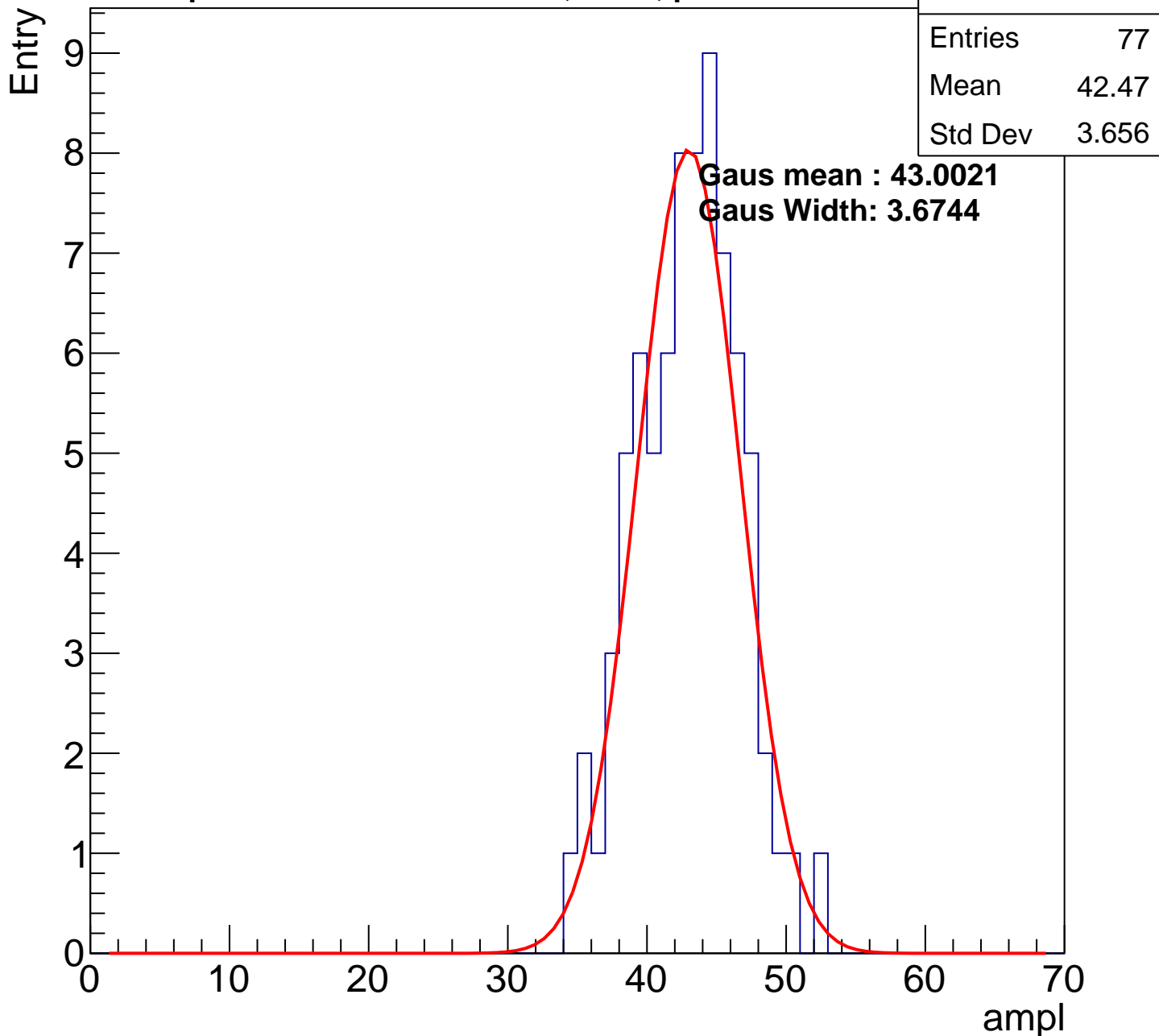
**Gaus mean : 36.3324**

**Gaus Width: 3.9306**



# B1L103S, U21-ch6, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U21-ch6, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

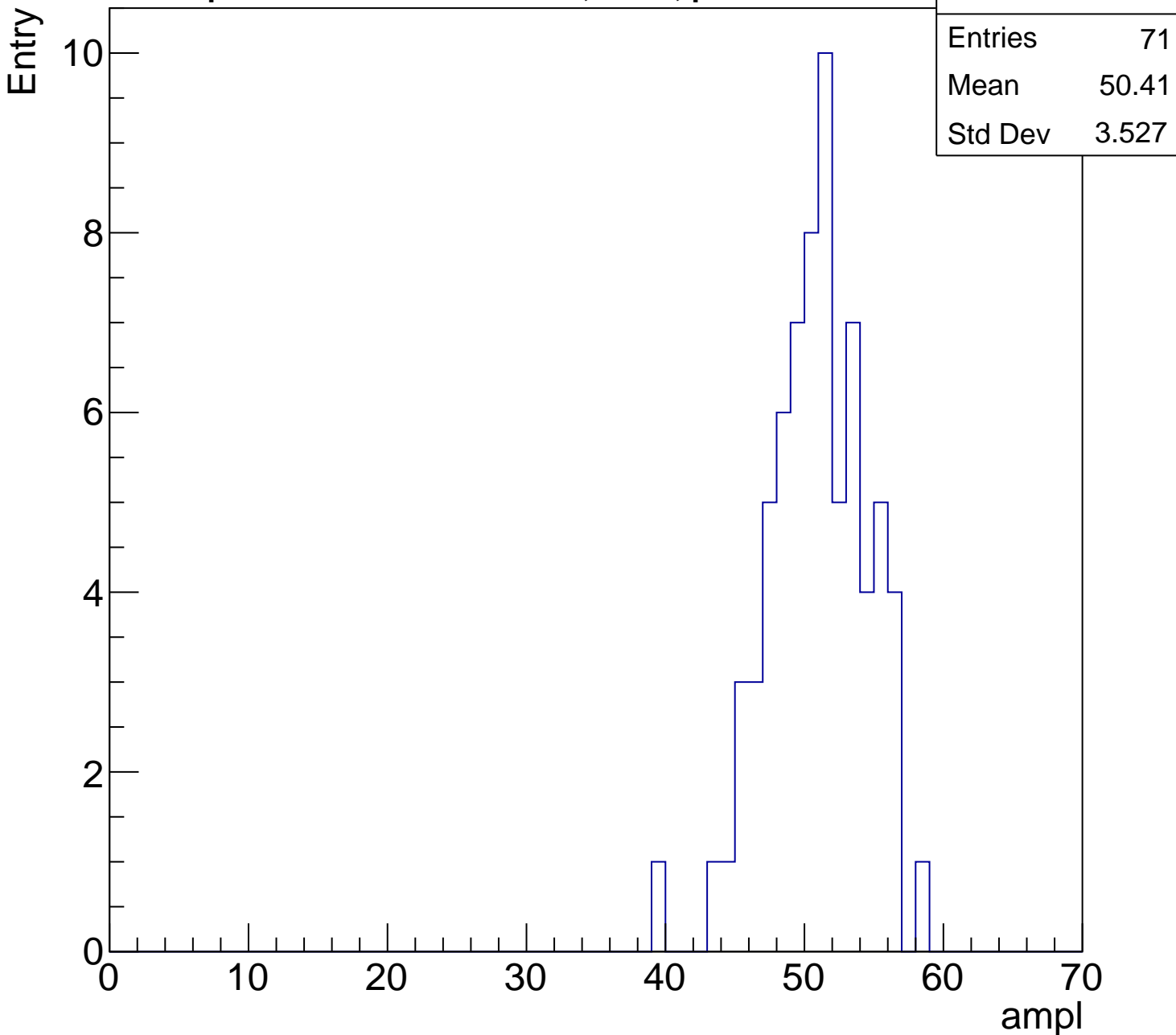
Entries	71
Mean	50.41
Std Dev	3.527

Entry

10  
8  
6  
4  
2  
0

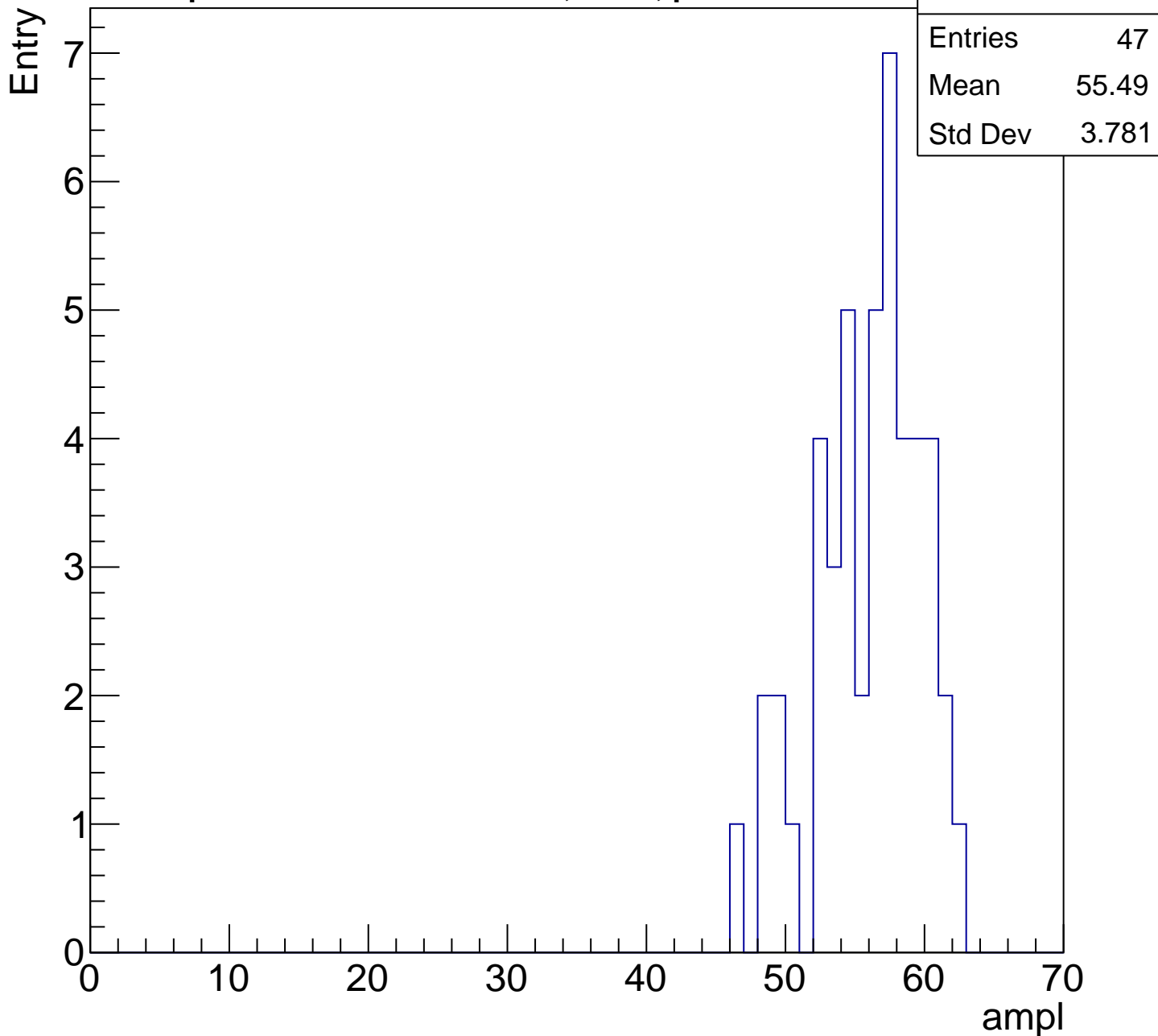
0 10 20 30 40 50 60 70

ampl



# B1L103S, U21-ch6, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

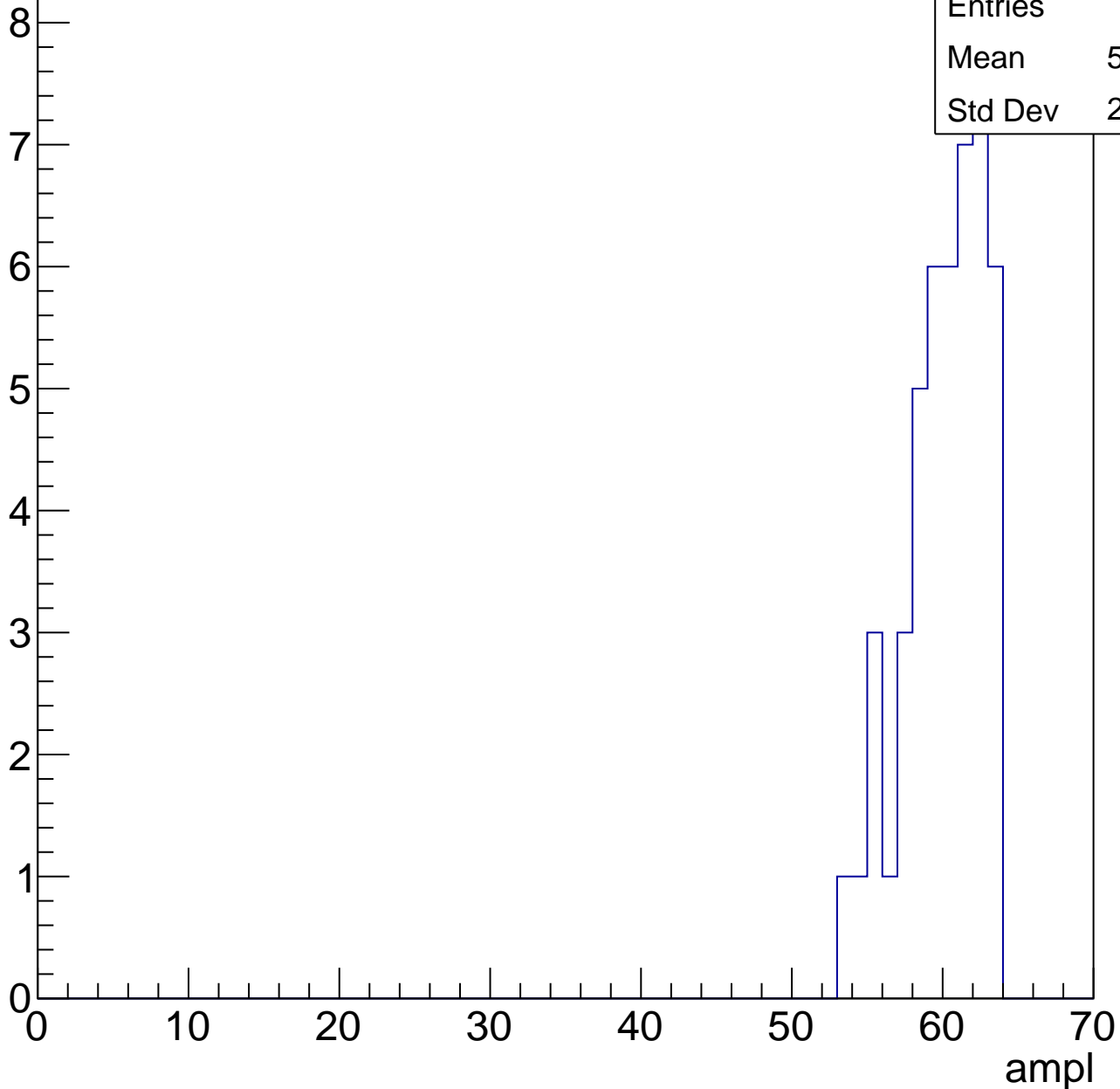


# B1L103S, U21-ch6, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

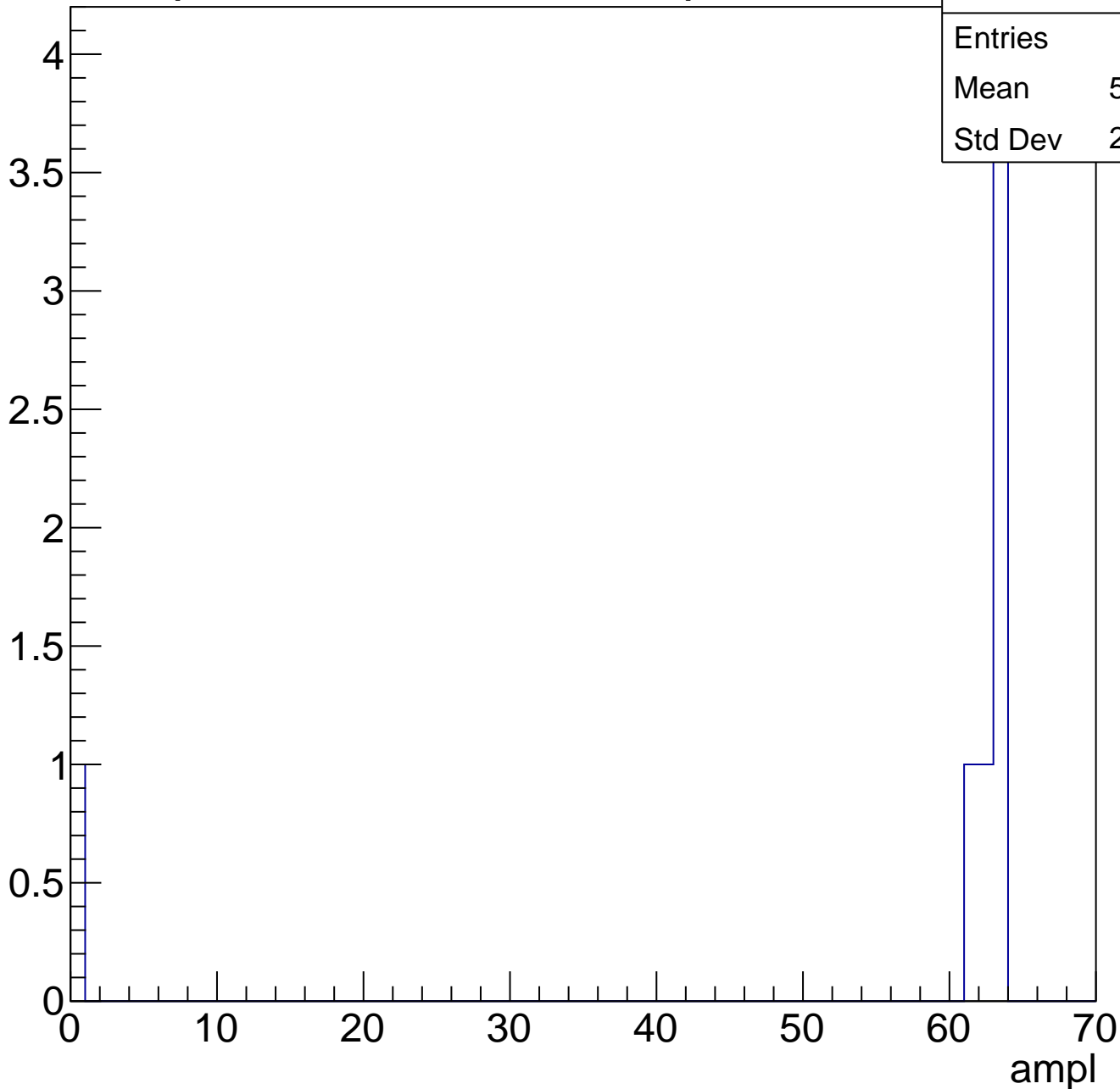
Entries	47
Mean	59.66
Std Dev	2.595



# B1L103S, U21-ch6, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U21-ch6, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U21-ch7, adc0

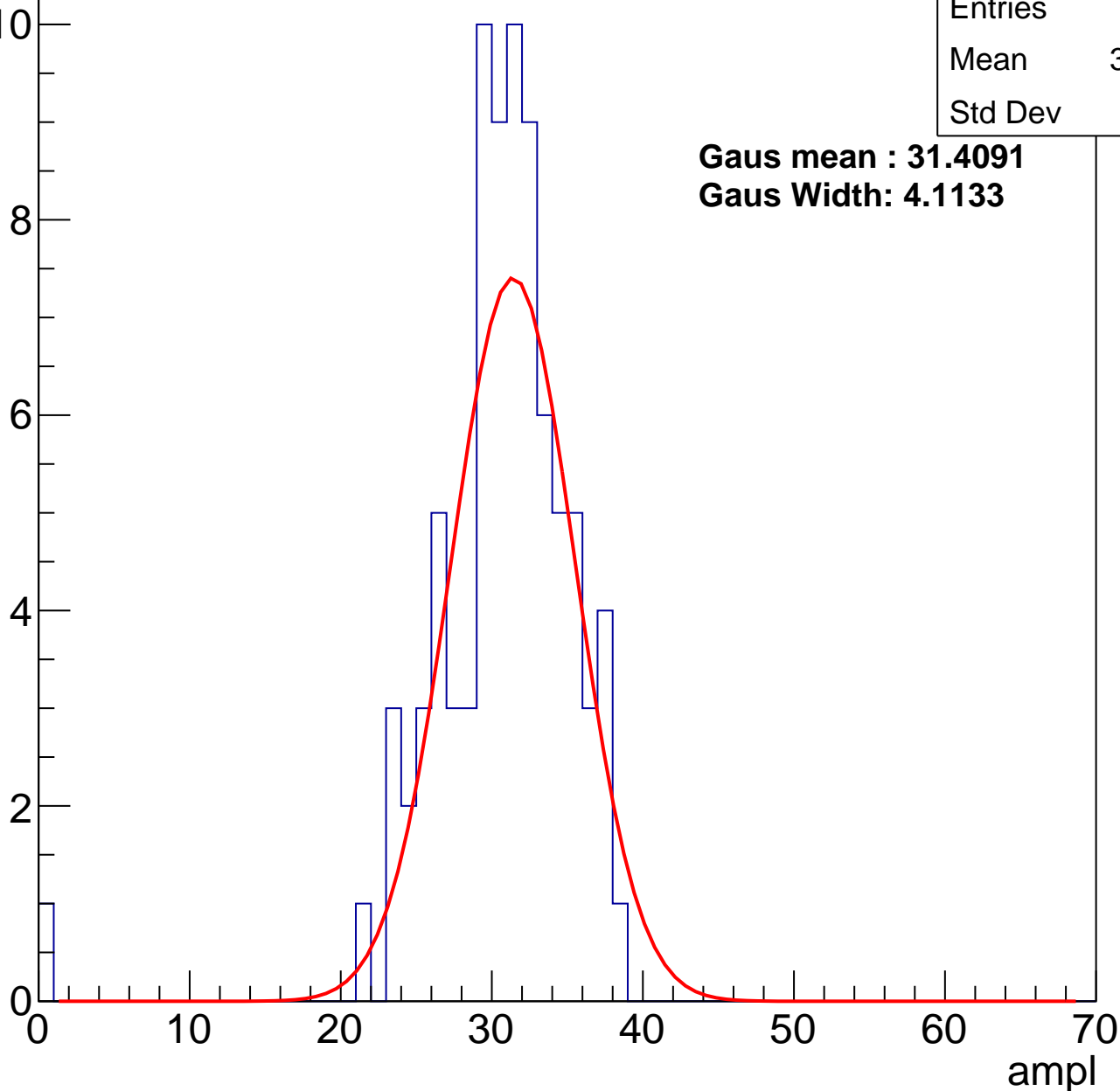
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	83
Mean	30.16
Std Dev	5

**Gaus mean : 31.4091**

**Gaus Width: 4.1133**



# B1L103S, U21-ch7, adc1

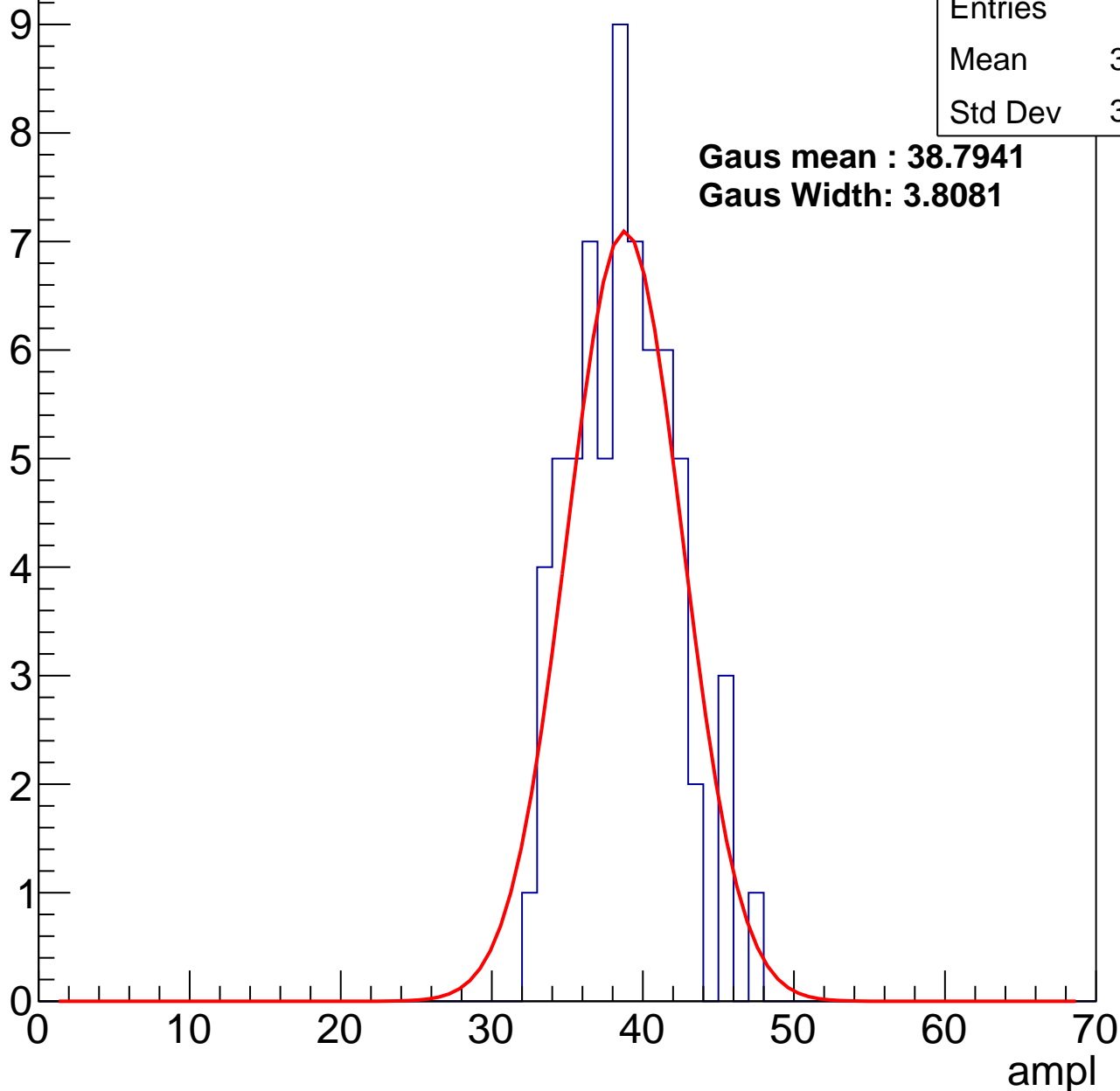
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	38.26
Std Dev	3.332

**Gaus mean : 38.7941**

**Gaus Width: 3.8081**



# B1L103S, U21-ch7, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	52
Mean	43.71
Std Dev	2.911

**Gaus mean : 43.8570**

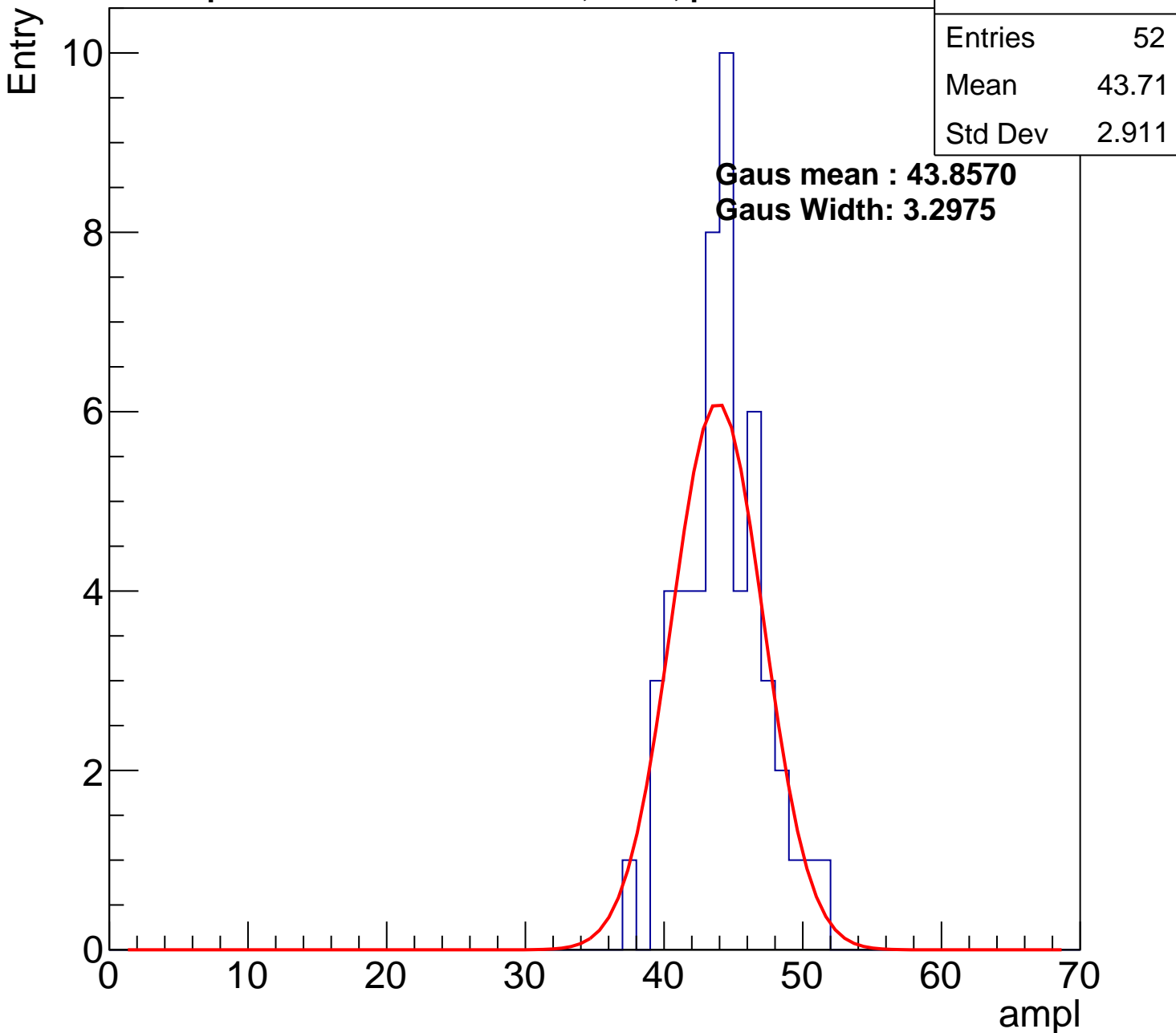
**Gaus Width: 3.2975**

Entry

10  
8  
6  
4  
2  
0

ampl

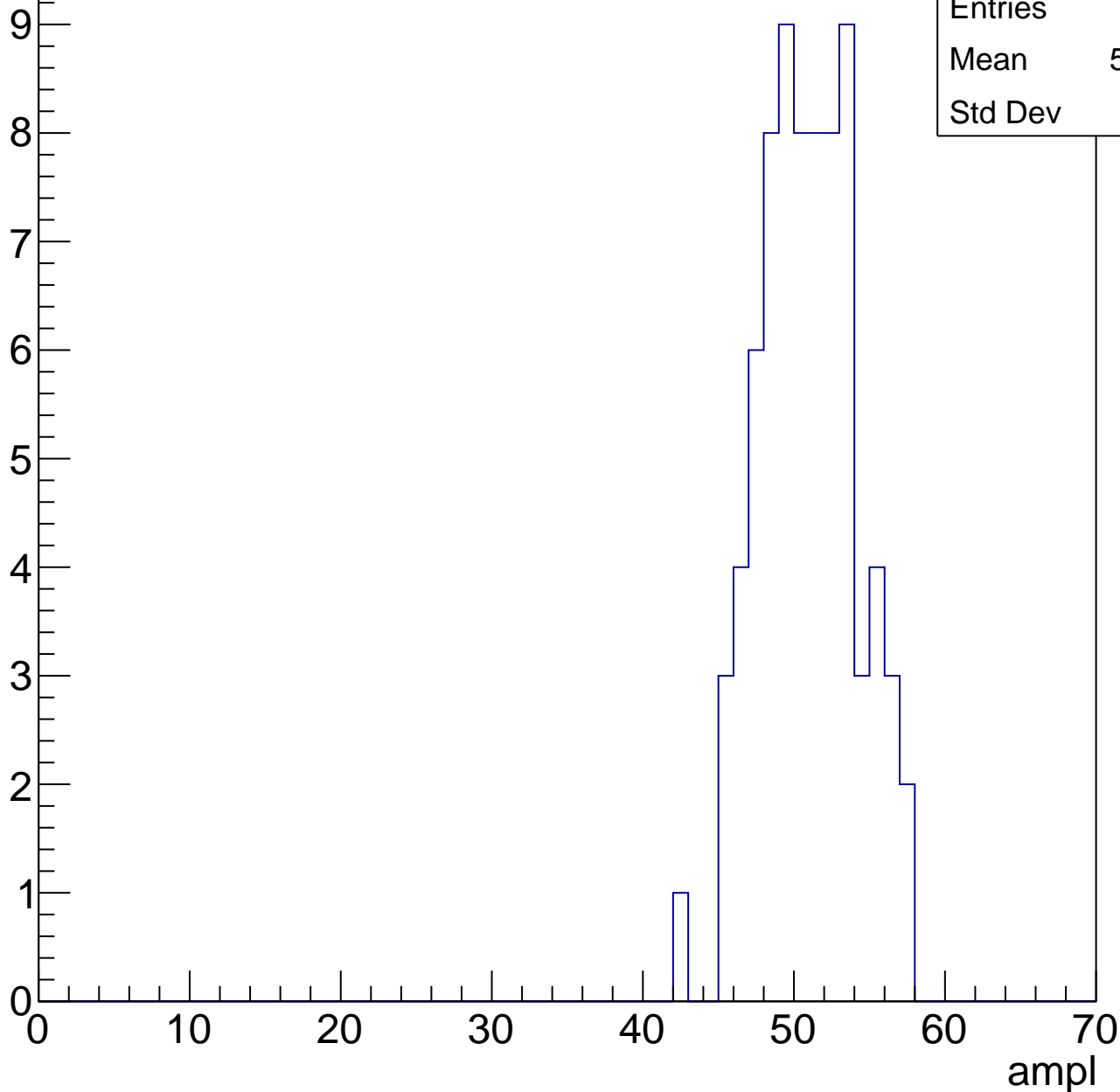
0 10 20 30 40 50 60 70



# B1L103S, U21-ch7, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

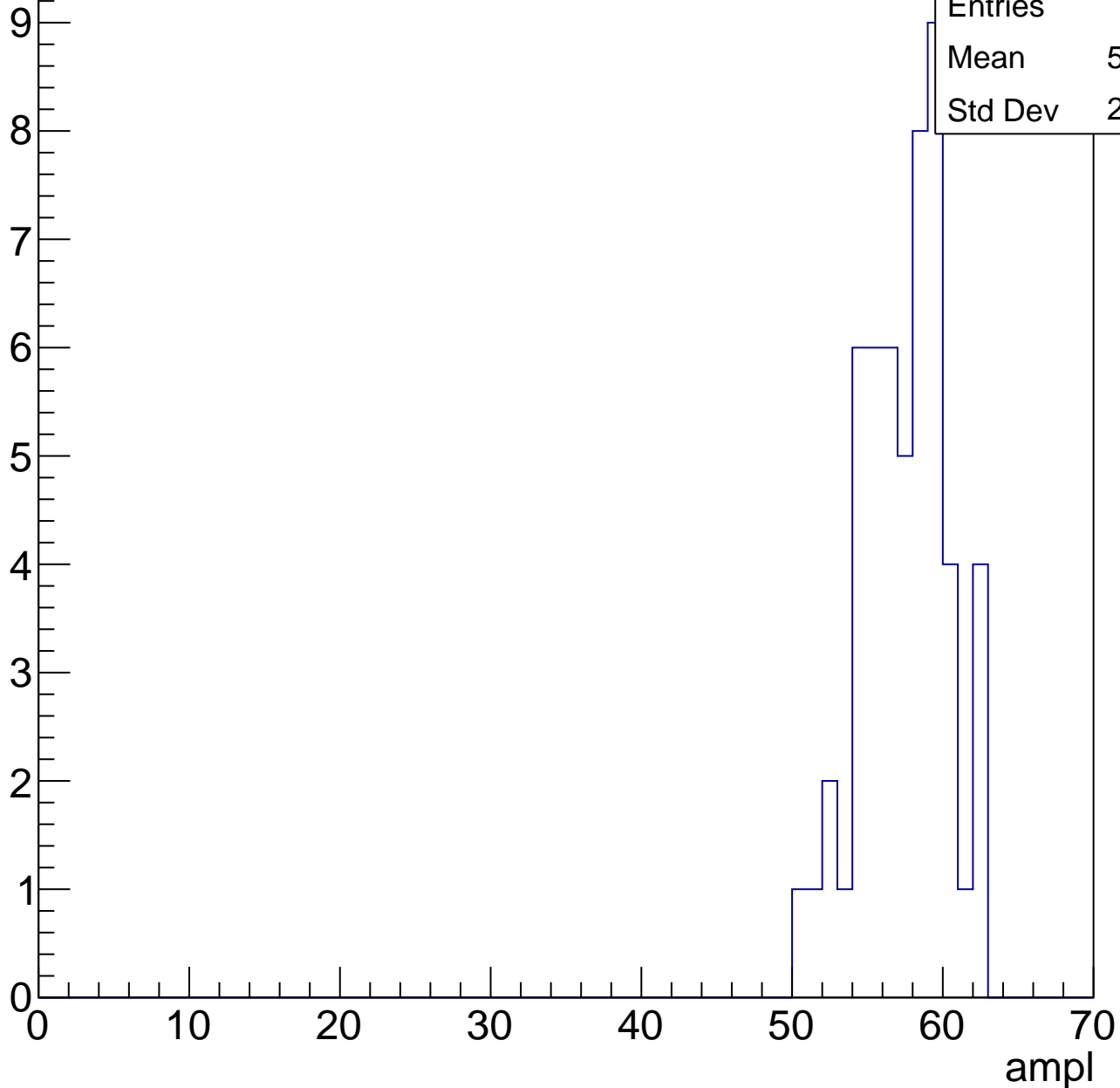
Entry



# B1L103S, U21-ch7, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



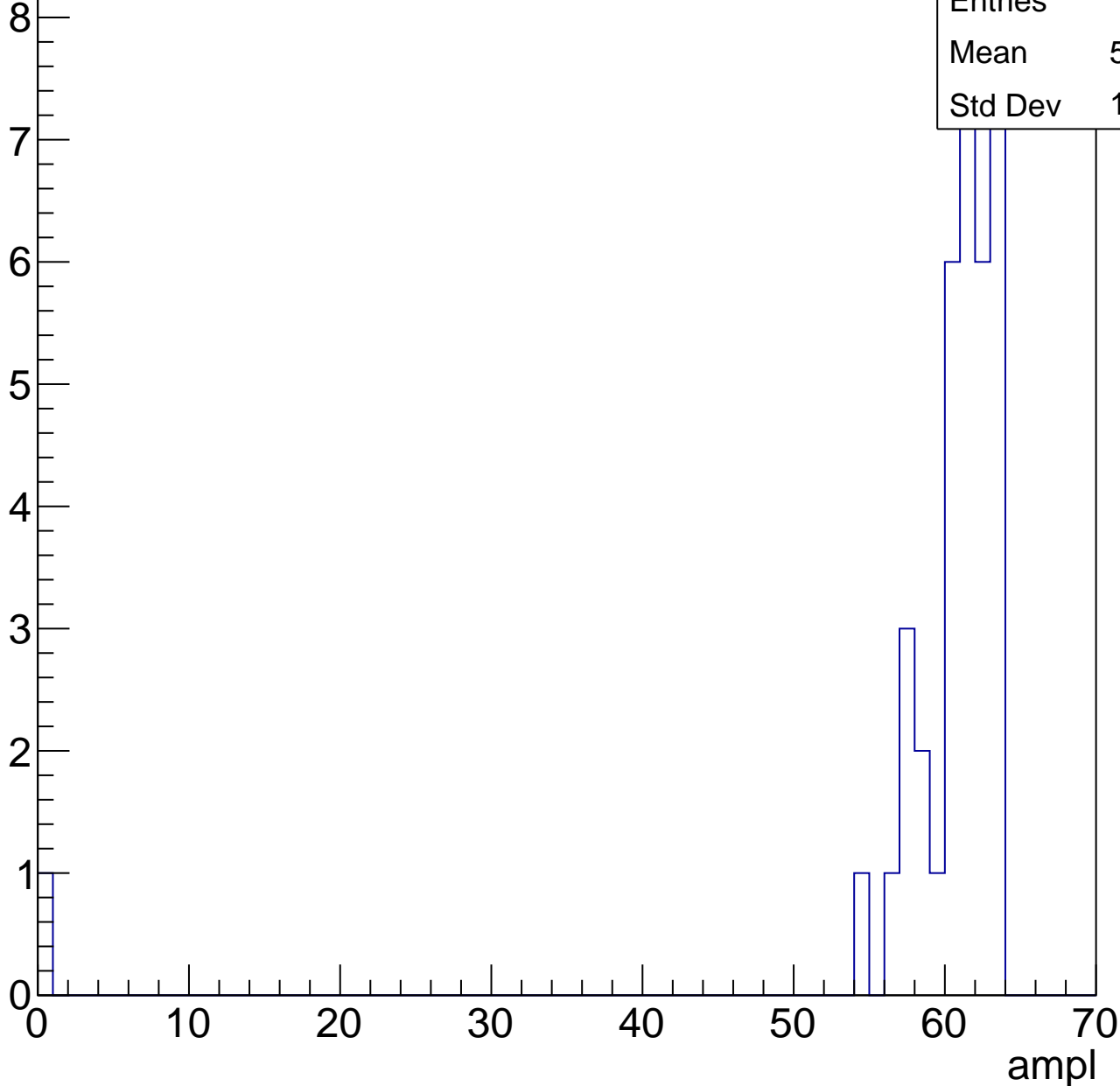
Entries	54
Mean	56.98
Std Dev	2.825

# B1L103S, U21-ch7, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

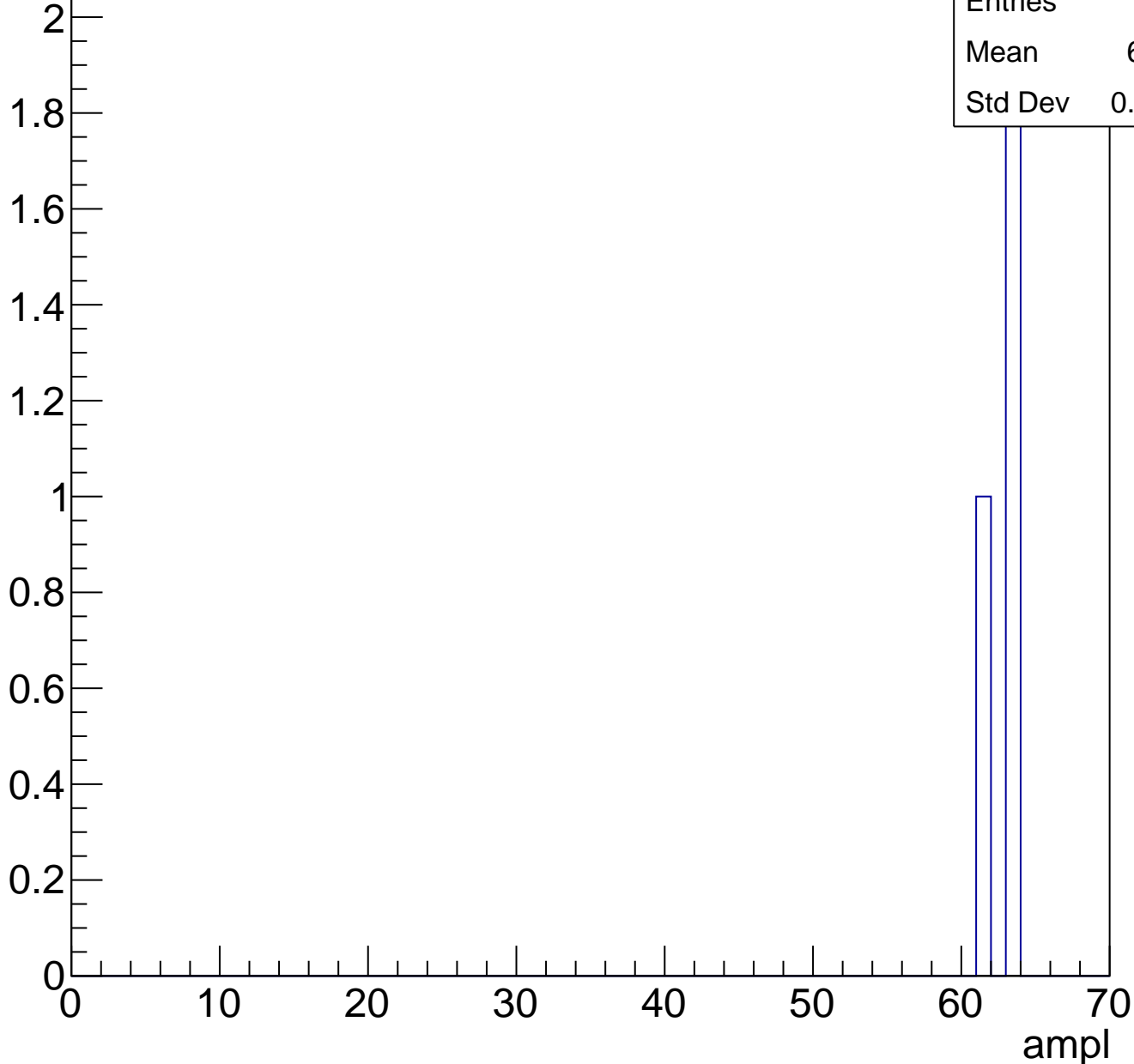
Entries	37
Mean	58.92
Std Dev	10.07



# B1L103S, U21-ch7, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U21-ch7, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U21-ch8, adc0

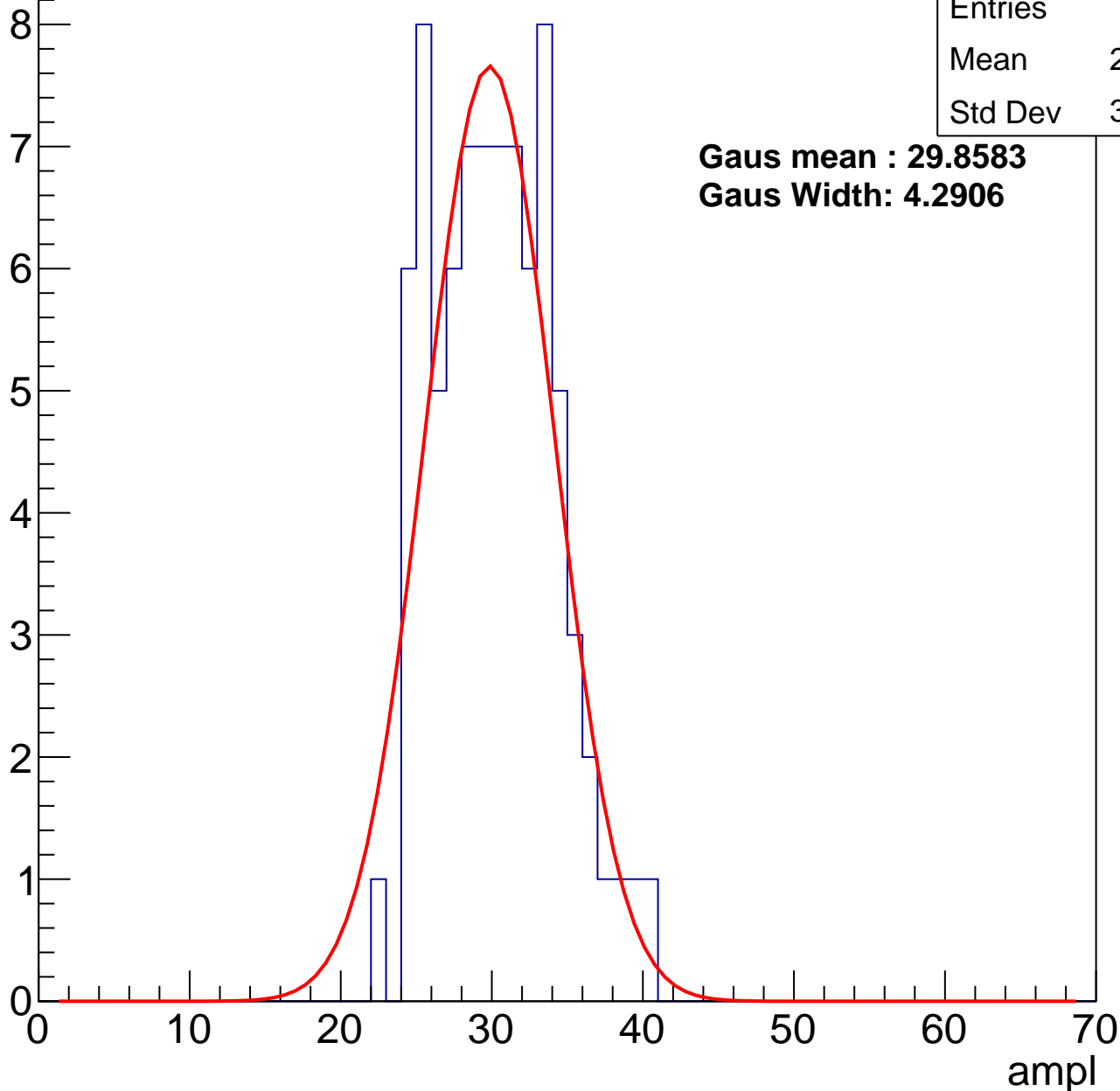
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	82
Mean	29.77
Std Dev	3.933

**Gaus mean : 29.8583**

**Gaus Width: 4.2906**



# B1L103S, U21-ch8, adc1

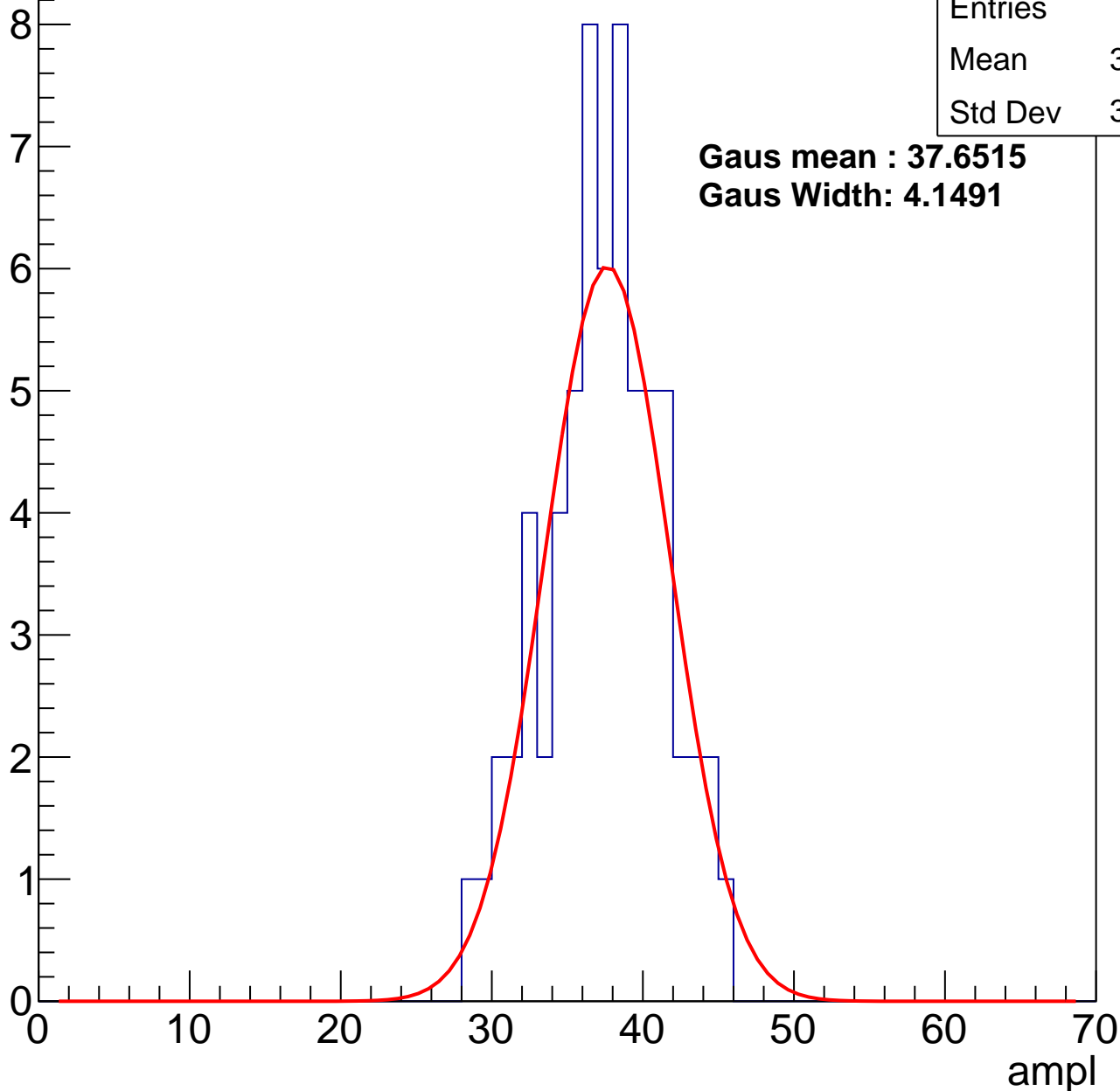
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	36.94
Std Dev	3.818

**Gaus mean : 37.6515**

**Gaus Width: 4.1491**



# B1L103S, U21-ch8, adc2

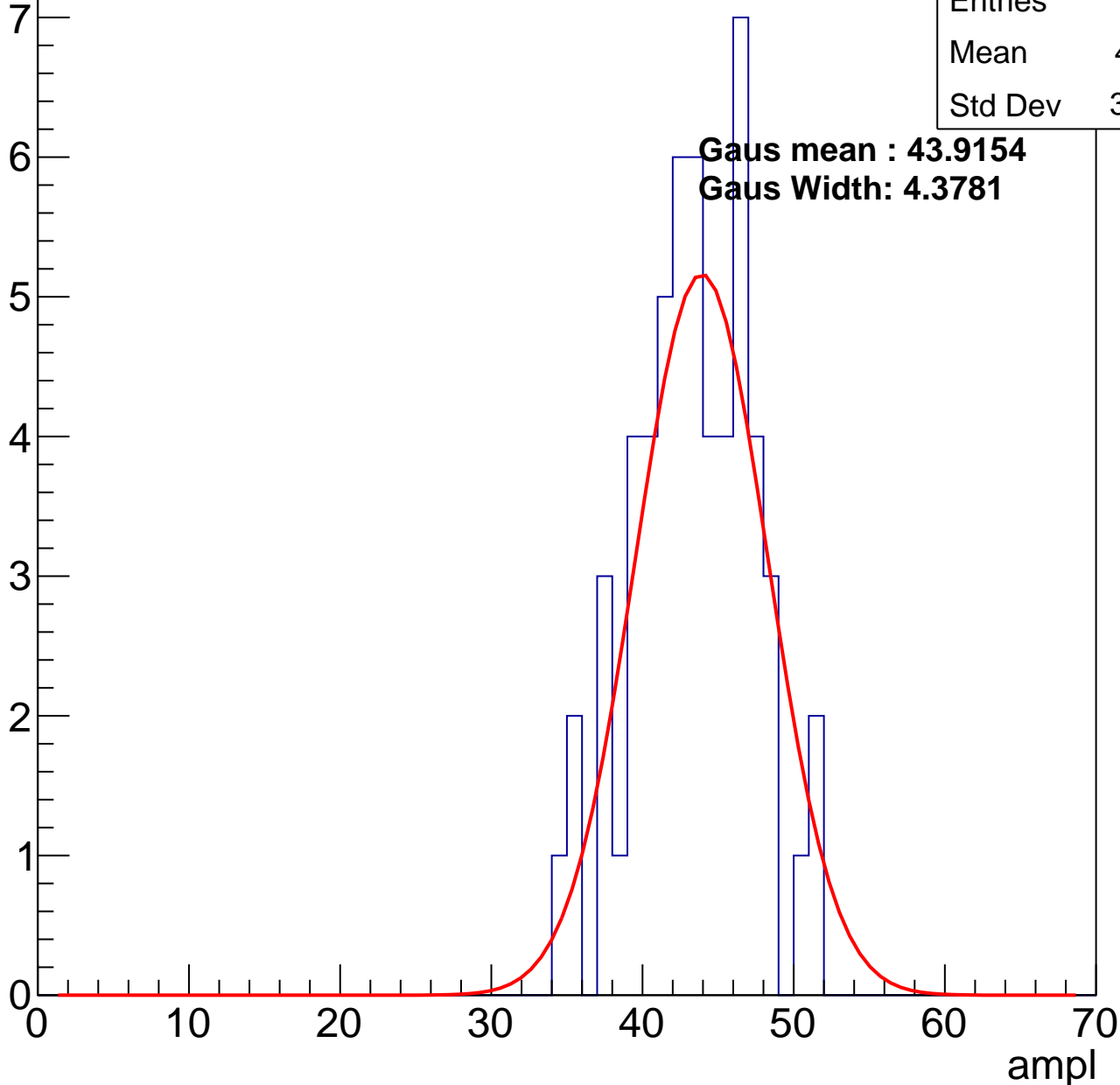
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	42.91
Std Dev	3.899

**Gaus mean : 43.9154**

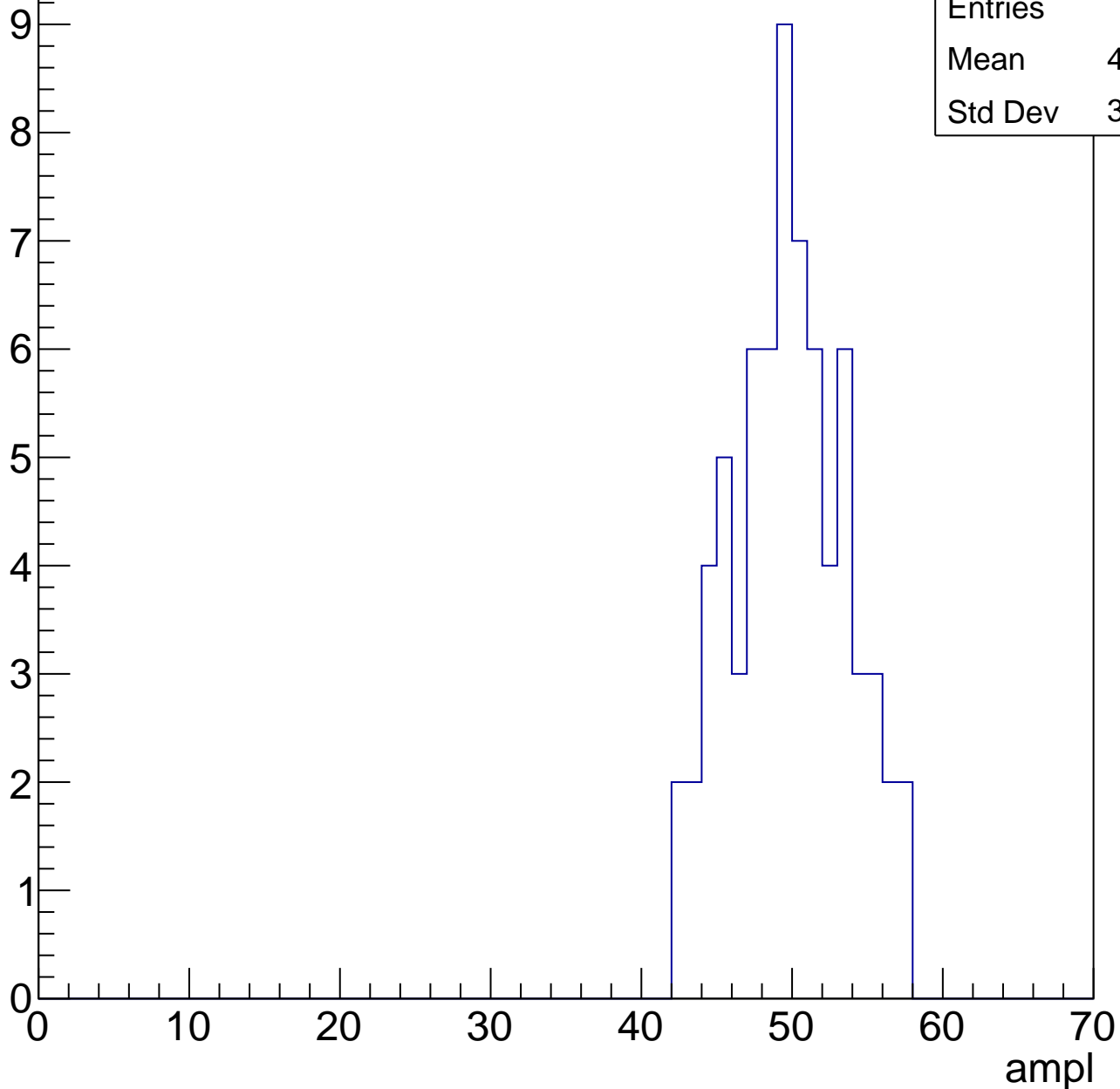
**Gaus Width: 4.3781**



# B1L103S, U21-ch8, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

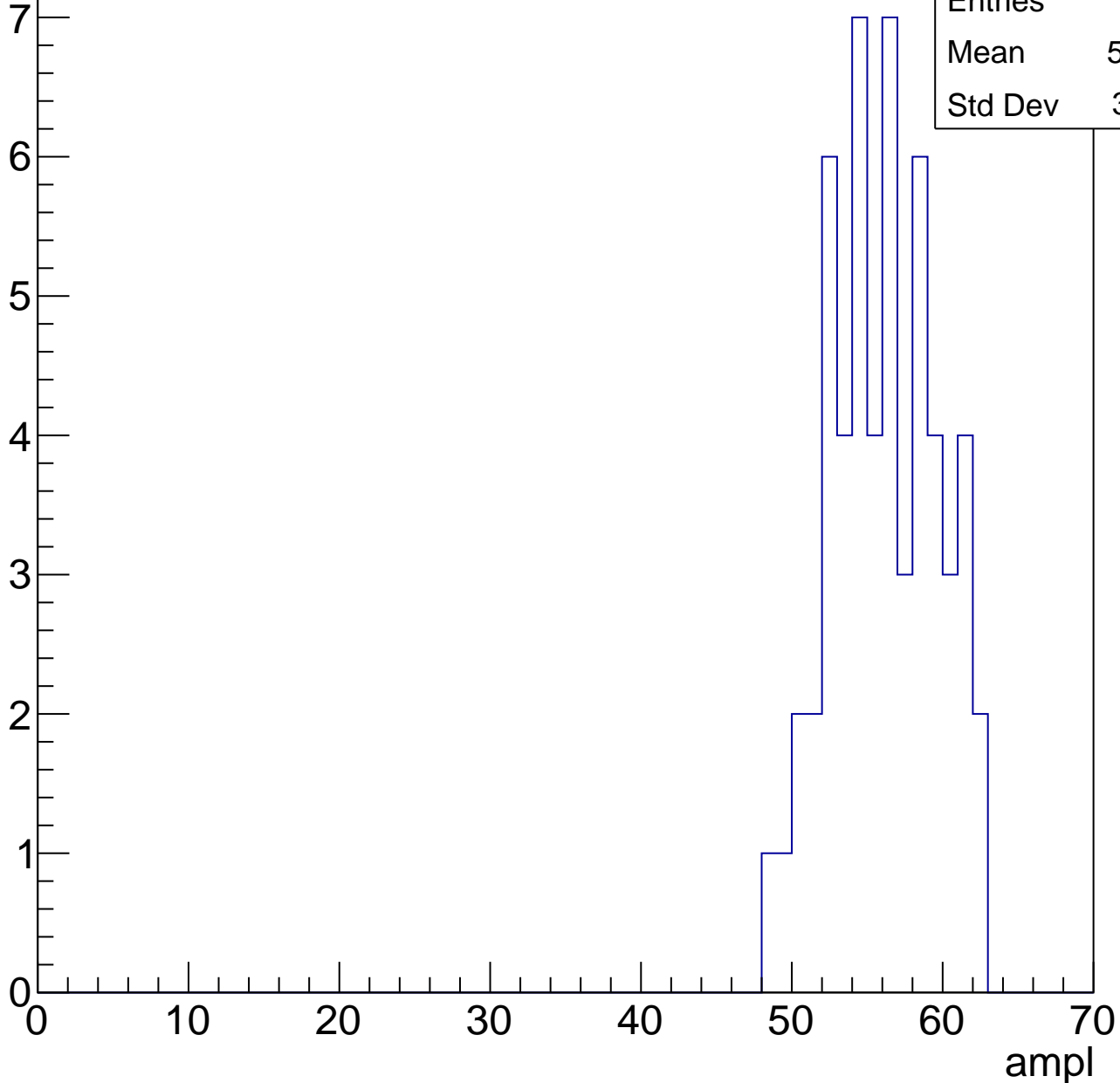


# B1L103S, U21-ch8, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	55.64
Std Dev	3.471



# B1L103S, U21-ch8, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

7

6

5

4

3

2

1

0

Entries

41

Mean

59.85

Std Dev

2.385

0

10

20

30

40

50

60

ampl

0

1

2

3

4

5

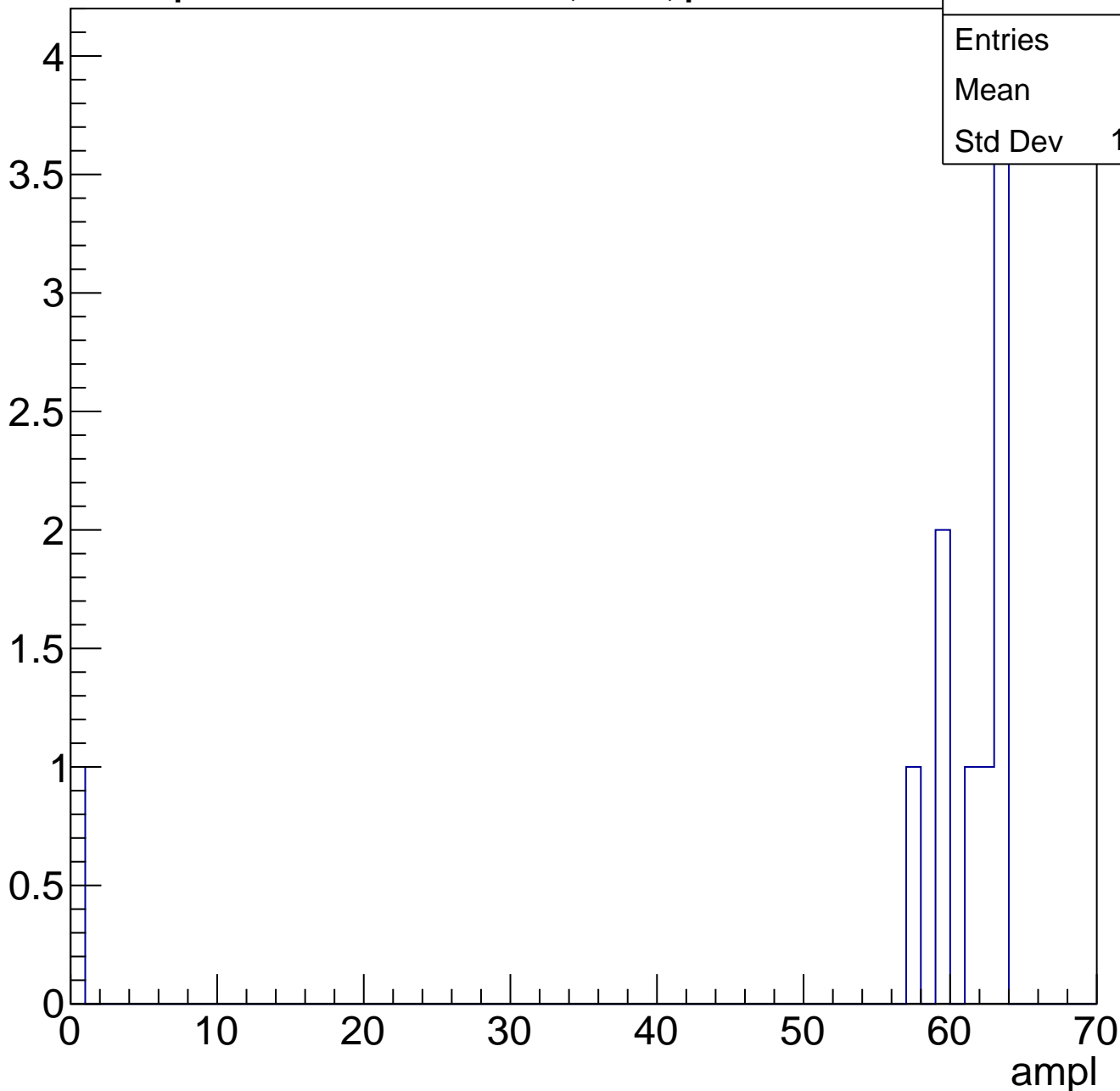
6

7

# B1L103S, U21-ch8, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	10
Mean	55
Std Dev	18.44



# B1L103S, U21-ch8, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U21-ch9, adc0

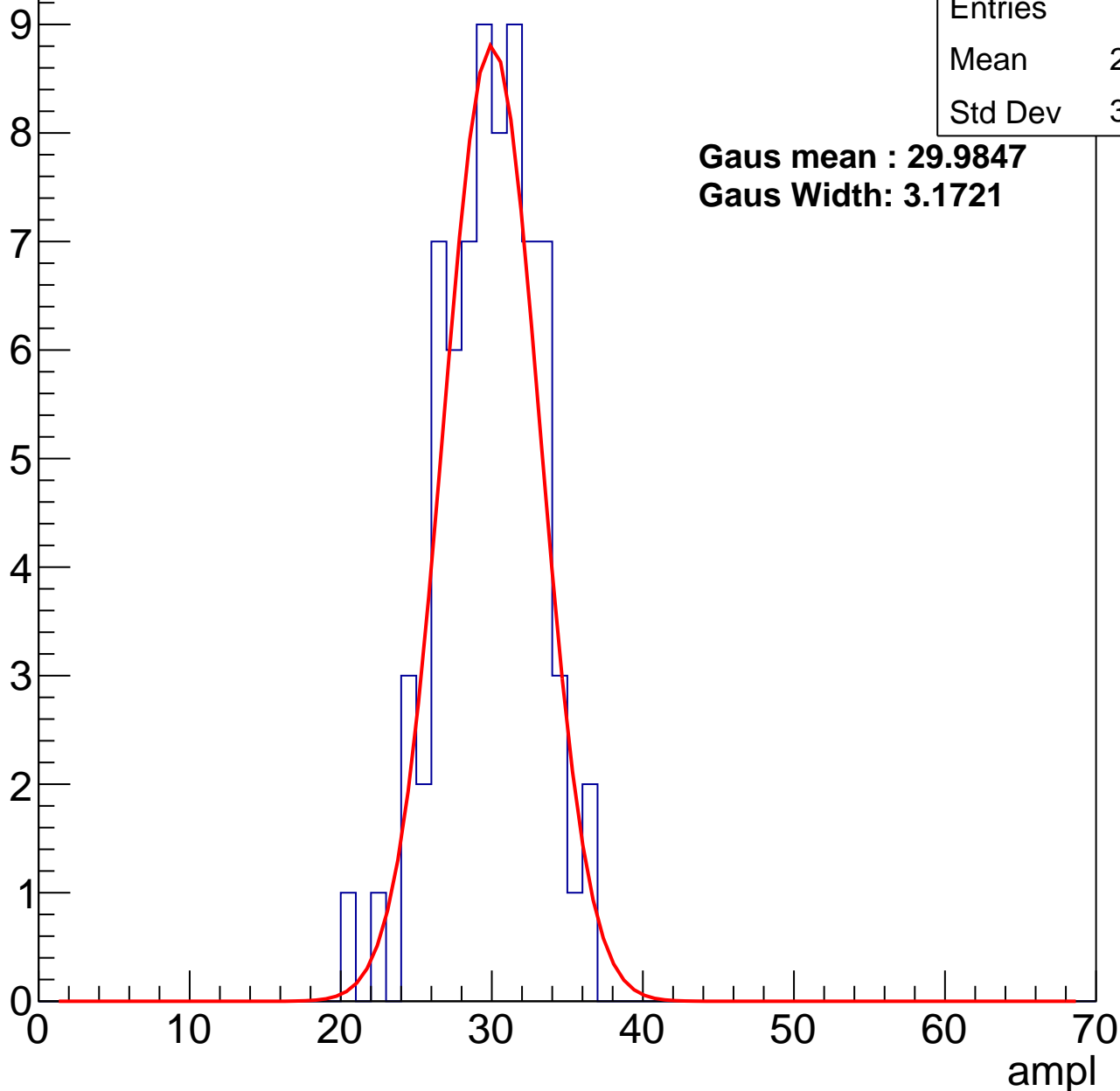
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	29.42
Std Dev	3.196

**Gaus mean : 29.9847**

**Gaus Width: 3.1721**



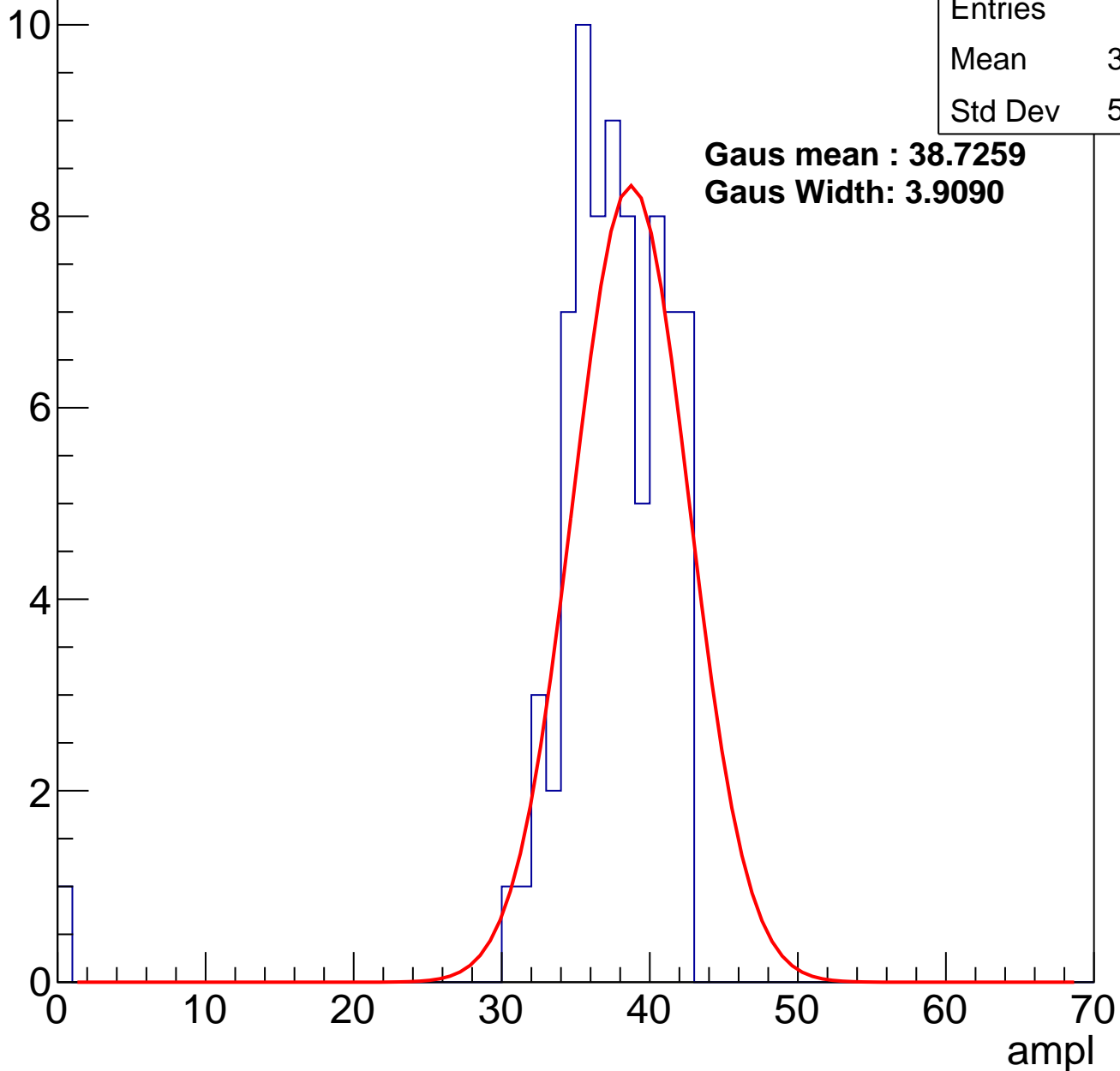
# B1L103S, U21-ch9, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	77
Mean	36.78
Std Dev	5.166

**Gaus mean : 38.7259**  
**Gaus Width: 3.9090**

Entry



# B1L103S, U21-ch9, adc2

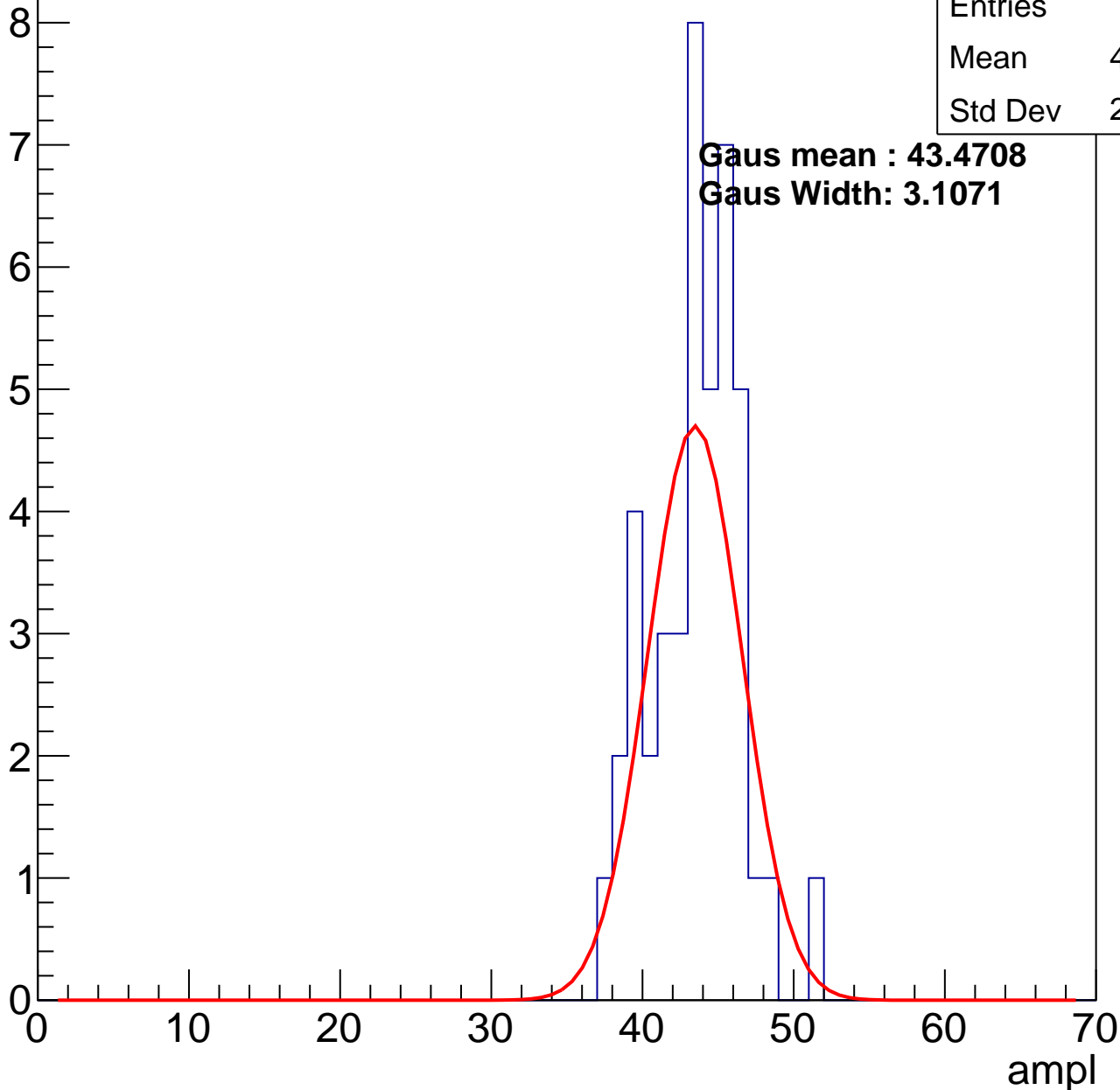
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	43
Mean	43.09
Std Dev	2.916

**Gaus mean : 43.4708**

**Gaus Width: 3.1071**

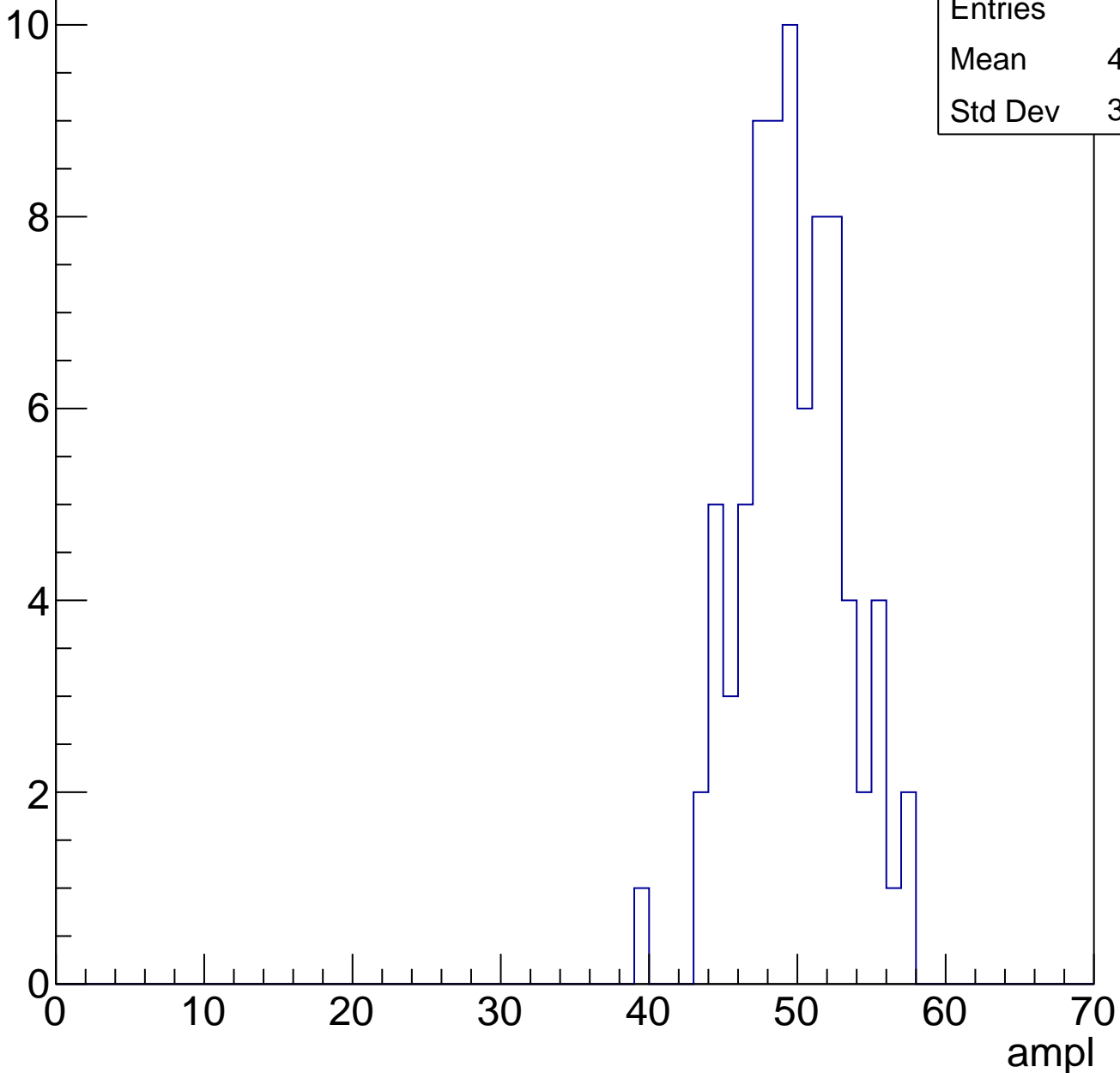


# B1L103S, U21-ch9, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	79
Mean	49.23
Std Dev	3.515

Entry

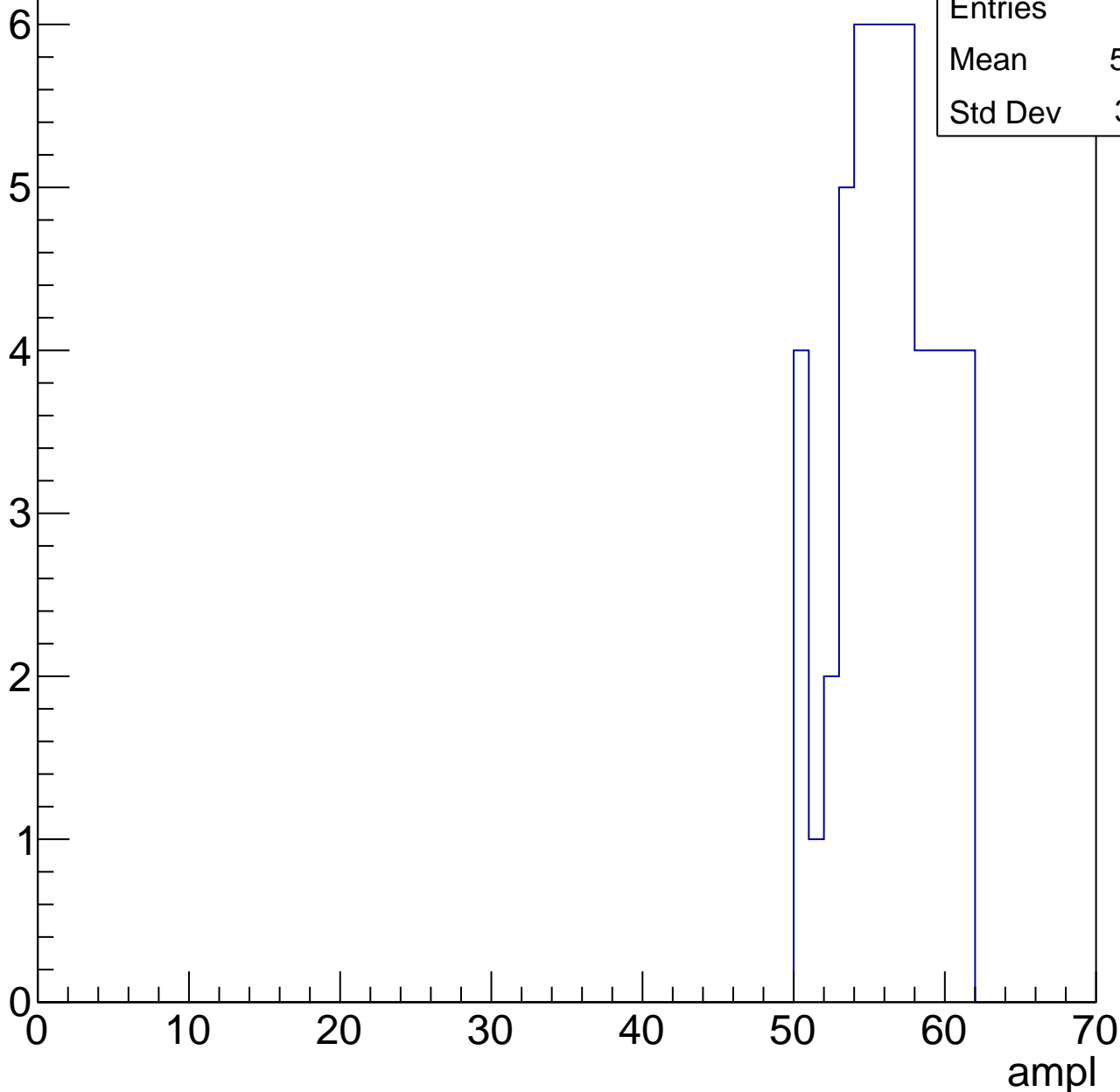


# B1L103S, U21-ch9, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	55.85
Std Dev	3.091

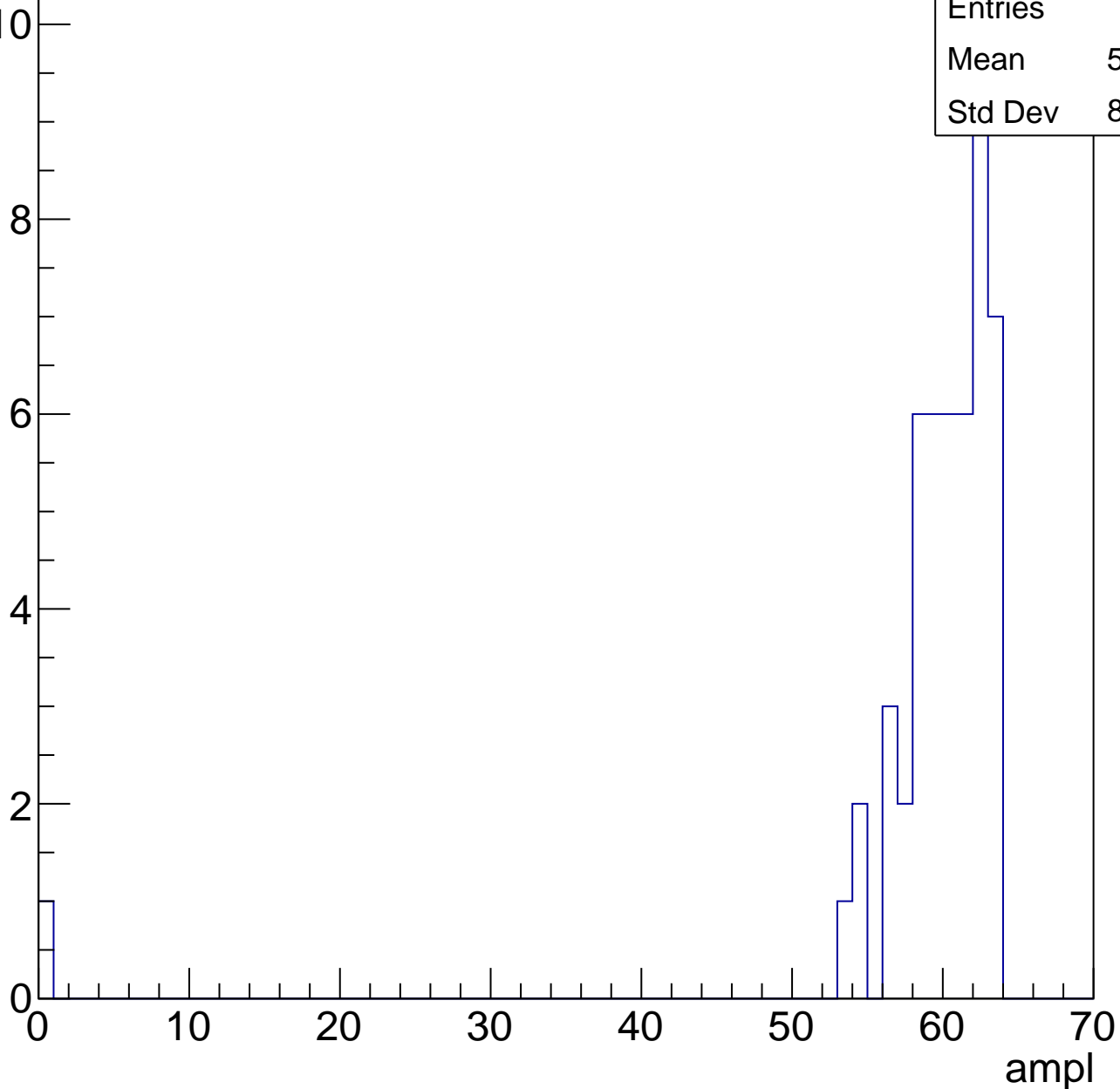


# B1L103S, U21-ch9, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	58.64
Std Dev	8.756



# B1L103S, U21-ch9, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U21-ch9, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U21-ch10, adc0

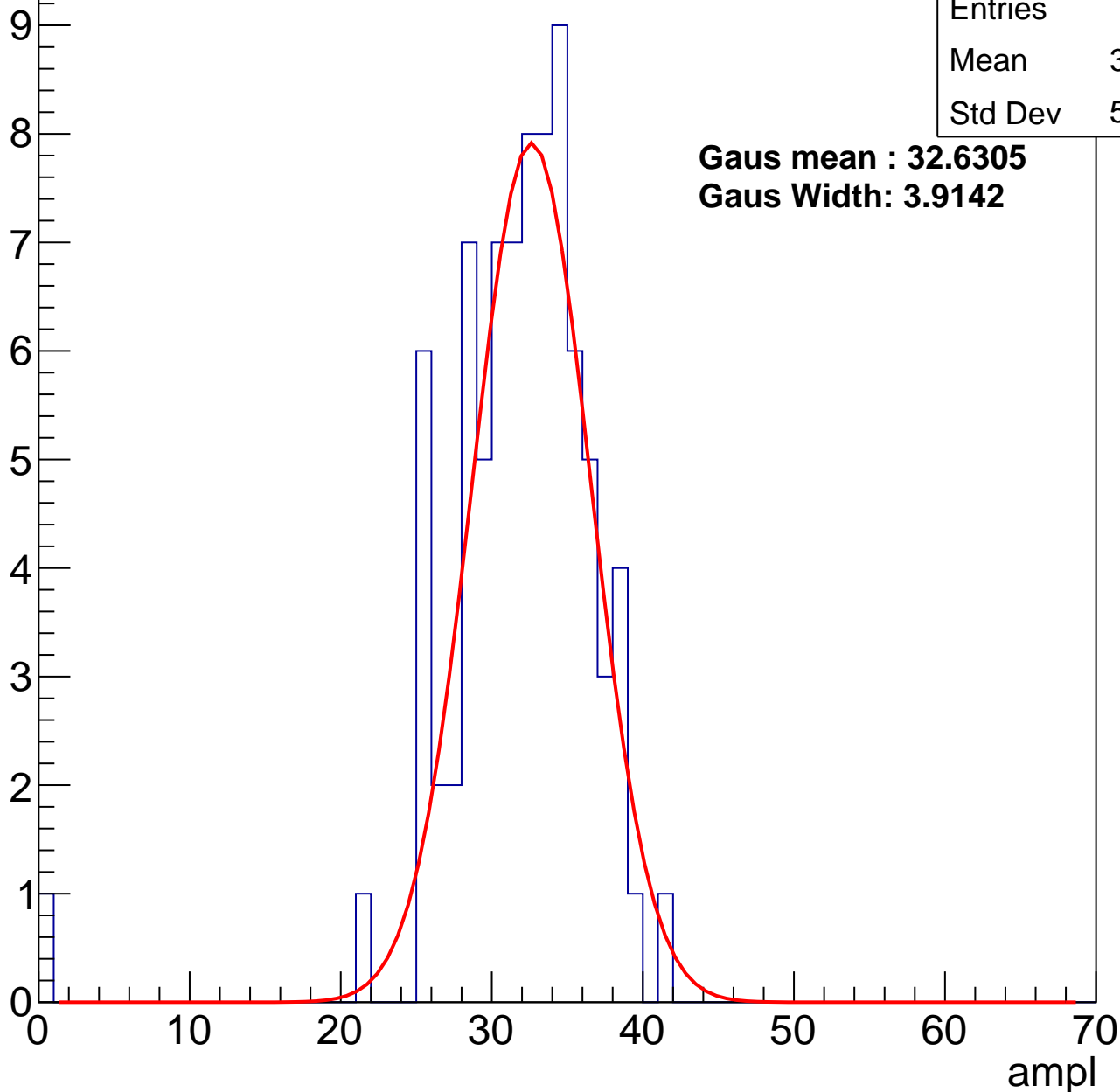
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	83
Mean	31.37
Std Dev	5.204

**Gaus mean : 32.6305**

**Gaus Width: 3.9142**



# B1L103S, U21-ch10, adc1

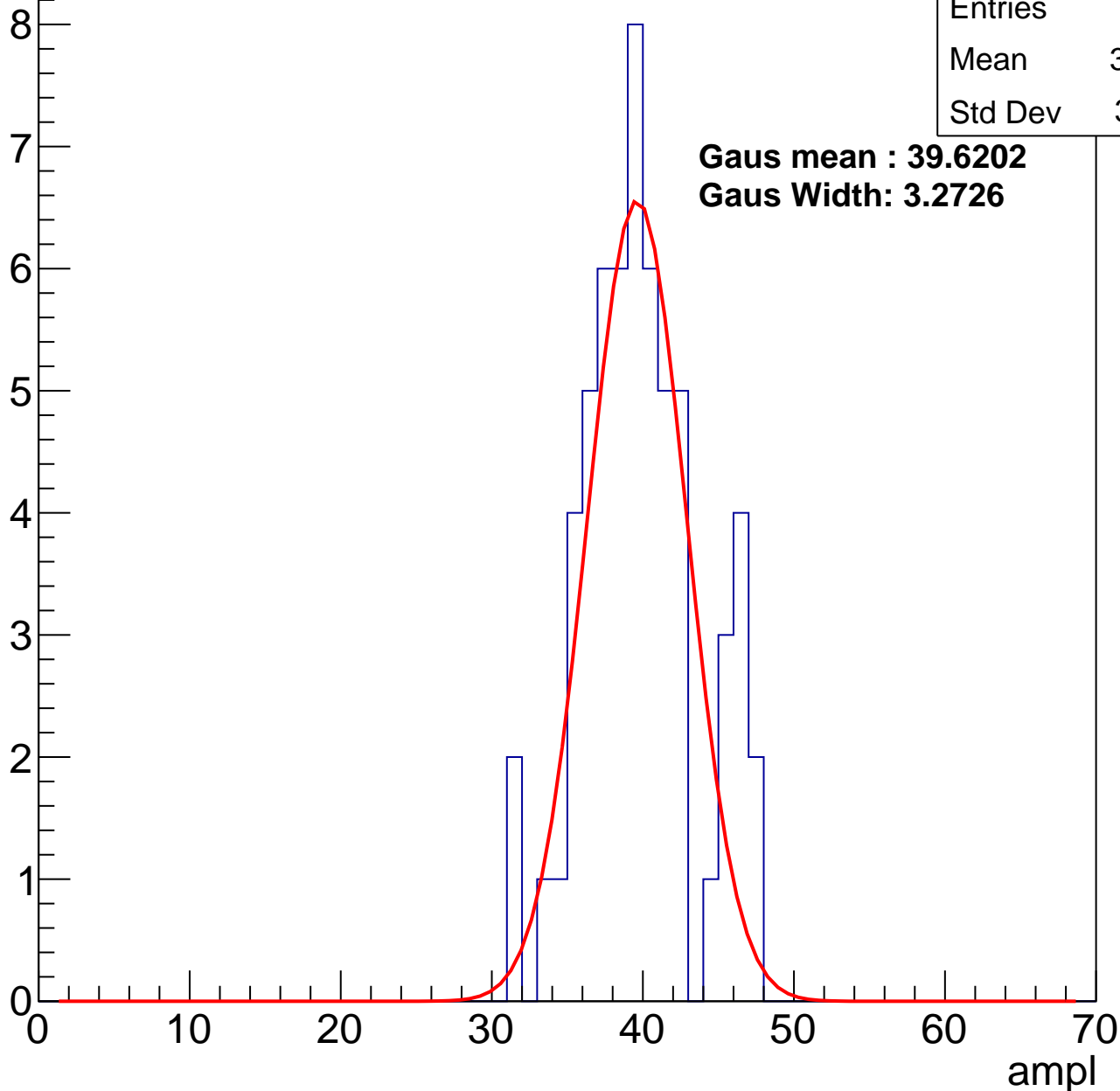
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	39.37
Std Dev	3.791

**Gaus mean : 39.6202**

**Gaus Width: 3.2726**



# B1L103S, U21-ch10, adc2

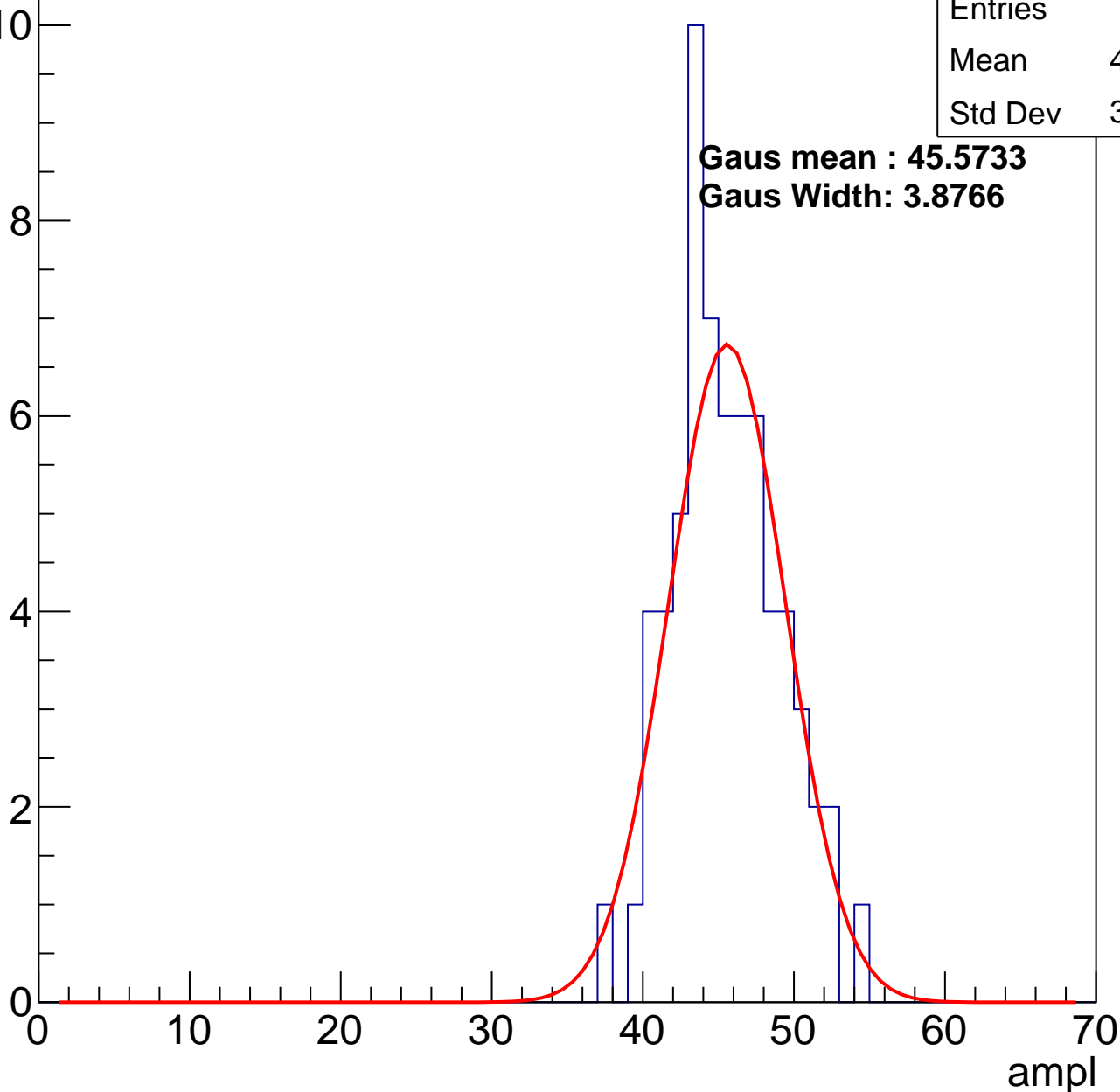
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	45.06
Std Dev	3.507

**Gaus mean : 45.5733**

**Gaus Width: 3.8766**

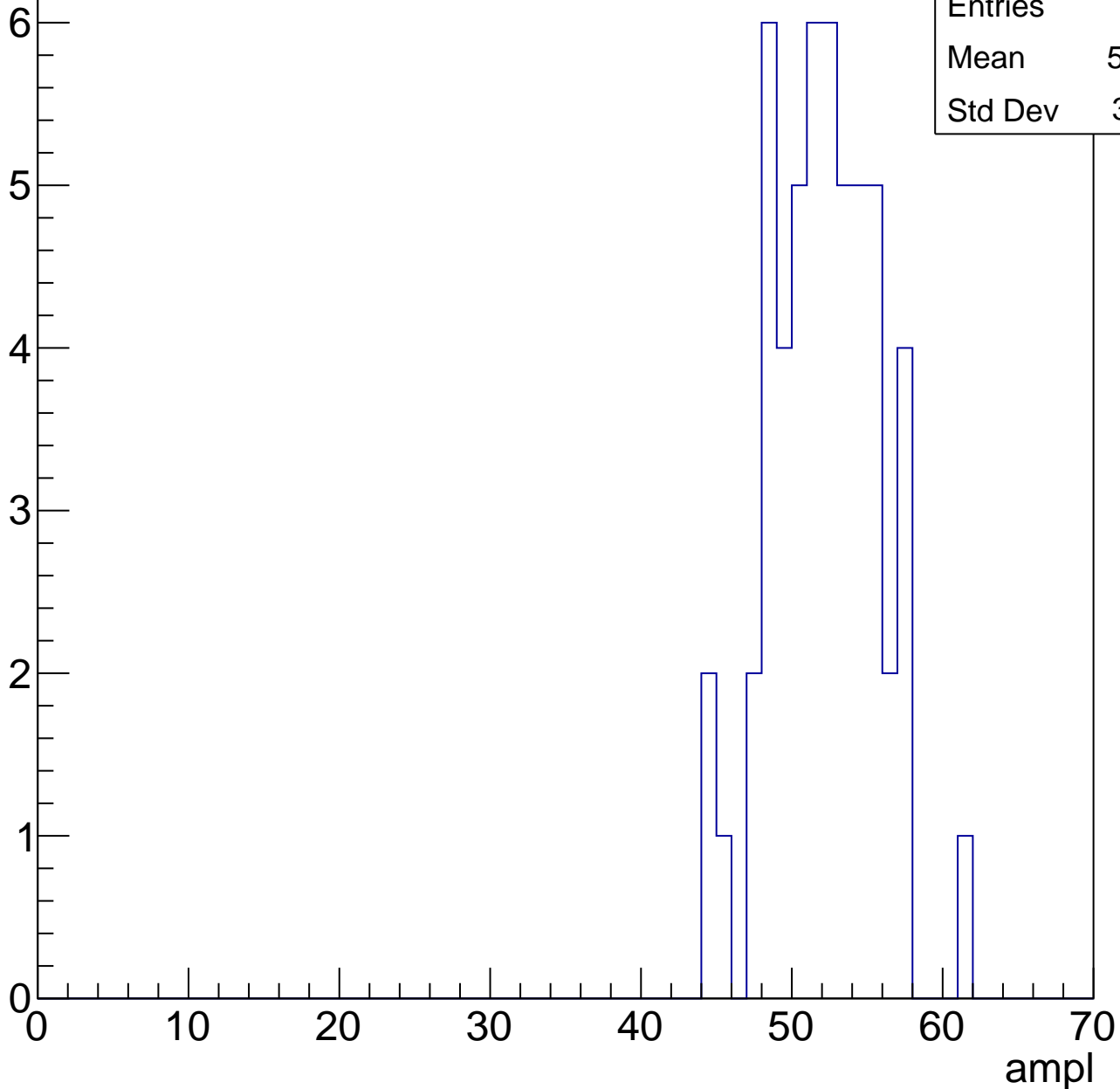


# B1L103S, U21-ch10, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	51.67
Std Dev	3.501

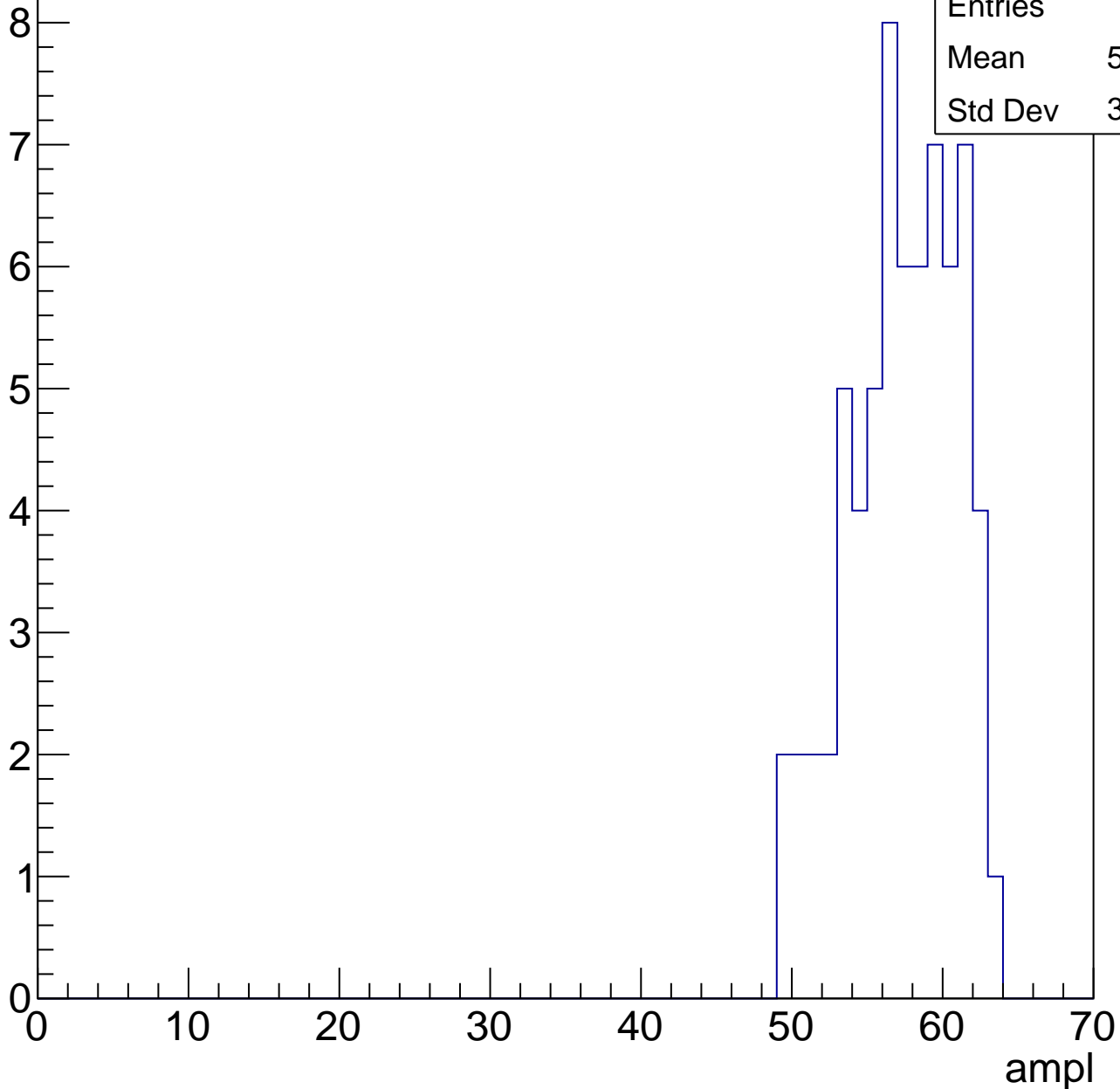


# B1L103S, U21-ch10, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	56.85
Std Dev	3.512

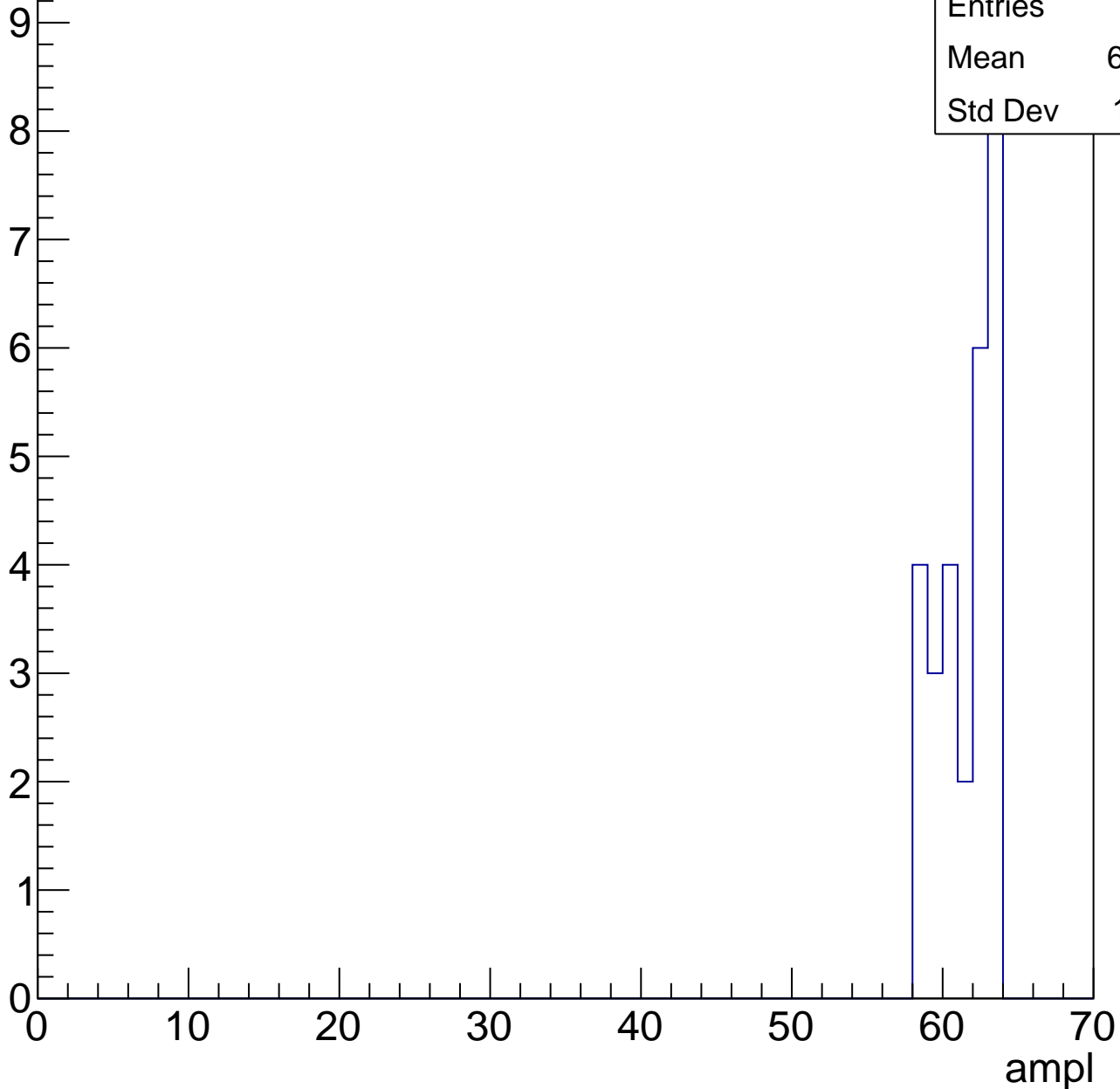


# B1L103S, U21-ch10, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	28
Mean	61.07
Std Dev	1.831



# B1L103S, U21-ch10, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U21-ch10, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U21-ch11, adc0

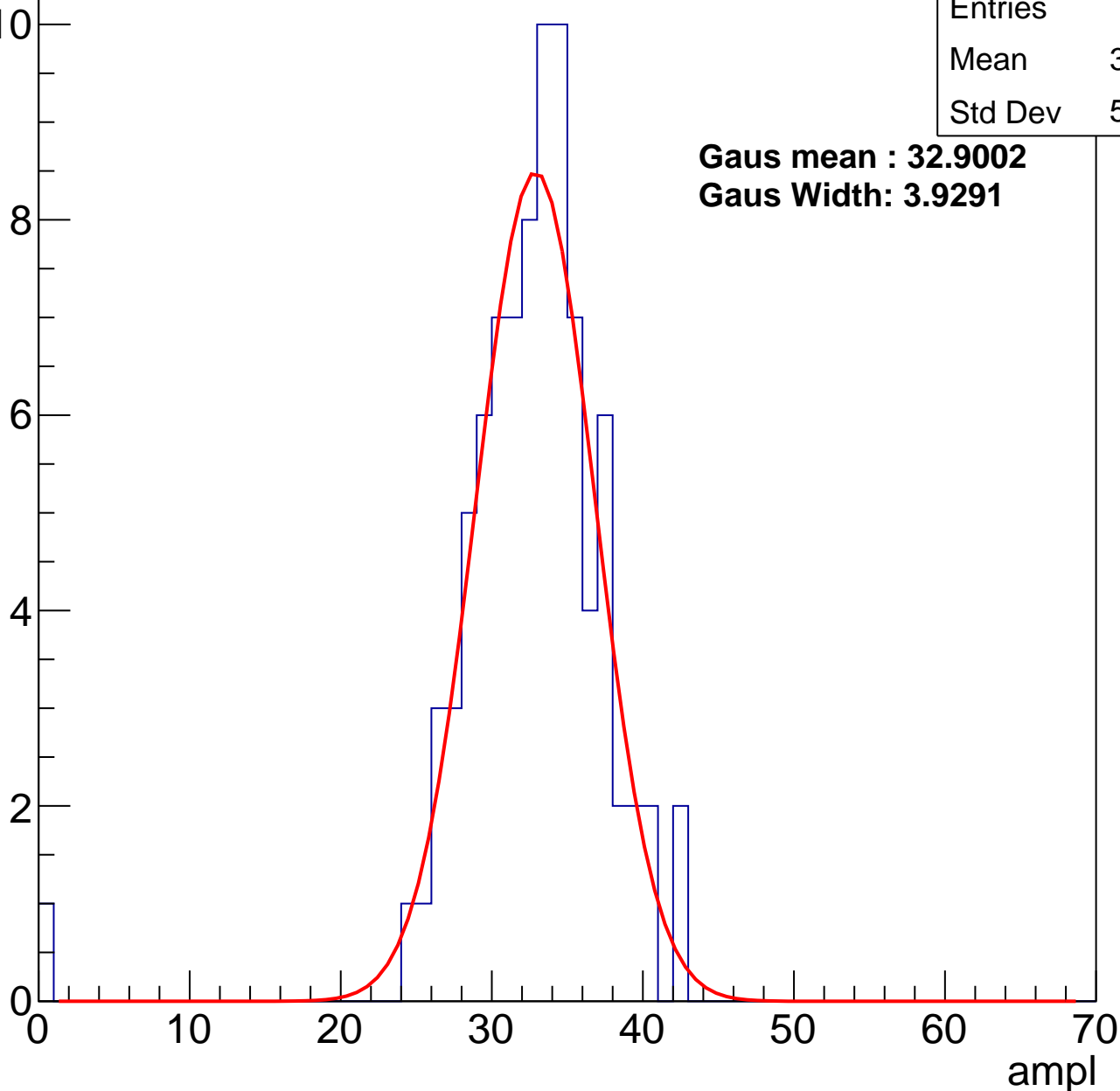
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	87
Mean	32.23
Std Dev	5.152

**Gaus mean : 32.9002**

**Gaus Width: 3.9291**

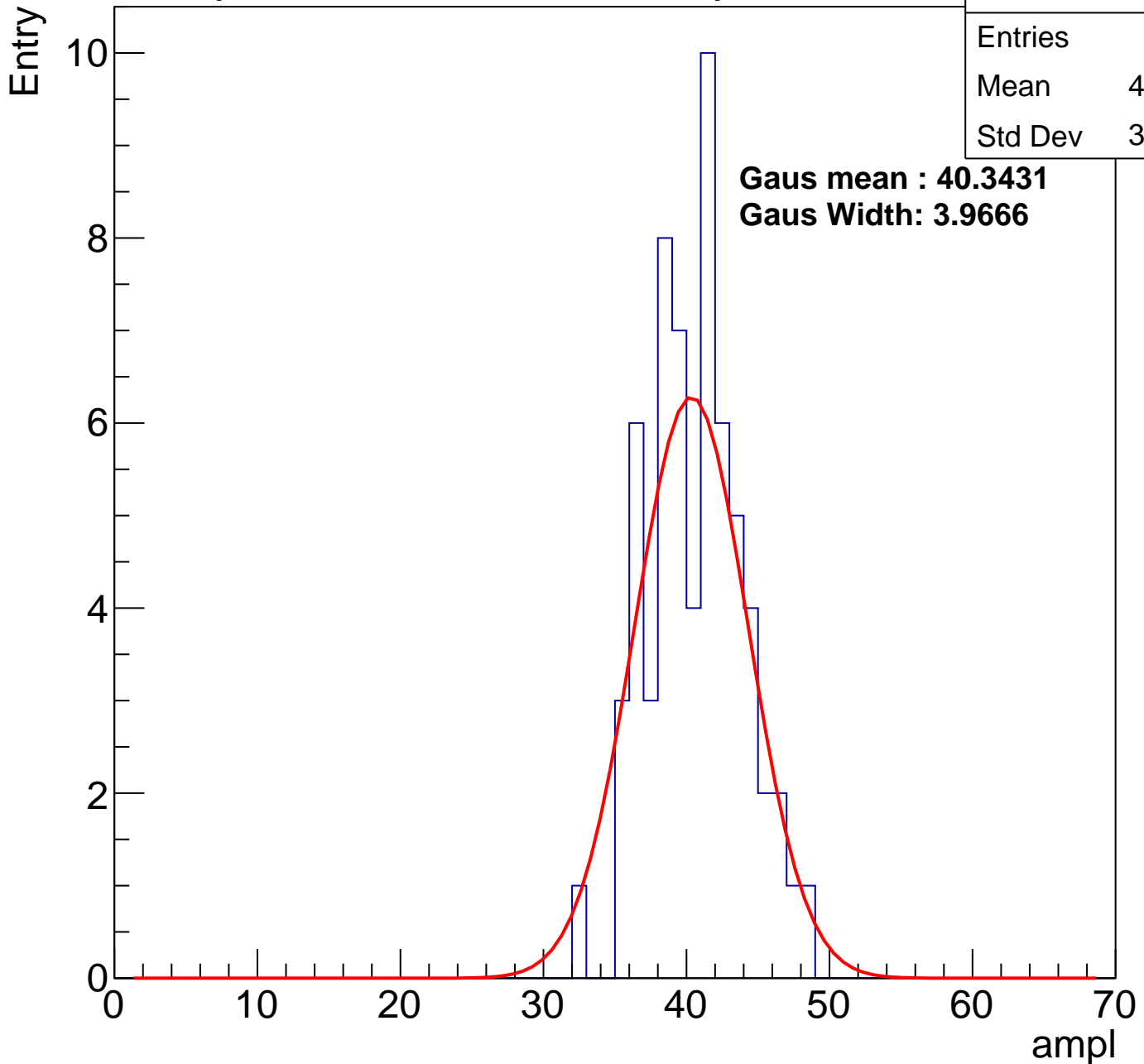


# B1L103S, U21-ch11, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	63
Mean	40.17
Std Dev	3.278

**Gaus mean : 40.3431**  
**Gaus Width: 3.9666**



# B1L103S, U21-ch11, adc2

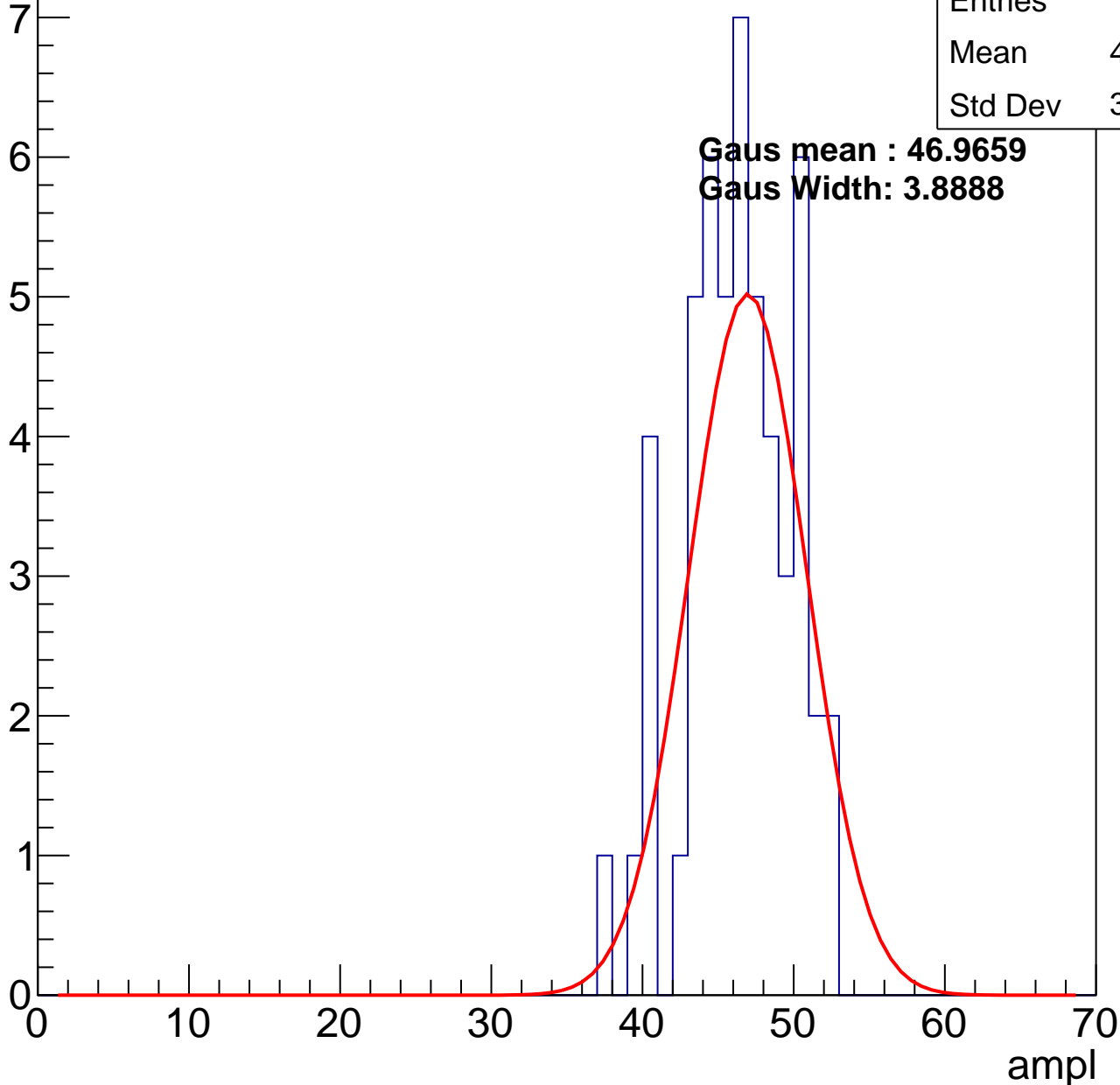
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	45.85
Std Dev	3.477

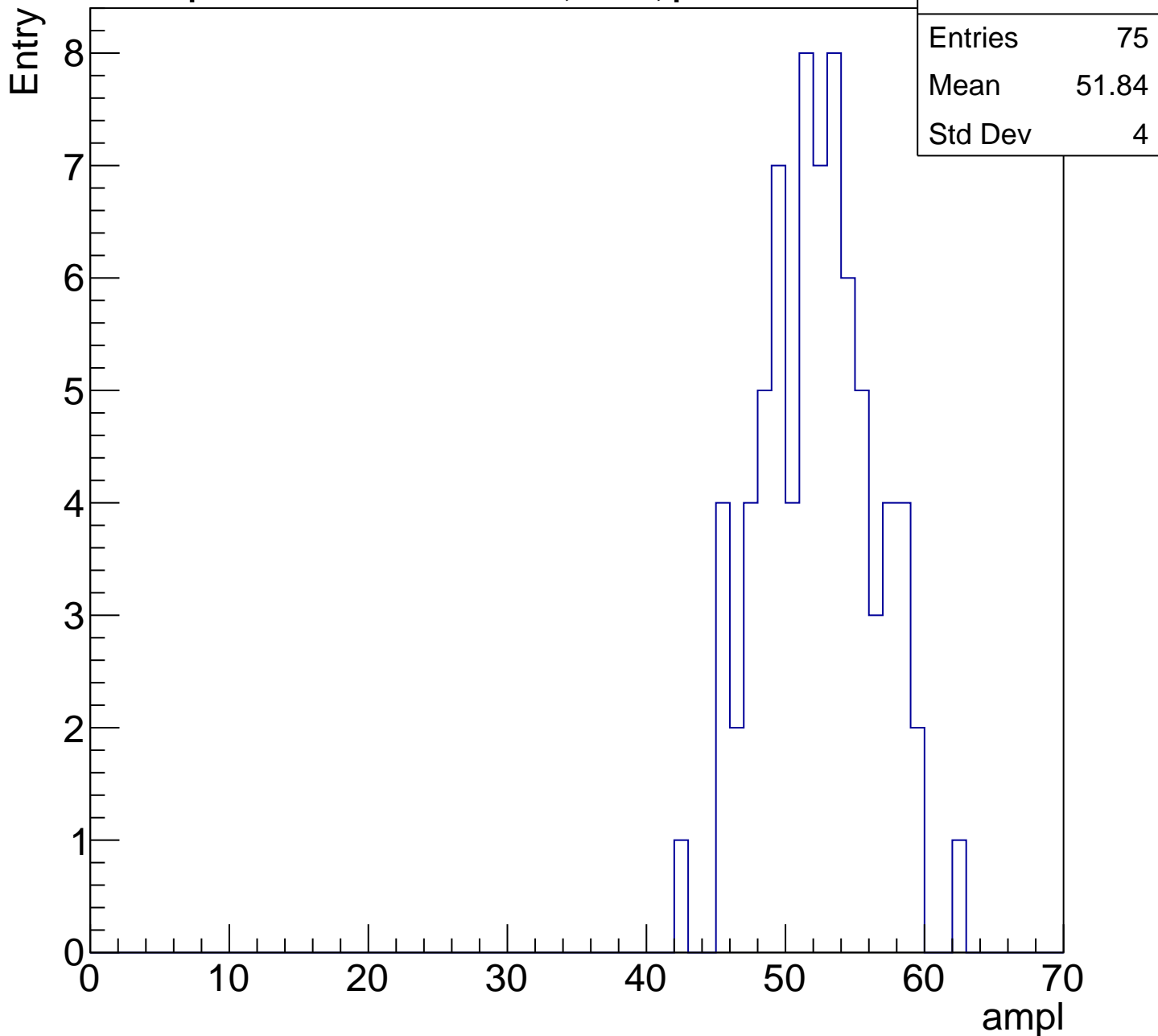
**Gaus mean : 46.9659**

**Gaus Width: 3.8888**



# B1L103S, U21-ch11, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

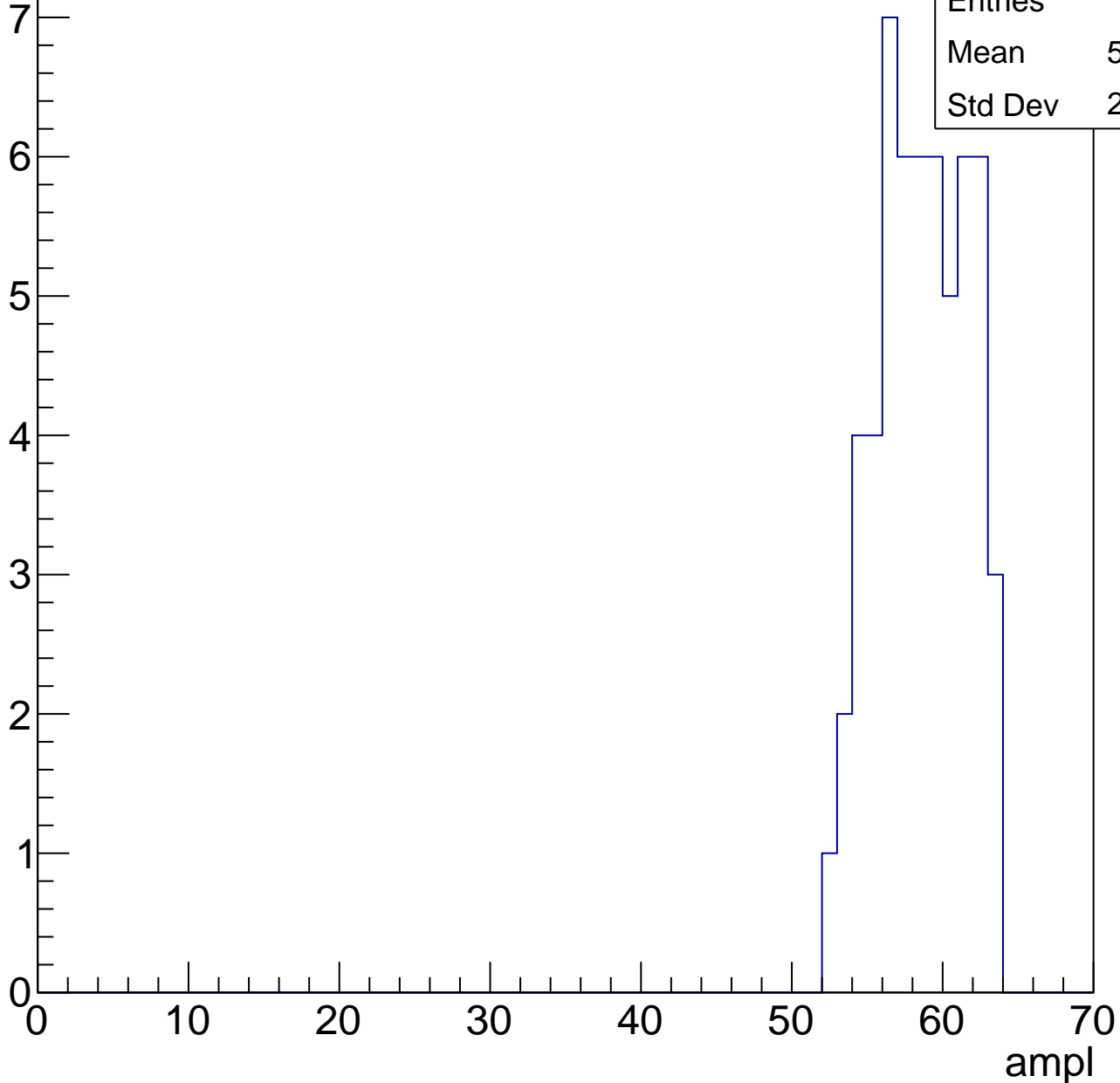


# B1L103S, U21-ch11, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	58.16
Std Dev	2.896

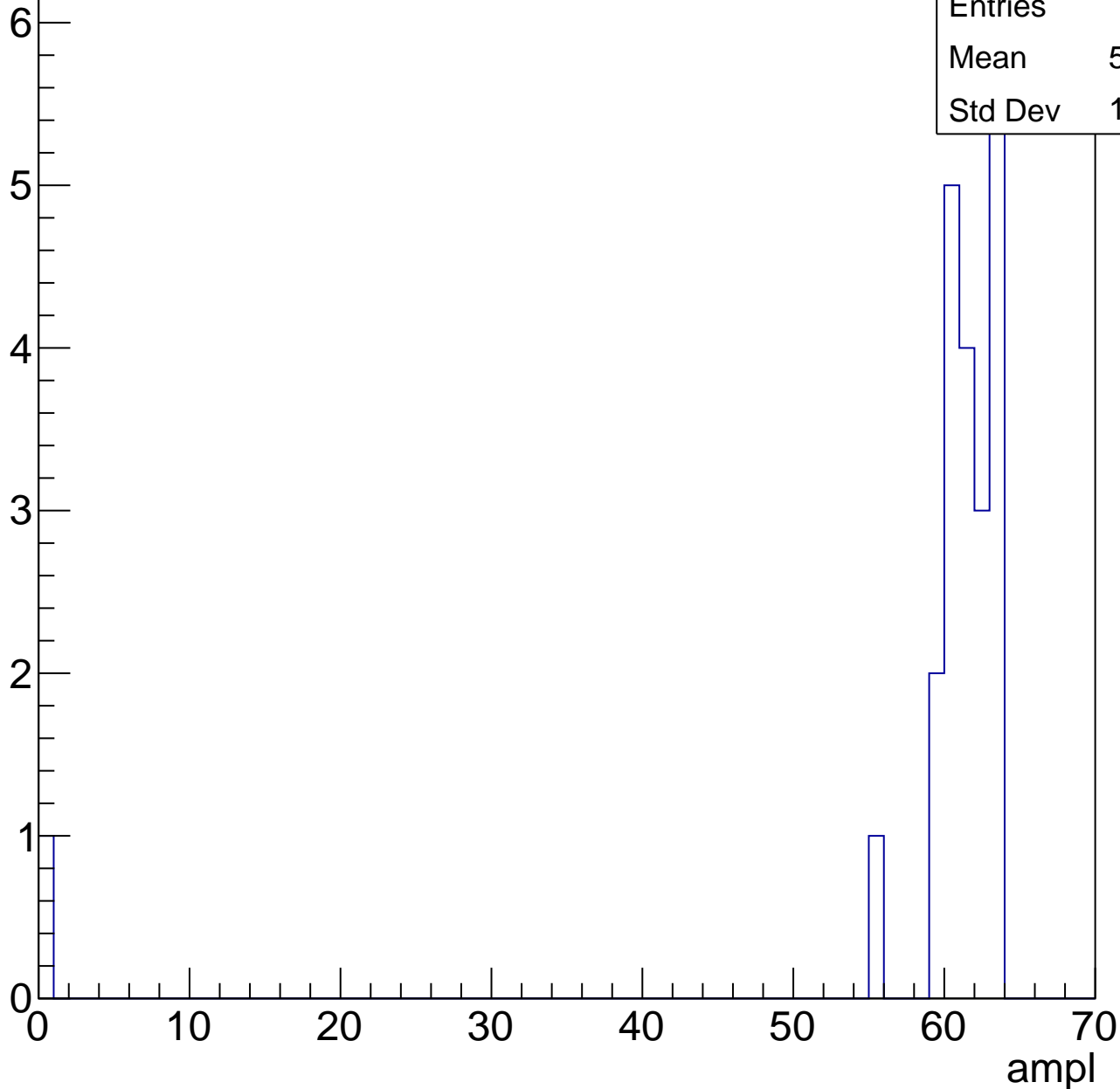


# B1L103S, U21-ch11, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	22
Mean	58.23
Std Dev	12.84



# B1L103S, U21-ch11, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	63
Std Dev	0



# B1L103S, U21-ch11, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U21-ch12, adc0

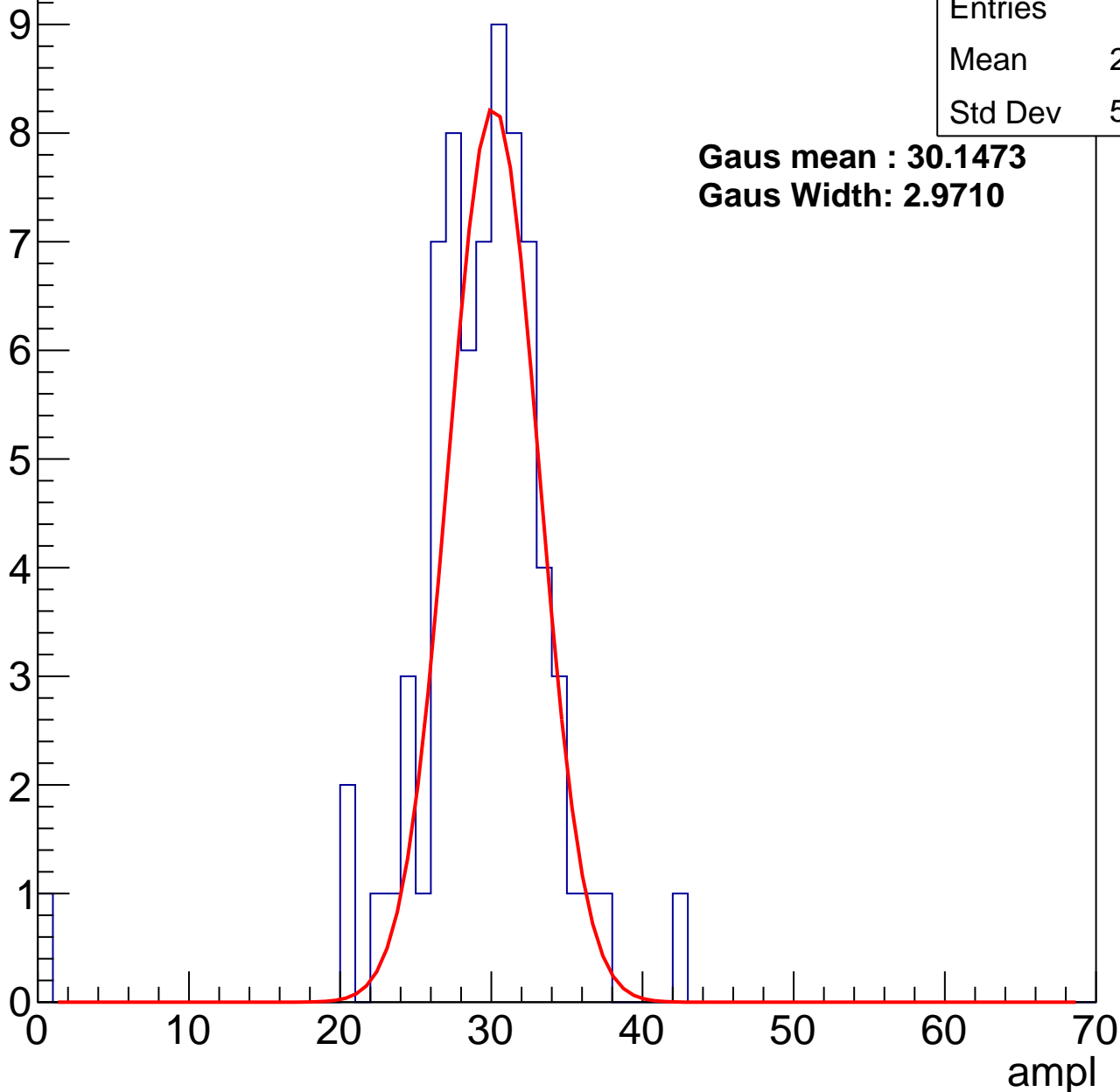
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	28.85
Std Dev	5.054

**Gaus mean : 30.1473**

**Gaus Width: 2.9710**



# B1L103S, U21-ch12, adc1

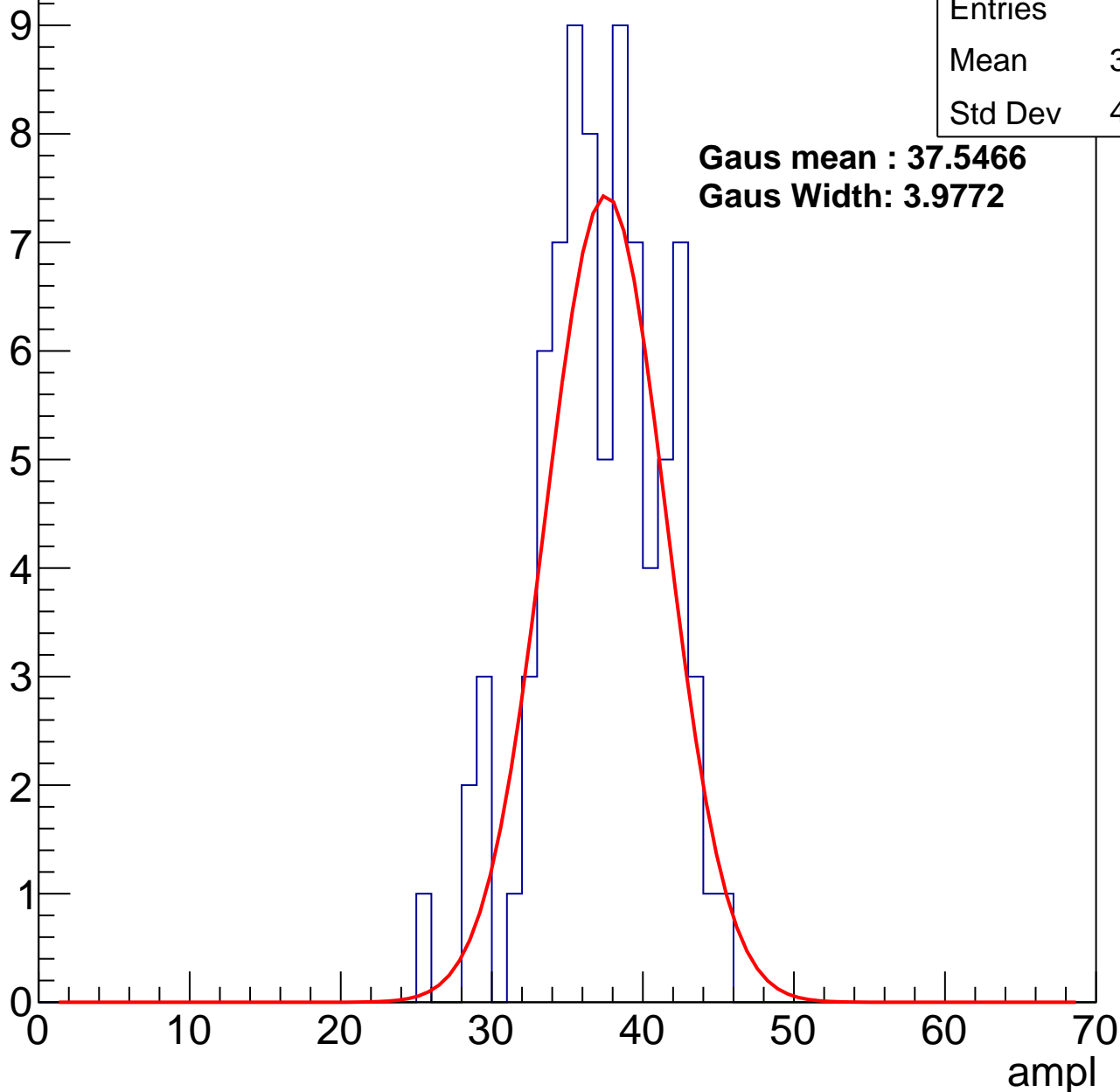
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	82
Mean	36.72
Std Dev	4.064

**Gaus mean : 37.5466**

**Gaus Width: 3.9772**



# B1L103S, U21-ch12, adc2

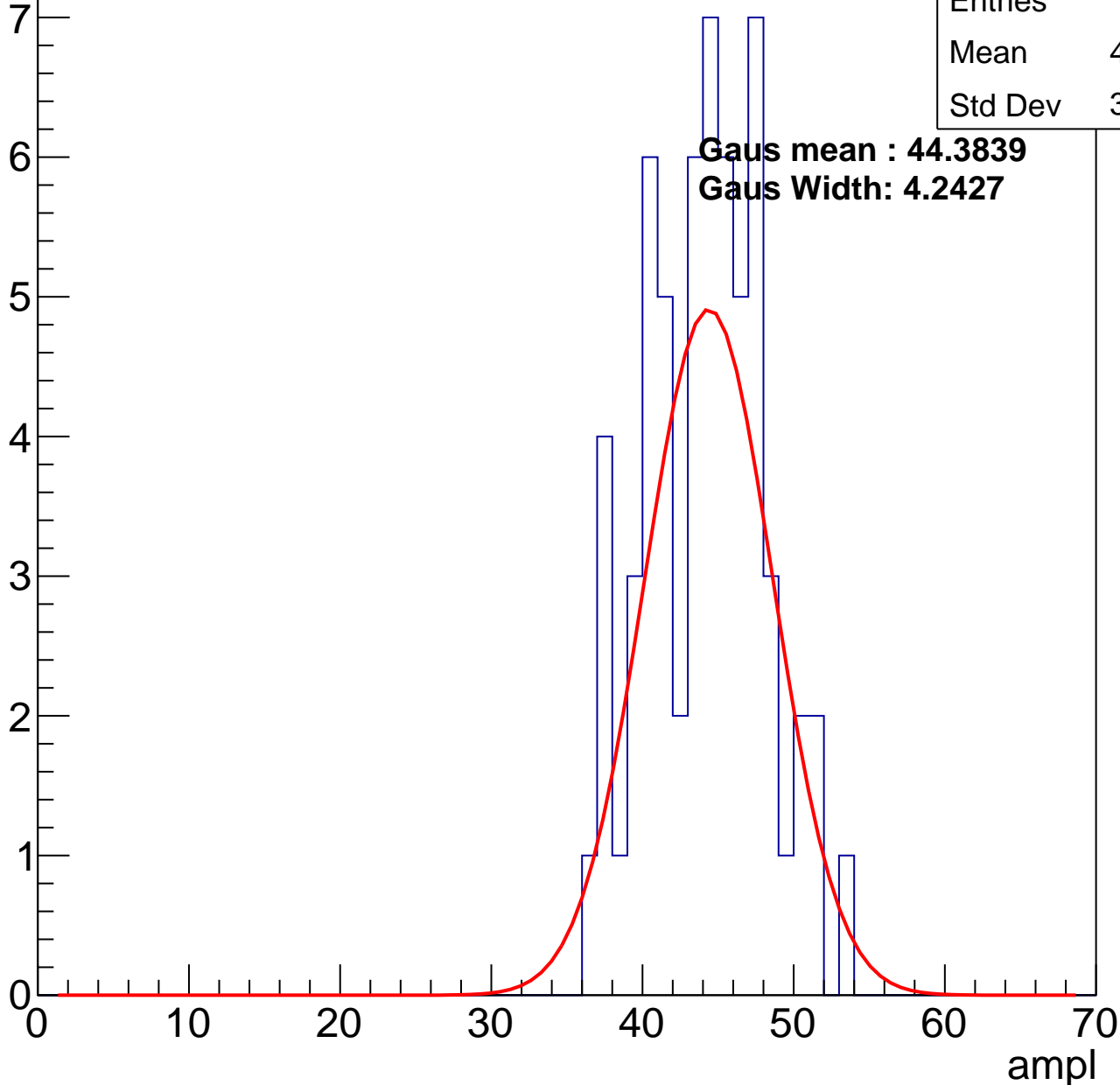
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	43.73
Std Dev	3.882

**Gaus mean : 44.3839**

**Gaus Width: 4.2427**

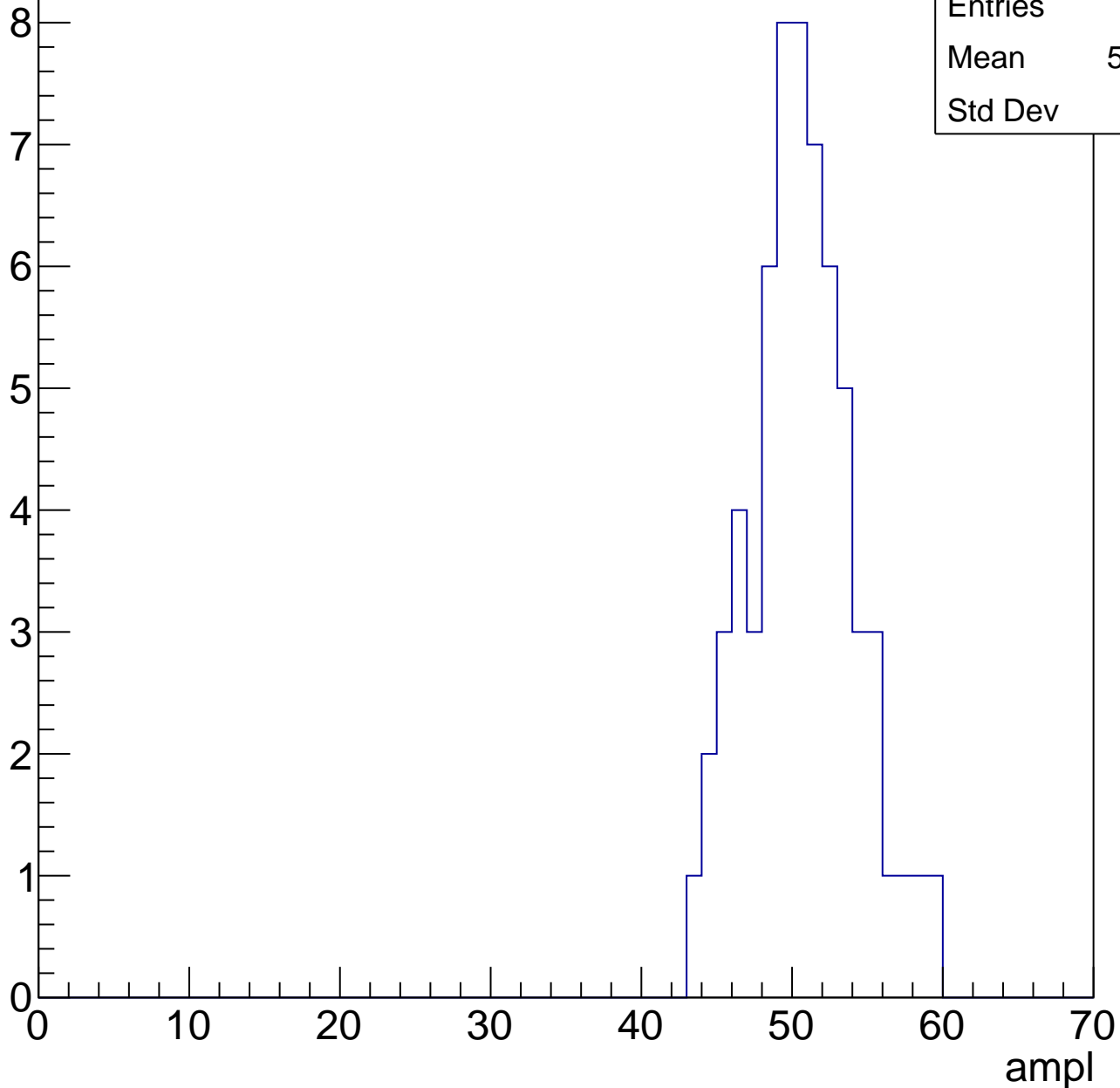


# B1L103S, U21-ch12, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	50.19
Std Dev	3.44

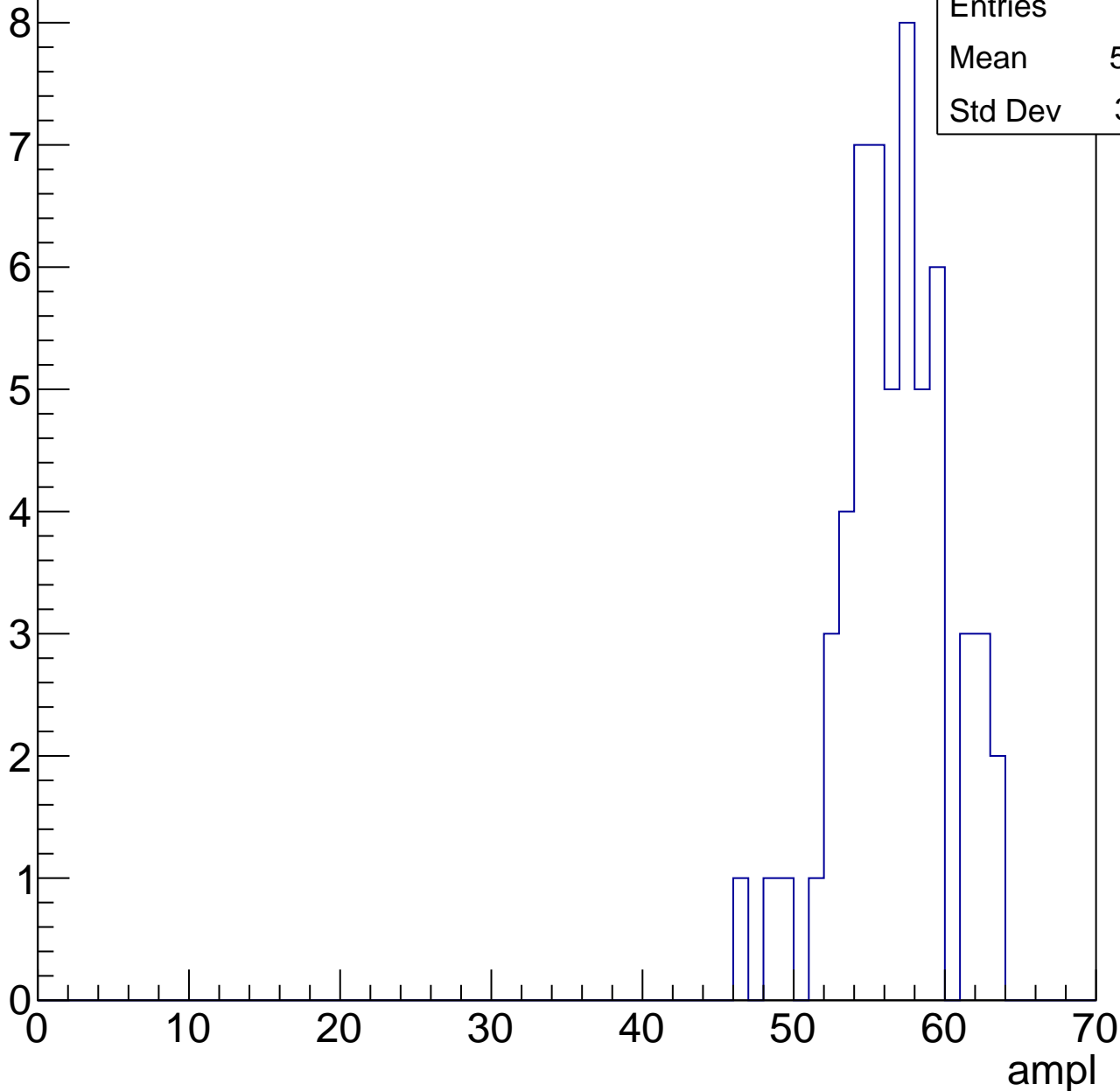


# B1L103S, U21-ch12, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	56.14
Std Dev	3.551

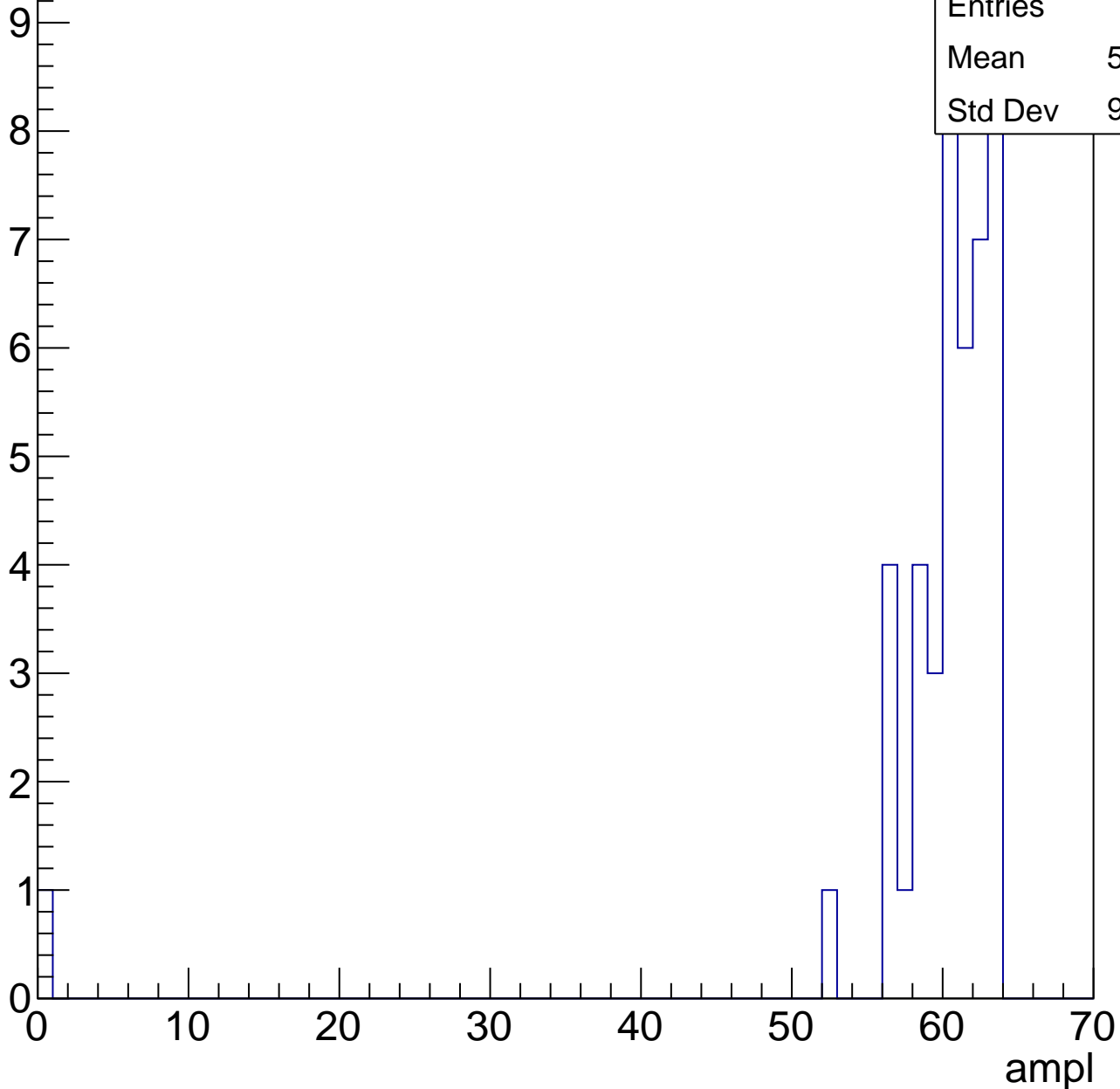


# B1L103S, U21-ch12, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

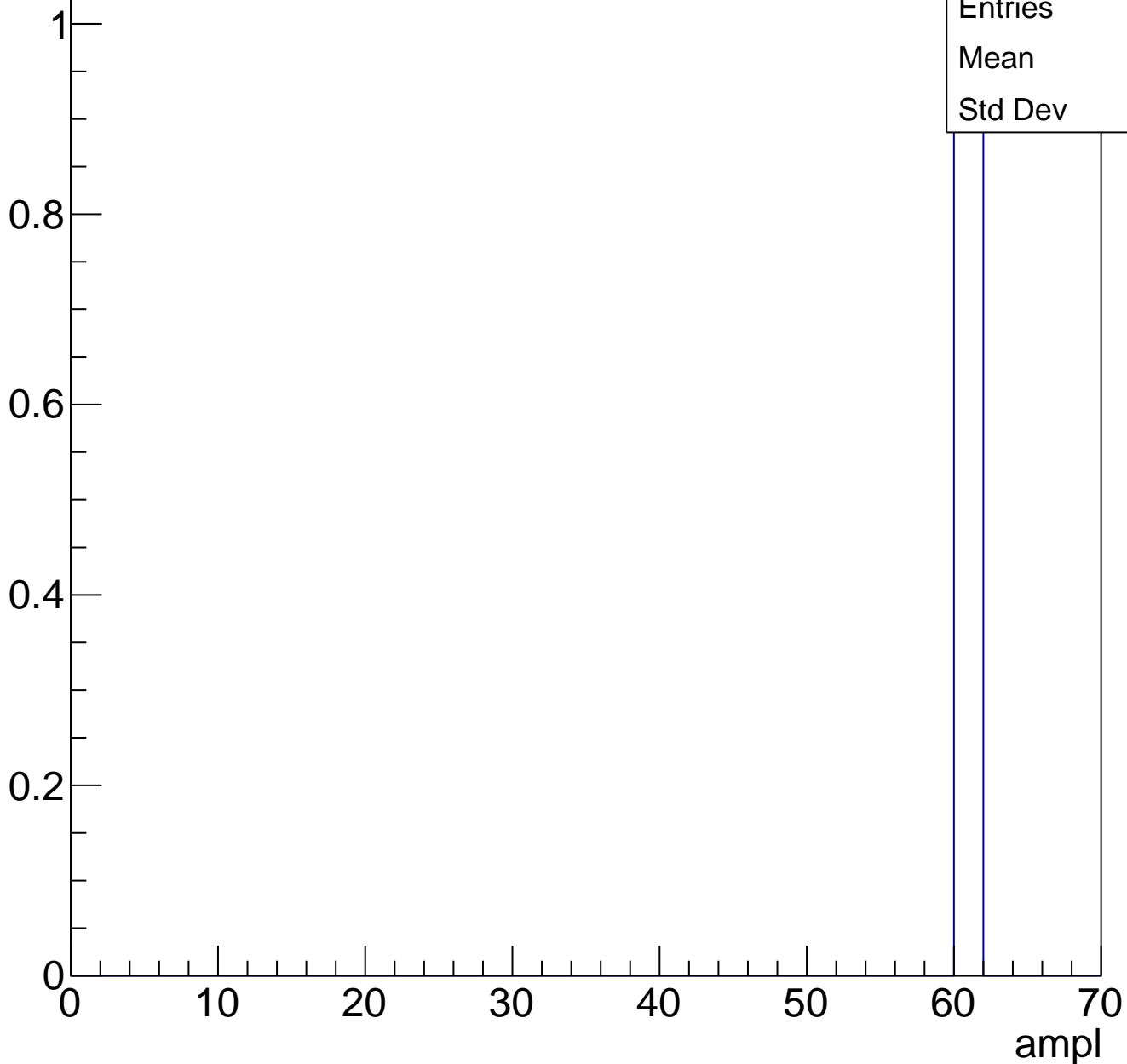
Entries	44
Mean	58.77
Std Dev	9.288



# B1L103S, U21-ch12, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U21-ch12, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	20
Std Dev	0

# B1L103S, U21-ch13, adc0

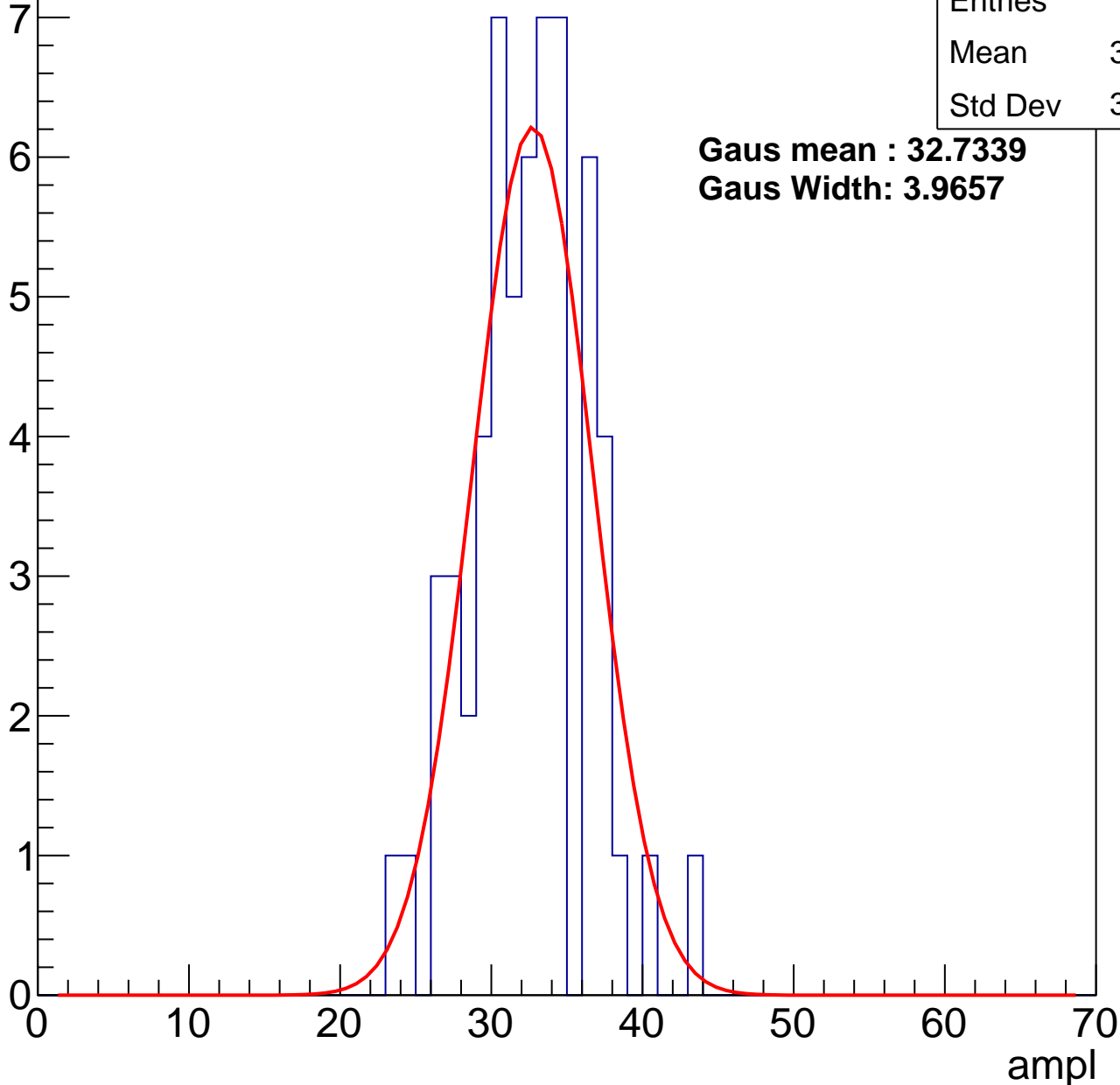
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	32.02
Std Dev	3.864

**Gaus mean : 32.7339**

**Gaus Width: 3.9657**



# B1L103S, U21-ch13, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	67
Mean	37.91
Std Dev	3.467

**Gaus mean : 37.9563**

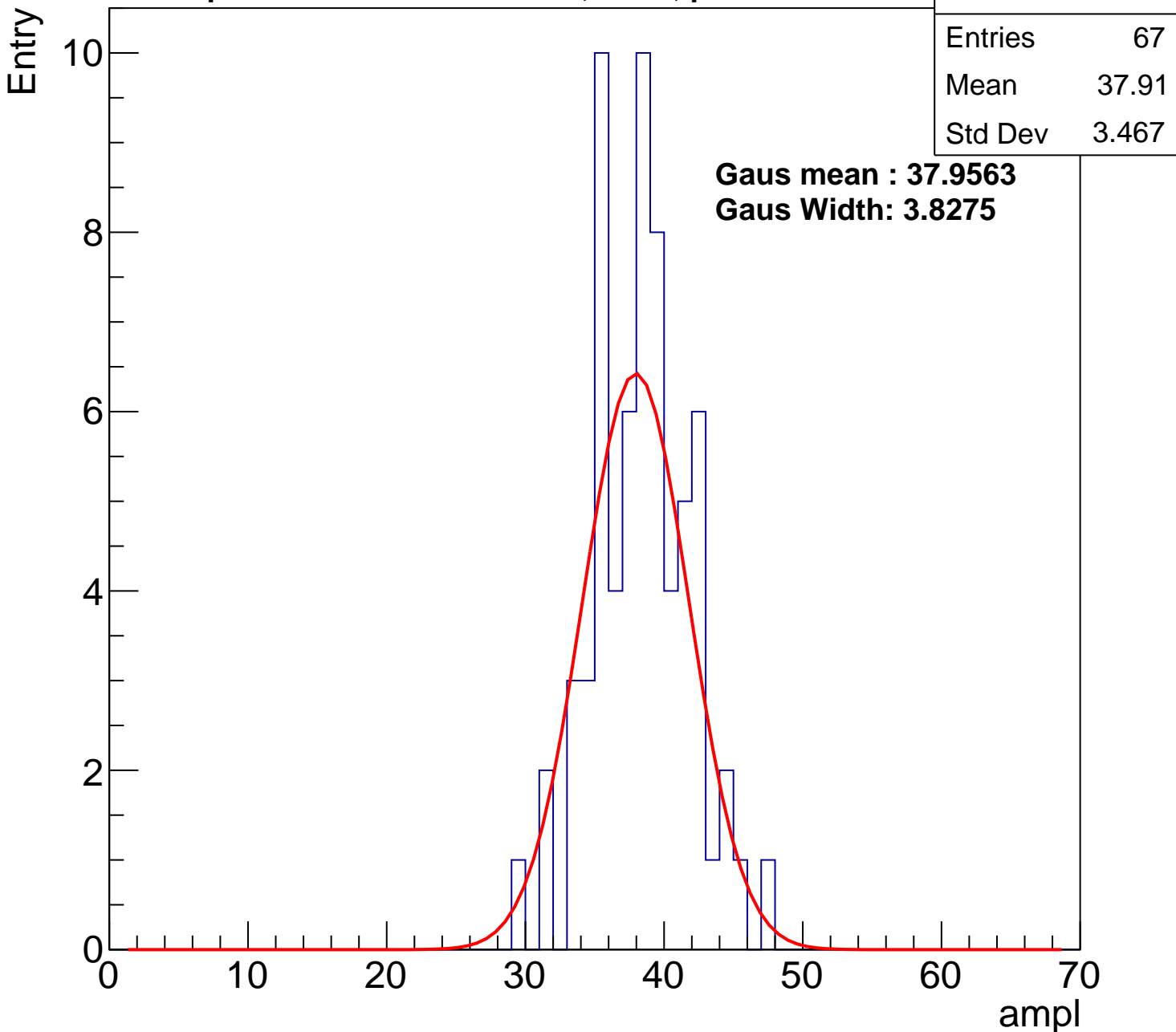
**Gaus Width: 3.8275**

Entry

10  
8  
6  
4  
2  
0

ampl

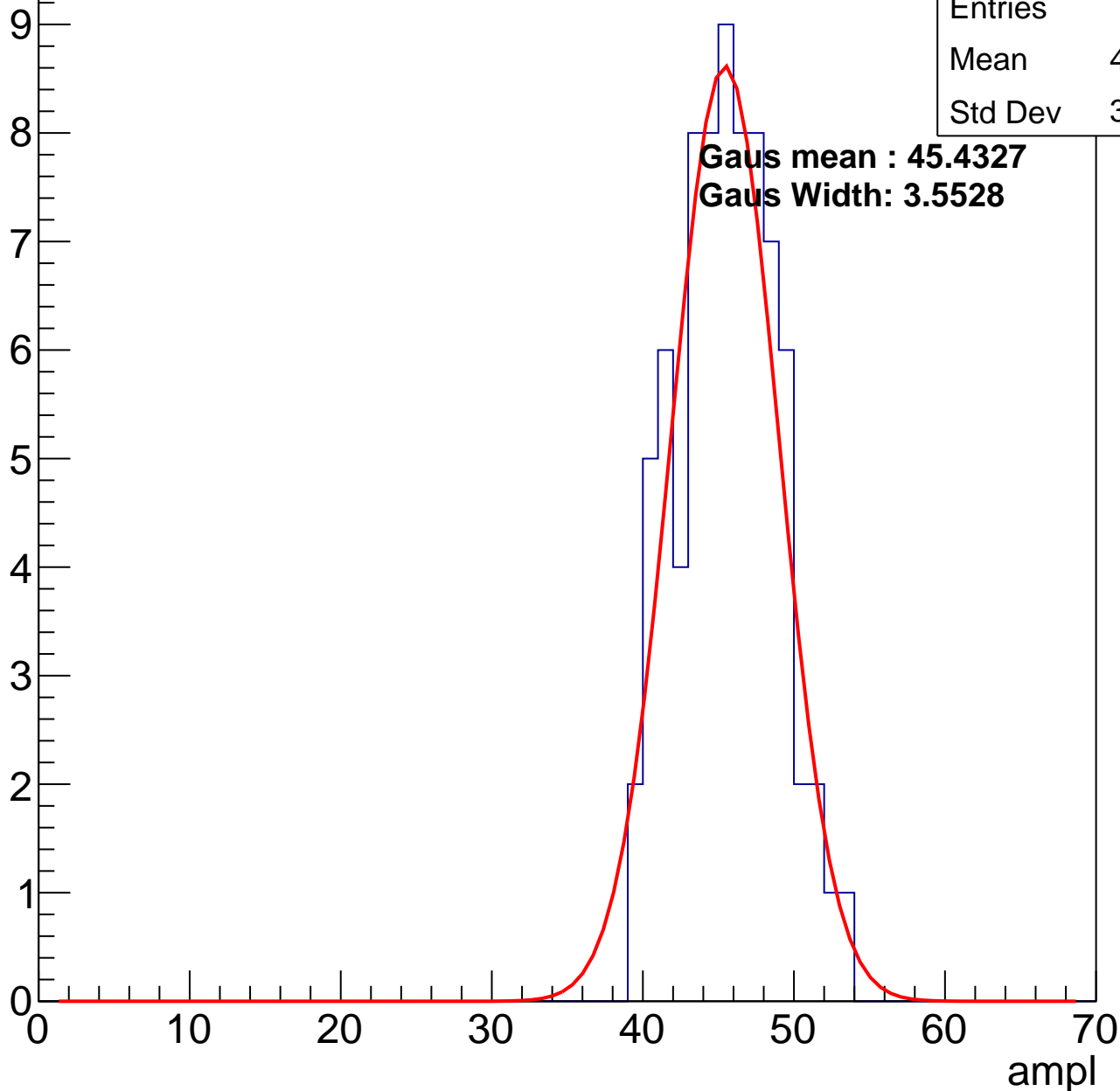
0 10 20 30 40 50 60 70



# B1L103S, U21-ch13, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	77
Mean	45.12
Std Dev	3.227

**Gaus mean : 45.4327**

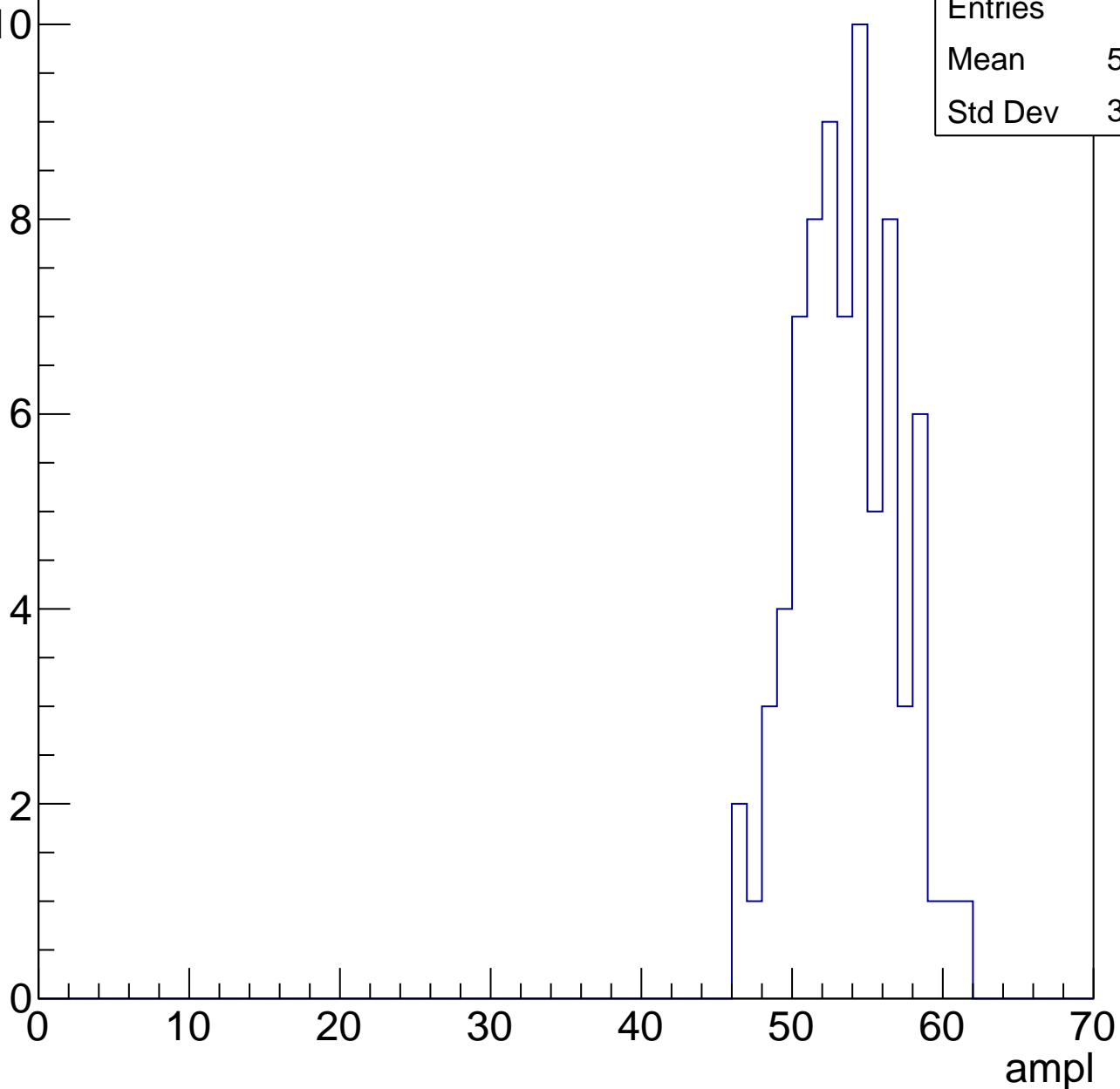
**Gaus Width: 3.5528**

# B1L103S, U21-ch13, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	53.13
Std Dev	3.294

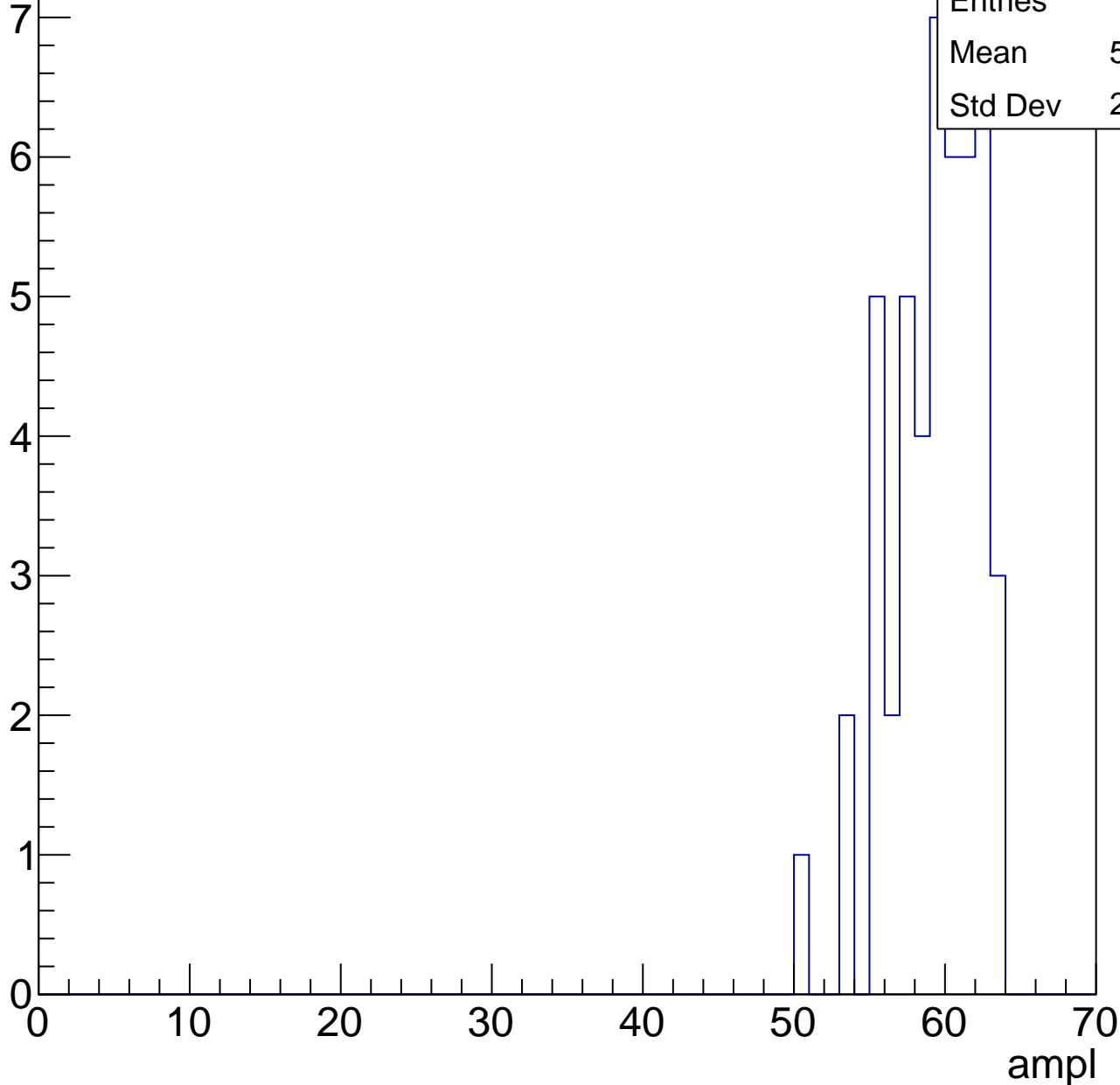


# B1L103S, U21-ch13, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	48
Mean	58.79
Std Dev	2.937

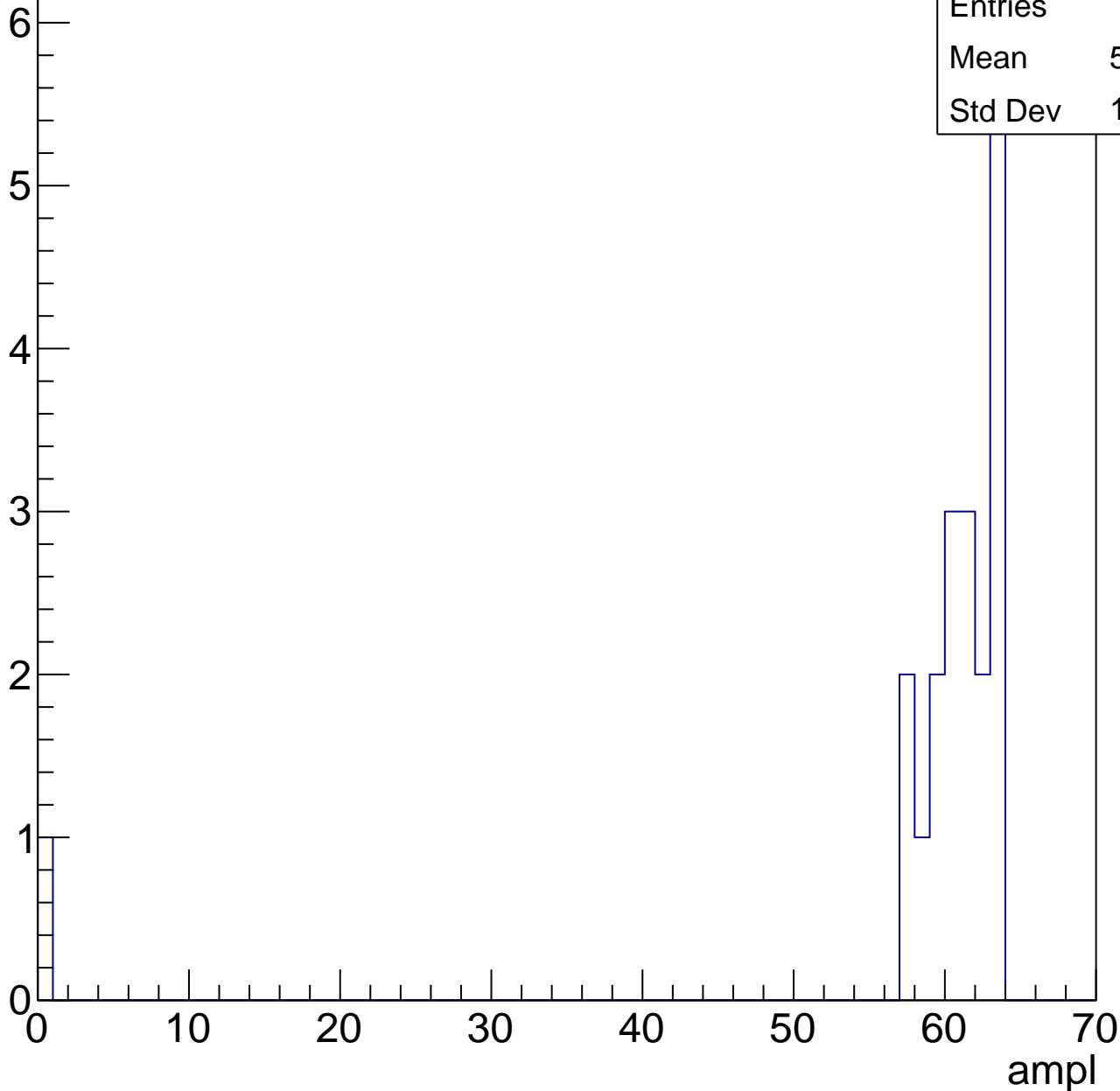


# B1L103S, U21-ch13, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	20
Mean	57.75
Std Dev	13.39



# B1L103S, U21-ch13, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U21-ch13, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U21-ch14, adc0

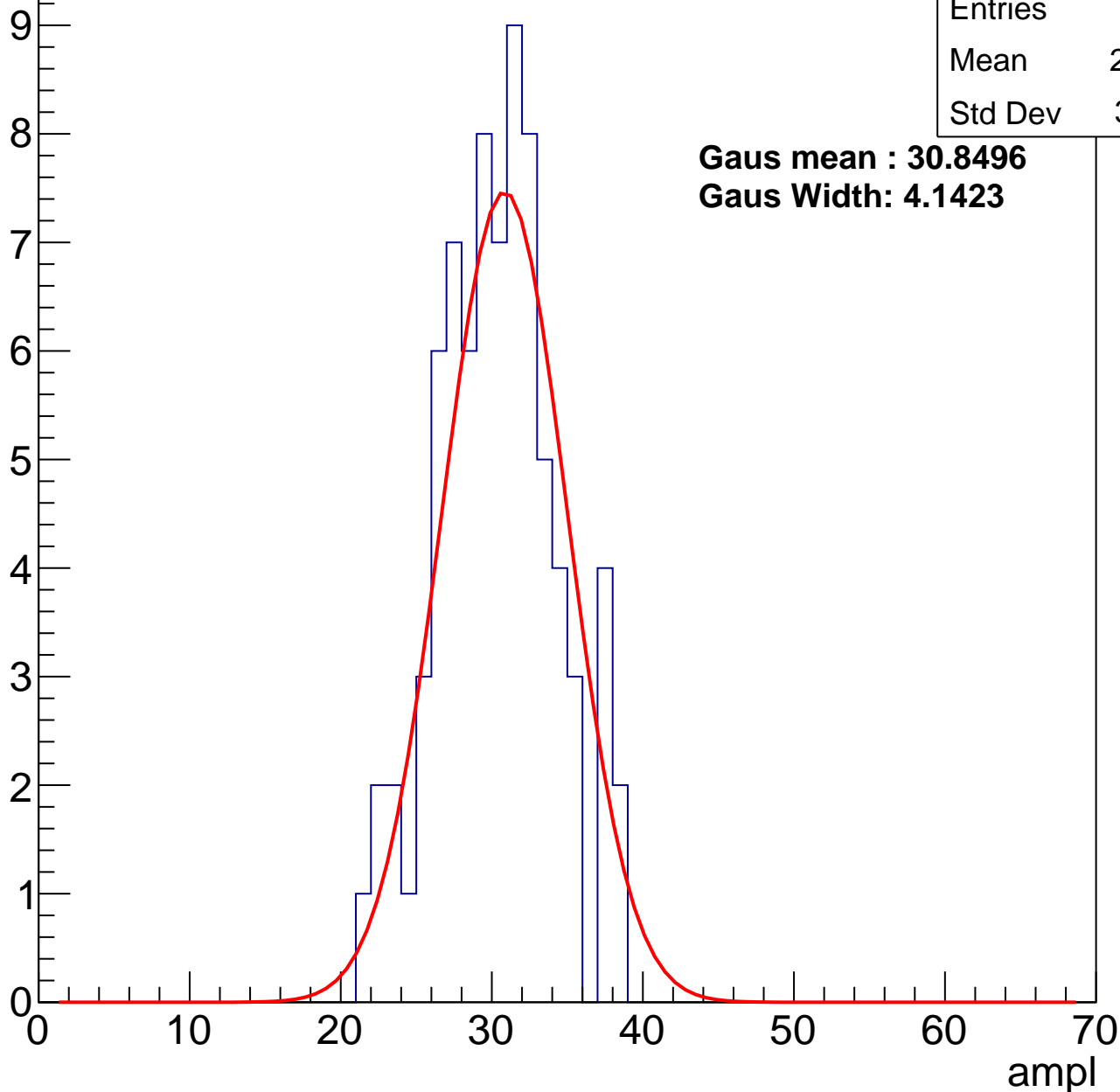
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	29.87
Std Dev	3.851

**Gaus mean : 30.8496**

**Gaus Width: 4.1423**



# B1L103S, U21-ch14, adc1

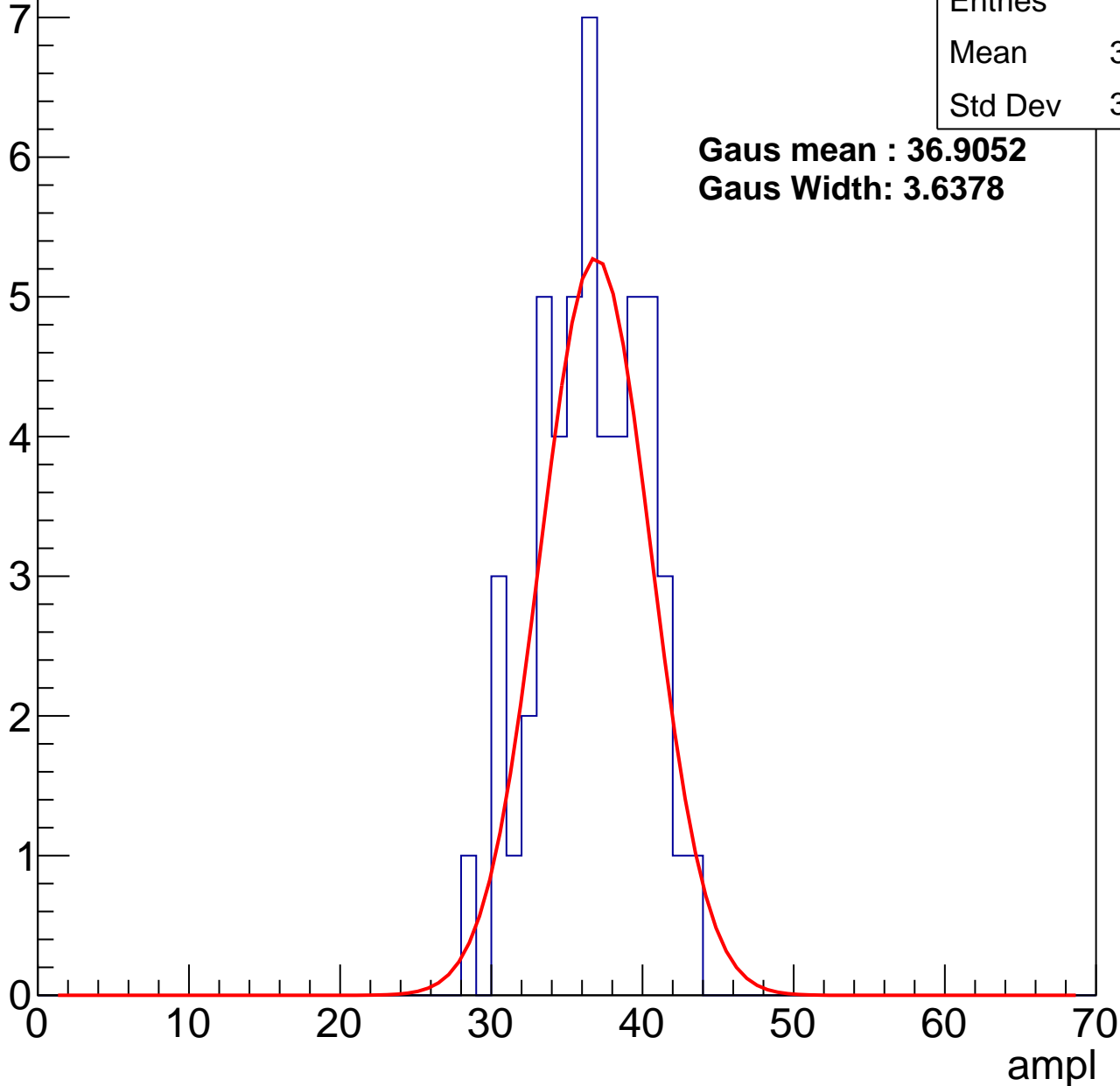
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	36.16
Std Dev	3.426

**Gaus mean : 36.9052**

**Gaus Width: 3.6378**



# B1L103S, U21-ch14, adc2

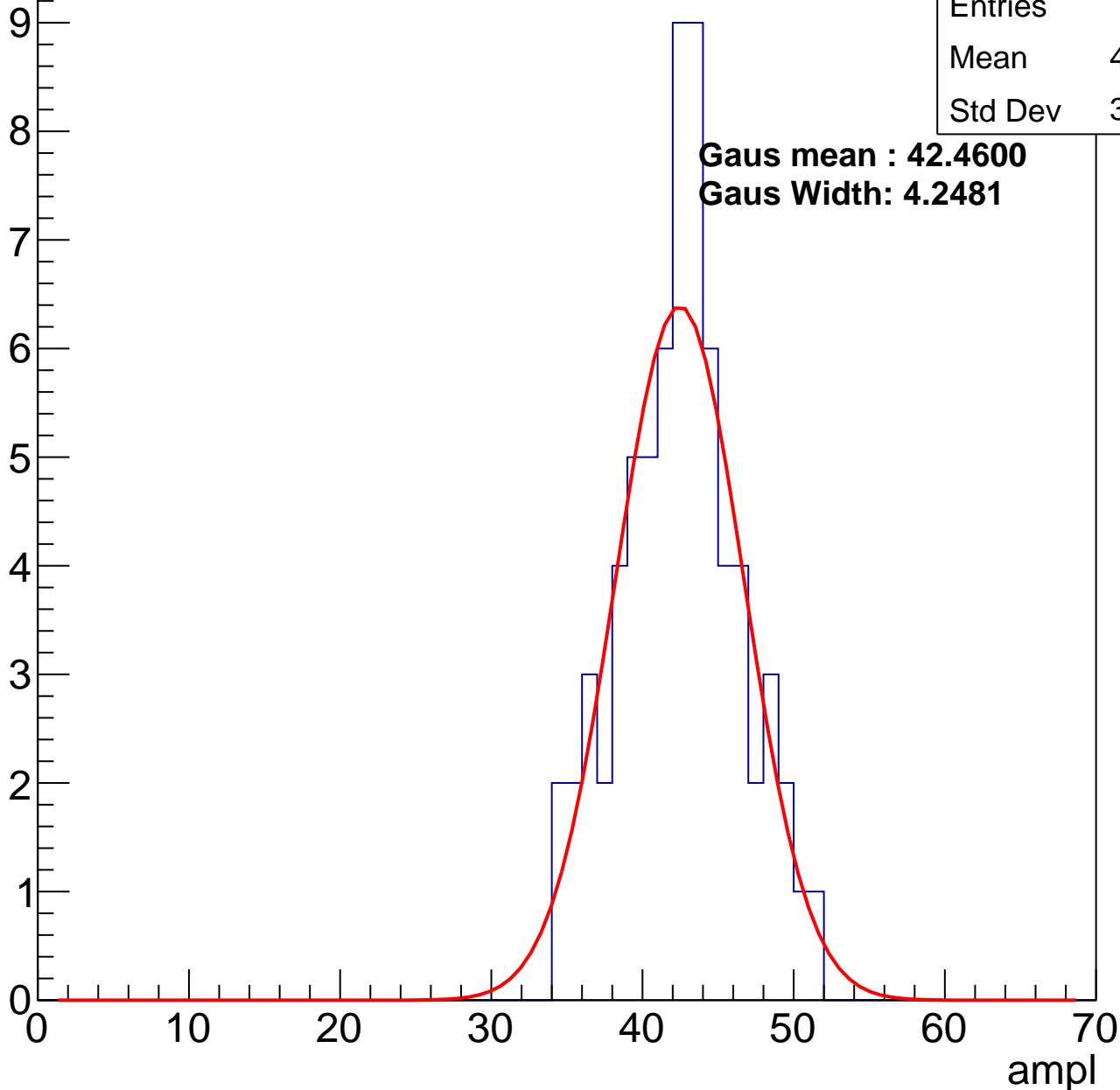
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	42.04
Std Dev	3.878

**Gaus mean : 42.4600**

**Gaus Width: 4.2481**

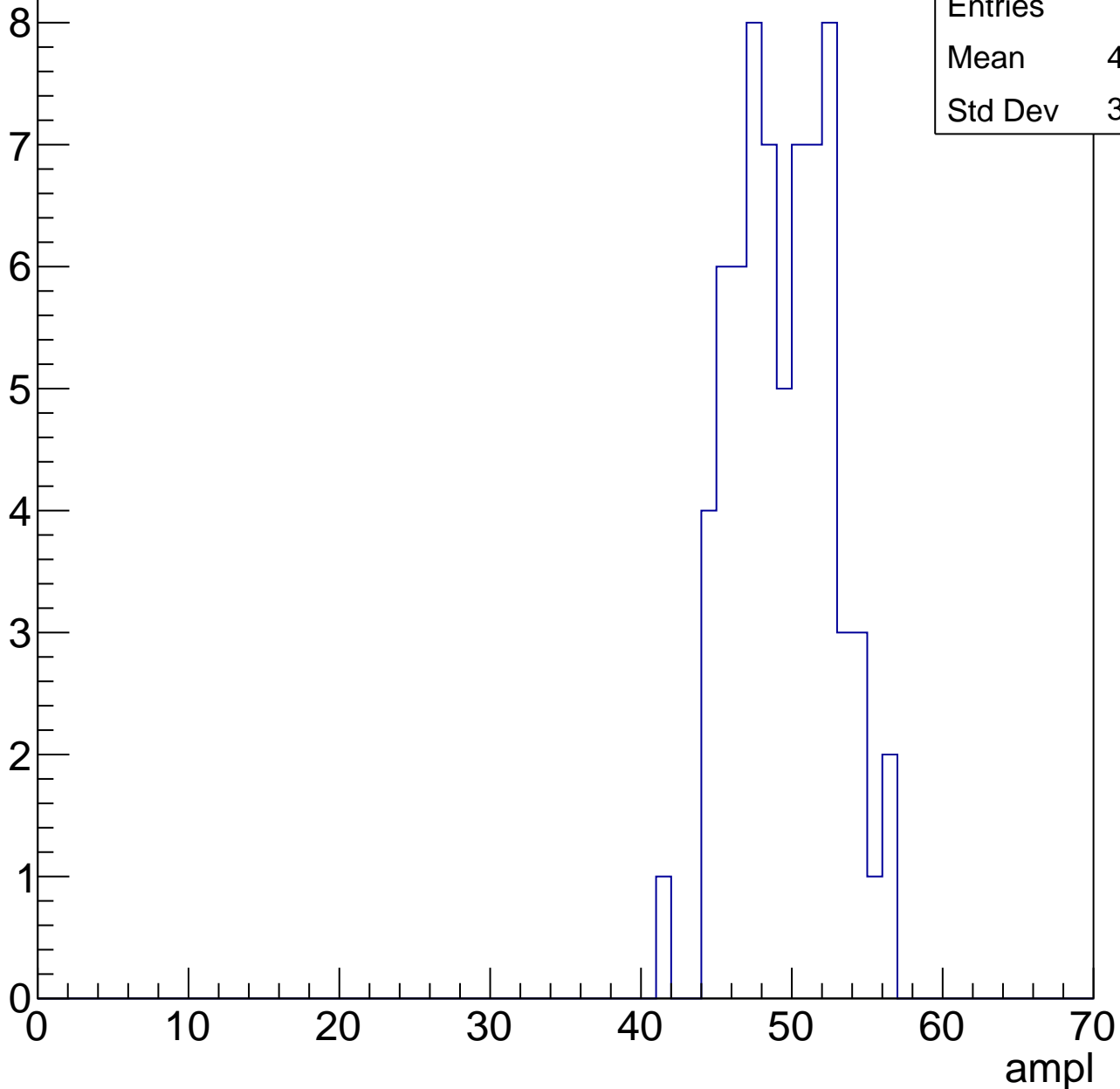


# B1L103S, U21-ch14, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	48.99
Std Dev	3.247

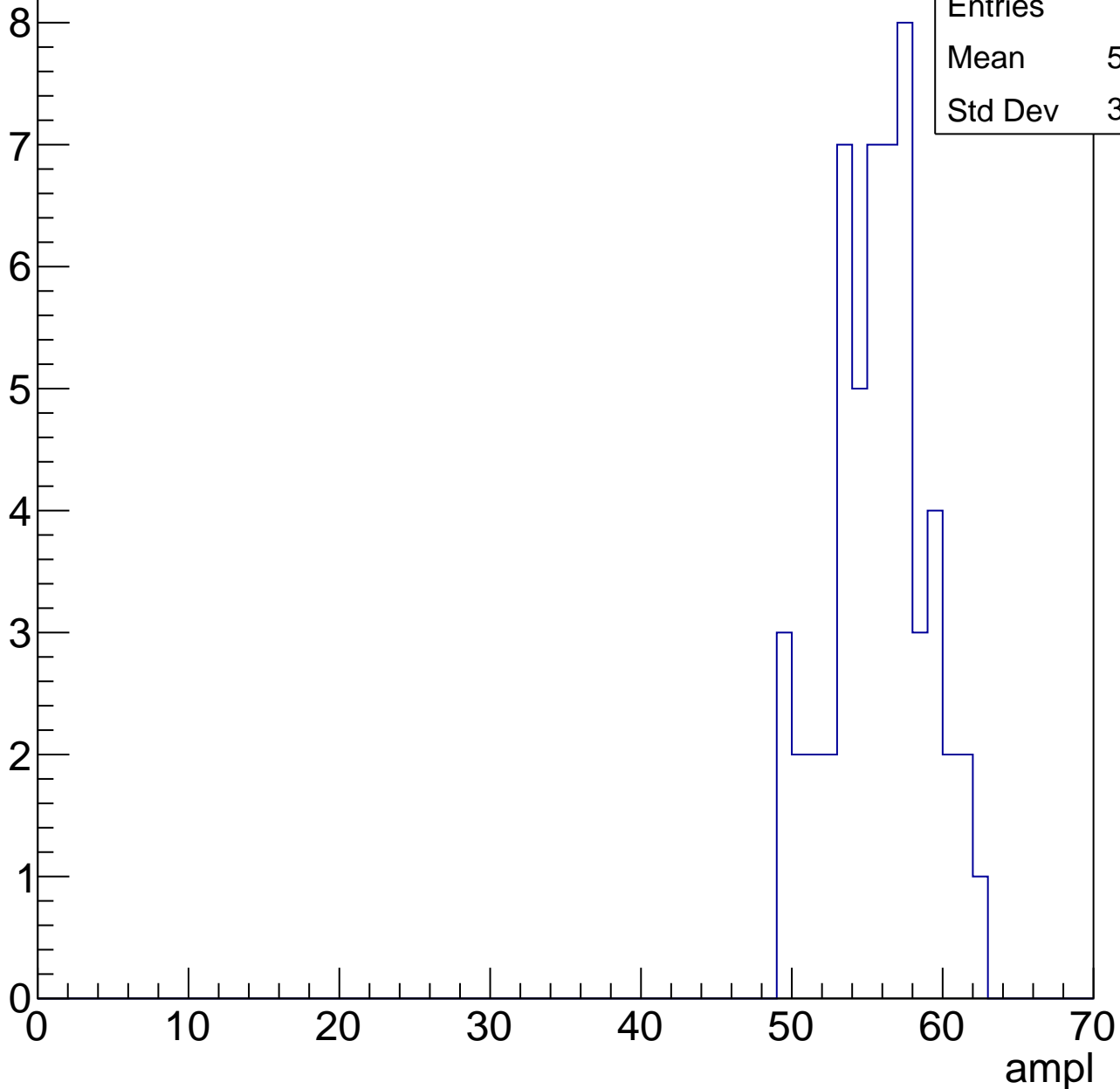


# B1L103S, U21-ch14, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	55.29
Std Dev	3.126



# B1L103S, U21-ch14, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

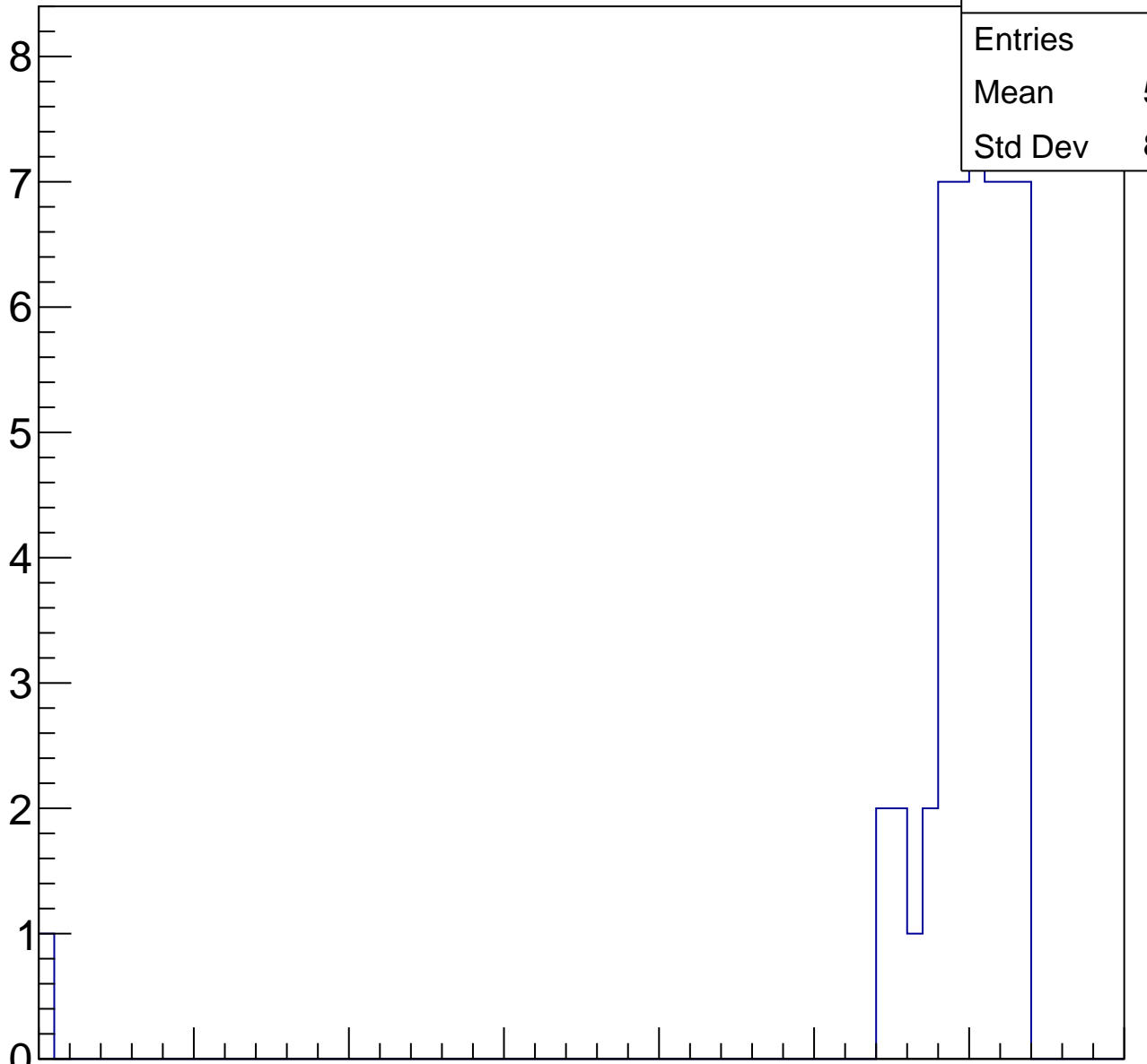
Entry

Entries	51
Mean	58.61
Std Dev	8.621

8  
7  
6  
5  
4  
3  
2  
1  
0

0 10 20 30 40 50 60 70

ampl



# B1L103S, U21-ch14, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	6
Mean	62.33
Std Dev	0.7454



# B1L103S, U21-ch14, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U21-ch15, adc0

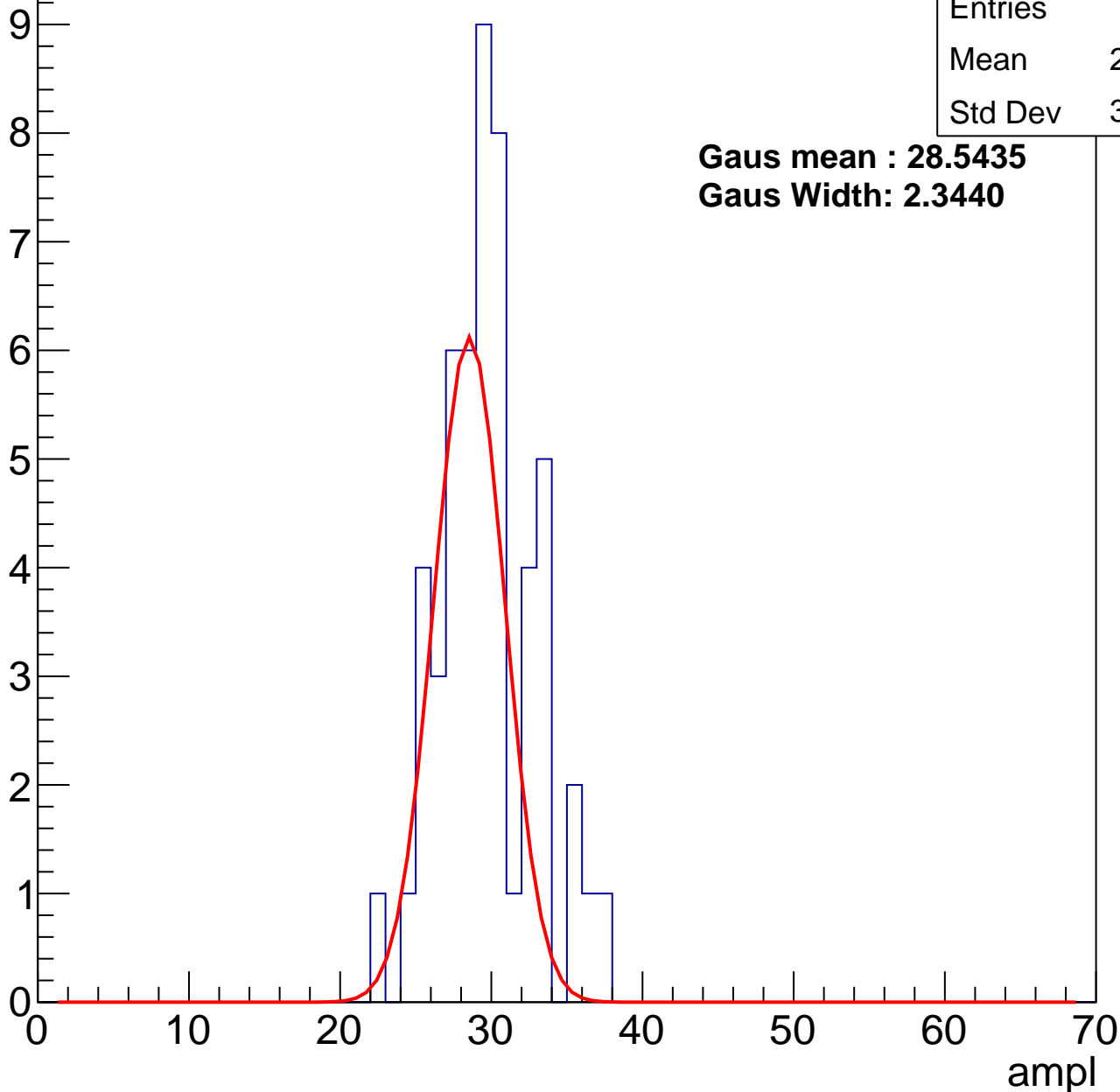
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	29.27
Std Dev	3.114

**Gaus mean : 28.5435**

**Gaus Width: 2.3440**



# B1L103S, U21-ch15, adc1

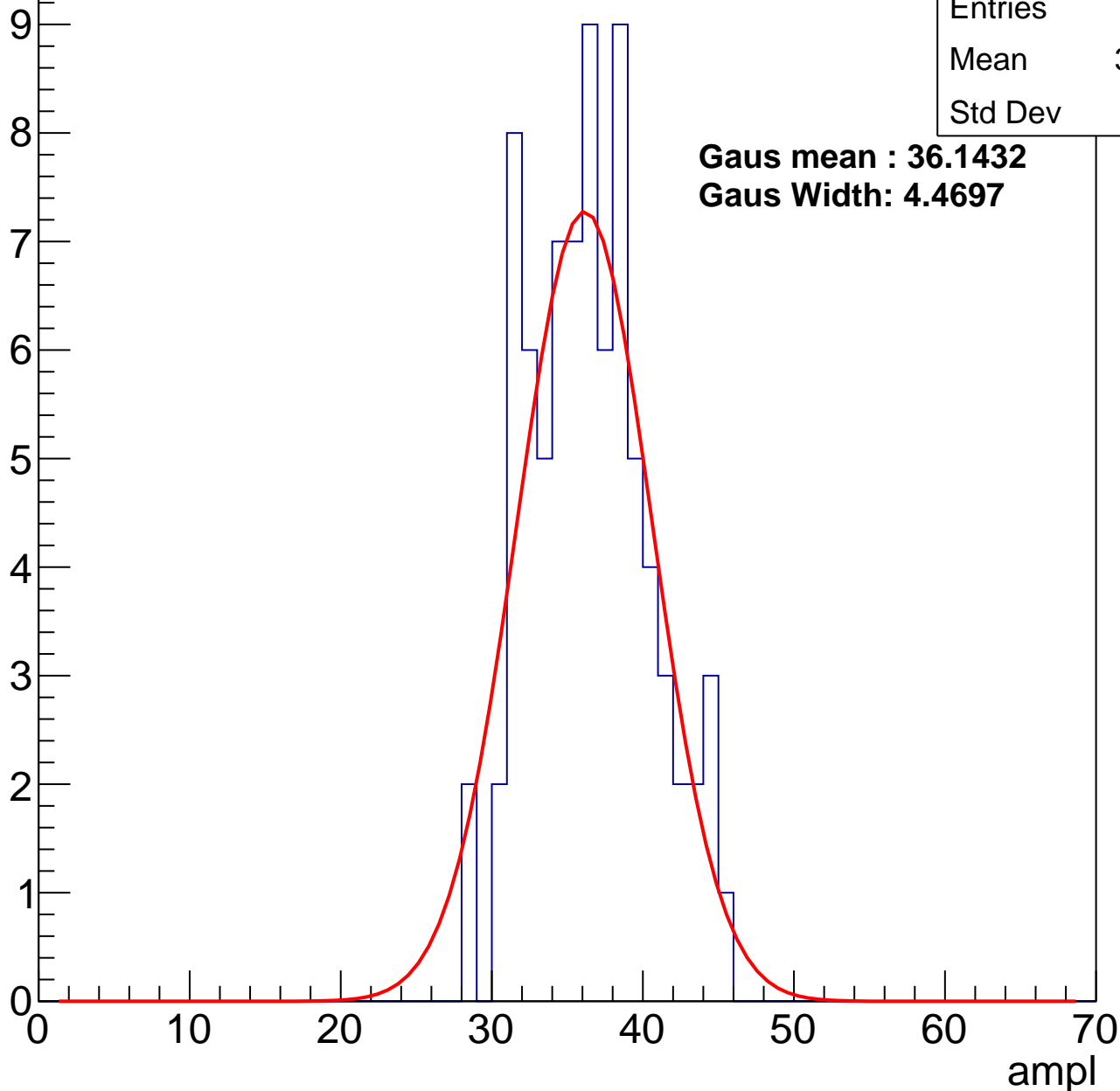
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	81
Mean	36.01
Std Dev	3.92

**Gaus mean : 36.1432**

**Gaus Width: 4.4697**



# B1L103S, U21-ch15, adc2

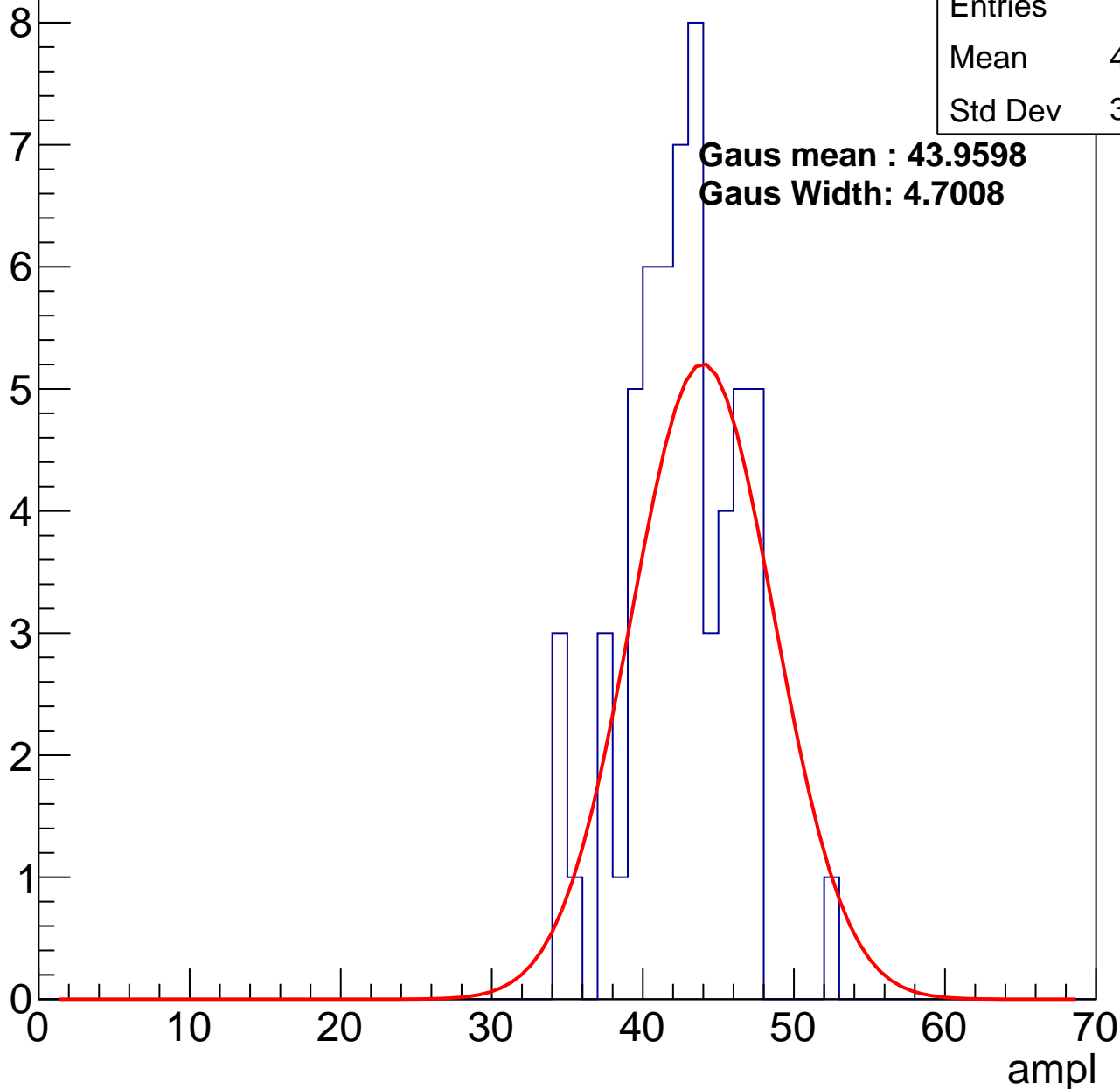
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	41.97
Std Dev	3.639

**Gaus mean : 43.9598**

**Gaus Width: 4.7008**

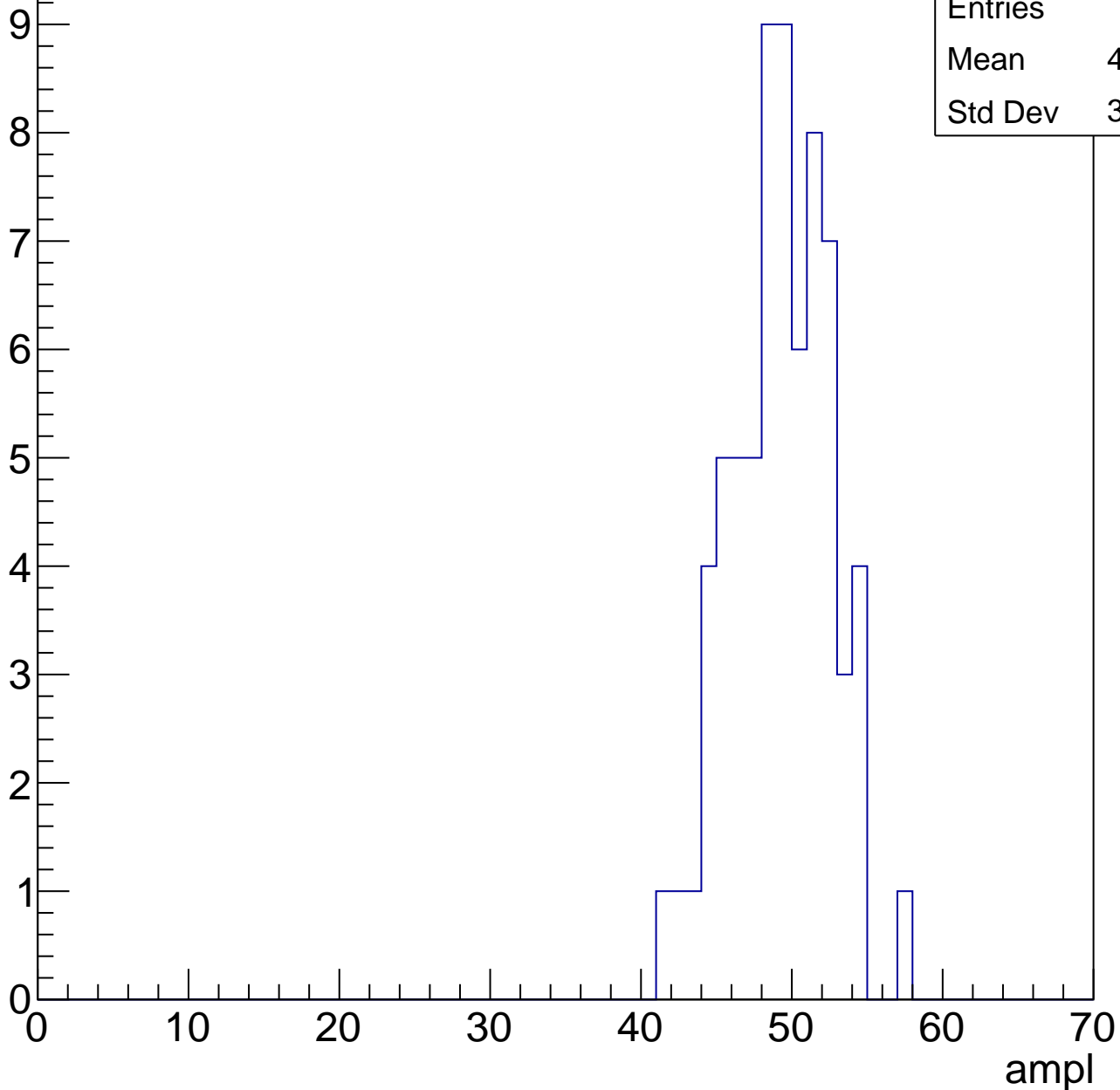


# B1L103S, U21-ch15, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	48.83
Std Dev	3.217

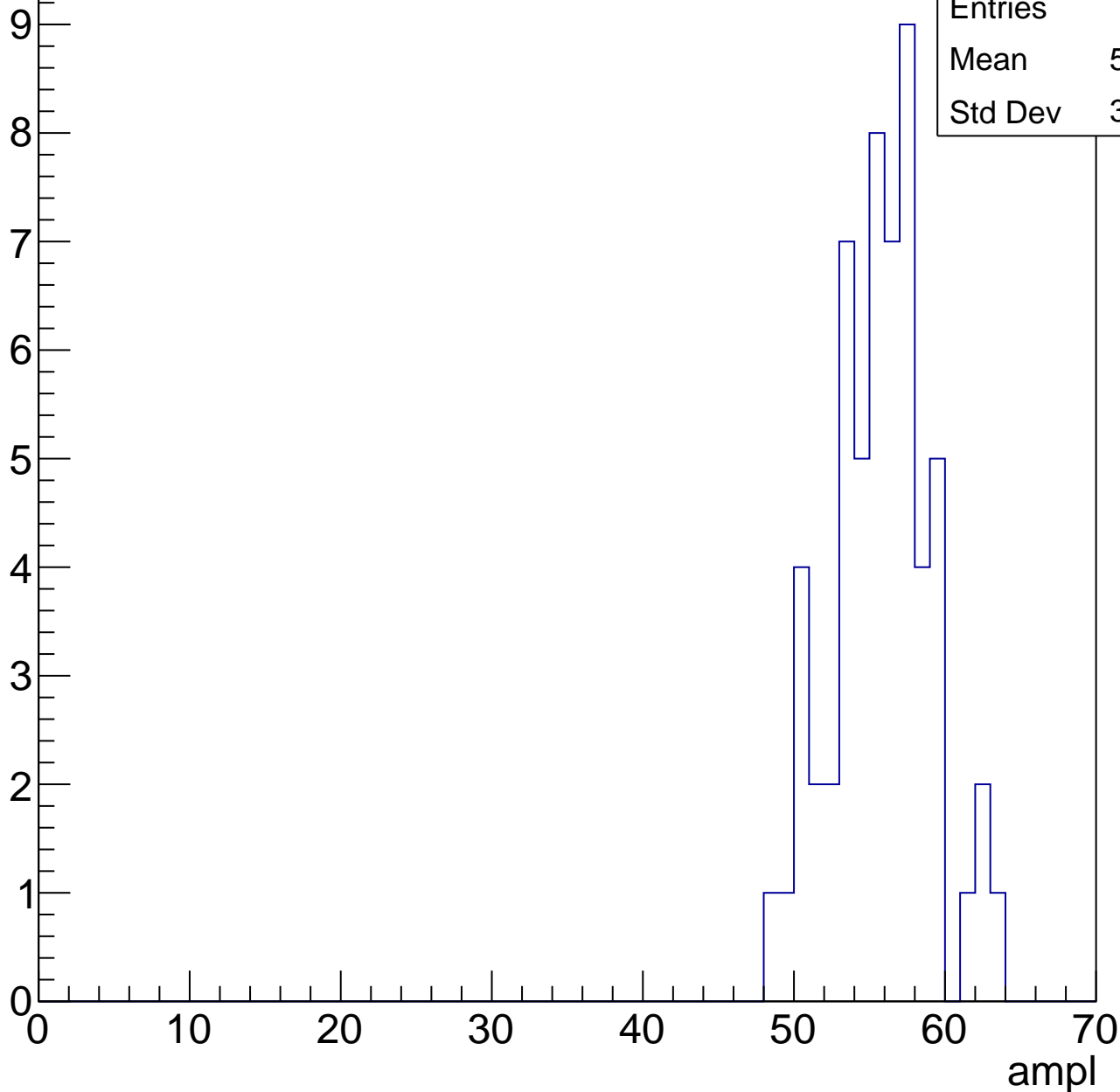


# B1L103S, U21-ch15, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	55.32
Std Dev	3.239

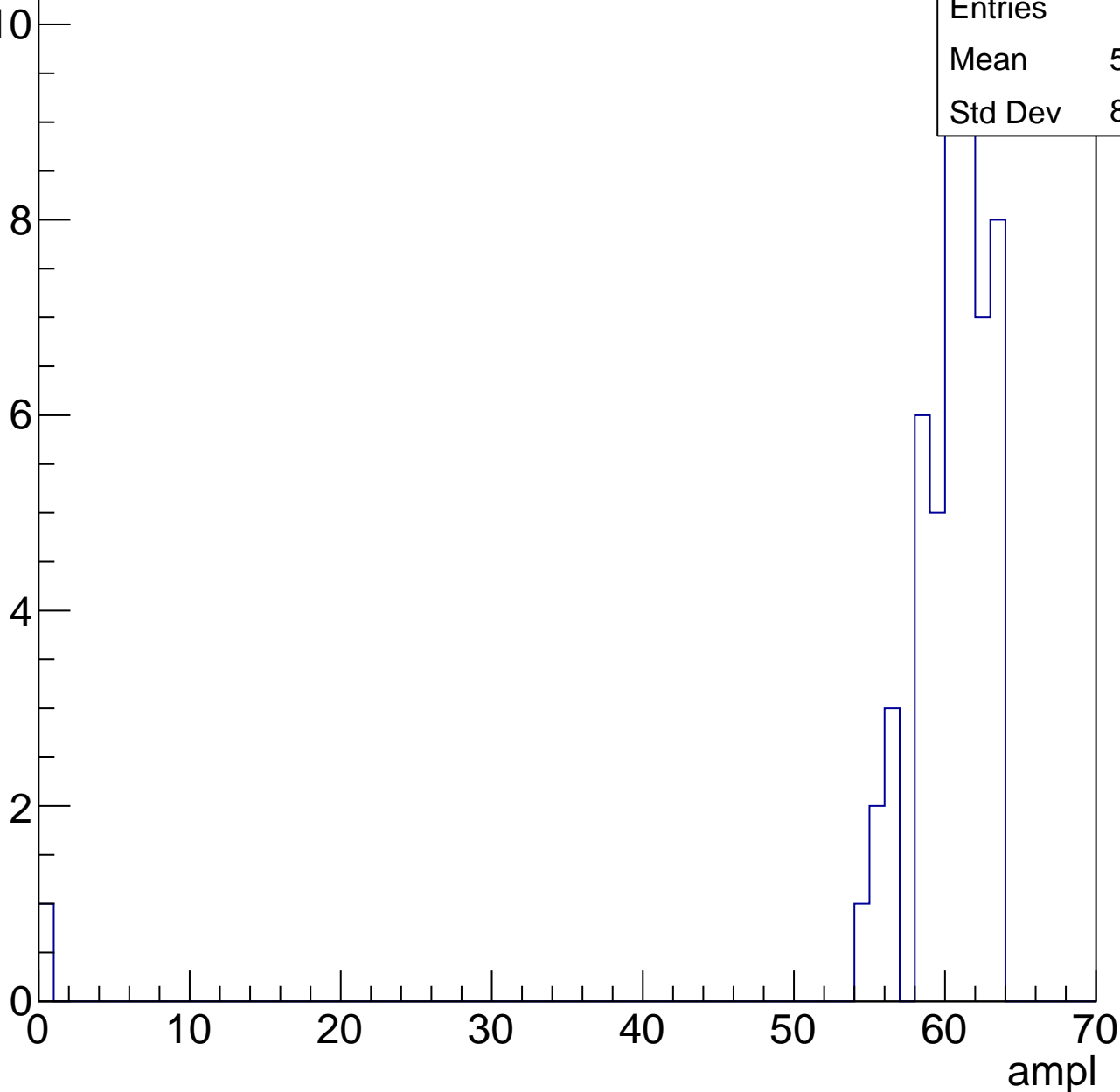


# B1L103S, U21-ch15, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	58.88
Std Dev	8.557



# B1L103S, U21-ch15, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U21-ch15, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U21-ch16, adc0

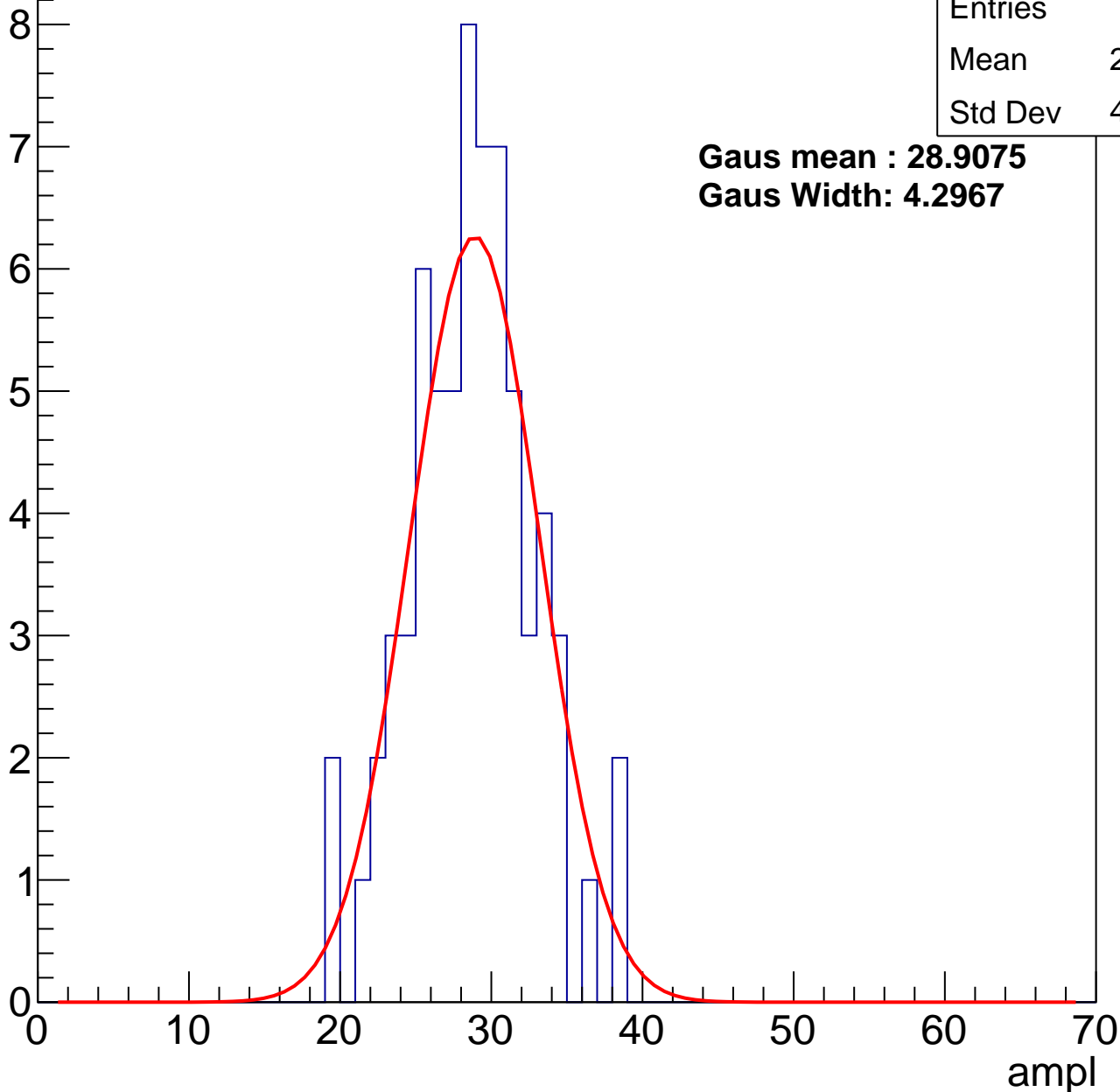
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	28.25
Std Dev	4.016

**Gaus mean : 28.9075**

**Gaus Width: 4.2967**



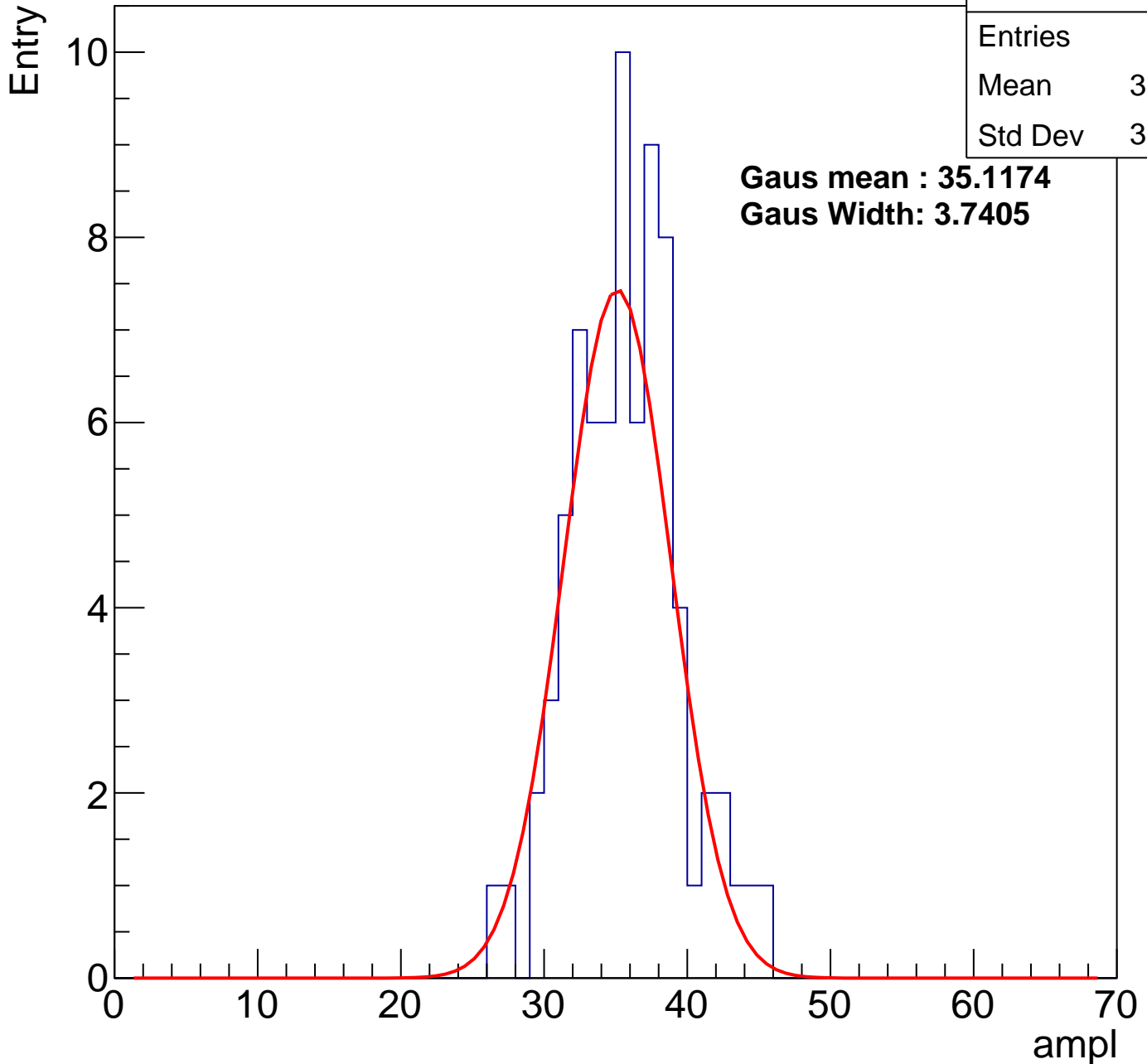
# B1L103S, U21-ch16, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	76
Mean	35.25
Std Dev	3.767

**Gaus mean : 35.1174**

**Gaus Width: 3.7405**



# B1L103S, U21-ch16, adc2

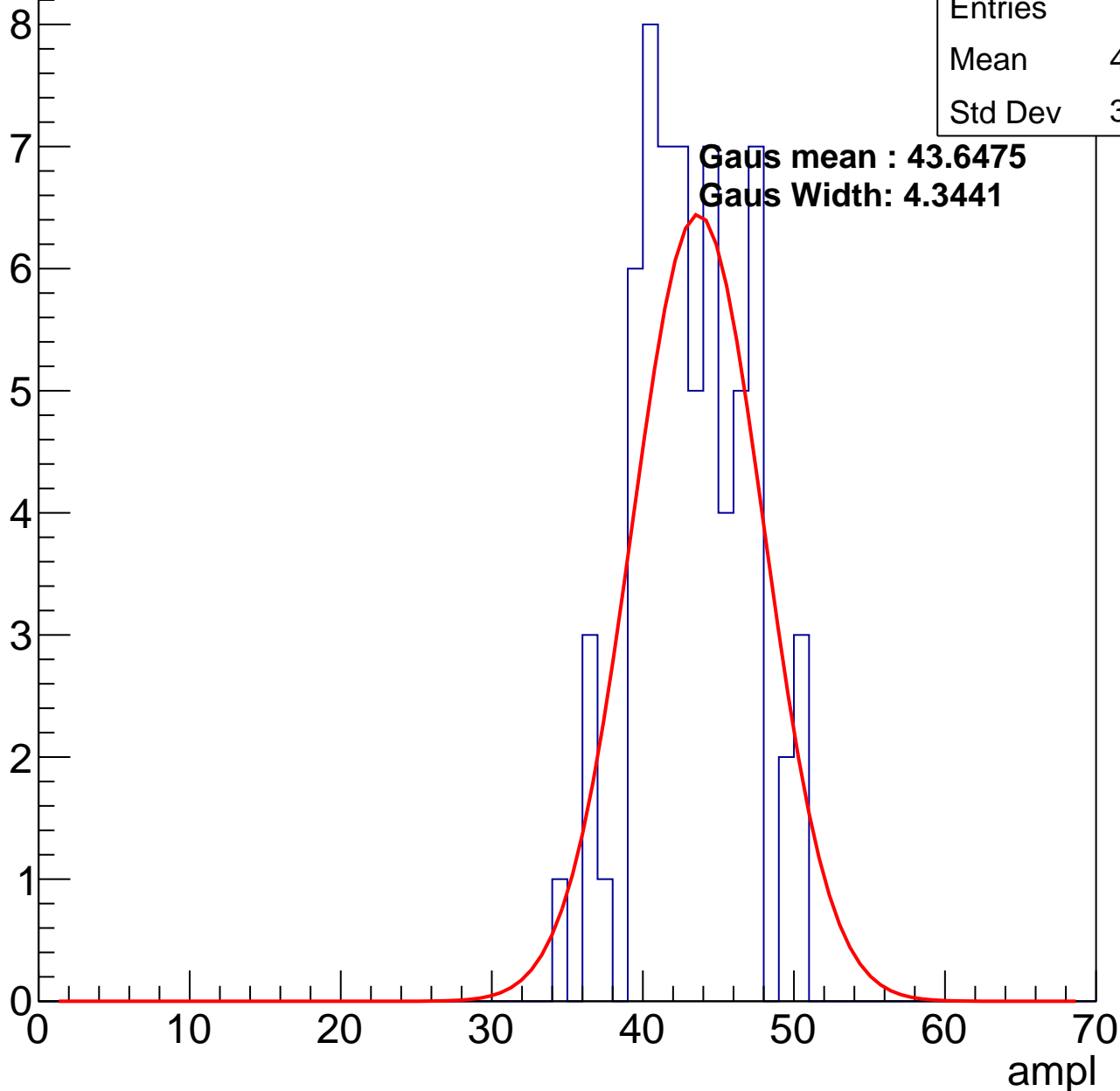
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	42.79
Std Dev	3.616

**Gaus mean : 43.6475**

**Gaus Width: 4.3441**

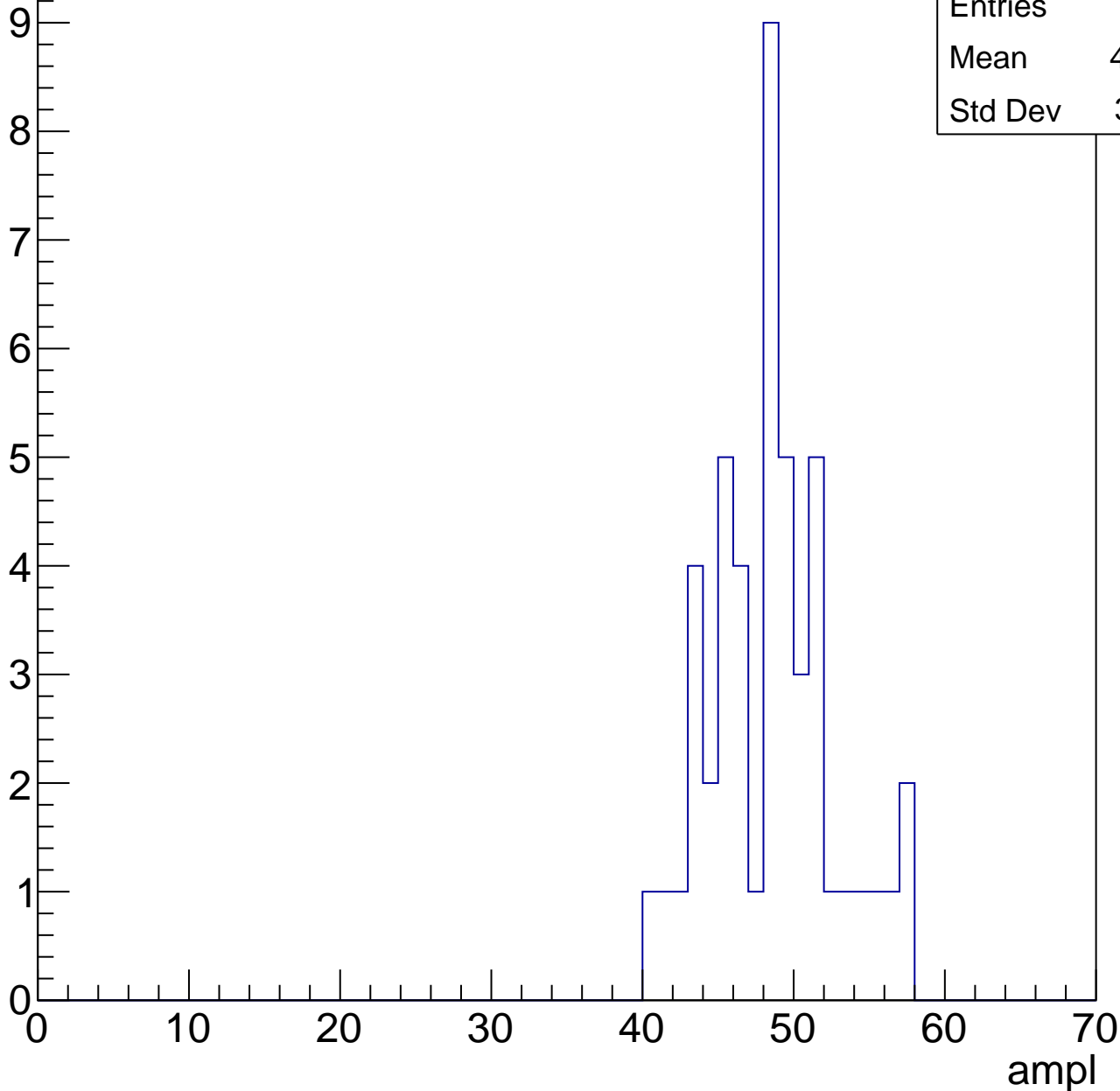


# B1L103S, U21-ch16, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	48
Mean	48.02
Std Dev	3.971

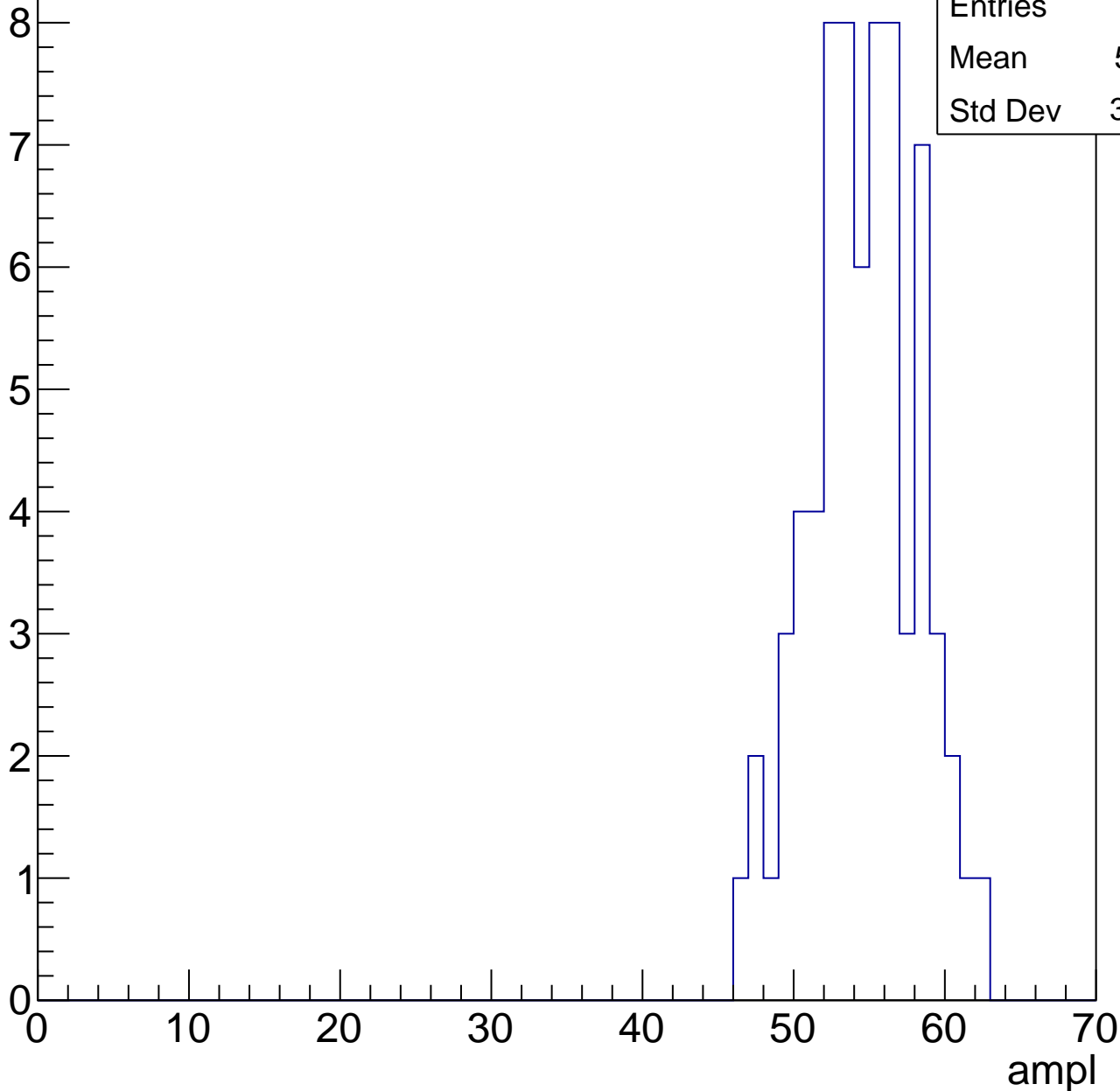


# B1L103S, U21-ch16, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	54.11
Std Dev	3.487

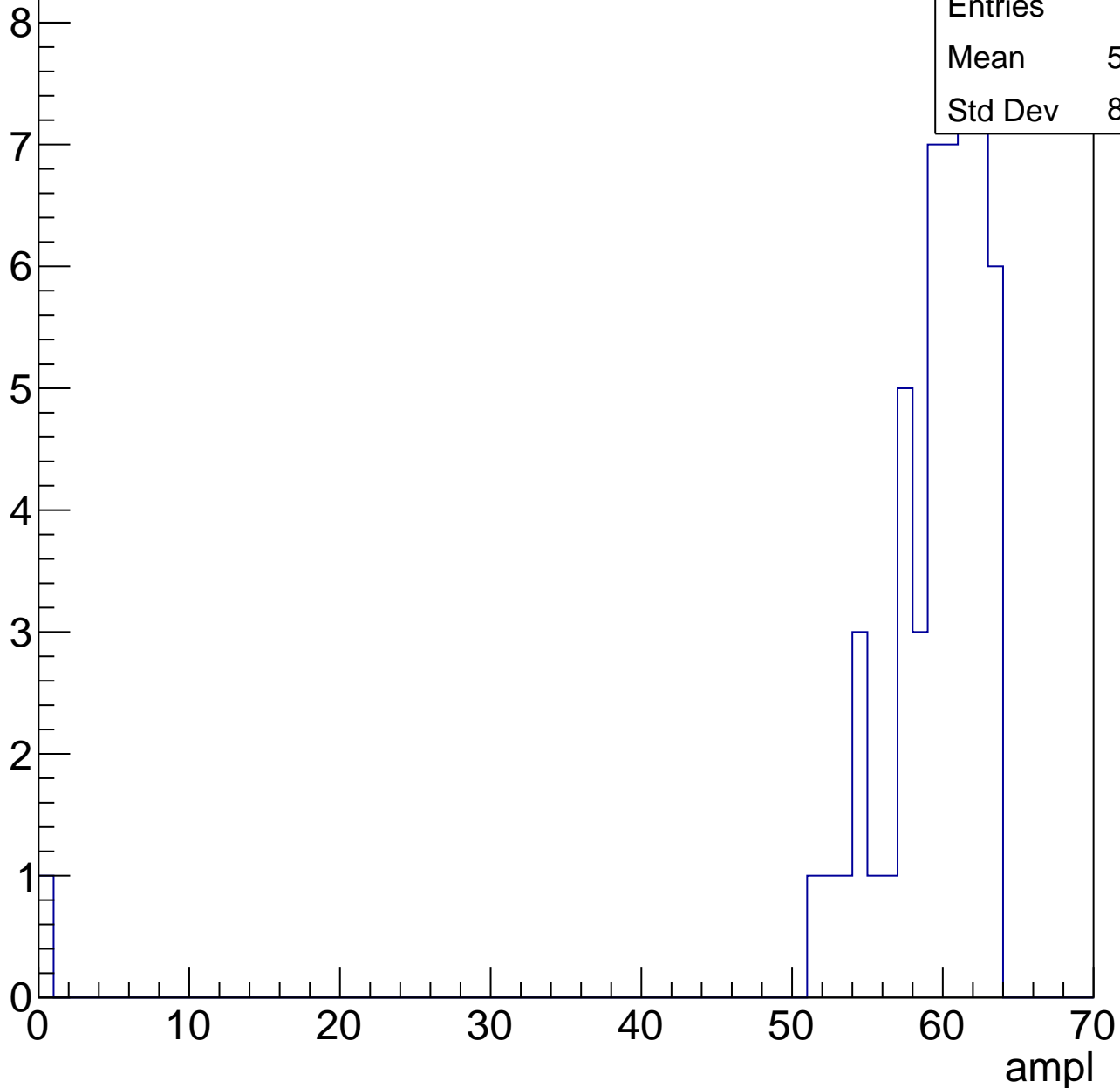


# B1L103S, U21-ch16, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

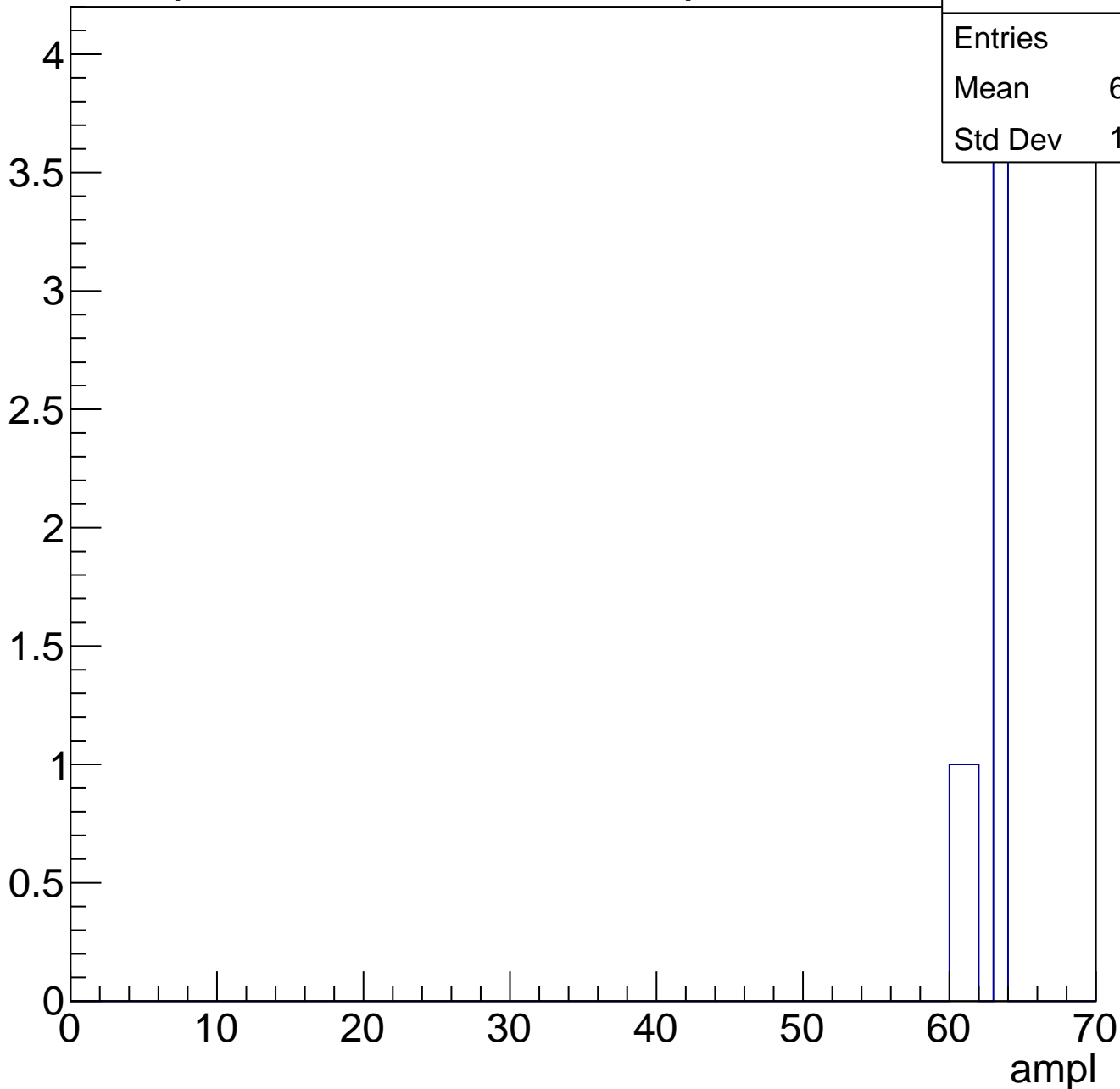
Entries	53
Mean	58.17
Std Dev	8.604



# B1L103S, U21-ch16, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U21-ch16, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U21-ch17, adc0

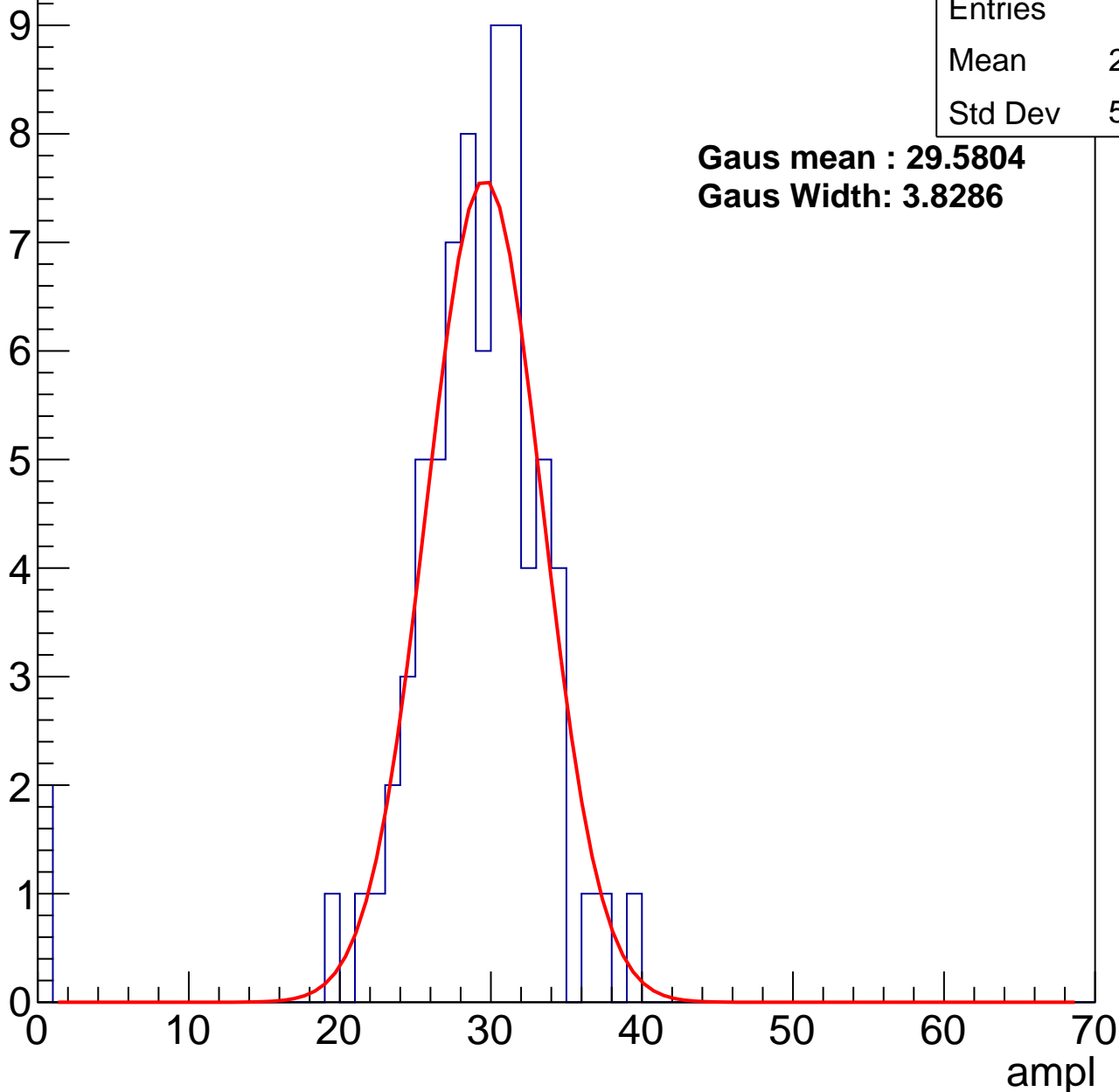
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	28.16
Std Dev	5.915

**Gaus mean : 29.5804**

**Gaus Width: 3.8286**



# B1L103S, U21-ch17, adc1

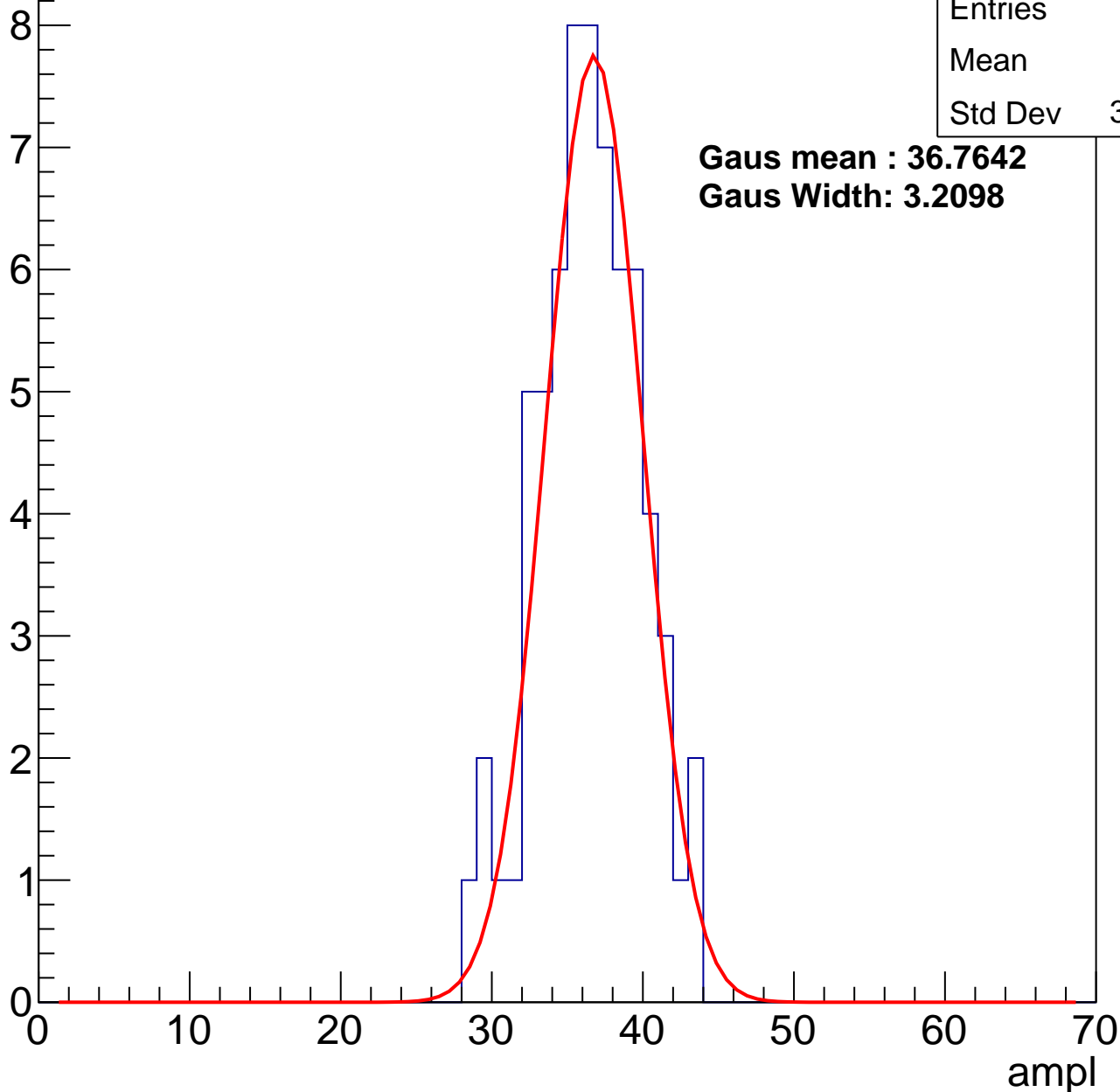
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	36
Std Dev	3.344

**Gaus mean : 36.7642**

**Gaus Width: 3.2098**



# B1L103S, U21-ch17, adc2

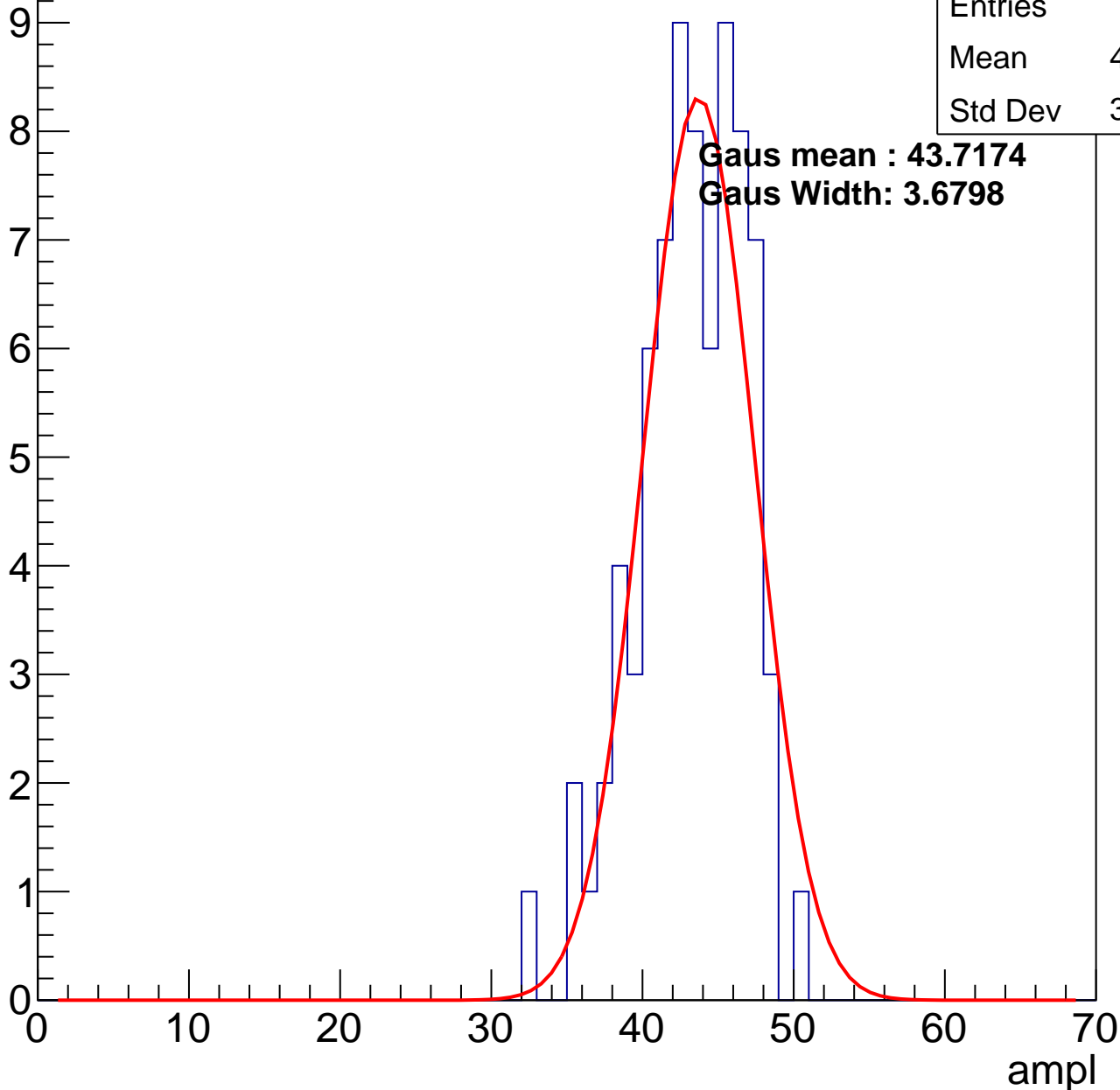
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	42.73
Std Dev	3.519

**Gaus mean : 43.7174**

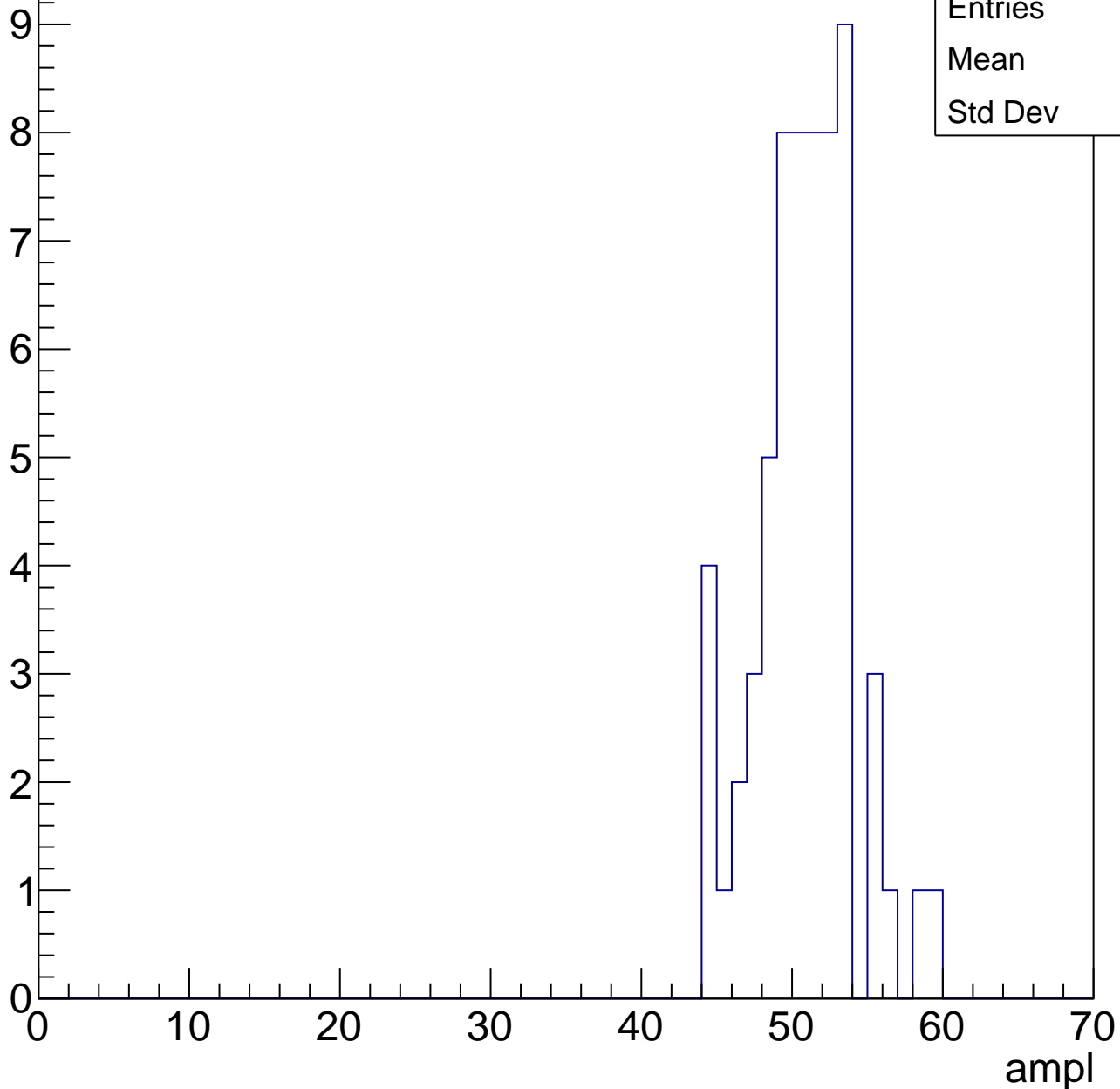
**Gaus Width: 3.6798**



# B1L103S, U21-ch17, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



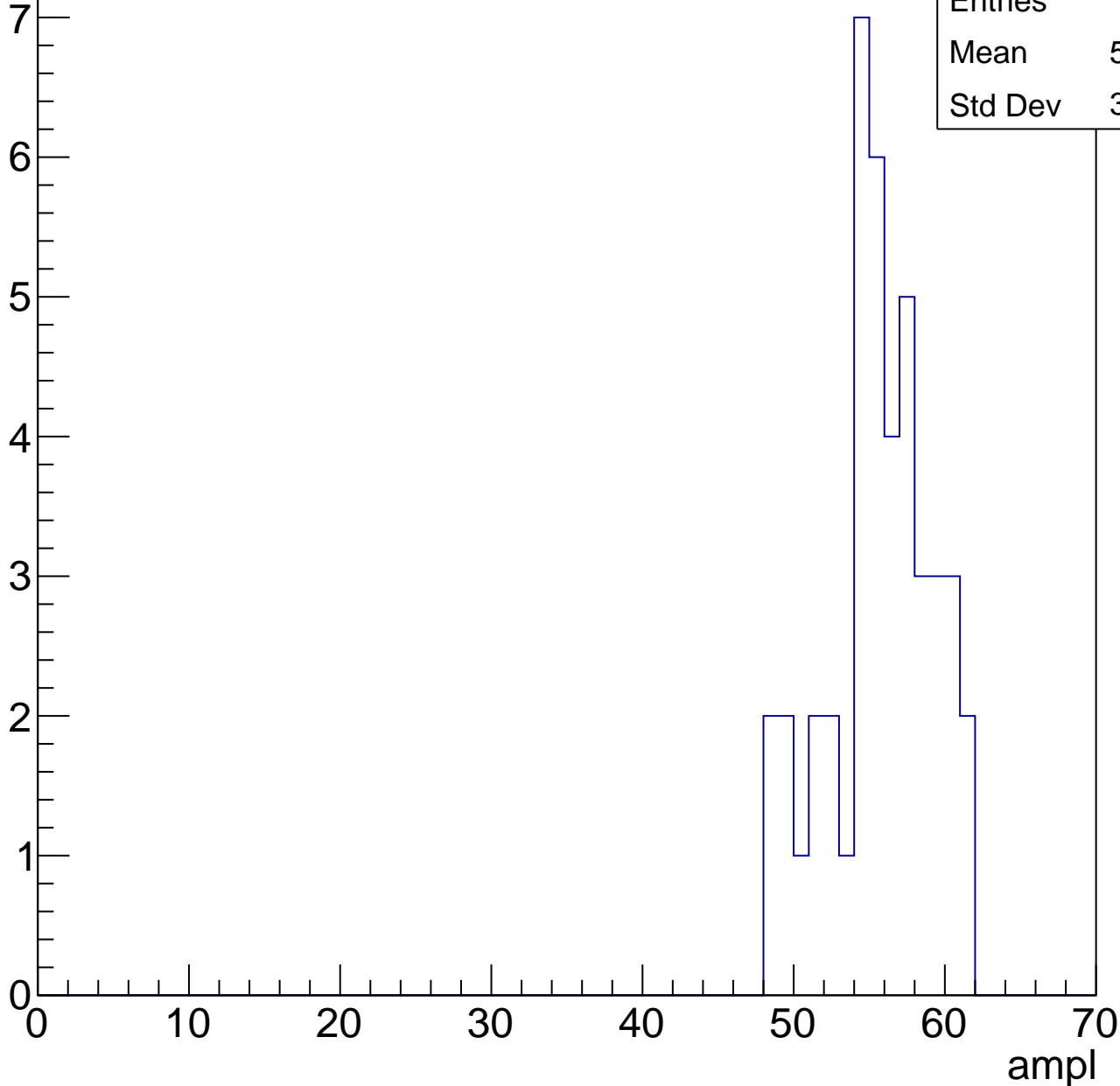
Entries	62
Mean	50.4
Std Dev	3.17

# B1L103S, U21-ch17, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	43
Mean	55.19
Std Dev	3.412

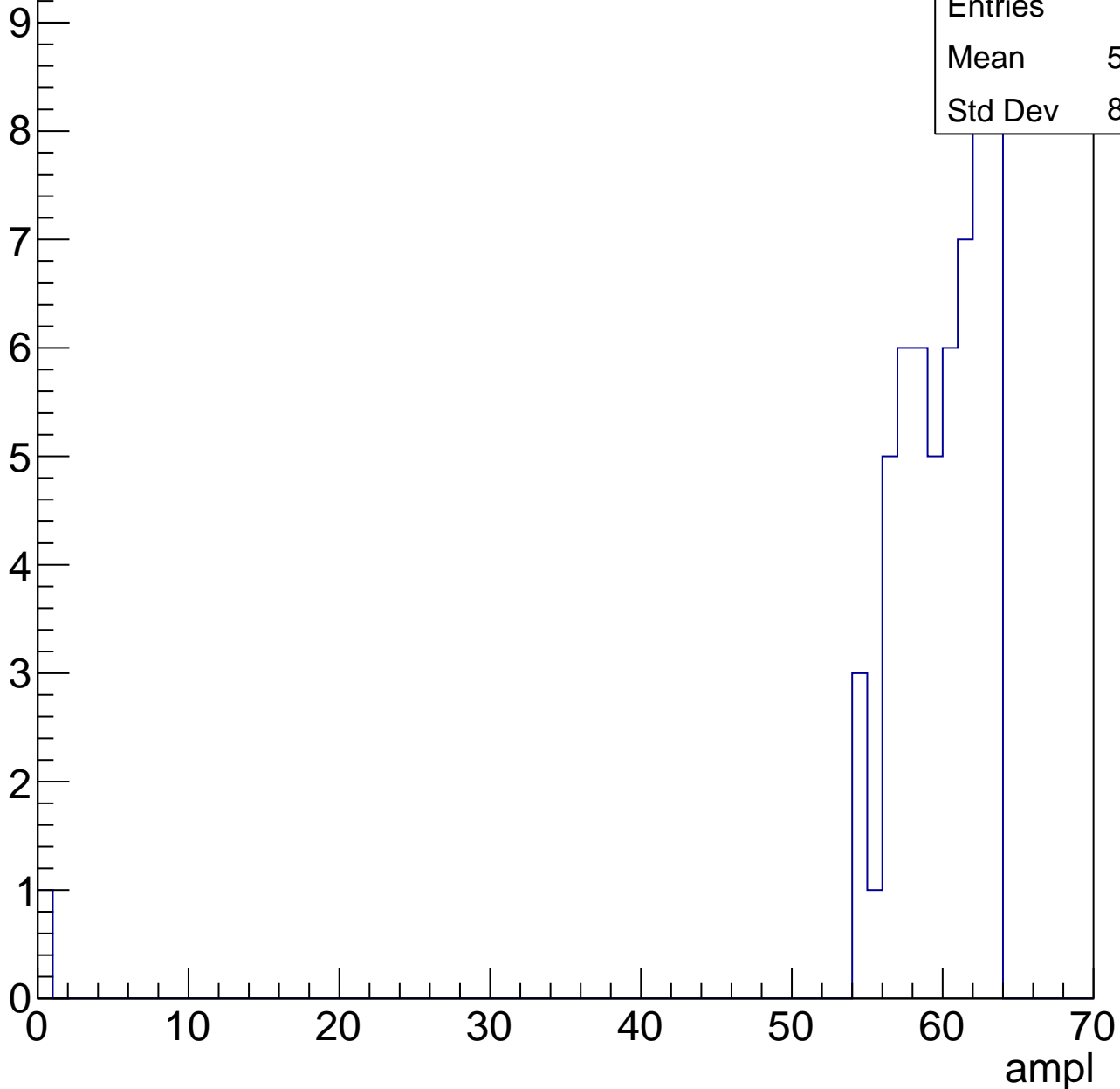


# B1L103S, U21-ch17, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	58.44
Std Dev	8.242



# B1L103S, U21-ch17, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

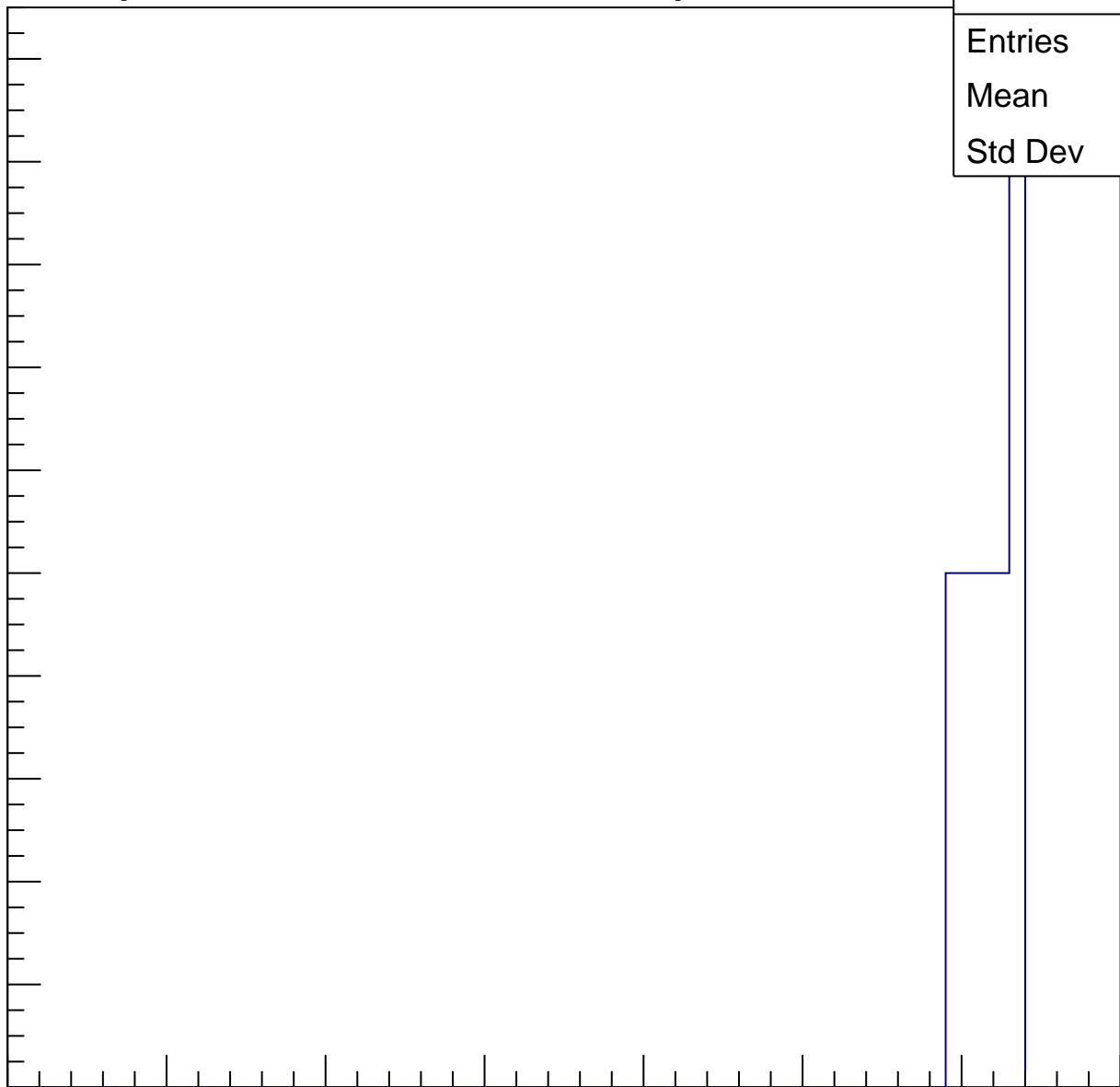
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	61.33
Std Dev	1.491

0 10 20 30 40 50 60 70

ampl





# B1L103S, U21-ch17, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U21-ch18, adc0

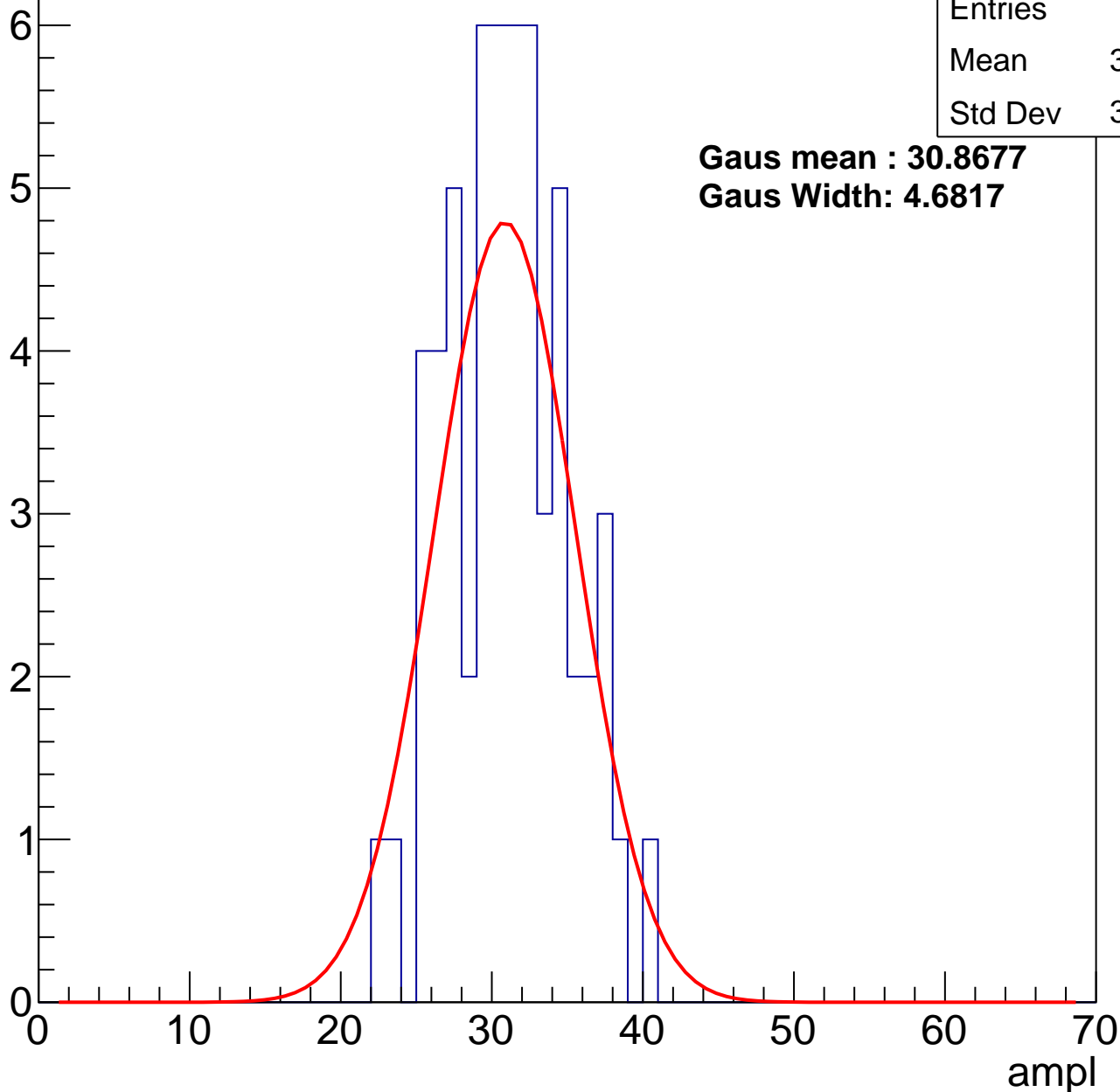
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	30.55
Std Dev	3.914

**Gaus mean : 30.8677**

**Gaus Width: 4.6817**



# B1L103S, U21-ch18, adc1

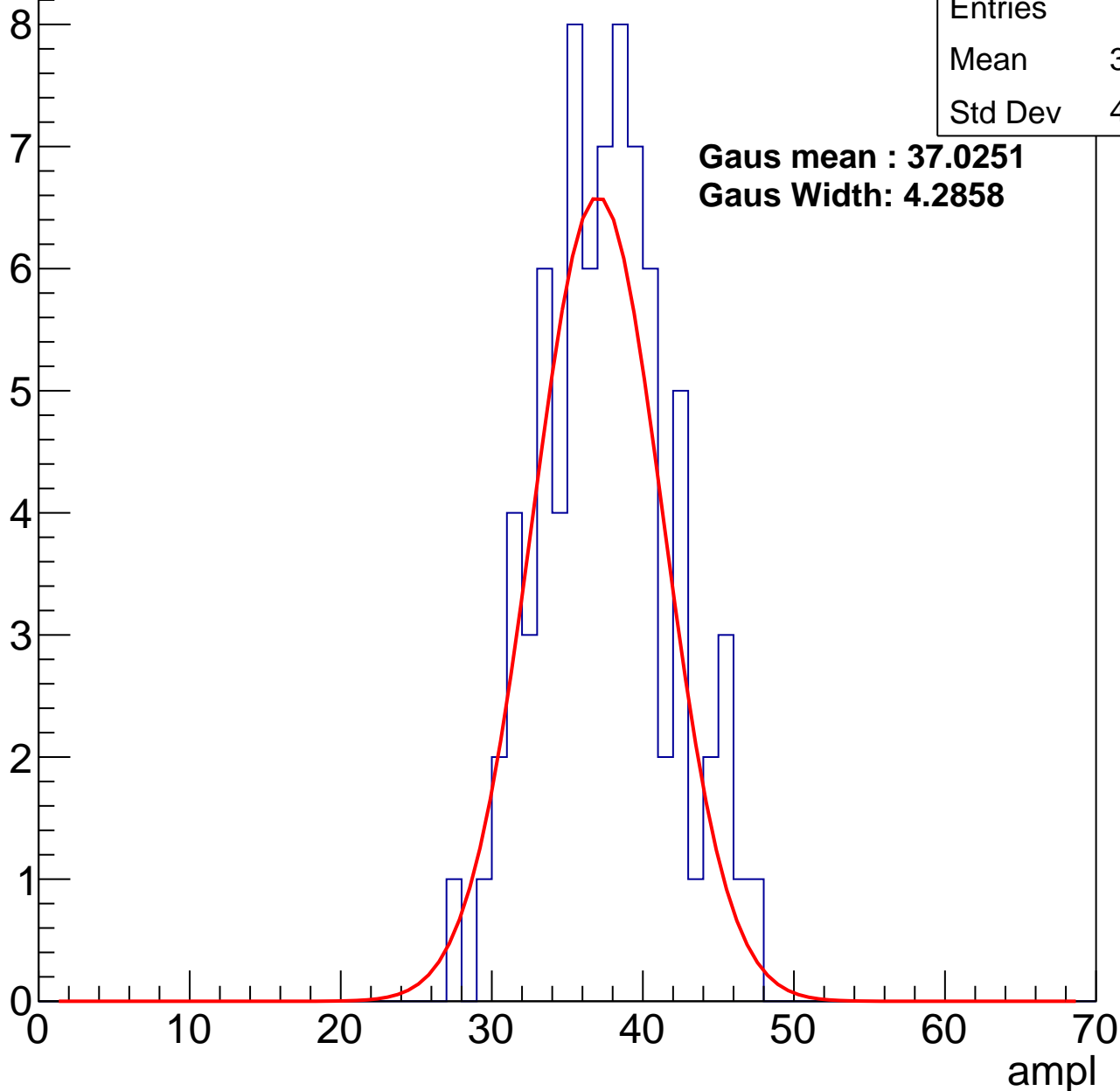
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	37.09
Std Dev	4.243

**Gaus mean : 37.0251**

**Gaus Width: 4.2858**



# B1L103S, U21-ch18, adc2

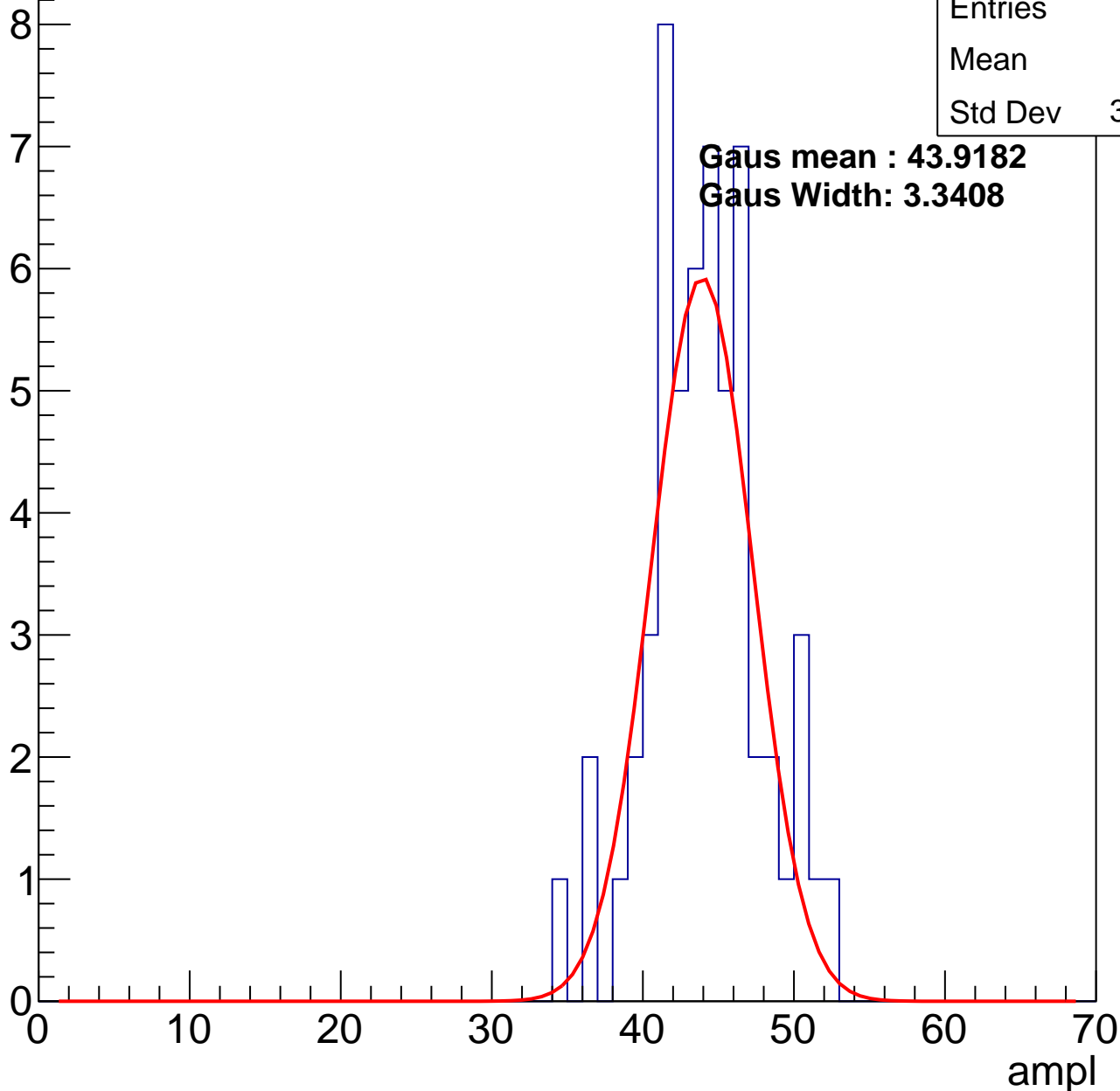
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	43.6
Std Dev	3.699

**Gaus mean : 43.9182**

**Gaus Width: 3.3408**

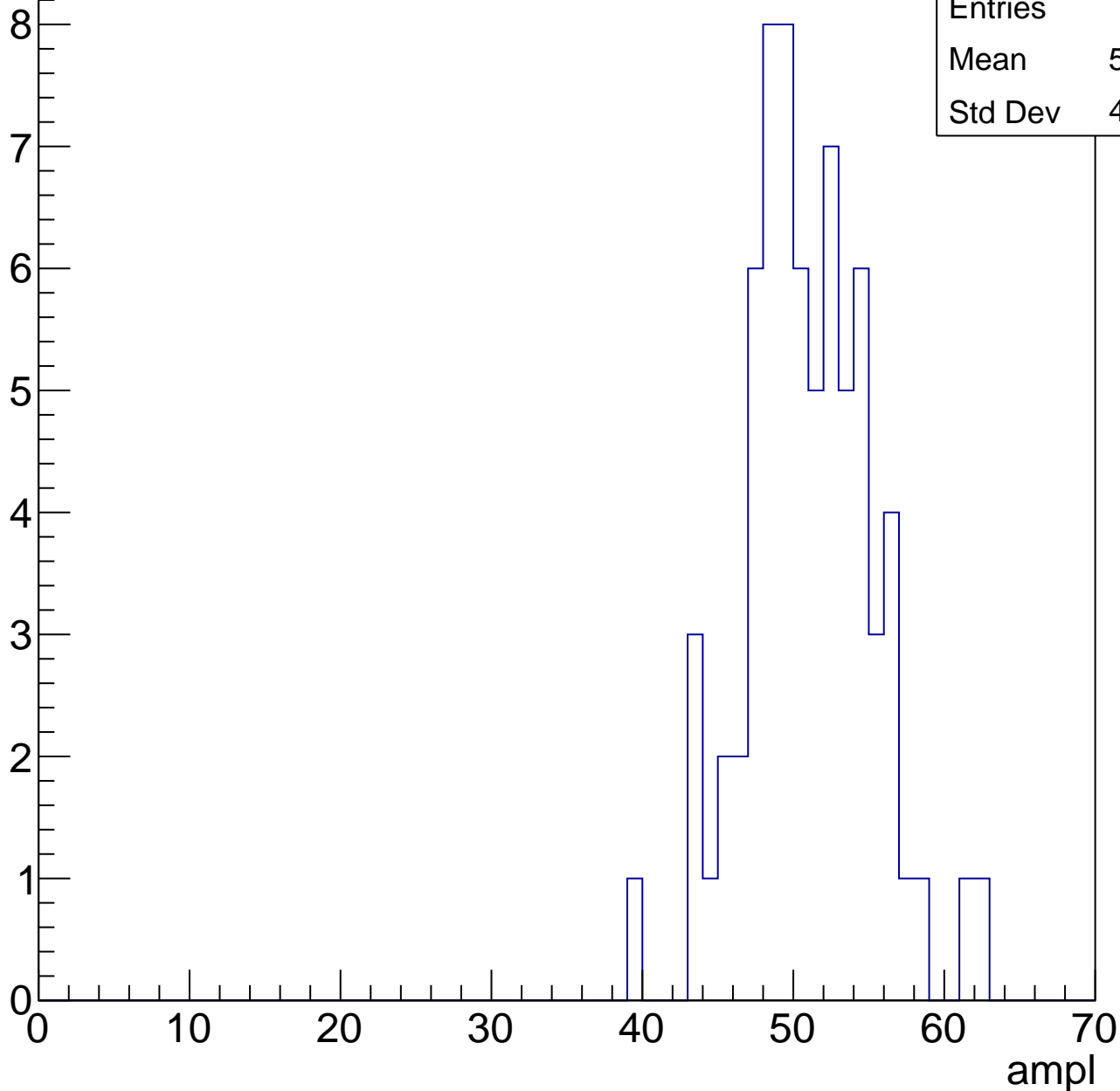


# B1L103S, U21-ch18, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	50.52
Std Dev	4.165

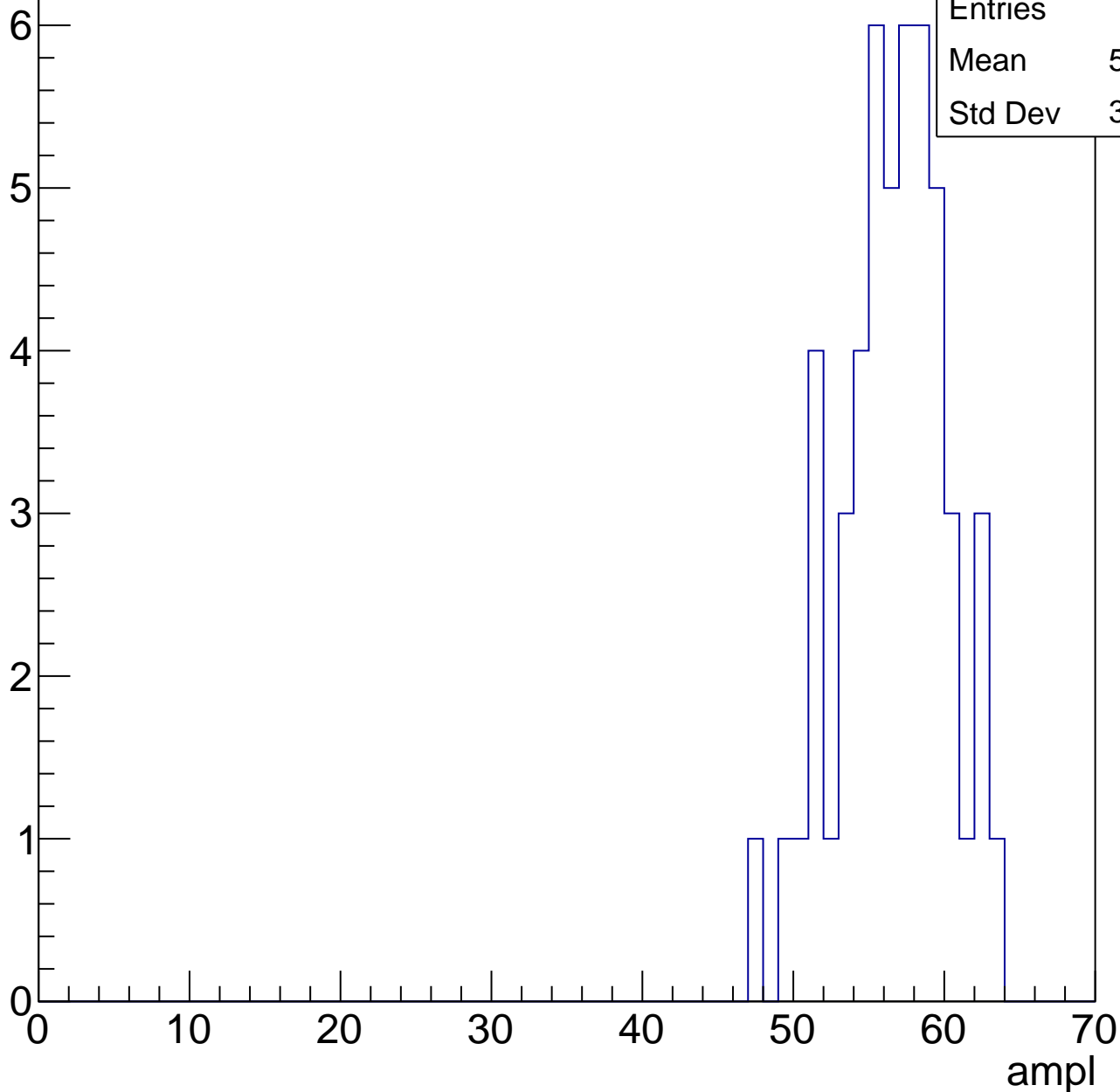


# B1L103S, U21-ch18, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	56.12
Std Dev	3.529

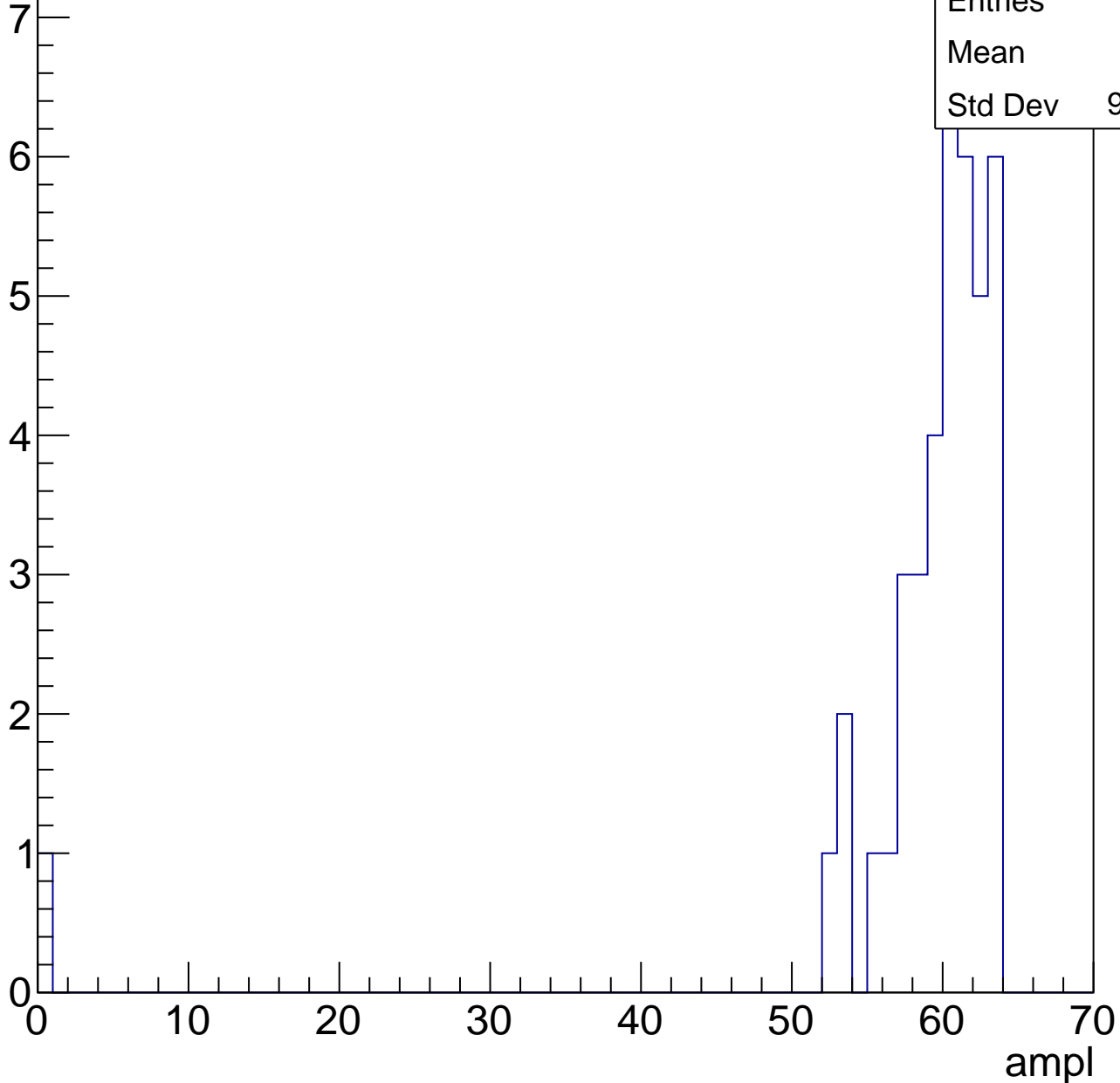


# B1L103S, U21-ch18, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

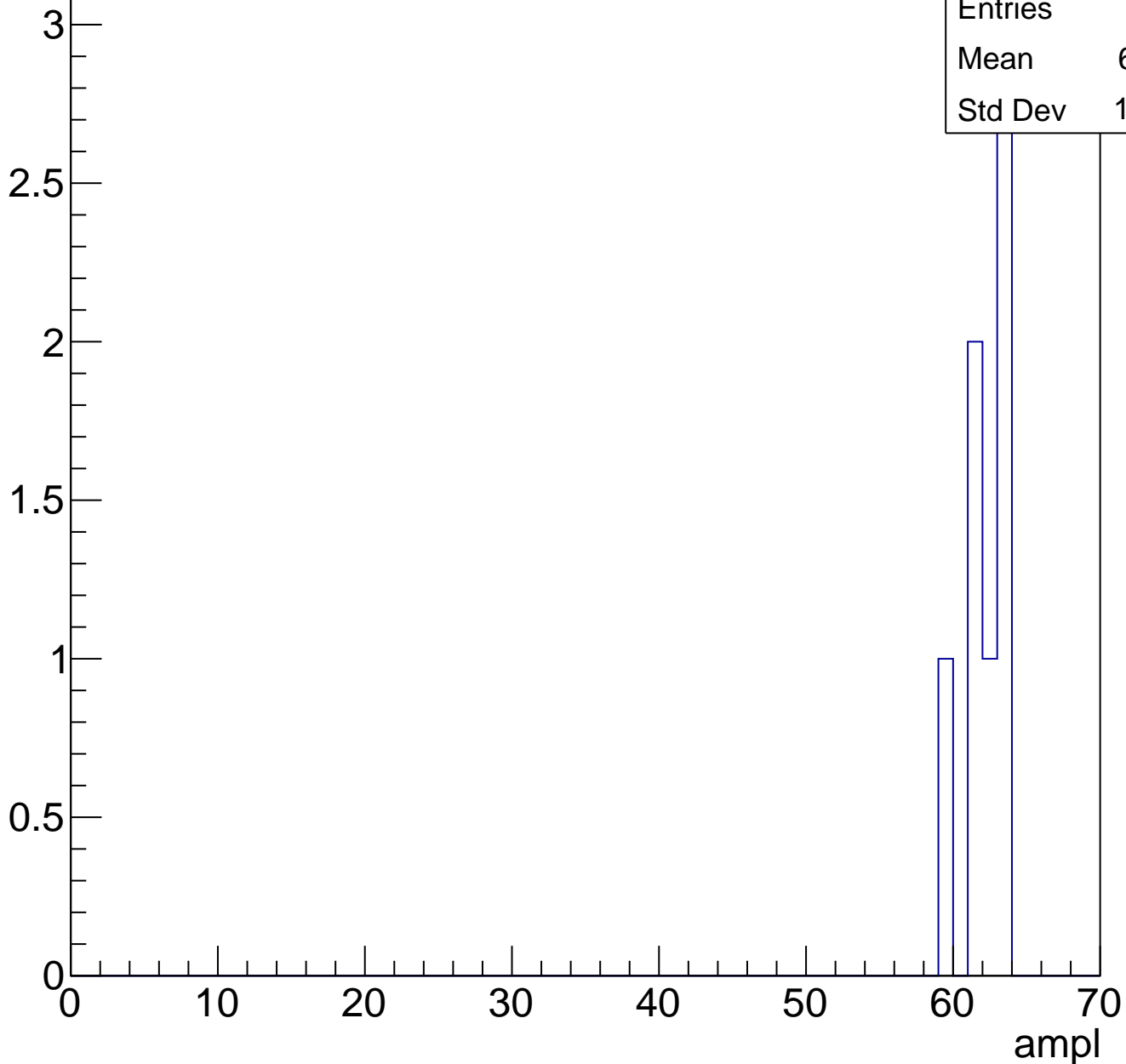
Entries	40
Mean	58.1
Std Dev	9.723



# B1L103S, U21-ch18, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U21-ch18, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U21-ch19, adc0

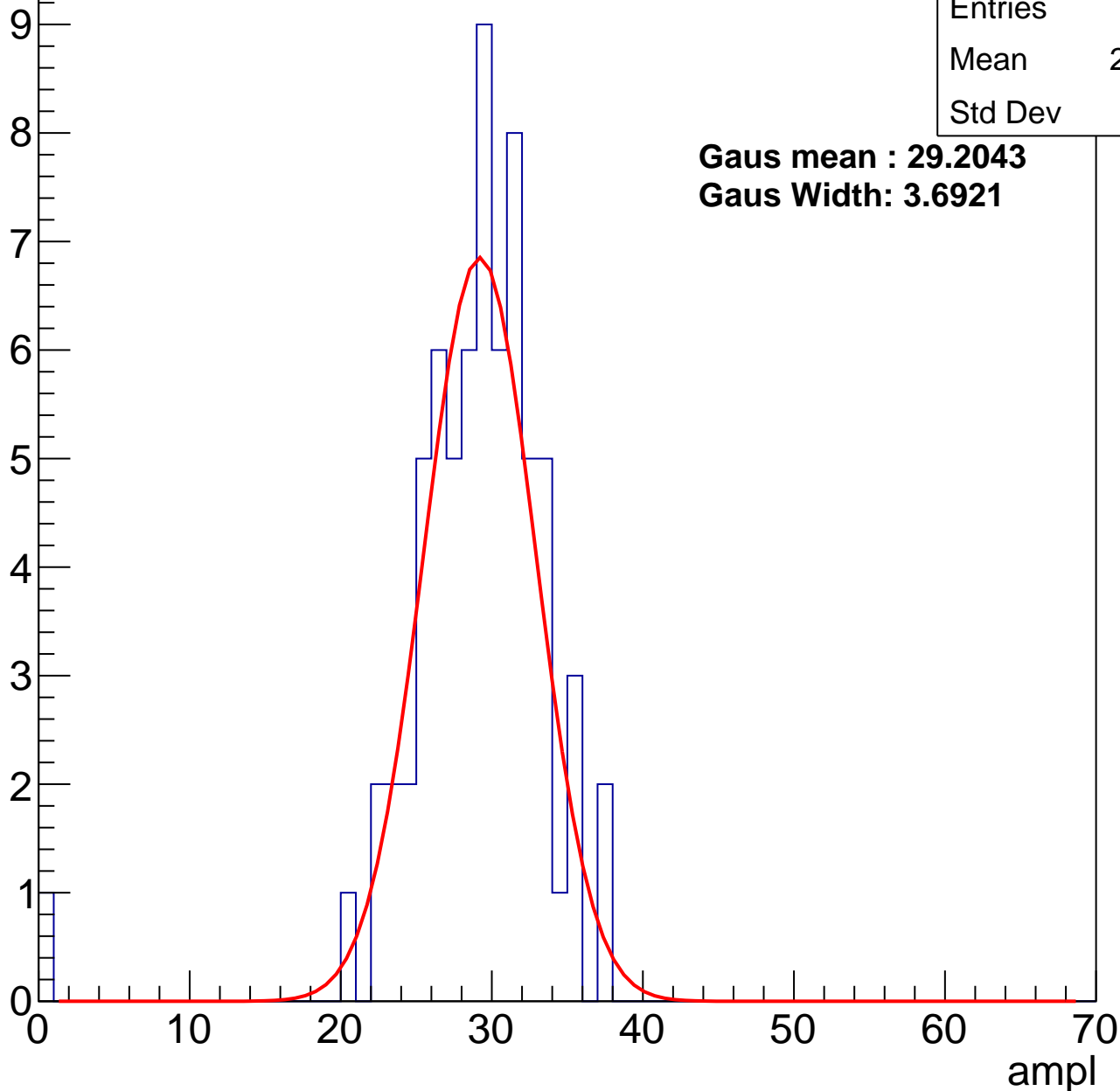
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	28.54
Std Dev	4.98

**Gaus mean : 29.2043**

**Gaus Width: 3.6921**



# B1L103S, U21-ch19, adc1

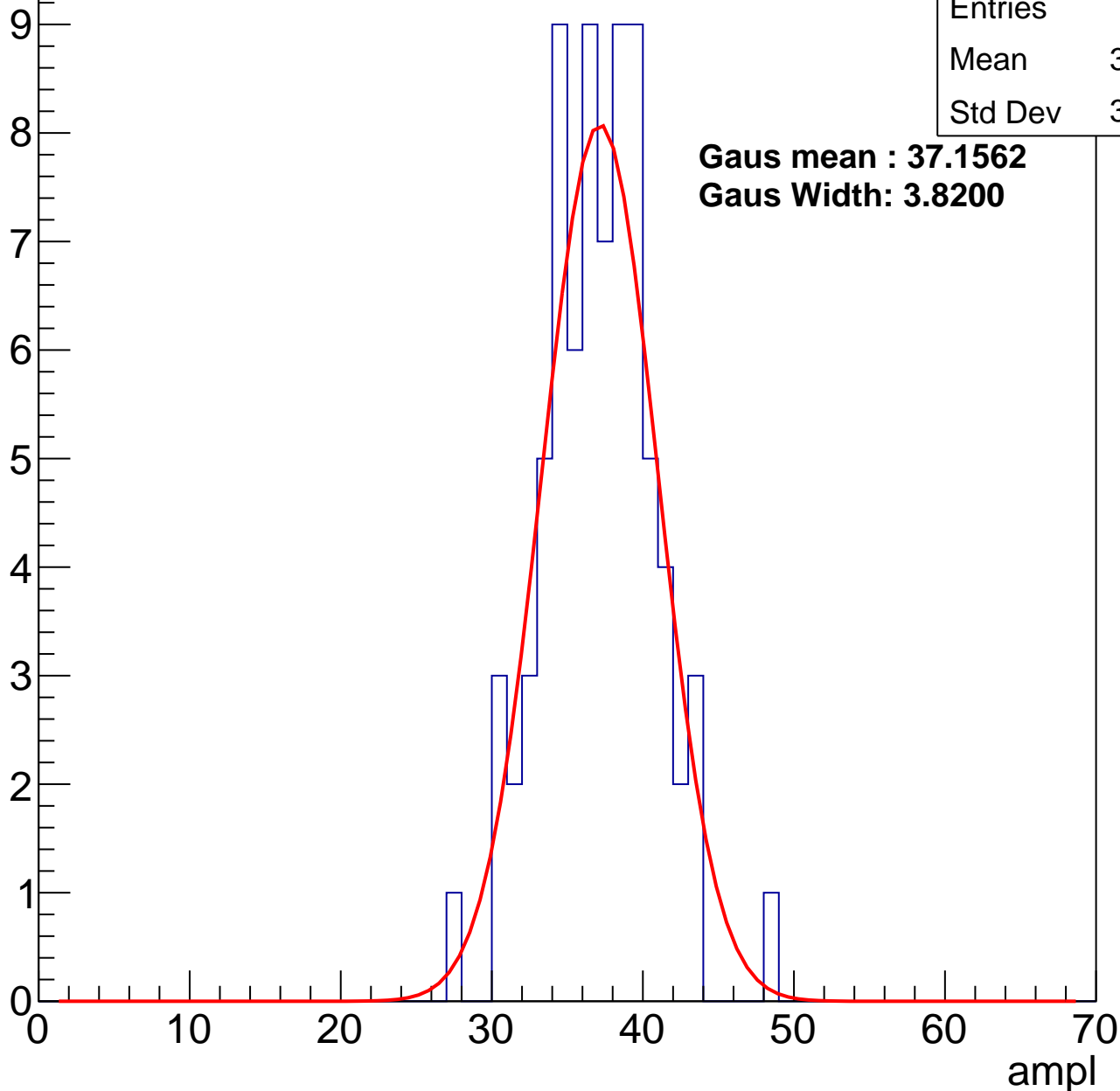
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	36.63
Std Dev	3.599

**Gaus mean : 37.1562**

**Gaus Width: 3.8200**



# B1L103S, U21-ch19, adc2

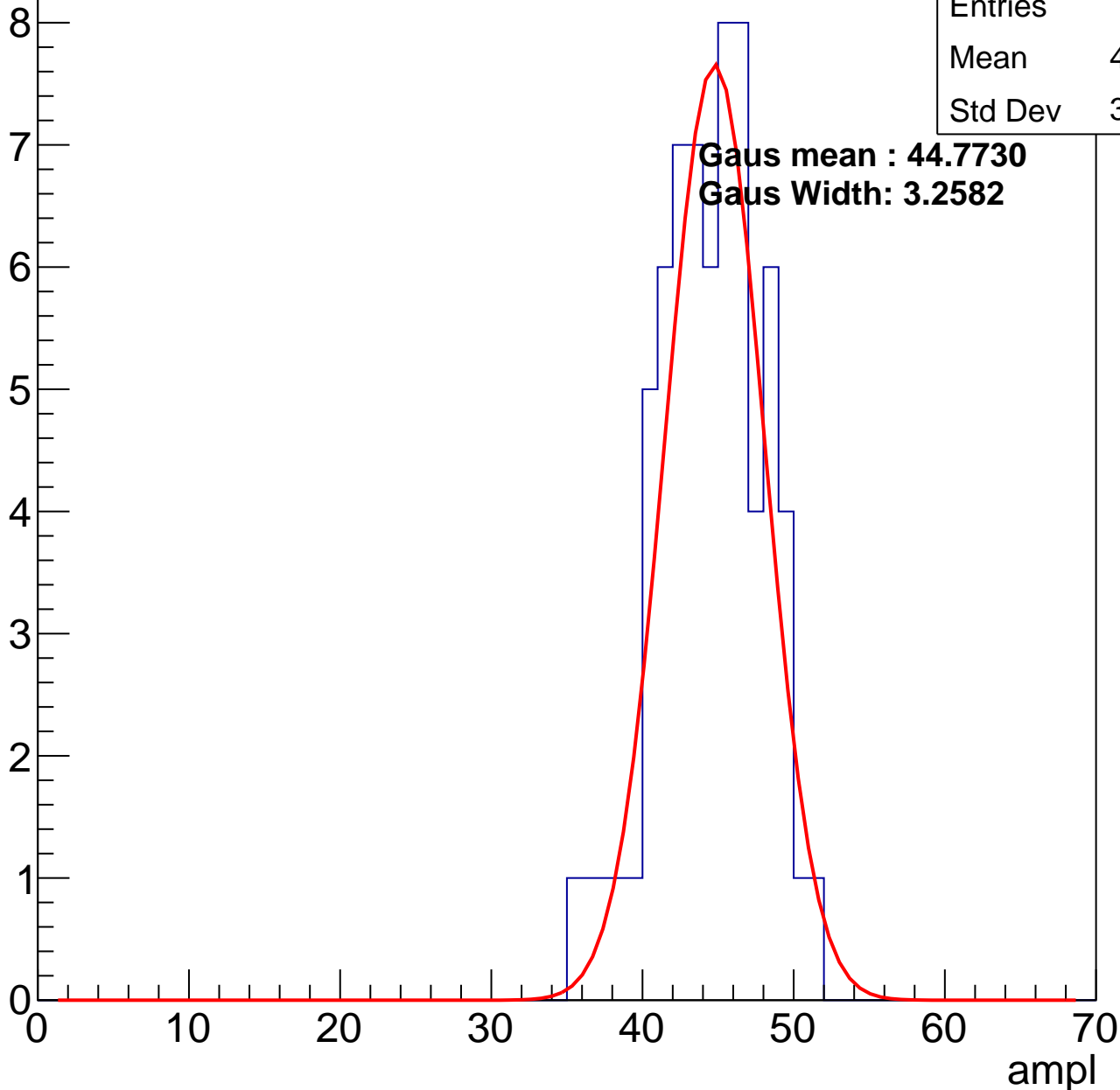
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	43.99
Std Dev	3.389

**Gaus mean : 44.7730**

**Gaus Width: 3.2582**

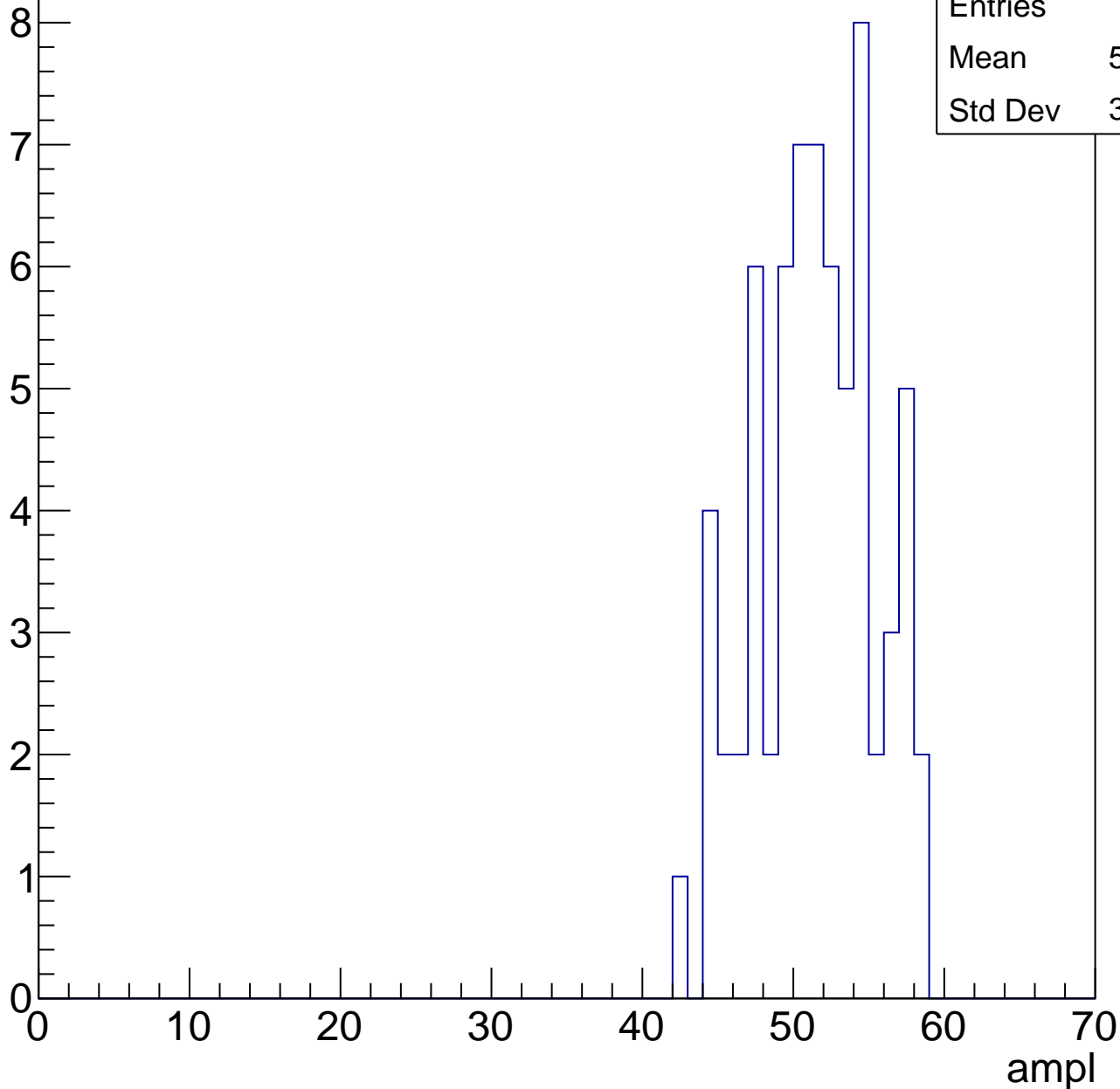


# B1L103S, U21-ch19, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

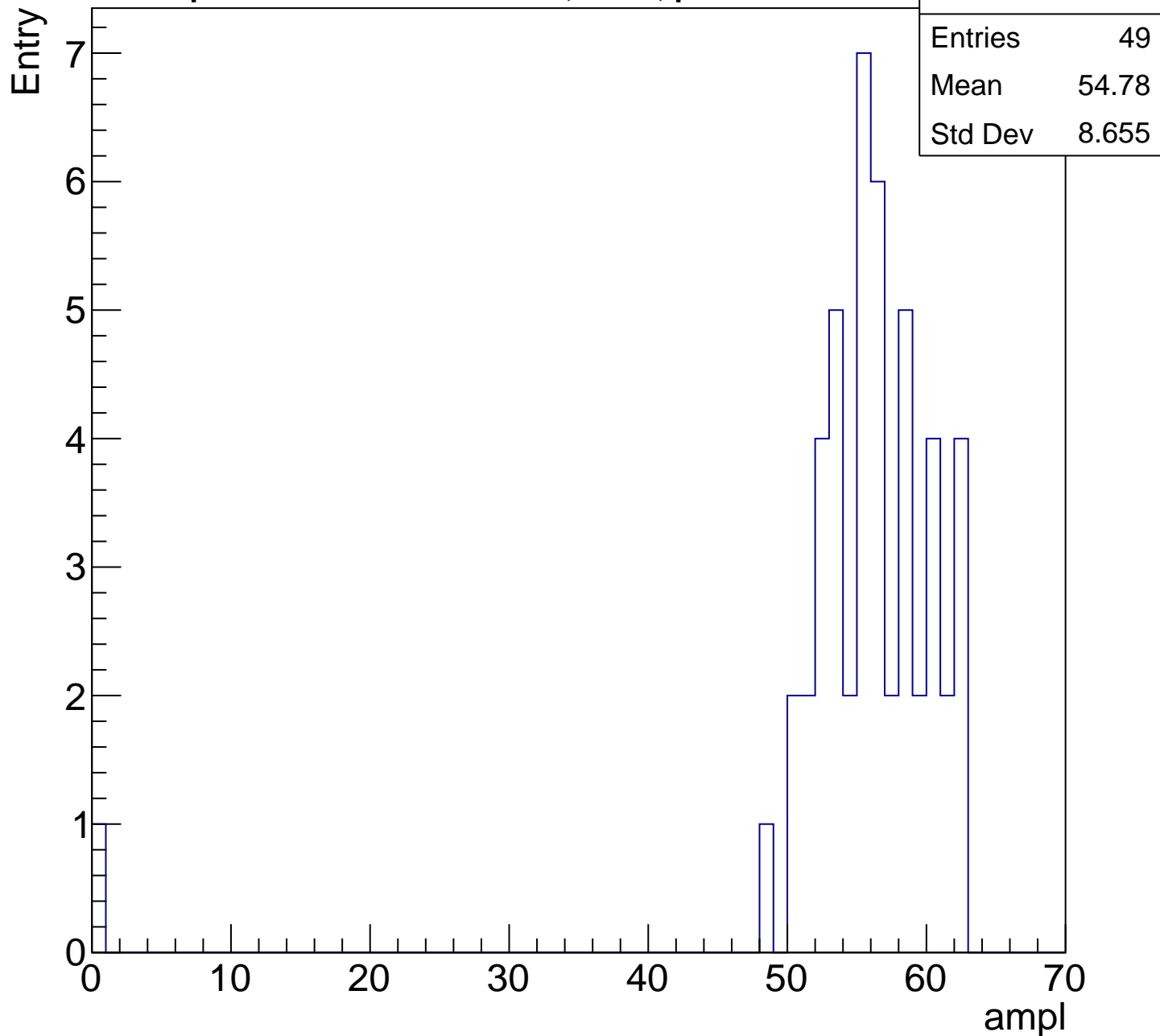
Entry

Entries	68
Mean	50.99
Std Dev	3.886



# B1L103S, U21-ch19, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U21-ch19, adc5

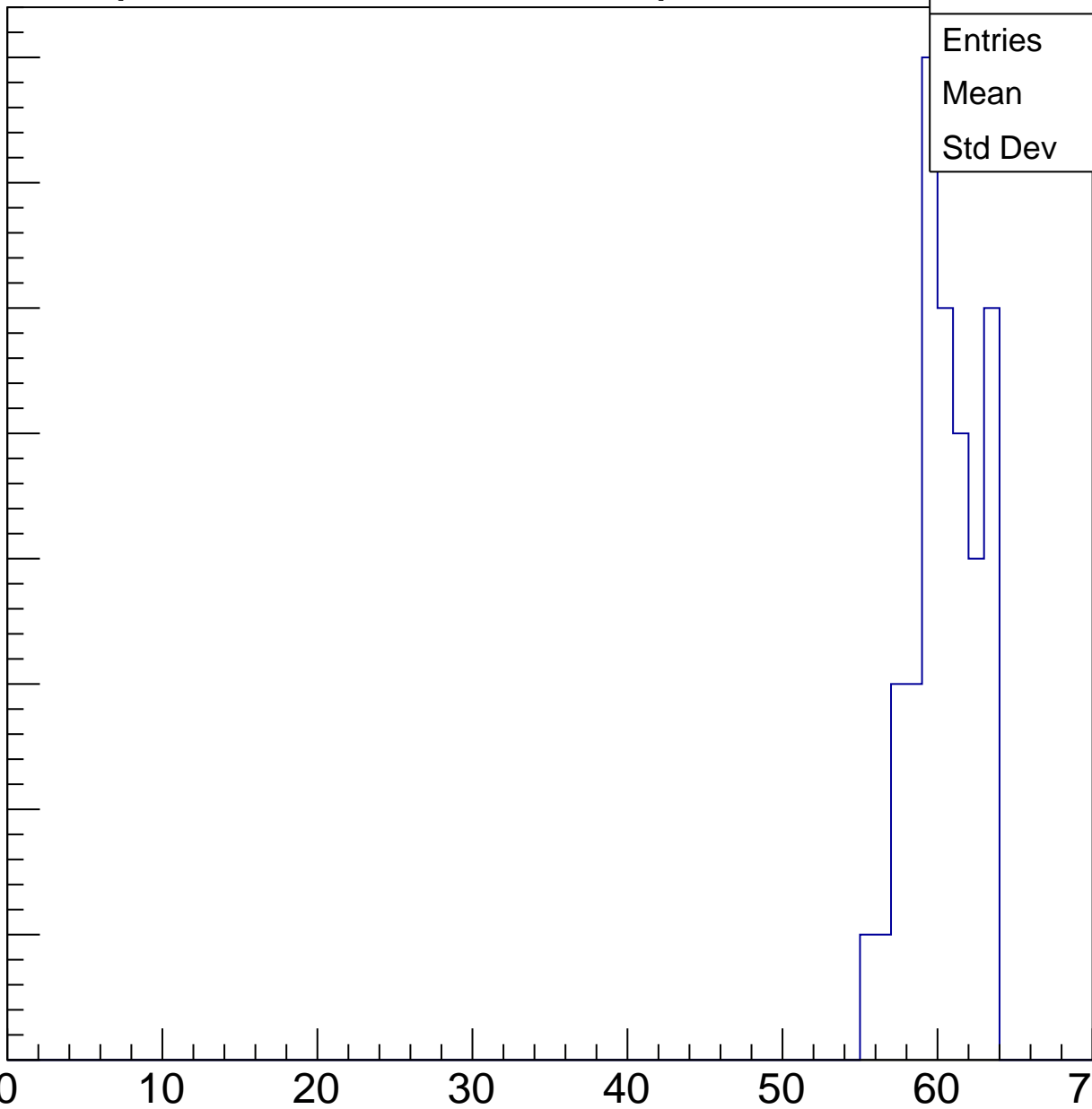
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	37
Mean	59.97
Std Dev	2.099

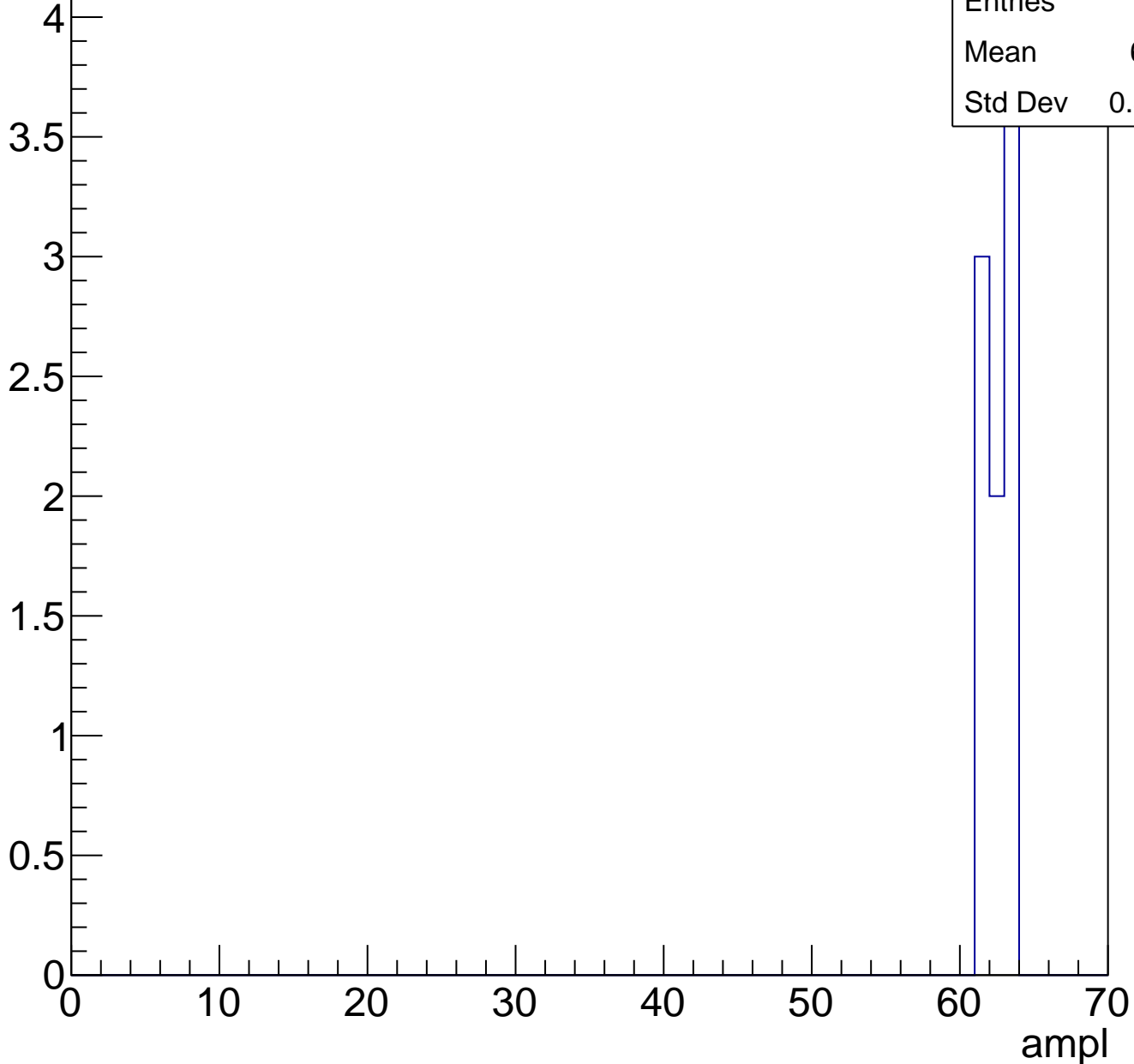
ampl



# B1L103S, U21-ch19, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U21-ch19, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U21-ch20, adc0

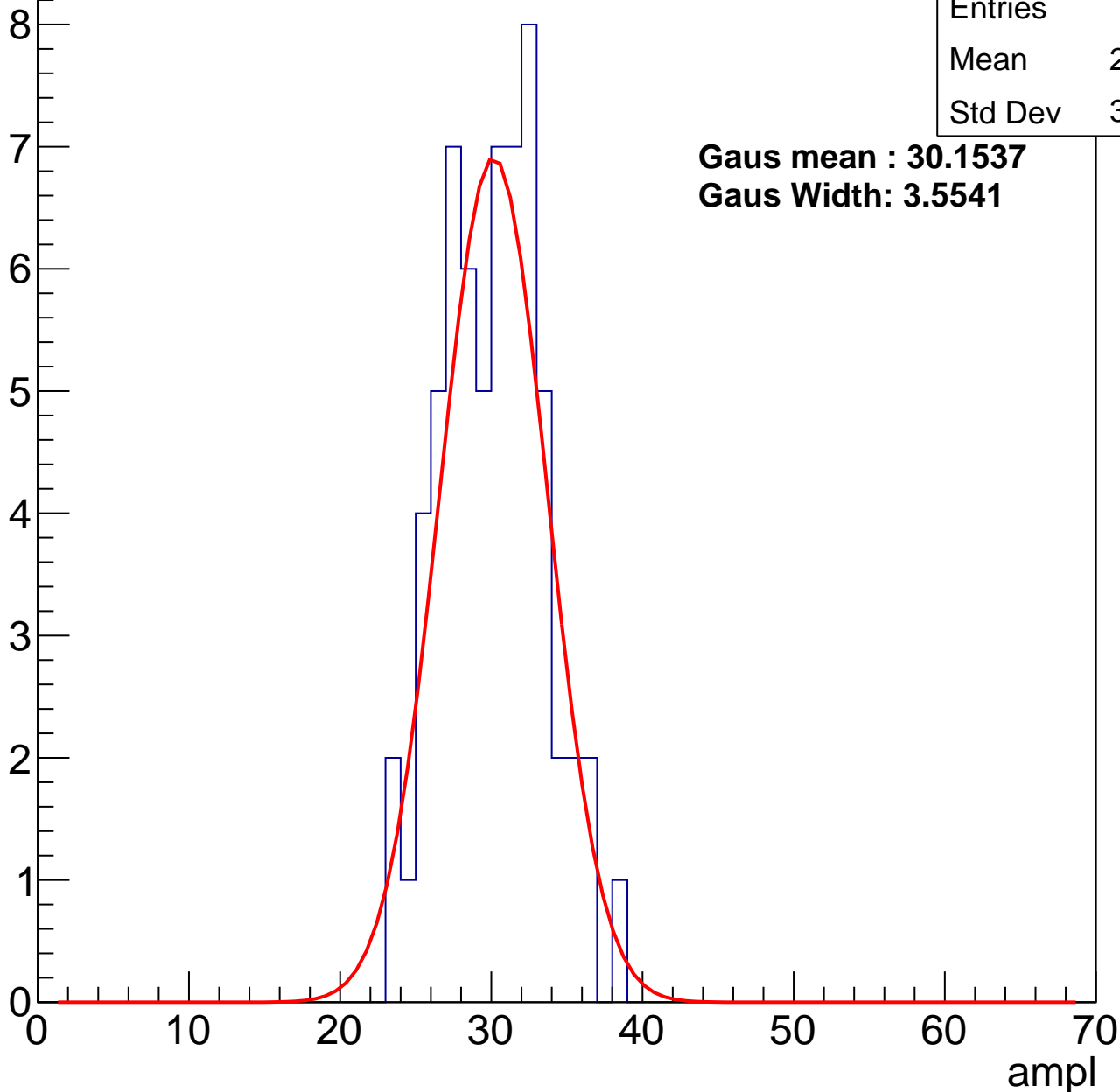
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	29.66
Std Dev	3.308

**Gaus mean : 30.1537**

**Gaus Width: 3.5541**



# B1L103S, U21-ch20, adc1

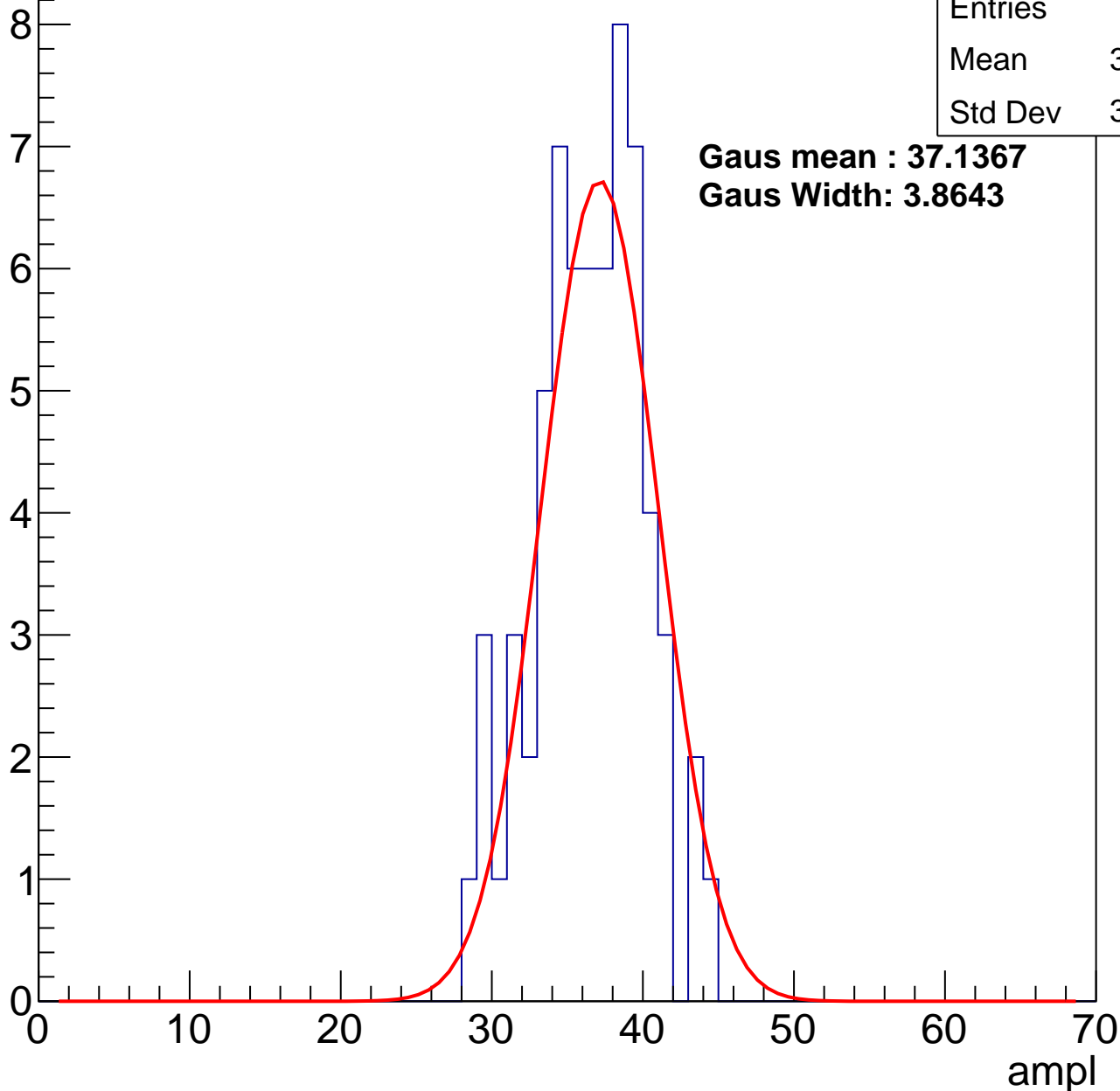
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	36.05
Std Dev	3.584

**Gaus mean : 37.1367**

**Gaus Width: 3.8643**



# B1L103S, U21-ch20, adc2

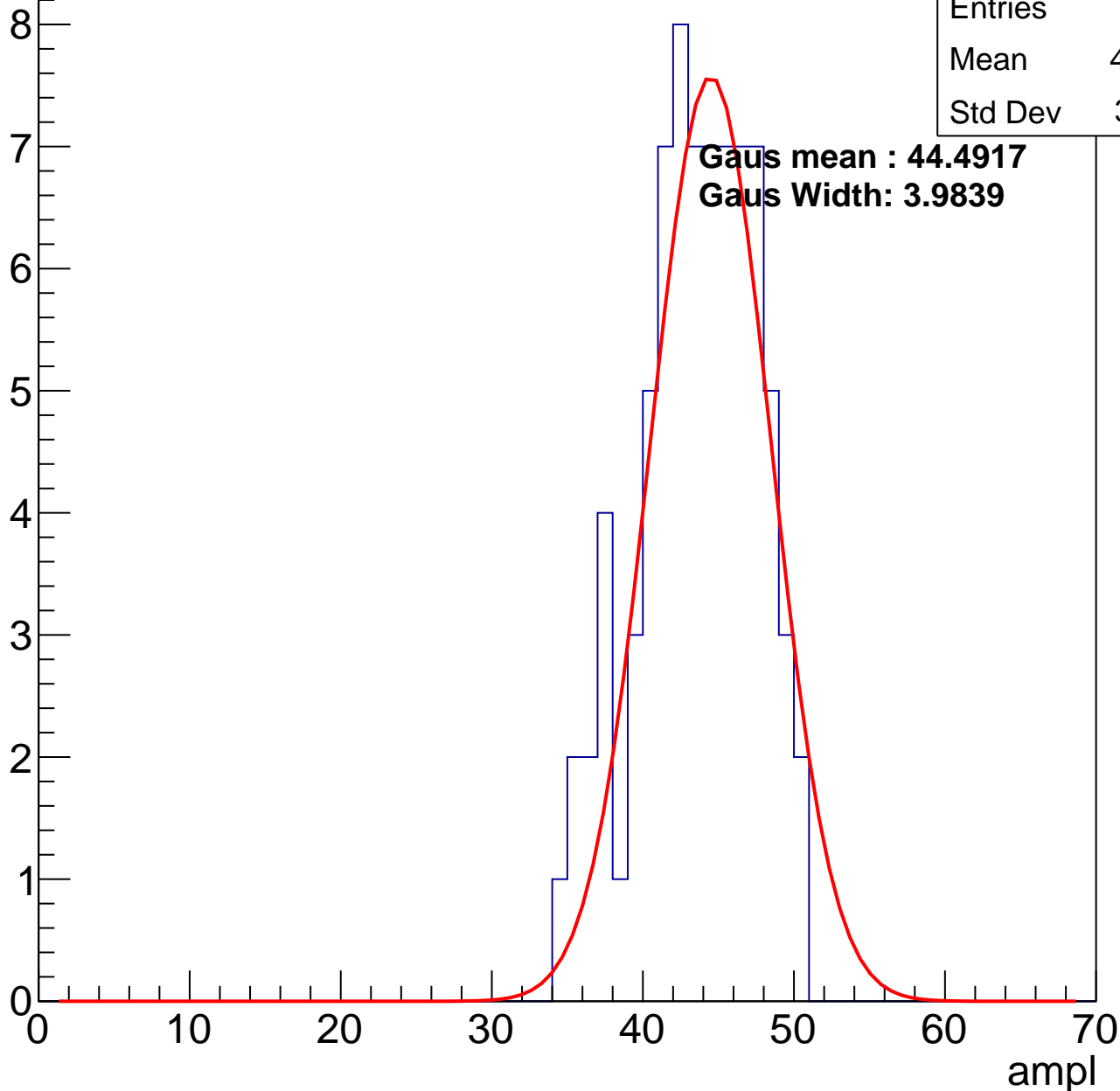
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	43.13
Std Dev	3.831

**Gaus mean : 44.4917**

**Gaus Width: 3.9839**

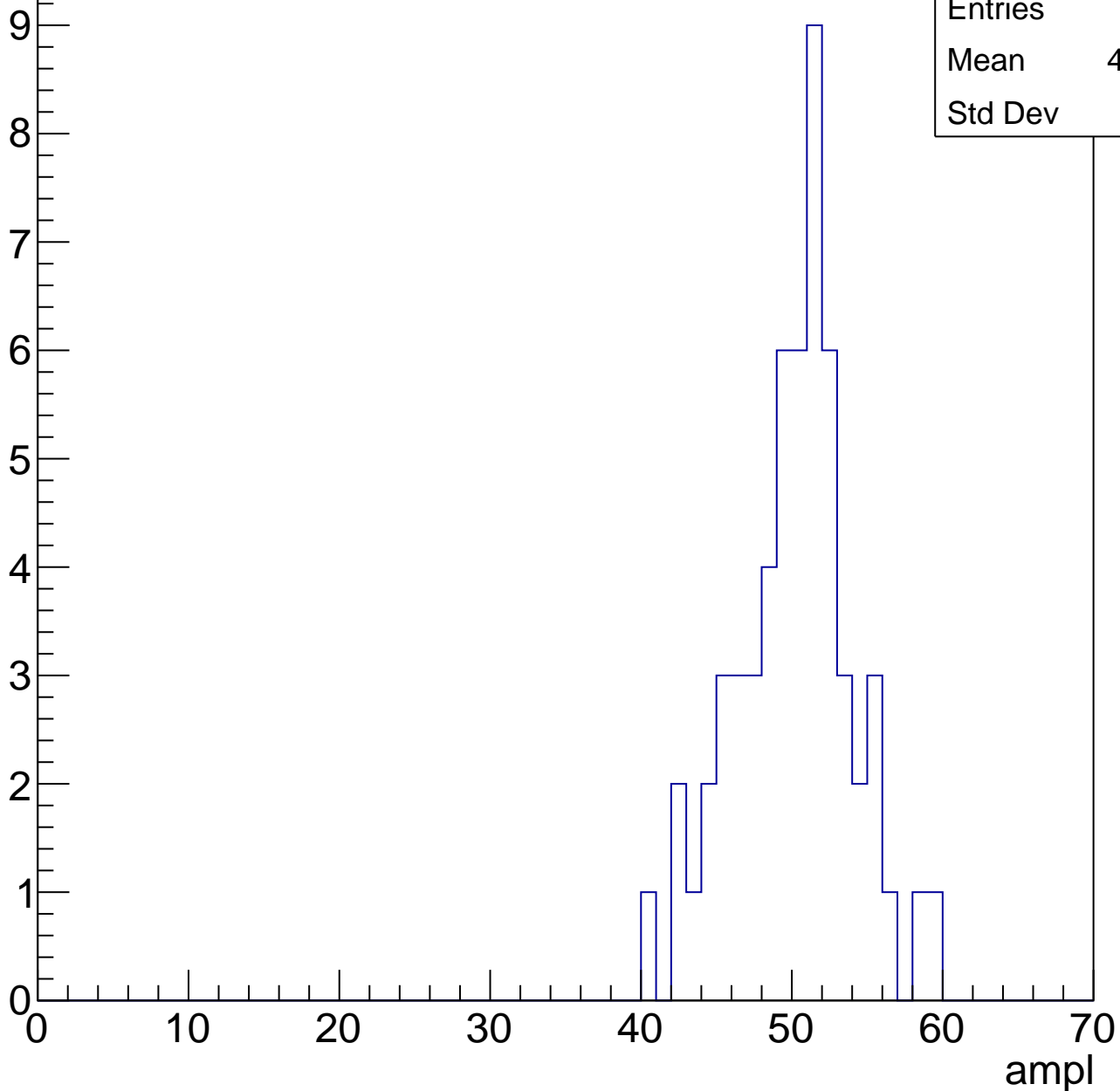


# B1L103S, U21-ch20, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	49.67
Std Dev	3.89

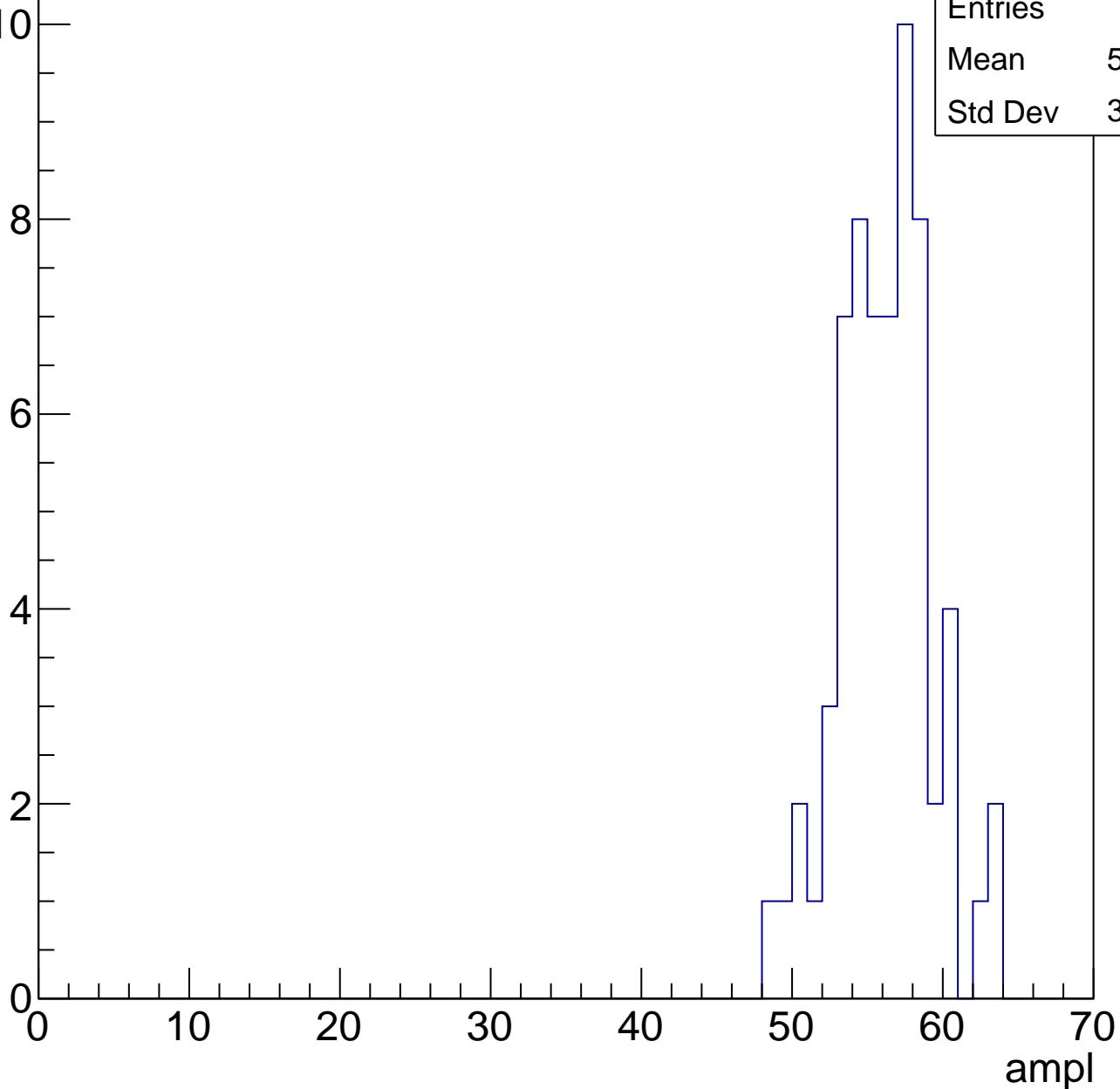


# B1L103S, U21-ch20, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	55.69
Std Dev	3.092

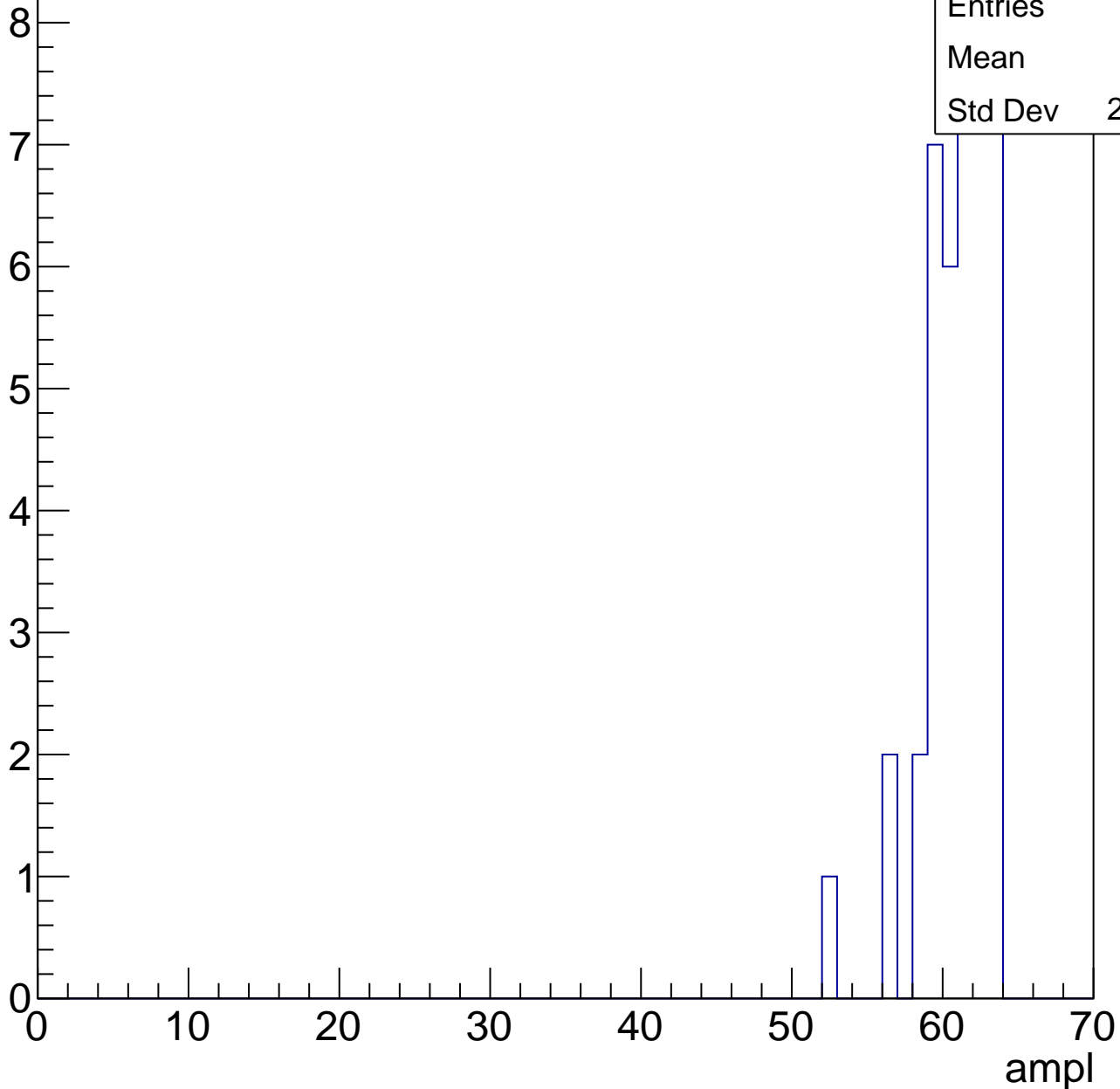


# B1L103S, U21-ch20, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

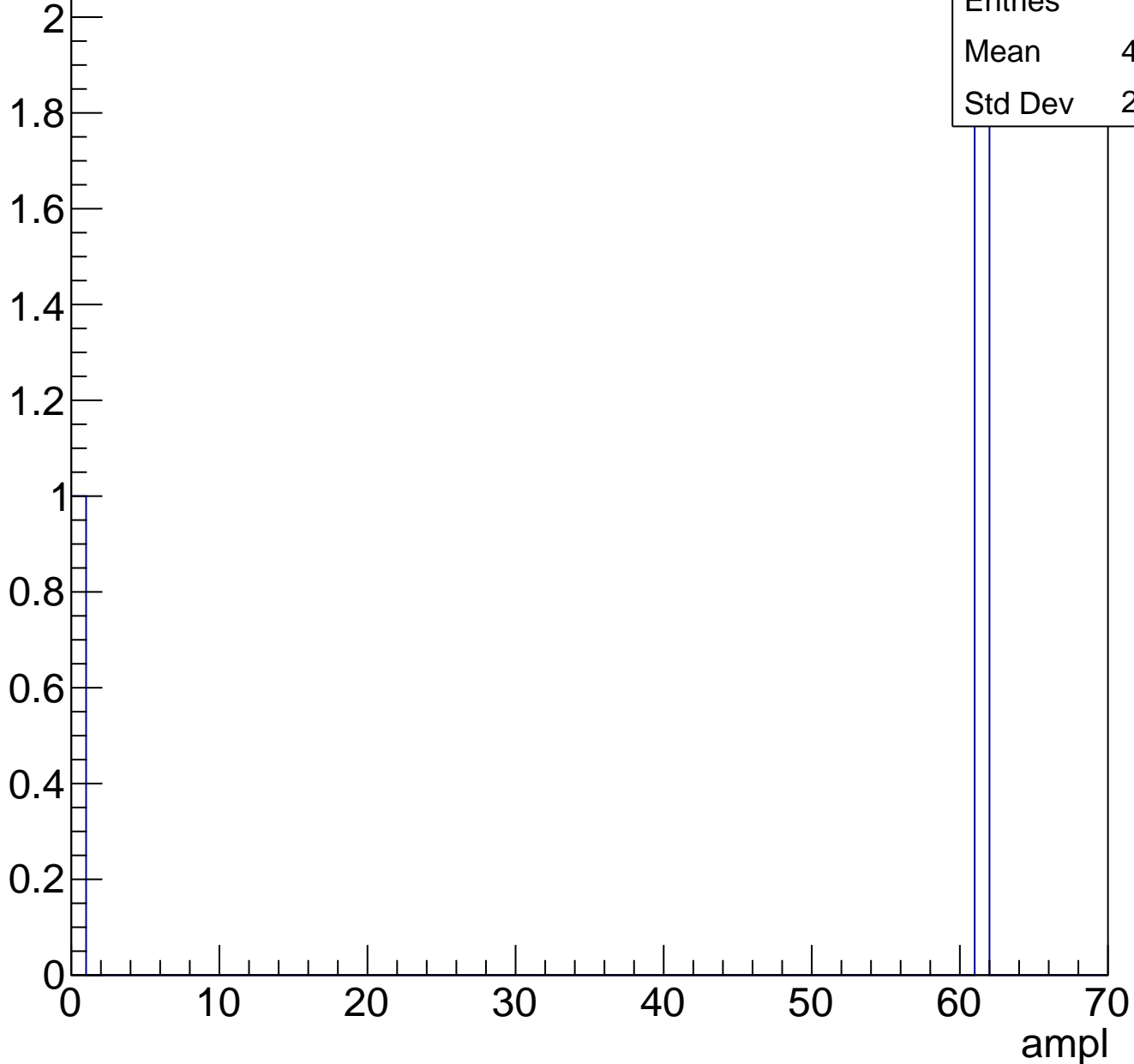
Entries	42
Mean	60.5
Std Dev	2.249



# B1L103S, U21-ch20, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U21-ch20, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U21-ch21, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	60
Mean	30.28
Std Dev	5.216

**Gaus mean : 31.1293**

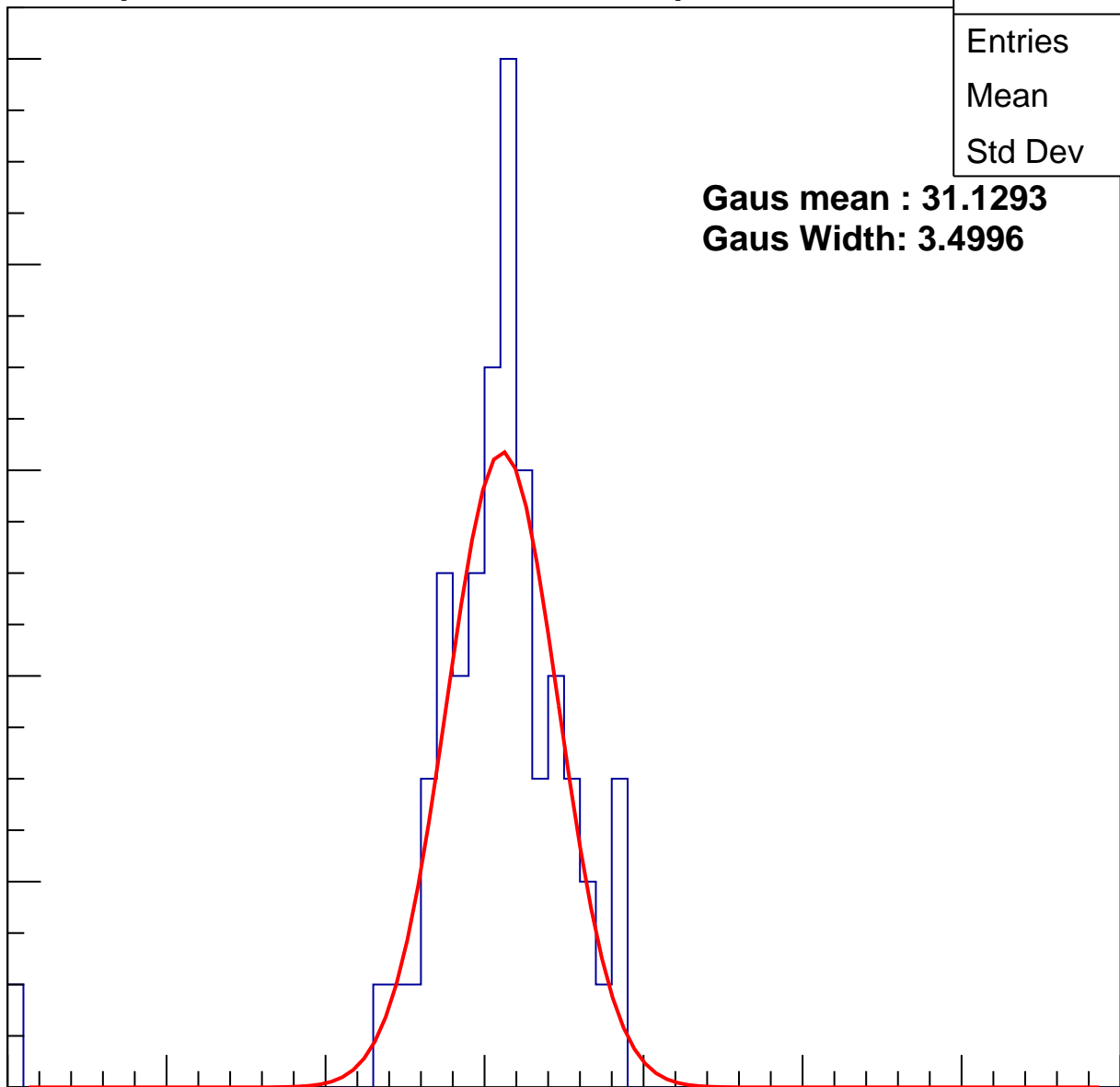
**Gaus Width: 3.4996**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U21-ch21, adc1

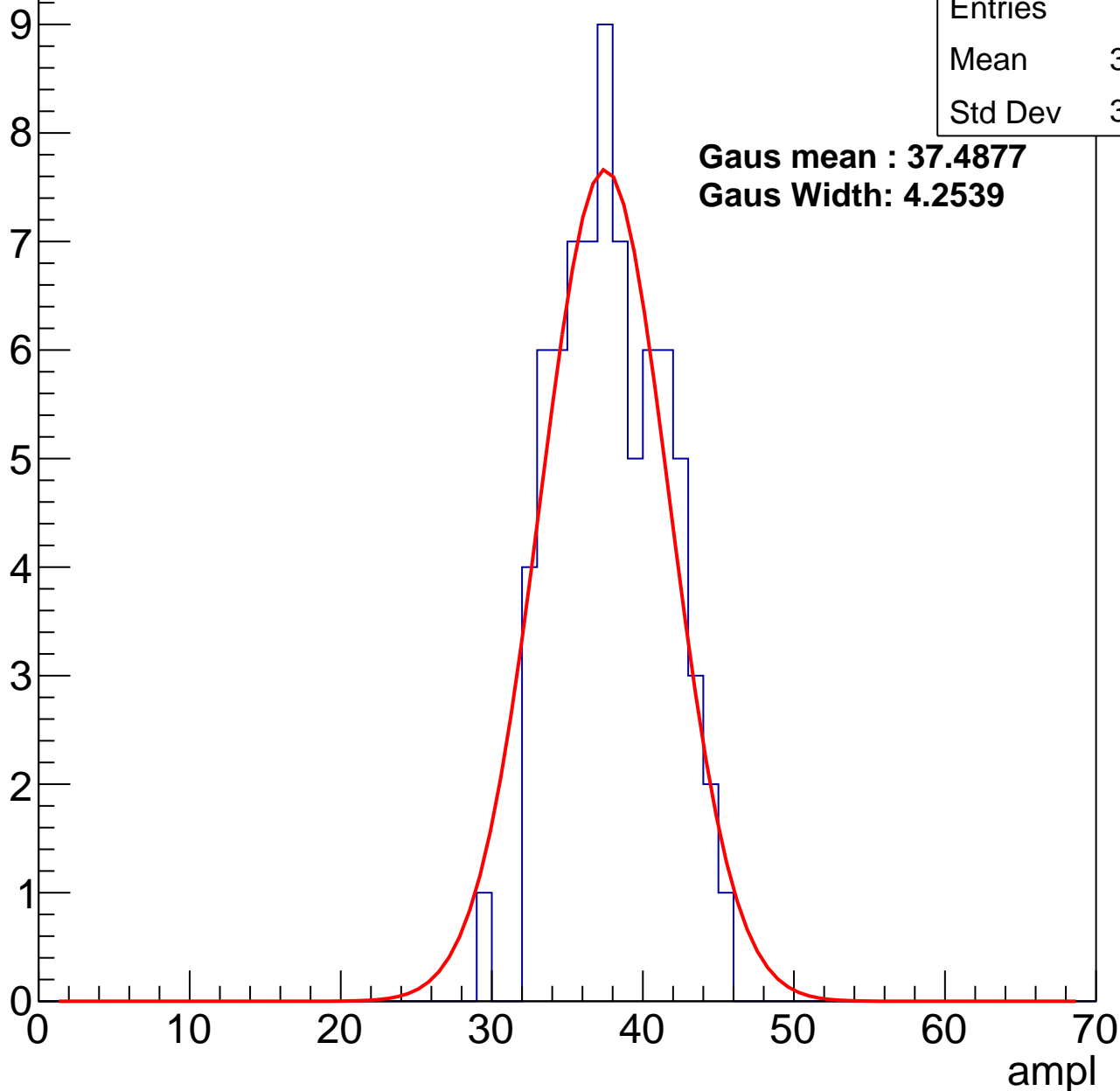
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	37.44
Std Dev	3.477

**Gaus mean : 37.4877**

**Gaus Width: 4.2539**



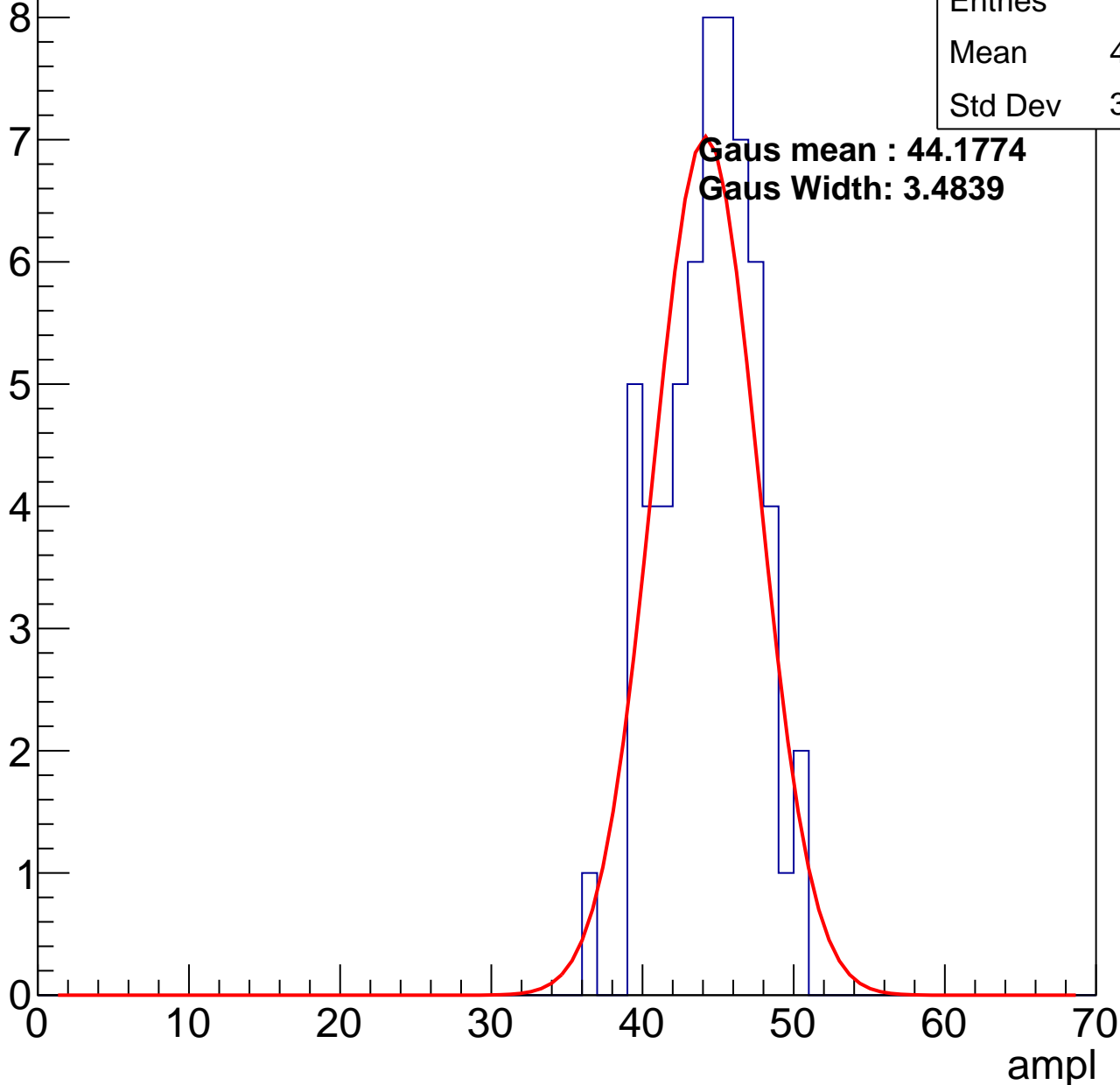
# B1L103S, U21-ch21, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	43.93
Std Dev	3.045

**Gaus mean : 44.1774**  
**Gaus Width: 3.4839**

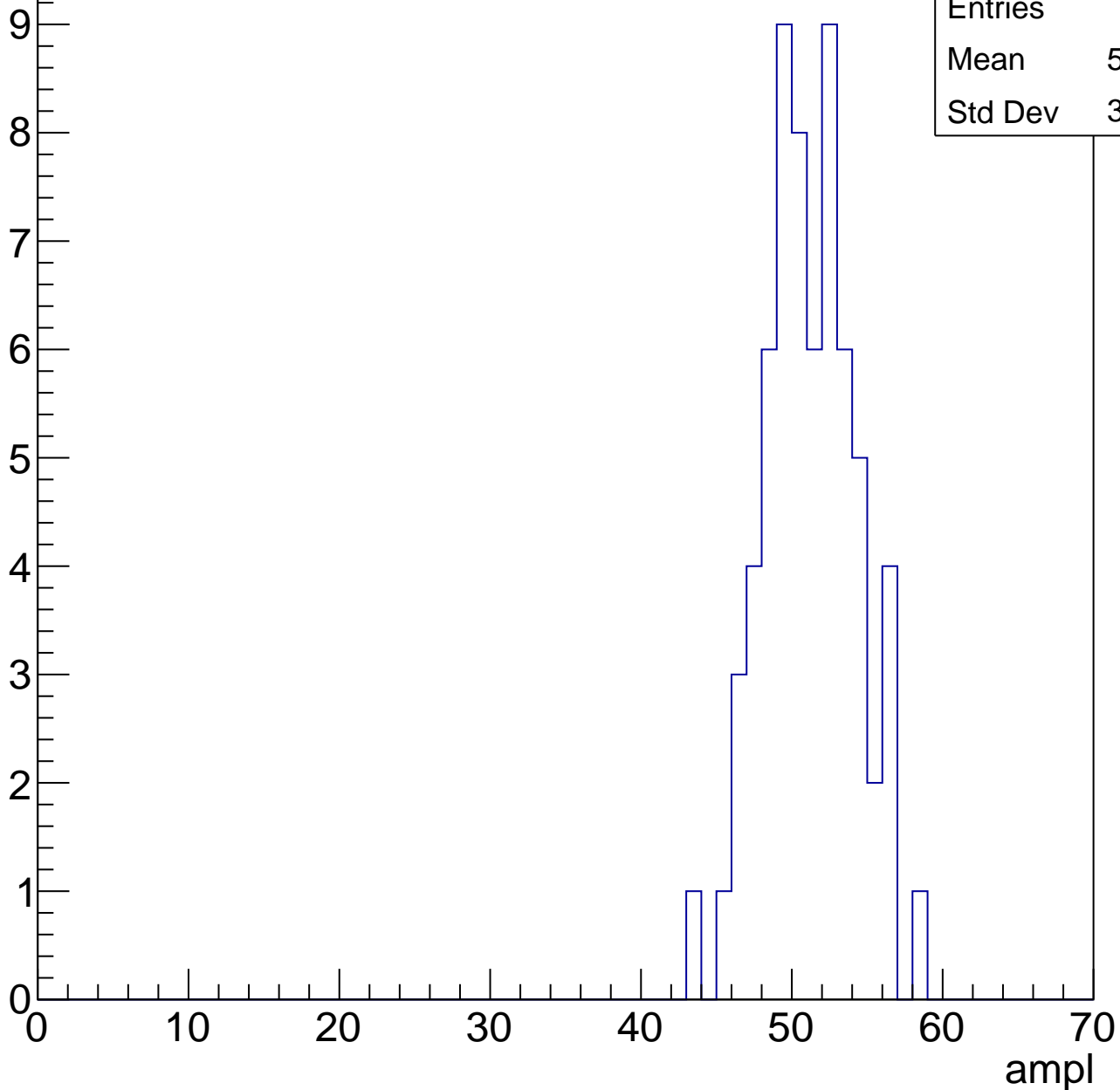


# B1L103S, U21-ch21, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	50.72
Std Dev	3.015

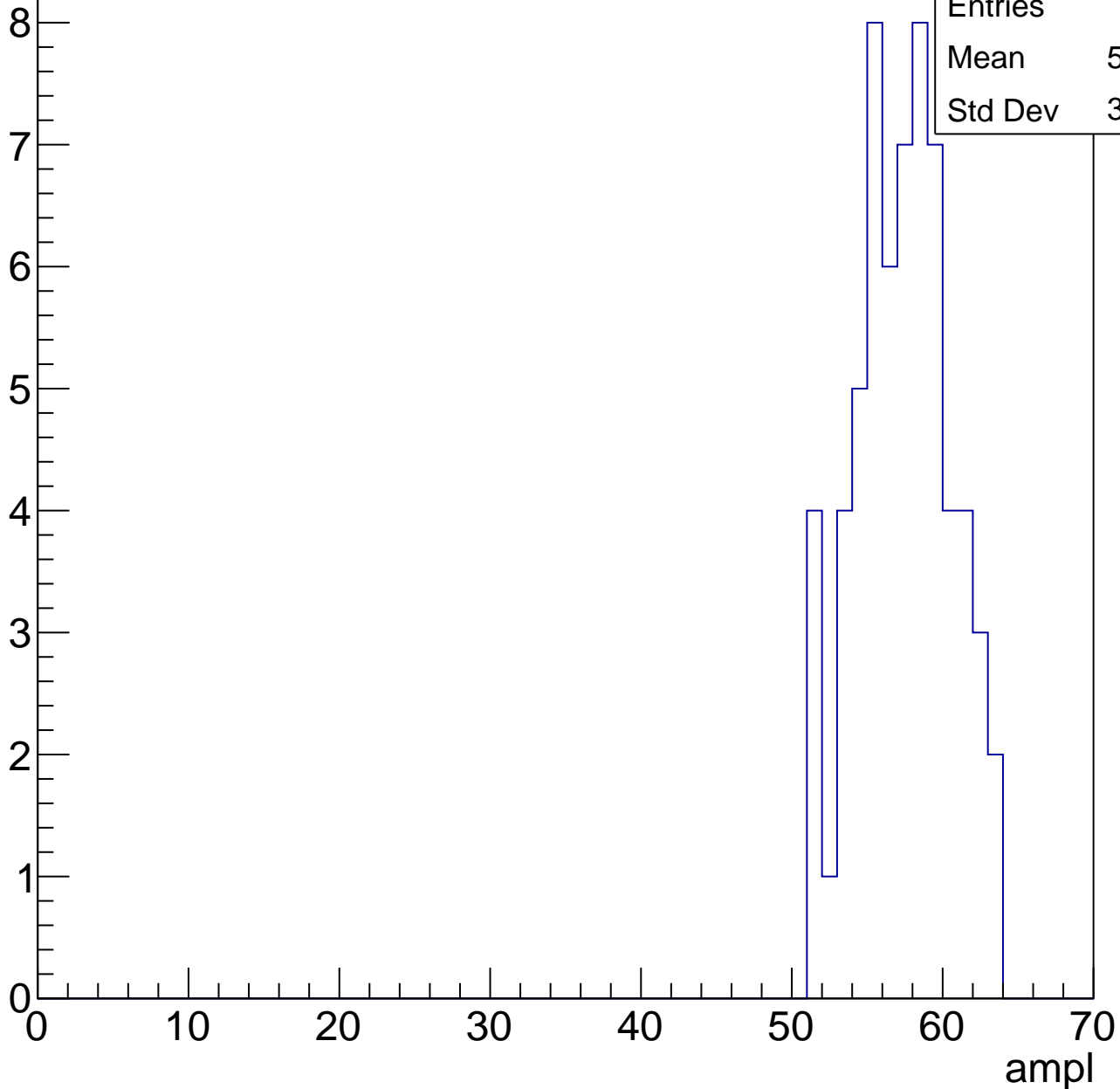


# B1L103S, U21-ch21, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	56.92
Std Dev	3.082

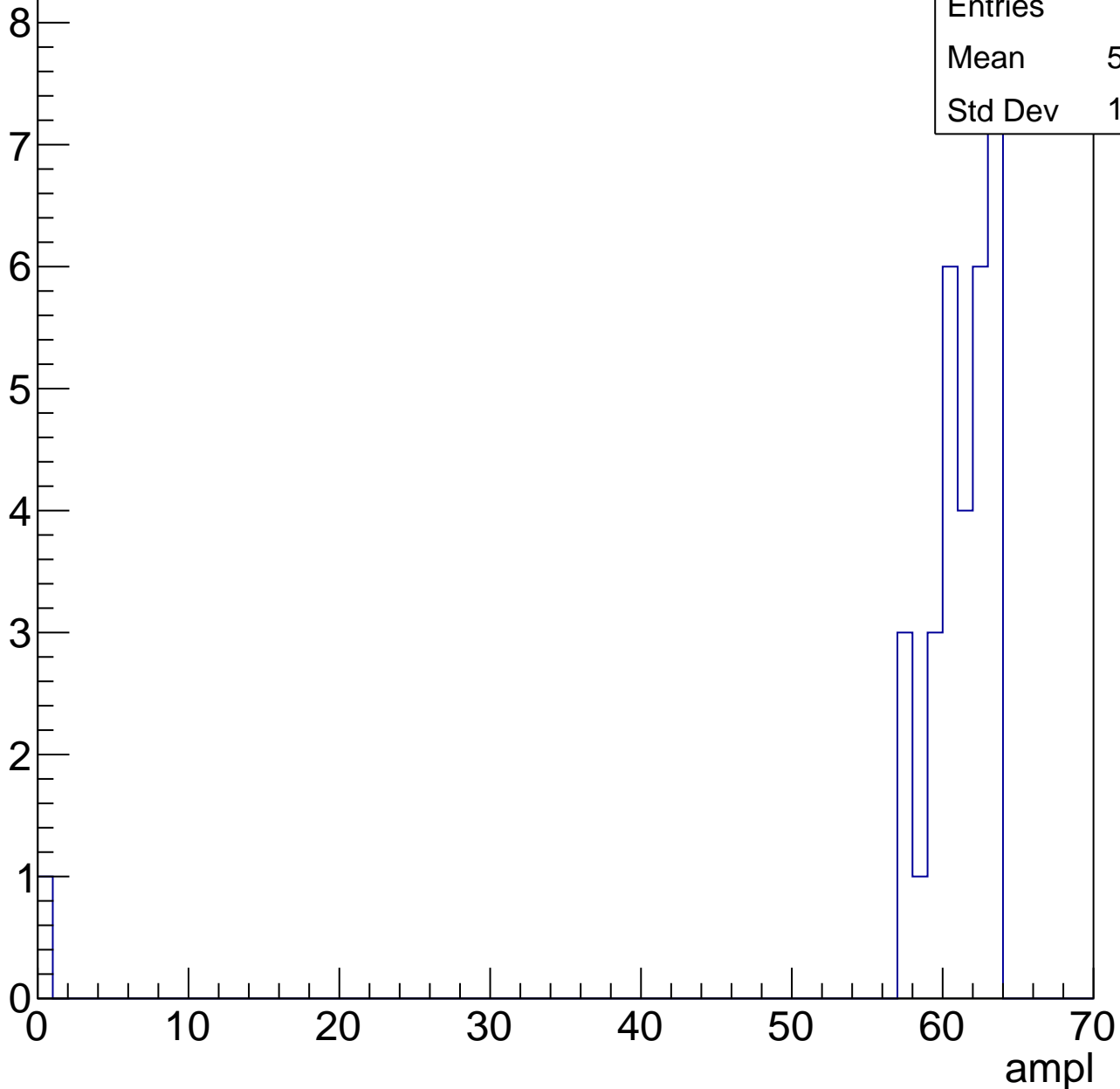


# B1L103S, U21-ch21, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	32
Mean	58.94
Std Dev	10.75



# B1L103S, U21-ch21, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	61.33
Std Dev	0.4714

ampl

0 10 20 30 40 50 60 70



# B1L103S, U21-ch21, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U21-ch22, adc0

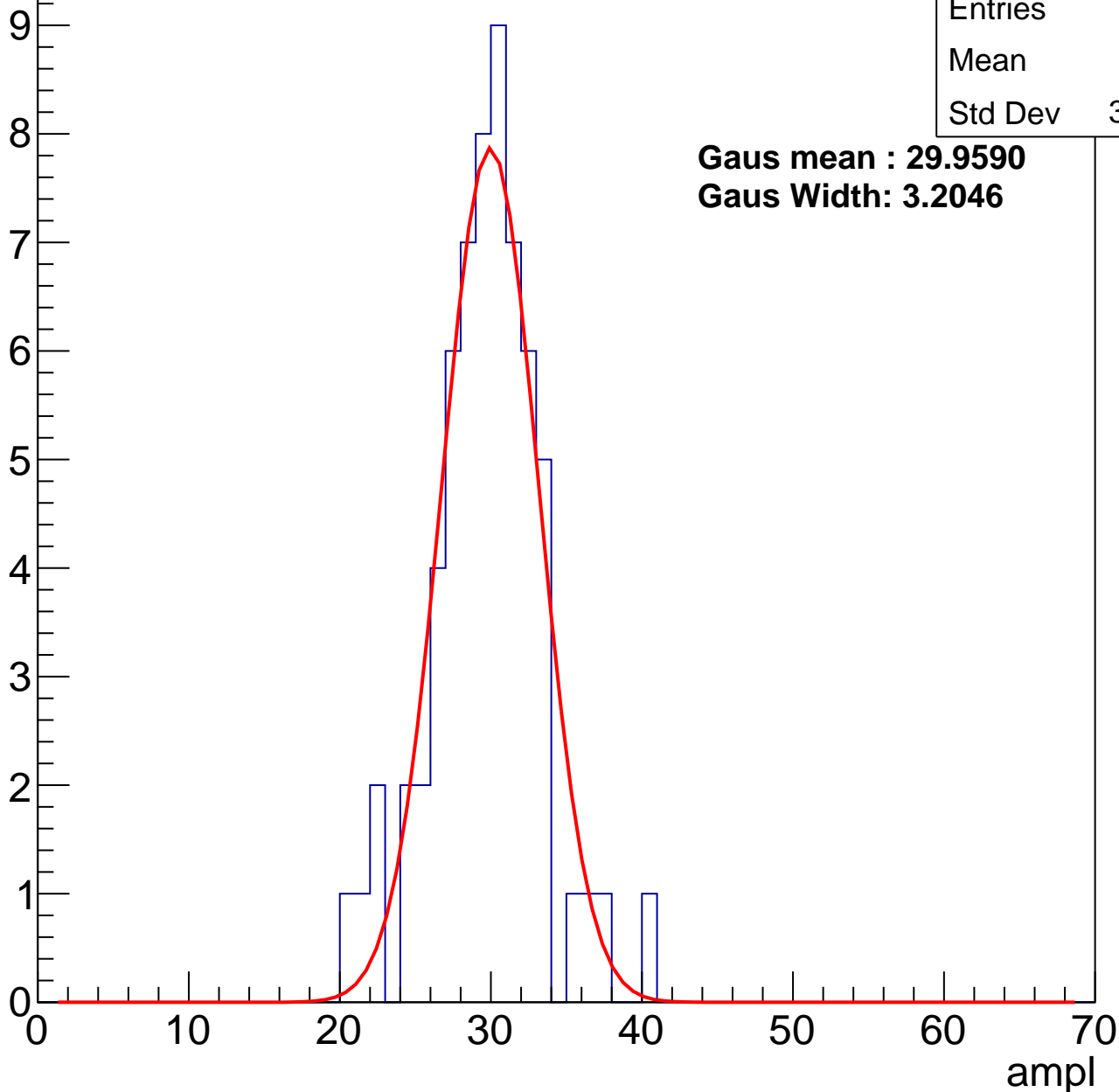
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	29.2
Std Dev	3.602

**Gaus mean : 29.9590**

**Gaus Width: 3.2046**



# B1L103S, U21-ch22, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	79
Mean	35.84
Std Dev	3.96

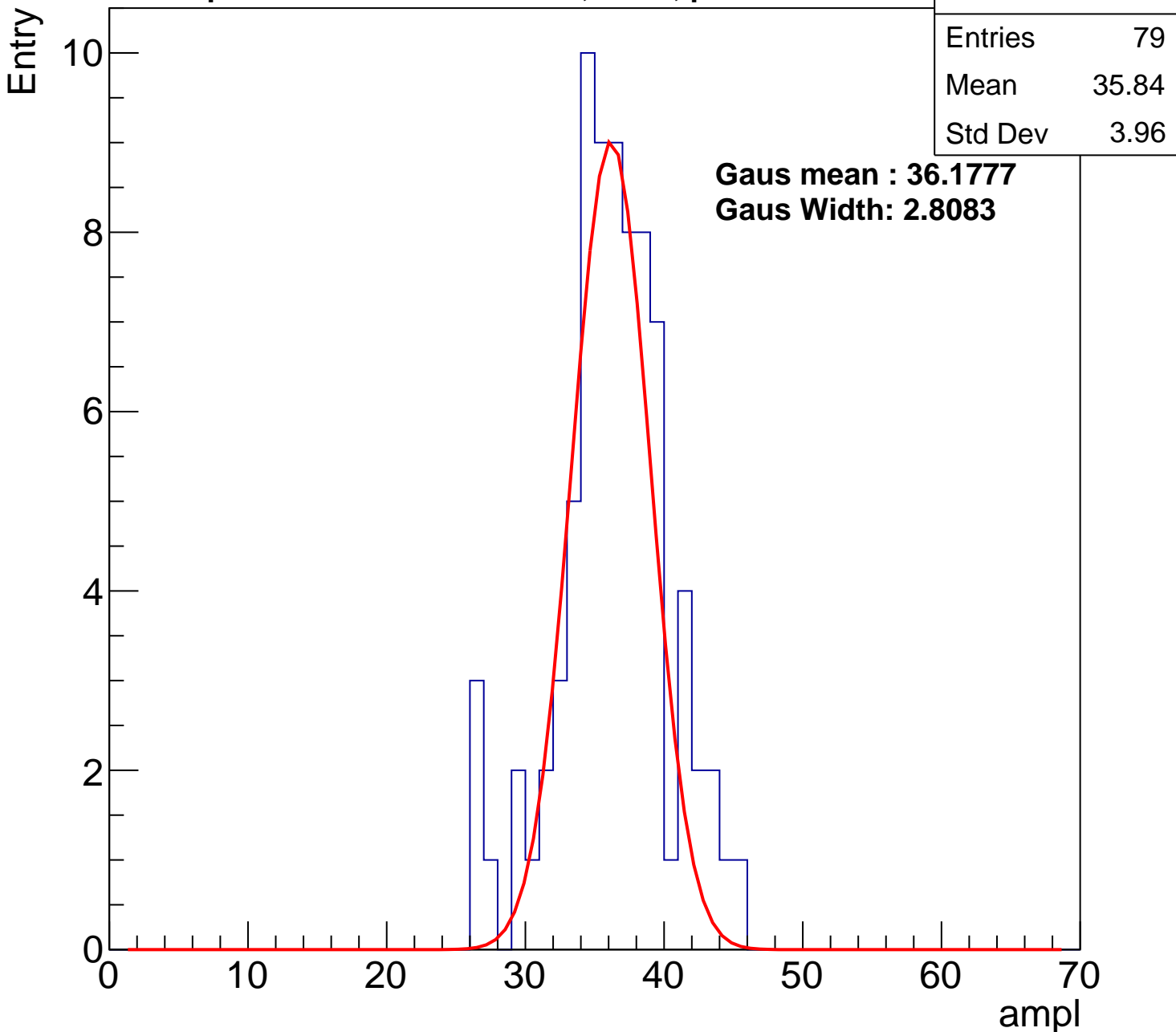
**Gaus mean : 36.1777**  
**Gaus Width: 2.8083**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U21-ch22, adc2

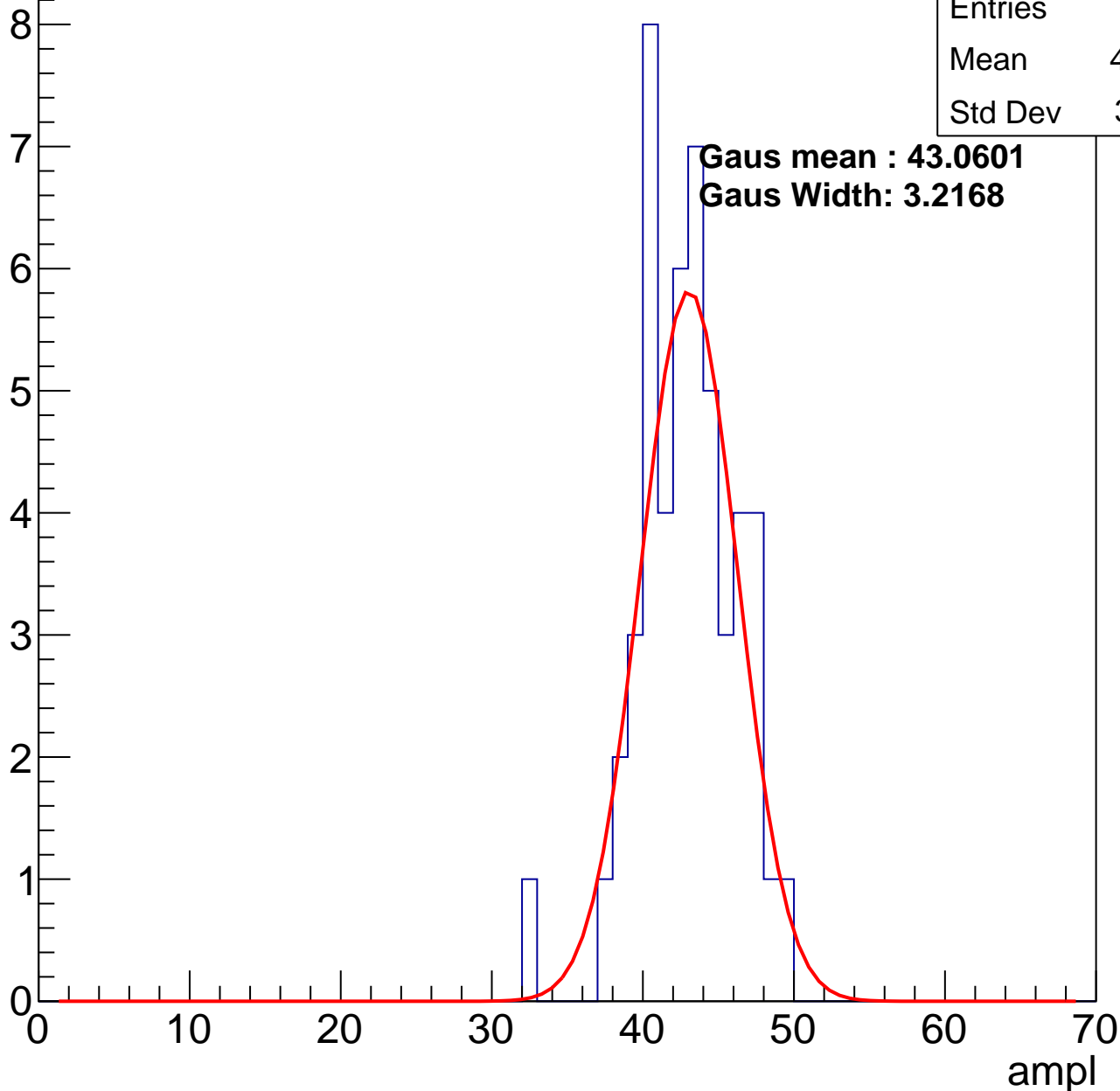
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	42.46
Std Dev	3.201

**Gaus mean : 43.0601**

**Gaus Width: 3.2168**

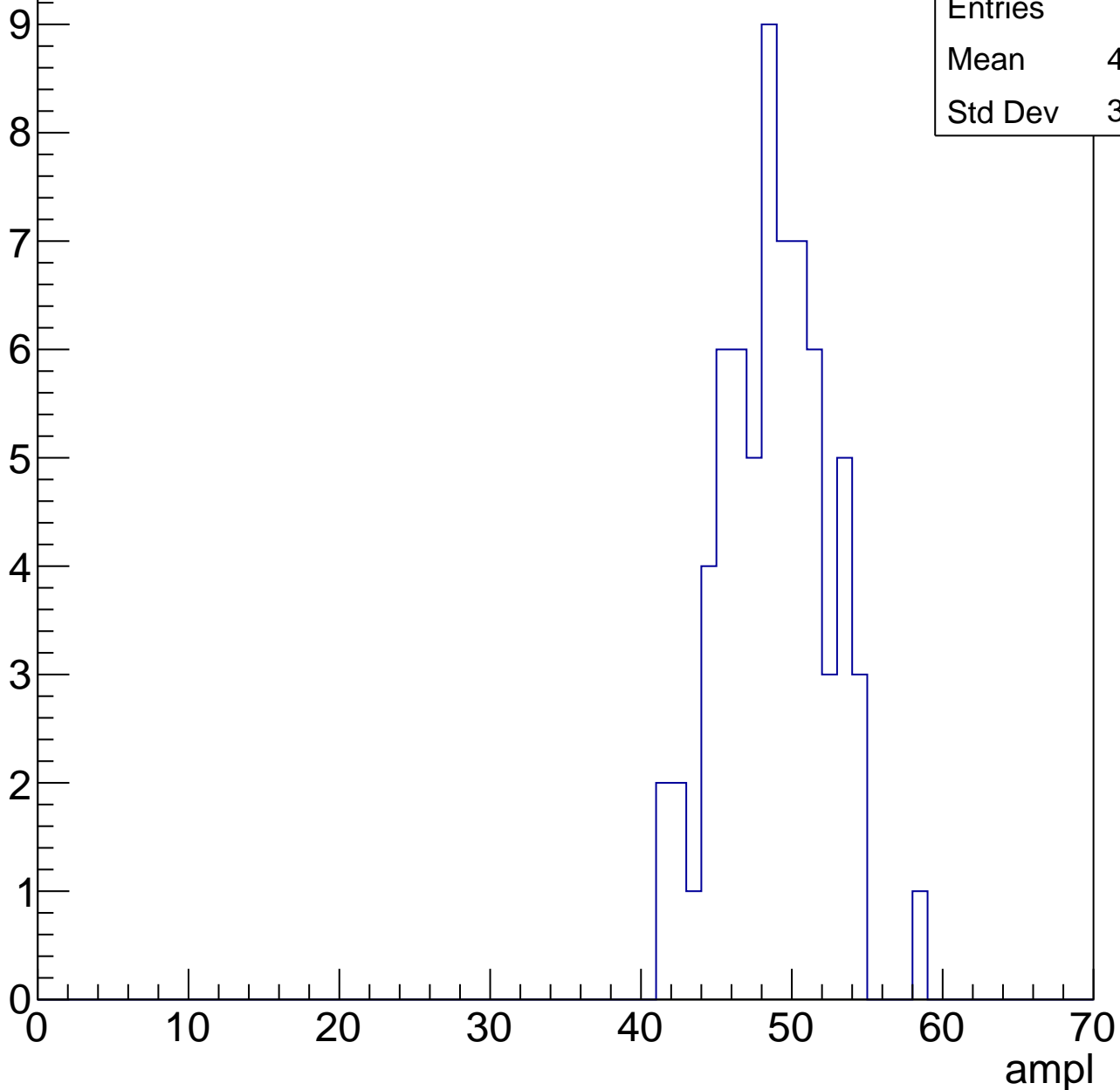


# B1L103S, U21-ch22, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	48.33
Std Dev	3.466

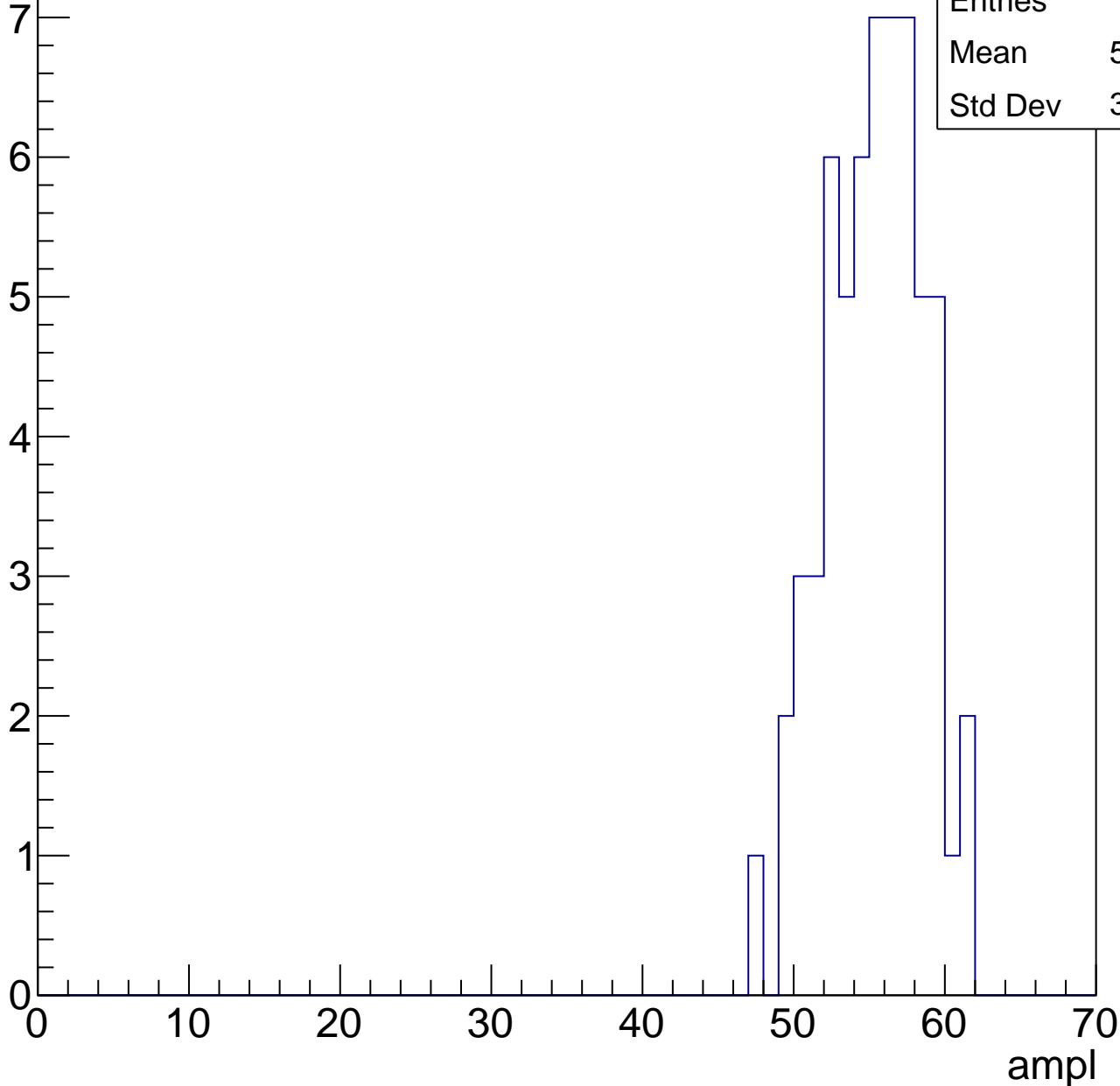


# B1L103S, U21-ch22, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	54.87
Std Dev	3.149

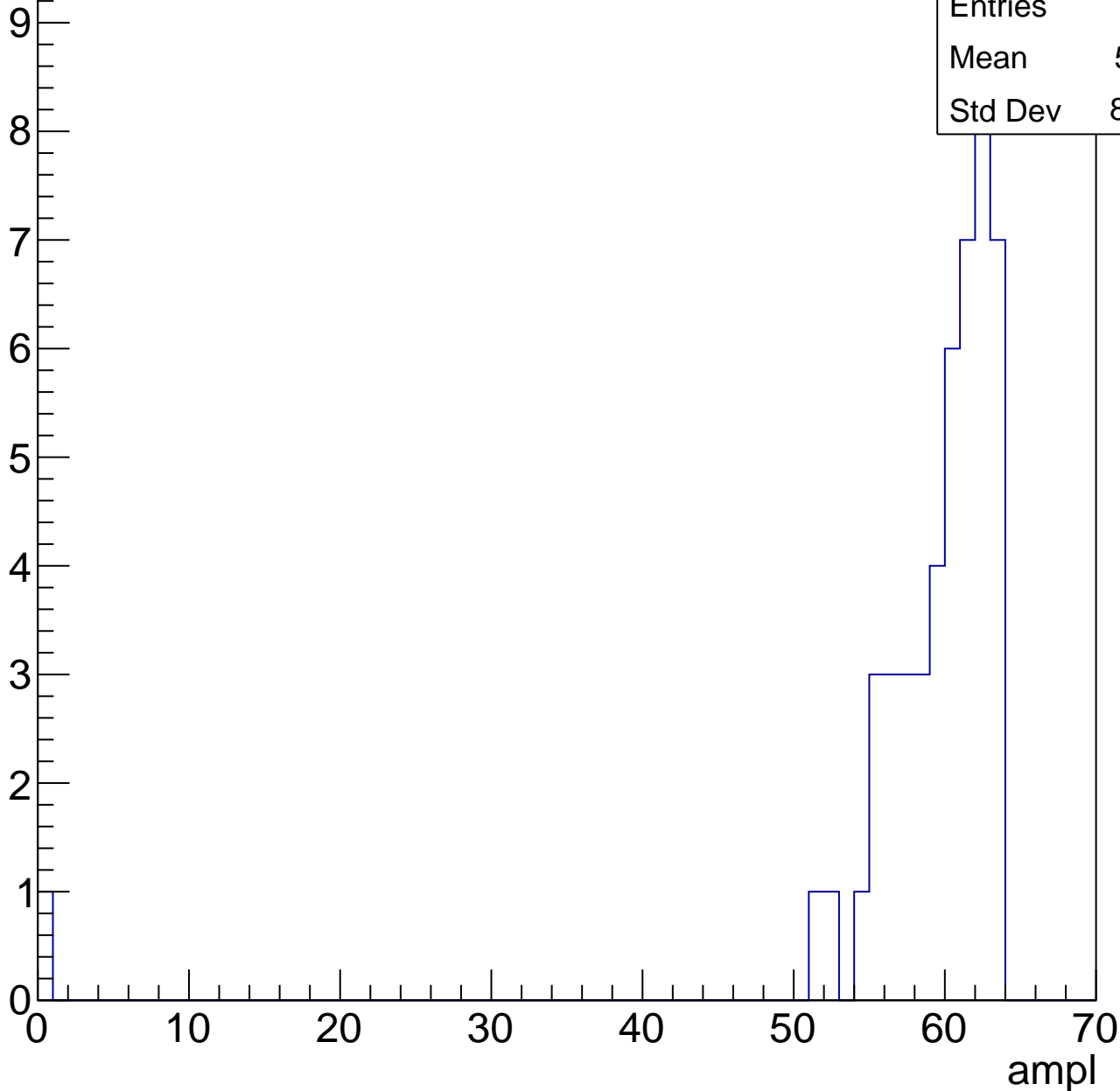


# B1L103S, U21-ch22, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	58.31
Std Dev	8.936



# B1L103S, U21-ch22, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

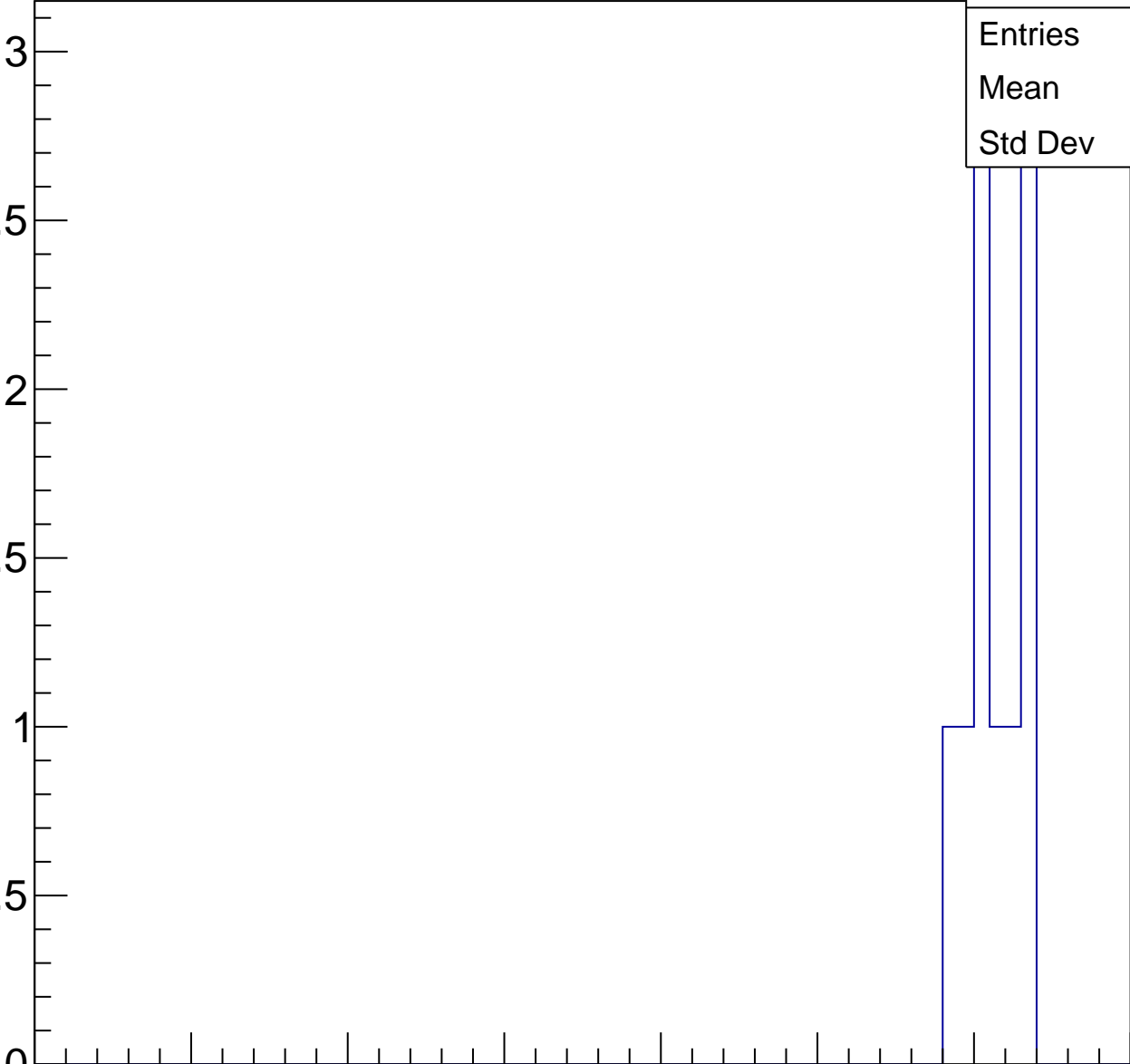
Entry

3  
2.5  
2  
1.5  
1  
0.5  
0

Entries	10
Mean	60.9
Std Dev	1.7

ampl

0 10 20 30 40 50 60 70





# B1L103S, U21-ch22, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	20
Std Dev	0

# B1L103S, U21-ch23, adc0

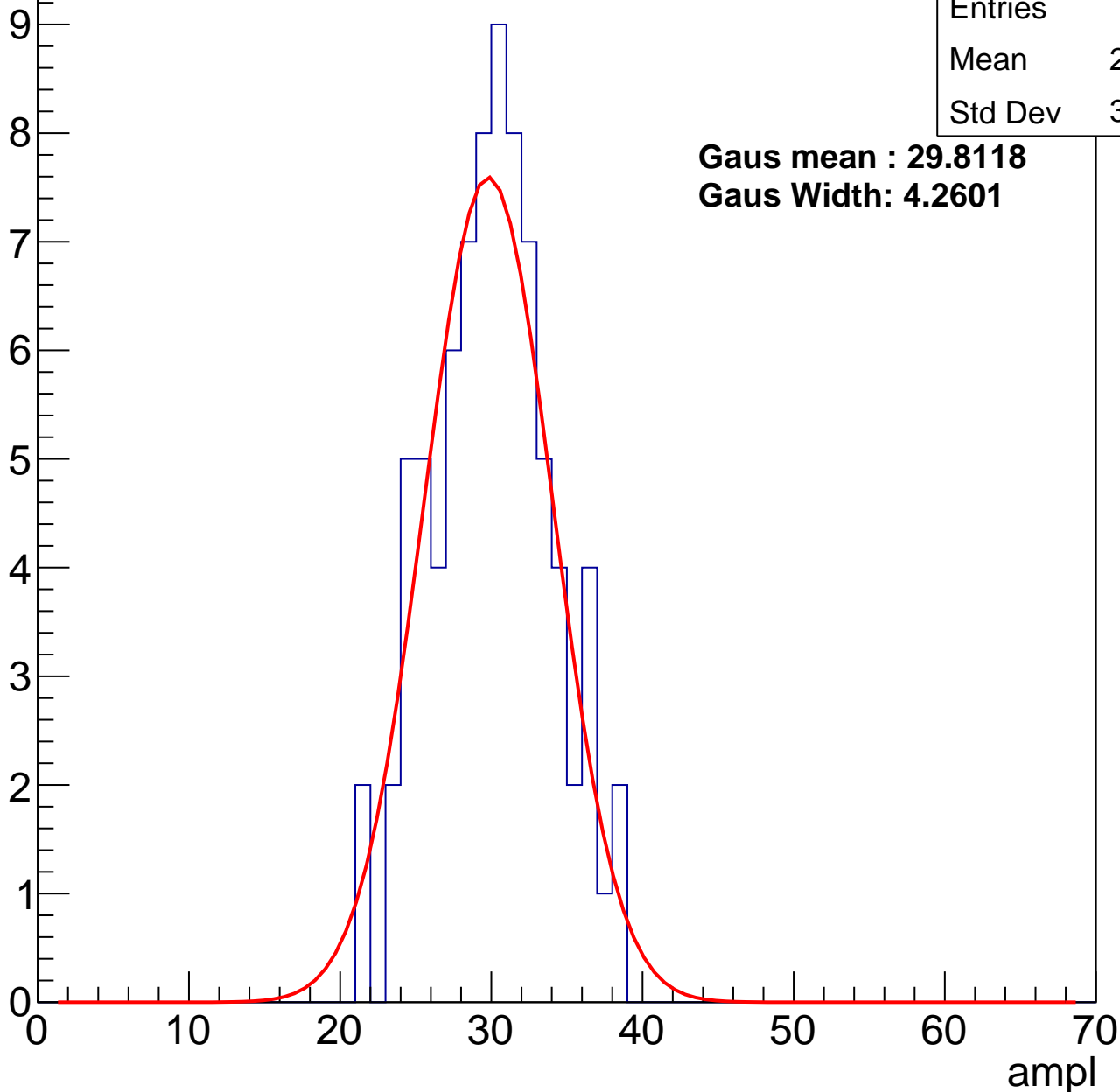
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	81
Mean	29.59
Std Dev	3.883

**Gaus mean : 29.8118**

**Gaus Width: 4.2601**



# B1L103S, U21-ch23, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	69
Mean	37.09
Std Dev	3.331

**Gaus mean : 37.3809**

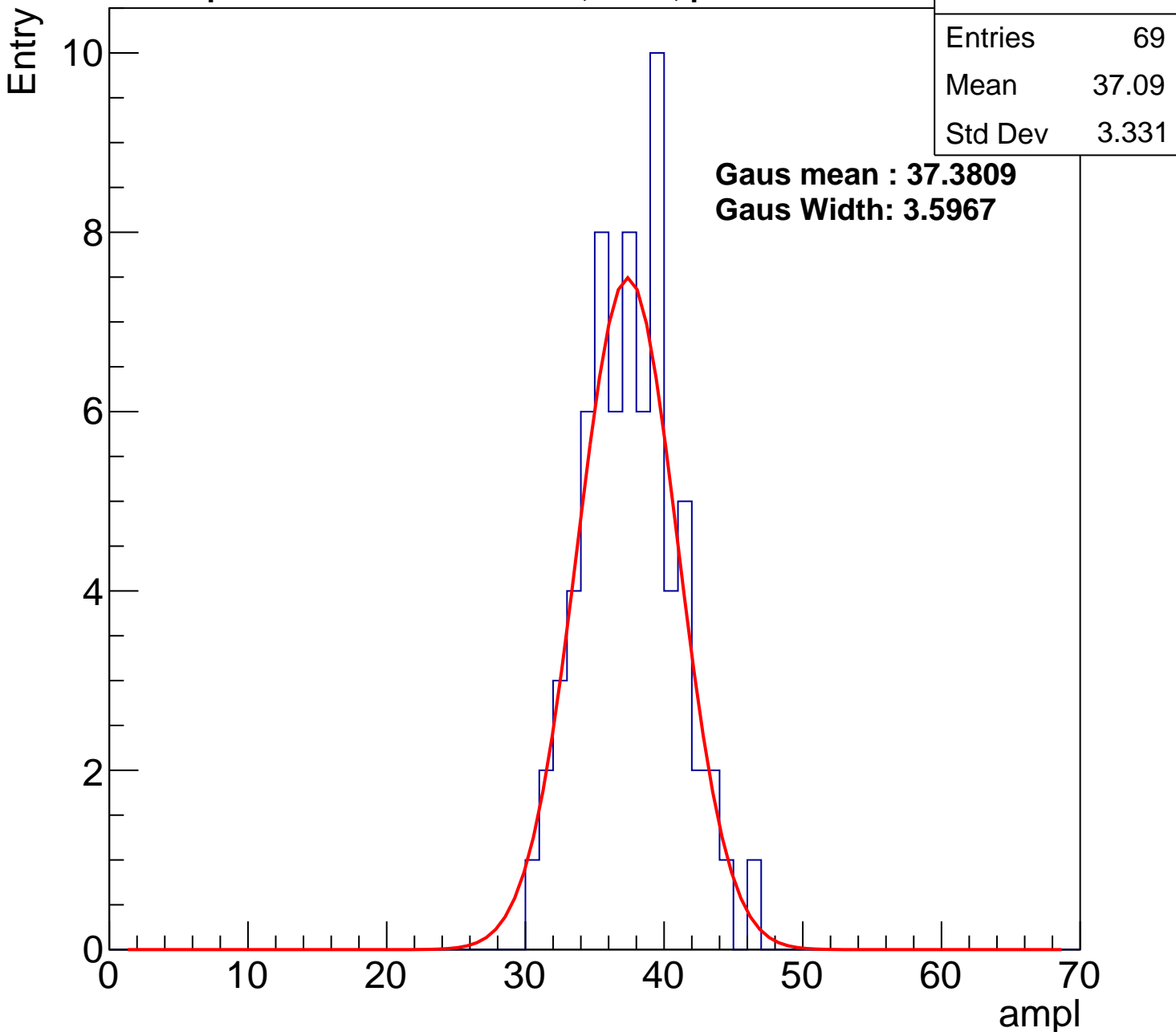
**Gaus Width: 3.5967**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U21-ch23, adc2

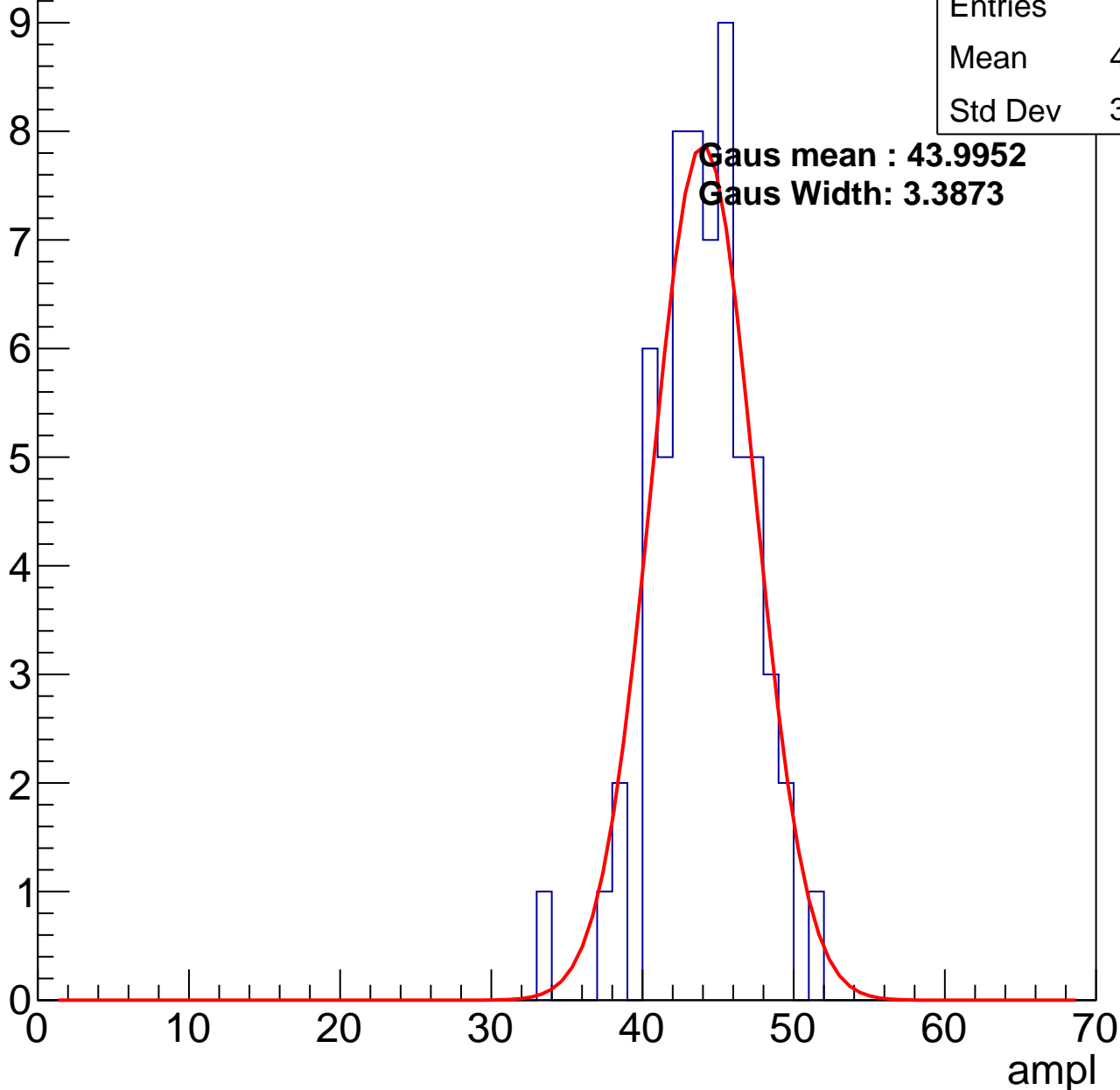
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	43.52
Std Dev	3.162

**Gaus mean : 43.9952**

**Gaus Width: 3.3873**

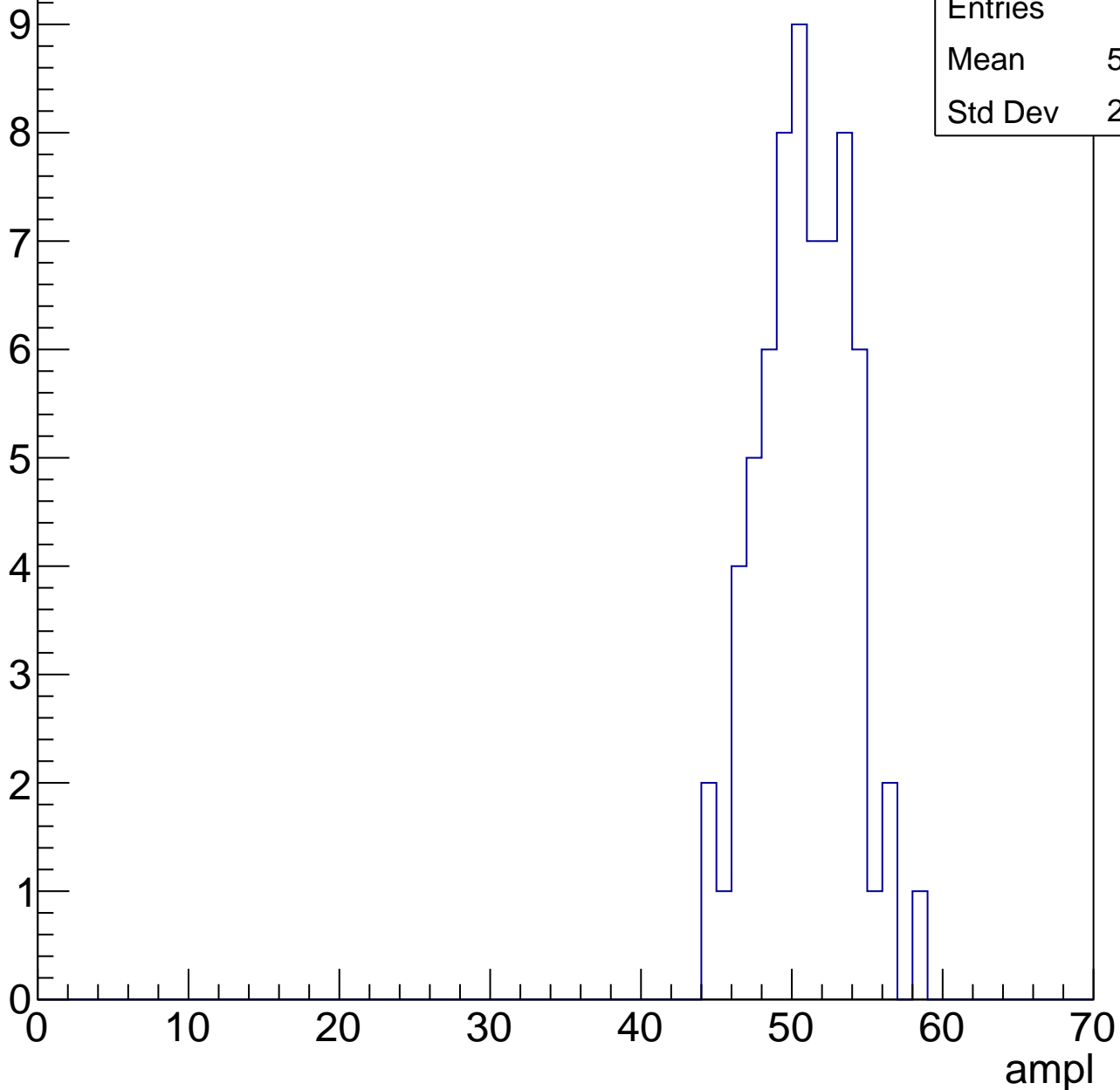


# B1L103S, U21-ch23, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	50.39
Std Dev	2.972



# B1L103S, U21-ch23, adc4

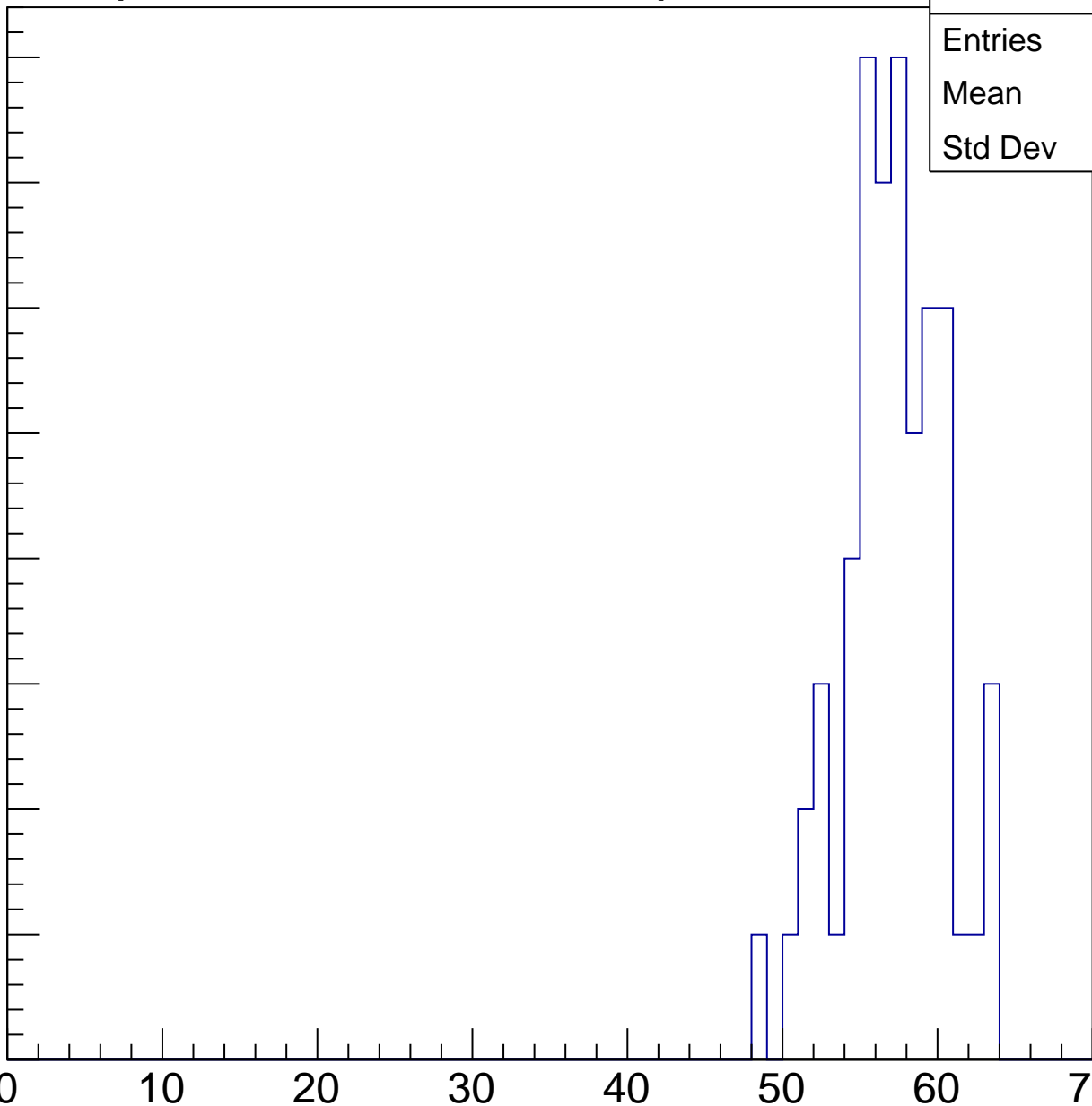
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	57
Mean	56.65
Std Dev	3.225

ampl

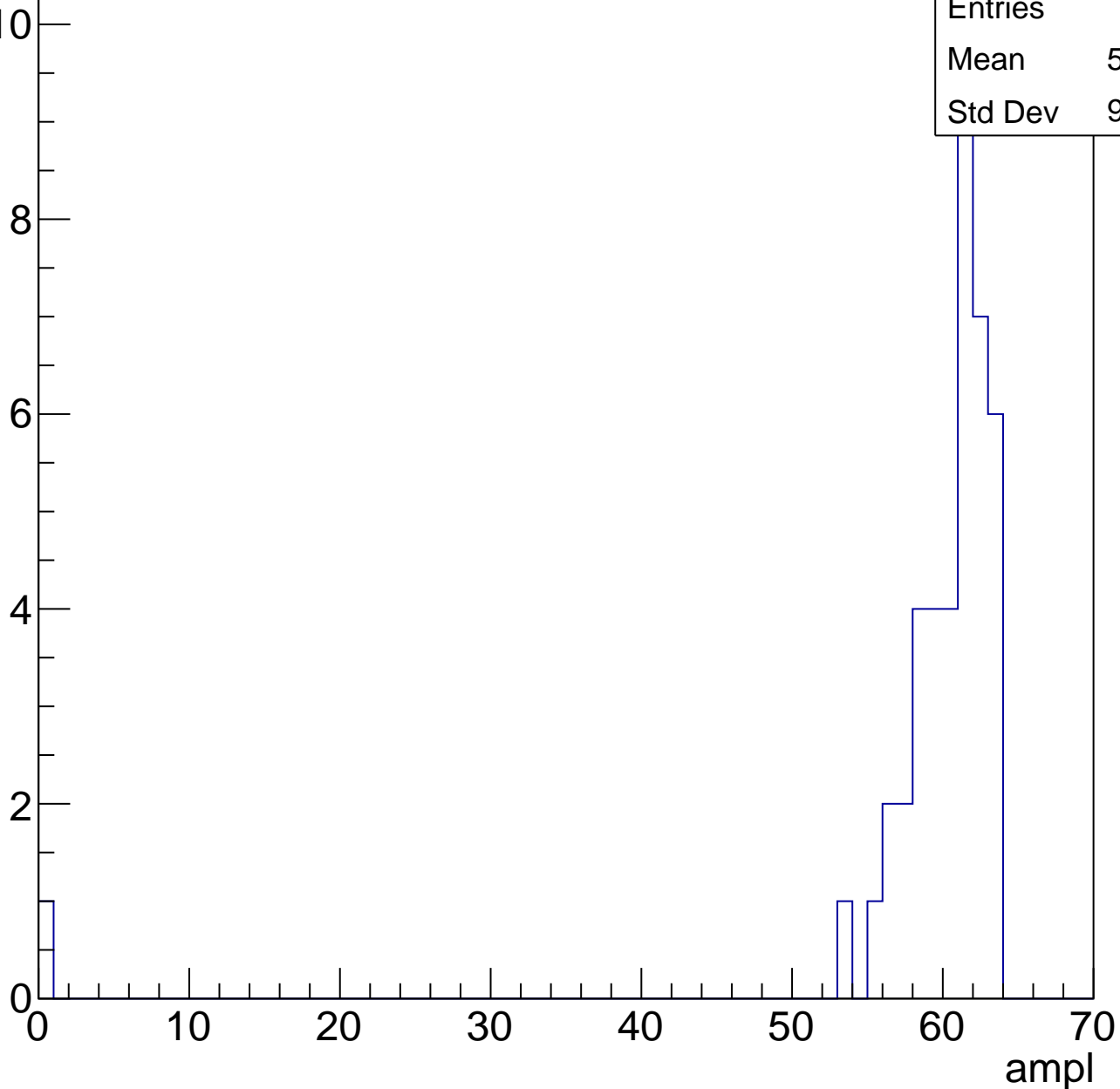


# B1L103S, U21-ch23, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	42
Mean	58.67
Std Dev	9.463



# B1L103S, U21-ch23, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.33
Std Dev	0.4714

ampl

0 10 20 30 40 50 60 70



# B1L103S, U21-ch23, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U21-ch24, adc0

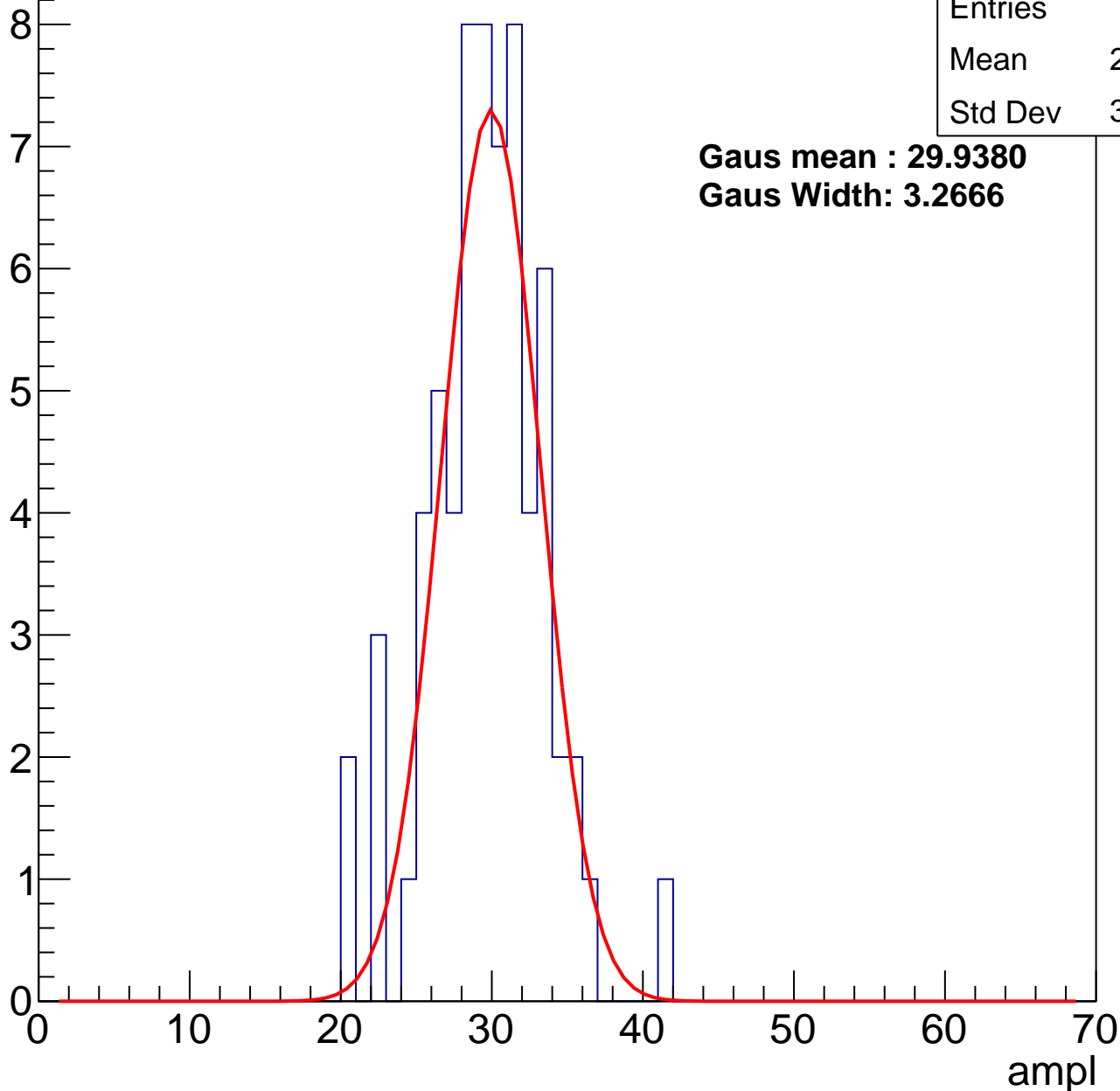
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	29.14
Std Dev	3.797

**Gaus mean : 29.9380**

**Gaus Width: 3.2666**



# B1L103S, U21-ch24, adc1

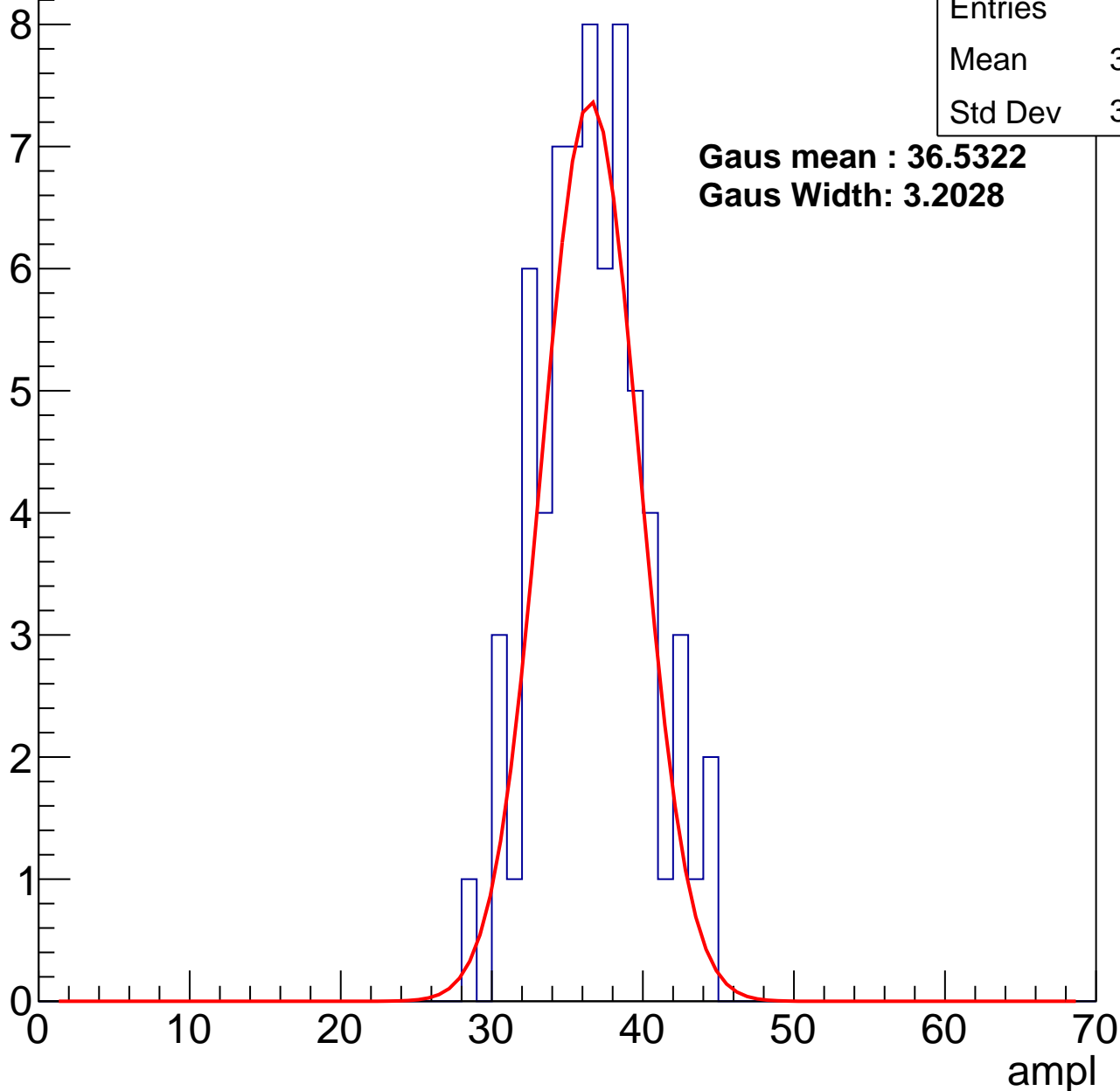
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	36.16
Std Dev	3.497

**Gaus mean : 36.5322**

**Gaus Width: 3.2028**



# B1L103S, U21-ch24, adc2

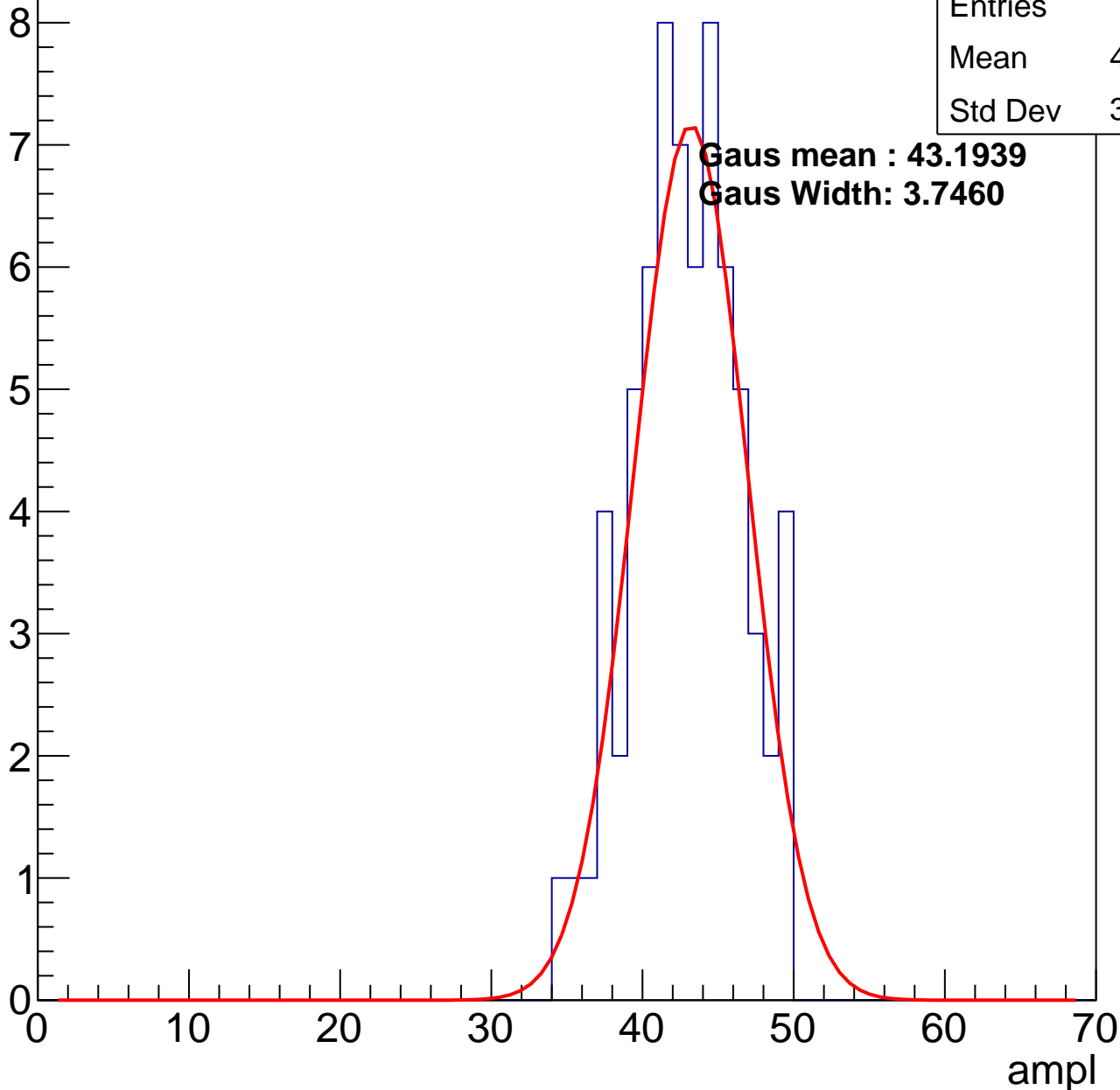
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	42.45
Std Dev	3.529

**Gaus mean : 43.1939**

**Gaus Width: 3.7460**

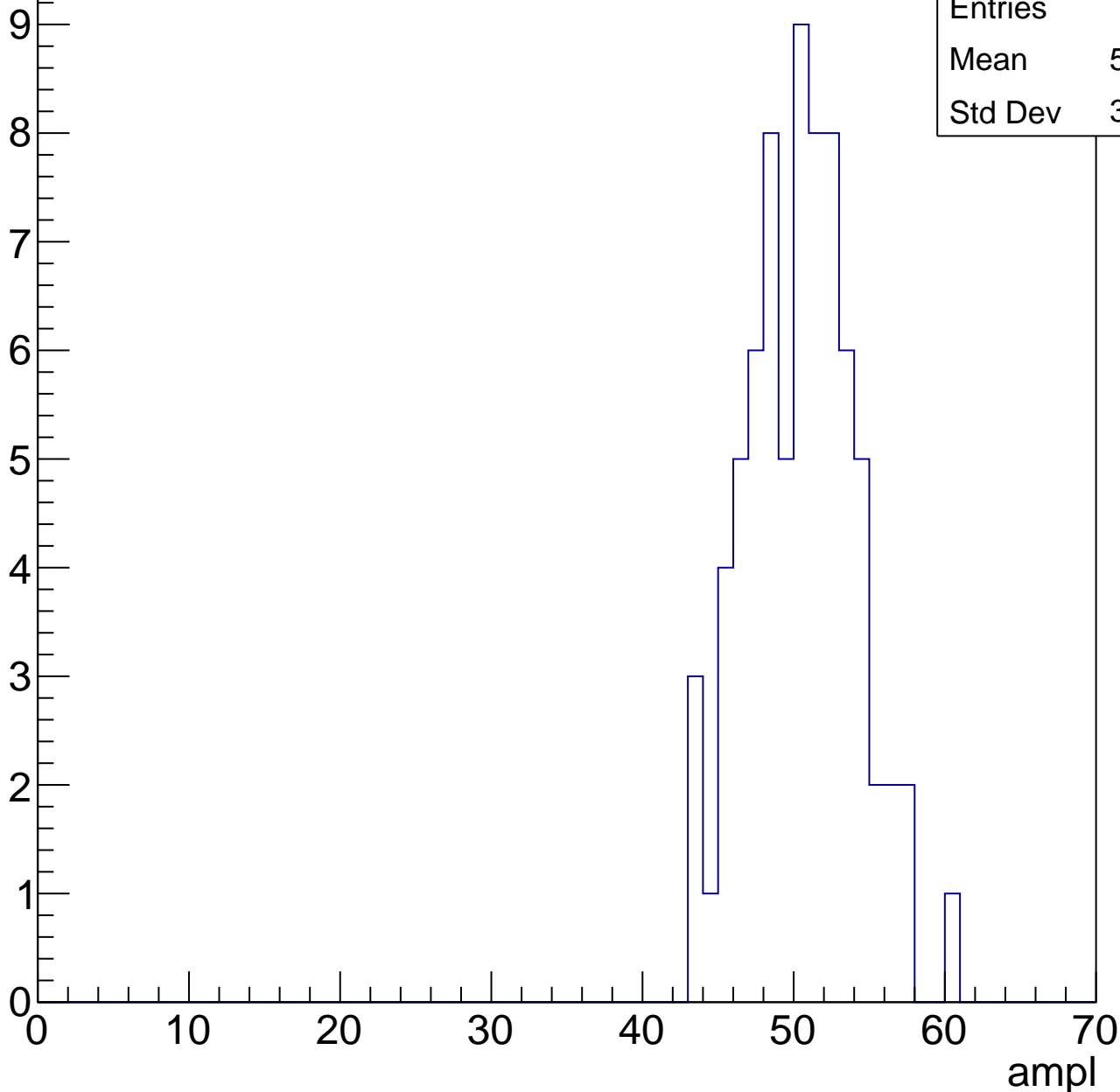


# B1L103S, U21-ch24, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	50.03
Std Dev	3.555

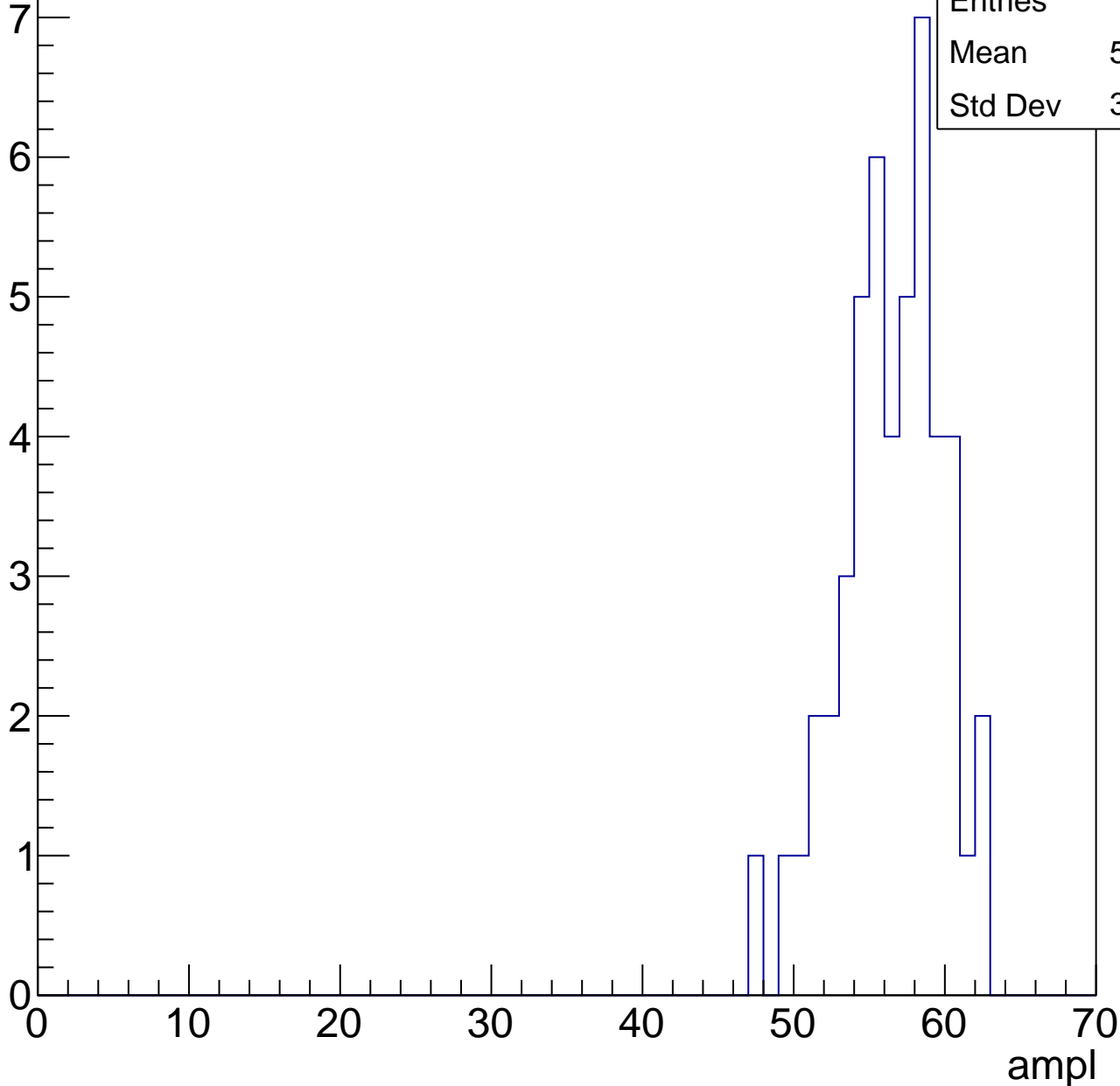


# B1L103S, U21-ch24, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	48
Mean	55.98
Std Dev	3.326

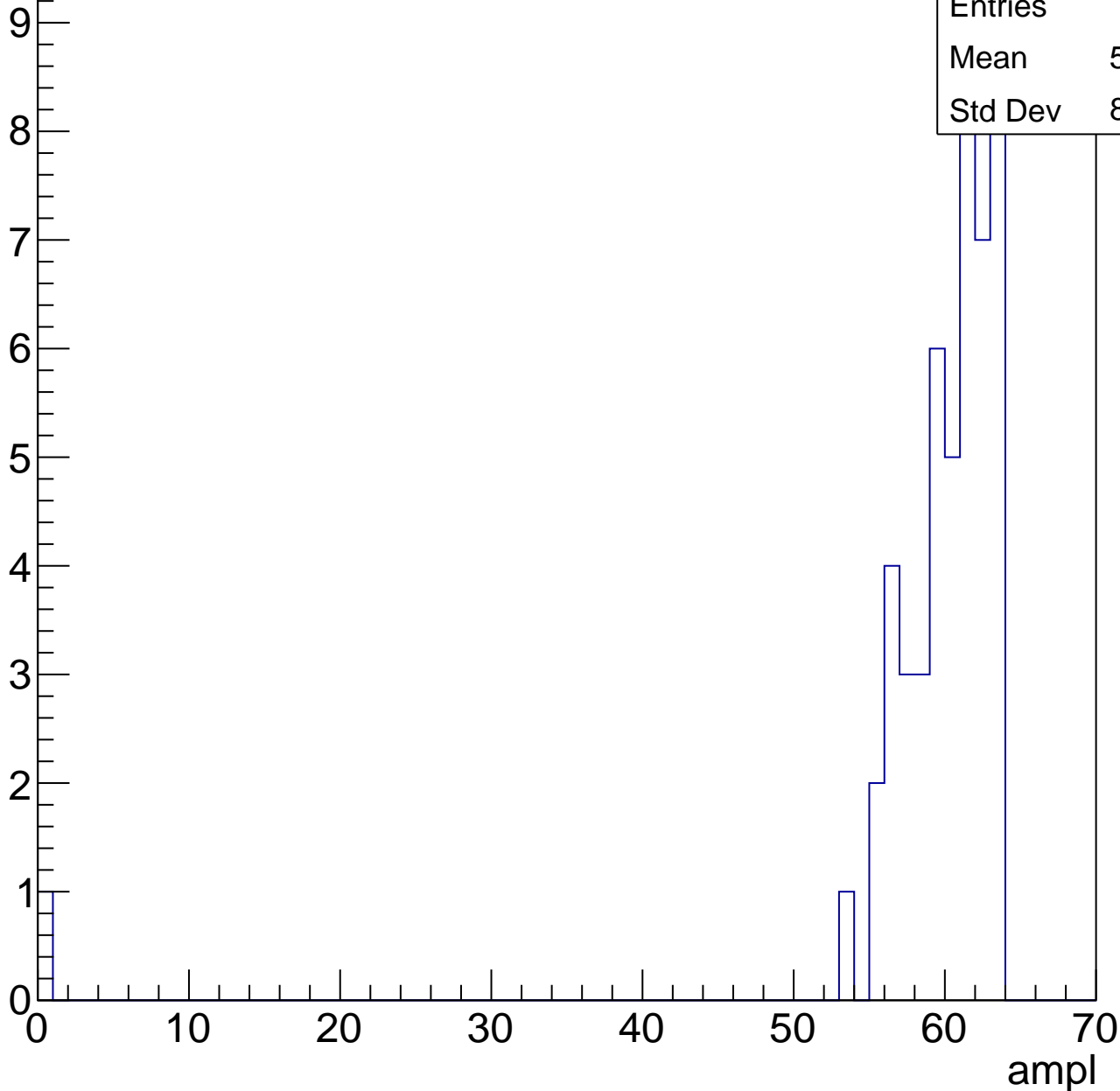


# B1L103S, U21-ch24, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	58.63
Std Dev	8.836



# B1L103S, U21-ch24, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

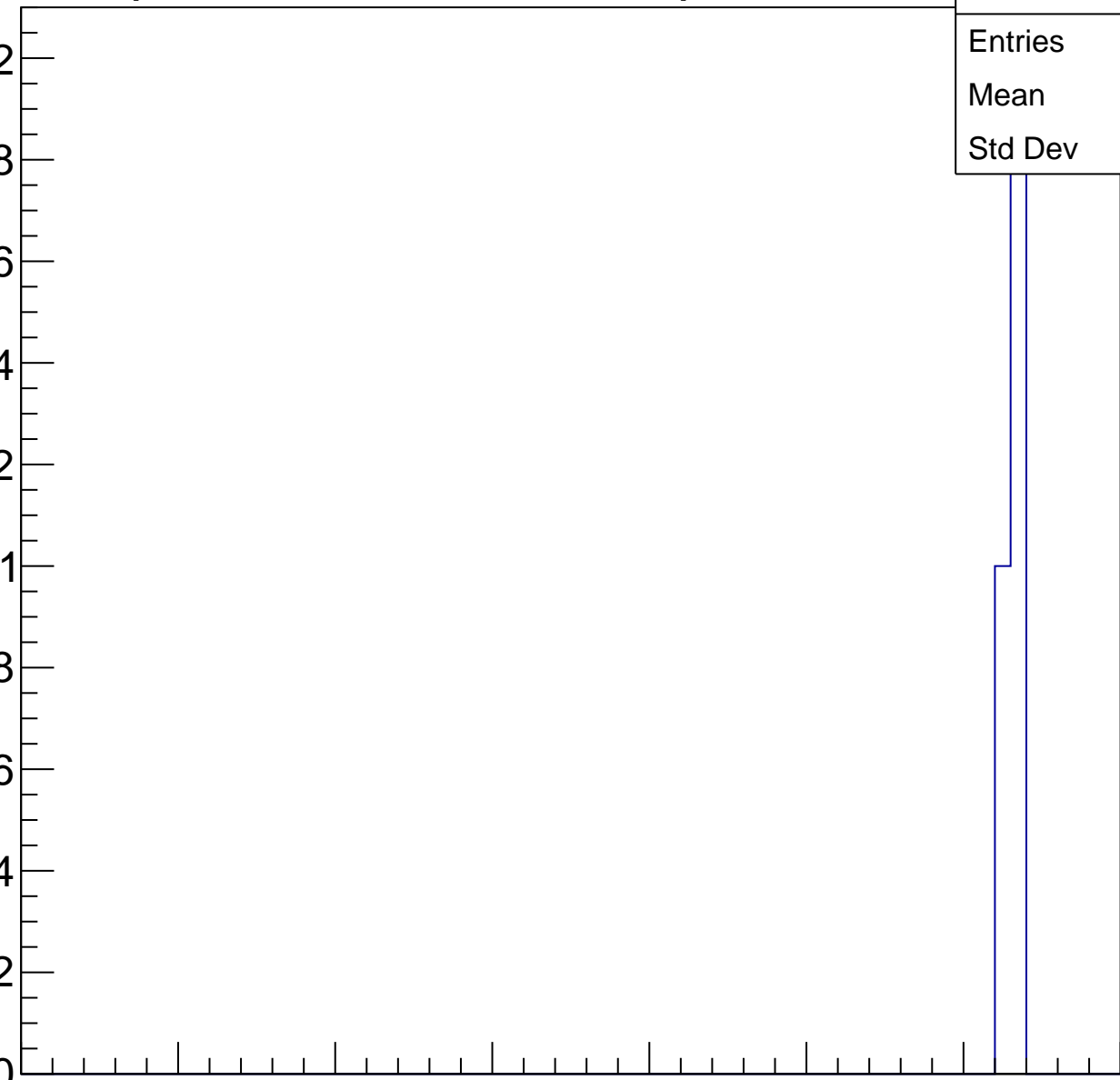
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.67
Std Dev	0.4714

ampl

0 10 20 30 40 50 60 70





# B1L103S, U21-ch24, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U21-ch25, adc0

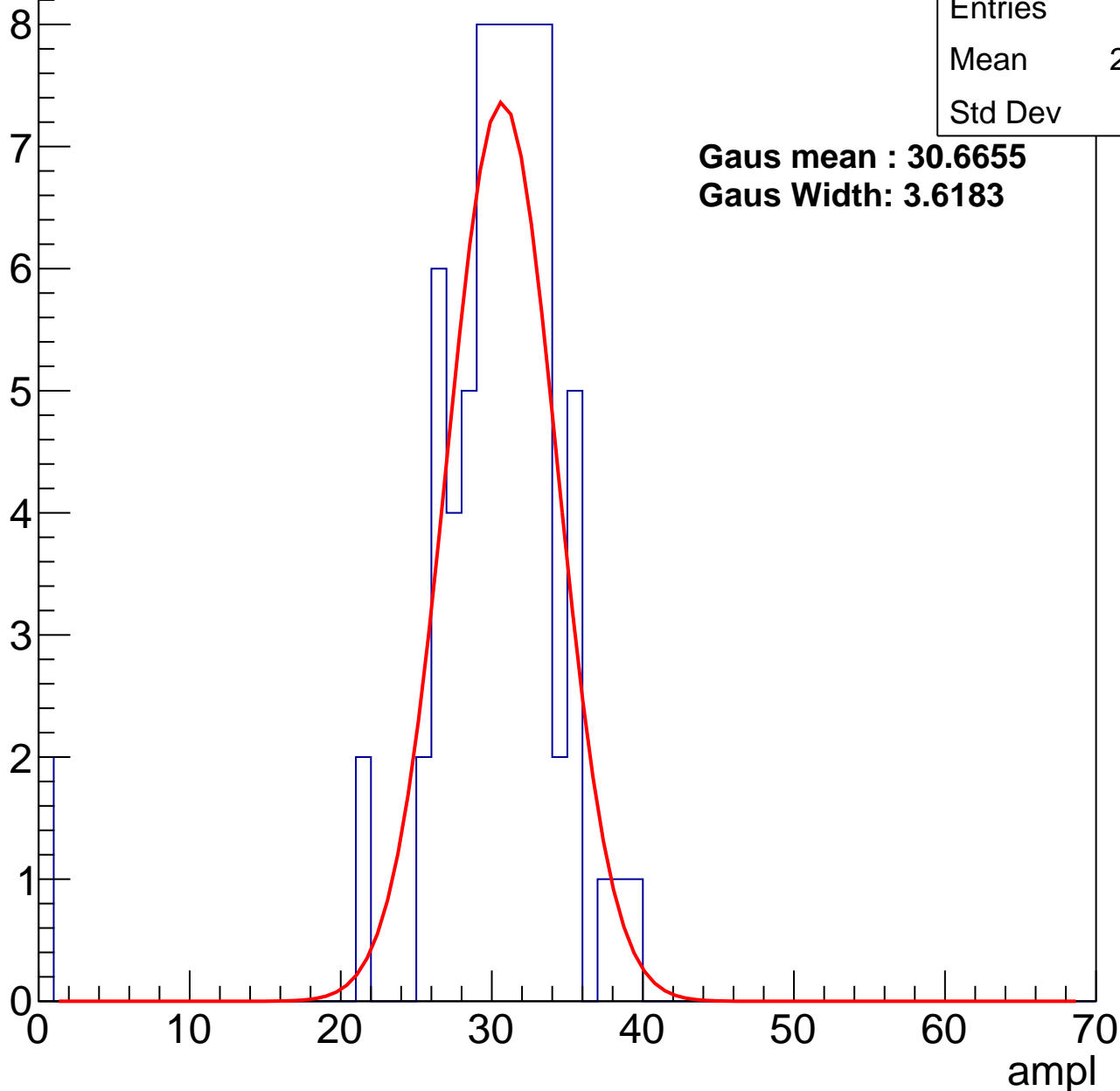
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	29.48
Std Dev	6.07

**Gaus mean : 30.6655**

**Gaus Width: 3.6183**

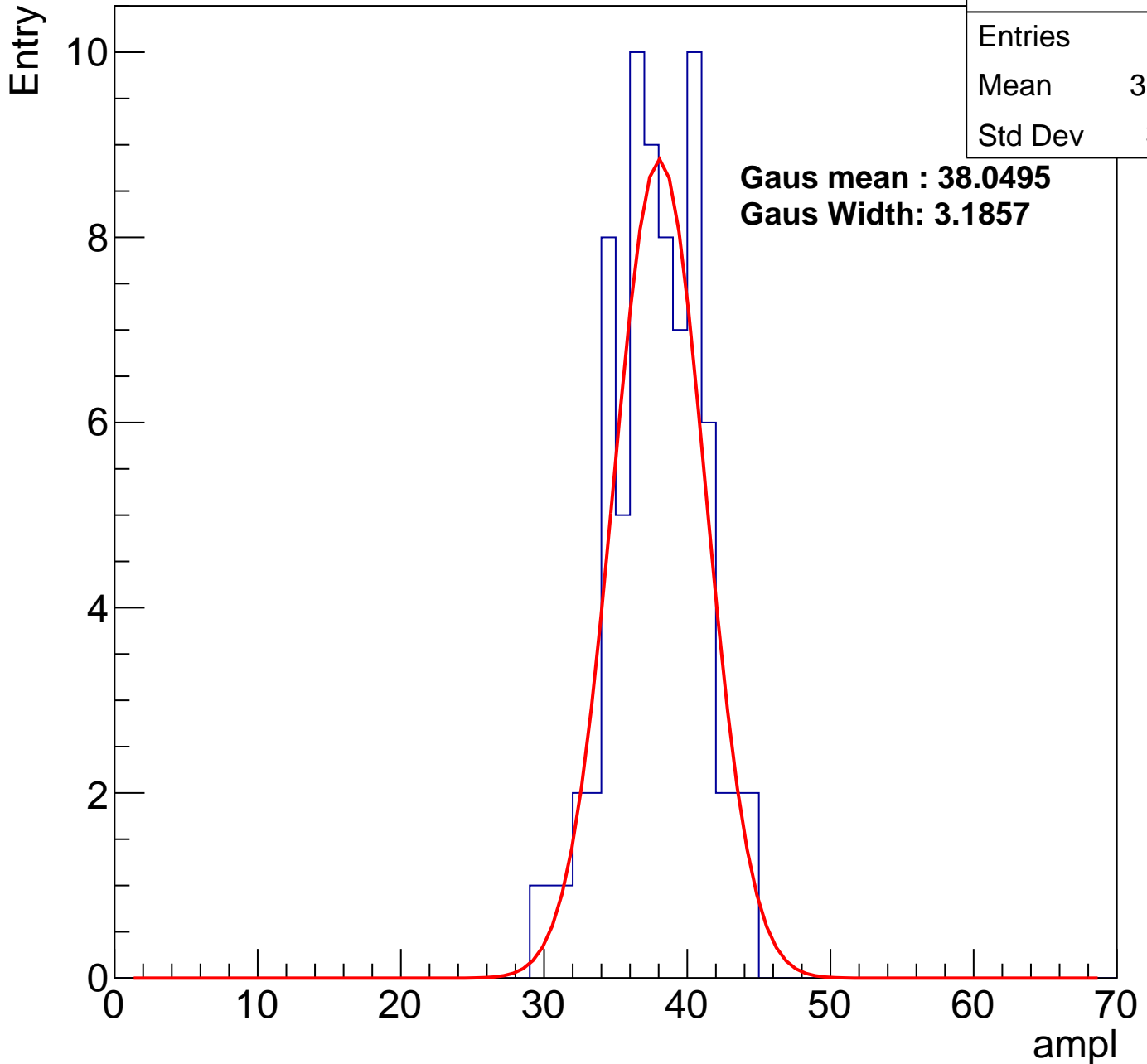


# B1L103S, U21-ch25, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	76
Mean	37.38
Std Dev	3.17

**Gaus mean : 38.0495**  
**Gaus Width: 3.1857**



# B1L103S, U21-ch25, adc2

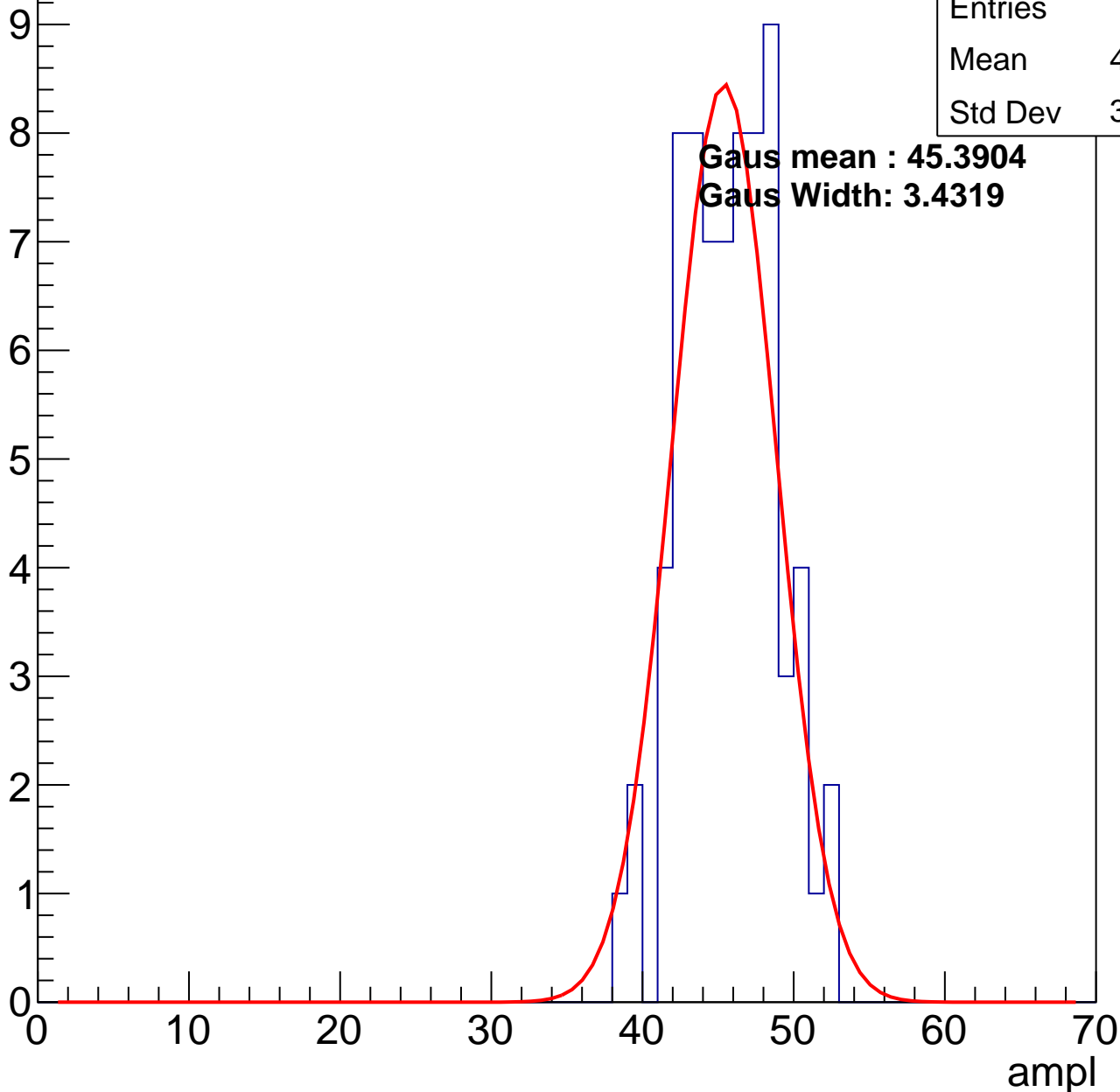
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	45.29
Std Dev	3.102

**Gaus mean : 45.3904**

**Gaus Width: 3.4319**

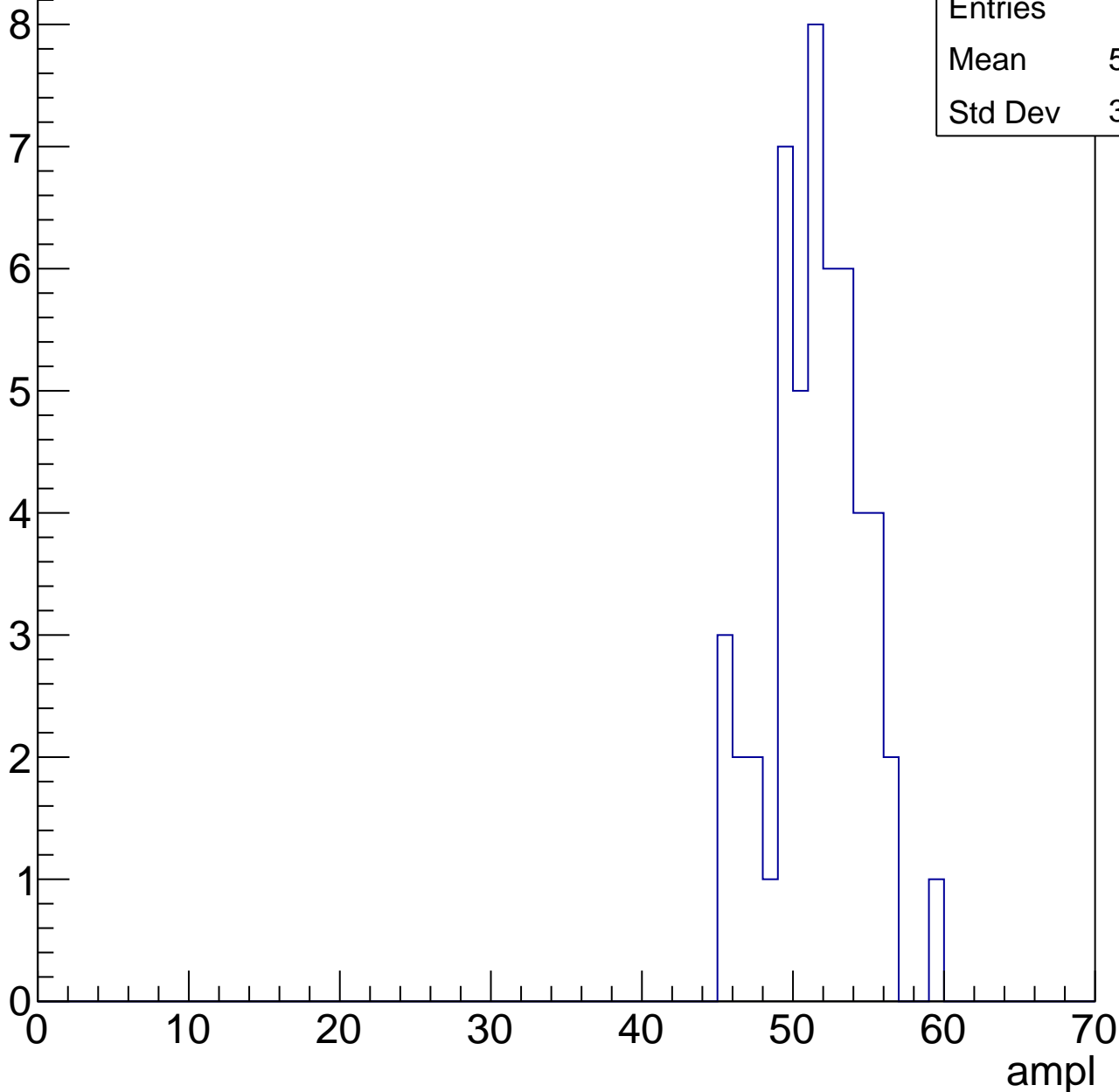


# B1L103S, U21-ch25, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	51.12
Std Dev	3.053

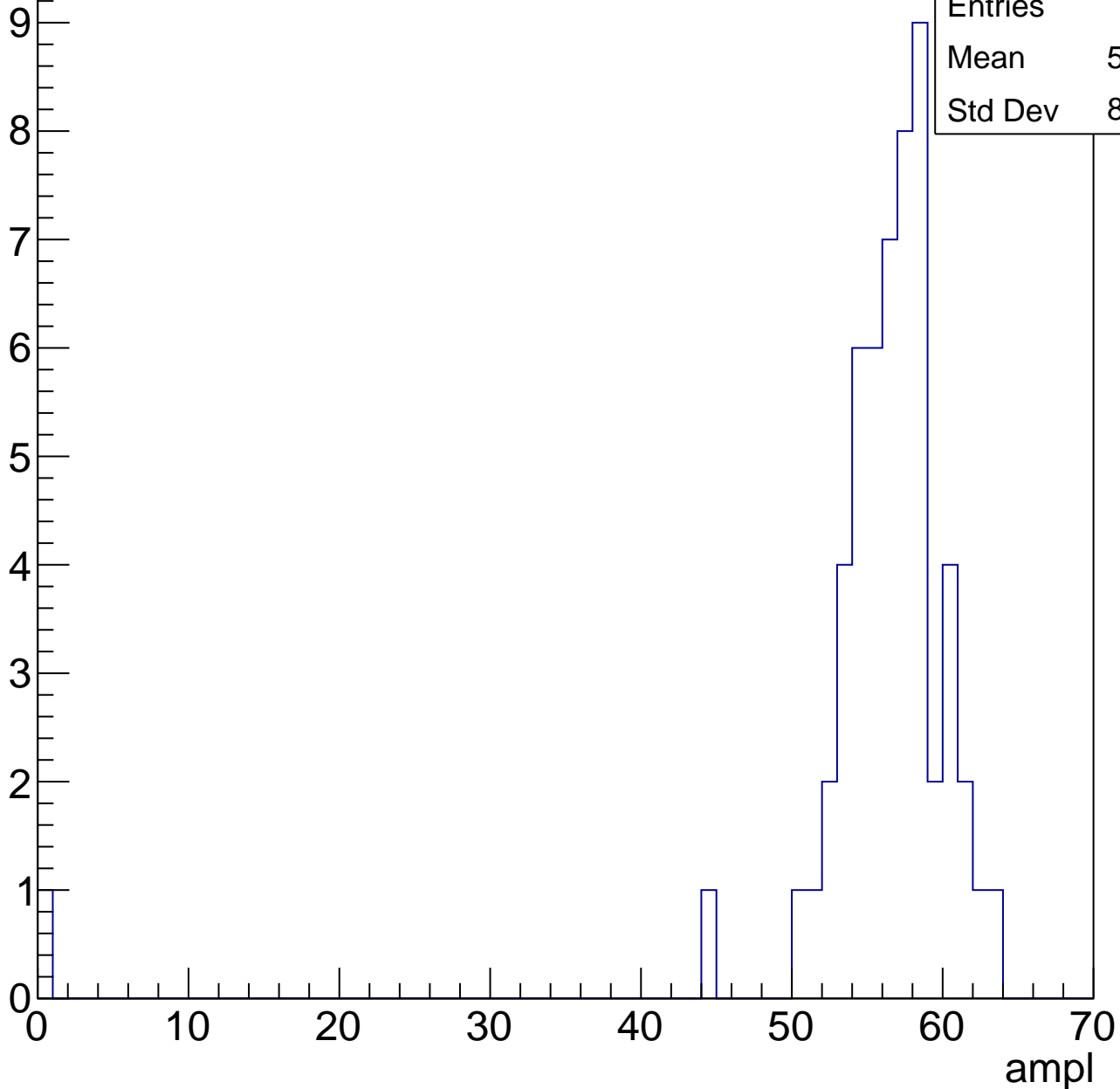


# B1L103S, U21-ch25, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

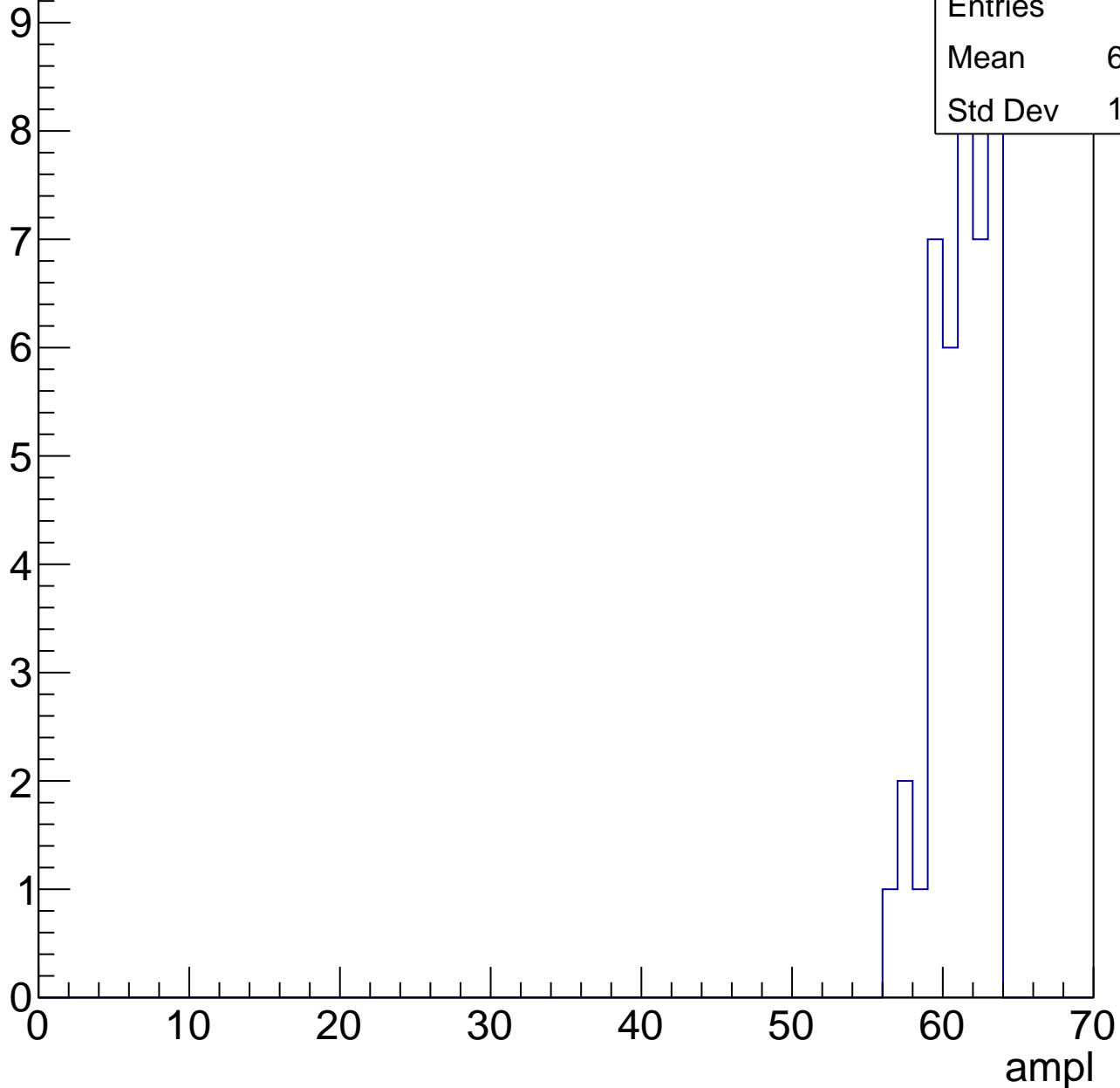
Entries	56
Mean	55.18
Std Dev	8.087



# B1L103S, U21-ch25, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U21-ch25, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U21-ch25, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U21-ch26, adc0

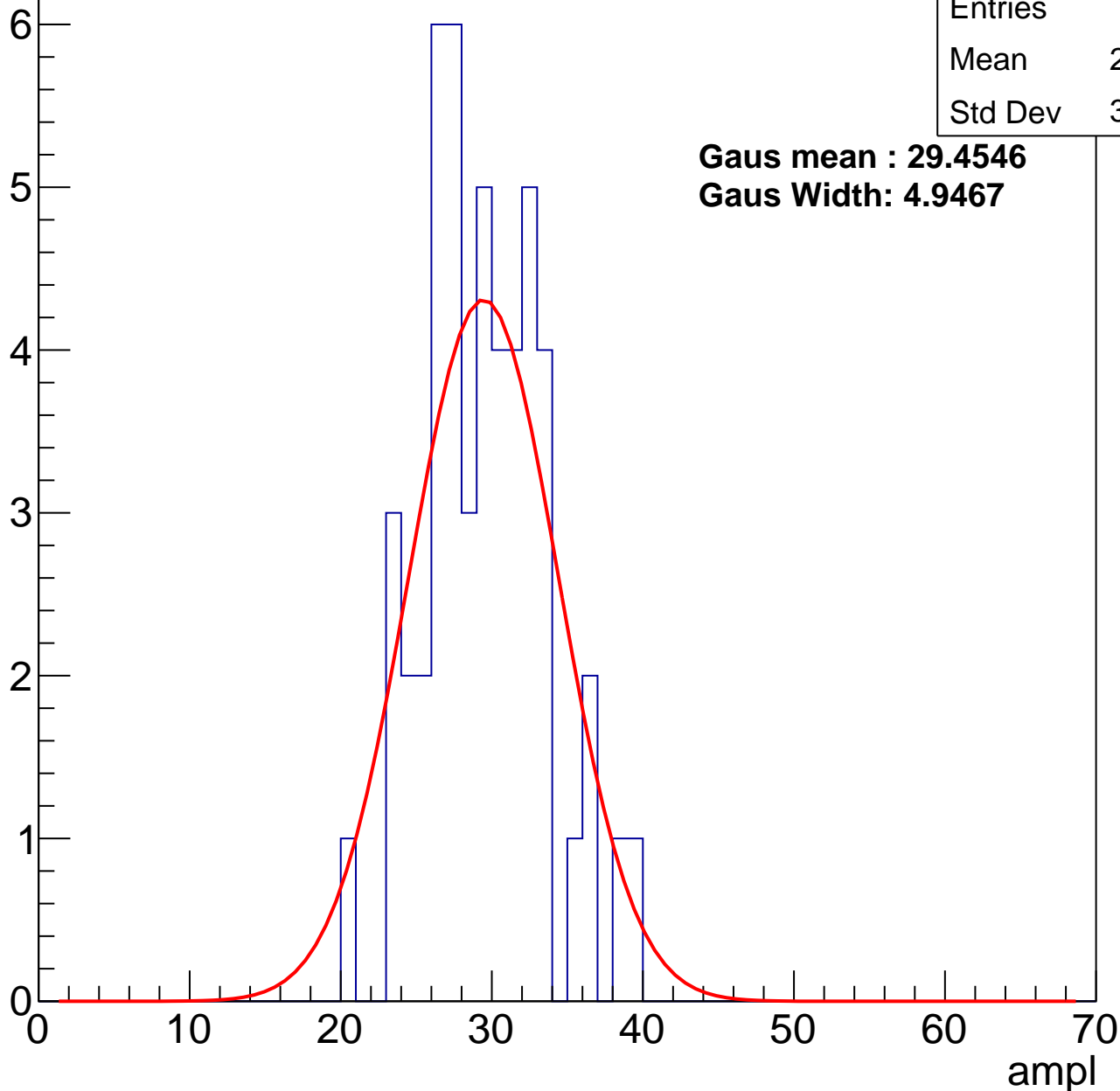
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	29.08
Std Dev	3.989

**Gaus mean : 29.4546**

**Gaus Width: 4.9467**



# B1L103S, U21-ch26, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	91
Mean	35.86
Std Dev	3.93

**Gaus mean : 36.1400**

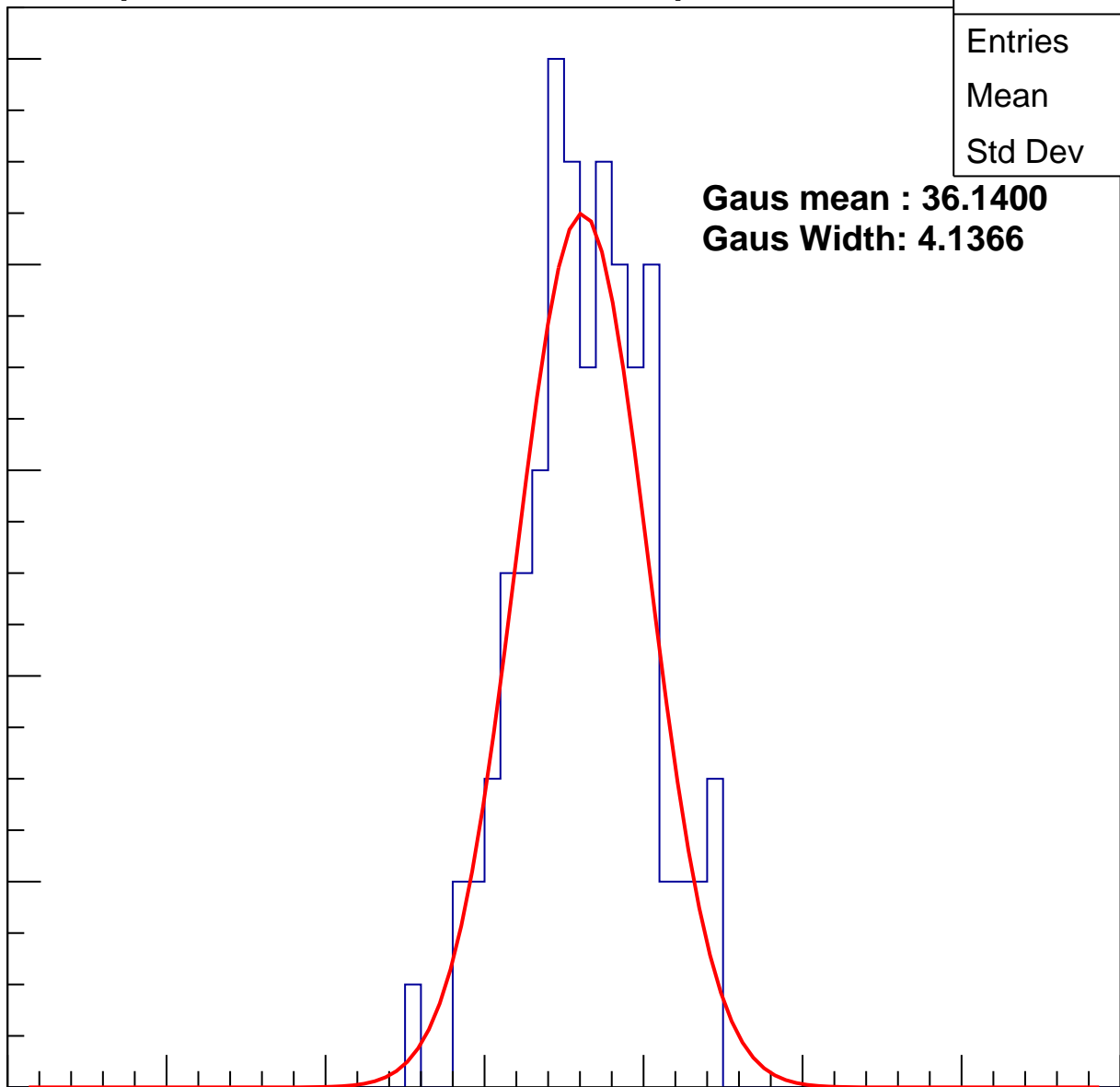
**Gaus Width: 4.1366**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U21-ch26, adc2

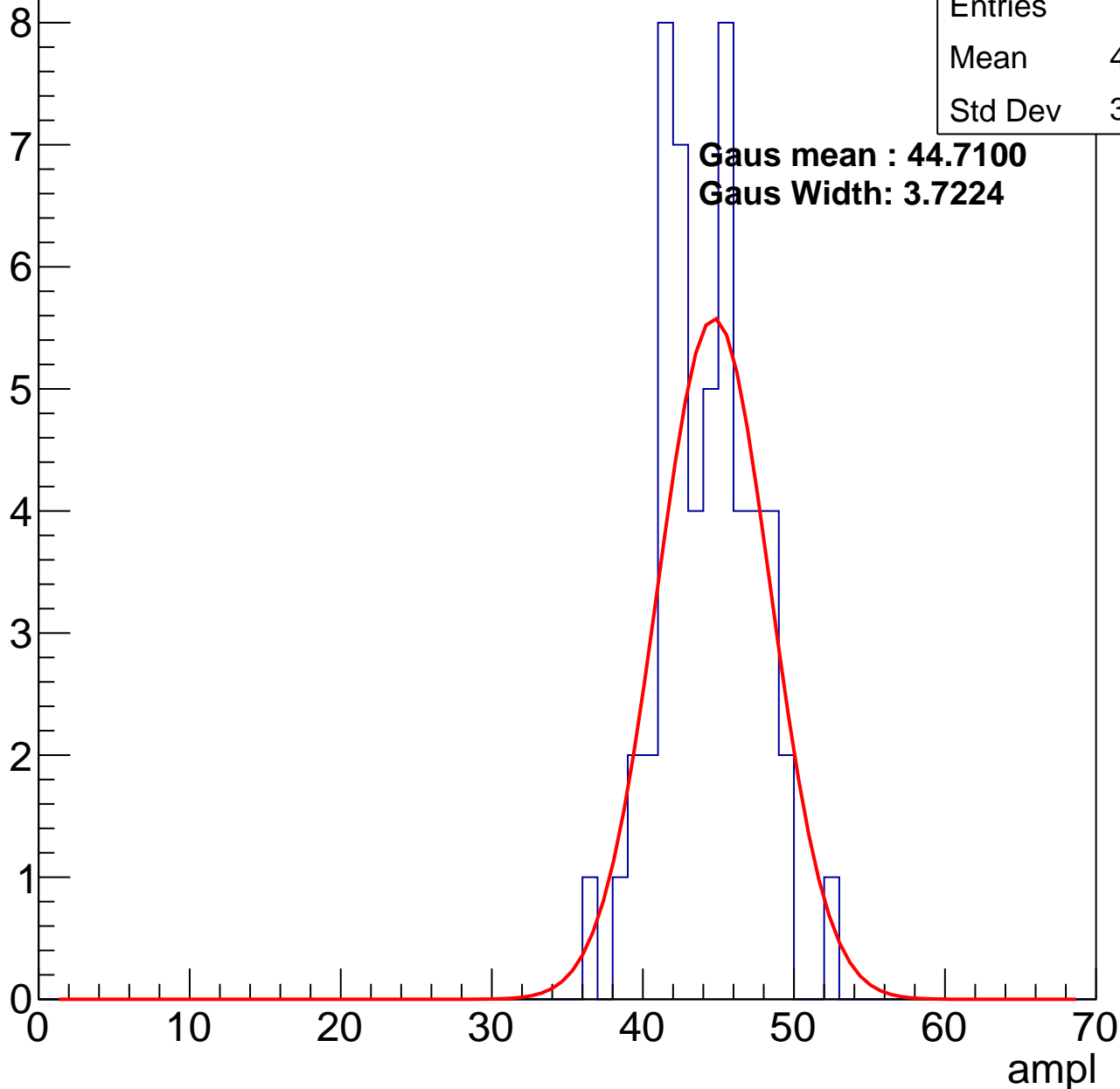
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	43.77
Std Dev	3.136

**Gaus mean : 44.7100**

**Gaus Width: 3.7224**

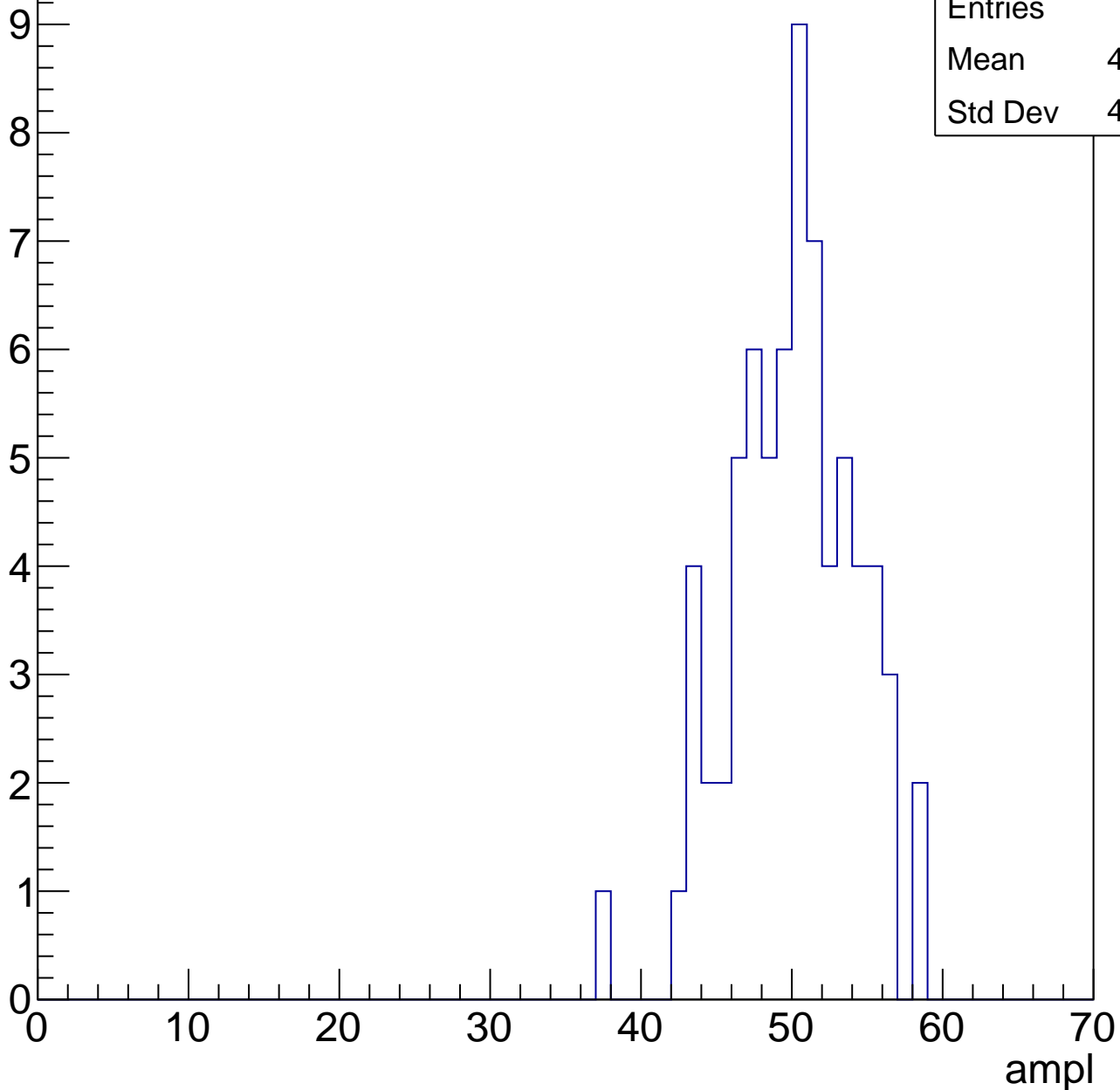


# B1L103S, U21-ch26, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	49.64
Std Dev	4.088

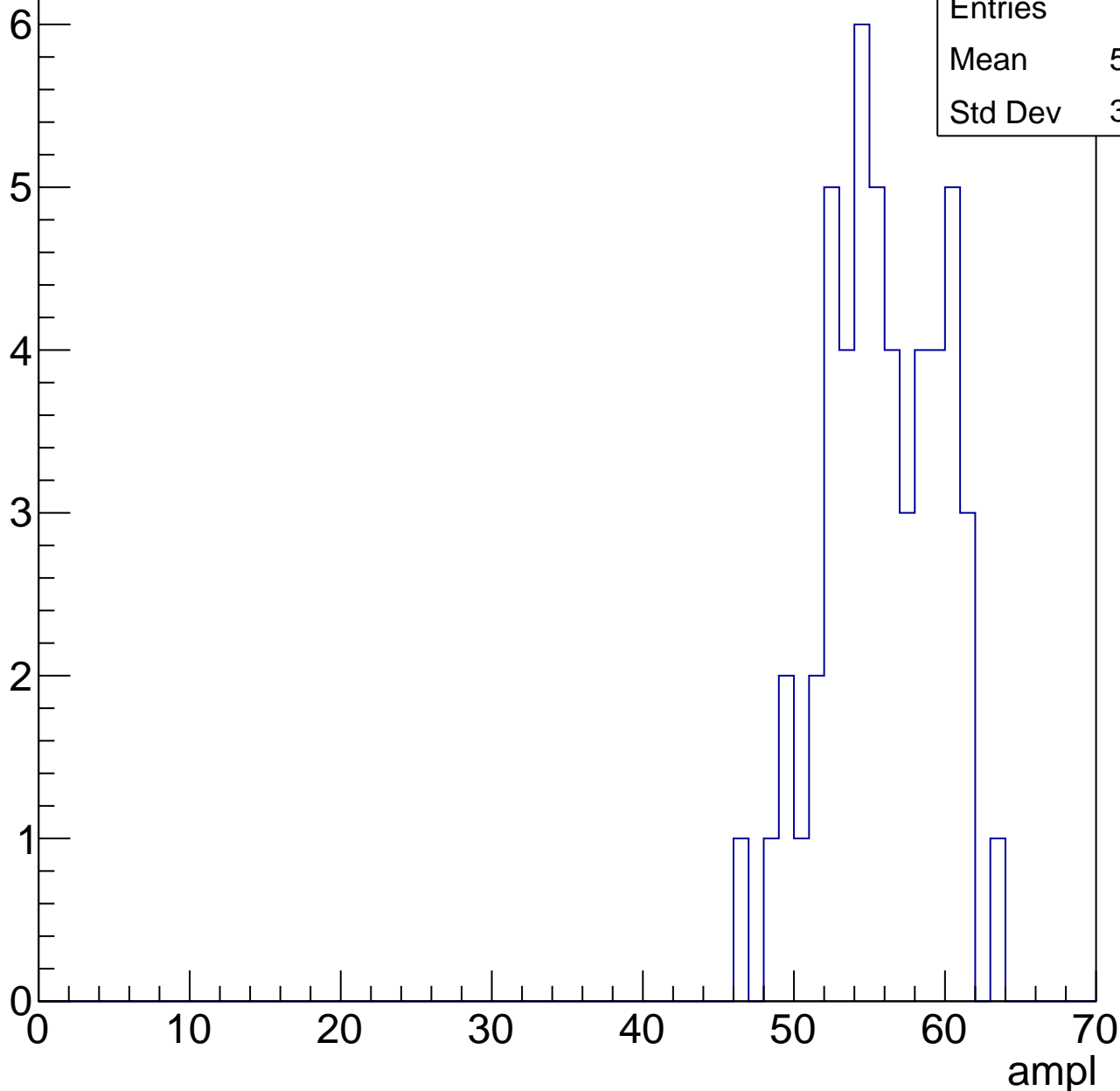


# B1L103S, U21-ch26, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	55.37
Std Dev	3.788

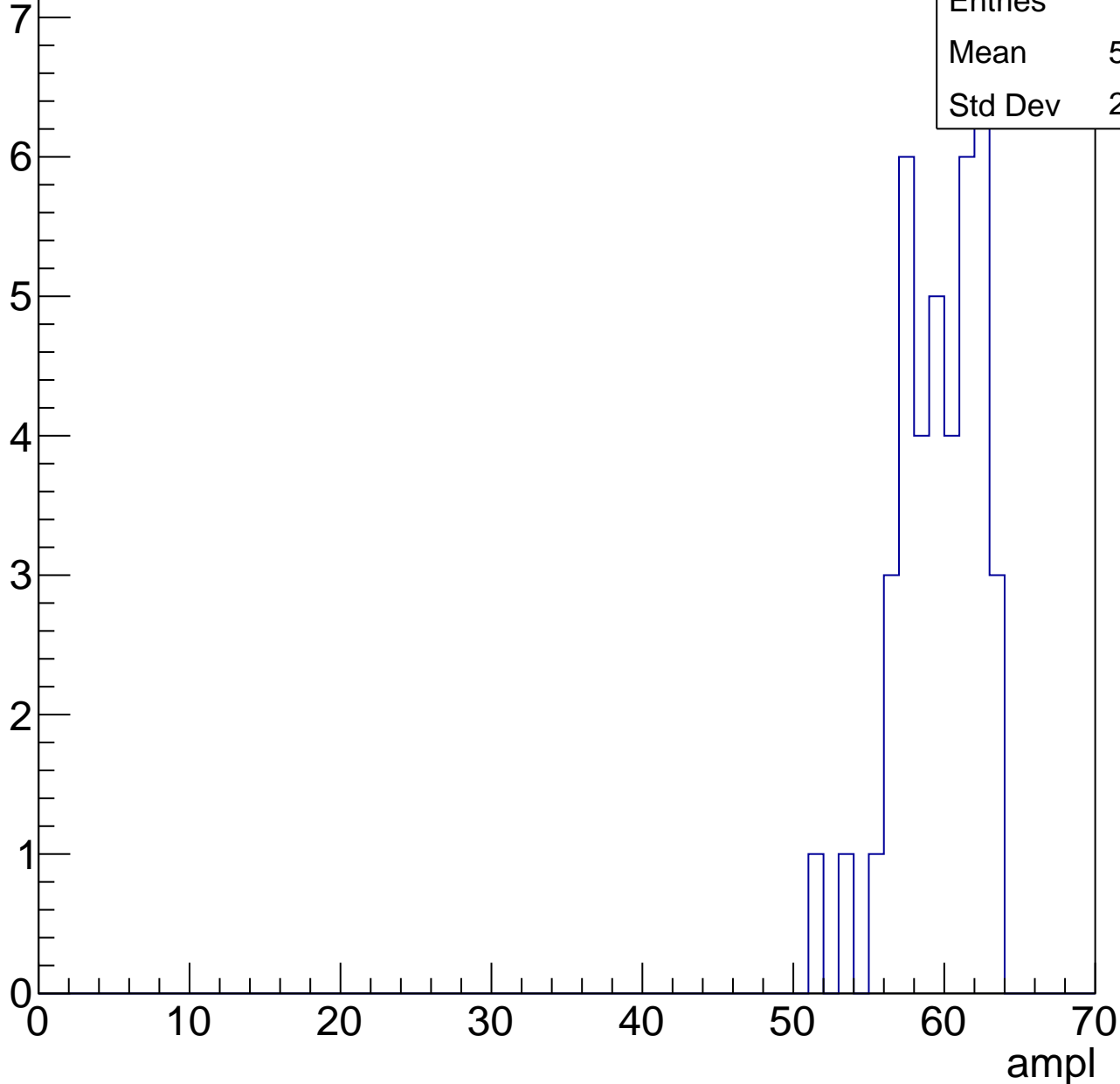


# B1L103S, U21-ch26, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	41
Mean	59.15
Std Dev	2.746

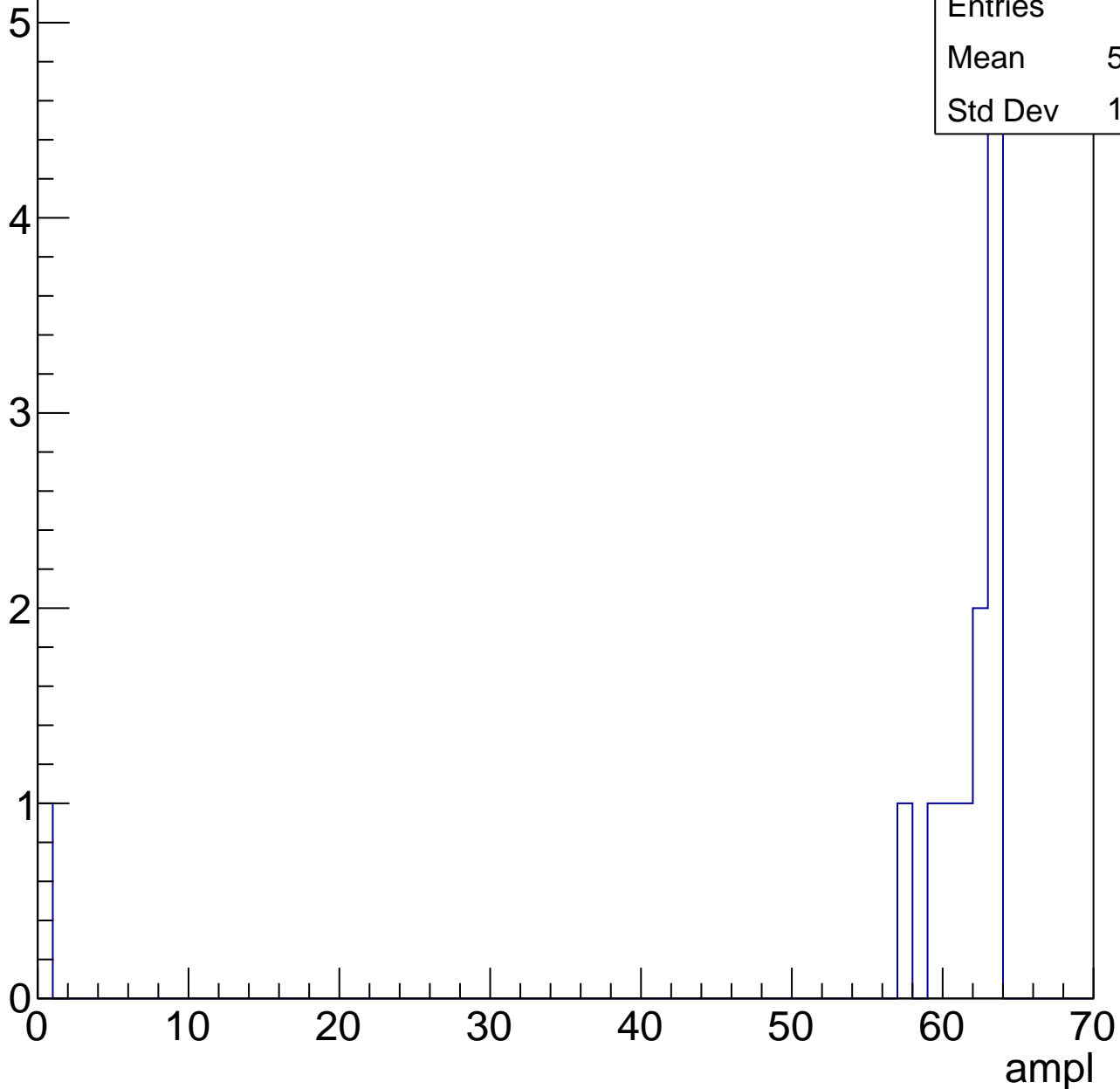


# B1L103S, U21-ch26, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	12
Mean	56.33
Std Dev	17.08





# B1L103S, U21-ch26, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	4
Mean	31.25
Std Dev	31.25

# B1L103S, U21-ch27, adc0

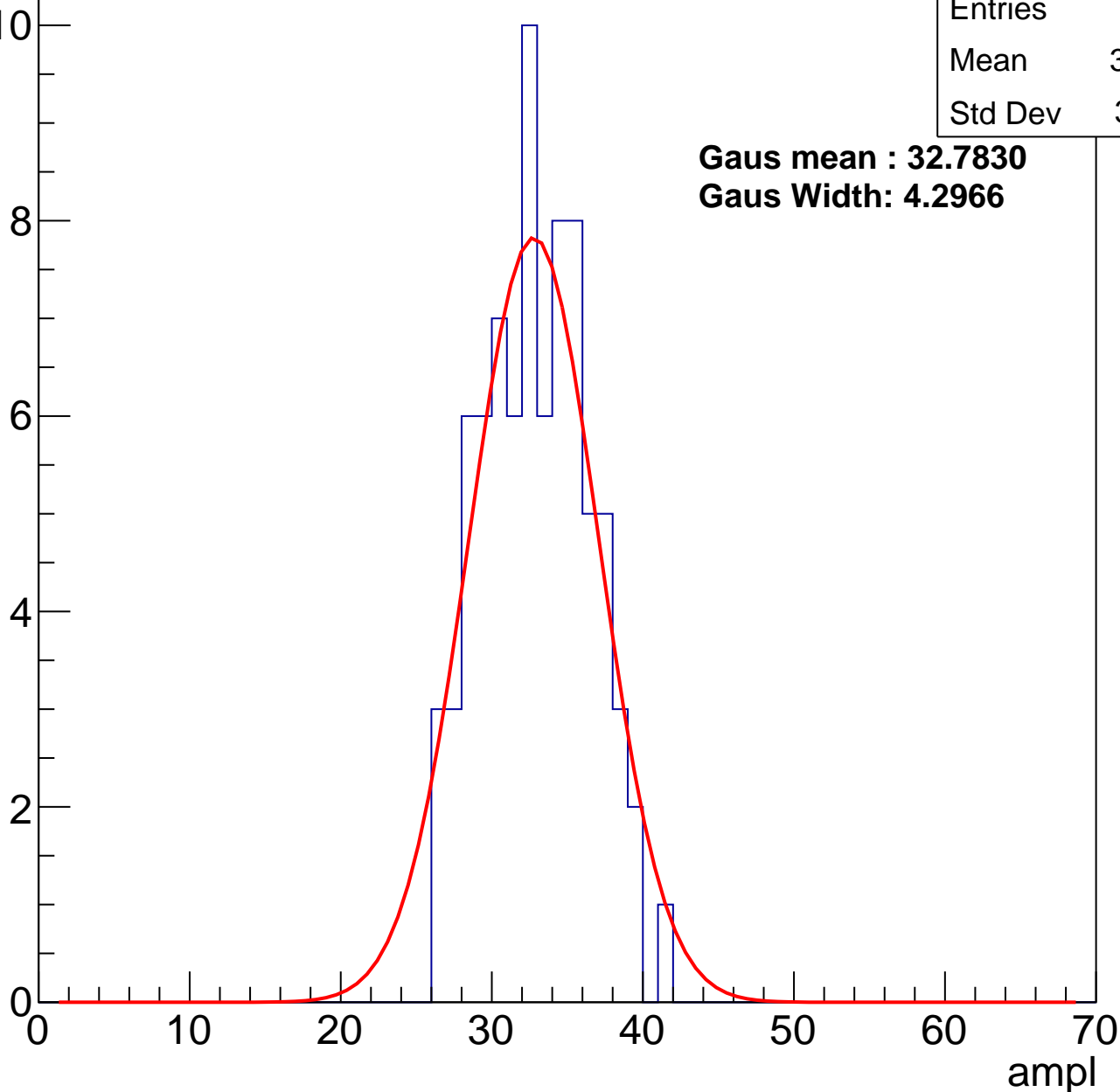
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	79
Mean	32.47
Std Dev	3.471

**Gaus mean : 32.7830**

**Gaus Width: 4.2966**



# B1L103S, U21-ch27, adc1

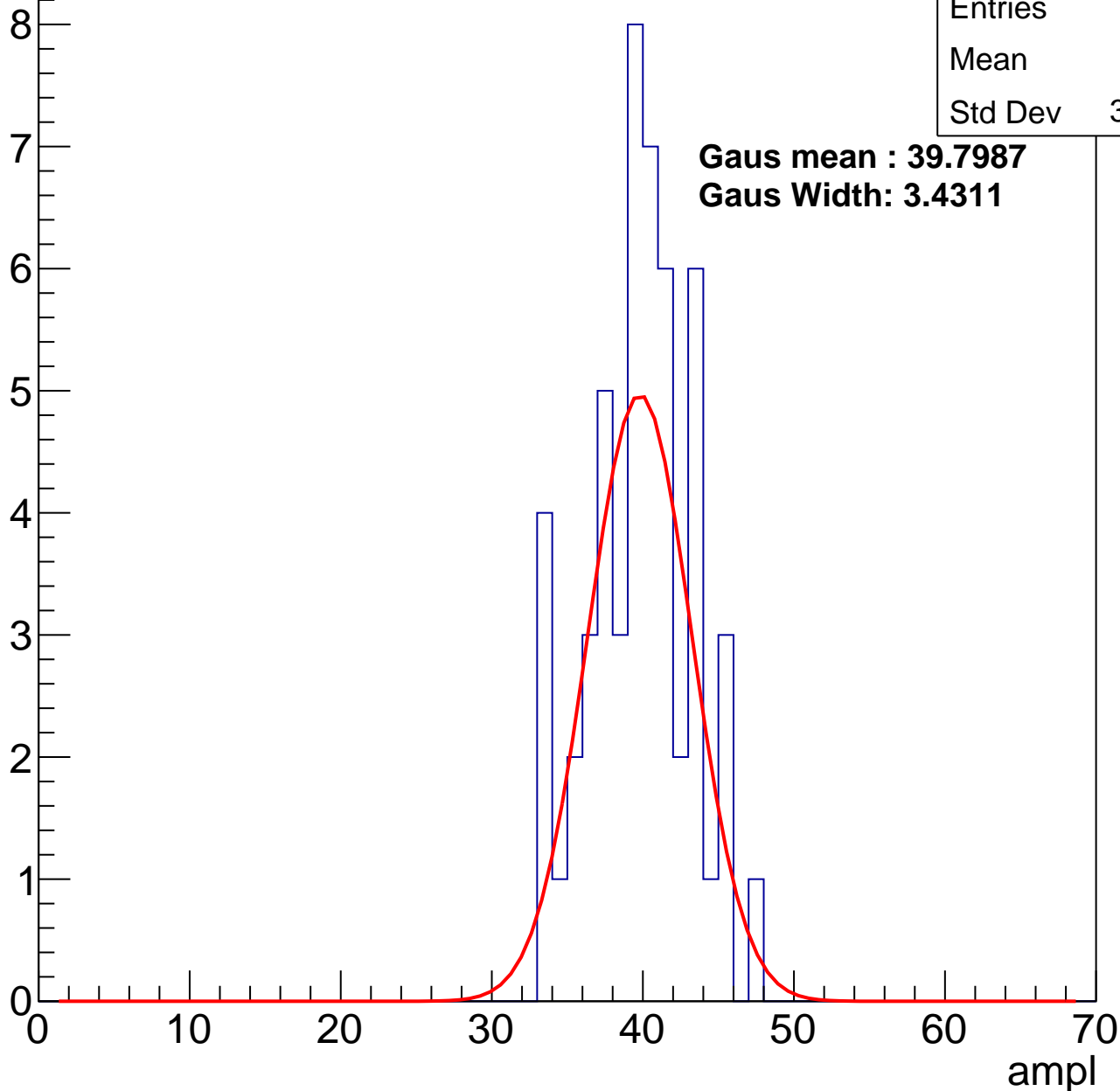
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	39.4
Std Dev	3.353

**Gaus mean : 39.7987**

**Gaus Width: 3.4311**



# B1L103S, U21-ch27, adc2

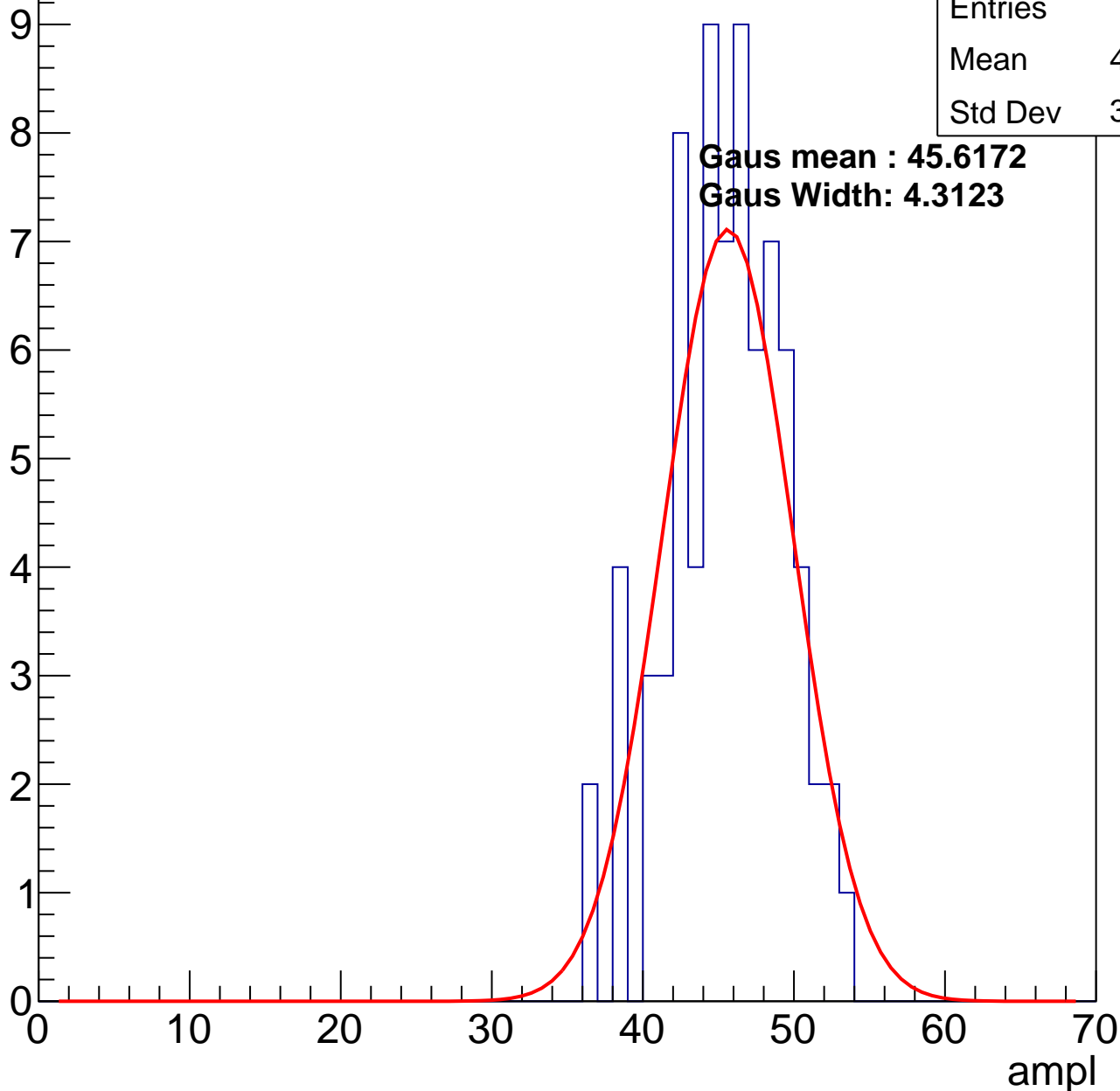
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	45.08
Std Dev	3.786

**Gaus mean : 45.6172**

**Gaus Width: 4.3123**

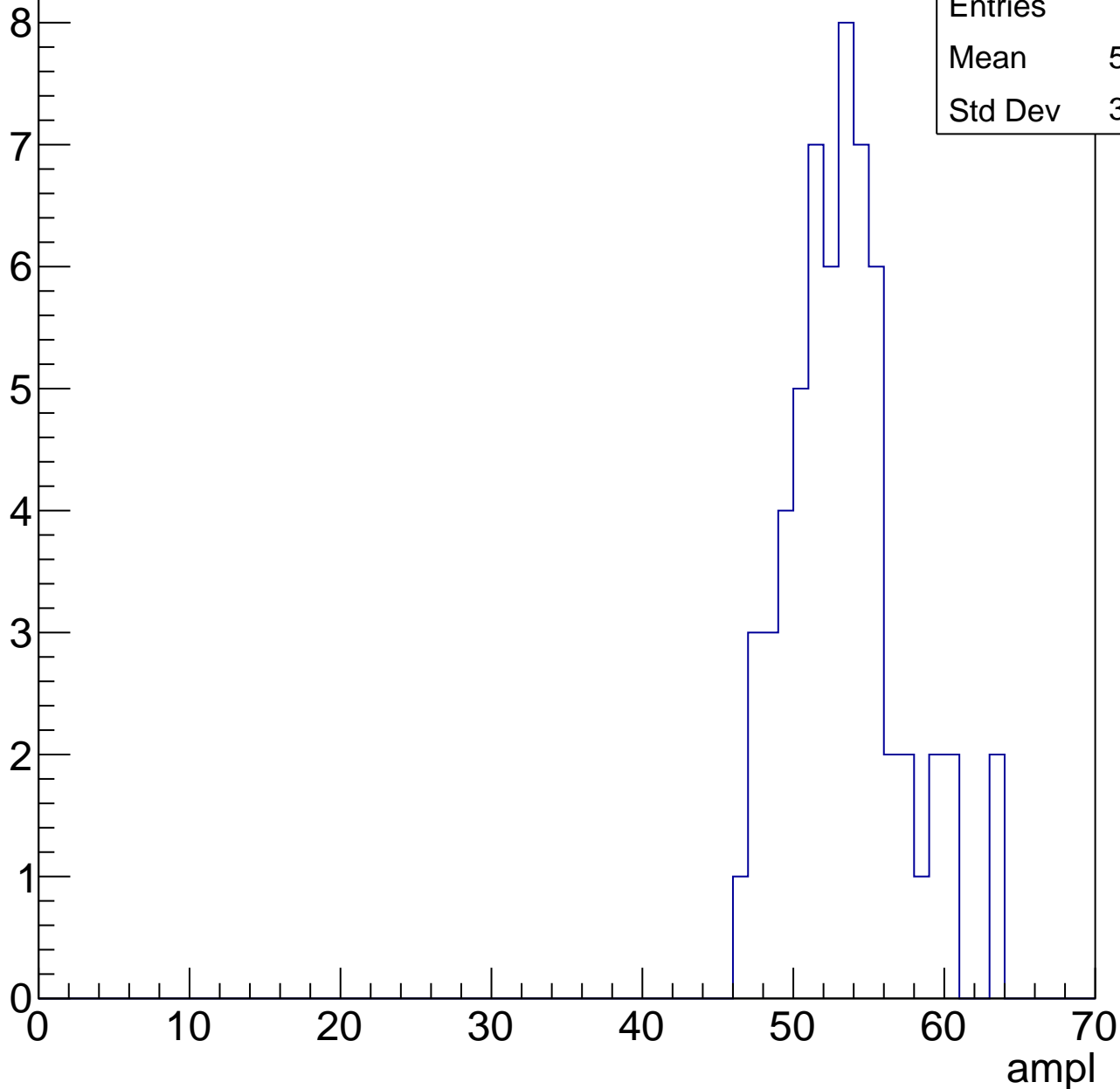


# B1L103S, U21-ch27, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

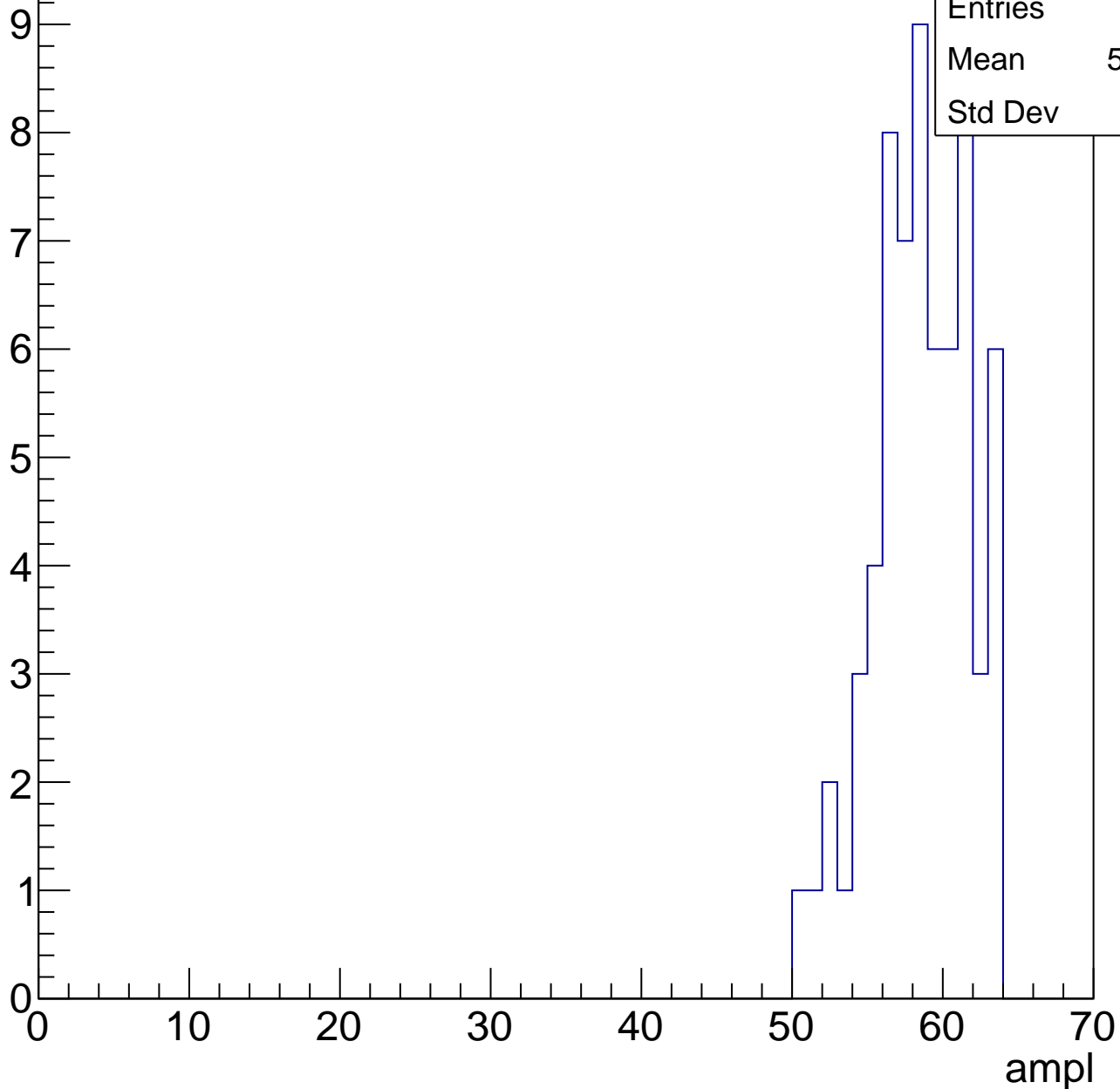
Entries	61
Mean	52.89
Std Dev	3.733



# B1L103S, U21-ch27, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



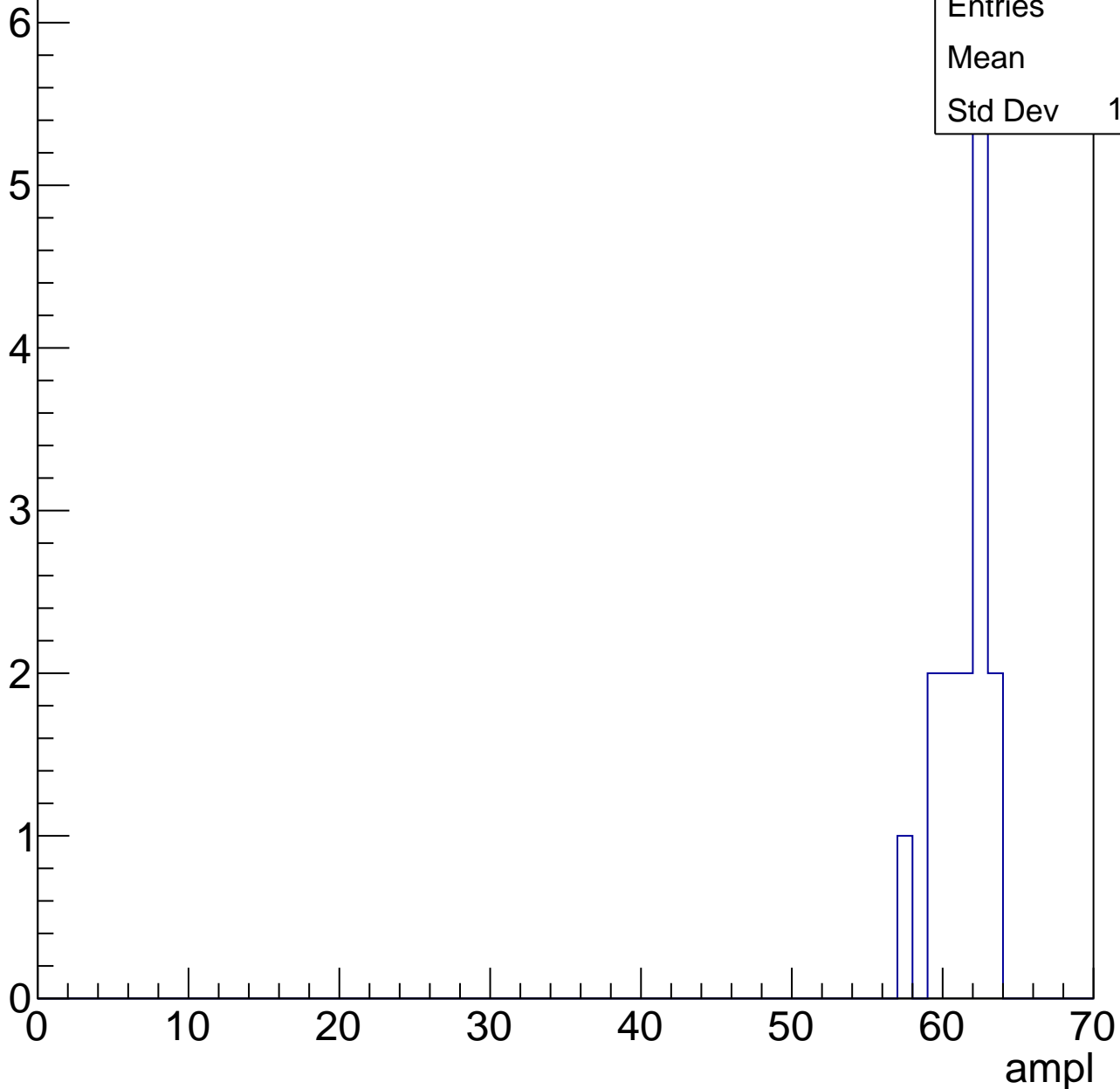
Entries	65
Mean	58.08
Std Dev	3.12

# B1L103S, U21-ch27, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	15
Mean	61
Std Dev	1.633



# B1L103S, U21-ch27, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U21-ch27, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	12.5
Std Dev	12.5

ampl

# B1L103S, U21-ch28, adc0

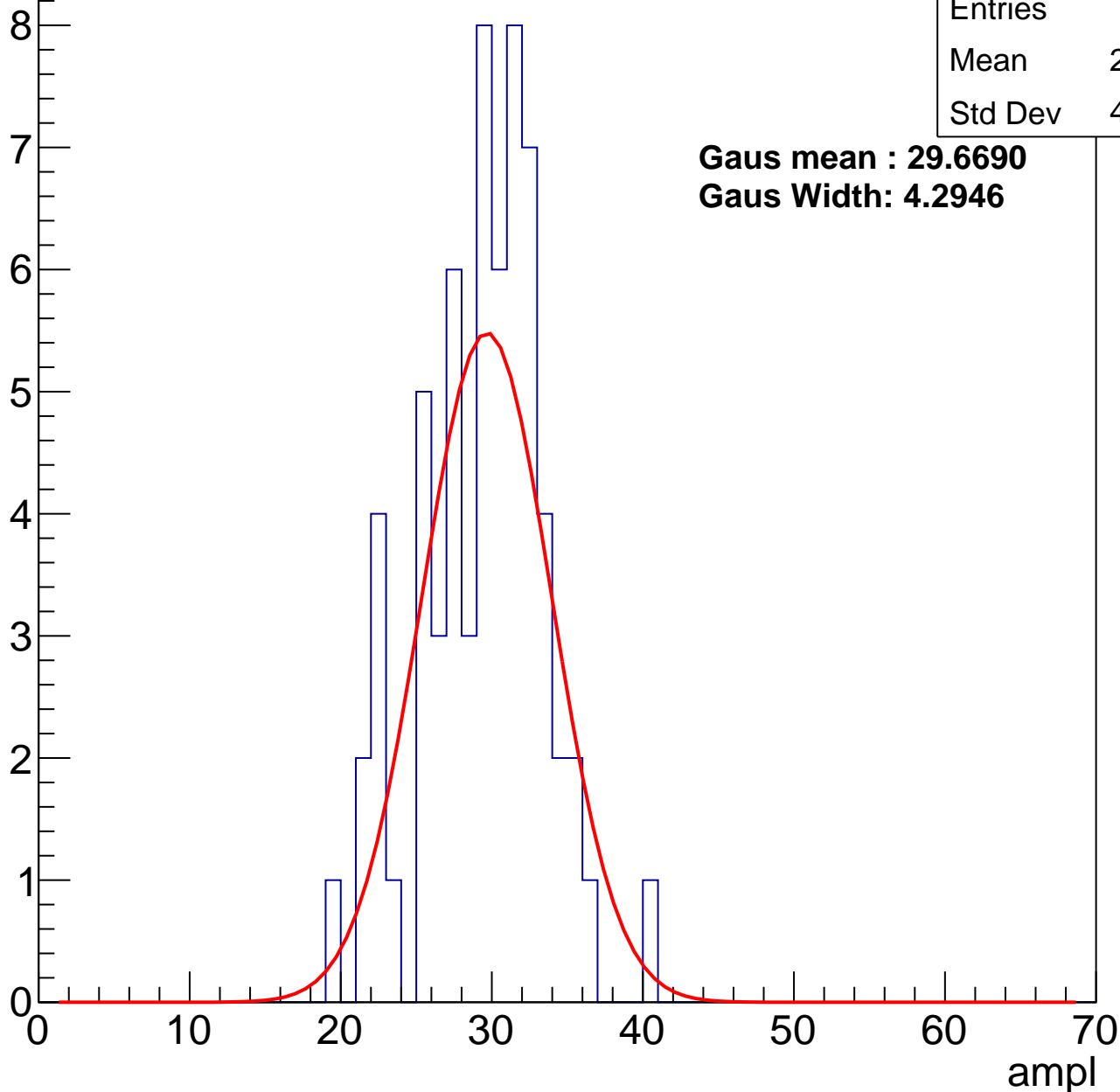
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	28.92
Std Dev	4.052

**Gaus mean : 29.6690**

**Gaus Width: 4.2946**



# B1L103S, U21-ch28, adc1

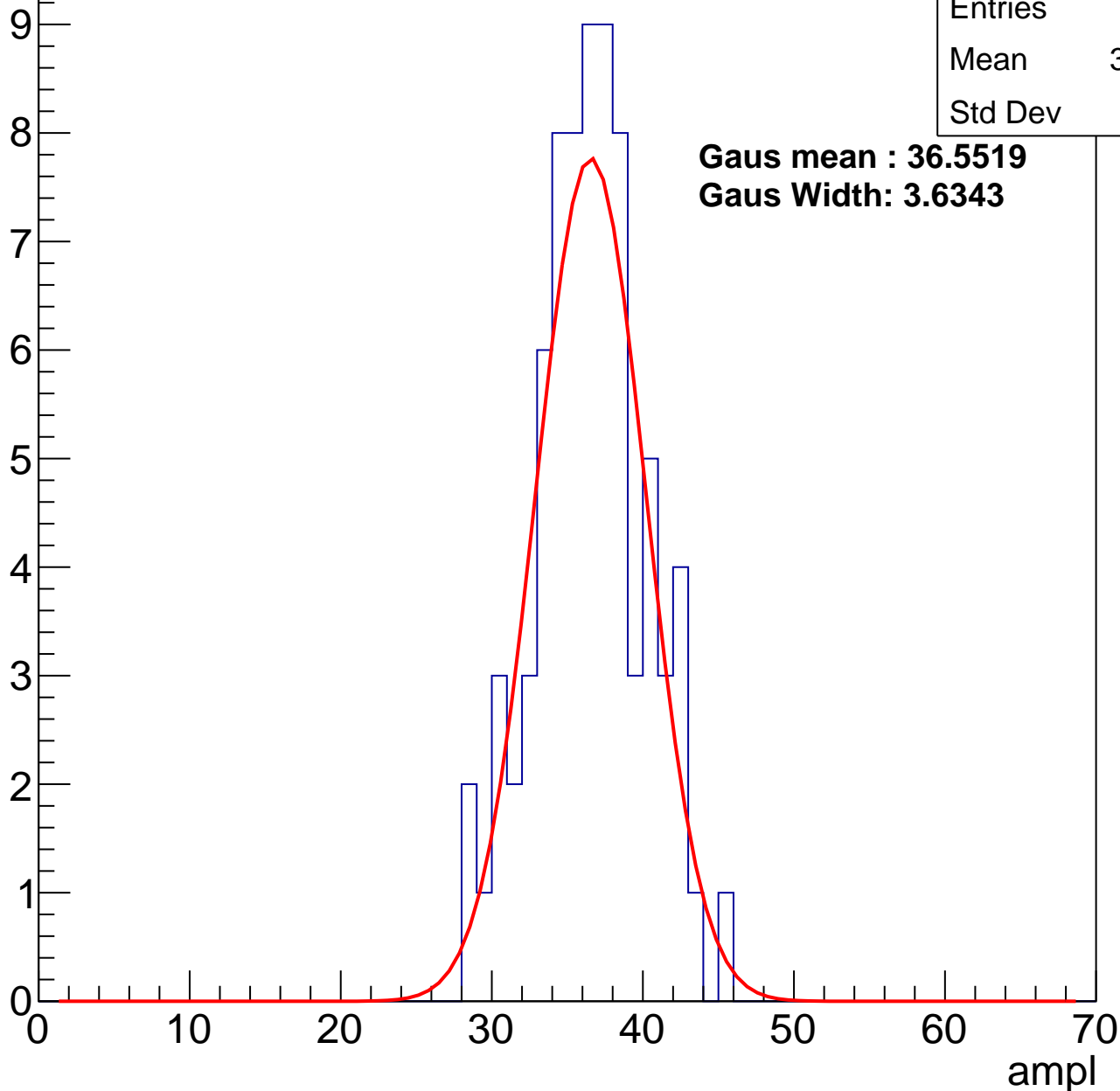
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	36.05
Std Dev	3.58

**Gaus mean : 36.5519**

**Gaus Width: 3.6343**



# B1L103S, U21-ch28, adc2

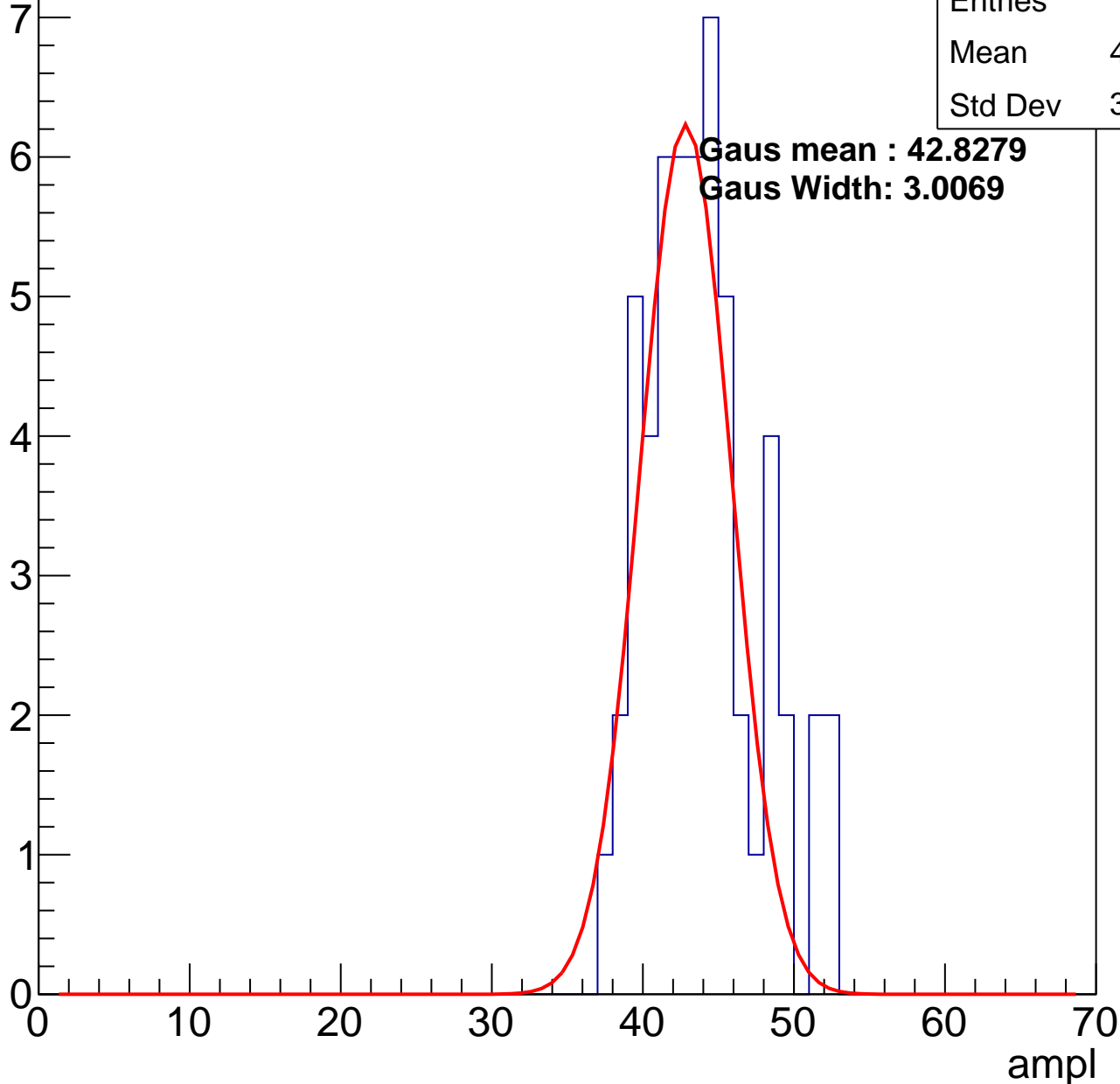
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	43.49
Std Dev	3.672

**Gaus mean : 42.8279**

**Gaus Width: 3.0069**

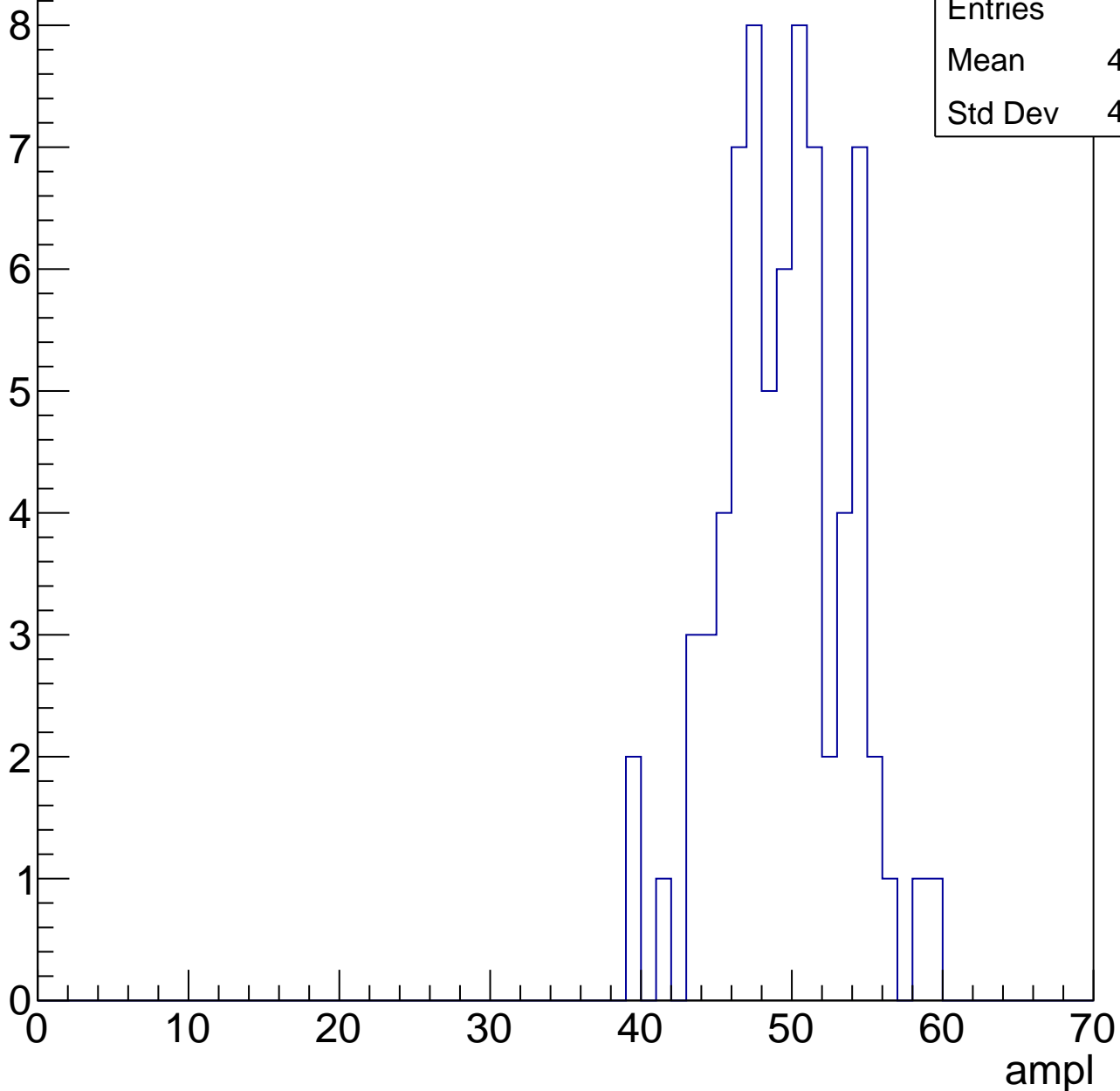


# B1L103S, U21-ch28, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	48.97
Std Dev	4.093

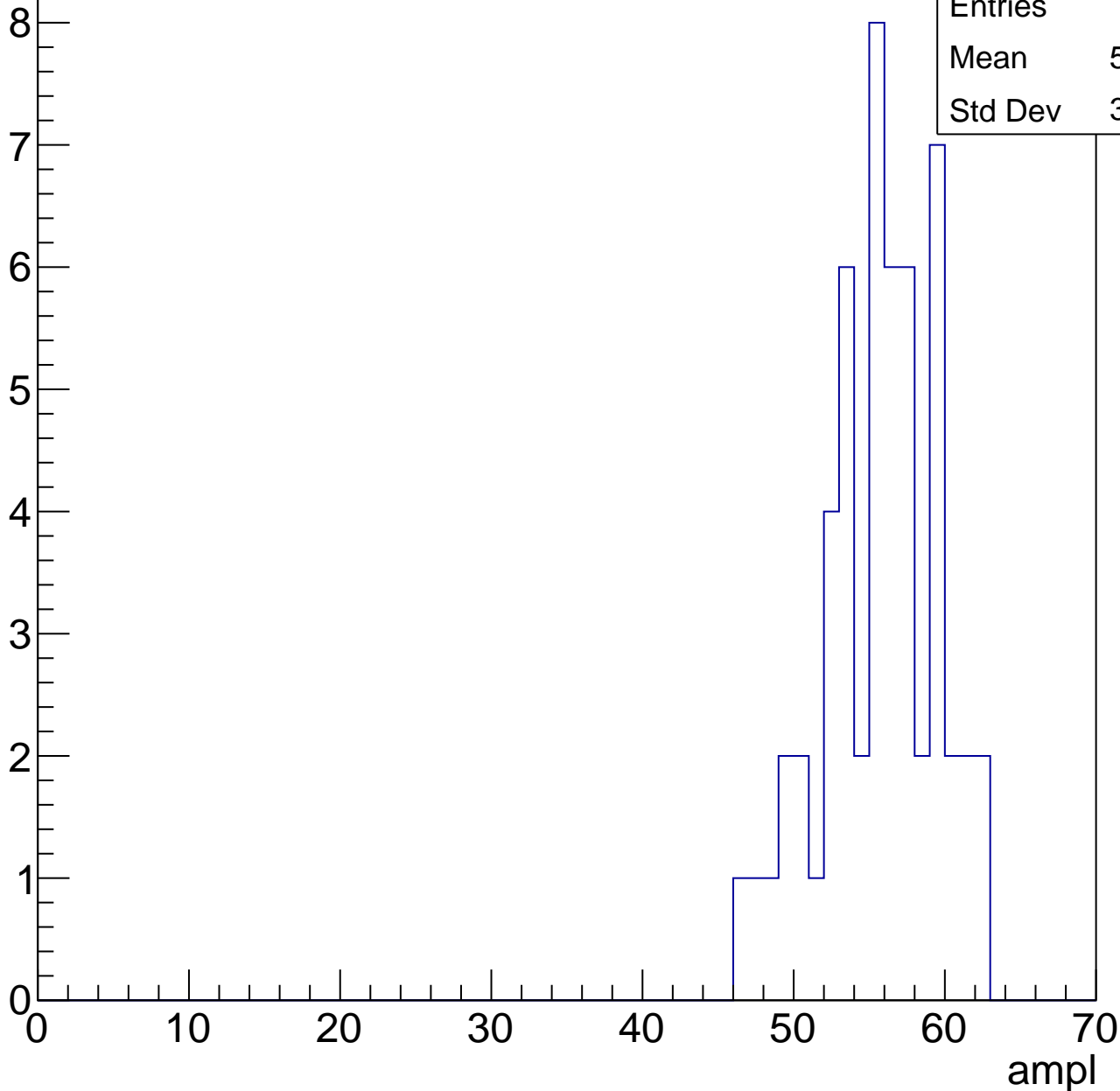


# B1L103S, U21-ch28, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	55.22
Std Dev	3.745

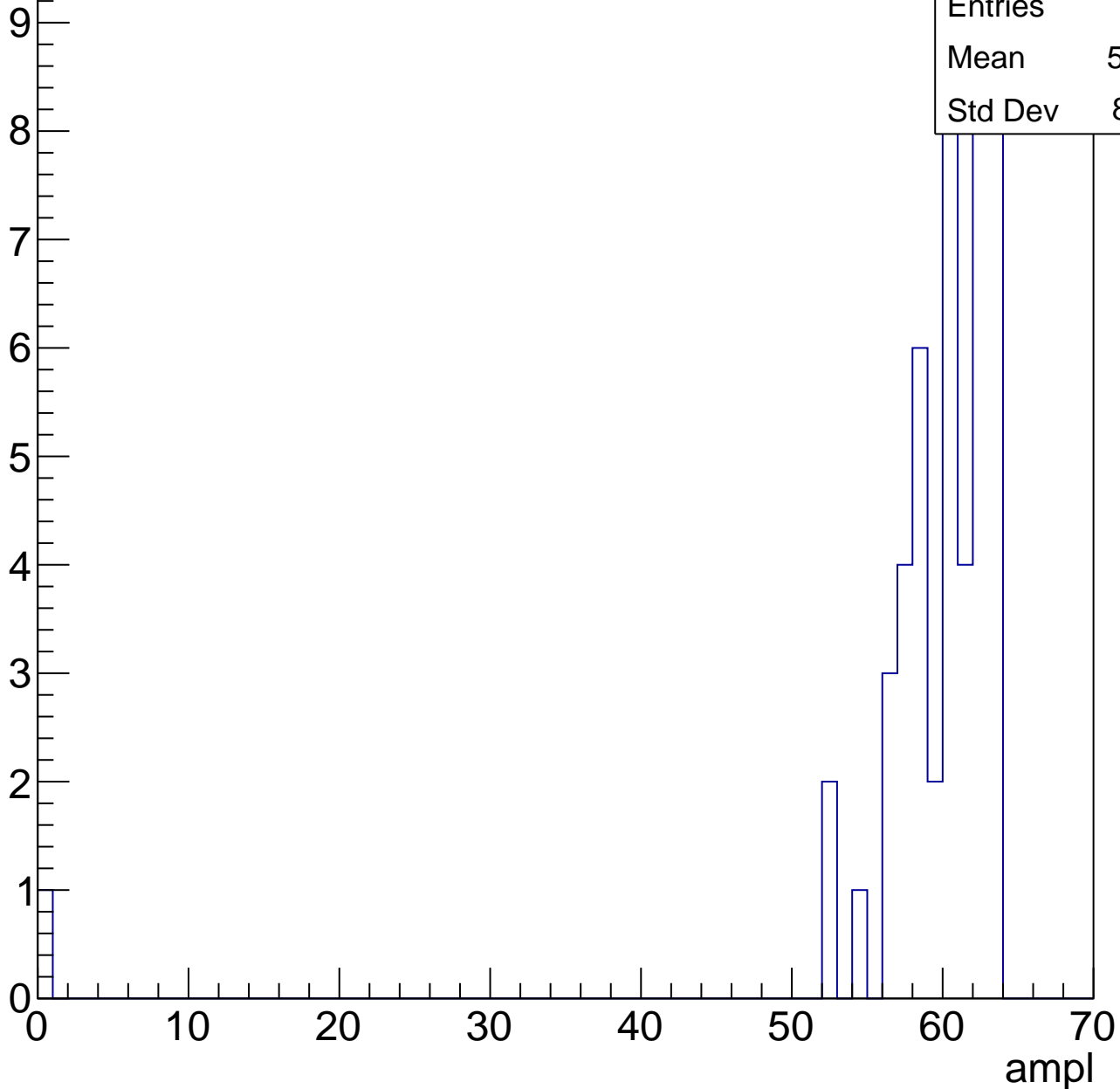


# B1L103S, U21-ch28, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

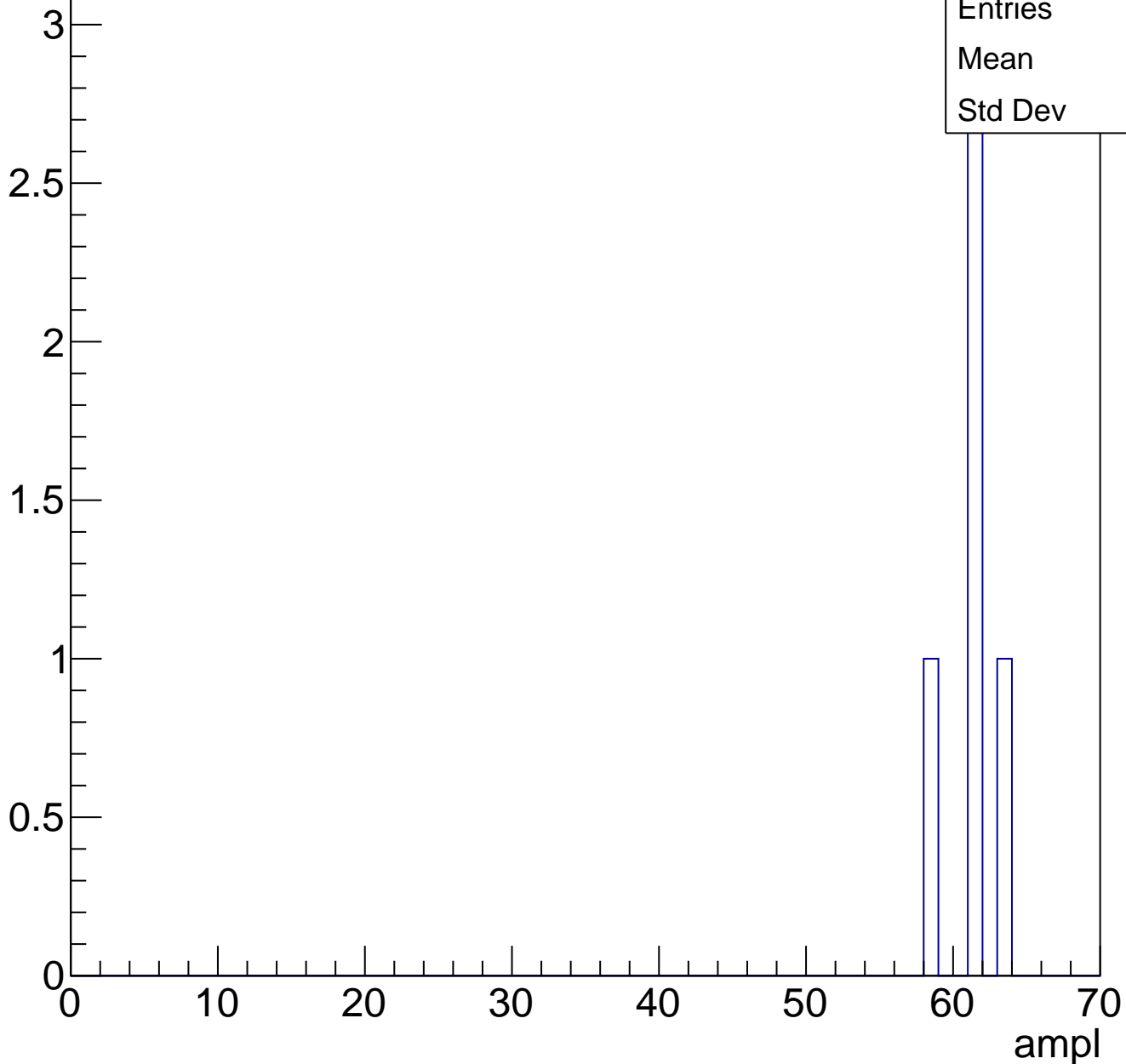
Entries	48
Mean	58.48
Std Dev	8.991



# B1L103S, U21-ch28, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U21-ch28, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U21-ch29, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

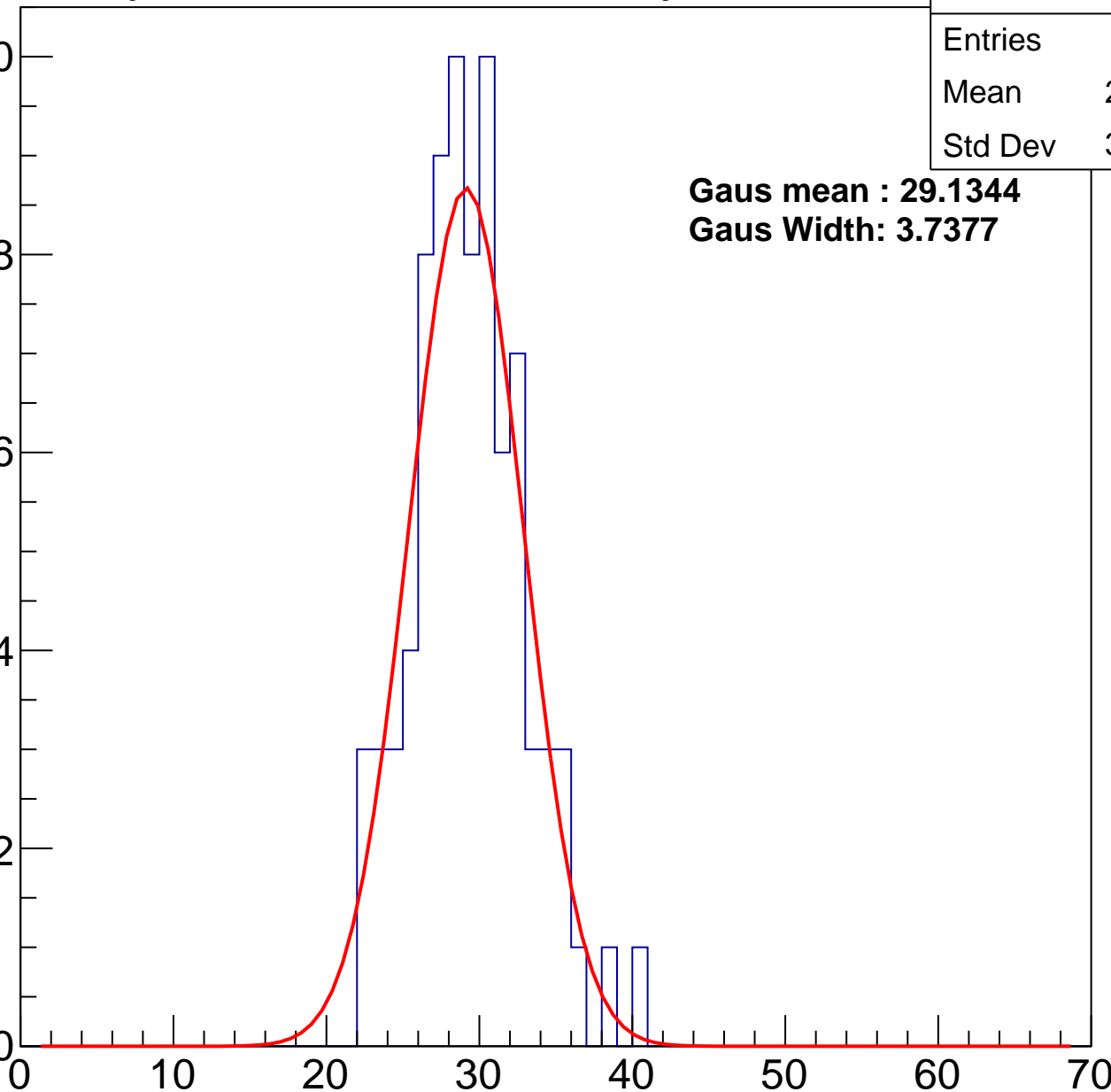
Entries	83
Mean	28.92
Std Dev	3.625

**Gaus mean : 29.1344**

**Gaus Width: 3.7377**

10  
8  
6  
4  
2  
0

ampl



# B1L103S, U21-ch29, adc1

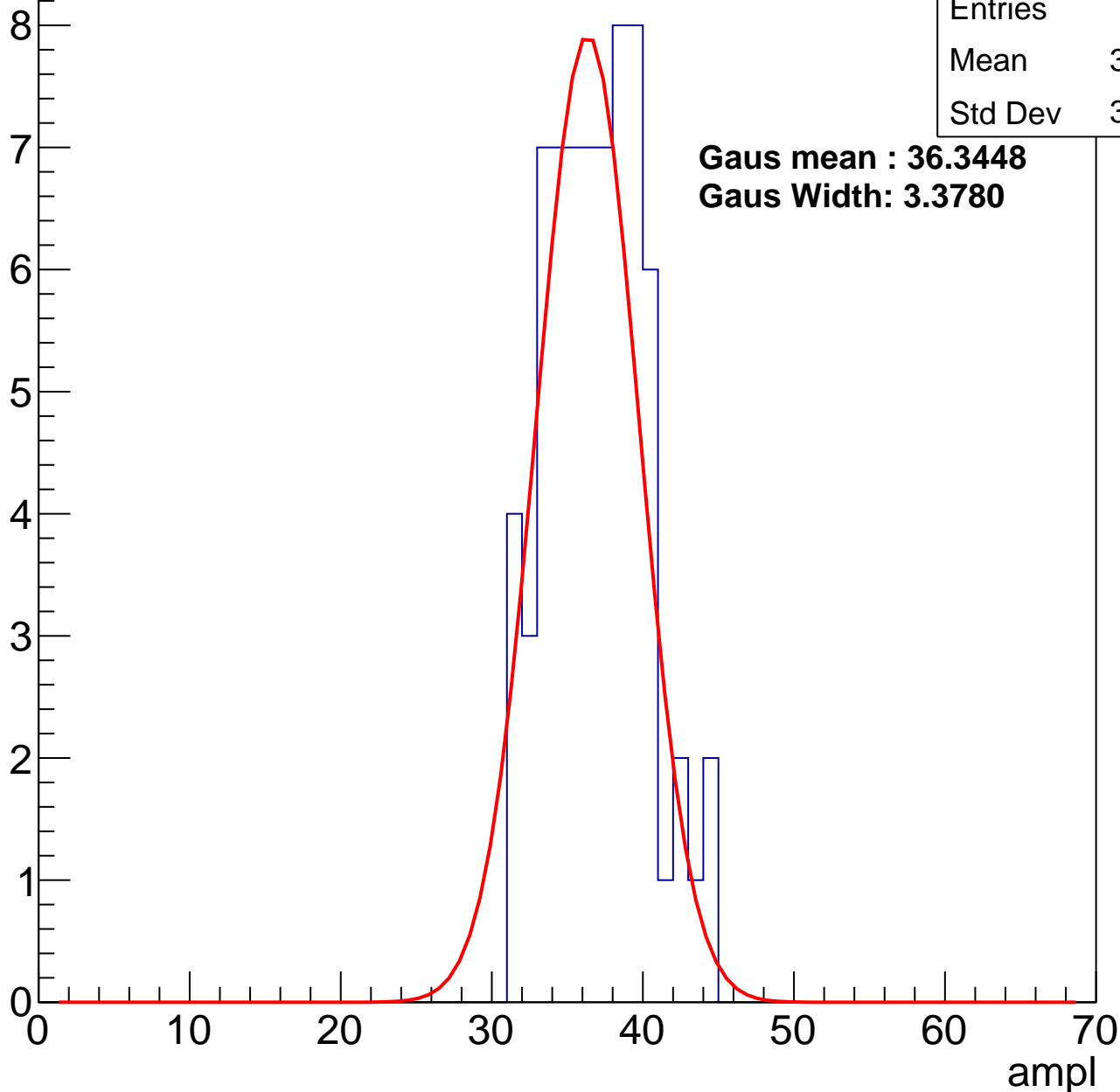
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	36.53
Std Dev	3.179

**Gaus mean : 36.3448**

**Gaus Width: 3.3780**



# B1L103S, U21-ch29, adc2

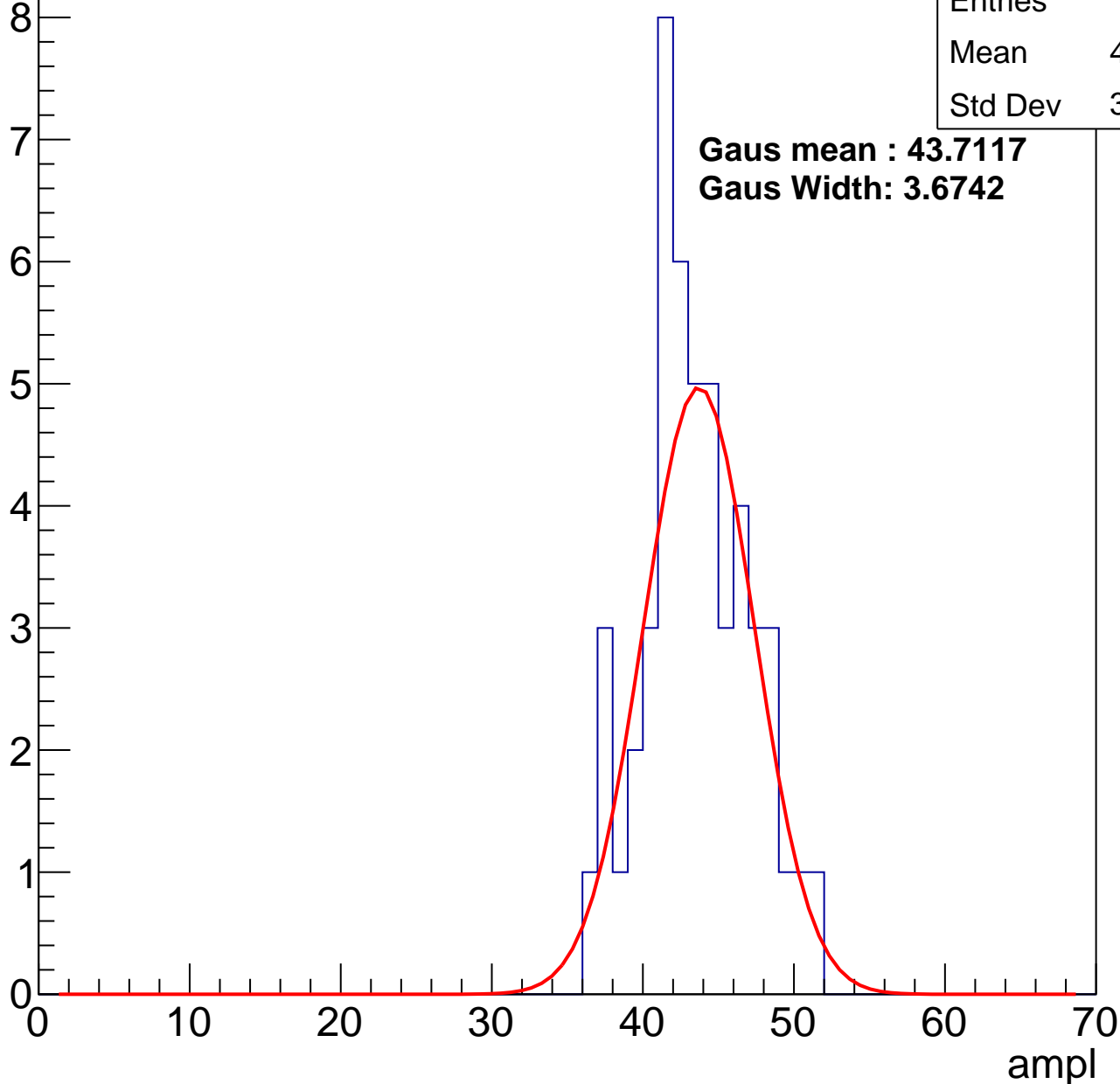
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	43.04
Std Dev	3.475

**Gaus mean : 43.7117**

**Gaus Width: 3.6742**

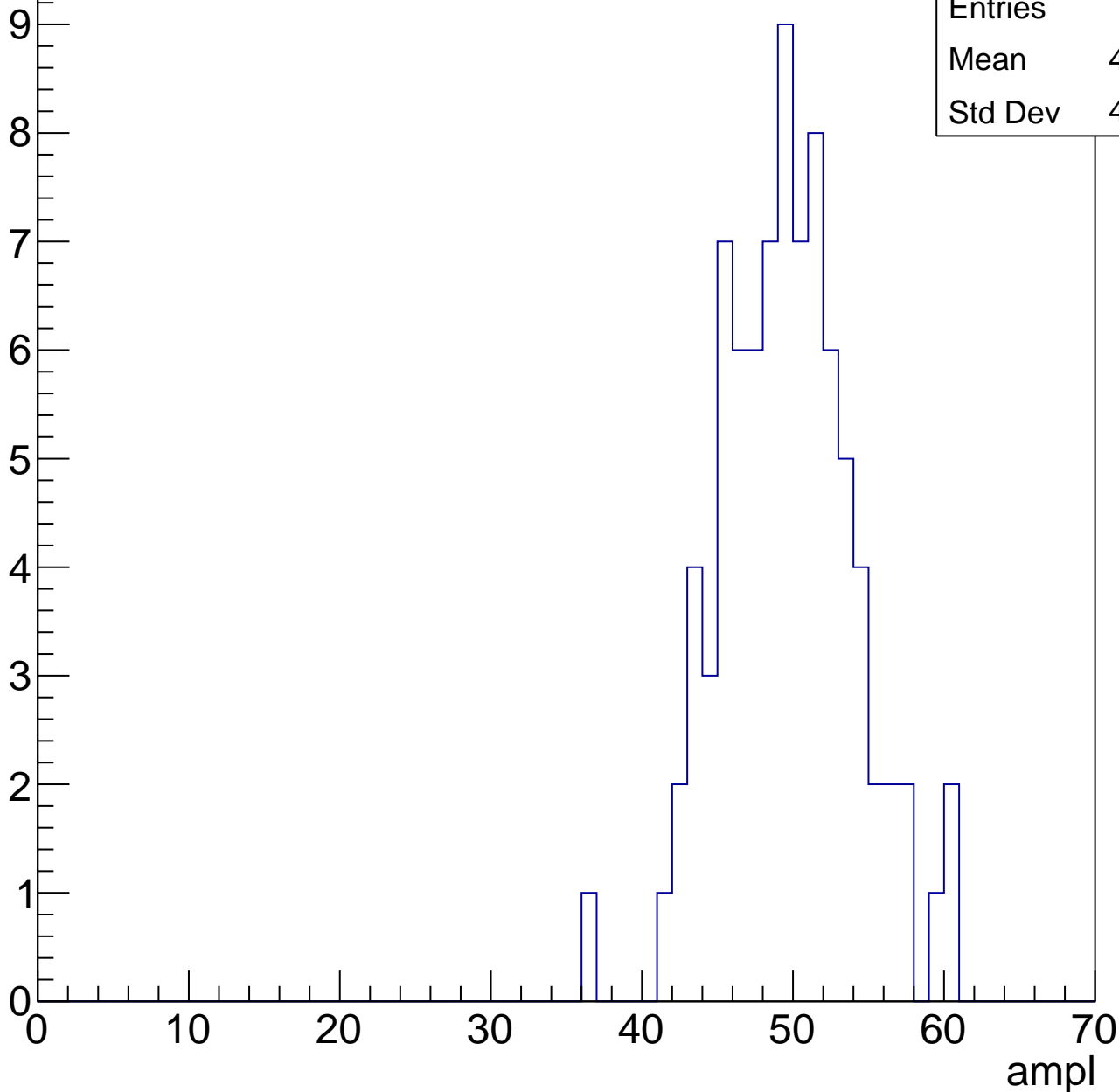


# B1L103S, U21-ch29, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	85
Mean	49.19
Std Dev	4.415

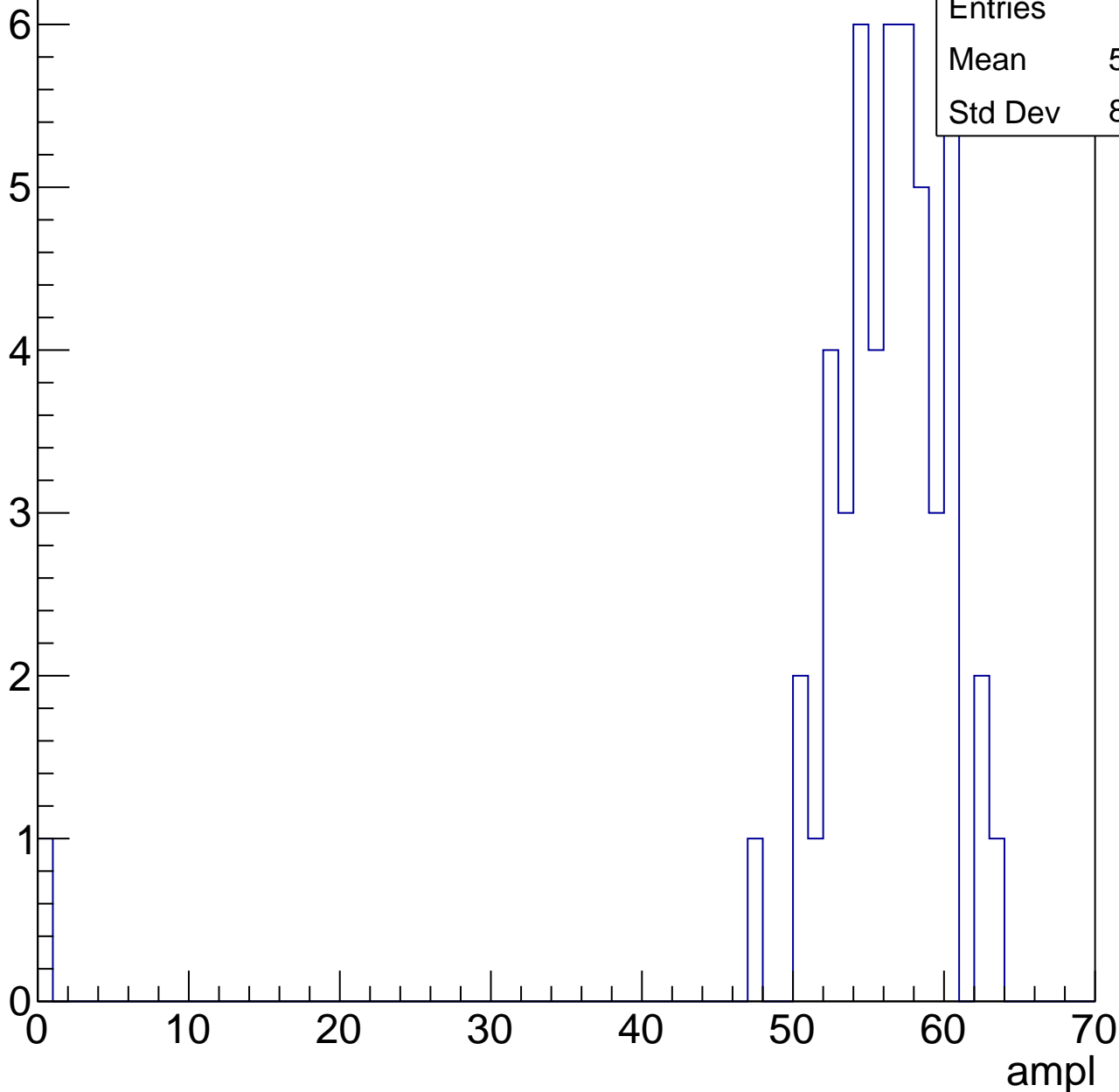


# B1L103S, U21-ch29, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	54.92
Std Dev	8.453

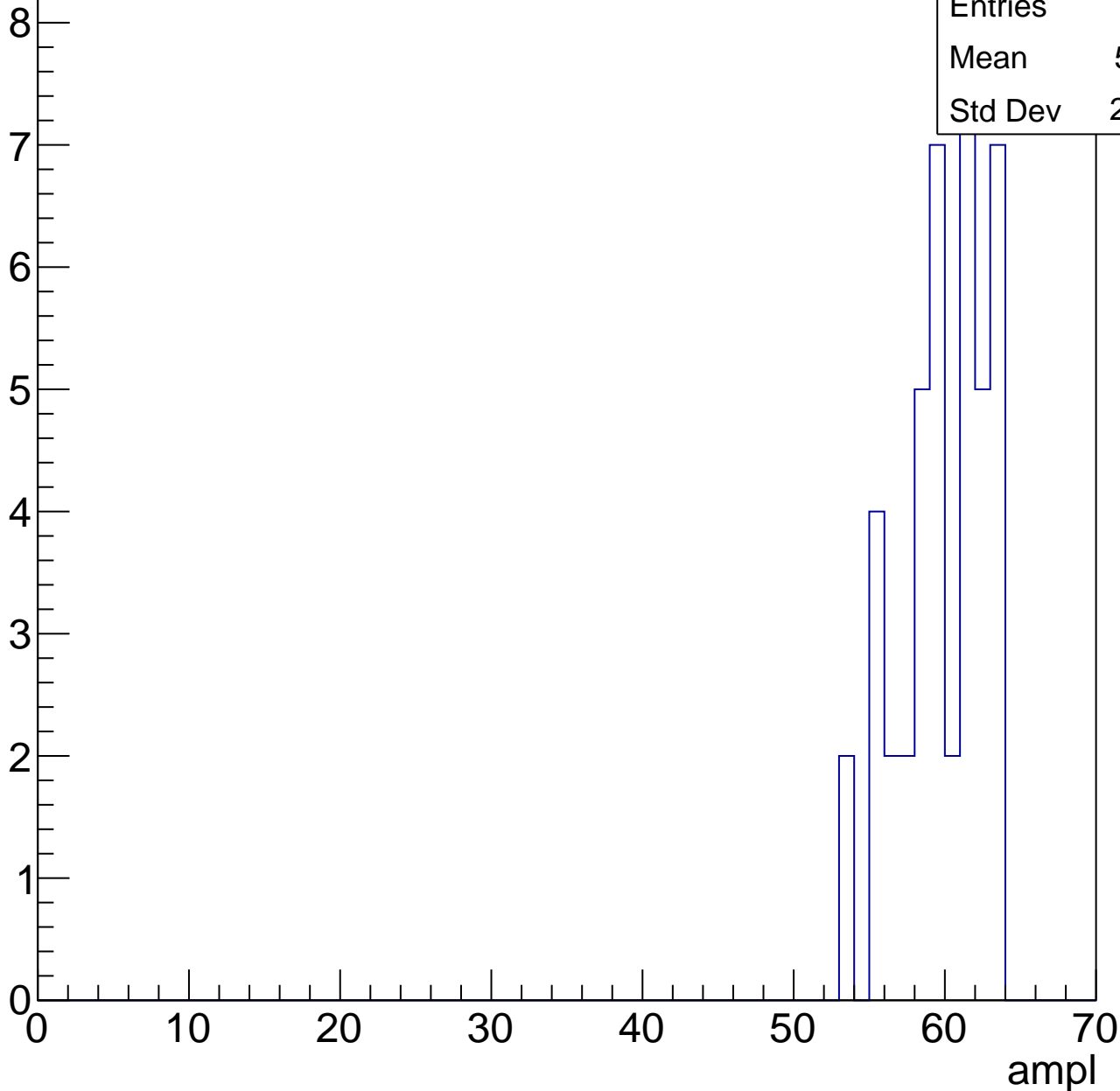


# B1L103S, U21-ch29, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

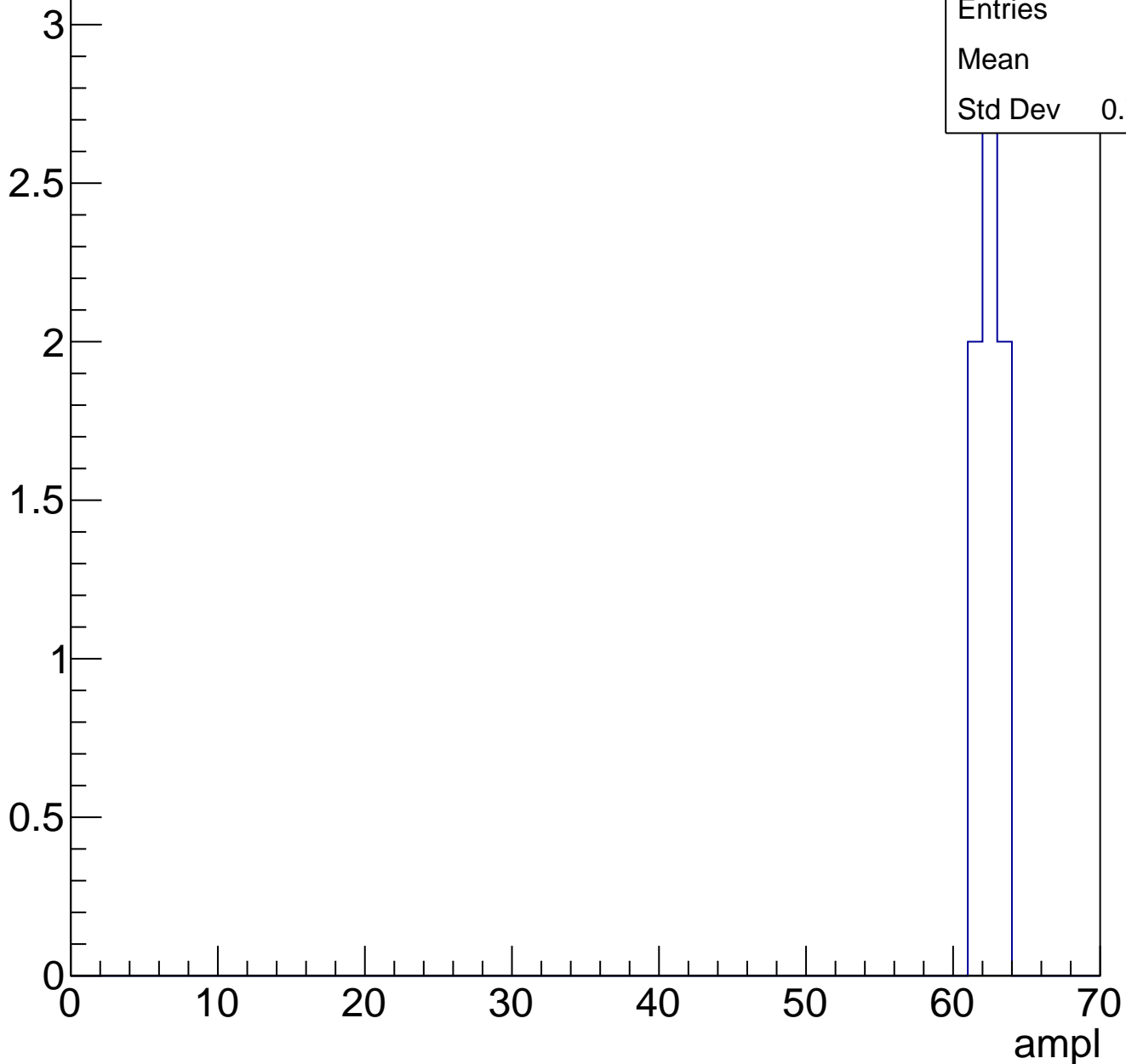
Entries	44
Mean	59.41
Std Dev	2.823



# B1L103S, U21-ch29, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U21-ch29, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U21-ch30, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	84
Mean	28.67
Std Dev	6.439

**Gaus mean : 30.6630**

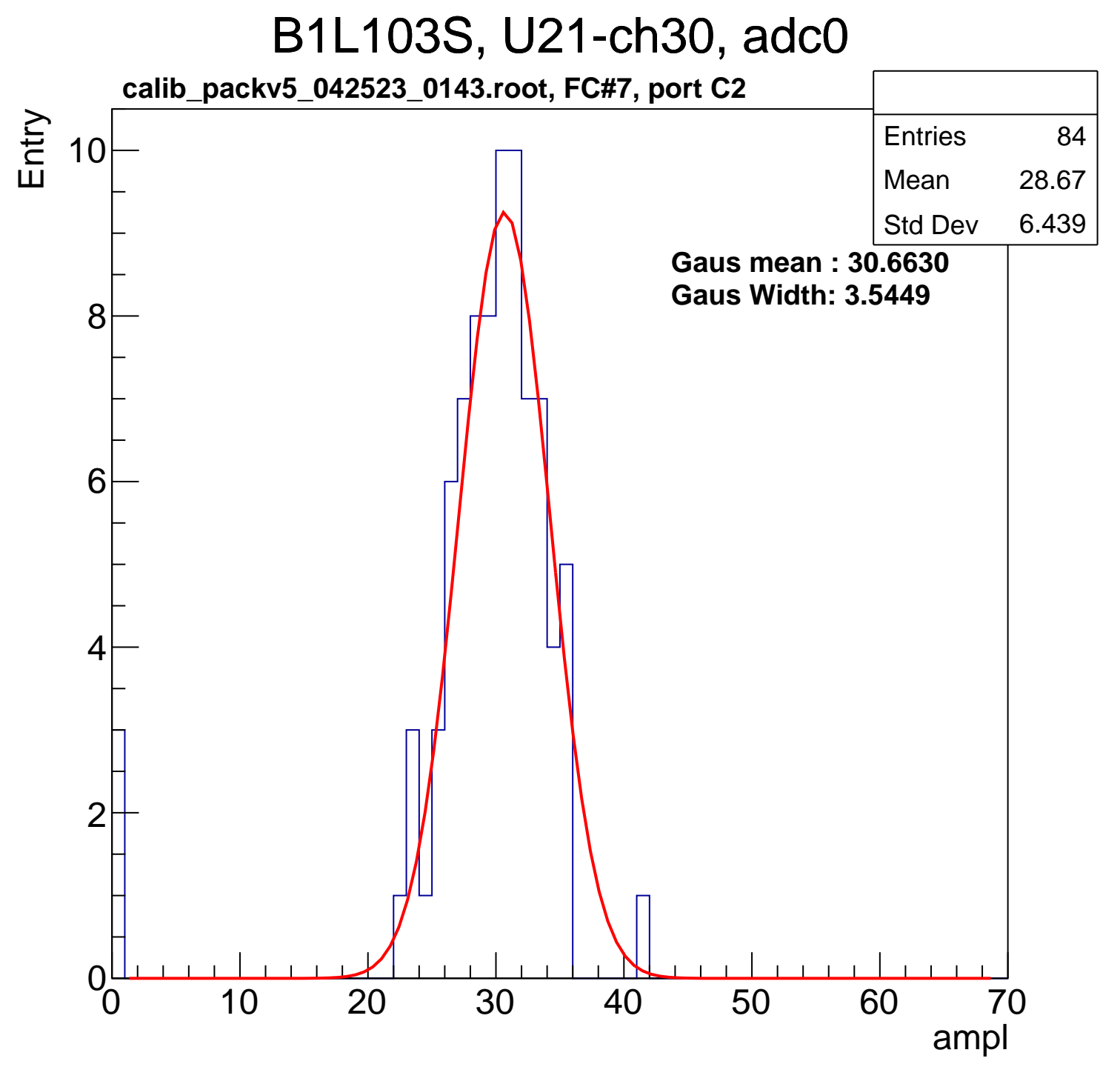
**Gaus Width: 3.5449**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U21-ch30, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	74
Mean	37.8
Std Dev	3.579

**Gaus mean : 37.8765**

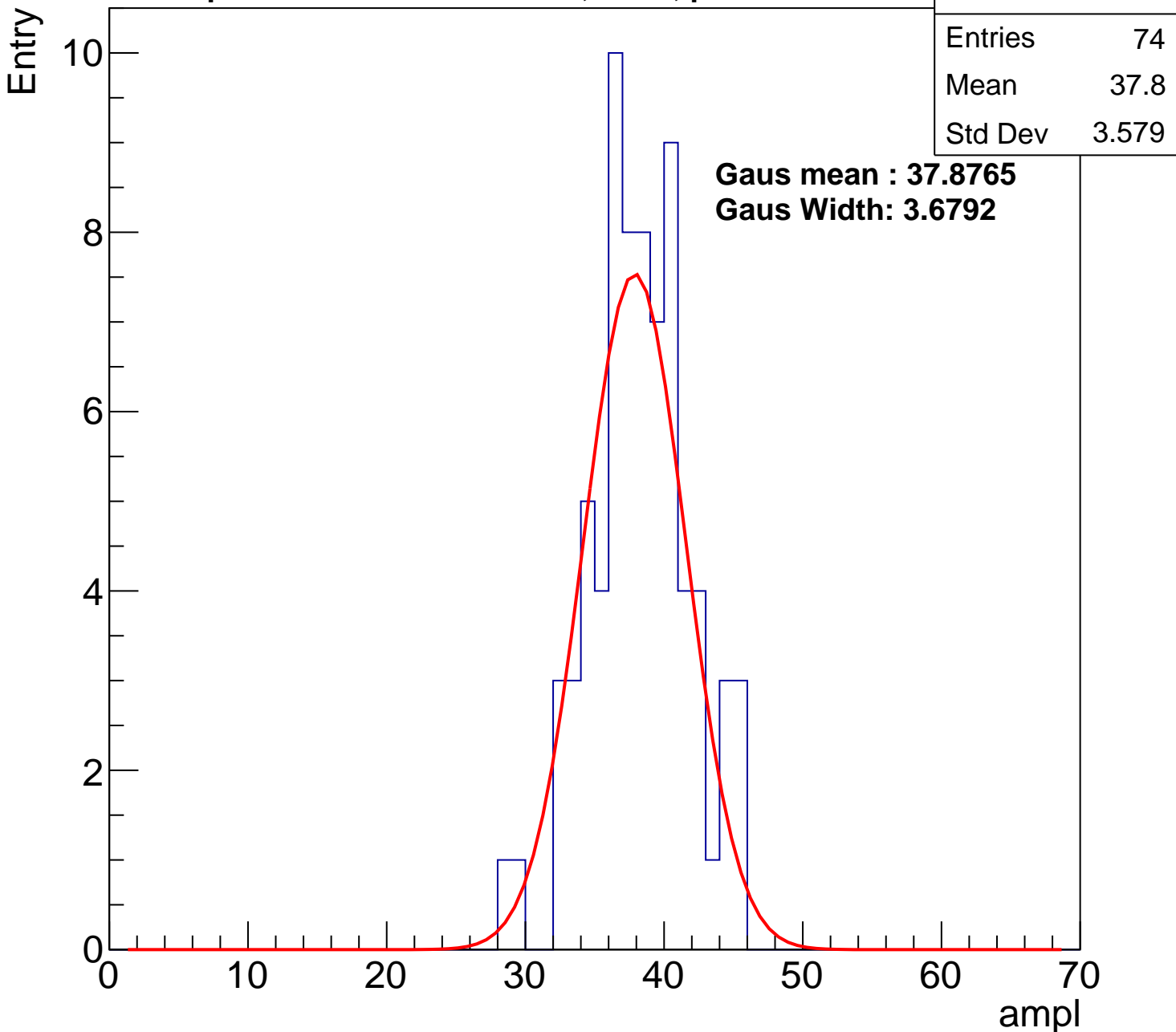
**Gaus Width: 3.6792**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L103S, U21-ch30, adc2

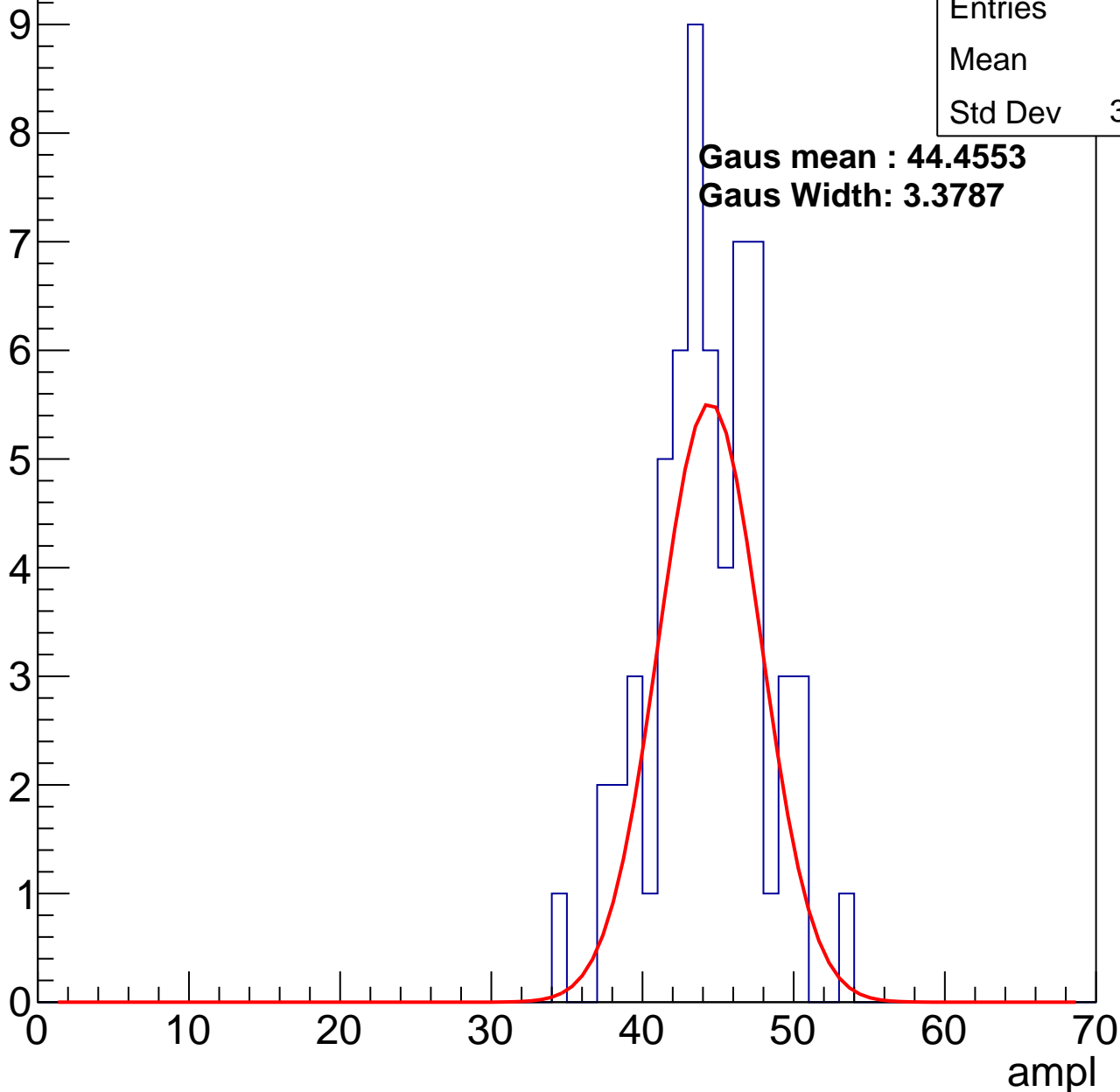
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	43.9
Std Dev	3.652

**Gaus mean : 44.4553**

**Gaus Width: 3.3787**

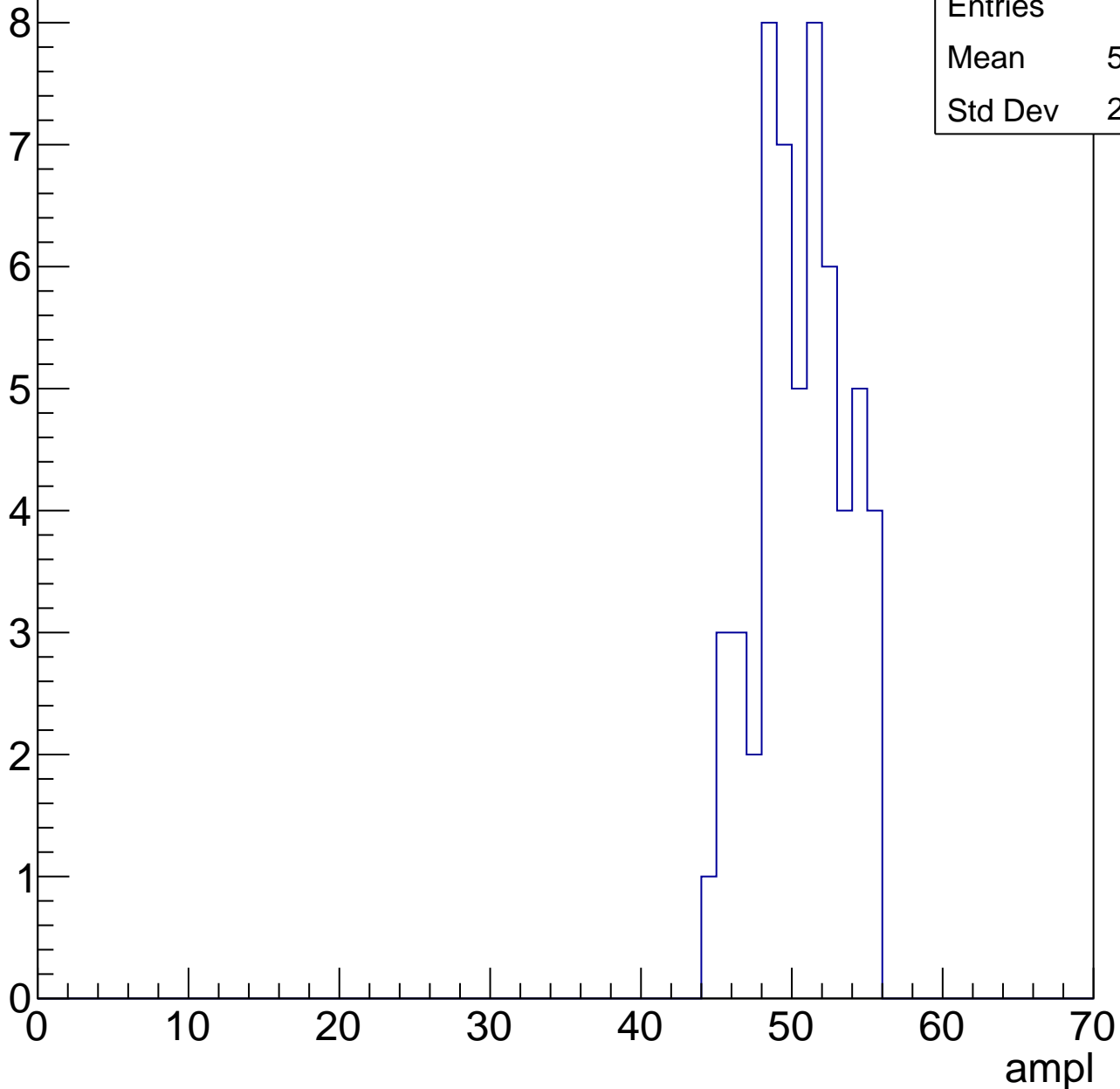


# B1L103S, U21-ch30, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	50.18
Std Dev	2.873

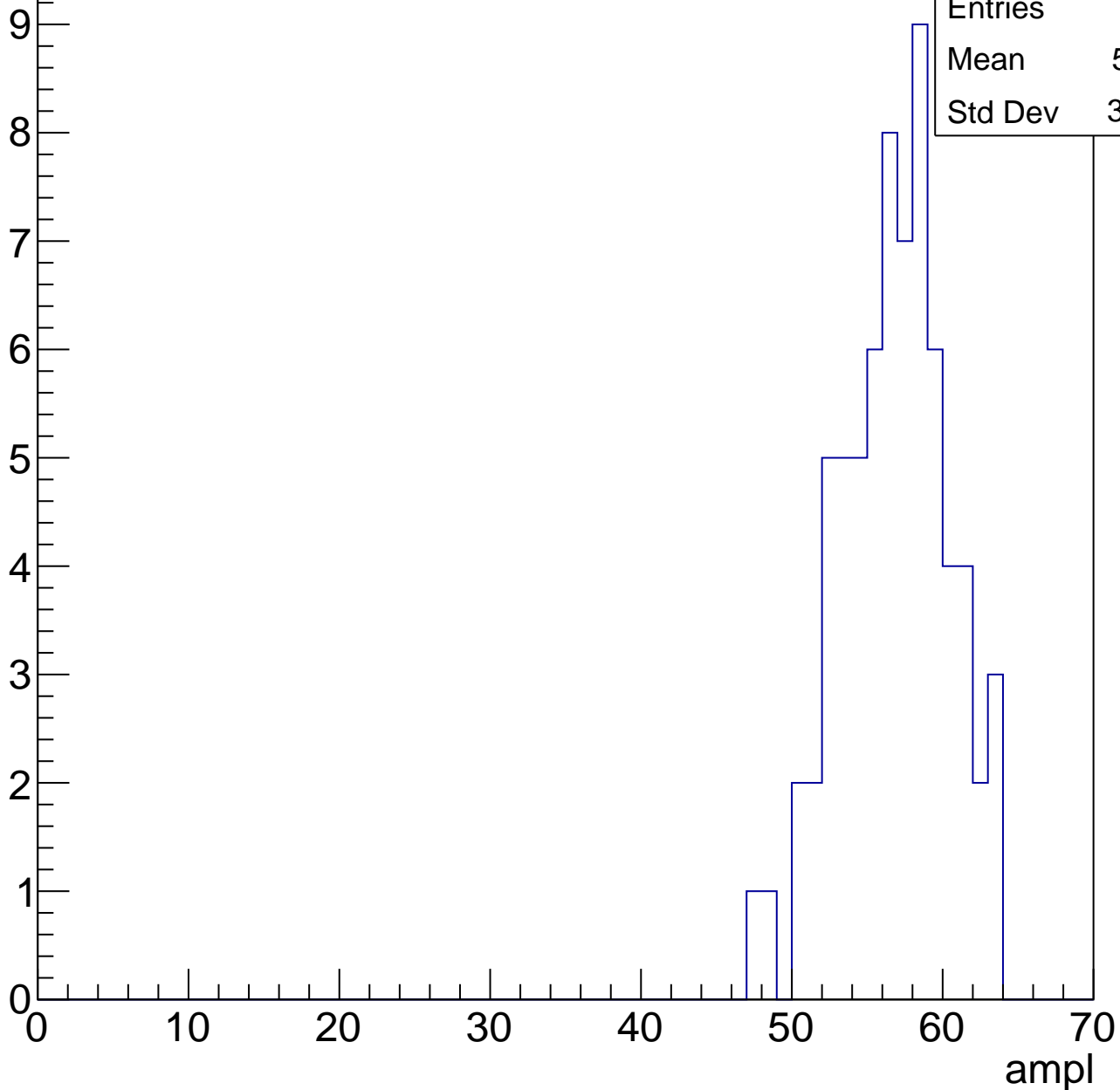


# B1L103S, U21-ch30, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

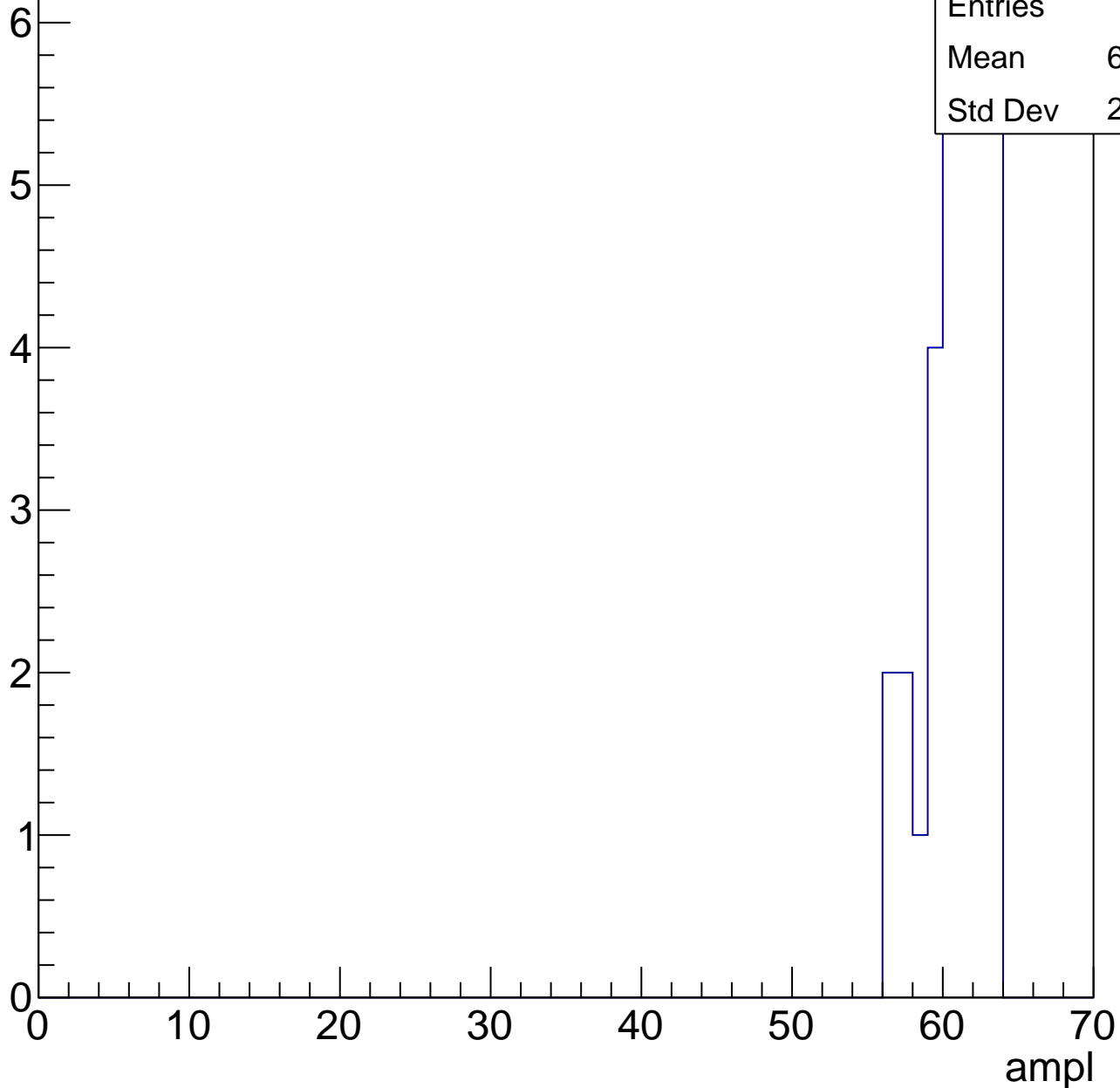
Entries	70
Mean	56.31
Std Dev	3.568



# B1L103S, U21-ch30, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

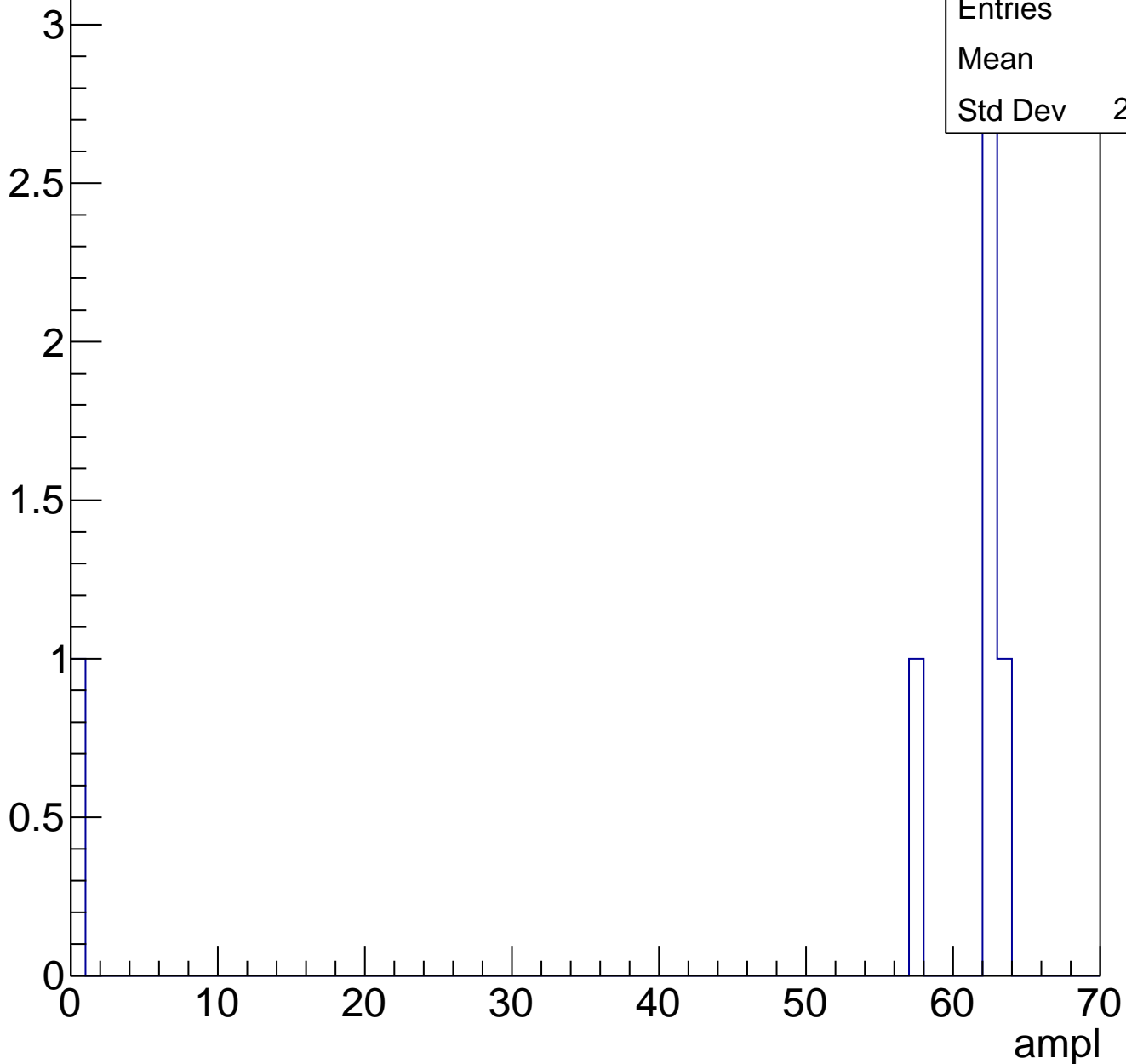


Entries	33
Mean	60.48
Std Dev	2.017

# B1L103S, U21-ch30, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U21-ch30, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U21-ch31, adc0

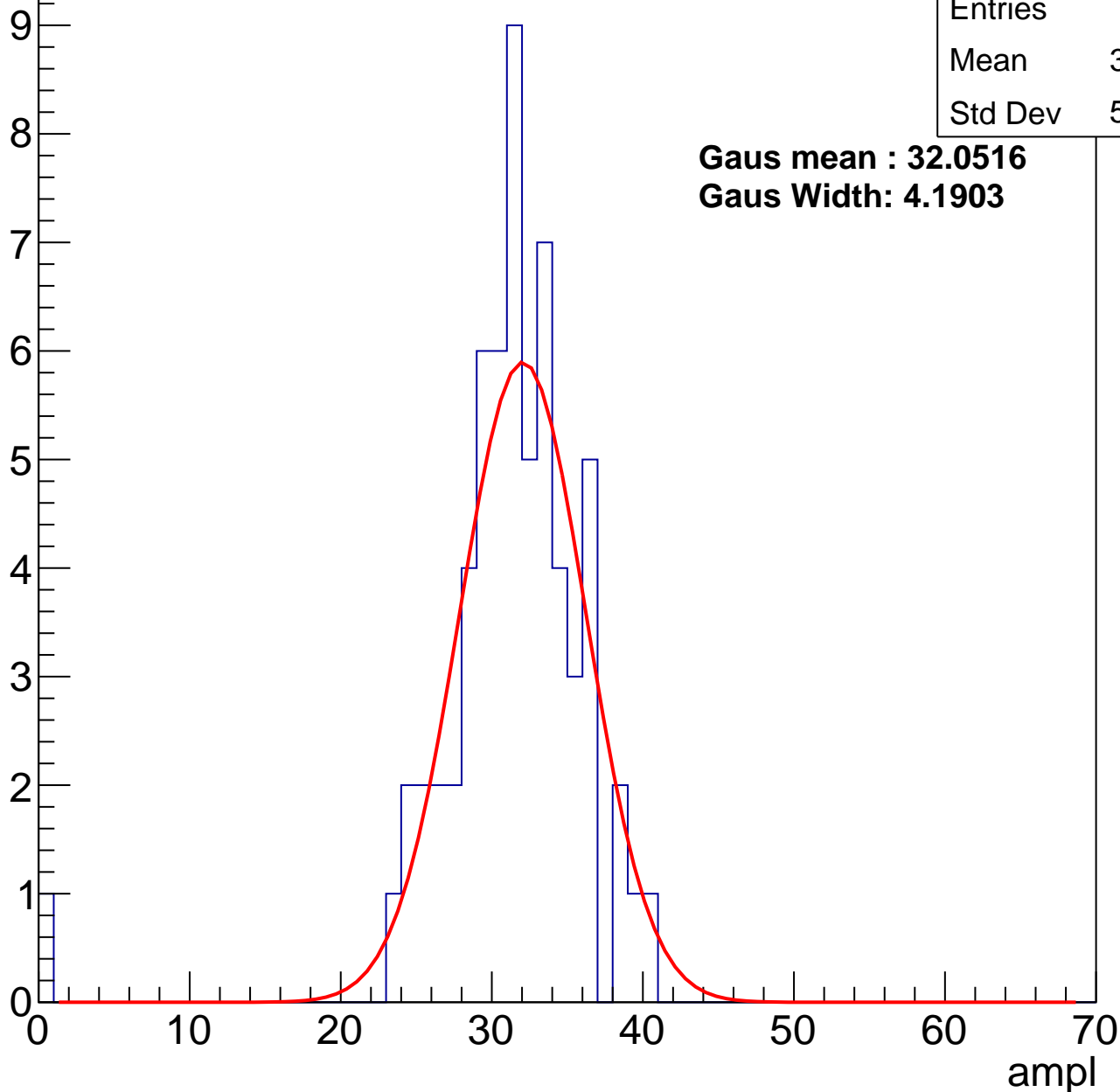
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	30.78
Std Dev	5.382

**Gaus mean : 32.0516**

**Gaus Width: 4.1903**



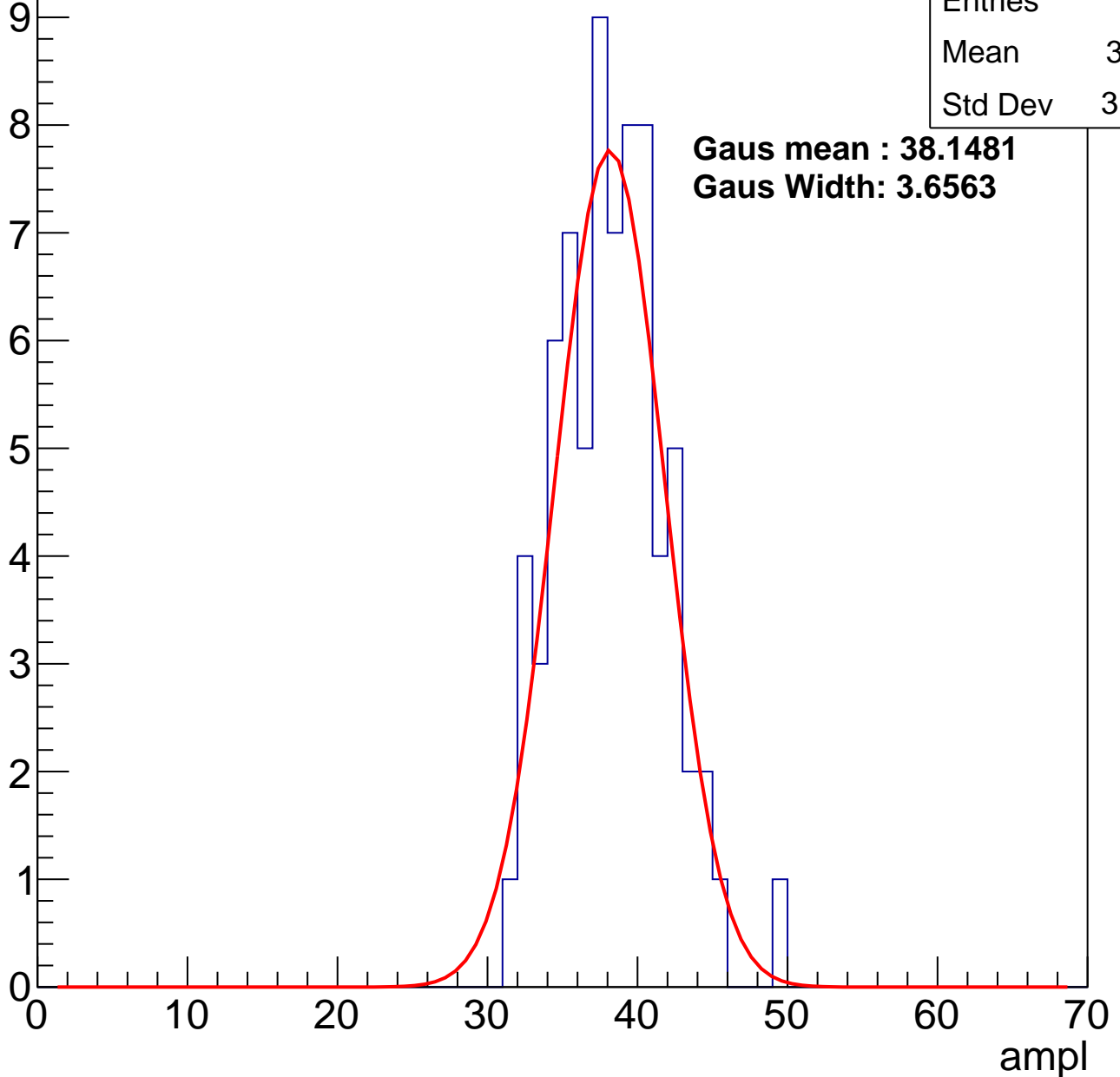
# B1L103S, U21-ch31, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

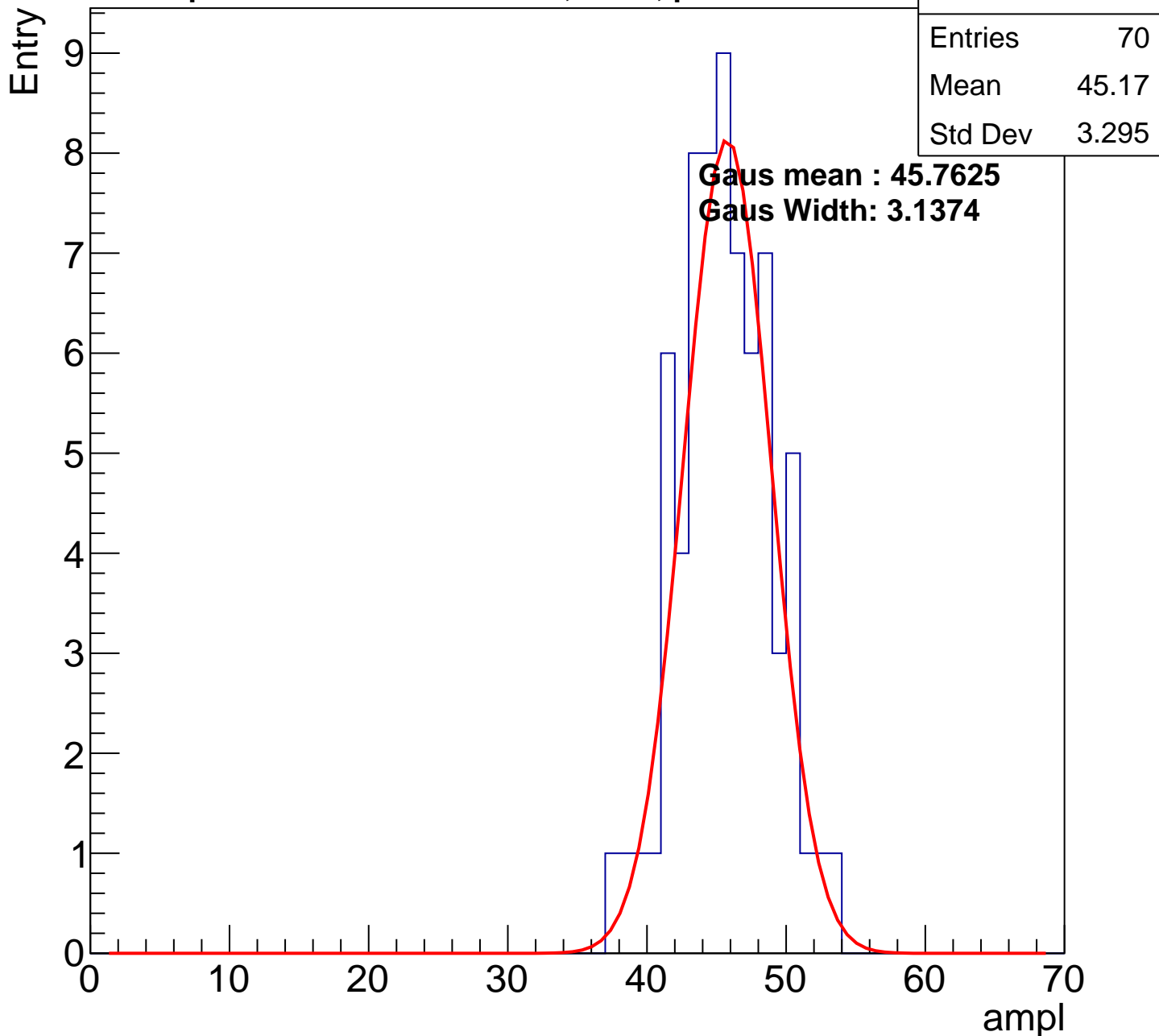
Entries	73
Mean	37.81
Std Dev	3.514

**Gaus mean : 38.1481**  
**Gaus Width: 3.6563**



# B1L103S, U21-ch31, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

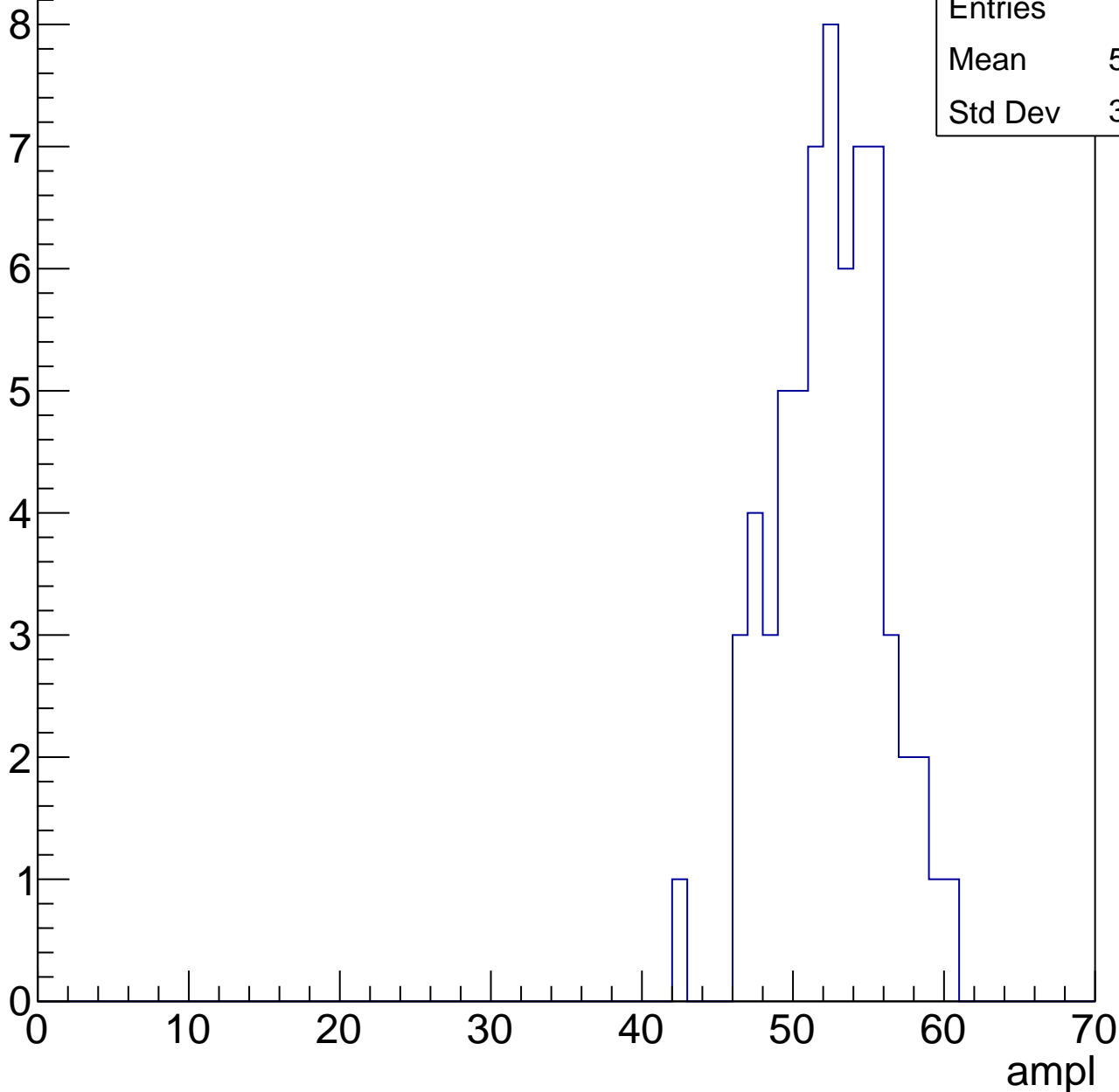


# B1L103S, U21-ch31, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	51.97
Std Dev	3.526

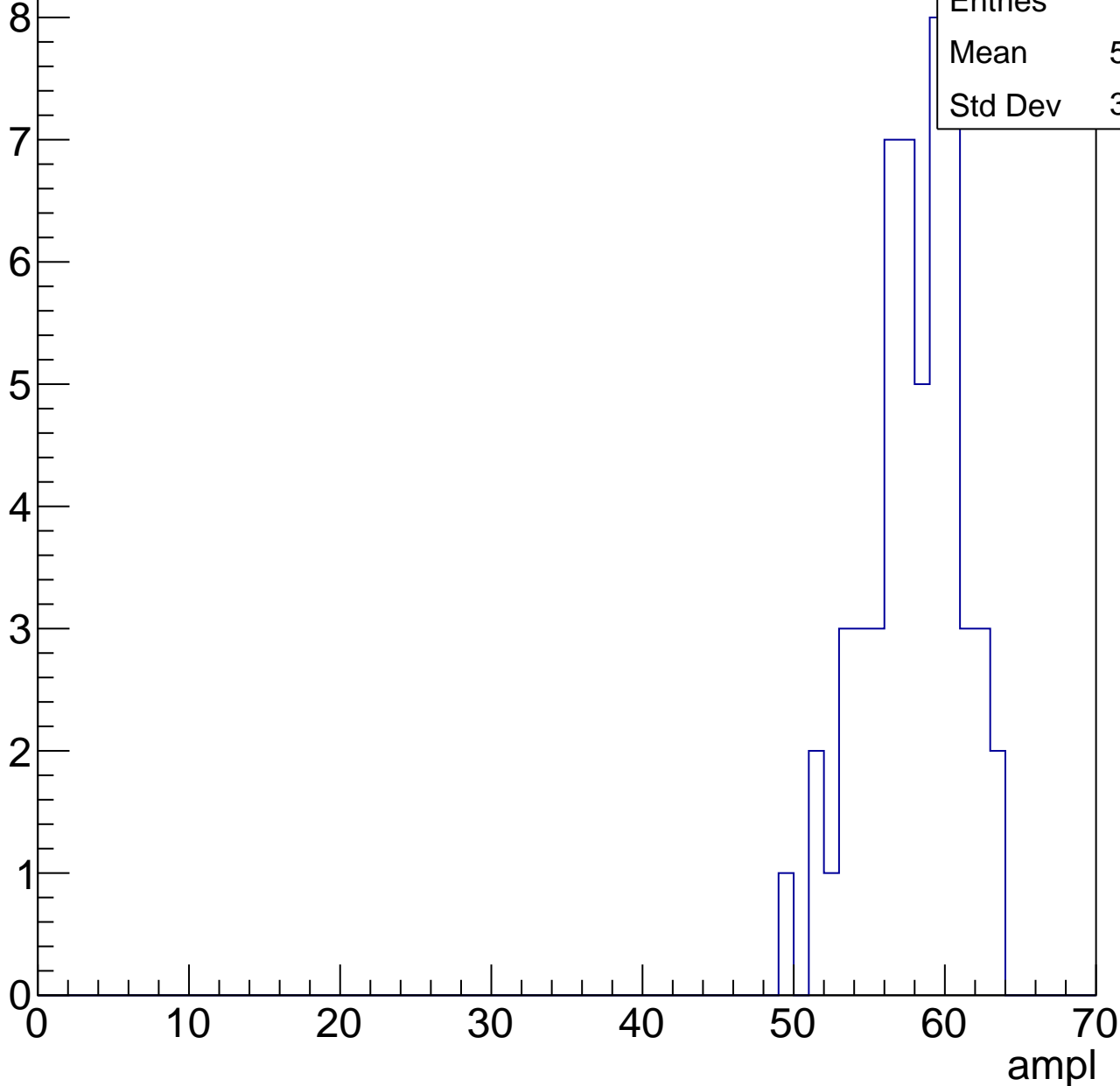


# B1L103S, U21-ch31, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	57.45
Std Dev	3.128

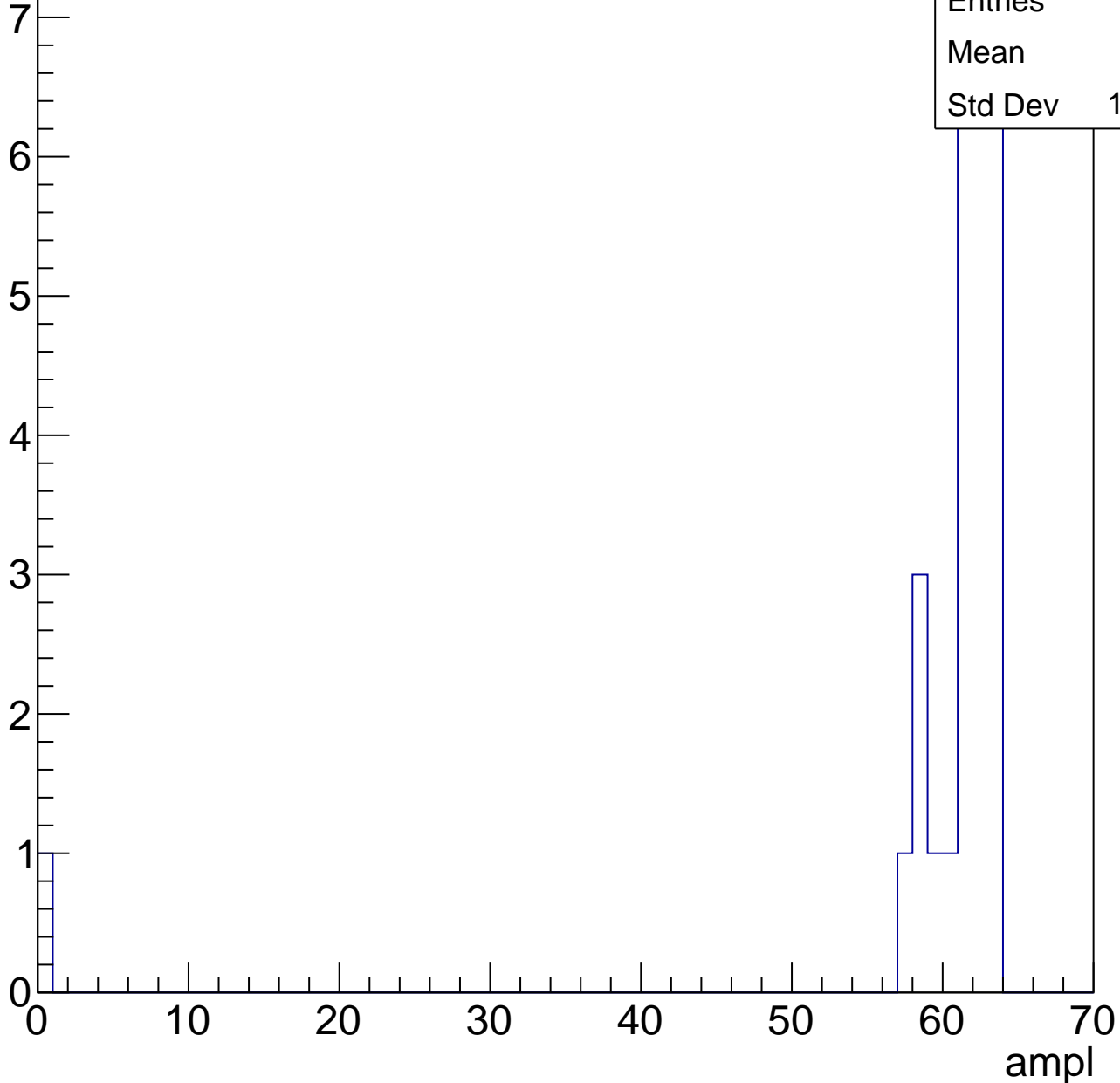


# B1L103S, U21-ch31, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	28
Mean	59
Std Dev	11.48



# B1L103S, U21-ch31, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U21-ch31, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U21-ch32, adc0

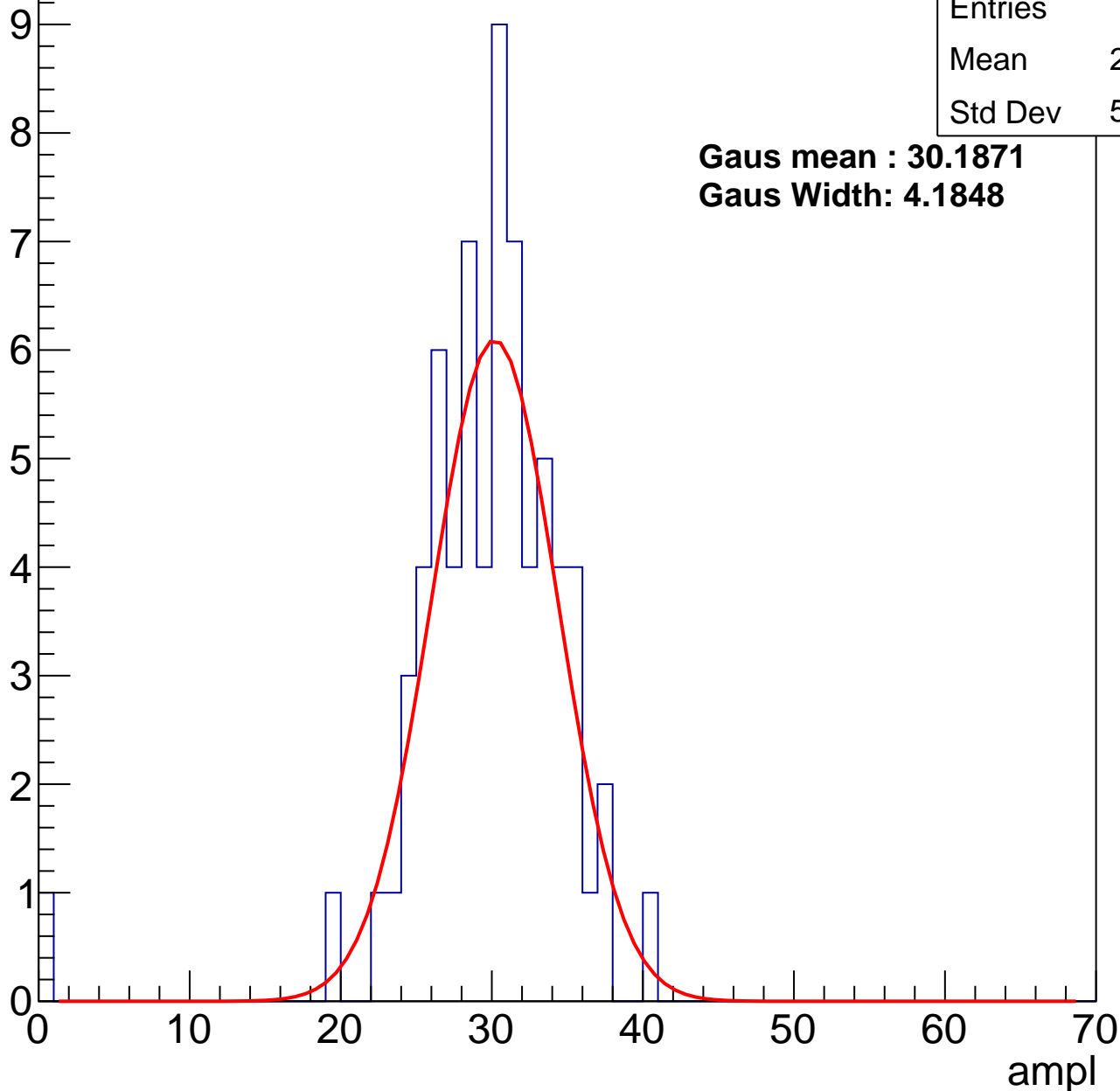
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	29.25
Std Dev	5.293

**Gaus mean : 30.1871**

**Gaus Width: 4.1848**



# B1L103S, U21-ch32, adc1

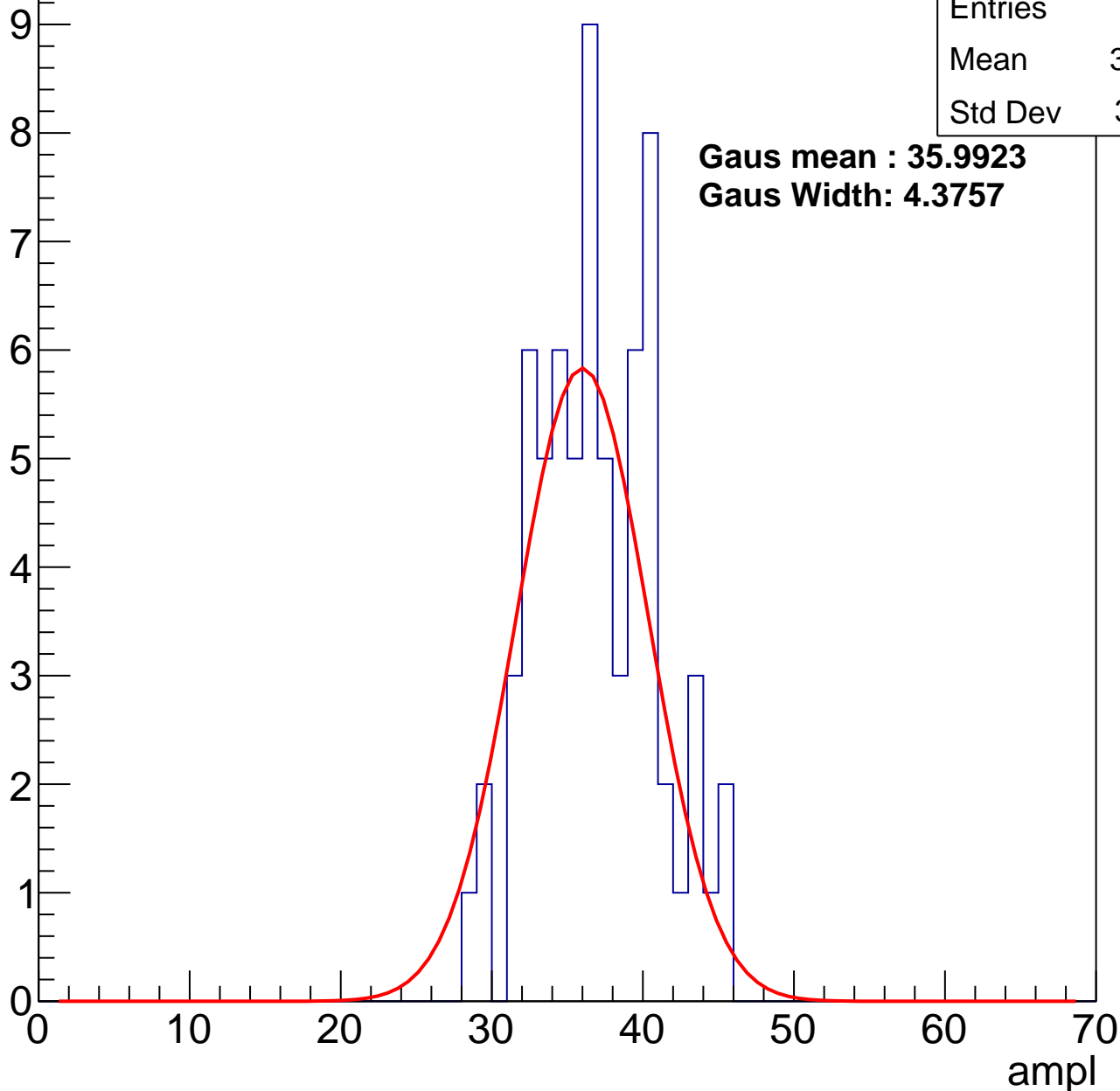
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	36.46
Std Dev	3.931

**Gaus mean : 35.9923**

**Gaus Width: 4.3757**



# B1L103S, U21-ch32, adc2

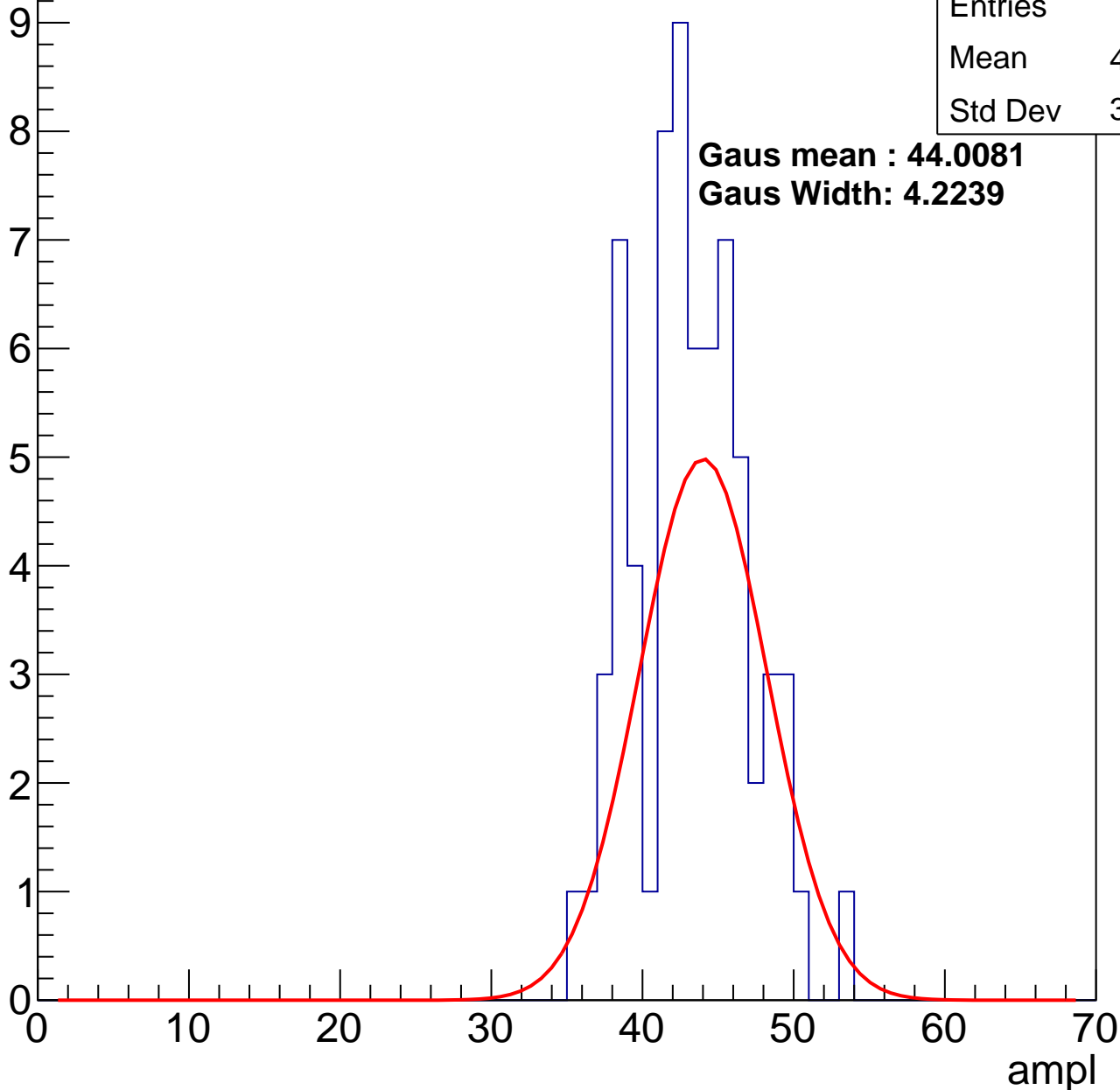
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	42.72
Std Dev	3.733

**Gaus mean : 44.0081**

**Gaus Width: 4.2239**

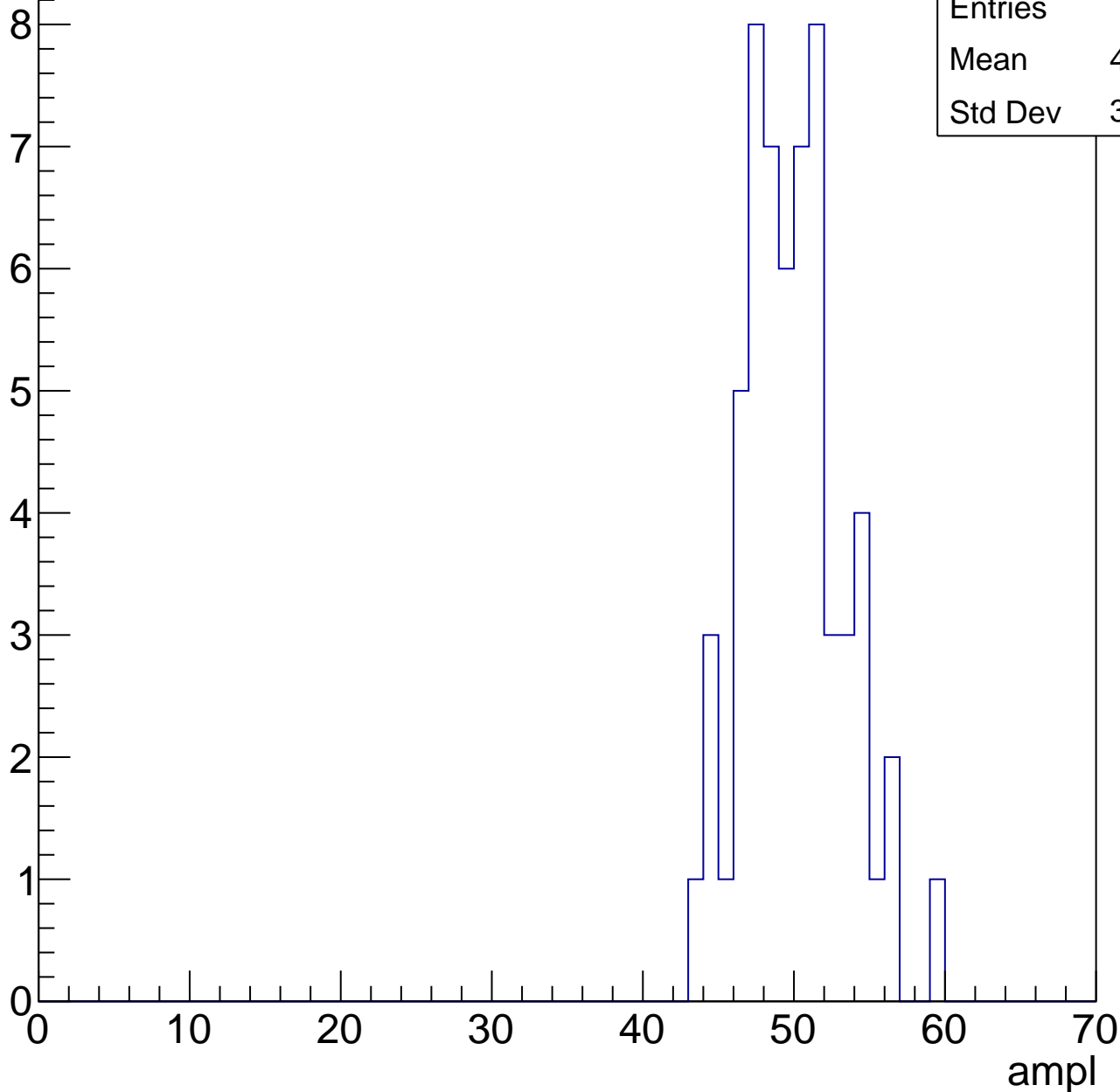


# B1L103S, U21-ch32, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	49.52
Std Dev	3.274

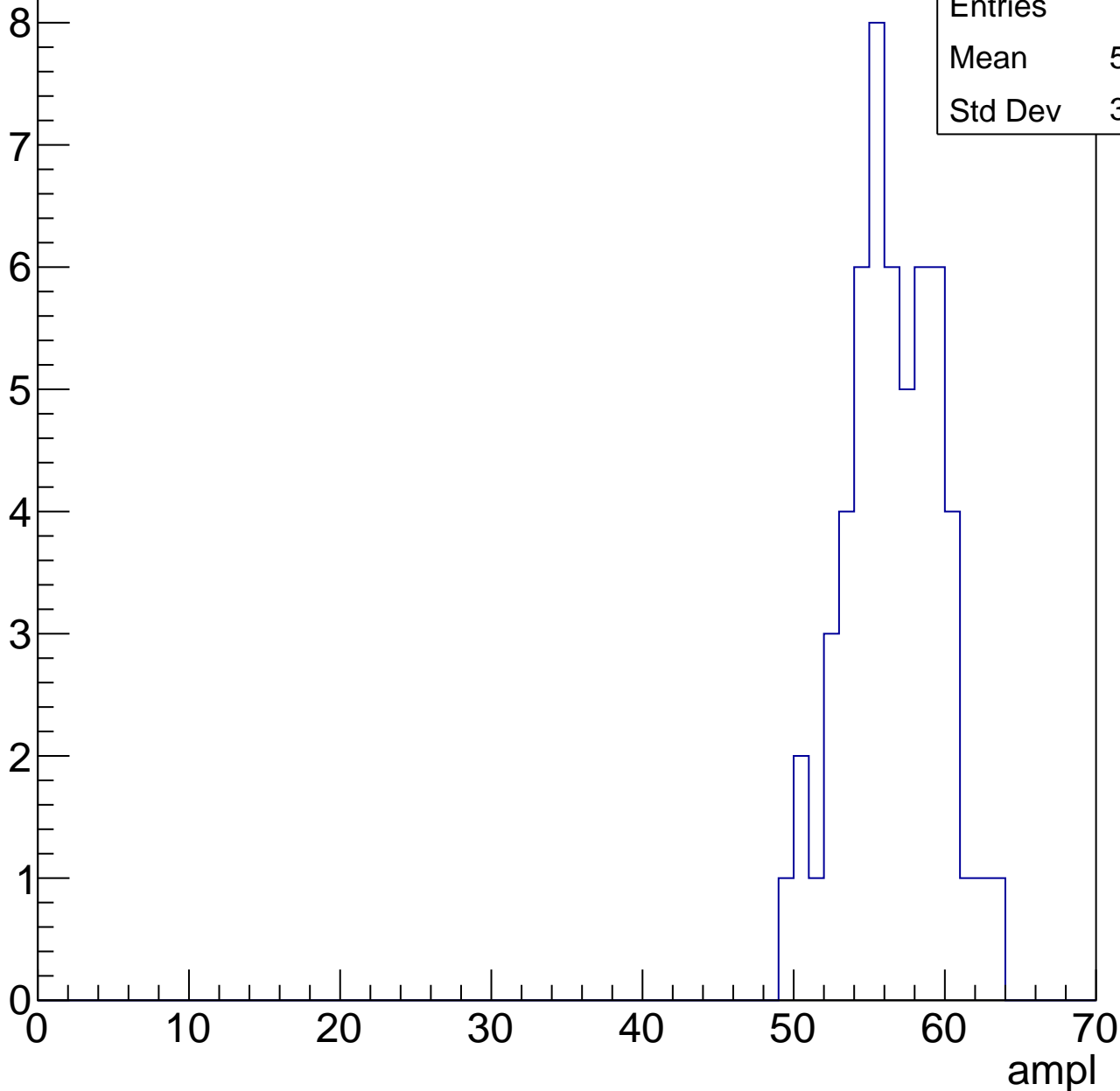


# B1L103S, U21-ch32, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	56.02
Std Dev	3.072



# B1L103S, U21-ch32, adc5

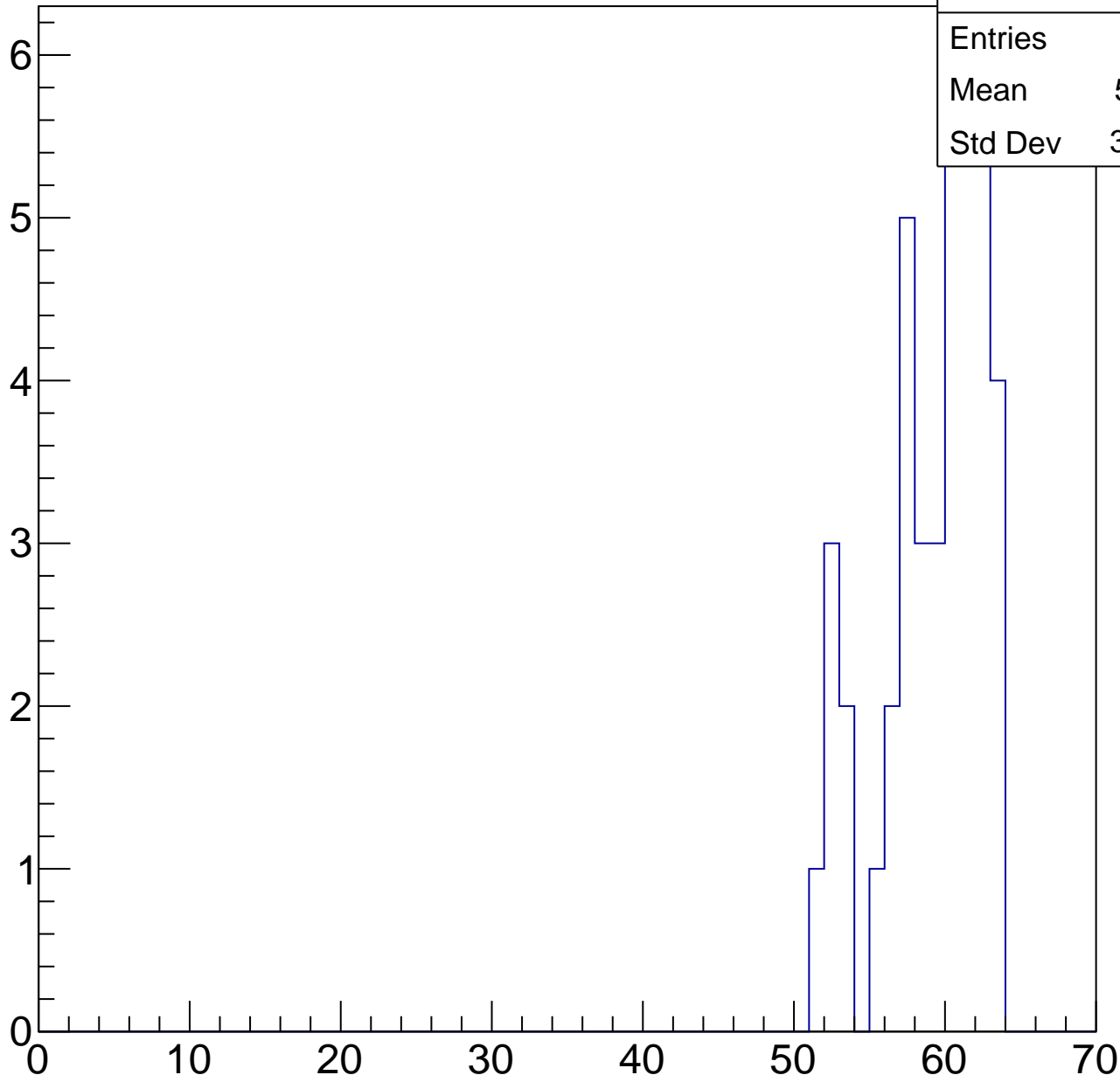
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

6  
5  
4  
3  
2  
1  
0

Entries	42
Mean	58.71
Std Dev	3.397

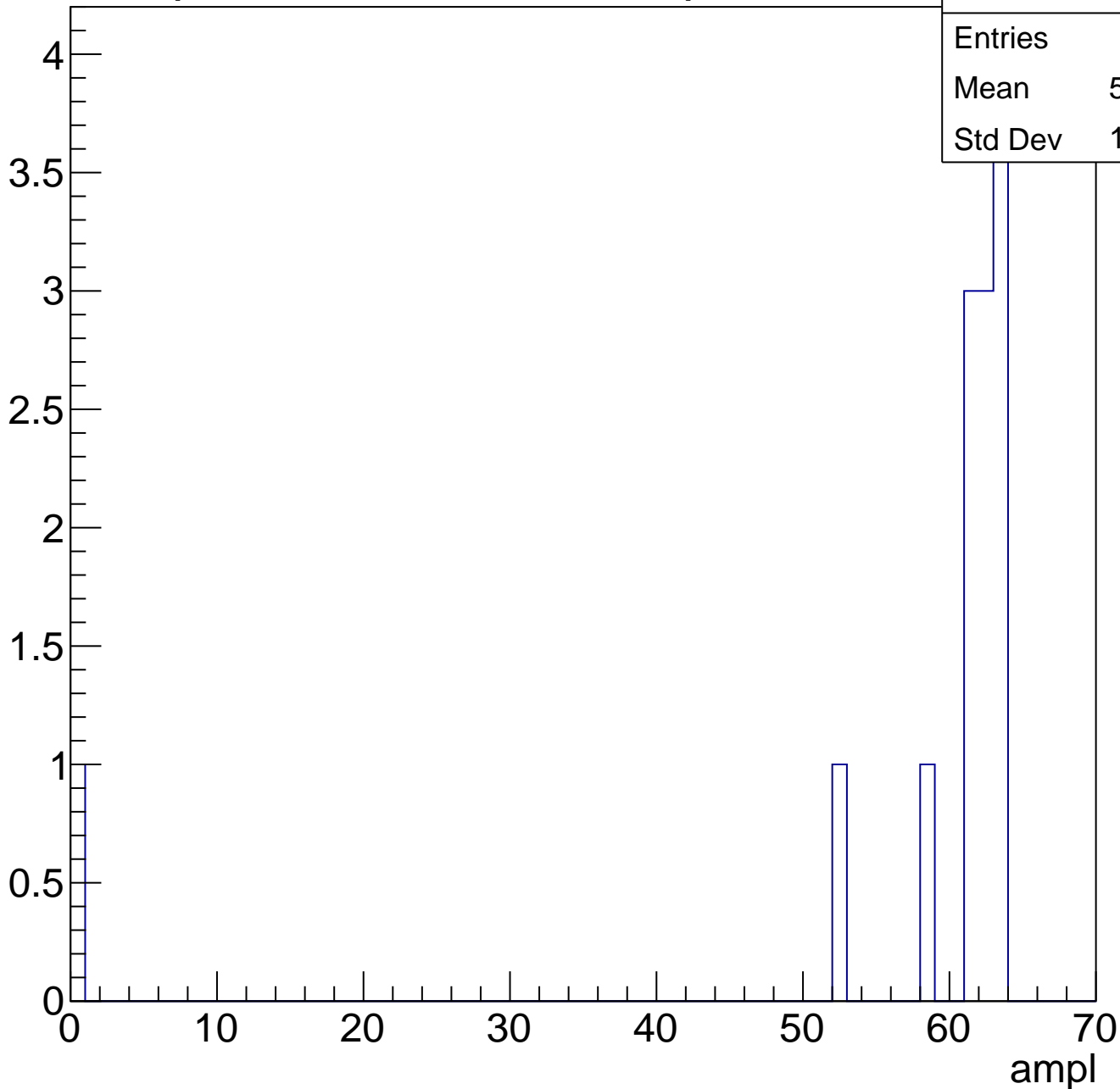
ampl



# B1L103S, U21-ch32, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U21-ch32, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U21-ch33, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	82
Mean	28.82
Std Dev	5.67

**Gaus mean : 30.4275**

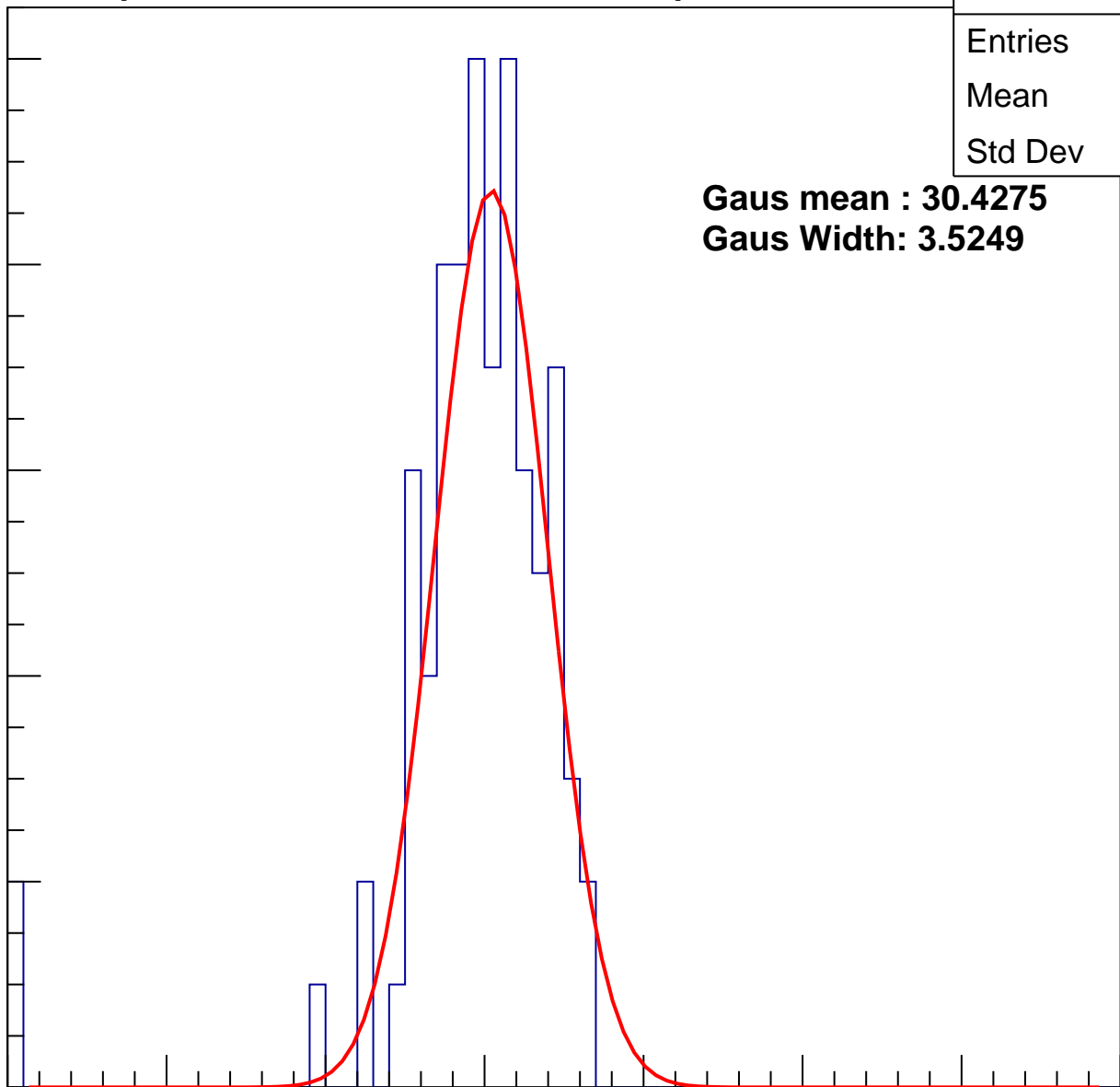
**Gaus Width: 3.5249**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U21-ch33, adc1

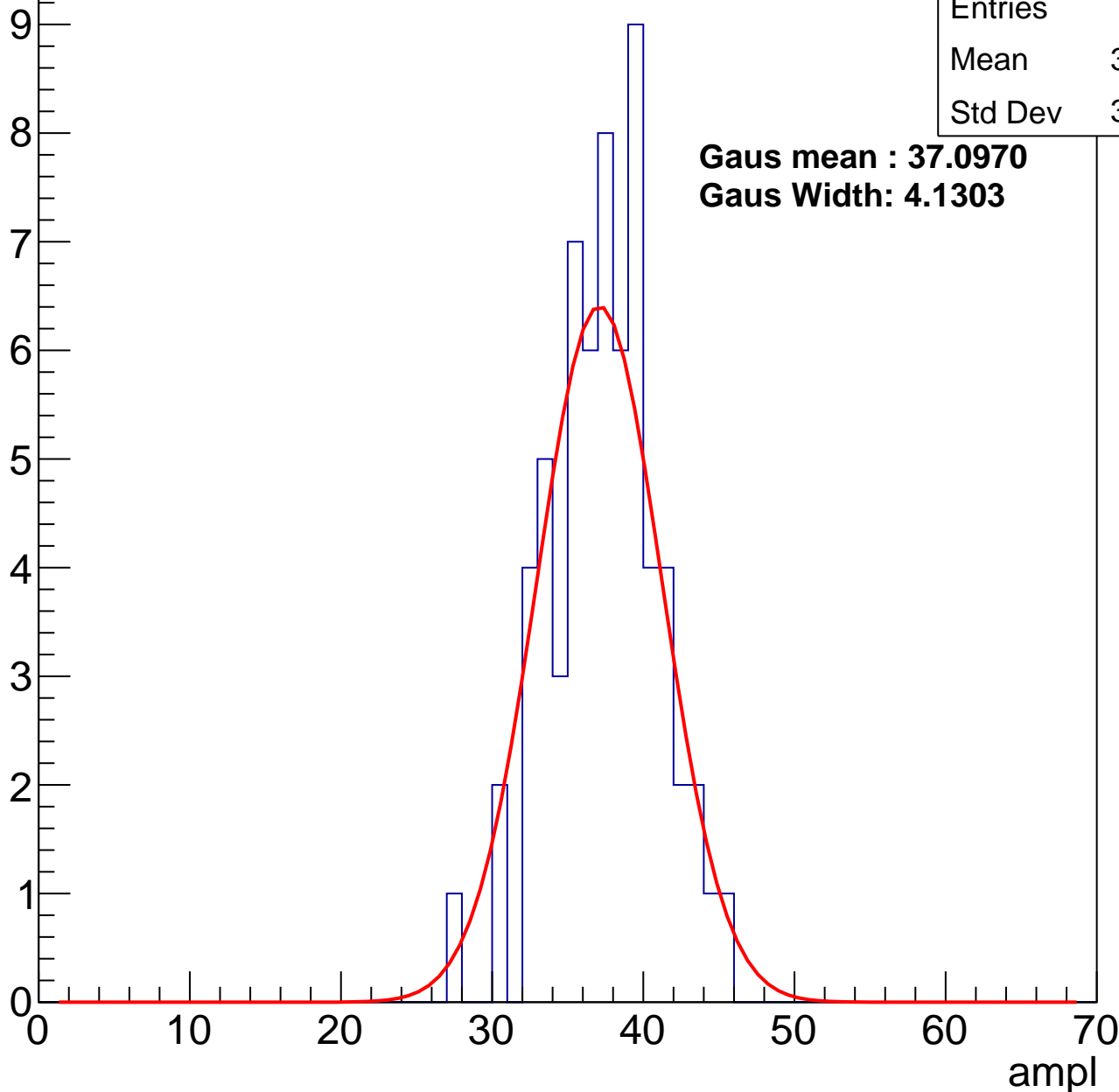
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	36.94
Std Dev	3.543

**Gaus mean : 37.0970**

**Gaus Width: 4.1303**



# B1L103S, U21-ch33, adc2

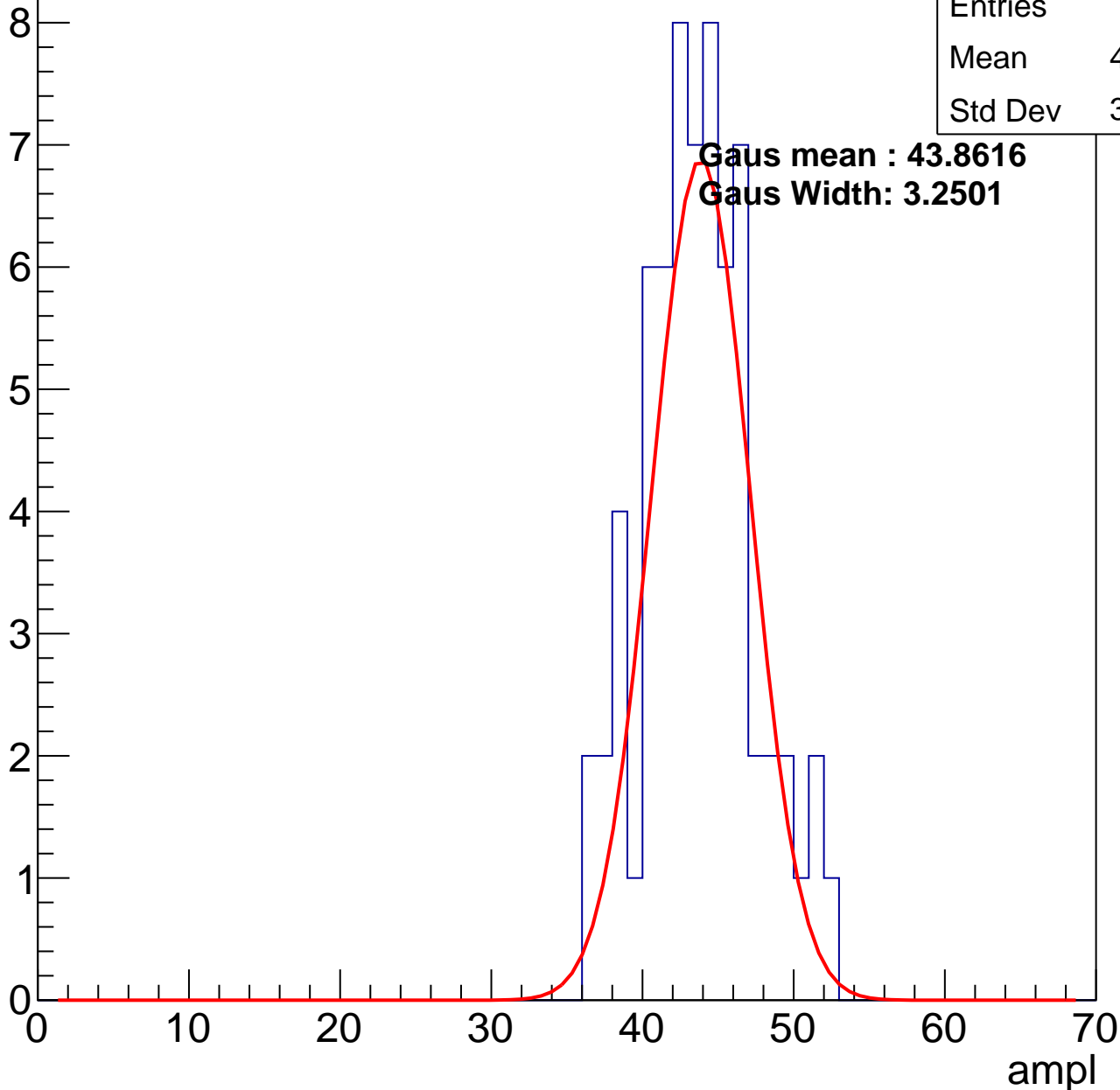
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	43.22
Std Dev	3.615

**Gaus mean : 43.8616**

**Gaus Width: 3.2501**

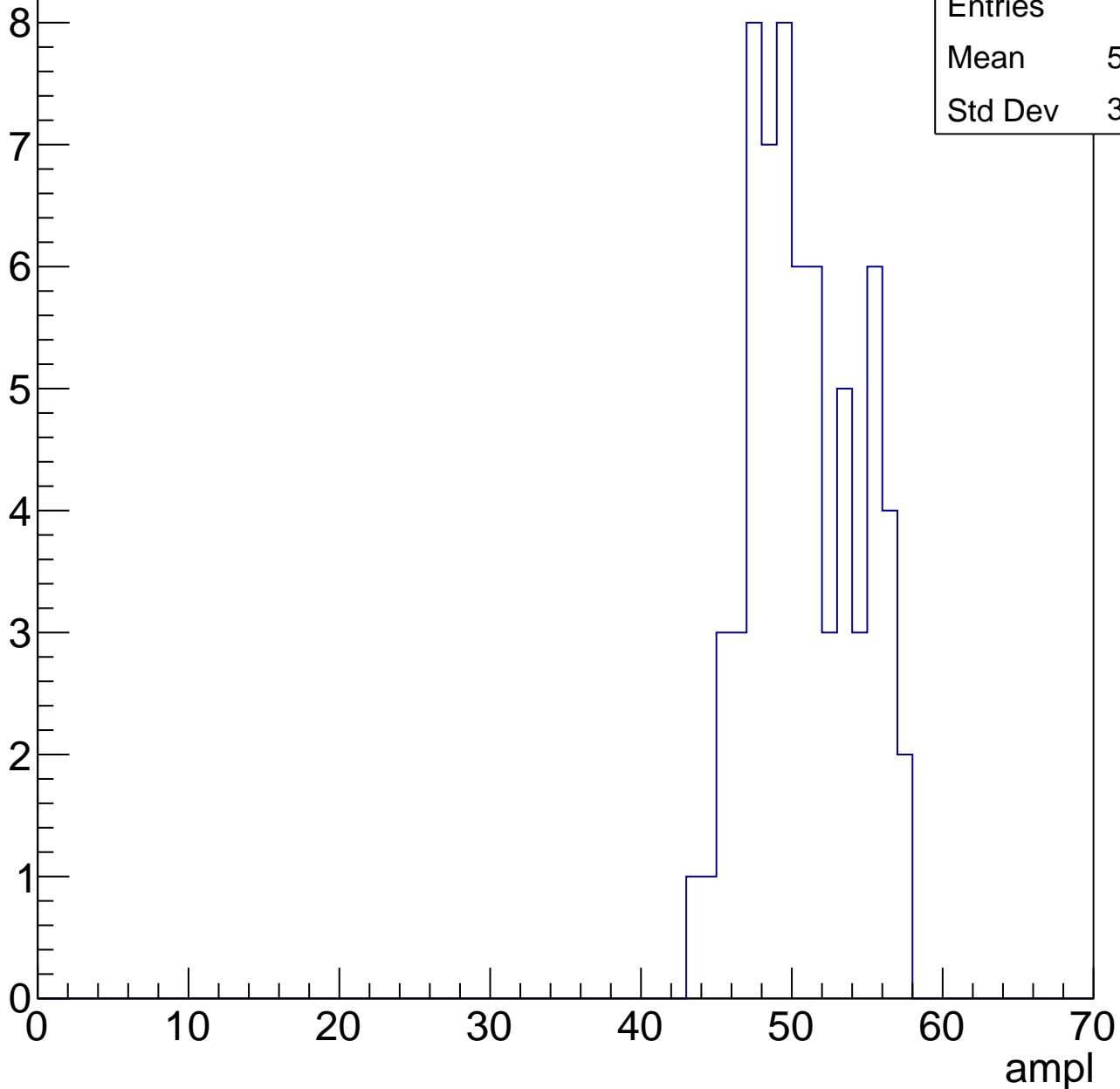


# B1L103S, U21-ch33, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	50.32
Std Dev	3.508

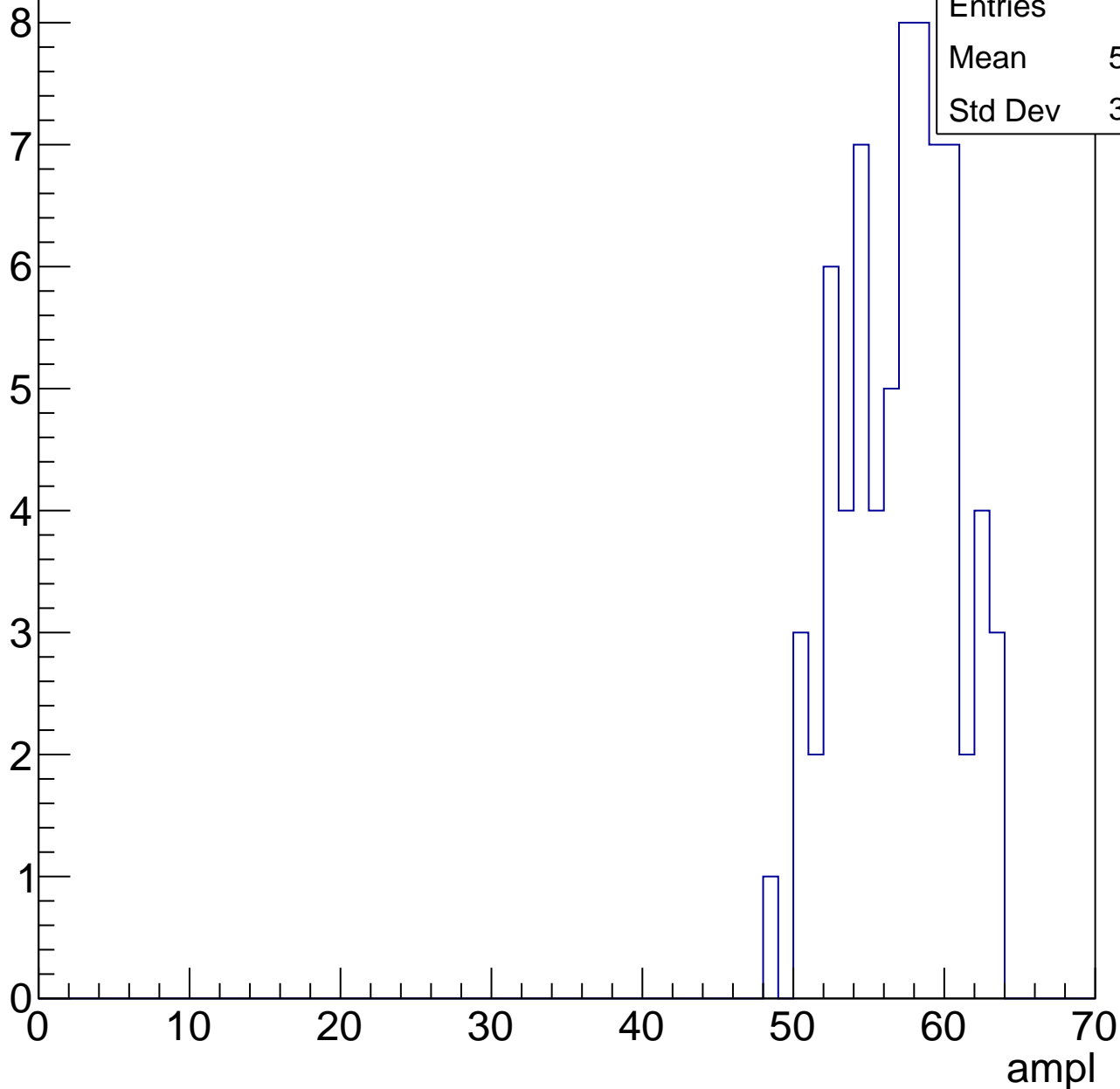


# B1L103S, U21-ch33, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	56.54
Std Dev	3.603

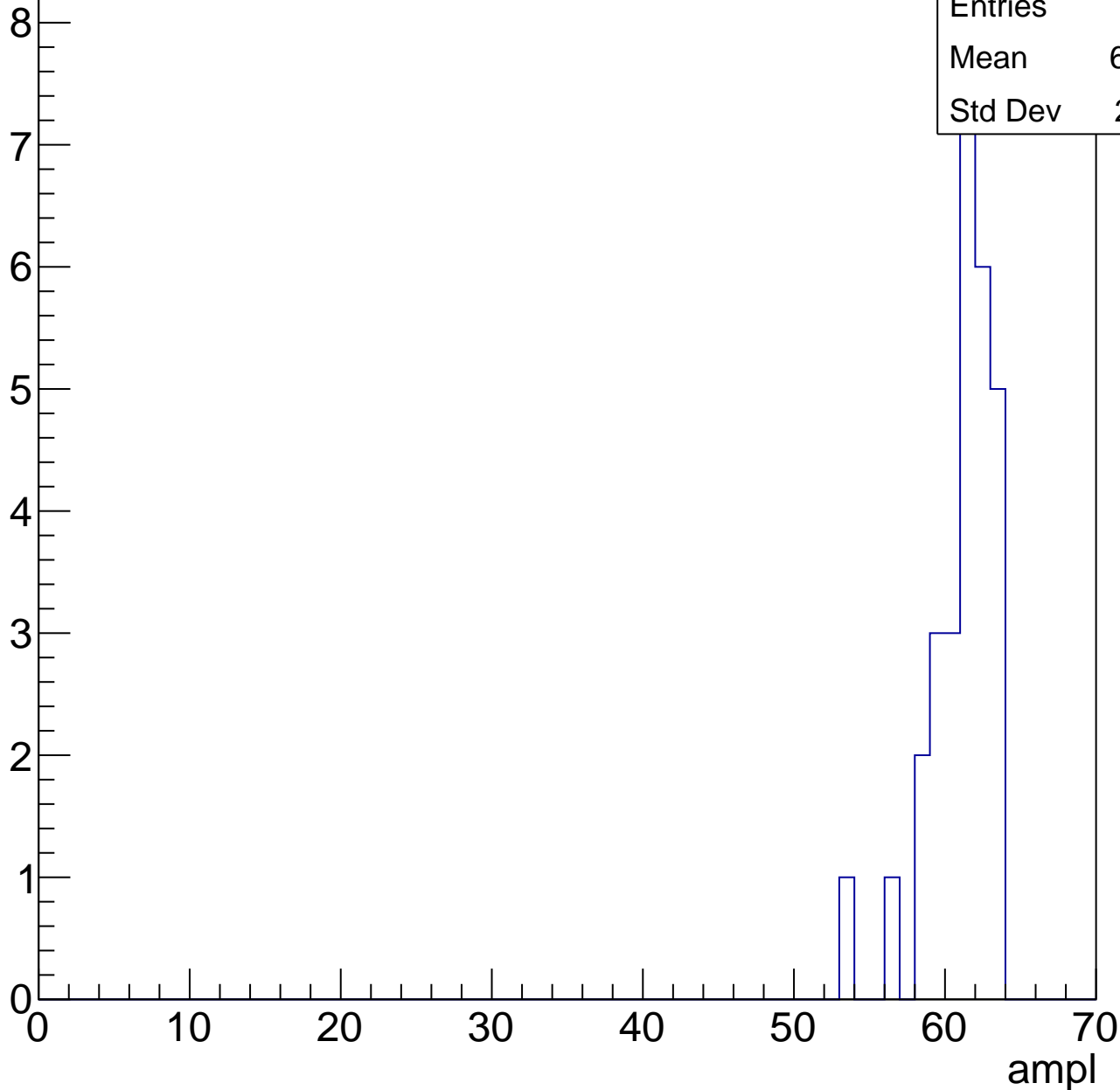


# B1L103S, U21-ch33, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	29
Mean	60.59
Std Dev	2.221



# B1L103S, U21-ch33, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U21-ch33, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U21-ch34, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	27.39
Std Dev	4.611

**Gaus mean : 28.0189**

**Gaus Width: 3.4198**

10

8

6

4

2

0

ampl

0

10

20

30

40

50

60

70

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70

# B1L103S, U21-ch34, adc1

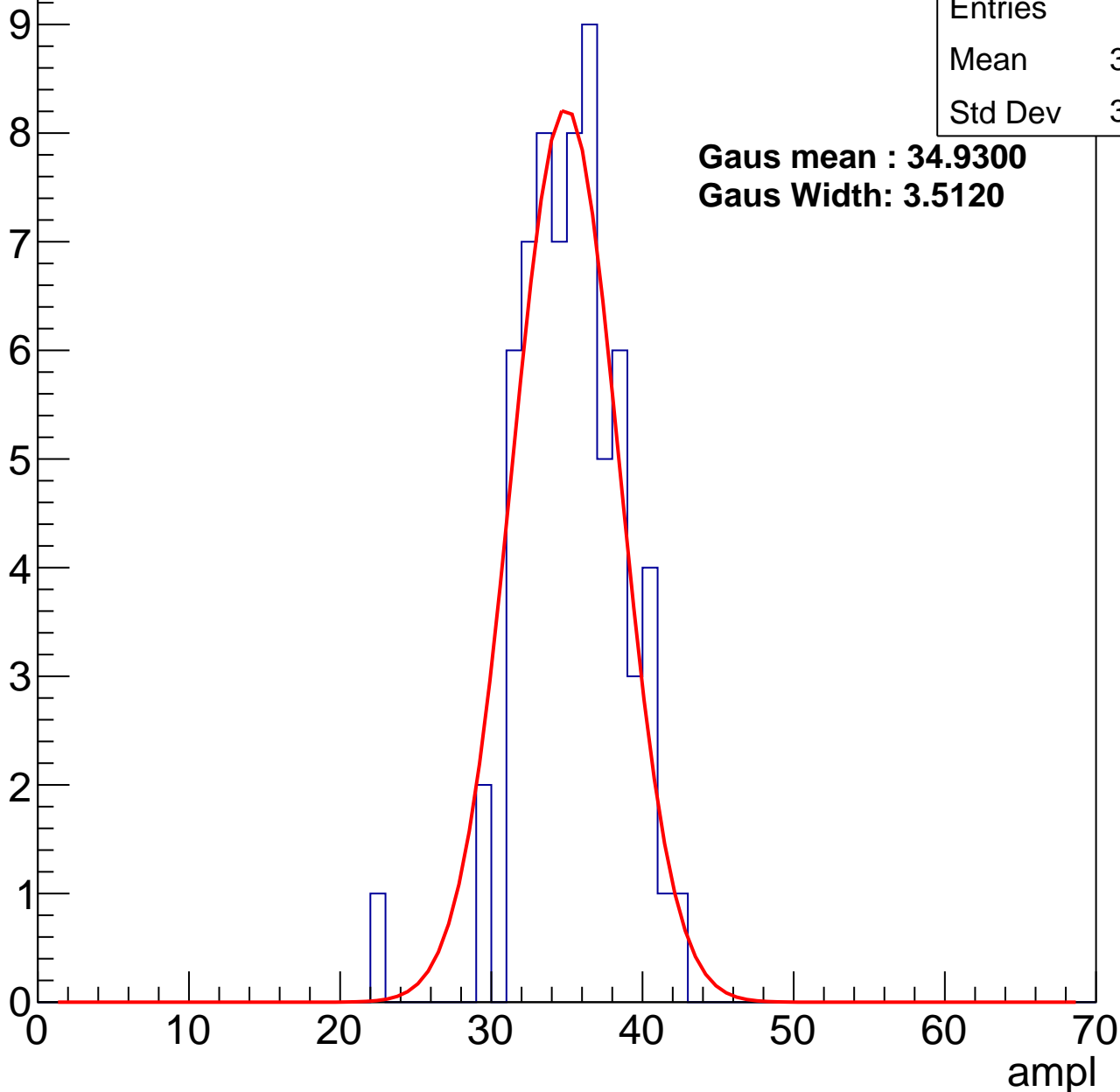
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	34.84
Std Dev	3.328

**Gaus mean : 34.9300**

**Gaus Width: 3.5120**



# B1L103S, U21-ch34, adc2

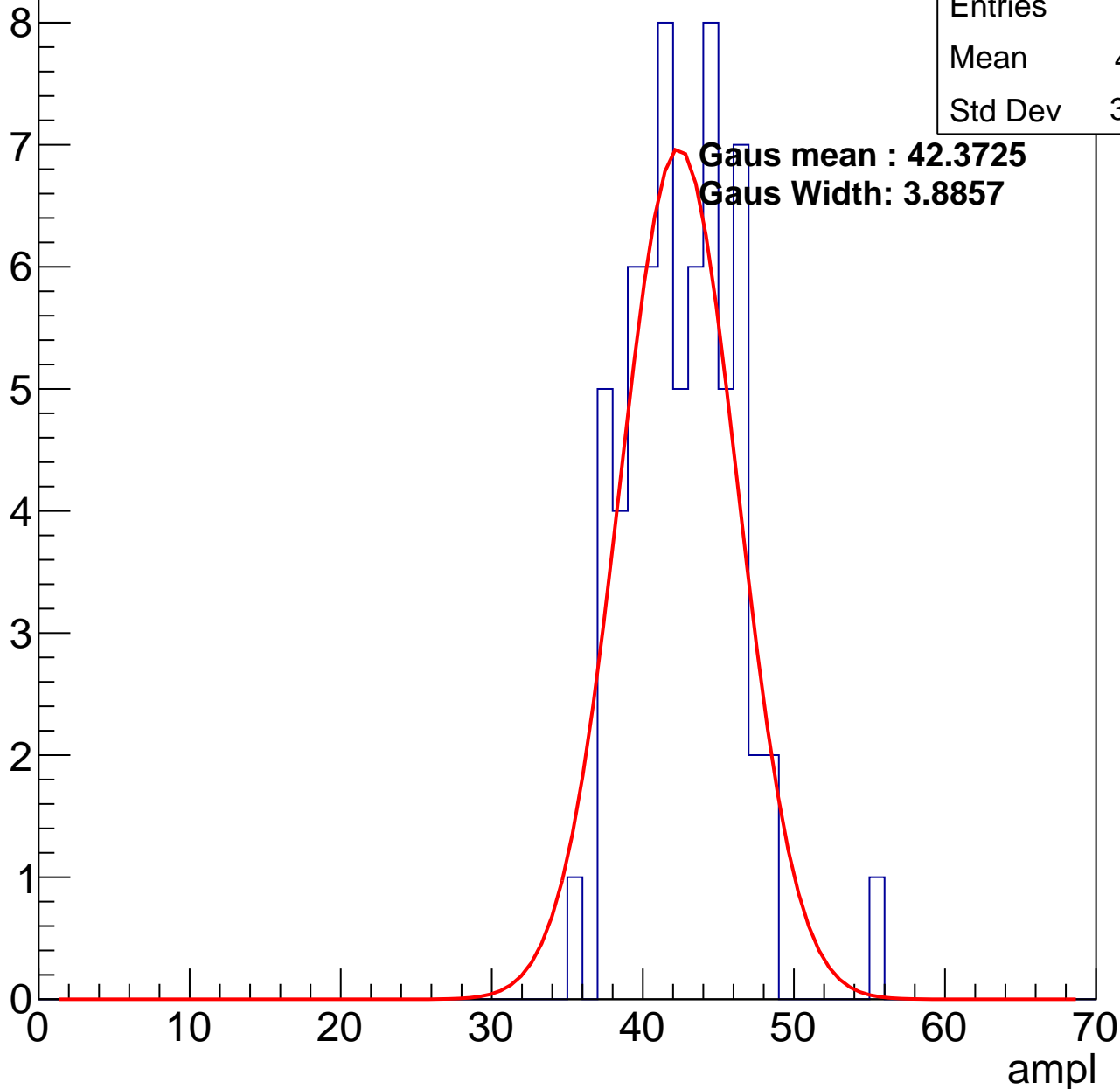
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	42.21
Std Dev	3.497

**Gaus mean : 42.3725**

**Gaus Width: 3.8857**

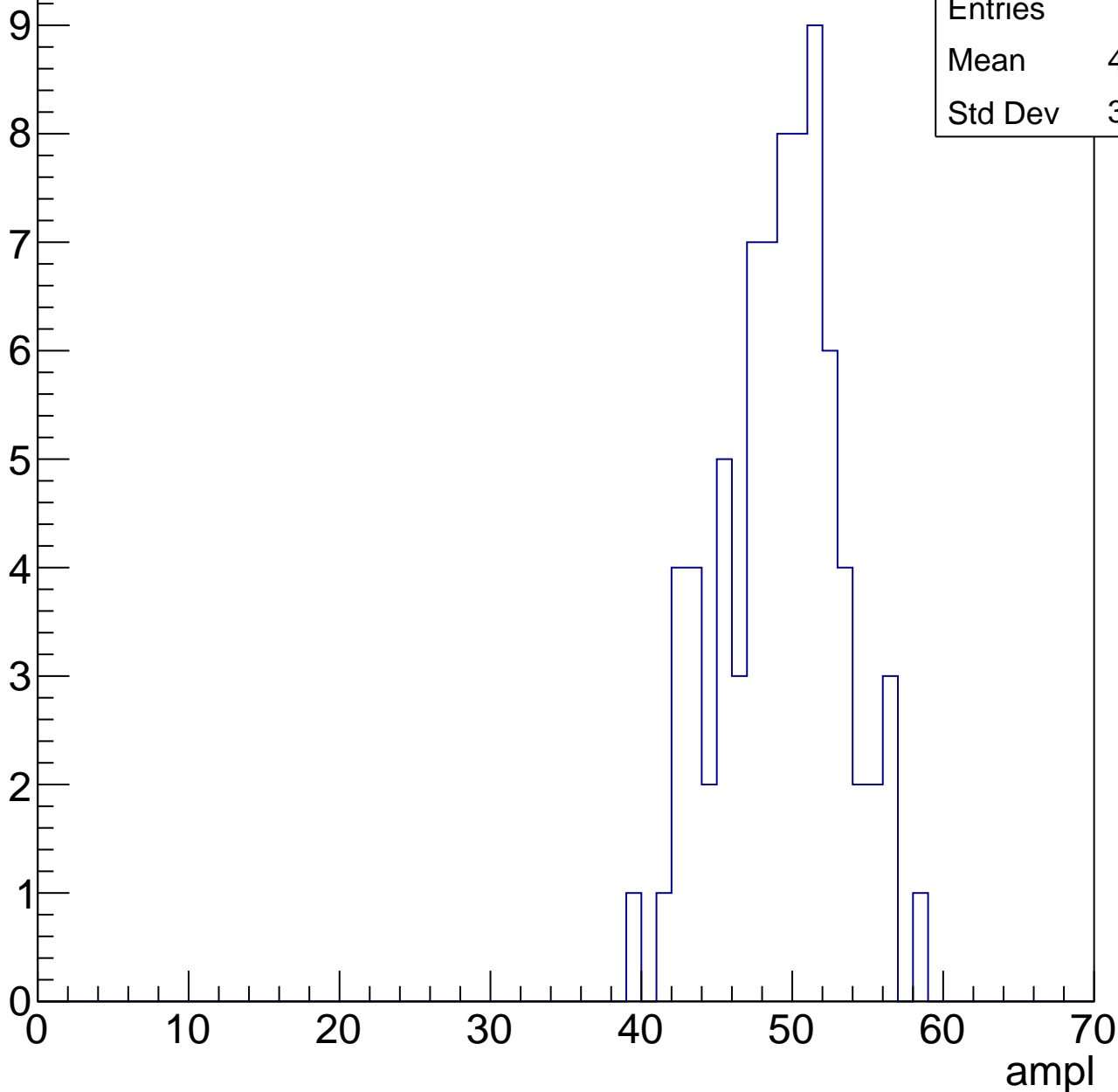


# B1L103S, U21-ch34, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	48.77
Std Dev	3.954



# B1L103S, U21-ch34, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

7

6

5

4

3

2

1

0

Entries	59
Mean	55.61
Std Dev	3.622

ampl

0

10

20

30

40

50

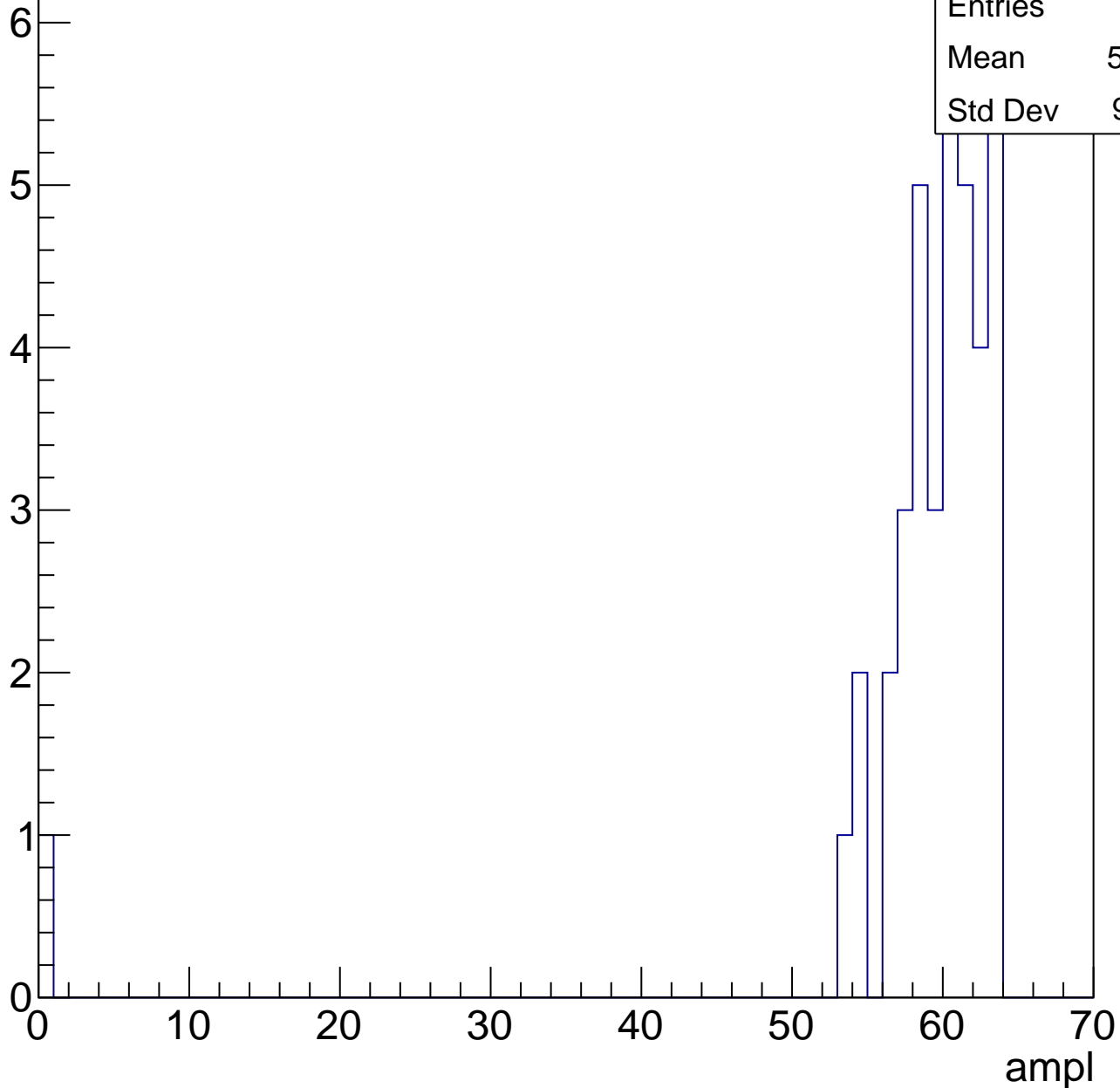
60

70

# B1L103S, U21-ch34, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

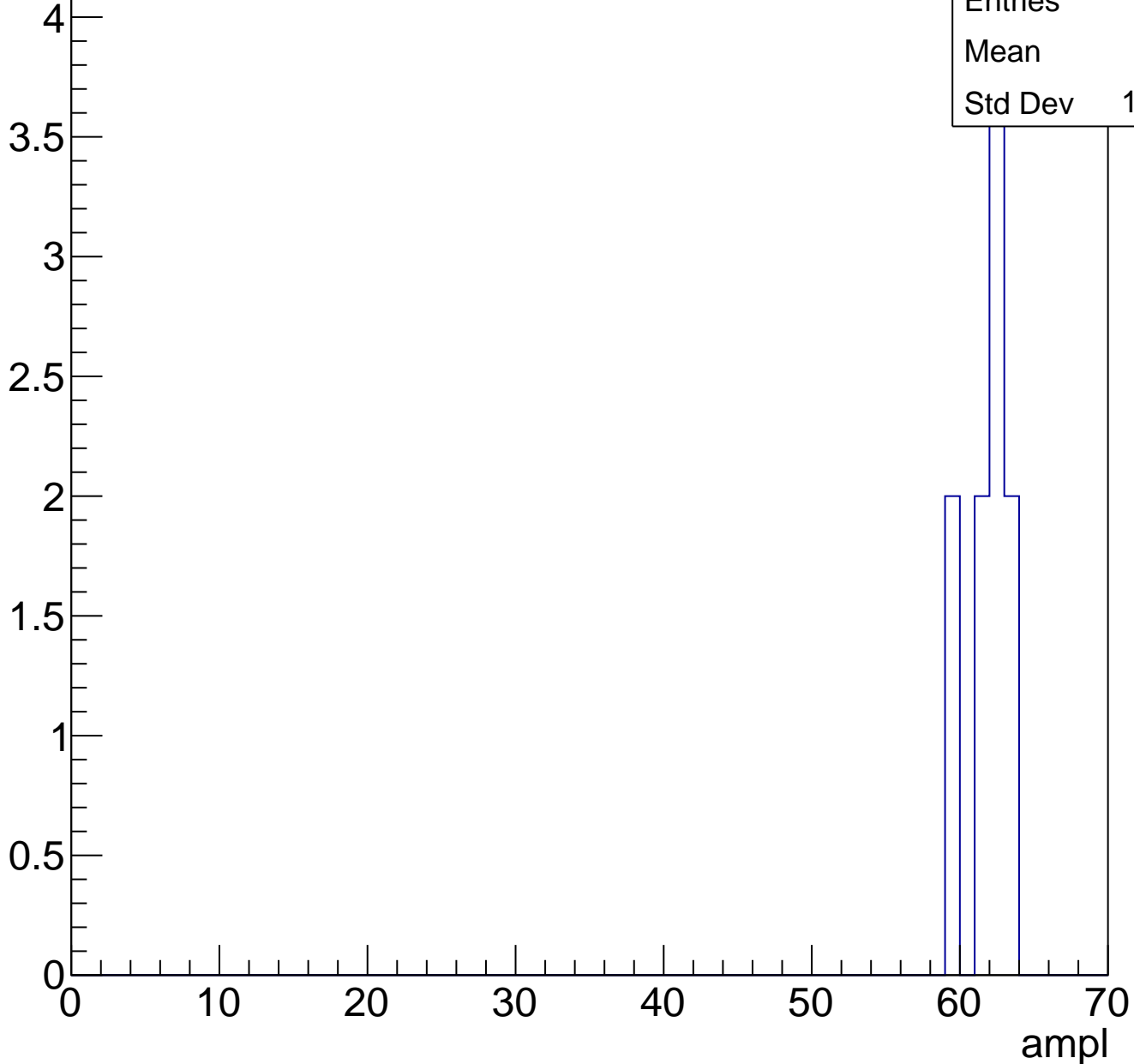
Entry



# B1L103S, U21-ch34, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

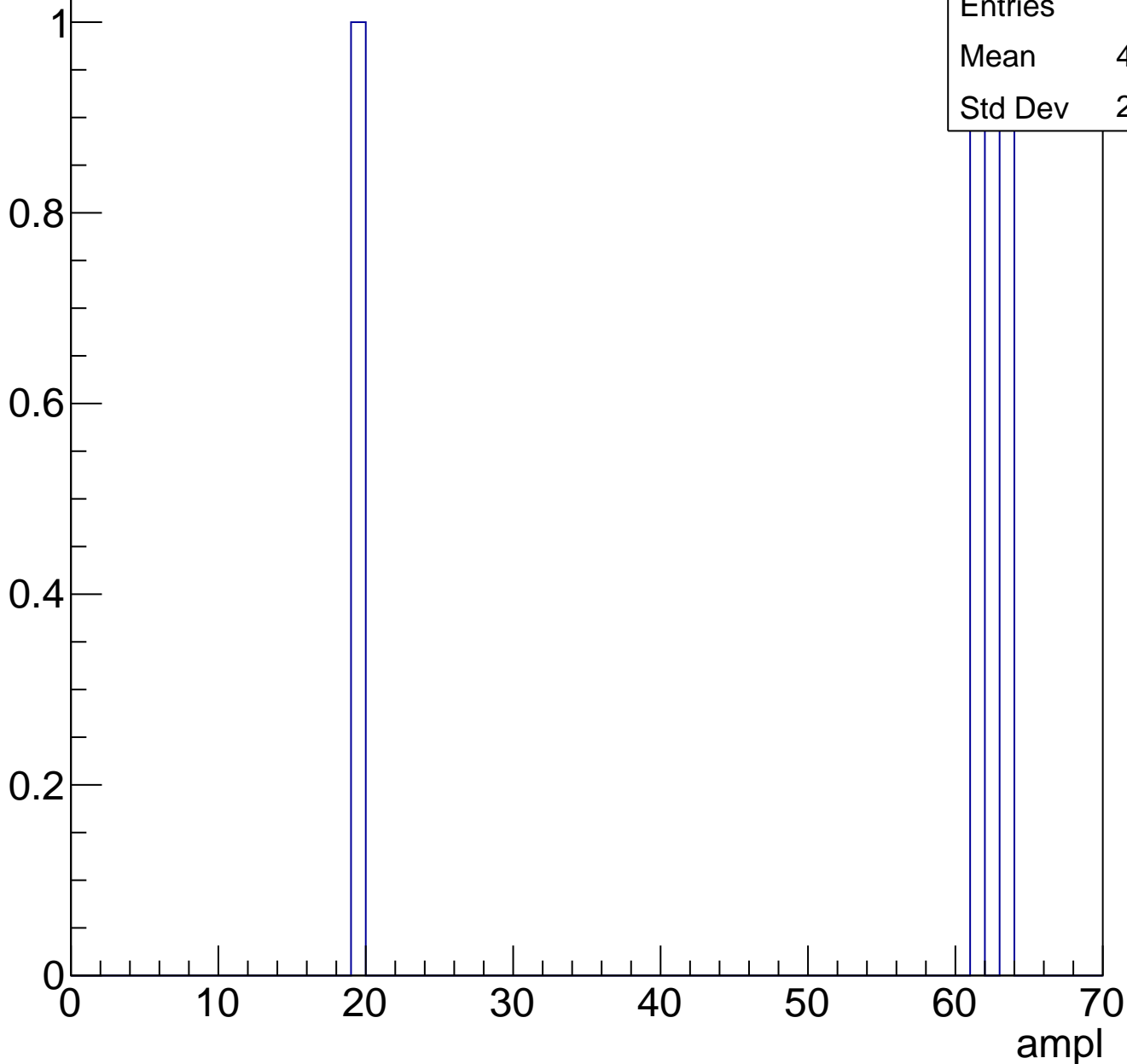




# B1L103S, U21-ch34, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U21-ch35, adc0

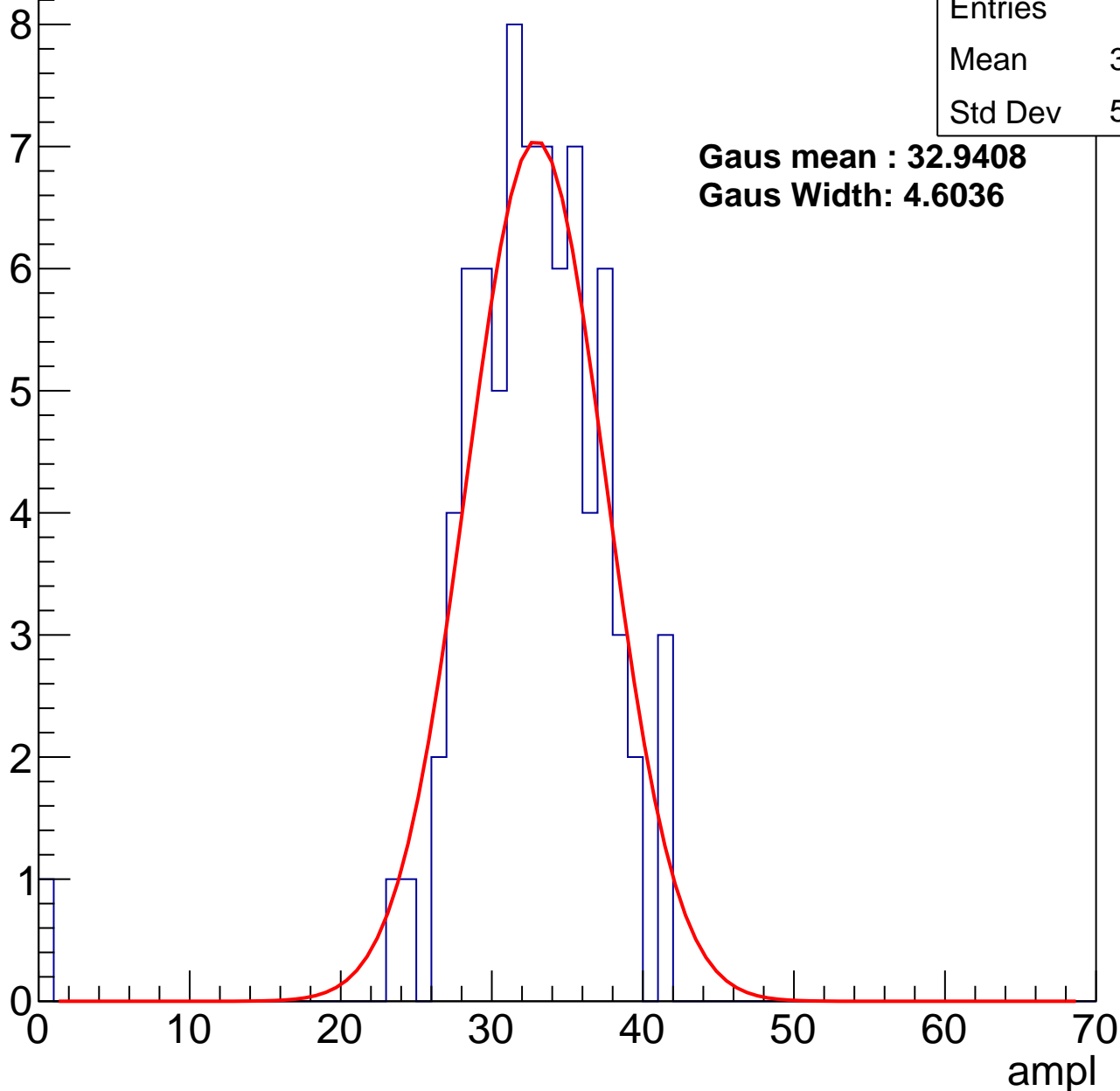
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	79
Mean	32.05
Std Dev	5.367

**Gaus mean : 32.9408**

**Gaus Width: 4.6036**



# B1L103S, U21-ch35, adc1

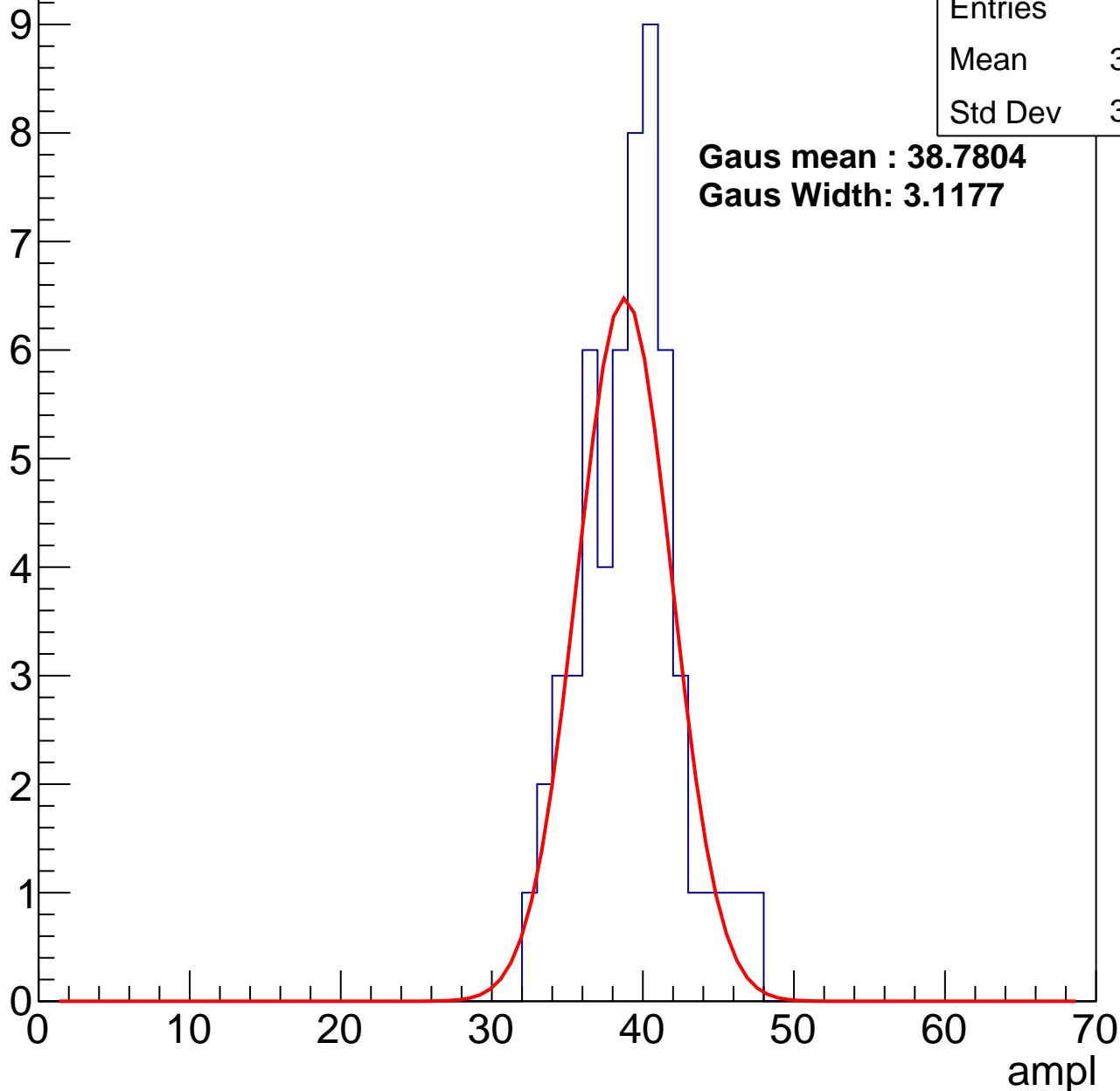
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	38.68
Std Dev	3.174

**Gaus mean : 38.7804**

**Gaus Width: 3.1177**



# B1L103S, U21-ch35, adc2

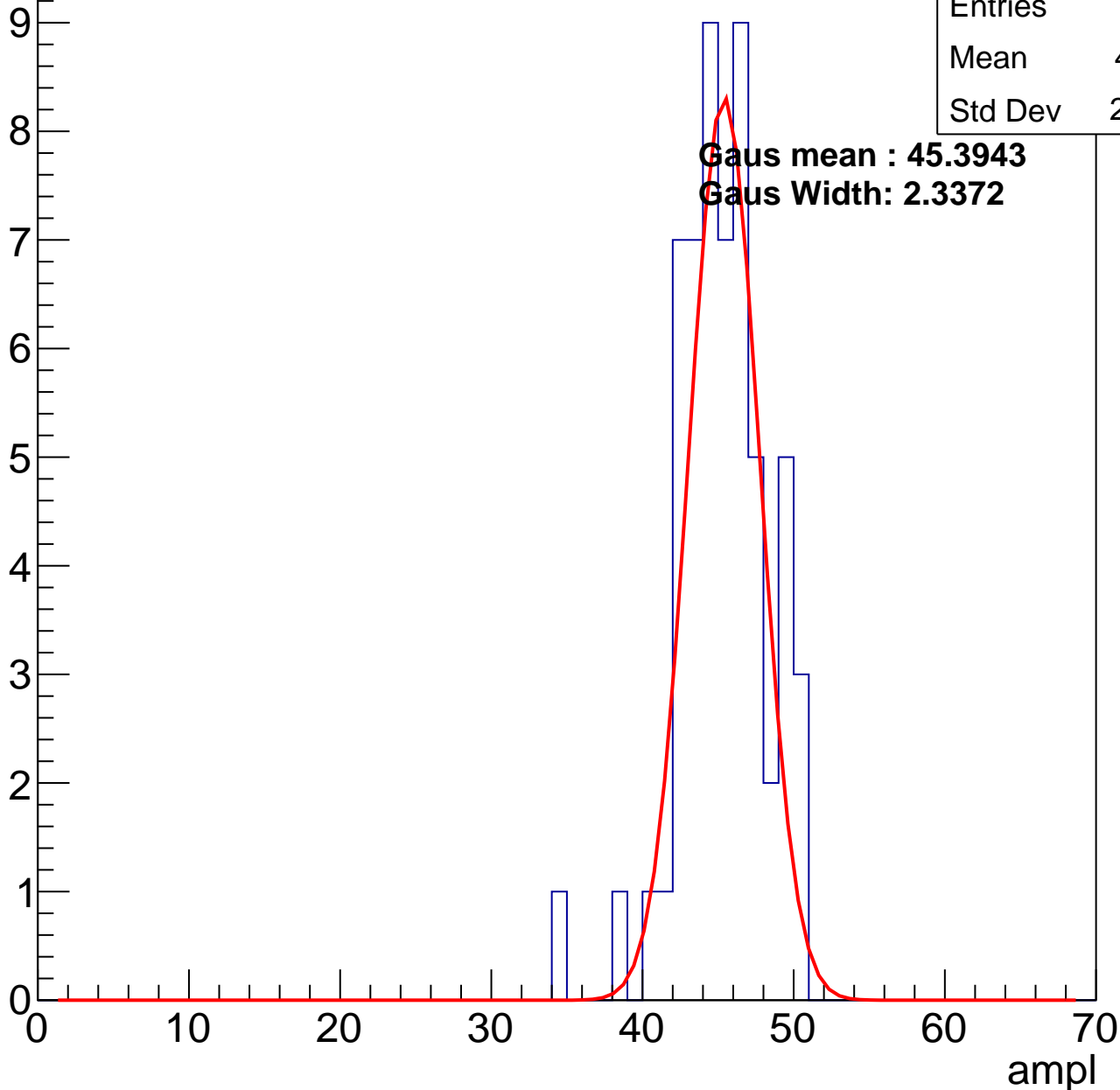
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	44.81
Std Dev	2.968

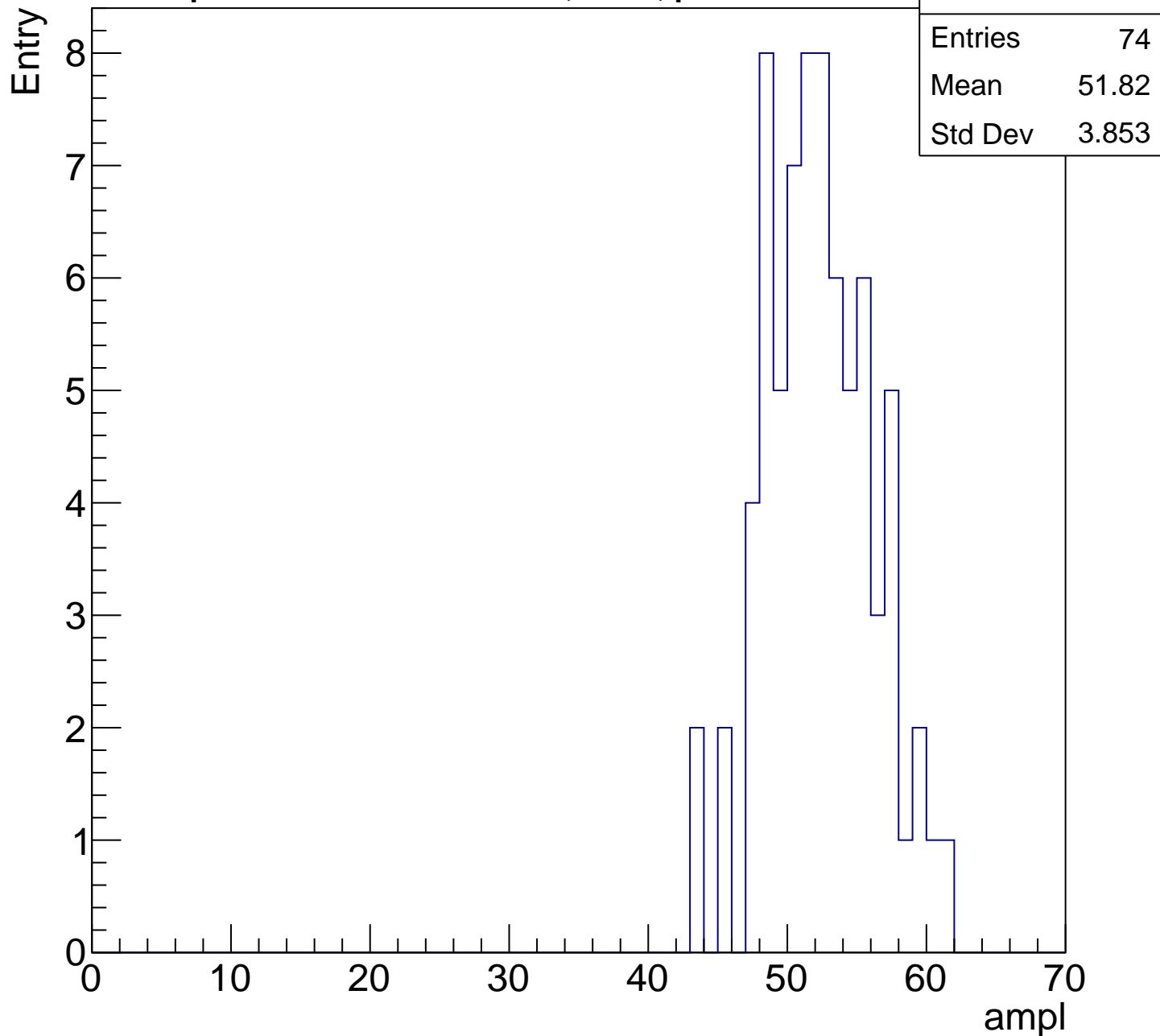
**Gaus mean : 45.3943**

**Gaus Width: 2.3372**



# B1L103S, U21-ch35, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

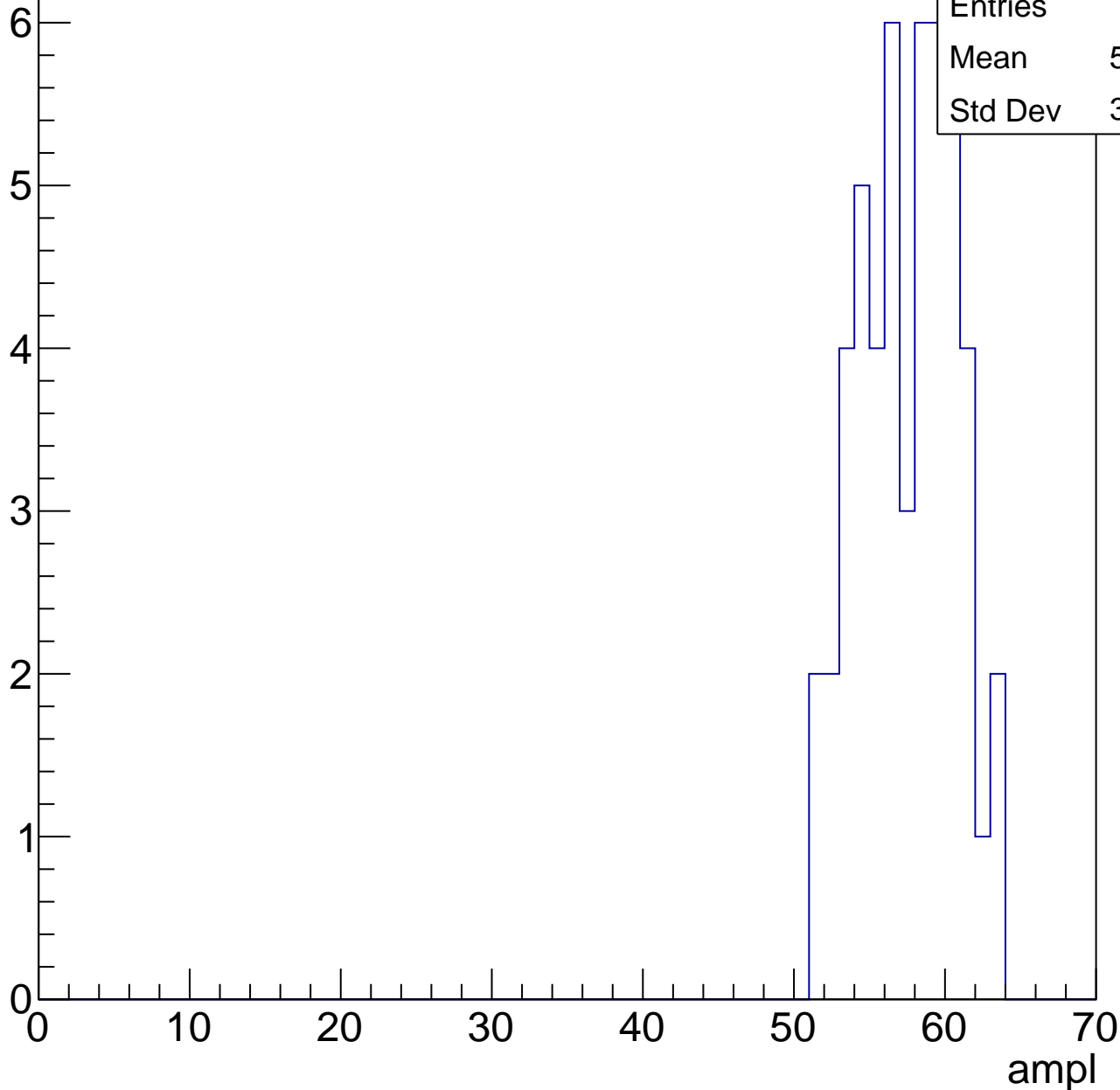


# B1L103S, U21-ch35, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	57.04
Std Dev	3.125

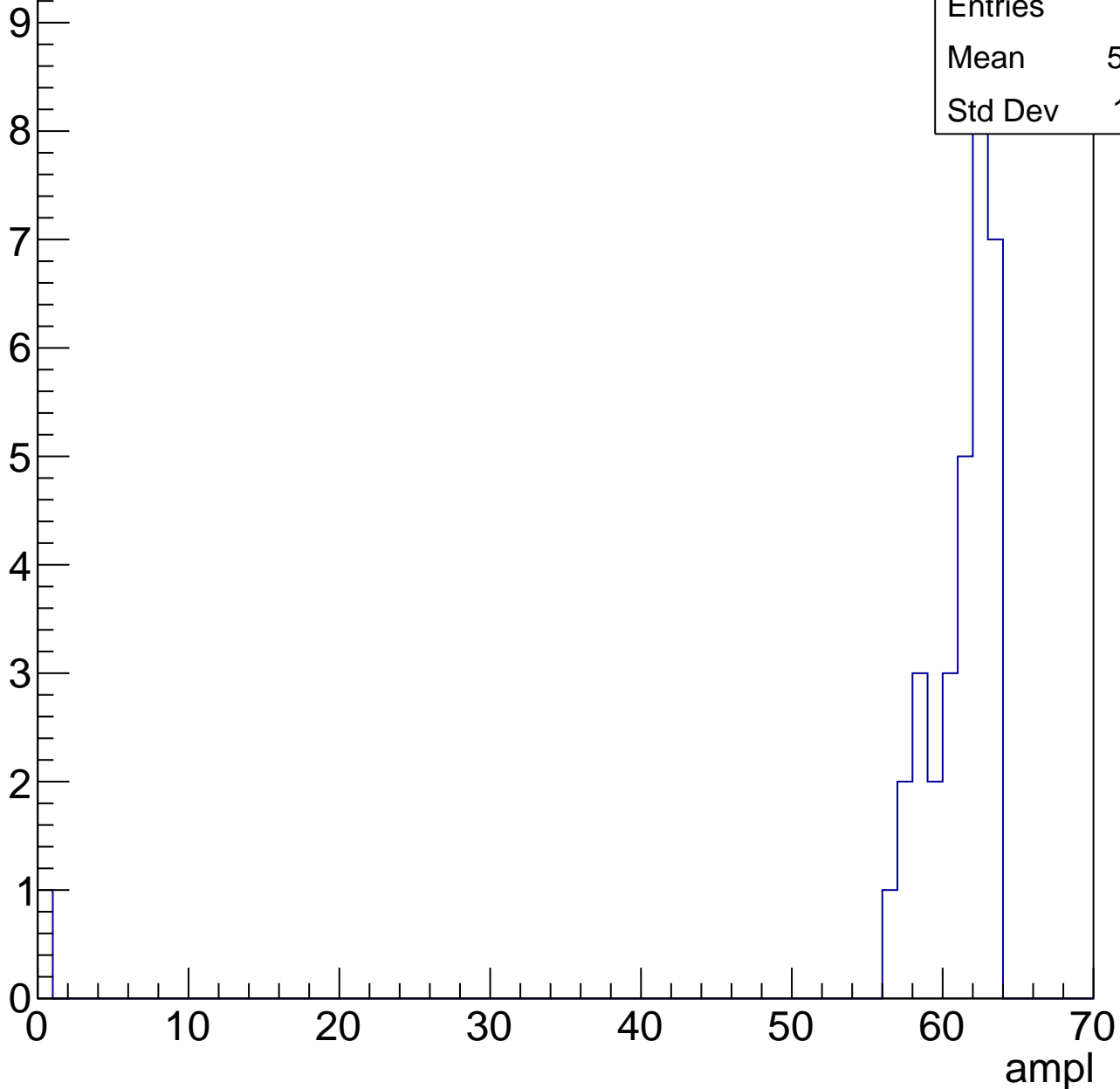


# B1L103S, U21-ch35, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	33
Mean	58.97
Std Dev	10.61



# B1L103S, U21-ch35, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U21-ch35, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U21-ch36, adc0

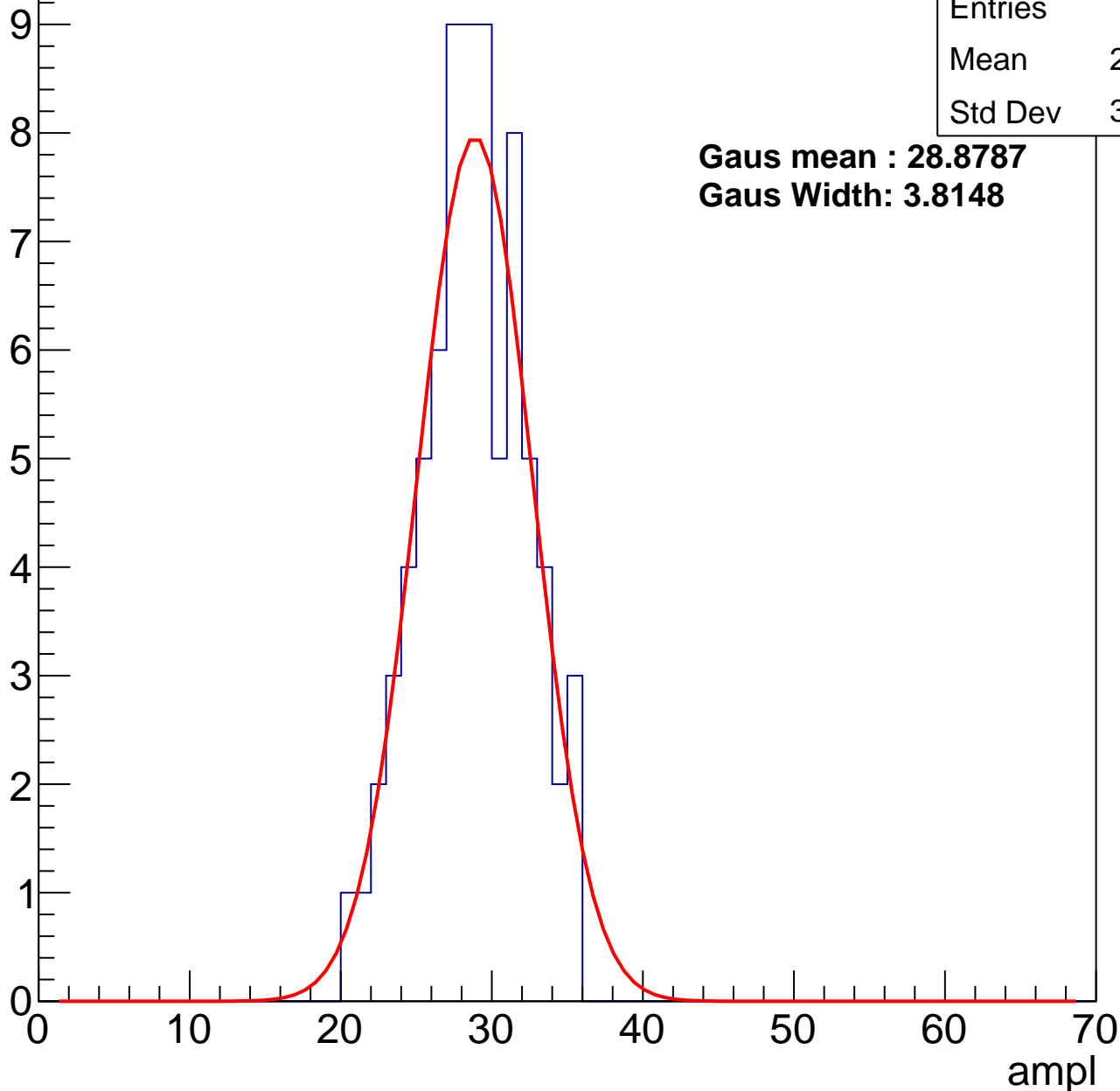
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	28.29
Std Dev	3.433

**Gaus mean : 28.8787**

**Gaus Width: 3.8148**



# B1L103S, U21-ch36, adc1

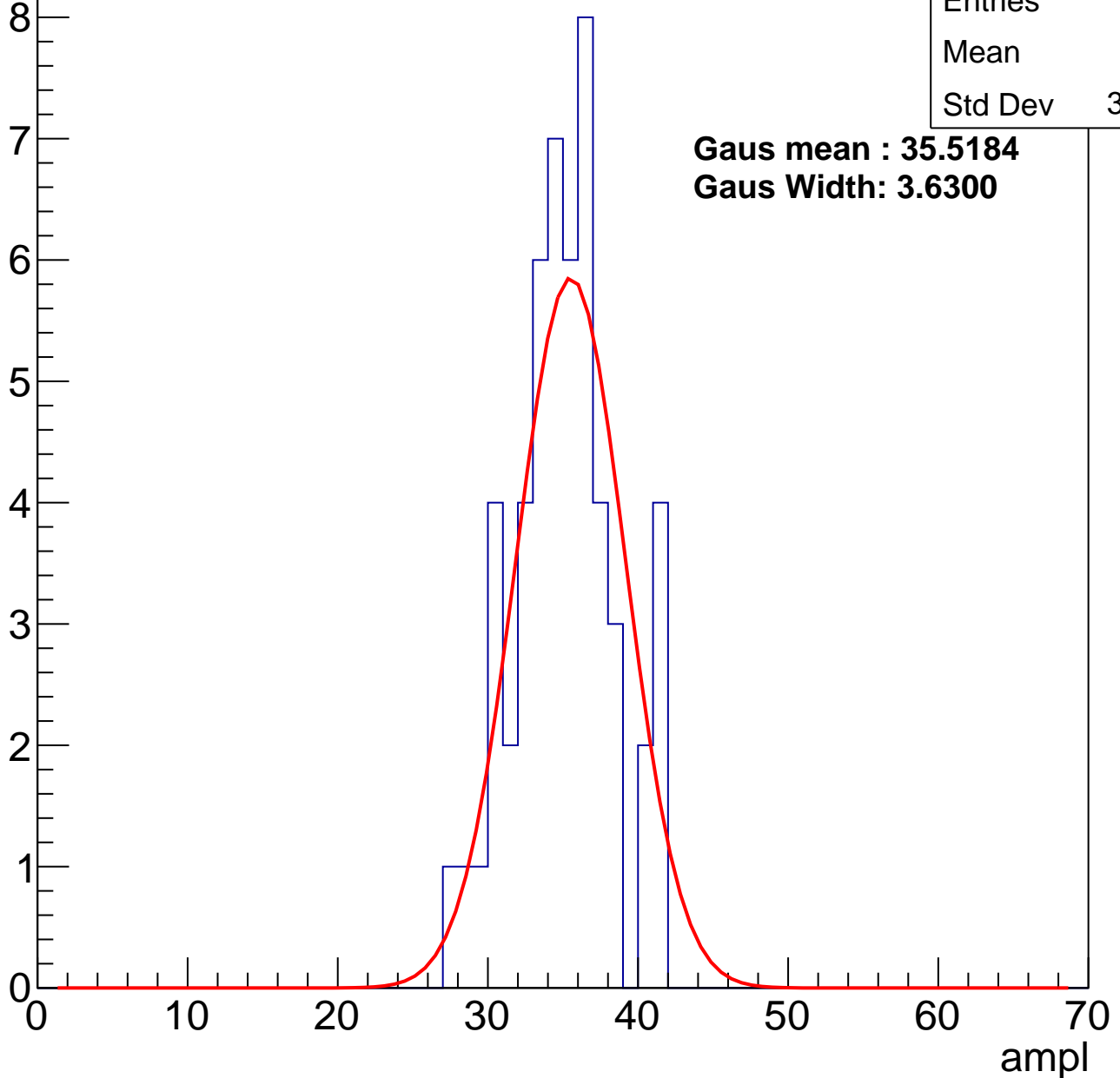
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	34.6
Std Dev	3.321

**Gaus mean : 35.5184**

**Gaus Width: 3.6300**



# B1L103S, U21-ch36, adc2

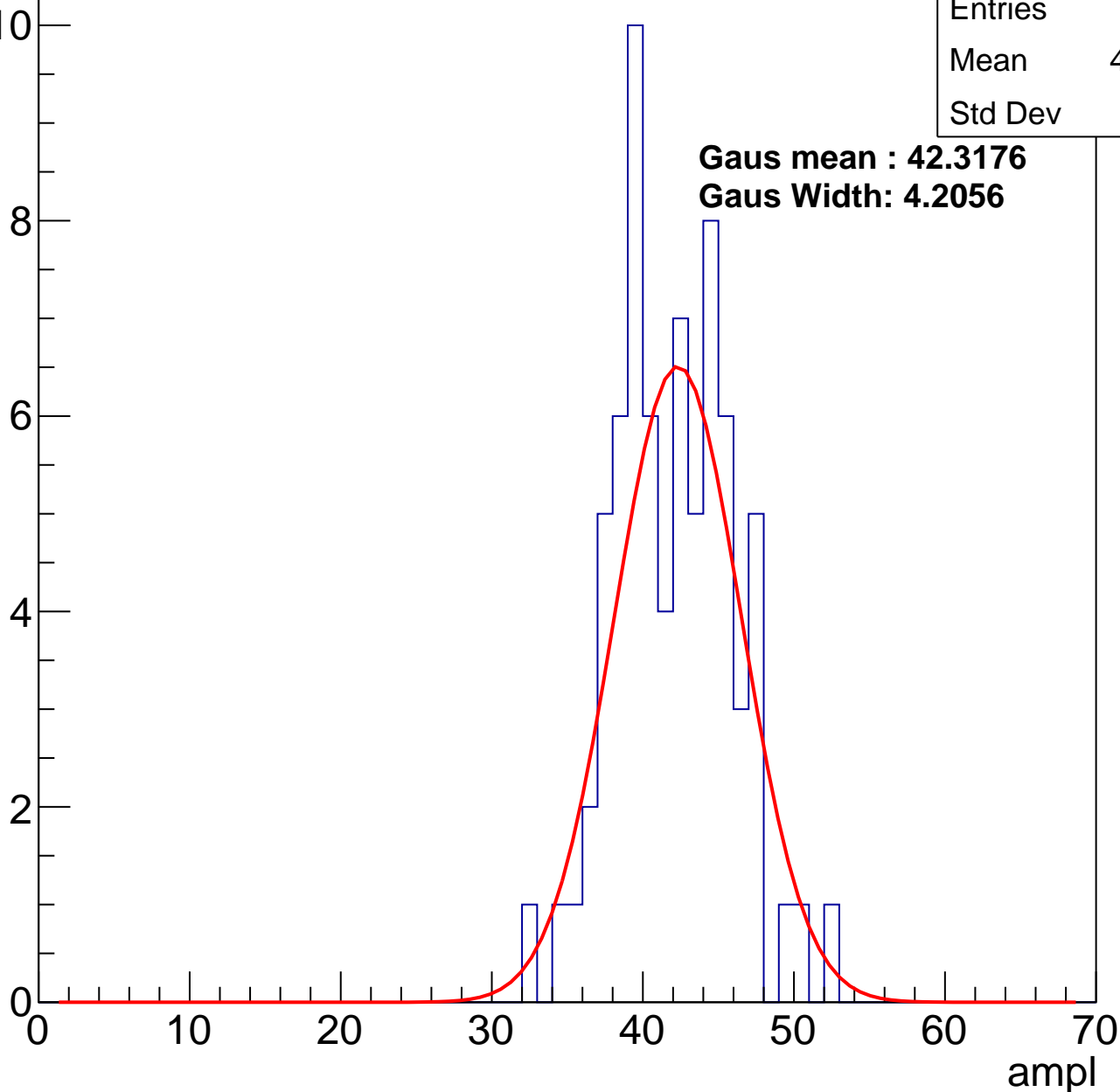
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	41.58
Std Dev	3.86

**Gaus mean : 42.3176**

**Gaus Width: 4.2056**

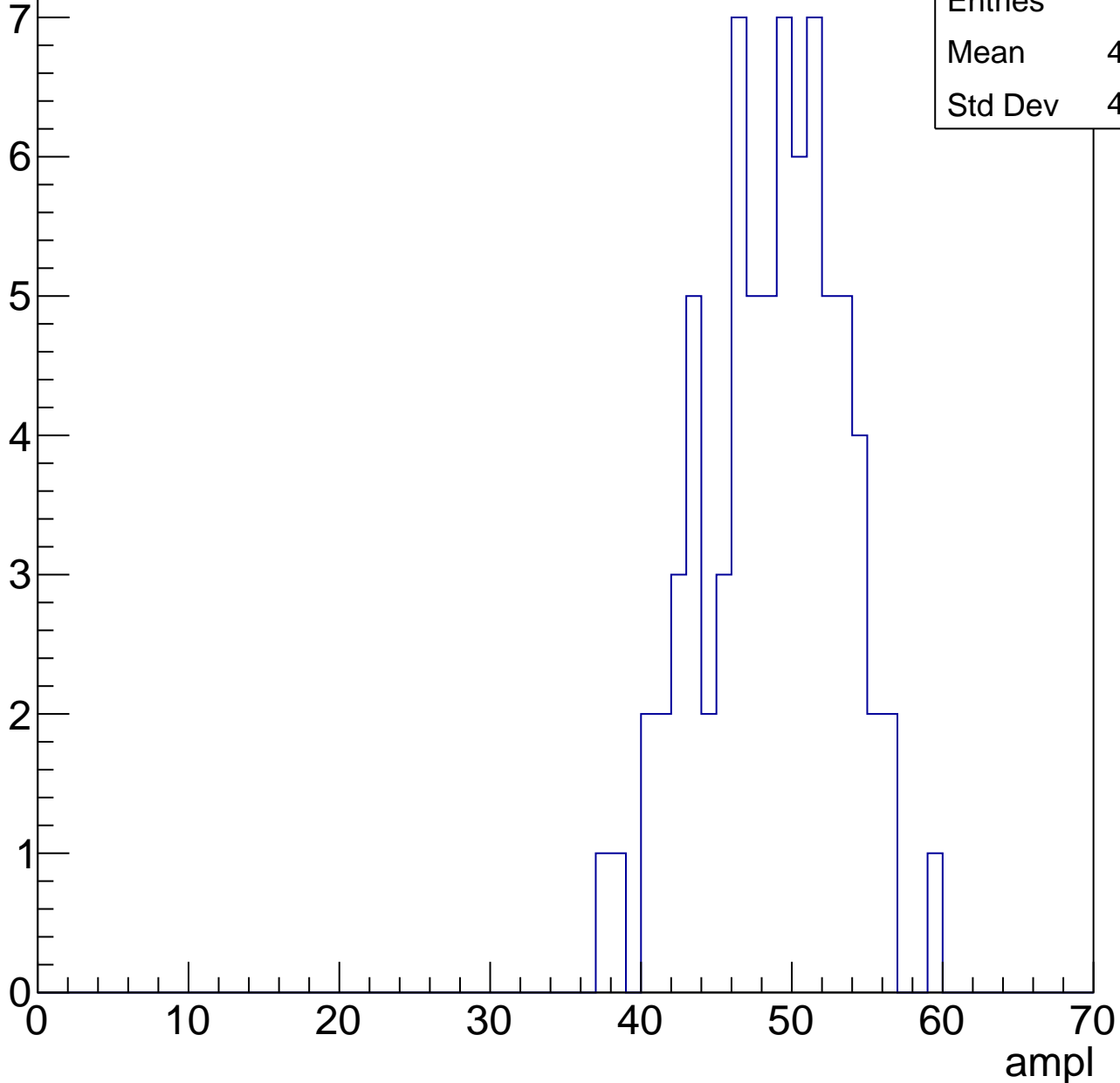


# B1L103S, U21-ch36, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	48.27
Std Dev	4.556

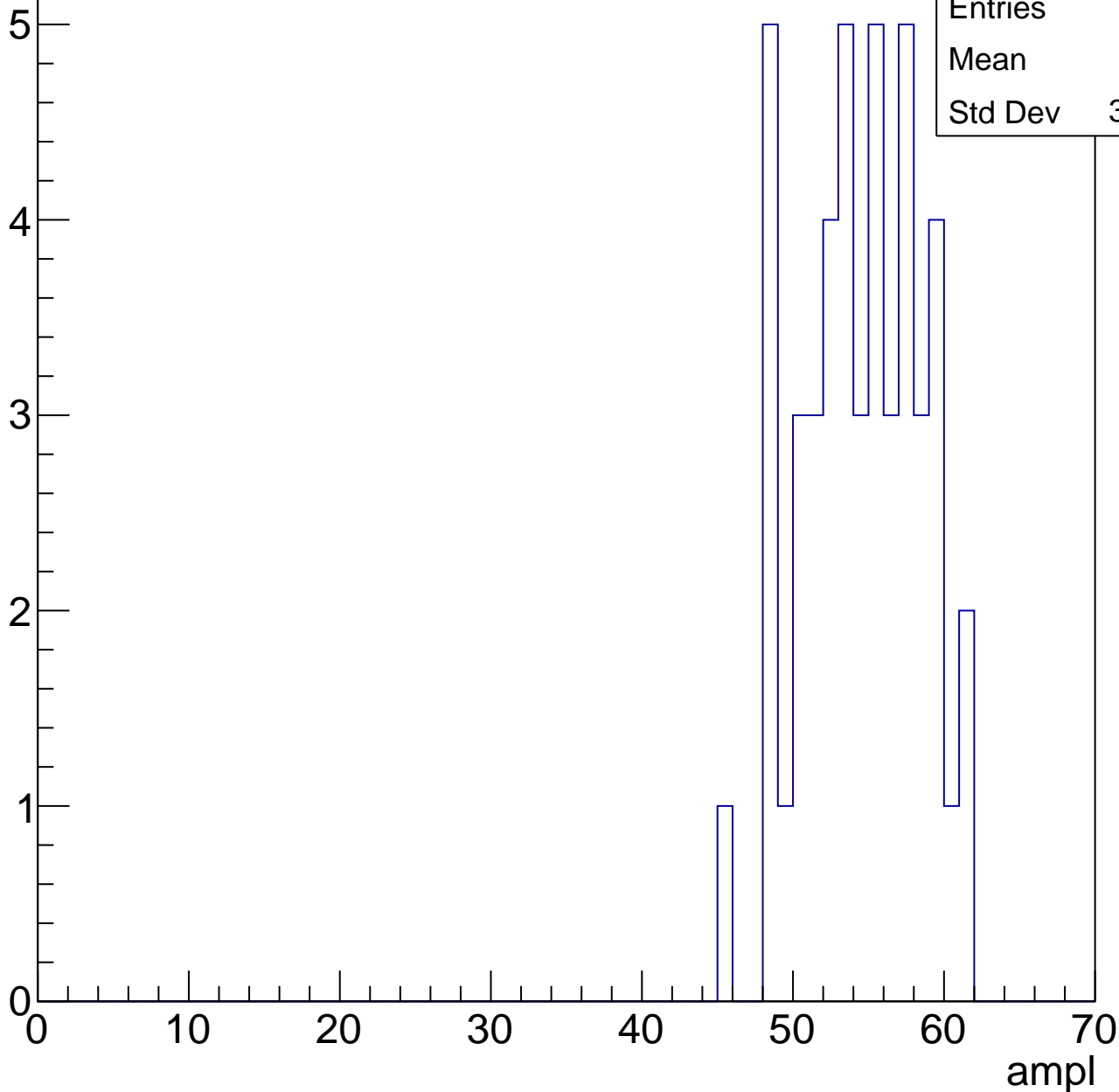


# B1L103S, U21-ch36, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	48
Mean	54
Std Dev	3.889

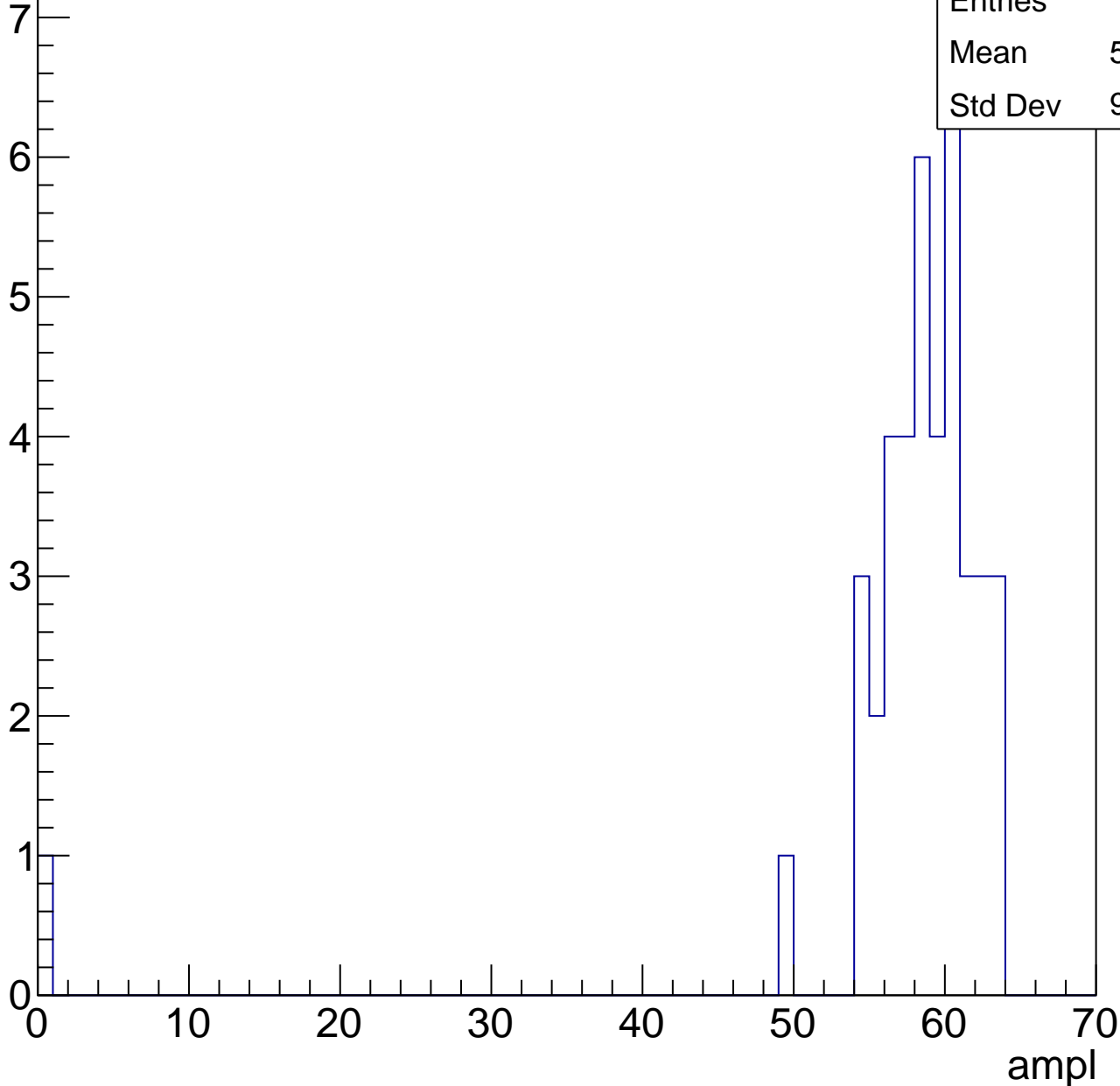


# B1L103S, U21-ch36, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	41
Mean	56.95
Std Dev	9.458

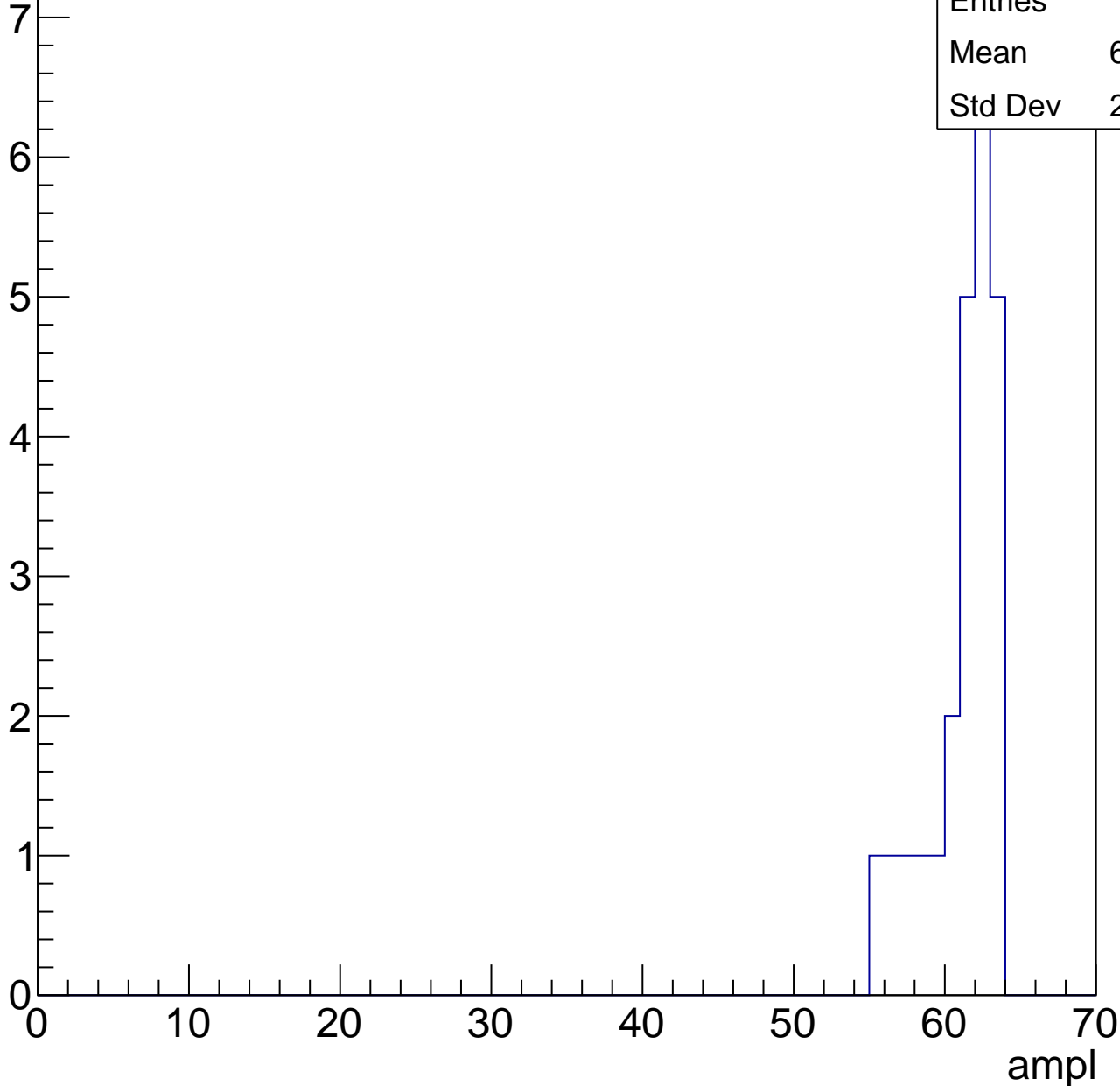


# B1L103S, U21-ch36, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	24
Mean	60.79
Std Dev	2.217





# B1L103S, U21-ch36, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U21-ch37, adc0

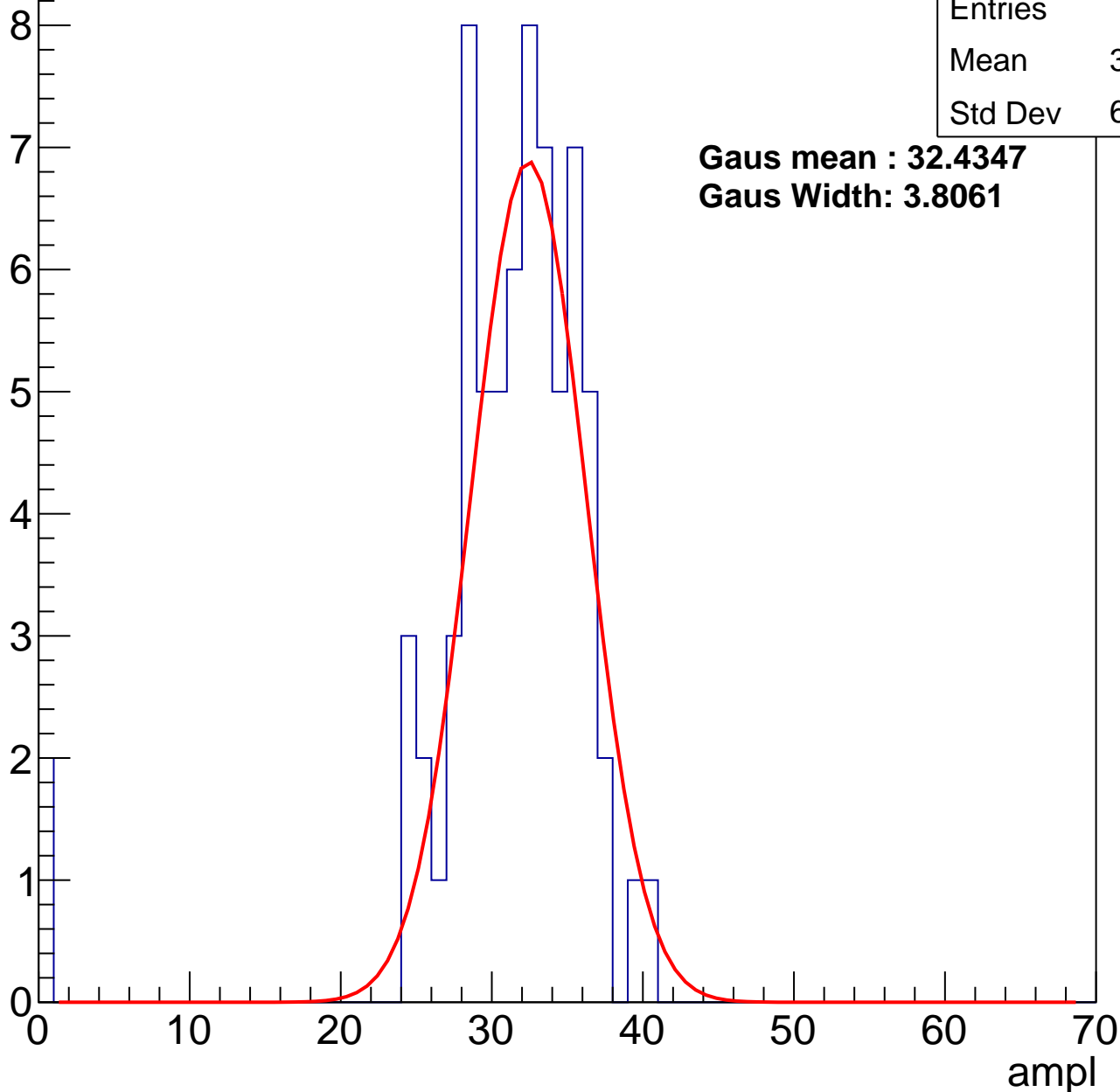
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	30.55
Std Dev	6.315

**Gaus mean : 32.4347**

**Gaus Width: 3.8061**



# B1L103S, U21-ch37, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	81
Mean	39.25
Std Dev	3.647

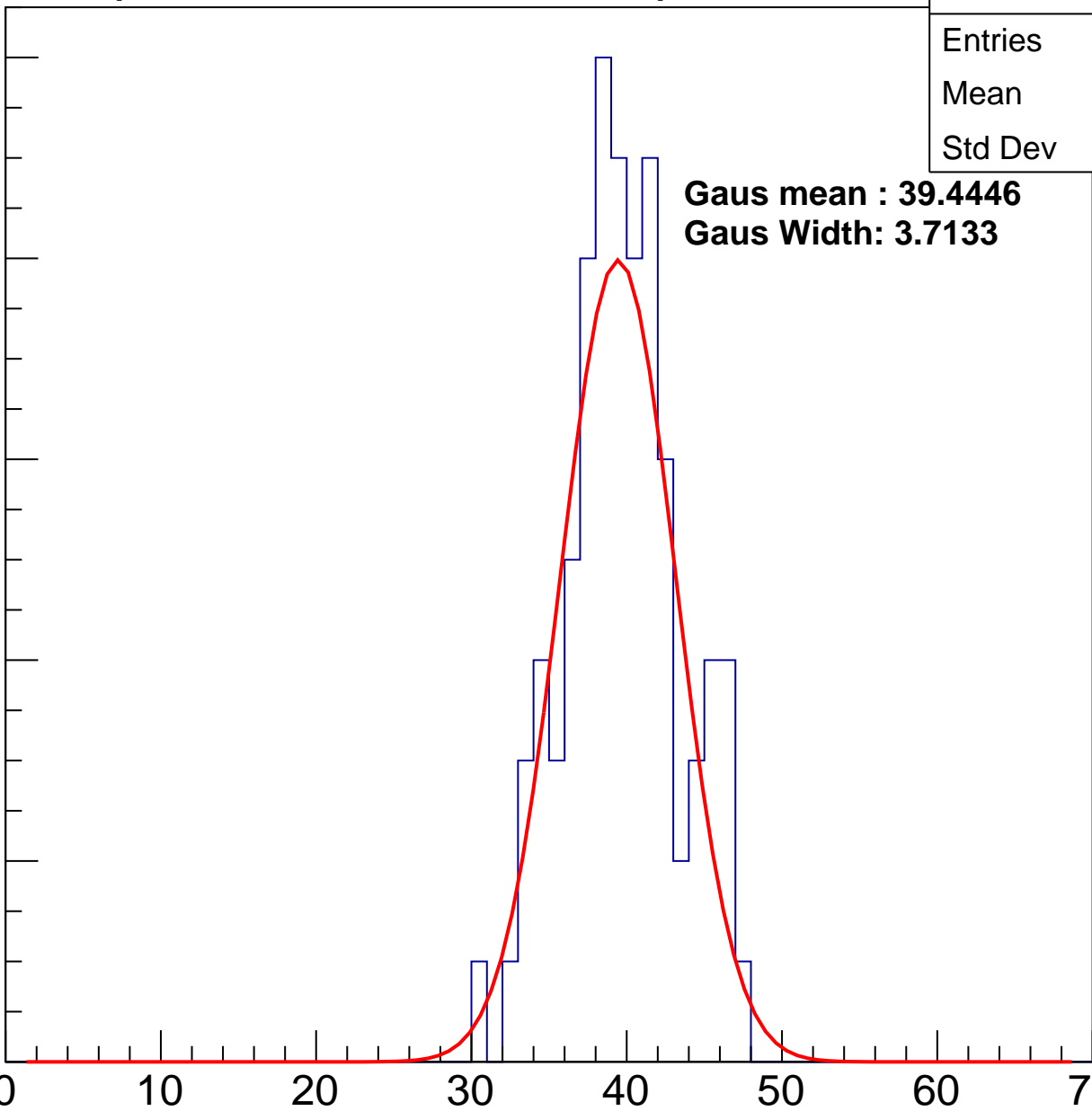
**Gaus mean : 39.4446**

**Gaus Width: 3.7133**

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L103S, U21-ch37, adc2

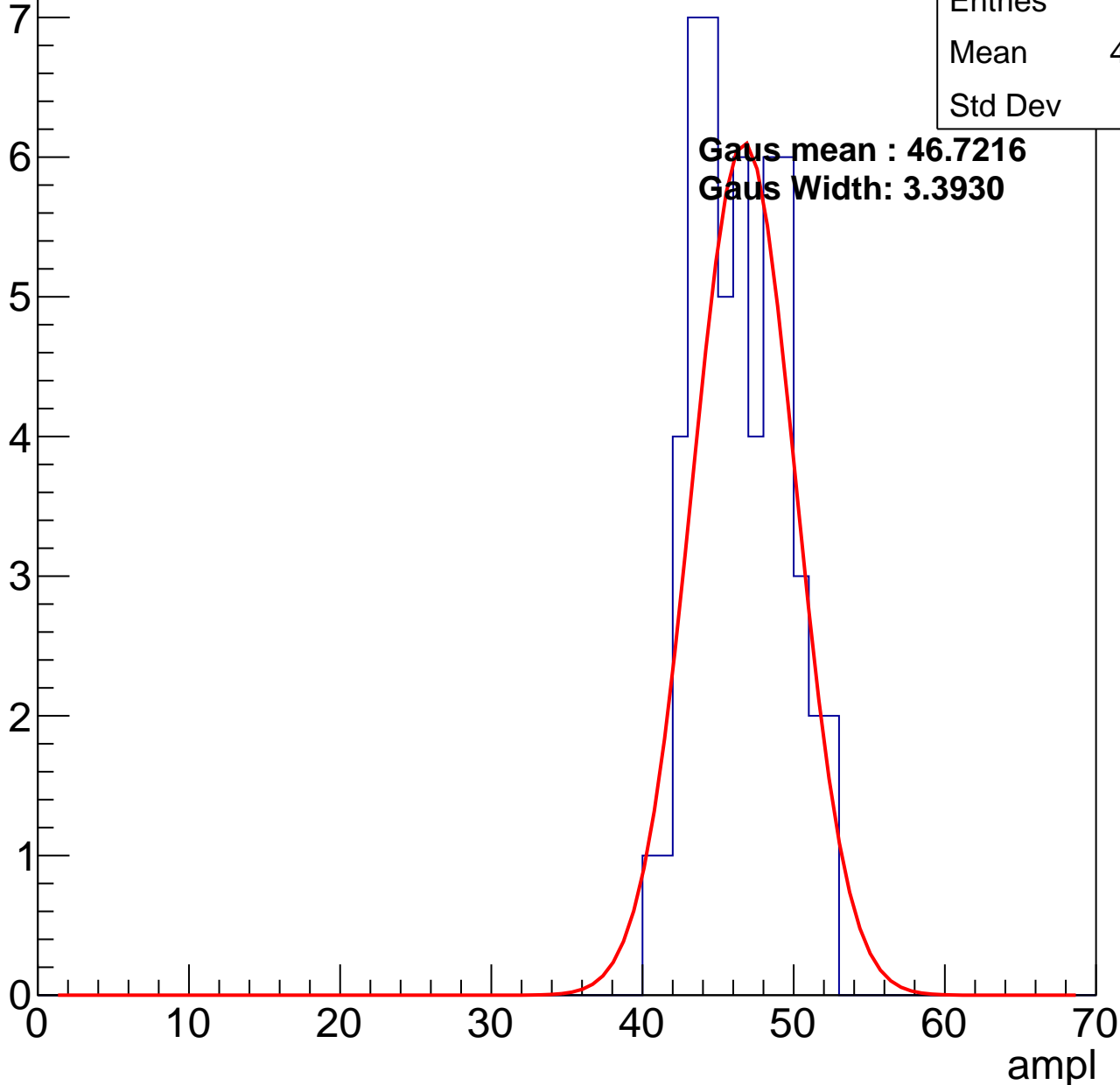
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	46.02
Std Dev	2.96

Gaus mean : 46.7216

Gaus Width: 3.3930

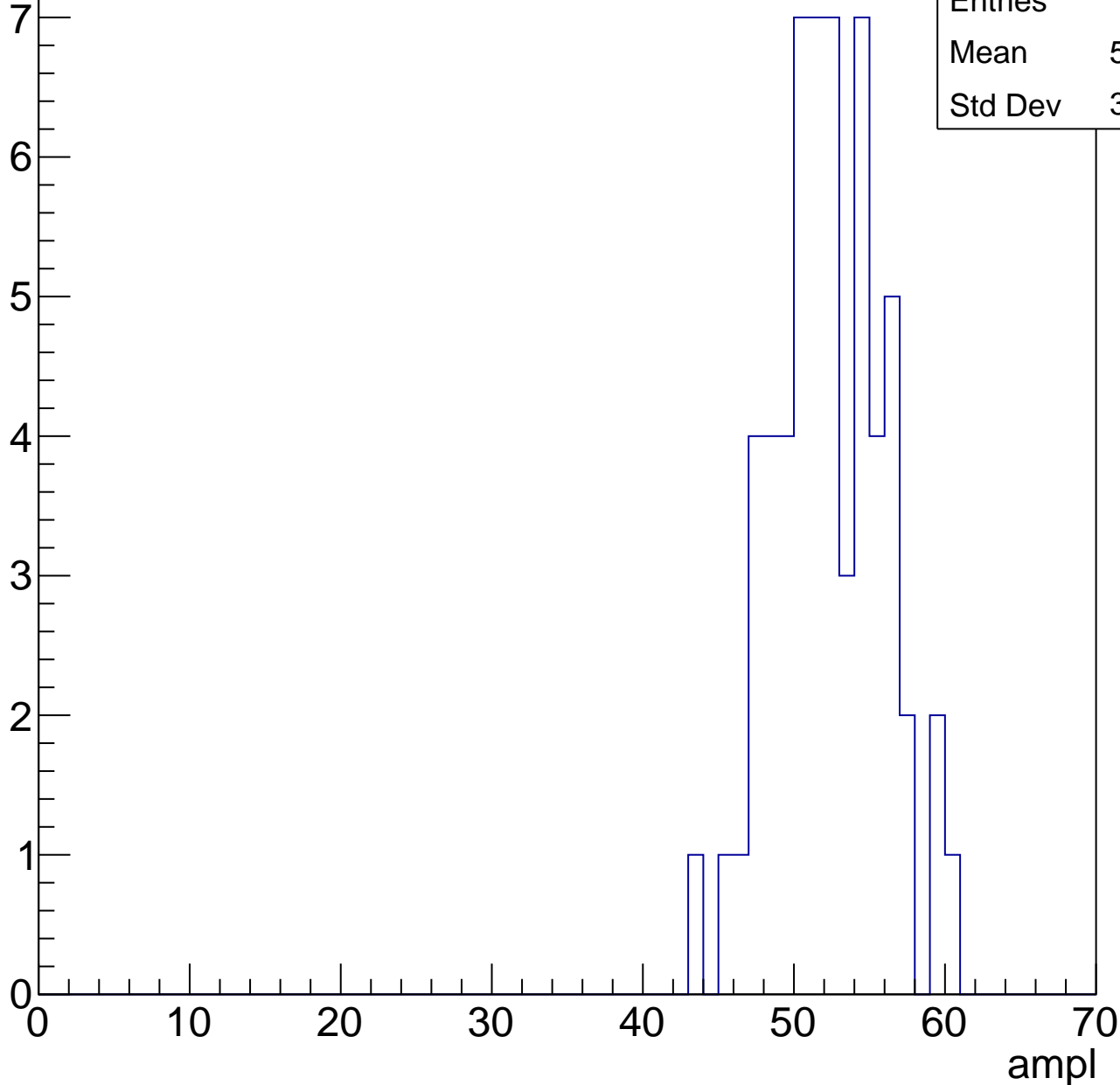


# B1L103S, U21-ch37, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	51.83
Std Dev	3.555

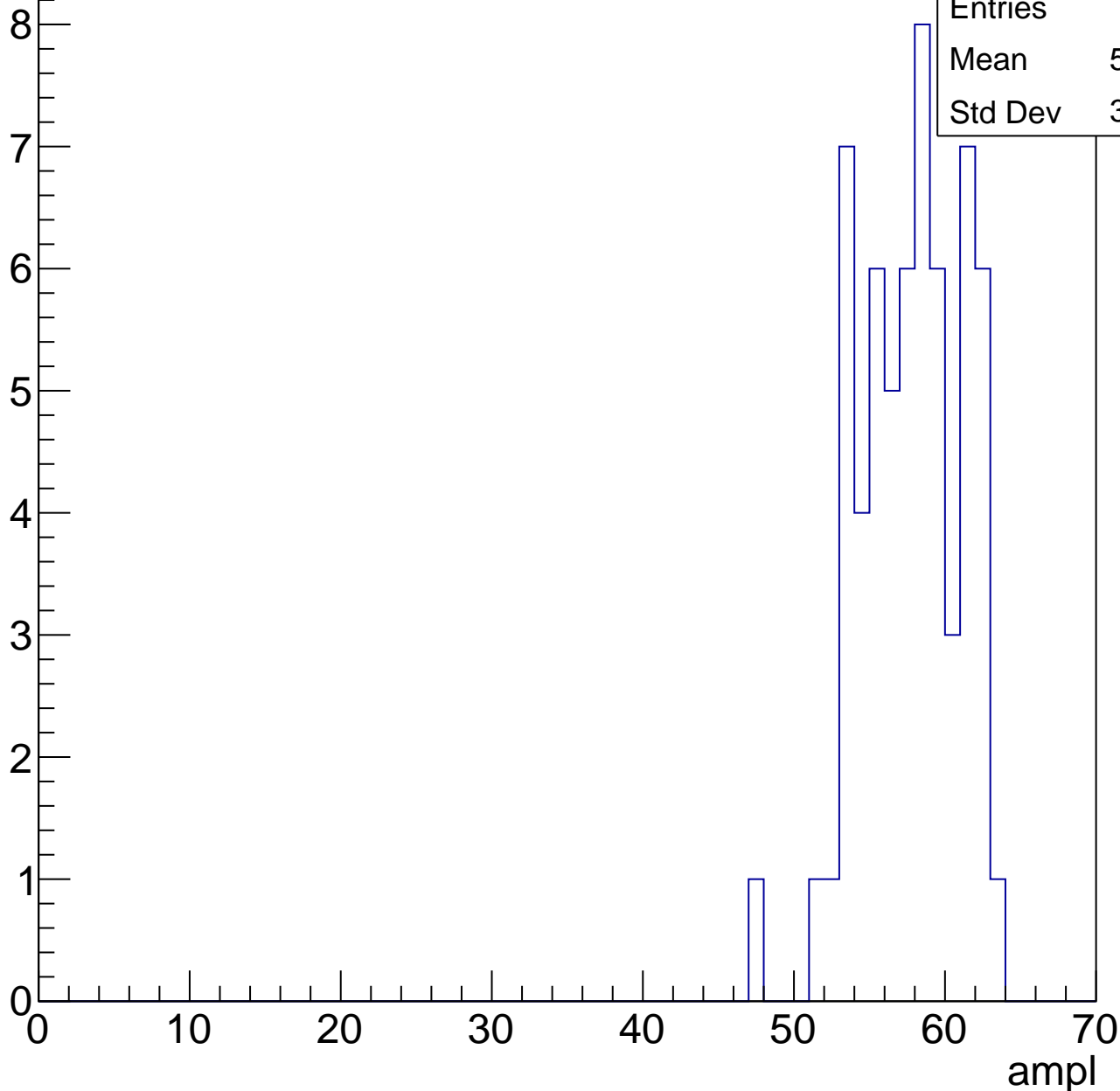


# B1L103S, U21-ch37, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	57.24
Std Dev	3.339

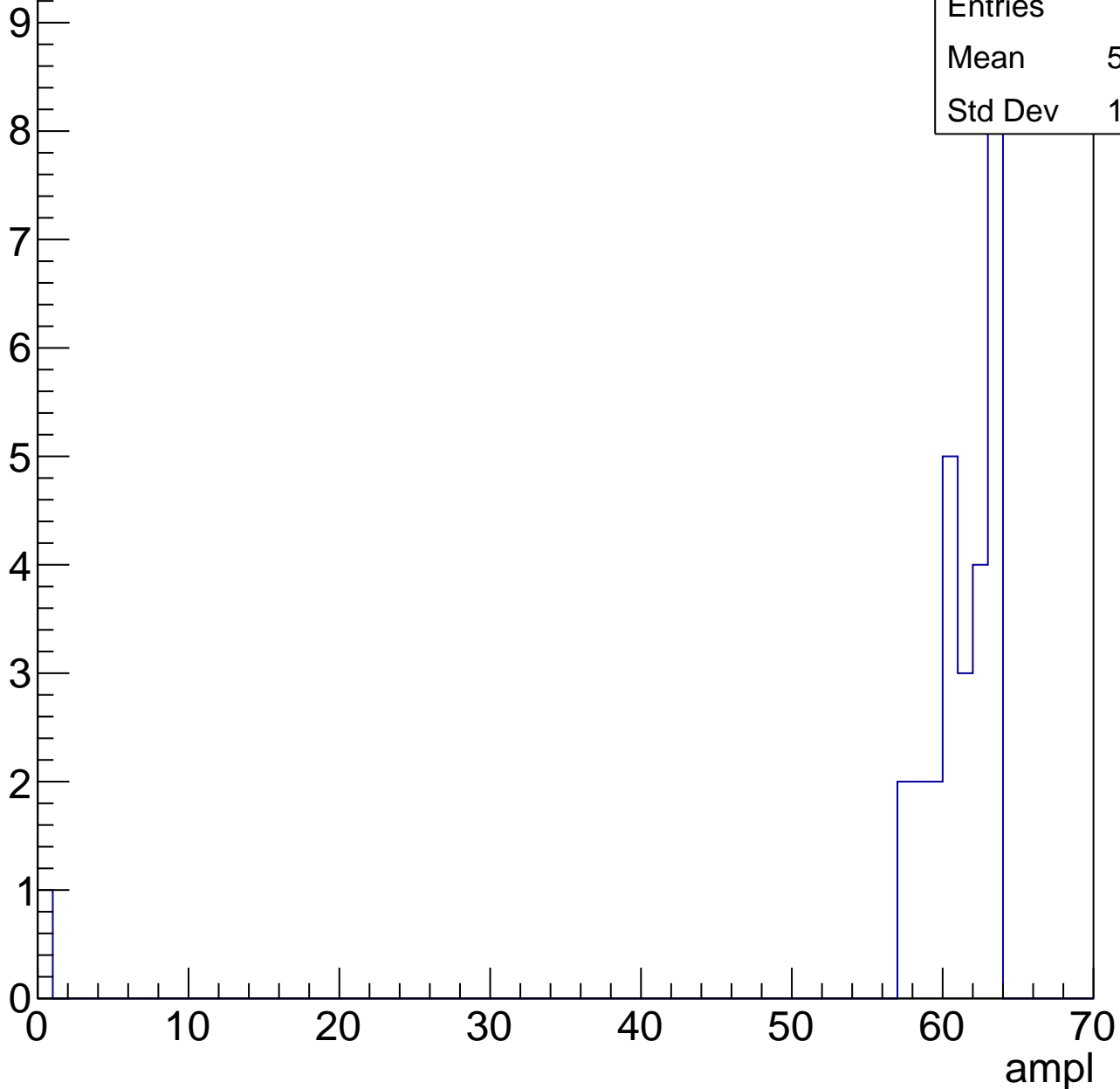


# B1L103S, U21-ch37, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	28
Mean	58.79
Std Dev	11.47



# B1L103S, U21-ch37, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U21-ch37, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U21-ch38, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	98
Mean	29.4
Std Dev	4.261

**Gaus mean : 29.2245**

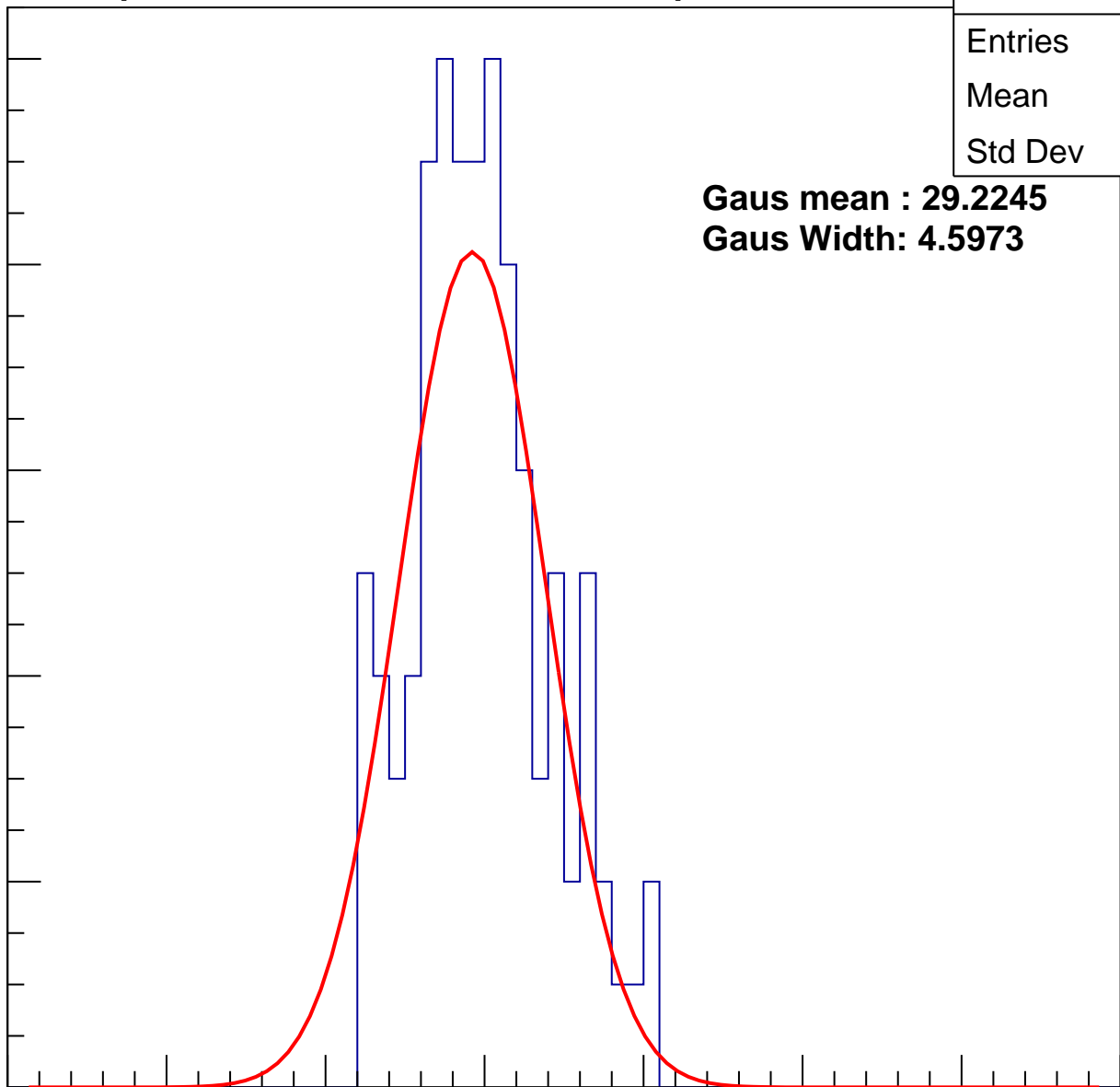
**Gaus Width: 4.5973**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U21-ch38, adc1

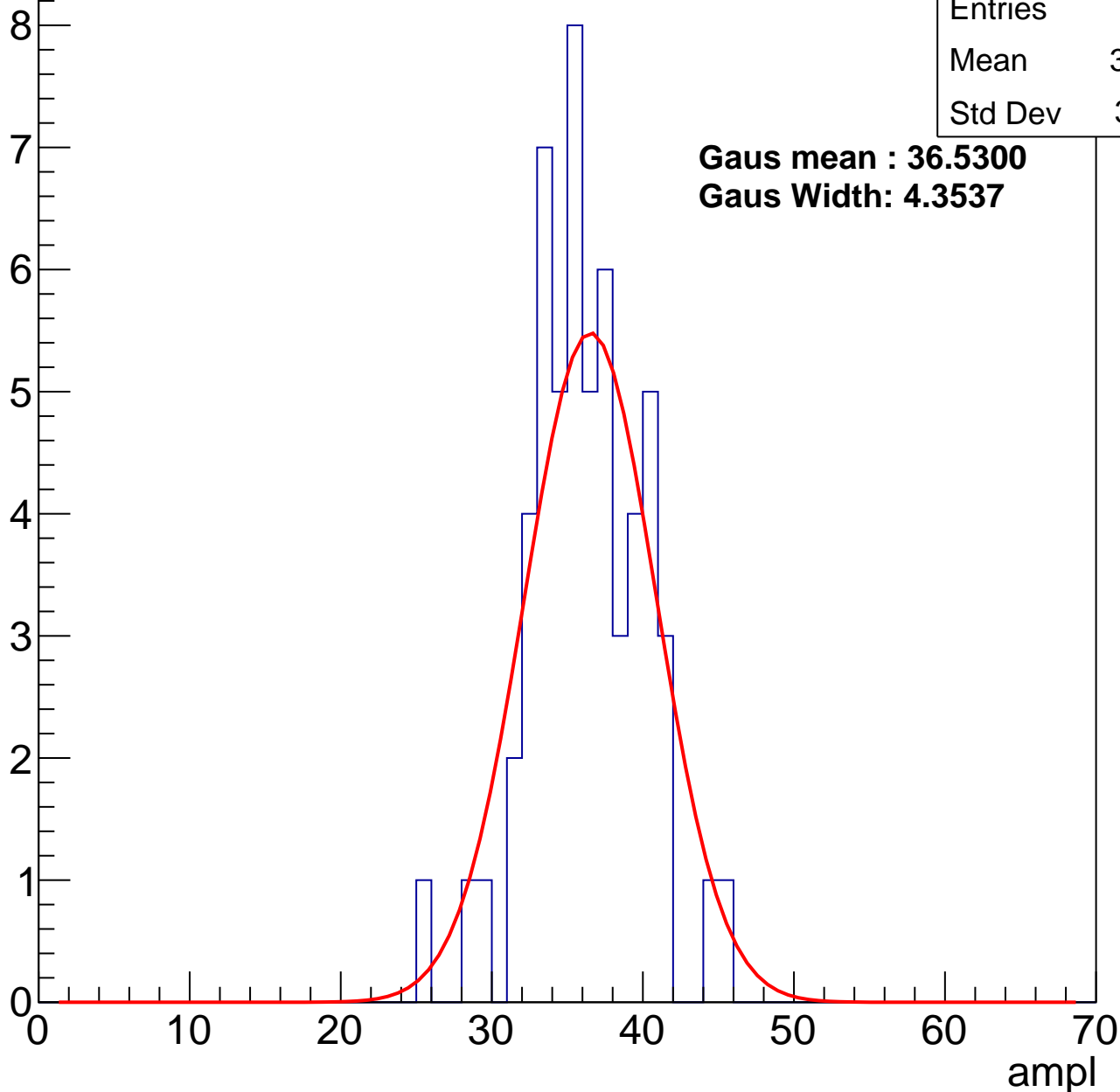
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	35.74
Std Dev	3.721

**Gaus mean : 36.5300**

**Gaus Width: 4.3537**



# B1L103S, U21-ch38, adc2

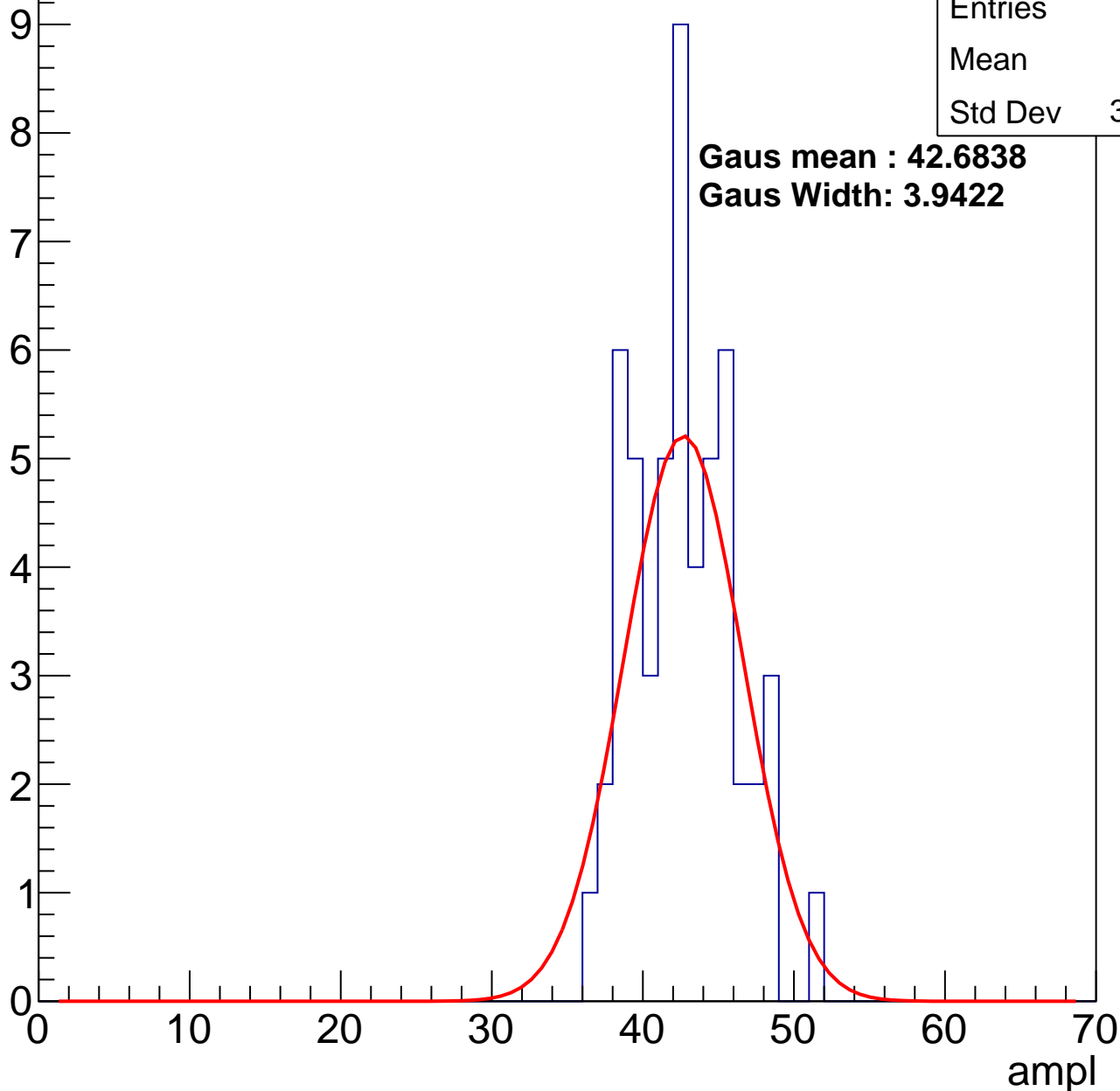
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	42.2
Std Dev	3.308

**Gaus mean : 42.6838**

**Gaus Width: 3.9422**

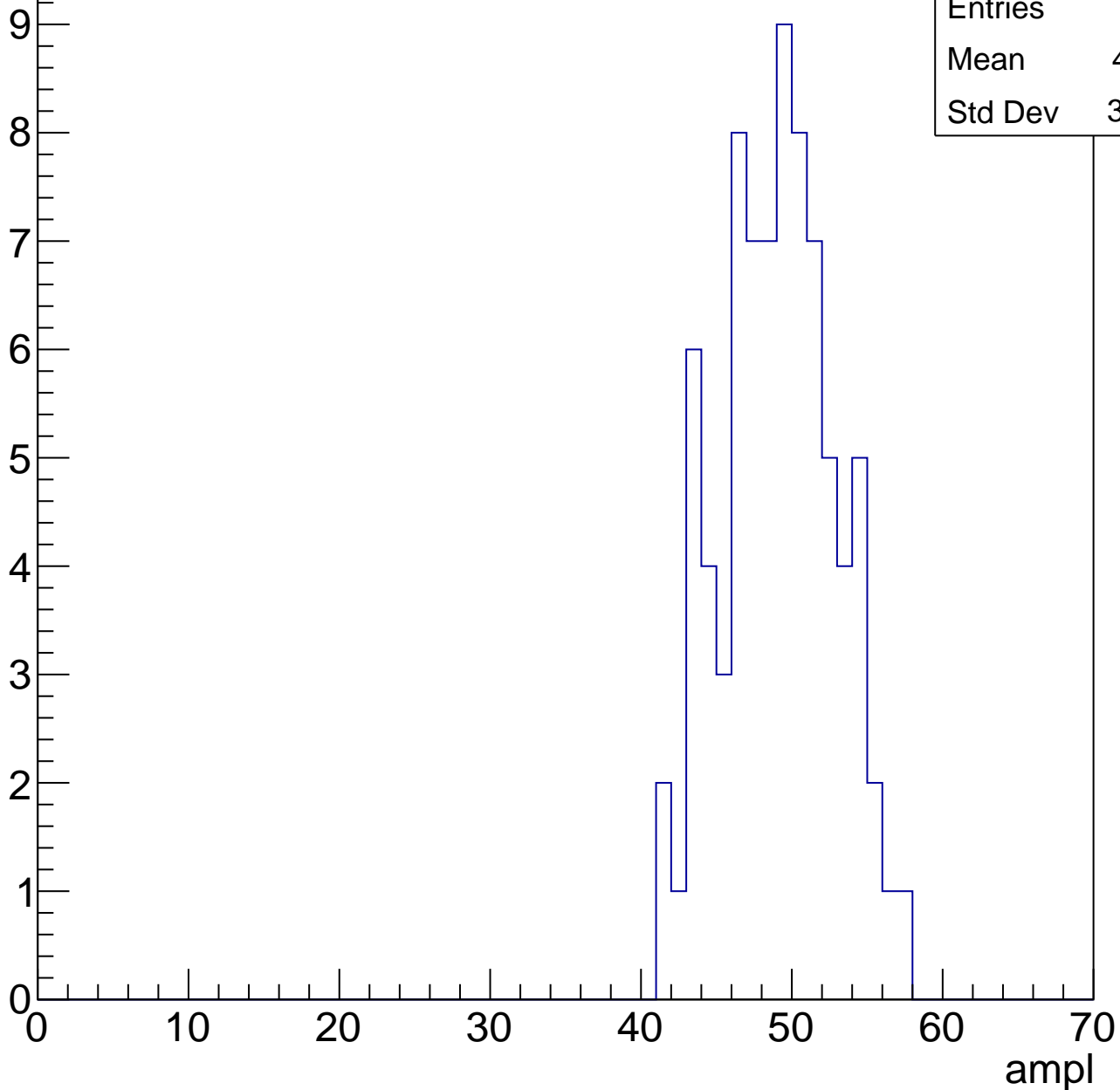


# B1L103S, U21-ch38, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	80
Mean	48.61
Std Dev	3.693

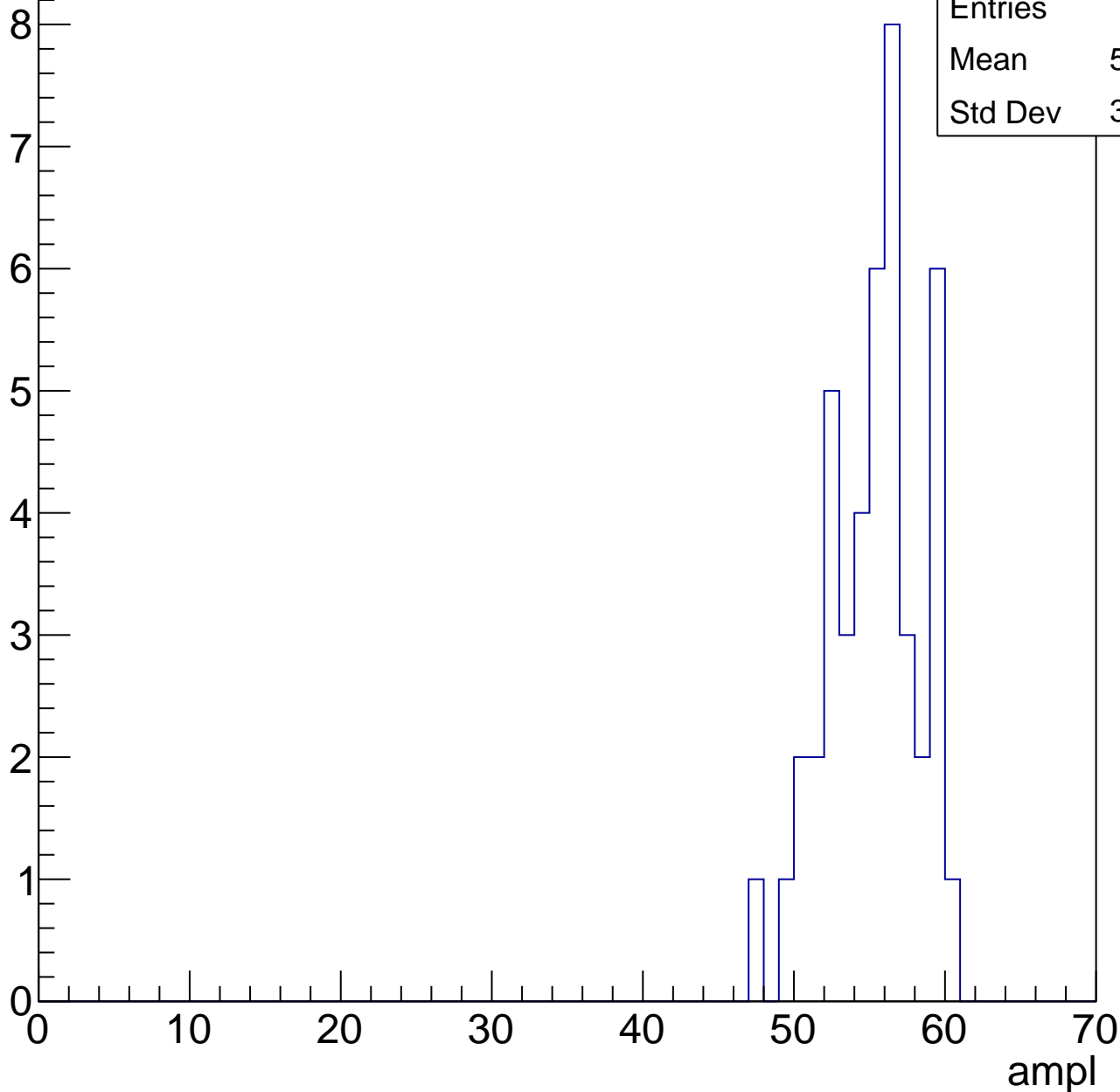


# B1L103S, U21-ch38, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

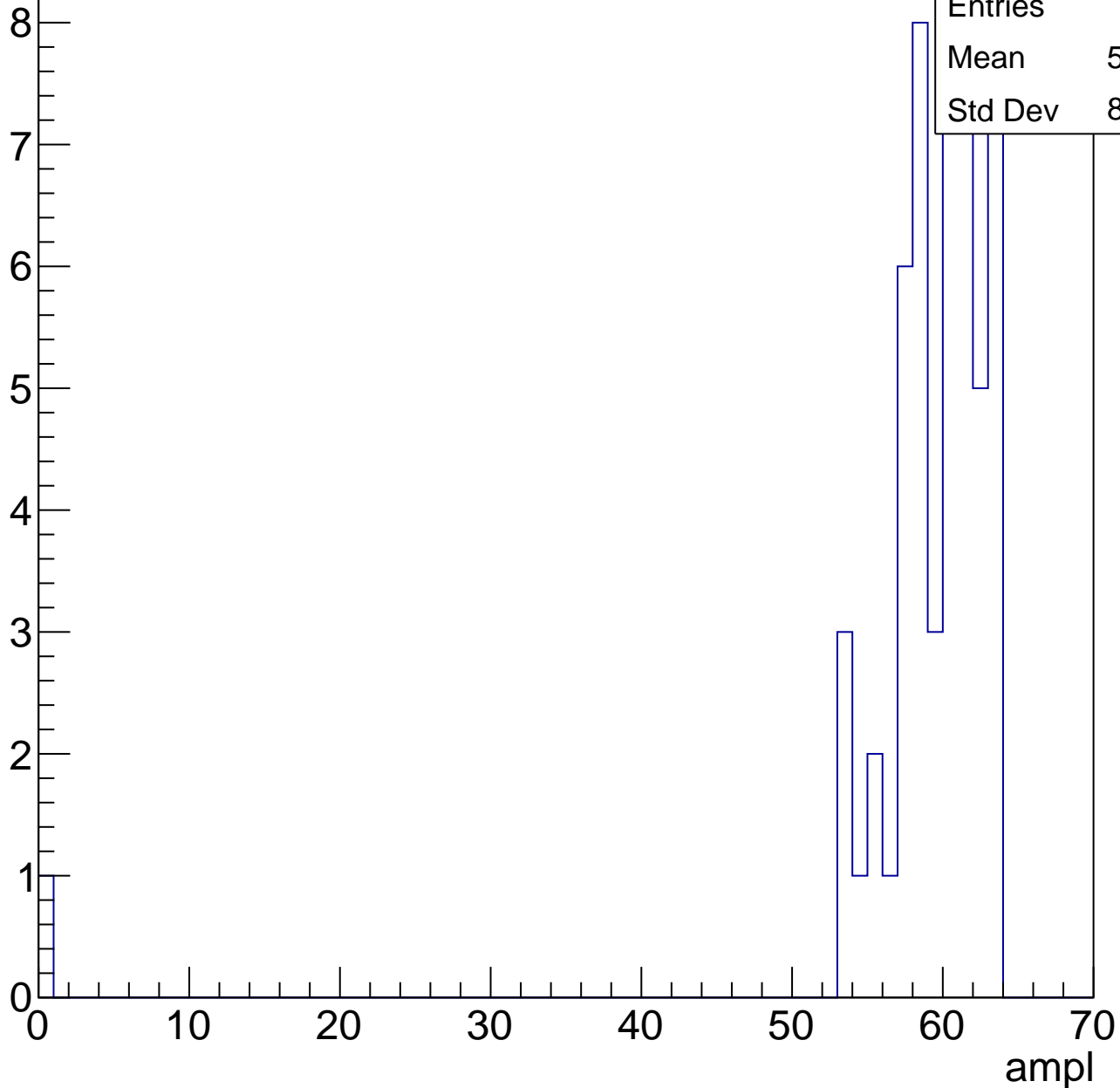
Entries	44
Mean	54.82
Std Dev	3.017



# B1L103S, U21-ch38, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

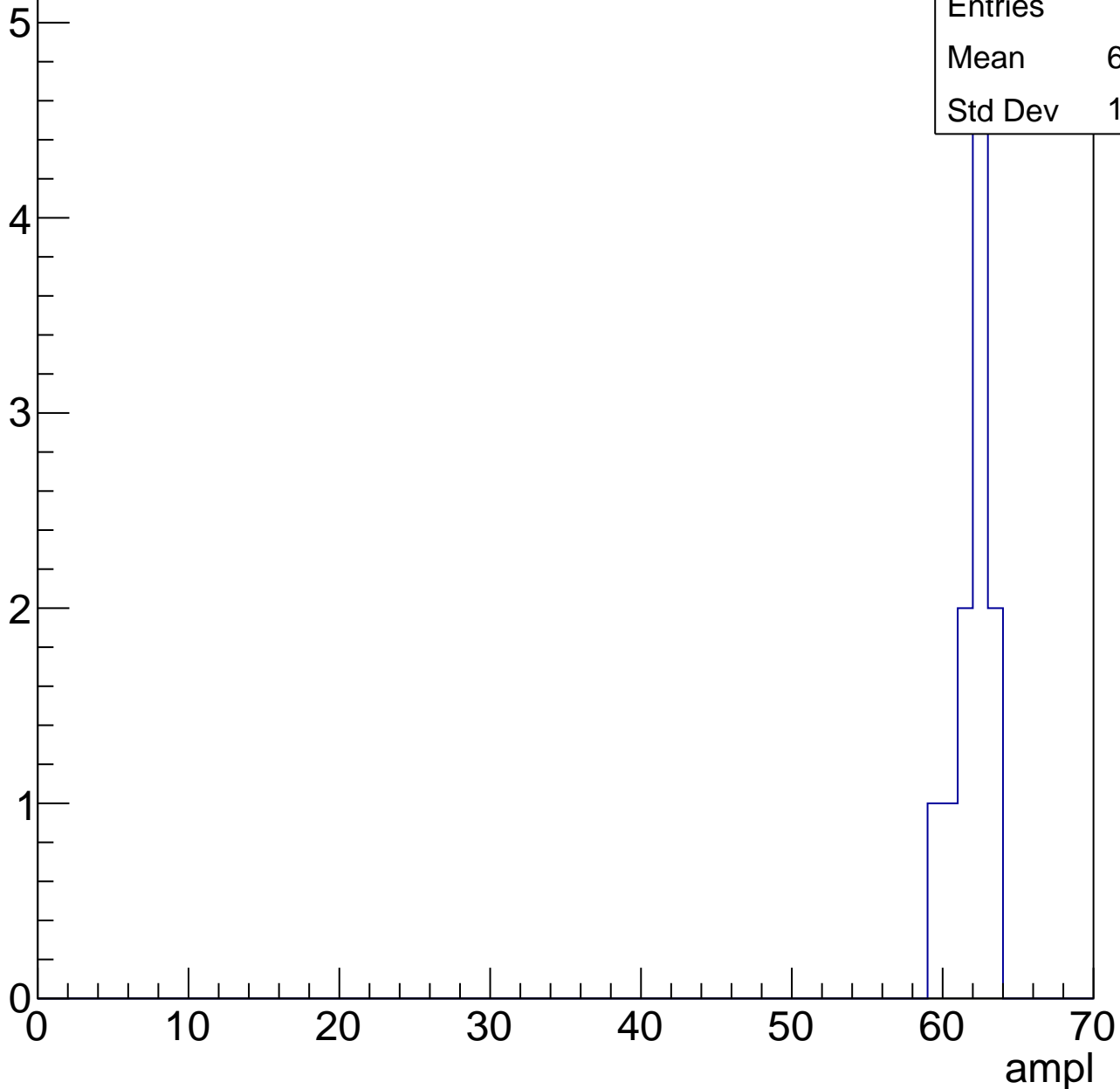


# B1L103S, U21-ch38, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	11
Mean	61.55
Std Dev	1.157





# B1L103S, U21-ch38, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	11
Std Dev	11

# B1L103S, U21-ch39, adc0

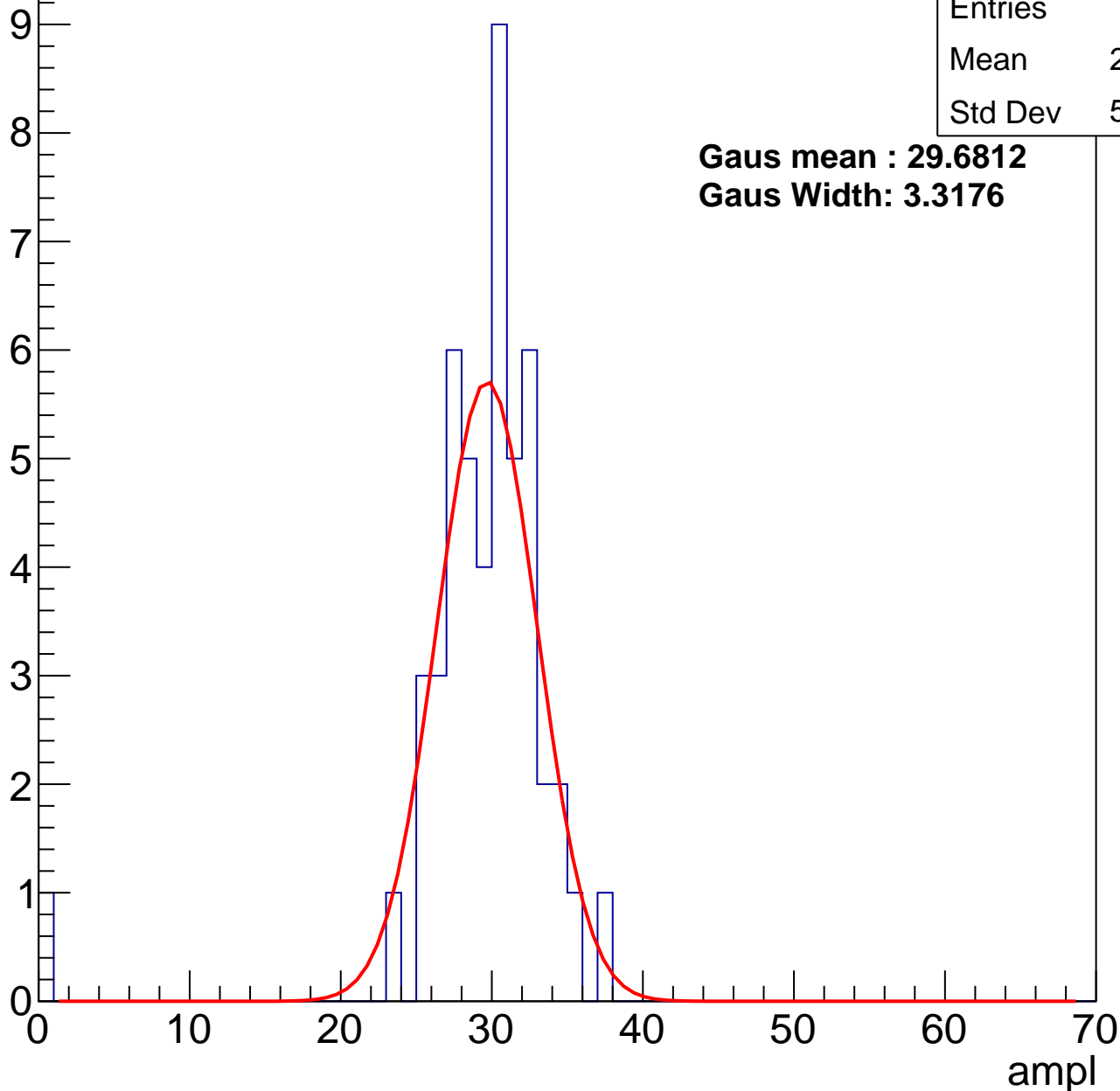
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	28.92
Std Dev	5.042

**Gaus mean : 29.6812**

**Gaus Width: 3.3176**



# B1L103S, U21-ch39, adc1

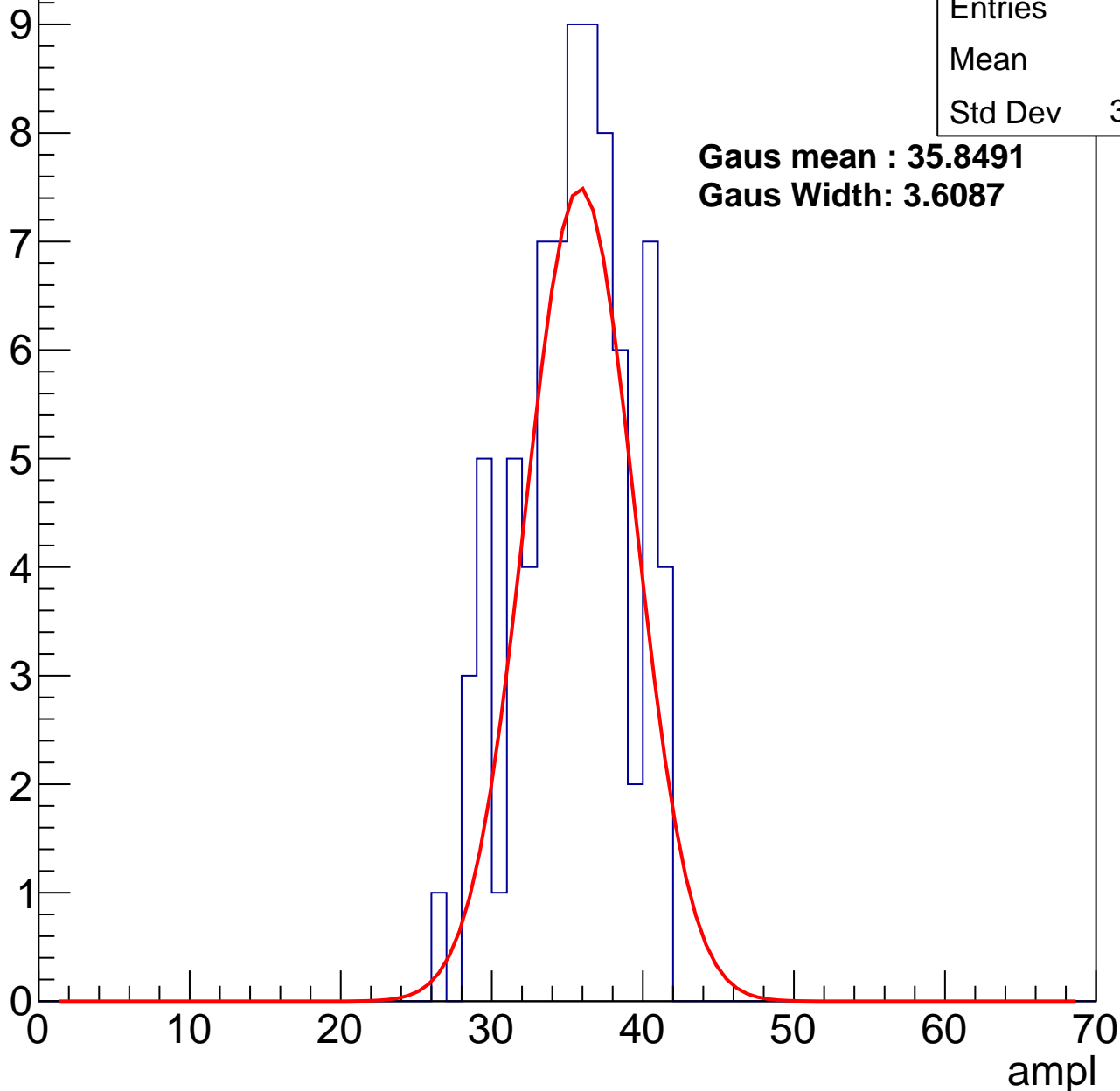
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	34.9
Std Dev	3.632

**Gaus mean : 35.8491**

**Gaus Width: 3.6087**



# B1L103S, U21-ch39, adc2

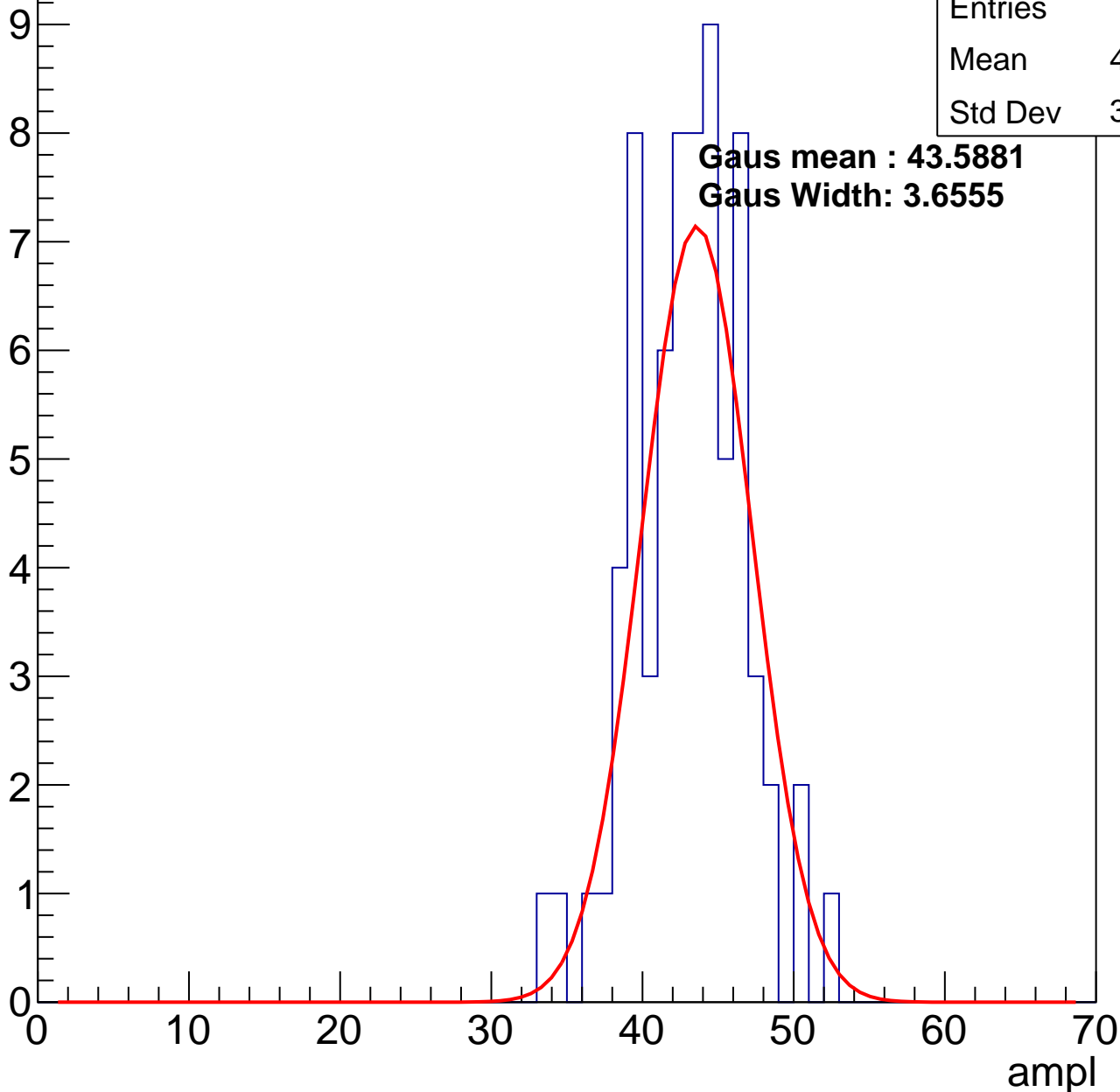
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	42.65
Std Dev	3.604

**Gaus mean : 43.5881**

**Gaus Width: 3.6555**

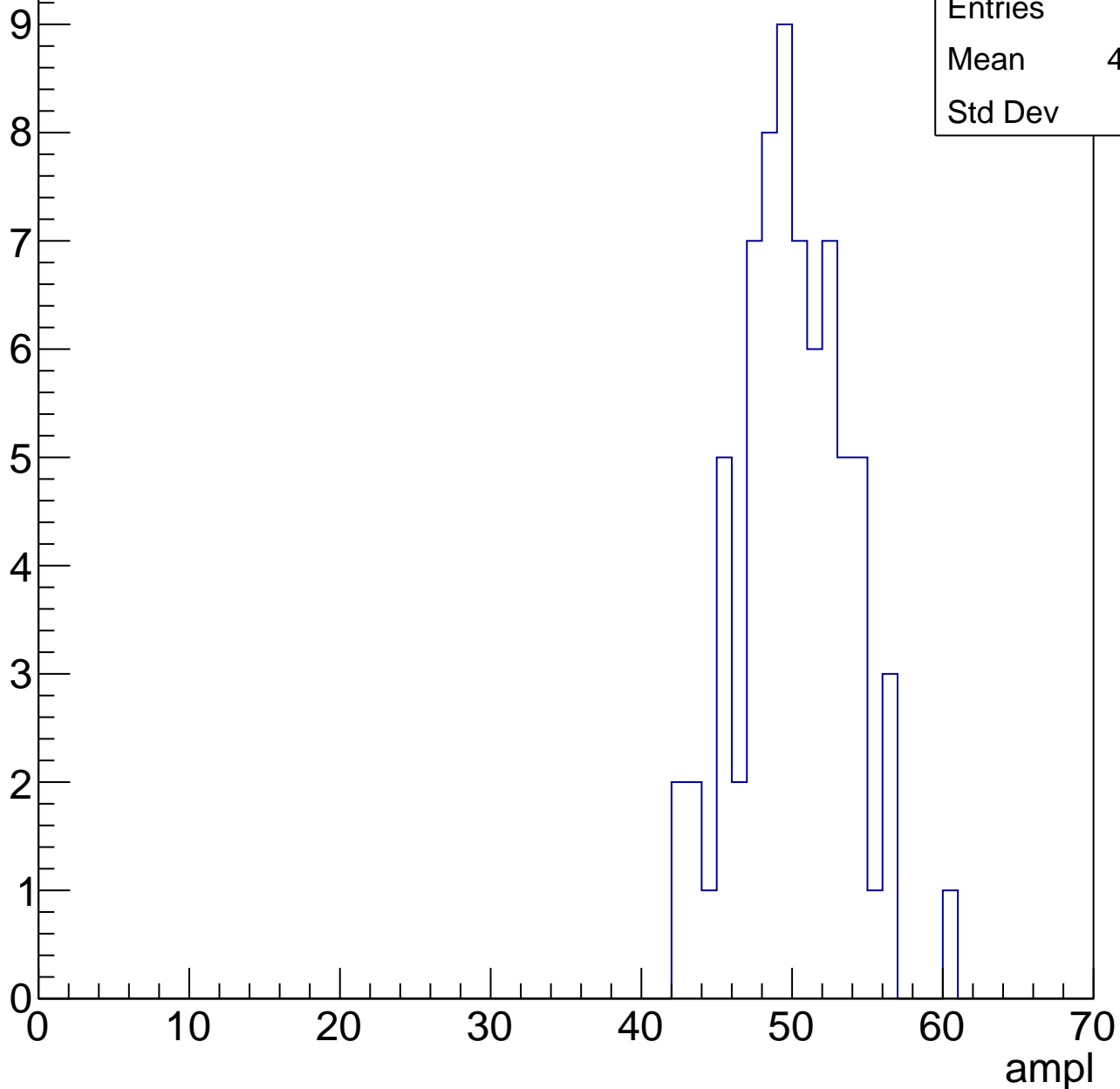


# B1L103S, U21-ch39, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	49.62
Std Dev	3.57

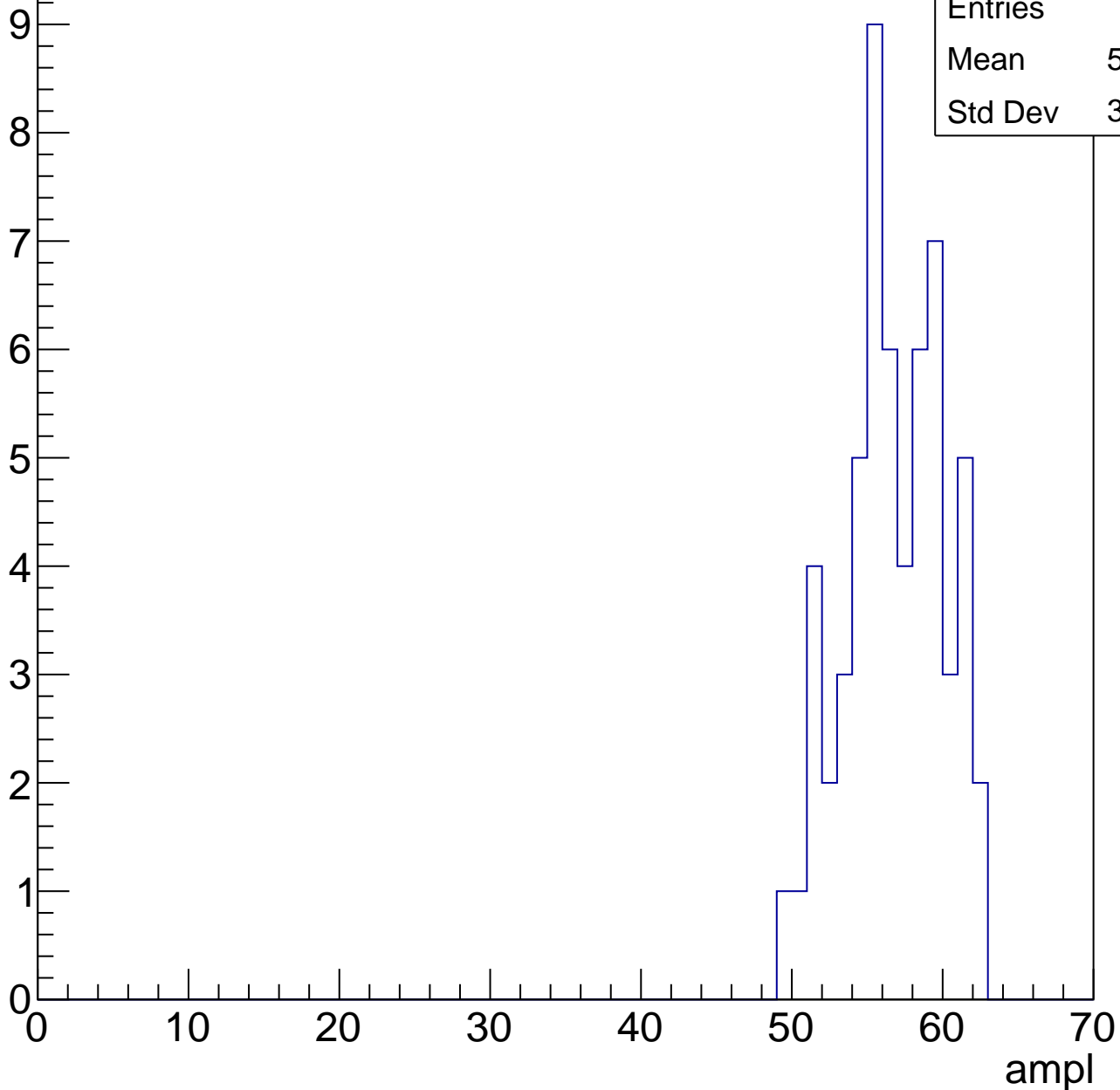


# B1L103S, U21-ch39, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	56.29
Std Dev	3.227

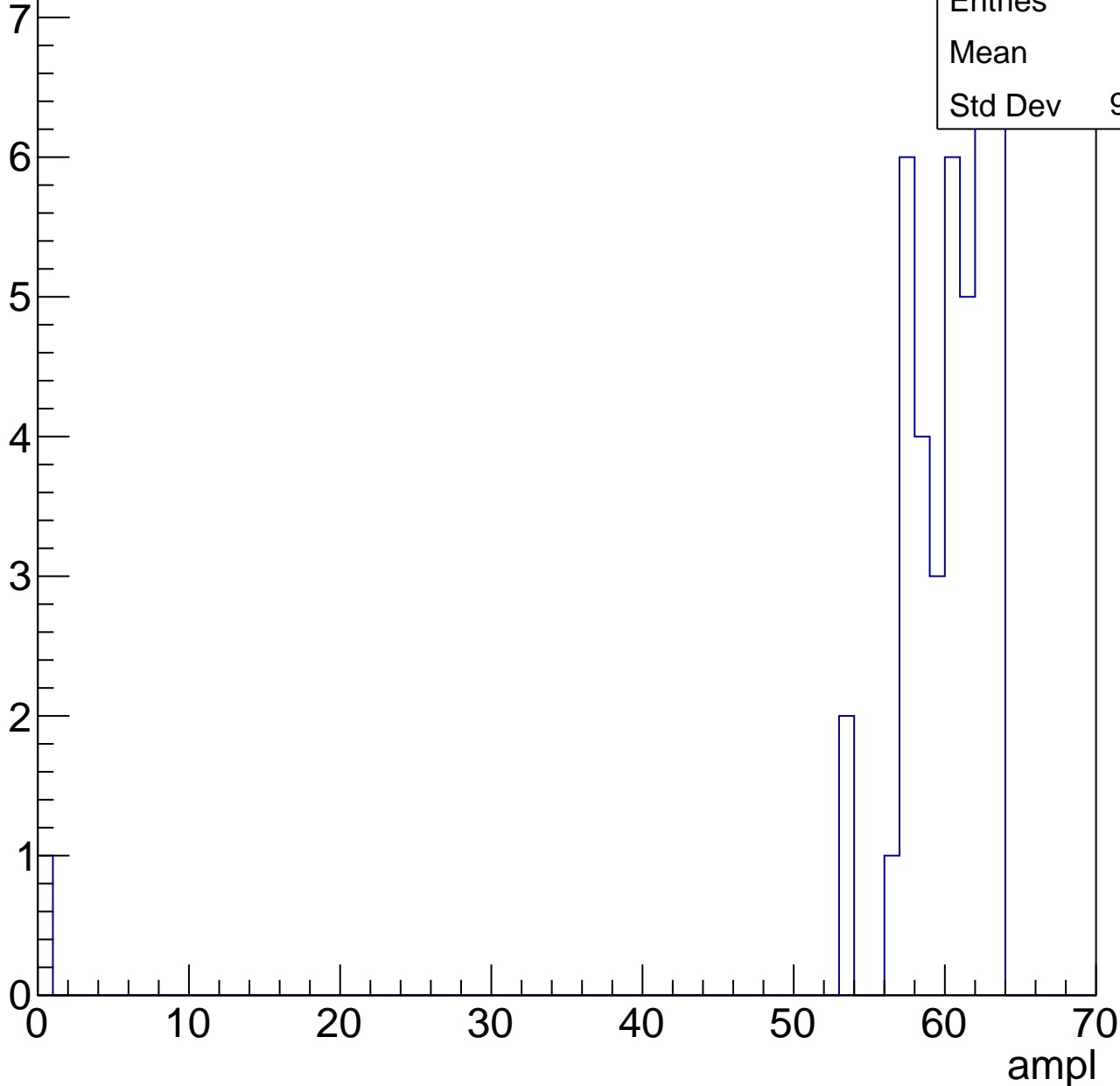


# B1L103S, U21-ch39, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	42
Mean	58.4
Std Dev	9.482



# B1L103S, U21-ch39, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U21-ch39, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L103S, U21-ch40, adc0

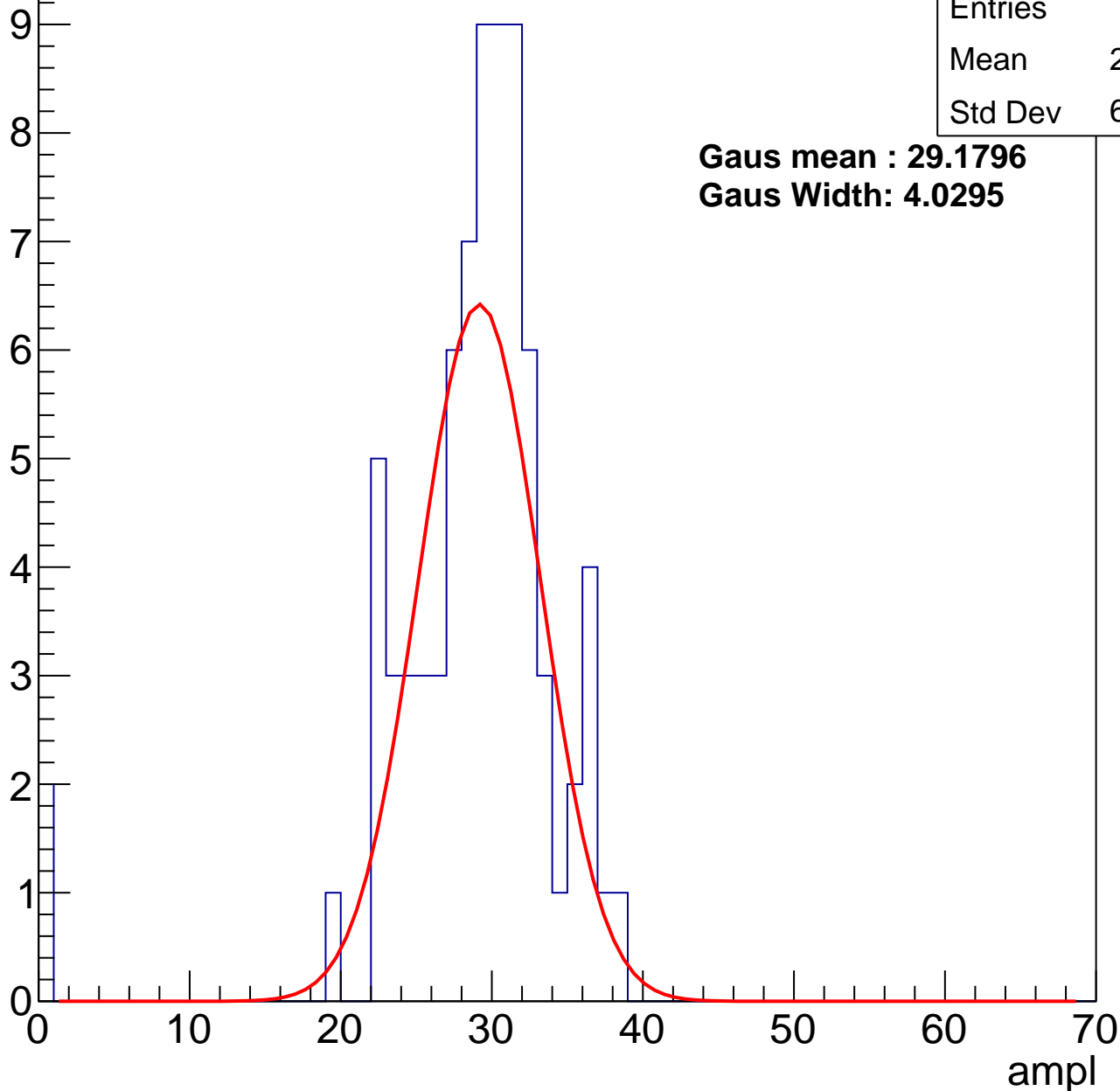
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	28.27
Std Dev	6.055

**Gaus mean : 29.1796**

**Gaus Width: 4.0295**



# B1L103S, U21-ch40, adc1

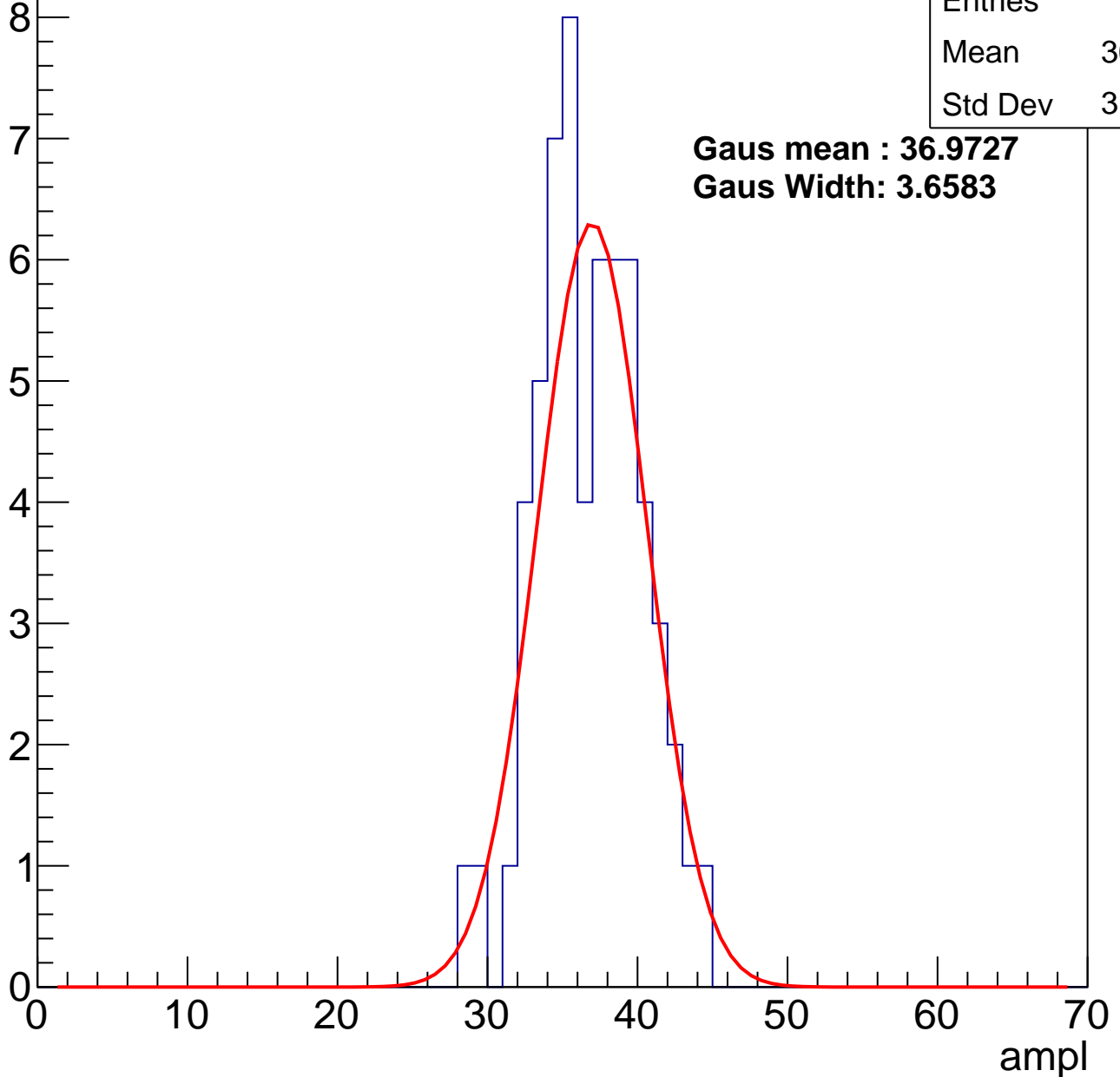
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	36.35
Std Dev	3.376

**Gaus mean : 36.9727**

**Gaus Width: 3.6583**



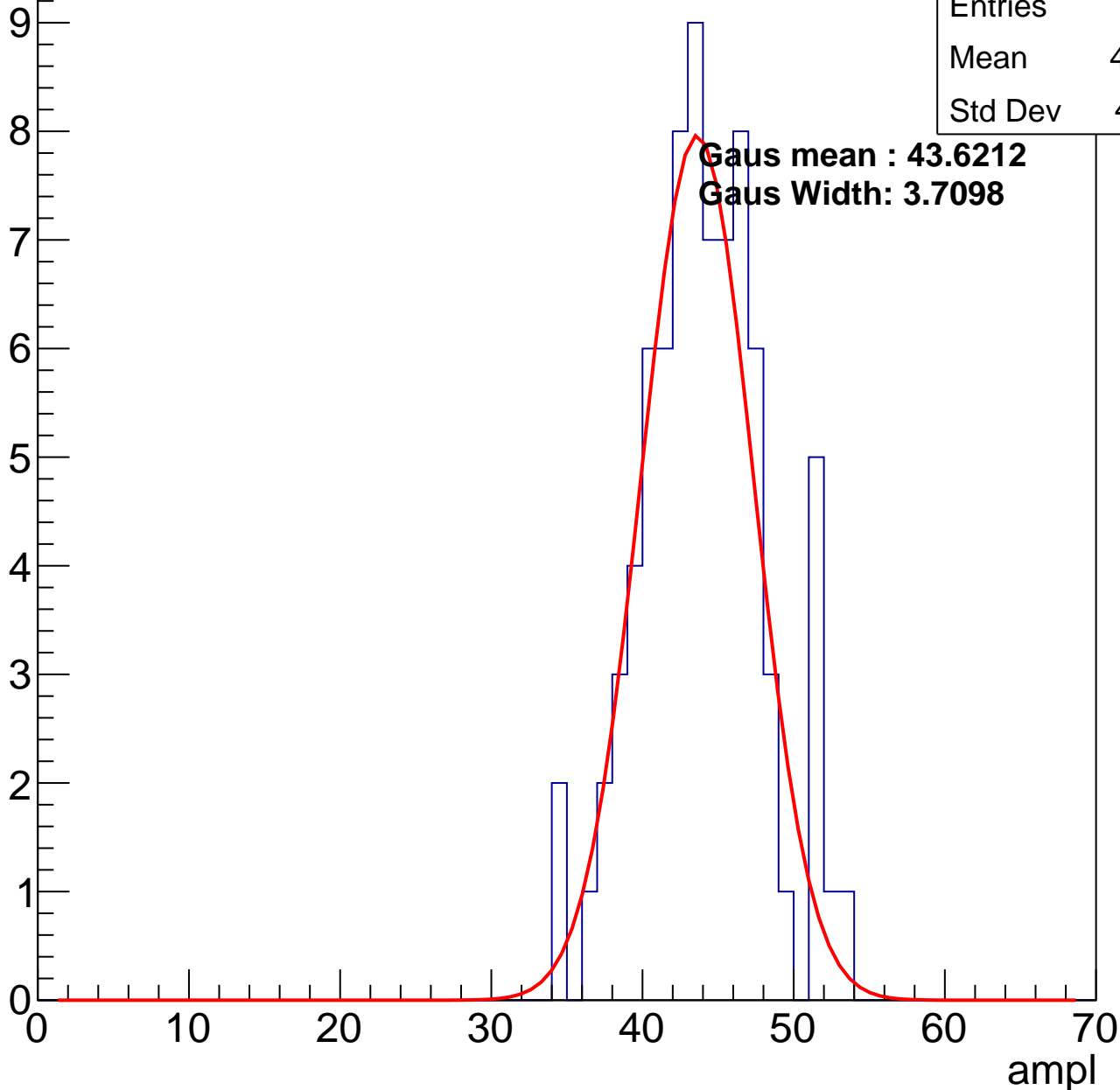
# B1L103S, U21-ch40, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	80
Mean	43.54
Std Dev	4.031

**Gaus mean : 43.6212**  
**Gaus Width: 3.7098**

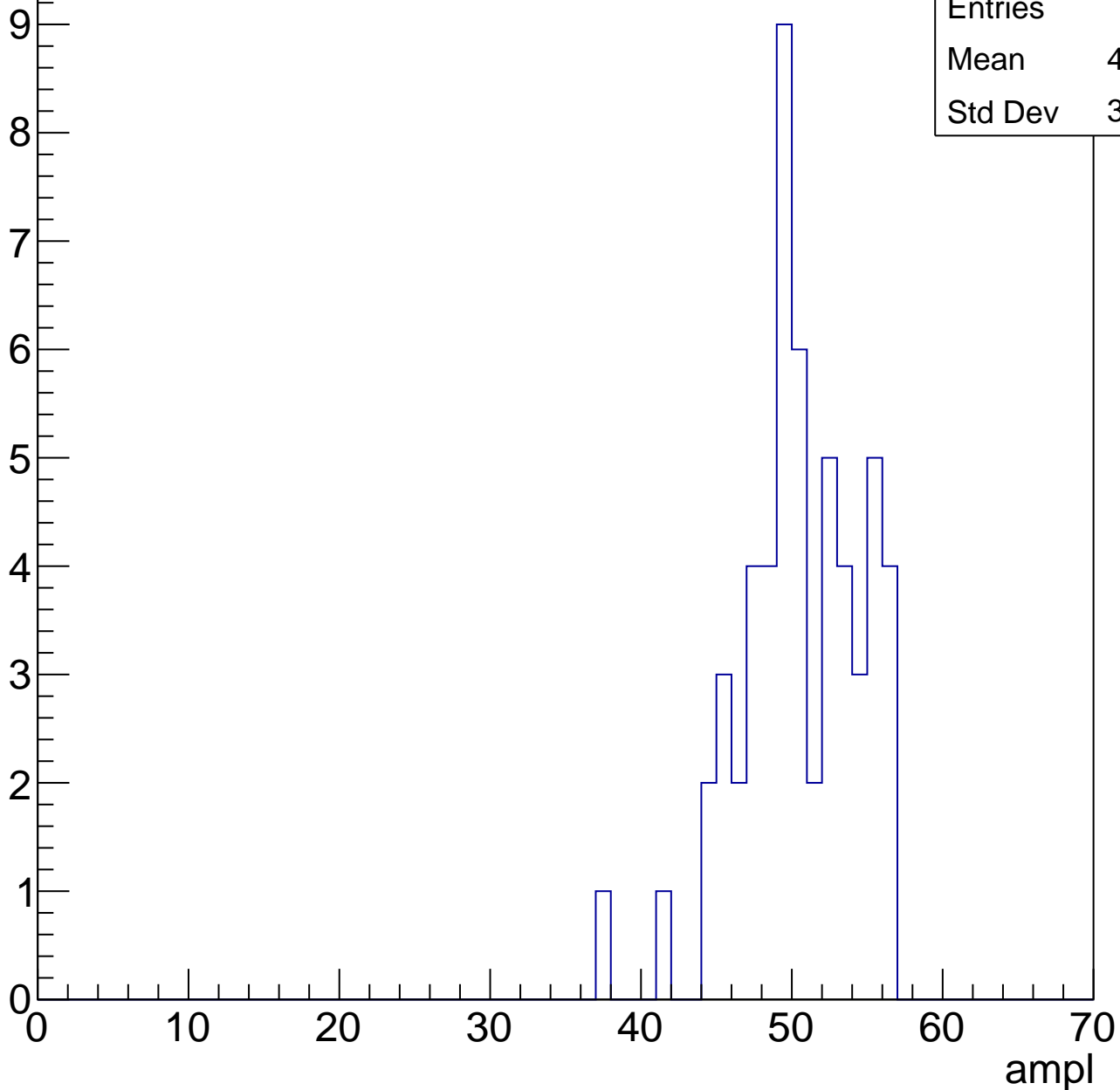


# B1L103S, U21-ch40, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	49.98
Std Dev	3.966

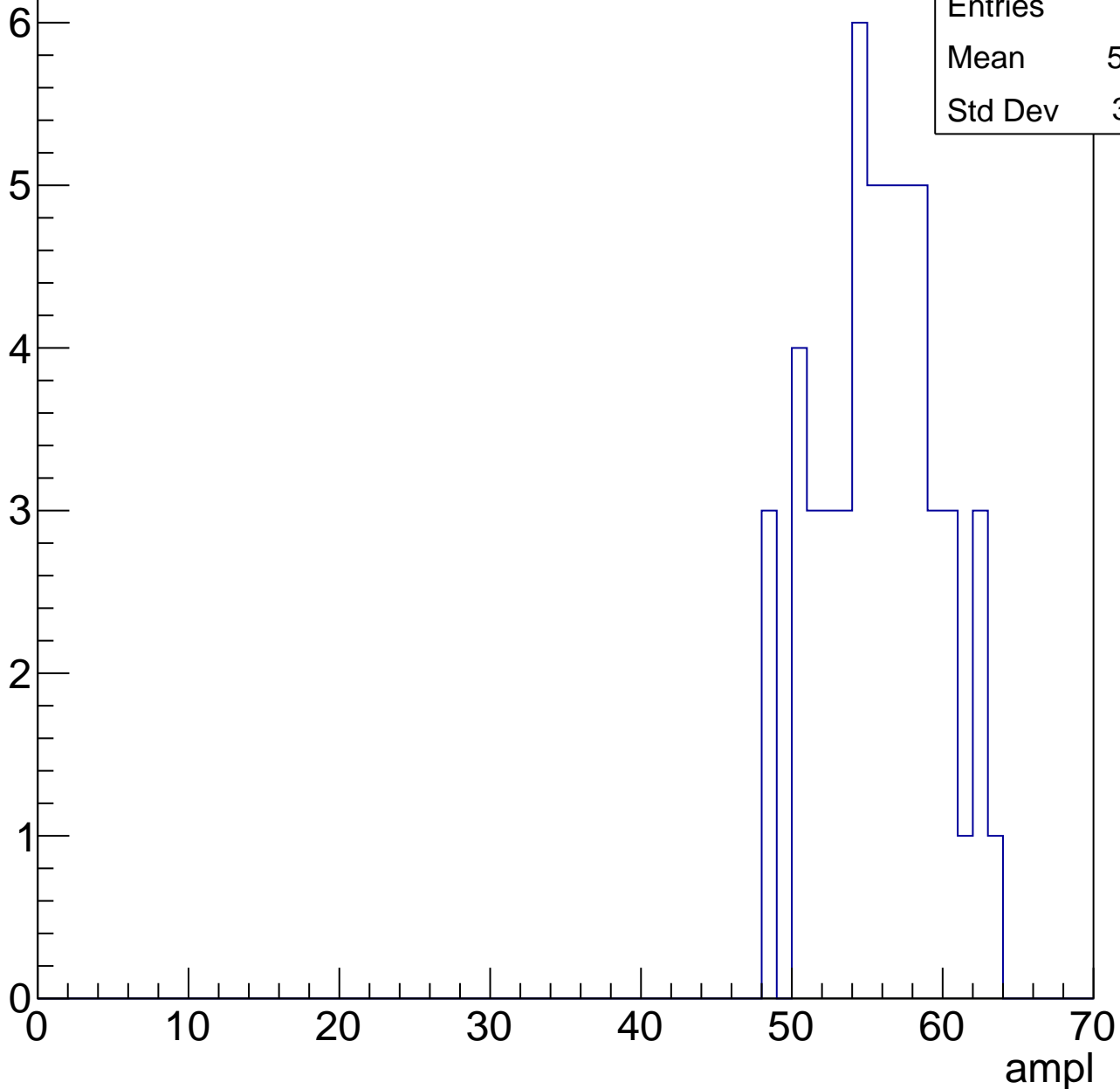


# B1L103S, U21-ch40, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	55.34
Std Dev	3.821

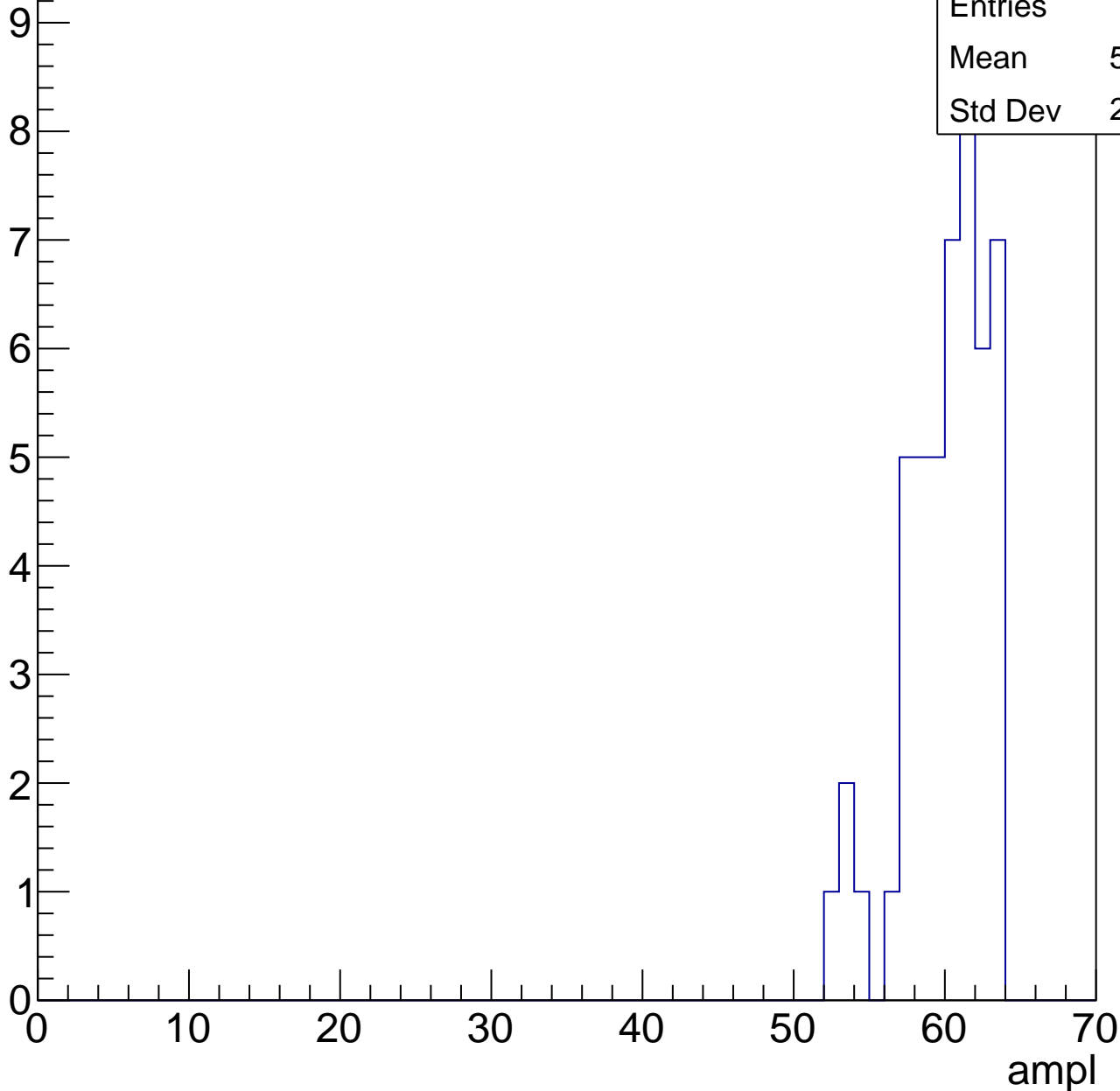


# B1L103S, U21-ch40, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

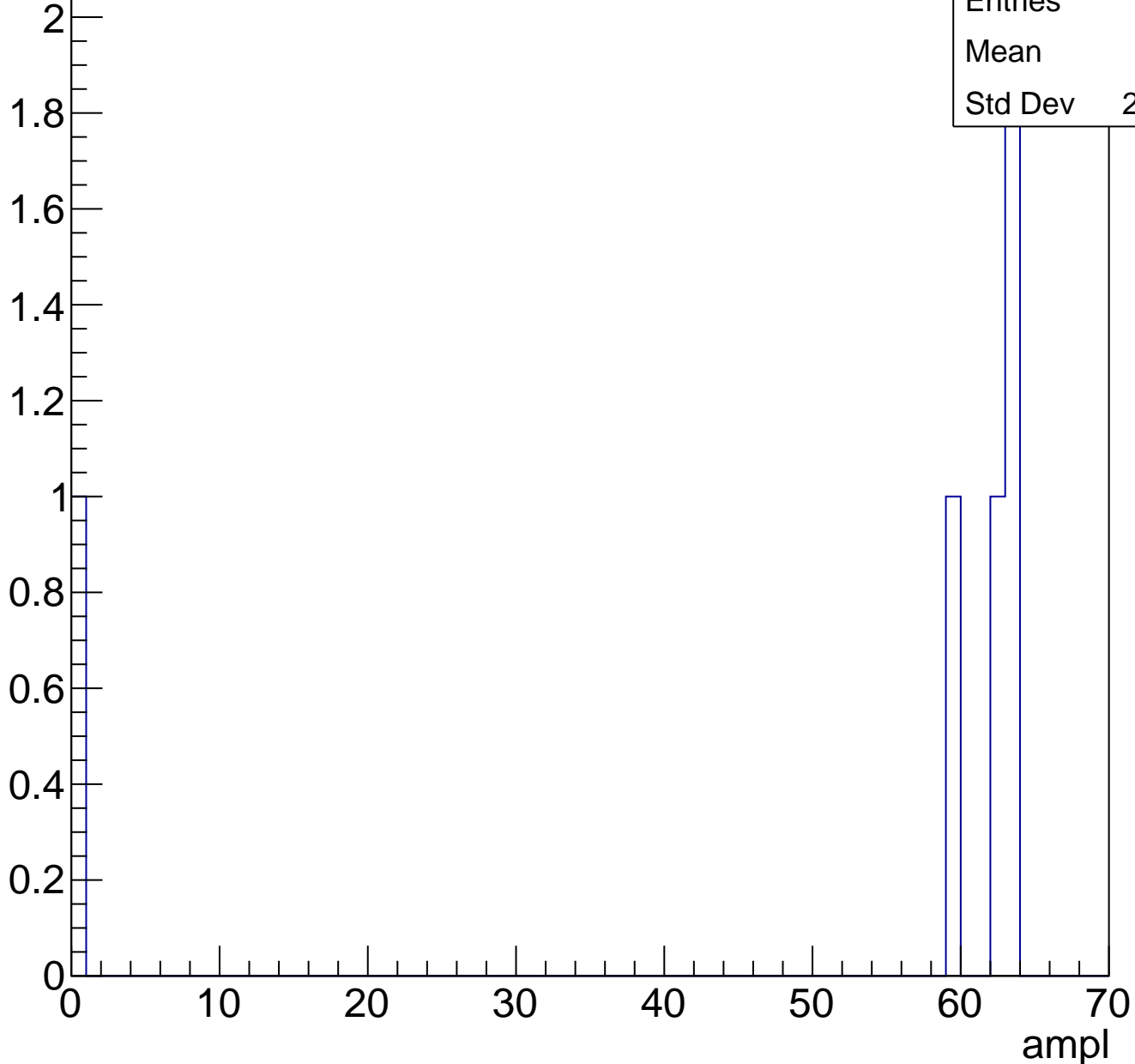
Entries	49
Mean	59.59
Std Dev	2.755



# B1L103S, U21-ch40, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U21-ch40, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

ampl

Entries

1

Mean

59

Std Dev

0

# B1L103S, U21-ch41, adc0

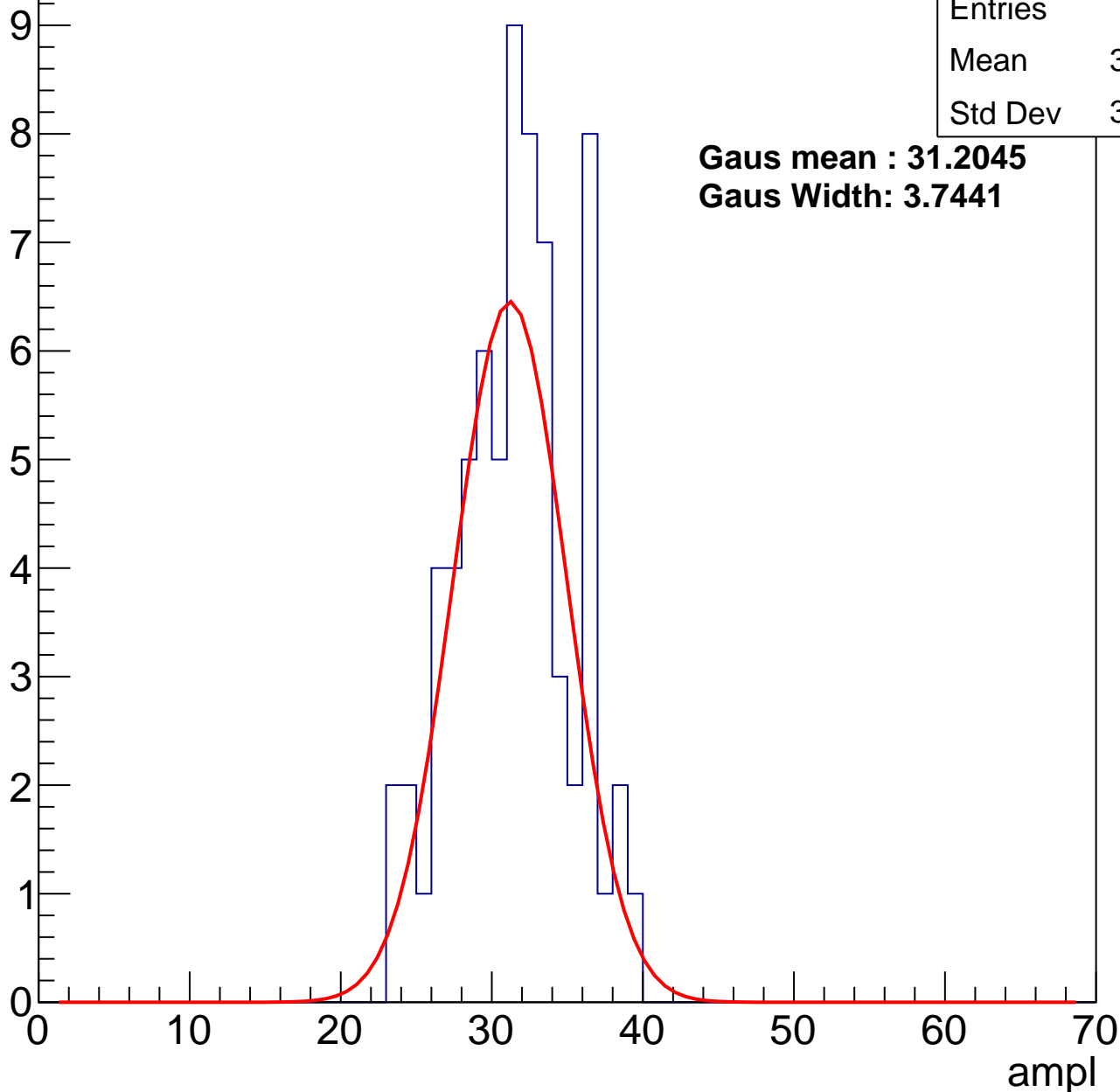
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	31.04
Std Dev	3.766

**Gaus mean : 31.2045**

**Gaus Width: 3.7441**



# B1L103S, U21-ch41, adc1

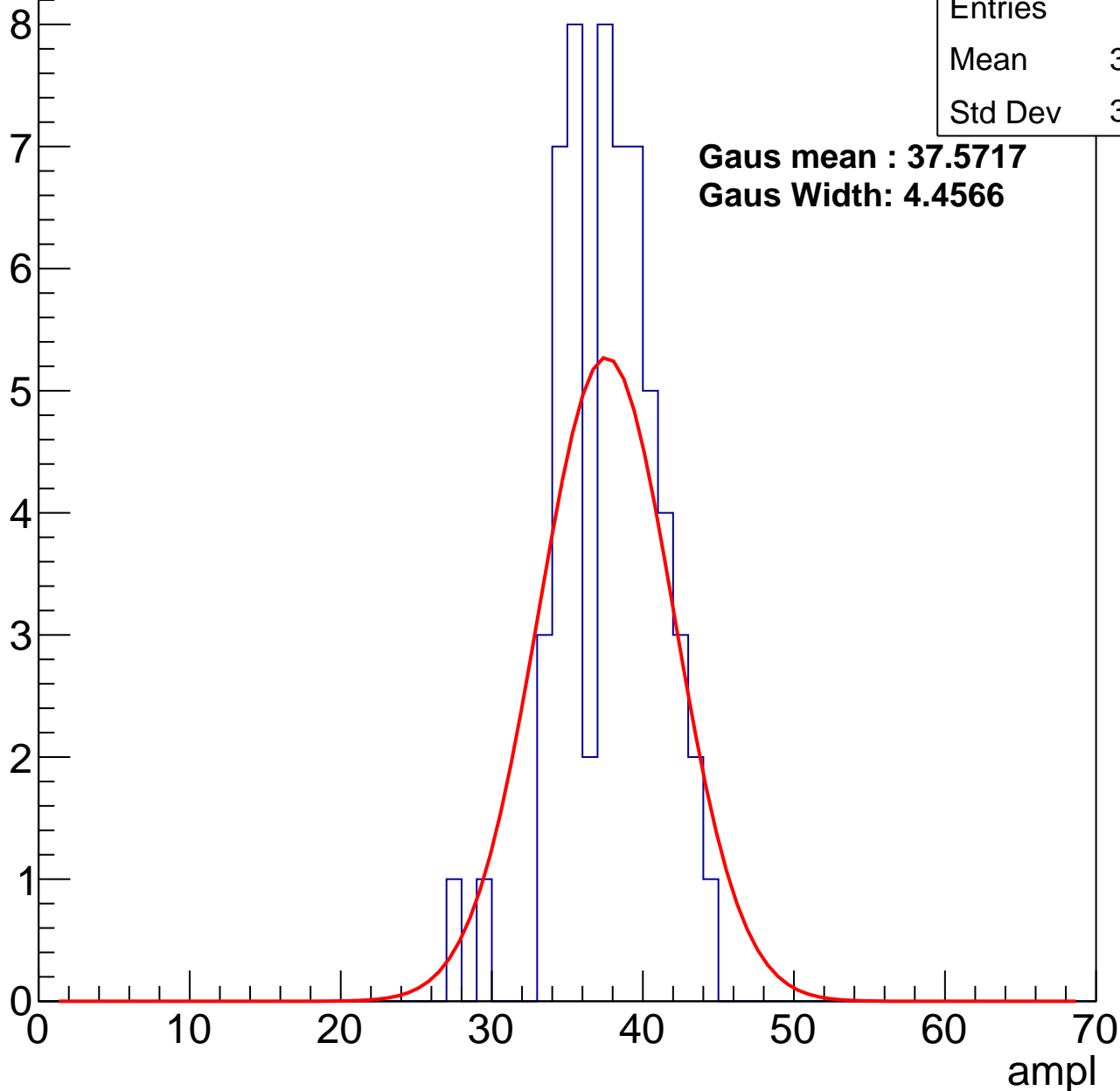
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	37.29
Std Dev	3.304

**Gaus mean : 37.5717**

**Gaus Width: 4.4566**



# B1L103S, U21-ch41, adc2

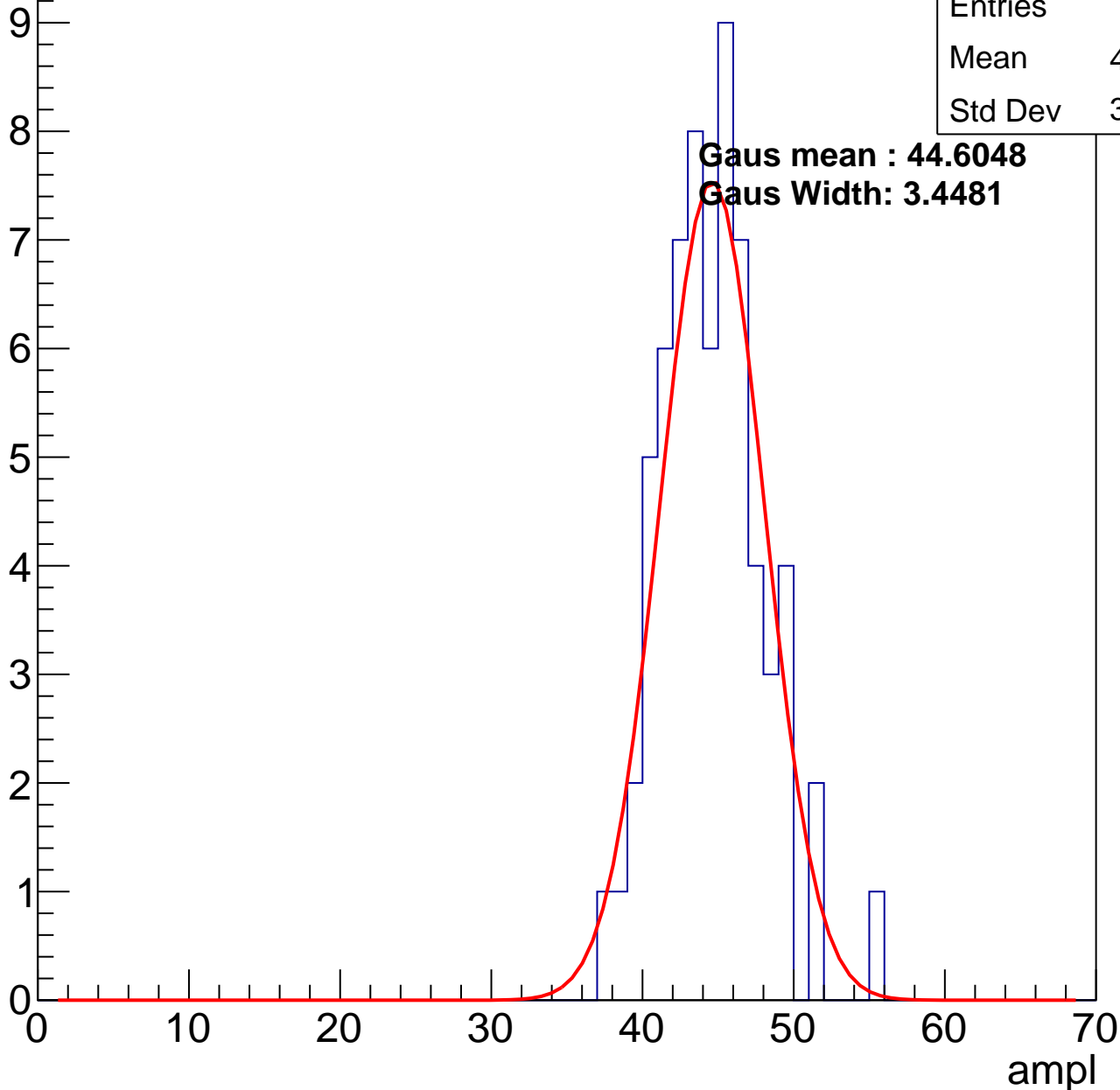
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	44.14
Std Dev	3.357

**Gaus mean : 44.6048**

**Gaus Width: 3.4481**

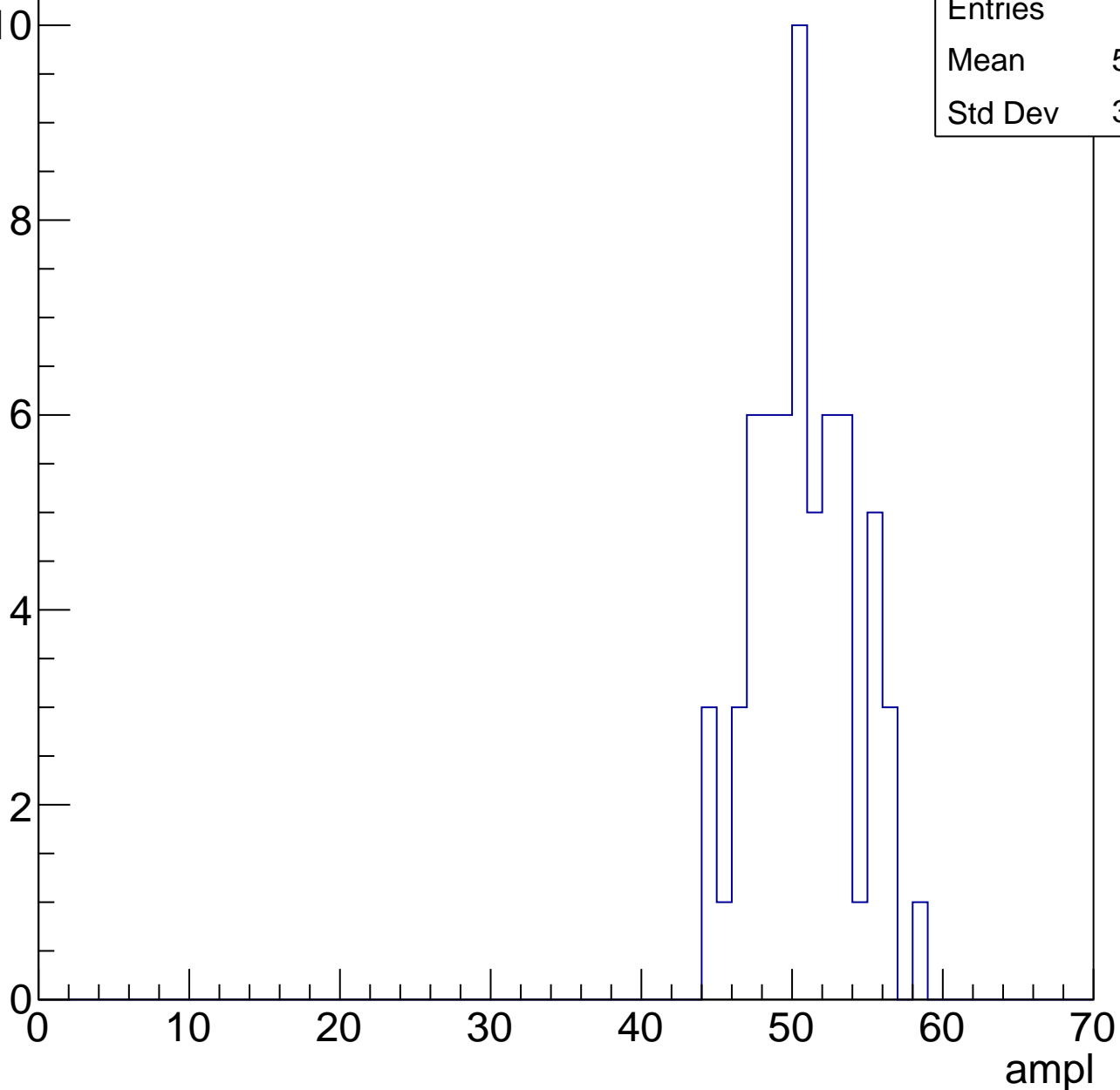


# B1L103S, U21-ch41, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	50.31
Std Dev	3.251

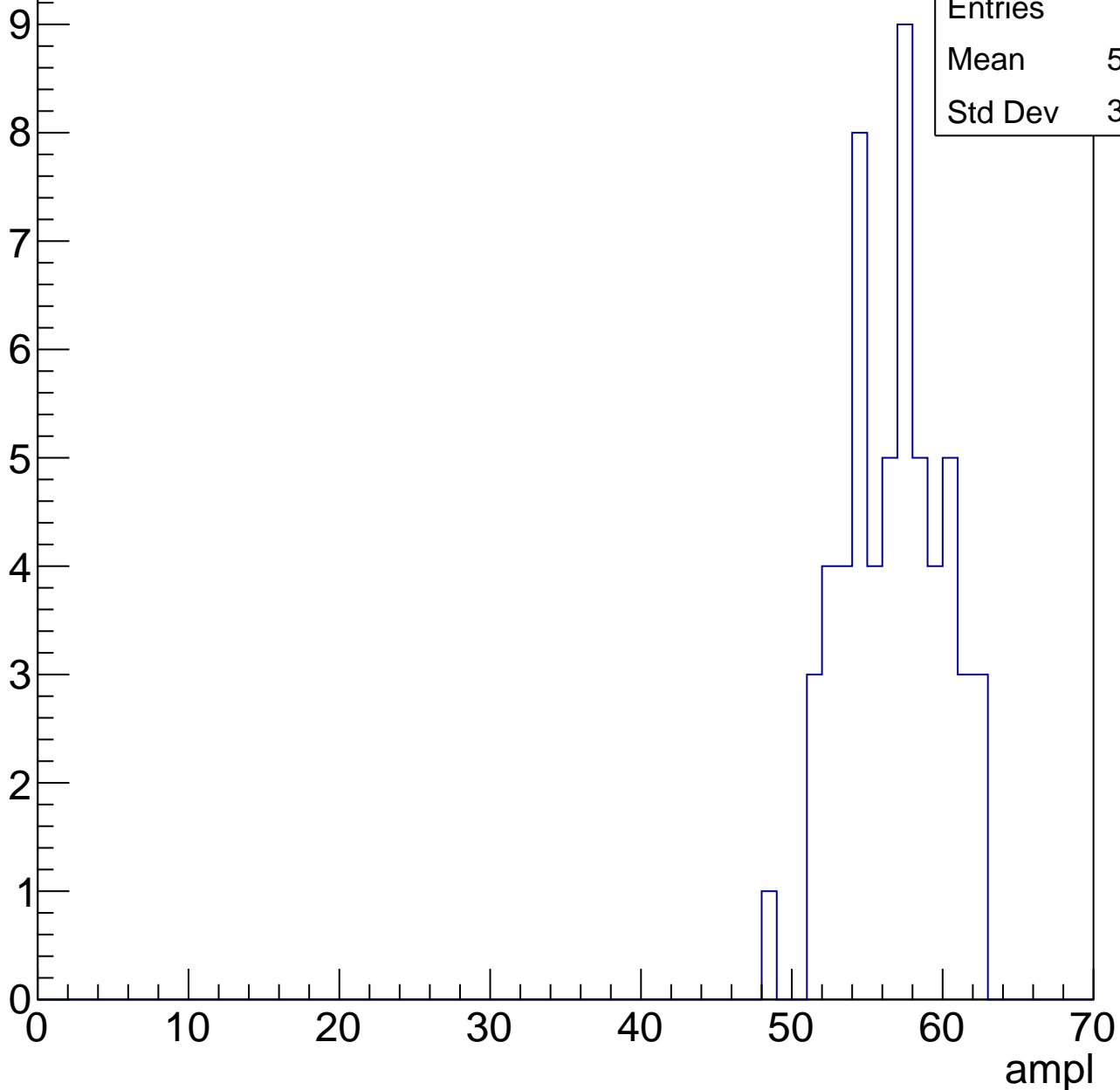


# B1L103S, U21-ch41, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	56.22
Std Dev	3.217

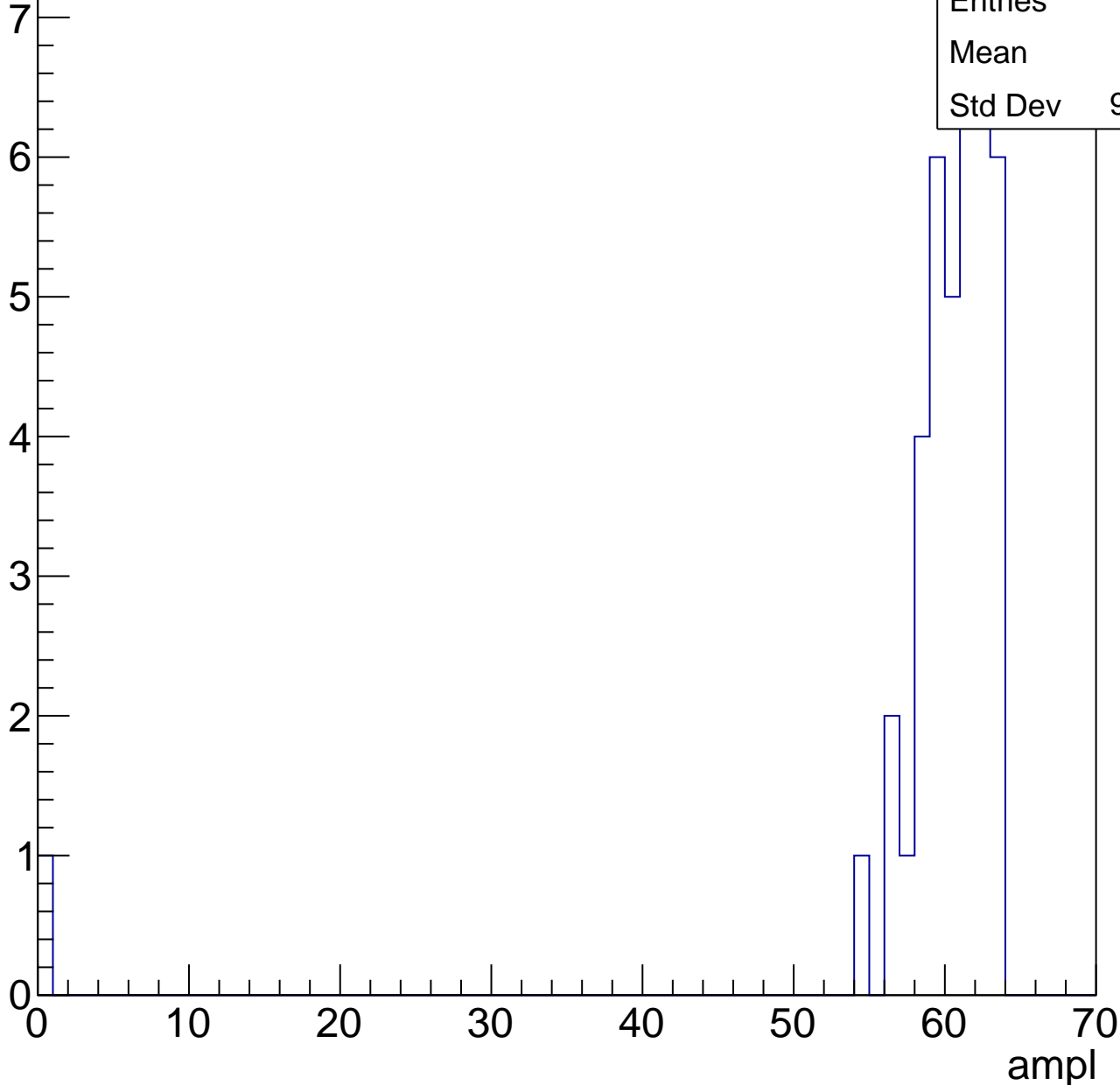


# B1L103S, U21-ch41, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	40
Mean	58.7
Std Dev	9.644



# B1L103S, U21-ch41, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

4  
3.5  
3  
2.5  
2  
1.5  
1  
0.5  
0

0

10

20

30

40

50

60

70

ampl

Entries

4

Mean

63

Std Dev

0



# B1L103S, U21-ch41, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U21-ch42, adc0

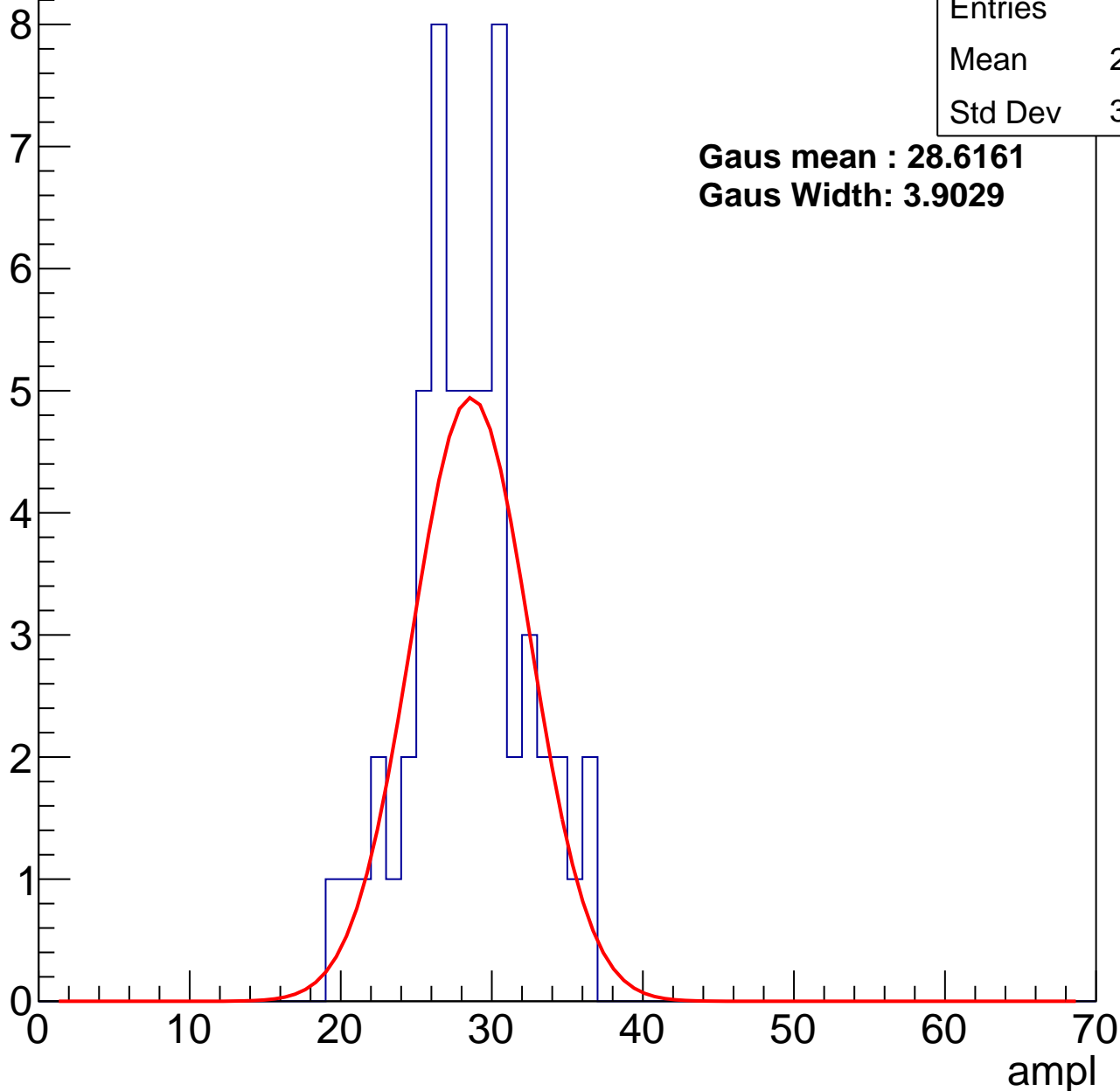
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	27.98
Std Dev	3.796

**Gaus mean : 28.6161**

**Gaus Width: 3.9029**



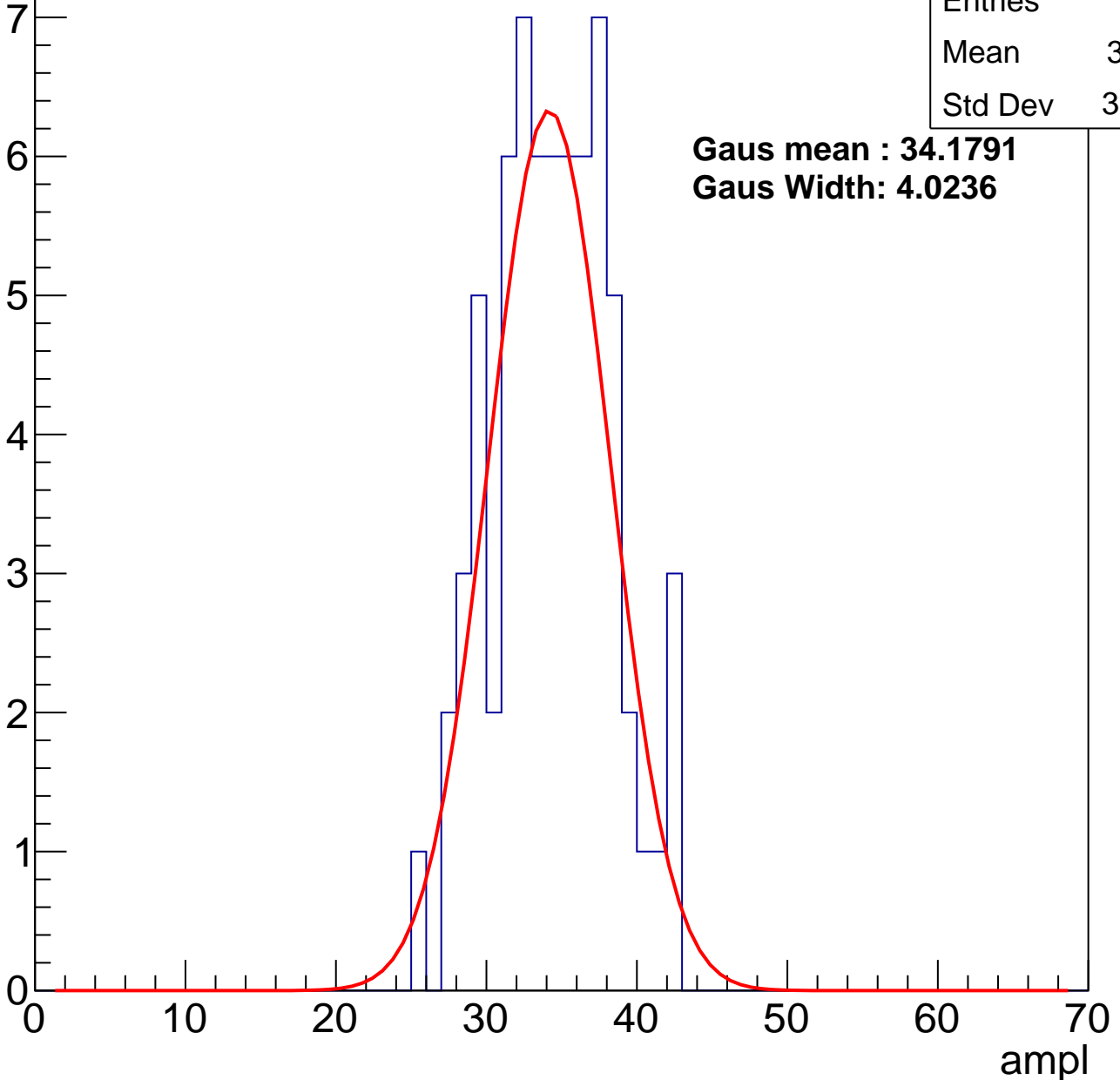
# B1L103S, U21-ch42, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	33.91
Std Dev	3.866

**Gaus mean : 34.1791**  
**Gaus Width: 4.0236**



# B1L103S, U21-ch42, adc2

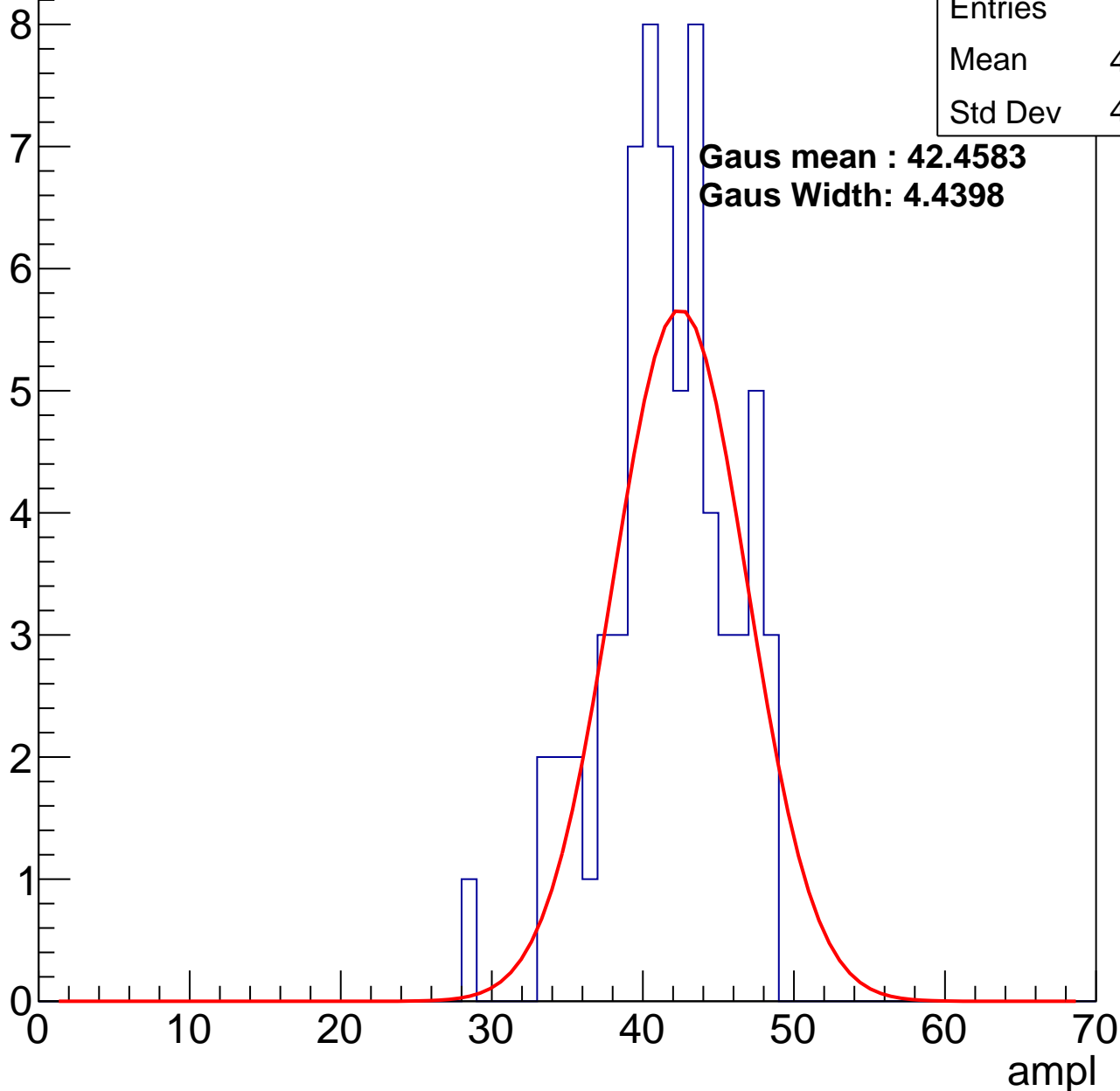
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	41.12
Std Dev	4.098

**Gaus mean : 42.4583**

**Gaus Width: 4.4398**



# B1L103S, U21-ch42, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	67
Mean	46.72
Std Dev	4.245

Entry

10

8

6

4

2

0

0

10

20

30

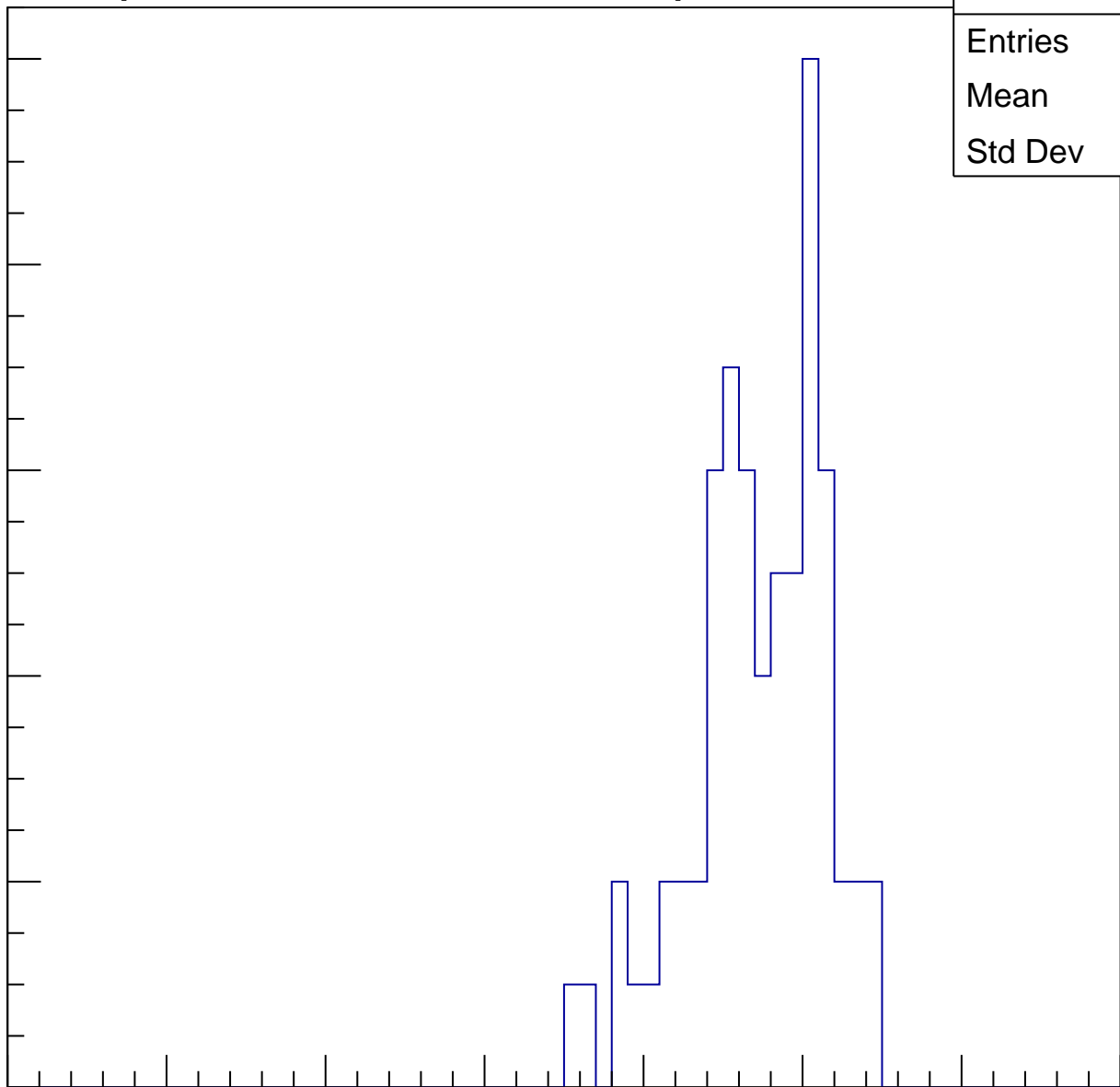
40

50

60

70

ampl

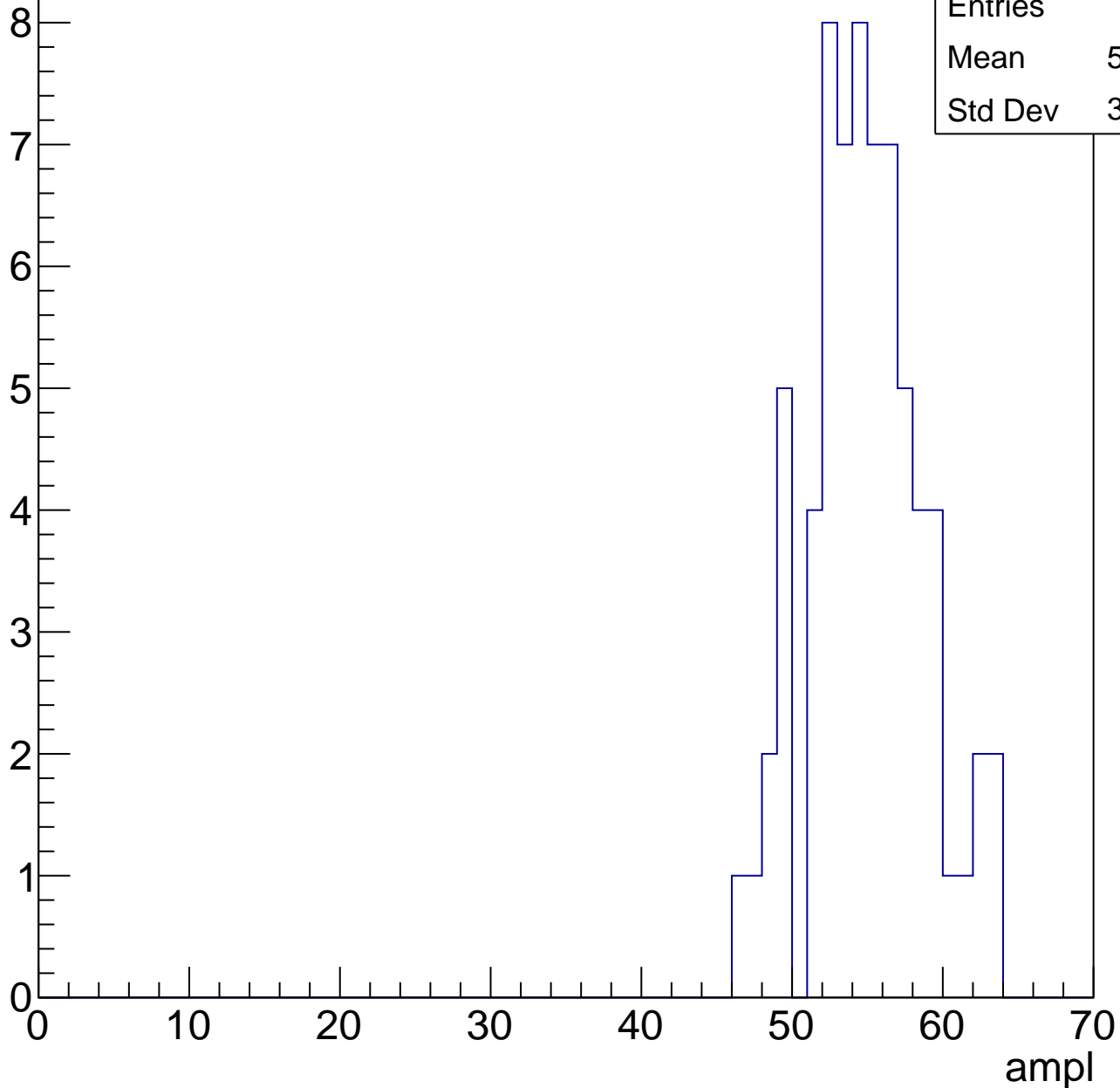


# B1L103S, U21-ch42, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	54.46
Std Dev	3.786

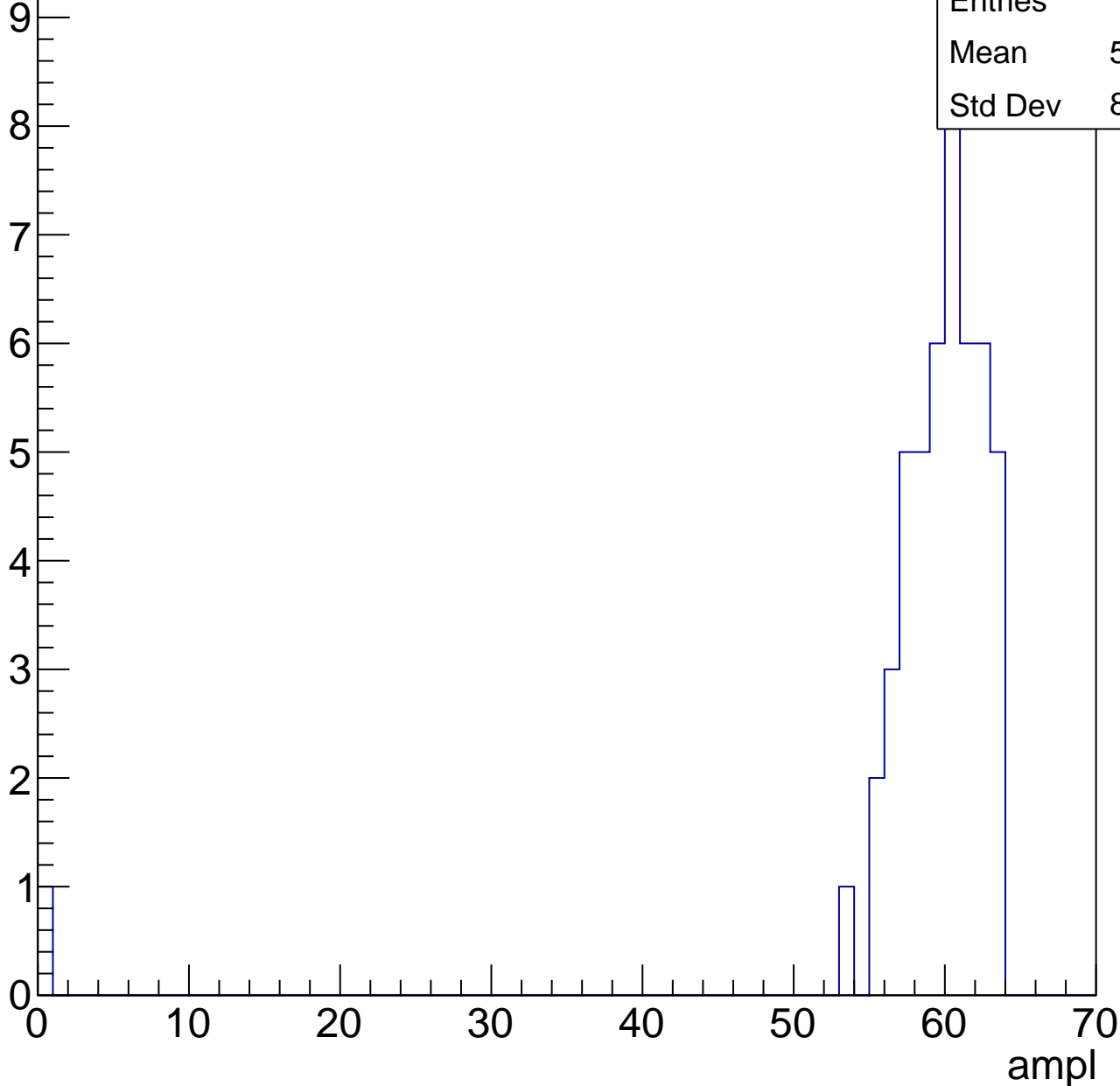


# B1L103S, U21-ch42, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

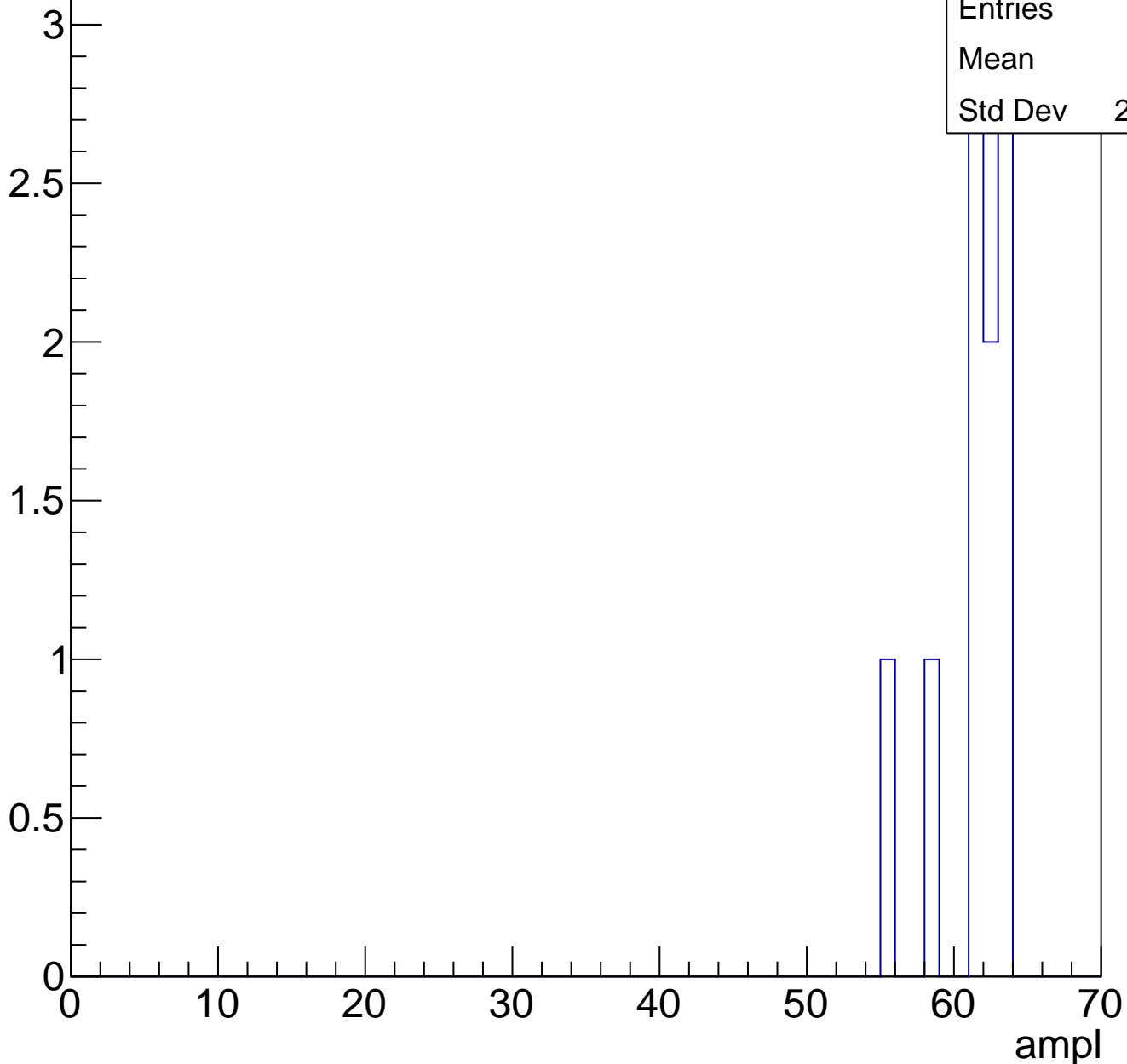
Entries	49
Mean	58.22
Std Dev	8.735



# B1L103S, U21-ch42, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U21-ch42, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U21-ch43, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	82
Mean	30.37
Std Dev	4.825

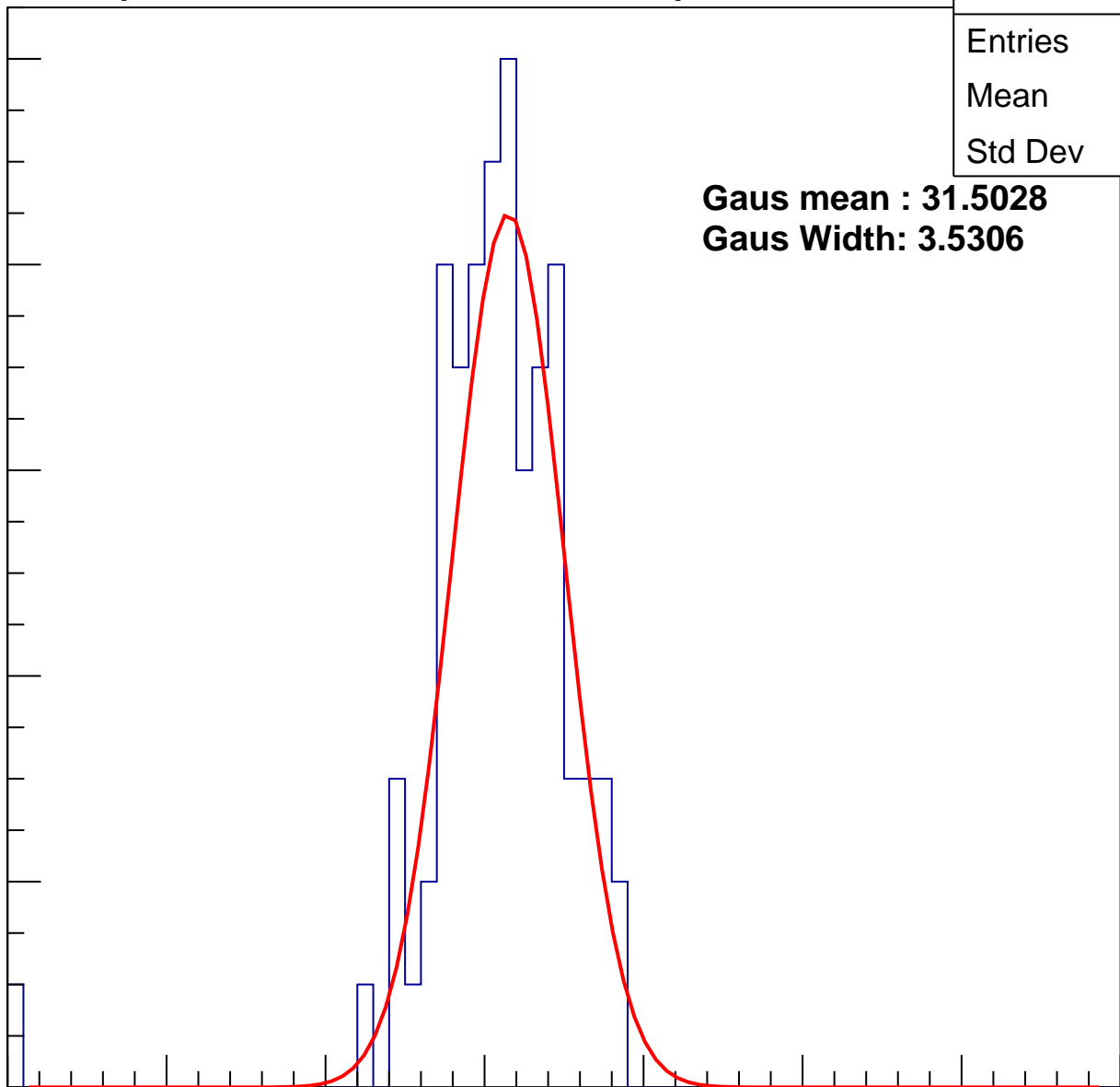
**Gaus mean : 31.5028**

**Gaus Width: 3.5306**

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U21-ch43, adc1

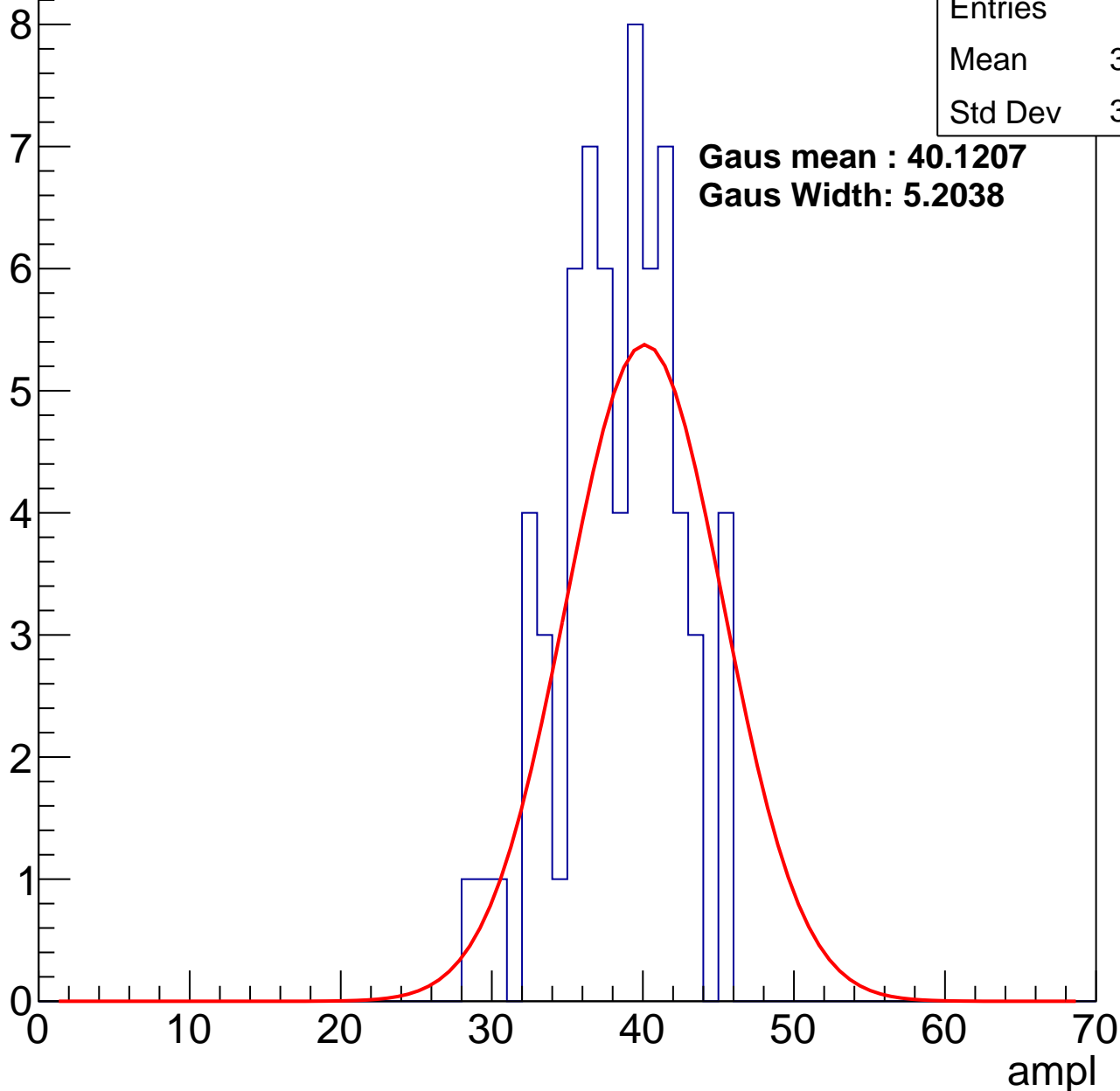
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	37.88
Std Dev	3.887

**Gaus mean : 40.1207**

**Gaus Width: 5.2038**



# B1L103S, U21-ch43, adc2

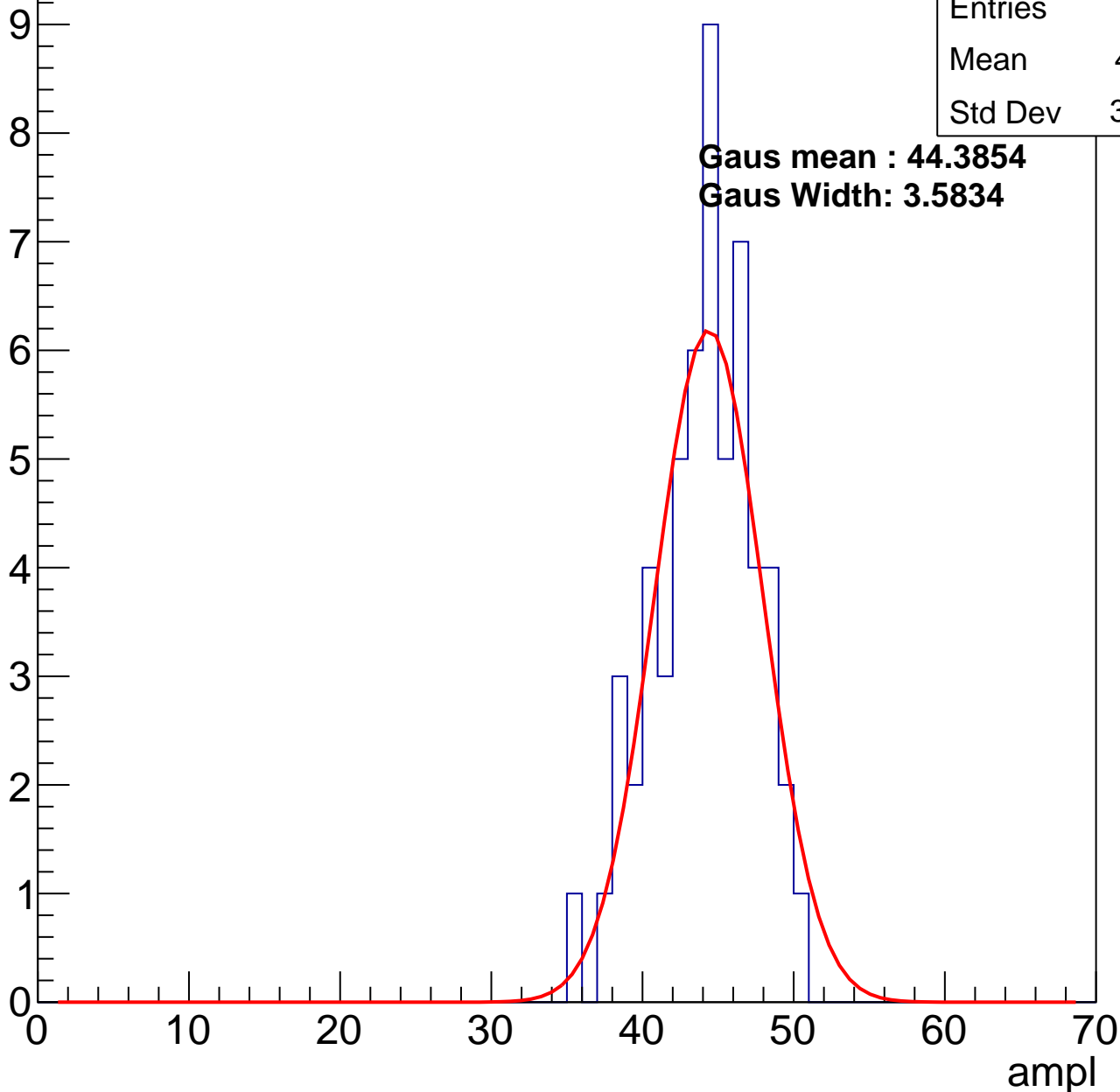
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	43.61
Std Dev	3.286

**Gaus mean : 44.3854**

**Gaus Width: 3.5834**

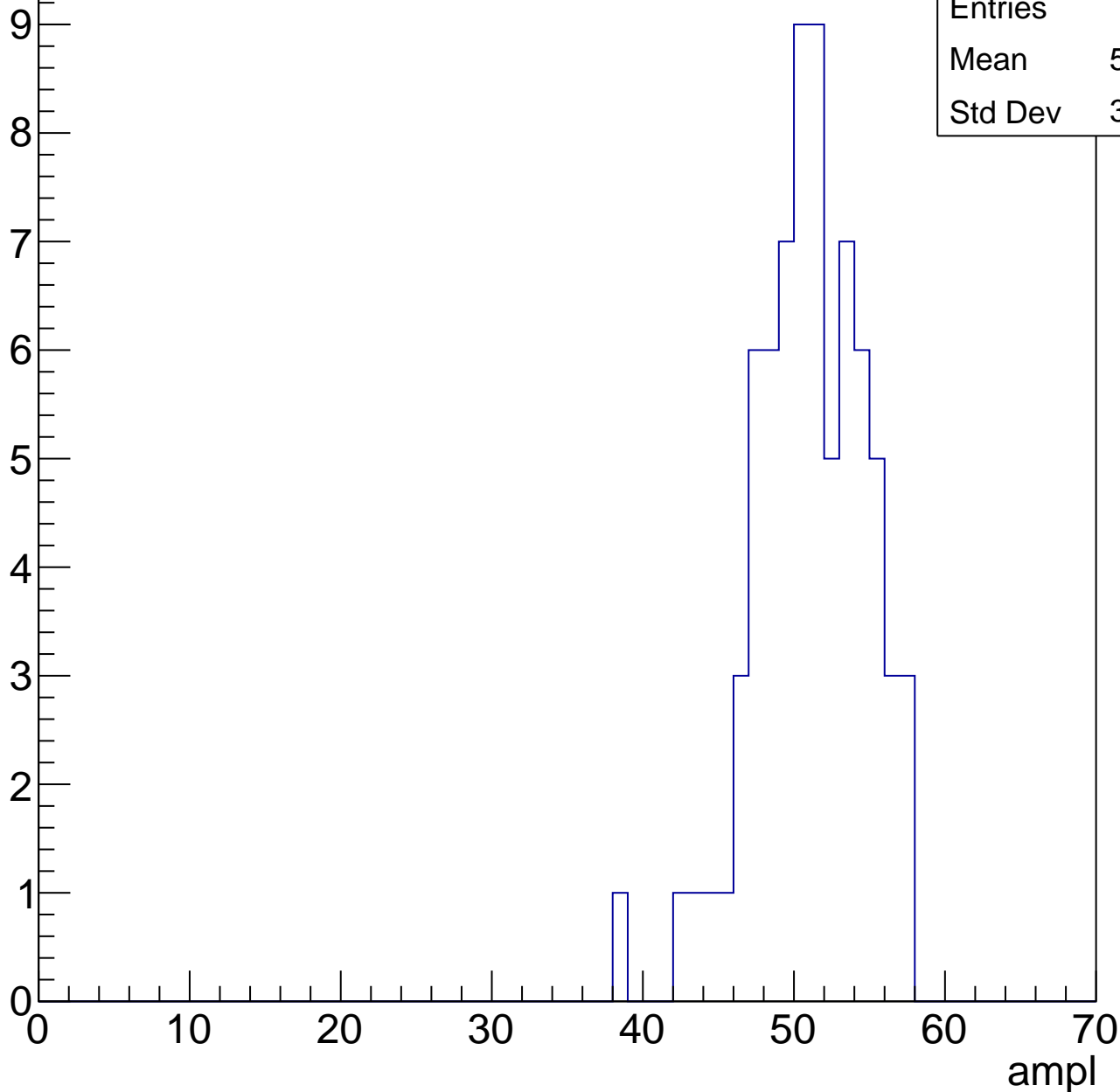


# B1L103S, U21-ch43, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	50.55
Std Dev	3.669

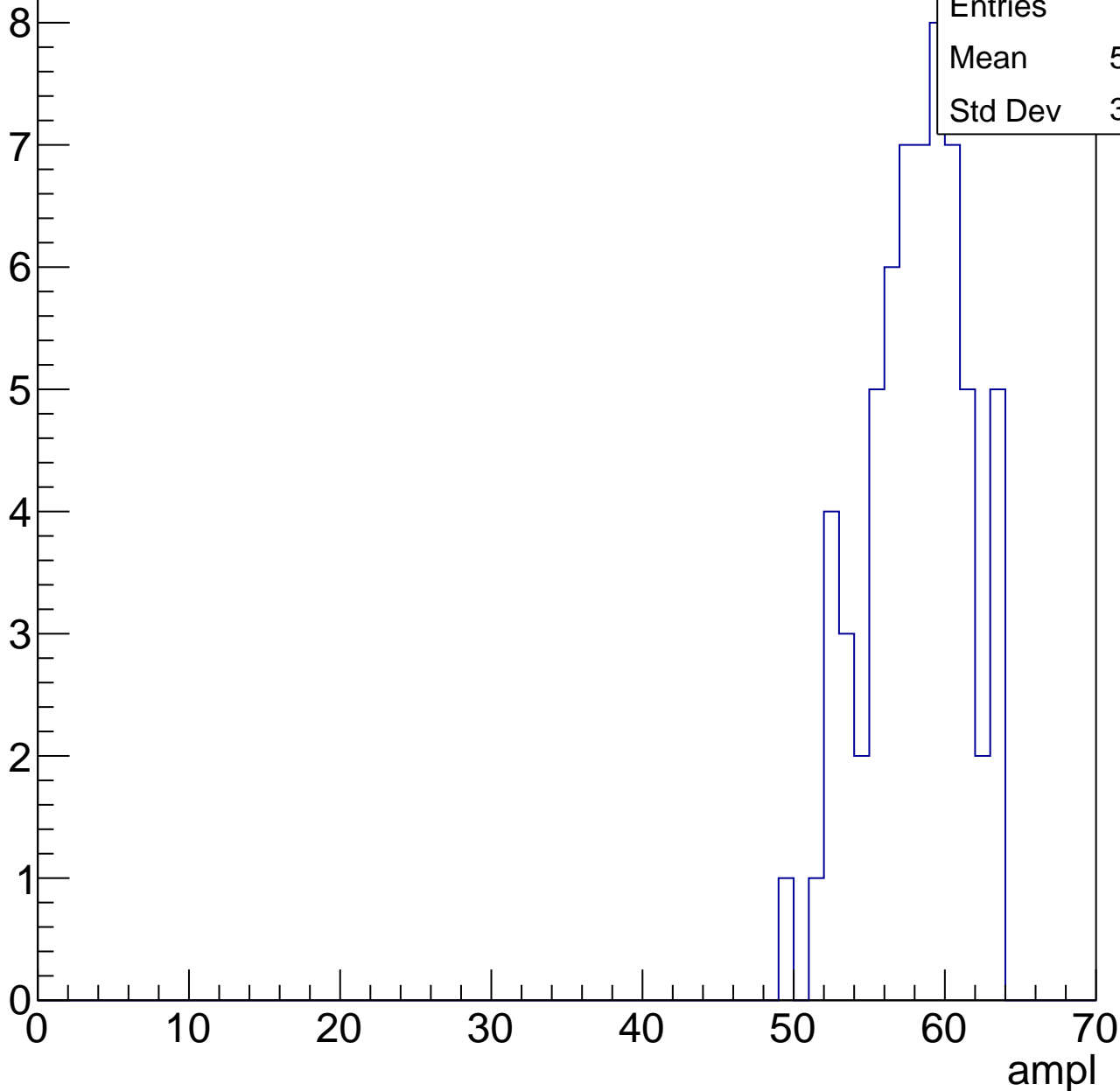


# B1L103S, U21-ch43, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	57.57
Std Dev	3.294

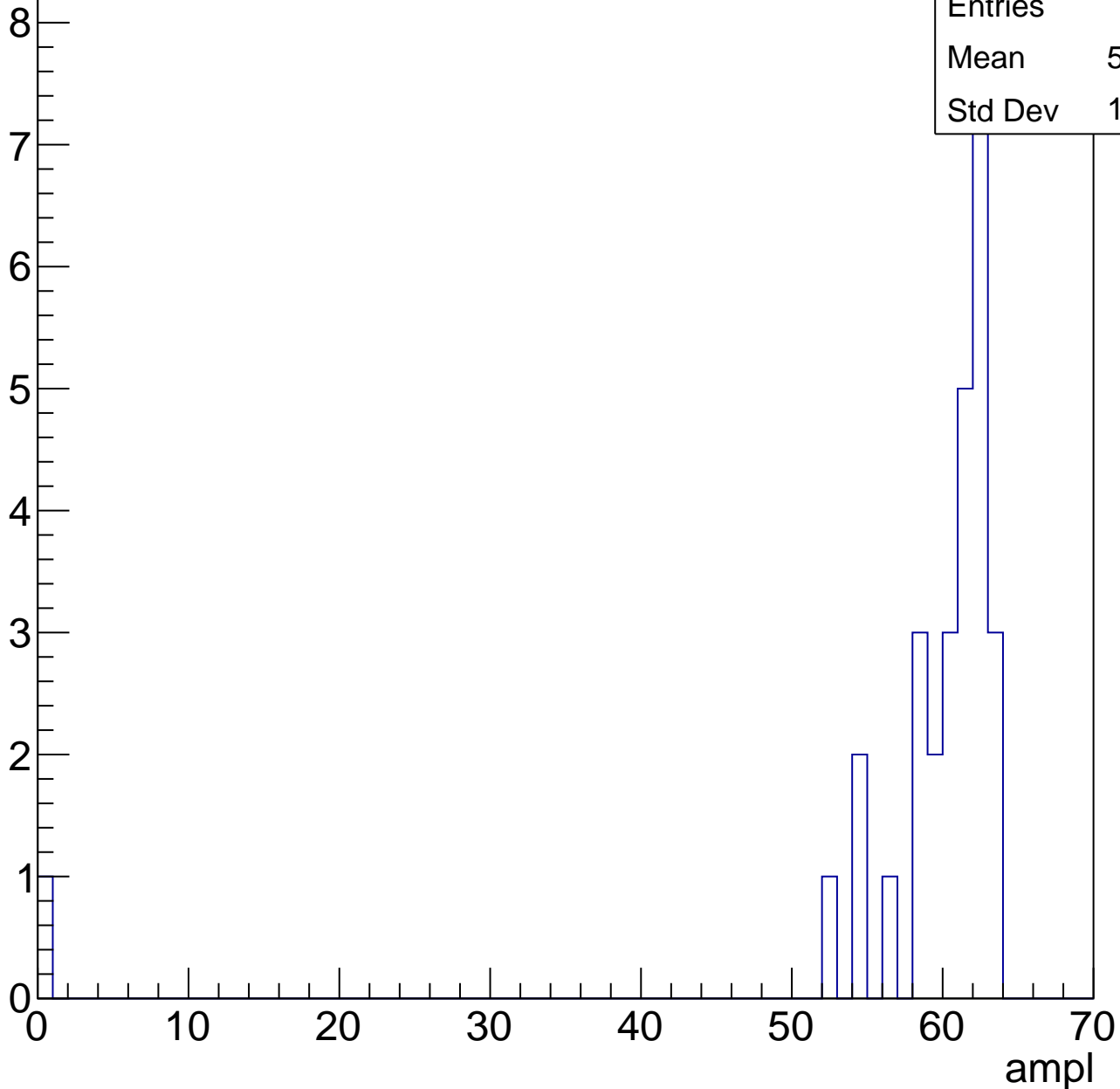


# B1L103S, U21-ch43, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	29
Mean	57.86
Std Dev	11.29



# B1L103S, U21-ch43, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	63
Std Dev	0

ampl



# B1L103S, U21-ch43, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U21-ch44, adc0

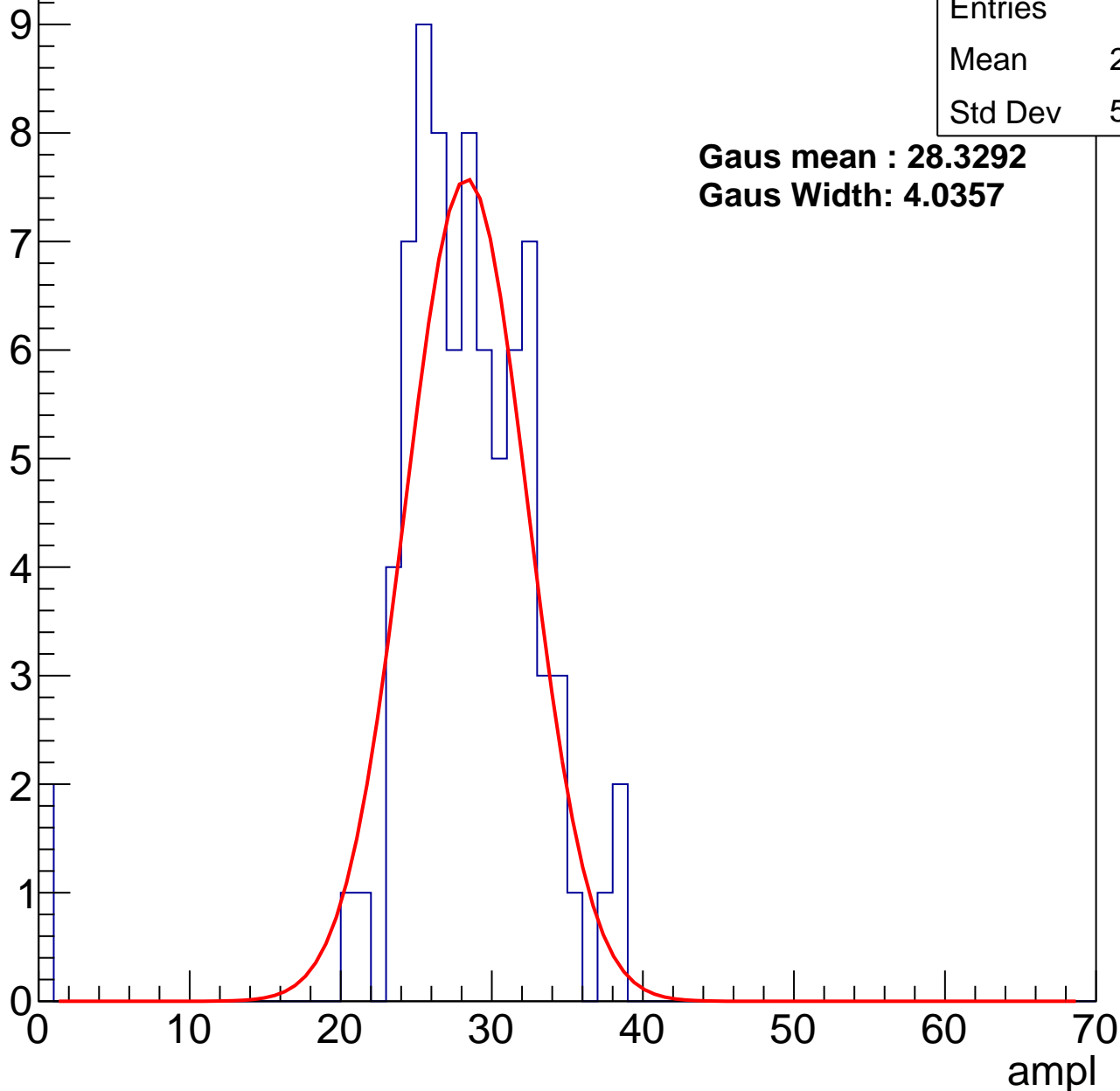
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	80
Mean	27.54
Std Dev	5.809

**Gaus mean : 28.3292**

**Gaus Width: 4.0357**



# B1L103S, U21-ch44, adc1

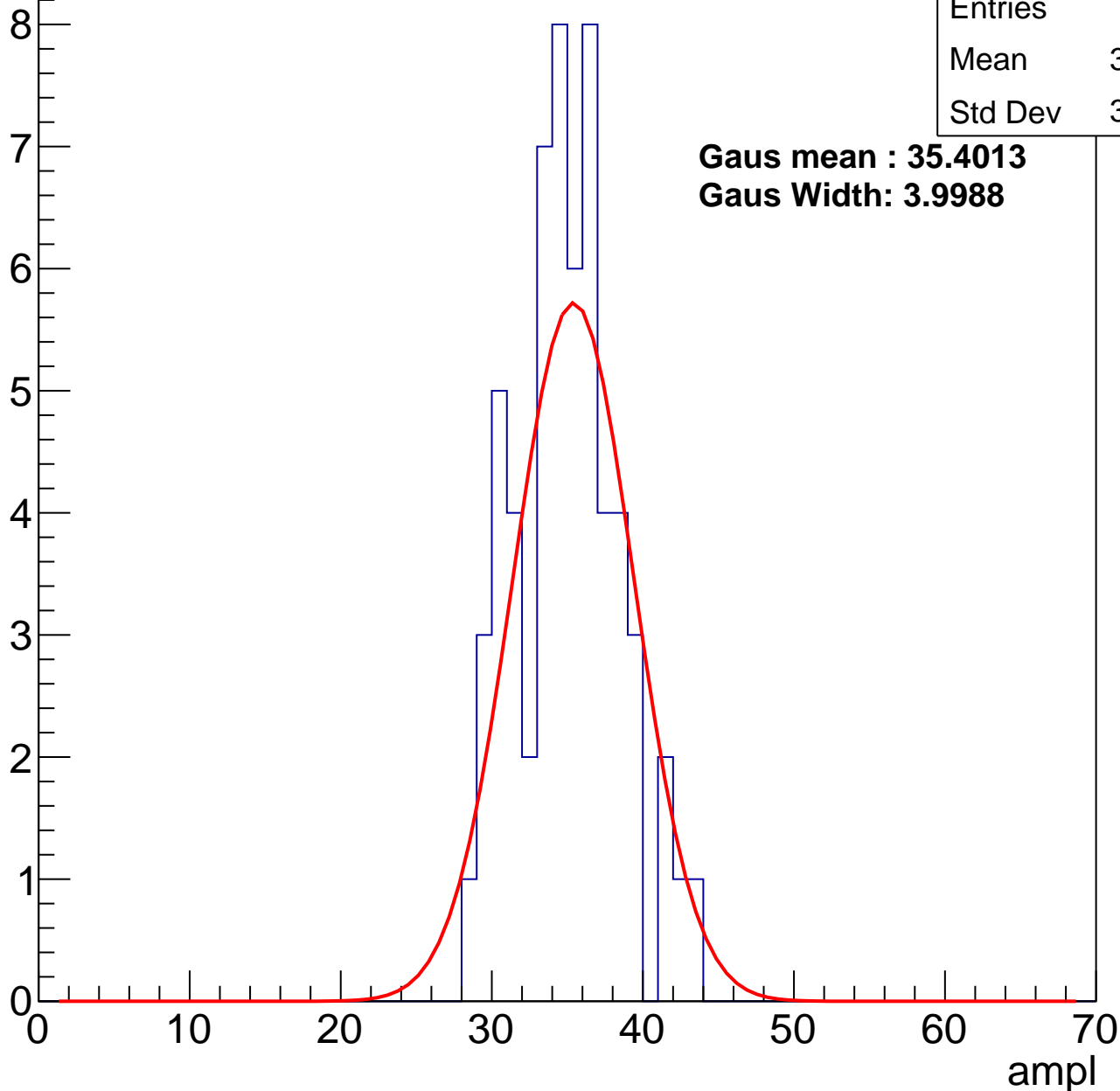
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	34.54
Std Dev	3.397

**Gaus mean : 35.4013**

**Gaus Width: 3.9988**



# B1L103S, U21-ch44, adc2

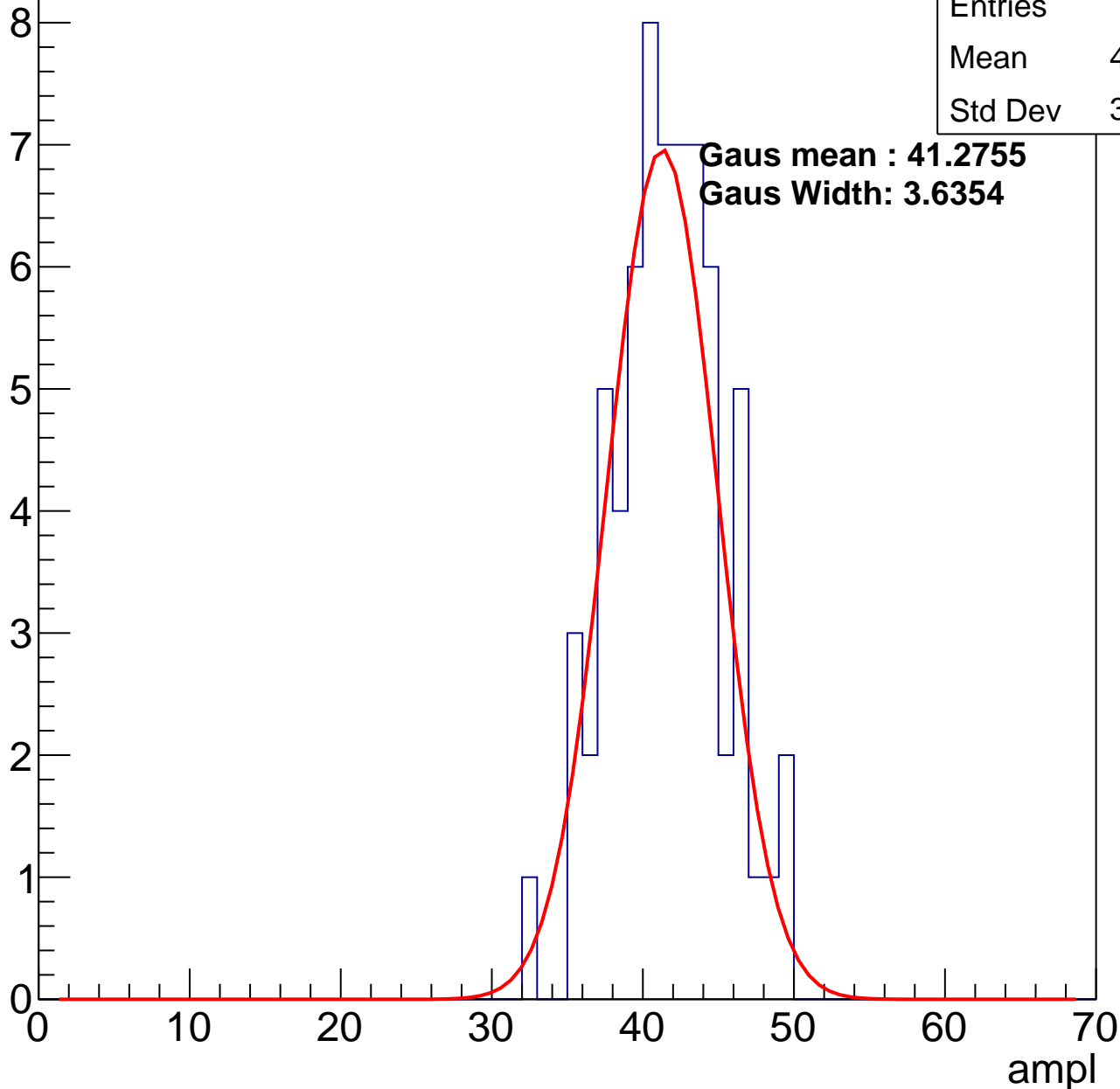
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	41.18
Std Dev	3.549

**Gaus mean : 41.2755**

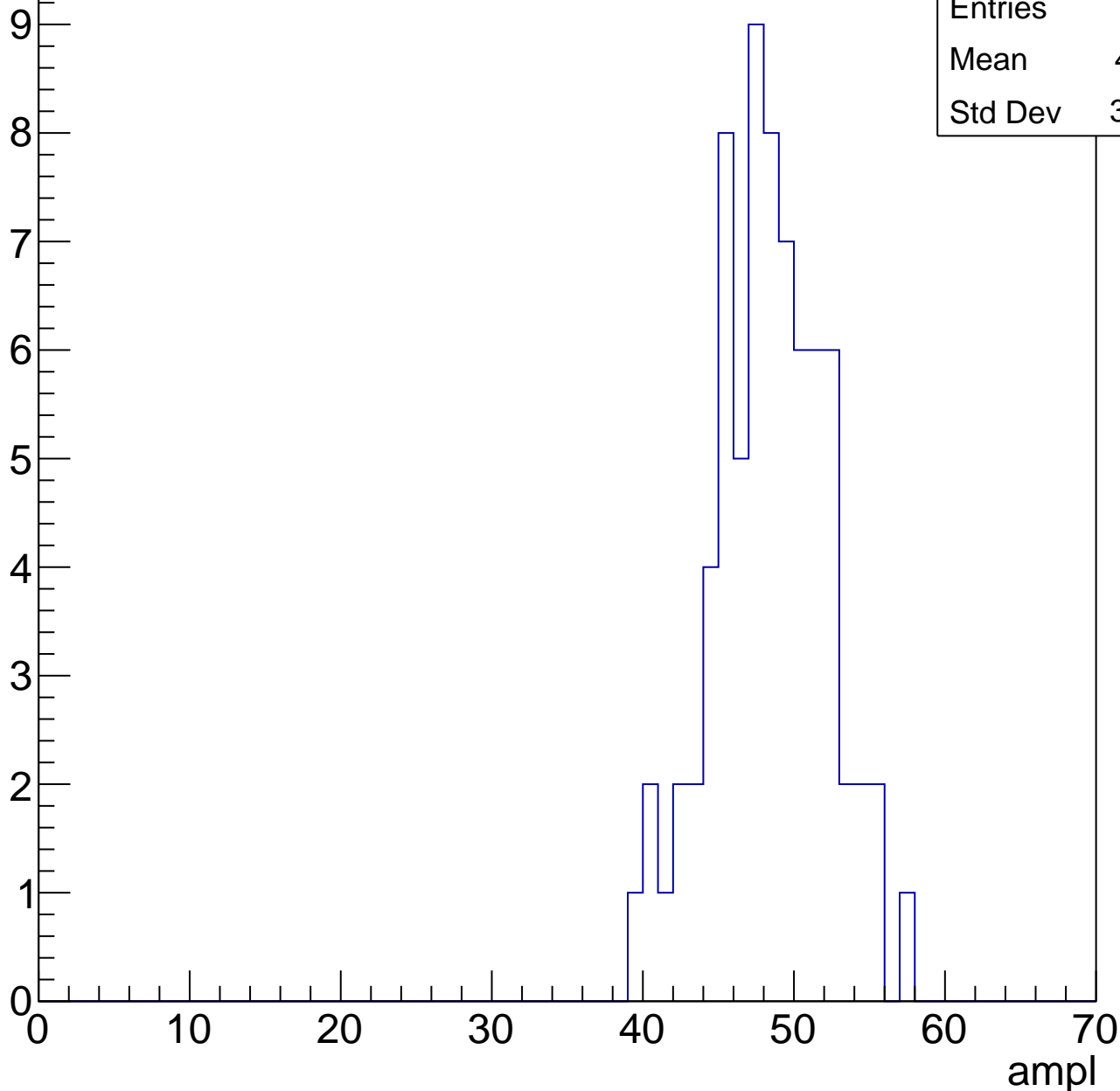
**Gaus Width: 3.6354**



# B1L103S, U21-ch44, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

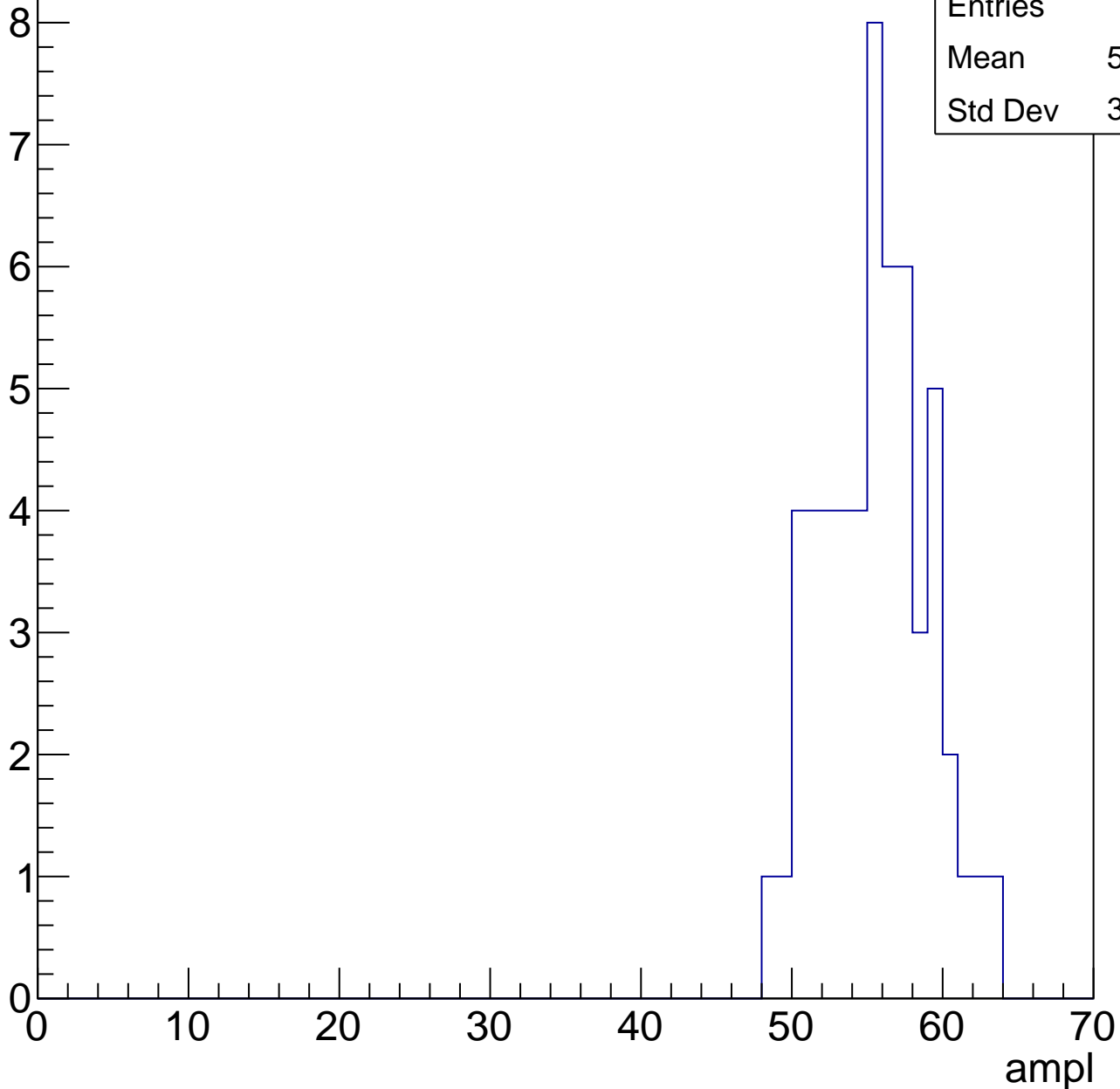


# B1L103S, U21-ch44, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	55.09
Std Dev	3.413

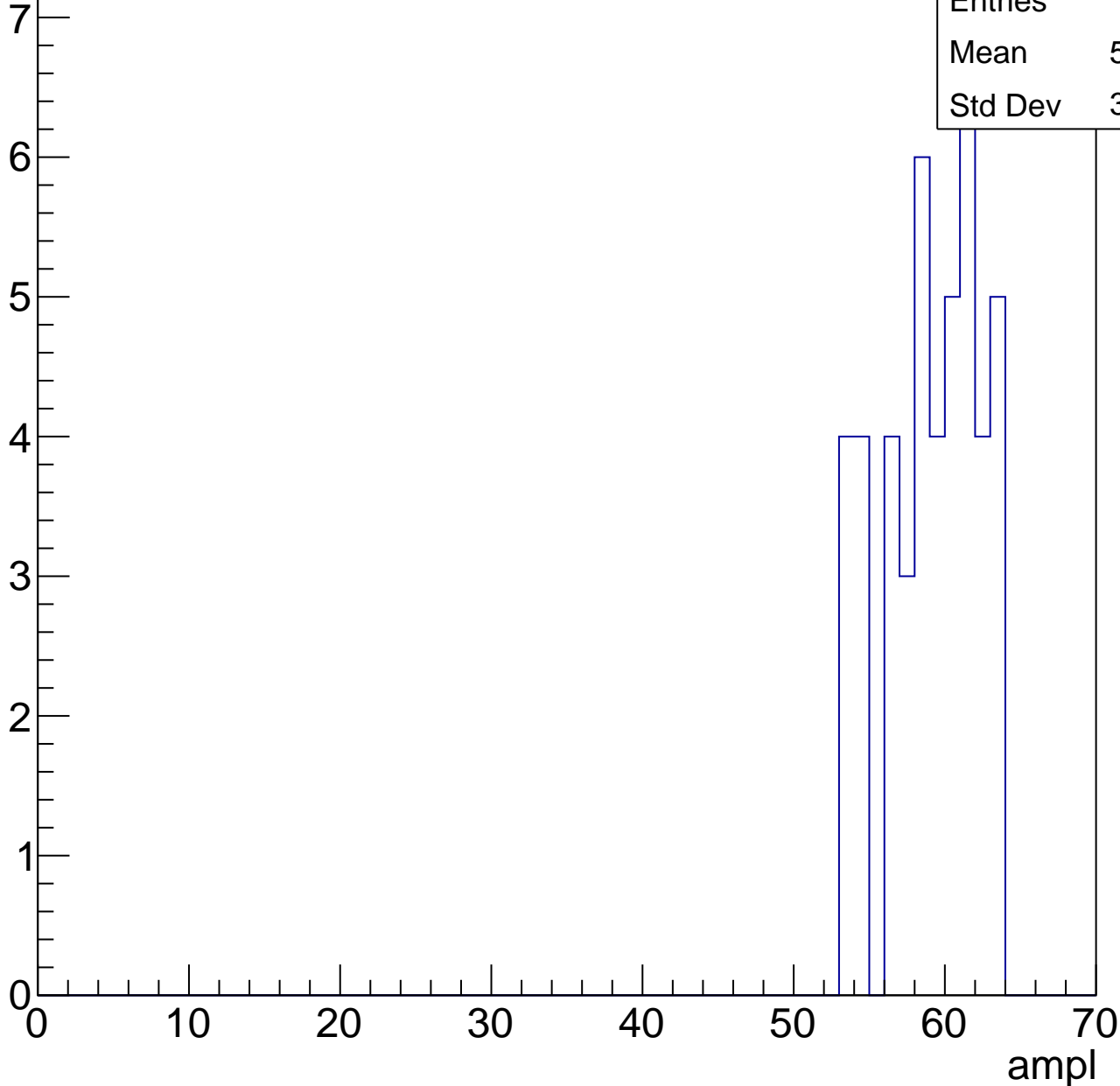


# B1L103S, U21-ch44, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	46
Mean	58.63
Std Dev	3.095

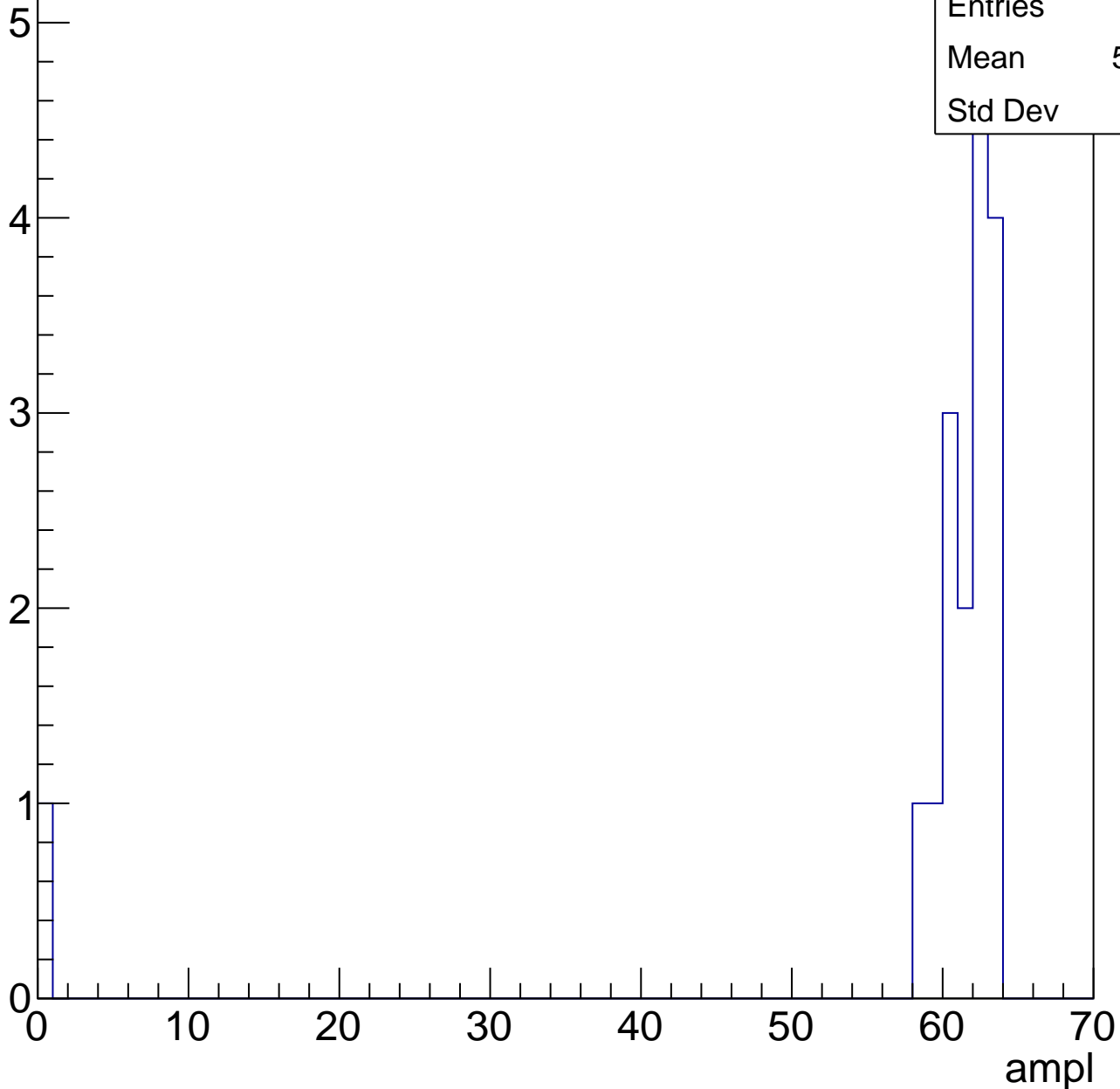


# B1L103S, U21-ch44, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	17
Mean	57.71
Std Dev	14.5





# B1L103S, U21-ch44, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U21-ch45, adc0

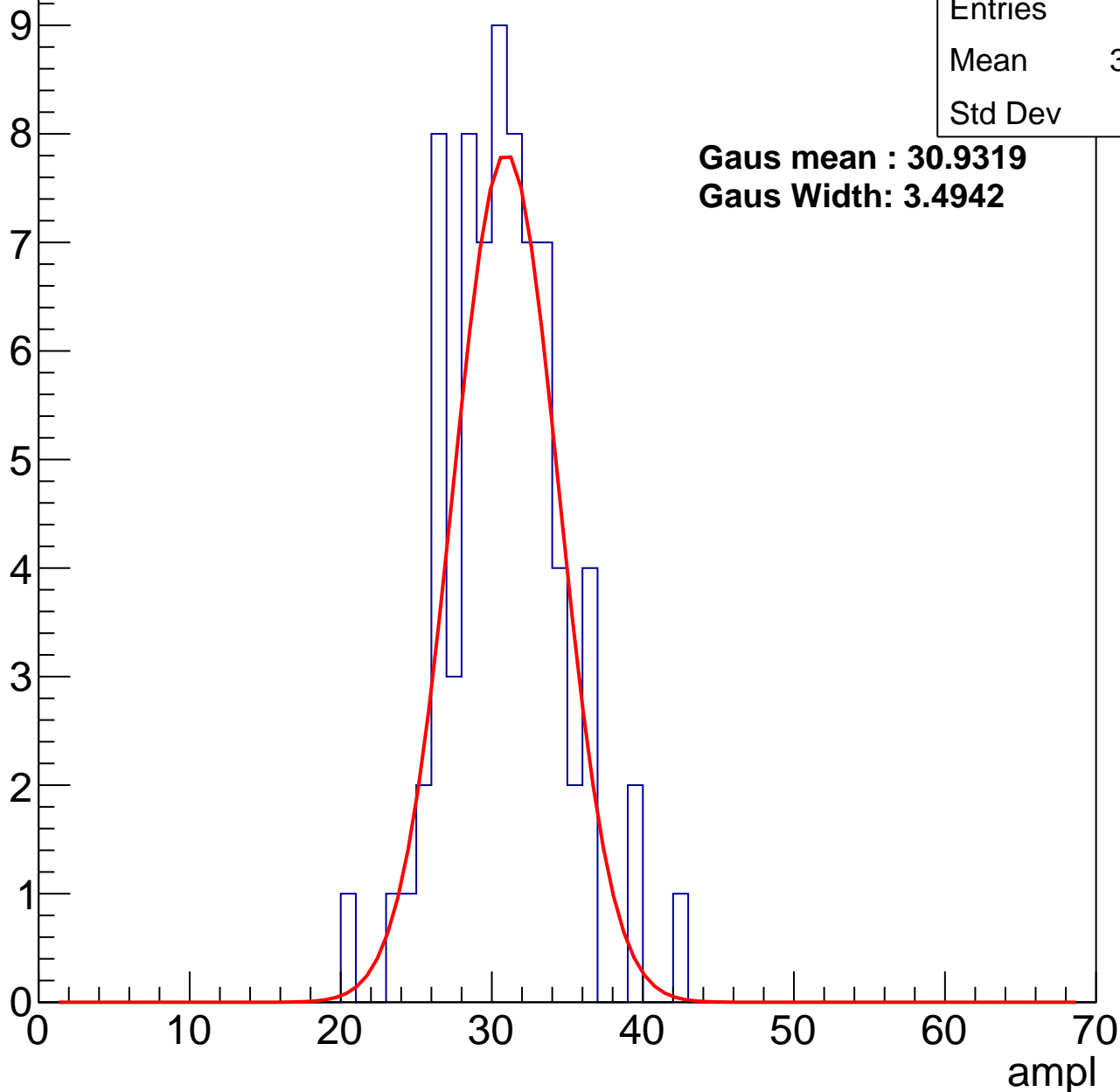
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	30.35
Std Dev	3.8

**Gaus mean : 30.9319**

**Gaus Width: 3.4942**



# B1L103S, U21-ch45, adc1

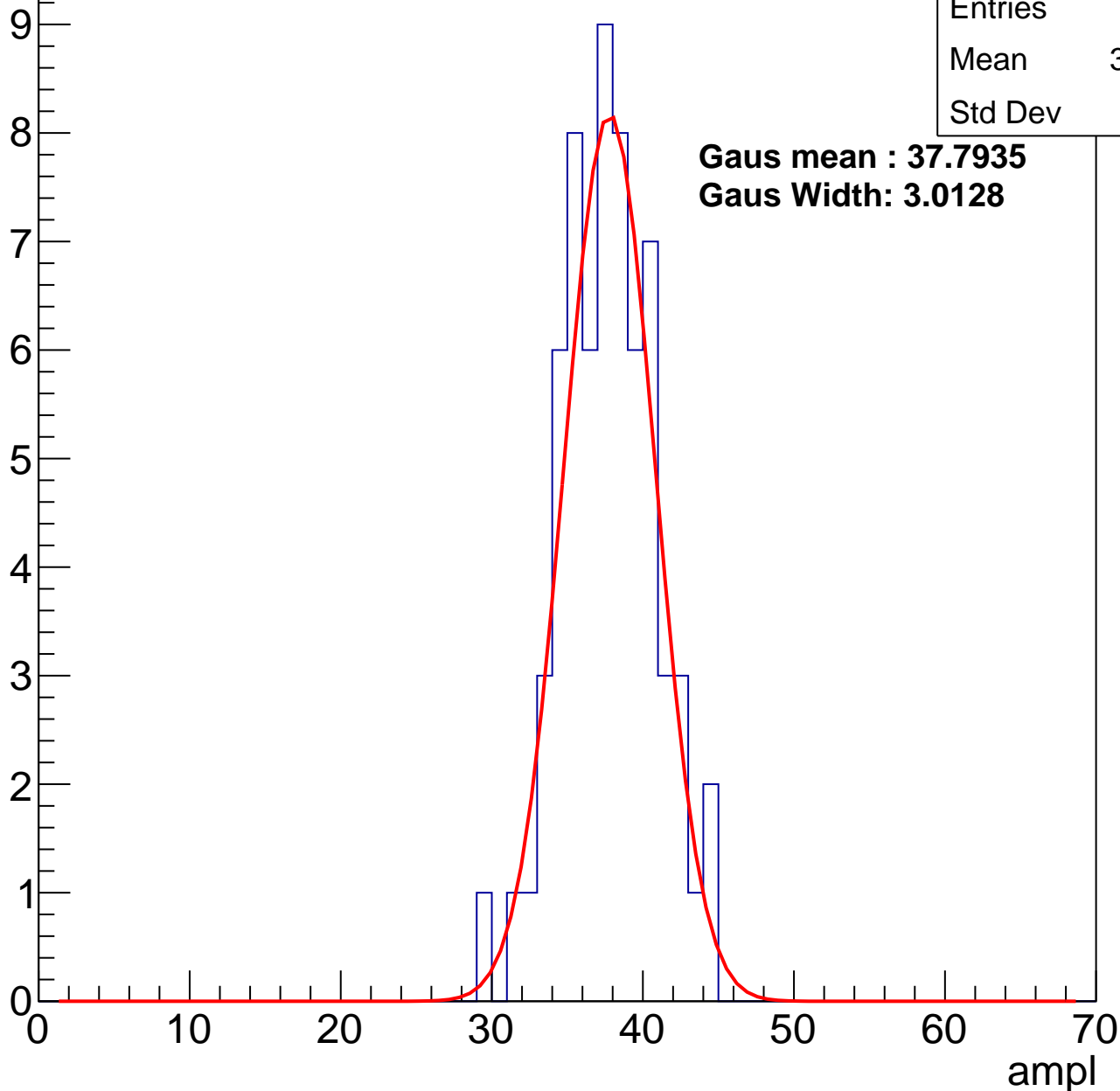
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	37.26
Std Dev	3.07

**Gaus mean : 37.7935**

**Gaus Width: 3.0128**



# B1L103S, U21-ch45, adc2

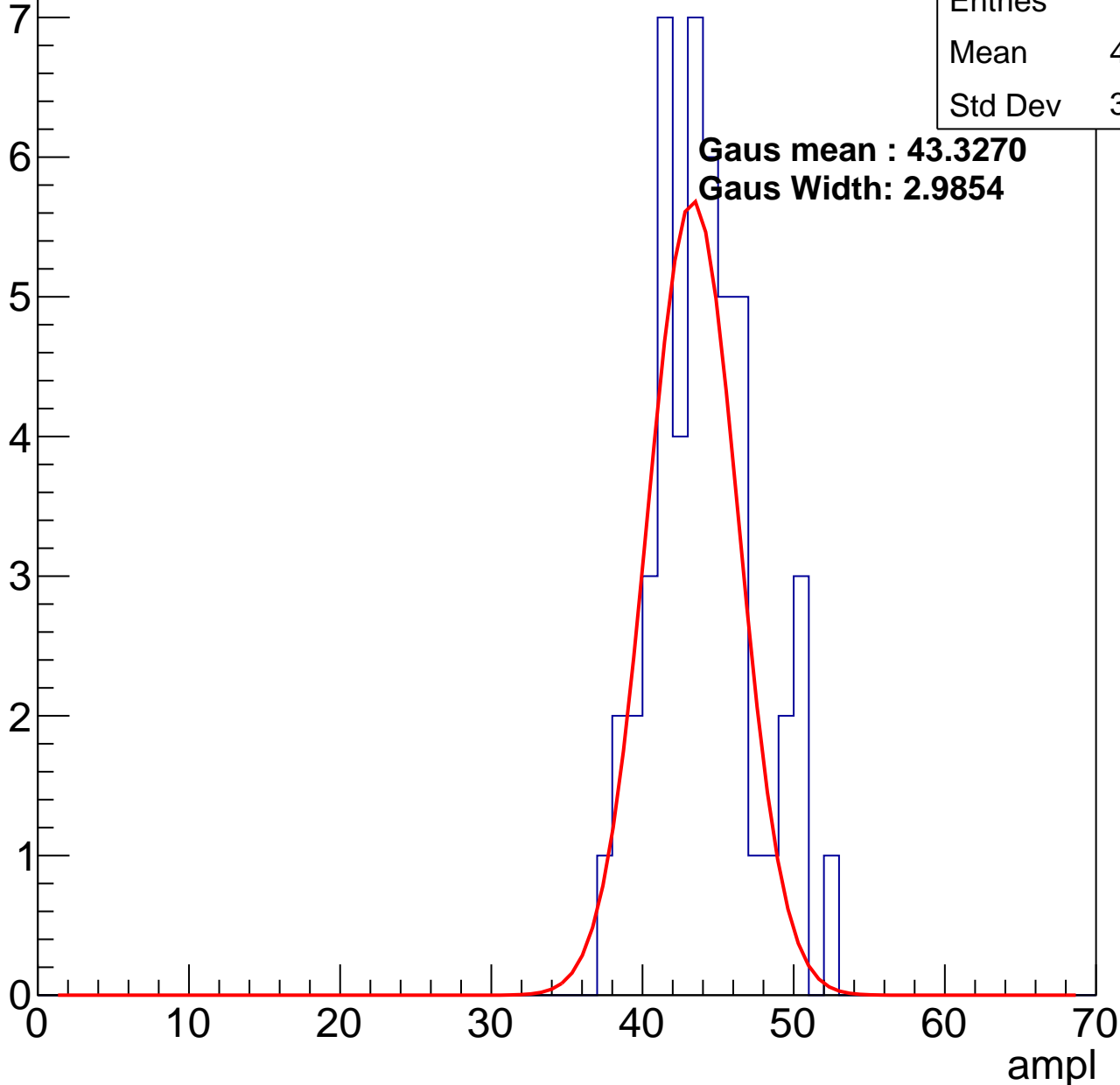
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	43.62
Std Dev	3.376

**Gaus mean : 43.3270**

**Gaus Width: 2.9854**

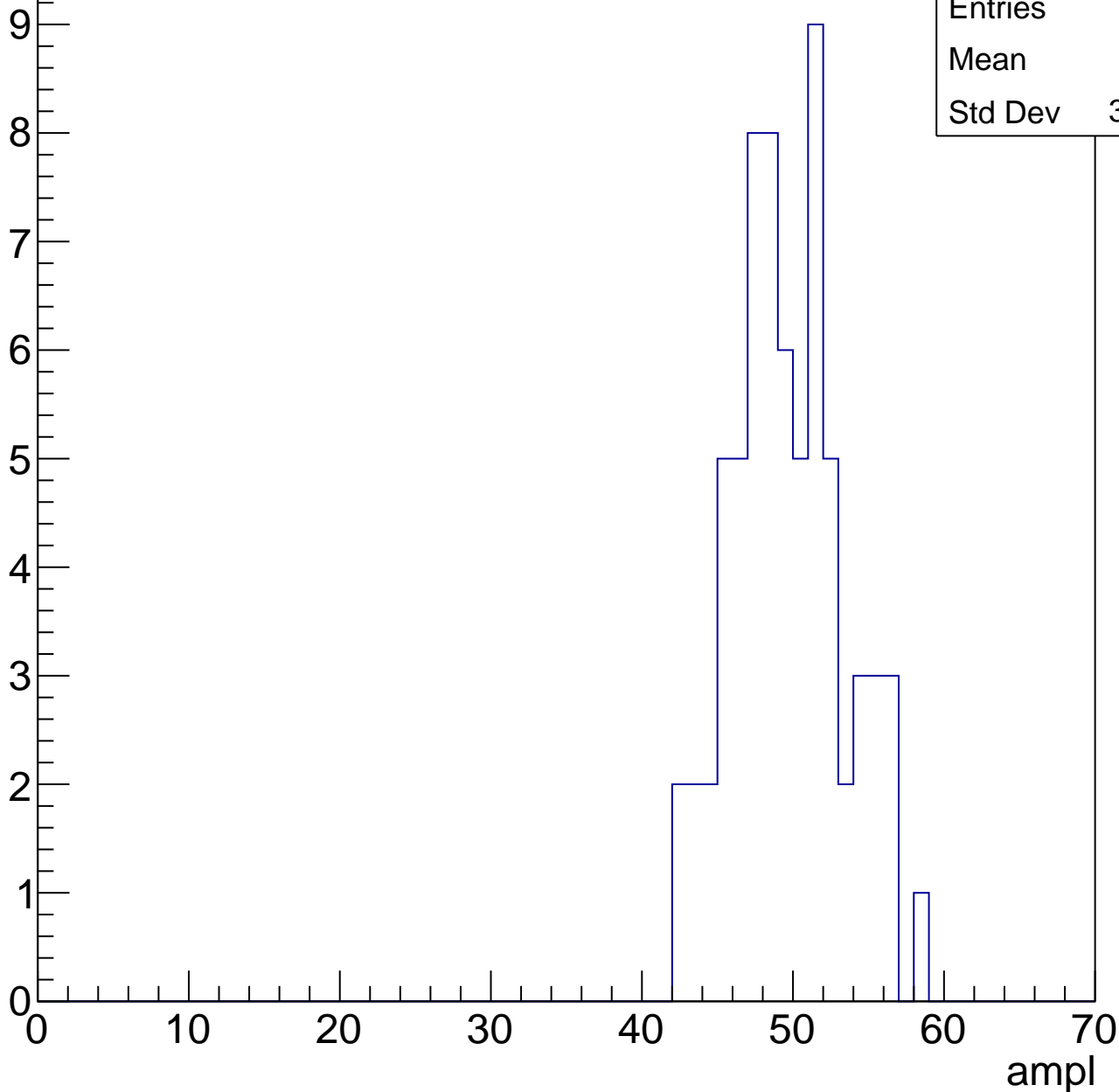


# B1L103S, U21-ch45, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	49.2
Std Dev	3.634

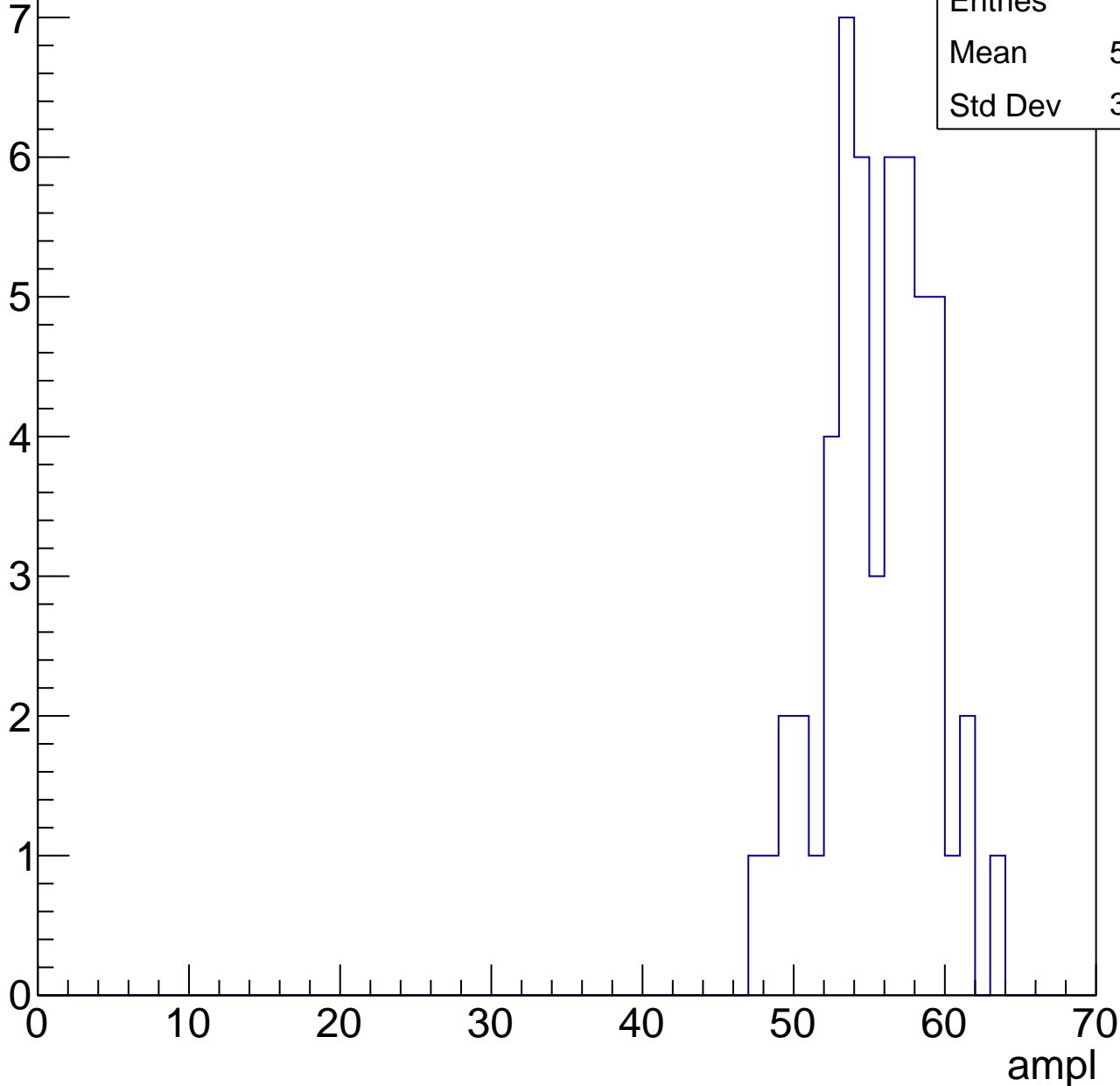


# B1L103S, U21-ch45, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	55.09
Std Dev	3.466

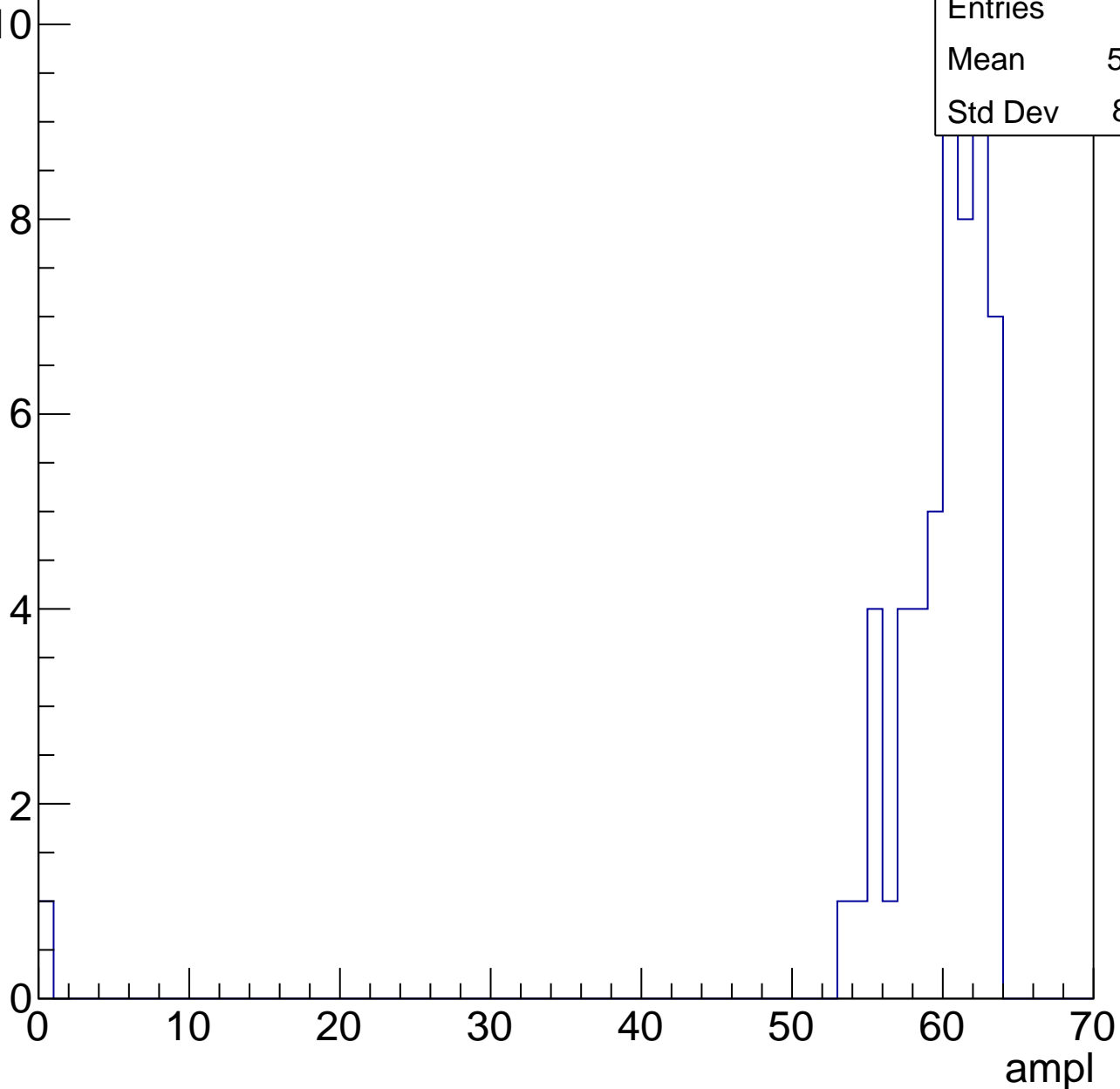


# B1L103S, U21-ch45, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	58.67
Std Dev	8.391



# B1L103S, U21-ch45, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U21-ch45, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U21-ch46, adc0

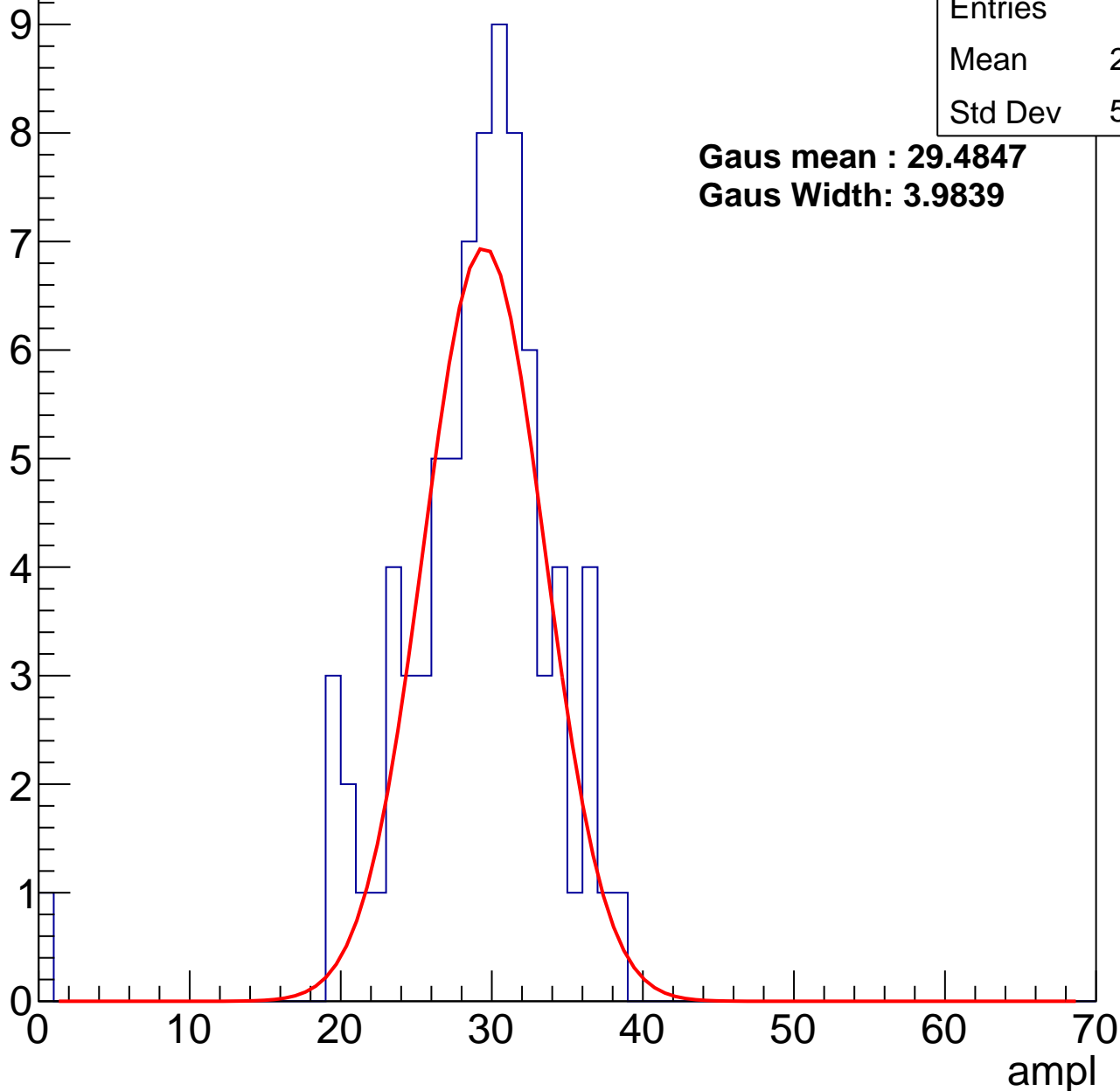
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	80
Mean	28.39
Std Dev	5.414

**Gaus mean : 29.4847**

**Gaus Width: 3.9839**



# B1L103S, U21-ch46, adc1

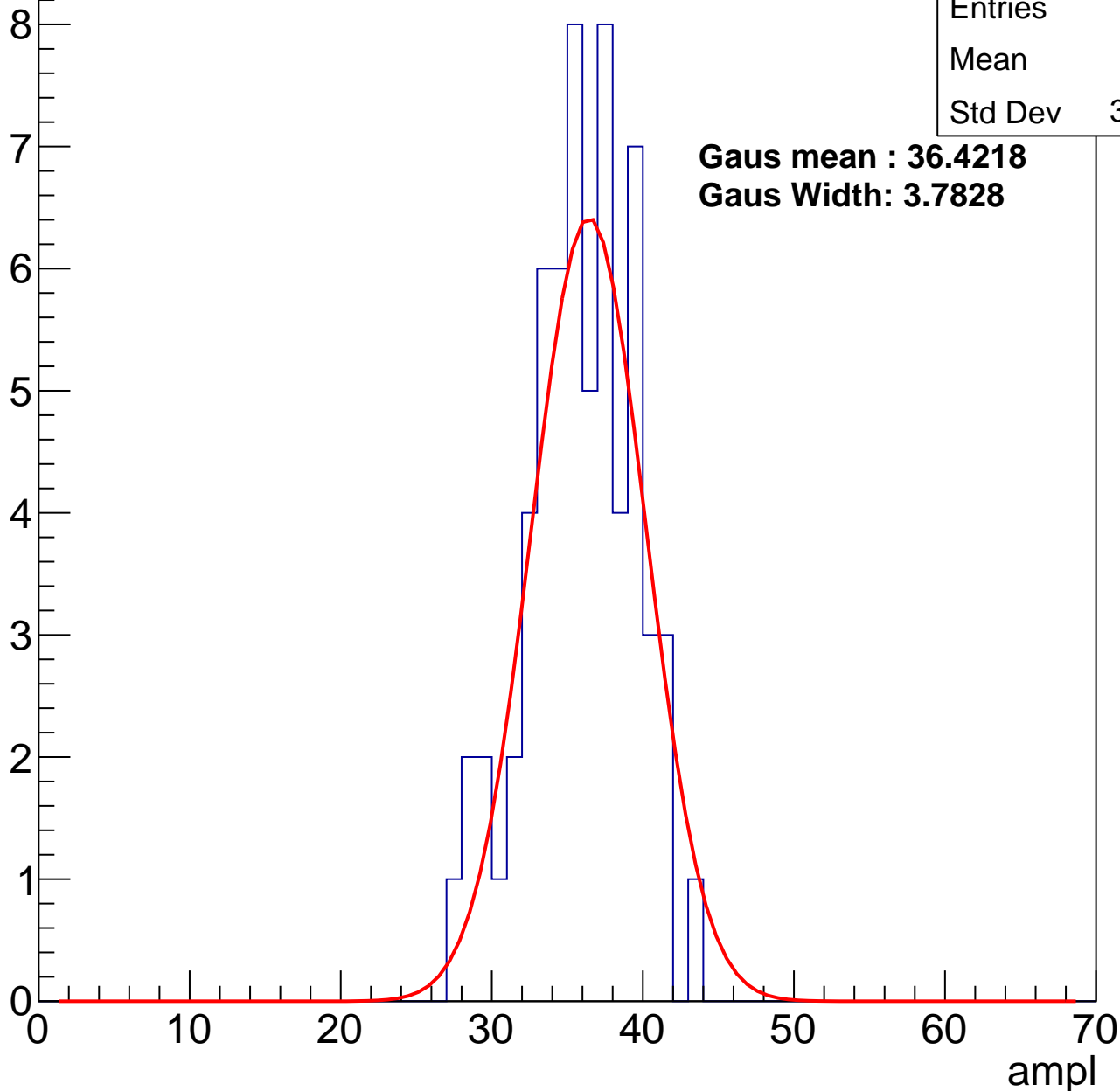
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	35.4
Std Dev	3.517

**Gaus mean : 36.4218**

**Gaus Width: 3.7828**



# B1L103S, U21-ch46, adc2

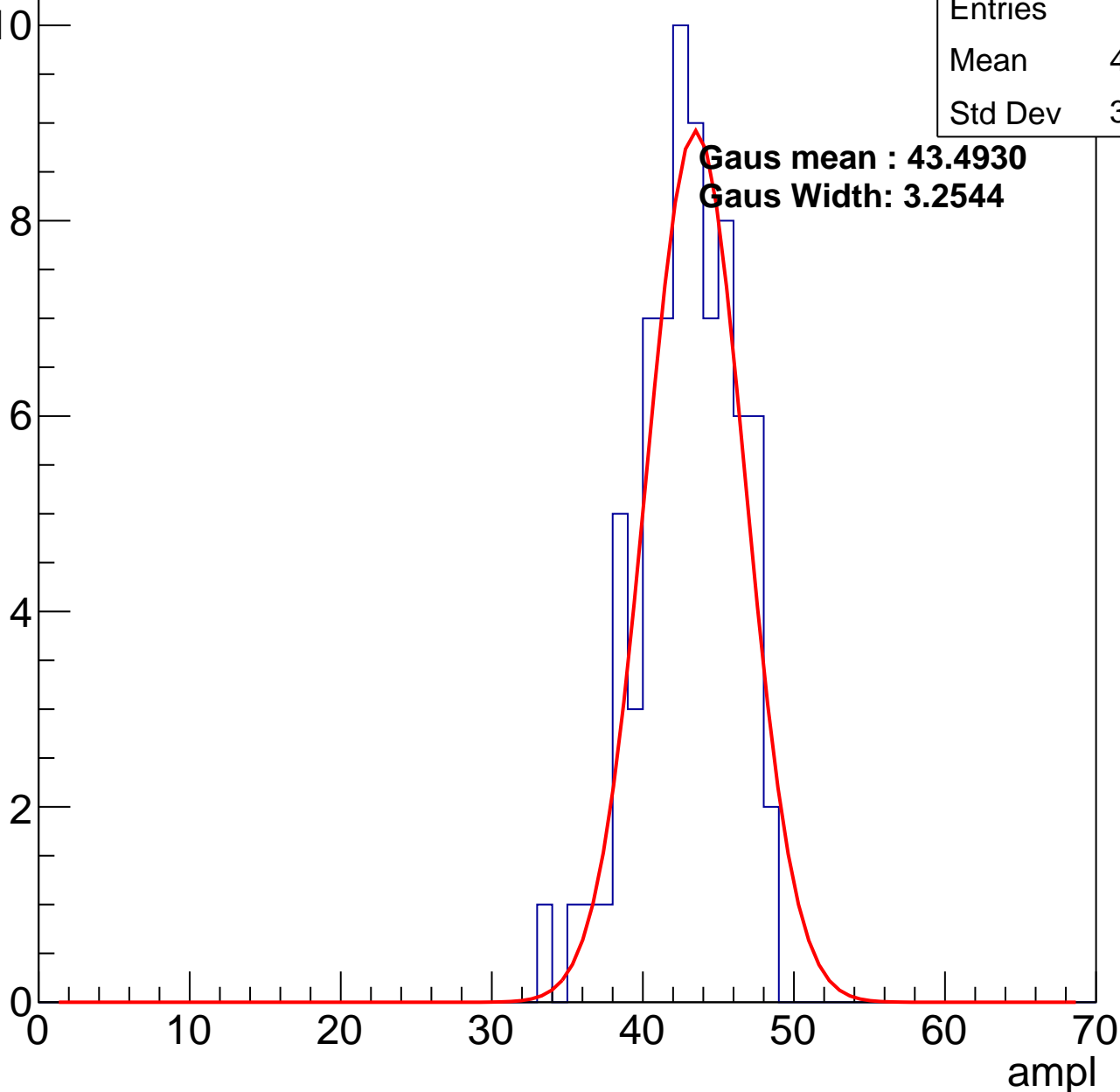
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	42.49
Std Dev	3.168

**Gaus mean : 43.4930**

**Gaus Width: 3.2544**

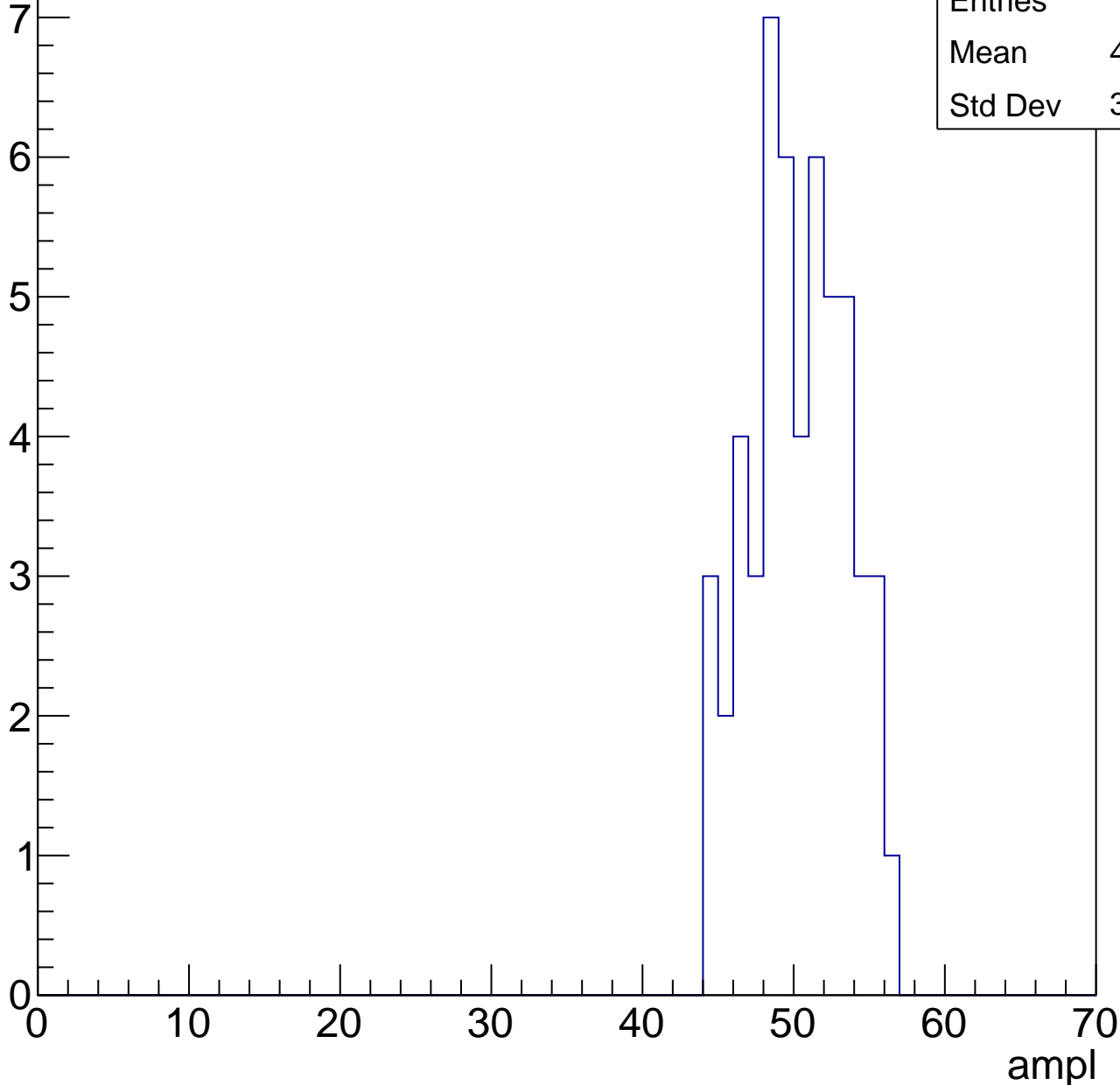


# B1L103S, U21-ch46, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	49.83
Std Dev	3.136

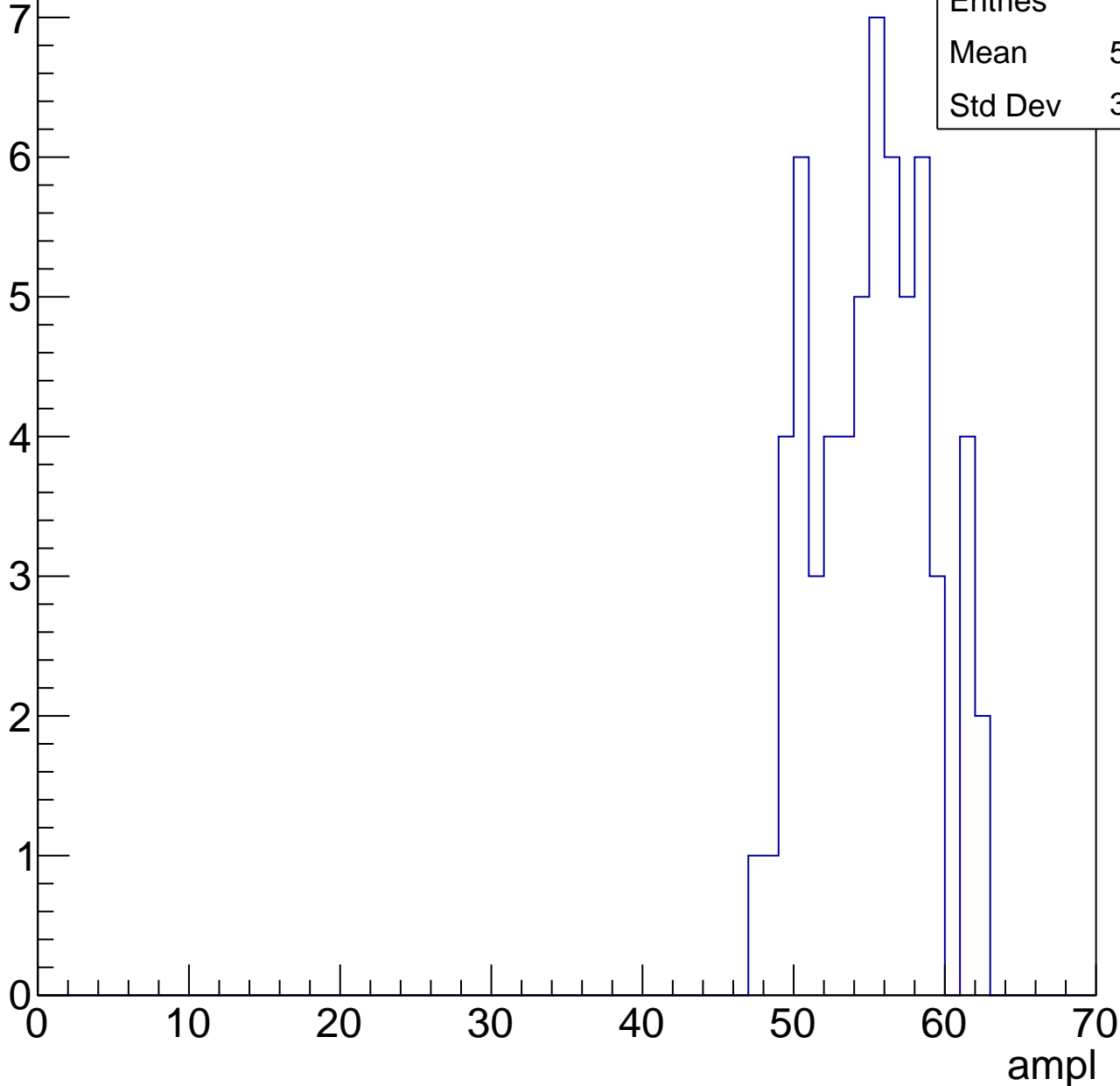


# B1L103S, U21-ch46, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	54.64
Std Dev	3.785



# B1L103S, U21-ch46, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

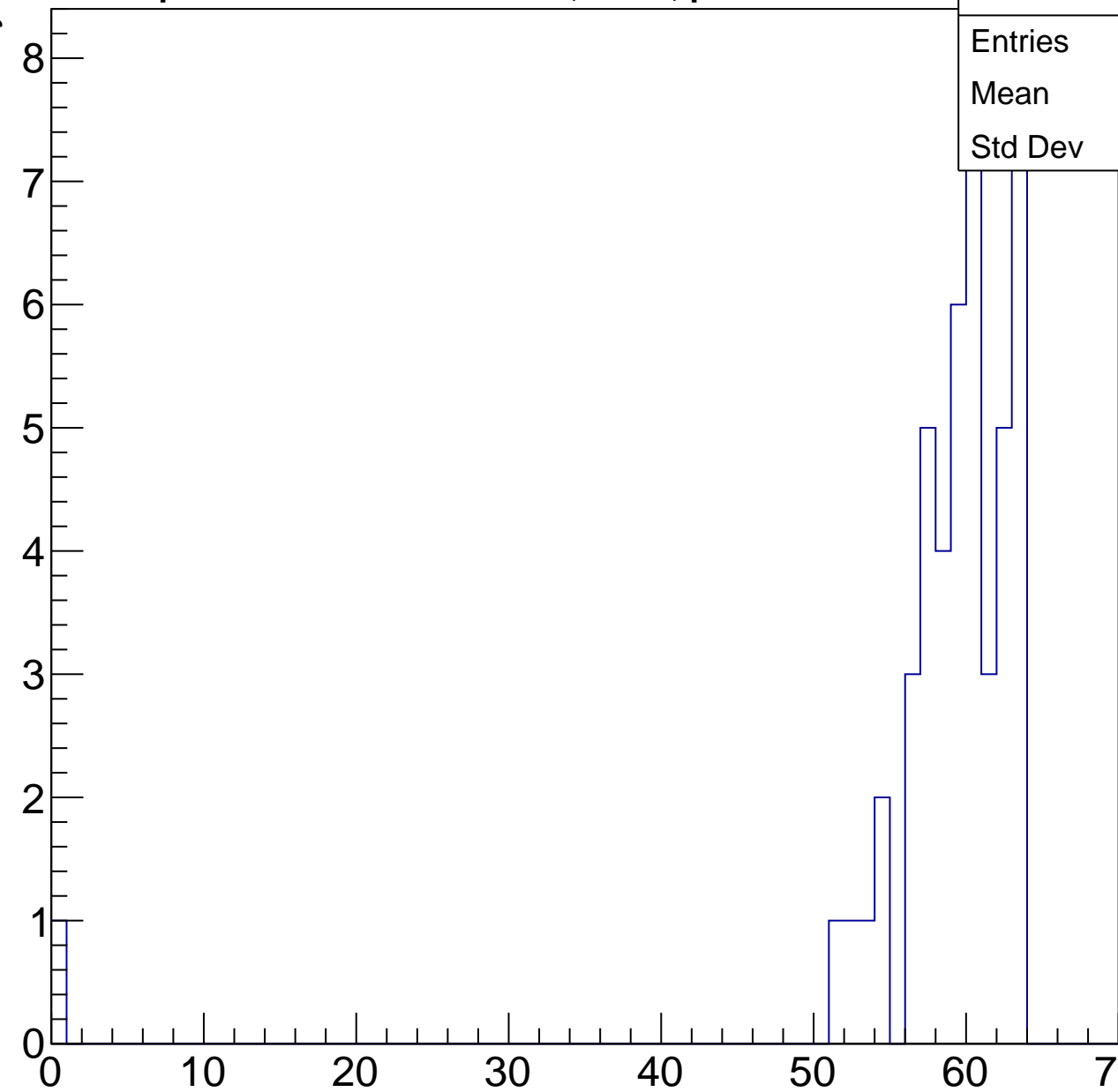
Entry

Entries	48
Mean	57.92
Std Dev	8.976

8  
7  
6  
5  
4  
3  
2  
1  
0

0 10 20 30 40 50 60 70

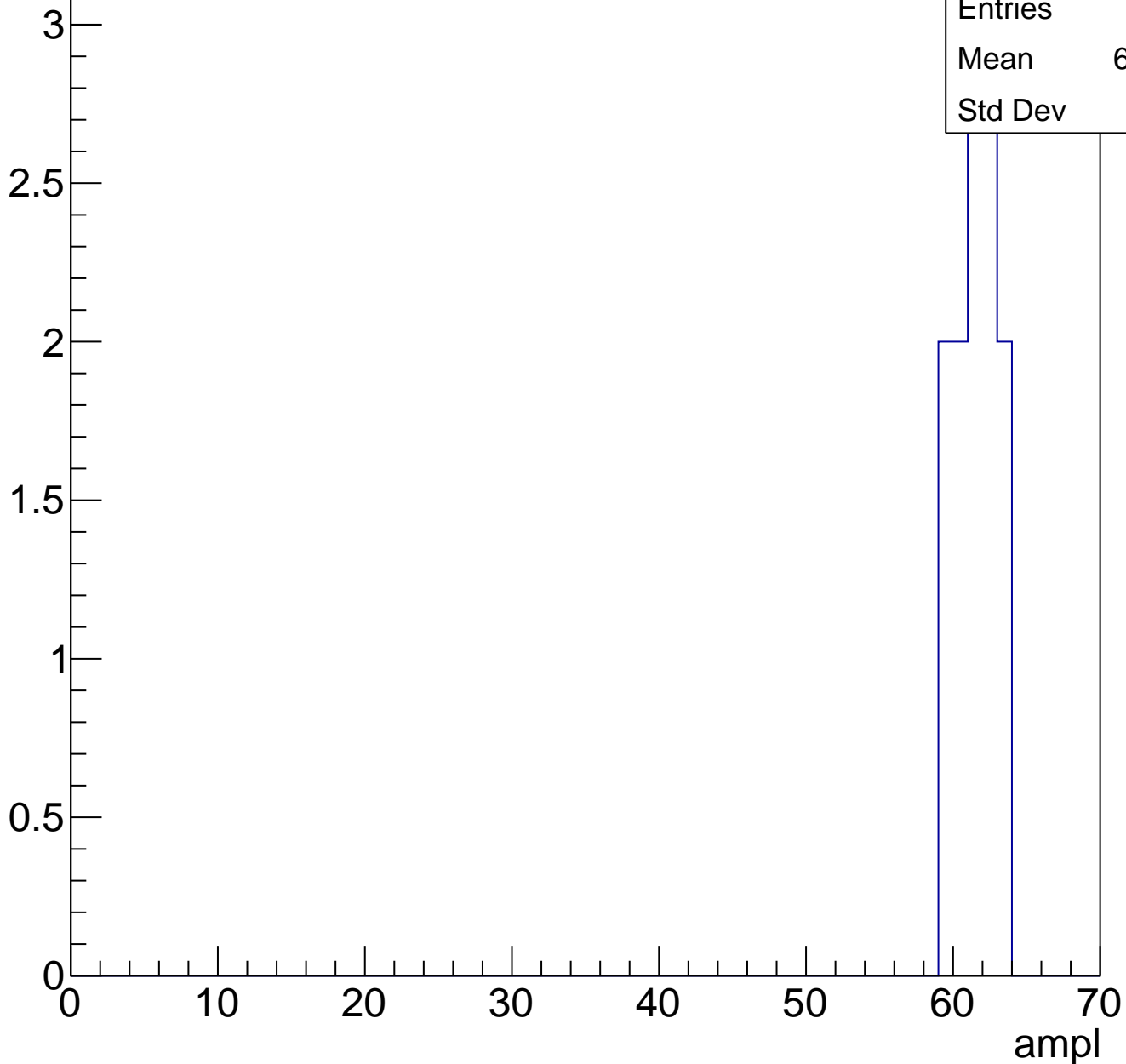
ampl



# B1L103S, U21-ch46, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U21-ch46, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U21-ch47, adc0

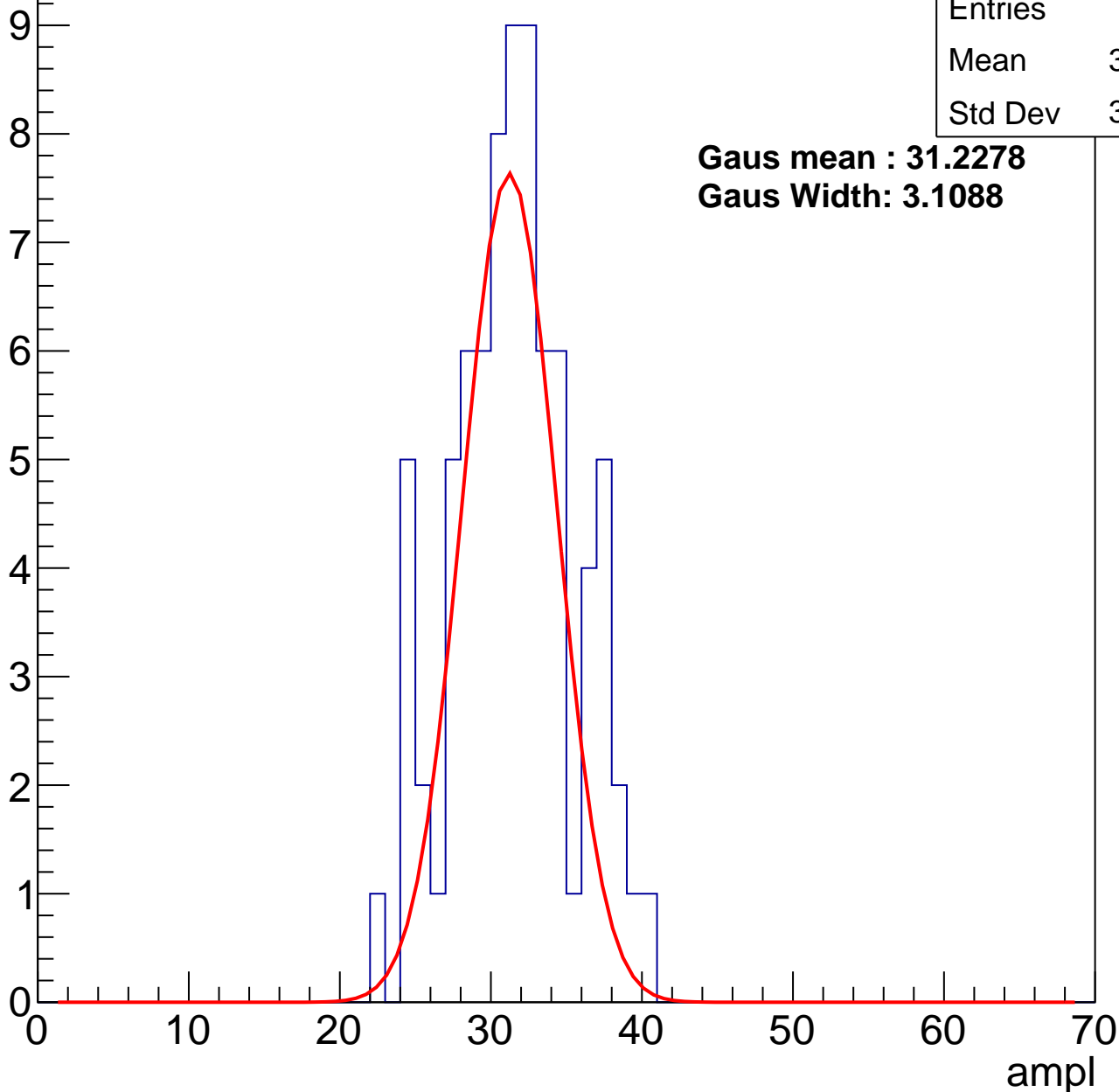
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	31.06
Std Dev	3.946

**Gaus mean : 31.2278**

**Gaus Width: 3.1088**



# B1L103S, U21-ch47, adc1

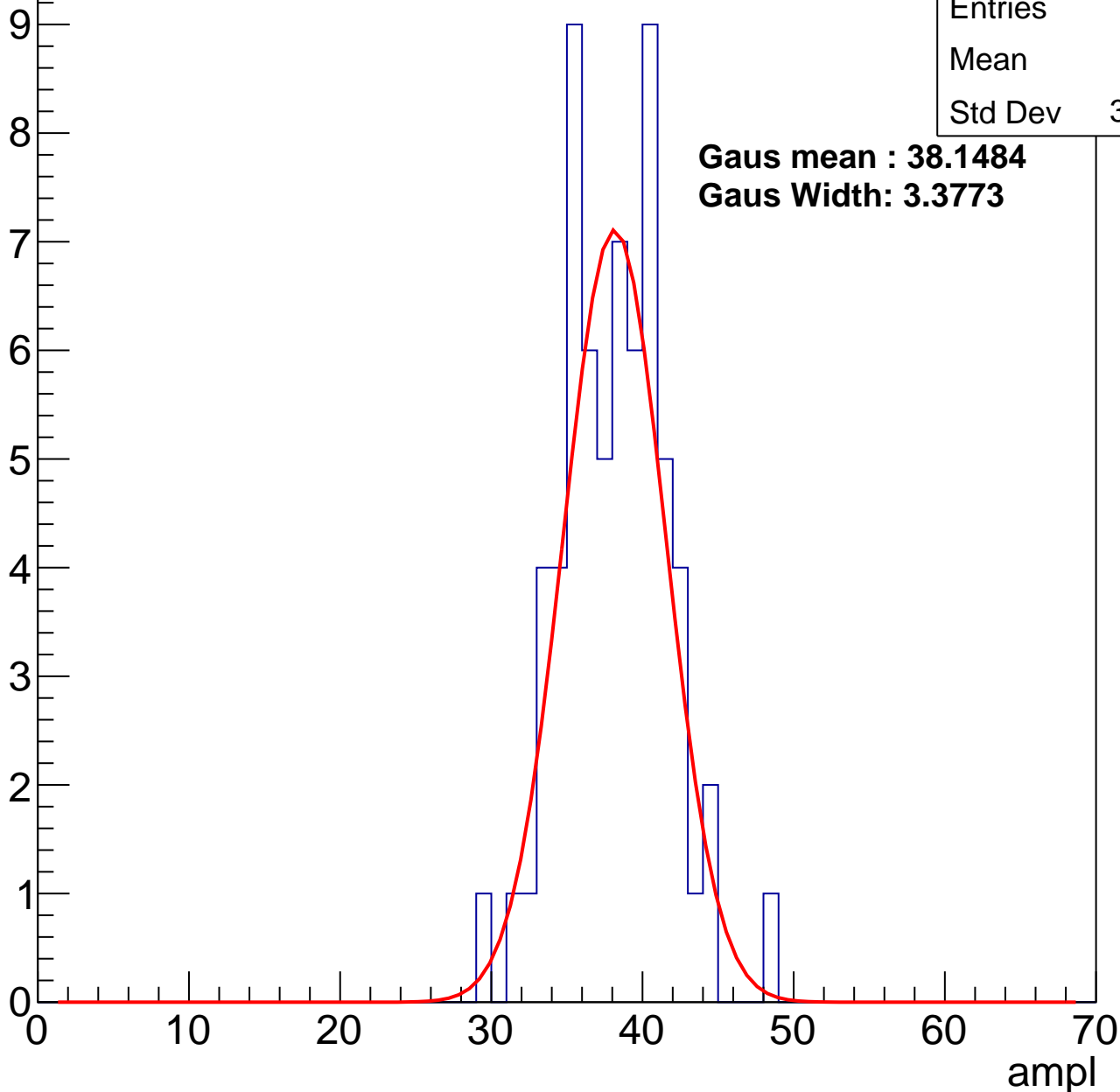
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	37.7
Std Dev	3.442

**Gaus mean : 38.1484**

**Gaus Width: 3.3773**



# B1L103S, U21-ch47, adc2

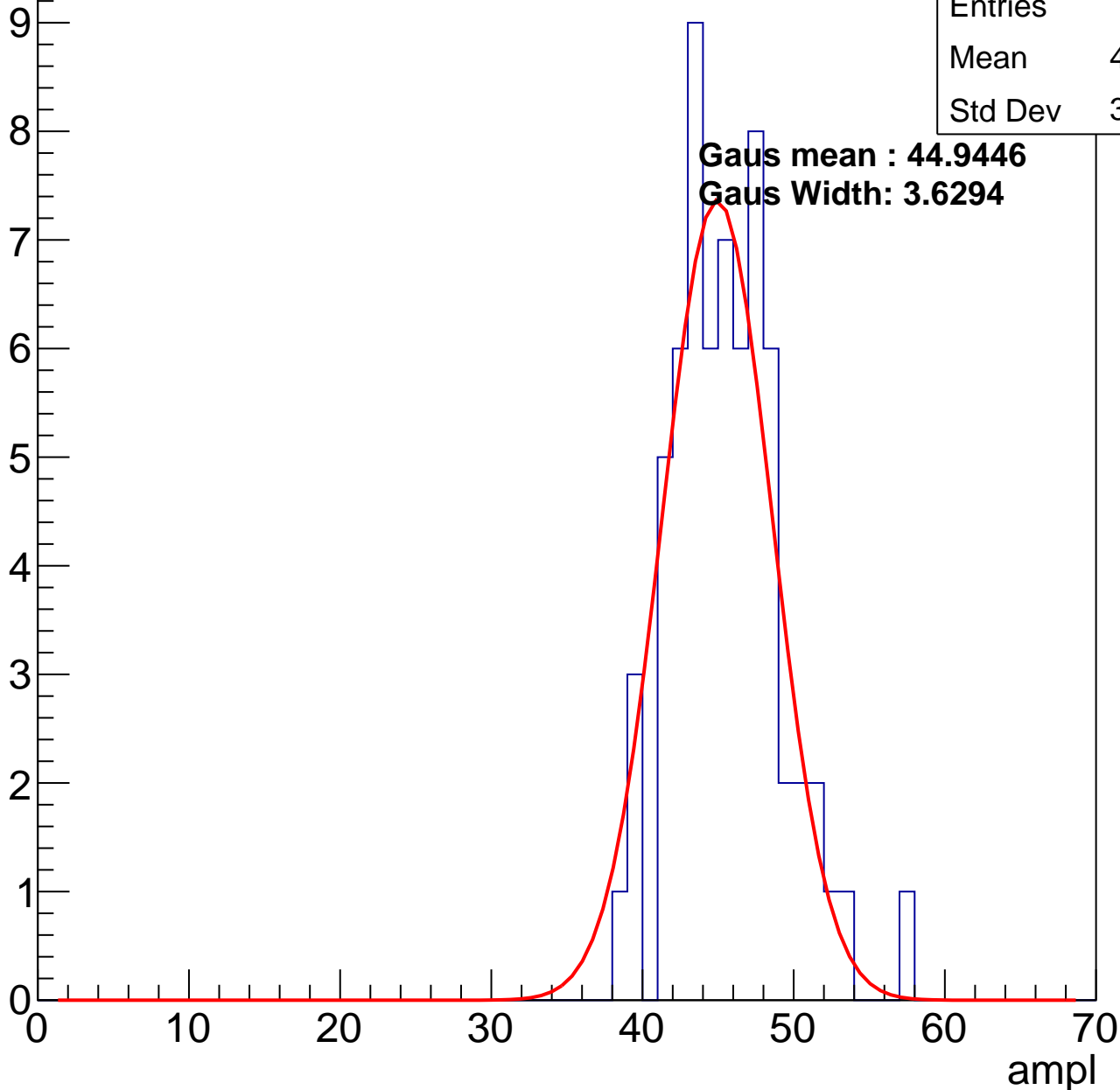
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	45.15
Std Dev	3.556

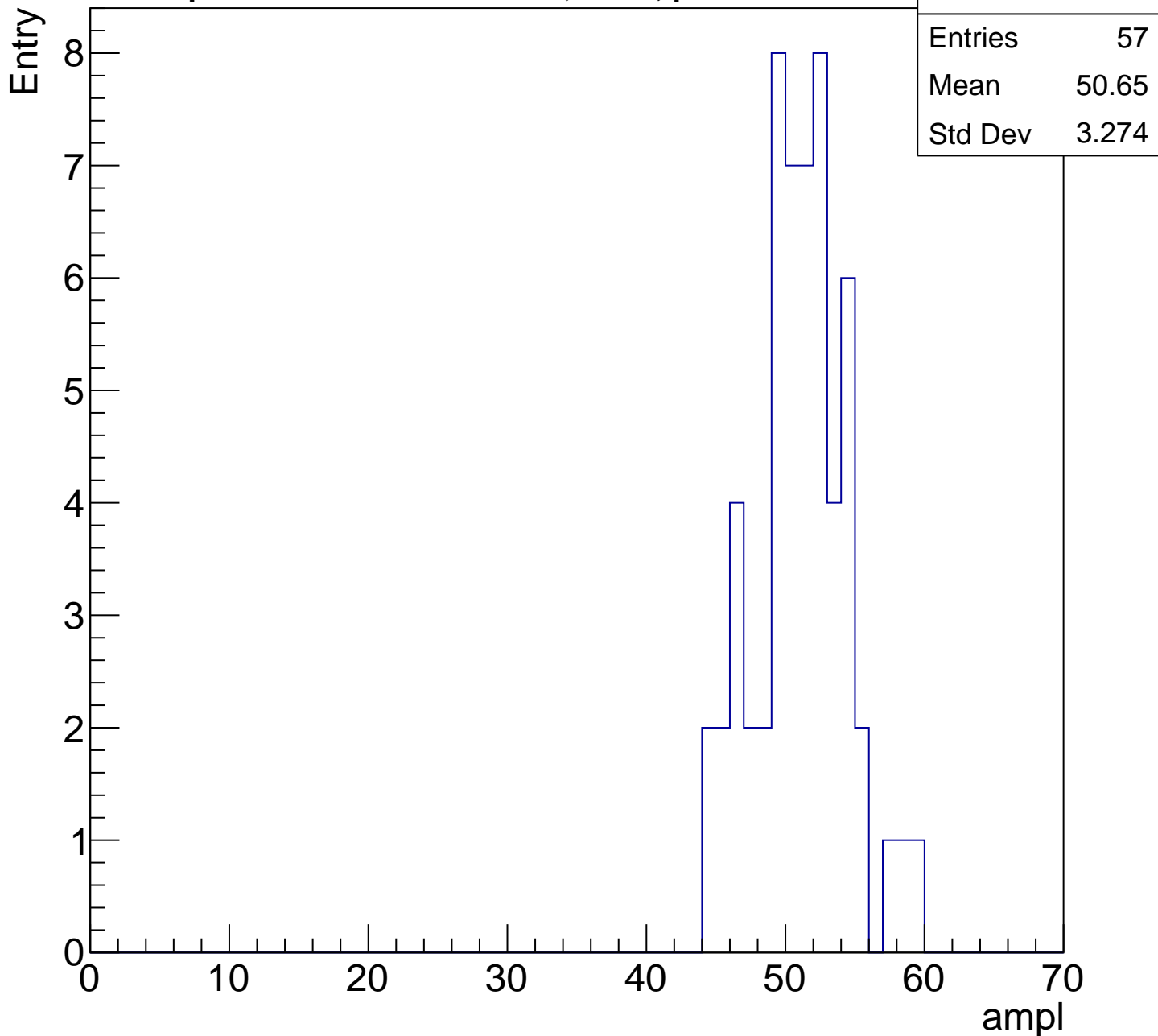
**Gaus mean : 44.9446**

**Gaus Width: 3.6294**



# B1L103S, U21-ch47, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

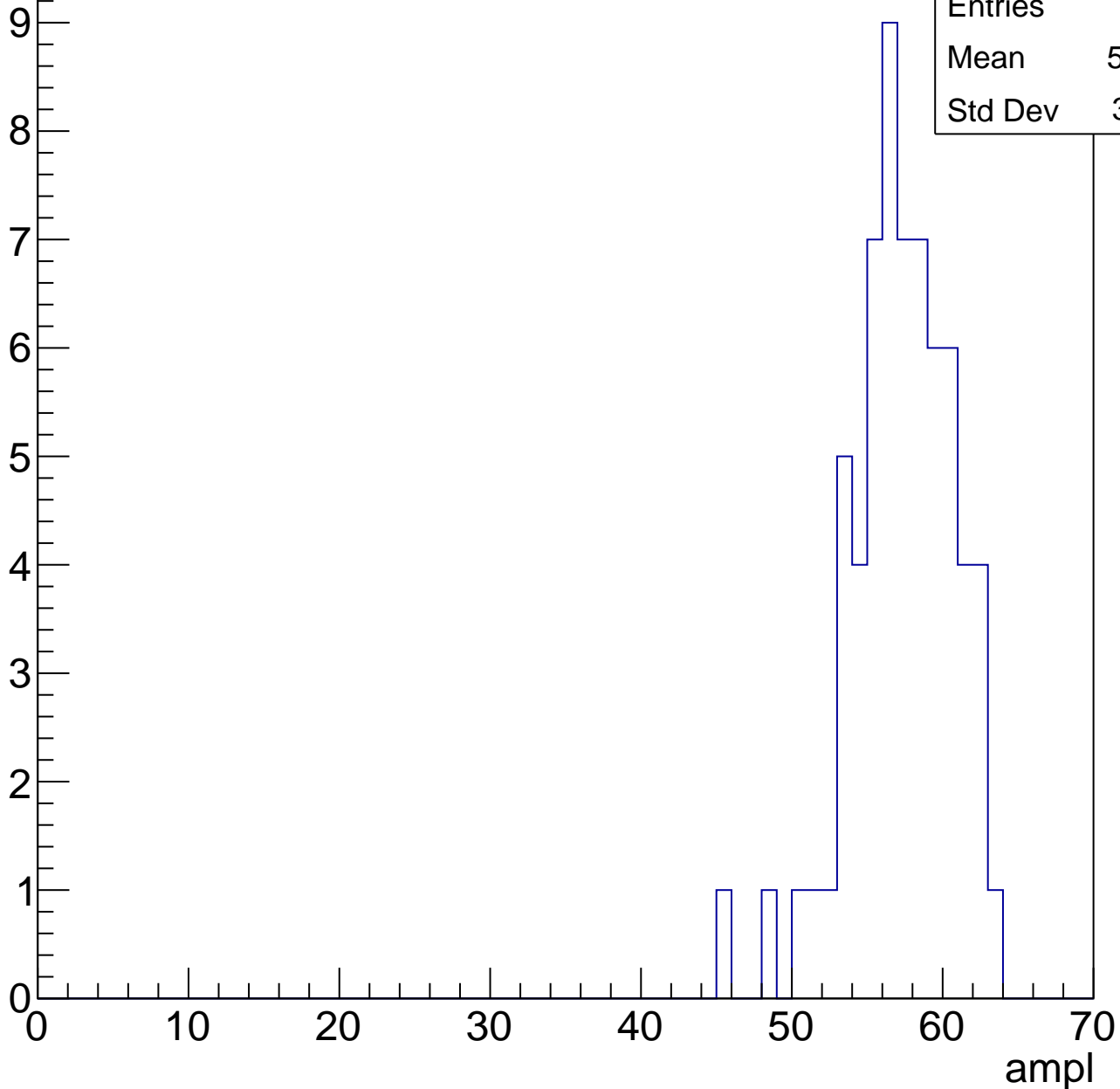


# B1L103S, U21-ch47, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	56.77
Std Dev	3.441

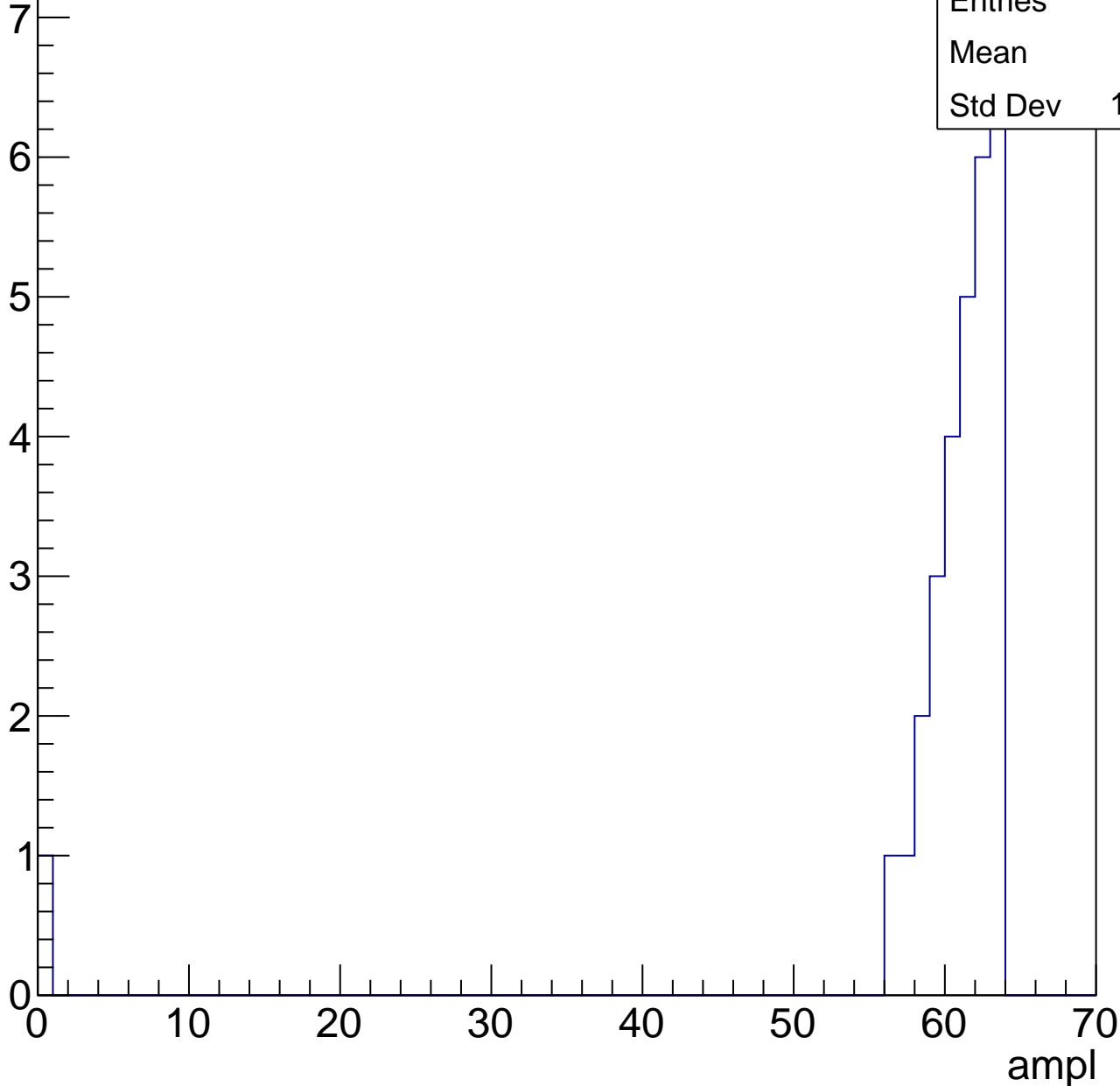


# B1L103S, U21-ch47, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

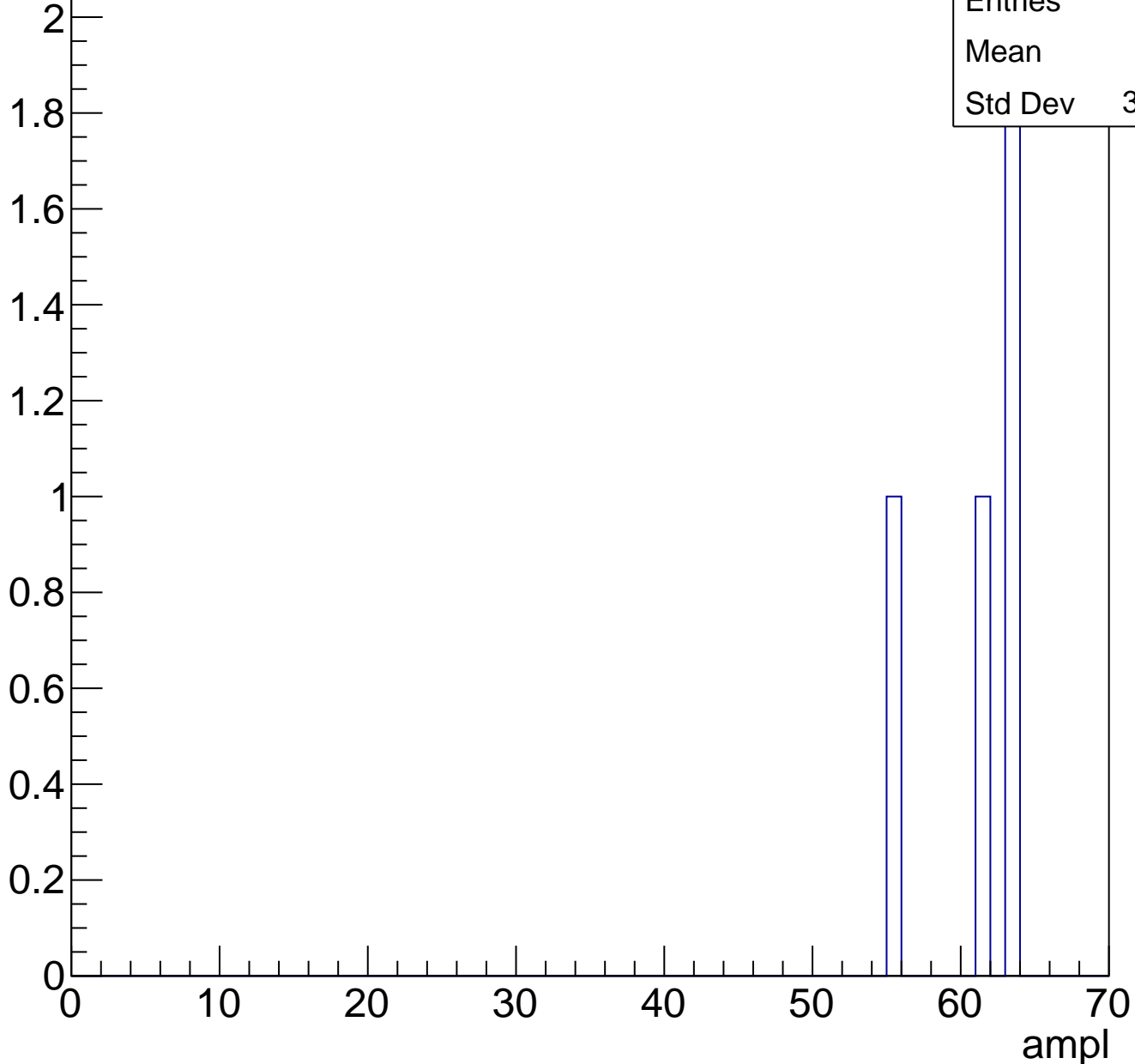
Entries	30
Mean	58.8
Std Dev	11.08



# B1L103S, U21-ch47, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U21-ch47, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U21-ch48, adc0

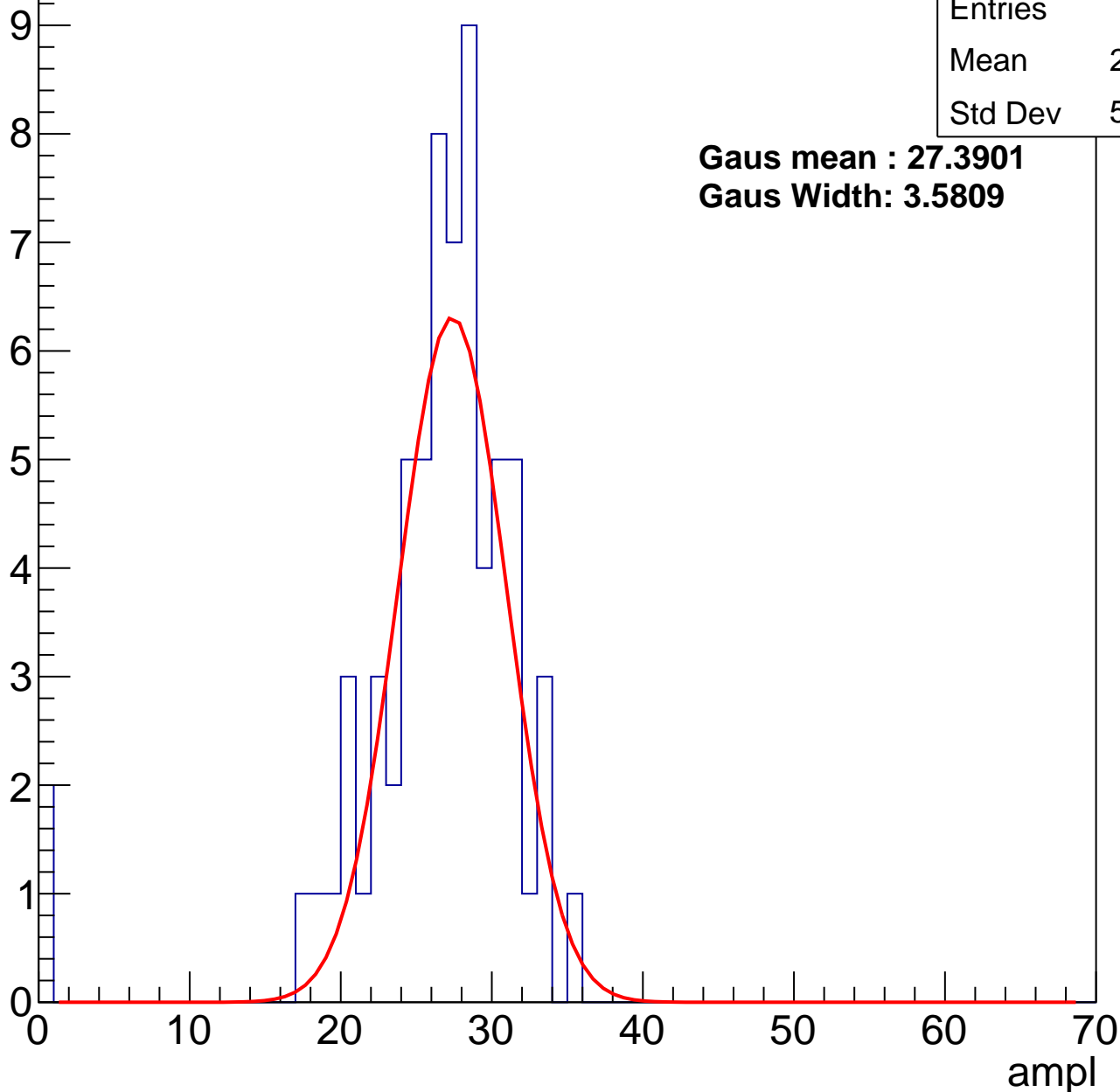
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	25.79
Std Dev	5.878

**Gaus mean : 27.3901**

**Gaus Width: 3.5809**



# B1L103S, U21-ch48, adc1

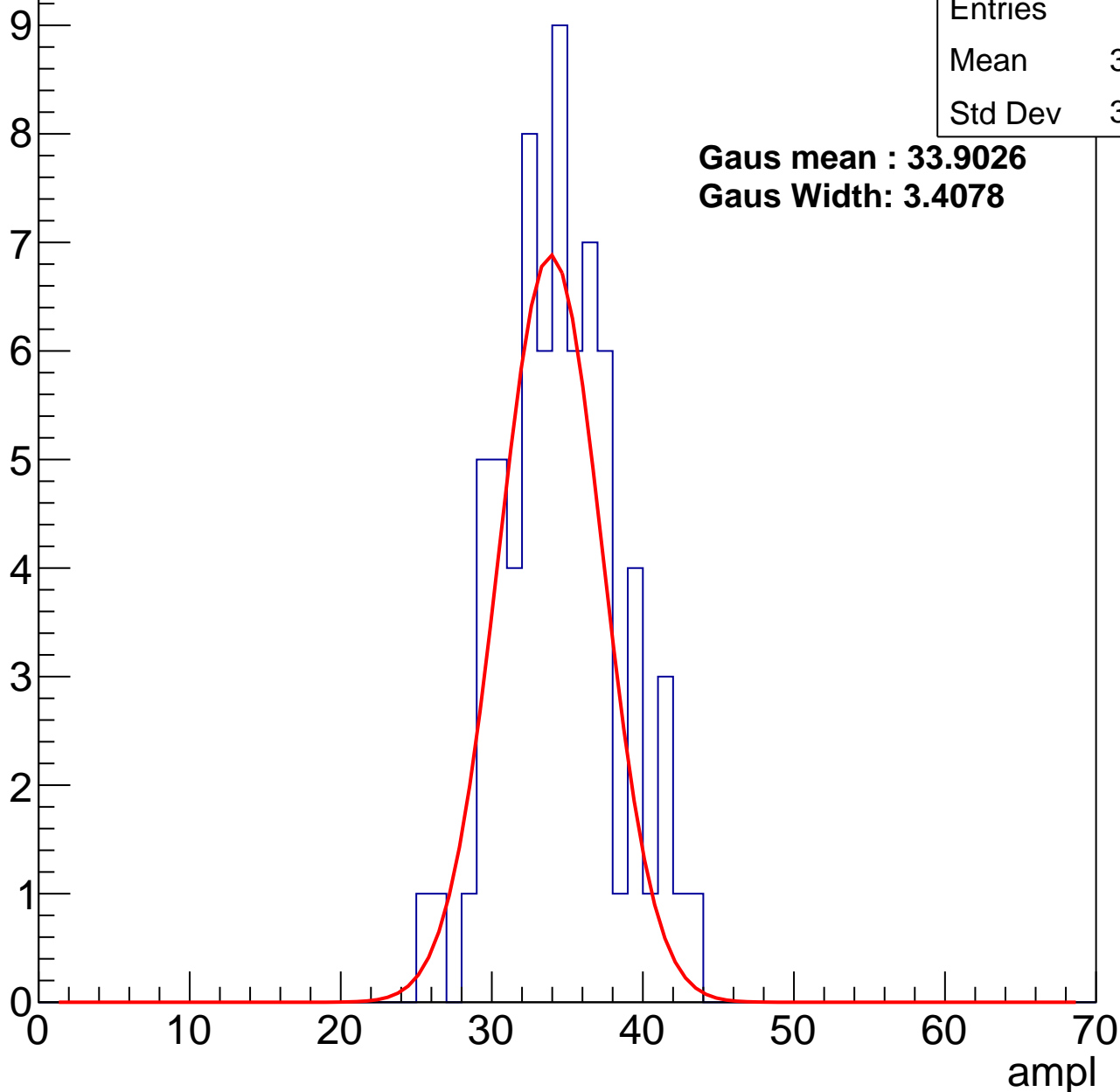
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	34.06
Std Dev	3.764

**Gaus mean : 33.9026**

**Gaus Width: 3.4078**



# B1L103S, U21-ch48, adc2

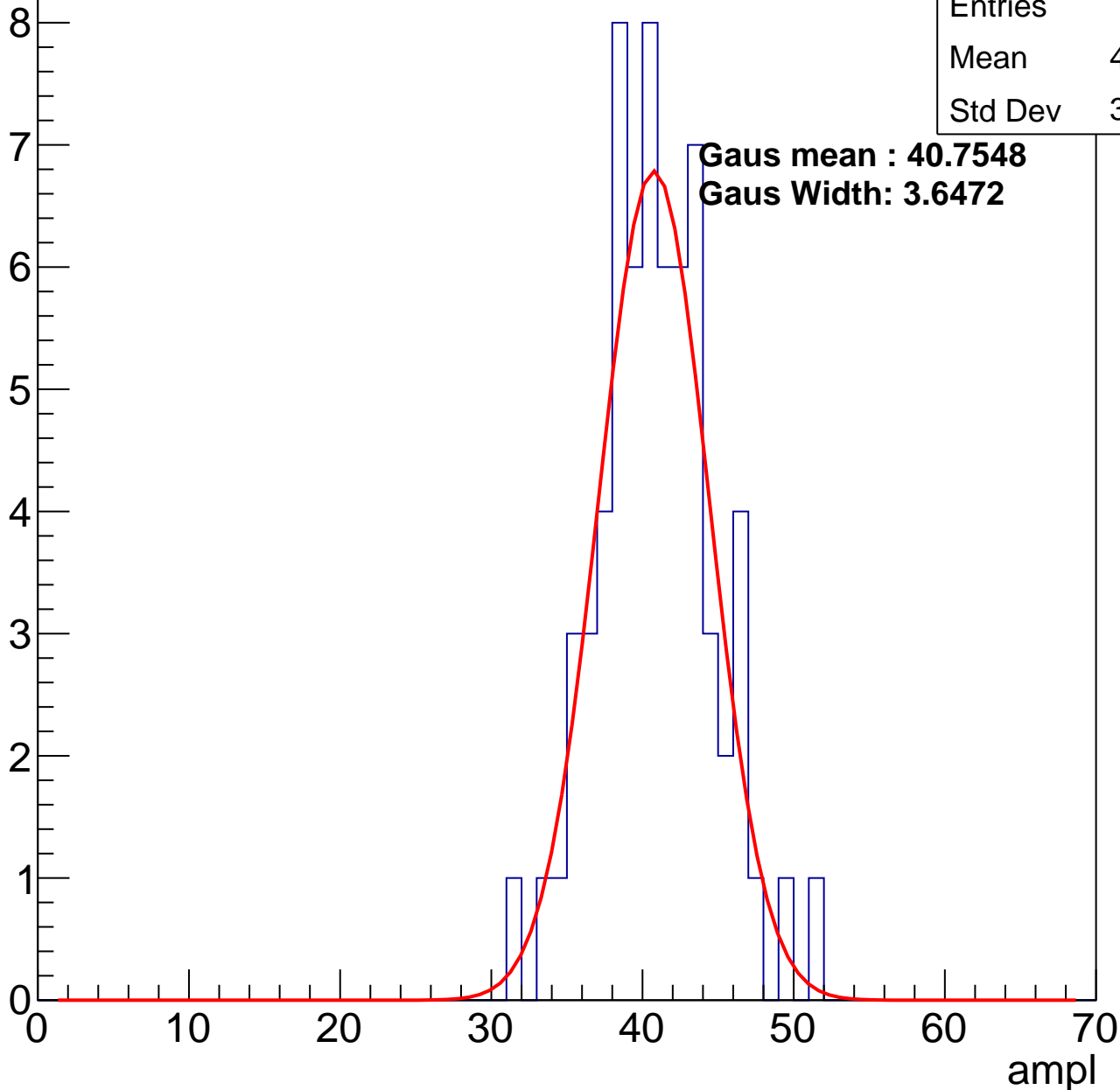
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	40.44
Std Dev	3.766

**Gaus mean : 40.7548**

**Gaus Width: 3.6472**

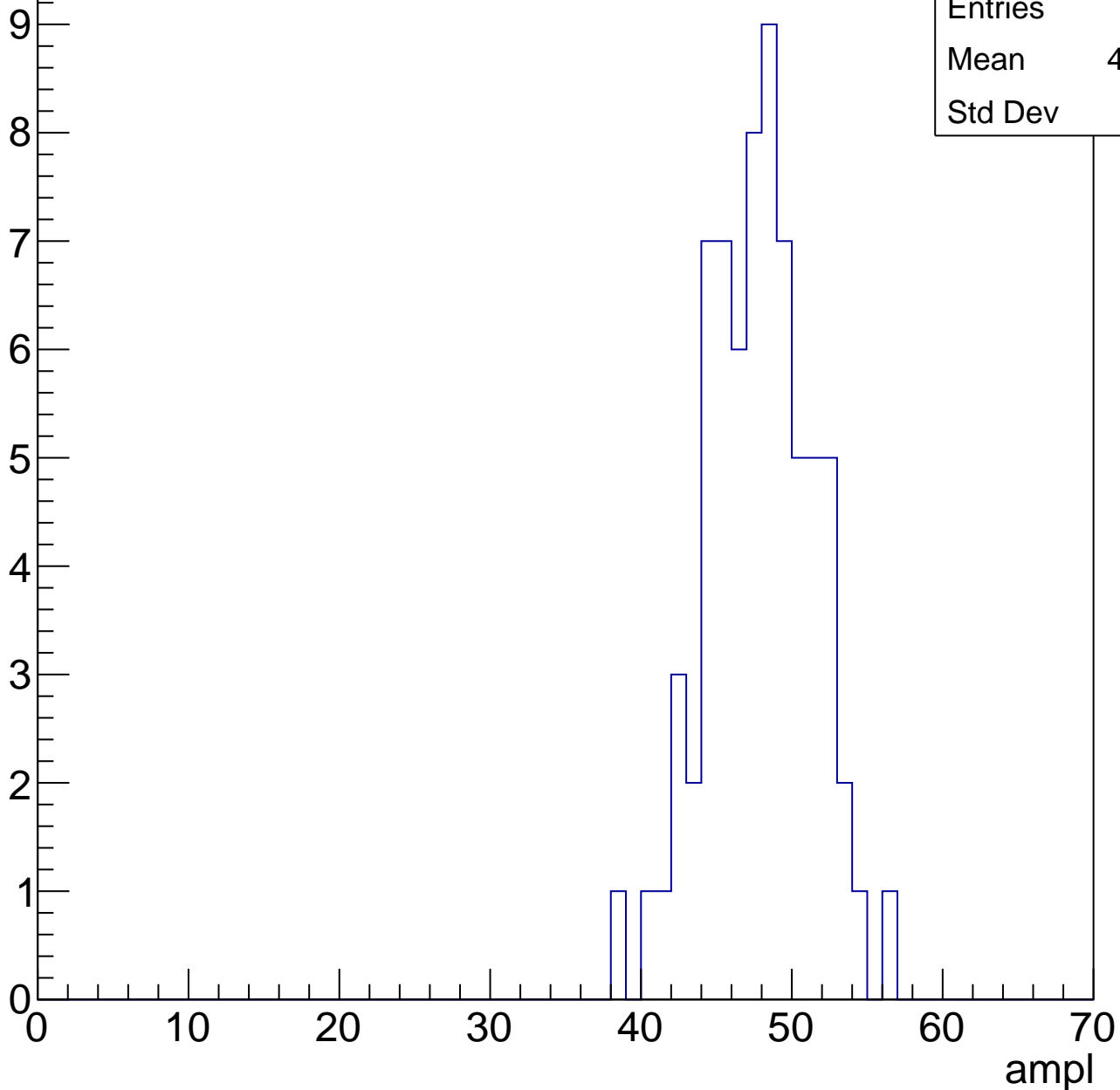


# B1L103S, U21-ch48, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	47.35
Std Dev	3.46

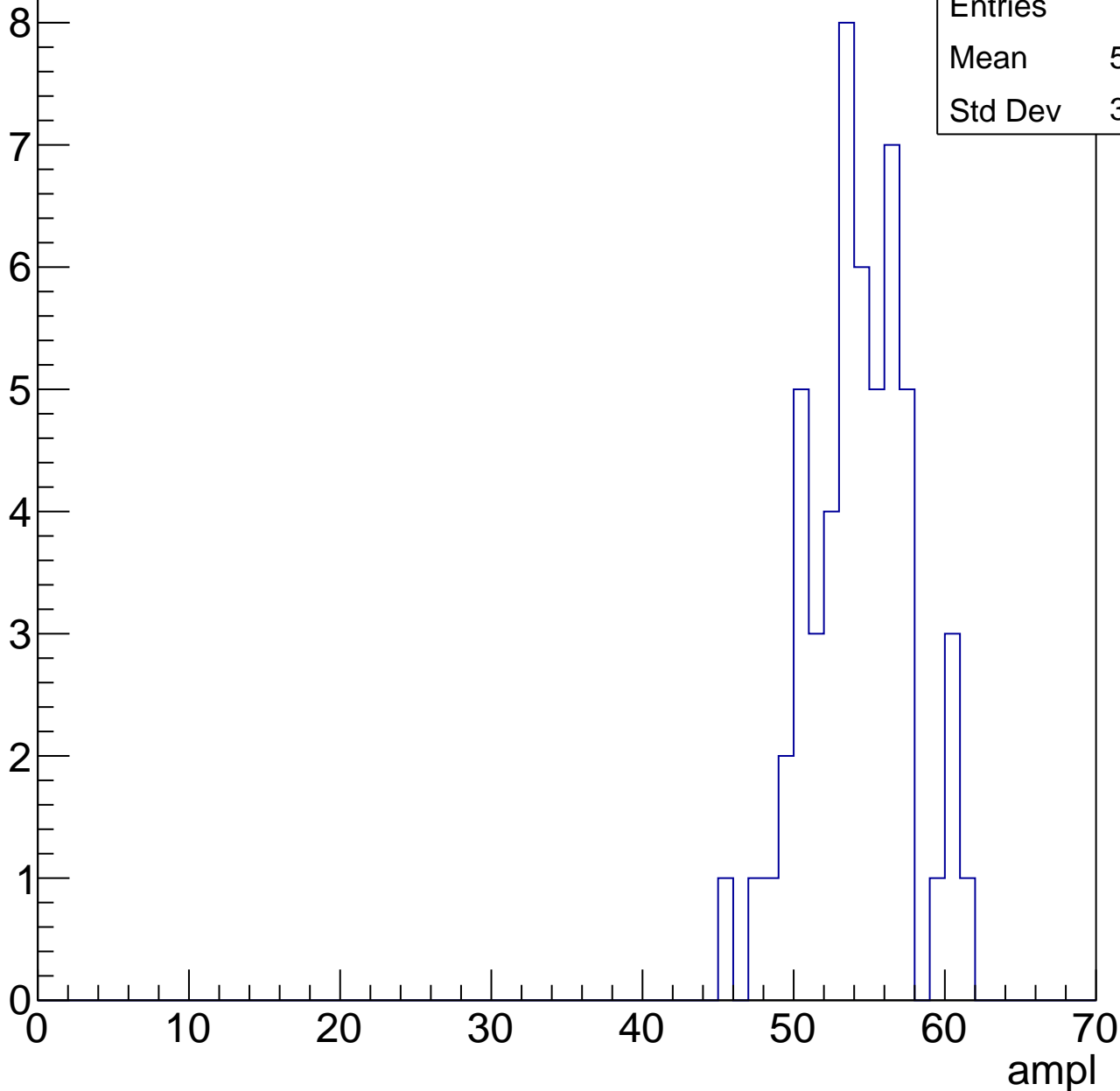


# B1L103S, U21-ch48, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	53.75
Std Dev	3.375

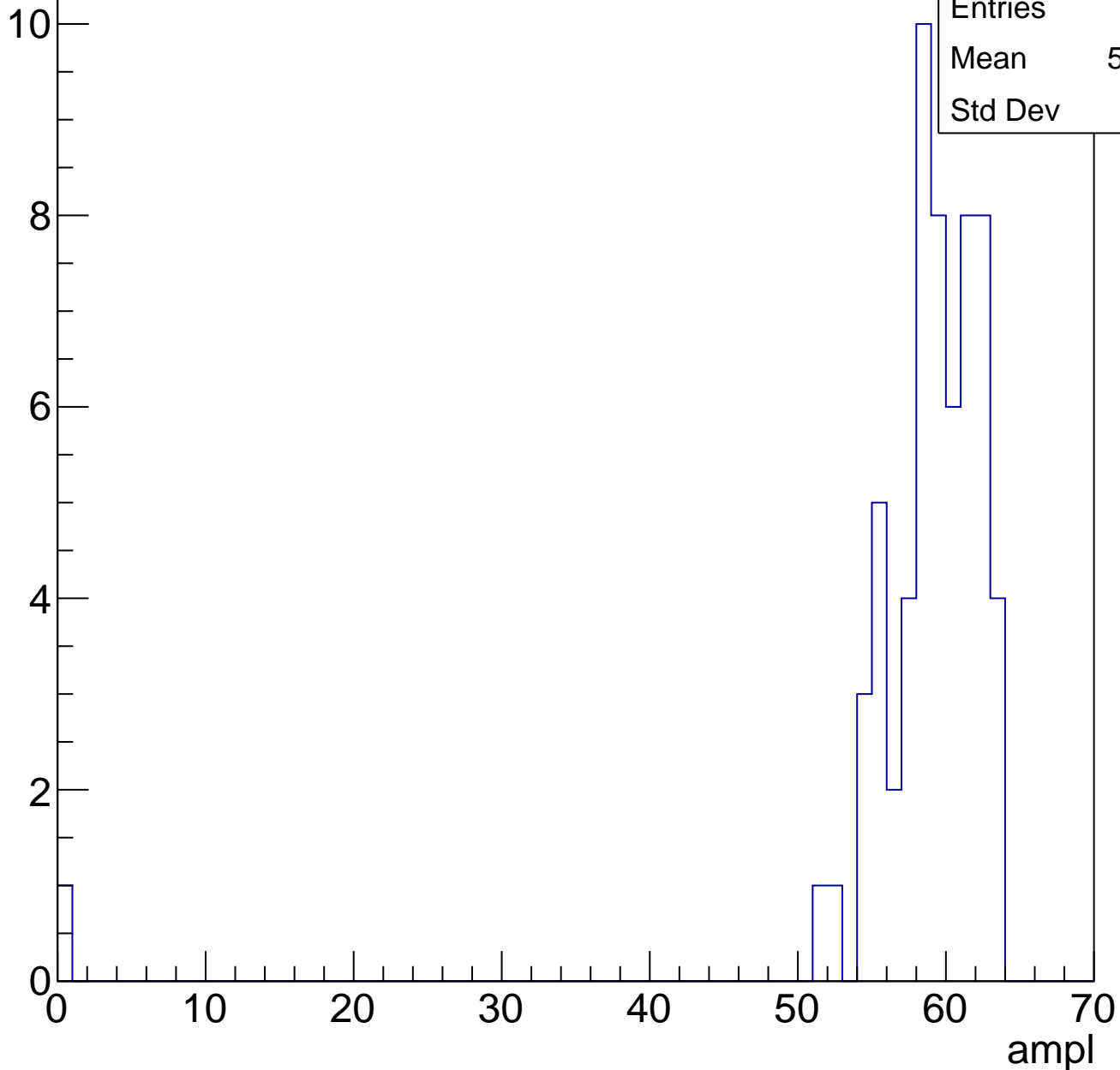


# B1L103S, U21-ch48, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	61
Mean	57.84
Std Dev	7.98

Entry

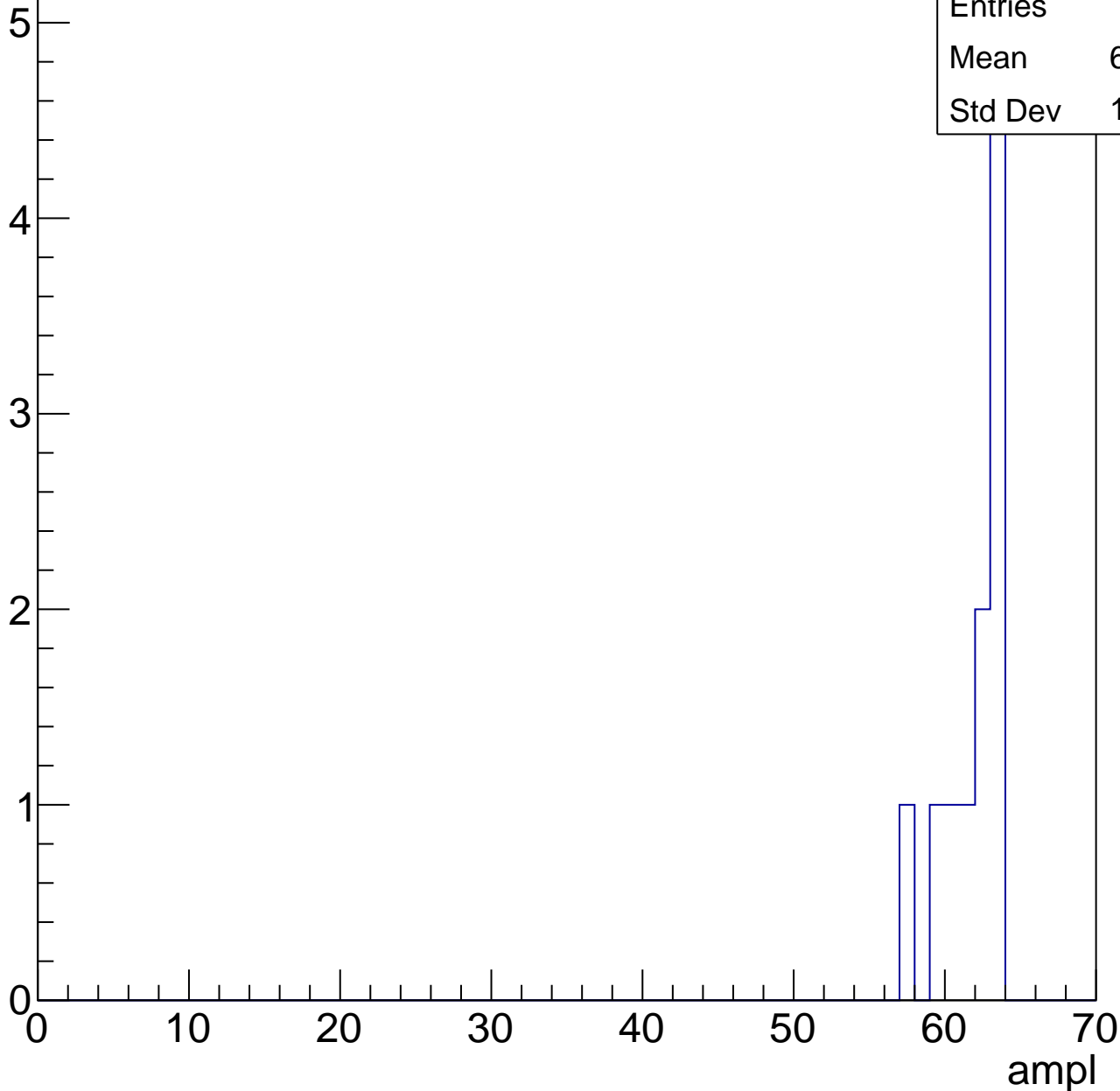


# B1L103S, U21-ch48, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	11
Mean	61.45
Std Dev	1.924

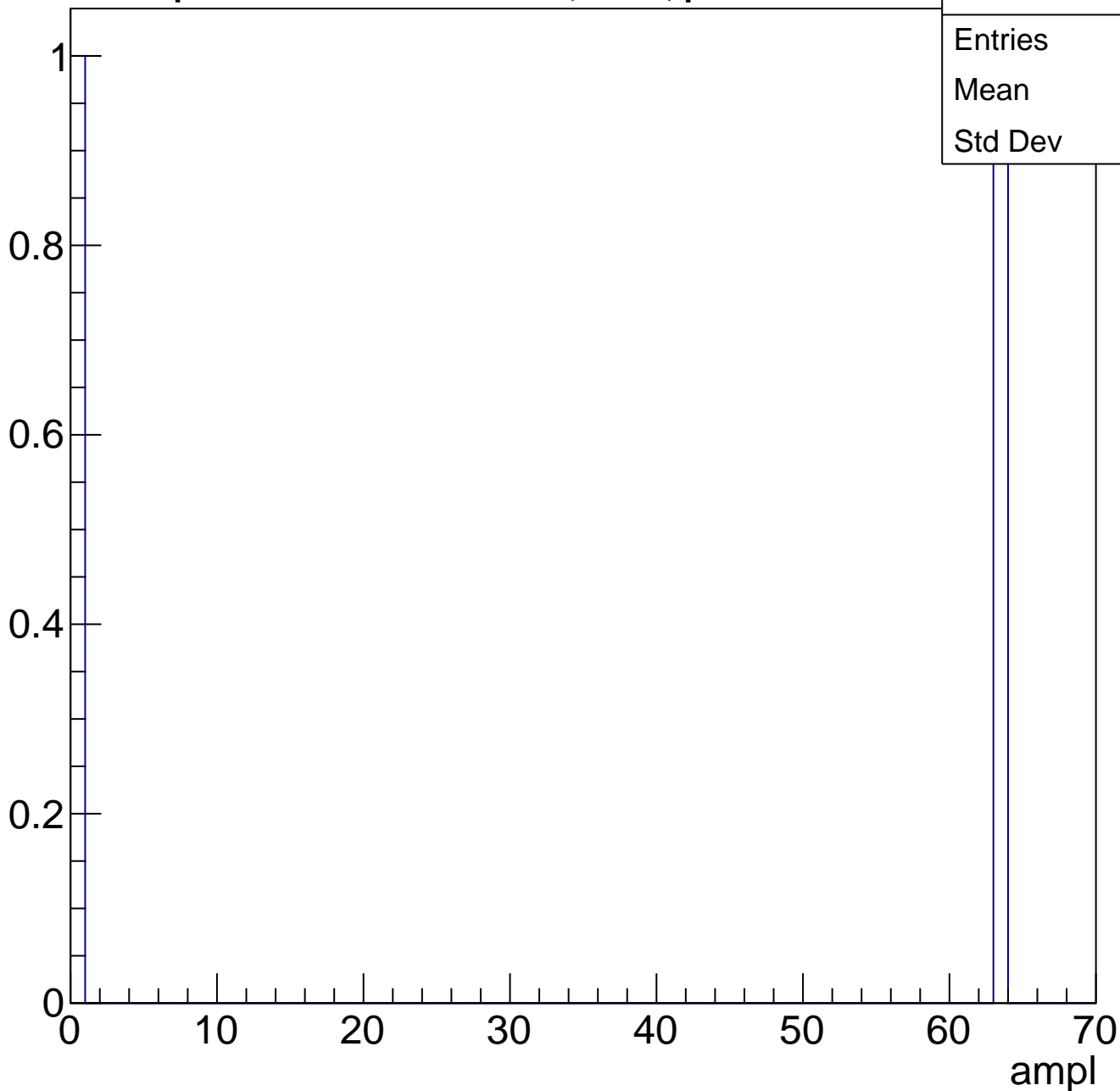




# B1L103S, U21-ch48, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U21-ch49, adc0

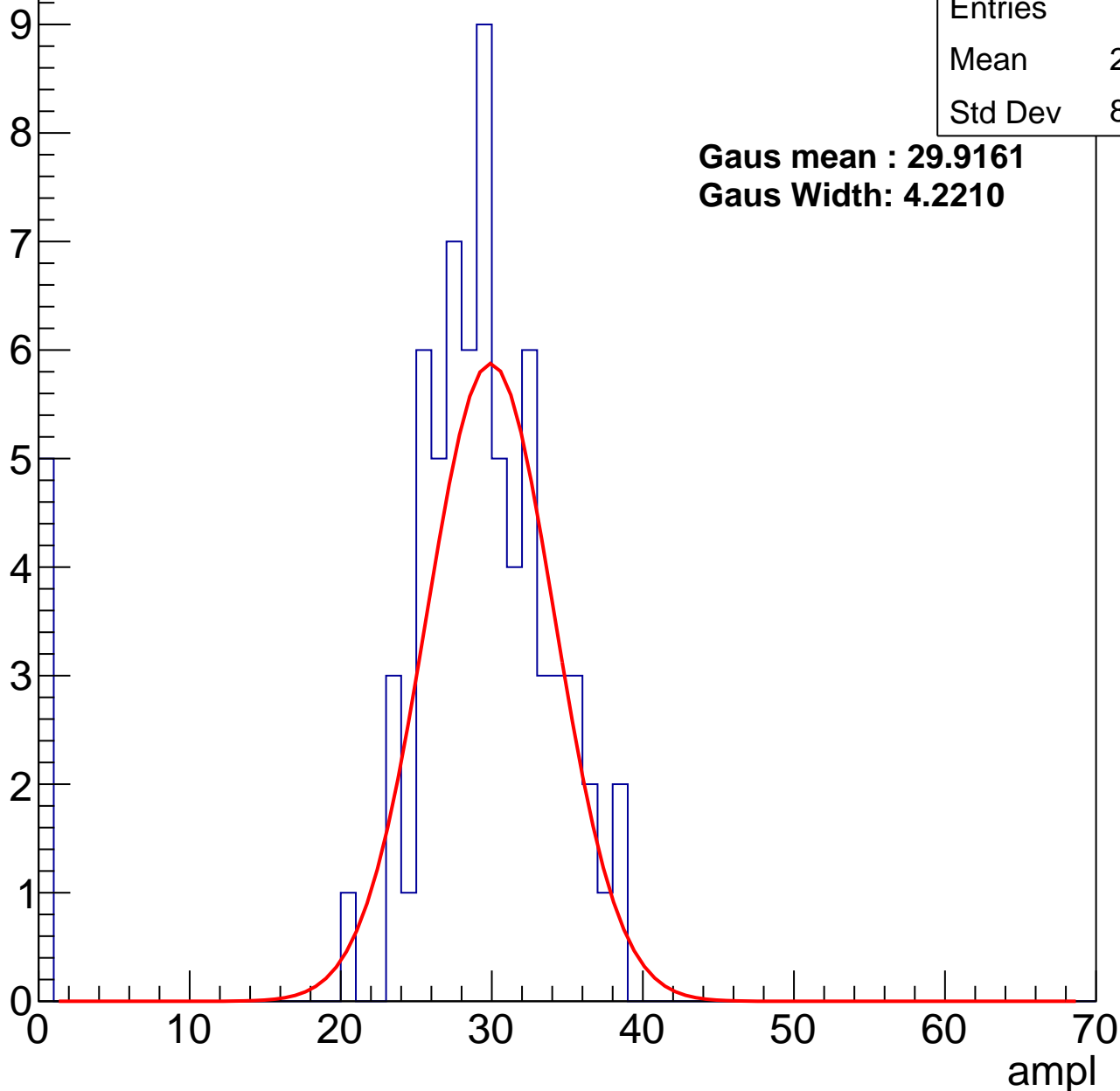
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	27.33
Std Dev	8.353

**Gaus mean : 29.9161**

**Gaus Width: 4.2210**



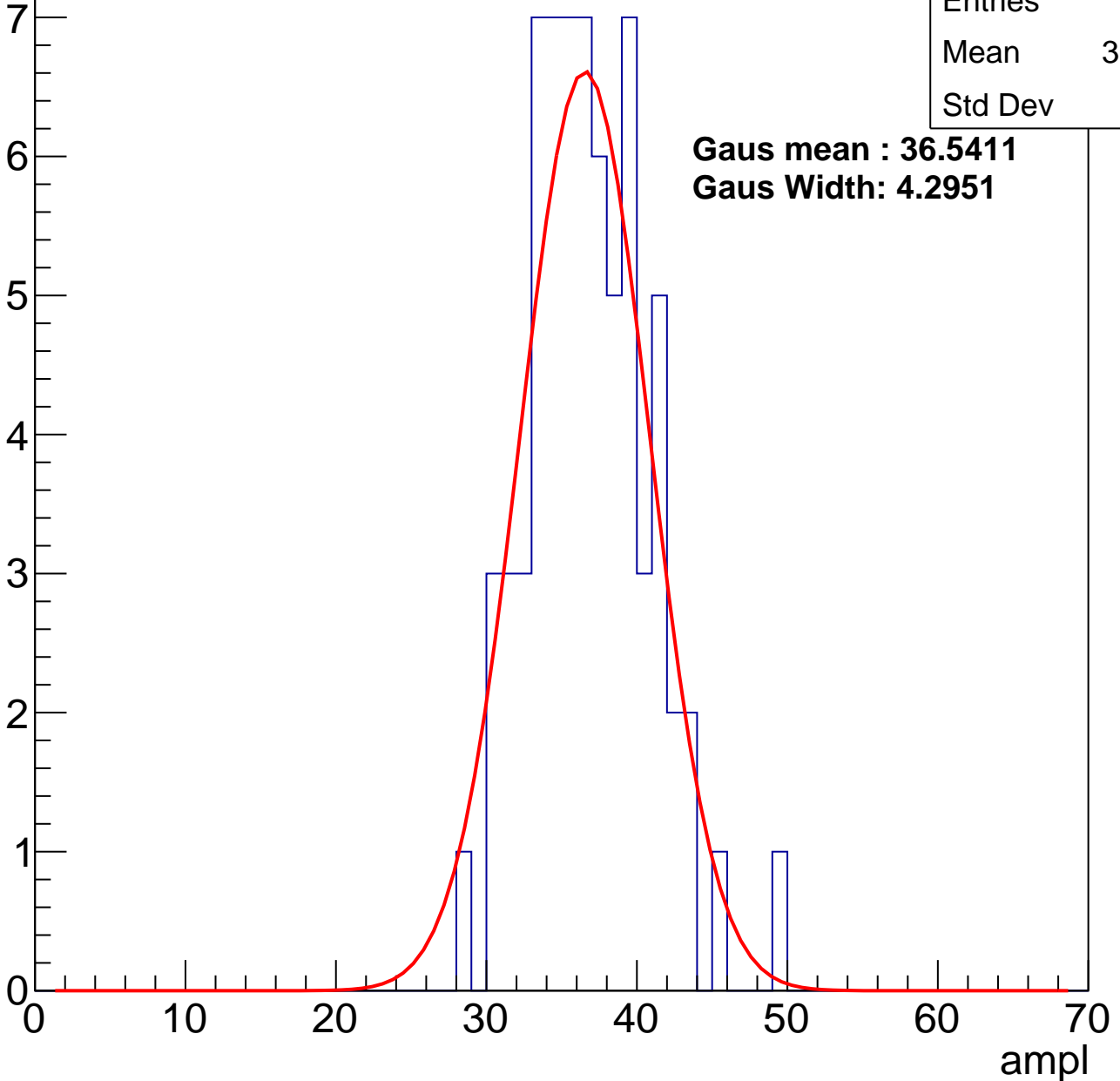
# B1L103S, U21-ch49, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	36.39
Std Dev	3.9

**Gaus mean : 36.5411**  
**Gaus Width: 4.2951**



# B1L103S, U21-ch49, adc2

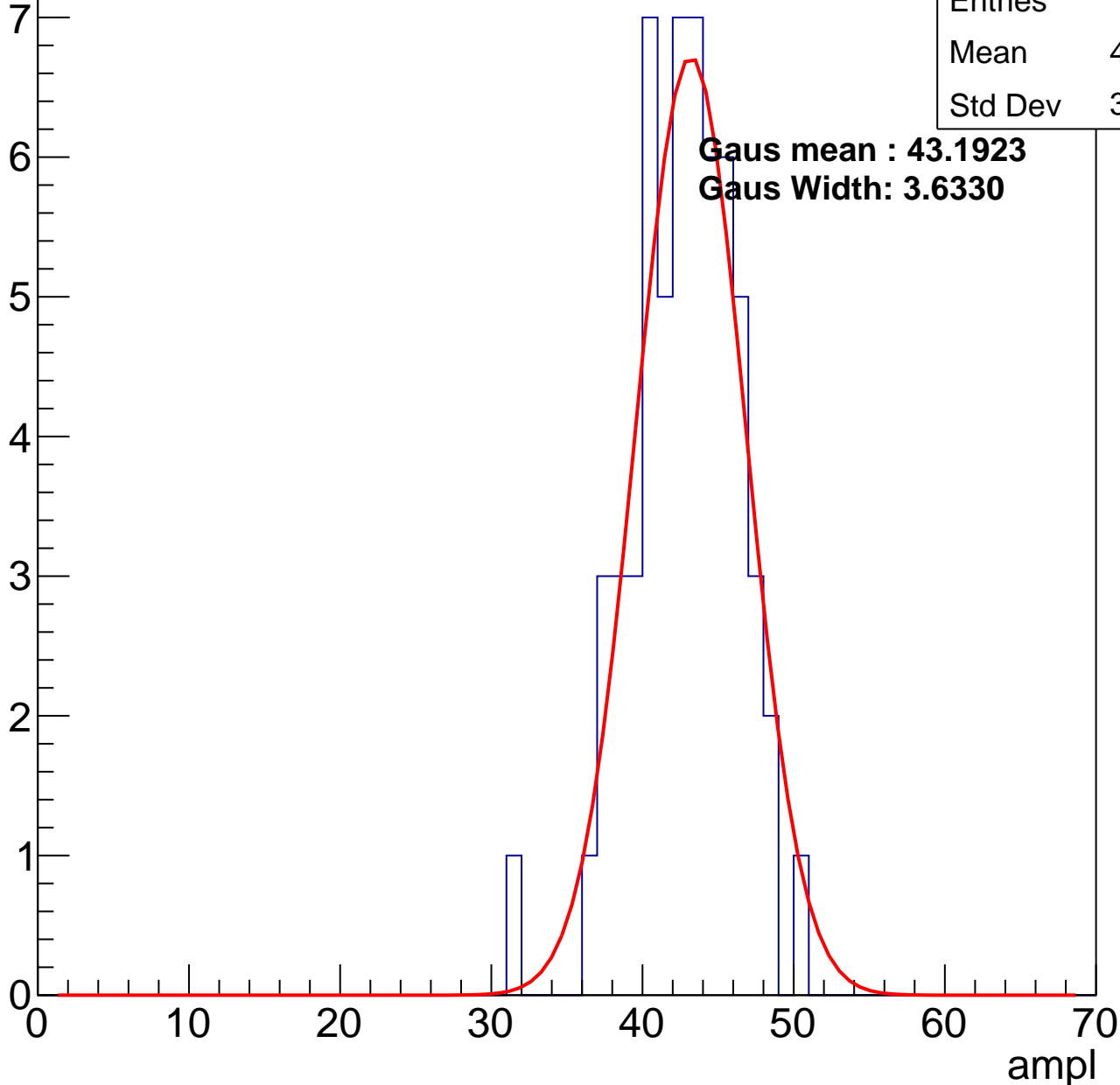
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	42.33
Std Dev	3.438

**Gaus mean : 43.1923**

**Gaus Width: 3.6330**

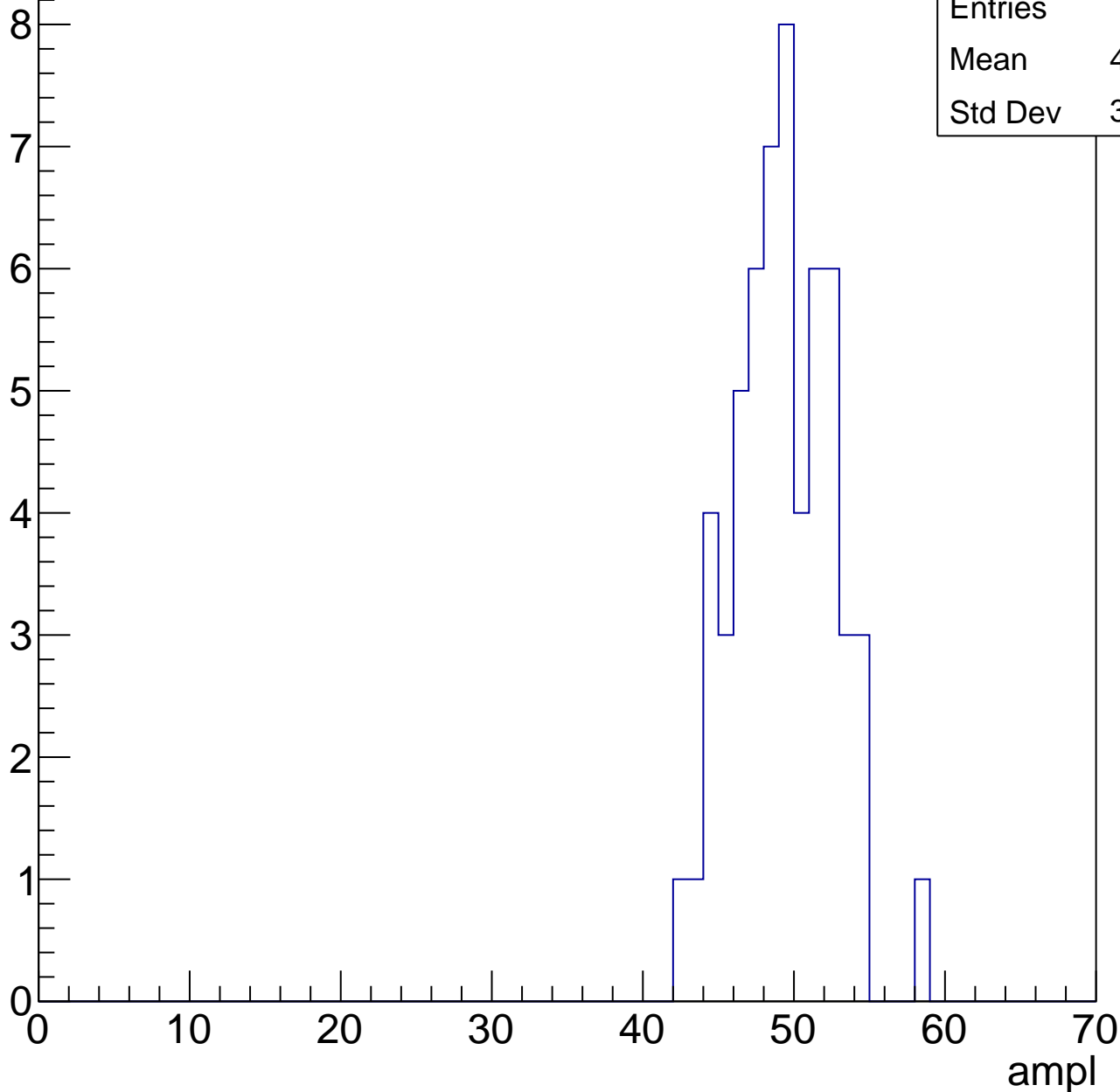


# B1L103S, U21-ch49, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	48.84
Std Dev	3.199

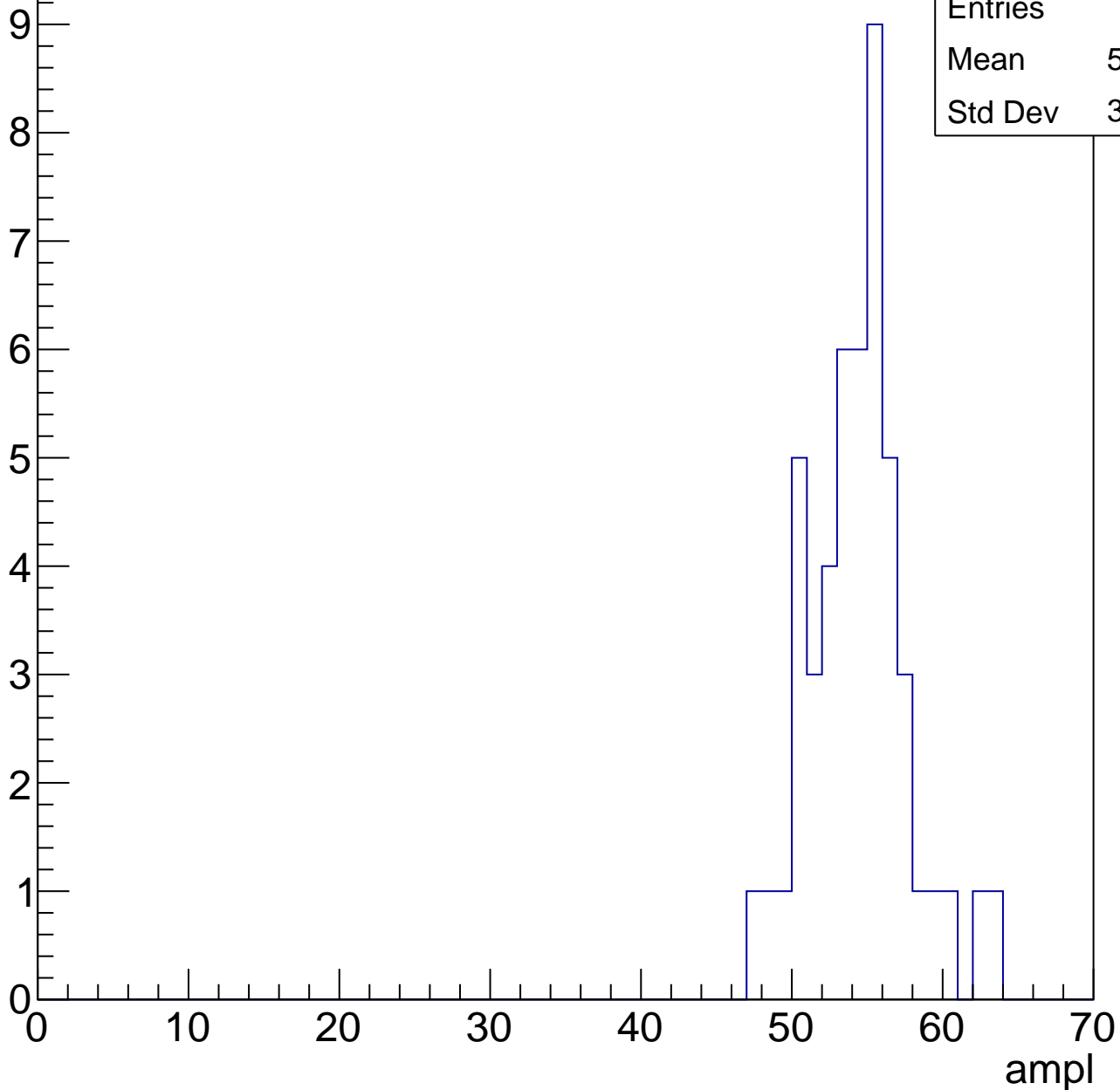


# B1L103S, U21-ch49, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	53.98
Std Dev	3.248



# B1L103S, U21-ch49, adc5

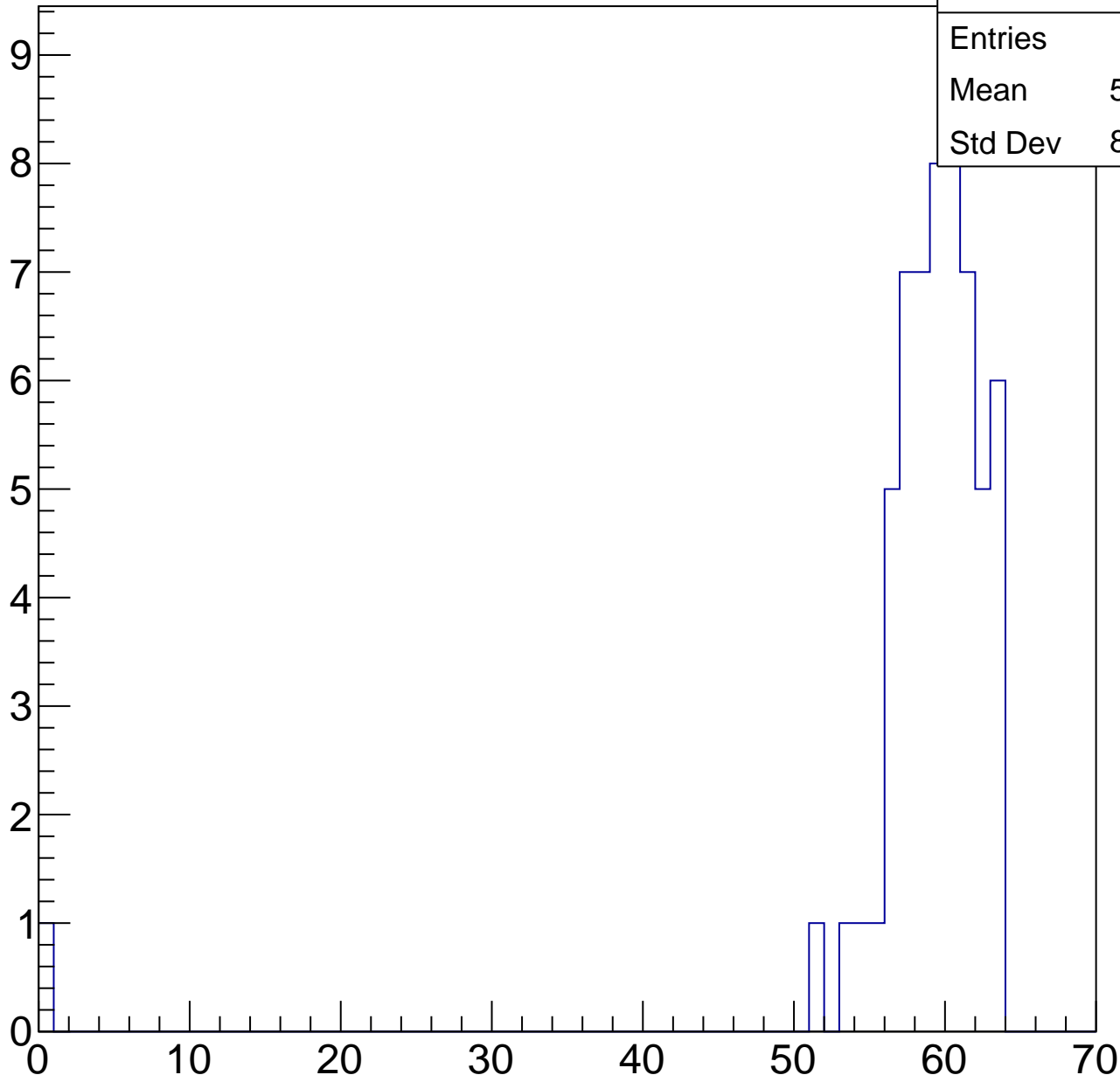
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	59
Mean	58.05
Std Dev	8.054

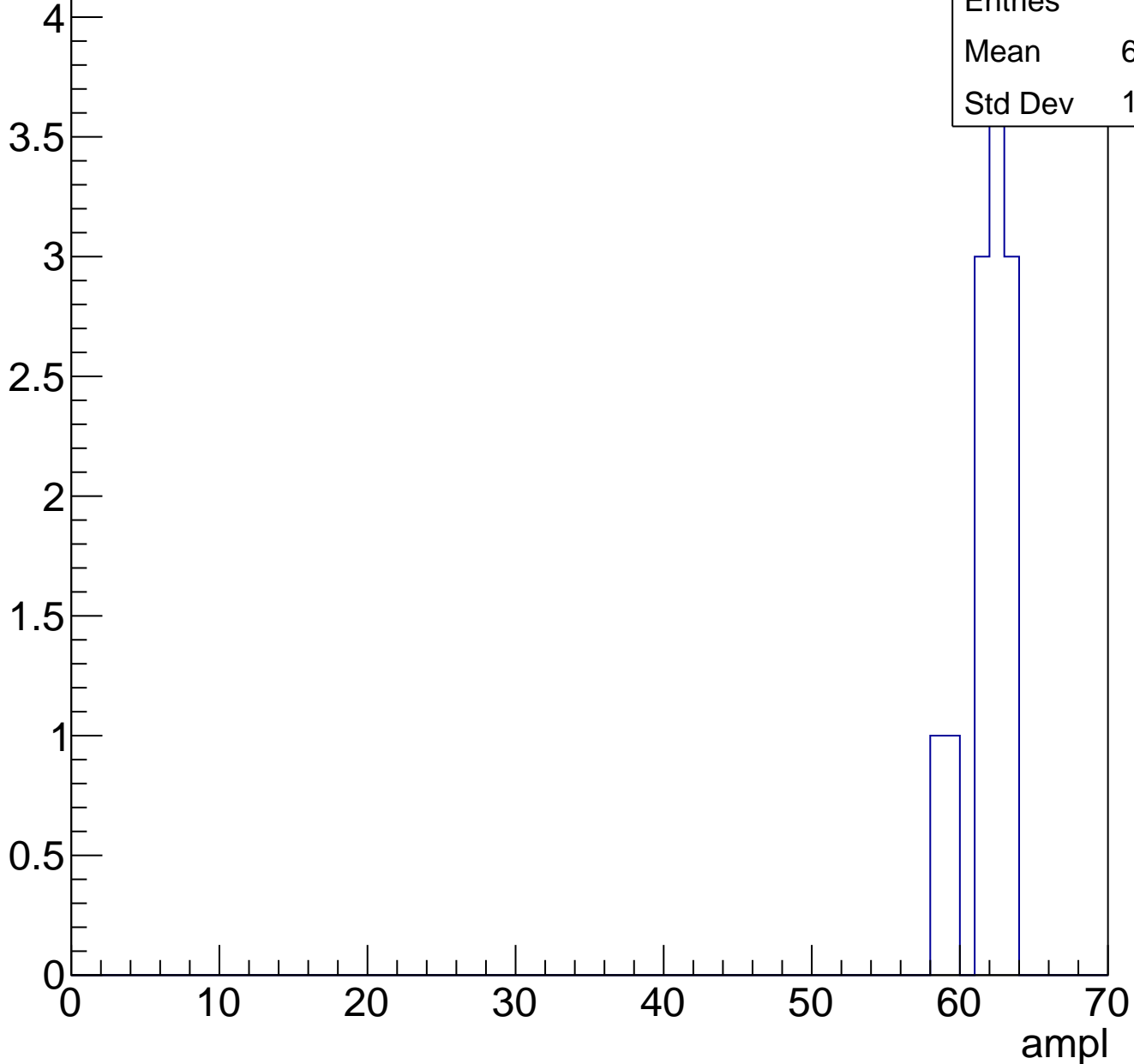
ampl



# B1L103S, U21-ch49, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U21-ch49, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U21-ch50, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	81
Mean	29.1
Std Dev	5.36

**Gaus mean : 29.4459**

**Gaus Width: 4.3781**

Entry

10  
8  
6  
4  
2  
0

ampl

0

10

20

30

40

50

60

70

# B1L103S, U21-ch50, adc1

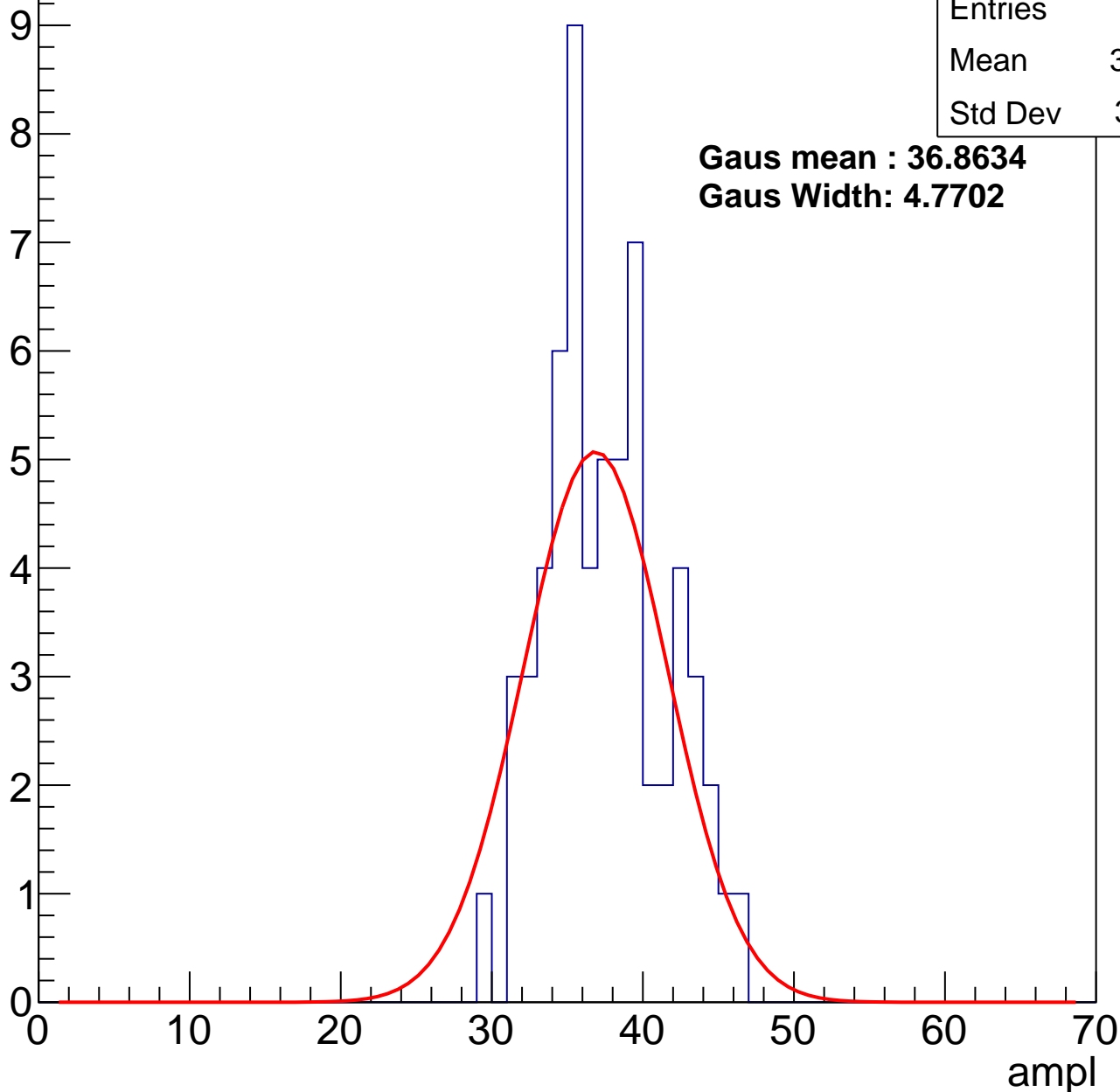
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	37.08
Std Dev	3.891

**Gaus mean : 36.8634**

**Gaus Width: 4.7702**



# B1L103S, U21-ch50, adc2

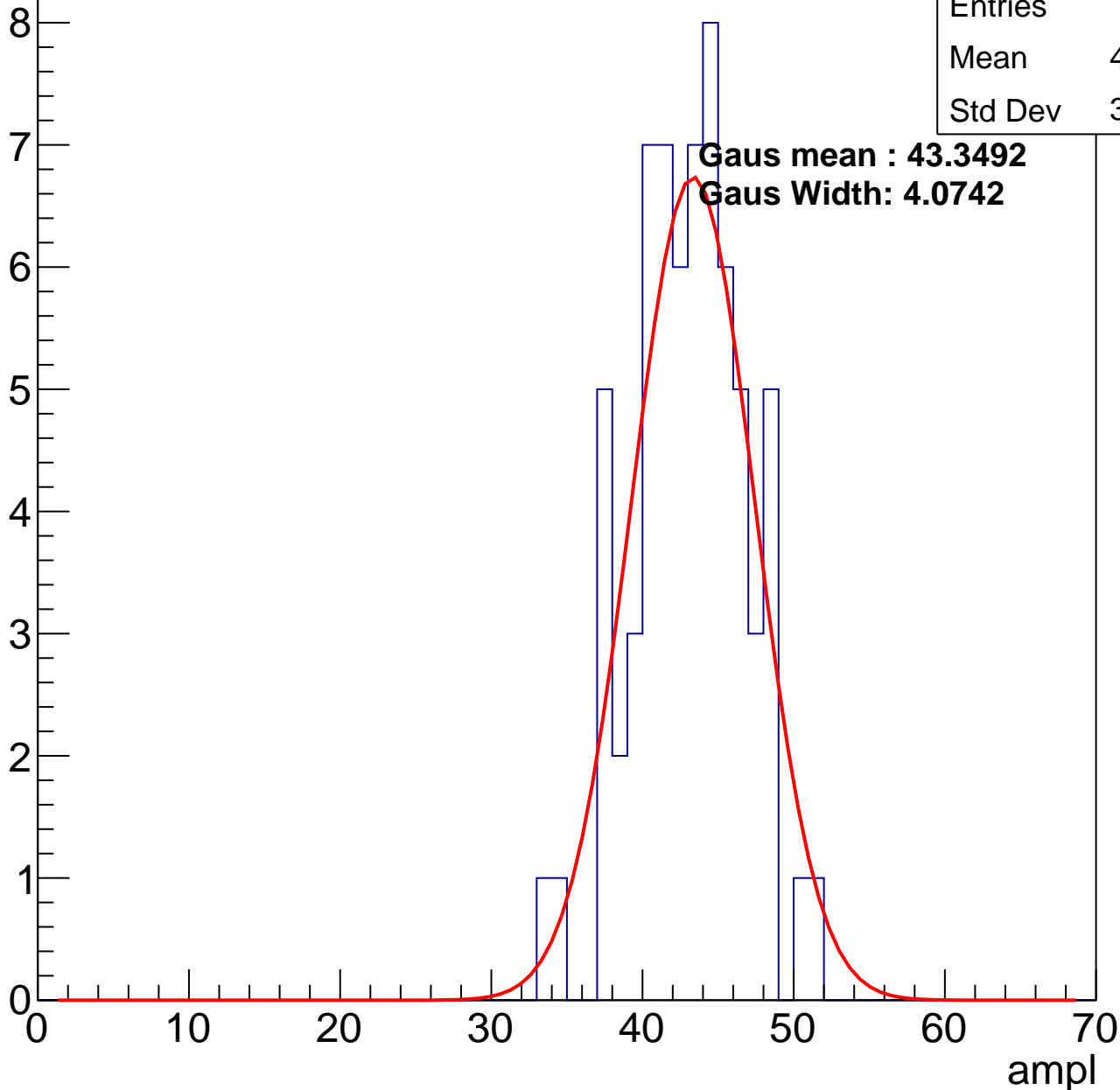
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	42.63
Std Dev	3.658

**Gaus mean : 43.3492**

**Gaus Width: 4.0742**

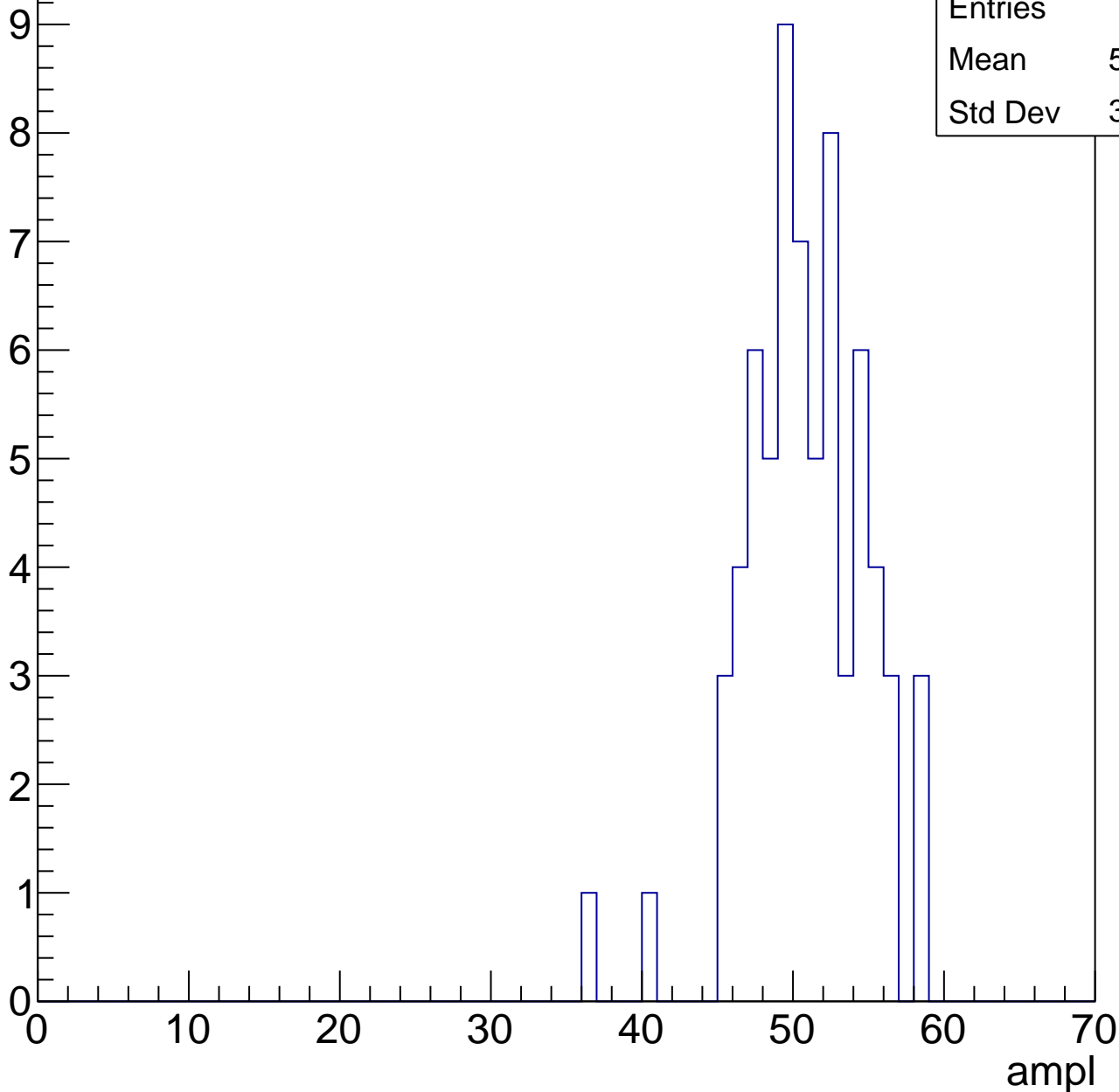


# B1L103S, U21-ch50, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	50.35
Std Dev	3.966

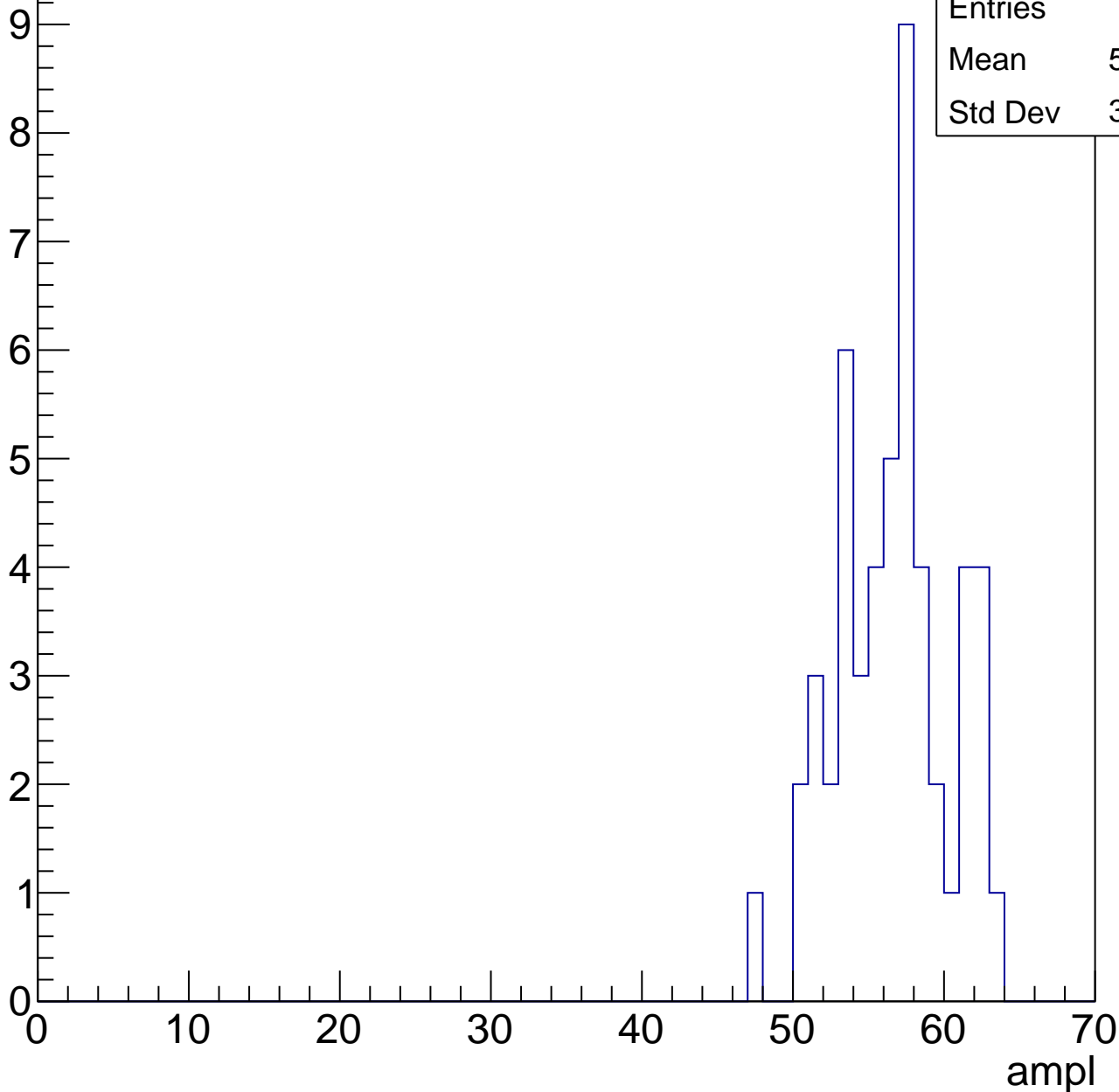


# B1L103S, U21-ch50, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	56.12
Std Dev	3.655



# B1L103S, U21-ch50, adc5

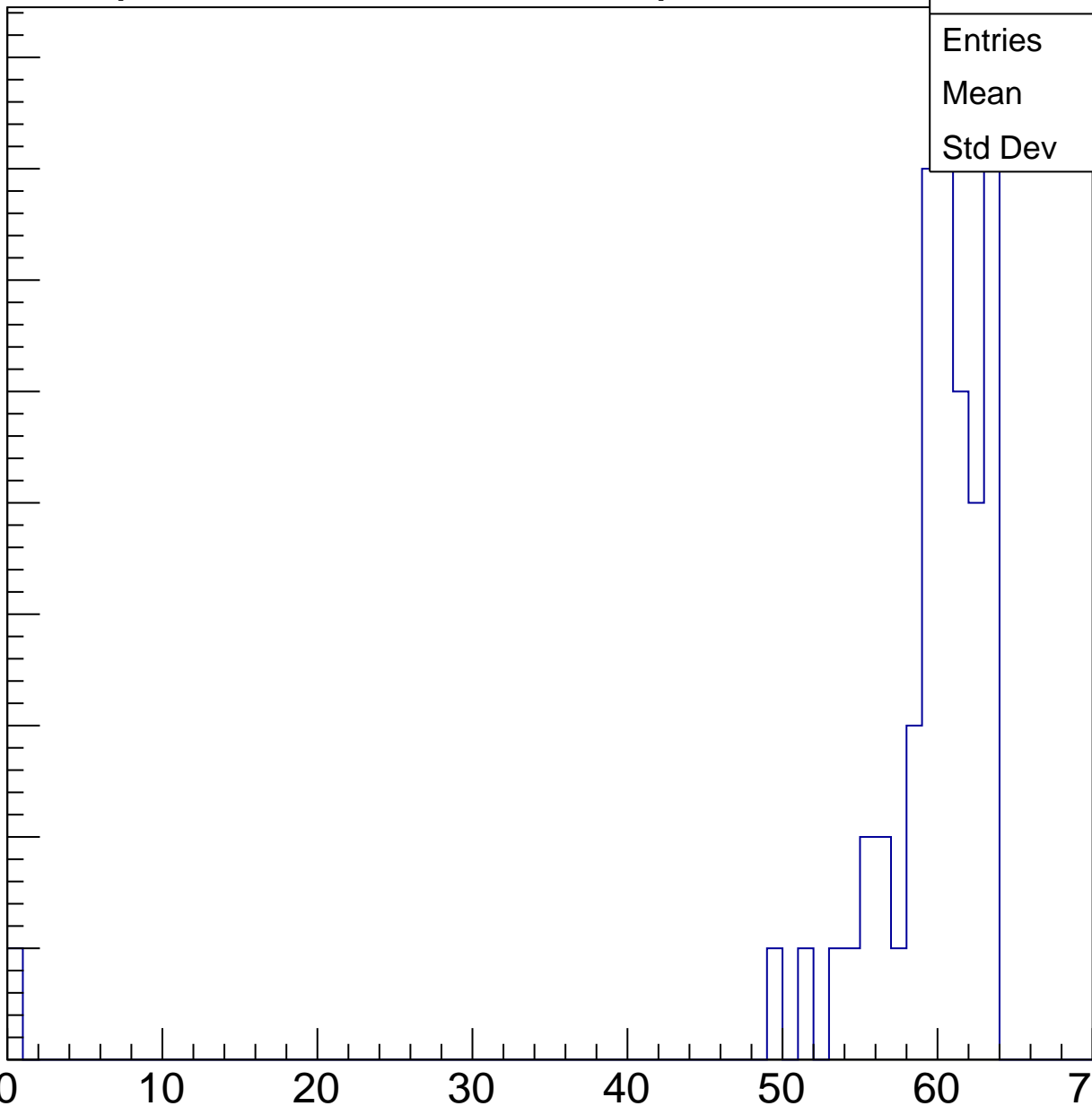
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	49
Mean	58.2
Std Dev	8.965

ampl



# B1L103S, U21-ch50, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



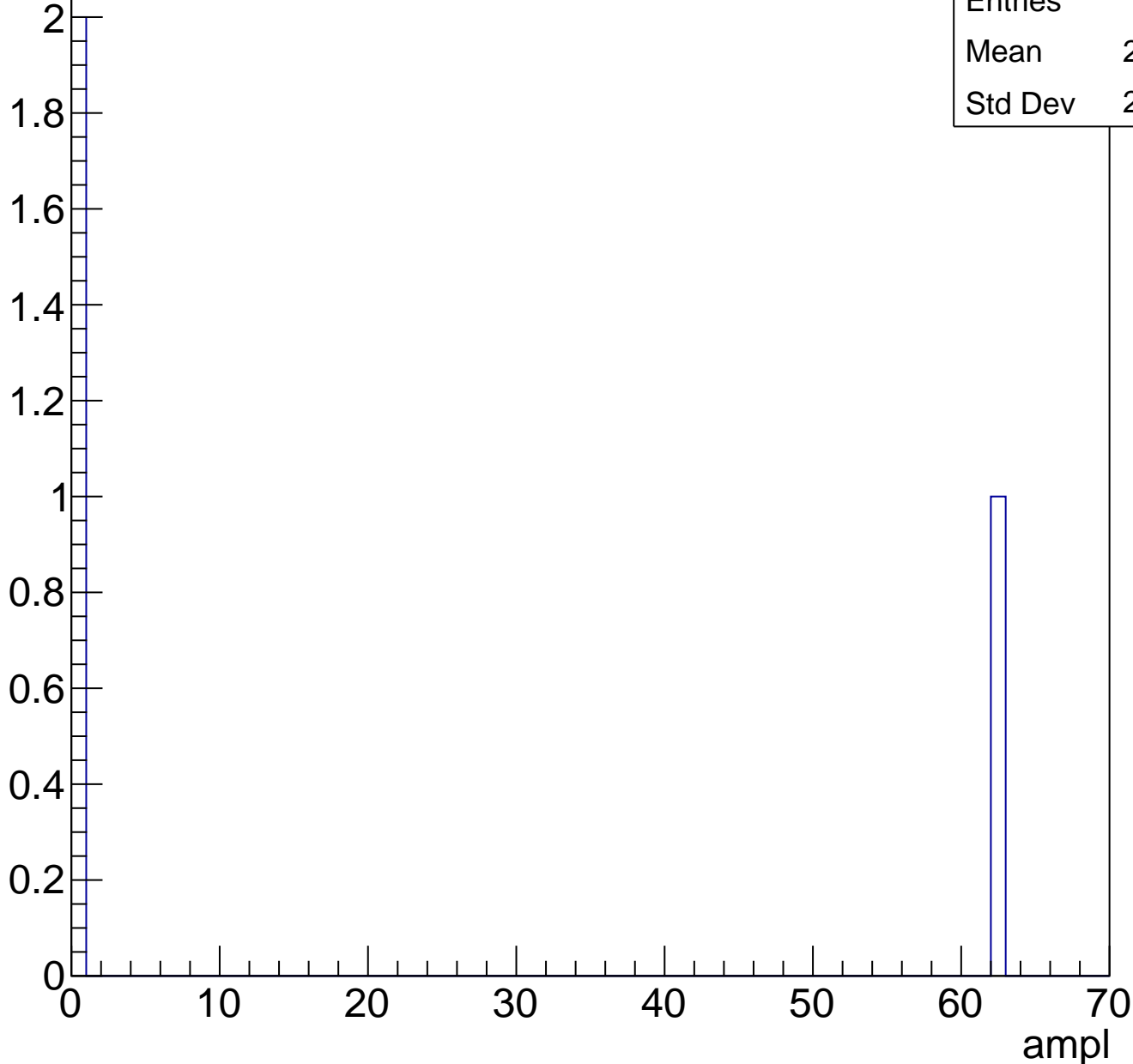
Entries	1
Mean	63
Std Dev	0



# B1L103S, U21-ch50, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	3
Mean	20.67
Std Dev	29.23

# B1L103S, U21-ch51, adc0

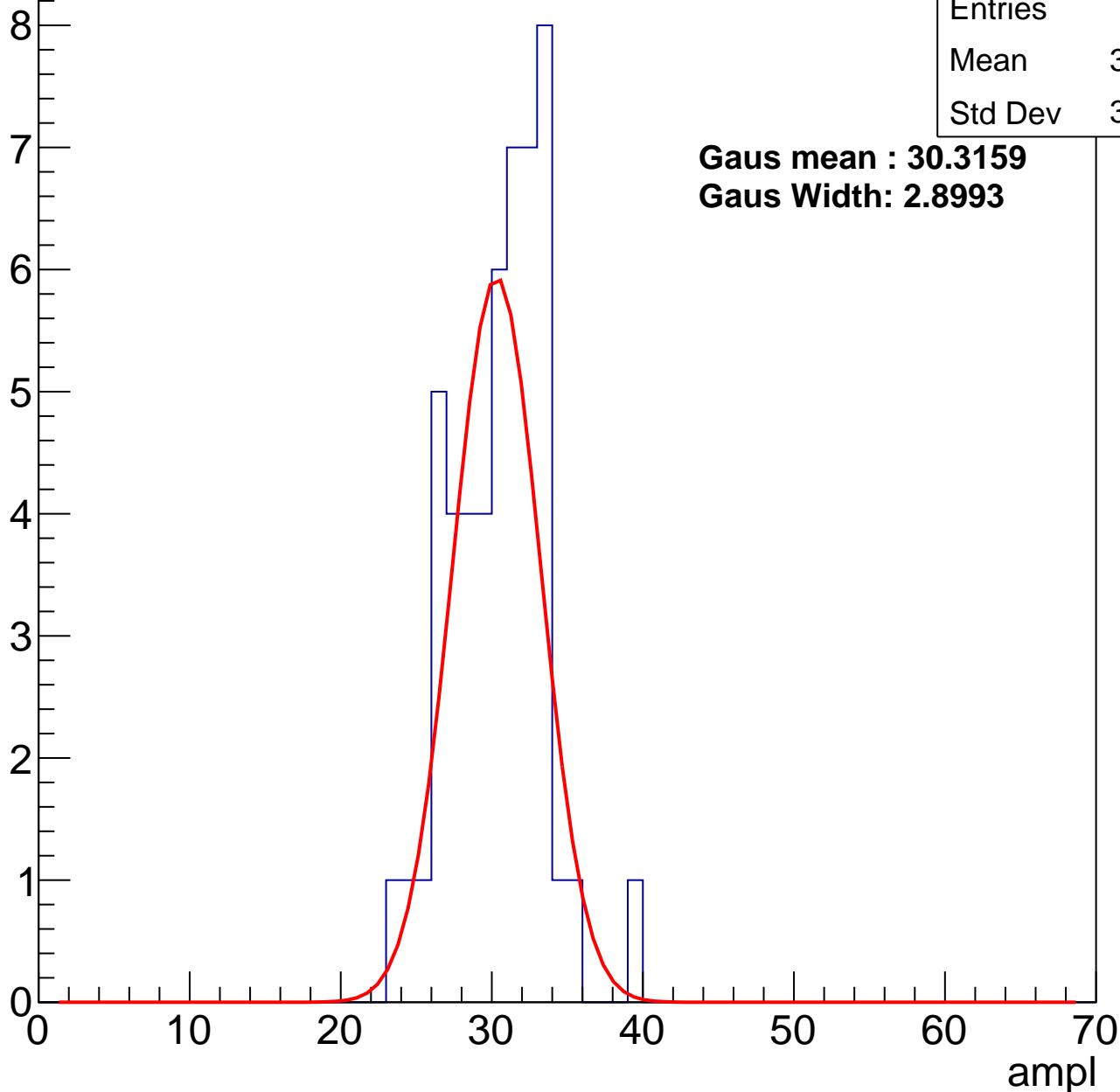
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	30.02
Std Dev	3.052

**Gaus mean : 30.3159**

**Gaus Width: 2.8993**



# B1L103S, U21-ch51, adc1

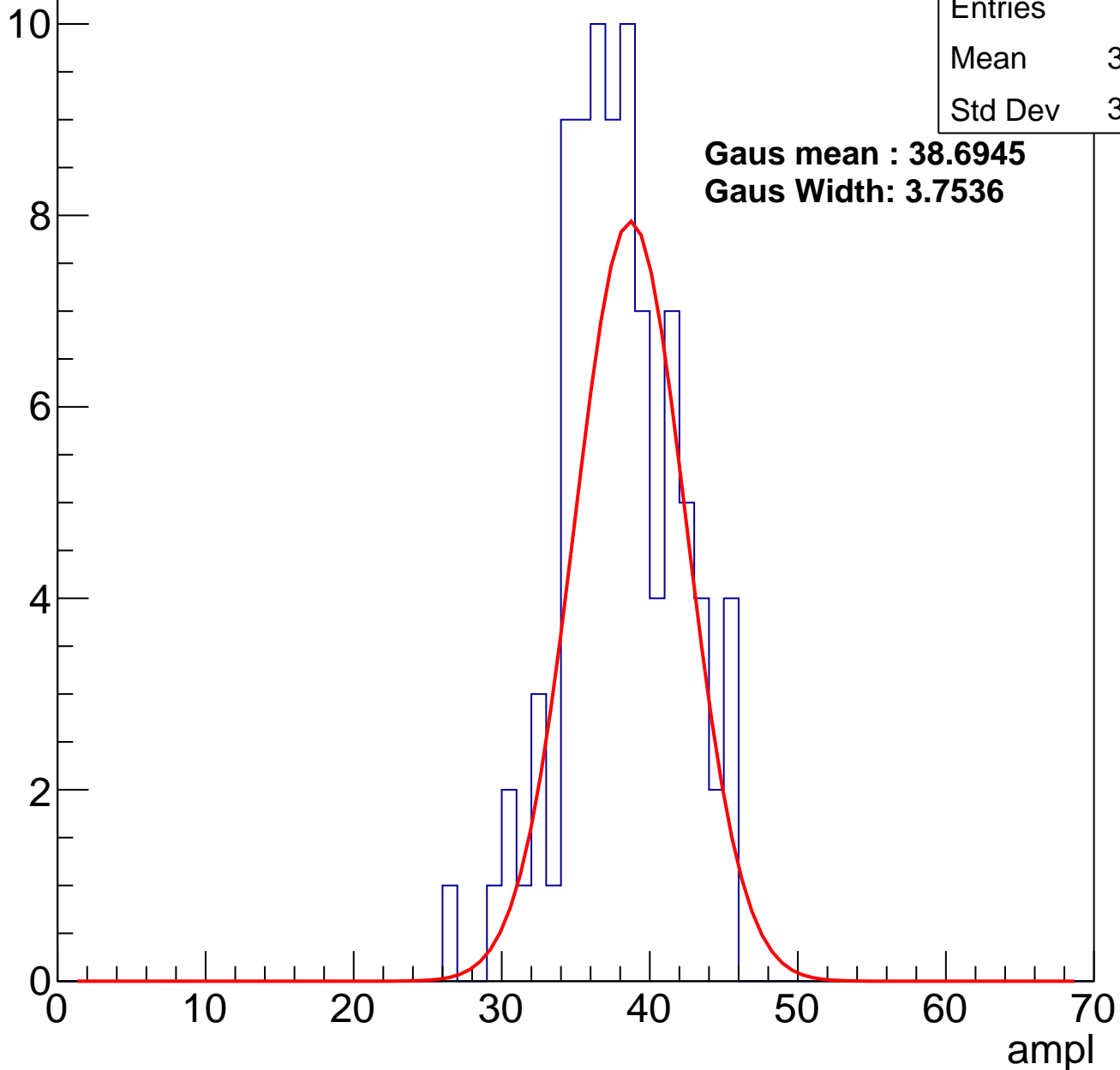
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	89
Mean	37.52
Std Dev	3.854

**Gaus mean : 38.6945**

**Gaus Width: 3.7536**

Entry



# B1L103S, U21-ch51, adc2

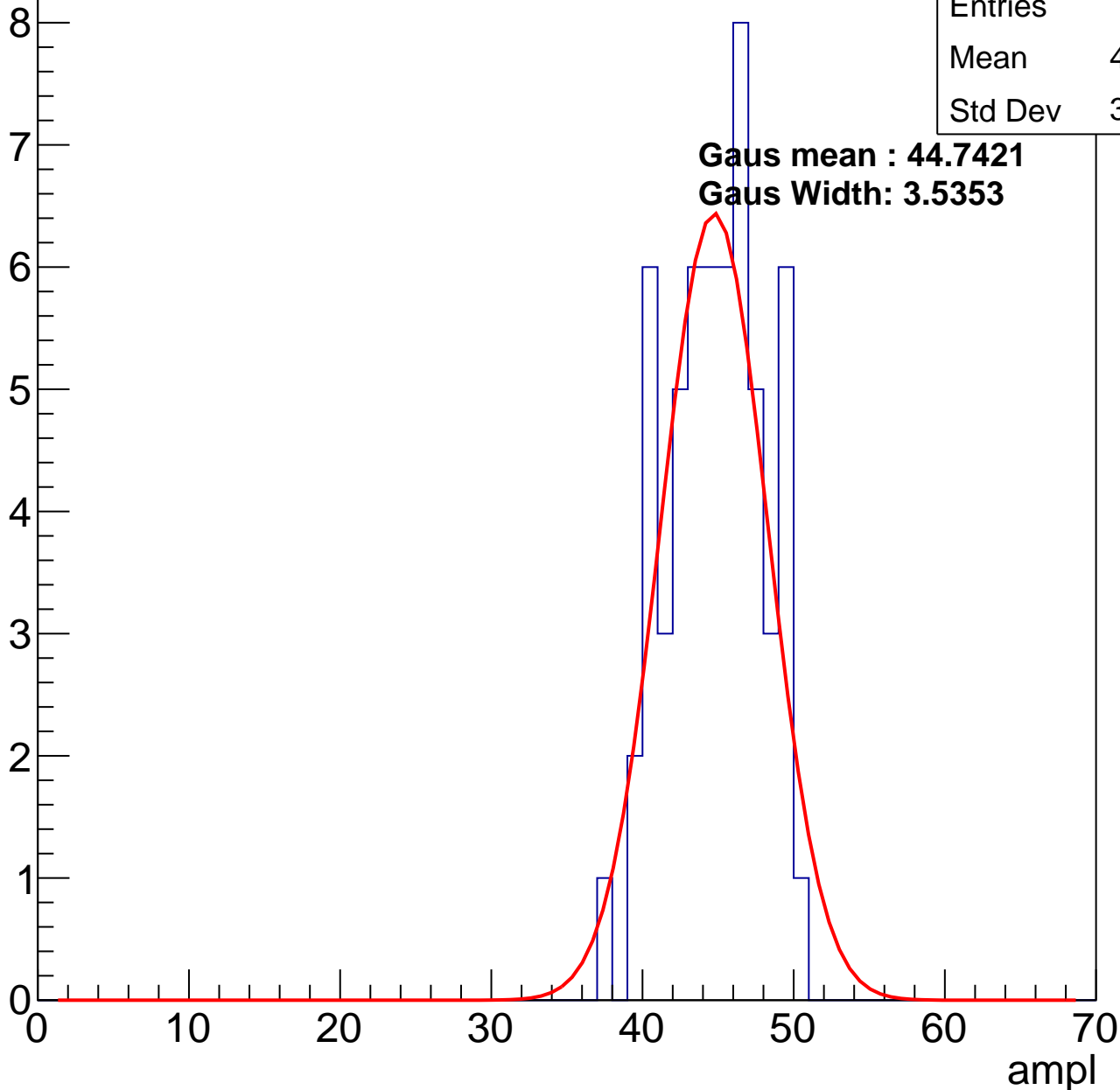
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	44.33
Std Dev	3.104

**Gaus mean : 44.7421**

**Gaus Width: 3.5353**



# B1L103S, U21-ch51, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	62
Mean	50.97
Std Dev	3.121

Entry

10

8

6

4

2

0

0

10

20

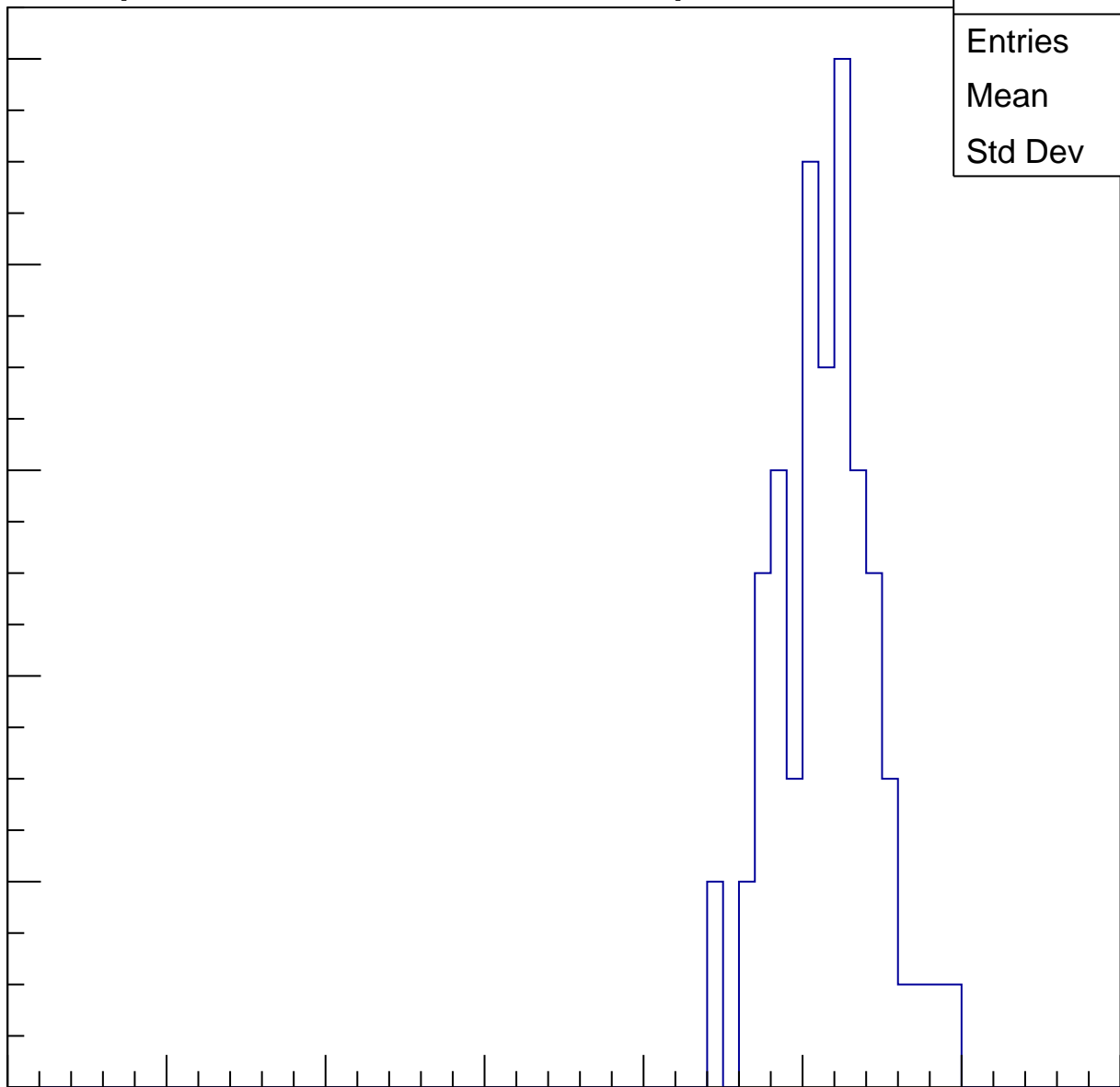
30

40

50

60

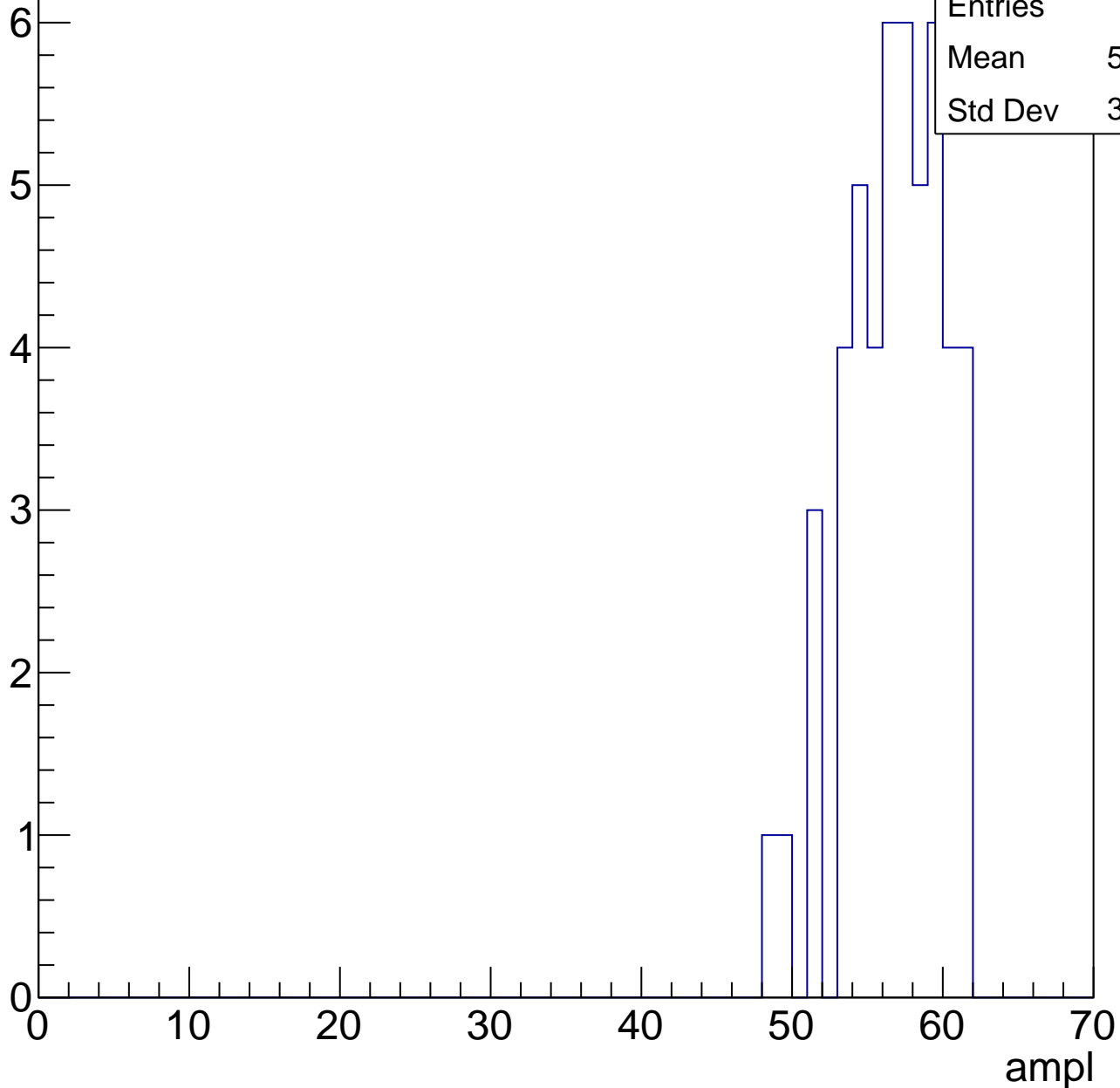
ampl



# B1L103S, U21-ch51, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



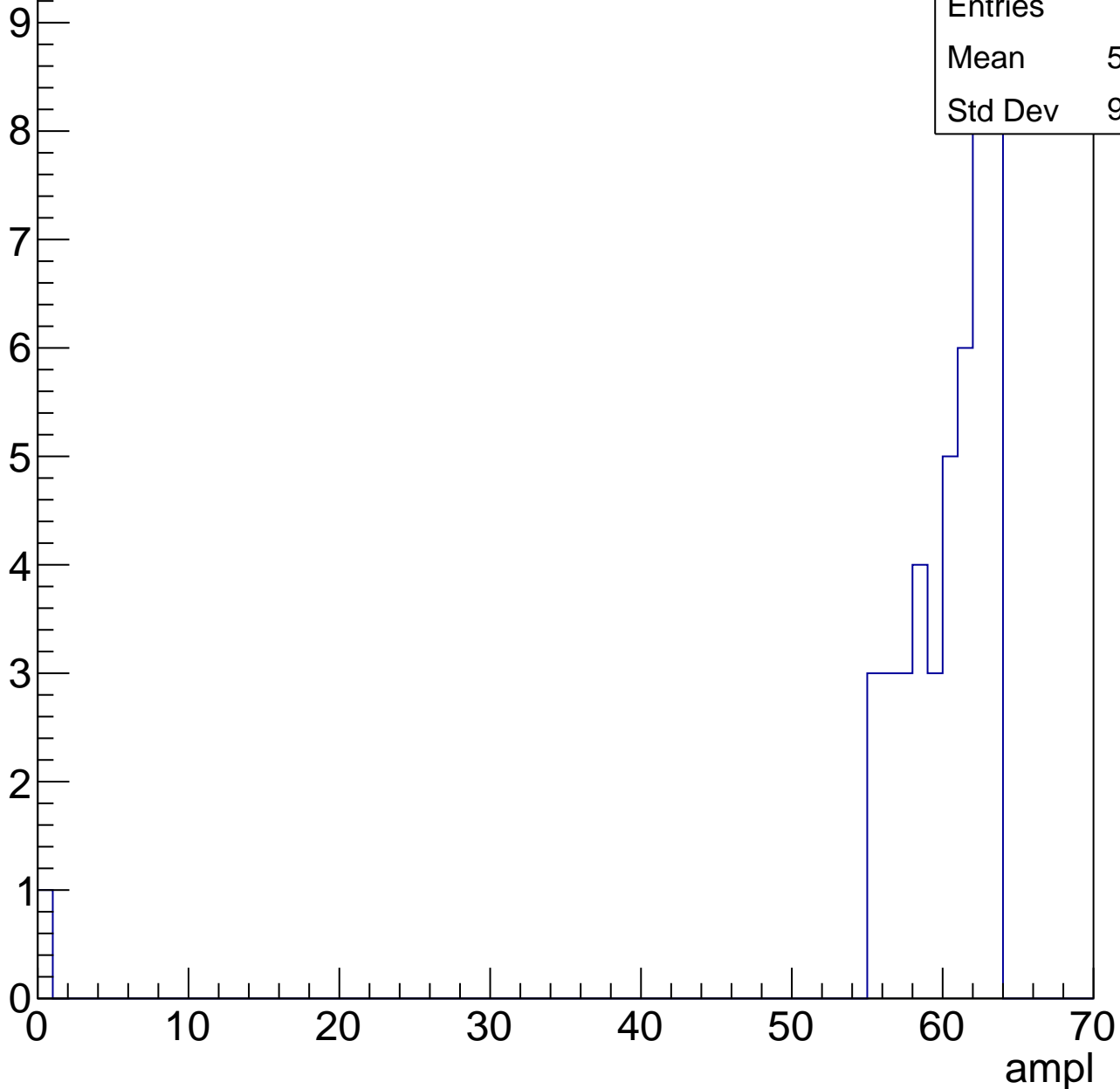
Entries	49
Mean	56.29
Std Dev	3.156

# B1L103S, U21-ch51, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	45
Mean	58.69
Std Dev	9.196



# B1L103S, U21-ch51, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U21-ch51, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U21-ch52, adc0

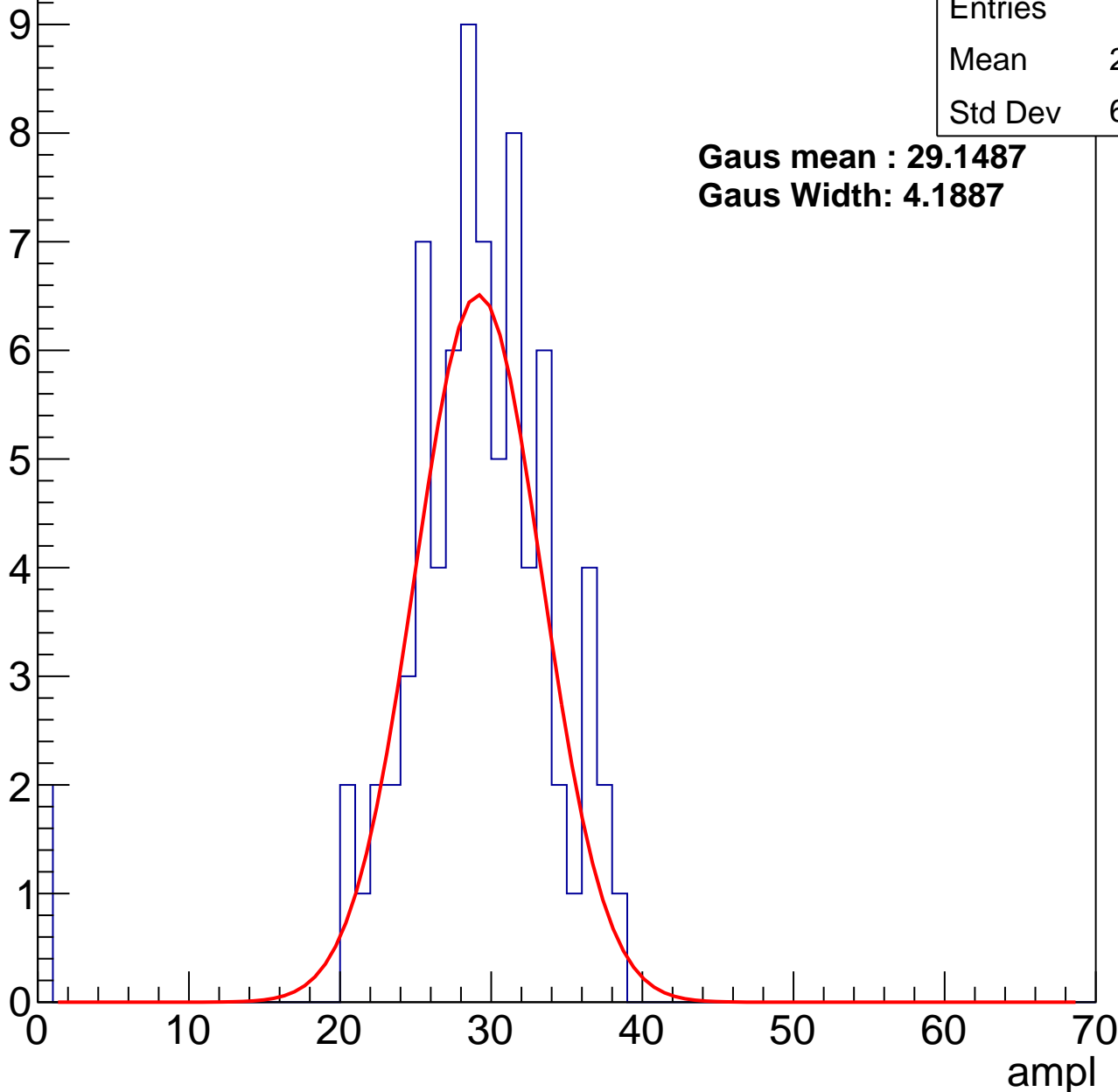
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	28.23
Std Dev	6.148

**Gaus mean : 29.1487**

**Gaus Width: 4.1887**



# B1L103S, U21-ch52, adc1

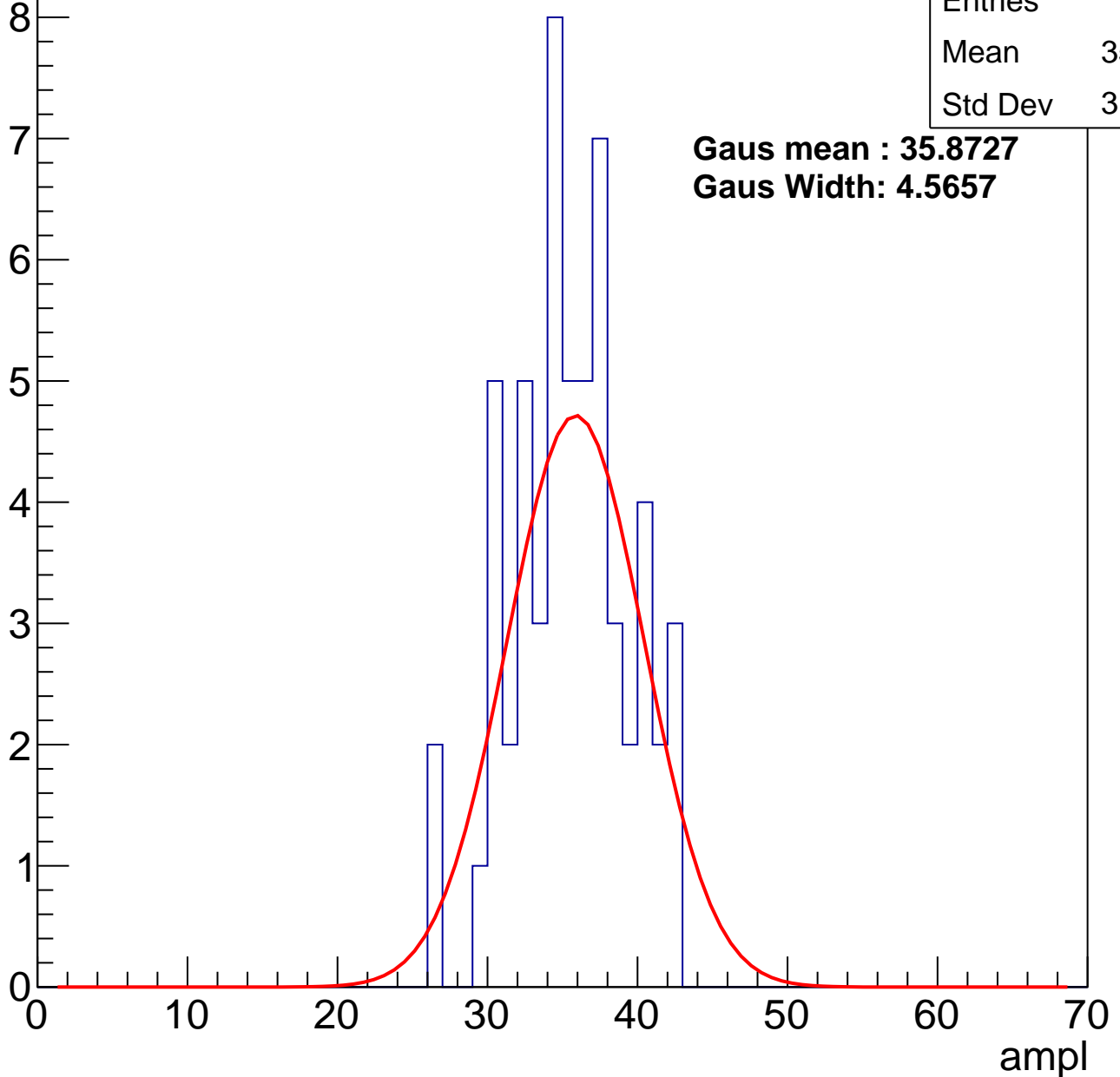
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	35.05
Std Dev	3.818

**Gaus mean : 35.8727**

**Gaus Width: 4.5657**



# B1L103S, U21-ch52, adc2

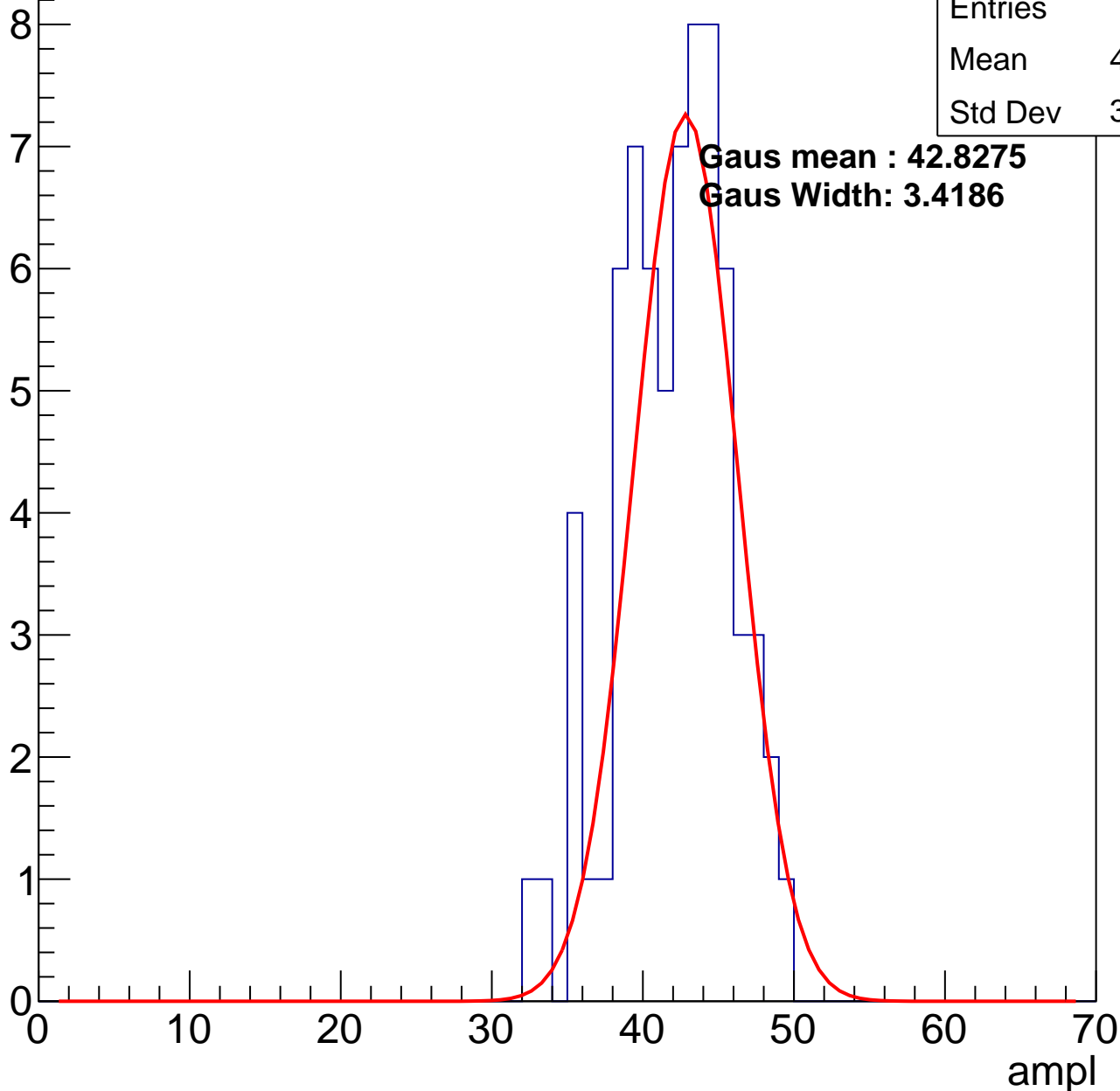
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	41.54
Std Dev	3.683

**Gaus mean : 42.8275**

**Gaus Width: 3.4186**

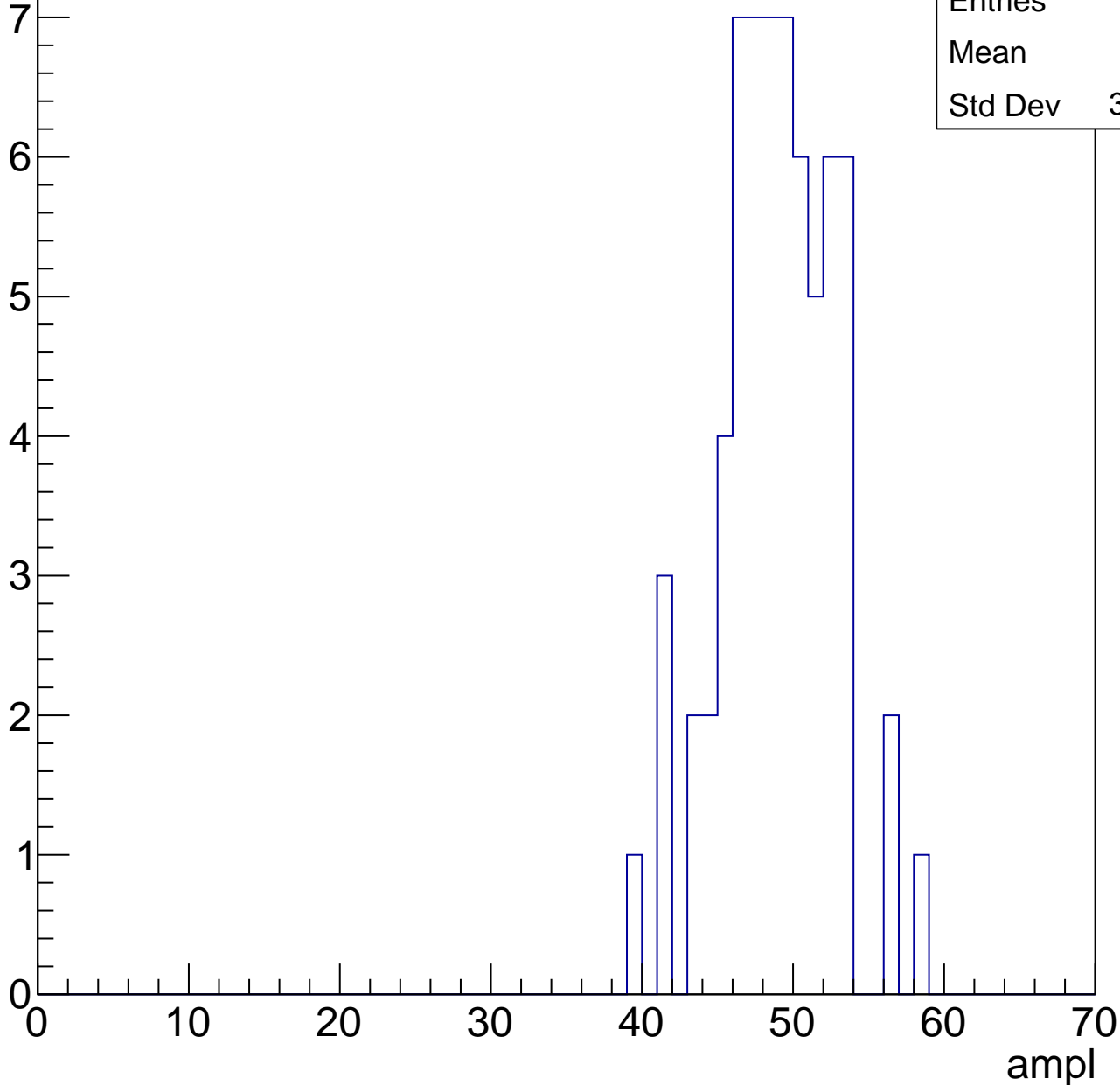


# B1L103S, U21-ch52, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	48.5
Std Dev	3.722

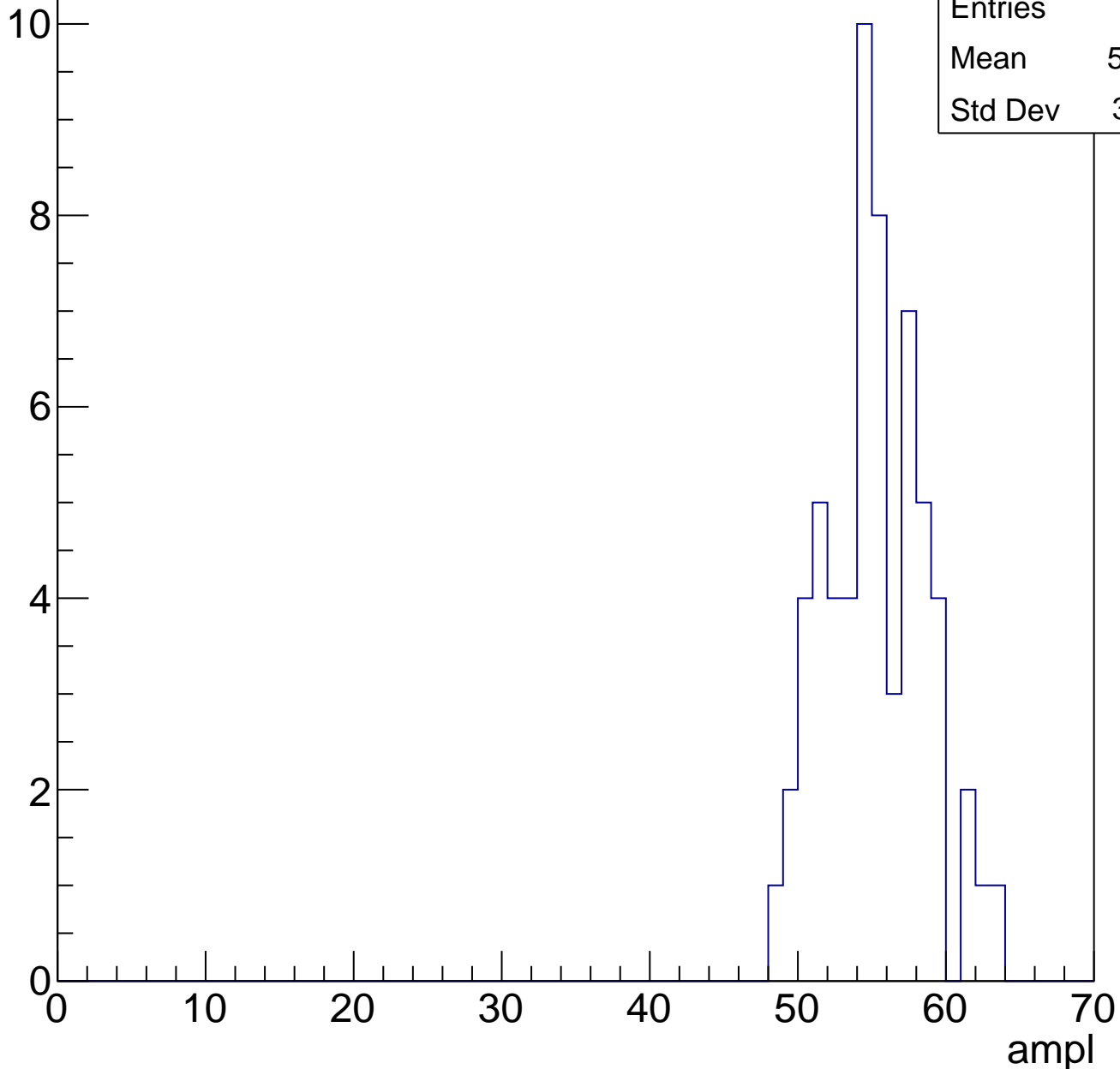


# B1L103S, U21-ch52, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	61
Mean	54.77
Std Dev	3.351

Entry

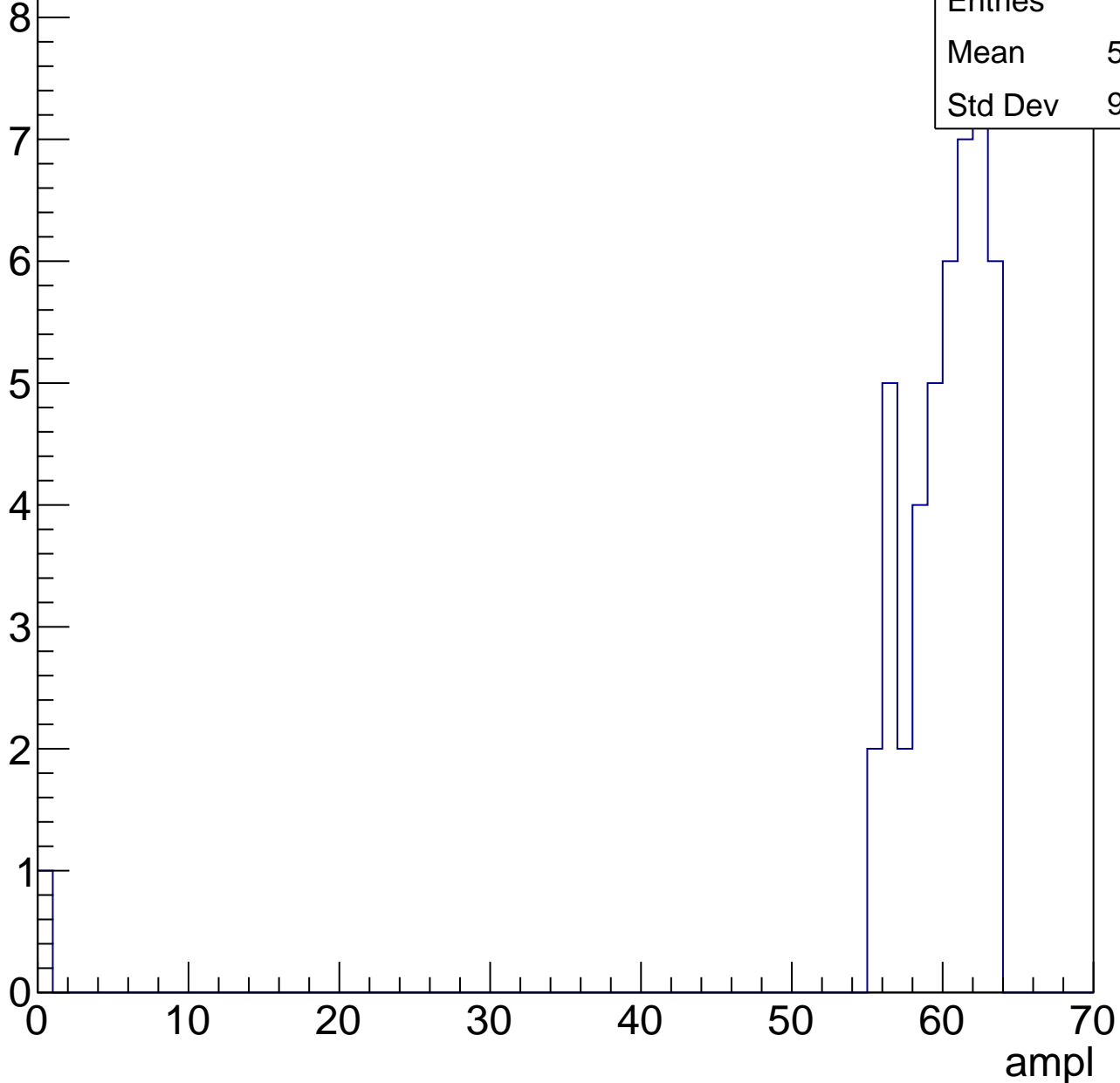


# B1L103S, U21-ch52, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

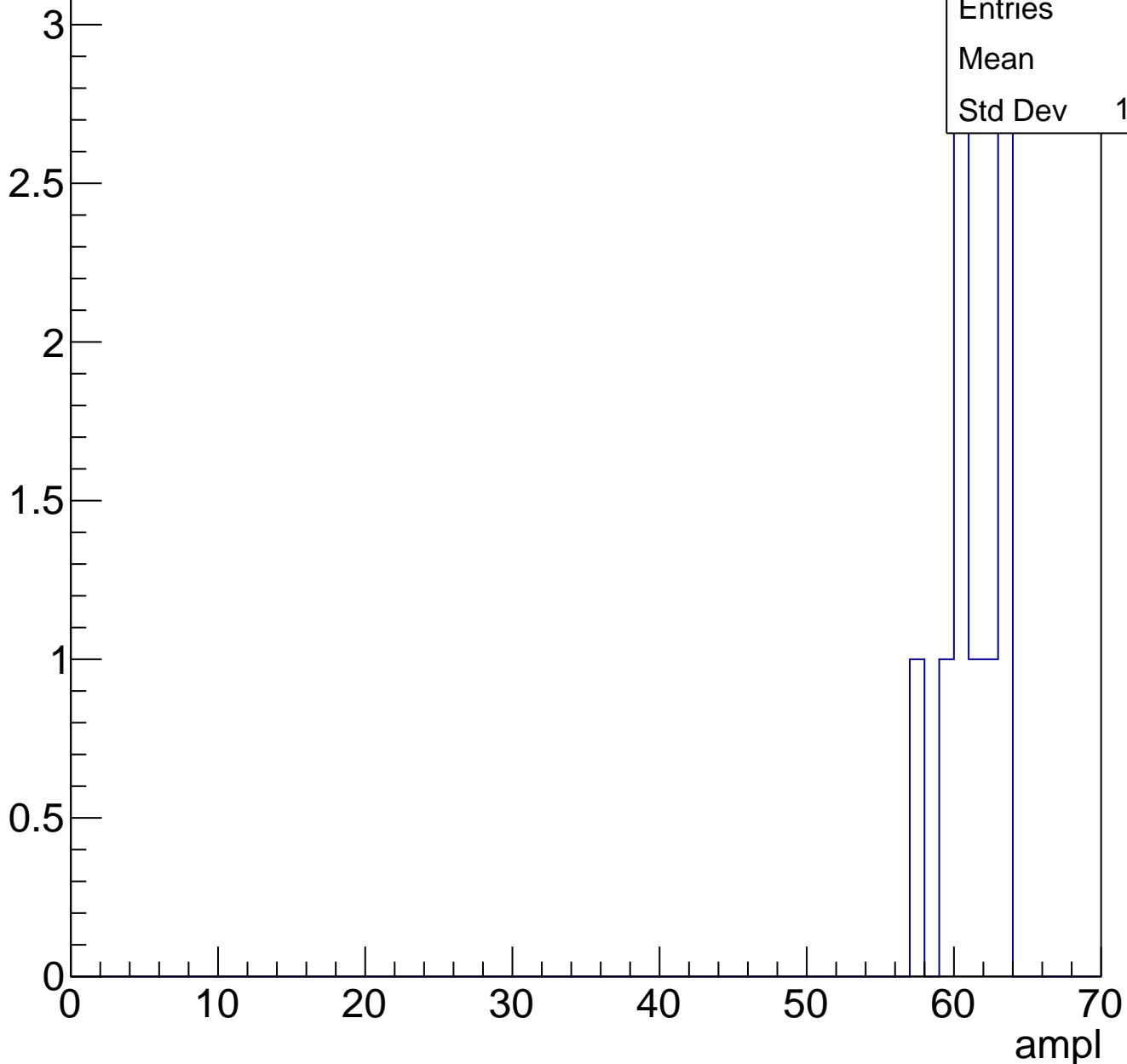
Entries	46
Mean	58.52
Std Dev	9.043



# B1L103S, U21-ch52, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

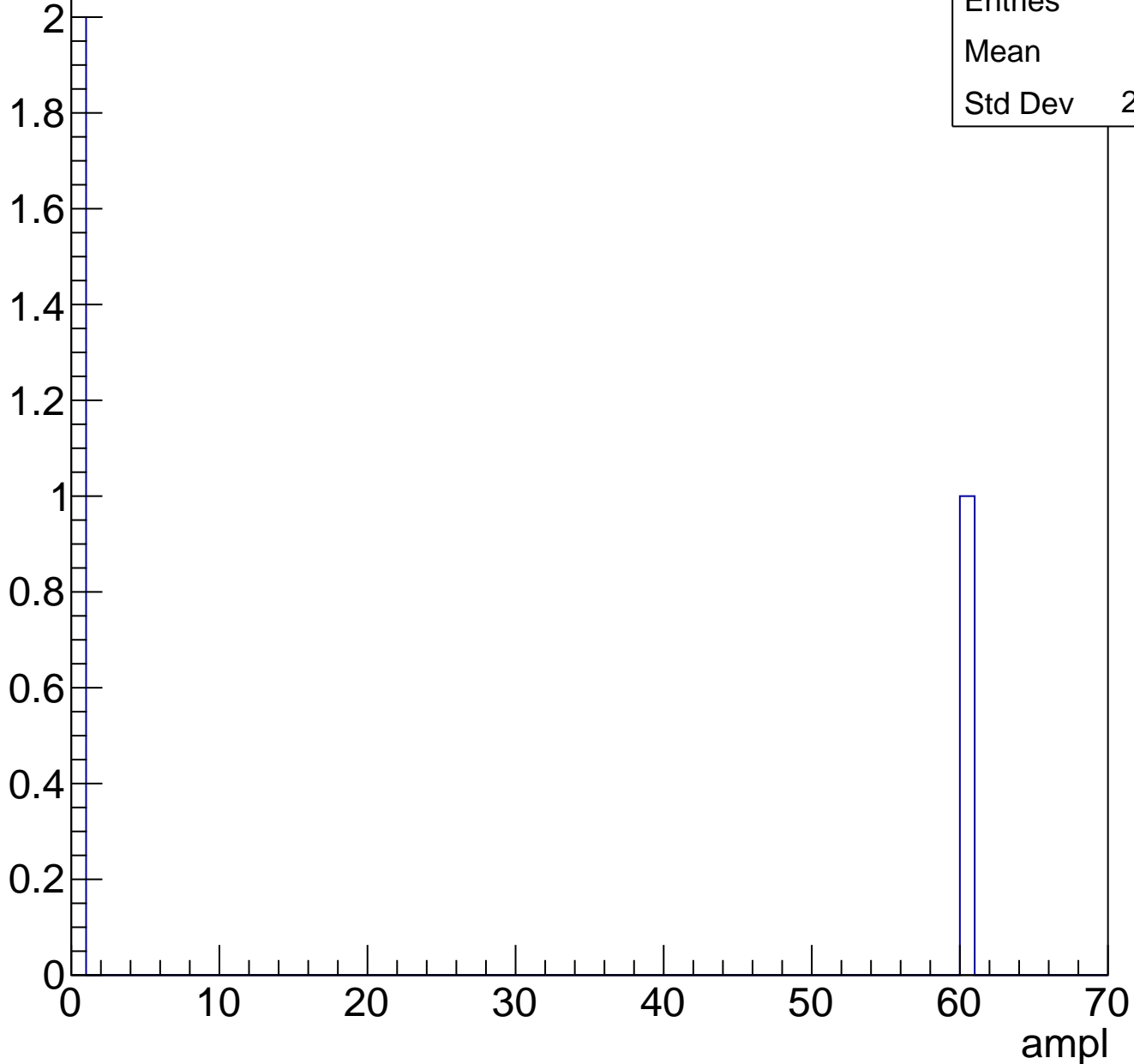




# B1L103S, U21-ch52, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	3
Mean	20
Std Dev	28.28

# B1L103S, U21-ch53, adc0

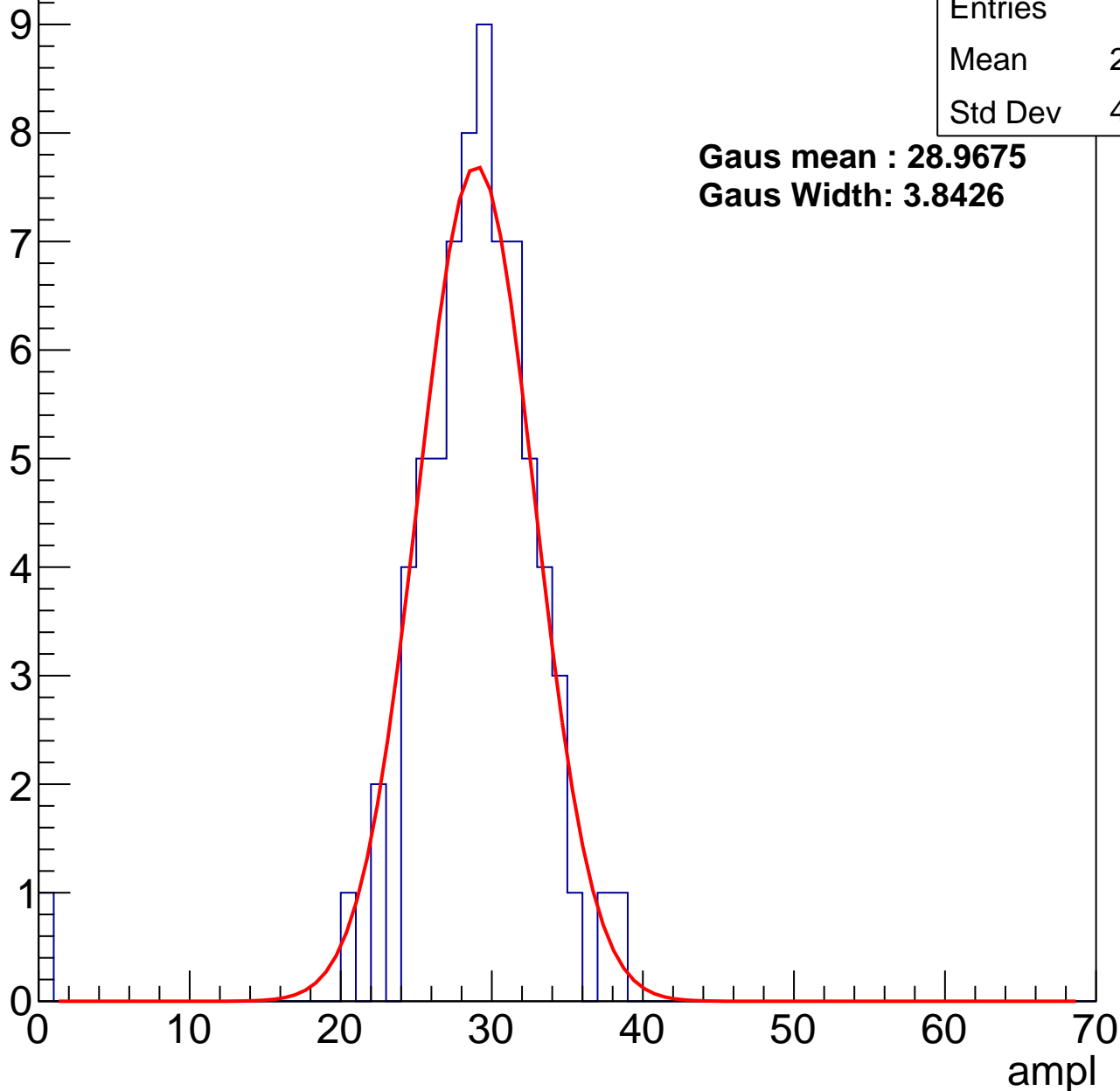
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	28.45
Std Dev	4.835

**Gaus mean : 28.9675**

**Gaus Width: 3.8426**



# B1L103S, U21-ch53, adc1

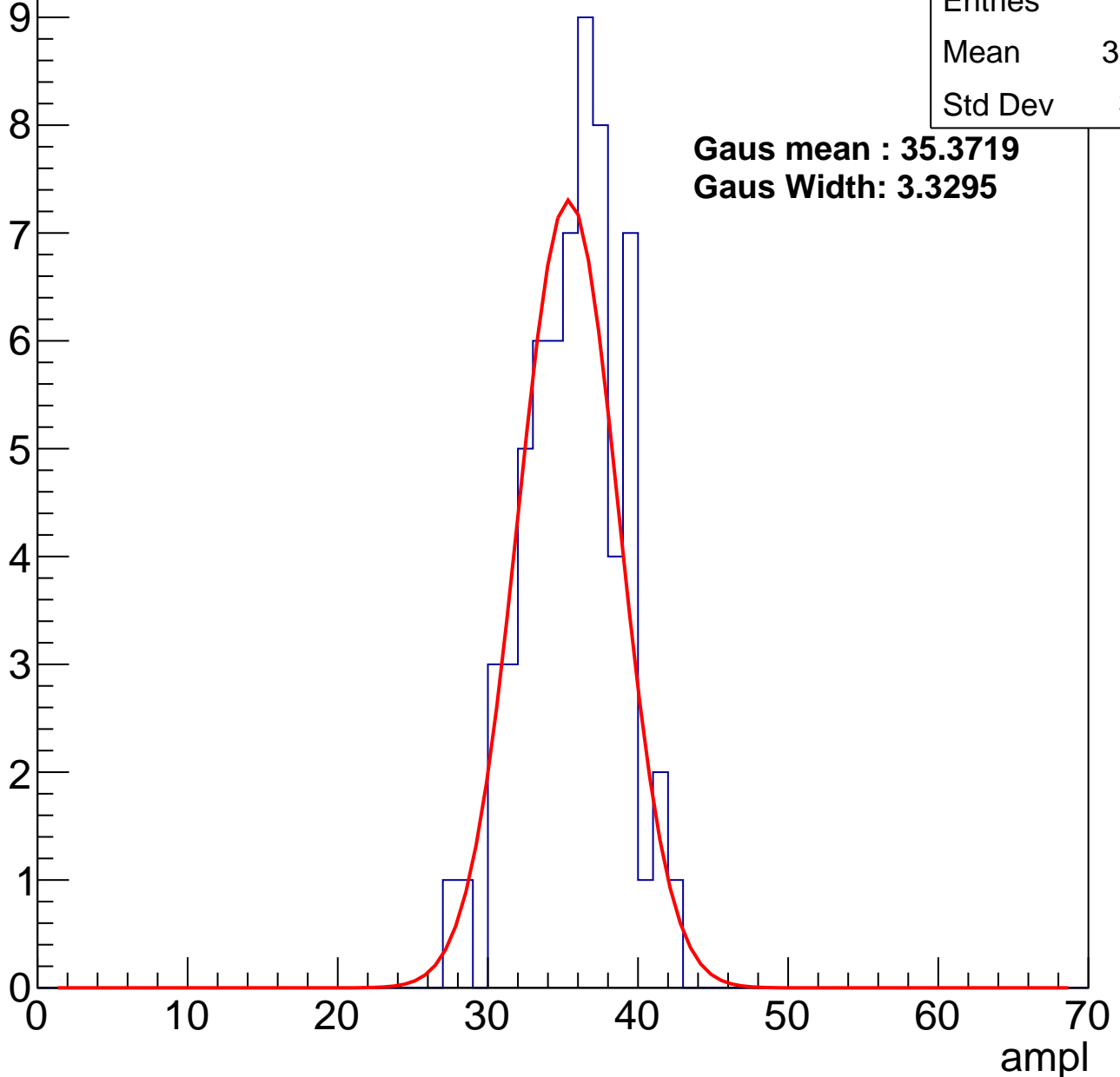
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	35.22
Std Dev	3.17

**Gaus mean : 35.3719**

**Gaus Width: 3.3295**



# B1L103S, U21-ch53, adc2

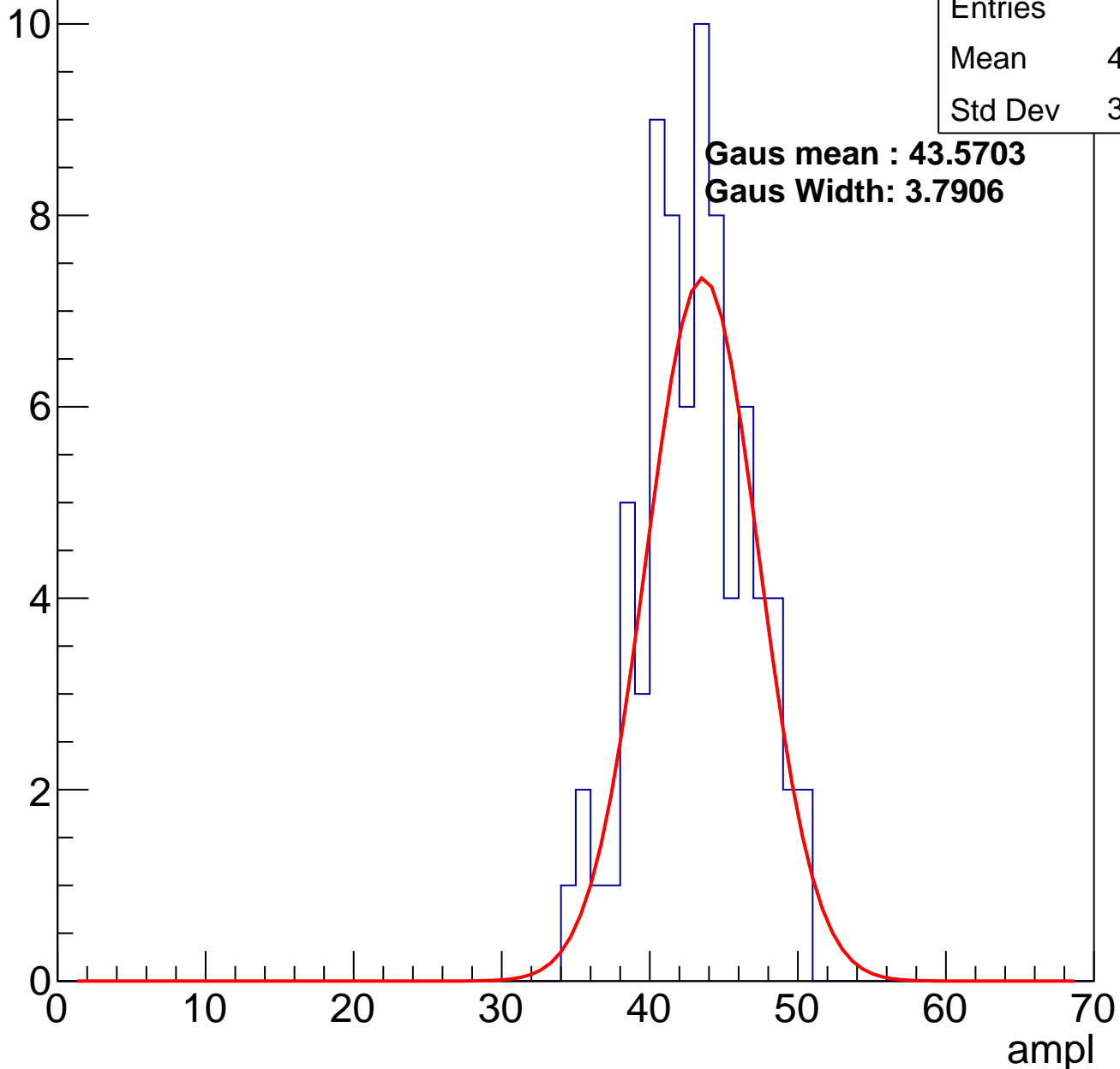
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	76
Mean	42.63
Std Dev	3.605

**Gaus mean : 43.5703**

**Gaus Width: 3.7906**

Entry

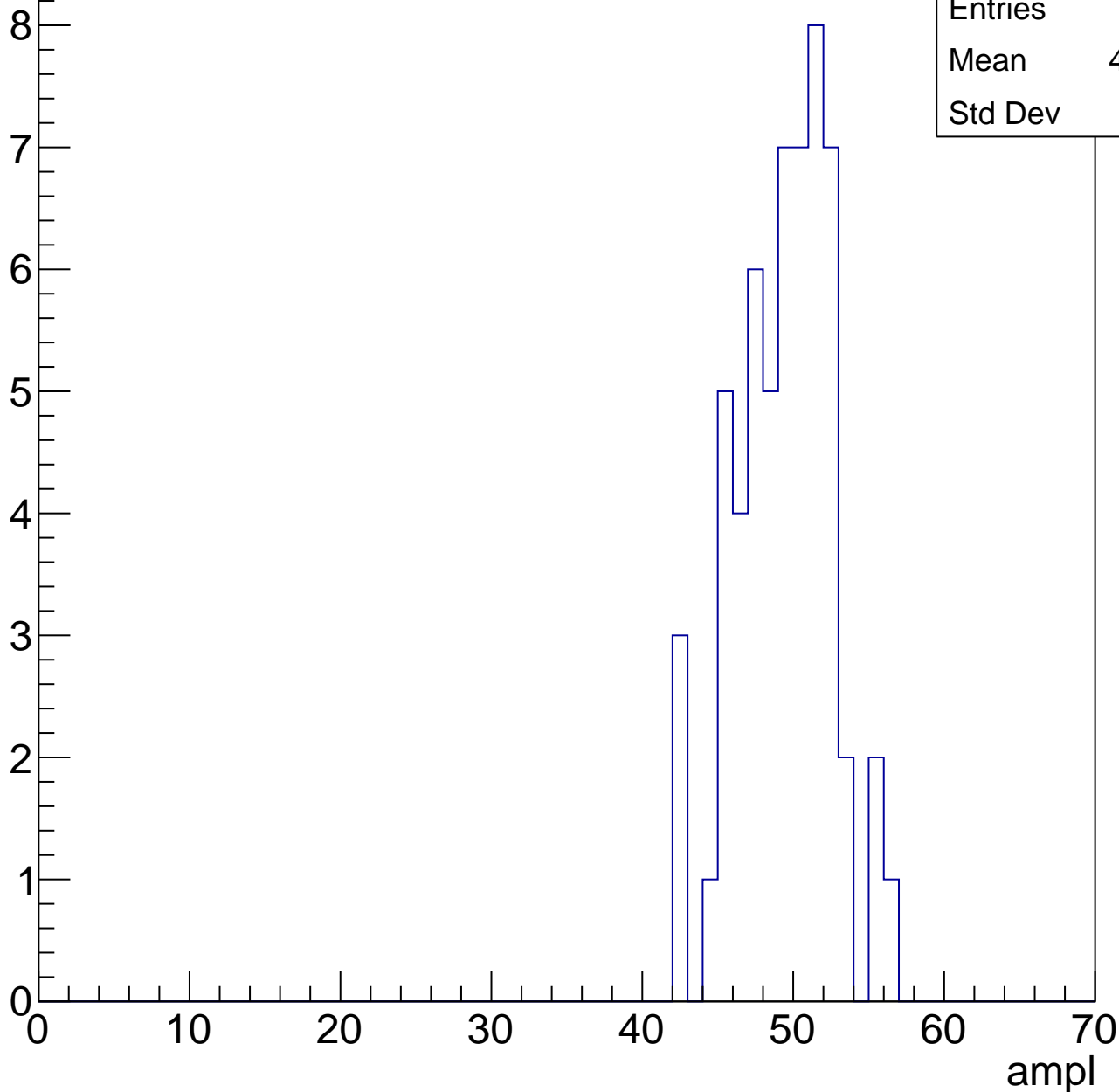


# B1L103S, U21-ch53, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	48.93
Std Dev	3.14



# B1L103S, U21-ch53, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

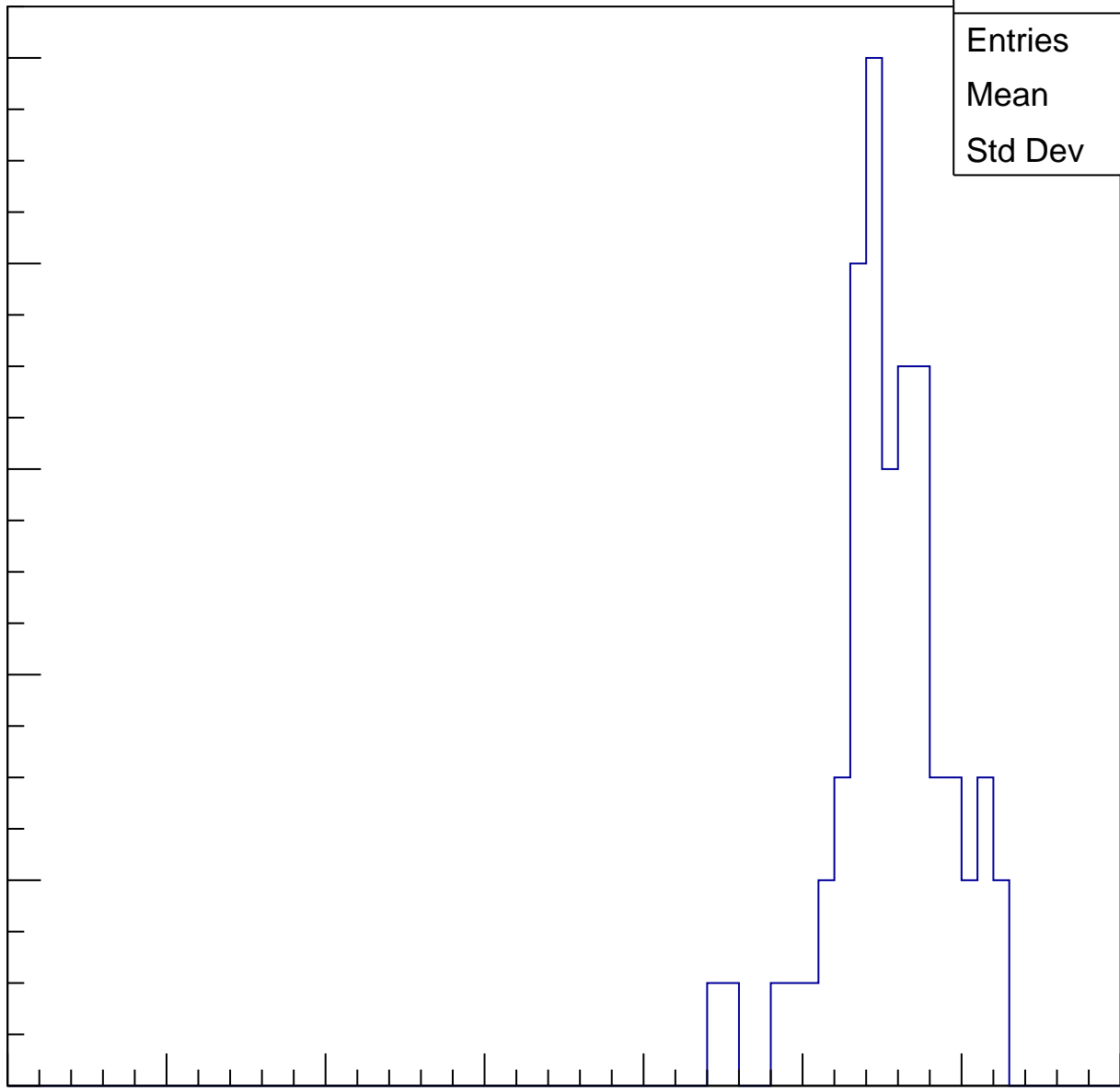
Entries	61
Mean	55.03
Std Dev	3.617

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

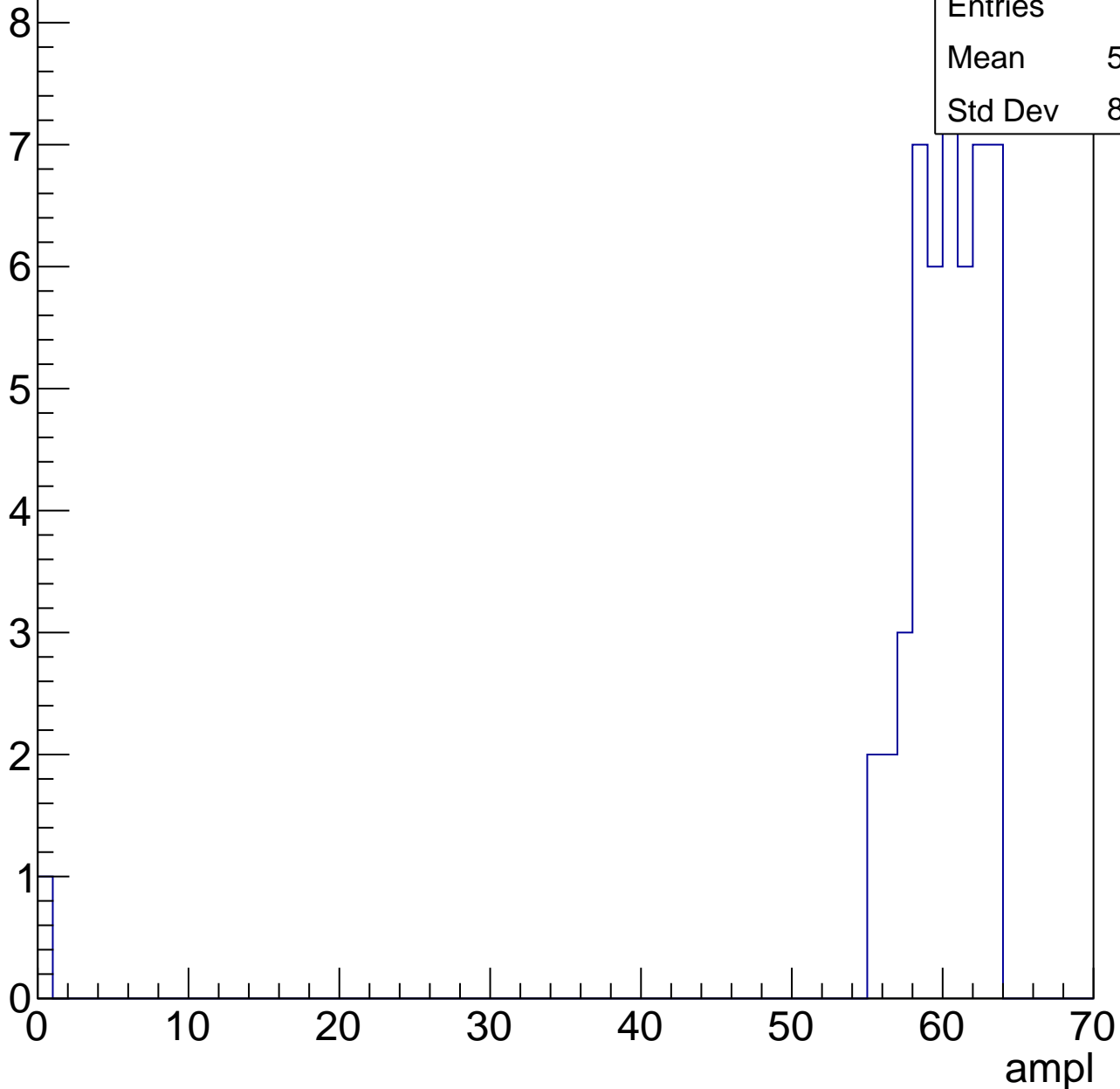


# B1L103S, U21-ch53, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	58.65
Std Dev	8.749



# B1L103S, U21-ch53, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U21-ch53, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L103S, U21-ch54, adc0

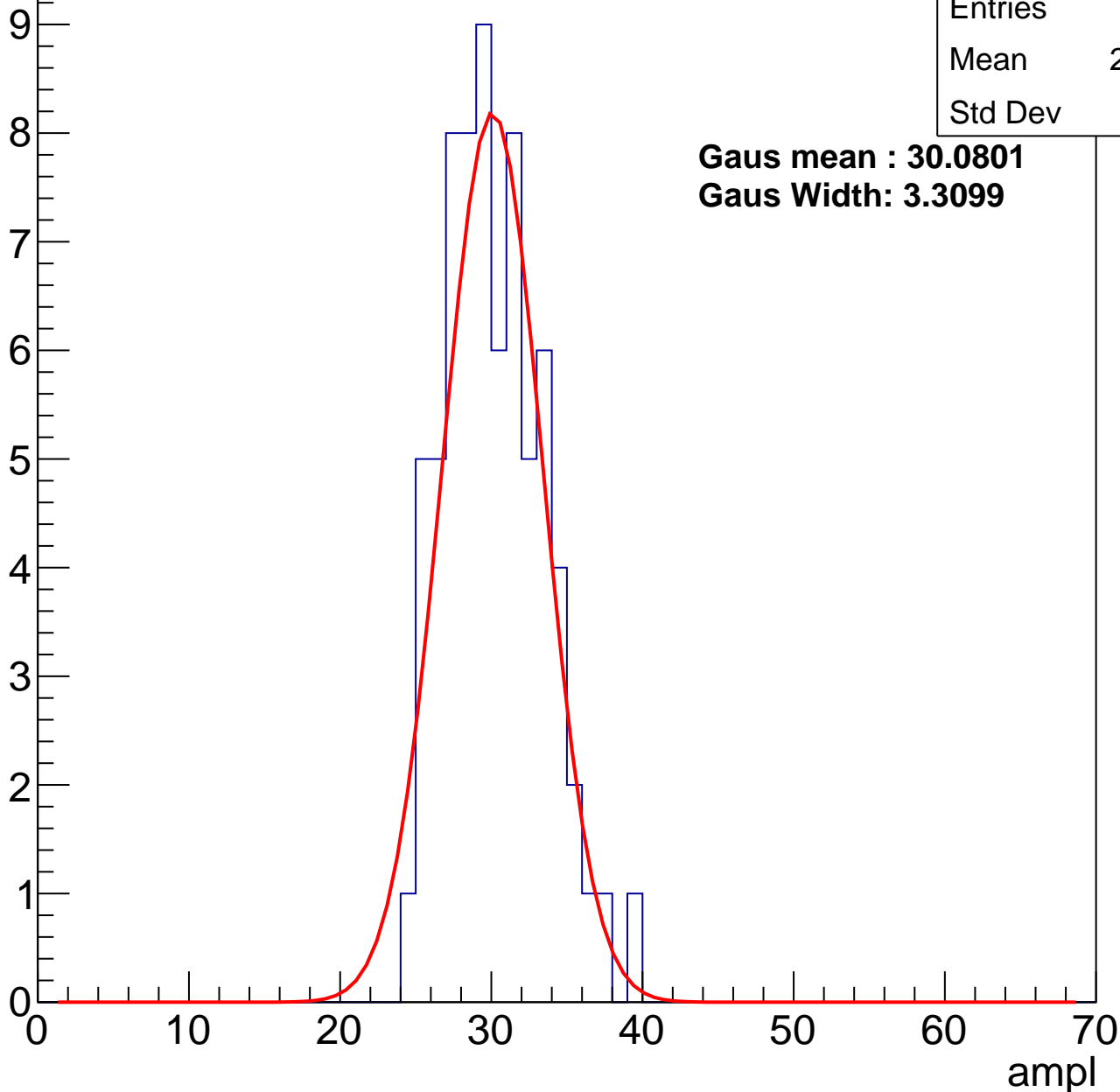
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	29.77
Std Dev	3.19

**Gaus mean : 30.0801**

**Gaus Width: 3.3099**



# B1L103S, U21-ch54, adc1

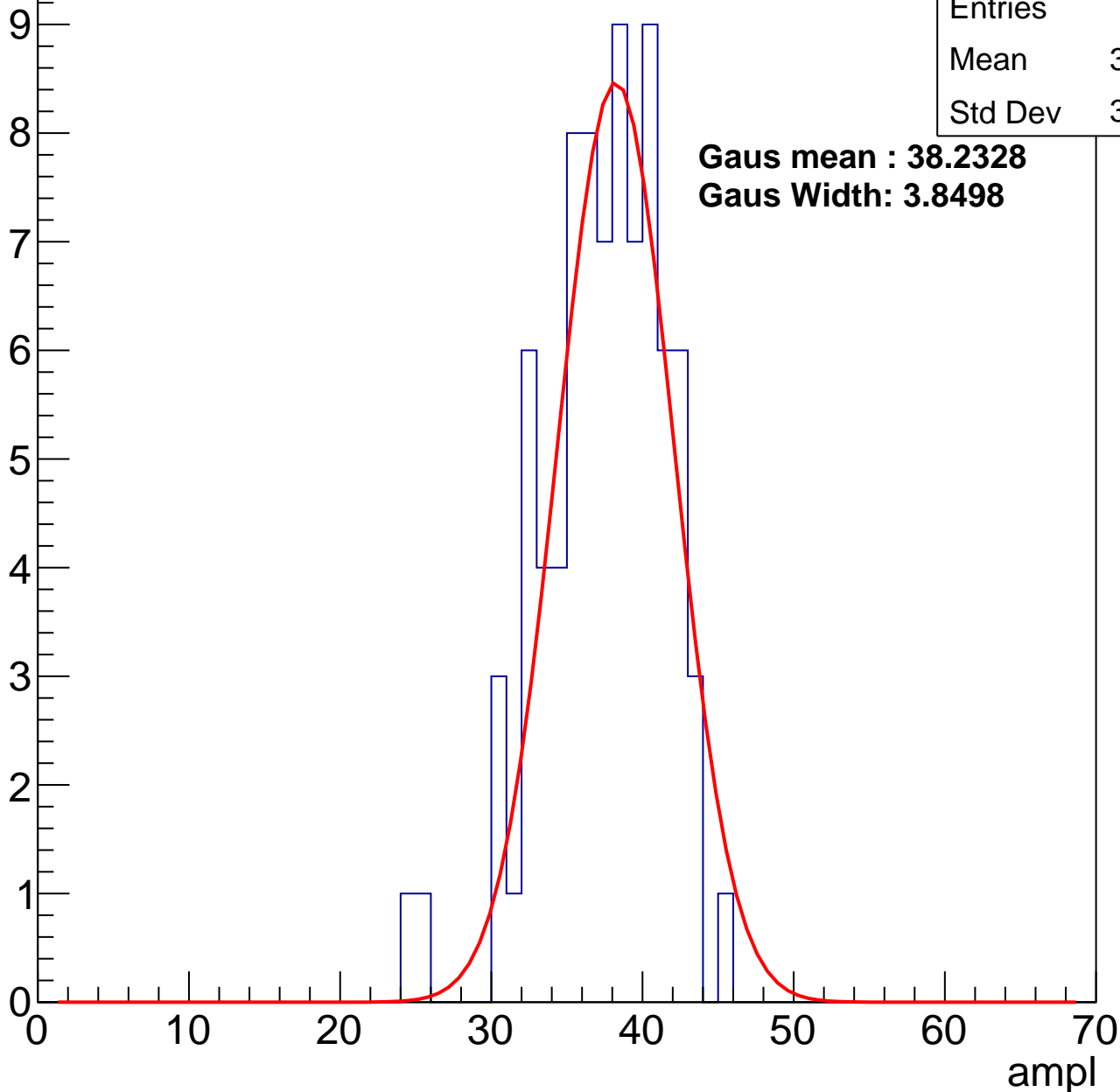
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	84
Mean	36.95
Std Dev	3.967

**Gaus mean : 38.2328**

**Gaus Width: 3.8498**



# B1L103S, U21-ch54, adc2

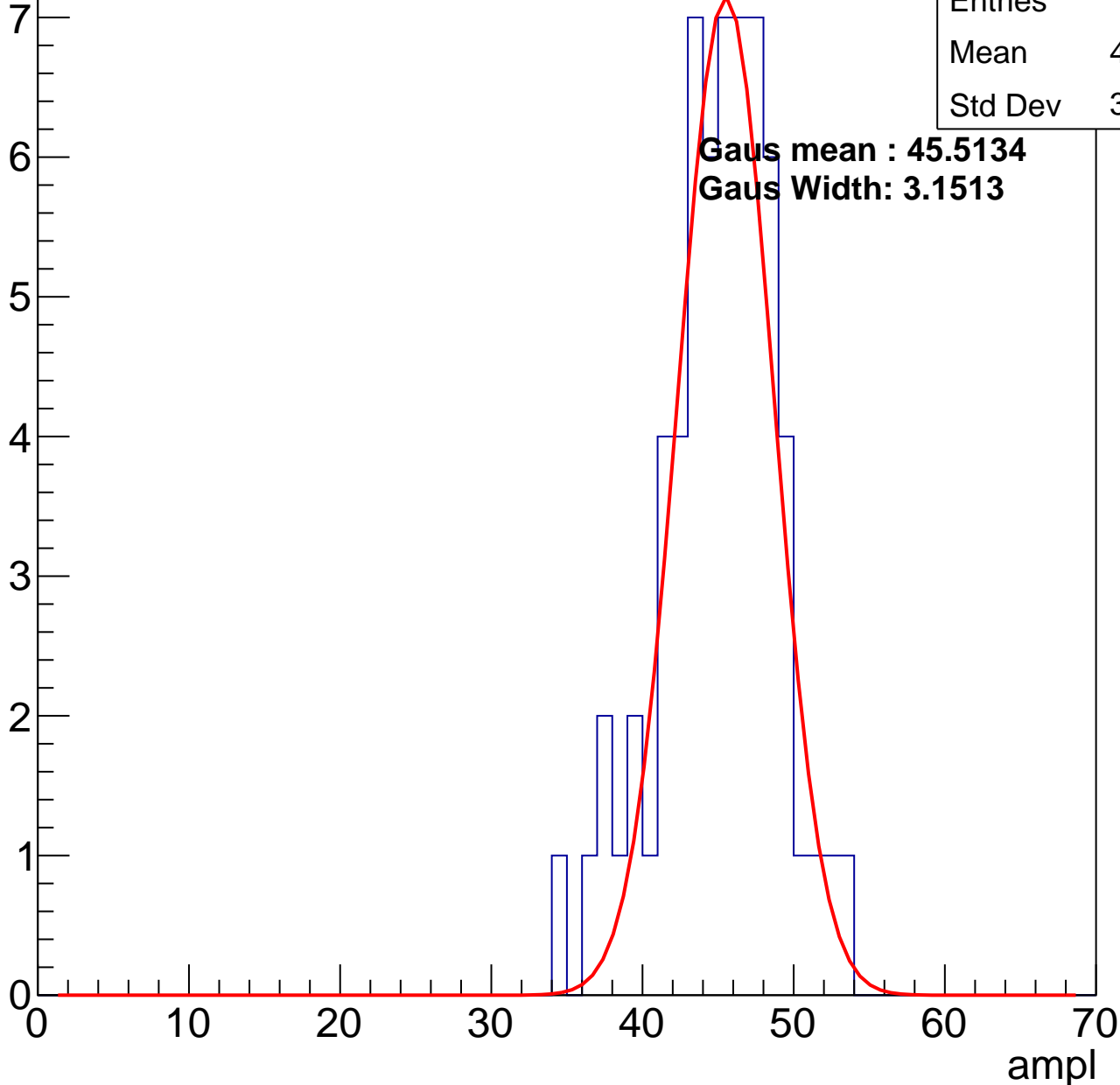
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	44.58
Std Dev	3.803

**Gaus mean : 45.5134**

**Gaus Width: 3.1513**

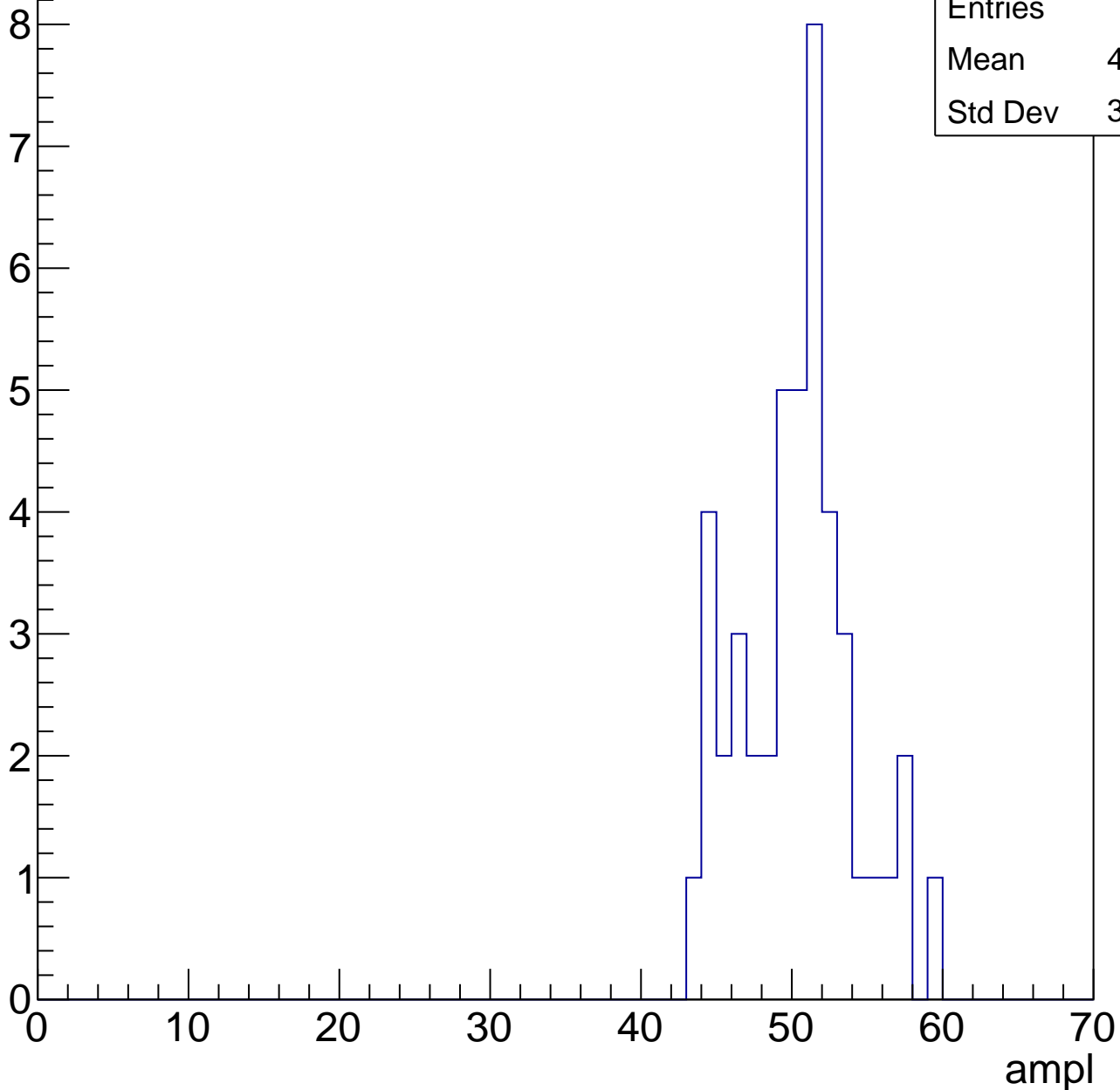


# B1L103S, U21-ch54, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	45
Mean	49.89
Std Dev	3.737

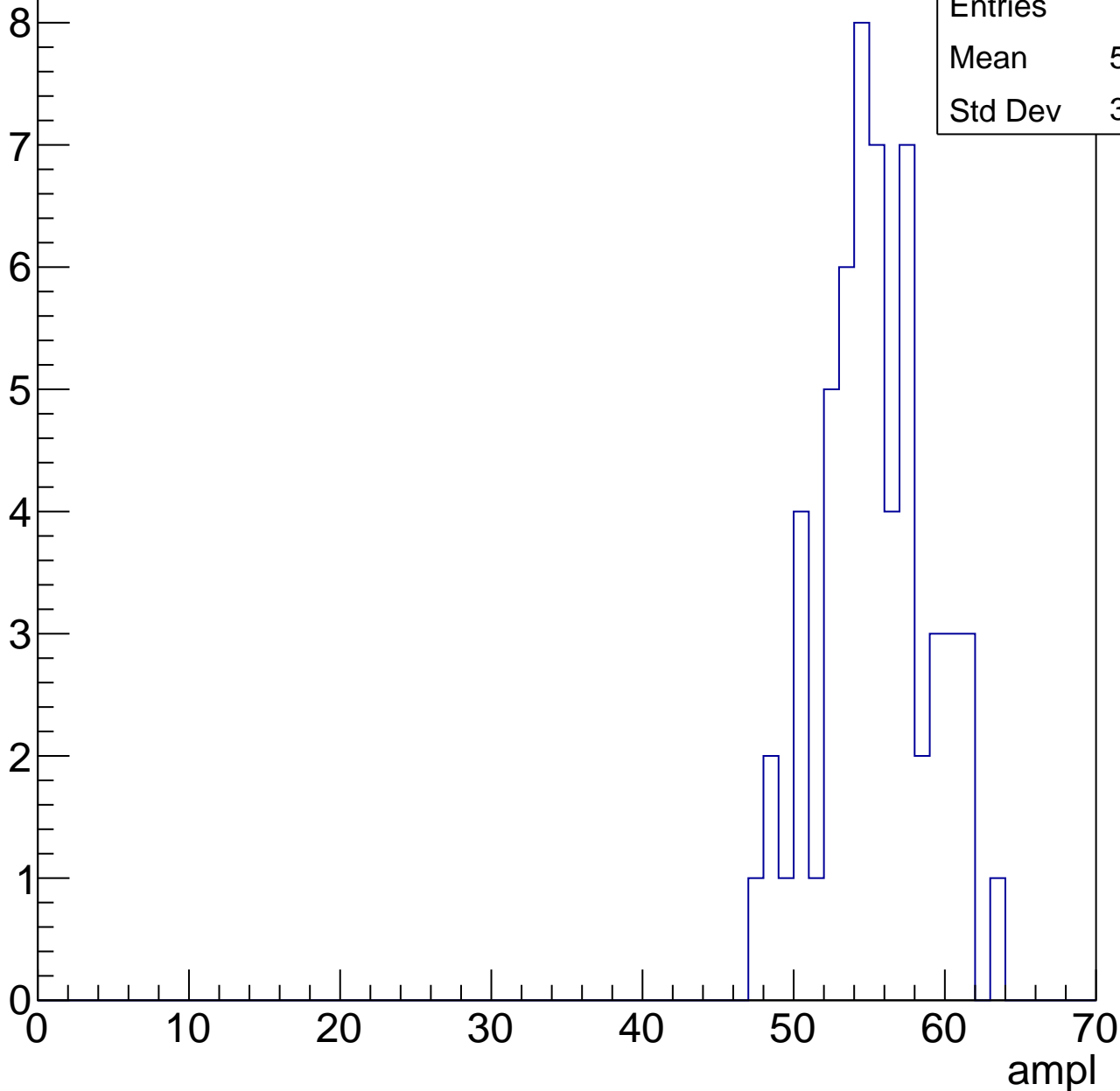


# B1L103S, U21-ch54, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	54.83
Std Dev	3.558

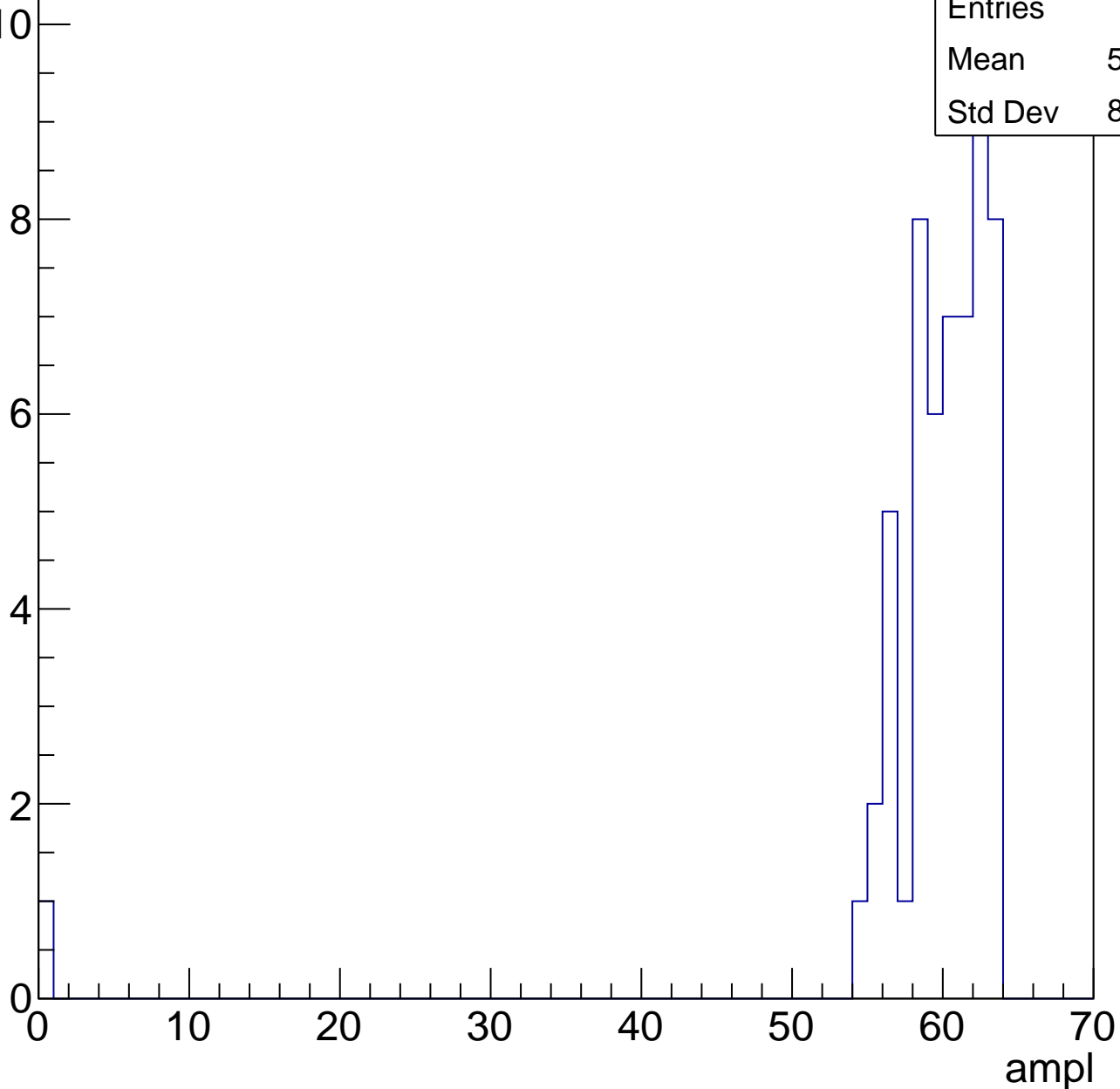


# B1L103S, U21-ch54, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	58.75
Std Dev	8.286



# B1L103S, U21-ch54, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	63
Std Dev	0



# B1L103S, U21-ch54, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U21-ch55, adc0

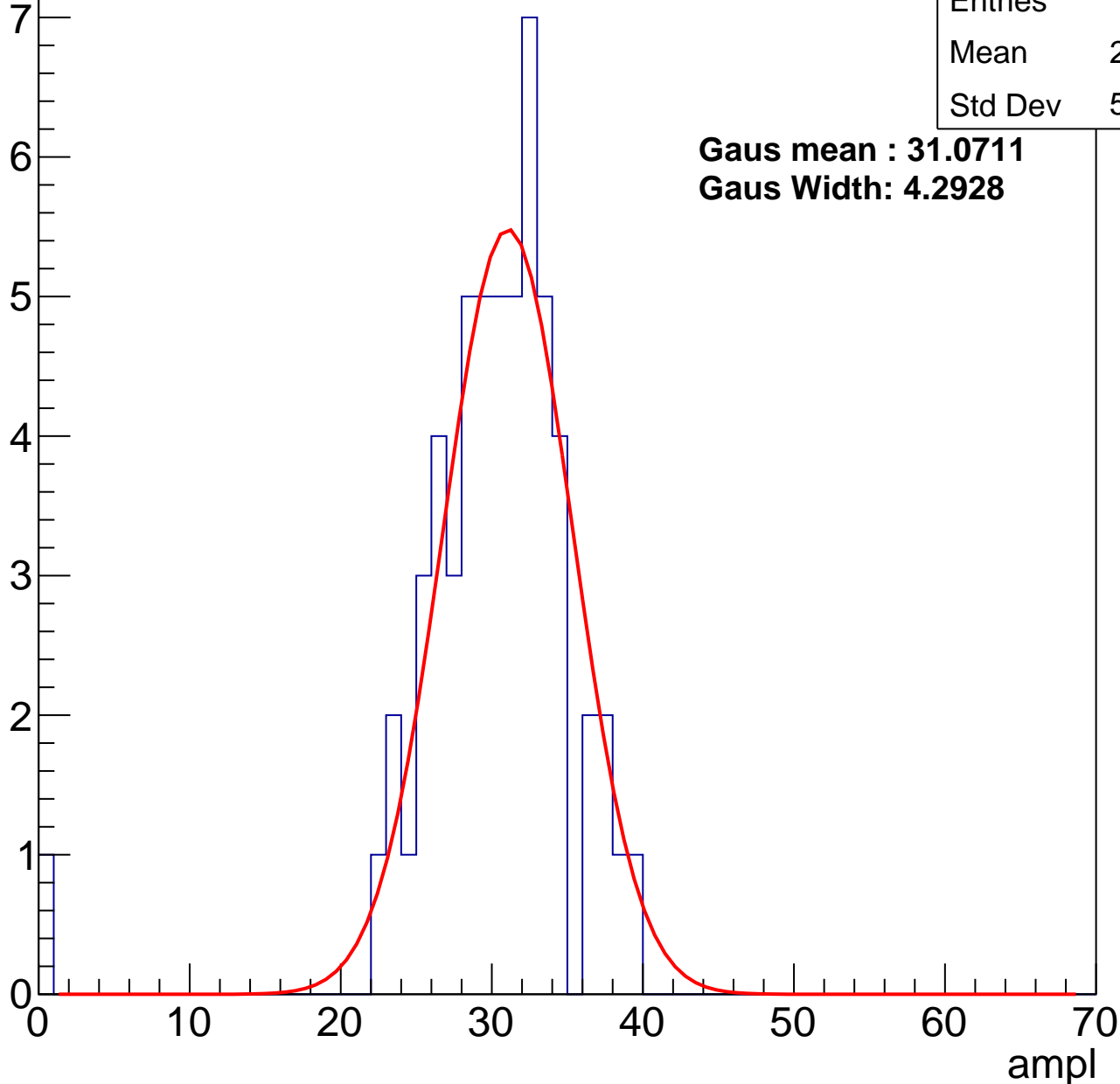
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	29.65
Std Dev	5.523

**Gaus mean : 31.0711**

**Gaus Width: 4.2928**



# B1L103S, U21-ch55, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	71
Mean	36.65
Std Dev	4.06

**Gaus mean : 36.6949**

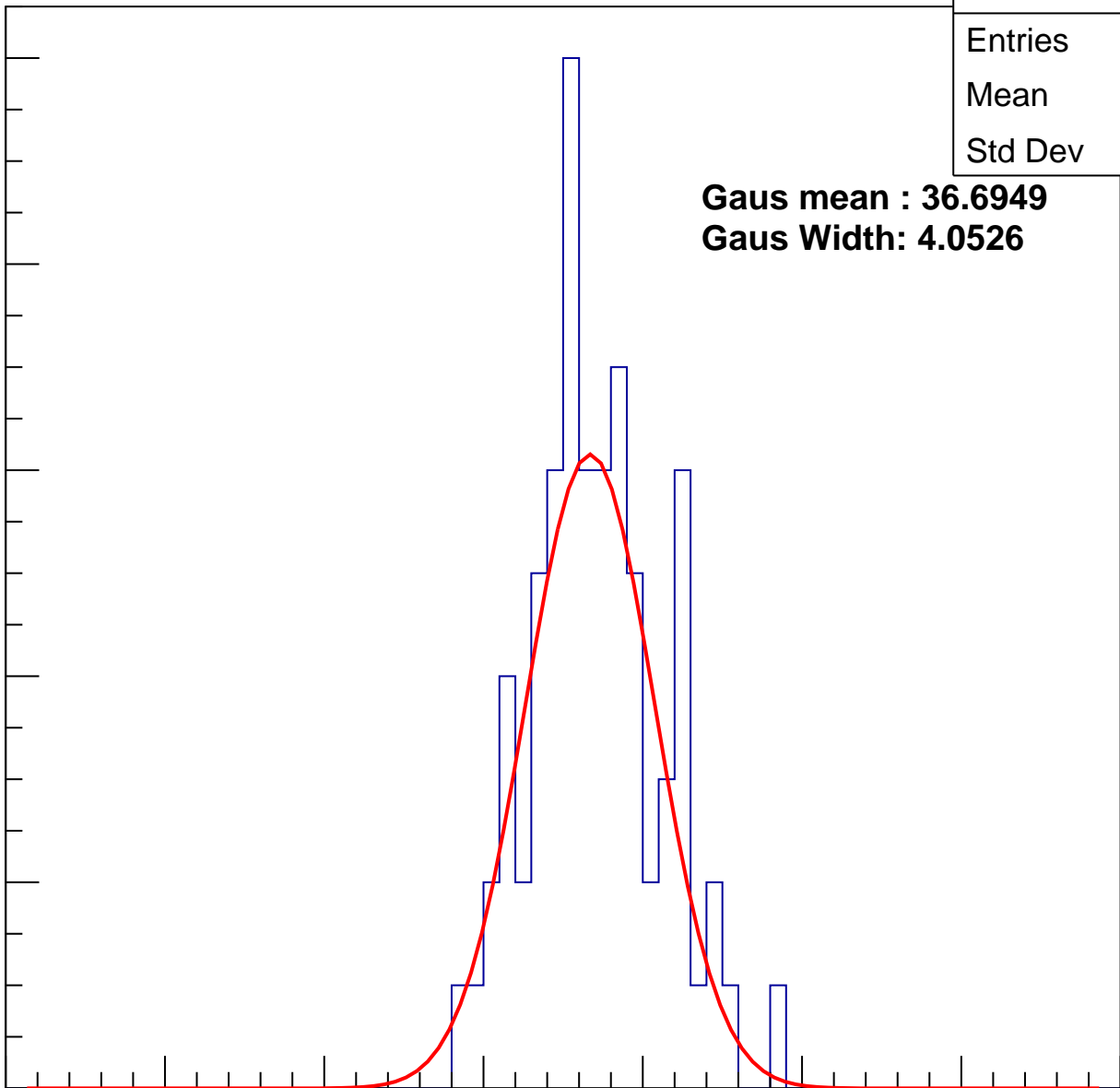
**Gaus Width: 4.0526**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U21-ch55, adc2

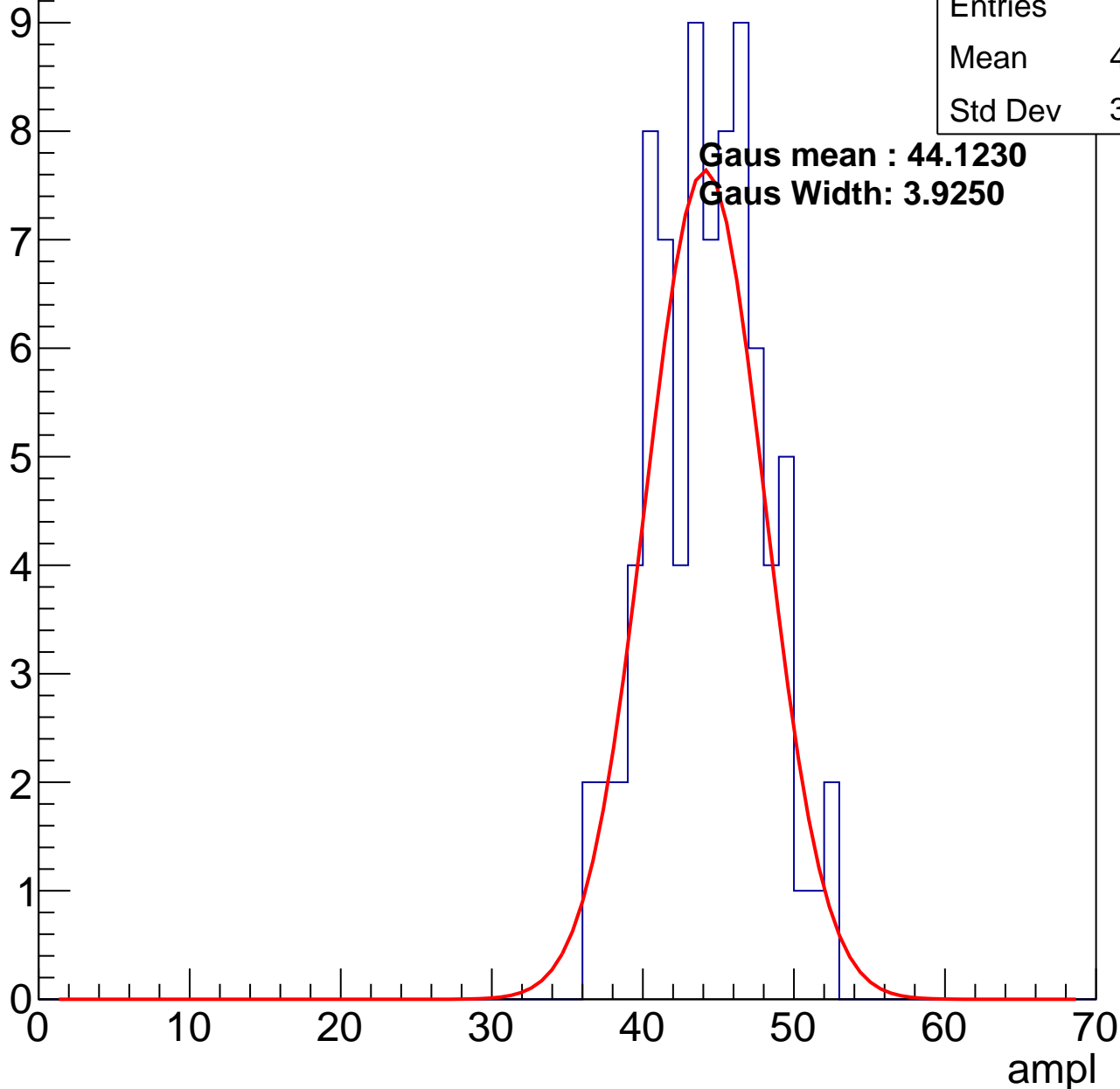
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	81
Mean	43.78
Std Dev	3.702

**Gaus mean : 44.1230**

**Gaus Width: 3.9250**

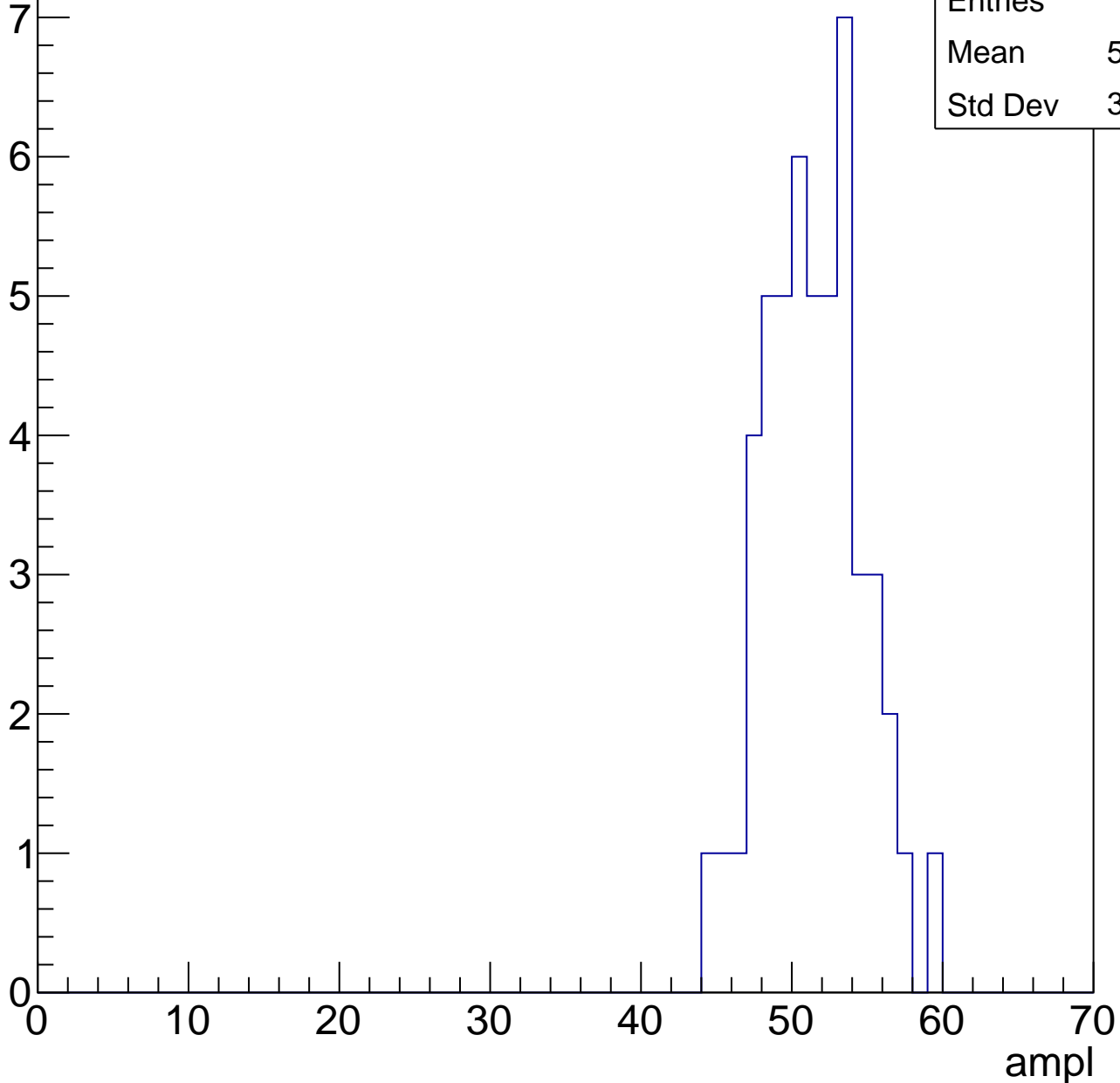


# B1L103S, U21-ch55, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	50.98
Std Dev	3.172

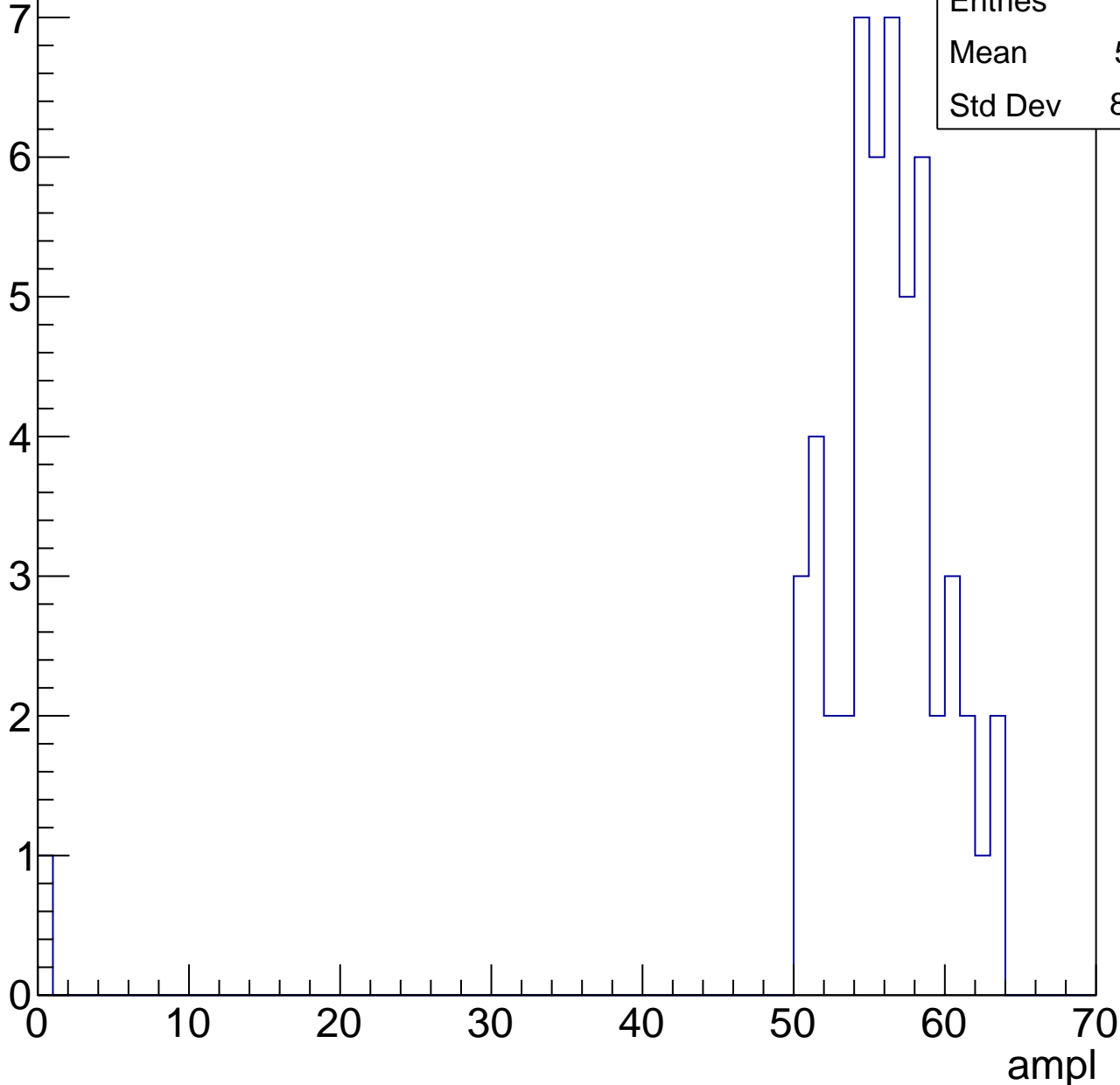


# B1L103S, U21-ch55, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	54.81
Std Dev	8.278



# B1L103S, U21-ch55, adc5

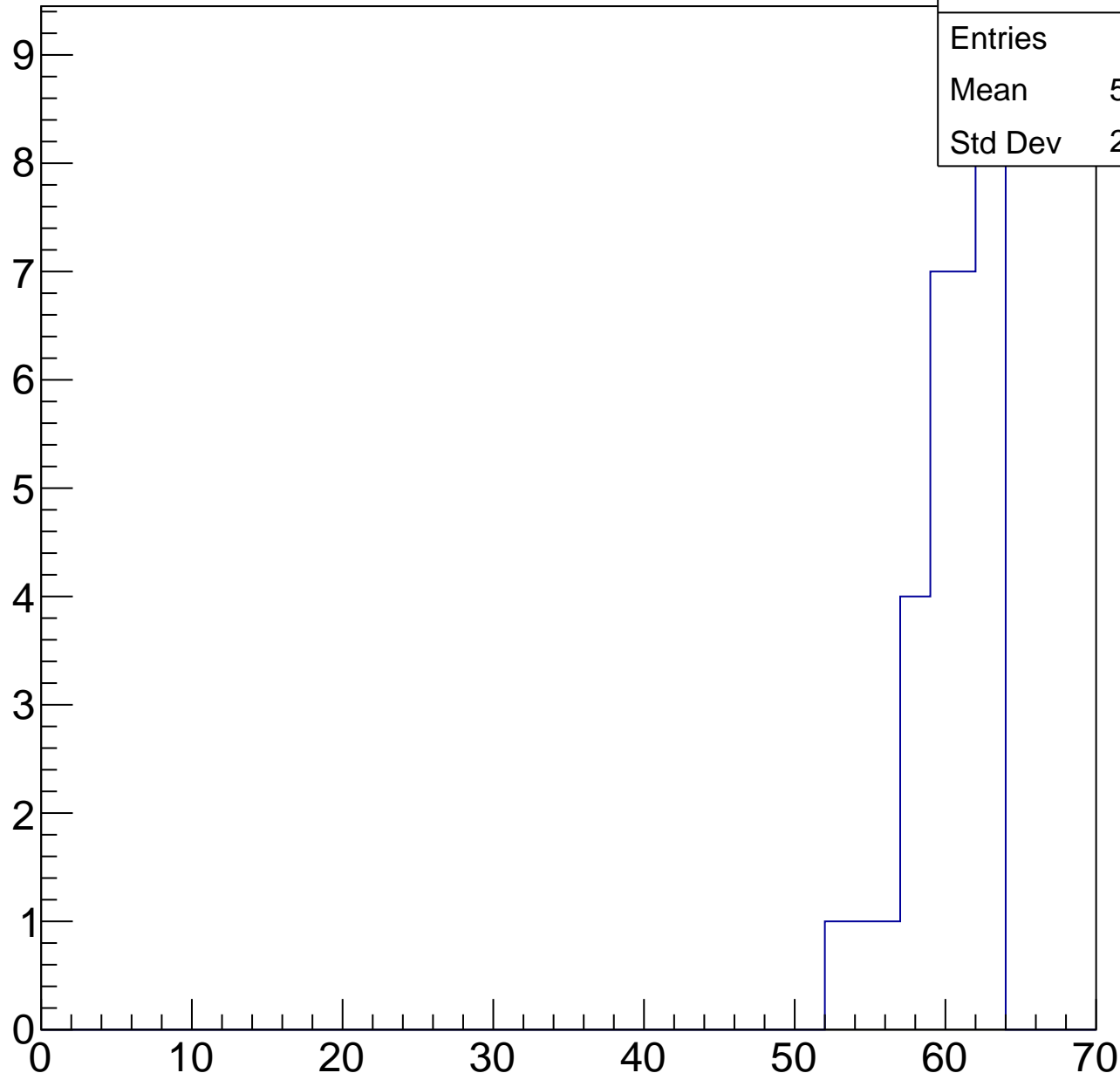
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	51
Mean	59.84
Std Dev	2.667

ampl



# B1L103S, U21-ch55, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	61
Std Dev	0



# B1L103S, U21-ch55, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L103S, U21-ch56, adc0

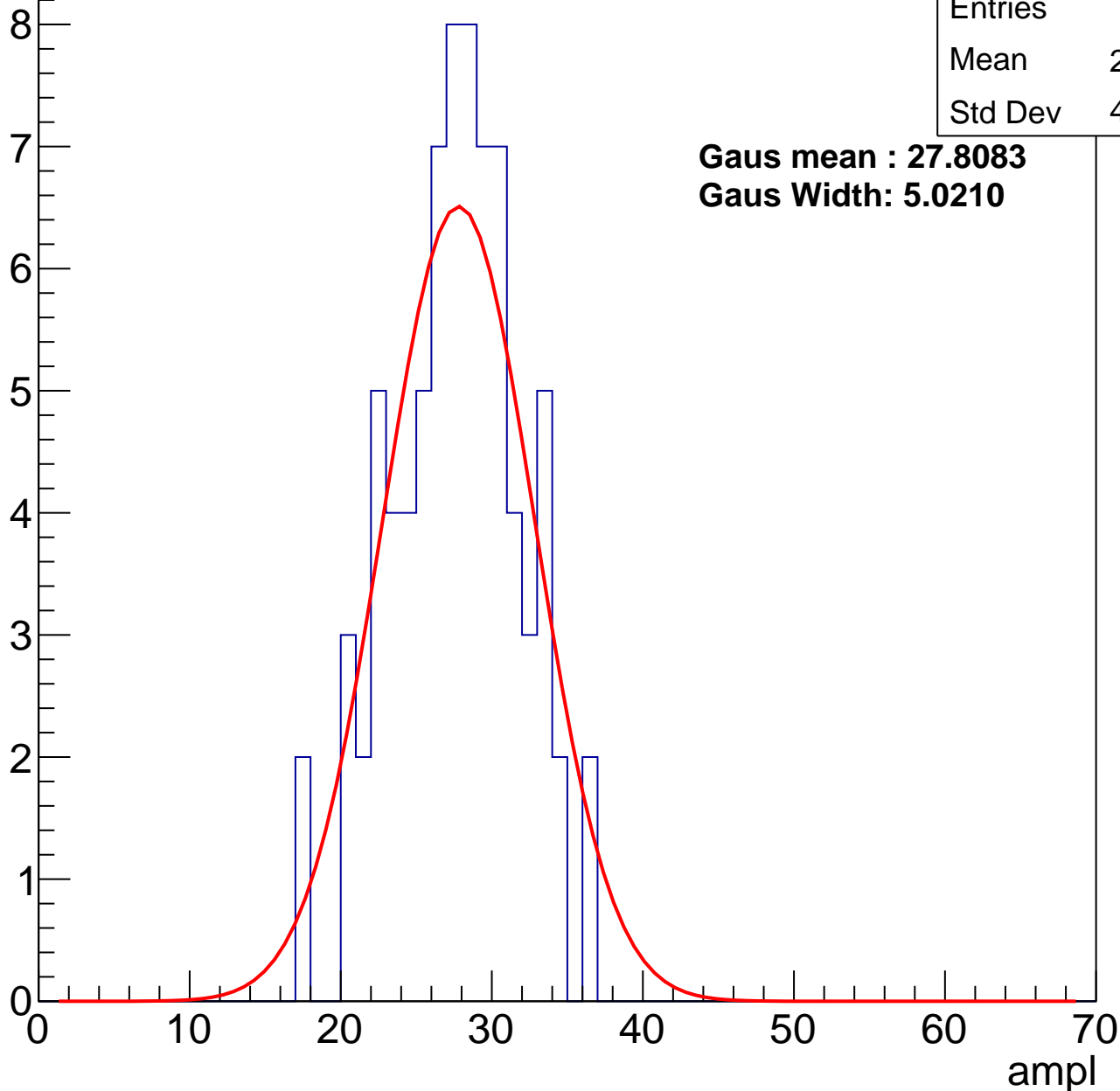
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	27.17
Std Dev	4.155

**Gaus mean : 27.8083**

**Gaus Width: 5.0210**



# B1L103S, U21-ch56, adc1

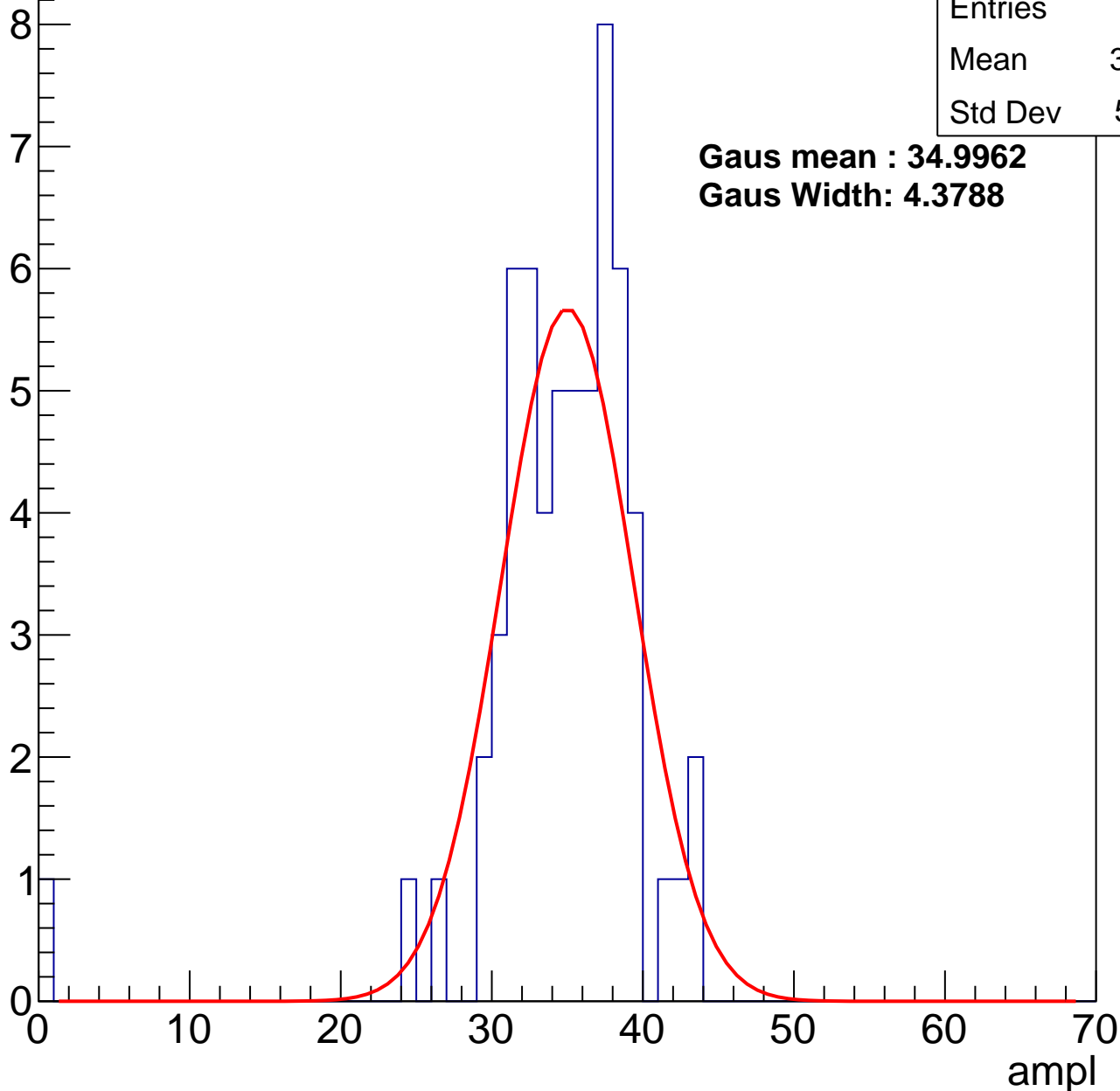
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	34.13
Std Dev	5.821

**Gaus mean : 34.9962**

**Gaus Width: 4.3788**



# B1L103S, U21-ch56, adc2

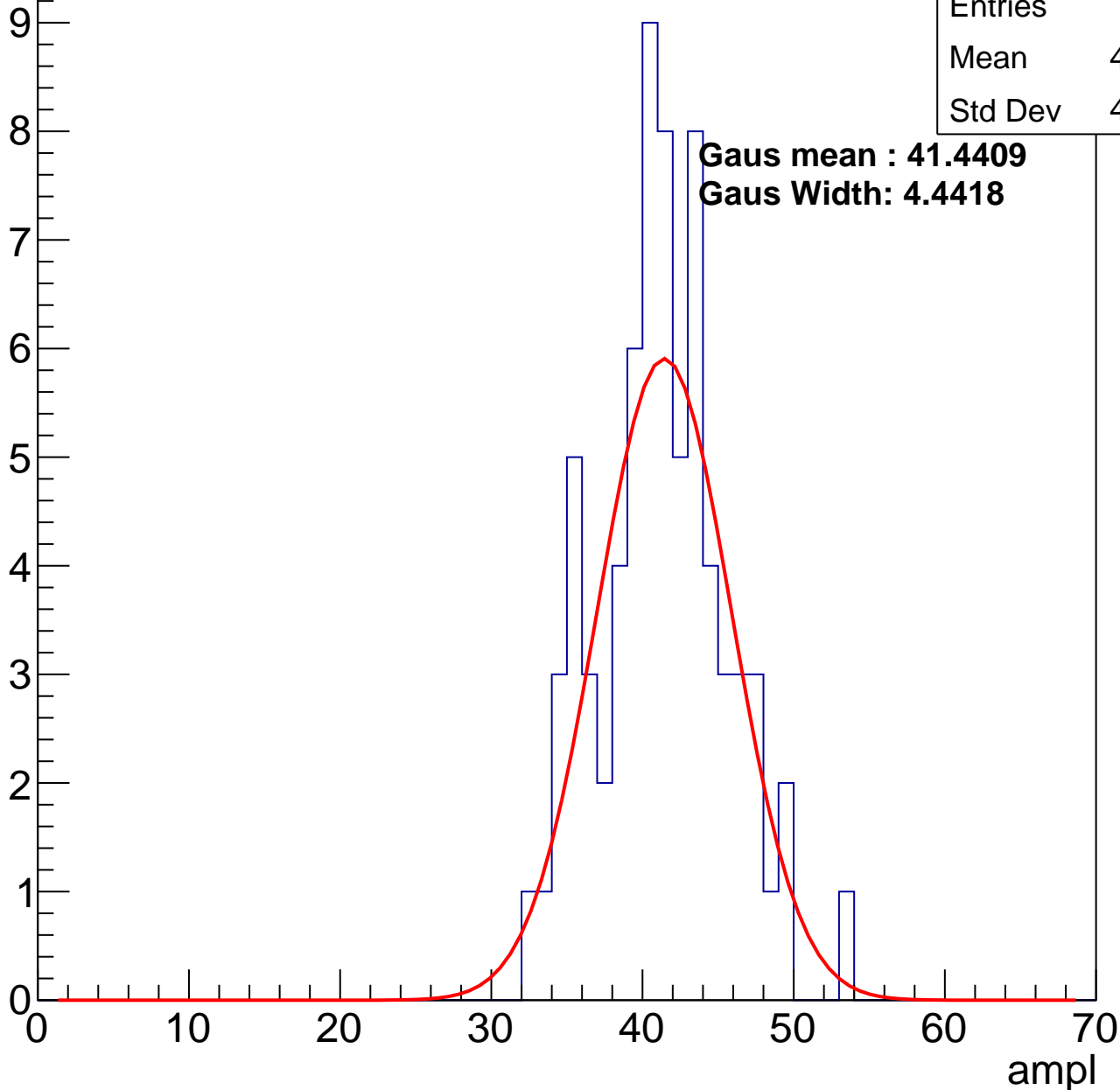
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	40.85
Std Dev	4.202

**Gaus mean : 41.4409**

**Gaus Width: 4.4418**

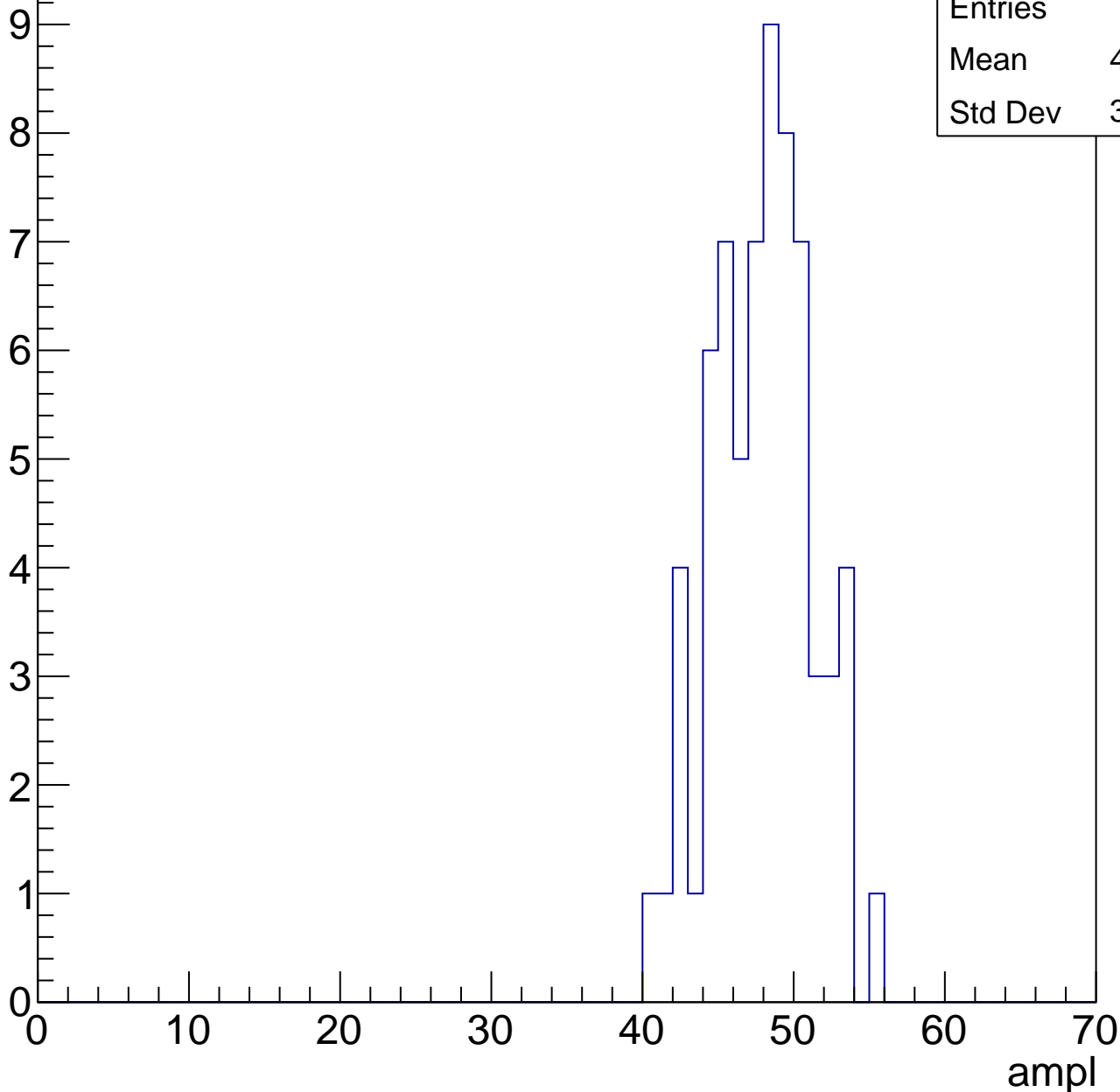


# B1L103S, U21-ch56, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	47.46
Std Dev	3.252

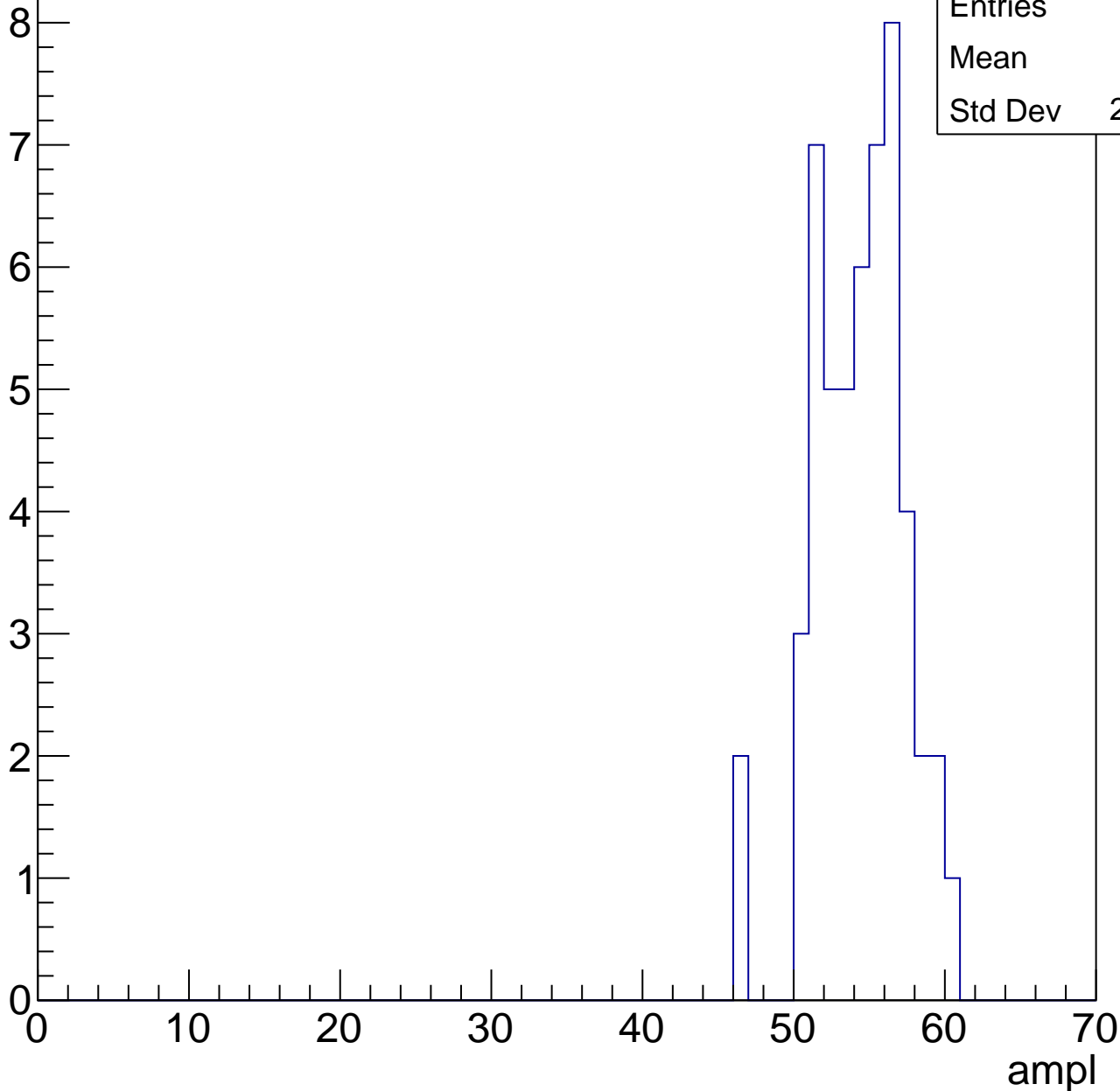


# B1L103S, U21-ch56, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

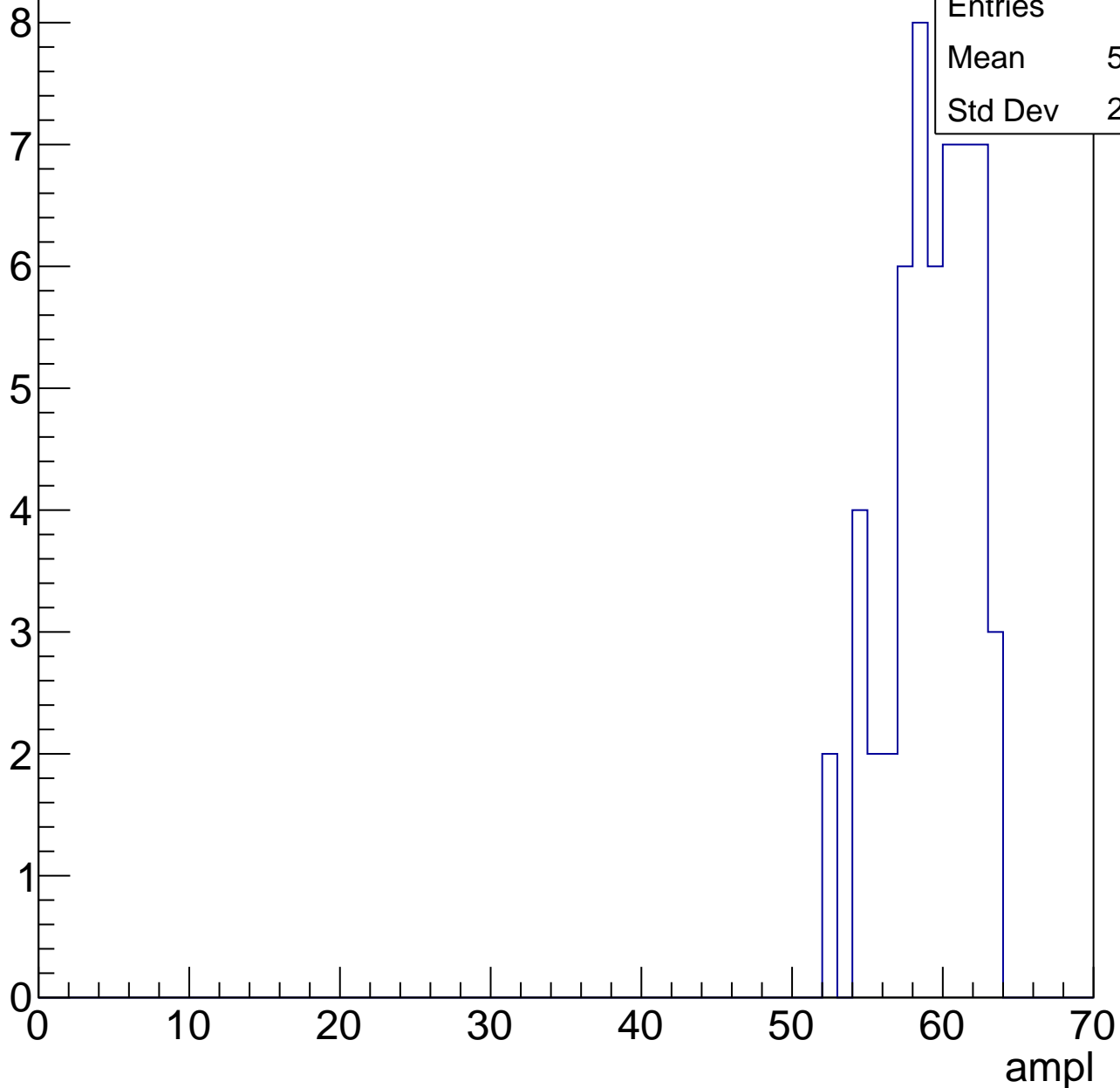
Entries	52
Mean	53.9
Std Dev	2.963



# B1L103S, U21-ch56, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

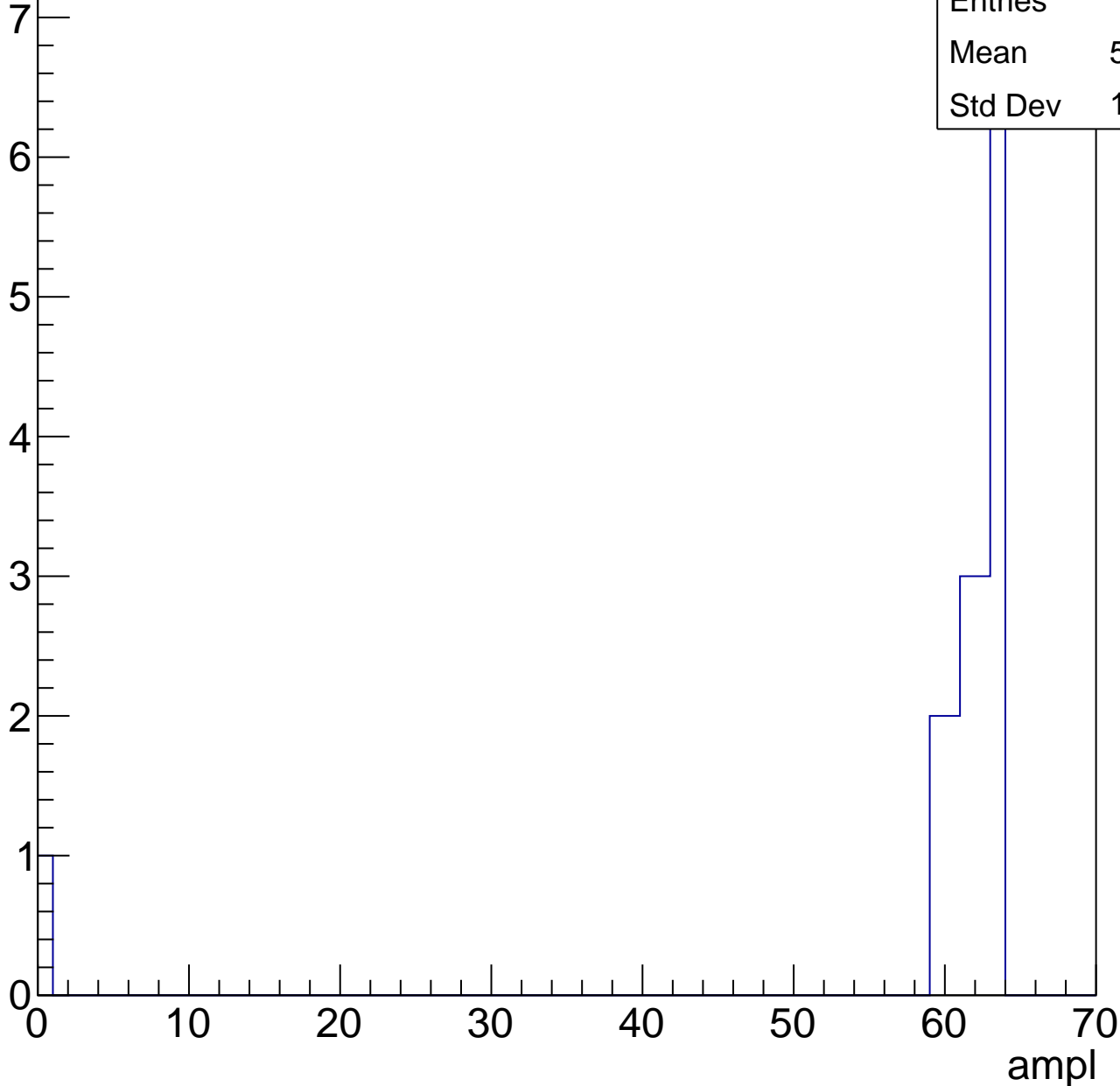


# B1L103S, U21-ch56, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	18
Mean	58.22
Std Dev	14.19





# B1L103S, U21-ch56, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U21-ch57, adc0

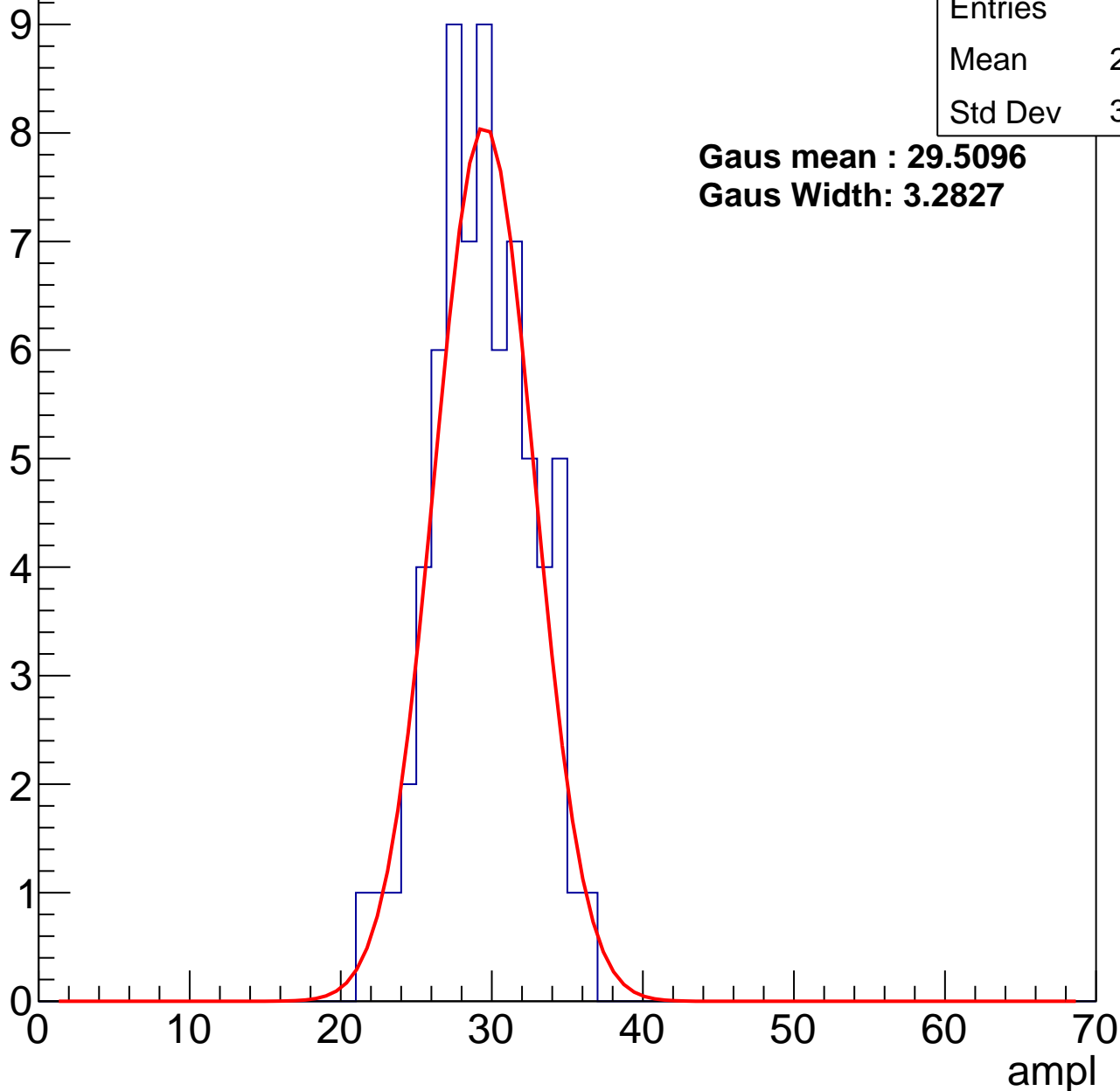
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	28.99
Std Dev	3.215

**Gaus mean : 29.5096**

**Gaus Width: 3.2827**



# B1L103S, U21-ch57, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	86
Mean	37.64
Std Dev	3.757

**Gaus mean : 37.8996**

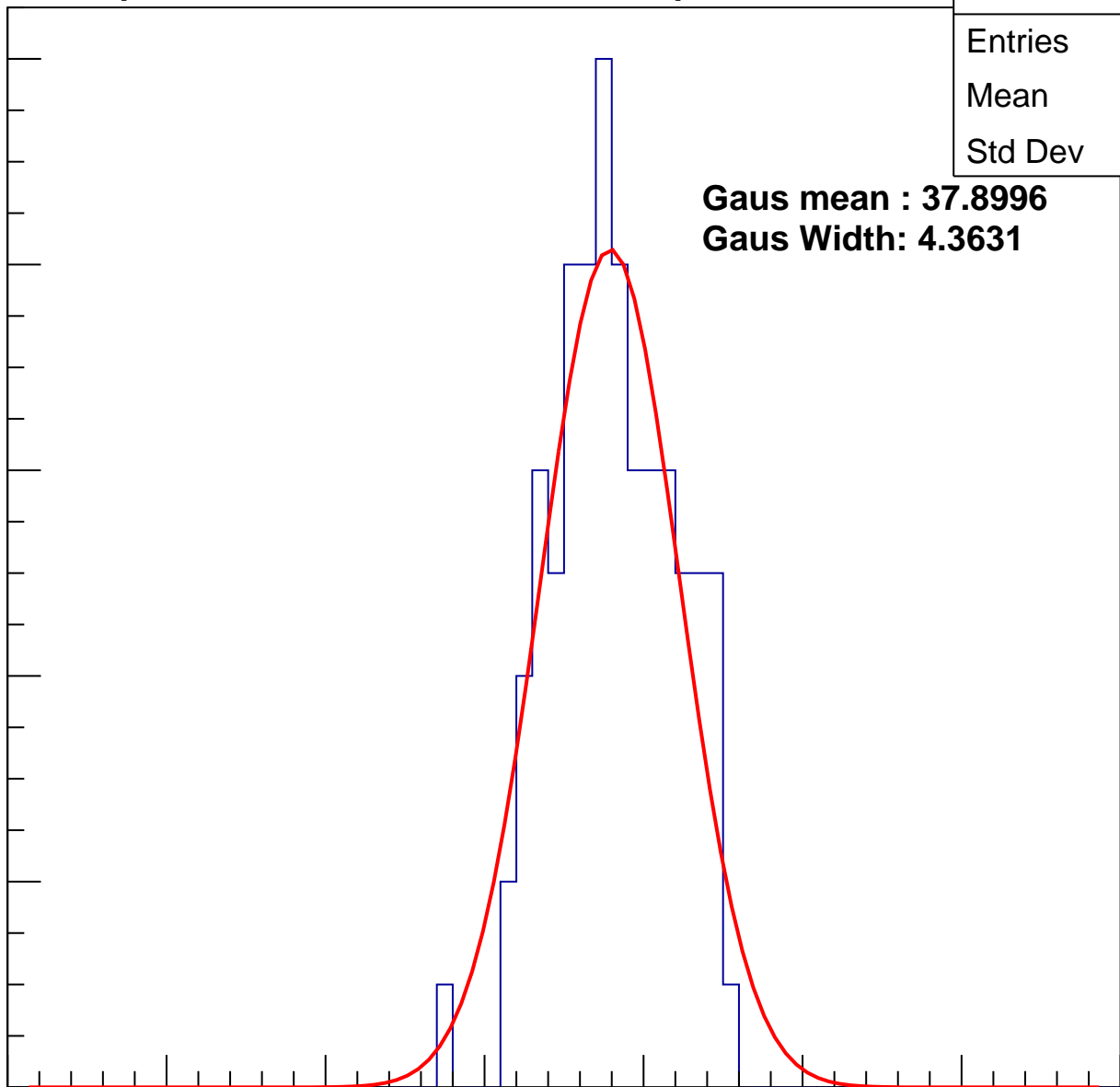
**Gaus Width: 4.3631**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U21-ch57, adc2

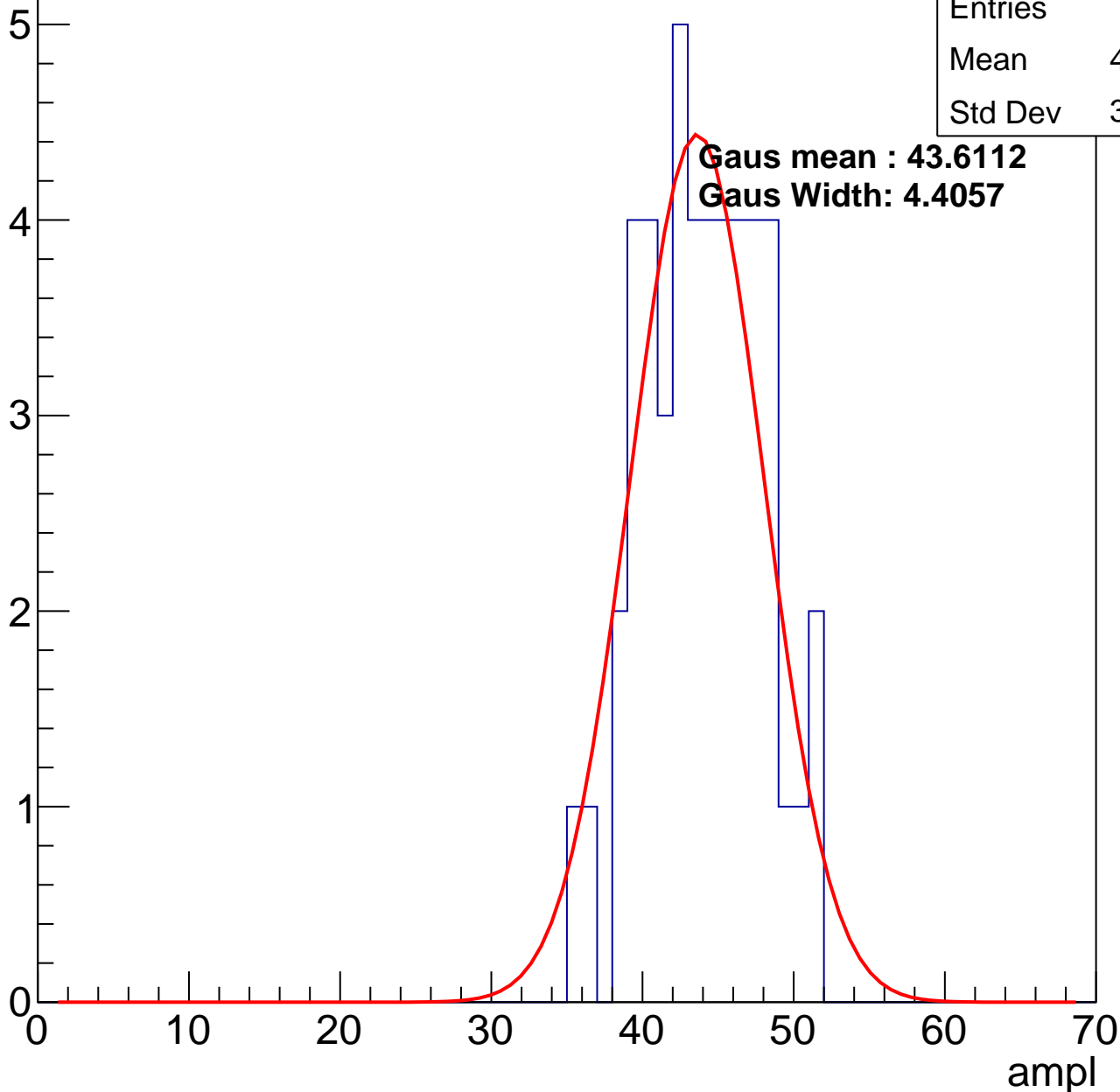
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	48
Mean	43.52
Std Dev	3.819

**Gaus mean : 43.6112**

**Gaus Width: 4.4057**

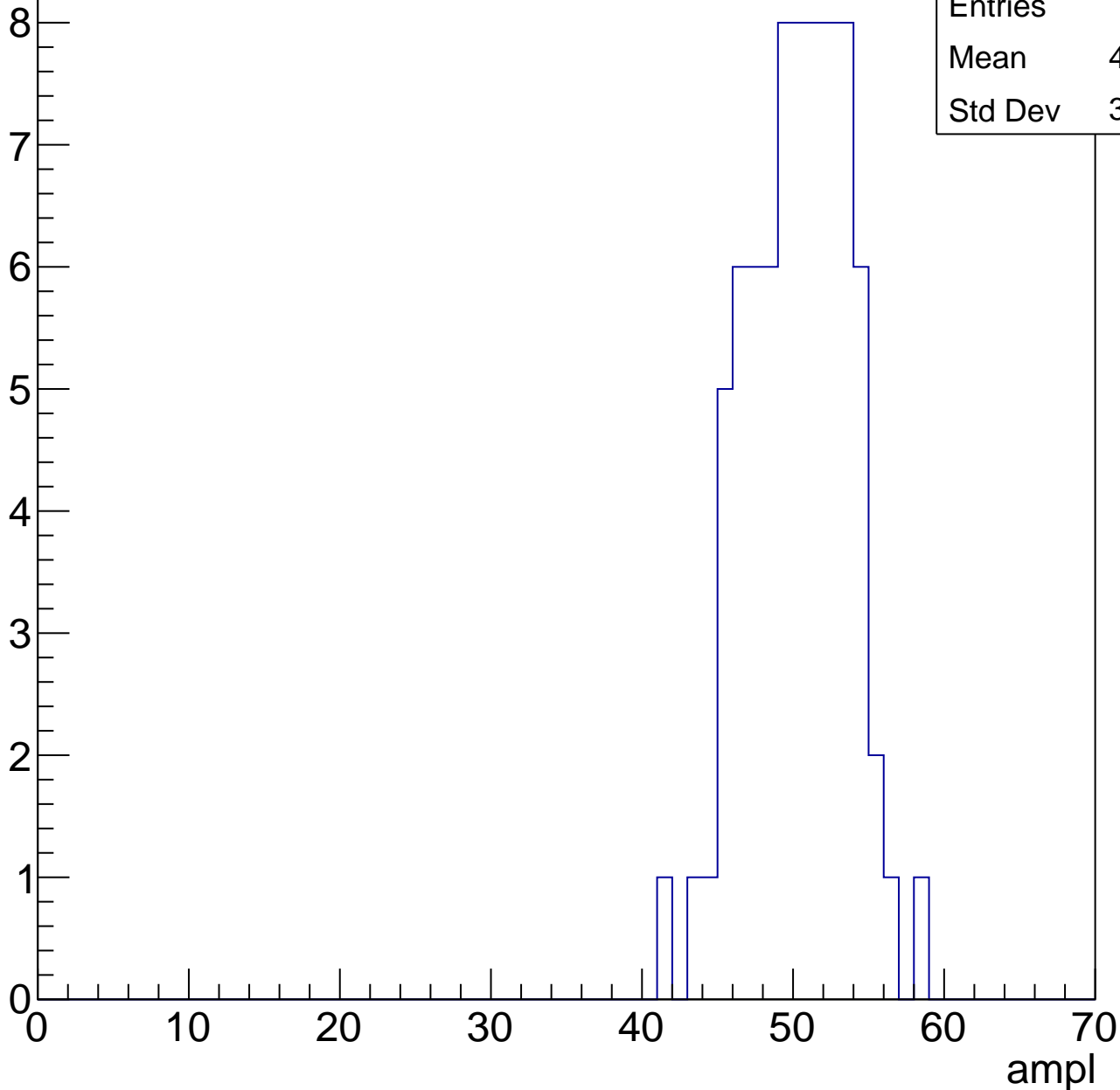


# B1L103S, U21-ch57, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	49.83
Std Dev	3.302

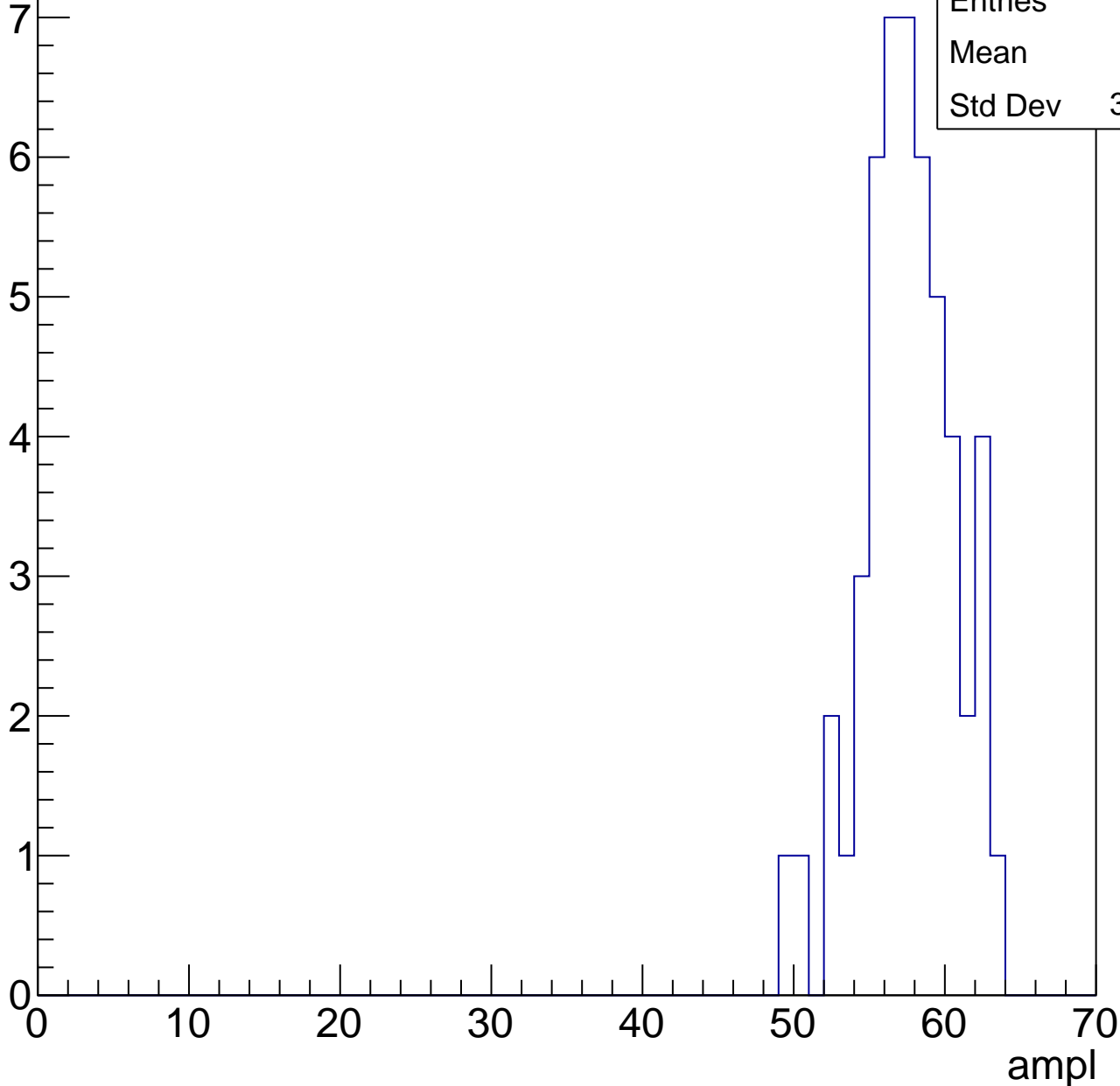


# B1L103S, U21-ch57, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	57.1
Std Dev	3.055

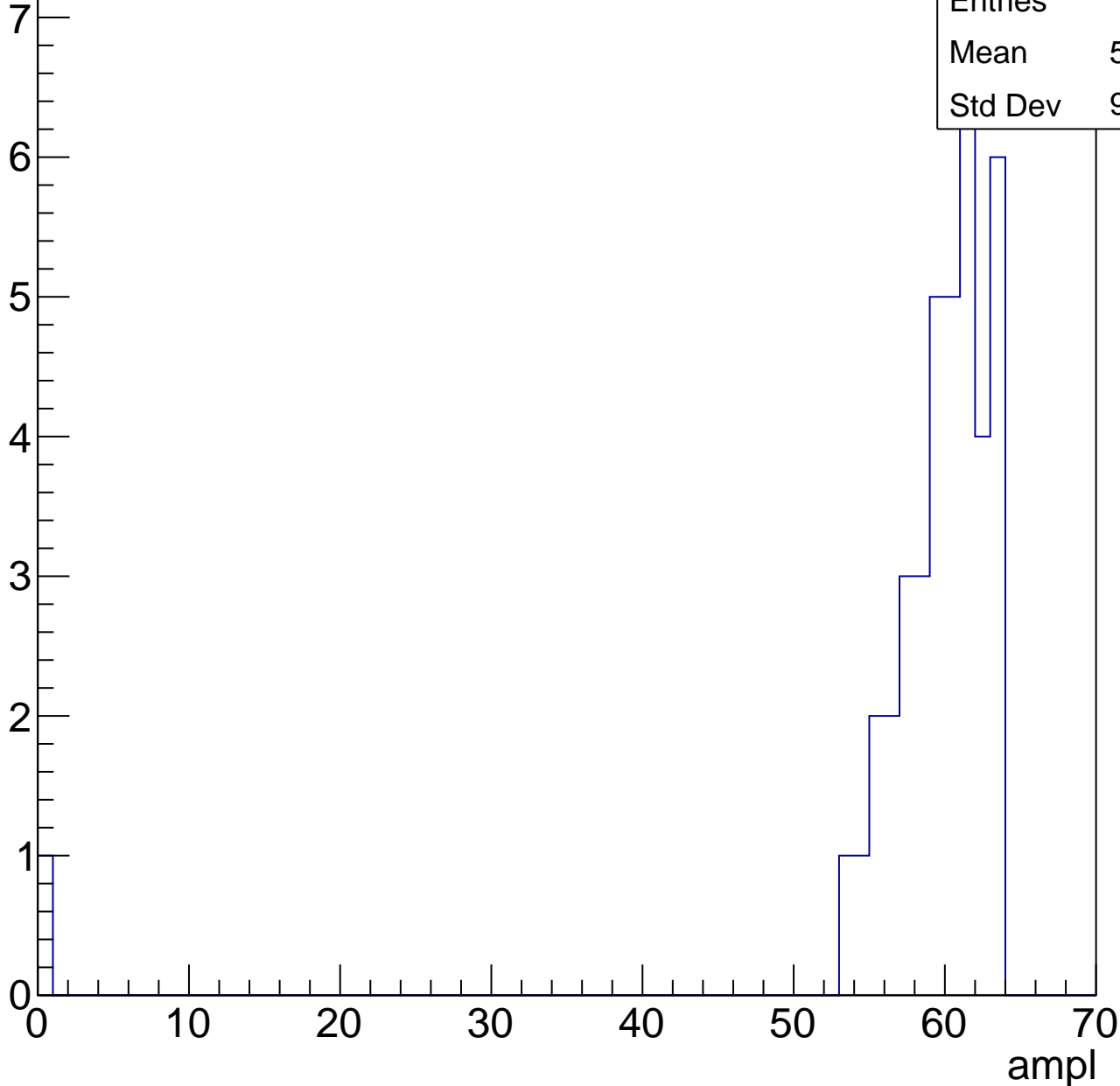


# B1L103S, U21-ch57, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	40
Mean	58.05
Std Dev	9.664



# B1L103S, U21-ch57, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U21-ch57, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U21-ch58, adc0

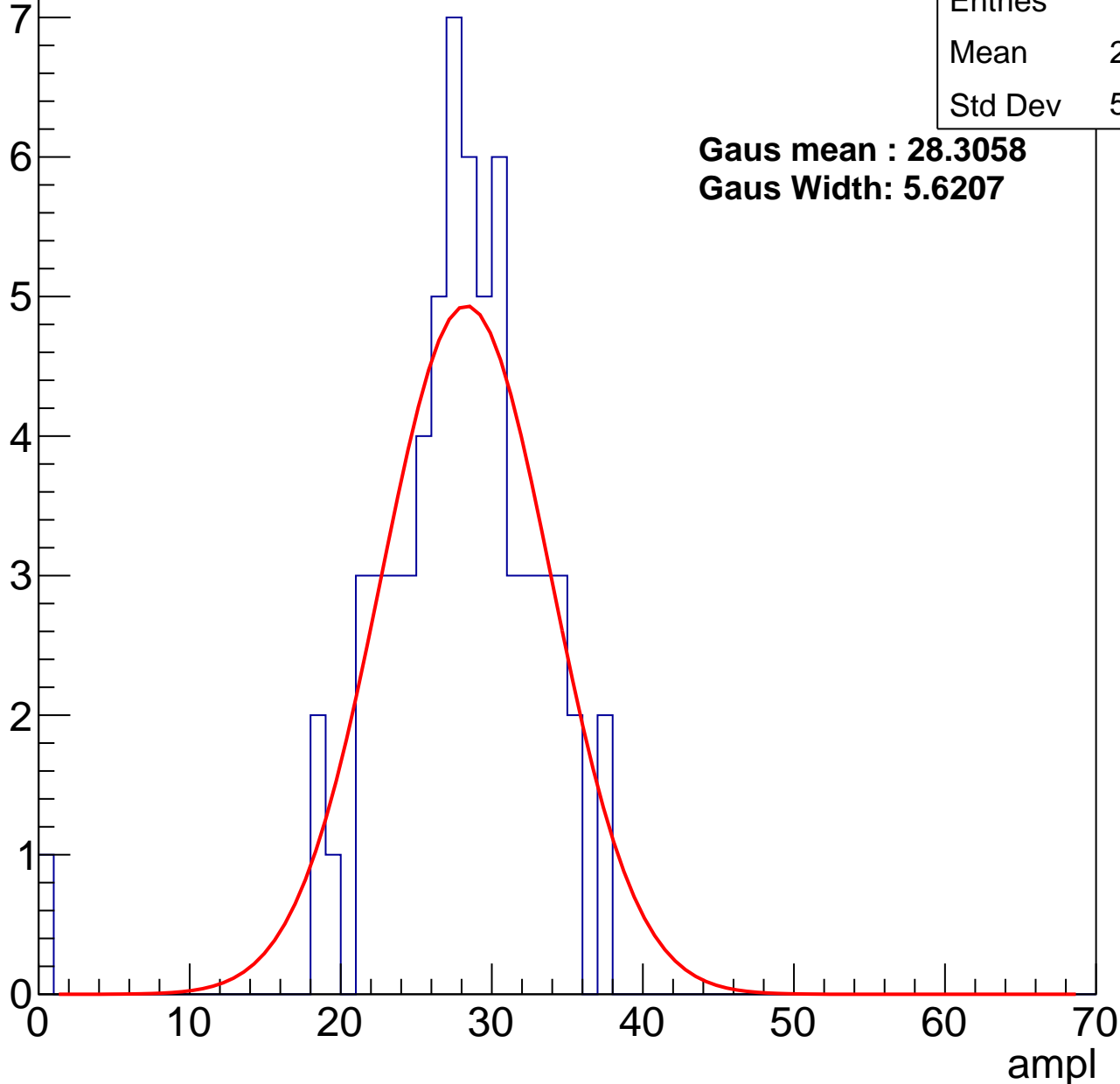
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	27.25
Std Dev	5.569

**Gaus mean : 28.3058**

**Gaus Width: 5.6207**



# B1L103S, U21-ch58, adc1

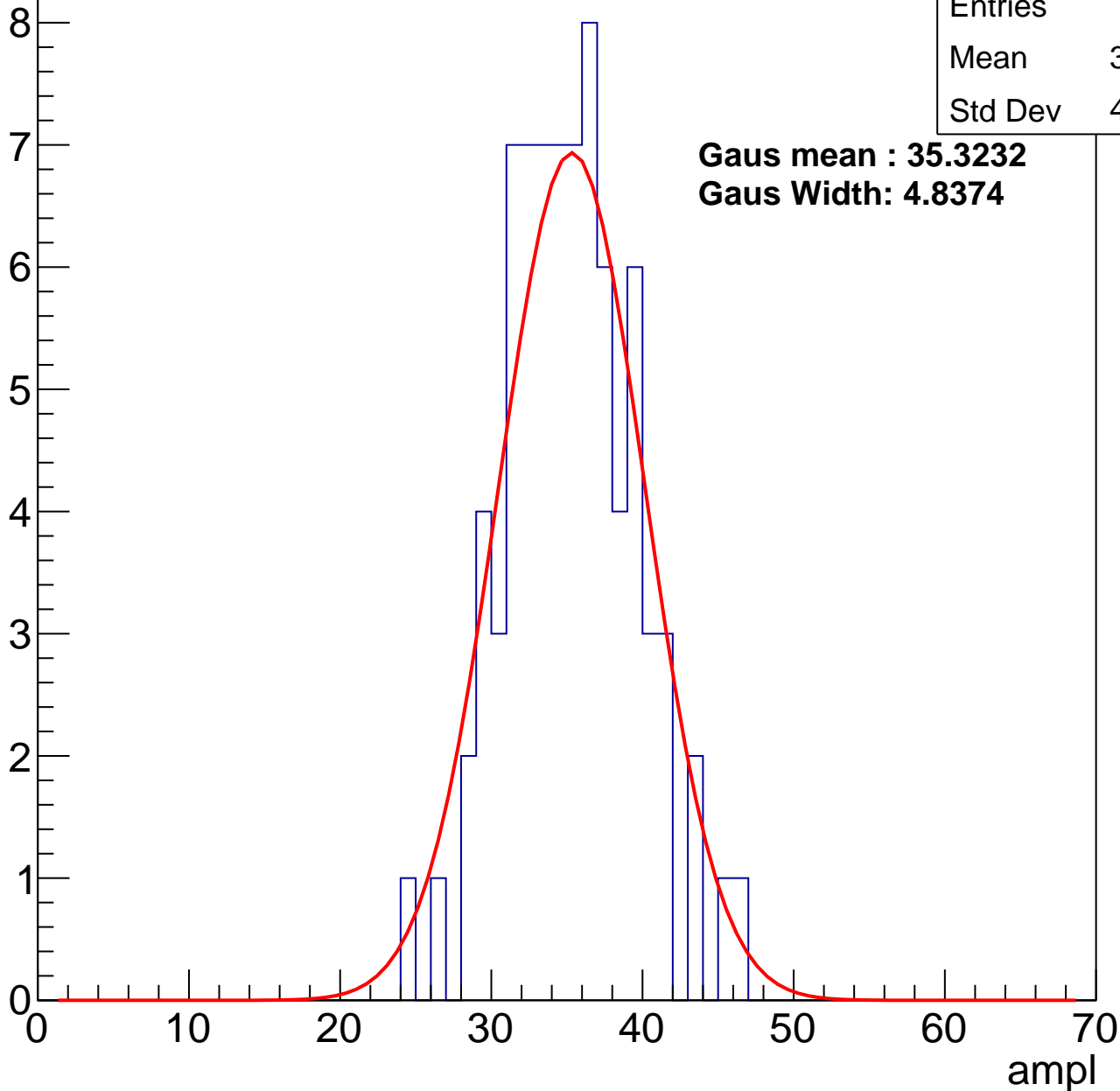
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	80
Mean	34.79
Std Dev	4.215

**Gaus mean : 35.3232**

**Gaus Width: 4.8374**



# B1L103S, U21-ch58, adc2

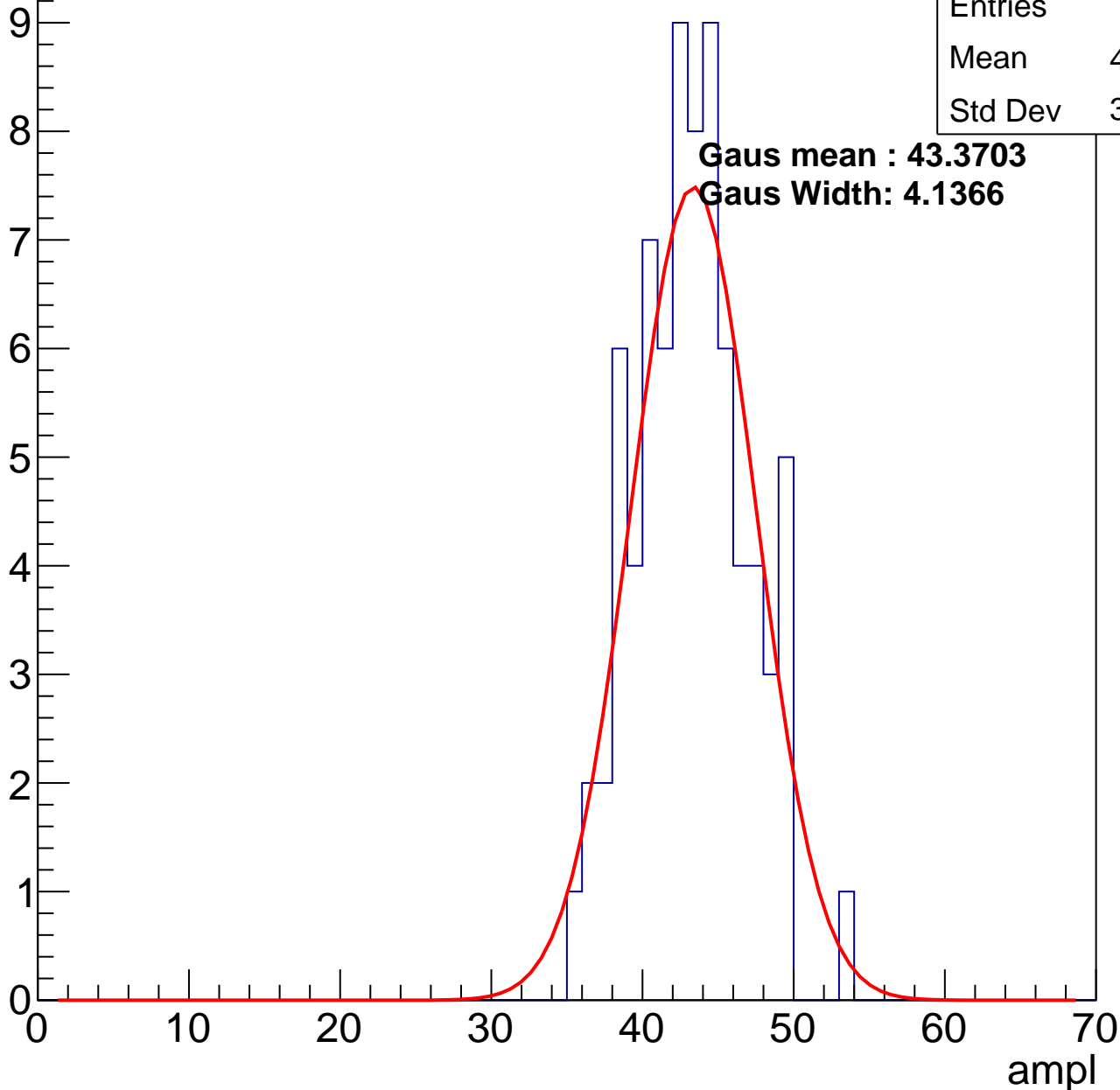
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	42.77
Std Dev	3.653

**Gaus mean : 43.3703**

**Gaus Width: 4.1366**

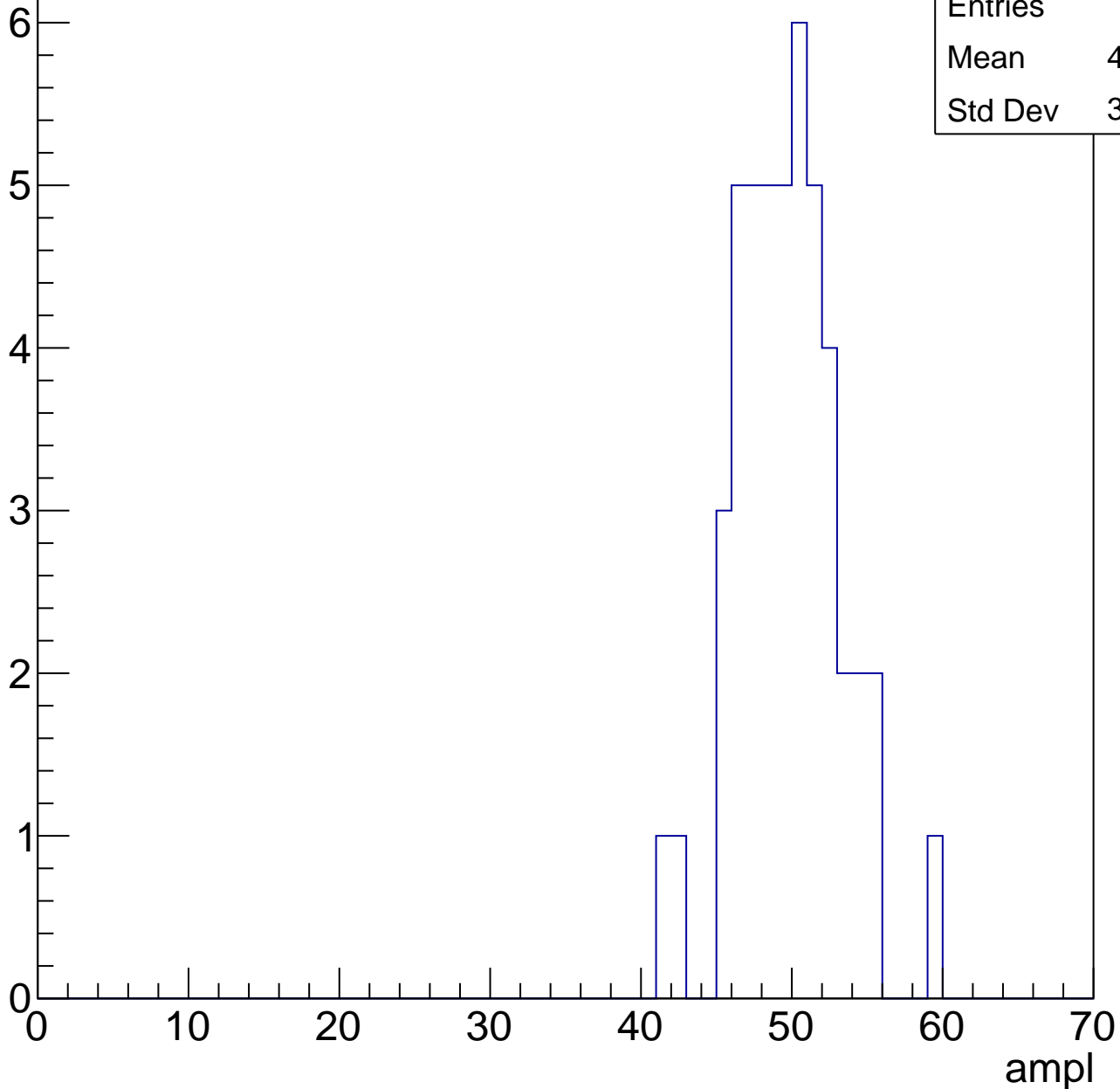


# B1L103S, U21-ch58, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

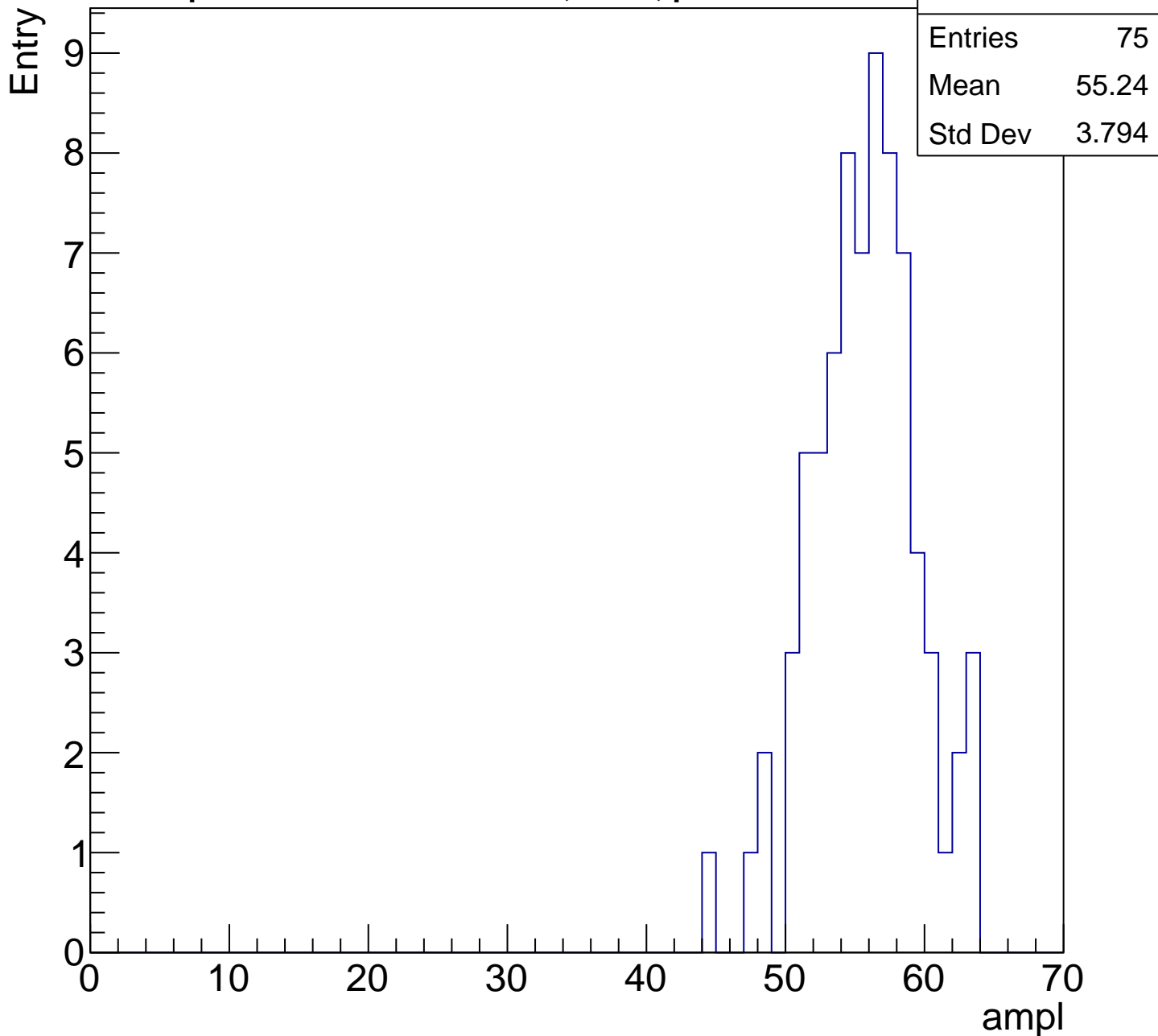
Entry

Entries	47
Mean	49.23
Std Dev	3.403



# B1L103S, U21-ch58, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U21-ch58, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

7

6

5

4

3

2

1

0

Entries	37
Mean	59.68
Std Dev	3.146

ampl

10

20

30

40

50

60

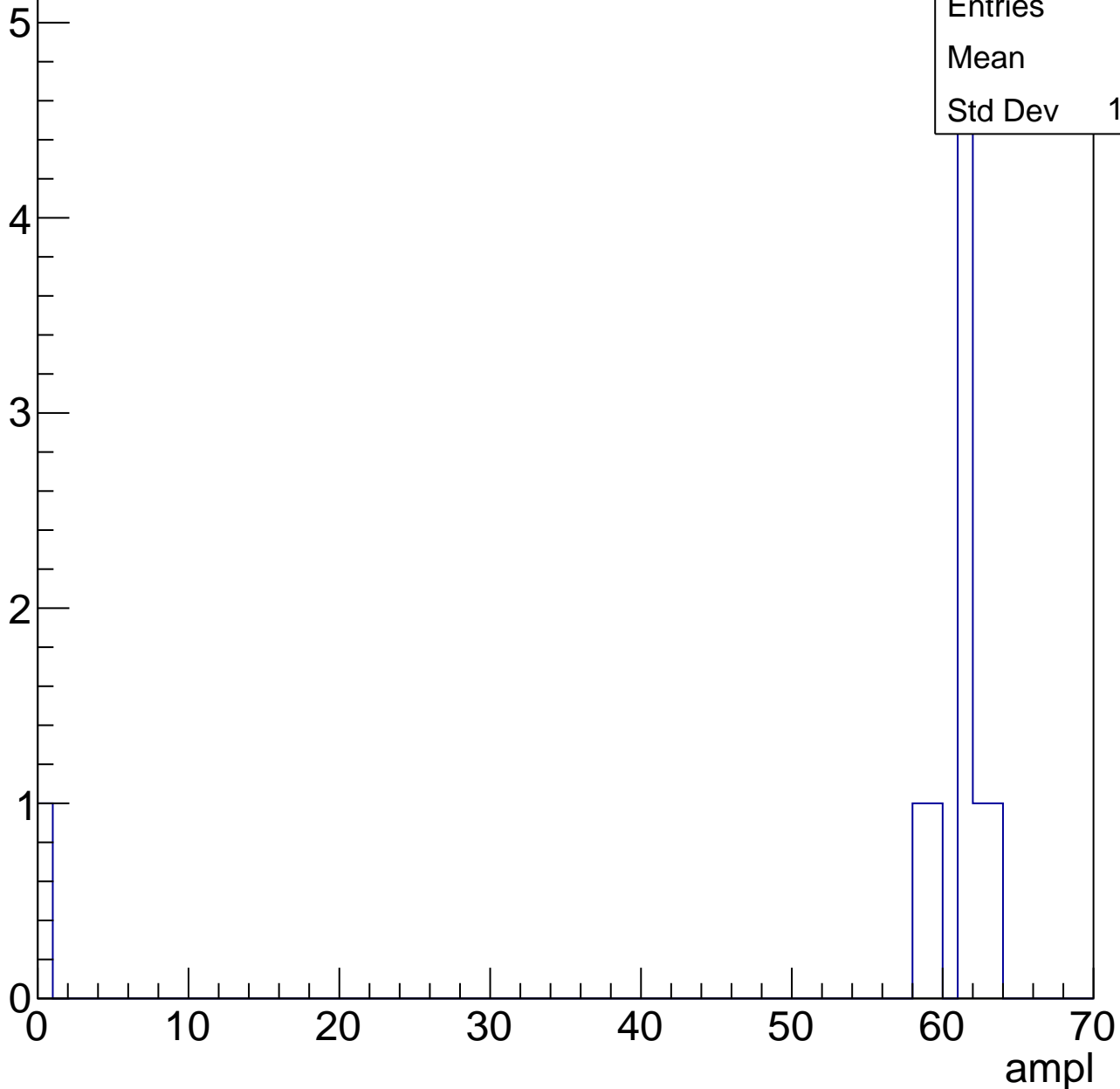
70

# B1L103S, U21-ch58, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	10
Mean	54.7
Std Dev	18.28





# B1L103S, U21-ch58, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U21-ch59, adc0

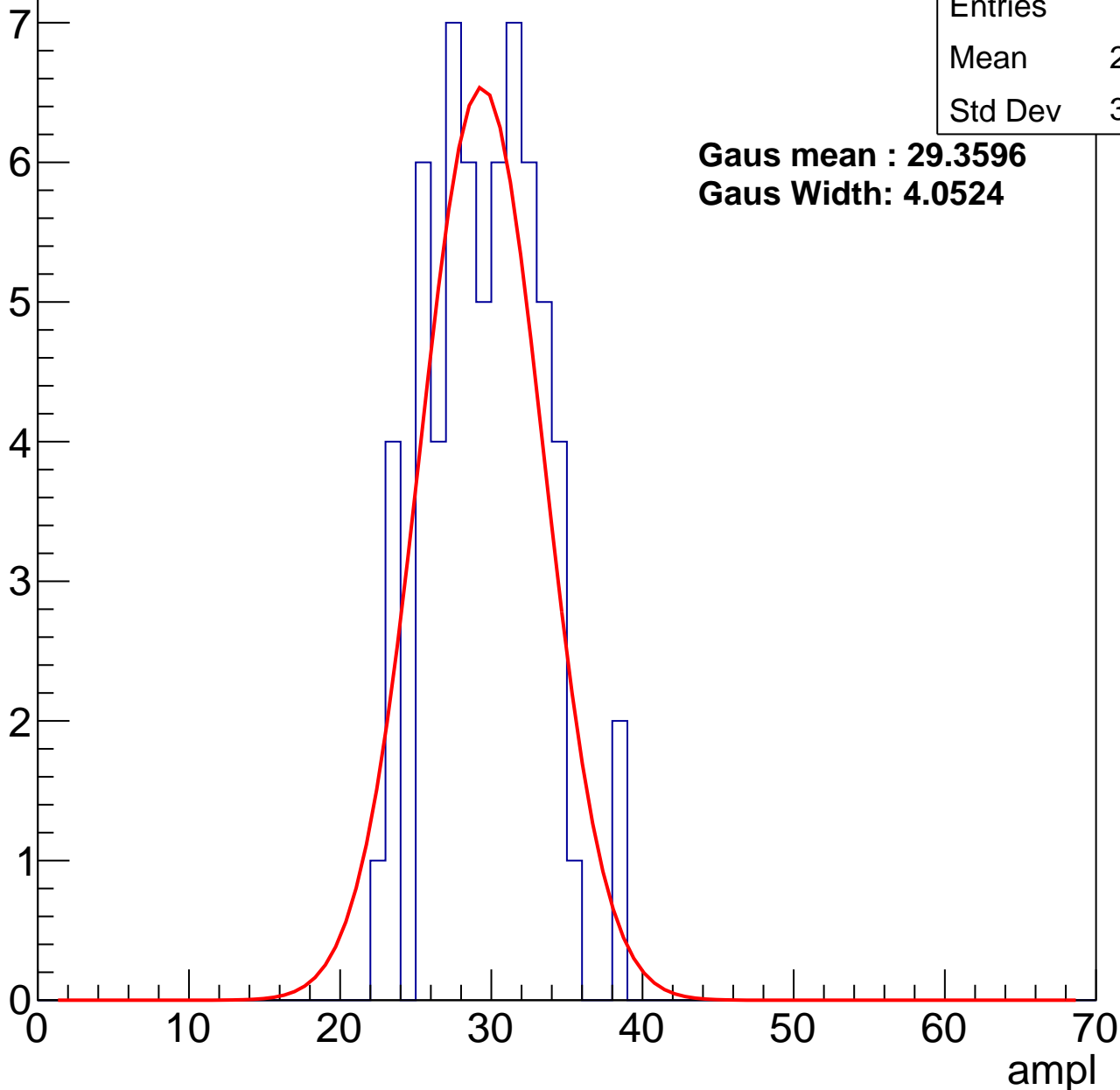
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	29.23
Std Dev	3.583

**Gaus mean : 29.3596**

**Gaus Width: 4.0524**



# B1L103S, U21-ch59, adc1

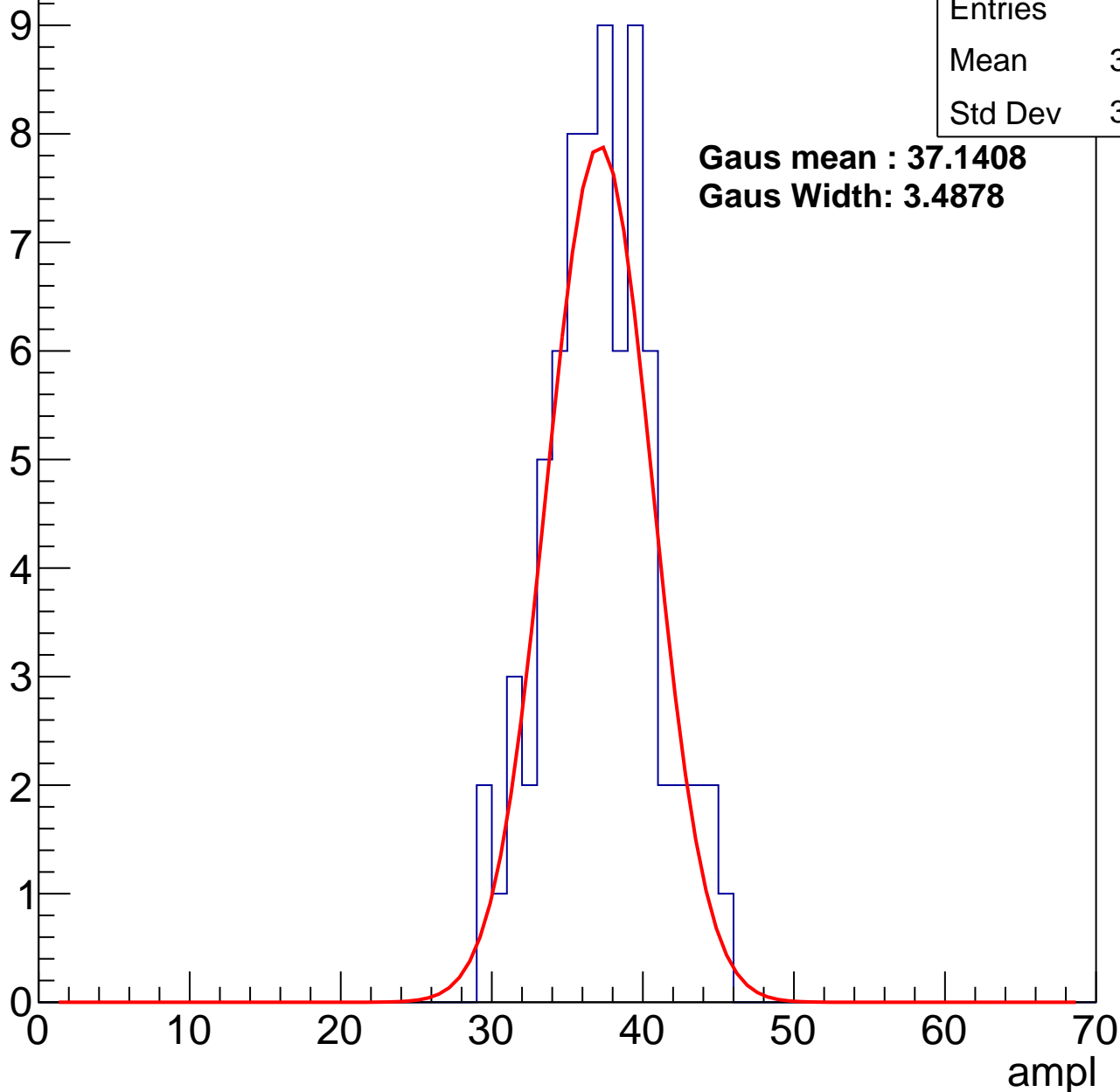
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	36.74
Std Dev	3.519

**Gaus mean : 37.1408**

**Gaus Width: 3.4878**

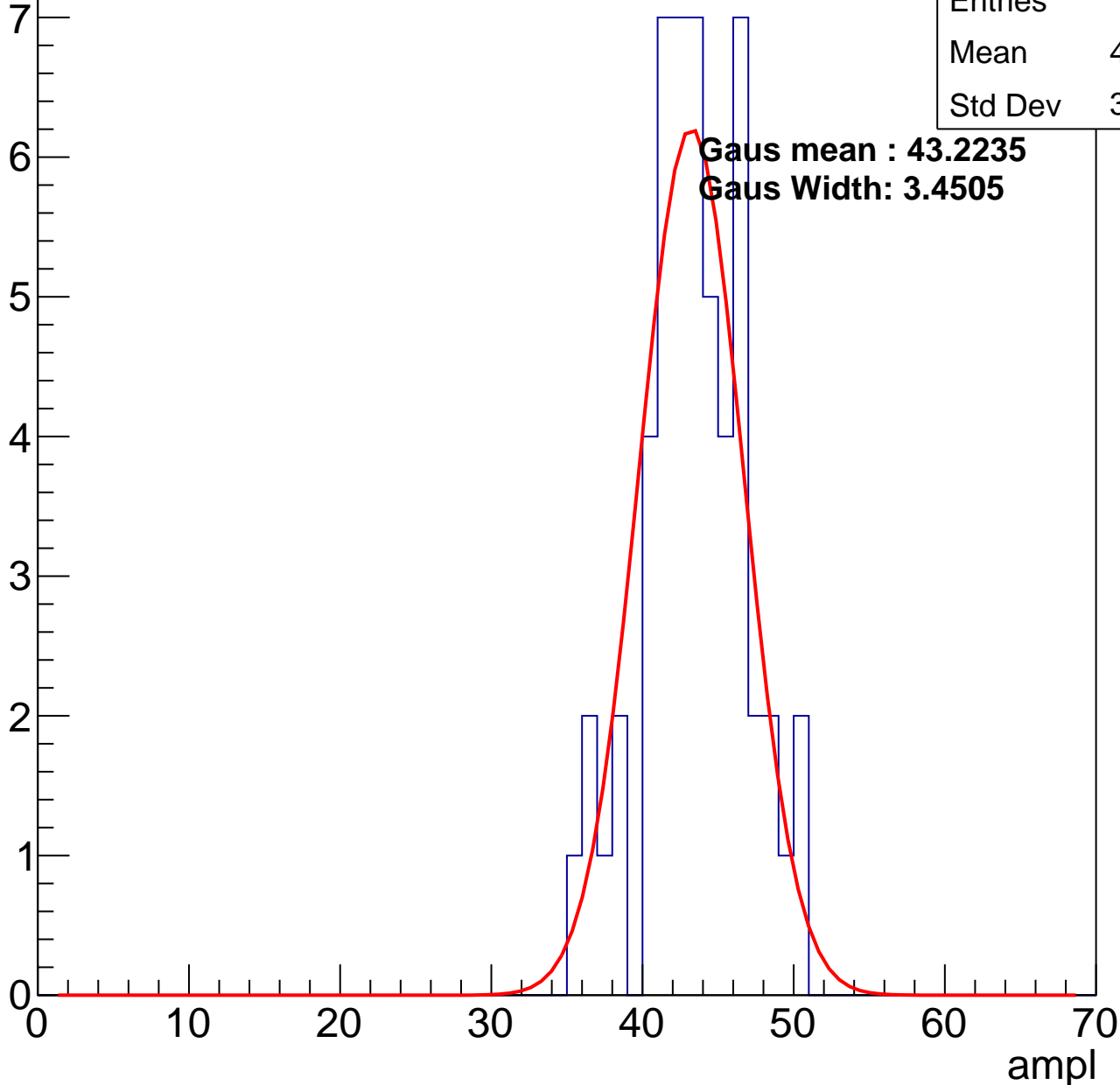


# B1L103S, U21-ch59, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	43.02
Std Dev	3.386

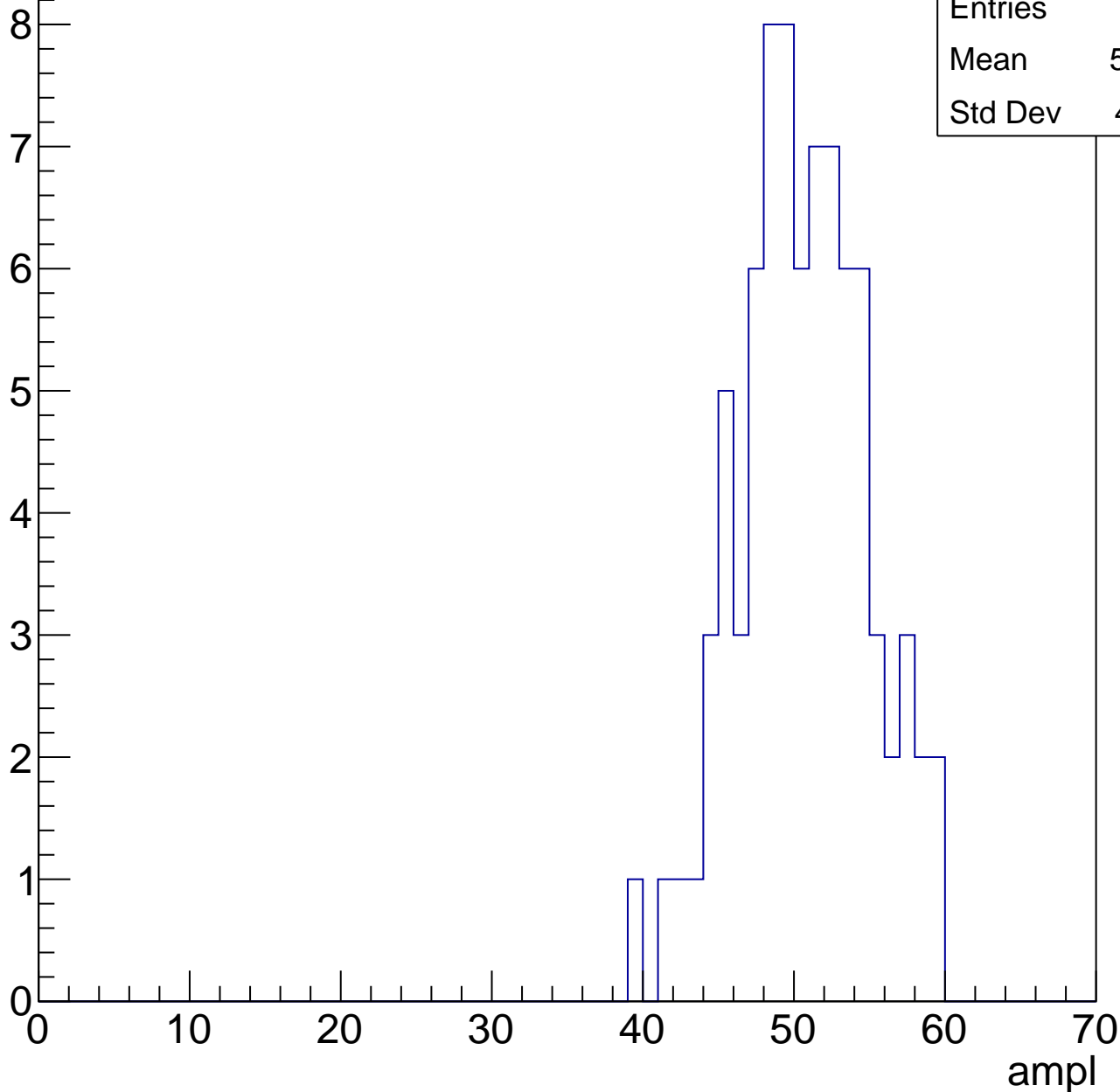


# B1L103S, U21-ch59, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	81
Mean	50.16
Std Dev	4.241

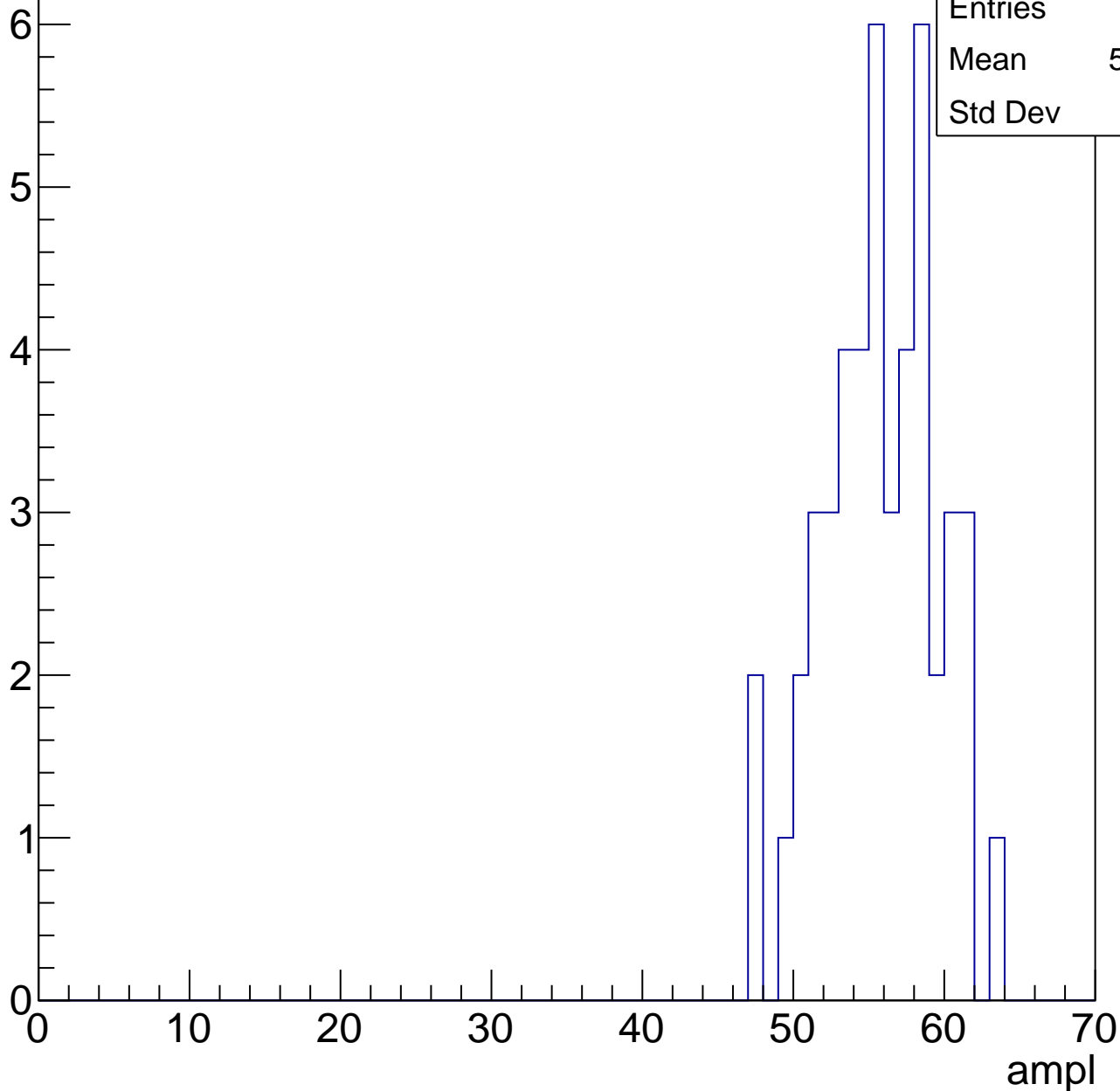


# B1L103S, U21-ch59, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	47
Mean	55.28
Std Dev	3.74

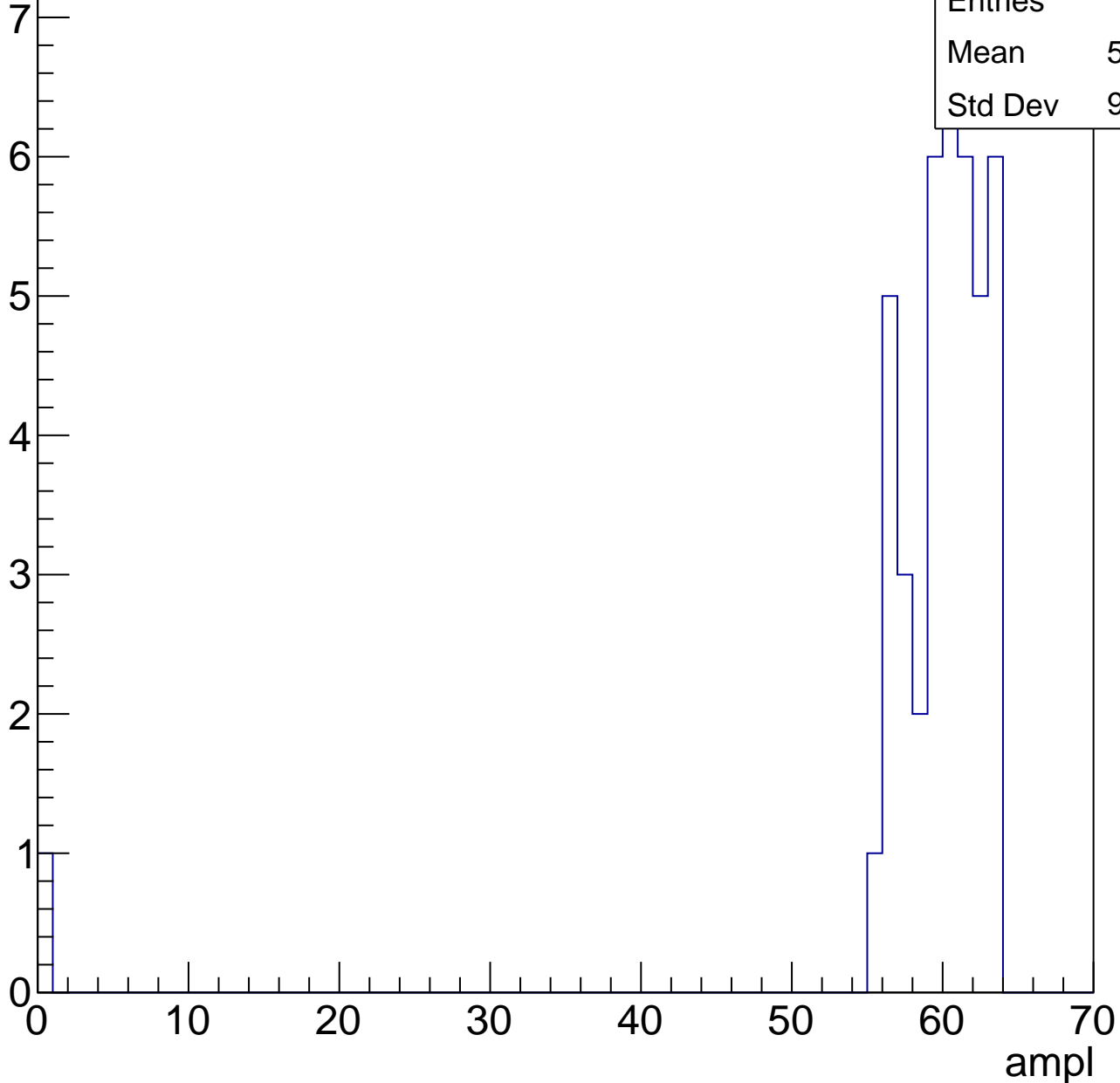


# B1L103S, U21-ch59, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	42
Mean	58.33
Std Dev	9.398



# B1L103S, U21-ch59, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U21-ch59, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U21-ch60, adc0

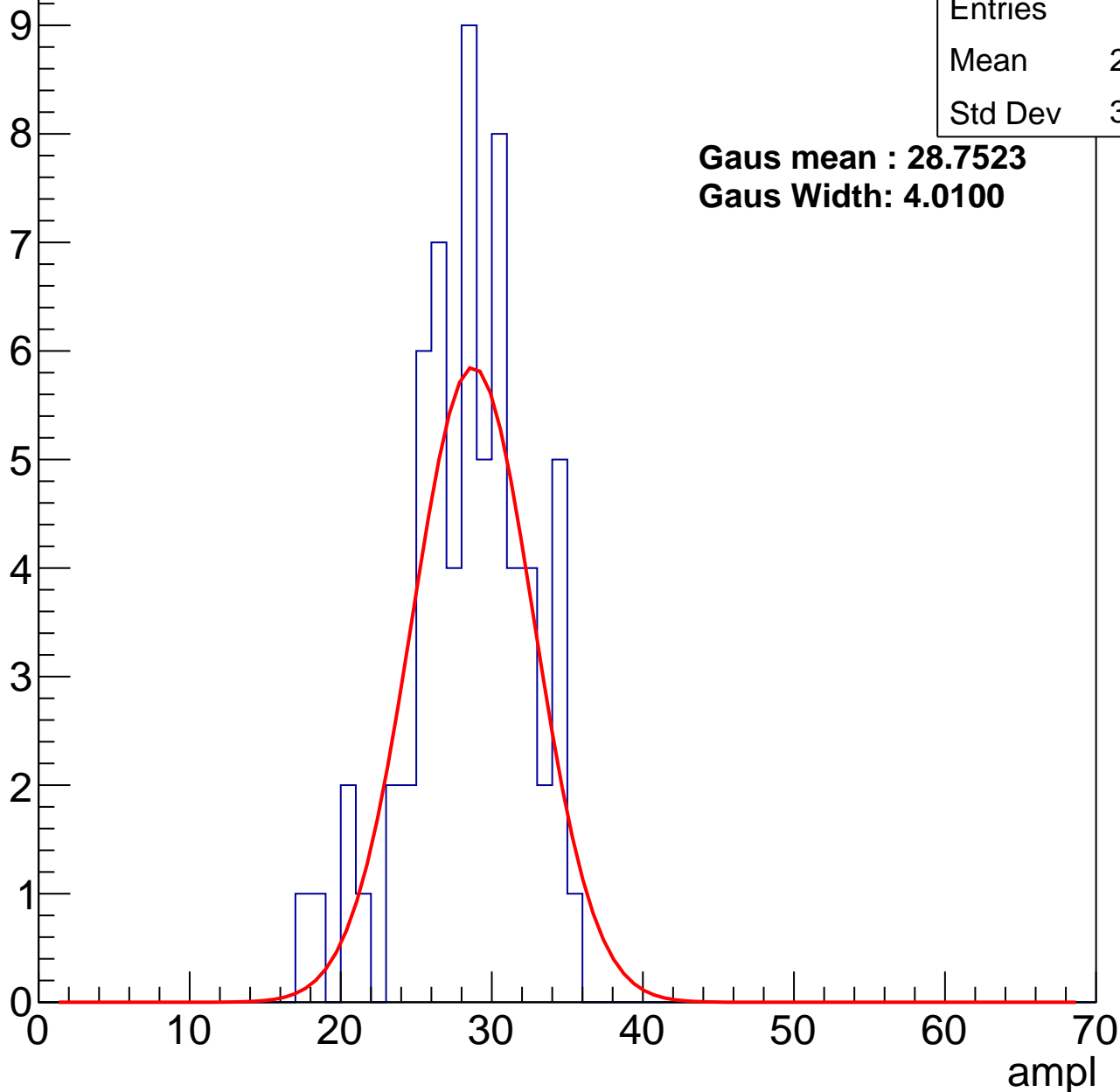
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	27.97
Std Dev	3.917

**Gaus mean : 28.7523**

**Gaus Width: 4.0100**



# B1L103S, U21-ch60, adc1

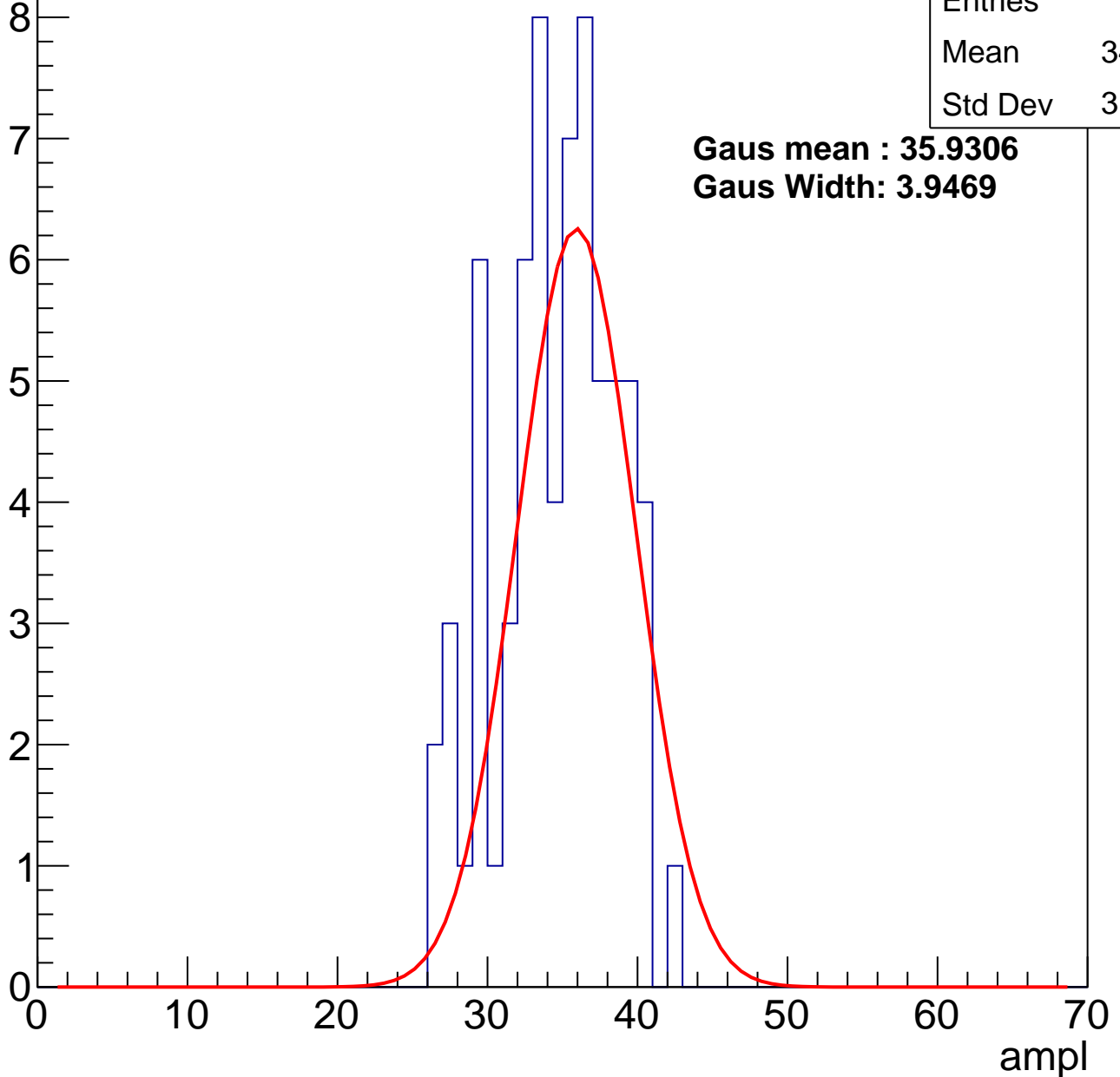
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	34.13
Std Dev	3.867

**Gaus mean : 35.9306**

**Gaus Width: 3.9469**



# B1L103S, U21-ch60, adc2

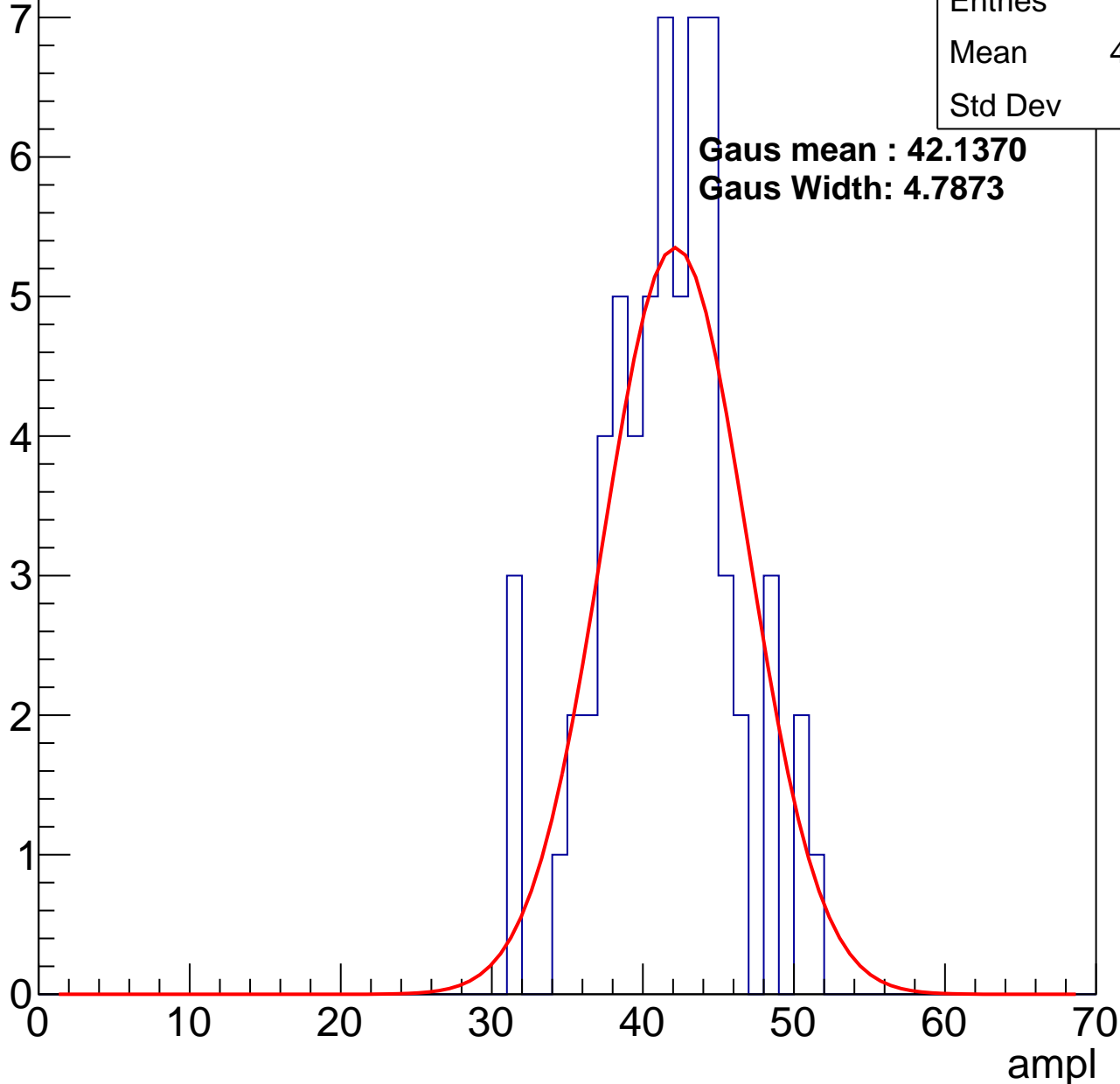
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	41.13
Std Dev	4.37

**Gaus mean : 42.1370**

**Gaus Width: 4.7873**

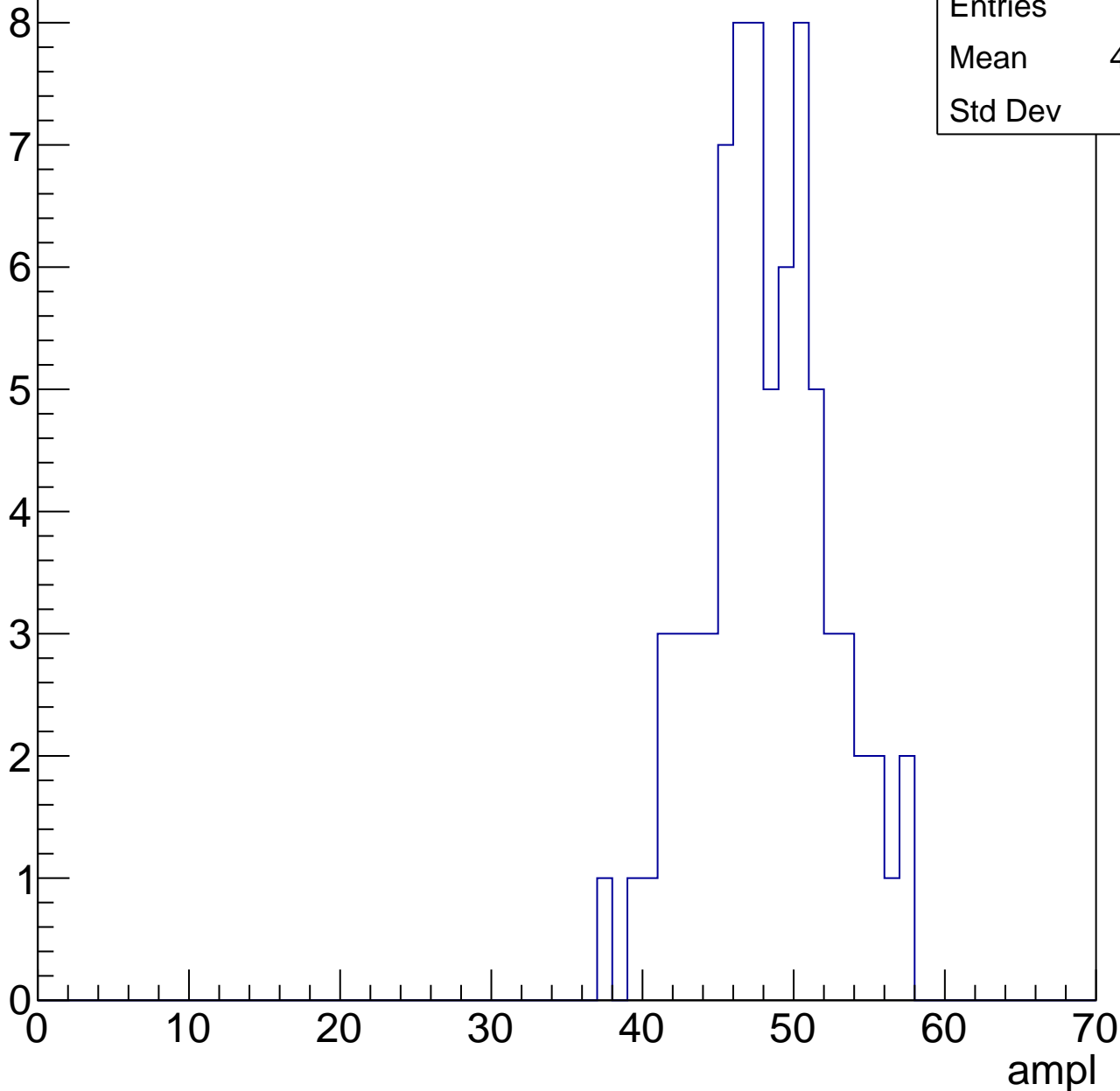


# B1L103S, U21-ch60, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

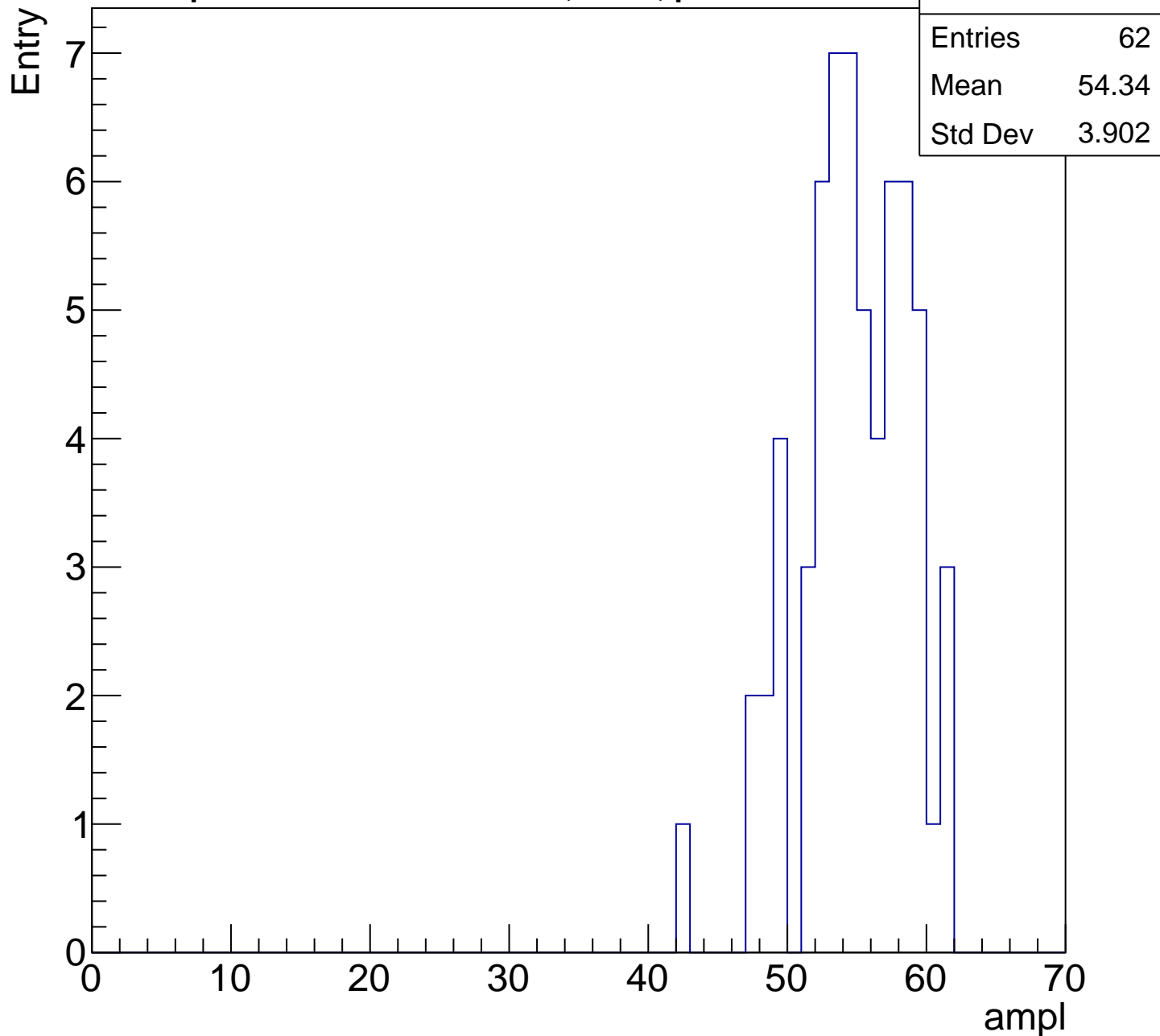
Entry

Entries	75
Mean	47.69
Std Dev	4.23



# B1L103S, U21-ch60, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

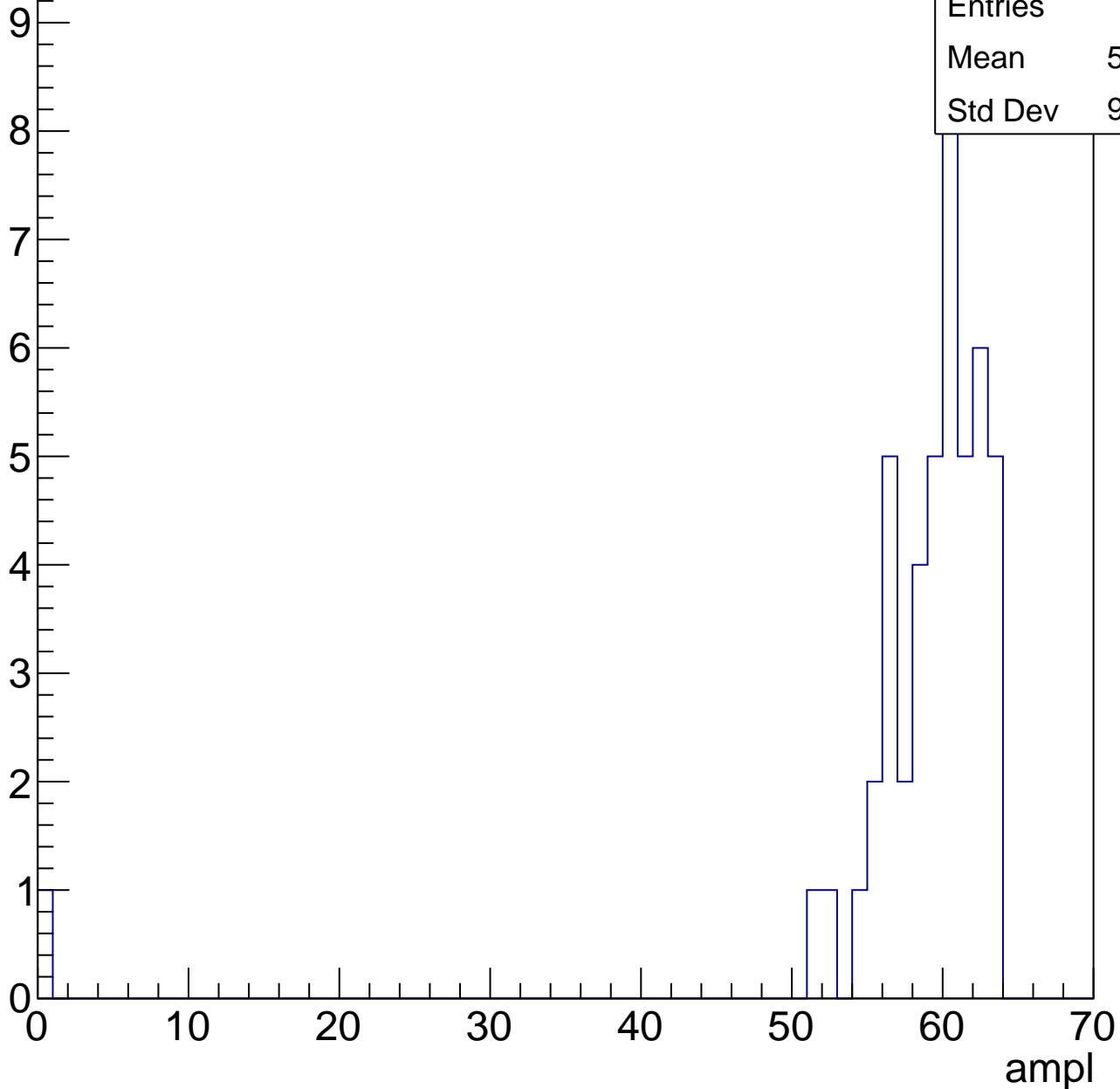


# B1L103S, U21-ch60, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

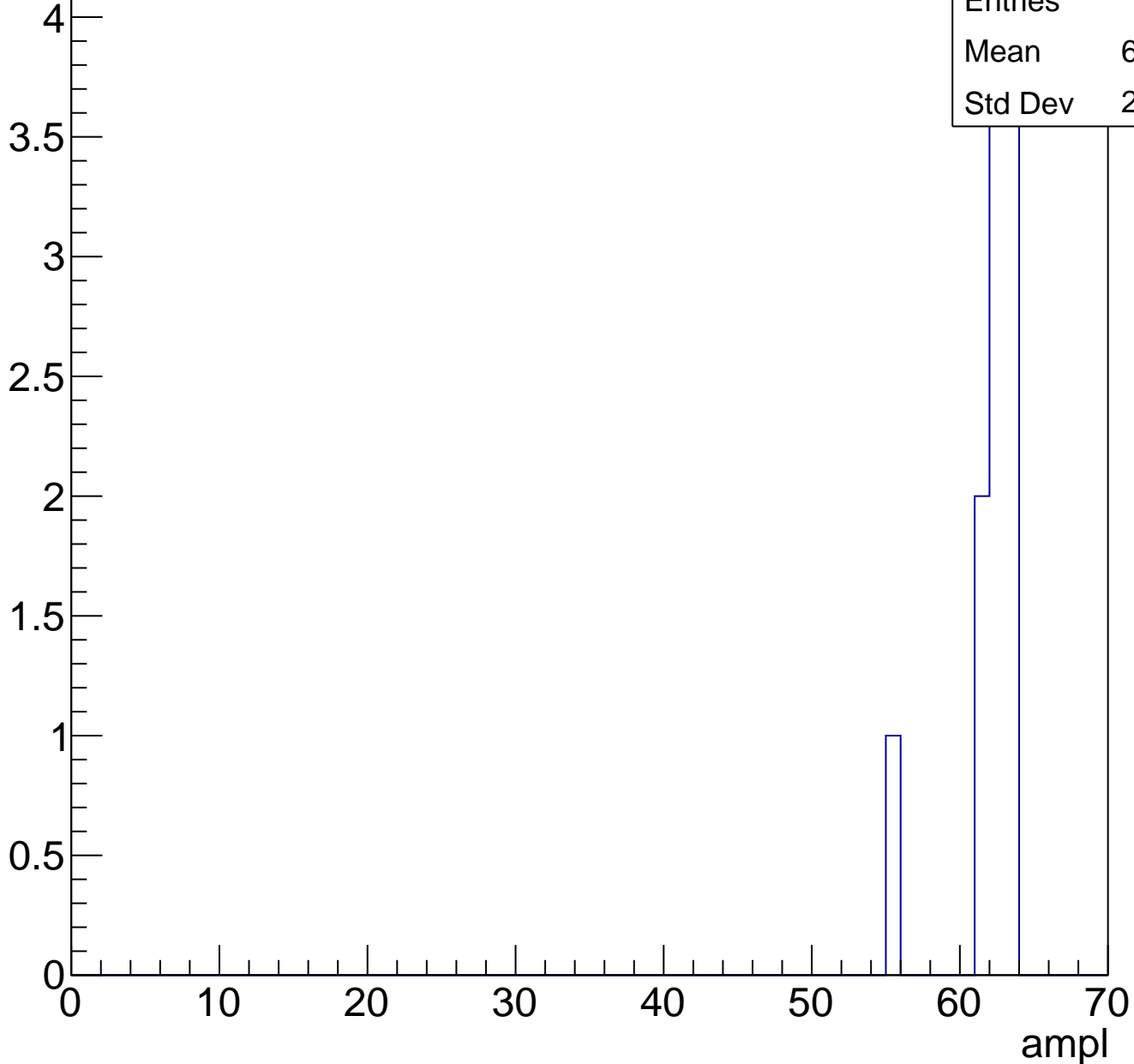
Entries	47
Mean	57.87
Std Dev	9.005



# B1L103S, U21-ch60, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U21-ch60, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U21-ch61, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	83
Mean	28.57
Std Dev	5.97

**Gaus mean : 30.0922**

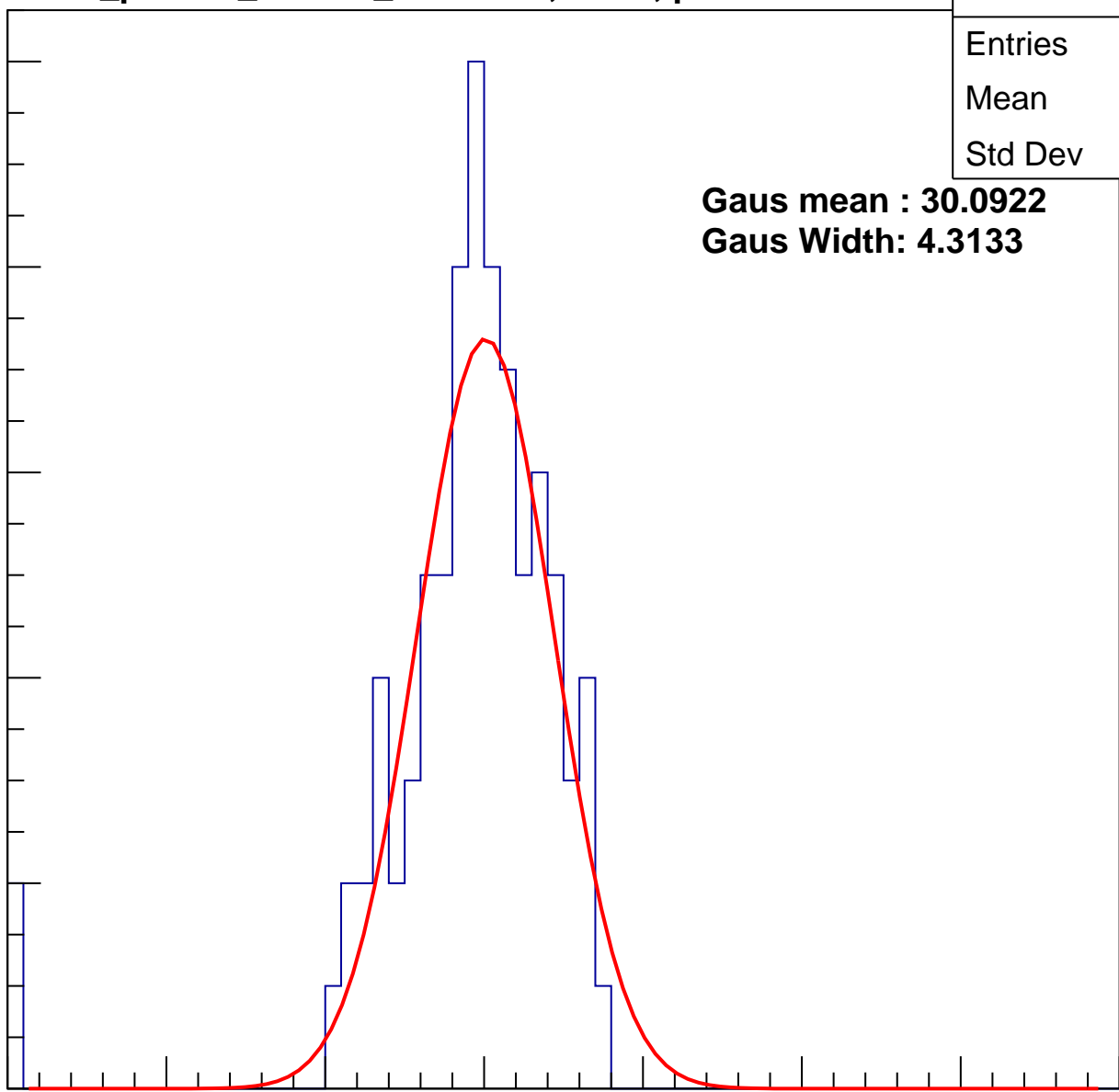
**Gaus Width: 4.3133**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U21-ch61, adc1

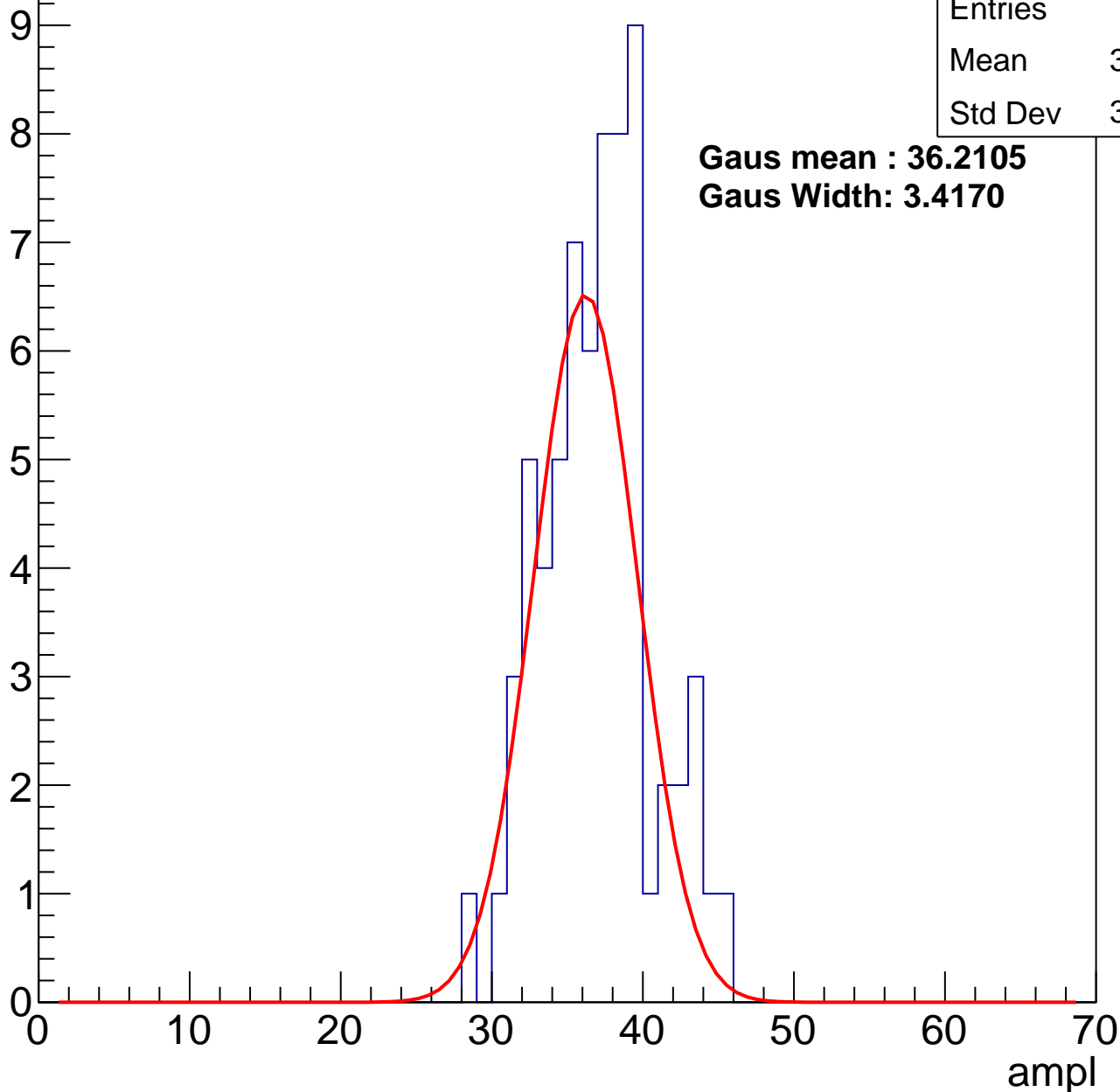
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	36.55
Std Dev	3.559

**Gaus mean : 36.2105**

**Gaus Width: 3.4170**



# B1L103S, U21-ch61, adc2

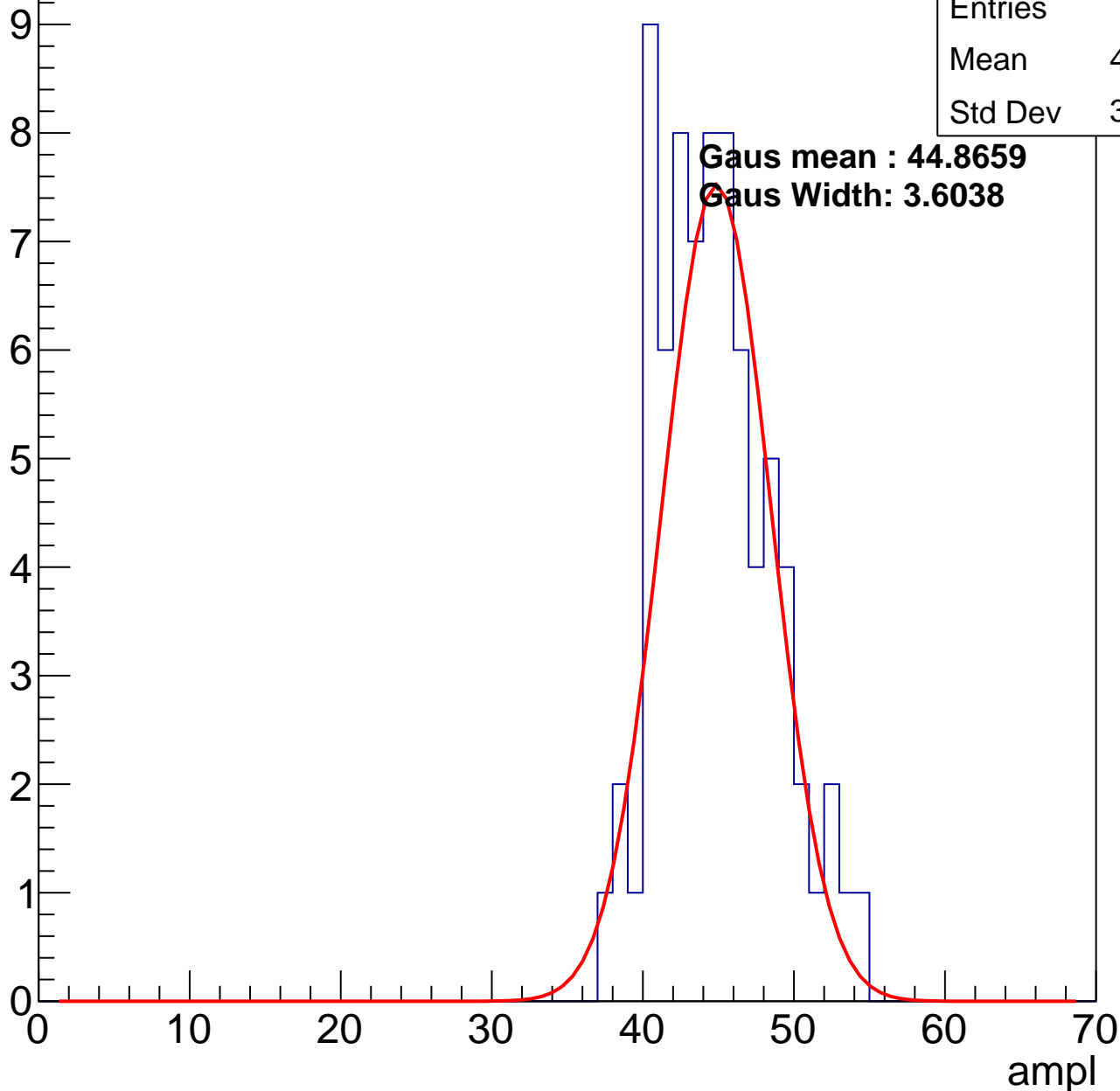
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	44.33
Std Dev	3.722

**Gaus mean : 44.8659**

**Gaus Width: 3.6038**

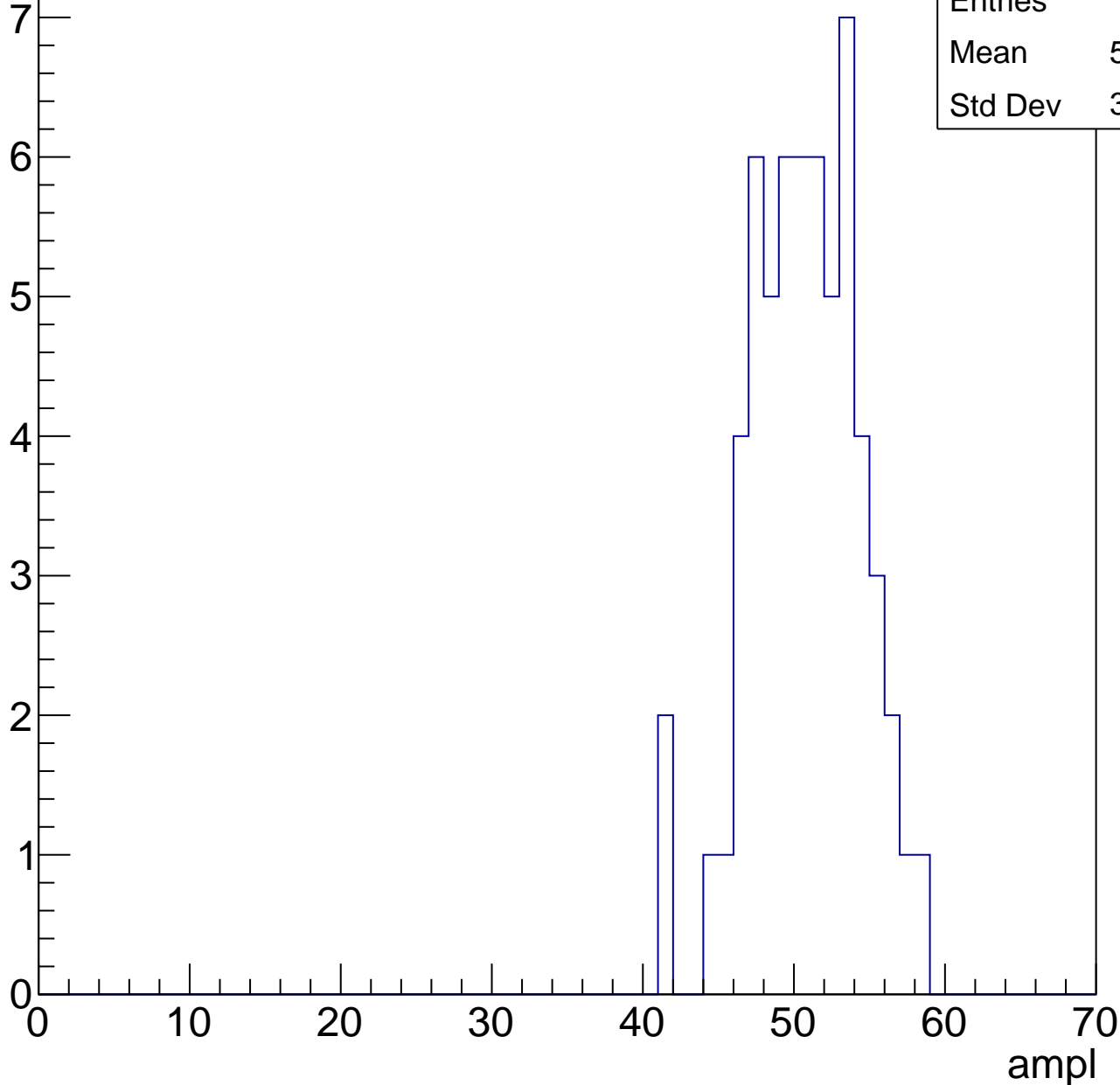


# B1L103S, U21-ch61, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

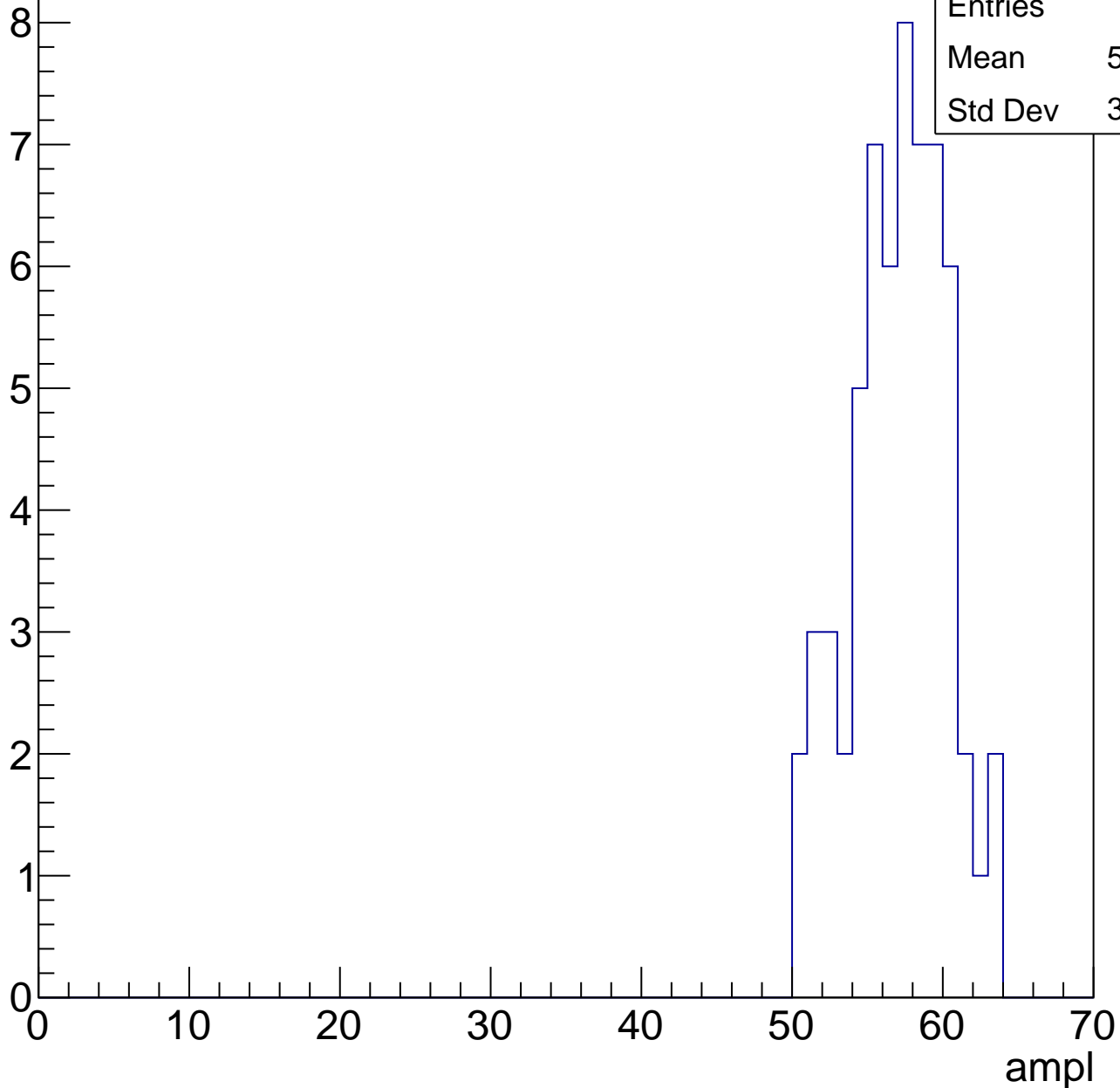
Entries	60
Mean	50.27
Std Dev	3.596



# B1L103S, U21-ch61, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

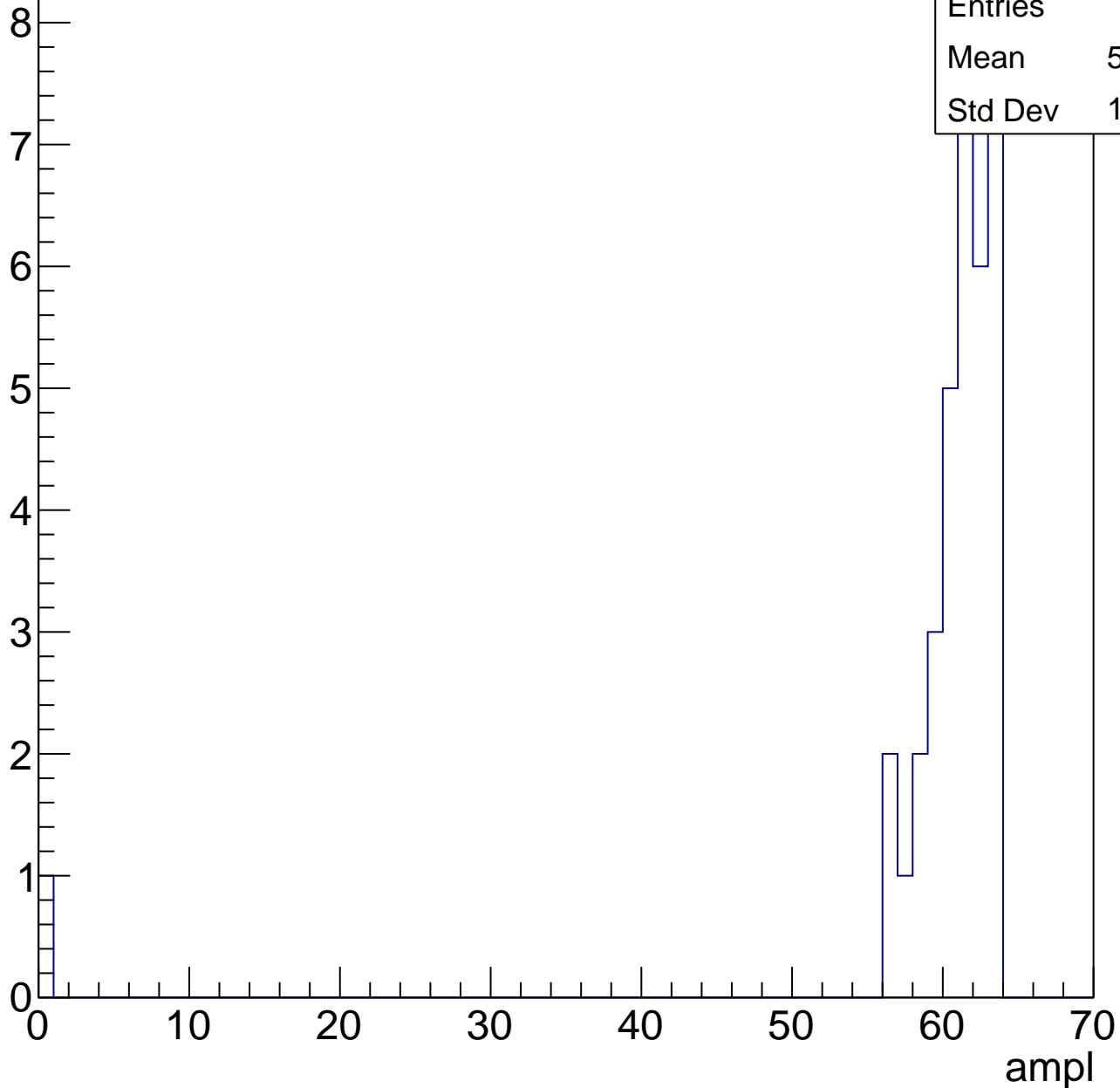


# B1L103S, U21-ch61, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	36
Mean	59.06
Std Dev	10.17



# B1L103S, U21-ch61, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U21-ch61, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L103S, U21-ch62, adc0

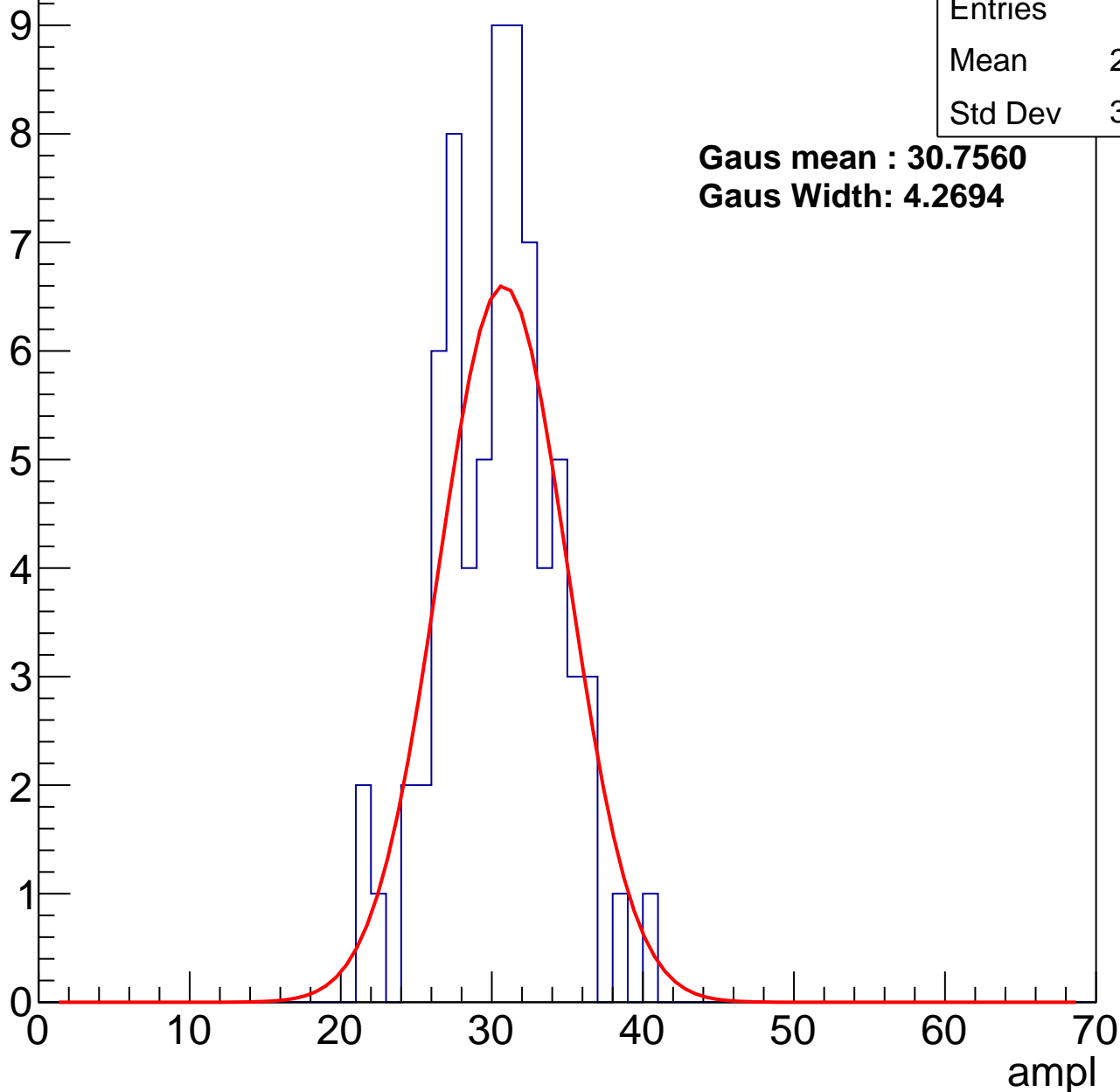
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	29.96
Std Dev	3.795

**Gaus mean : 30.7560**

**Gaus Width: 4.2694**



# B1L103S, U21-ch62, adc1

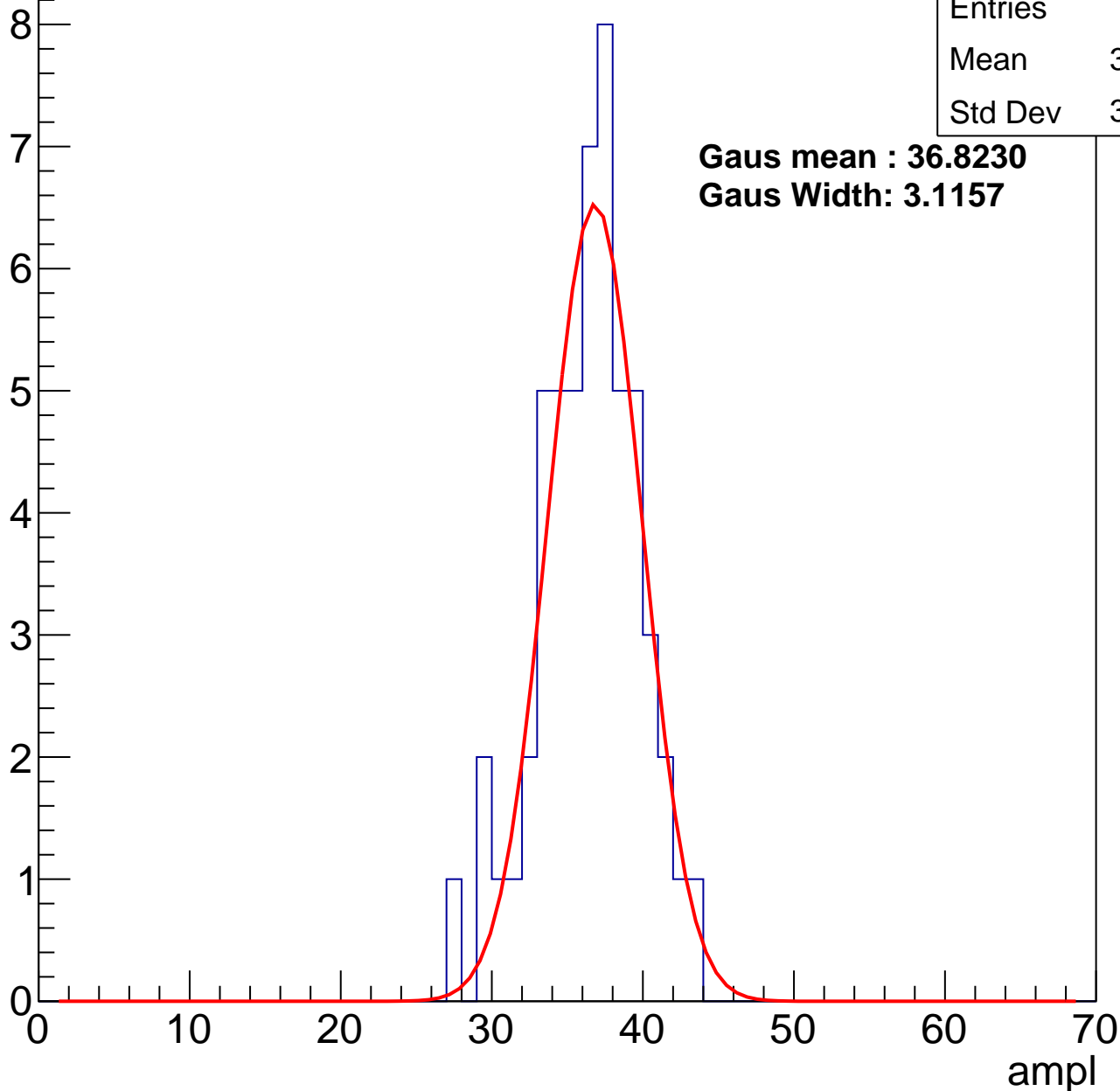
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	35.93
Std Dev	3.327

**Gaus mean : 36.8230**

**Gaus Width: 3.1157**



# B1L103S, U21-ch62, adc2

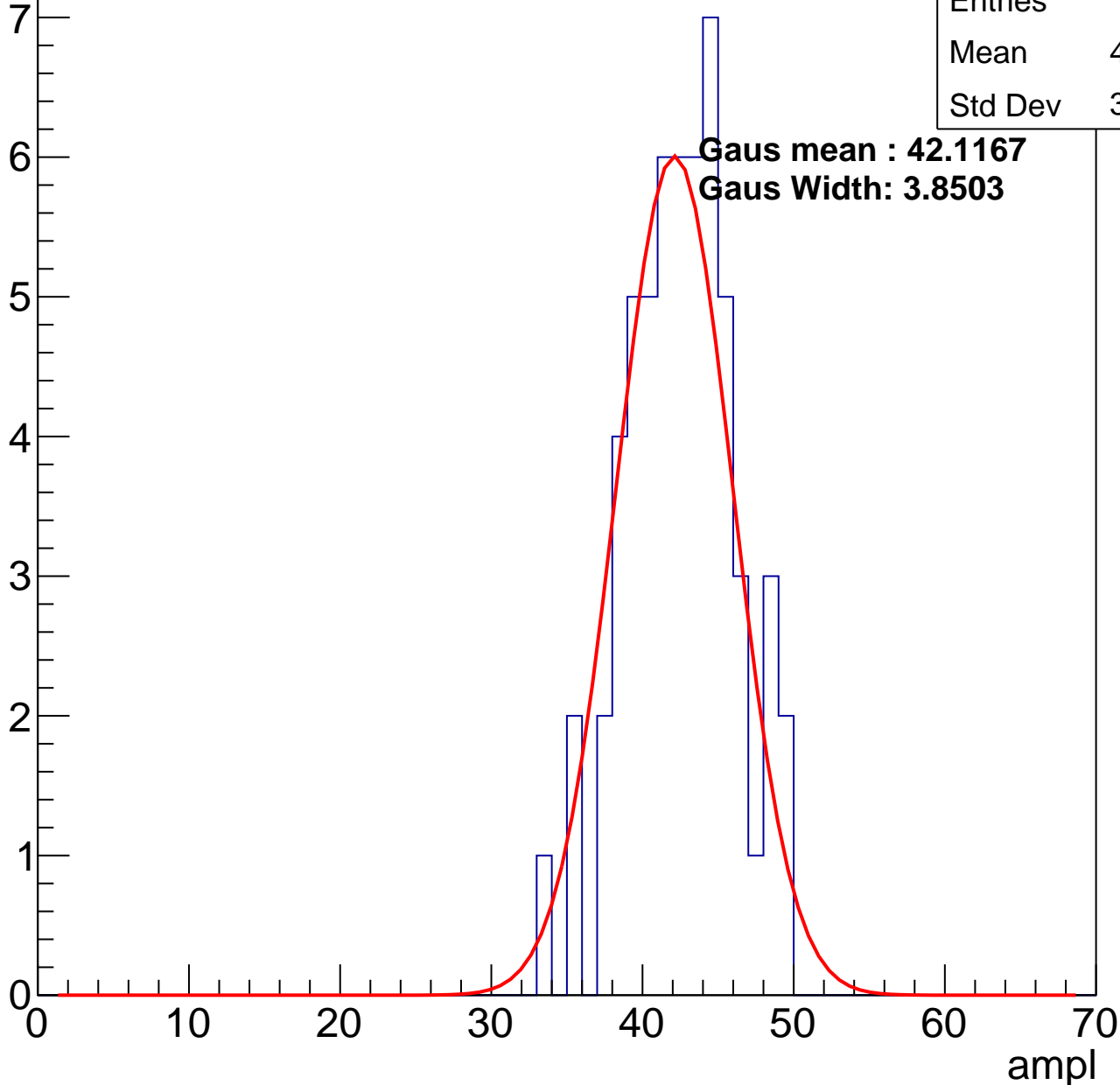
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	42.07
Std Dev	3.528

**Gaus mean : 42.1167**

**Gaus Width: 3.8503**

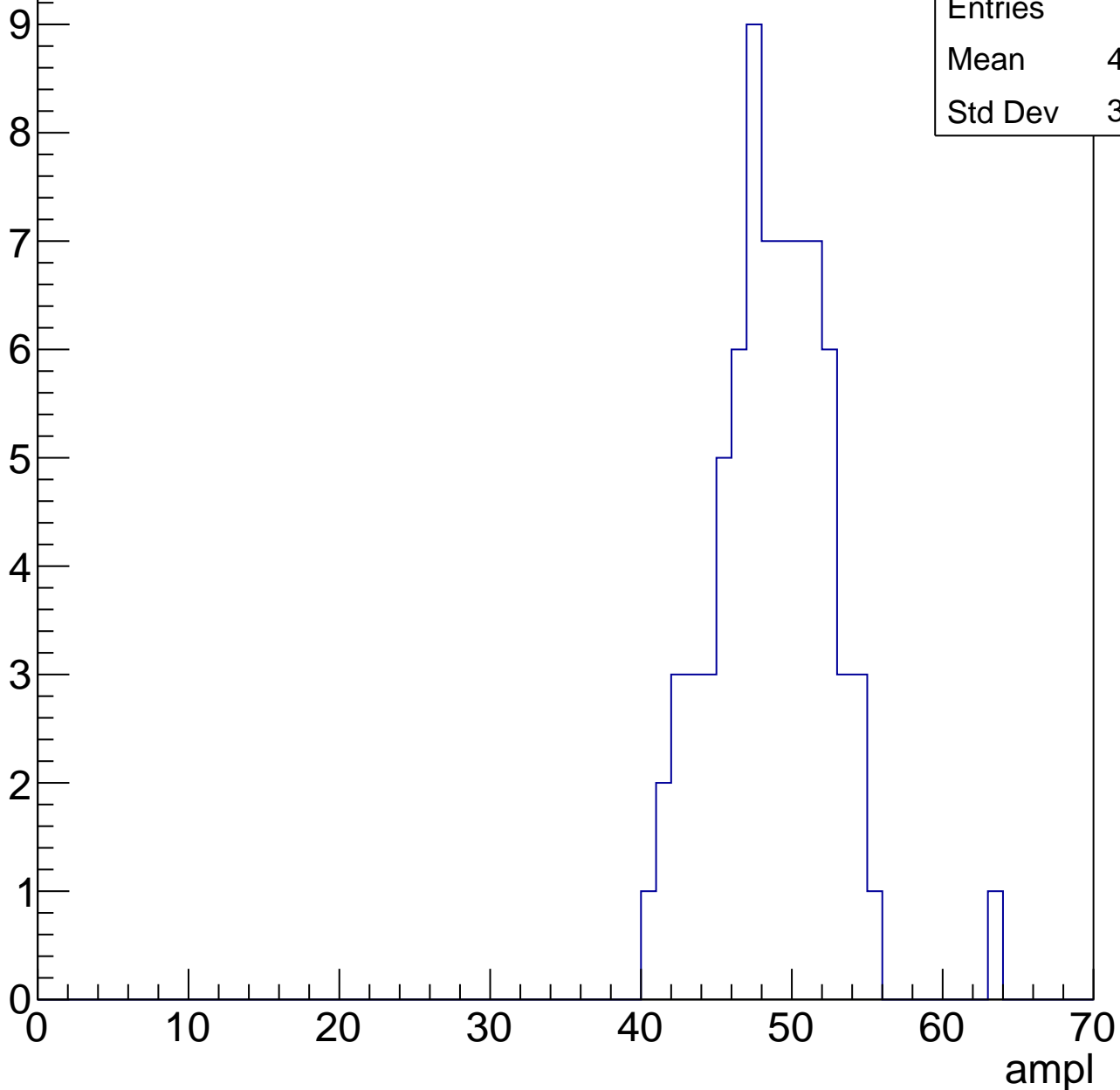


# B1L103S, U21-ch62, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

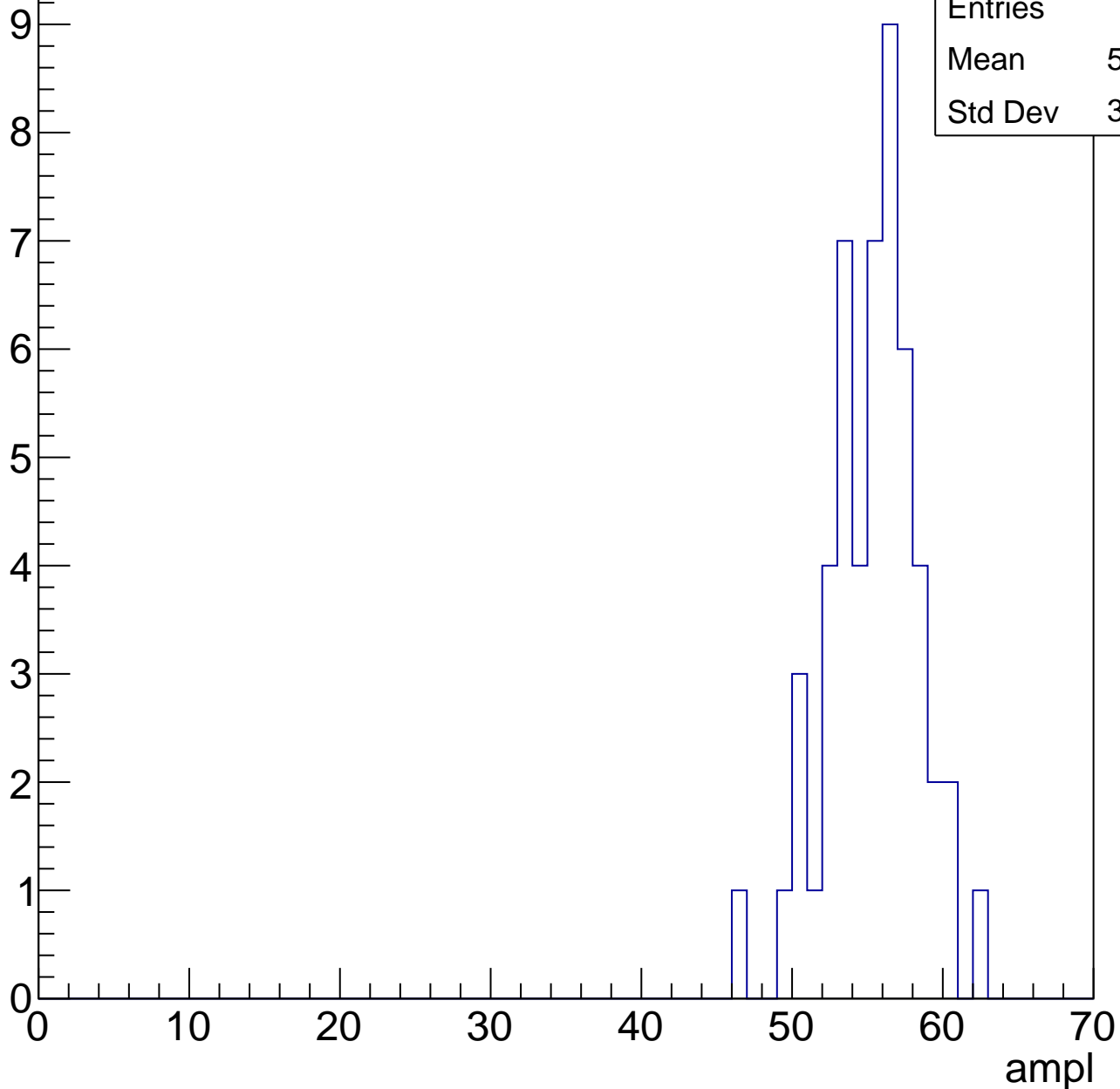
Entries	74
Mean	48.24
Std Dev	3.886



# B1L103S, U21-ch62, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

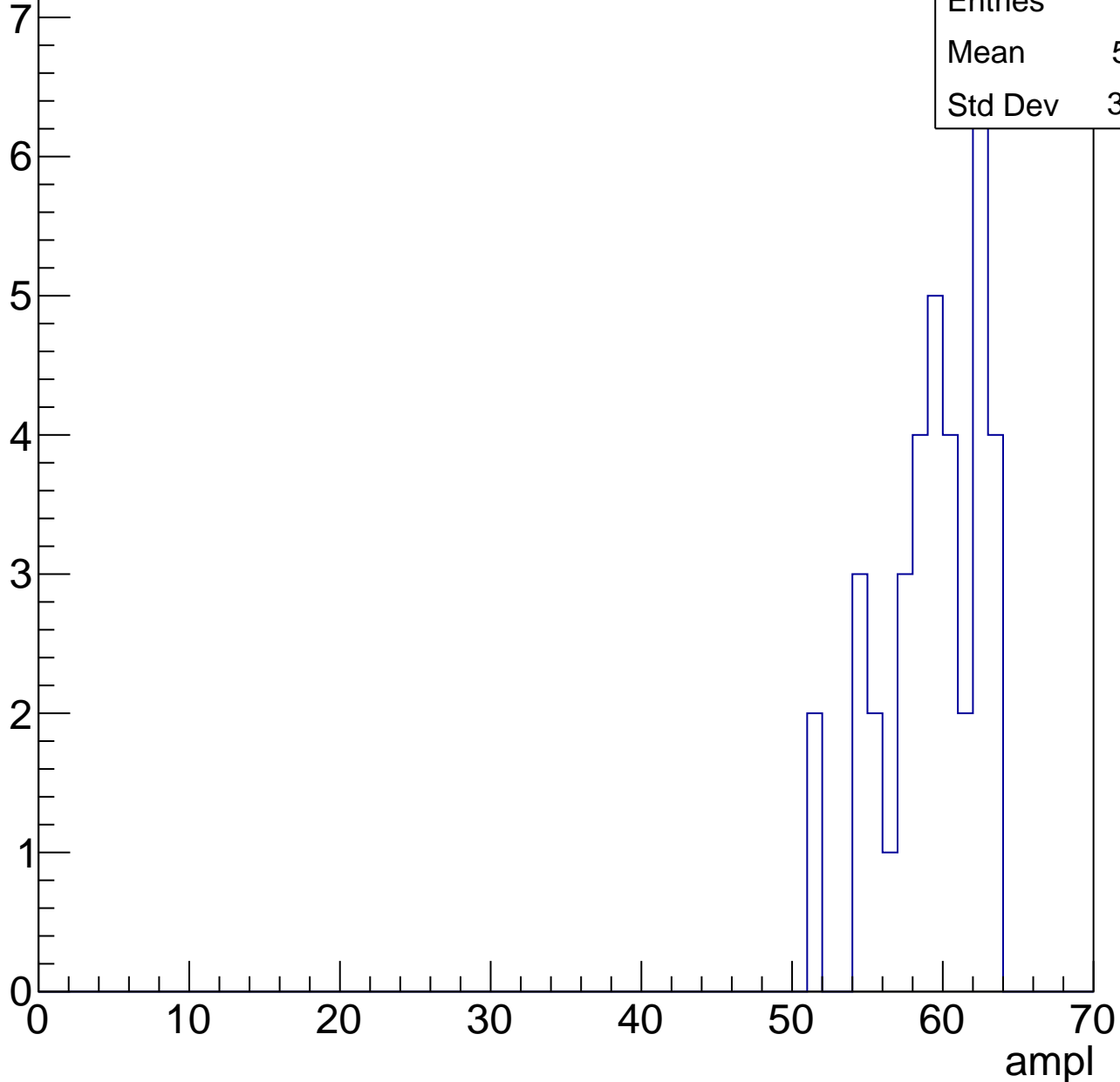


# B1L103S, U21-ch62, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	37
Mean	58.81
Std Dev	3.278

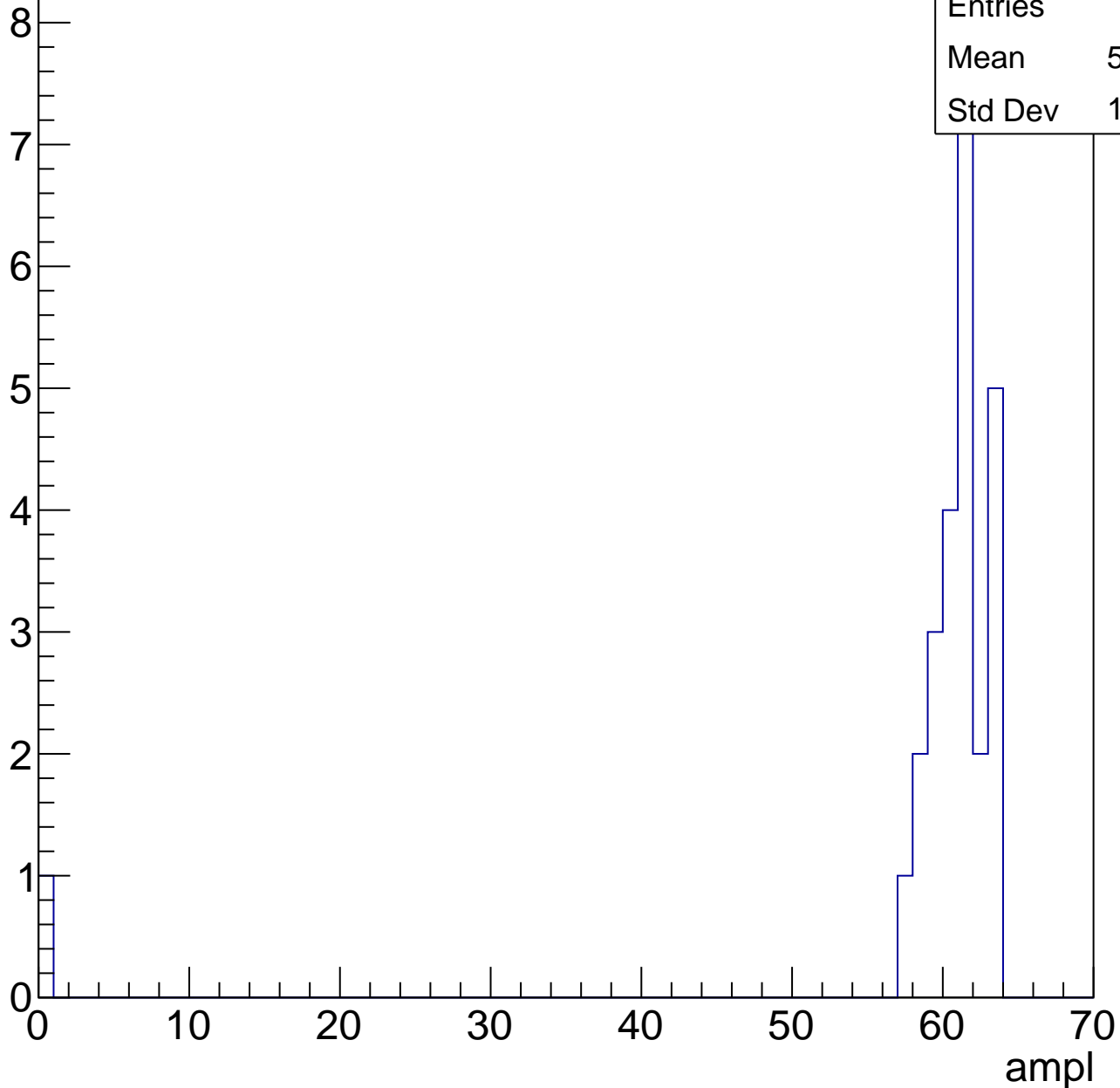


# B1L103S, U21-ch62, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	26
Mean	58.35
Std Dev	11.78





# B1L103S, U21-ch62, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U21-ch63, adc0

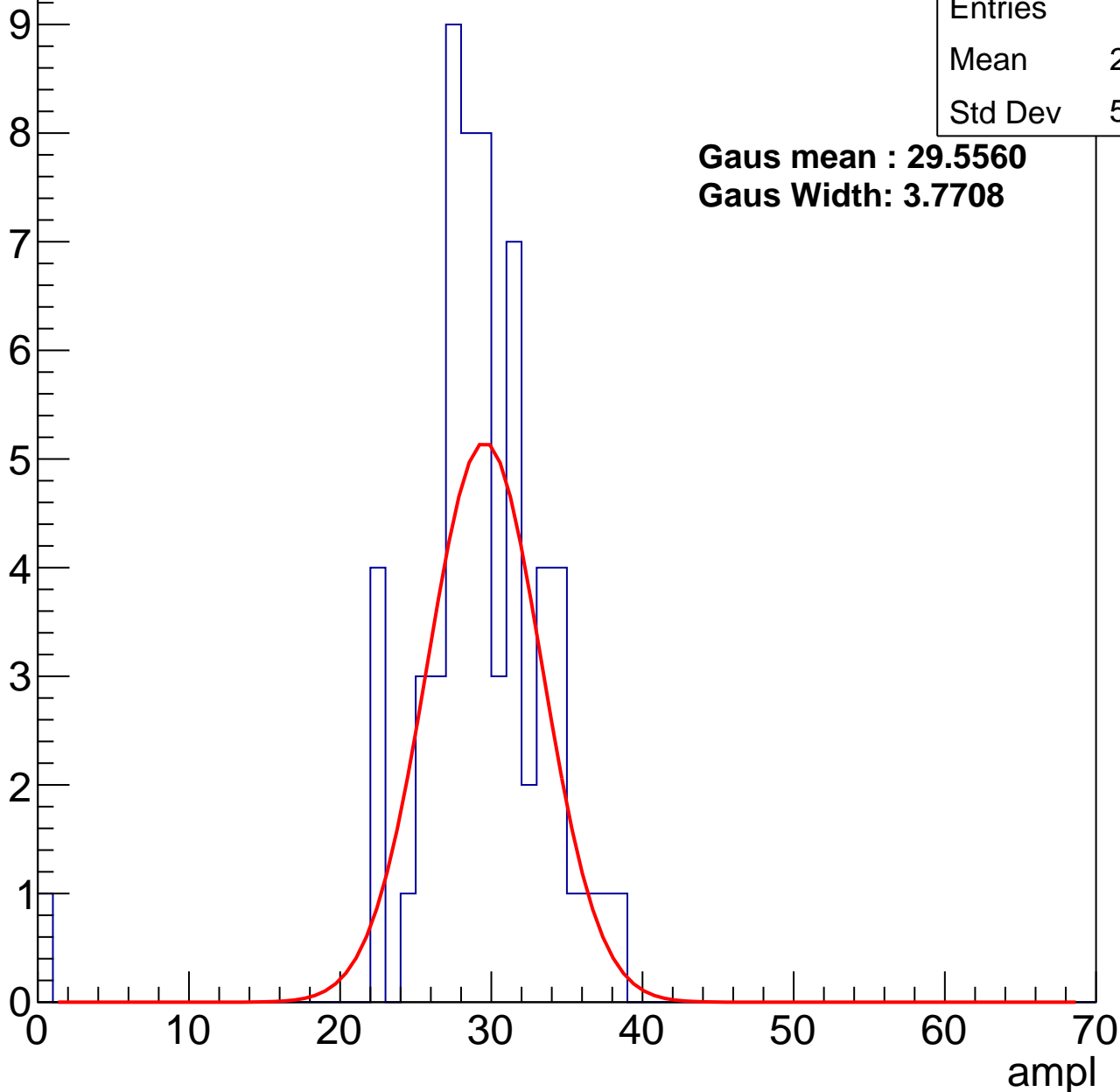
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	28.67
Std Dev	5.149

**Gaus mean : 29.5560**

**Gaus Width: 3.7708**



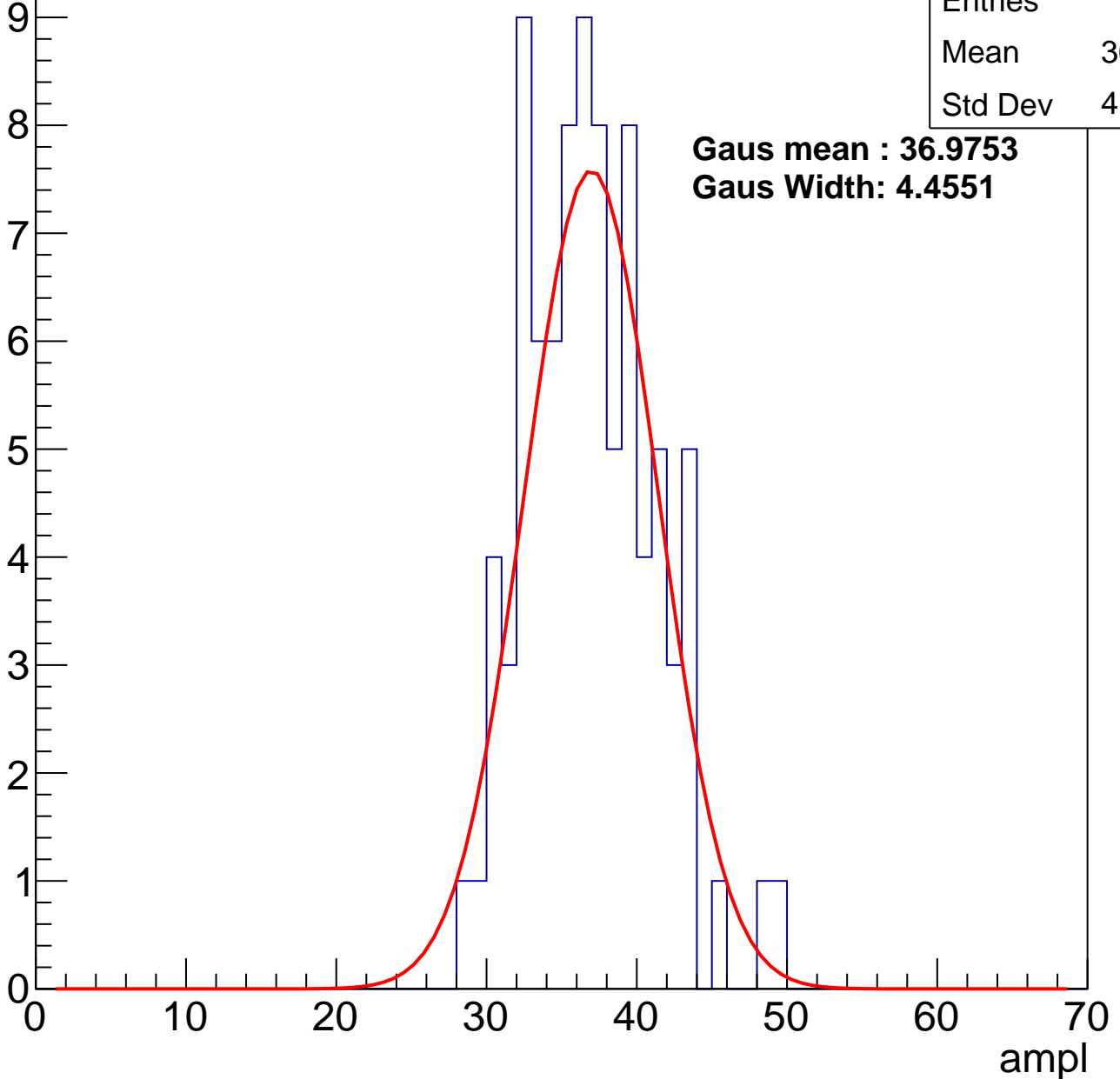
# B1L103S, U21-ch63, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	88
Mean	36.48
Std Dev	4.235

**Gaus mean : 36.9753**  
**Gaus Width: 4.4551**



# B1L103S, U21-ch63, adc2

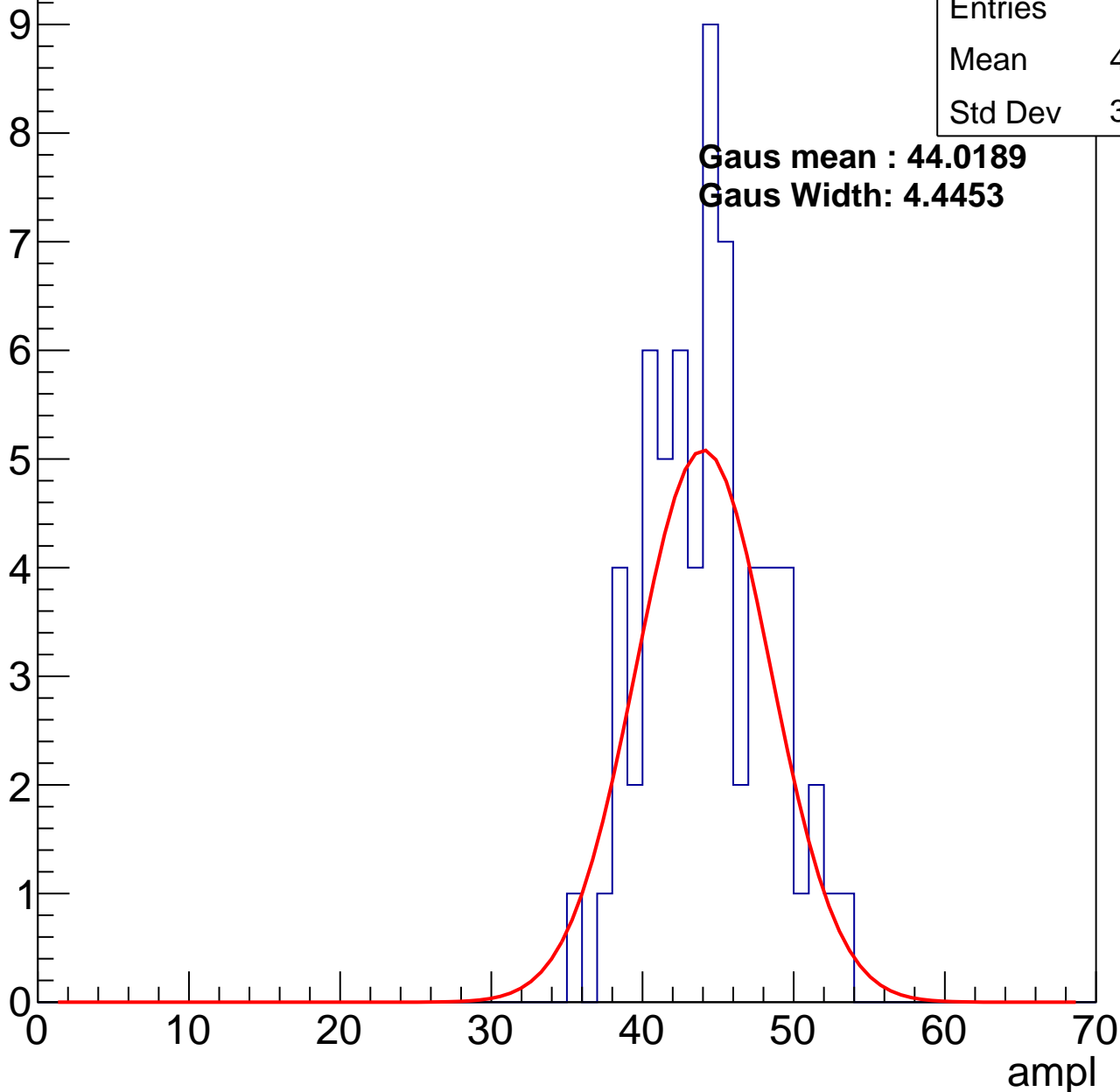
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	43.86
Std Dev	3.925

**Gaus mean : 44.0189**

**Gaus Width: 4.4453**

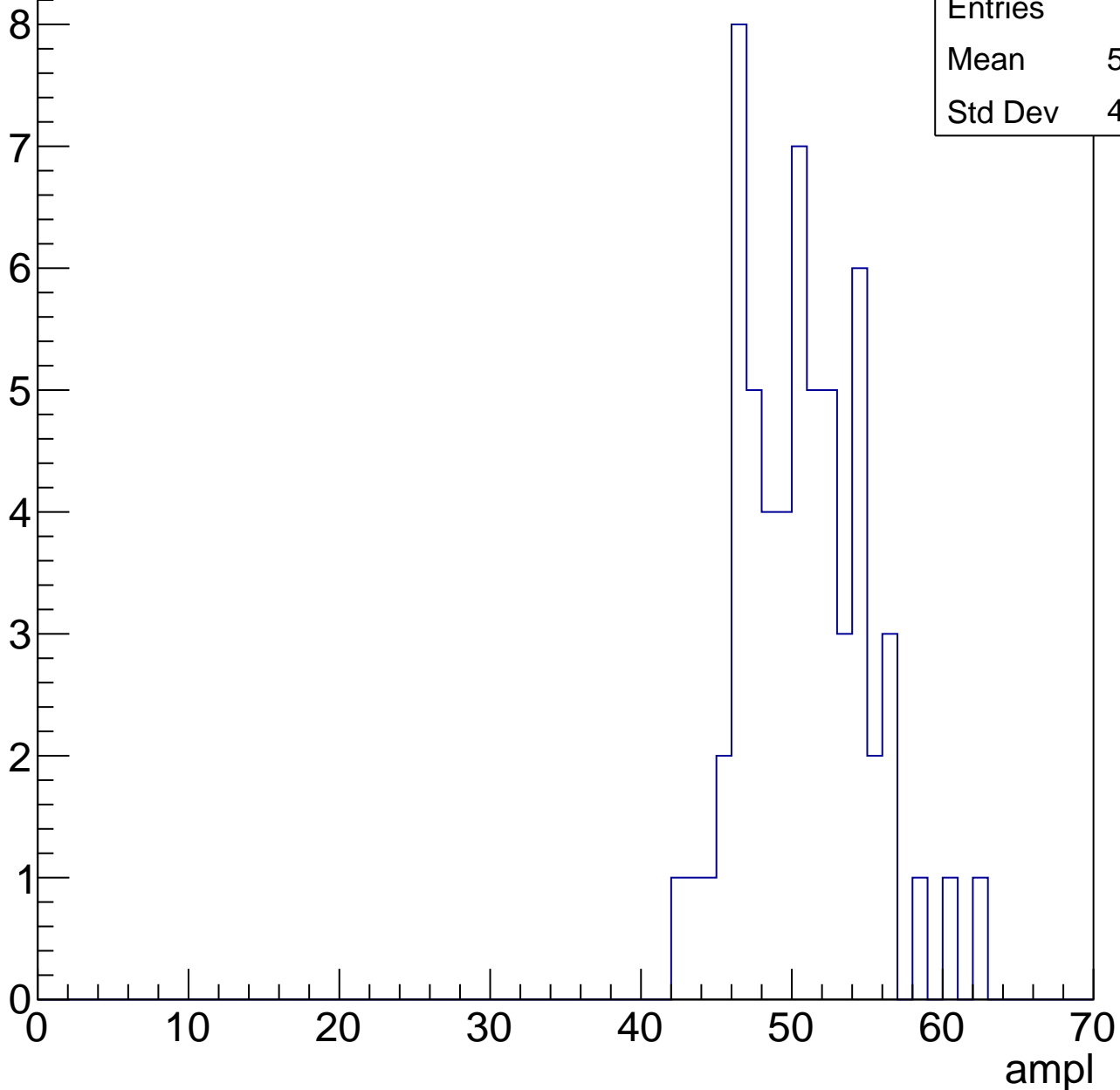


# B1L103S, U21-ch63, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	50.27
Std Dev	4.086

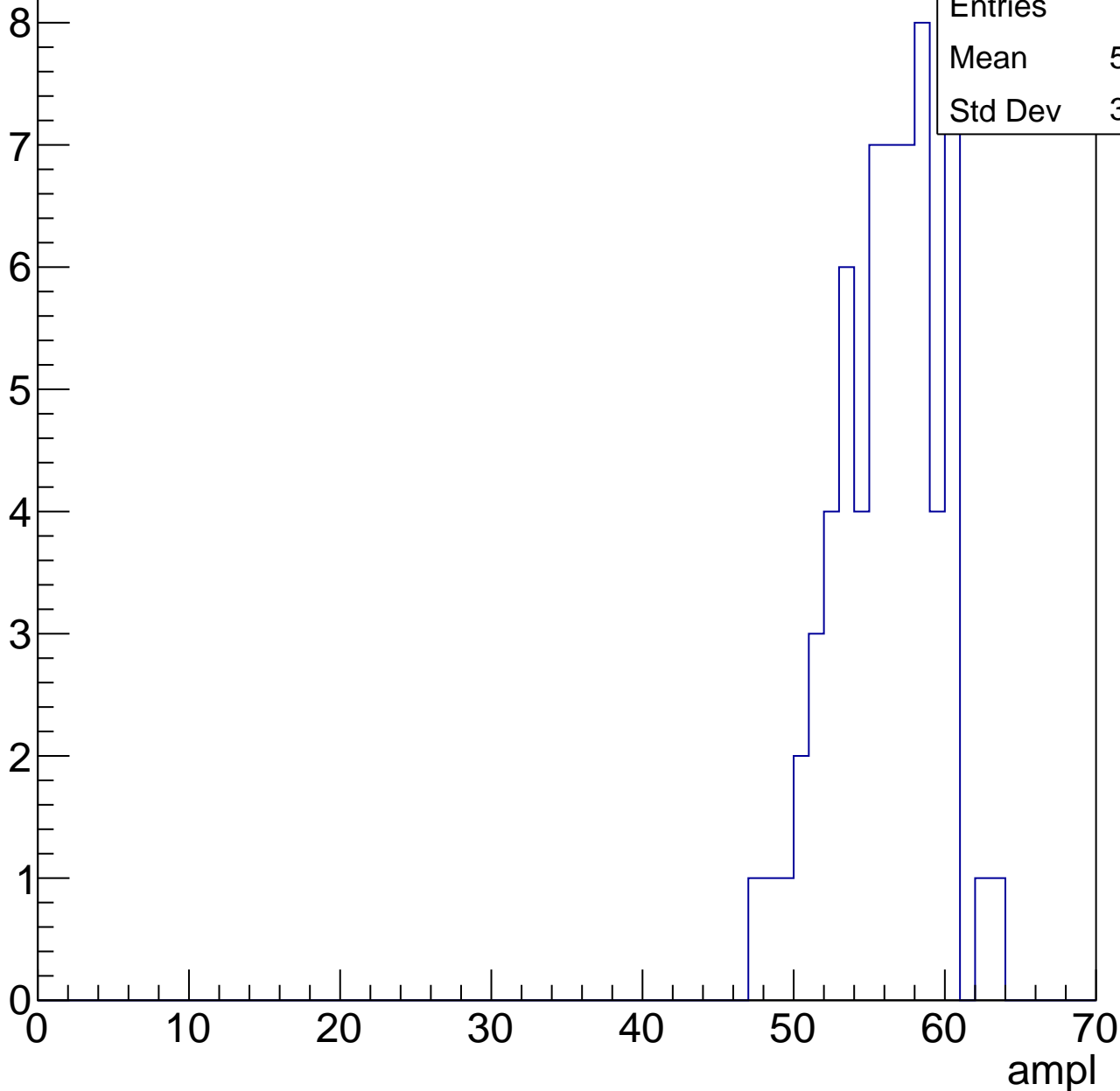


# B1L103S, U21-ch63, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	55.69
Std Dev	3.428



# B1L103S, U21-ch63, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

10

Entries 37

Mean 59

Std Dev 10.04

8

6

4

2

0

0

10

20

30

40

50

60

ampl

0

2

4

6

8

10

# B1L103S, U21-ch63, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

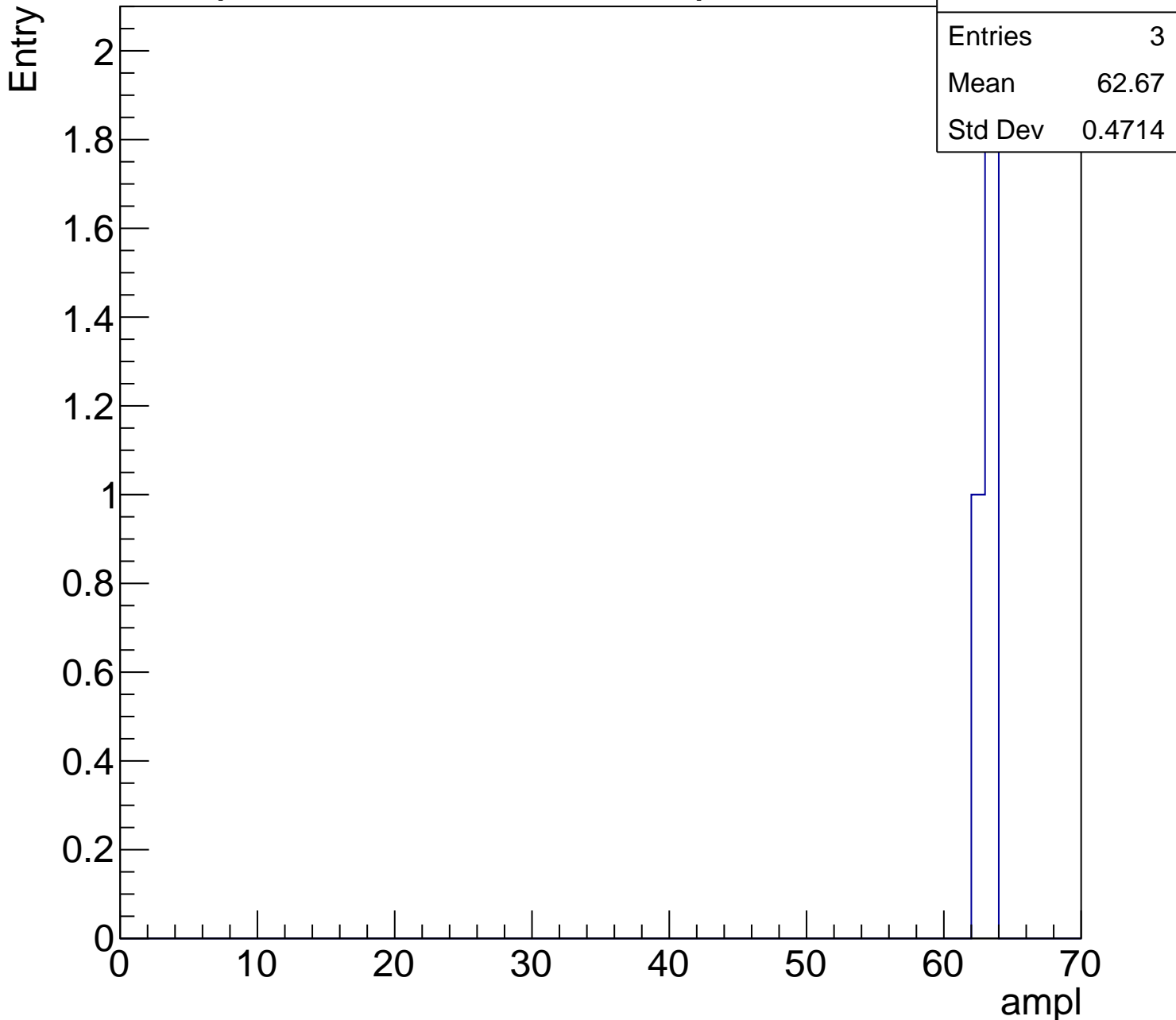
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.67
Std Dev	0.4714

0 10 20 30 40 50 60 70

ampl





# B1L103S, U21-ch63, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	10.5
Std Dev	10.5

# B1L103S, U21-ch64, adc0

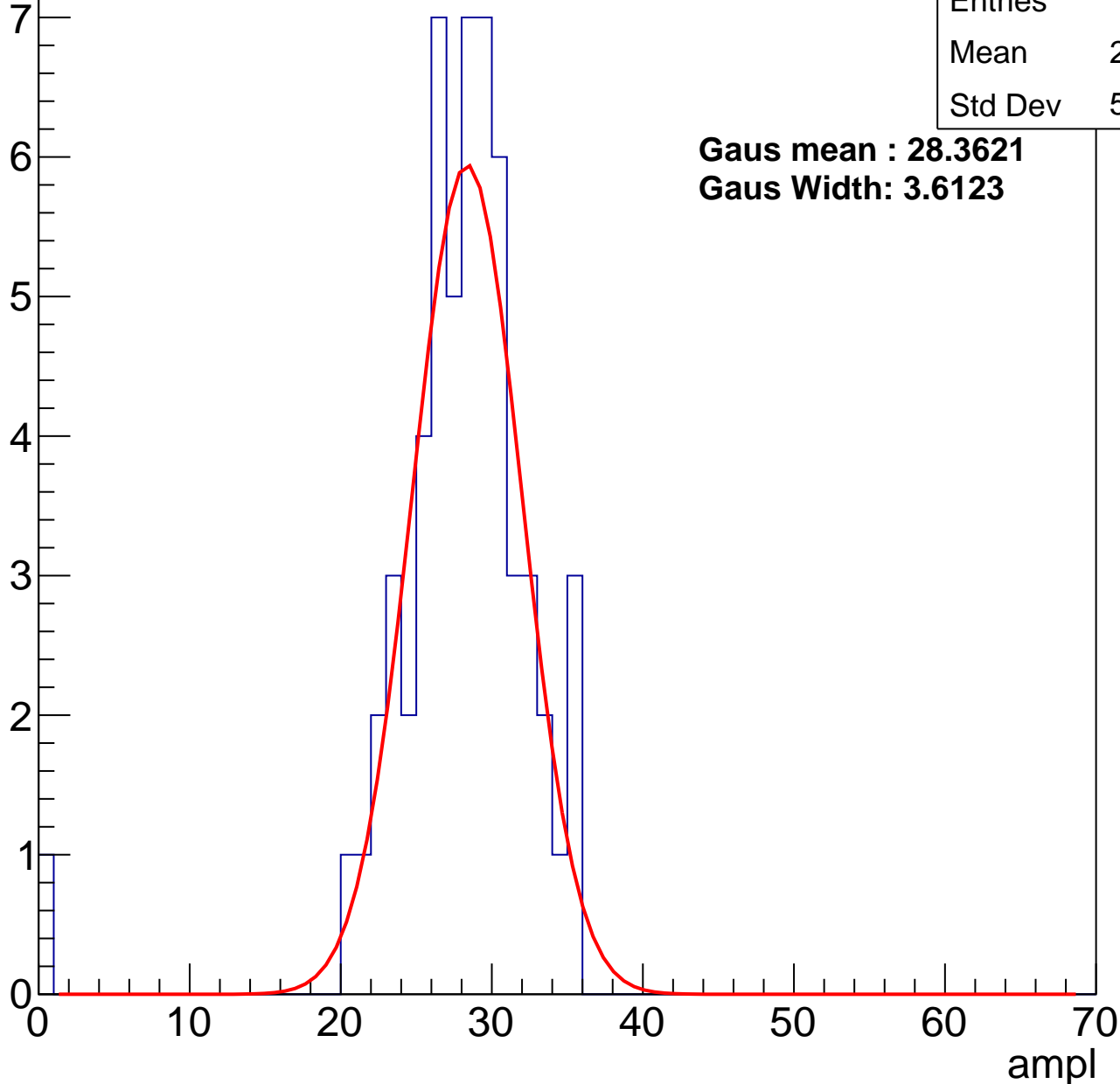
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	27.45
Std Dev	5.028

**Gaus mean : 28.3621**

**Gaus Width: 3.6123**



# B1L103S, U21-ch64, adc1

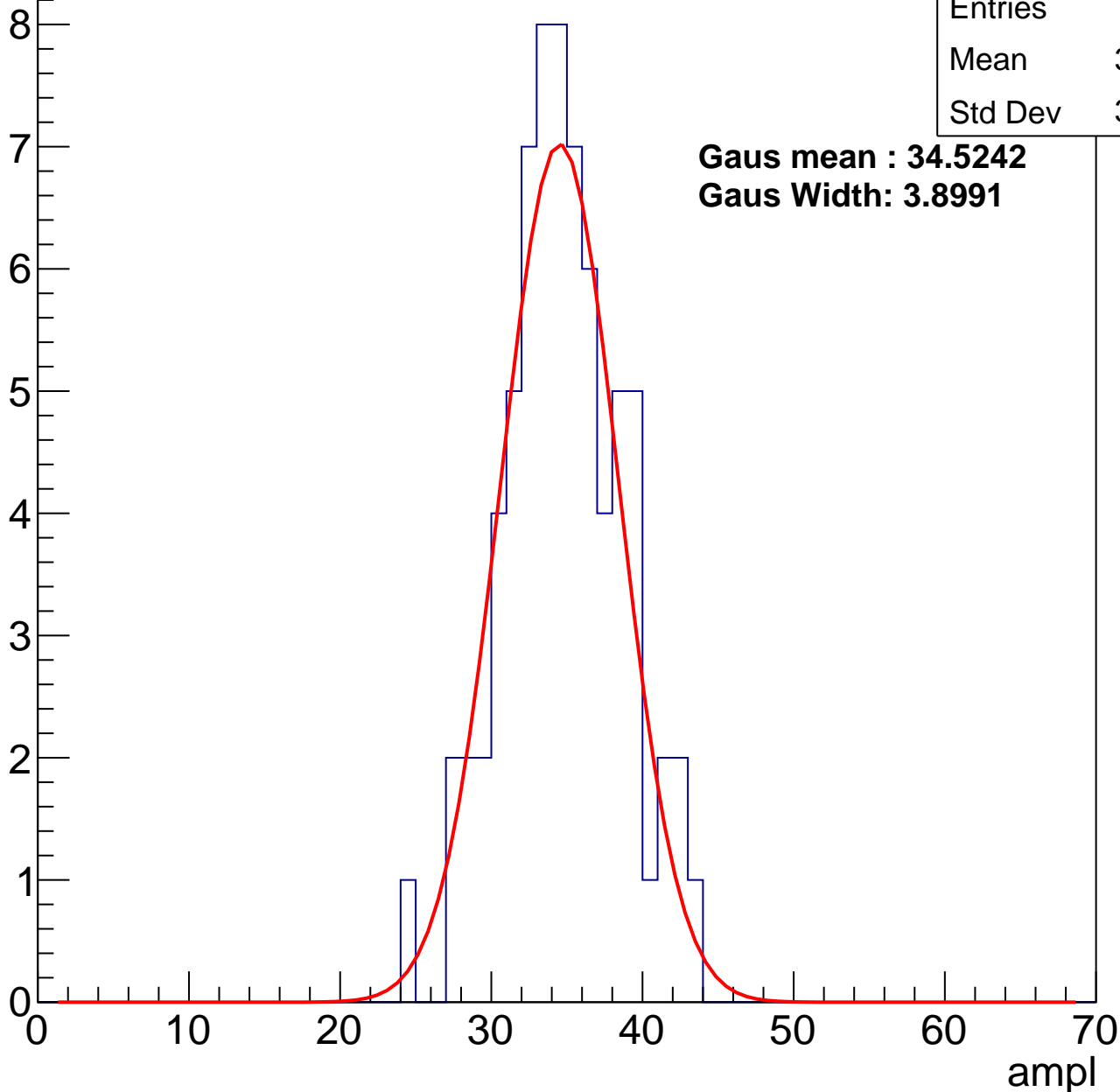
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	34.31
Std Dev	3.861

**Gaus mean : 34.5242**

**Gaus Width: 3.8991**



# B1L103S, U21-ch64, adc2

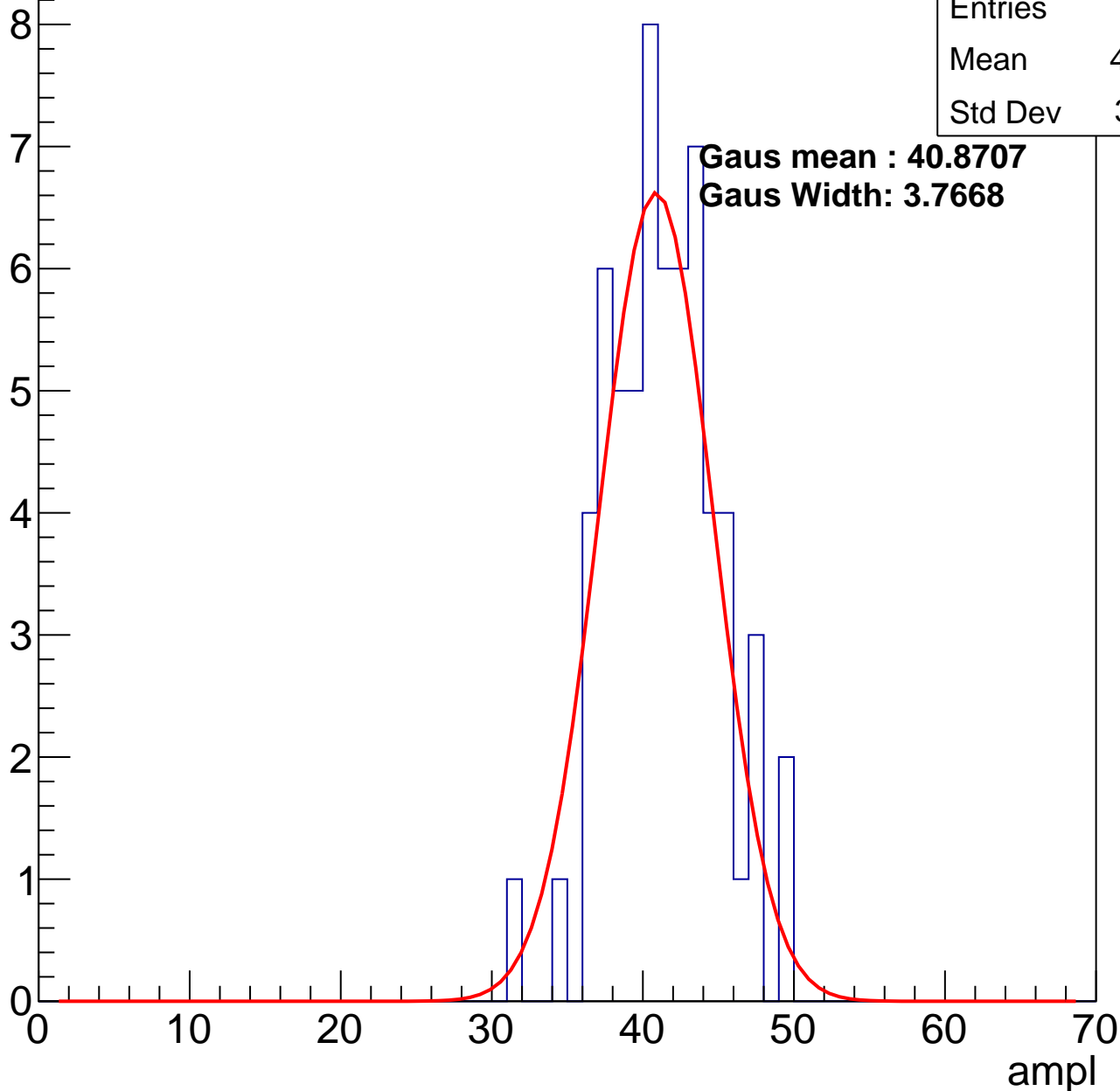
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	40.89
Std Dev	3.591

**Gaus mean : 40.8707**

**Gaus Width: 3.7668**

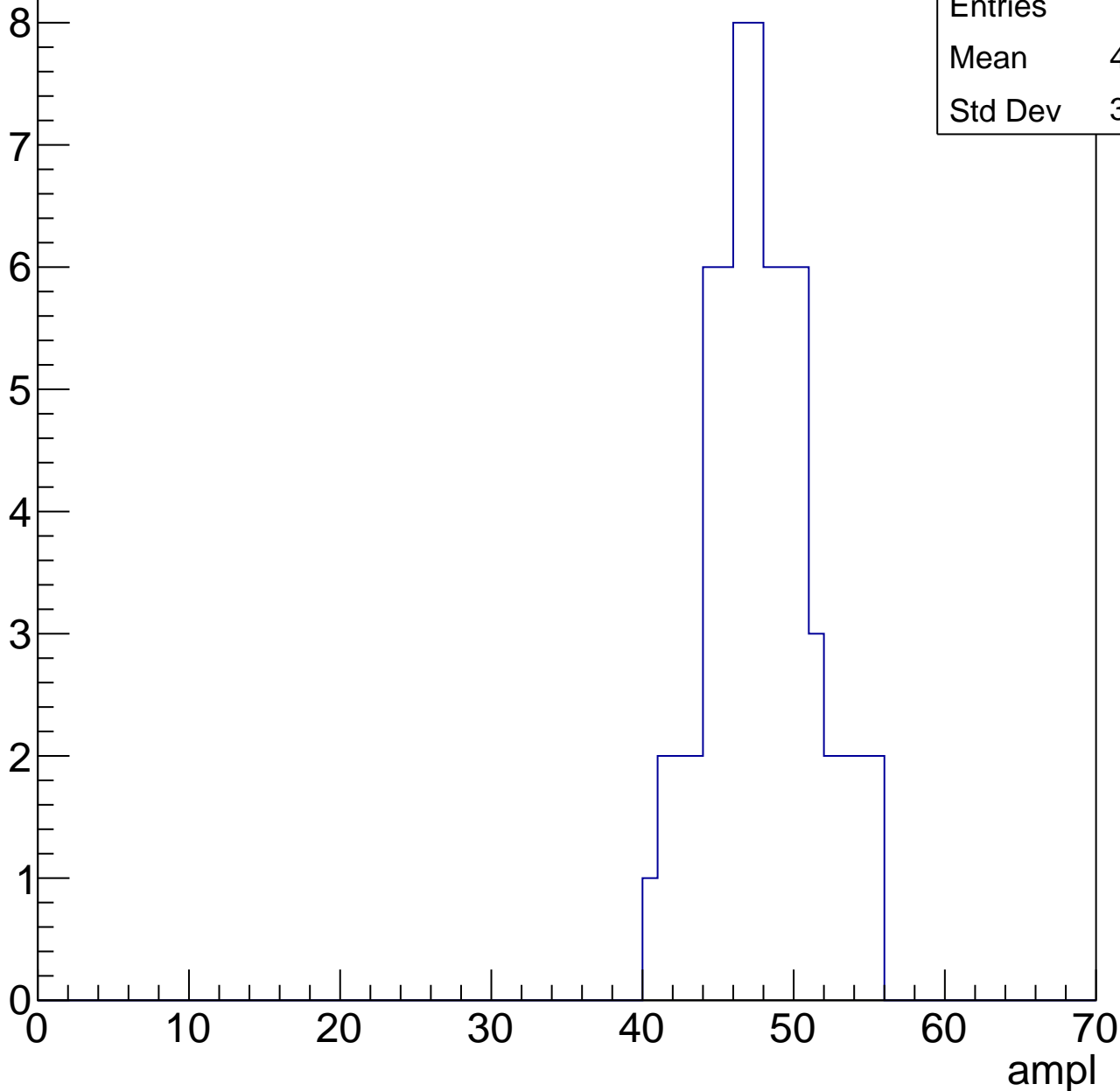


# B1L103S, U21-ch64, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	47.39
Std Dev	3.444

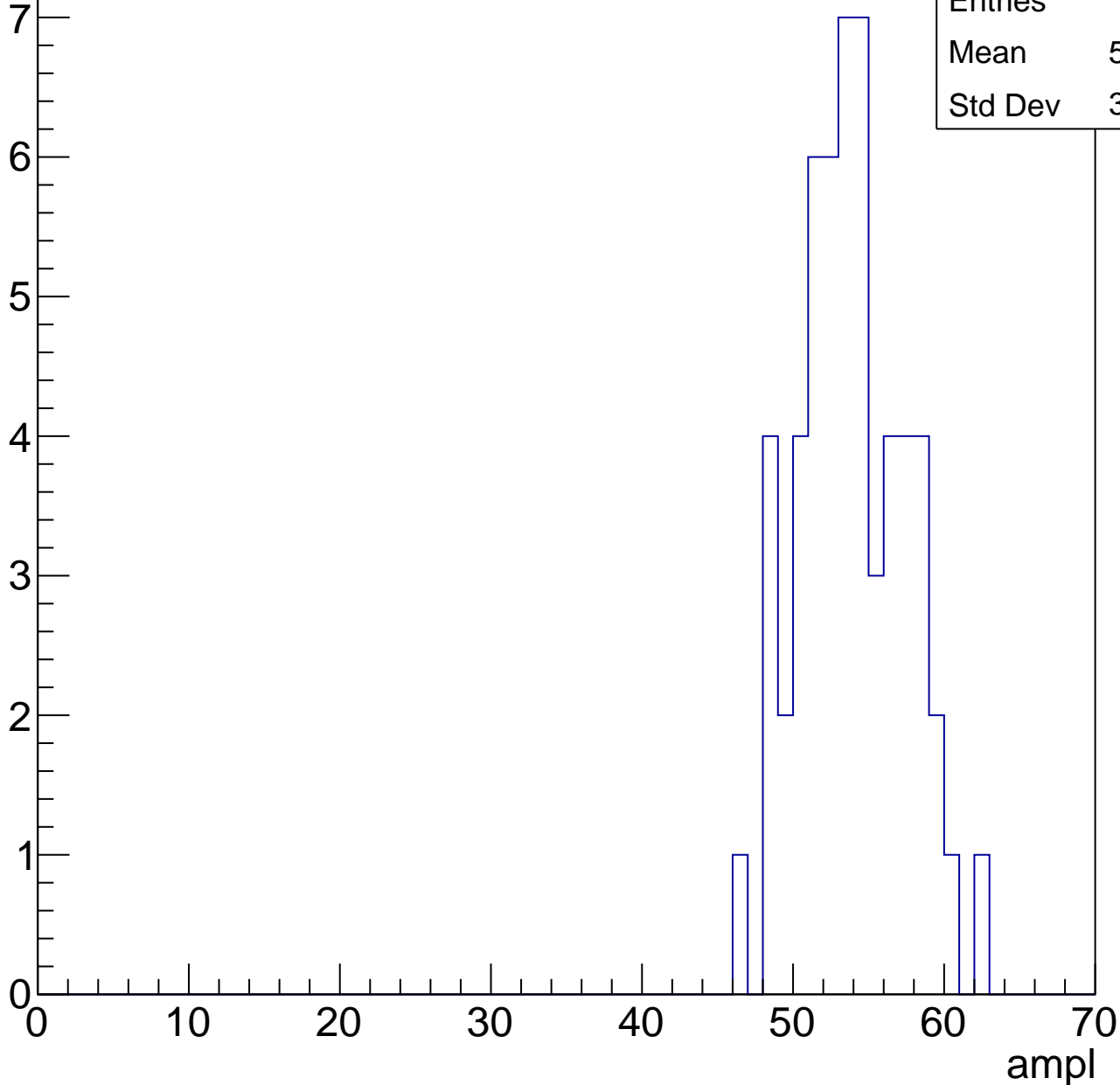


# B1L103S, U21-ch64, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	53.43
Std Dev	3.427

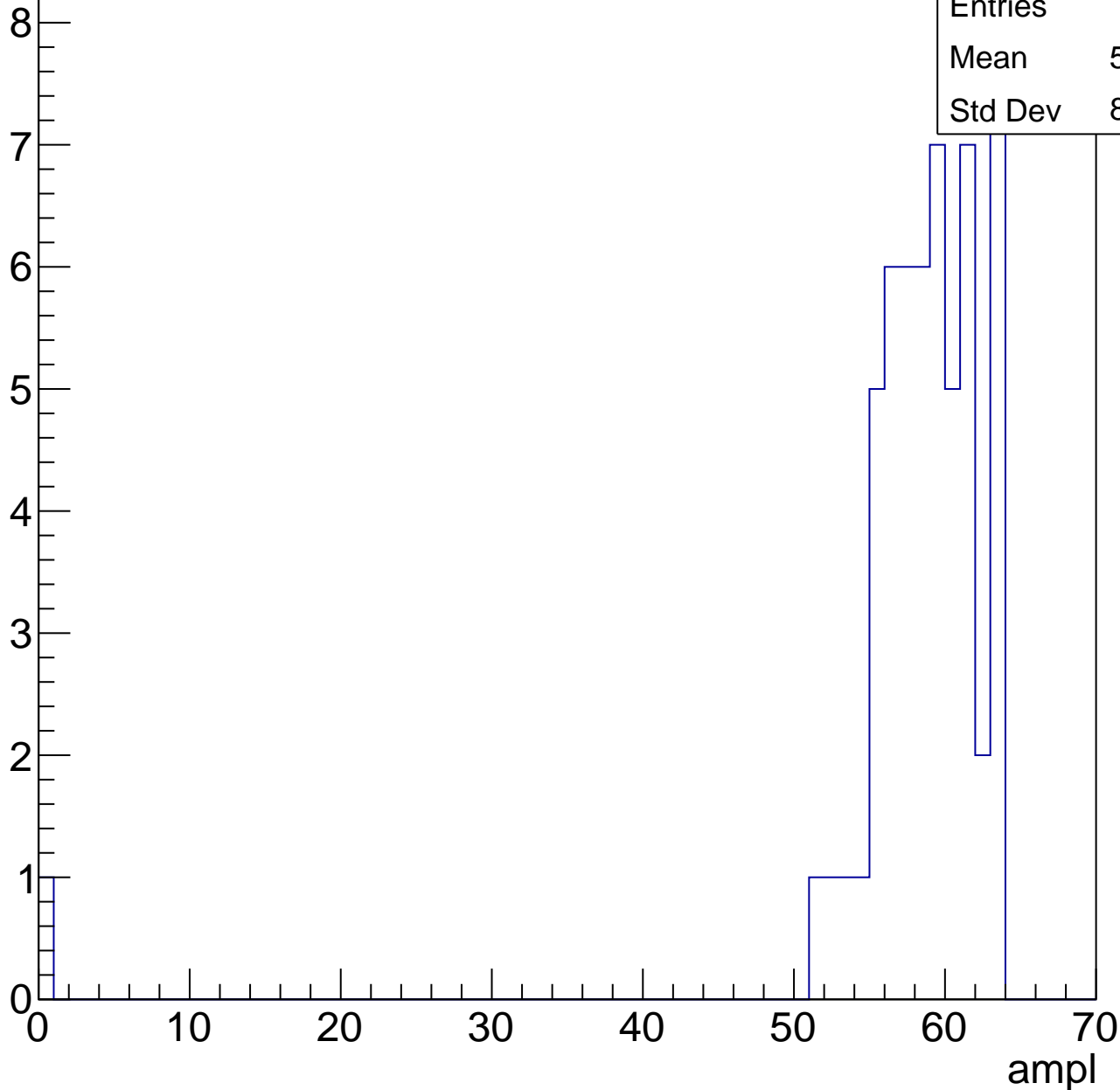


# B1L103S, U21-ch64, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	57.53
Std Dev	8.244

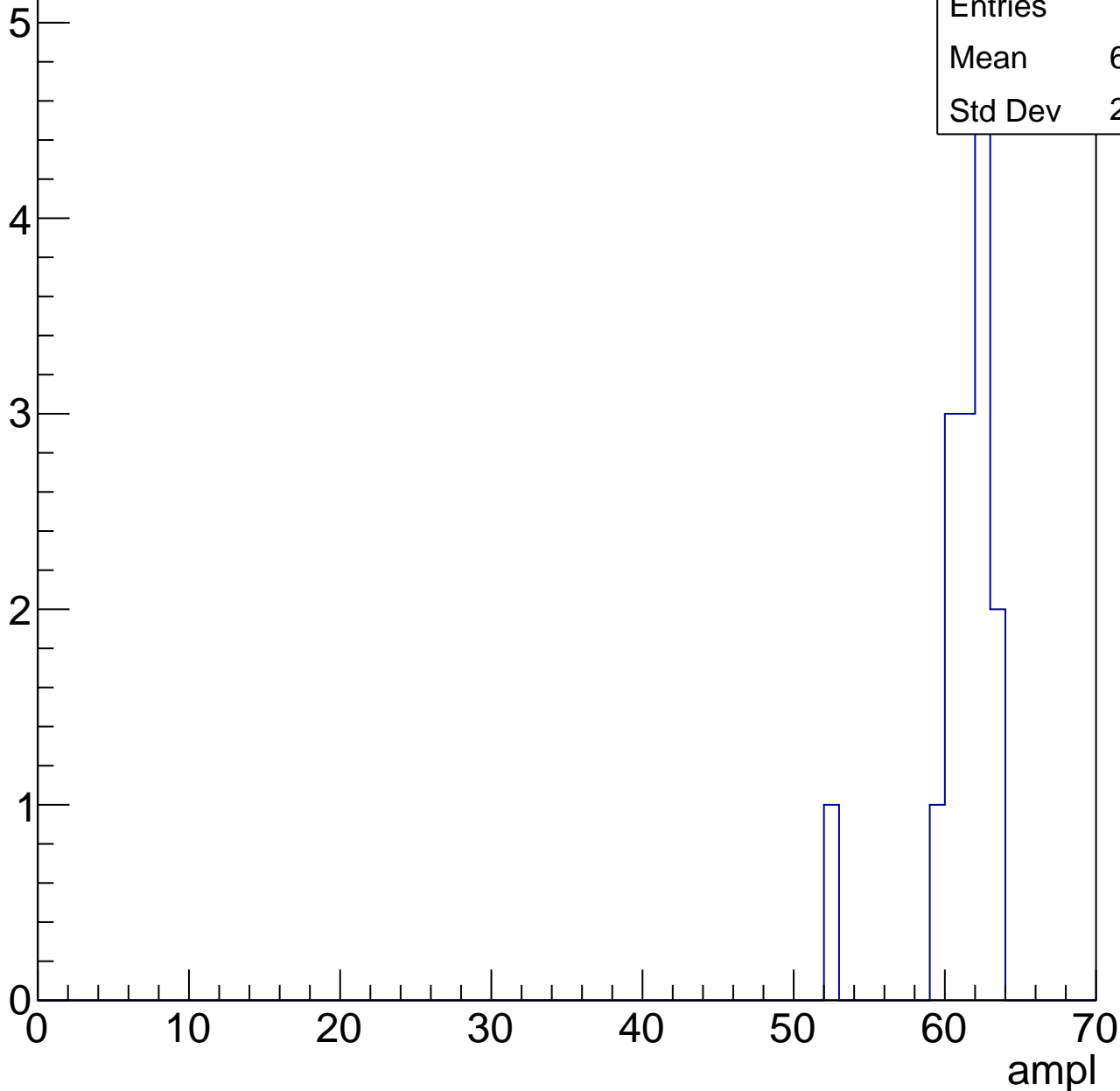


# B1L103S, U21-ch64, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	15
Mean	60.67
Std Dev	2.573

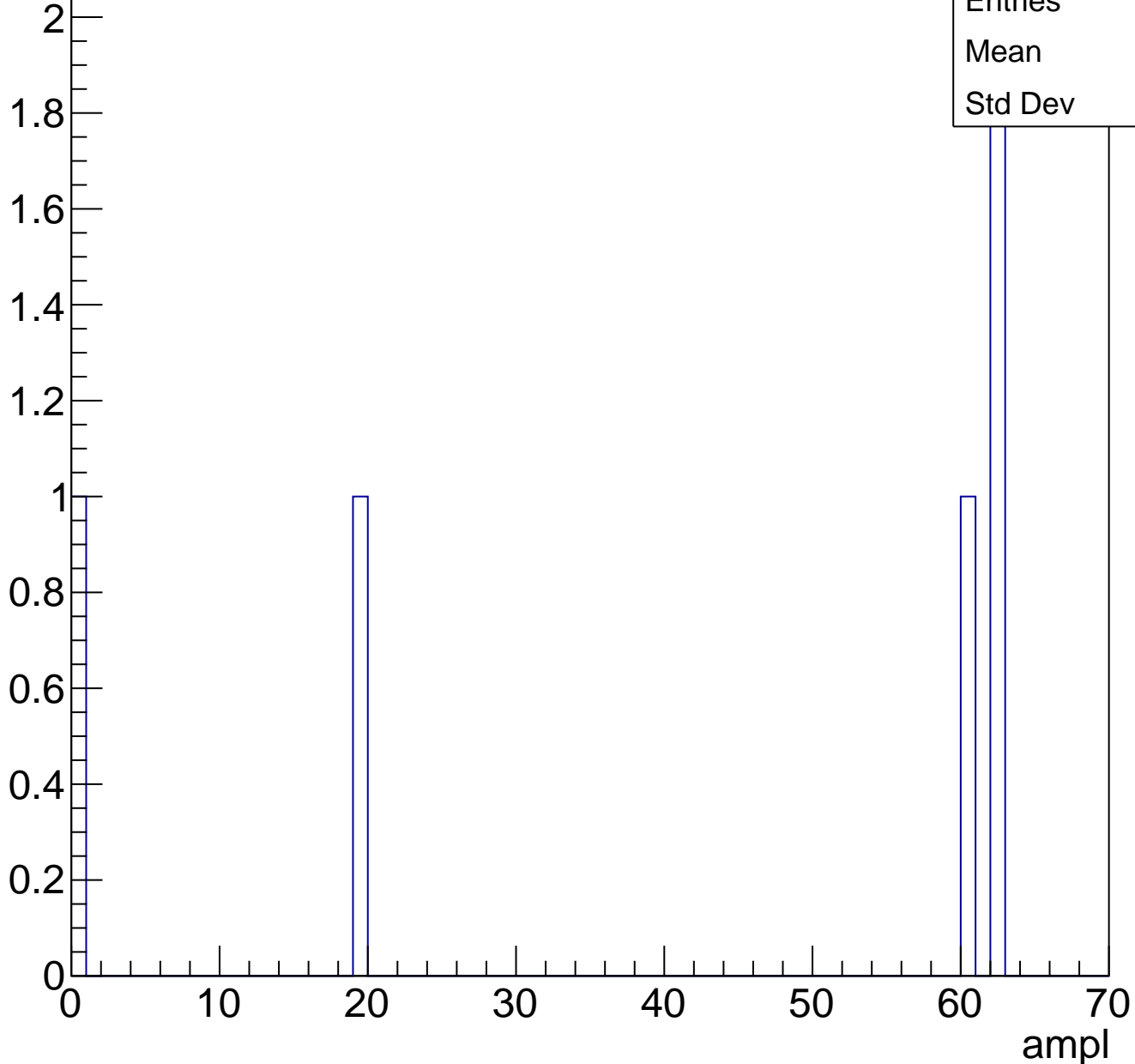




# B1L103S, U21-ch64, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	5
Mean	40.6
Std Dev	26.1

# B1L103S, U21-ch65, adc0

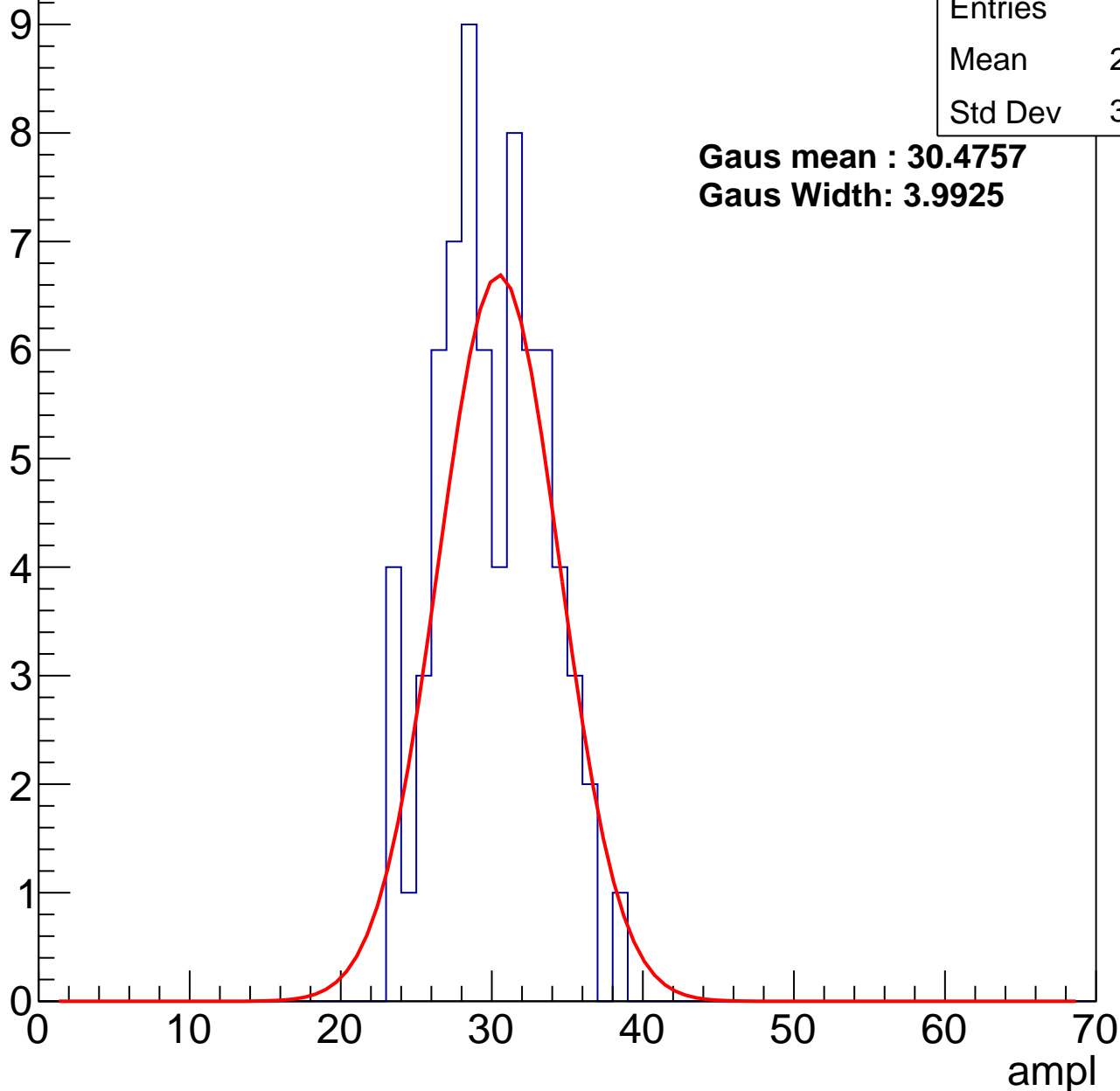
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	29.59
Std Dev	3.499

**Gaus mean : 30.4757**

**Gaus Width: 3.9925**



# B1L103S, U21-ch65, adc1

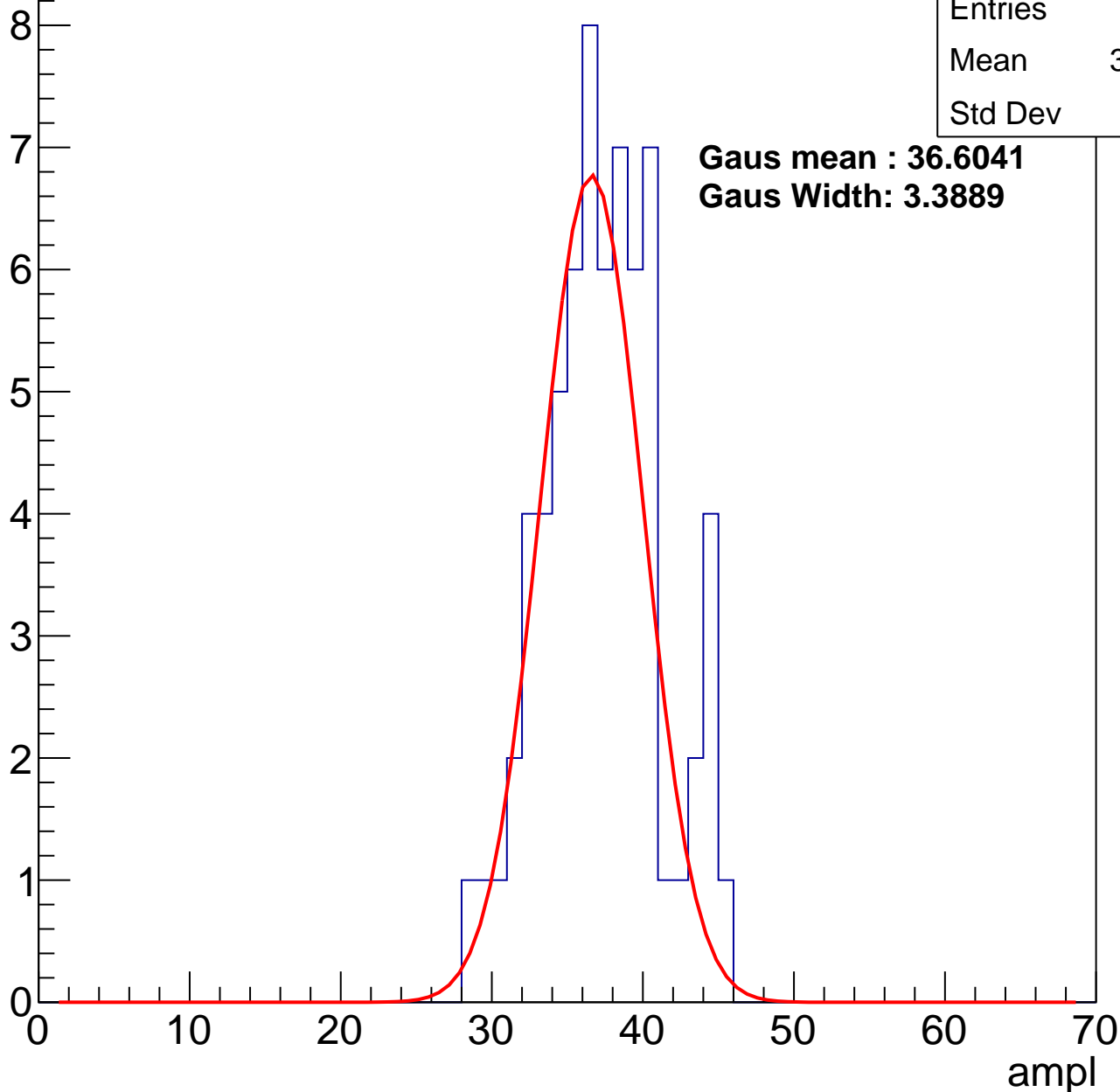
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	36.85
Std Dev	3.81

**Gaus mean : 36.6041**

**Gaus Width: 3.3889**



# B1L103S, U21-ch65, adc2

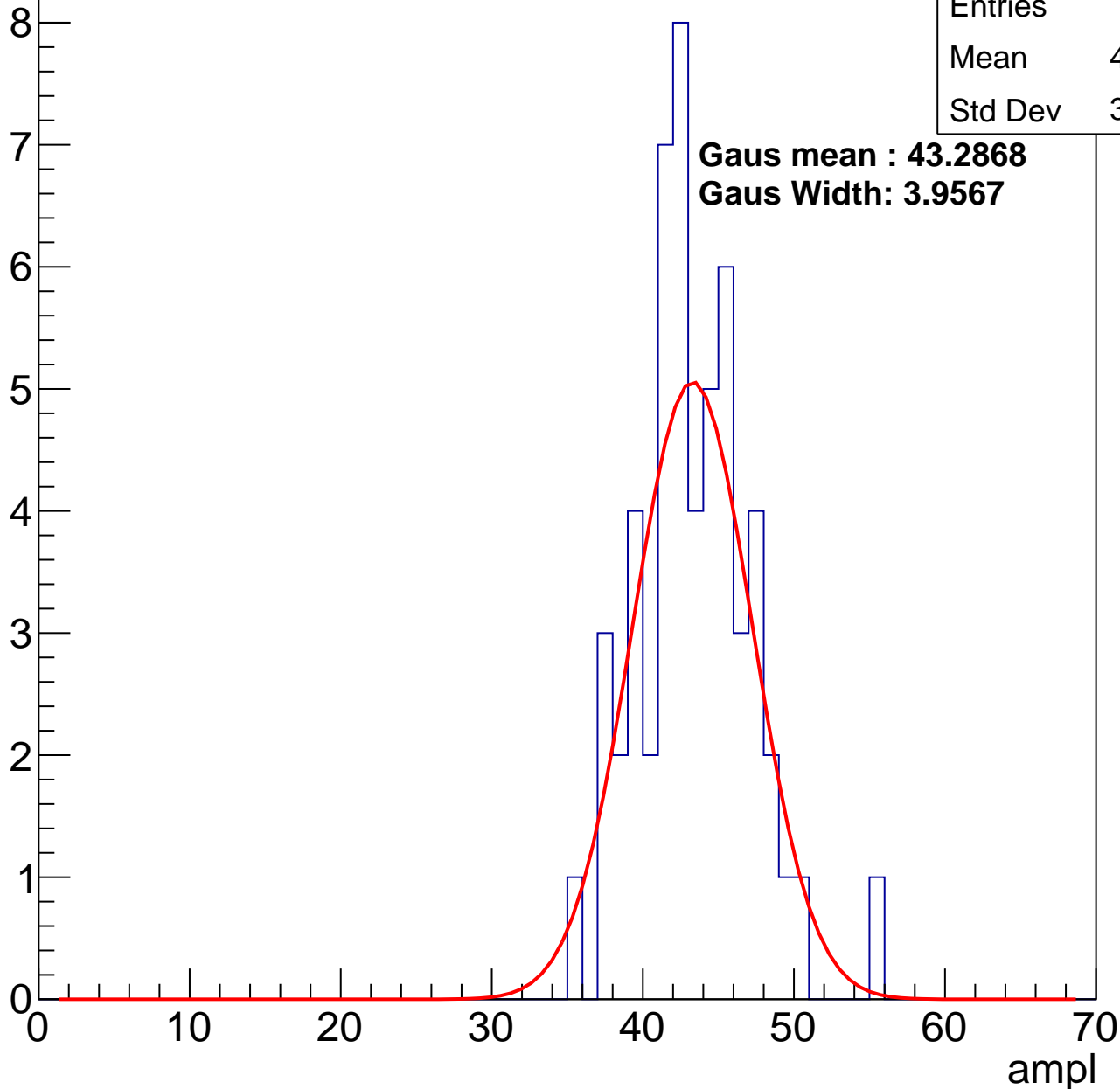
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	42.94
Std Dev	3.699

**Gaus mean : 43.2868**

**Gaus Width: 3.9567**

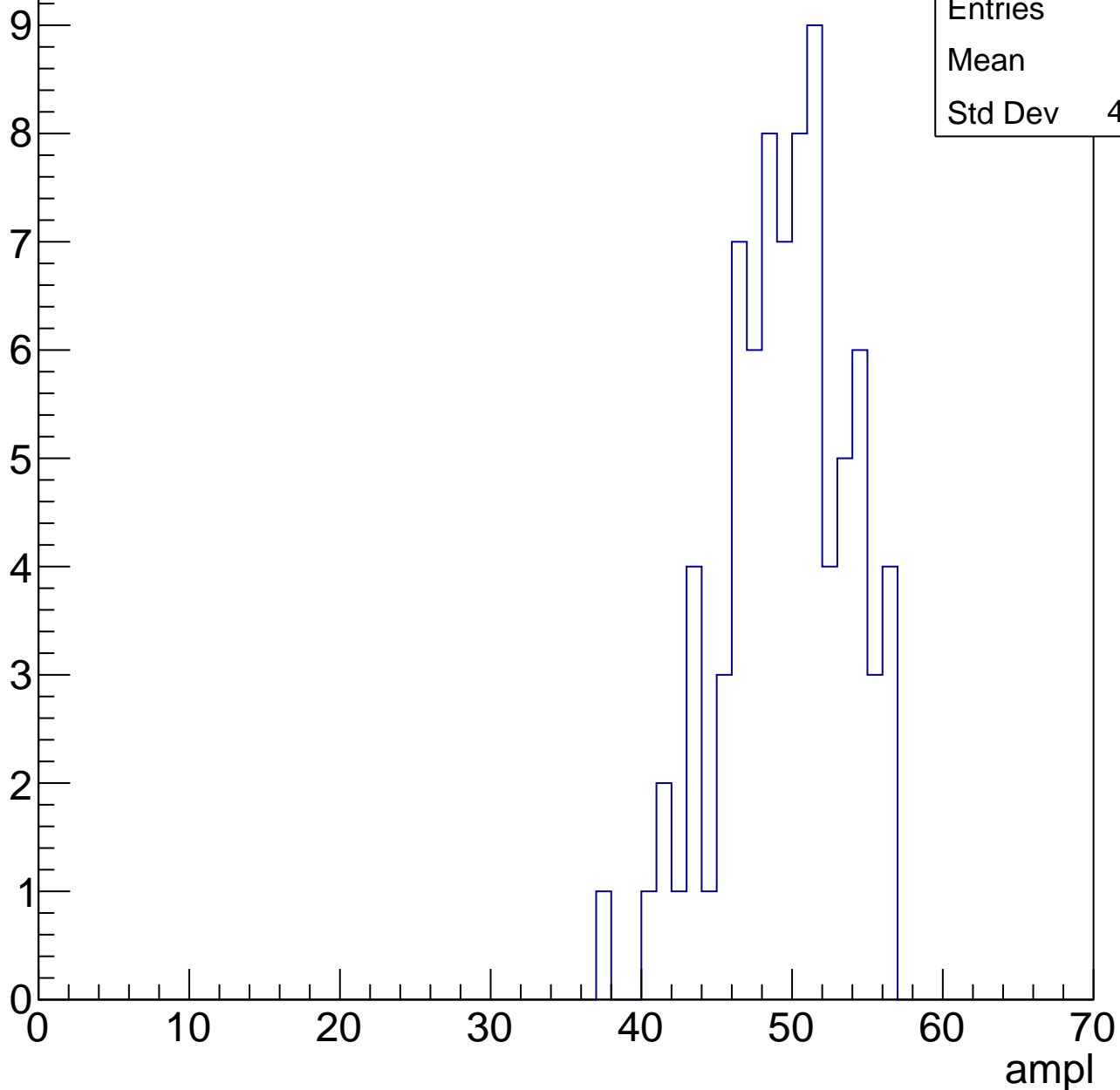


# B1L103S, U21-ch65, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	80
Mean	49.1
Std Dev	4.073

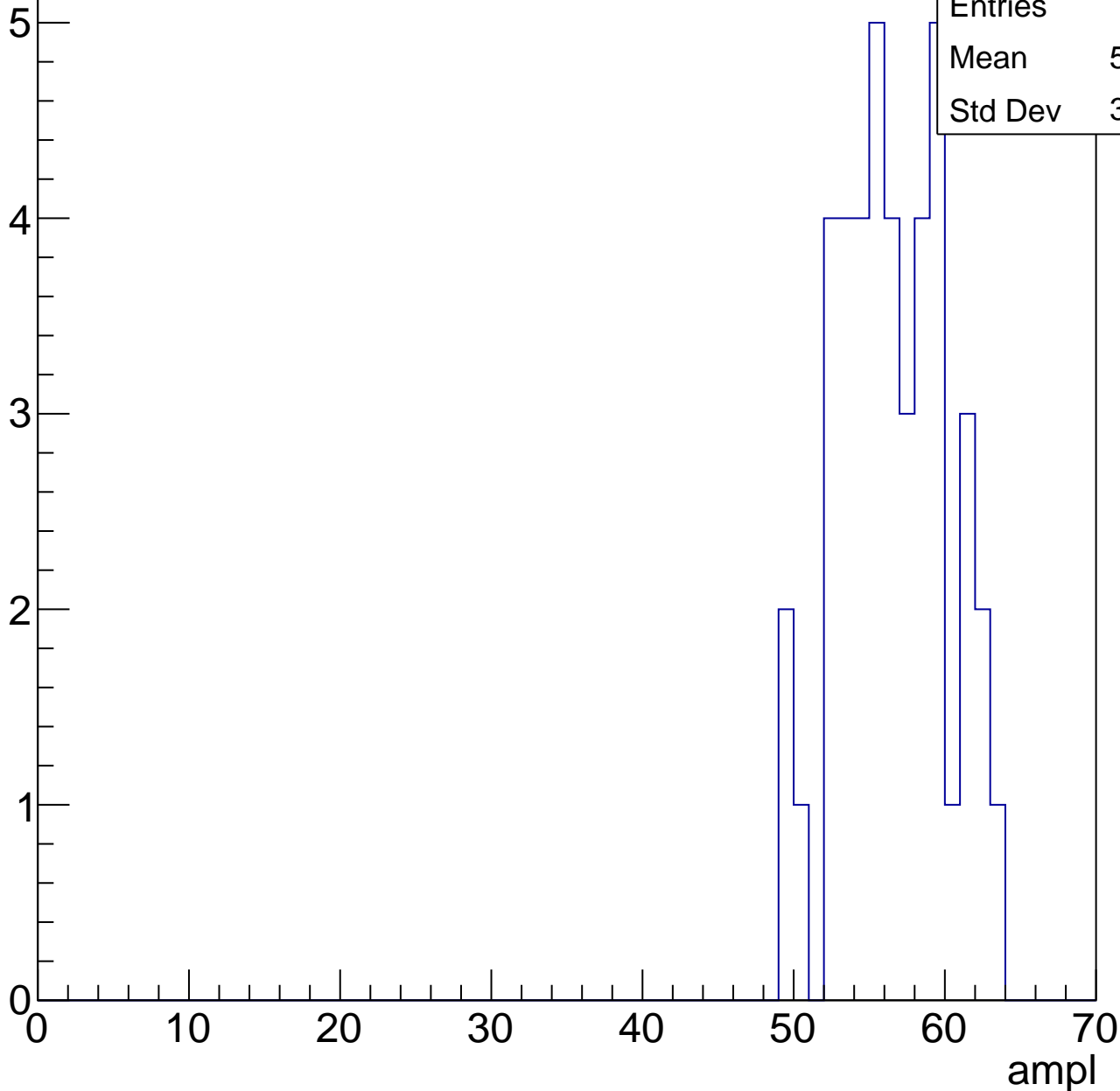


# B1L103S, U21-ch65, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

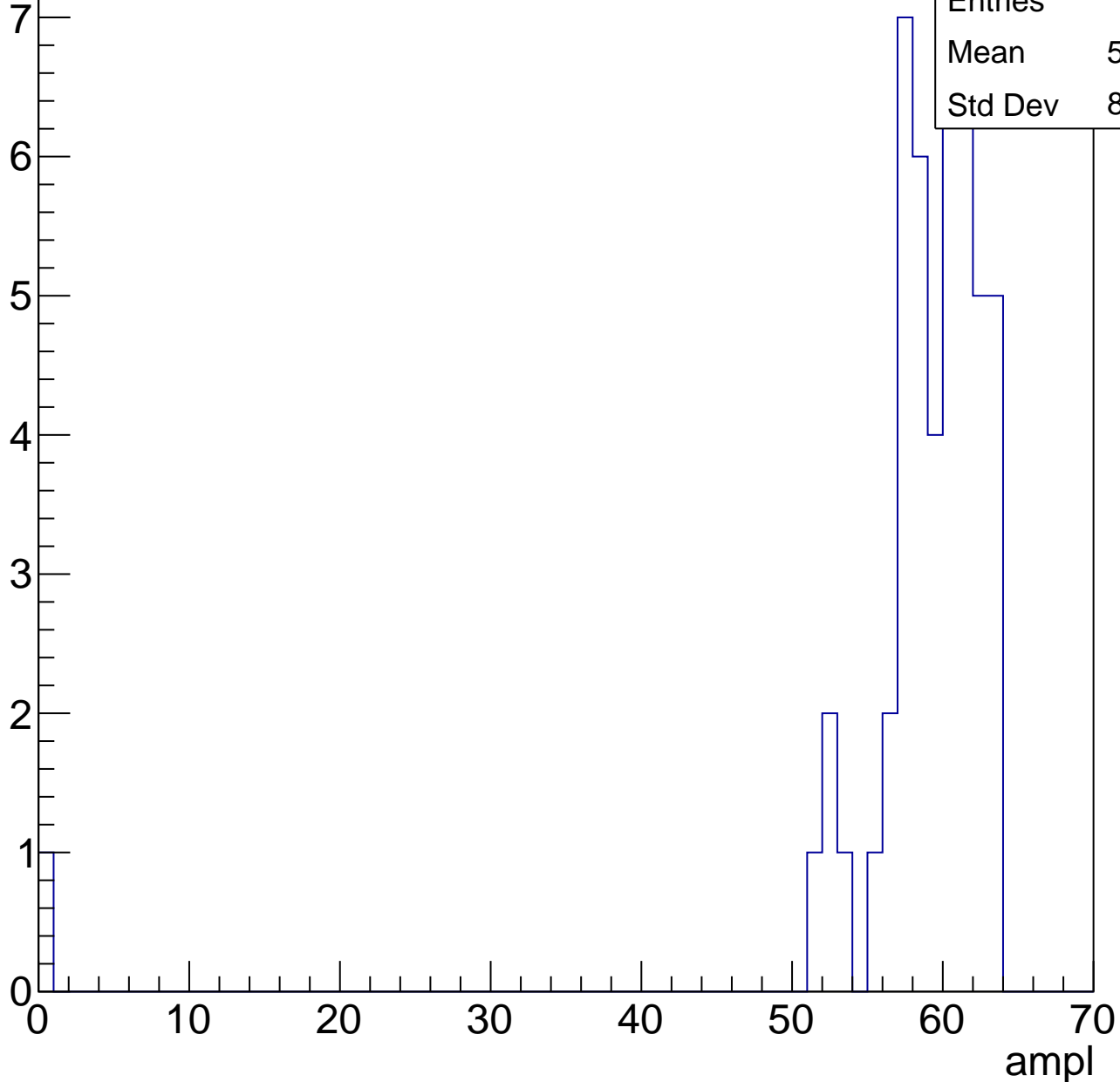
Entries	43
Mean	56.07
Std Dev	3.513



# B1L103S, U21-ch65, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

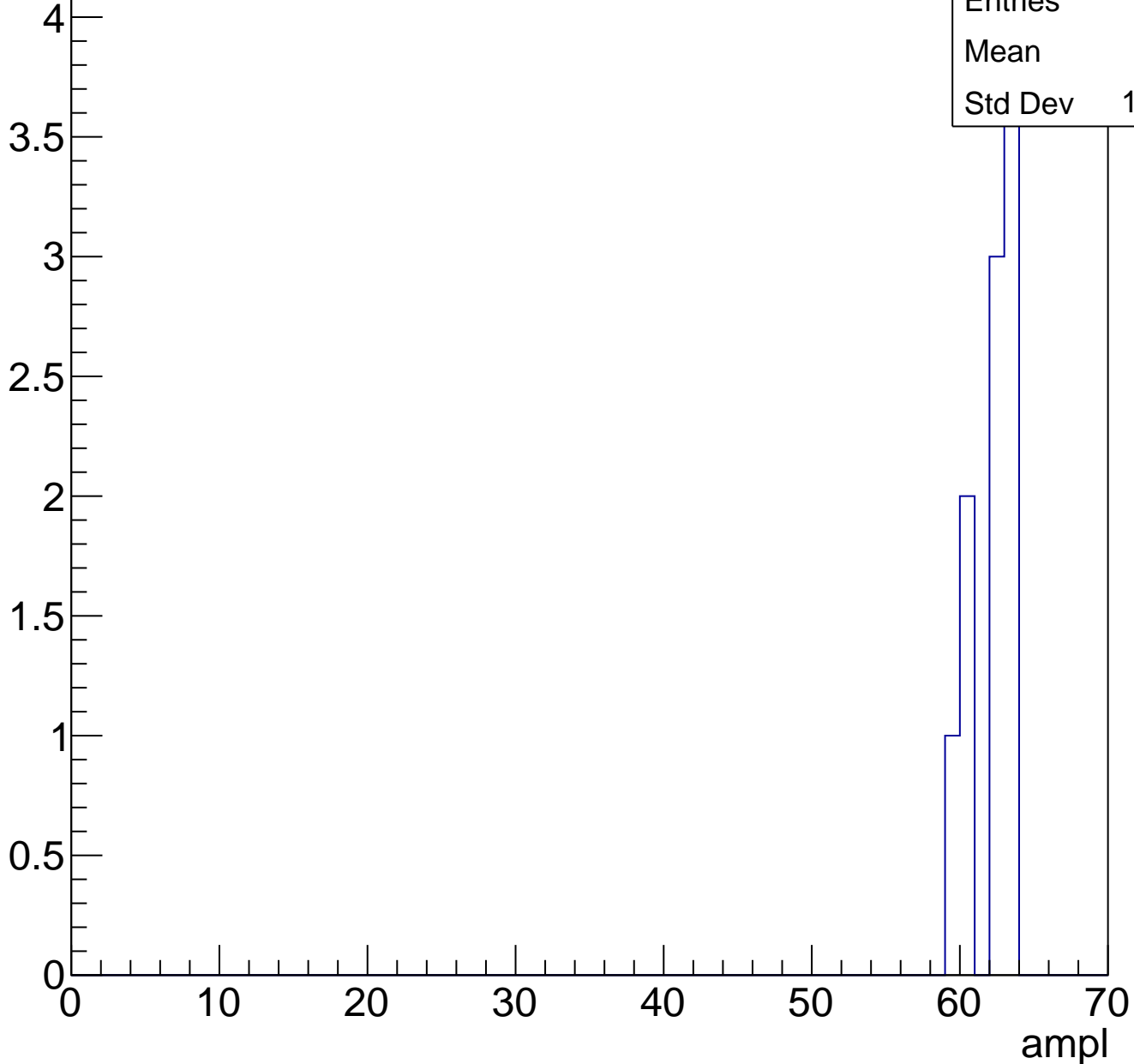
Entry



# B1L103S, U21-ch65, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U21-ch65, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U21-ch66, adc0

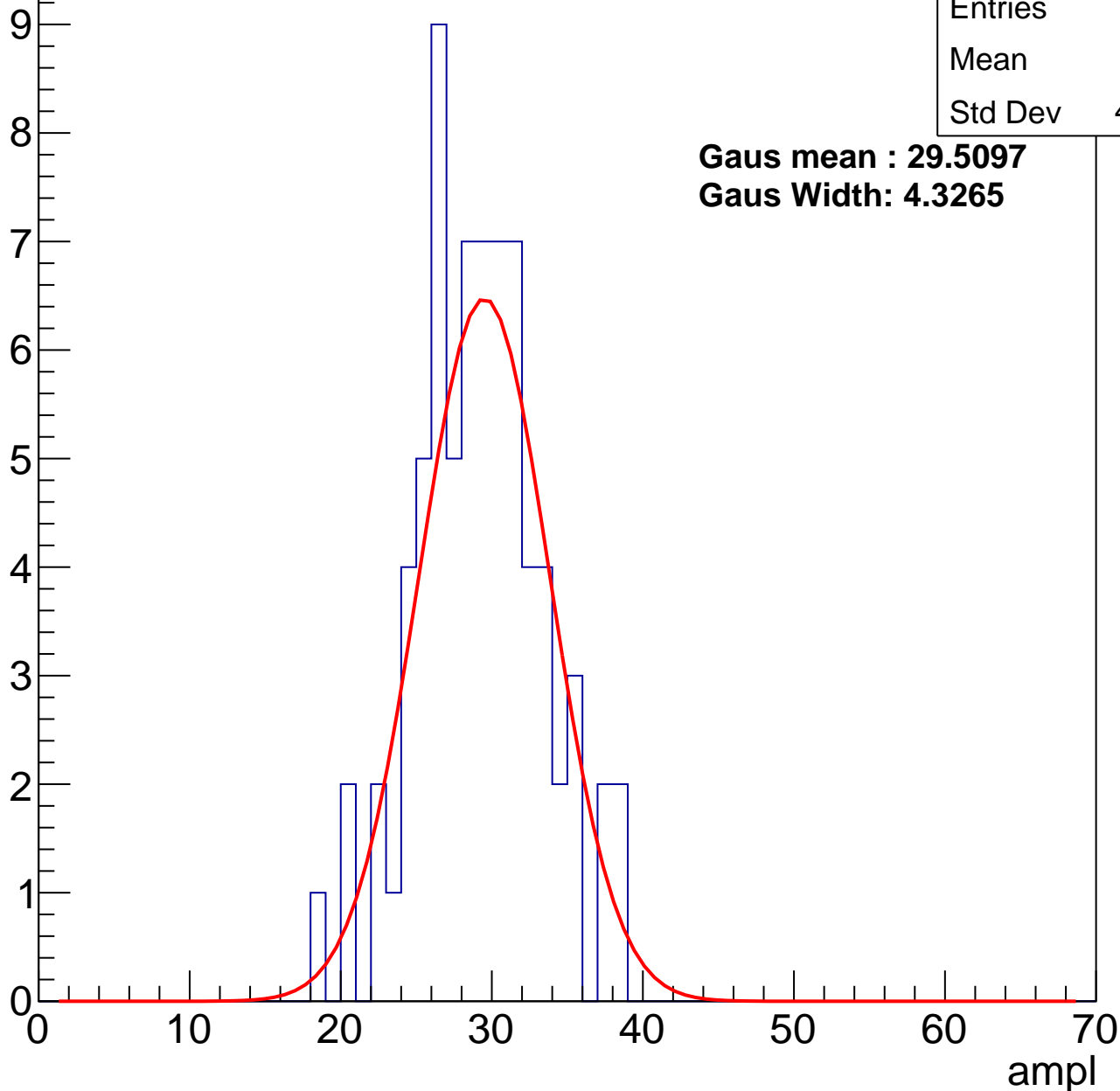
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	28.7
Std Dev	4.161

**Gaus mean : 29.5097**

**Gaus Width: 4.3265**



# B1L103S, U21-ch66, adc1

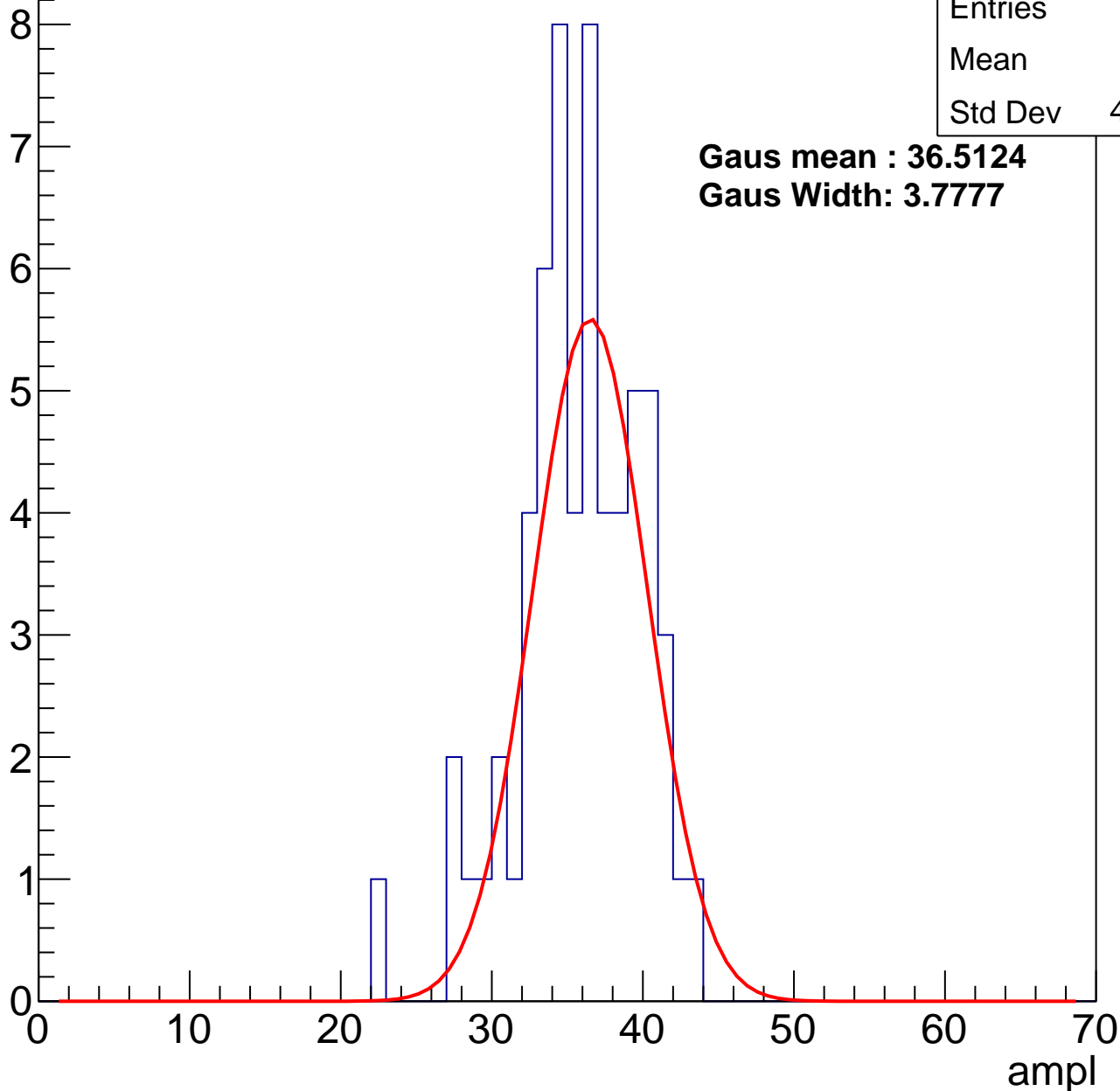
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	35.3
Std Dev	4.042

**Gaus mean : 36.5124**

**Gaus Width: 3.7777**



# B1L103S, U21-ch66, adc2

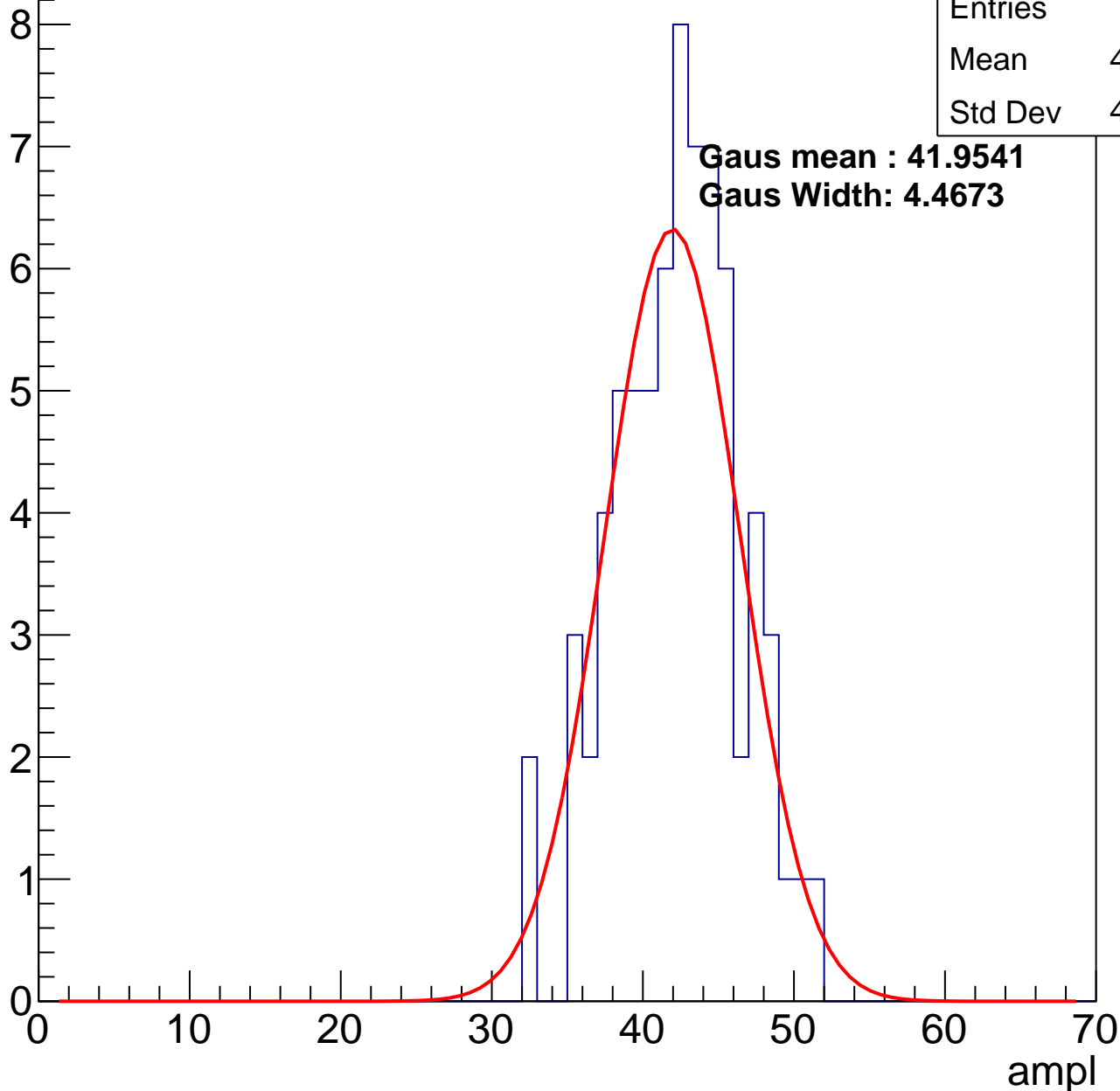
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	41.79
Std Dev	4.065

**Gaus mean : 41.9541**

**Gaus Width: 4.4673**

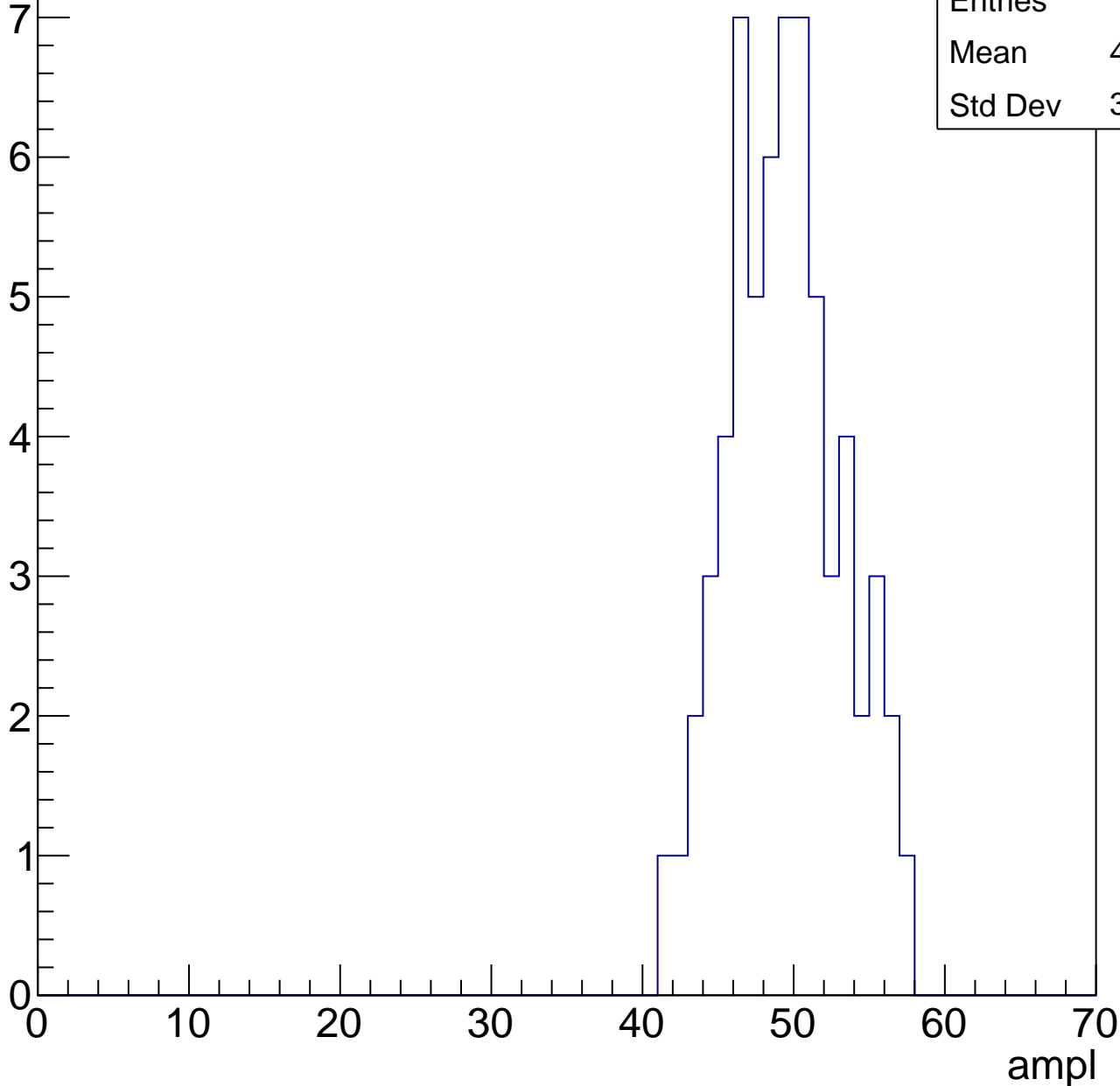


# B1L103S, U21-ch66, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	48.95
Std Dev	3.675

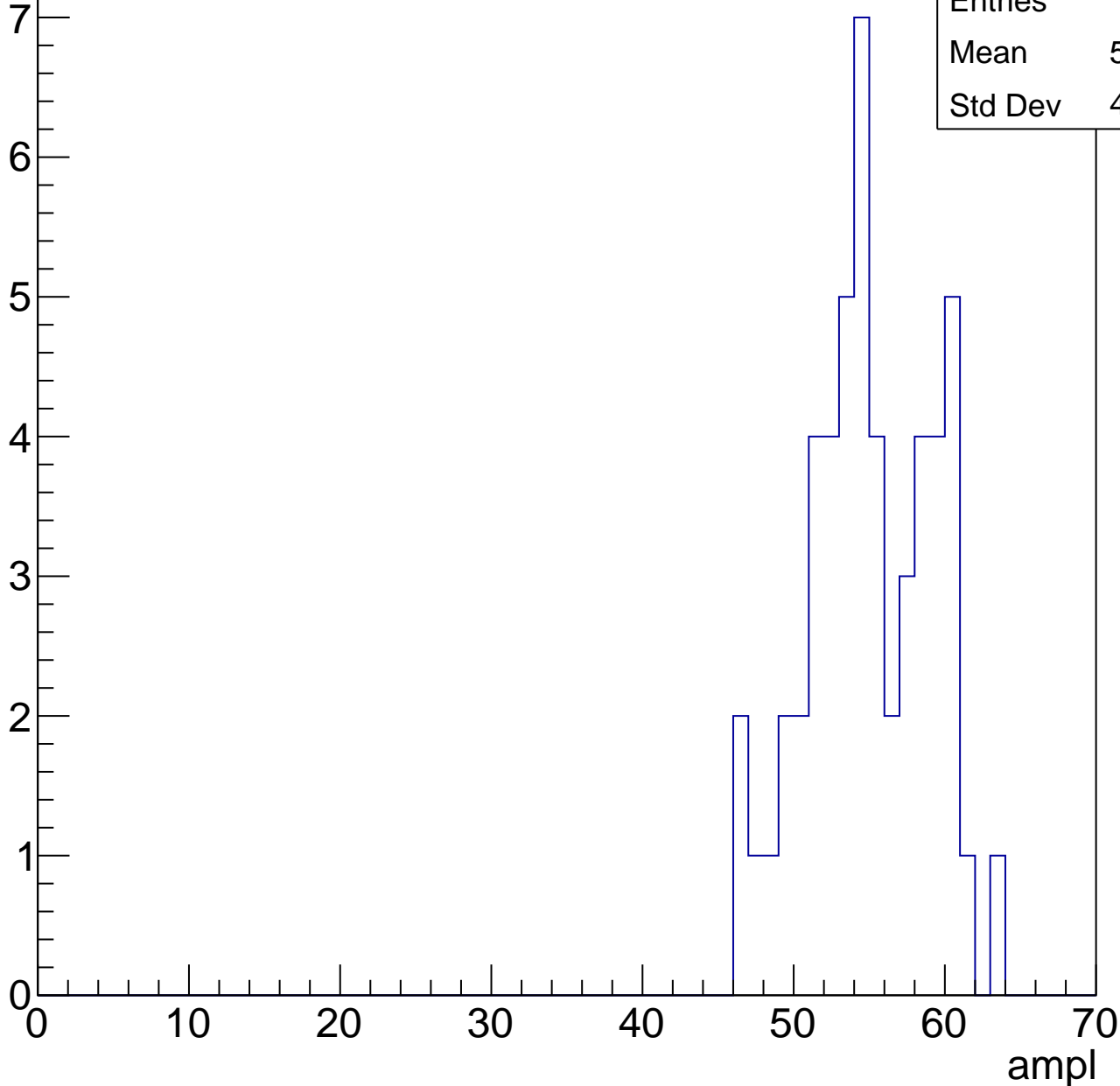


# B1L103S, U21-ch66, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	54.52
Std Dev	4.045

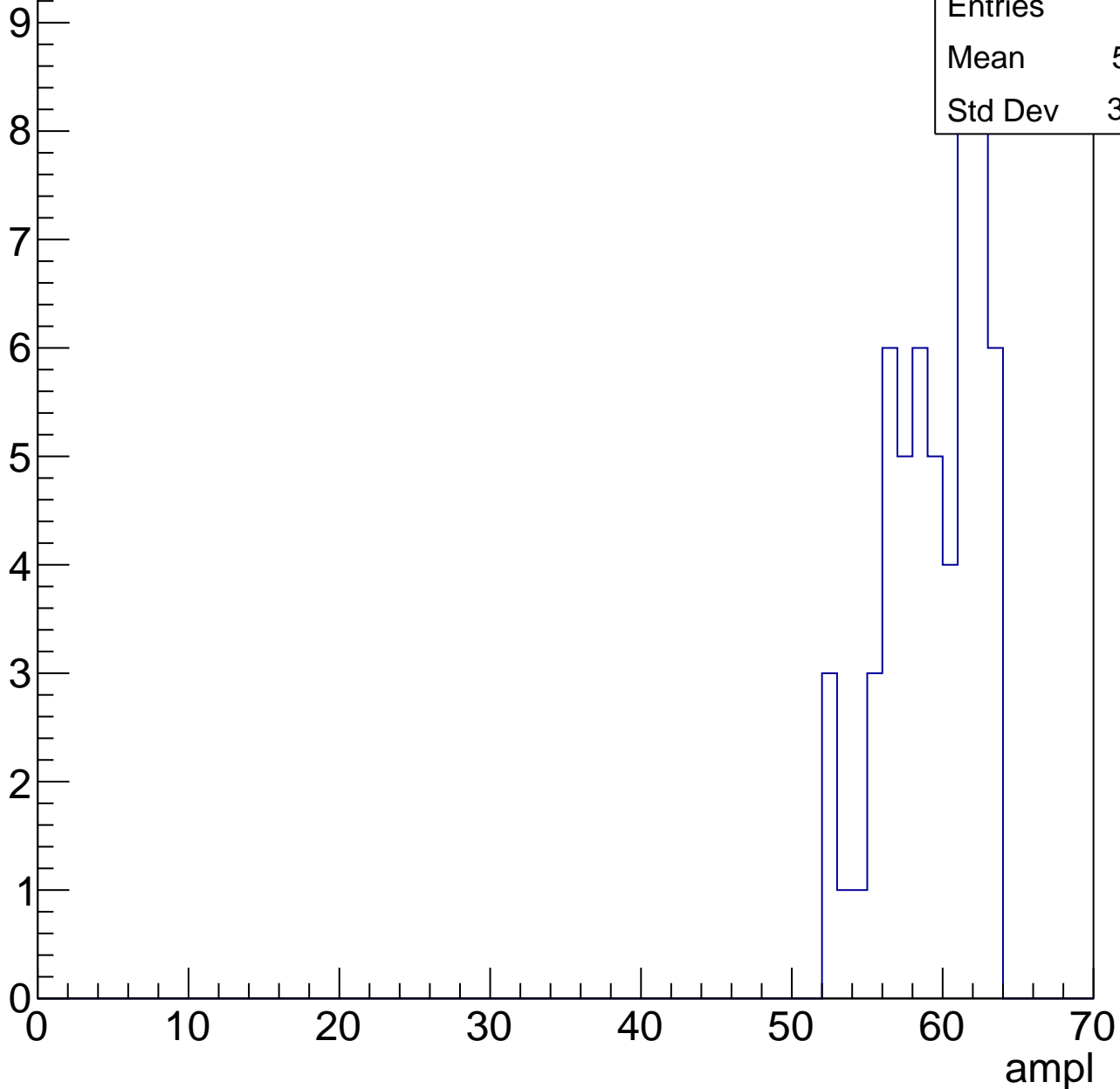


# B1L103S, U21-ch66, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

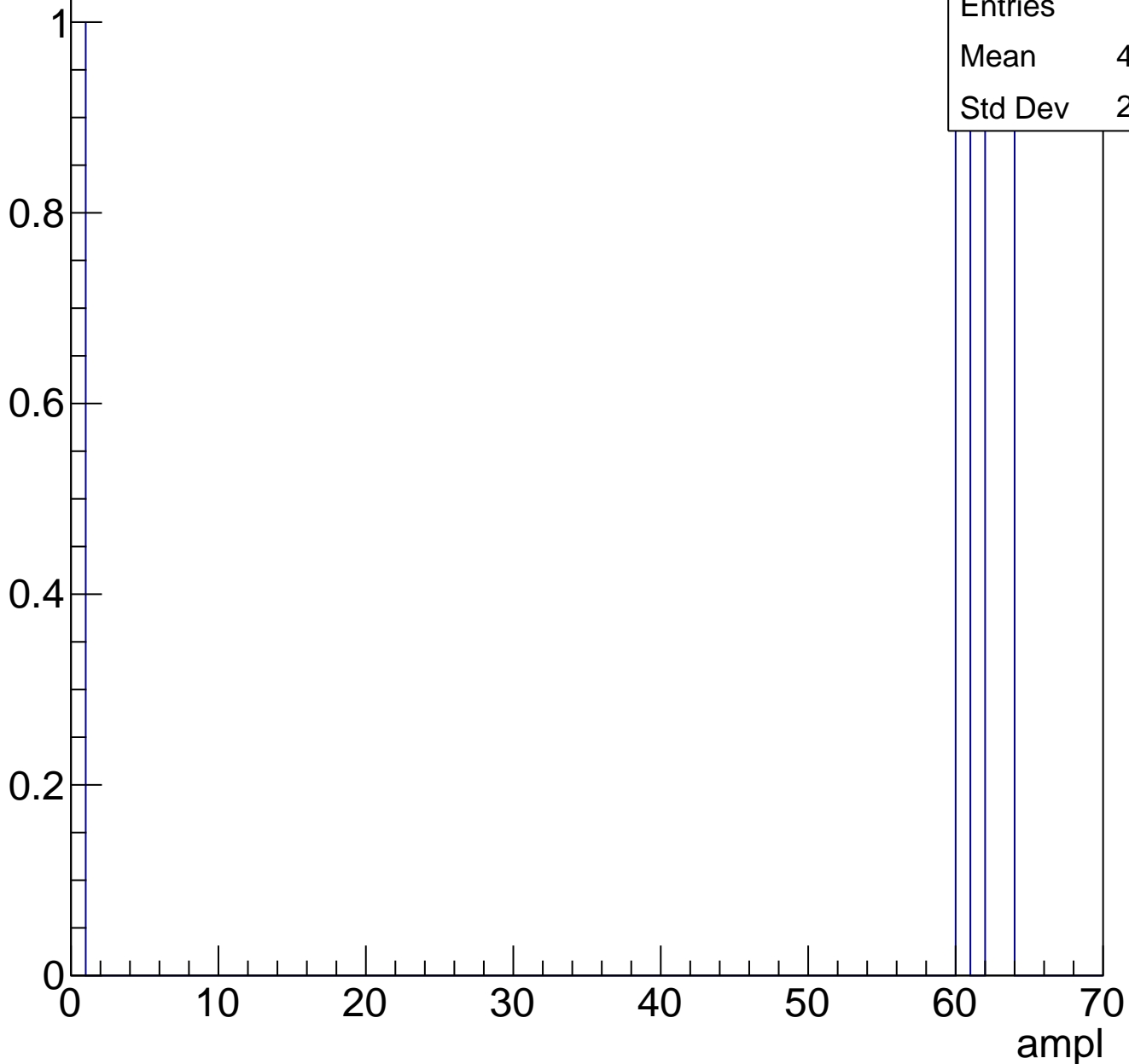
Entries	58
Mean	58.91
Std Dev	3.087



# B1L103S, U21-ch66, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

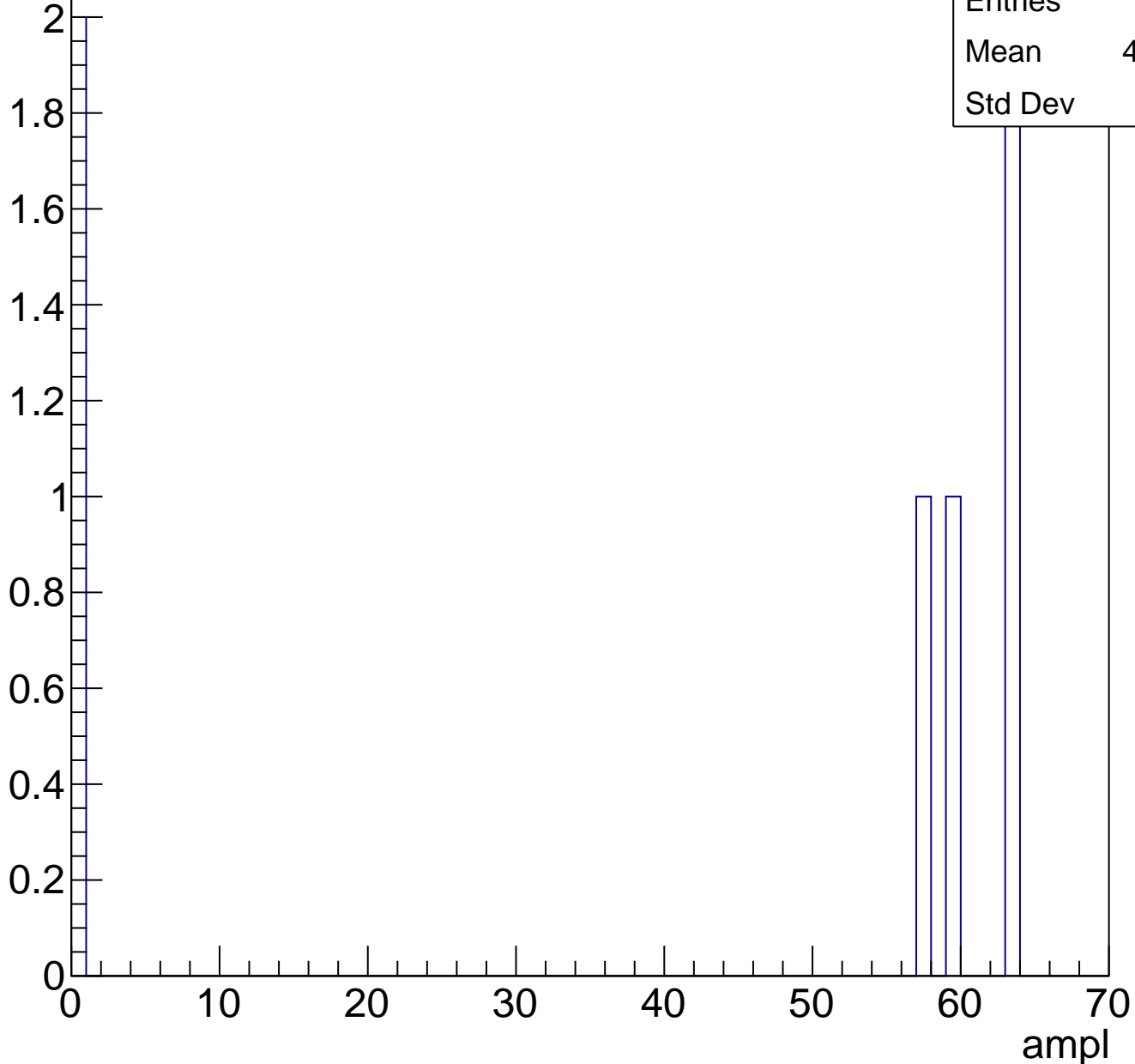




# B1L103S, U21-ch66, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U21-ch67, adc0

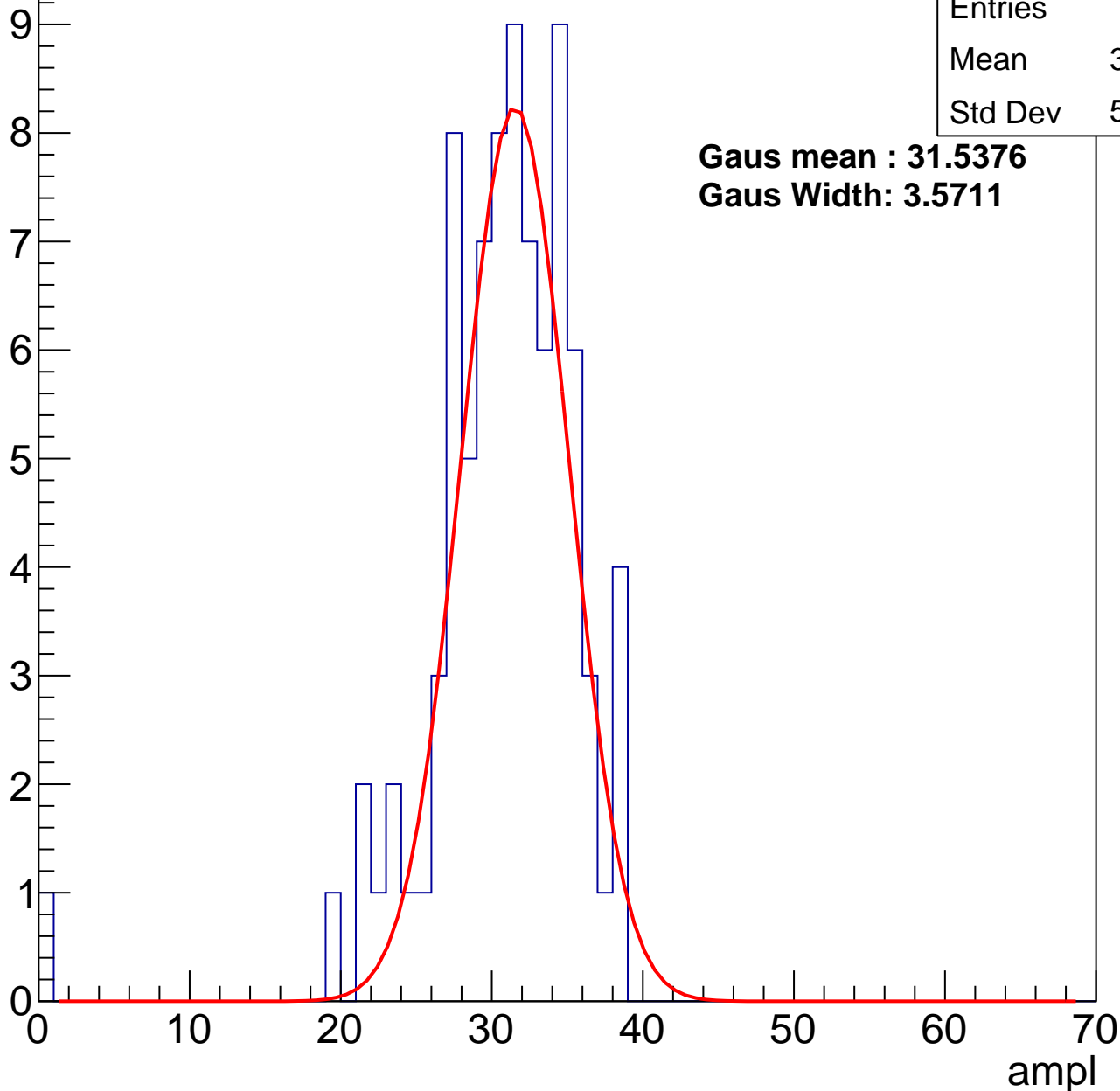
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	85
Mean	30.22
Std Dev	5.254

**Gaus mean : 31.5376**

**Gaus Width: 3.5711**



# B1L103S, U21-ch67, adc1

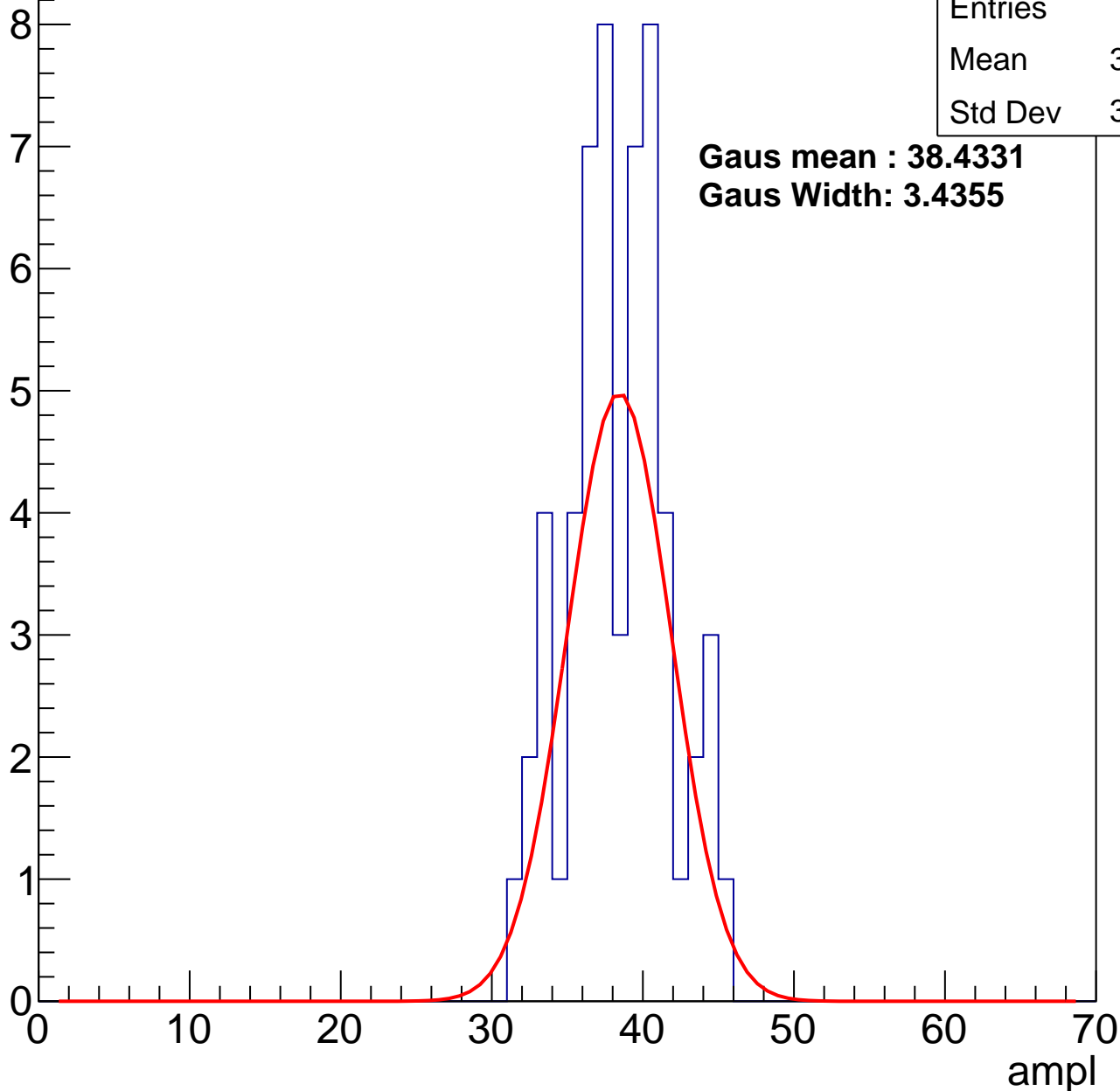
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	37.95
Std Dev	3.292

**Gaus mean : 38.4331**

**Gaus Width: 3.4355**



# B1L103S, U21-ch67, adc2

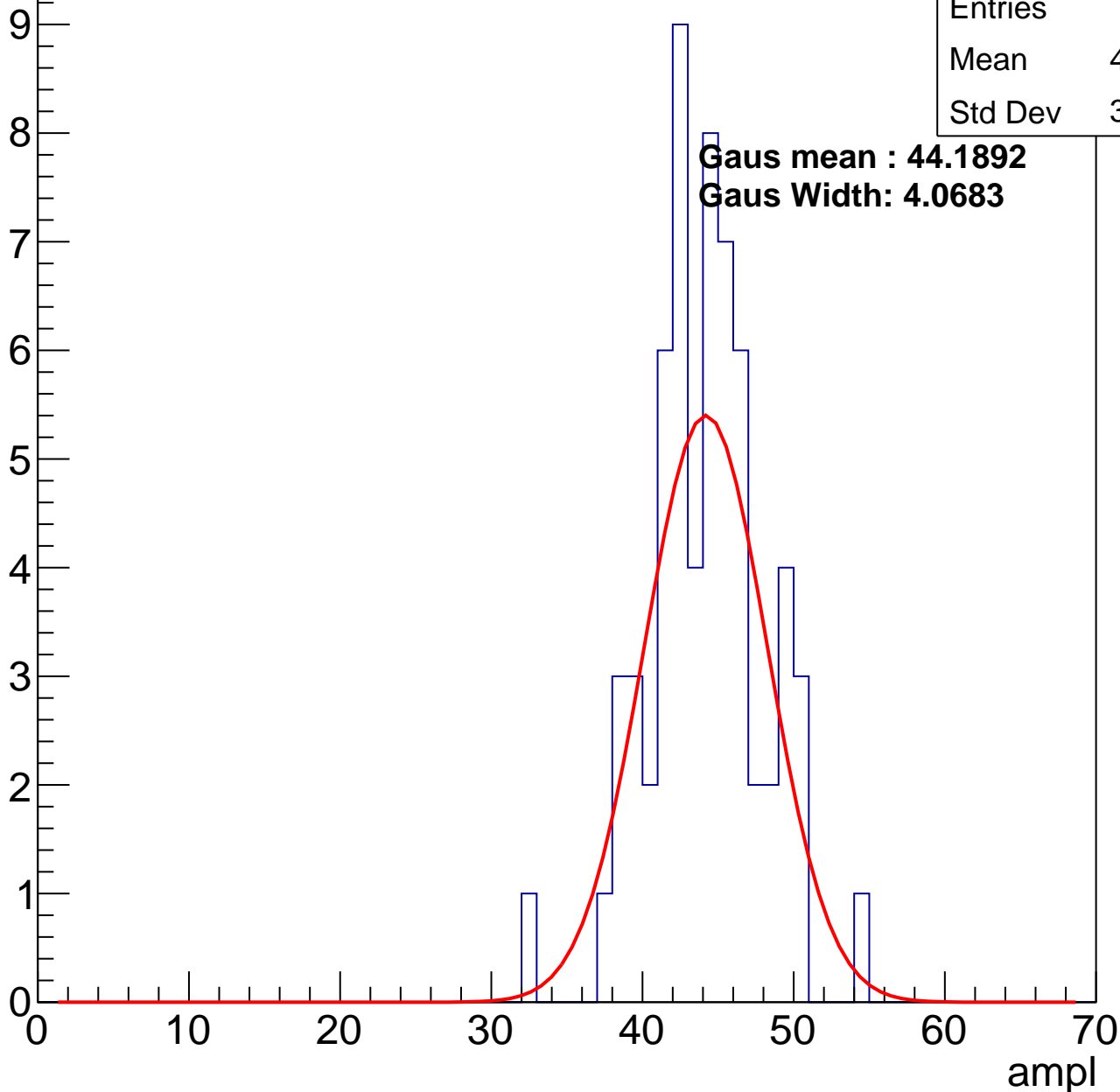
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	43.69
Std Dev	3.778

**Gaus mean : 44.1892**

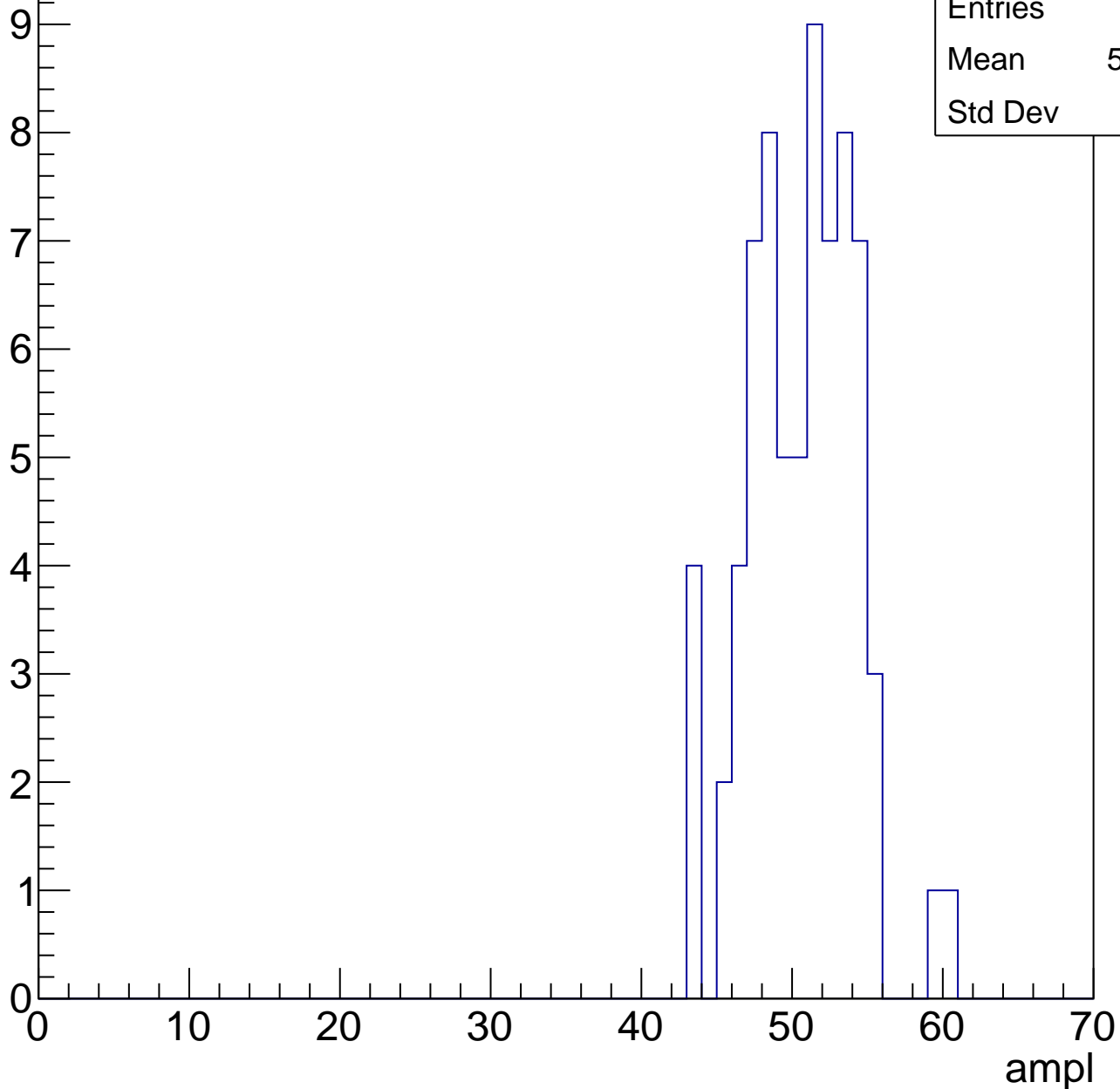
**Gaus Width: 4.0683**



# B1L103S, U21-ch67, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

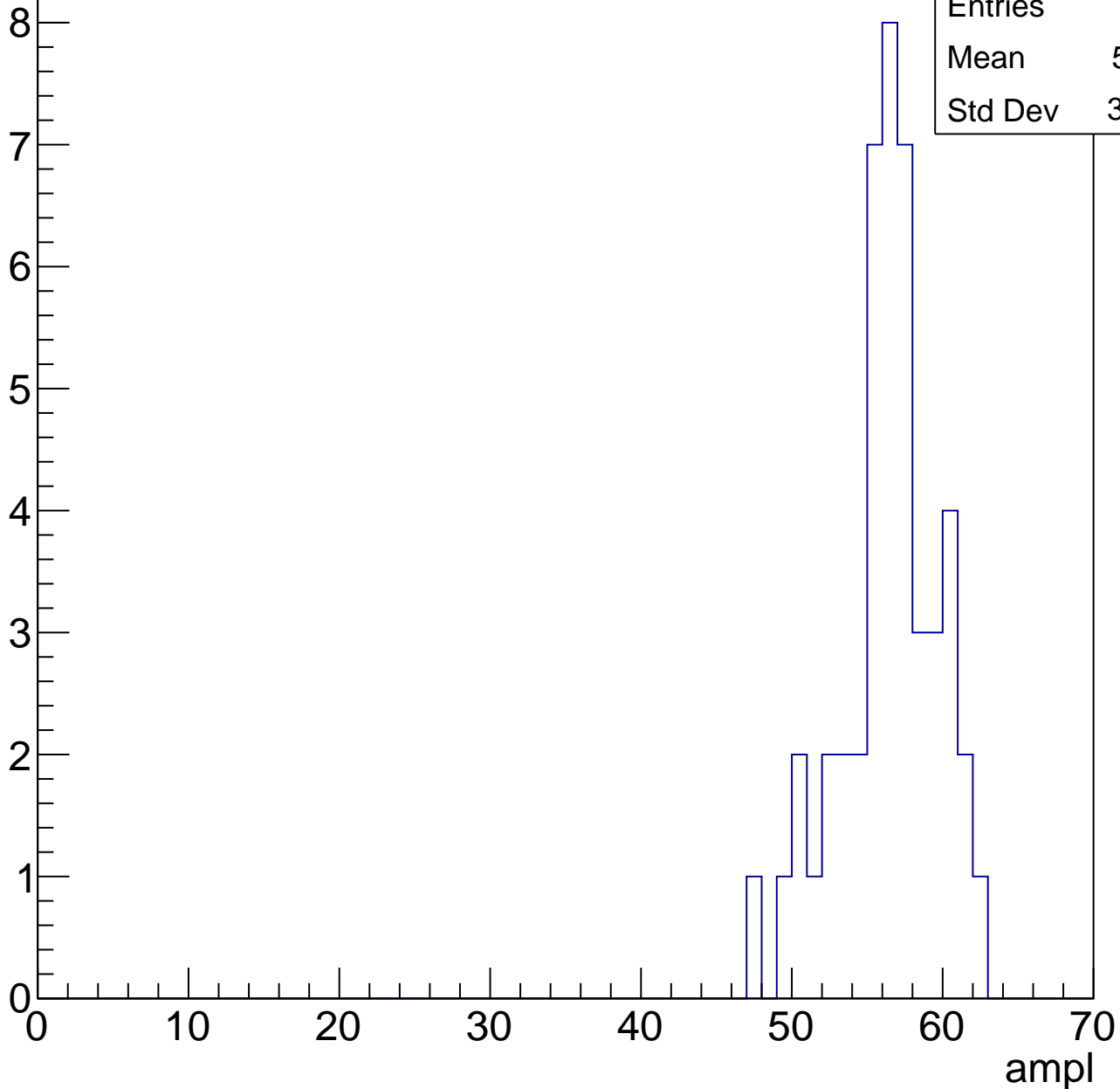


# B1L103S, U21-ch67, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	46
Mean	55.91
Std Dev	3.256

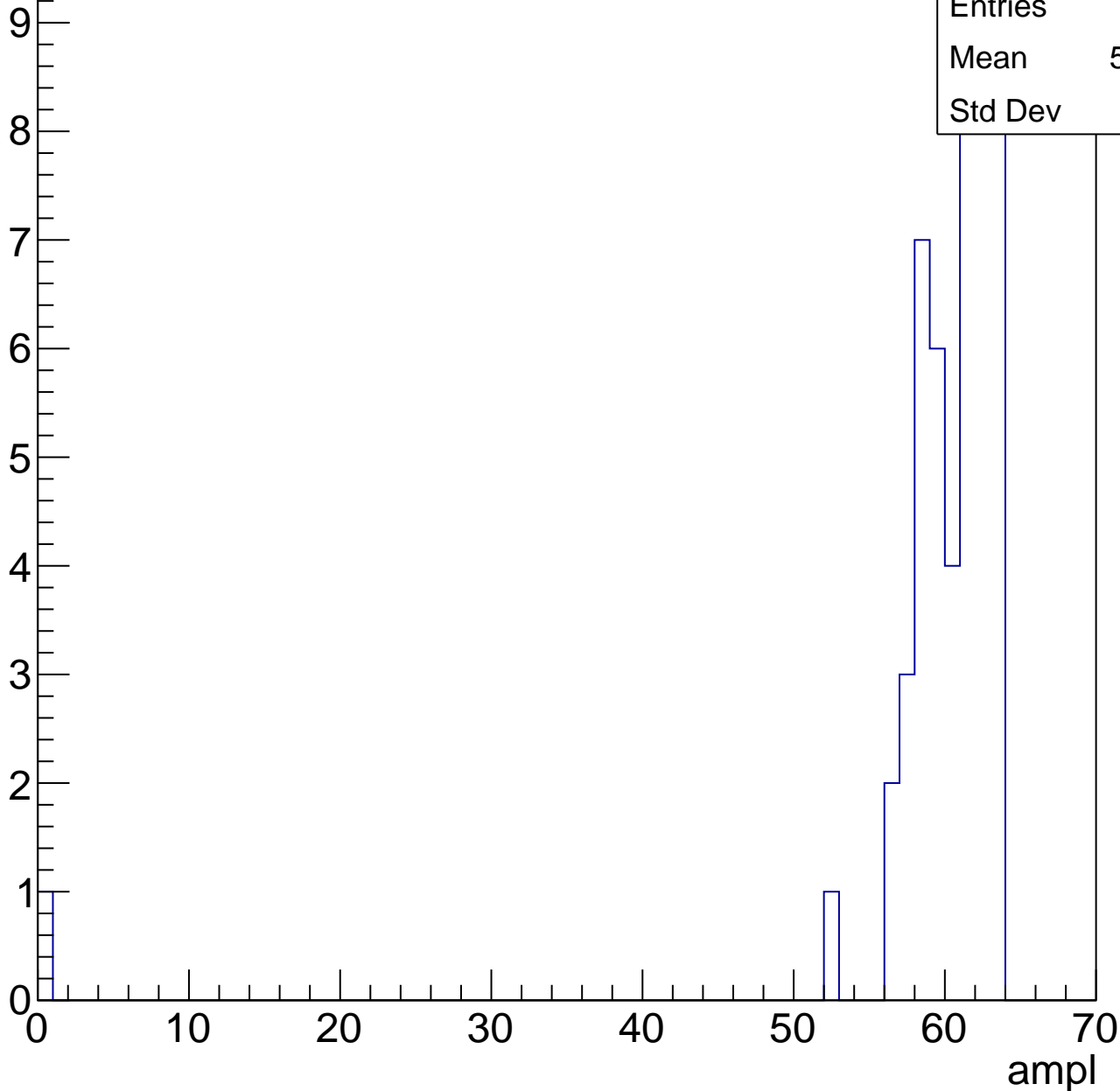


# B1L103S, U21-ch67, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	58.96
Std Dev	8.75



# B1L103S, U21-ch67, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U21-ch67, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U21-ch68, adc0

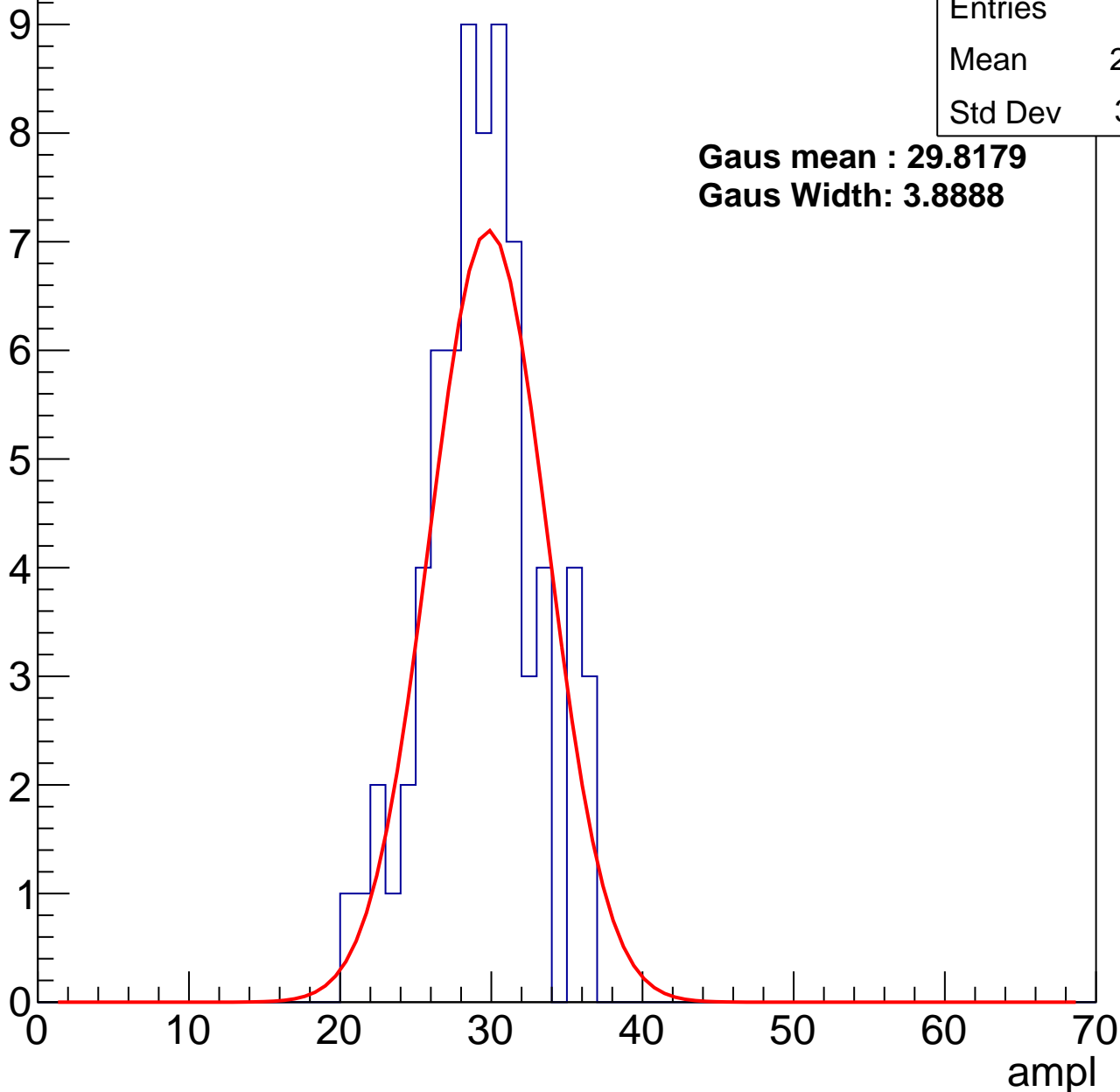
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	28.87
Std Dev	3.581

**Gaus mean : 29.8179**

**Gaus Width: 3.8888**



# B1L103S, U21-ch68, adc1

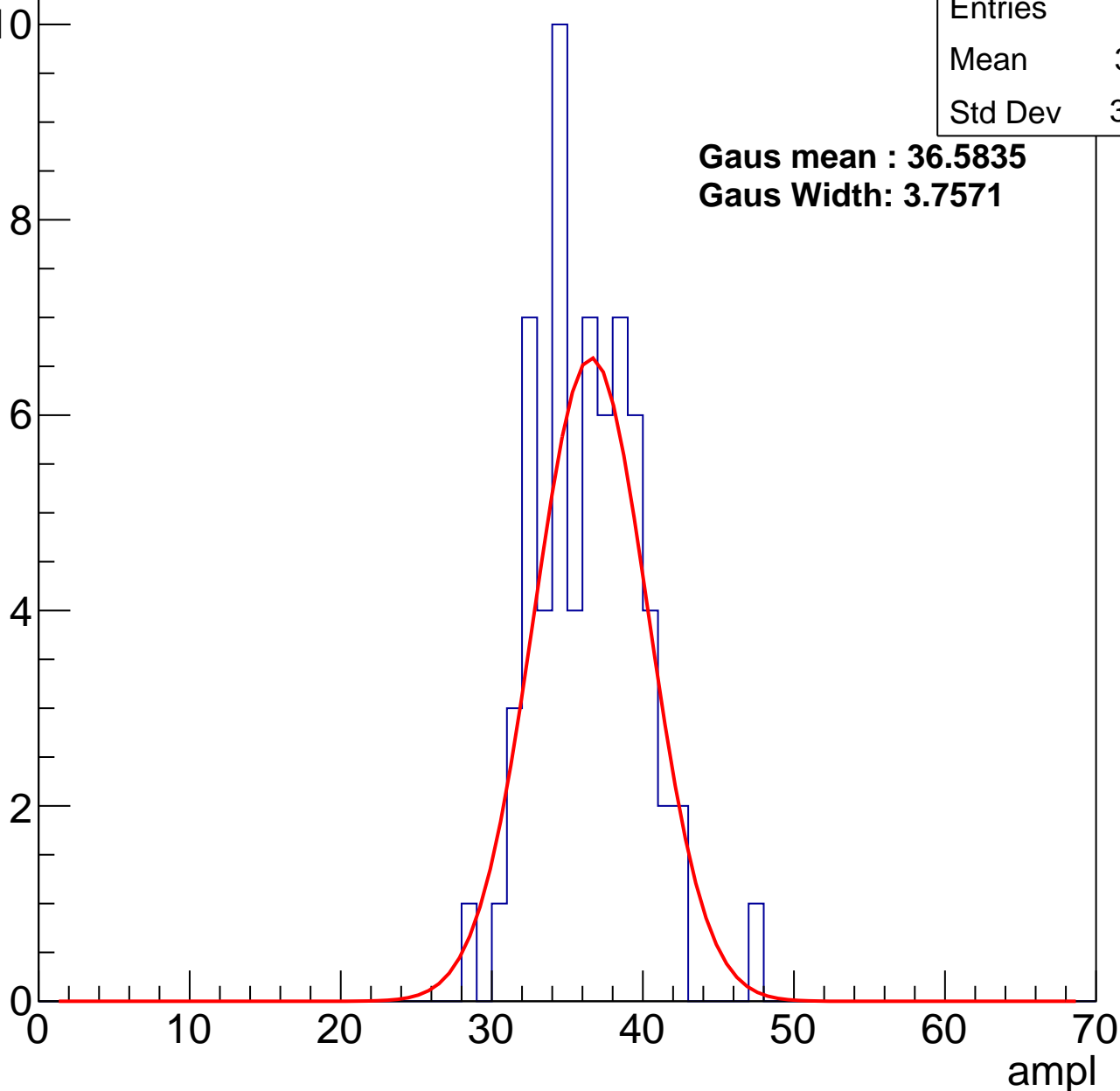
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	35.91
Std Dev	3.423

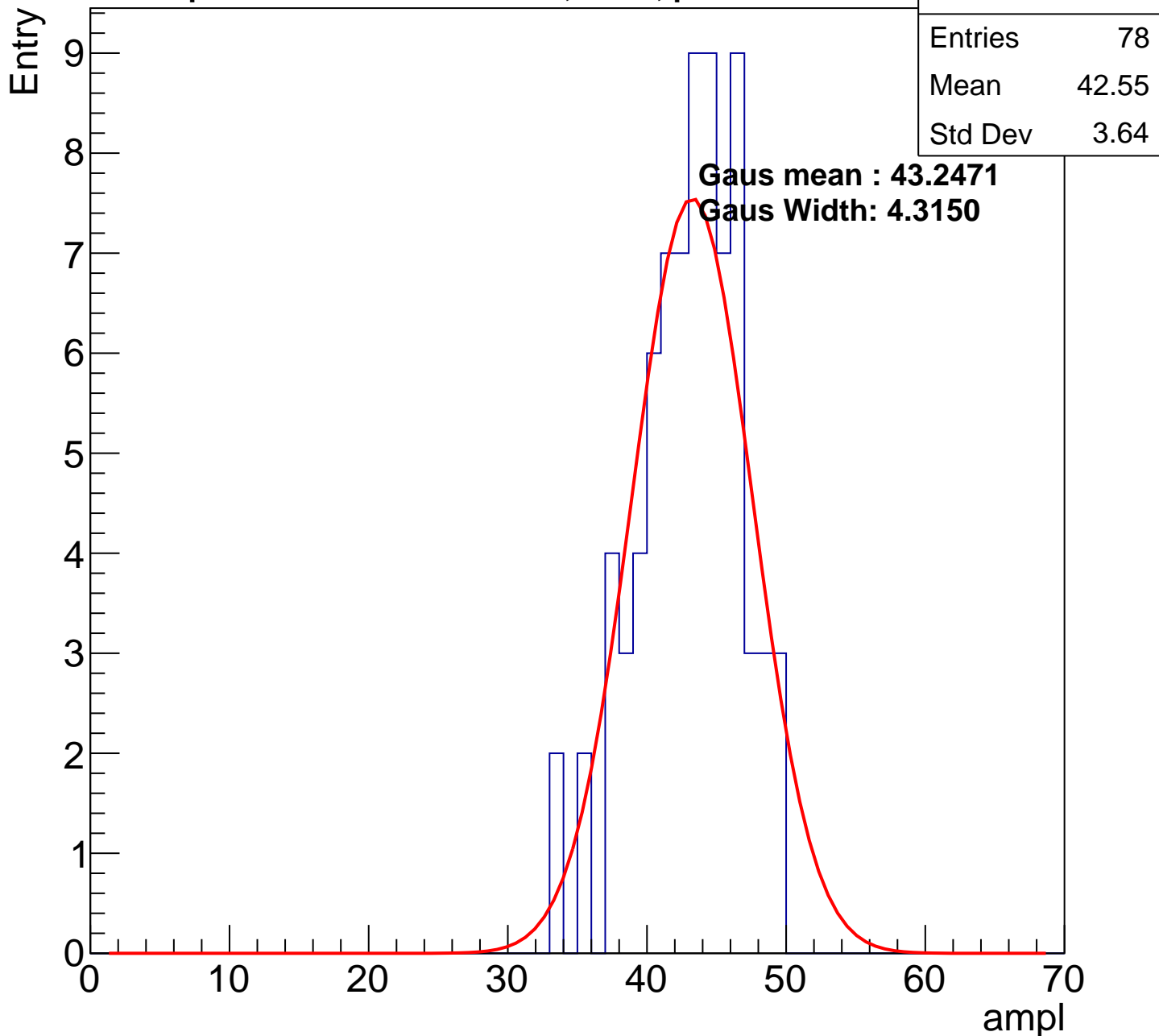
**Gaus mean : 36.5835**

**Gaus Width: 3.7571**



# B1L103S, U21-ch68, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

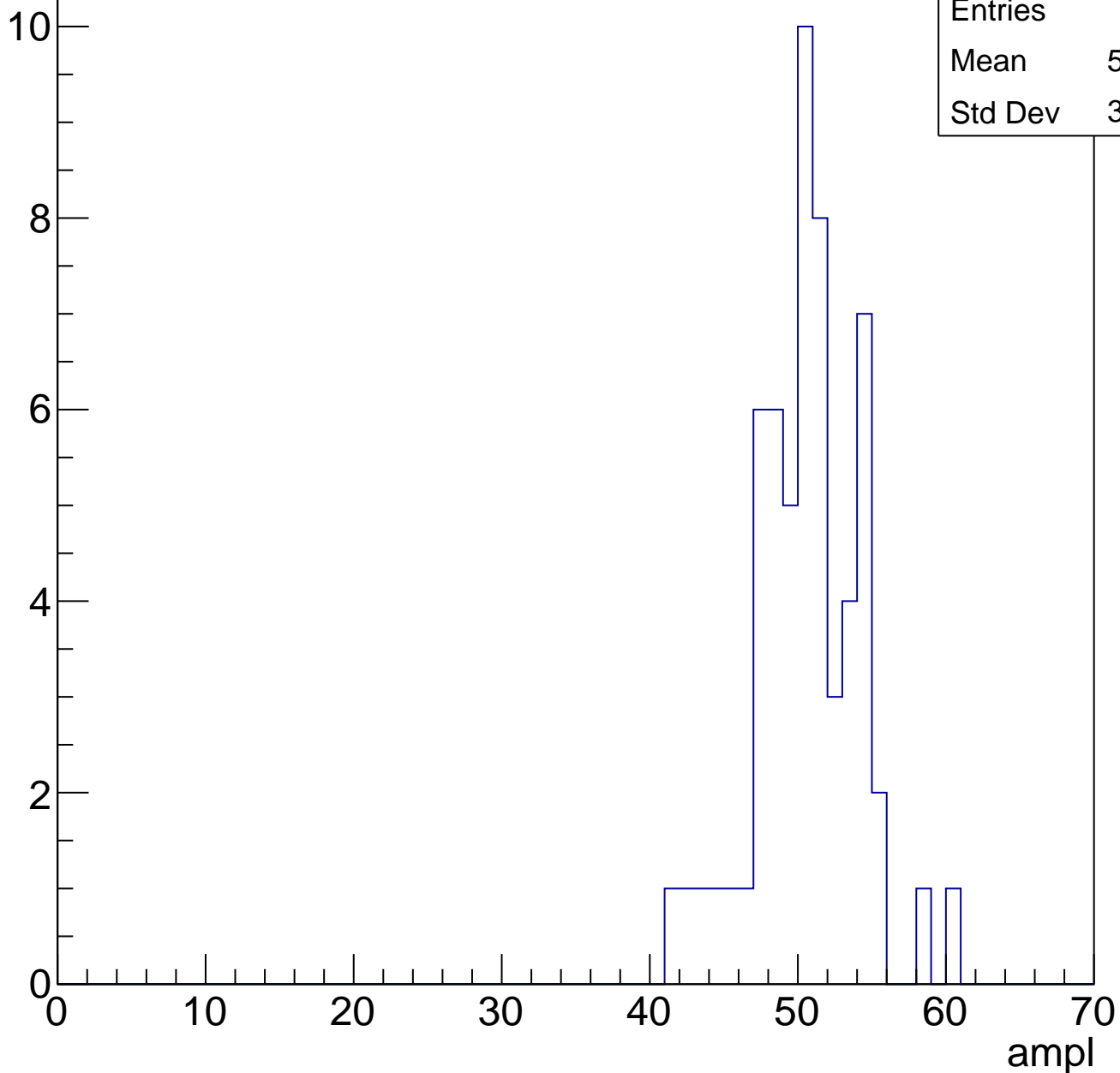


# B1L103S, U21-ch68, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	50.14
Std Dev	3.529

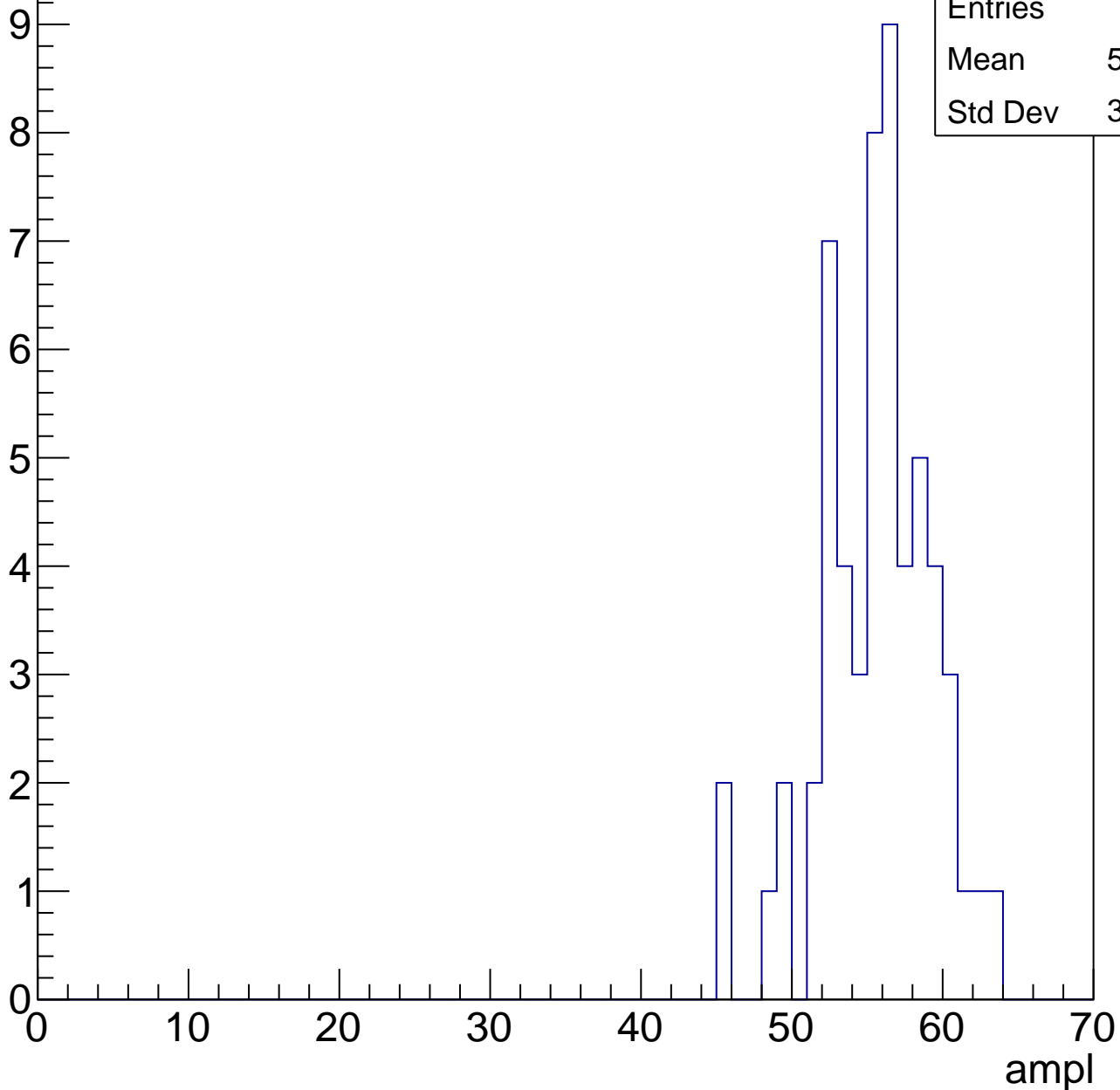


# B1L103S, U21-ch68, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	55.09
Std Dev	3.729

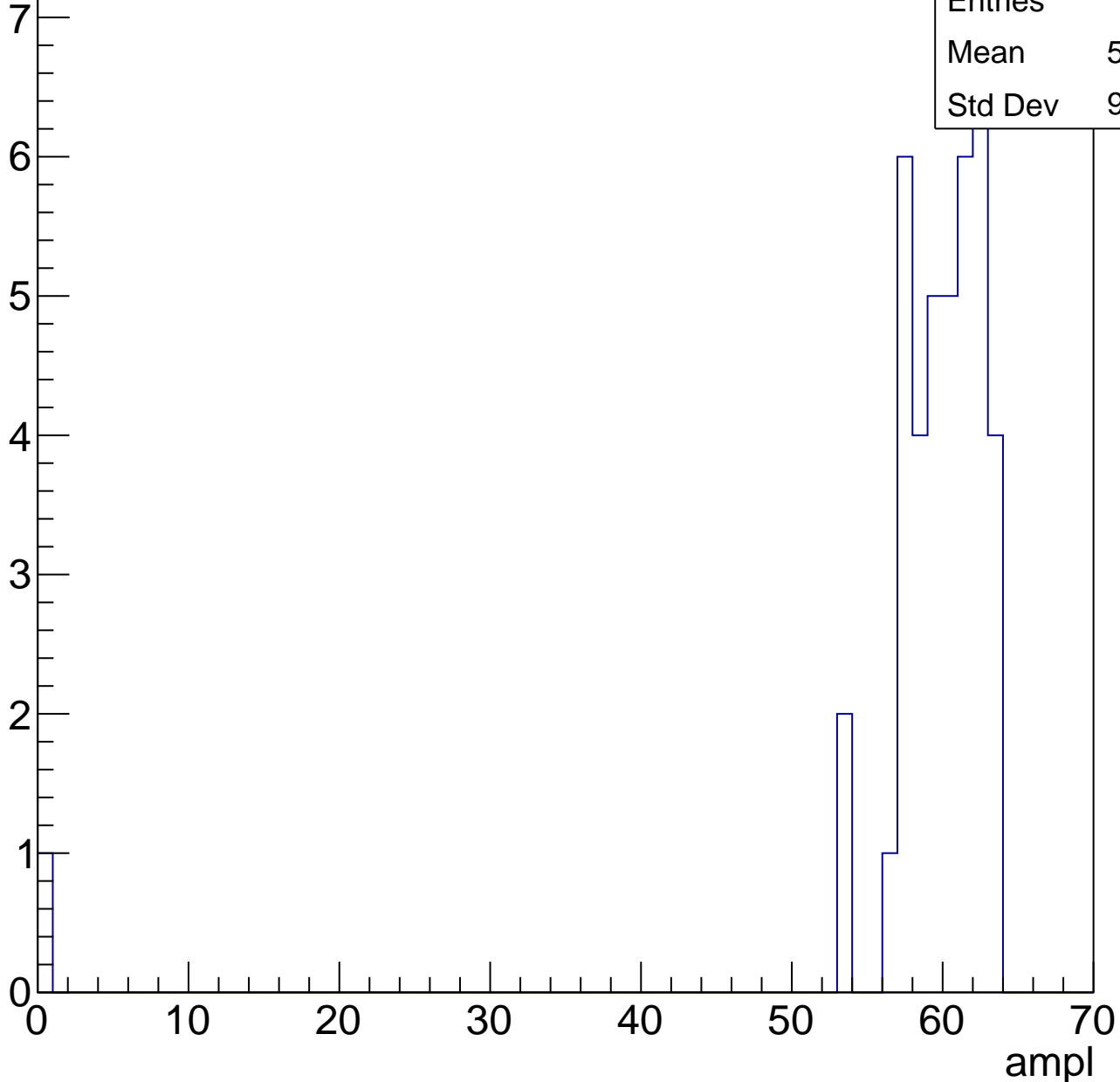


# B1L103S, U21-ch68, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	41
Mean	58.12
Std Dev	9.518

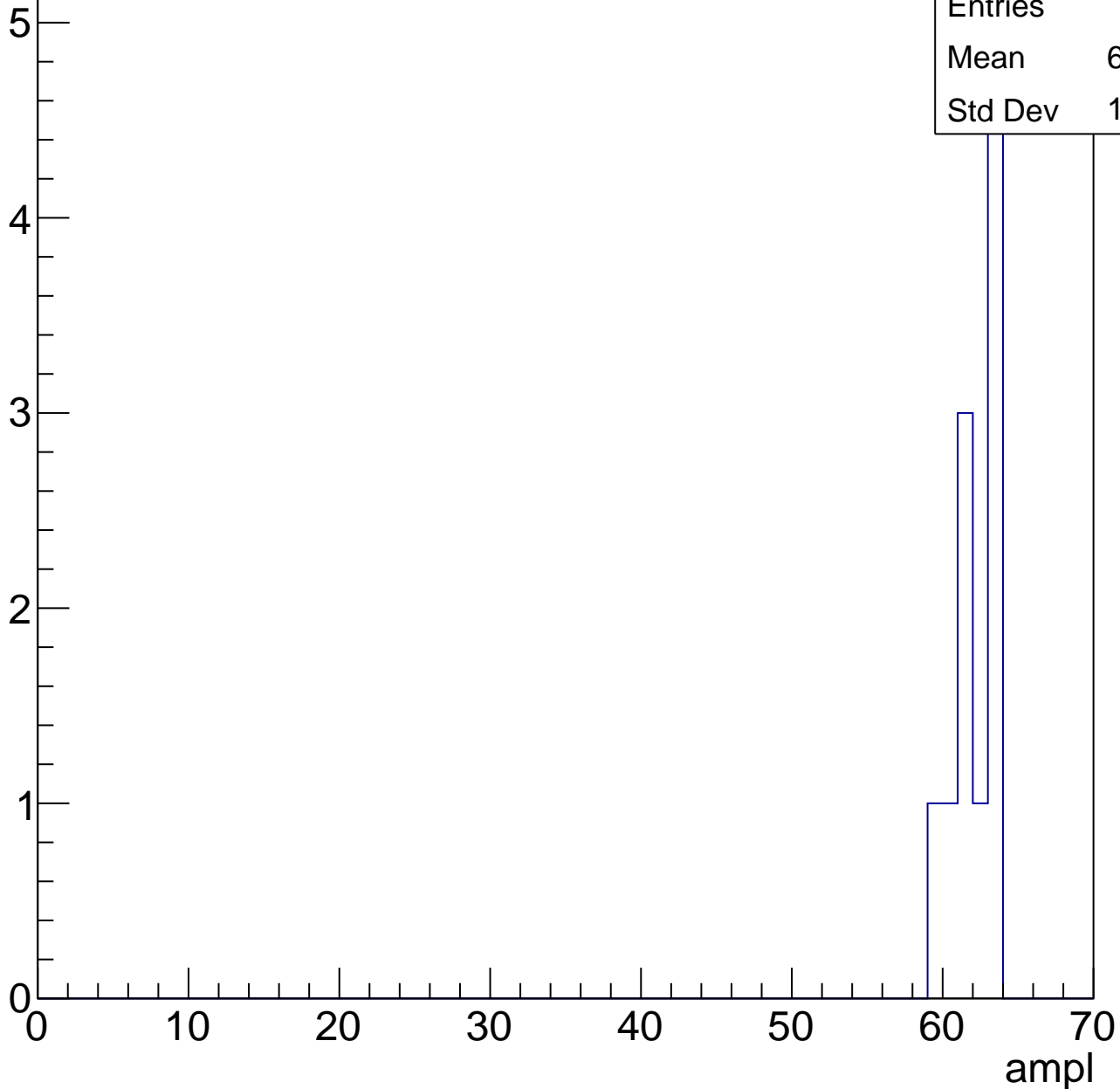


# B1L103S, U21-ch68, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	11
Mean	61.73
Std Dev	1.355





# B1L103S, U21-ch68, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U21-ch69, adc0

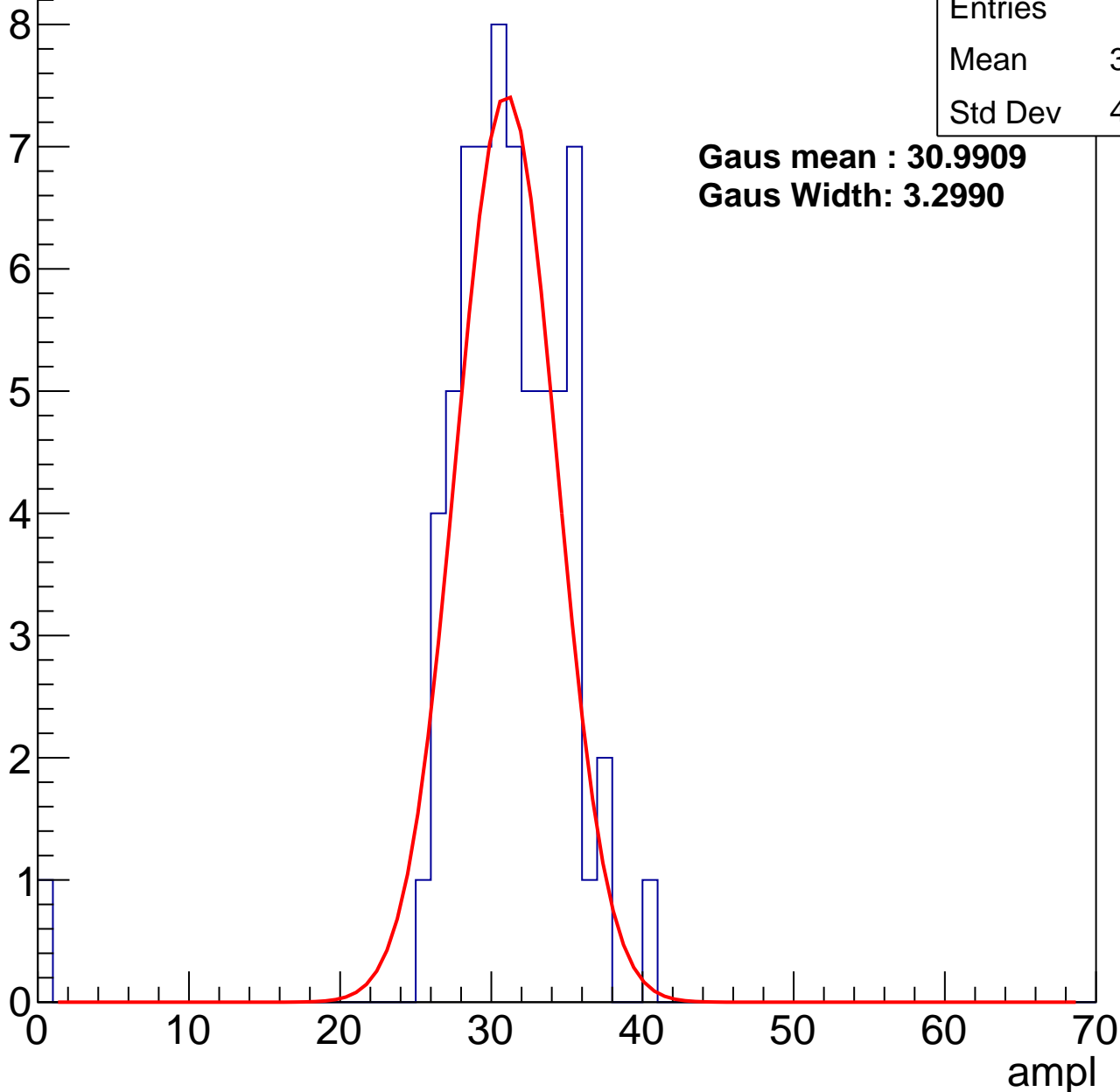
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	30.45
Std Dev	4.949

**Gaus mean : 30.9909**

**Gaus Width: 3.2990**



# B1L103S, U21-ch69, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	79
Mean	38.29
Std Dev	3.65

**Gaus mean : 38.7341**

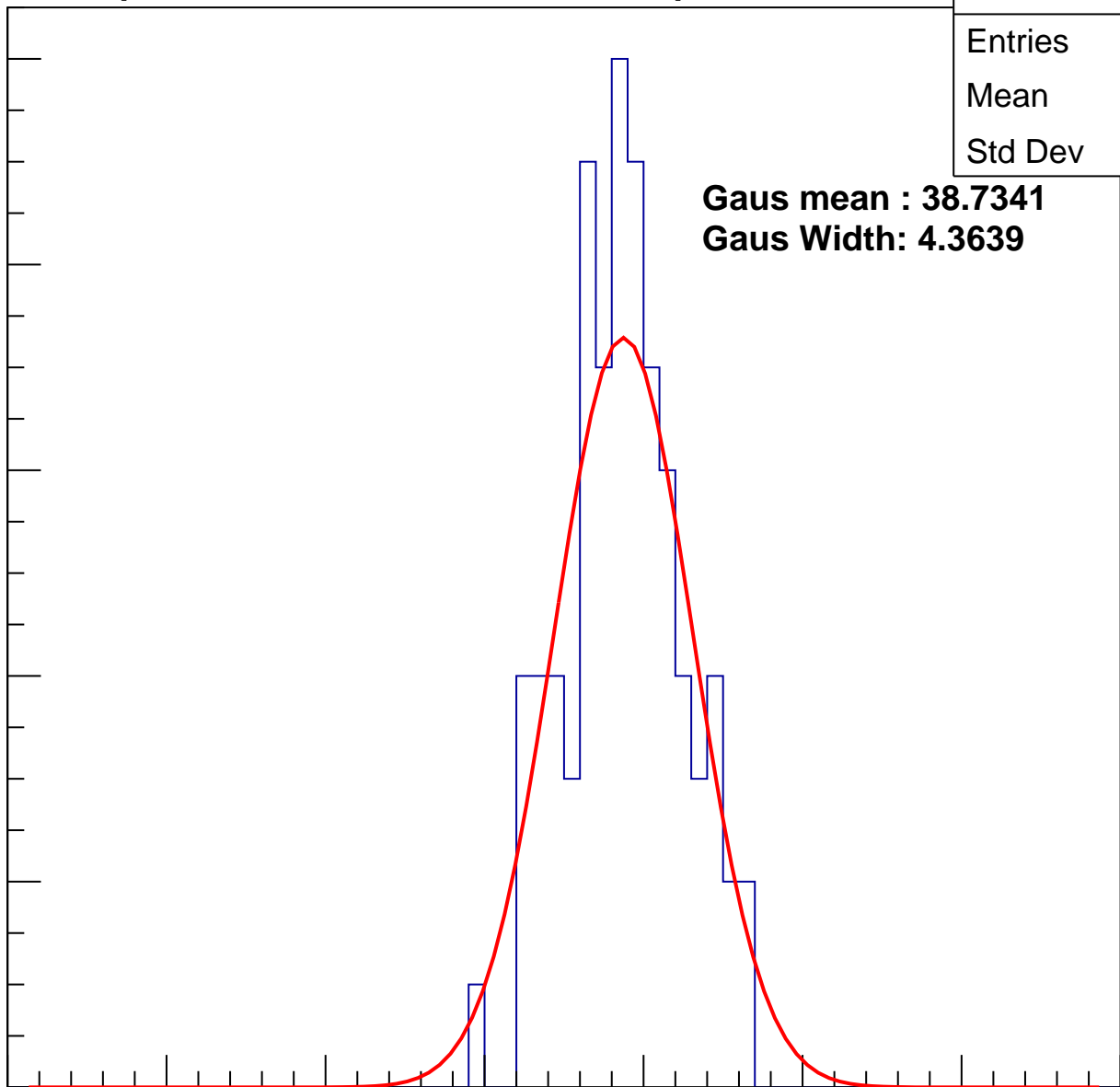
**Gaus Width: 4.3639**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

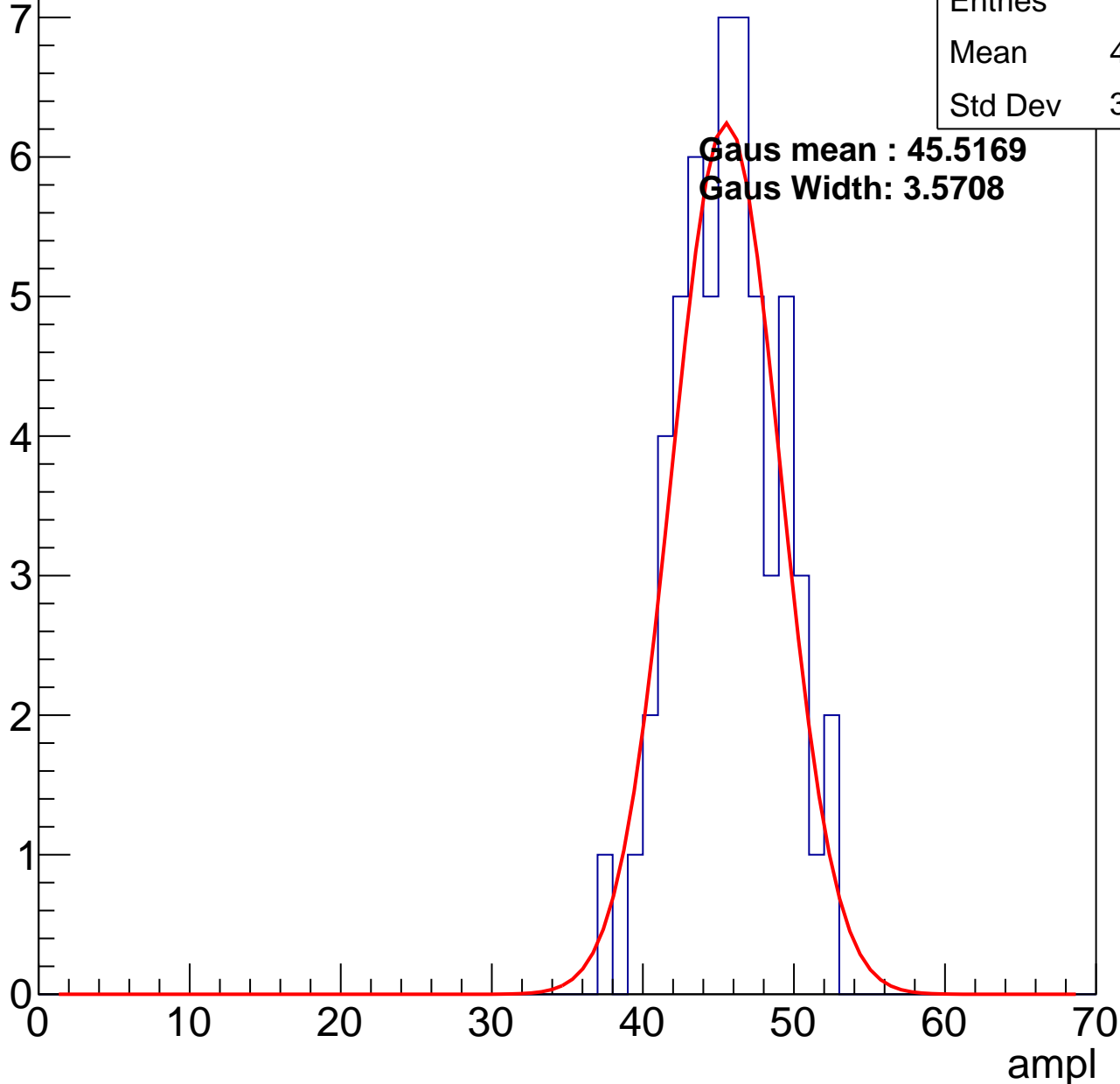


# B1L103S, U21-ch69, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	45.16
Std Dev	3.323

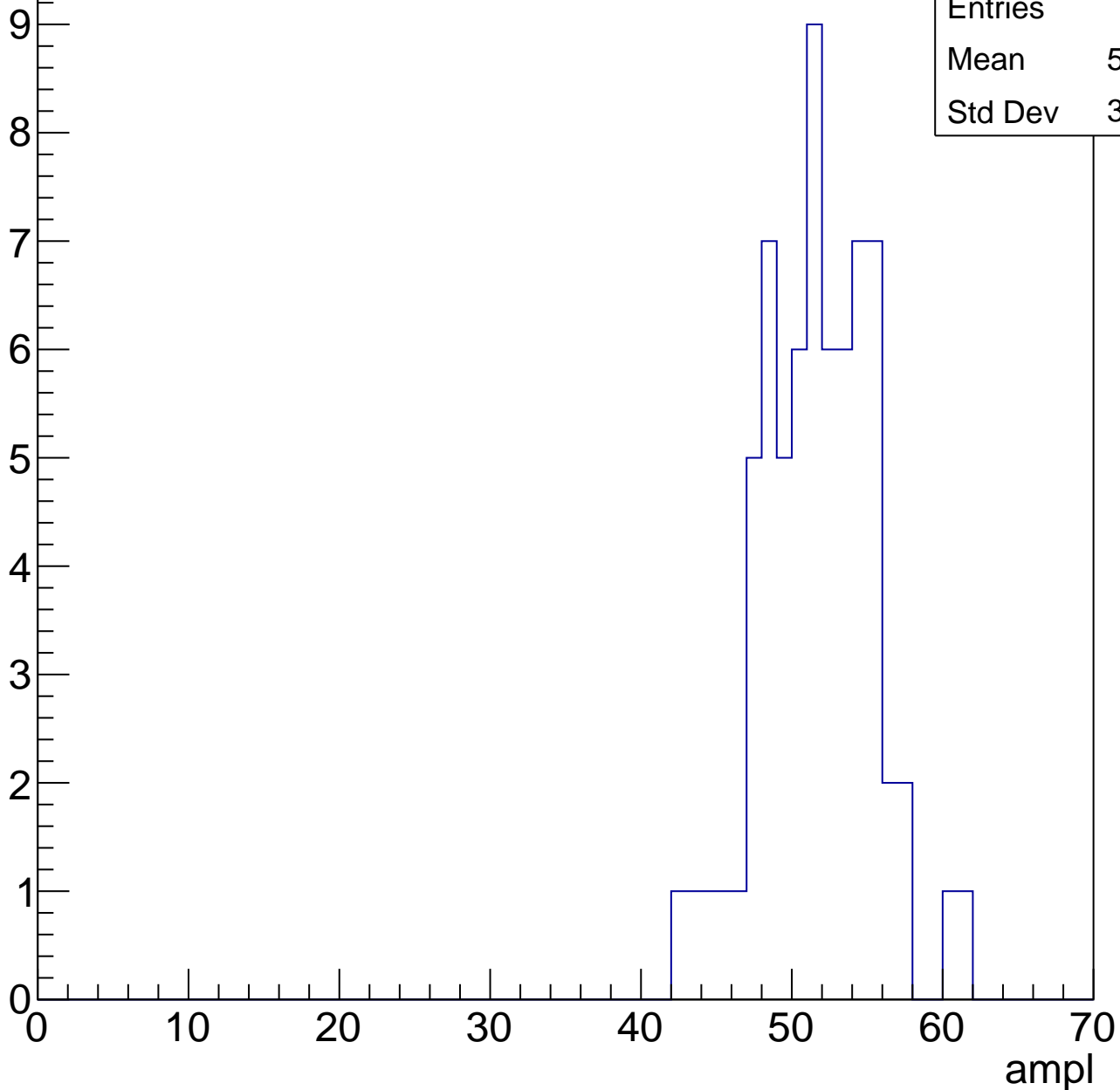


# B1L103S, U21-ch69, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	51.23
Std Dev	3.668

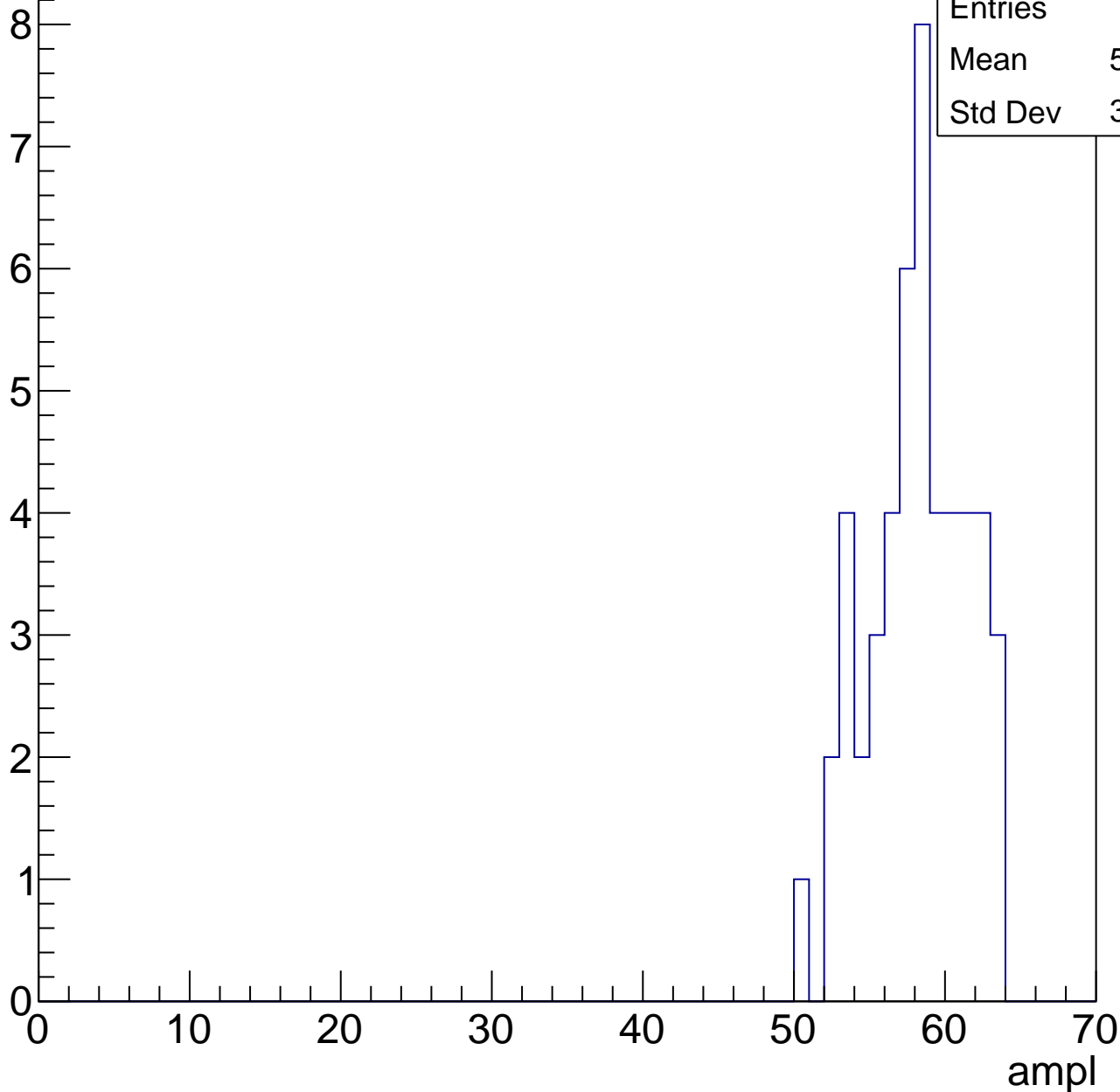


# B1L103S, U21-ch69, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

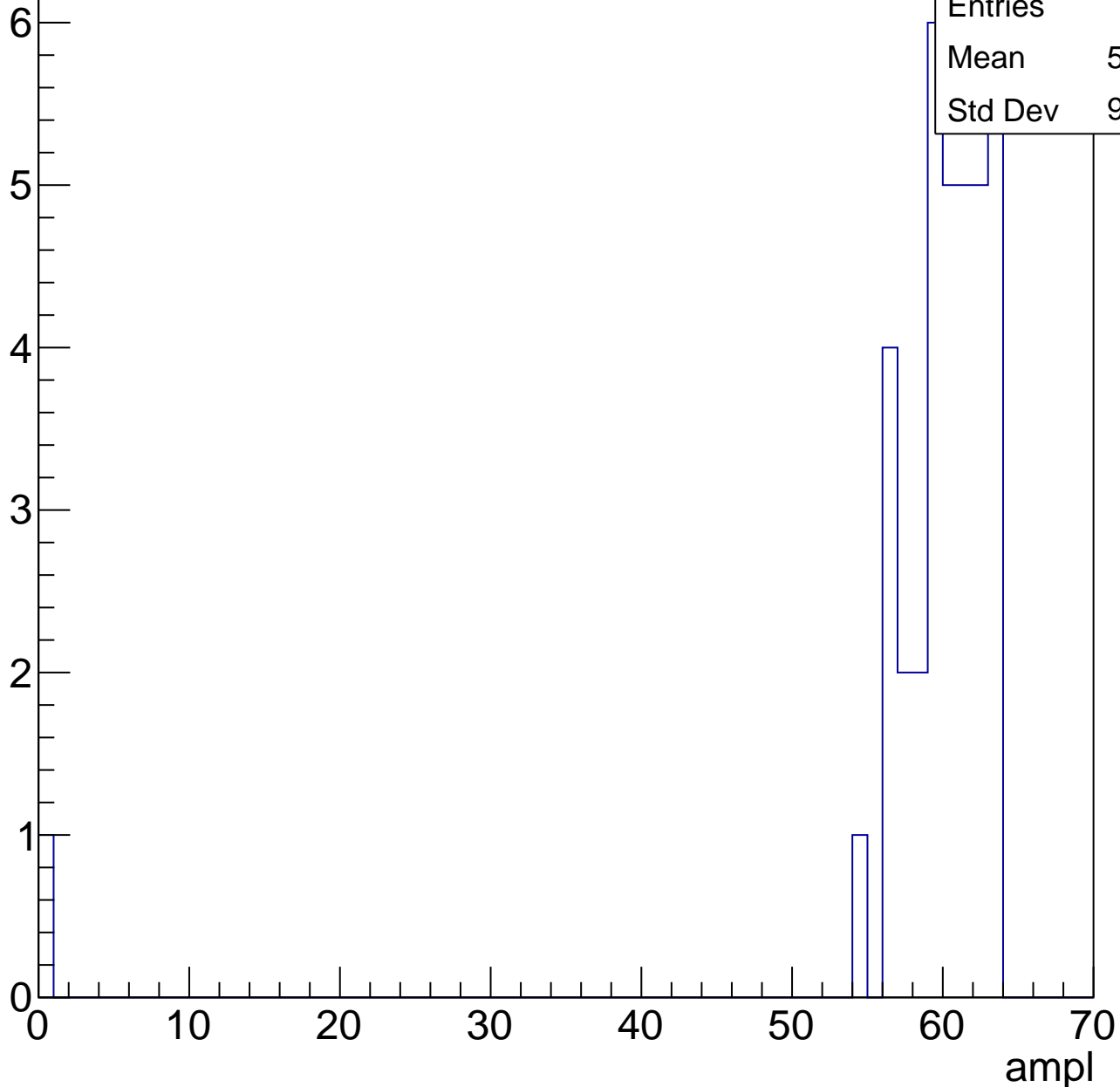
Entries	49
Mean	57.67
Std Dev	3.216



# B1L103S, U21-ch69, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U21-ch69, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U21-ch69, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U21-ch70, adc0

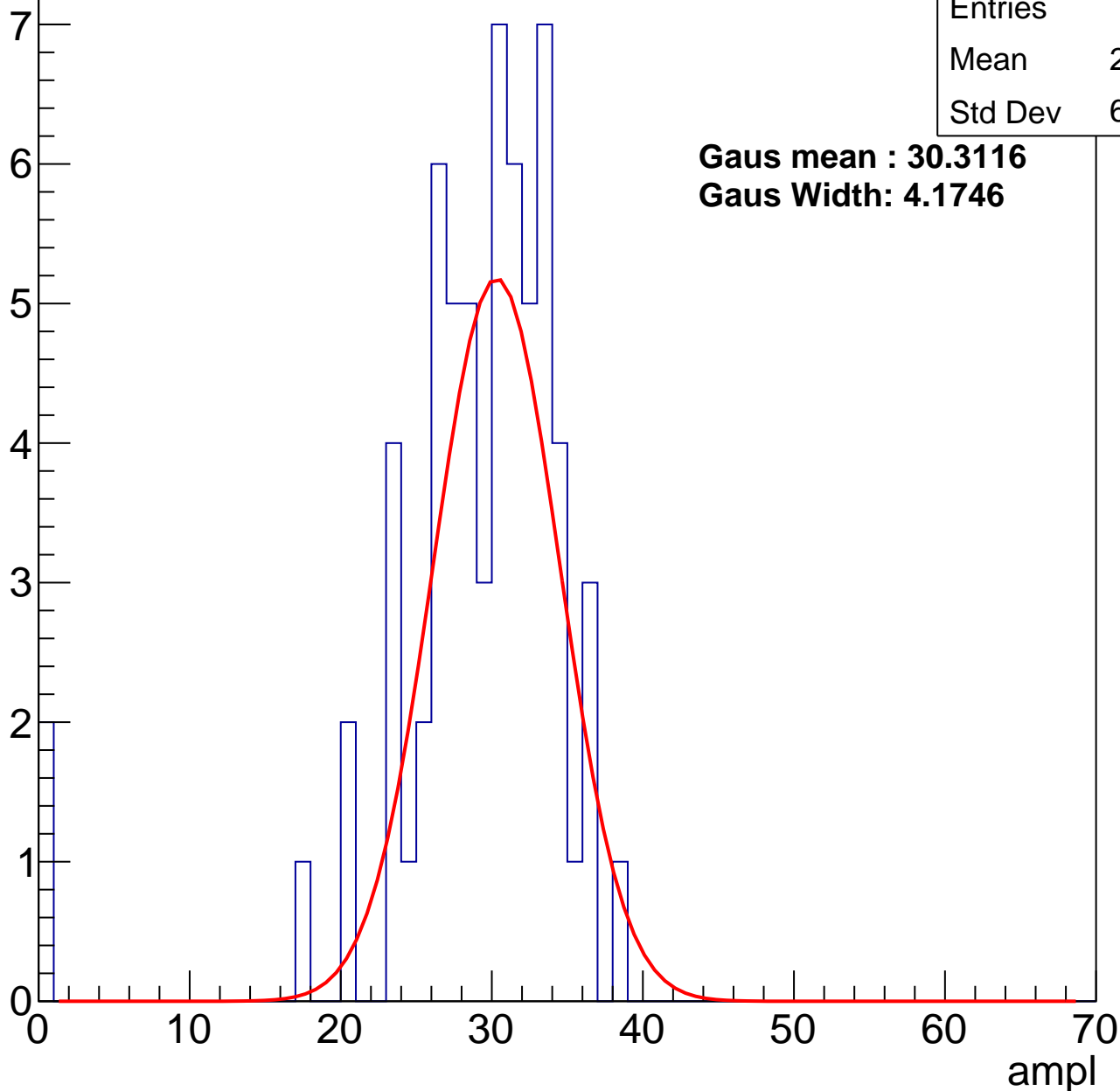
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	28.38
Std Dev	6.558

**Gaus mean : 30.3116**

**Gaus Width: 4.1746**



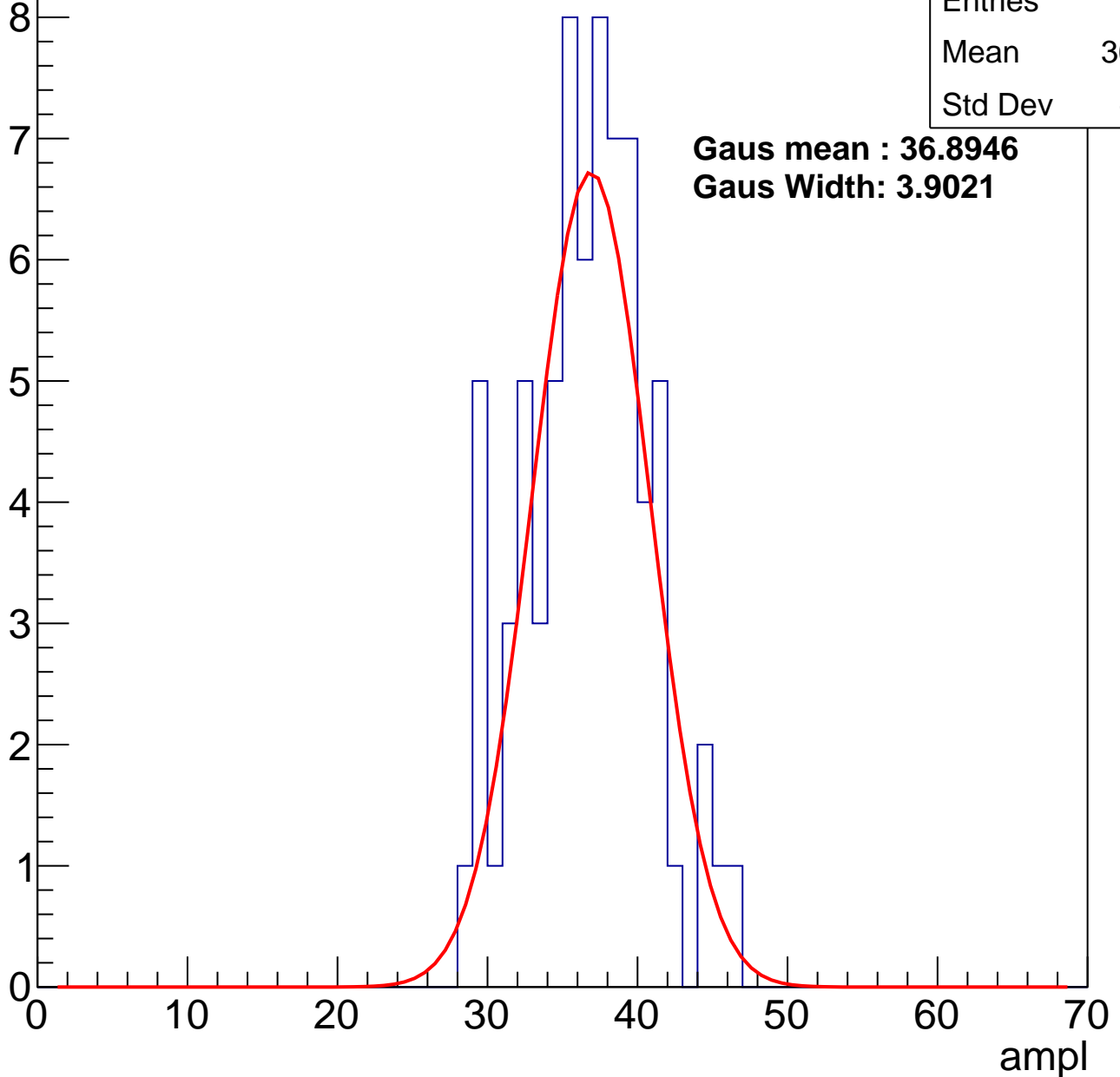
# B1L103S, U21-ch70, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	36.19
Std Dev	4.03

**Gaus mean : 36.8946**  
**Gaus Width: 3.9021**



# B1L103S, U21-ch70, adc2

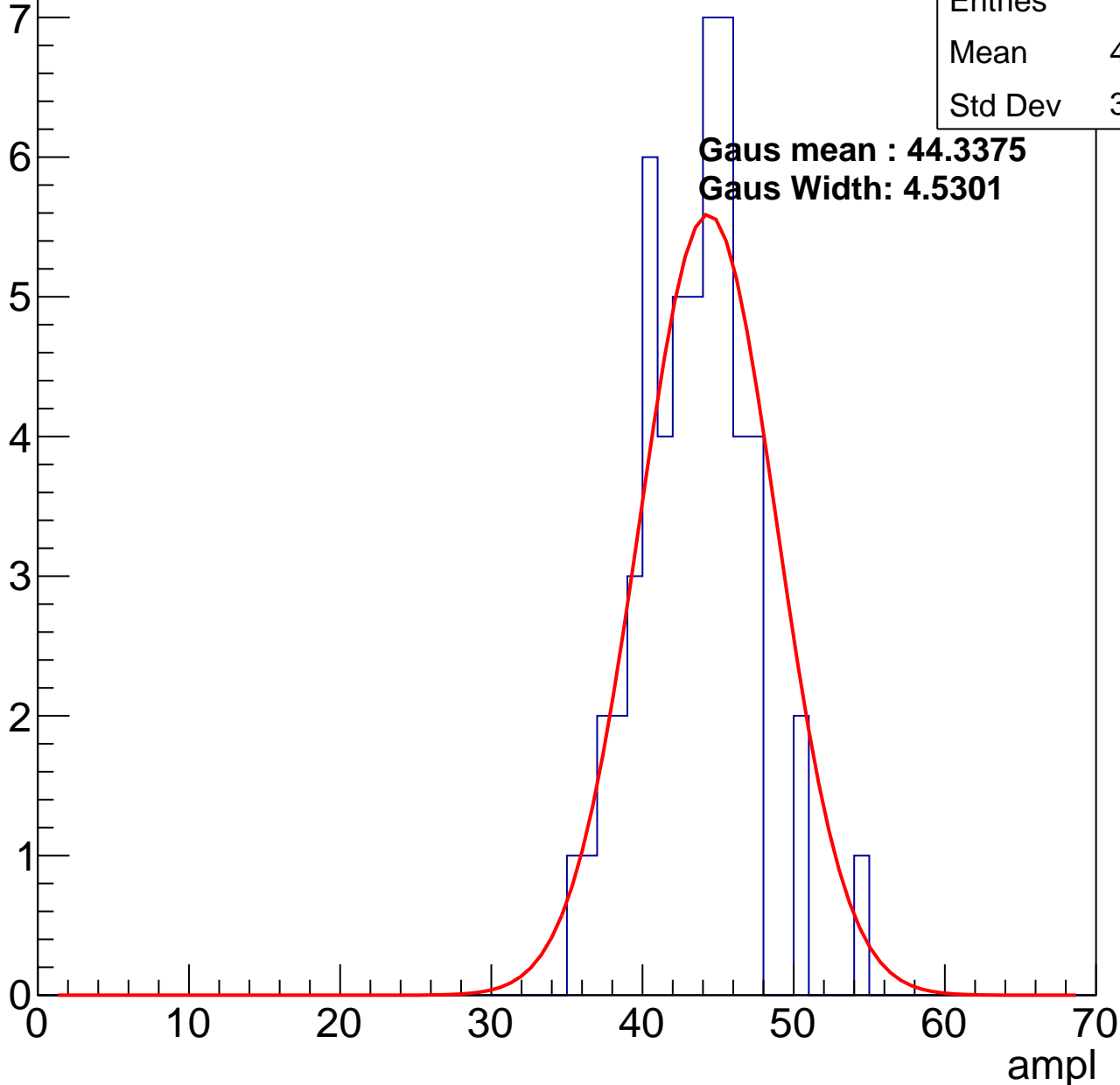
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	42.89
Std Dev	3.629

**Gaus mean : 44.3375**

**Gaus Width: 4.5301**

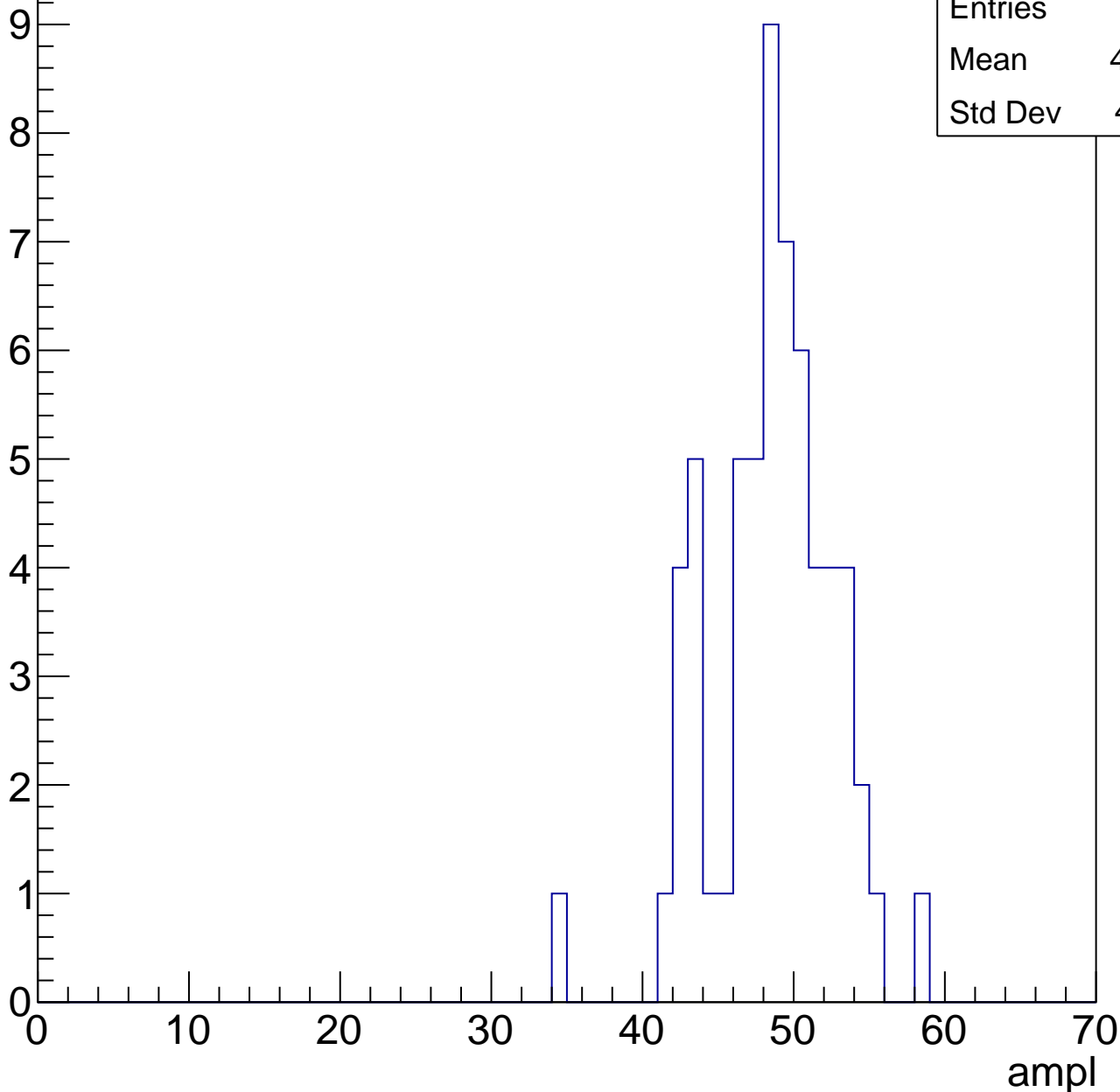


# B1L103S, U21-ch70, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	48.07
Std Dev	4.081

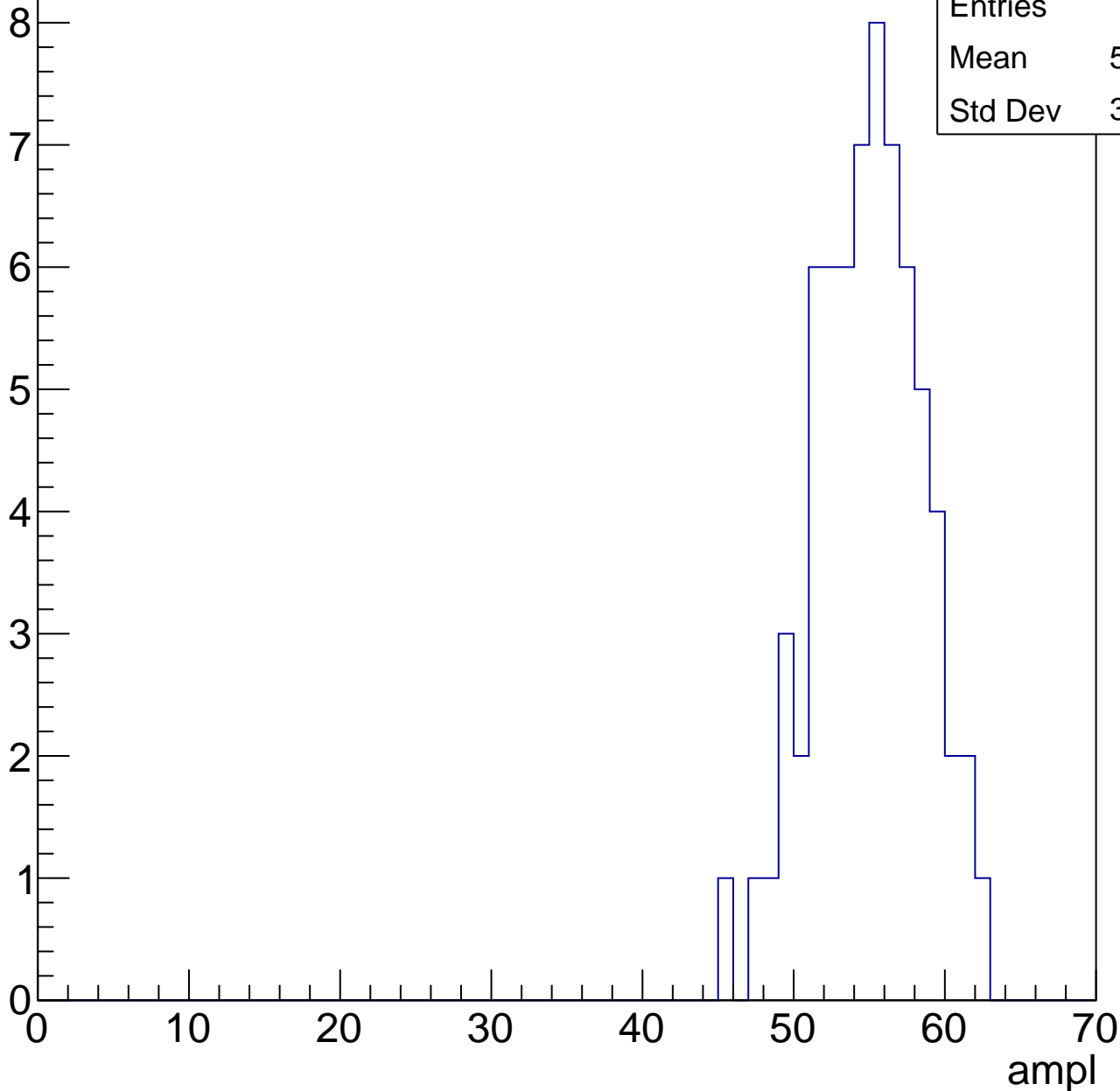


# B1L103S, U21-ch70, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

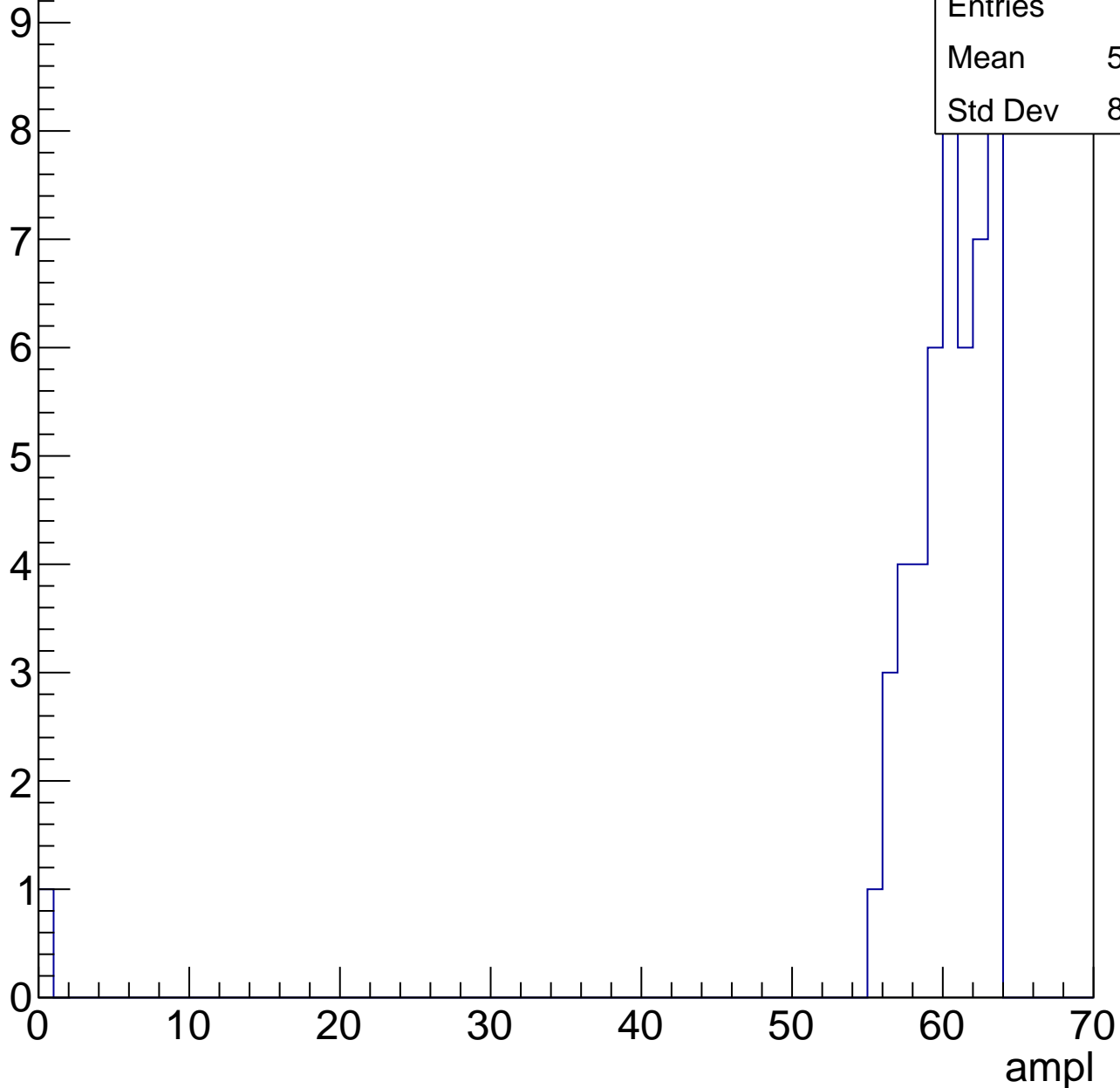
Entries	68
Mean	54.49
Std Dev	3.525



# B1L103S, U21-ch70, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U21-ch70, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	61.8
Std Dev	0.7483

ampl

0 10 20 30 40 50 60 70



# B1L103S, U21-ch70, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U21-ch71, adc0

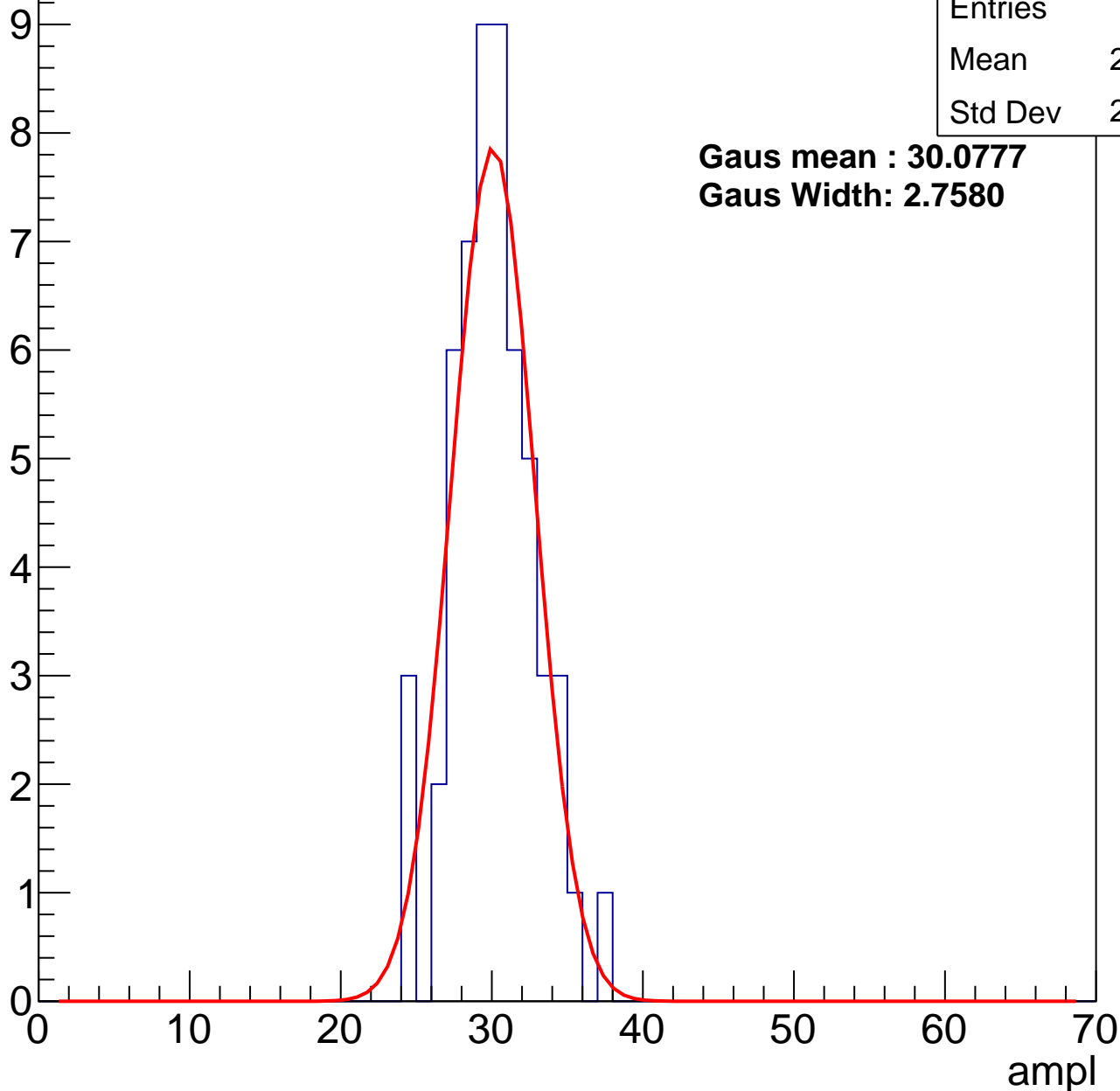
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	29.67
Std Dev	2.697

**Gaus mean : 30.0777**

**Gaus Width: 2.7580**



# B1L103S, U21-ch71, adc1

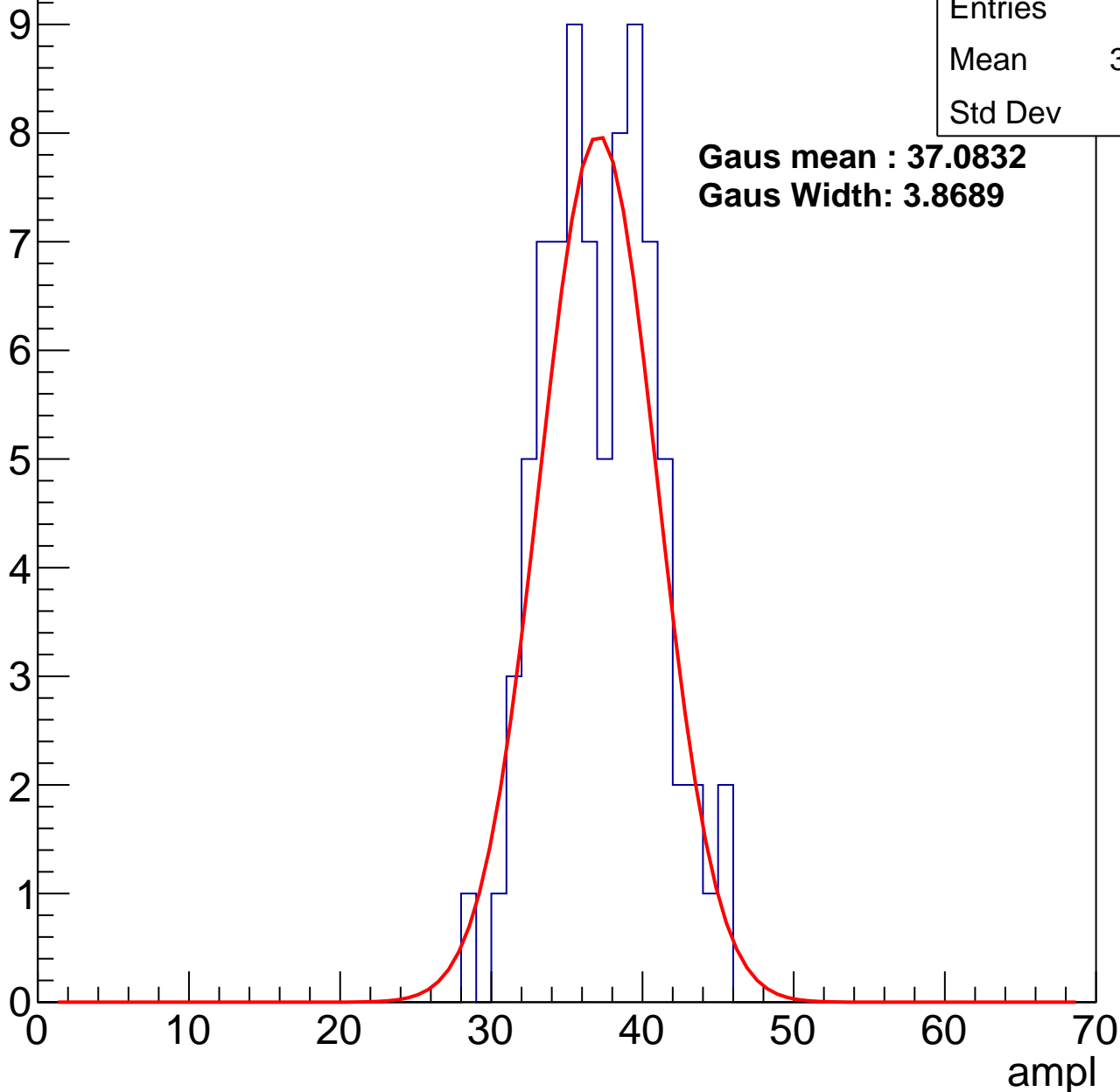
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	81
Mean	36.74
Std Dev	3.62

**Gaus mean : 37.0832**

**Gaus Width: 3.8689**



# B1L103S, U21-ch71, adc2

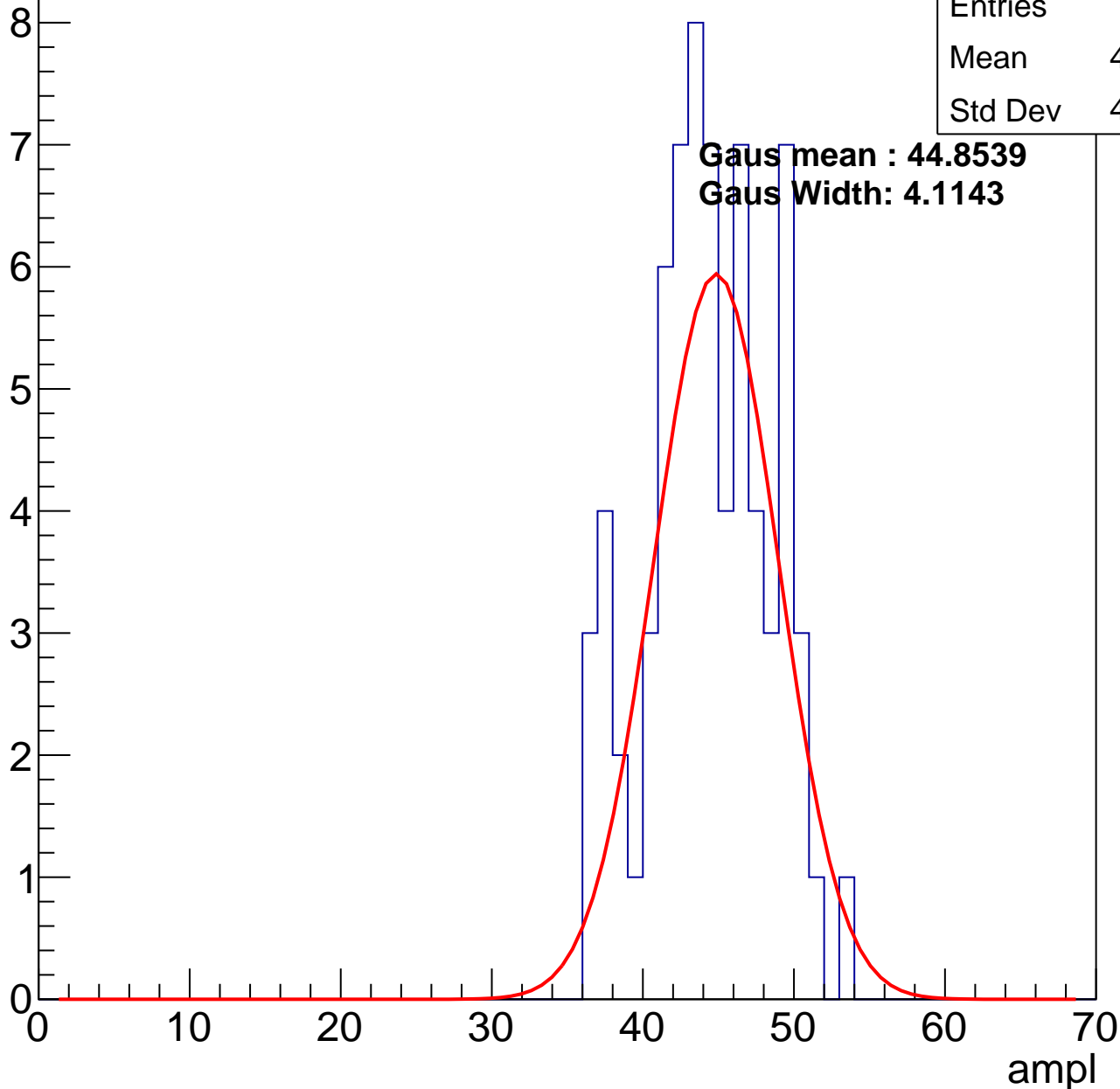
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	43.86
Std Dev	4.026

**Gaus mean : 44.8539**

**Gaus Width: 4.1143**

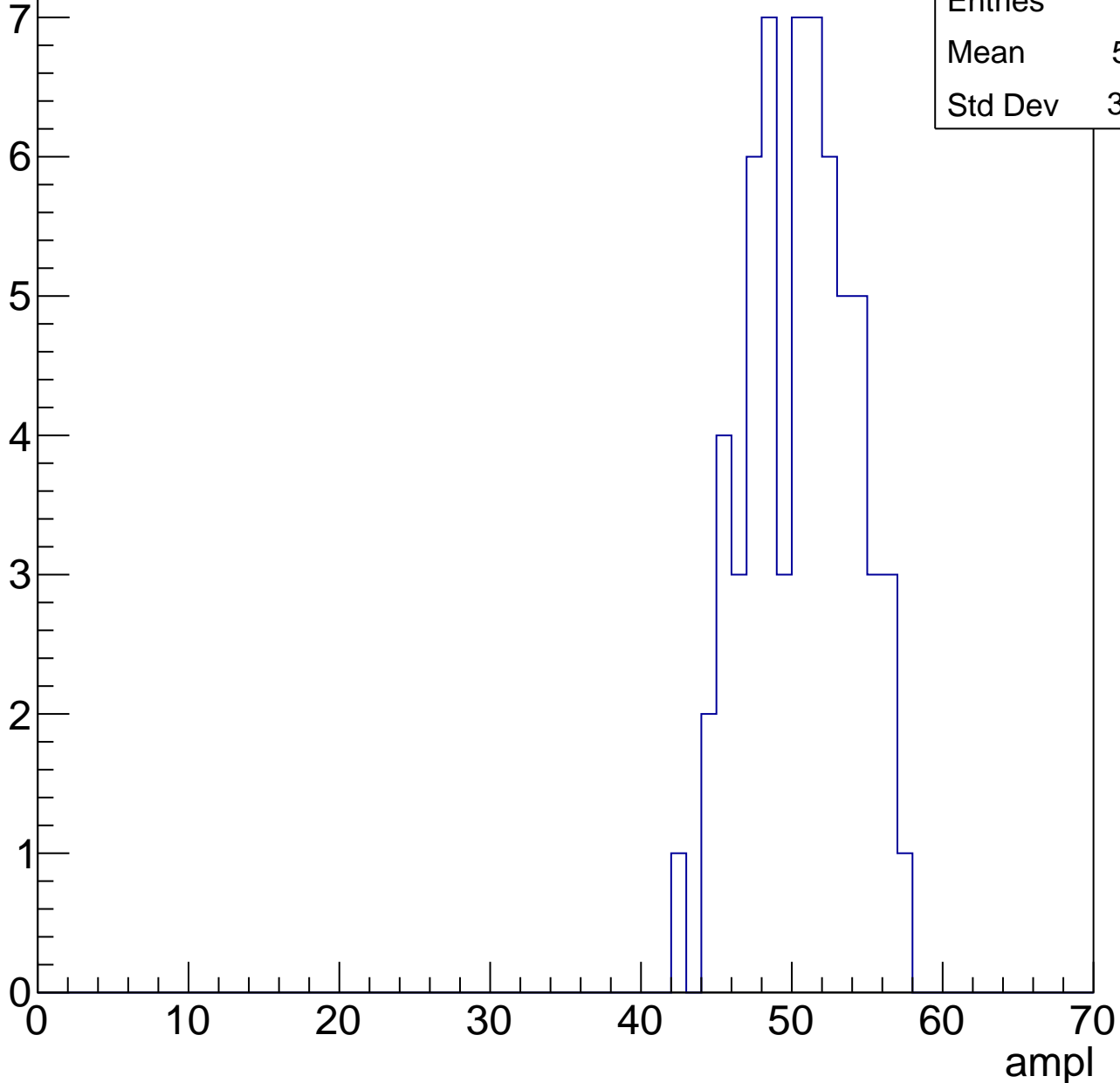


# B1L103S, U21-ch71, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

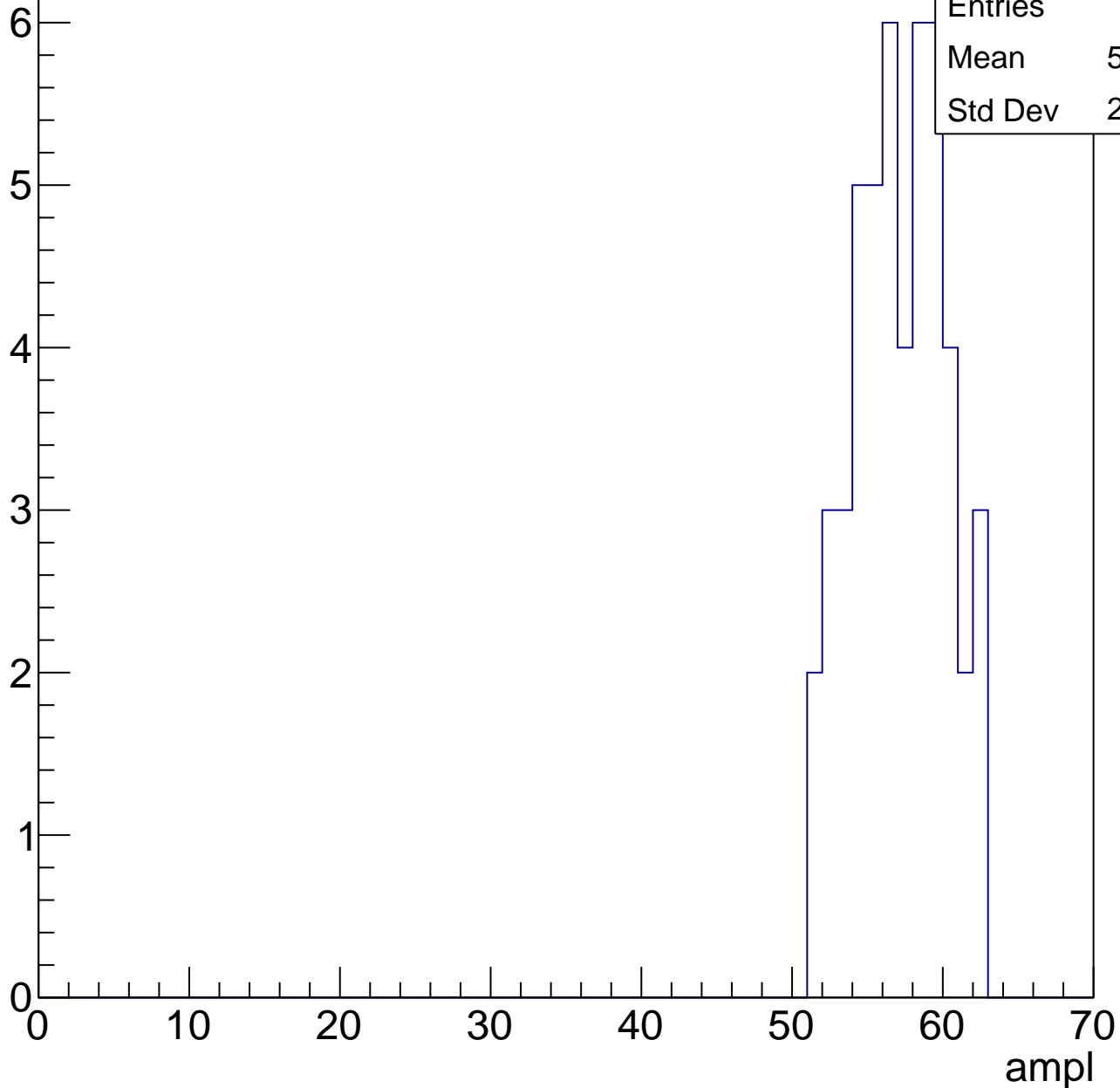
Entries	63
Mean	50.11
Std Dev	3.465



# B1L103S, U21-ch71, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



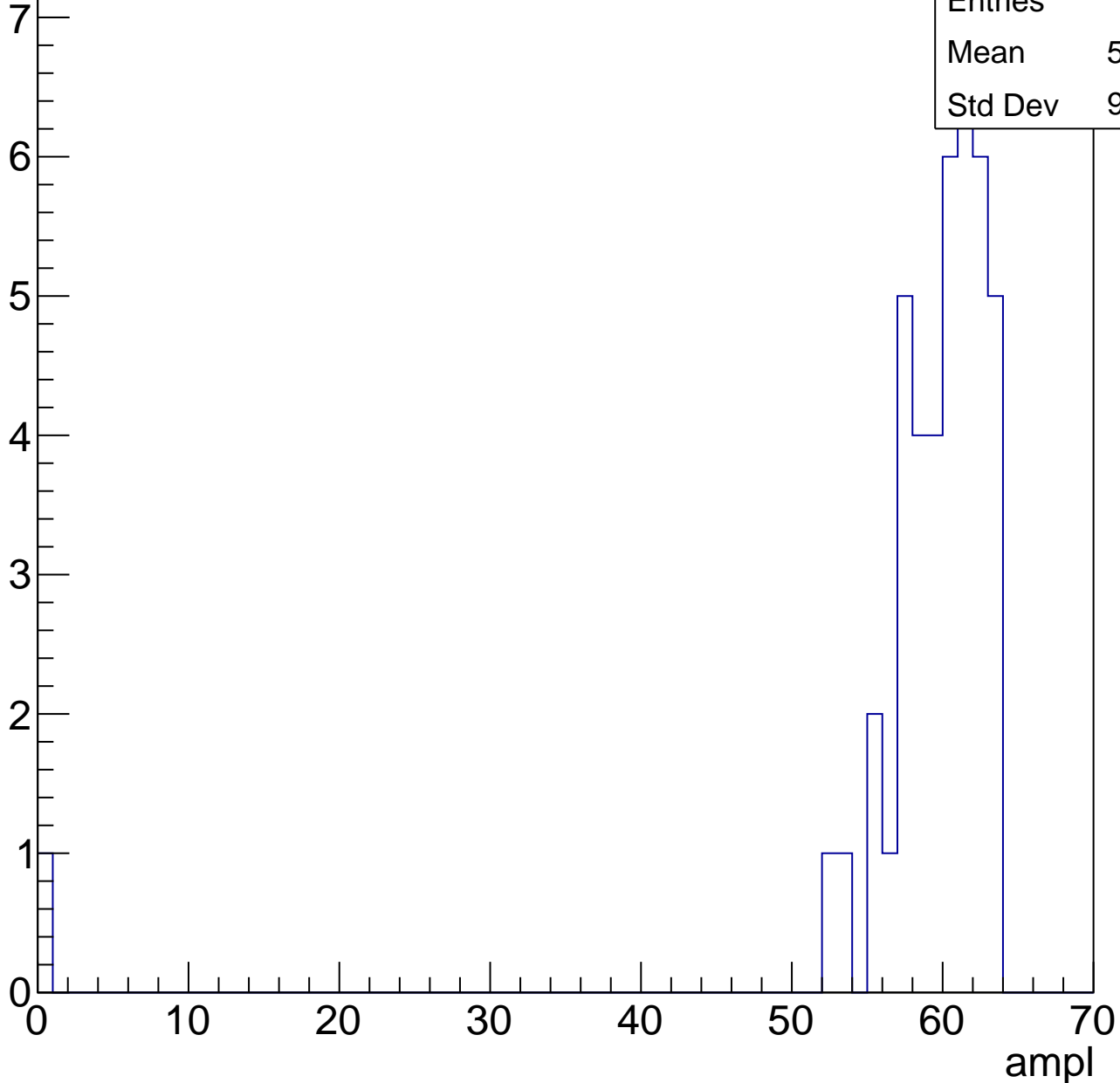
Entries	49
Mean	56.65
Std Dev	2.973

# B1L103S, U21-ch71, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	43
Mean	58.09
Std Dev	9.356

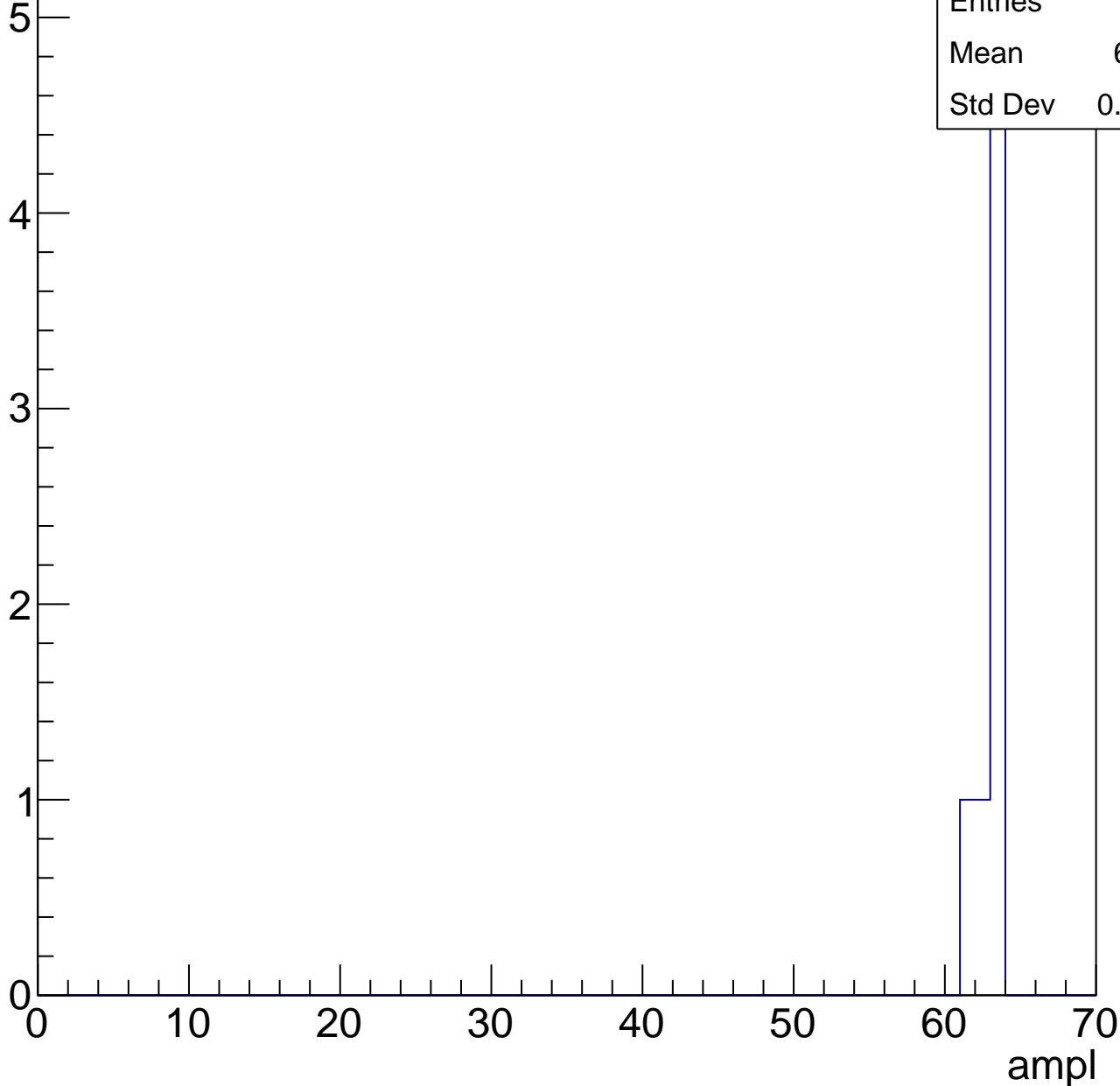


# B1L103S, U21-ch71, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	7
Mean	62.57
Std Dev	0.7284





# B1L103S, U21-ch71, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U21-ch72, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

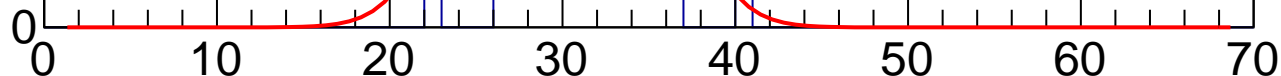
70

ampl

Entries	64
Mean	30.39
Std Dev	3.141

**Gaus mean : 30.0742**

**Gaus Width: 4.0152**



# B1L103S, U21-ch72, adc1

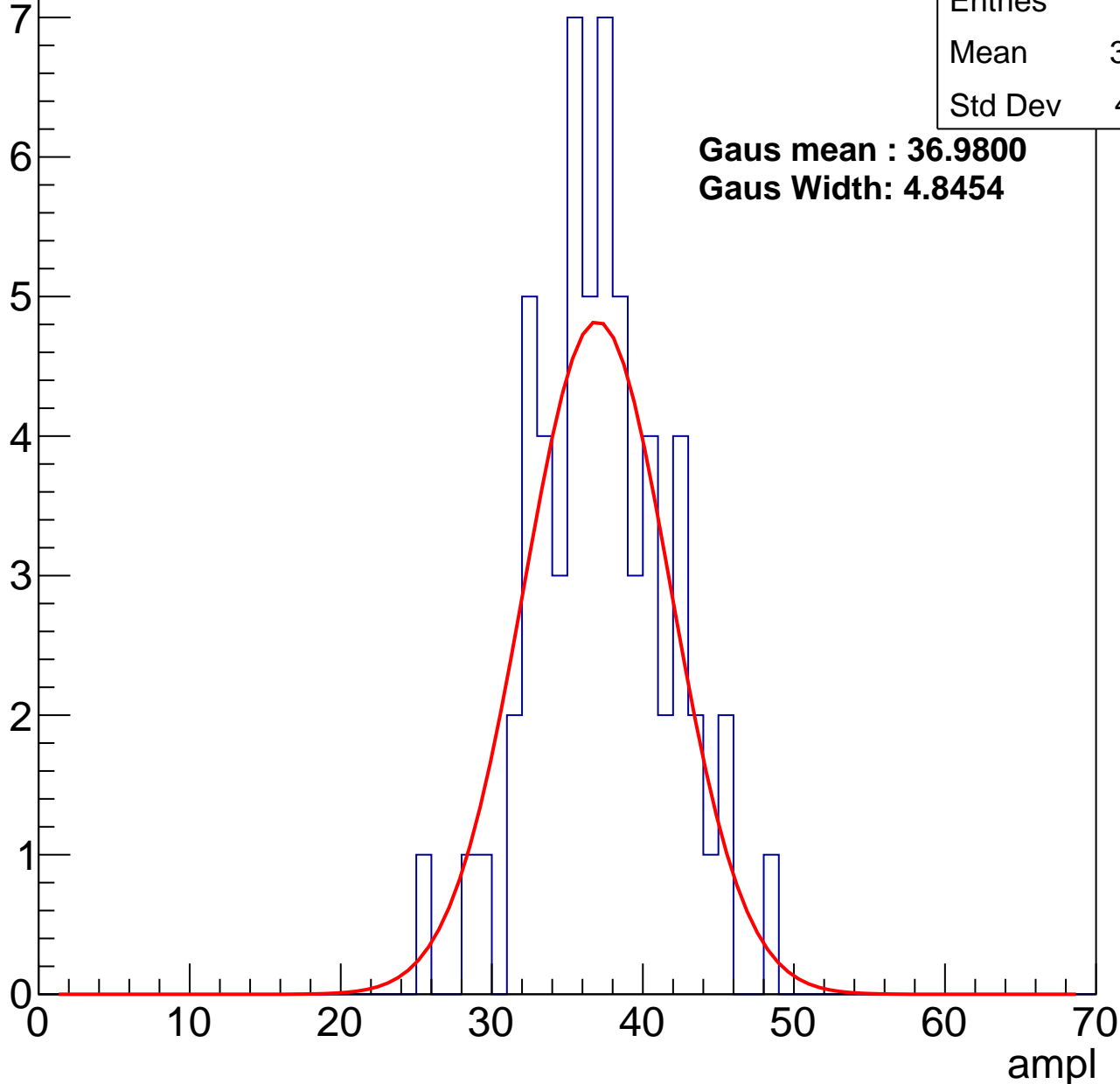
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	36.78
Std Dev	4.401

**Gaus mean : 36.9800**

**Gaus Width: 4.8454**



# B1L103S, U21-ch72, adc2

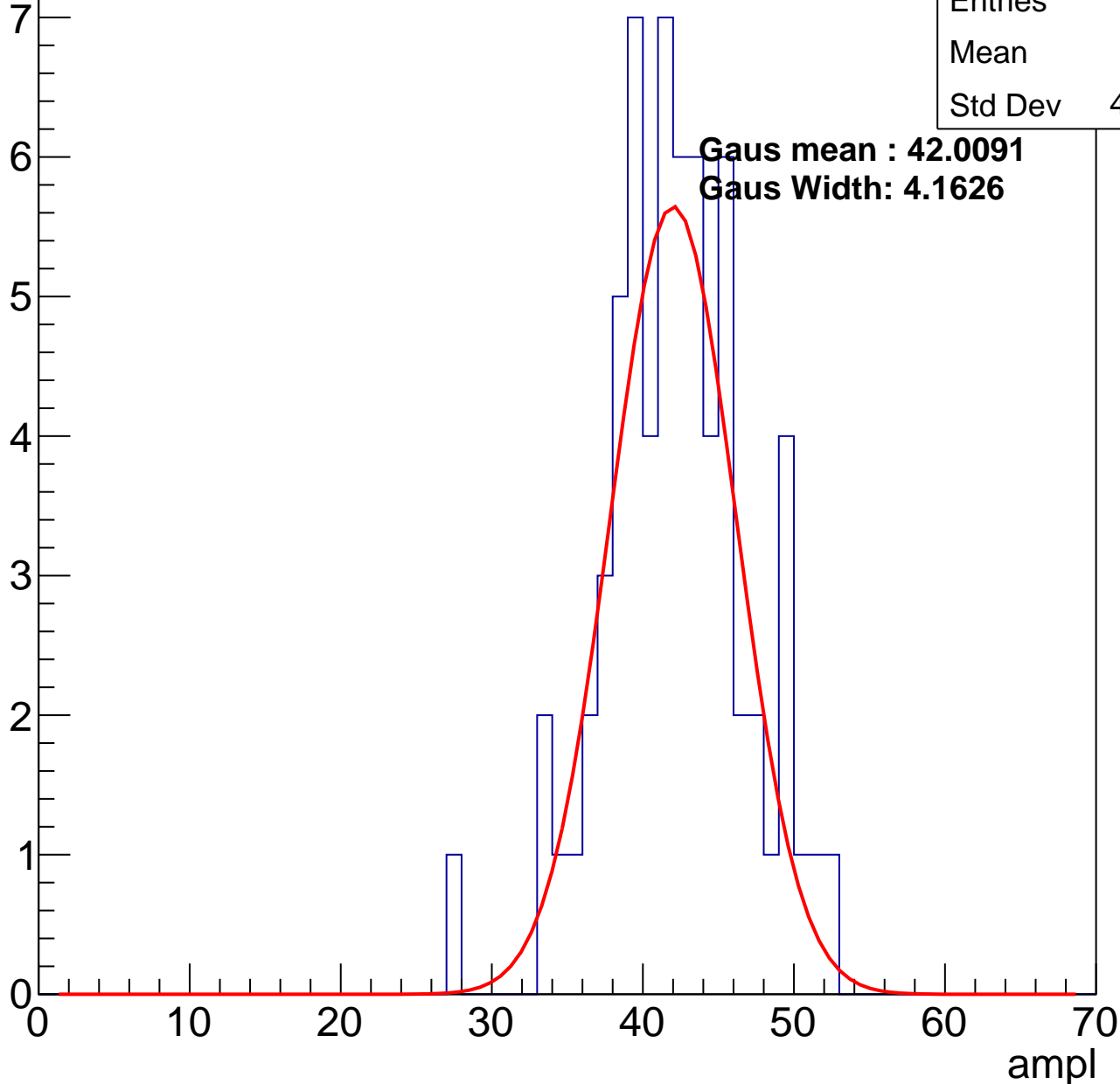
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	41.7
Std Dev	4.639

Gaus mean : 42.0091

Gaus Width: 4.1626

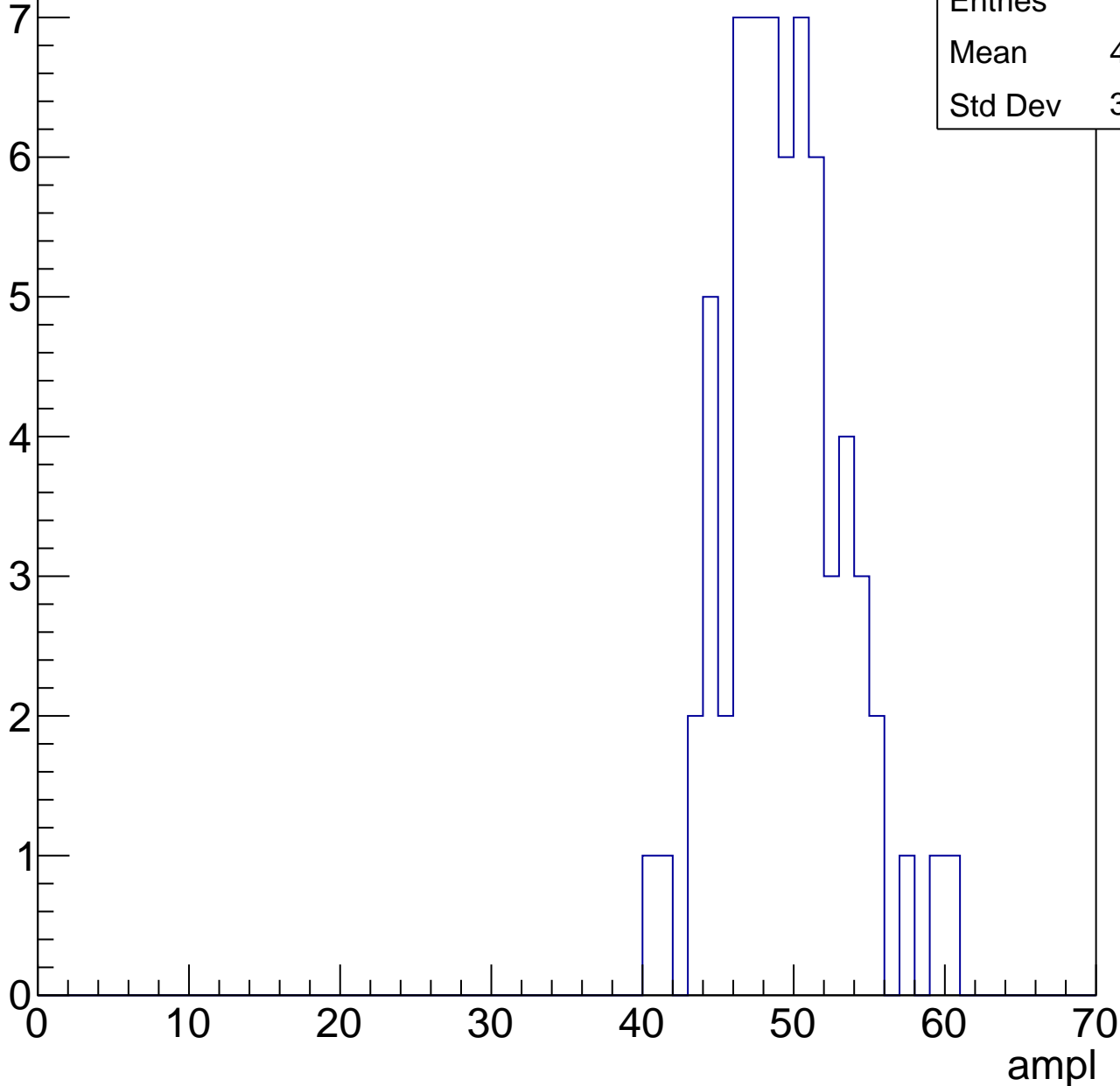


# B1L103S, U21-ch72, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	48.94
Std Dev	3.942

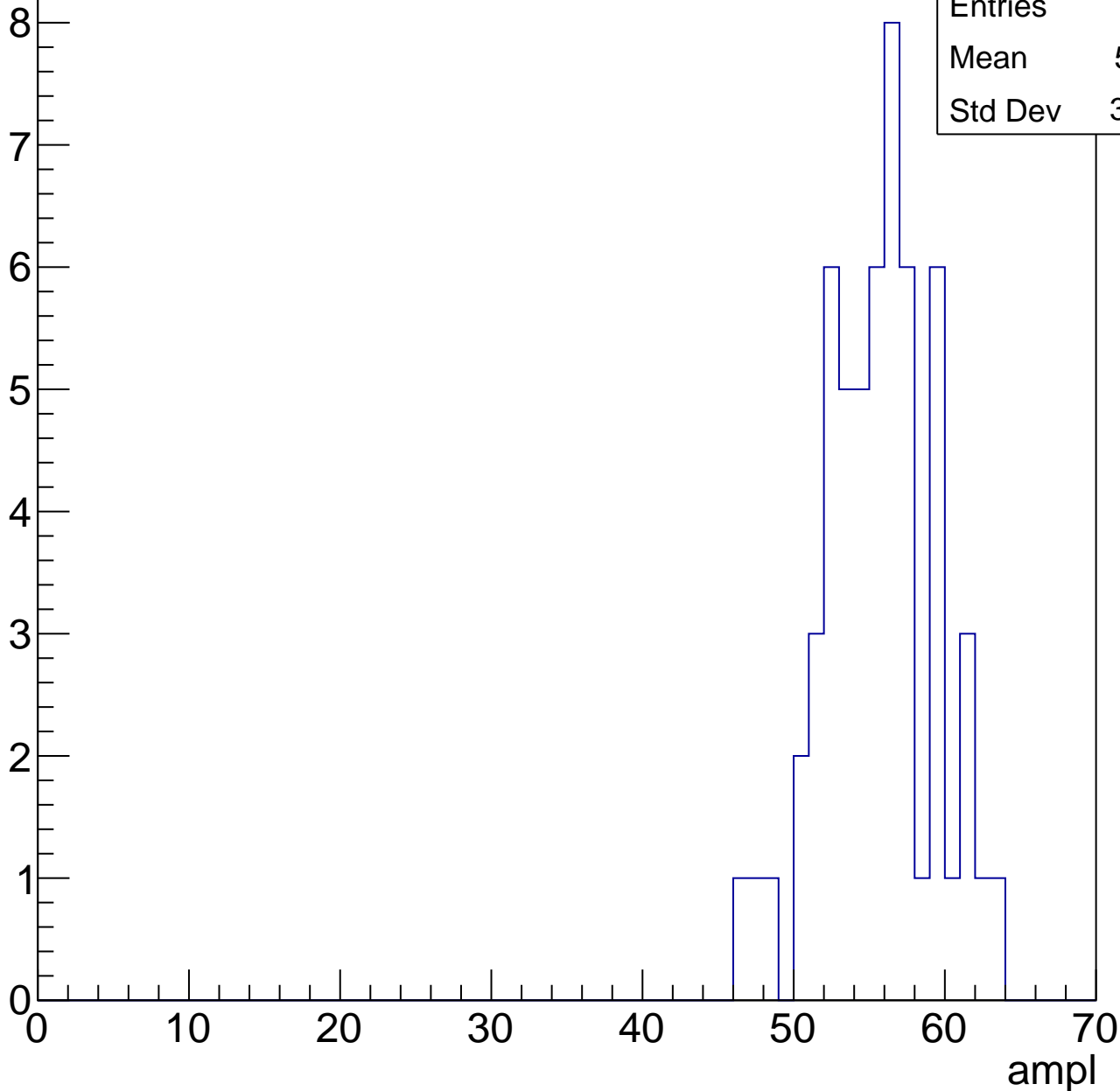


# B1L103S, U21-ch72, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	55.11
Std Dev	3.636

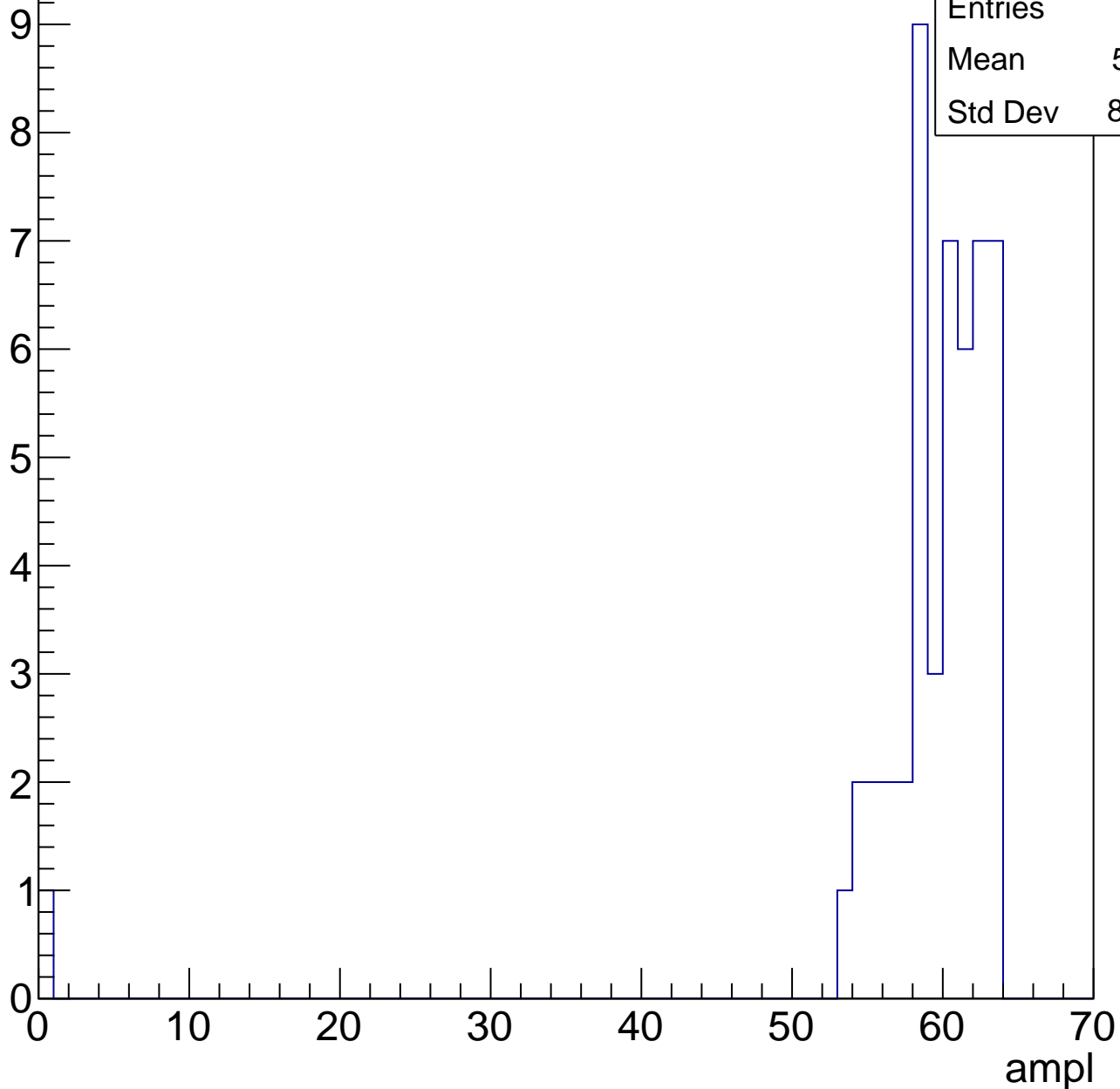


# B1L103S, U21-ch72, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	58.31
Std Dev	8.825



# B1L103S, U21-ch72, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

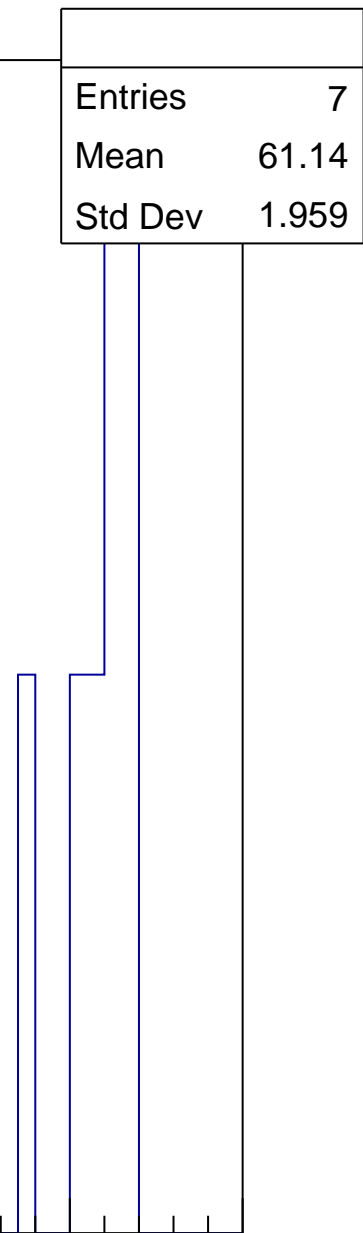
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	7
Mean	61.14
Std Dev	1.959

ampl

0 10 20 30 40 50 60 70





# B1L103S, U21-ch72, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L103S, U21-ch73, adc0

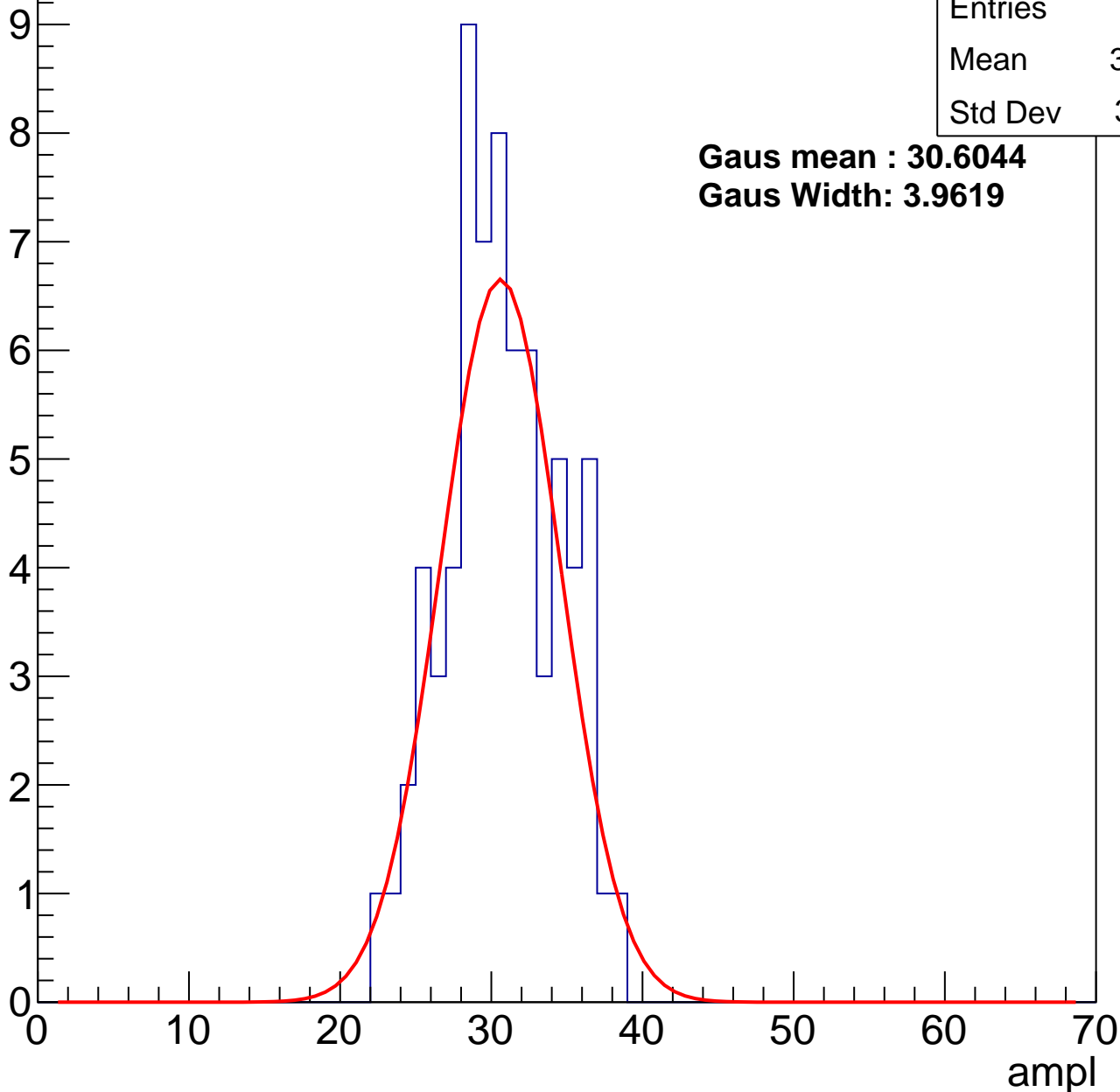
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	30.23
Std Dev	3.661

**Gaus mean : 30.6044**

**Gaus Width: 3.9619**



# B1L103S, U21-ch73, adc1

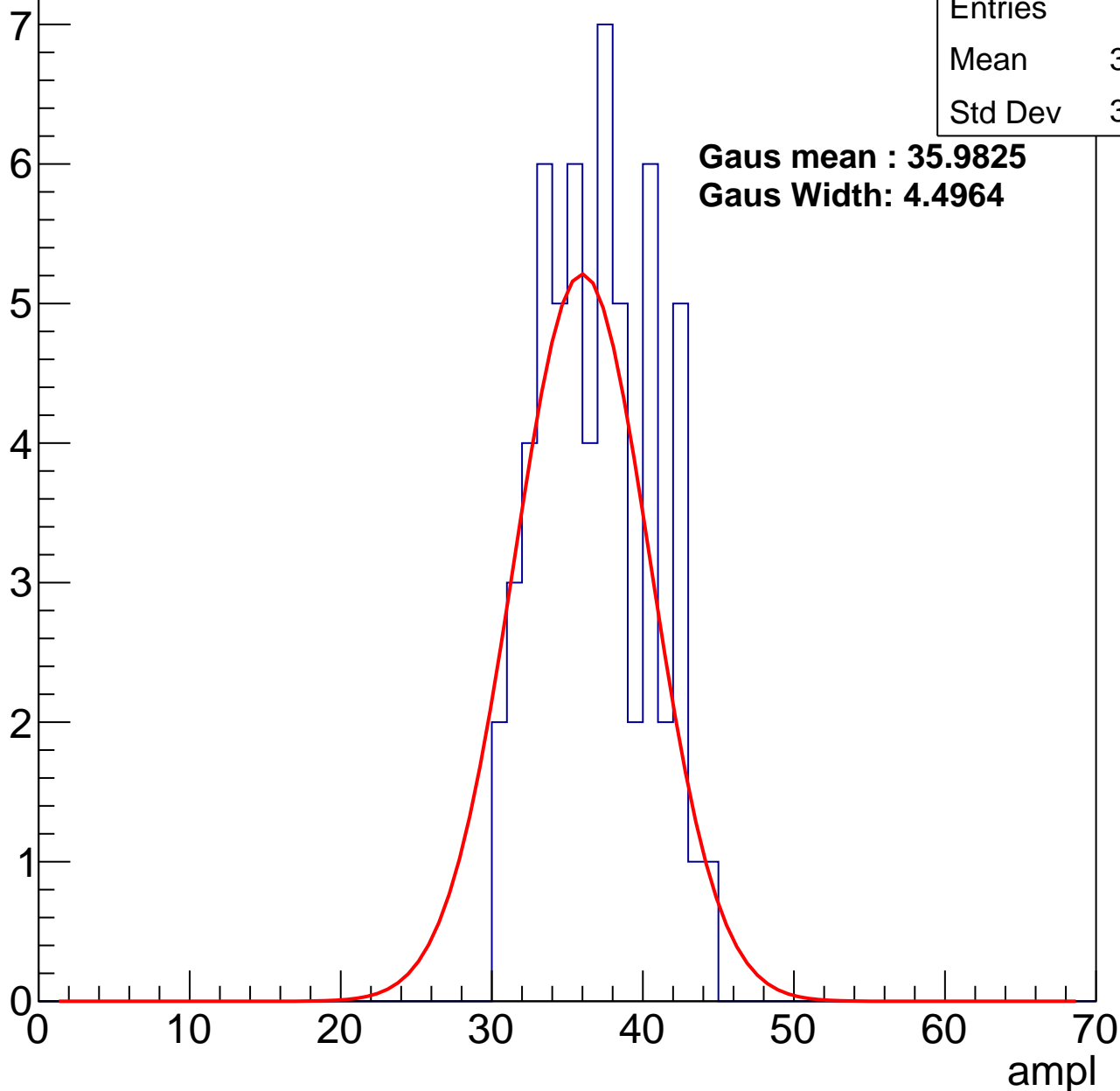
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	36.42
Std Dev	3.599

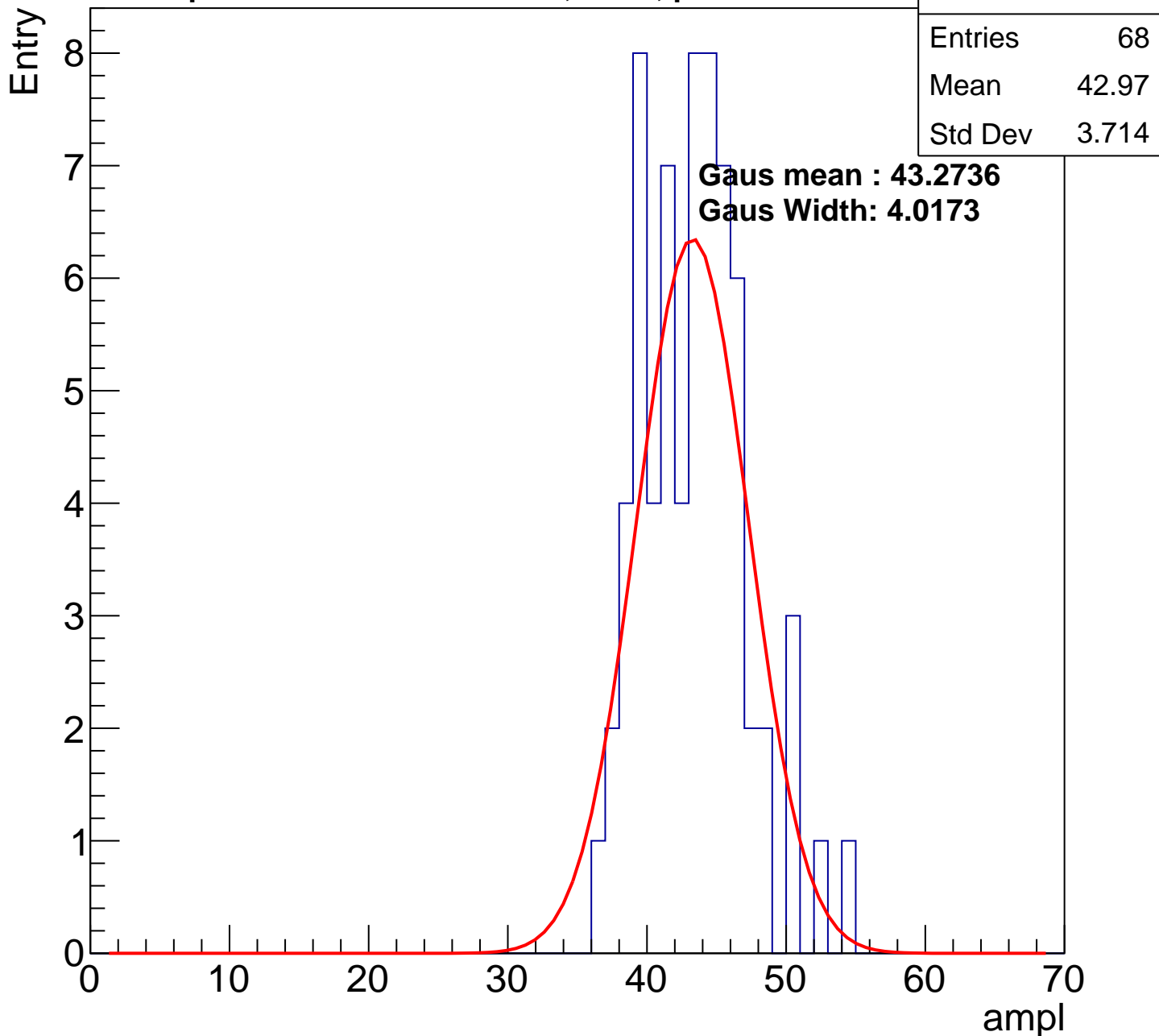
**Gaus mean : 35.9825**

**Gaus Width: 4.4964**



# B1L103S, U21-ch73, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

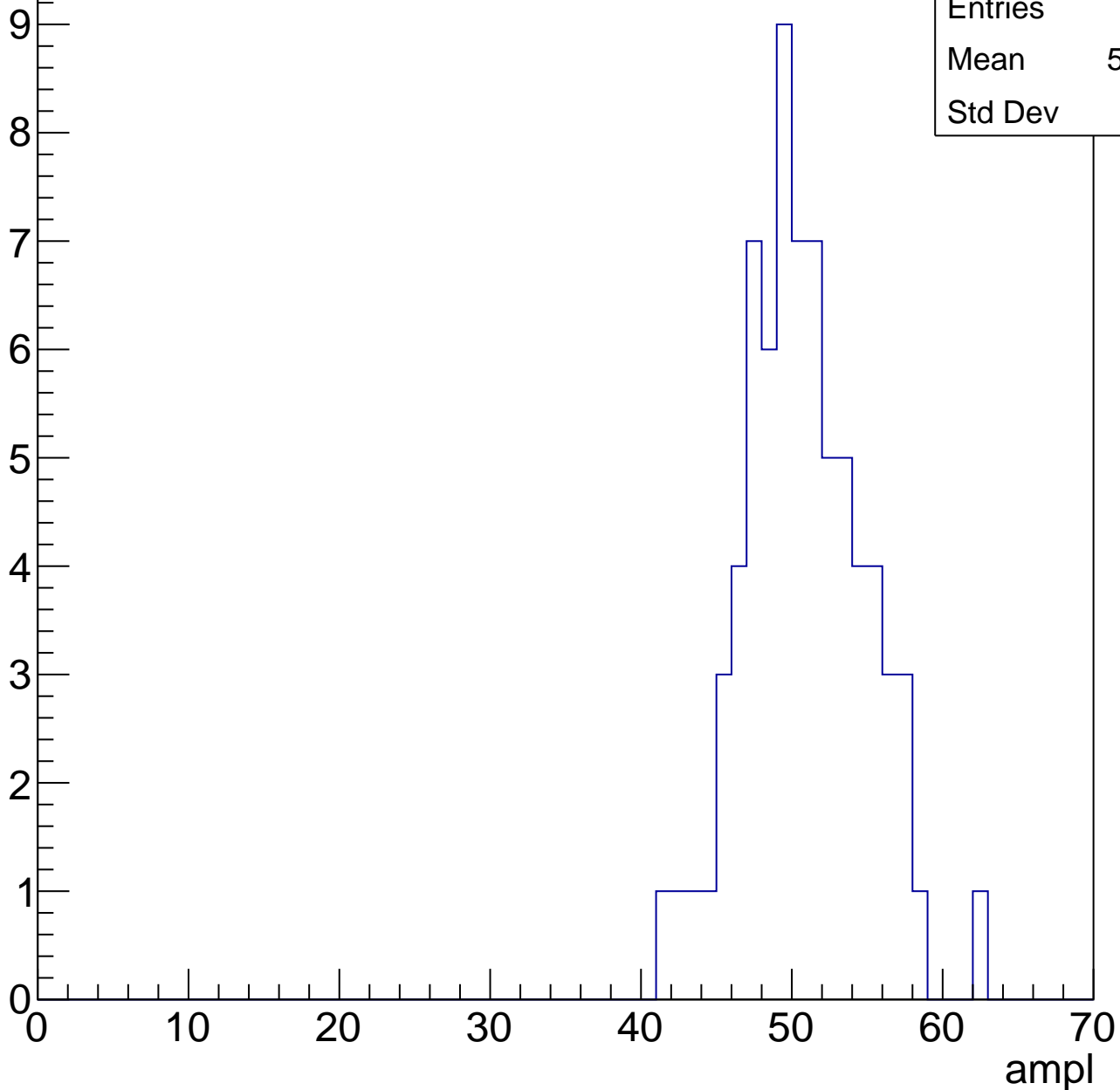


# B1L103S, U21-ch73, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	50.33
Std Dev	3.98

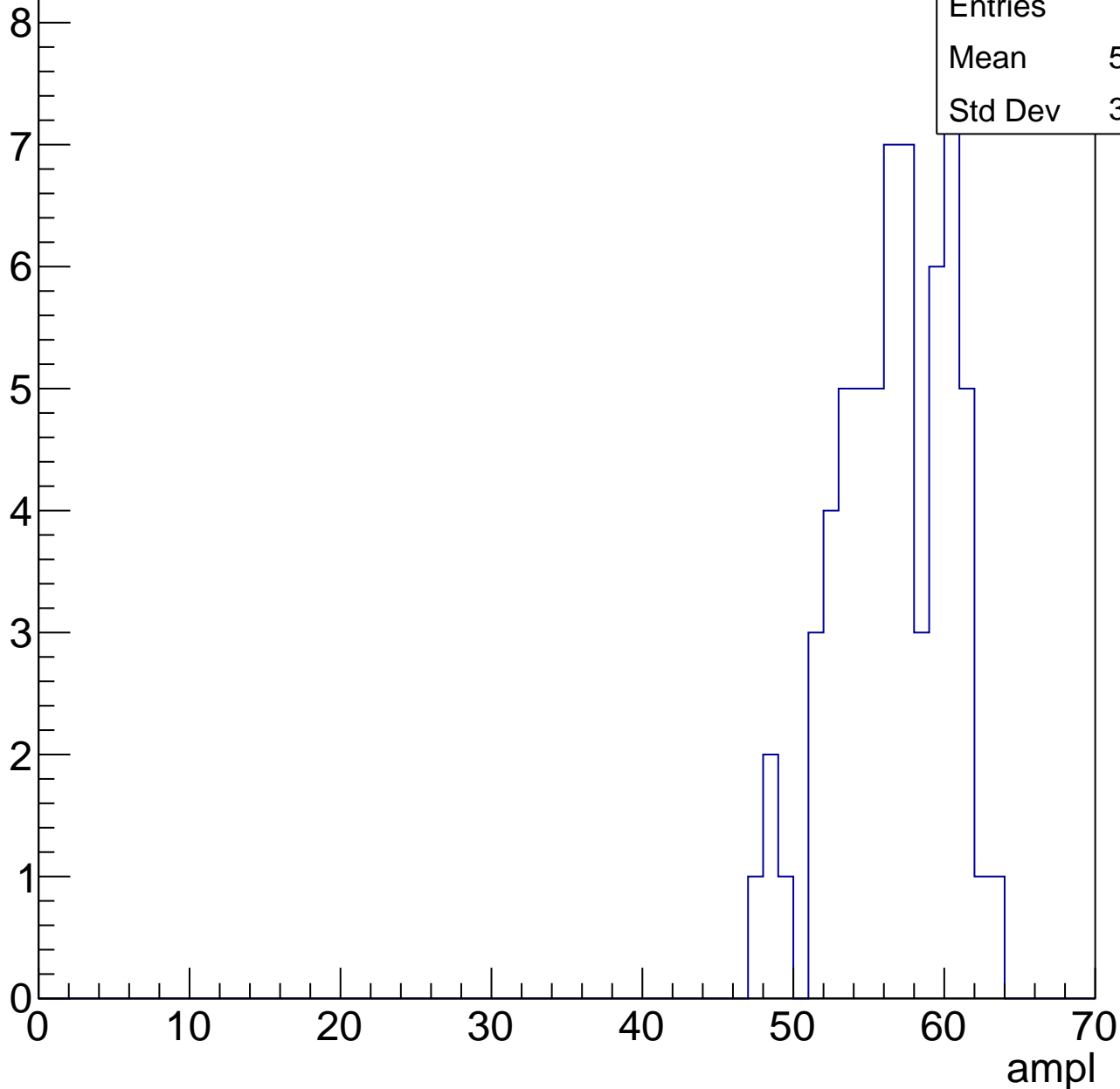


# B1L103S, U21-ch73, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	56.12
Std Dev	3.702

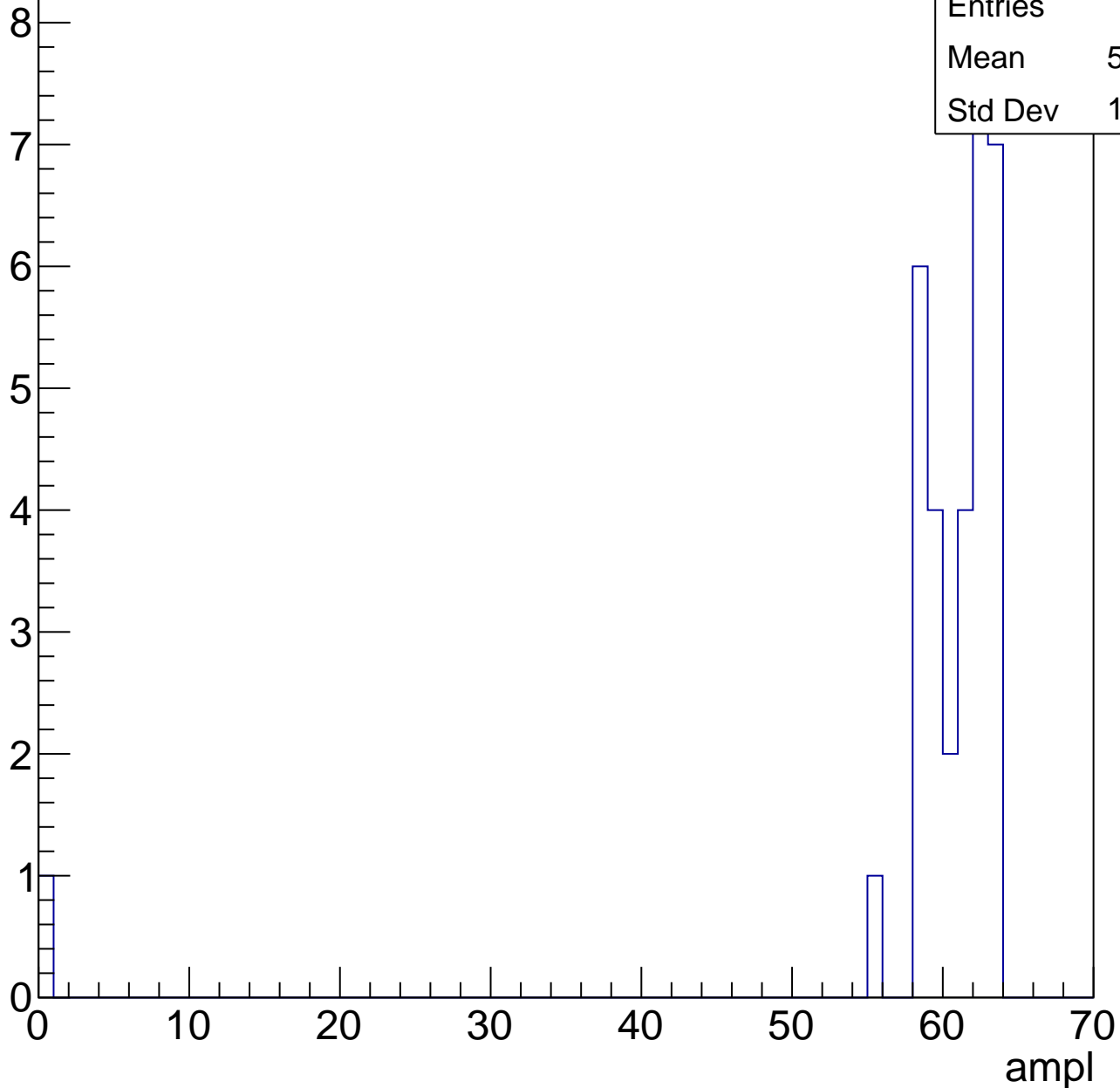


# B1L103S, U21-ch73, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	33
Mean	58.79
Std Dev	10.59



# B1L103S, U21-ch73, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U21-ch73, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U21-ch74, adc0

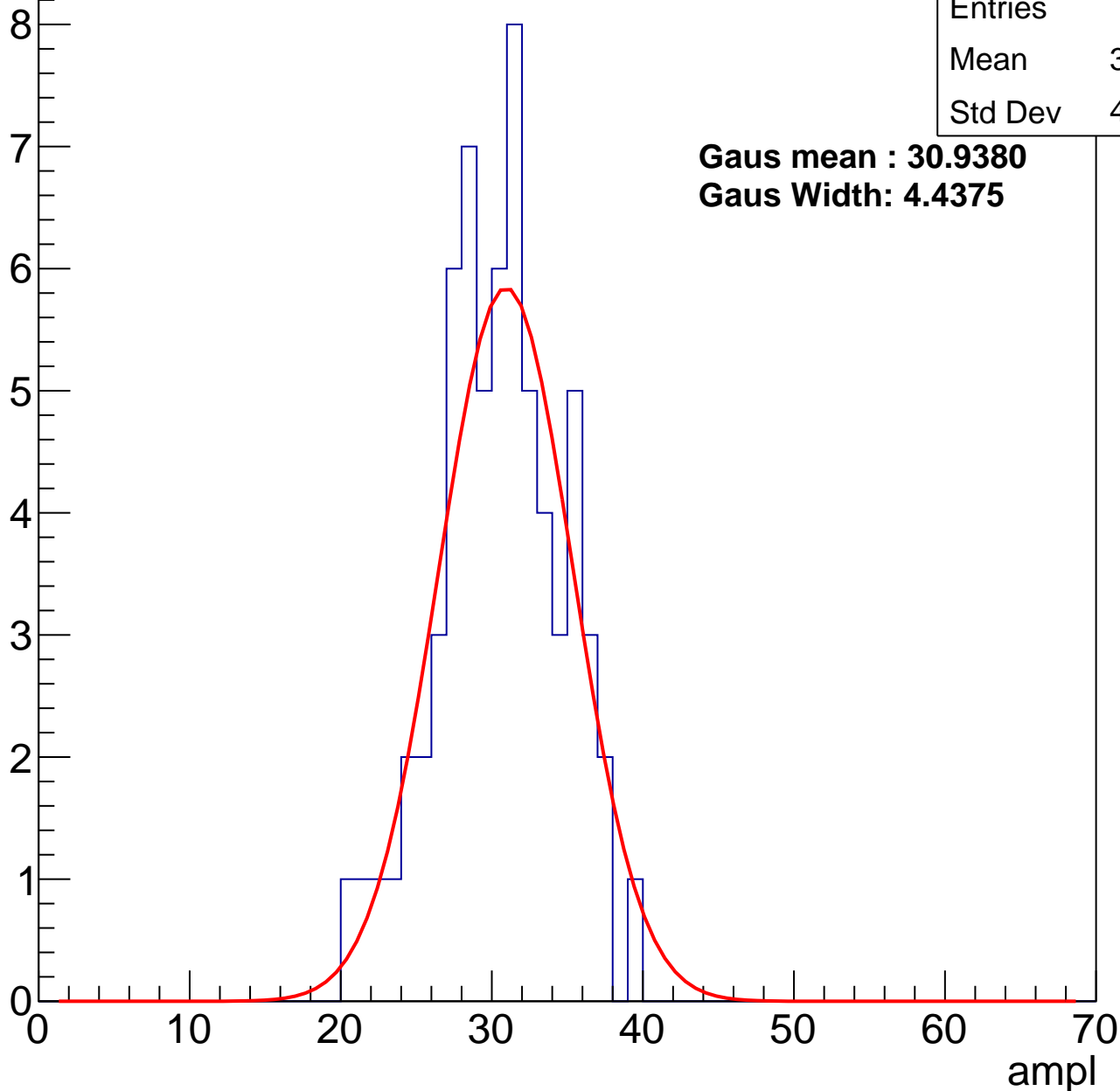
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	30.05
Std Dev	4.036

**Gaus mean : 30.9380**

**Gaus Width: 4.4375**



# B1L103S, U21-ch74, adc1

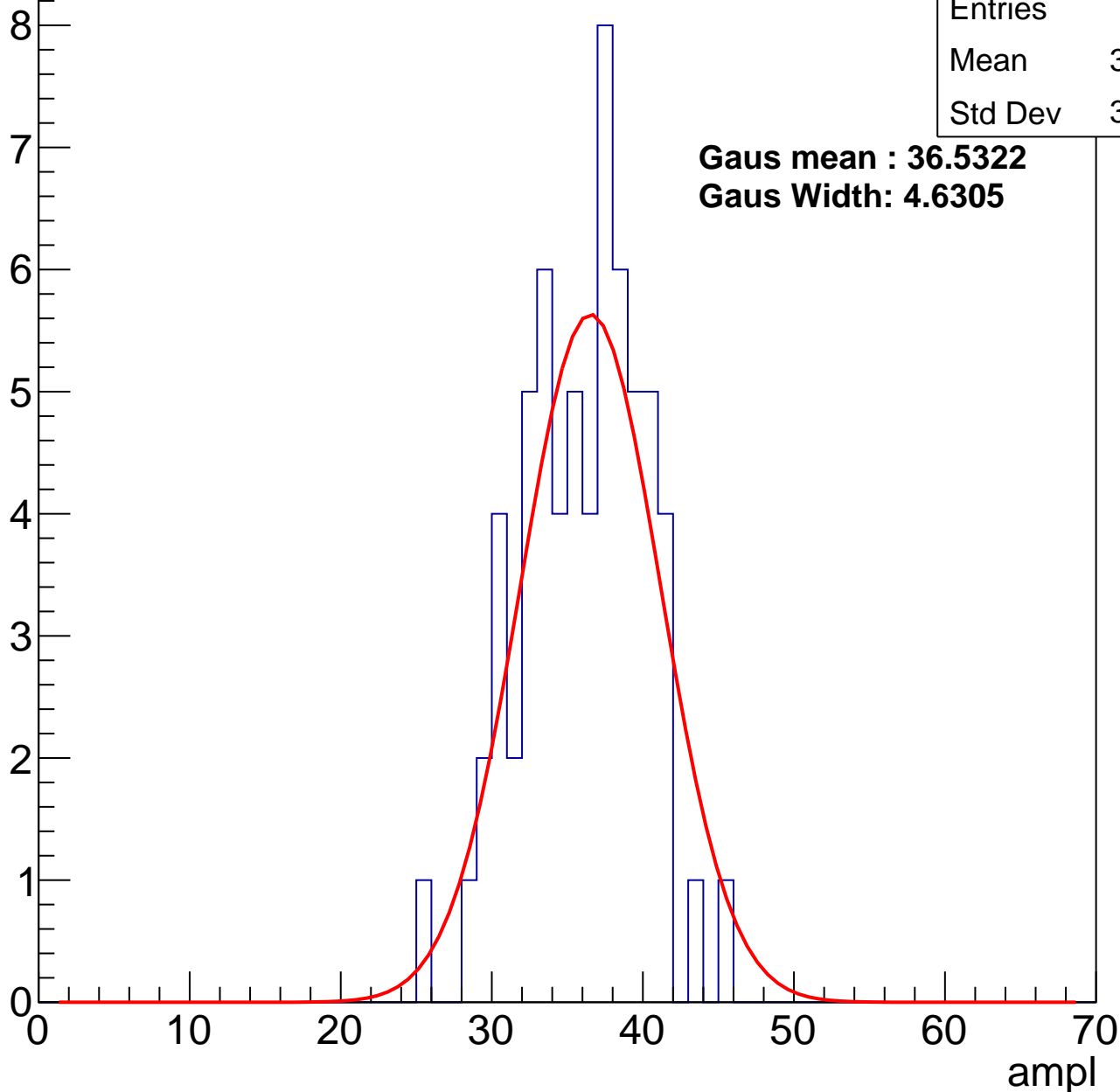
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	35.58
Std Dev	3.968

**Gaus mean : 36.5322**

**Gaus Width: 4.6305**



# B1L103S, U21-ch74, adc2

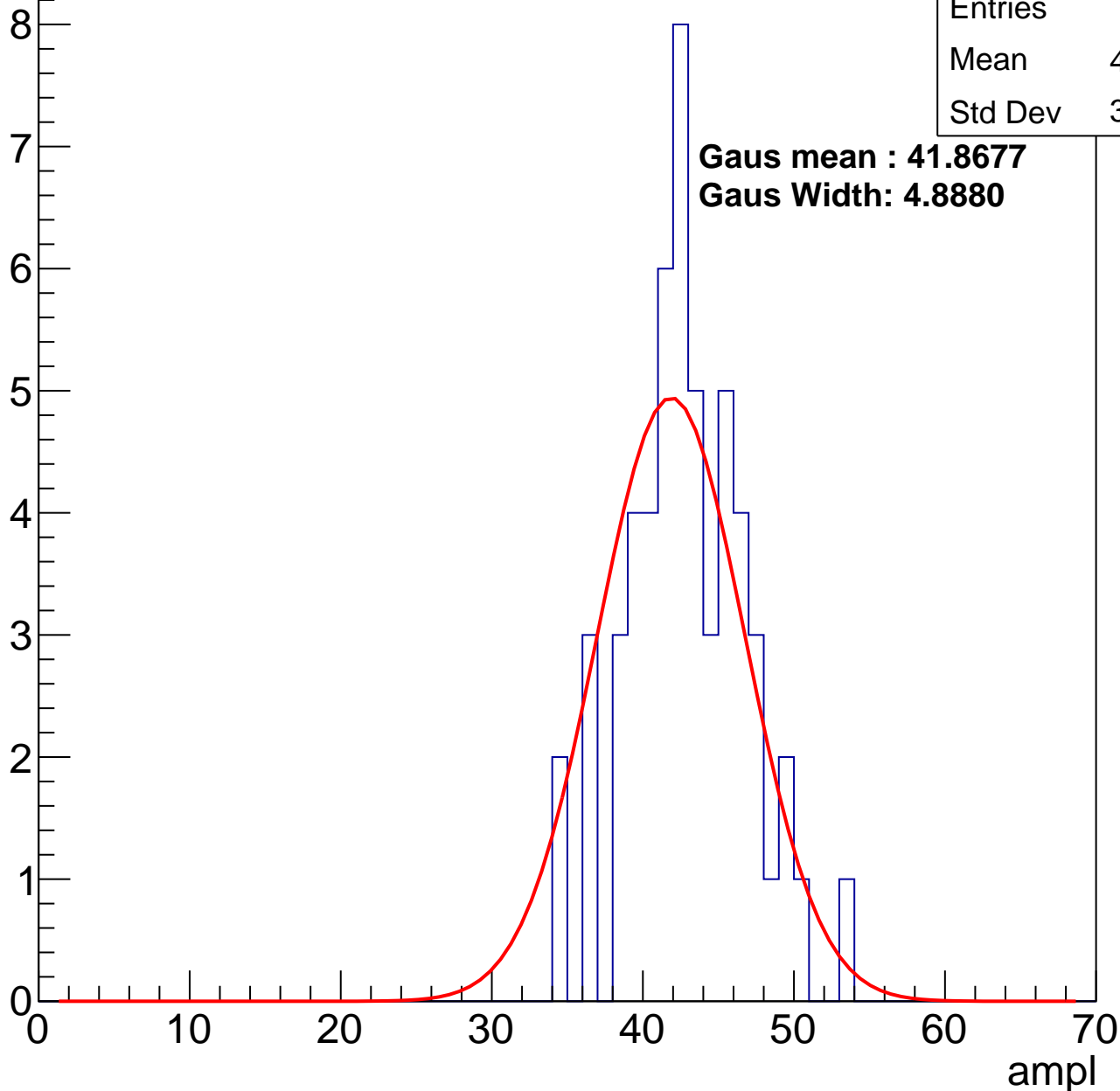
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	42.44
Std Dev	3.935

**Gaus mean : 41.8677**

**Gaus Width: 4.8880**

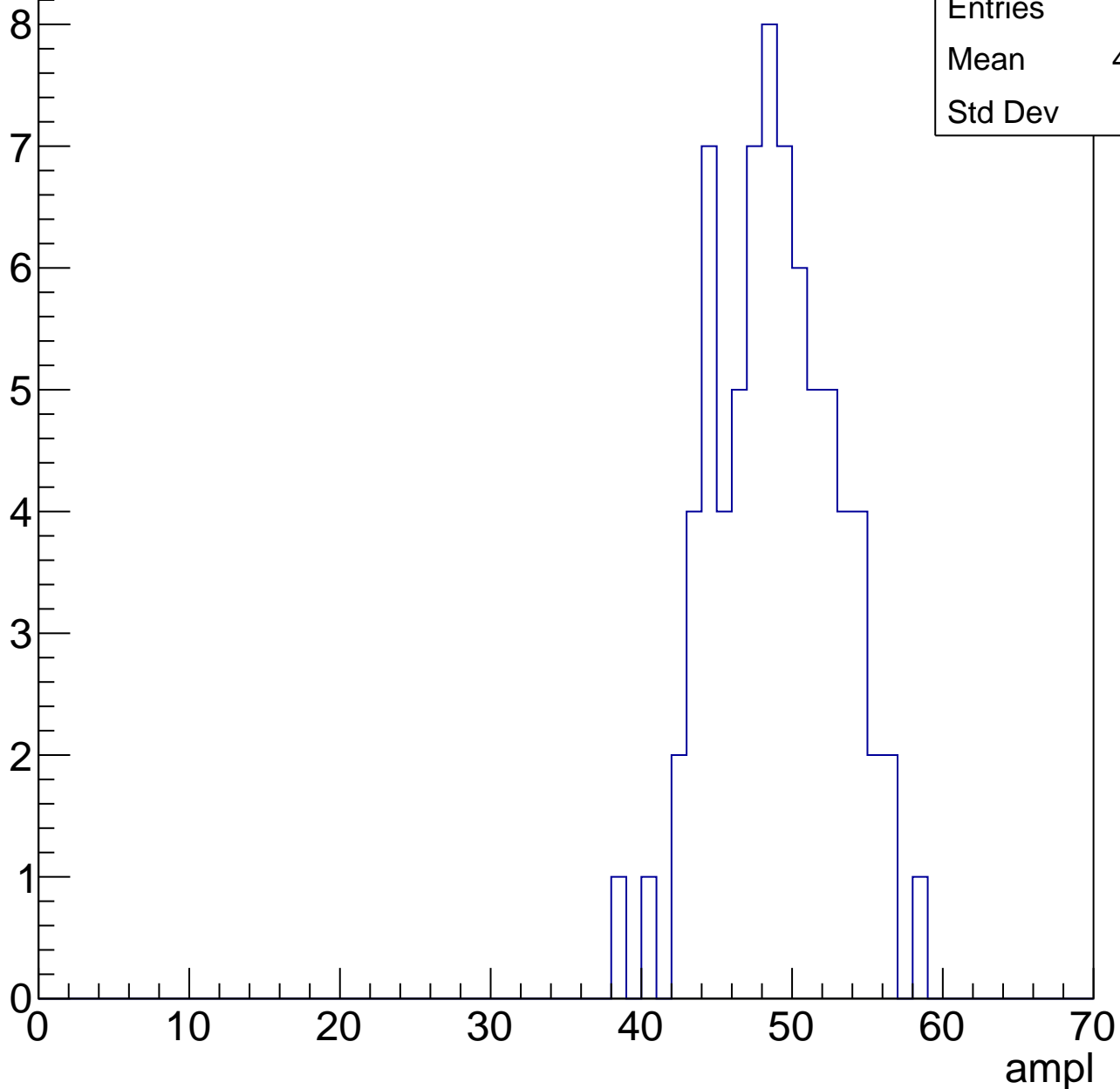


# B1L103S, U21-ch74, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	48.41
Std Dev	4.04

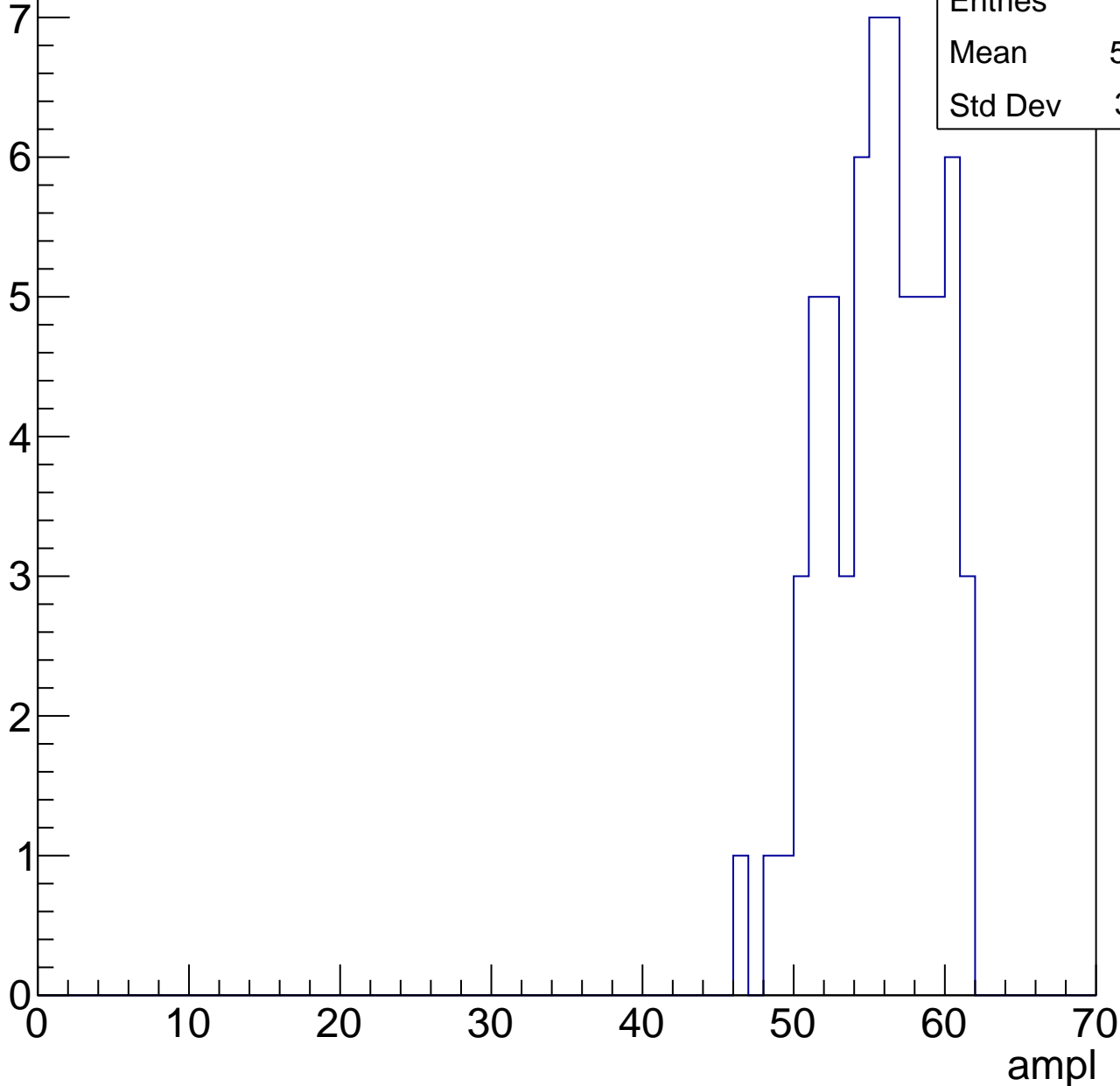


# B1L103S, U21-ch74, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	55.25
Std Dev	3.541

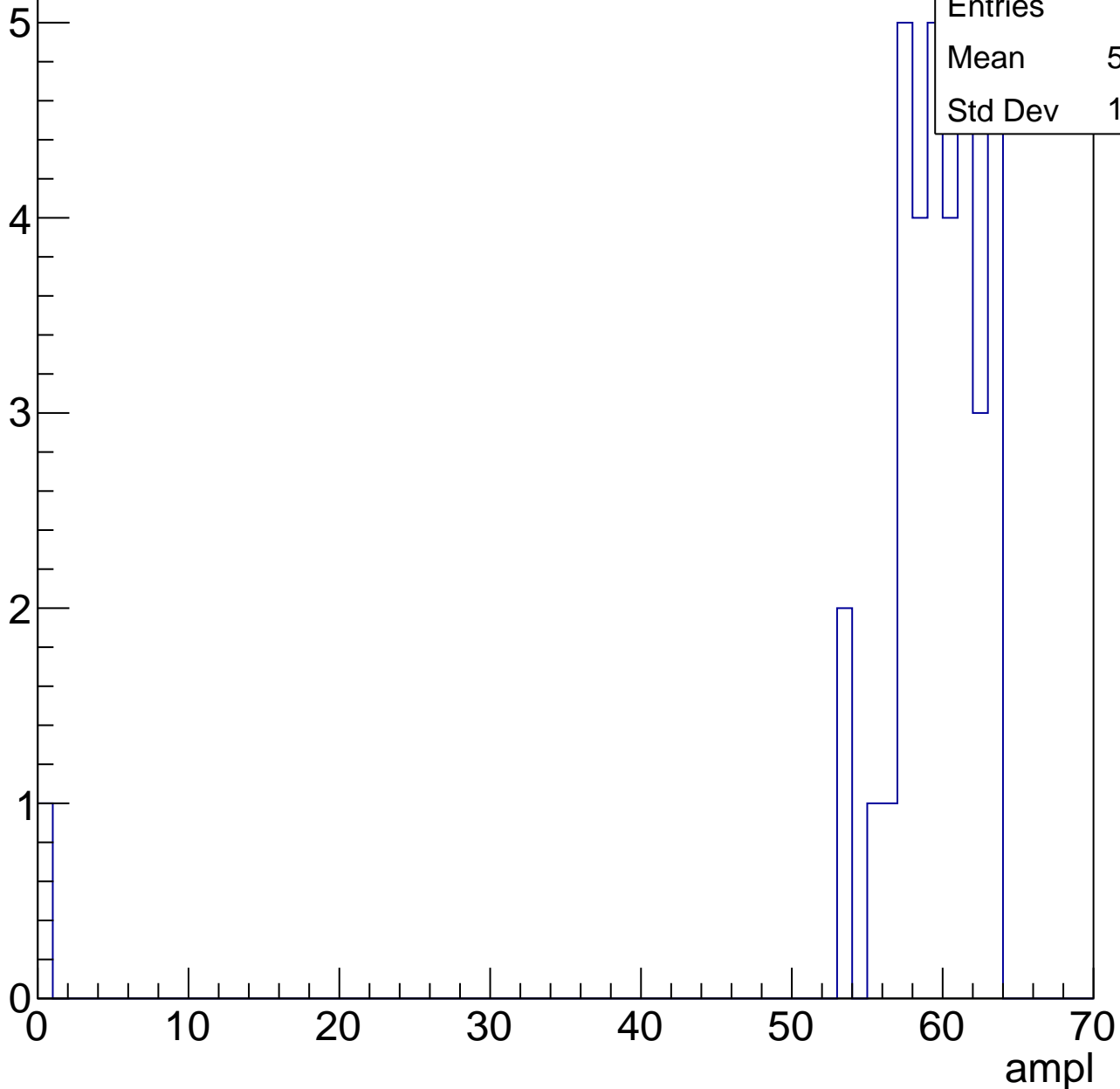


# B1L103S, U21-ch74, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	36
Mean	57.64
Std Dev	10.09

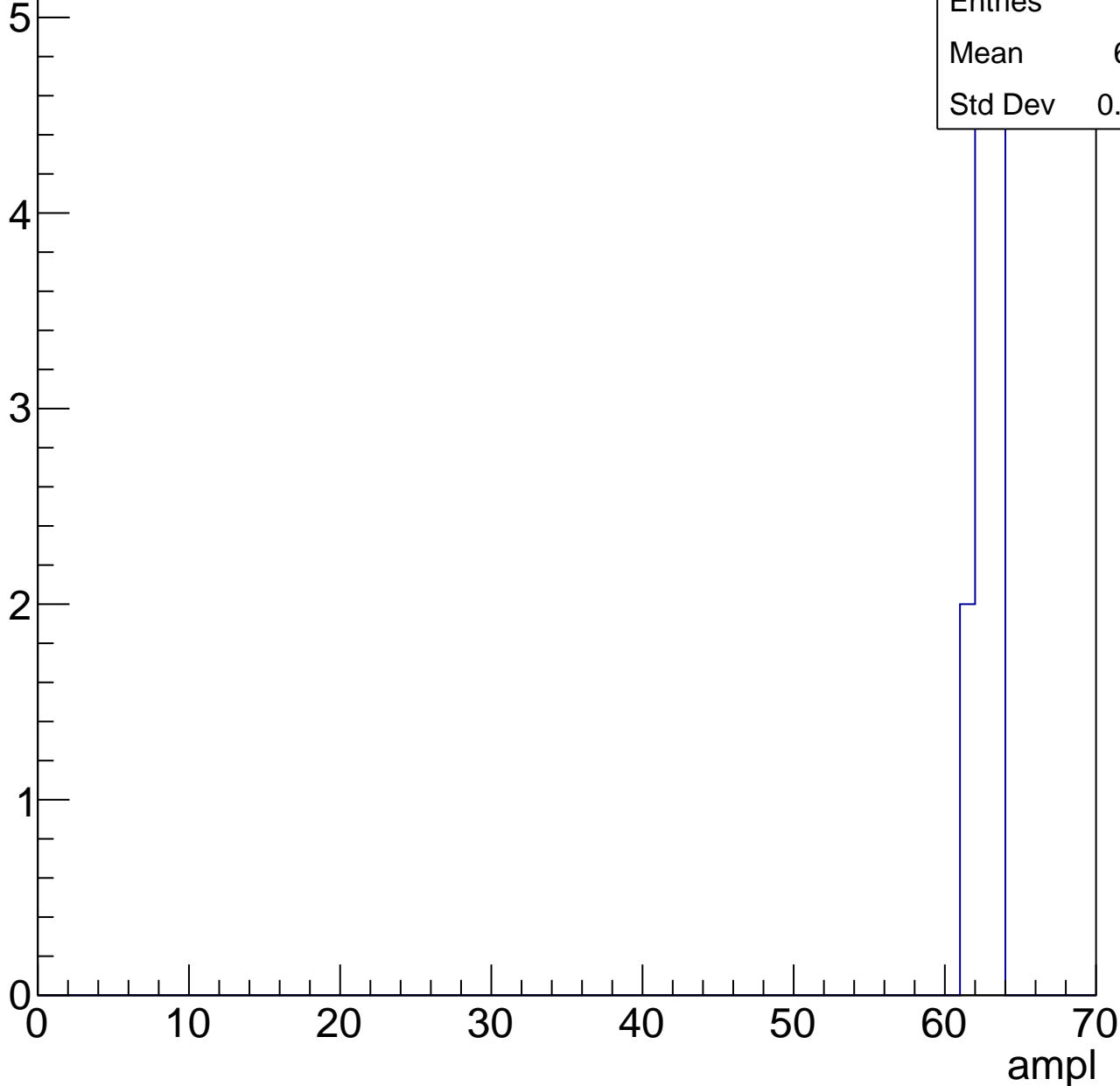


# B1L103S, U21-ch74, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	12
Mean	62.25
Std Dev	0.7217

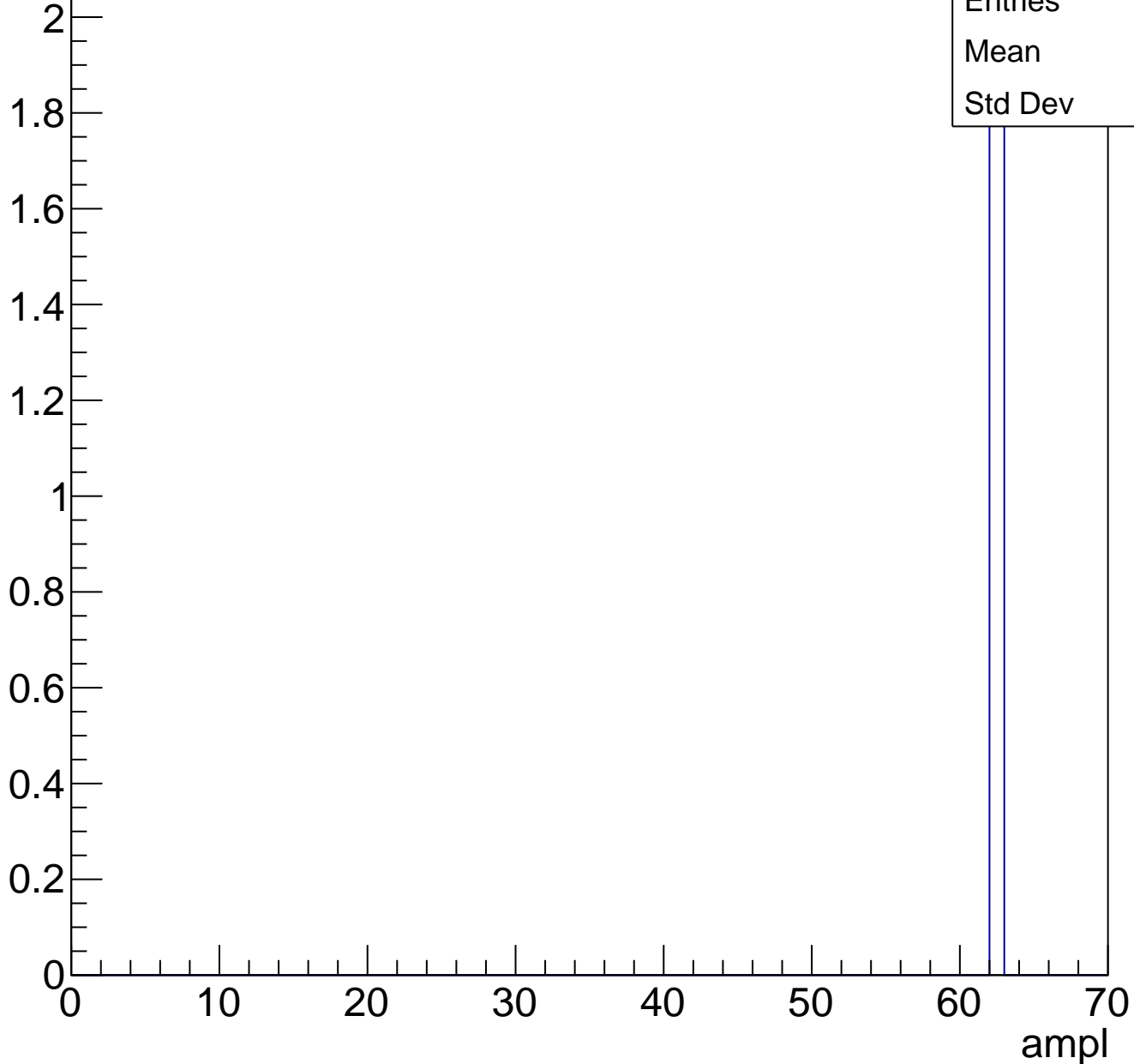




# B1L103S, U21-ch74, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U21-ch75, adc0

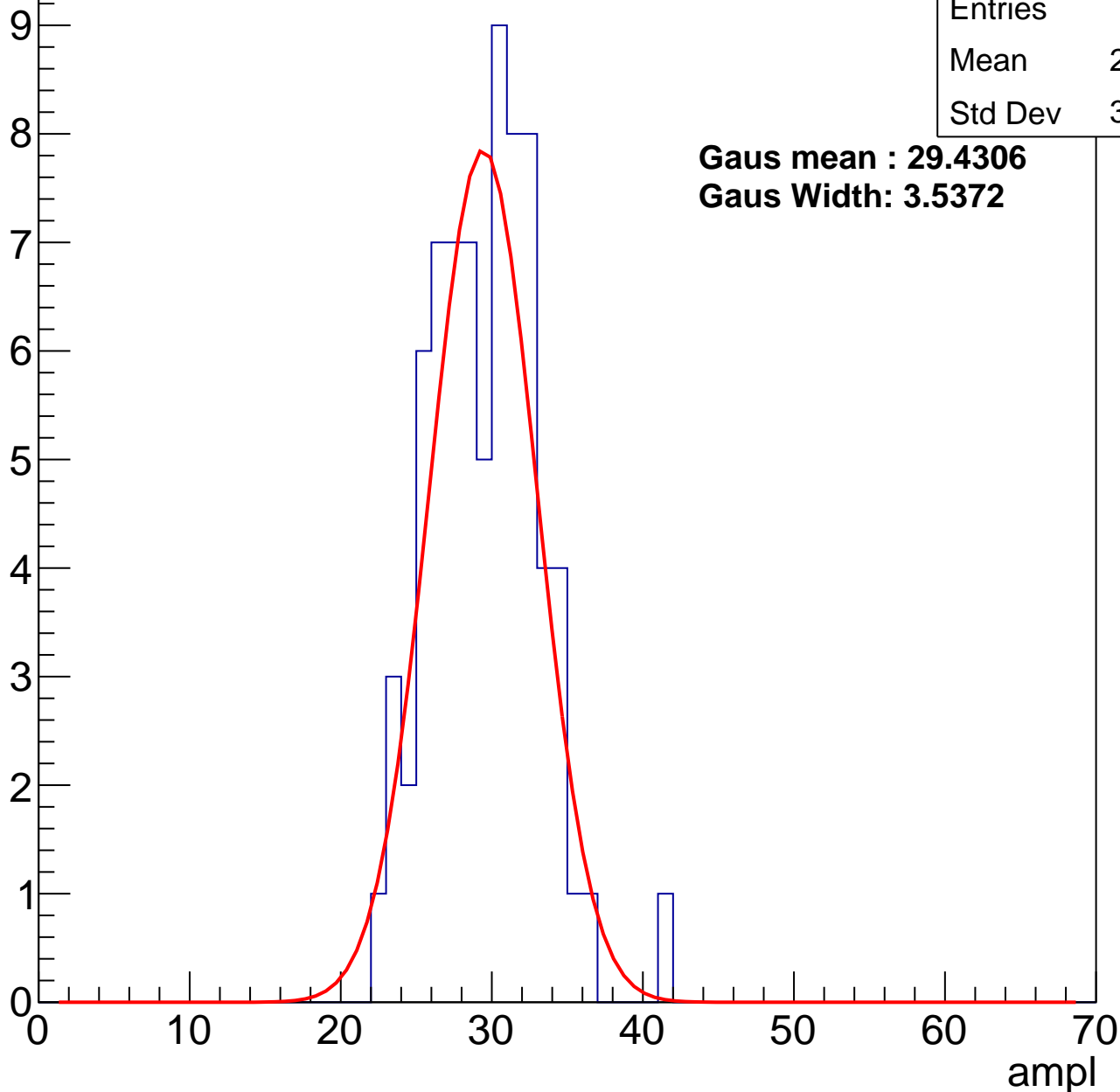
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	29.12
Std Dev	3.499

**Gaus mean : 29.4306**

**Gaus Width: 3.5372**



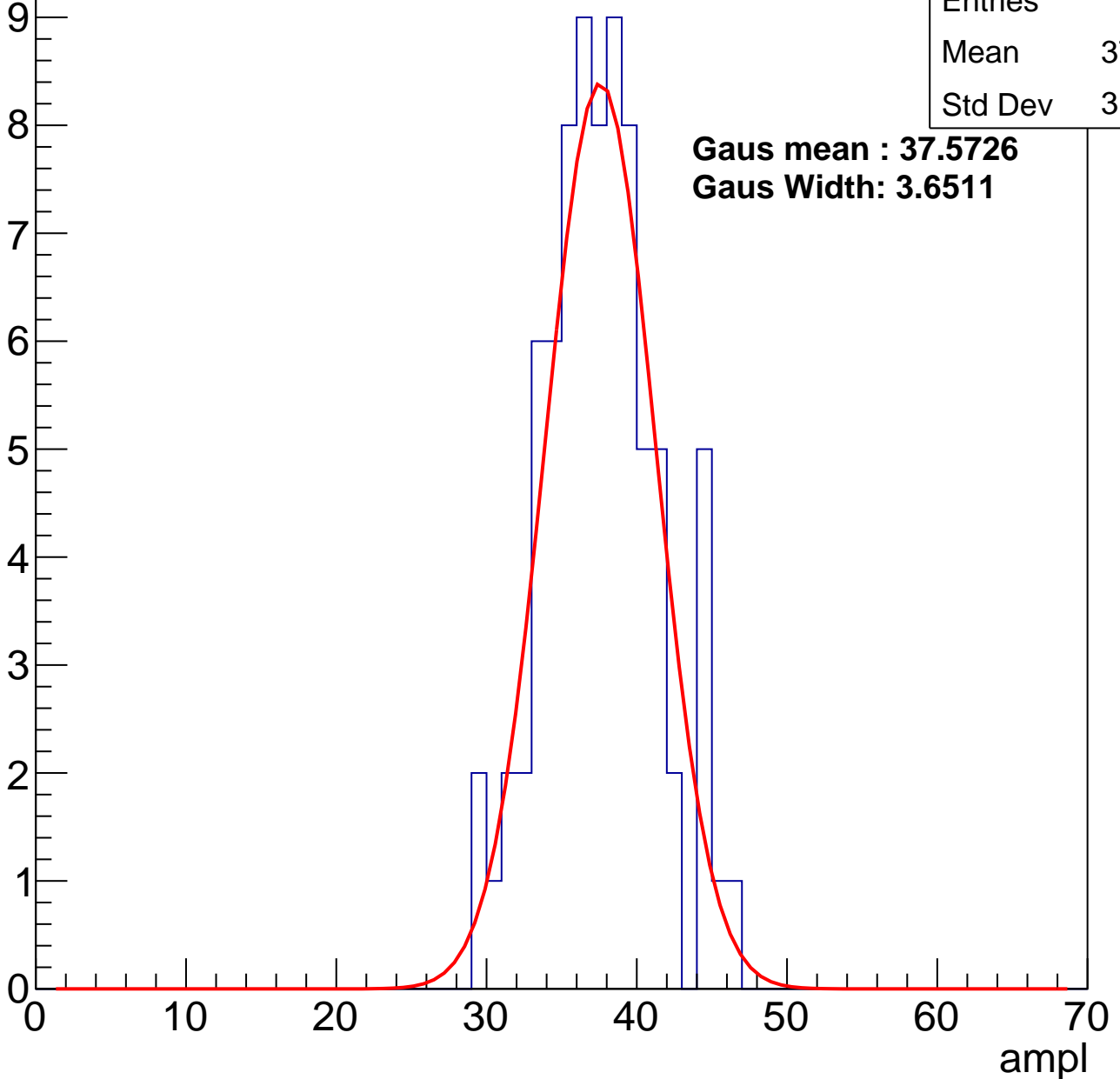
# B1L103S, U21-ch75, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	80
Mean	37.12
Std Dev	3.699

**Gaus mean : 37.5726**  
**Gaus Width: 3.6511**



# B1L103S, U21-ch75, adc2

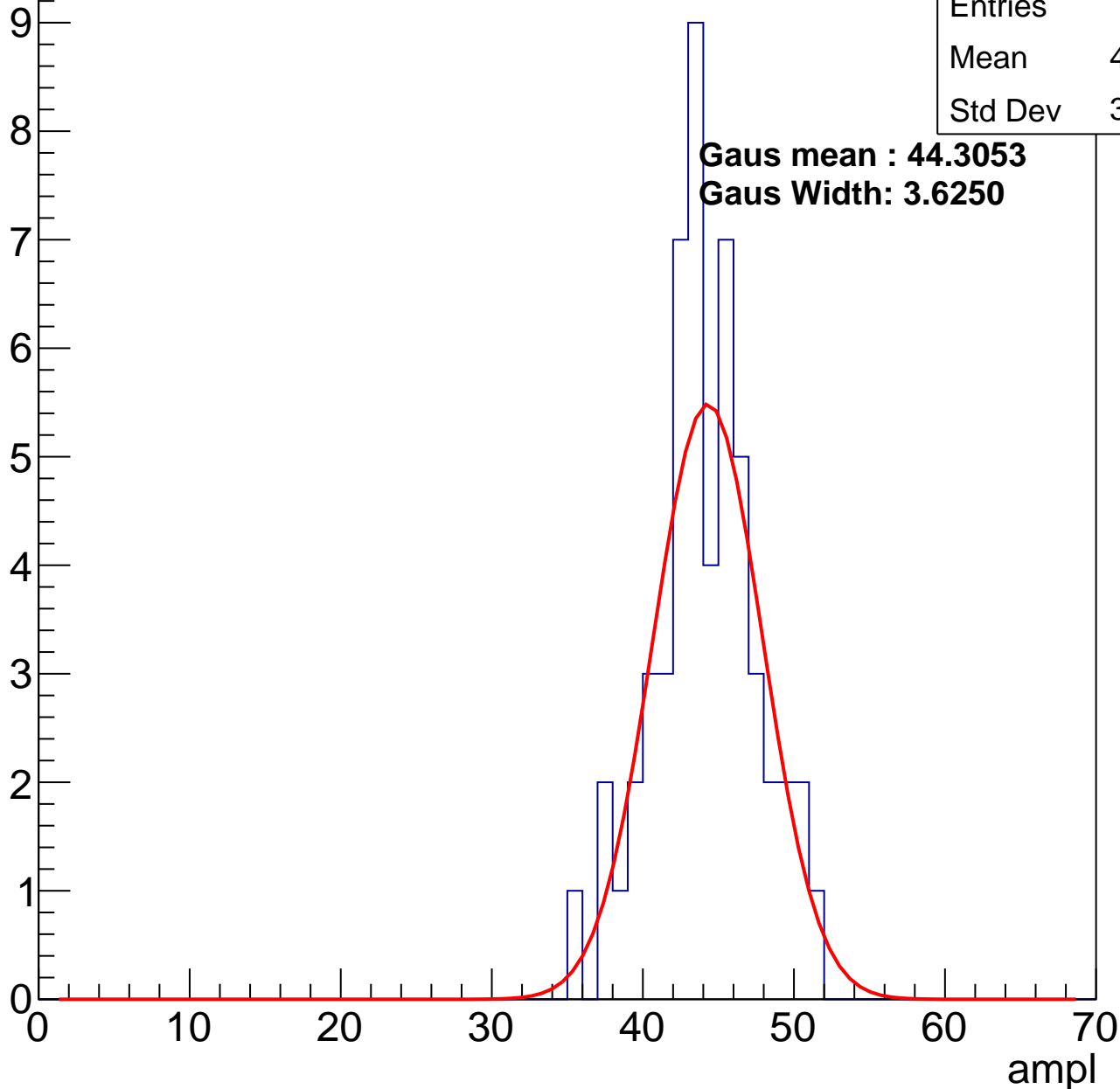
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	43.63
Std Dev	3.406

**Gaus mean : 44.3053**

**Gaus Width: 3.6250**

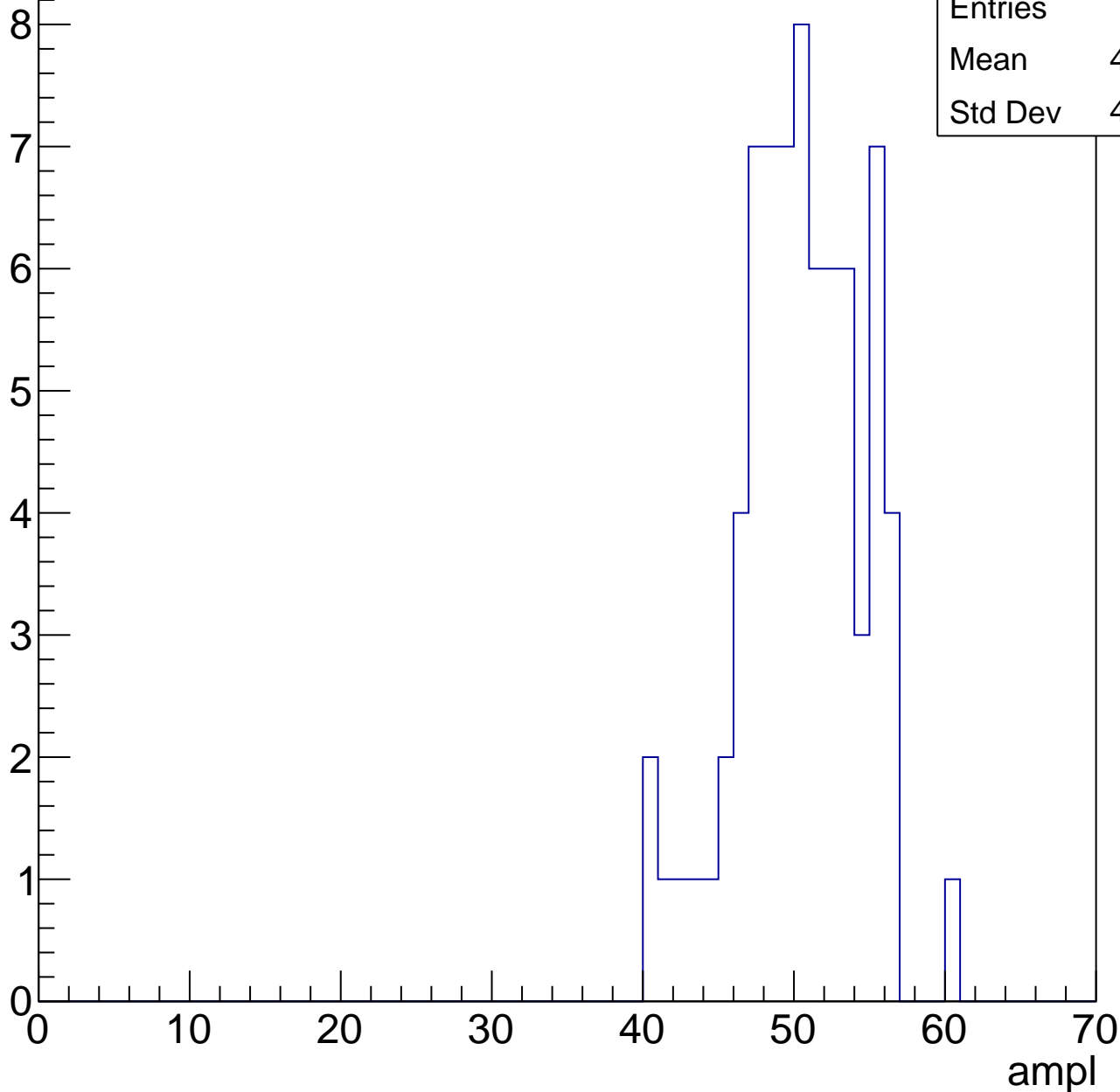


# B1L103S, U21-ch75, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	49.99
Std Dev	4.015

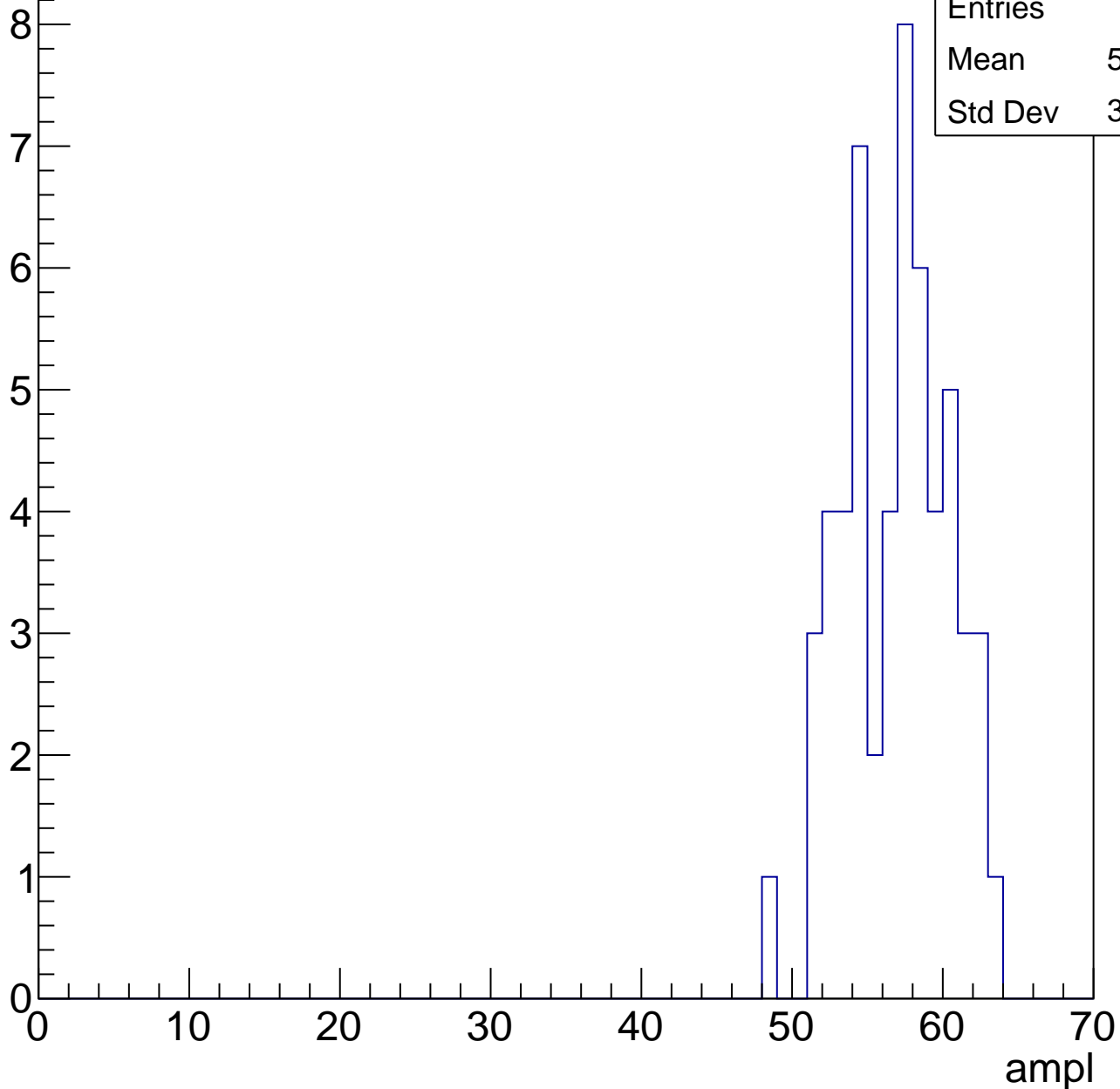


# B1L103S, U21-ch75, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	56.45
Std Dev	3.405

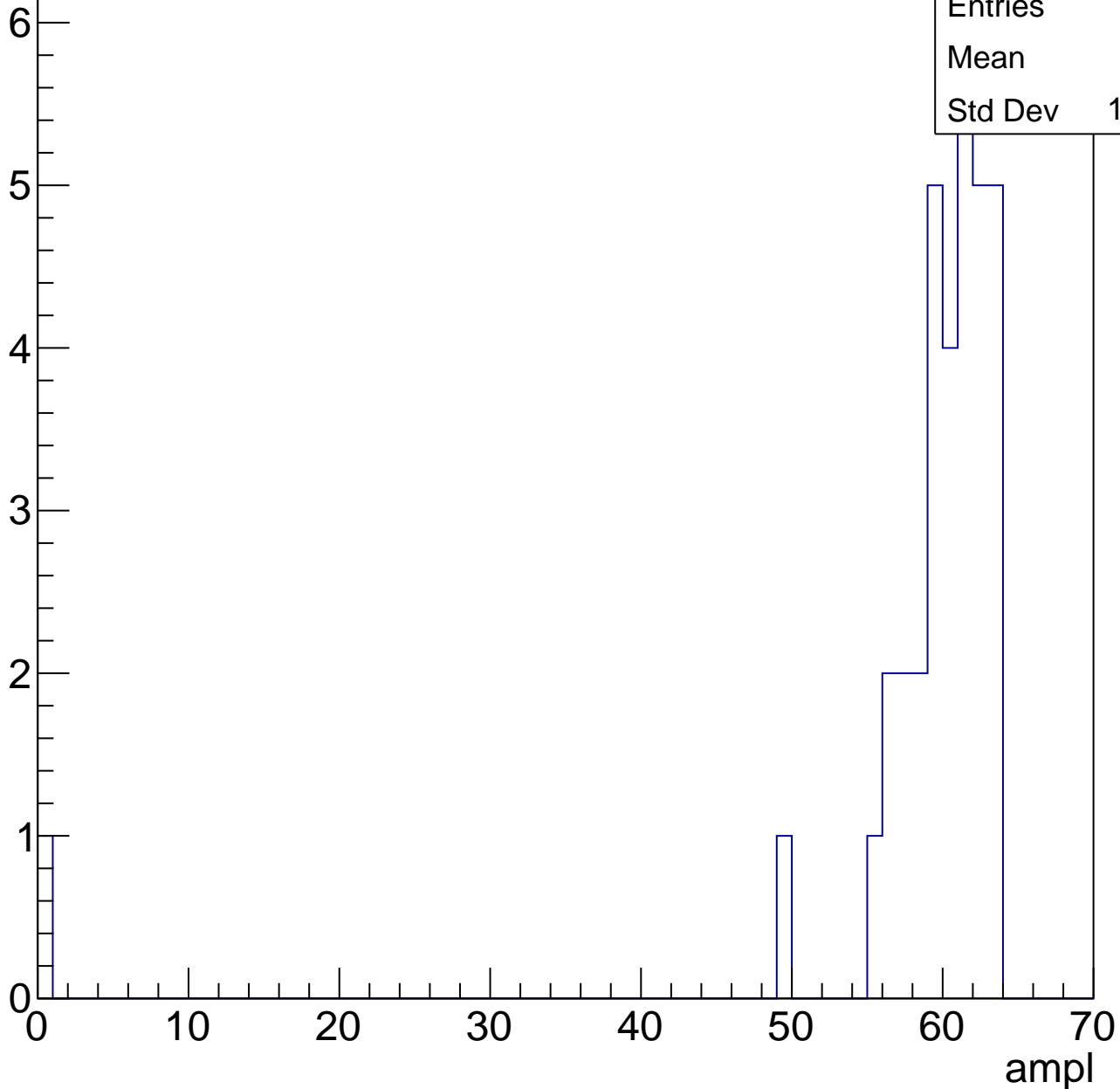


# B1L103S, U21-ch75, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

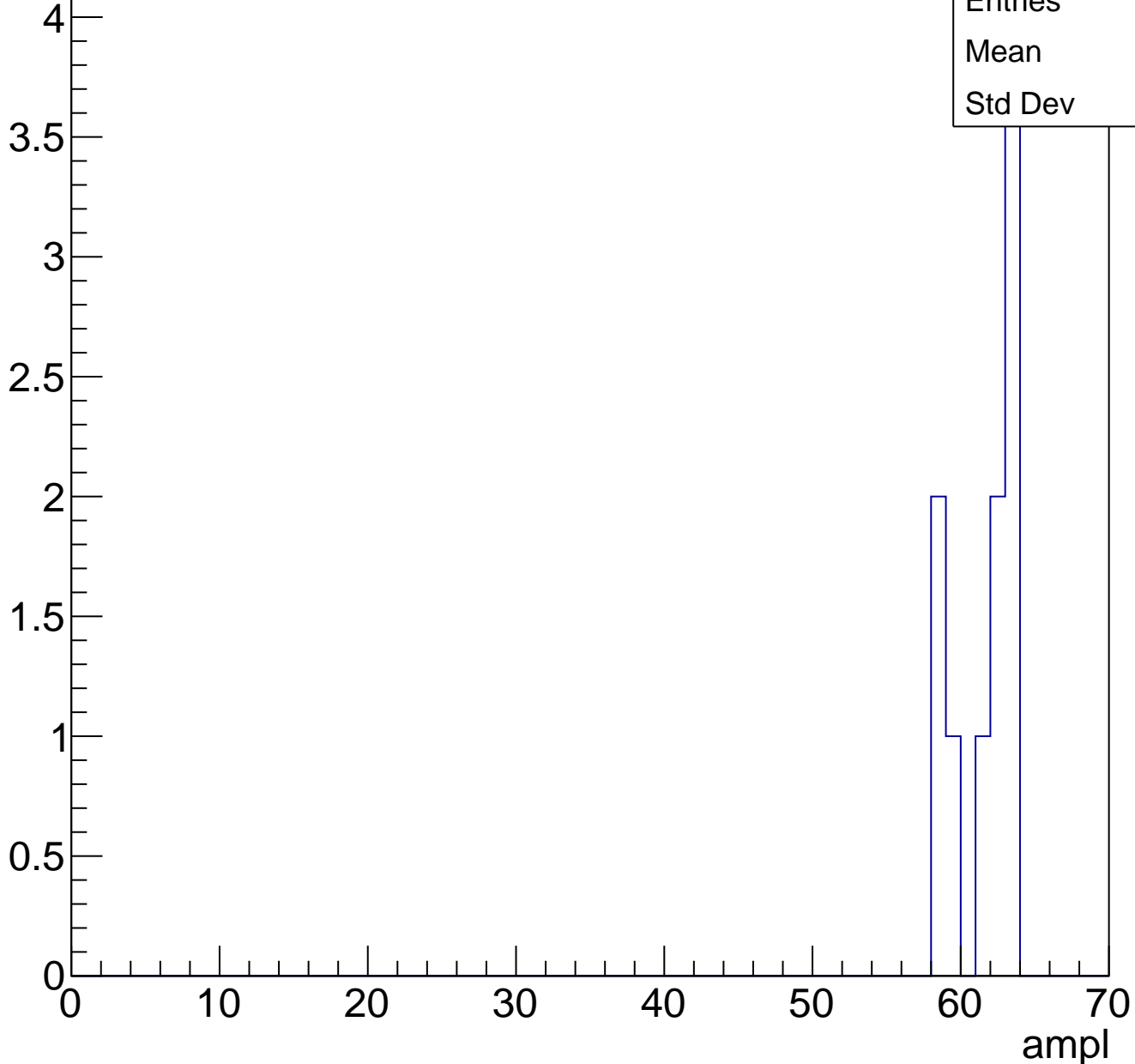
Entries	34
Mean	58
Std Dev	10.49



# B1L103S, U21-ch75, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U21-ch75, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U21-ch76, adc0

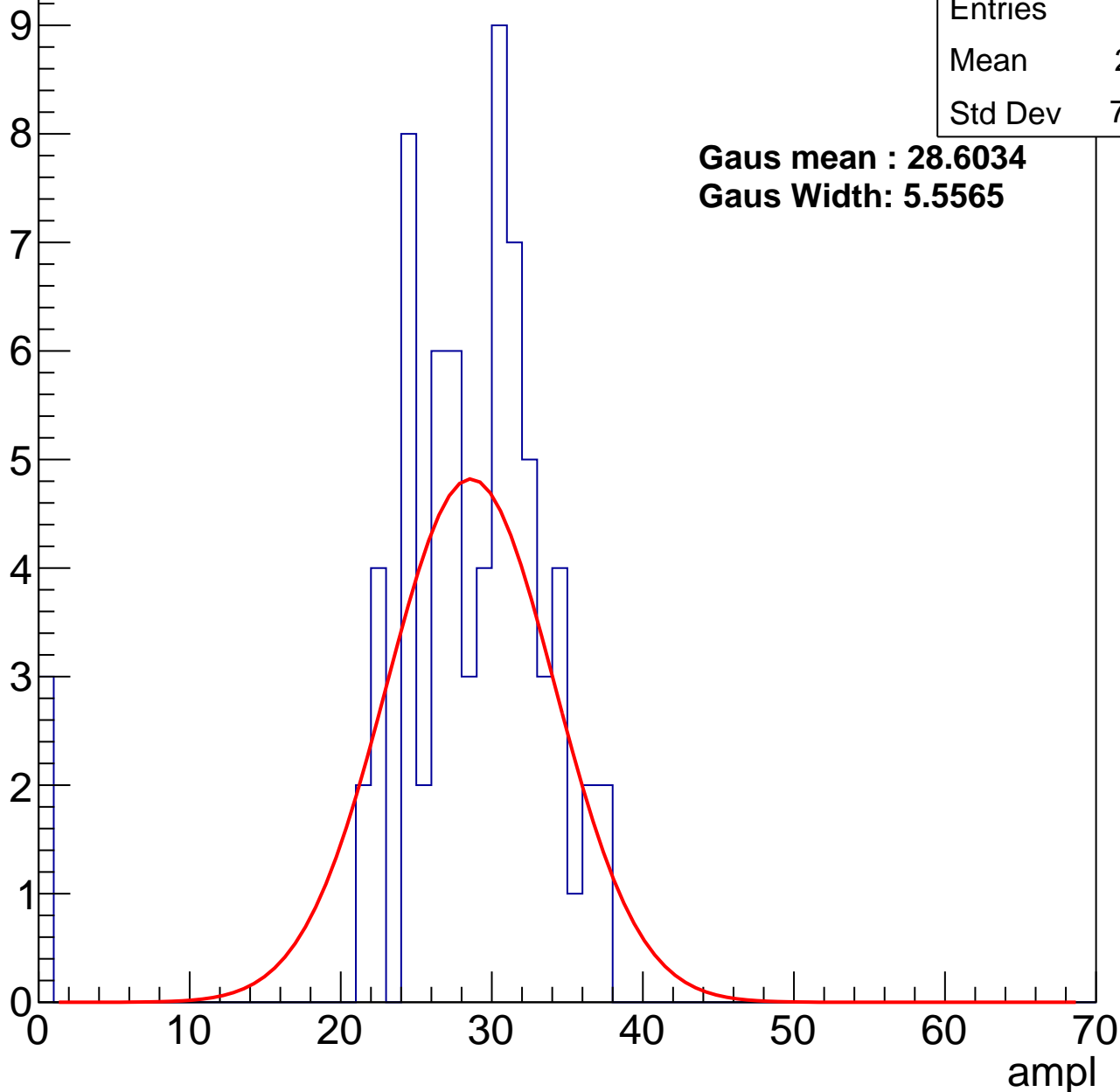
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	27.51
Std Dev	7.015

**Gaus mean : 28.6034**

**Gaus Width: 5.5565**



# B1L103S, U21-ch76, adc1

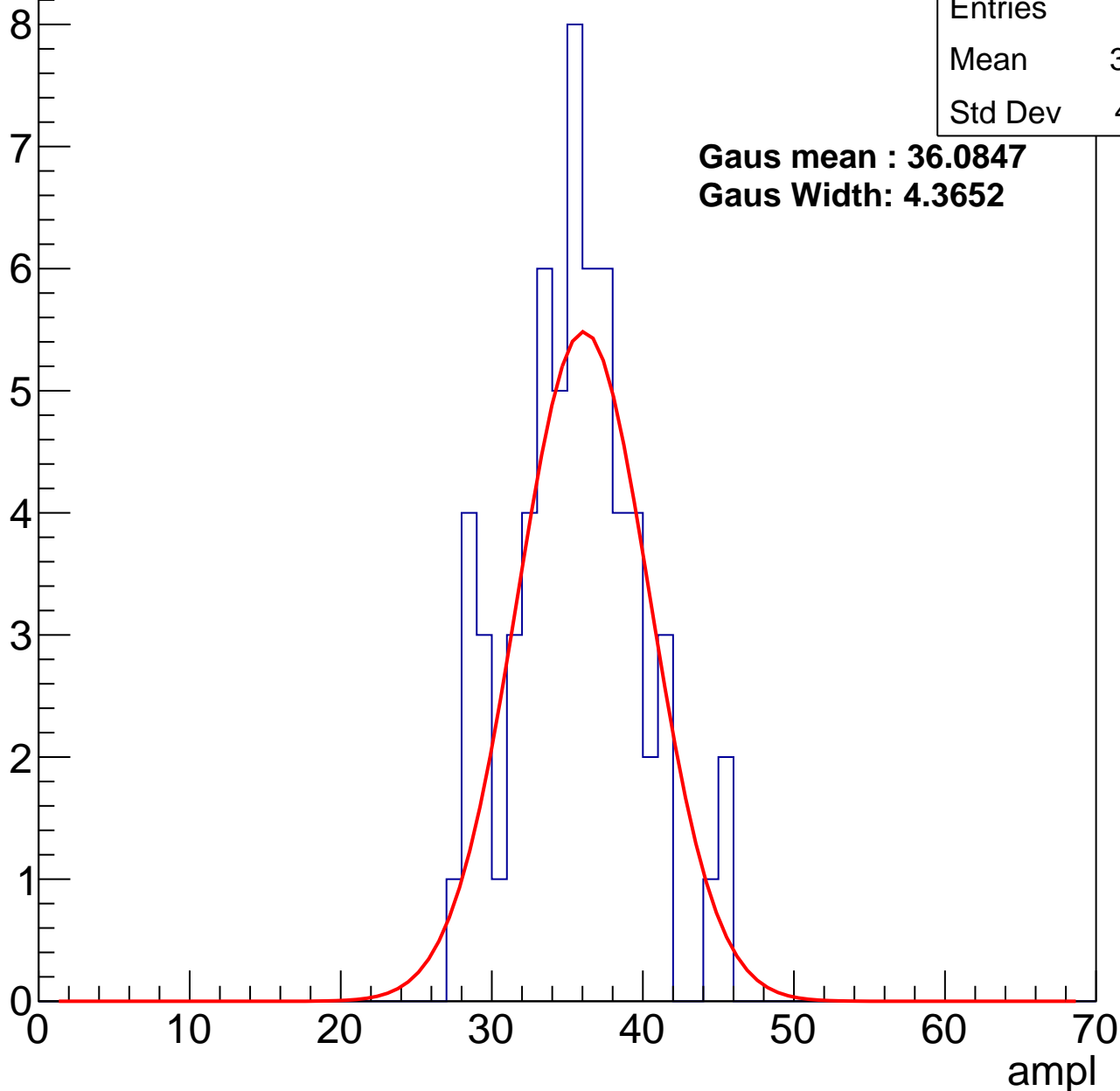
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	35.05
Std Dev	4.131

**Gaus mean : 36.0847**

**Gaus Width: 4.3652**



# B1L103S, U21-ch76, adc2

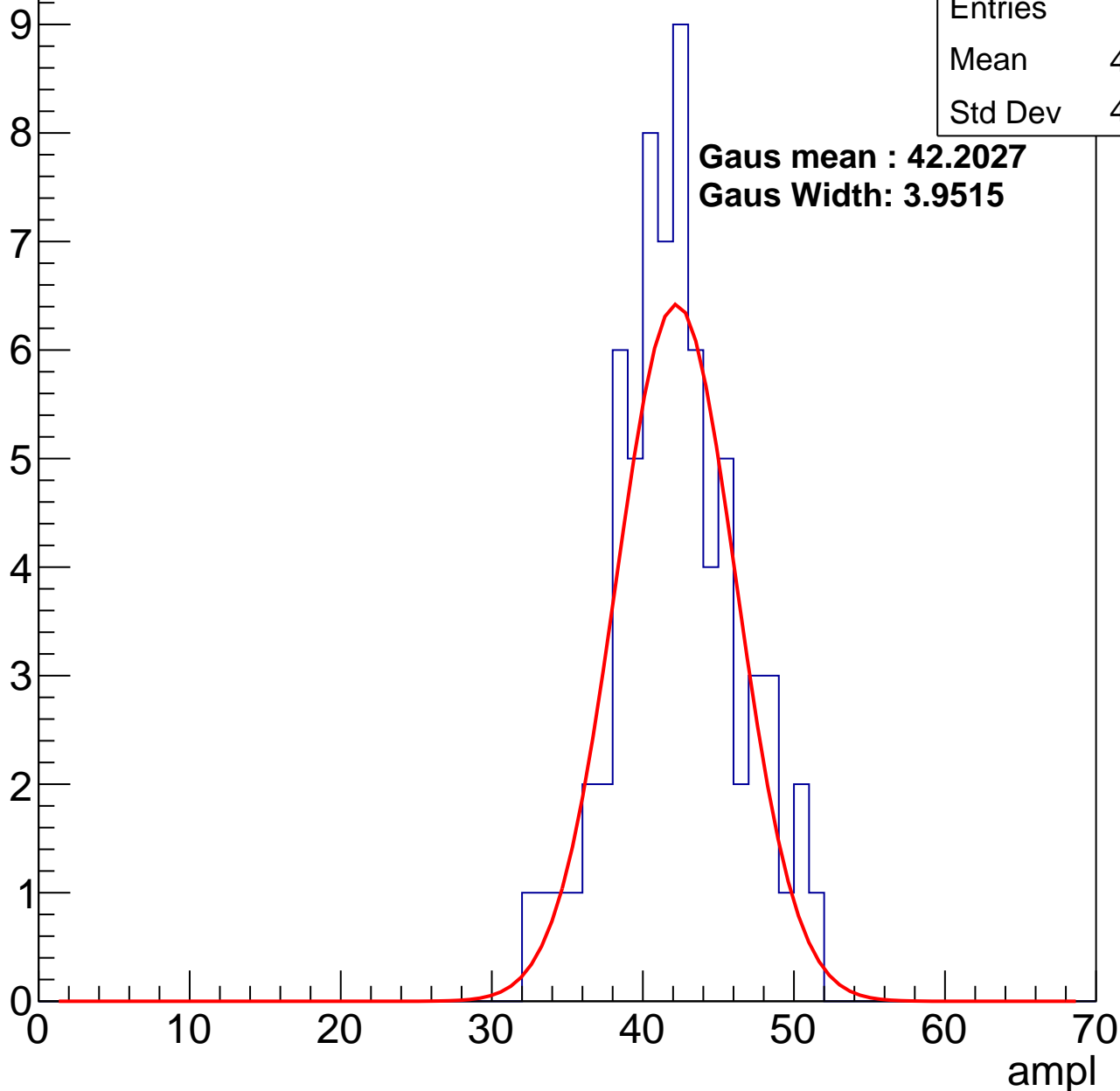
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	41.77
Std Dev	4.022

**Gaus mean : 42.2027**

**Gaus Width: 3.9515**

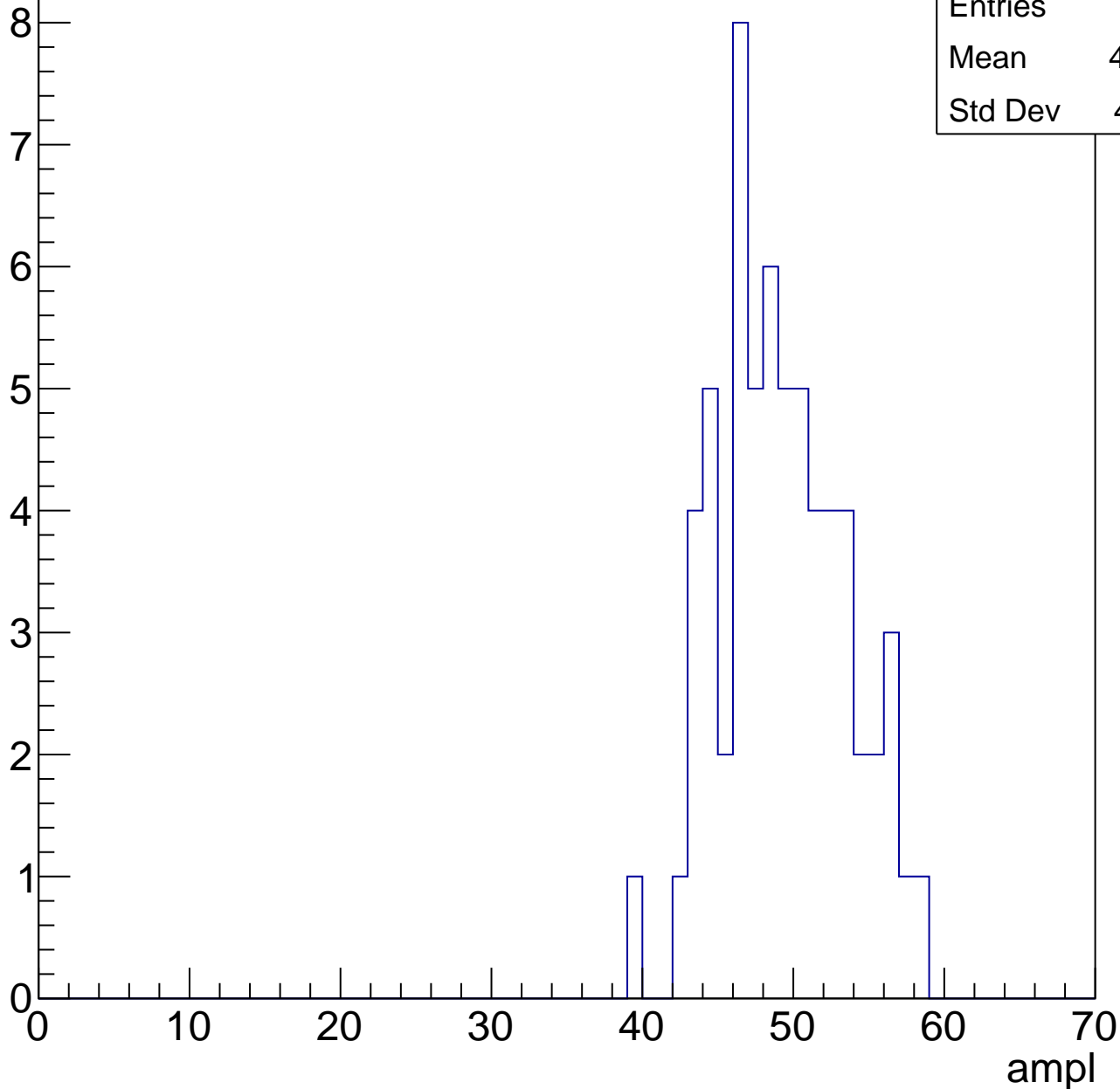


# B1L103S, U21-ch76, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	48.79
Std Dev	4.141

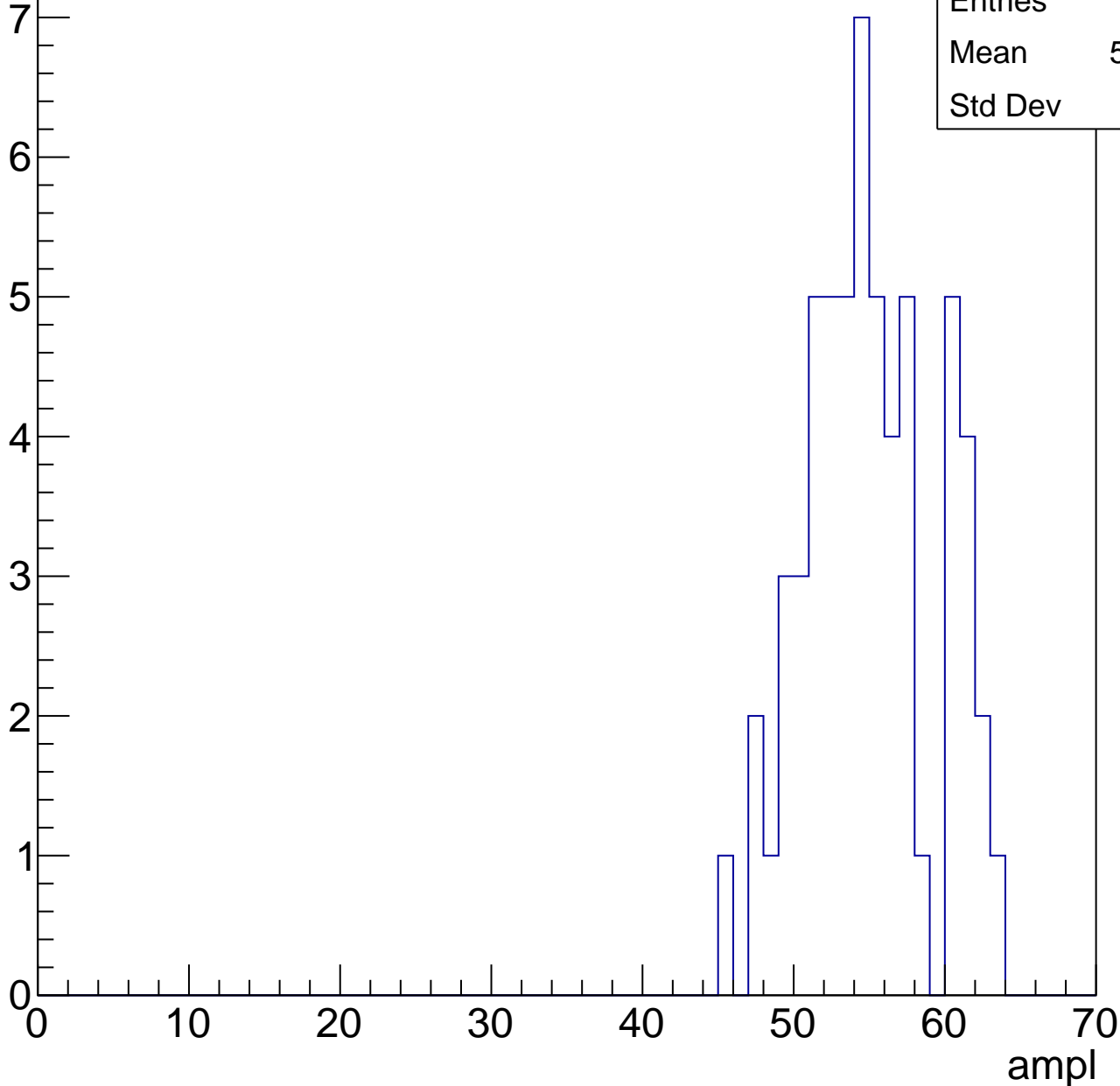


# B1L103S, U21-ch76, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	54.49
Std Dev	4.24

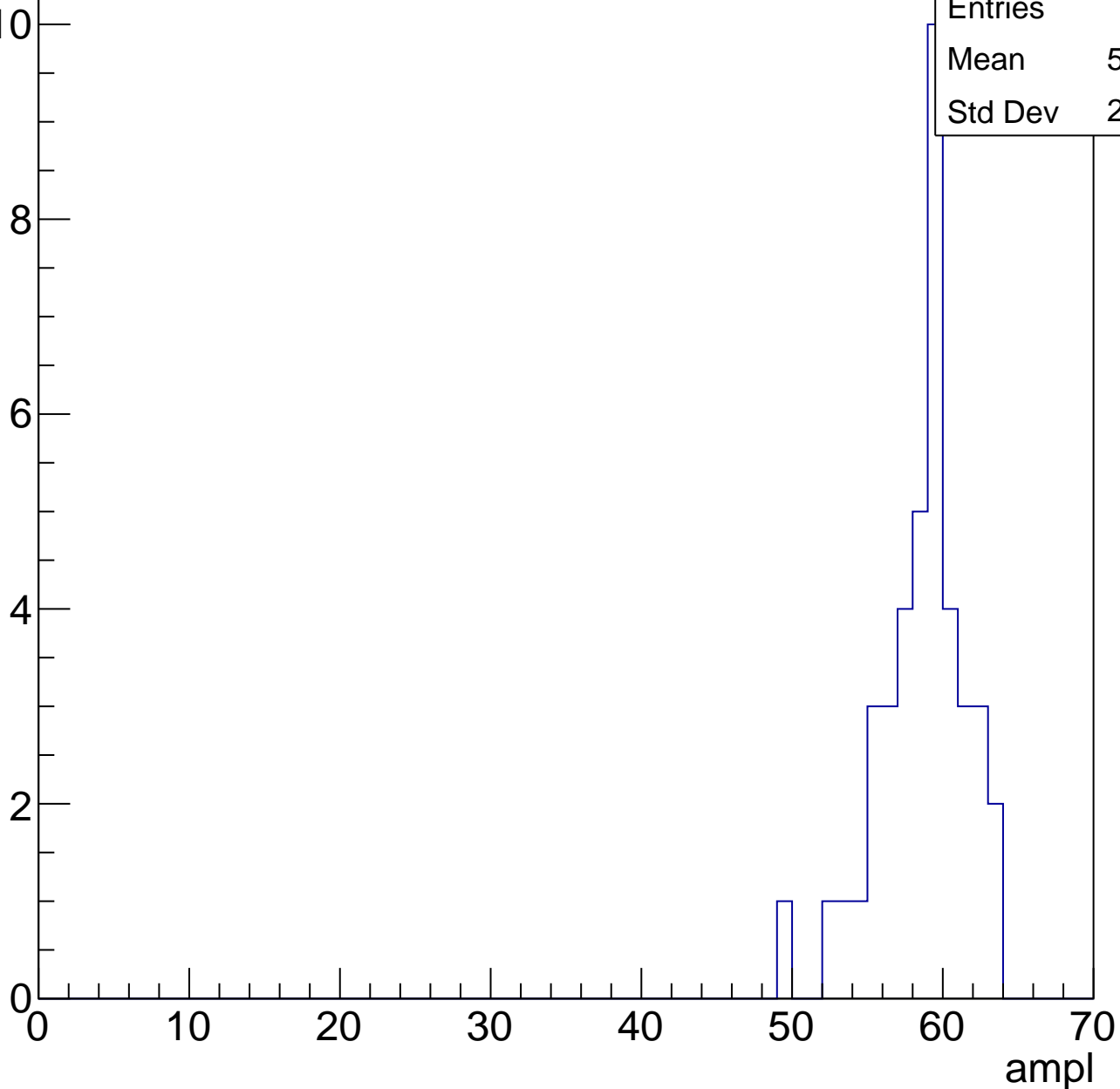


# B1L103S, U21-ch76, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

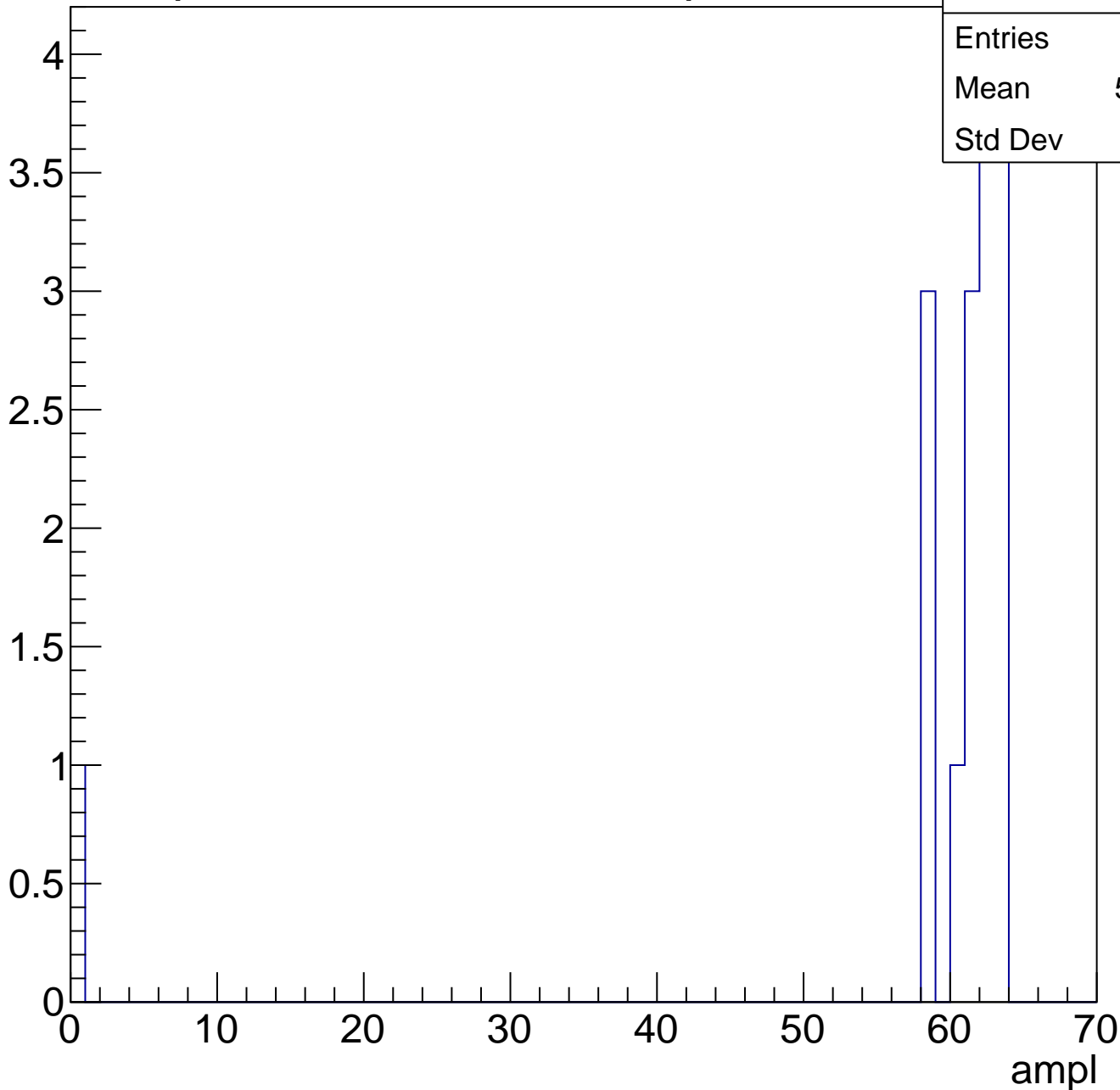
Entries	41
Mean	58.15
Std Dev	2.926



# B1L103S, U21-ch76, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

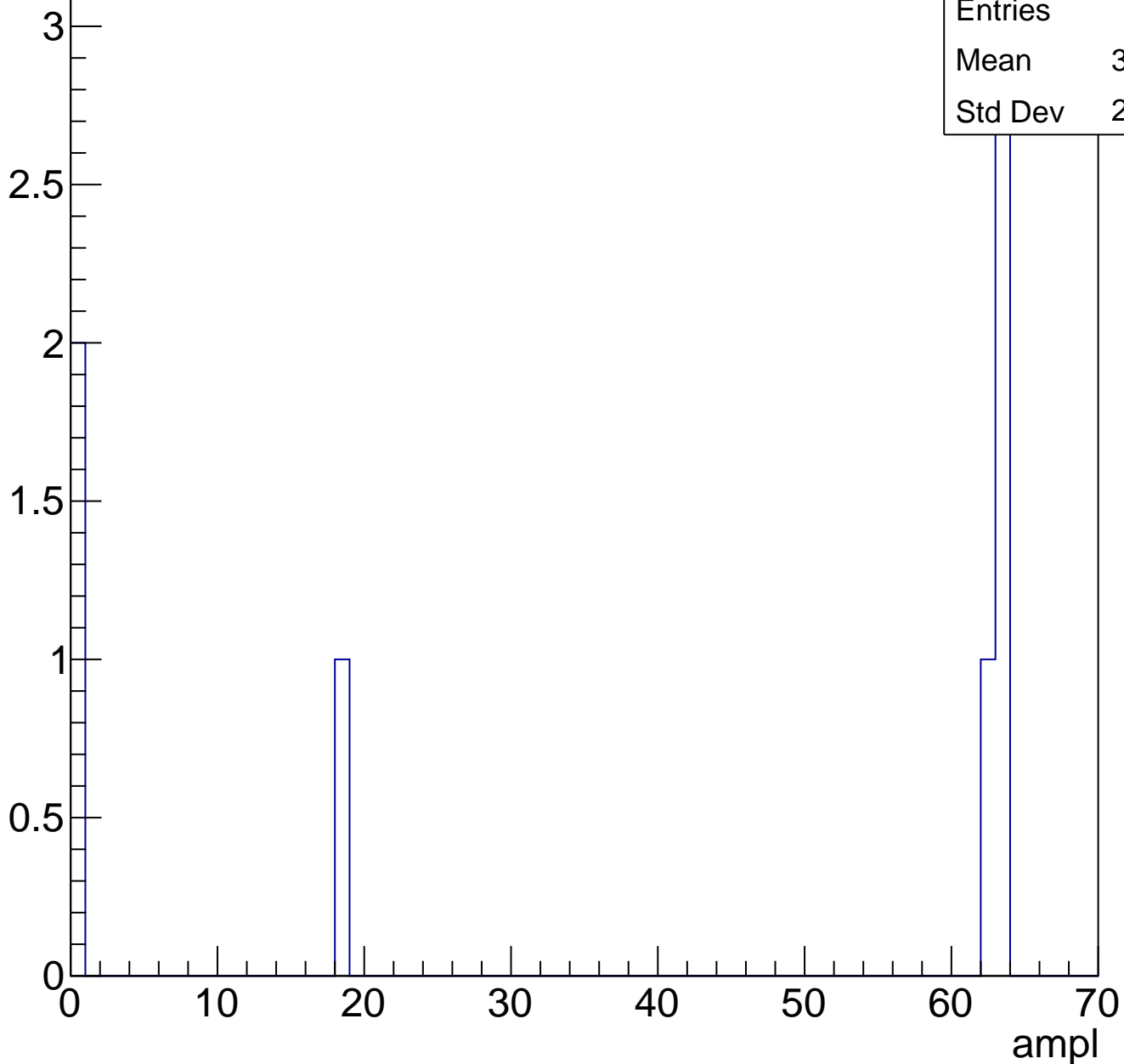




# B1L103S, U21-ch76, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U21-ch77, adc0

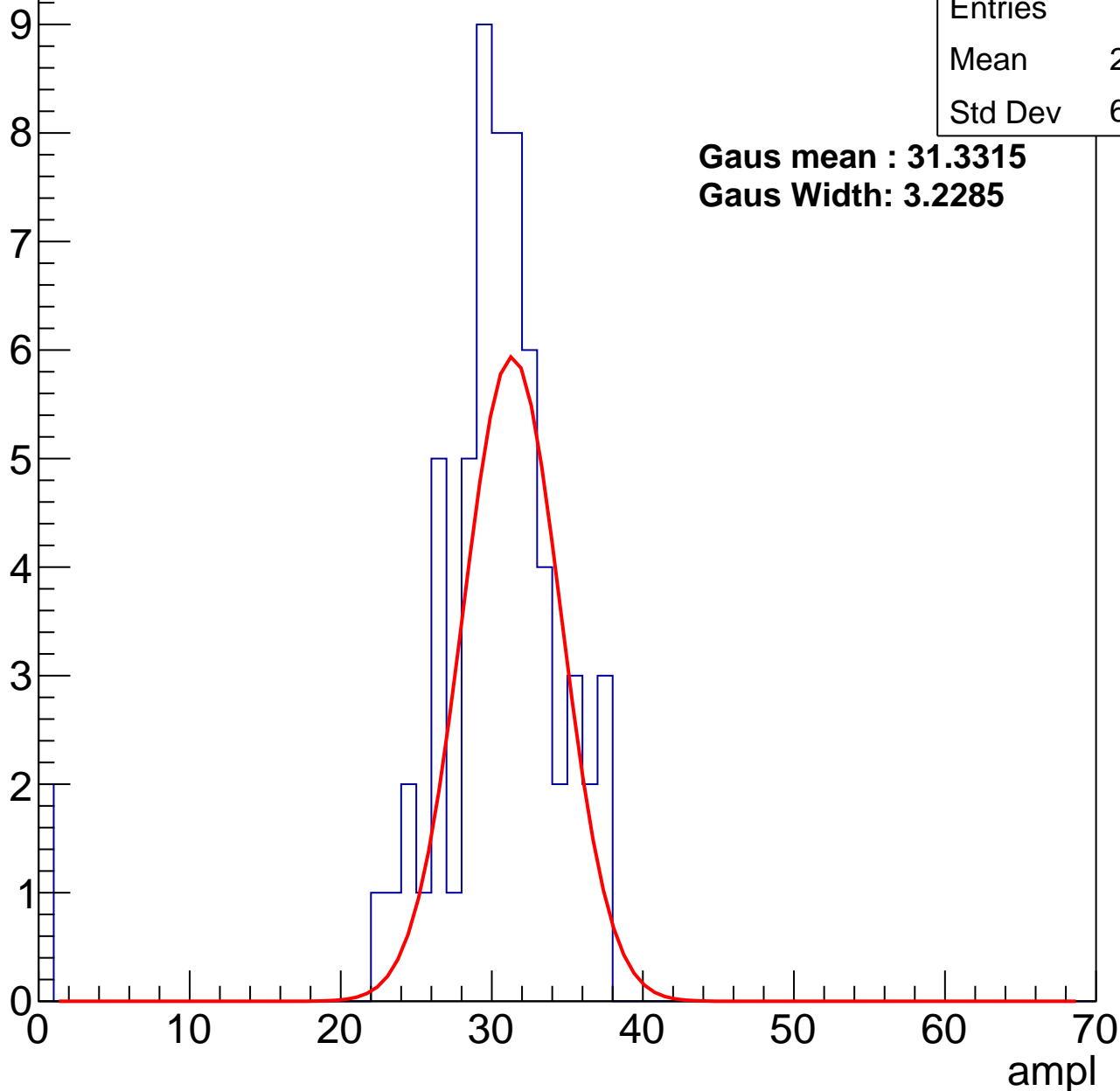
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	29.27
Std Dev	6.285

**Gaus mean : 31.3315**

**Gaus Width: 3.2285**



# B1L103S, U21-ch77, adc1

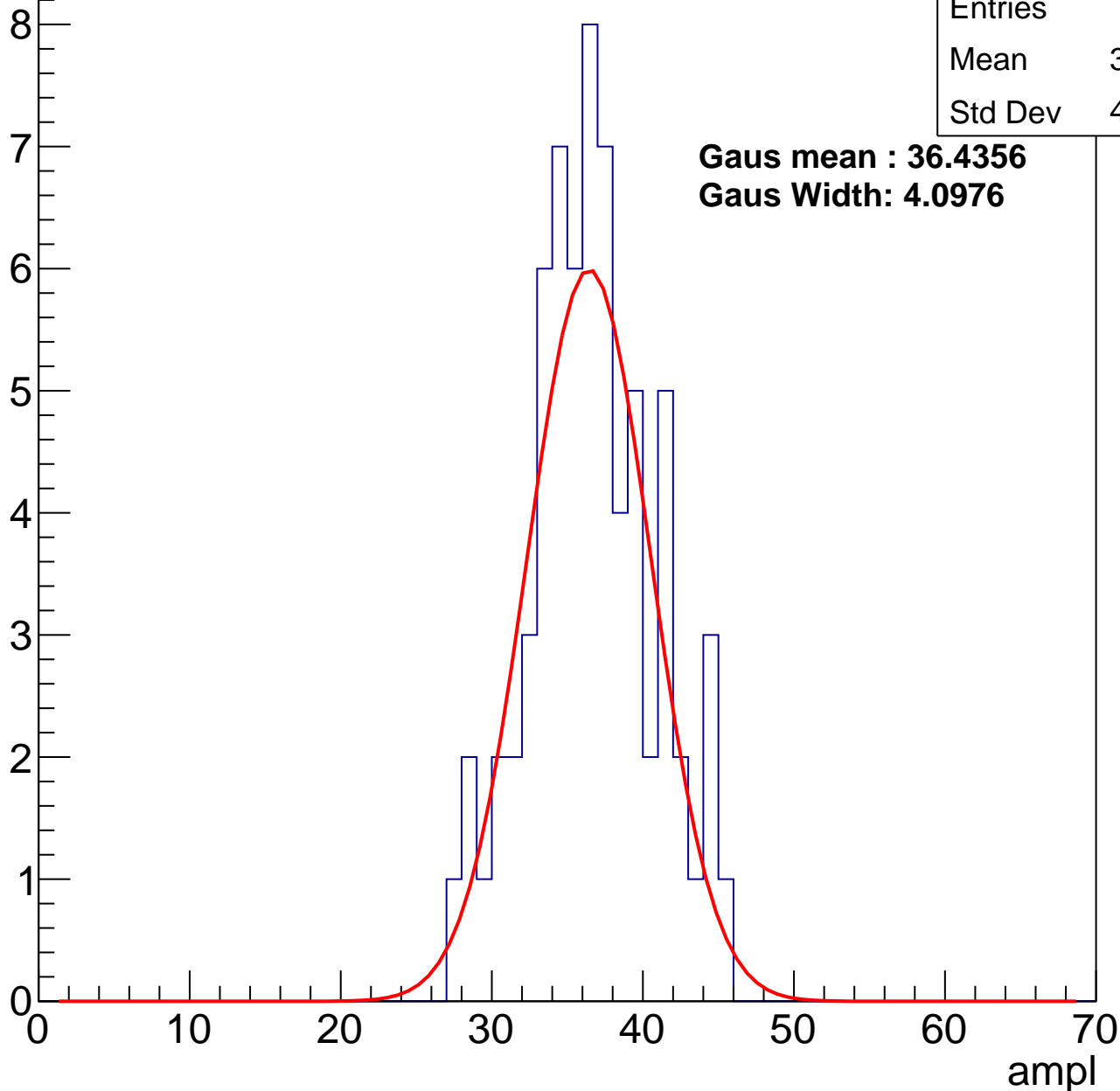
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	36.16
Std Dev	4.082

**Gaus mean : 36.4356**

**Gaus Width: 4.0976**



# B1L103S, U21-ch77, adc2

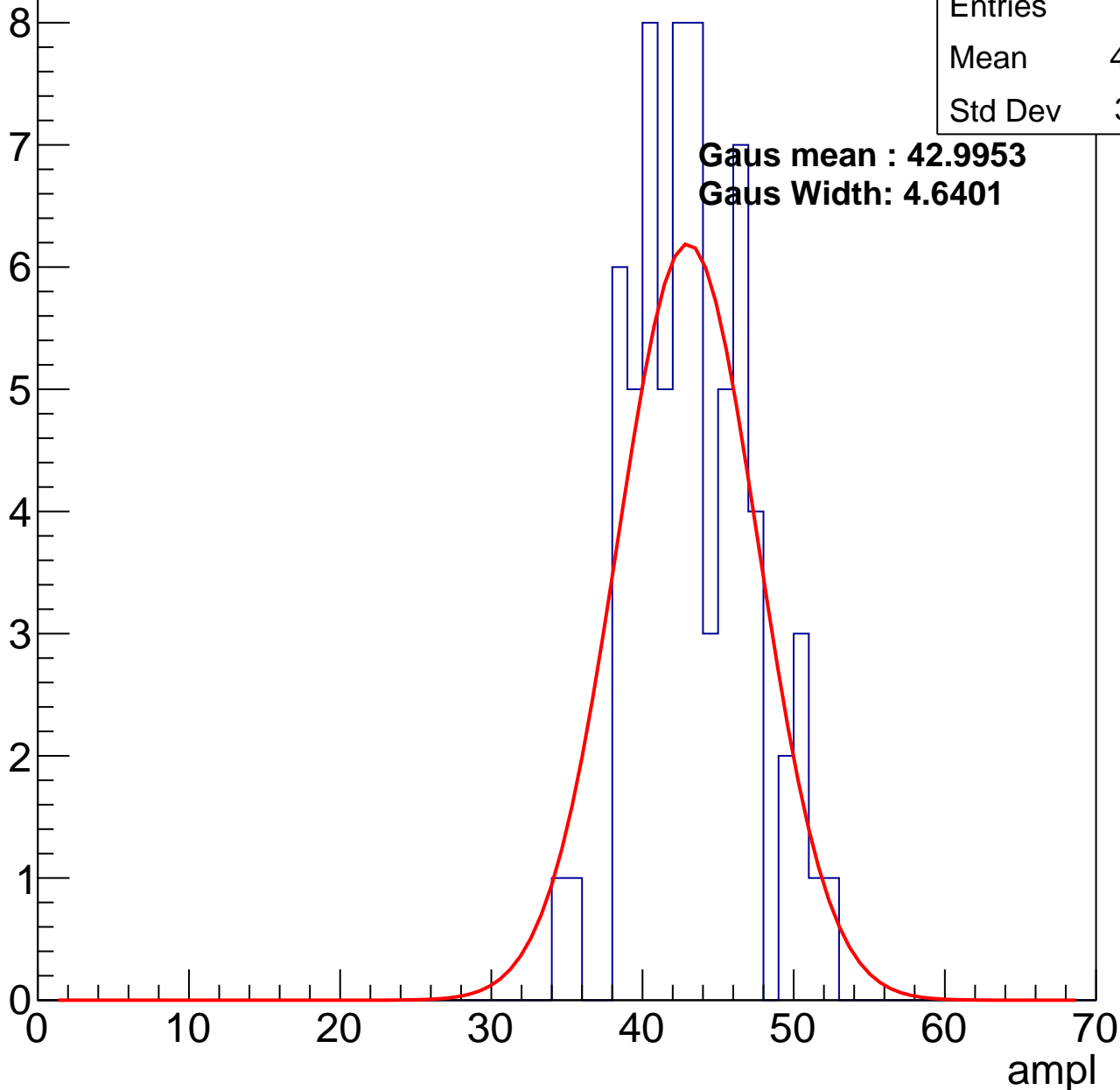
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	42.87
Std Dev	3.811

**Gaus mean : 42.9953**

**Gaus Width: 4.6401**

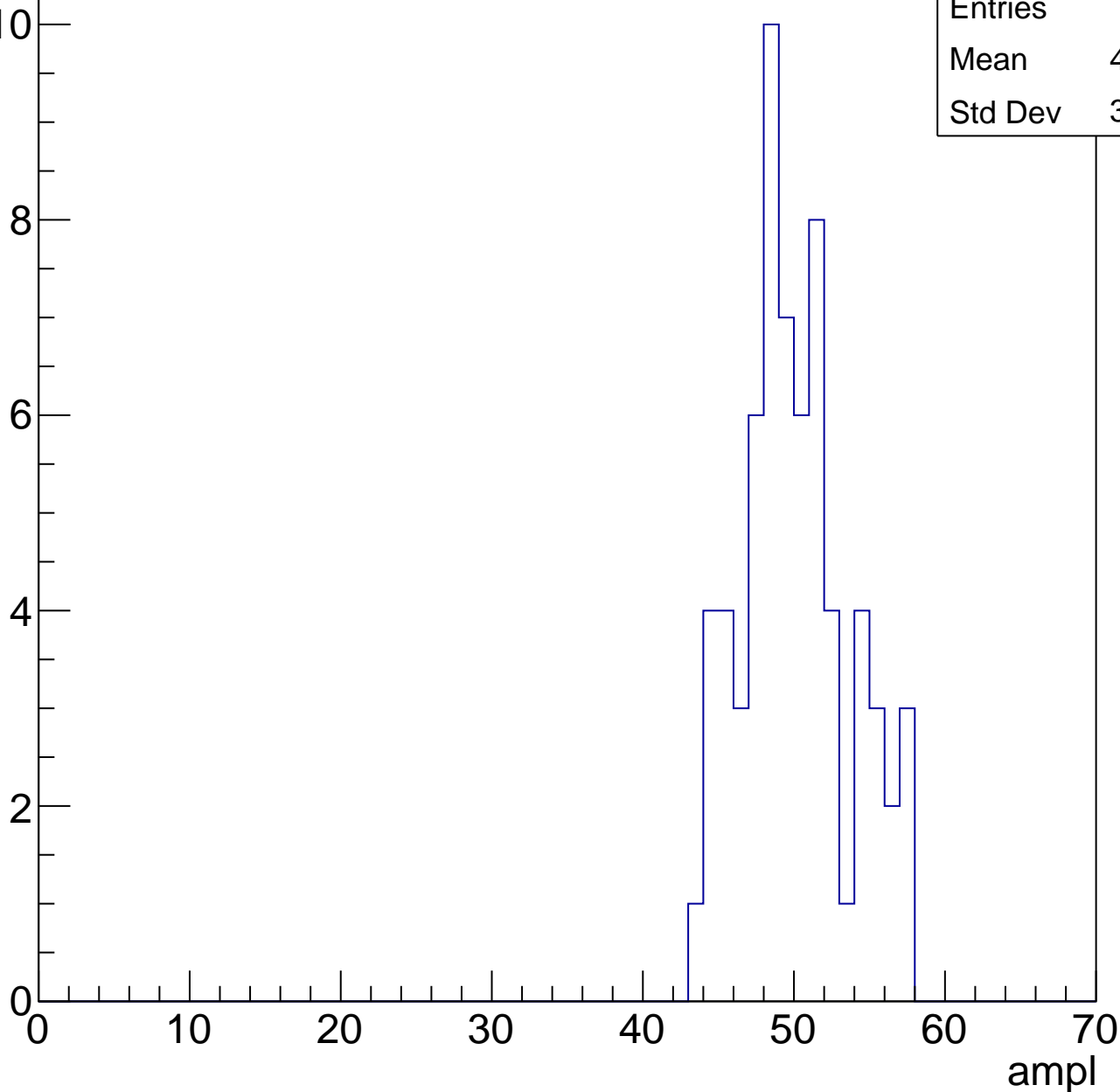


# B1L103S, U21-ch77, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	49.62
Std Dev	3.532

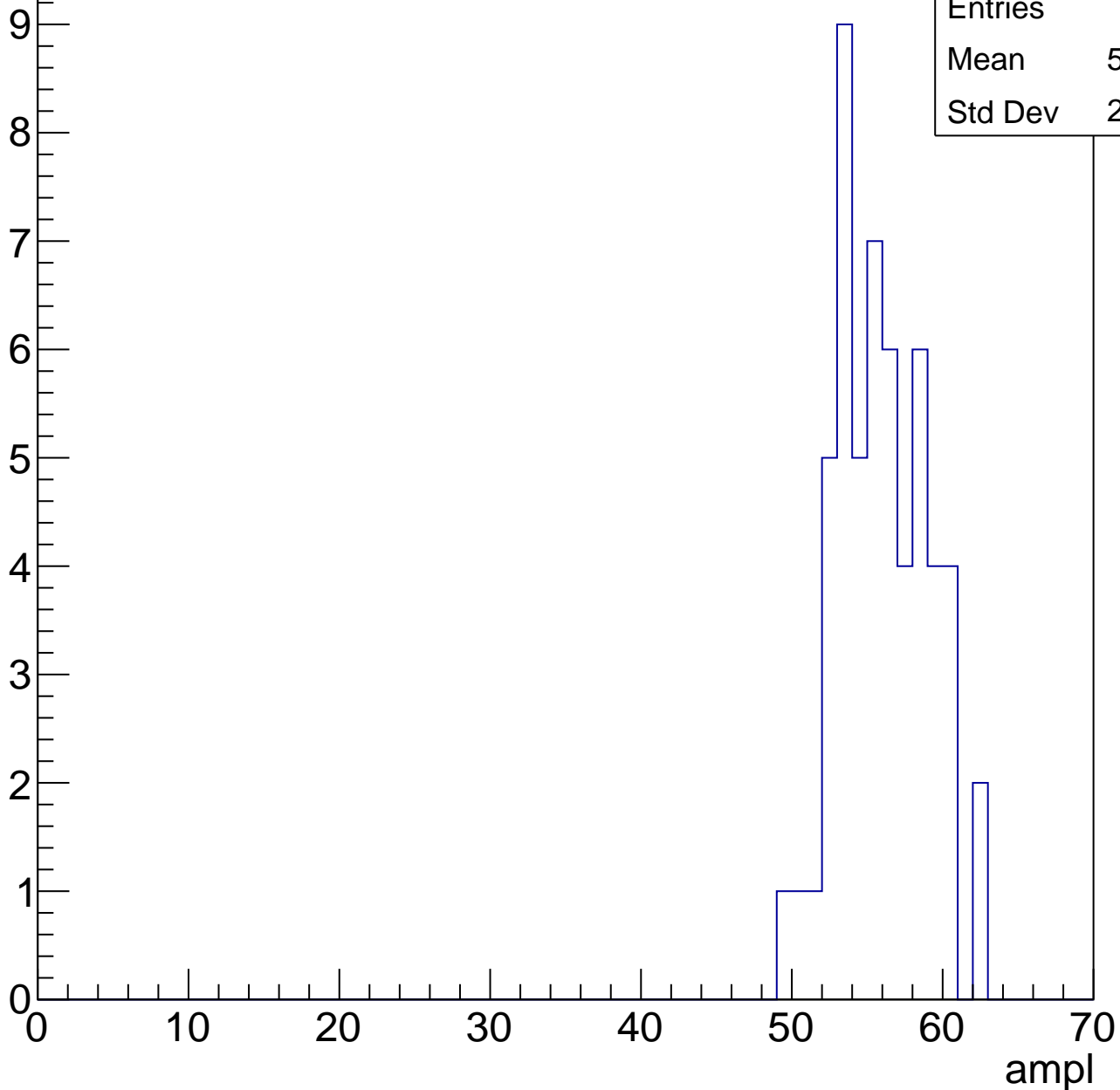


# B1L103S, U21-ch77, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	55.53
Std Dev	2.972

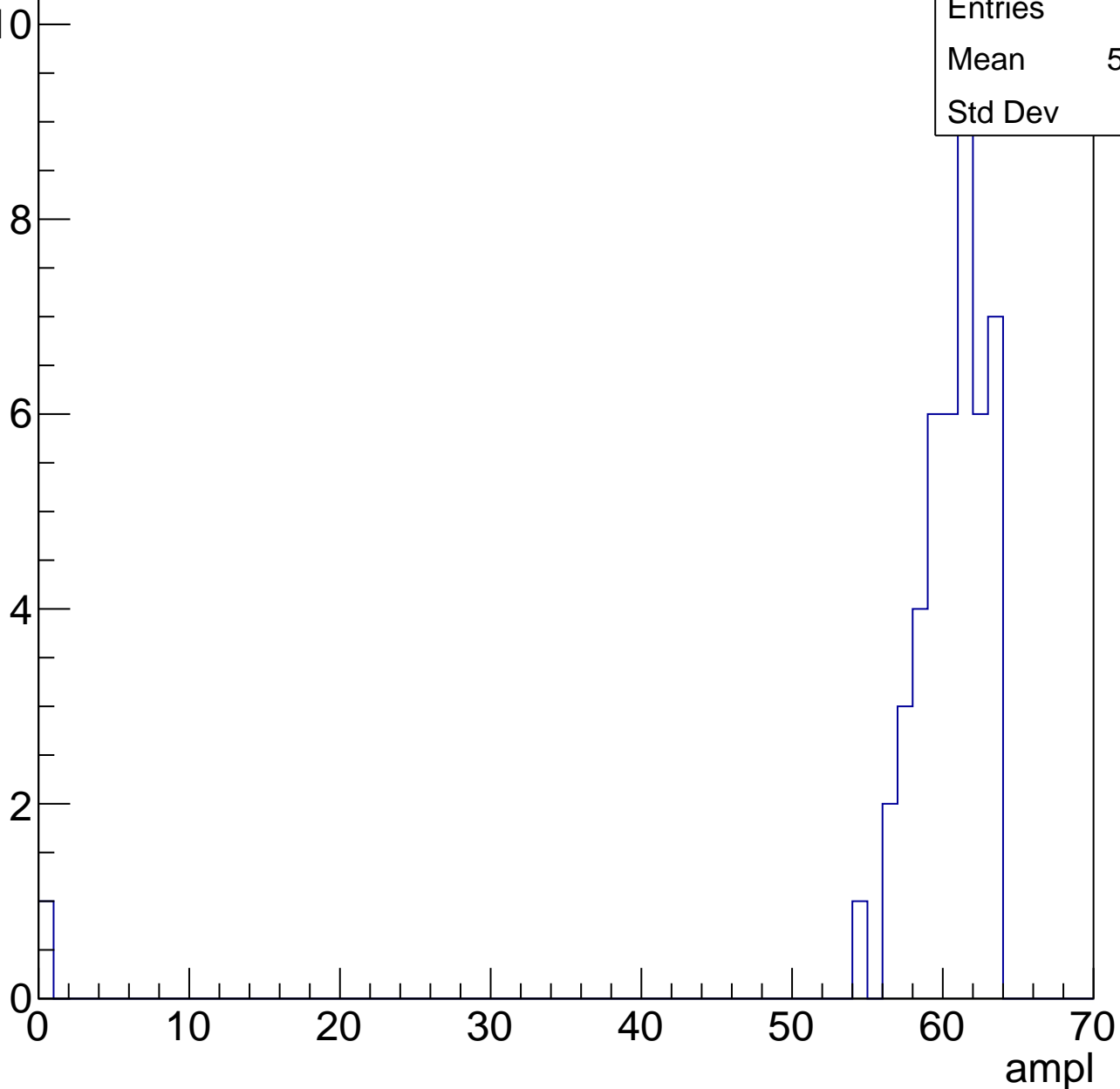


# B1L103S, U21-ch77, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	46
Mean	58.83
Std Dev	9.03



# B1L103S, U21-ch77, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U21-ch77, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L103S, U21-ch78, adc0

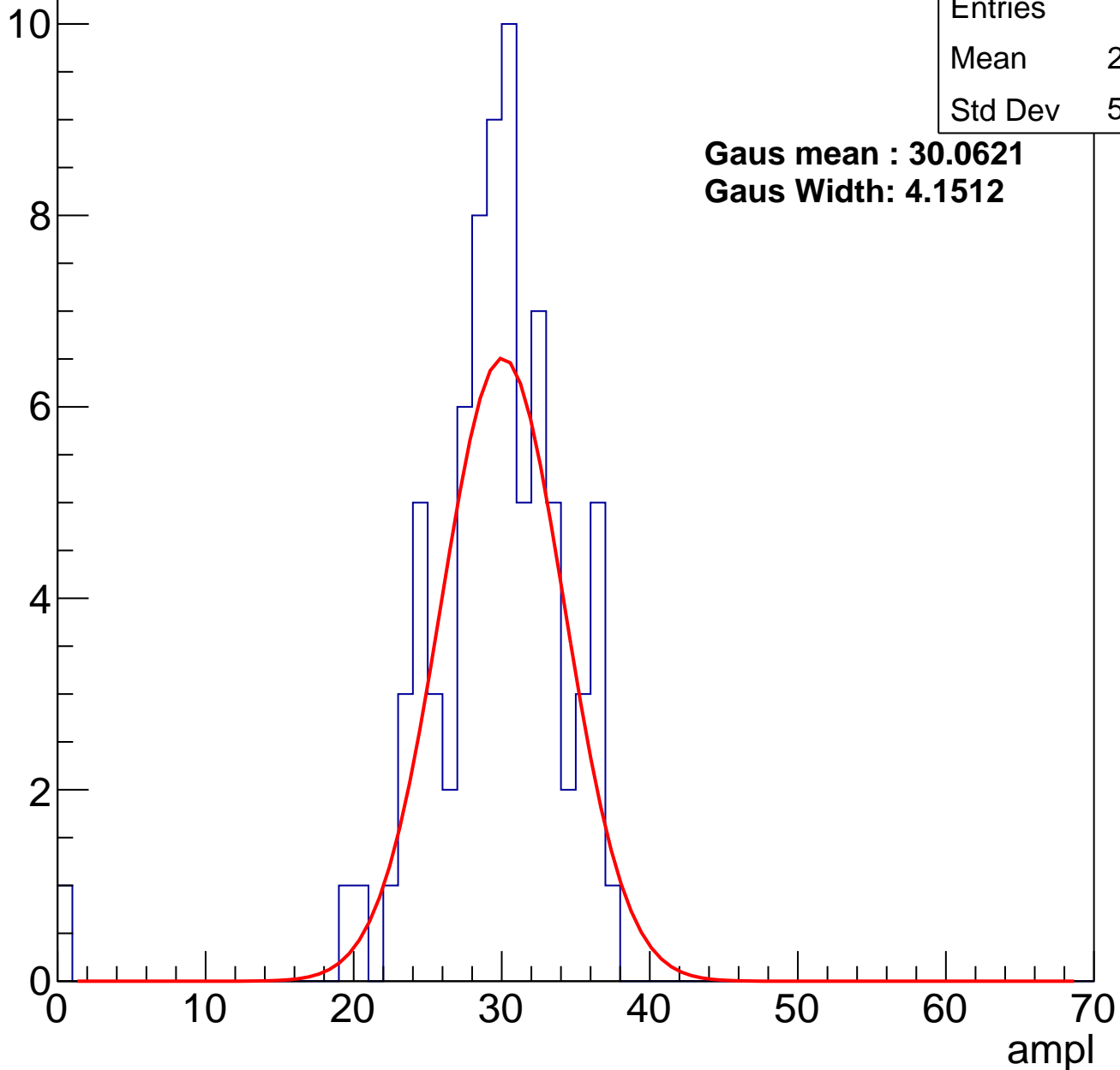
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	78
Mean	28.95
Std Dev	5.116

**Gaus mean : 30.0621**

**Gaus Width: 4.1512**

Entry



# B1L103S, U21-ch78, adc1

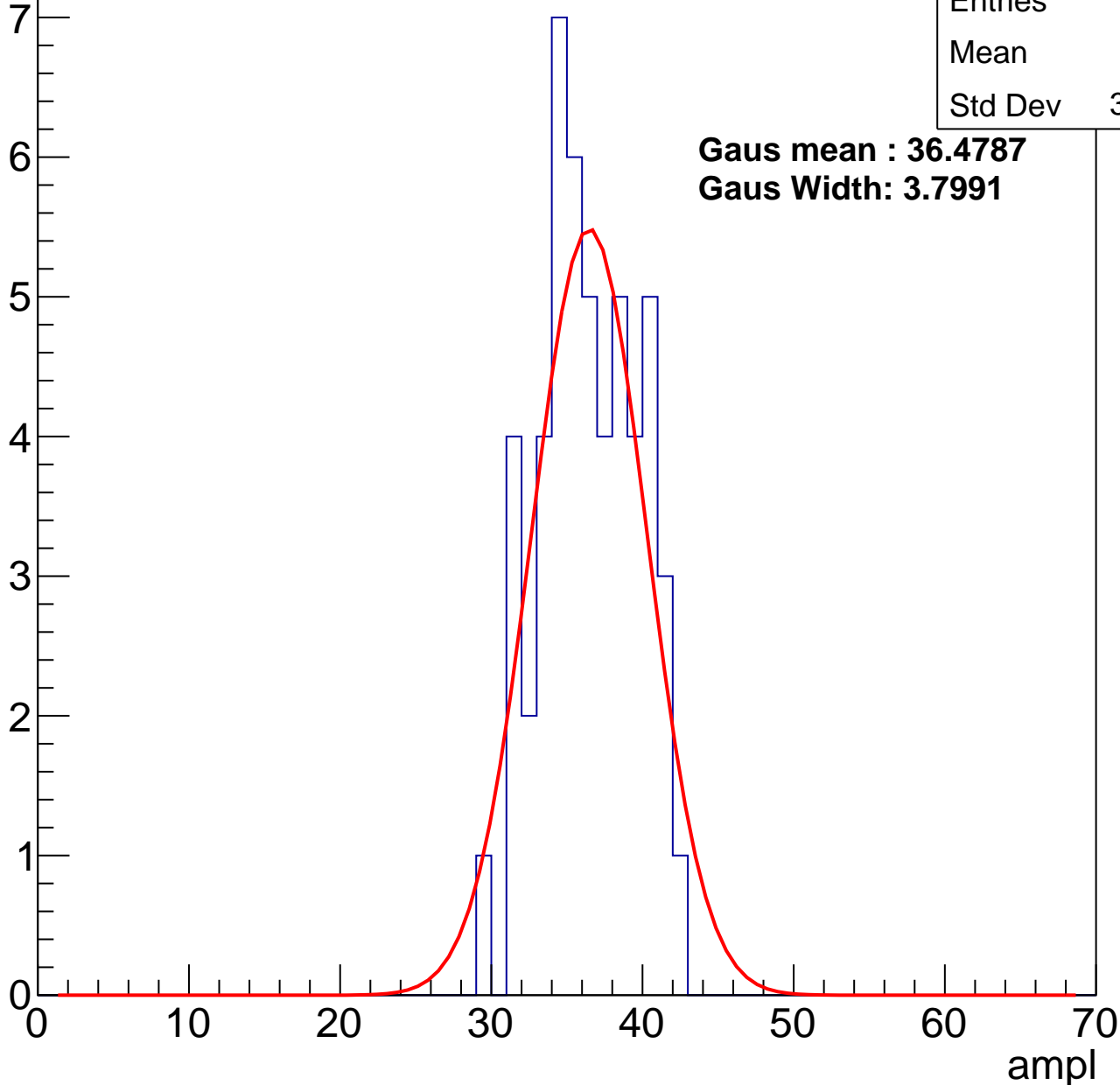
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	36
Std Dev	3.137

**Gaus mean : 36.4787**

**Gaus Width: 3.7991**



# B1L103S, U21-ch78, adc2

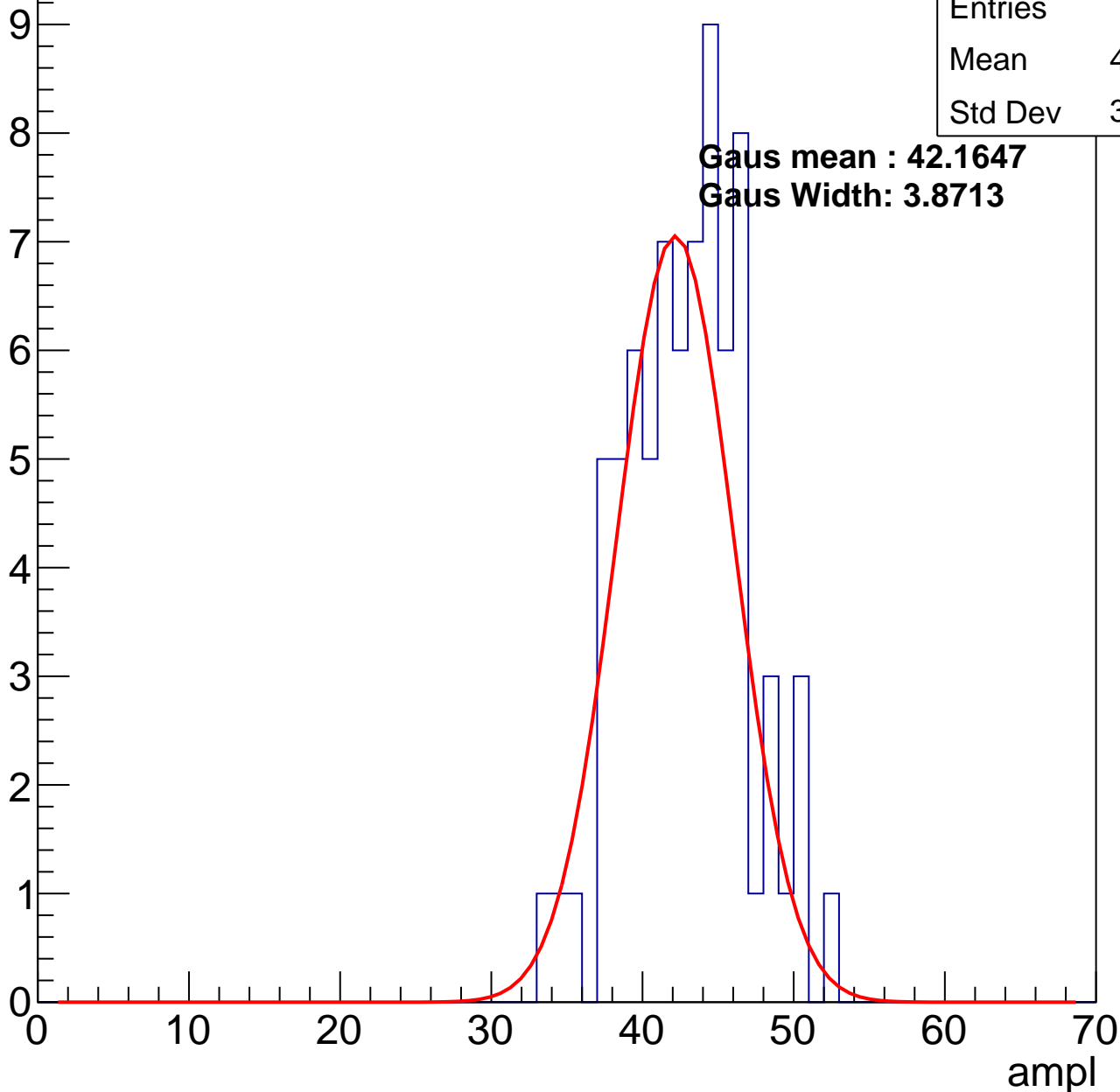
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	42.46
Std Dev	3.912

**Gaus mean : 42.1647**

**Gaus Width: 3.8713**

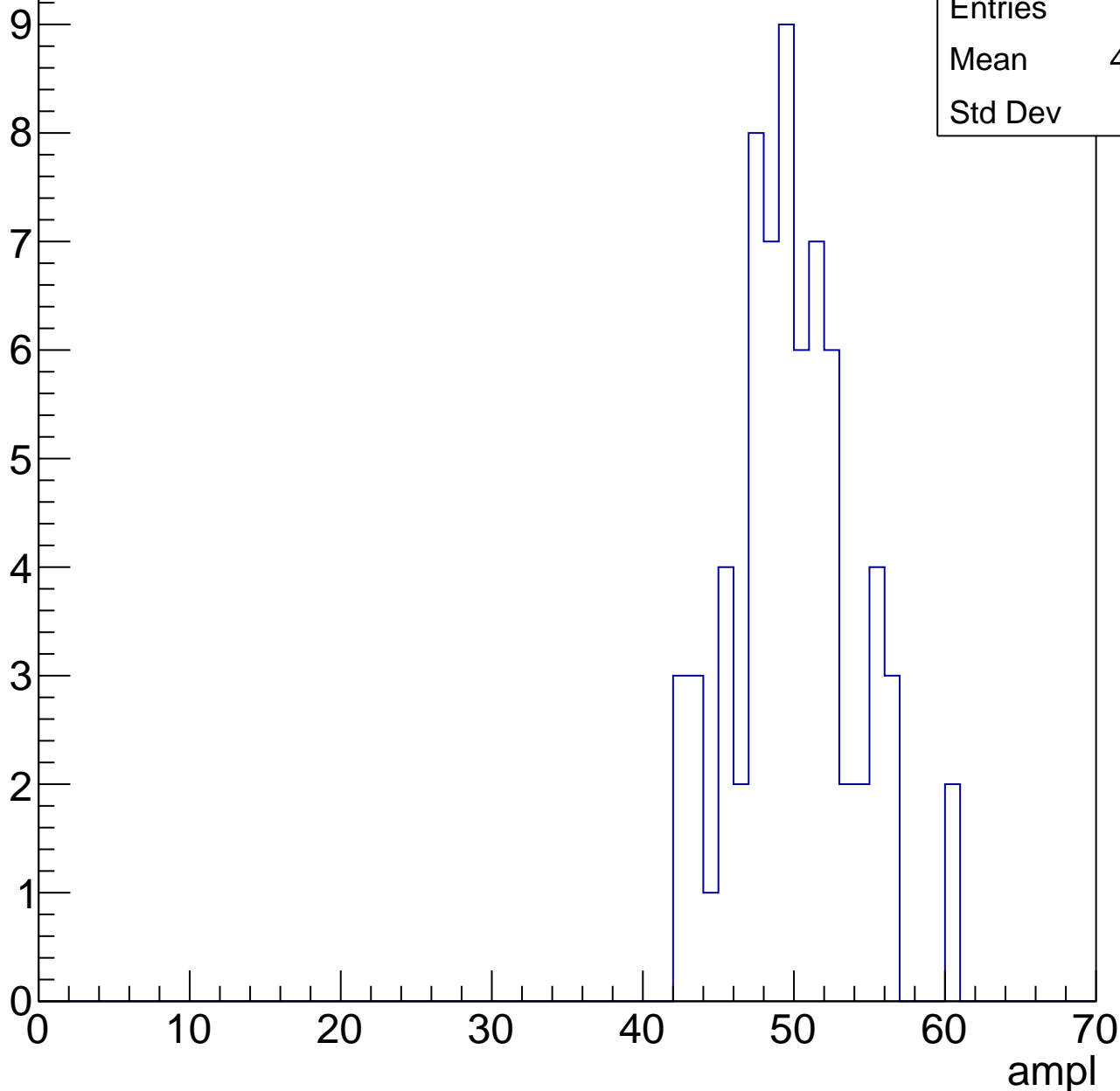


# B1L103S, U21-ch78, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	49.49
Std Dev	3.97

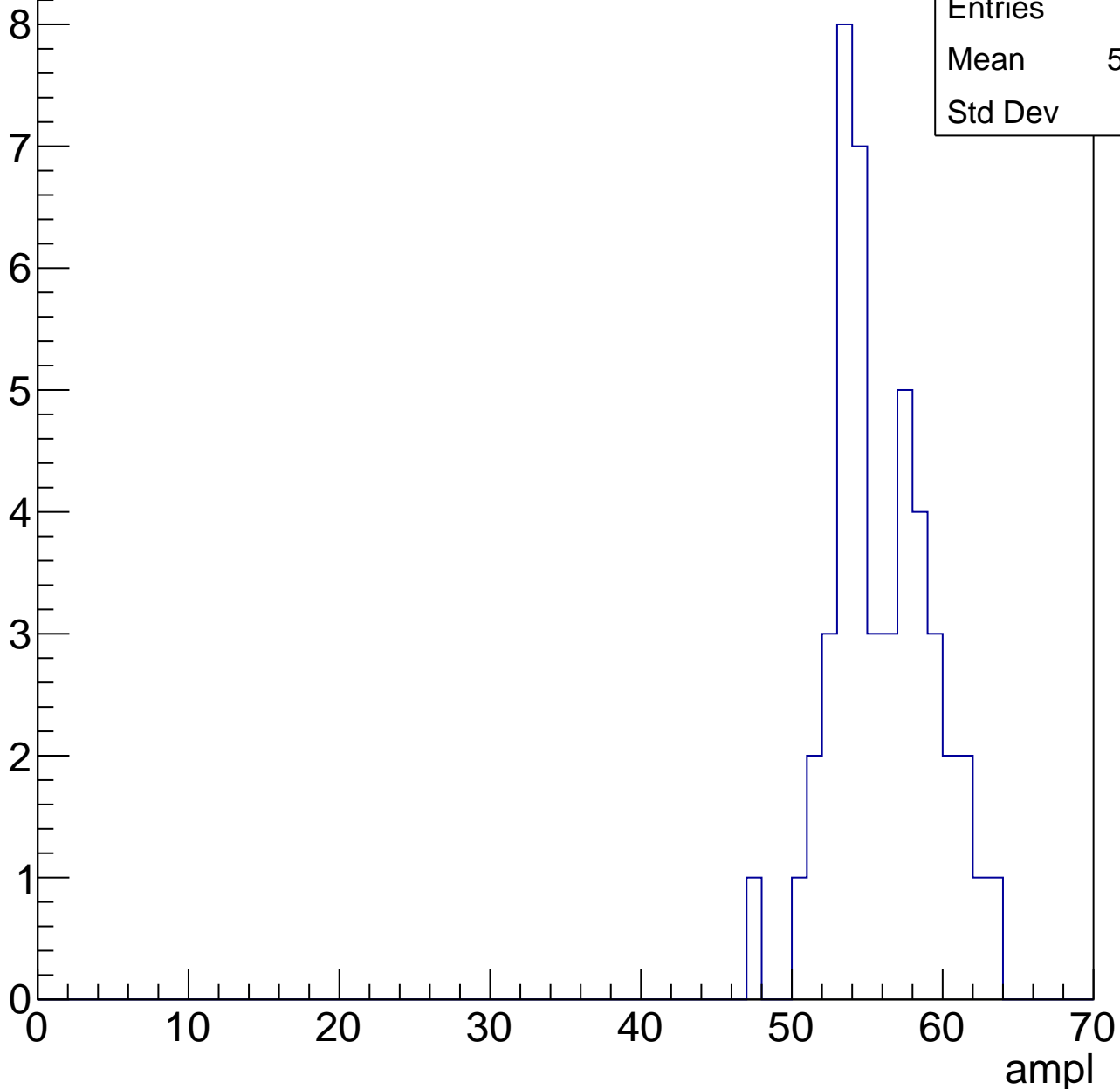


# B1L103S, U21-ch78, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	46
Mean	55.46
Std Dev	3.36

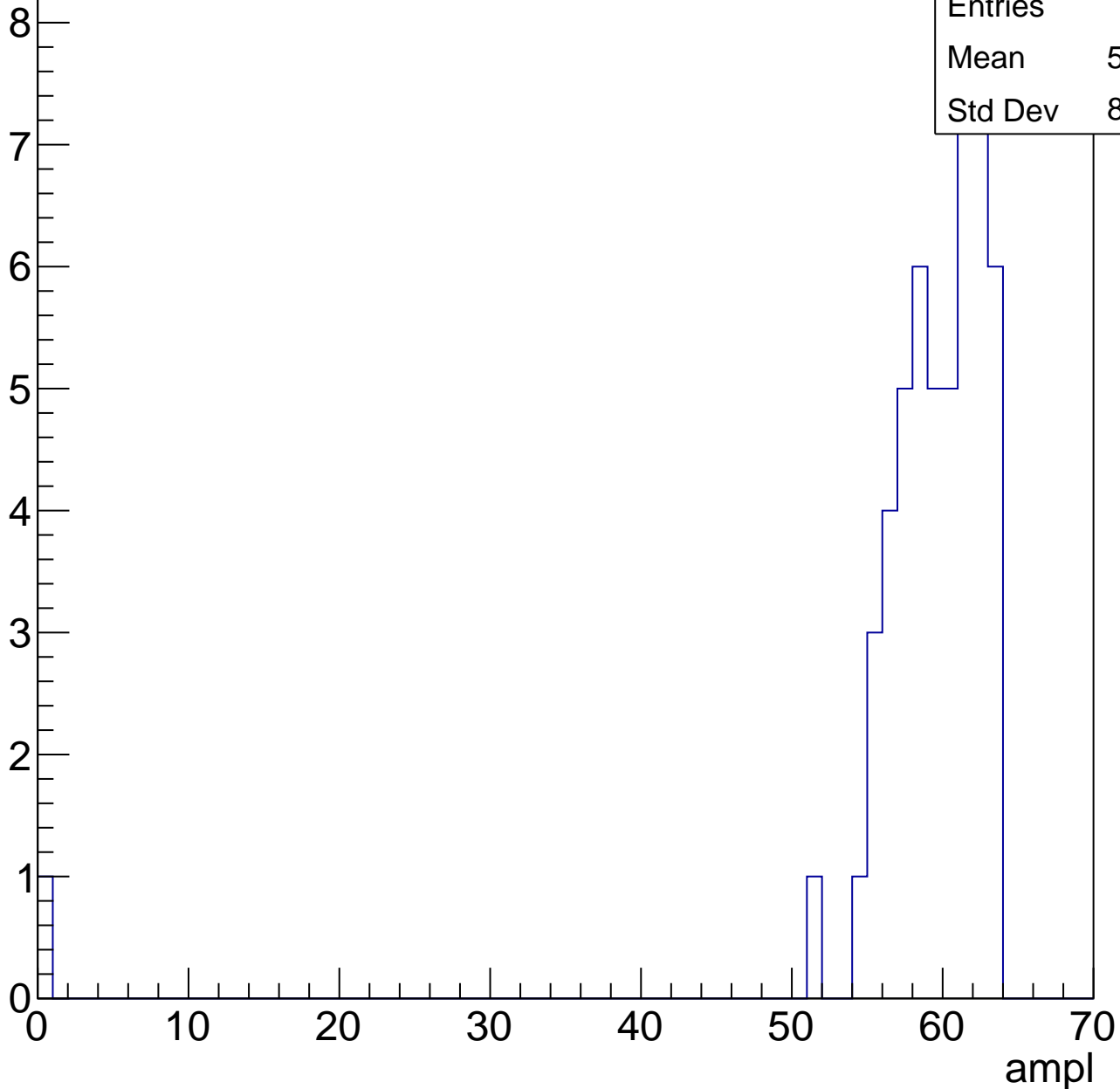


# B1L103S, U21-ch78, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

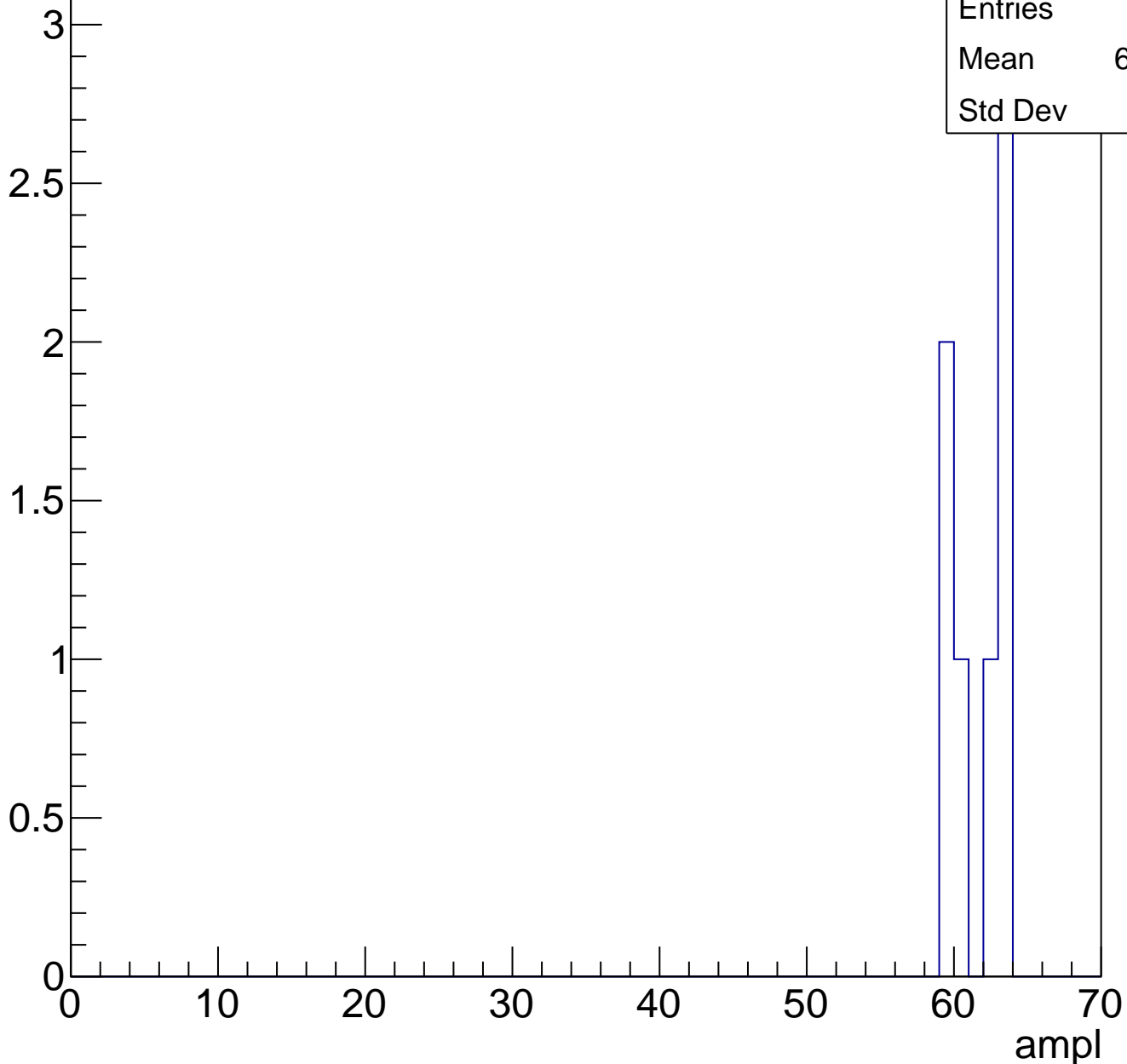
Entries	53
Mean	58.19
Std Dev	8.523



# B1L103S, U21-ch78, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	7
Mean	61.29
Std Dev	1.75



# B1L103S, U21-ch78, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U21-ch79, adc0

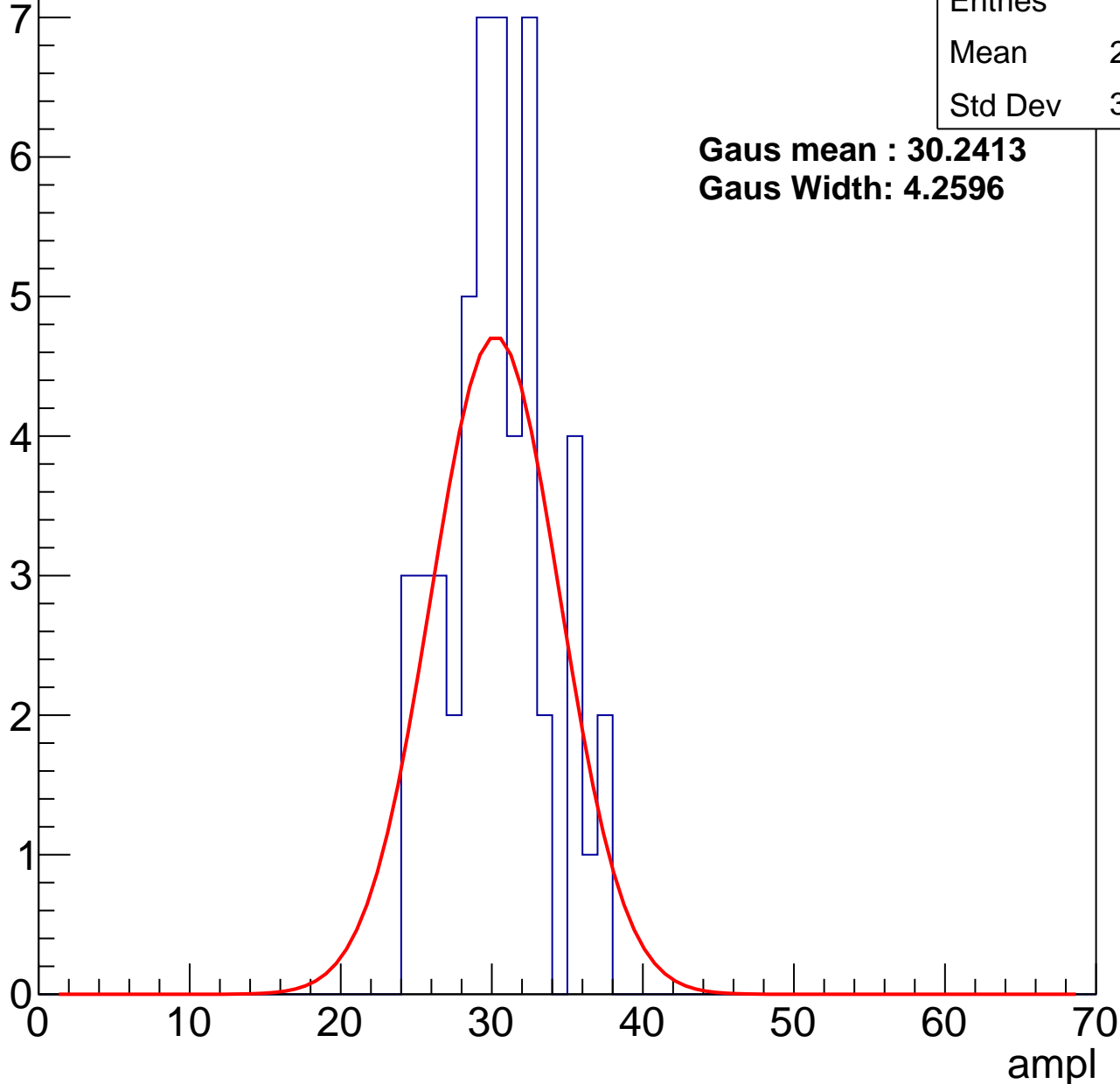
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	29.92
Std Dev	3.346

**Gaus mean : 30.2413**

**Gaus Width: 4.2596**



# B1L103S, U21-ch79, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	61
Mean	35.49
Std Dev	3.865

**Gaus mean : 36.1980**

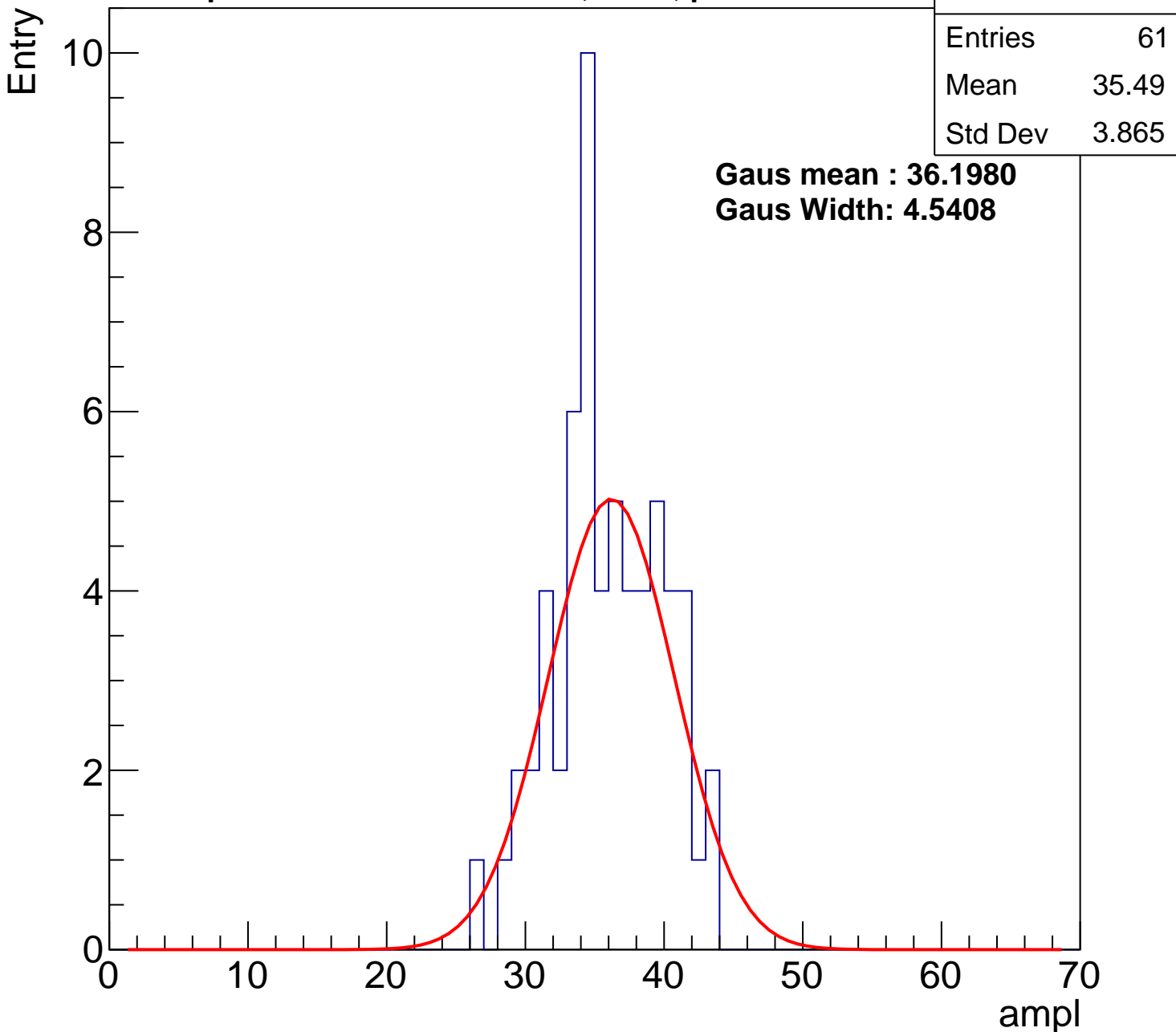
**Gaus Width: 4.5408**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U21-ch79, adc2

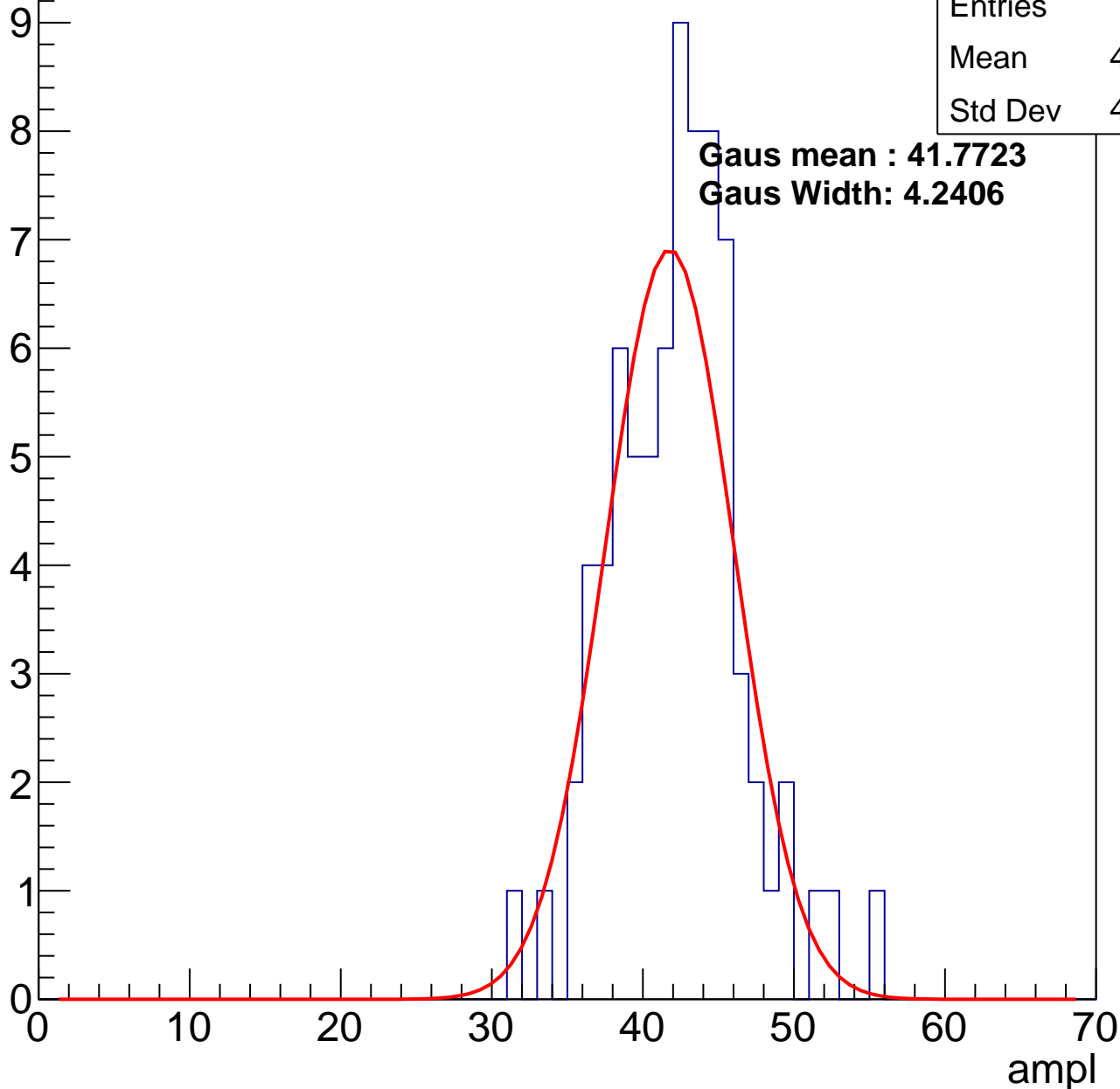
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	41.82
Std Dev	4.254

**Gaus mean : 41.7723**

**Gaus Width: 4.2406**

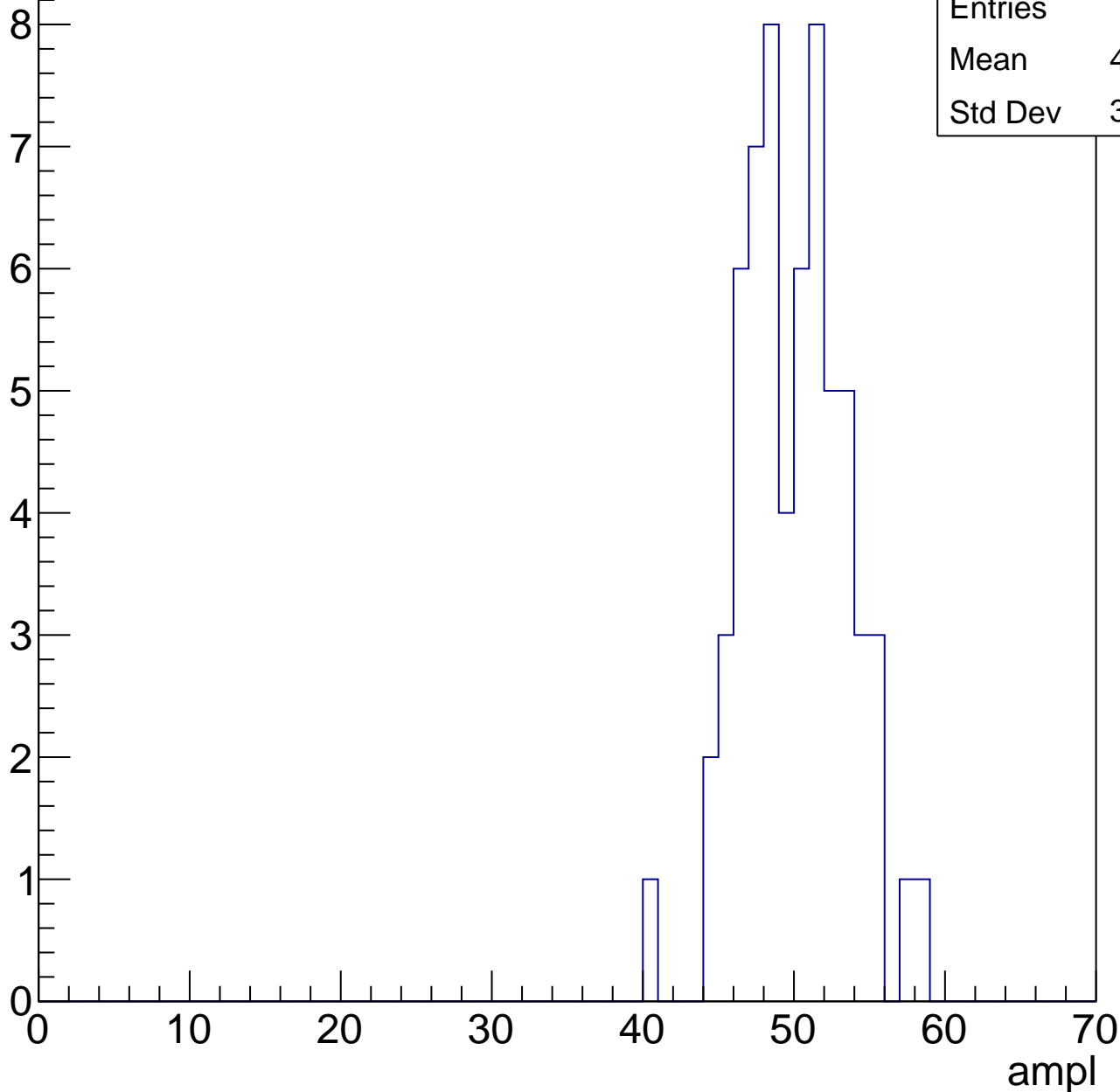


# B1L103S, U21-ch79, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	49.57
Std Dev	3.426

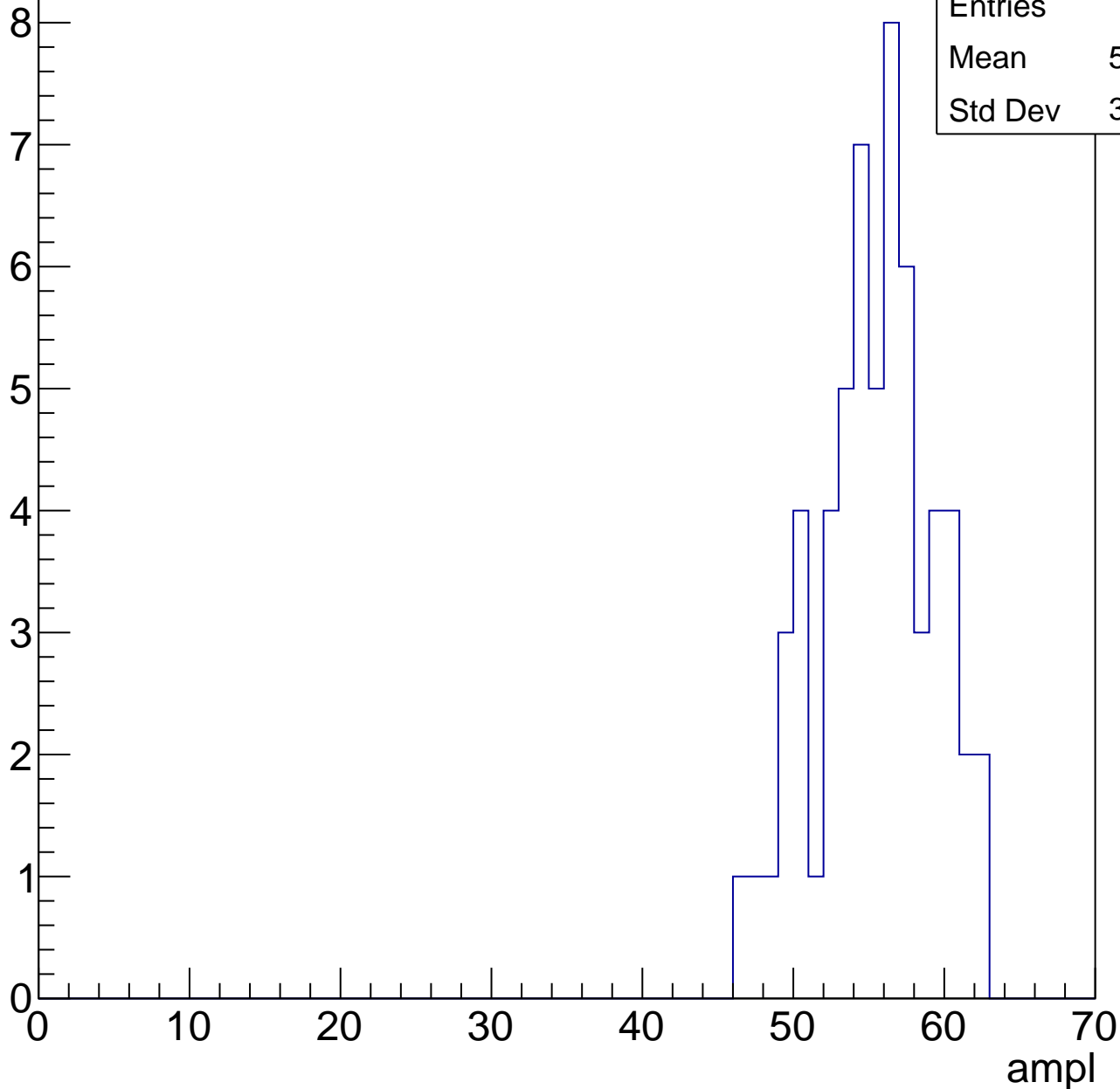


# B1L103S, U21-ch79, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	54.93
Std Dev	3.785

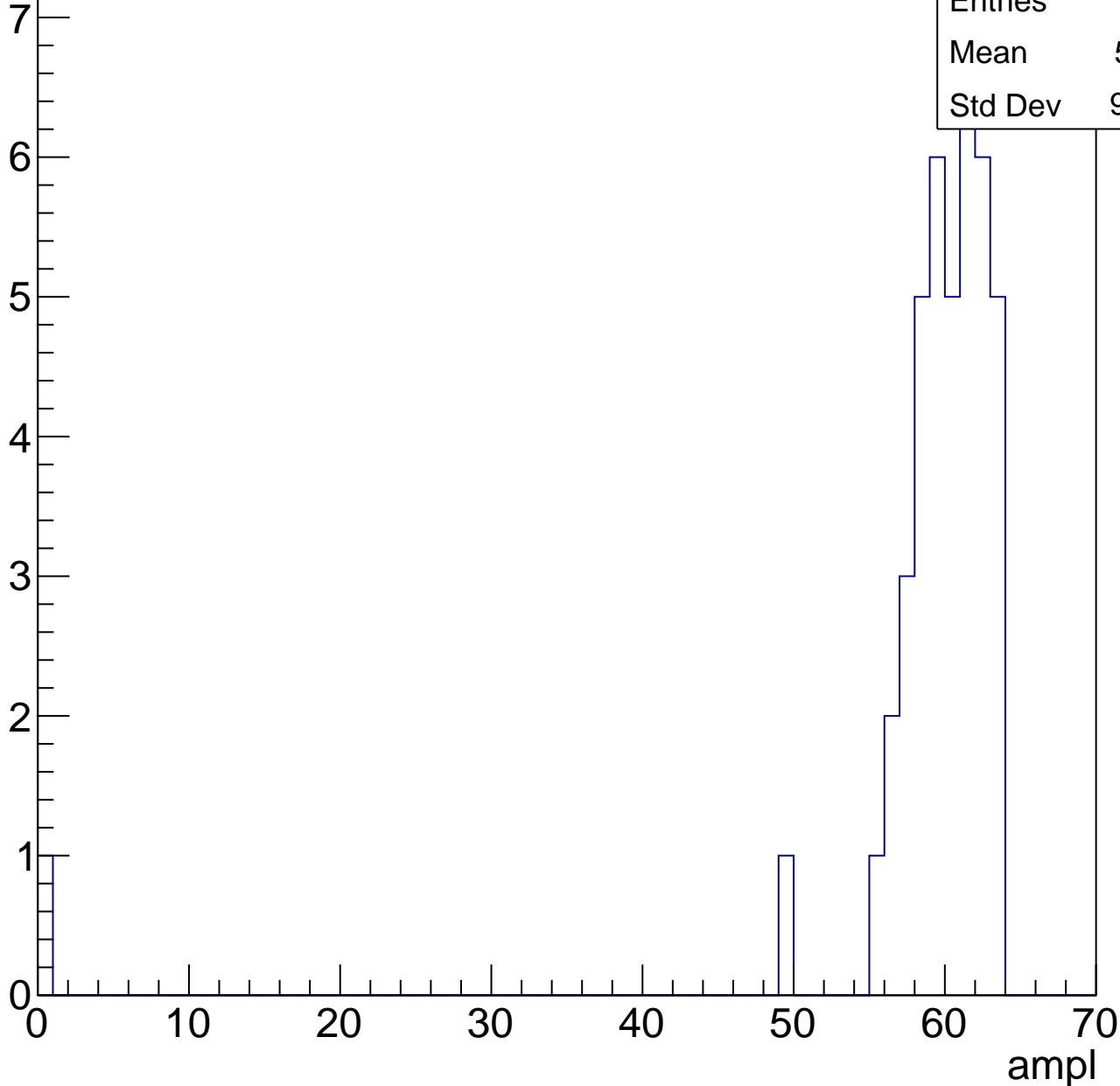


# B1L103S, U21-ch79, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	42
Mean	58.21
Std Dev	9.478

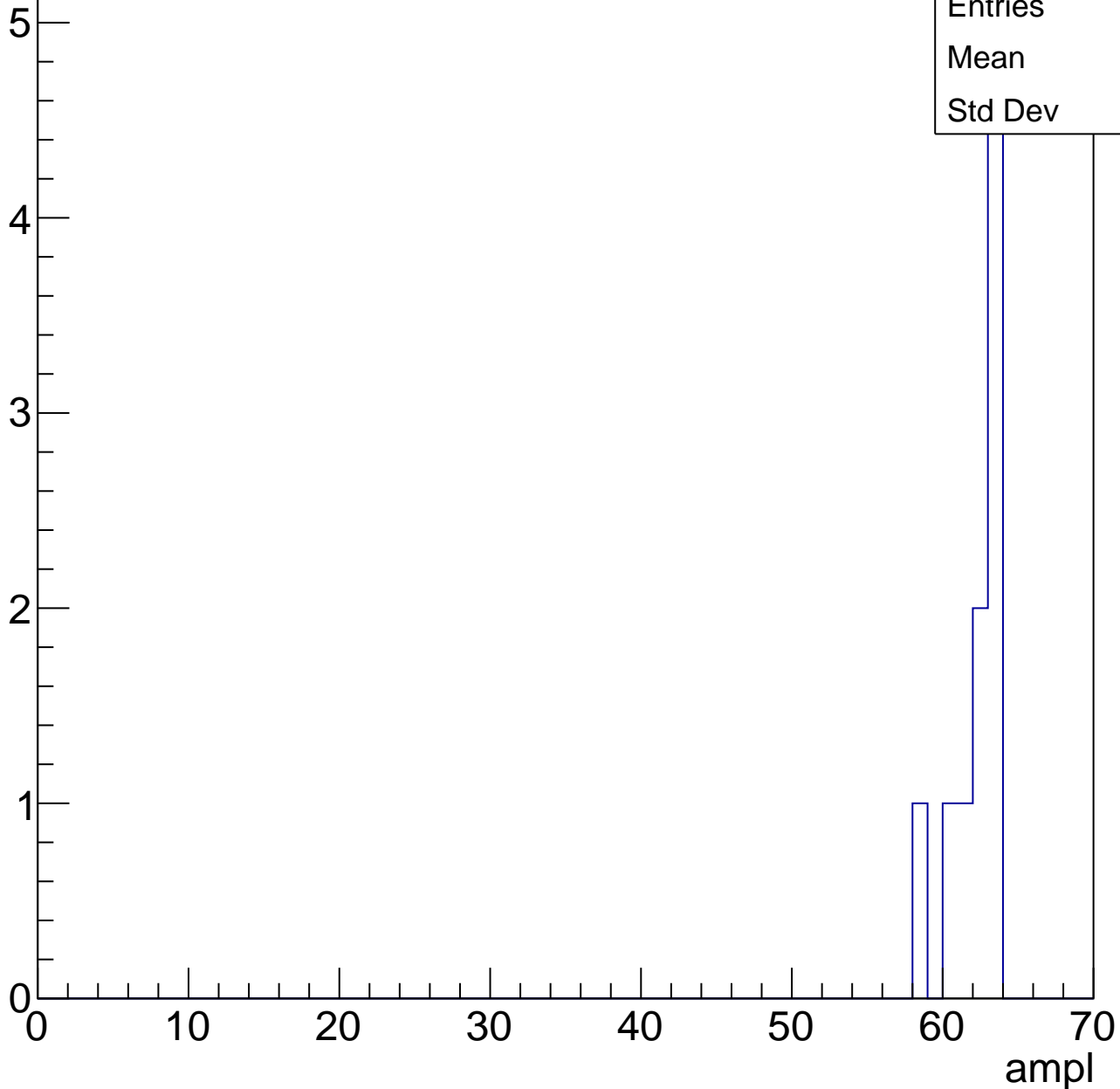


# B1L103S, U21-ch79, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	10
Mean	61.8
Std Dev	1.6





# B1L103S, U21-ch79, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U21-ch80, adc0

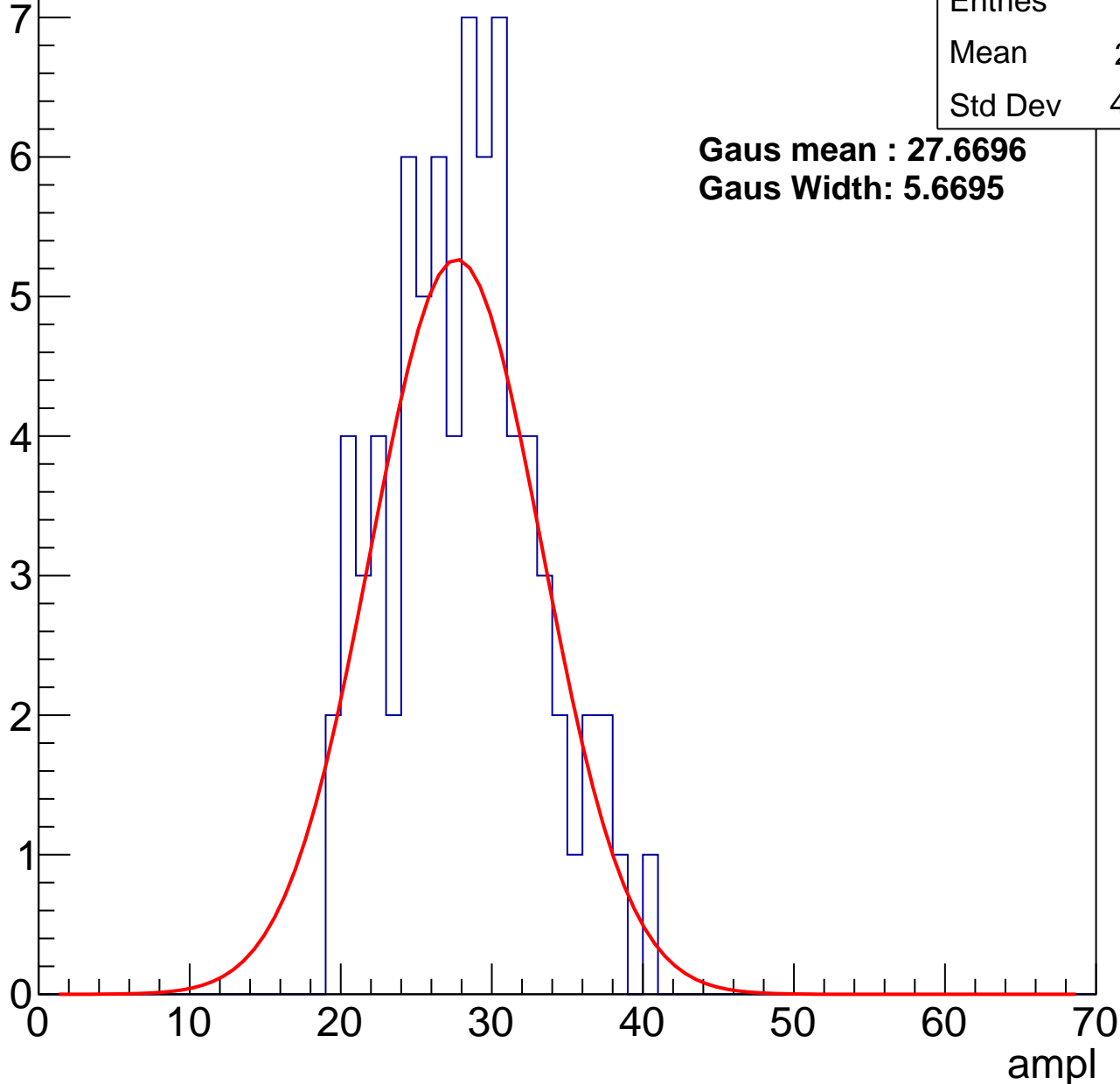
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	27.71
Std Dev	4.847

**Gaus mean : 27.6696**

**Gaus Width: 5.6695**



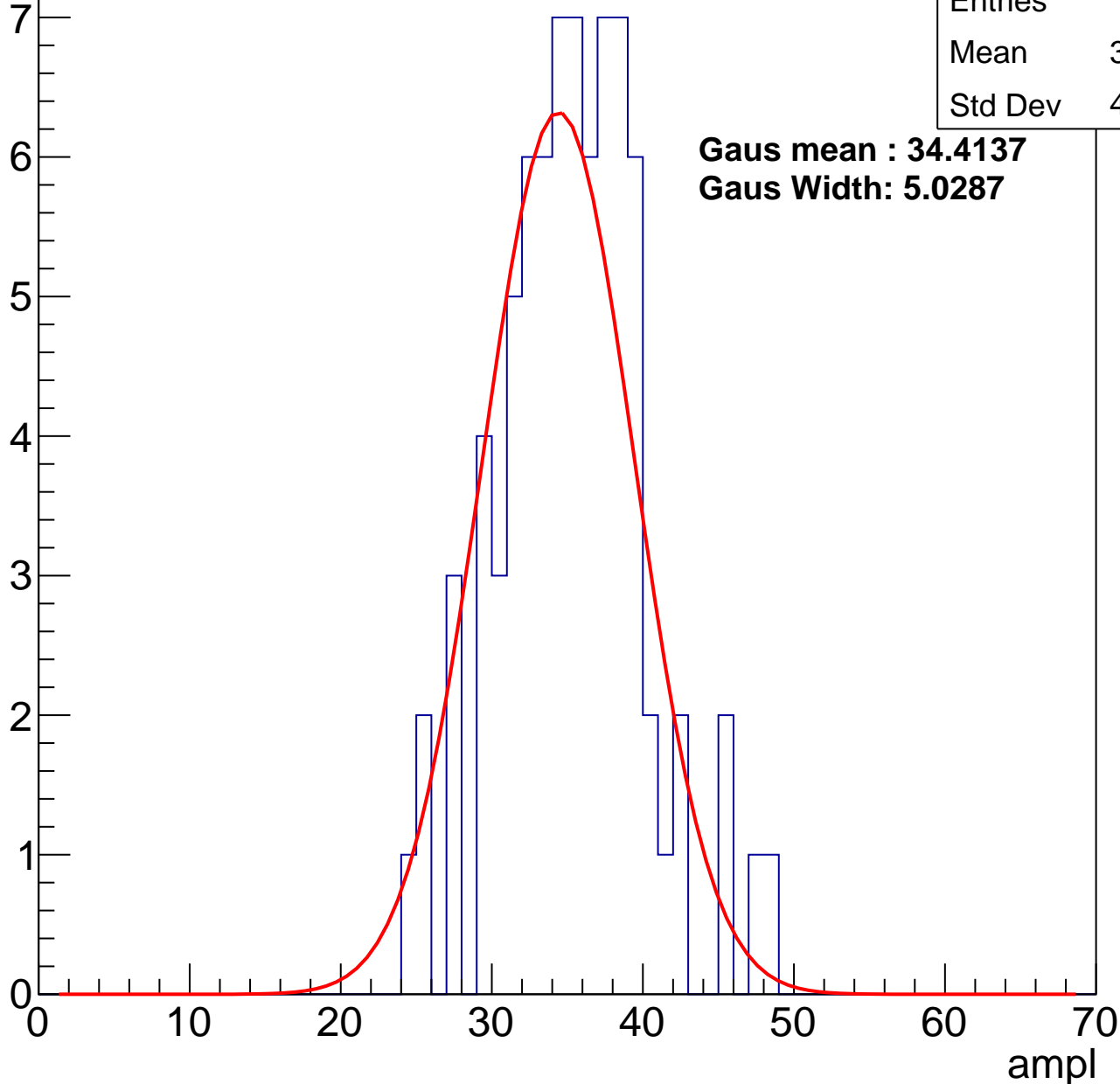
# B1L103S, U21-ch80, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	79
Mean	34.86
Std Dev	4.754

**Gaus mean : 34.4137**  
**Gaus Width: 5.0287**



# B1L103S, U21-ch80, adc2

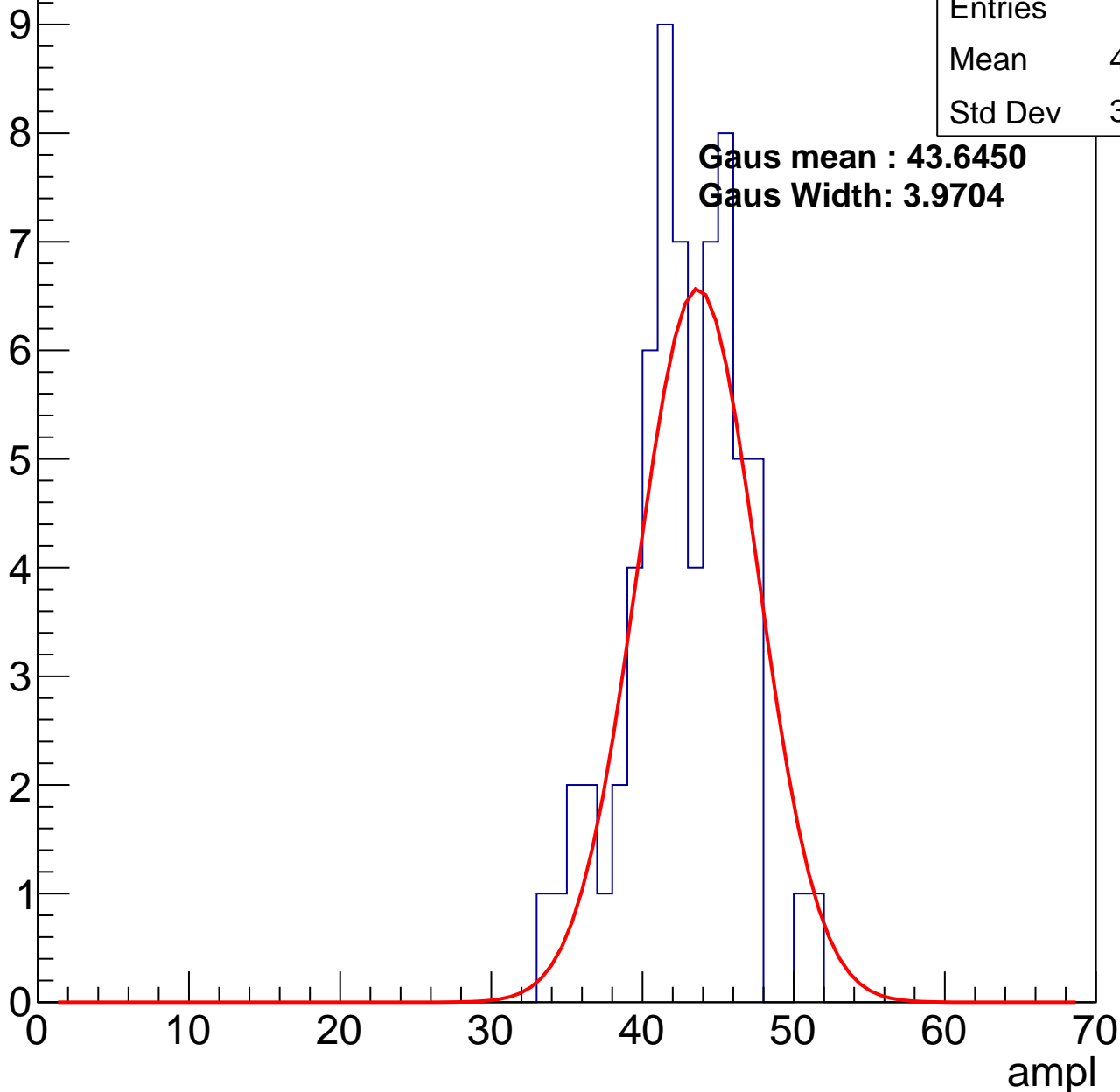
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	42.23
Std Dev	3.675

**Gaus mean : 43.6450**

**Gaus Width: 3.9704**

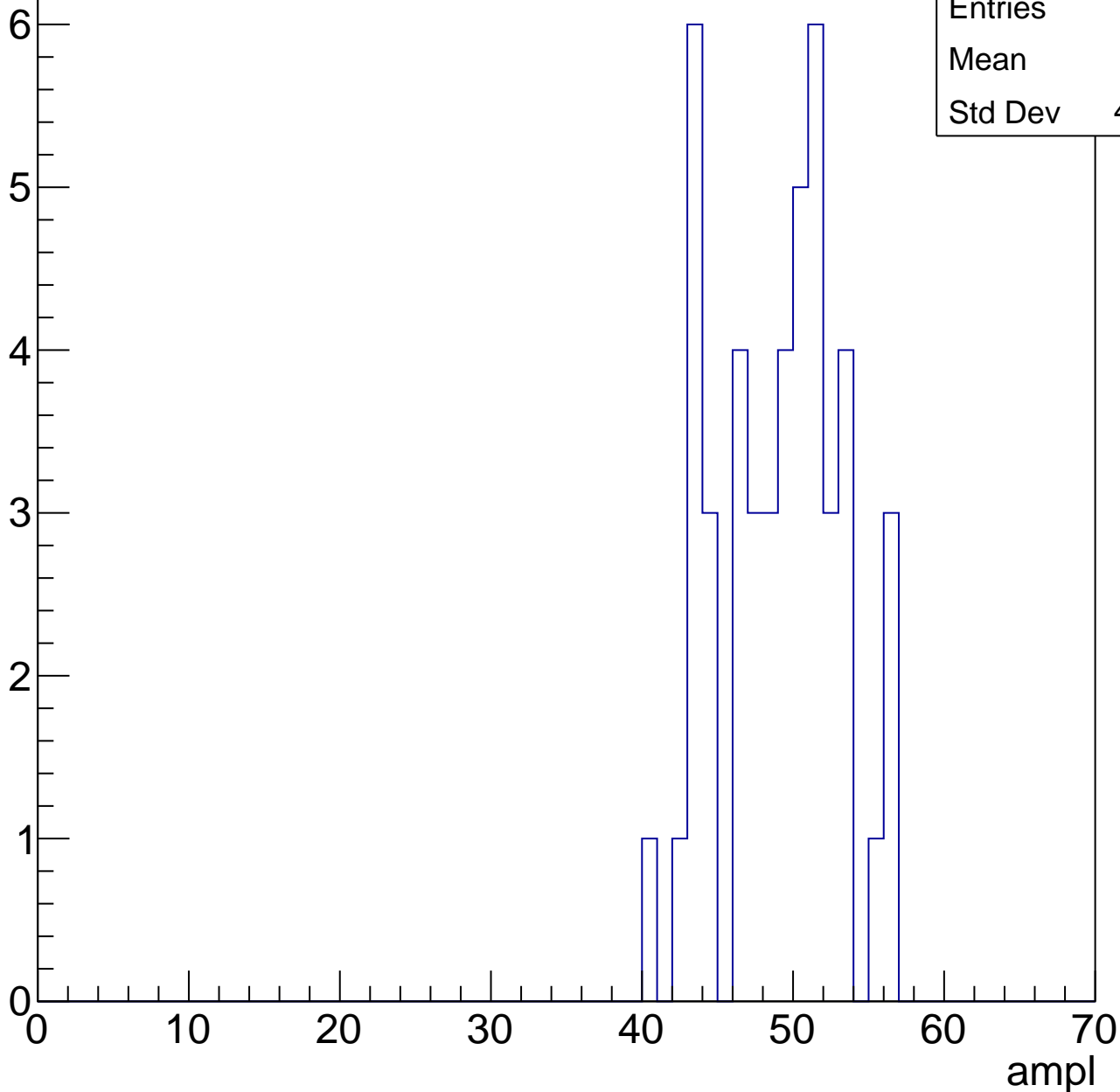


# B1L103S, U21-ch80, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	47
Mean	48.6
Std Dev	4.041

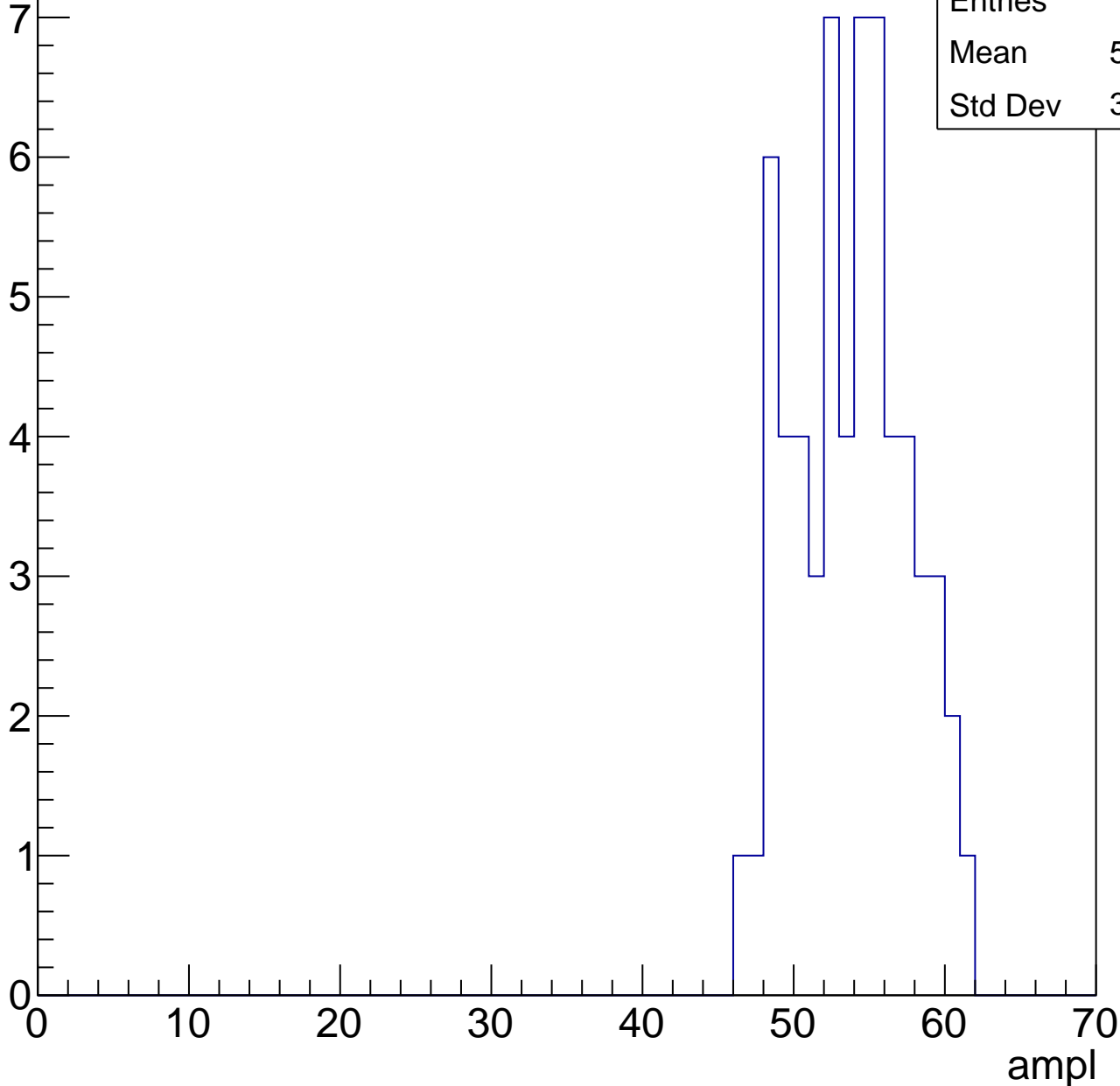


# B1L103S, U21-ch80, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	53.33
Std Dev	3.683

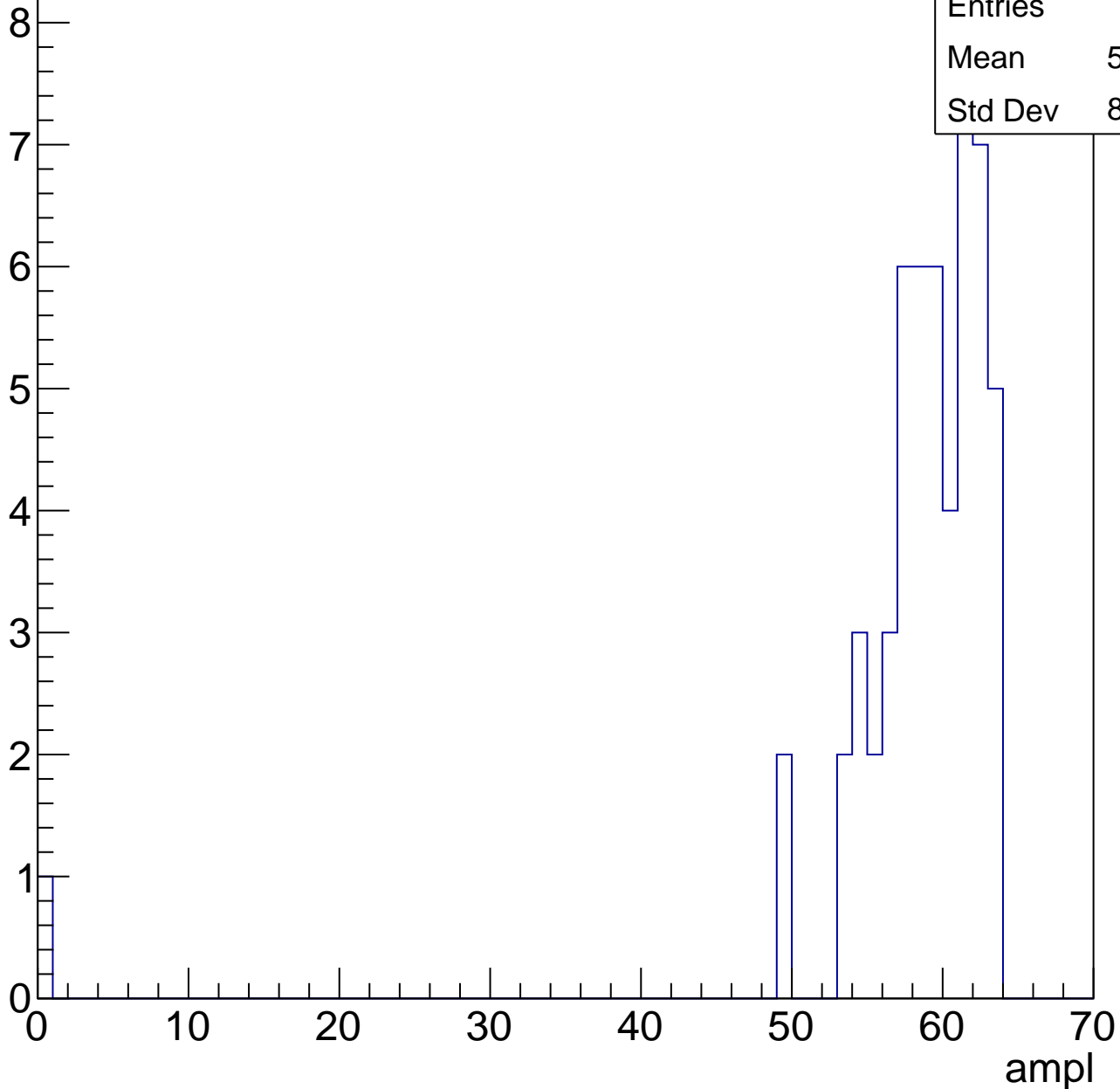


# B1L103S, U21-ch80, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	57.55
Std Dev	8.506

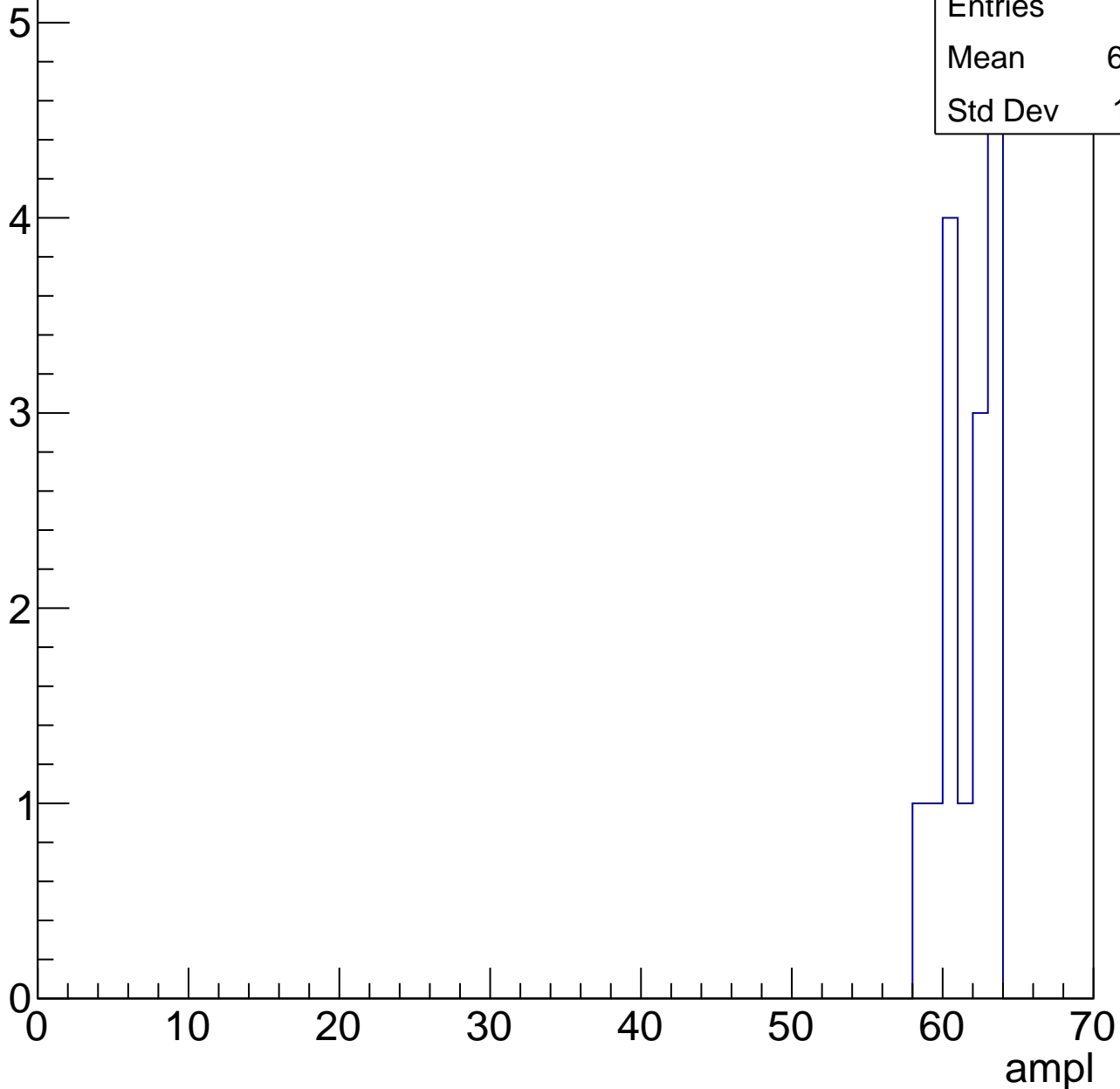


# B1L103S, U21-ch80, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	15
Mean	61.27
Std Dev	1.611





# B1L103S, U21-ch80, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L103S, U21-ch81, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	60
Mean	29.03
Std Dev	5

**Gaus mean : 29.9052**

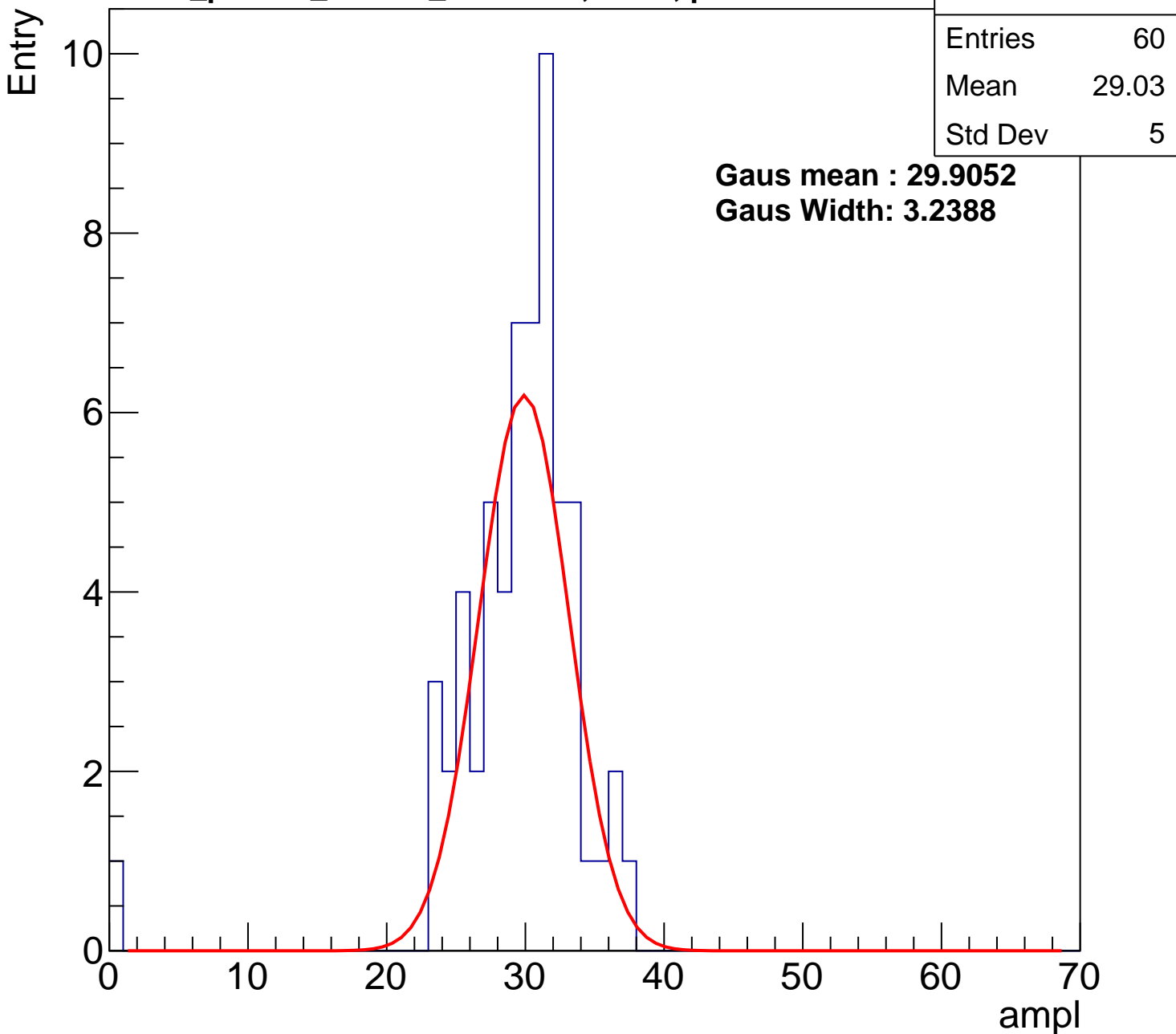
**Gaus Width: 3.2388**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U21-ch81, adc1

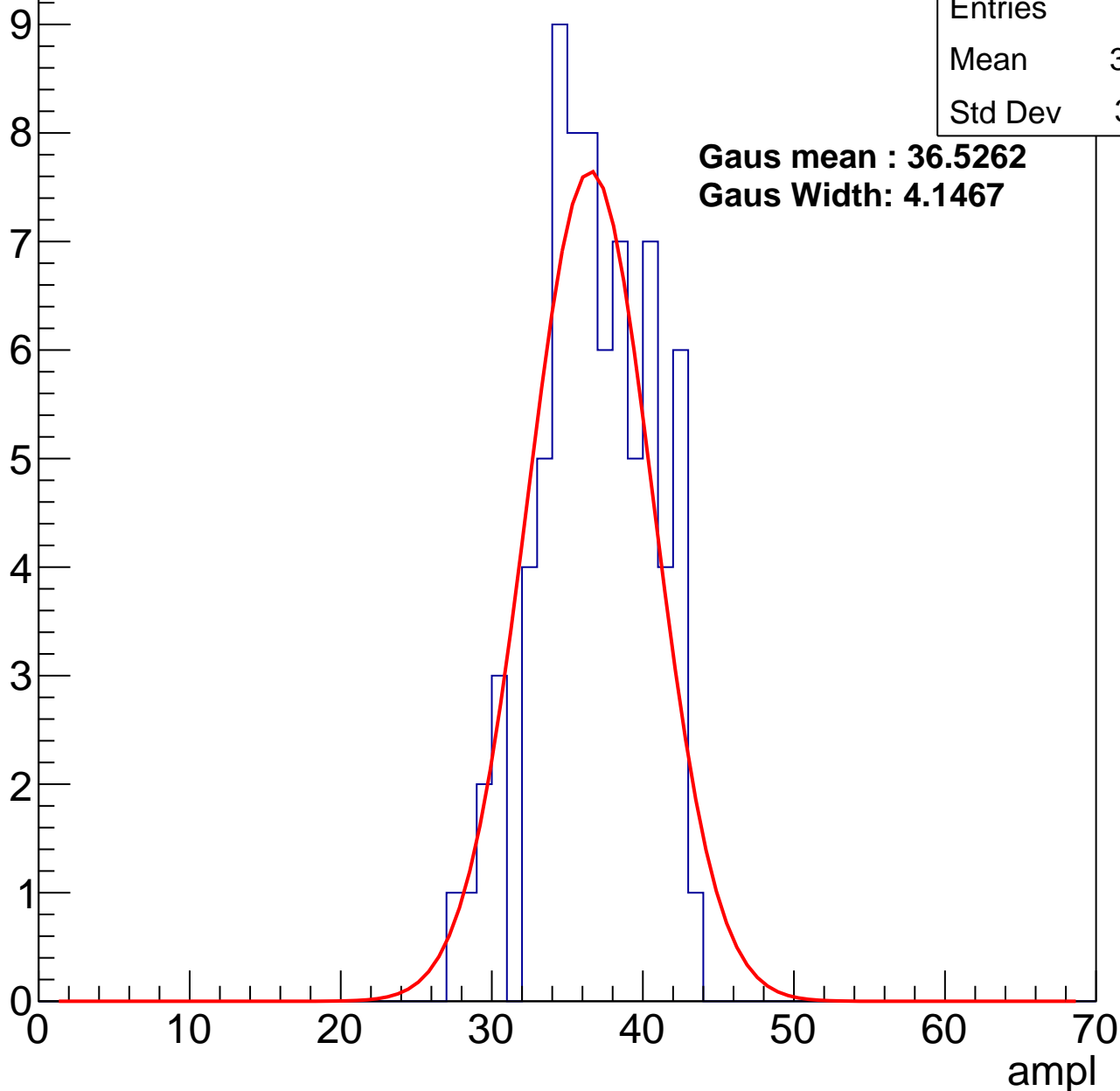
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	36.26
Std Dev	3.701

**Gaus mean : 36.5262**

**Gaus Width: 4.1467**



# B1L103S, U21-ch81, adc2

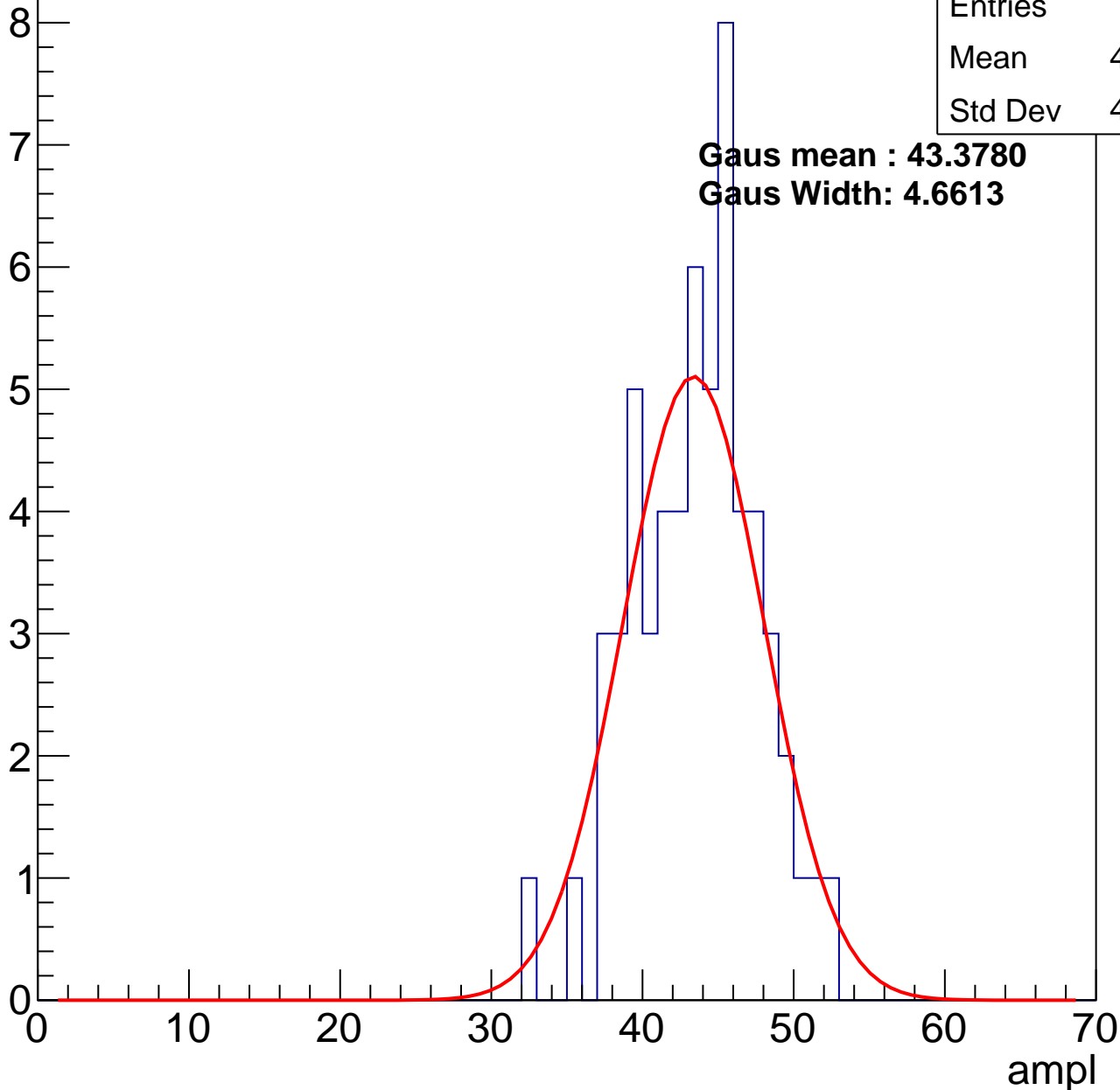
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	43.12
Std Dev	4.059

**Gaus mean : 43.3780**

**Gaus Width: 4.6613**

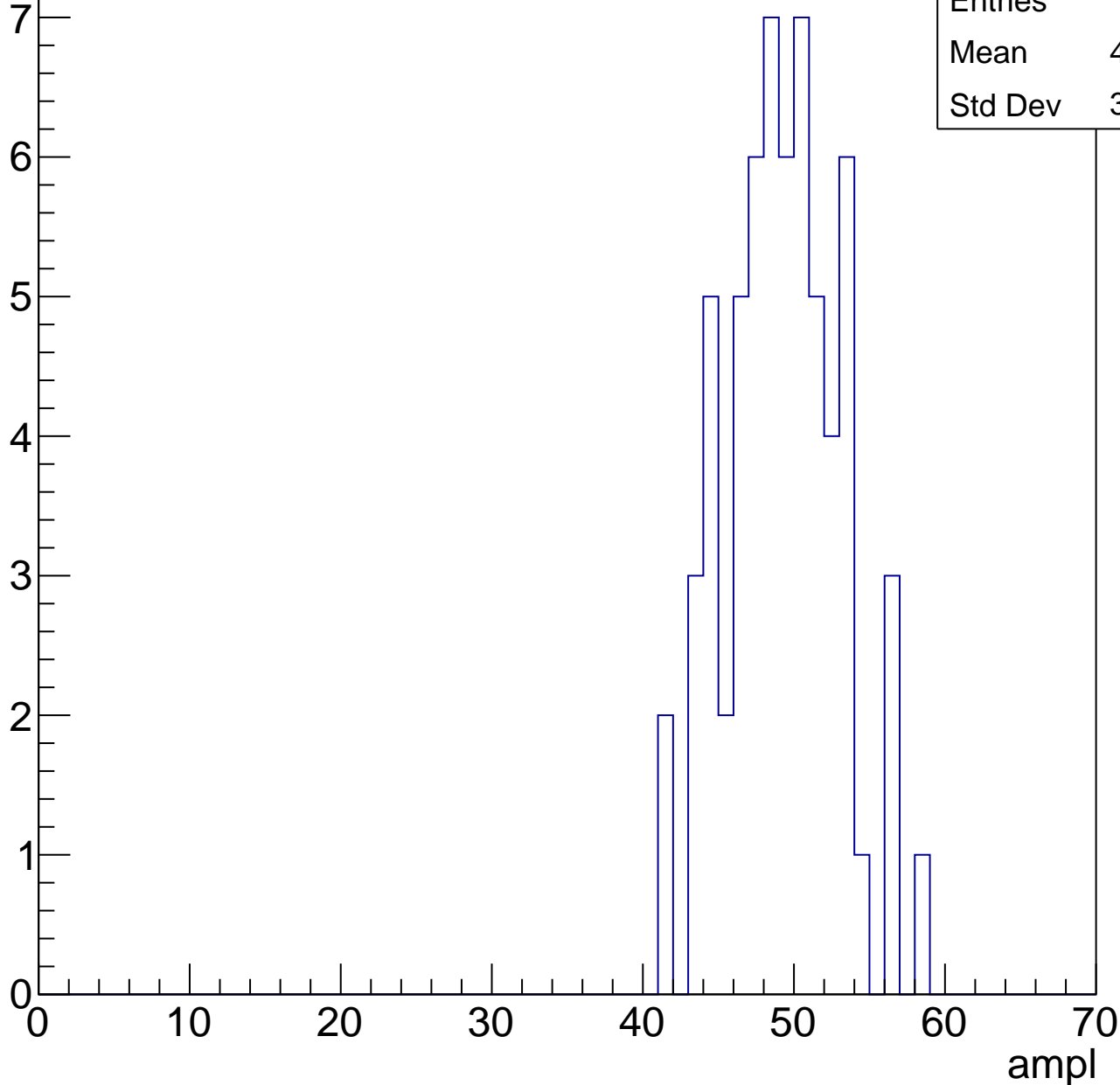


# B1L103S, U21-ch81, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	48.79
Std Dev	3.734

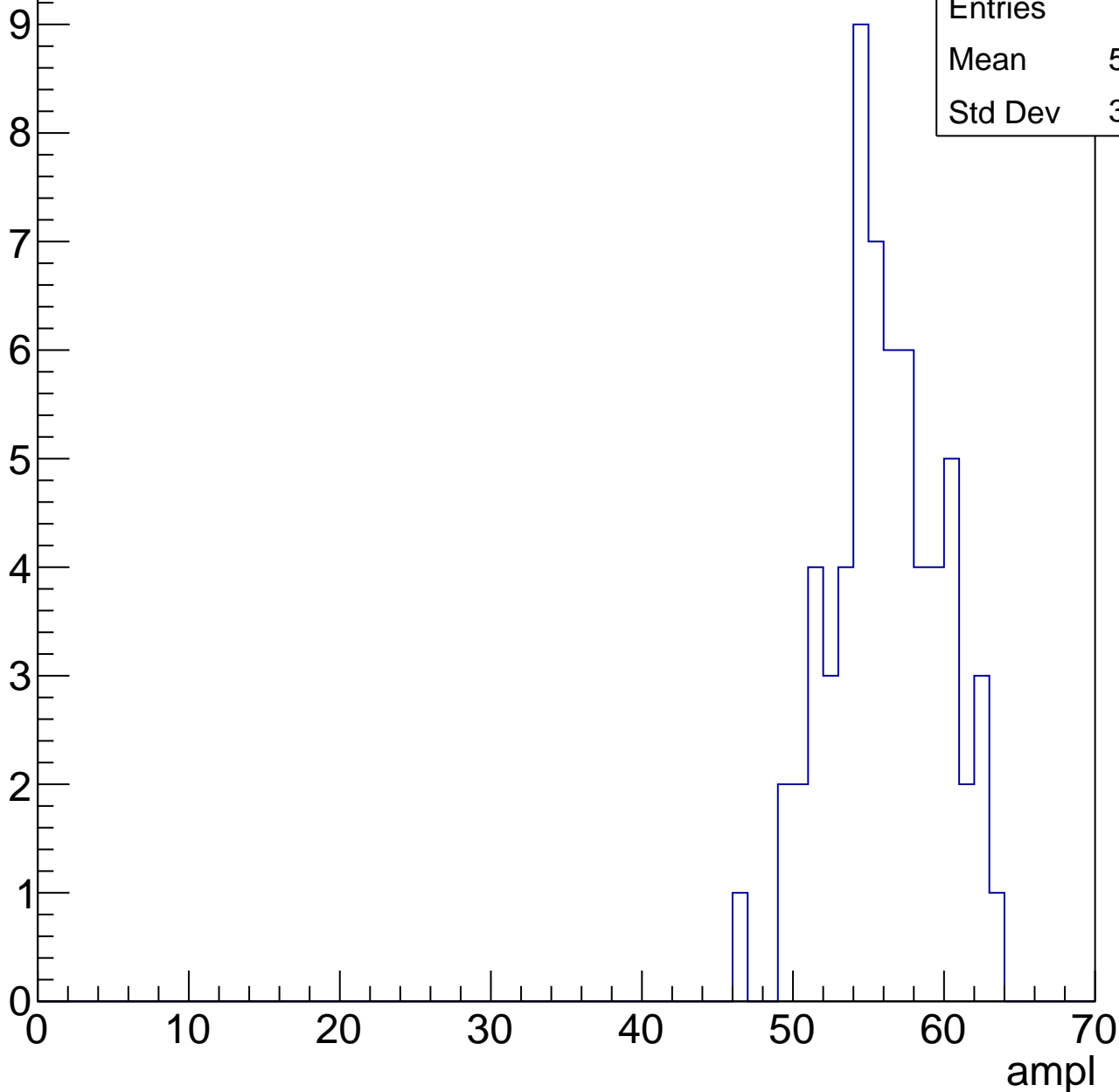


# B1L103S, U21-ch81, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	55.62
Std Dev	3.636

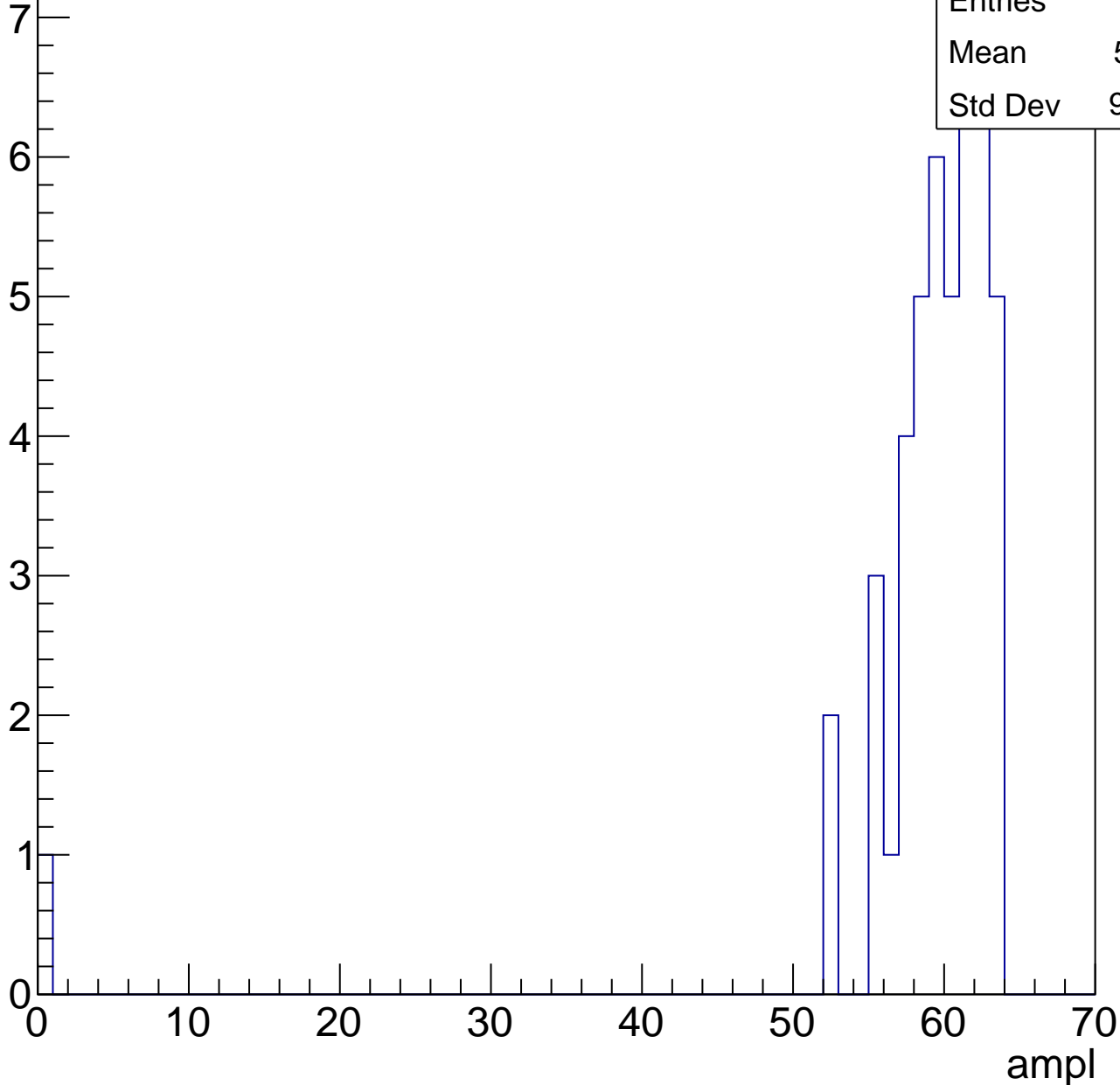


# B1L103S, U21-ch81, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	46
Mean	58.11
Std Dev	9.085



# B1L103S, U21-ch81, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U21-ch81, adc7

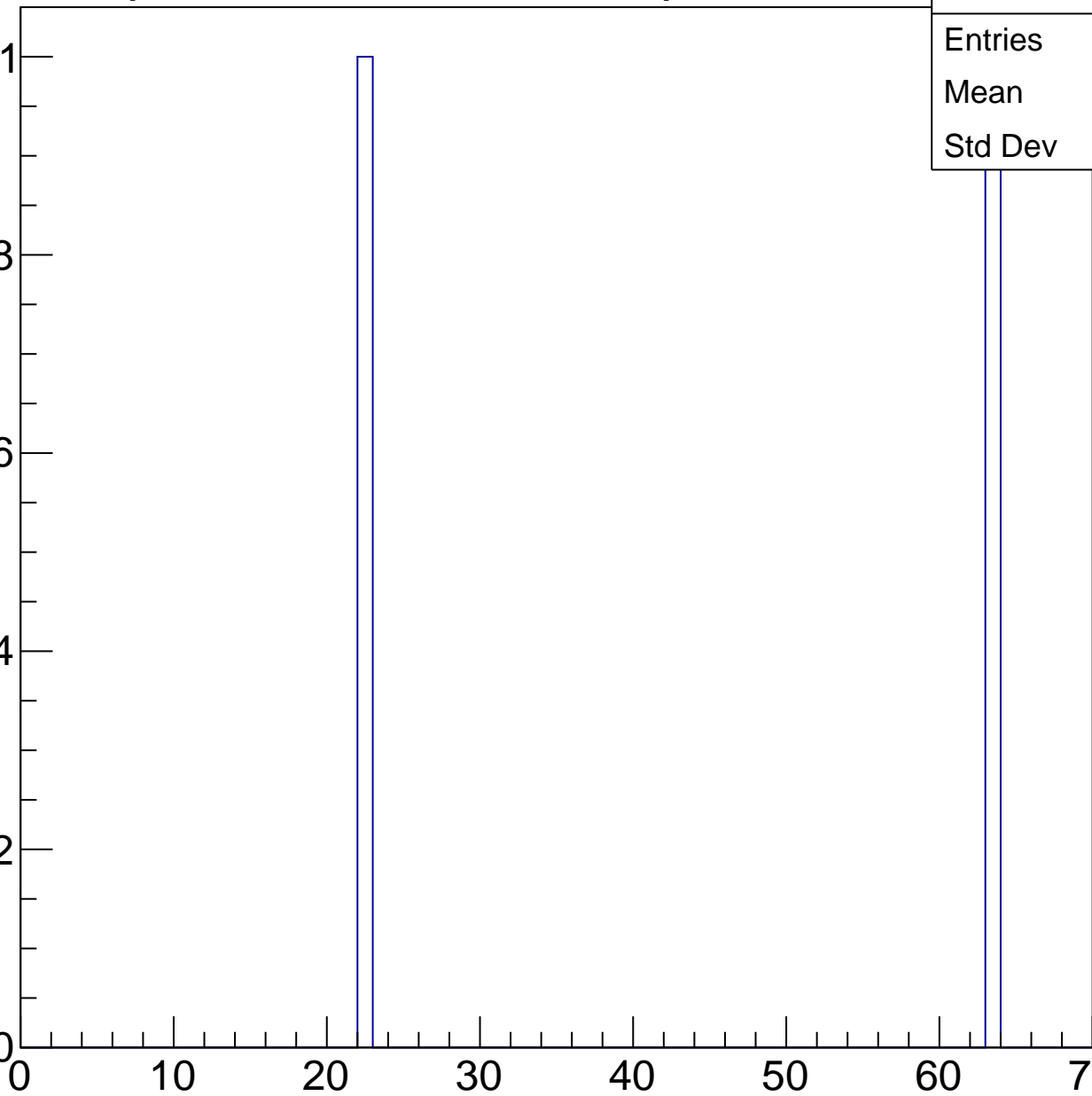
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	42.5
Std Dev	20.5

ampl



# B1L103S, U21-ch82, adc0

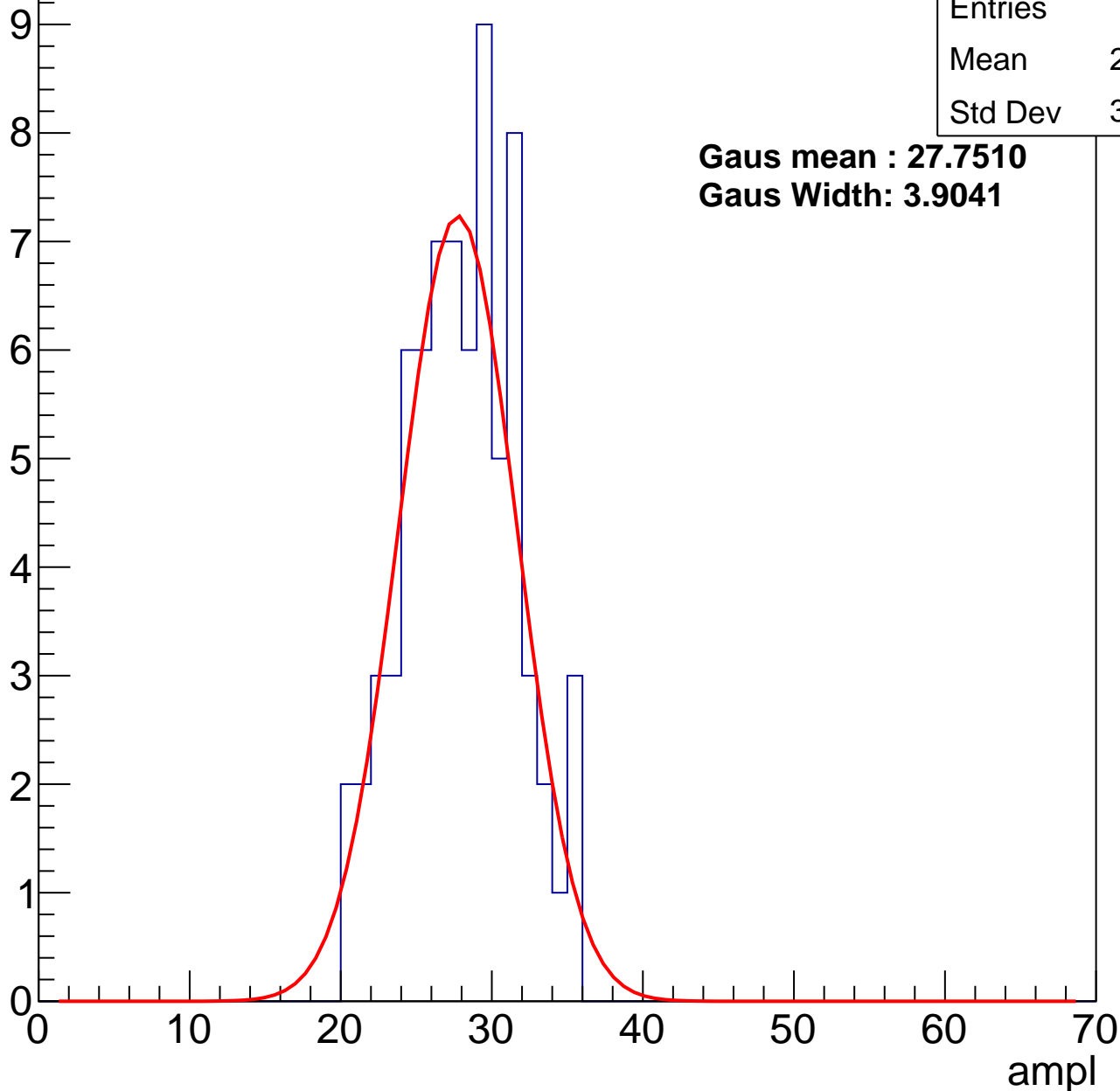
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	27.53
Std Dev	3.627

**Gaus mean : 27.7510**

**Gaus Width: 3.9041**



# B1L103S, U21-ch82, adc1

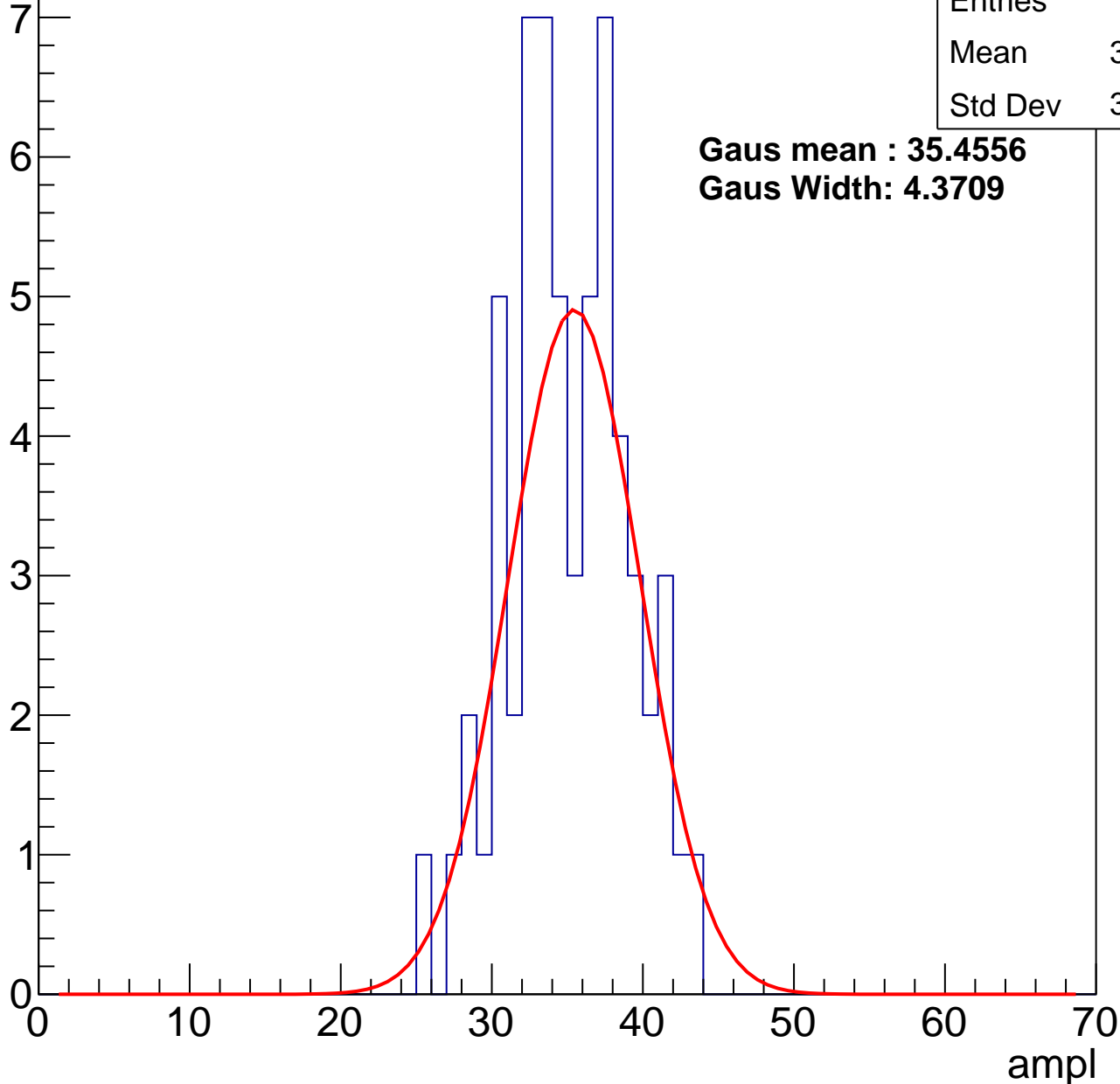
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	34.58
Std Dev	3.934

**Gaus mean : 35.4556**

**Gaus Width: 4.3709**



# B1L103S, U21-ch82, adc2

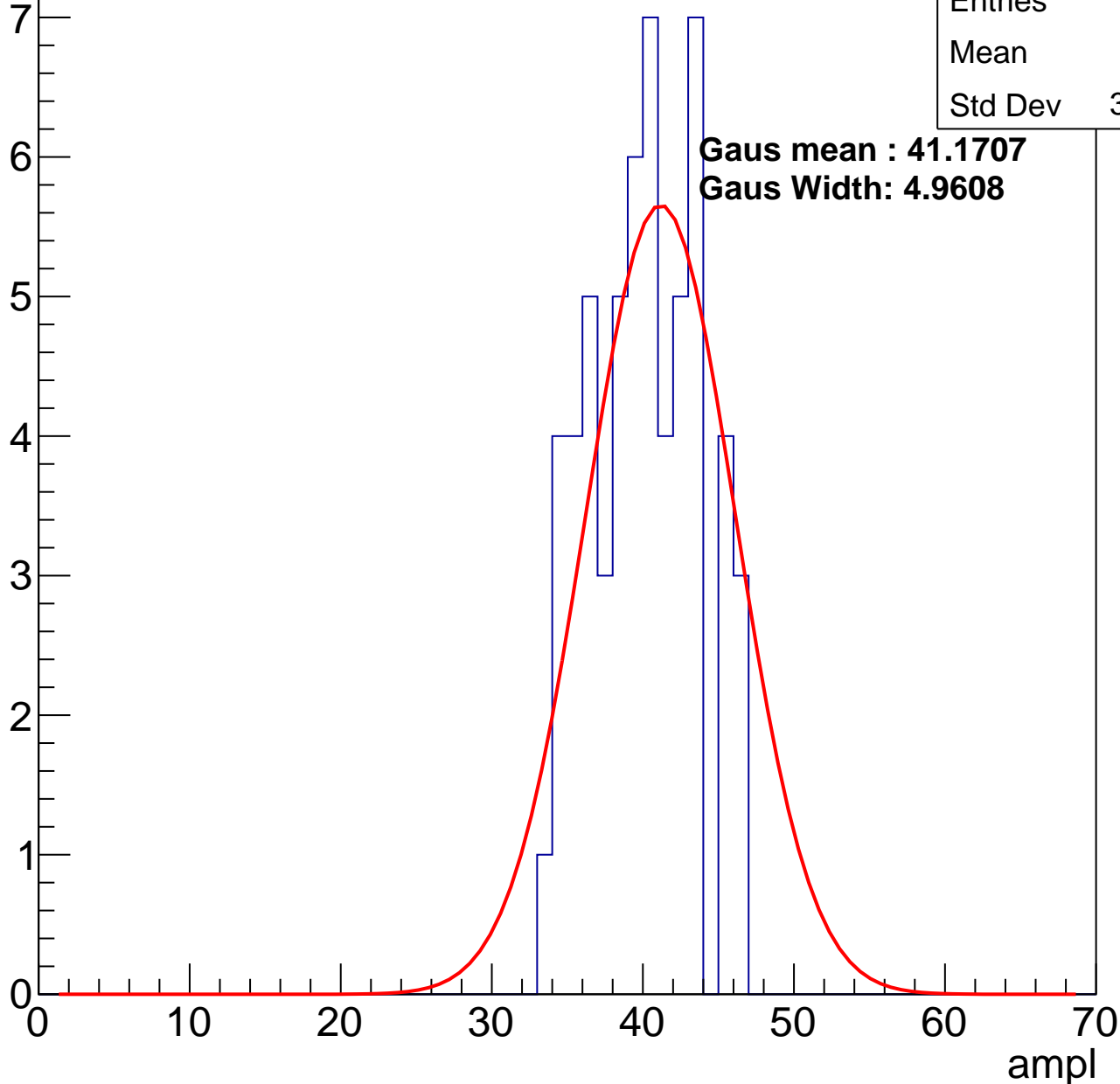
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	39.6
Std Dev	3.503

**Gaus mean : 41.1707**

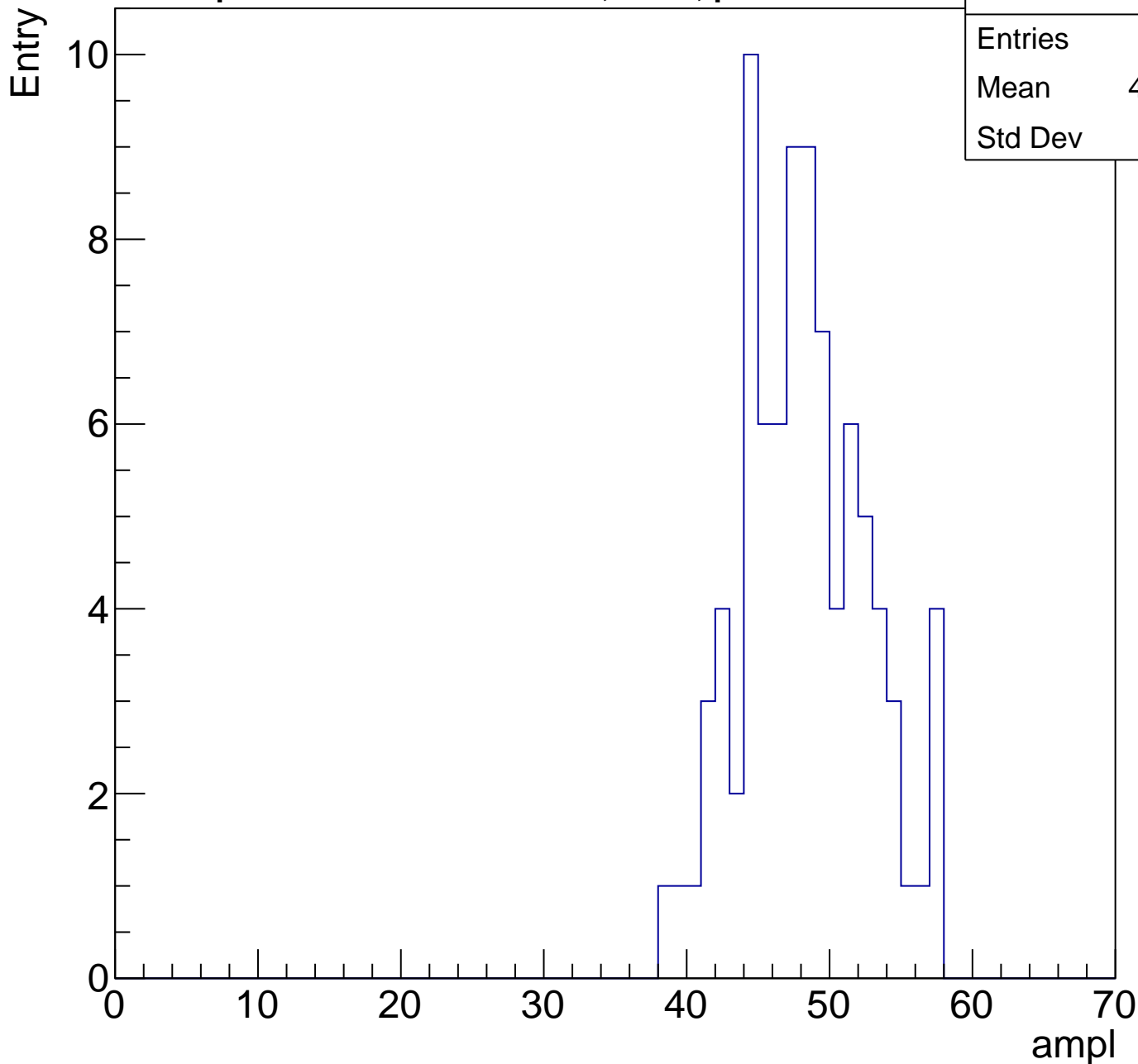
**Gaus Width: 4.9608**



# B1L103S, U21-ch82, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	87
Mean	47.78
Std Dev	4.33

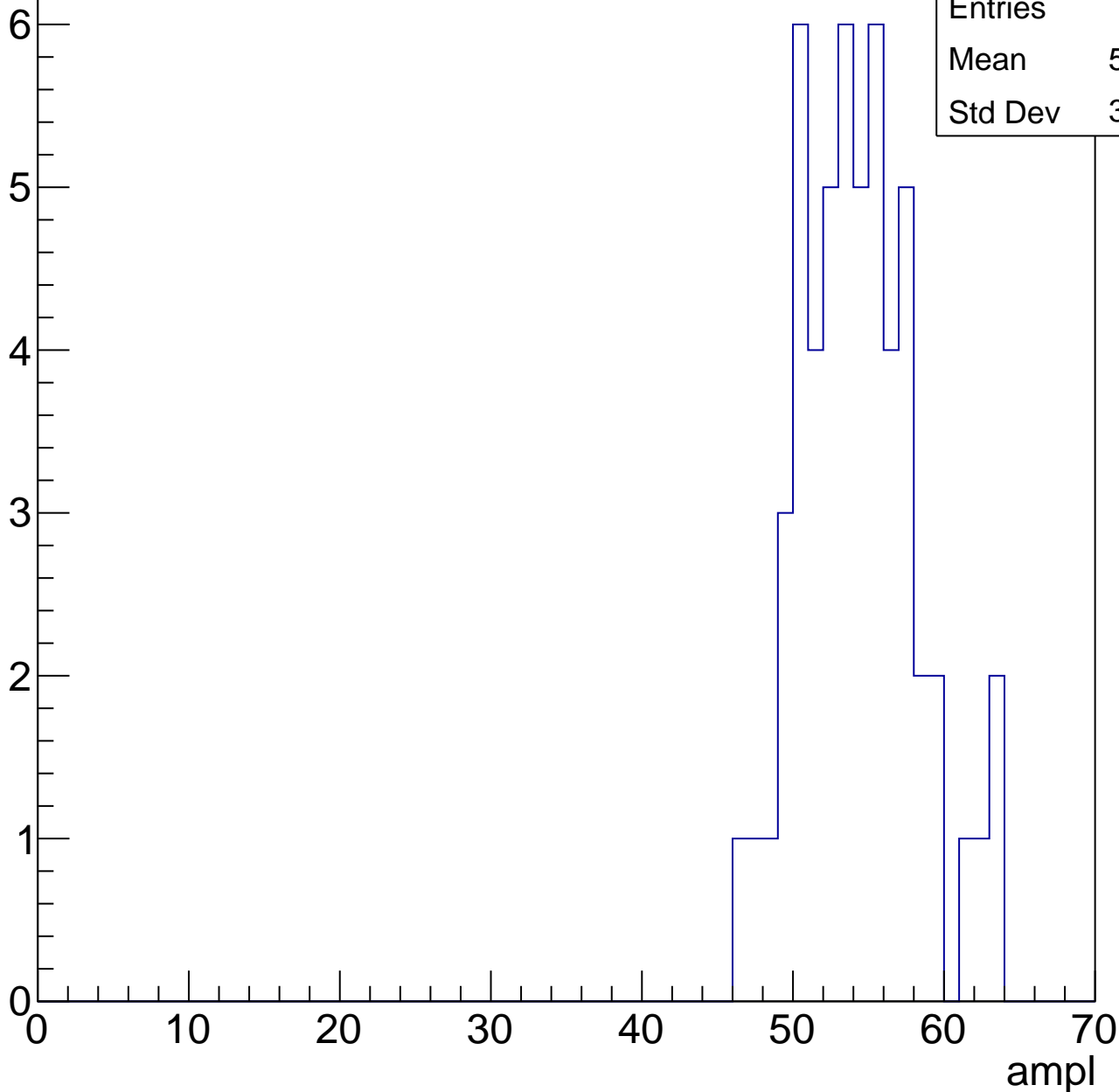


# B1L103S, U21-ch82, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	53.85
Std Dev	3.825

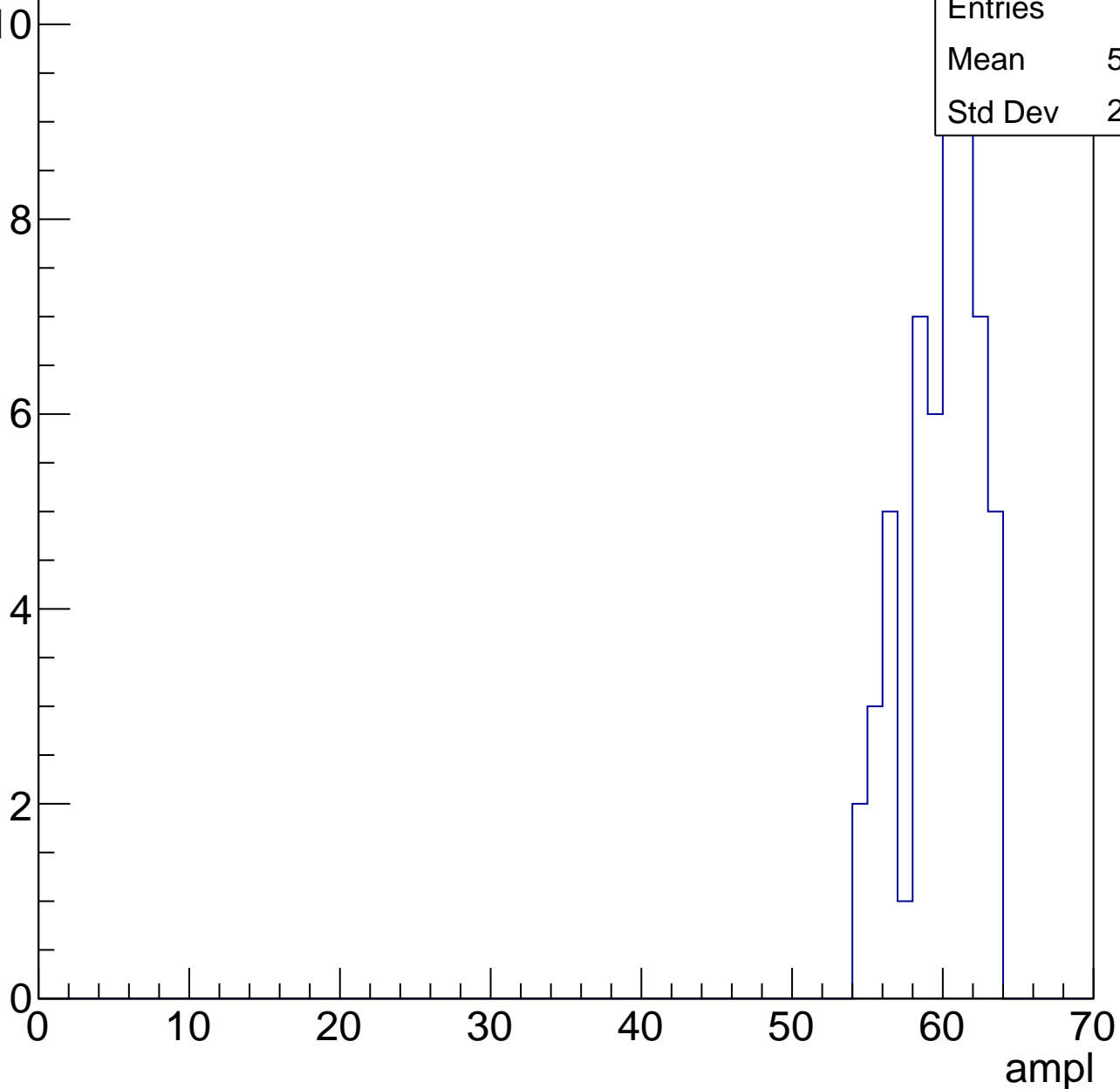


# B1L103S, U21-ch82, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	59.42
Std Dev	2.462



# B1L103S, U21-ch82, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

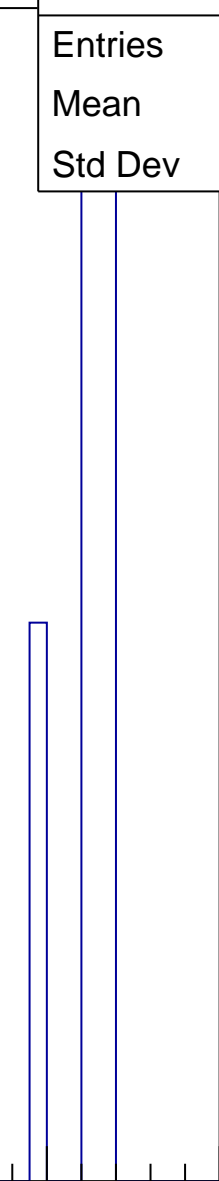
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	61.8
Std Dev	1.47

0 10 20 30 40 50 60 70

ampl

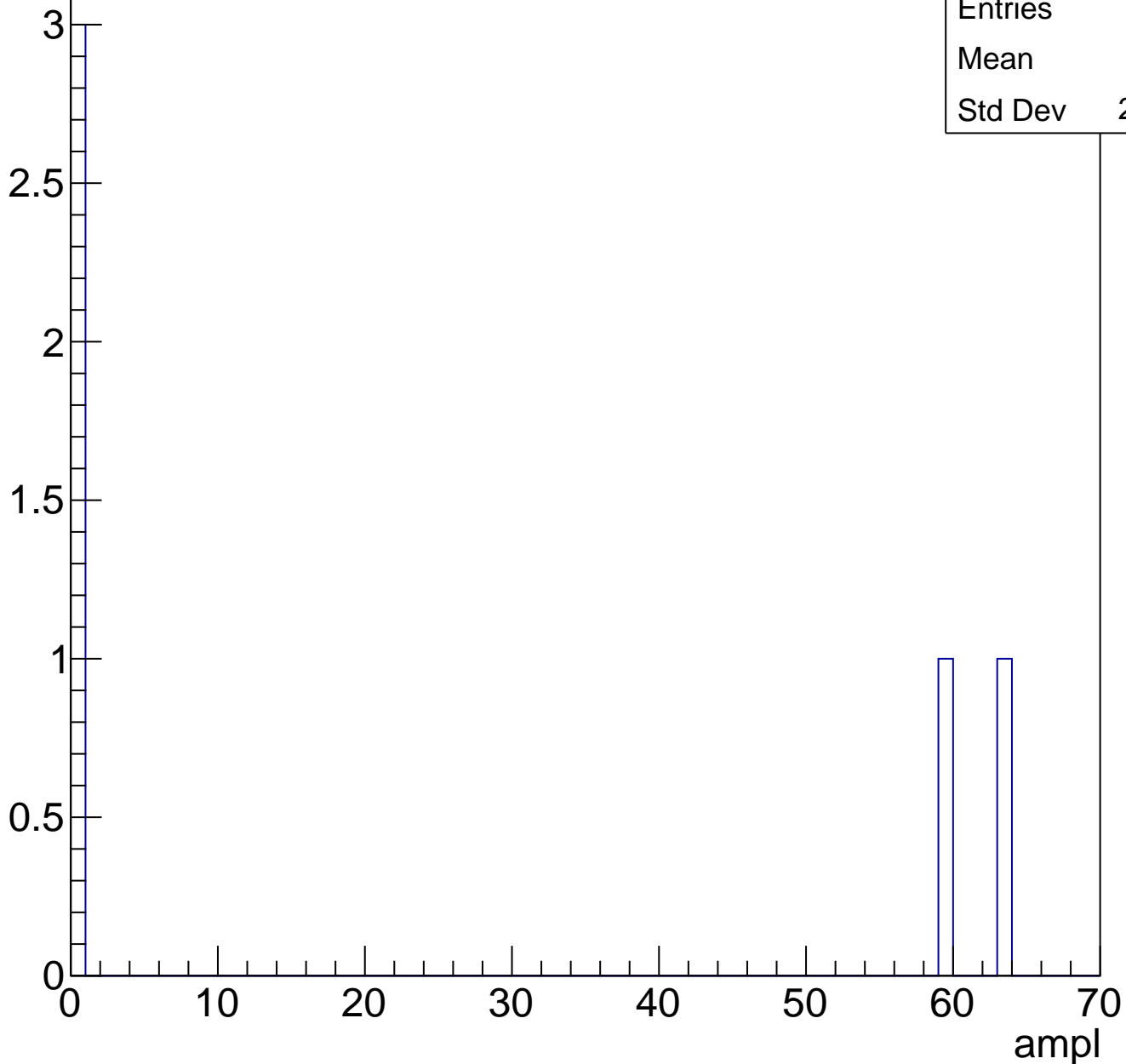




# B1L103S, U21-ch82, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U21-ch83, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	59
Mean	29.41
Std Dev	5.409

**Gaus mean : 29.8404**

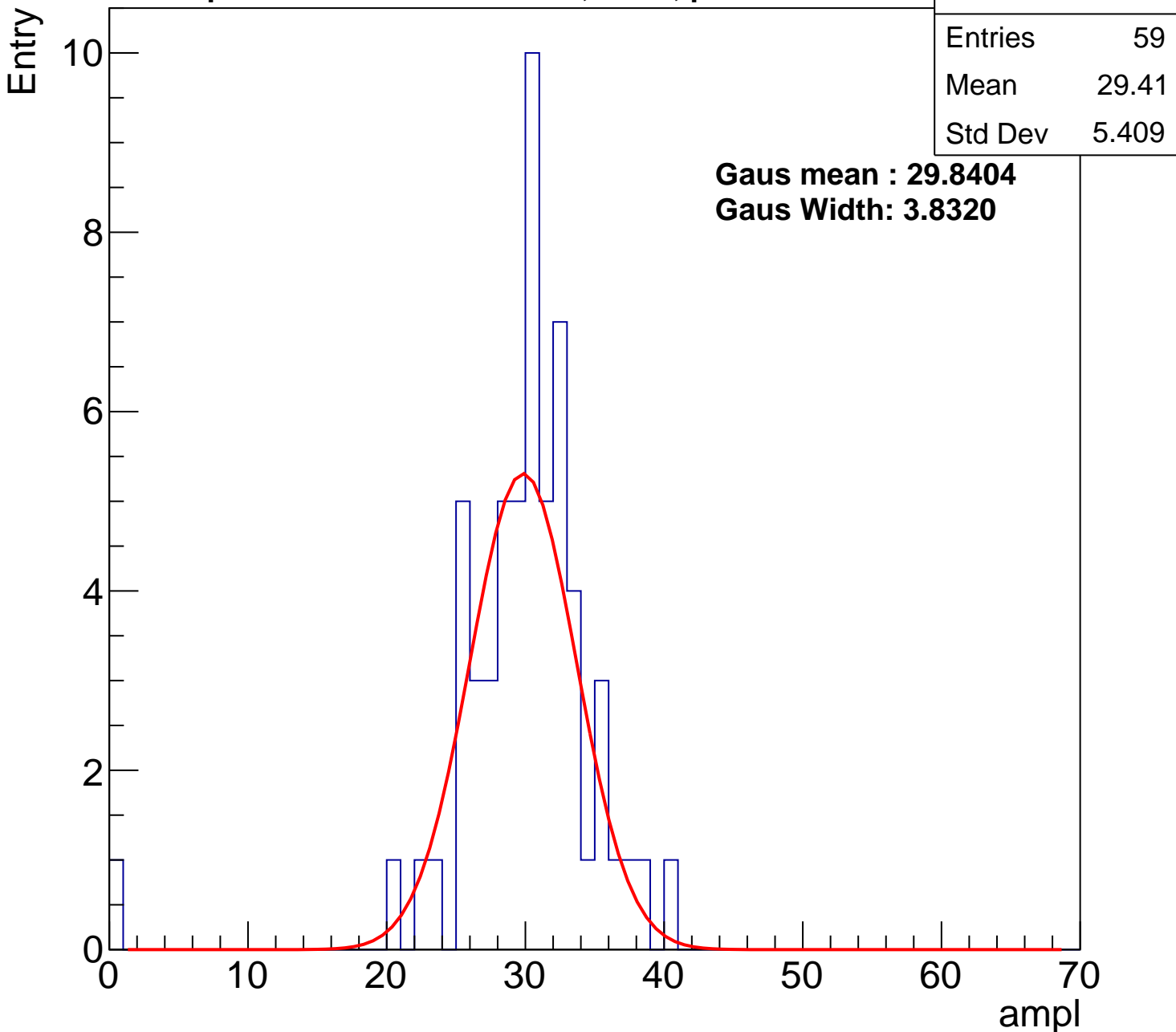
**Gaus Width: 3.8320**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U21-ch83, adc1

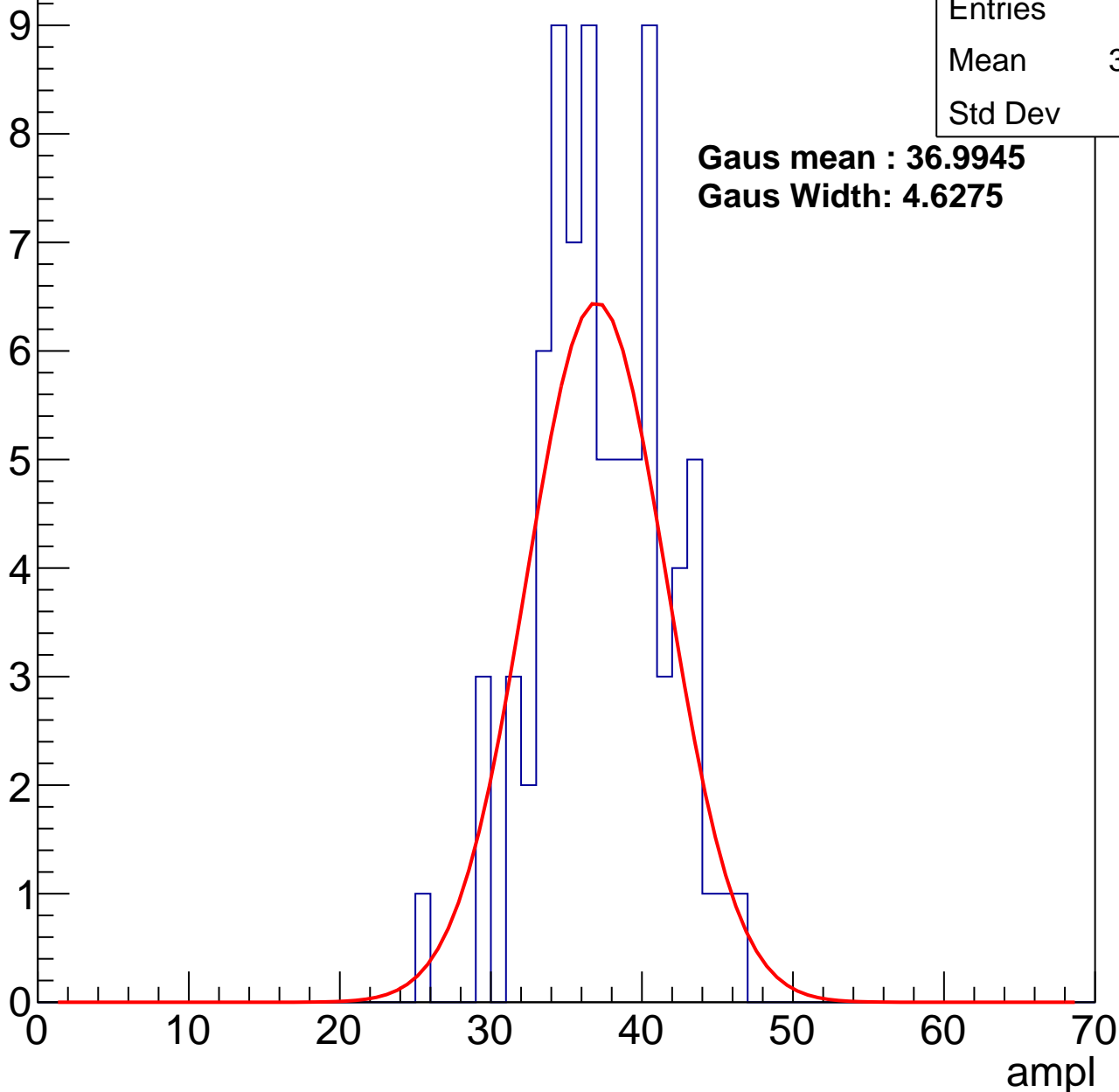
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	79
Mean	36.87
Std Dev	4.11

**Gaus mean : 36.9945**

**Gaus Width: 4.6275**



# B1L103S, U21-ch83, adc2

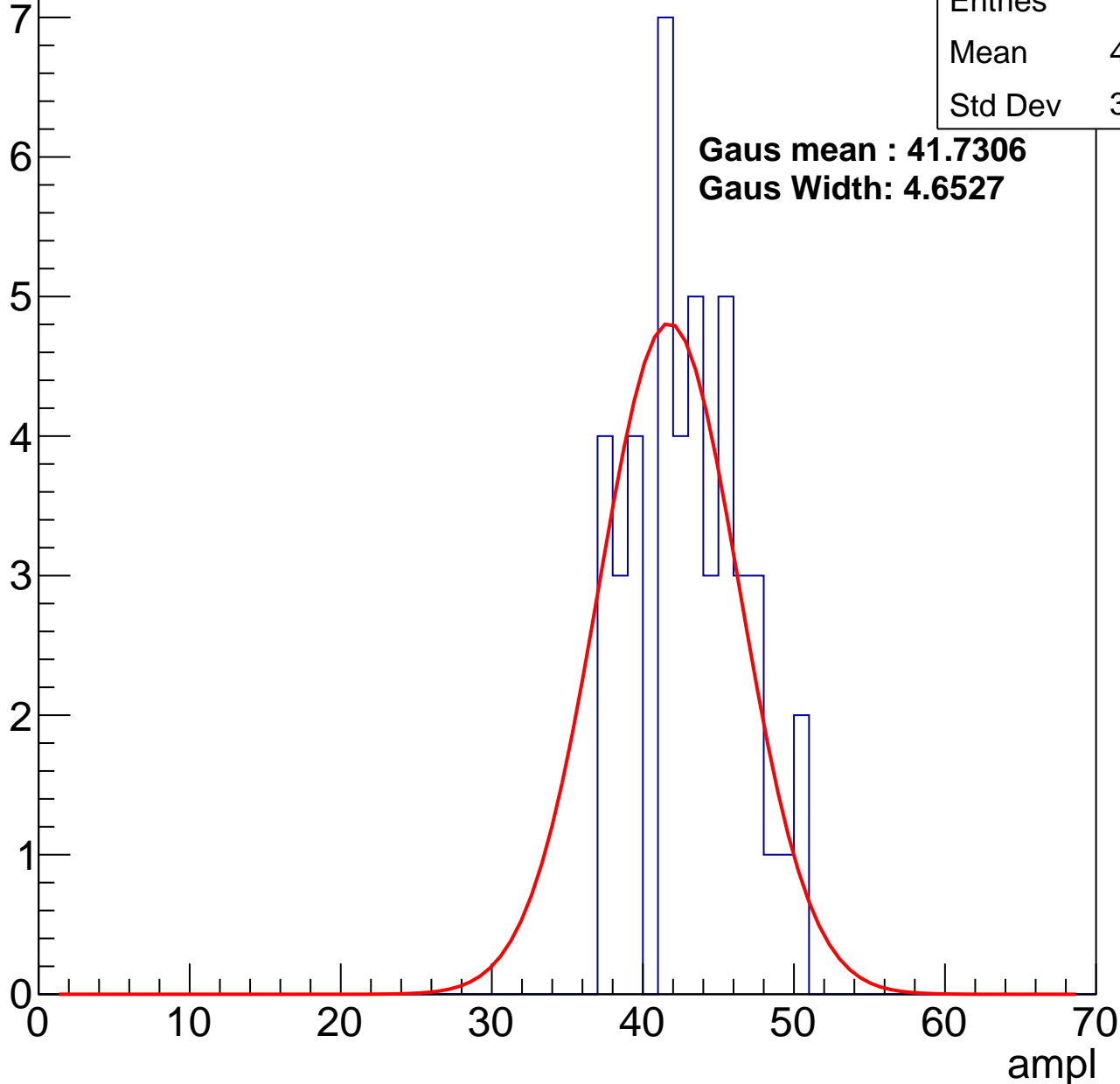
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	45
Mean	42.69
Std Dev	3.552

**Gaus mean : 41.7306**

**Gaus Width: 4.6527**

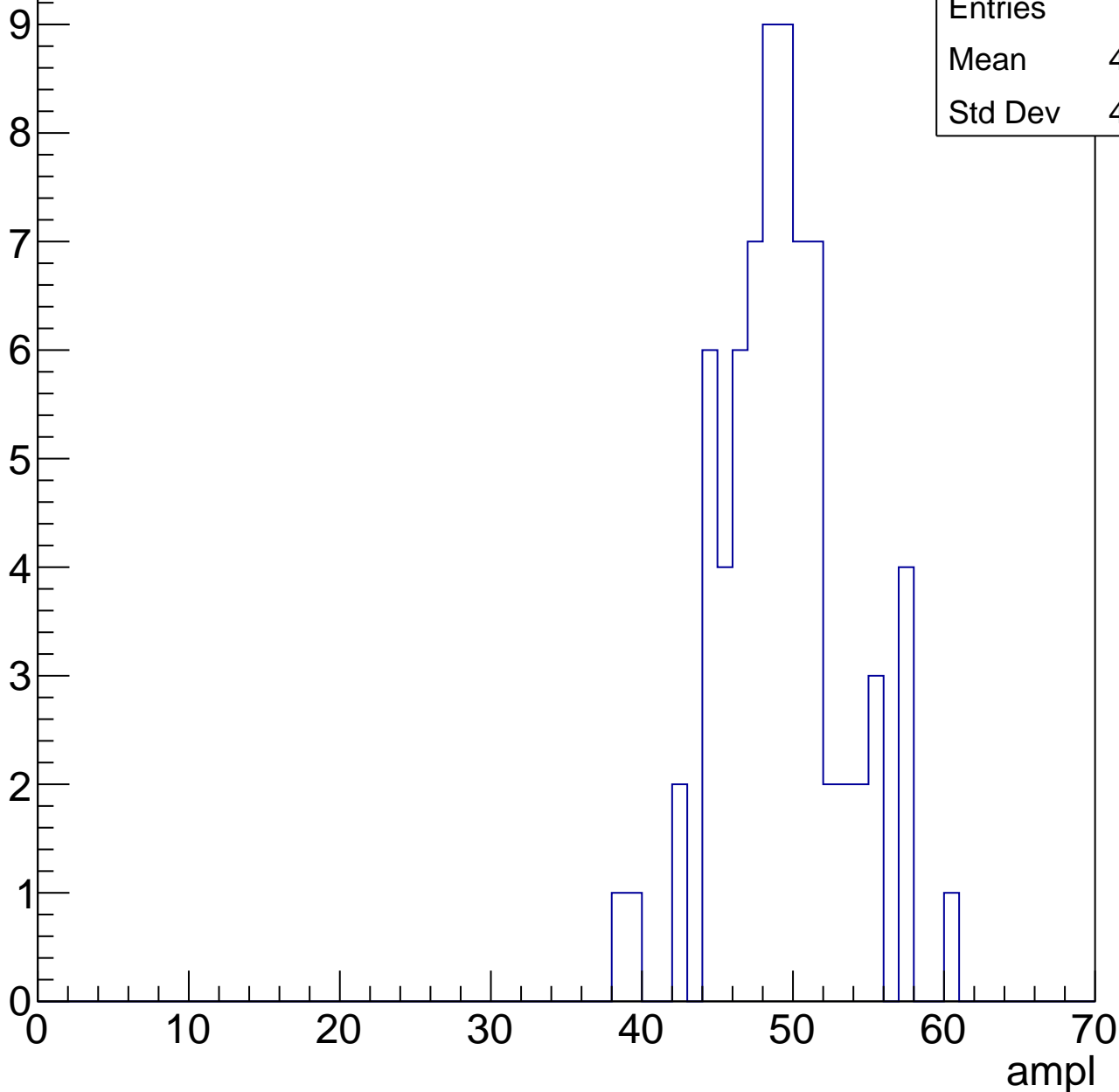


# B1L103S, U21-ch83, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	48.78
Std Dev	4.122

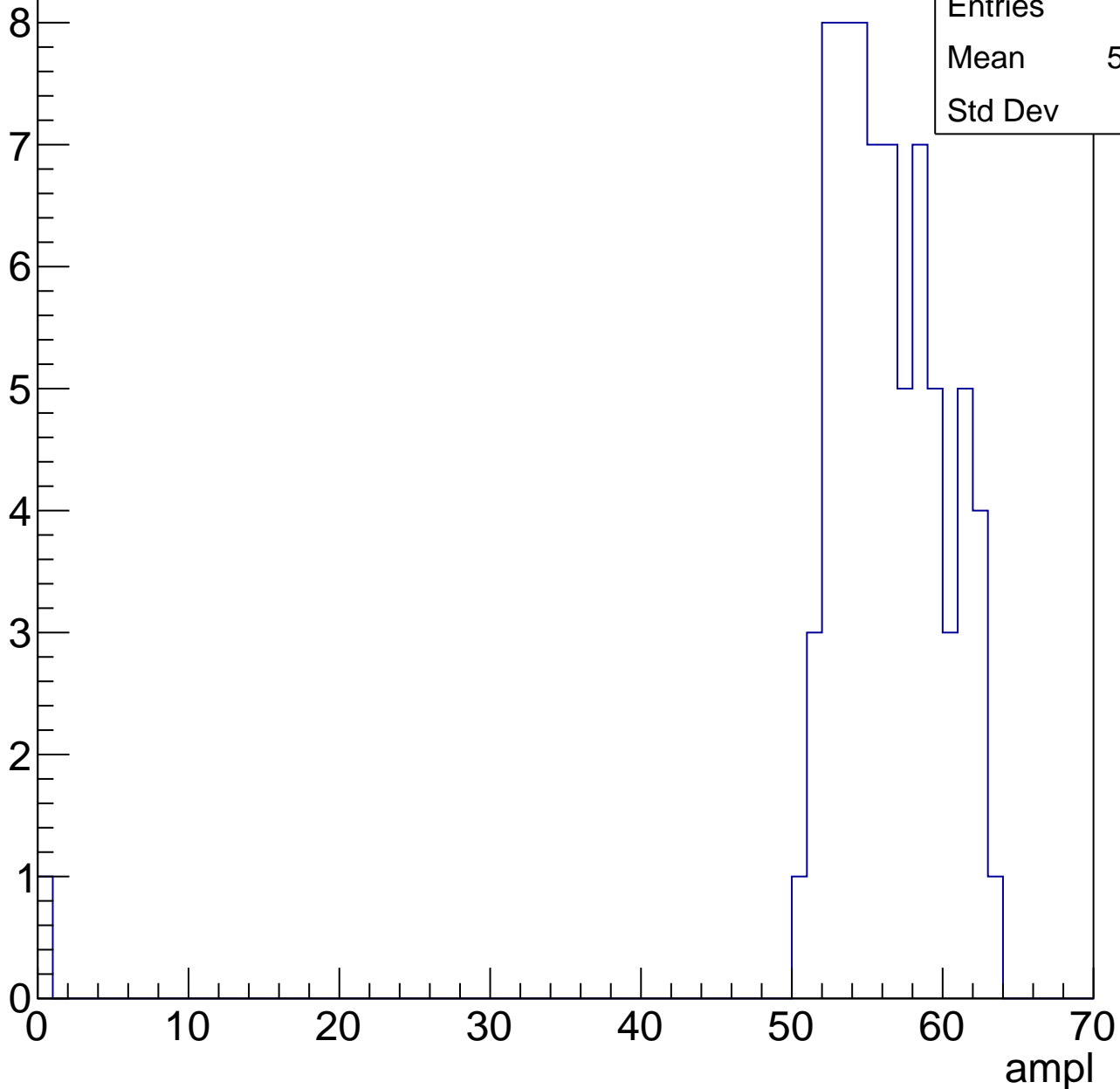


# B1L103S, U21-ch83, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	55.26
Std Dev	7.3

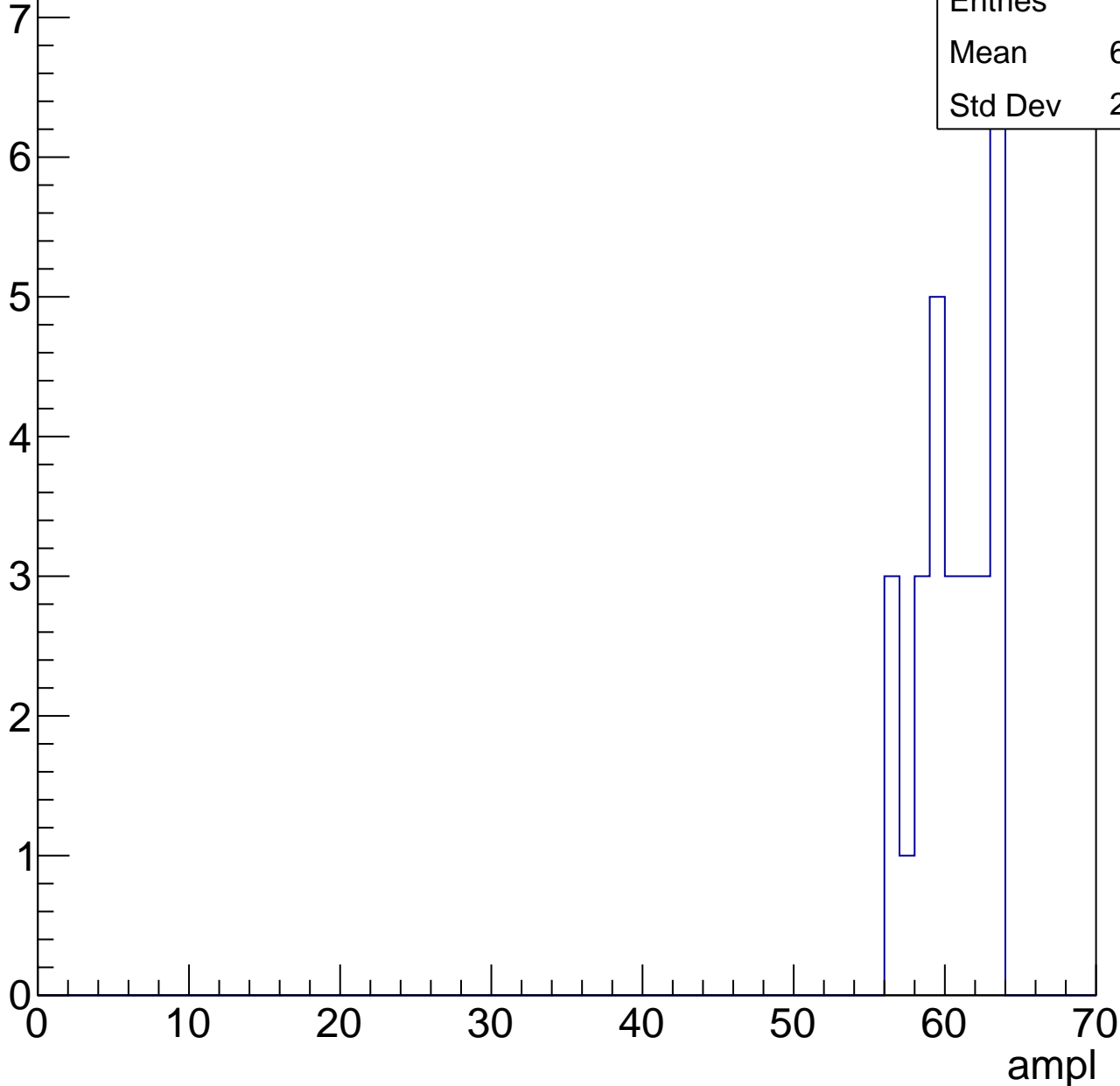


# B1L103S, U21-ch83, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

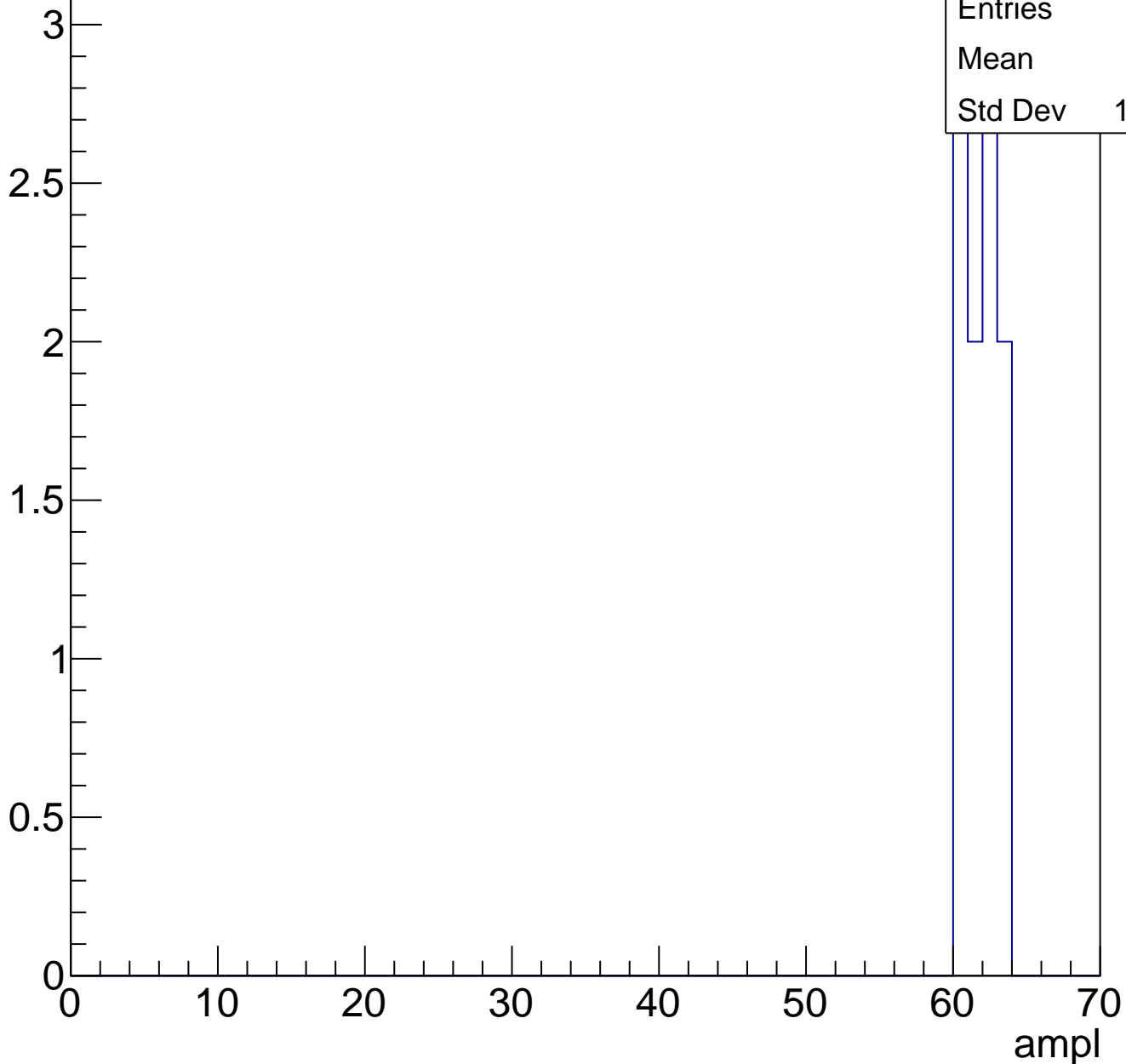
Entries	28
Mean	60.14
Std Dev	2.326



# B1L103S, U21-ch83, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U21-ch83, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L103S, U21-ch84, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	89
Mean	27.57
Std Dev	4.143

**Gaus mean : 27.9524**

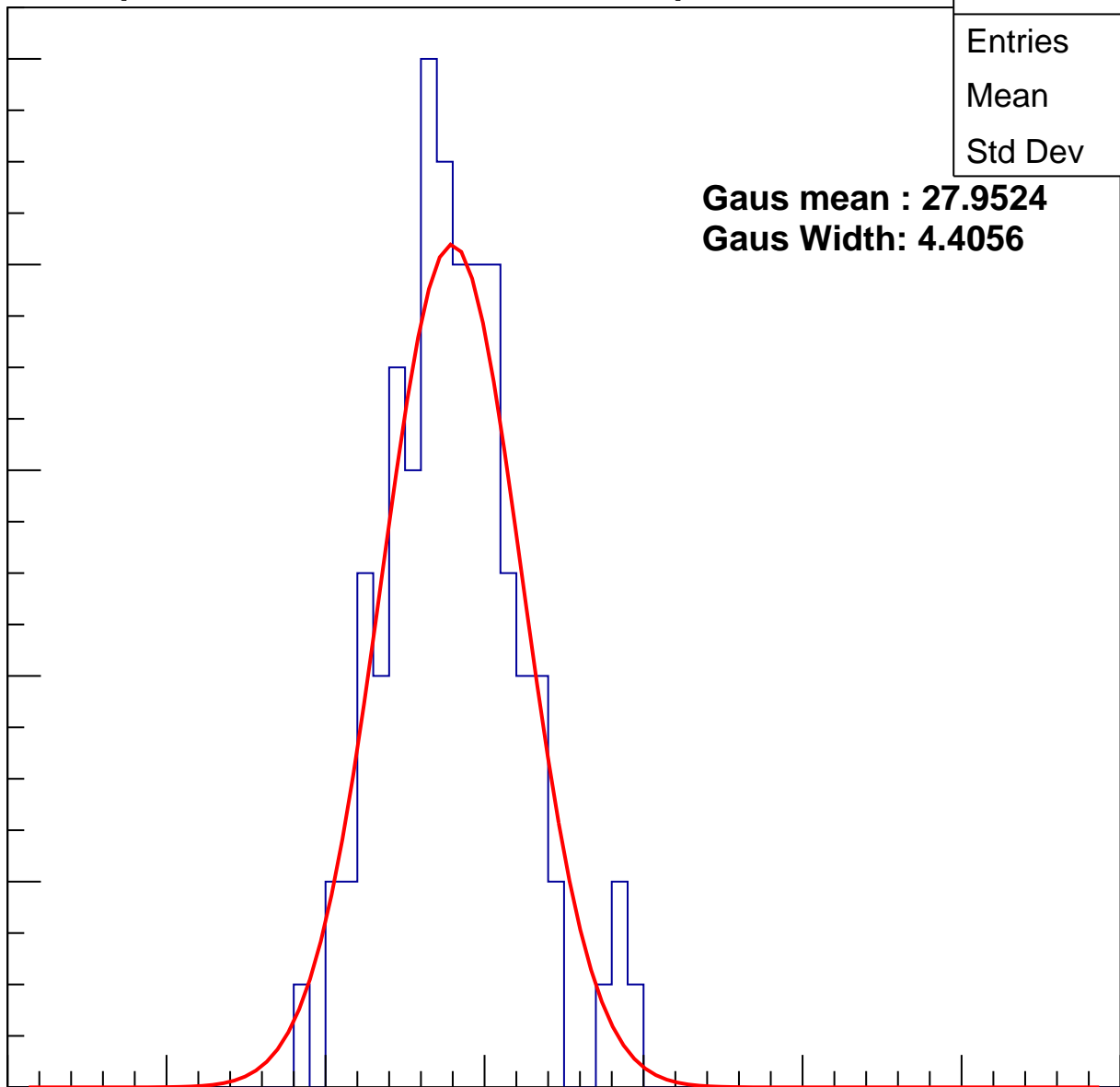
**Gaus Width: 4.4056**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U21-ch84, adc1

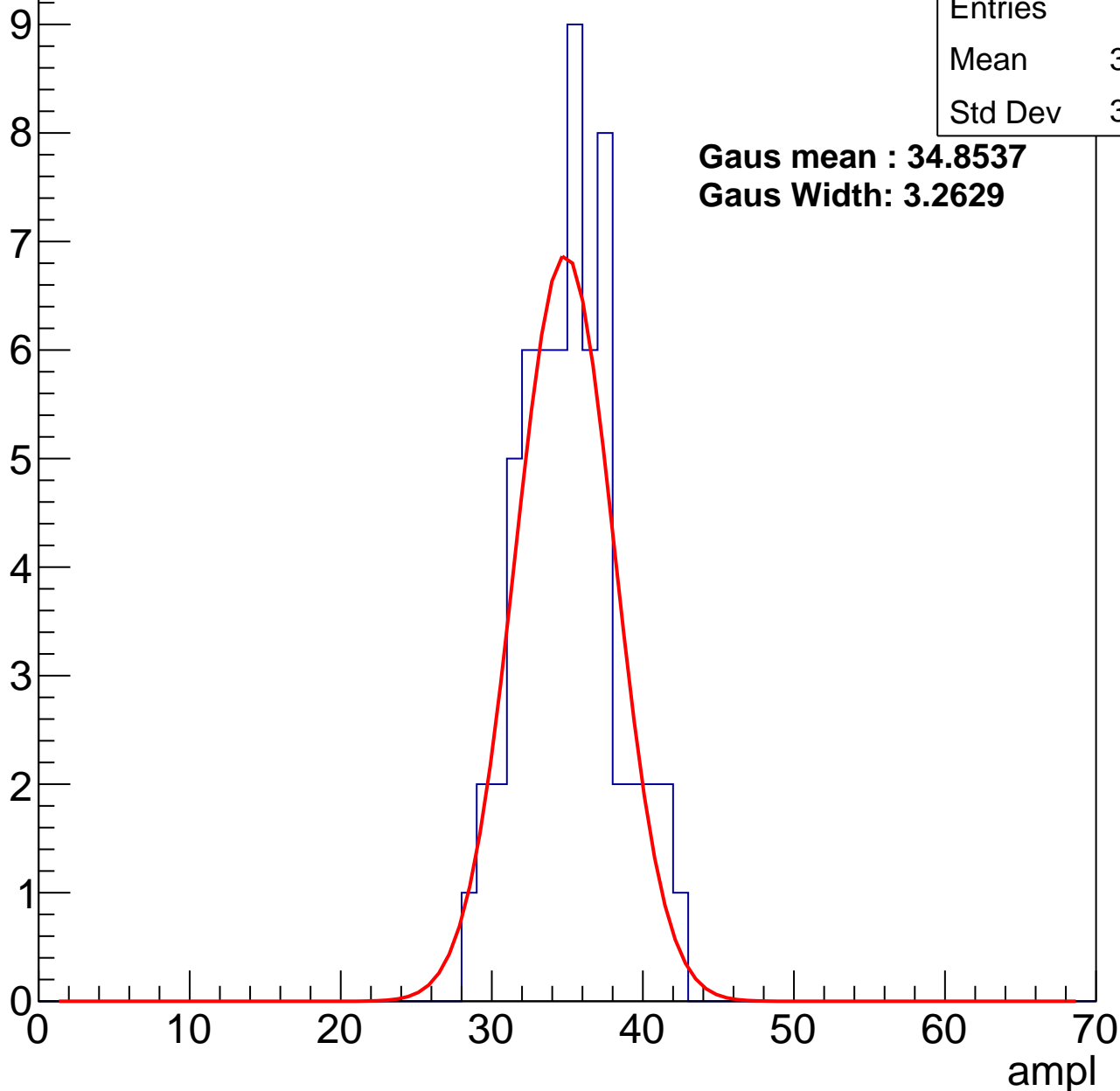
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	34.67
Std Dev	3.129

**Gaus mean : 34.8537**

**Gaus Width: 3.2629**



# B1L103S, U21-ch84, adc2

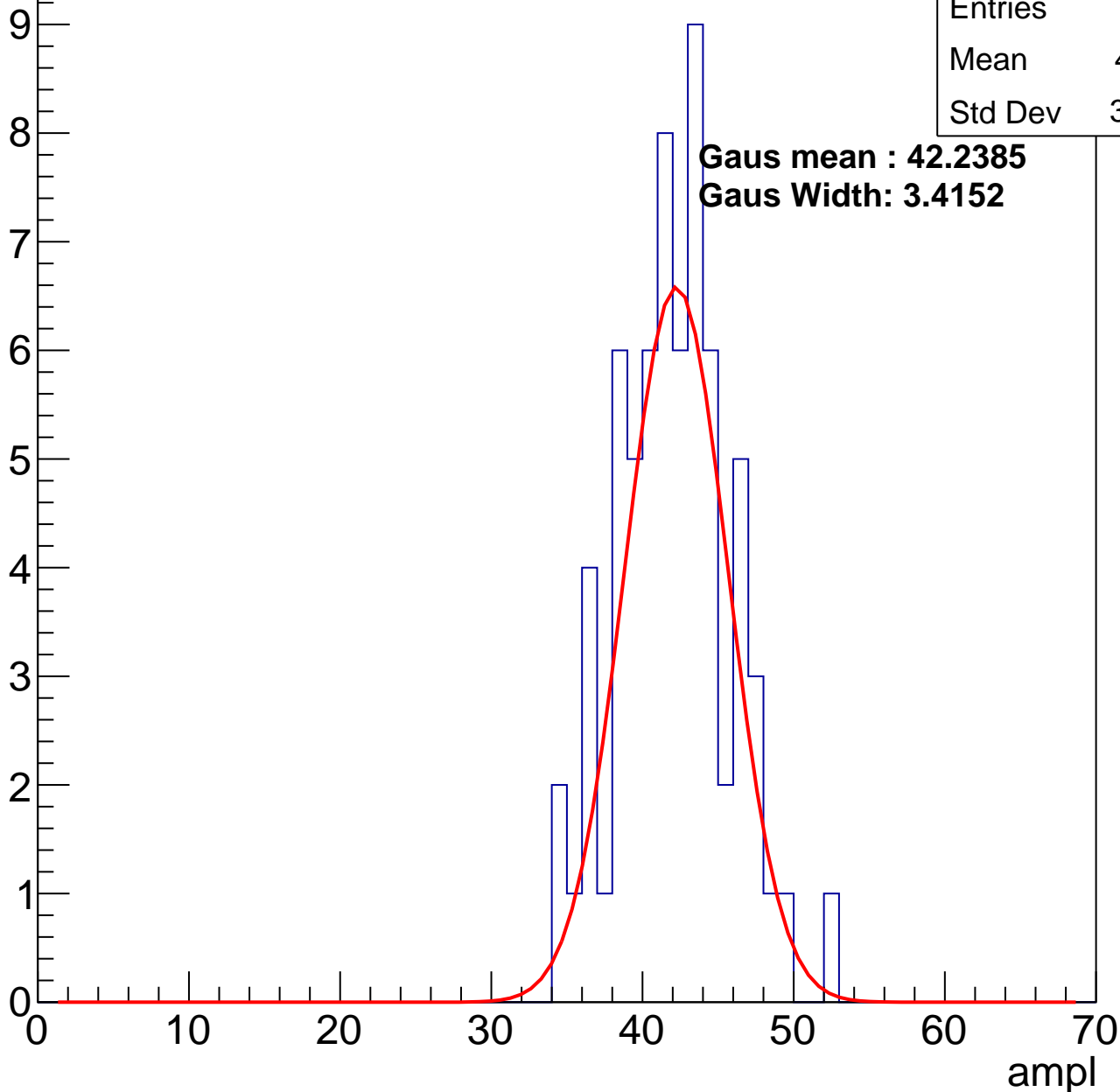
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	41.61
Std Dev	3.665

**Gaus mean : 42.2385**

**Gaus Width: 3.4152**

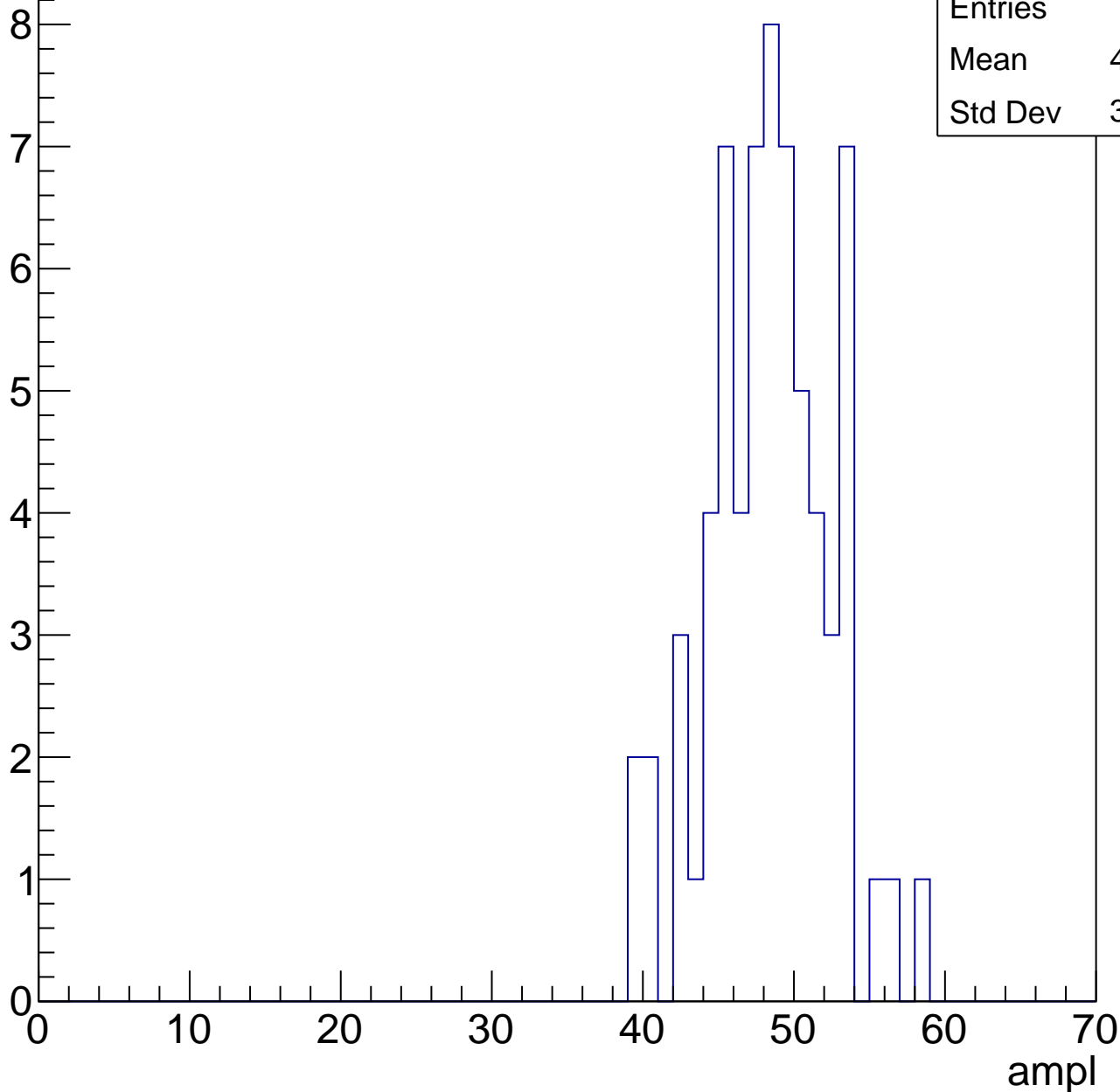


# B1L103S, U21-ch84, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	47.88
Std Dev	3.998

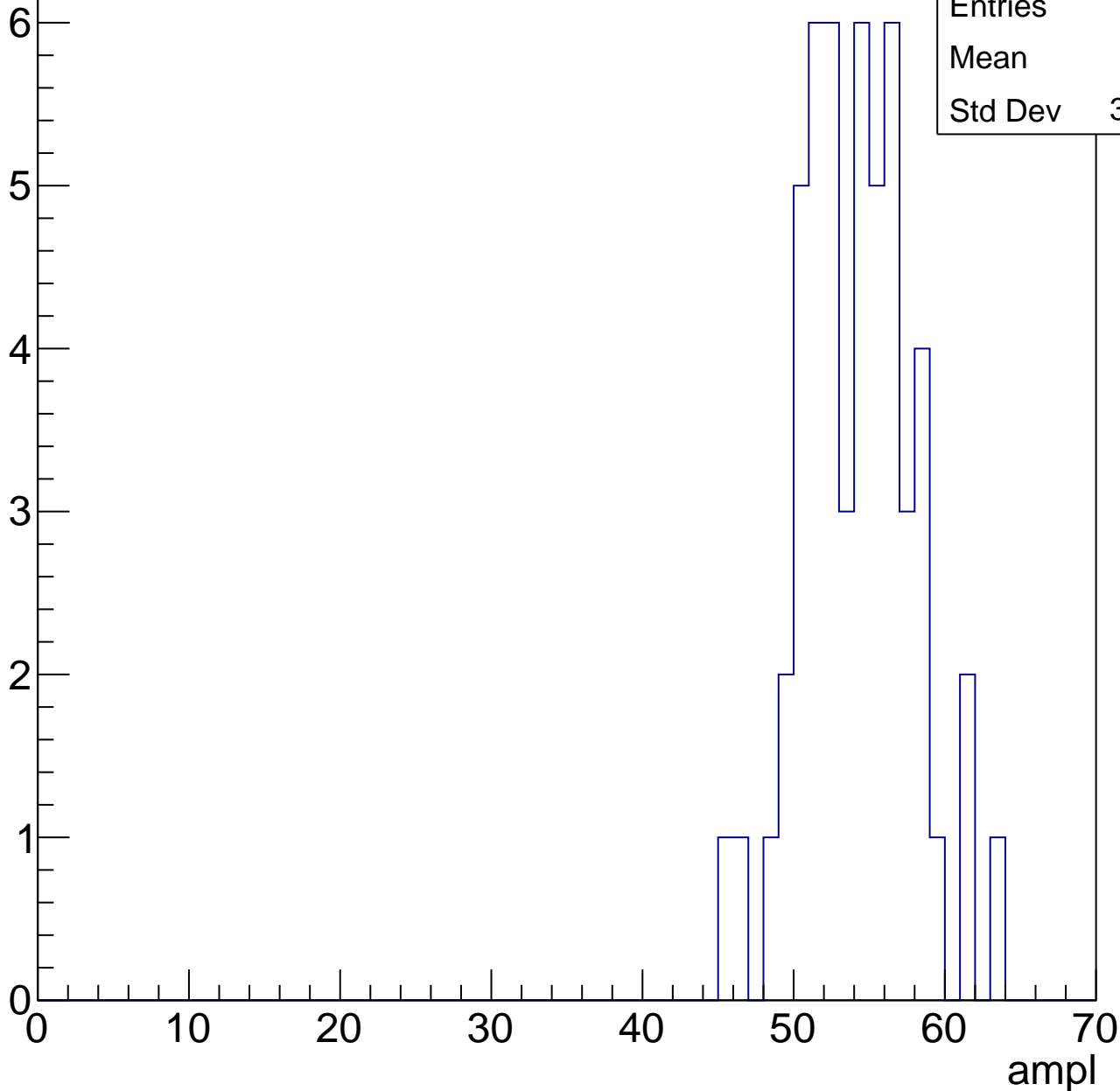


# B1L103S, U21-ch84, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	53.7
Std Dev	3.663

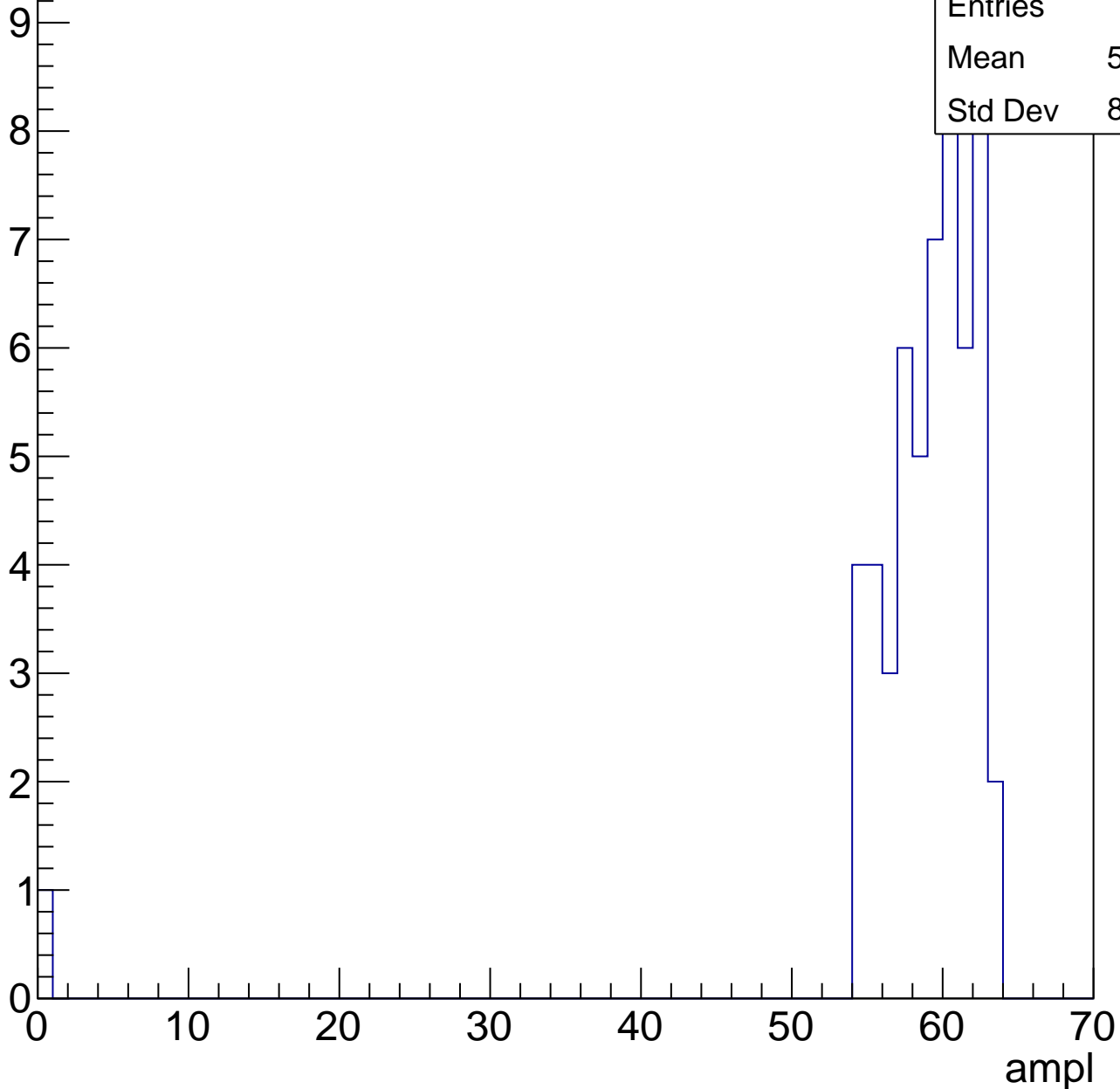


# B1L103S, U21-ch84, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	57.84
Std Dev	8.207

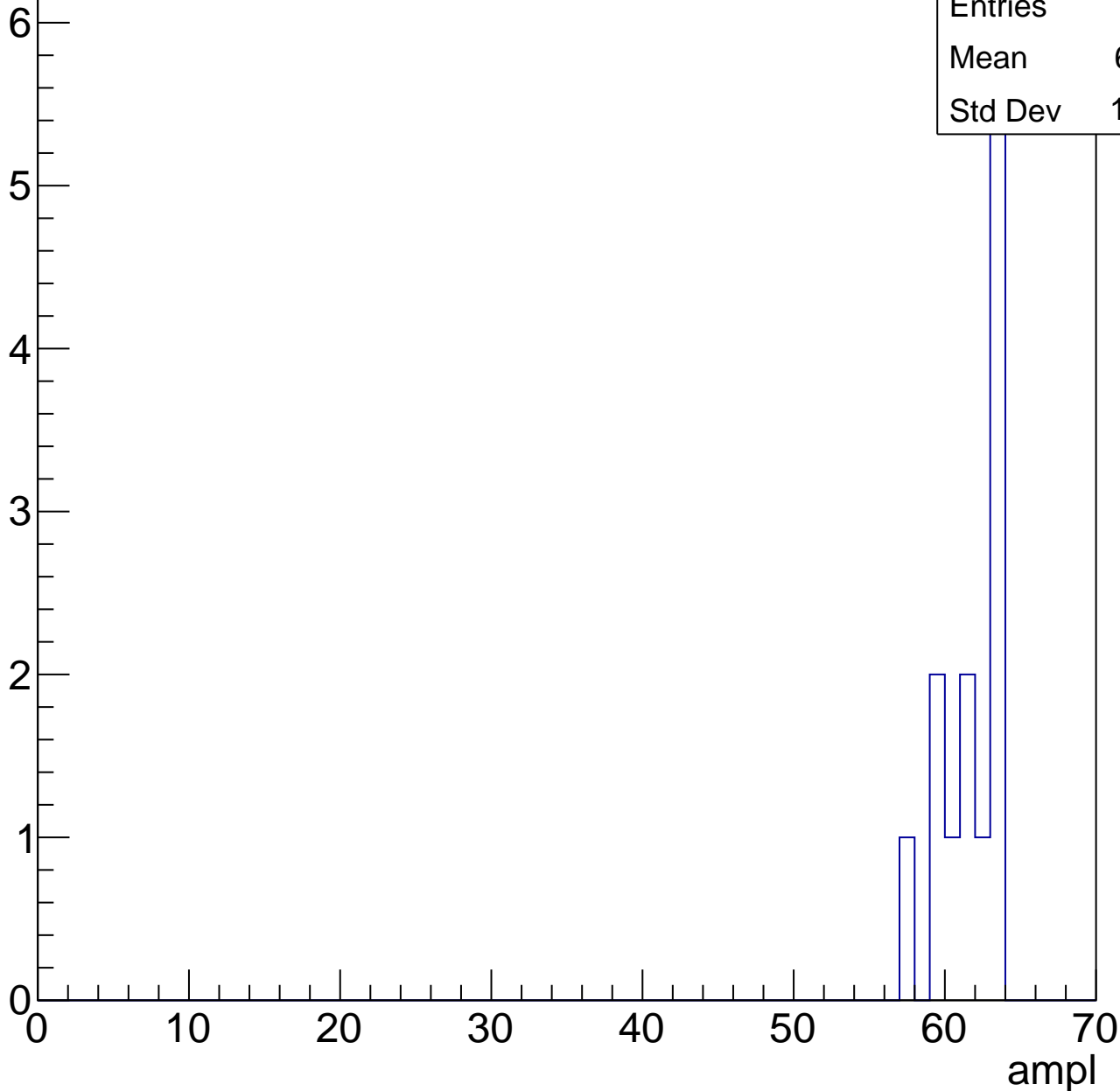


# B1L103S, U21-ch84, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	13
Mean	61.31
Std Dev	1.937





# B1L103S, U21-ch84, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U21-ch85, adc0

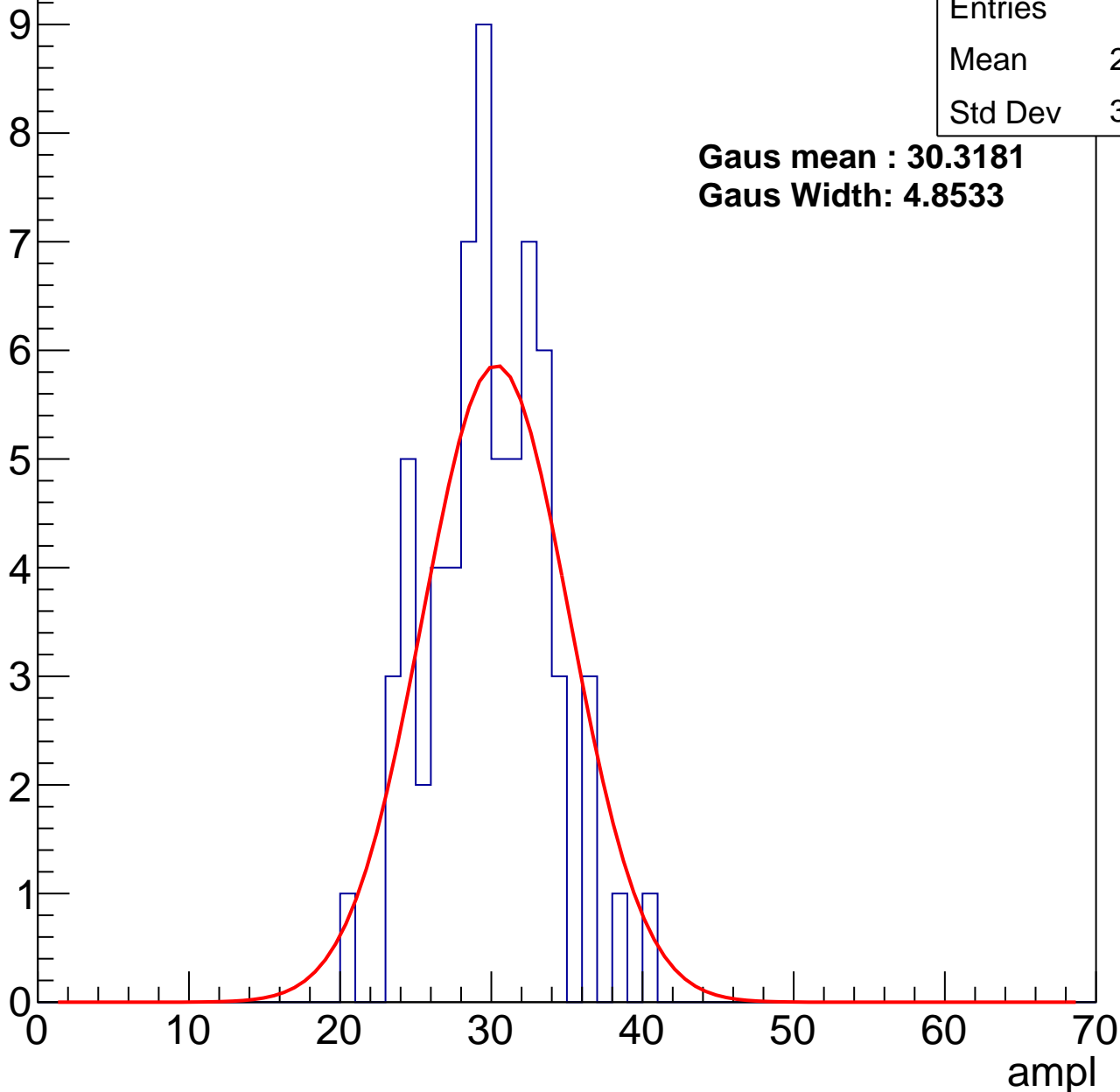
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	29.44
Std Dev	3.893

**Gaus mean : 30.3181**

**Gaus Width: 4.8533**



# B1L103S, U21-ch85, adc1

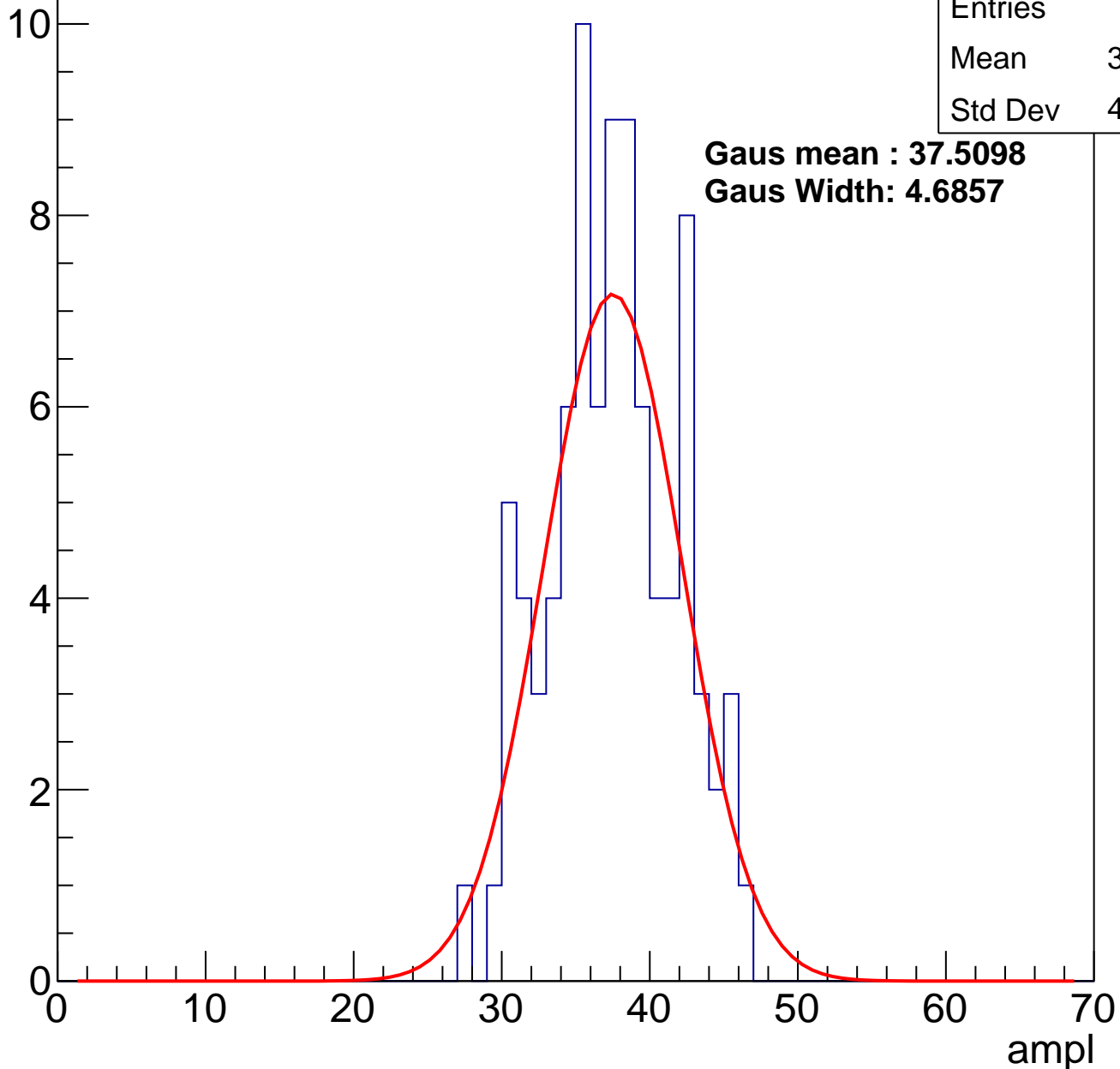
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	89
Mean	37.02
Std Dev	4.245

**Gaus mean : 37.5098**

**Gaus Width: 4.6857**

Entry



# B1L103S, U21-ch85, adc2

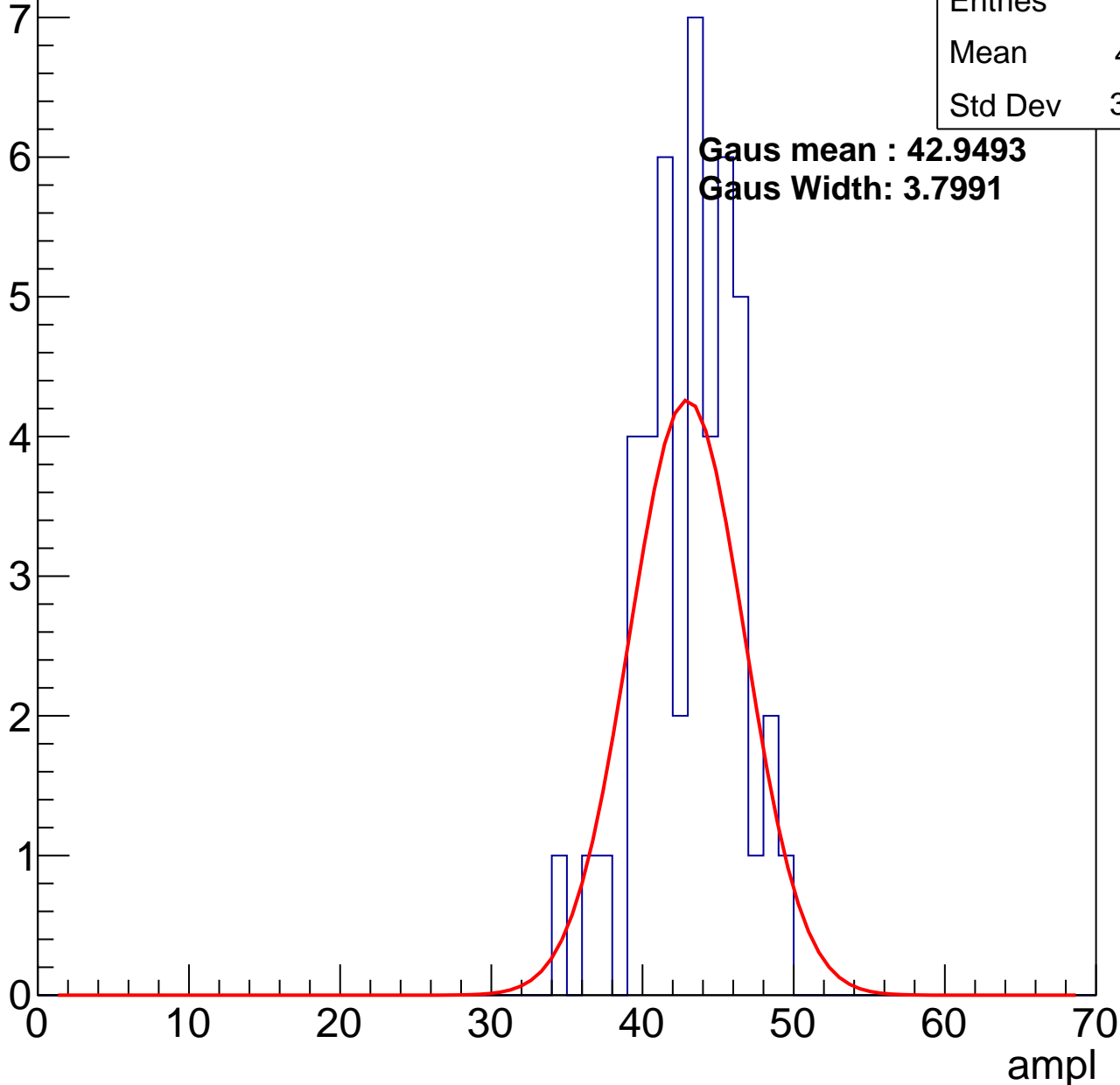
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	45
Mean	42.71
Std Dev	3.208

**Gaus mean : 42.9493**

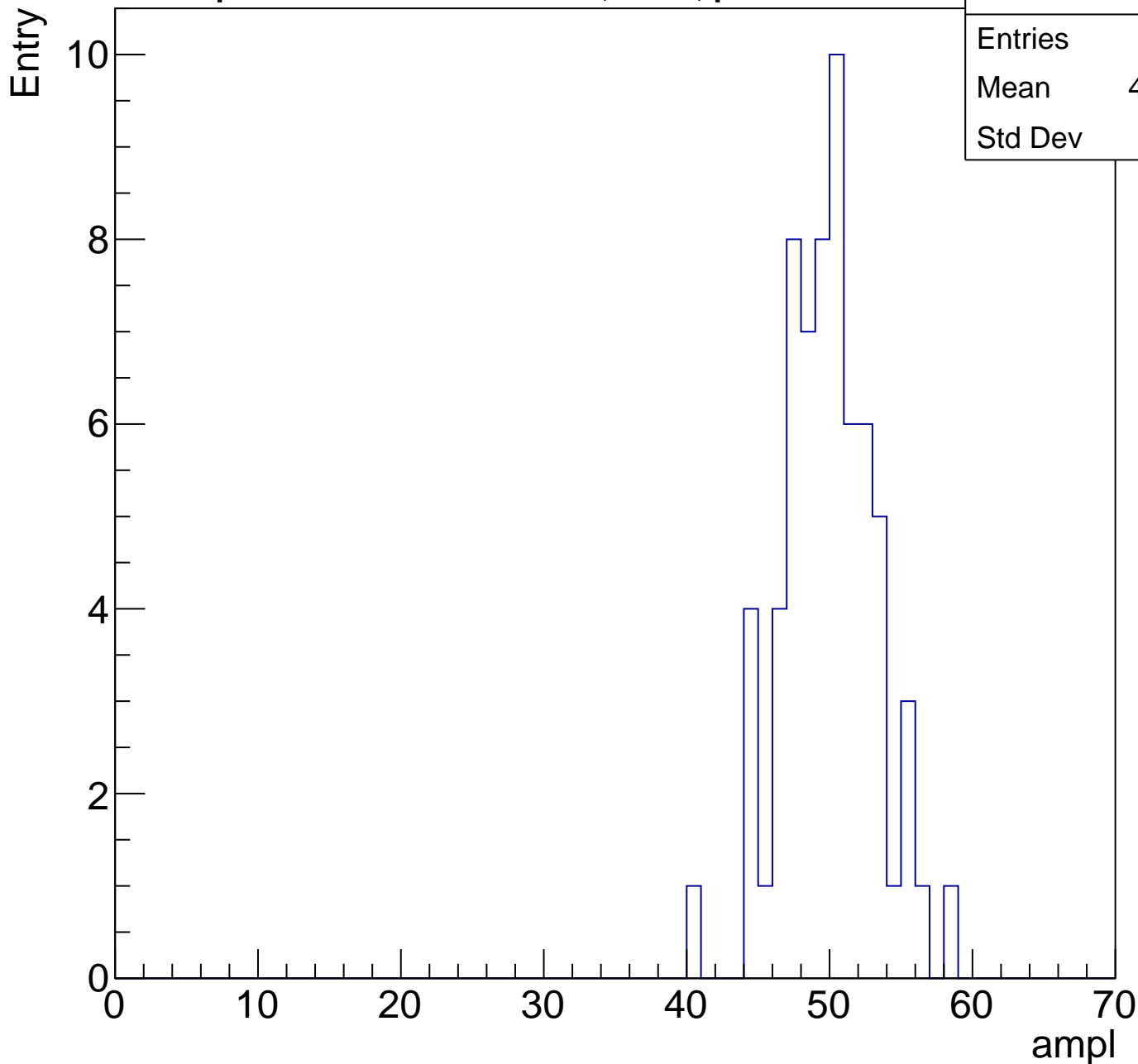
**Gaus Width: 3.7991**



# B1L103S, U21-ch85, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	66
Mean	49.47
Std Dev	3.23

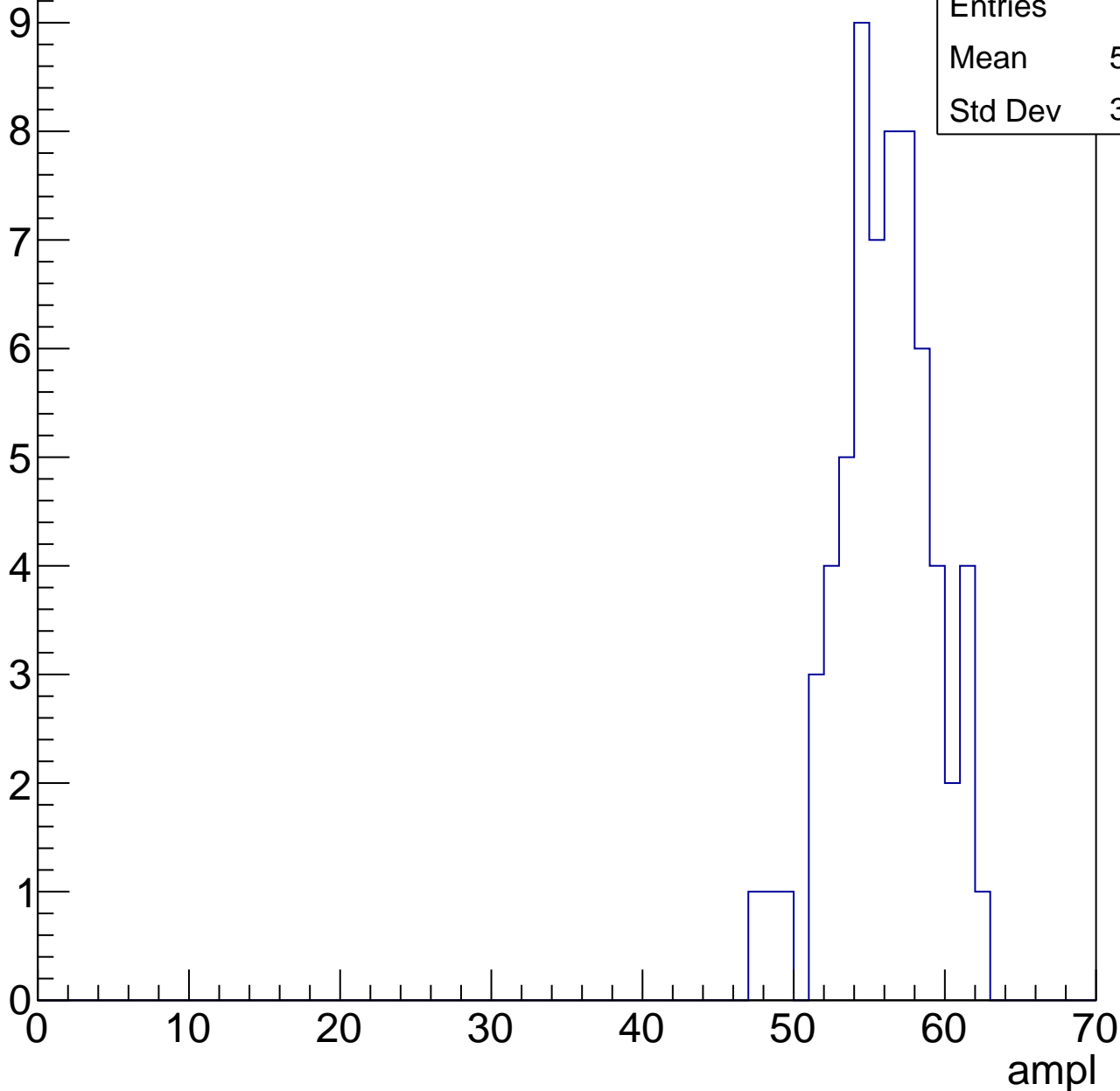


# B1L103S, U21-ch85, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

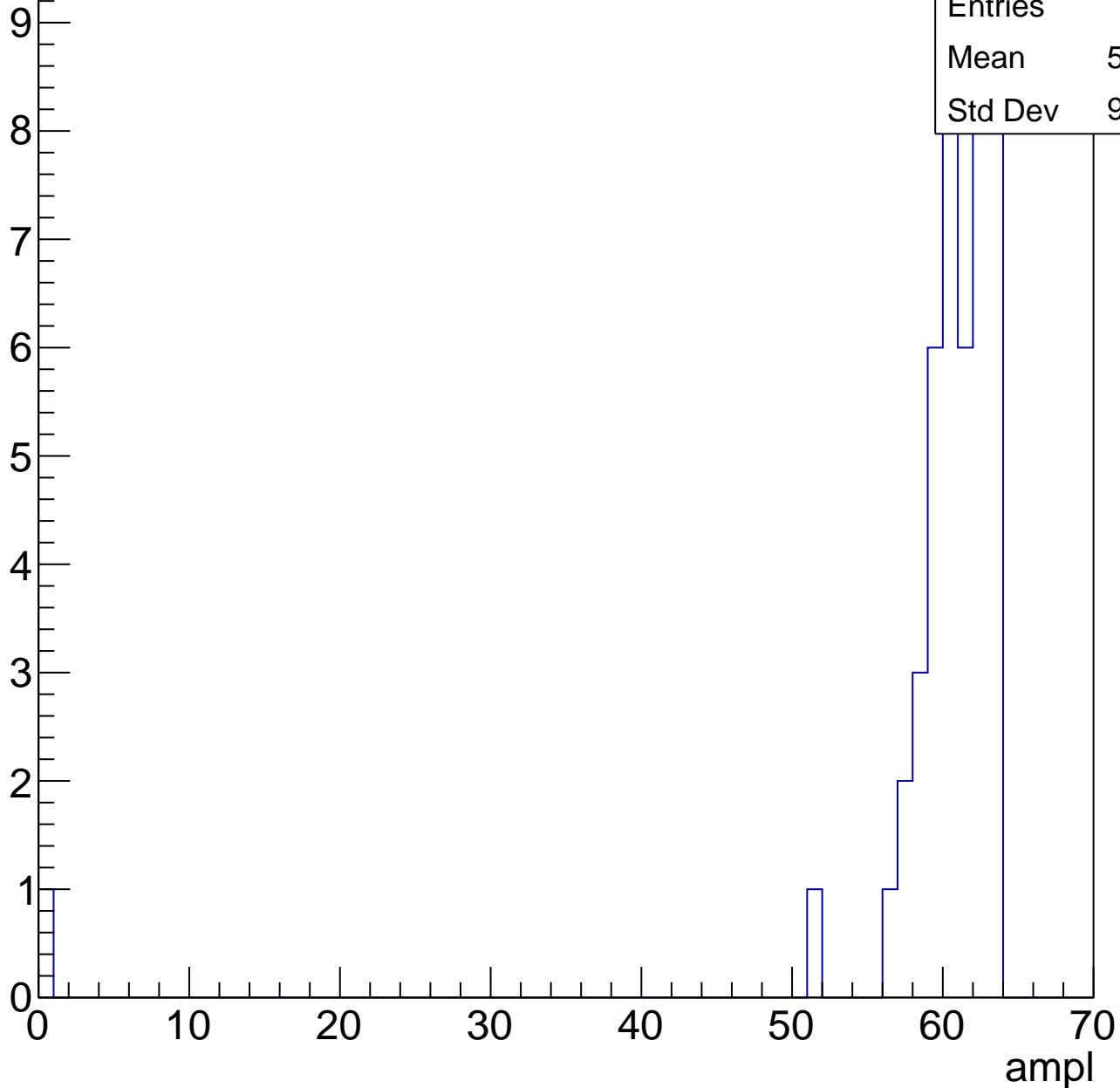
Entries	64
Mean	55.55
Std Dev	3.172



# B1L103S, U21-ch85, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U21-ch85, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U21-ch85, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U21-ch86, adc0

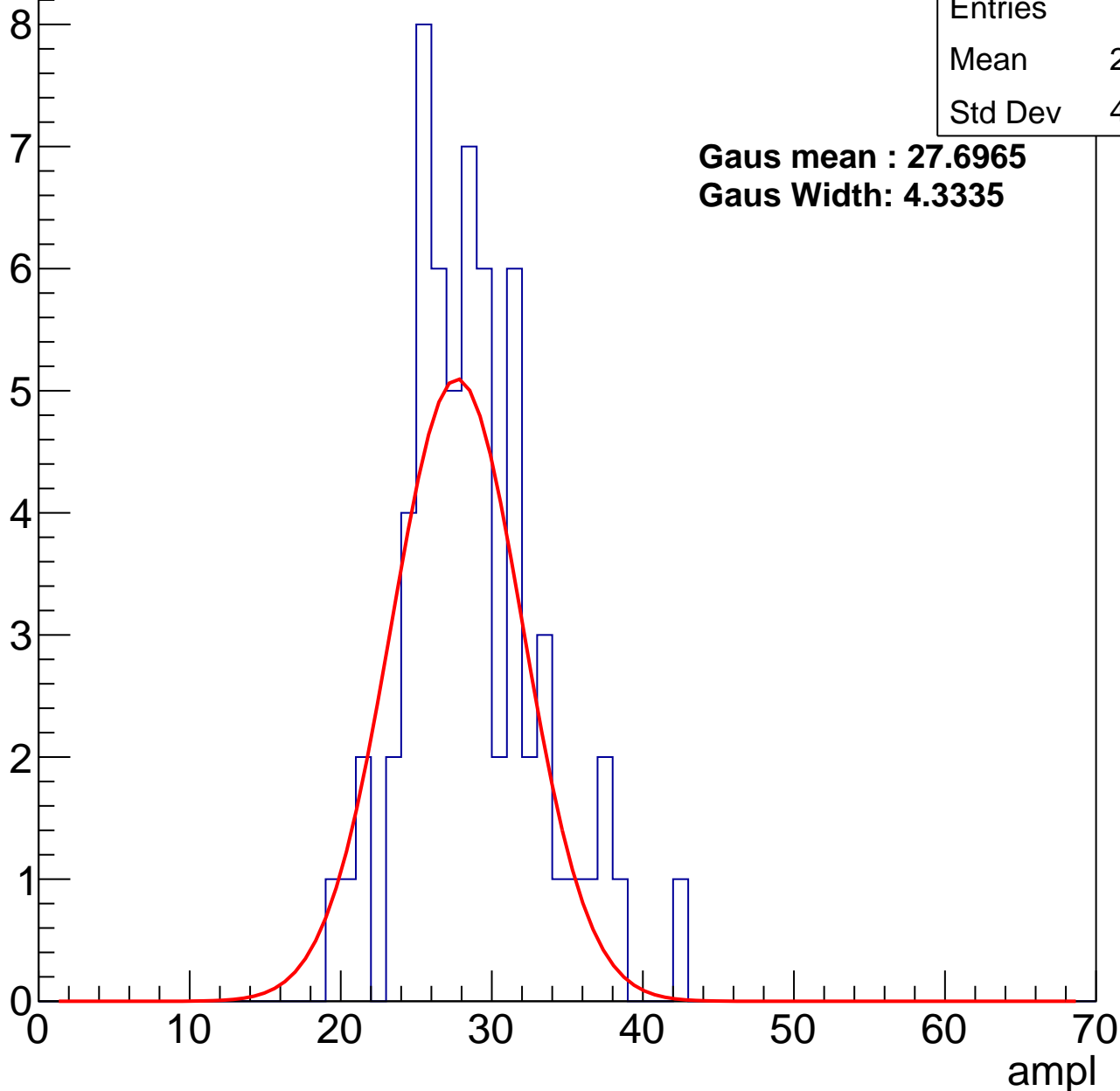
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	28.26
Std Dev	4.465

**Gaus mean : 27.6965**

**Gaus Width: 4.3335**



# B1L103S, U21-ch86, adc1

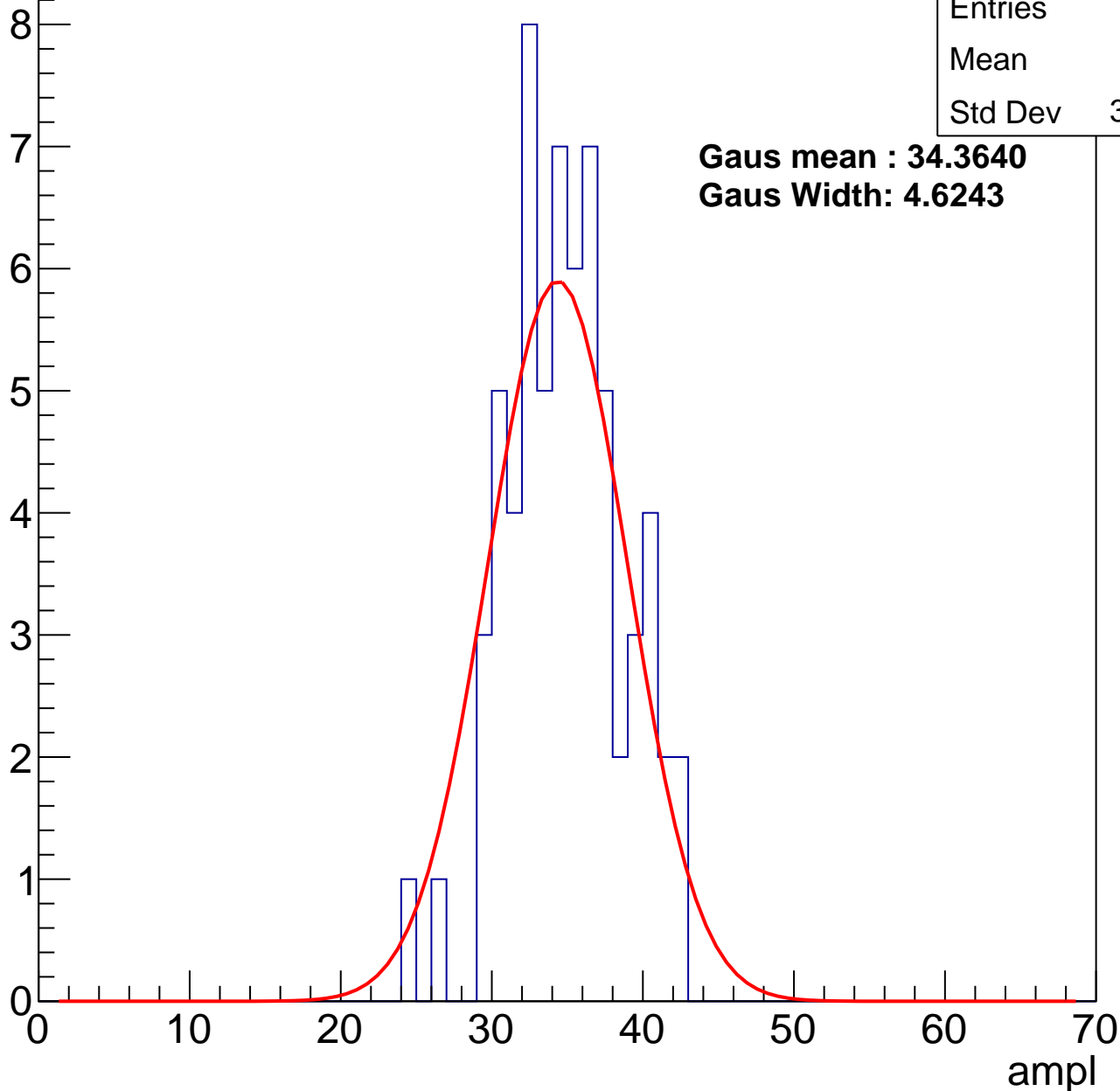
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	34.4
Std Dev	3.798

**Gaus mean : 34.3640**

**Gaus Width: 4.6243**



# B1L103S, U21-ch86, adc2

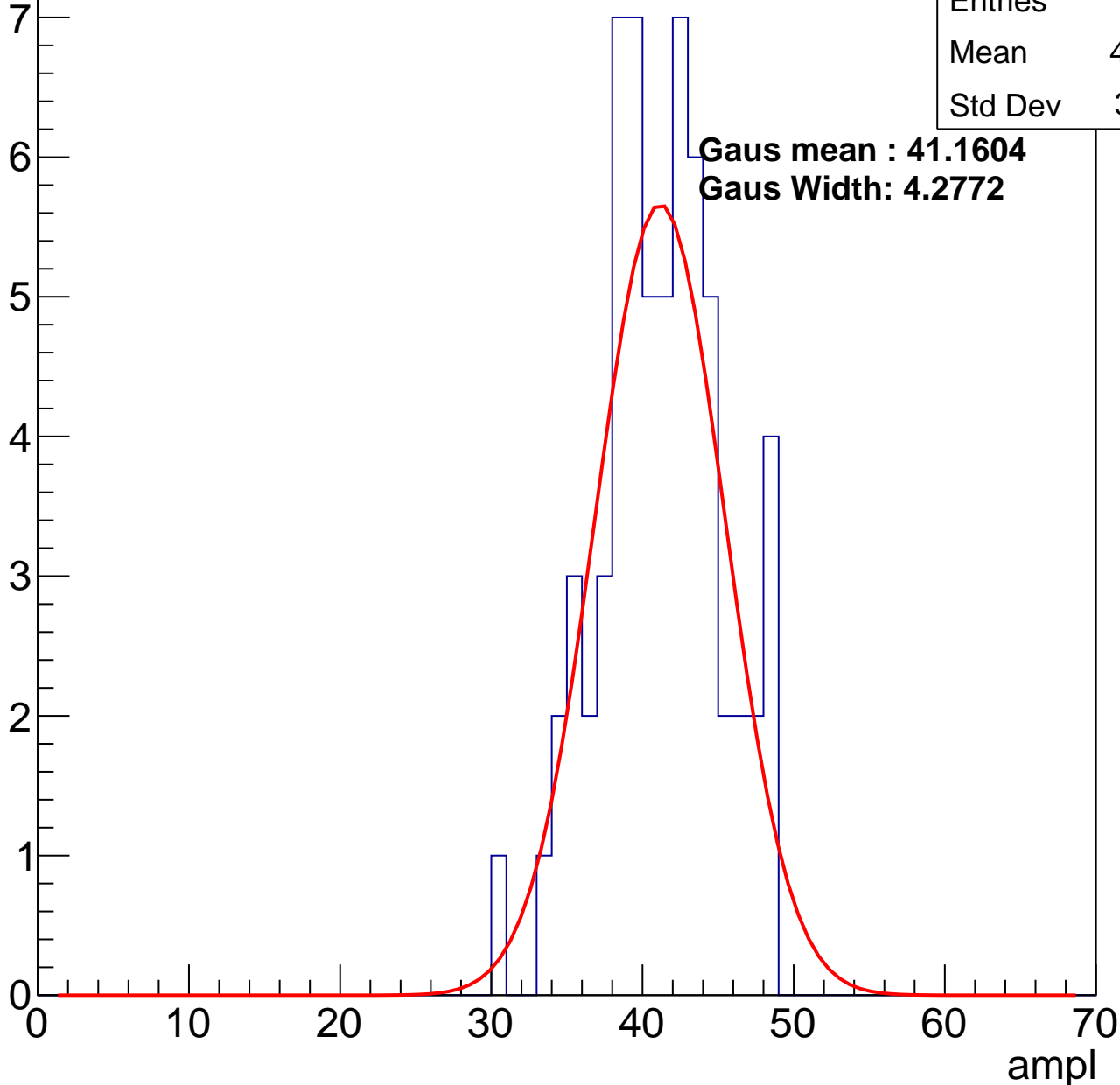
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	40.67
Std Dev	3.961

**Gaus mean : 41.1604**

**Gaus Width: 4.2772**

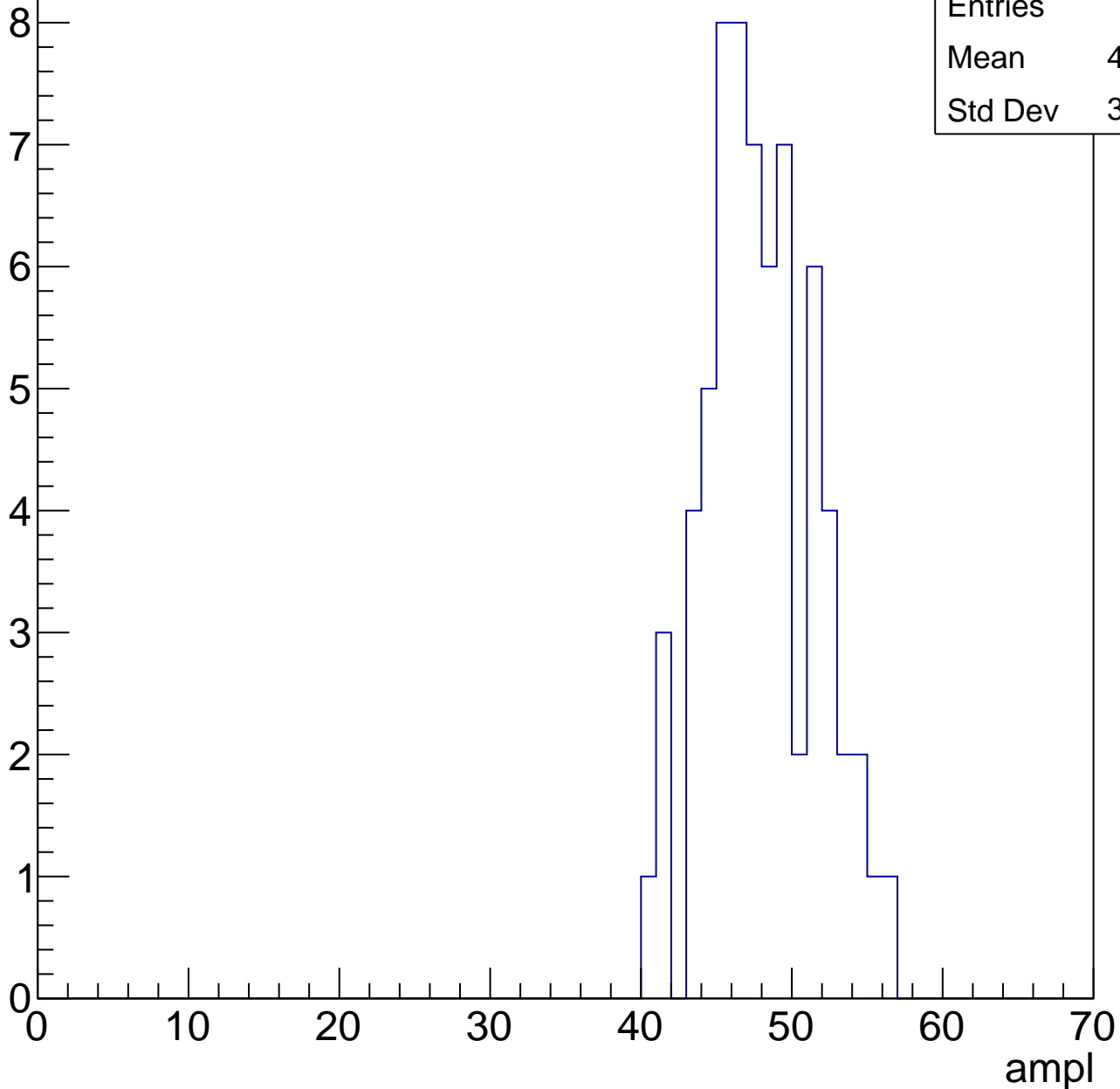


# B1L103S, U21-ch86, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	47.49
Std Dev	3.568

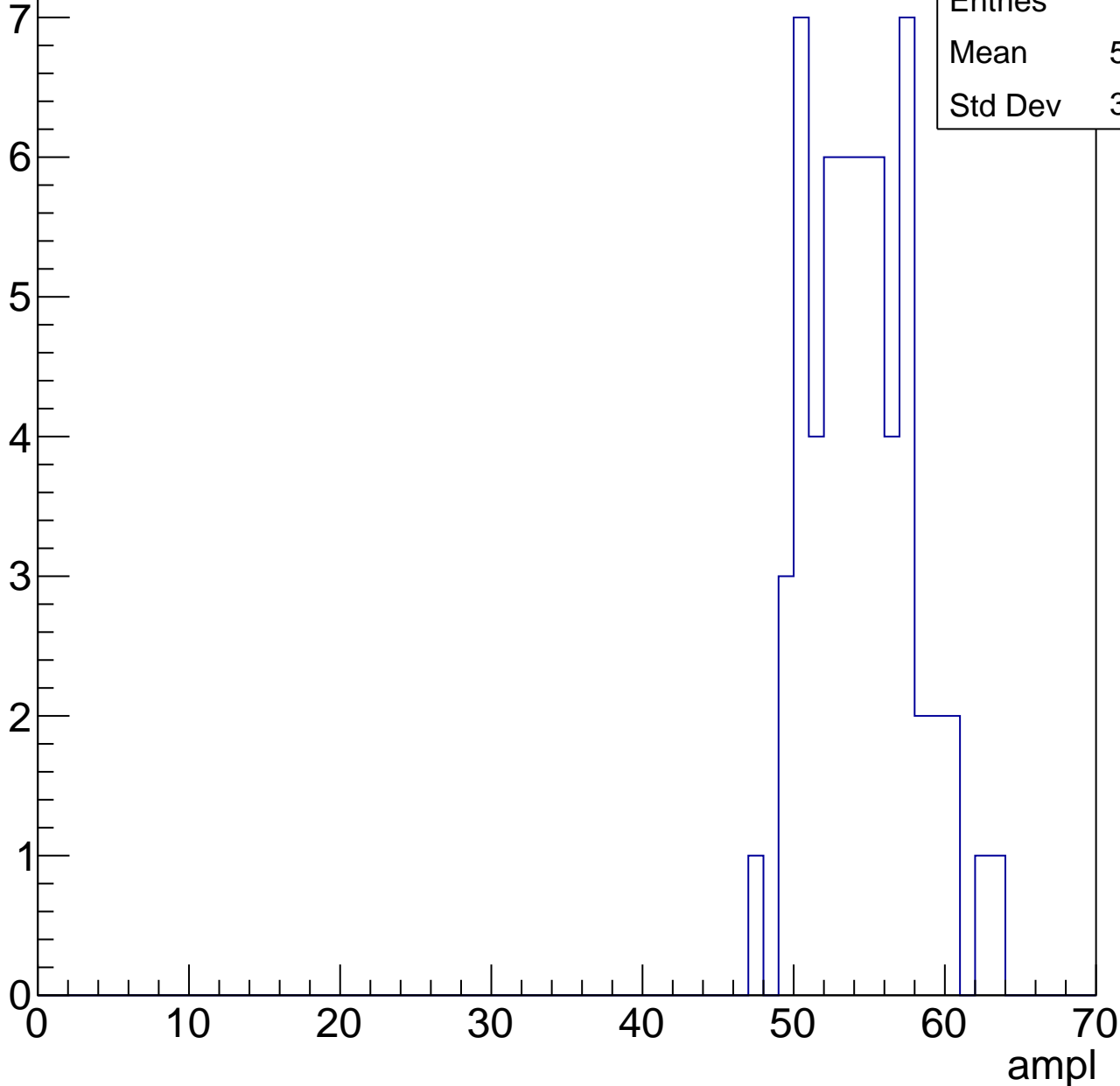


# B1L103S, U21-ch86, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	54.03
Std Dev	3.439

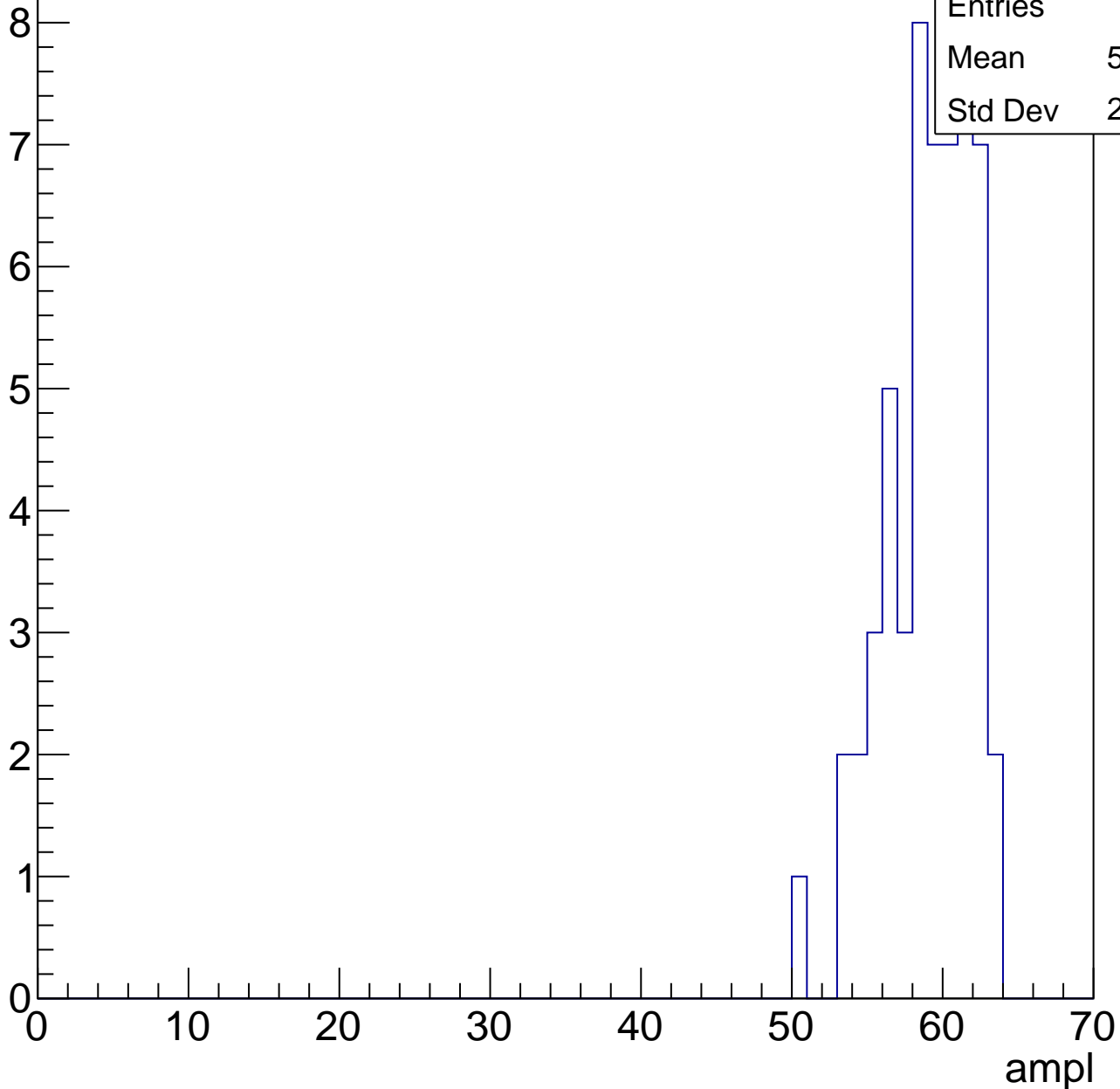


# B1L103S, U21-ch86, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

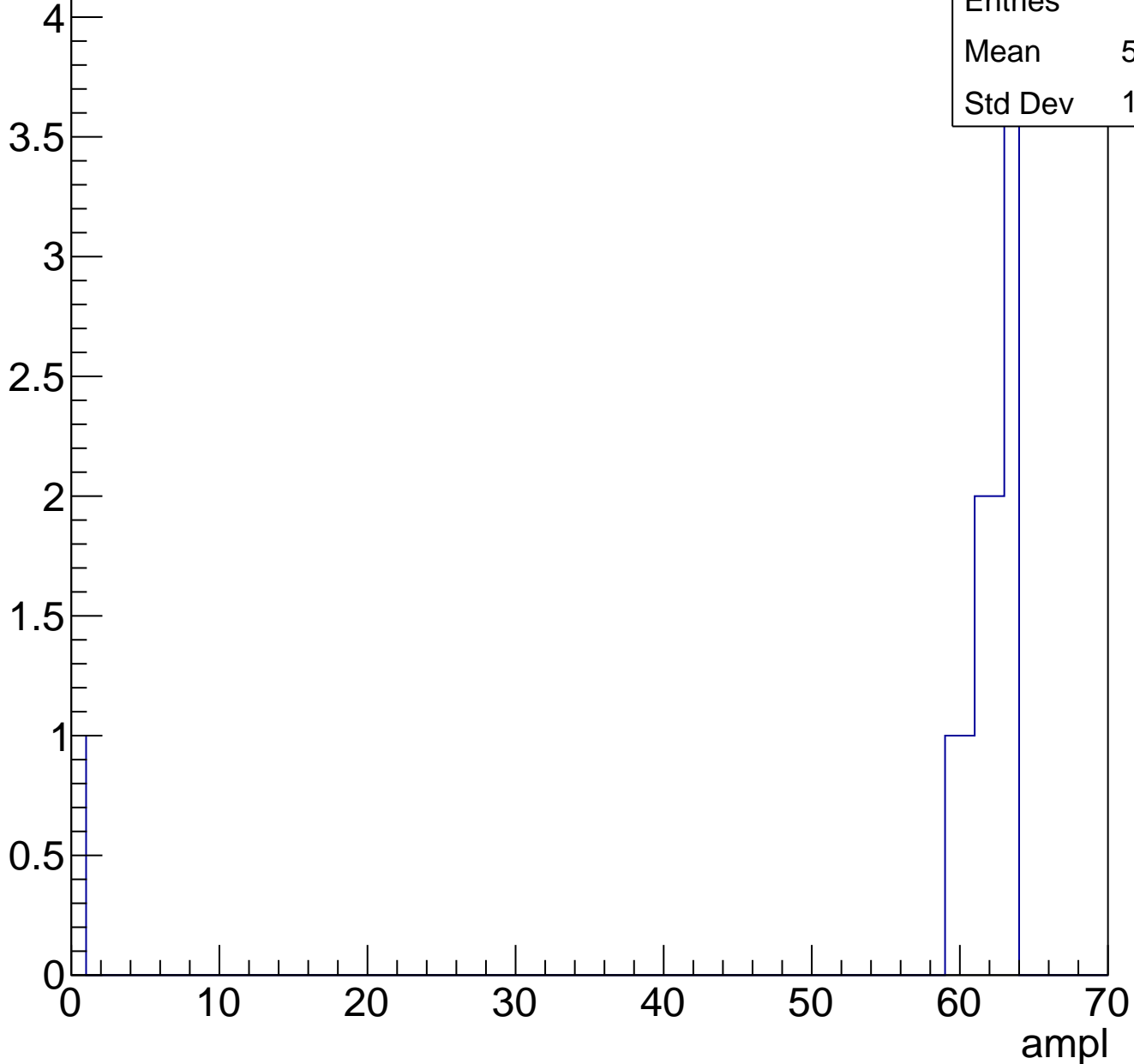
Entries	55
Mean	58.64
Std Dev	2.837



# B1L103S, U21-ch86, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U21-ch86, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U21-ch87, adc0

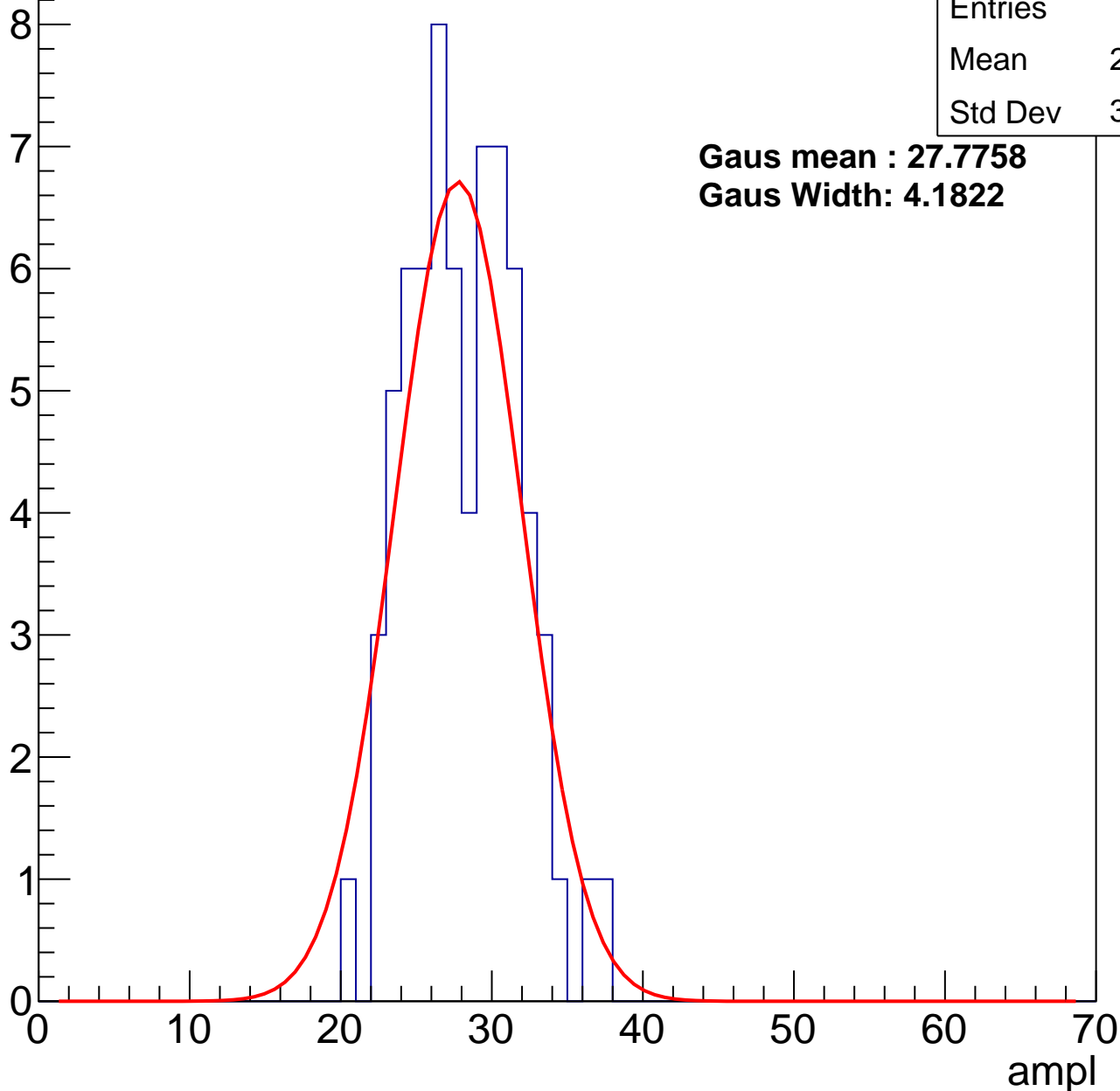
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	27.68
Std Dev	3.585

**Gaus mean : 27.7758**

**Gaus Width: 4.1822**



# B1L103S, U21-ch87, adc1

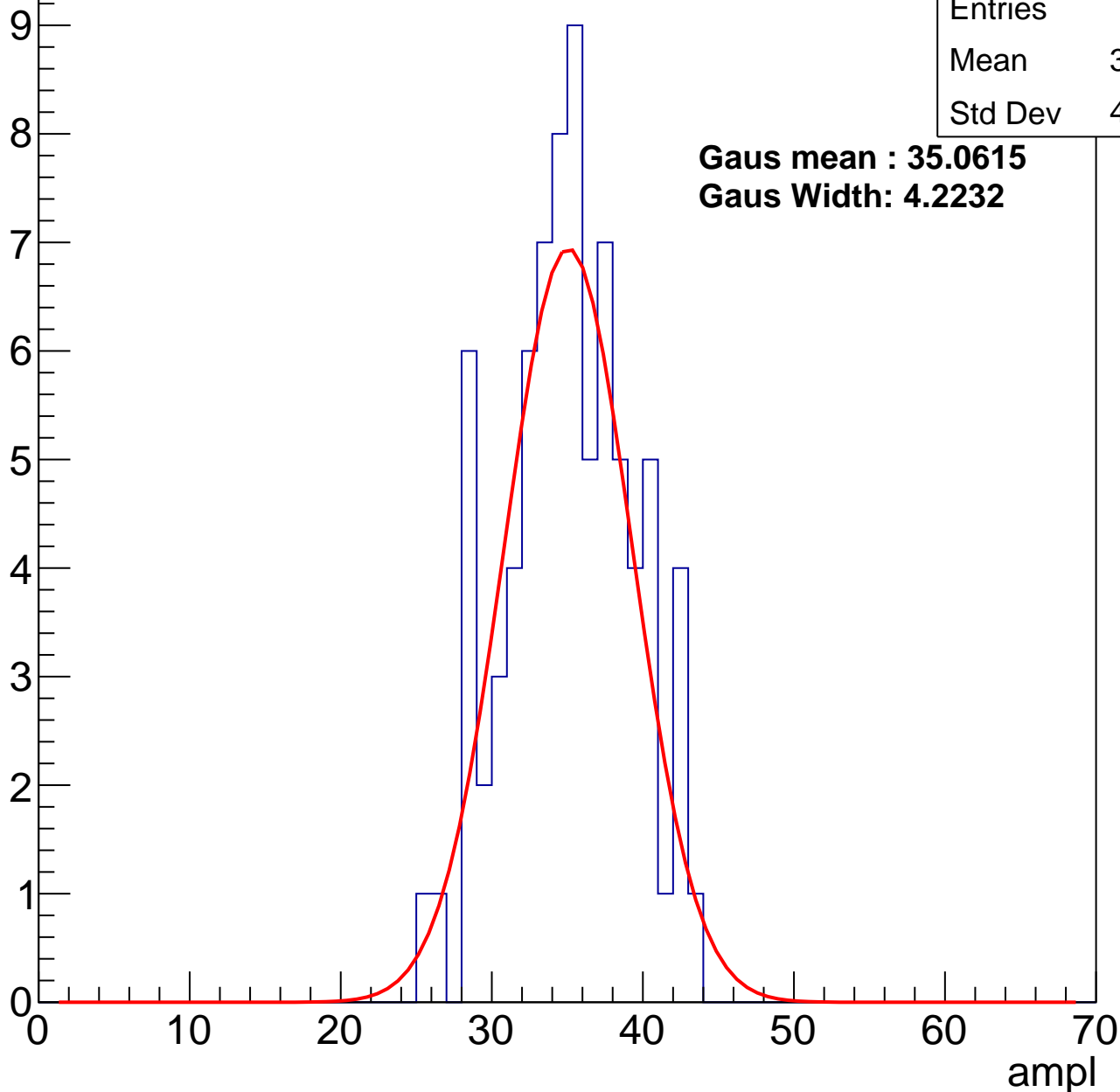
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	79
Mean	34.66
Std Dev	4.103

**Gaus mean : 35.0615**

**Gaus Width: 4.2232**



# B1L103S, U21-ch87, adc2

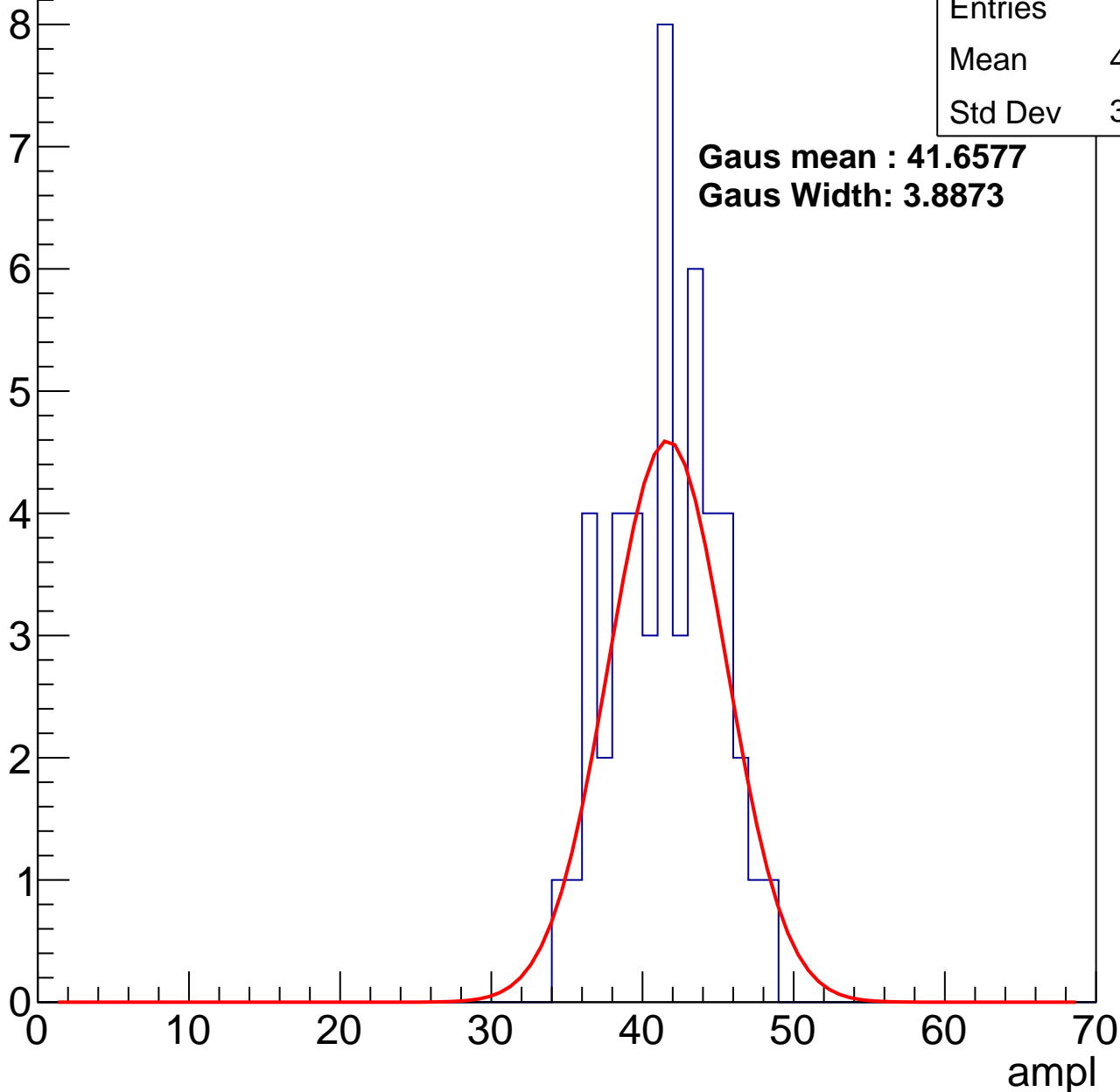
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	48
Mean	41.04
Std Dev	3.335

**Gaus mean : 41.6577**

**Gaus Width: 3.8873**

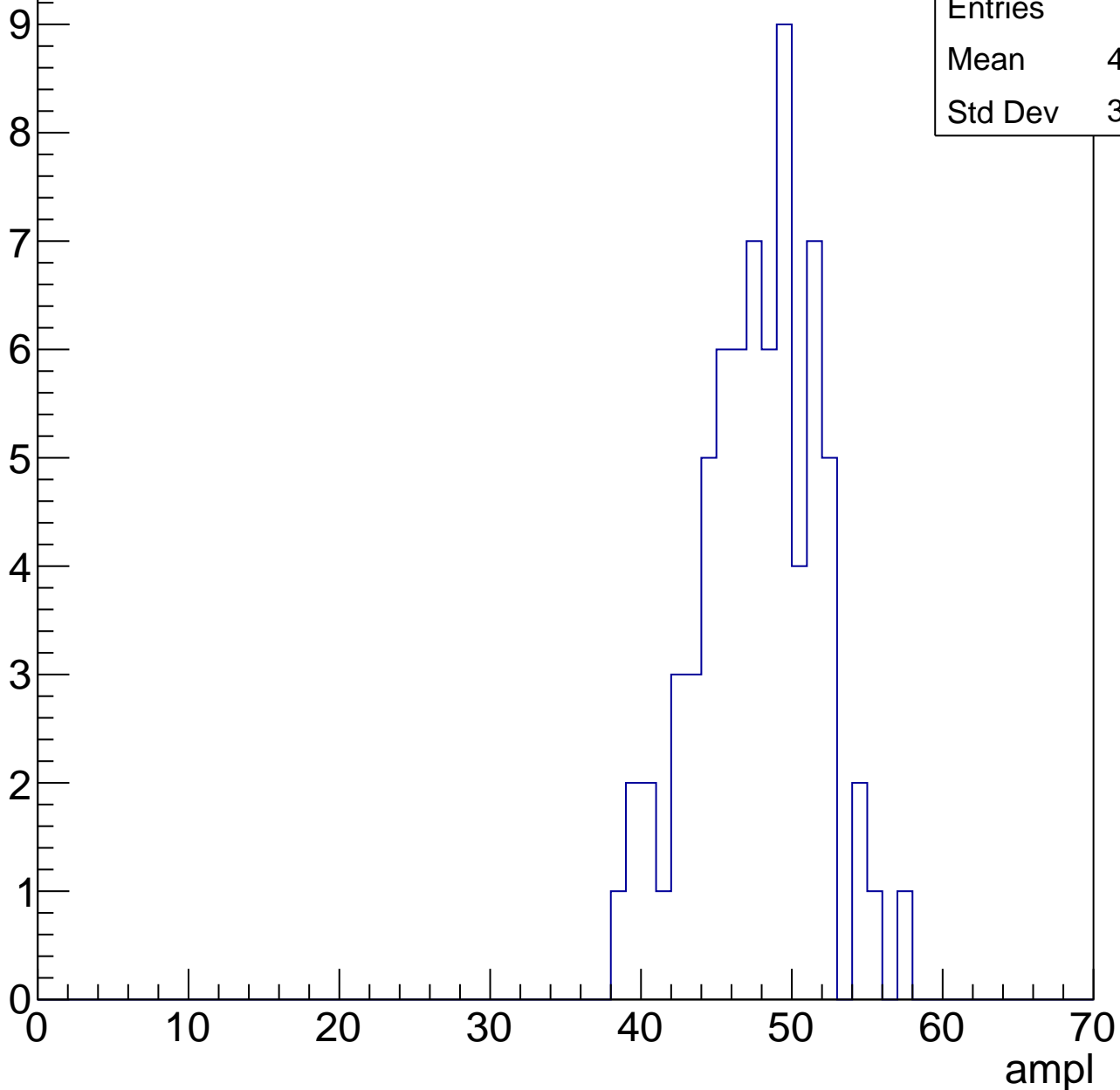


# B1L103S, U21-ch87, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	47.23
Std Dev	3.962

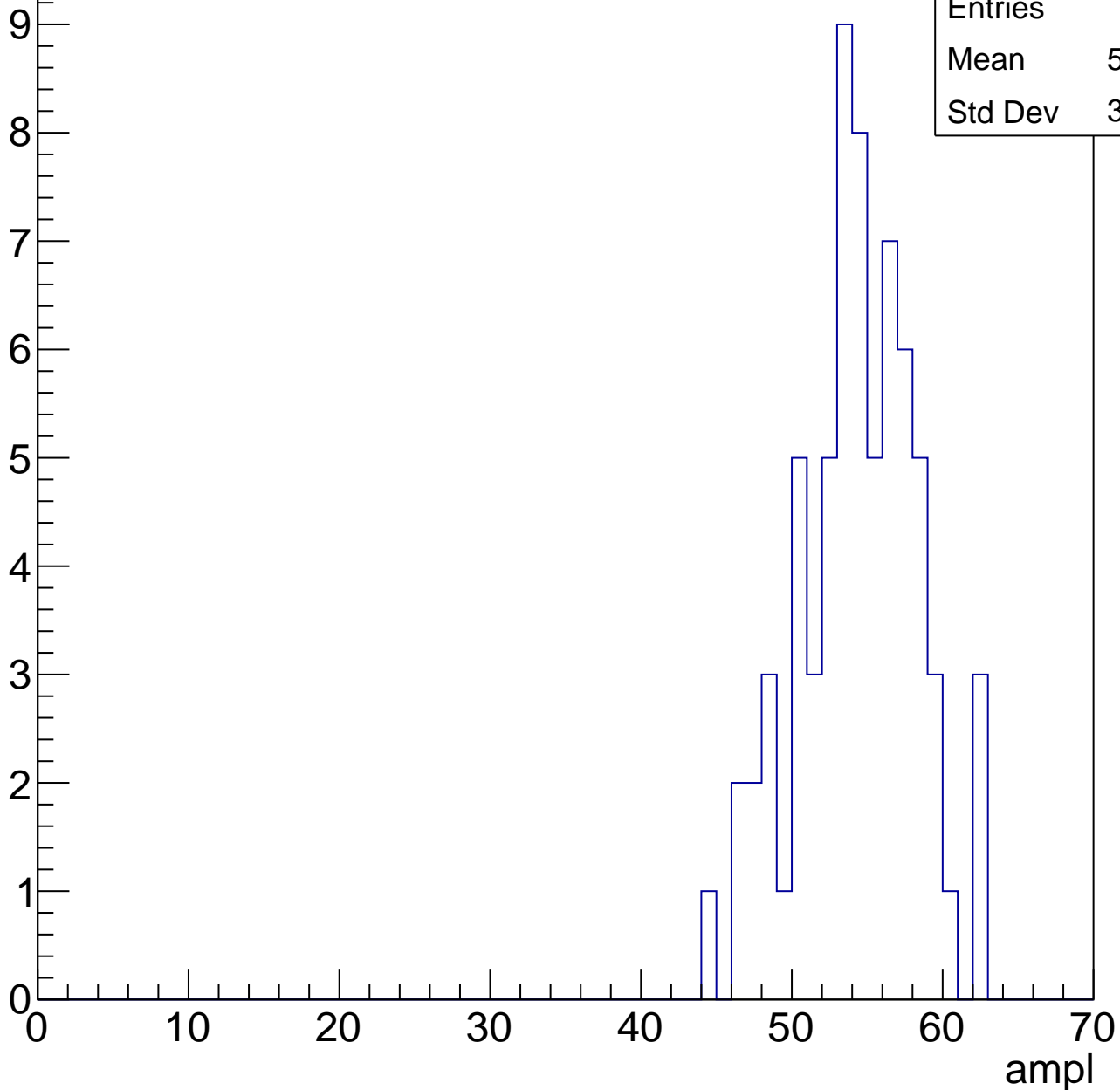


# B1L103S, U21-ch87, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	53.87
Std Dev	3.927

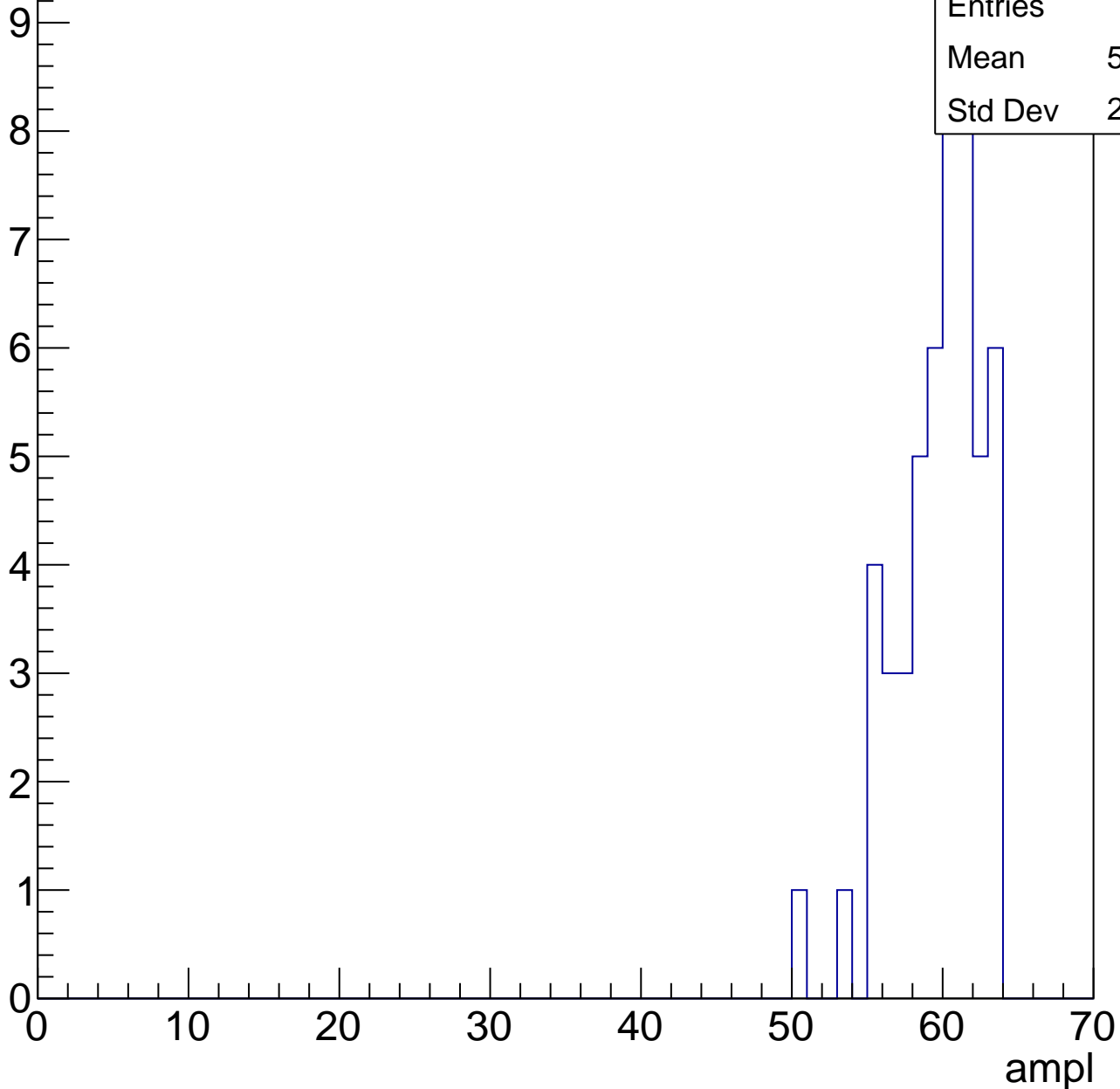


# B1L103S, U21-ch87, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

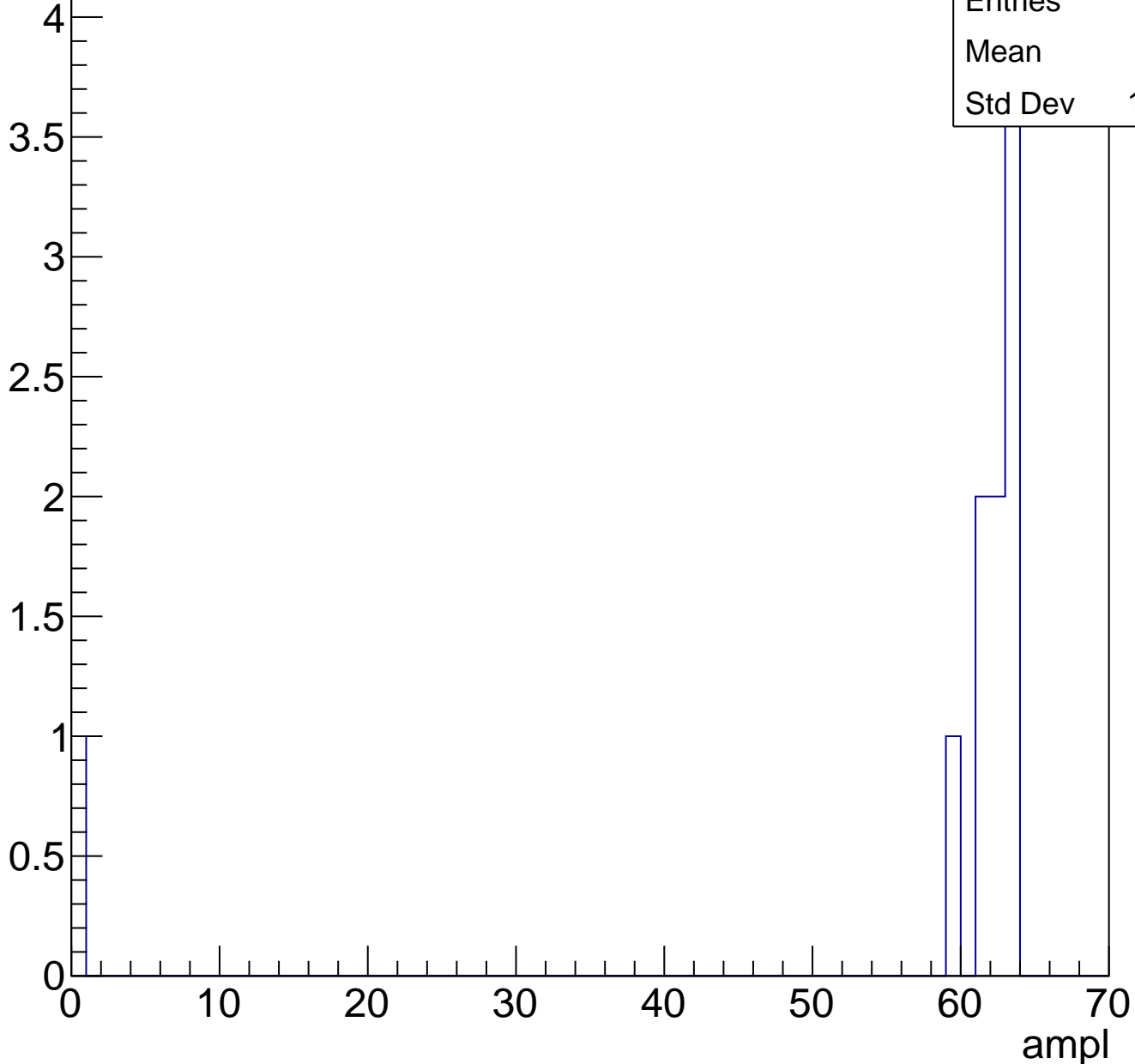
Entries	51
Mean	59.25
Std Dev	2.813



# B1L103S, U21-ch87, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

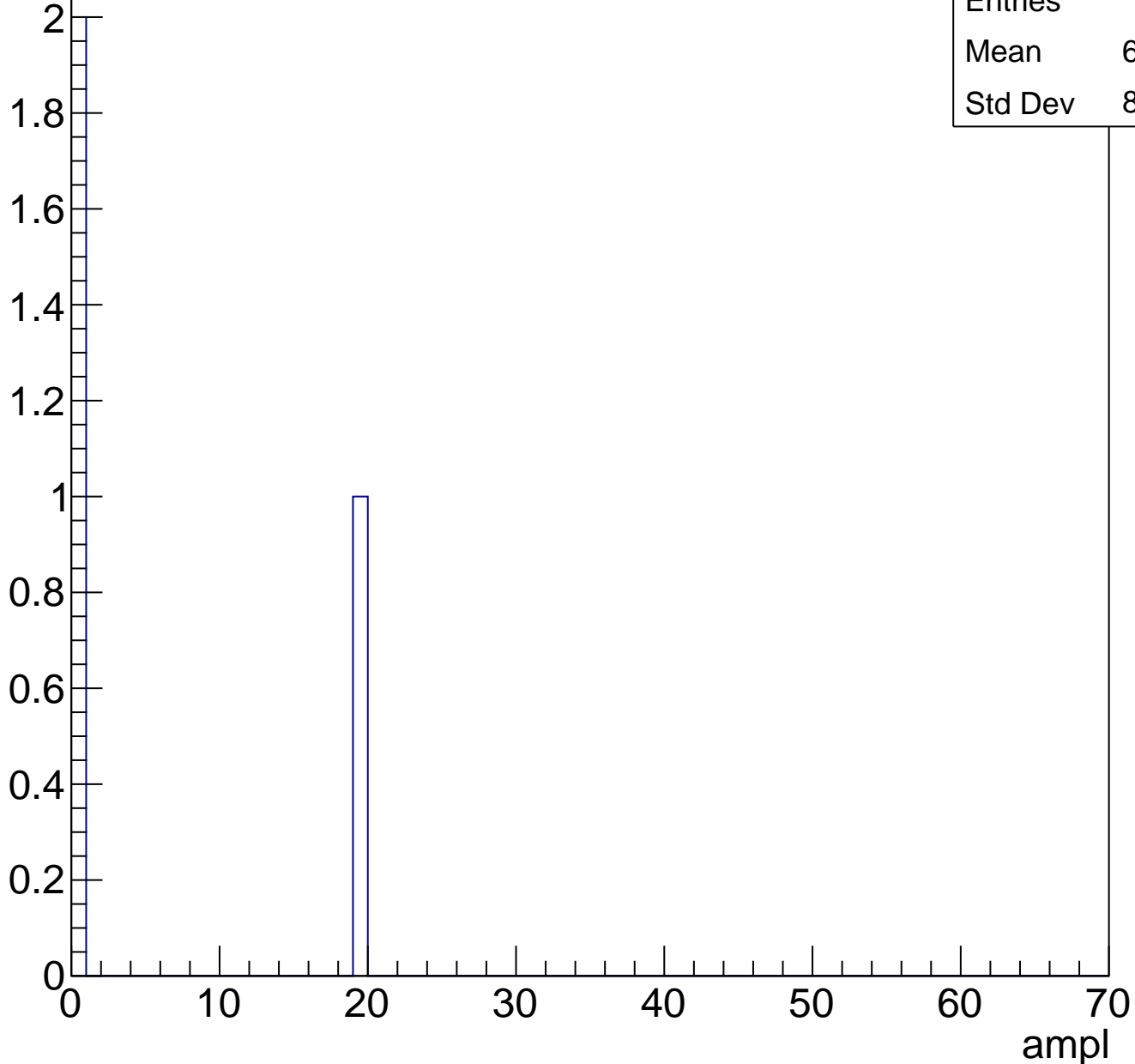




# B1L103S, U21-ch87, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	3
Mean	6.333
Std Dev	8.957

# B1L103S, U21-ch88, adc0

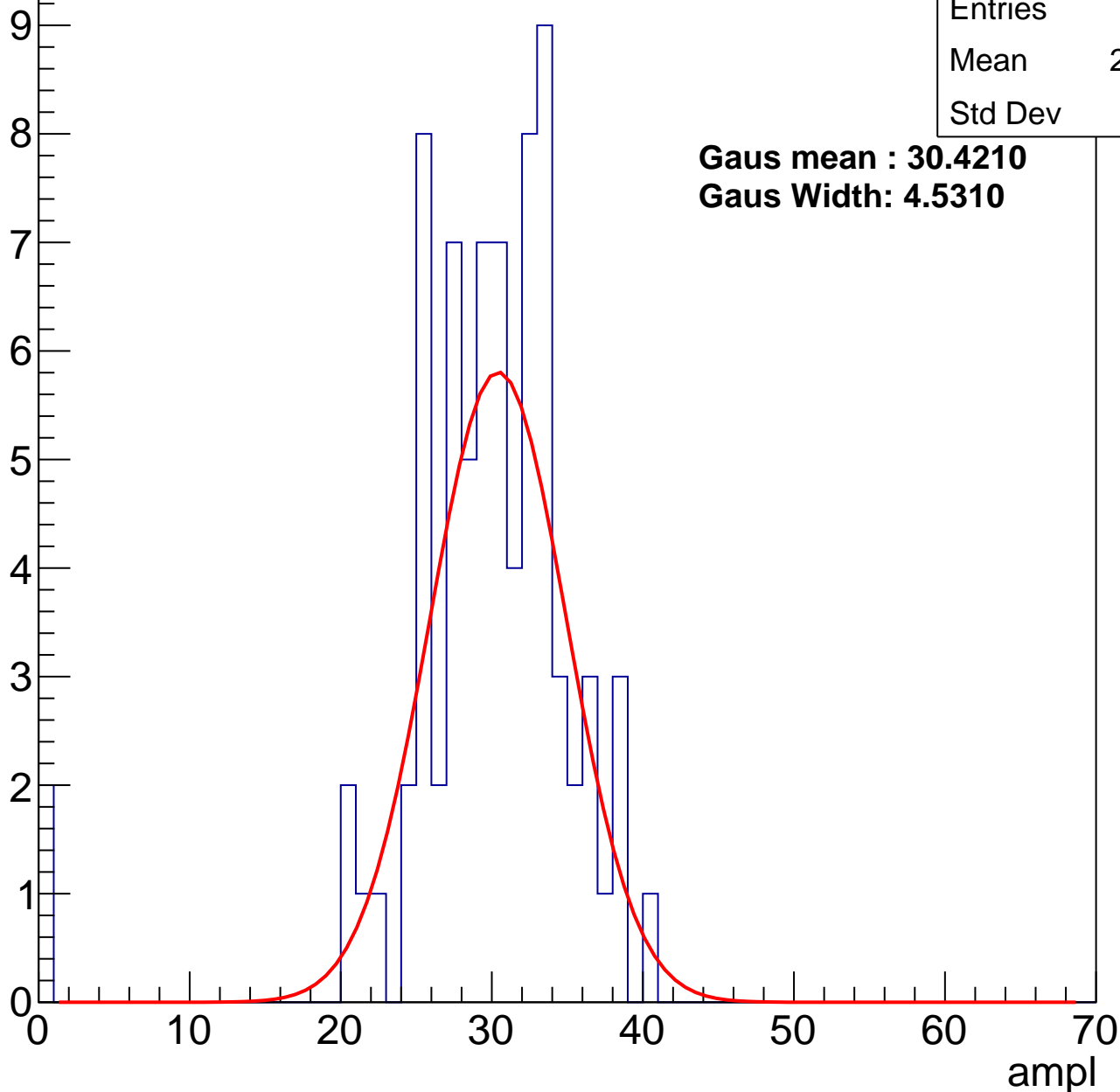
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	29.14
Std Dev	6.35

**Gaus mean : 30.4210**

**Gaus Width: 4.5310**



# B1L103S, U21-ch88, adc1

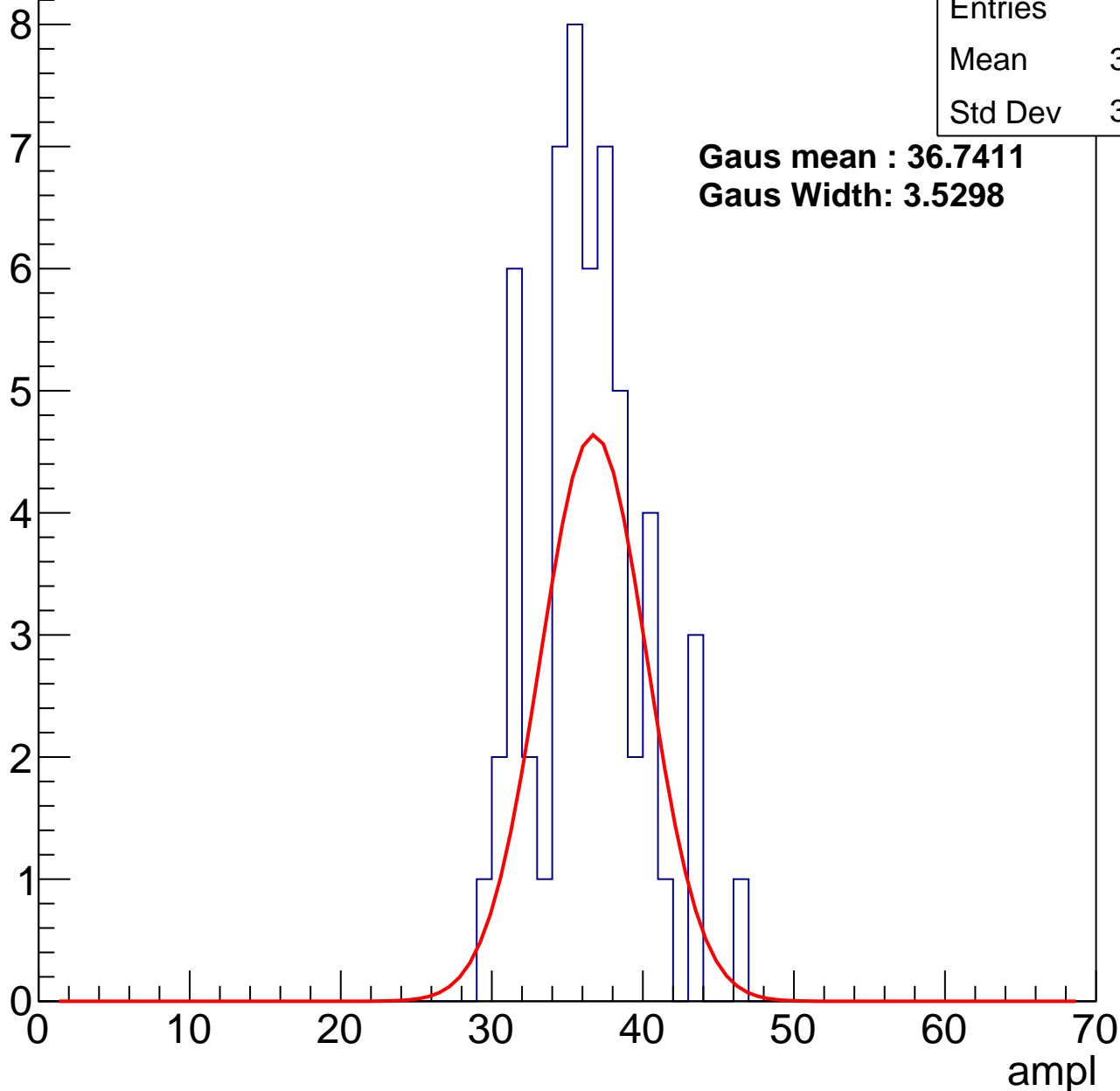
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	35.88
Std Dev	3.606

**Gaus mean : 36.7411**

**Gaus Width: 3.5298**



# B1L103S, U21-ch88, adc2

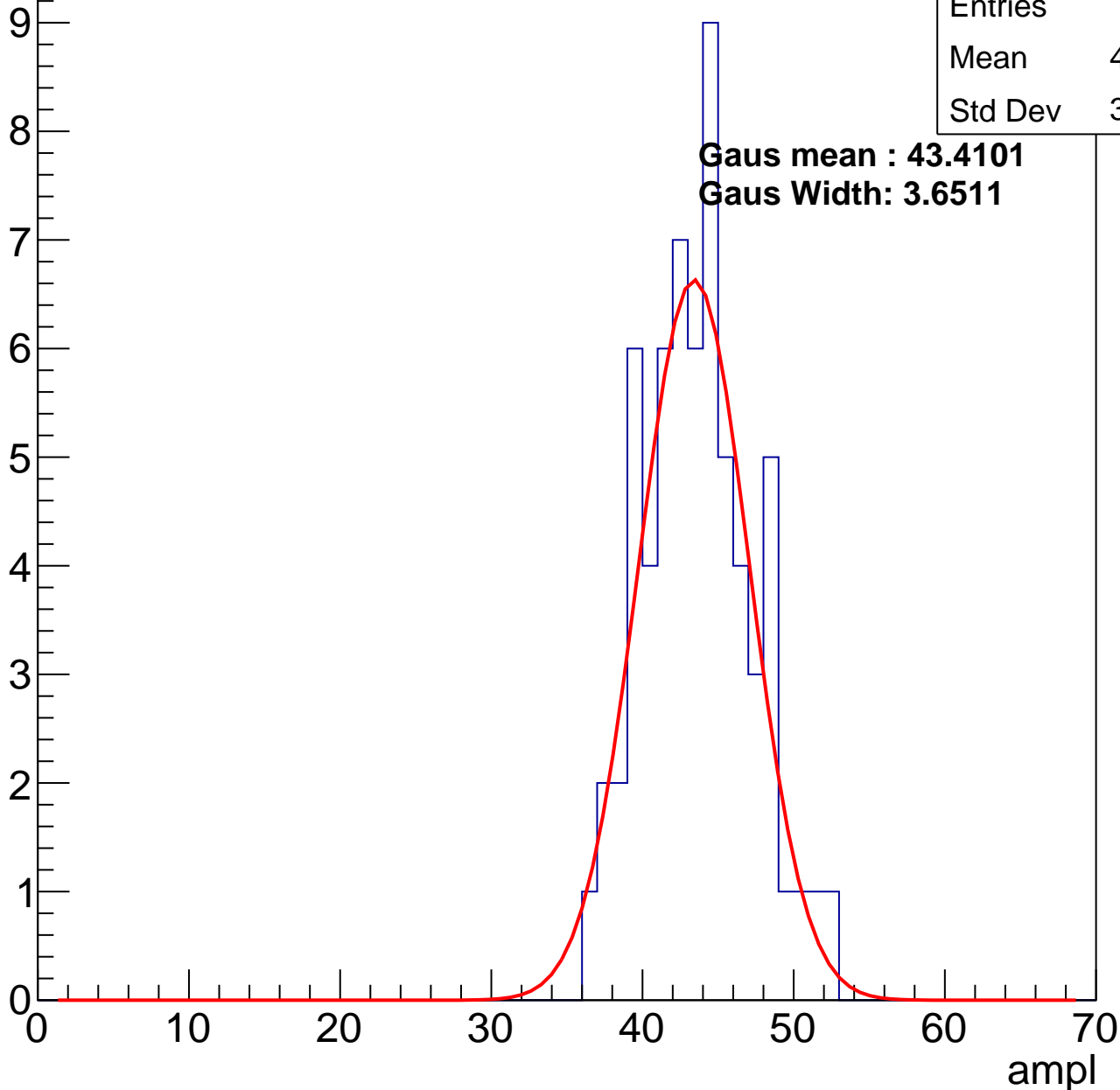
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	43.22
Std Dev	3.533

**Gaus mean : 43.4101**

**Gaus Width: 3.6511**

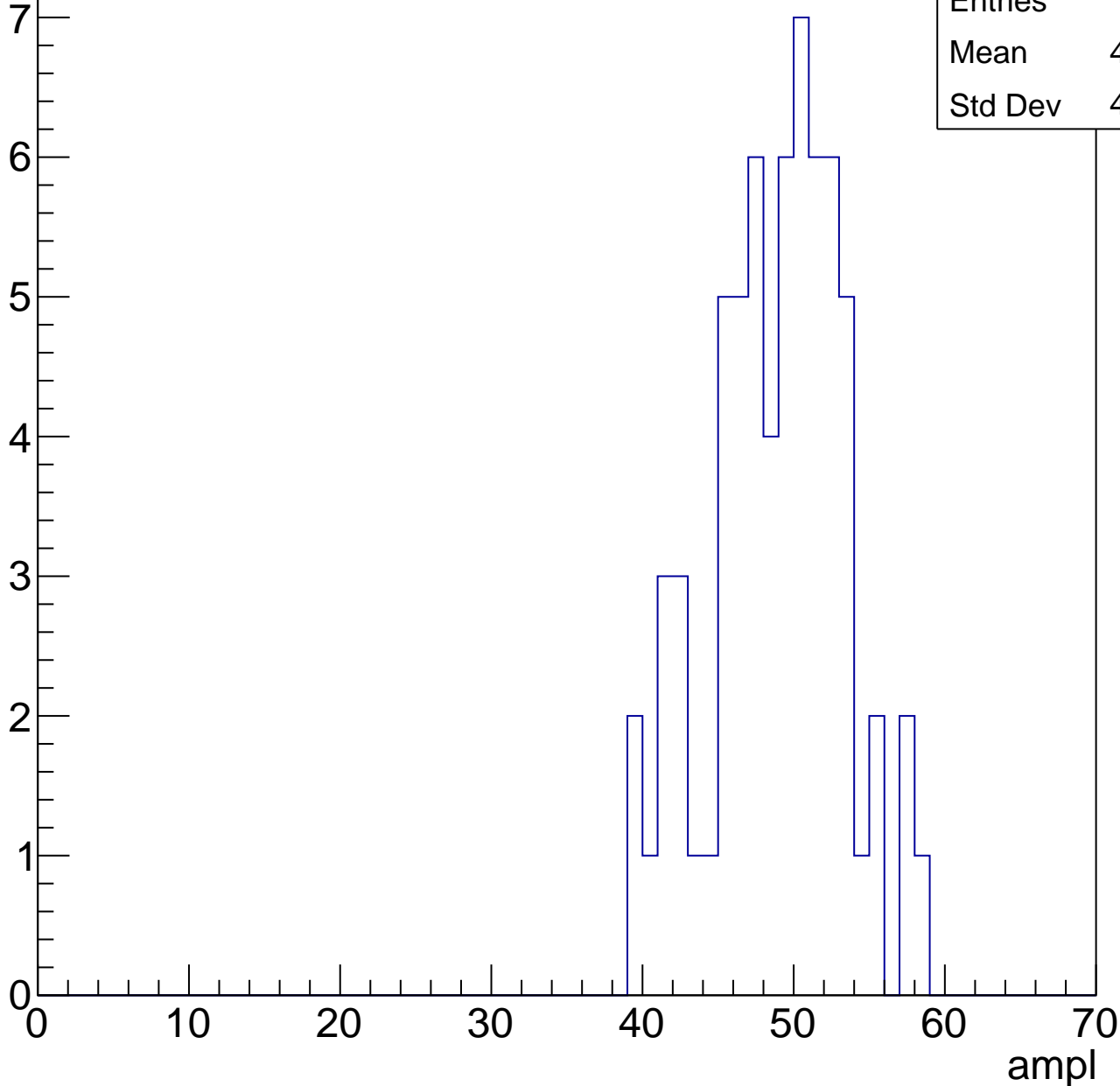


# B1L103S, U21-ch88, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	48.45
Std Dev	4.379

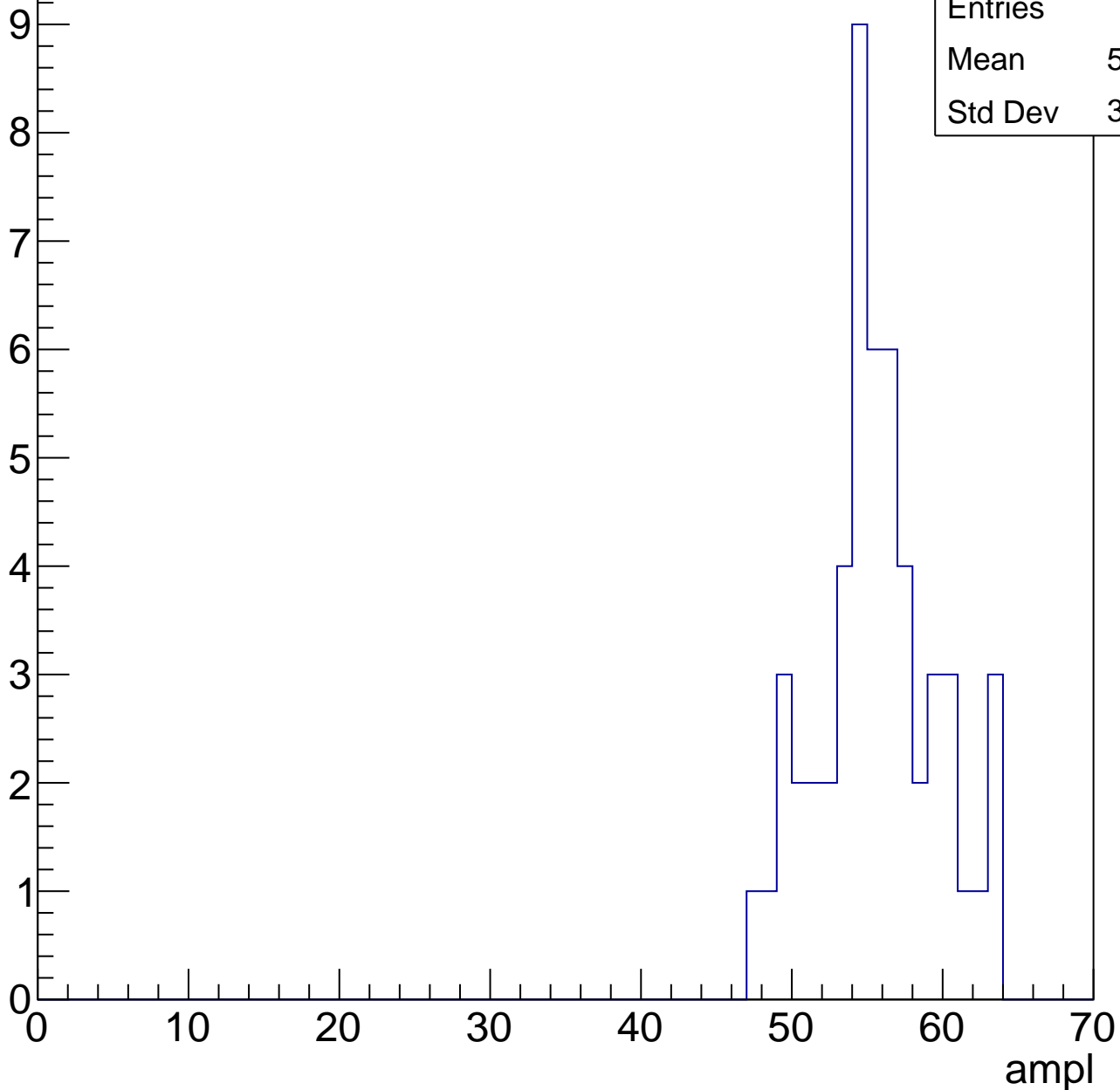


# B1L103S, U21-ch88, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	55.19
Std Dev	3.846

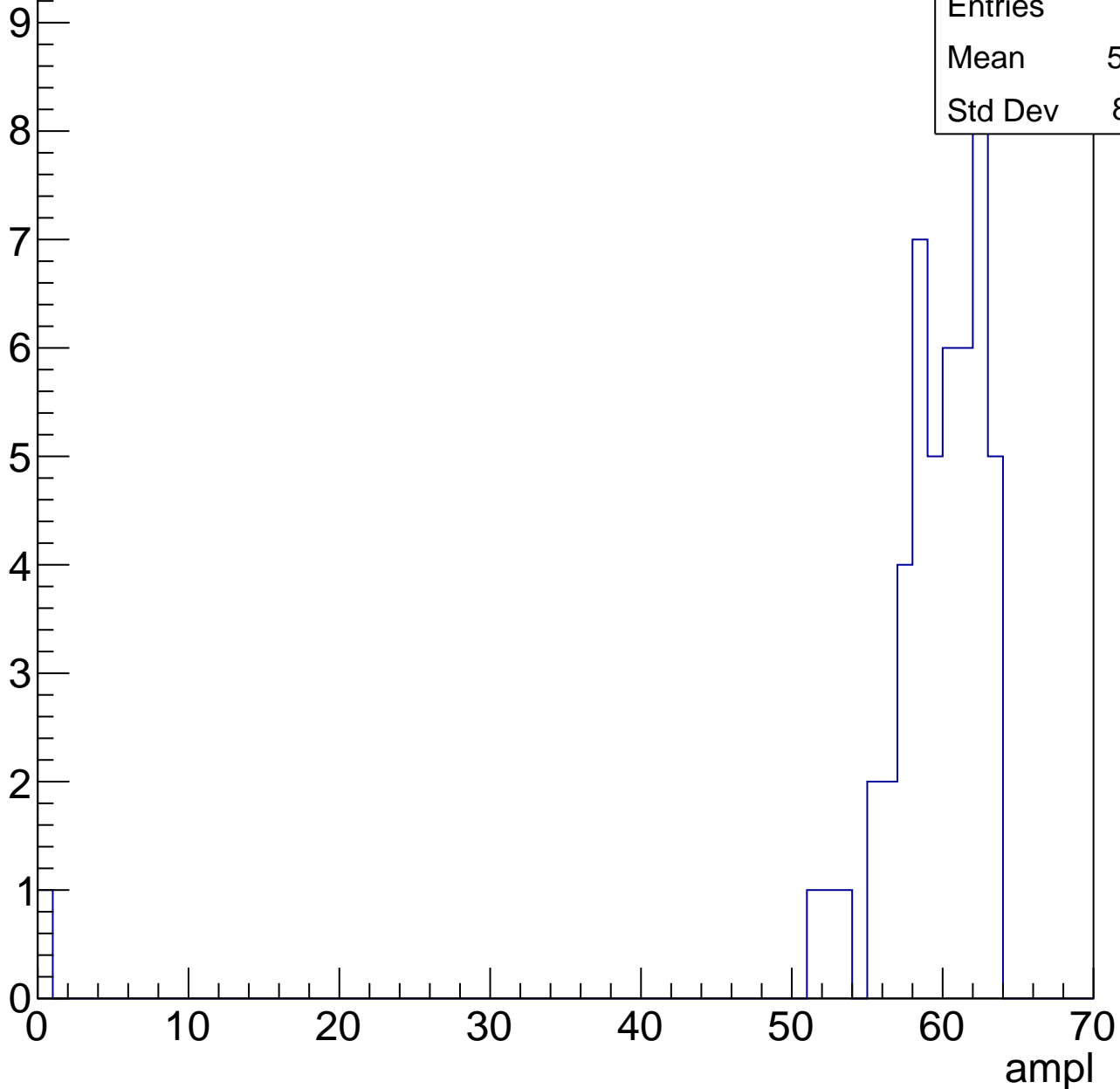


# B1L103S, U21-ch88, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	58.12
Std Dev	8.781



# B1L103S, U21-ch88, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries

9

Mean

59.56

Std Dev

2.217

3

2.5

2

1.5

1

0.5

0

10

20

30

40

50

60

70

ampl

Entries

9

Mean

59.56

Std Dev

2.217



# B1L103S, U21-ch88, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U21-ch89, adc0

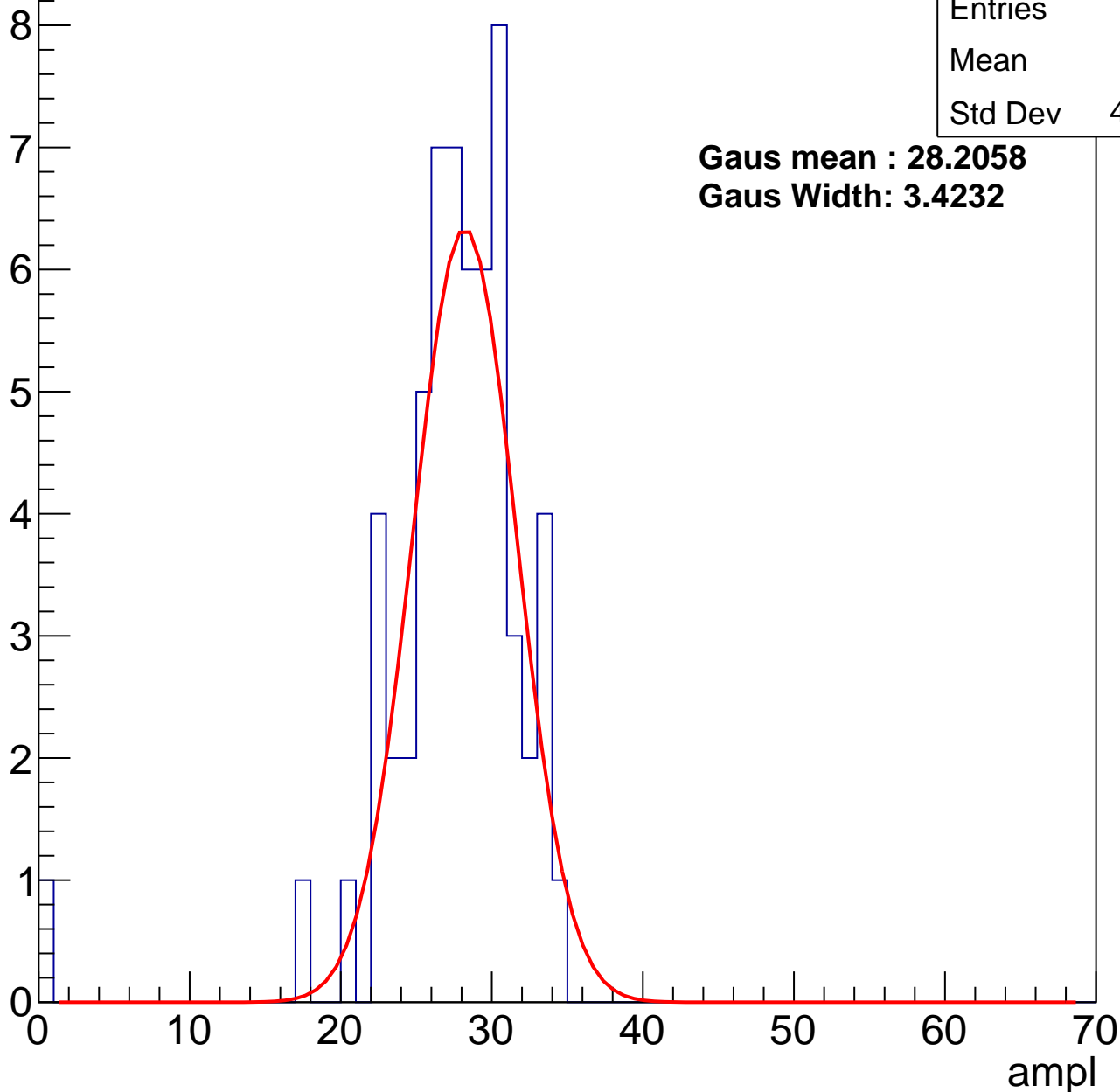
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	27
Std Dev	4.913

**Gaus mean : 28.2058**

**Gaus Width: 3.4232**



# B1L103S, U21-ch89, adc1

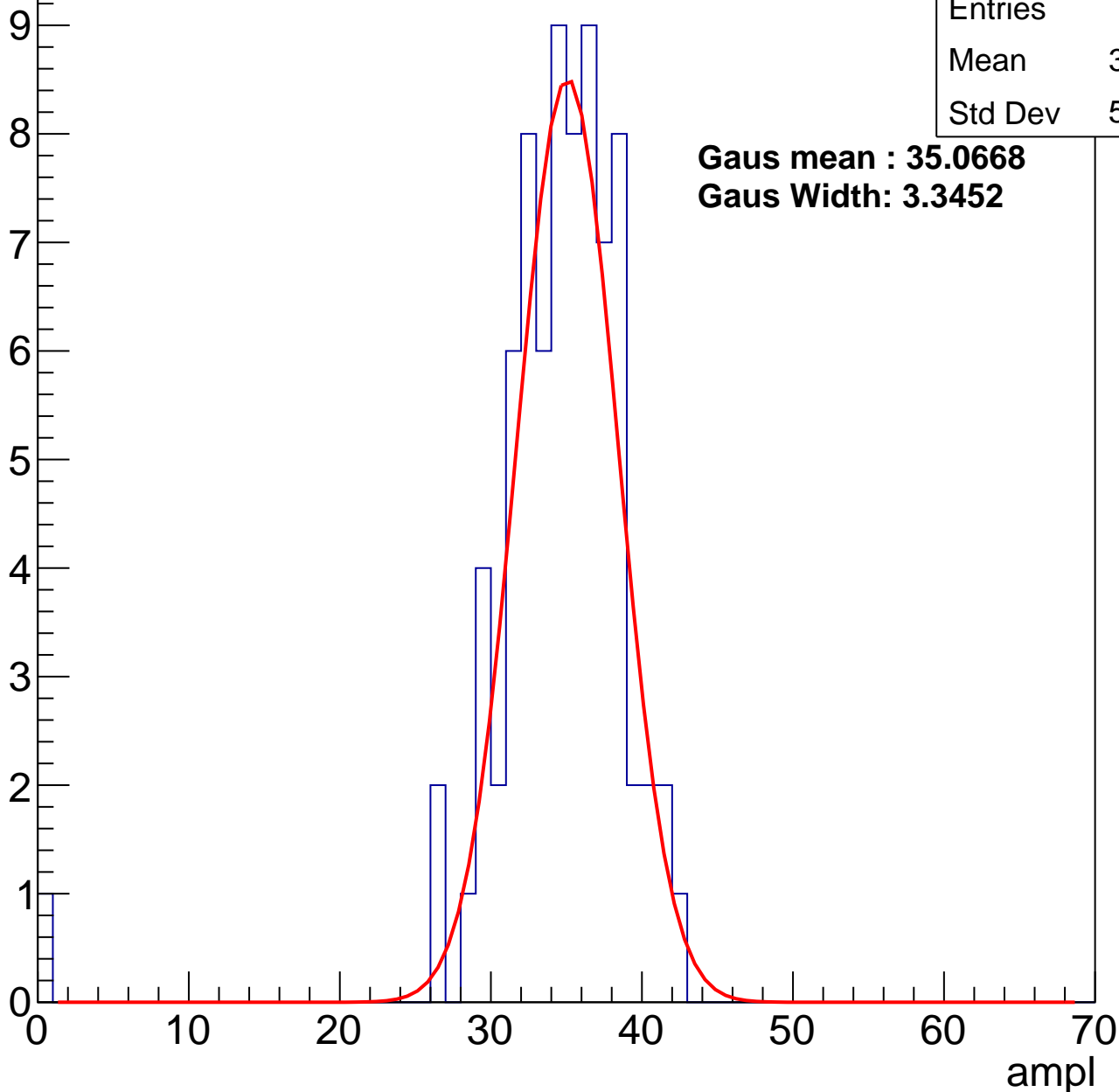
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	33.99
Std Dev	5.143

**Gaus mean : 35.0668**

**Gaus Width: 3.3452**



# B1L103S, U21-ch89, adc2

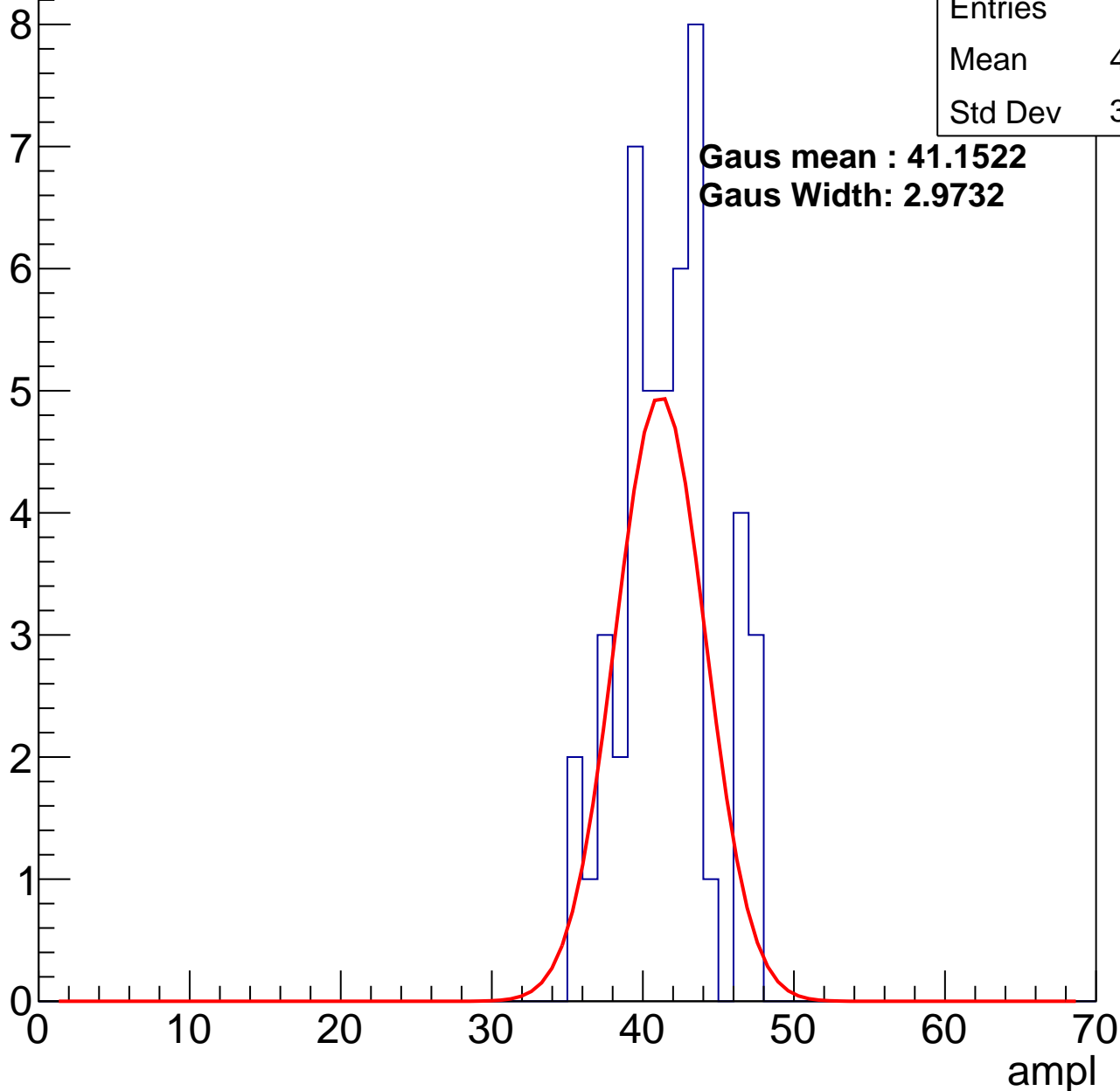
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	47
Mean	41.19
Std Dev	3.092

**Gaus mean : 41.1522**

**Gaus Width: 2.9732**

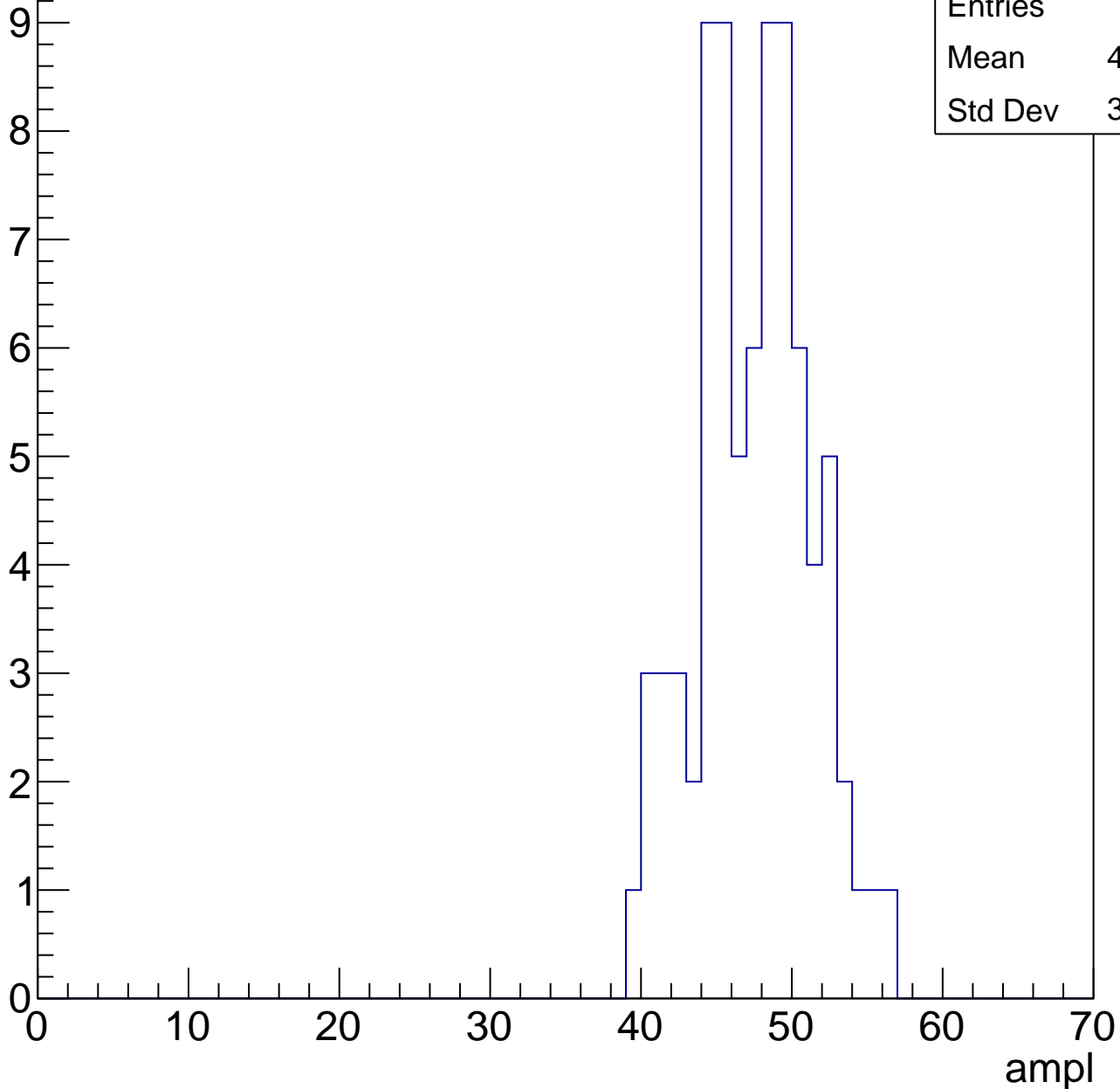


# B1L103S, U21-ch89, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	79
Mean	47.03
Std Dev	3.735

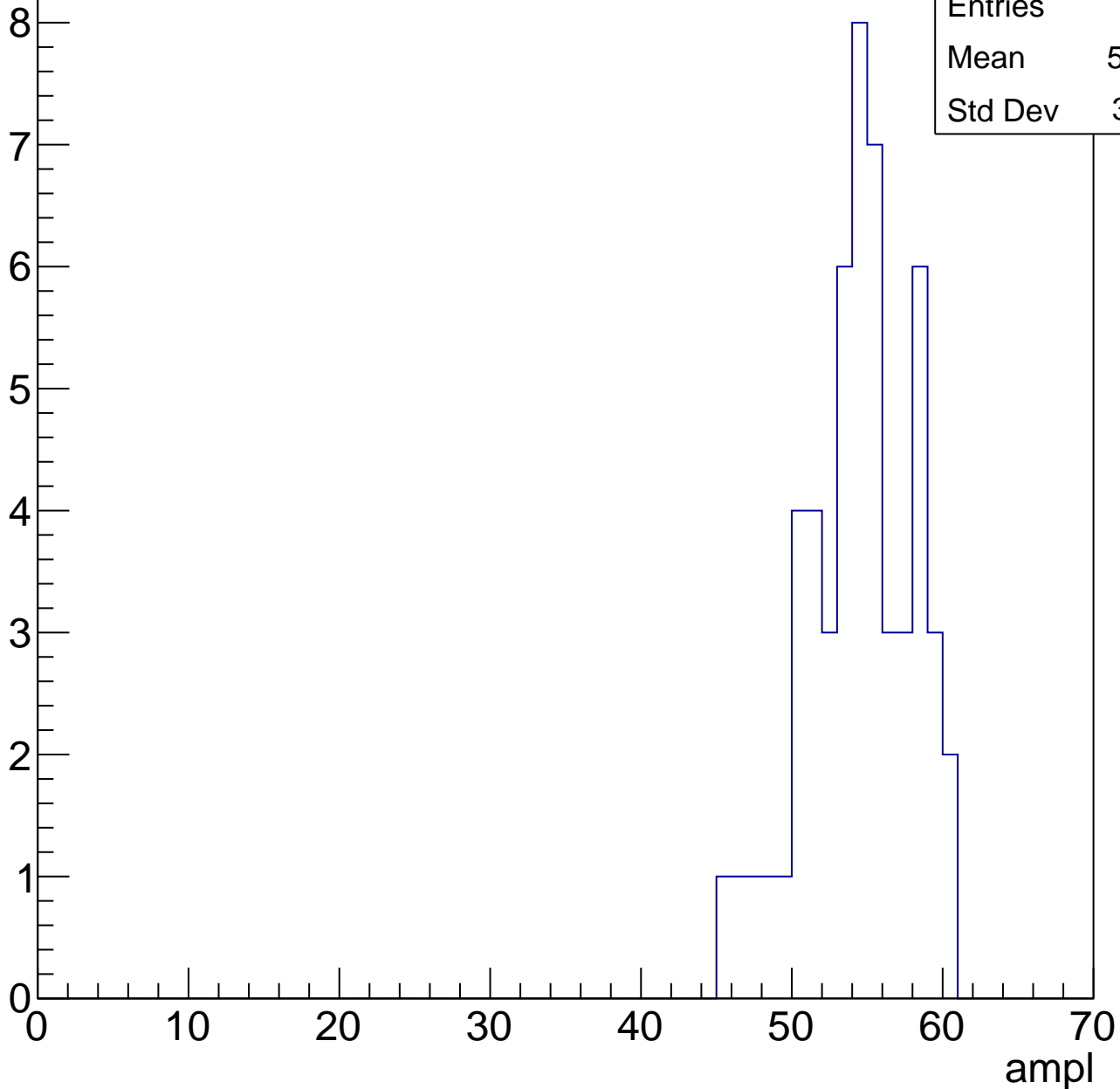


# B1L103S, U21-ch89, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	53.96
Std Dev	3.501

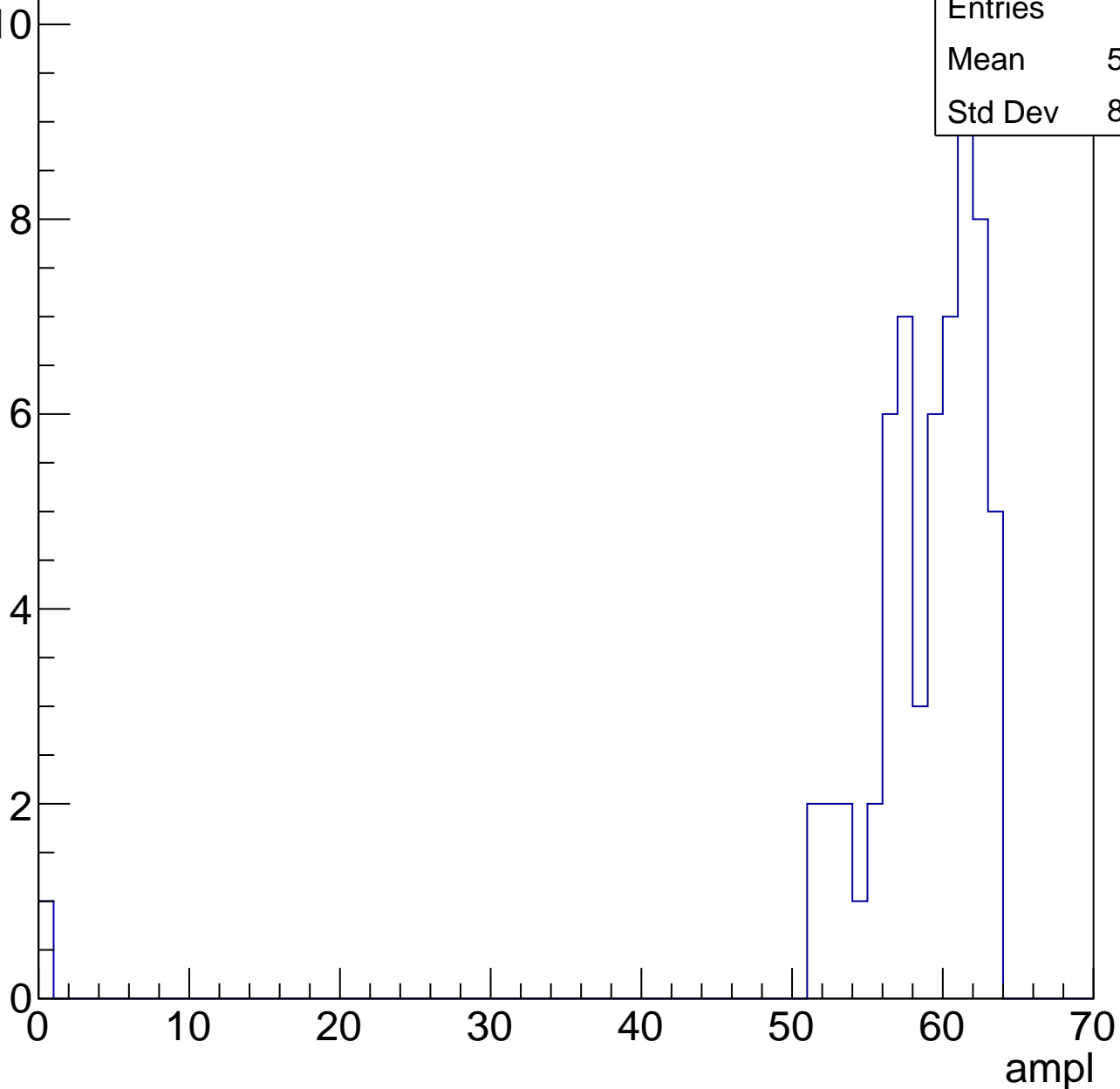


# B1L103S, U21-ch89, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	57.74
Std Dev	8.054

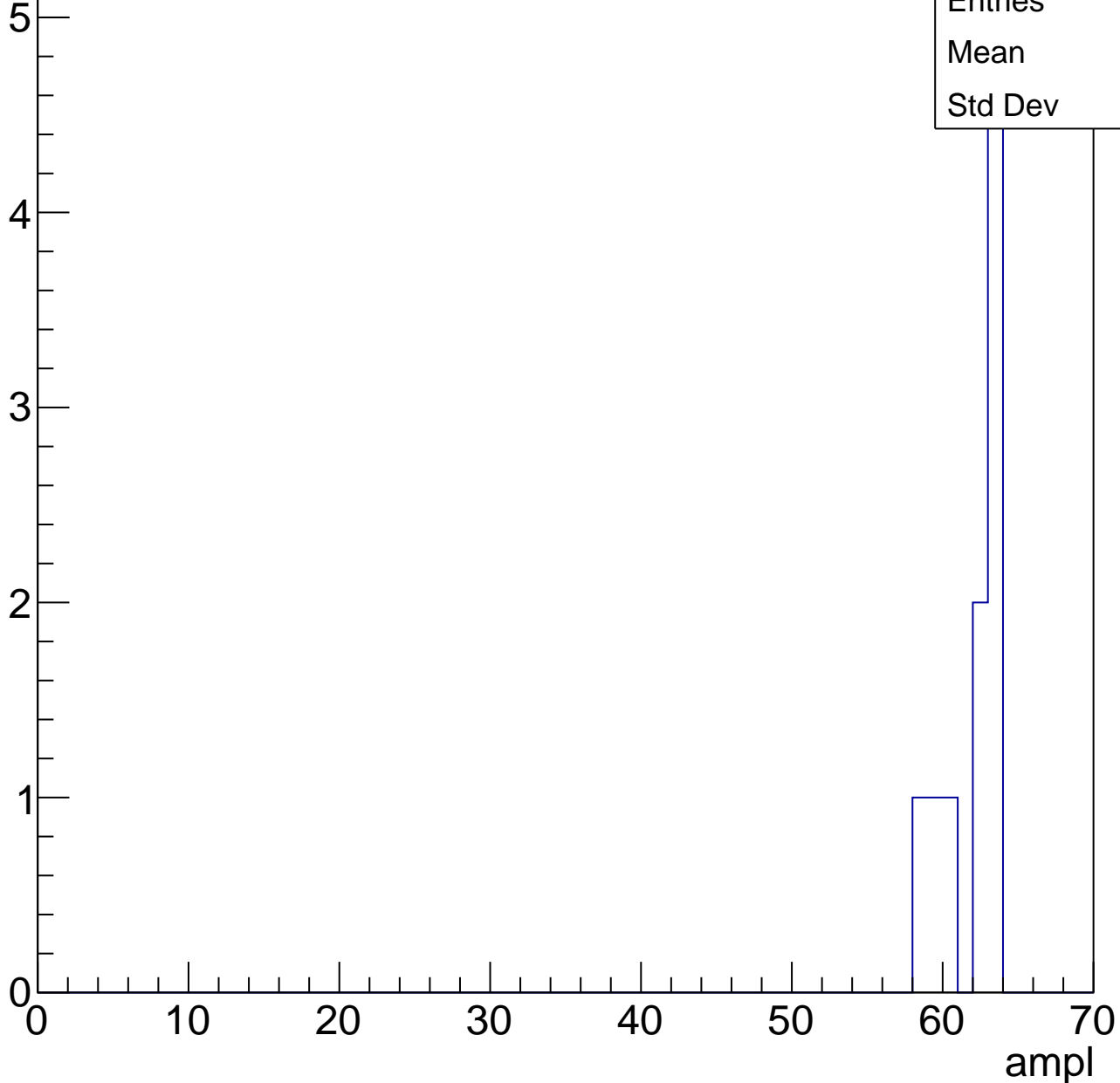


# B1L103S, U21-ch89, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	10
Mean	61.6
Std Dev	1.8





# B1L103S, U21-ch89, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U21-ch90, adc0

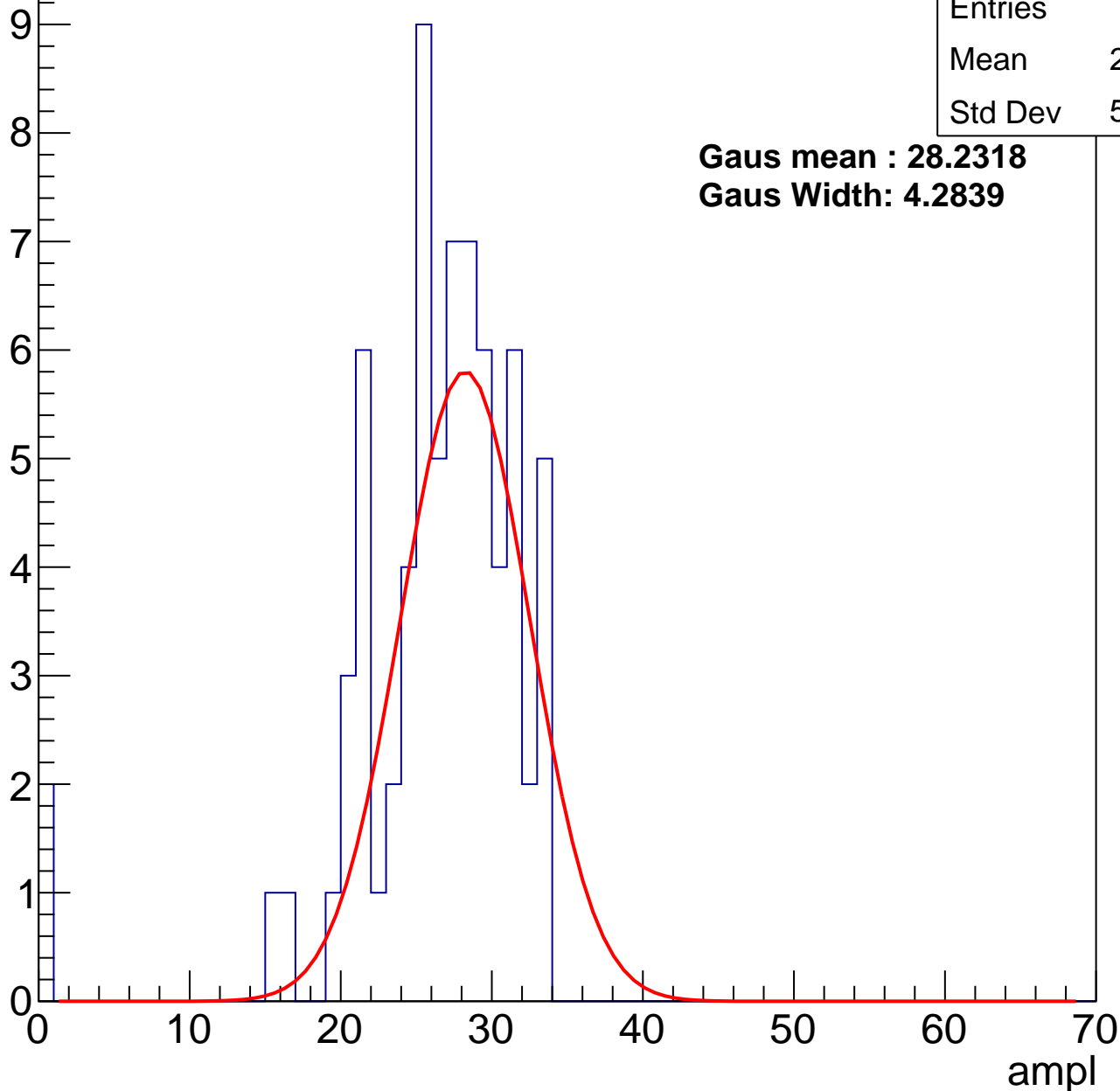
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	25.68
Std Dev	5.953

**Gaus mean : 28.2318**

**Gaus Width: 4.2839**



# B1L103S, U21-ch90, adc1

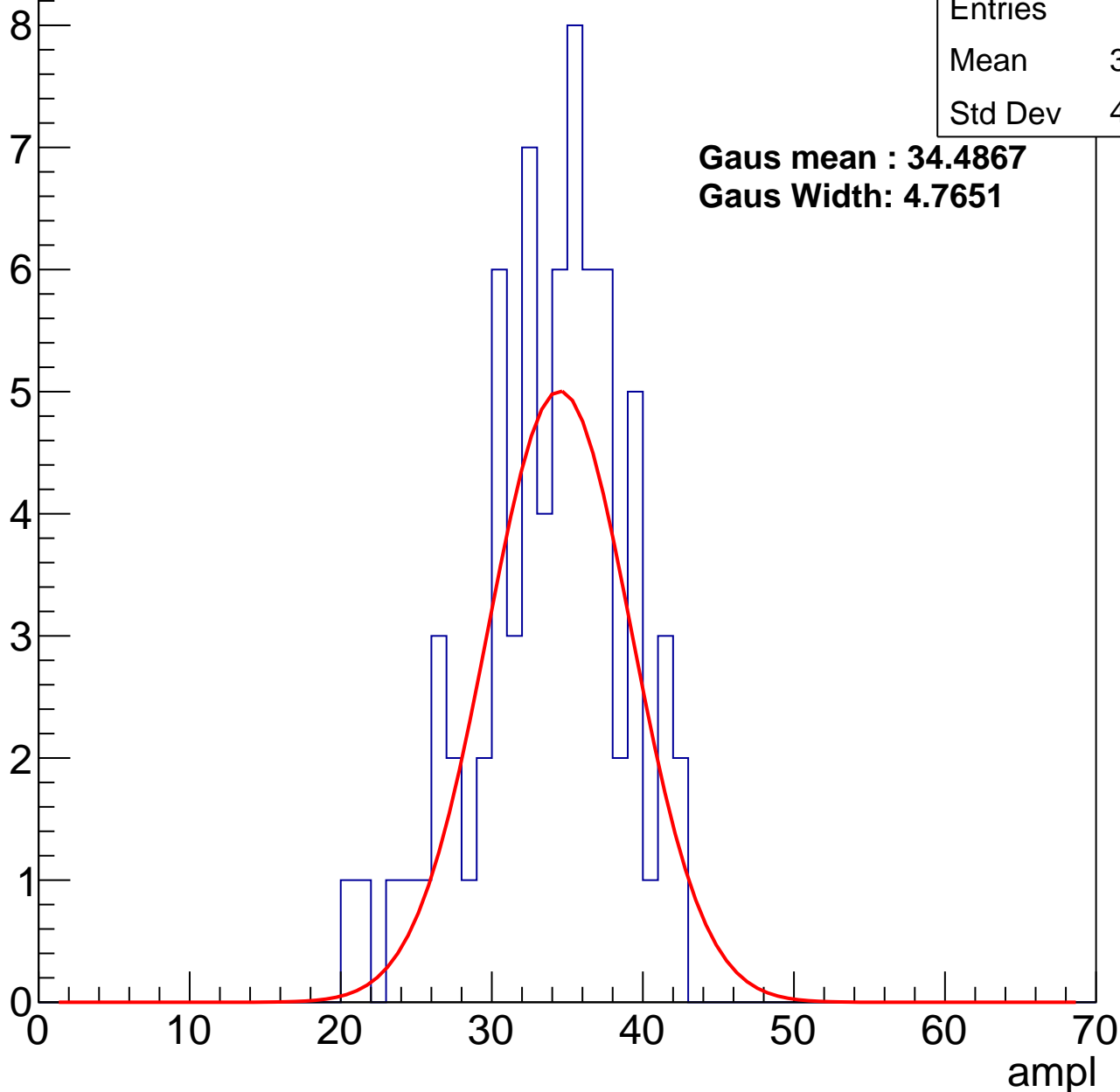
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	33.33
Std Dev	4.888

**Gaus mean : 34.4867**

**Gaus Width: 4.7651**



# B1L103S, U21-ch90, adc2

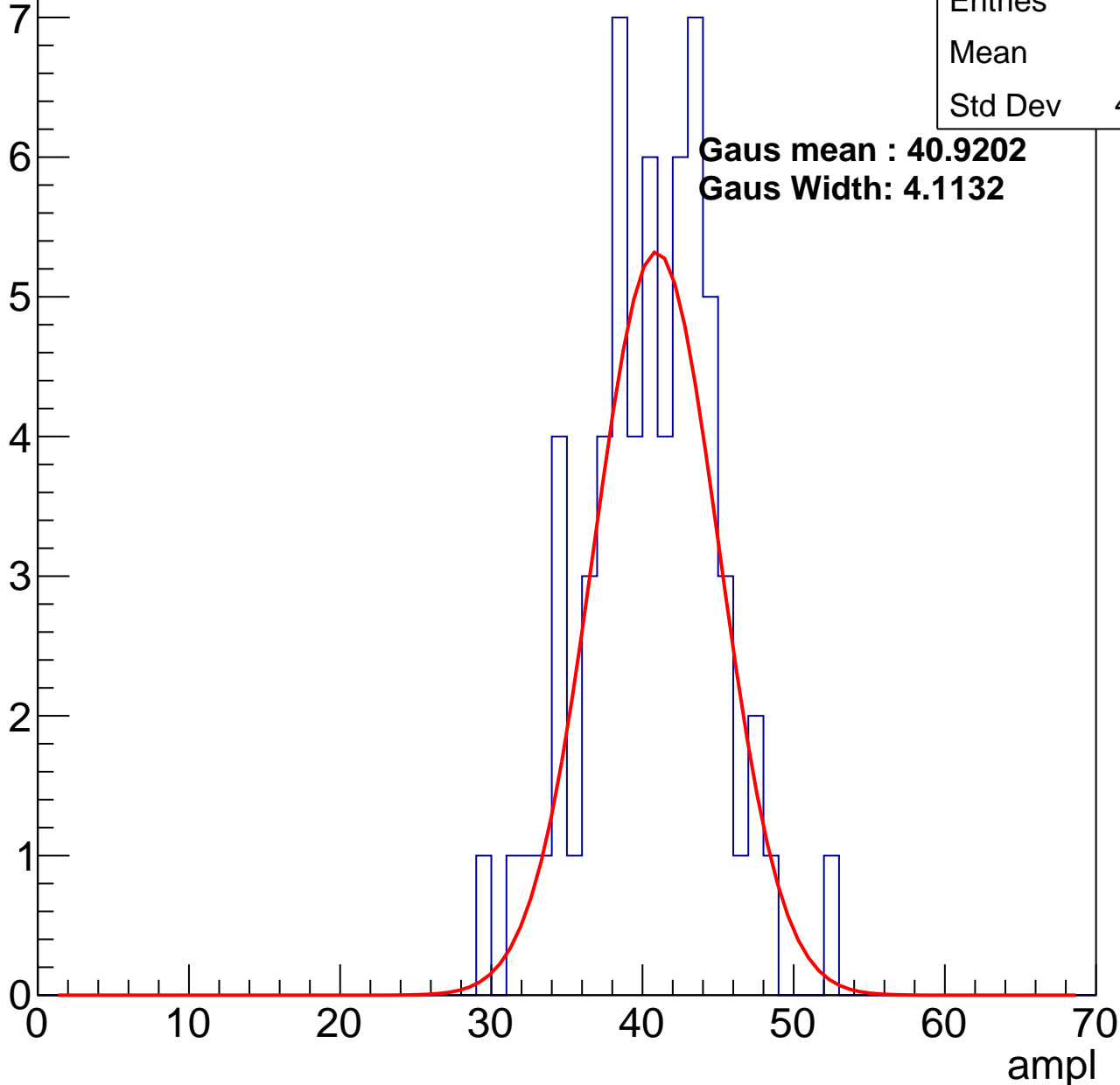
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	40.1
Std Dev	4.341

**Gaus mean : 40.9202**

**Gaus Width: 4.1132**

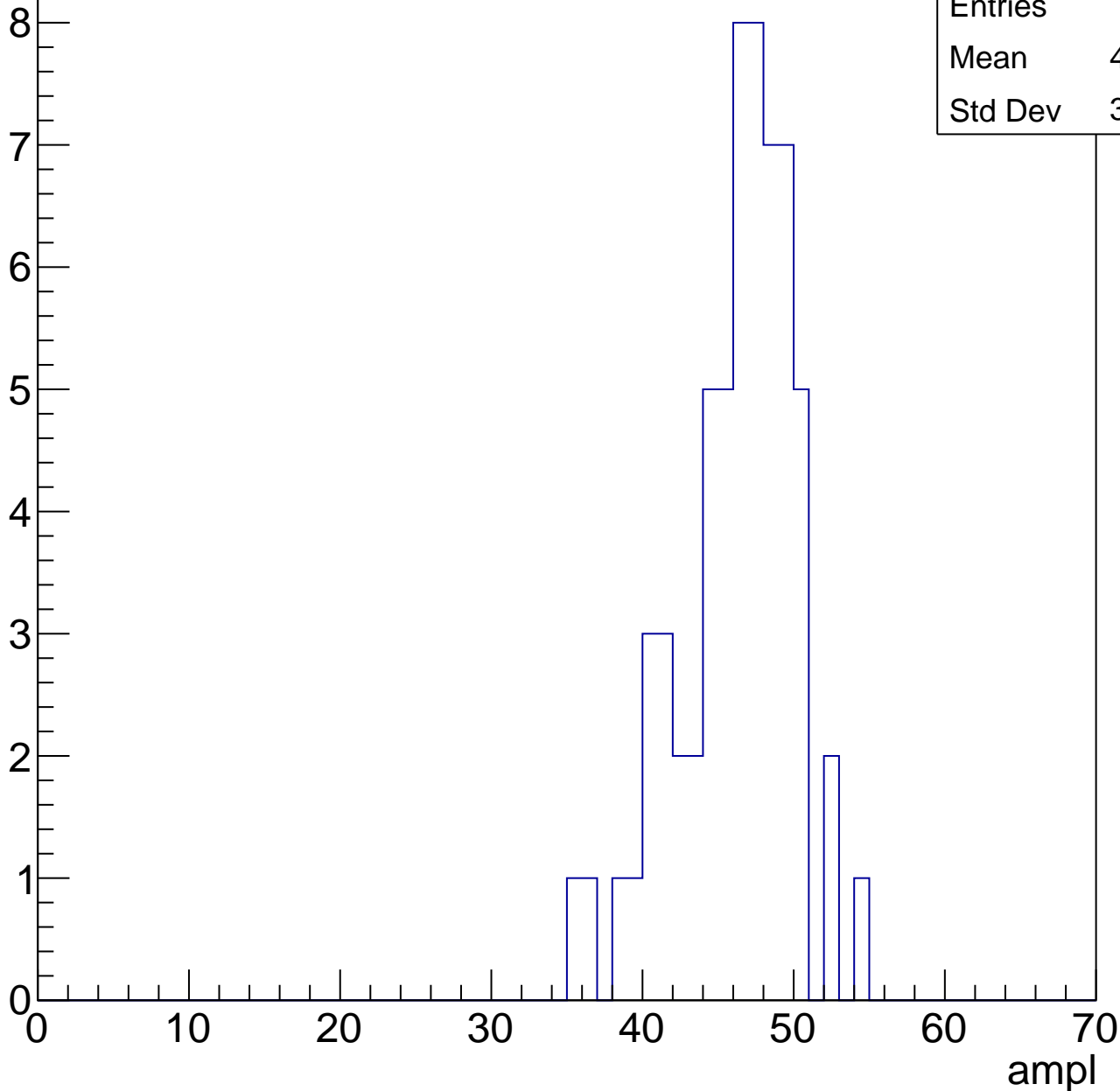


# B1L103S, U21-ch90, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	45.76
Std Dev	3.817



# B1L103S, U21-ch90, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	57
Mean	52.51
Std Dev	3.628

Entry

10

8

6

4

2

0

0

10

20

30

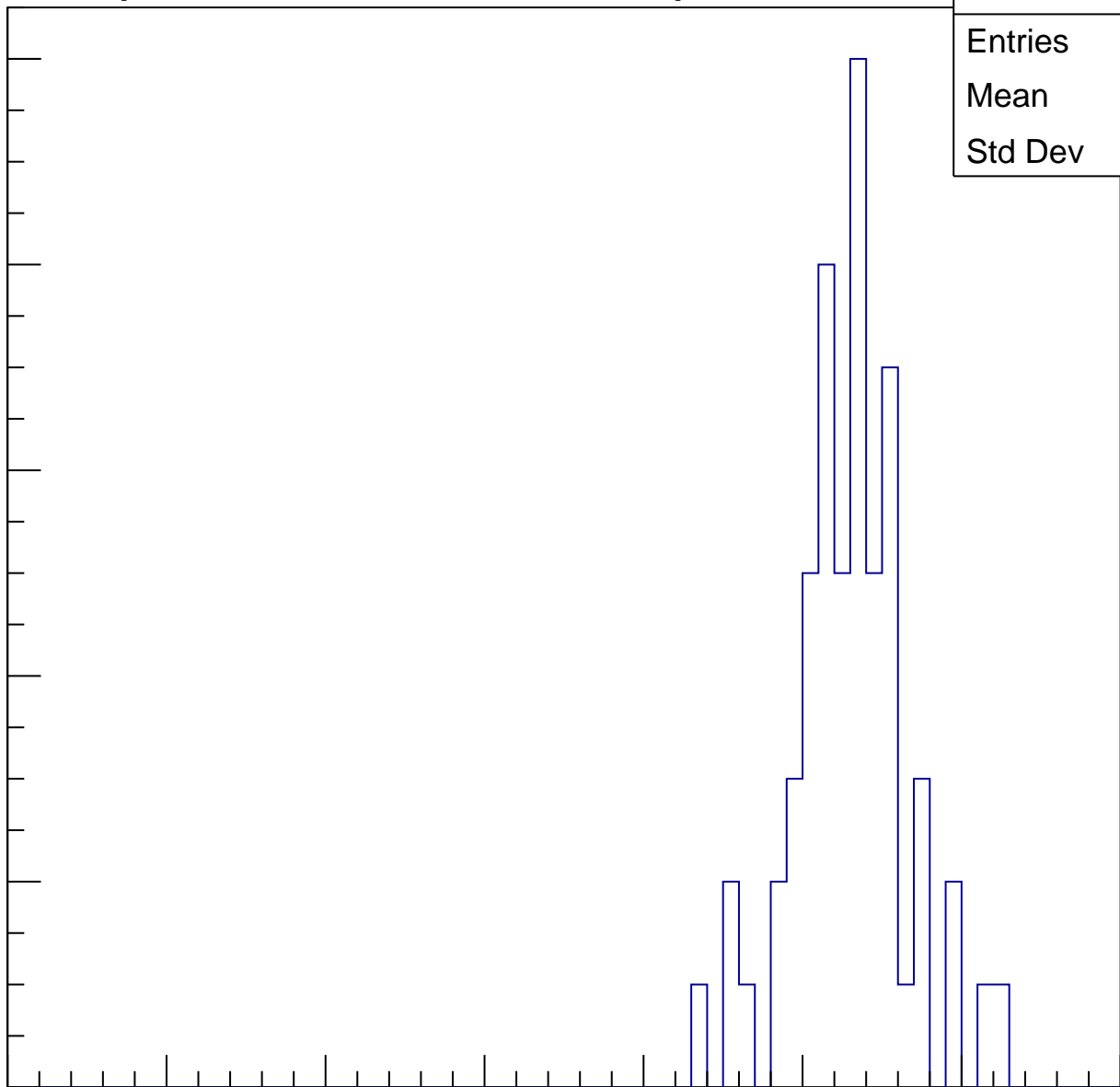
40

50

60

70

ampl

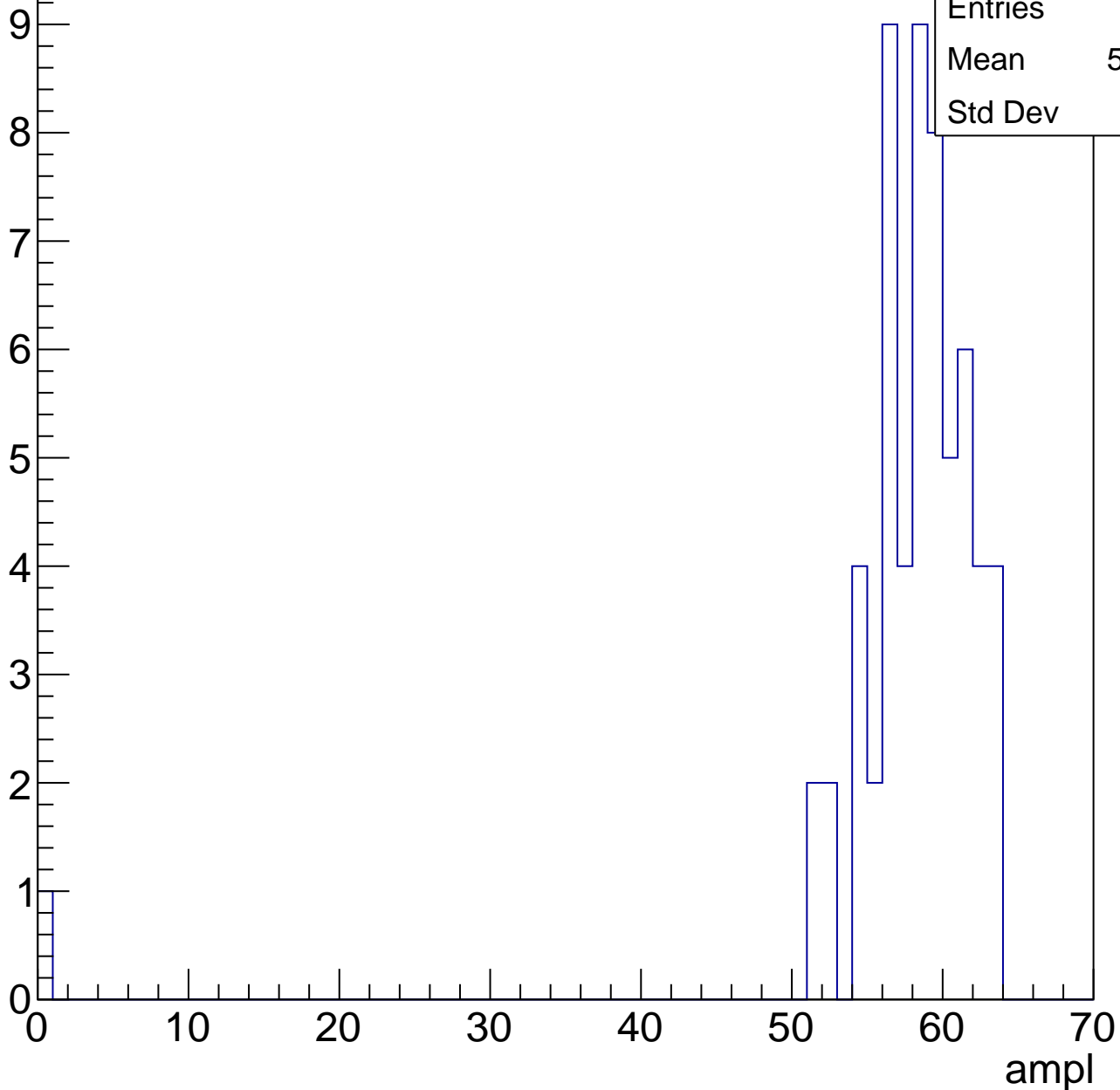


# B1L103S, U21-ch90, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	57.07
Std Dev	8.01

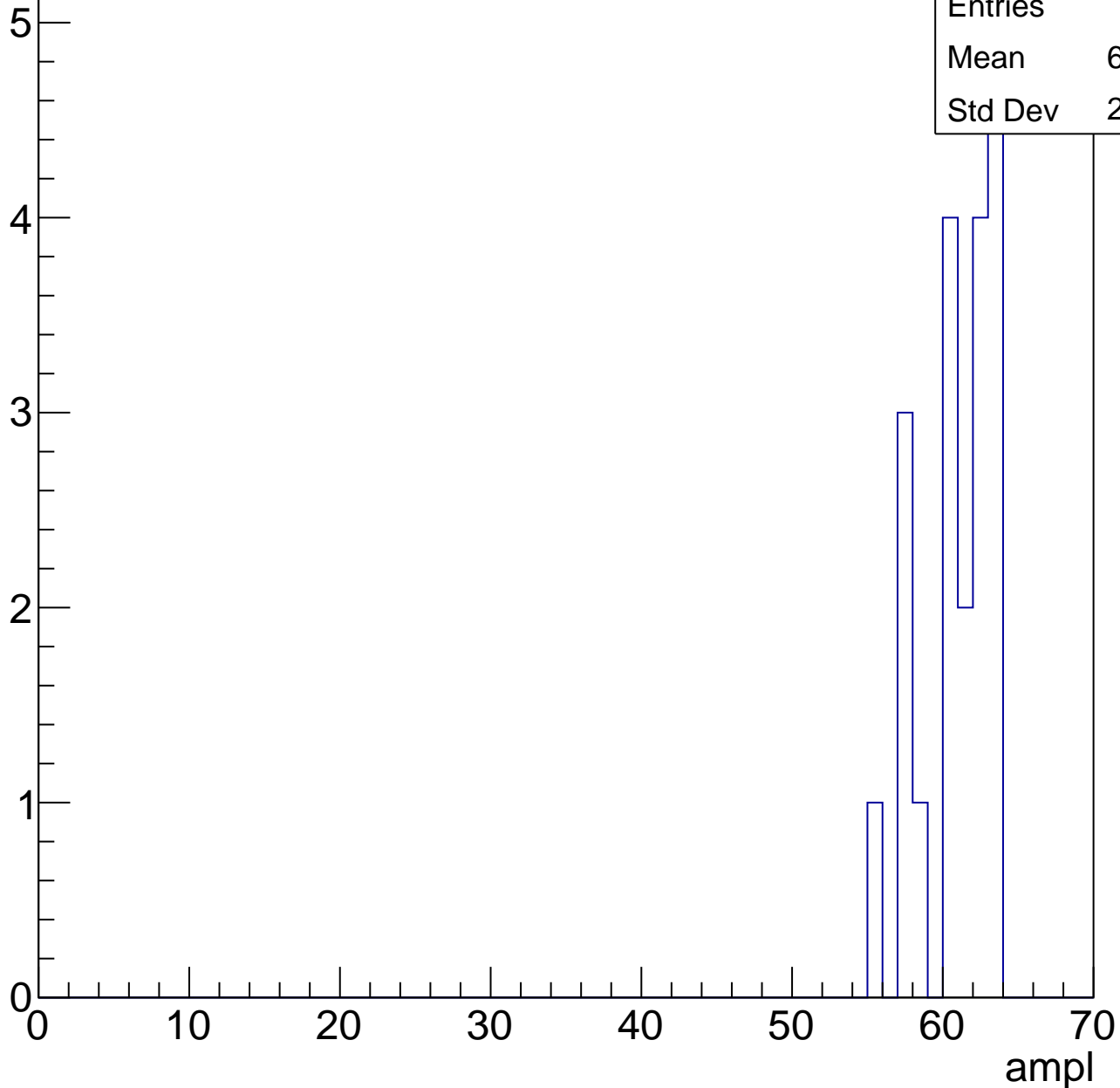


# B1L103S, U21-ch90, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	20
Mean	60.45
Std Dev	2.397

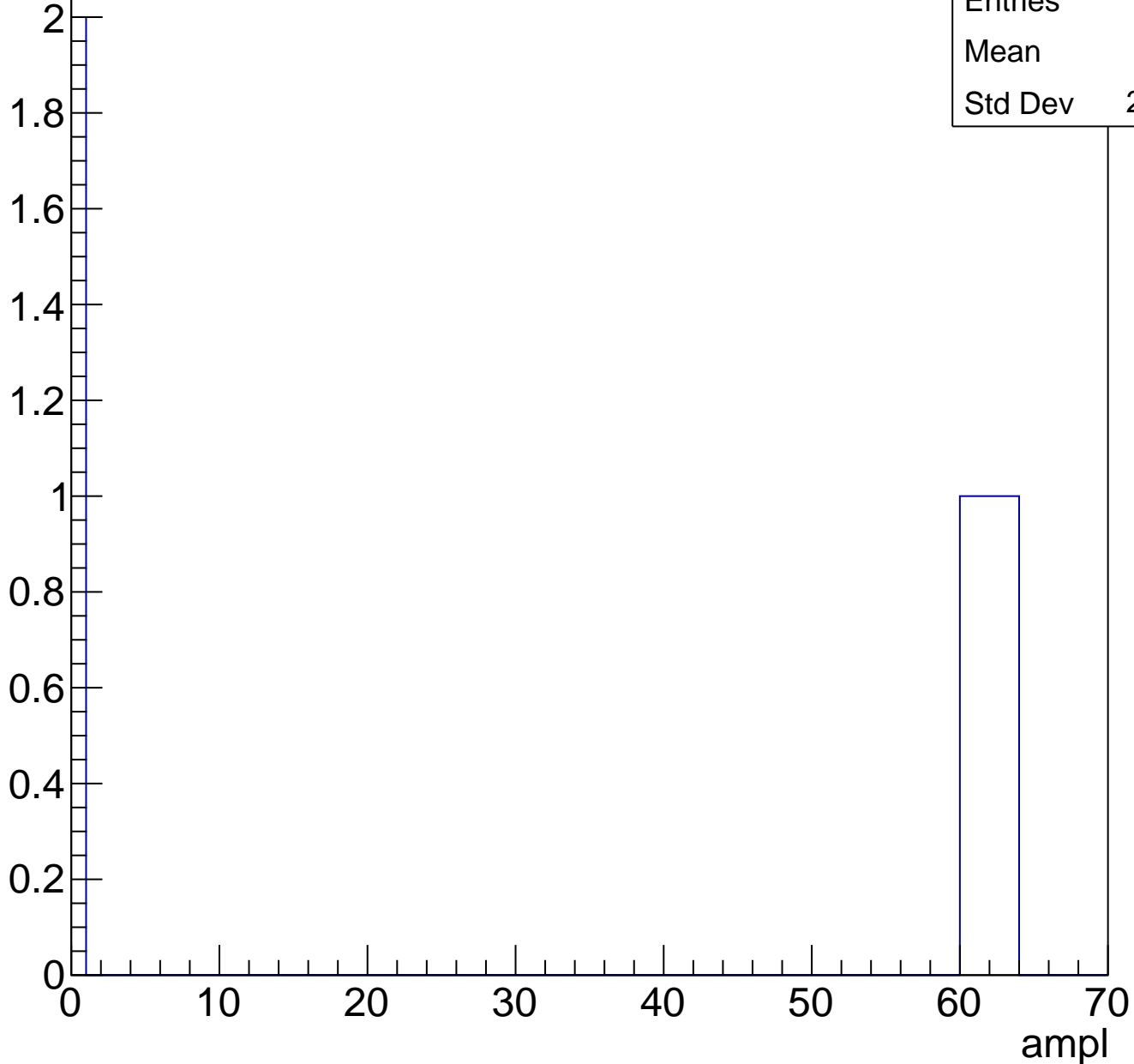




# B1L103S, U21-ch90, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U21-ch91, adc0

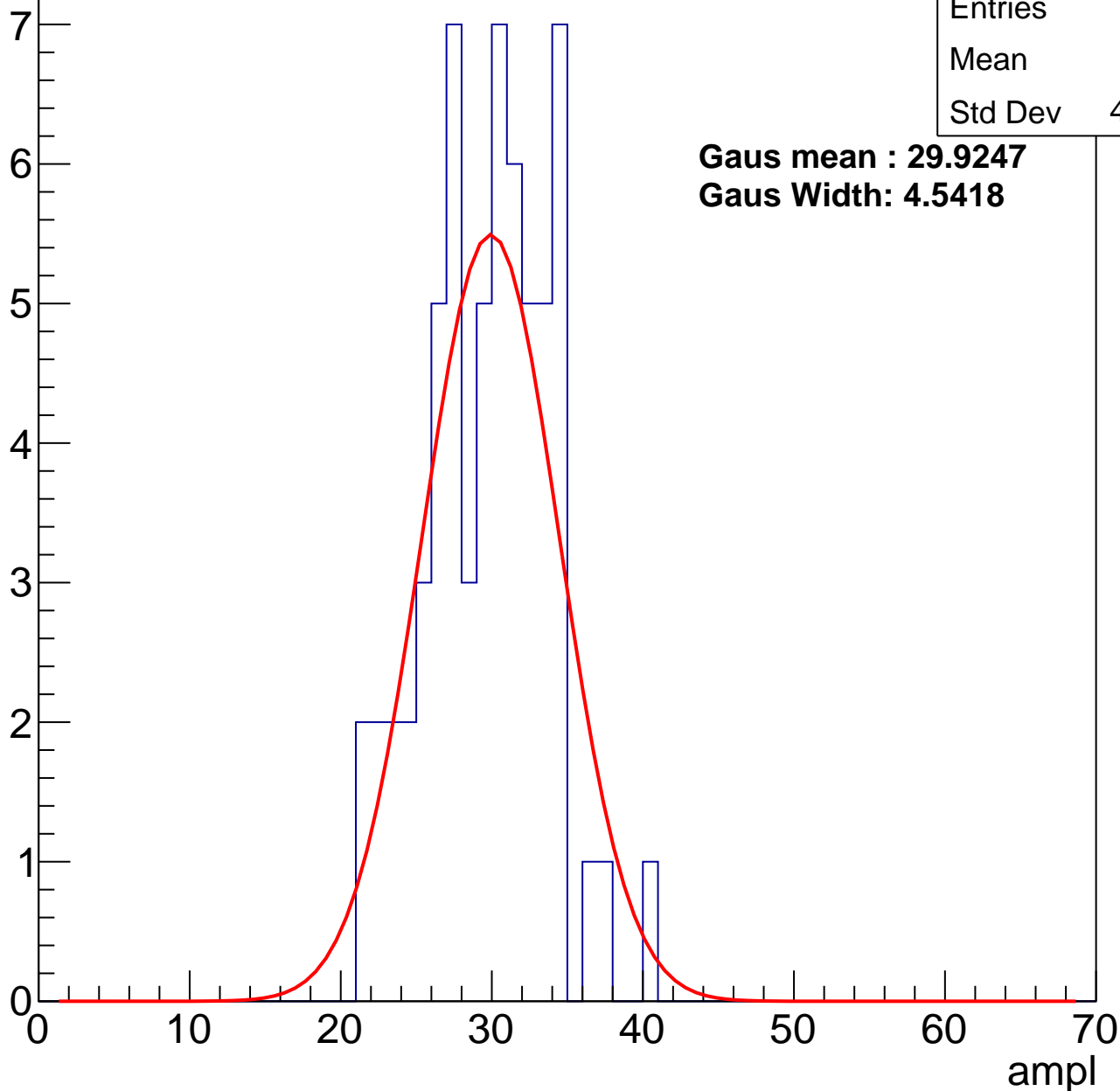
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	29.3
Std Dev	4.014

**Gaus mean : 29.9247**

**Gaus Width: 4.5418**



# B1L103S, U21-ch91, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	77
Mean	36.26
Std Dev	4.244

**Gaus mean : 36.4376**

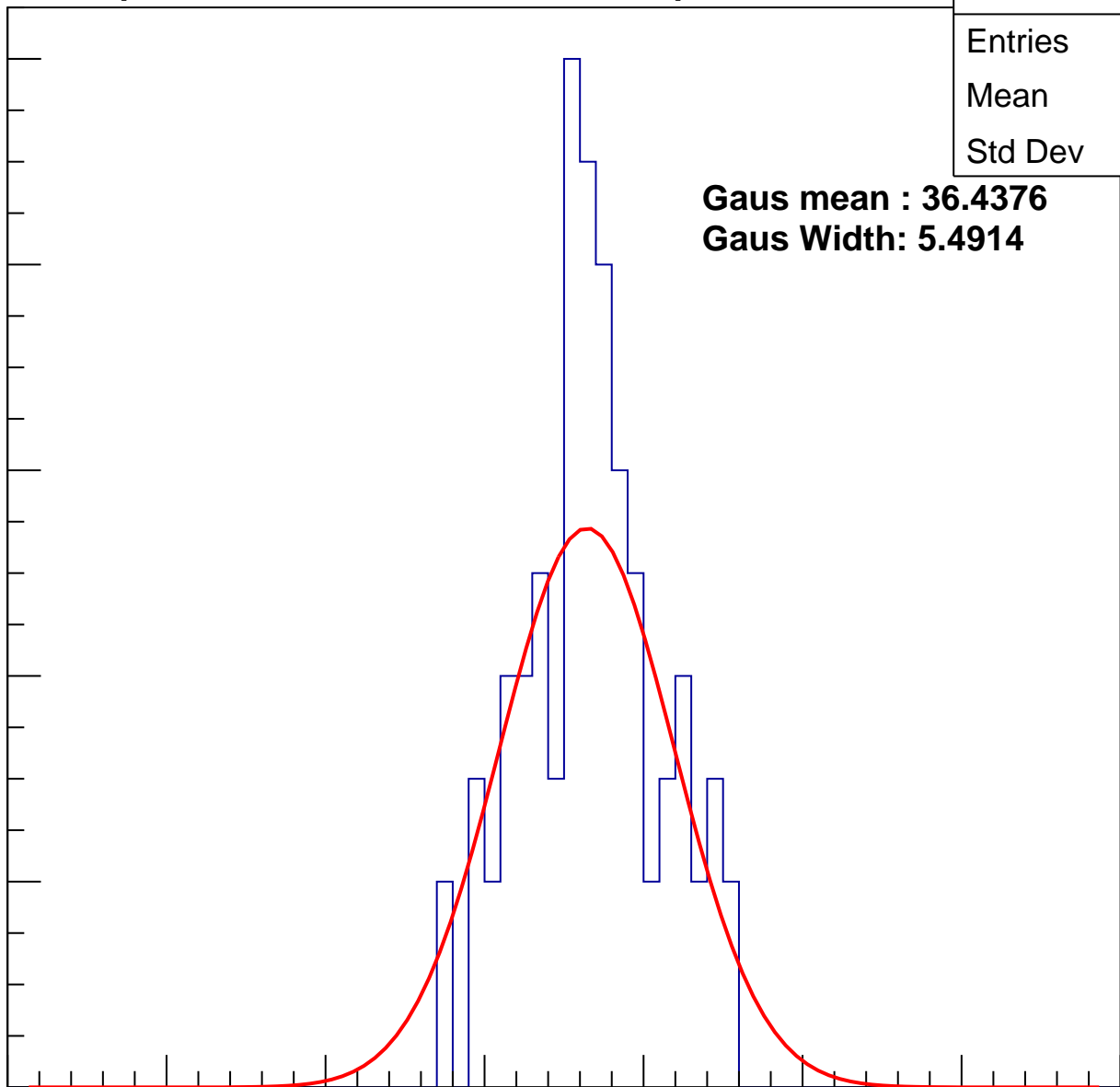
**Gaus Width: 5.4914**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U21-ch91, adc2

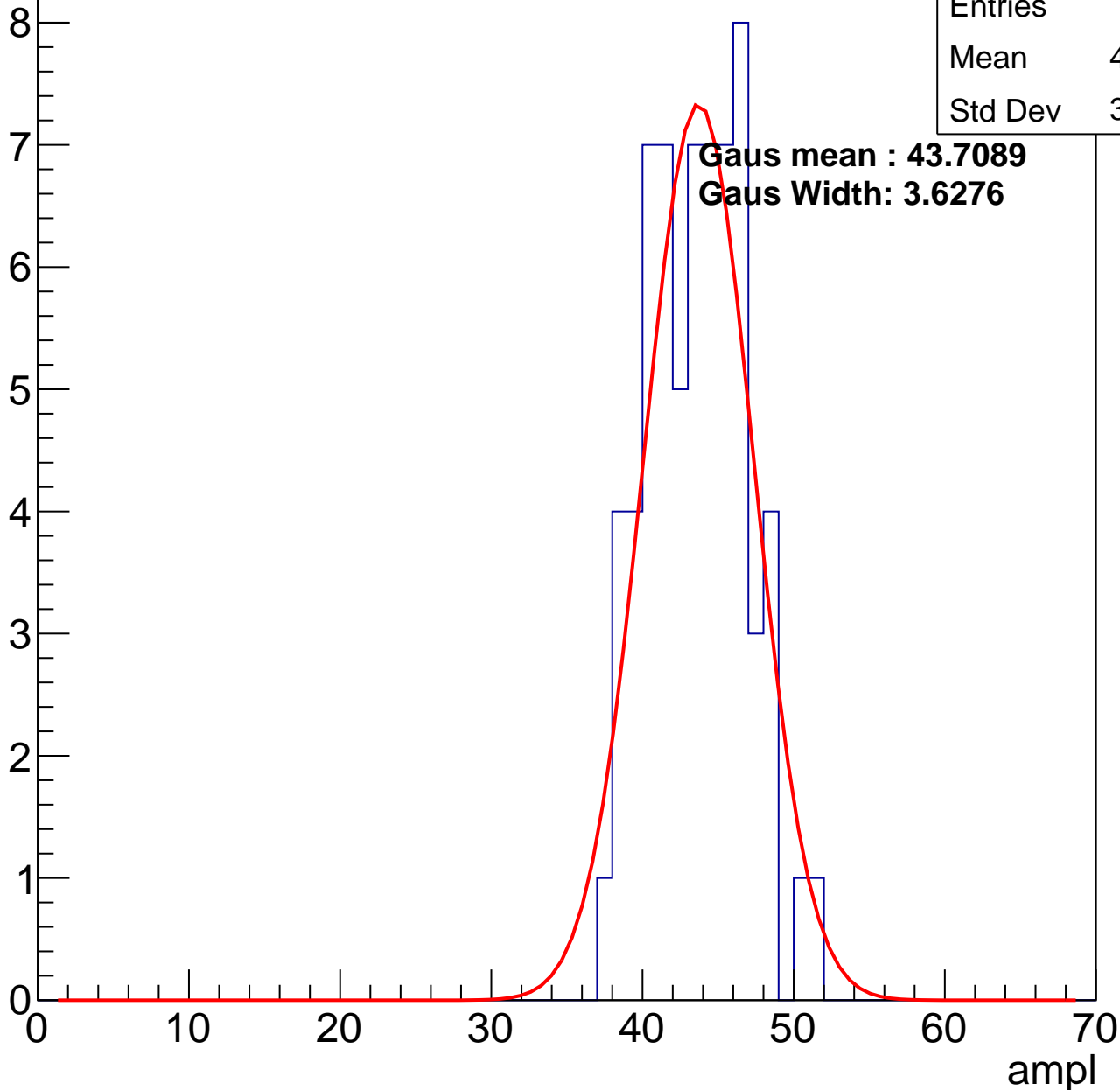
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	43.15
Std Dev	3.168

**Gaus mean : 43.7089**

**Gaus Width: 3.6276**

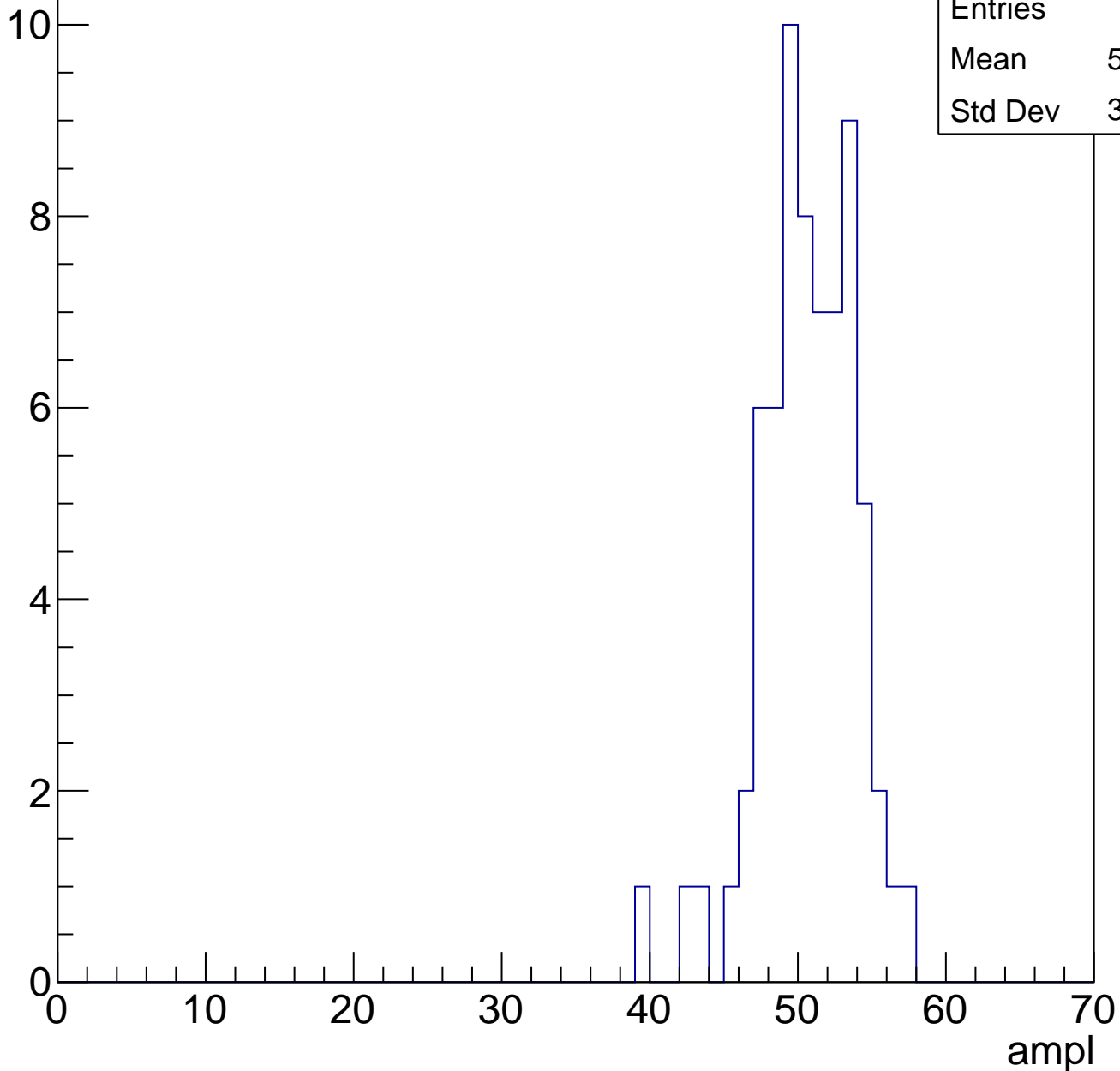


# B1L103S, U21-ch91, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	68
Mean	50.18
Std Dev	3.226

Entry

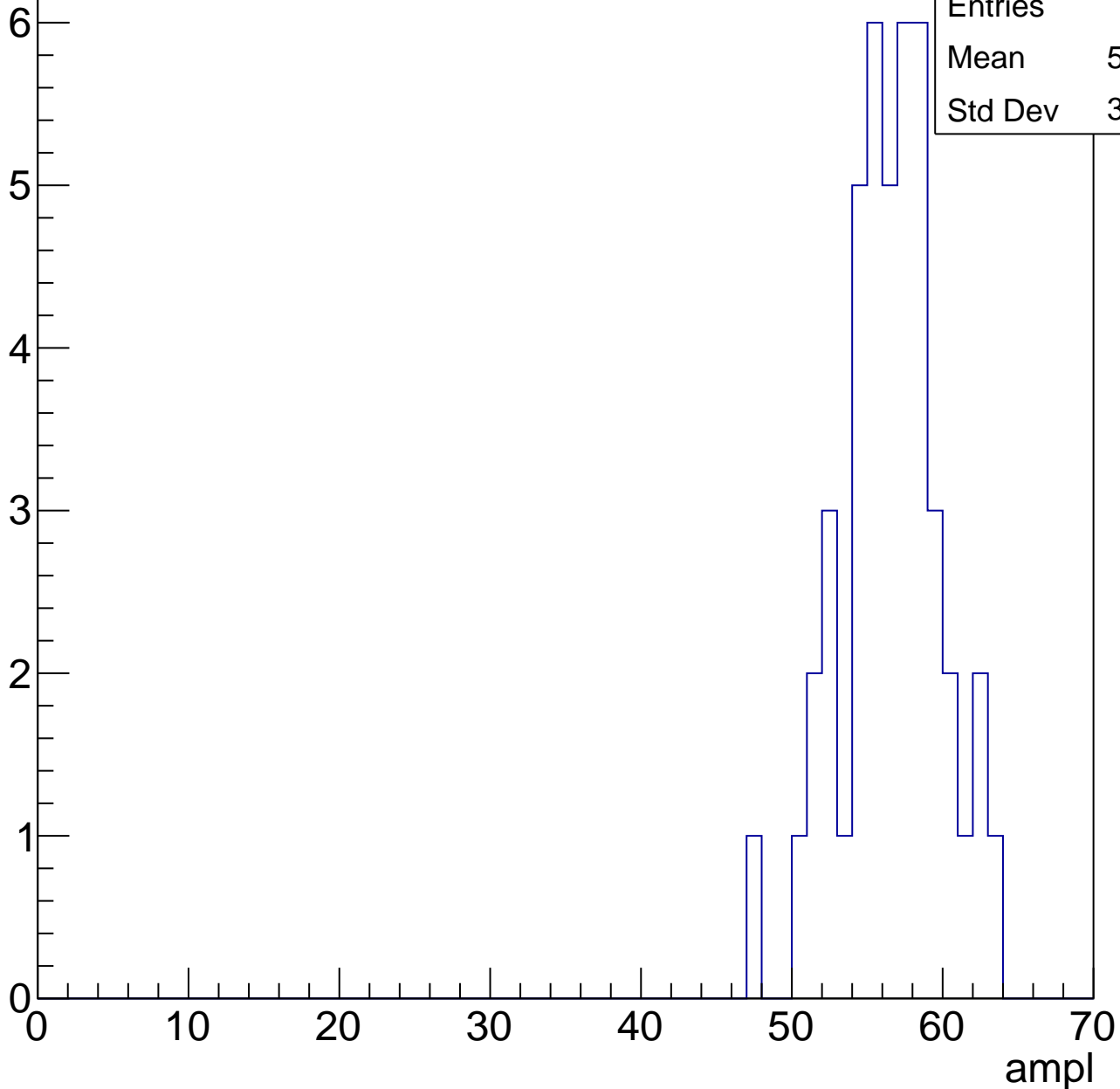


# B1L103S, U21-ch91, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	45
Mean	56.07
Std Dev	3.282



# B1L103S, U21-ch91, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

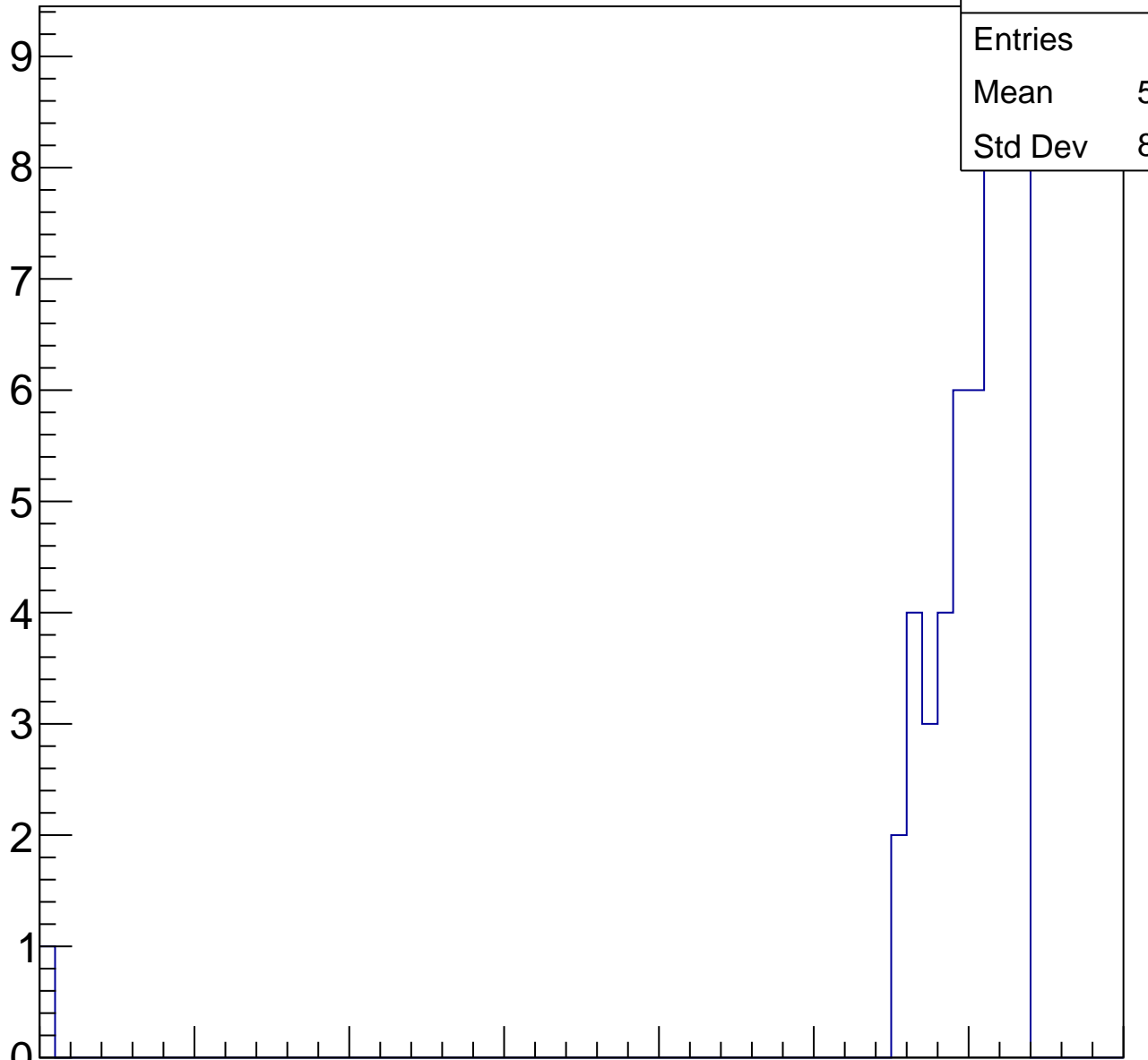
Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	51
Mean	58.82
Std Dev	8.638

ampl

0 10 20 30 40 50 60 70



# B1L103S, U21-ch91, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

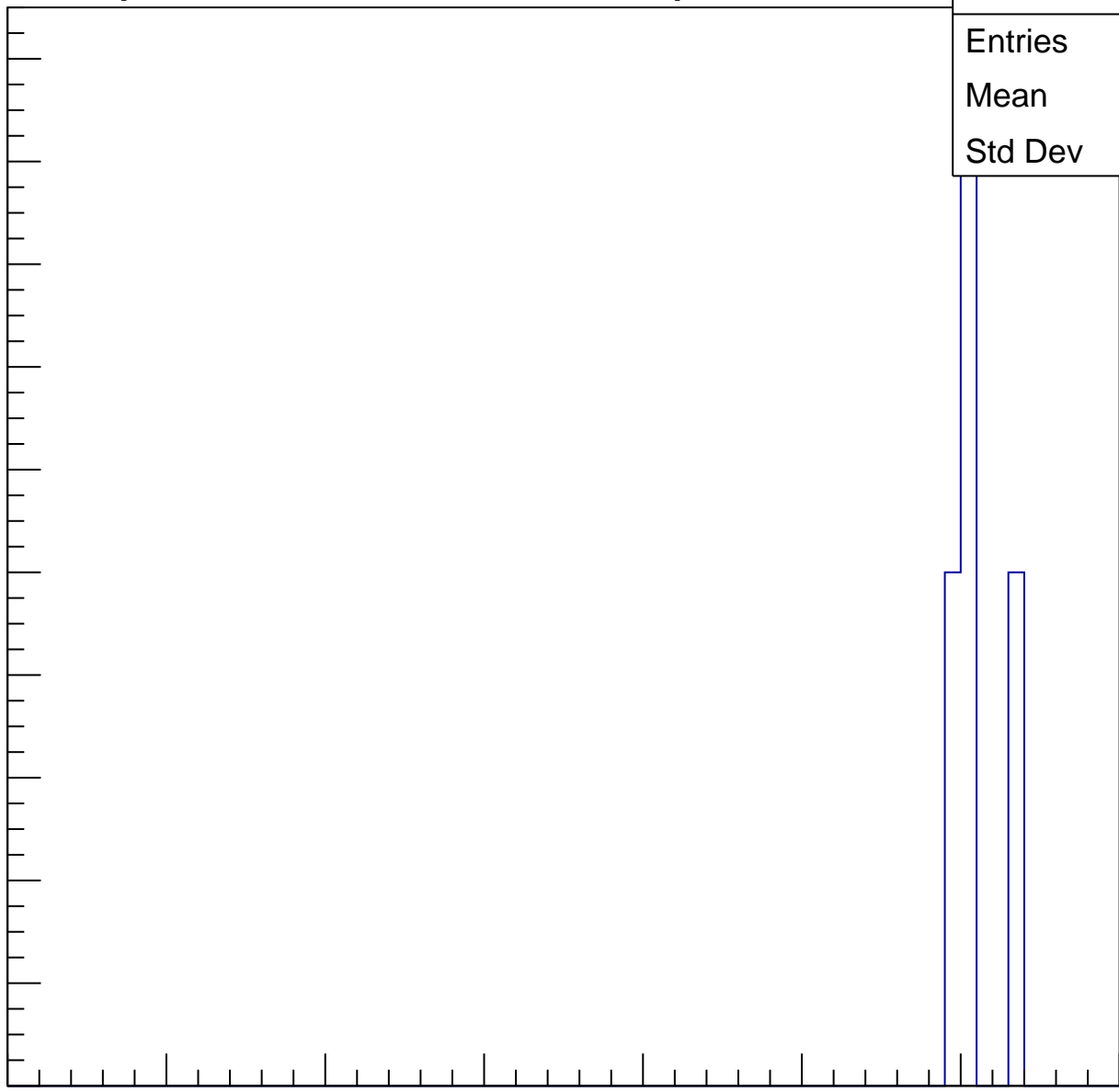
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	60.5
Std Dev	1.5

ampl

0 10 20 30 40 50 60 70





# B1L103S, U21-ch91, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U21-ch92, adc0

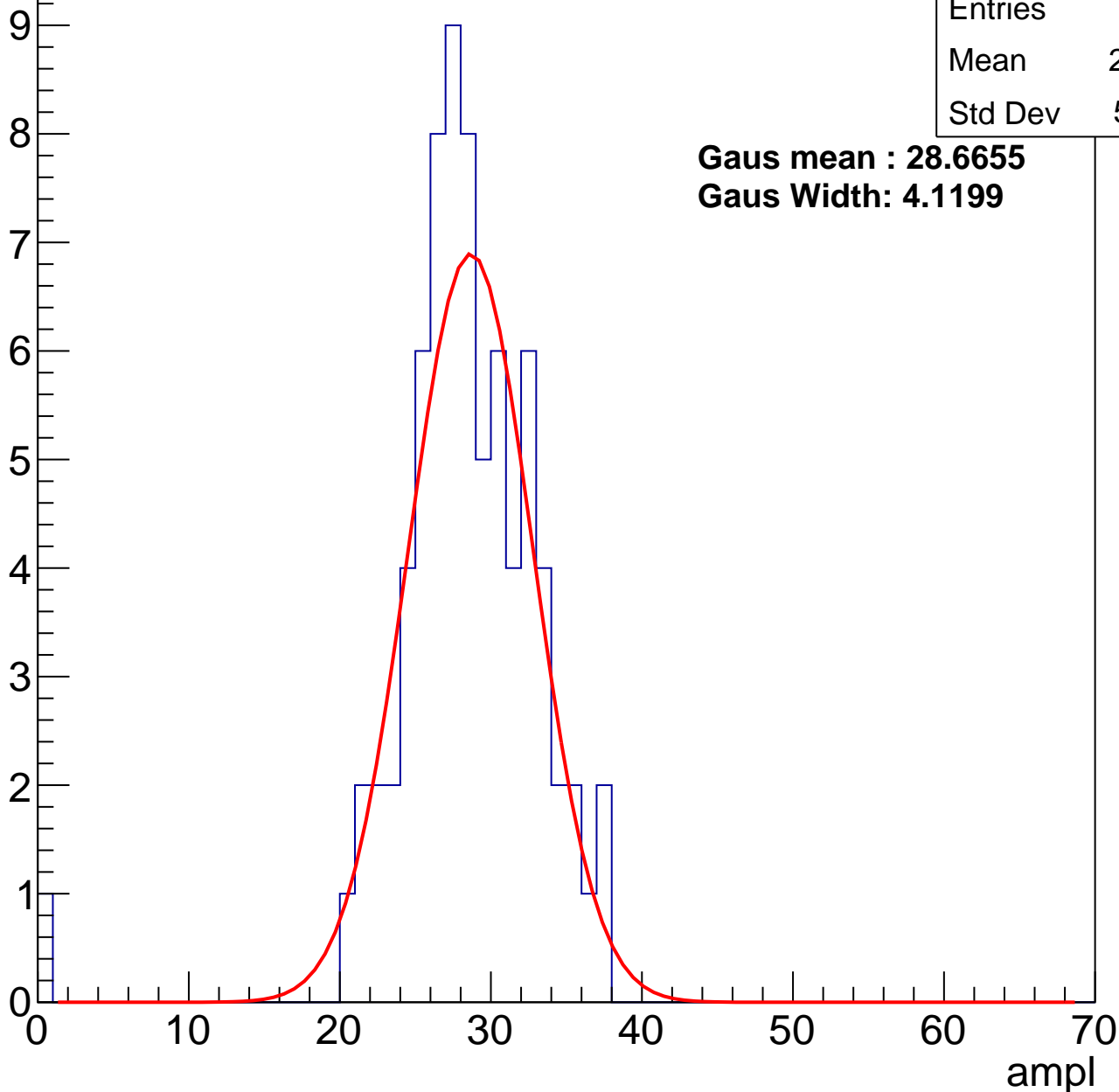
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	27.92
Std Dev	5.011

**Gaus mean : 28.6655**

**Gaus Width: 4.1199**



# B1L103S, U21-ch92, adc1

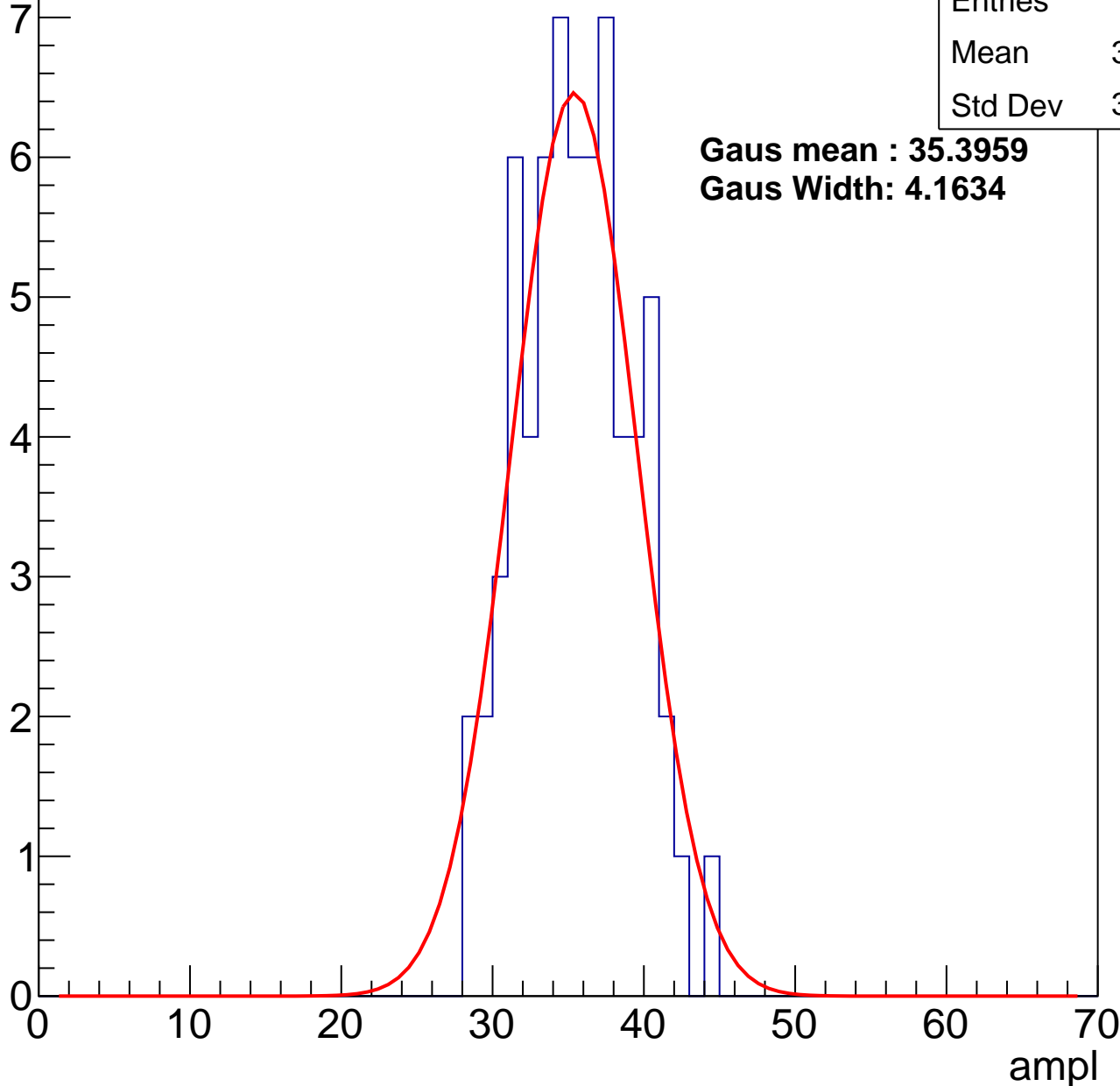
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	35.08
Std Dev	3.628

**Gaus mean : 35.3959**

**Gaus Width: 4.1634**



# B1L103S, U21-ch92, adc2

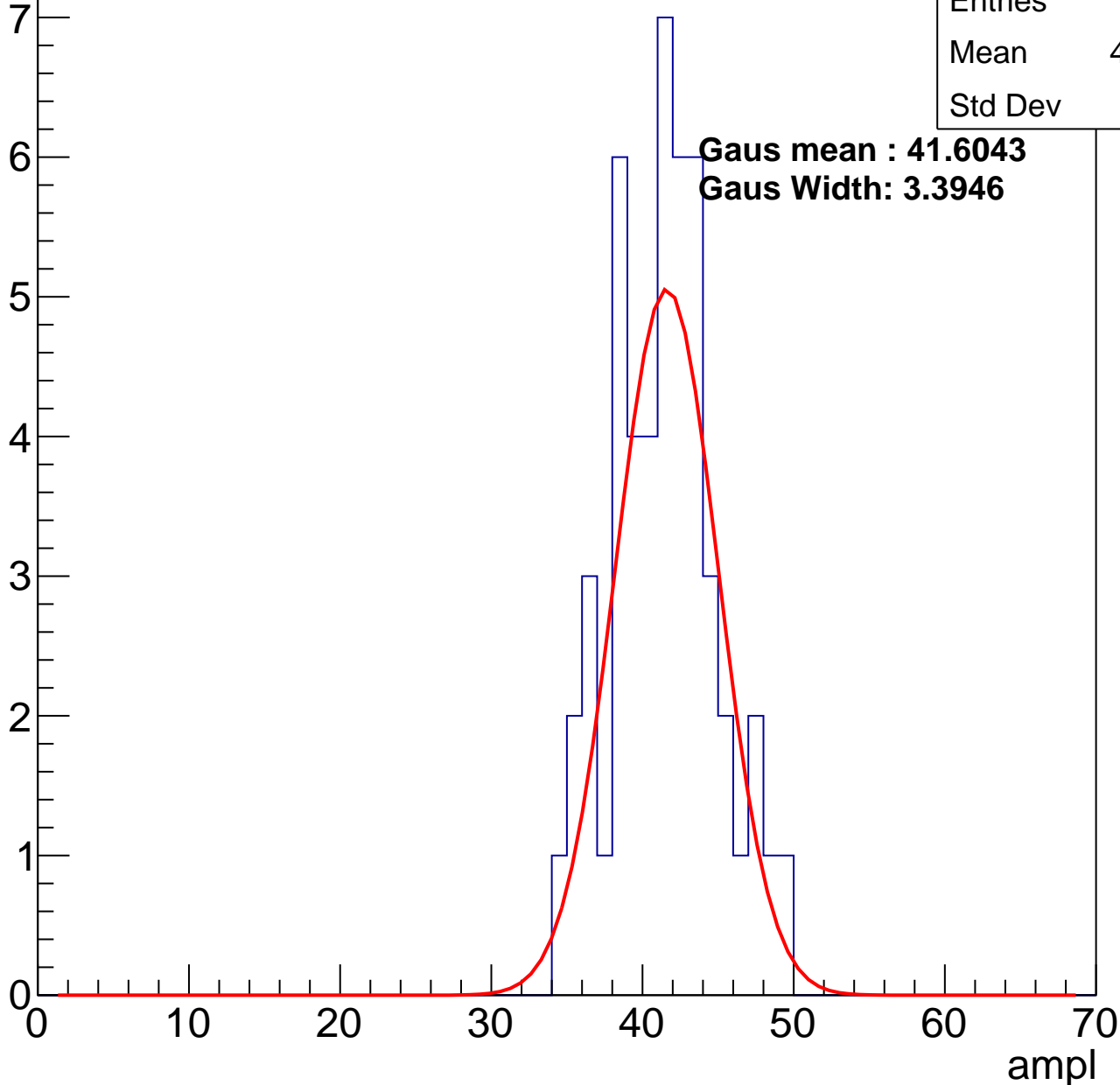
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	40.98
Std Dev	3.42

**Gaus mean : 41.6043**

**Gaus Width: 3.3946**

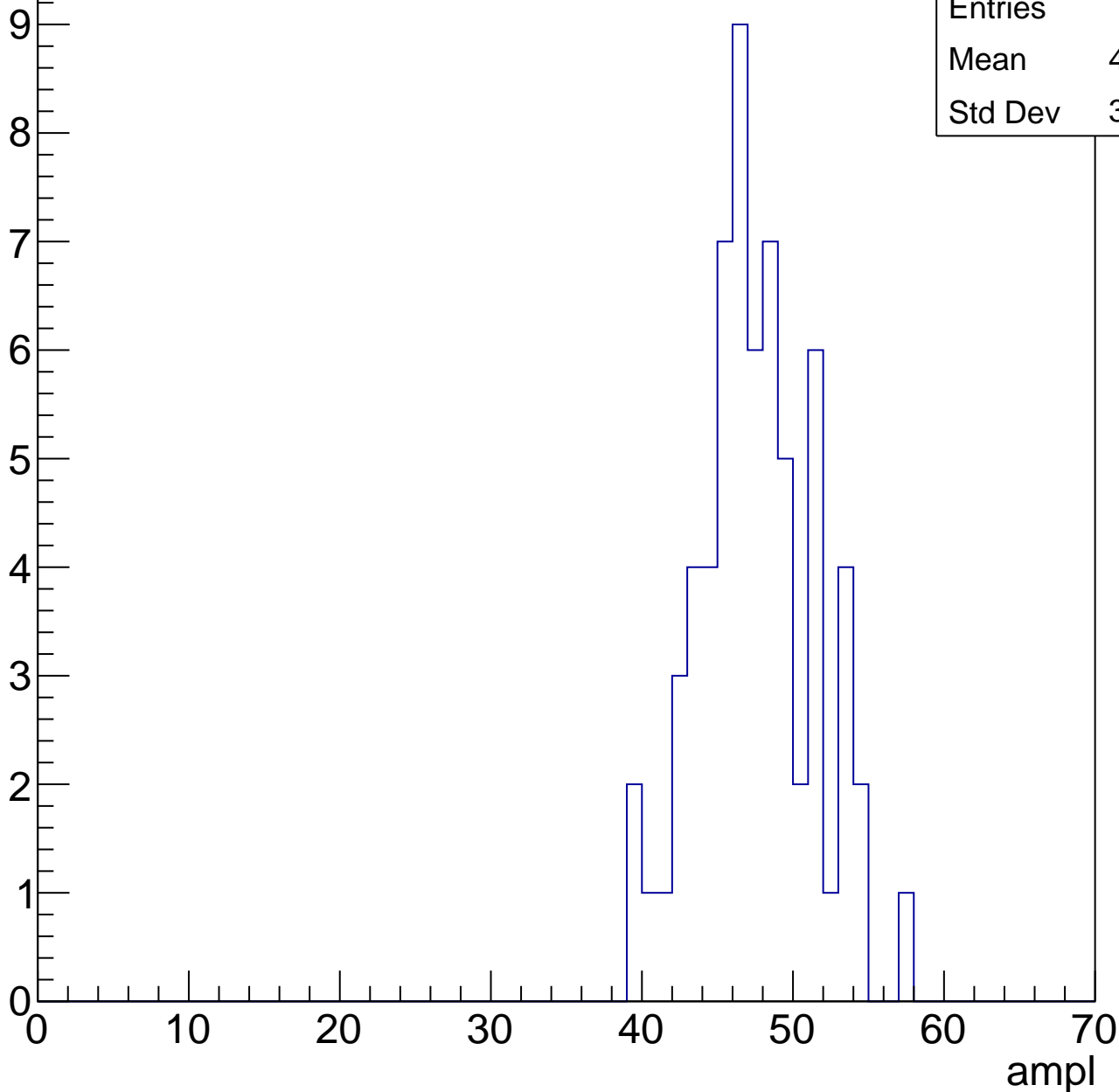


# B1L103S, U21-ch92, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	47.08
Std Dev	3.788

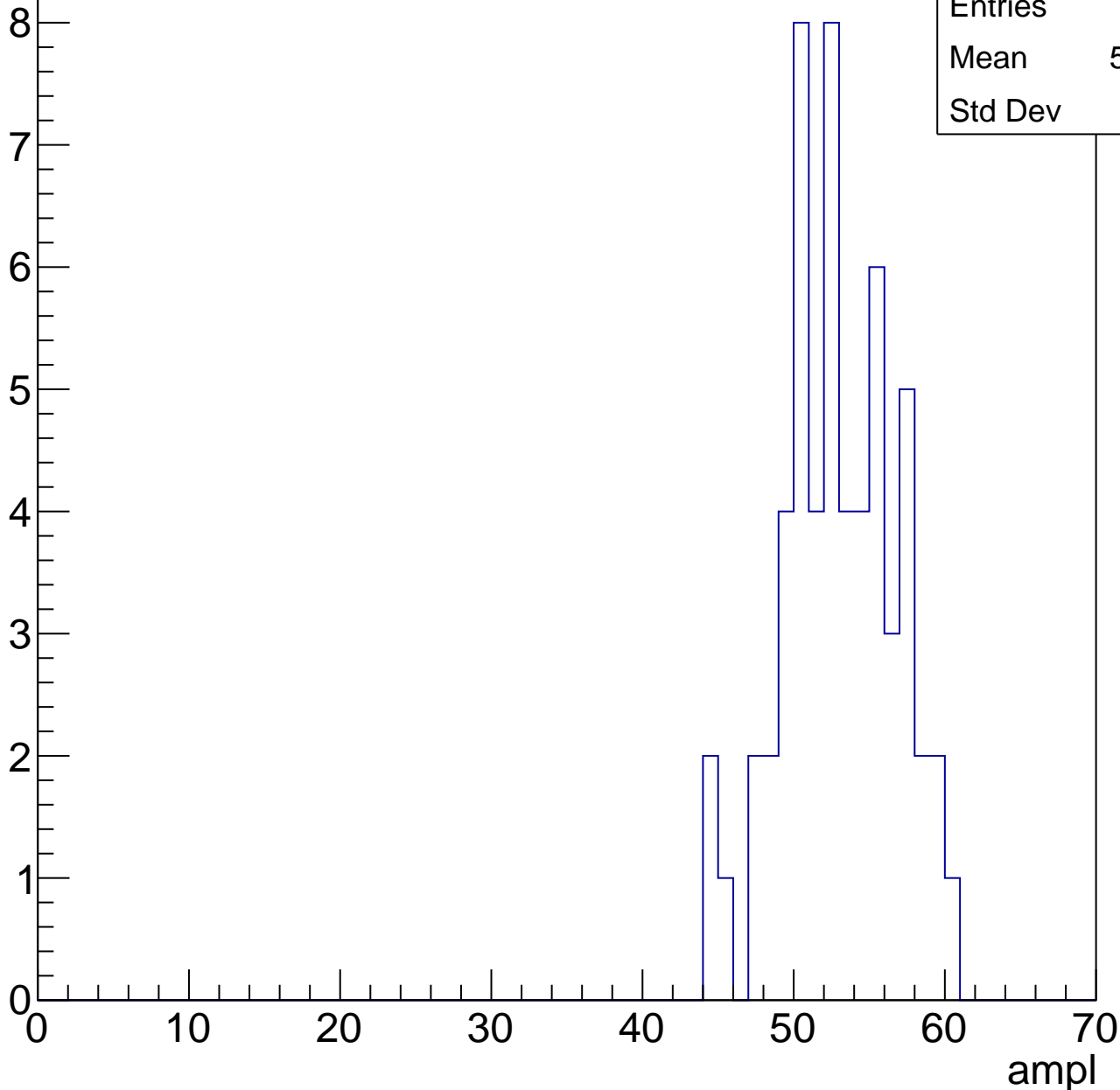


# B1L103S, U21-ch92, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

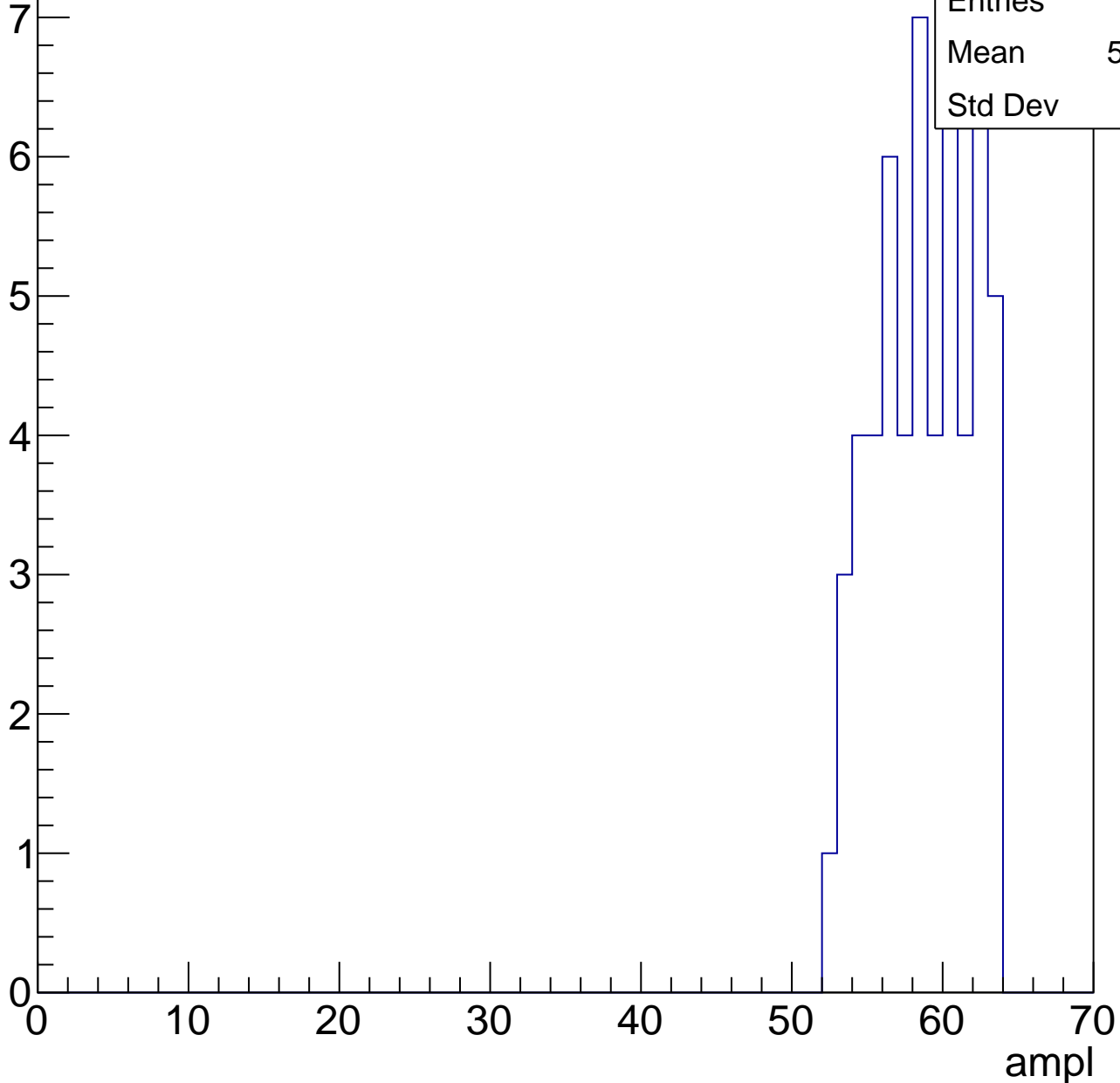
Entries	58
Mean	52.48
Std Dev	3.71



# B1L103S, U21-ch92, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



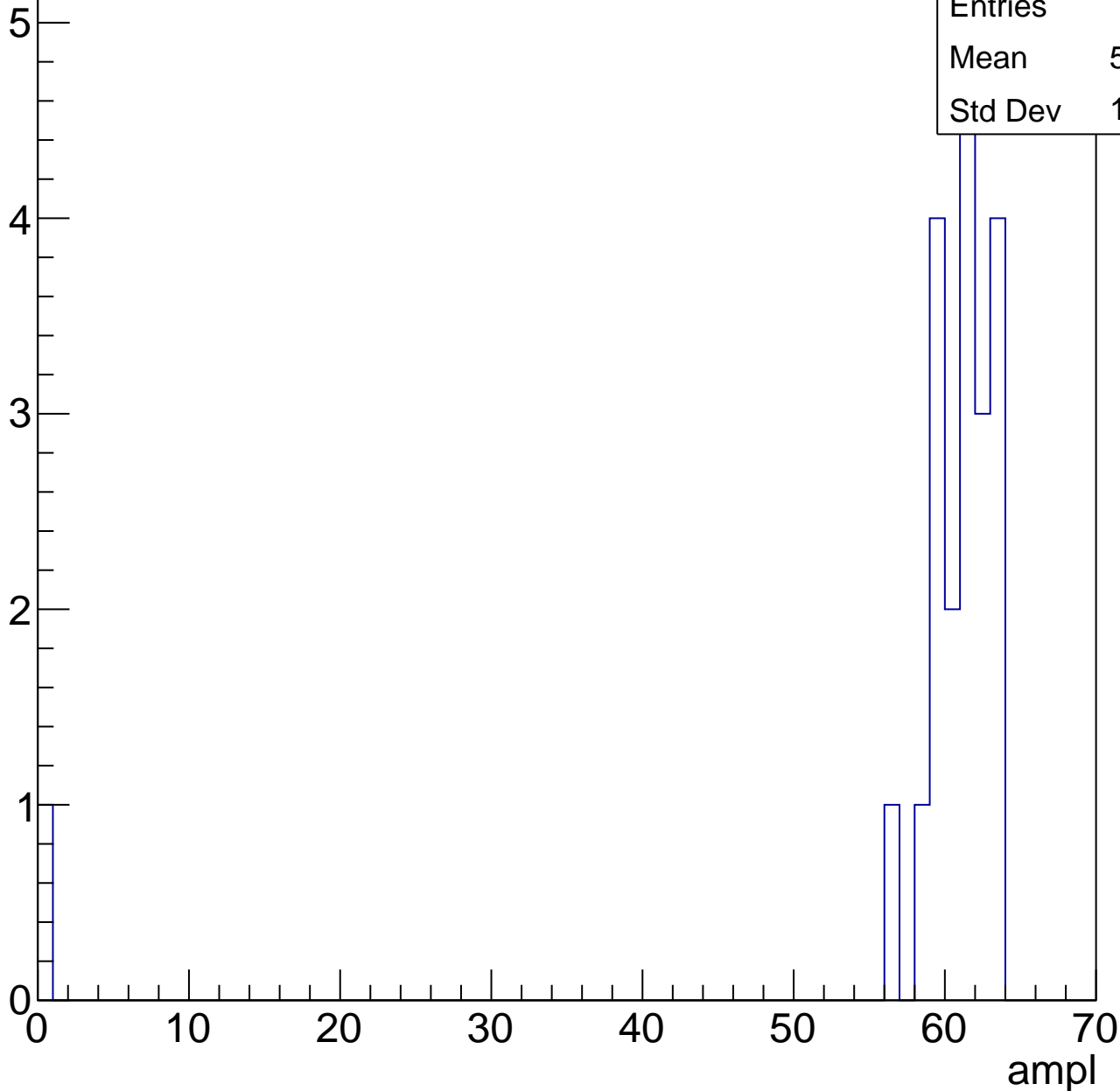
Entries	56
Mean	58.32
Std Dev	3.1

# B1L103S, U21-ch92, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	21
Mean	57.76
Std Dev	13.04

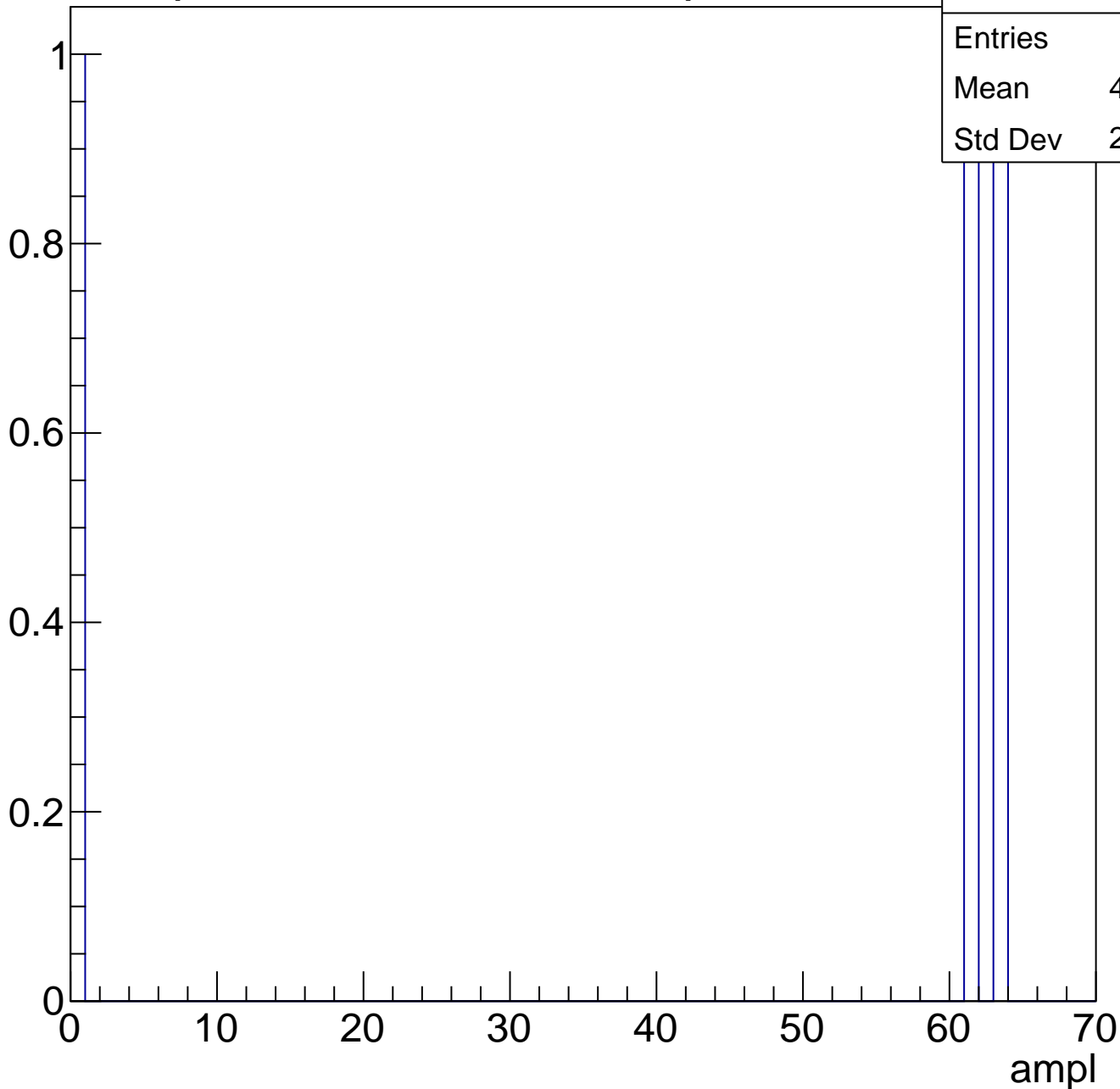




# B1L103S, U21-ch92, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U21-ch93, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	28.56
Std Dev	5.136

**Gaus mean : 28.8376**

**Gaus Width: 4.4208**

10

8

6

4

2

0

0

10

20

30

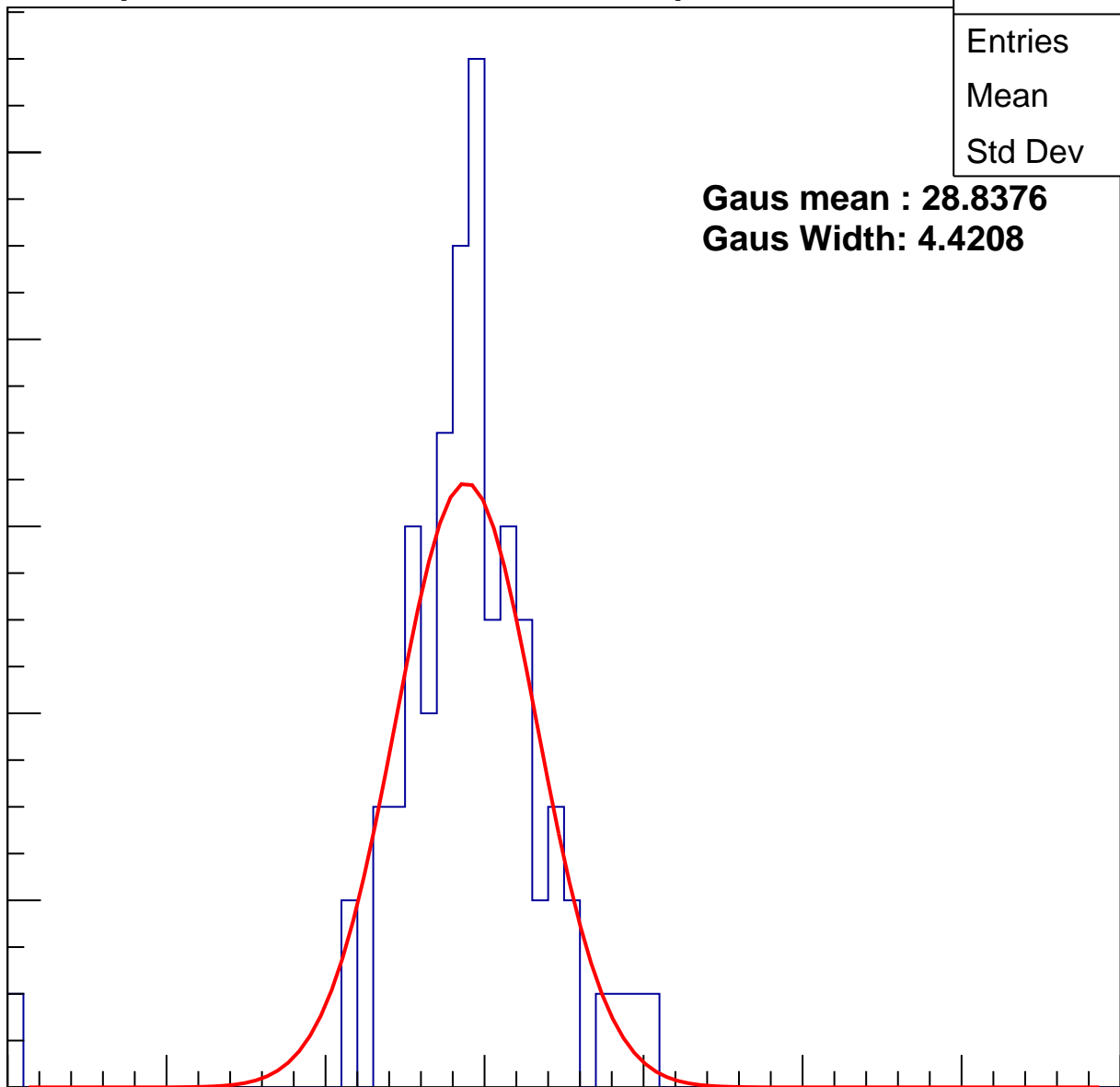
40

50

60

70

ampl



# B1L103S, U21-ch93, adc1

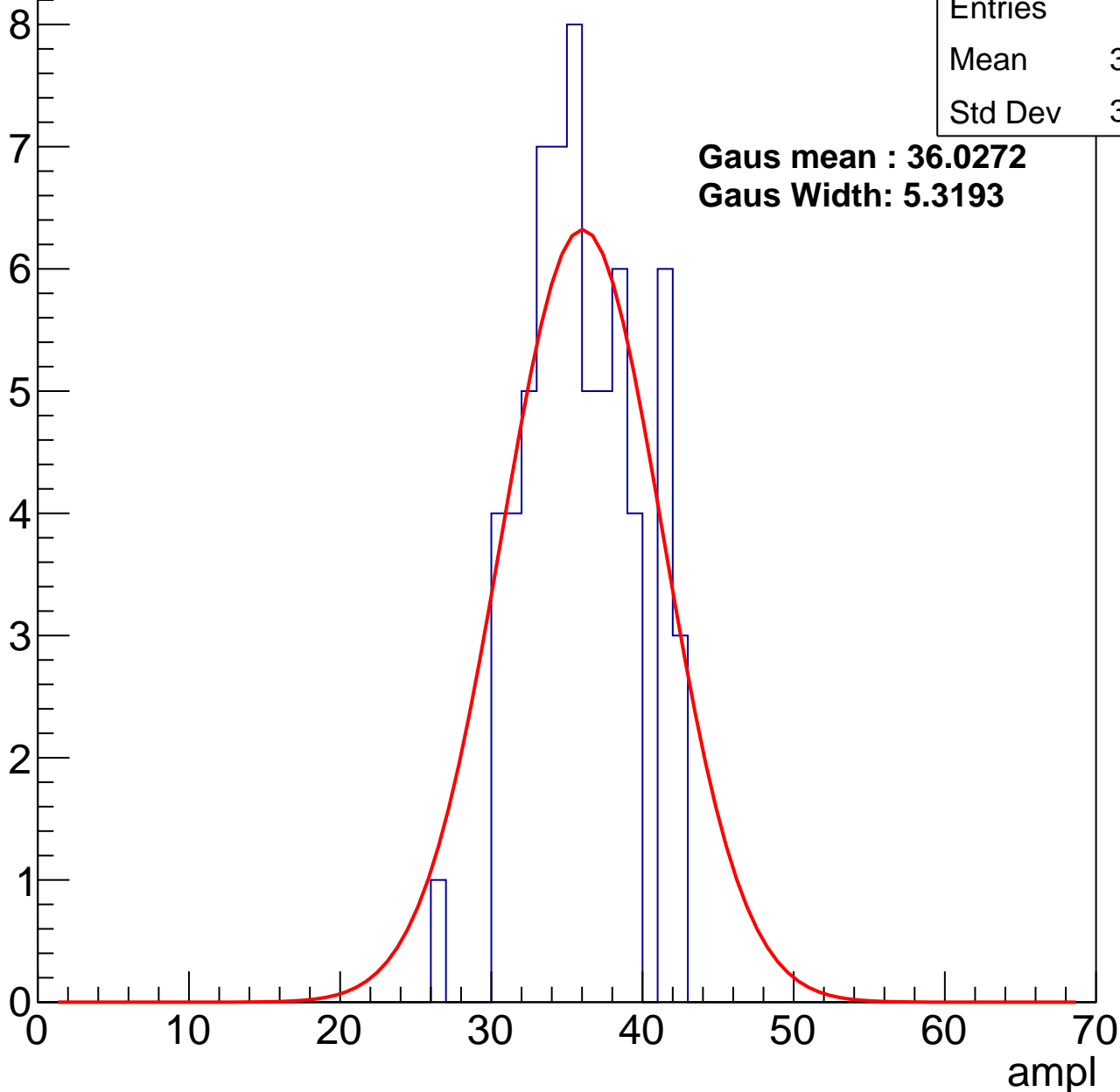
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	35.38
Std Dev	3.555

**Gaus mean : 36.0272**

**Gaus Width: 5.3193**



# B1L103S, U21-ch93, adc2

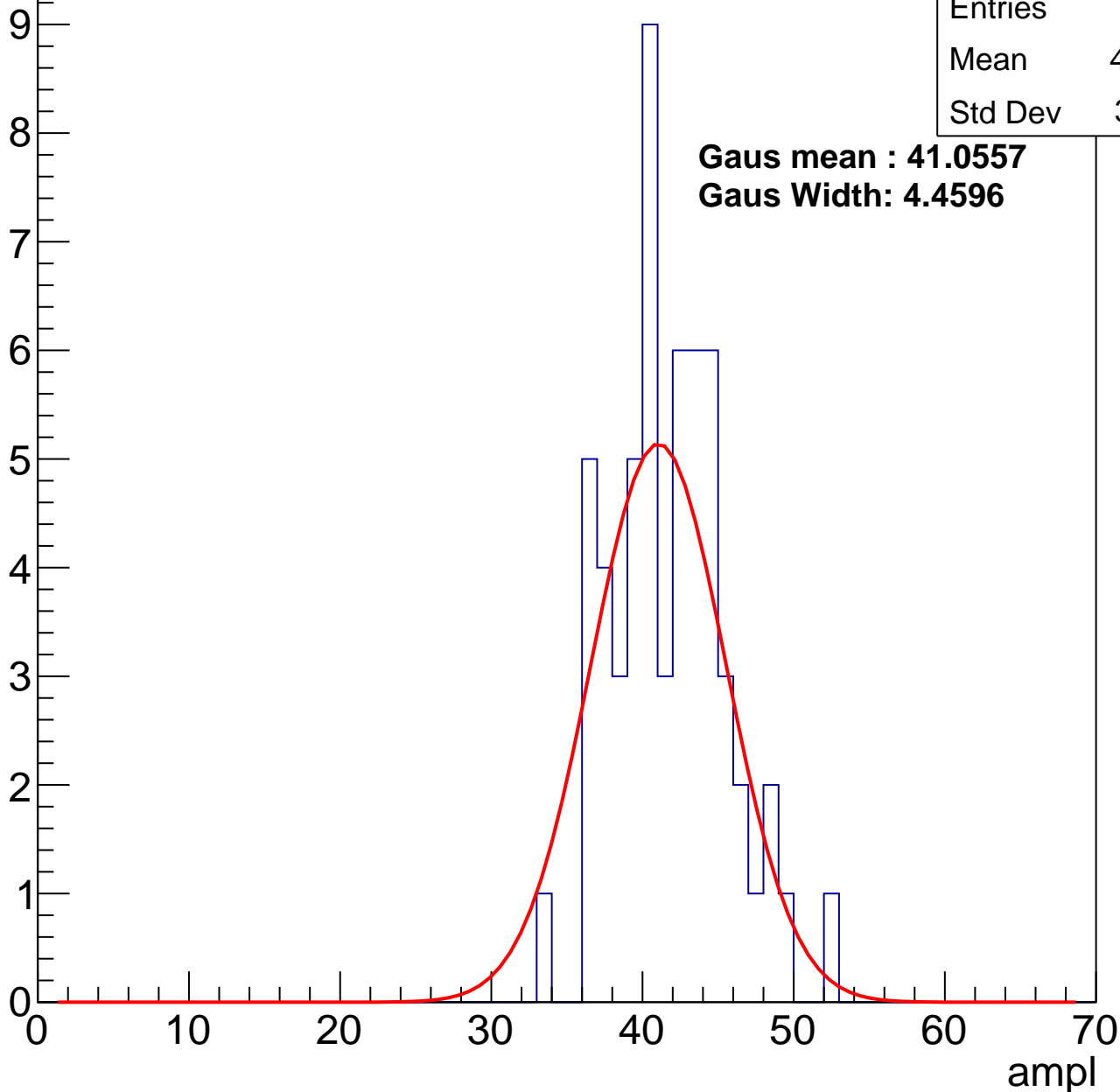
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	41.34
Std Dev	3.721

**Gaus mean : 41.0557**

**Gaus Width: 4.4596**

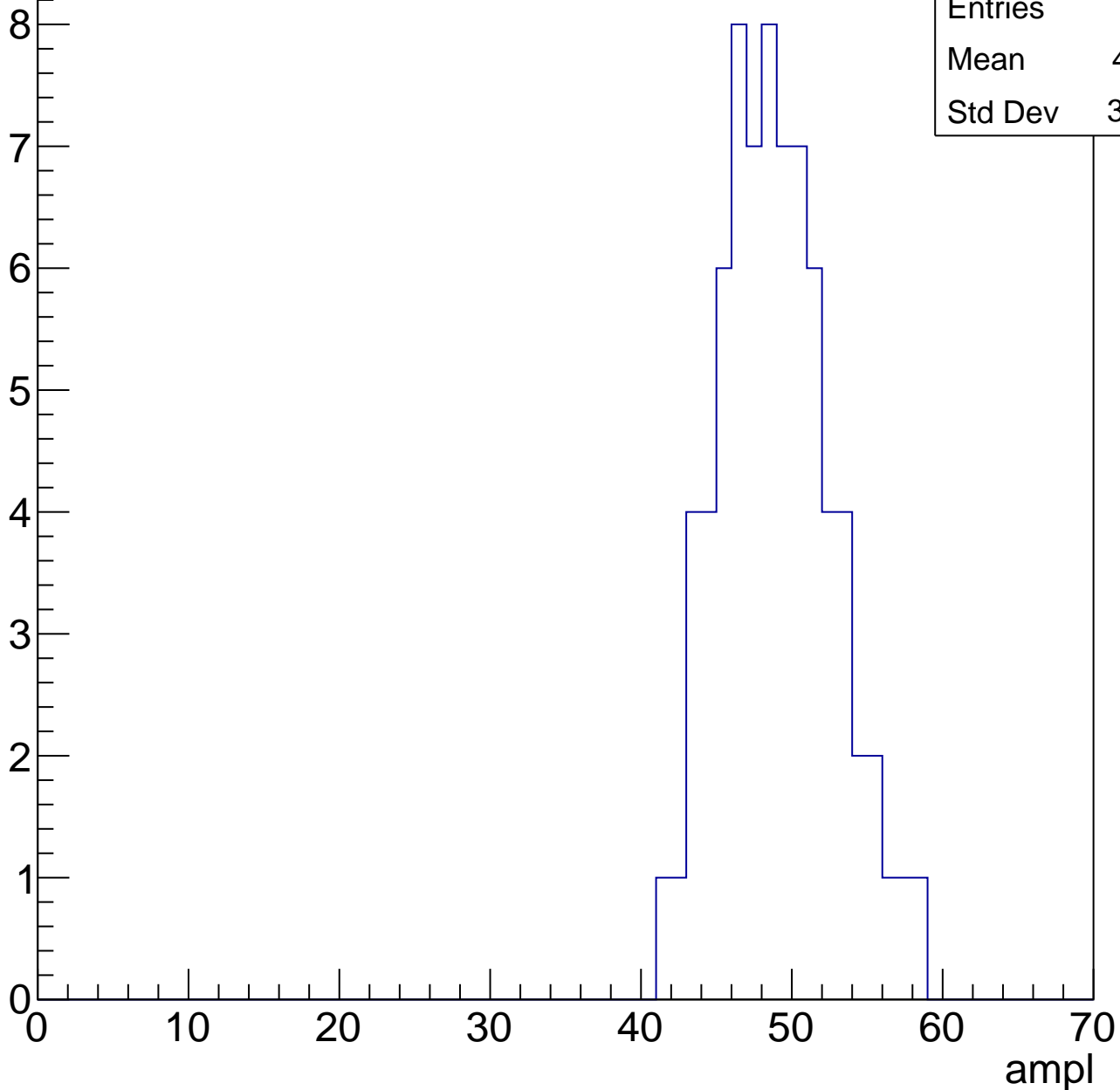


# B1L103S, U21-ch93, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	48.51
Std Dev	3.659

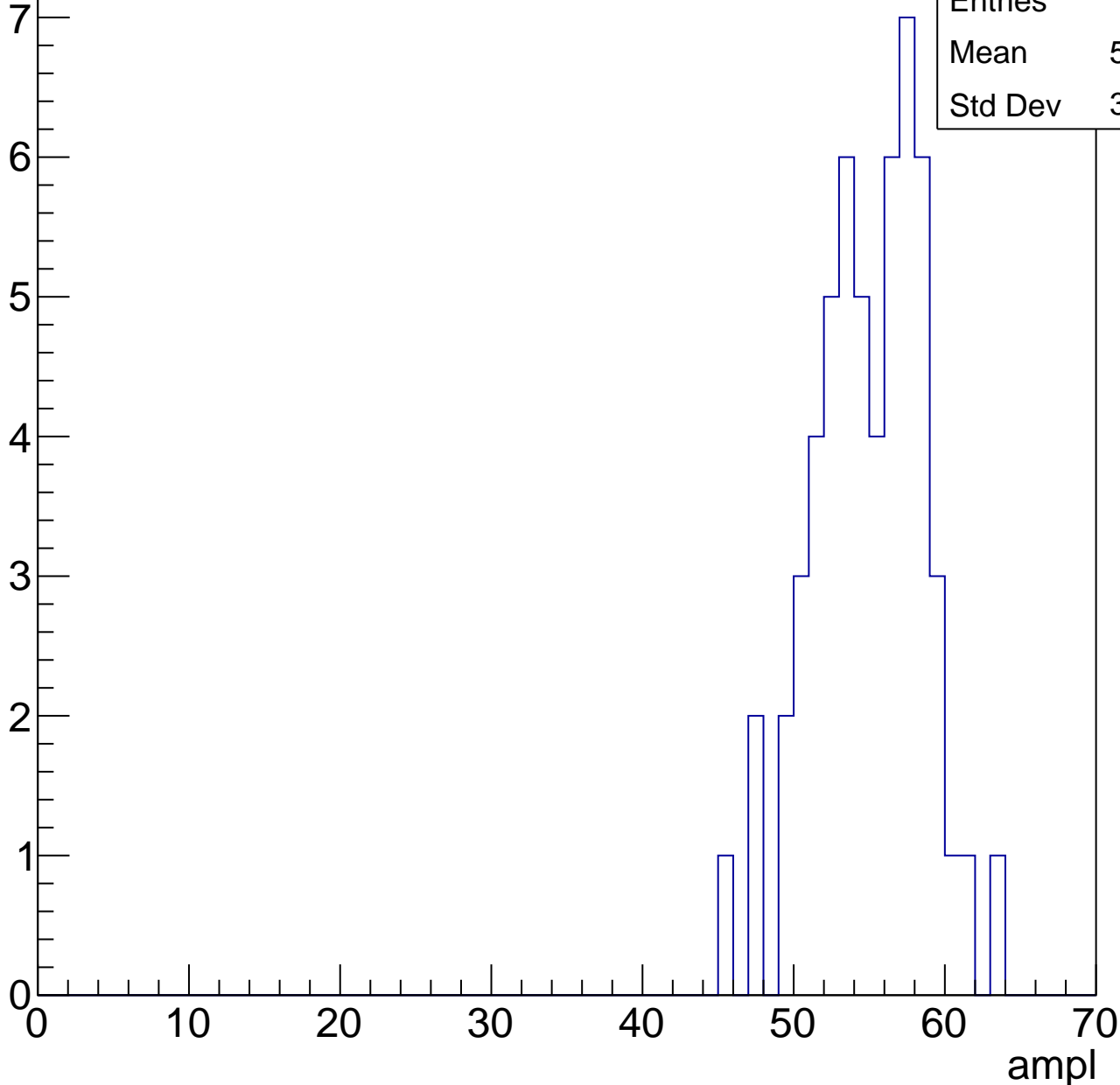


# B1L103S, U21-ch93, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	54.44
Std Dev	3.642

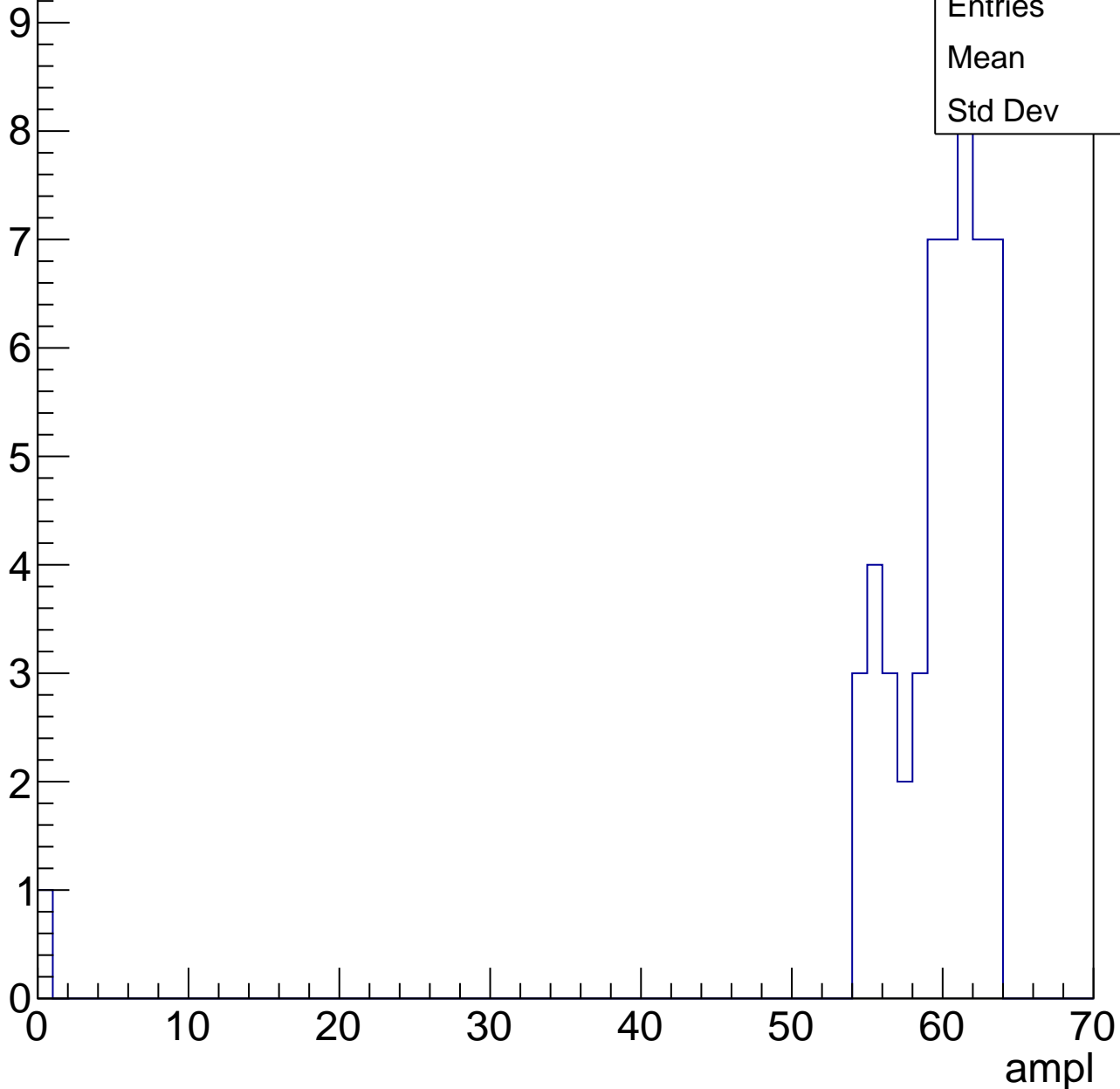


# B1L103S, U21-ch93, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

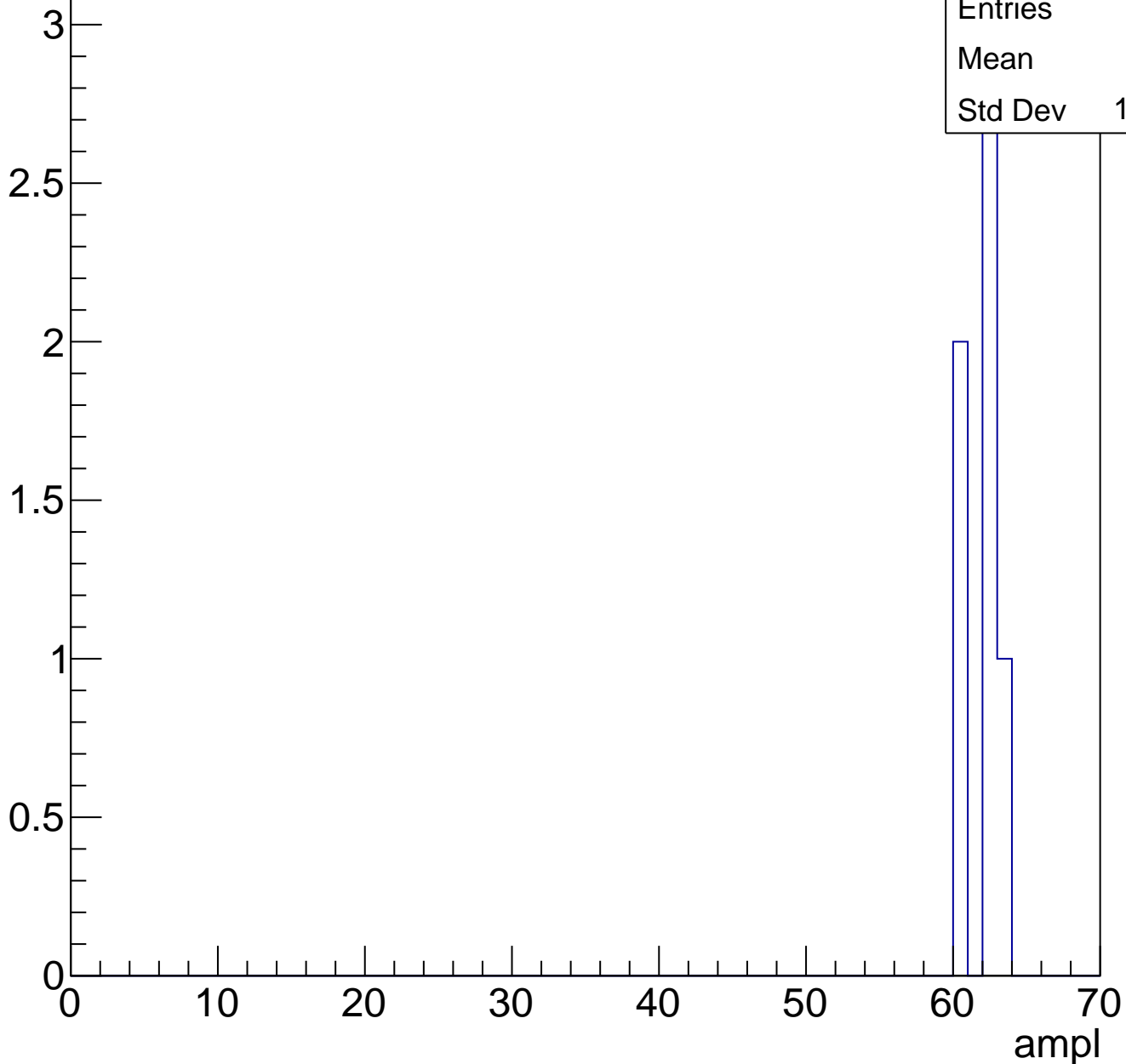
Entries	53
Mean	58.4
Std Dev	8.53



# B1L103S, U21-ch93, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

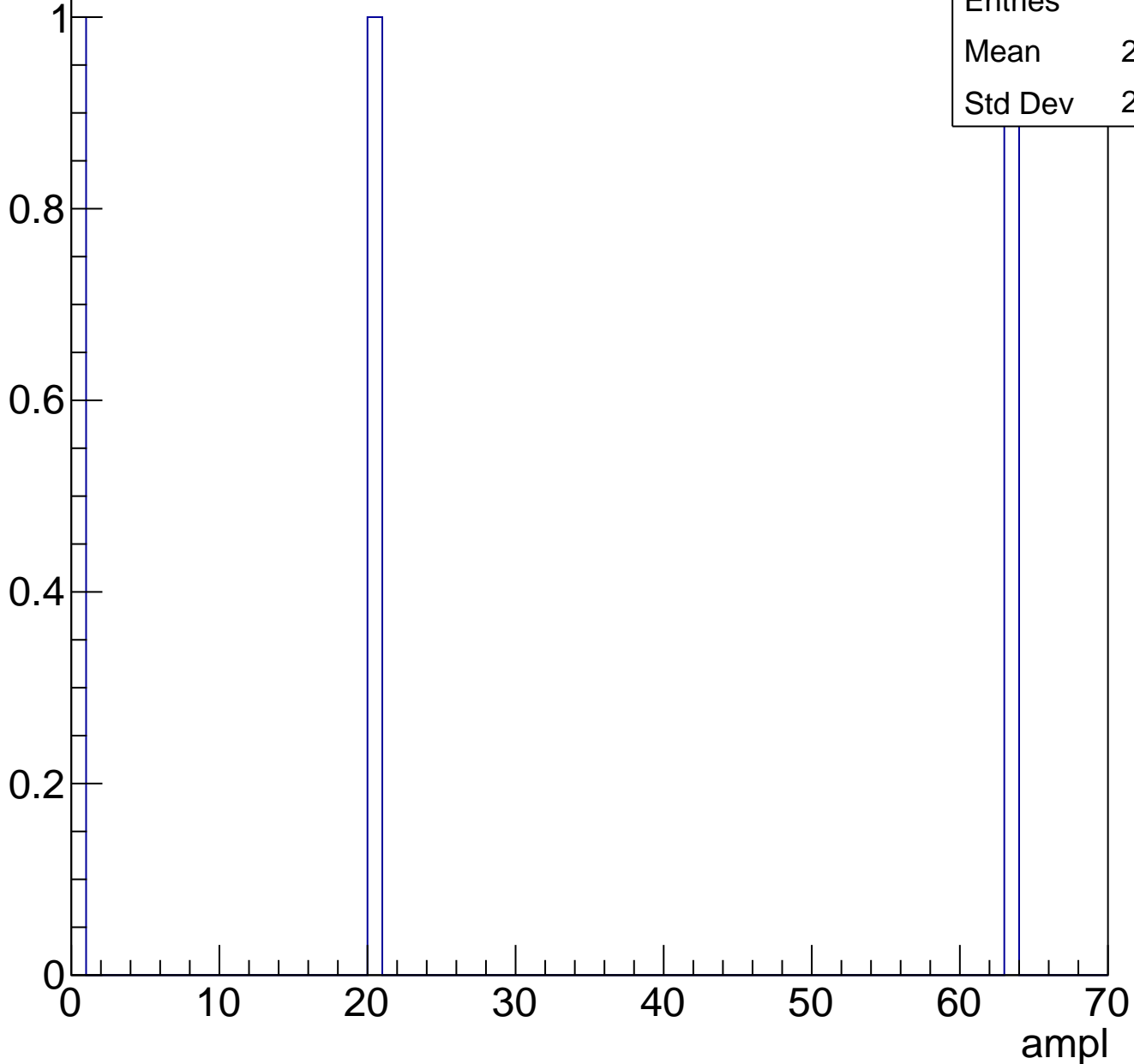




# B1L103S, U21-ch93, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	3
Mean	27.67
Std Dev	26.28

# B1L103S, U21-ch94, adc0

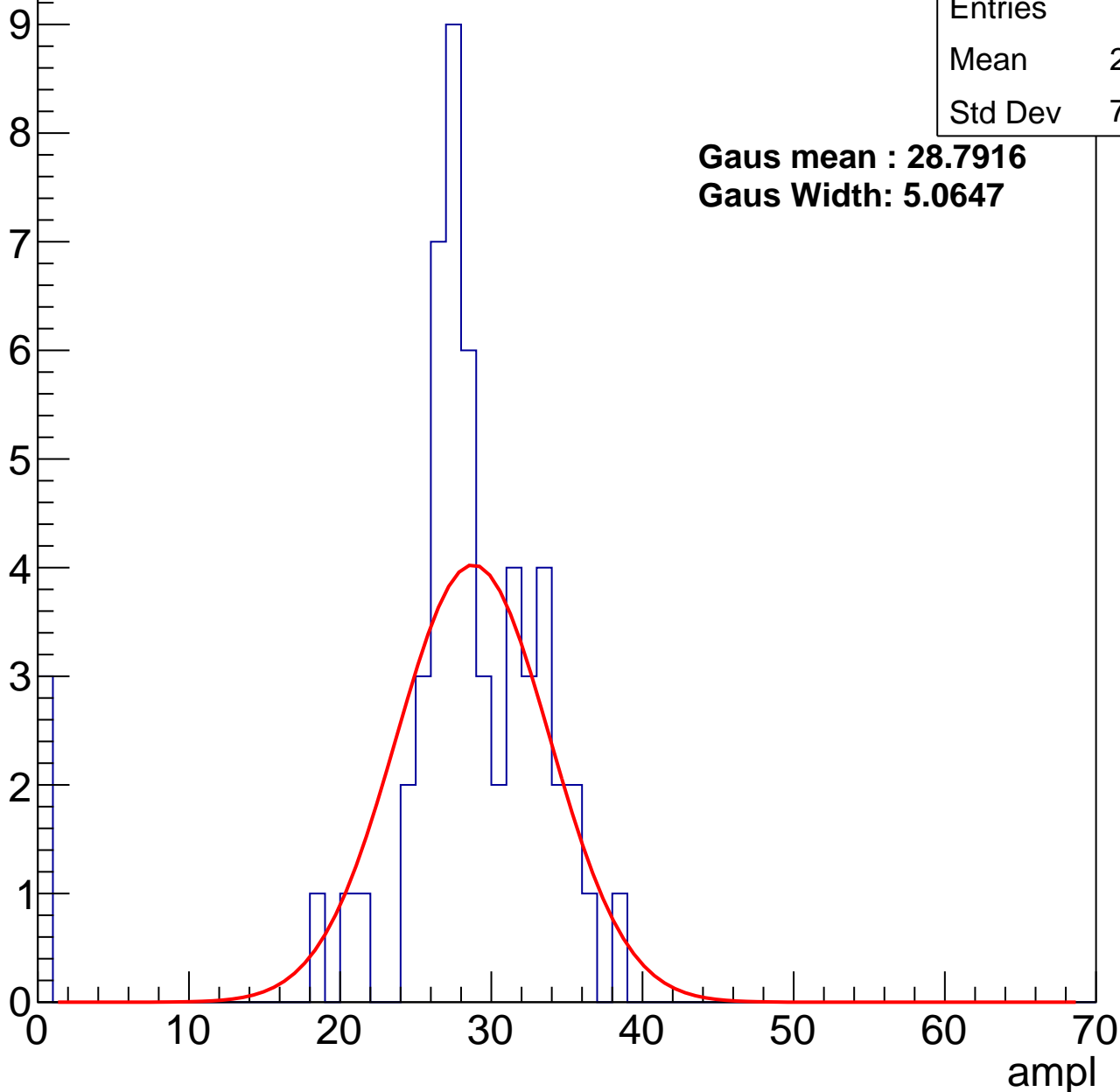
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	27.02
Std Dev	7.552

**Gaus mean : 28.7916**

**Gaus Width: 5.0647**



# B1L103S, U21-ch94, adc1

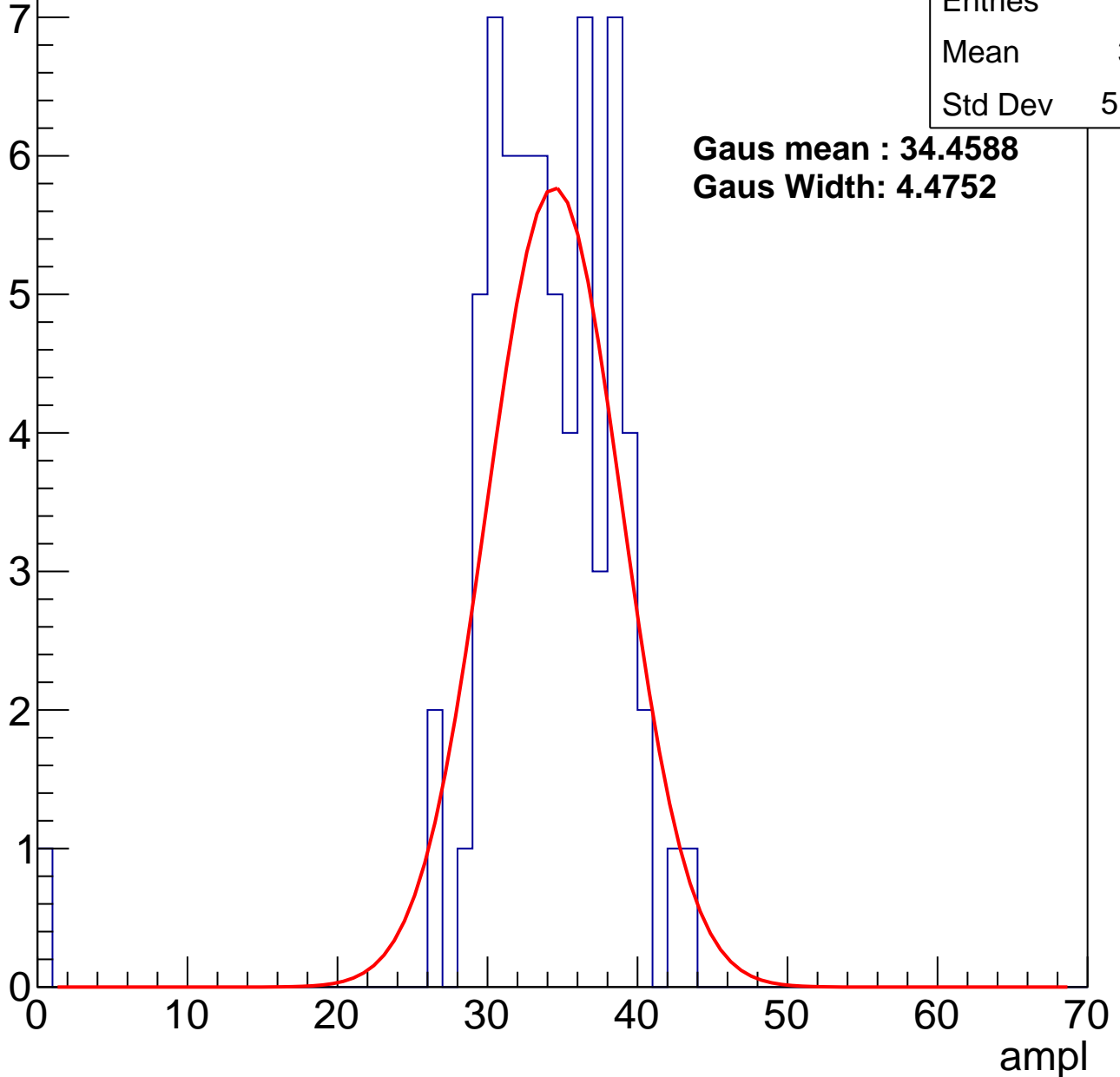
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	33.4
Std Dev	5.563

**Gaus mean : 34.4588**

**Gaus Width: 4.4752**



# B1L103S, U21-ch94, adc2

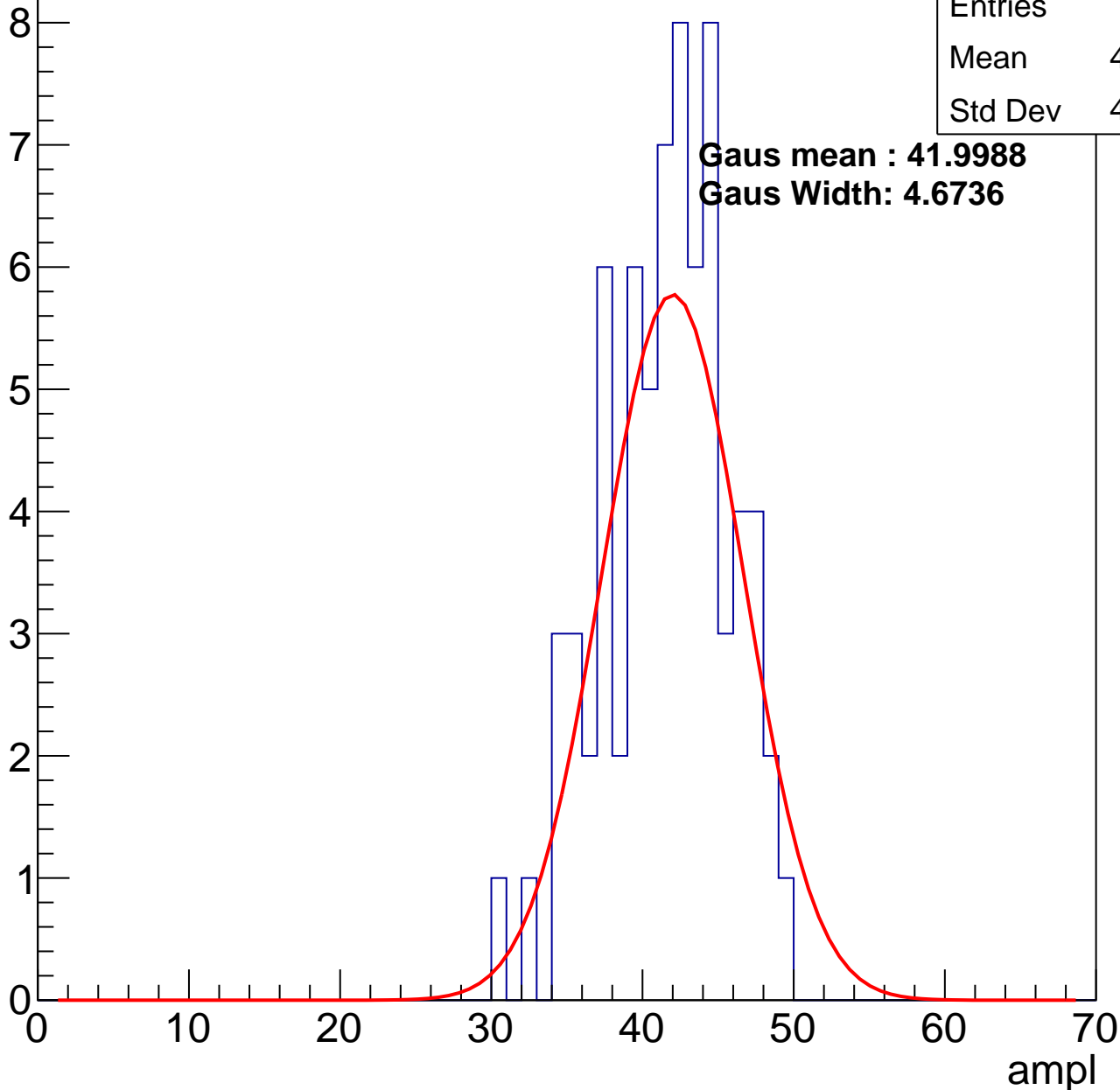
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	41.08
Std Dev	4.095

**Gaus mean : 41.9988**

**Gaus Width: 4.6736**

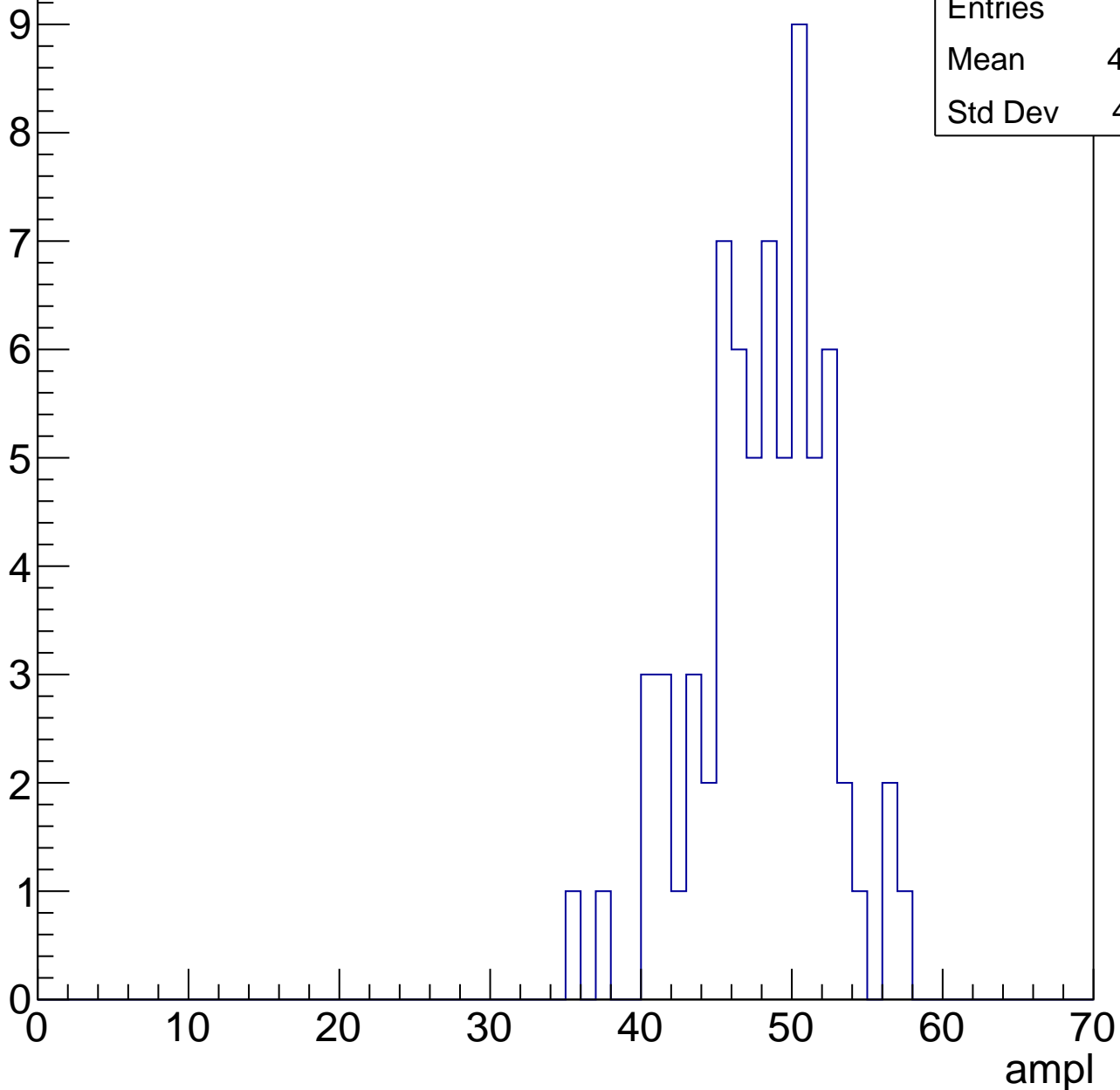


# B1L103S, U21-ch94, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	47.53
Std Dev	4.351

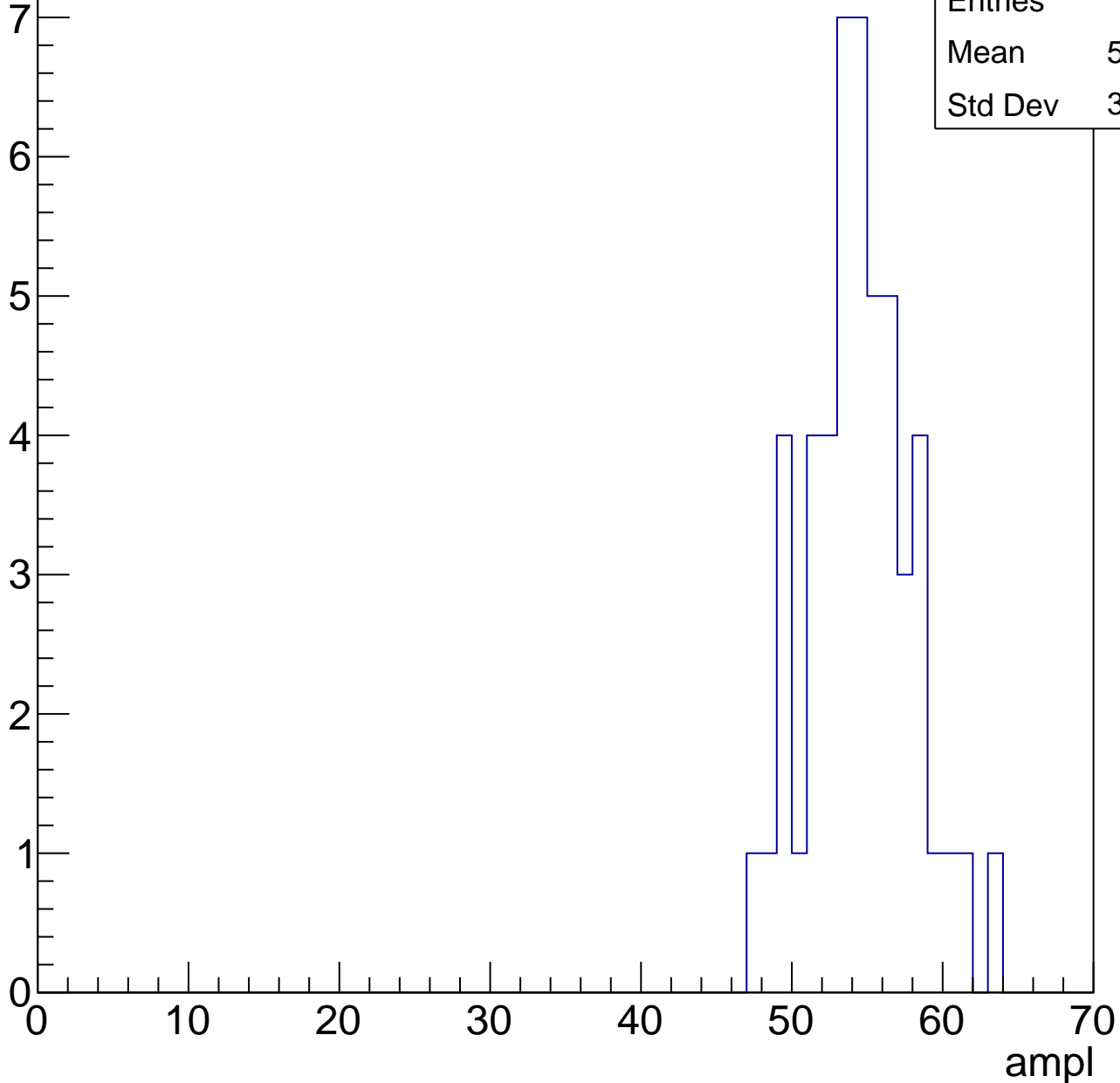


# B1L103S, U21-ch94, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	54.06
Std Dev	3.367

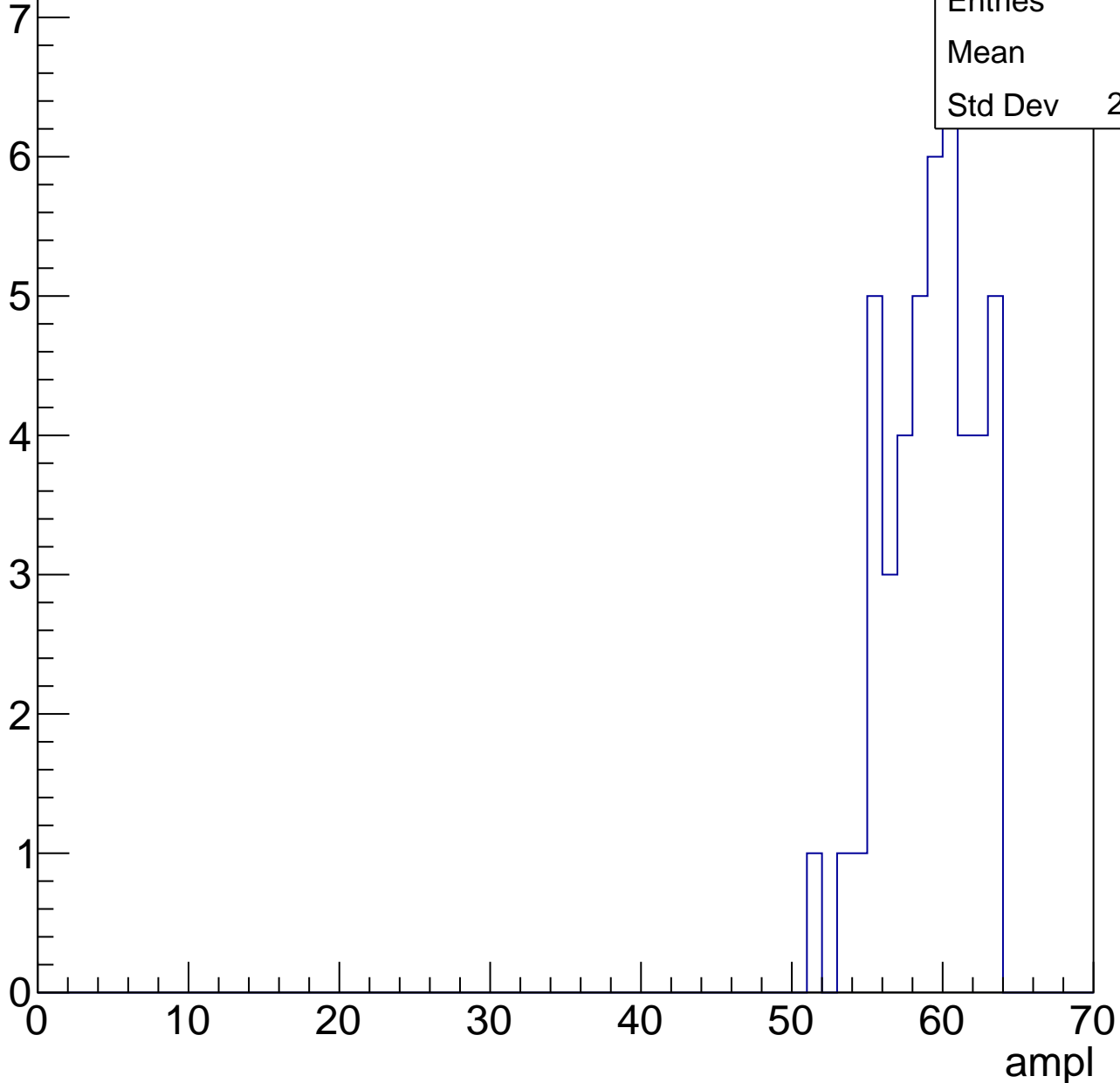


# B1L103S, U21-ch94, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	46
Mean	58.7
Std Dev	2.903

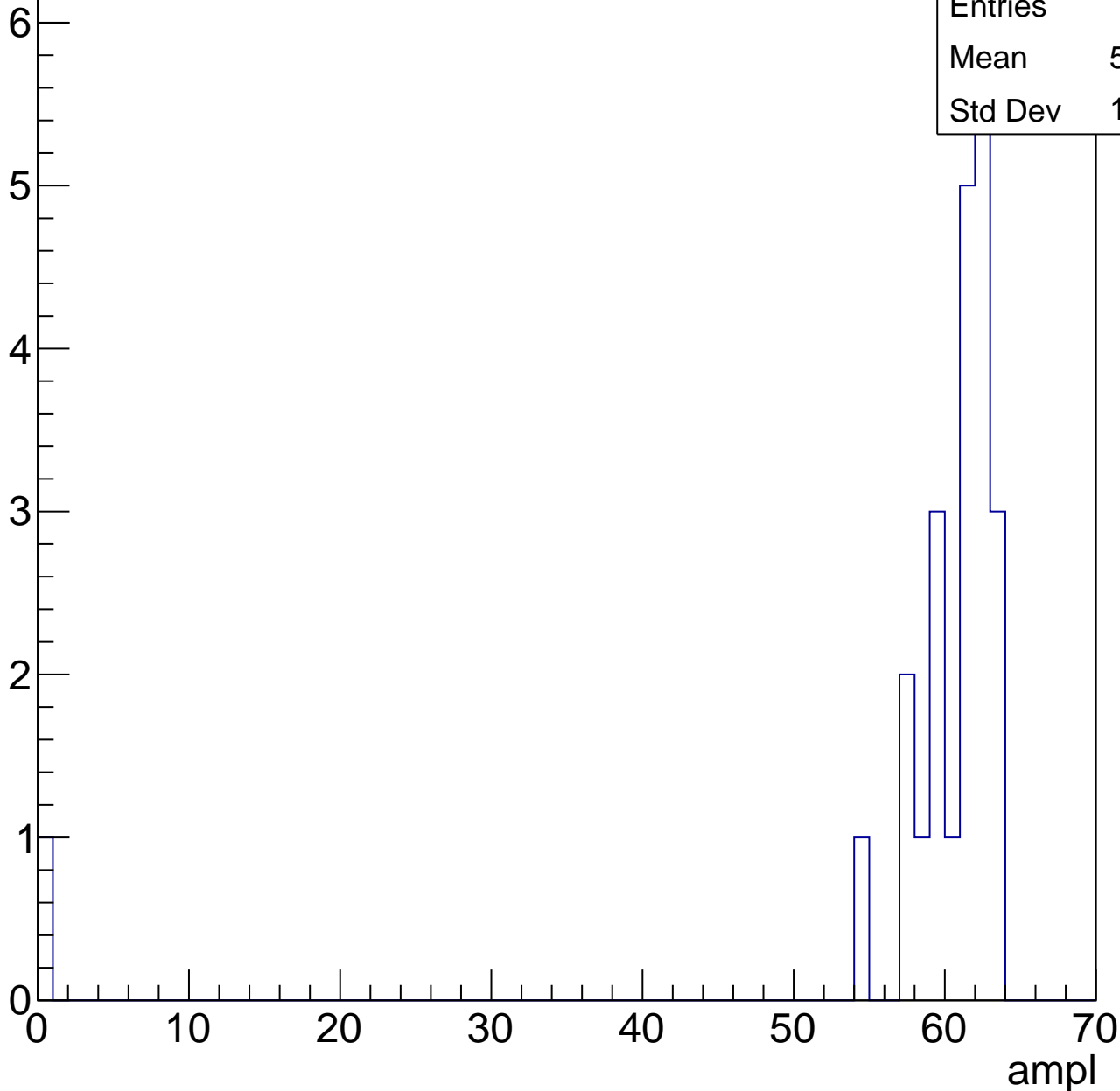


# B1L103S, U21-ch94, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	23
Mean	57.78
Std Dev	12.52

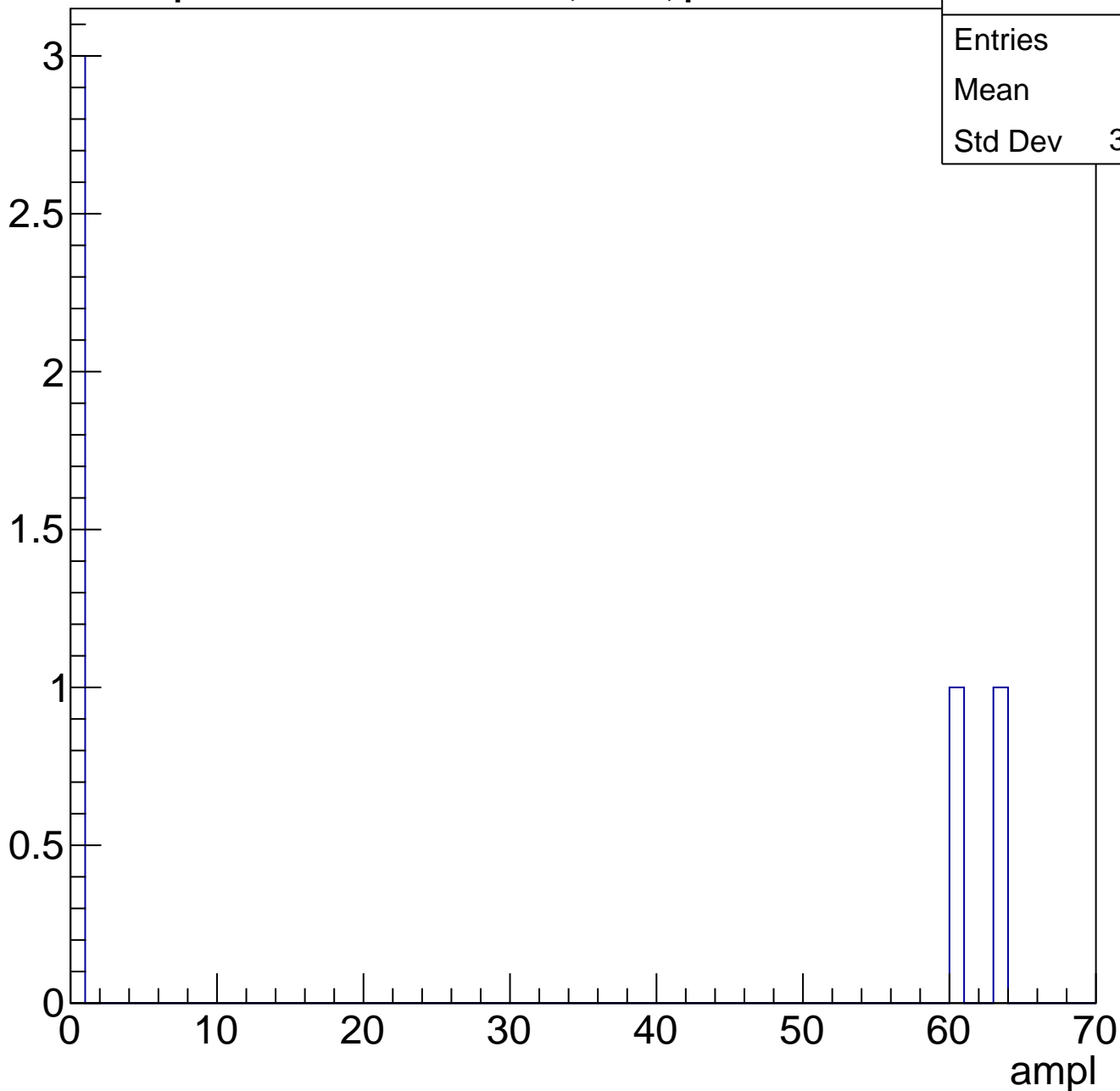




# B1L103S, U21-ch94, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U21-ch95, adc0

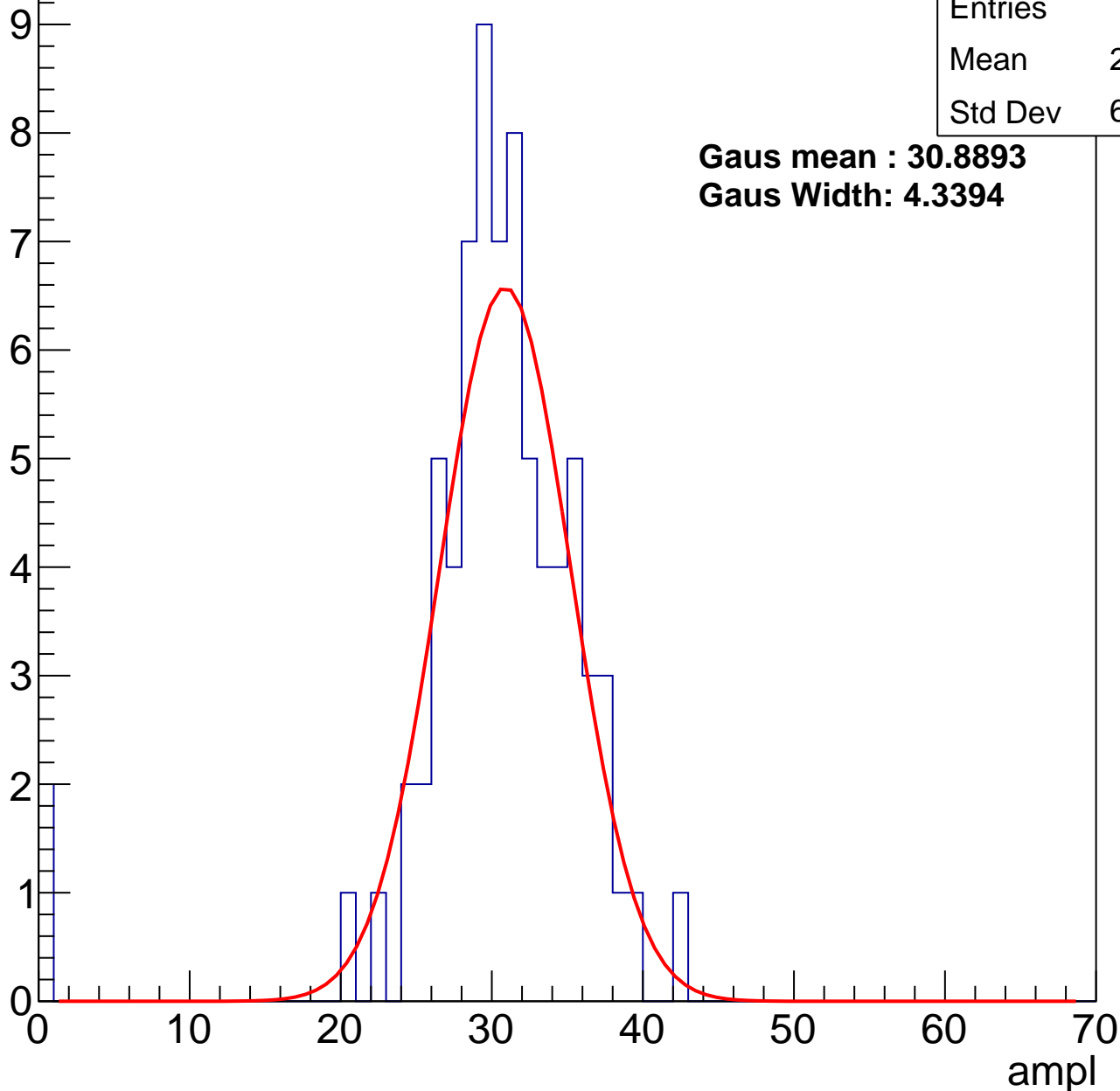
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	29.79
Std Dev	6.359

**Gaus mean : 30.8893**

**Gaus Width: 4.3394**



# B1L103S, U21-ch95, adc1

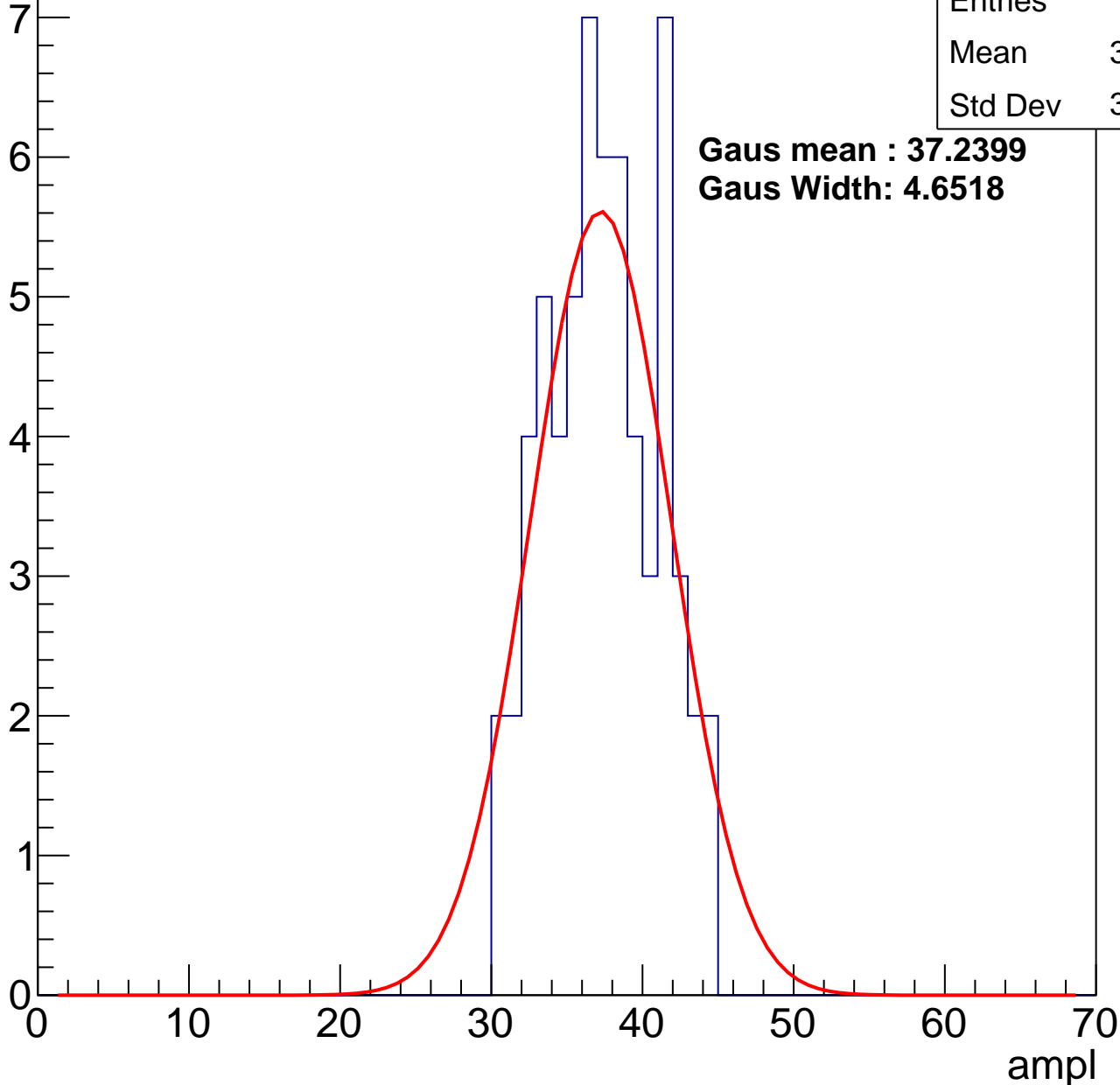
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	36.95
Std Dev	3.634

**Gaus mean : 37.2399**

**Gaus Width: 4.6518**



# B1L103S, U21-ch95, adc2

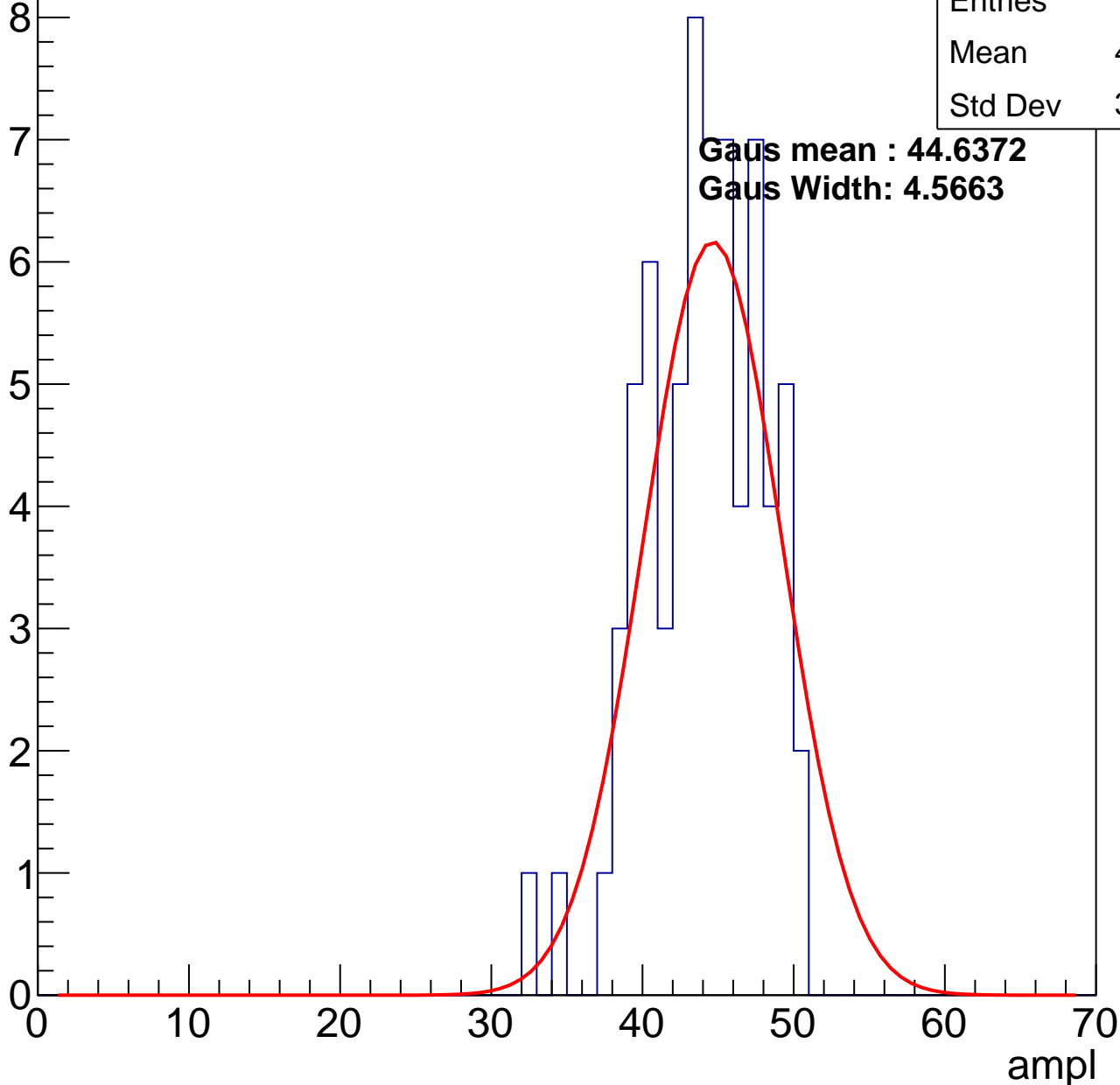
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	43.51
Std Dev	3.821

**Gaus mean : 44.6372**

**Gaus Width: 4.5663**

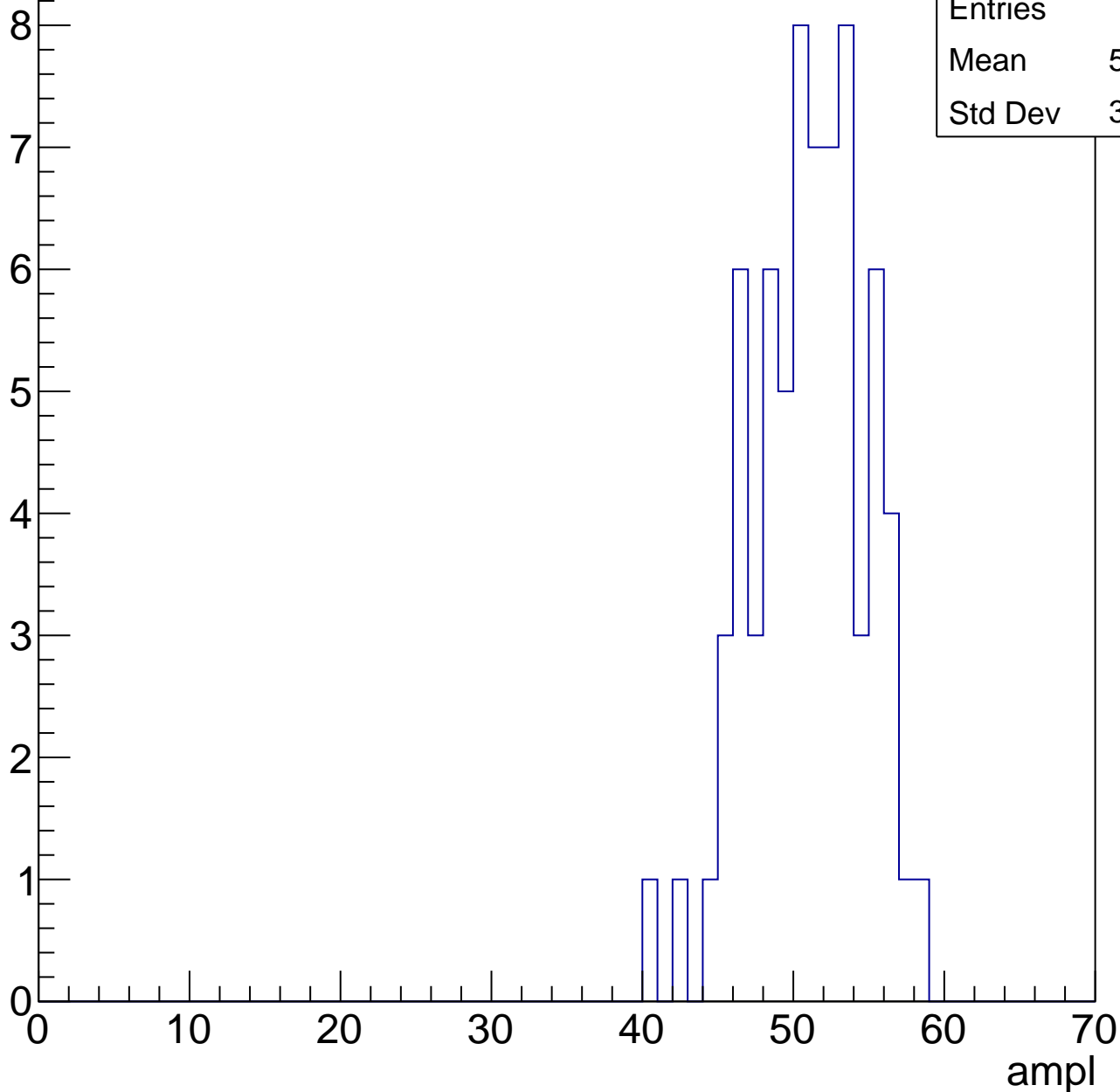


# B1L103S, U21-ch95, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

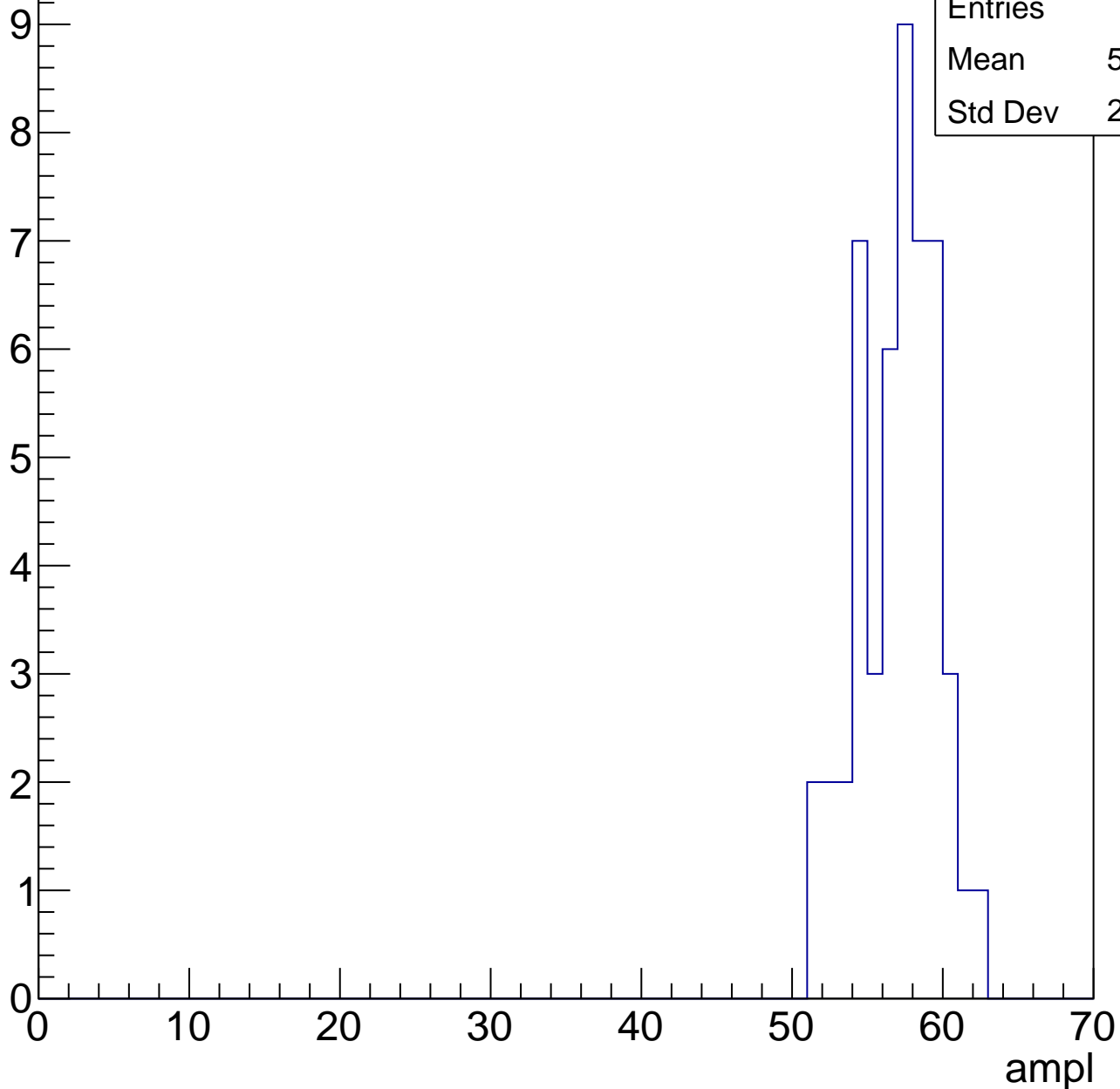
Entries	71
Mean	50.52
Std Dev	3.696



# B1L103S, U21-ch95, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



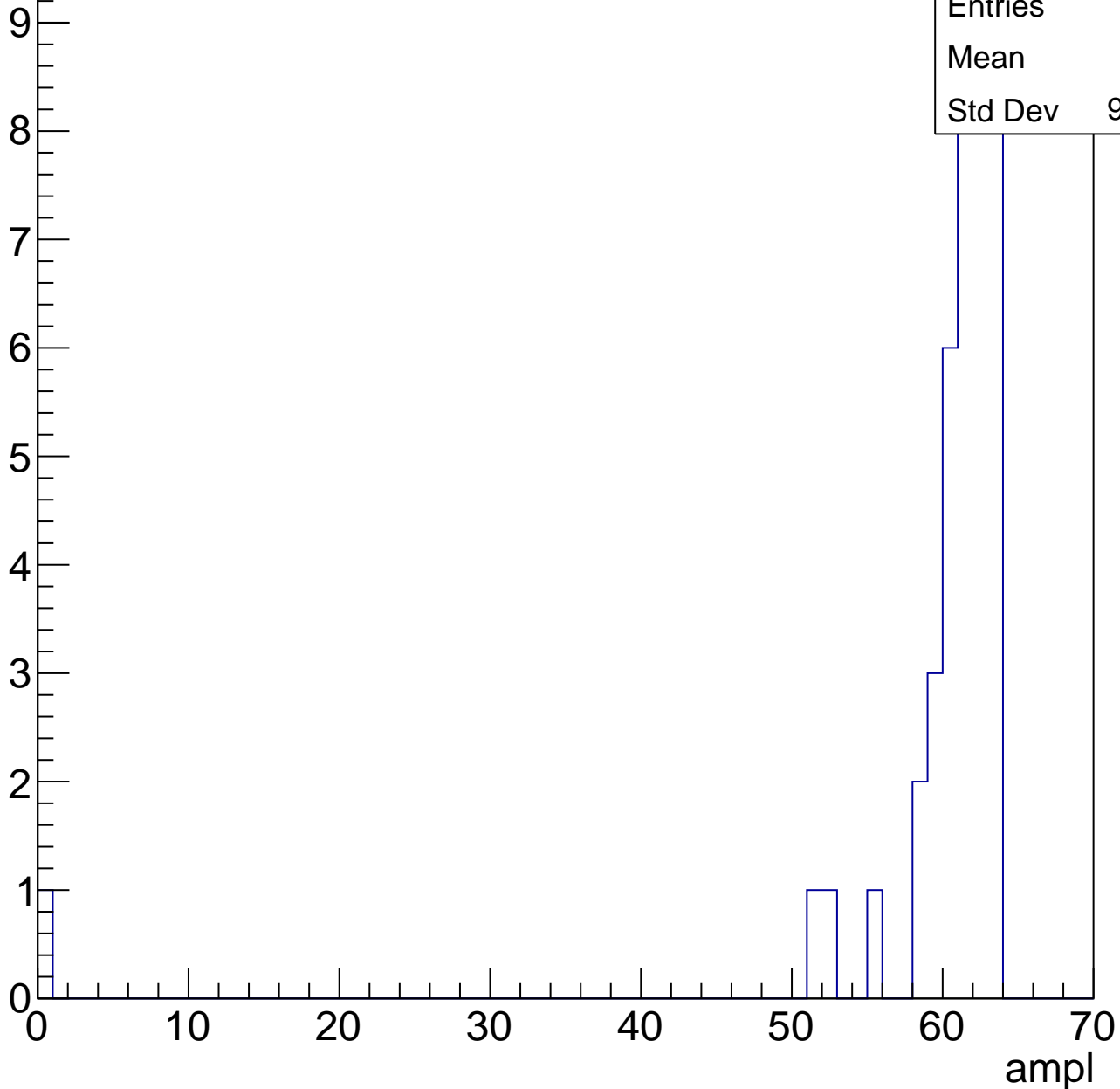
Entries	50
Mean	56.52
Std Dev	2.555

# B1L103S, U21-ch95, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	40
Mean	59
Std Dev	9.816



# B1L103S, U21-ch95, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	4
Mean	62
Std Dev	1.225



# B1L103S, U21-ch95, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L103S, U21-ch96, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	67
Mean	27.46
Std Dev	3.576

**Gaus mean : 28.0763**

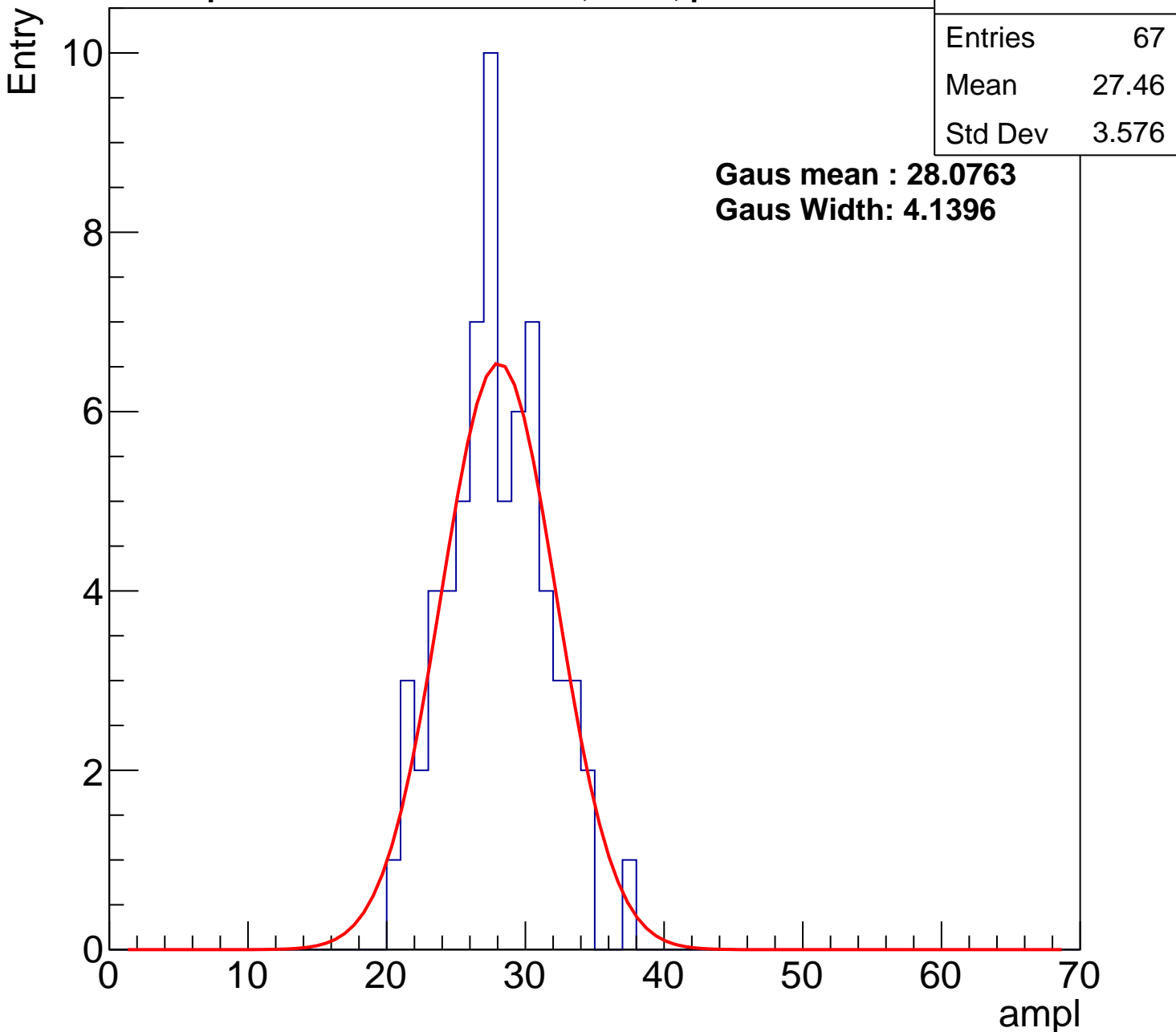
**Gaus Width: 4.1396**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



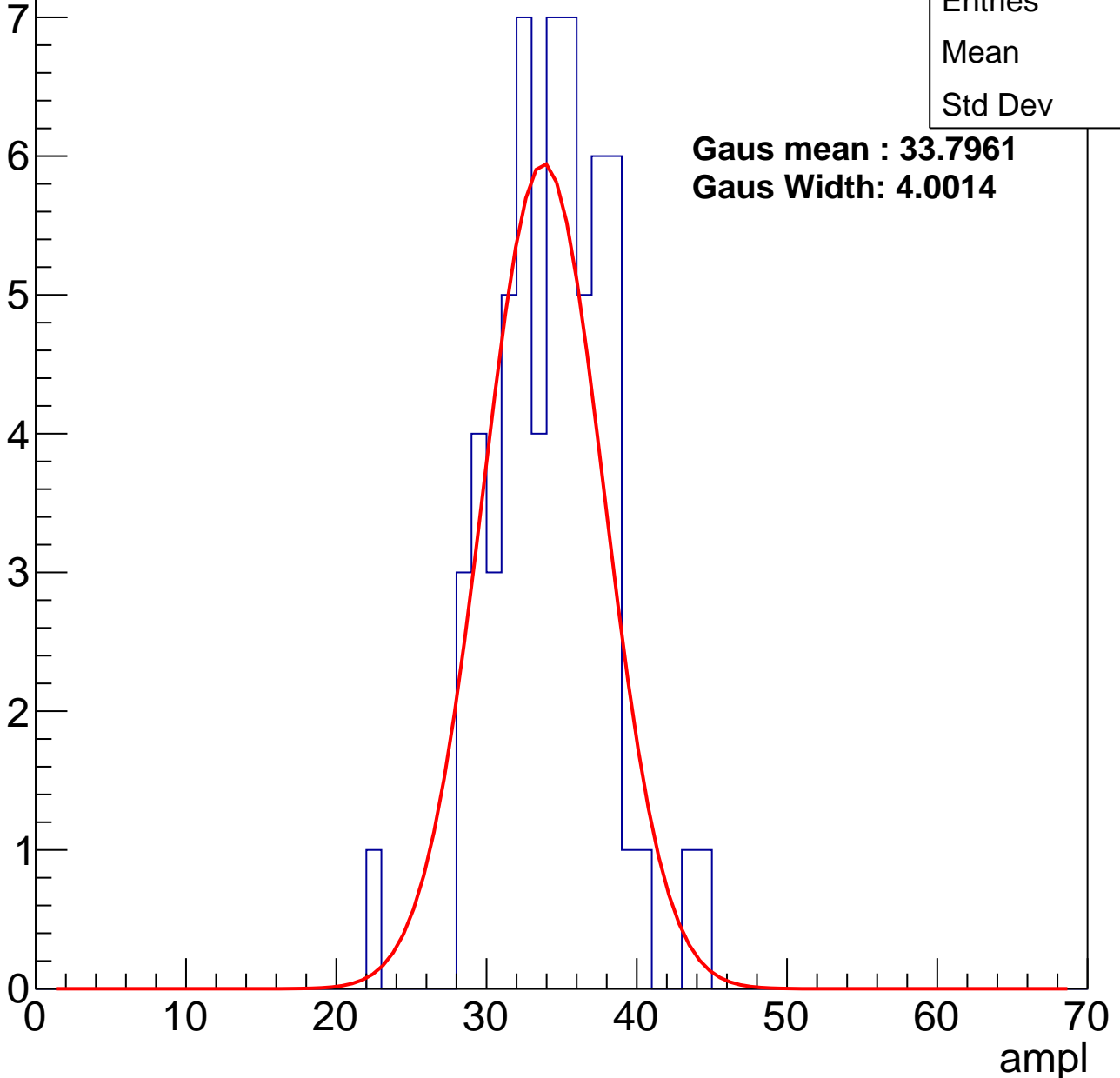
# B1L103S, U21-ch96, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	33.9
Std Dev	3.8

**Gaus mean : 33.7961**  
**Gaus Width: 4.0014**



# B1L103S, U21-ch96, adc2

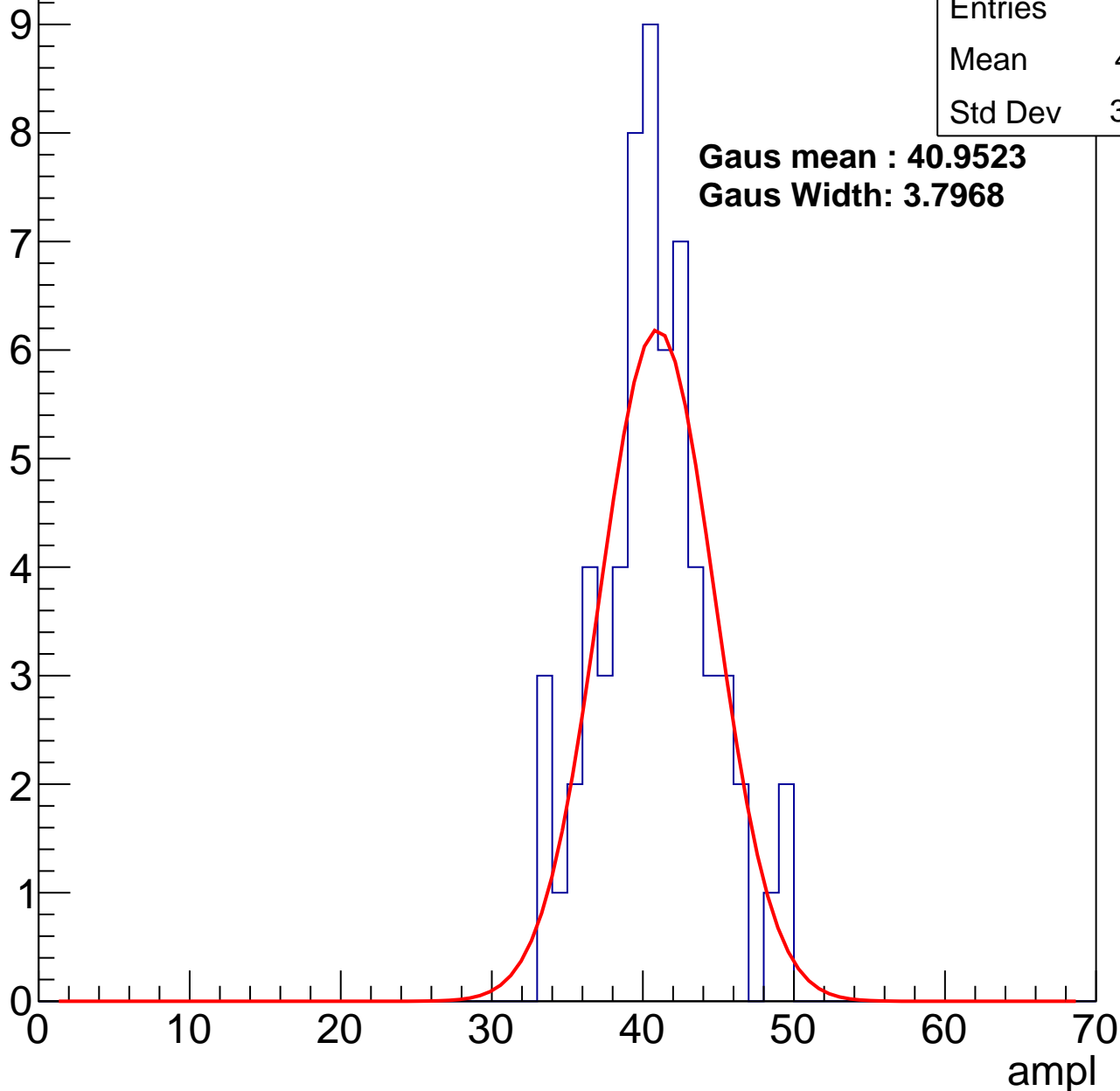
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	40.31
Std Dev	3.666

**Gaus mean : 40.9523**

**Gaus Width: 3.7968**

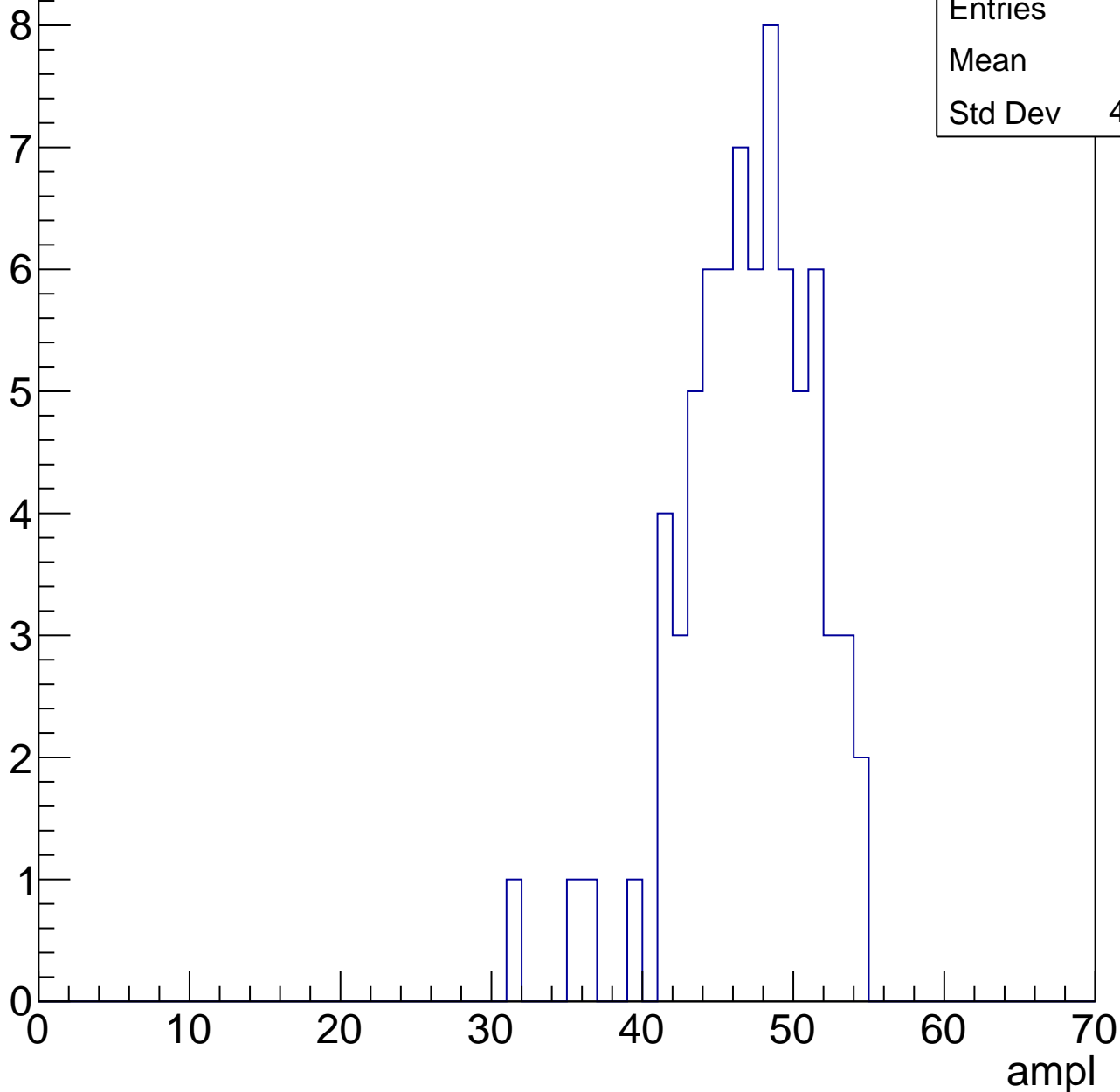


# B1L103S, U21-ch96, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	46.5
Std Dev	4.357

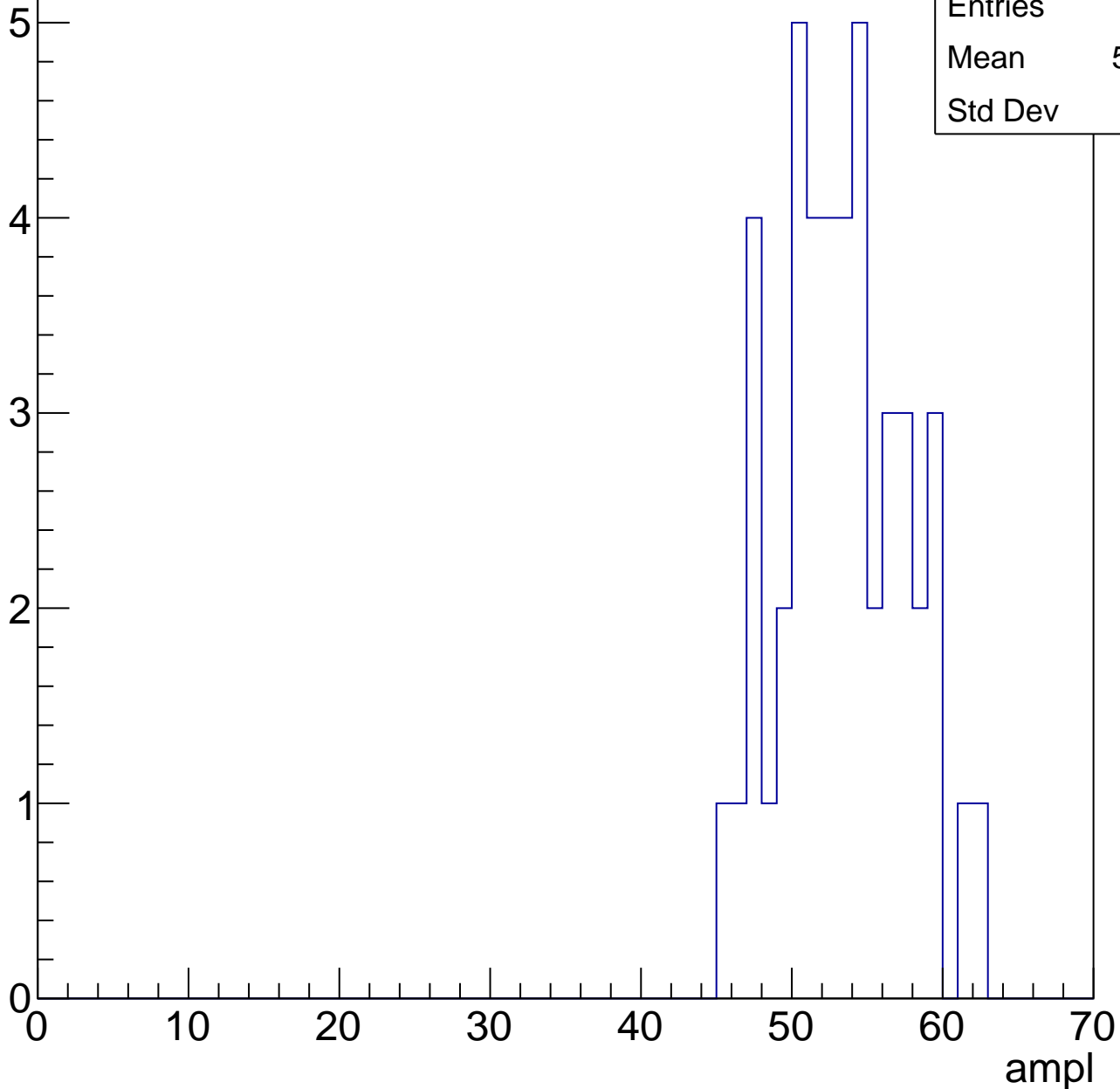


# B1L103S, U21-ch96, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	46
Mean	52.91
Std Dev	4.09

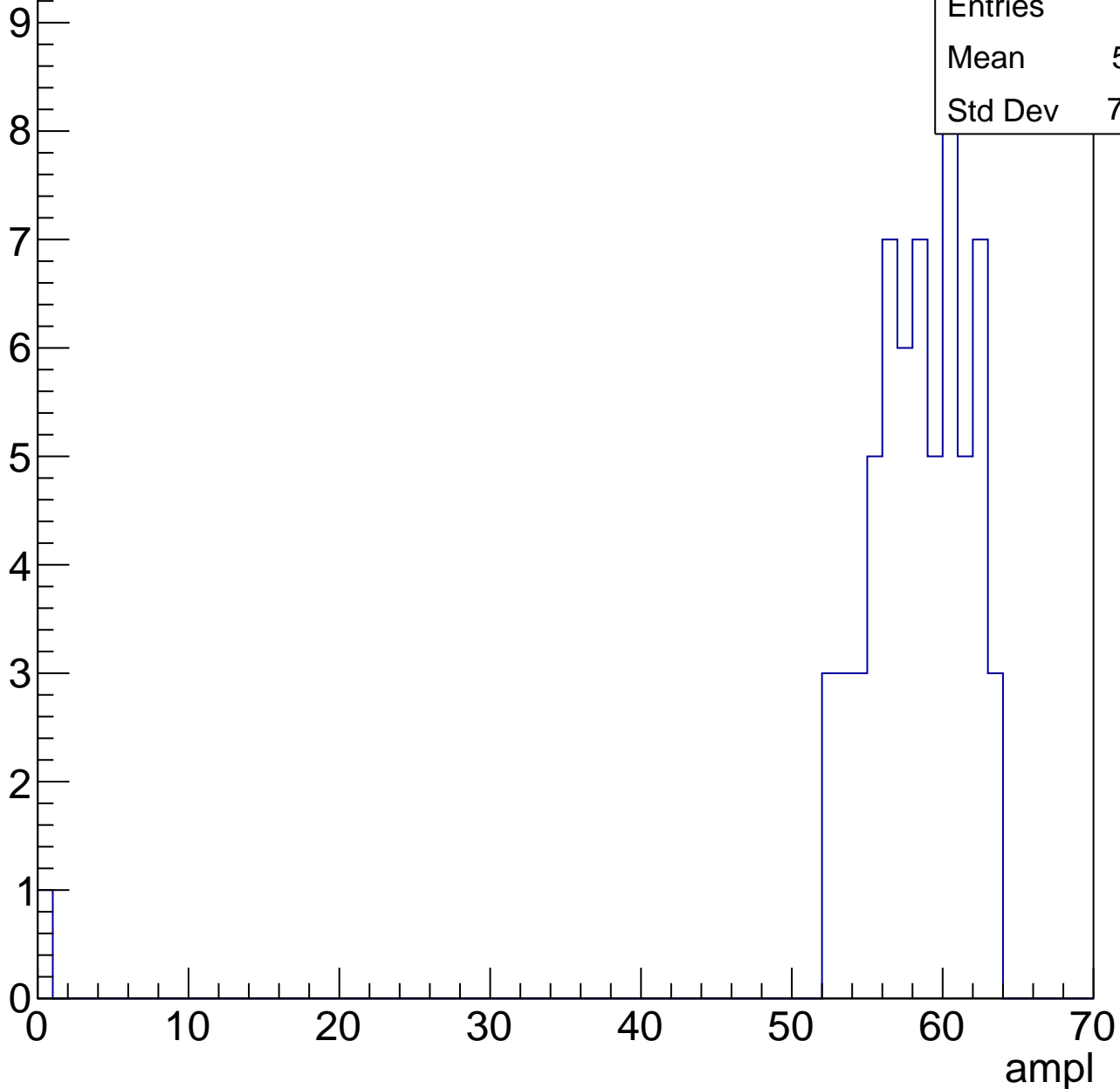


# B1L103S, U21-ch96, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	57.11
Std Dev	7.802

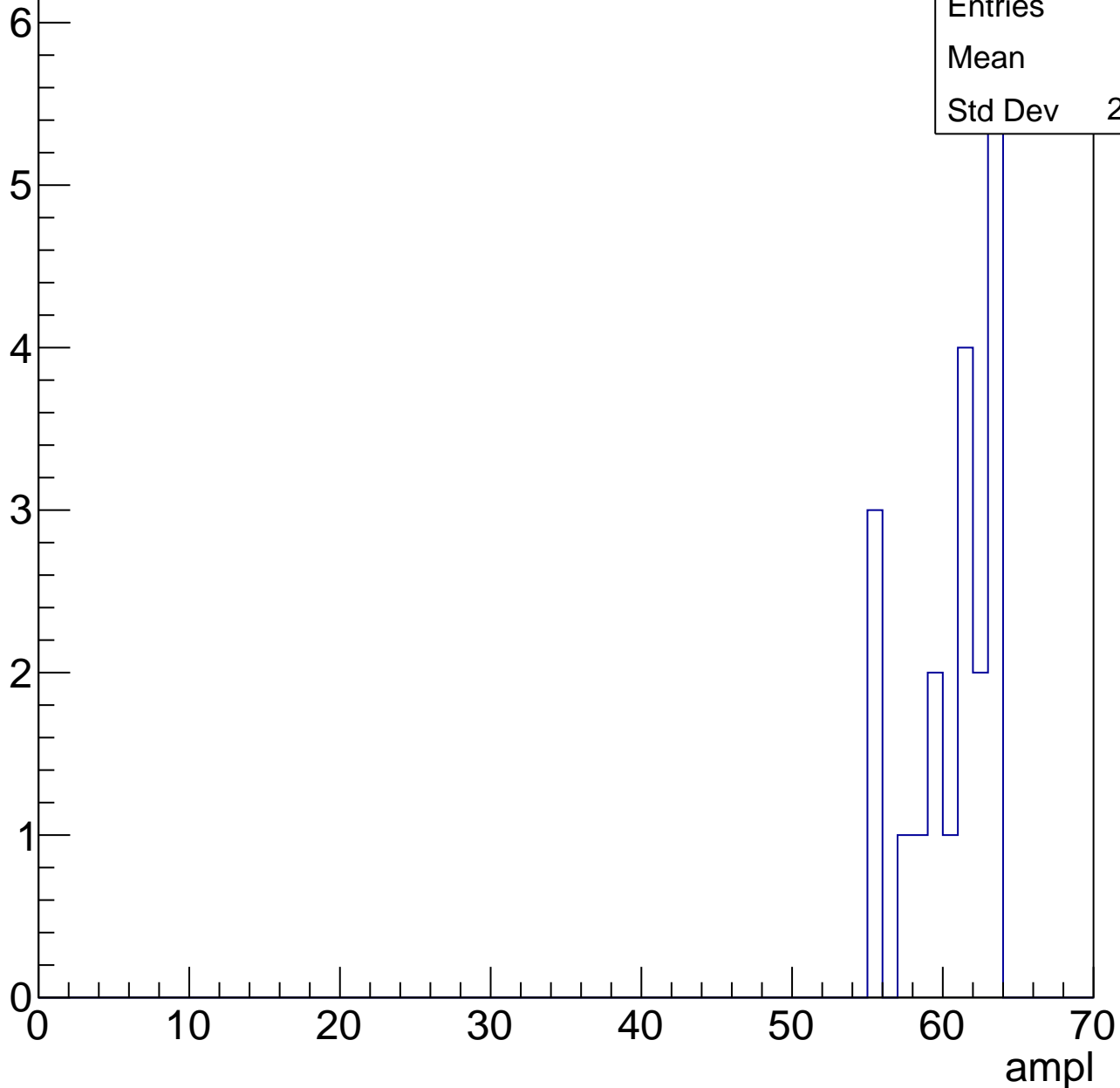


# B1L103S, U21-ch96, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	20
Mean	60.2
Std Dev	2.786





# B1L103S, U21-ch96, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U21-ch97, adc0

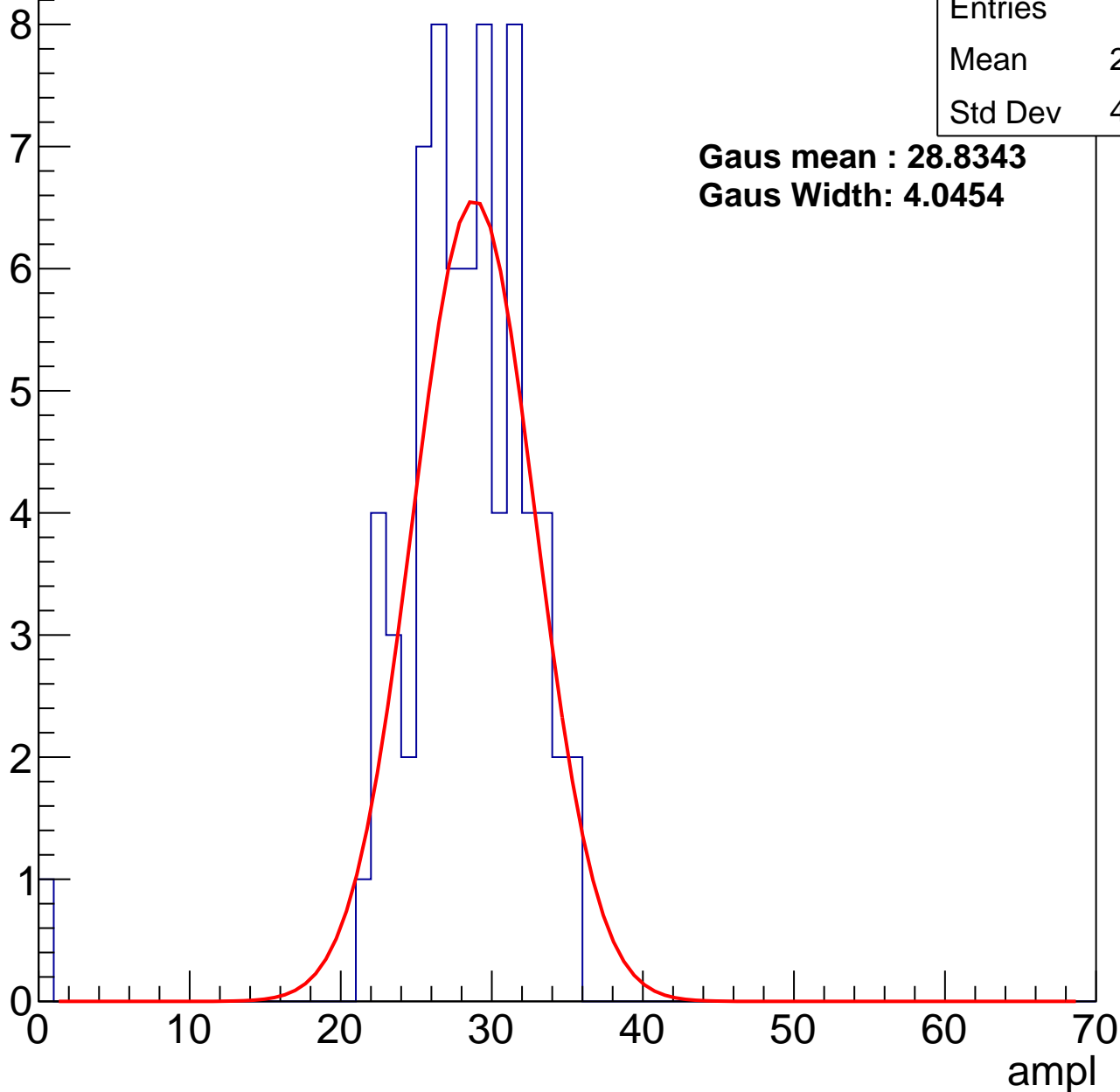
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	27.67
Std Dev	4.792

**Gaus mean : 28.8343**

**Gaus Width: 4.0454**



# B1L103S, U21-ch97, adc1

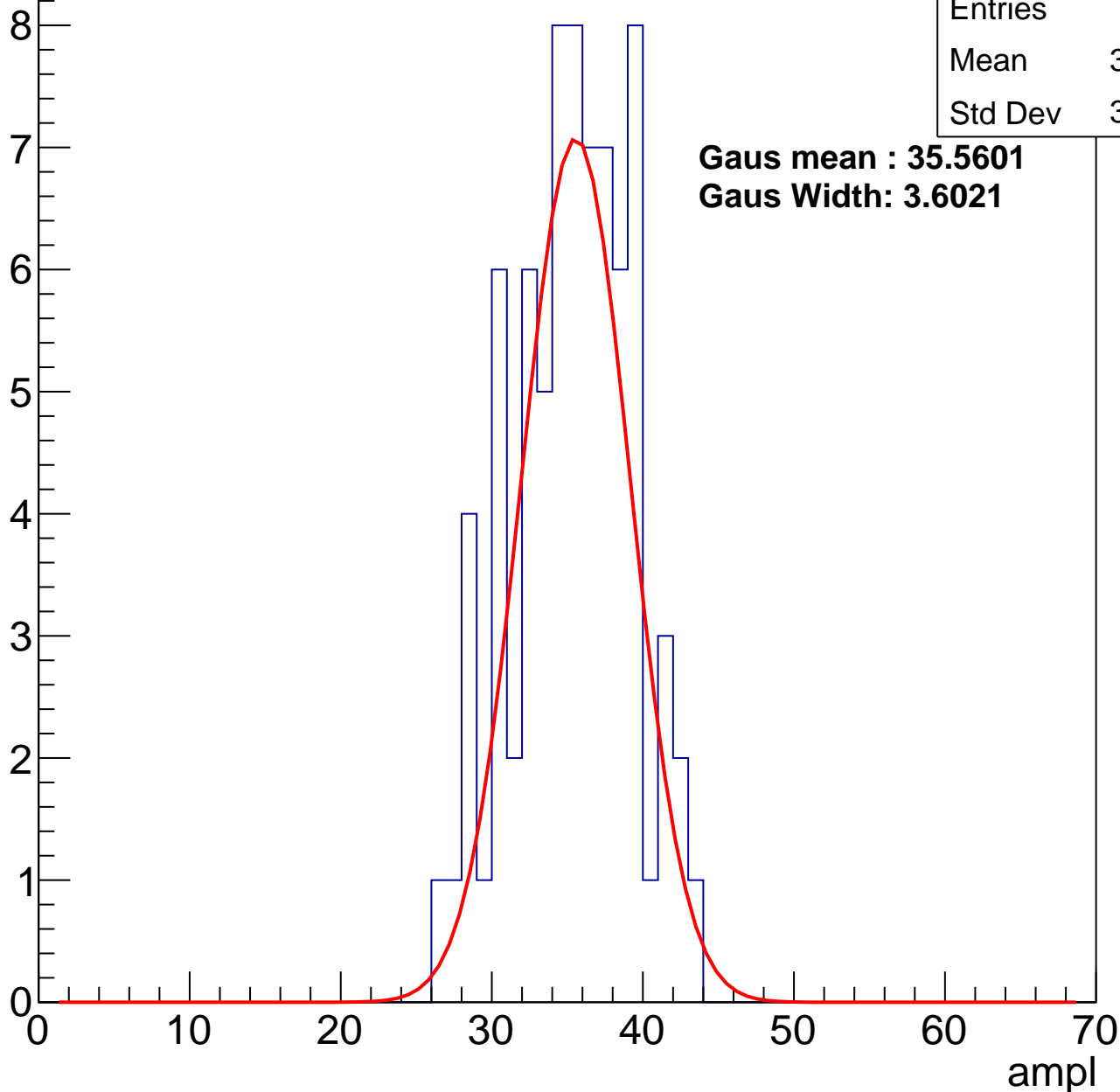
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	34.88
Std Dev	3.868

**Gaus mean : 35.5601**

**Gaus Width: 3.6021**



# B1L103S, U21-ch97, adc2

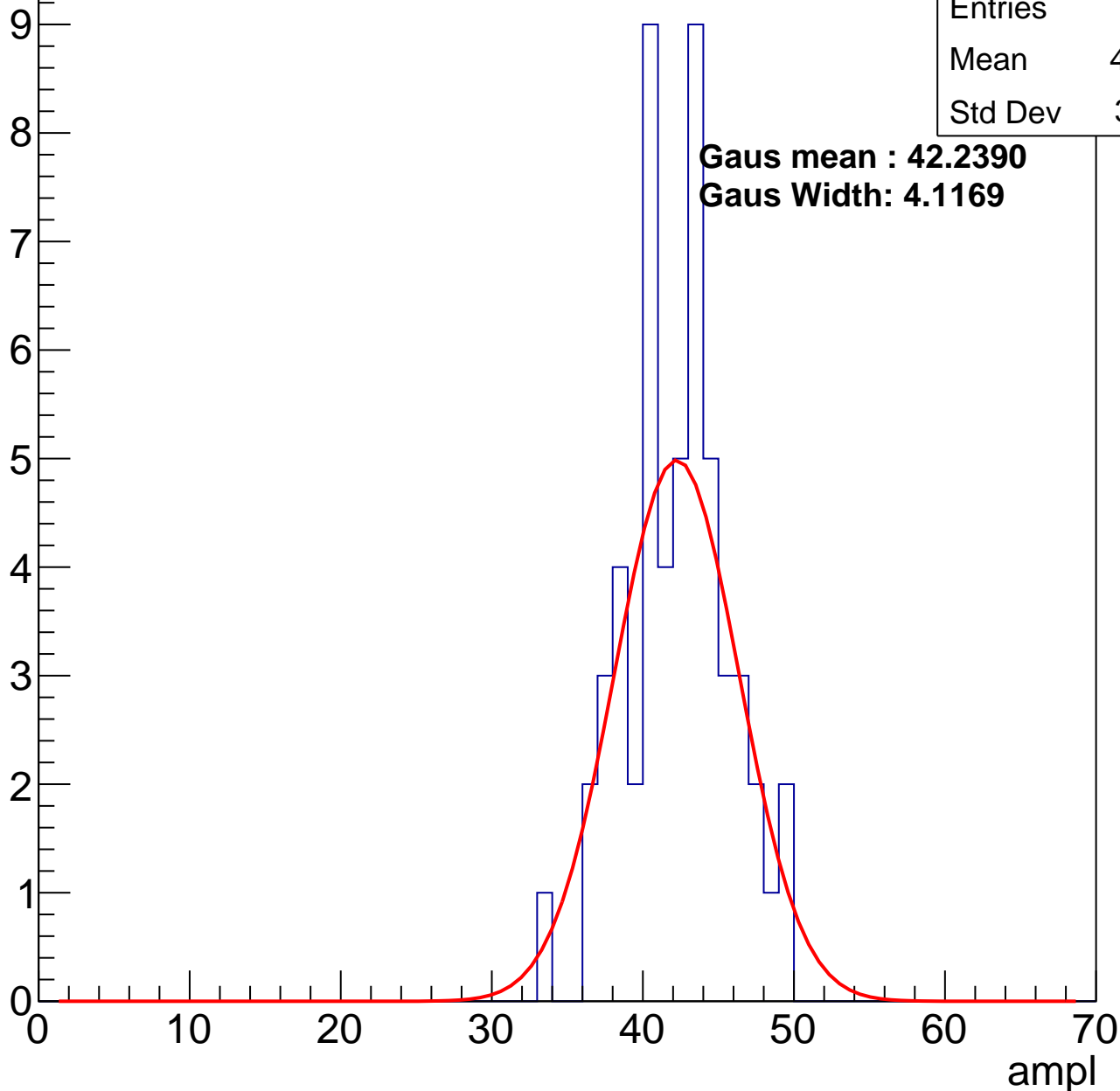
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	41.82
Std Dev	3.401

**Gaus mean : 42.2390**

**Gaus Width: 4.1169**

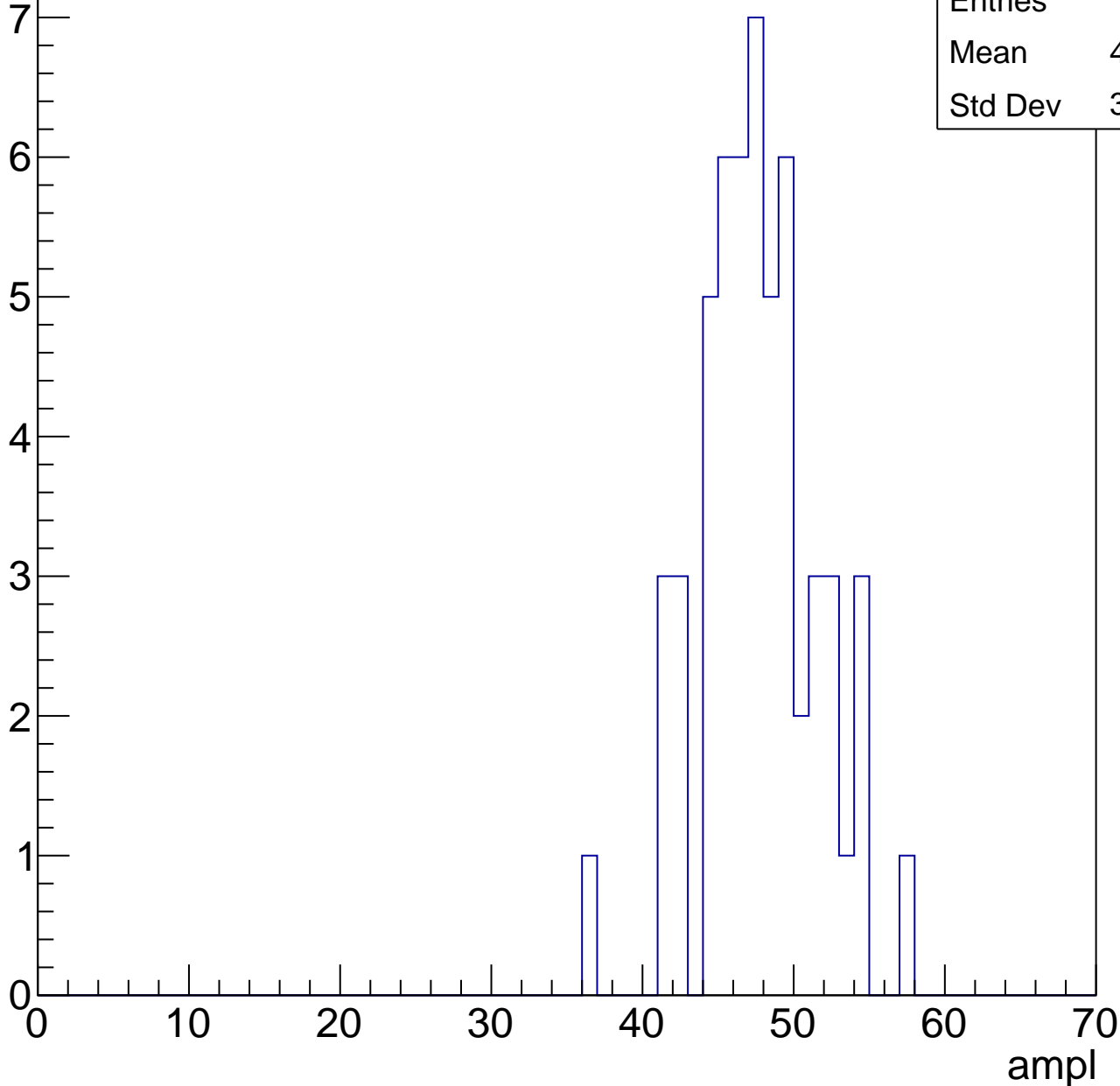


# B1L103S, U21-ch97, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	47.18
Std Dev	3.885

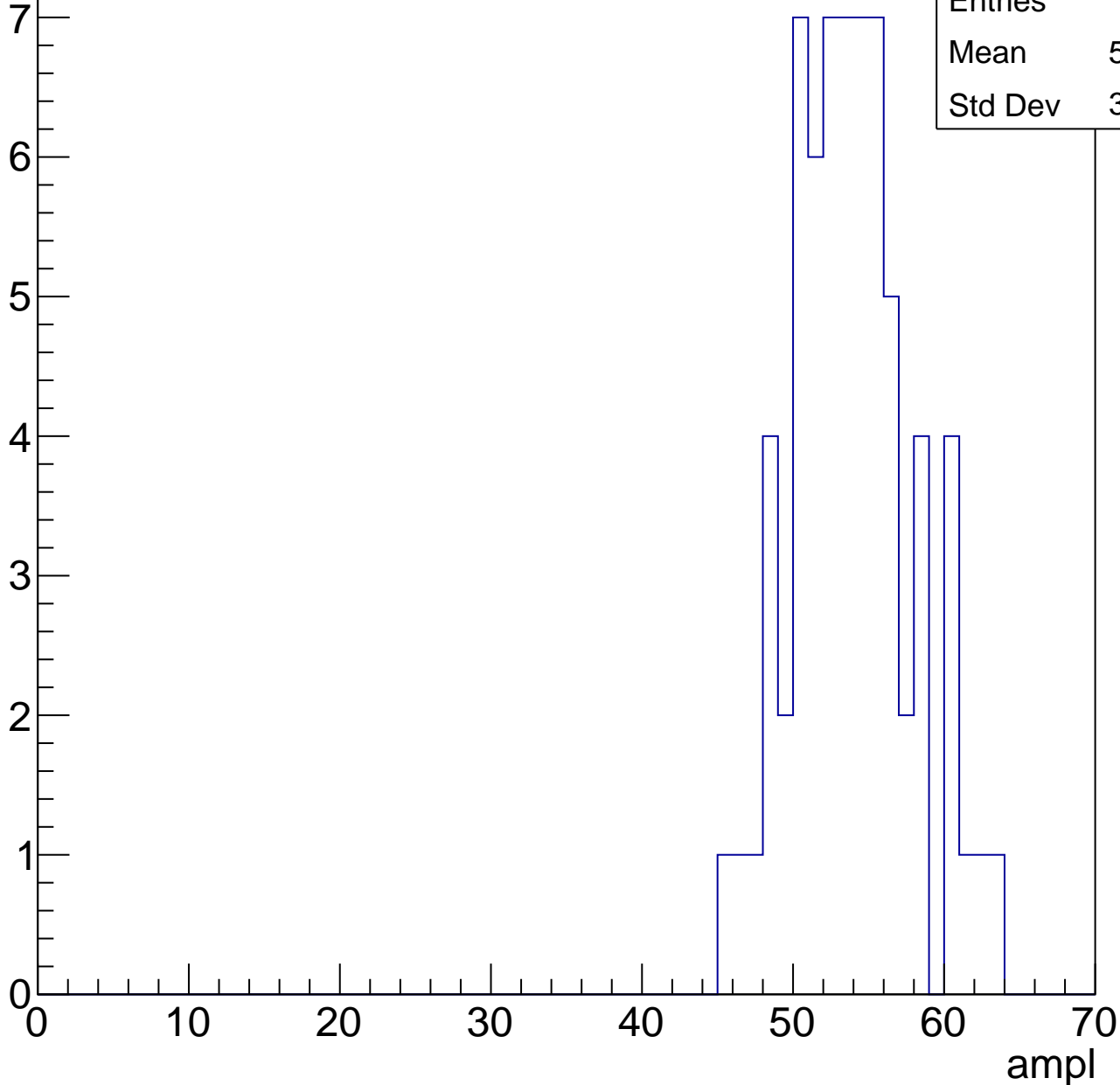


# B1L103S, U21-ch97, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	53.44
Std Dev	3.863

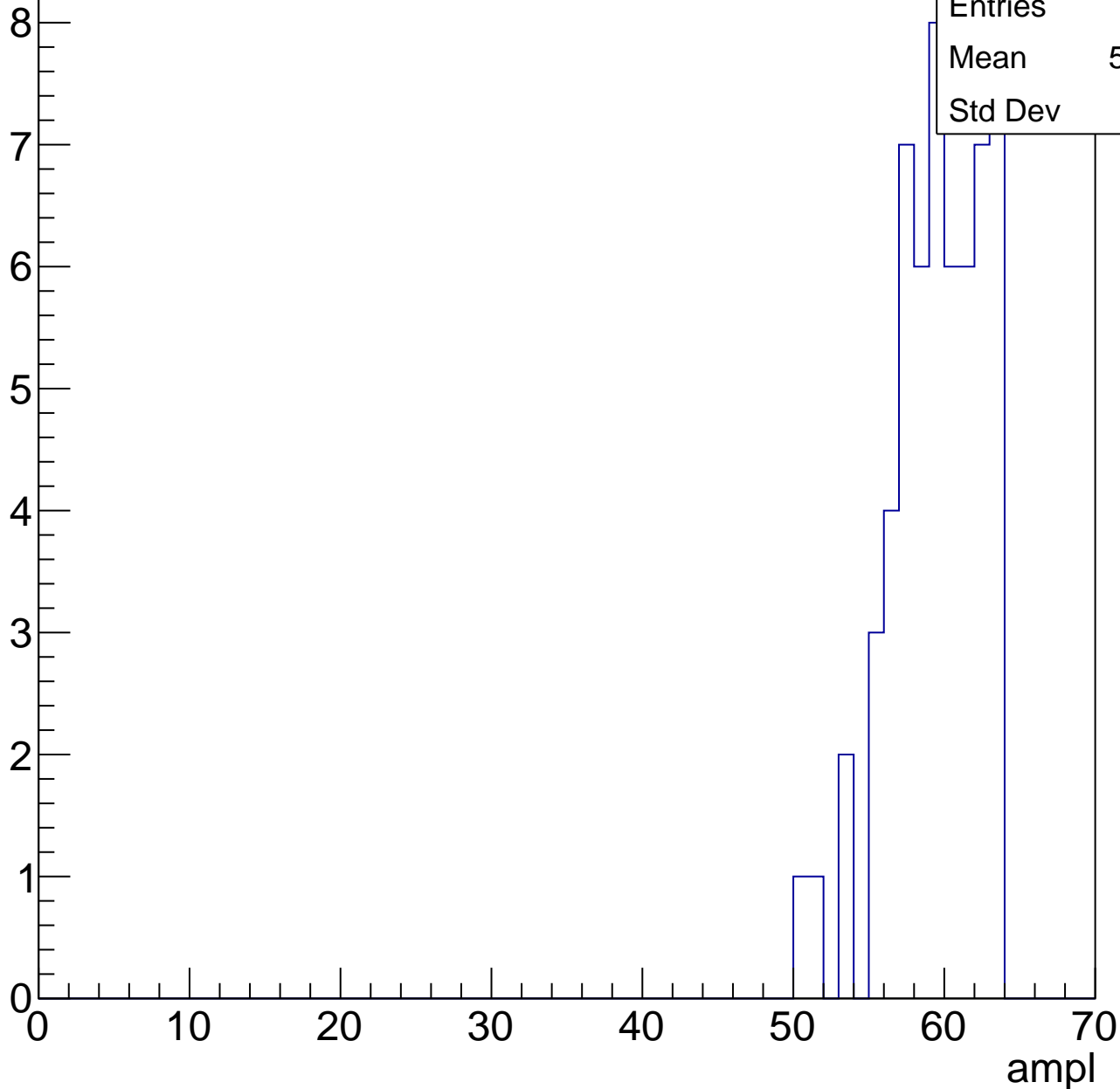


# B1L103S, U21-ch97, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	58.97
Std Dev	3.07



# B1L103S, U21-ch97, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

3

2.5

2

1.5

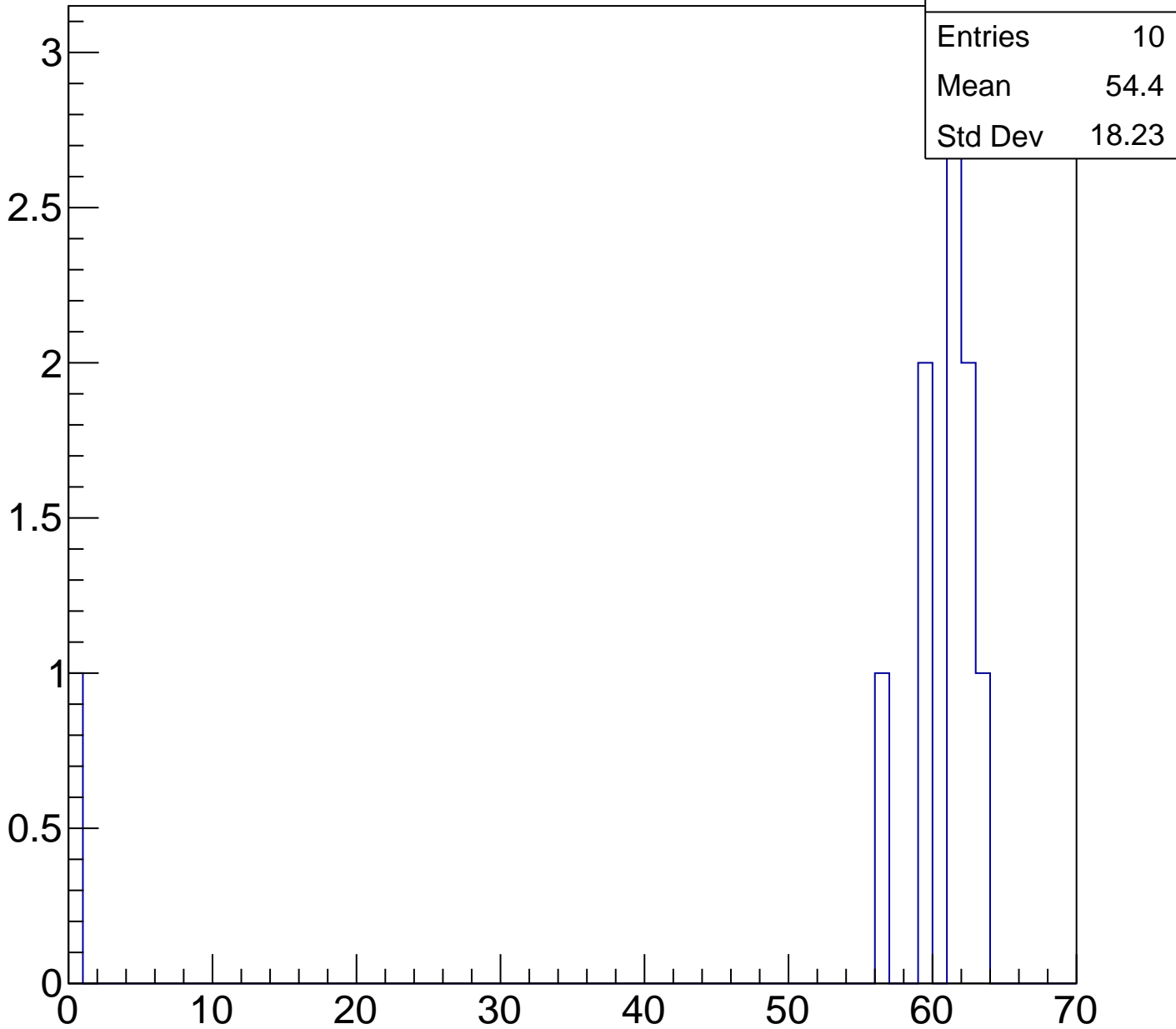
1

0.5

0

ampl

Entries	10
Mean	54.4
Std Dev	18.23





# B1L103S, U21-ch97, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	10
Std Dev	10

# B1L103S, U21-ch98, adc0

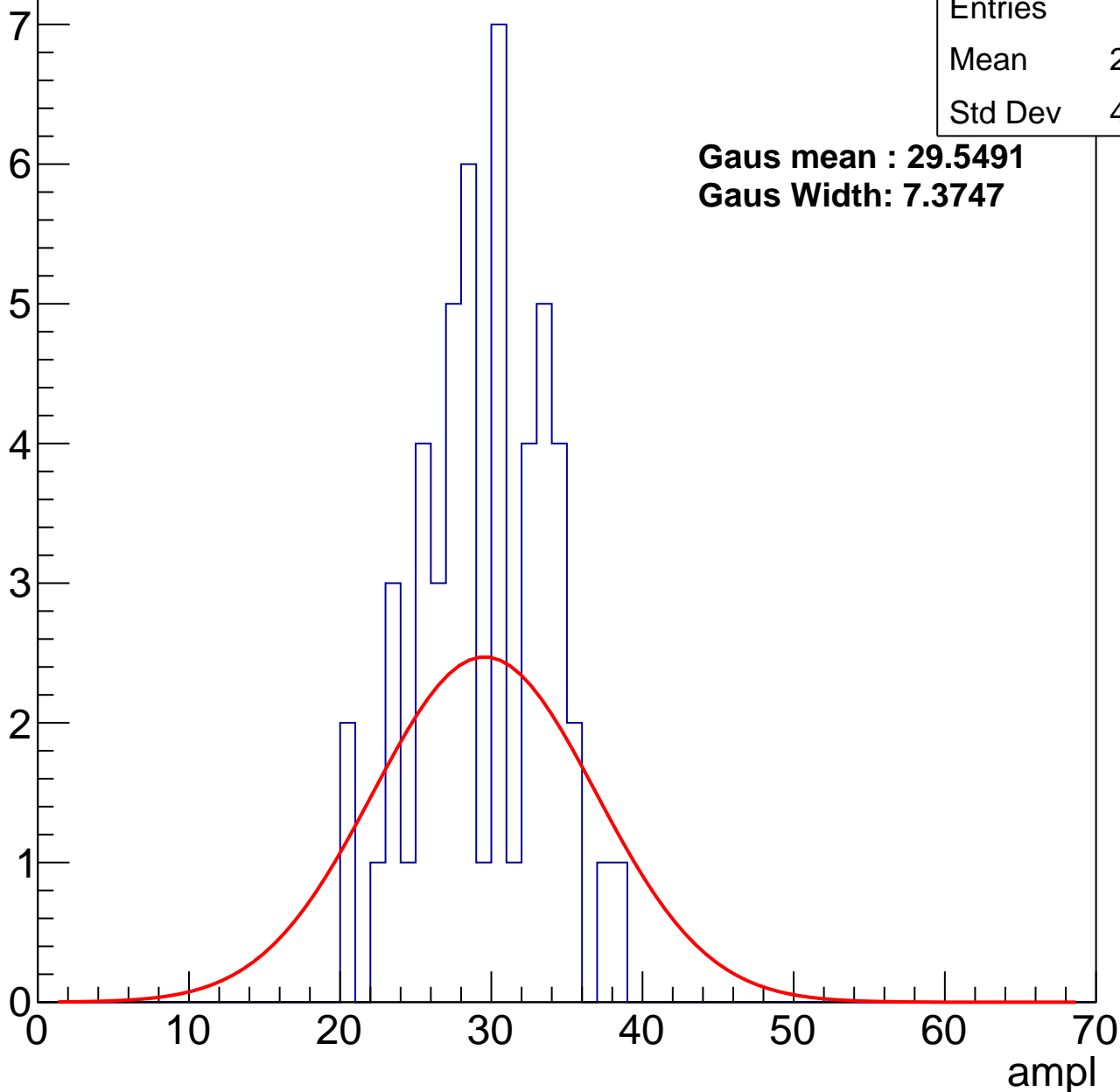
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	29.02
Std Dev	4.212

**Gaus mean : 29.5491**

**Gaus Width: 7.3747**



# B1L103S, U21-ch98, adc1

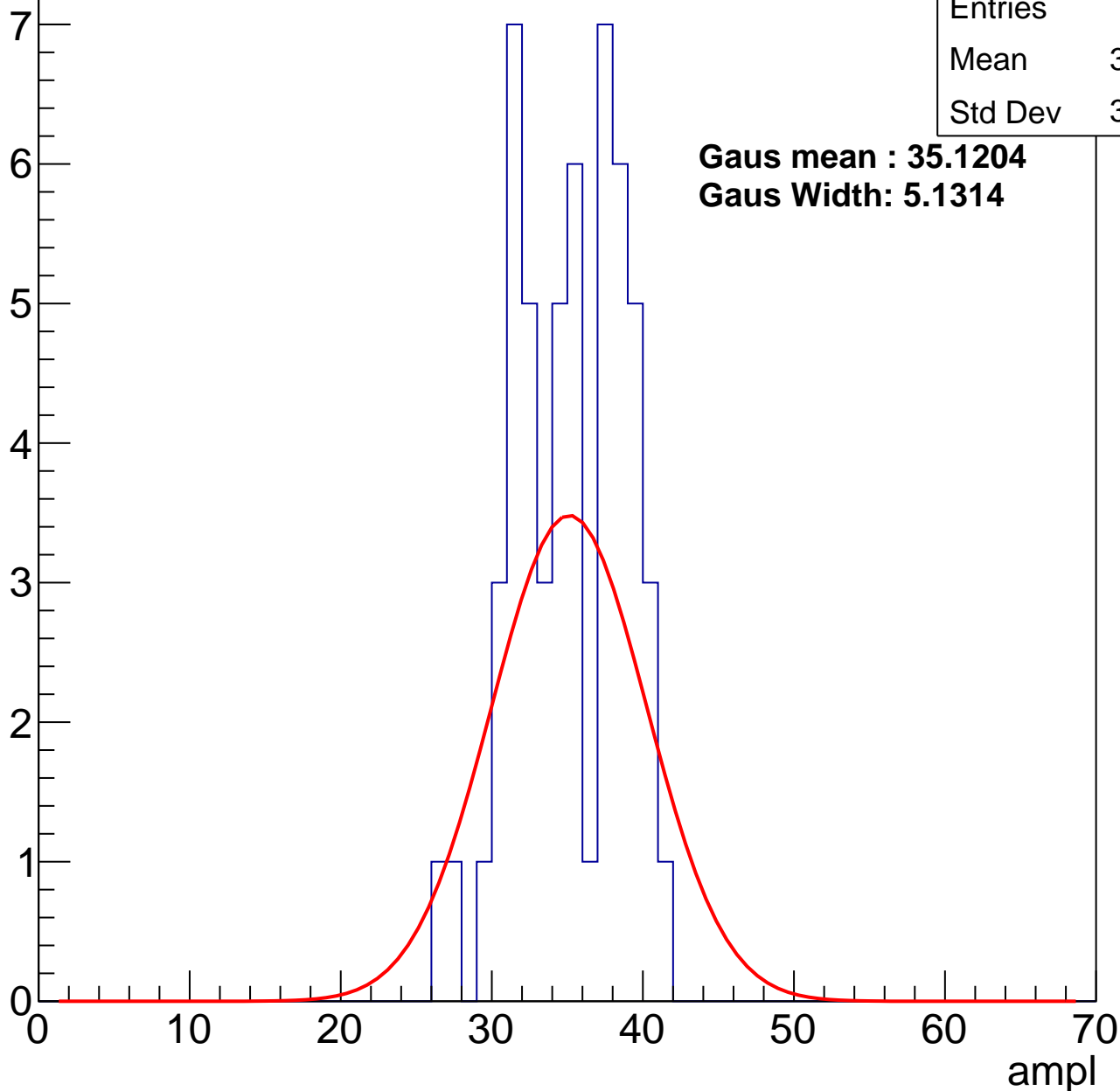
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	34.67
Std Dev	3.563

**Gaus mean : 35.1204**

**Gaus Width: 5.1314**



# B1L103S, U21-ch98, adc2

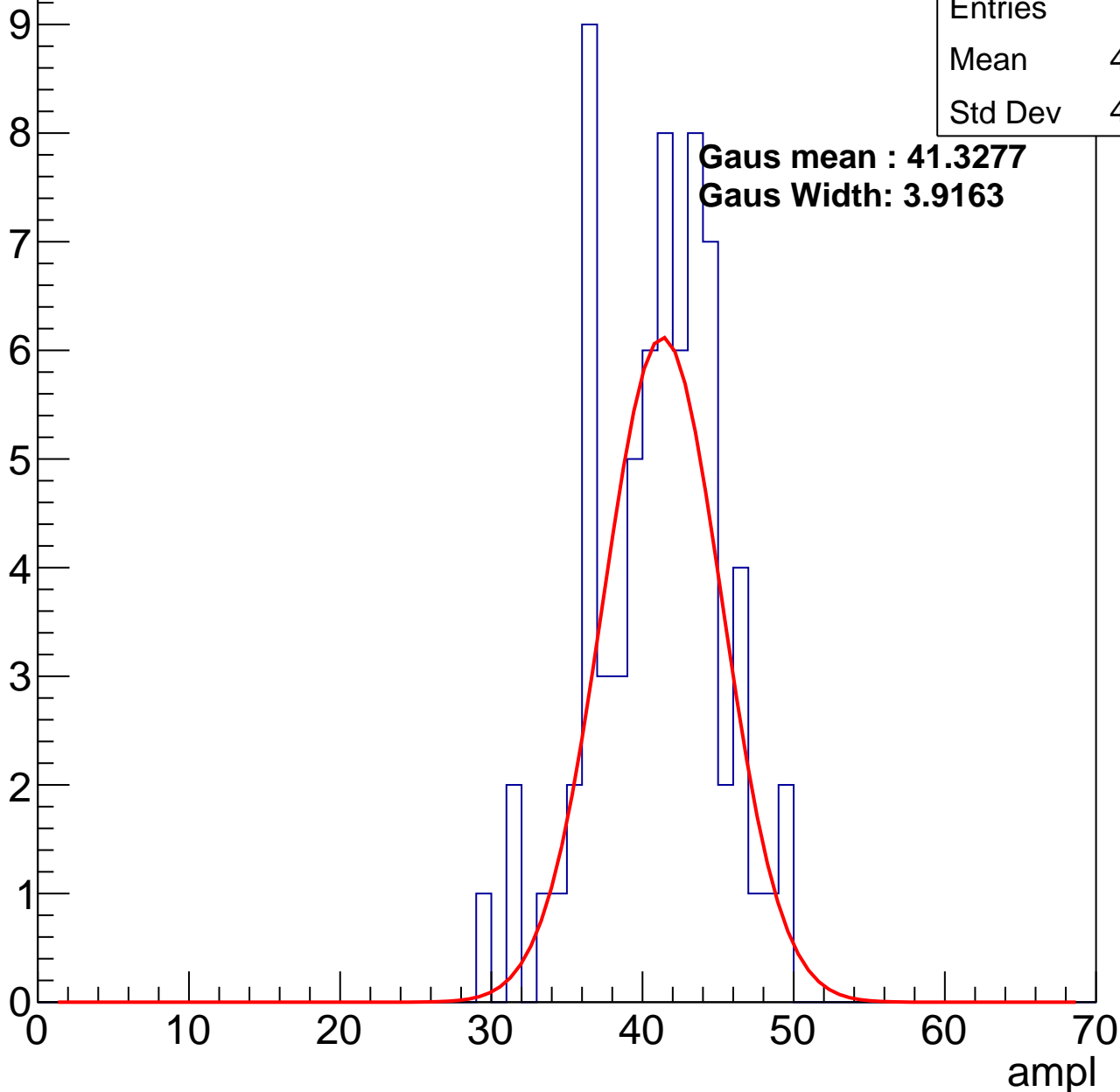
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	40.43
Std Dev	4.213

**Gaus mean : 41.3277**

**Gaus Width: 3.9163**

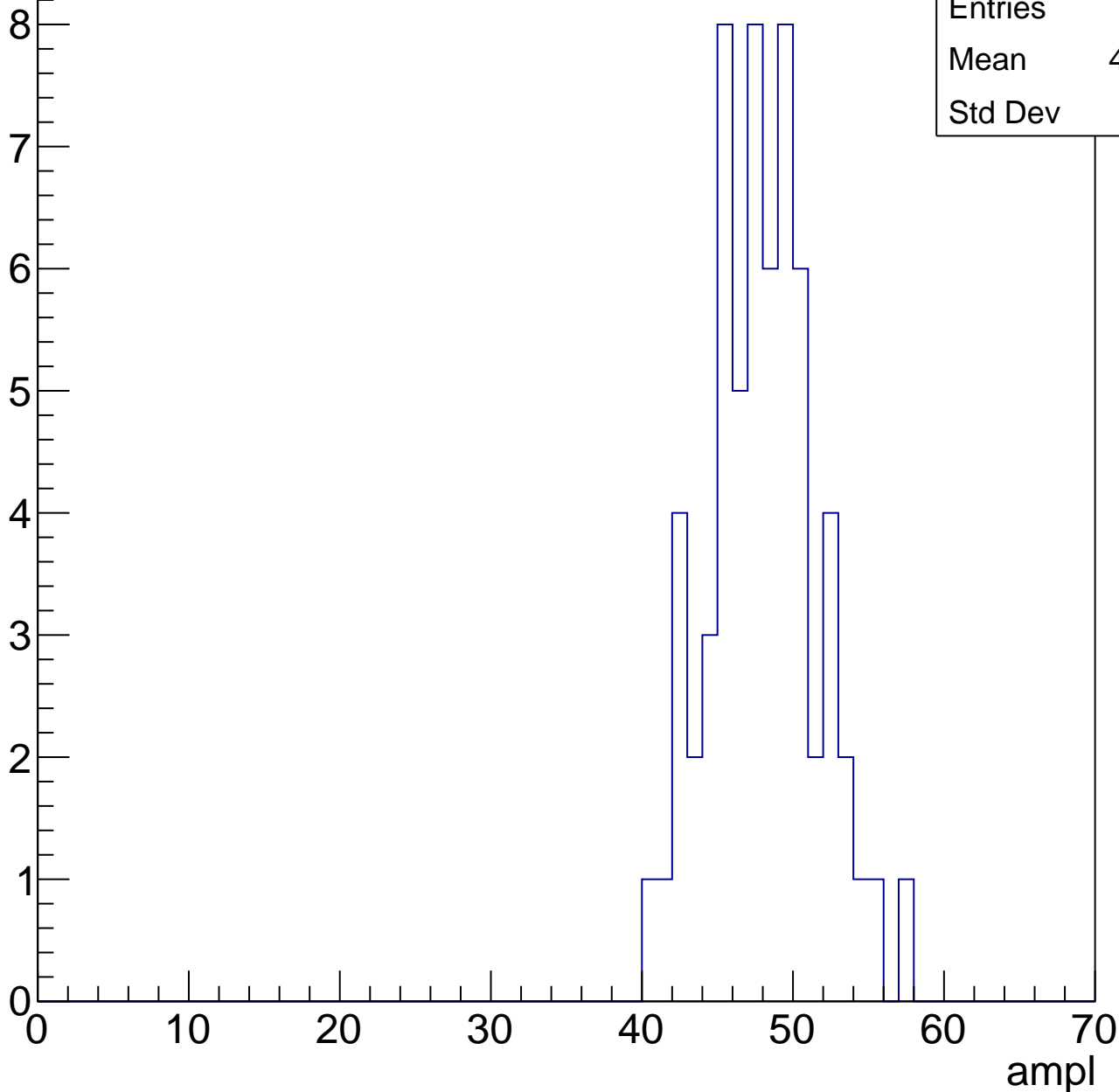


# B1L103S, U21-ch98, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	47.54
Std Dev	3.5

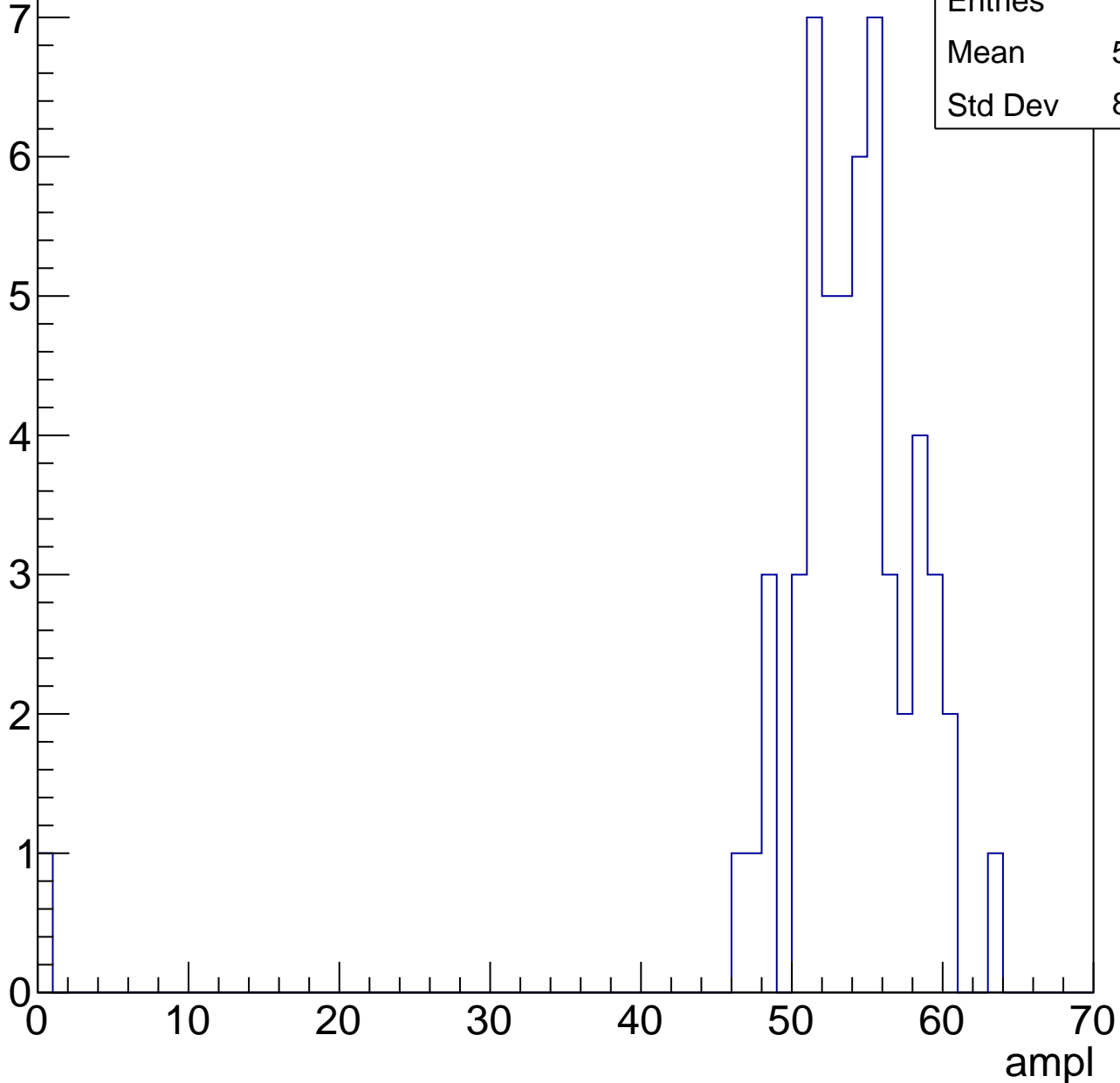


# B1L103S, U21-ch98, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	52.81
Std Dev	8.081

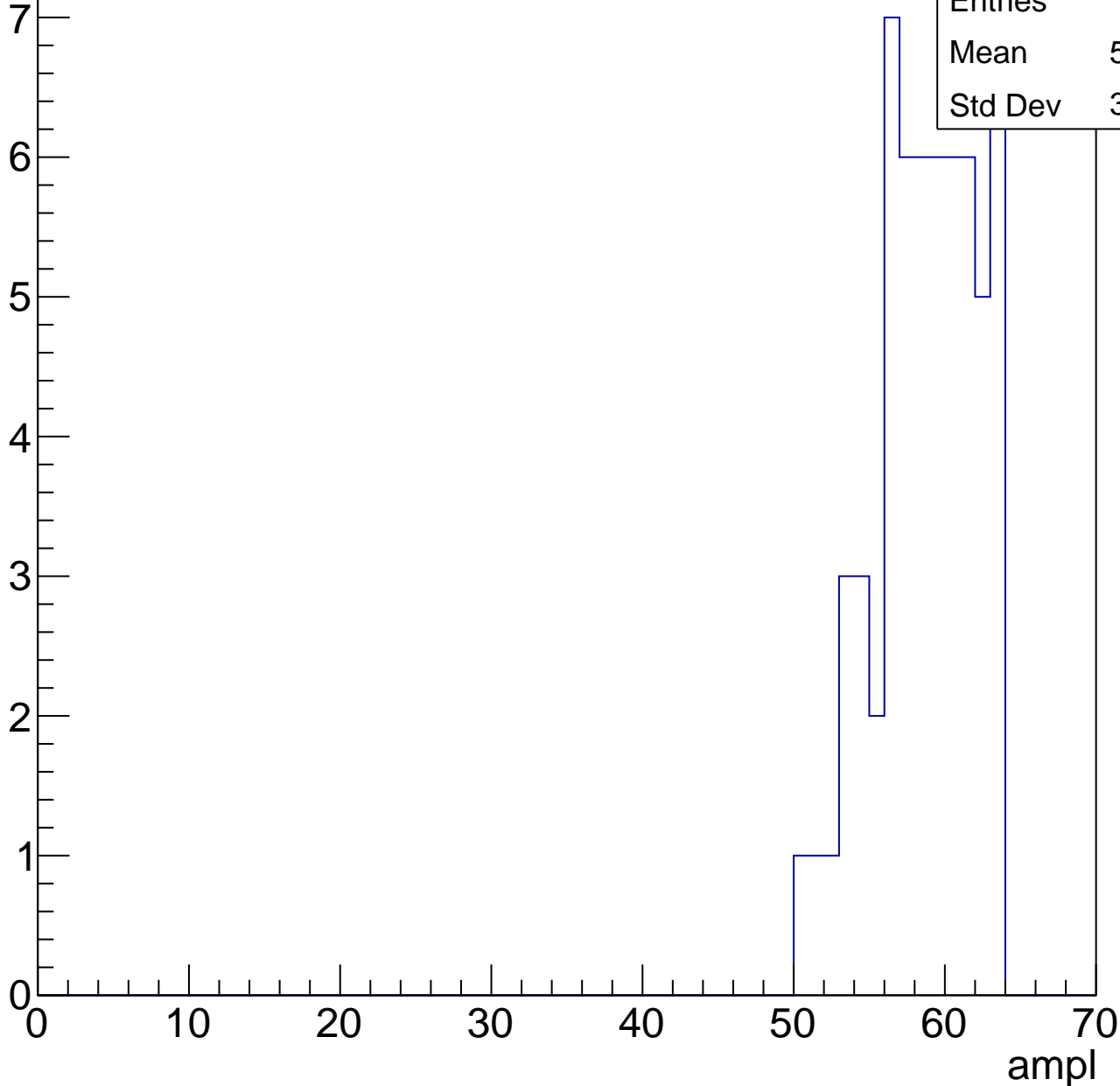


# B1L103S, U21-ch98, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	58.28
Std Dev	3.312

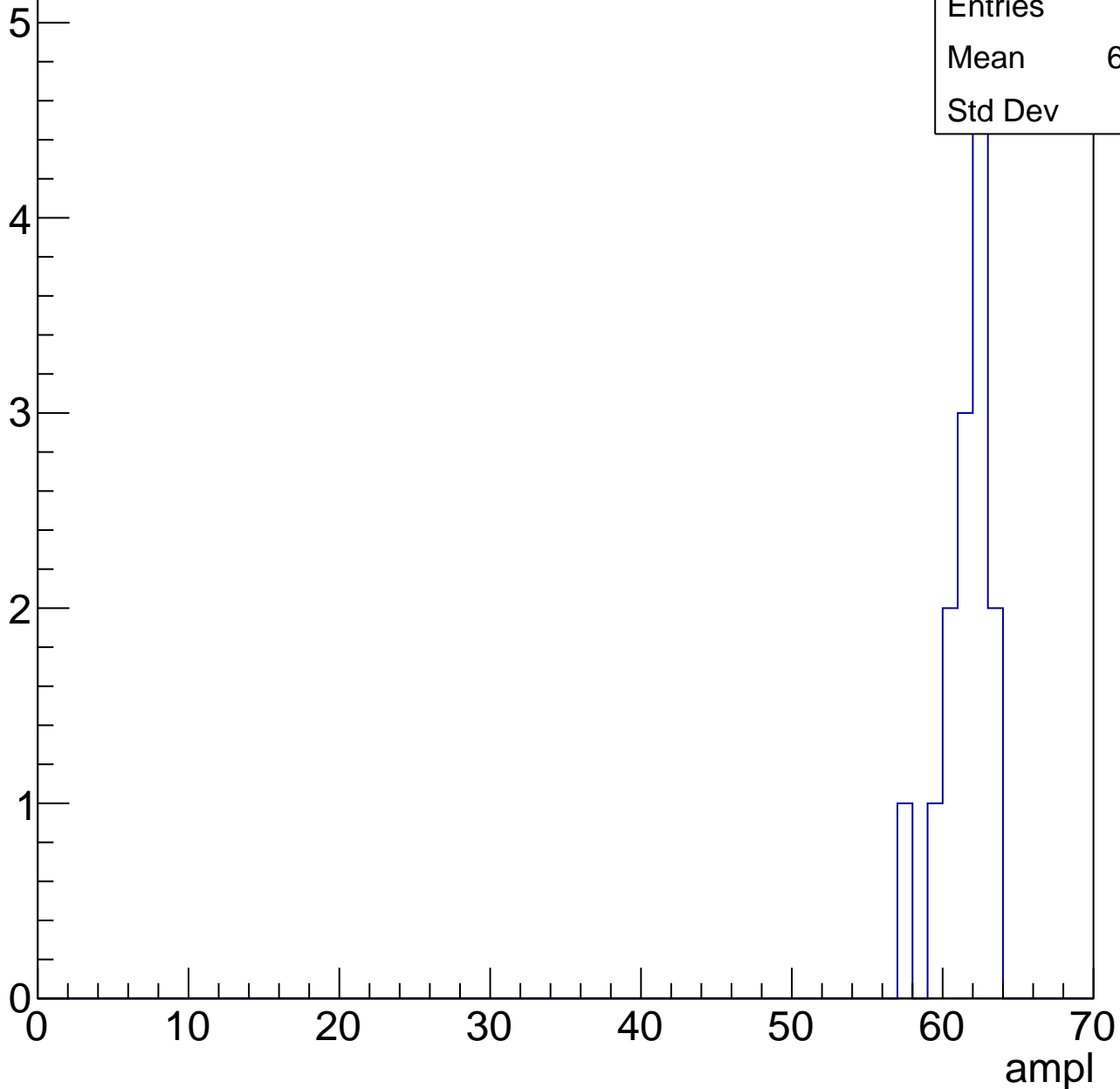


# B1L103S, U21-ch98, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	14
Mean	61.07
Std Dev	1.58





# B1L103S, U21-ch98, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U21-ch99, adc0

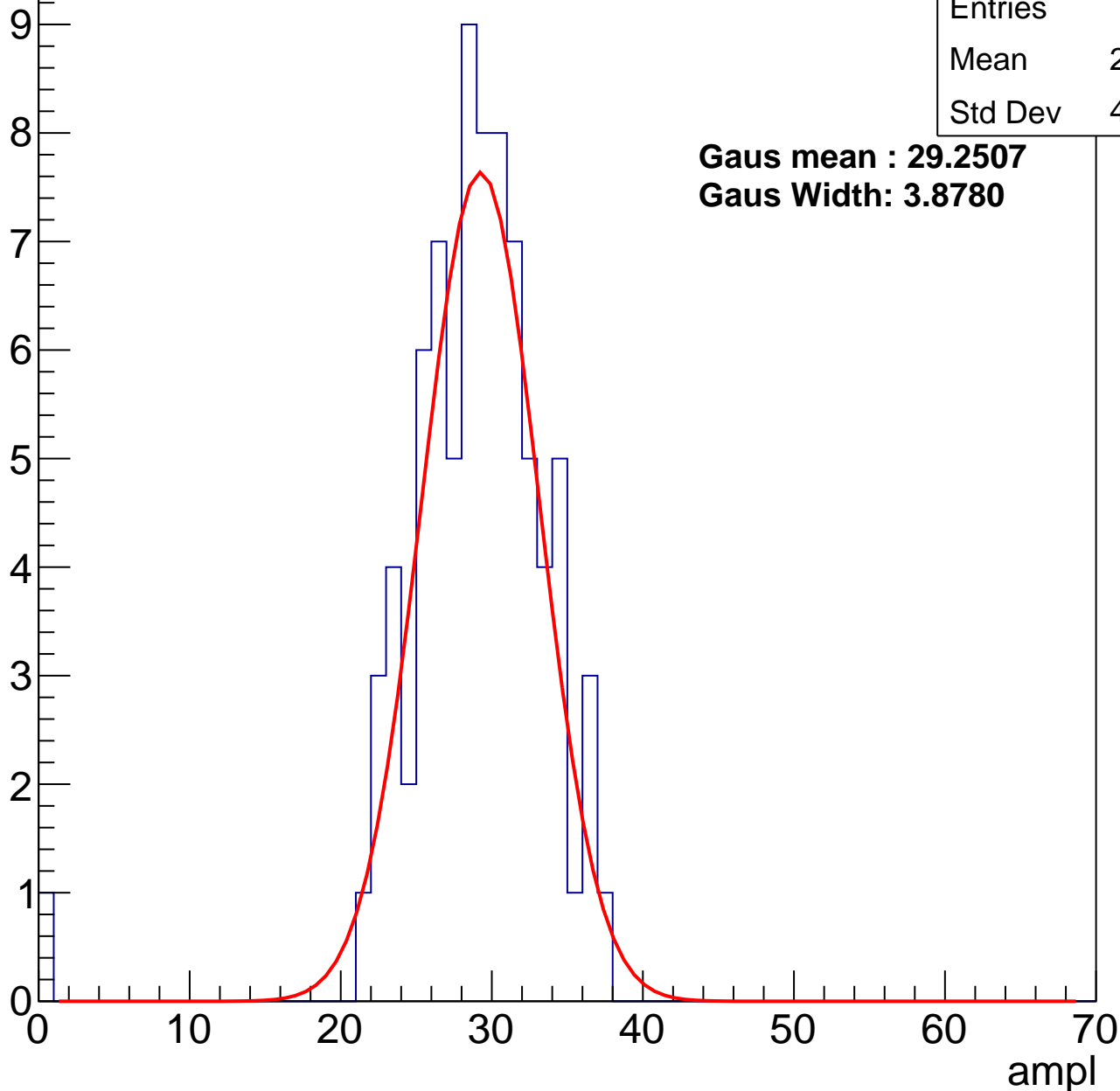
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	80
Mean	28.46
Std Dev	4.909

**Gaus mean : 29.2507**

**Gaus Width: 3.8780**



# B1L103S, U21-ch99, adc1

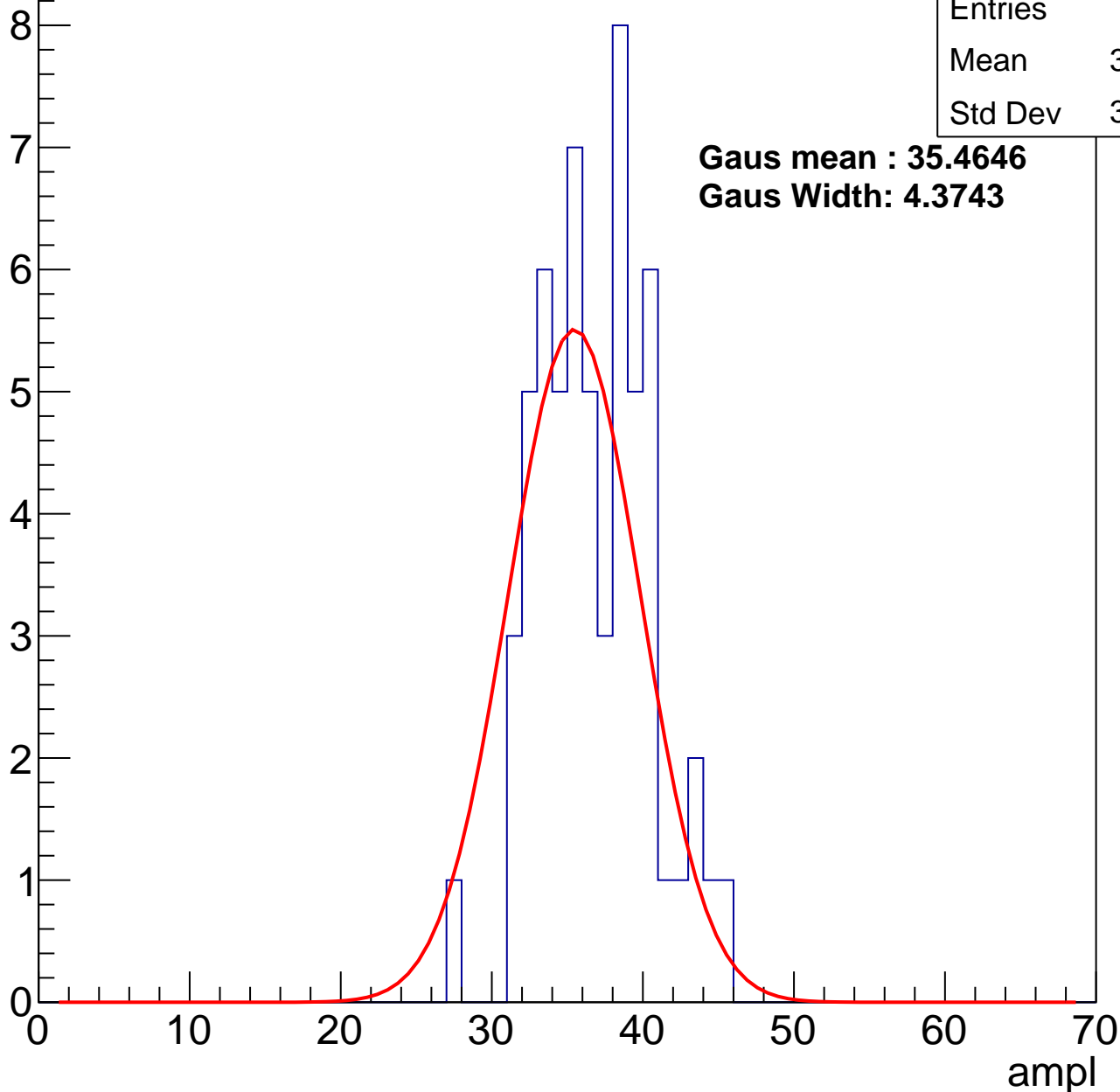
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	36.35
Std Dev	3.628

**Gaus mean : 35.4646**

**Gaus Width: 4.3743**



# B1L103S, U21-ch99, adc2

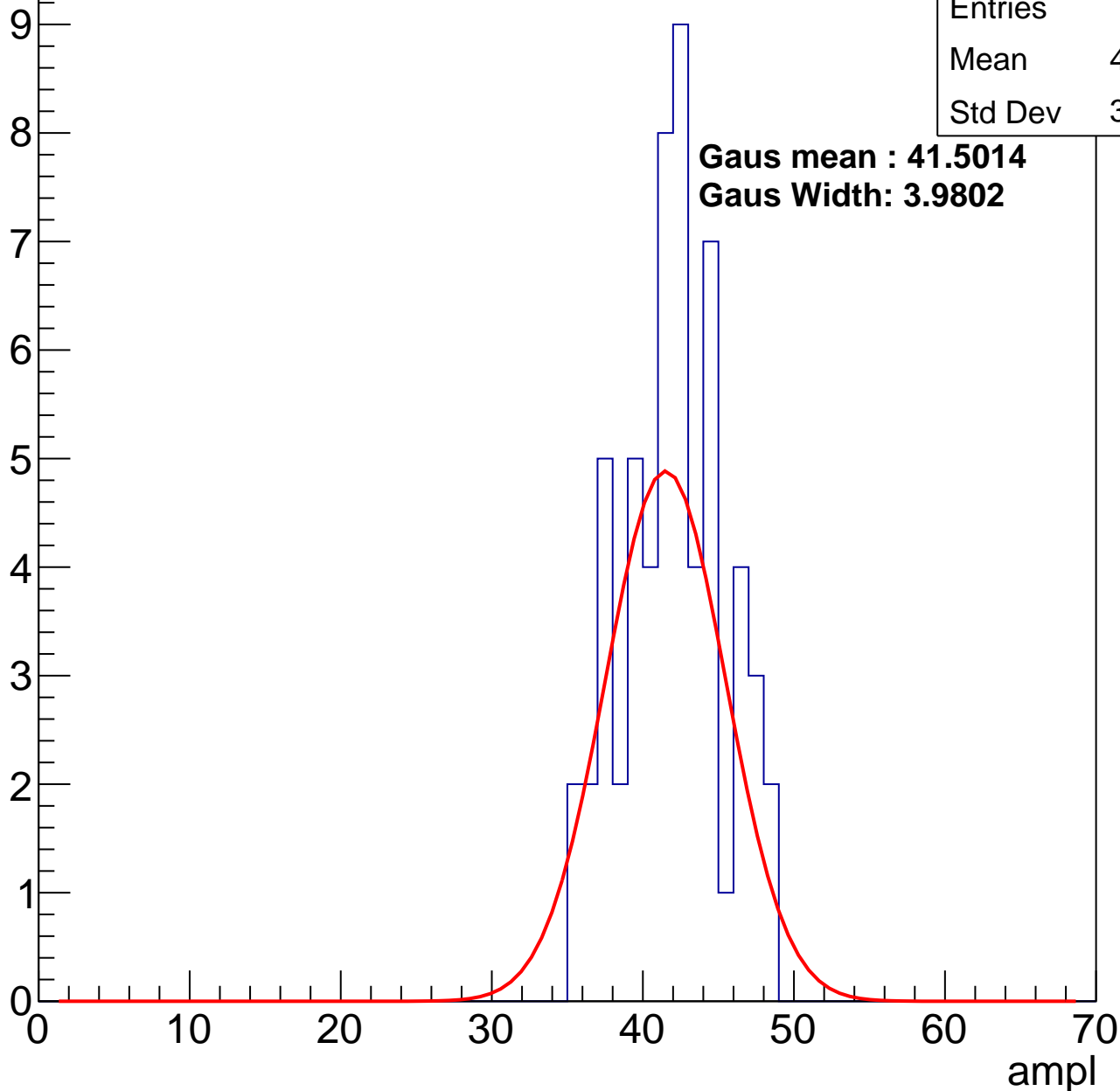
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	41.55
Std Dev	3.312

**Gaus mean : 41.5014**

**Gaus Width: 3.9802**

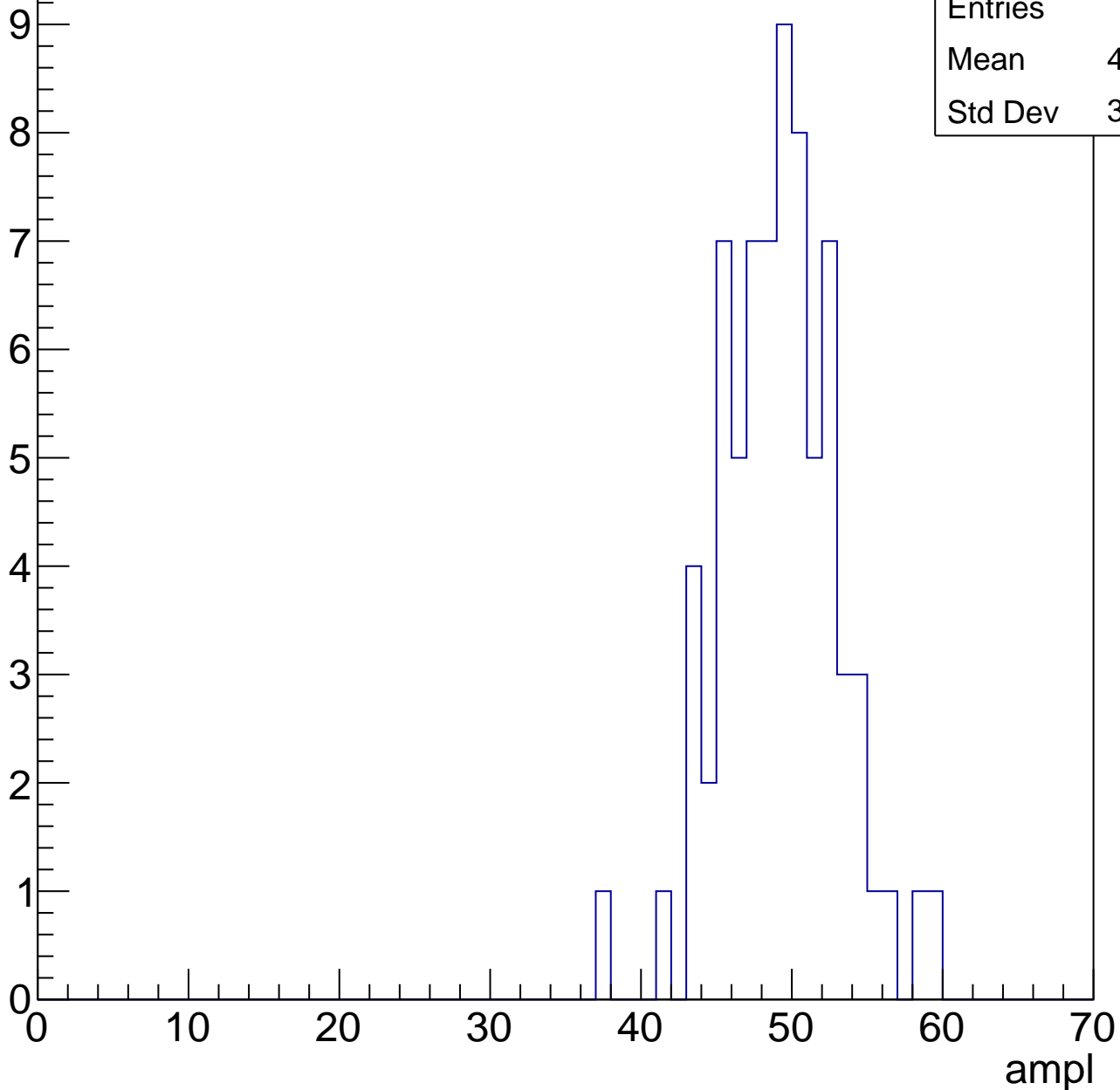


# B1L103S, U21-ch99, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	48.73
Std Dev	3.826

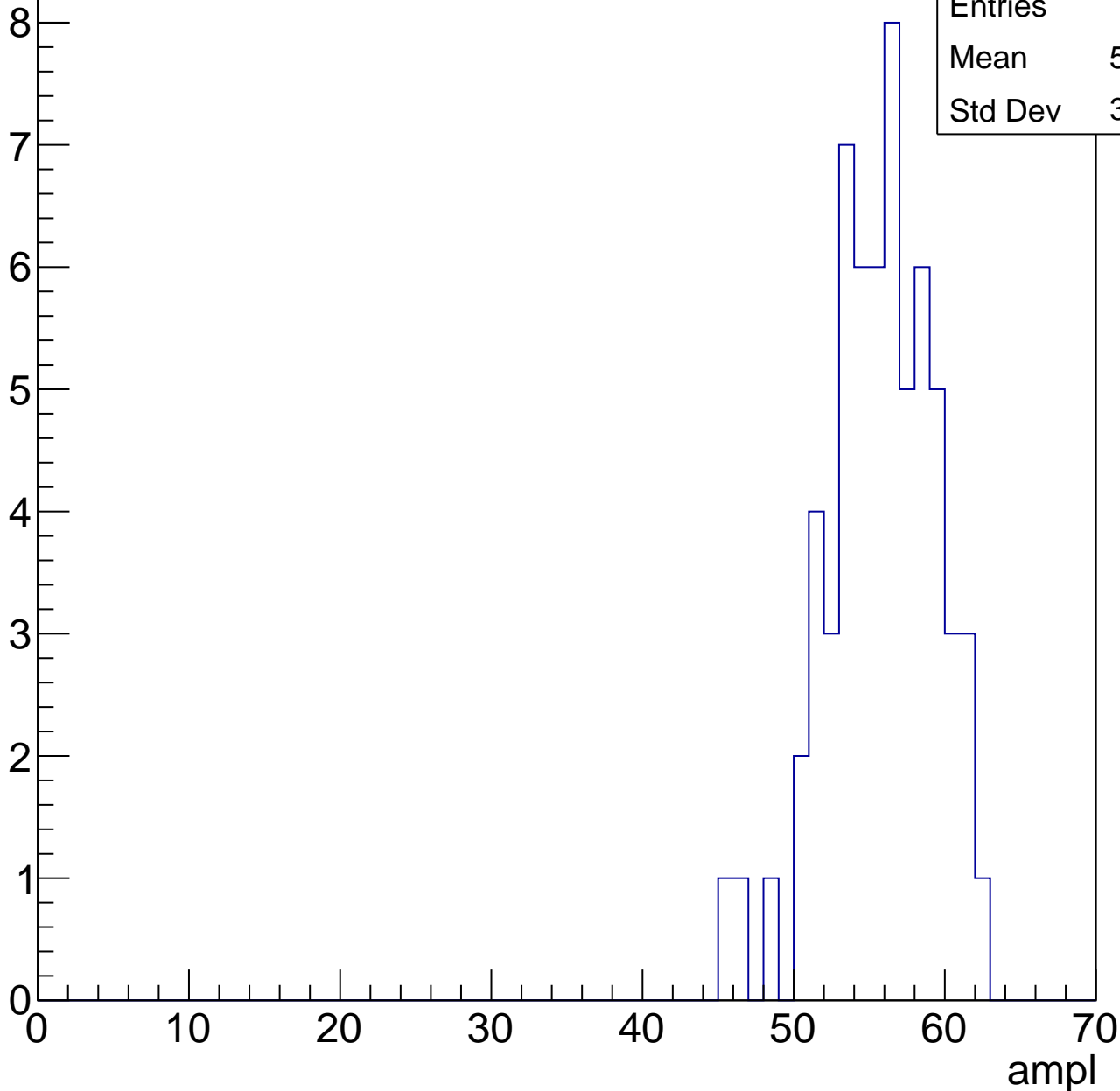


# B1L103S, U21-ch99, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

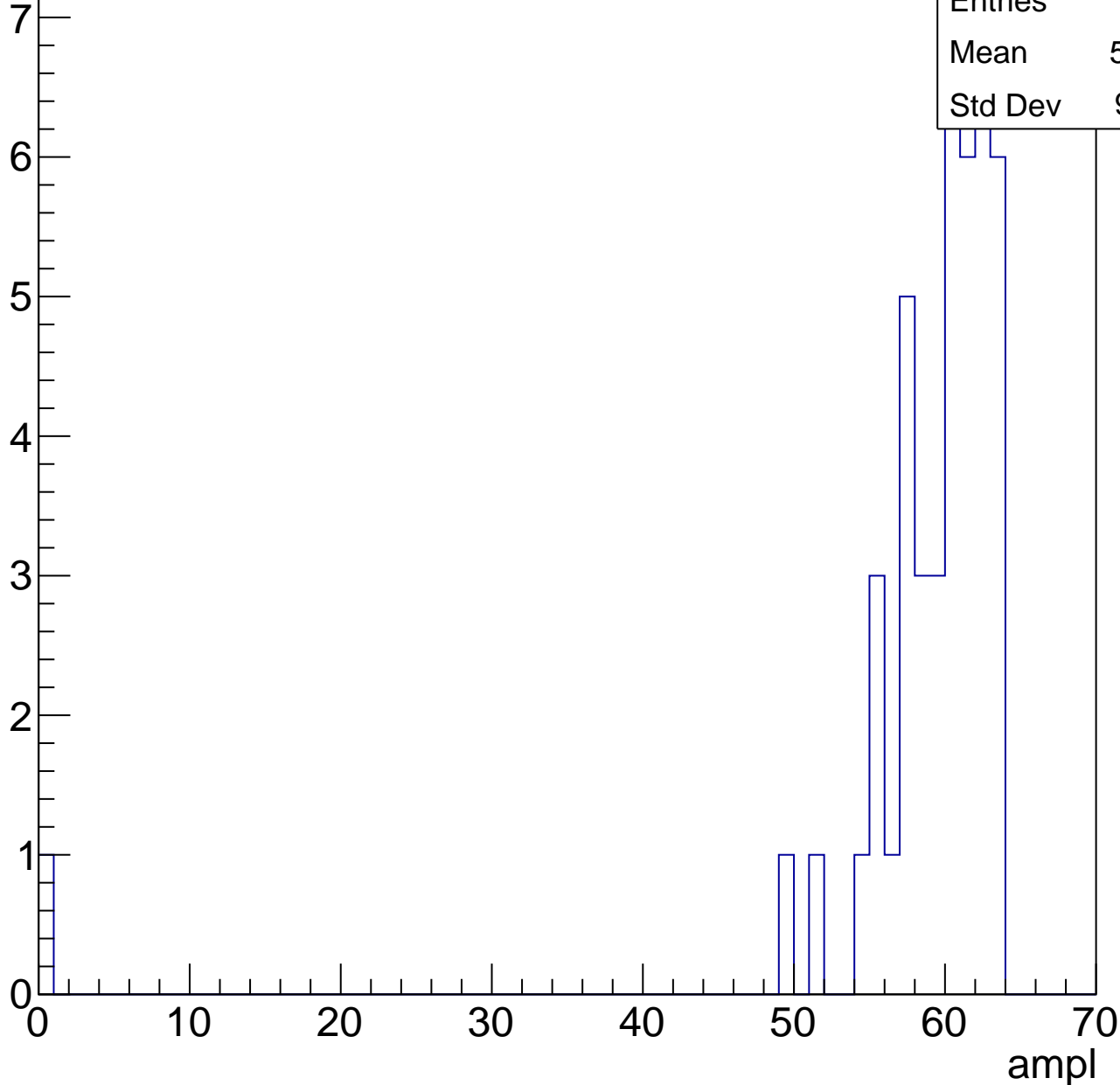
Entries	62
Mean	55.24
Std Dev	3.582



# B1L103S, U21-ch99, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

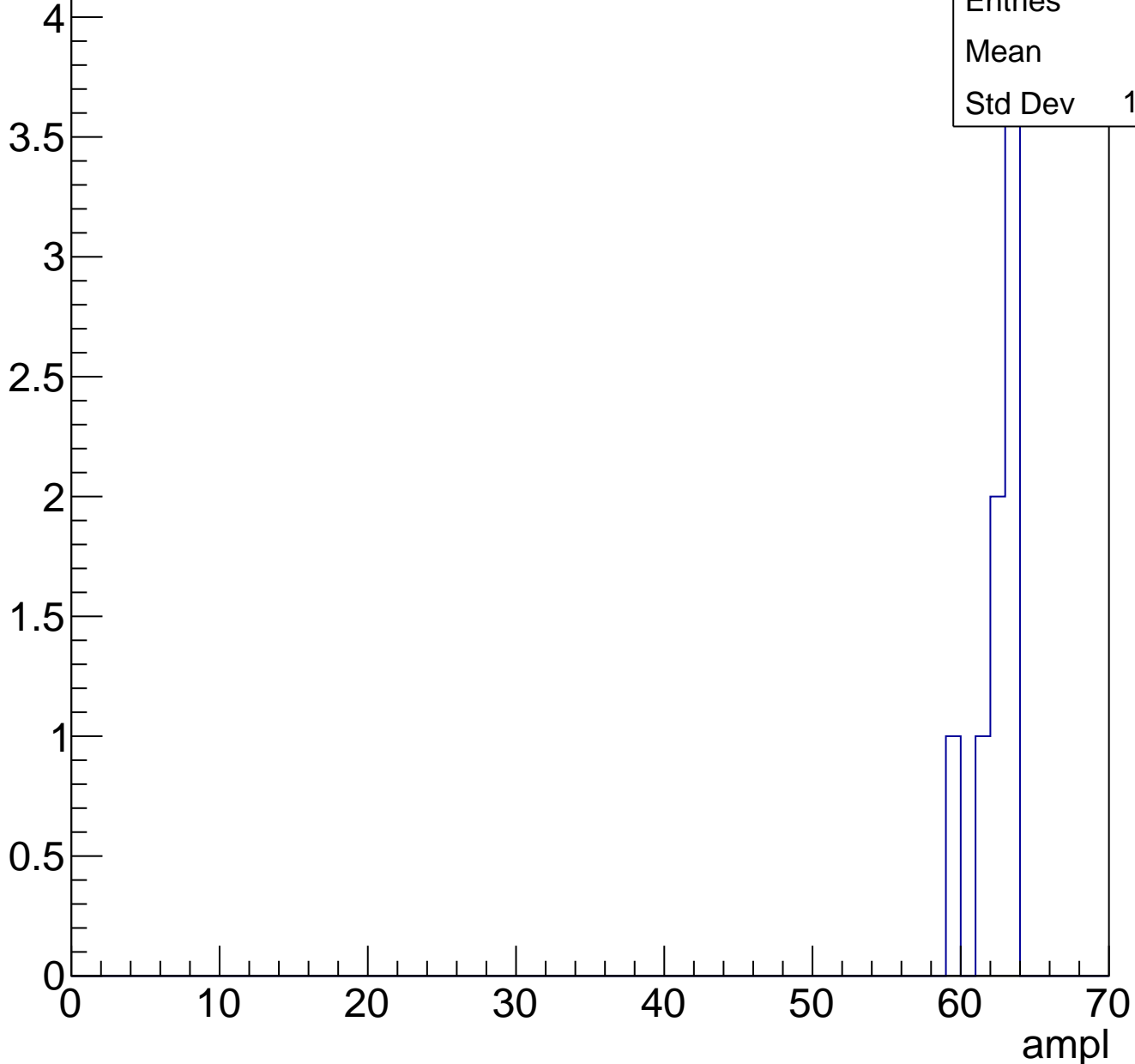
Entry



# B1L103S, U21-ch99, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	8
Mean	62
Std Dev	1.323



# B1L103S, U21-ch99, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U21-ch100, adc0

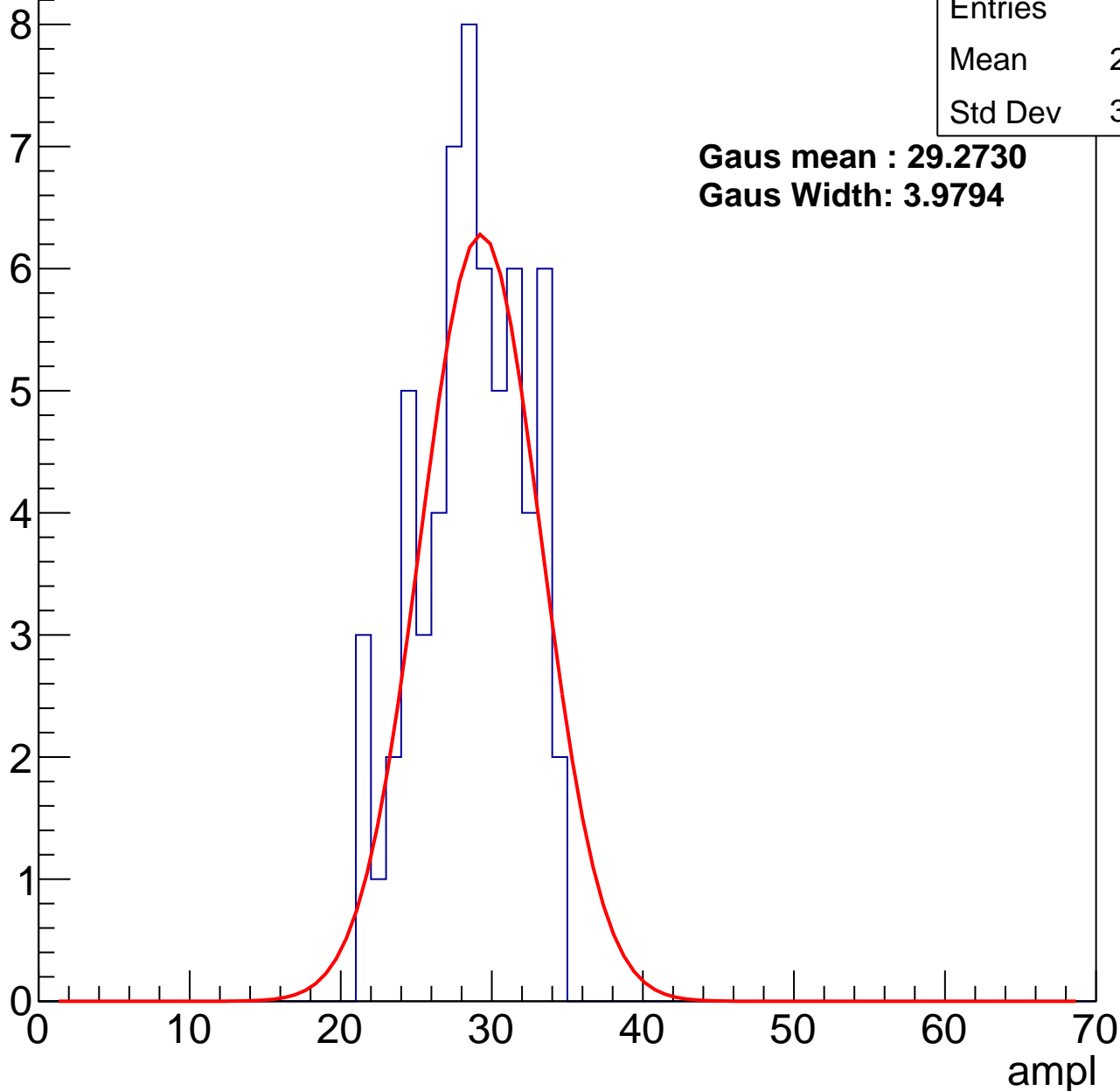
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	28.18
Std Dev	3.424

**Gaus mean : 29.2730**

**Gaus Width: 3.9794**



# B1L103S, U21-ch100, adc1

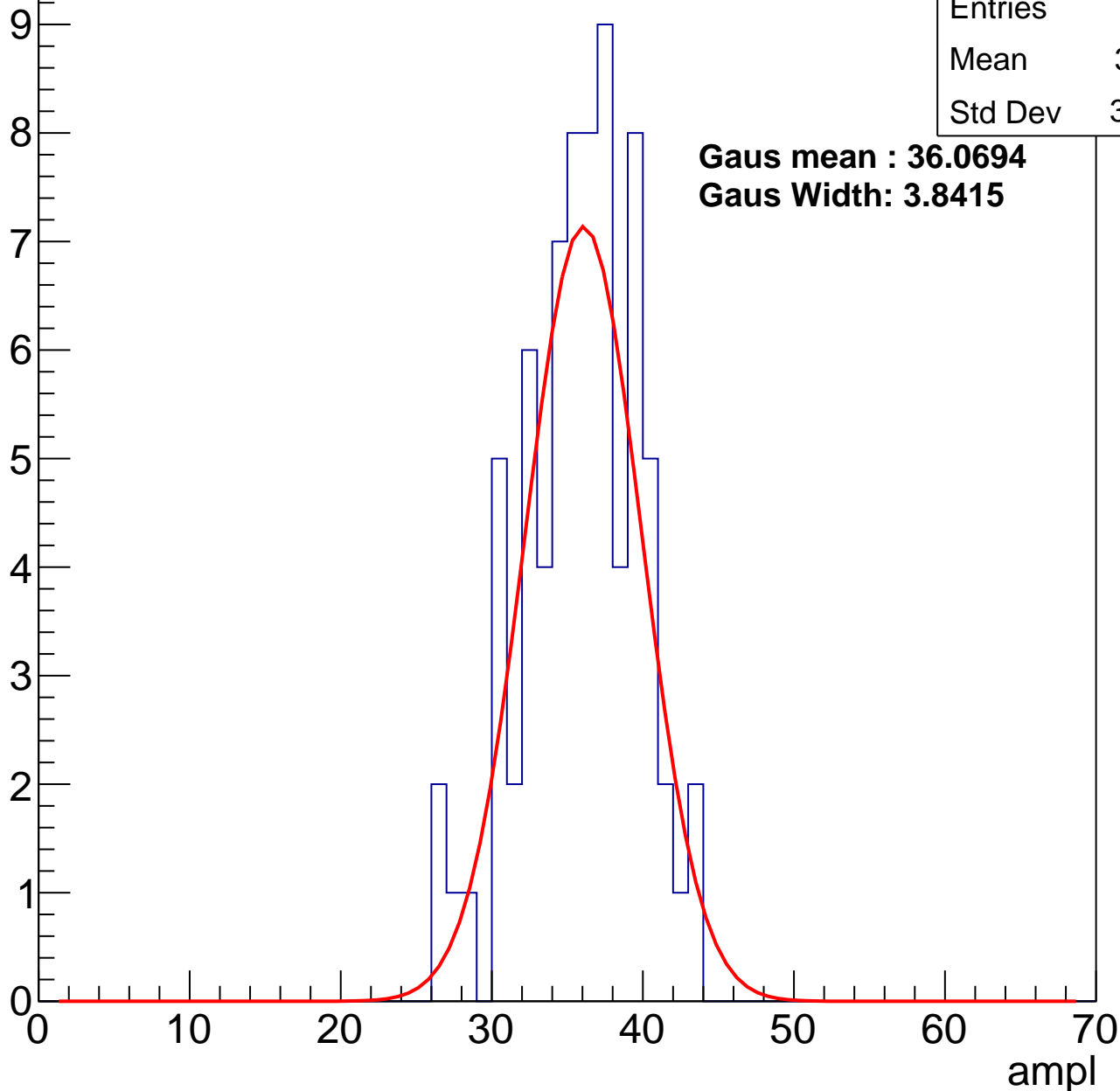
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	35.41
Std Dev	3.792

**Gaus mean : 36.0694**

**Gaus Width: 3.8415**



# B1L103S, U21-ch100, adc2

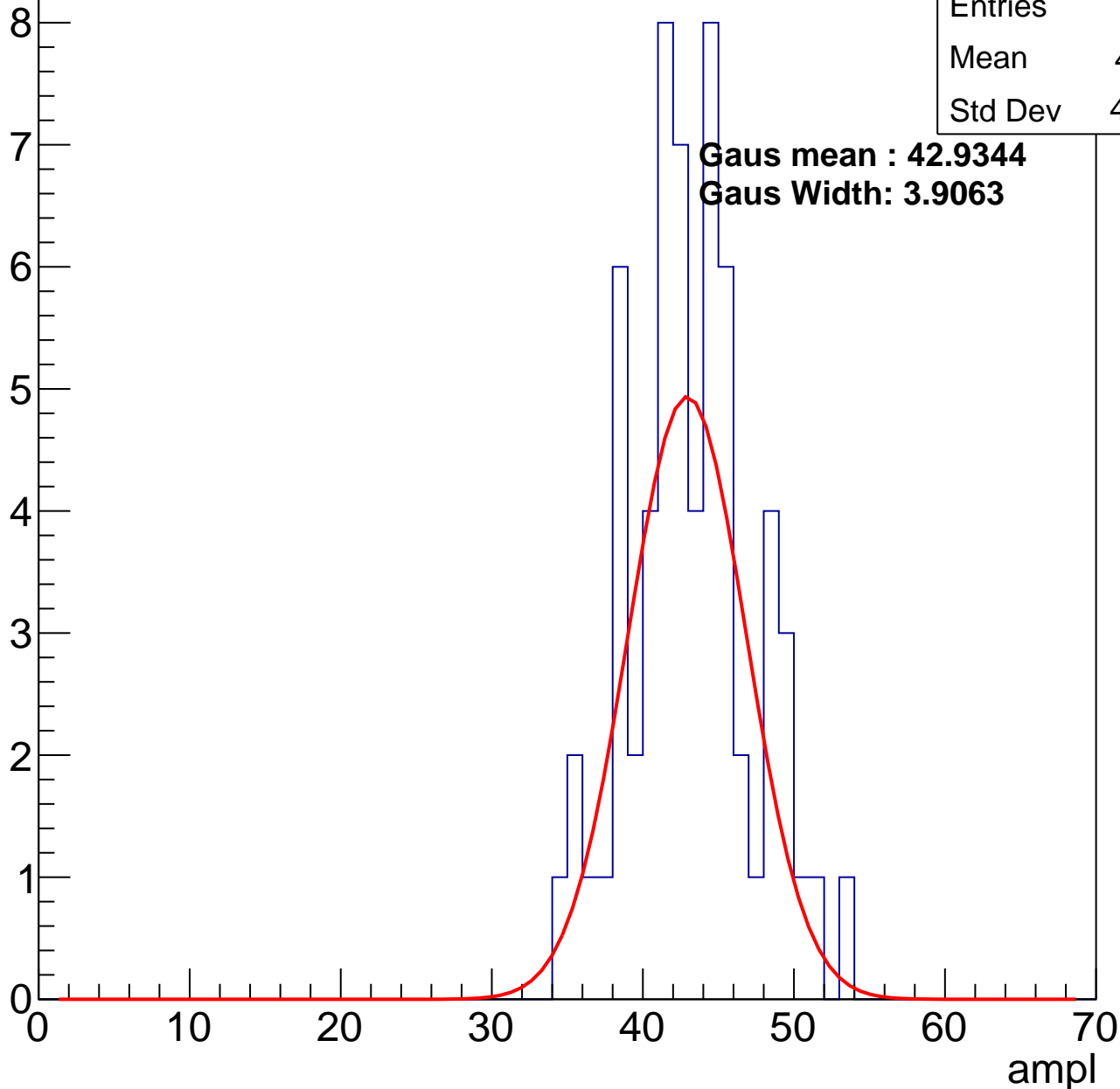
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	42.71
Std Dev	4.049

**Gaus mean : 42.9344**

**Gaus Width: 3.9063**

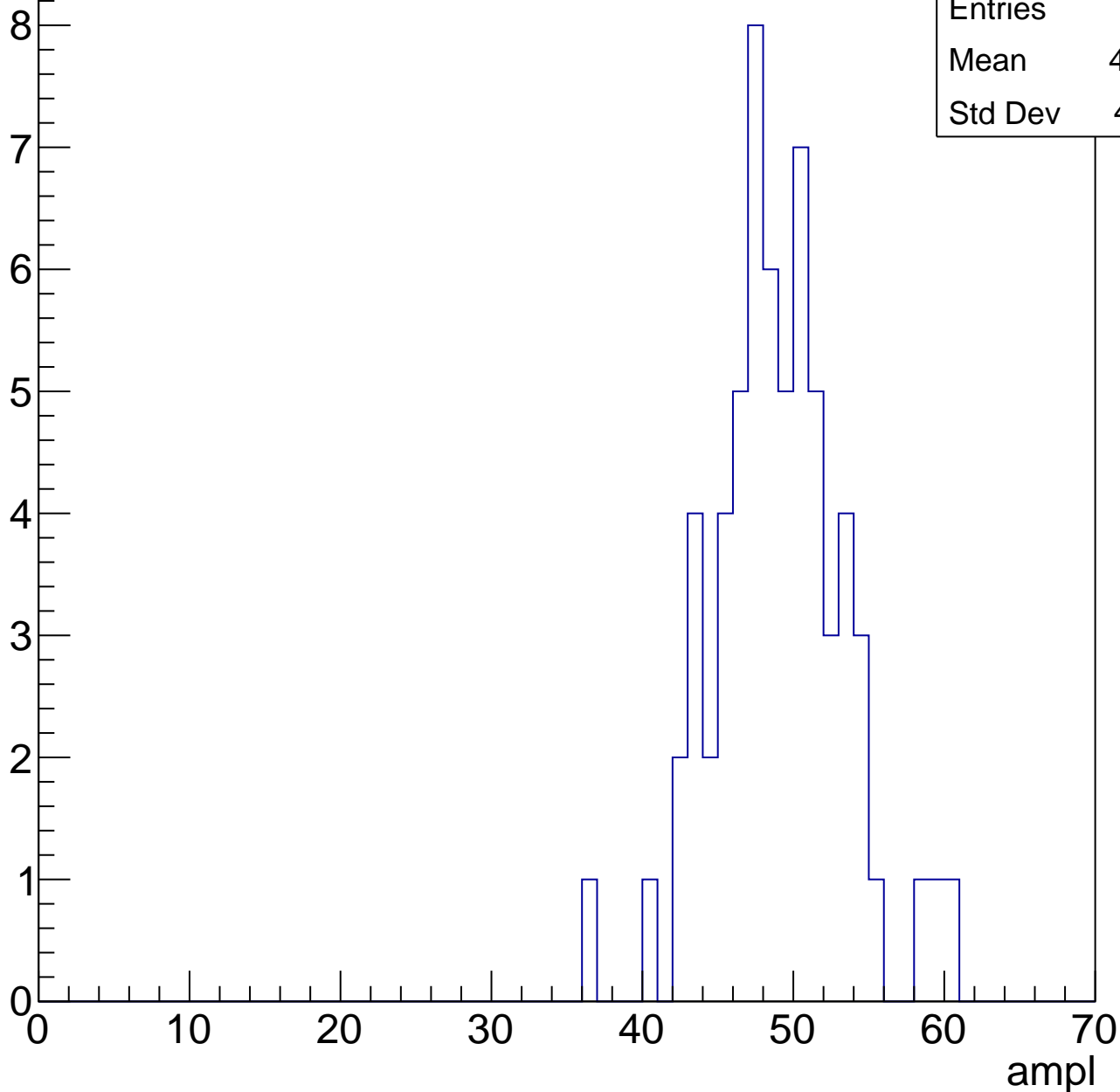


# B1L103S, U21-ch100, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	48.53
Std Dev	4.341

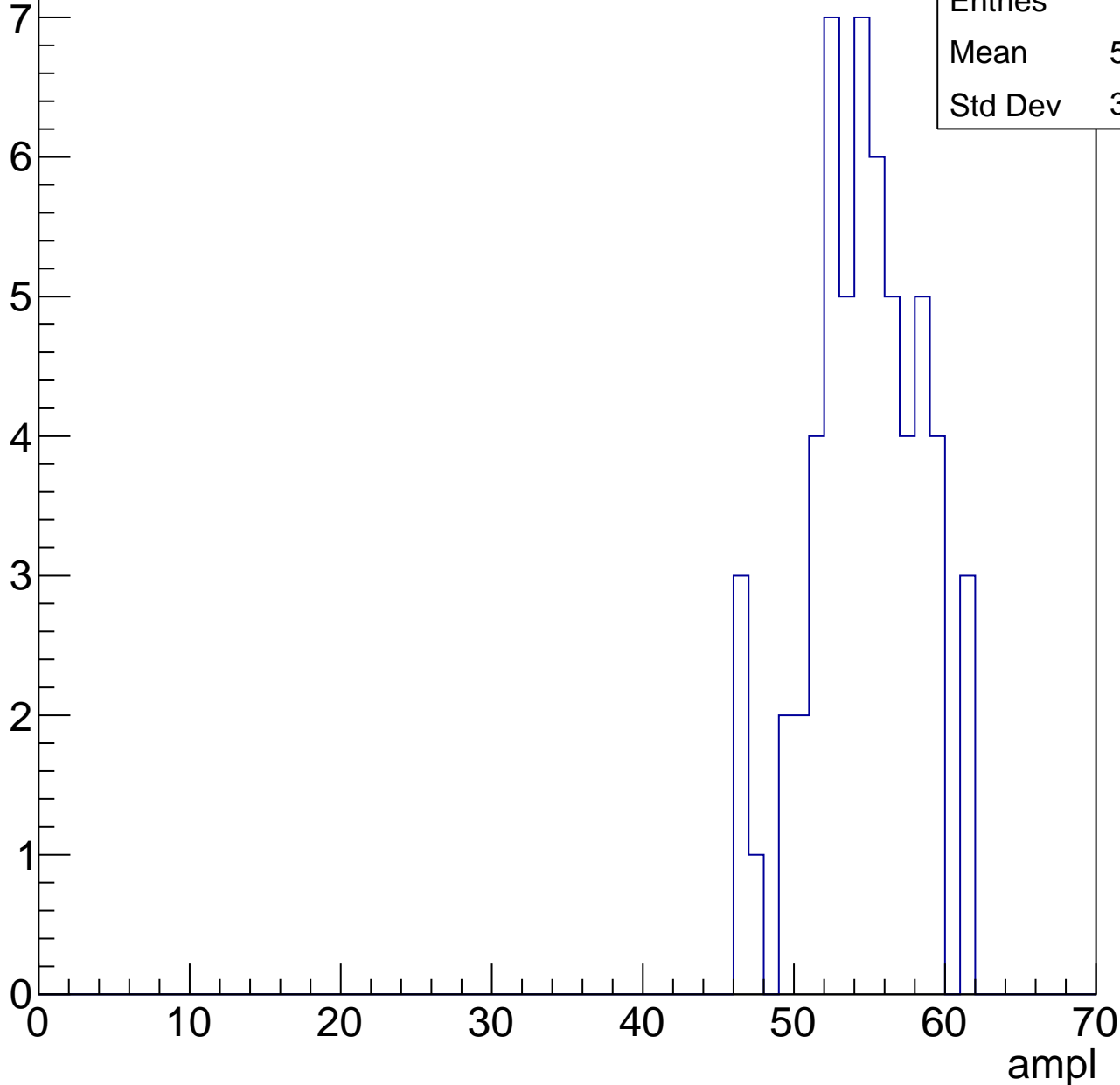


# B1L103S, U21-ch100, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	54.16
Std Dev	3.666

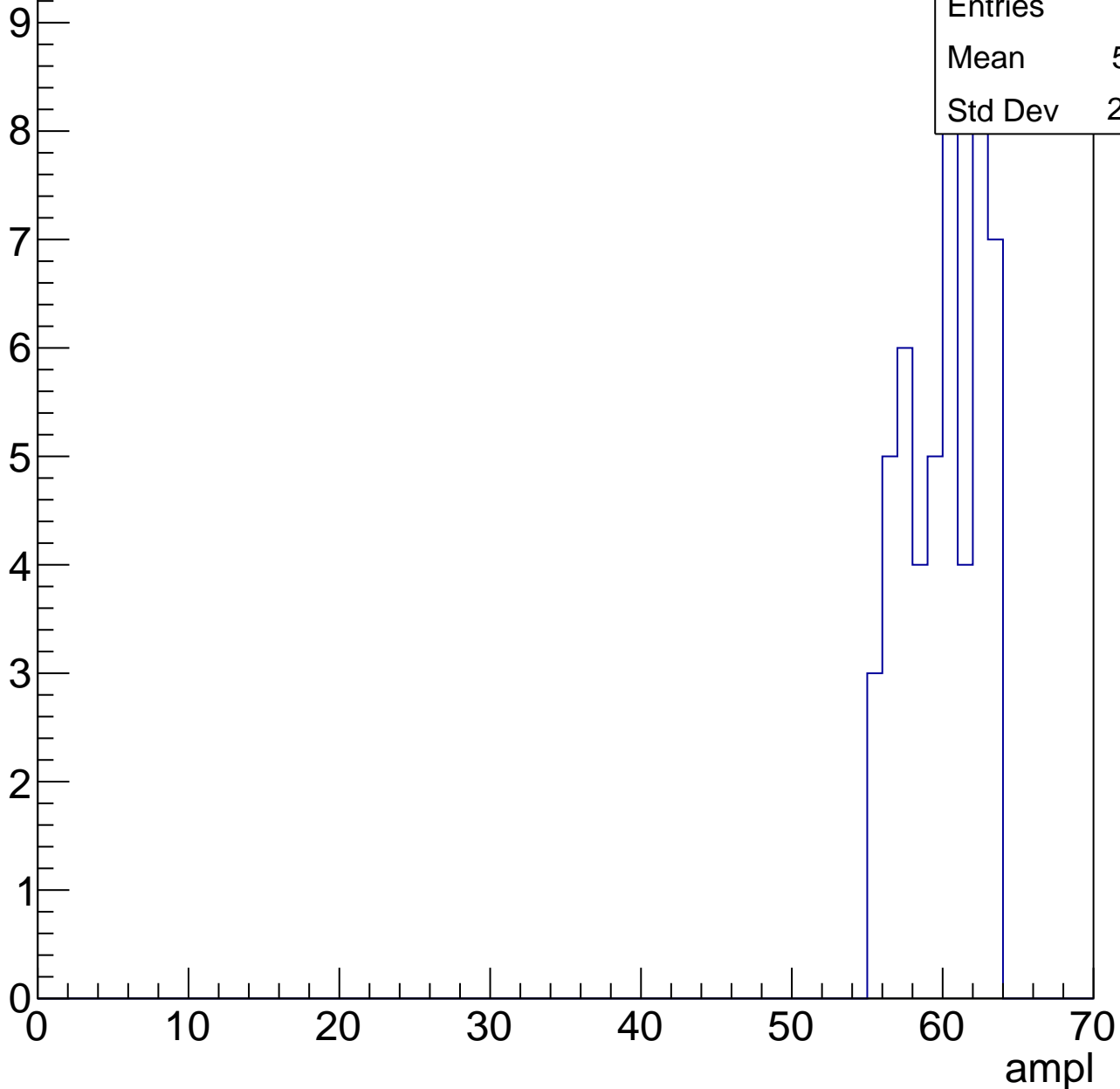


# B1L103S, U21-ch100, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

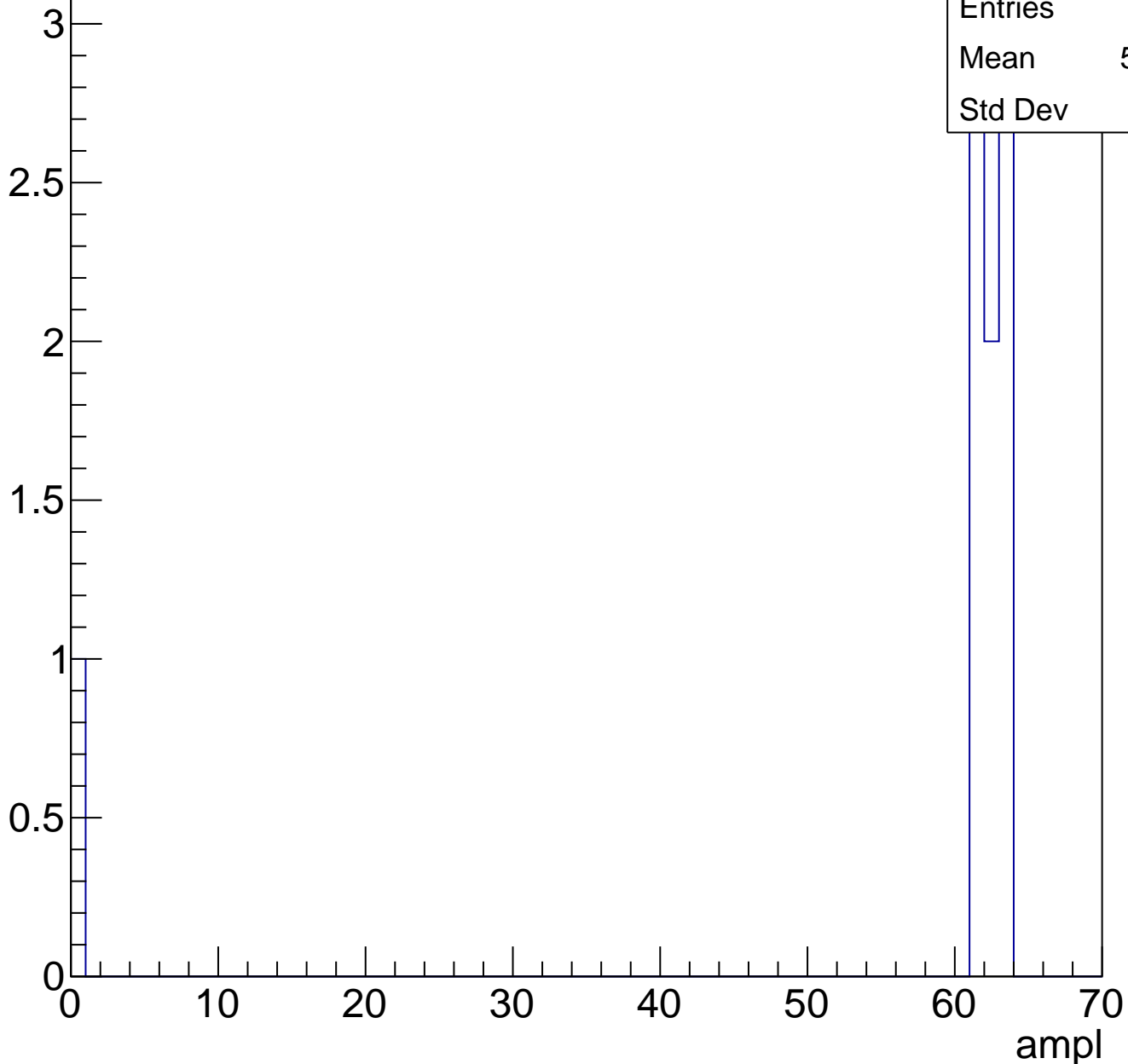
Entries	51
Mean	59.51
Std Dev	2.492



# B1L103S, U21-ch100, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

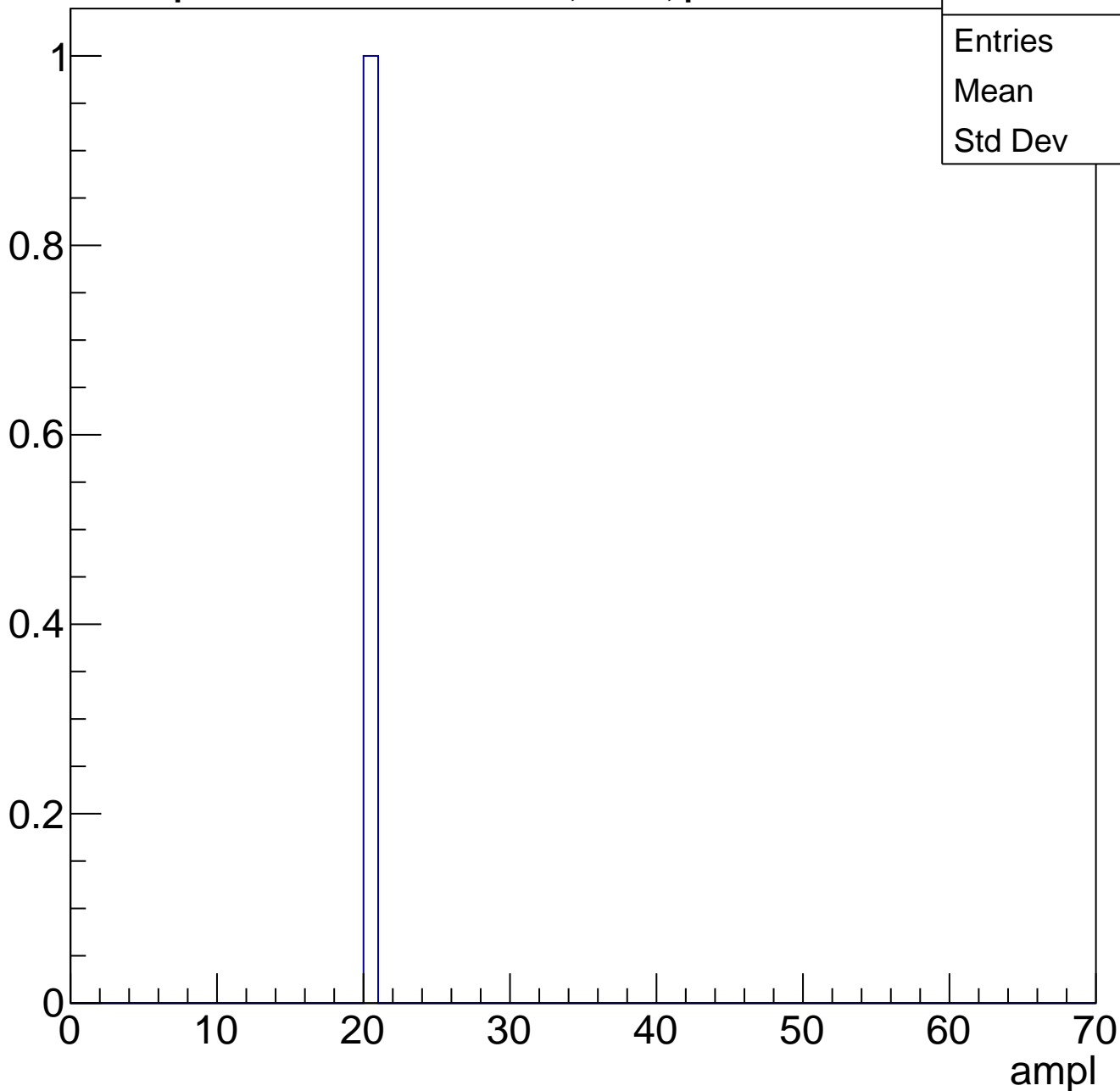




# B1L103S, U21-ch100, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	20
Std Dev	0

# B1L103S, U21-ch101, adc0

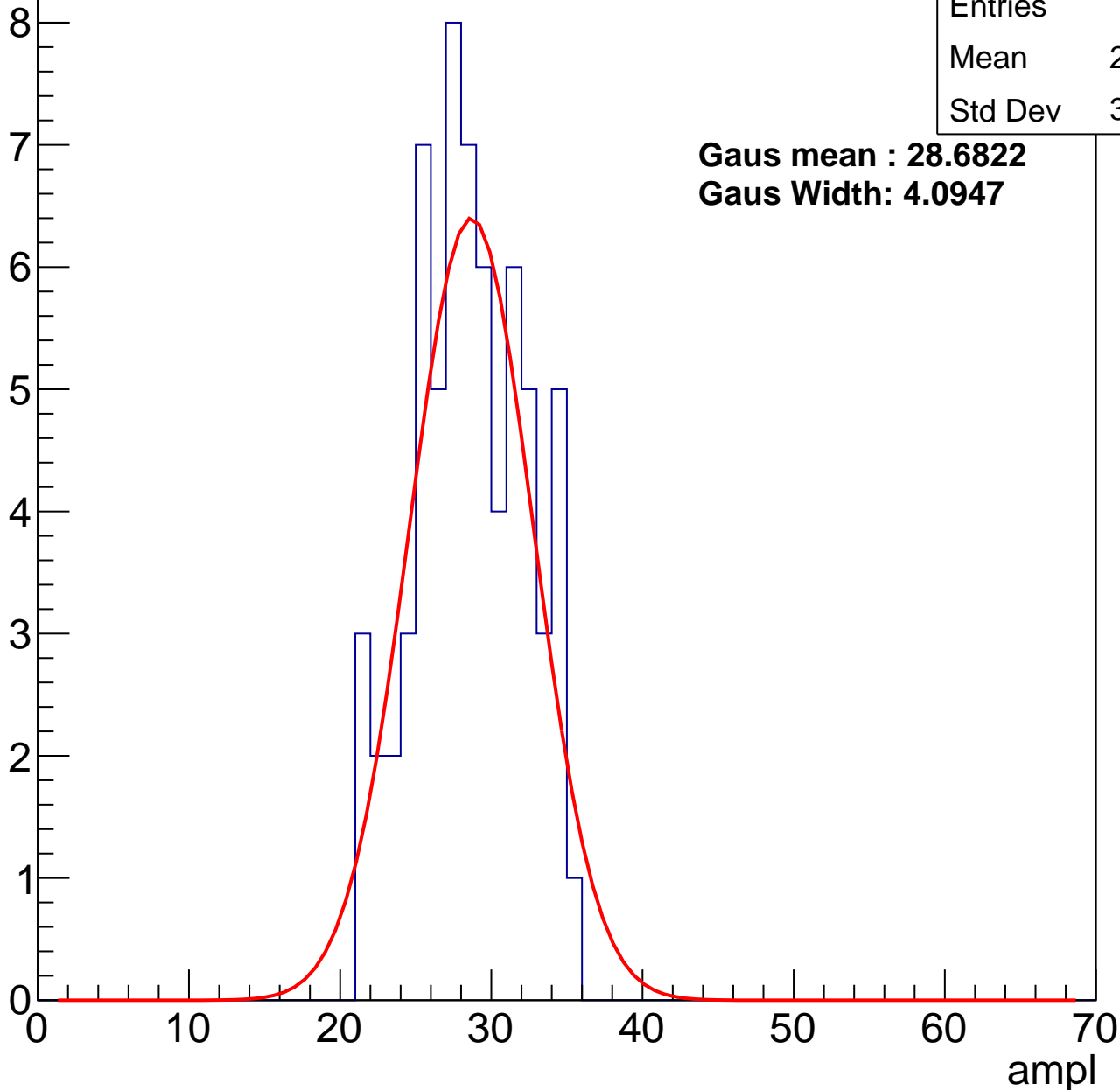
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	28.15
Std Dev	3.596

**Gaus mean : 28.6822**

**Gaus Width: 4.0947**



# B1L103S, U21-ch101, adc1

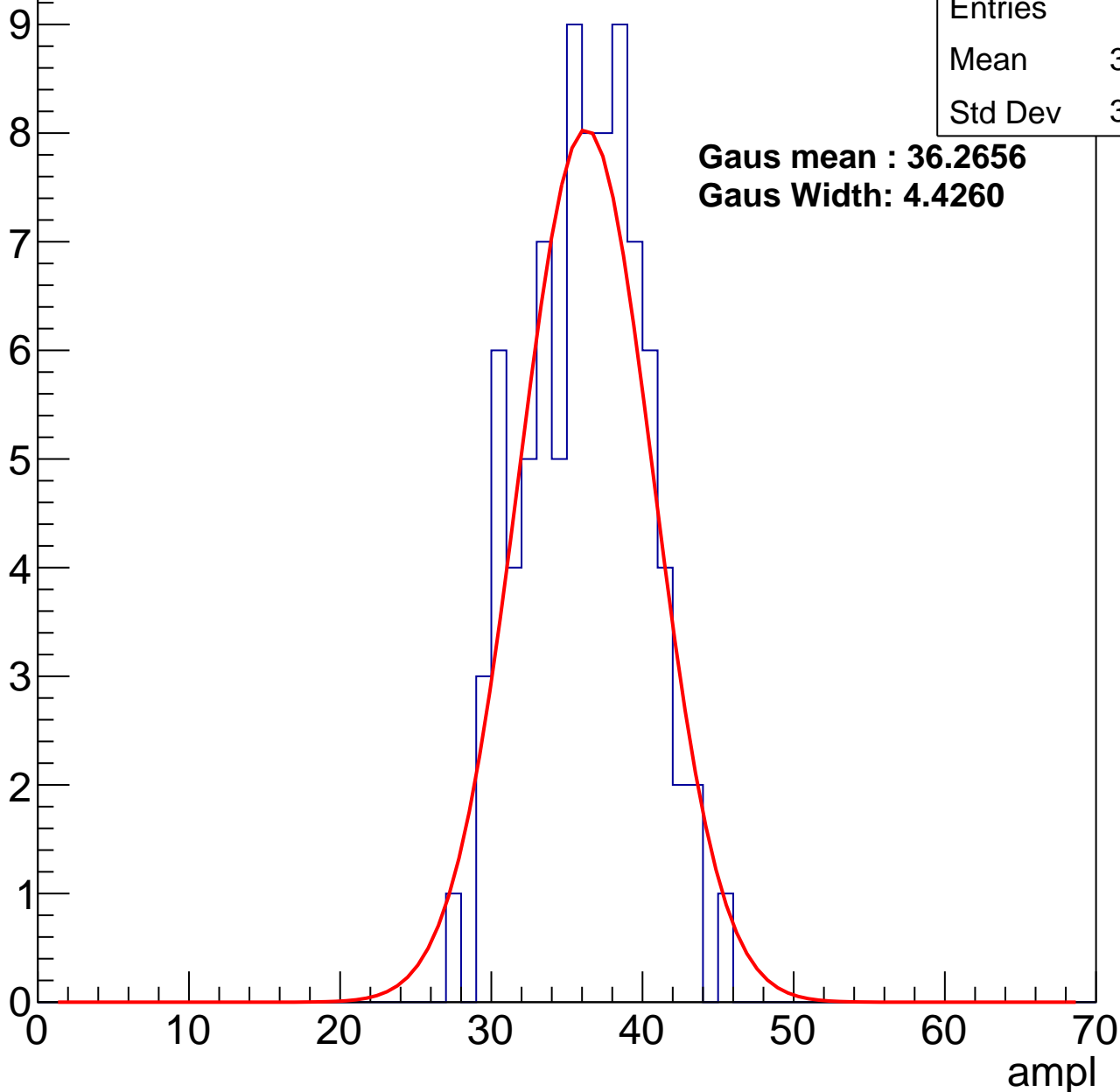
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	87
Mean	35.77
Std Dev	3.814

**Gaus mean : 36.2656**

**Gaus Width: 4.4260**



# B1L103S, U21-ch101, adc2

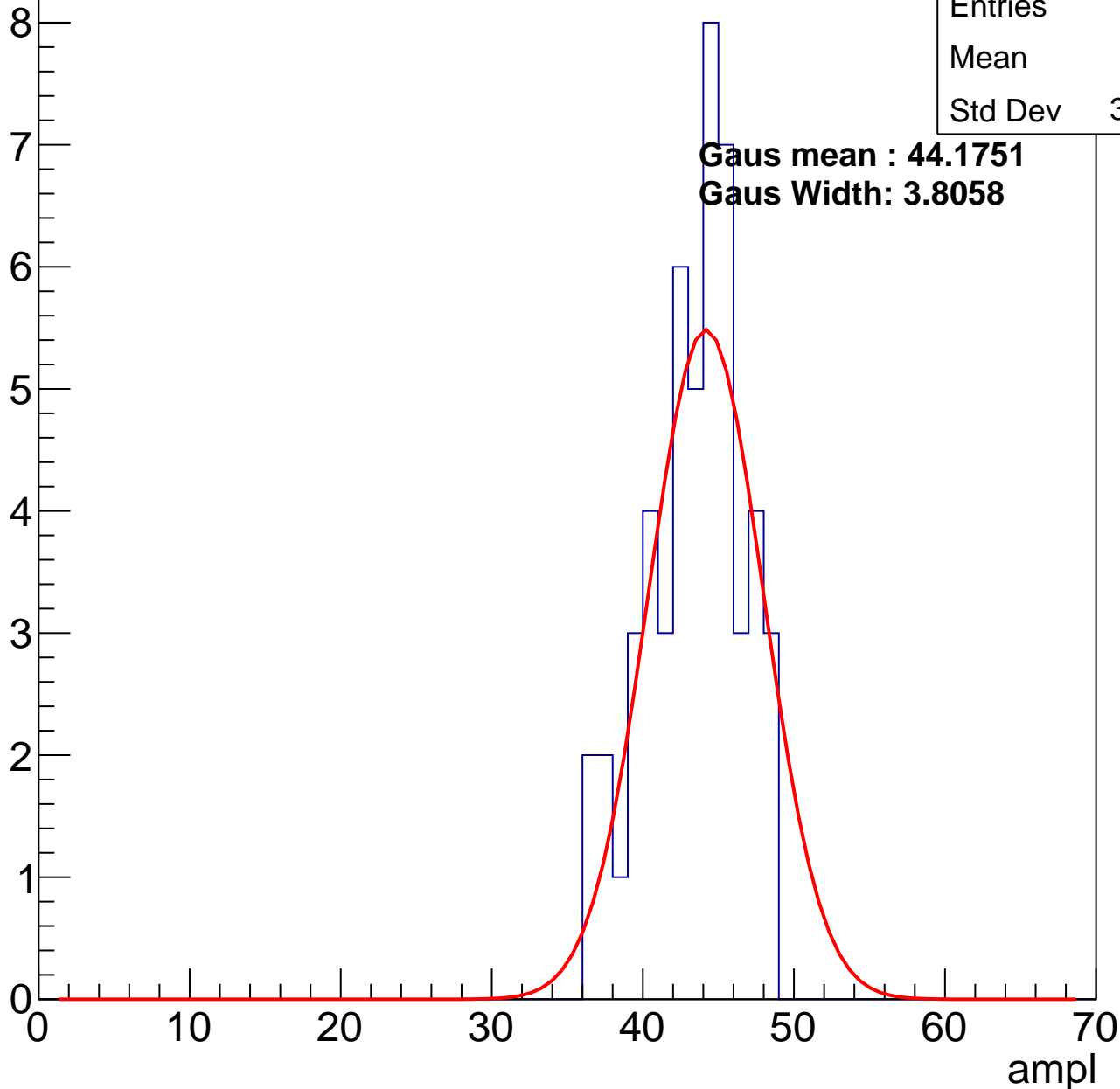
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	42.9
Std Dev	3.126

**Gaus mean : 44.1751**

**Gaus Width: 3.8058**



# B1L103S, U21-ch101, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	96
Mean	50.17
Std Dev	4.257

Entry

10

8

6

4

2

0

0

10

20

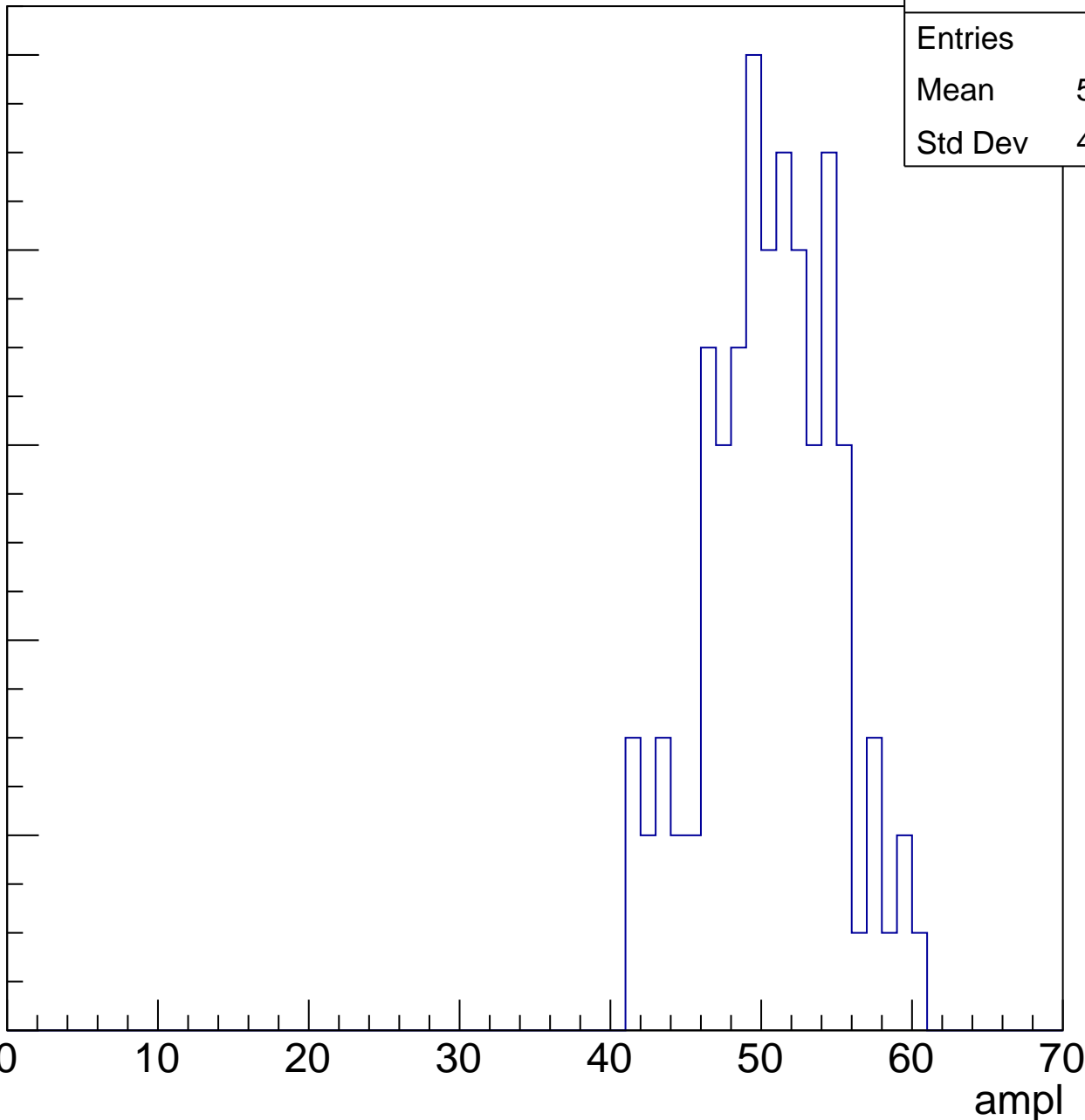
30

40

50

60

ampl

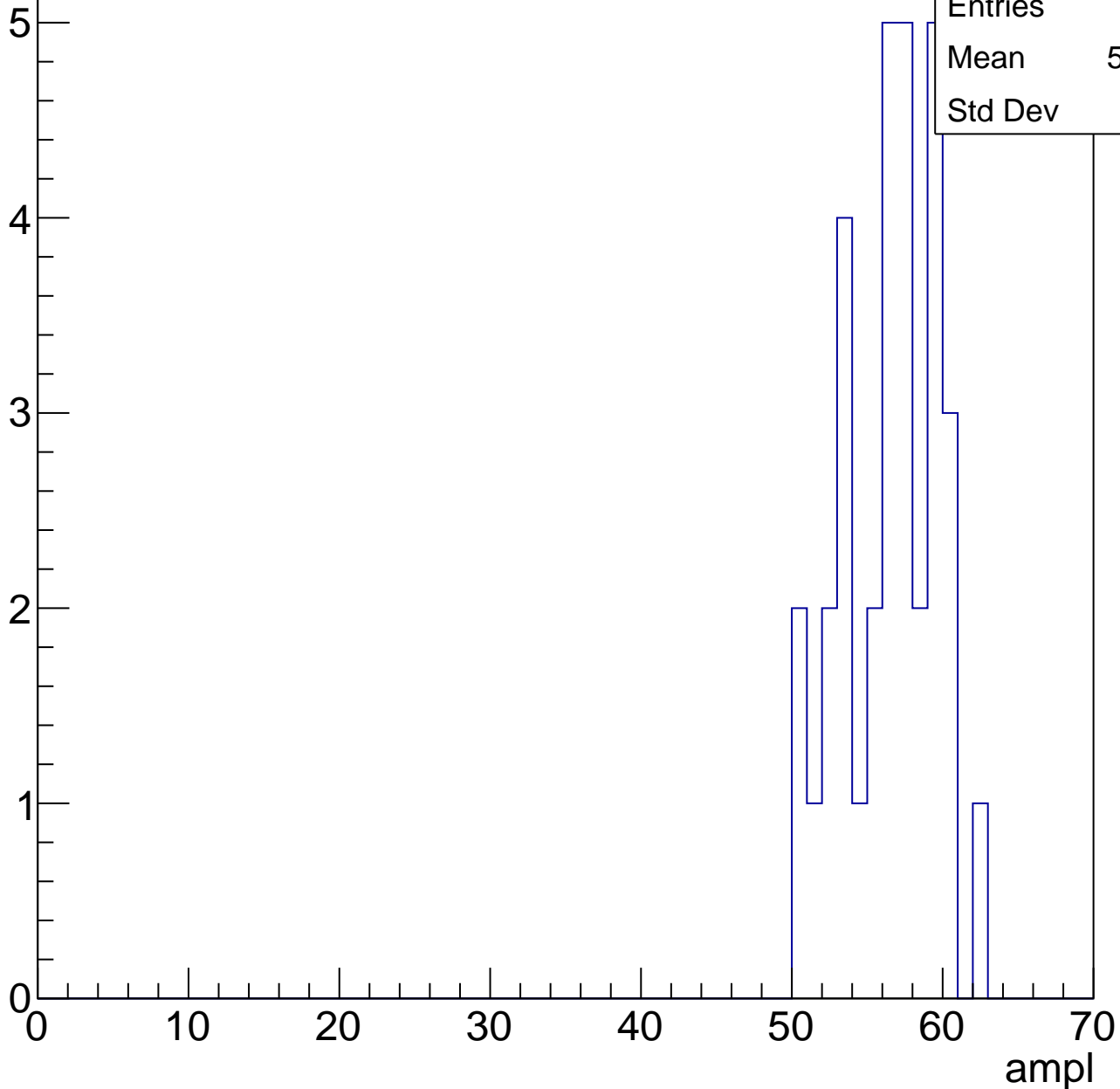


# B1L103S, U21-ch101, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

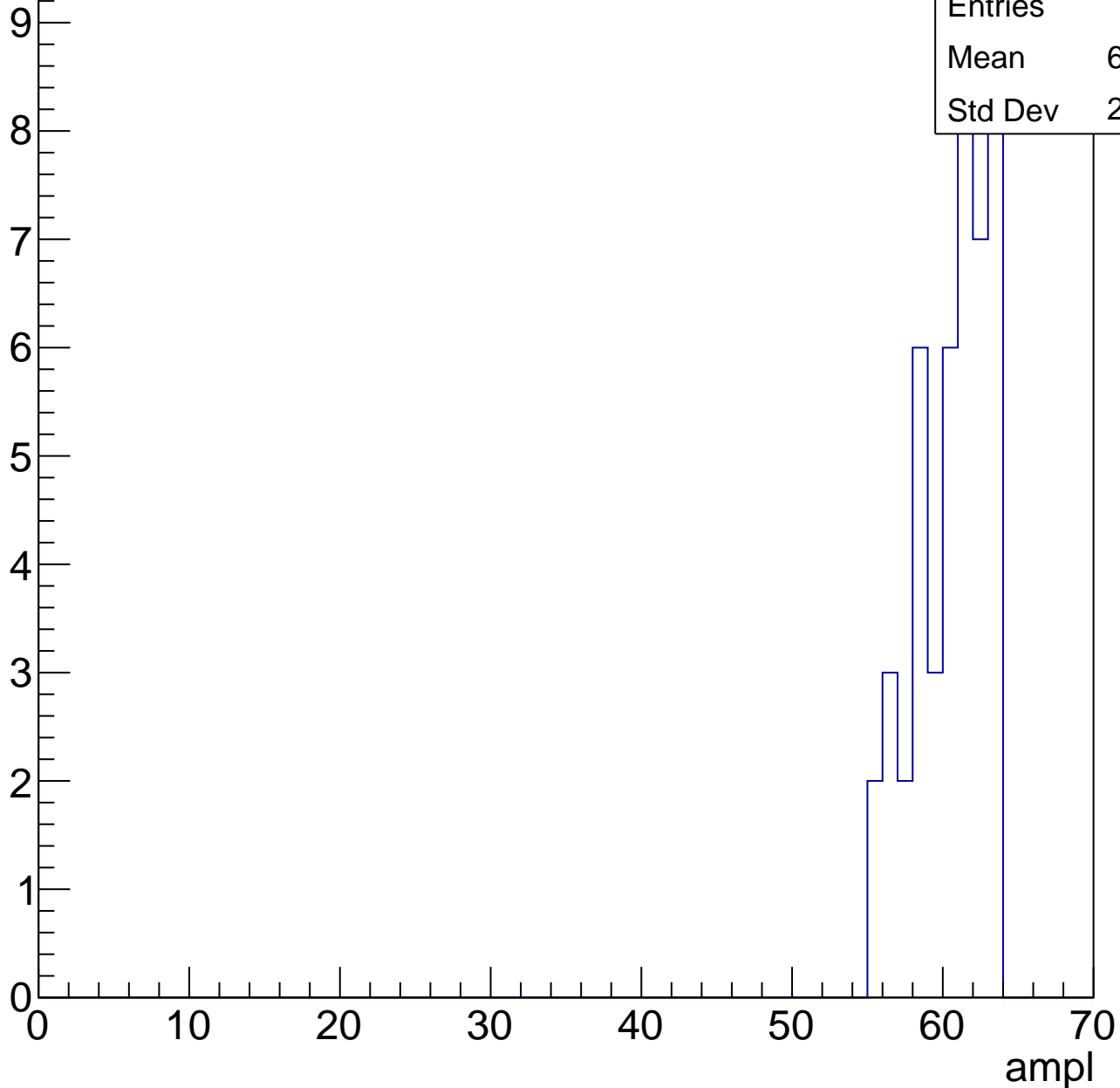
Entries	33
Mean	56.03
Std Dev	3.08



# B1L103S, U21-ch101, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	46
Mean	60.13
Std Dev	2.374

# B1L103S, U21-ch101, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

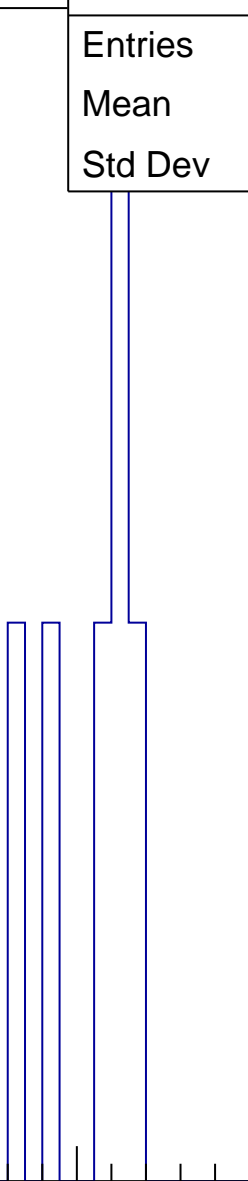
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	60.33
Std Dev	2.494

0 10 20 30 40 50 60 70

ampl





# B1L103S, U21-ch101, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	3
Mean	20.33
Std Dev	28.76

# B1L103S, U21-ch102, adc0

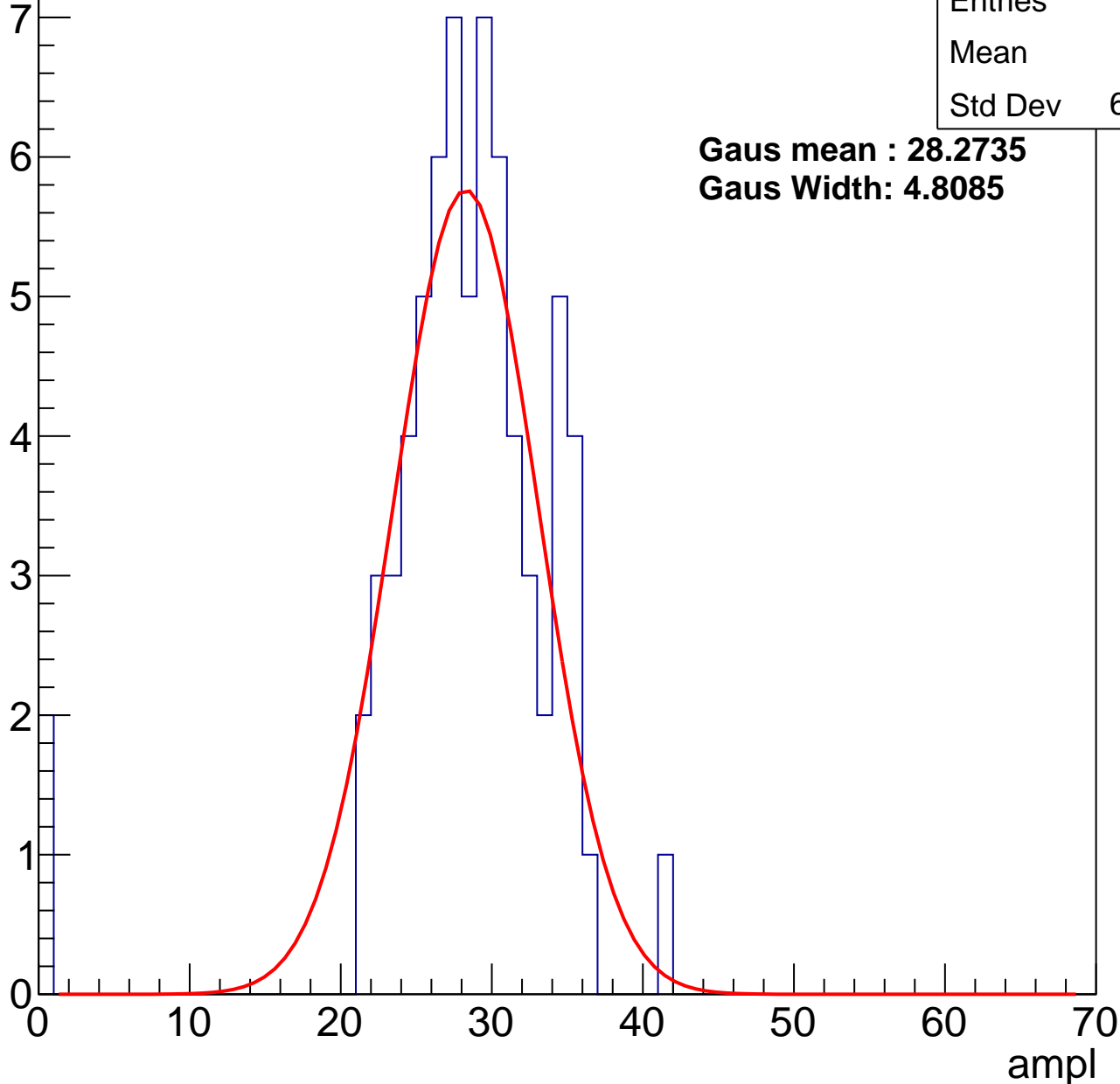
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	27.7
Std Dev	6.275

**Gaus mean : 28.2735**

**Gaus Width: 4.8085**



# B1L103S, U21-ch102, adc1

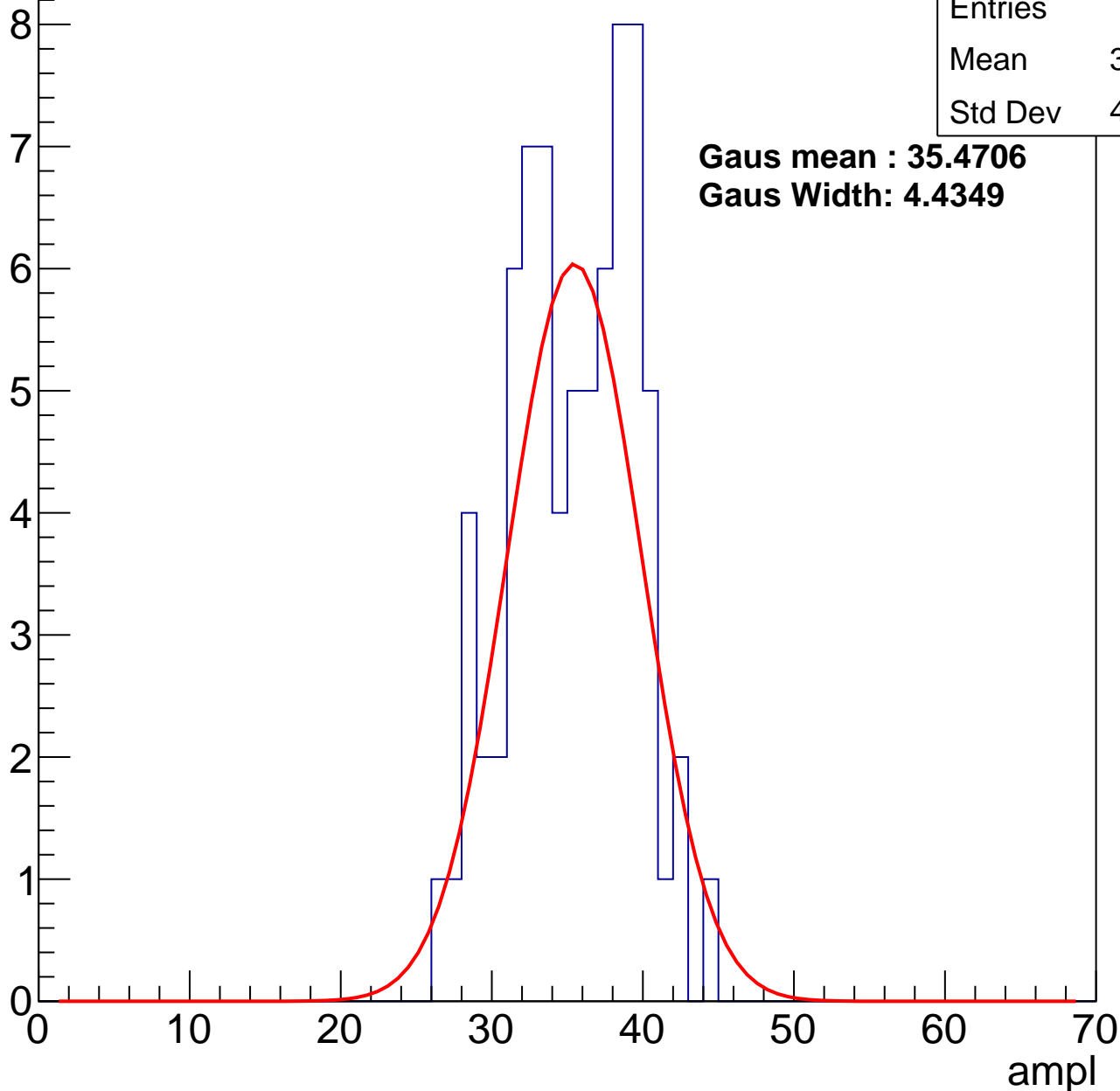
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	34.96
Std Dev	4.038

**Gaus mean : 35.4706**

**Gaus Width: 4.4349**



# B1L103S, U21-ch102, adc2

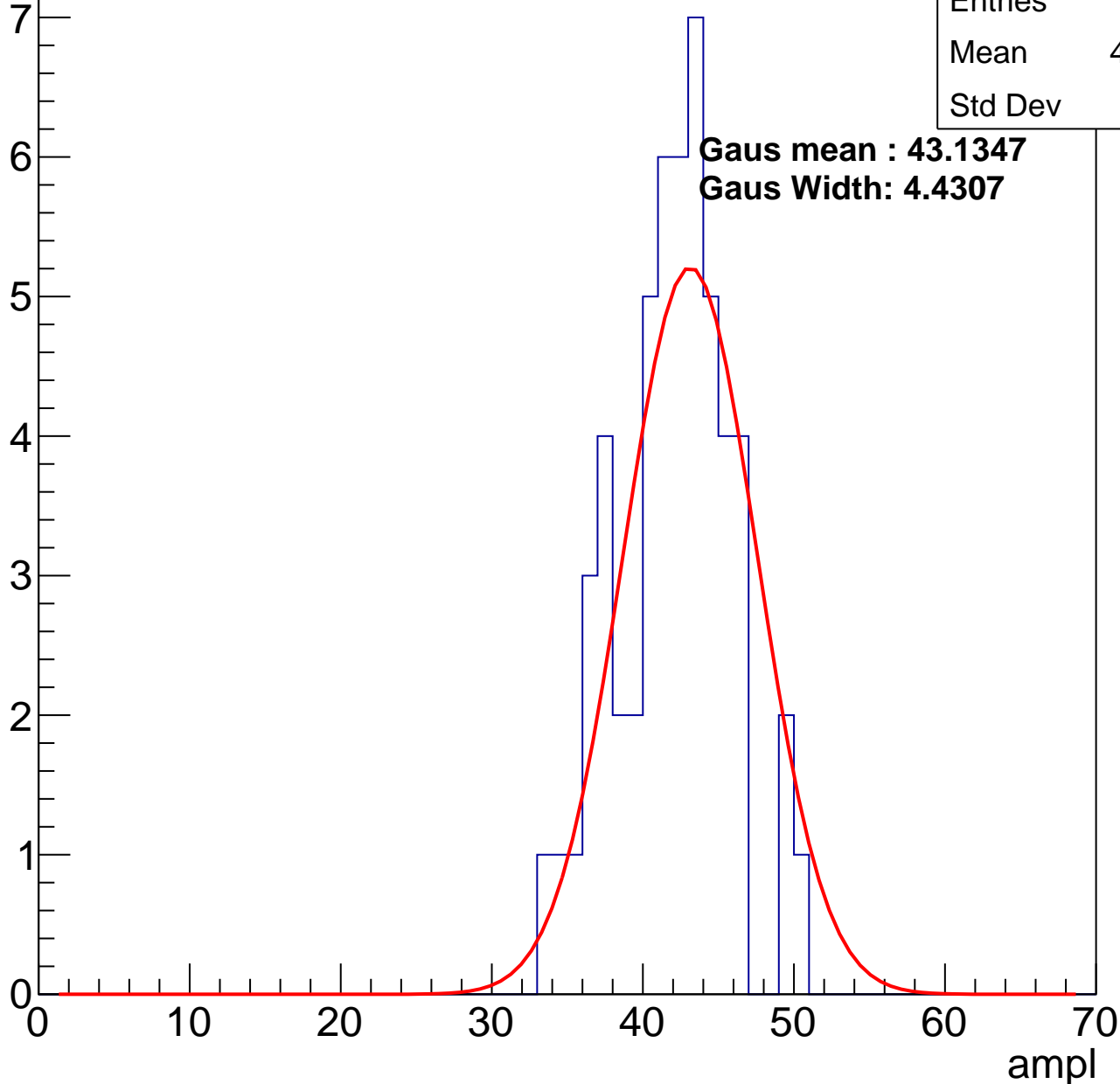
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	41.54
Std Dev	3.74

**Gaus mean : 43.1347**

**Gaus Width: 4.4307**

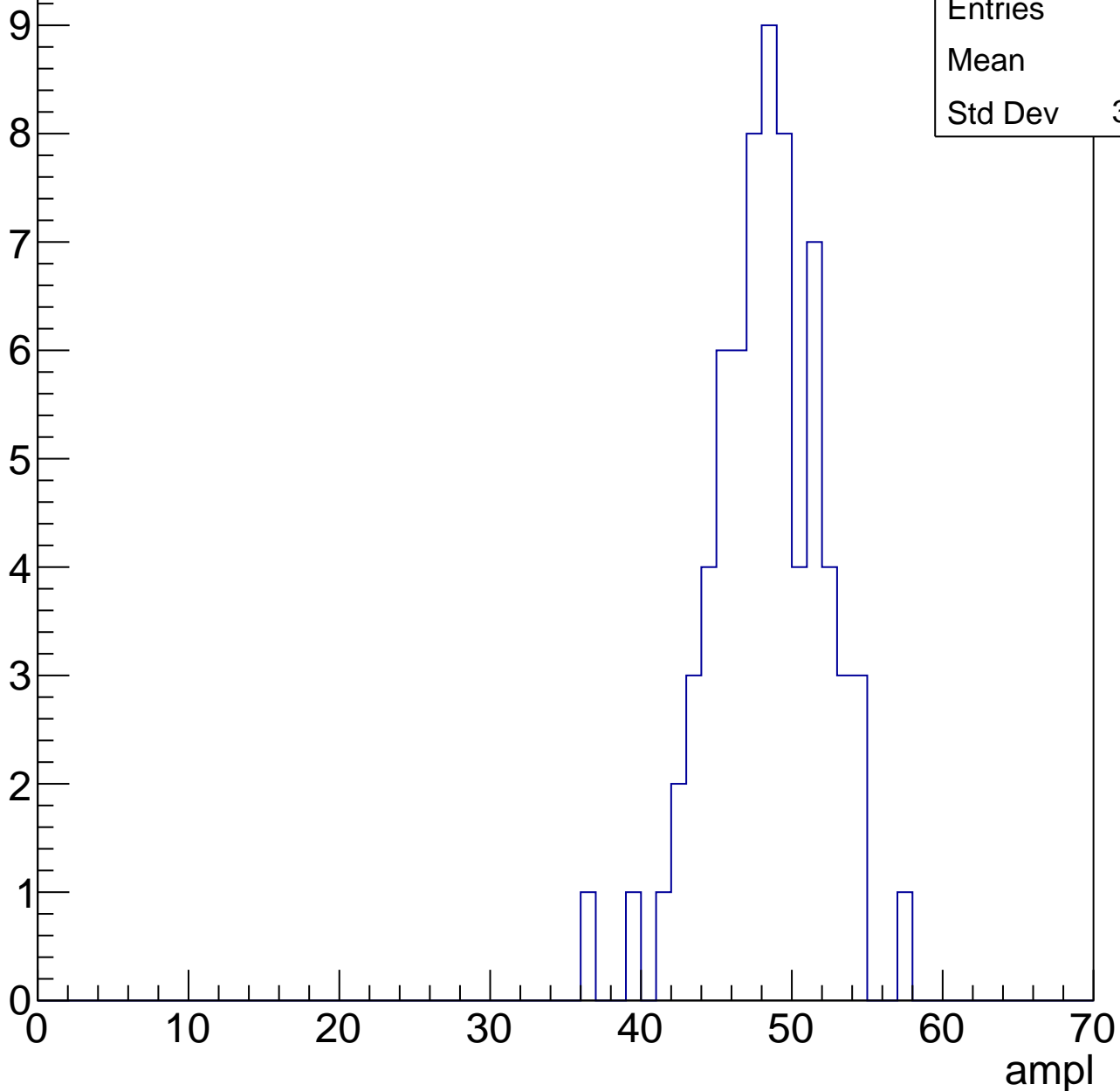


# B1L103S, U21-ch102, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	47.8
Std Dev	3.721

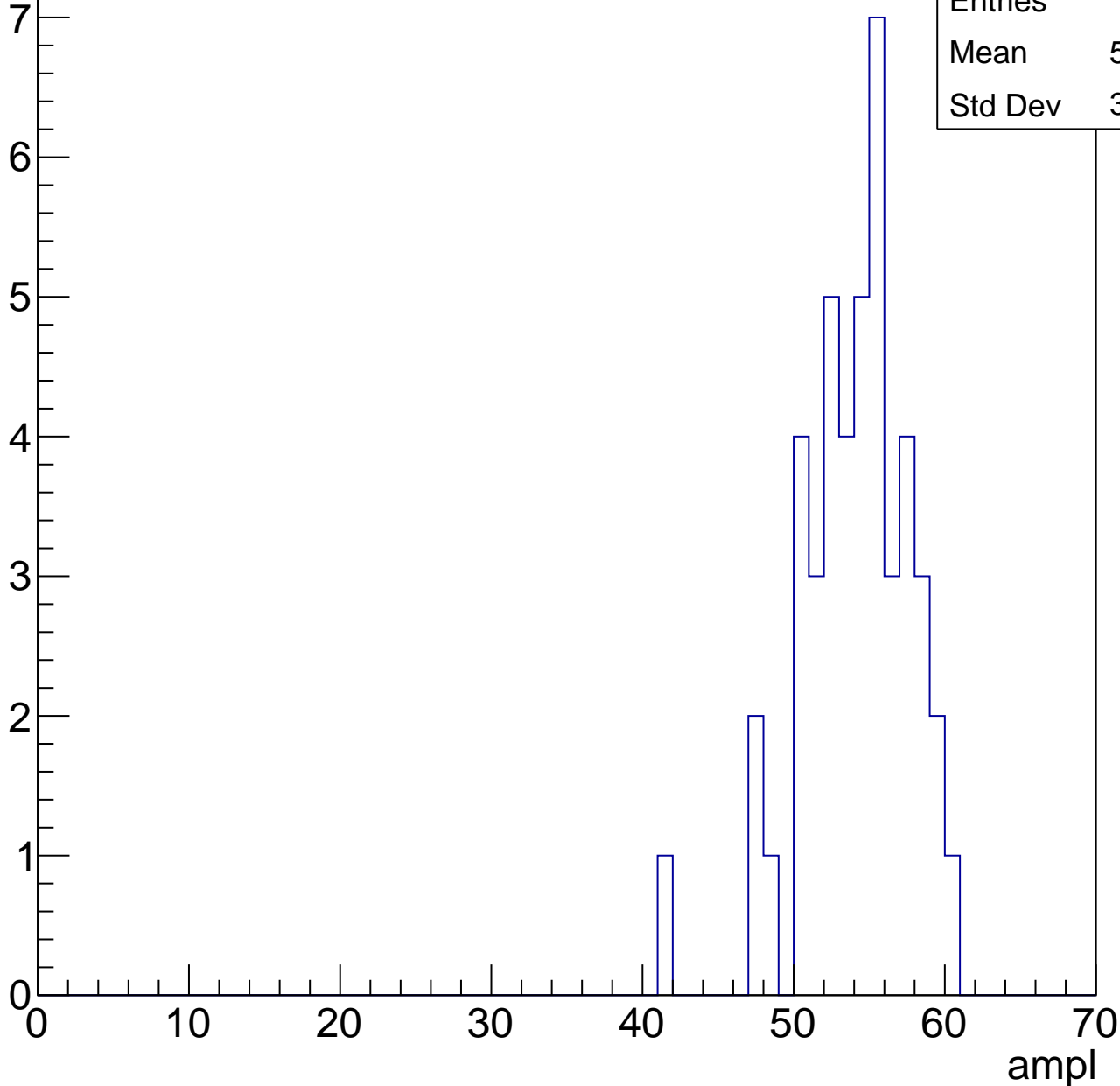


# B1L103S, U21-ch102, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	45
Mean	53.58
Std Dev	3.648

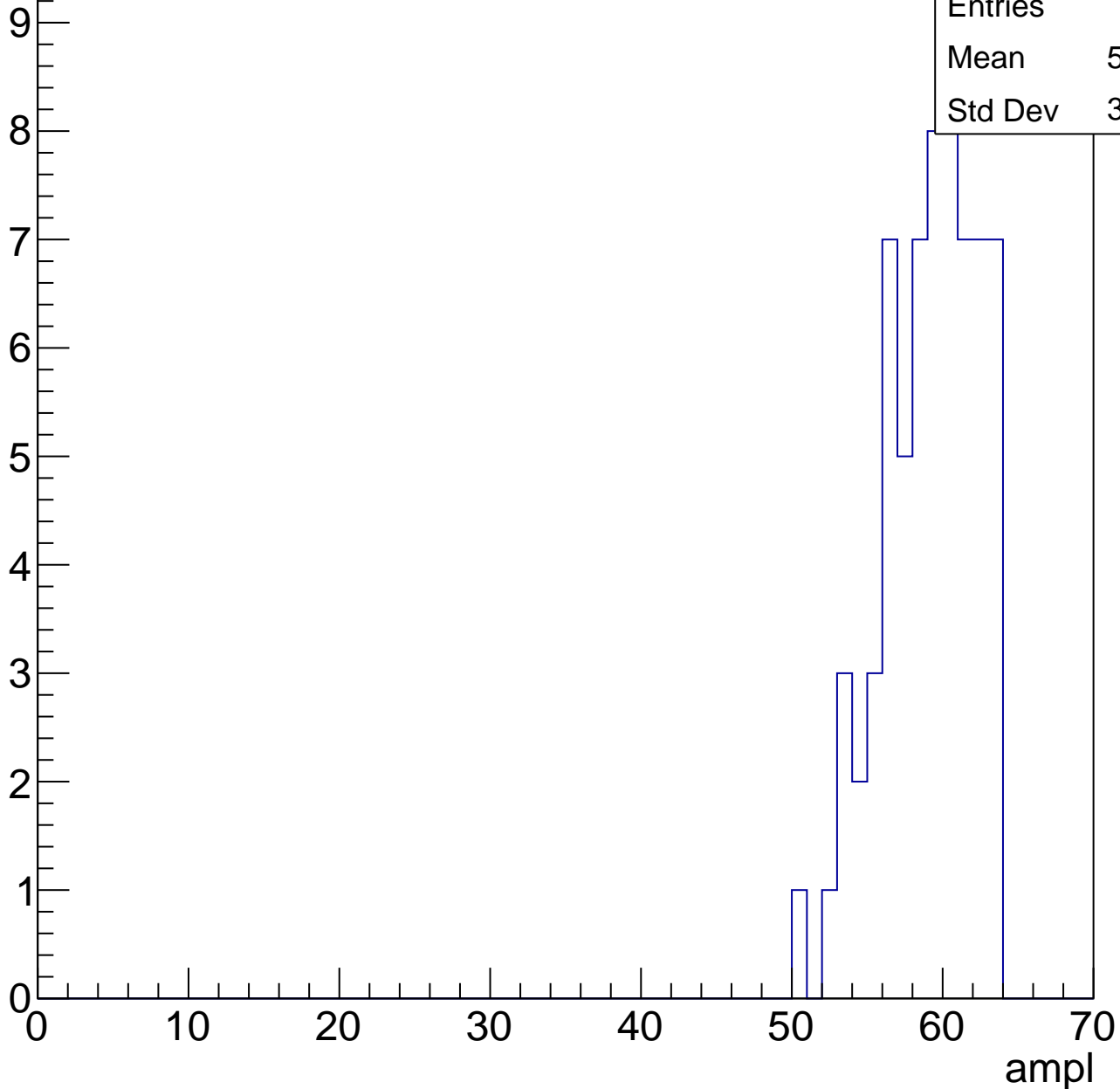


# B1L103S, U21-ch102, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

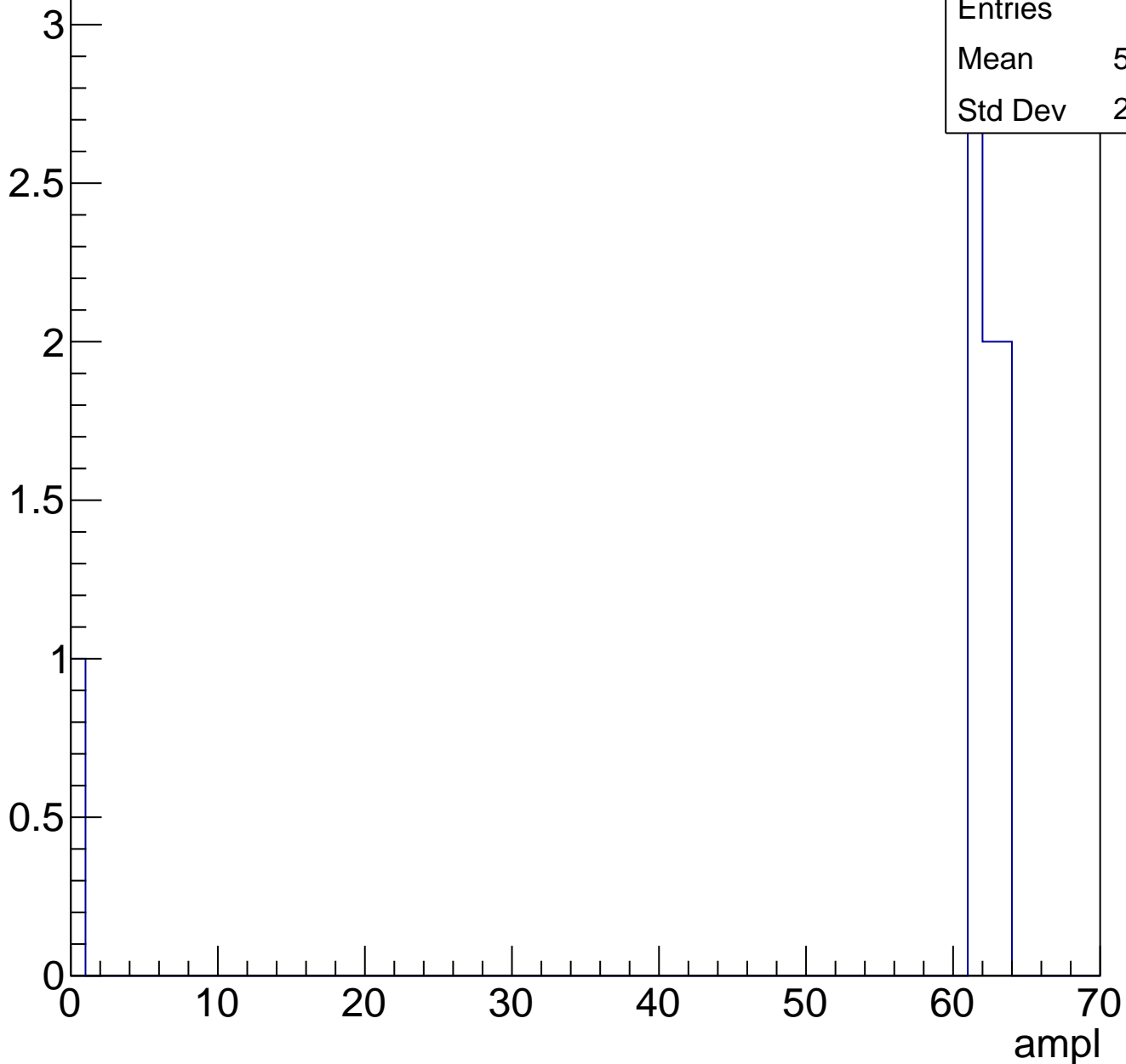
Entries	67
Mean	58.67
Std Dev	3.068



# B1L103S, U21-ch102, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

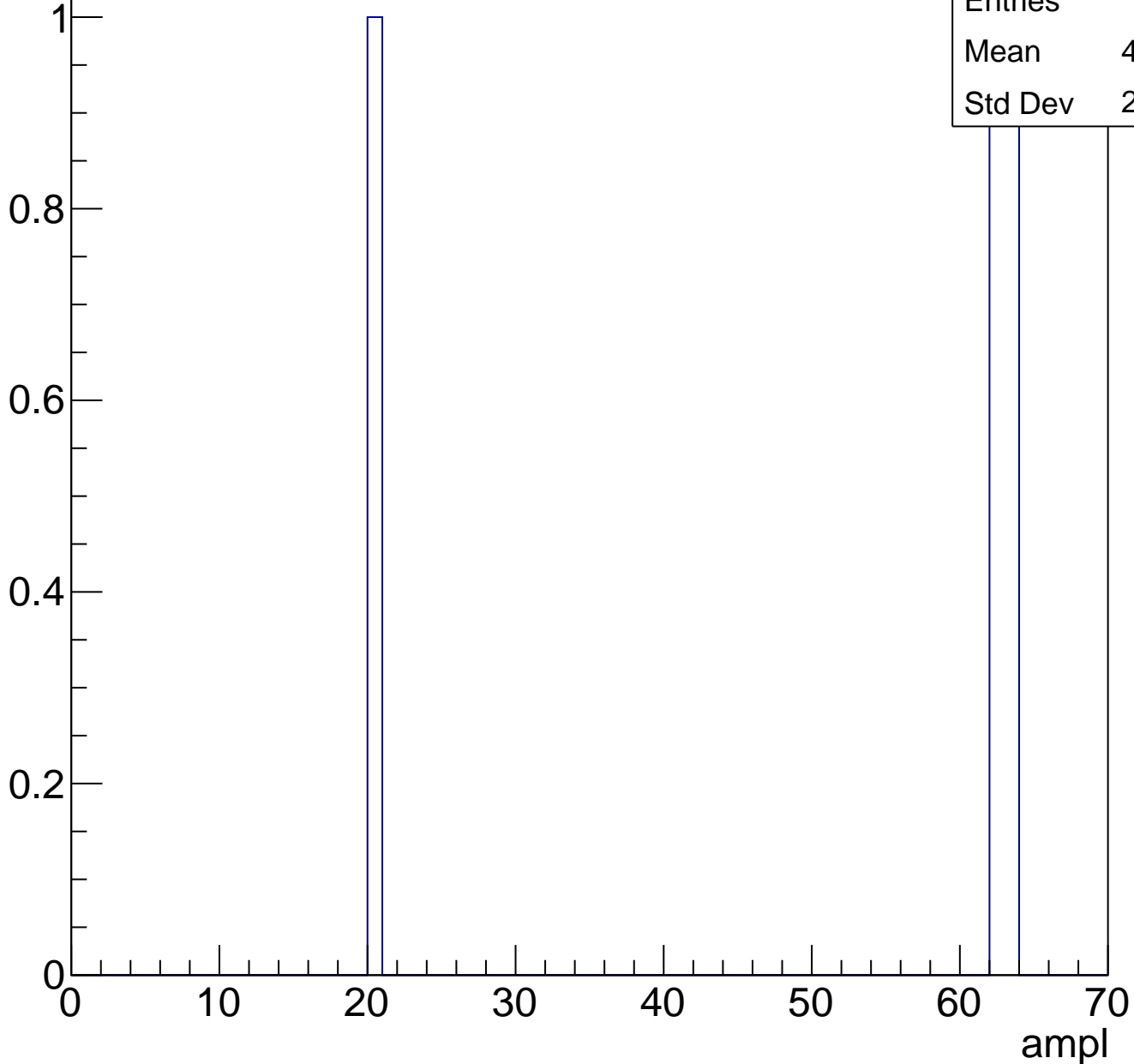




# B1L103S, U21-ch102, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U21-ch103, adc0

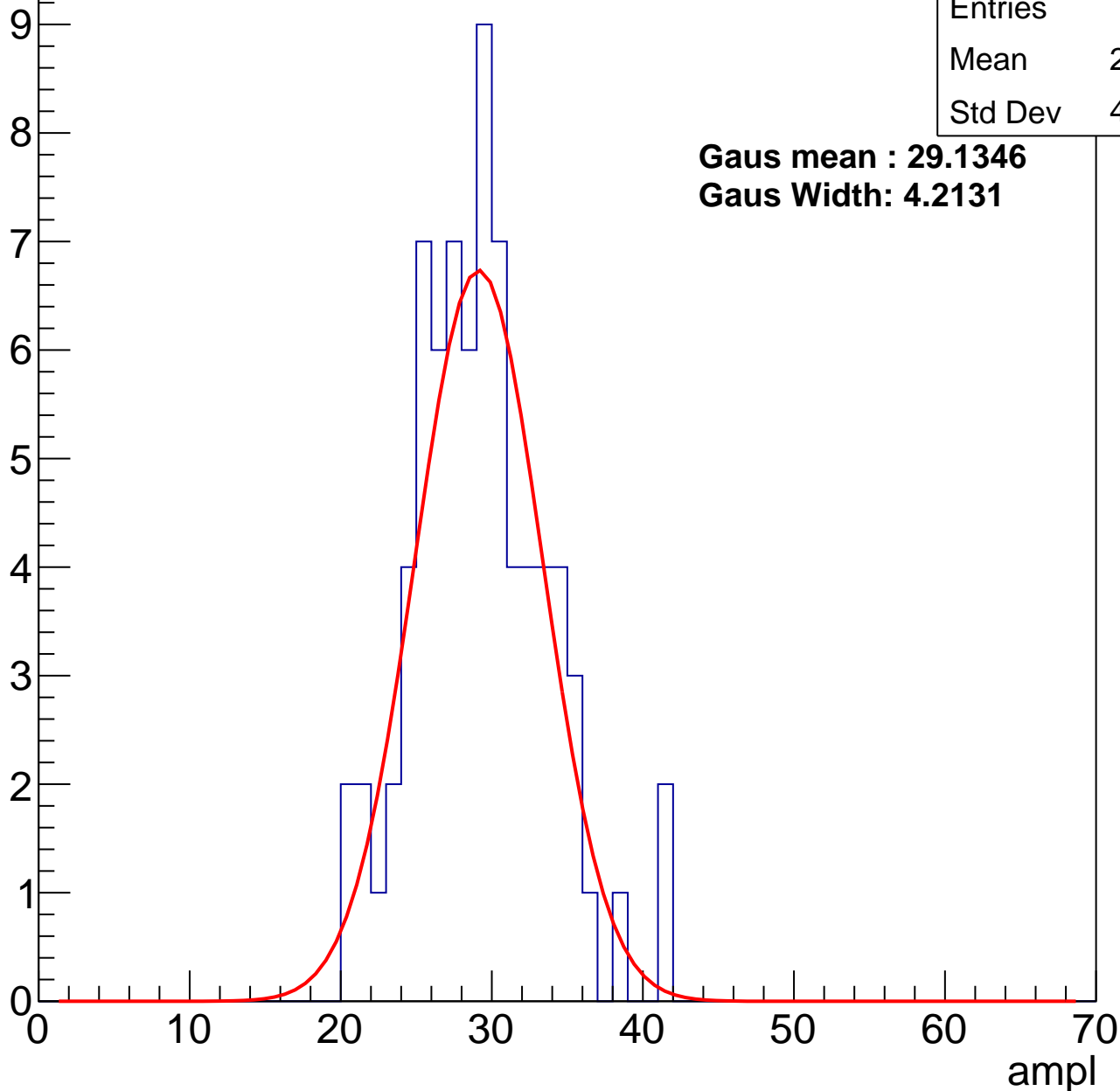
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	28.76
Std Dev	4.377

**Gaus mean : 29.1346**

**Gaus Width: 4.2131**



# B1L103S, U21-ch103, adc1

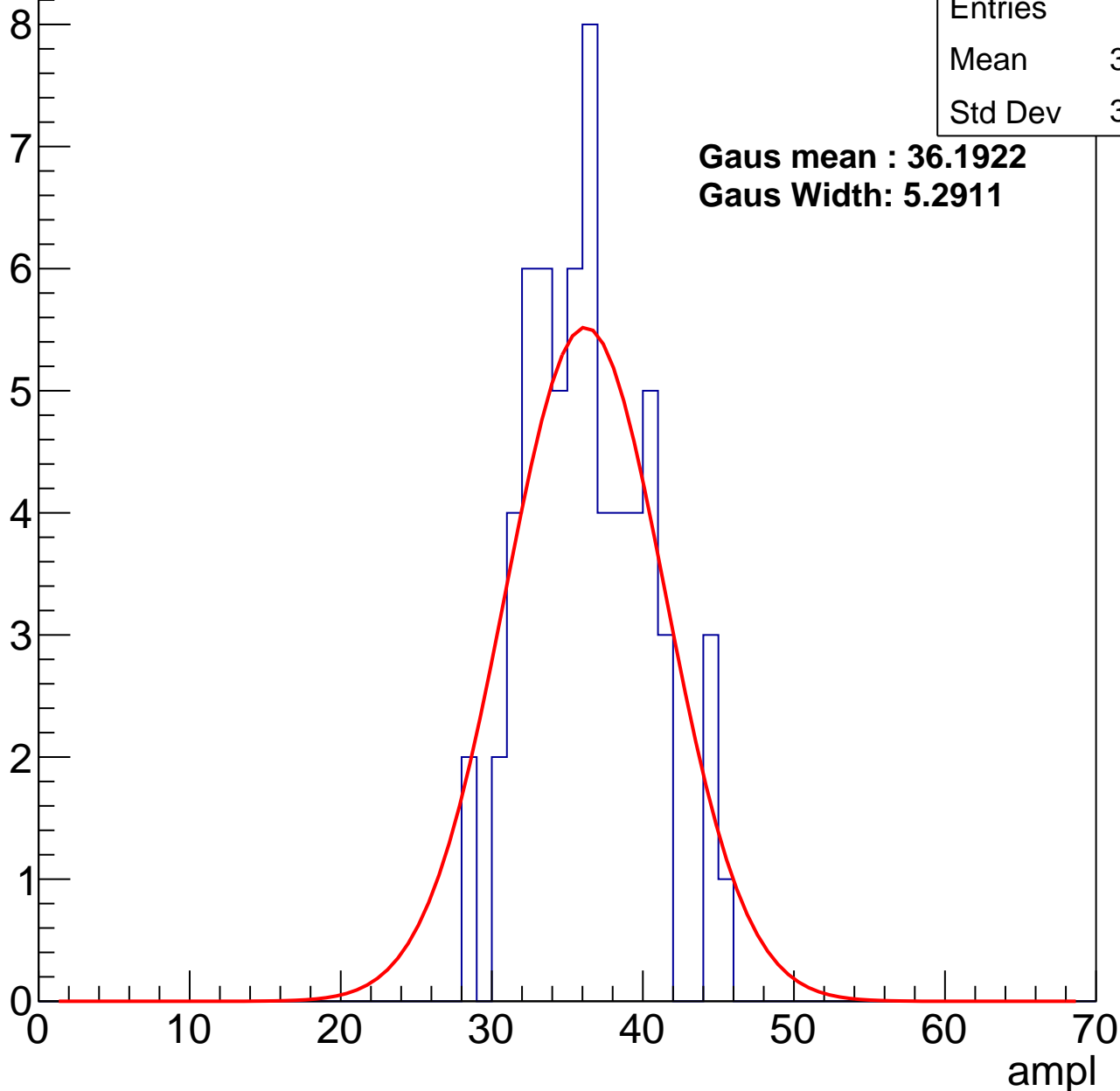
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	35.78
Std Dev	3.897

**Gaus mean : 36.1922**

**Gaus Width: 5.2911**



# B1L103S, U21-ch103, adc2

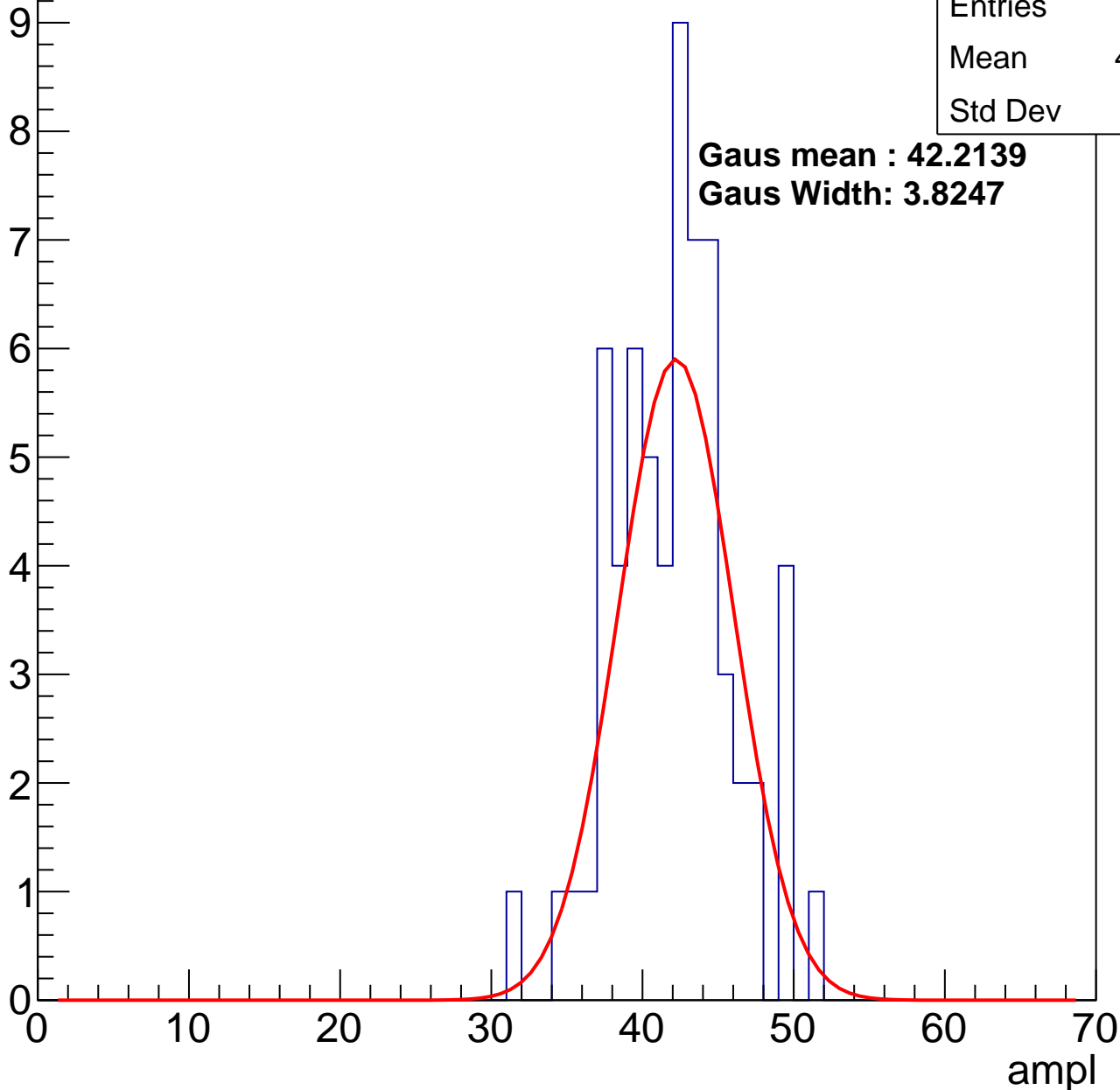
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	41.61
Std Dev	3.9

**Gaus mean : 42.2139**

**Gaus Width: 3.8247**

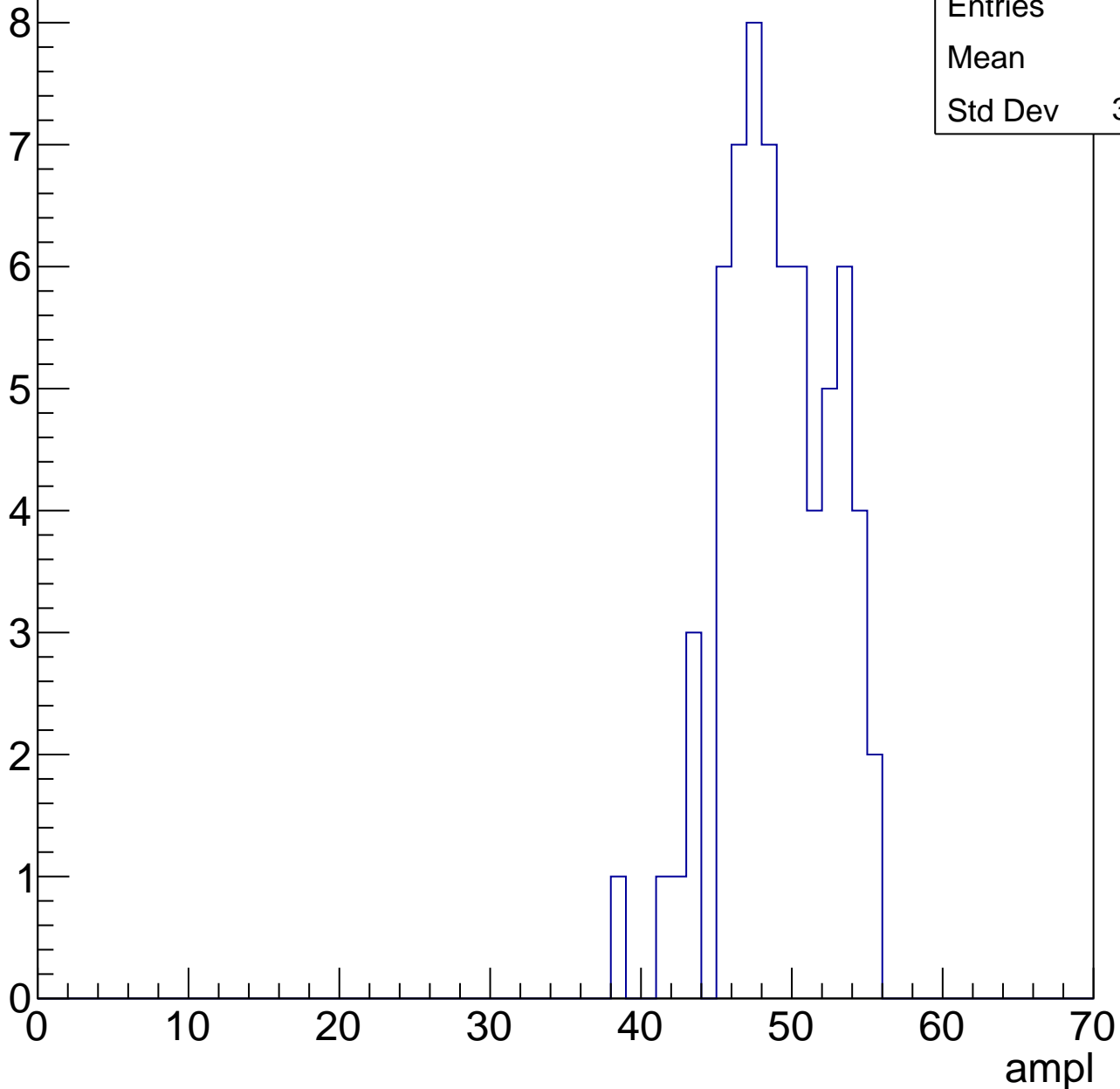


# B1L103S, U21-ch103, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	48.6
Std Dev	3.591

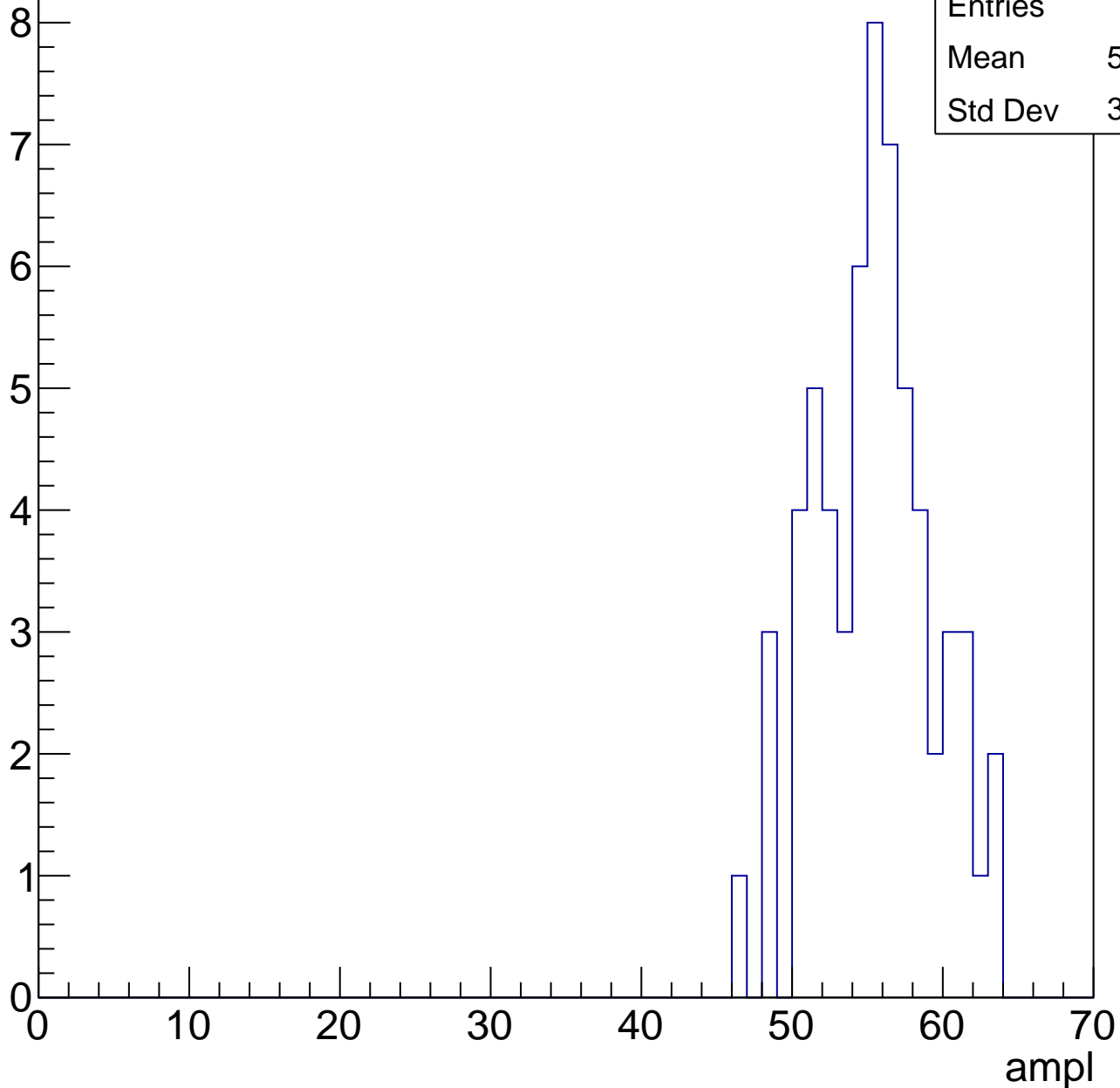


# B1L103S, U21-ch103, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	54.98
Std Dev	3.877

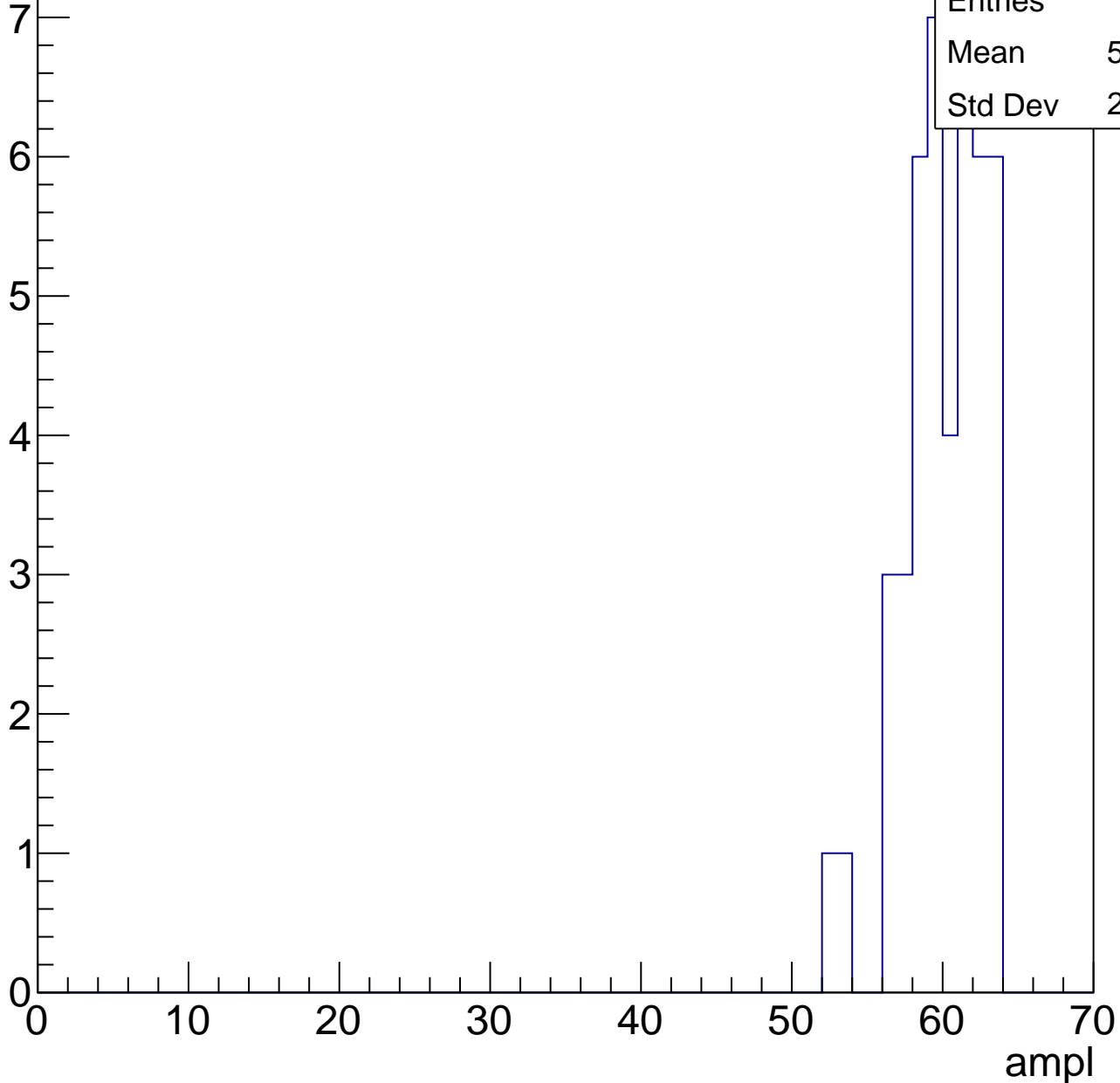


# B1L103S, U21-ch103, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

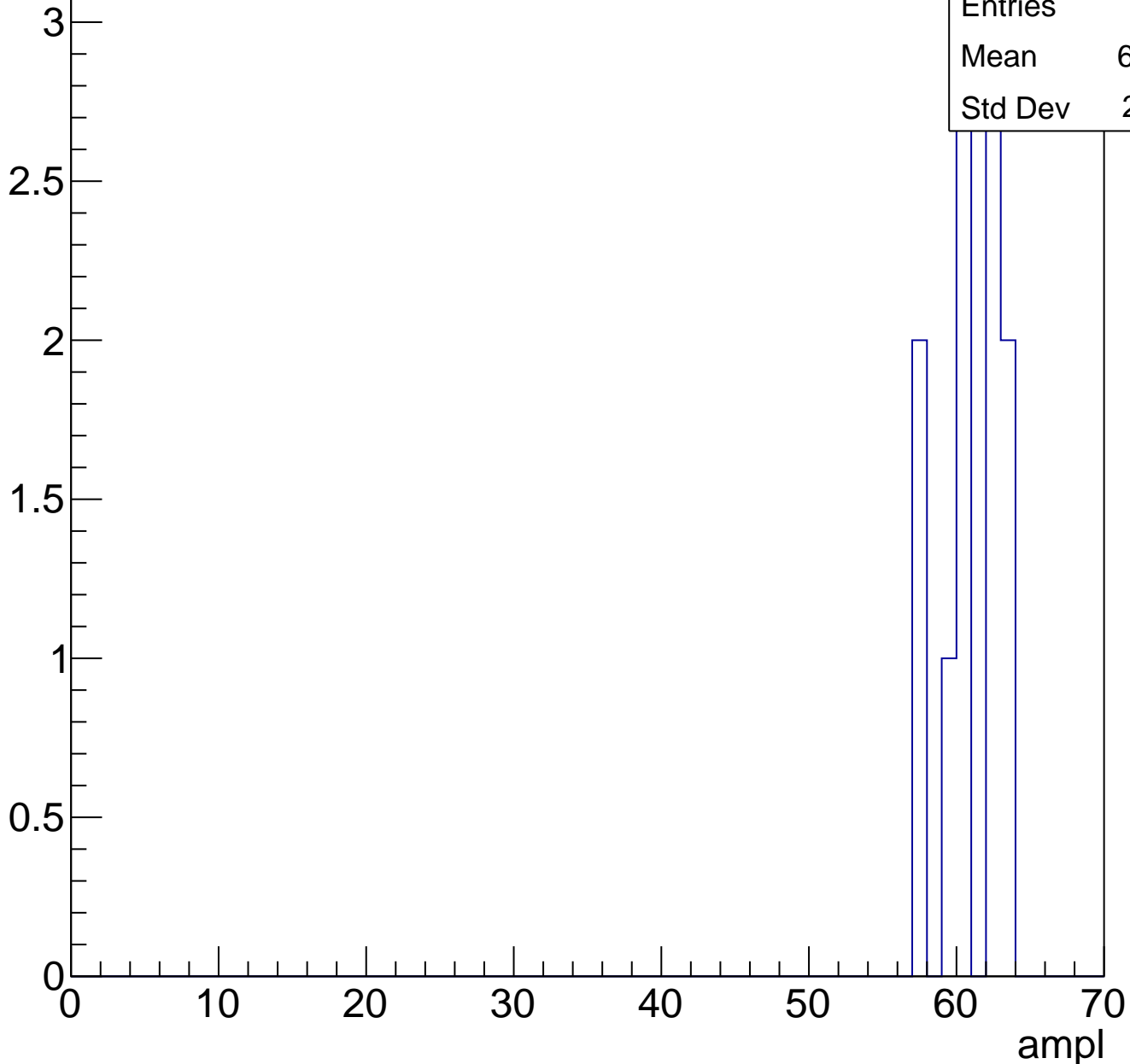
Entries	44
Mean	59.59
Std Dev	2.596



# B1L103S, U21-ch103, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U21-ch103, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U21-ch104, adc0

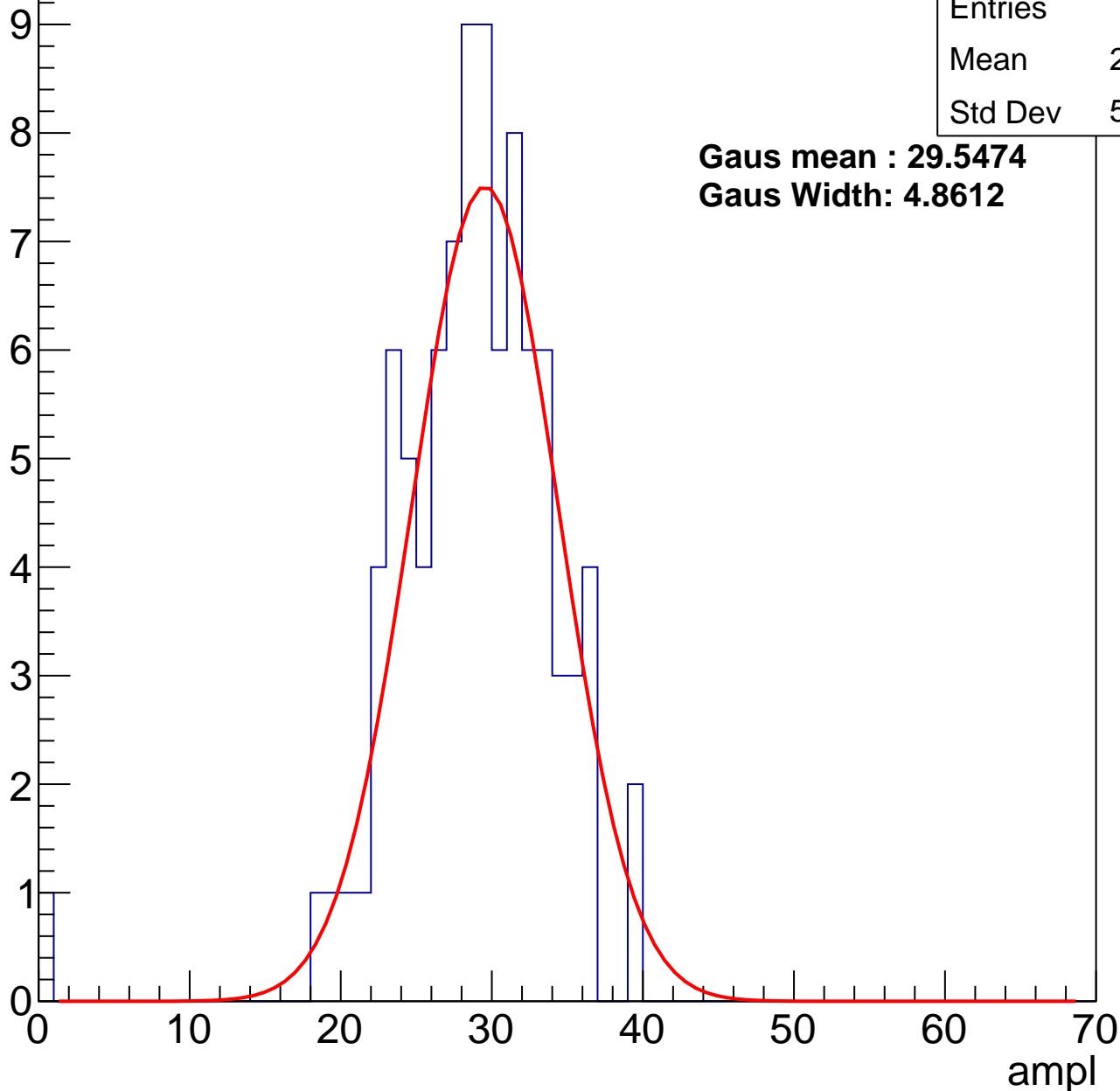
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	93
Mean	28.27
Std Dev	5.304

**Gaus mean : 29.5474**

**Gaus Width: 4.8612**



# B1L103S, U21-ch104, adc1

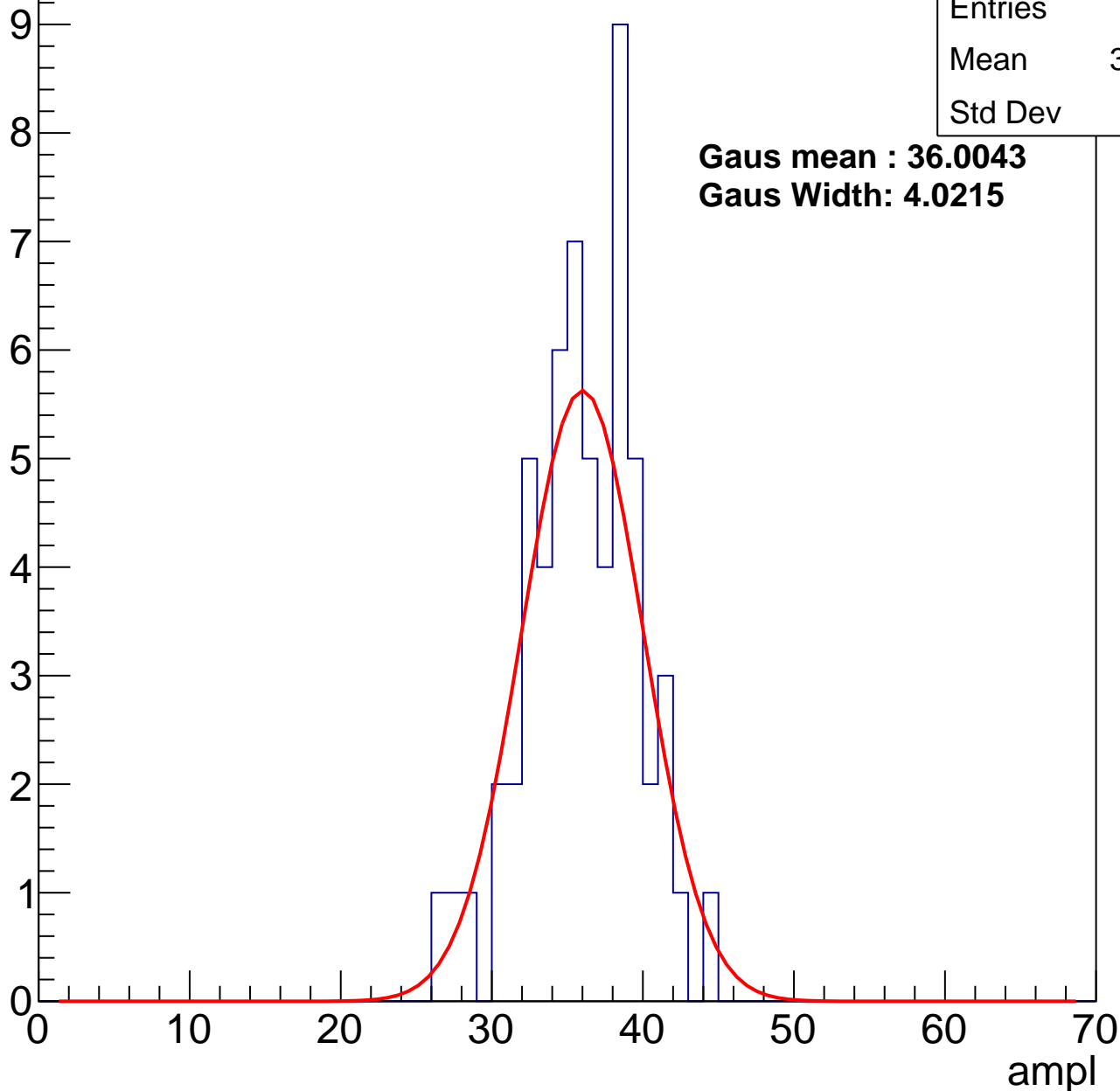
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	35.56
Std Dev	3.67

**Gaus mean : 36.0043**

**Gaus Width: 4.0215**



# B1L103S, U21-ch104, adc2

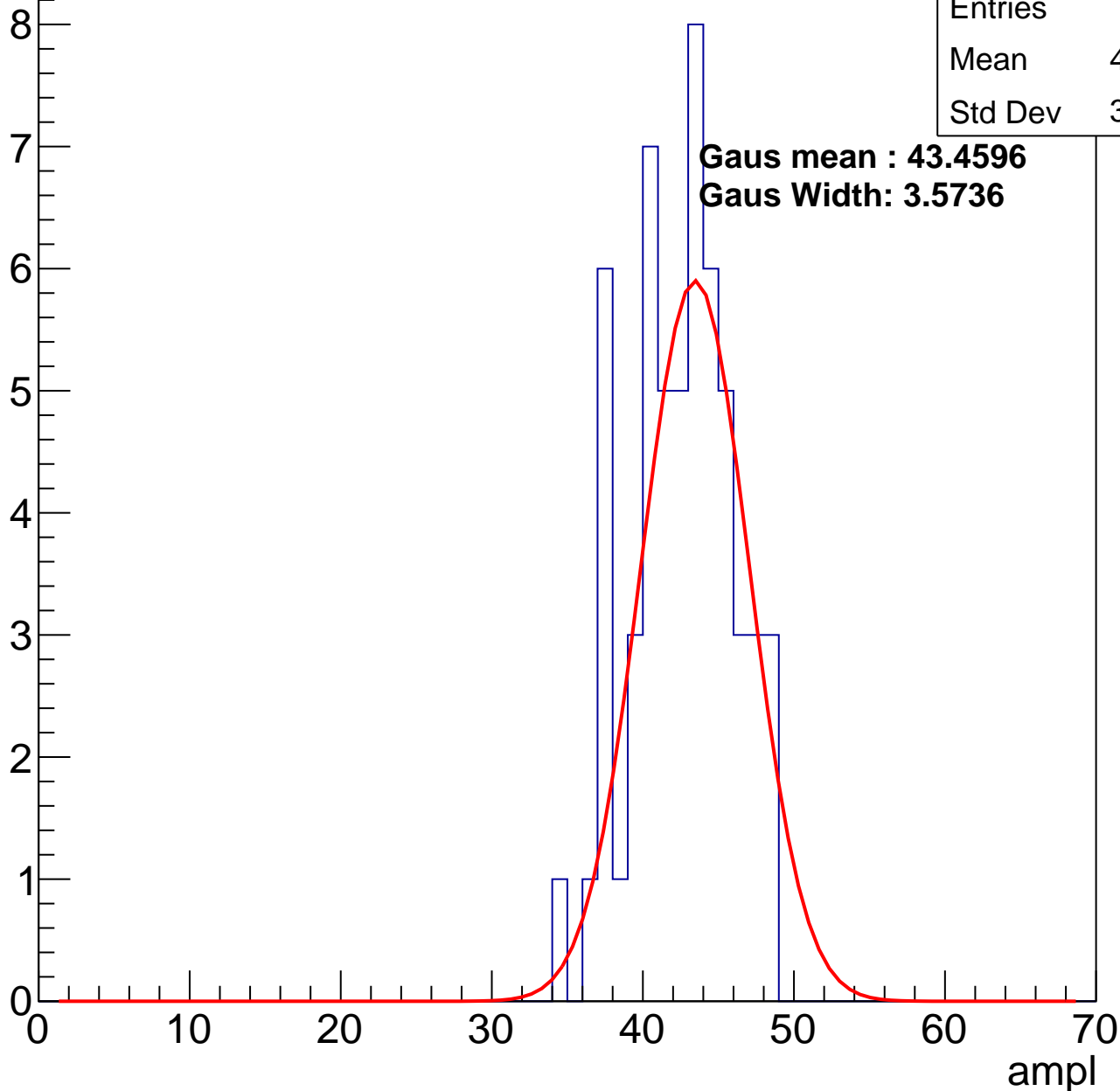
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	42.07
Std Dev	3.334

**Gaus mean : 43.4596**

**Gaus Width: 3.5736**



# B1L103S, U21-ch104, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	75
Mean	48.44
Std Dev	3.967

Entry

10

8

6

4

2

0

0

10

20

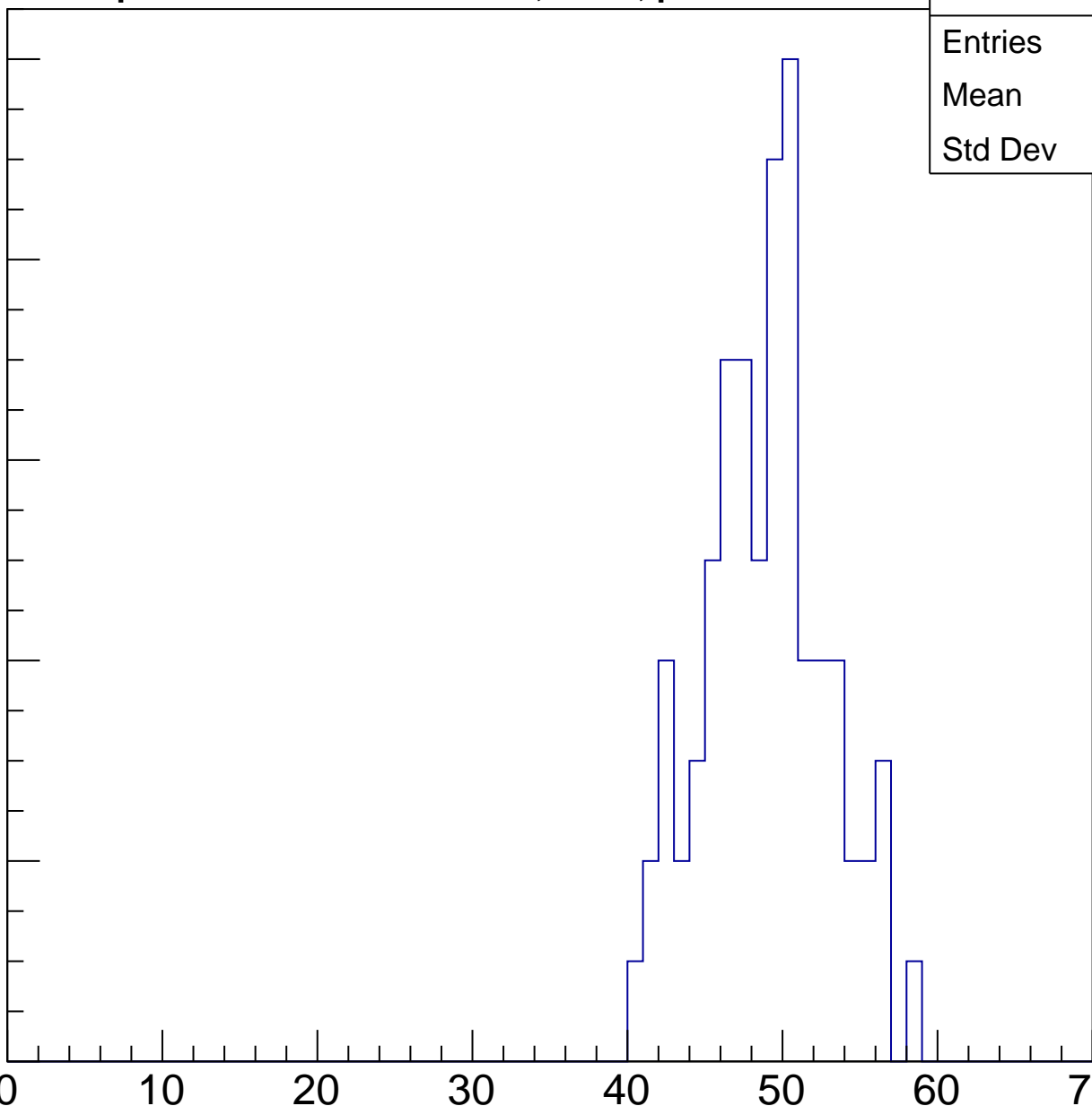
30

40

50

60

ampl

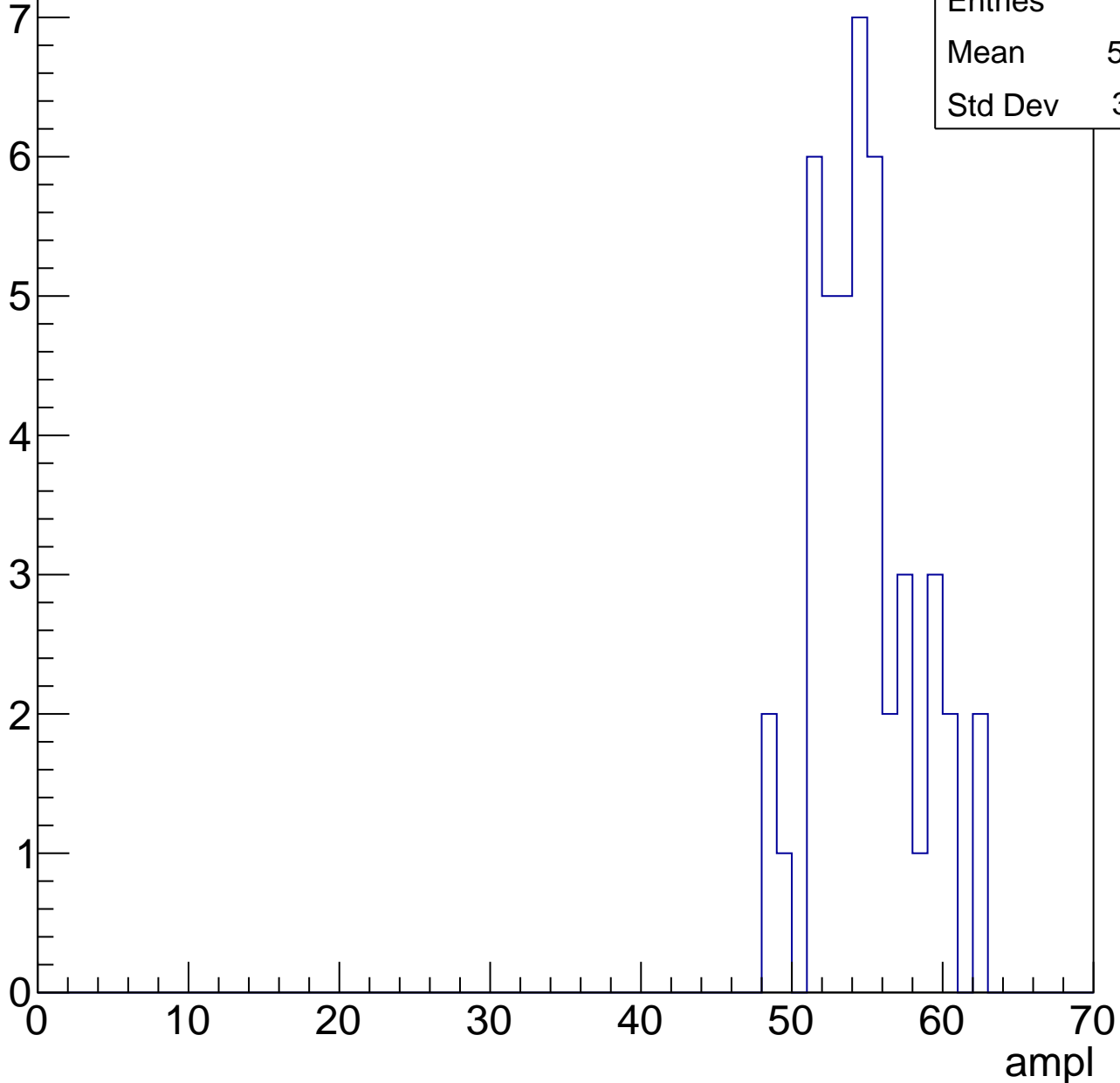


# B1L103S, U21-ch104, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

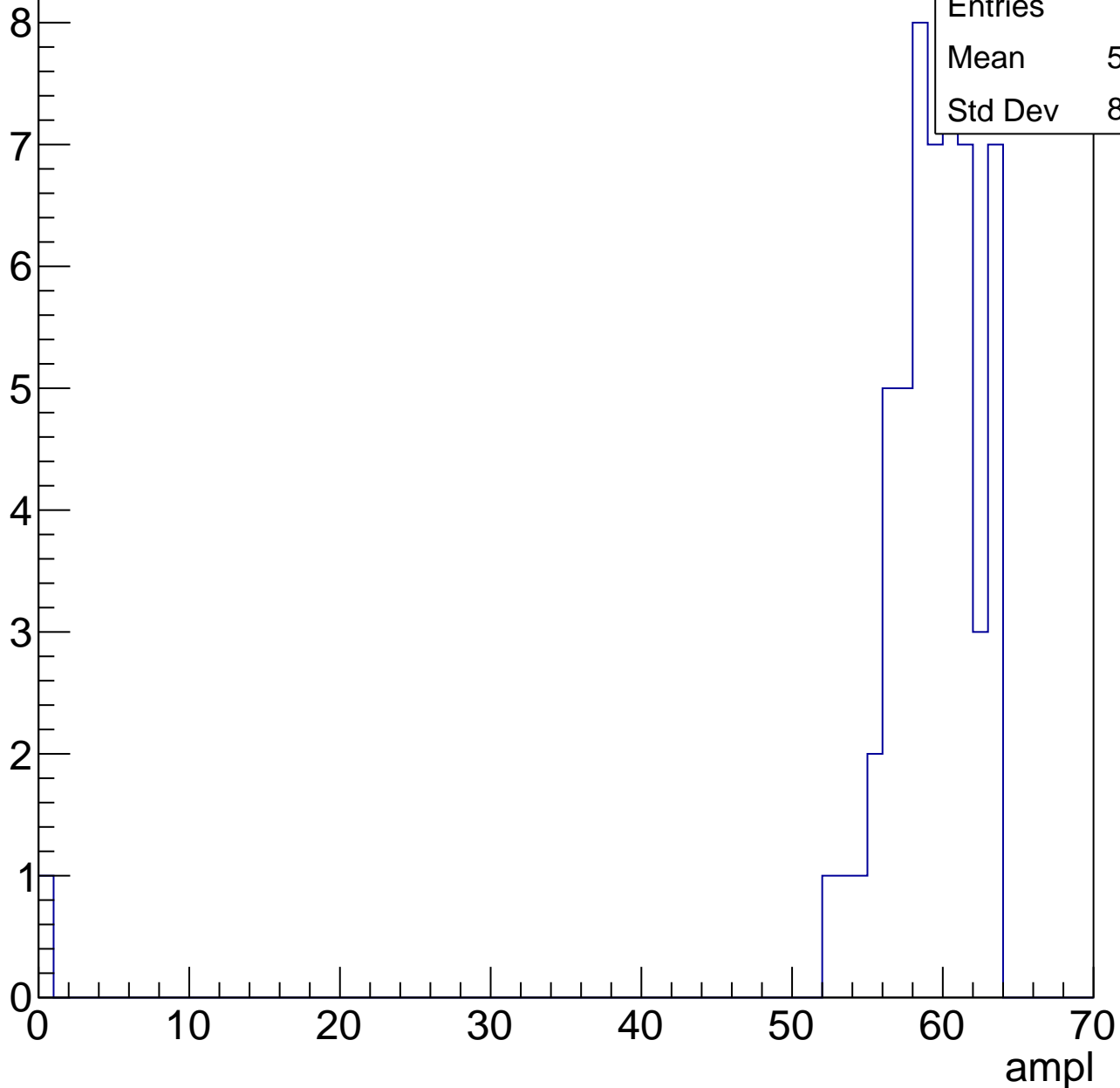
Entries	45
Mean	54.36
Std Dev	3.341



# B1L103S, U21-ch104, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

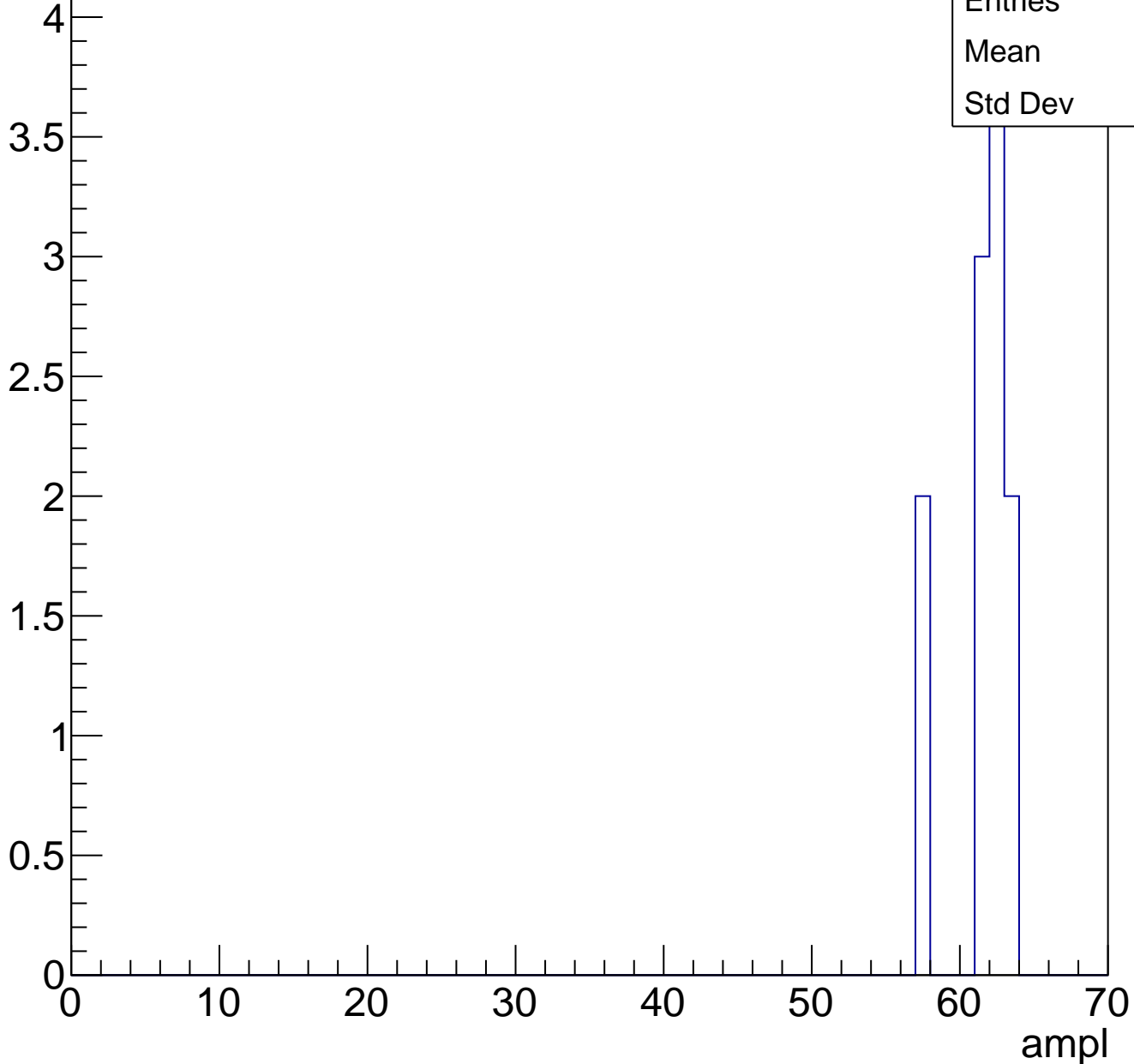


Entries	56
Mean	57.95
Std Dev	8.247

# B1L103S, U21-ch104, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U21-ch104, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U21-ch105, adc0

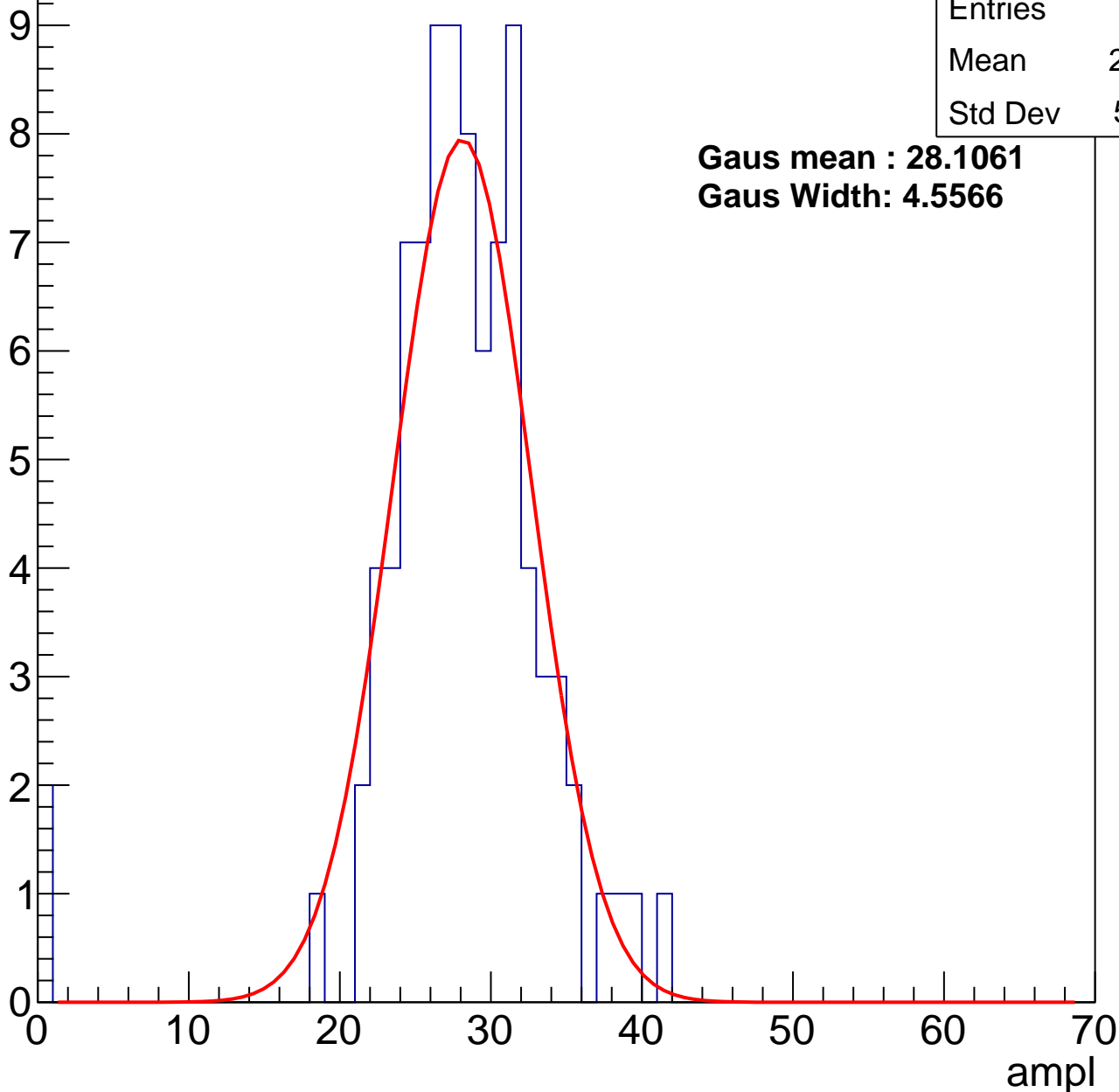
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	91
Mean	27.48
Std Dev	5.871

**Gaus mean : 28.1061**

**Gaus Width: 4.5566**



# B1L103S, U21-ch105, adc1

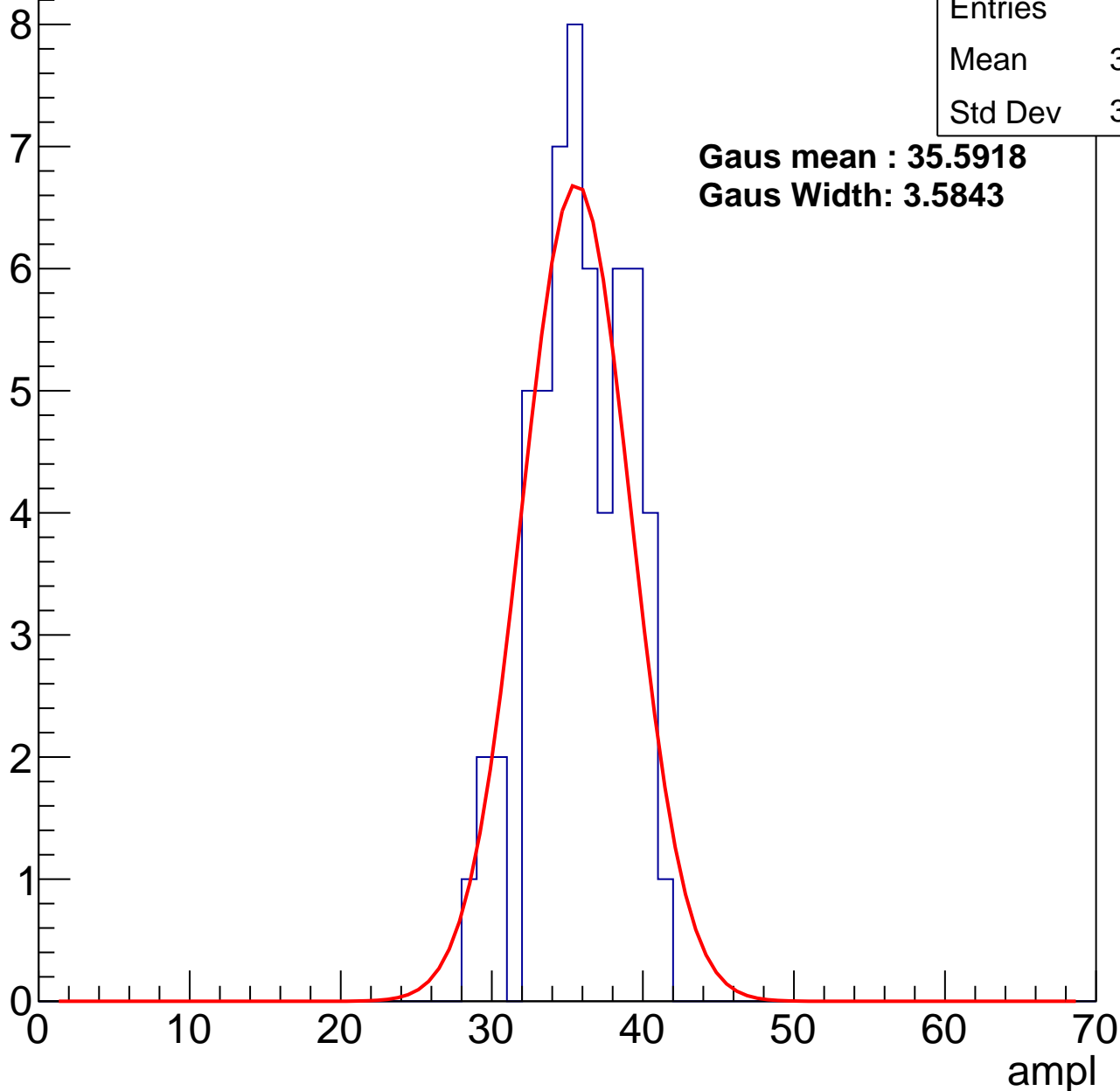
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	35.37
Std Dev	3.087

**Gaus mean : 35.5918**

**Gaus Width: 3.5843**



# B1L103S, U21-ch105, adc2

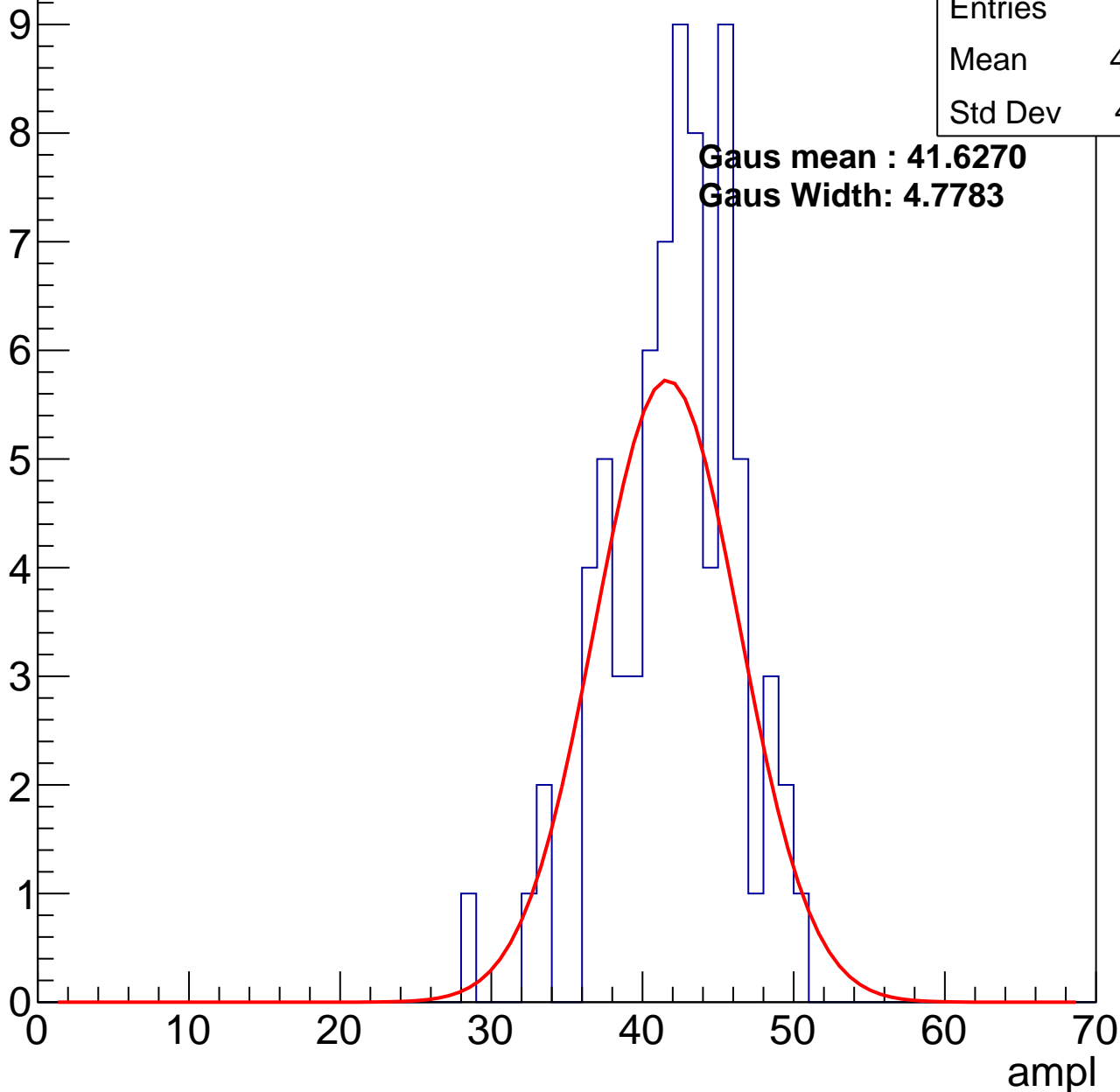
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	41.69
Std Dev	4.201

**Gaus mean : 41.6270**

**Gaus Width: 4.7783**

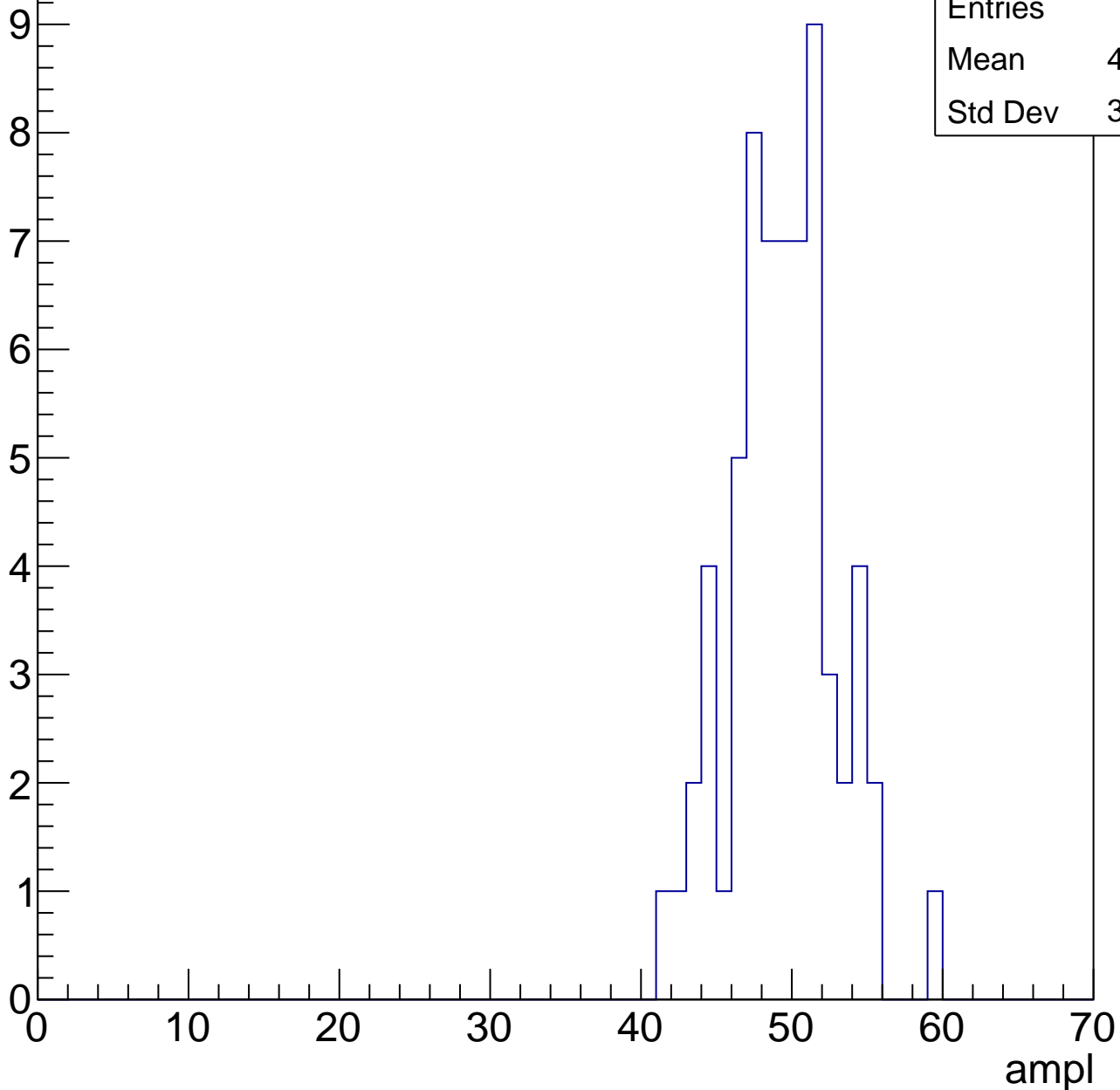


# B1L103S, U21-ch105, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

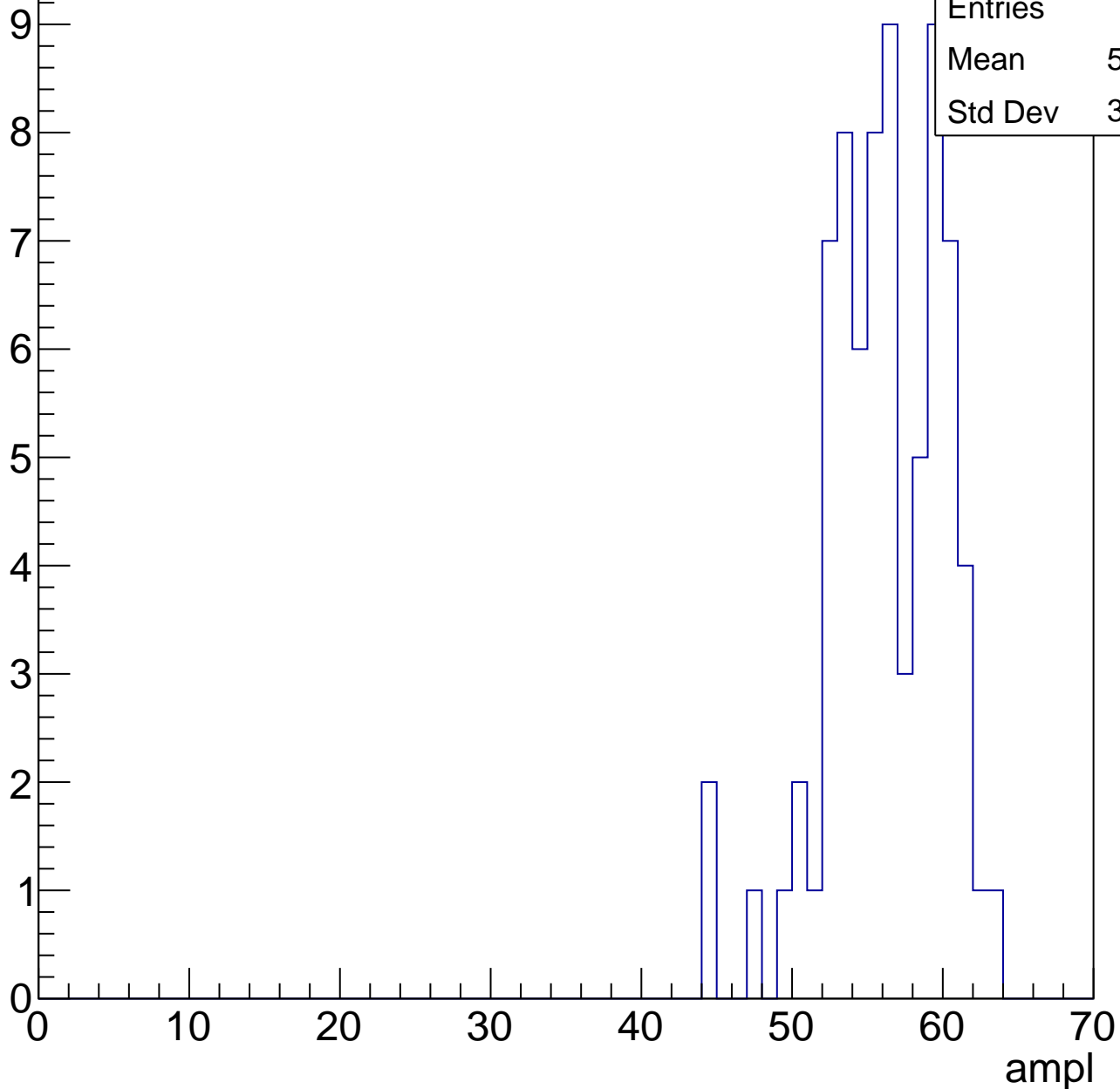
Entries	64
Mean	48.92
Std Dev	3.443



# B1L103S, U21-ch105, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

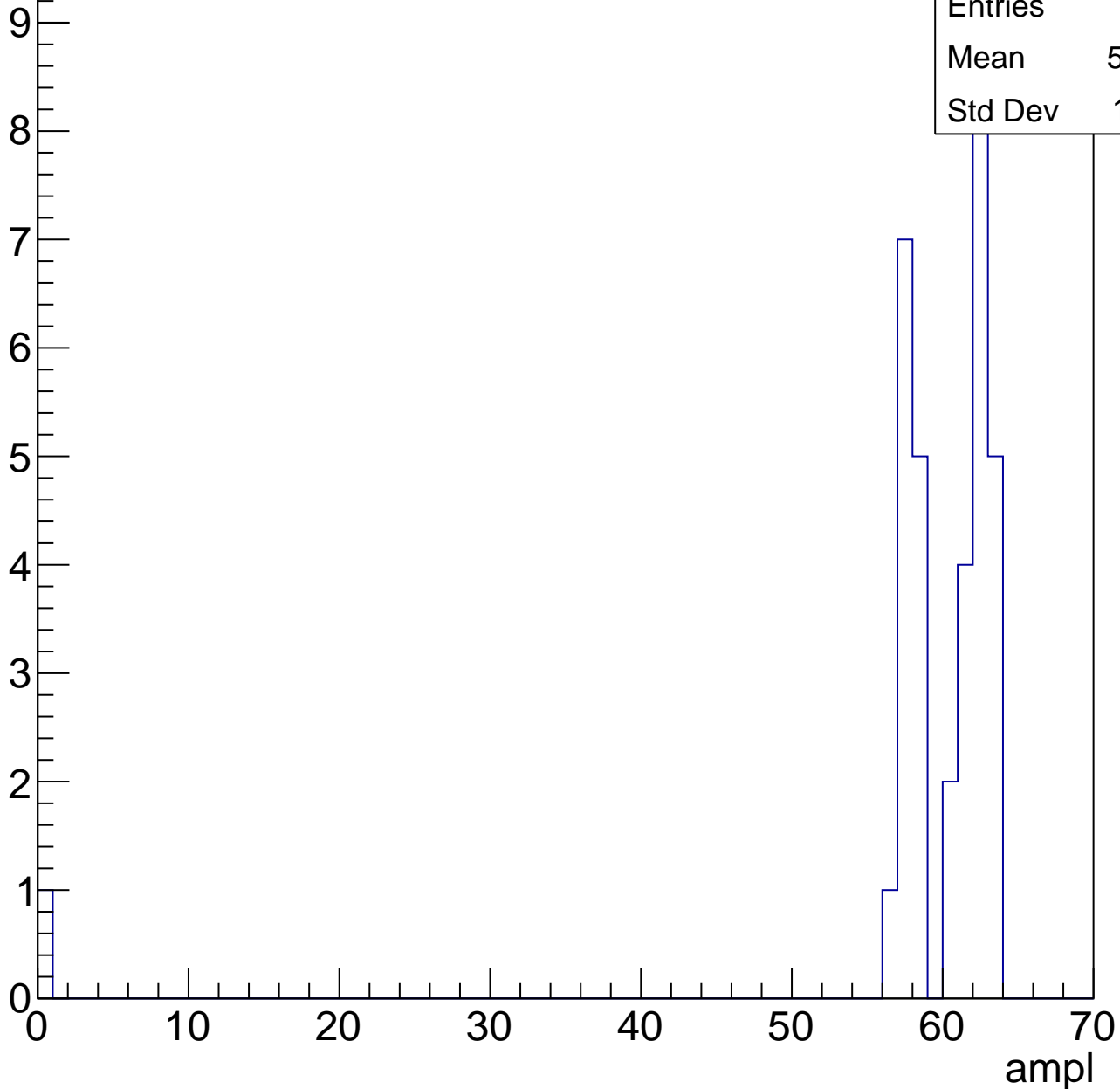


# B1L103S, U21-ch105, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

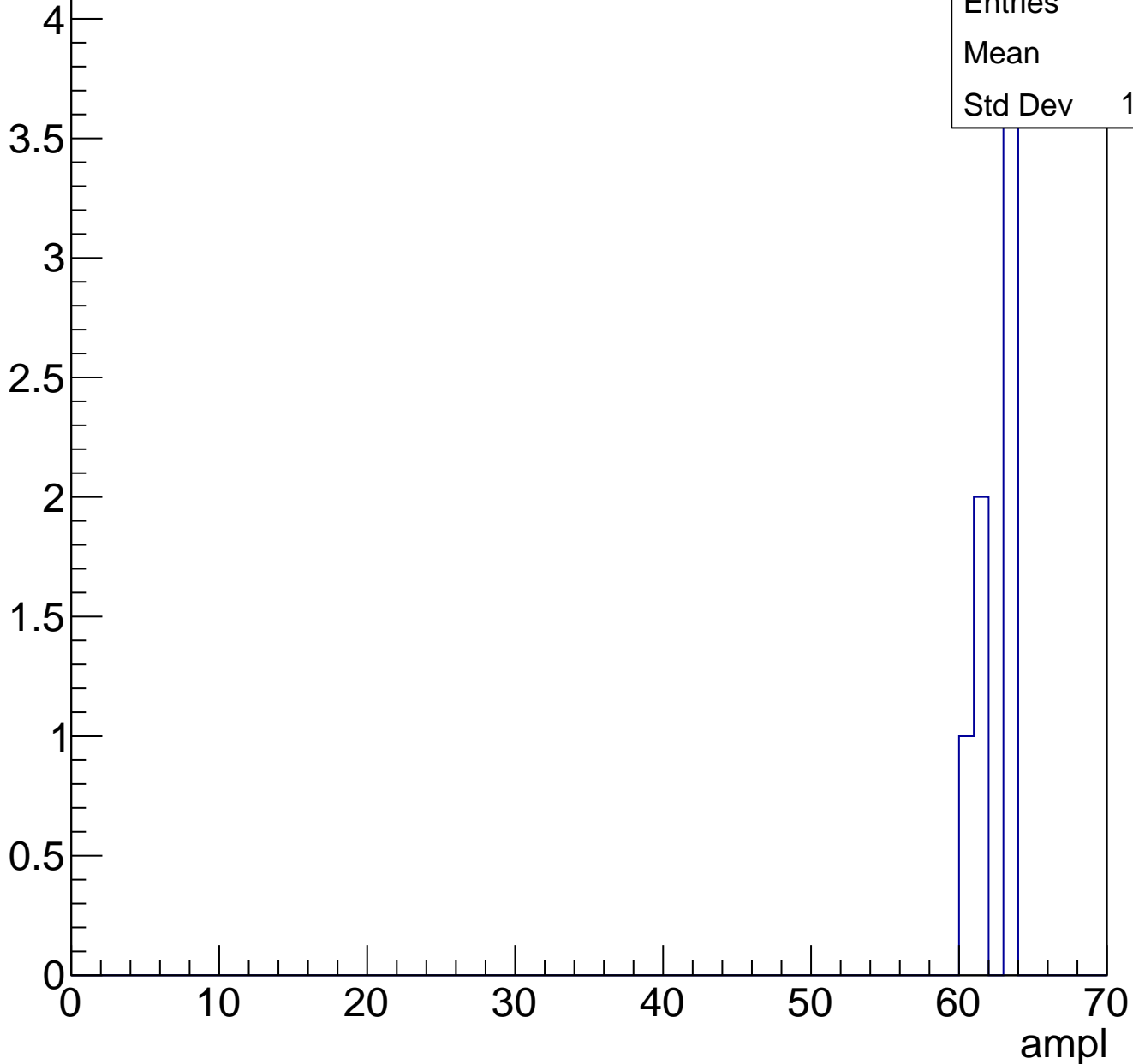
Entries	34
Mean	58.29
Std Dev	10.41



# B1L103S, U21-ch105, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U21-ch105, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L103S, U21-ch106, adc0

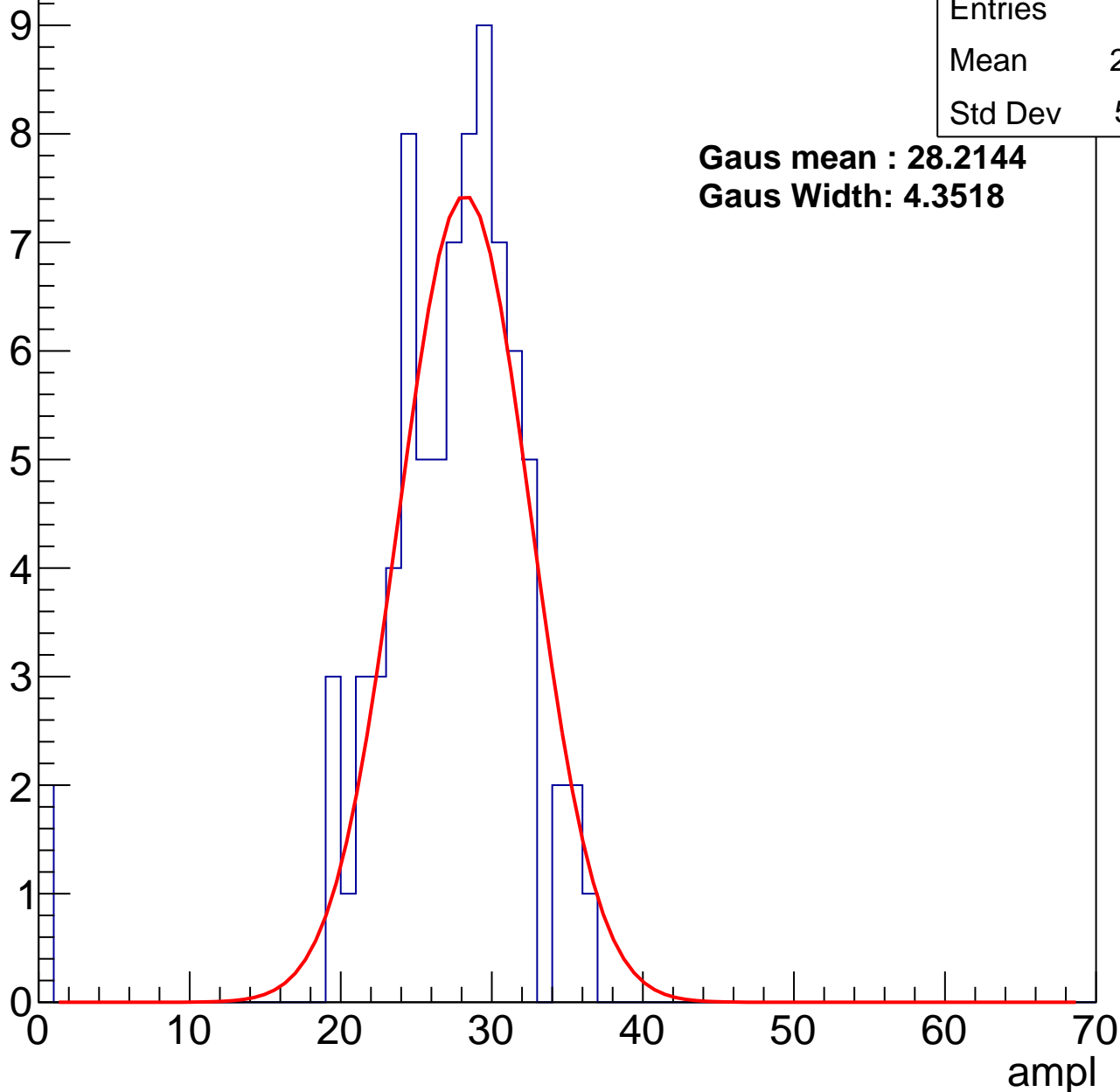
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	81
Mean	26.53
Std Dev	5.731

**Gaus mean : 28.2144**

**Gaus Width: 4.3518**



# B1L103S, U21-ch106, adc1

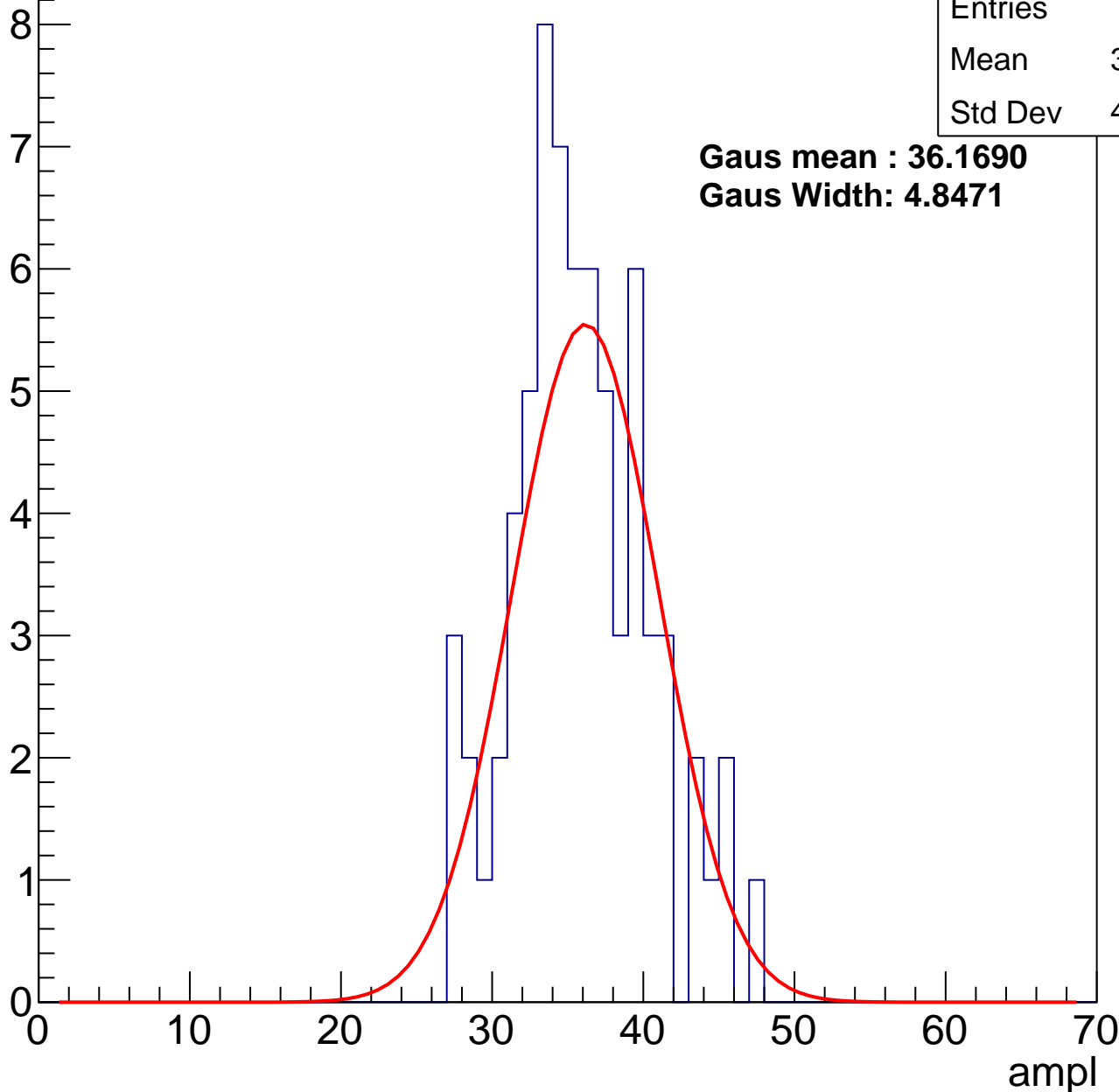
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	35.44
Std Dev	4.465

**Gaus mean : 36.1690**

**Gaus Width: 4.8471**



# B1L103S, U21-ch106, adc2

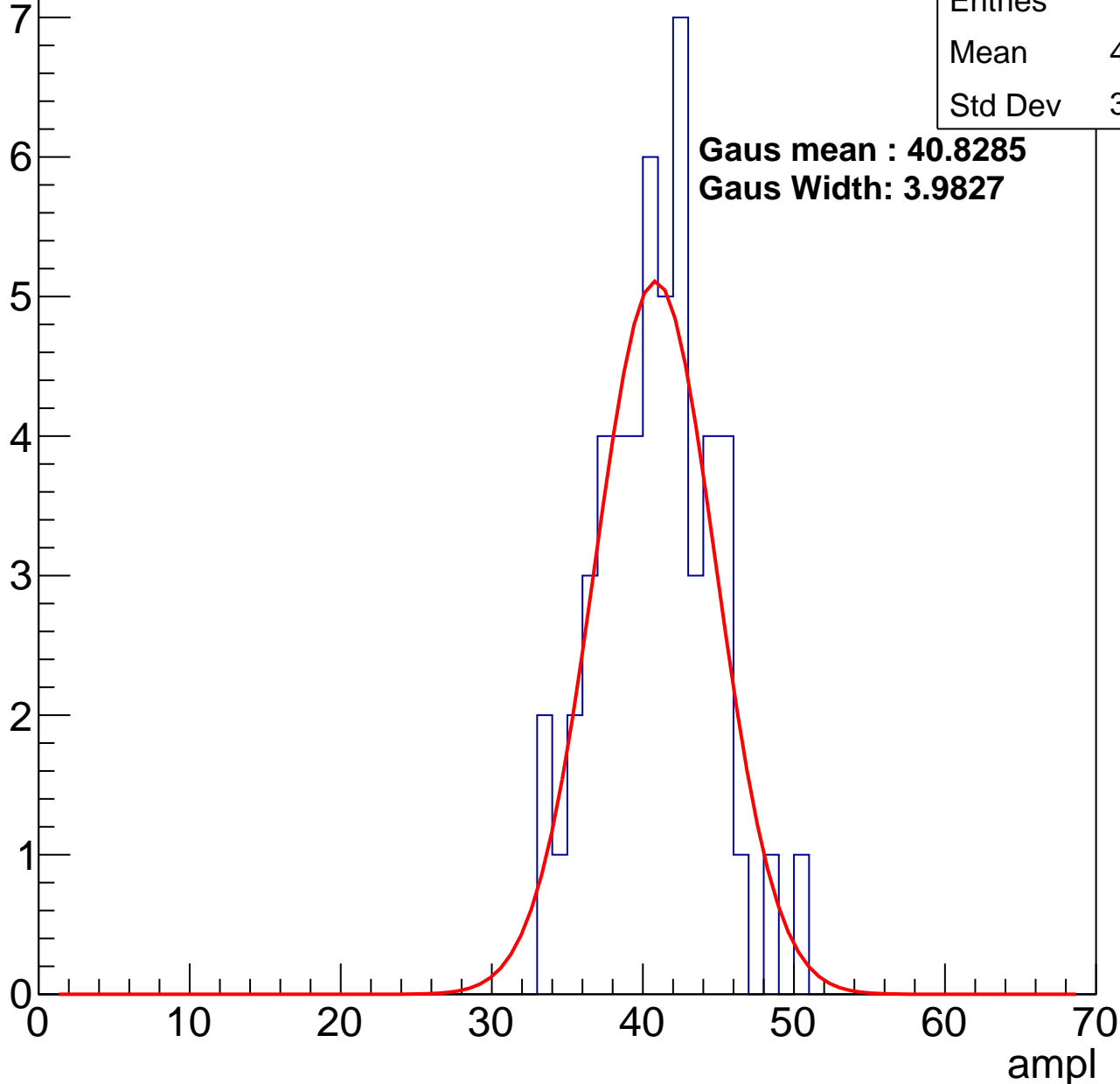
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	40.42
Std Dev	3.676

**Gaus mean : 40.8285**

**Gaus Width: 3.9827**

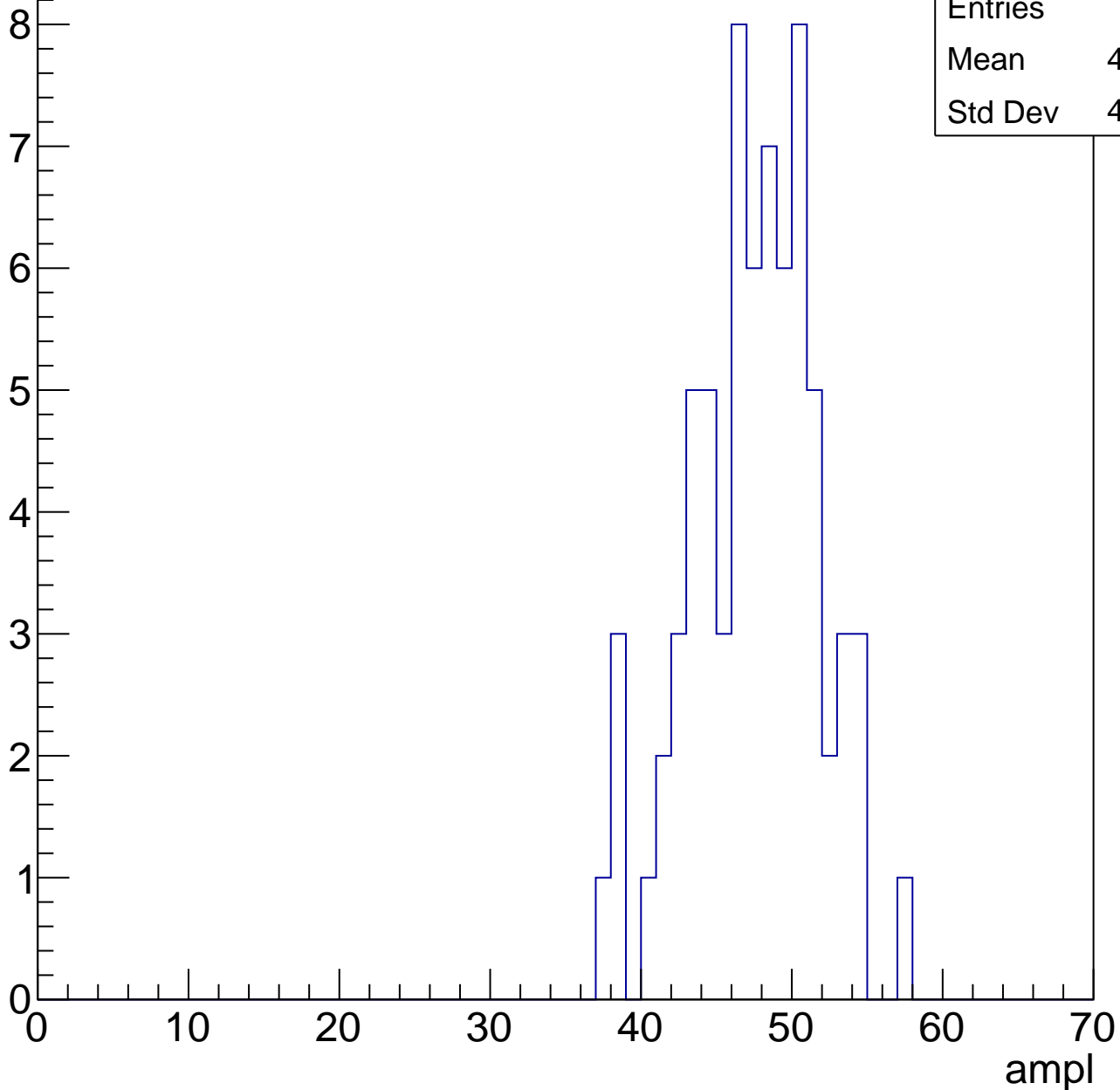


# B1L103S, U21-ch106, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	47.03
Std Dev	4.203

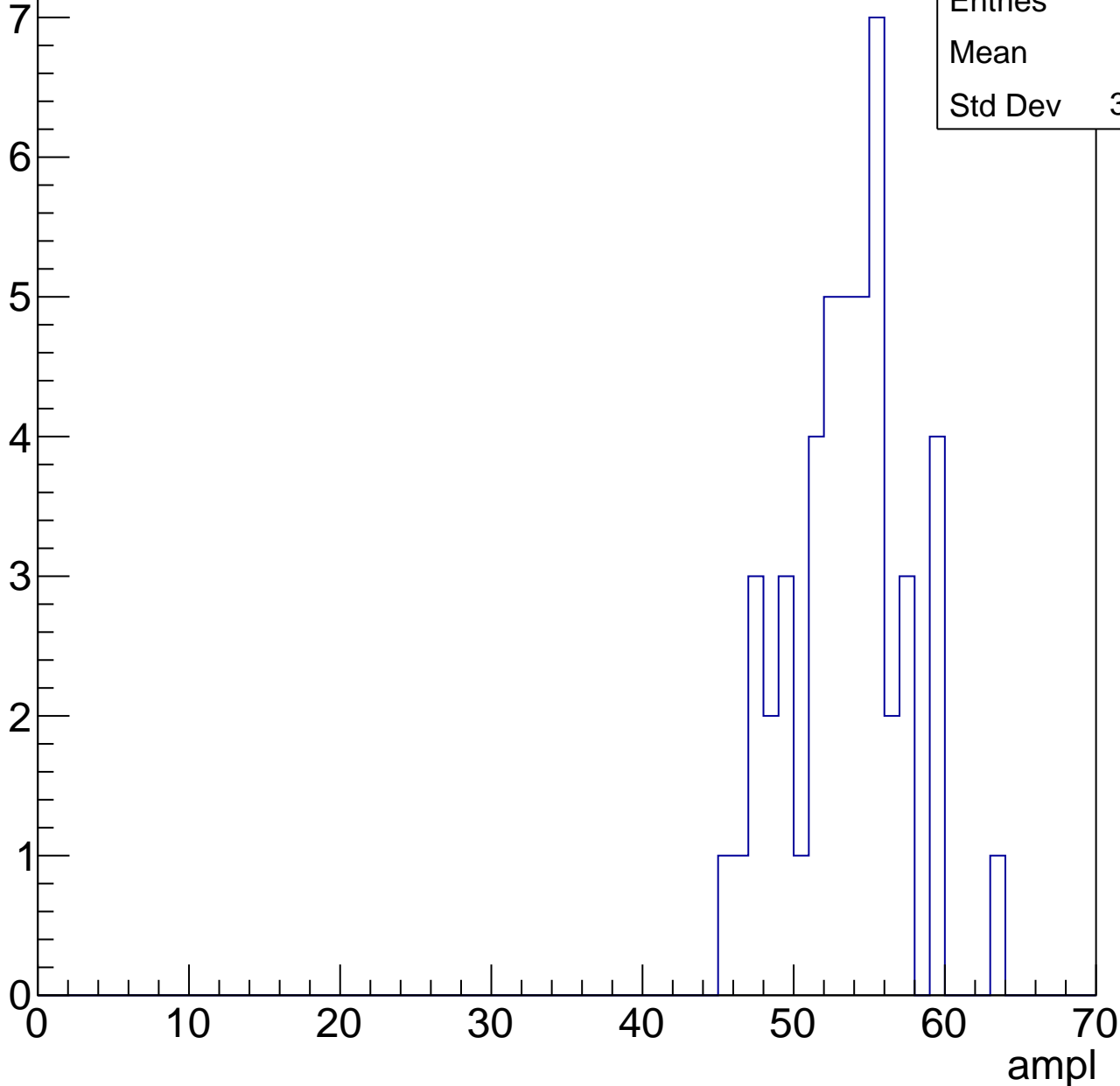


# B1L103S, U21-ch106, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	47
Mean	53
Std Dev	3.837

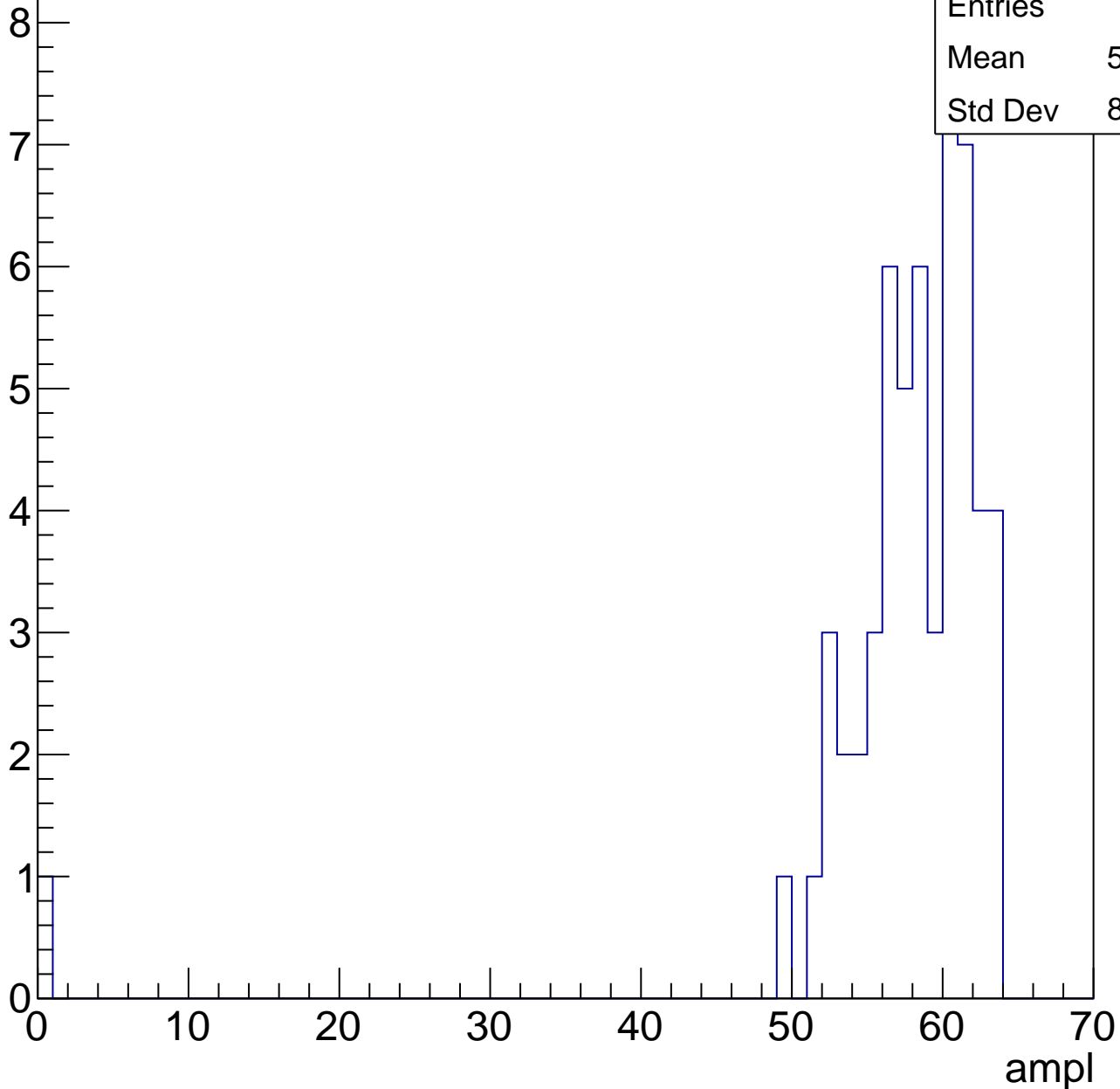


# B1L103S, U21-ch106, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	56.93
Std Dev	8.385

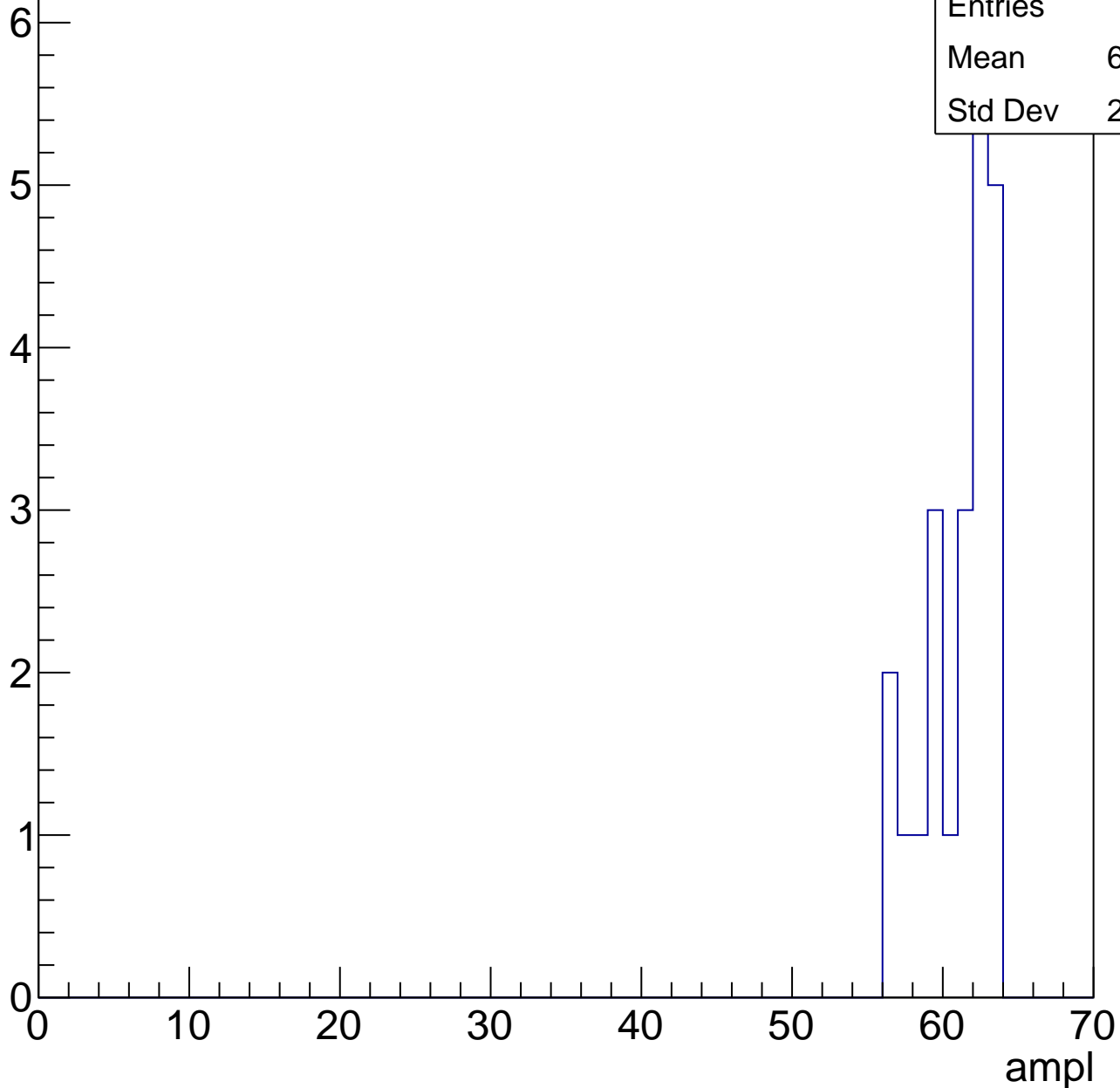


# B1L103S, U21-ch106, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	22
Mean	60.64
Std Dev	2.247

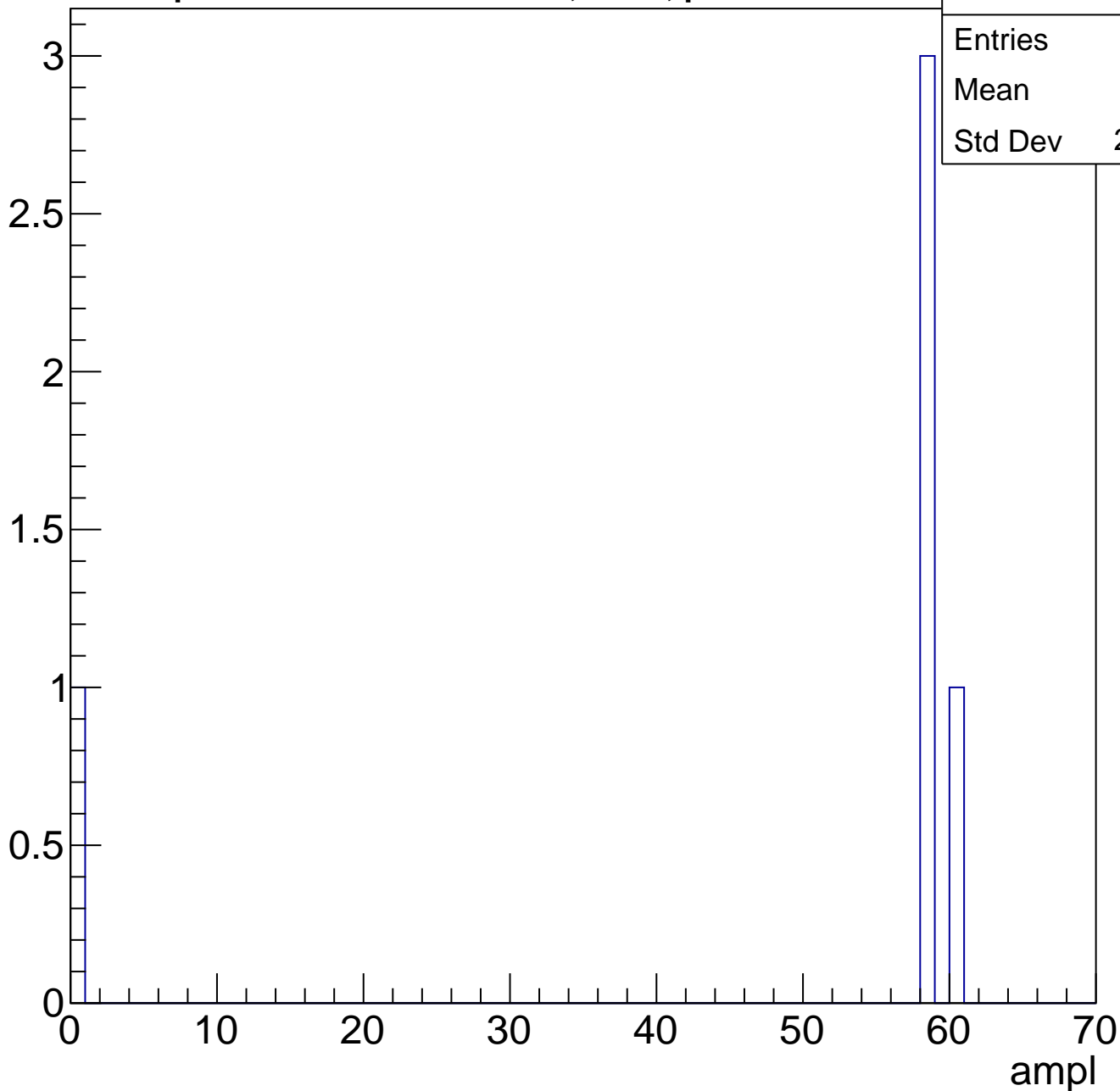




# B1L103S, U21-ch106, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	5
Mean	46.8
Std Dev	23.41

# B1L103S, U21-ch107, adc0

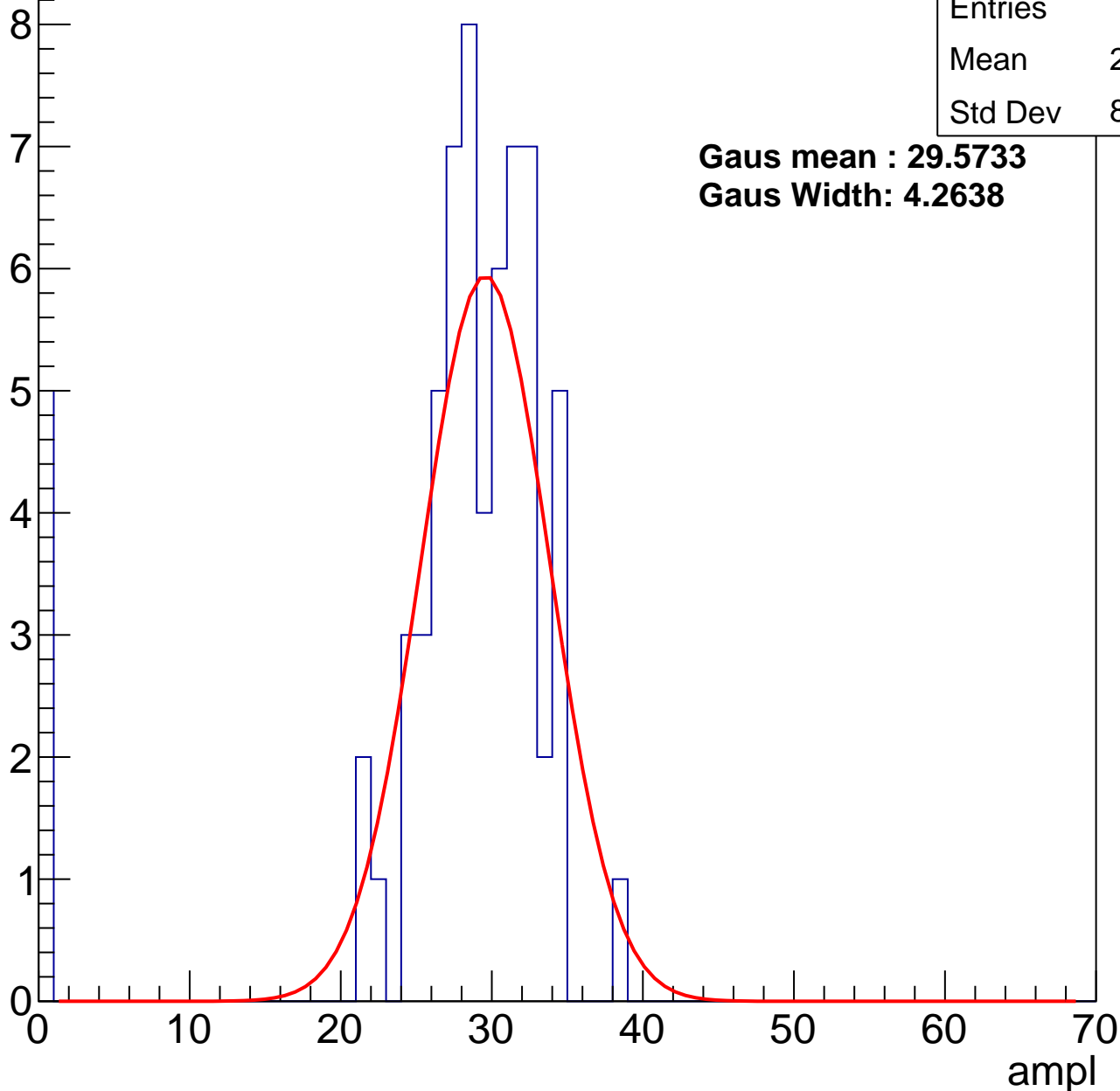
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	26.74
Std Dev	8.335

**Gaus mean : 29.5733**

**Gaus Width: 4.2638**



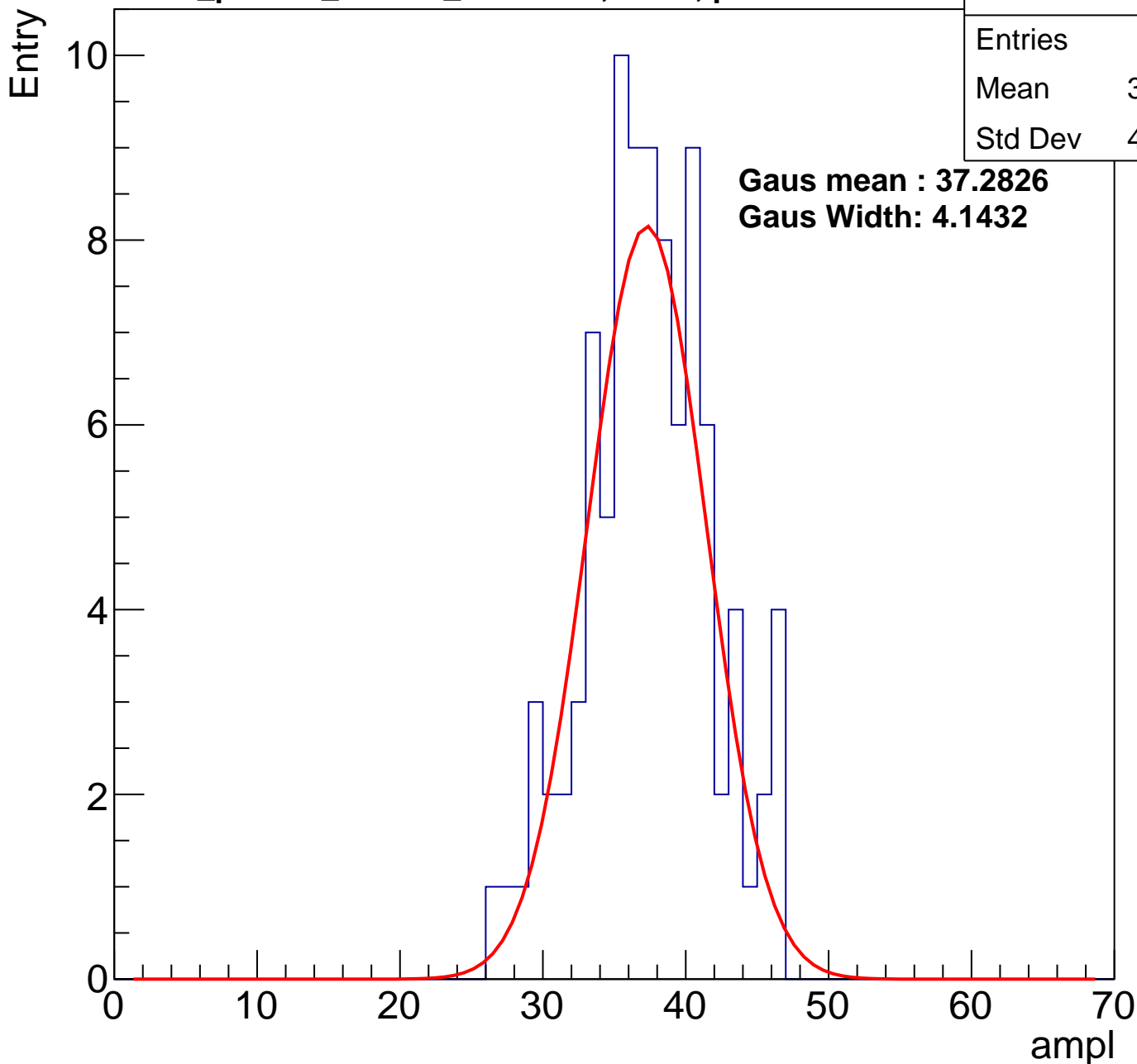
# B1L103S, U21-ch107, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	95
Mean	36.97
Std Dev	4.412

**Gaus mean : 37.2826**

**Gaus Width: 4.1432**



# B1L103S, U21-ch107, adc2

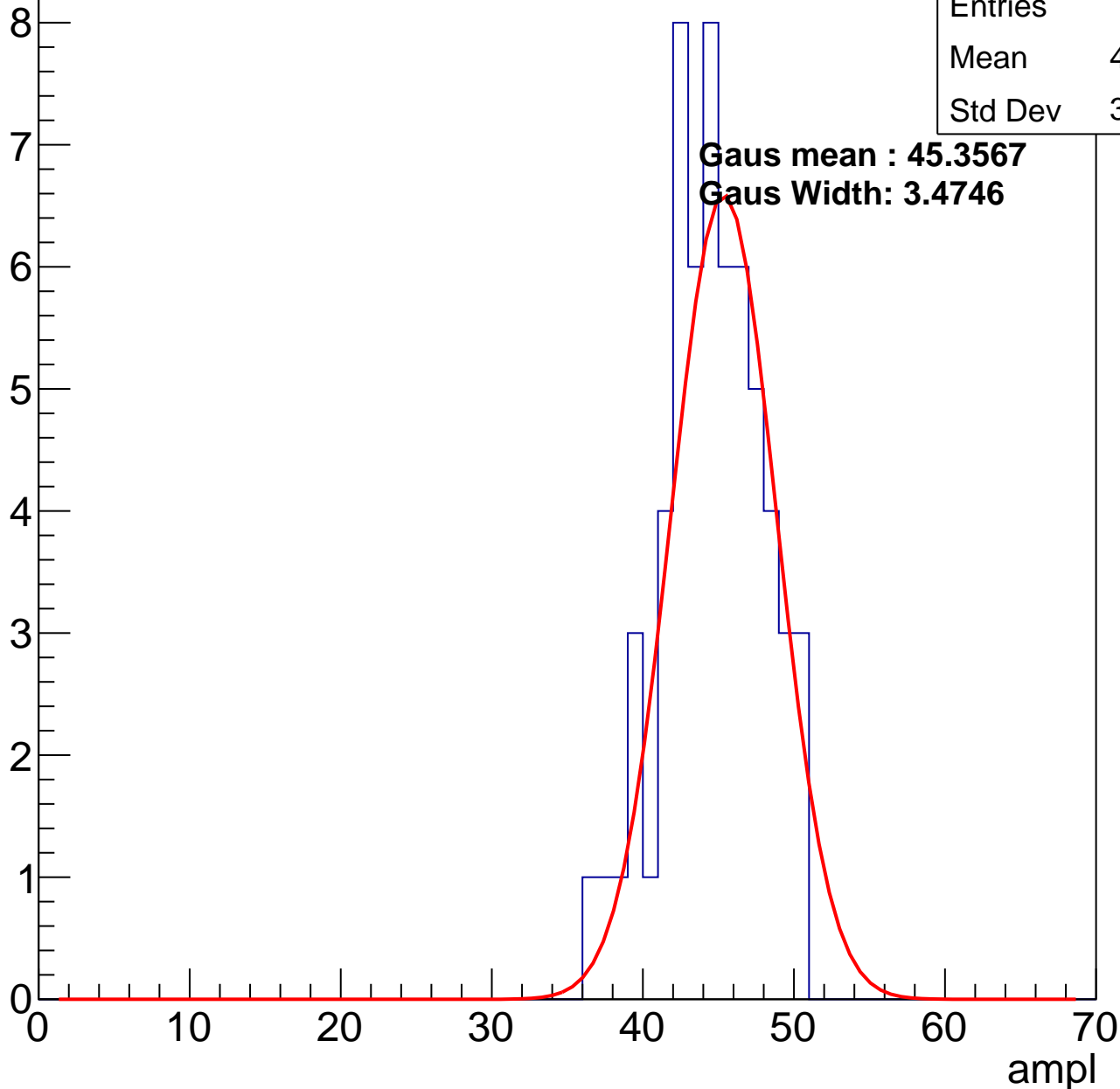
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	44.13
Std Dev	3.253

**Gaus mean : 45.3567**

**Gaus Width: 3.4746**

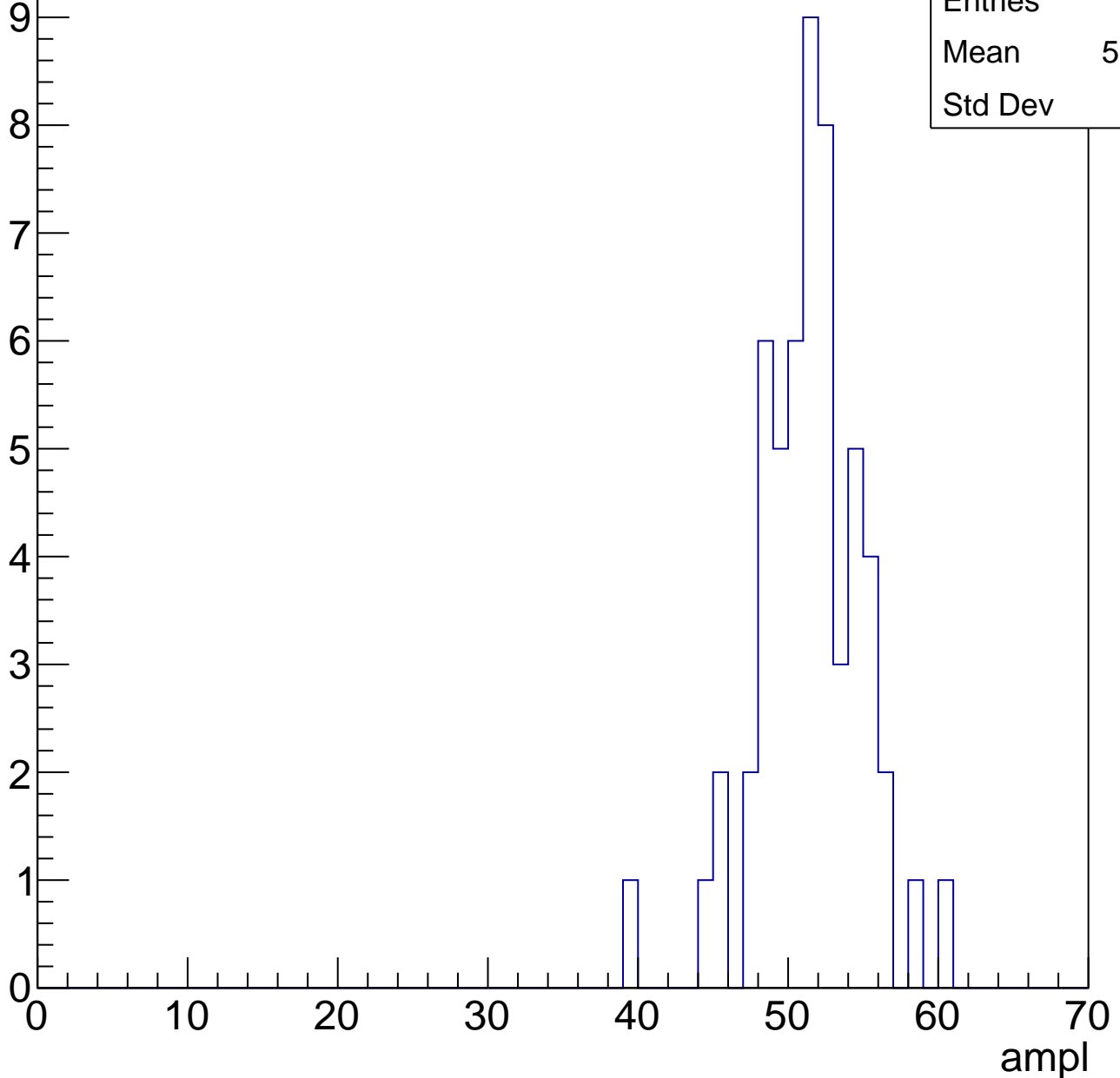


# B1L103S, U21-ch107, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	50.96
Std Dev	3.5

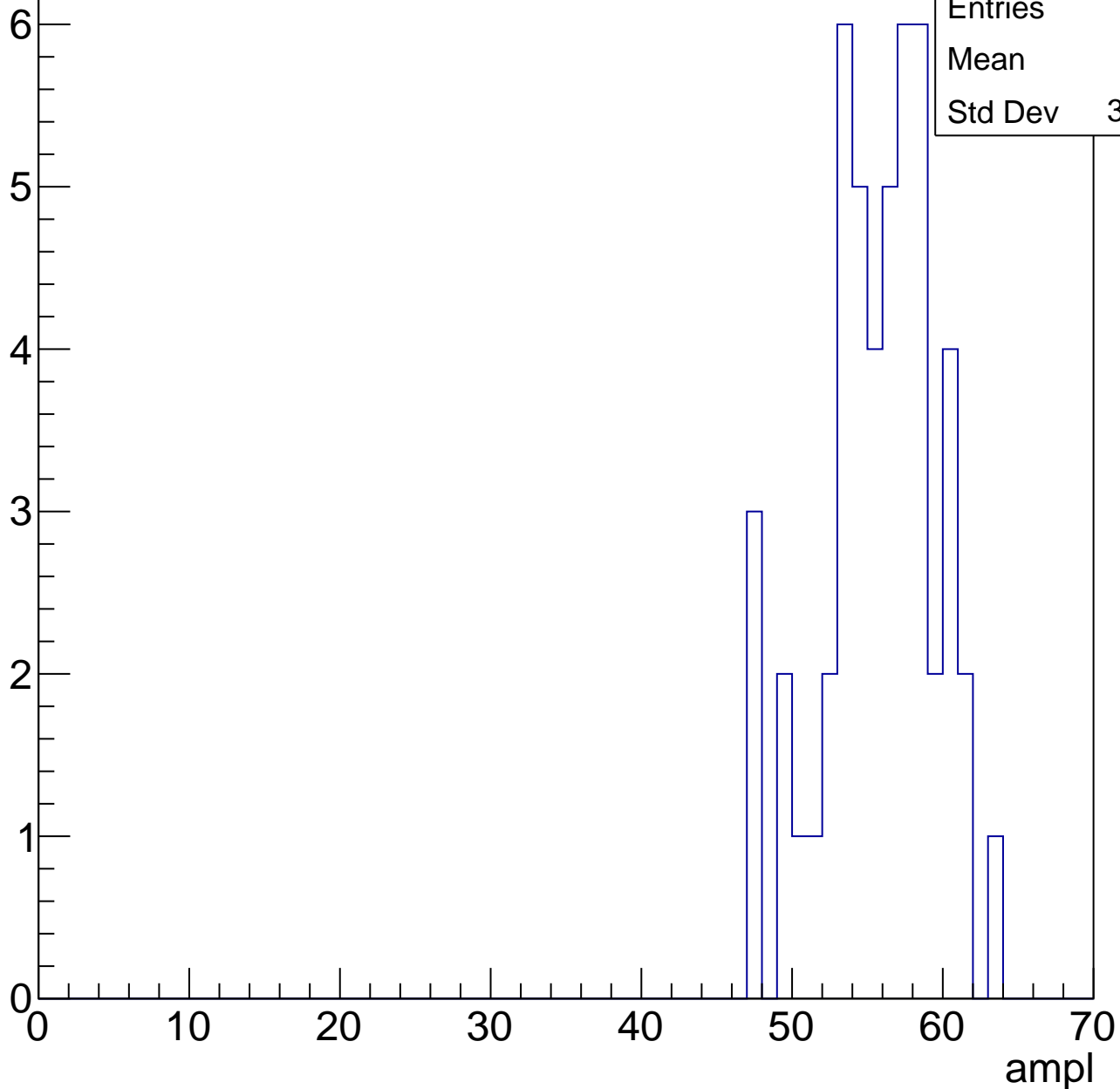


# B1L103S, U21-ch107, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	55.3
Std Dev	3.738

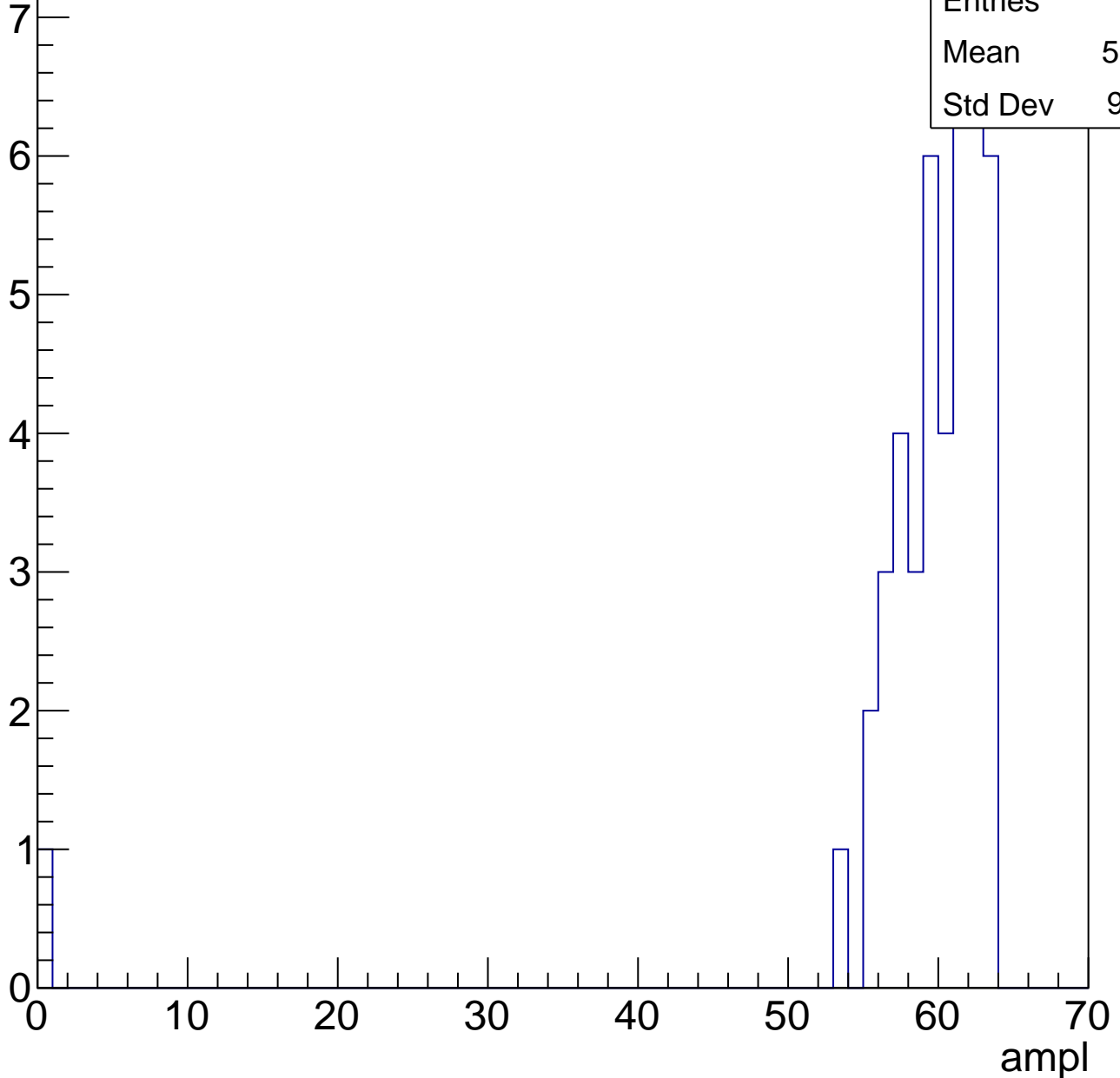


# B1L103S, U21-ch107, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

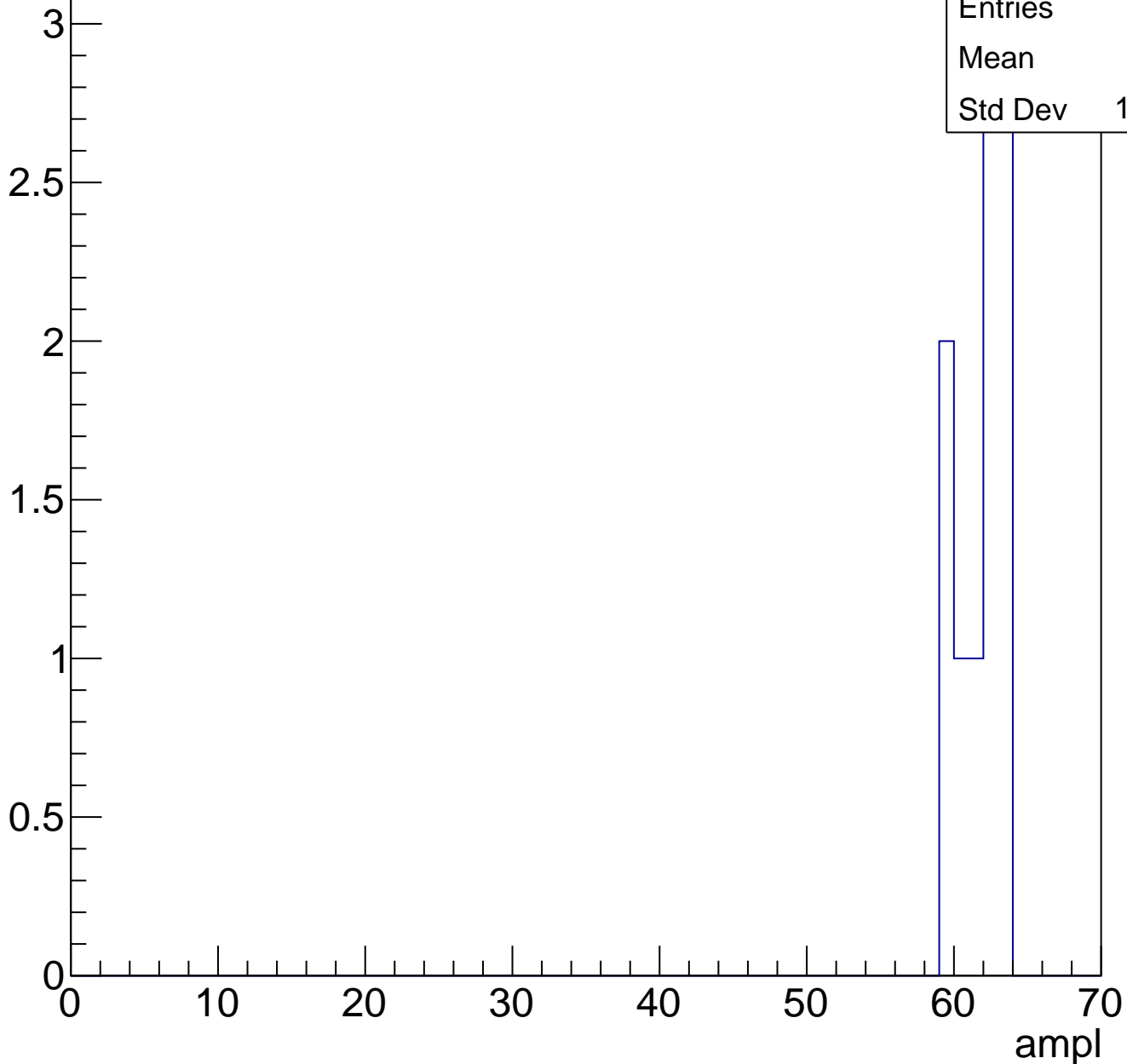
Entries	44
Mean	58.32
Std Dev	9.251



# B1L103S, U21-ch107, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U21-ch107, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U21-ch108, adc0

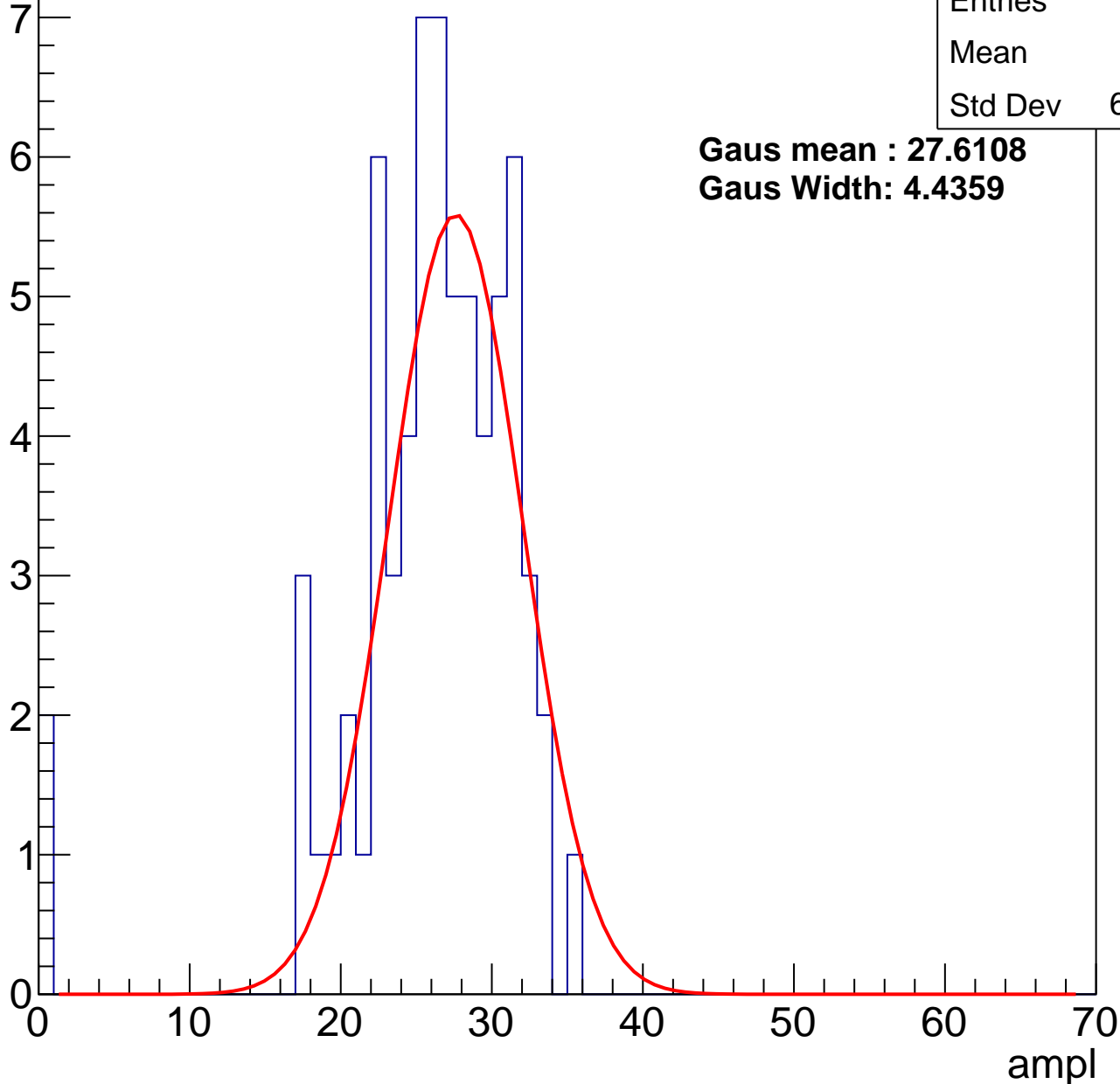
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	25.4
Std Dev	6.069

**Gaus mean : 27.6108**

**Gaus Width: 4.4359**



# B1L103S, U21-ch108, adc1

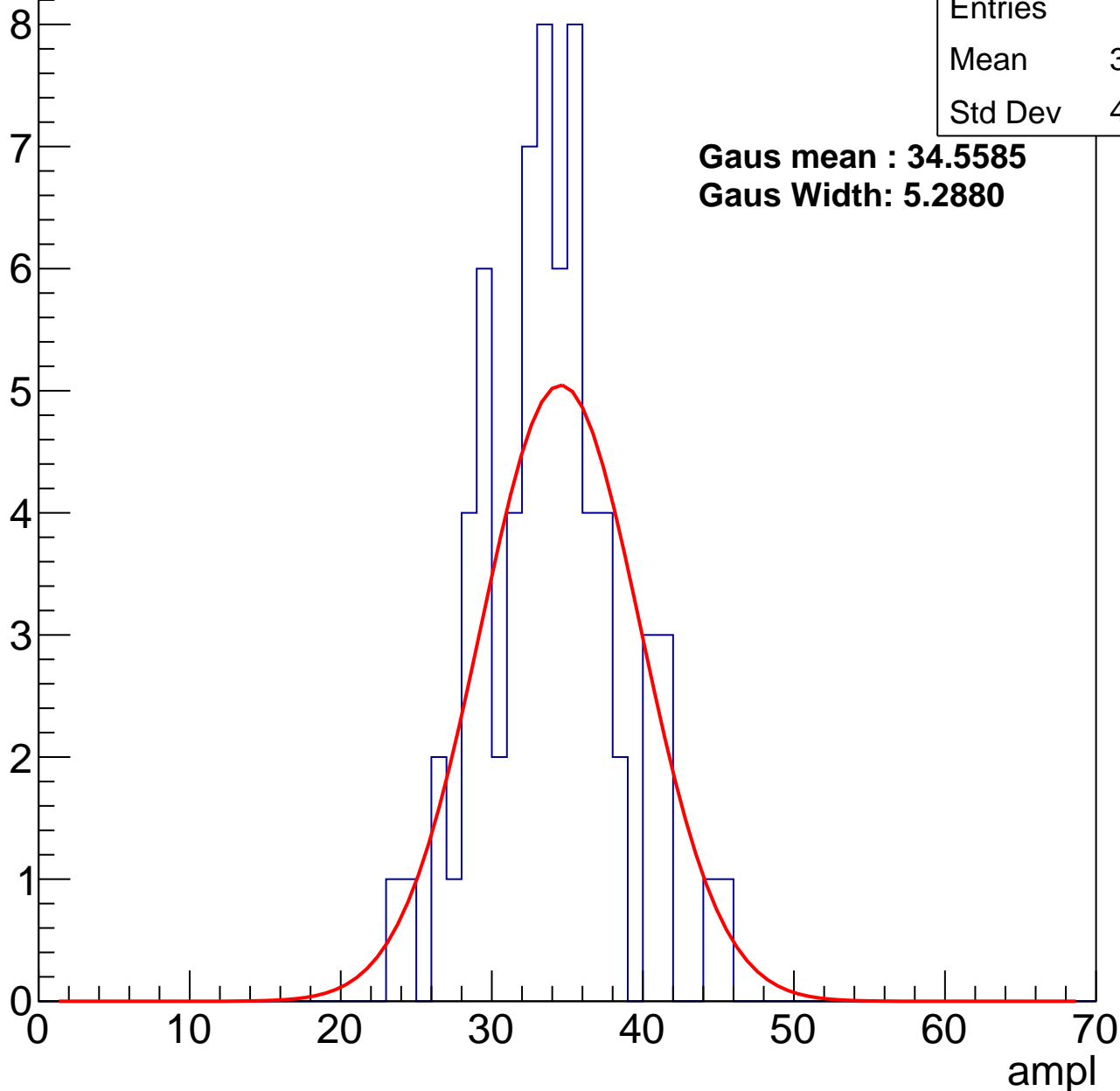
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	33.35
Std Dev	4.432

**Gaus mean : 34.5585**

**Gaus Width: 5.2880**



# B1L103S, U21-ch108, adc2

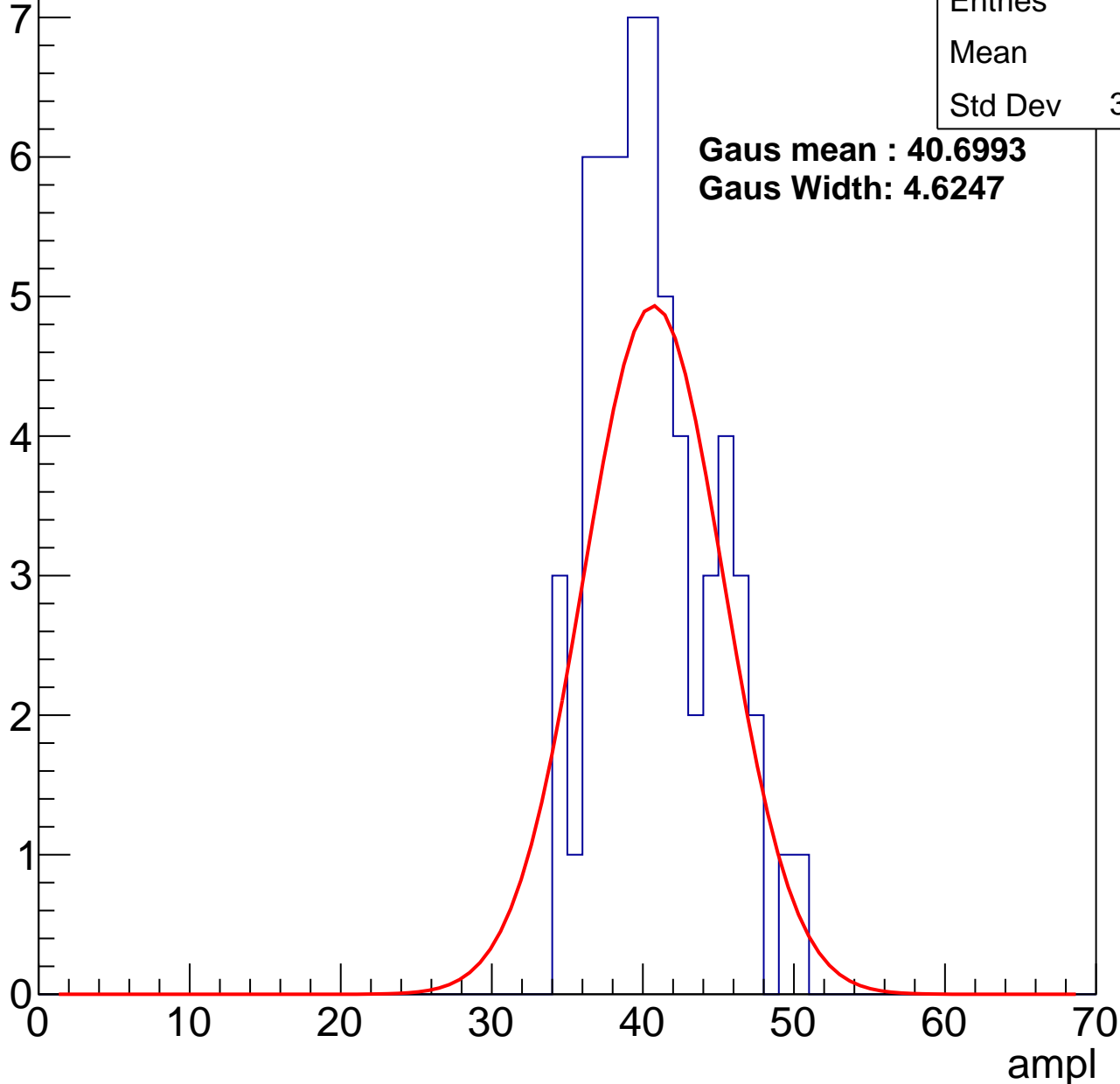
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	40.3
Std Dev	3.804

**Gaus mean : 40.6993**

**Gaus Width: 4.6247**

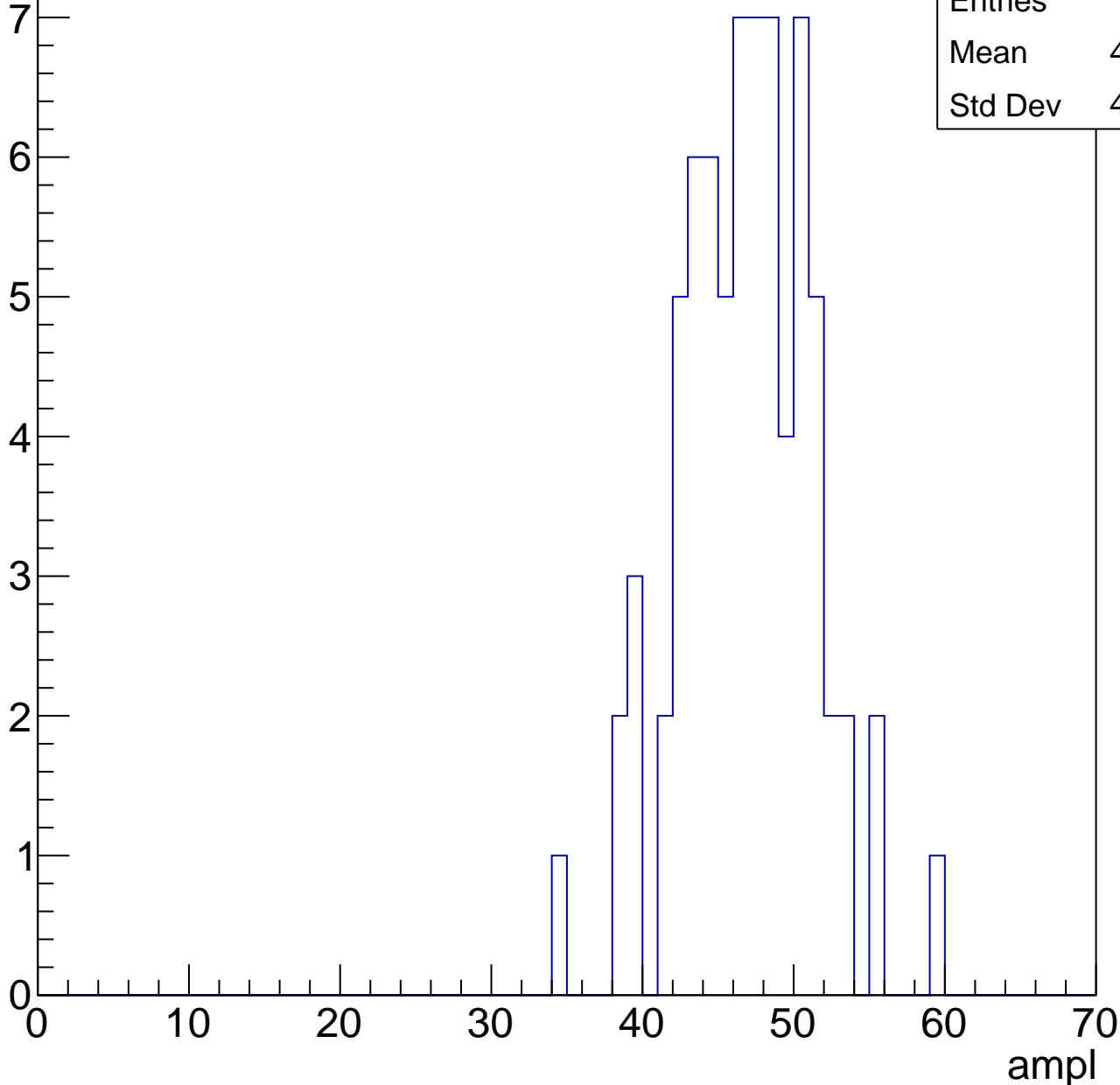


# B1L103S, U21-ch108, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	46.39
Std Dev	4.395

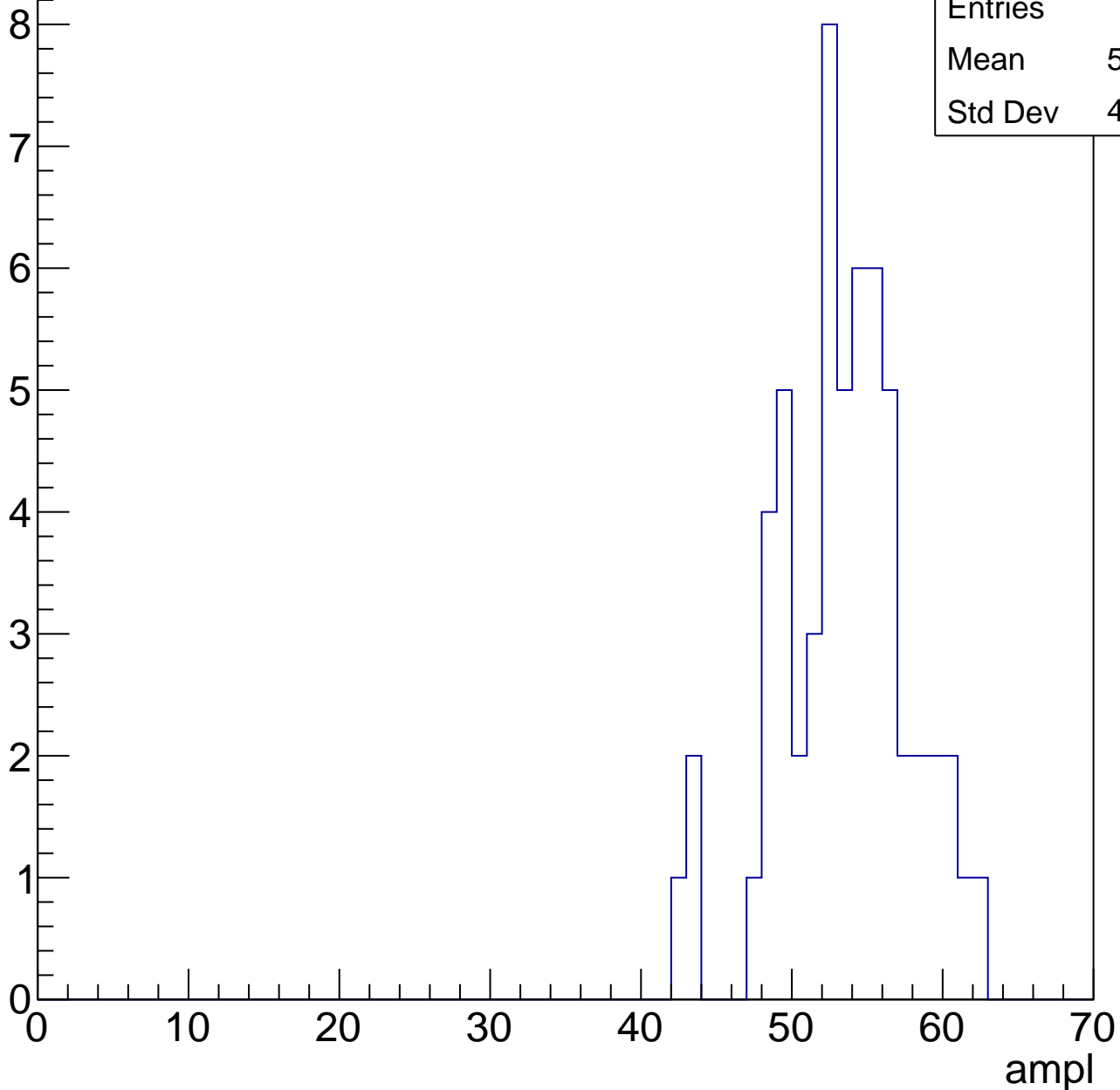


# B1L103S, U21-ch108, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

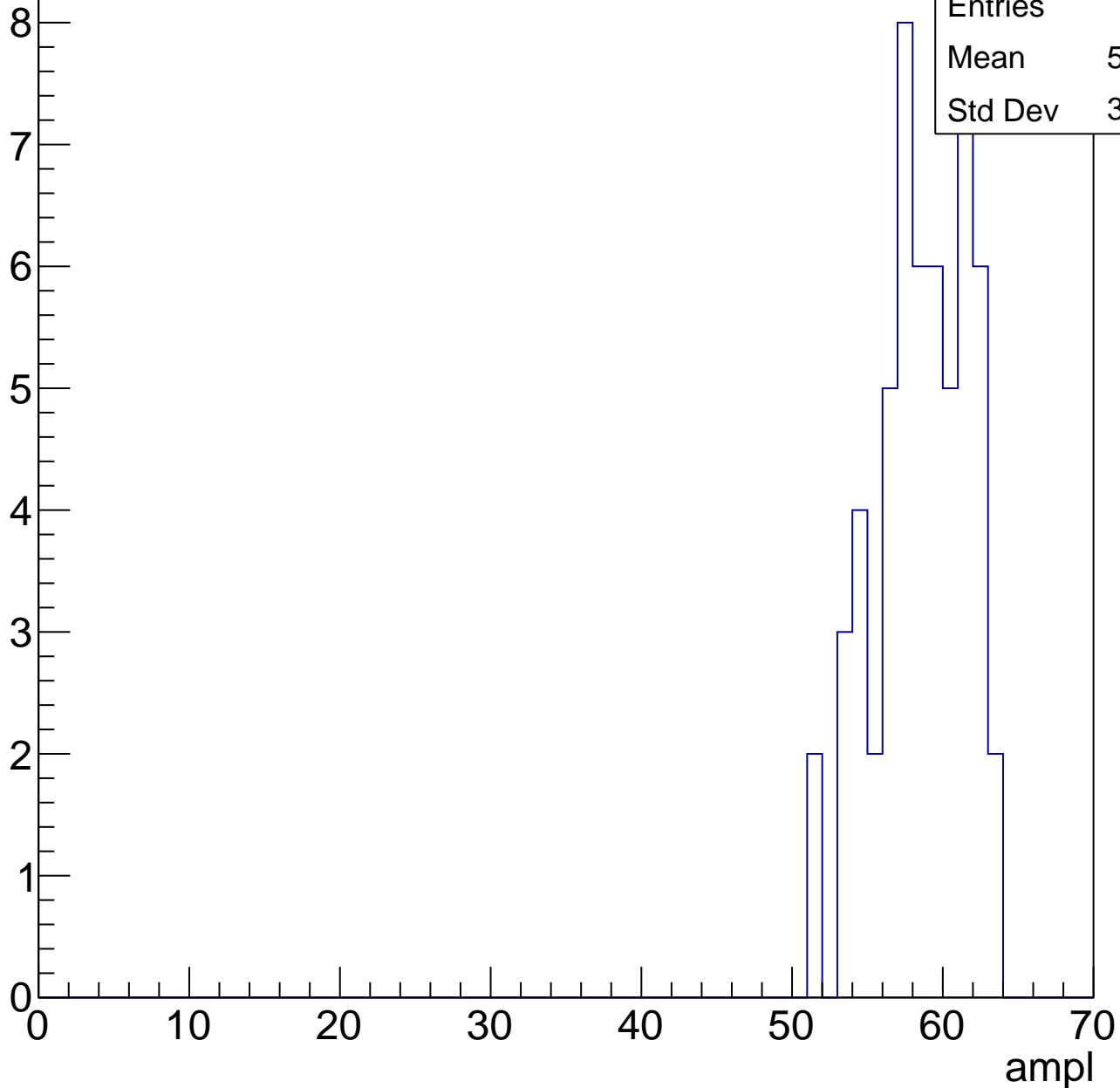
Entries	58
Mean	52.95
Std Dev	4.248



# B1L103S, U21-ch108, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



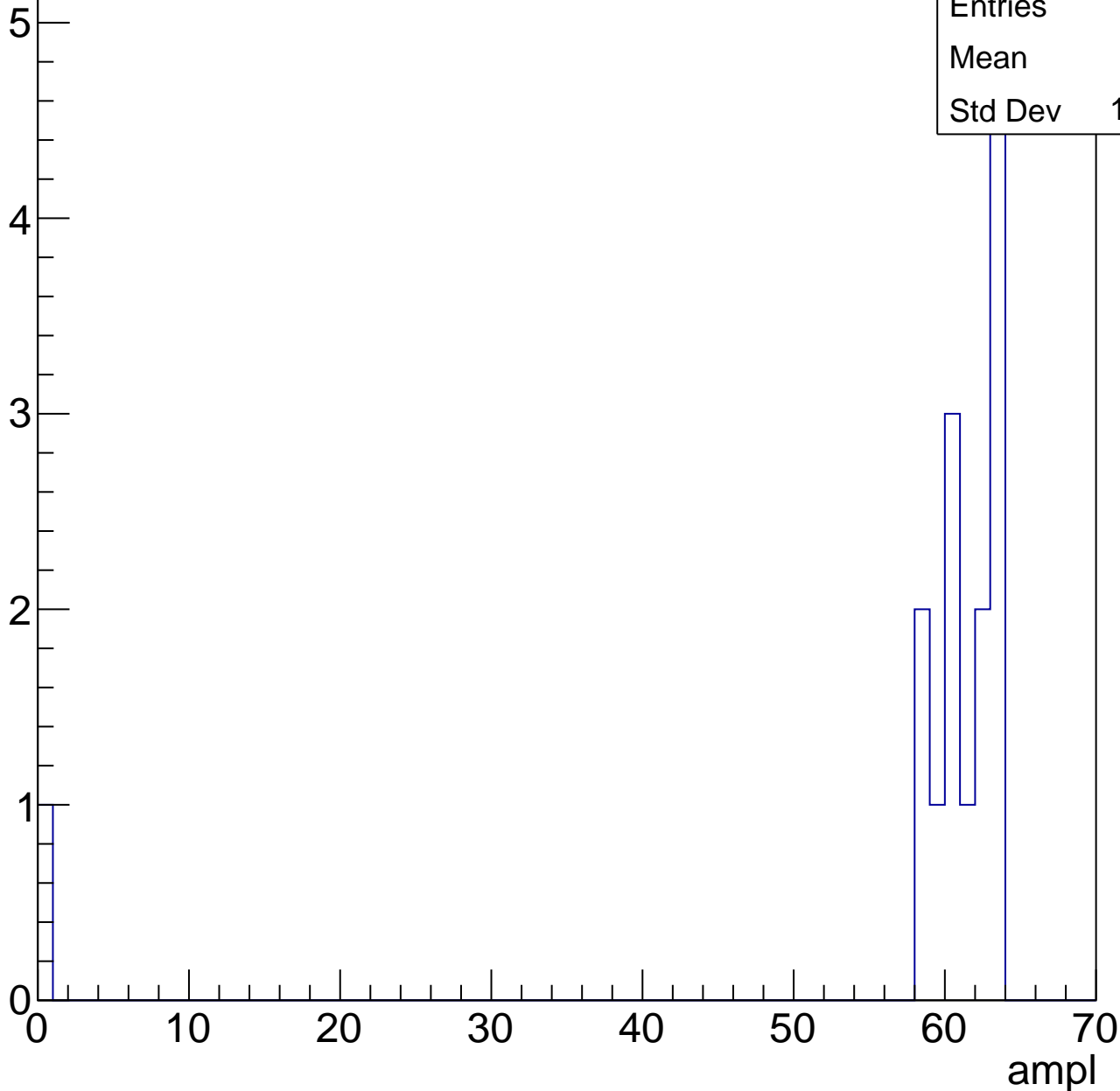
Entries	57
Mean	58.09
Std Dev	3.039

# B1L103S, U21-ch108, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	15
Mean	57
Std Dev	15.34

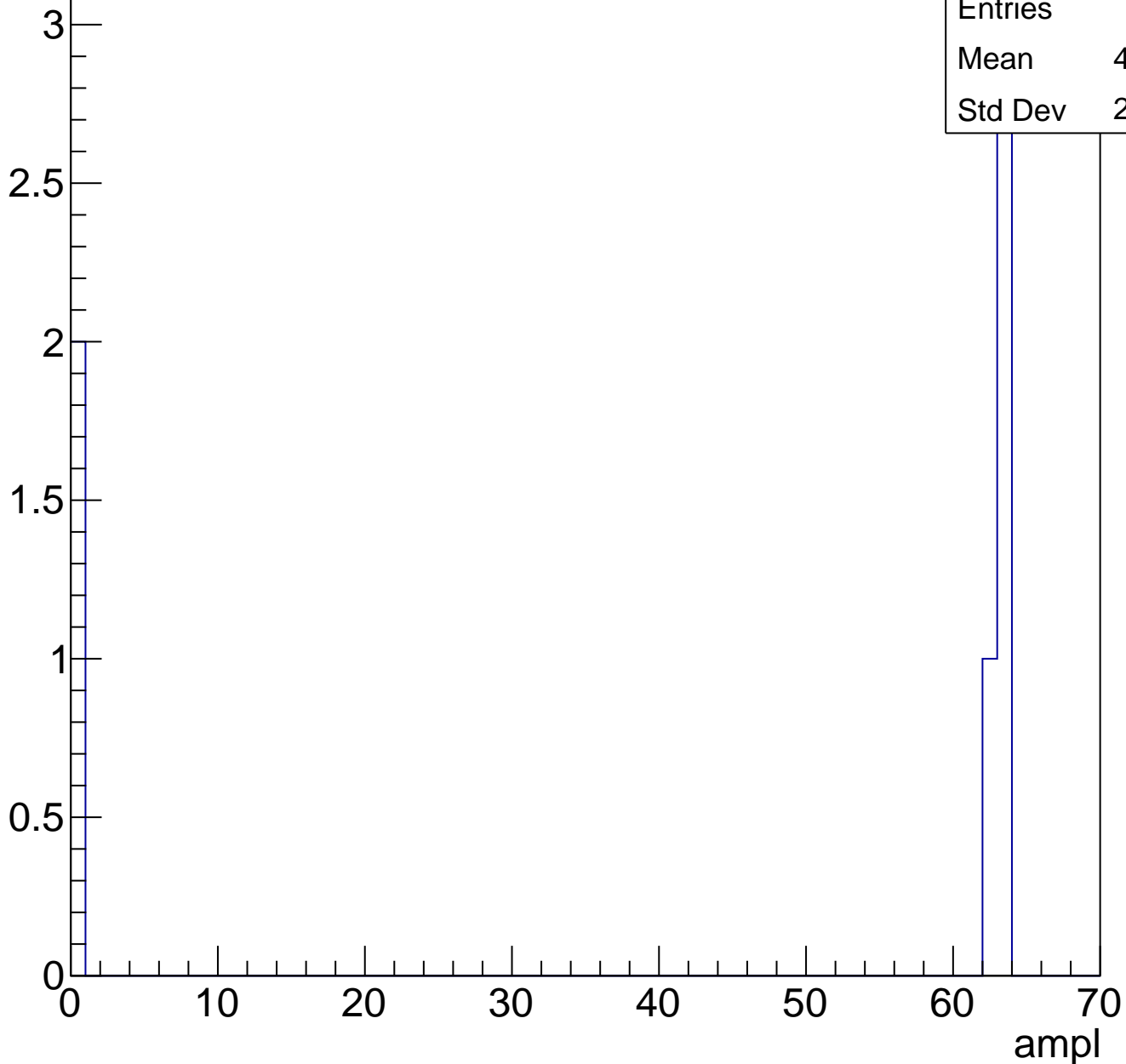




# B1L103S, U21-ch108, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U21-ch109, adc0

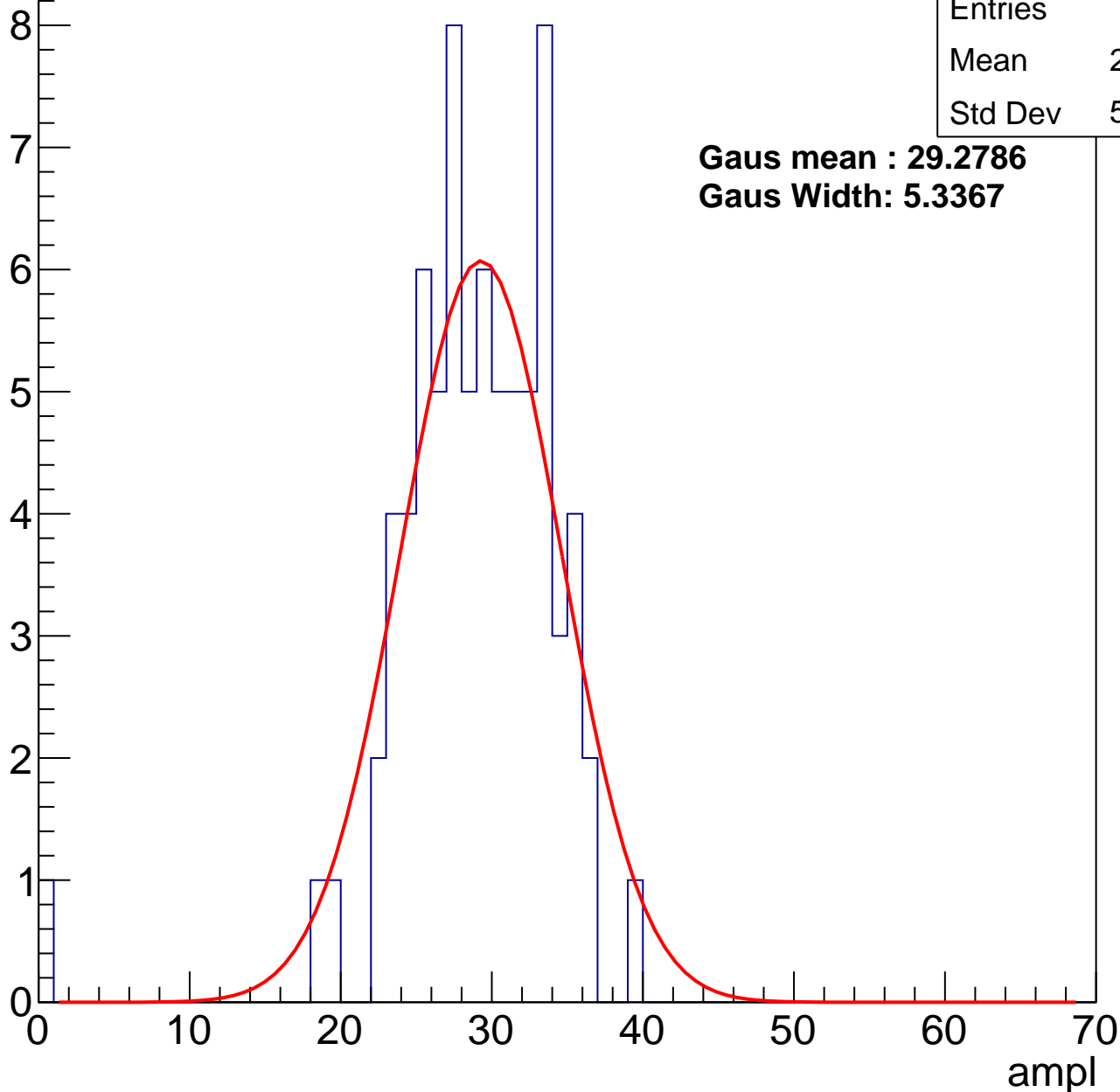
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	28.43
Std Dev	5.347

**Gaus mean : 29.2786**

**Gaus Width: 5.3367**



# B1L103S, U21-ch109, adc1

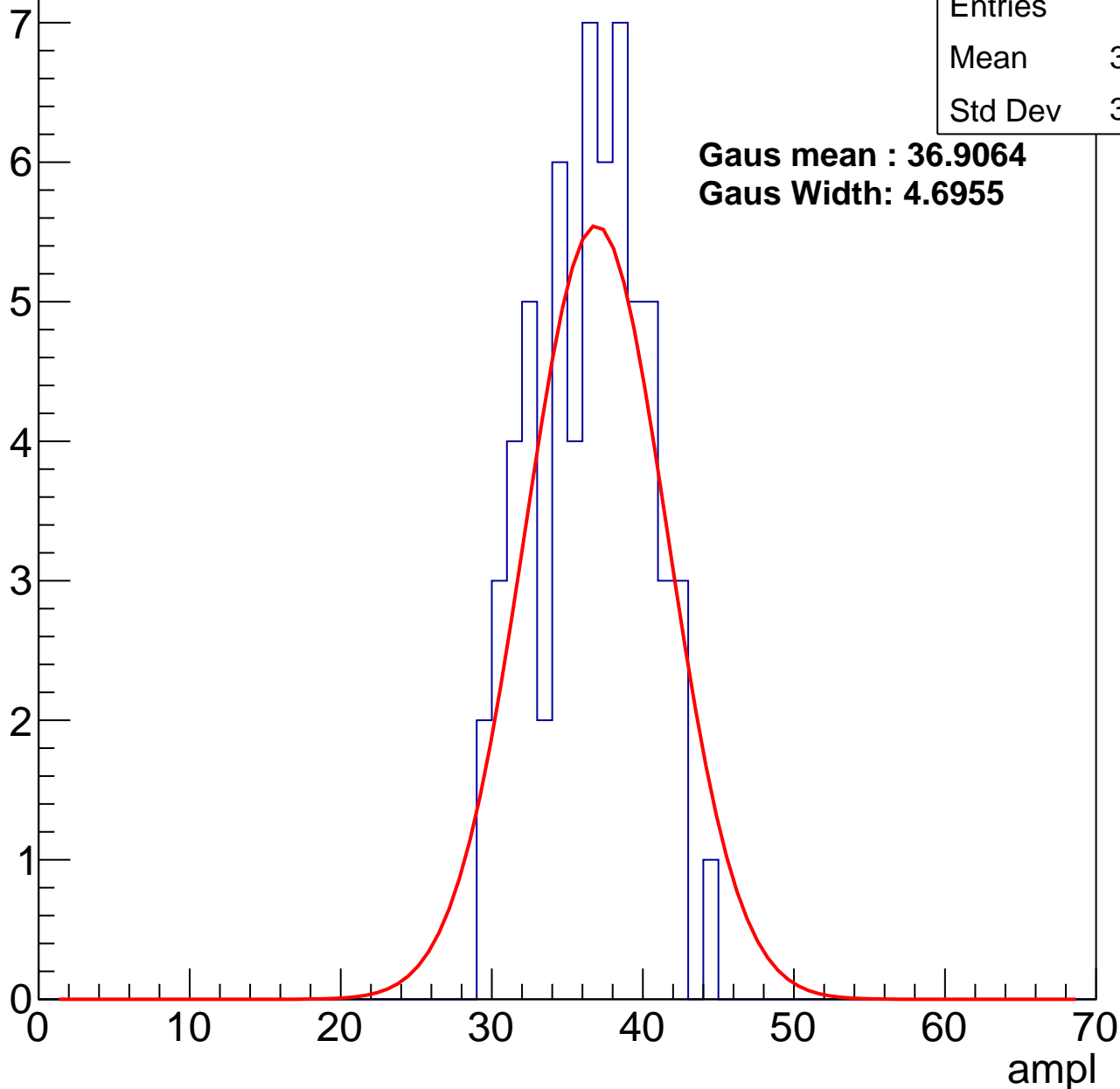
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	36.03
Std Dev	3.647

**Gaus mean : 36.9064**

**Gaus Width: 4.6955**



# B1L103S, U21-ch109, adc2

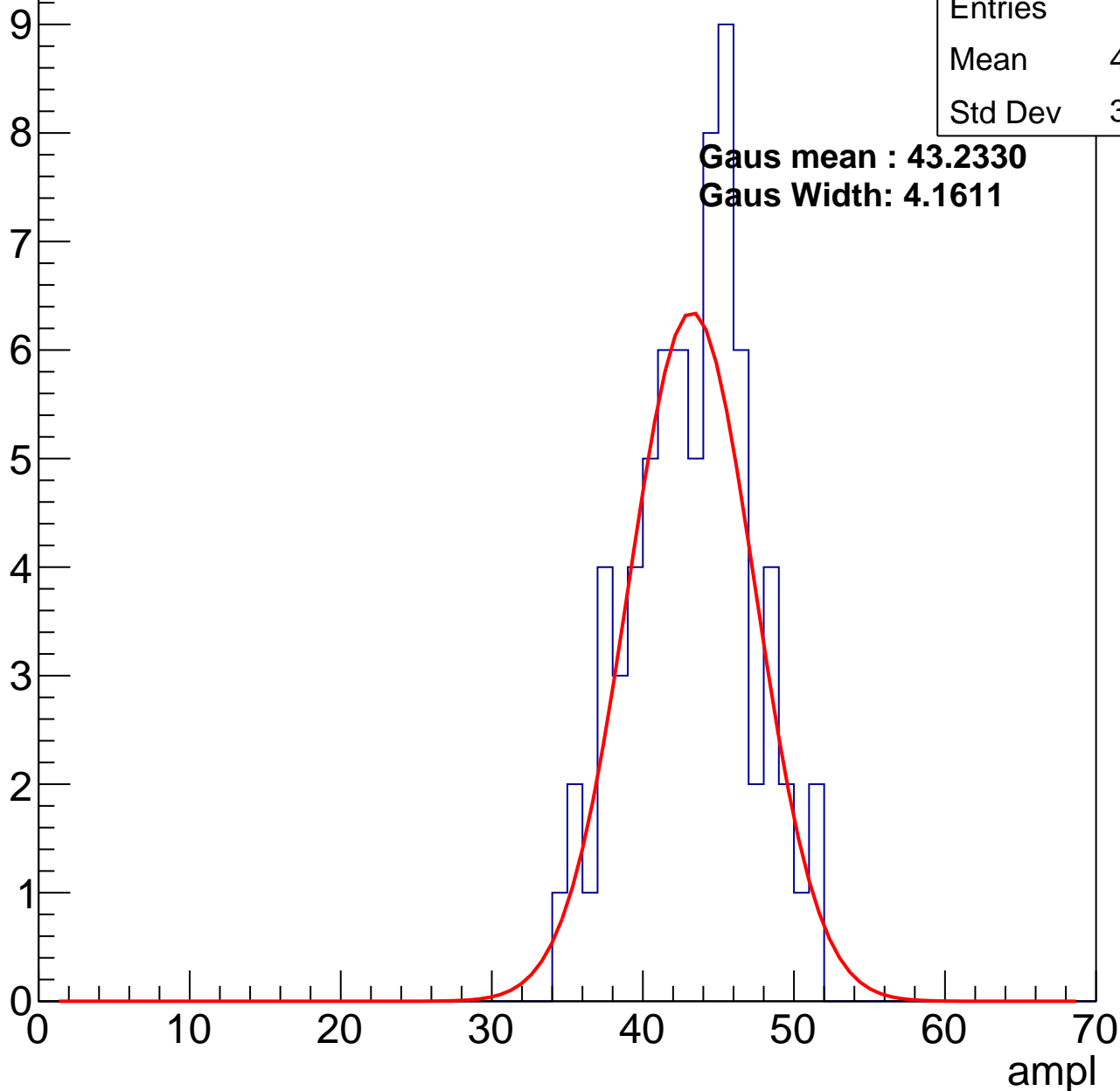
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	42.82
Std Dev	3.923

**Gaus mean : 43.2330**

**Gaus Width: 4.1611**

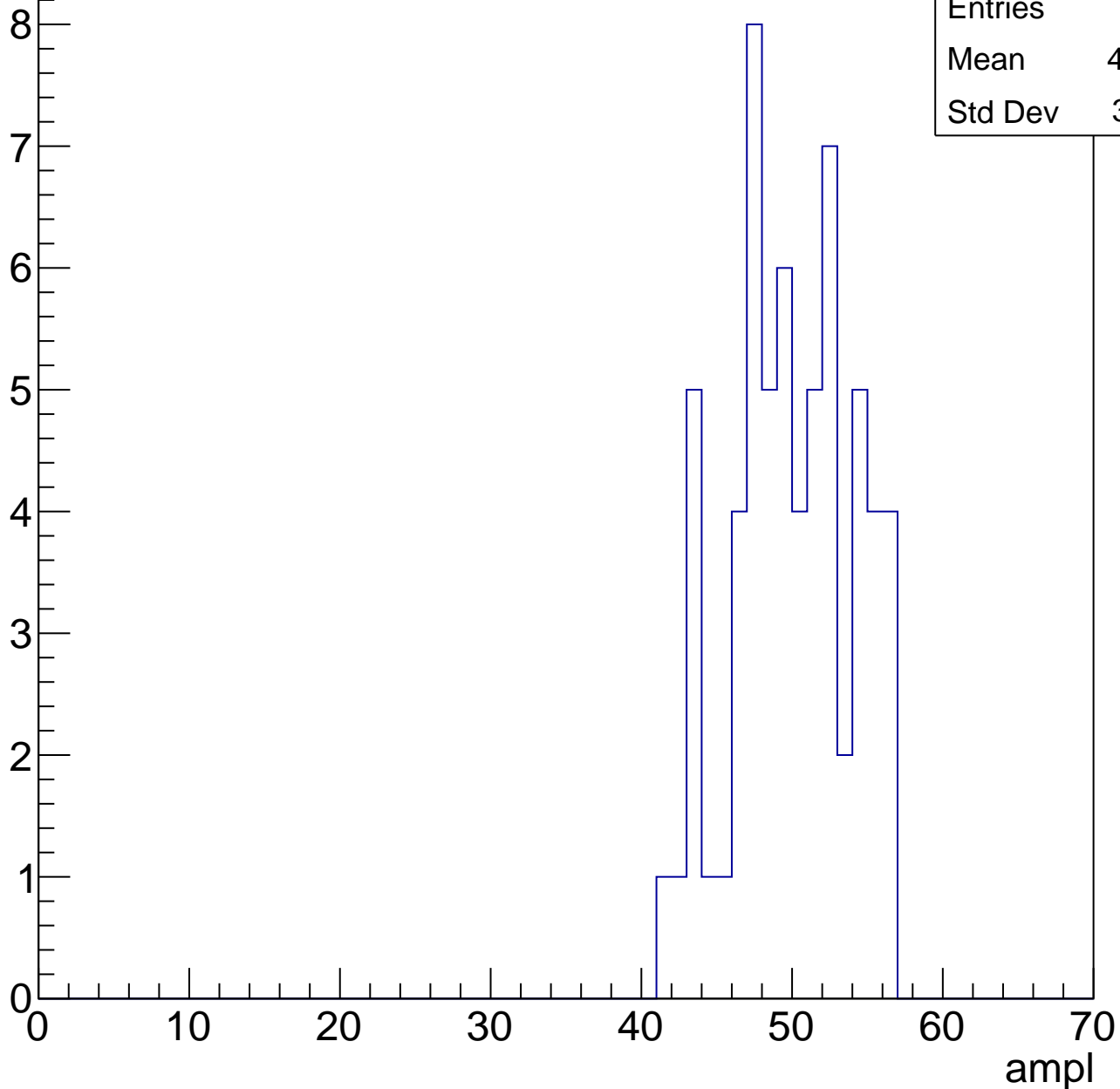


# B1L103S, U21-ch109, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	49.52
Std Dev	3.931

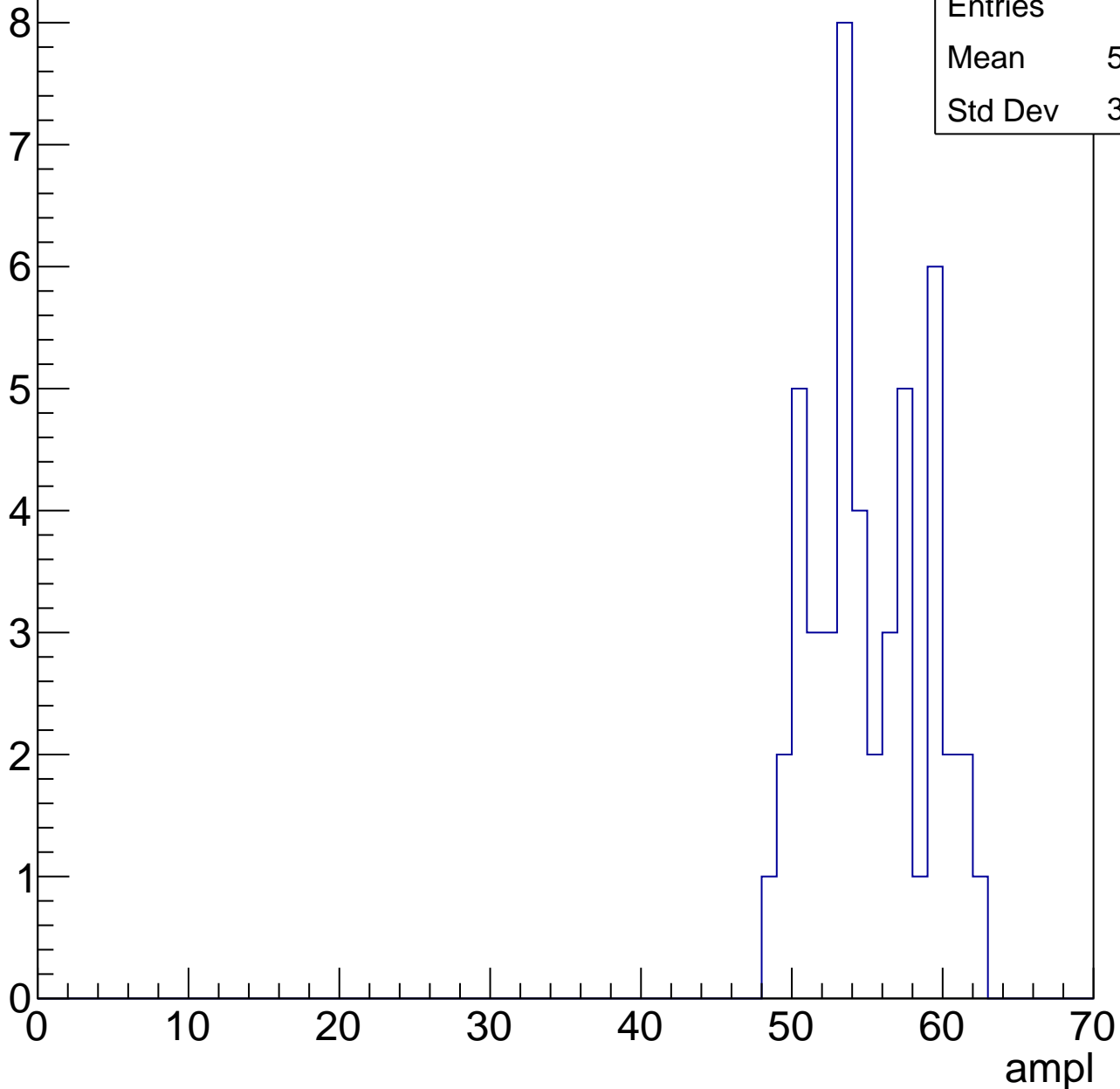


# B1L103S, U21-ch109, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	48
Mean	54.67
Std Dev	3.682

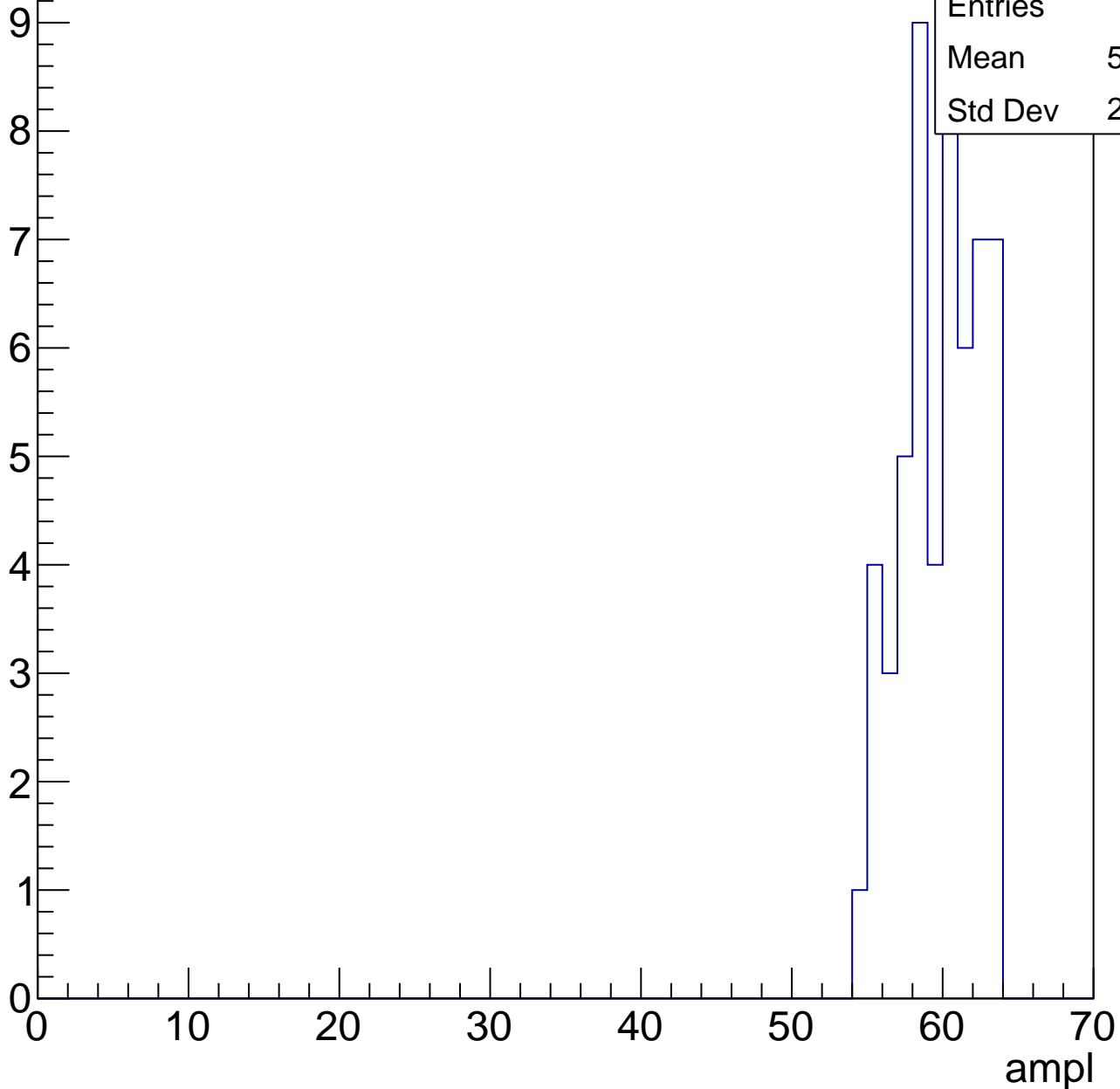


# B1L103S, U21-ch109, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

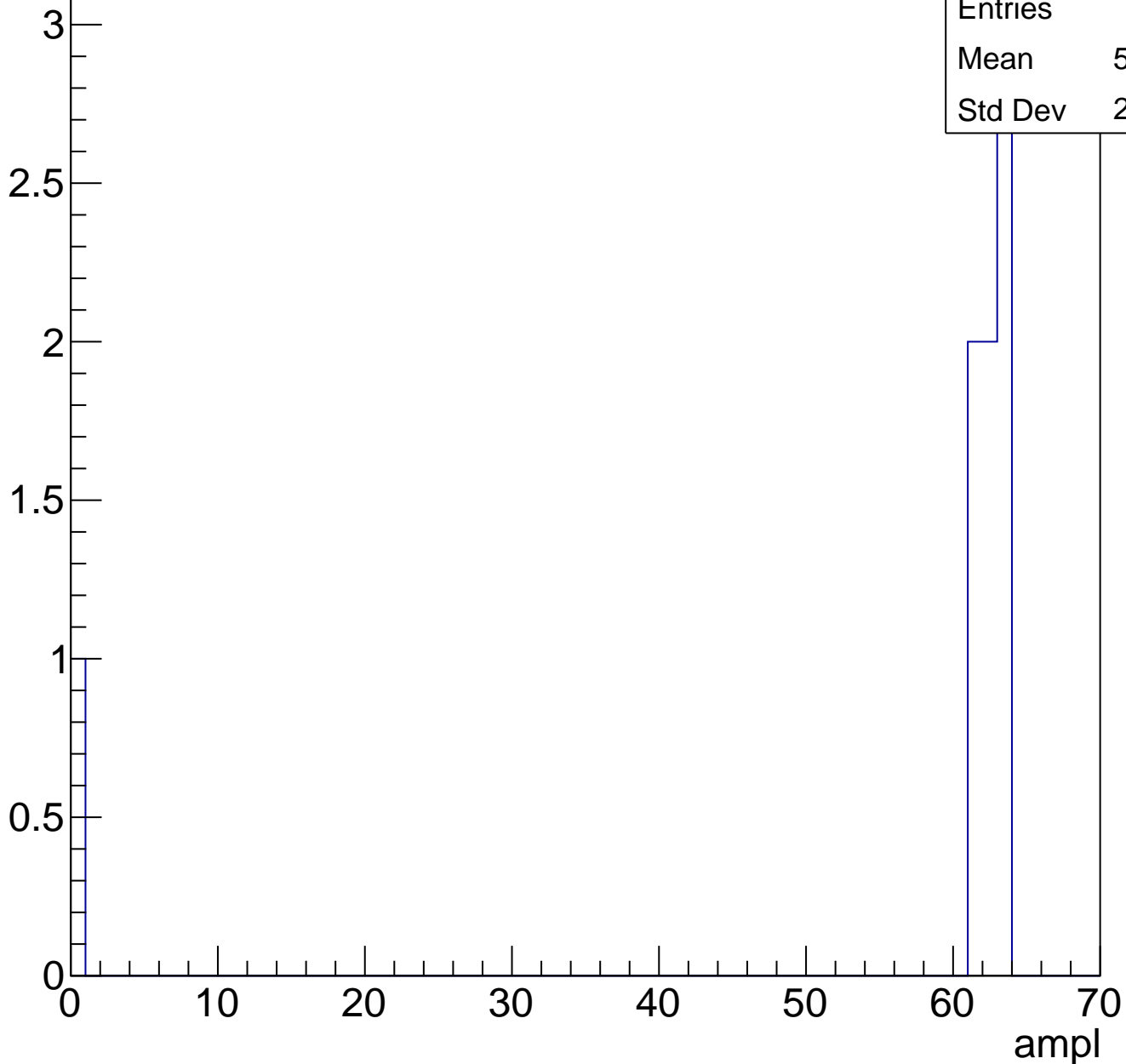
Entries	54
Mean	59.37
Std Dev	2.526



# B1L103S, U21-ch109, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U21-ch109, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U21-ch110, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	80
Mean	26.66
Std Dev	6.473

**Gaus mean : 27.7649**

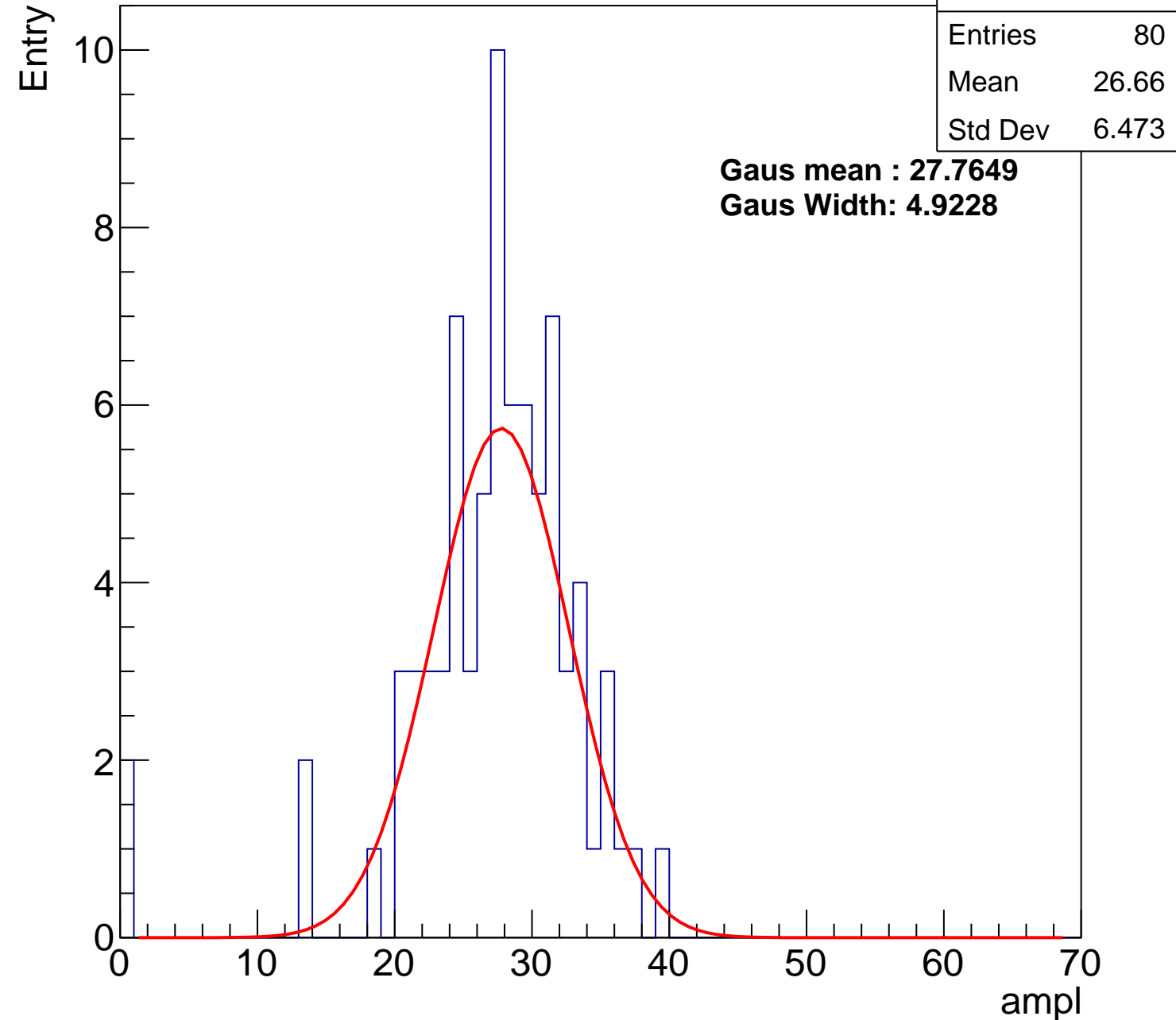
**Gaus Width: 4.9228**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U21-ch110, adc1

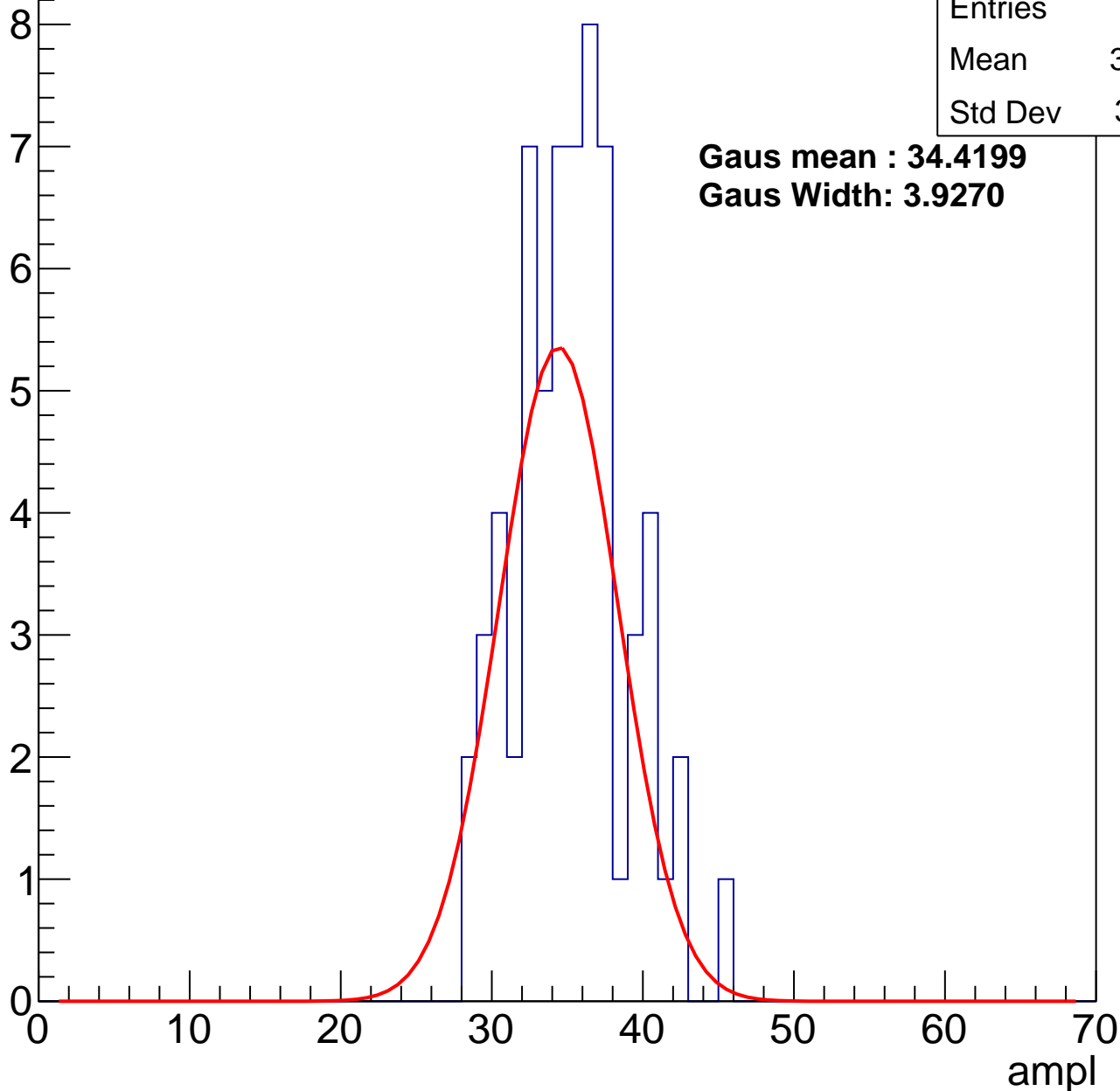
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	34.83
Std Dev	3.651

**Gaus mean : 34.4199**

**Gaus Width: 3.9270**



# B1L103S, U21-ch110, adc2

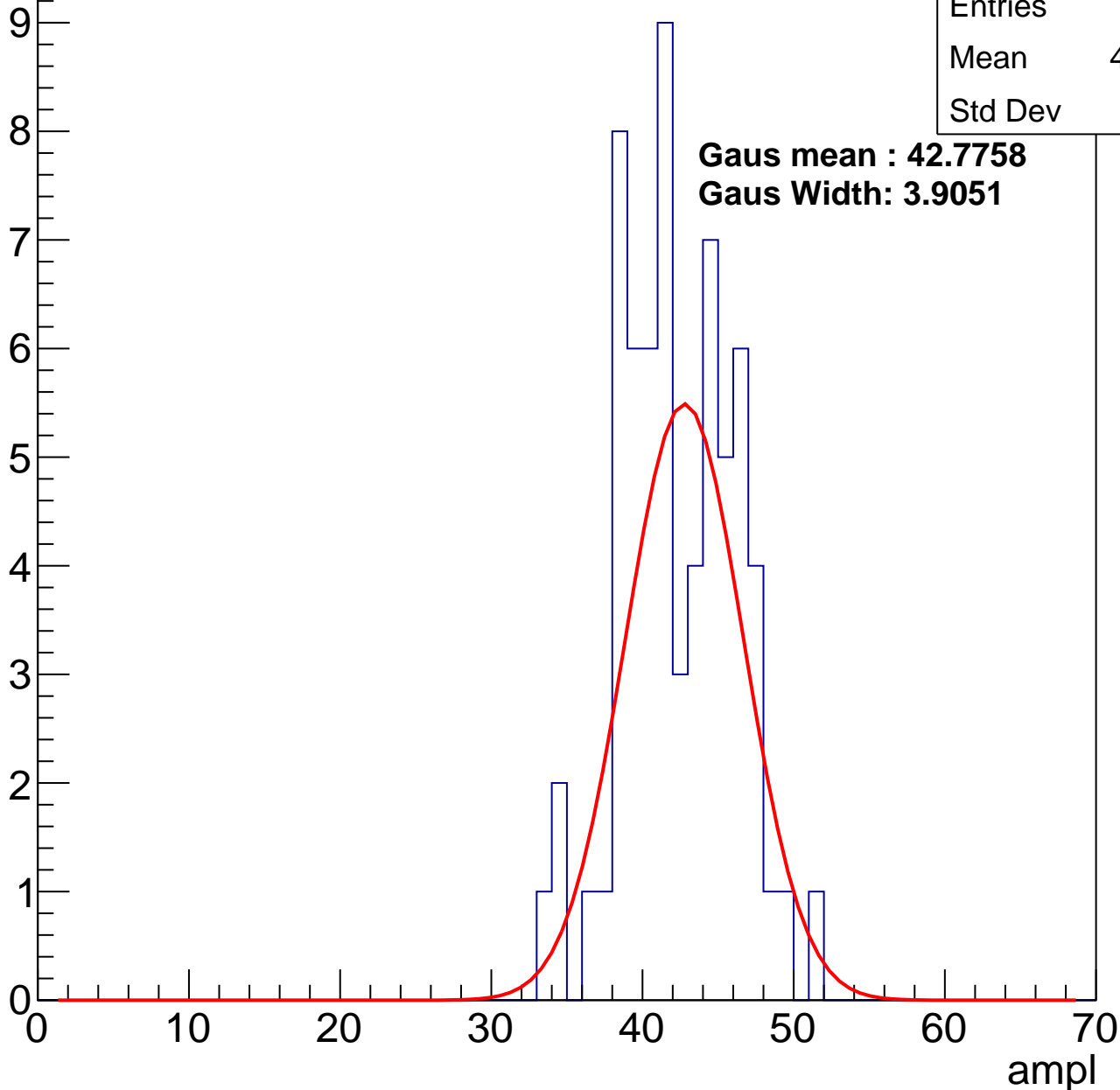
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	41.88
Std Dev	3.74

**Gaus mean : 42.7758**

**Gaus Width: 3.9051**

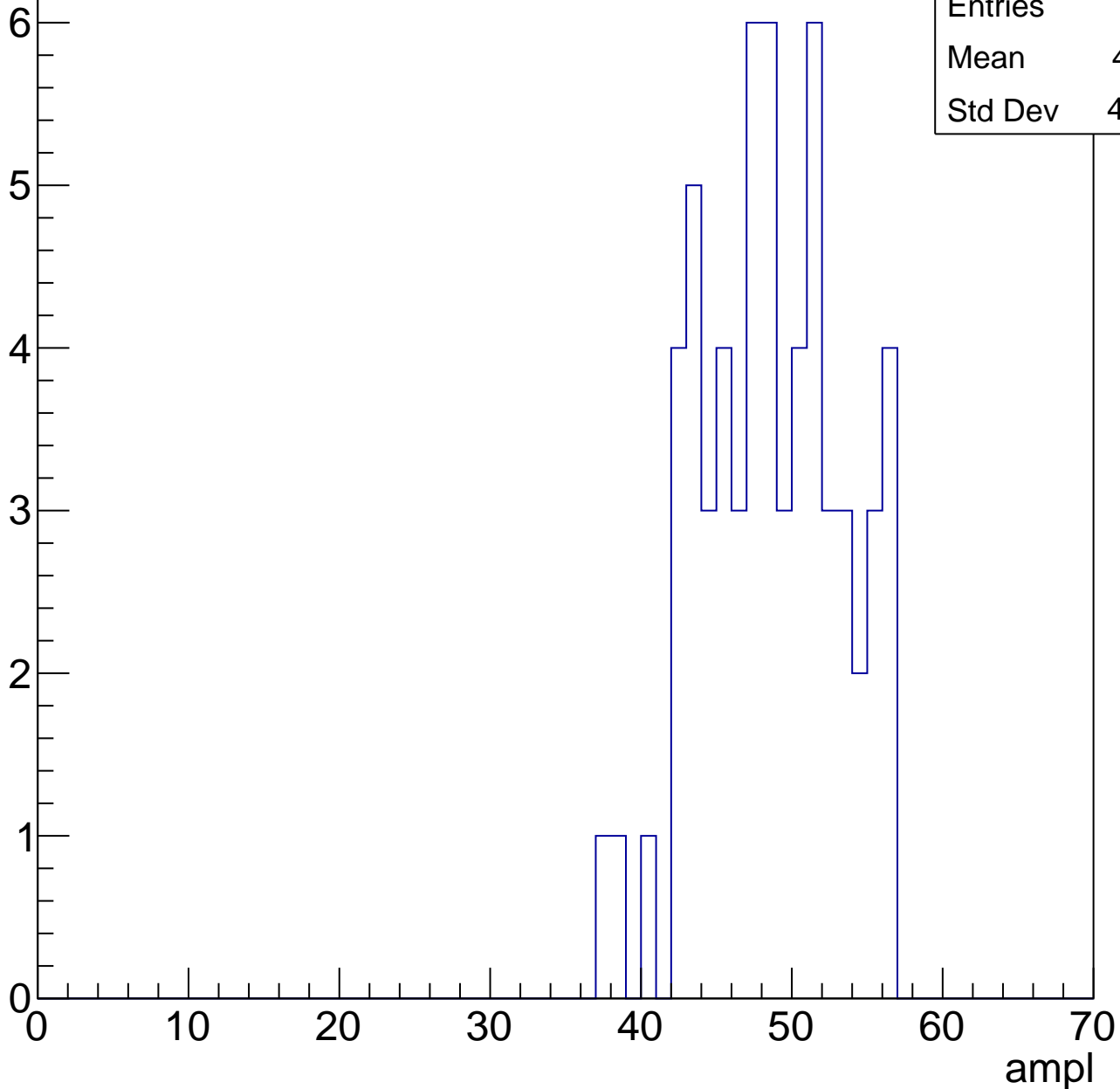


# B1L103S, U21-ch110, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	48.11
Std Dev	4.625

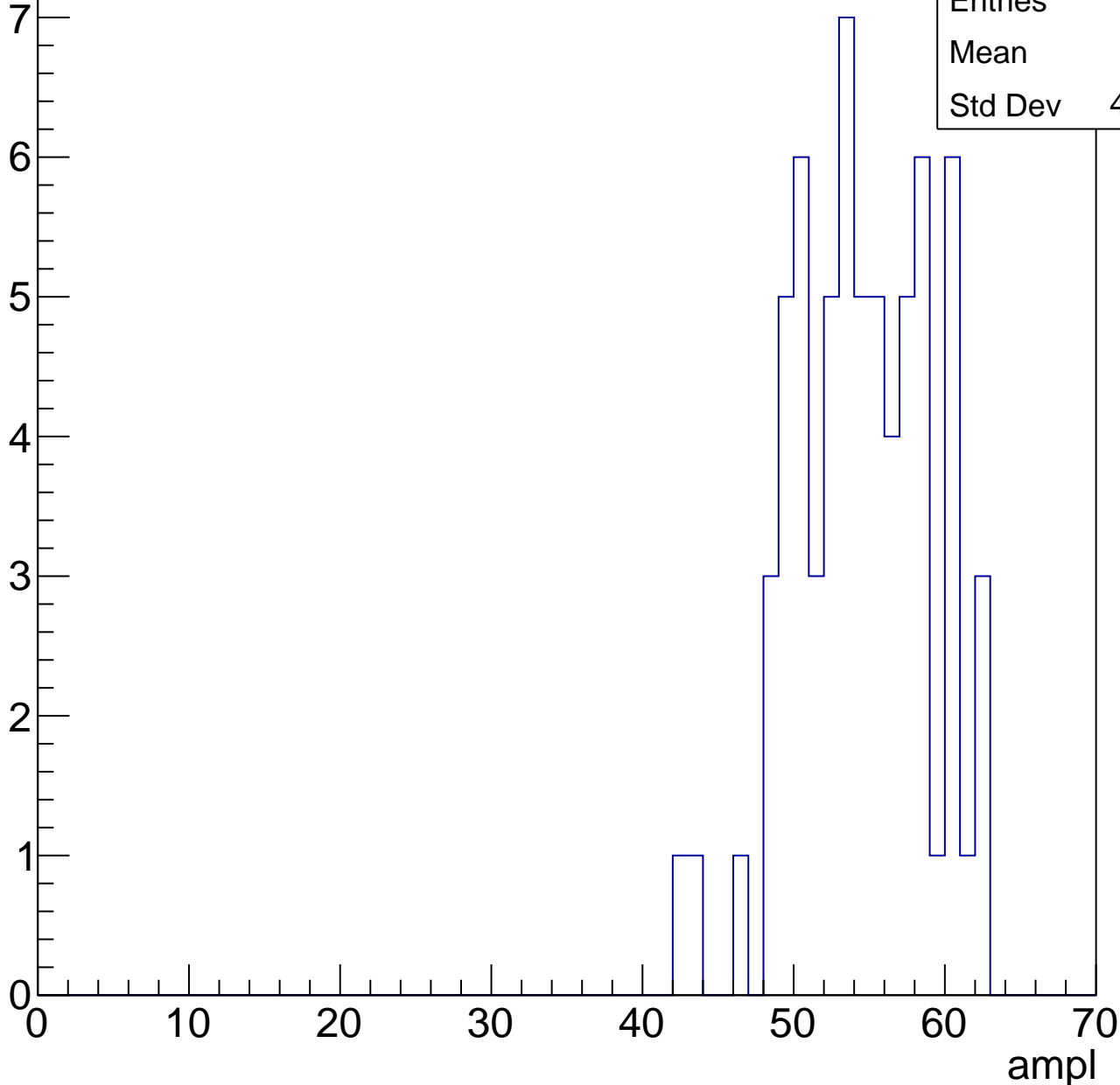


# B1L103S, U21-ch110, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	54
Std Dev	4.466

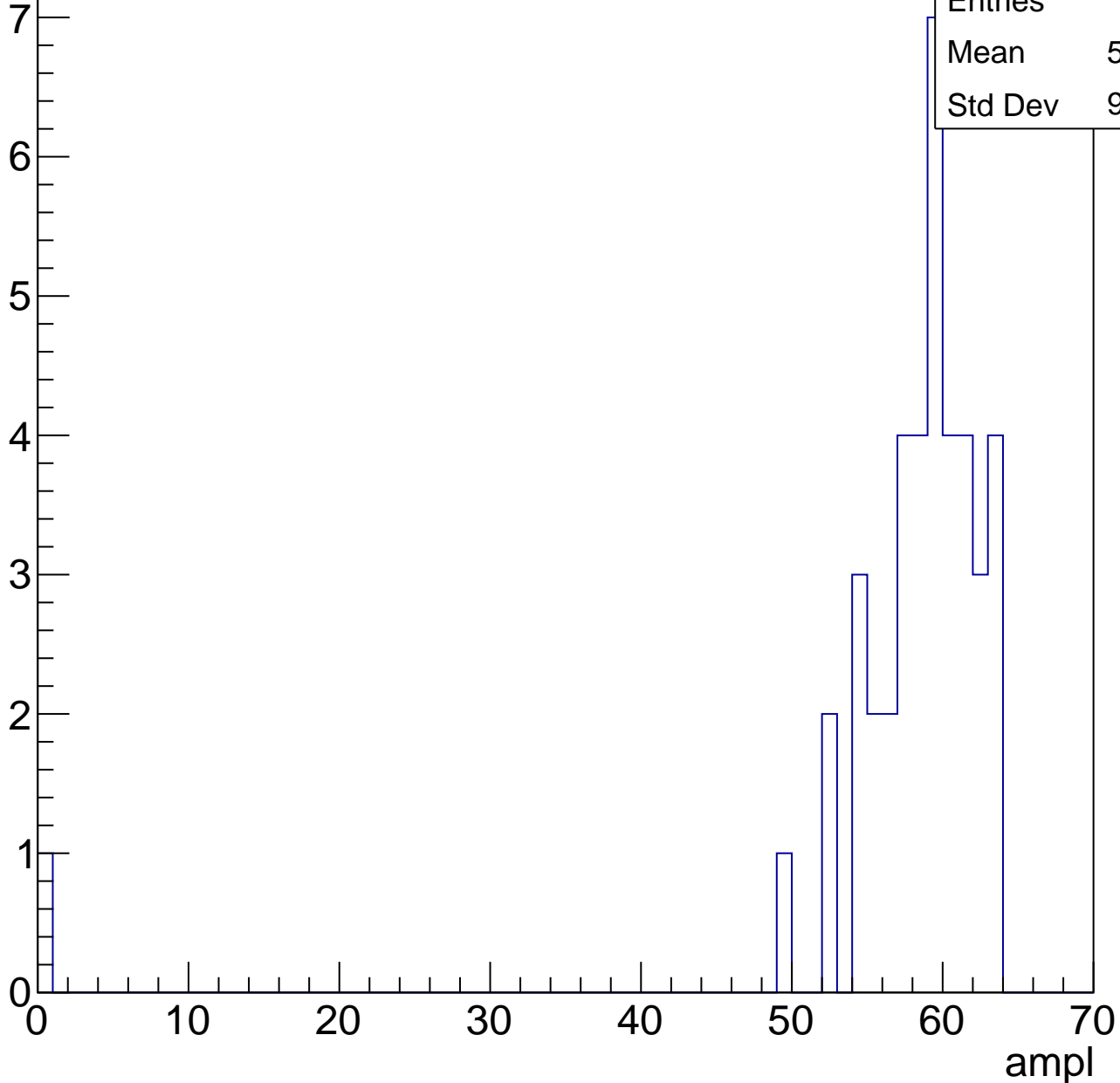


# B1L103S, U21-ch110, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

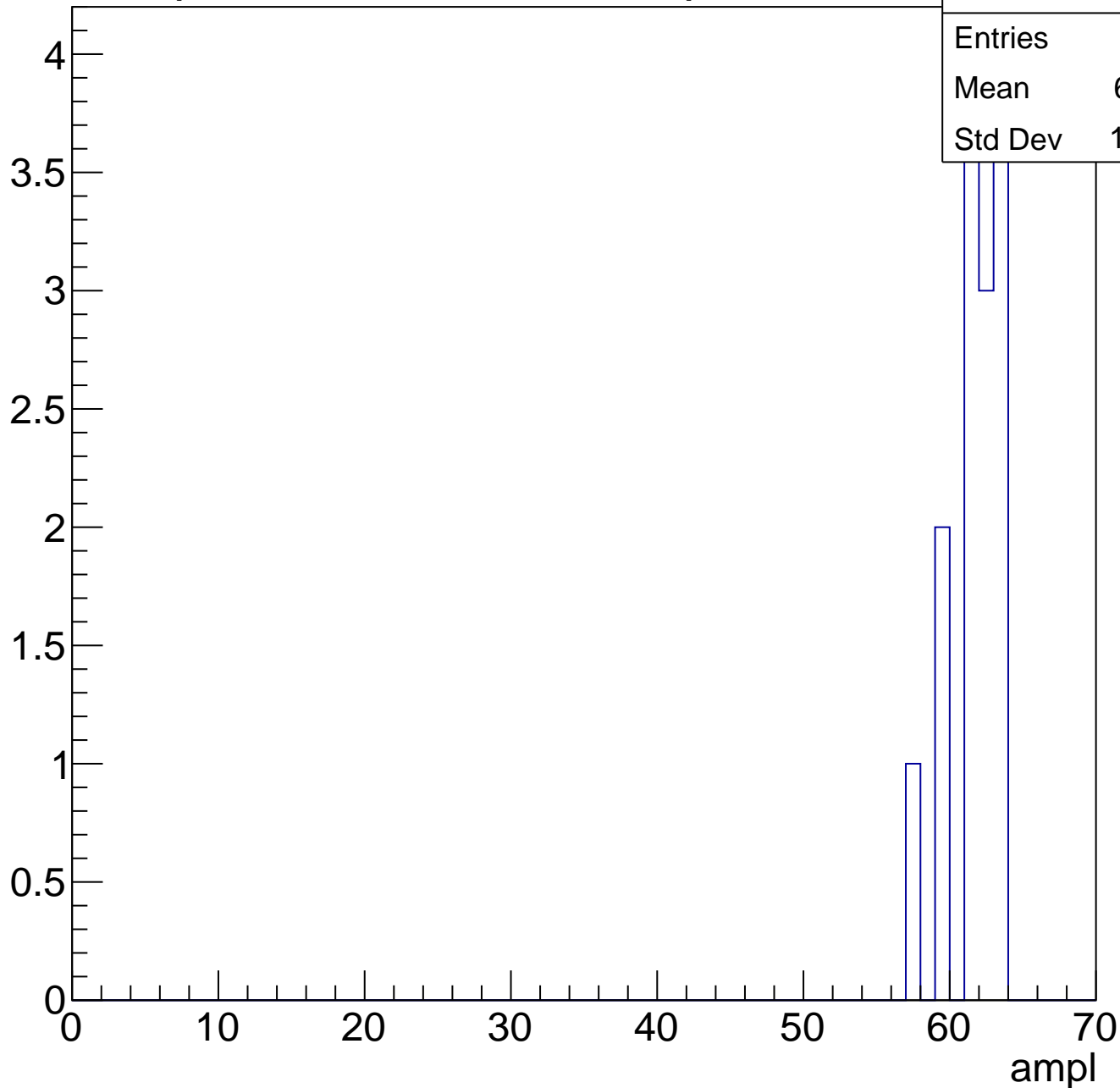
Entries	41
Mean	56.88
Std Dev	9.564



# B1L103S, U21-ch110, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



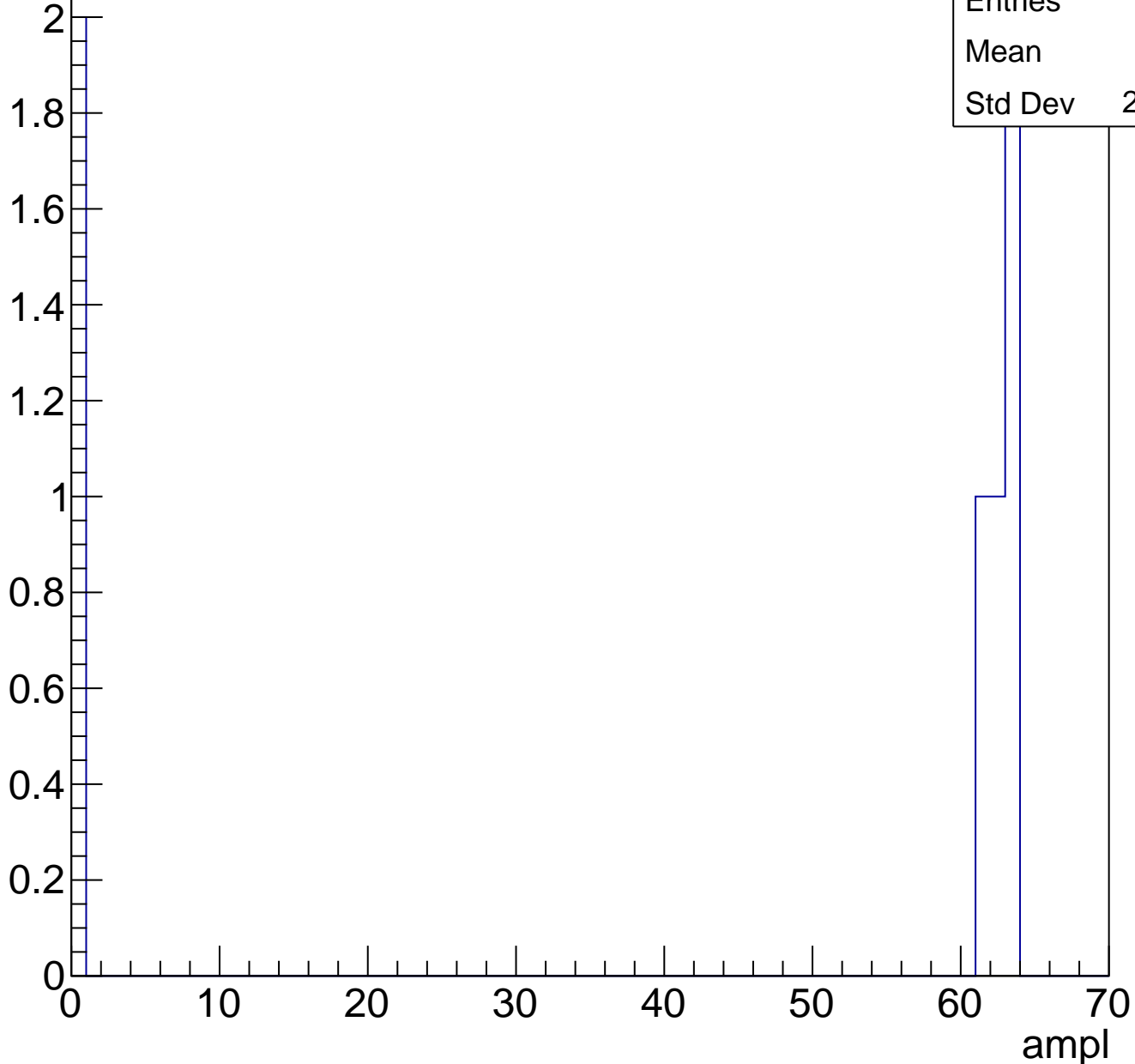
Entries	14
Mean	61.21
Std Dev	1.739



# B1L103S, U21-ch110, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	6
Mean	41.5
Std Dev	29.35

# B1L103S, U21-ch111, adc0

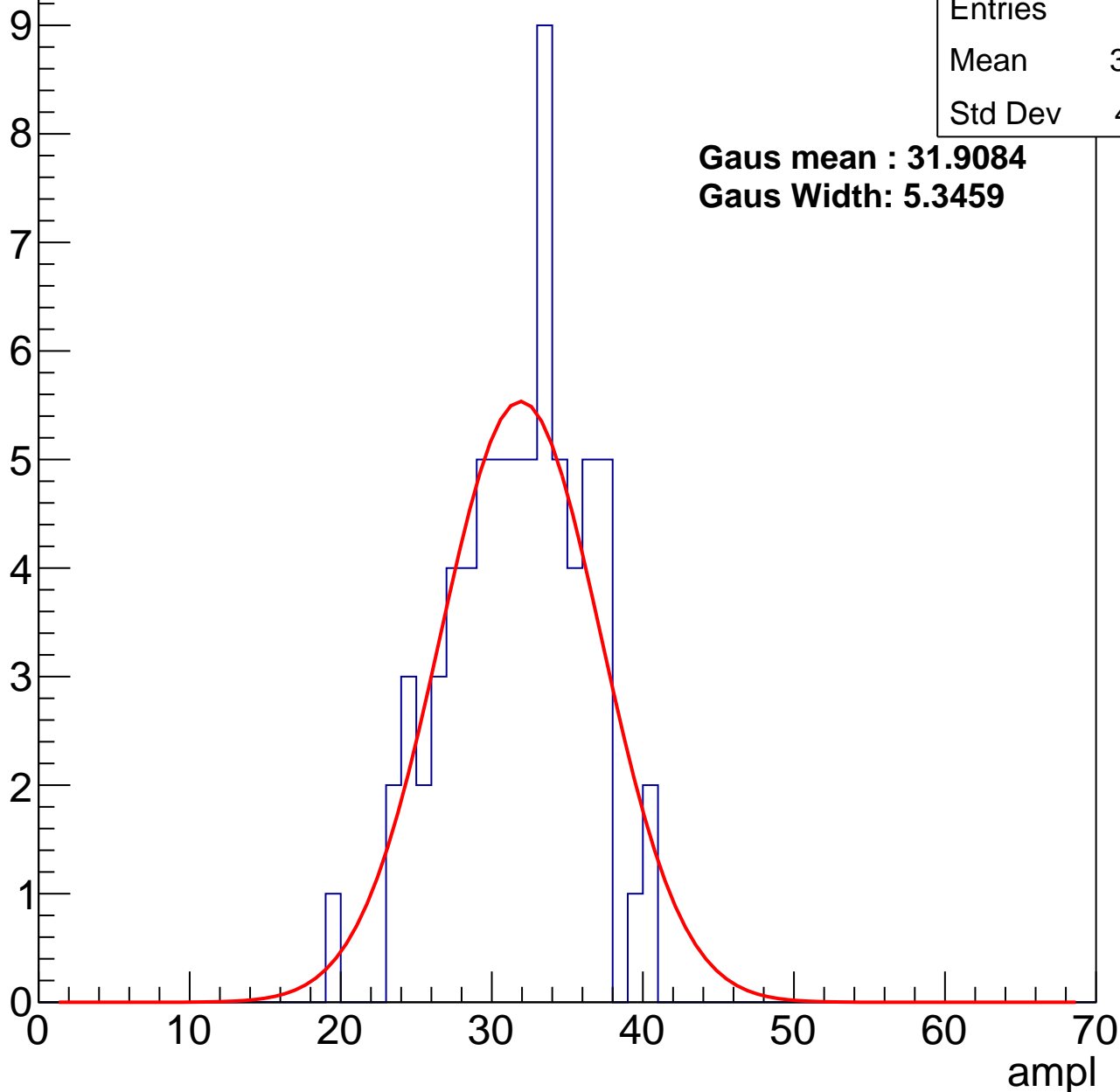
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	31.23
Std Dev	4.421

**Gaus mean : 31.9084**

**Gaus Width: 5.3459**



# B1L103S, U21-ch111, adc1

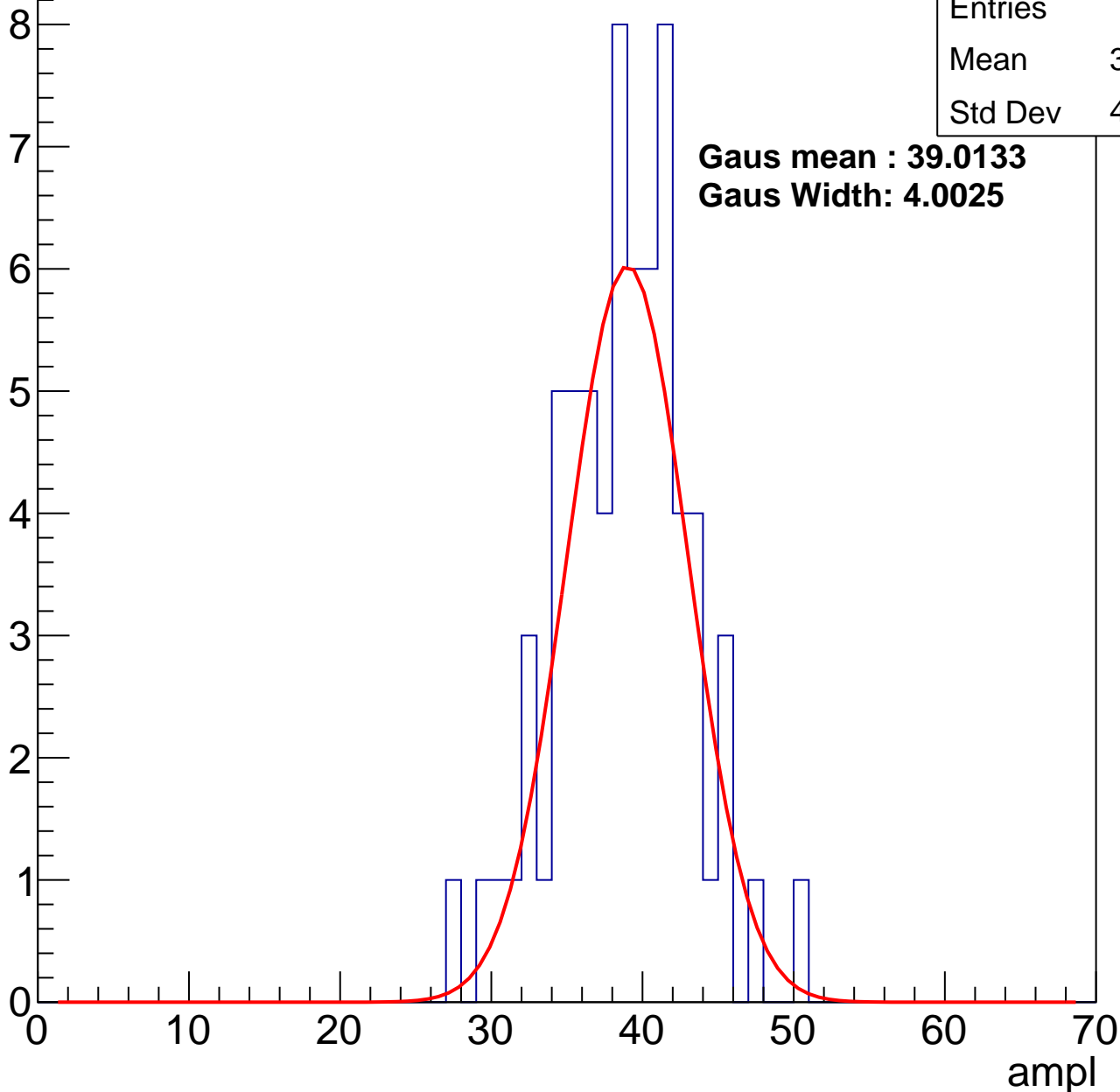
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	38.28
Std Dev	4.283

**Gaus mean : 39.0133**

**Gaus Width: 4.0025**



# B1L103S, U21-ch111, adc2

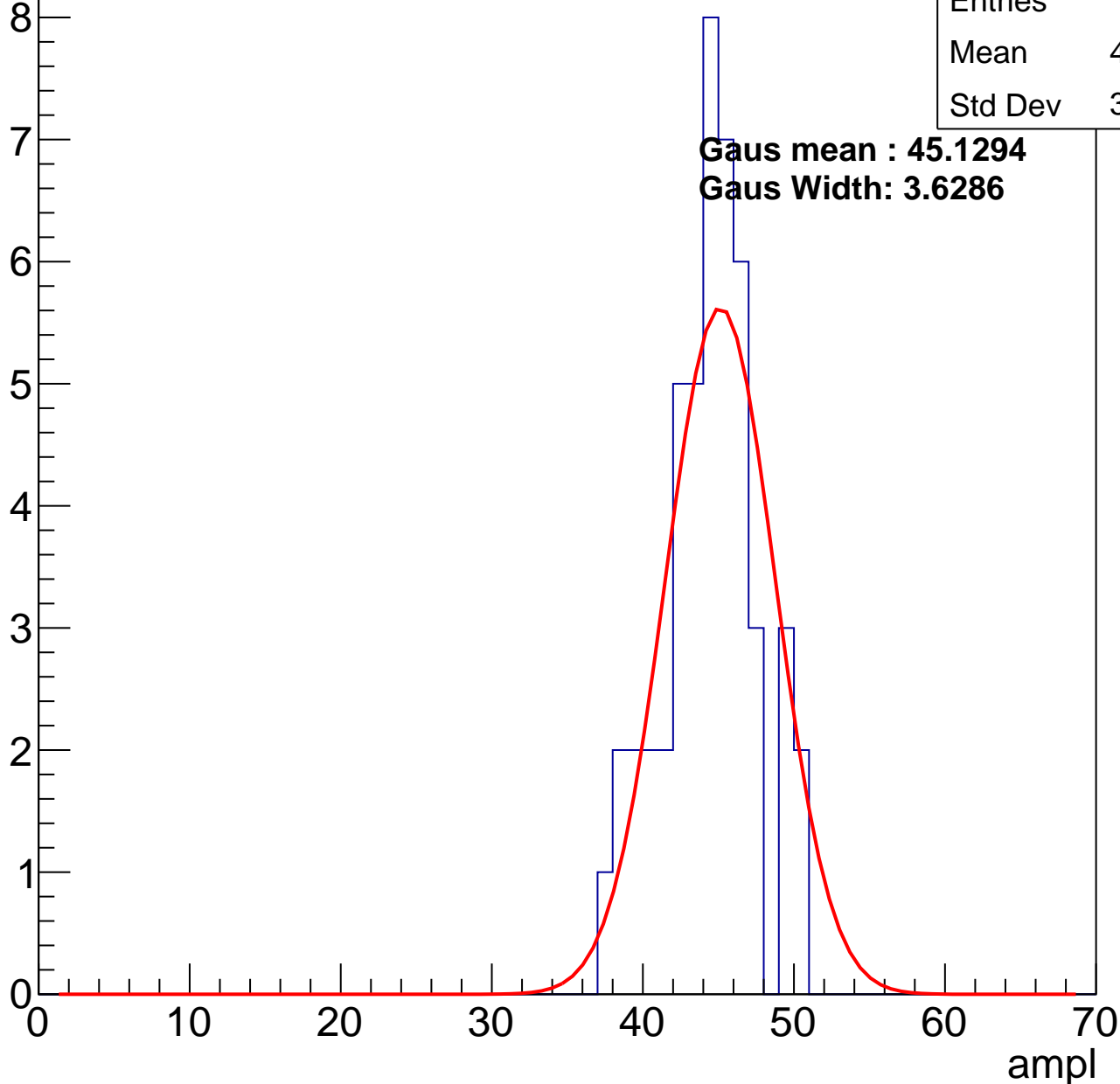
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	48
Mean	43.94
Std Dev	3.065

**Gaus mean : 45.1294**

**Gaus Width: 3.6286**



# B1L103S, U21-ch111, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

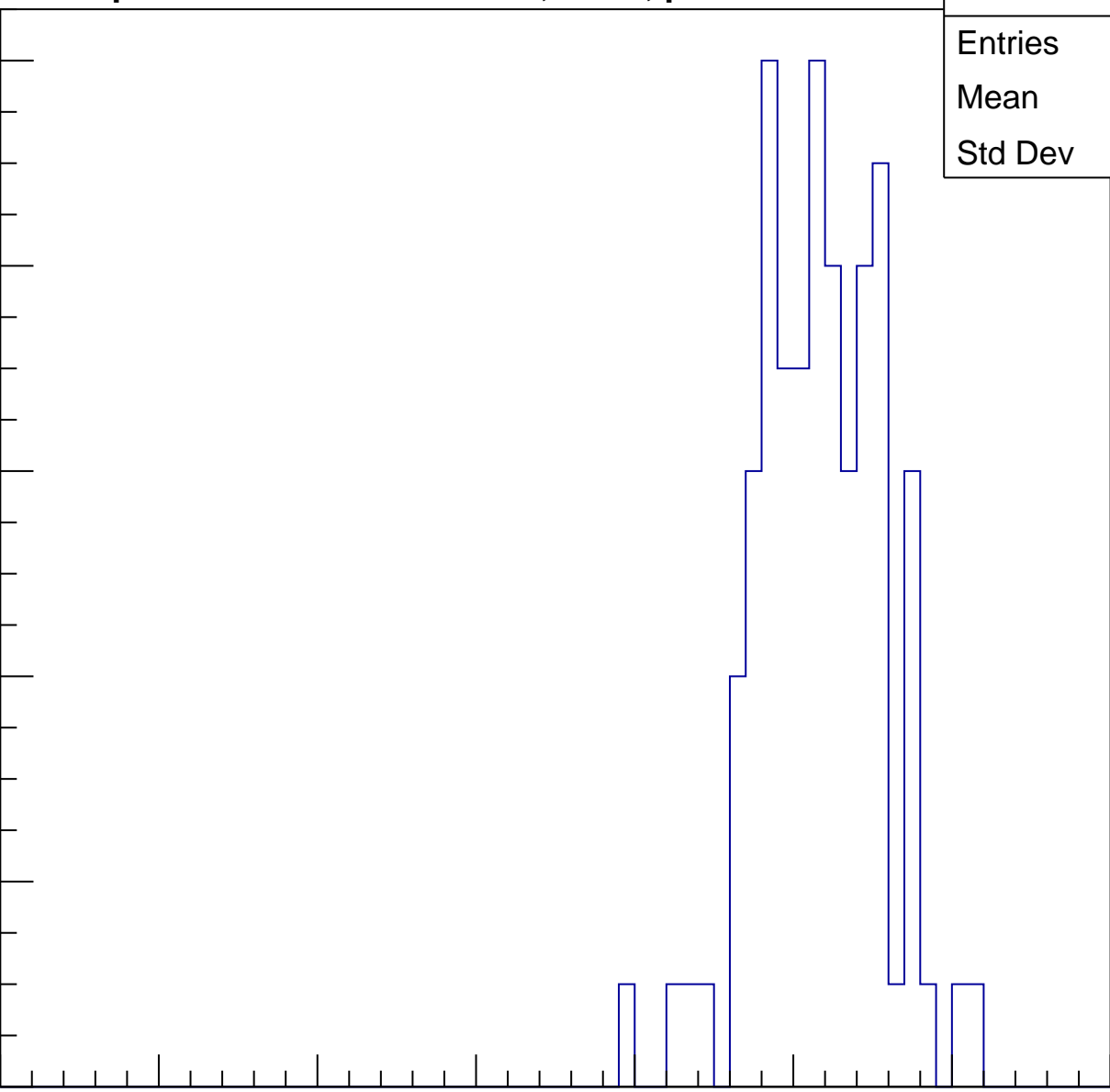
Entries	89
Mean	51.18
Std Dev	3.931

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

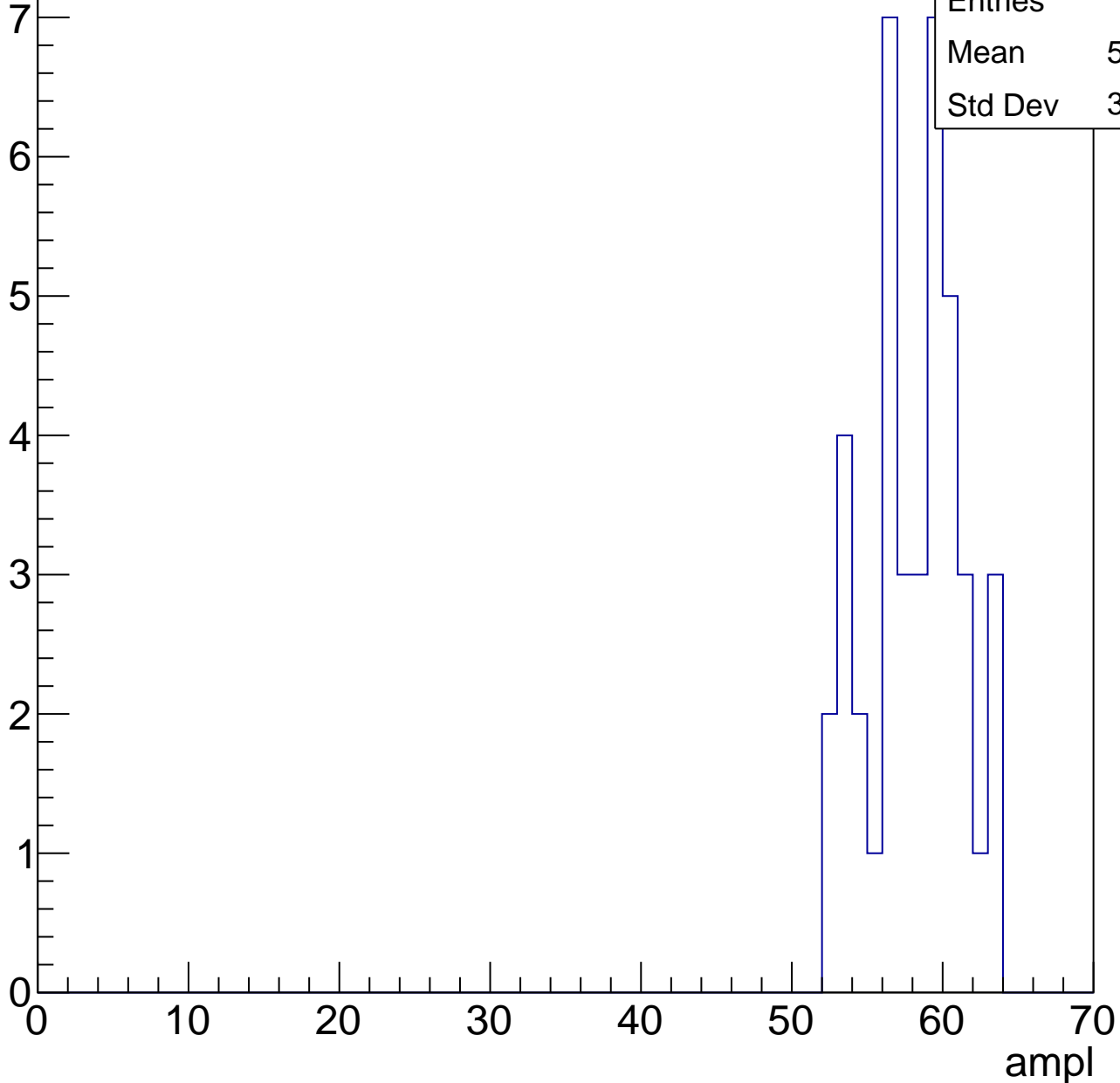


# B1L103S, U21-ch111, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	41
Mean	57.63
Std Dev	3.058

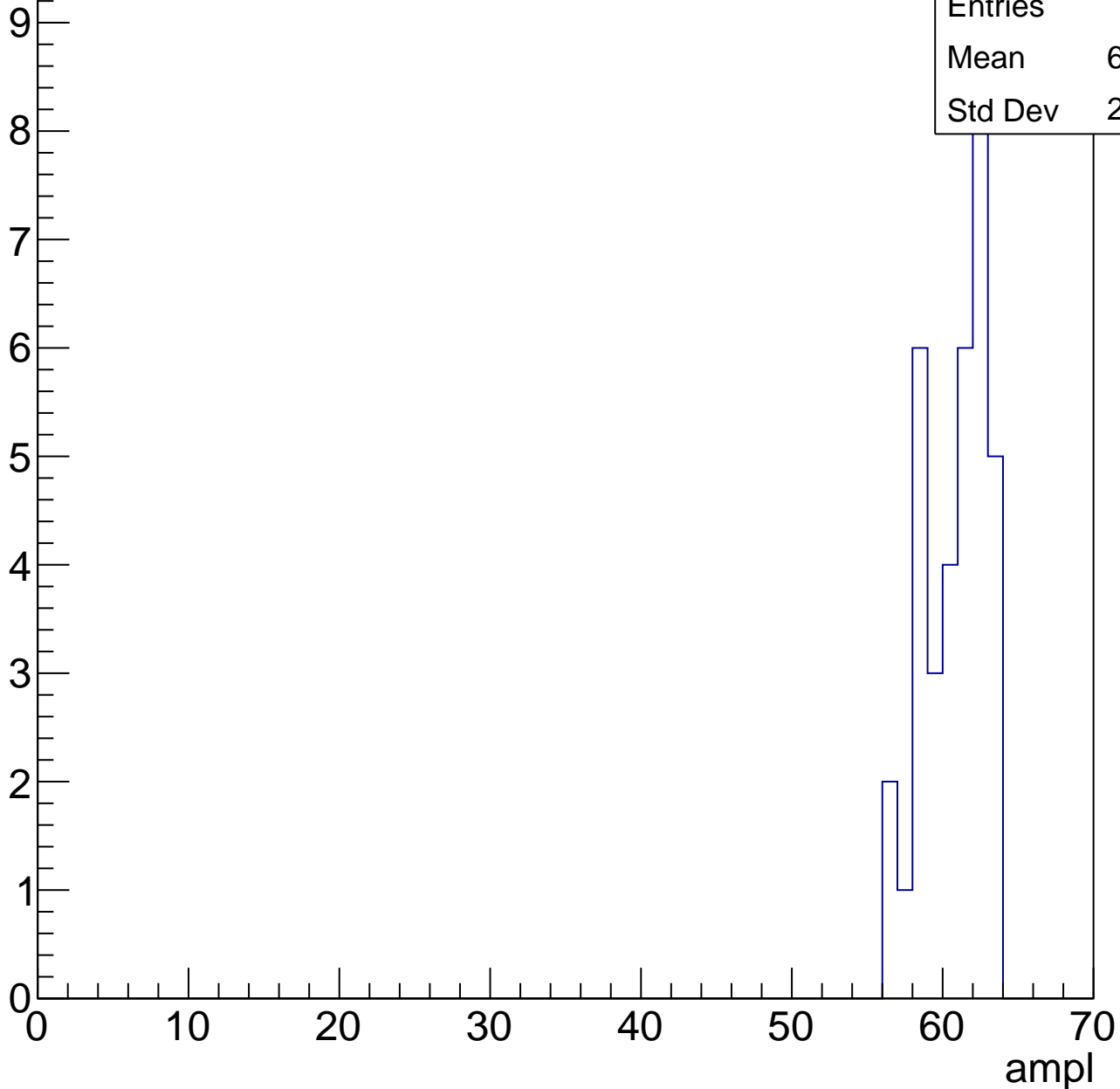


# B1L103S, U21-ch111, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	36
Mean	60.36
Std Dev	2.043



# B1L103S, U21-ch111, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U21-ch111, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

0

Mean

0

Std Dev

0

# B1L103S, U21-ch112, adc0

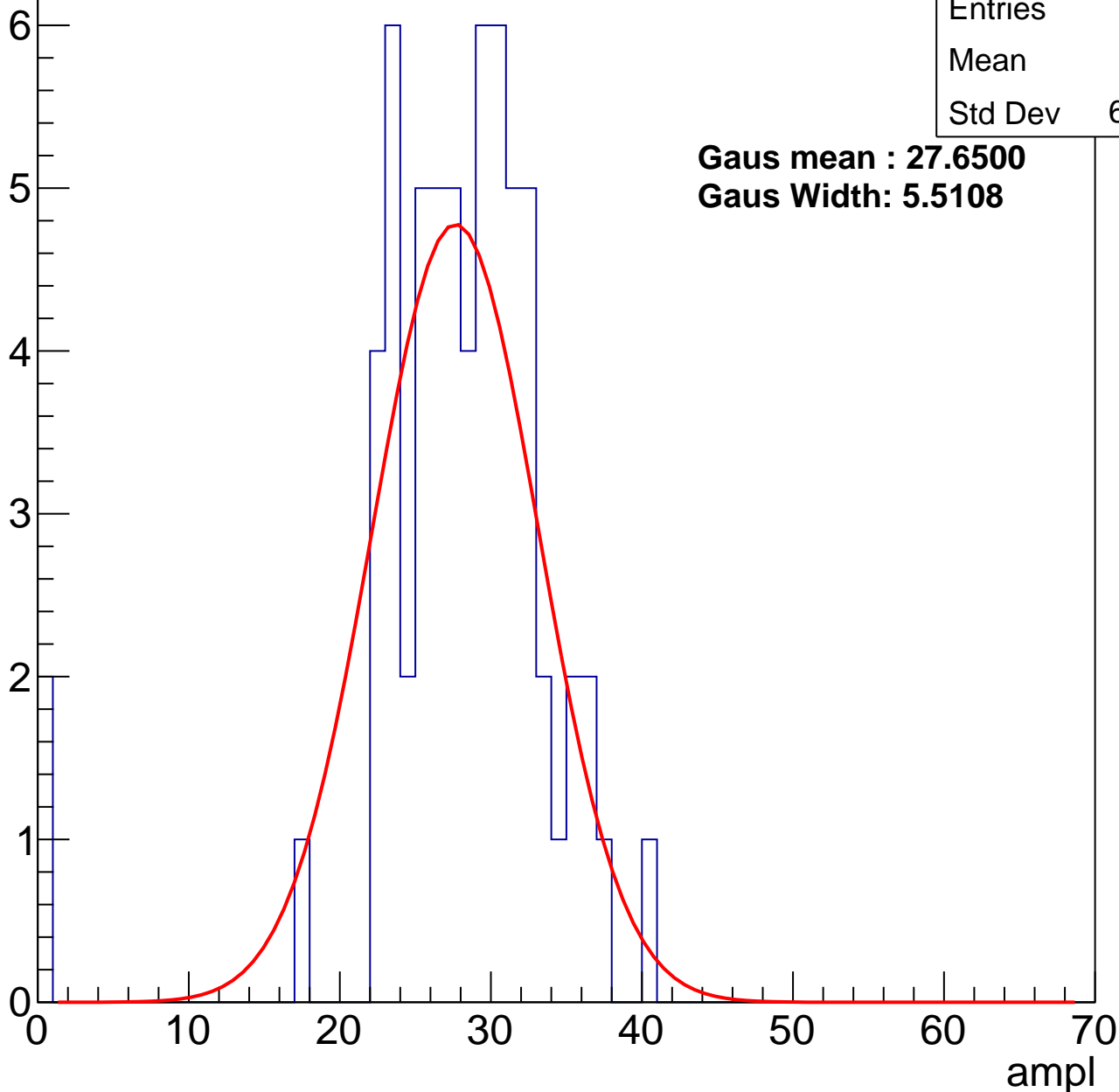
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	27.4
Std Dev	6.509

**Gaus mean : 27.6500**

**Gaus Width: 5.5108**



# B1L103S, U21-ch112, adc1

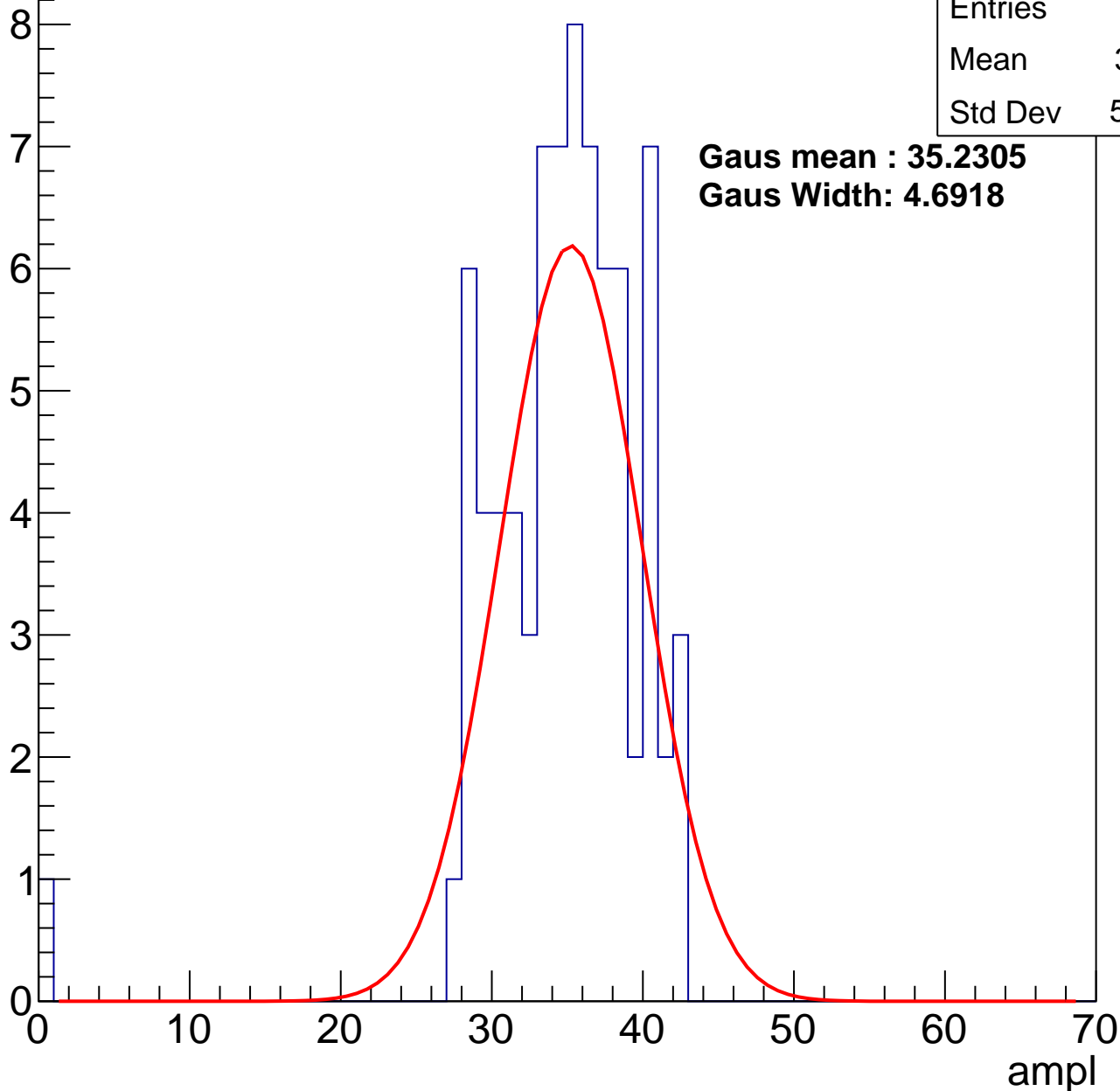
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	34.21
Std Dev	5.564

**Gaus mean : 35.2305**

**Gaus Width: 4.6918**



# B1L103S, U21-ch112, adc2

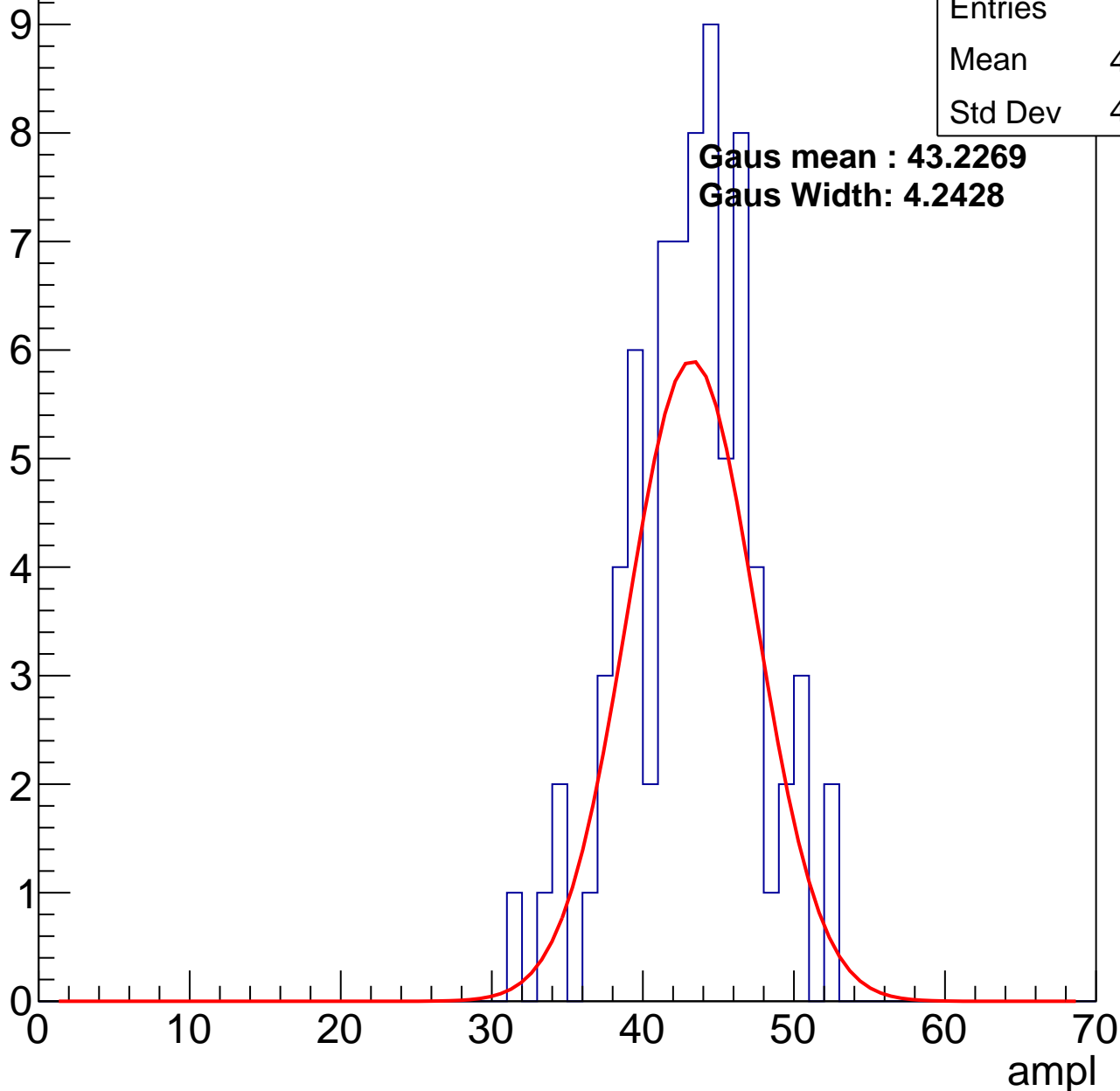
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	42.72
Std Dev	4.257

**Gaus mean : 43.2269**

**Gaus Width: 4.2428**

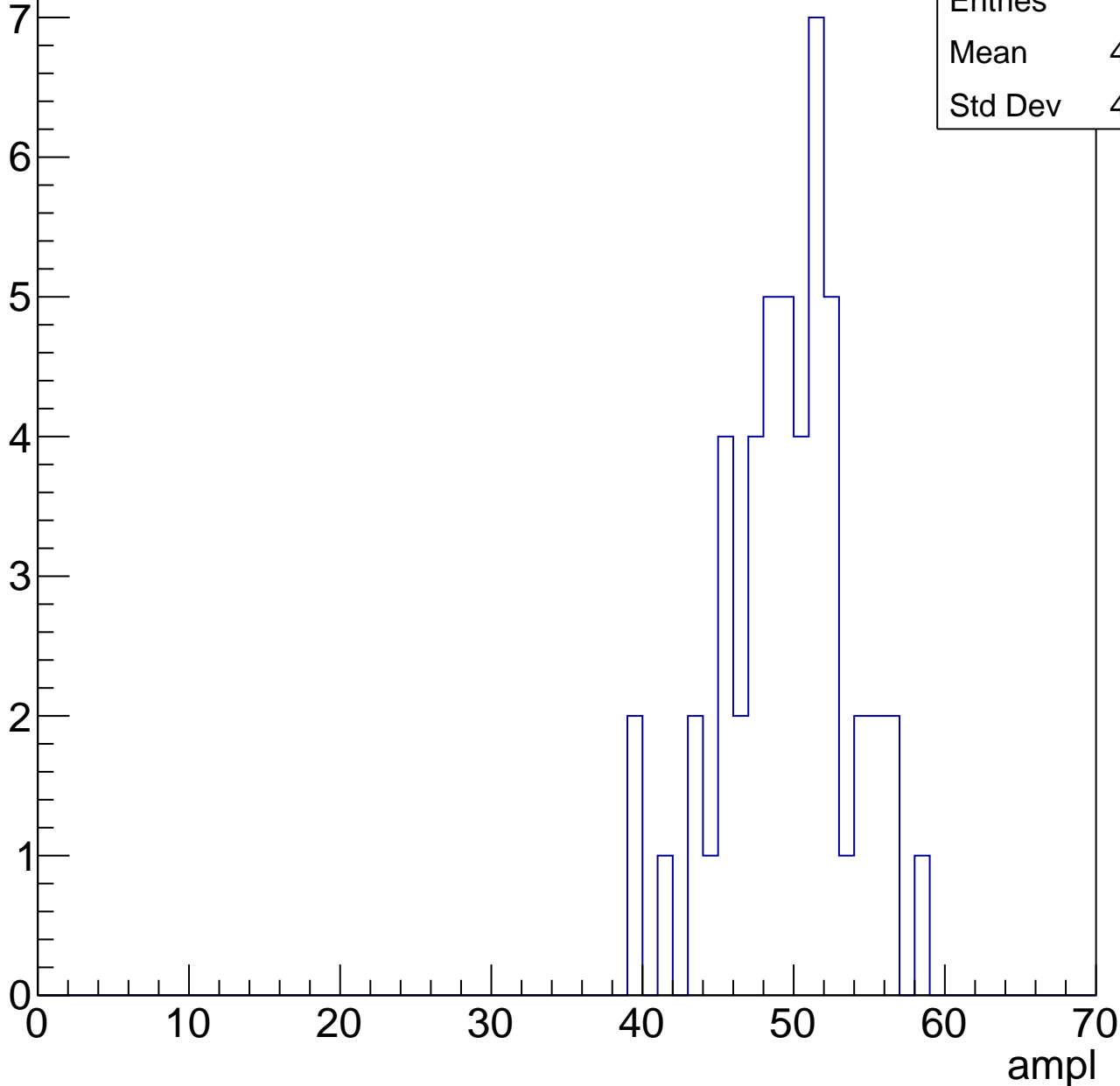


# B1L103S, U21-ch112, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	49.04
Std Dev	4.142

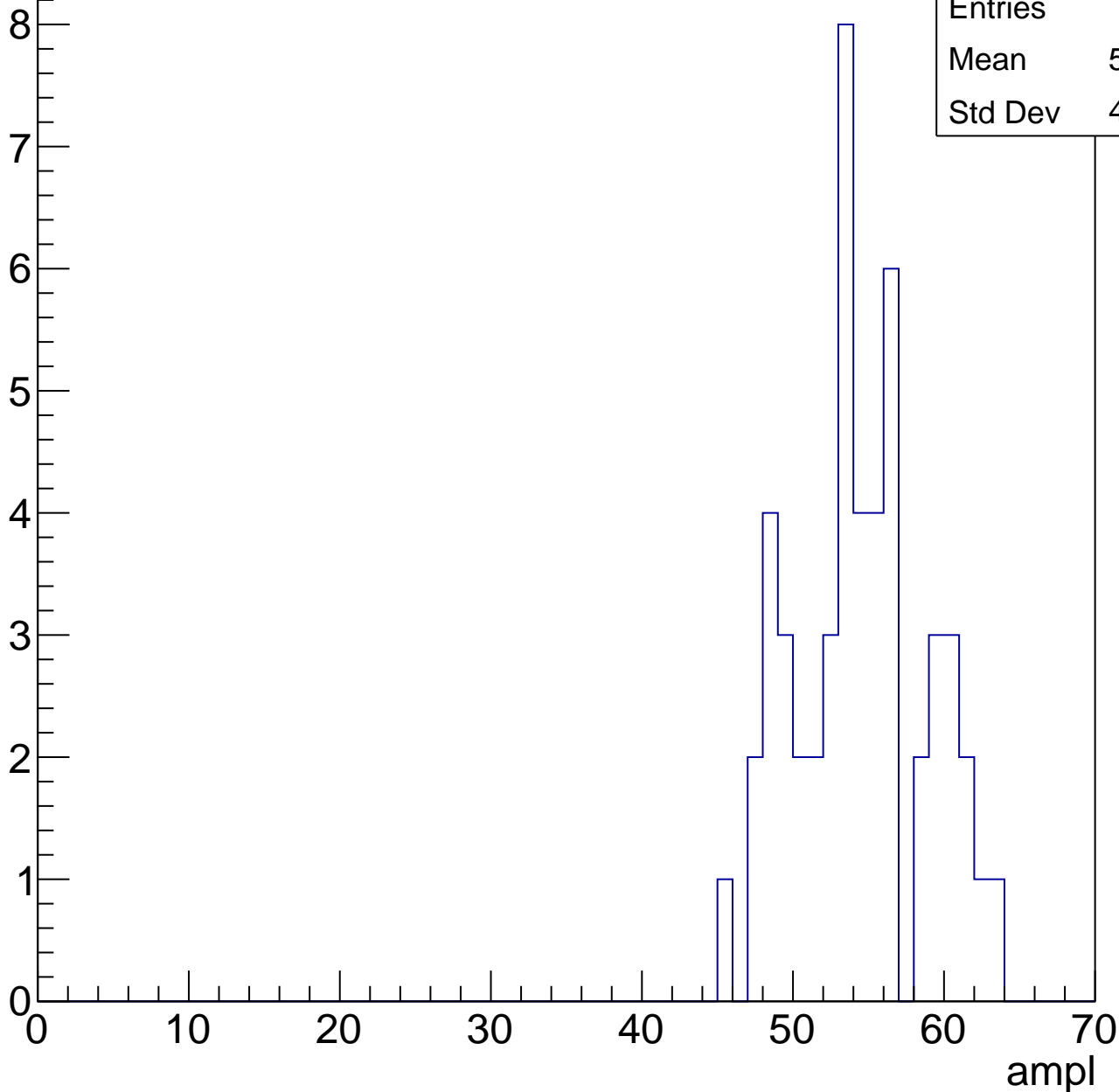


# B1L103S, U21-ch112, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	53.96
Std Dev	4.325



# B1L103S, U21-ch112, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	54
Mean	57.35
Std Dev	8.47

Entry

10

8

6

4

2

0

0

10

20

30

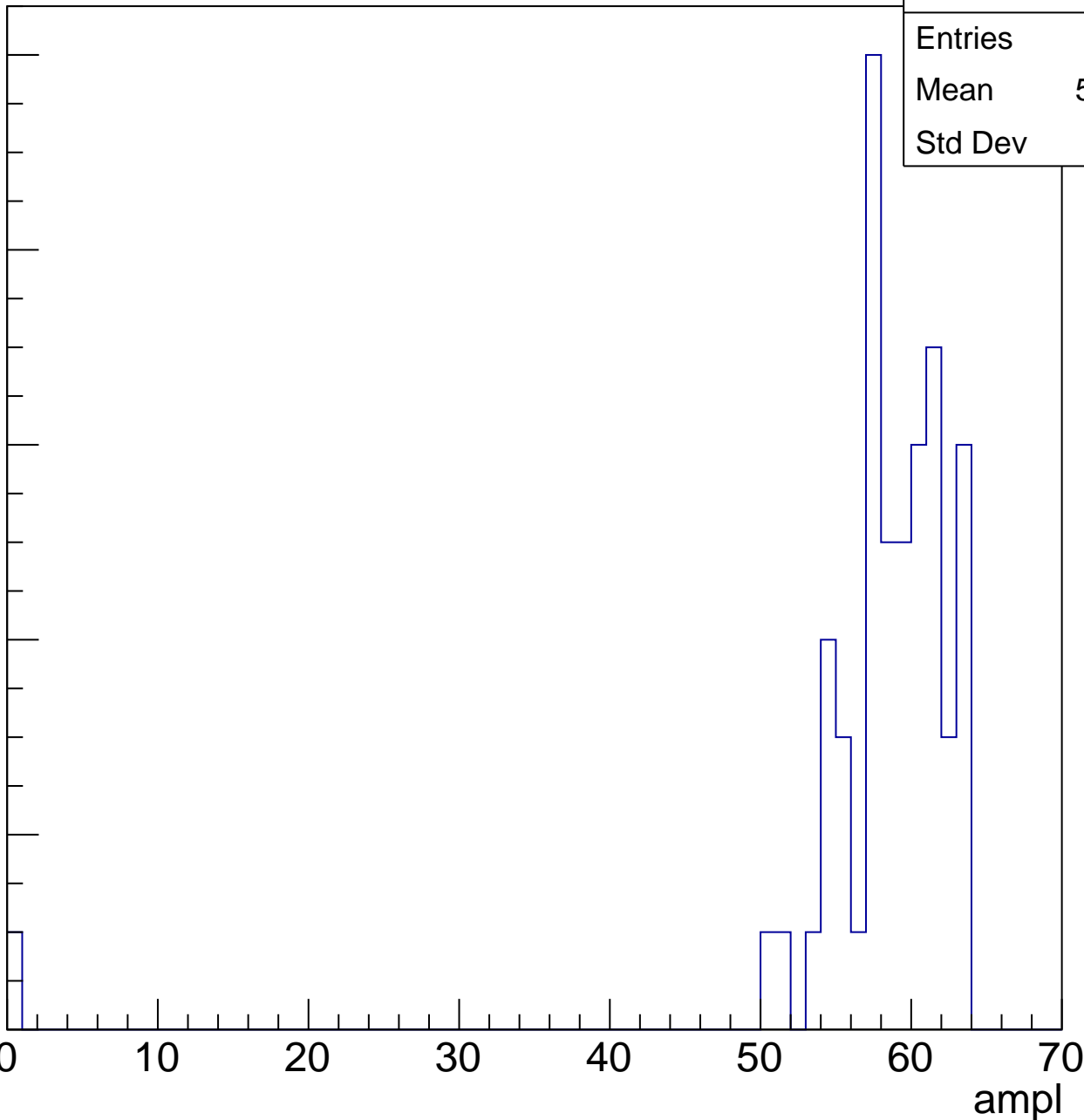
40

50

60

70

ampl

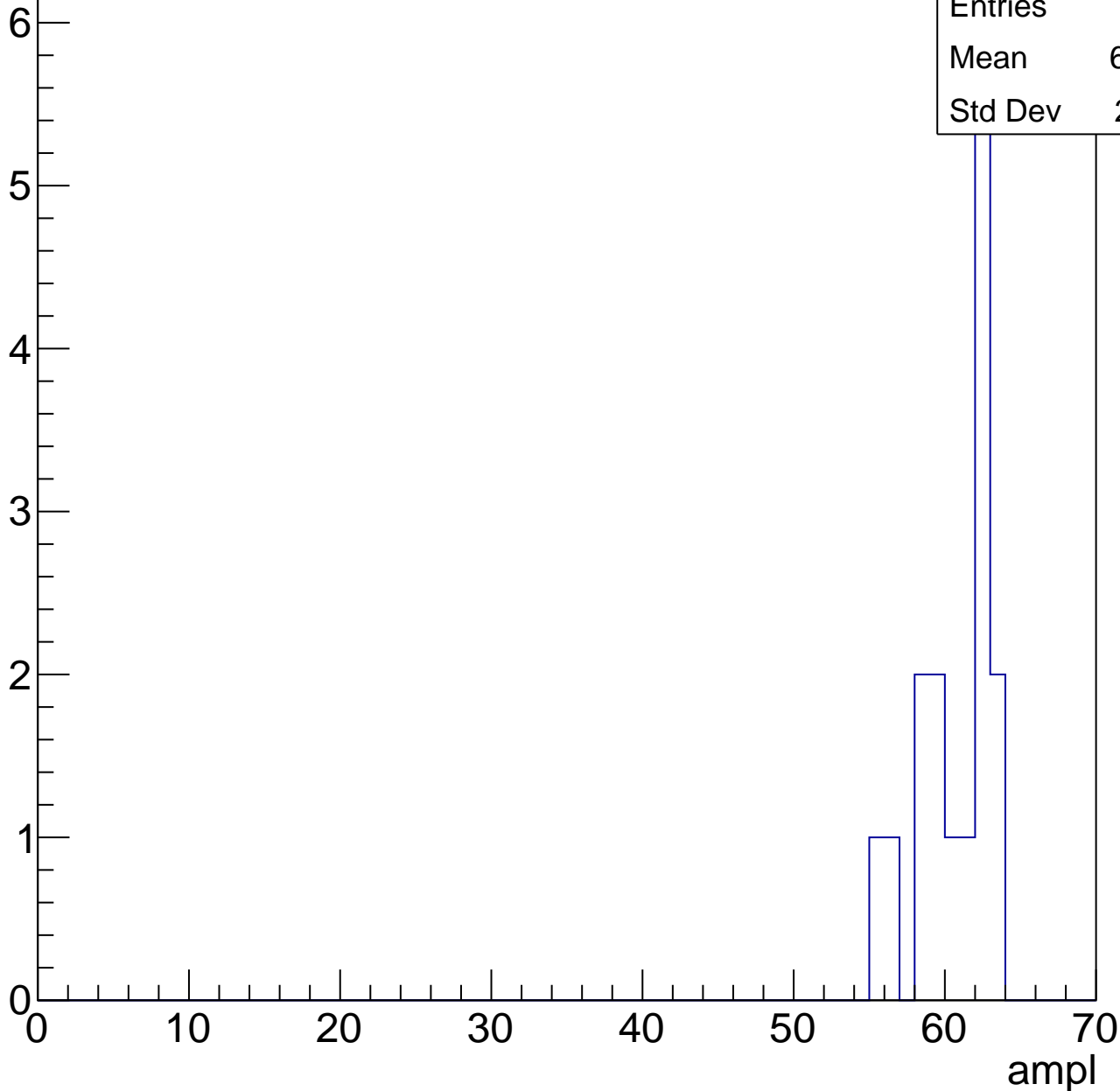


# B1L103S, U21-ch112, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	16
Mean	60.25
Std Dev	2.411





# B1L103S, U21-ch112, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

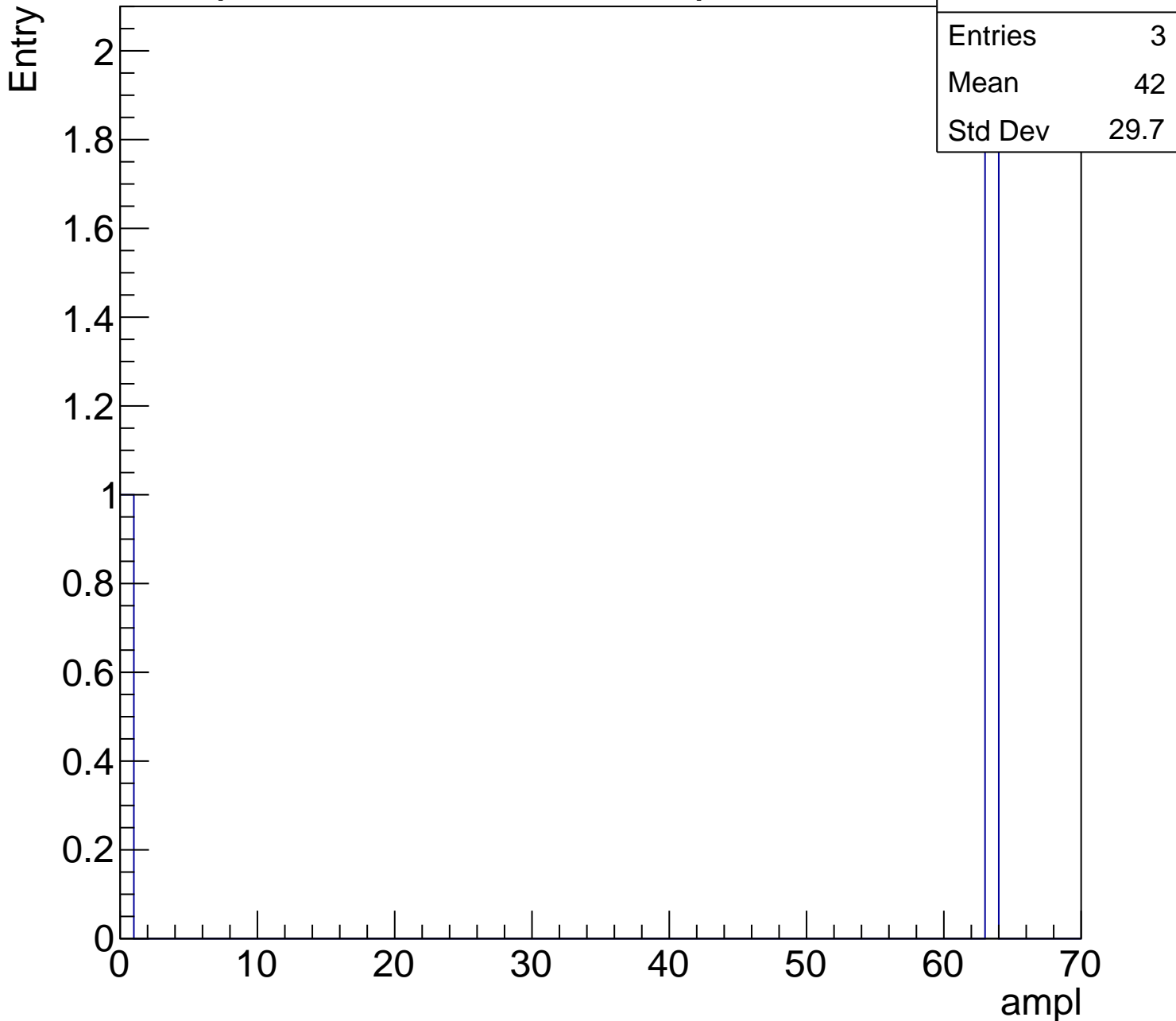
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	42
Std Dev	29.7

0 10 20 30 40 50 60 70

ampl



# B1L103S, U21-ch113, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	66
Mean	28.94
Std Dev	3.781

**Gaus mean : 28.8148**

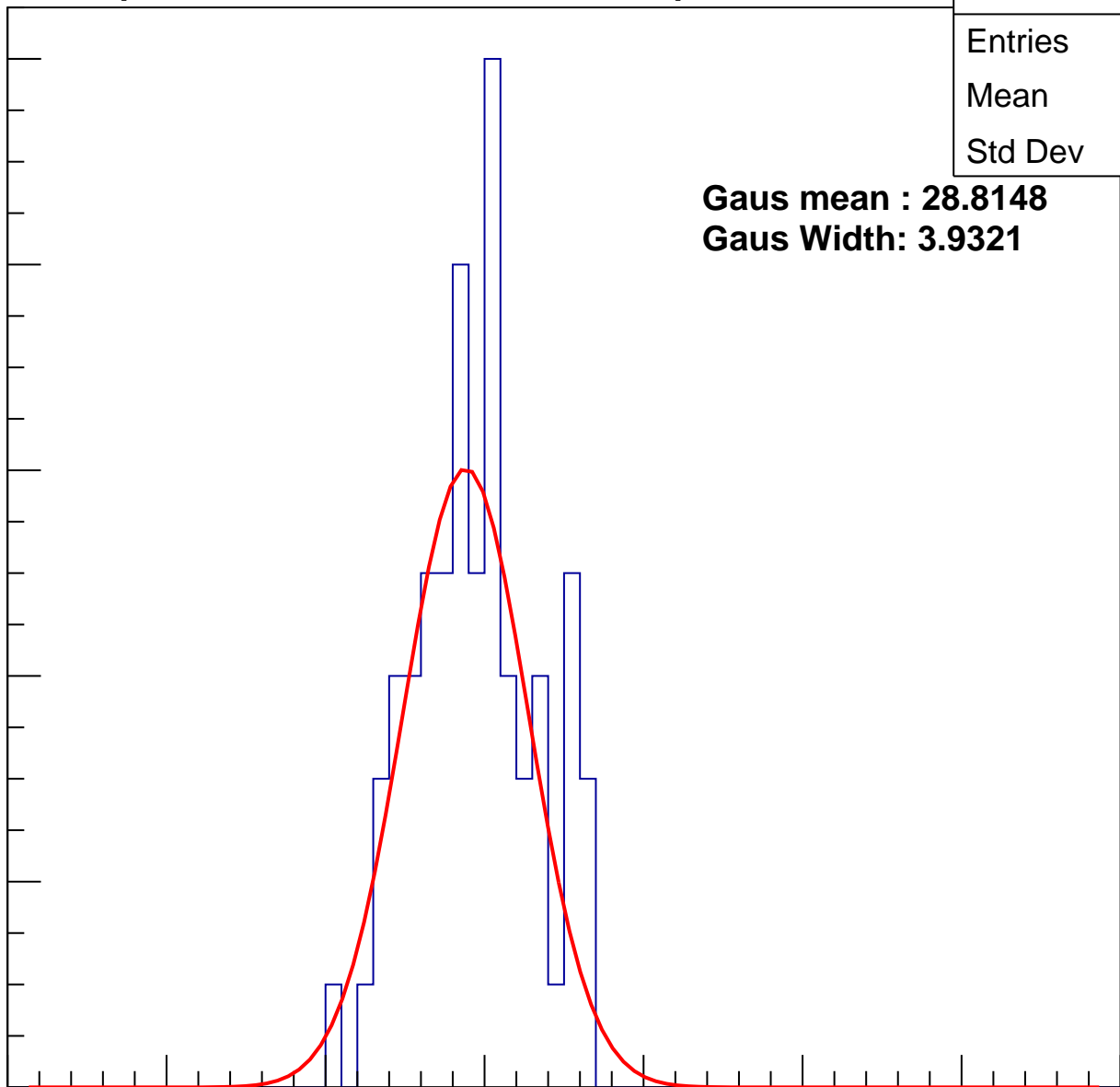
**Gaus Width: 3.9321**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U21-ch113, adc1

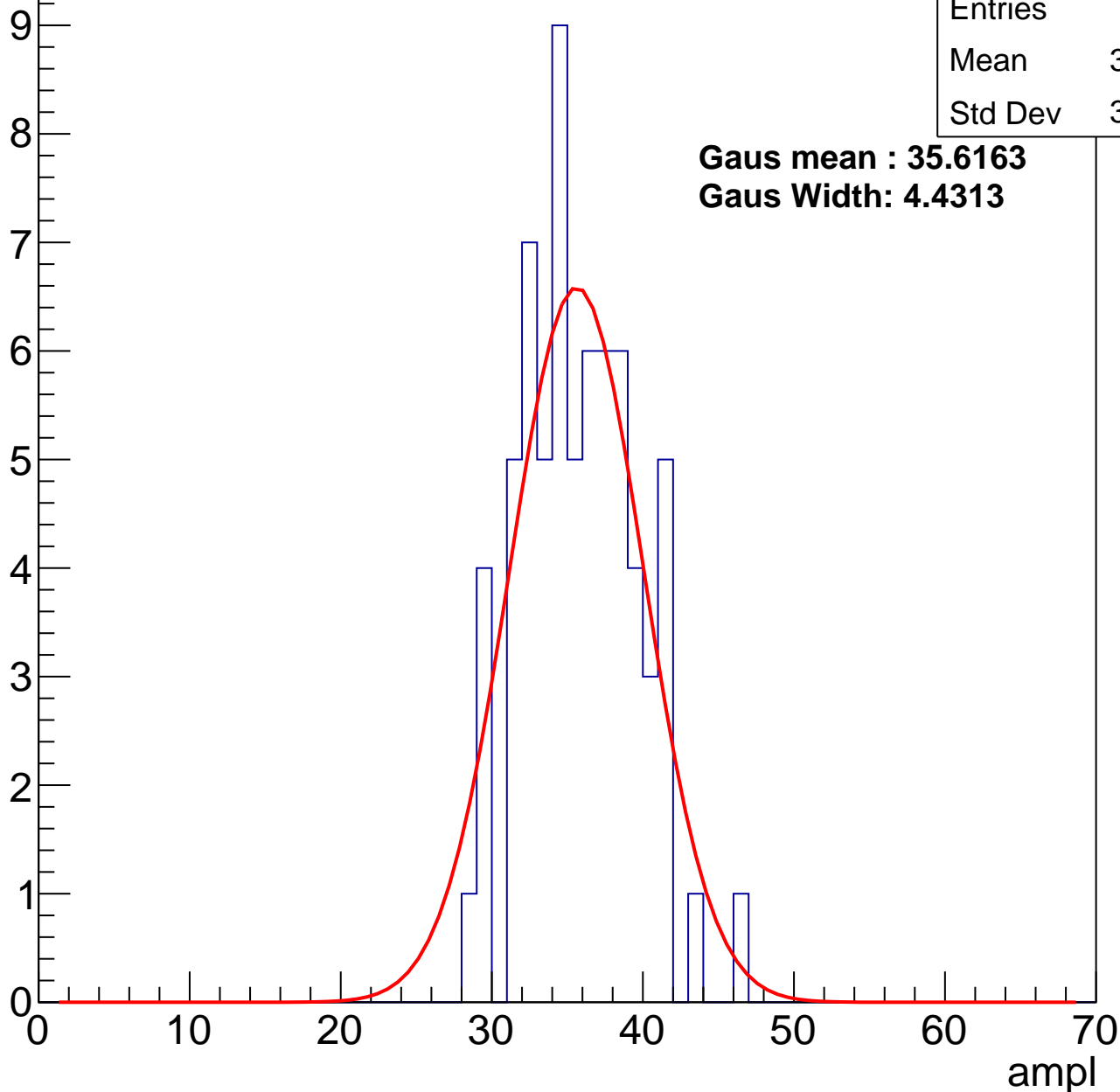
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	35.37
Std Dev	3.726

**Gaus mean : 35.6163**

**Gaus Width: 4.4313**

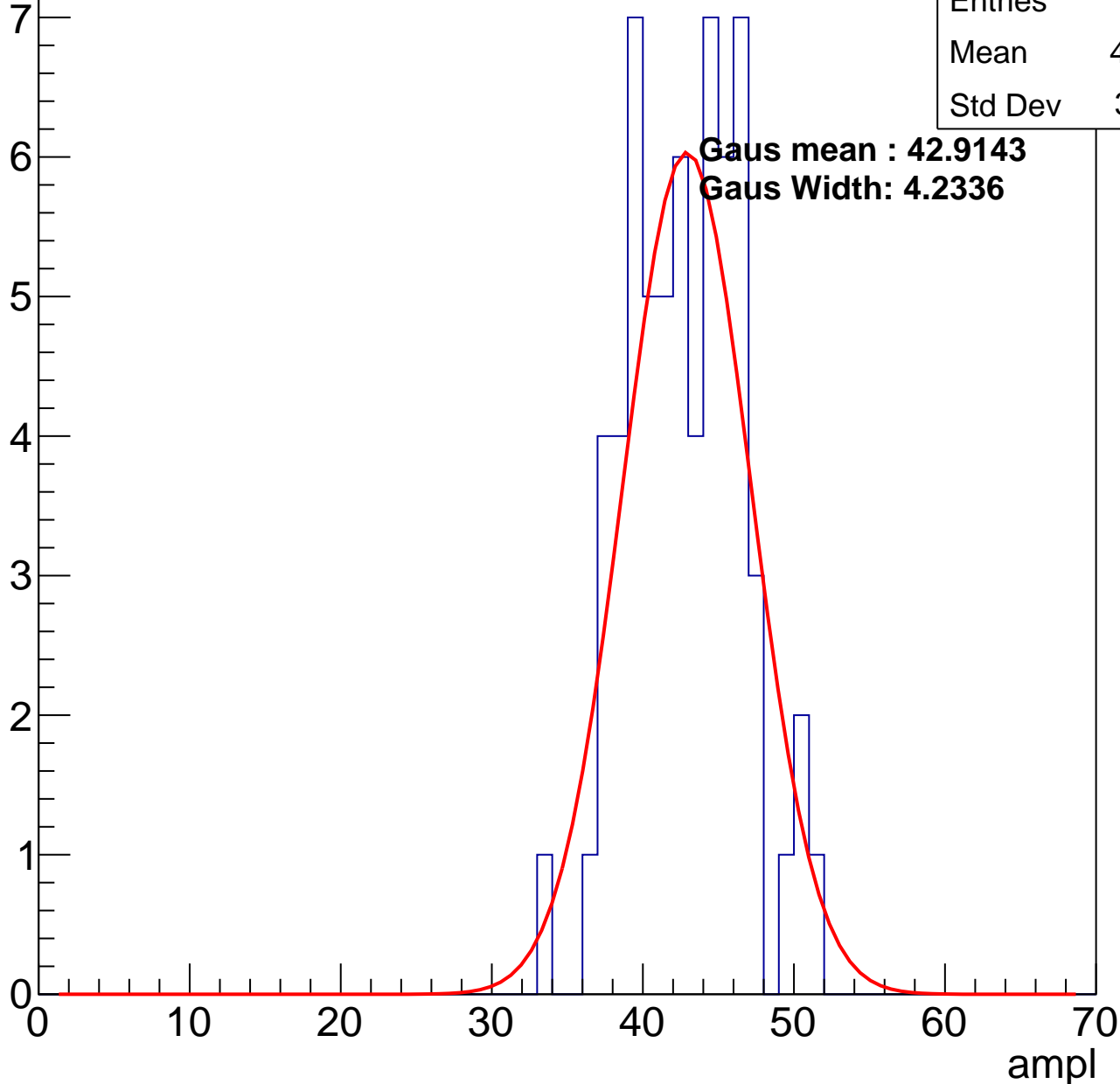


# B1L103S, U21-ch113, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	42.38
Std Dev	3.731

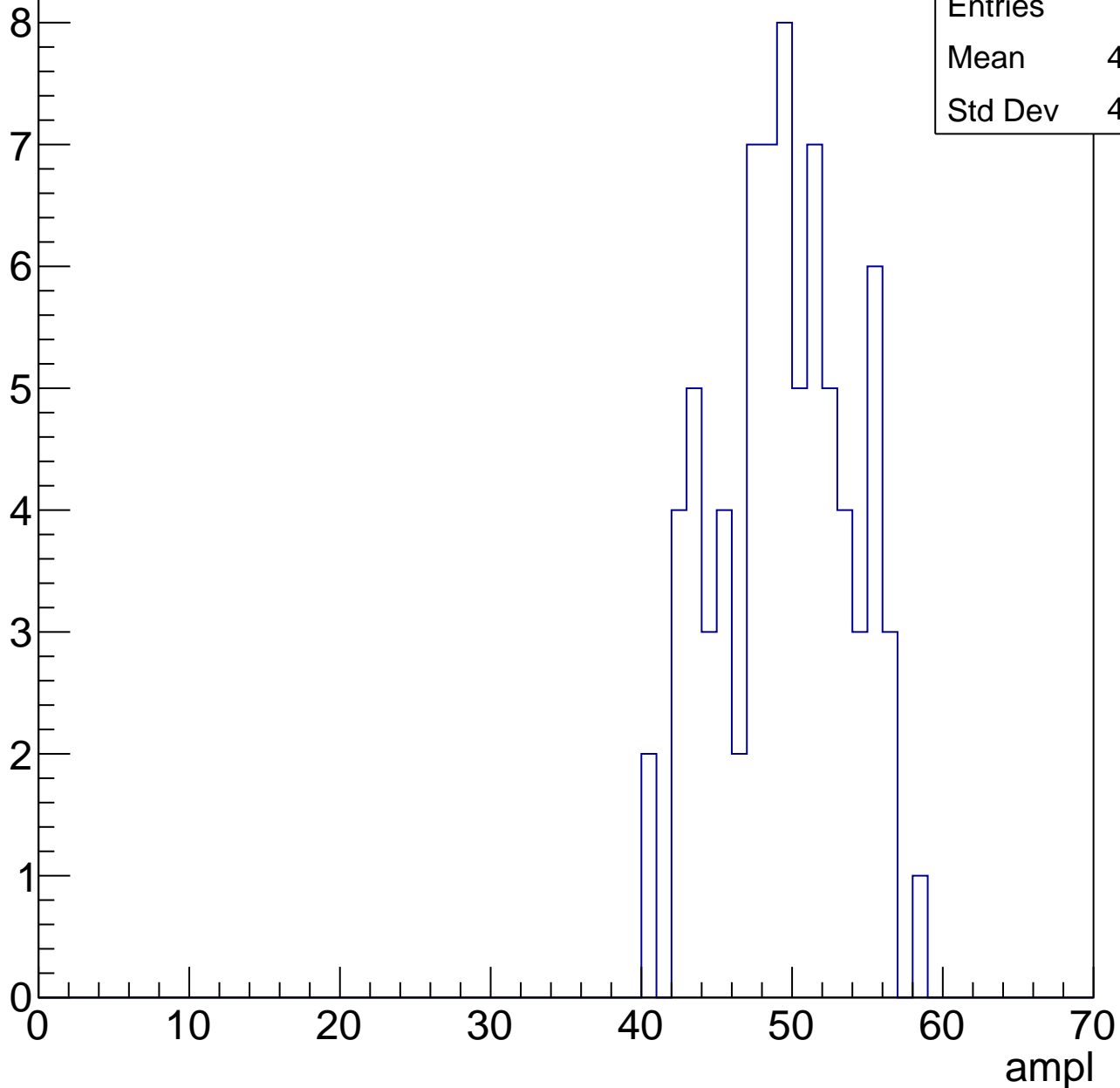


# B1L103S, U21-ch113, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	48.96
Std Dev	4.278

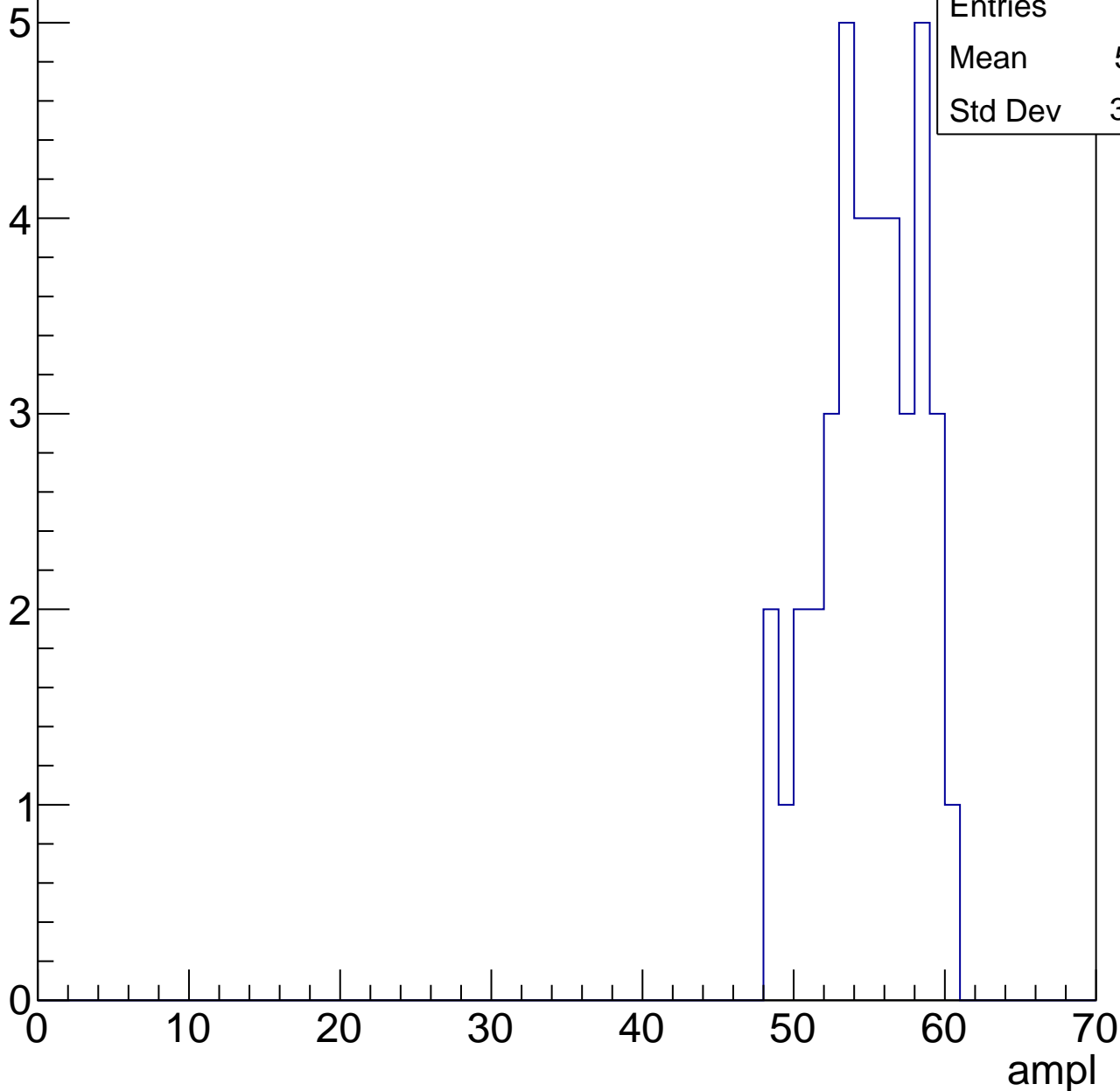


# B1L103S, U21-ch113, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	39
Mean	54.51
Std Dev	3.169

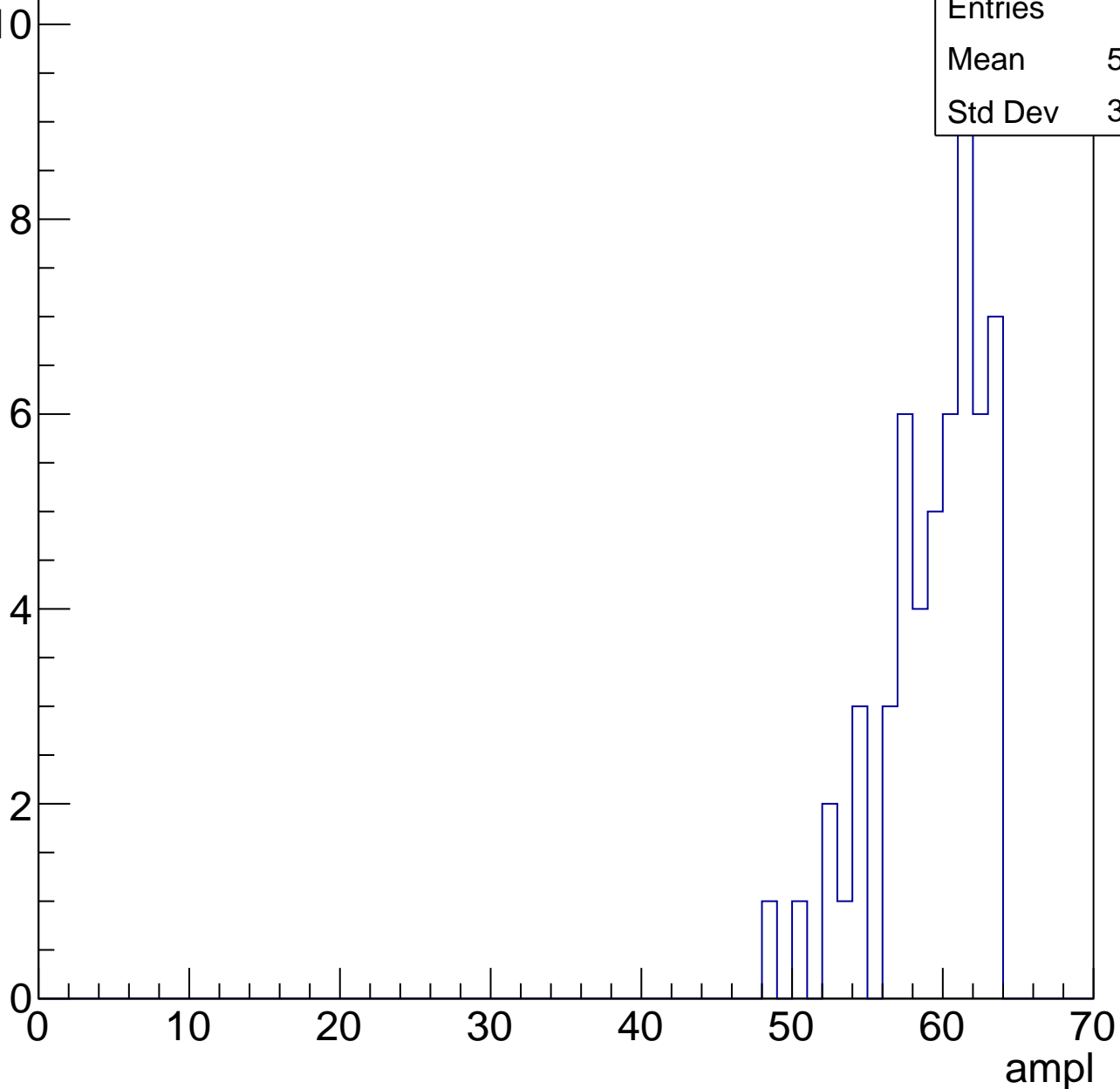


# B1L103S, U21-ch113, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

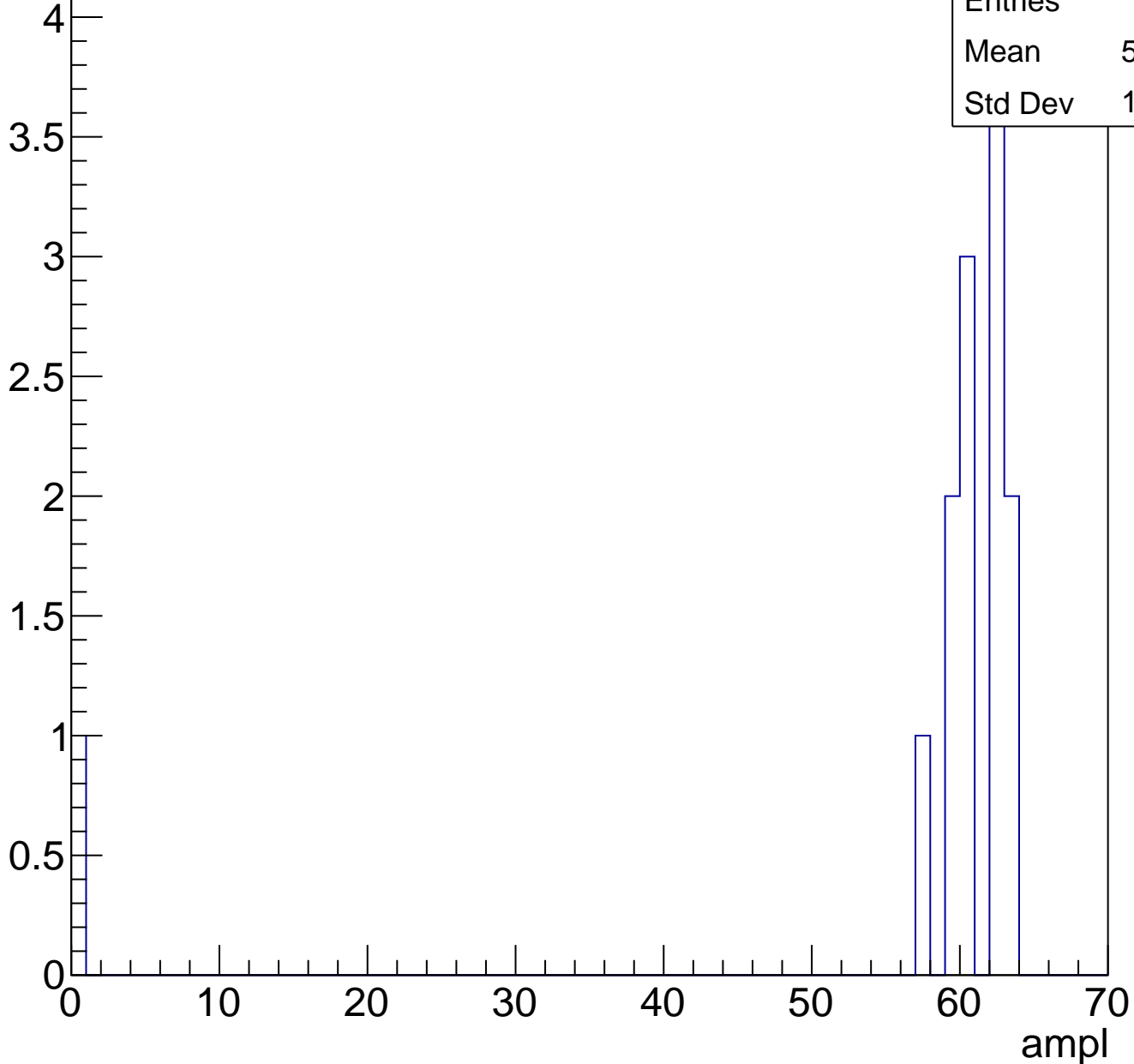
Entries	55
Mean	58.85
Std Dev	3.508



# B1L103S, U21-ch113, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U21-ch113, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U21-ch114, adc0

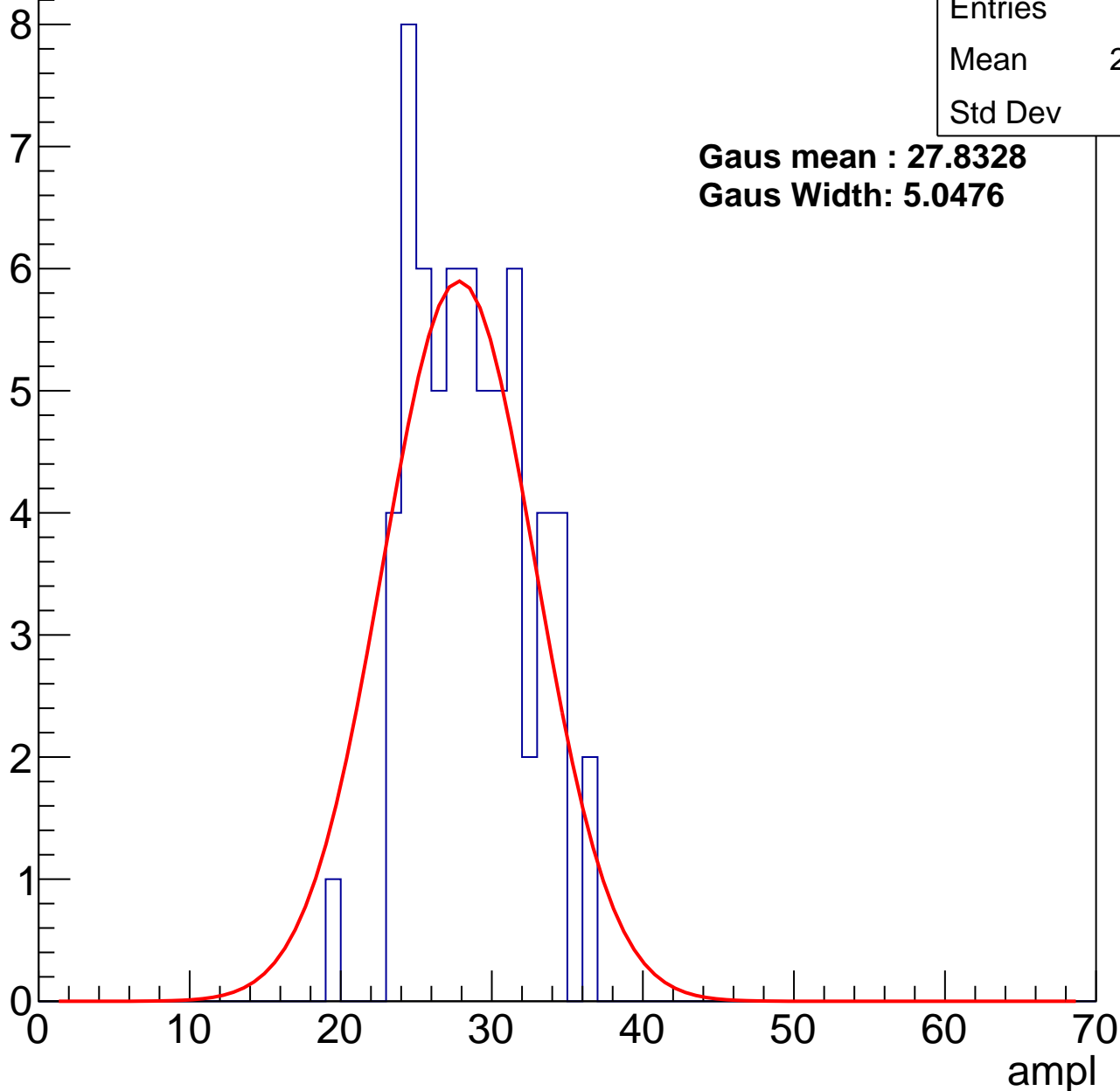
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	28.09
Std Dev	3.69

**Gaus mean : 27.8328**

**Gaus Width: 5.0476**



# B1L103S, U21-ch114, adc1

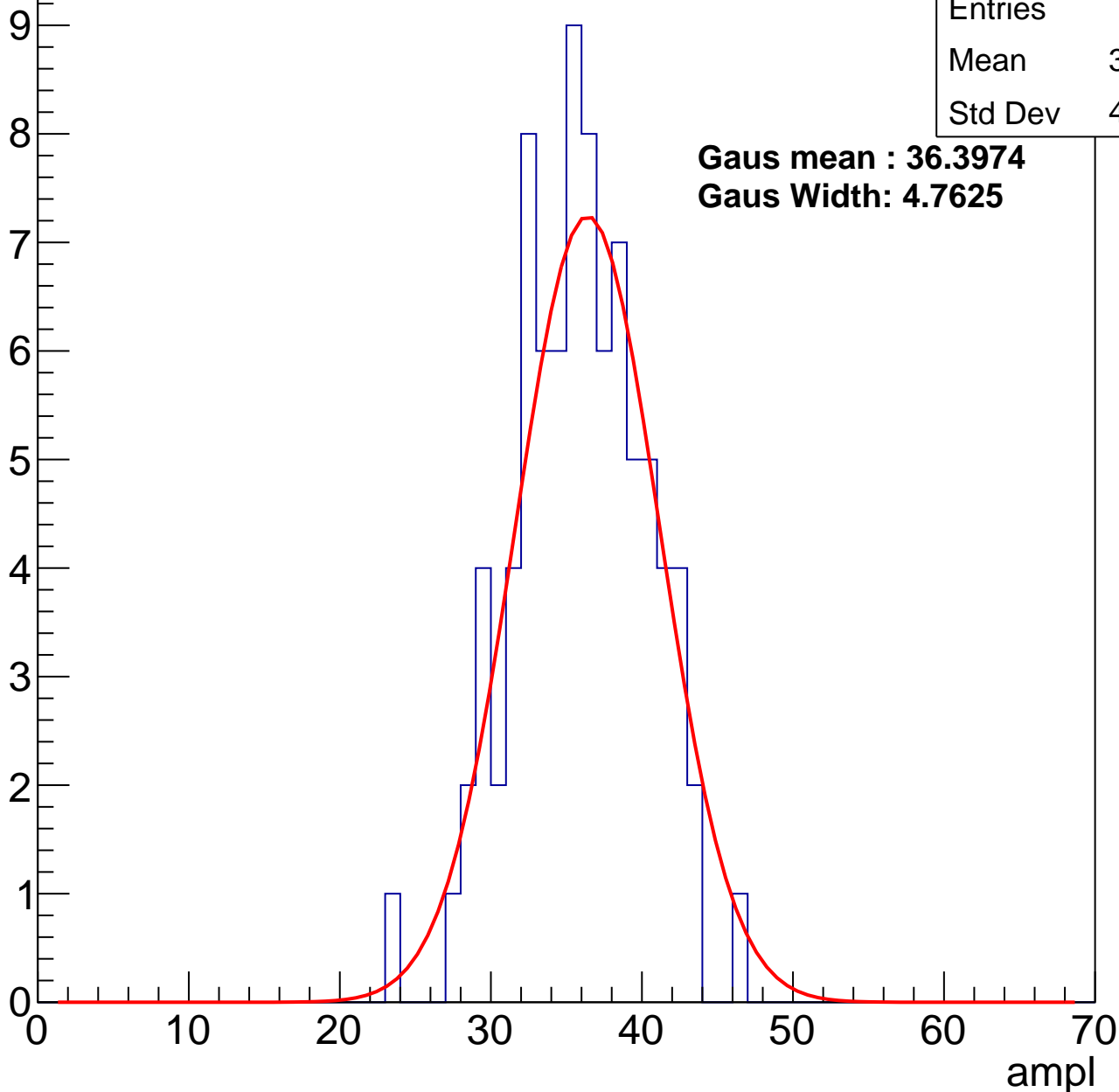
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	85
Mean	35.46
Std Dev	4.252

**Gaus mean : 36.3974**

**Gaus Width: 4.7625**



# B1L103S, U21-ch114, adc2

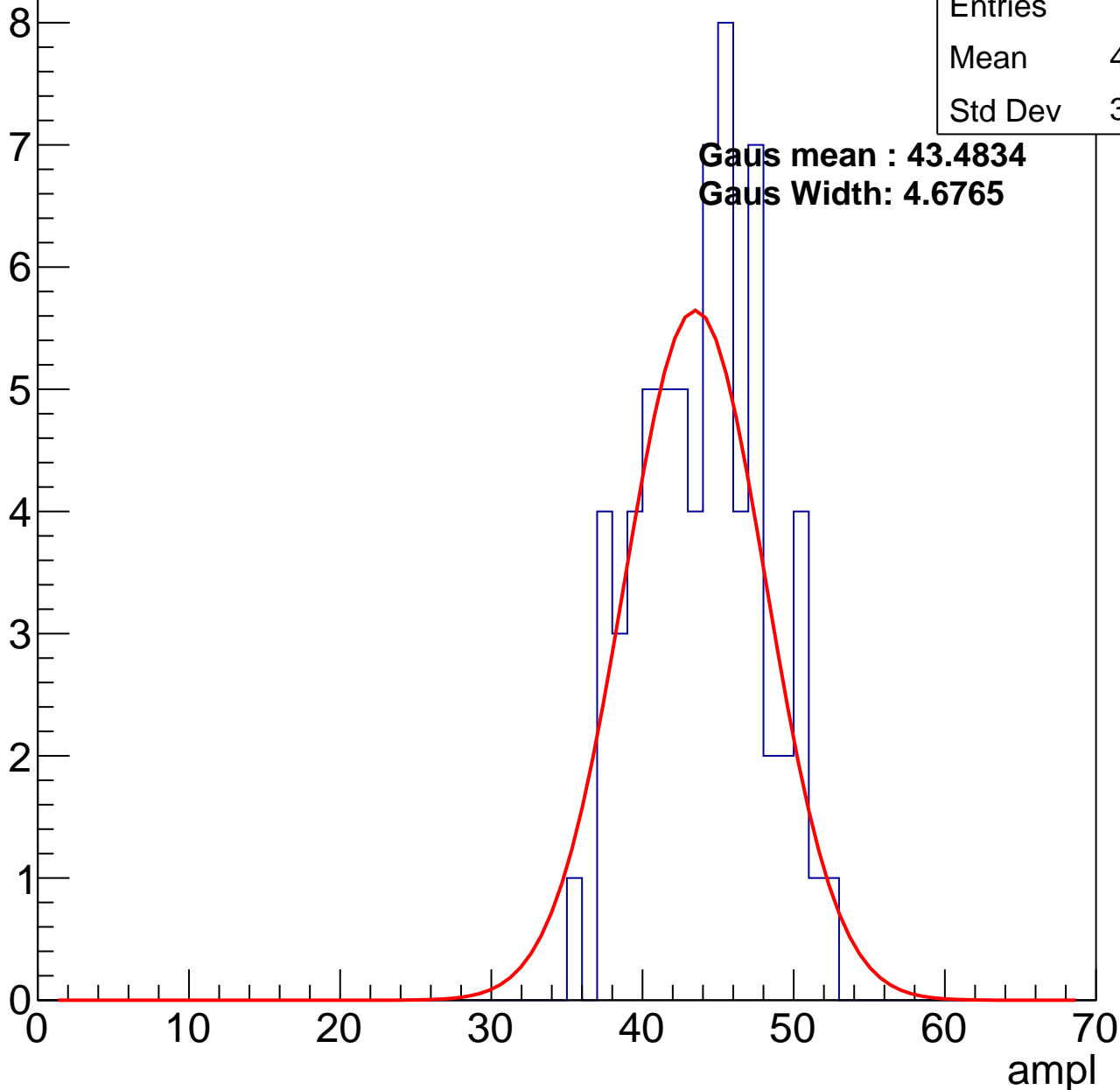
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	43.55
Std Dev	3.952

**Gaus mean : 43.4834**

**Gaus Width: 4.6765**

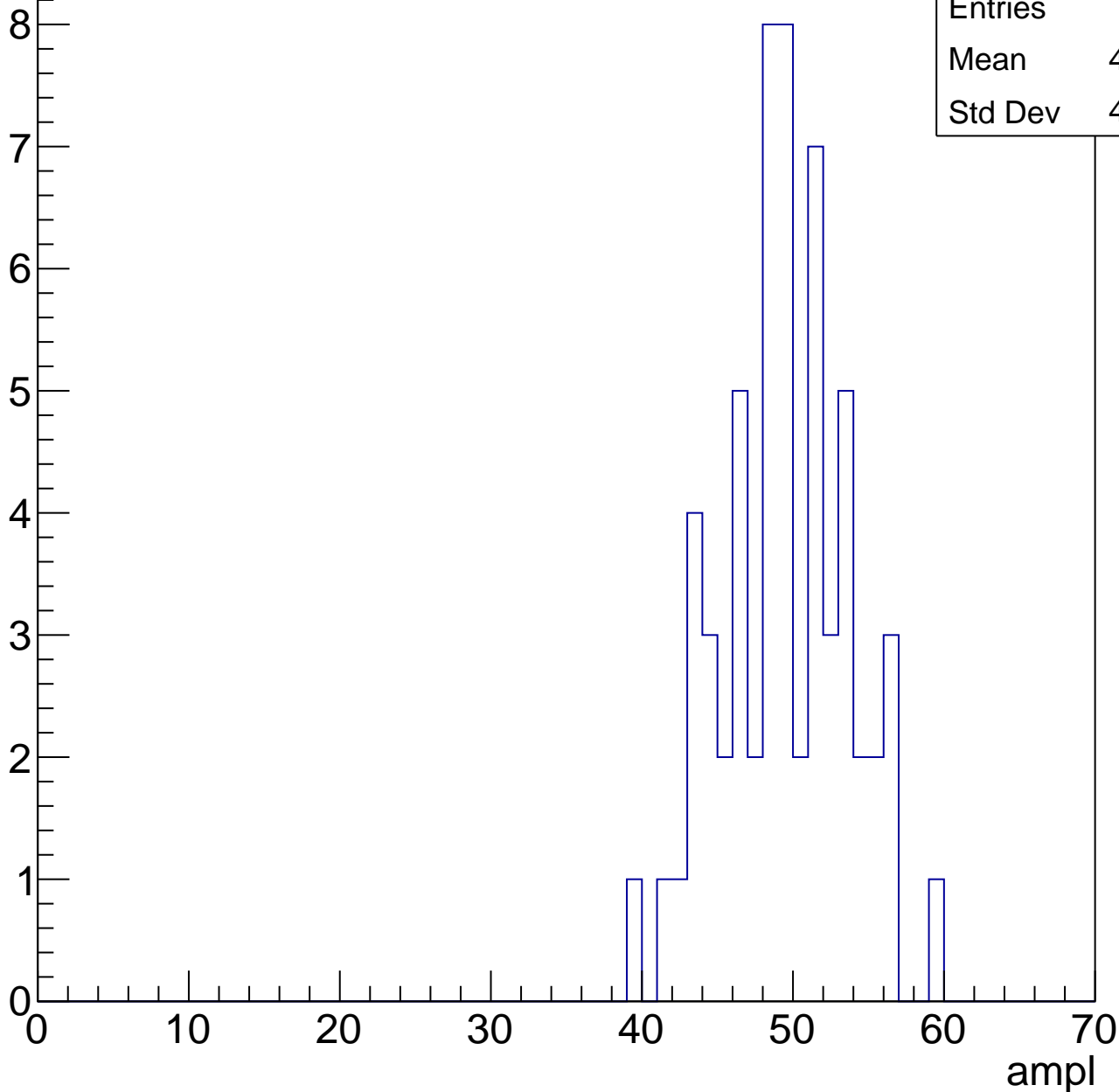


# B1L103S, U21-ch114, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	48.98
Std Dev	4.145

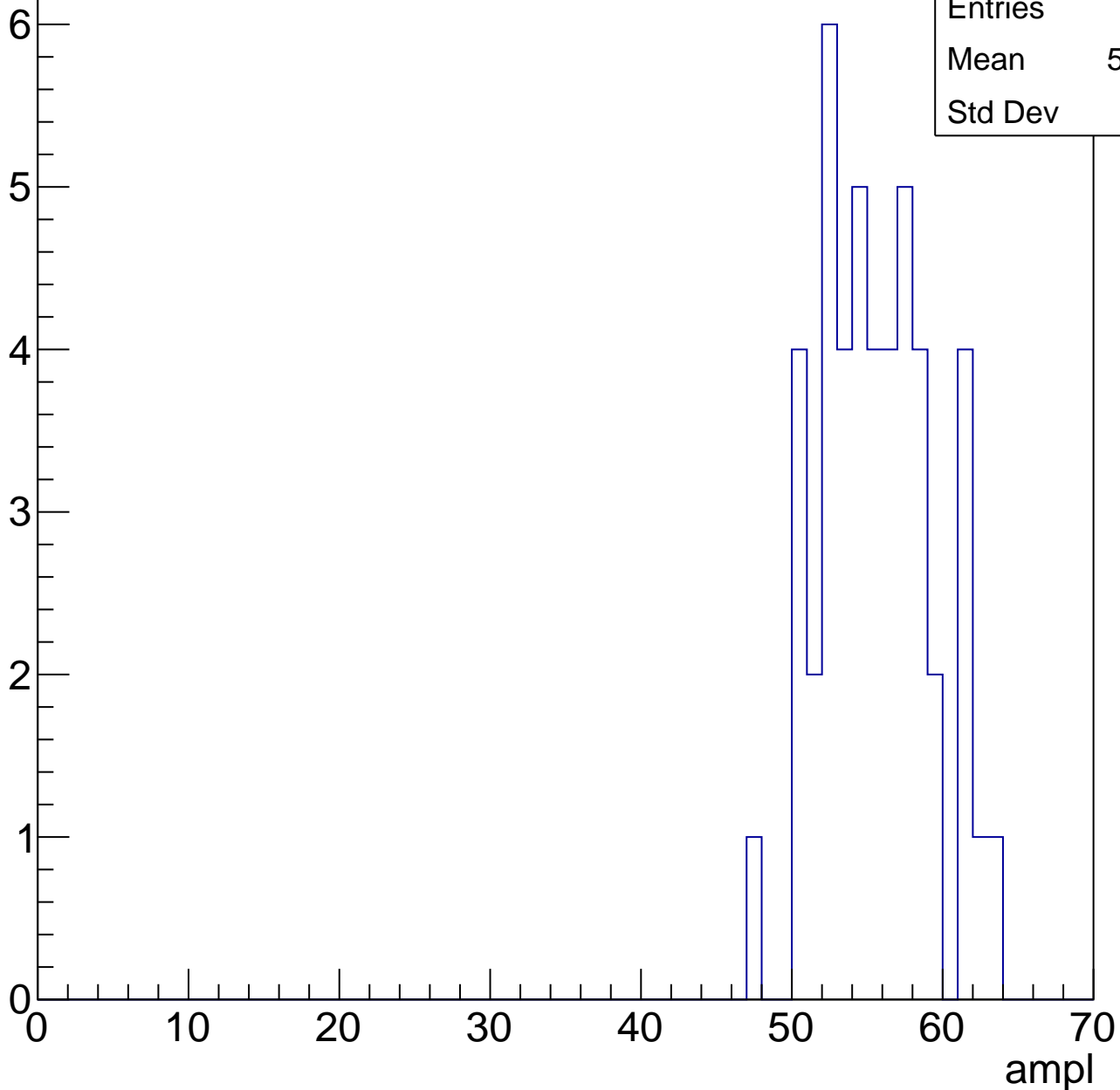


# B1L103S, U21-ch114, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	47
Mean	55.13
Std Dev	3.63

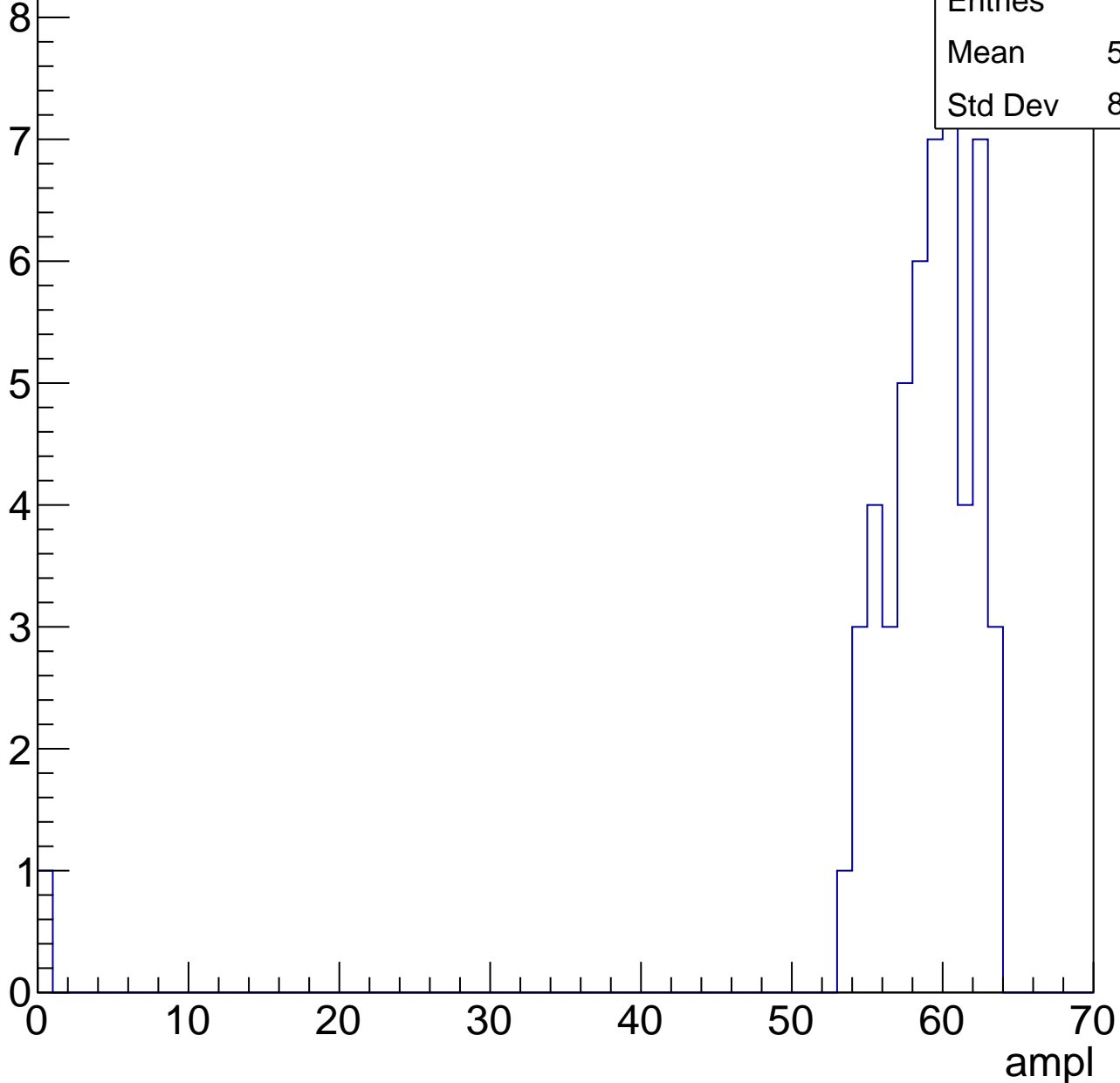


# B1L103S, U21-ch114, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	57.62
Std Dev	8.486



# B1L103S, U21-ch114, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	8
Mean	61.5
Std Dev	1.118

0 10 20 30 40 50 60 70

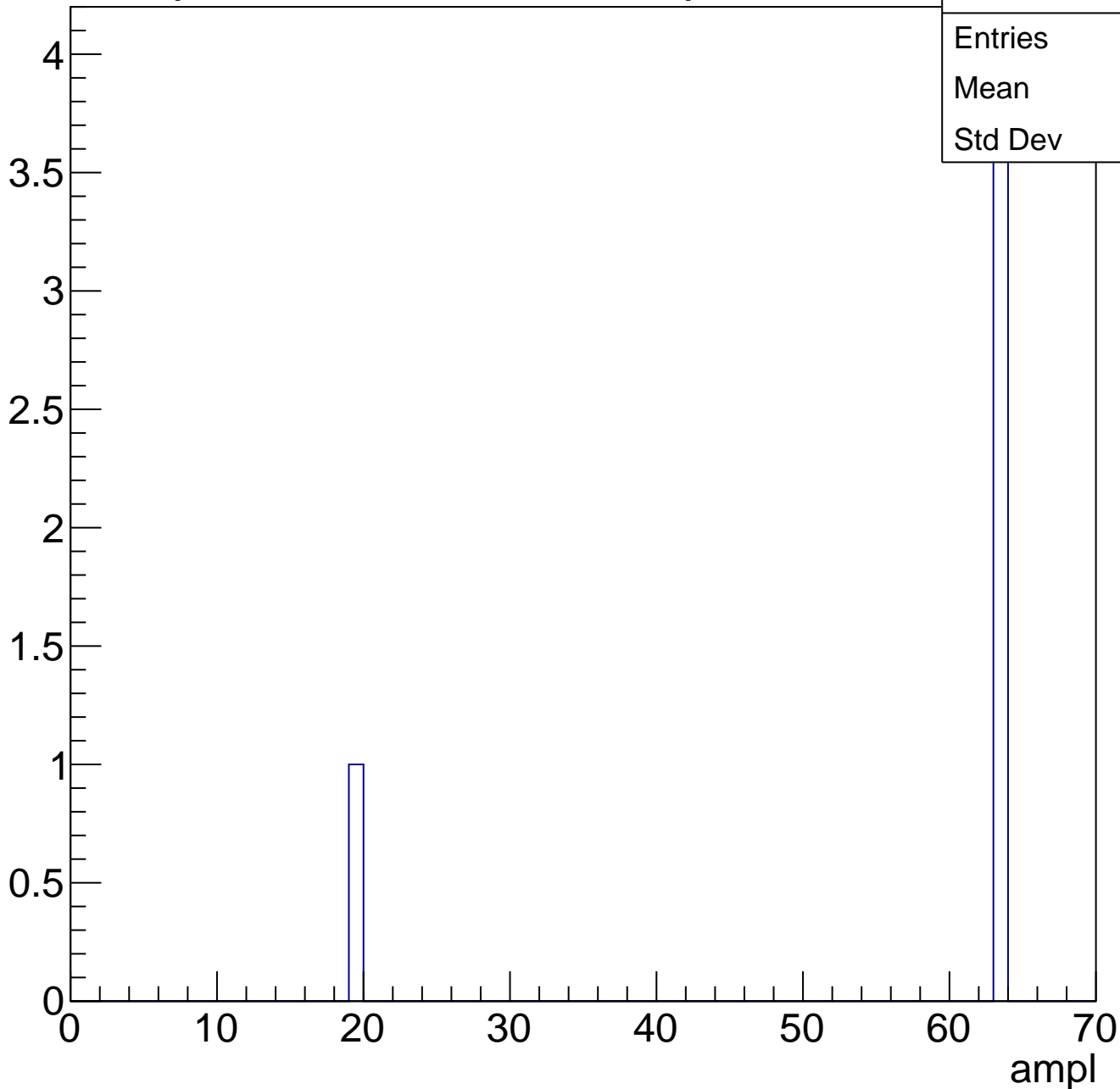
ampl



# B1L103S, U21-ch114, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U21-ch115, adc0

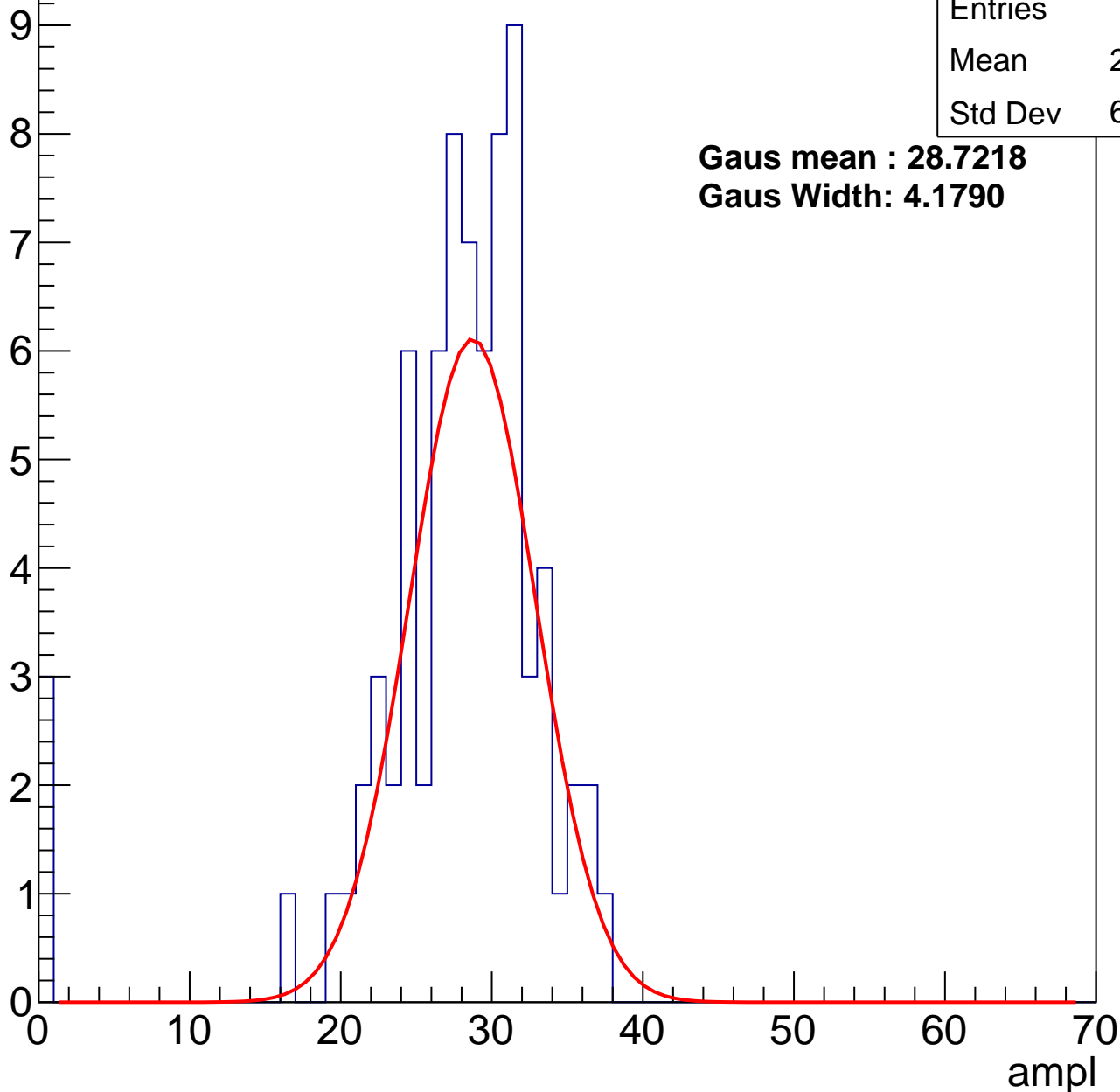
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	26.99
Std Dev	6.768

**Gaus mean : 28.7218**

**Gaus Width: 4.1790**



# B1L103S, U21-ch115, adc1

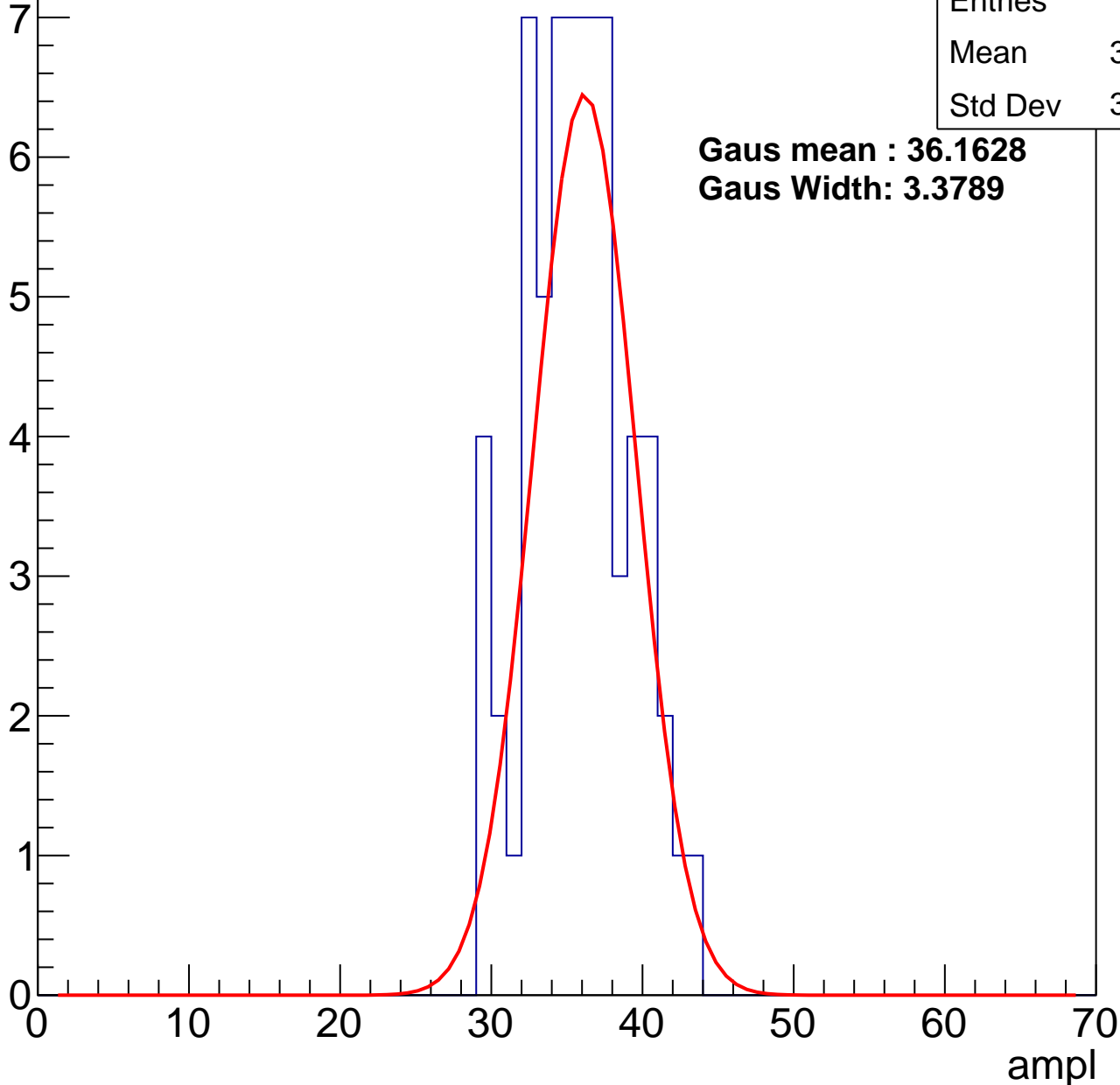
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	35.27
Std Dev	3.375

**Gaus mean : 36.1628**

**Gaus Width: 3.3789**



# B1L103S, U21-ch115, adc2

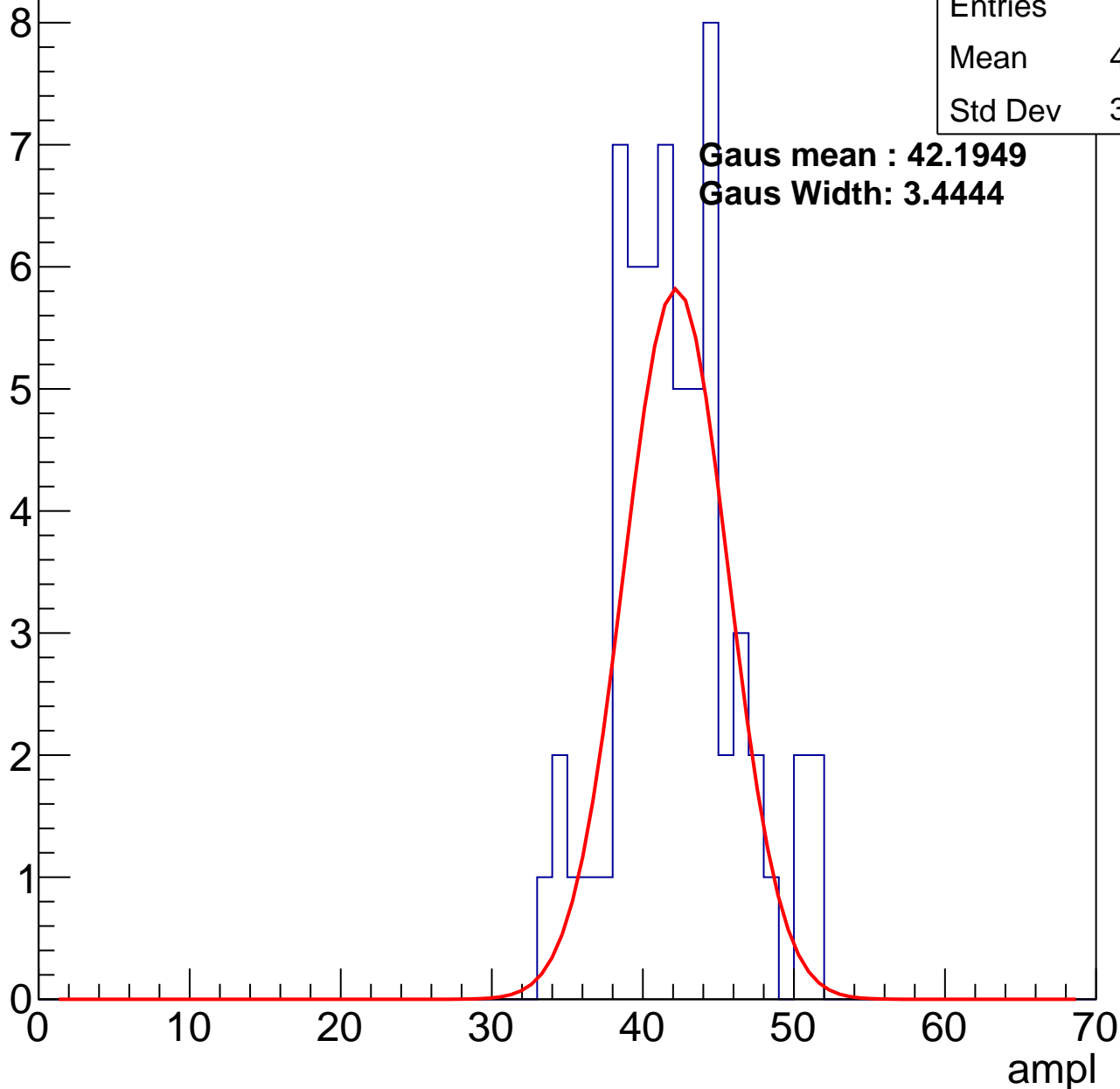
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	41.69
Std Dev	3.994

**Gaus mean : 42.1949**

**Gaus Width: 3.4444**

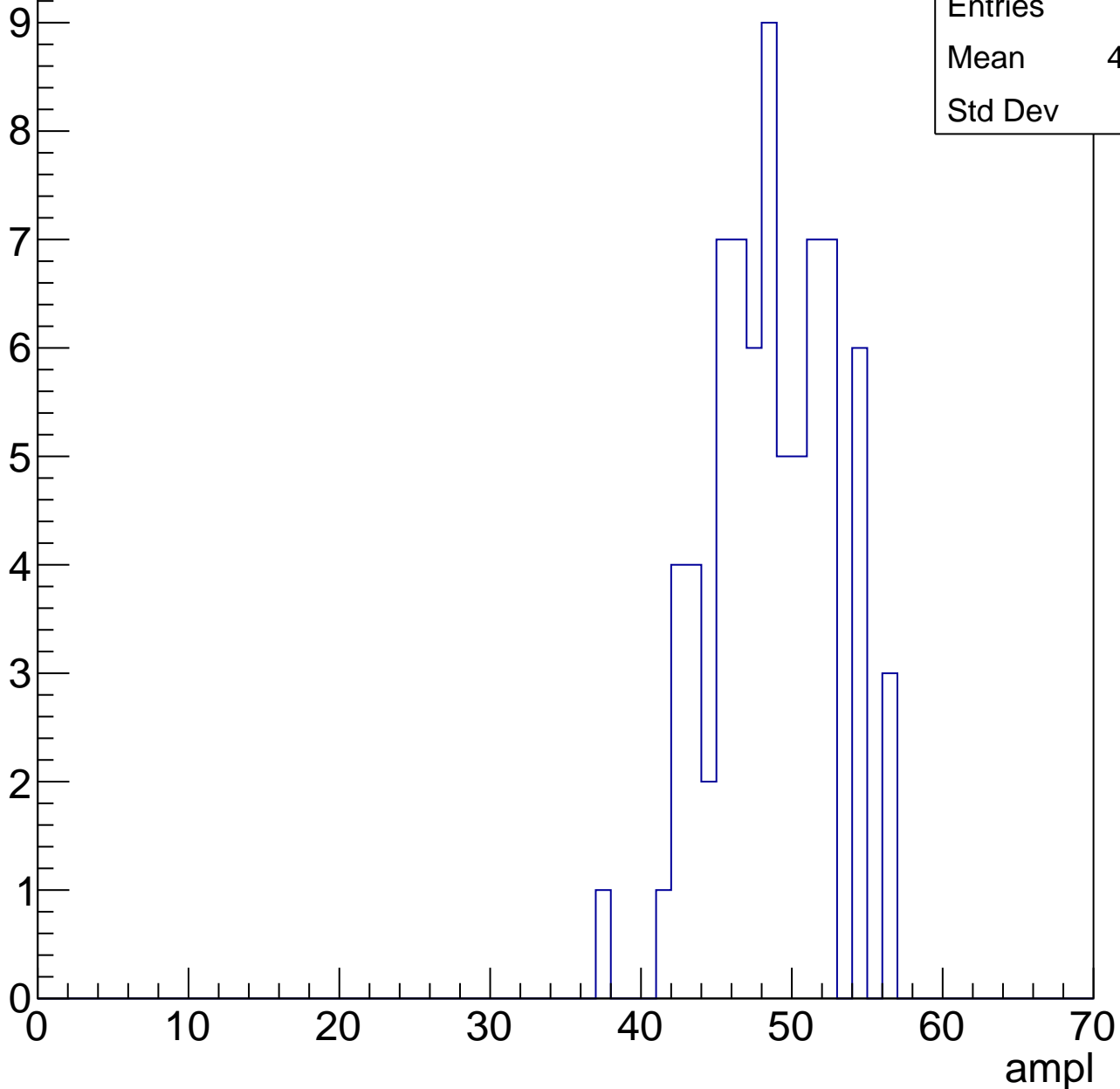


# B1L103S, U21-ch115, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	48.18
Std Dev	3.94

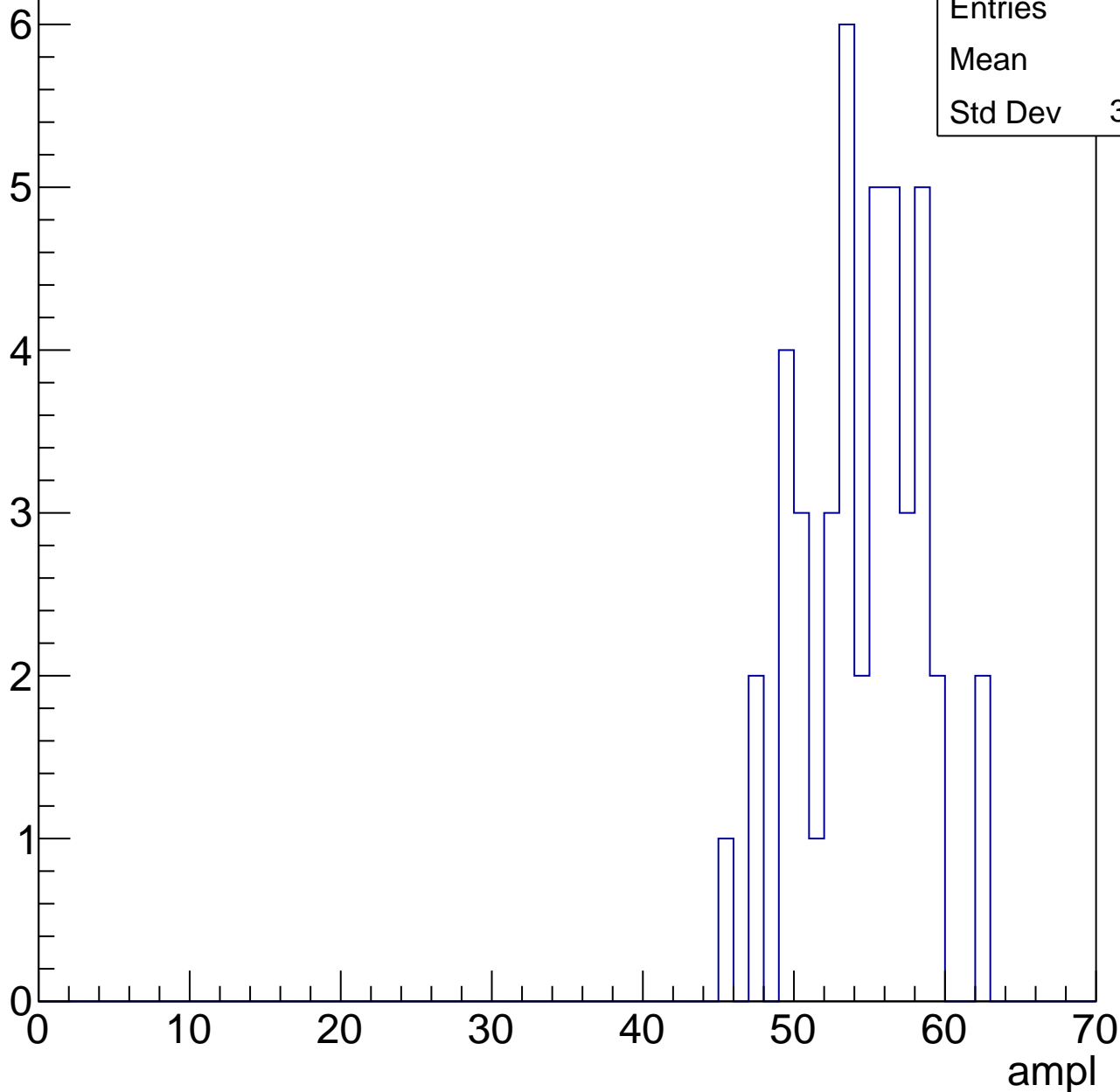


# B1L103S, U21-ch115, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	44
Mean	54
Std Dev	3.885

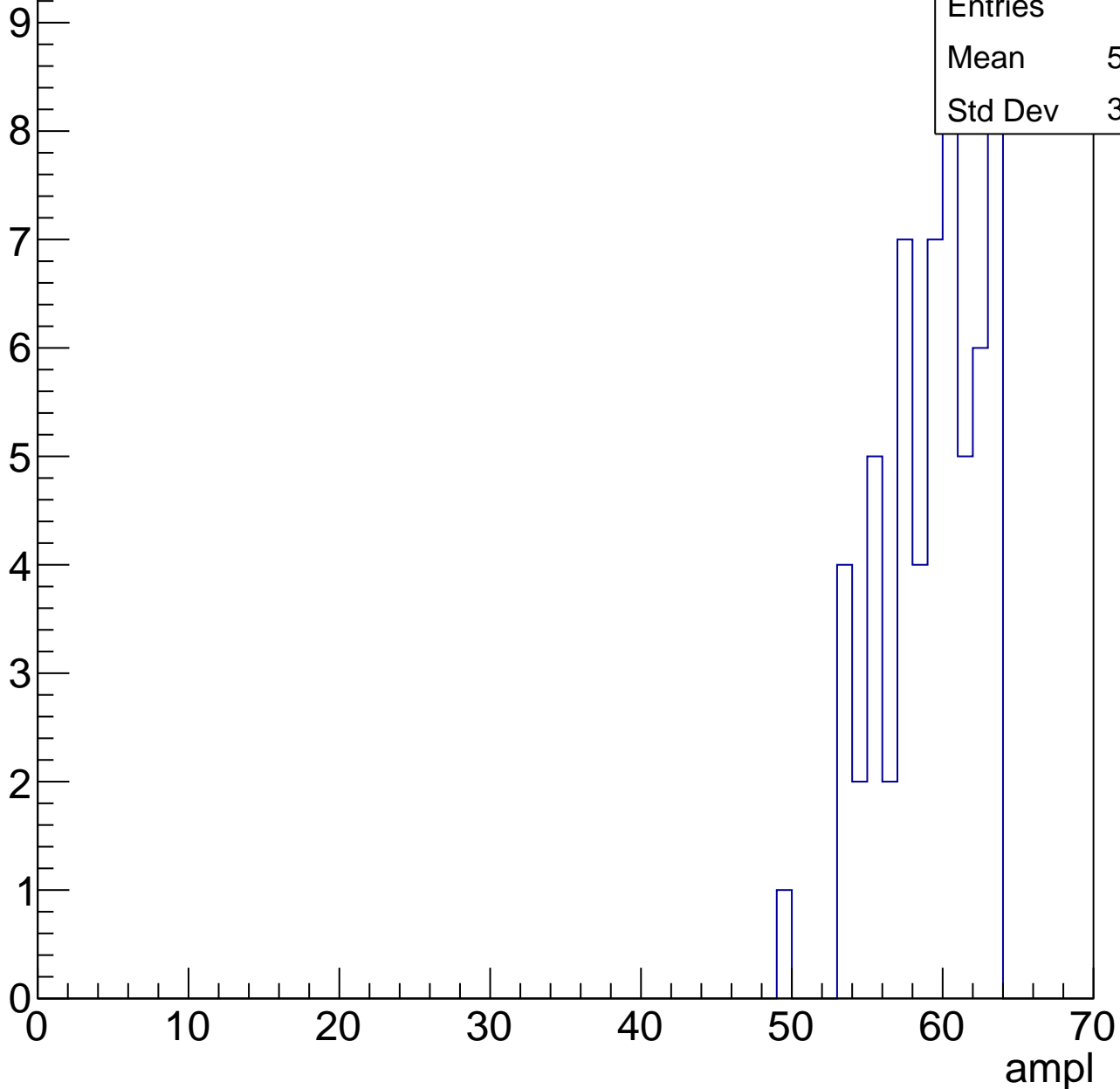


# B1L103S, U21-ch115, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	58.68
Std Dev	3.238

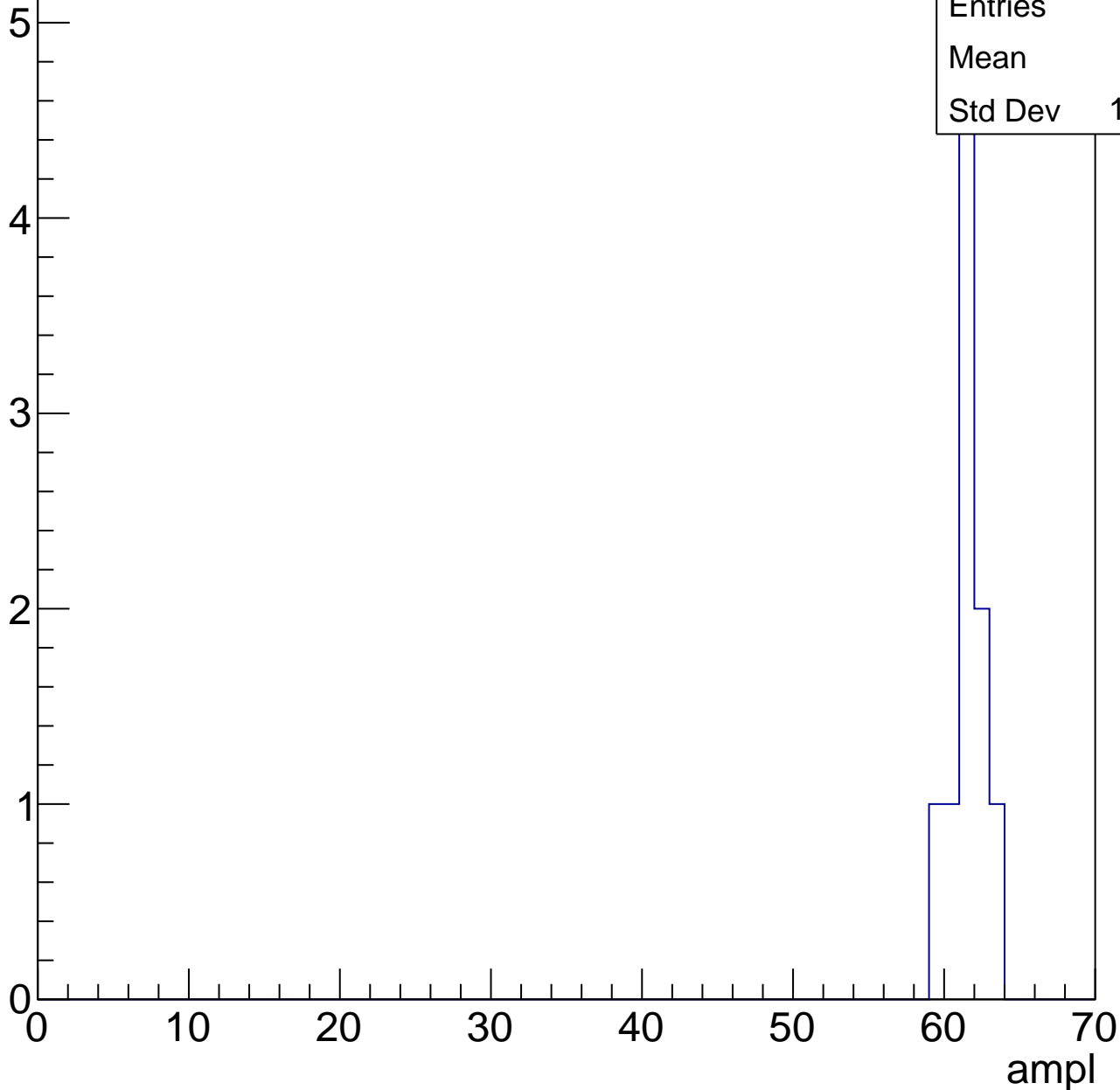


# B1L103S, U21-ch115, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	10
Mean	61.1
Std Dev	1.044

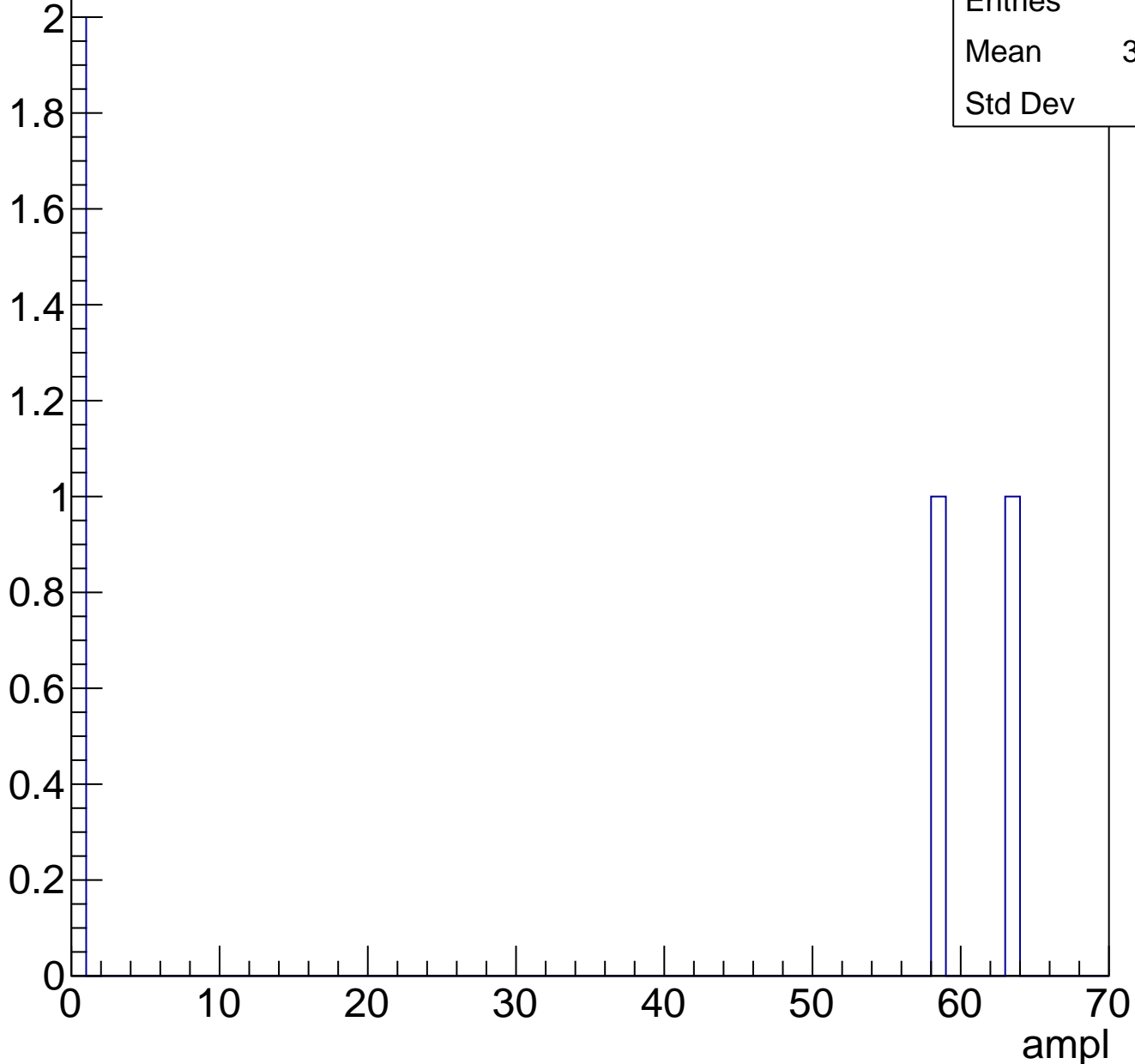




# B1L103S, U21-ch115, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	4
Mean	30.25
Std Dev	30.3

# B1L103S, U21-ch116, adc0

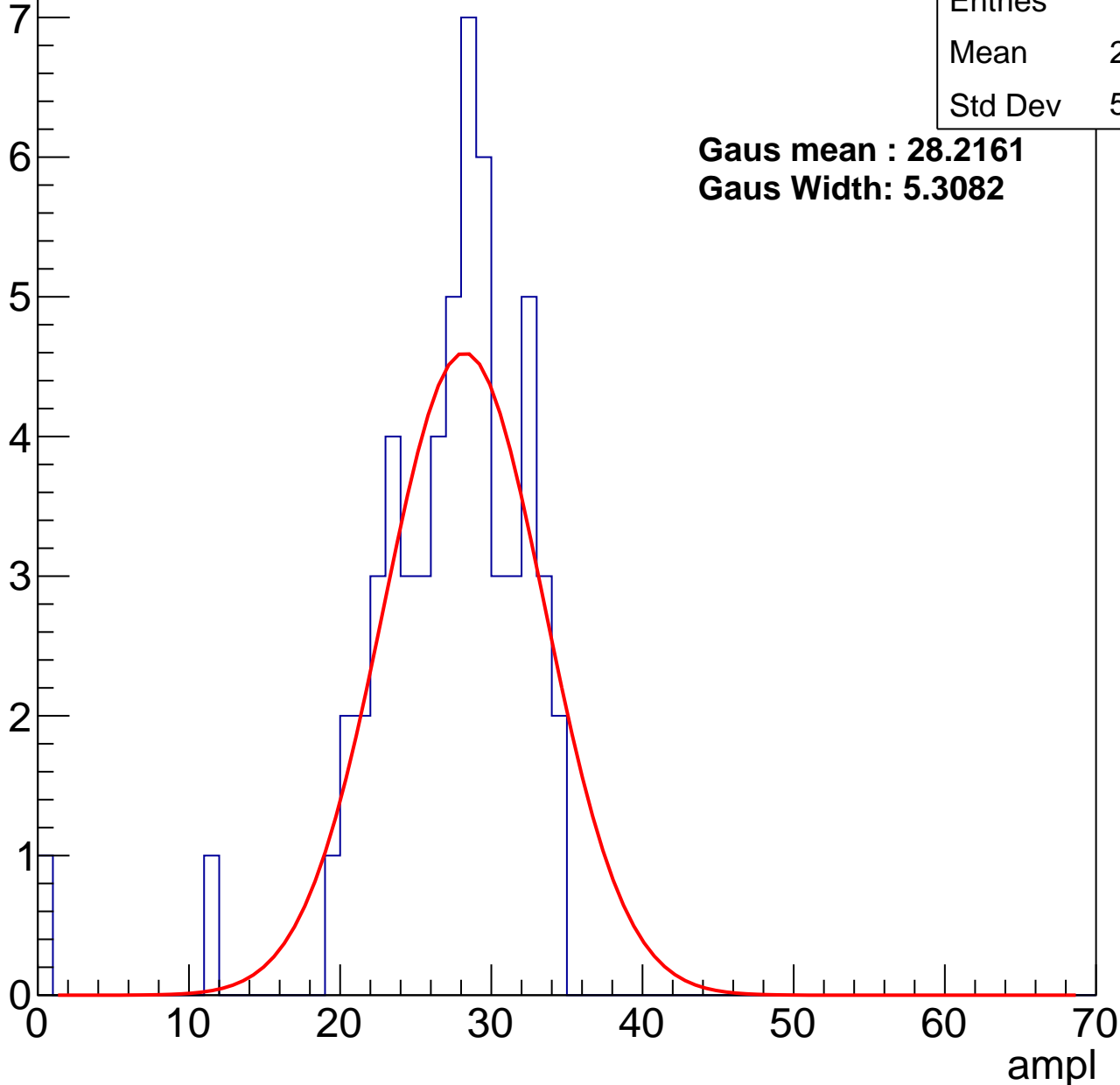
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	26.48
Std Dev	5.606

**Gaus mean : 28.2161**

**Gaus Width: 5.3082**



# B1L103S, U21-ch116, adc1

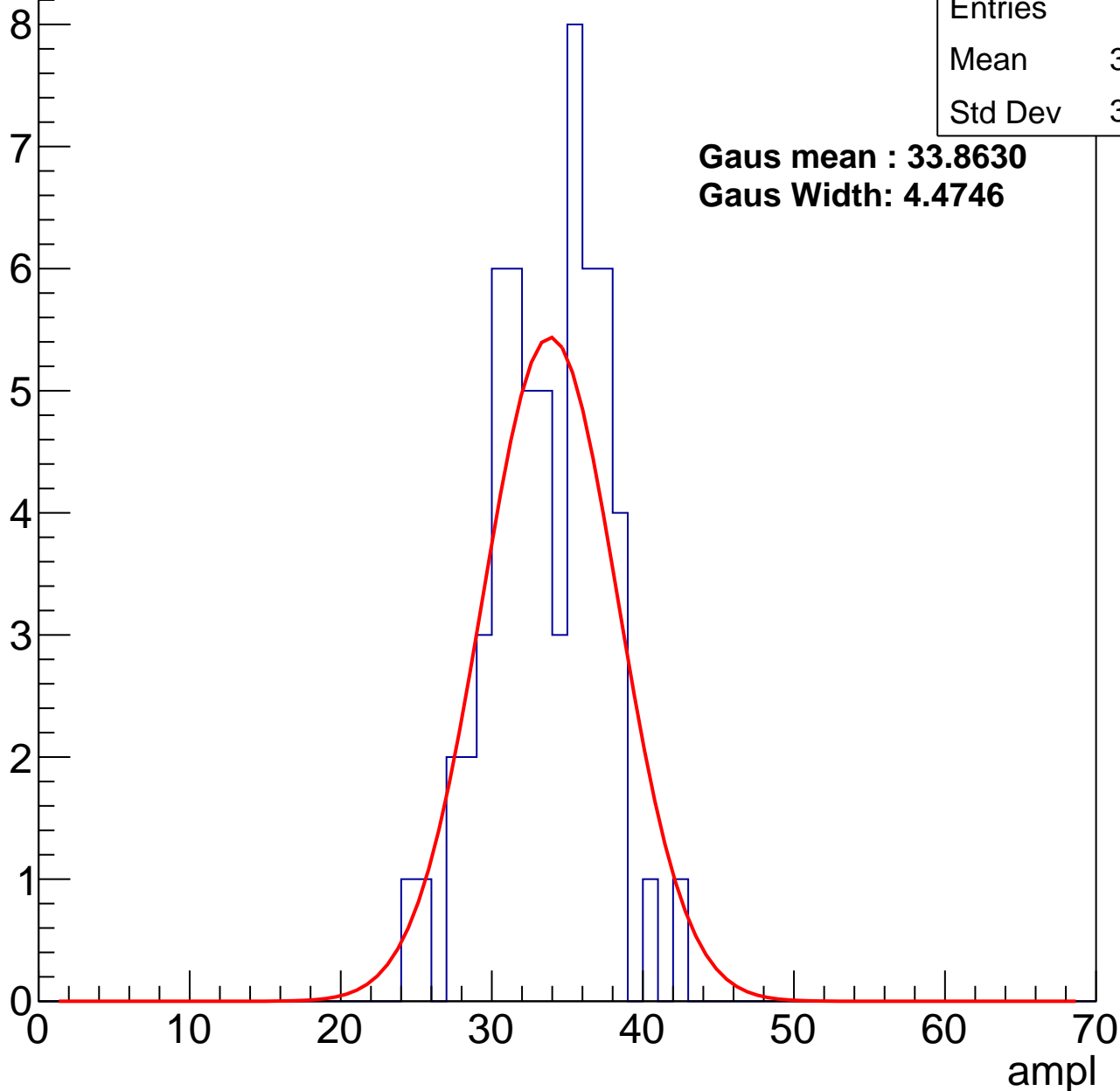
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	33.18
Std Dev	3.676

**Gaus mean : 33.8630**

**Gaus Width: 4.4746**



# B1L103S, U21-ch116, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	77
Mean	40.22
Std Dev	3.85

**Gaus mean : 40.9965**

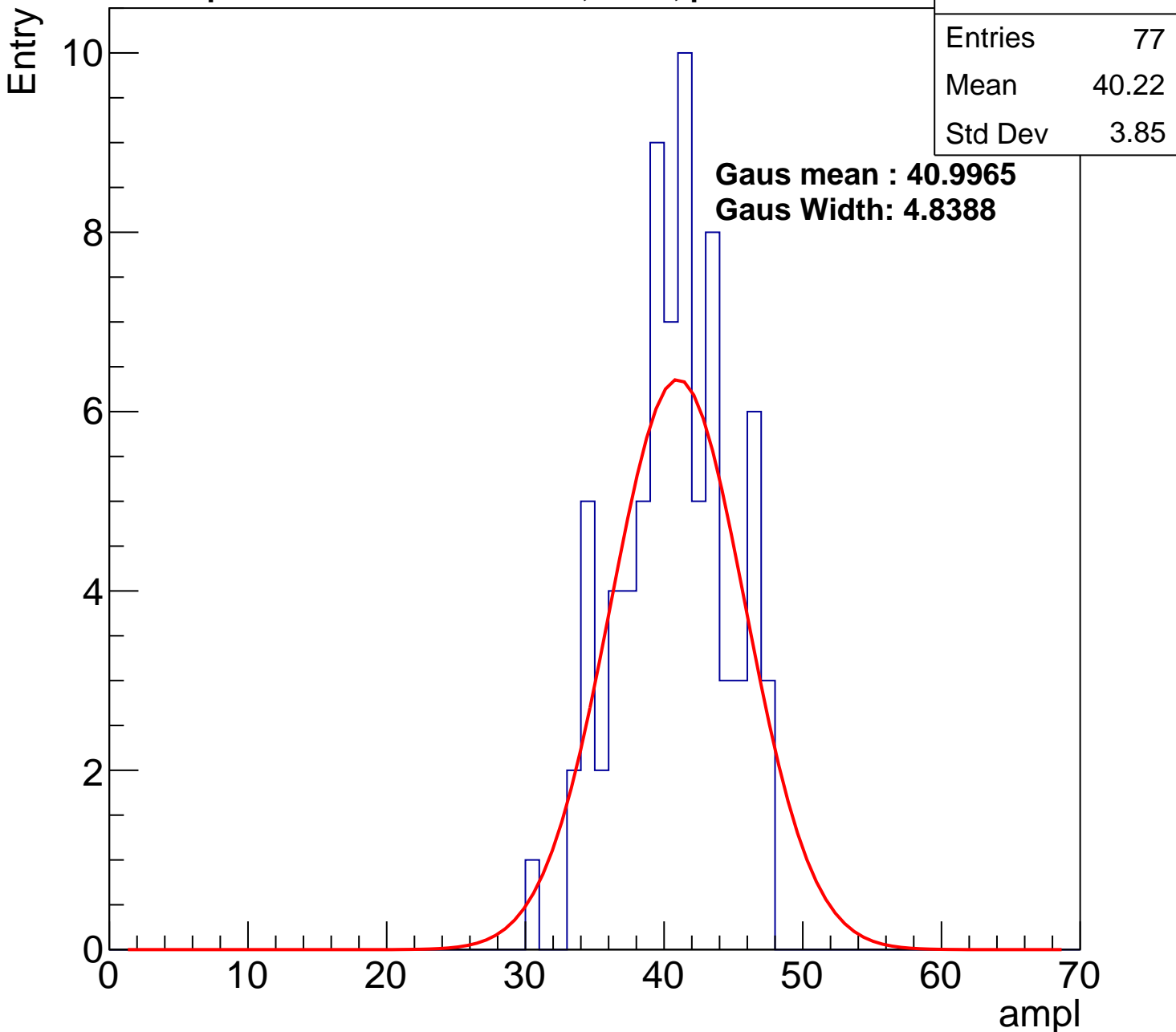
**Gaus Width: 4.8388**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

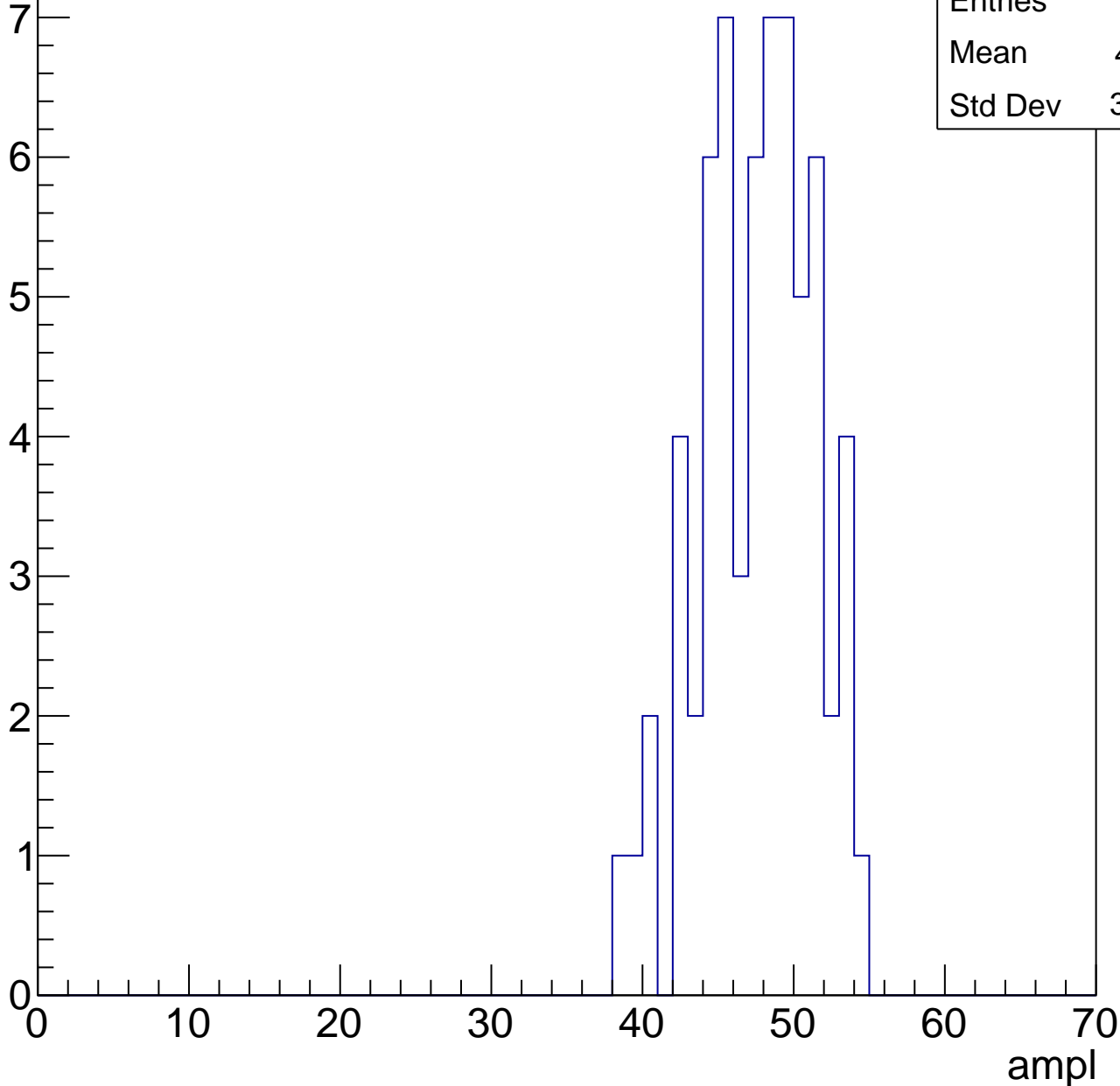


# B1L103S, U21-ch116, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	47.11
Std Dev	3.704

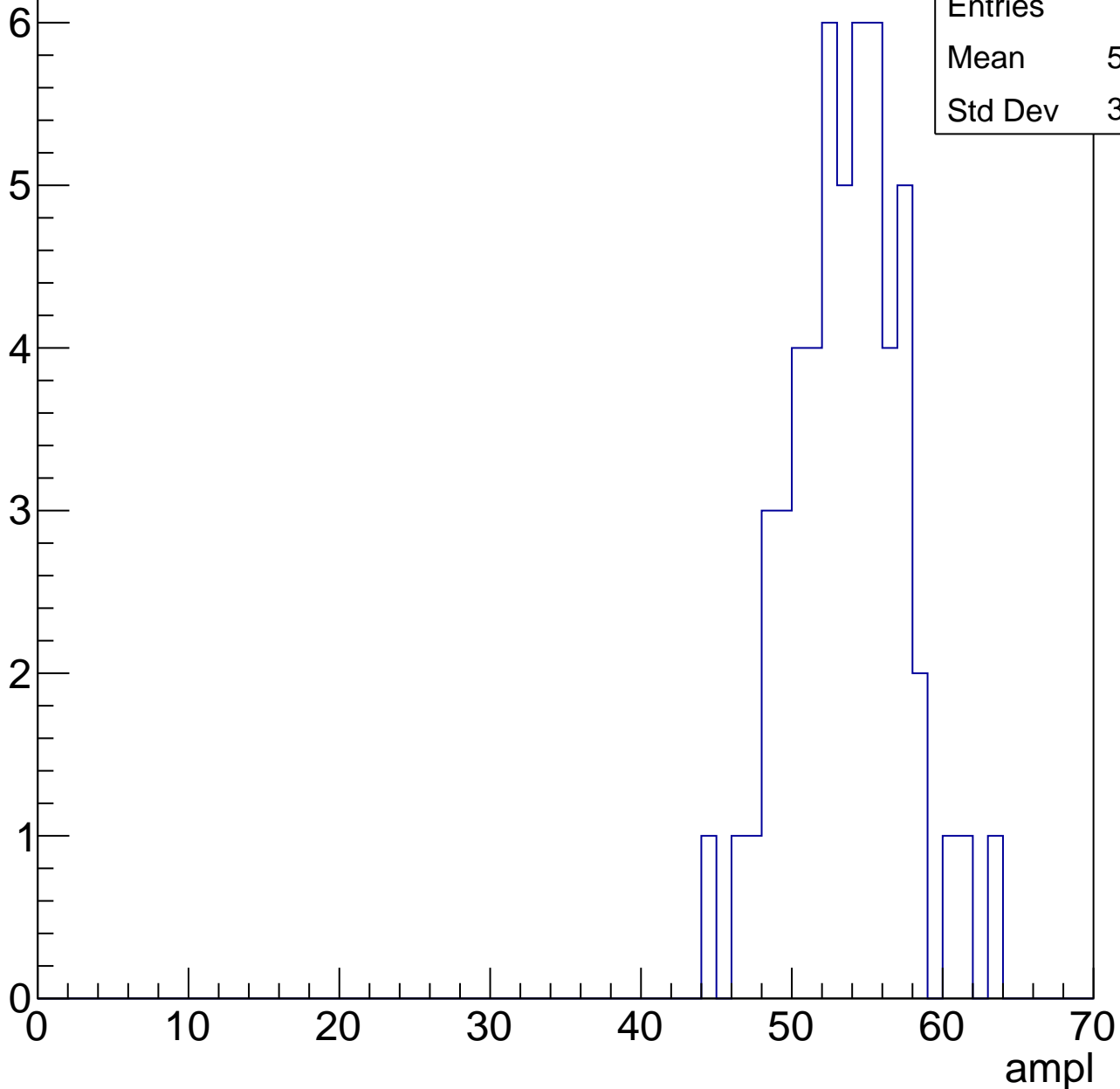


# B1L103S, U21-ch116, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

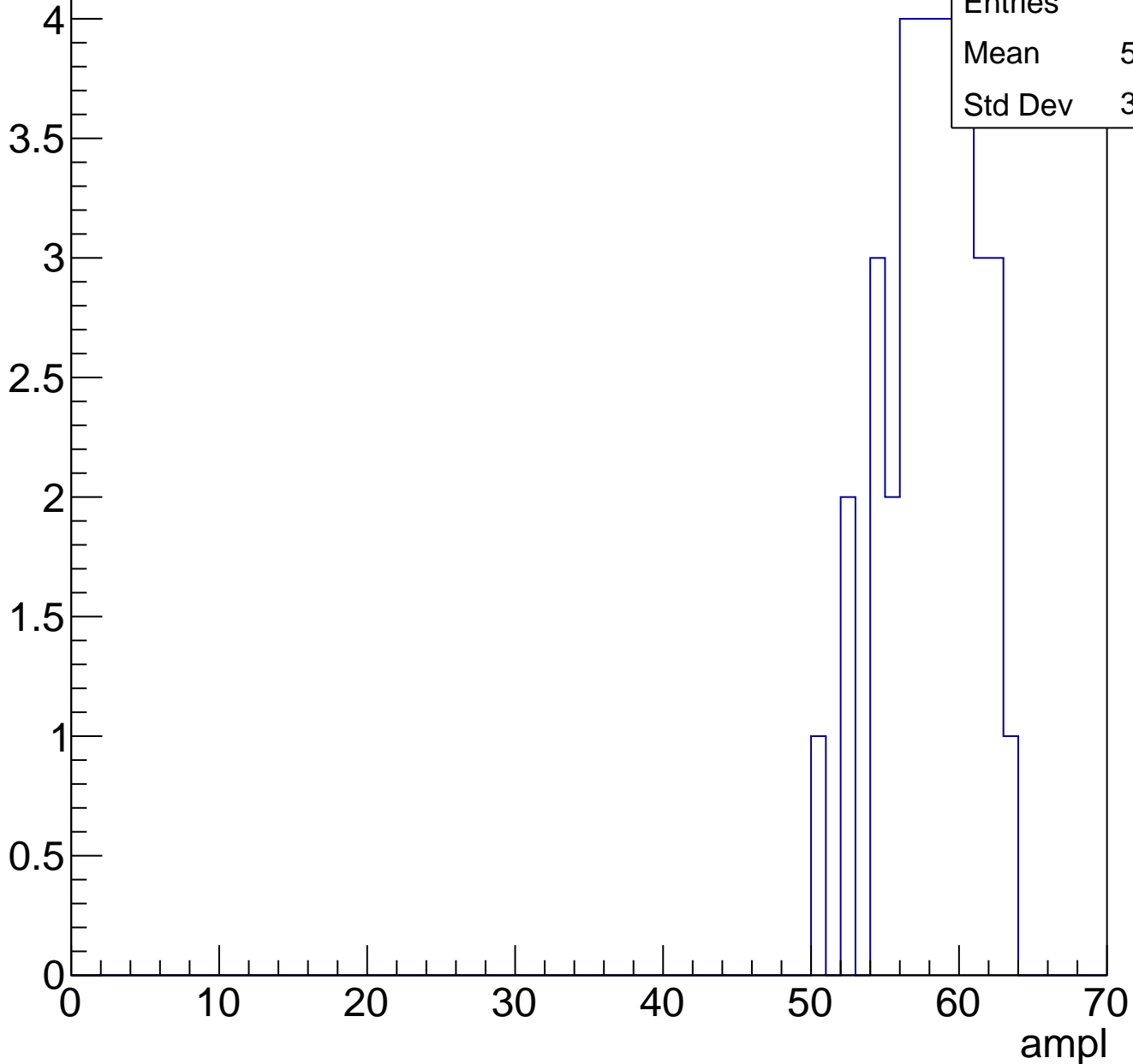
Entries	54
Mean	53.19
Std Dev	3.737



# B1L103S, U21-ch116, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

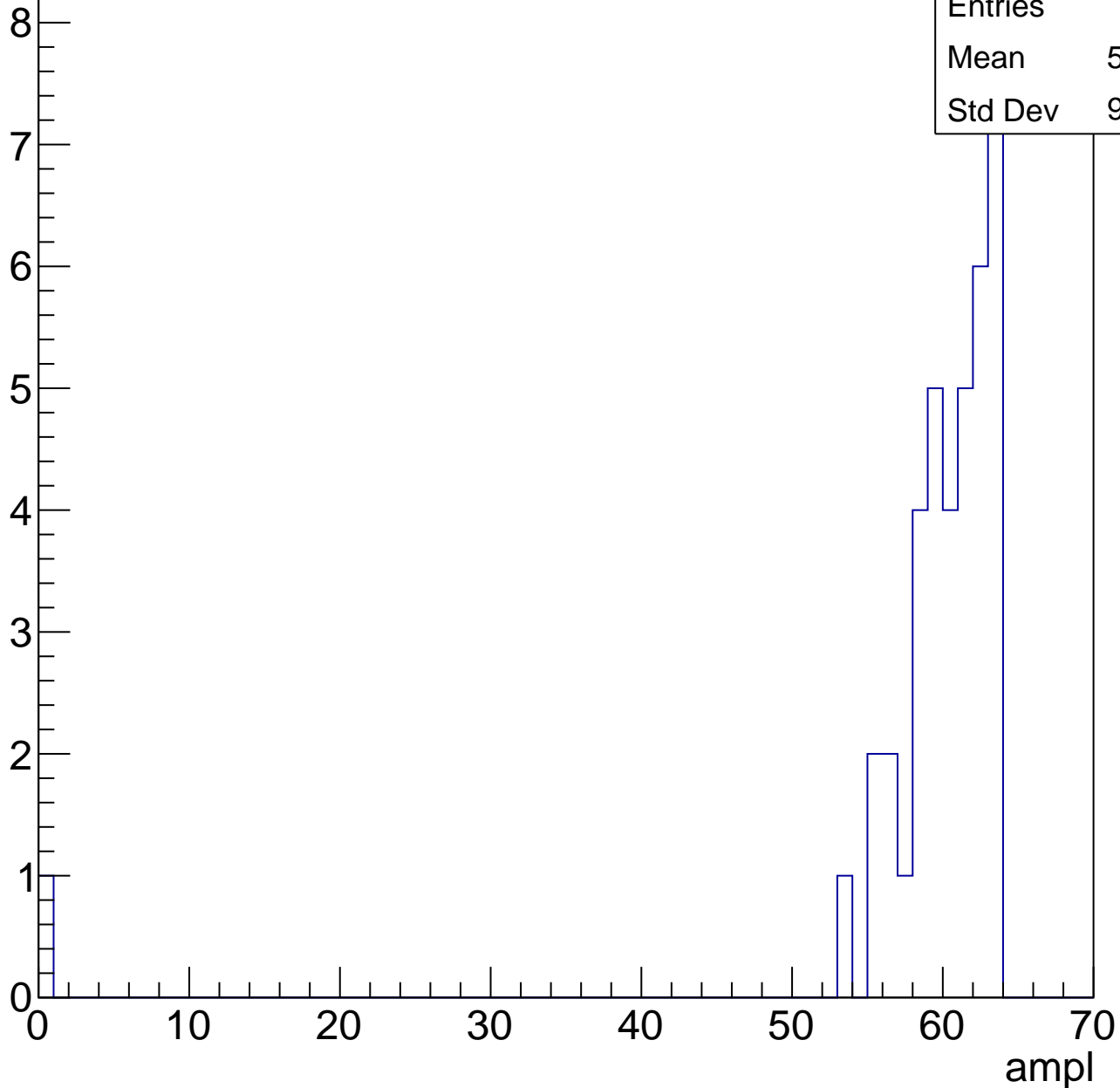


# B1L103S, U21-ch116, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	39
Mean	58.46
Std Dev	9.832

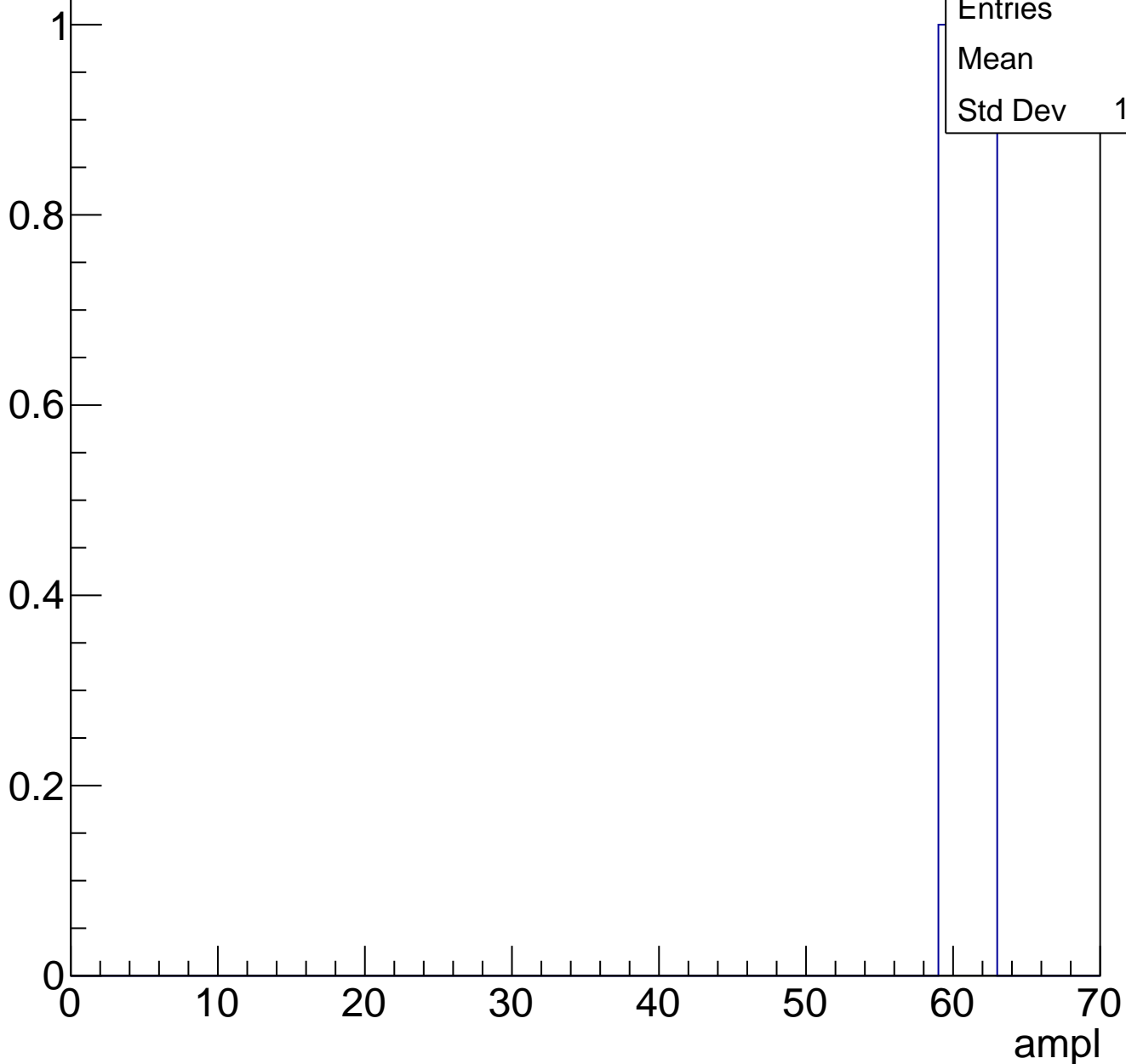




# B1L103S, U21-ch116, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



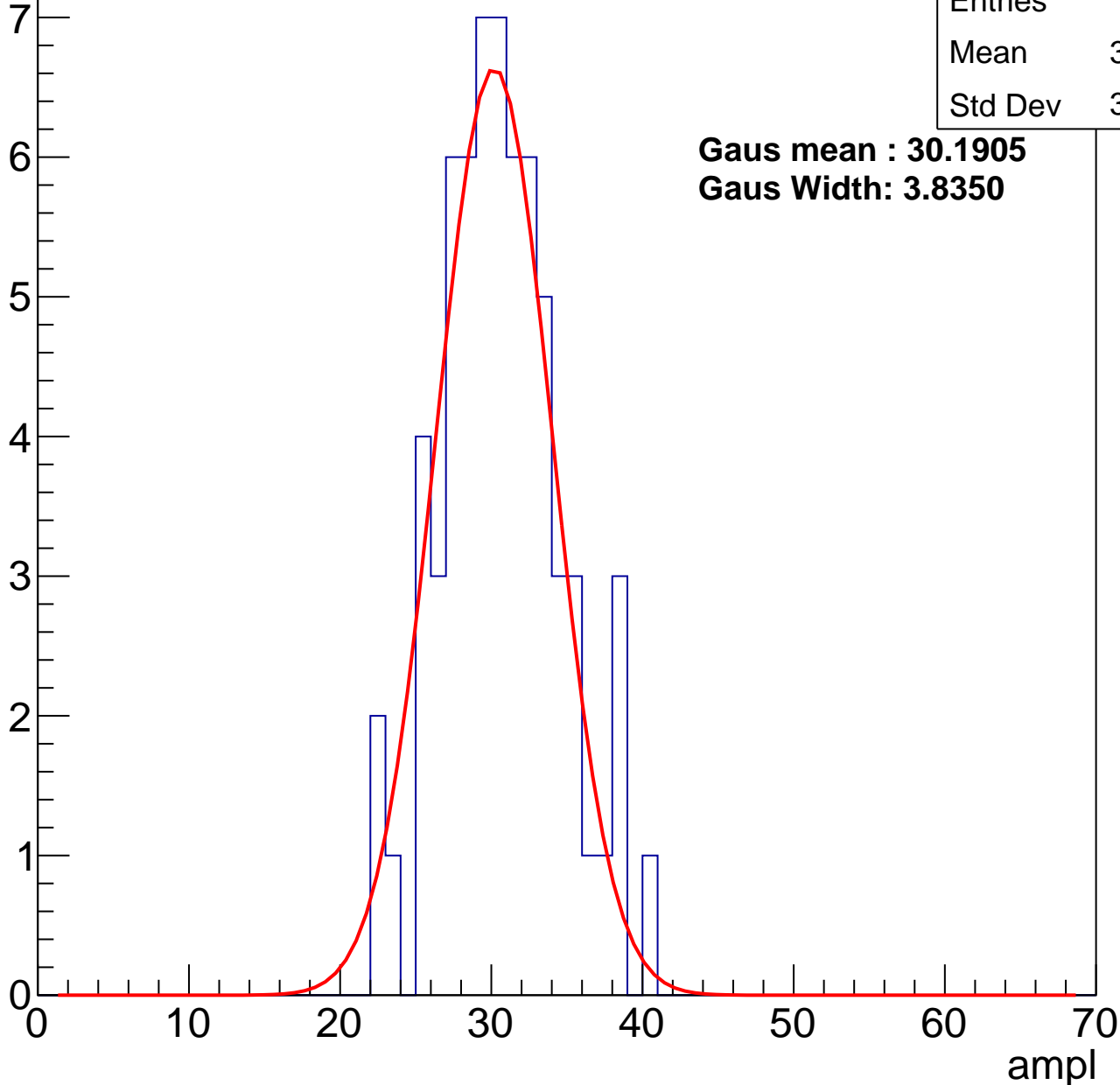
# B1L103S, U21-ch117, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	30.23
Std Dev	3.886

**Gaus mean : 30.1905**  
**Gaus Width: 3.8350**



# B1L103S, U21-ch117, adc1

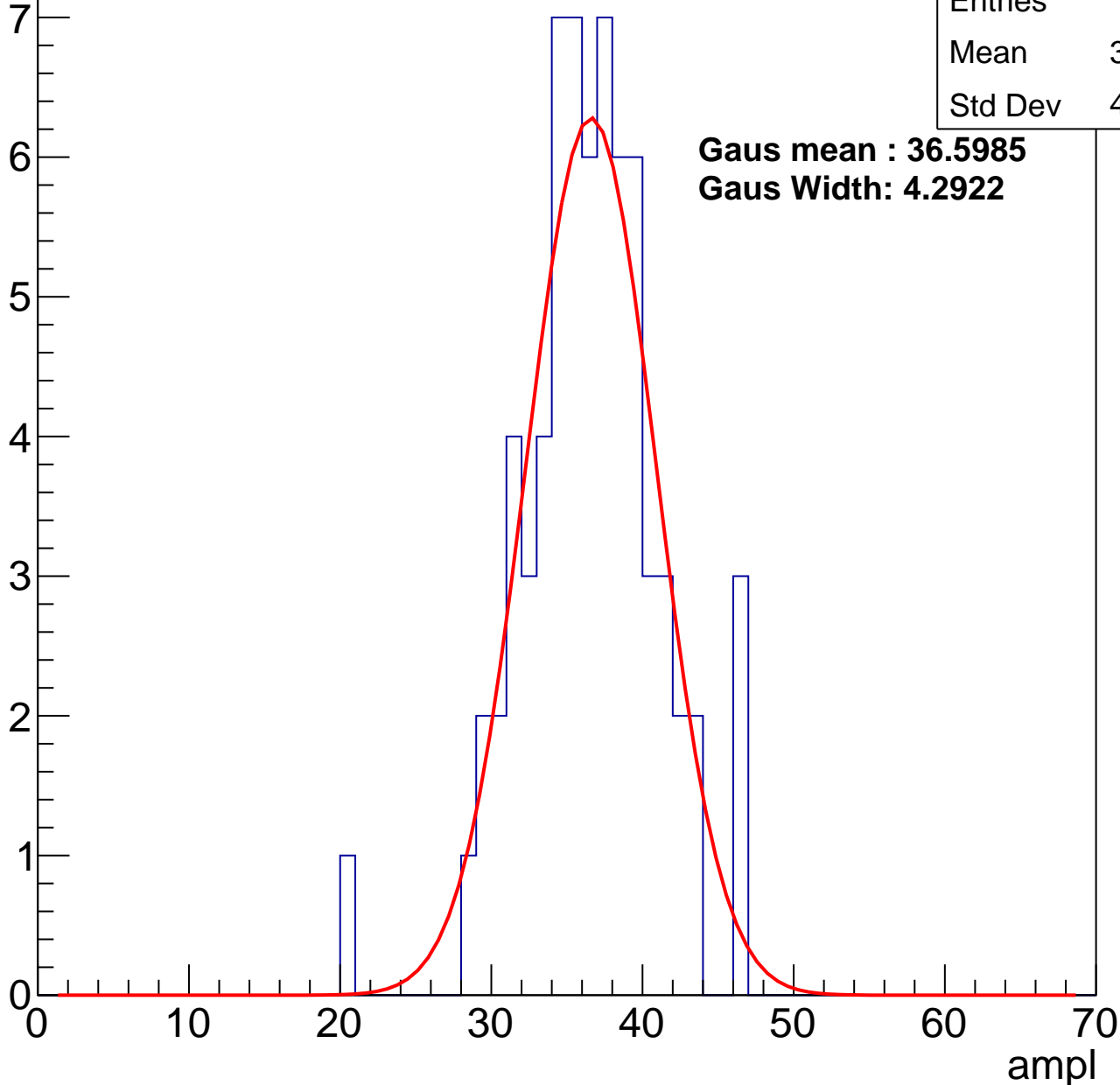
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	36.07
Std Dev	4.483

**Gaus mean : 36.5985**

**Gaus Width: 4.2922**



# B1L103S, U21-ch117, adc2

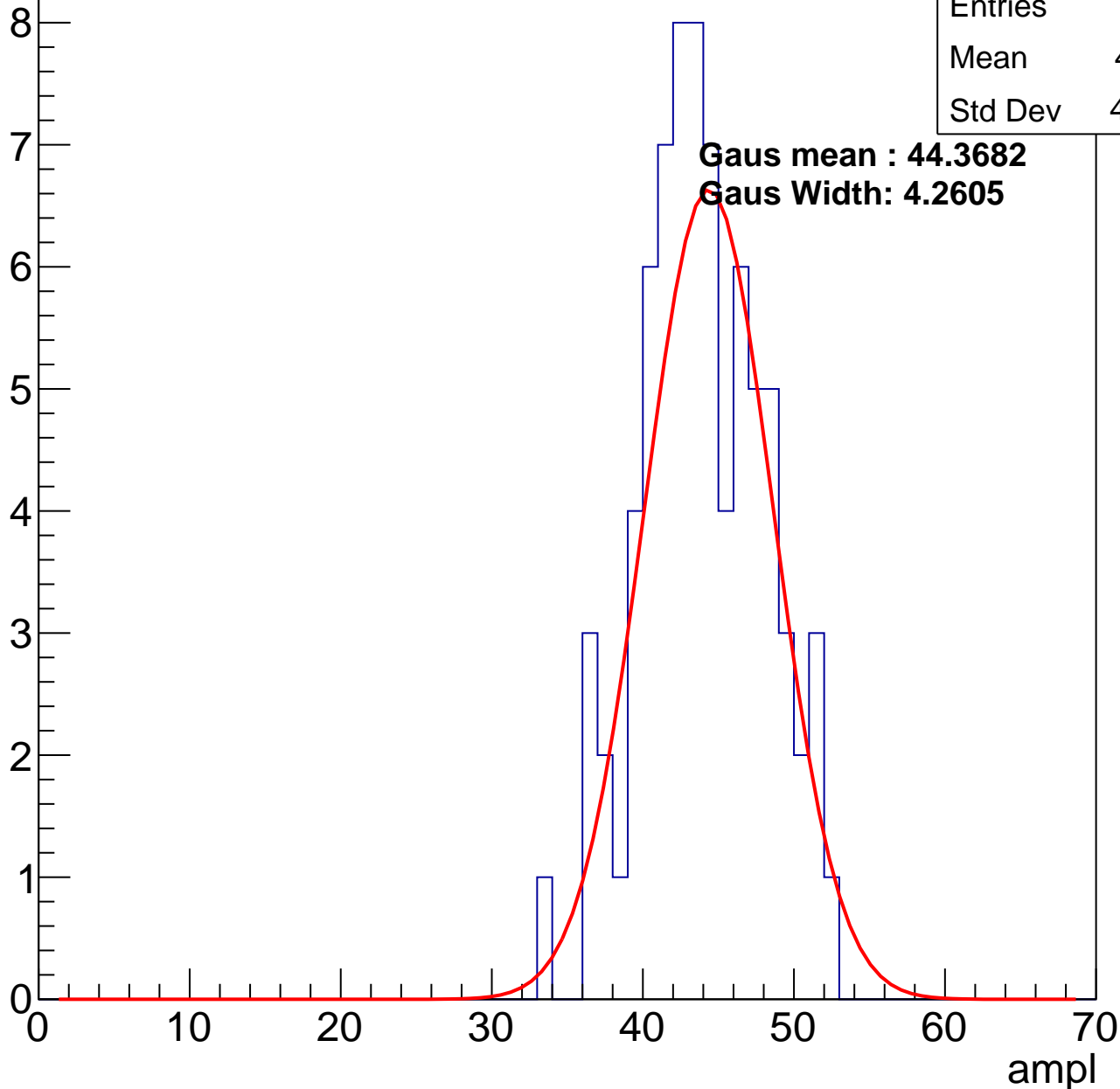
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	43.51
Std Dev	4.038

**Gaus mean : 44.3682**

**Gaus Width: 4.2605**

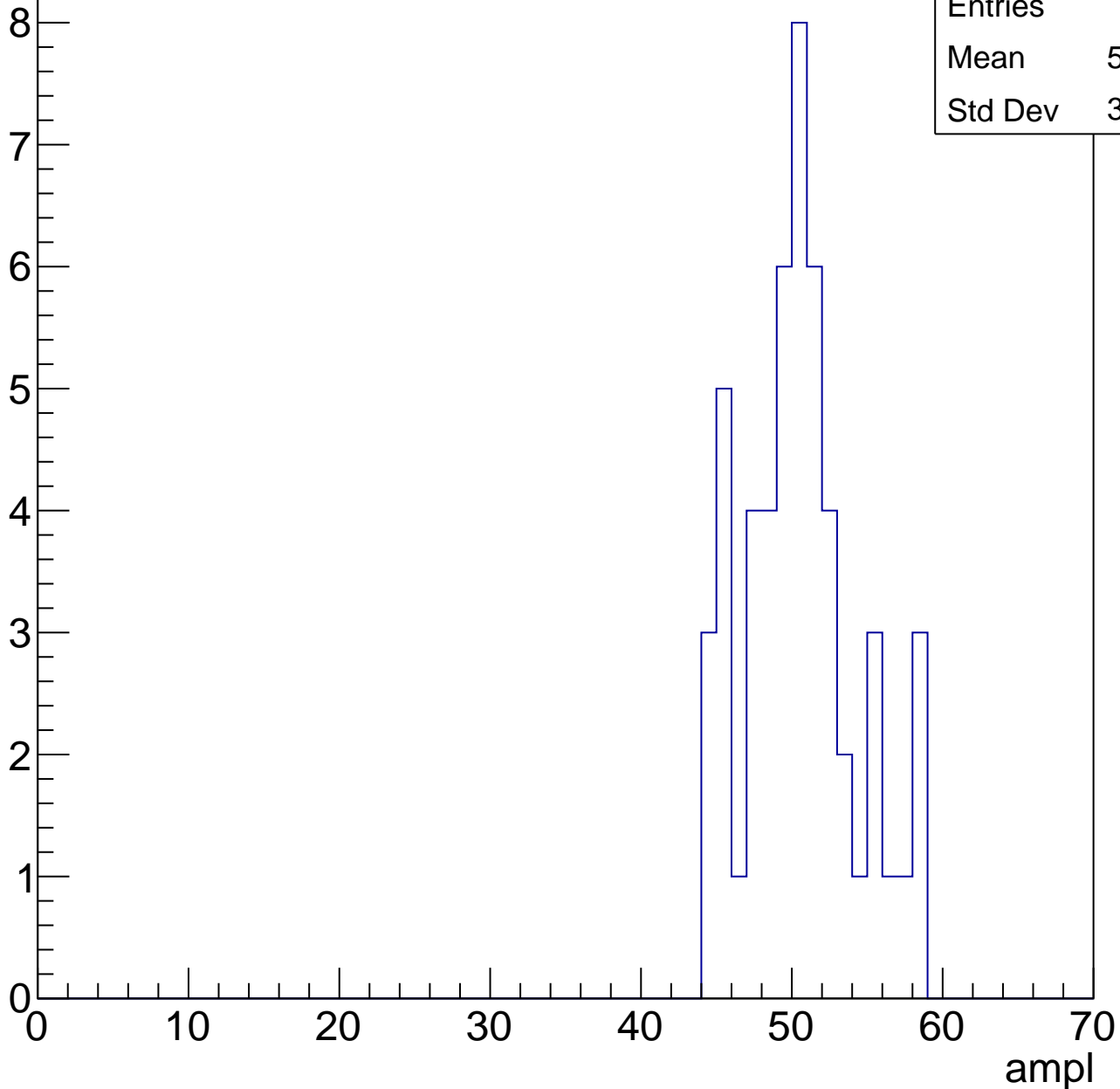


# B1L103S, U21-ch117, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	50.06
Std Dev	3.708

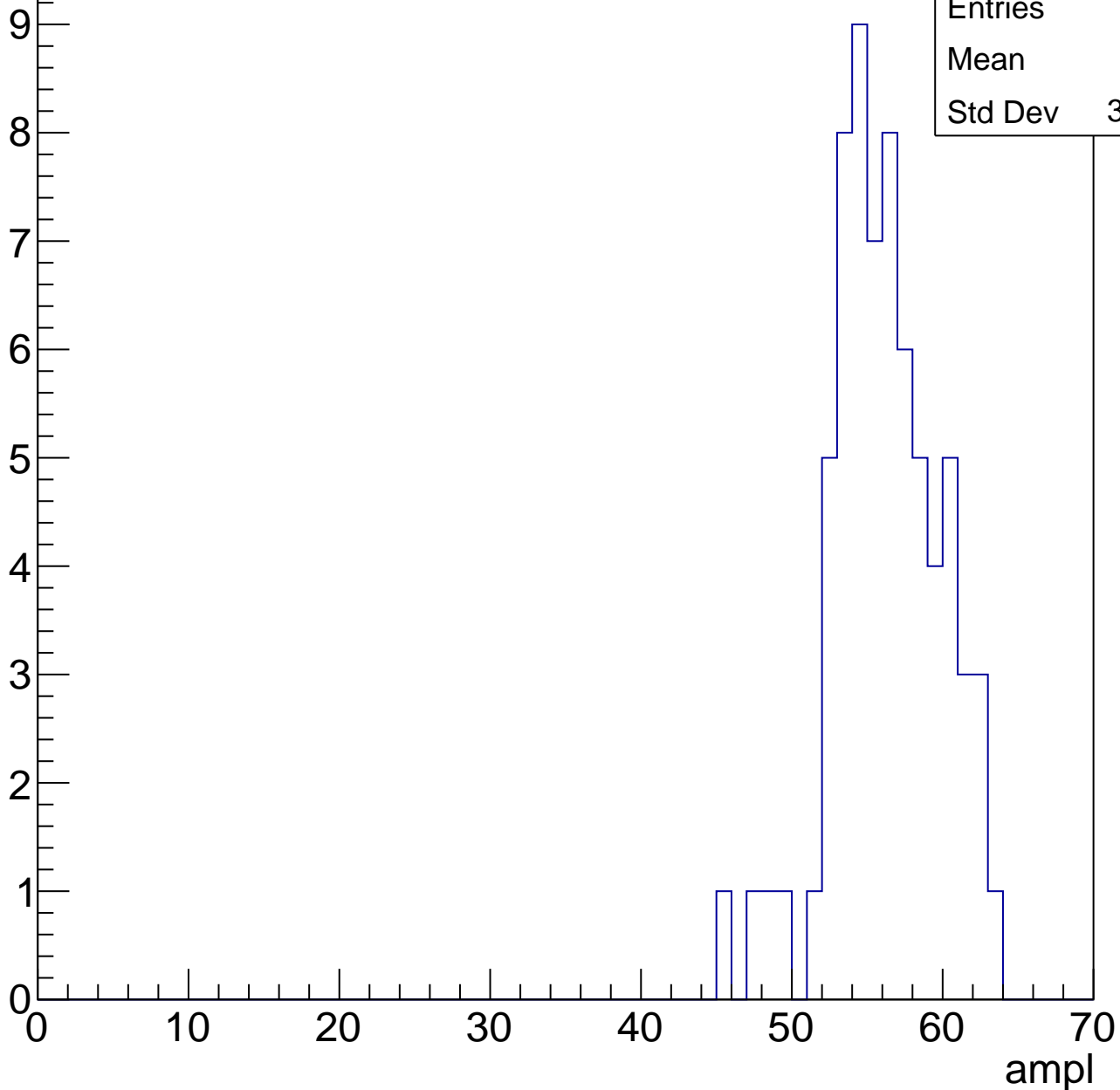


# B1L103S, U21-ch117, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	55.7
Std Dev	3.617

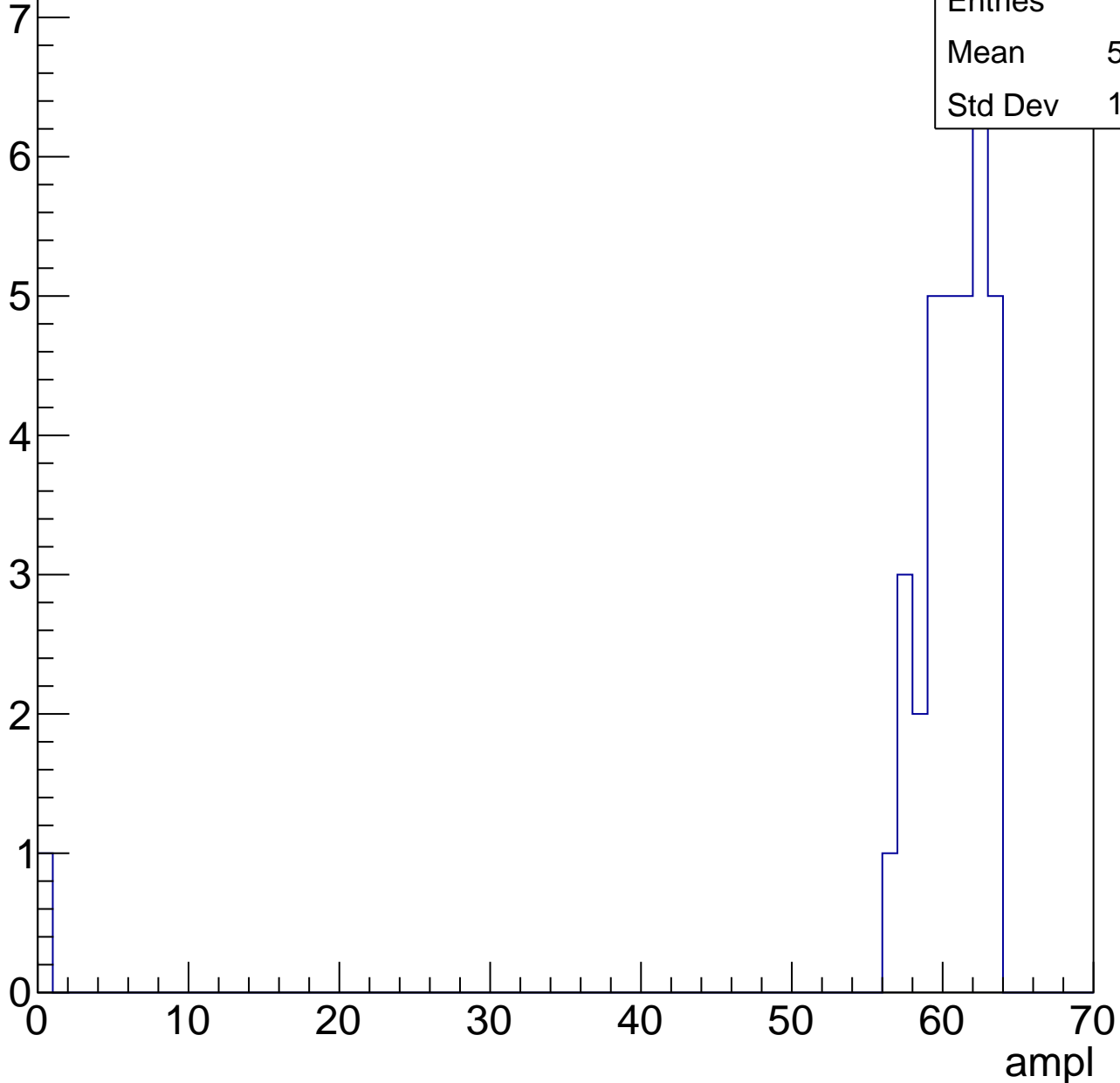


# B1L103S, U21-ch117, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

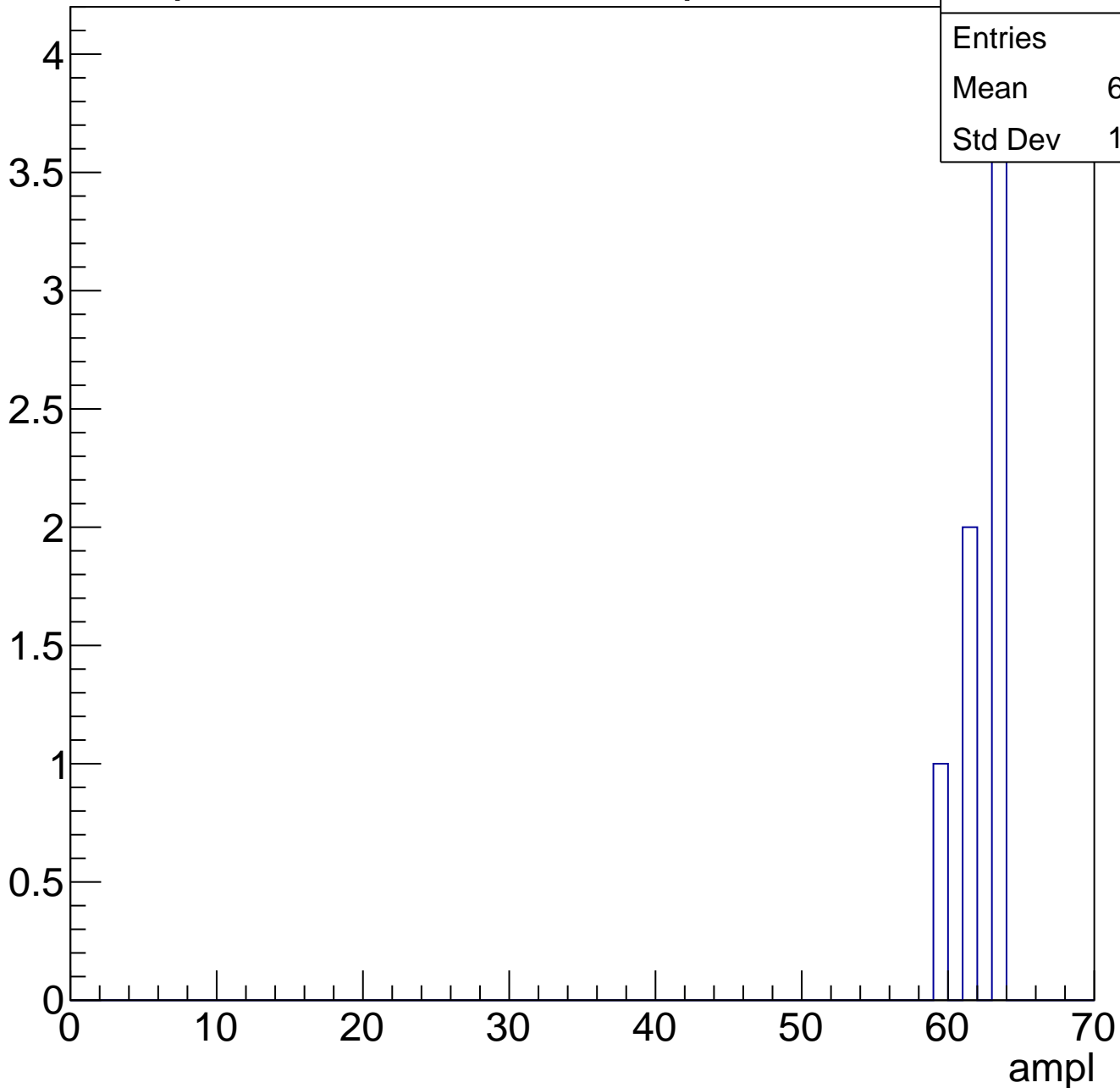
Entries	34
Mean	58.59
Std Dev	10.38



# B1L103S, U21-ch117, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

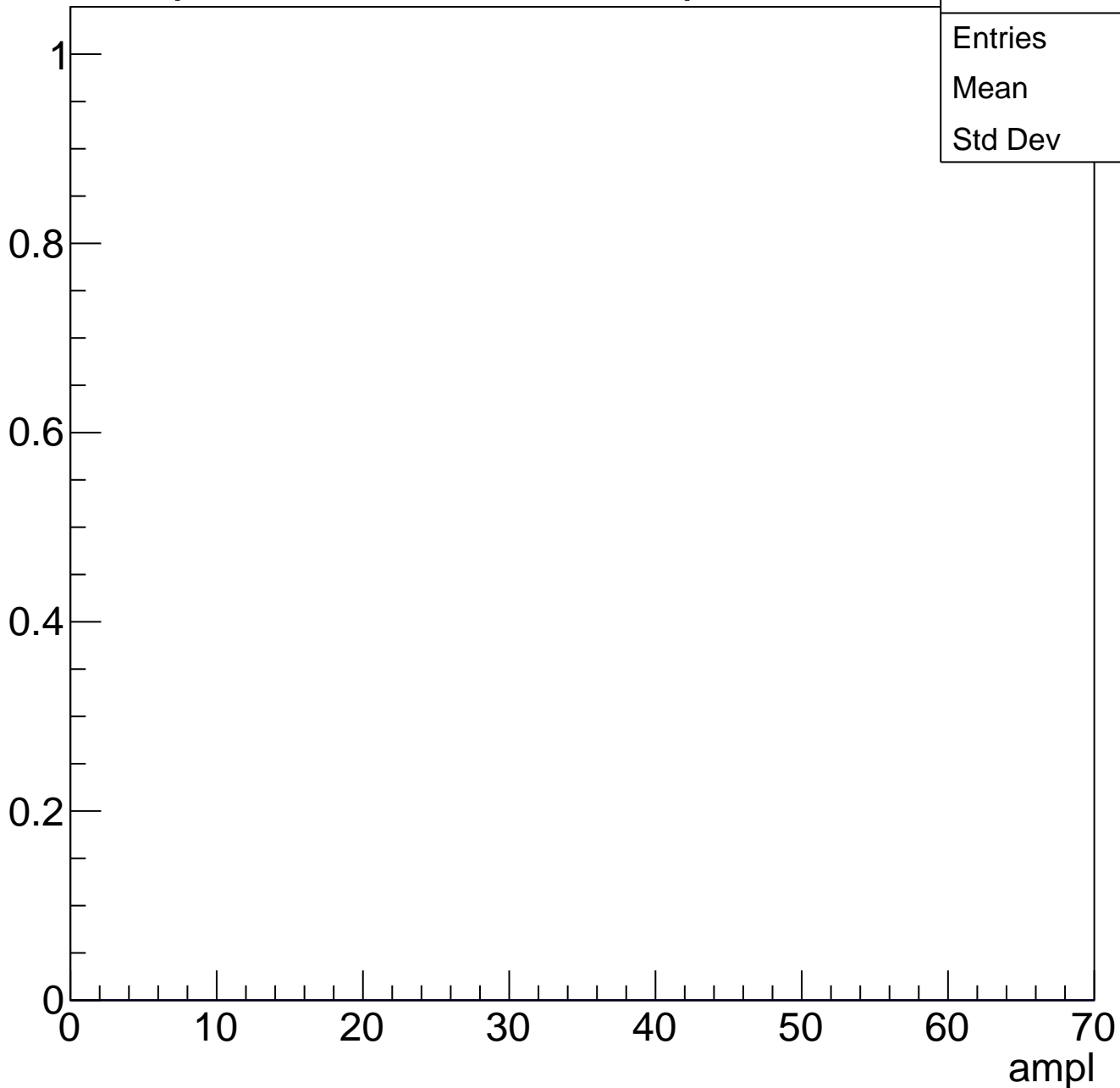




# B1L103S, U21-ch117, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U21-ch118, adc0

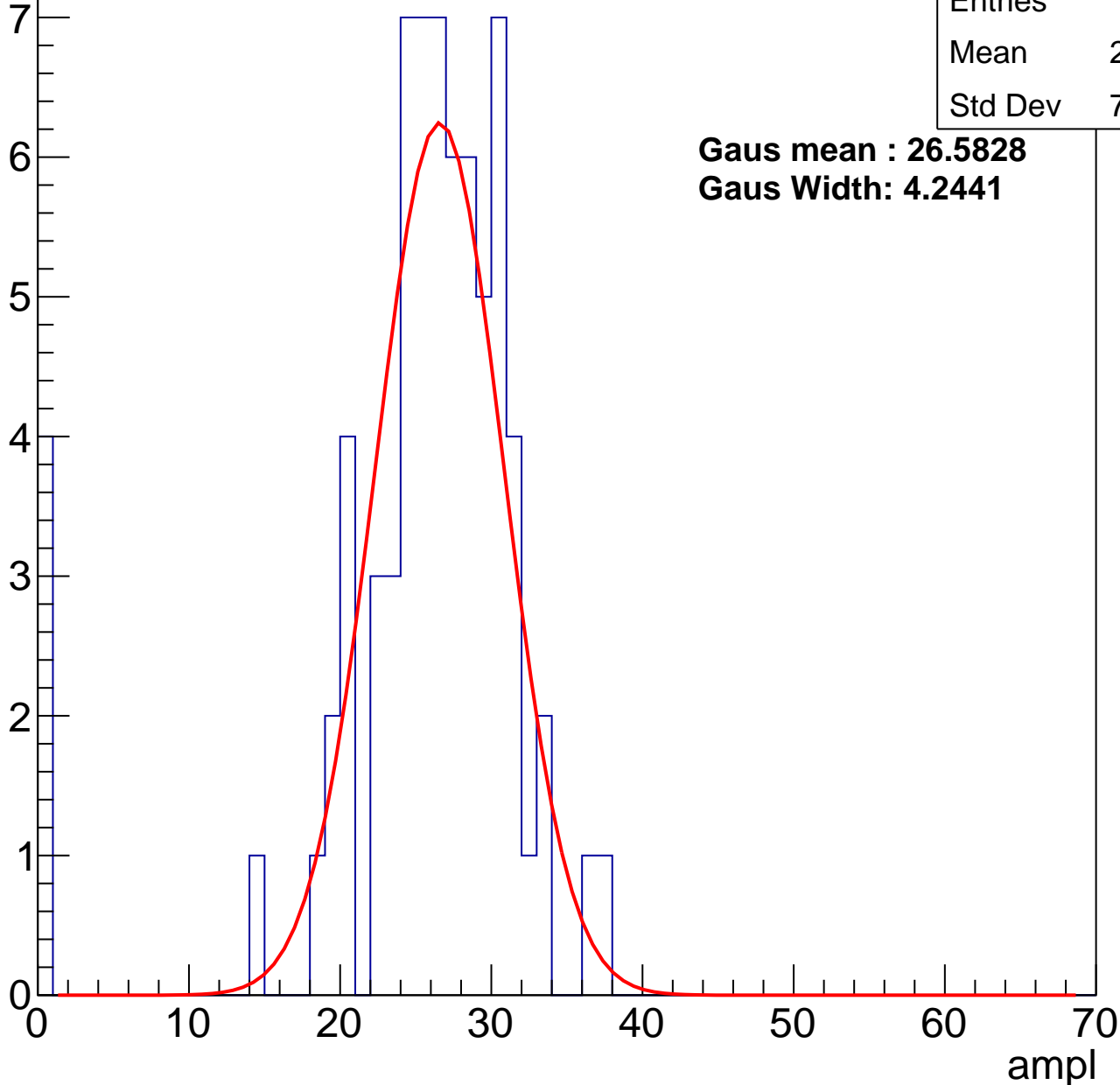
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	24.86
Std Dev	7.277

**Gaus mean : 26.5828**

**Gaus Width: 4.2441**



# B1L103S, U21-ch118, adc1

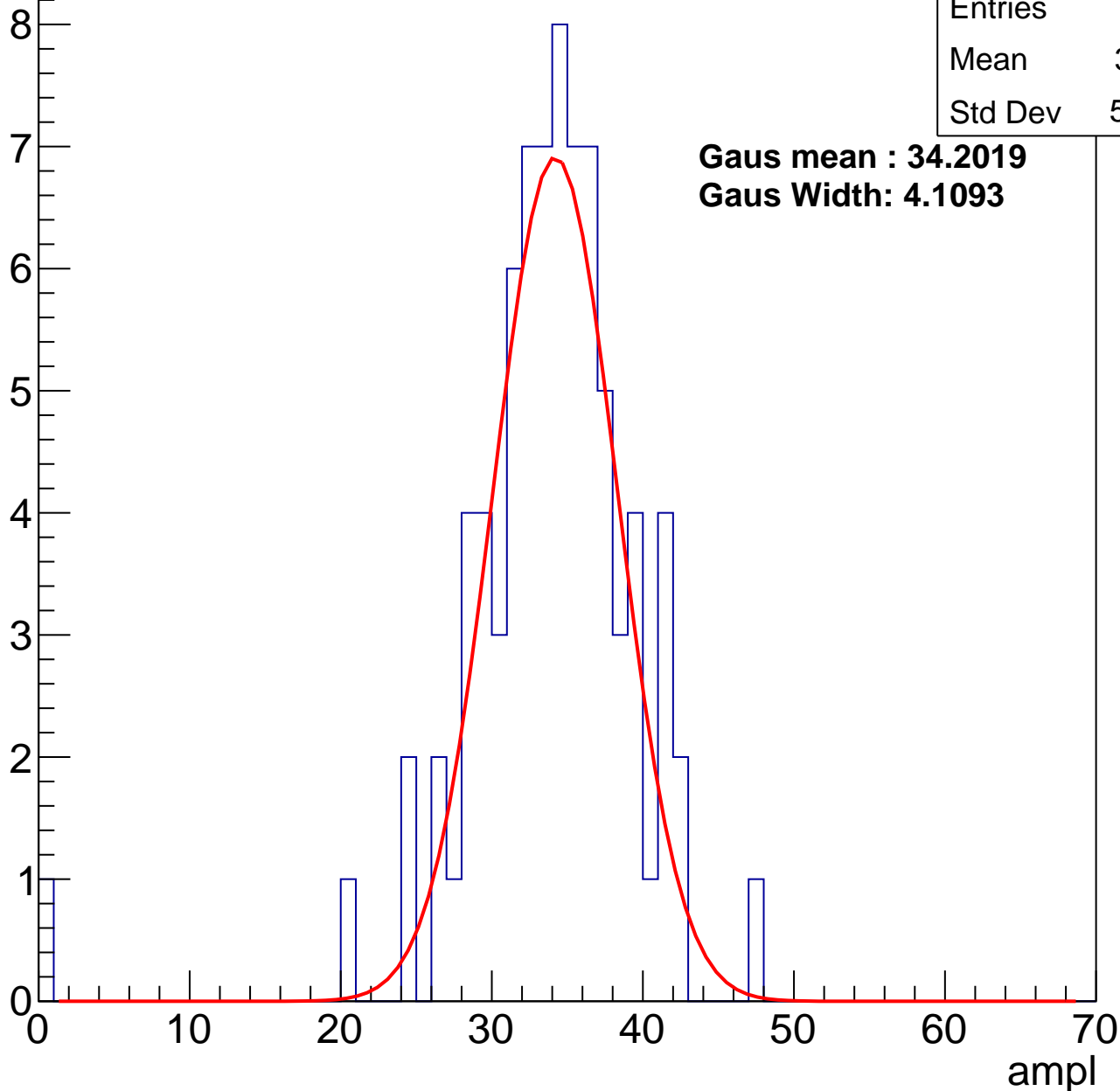
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	80
Mean	33.31
Std Dev	5.947

**Gaus mean : 34.2019**

**Gaus Width: 4.1093**



# B1L103S, U21-ch118, adc2

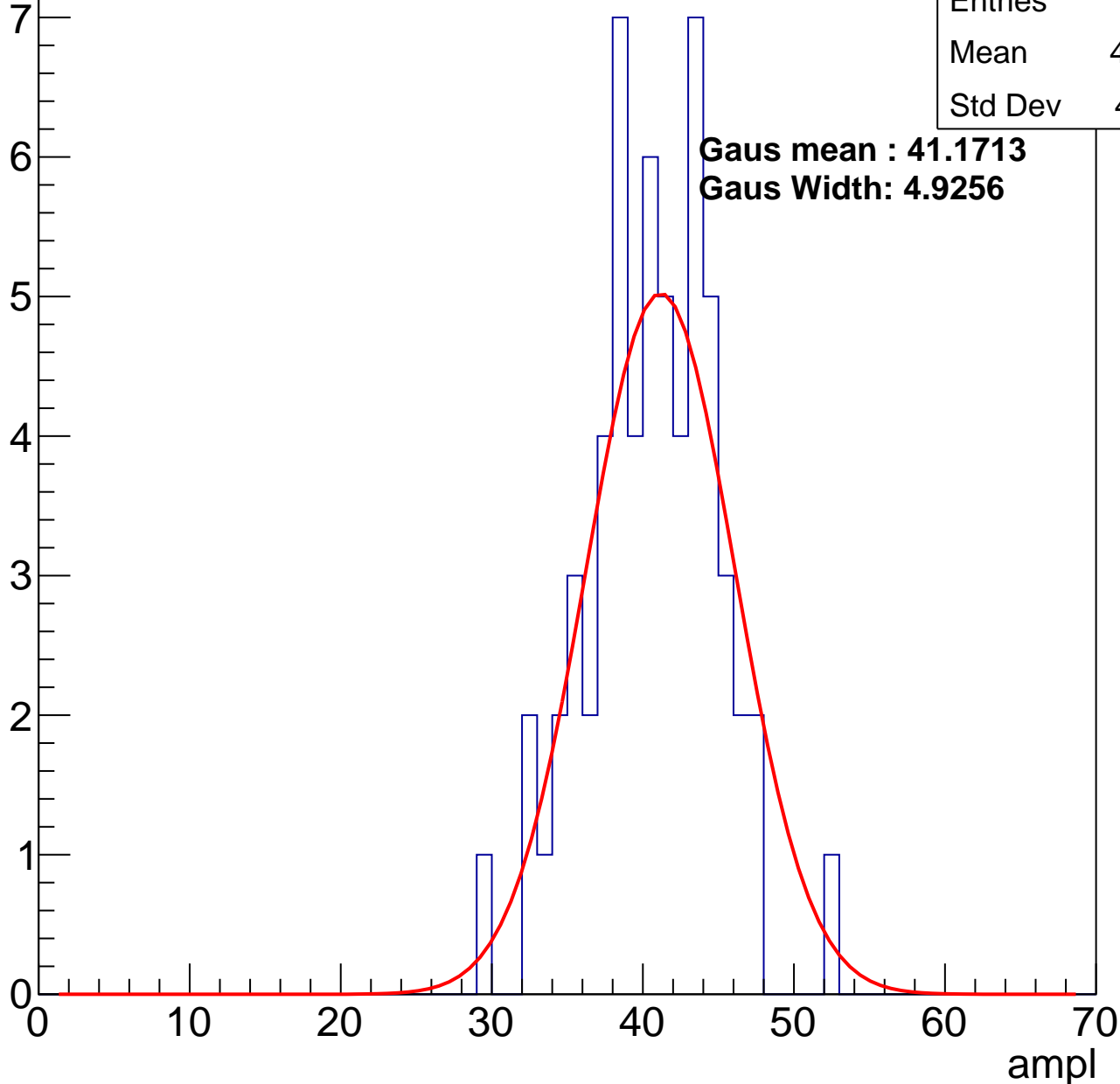
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	40.13
Std Dev	4.241

**Gaus mean : 41.1713**

**Gaus Width: 4.9256**

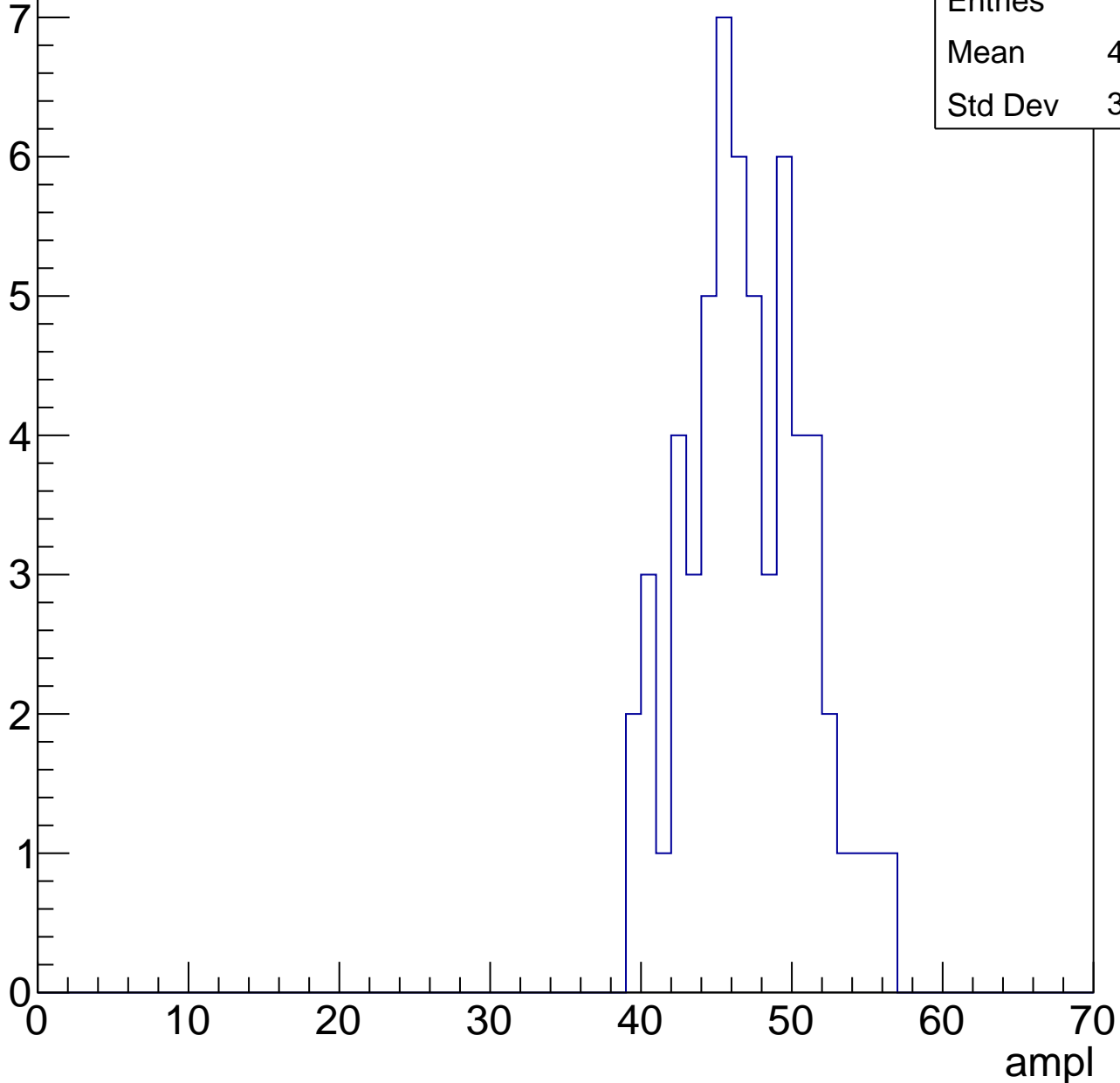


# B1L103S, U21-ch118, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	46.54
Std Dev	3.976

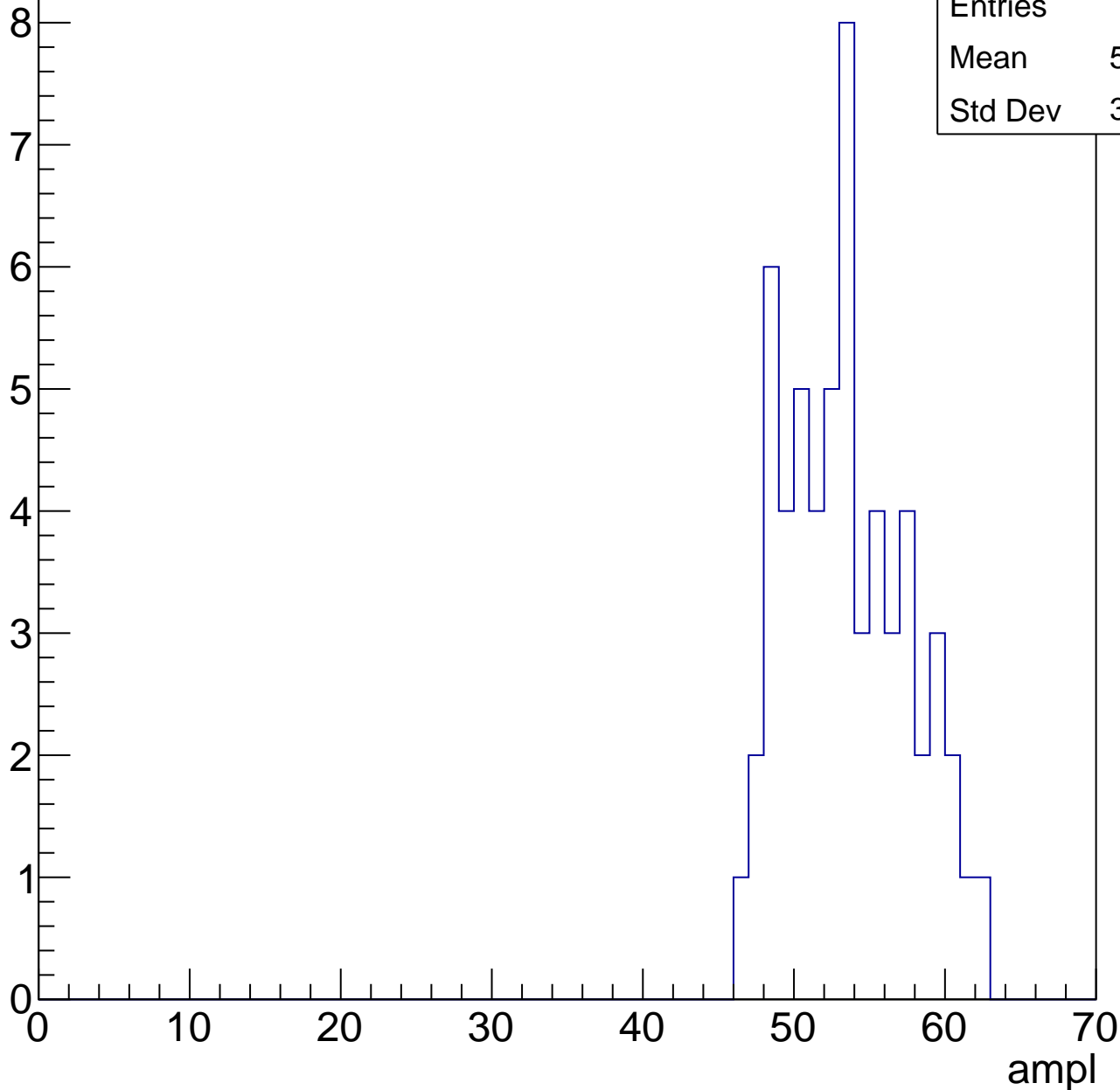


# B1L103S, U21-ch118, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	53.03
Std Dev	3.965

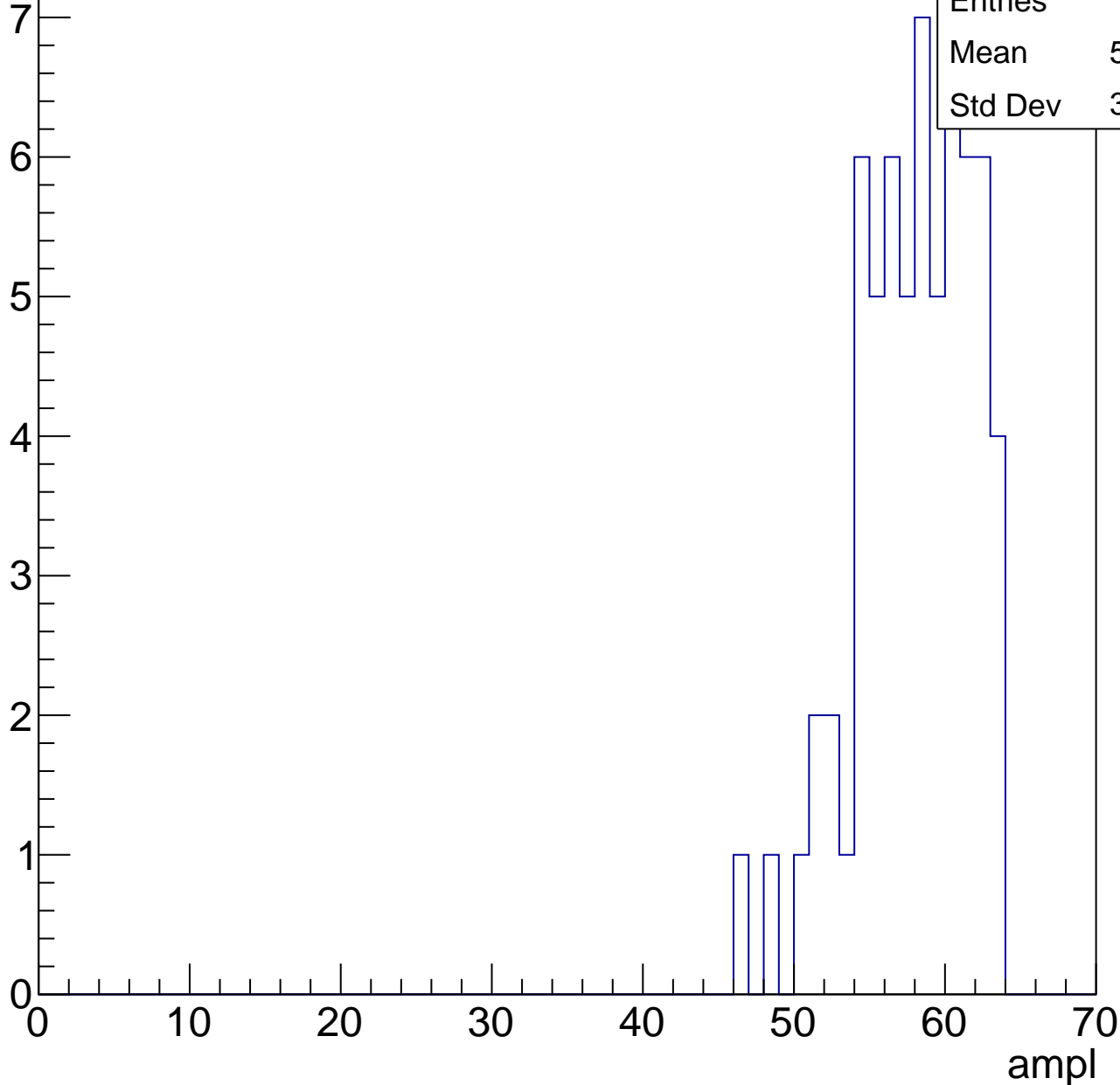


# B1L103S, U21-ch118, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	57.45
Std Dev	3.795

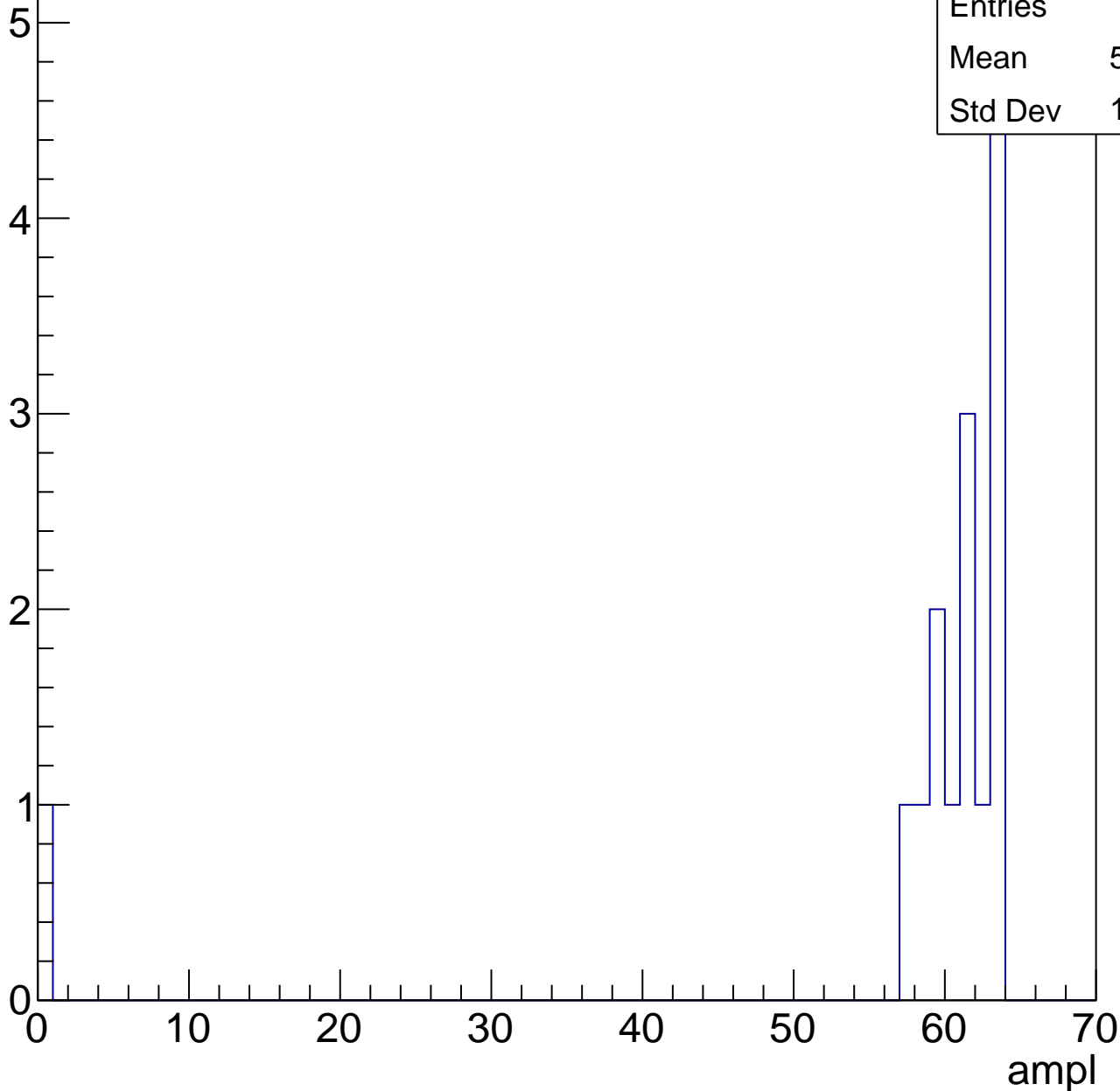


# B1L103S, U21-ch118, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	15
Mean	56.87
Std Dev	15.32

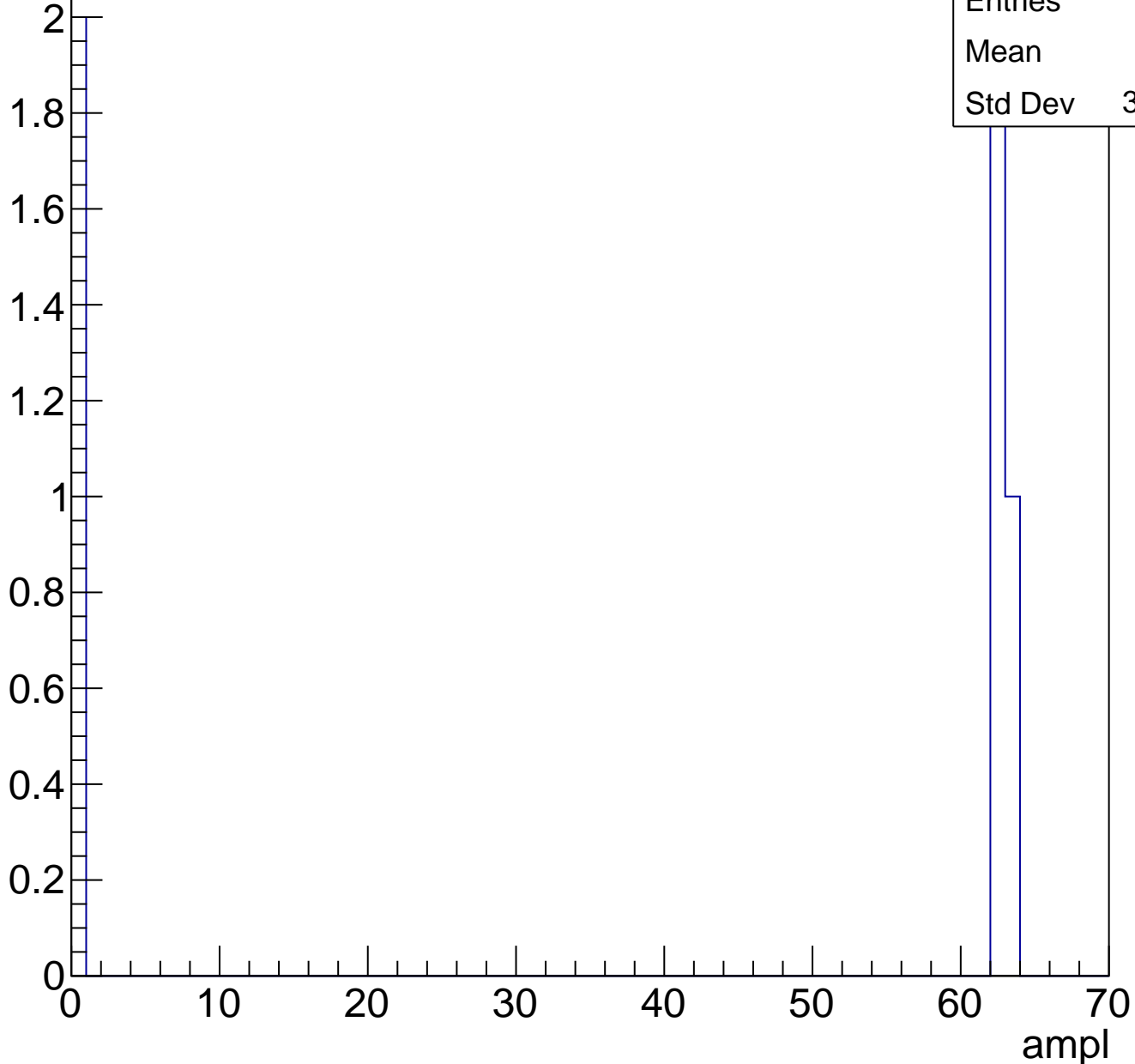




# B1L103S, U21-ch118, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U21-ch119, adc0

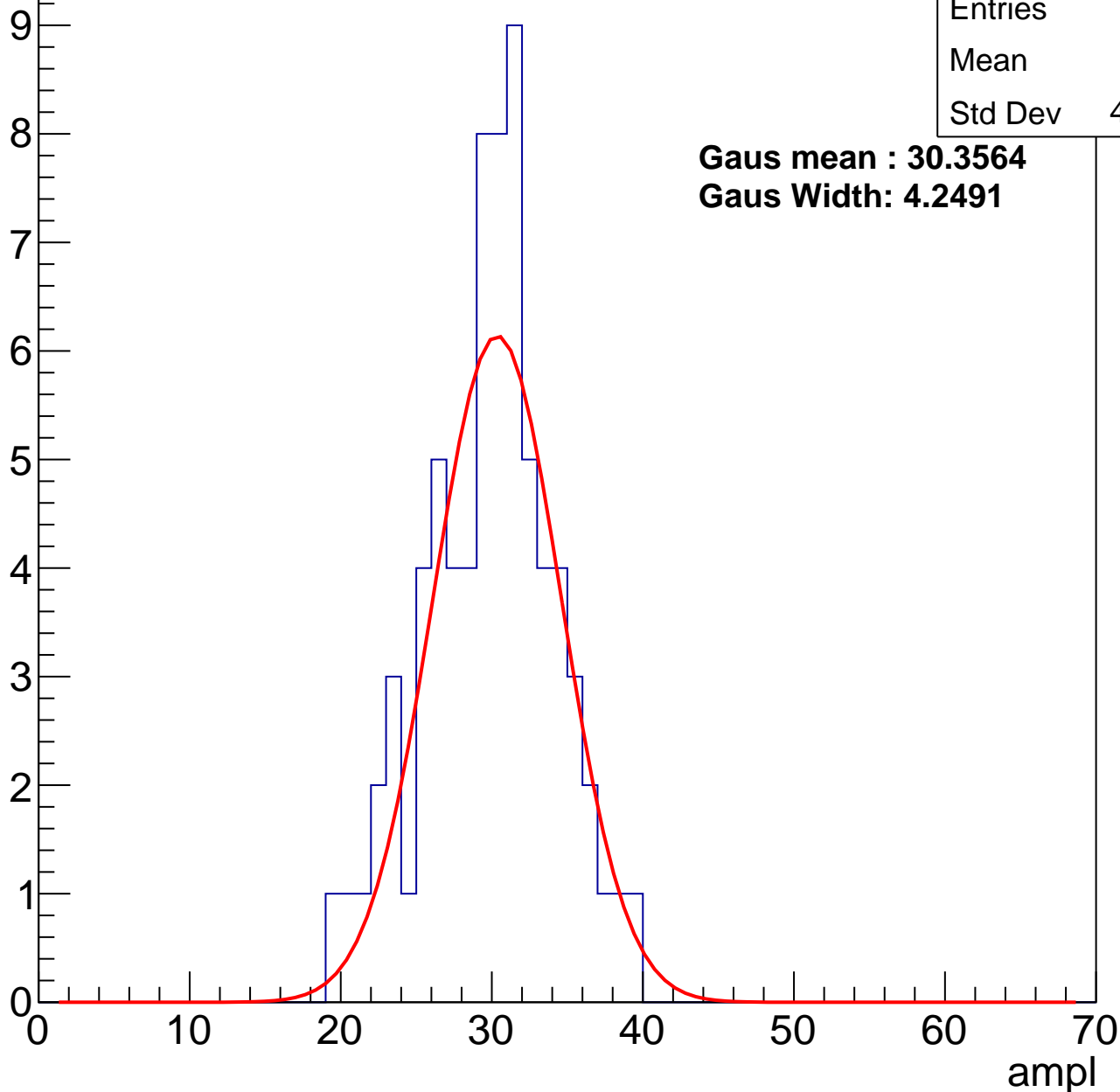
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	29.4
Std Dev	4.245

**Gaus mean : 30.3564**

**Gaus Width: 4.2491**



# B1L103S, U21-ch119, adc1

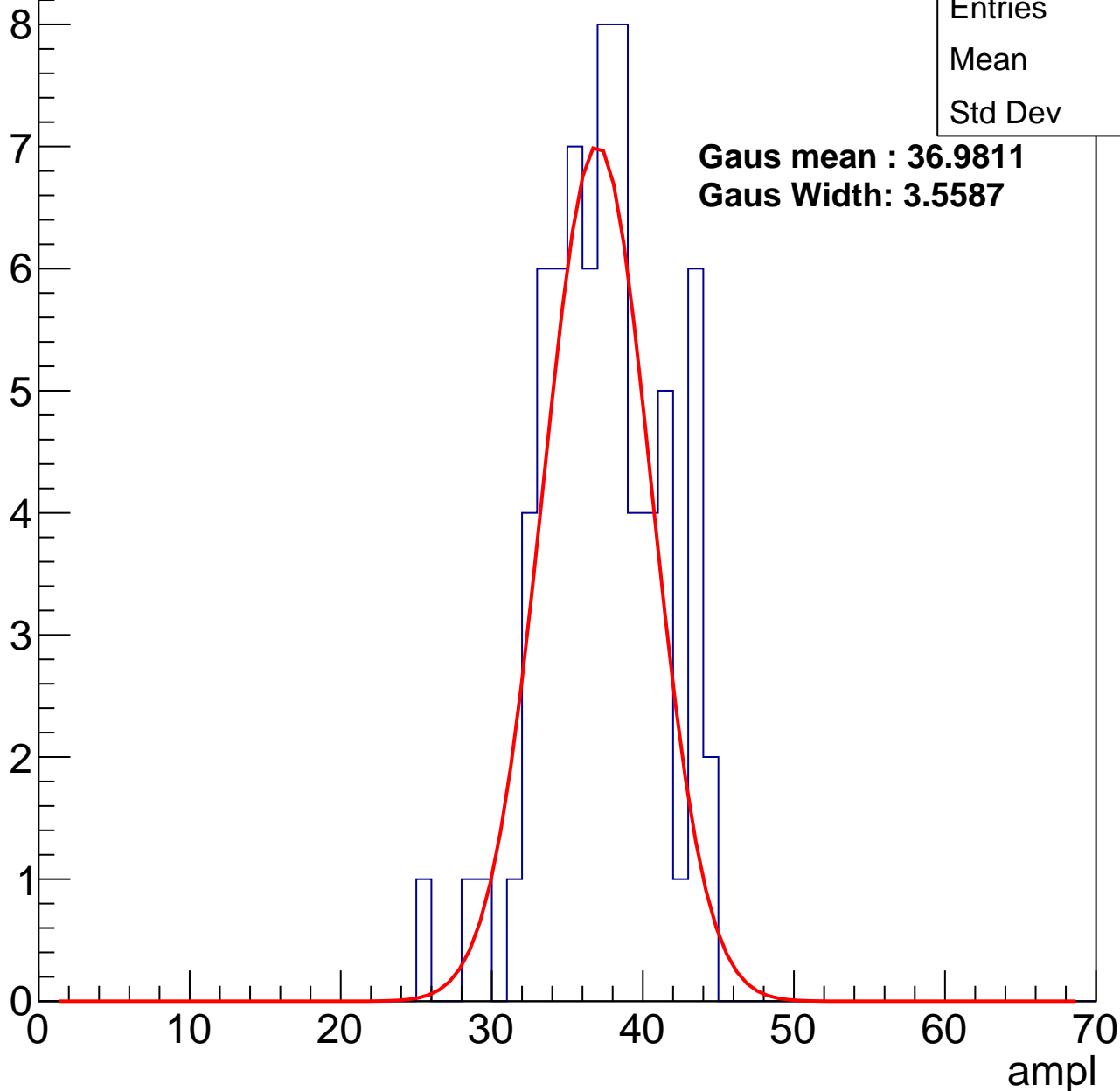
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	36.8
Std Dev	3.91

**Gaus mean : 36.9811**

**Gaus Width: 3.5587**



# B1L103S, U21-ch119, adc2

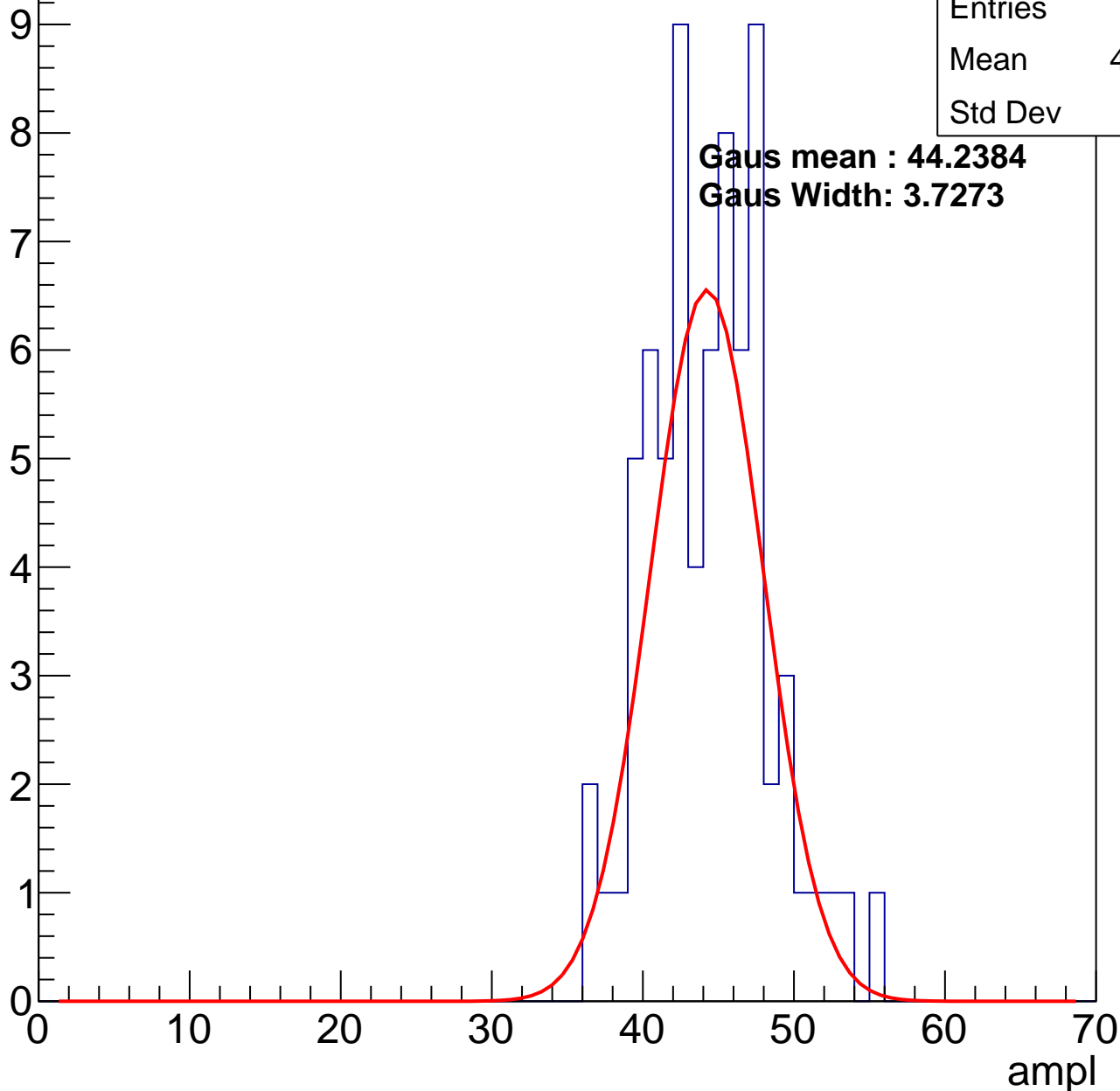
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	43.94
Std Dev	3.89

**Gaus mean : 44.2384**

**Gaus Width: 3.7273**

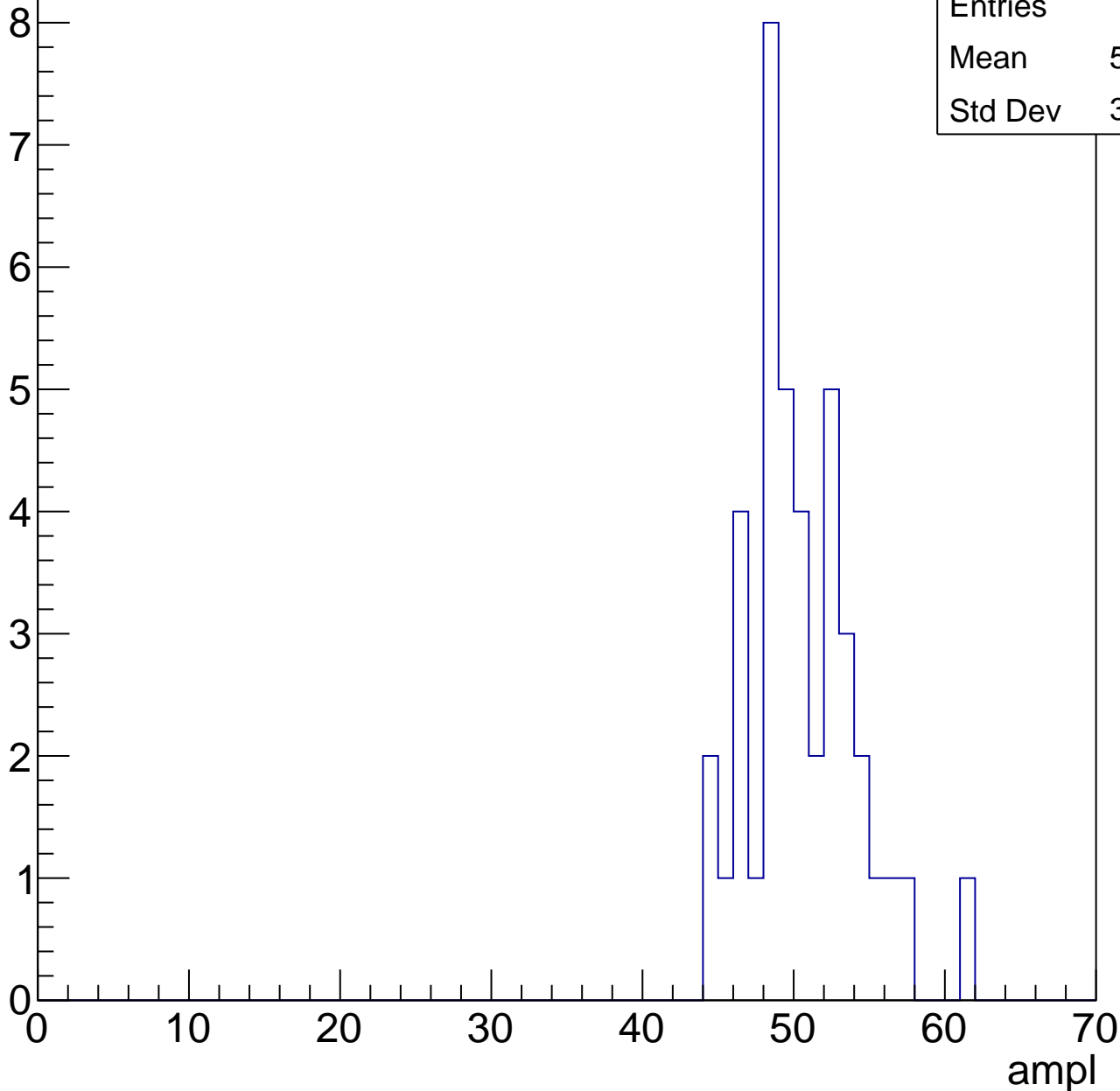


# B1L103S, U21-ch119, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	41
Mean	50.02
Std Dev	3.558

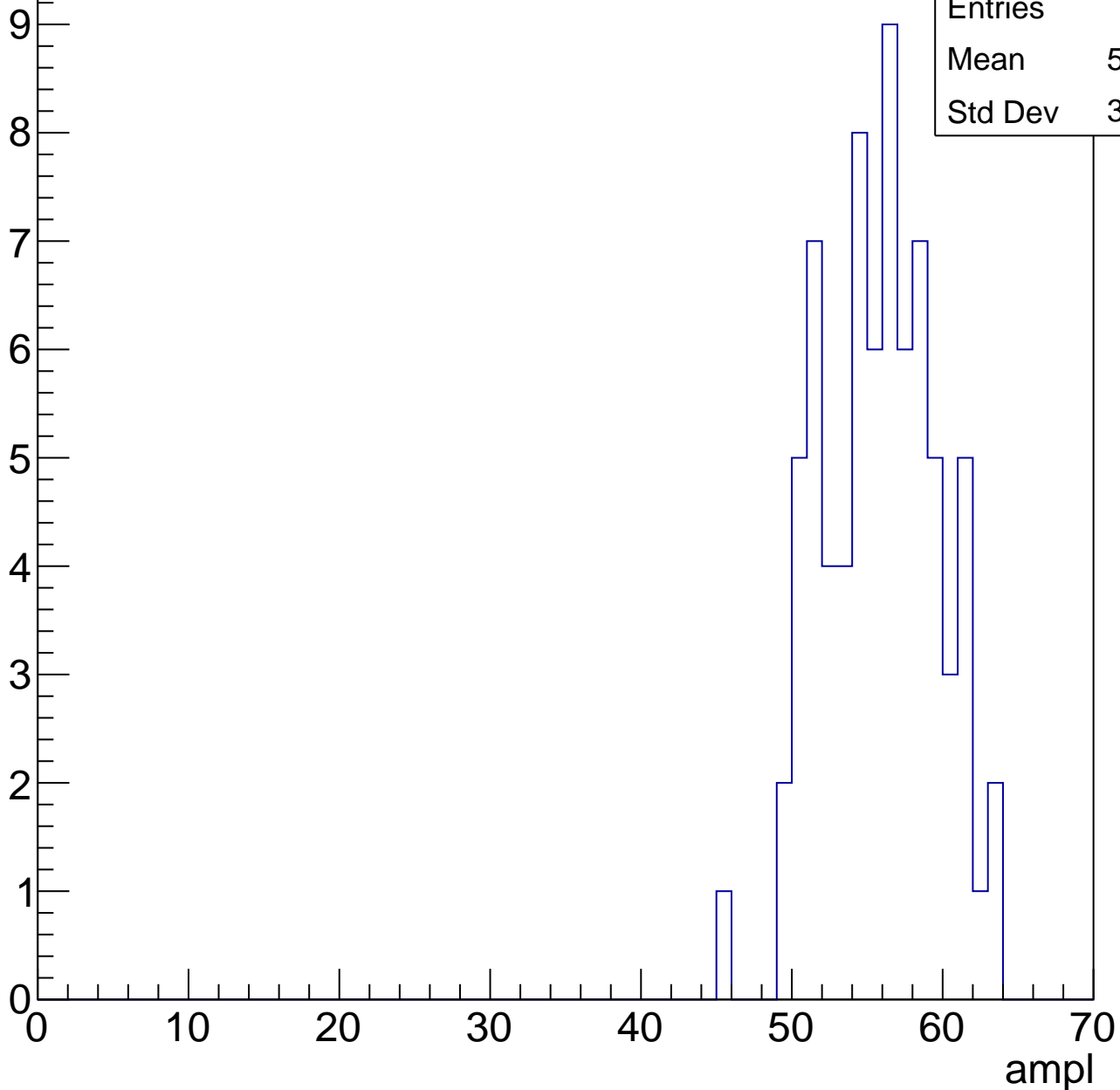


# B1L103S, U21-ch119, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	55.36
Std Dev	3.772

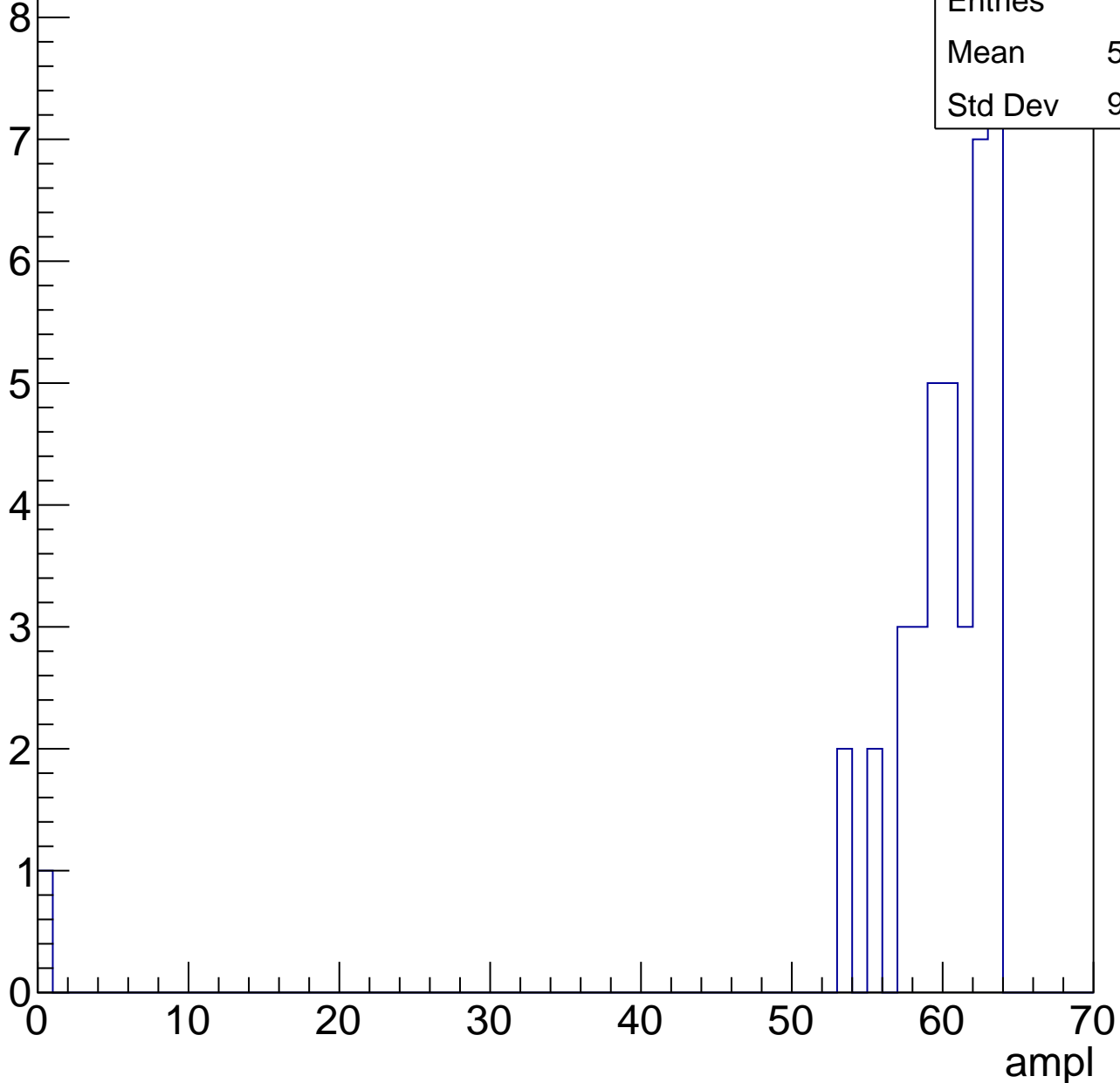


# B1L103S, U21-ch119, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

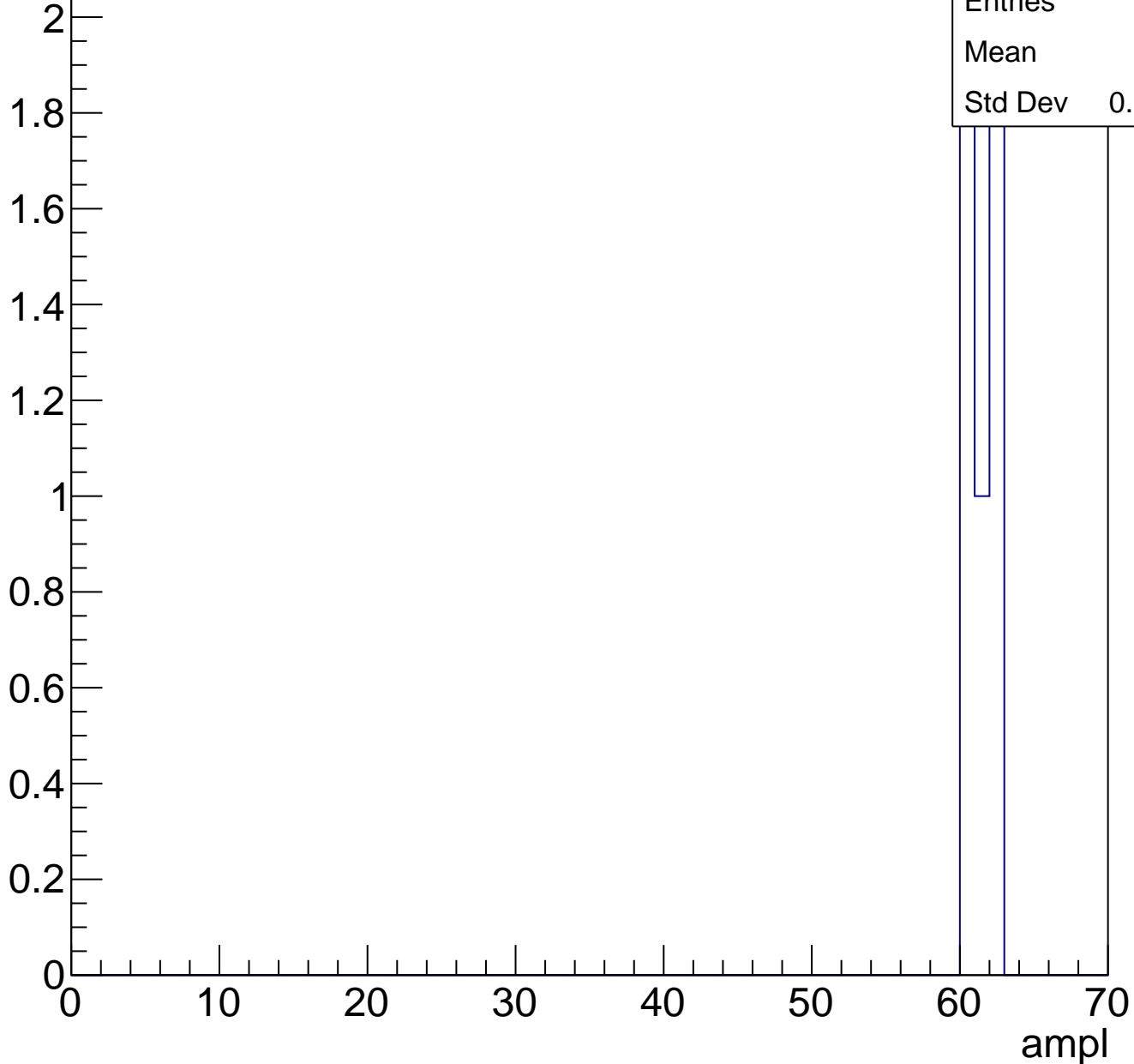
Entries	39
Mean	58.38
Std Dev	9.862



# B1L103S, U21-ch119, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U21-ch119, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U21-ch120, adc0

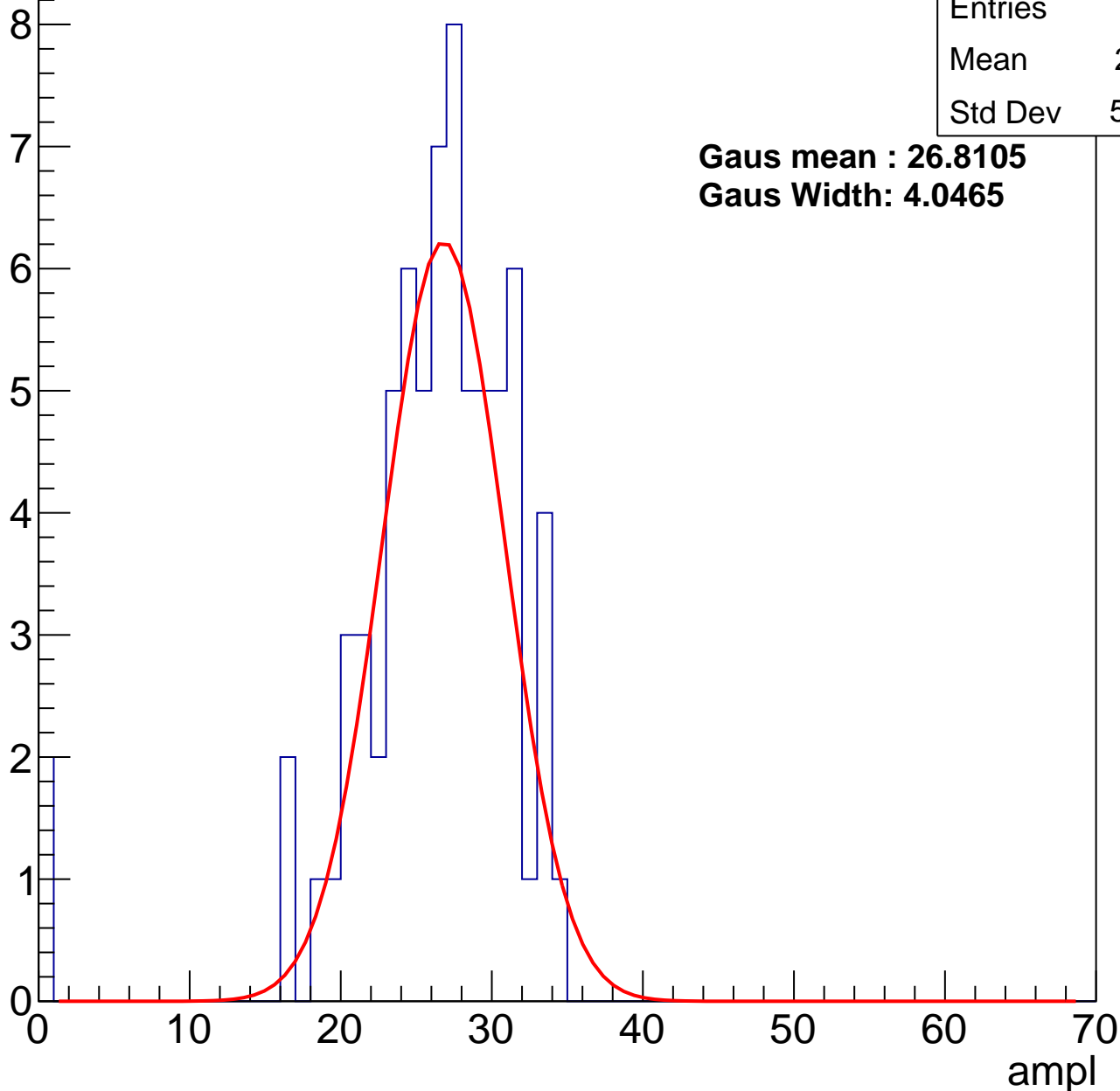
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	25.51
Std Dev	5.935

**Gaus mean : 26.8105**

**Gaus Width: 4.0465**



# B1L103S, U21-ch120, adc1

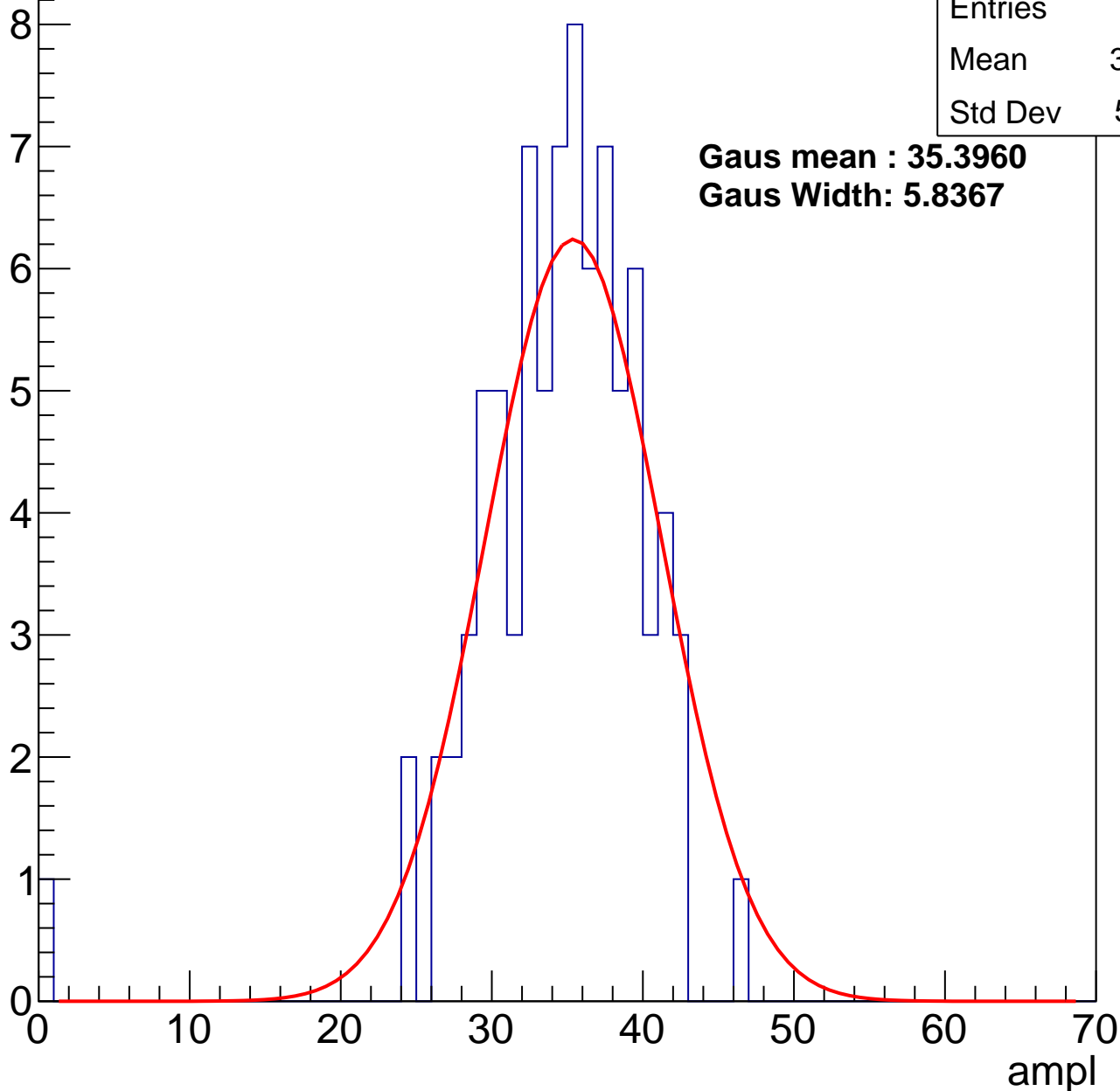
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	85
Mean	33.98
Std Dev	5.861

**Gaus mean : 35.3960**

**Gaus Width: 5.8367**



# B1L103S, U21-ch120, adc2

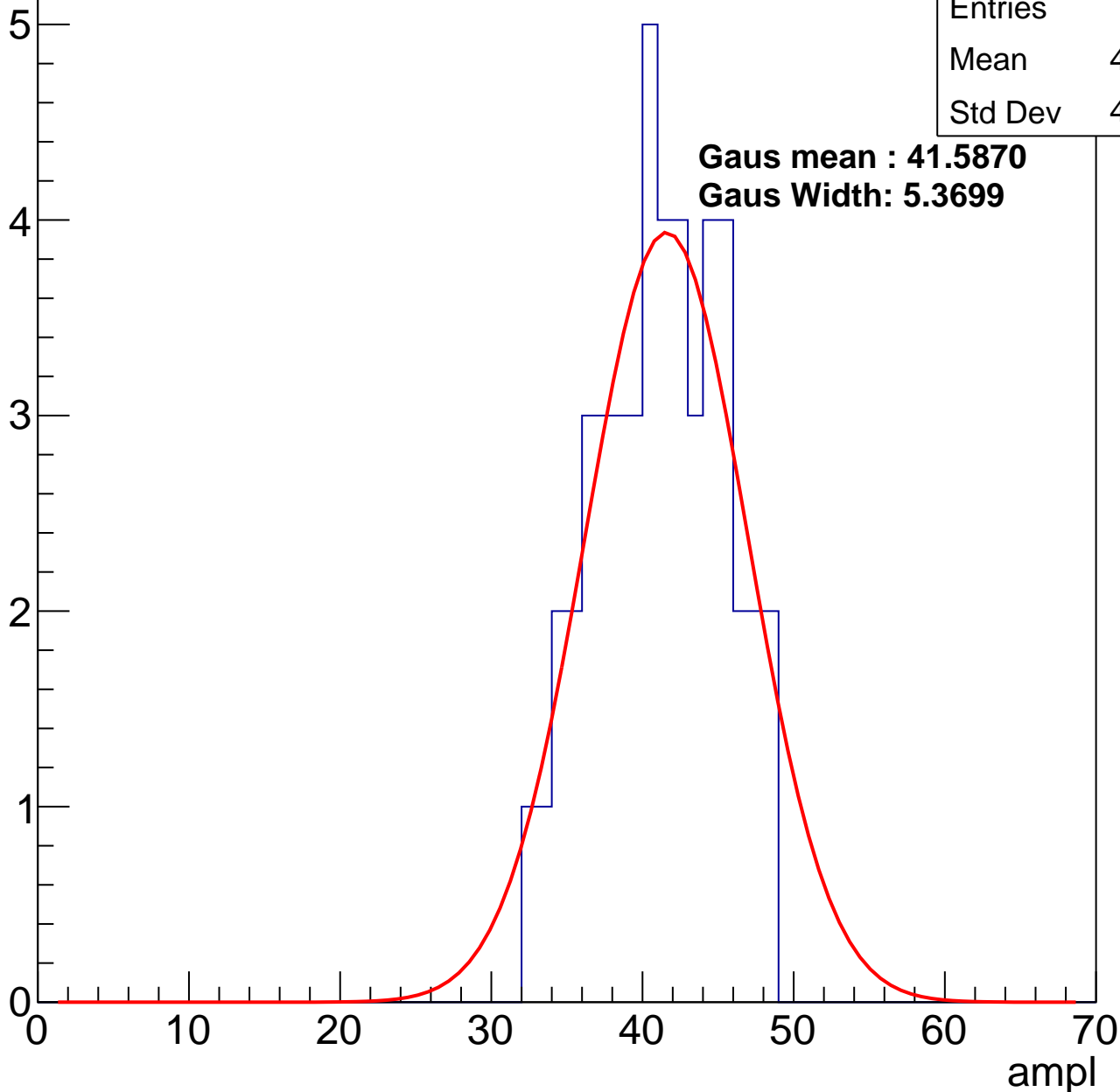
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	48
Mean	40.67
Std Dev	4.115

**Gaus mean : 41.5870**

**Gaus Width: 5.3699**

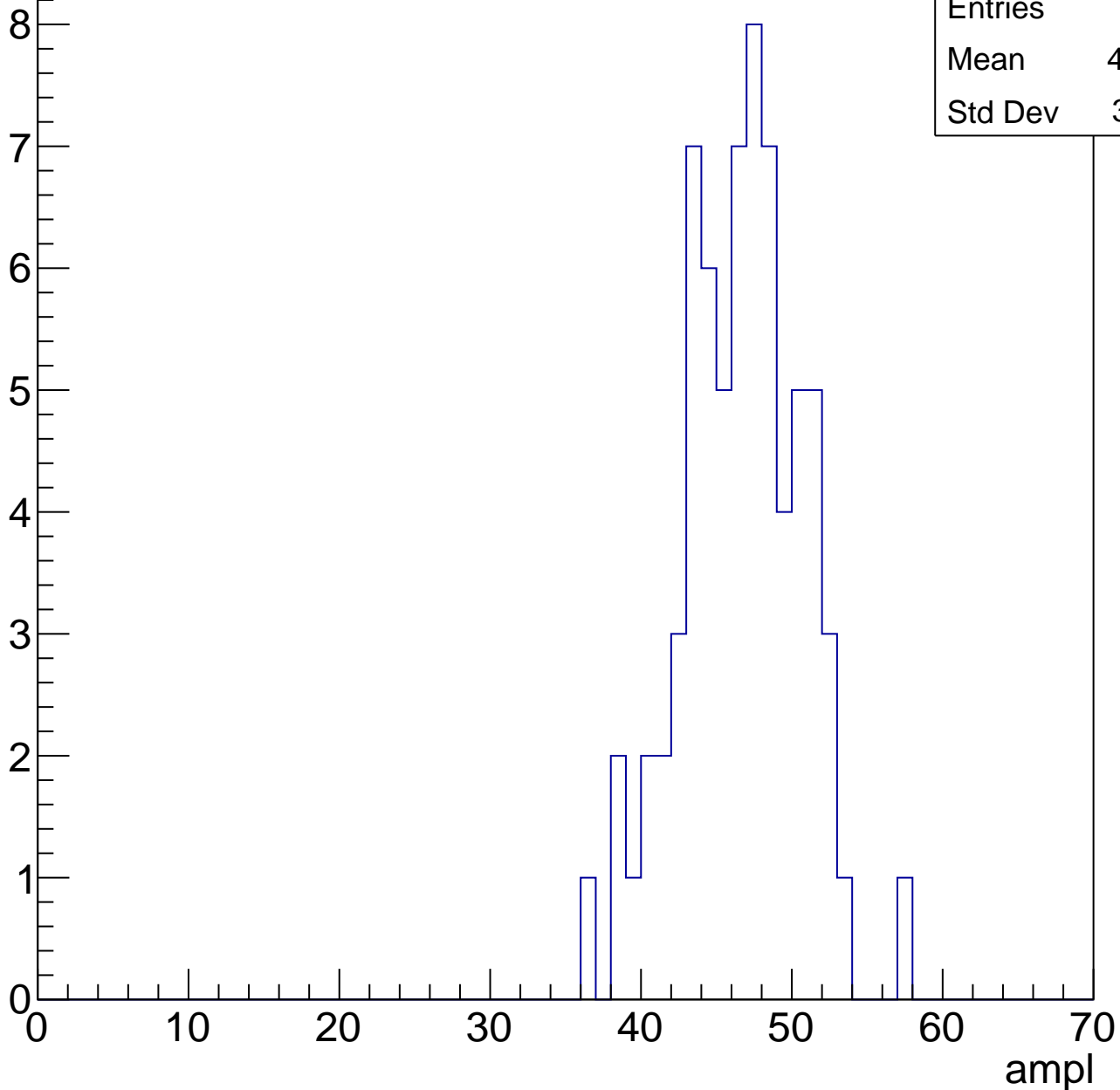


# B1L103S, U21-ch120, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	46.14
Std Dev	3.951

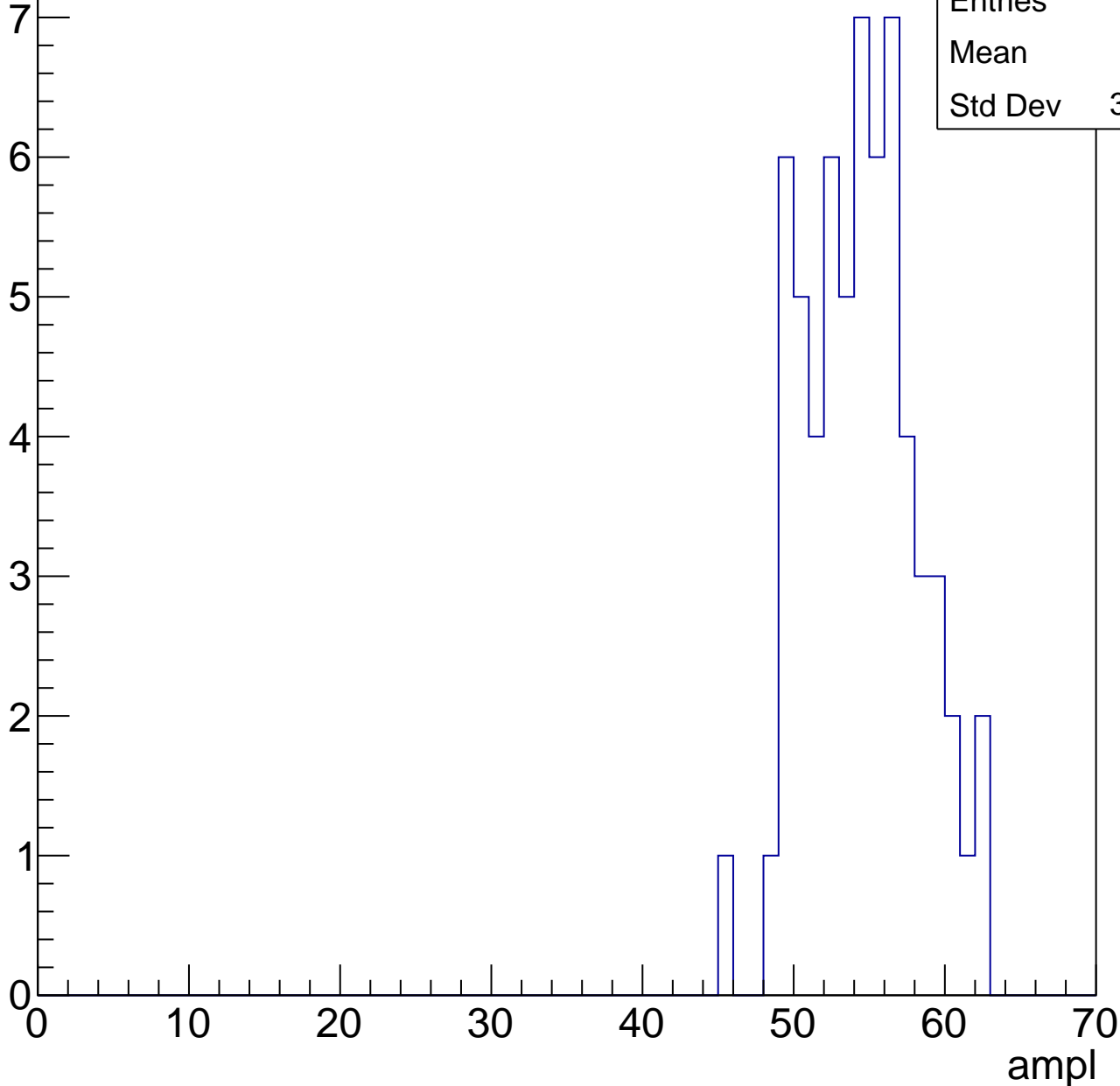


# B1L103S, U21-ch120, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

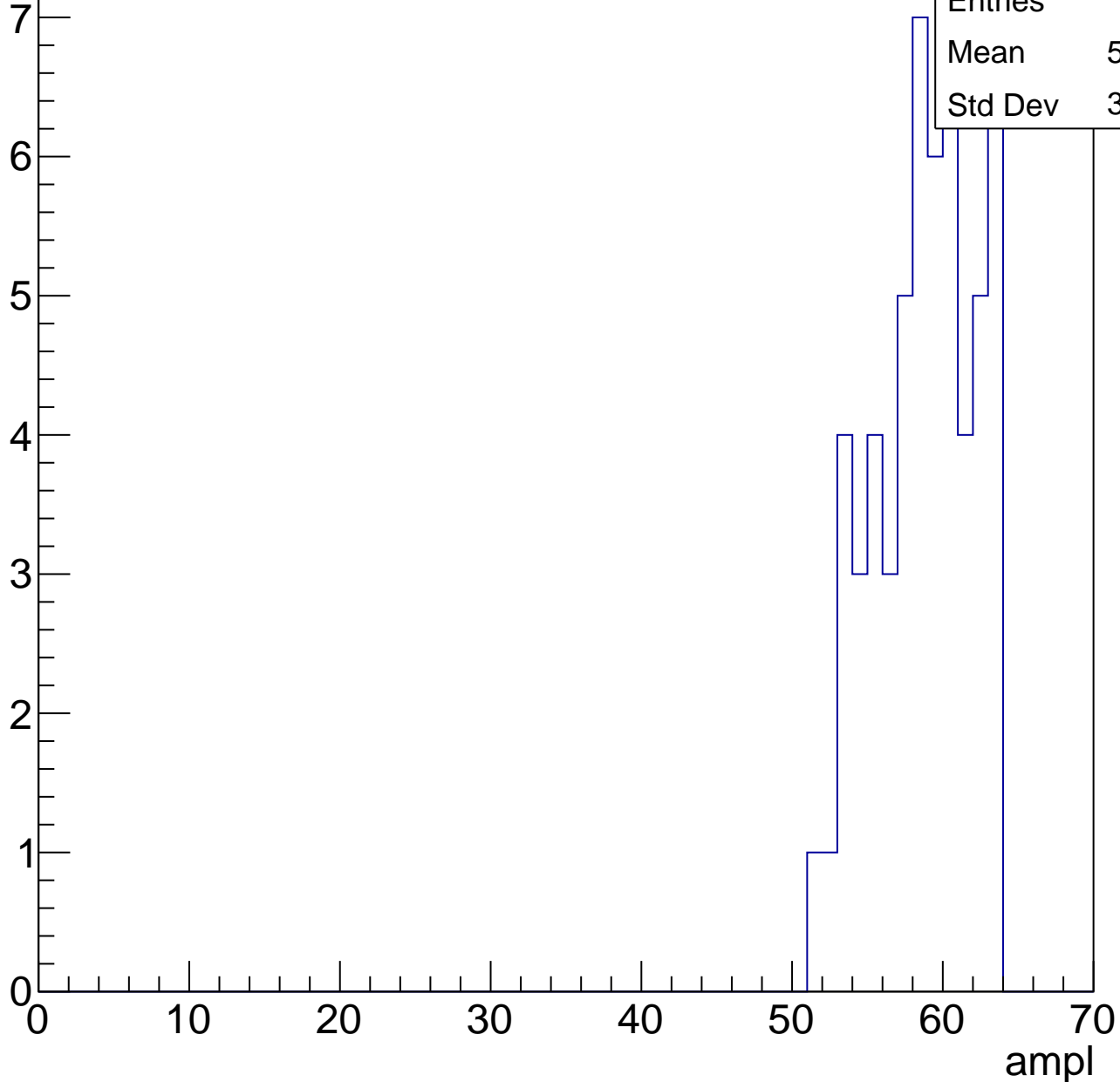
Entries	63
Mean	54
Std Dev	3.682



# B1L103S, U21-ch120, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

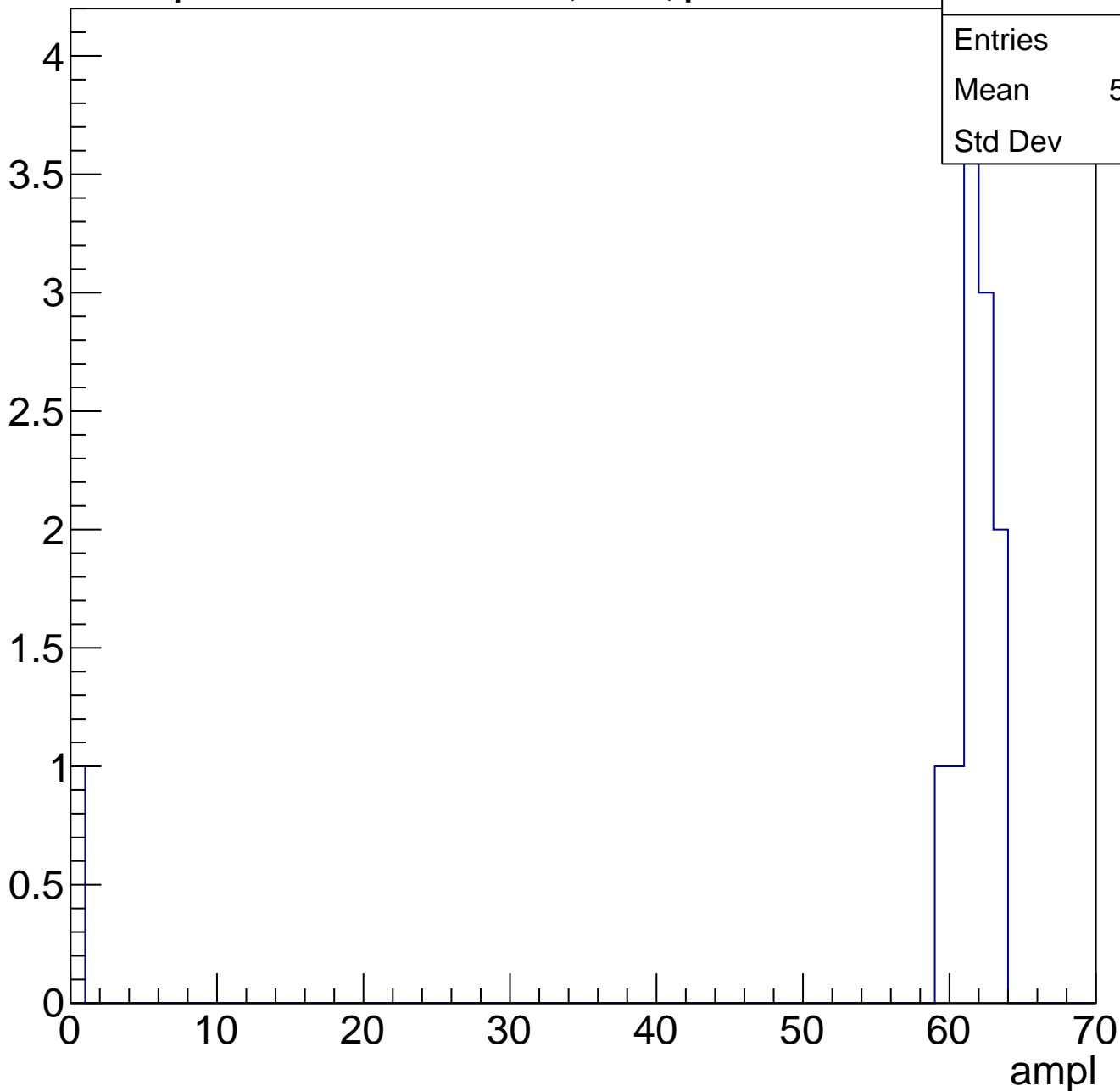
Entry



# B1L103S, U21-ch120, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

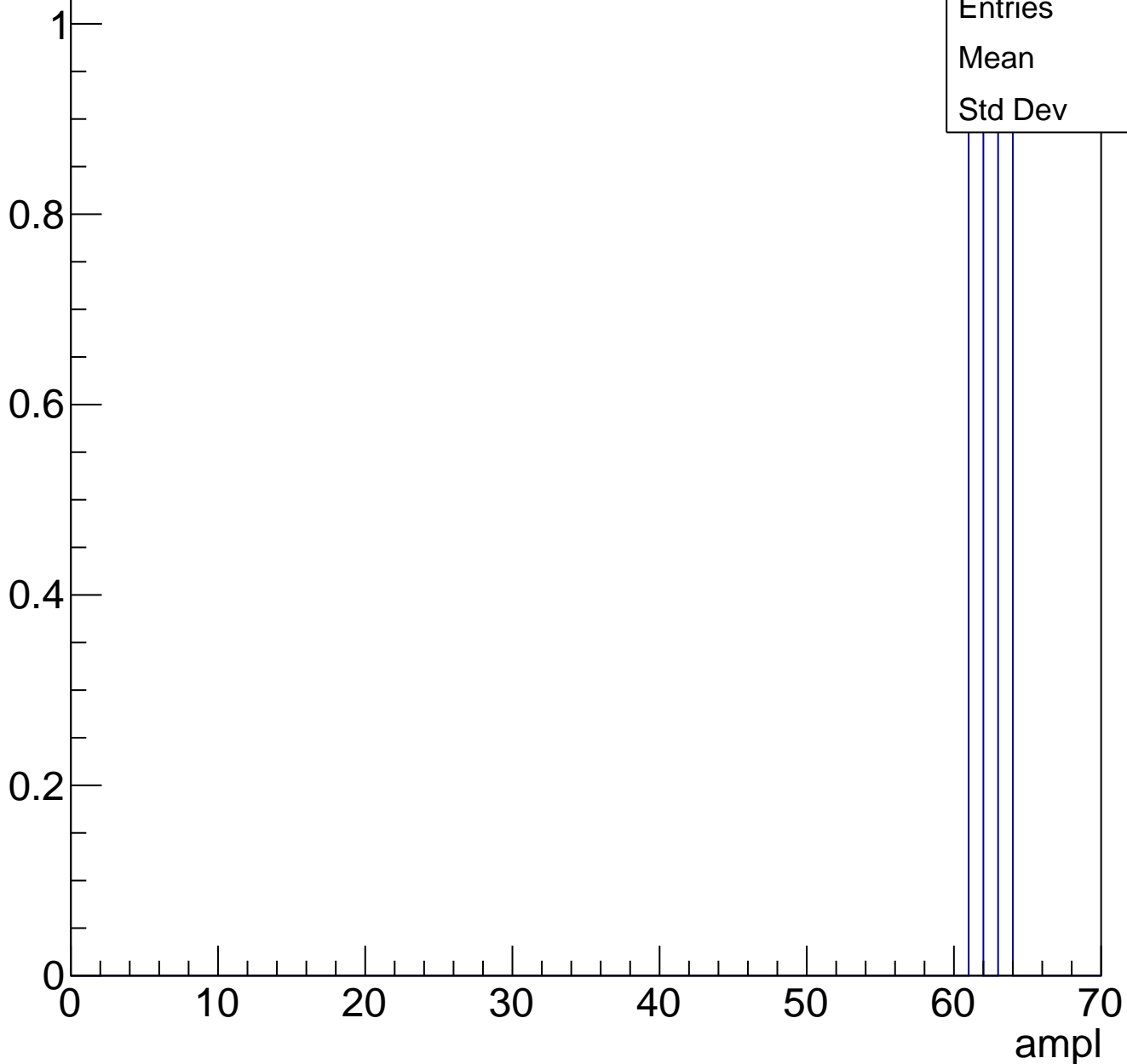




# B1L103S, U21-ch120, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U21-ch121, adc0

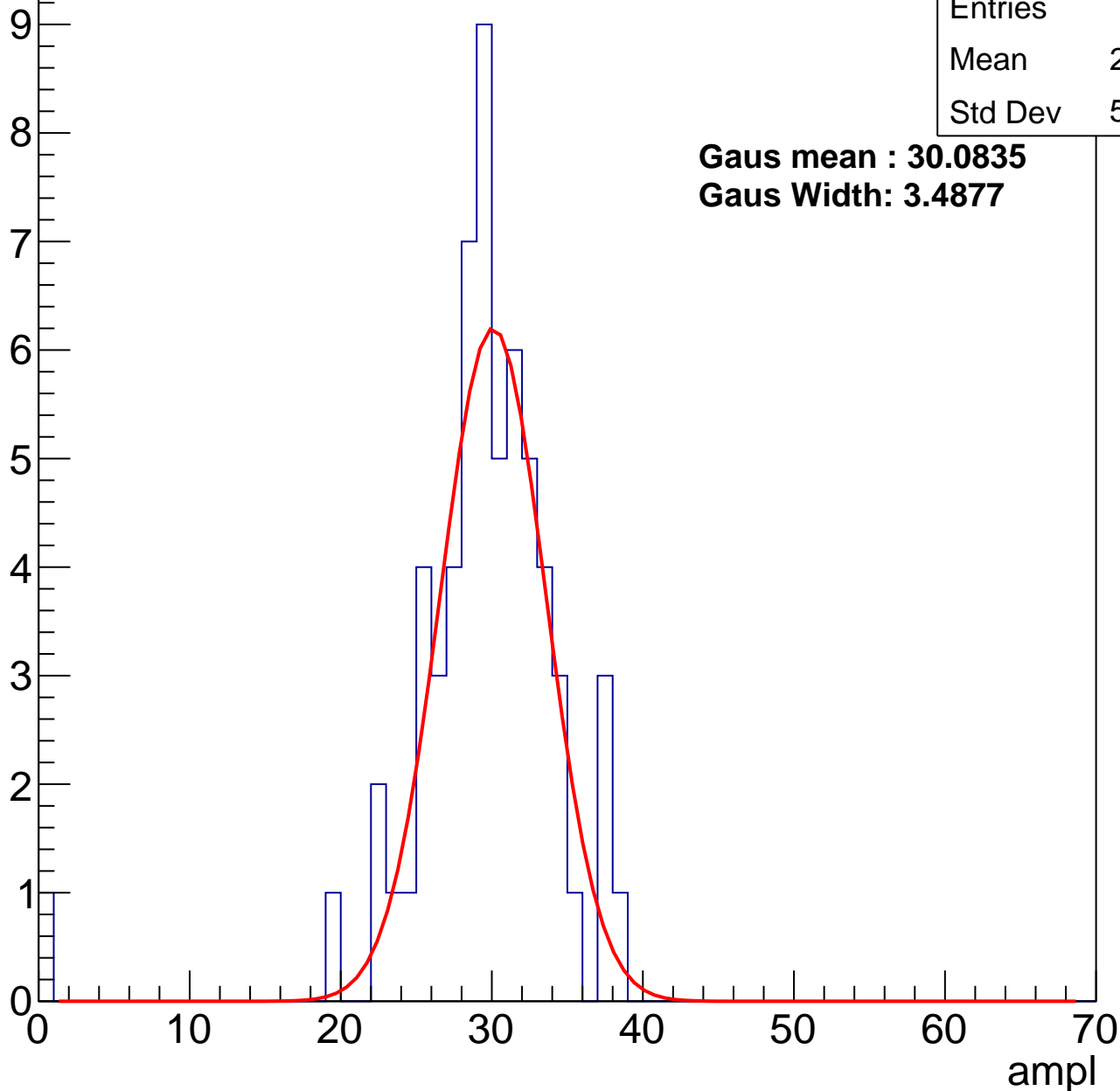
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	28.97
Std Dev	5.335

**Gaus mean : 30.0835**

**Gaus Width: 3.4877**



# B1L103S, U21-ch121, adc1

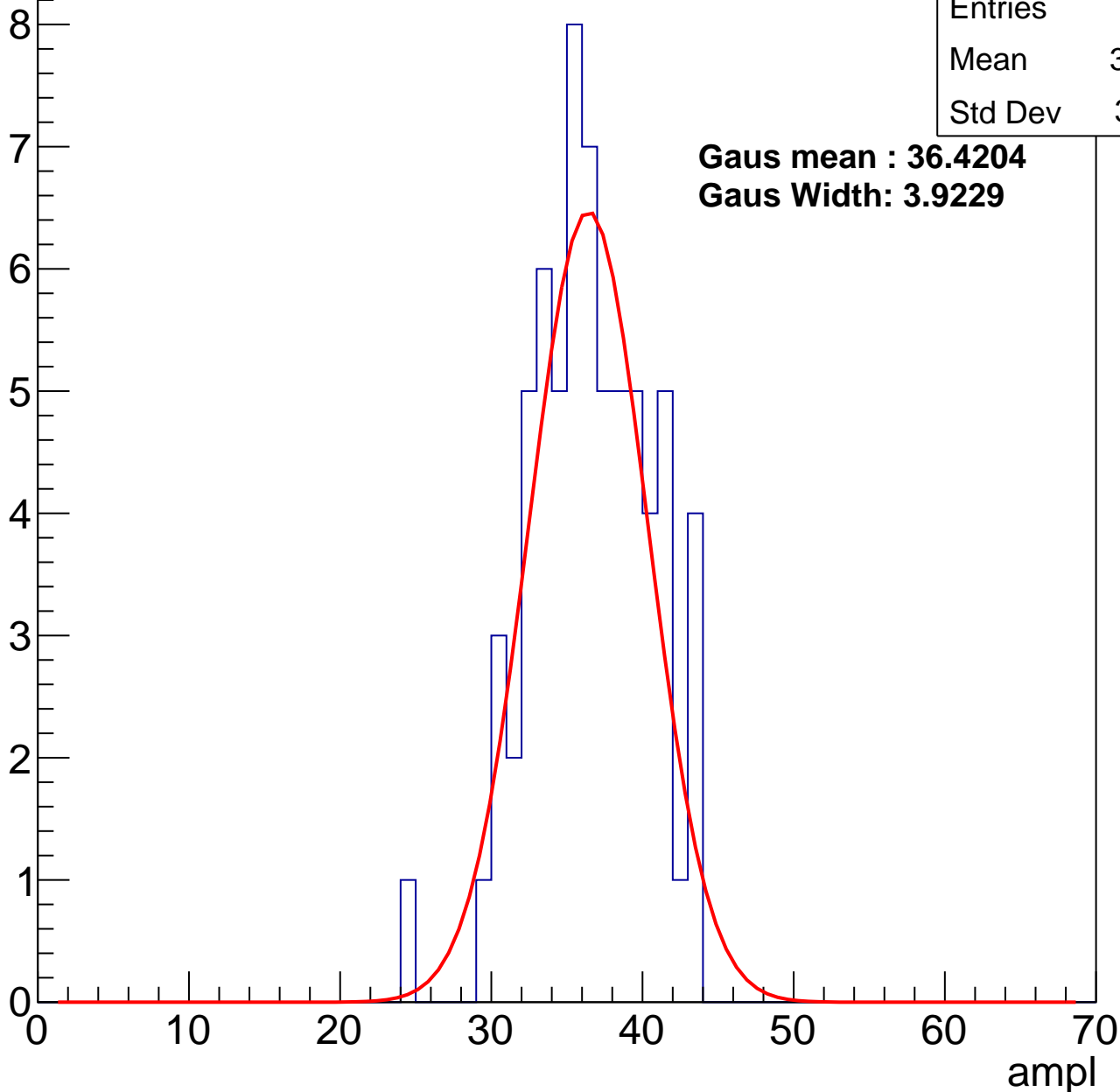
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	36.03
Std Dev	3.871

**Gaus mean : 36.4204**

**Gaus Width: 3.9229**



# B1L103S, U21-ch121, adc2

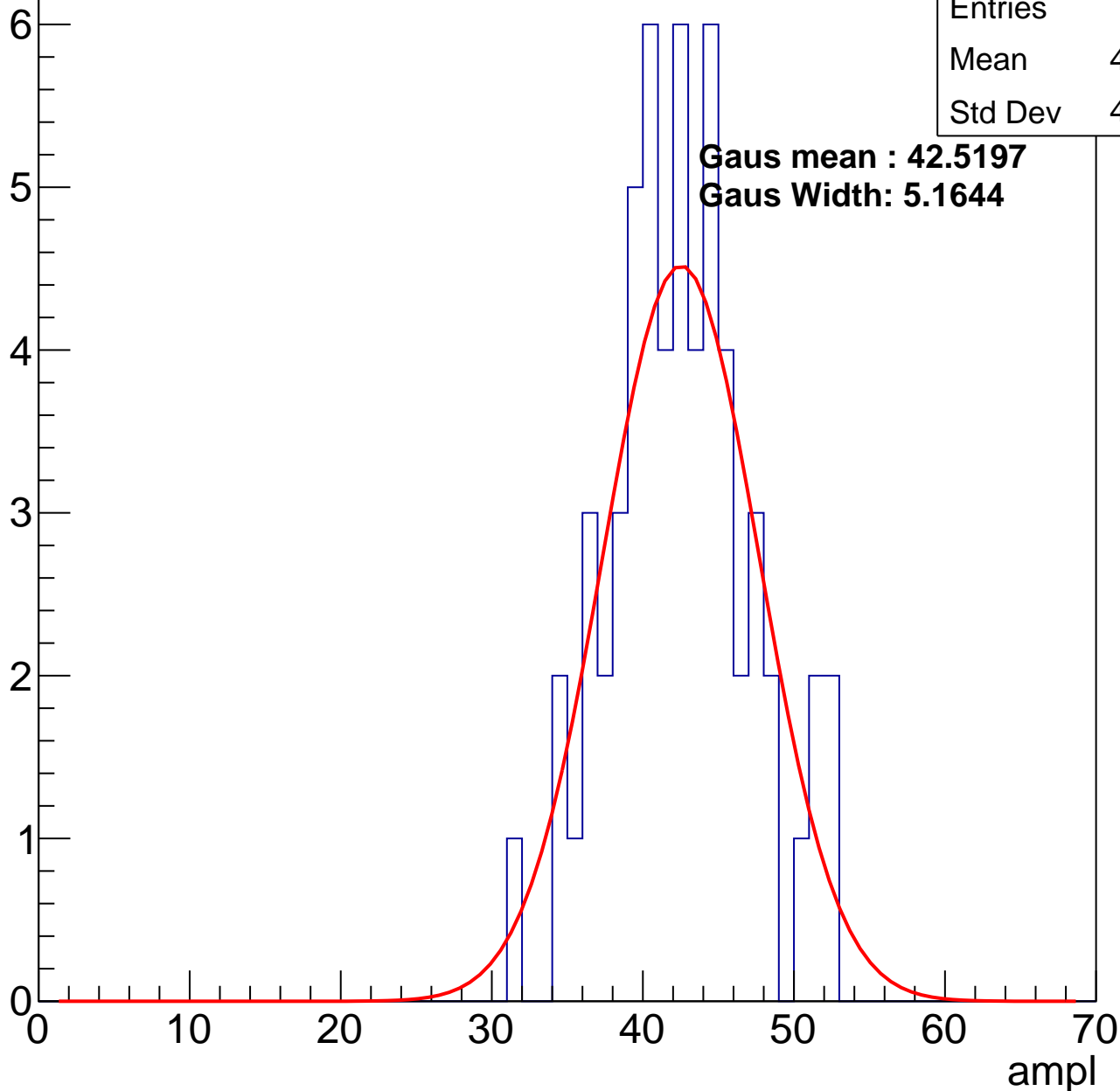
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	42.07
Std Dev	4.595

**Gaus mean : 42.5197**

**Gaus Width: 5.1644**

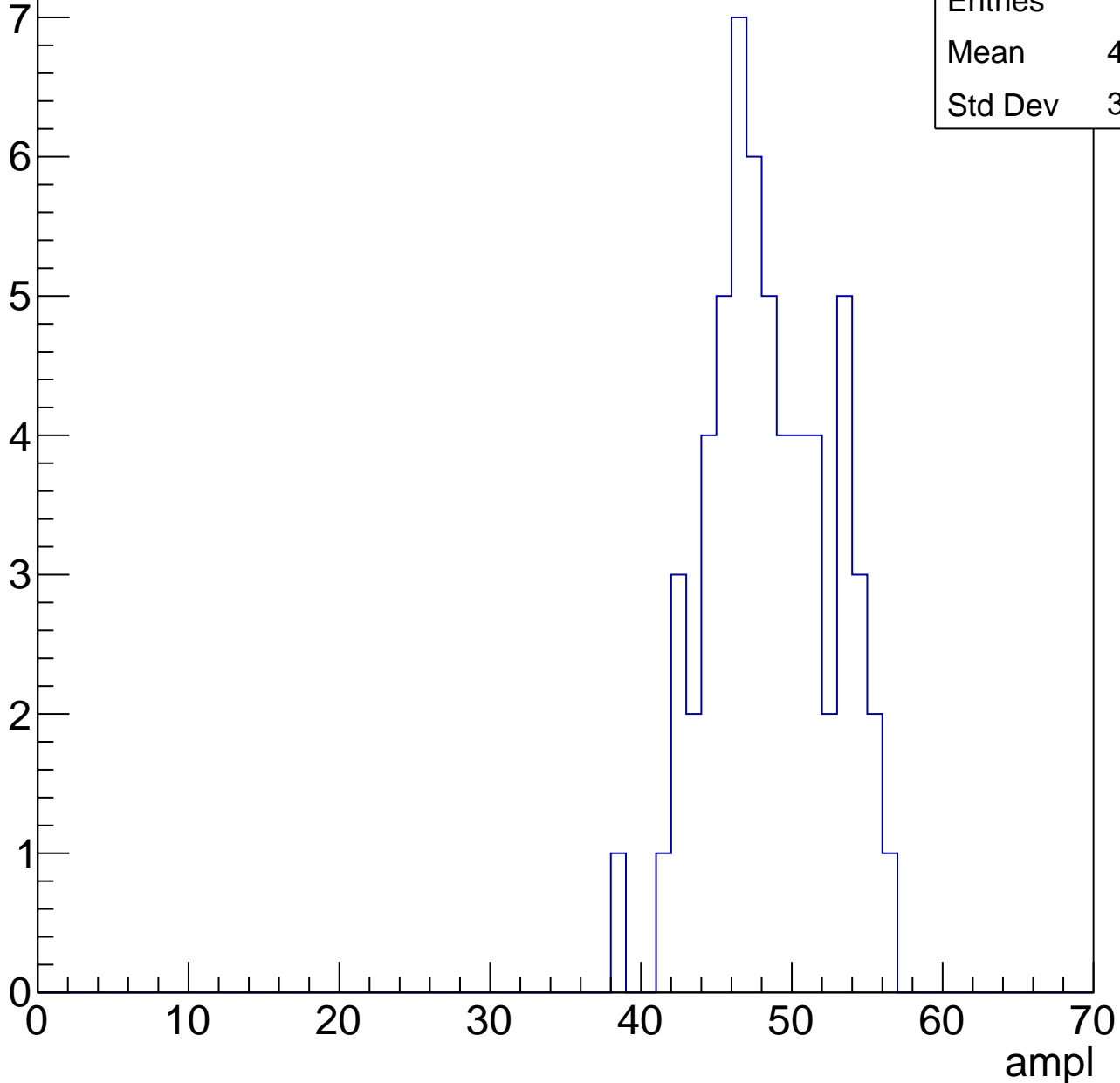


# B1L103S, U21-ch121, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	48.02
Std Dev	3.977

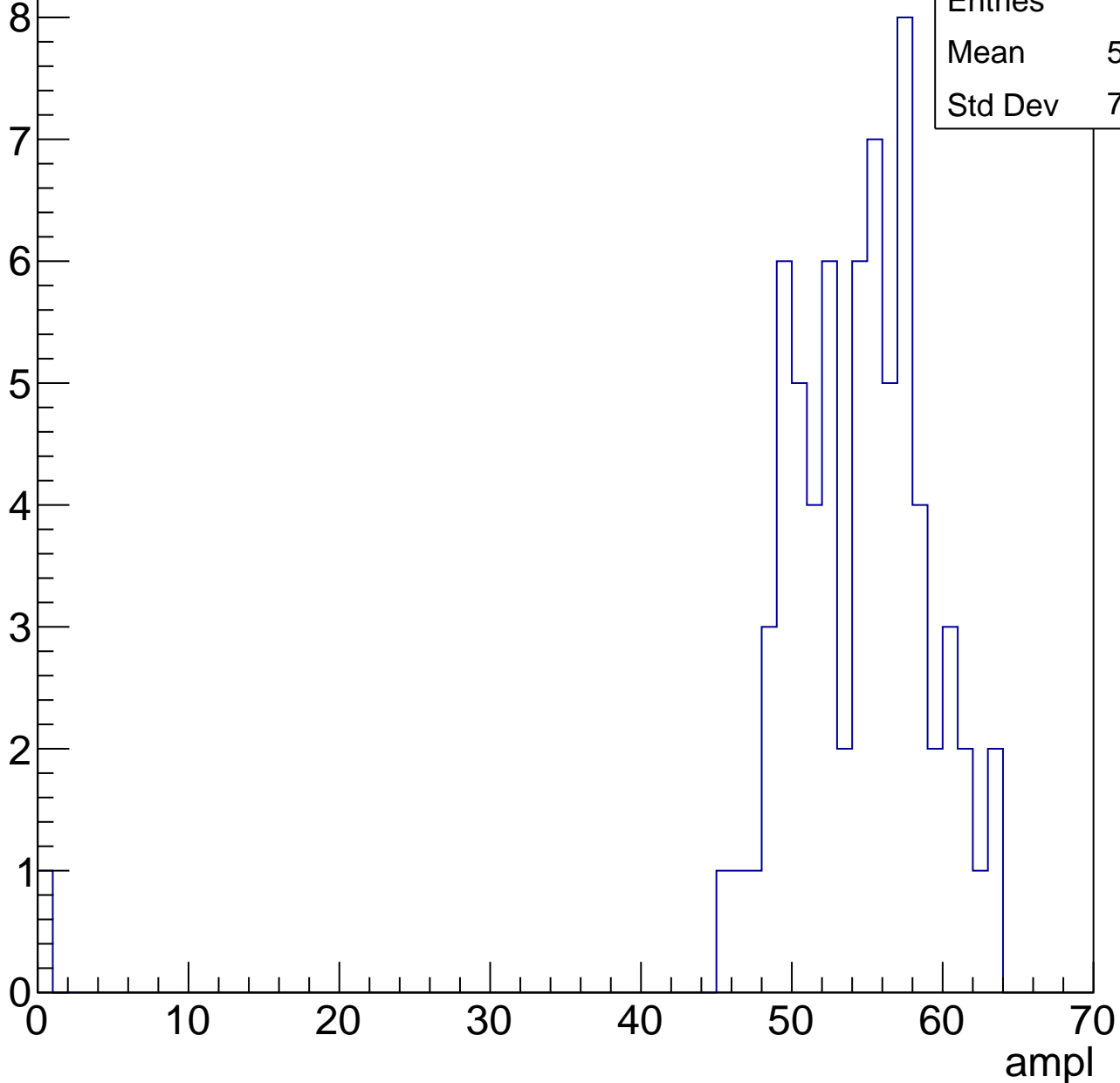


# B1L103S, U21-ch121, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

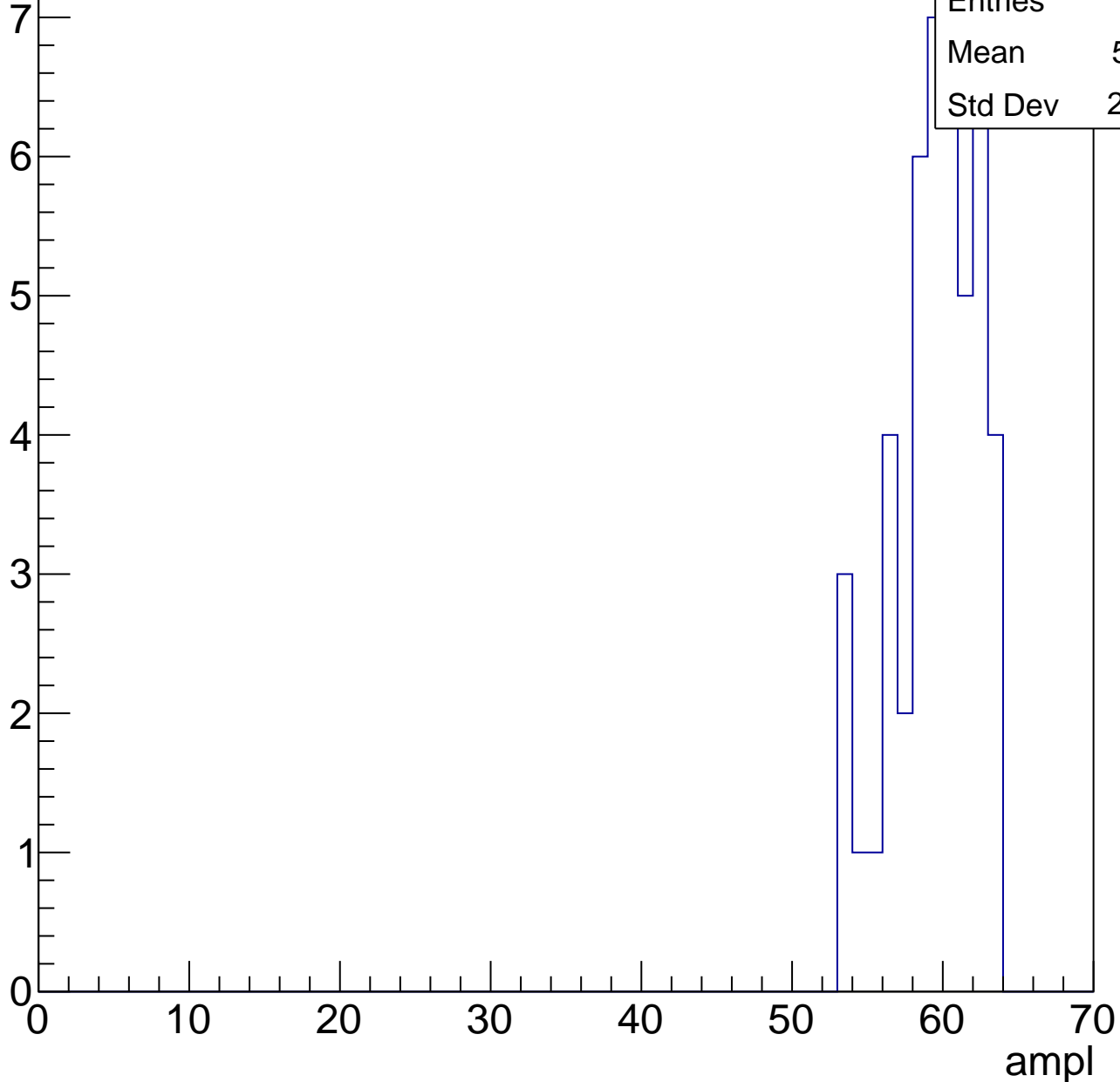
Entries	70
Mean	53.33
Std Dev	7.675



# B1L103S, U21-ch121, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

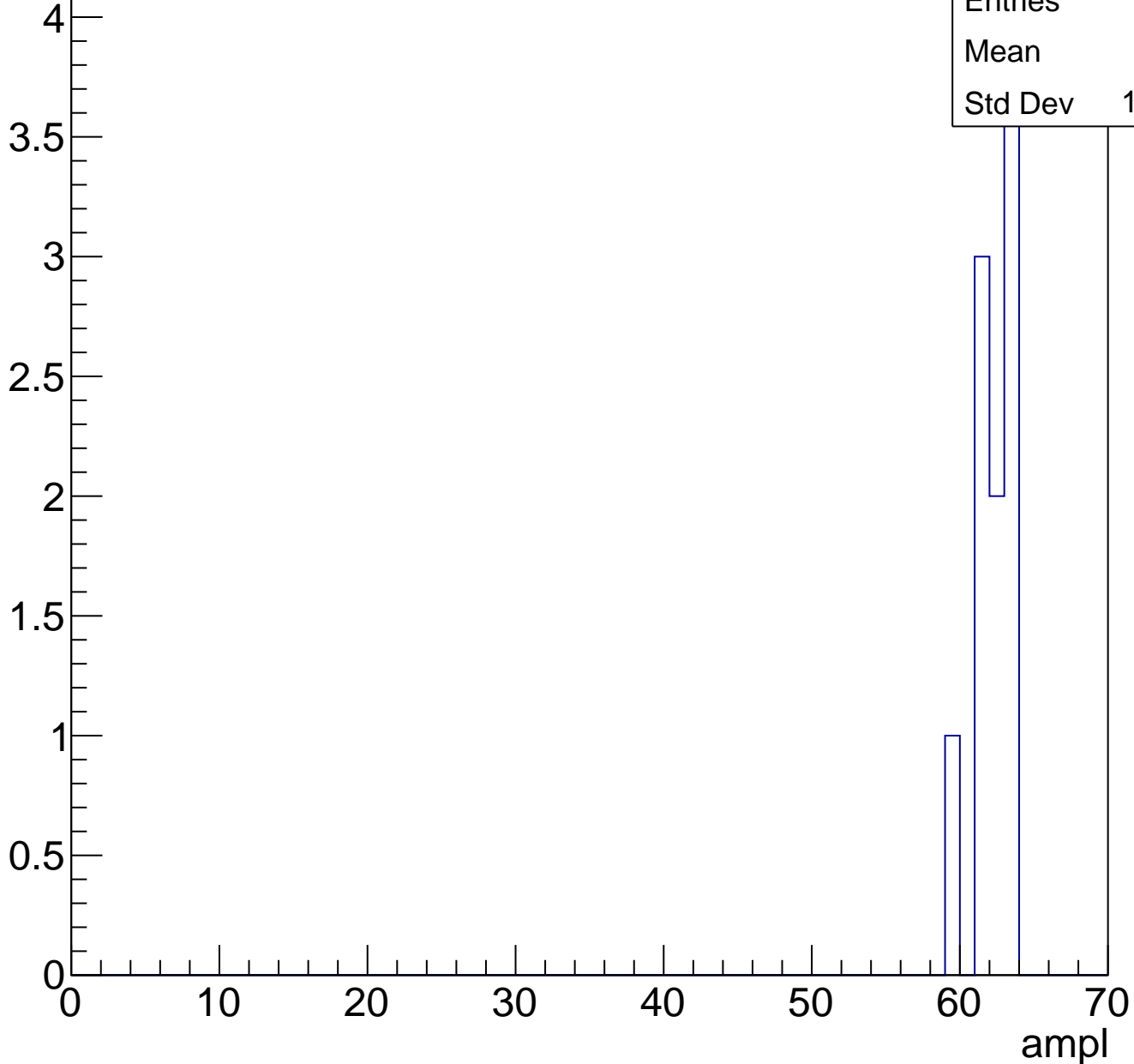
Entry



# B1L103S, U21-ch121, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	10
Mean	61.8
Std Dev	1.249



# B1L103S, U21-ch121, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L103S, U21-ch122, adc0

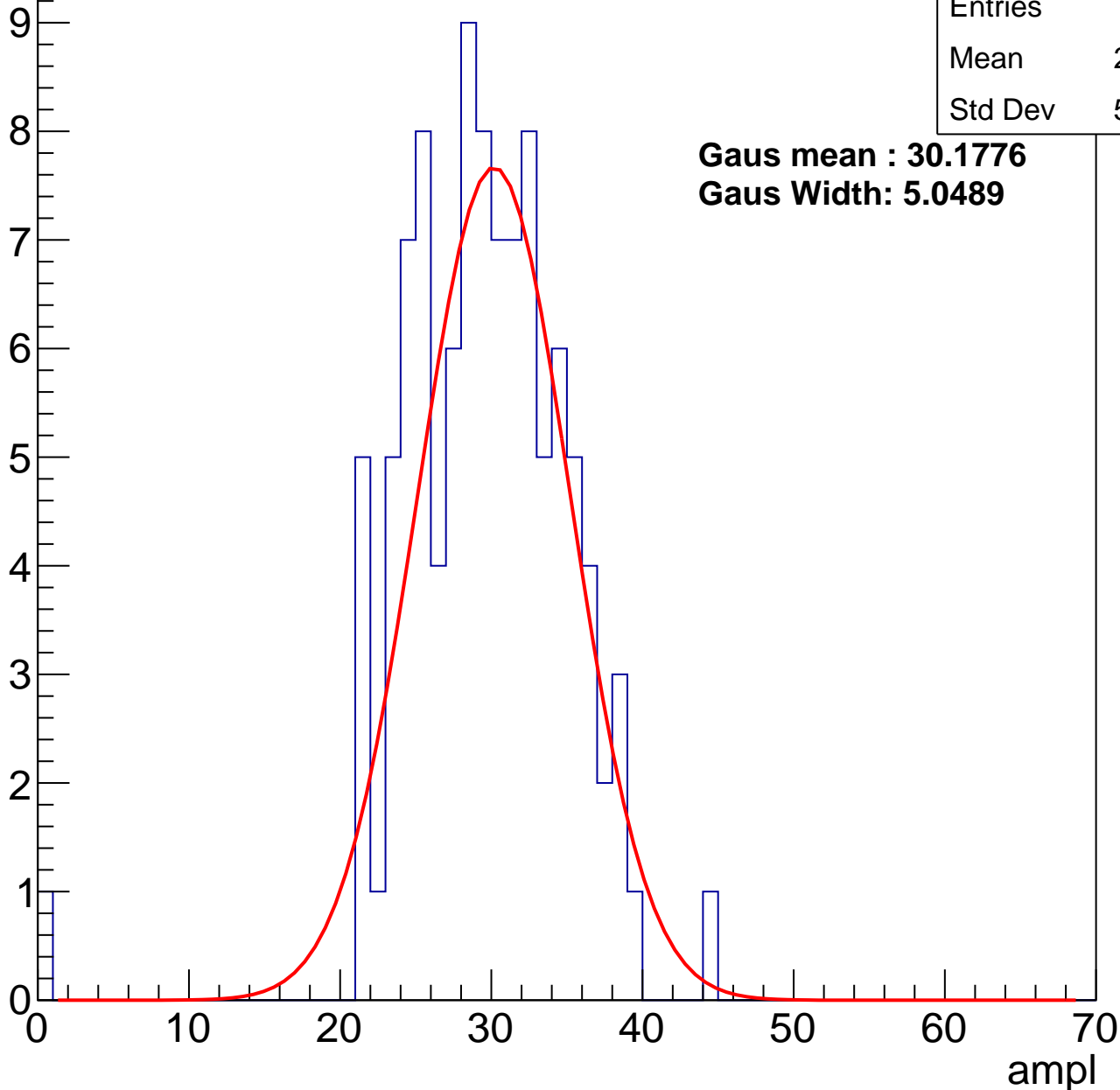
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	103
Mean	29.15
Std Dev	5.547

**Gaus mean : 30.1776**

**Gaus Width: 5.0489**



# B1L103S, U21-ch122, adc1

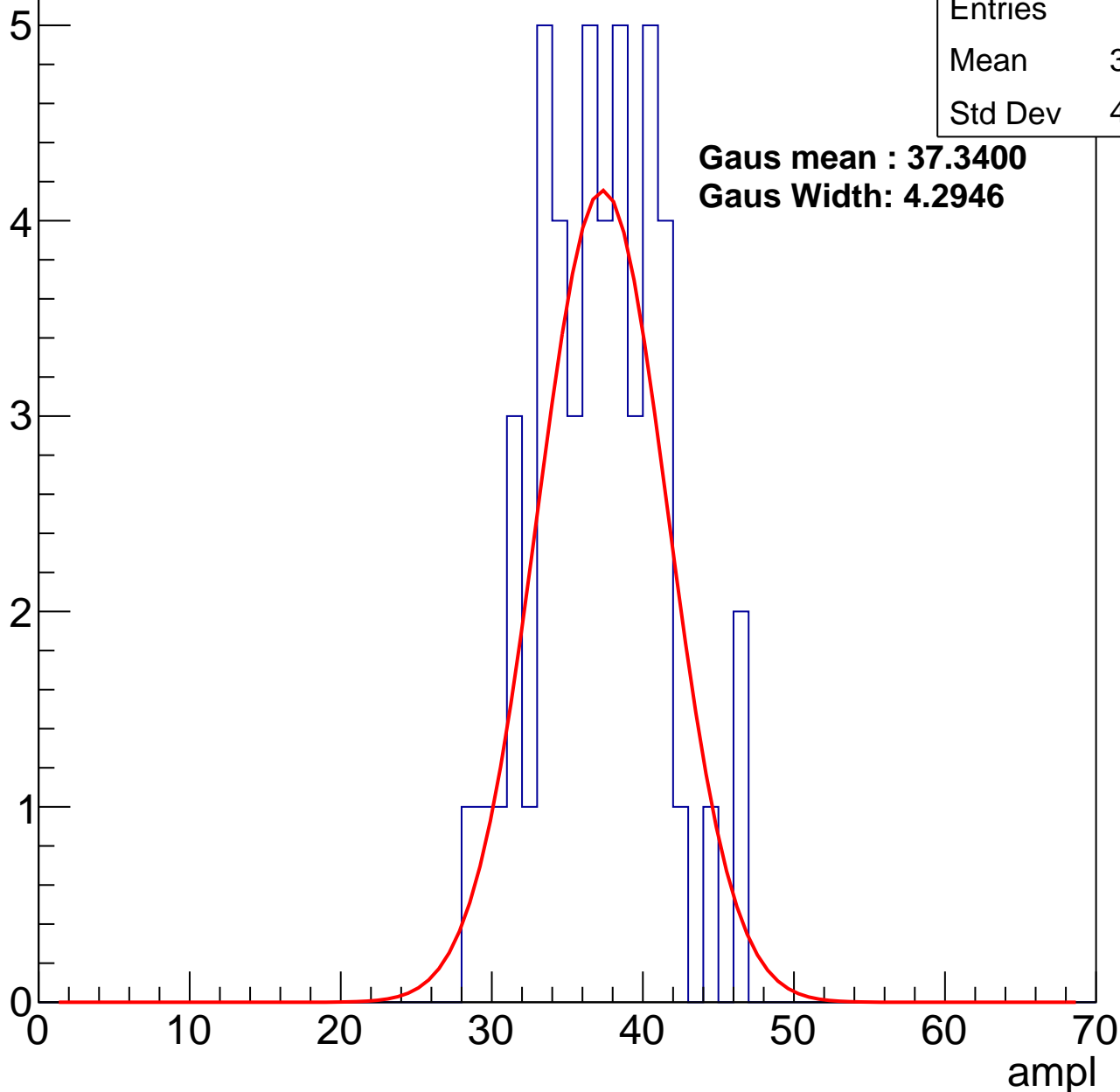
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	36.63
Std Dev	4.079

**Gaus mean : 37.3400**

**Gaus Width: 4.2946**



# B1L103S, U21-ch122, adc2

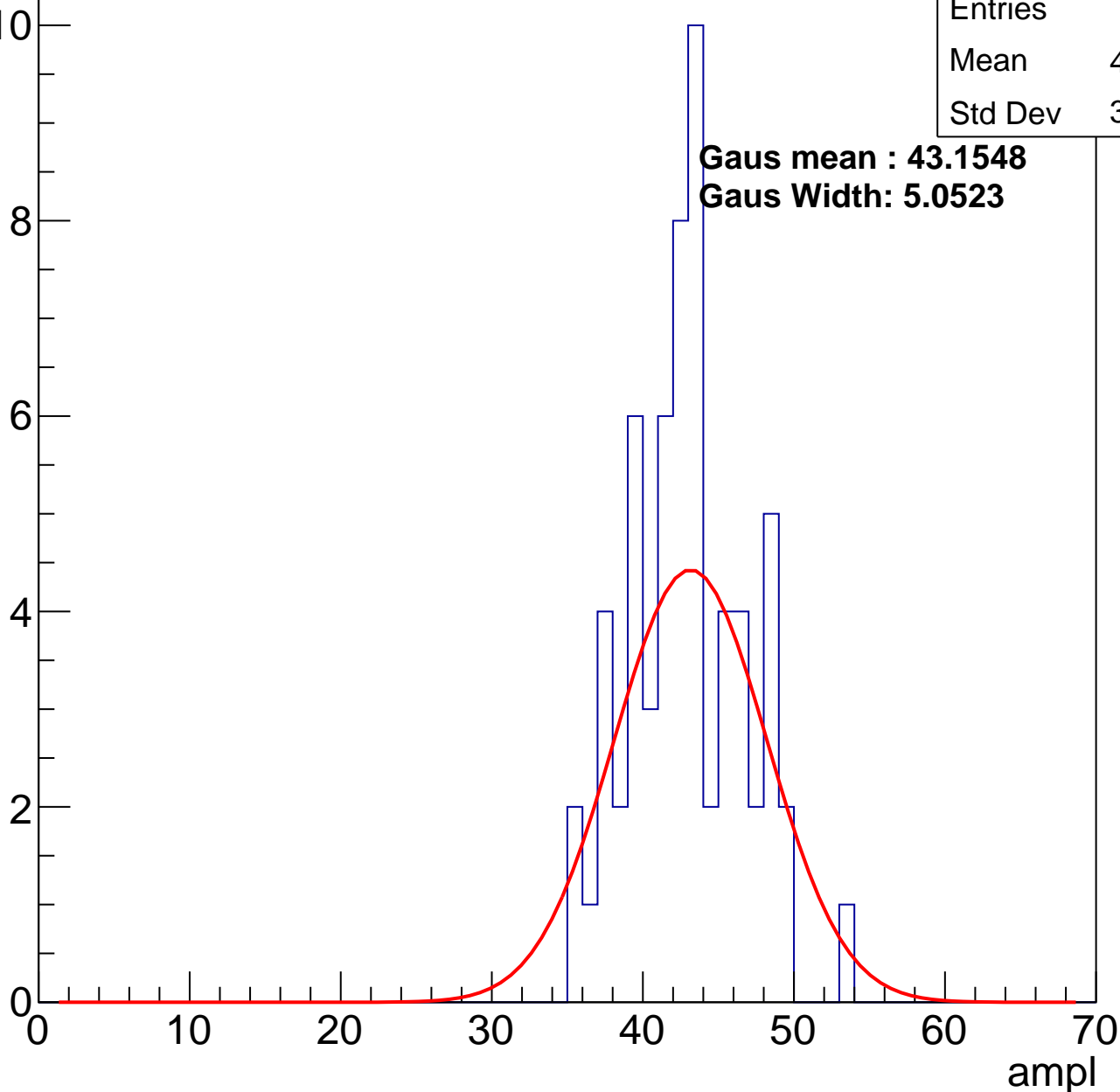
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	42.47
Std Dev	3.792

**Gaus mean : 43.1548**

**Gaus Width: 5.0523**

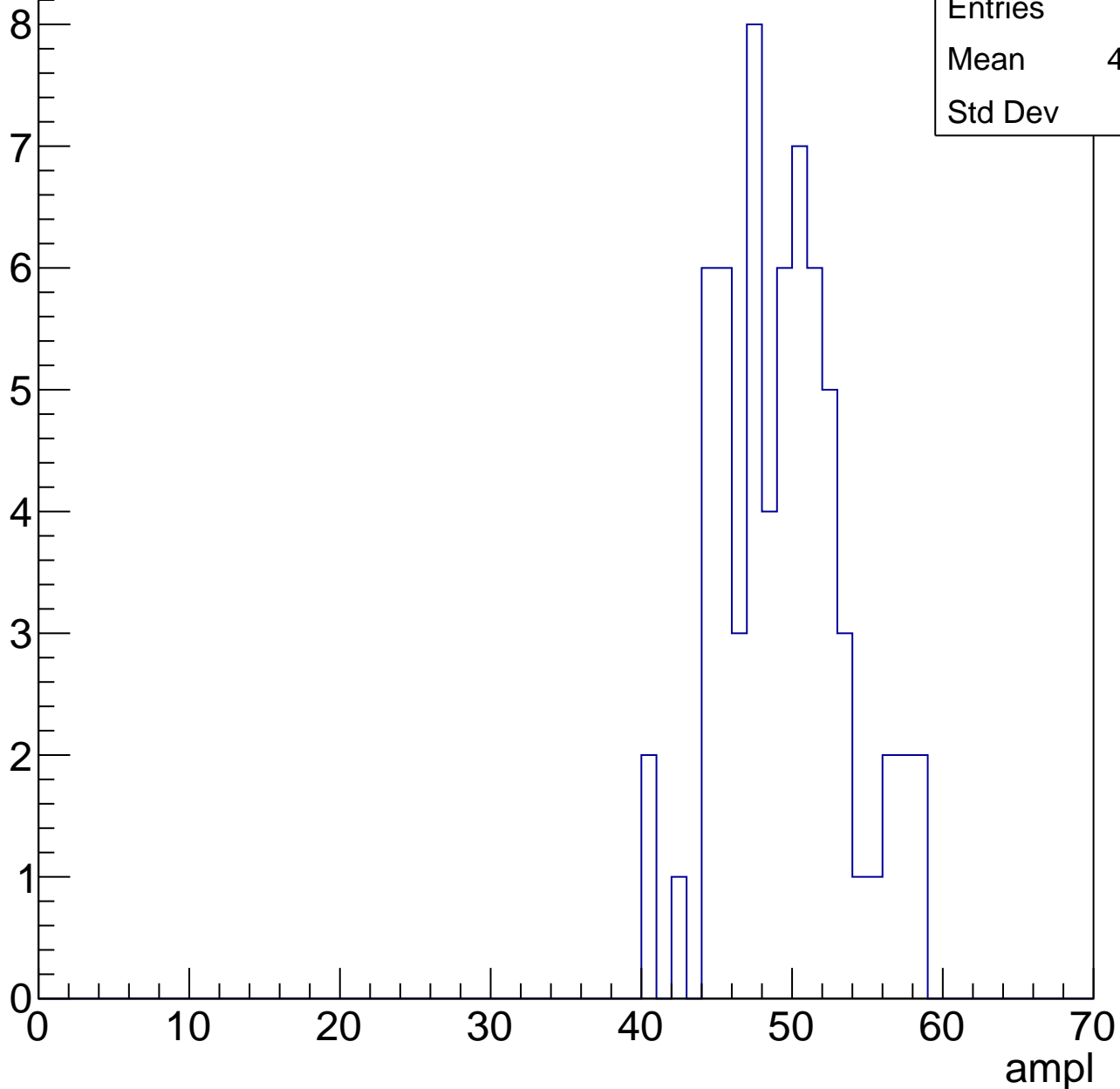


# B1L103S, U21-ch122, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	48.95
Std Dev	4.1

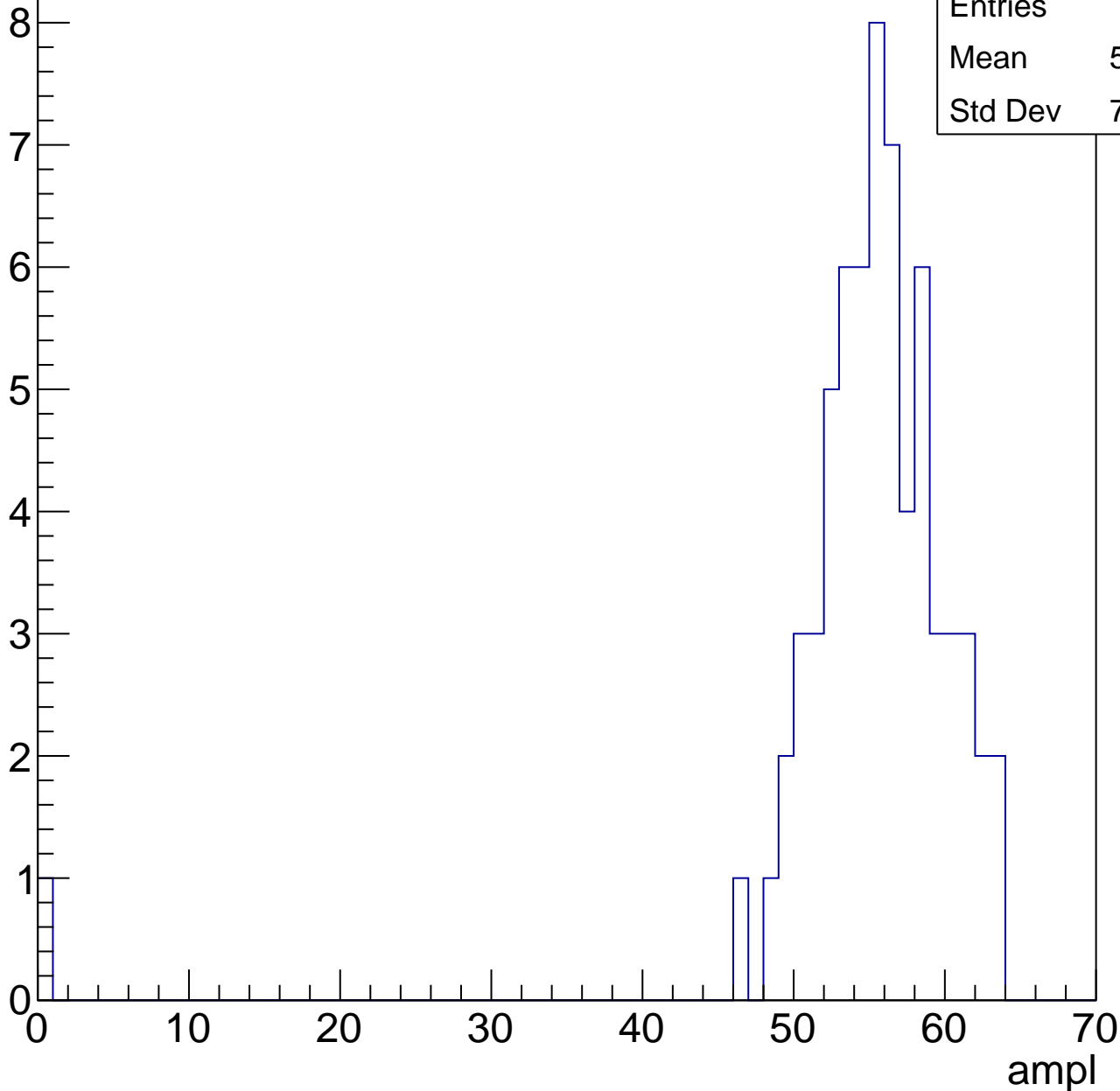


# B1L103S, U21-ch122, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	54.47
Std Dev	7.727

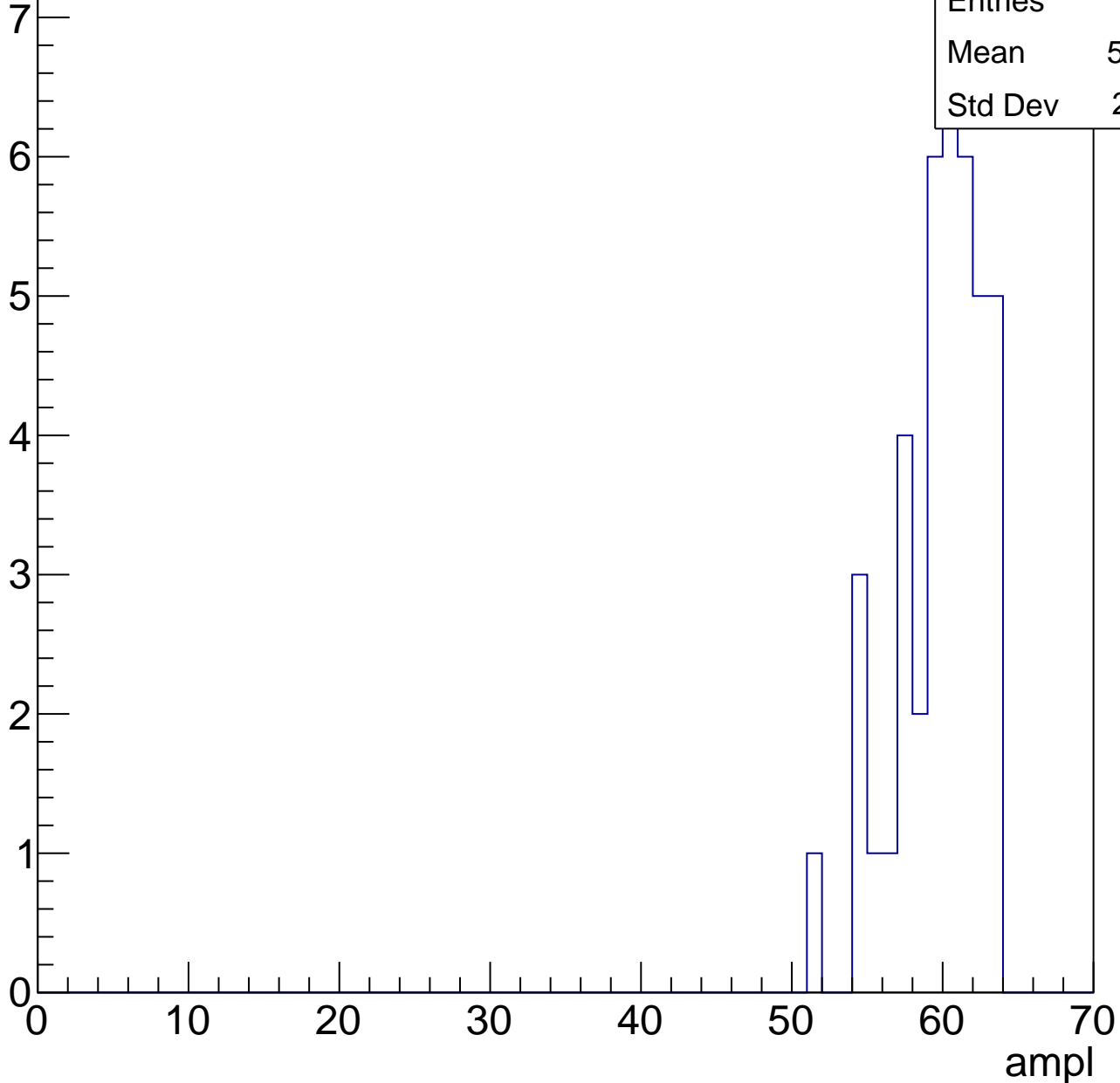


# B1L103S, U21-ch122, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

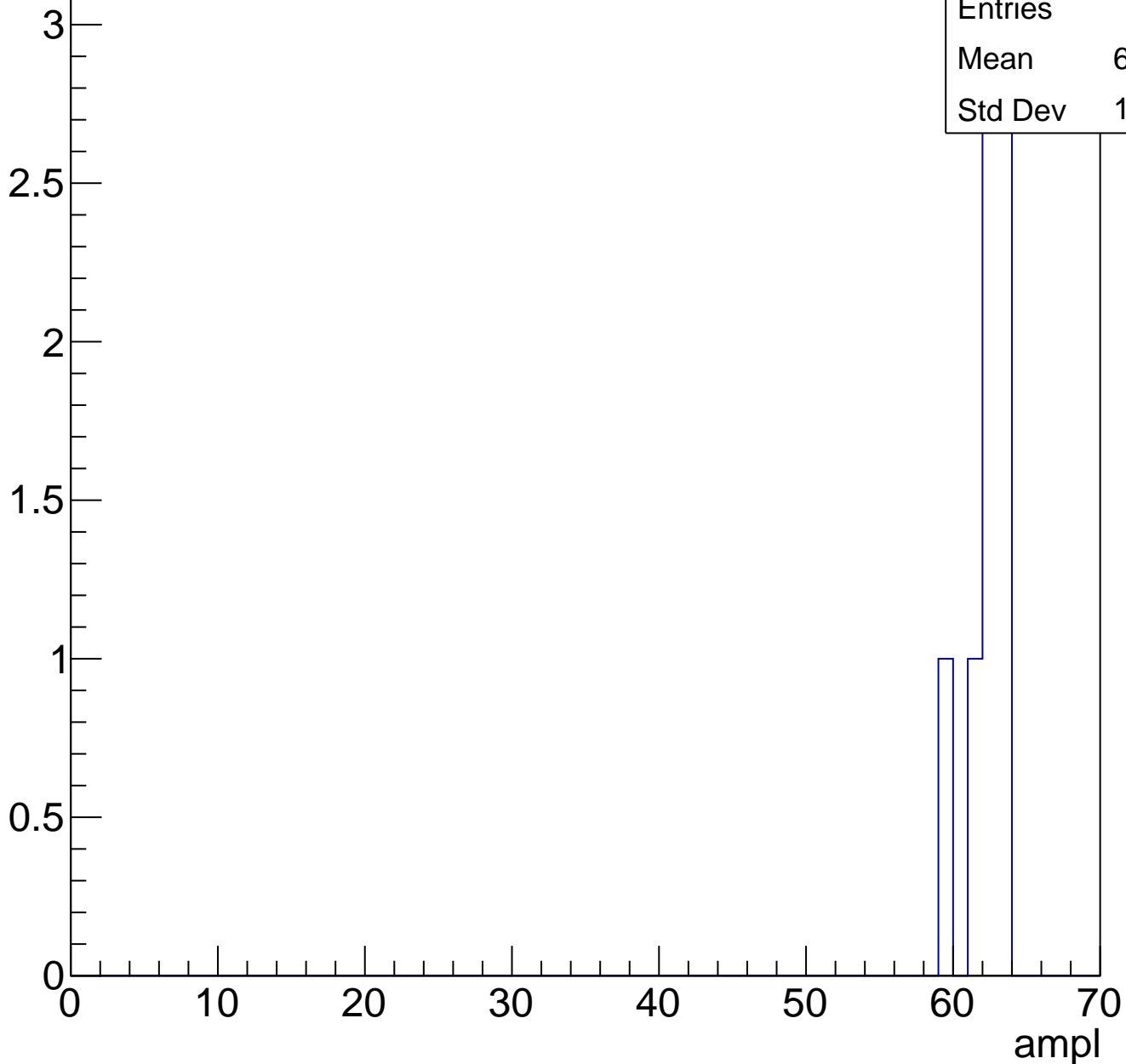
Entries	41
Mean	59.34
Std Dev	2.851



# B1L103S, U21-ch122, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U21-ch122, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	10
Std Dev	10

# B1L103S, U21-ch123, adc0

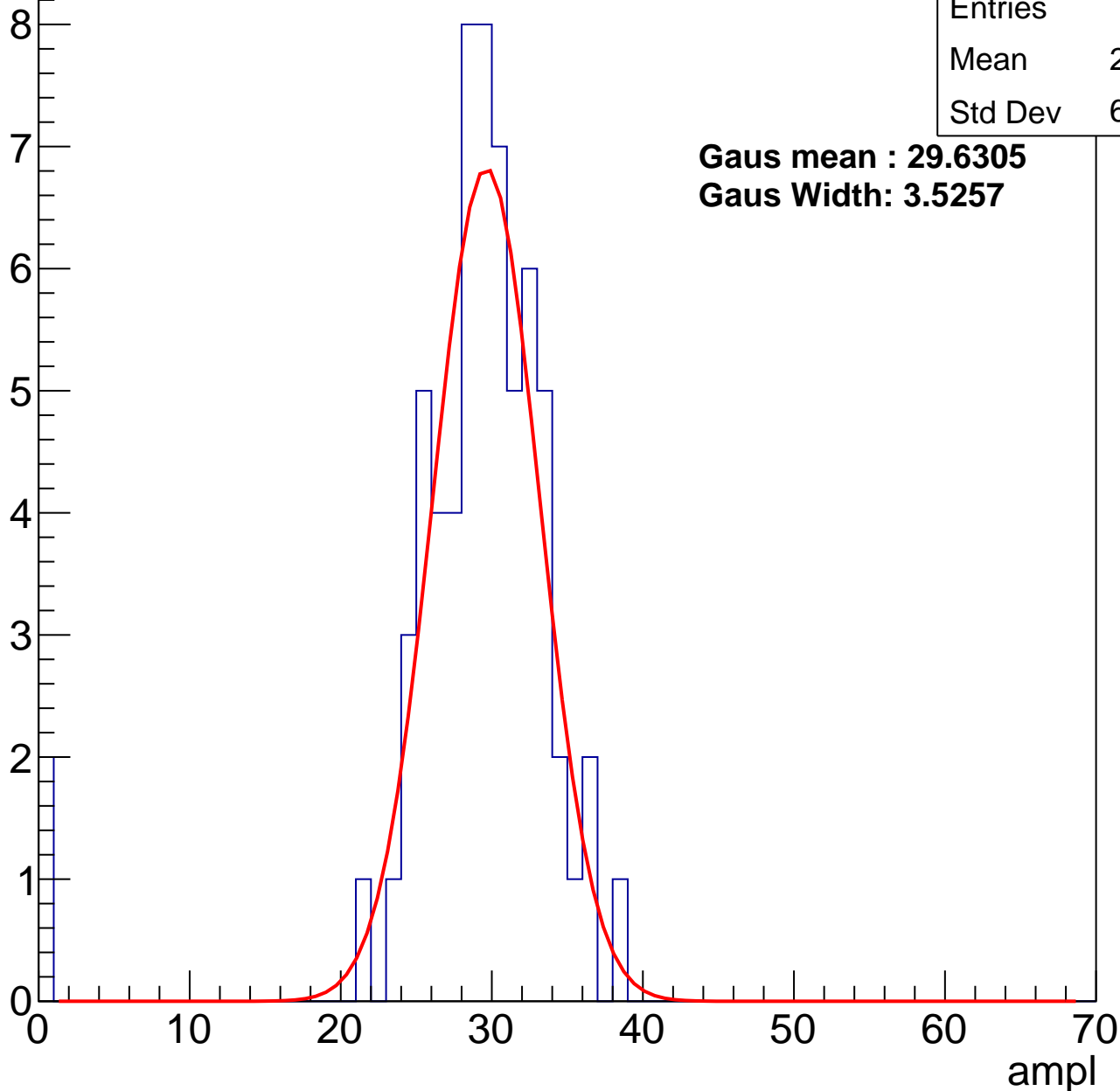
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	28.37
Std Dev	6.073

**Gaus mean : 29.6305**

**Gaus Width: 3.5257**



# B1L103S, U21-ch123, adc1

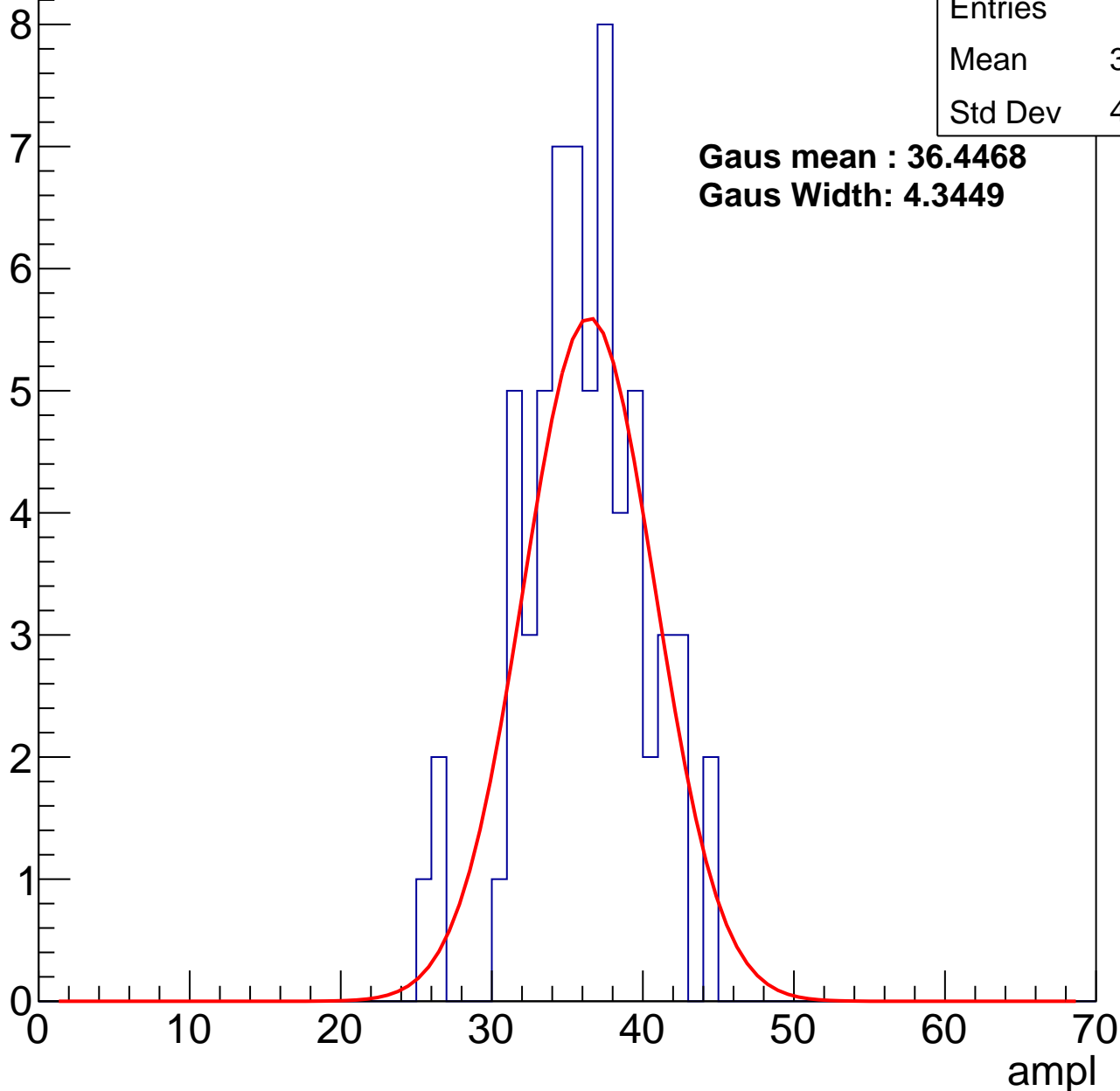
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	35.65
Std Dev	4.013

**Gaus mean : 36.4468**

**Gaus Width: 4.3449**



# B1L103S, U21-ch123, adc2

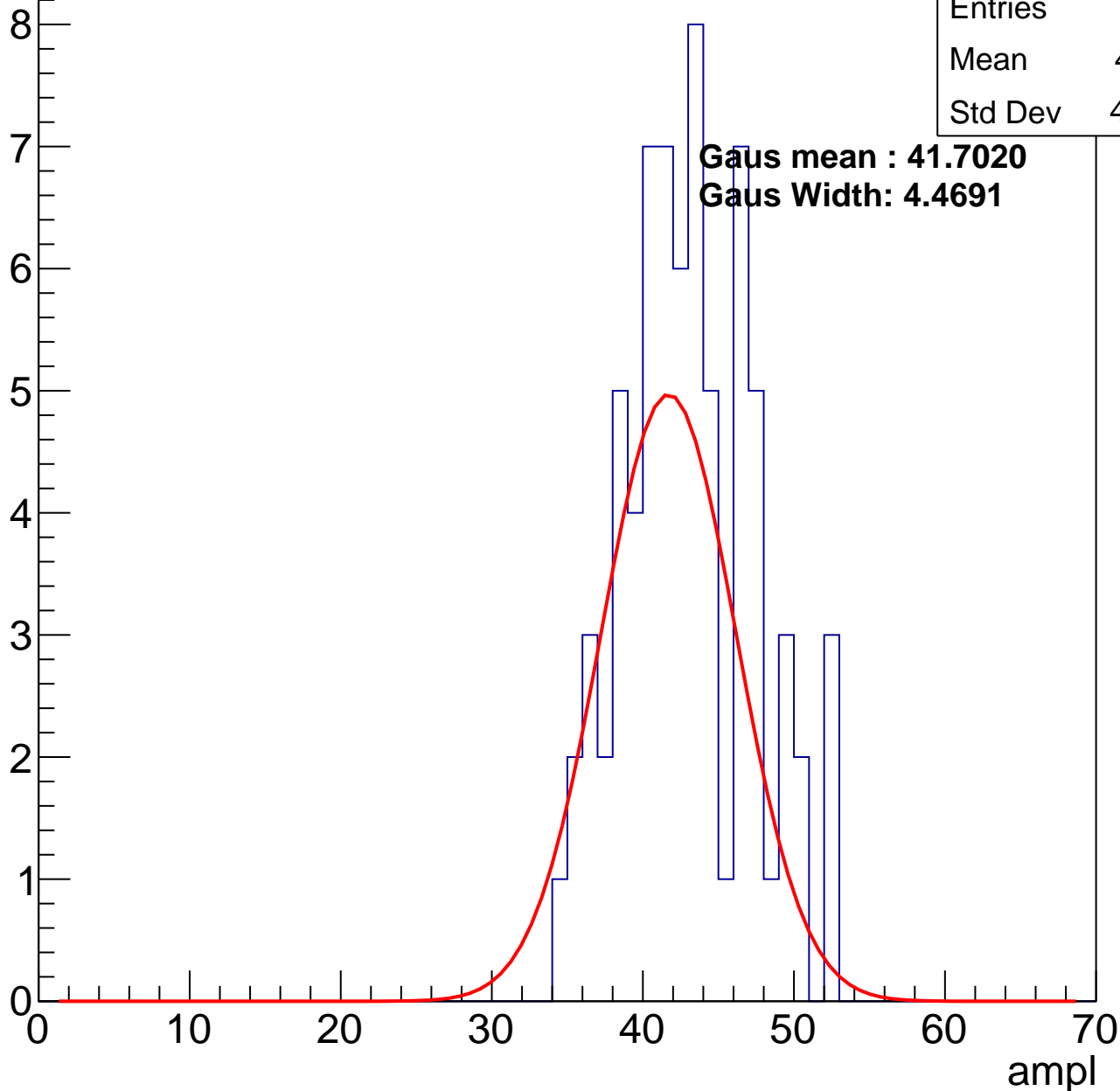
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	42.61
Std Dev	4.296

**Gaus mean : 41.7020**

**Gaus Width: 4.4691**



# B1L103S, U21-ch123, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

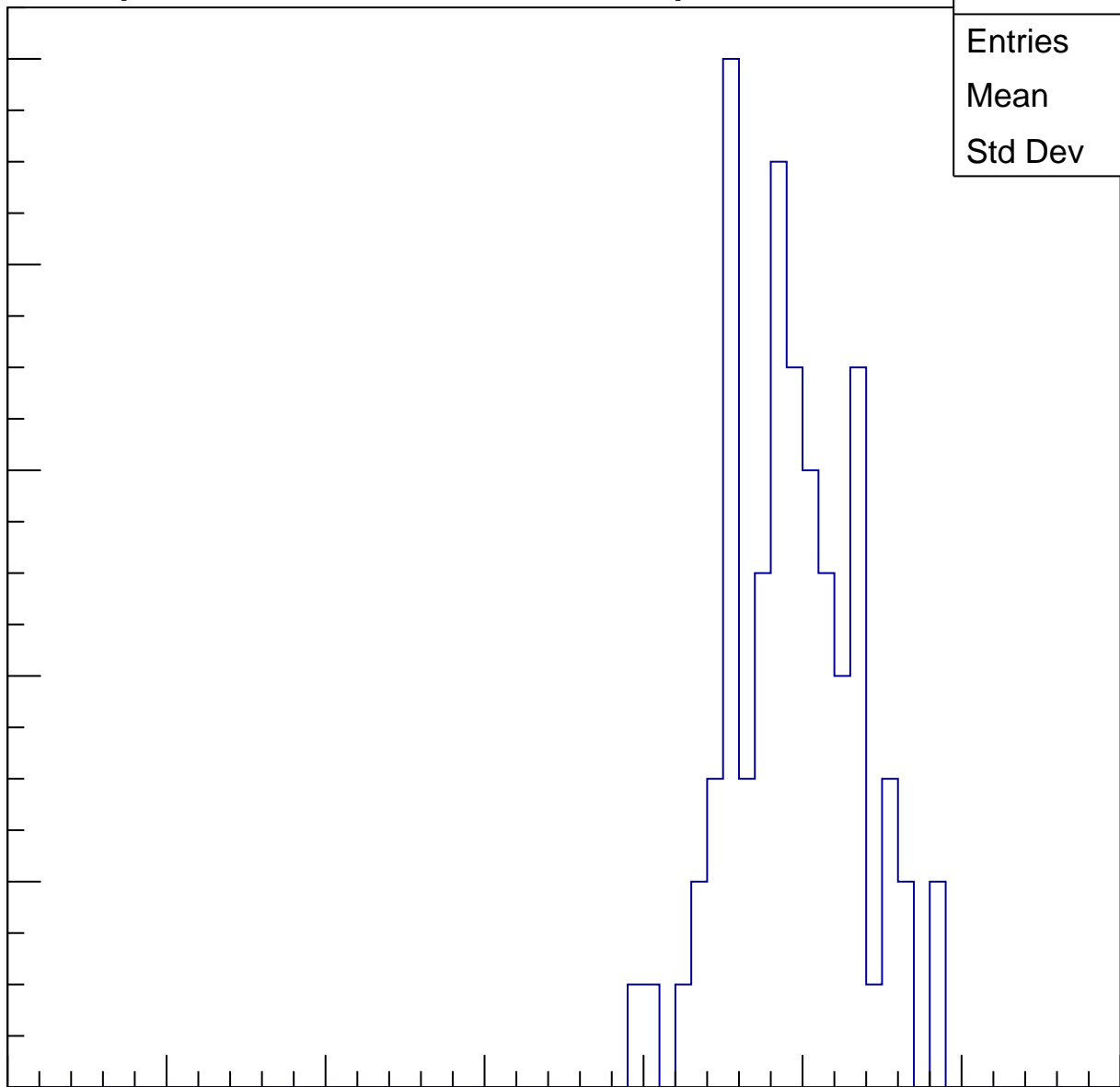
Entries	72
Mean	48.86
Std Dev	4.011

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

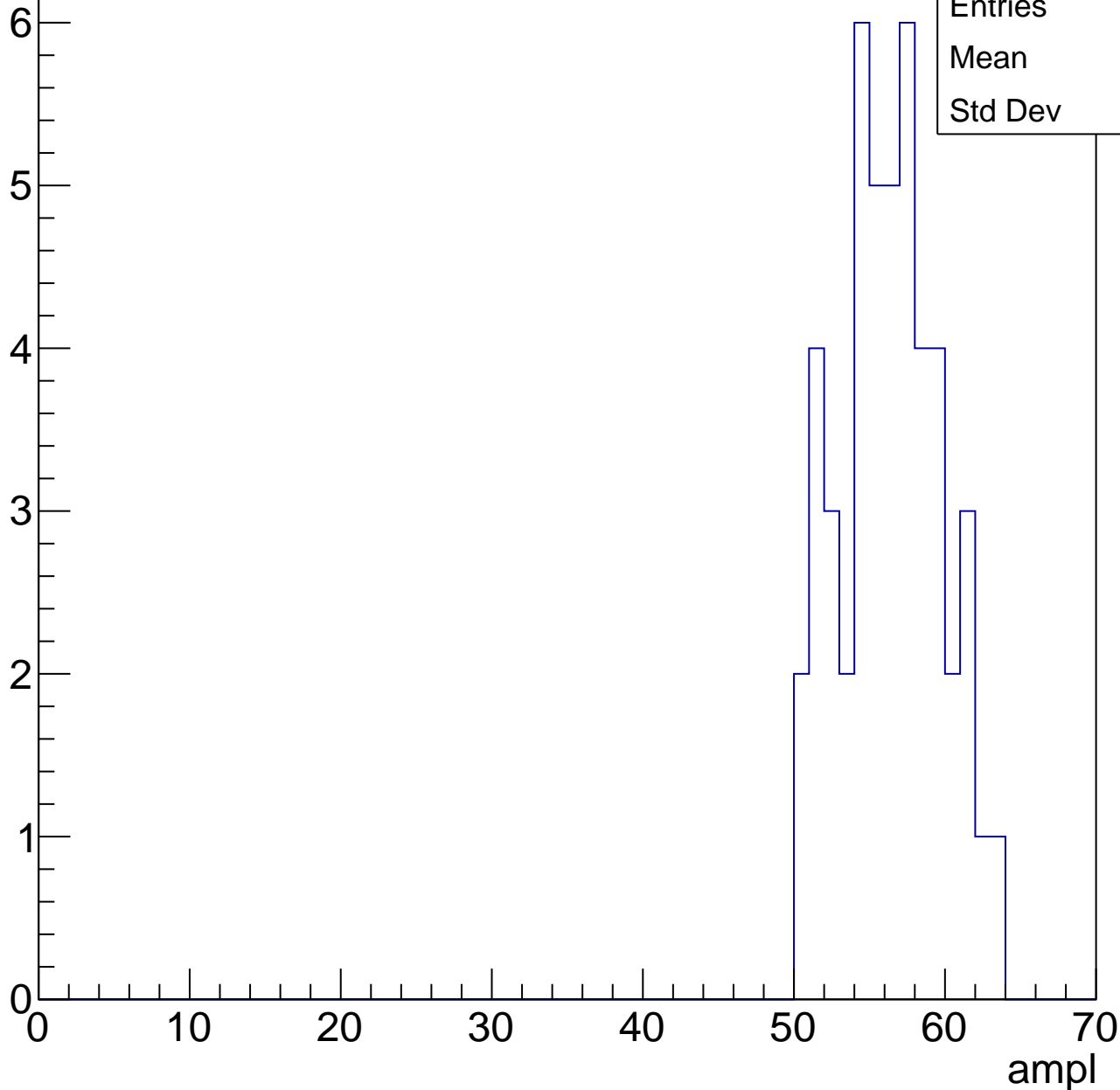


# B1L103S, U21-ch123, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	48
Mean	55.9
Std Dev	3.28

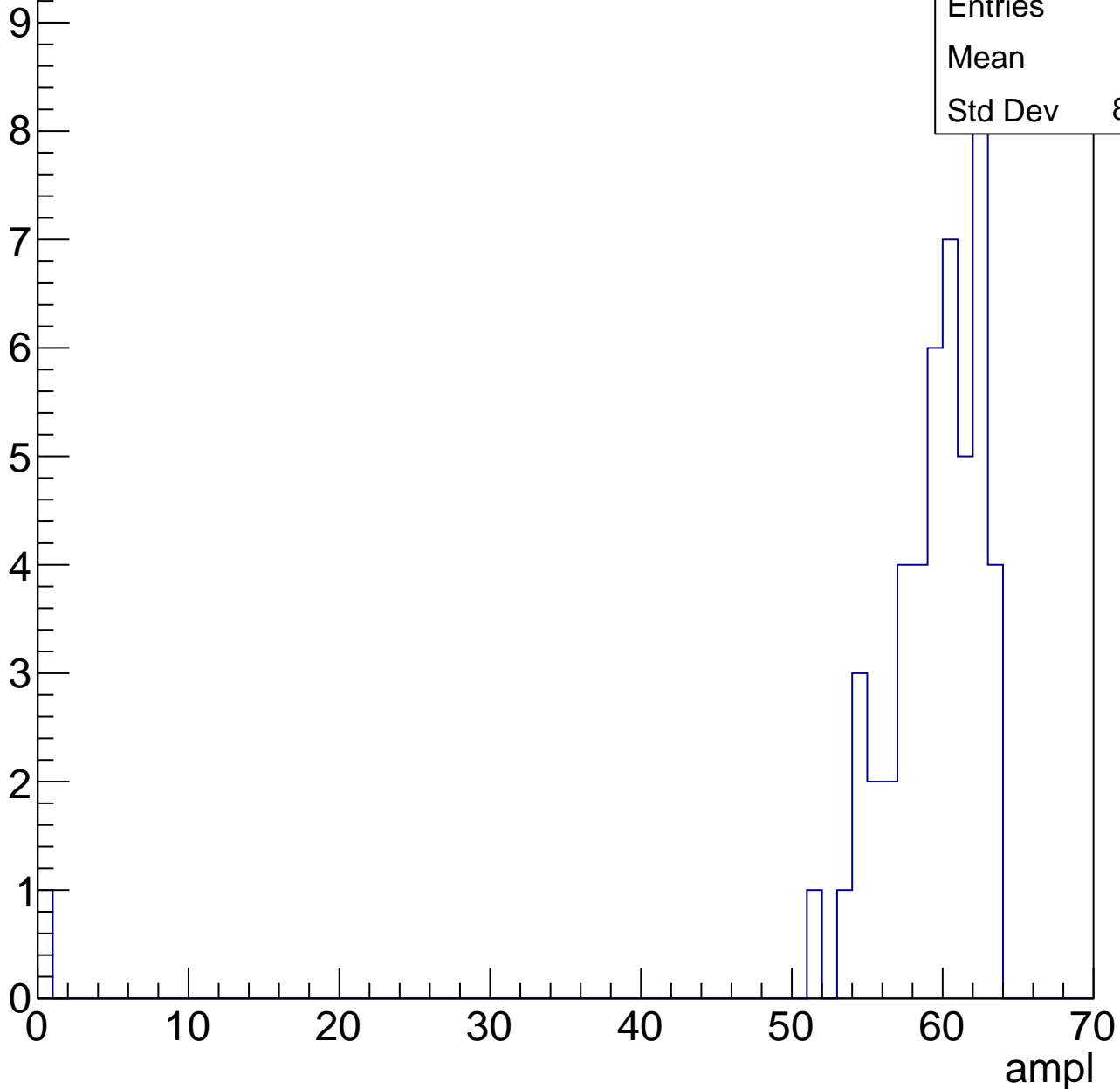


# B1L103S, U21-ch123, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

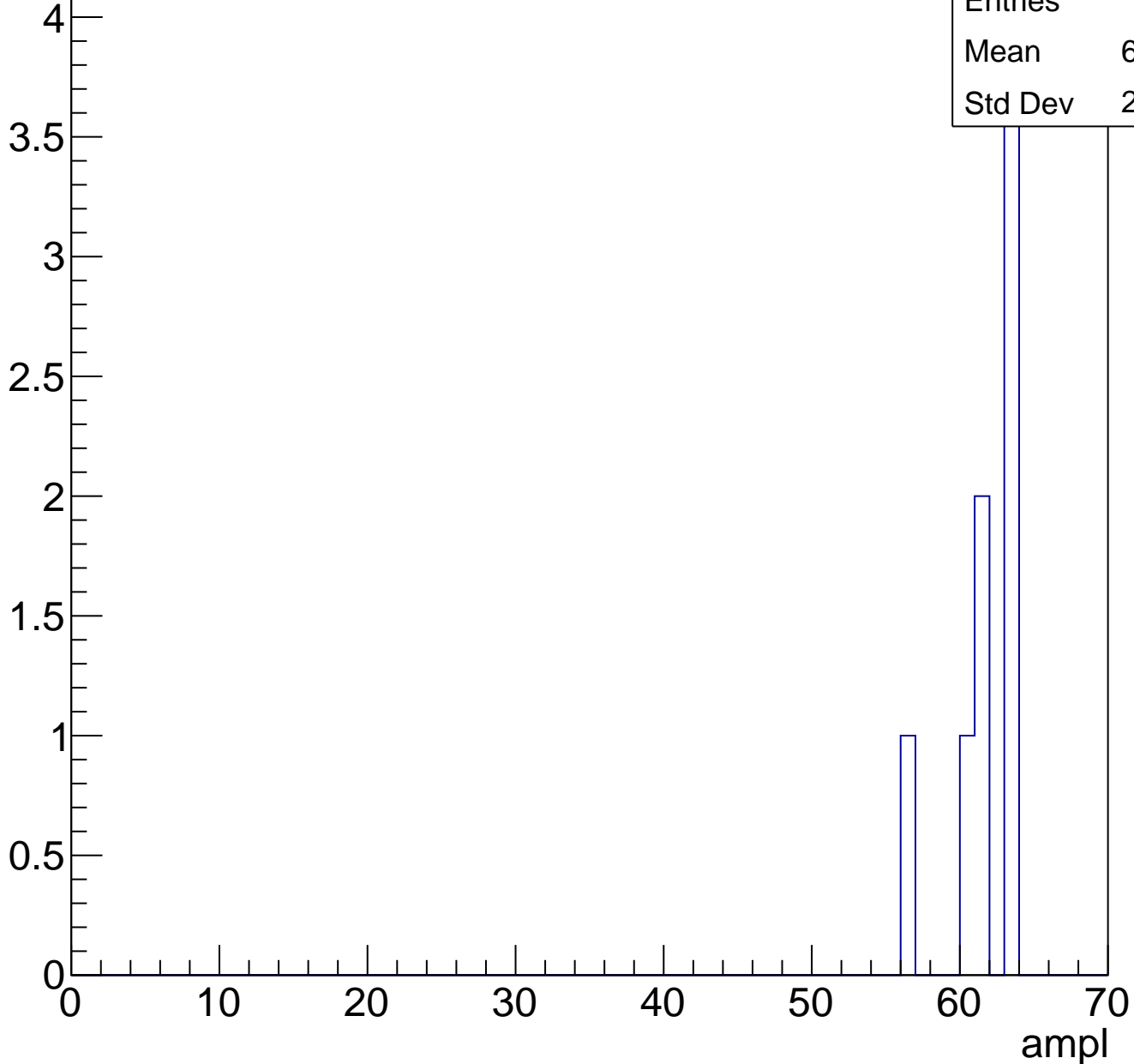
Entries	49
Mean	57.9
Std Dev	8.851



# B1L103S, U21-ch123, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

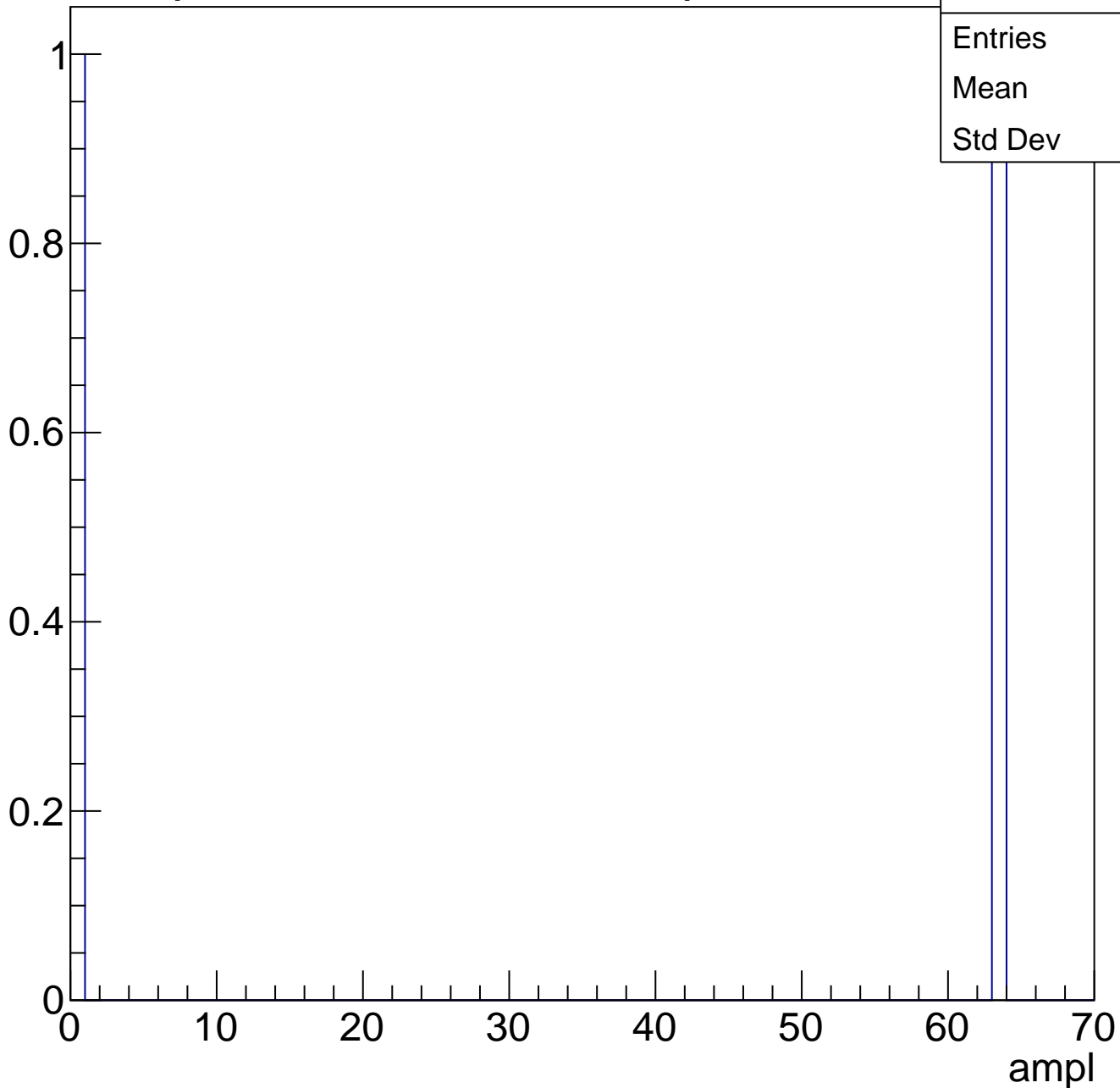




# B1L103S, U21-ch123, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	31.5
Std Dev	31.5

# B1L103S, U21-ch124, adc0

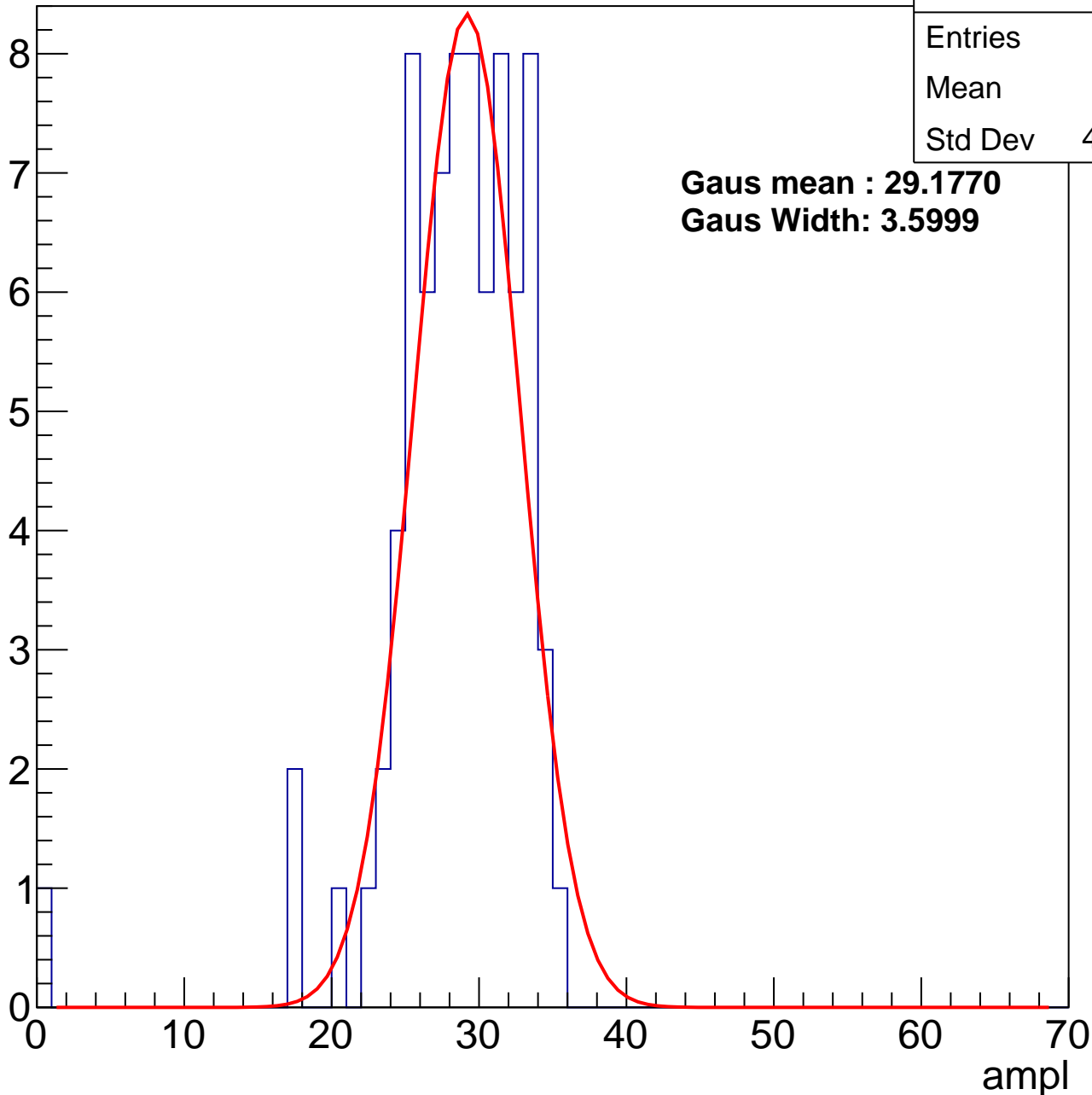
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	80
Mean	28
Std Dev	4.873

**Gaus mean : 29.1770**

**Gaus Width: 3.5999**



# B1L103S, U21-ch124, adc1

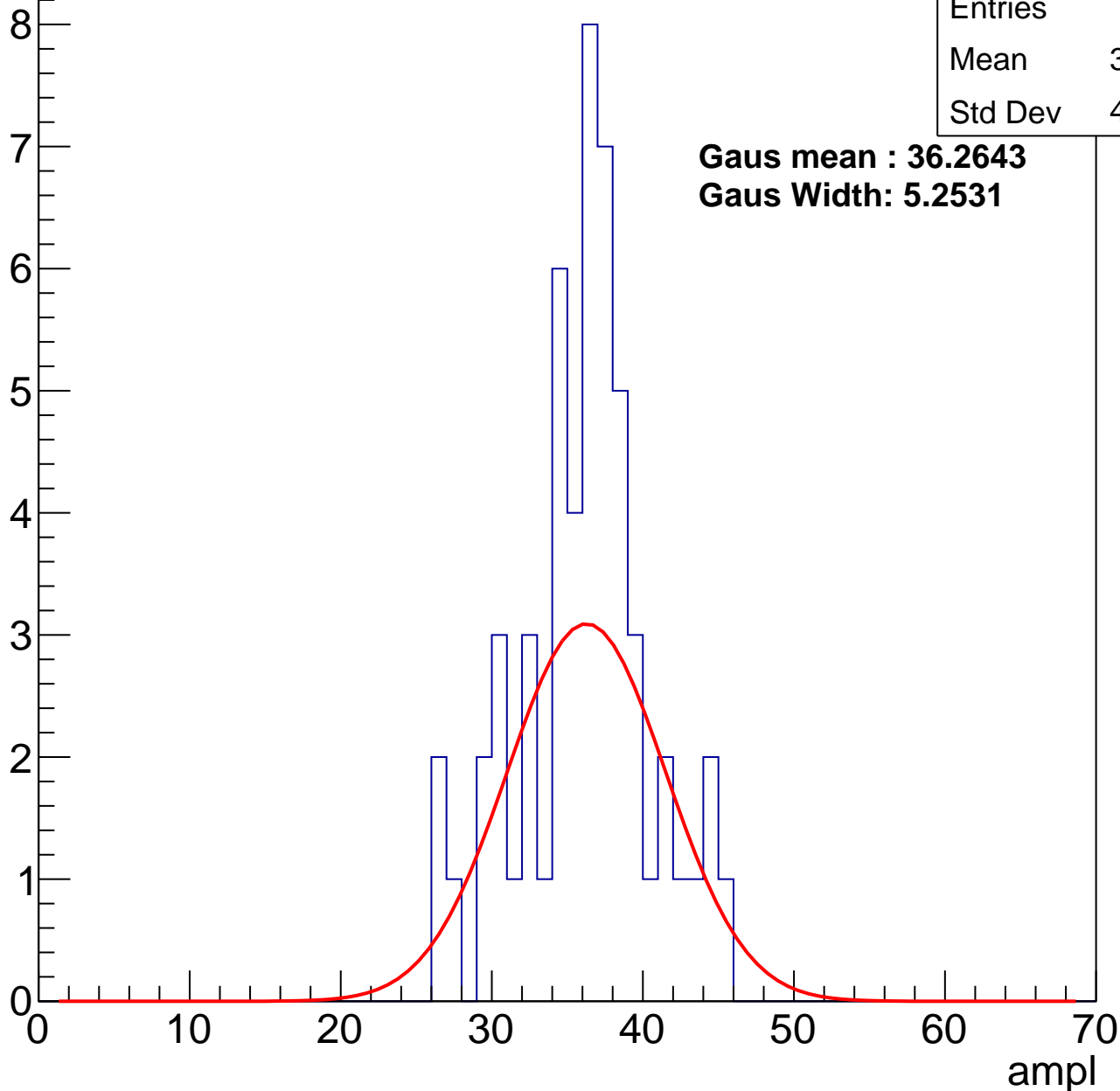
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	35.65
Std Dev	4.313

**Gaus mean : 36.2643**

**Gaus Width: 5.2531**



# B1L103S, U21-ch124, adc2

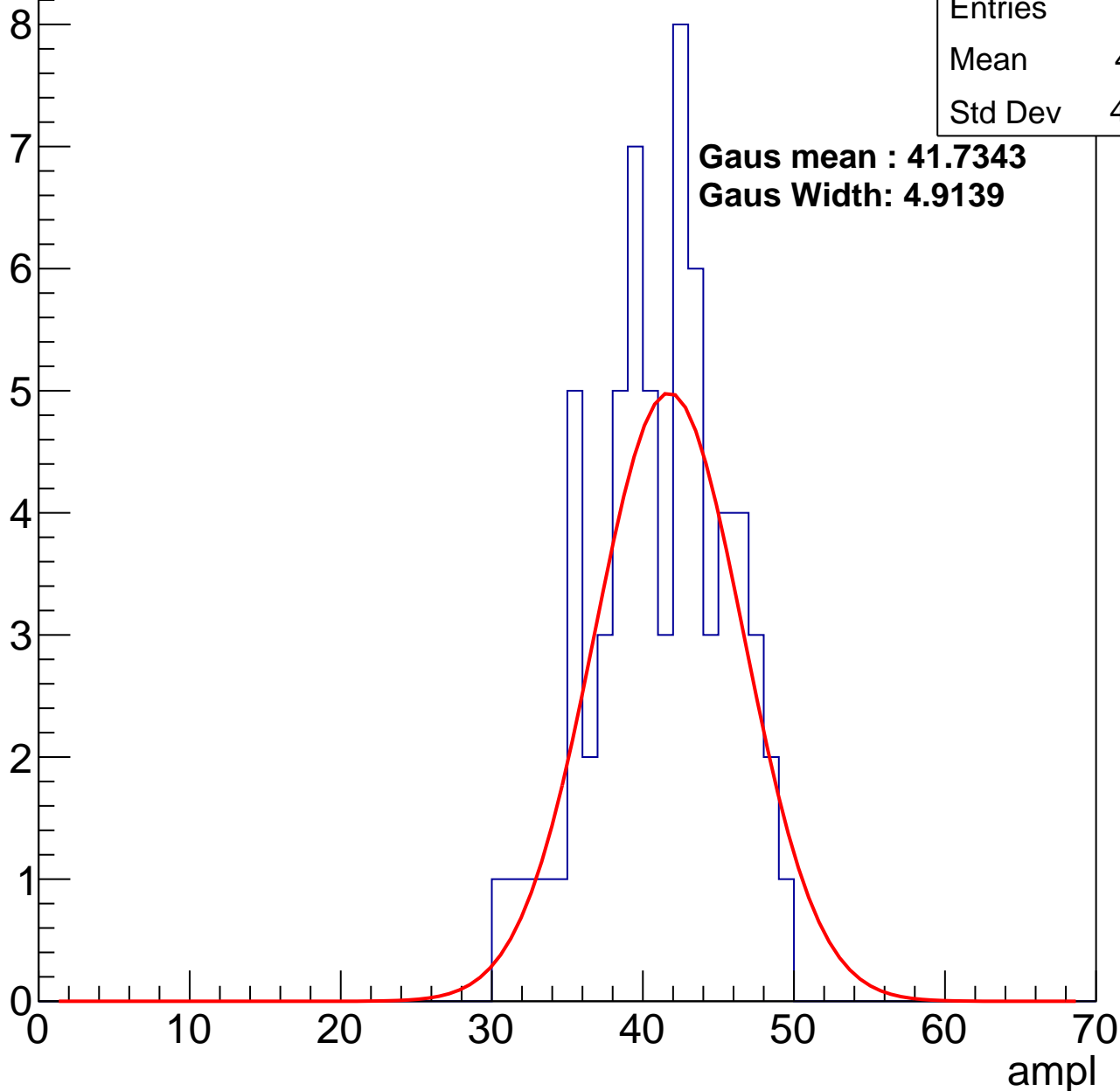
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	40.61
Std Dev	4.358

**Gaus mean : 41.7343**

**Gaus Width: 4.9139**

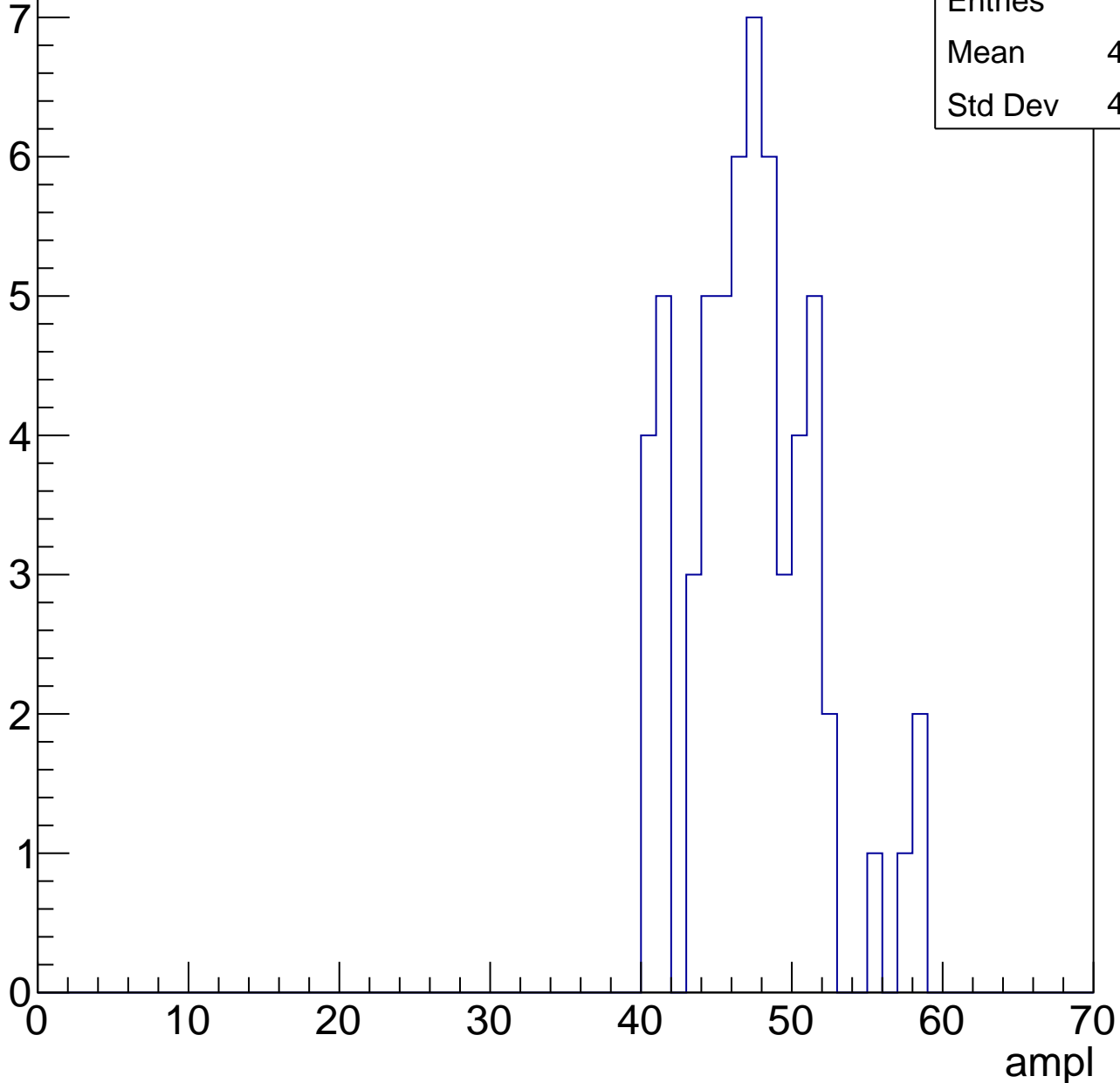


# B1L103S, U21-ch124, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	46.88
Std Dev	4.287

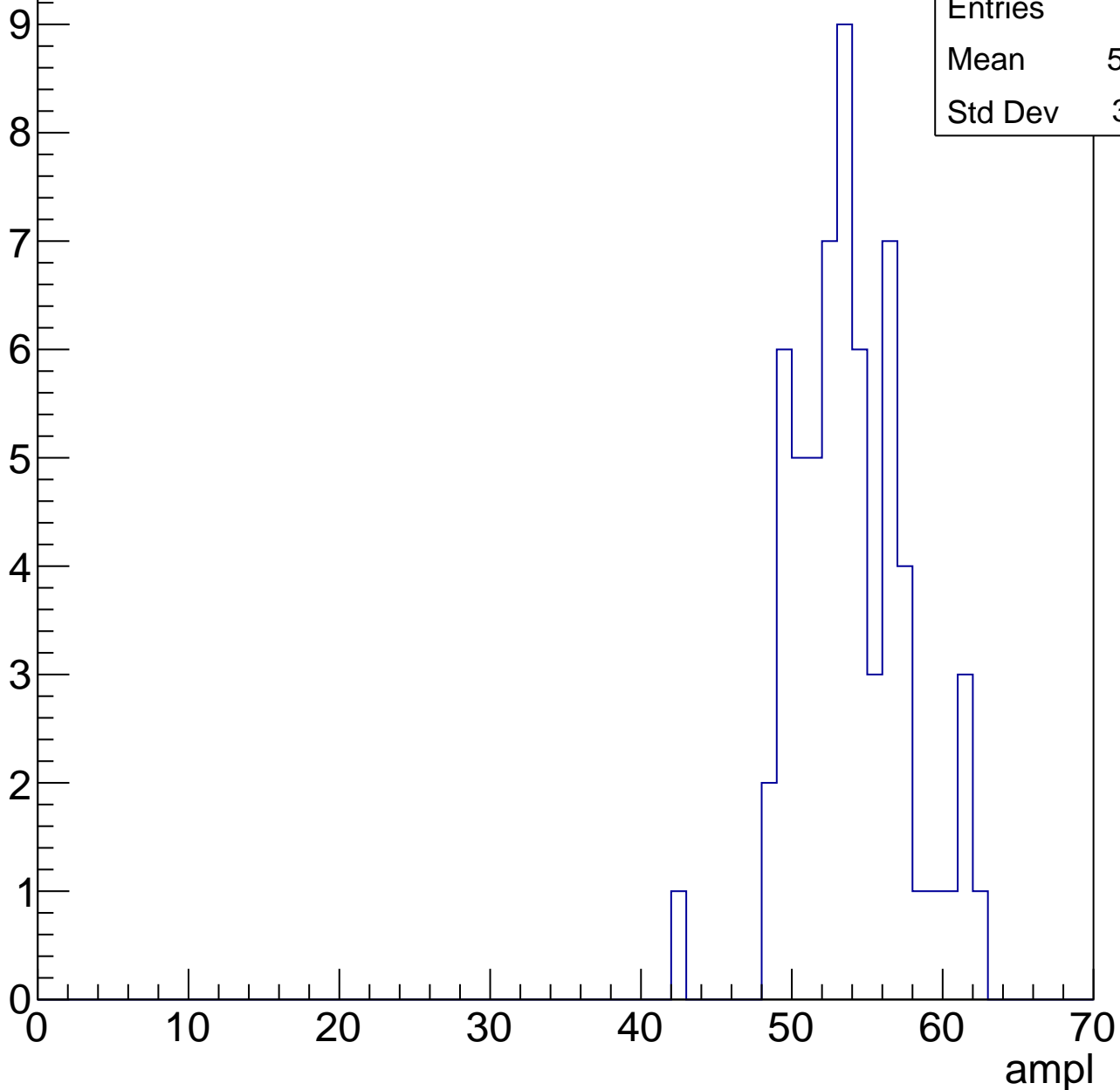


# B1L103S, U21-ch124, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	53.37
Std Dev	3.721

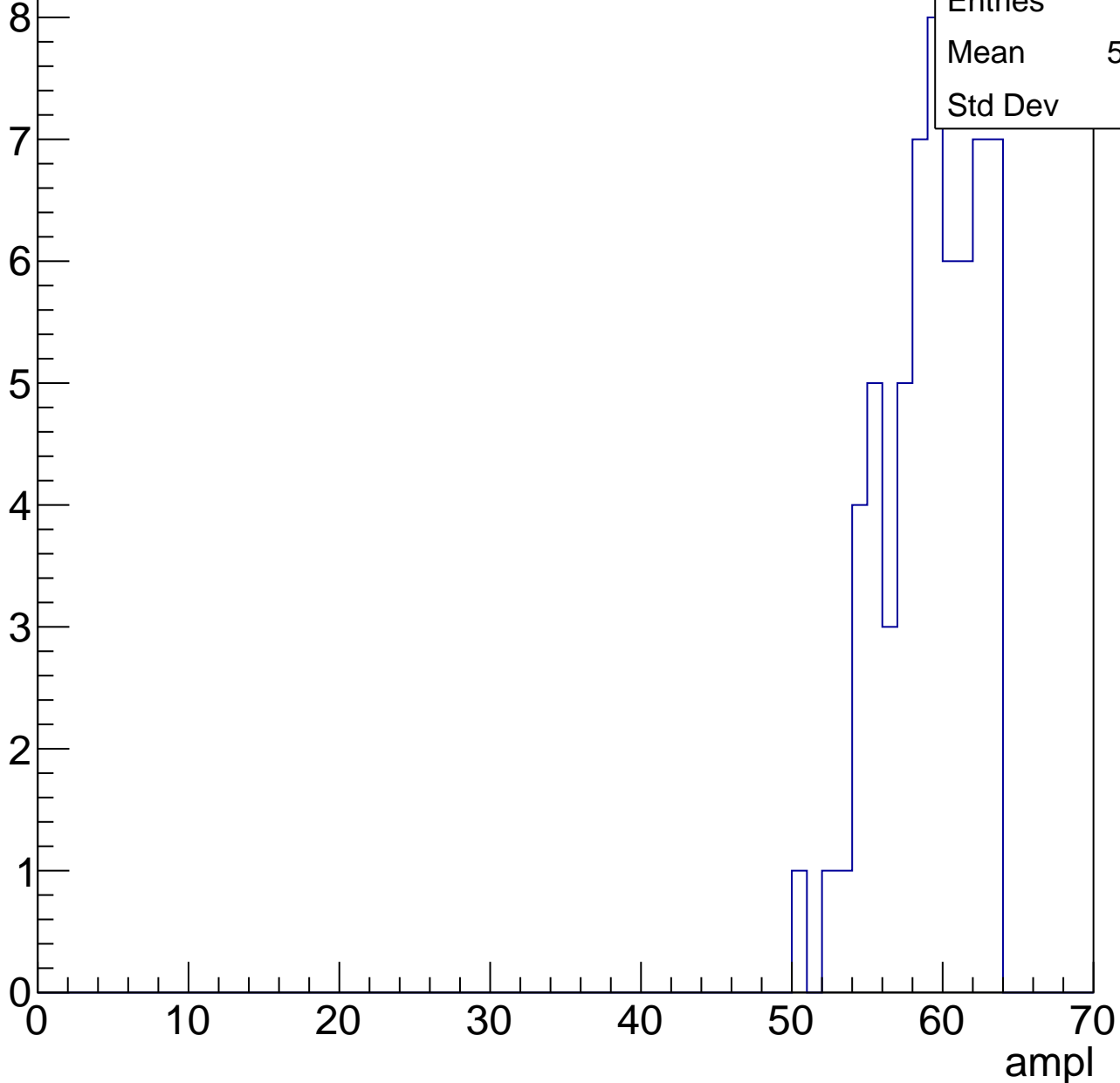


# B1L103S, U21-ch124, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	58.66
Std Dev	3.13



# B1L103S, U21-ch124, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

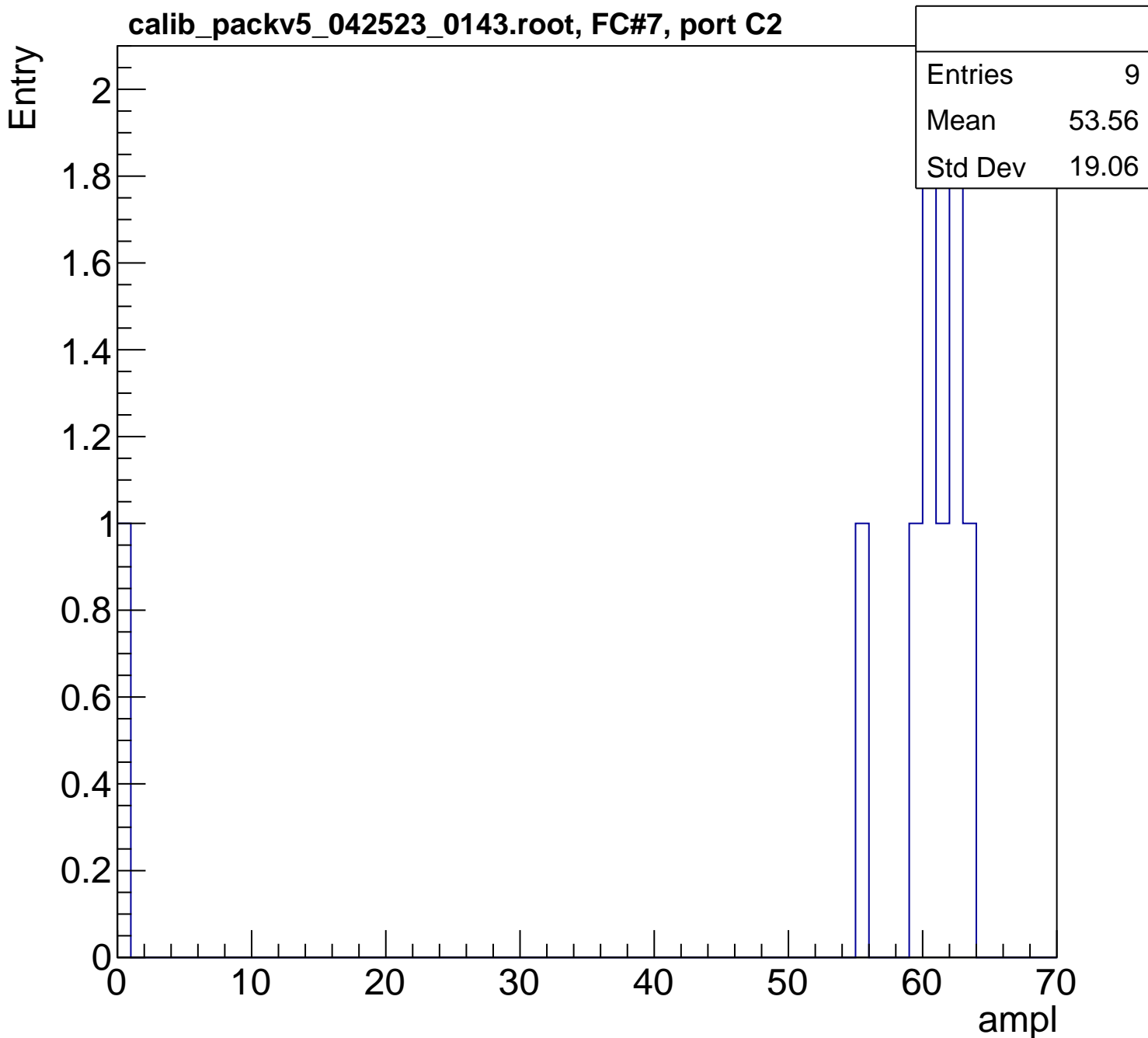
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	9
Mean	53.56
Std Dev	19.06

0 10 20 30 40 50 60 70

ampl

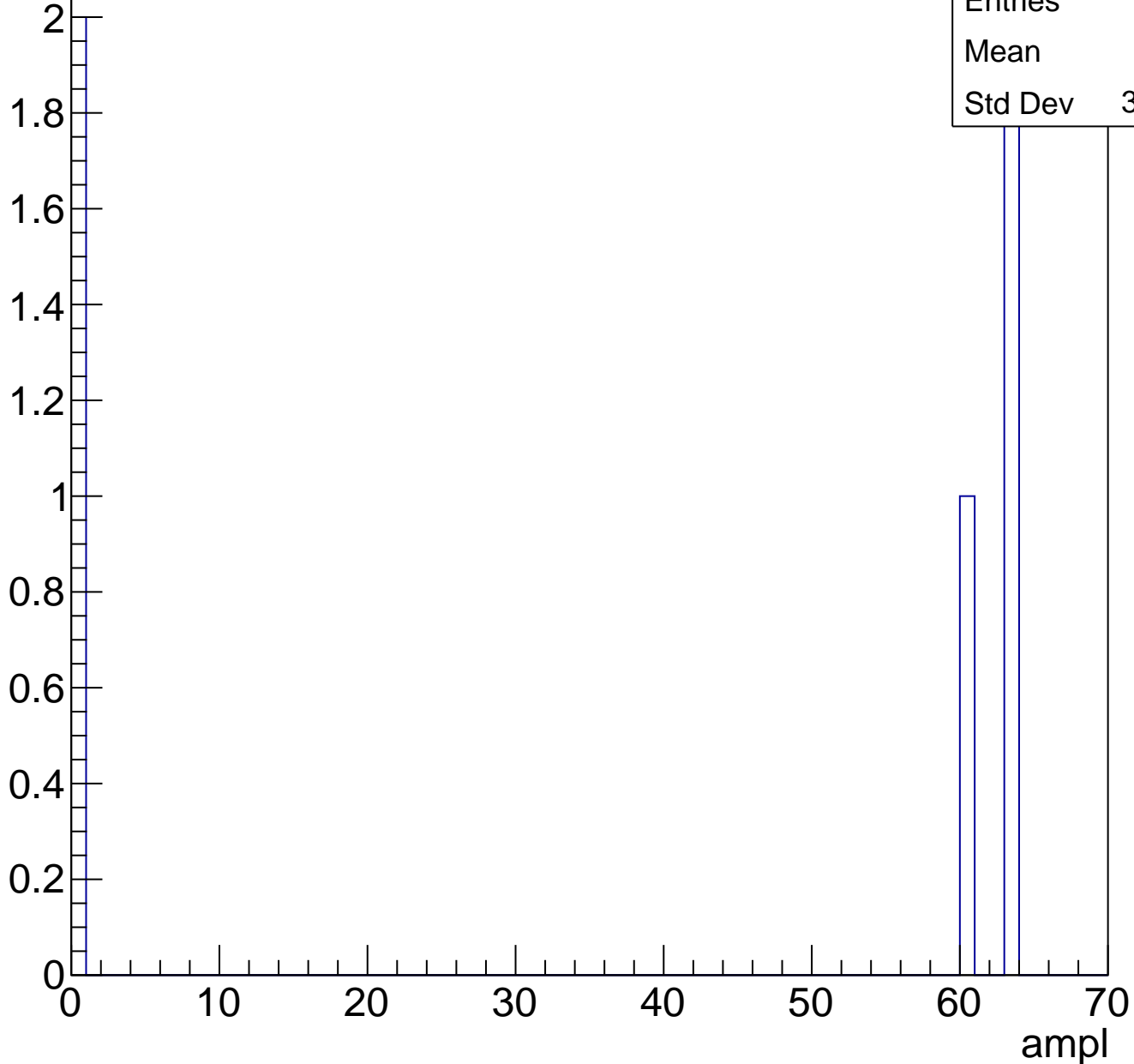




# B1L103S, U21-ch124, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U21-ch125, adc0

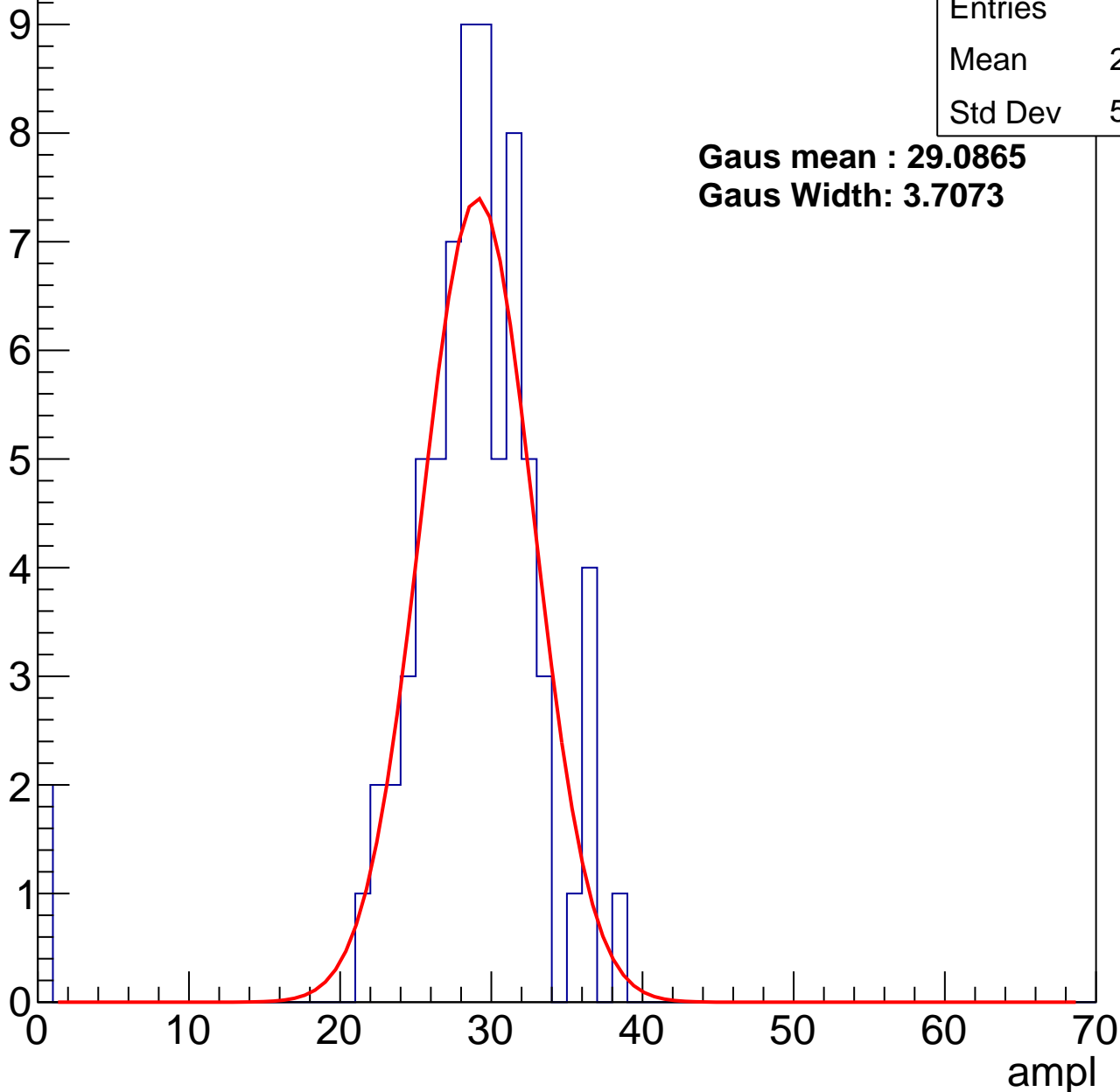
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	27.97
Std Dev	5.916

**Gaus mean : 29.0865**

**Gaus Width: 3.7073**



# B1L103S, U21-ch125, adc1

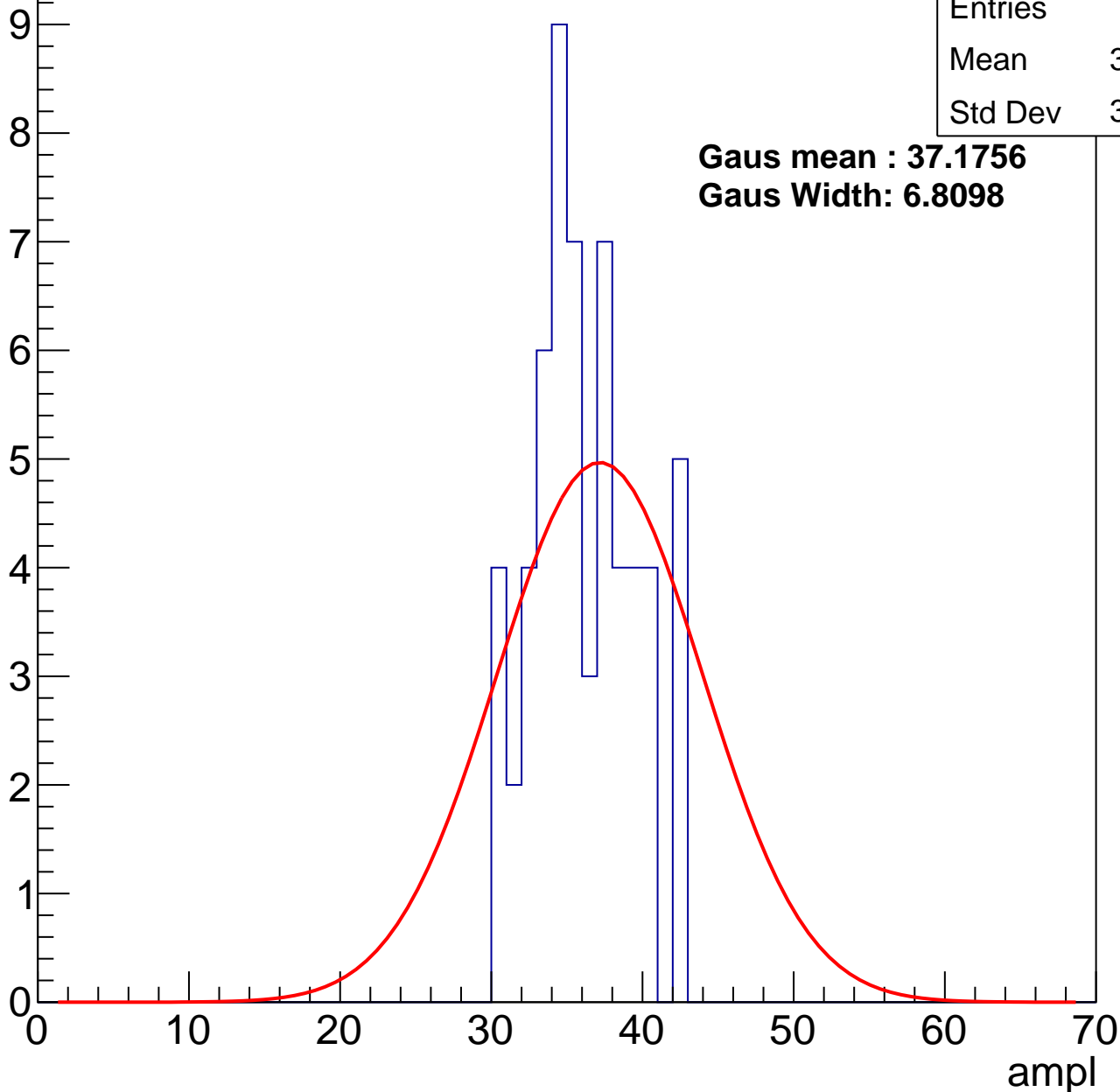
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	35.66
Std Dev	3.322

**Gaus mean : 37.1756**

**Gaus Width: 6.8098**



# B1L103S, U21-ch125, adc2

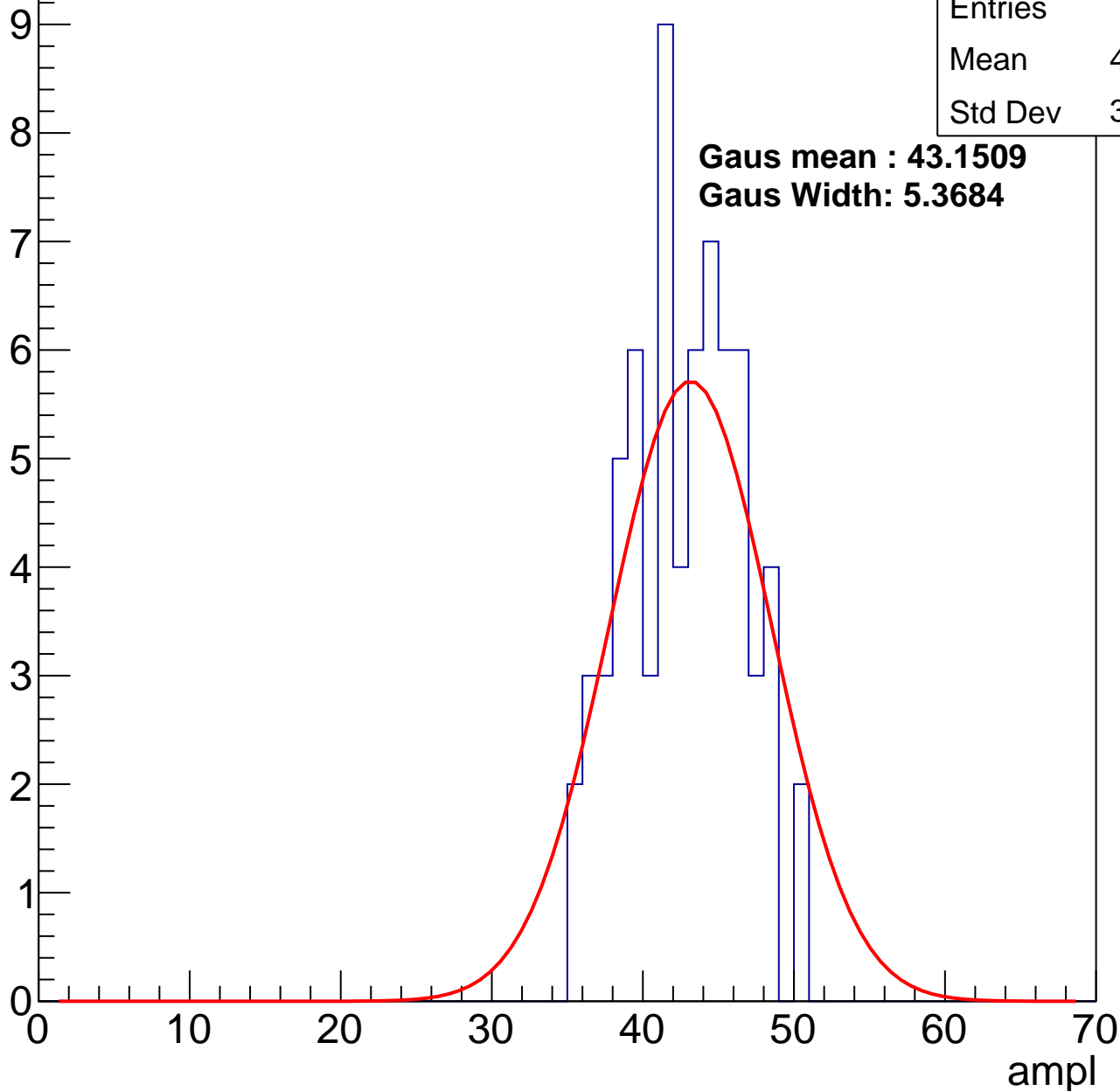
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	42.25
Std Dev	3.735

**Gaus mean : 43.1509**

**Gaus Width: 5.3684**

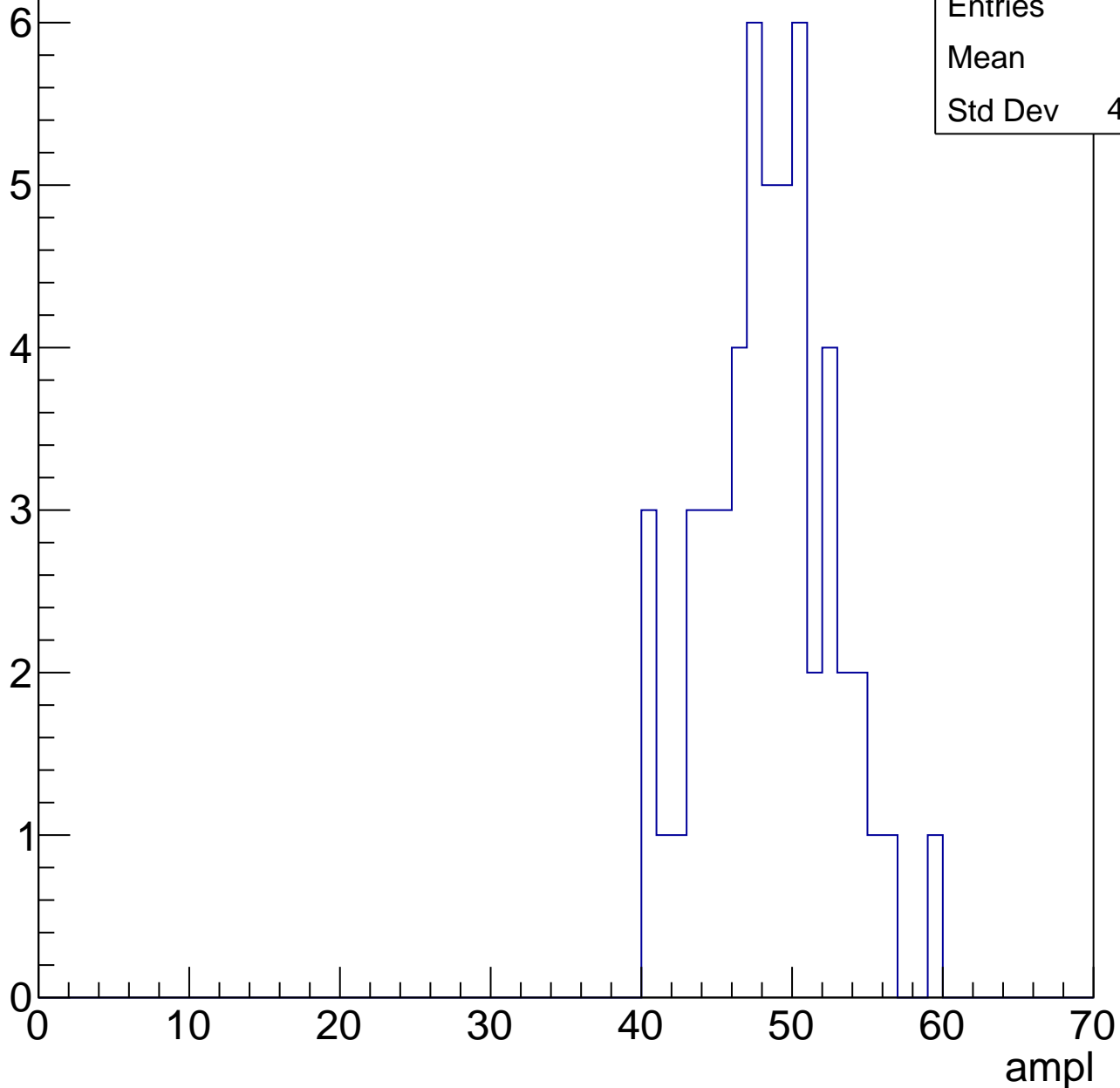


# B1L103S, U21-ch125, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	48
Std Dev	4.157

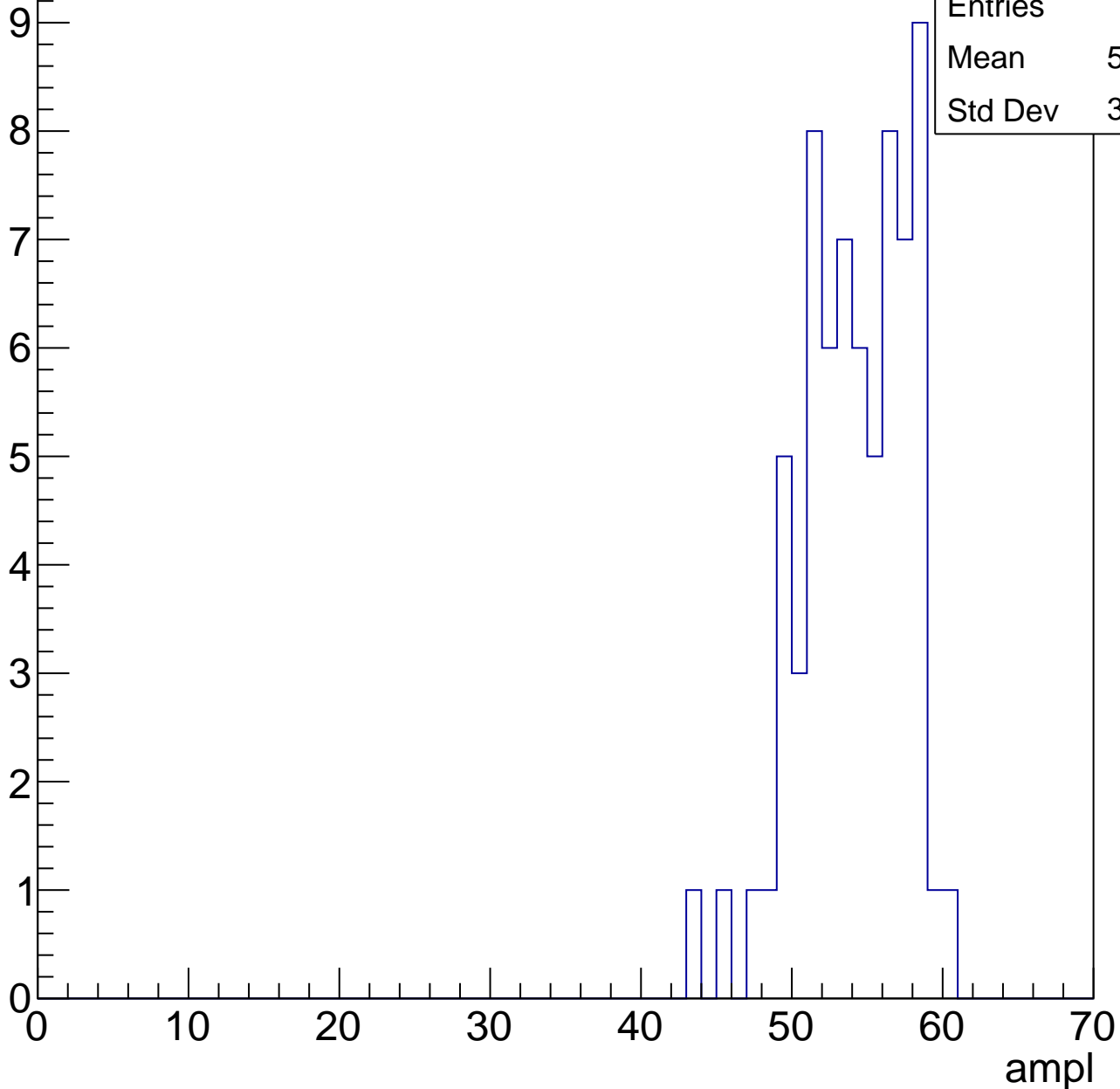


# B1L103S, U21-ch125, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	53.66
Std Dev	3.505

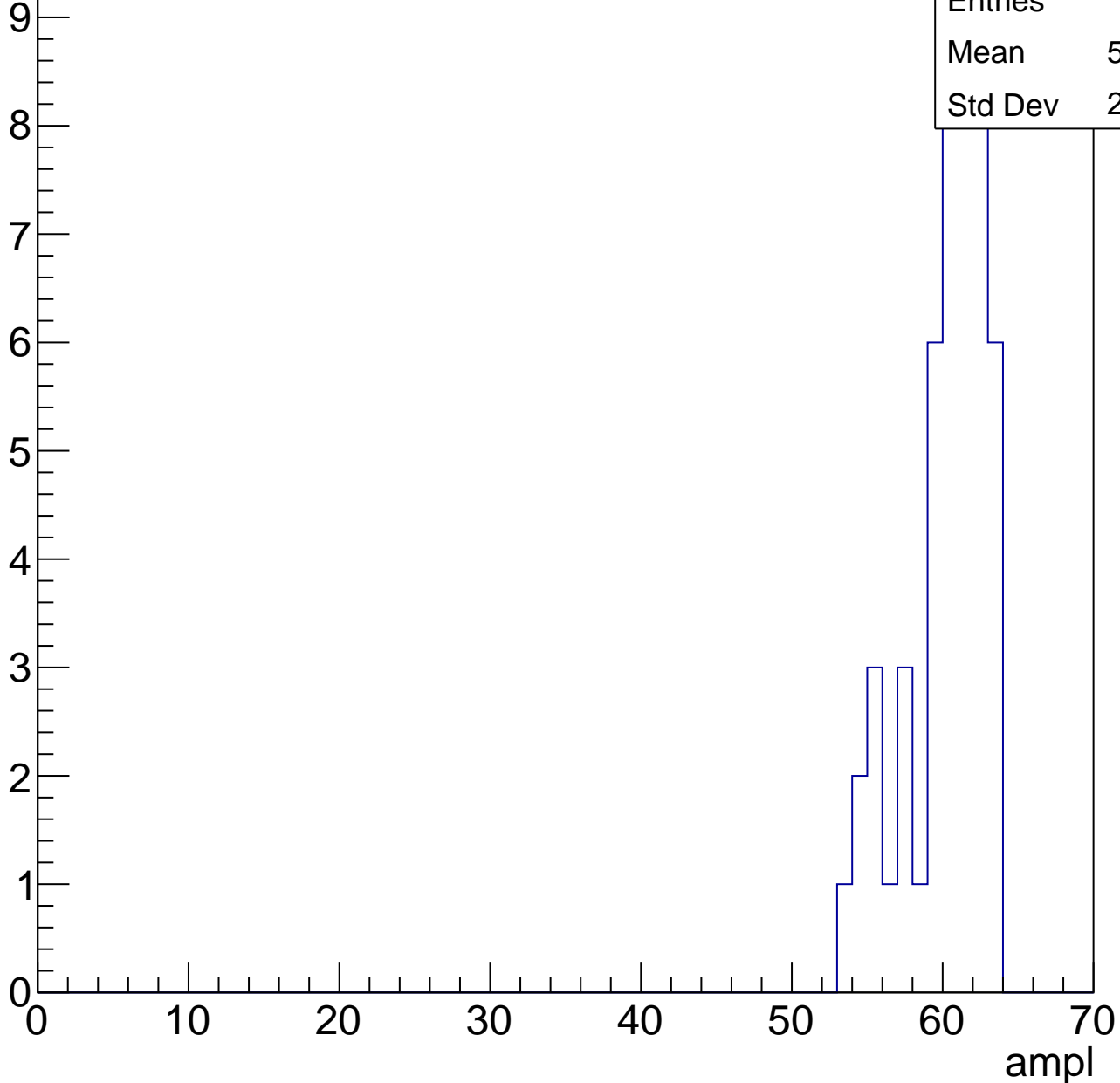


# B1L103S, U21-ch125, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

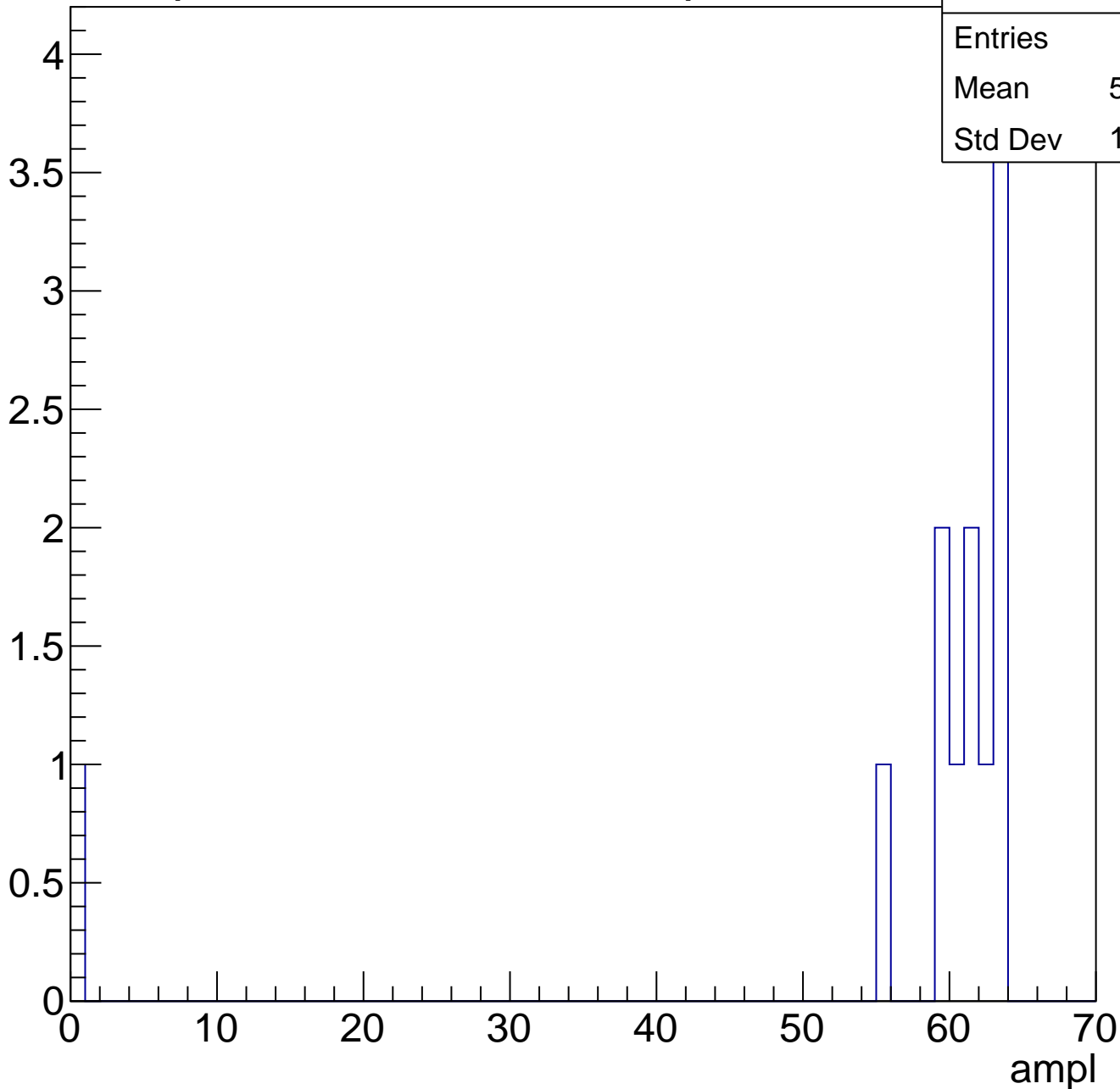
Entries	48
Mean	59.77
Std Dev	2.679



# B1L103S, U21-ch125, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U21-ch125, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U21-ch126, adc0

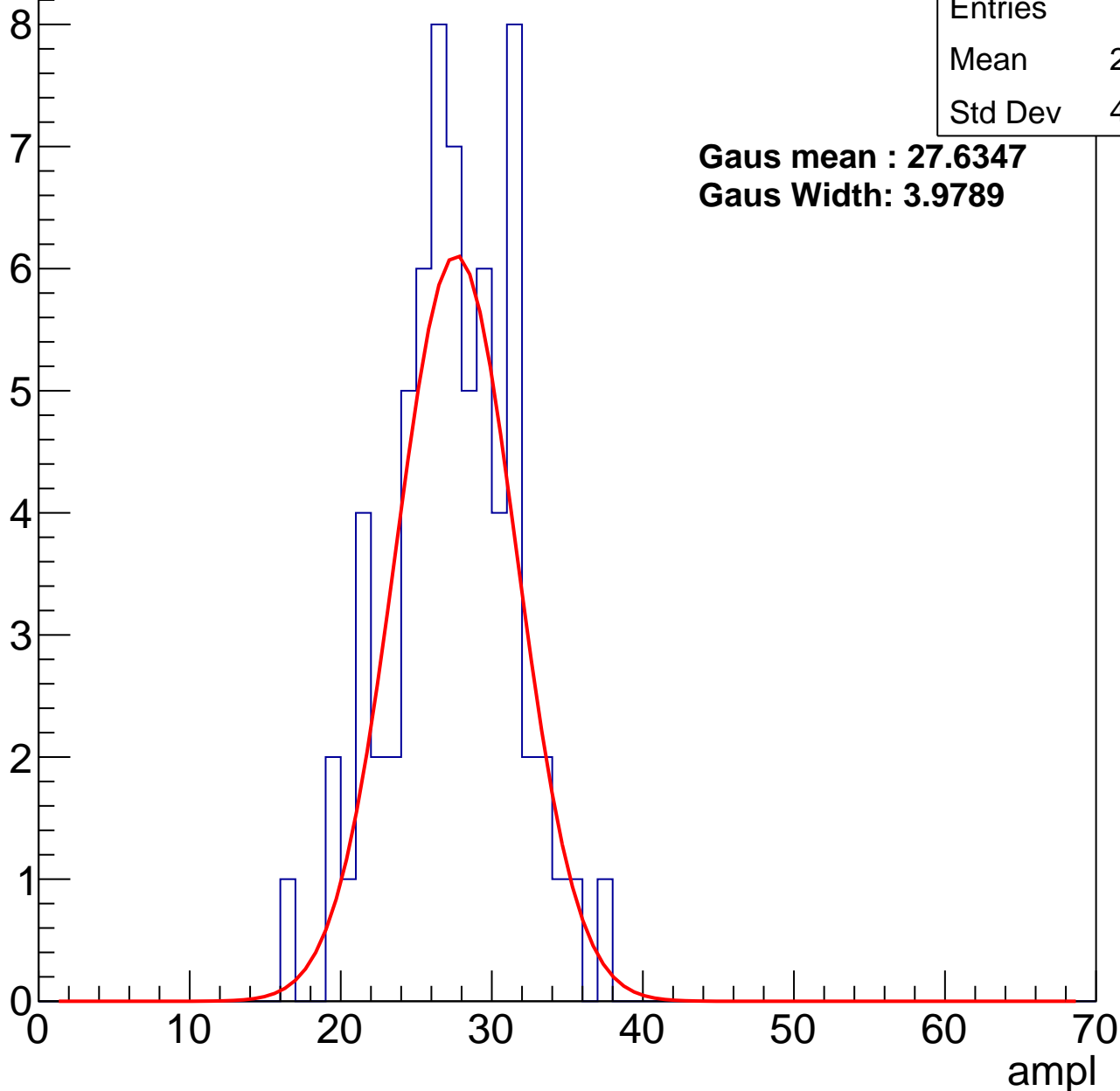
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	26.96
Std Dev	4.074

**Gaus mean : 27.6347**

**Gaus Width: 3.9789**



# B1L103S, U21-ch126, adc1

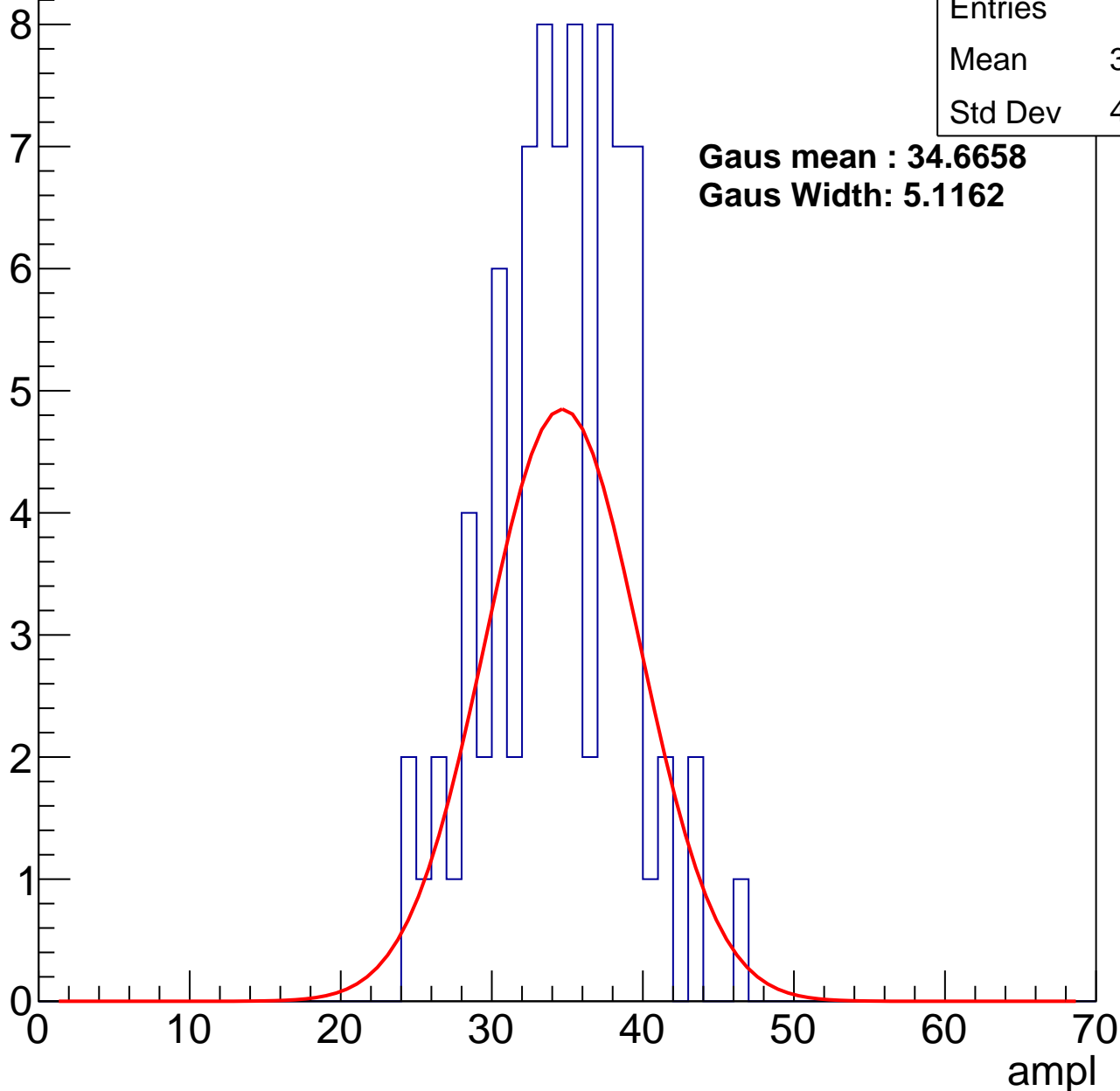
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	80
Mean	34.14
Std Dev	4.494

**Gaus mean : 34.6658**

**Gaus Width: 5.1162**



# B1L103S, U21-ch126, adc2

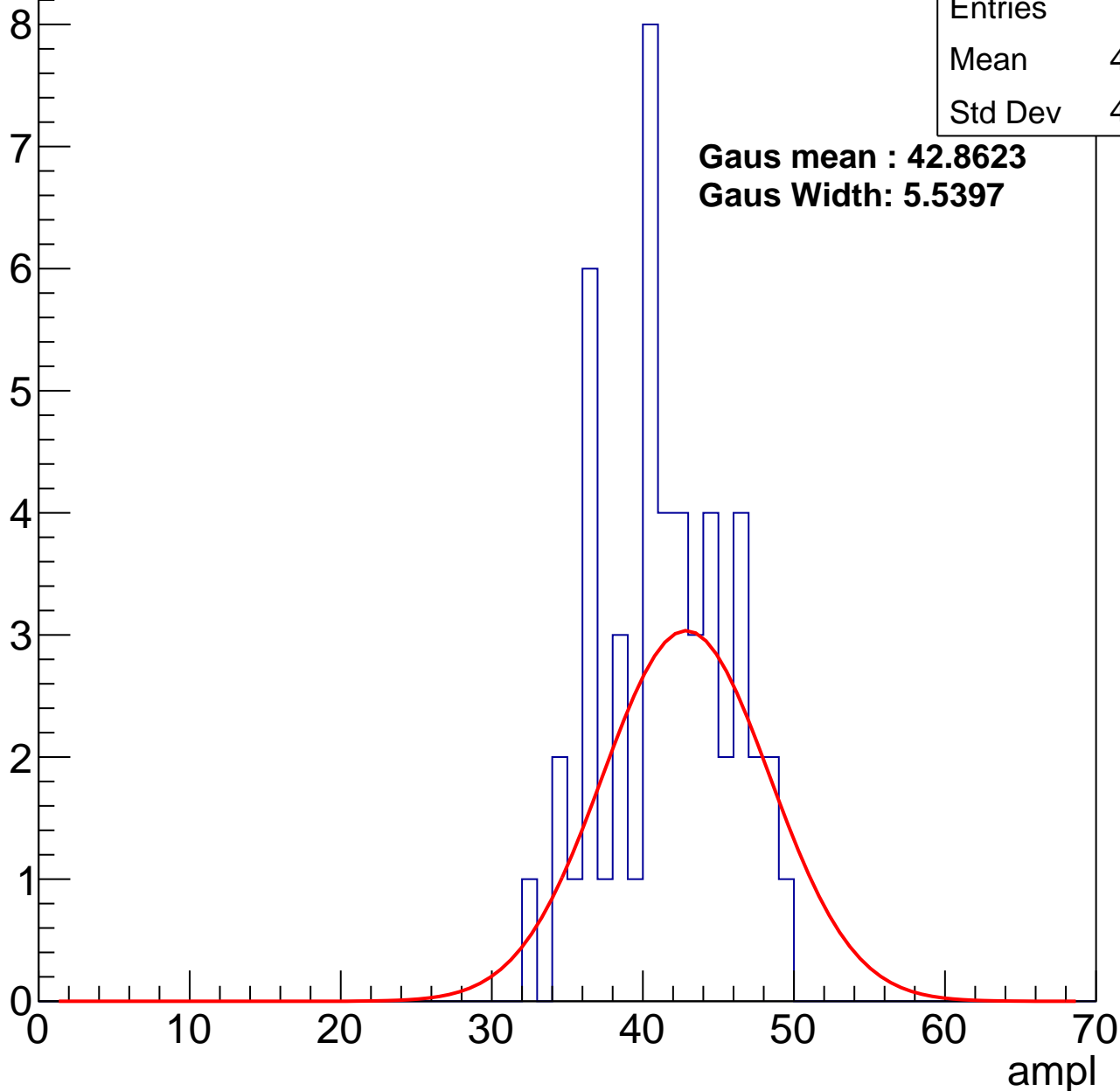
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	41.04
Std Dev	4.135

**Gaus mean : 42.8623**

**Gaus Width: 5.5397**

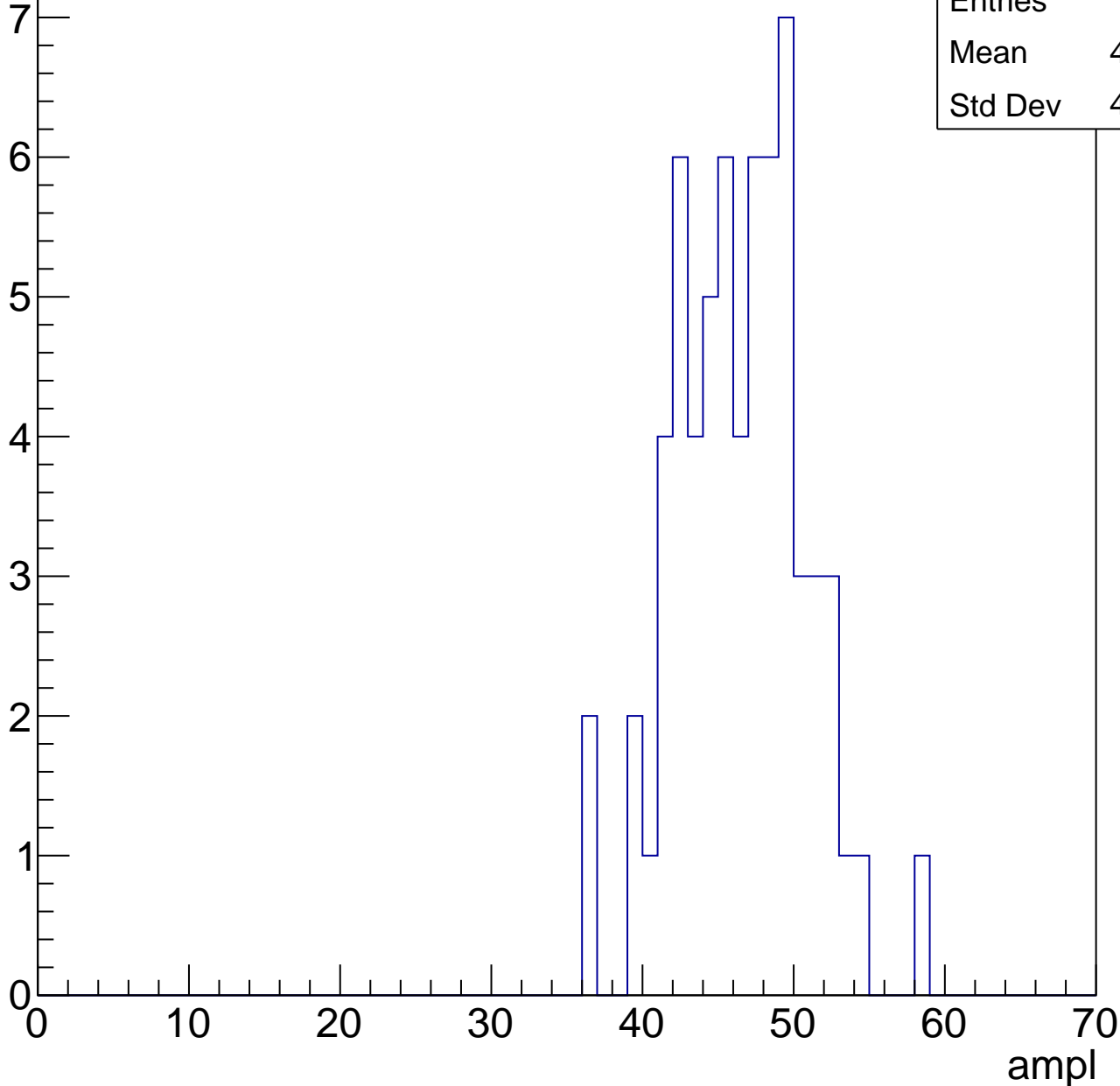


# B1L103S, U21-ch126, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	45.98
Std Dev	4.248

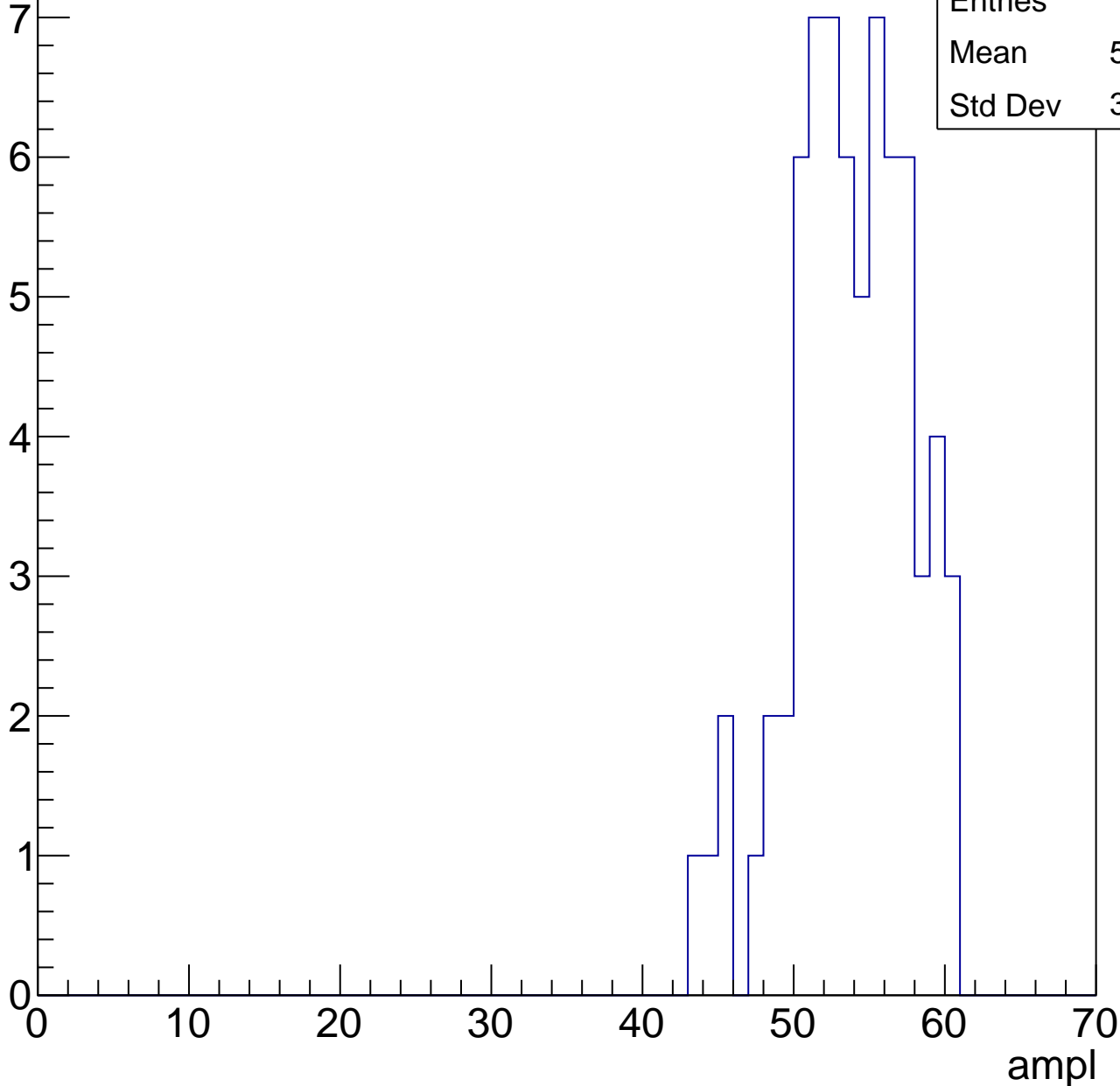


# B1L103S, U21-ch126, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	53.33
Std Dev	3.915

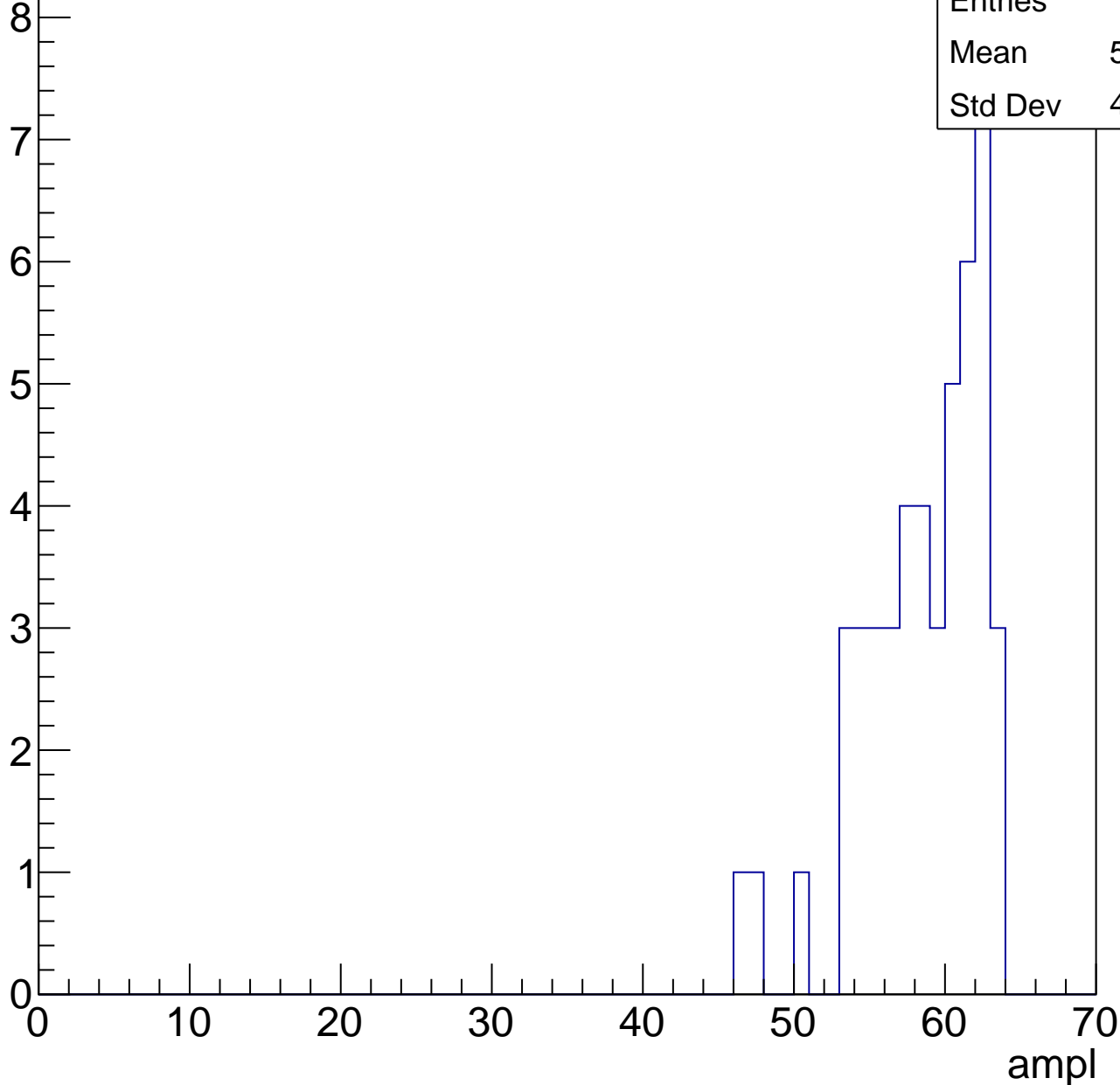


# B1L103S, U21-ch126, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

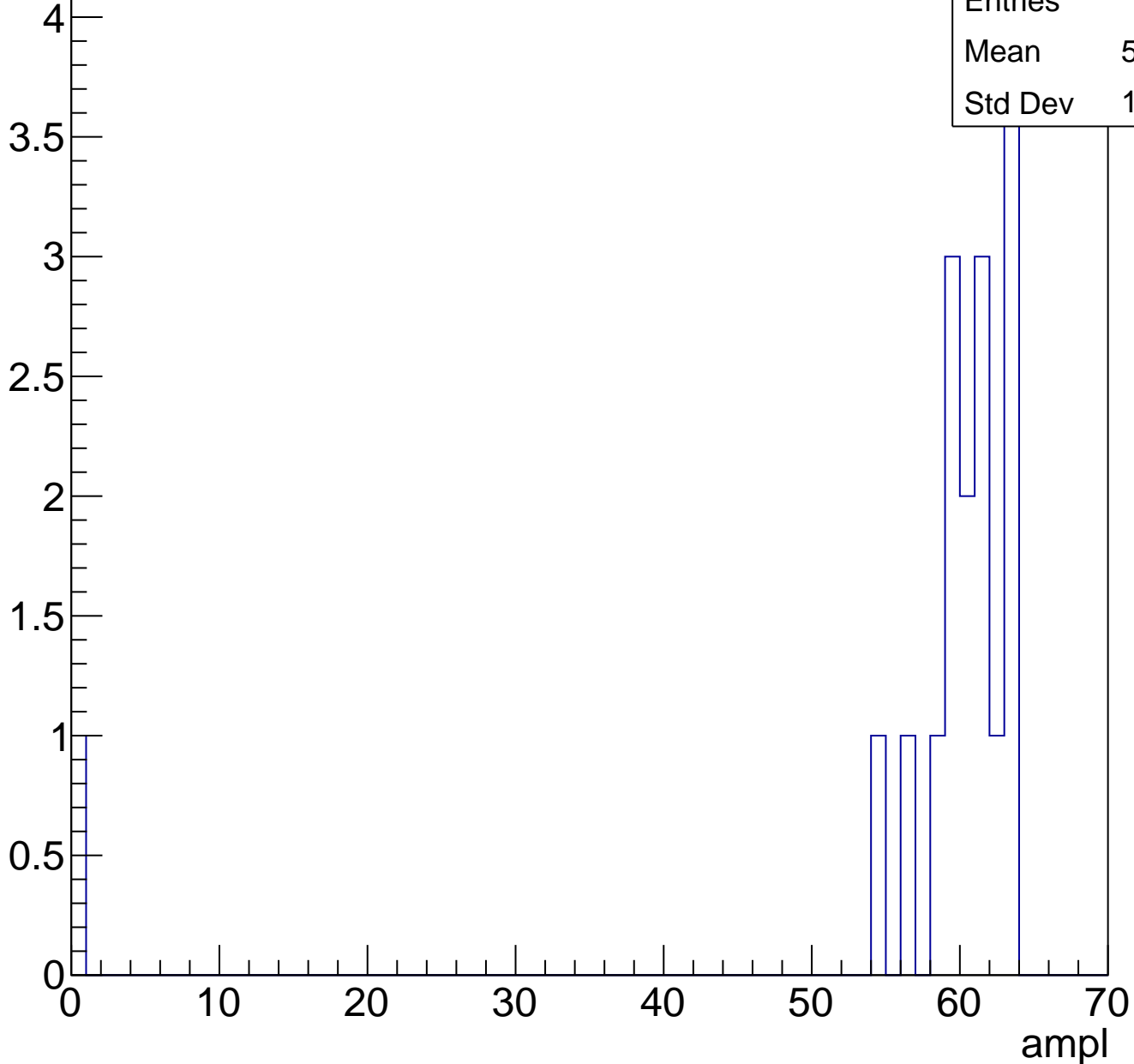
Entries	48
Mean	58.02
Std Dev	4.018



# B1L103S, U21-ch126, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

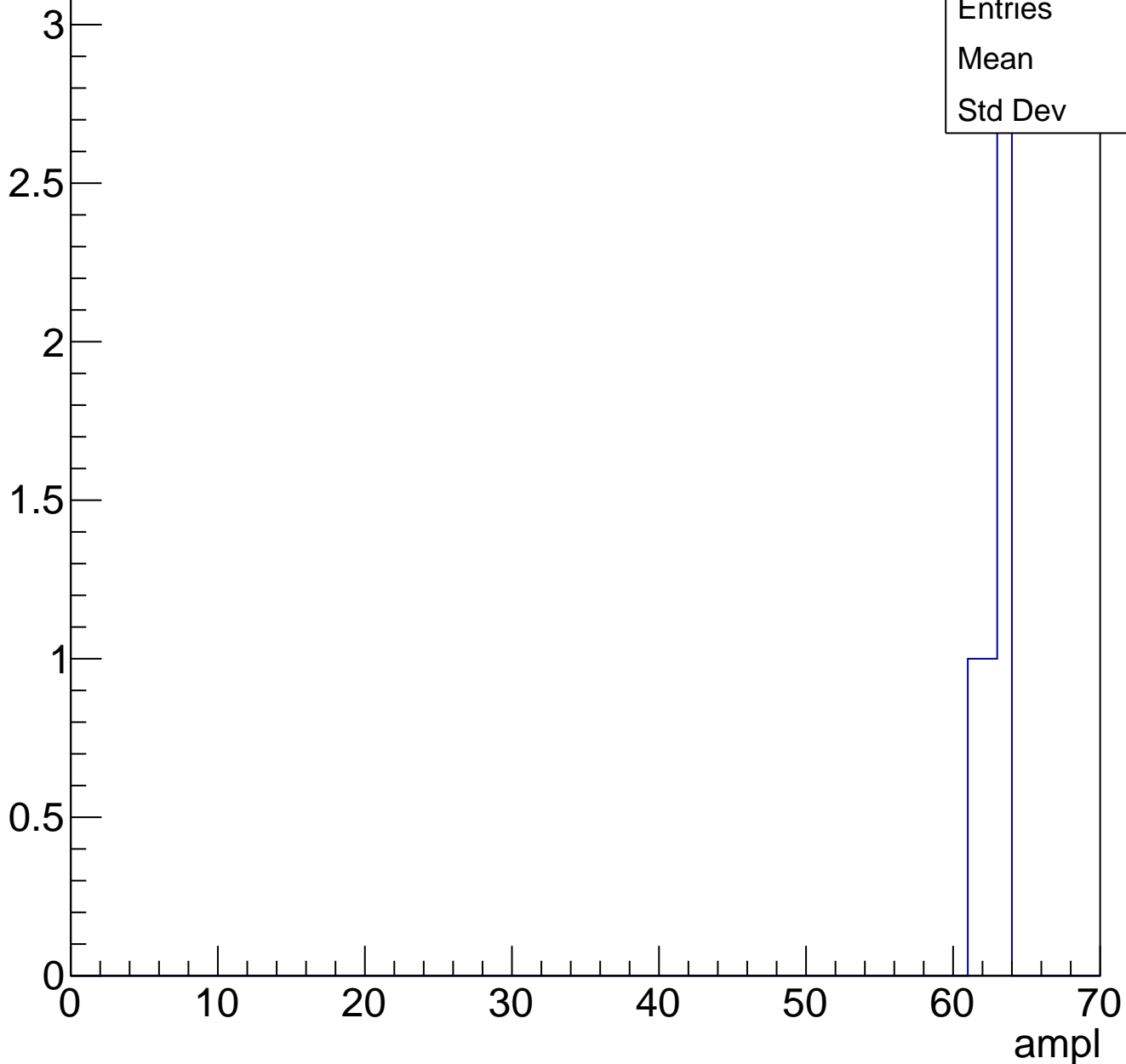




# B1L103S, U21-ch126, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U21-ch127, adc0

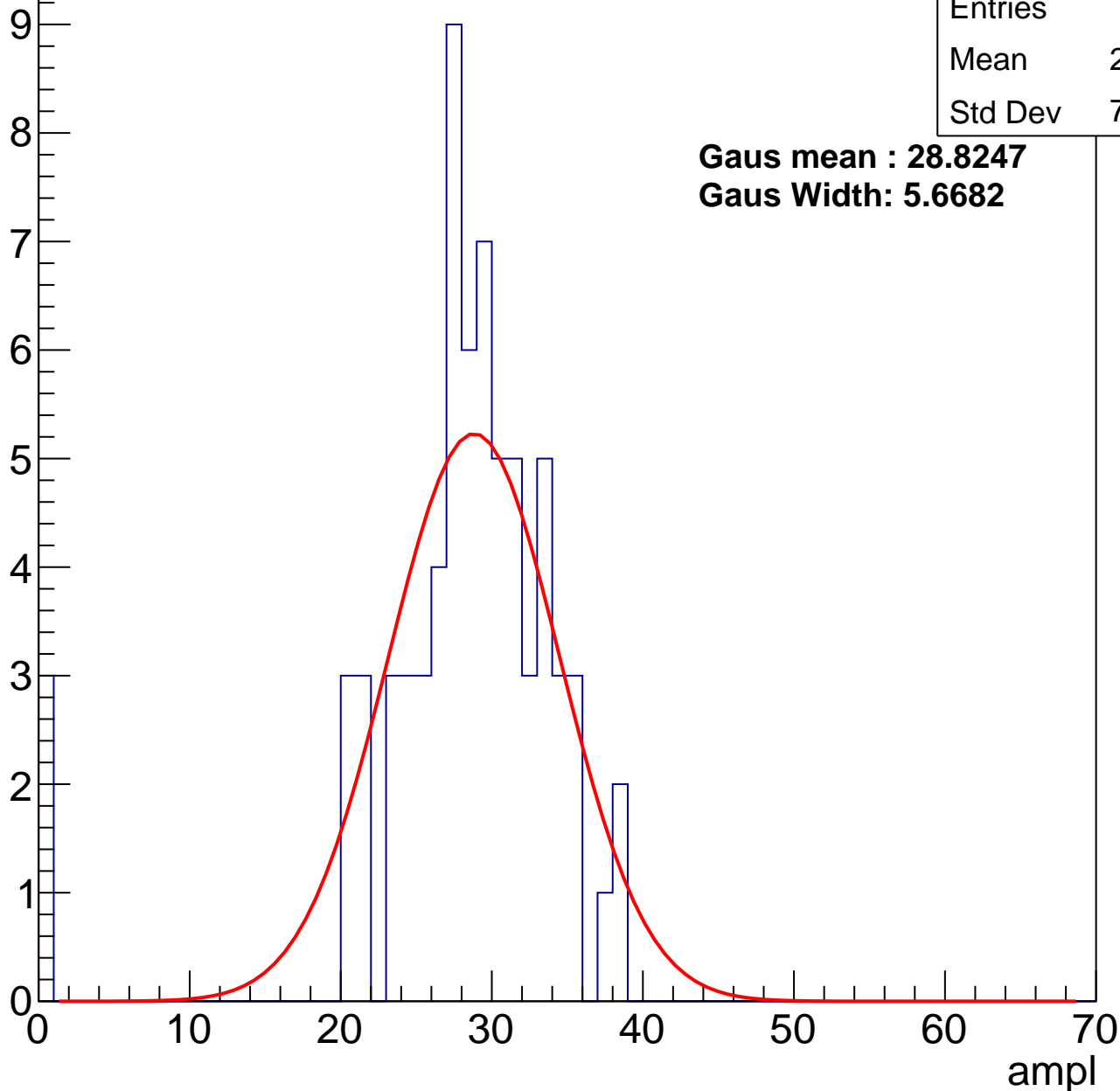
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	27.37
Std Dev	7.139

**Gaus mean : 28.8247**

**Gaus Width: 5.6682**



# B1L103S, U21-ch127, adc1

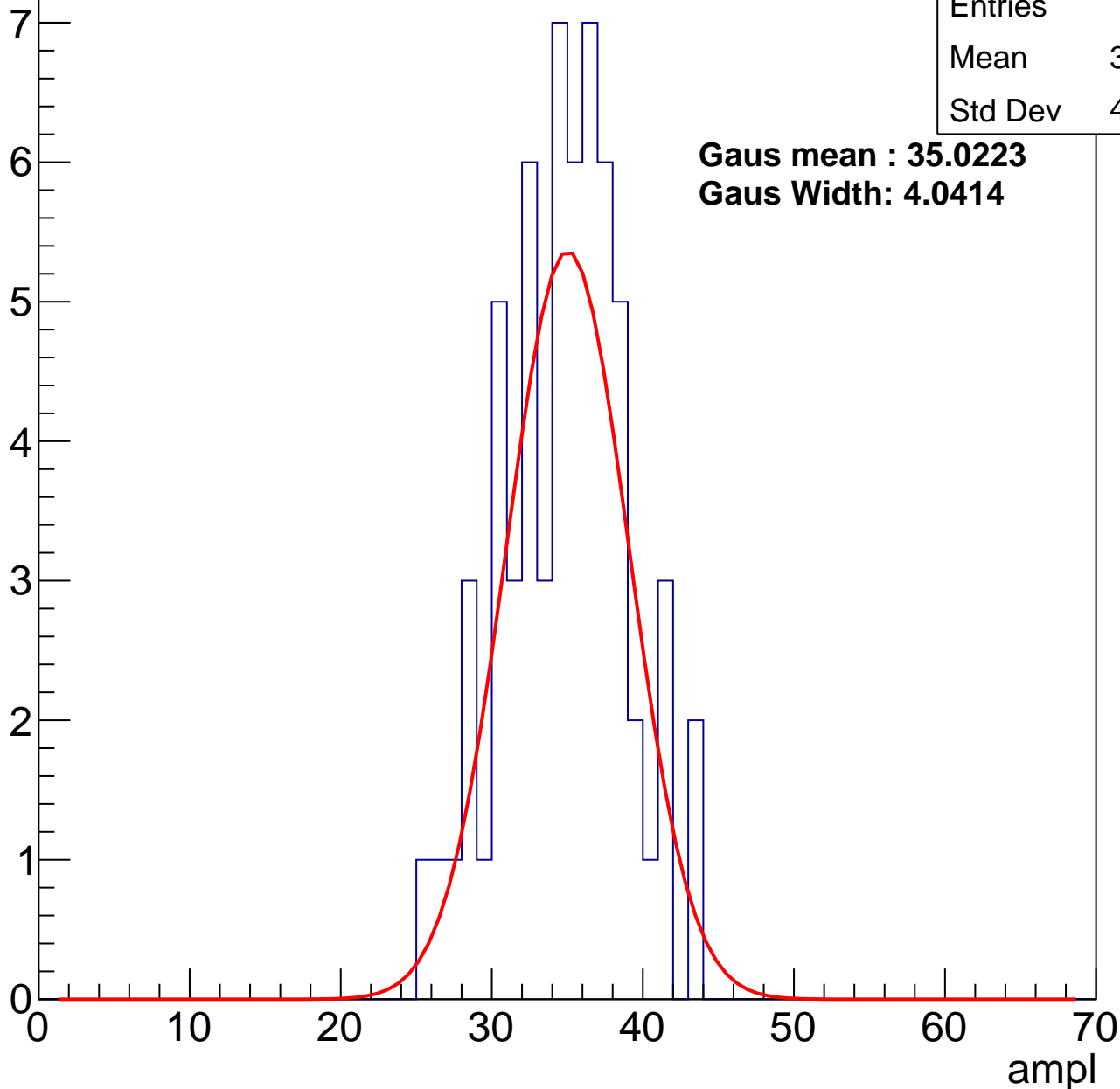
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	34.35
Std Dev	4.016

**Gaus mean : 35.0223**

**Gaus Width: 4.0414**



# B1L103S, U21-ch127, adc2

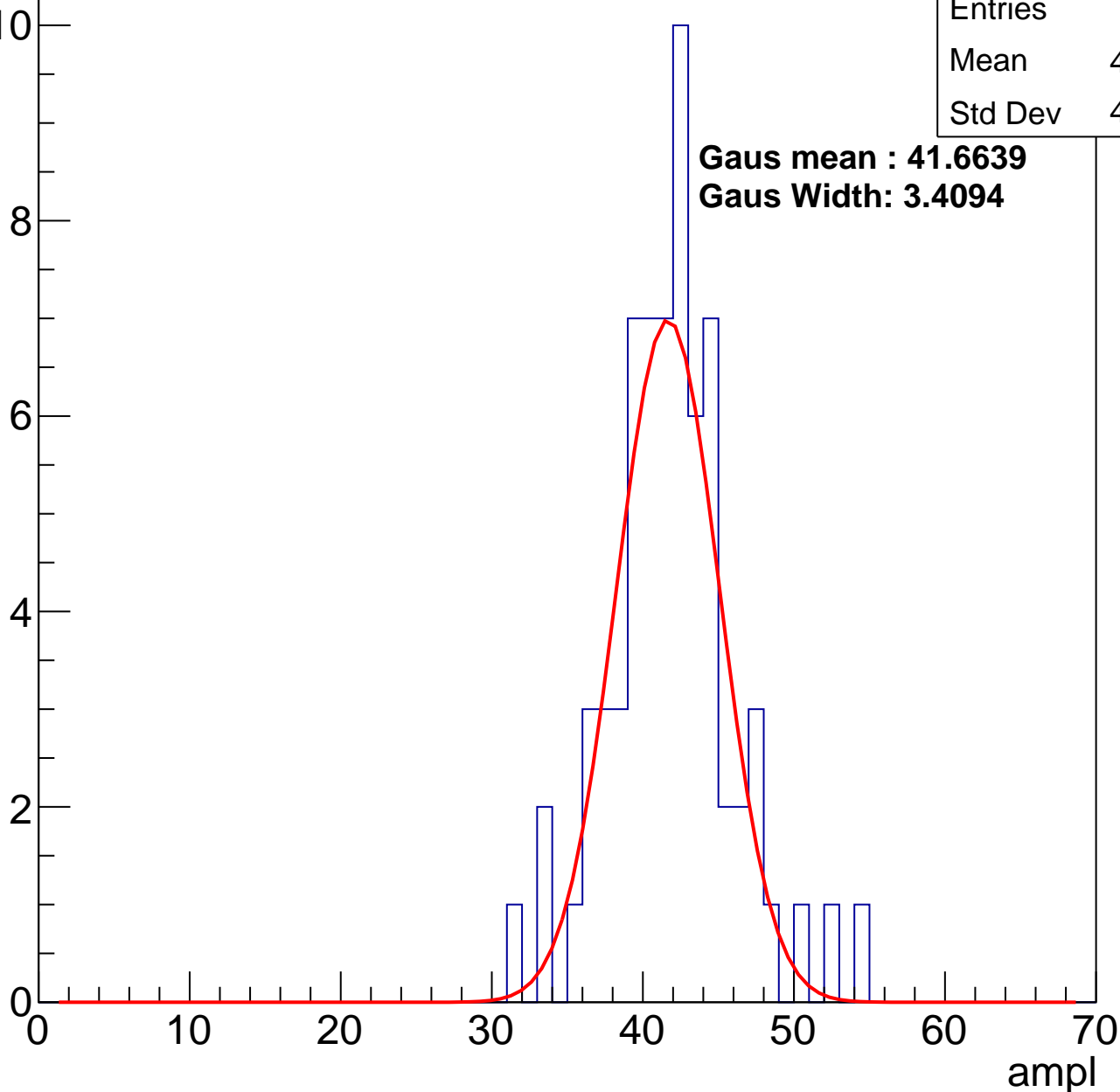
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	41.44
Std Dev	4.099

**Gaus mean : 41.6639**

**Gaus Width: 3.4094**

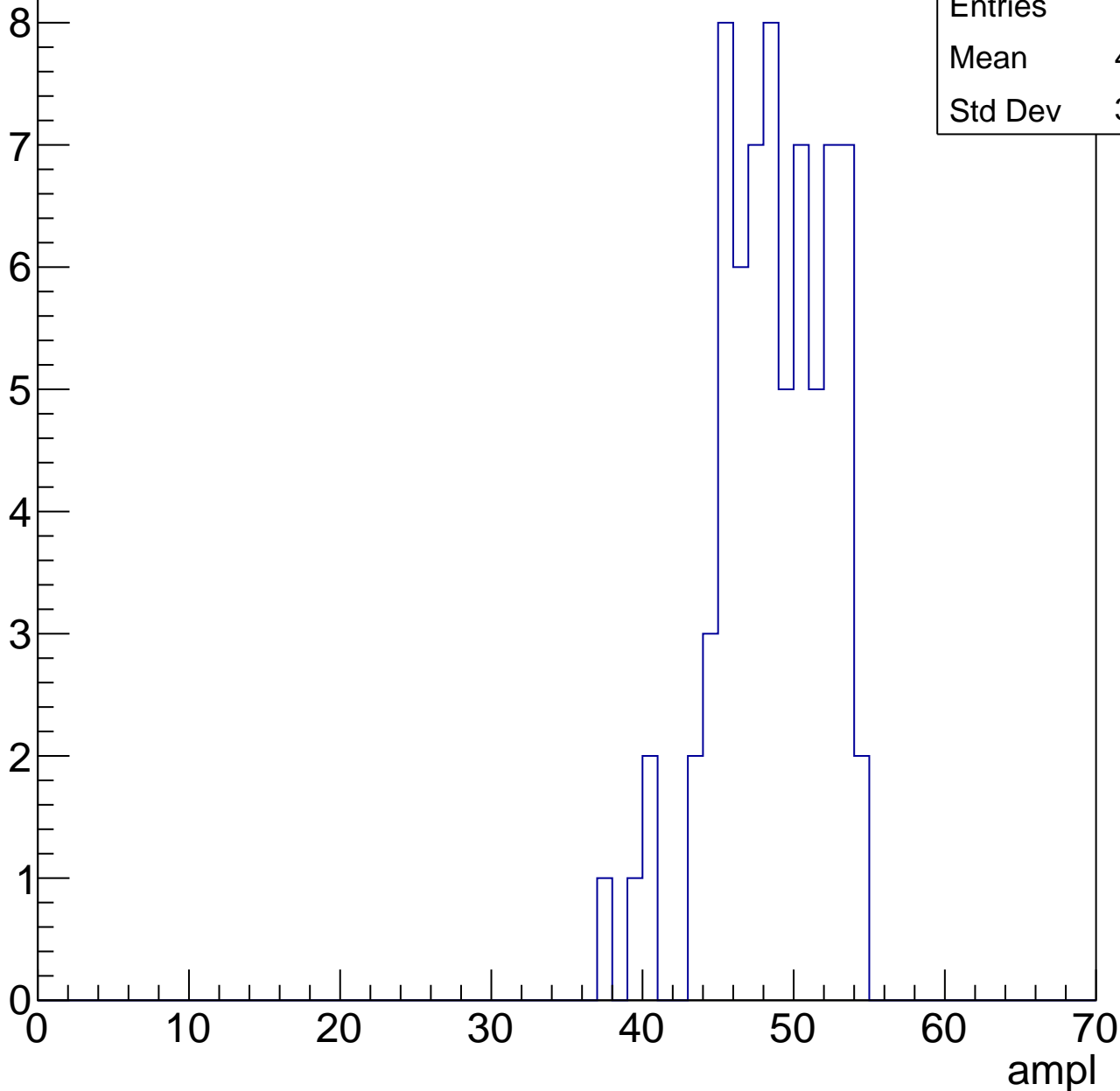


# B1L103S, U21-ch127, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	48.11
Std Dev	3.691

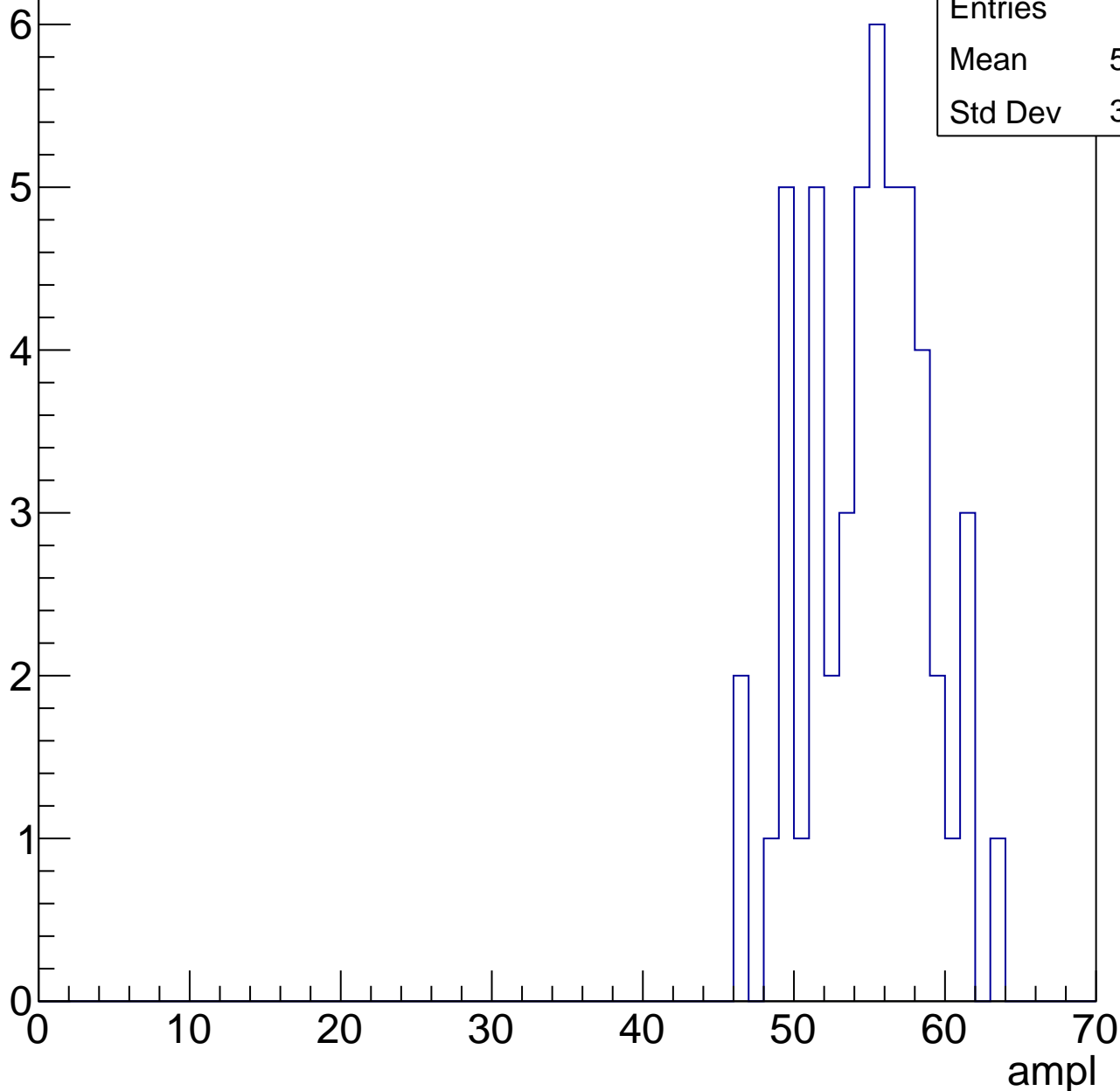


# B1L103S, U21-ch127, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	54.39
Std Dev	3.966

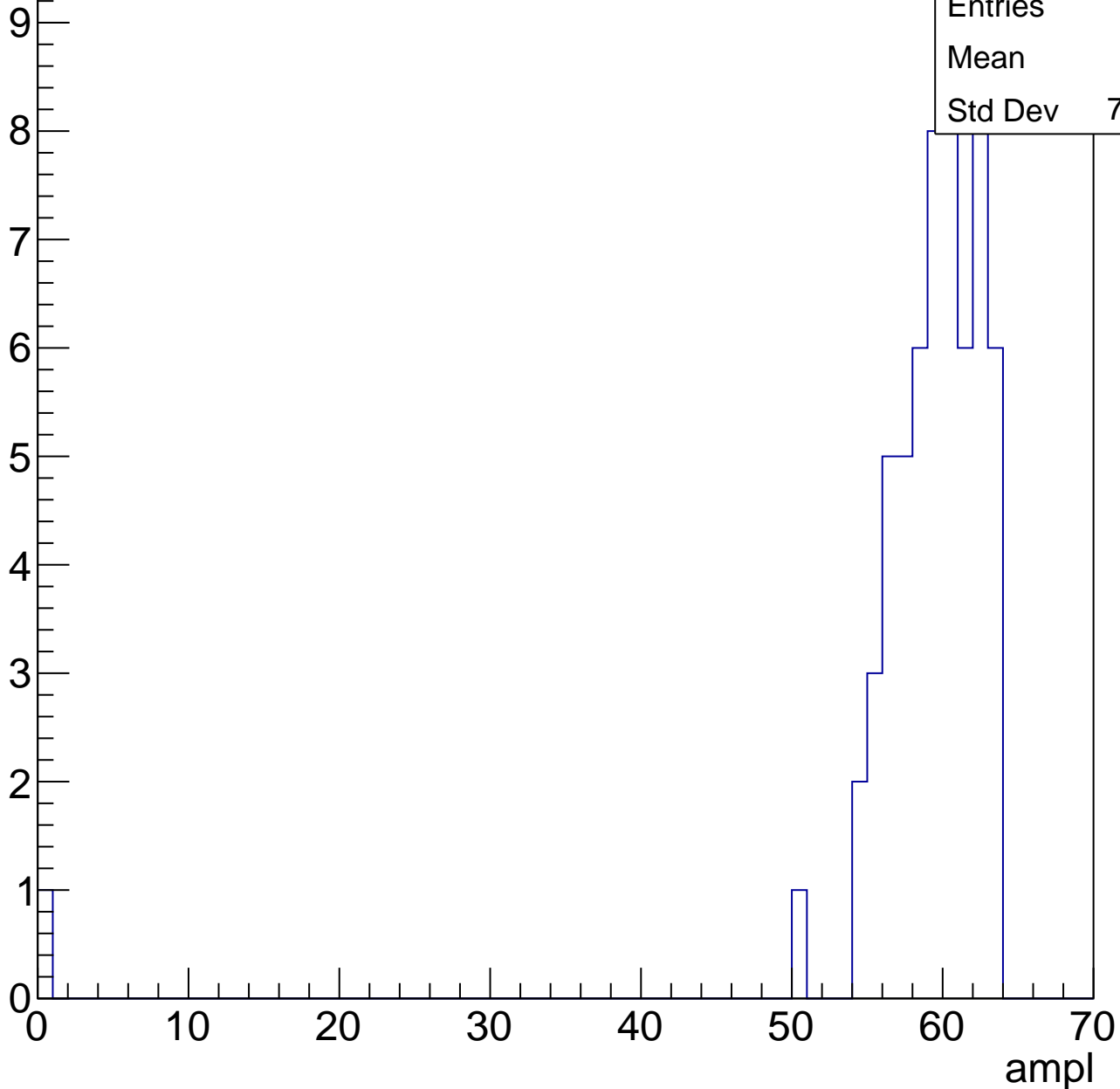


# B1L103S, U21-ch127, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	58.2
Std Dev	7.998



# B1L103S, U21-ch127, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U21-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U21-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0