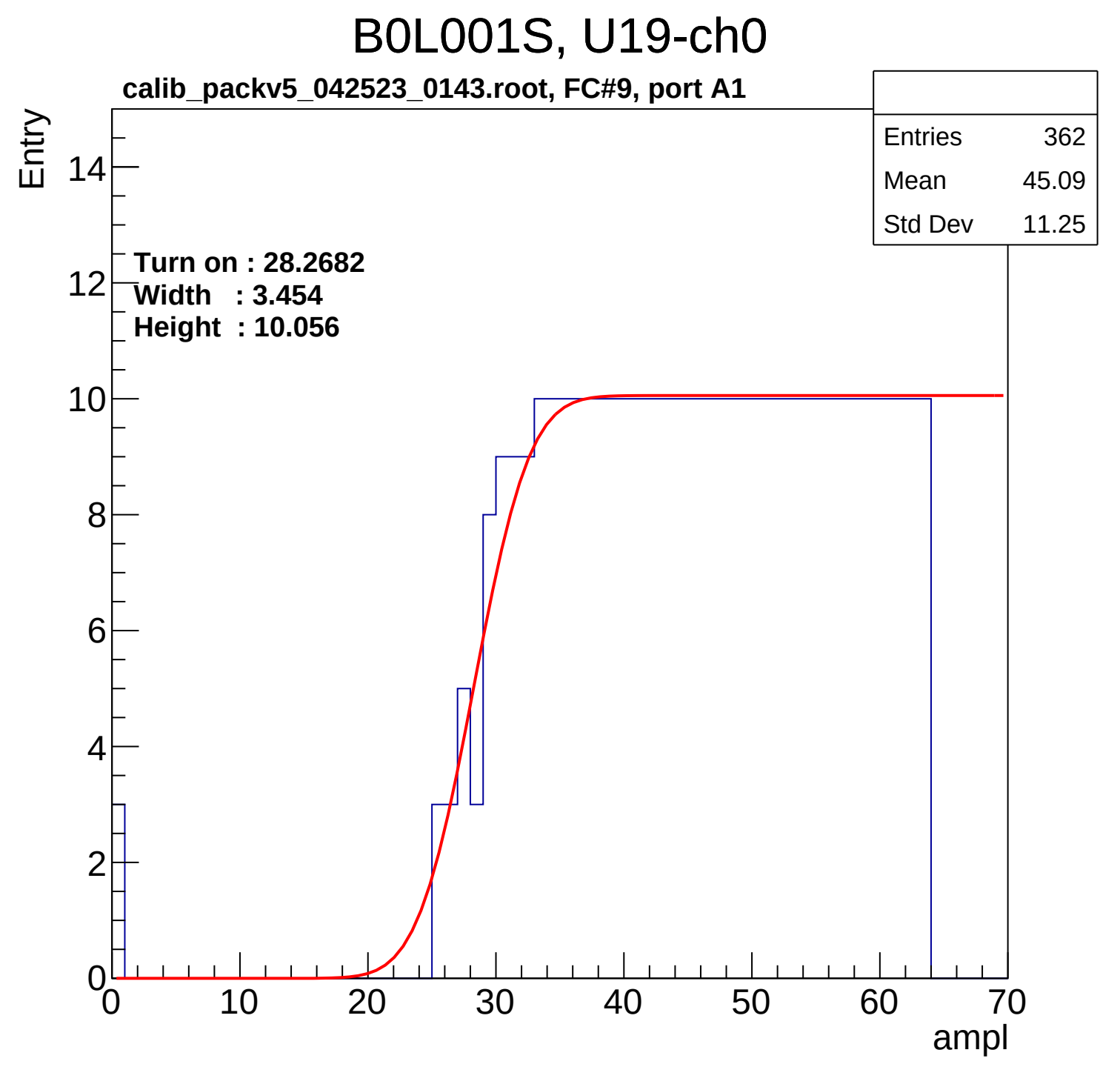
B0L001S, U19-ch0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 45.09
Std Dev 11.25
Turn on : 28.2682
Width : 3.454
Height : 10.056
Entry
ampl
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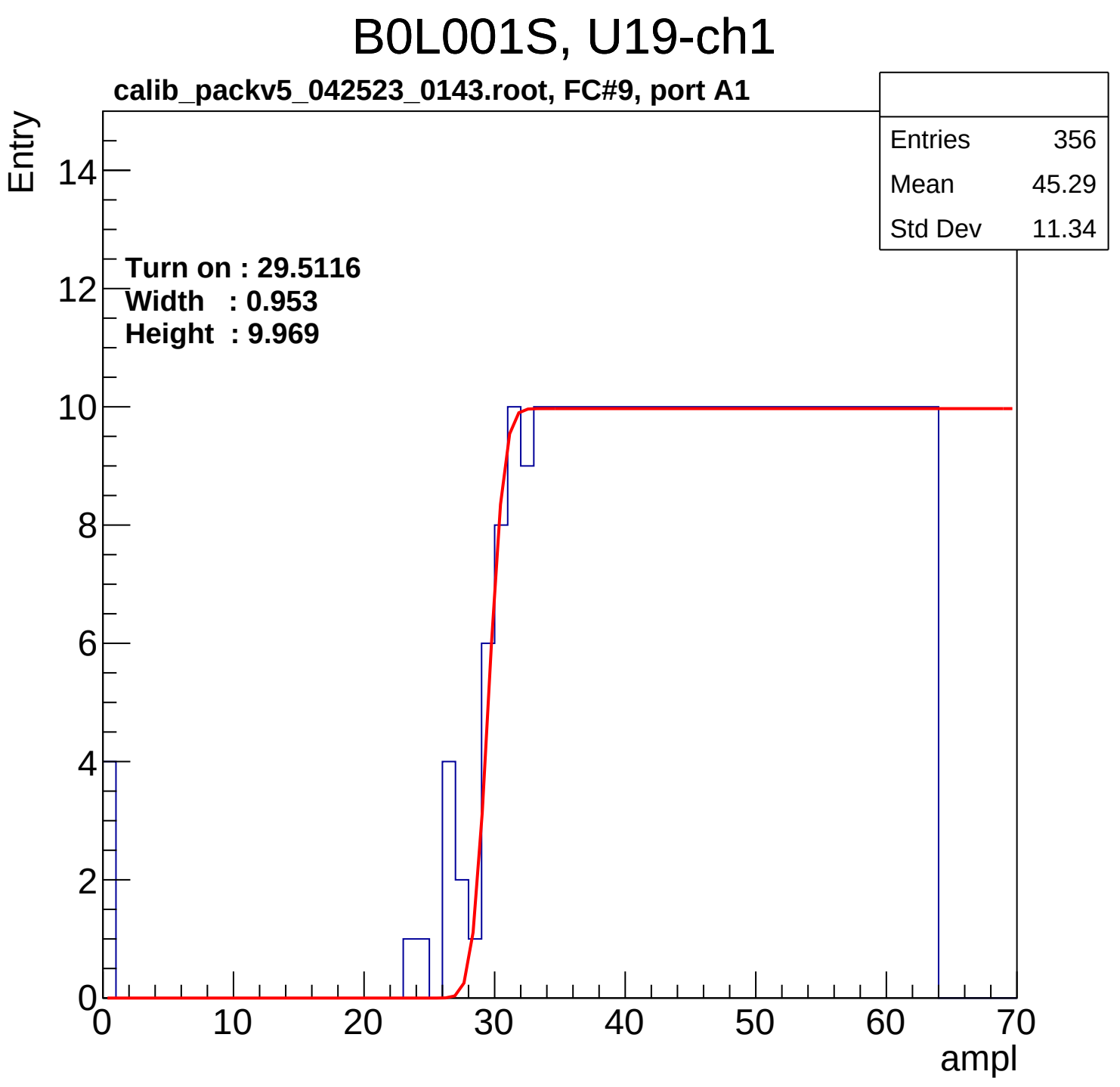
B0L001S, U19-ch1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 356
Mean 45.29
Std Dev 11.34
Turn on : 29.5116
Width : 0.953
Height : 9.969
Entry
ampl
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2
4
6
8
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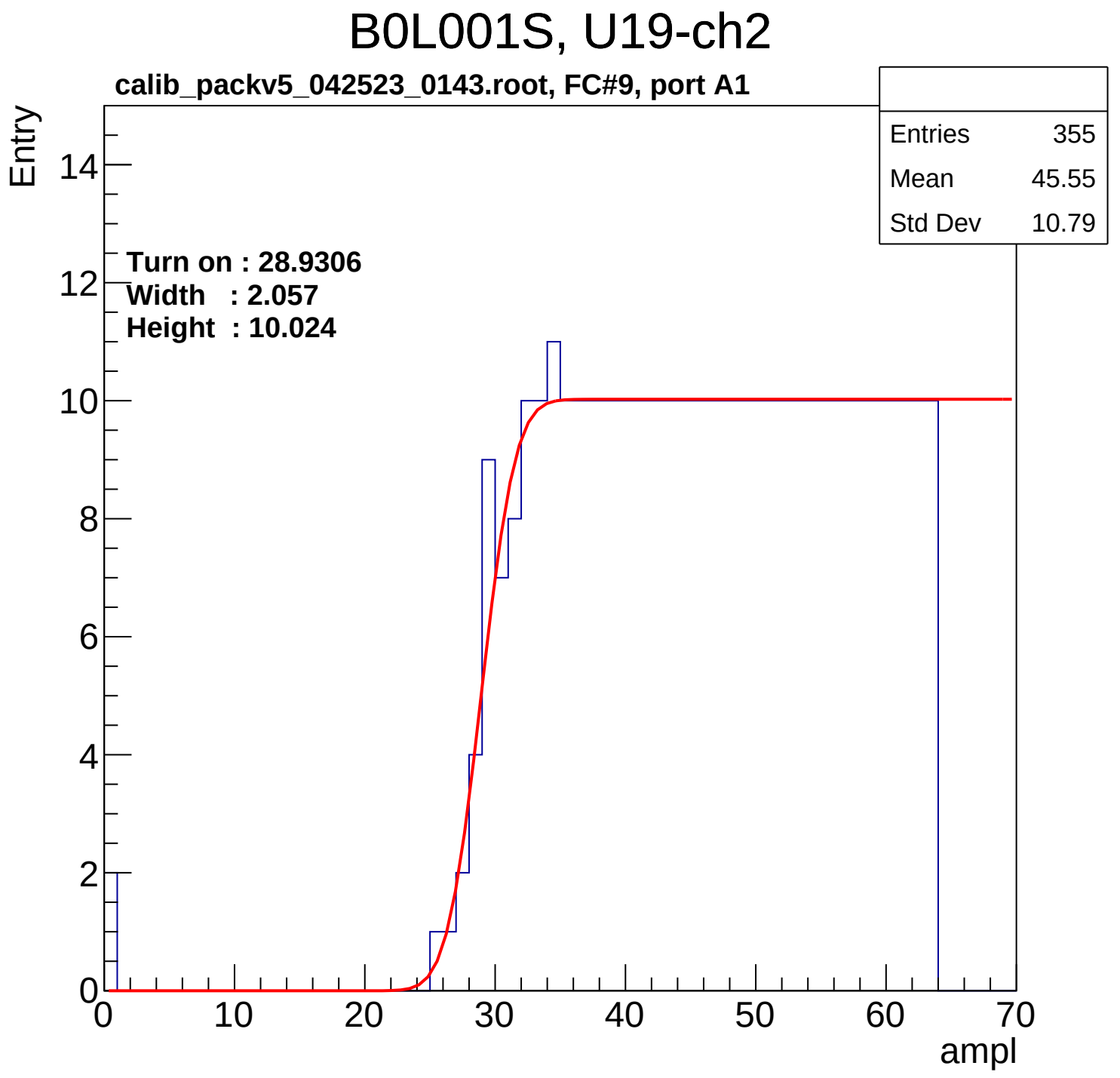
B0L001S, U19-ch2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 355
Mean 45.55
Std Dev 10.79
Turn on : 28.9306
Width : 2.057
Height : 10.024
Entry
ampl
0
2
4
6
8
10
12
14
0
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60
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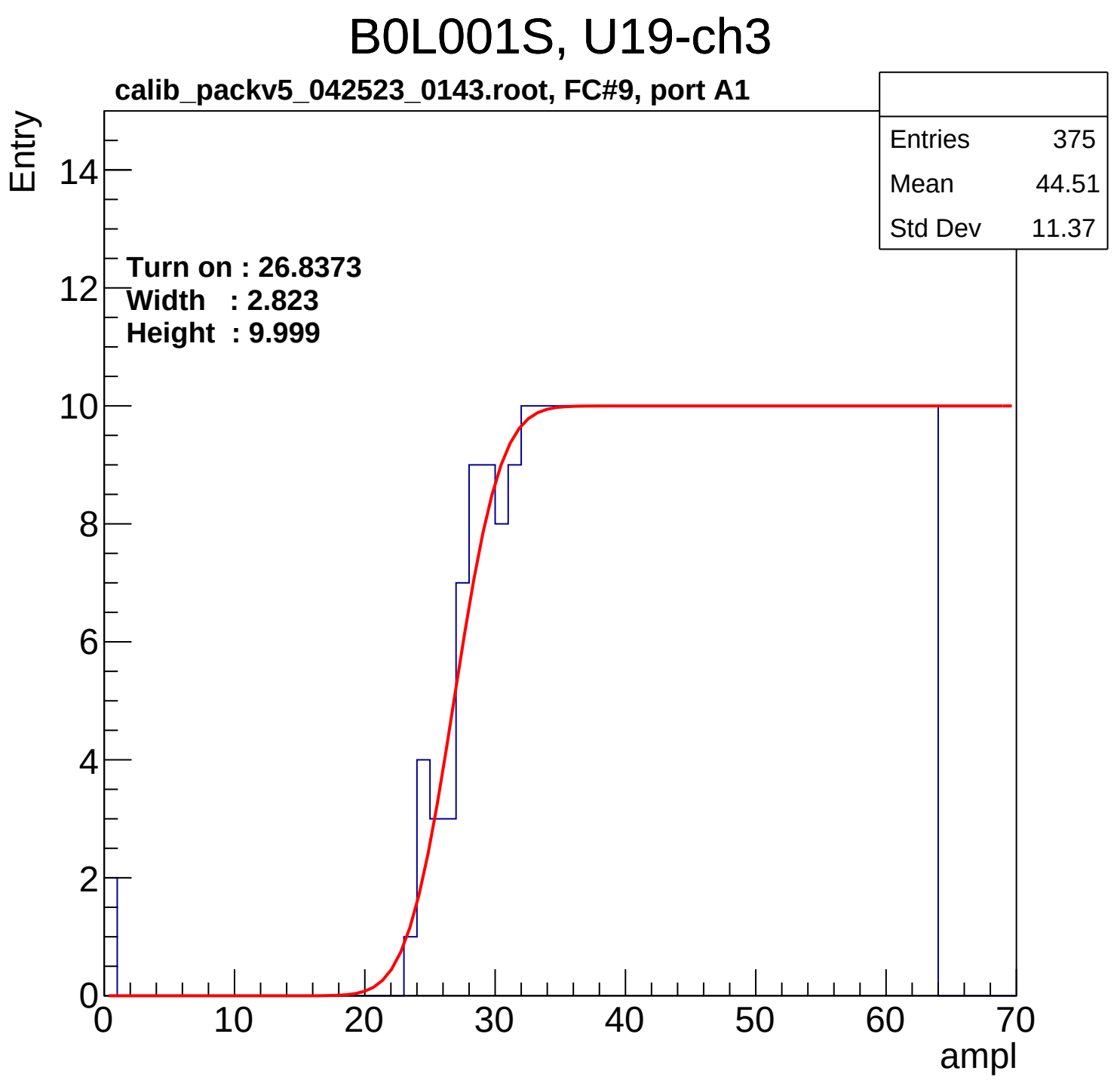
B0L001S, U19-ch3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 375
Mean 44.51
Std Dev 11.37
Turn on : 26.8373
Width : 2.823
Height : 9.999
Entry
ampl
0
2
4
6
8
10
12
14
0
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60
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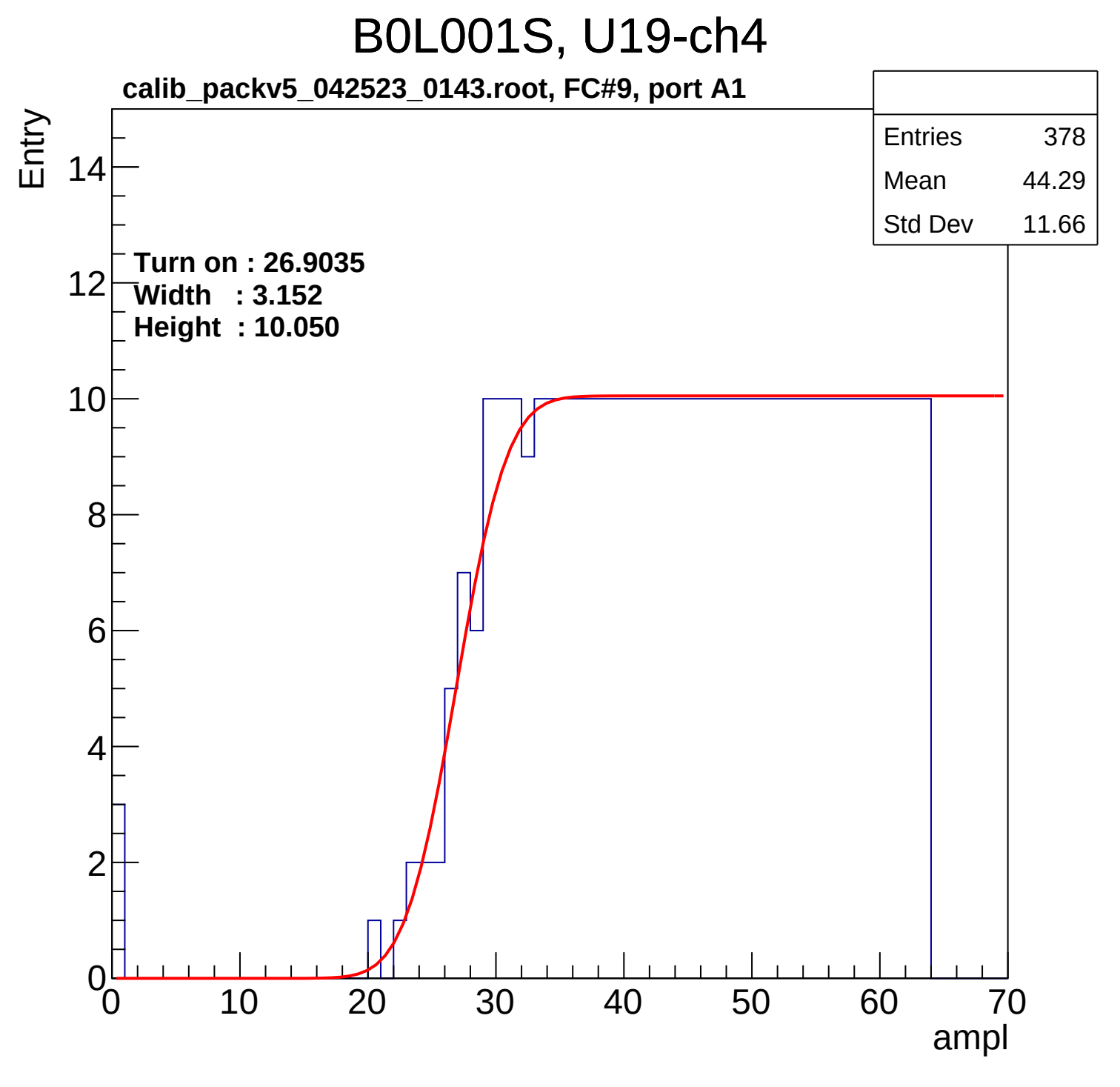
B0L001S, U19-ch4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 378
Mean 44.29
Std Dev 11.66
Turn on : 26.9035
Width : 3.152
Height : 10.050
Entry
ampl
0
2
4
6
8
10
12
14
0
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60
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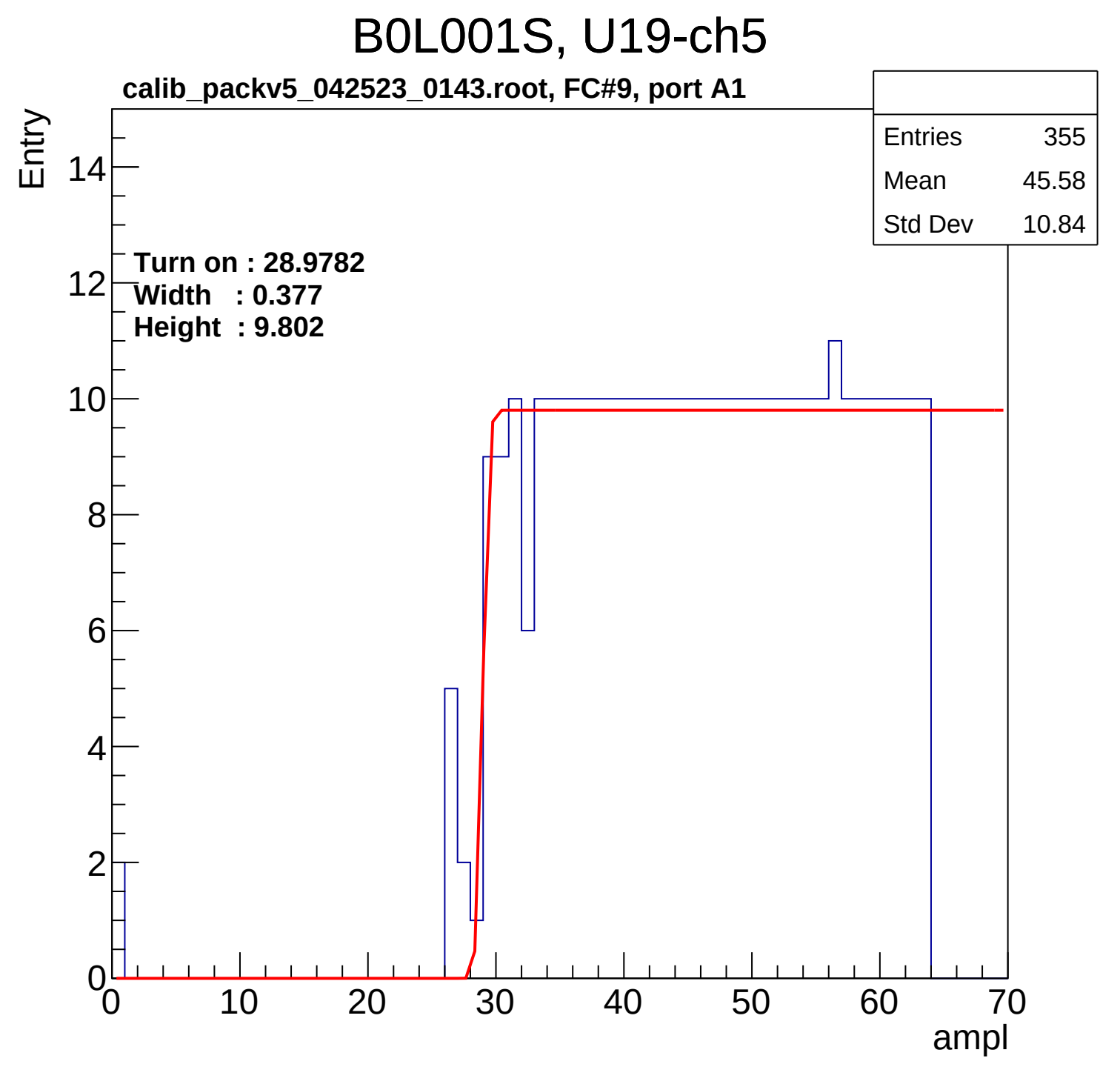
B0L001S, U19-ch5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 355
Mean 45.58
Std Dev 10.84
Turn on : 28.9782
Width : 0.377
Height : 9.802
Entry
ampl
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2
4
6
8
10
12
14
0
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60
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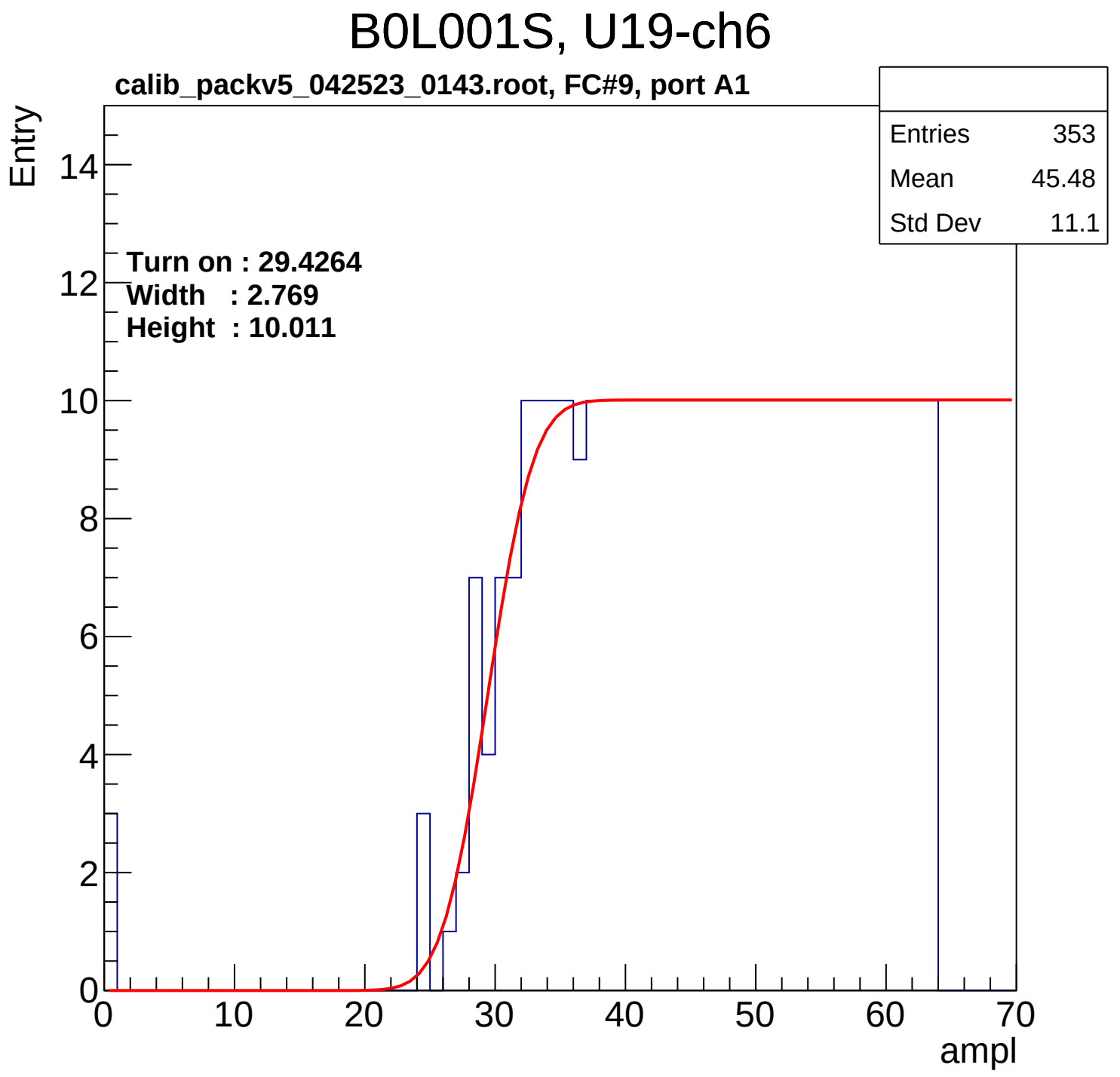
B0L001S, U19-ch6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 353
Mean 45.48
Std Dev 11.1
Turn on : 29.4264
Width : 2.769
Height : 10.011
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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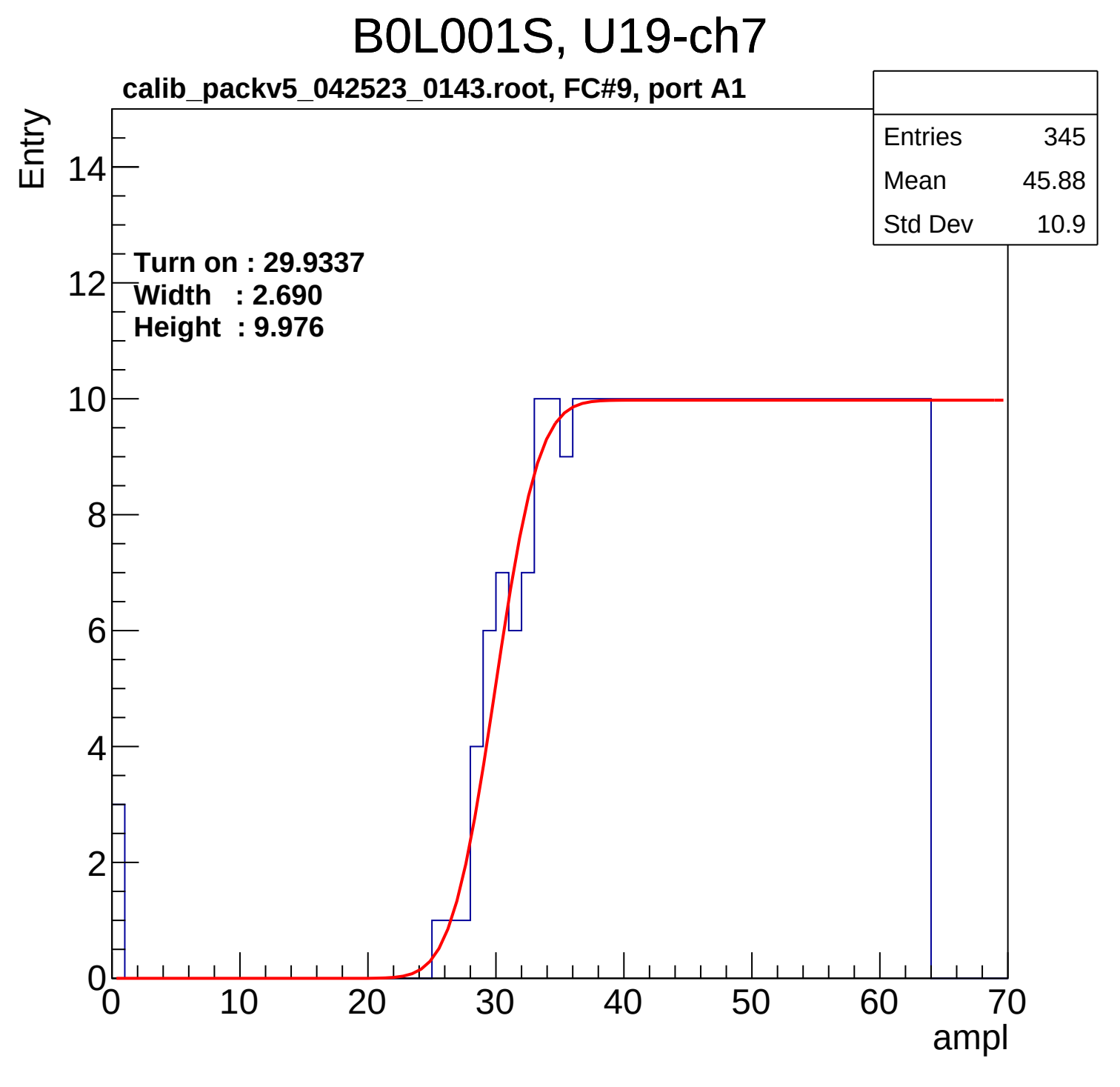
B0L001S, U19-ch7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 345
Mean 45.88
Std Dev 10.9
Turn on : 29.9337
Width : 2.690
Height : 9.976
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
50
60
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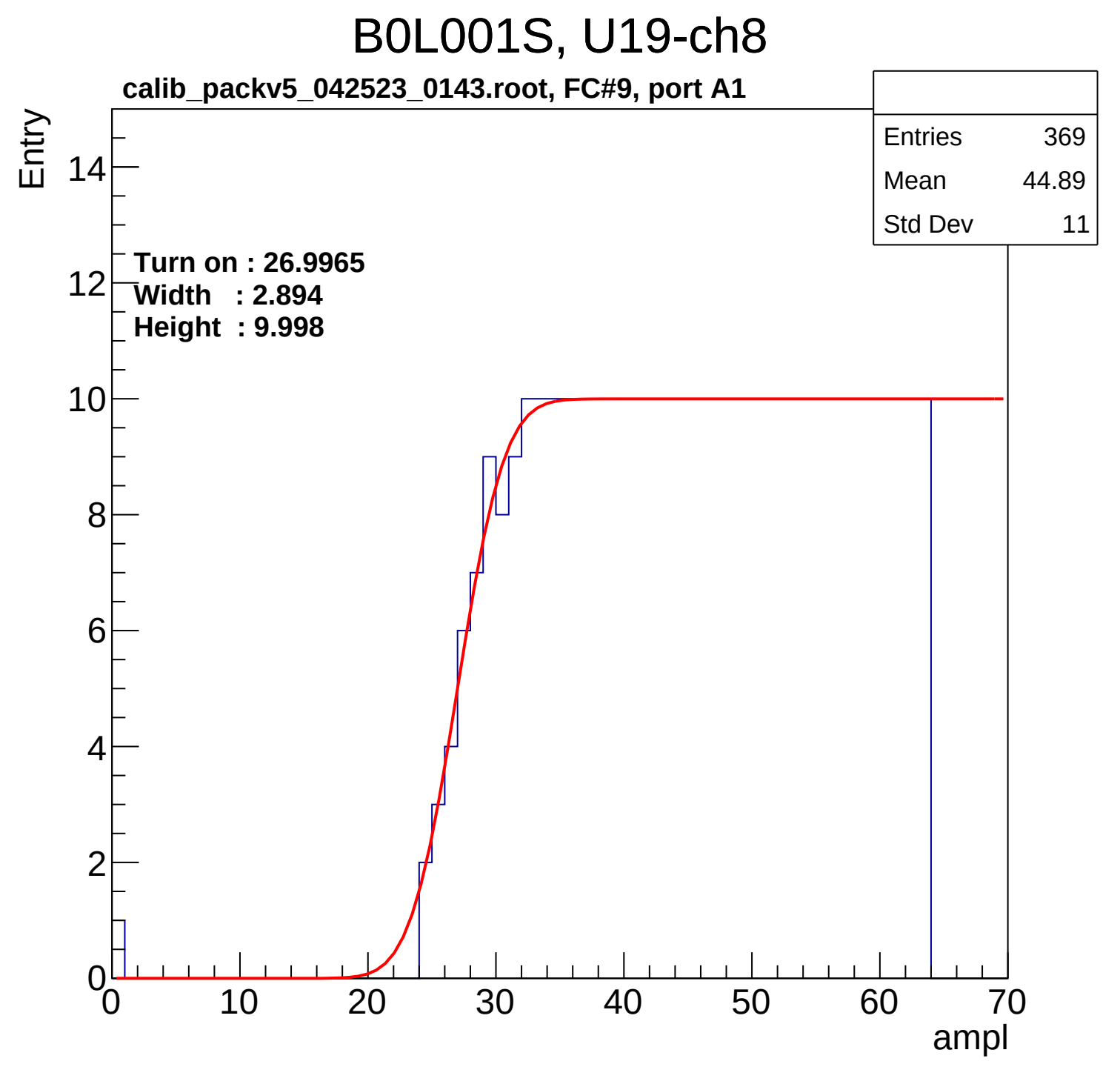
B0L001S, U19-ch8
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.89
Std Dev 11
Turn on : 26.9965
Width : 2.894
Height : 9.998
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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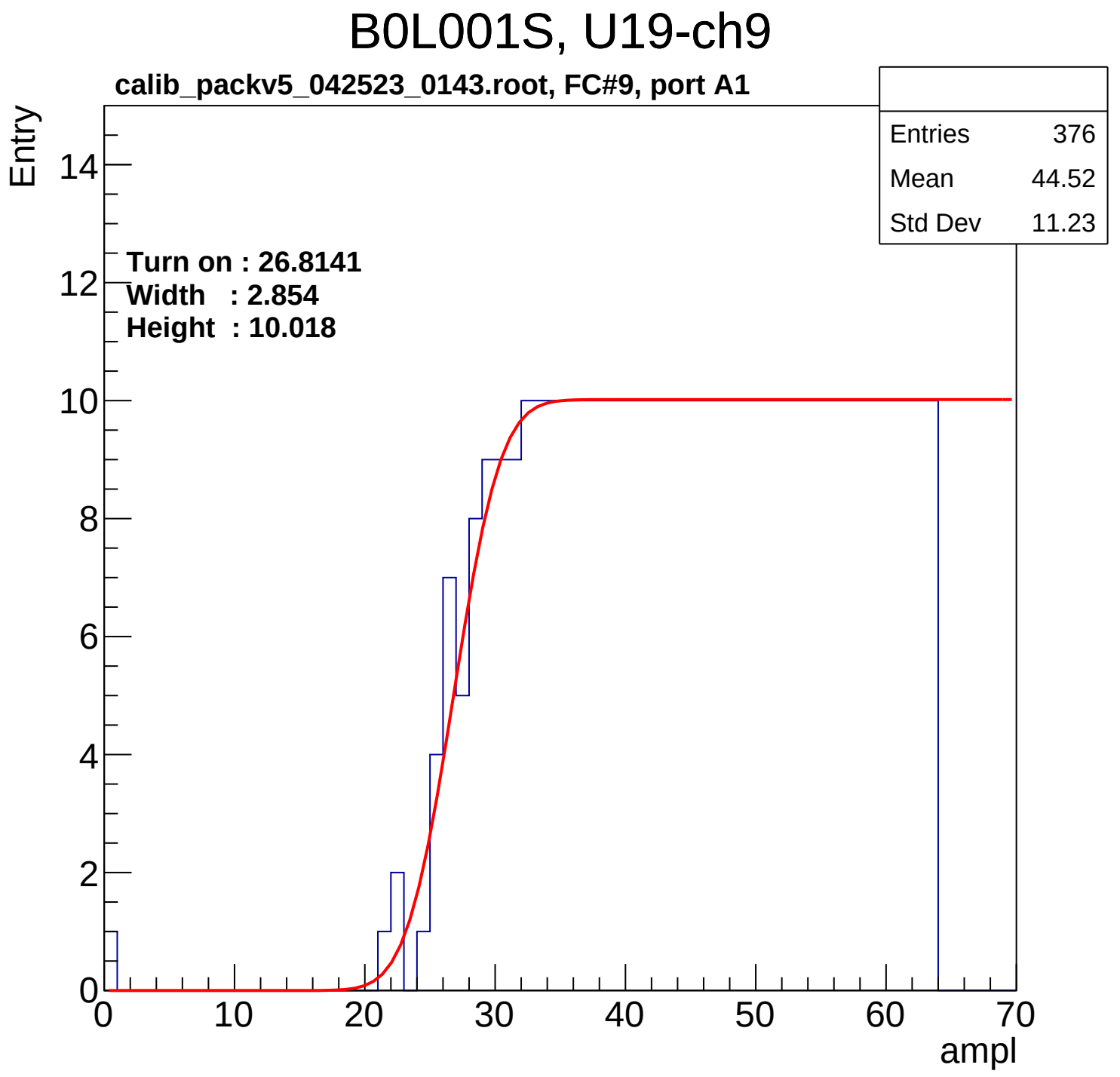
B0L001S, U19-ch9
calib_packv5_042523_0143.root, FC#9, port A1
Entries 376
Mean 44.52
Std Dev 11.23
Turn on : 26.8141
Width : 2.854
Height : 10.018
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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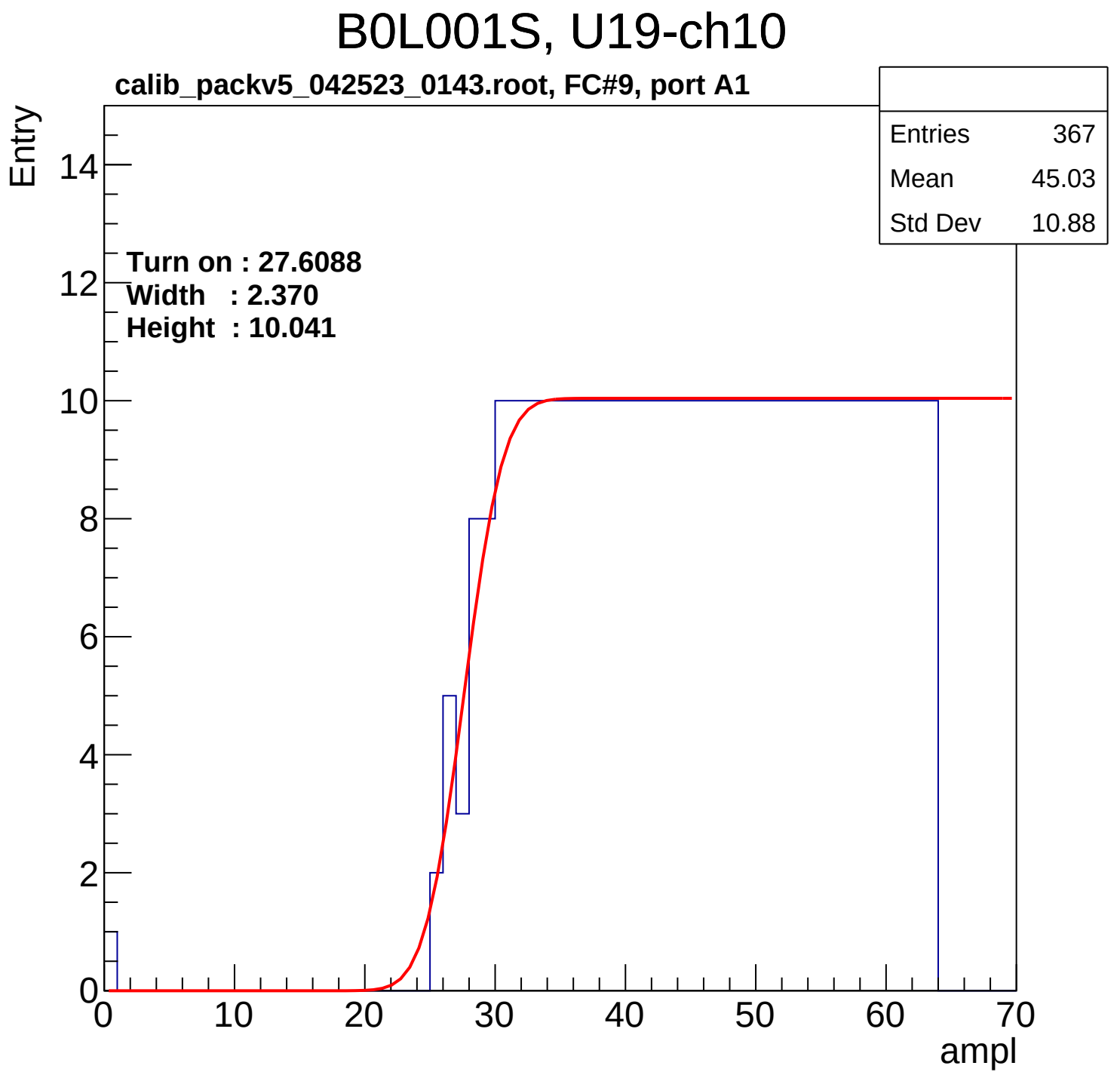
B0L001S, U19-ch10
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 45.03
Std Dev 10.88
Turn on : 27.6088
Width : 2.370
Height : 10.041
Entry
ampl
0
2
4
6
8
10
12
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0
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20
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60
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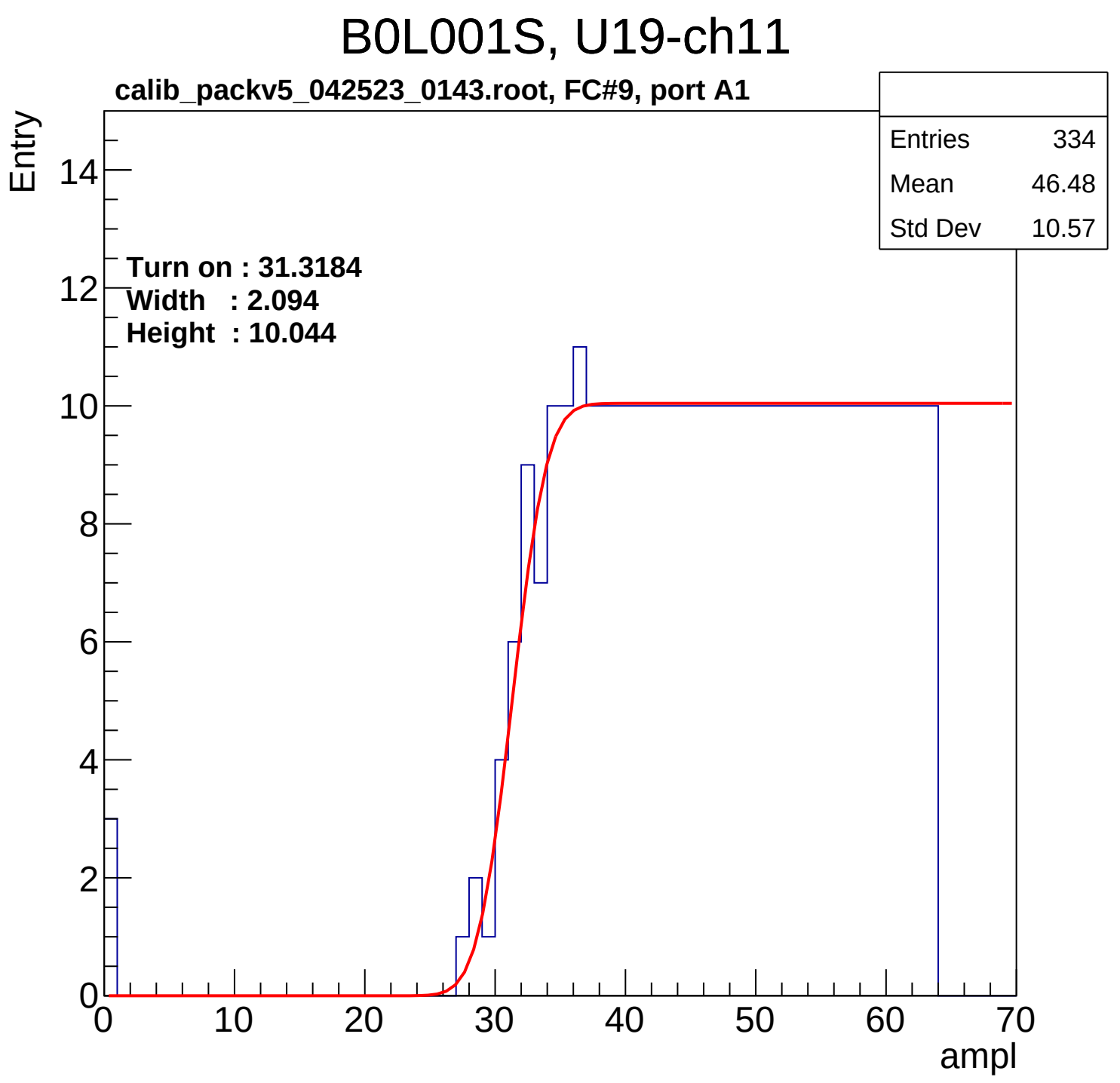
B0L001S, U19-ch11
calib_packv5_042523_0143.root, FC#9, port A1
Entries 334
Mean 46.48
Std Dev 10.57
Turn on : 31.3184
Width : 2.094
Height : 10.044
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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60
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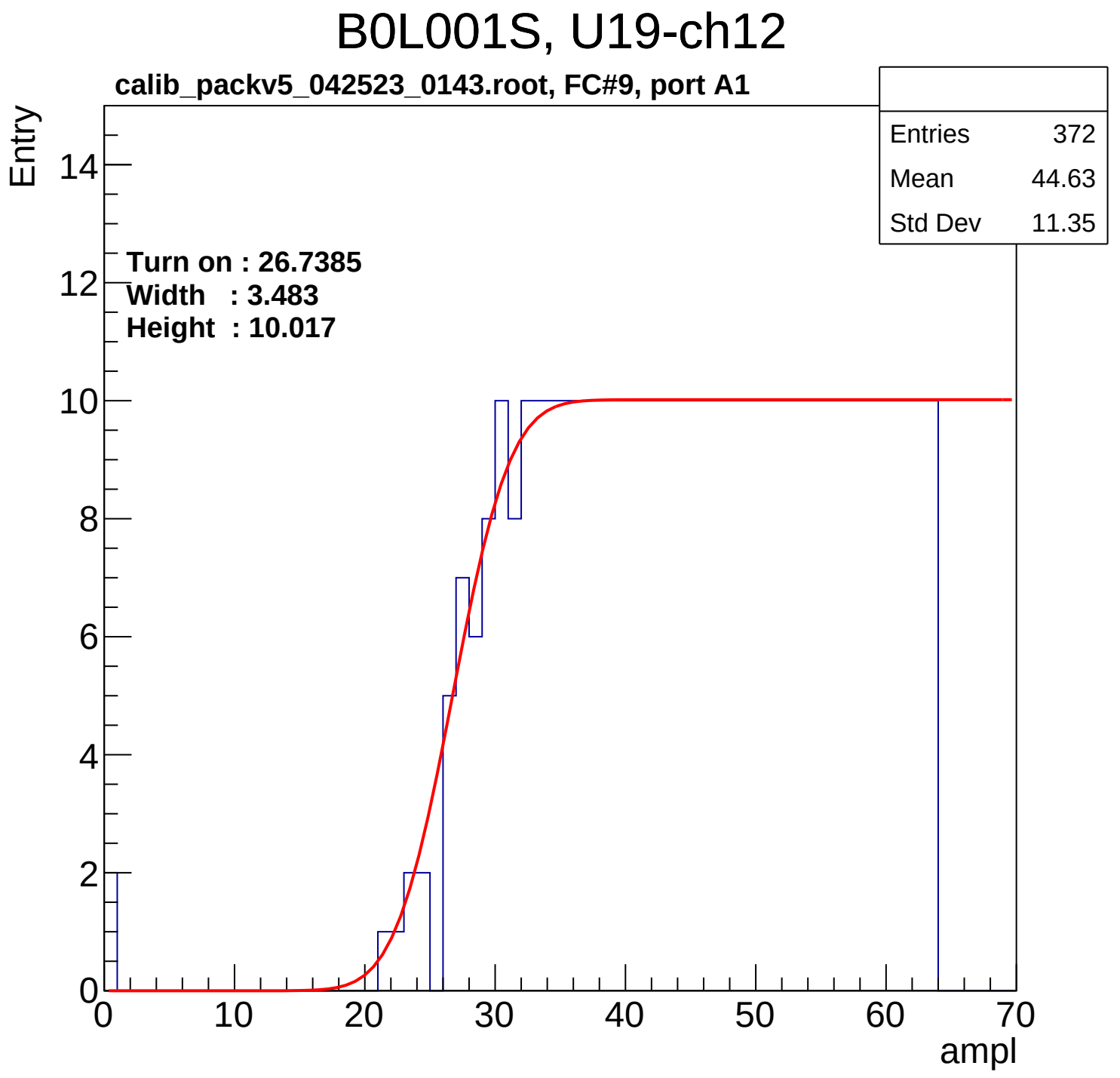
B0L001S, U19-ch12
calib_packv5_042523_0143.root, FC#9, port A1
Entries 372
Mean 44.63
Std Dev 11.35
Turn on : 26.7385
Width : 3.483
Height : 10.017
Entry
ampl
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4
6
8
10
12
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0
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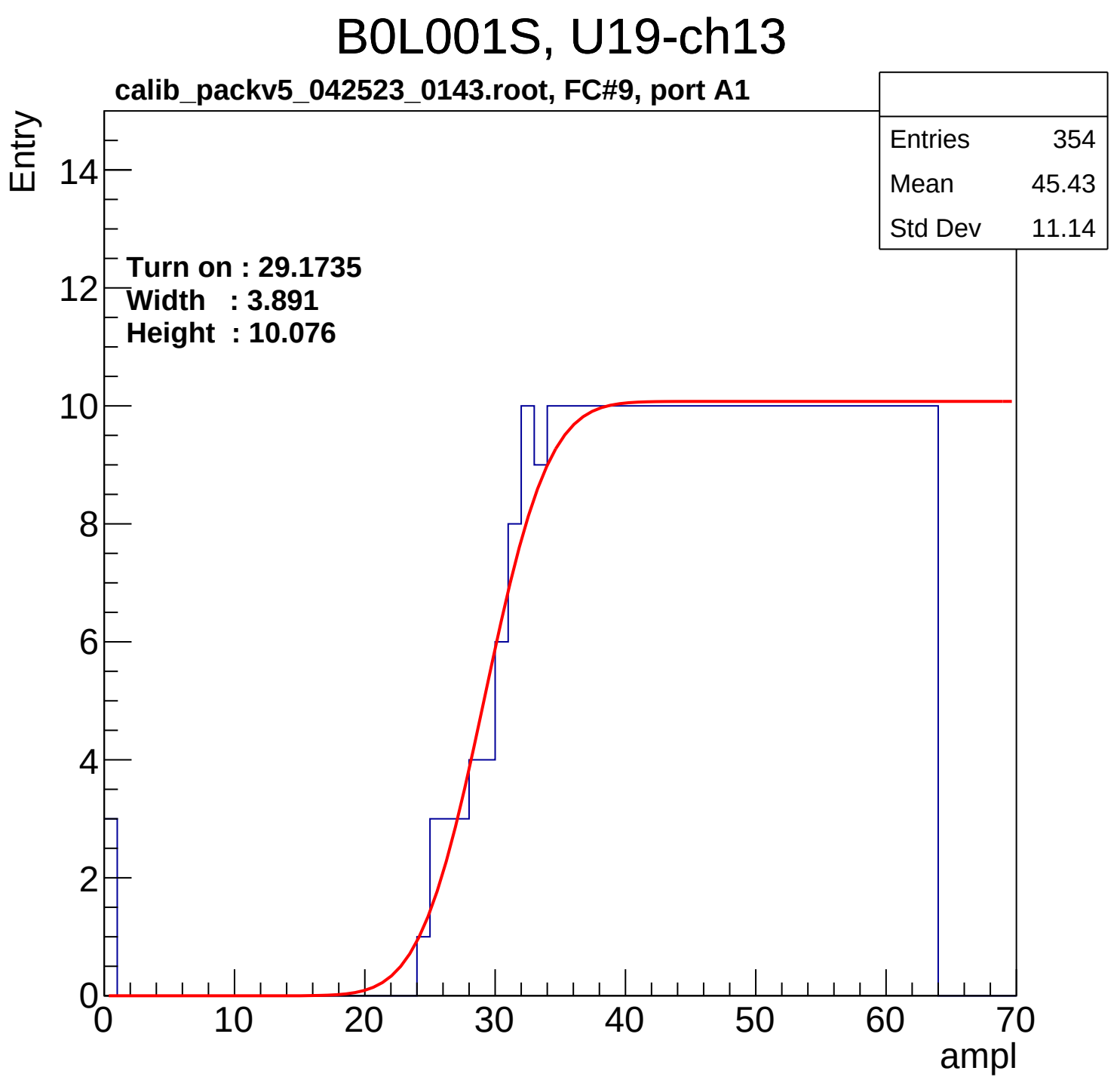
B0L001S, U19-ch13
calib_packv5_042523_0143.root, FC#9, port A1
Entries 354
Mean 45.43
Std Dev 11.14
Turn on : 29.1735
Width : 3.891
Height : 10.076
Entry
ampl
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6
8
10
12
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60
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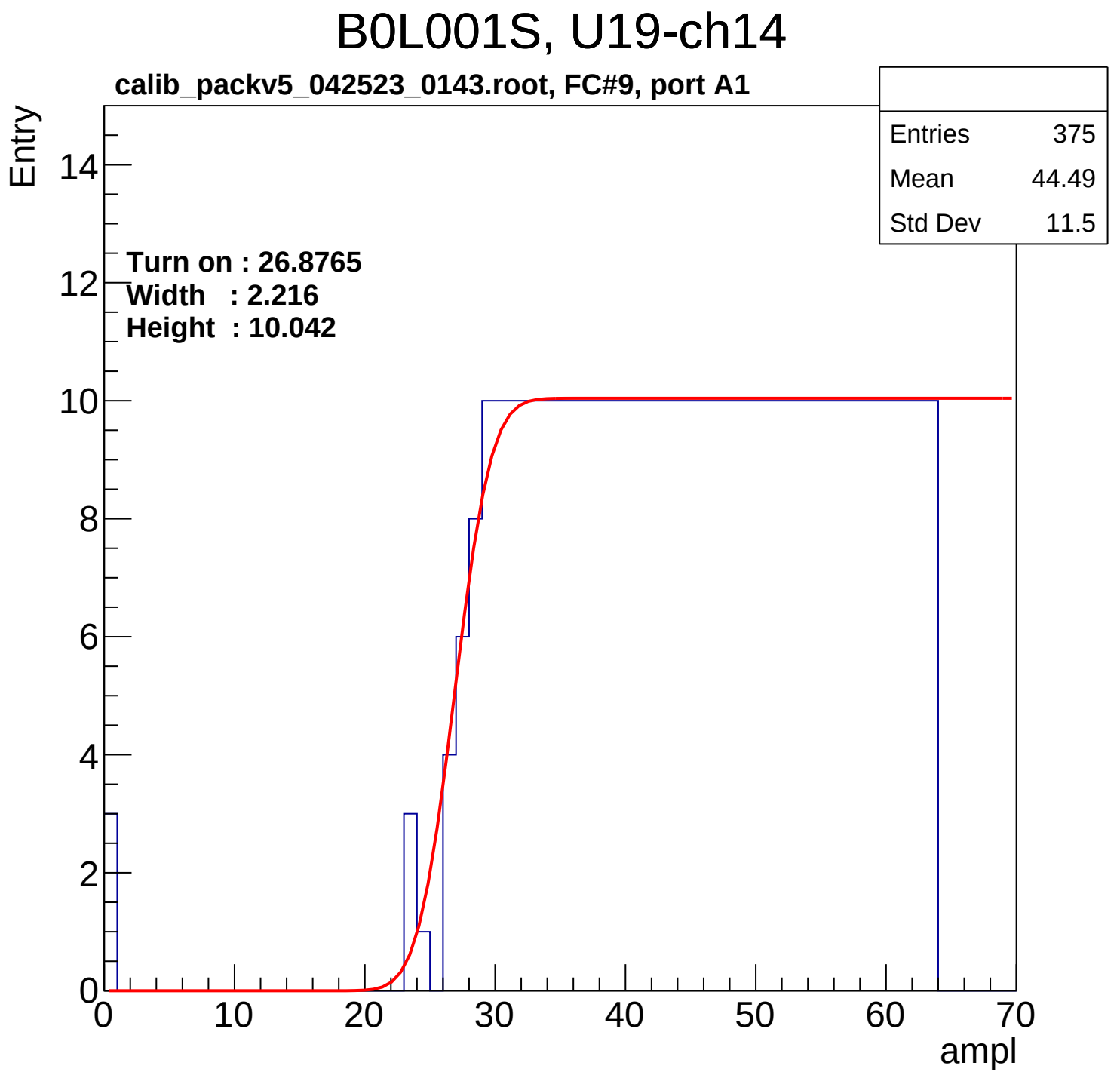
B0L001S, U19-ch14
calib_packv5_042523_0143.root, FC#9, port A1
Entries 375
Mean 44.49
Std Dev 11.5
Turn on : 26.8765
Width : 2.216
Height : 10.042
Entry
ampl
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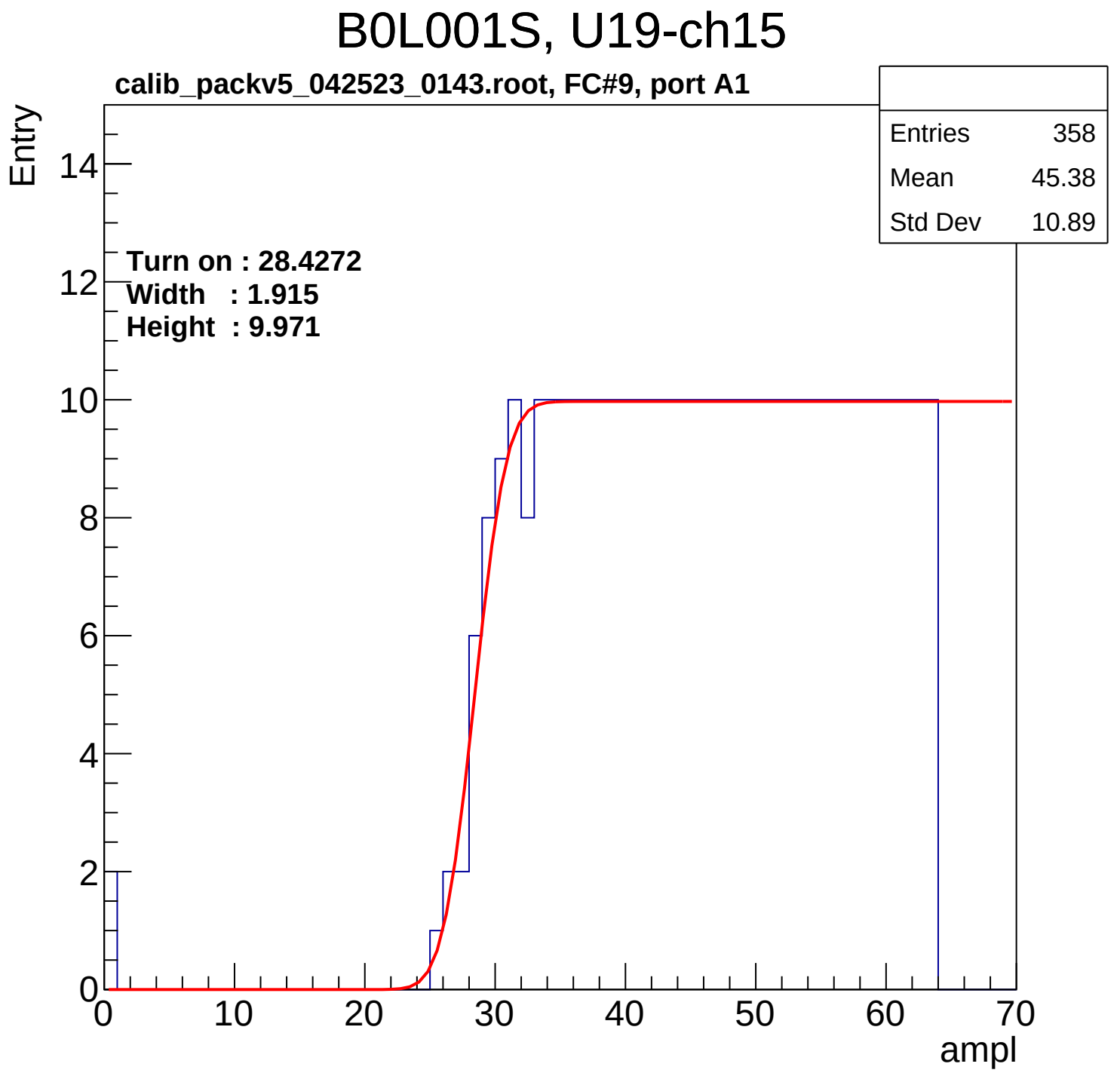
B0L001S, U19-ch15
calib_packv5_042523_0143.root, FC#9, port A1
Entries 358
Mean 45.38
Std Dev 10.89
Turn on : 28.4272
Width : 1.915
Height : 9.971
Entry
ampl
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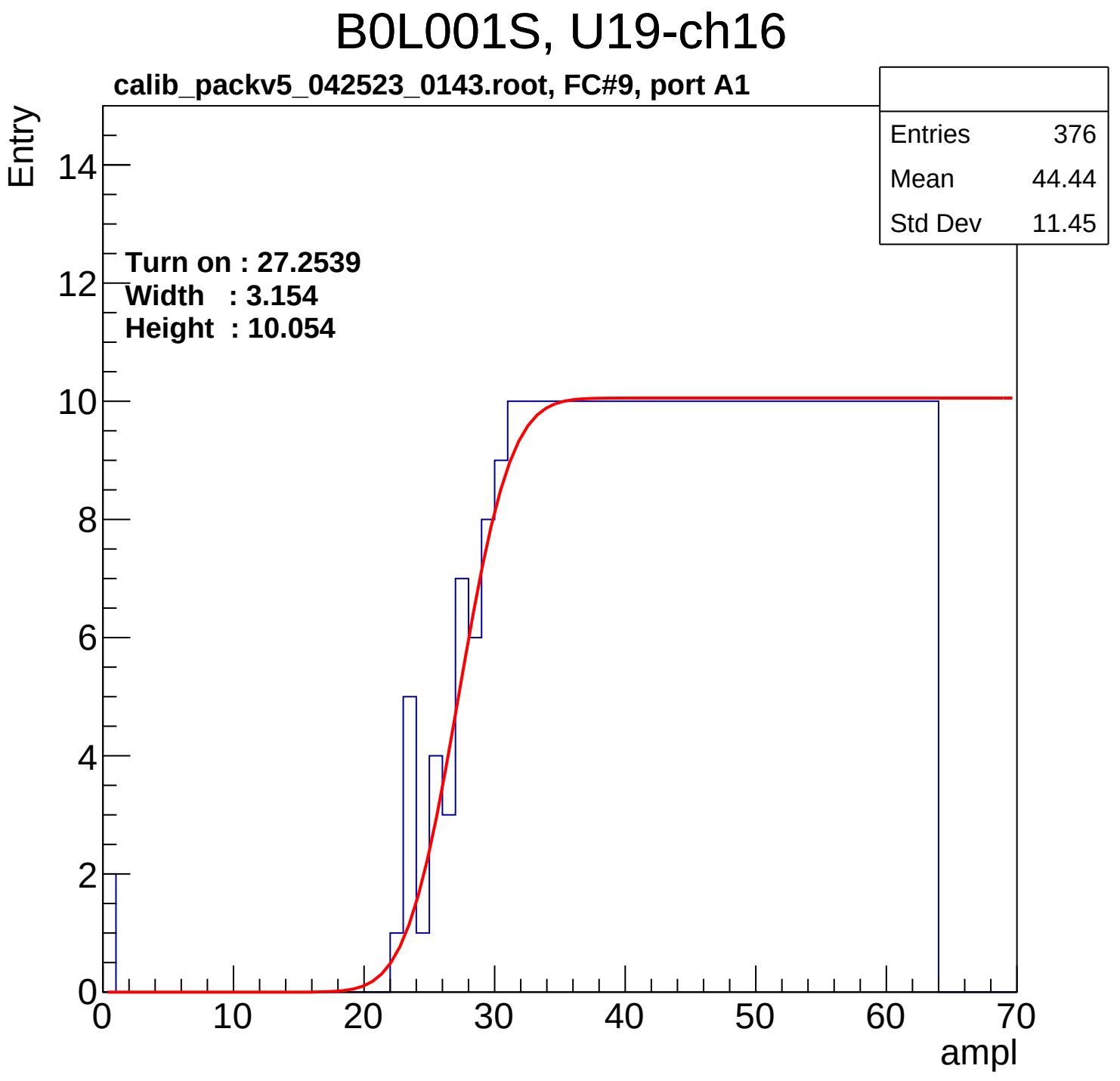
B0L001S, U19-ch16
calib_packv5_042523_0143.root, FC#9, port A1
Entries 376
Mean 44.44
Std Dev 11.45
Turn on : 27.2539
Width : 3.154
Height : 10.054
Entry
ampl
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8
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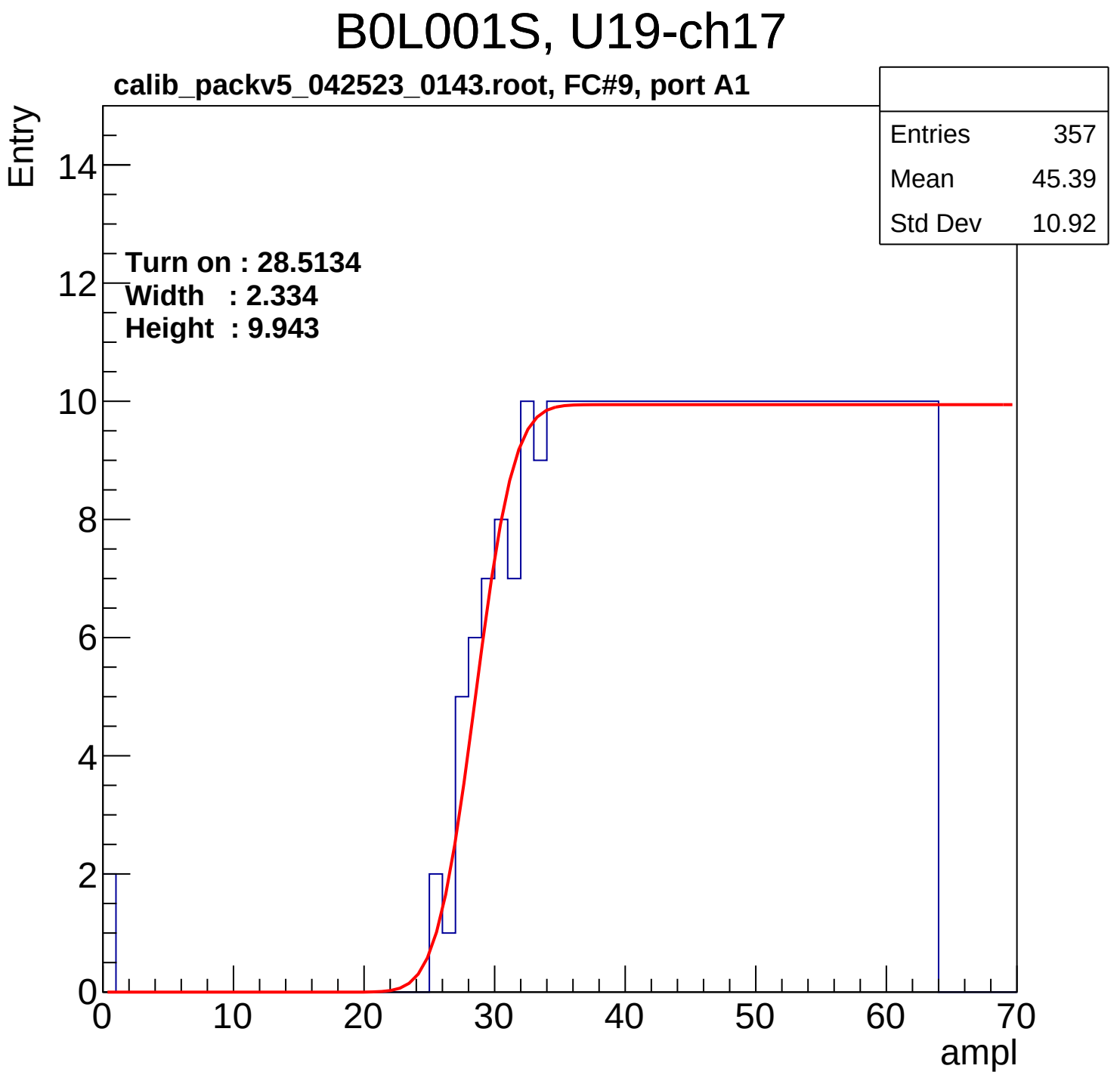
B0L001S, U19-ch17
calib_packv5_042523_0143.root, FC#9, port A1
Entries 357
Mean 45.39
Std Dev 10.92
Turn on : 28.5134
Width : 2.334
Height : 9.943
Entry
ampl
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6
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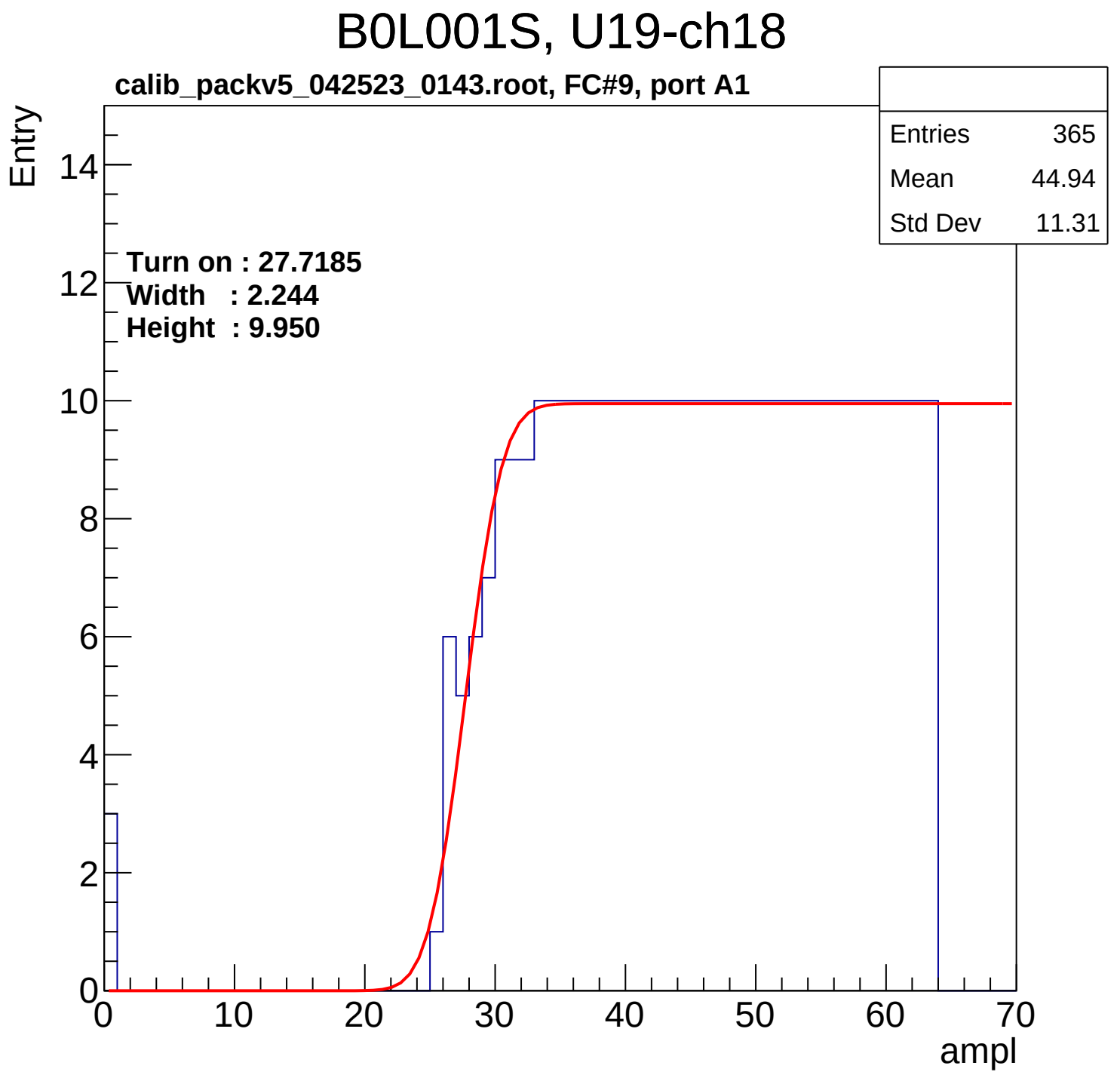
B0L001S, U19-ch18
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 44.94
Std Dev 11.31
Turn on : 27.7185
Width : 2.244
Height : 9.950
Entry
ampl
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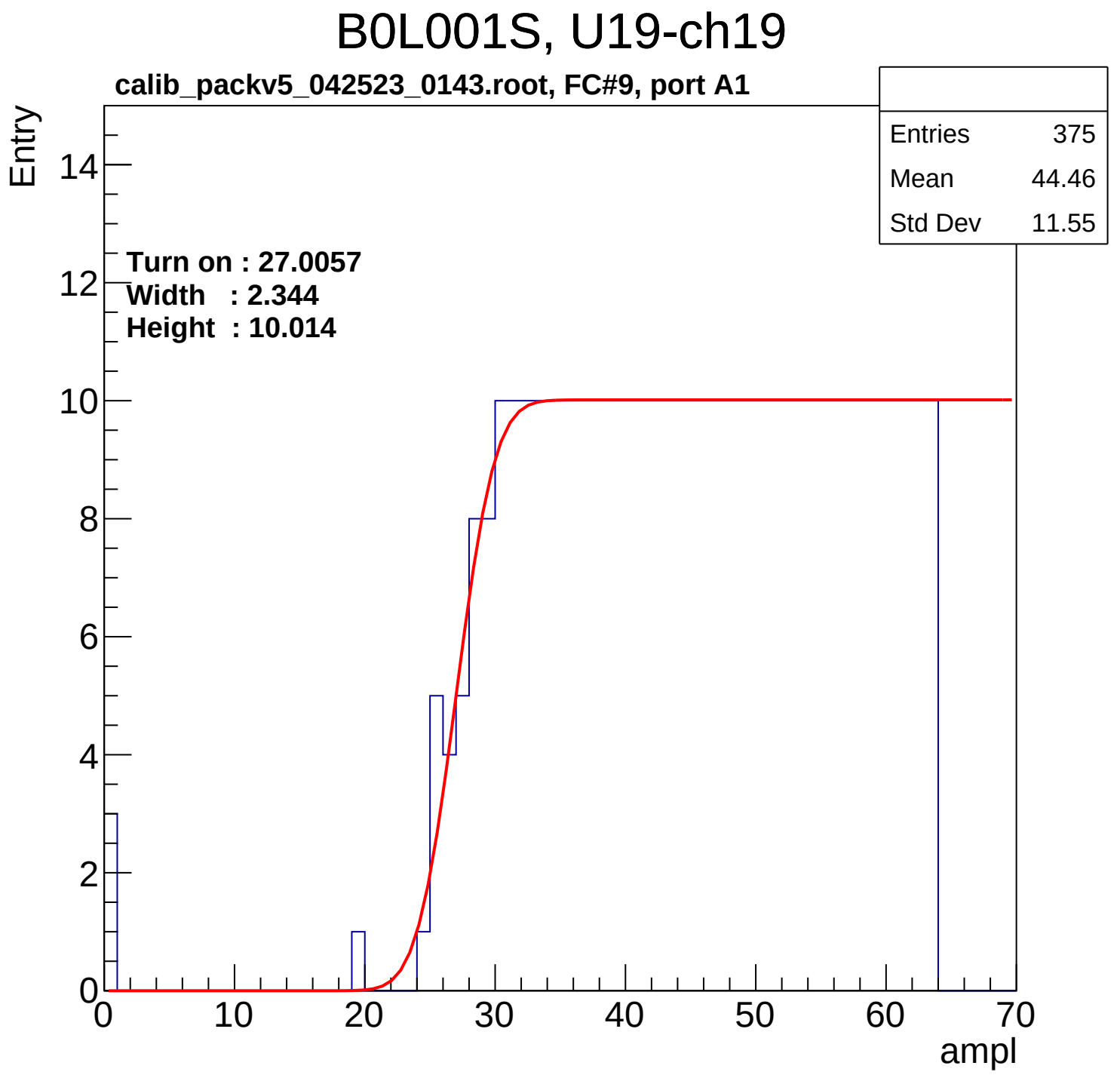
B0L001S, U19-ch19
calib_packv5_042523_0143.root, FC#9, port A1
Entries 375
Mean 44.46
Std Dev 11.55
Turn on : 27.0057
Width : 2.344
Height : 10.014
Entry
ampl
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6
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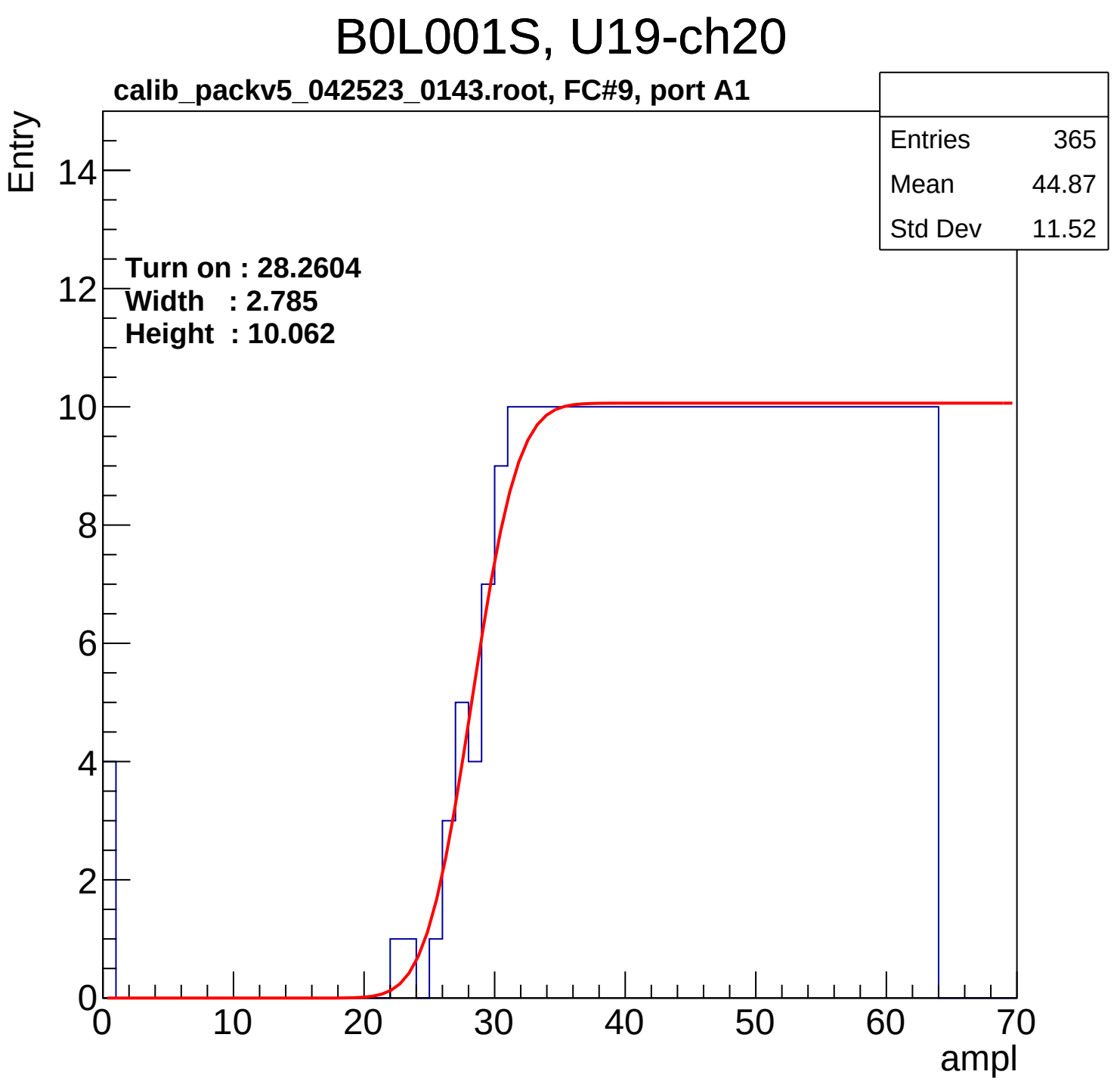
B0L001S, U19-ch20
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 44.87
Std Dev 11.52
Turn on : 28.2604
Width : 2.785
Height : 10.062
Entry
ampl
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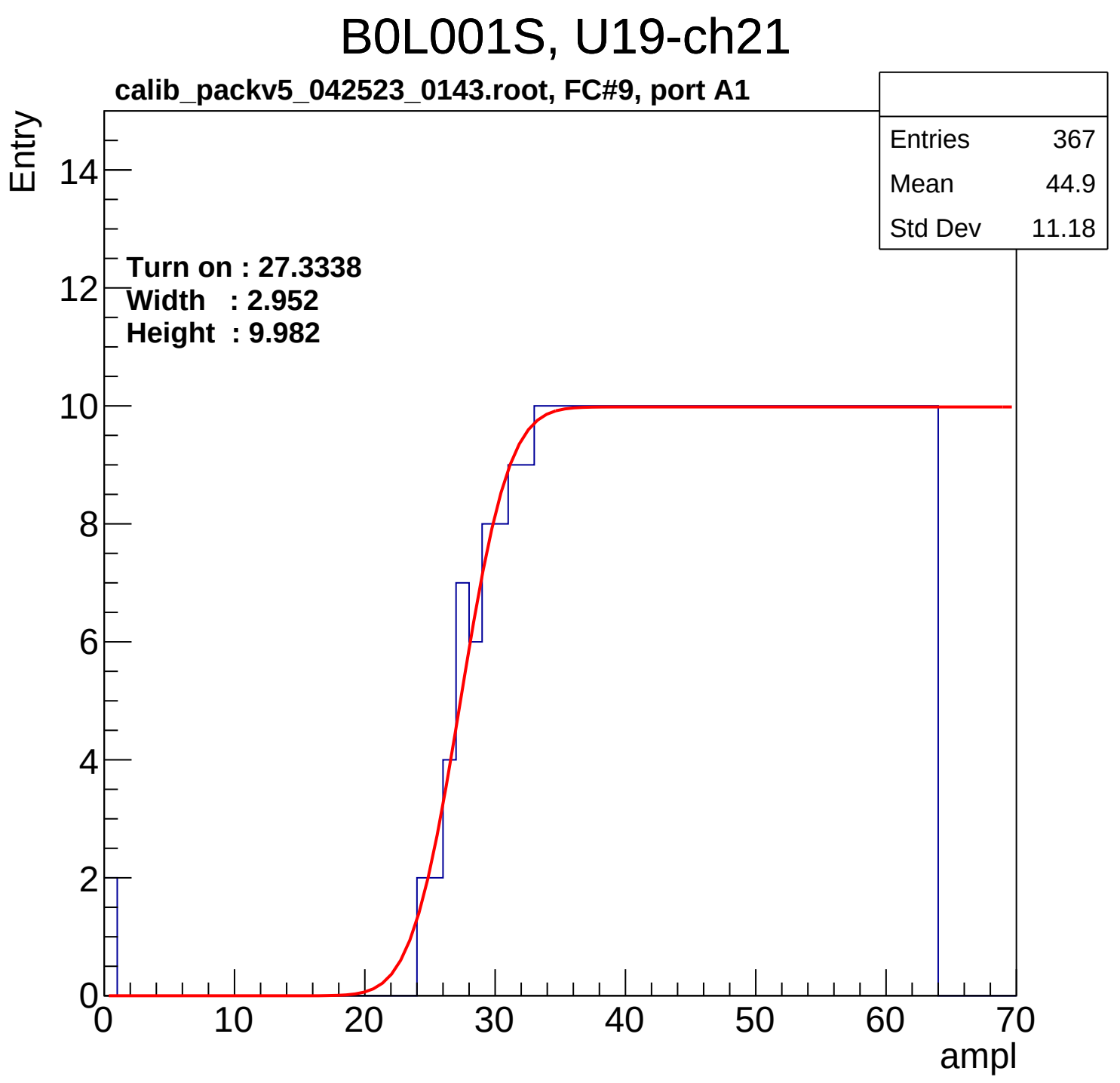
B0L001S, U19-ch21
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.9
Std Dev 11.18
Turn on : 27.3338
Width : 2.952
Height : 9.982
Entry
ampl
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2
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6
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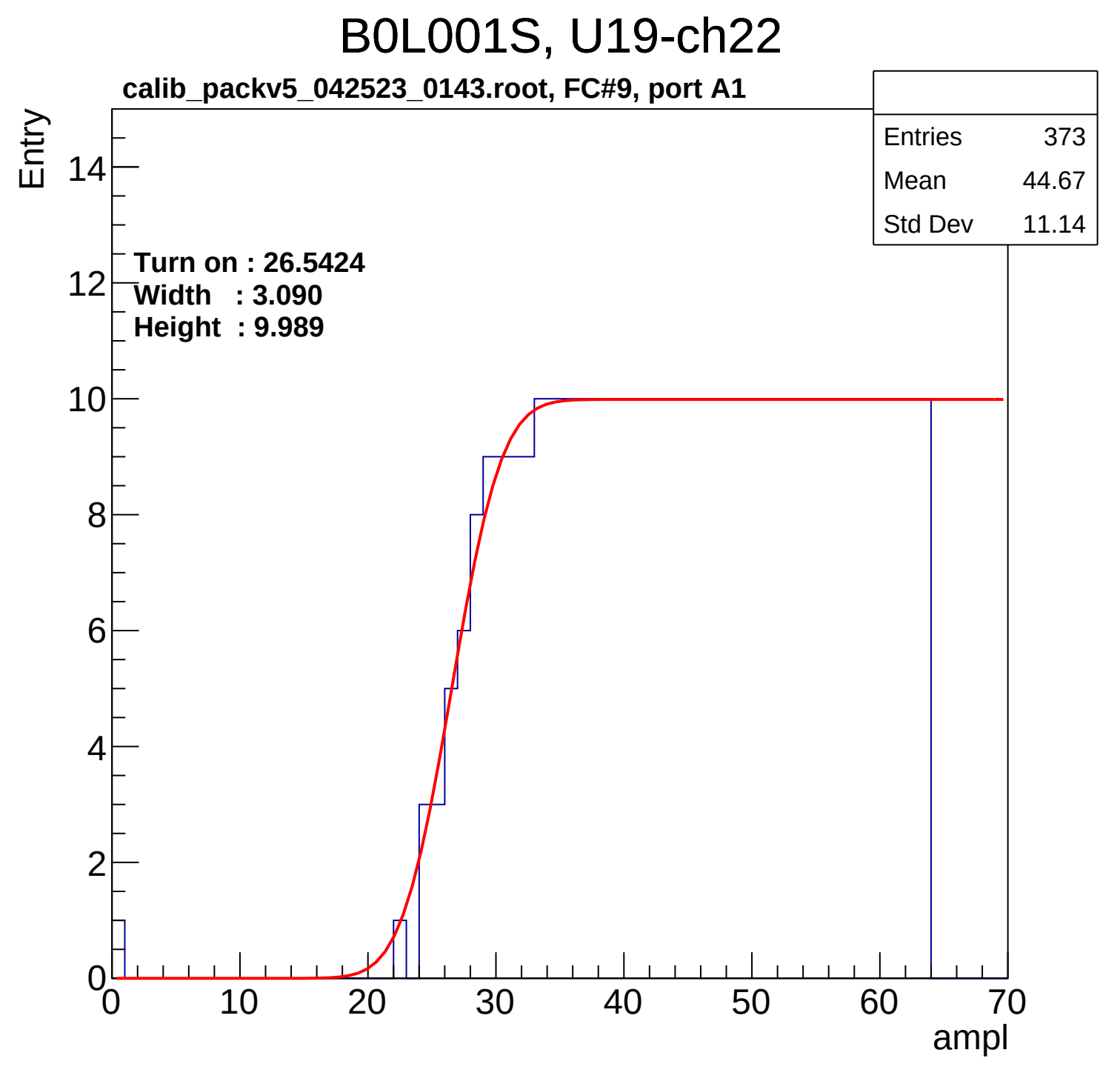
B0L001S, U19-ch22
calib_packv5_042523_0143.root, FC#9, port A1
Entries 373
Mean 44.67
Std Dev 11.14
Turn on : 26.5424
Width : 3.090
Height : 9.989
Entry
ampl
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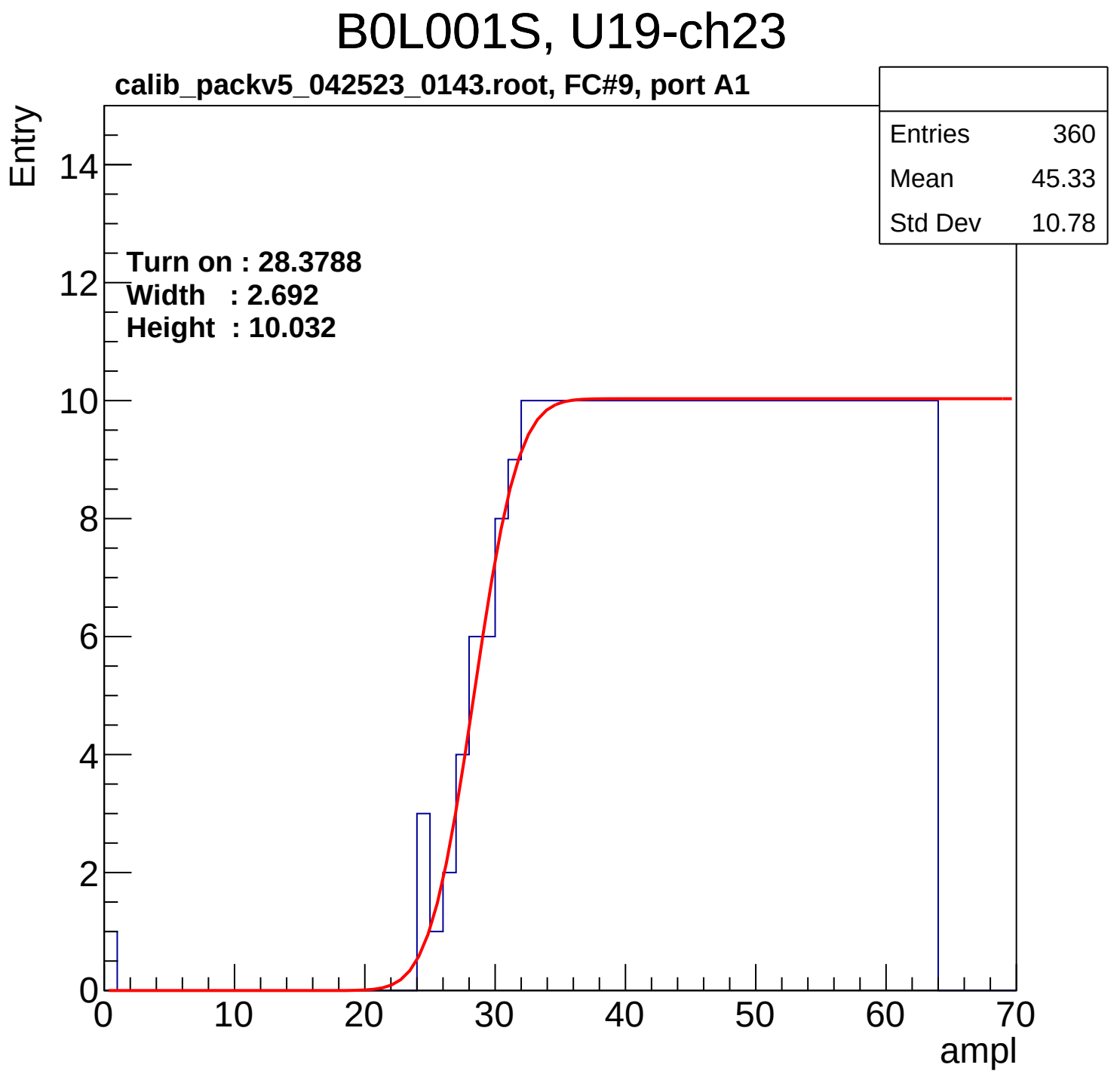
B0L001S, U19-ch23
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 45.33
Std Dev 10.78
Turn on : 28.3788
Width : 2.692
Height : 10.032
Entry
ampl
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6
8
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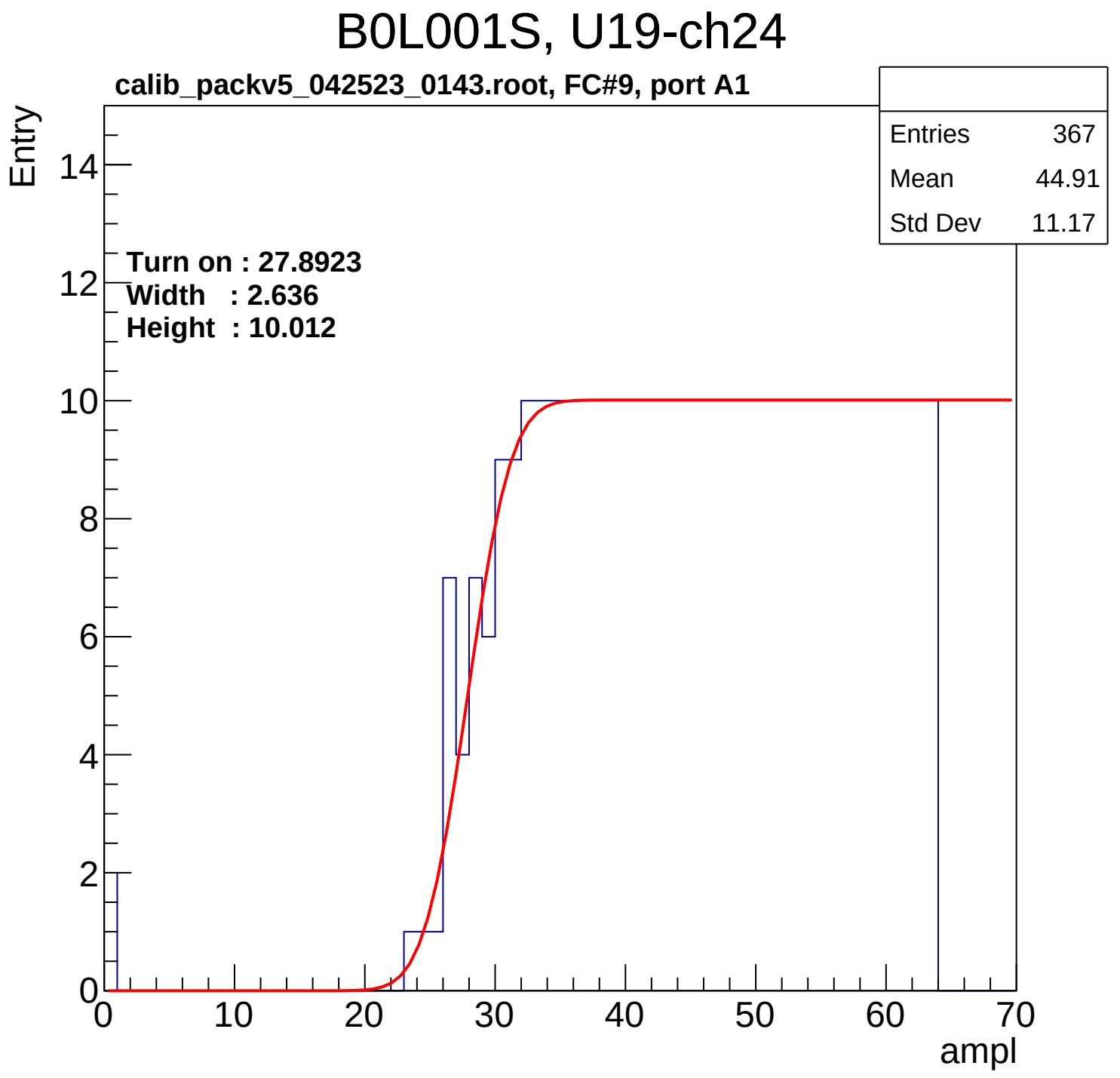
B0L001S, U19-ch24
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.91
Std Dev 11.17
Turn on : 27.8923
Width : 2.636
Height : 10.012
Entry
ampl
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4
6
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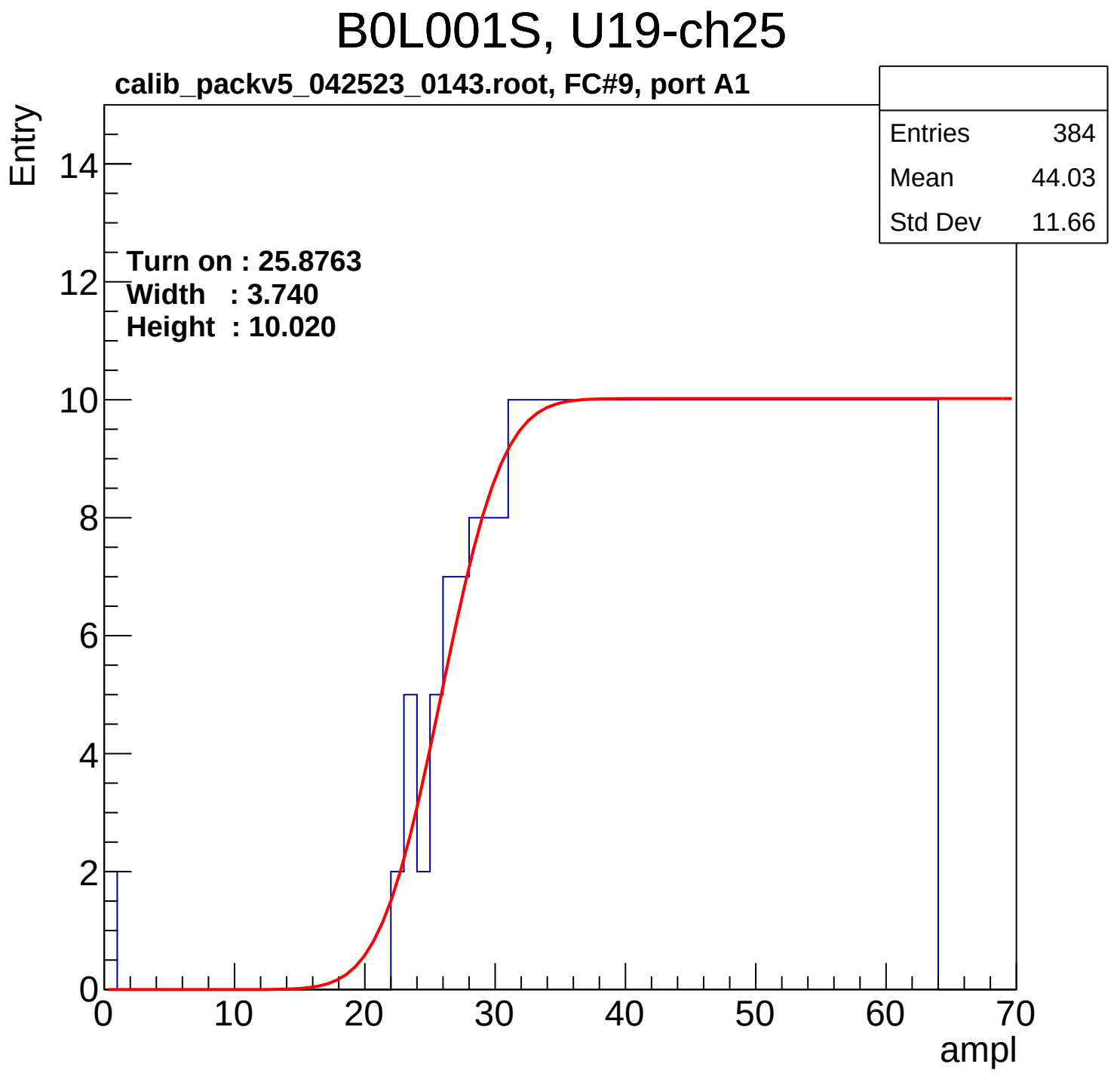
B0L001S, U19-ch25
calib_packv5_042523_0143.root, FC#9, port A1
Entries 384
Mean 44.03
Std Dev 11.66
Turn on : 25.8763
Width : 3.740
Height : 10.020
Entry
ampl
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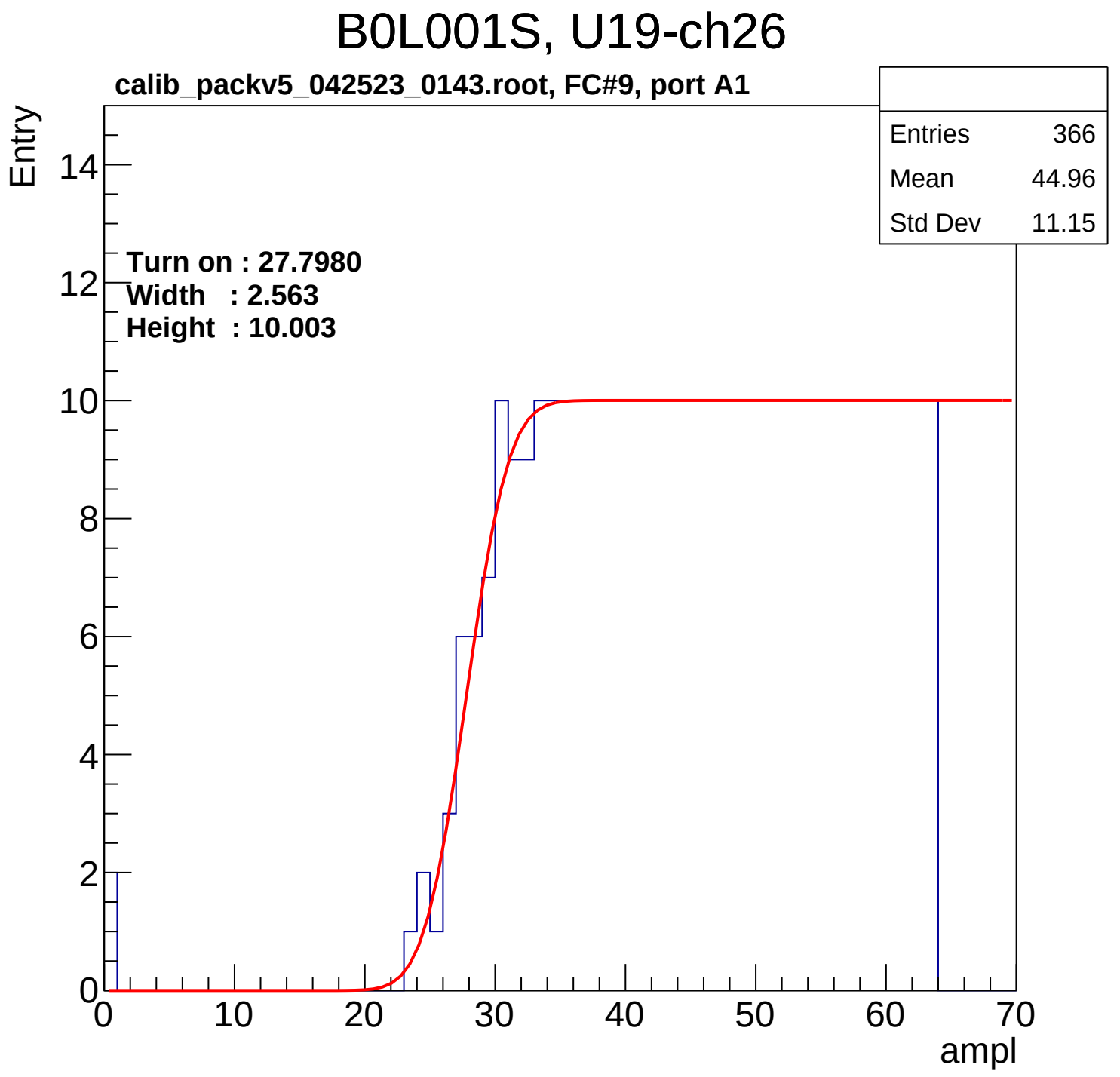
B0L001S, U19-ch26
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.96
Std Dev 11.15
Turn on : 27.7980
Width : 2.563
Height : 10.003
Entry
ampl
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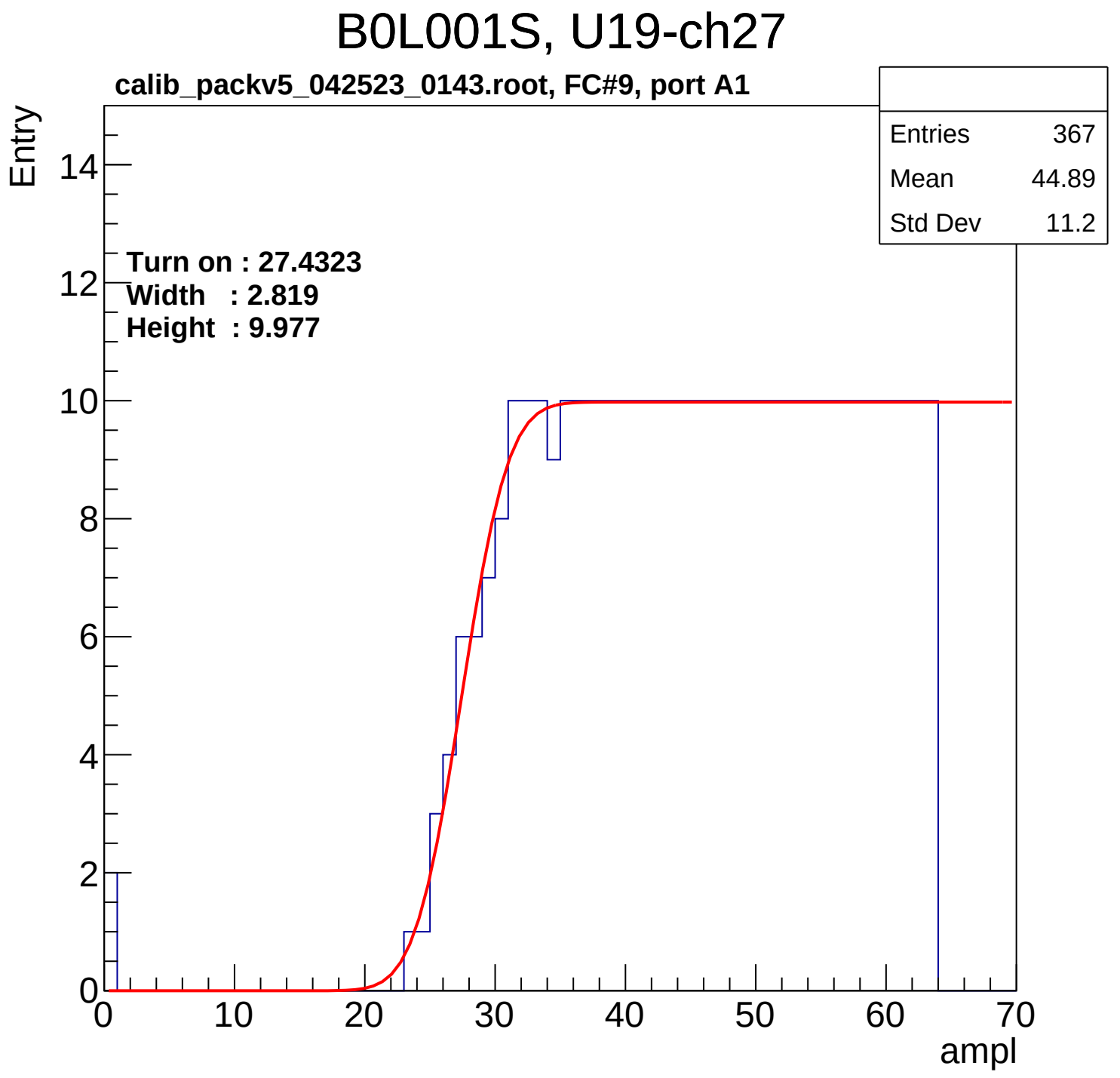
B0L001S, U19-ch27
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.89
Std Dev 11.2
Turn on : 27.4323
Width : 2.819
Height : 9.977
Entry
ampl
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8
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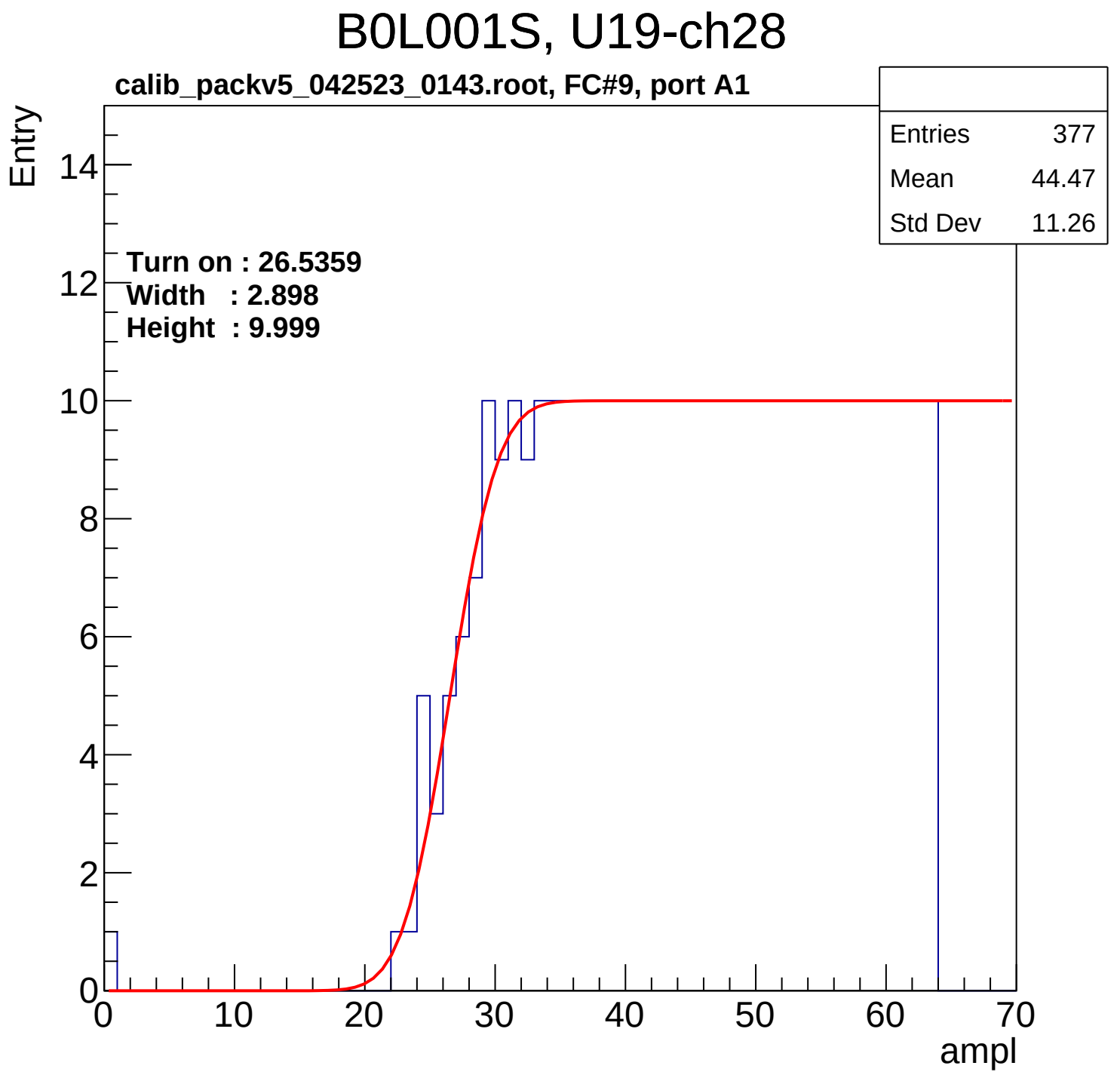
B0L001S, U19-ch28
calib_packv5_042523_0143.root, FC#9, port A1
Entries 377
Mean 44.47
Std Dev 11.26
Turn on : 26.5359
Width : 2.898
Height : 9.999
Entry
ampl
0
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4
6
8
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12
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10
20
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50
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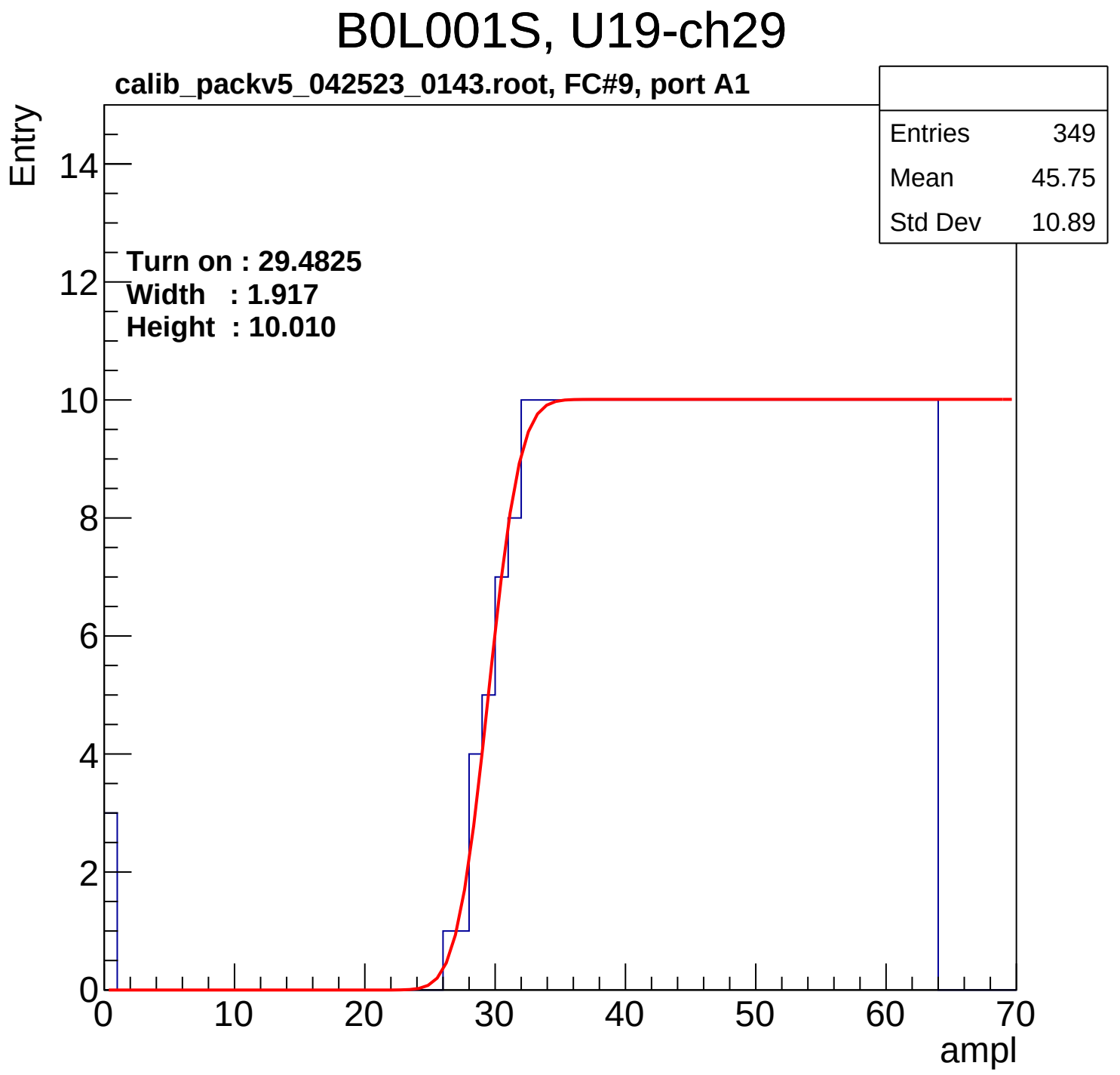
B0L001S, U19-ch29
calib_packv5_042523_0143.root, FC#9, port A1
Entries 349
Mean 45.75
Std Dev 10.89
Turn on : 29.4825
Width : 1.917
Height : 10.010
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ampl
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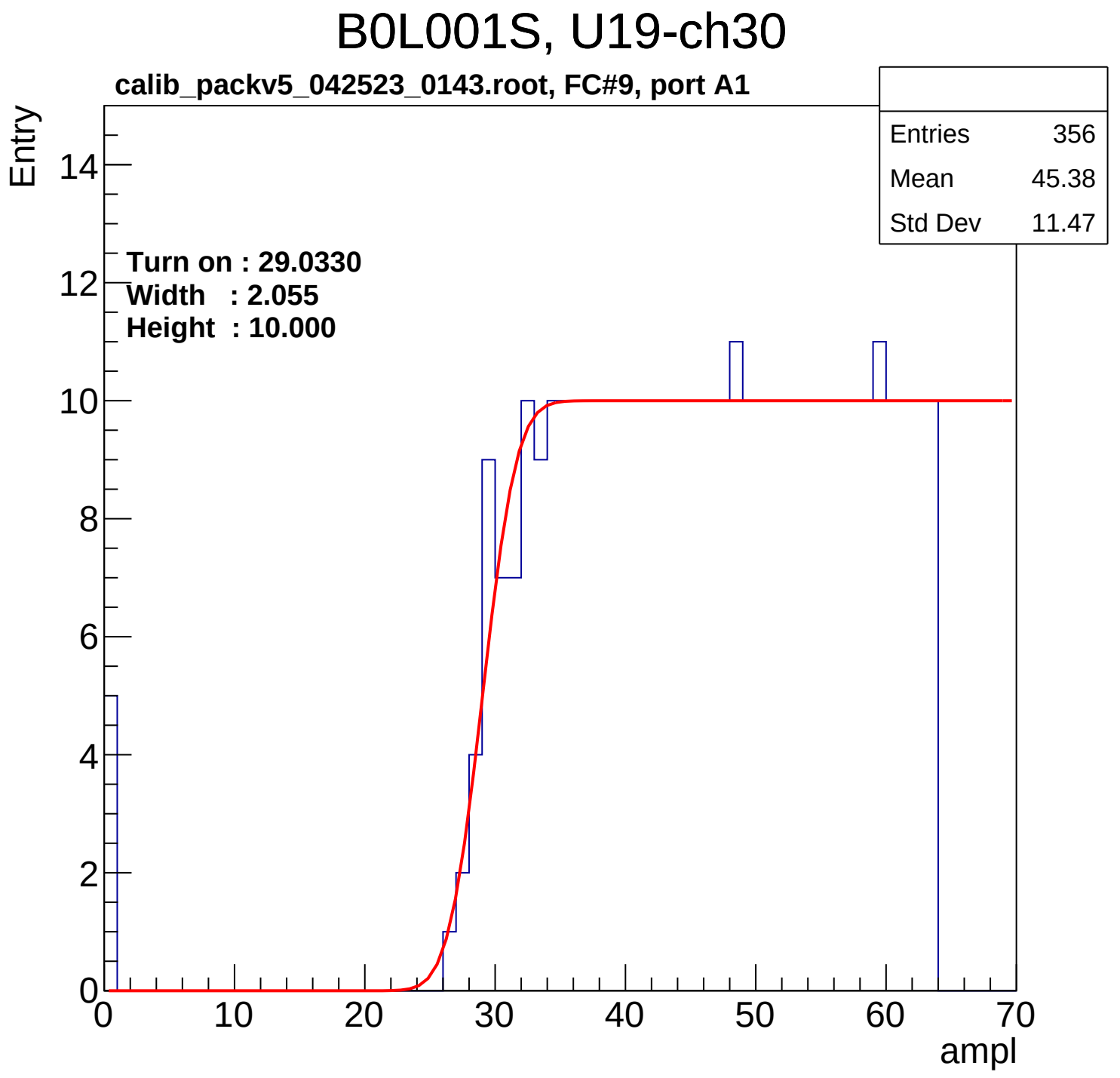
B0L001S, U19-ch30
calib_packv5_042523_0143.root, FC#9, port A1
Entries 356
Mean 45.38
Std Dev 11.47
Turn on : 29.0330
Width : 2.055
Height : 10.000
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ampl
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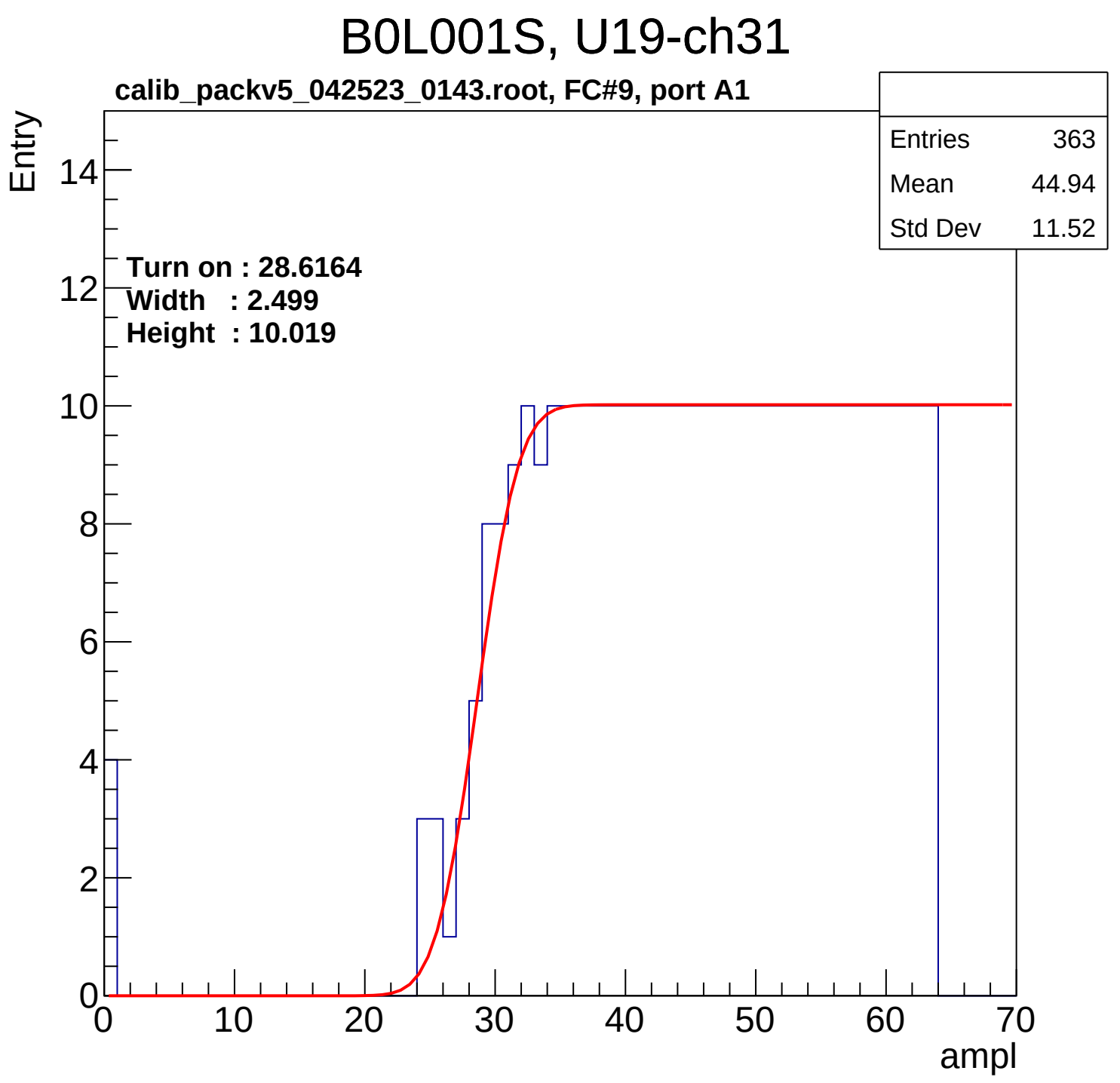
B0L001S, U19-ch31
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 44.94
Std Dev 11.52
Turn on : 28.6164
Width : 2.499
Height : 10.019
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ampl
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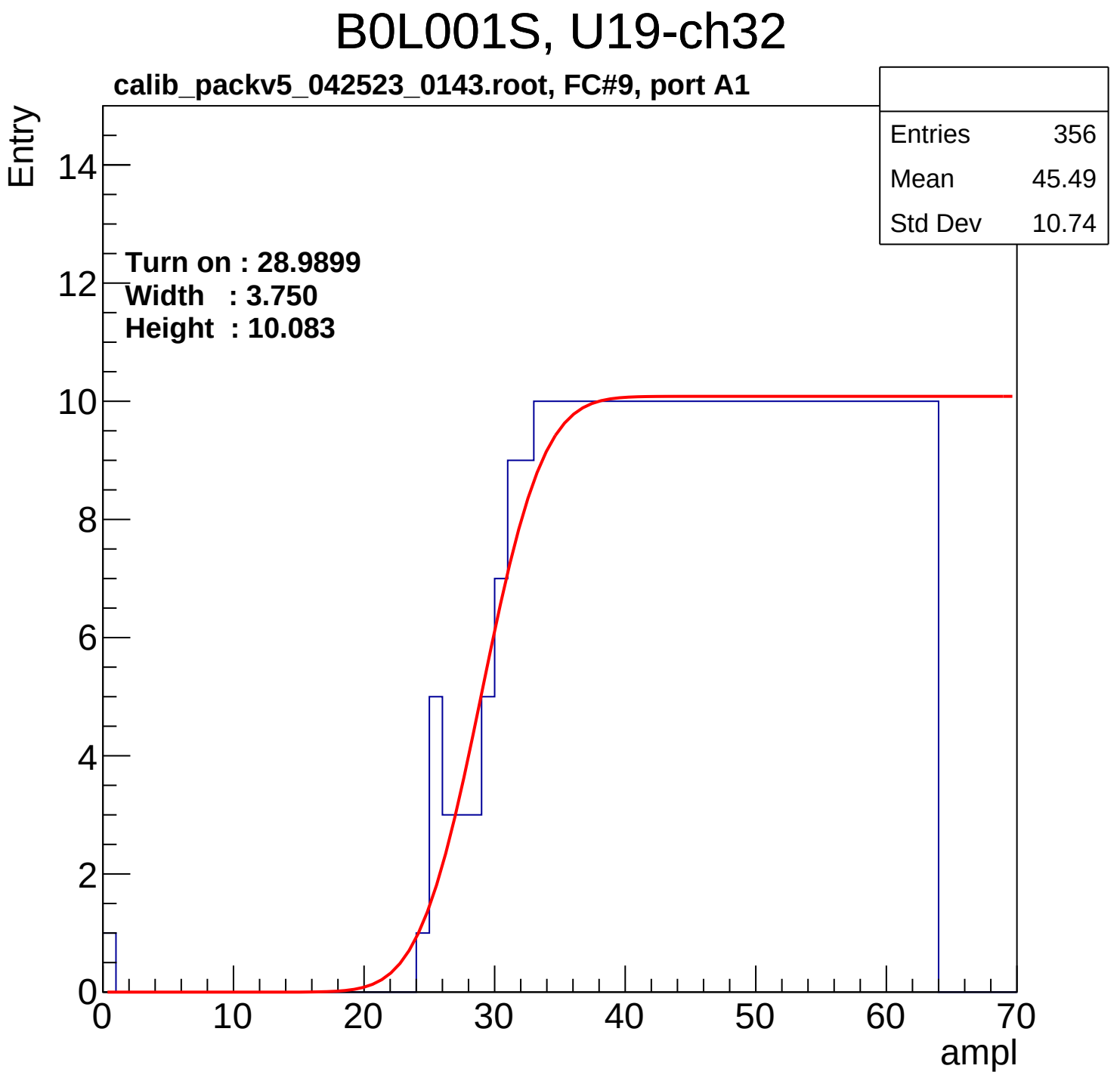
B0L001S, U19-ch32
calib_packv5_042523_0143.root, FC#9, port A1
Entries 356
Mean 45.49
Std Dev 10.74
Turn on : 28.9899
Width : 3.750
Height : 10.083
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ampl
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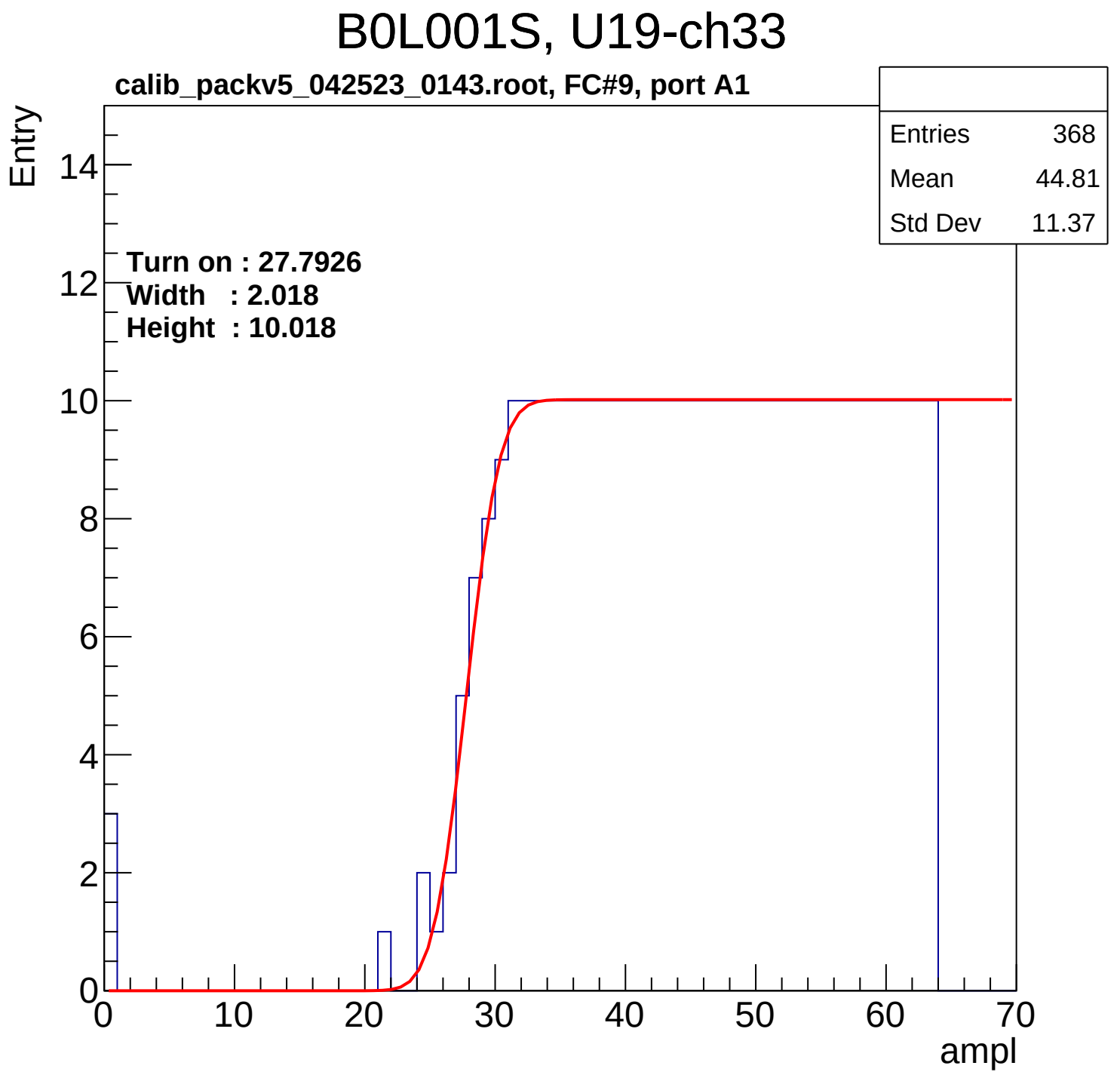
B0L001S, U19-ch33
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.81
Std Dev 11.37
Turn on : 27.7926
Width : 2.018
Height : 10.018
Entry
ampl
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2
4
6
8
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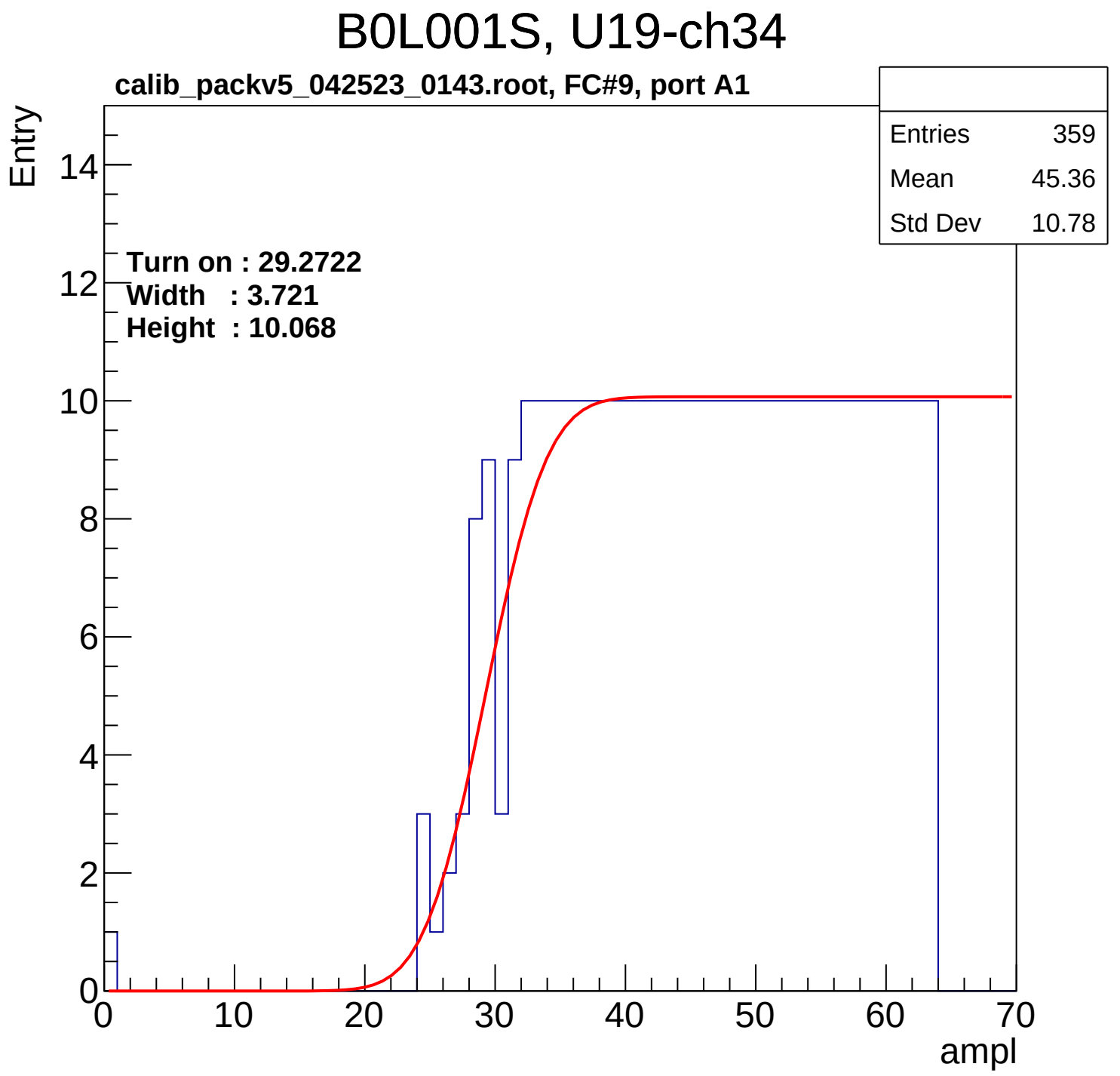
B0L001S, U19-ch34
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 45.36
Std Dev 10.78
Turn on : 29.2722
Width : 3.721
Height : 10.068
Entry
ampl
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2
4
6
8
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0
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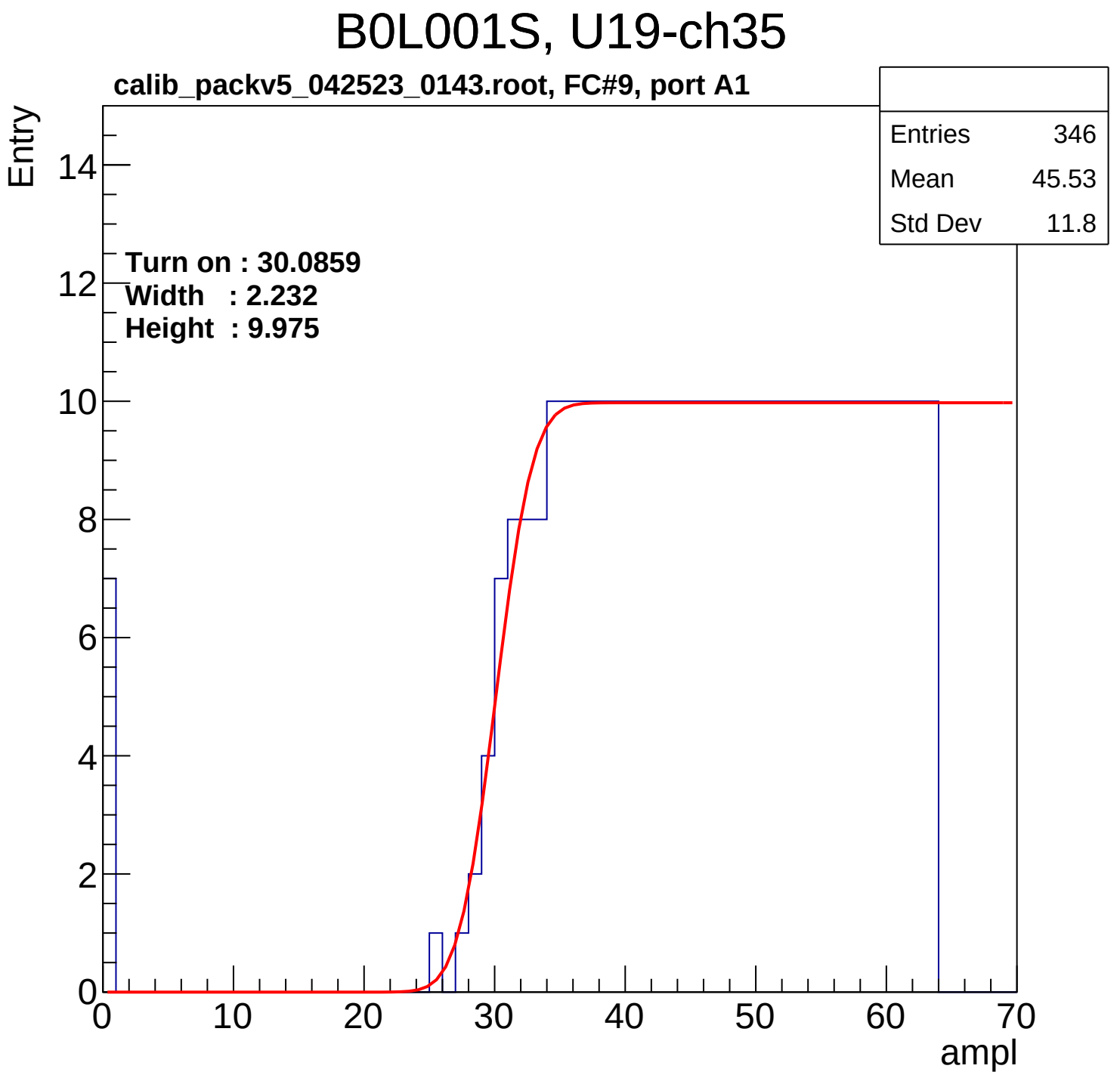
B0L001S, U19-ch35
calib_packv5_042523_0143.root, FC#9, port A1
Entries 346
Mean 45.53
Std Dev 11.8
Turn on : 30.0859
Width : 2.232
Height : 9.975
Entry
ampl
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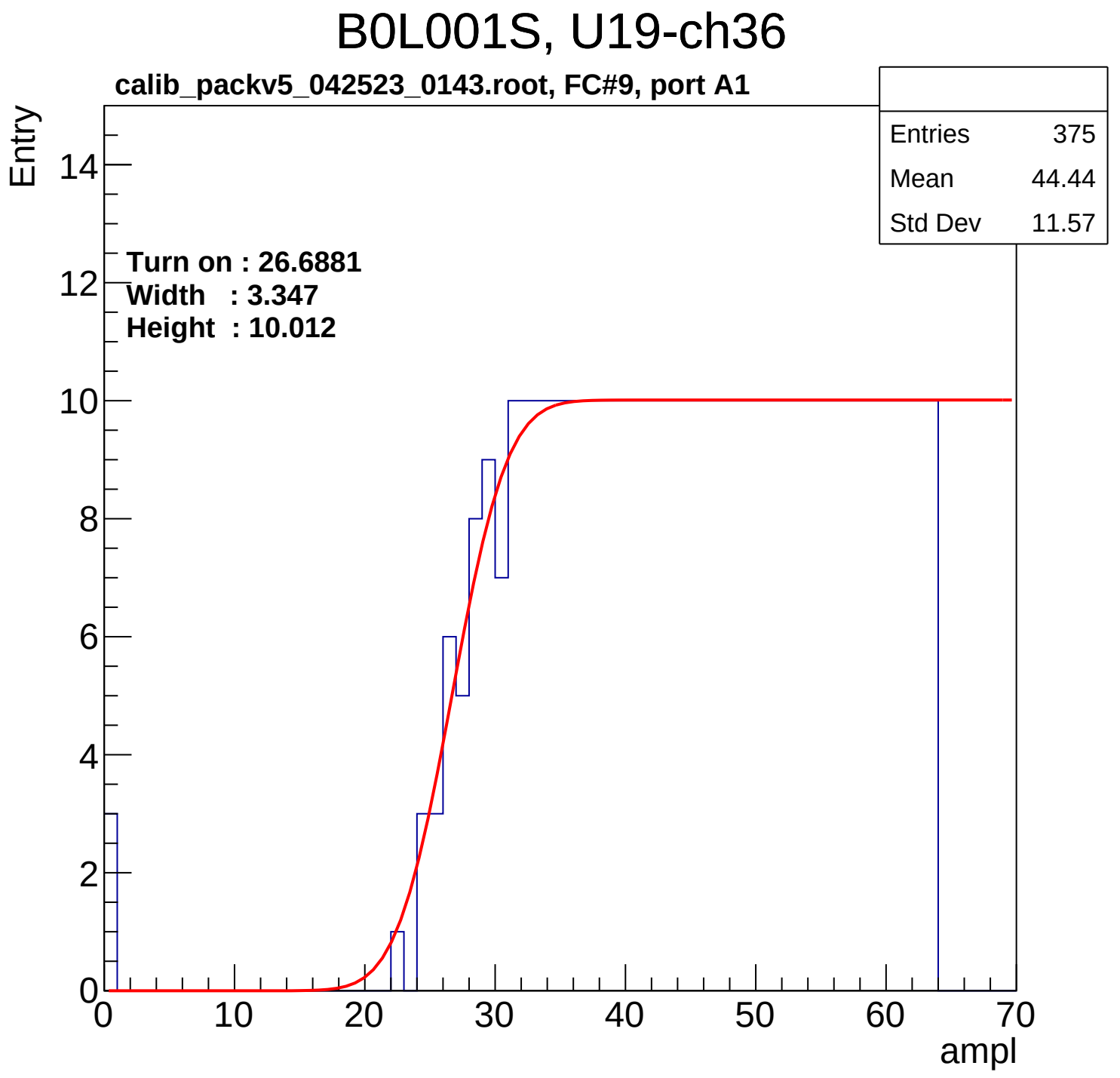
B0L001S, U19-ch36
calib_packv5_042523_0143.root, FC#9, port A1
Entries 375
Mean 44.44
Std Dev 11.57
Turn on : 26.6881
Width : 3.347
Height : 10.012
Entry
ampl
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2
4
6
8
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12
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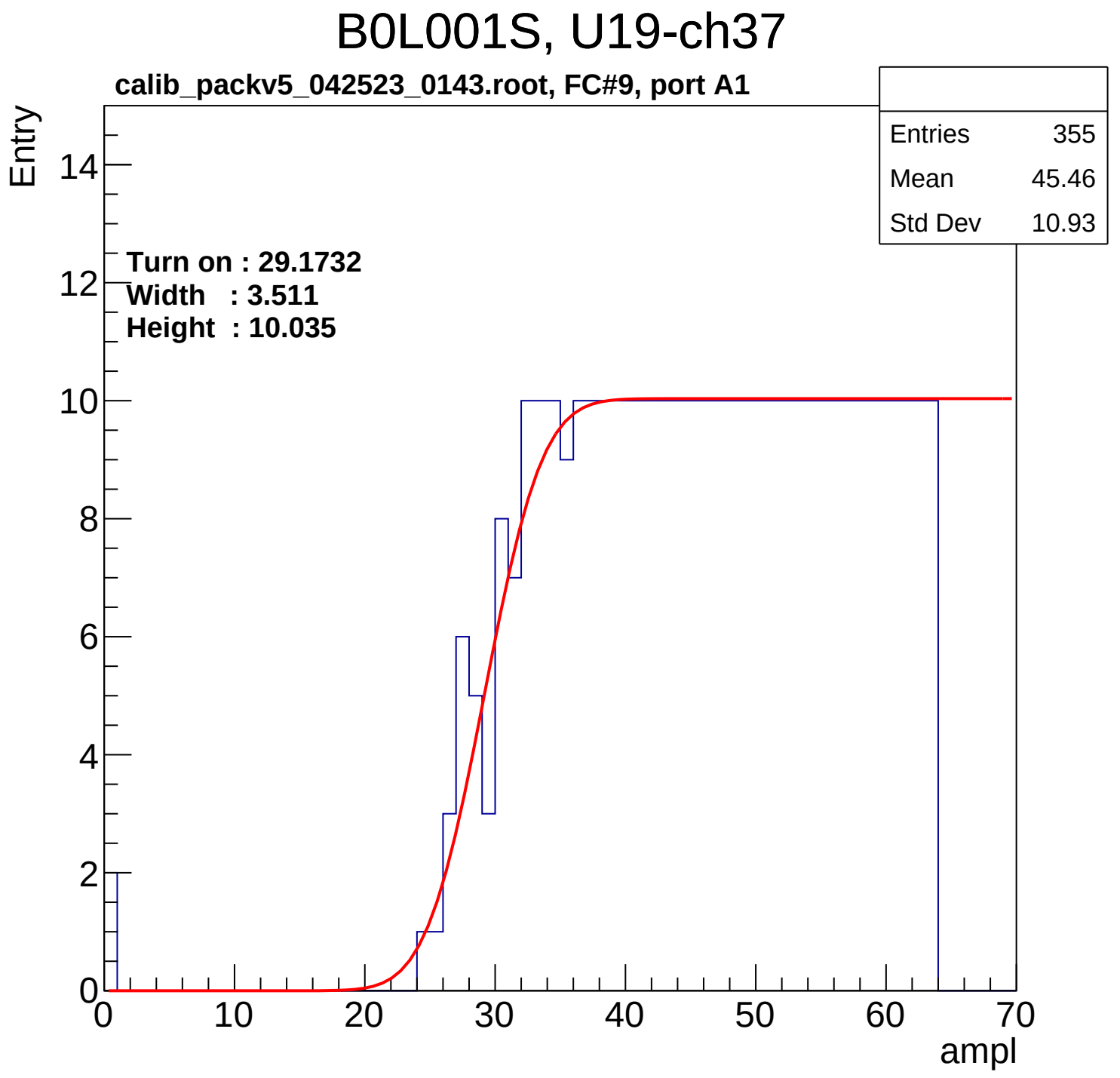
B0L001S, U19-ch37
calib_packv5_042523_0143.root, FC#9, port A1
Entries 355
Mean 45.46
Std Dev 10.93
Turn on : 29.1732
Width : 3.511
Height : 10.035
Entry
ampl
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6
8
10
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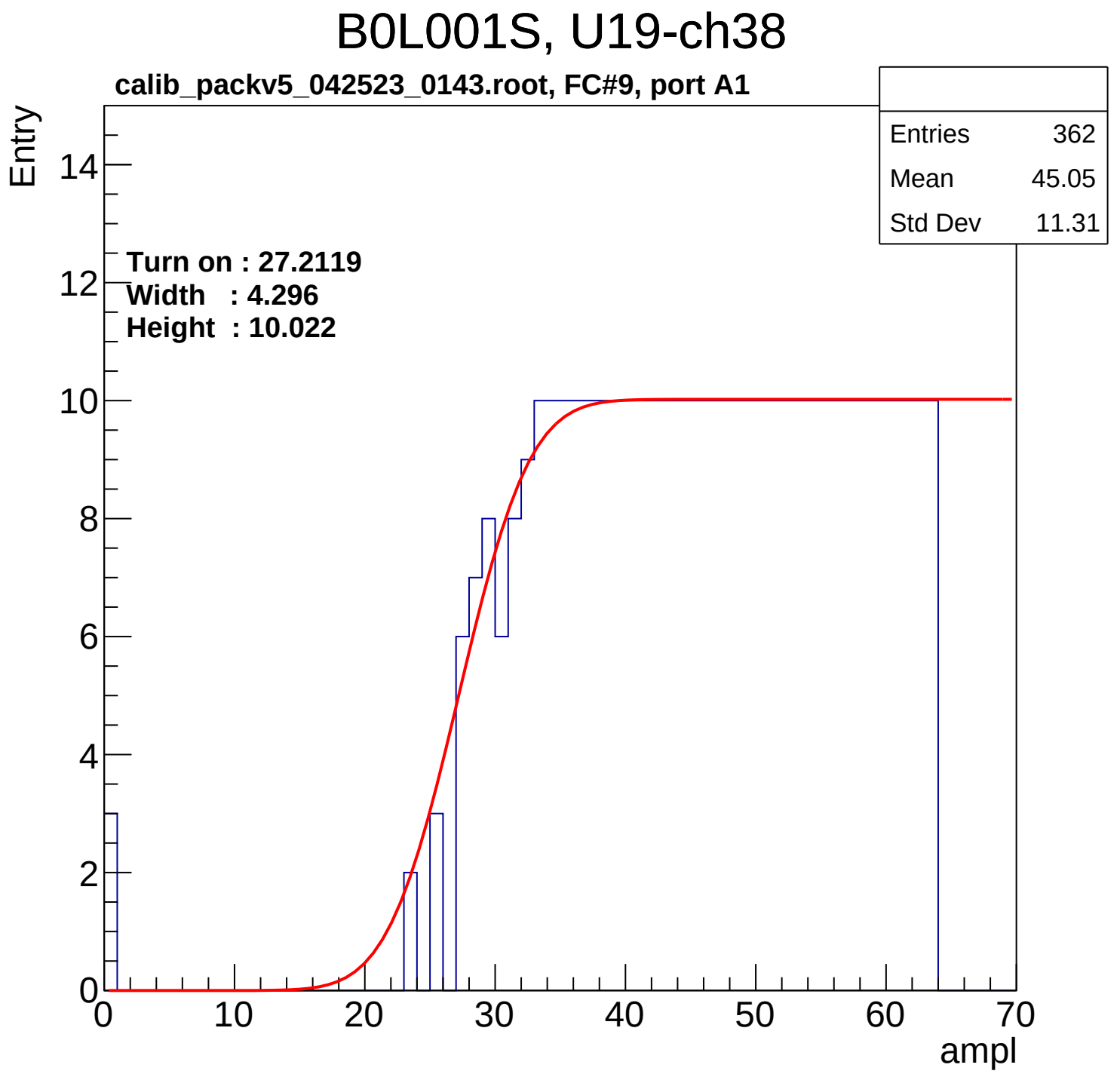
B0L001S, U19-ch38
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 45.05
Std Dev 11.31
Turn on : 27.2119
Width : 4.296
Height : 10.022
Entry
ampl
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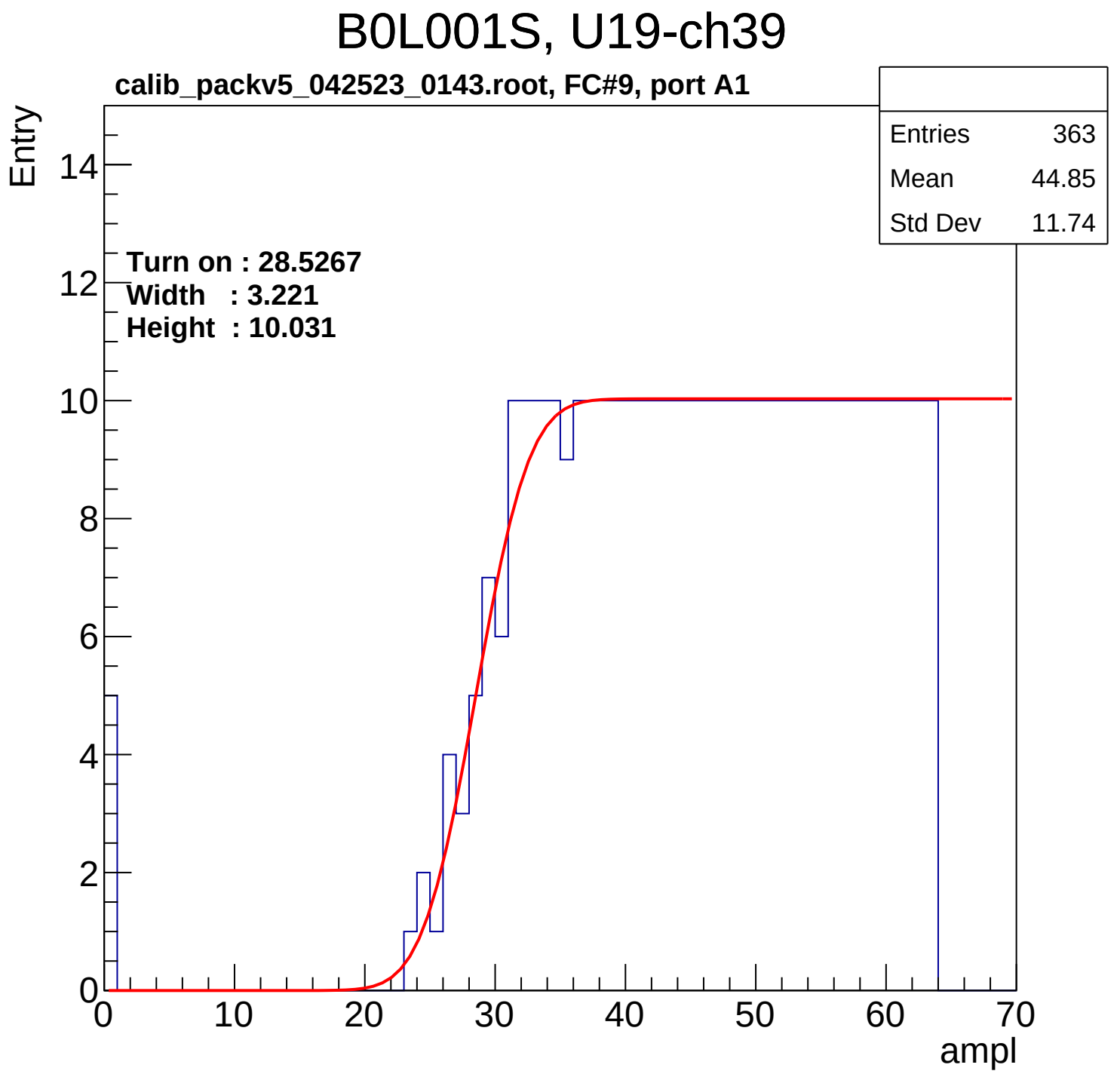
B0L001S, U19-ch39
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 44.85
Std Dev 11.74
Turn on : 28.5267
Width : 3.221
Height : 10.031
Entry
ampl
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6
8
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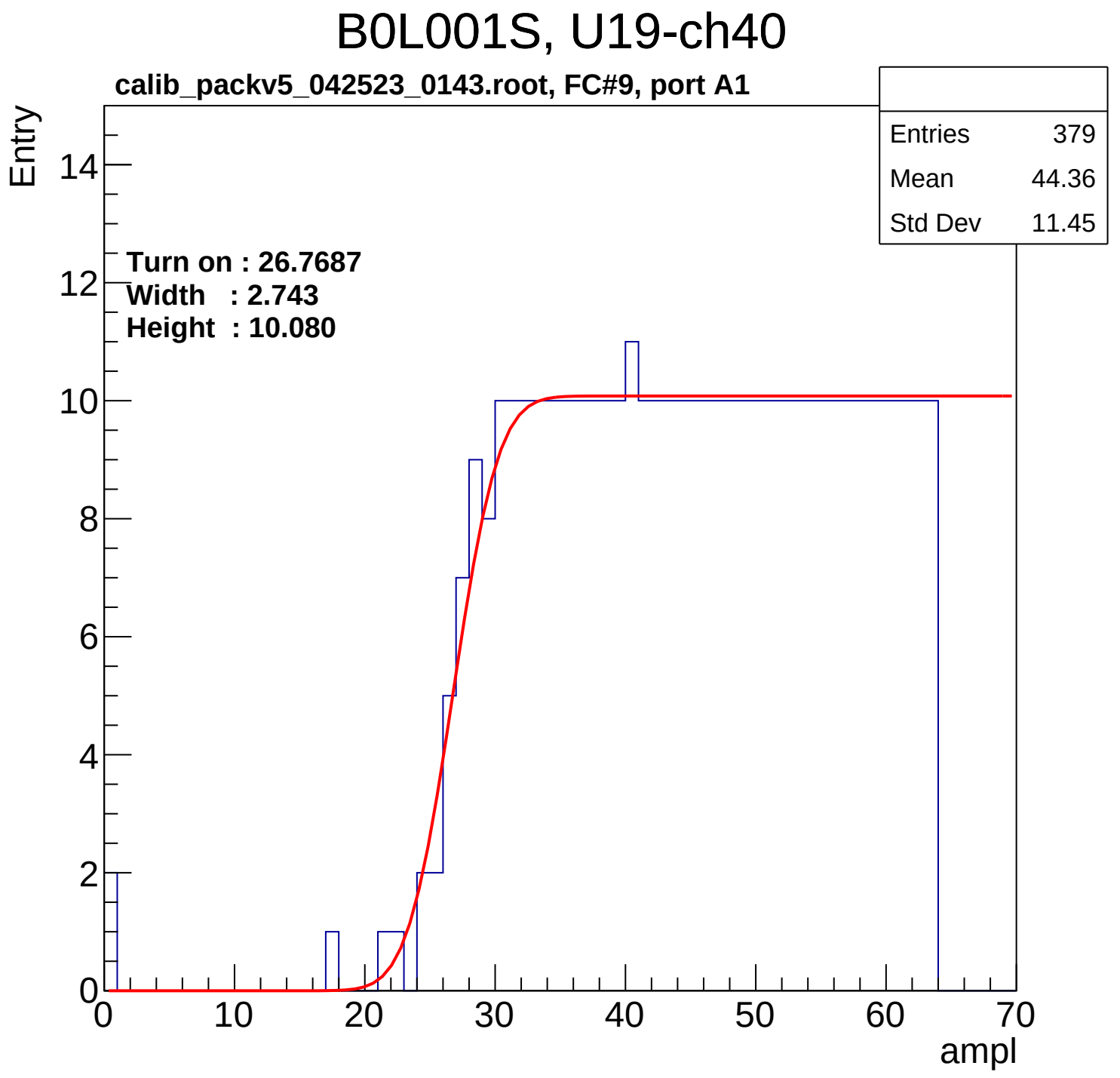
B0L001S, U19-ch40
calib_packv5_042523_0143.root, FC#9, port A1
Entries 379
Mean 44.36
Std Dev 11.45
Turn on : 26.7687
Width : 2.743
Height : 10.080
Entry
ampl
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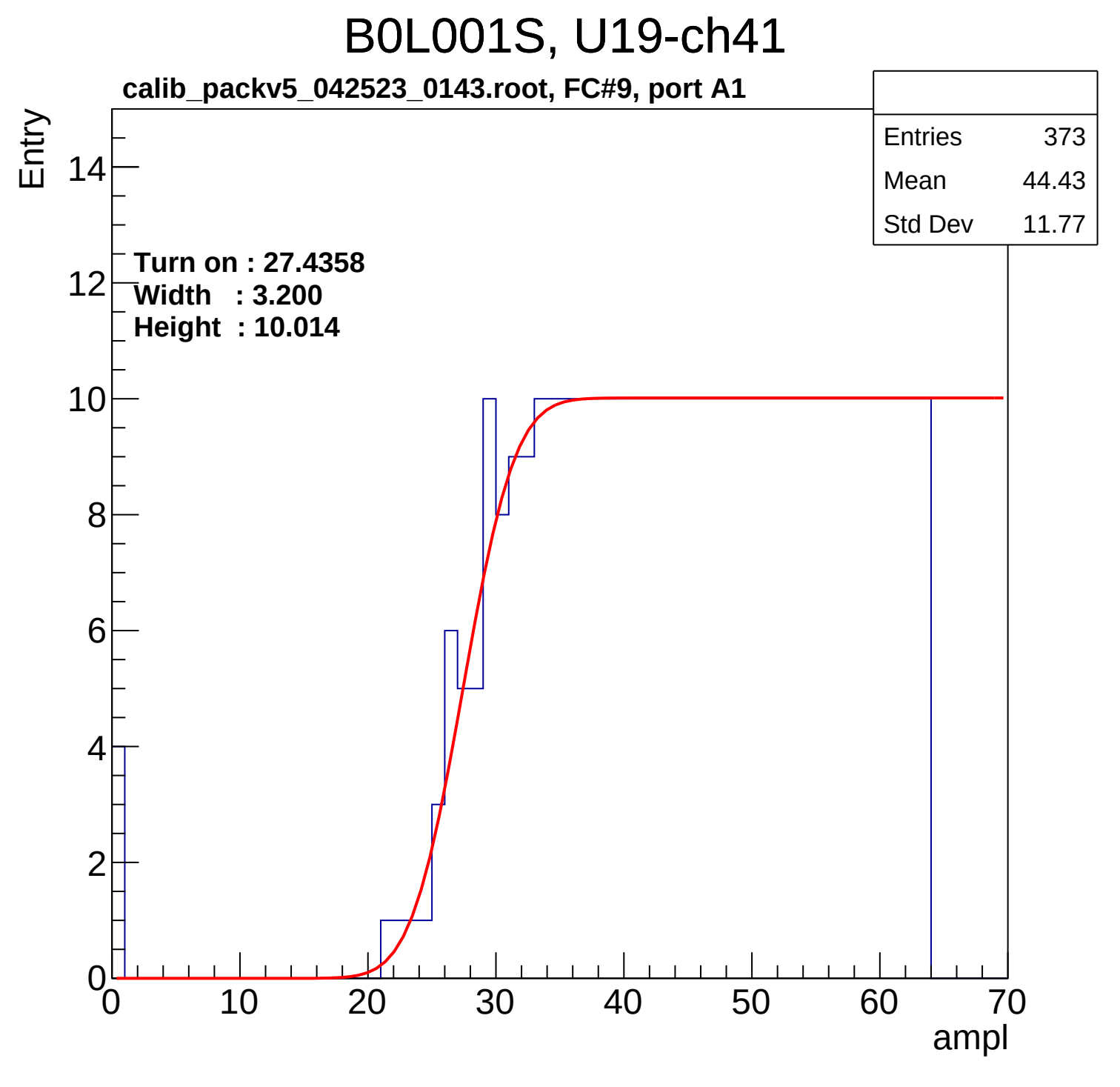
B0L001S, U19-ch41
calib_packv5_042523_0143.root, FC#9, port A1
Entries 373
Mean 44.43
Std Dev 11.77
Turn on : 27.4358
Width : 3.200
Height : 10.014
Entry
ampl
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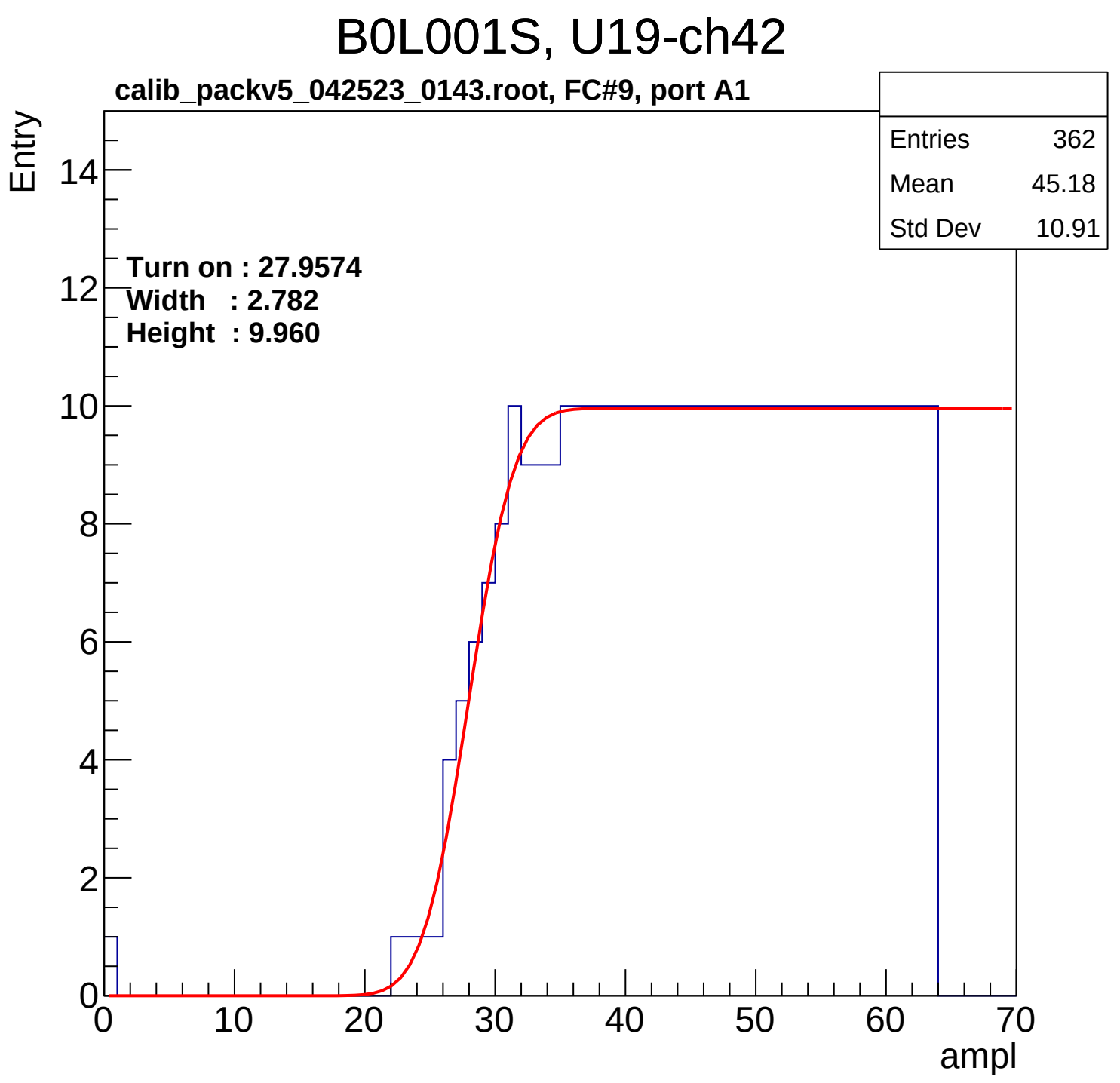
B0L001S, U19-ch42
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 45.18
Std Dev 10.91
Turn on : 27.9574
Width : 2.782
Height : 9.960
Entry
ampl
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8
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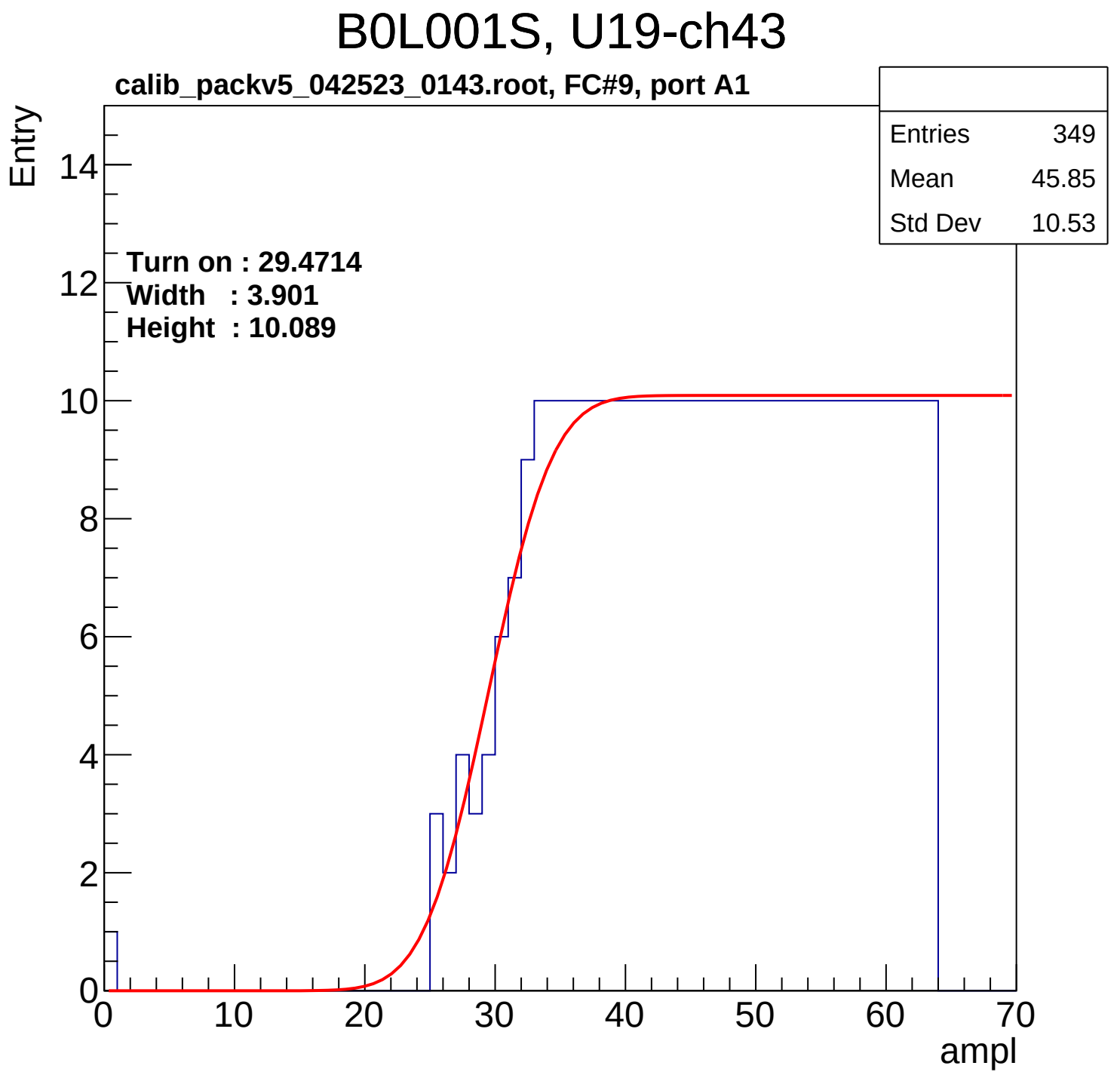
B0L001S, U19-ch43
calib_packv5_042523_0143.root, FC#9, port A1
Entries 349
Mean 45.85
Std Dev 10.53
Turn on : 29.4714
Width : 3.901
Height : 10.089
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ampl
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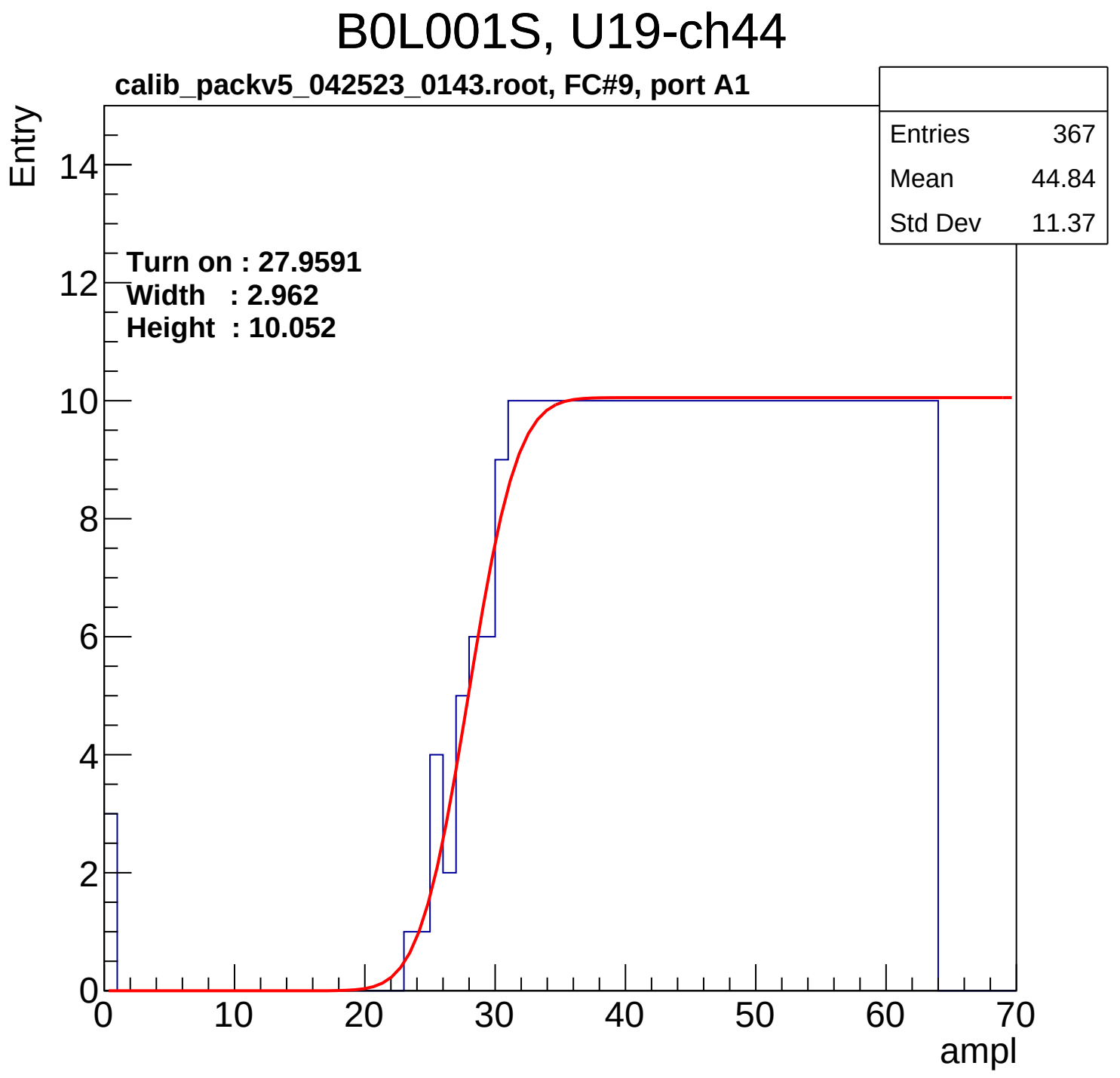
B0L001S, U19-ch44
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.84
Std Dev 11.37
Turn on : 27.9591
Width : 2.962
Height : 10.052
Entry
ampl
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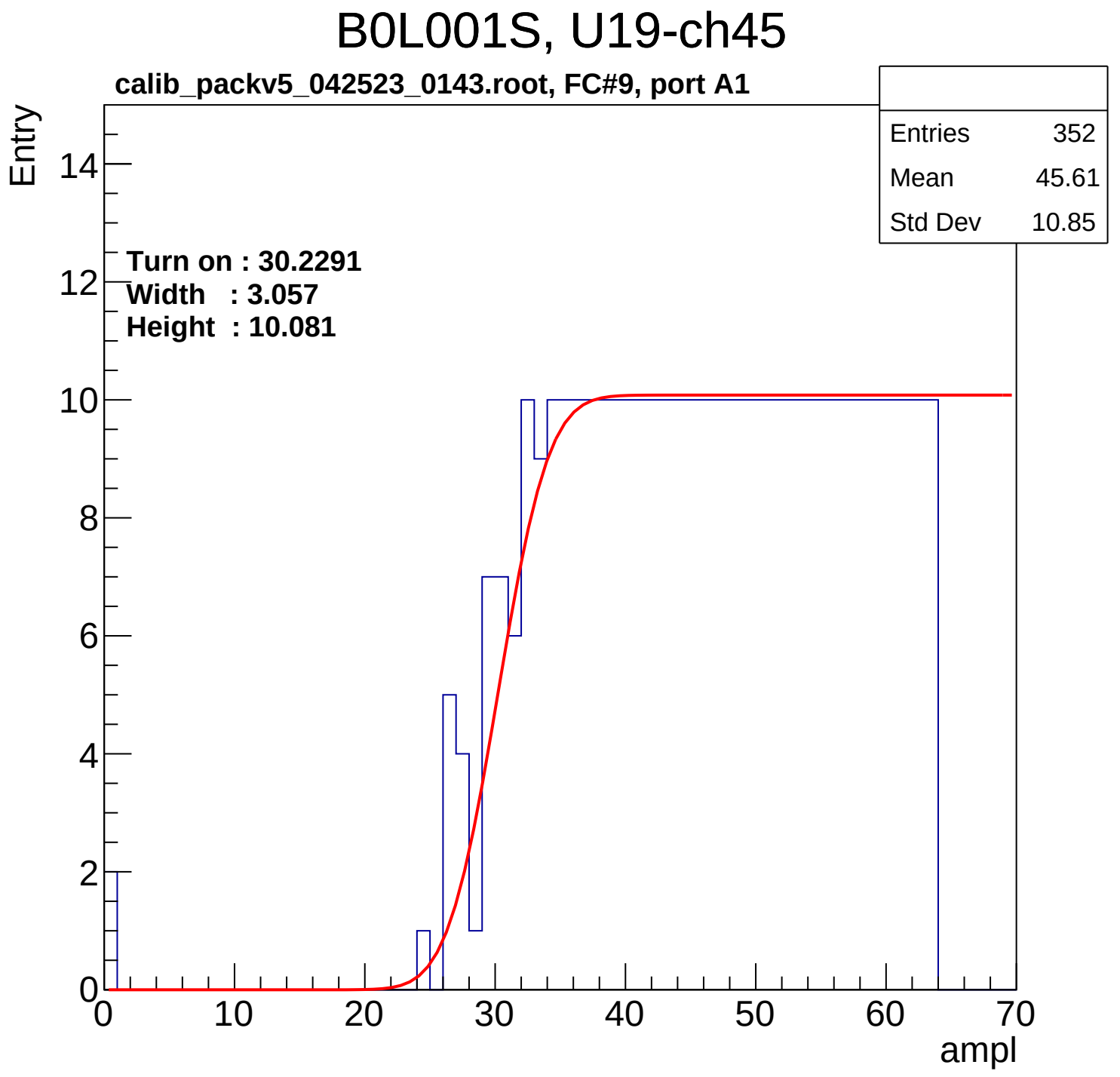
B0L001S, U19-ch45
calib_packv5_042523_0143.root, FC#9, port A1
Entries 352
Mean 45.61
Std Dev 10.85
Turn on : 30.2291
Width : 3.057
Height : 10.081
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ampl
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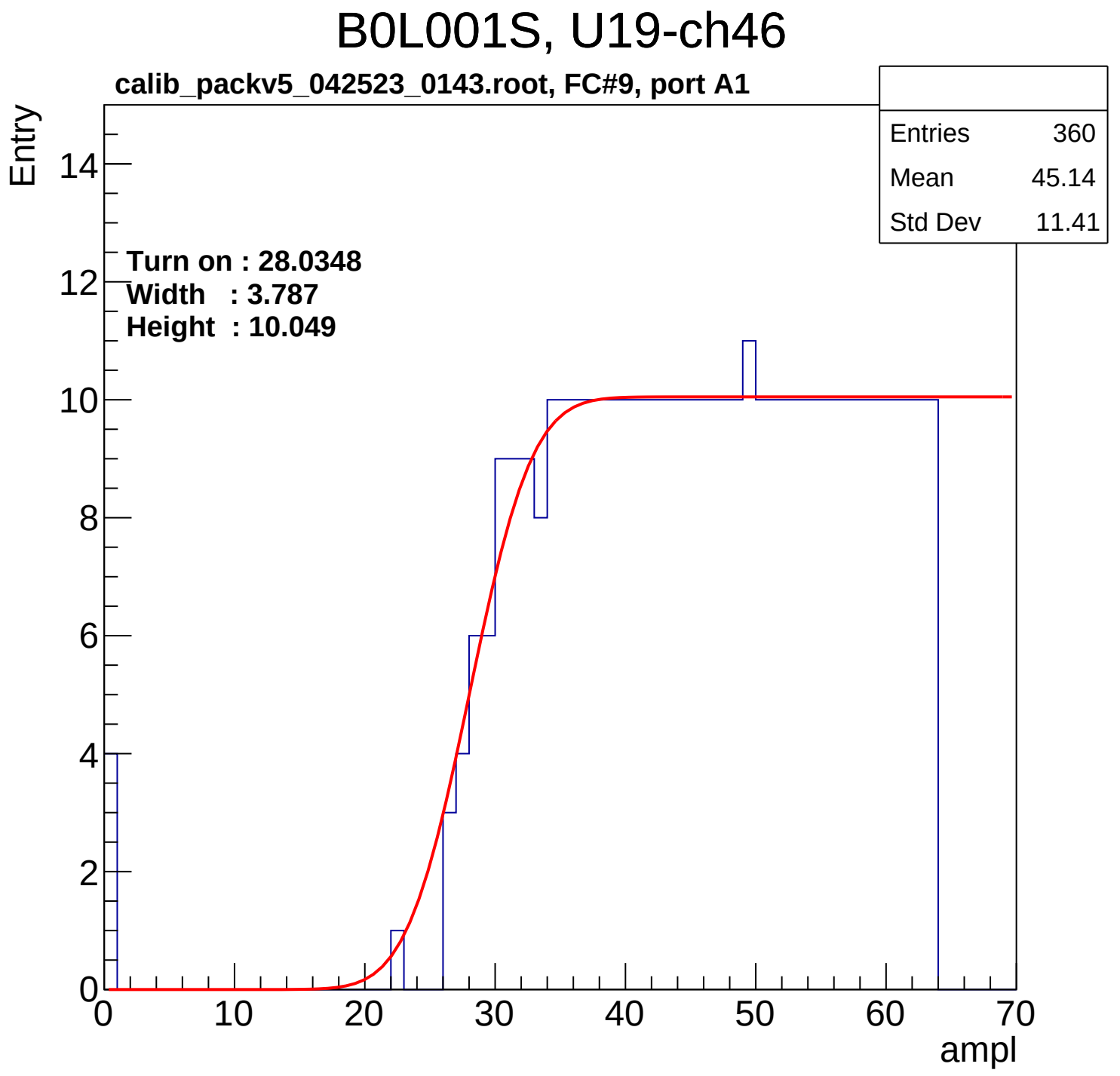
B0L001S, U19-ch46
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 45.14
Std Dev 11.41
Turn on : 28.0348
Width : 3.787
Height : 10.049
Entry
ampl
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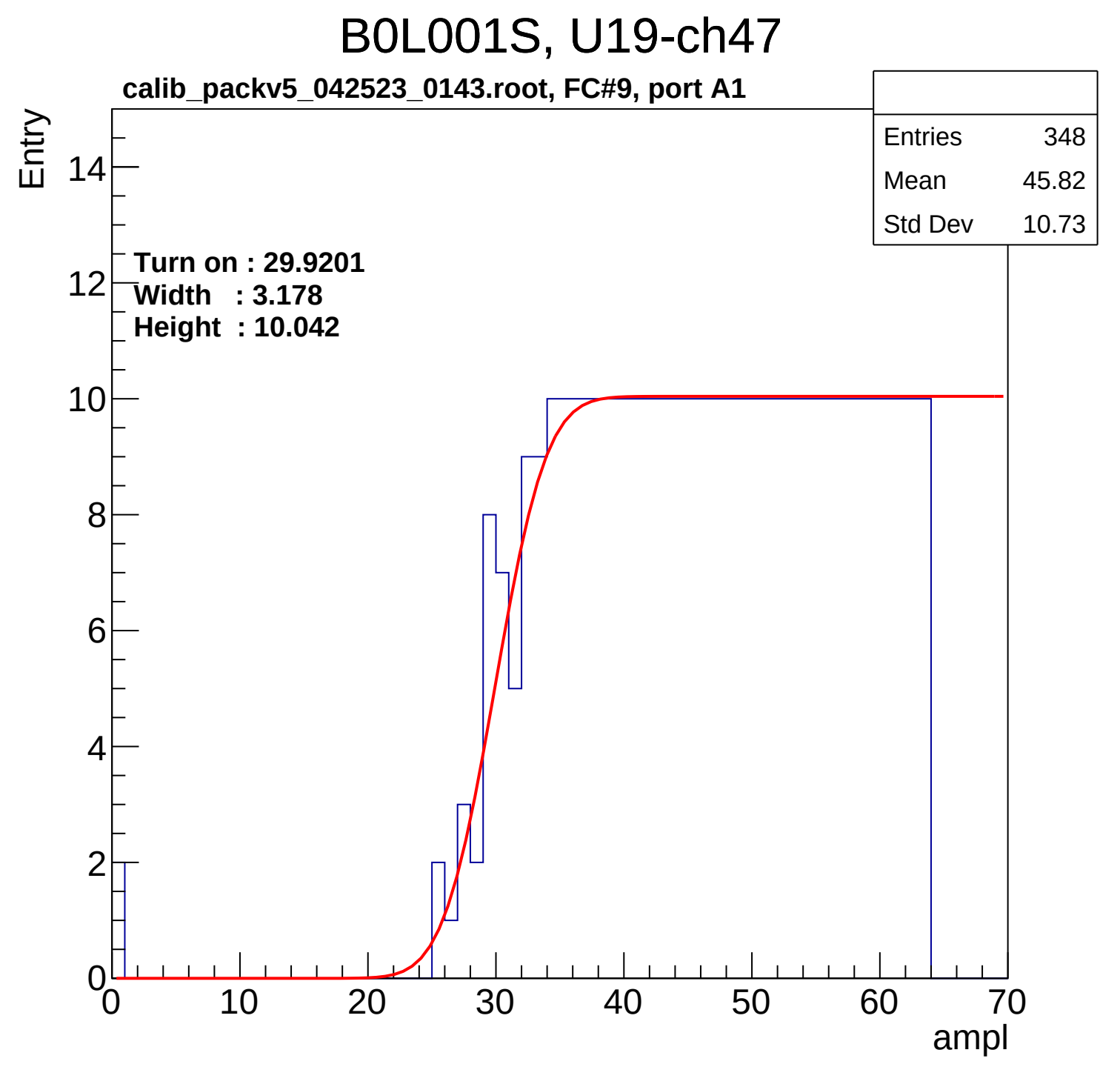
B0L001S, U19-ch47
calib_packv5_042523_0143.root, FC#9, port A1
Entries 348
Mean 45.82
Std Dev 10.73
Turn on : 29.9201
Width : 3.178
Height : 10.042
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ampl
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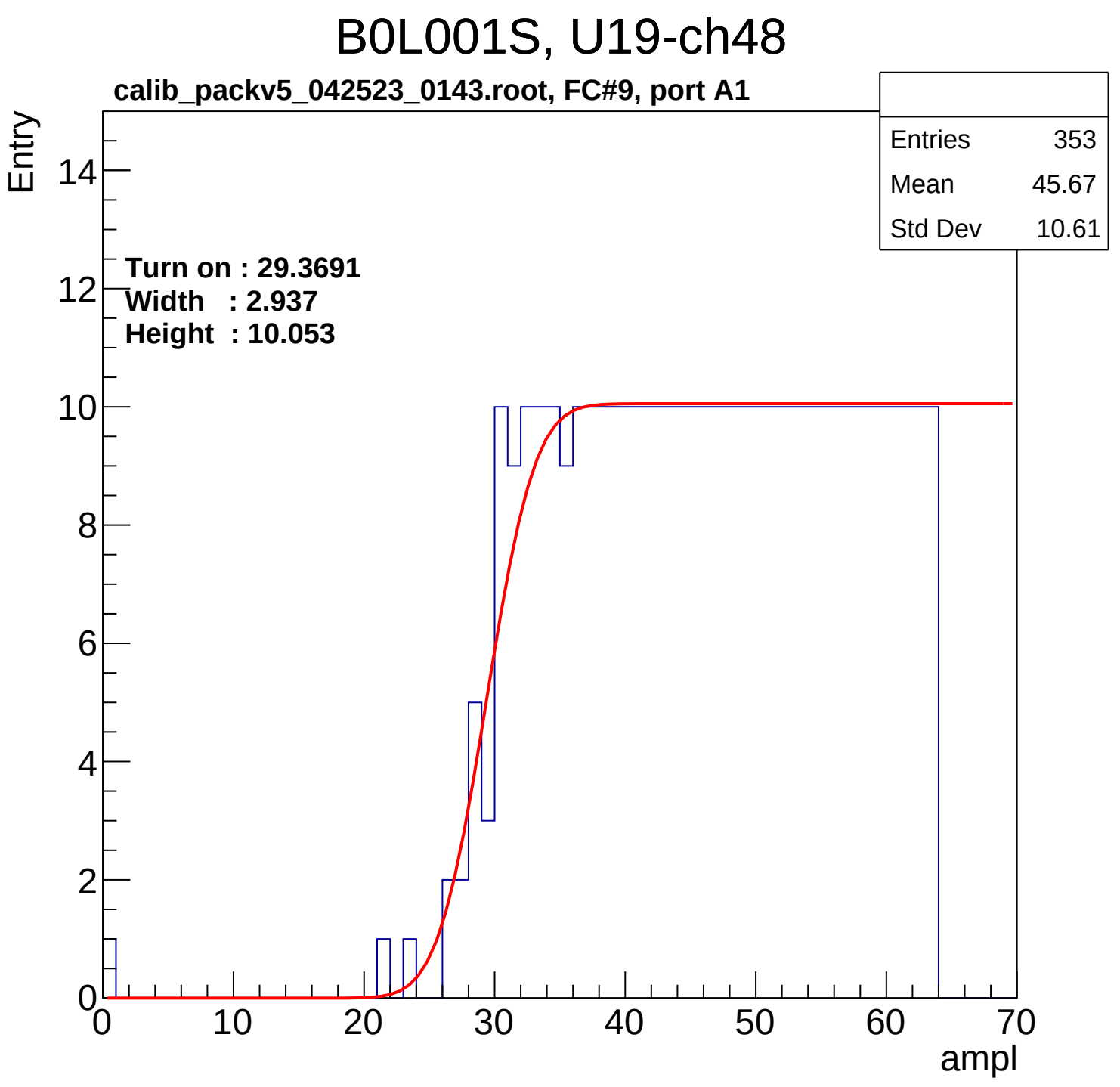
B0L001S, U19-ch48
calib_packv5_042523_0143.root, FC#9, port A1
Entries 353
Mean 45.67
Std Dev 10.61
Turn on : 29.3691
Width : 2.937
Height : 10.053
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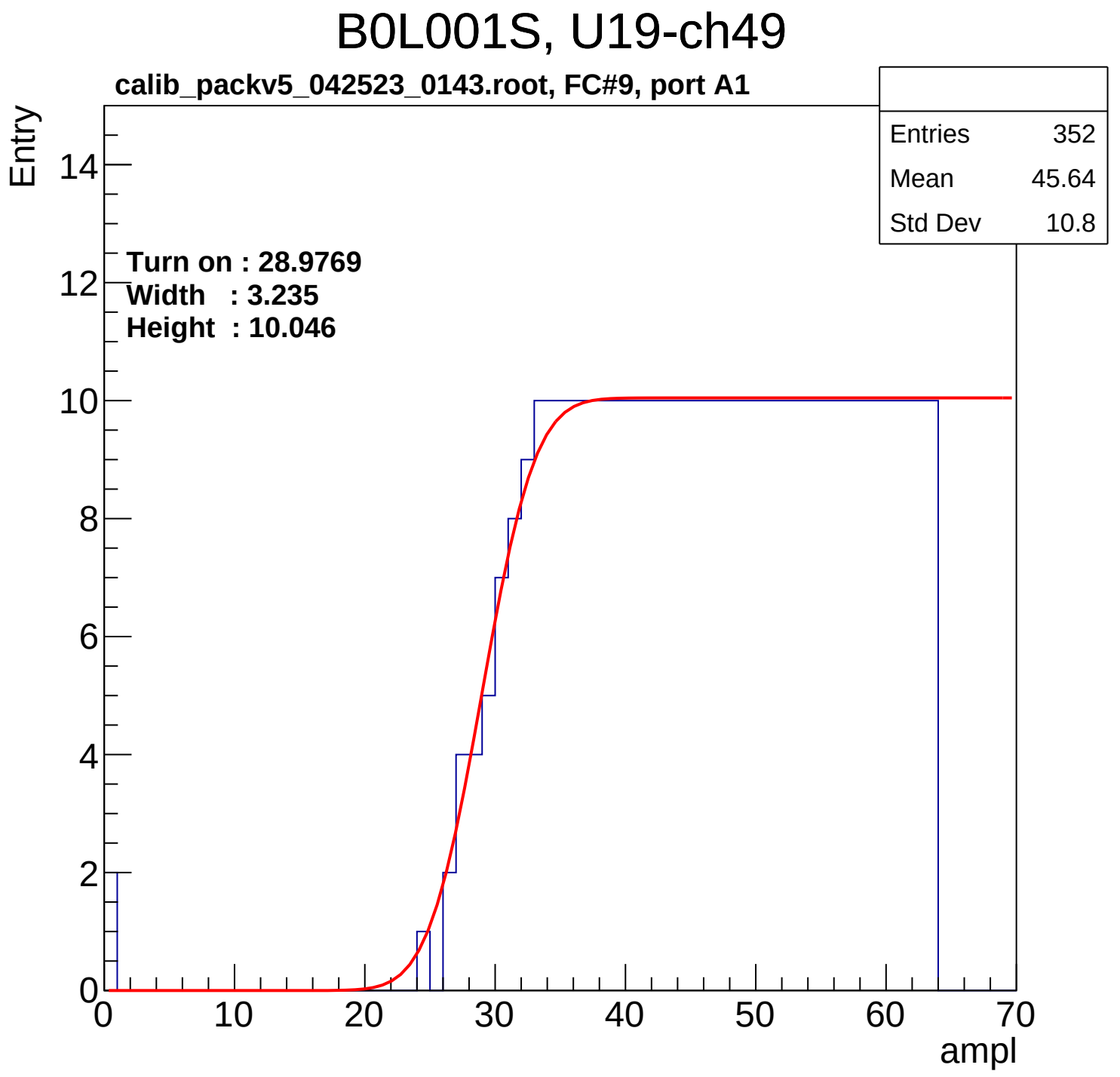
B0L001S, U19-ch49
calib_packv5_042523_0143.root, FC#9, port A1
Entries 352
Mean 45.64
Std Dev 10.8
Turn on : 28.9769
Width : 3.235
Height : 10.046
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ampl
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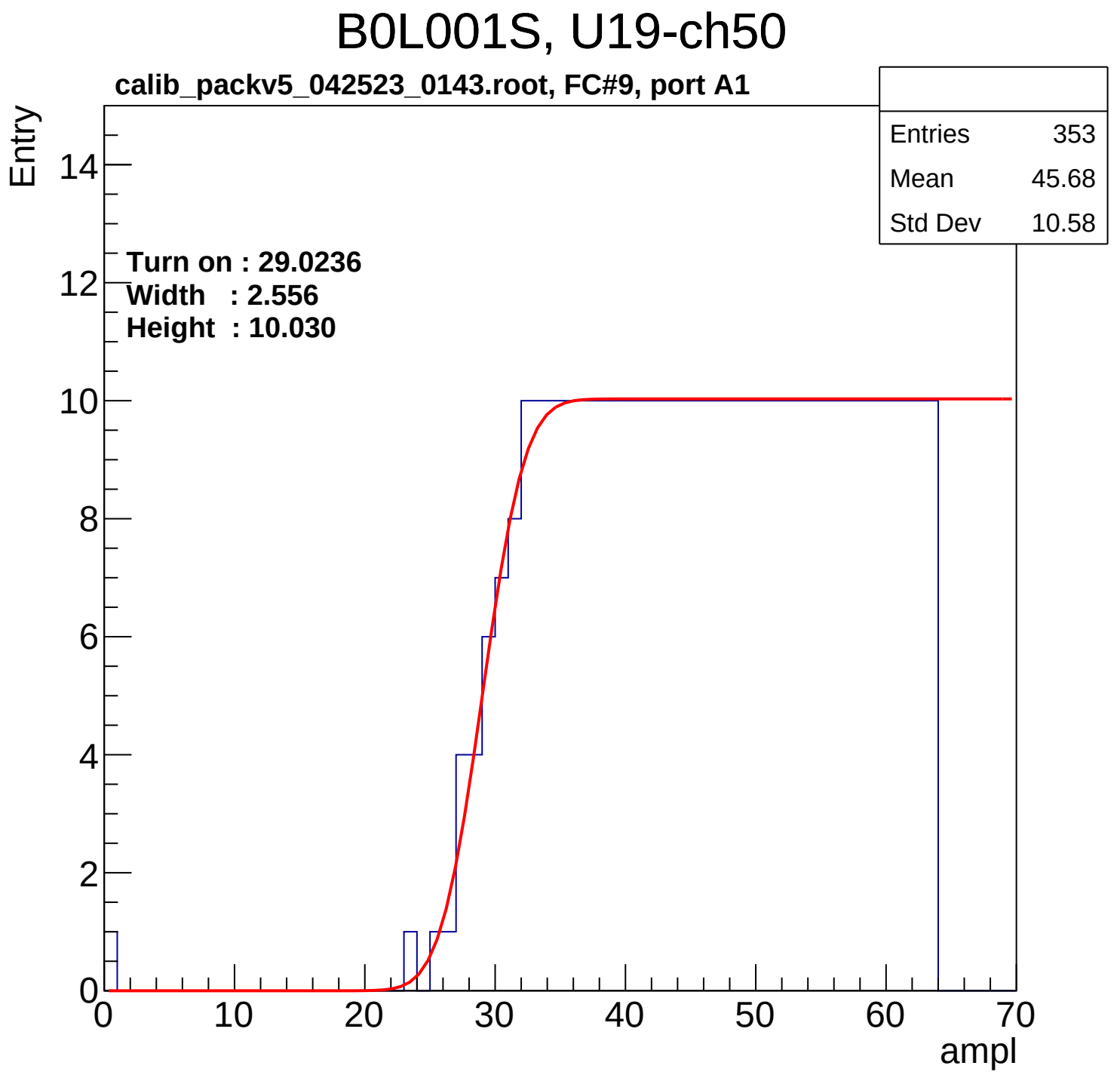
B0L001S, U19-ch50
calib_packv5_042523_0143.root, FC#9, port A1
Entries 353
Mean 45.68
Std Dev 10.58
Turn on : 29.0236
Width : 2.556
Height : 10.030
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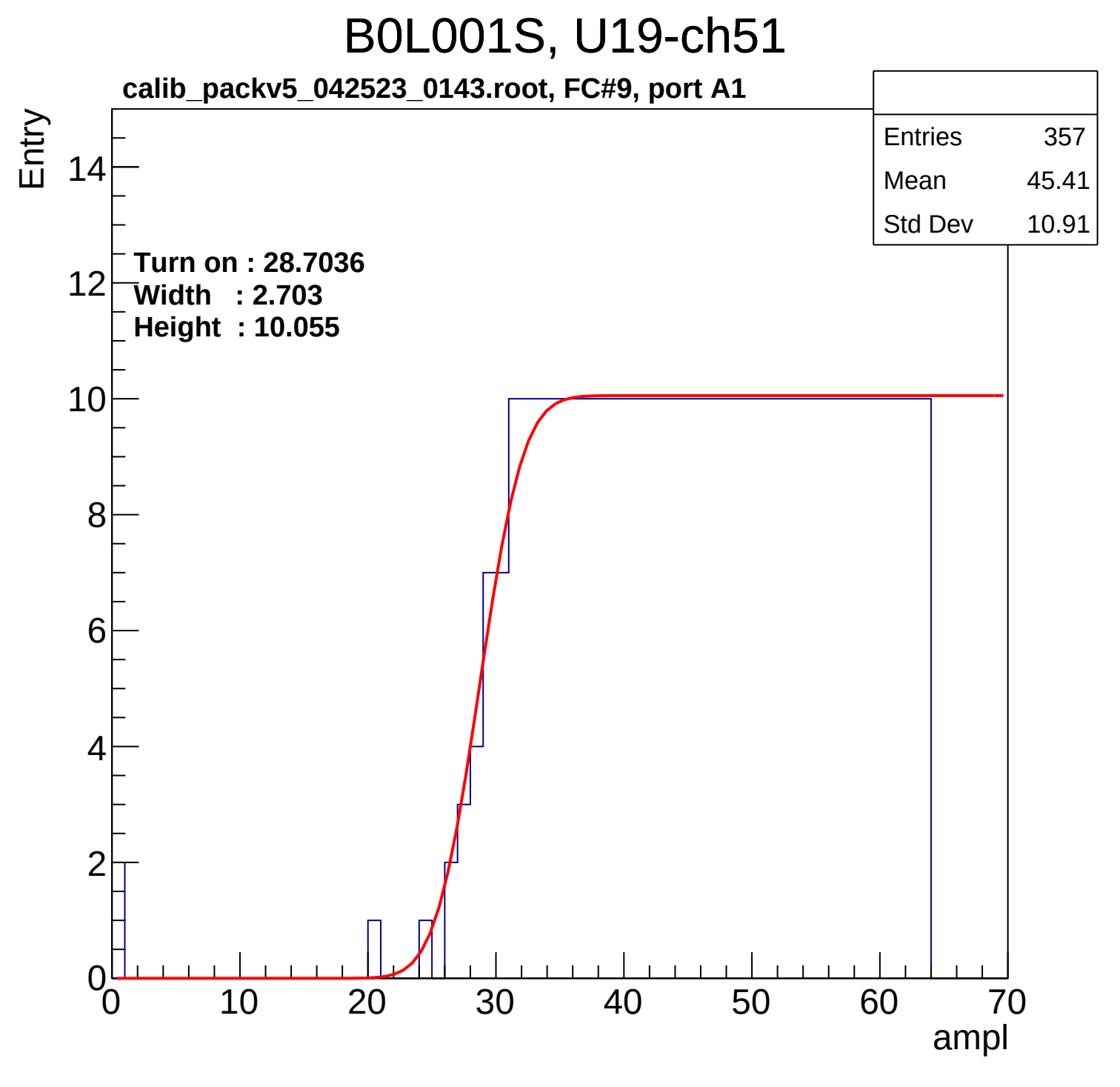
B0L001S, U19-ch51
calib_packv5_042523_0143.root, FC#9, port A1
Entries 357
Mean 45.41
Std Dev 10.91
Turn on : 28.7036
Width : 2.703
Height : 10.055
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ampl
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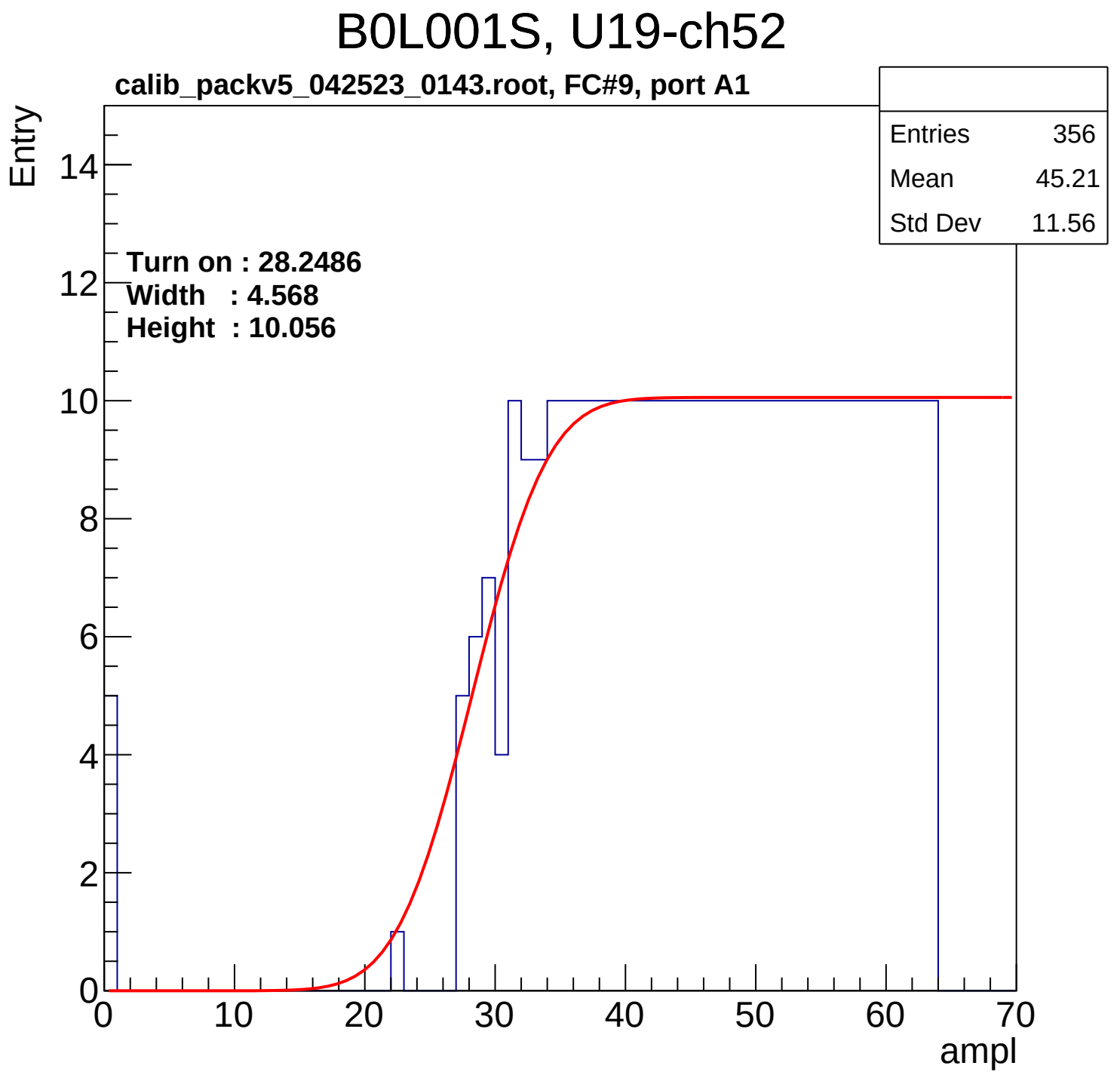
B0L001S, U19-ch52
calib_packv5_042523_0143.root, FC#9, port A1
Entries 356
Mean 45.21
Std Dev 11.56
Turn on : 28.2486
Width : 4.568
Height : 10.056
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ampl
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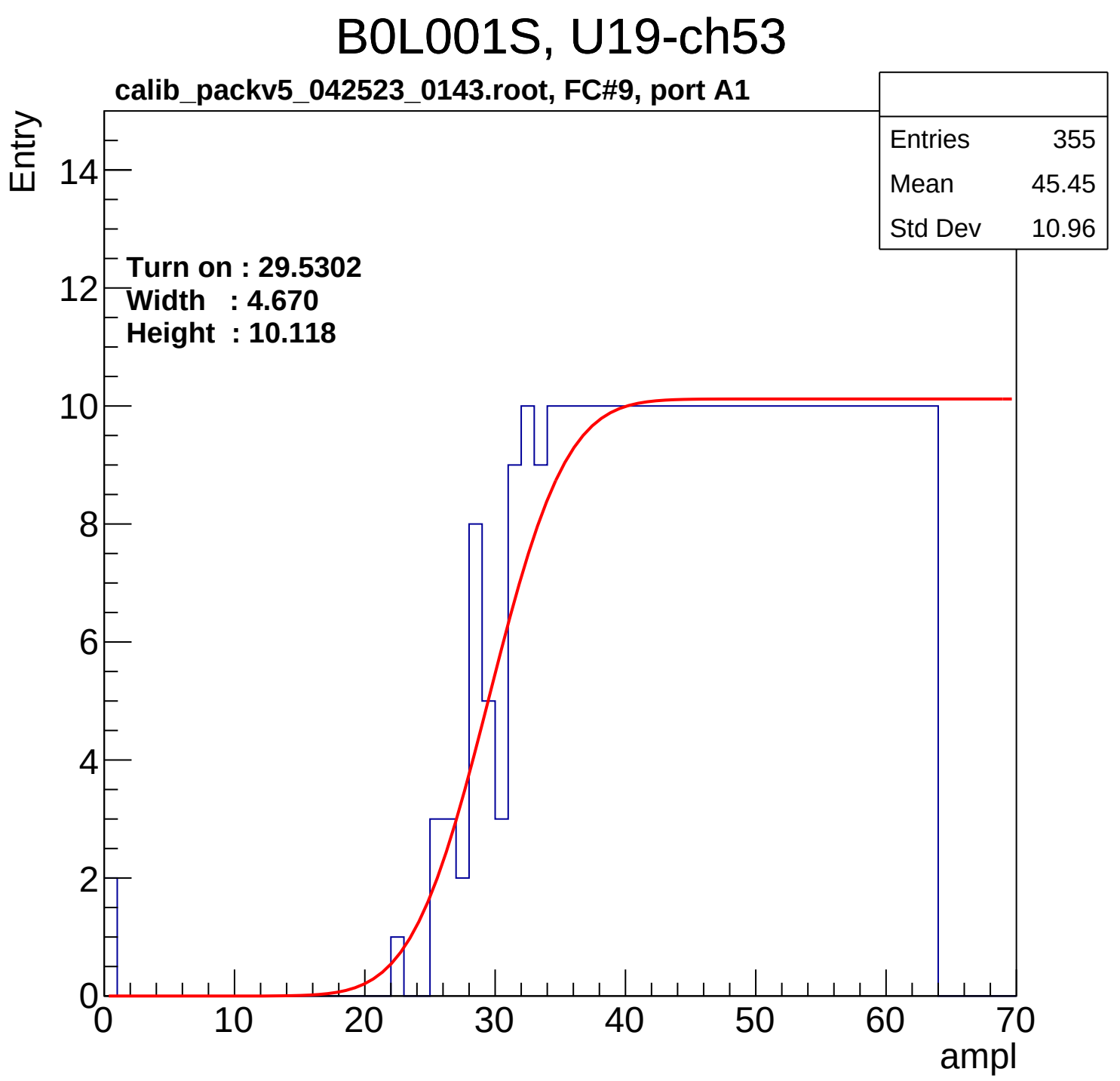
B0L001S, U19-ch53
calib_packv5_042523_0143.root, FC#9, port A1
Entries 355
Mean 45.45
Std Dev 10.96
Turn on : 29.5302
Width : 4.670
Height : 10.118
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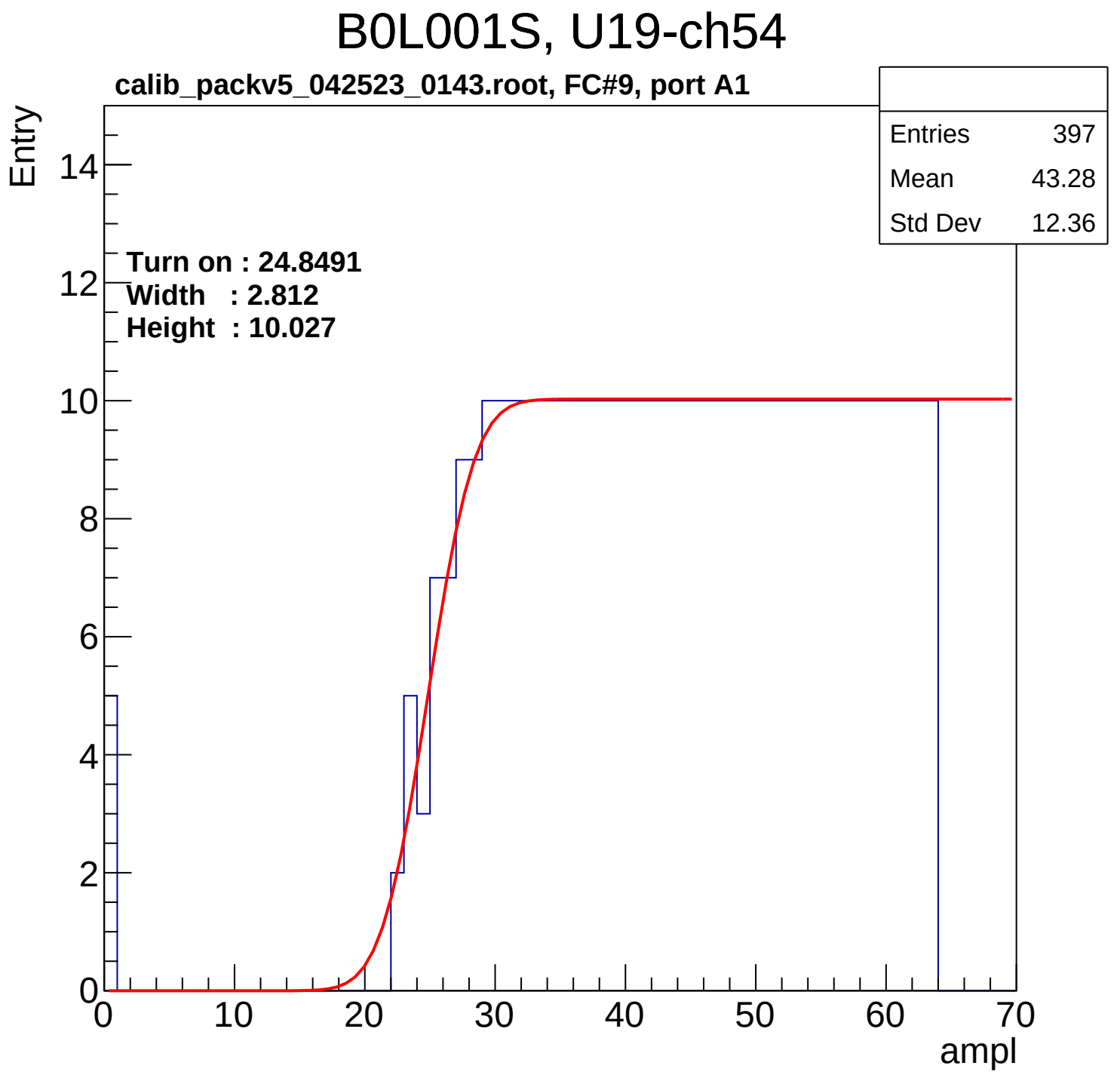
B0L001S, U19-ch54
calib_packv5_042523_0143.root, FC#9, port A1
Entries 397
Mean 43.28
Std Dev 12.36
Turn on : 24.8491
Width : 2.812
Height : 10.027
Entry
ampl
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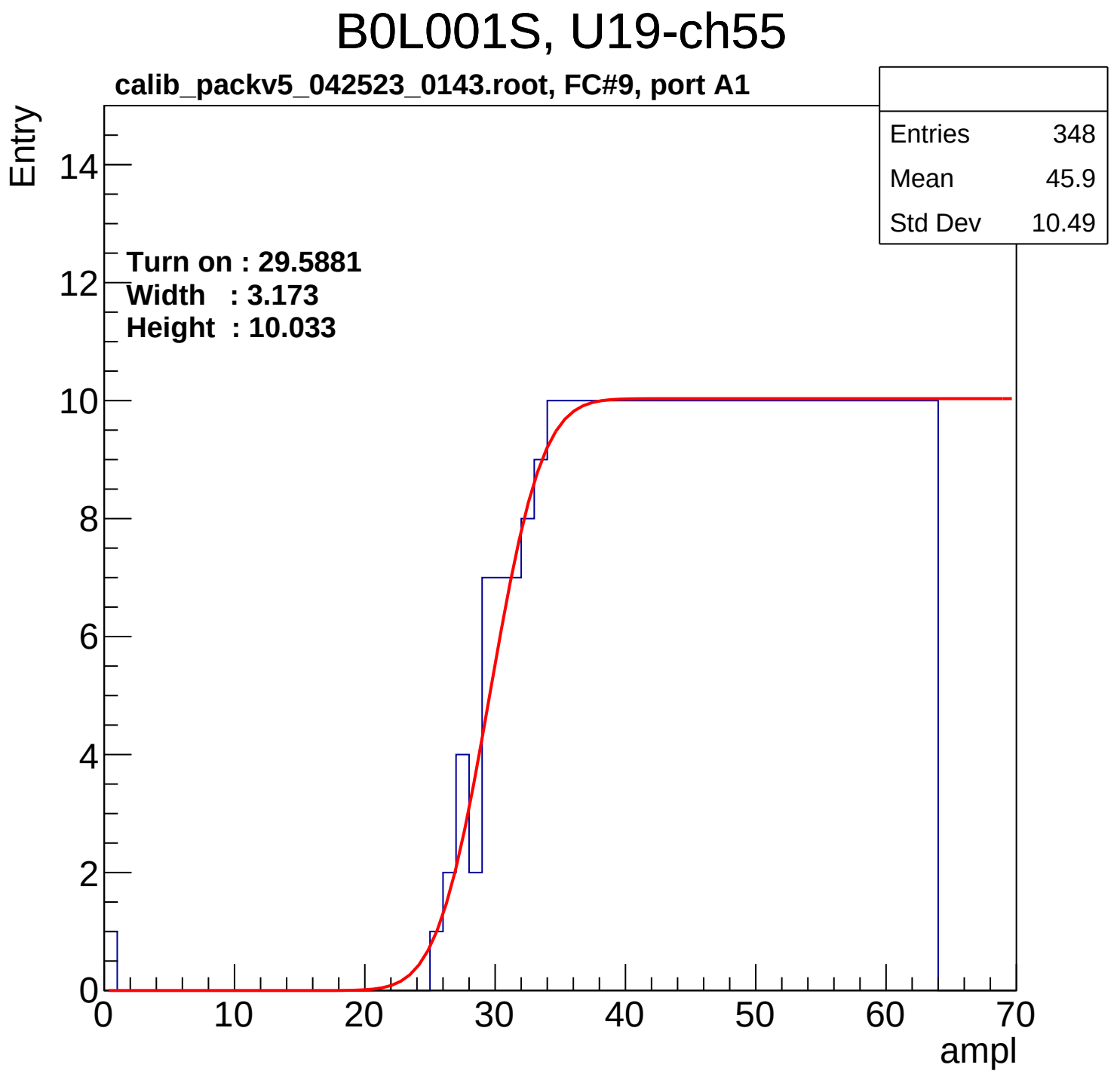
B0L001S, U19-ch55
calib_packv5_042523_0143.root, FC#9, port A1
Entries 348
Mean 45.9
Std Dev 10.49
Turn on : 29.5881
Width : 3.173
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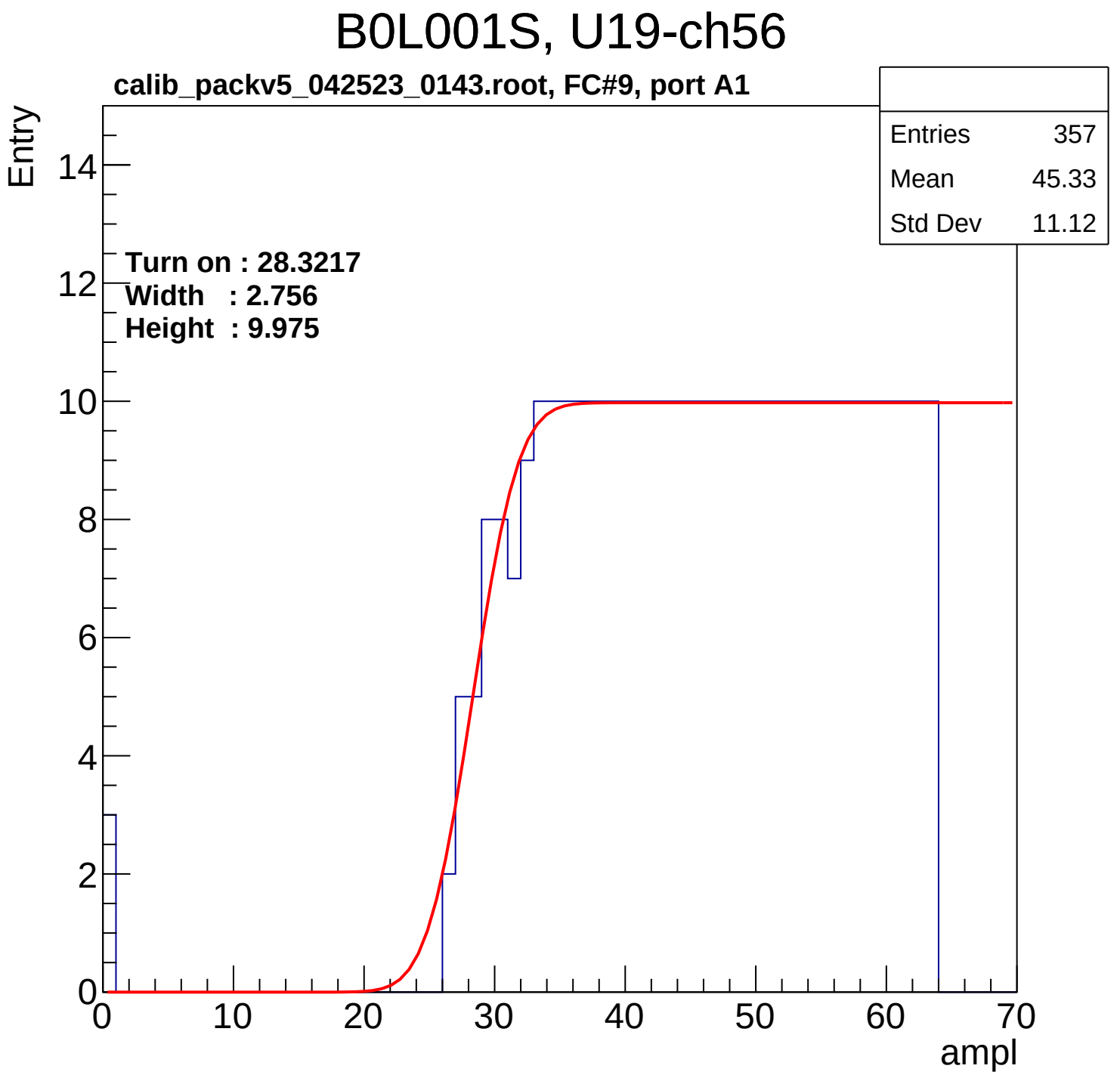
B0L001S, U19-ch56
calib_packv5_042523_0143.root, FC#9, port A1
Entries 357
Mean 45.33
Std Dev 11.12
Turn on : 28.3217
Width : 2.756
Height : 9.975
Entry
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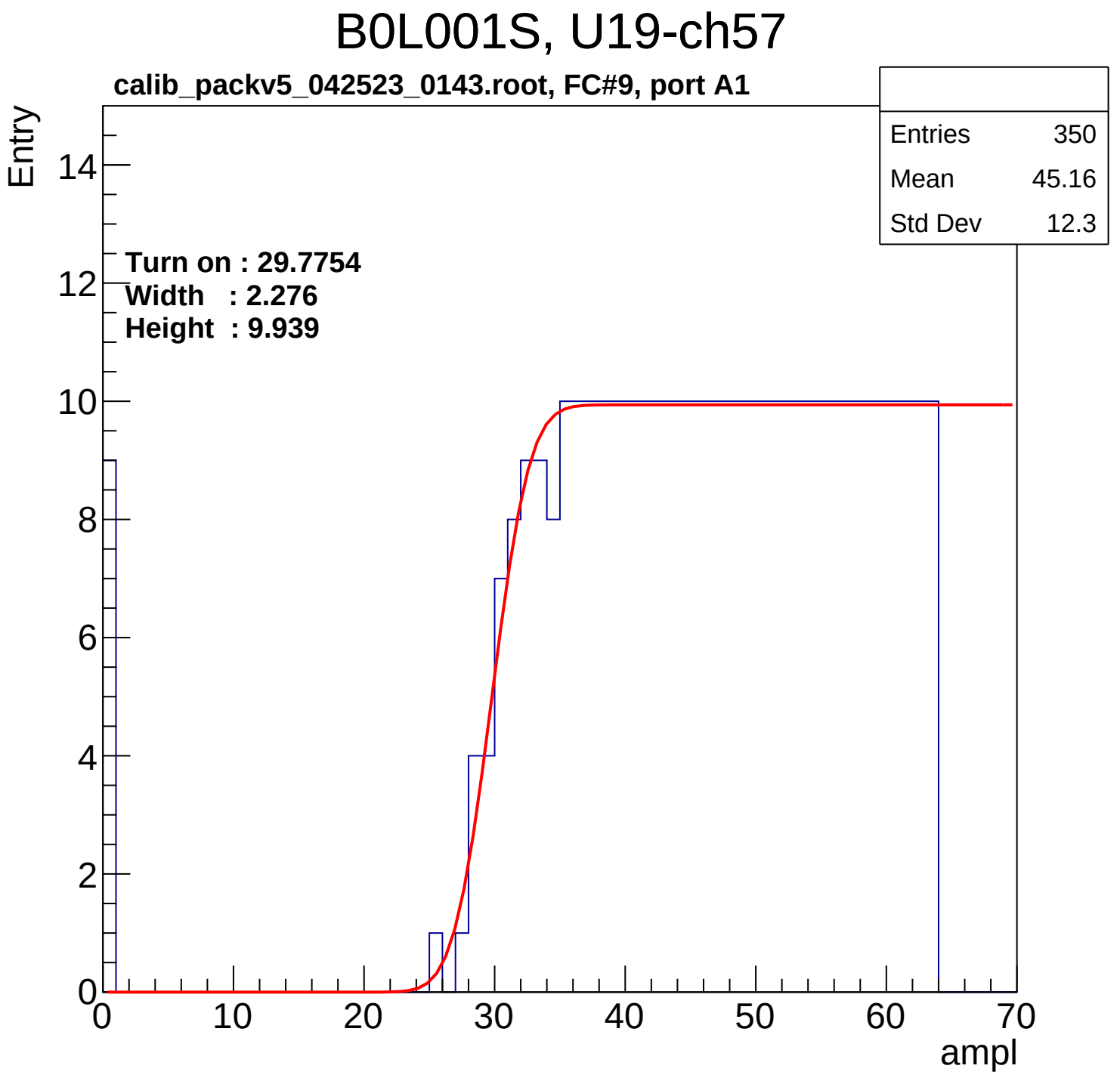
B0L001S, U19-ch57
calib_packv5_042523_0143.root, FC#9, port A1
Entries 350
Mean 45.16
Std Dev 12.3
Turn on : 29.7754
Width : 2.276
Height : 9.939
Entry
ampl
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4
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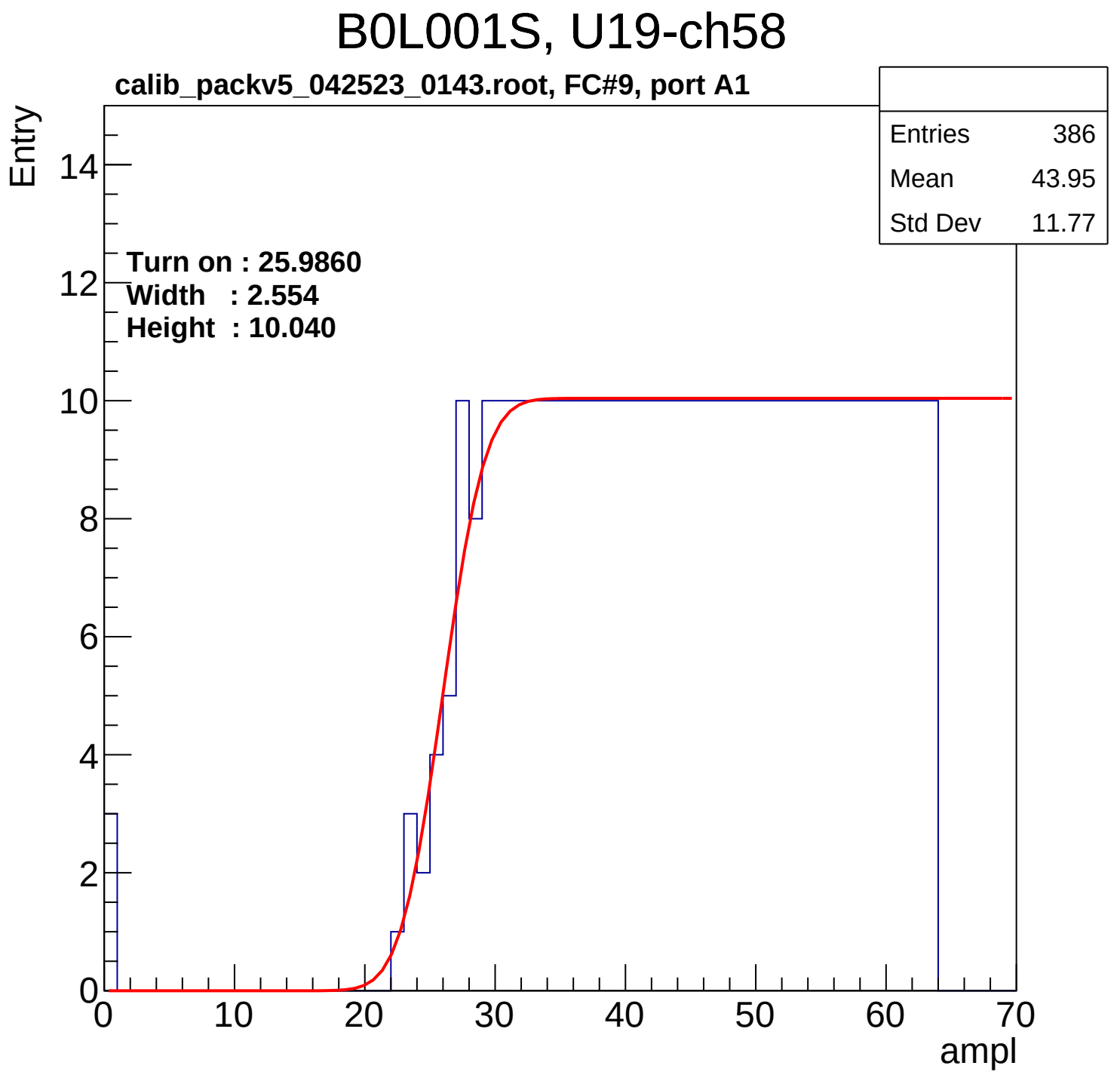
B0L001S, U19-ch58
calib_packv5_042523_0143.root, FC#9, port A1
Entries 386
Mean 43.95
Std Dev 11.77
Turn on : 25.9860
Width : 2.554
Height : 10.040
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ampl
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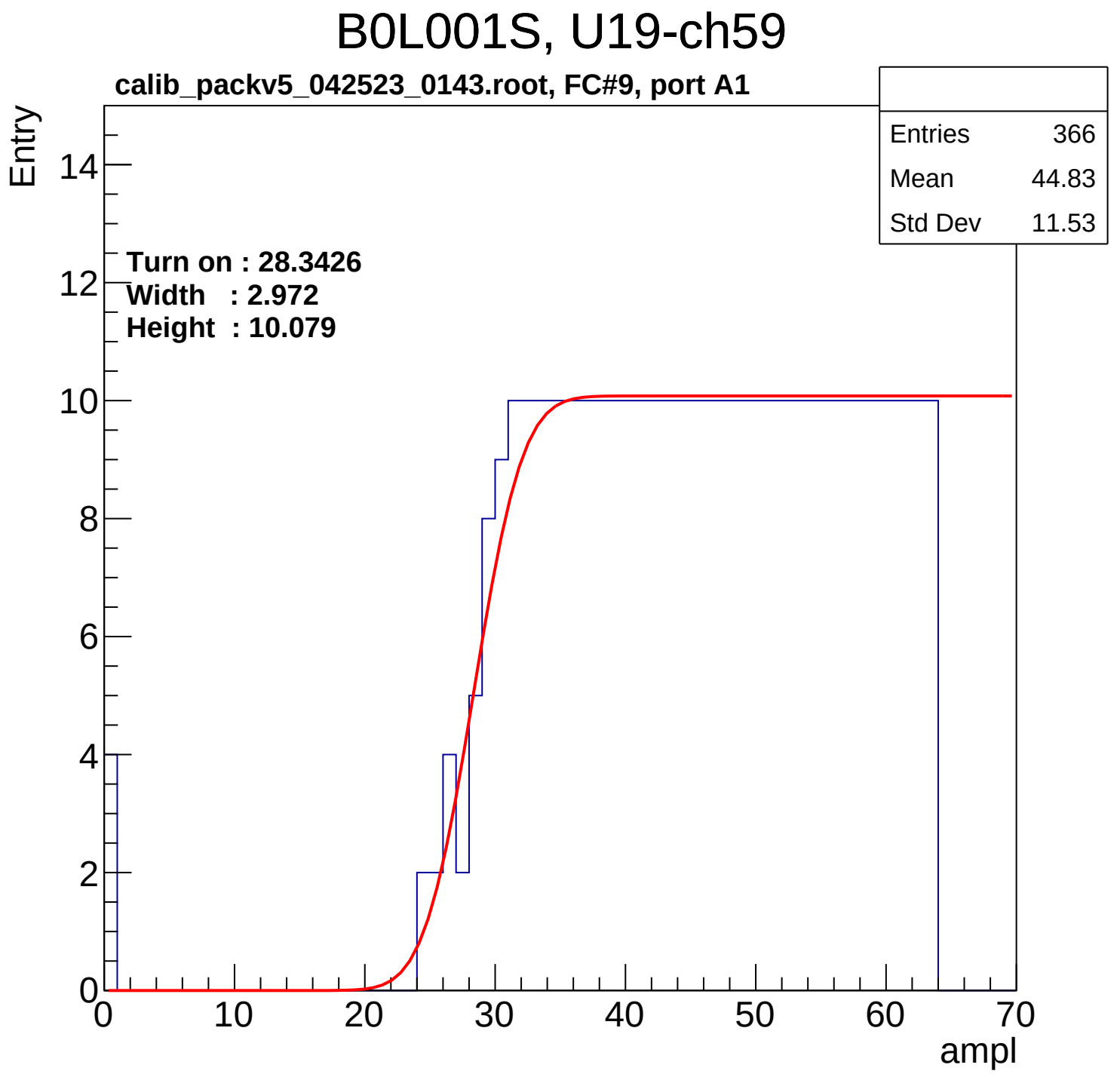
B0L001S, U19-ch59
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.83
Std Dev 11.53
Turn on : 28.3426
Width : 2.972
Height : 10.079
Entry
ampl
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2
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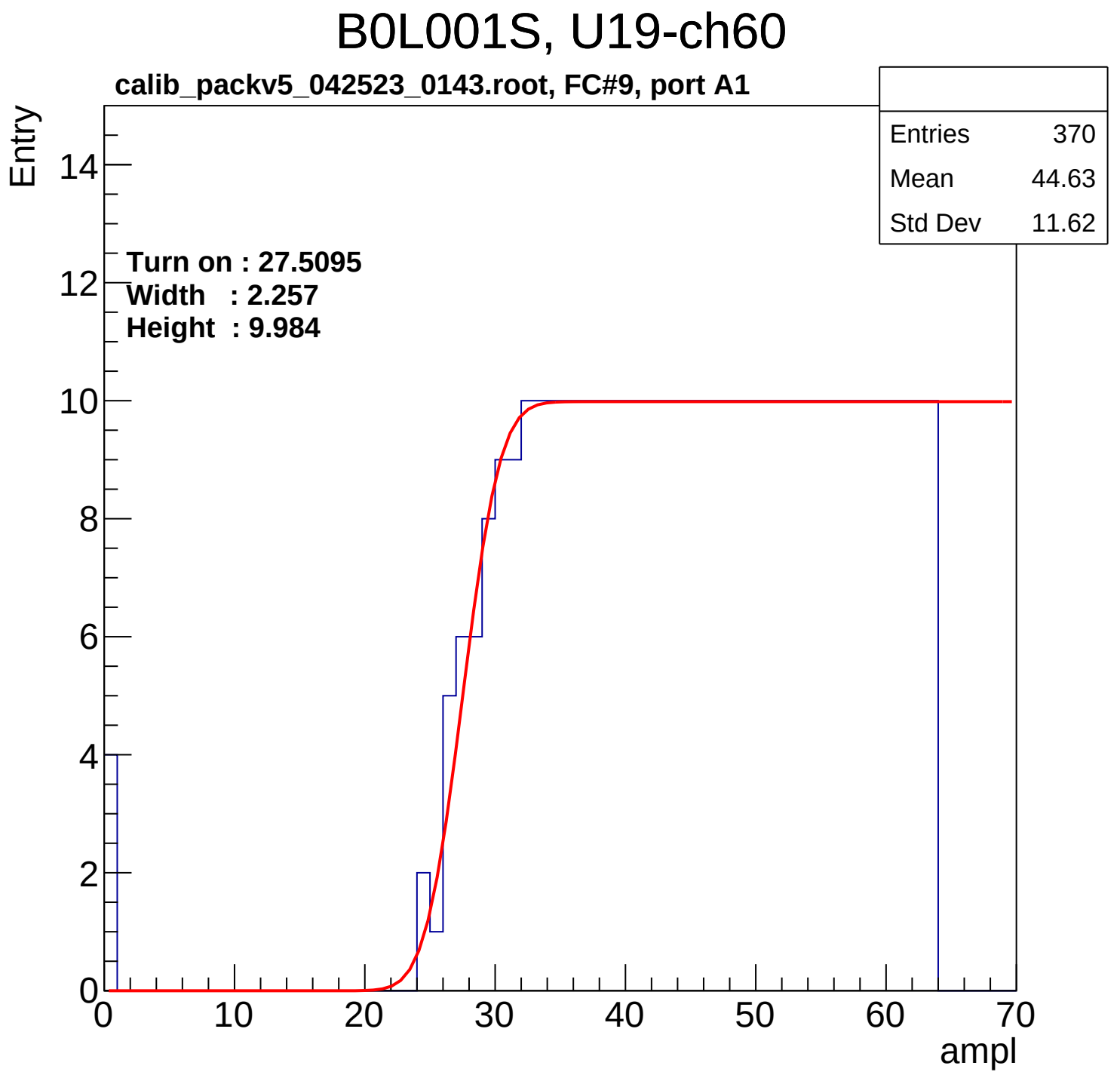
B0L001S, U19-ch60
calib_packv5_042523_0143.root, FC#9, port A1
Entries 370
Mean 44.63
Std Dev 11.62
Turn on : 27.5095
Width : 2.257
Height : 9.984
Entry
ampl
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2
4
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8
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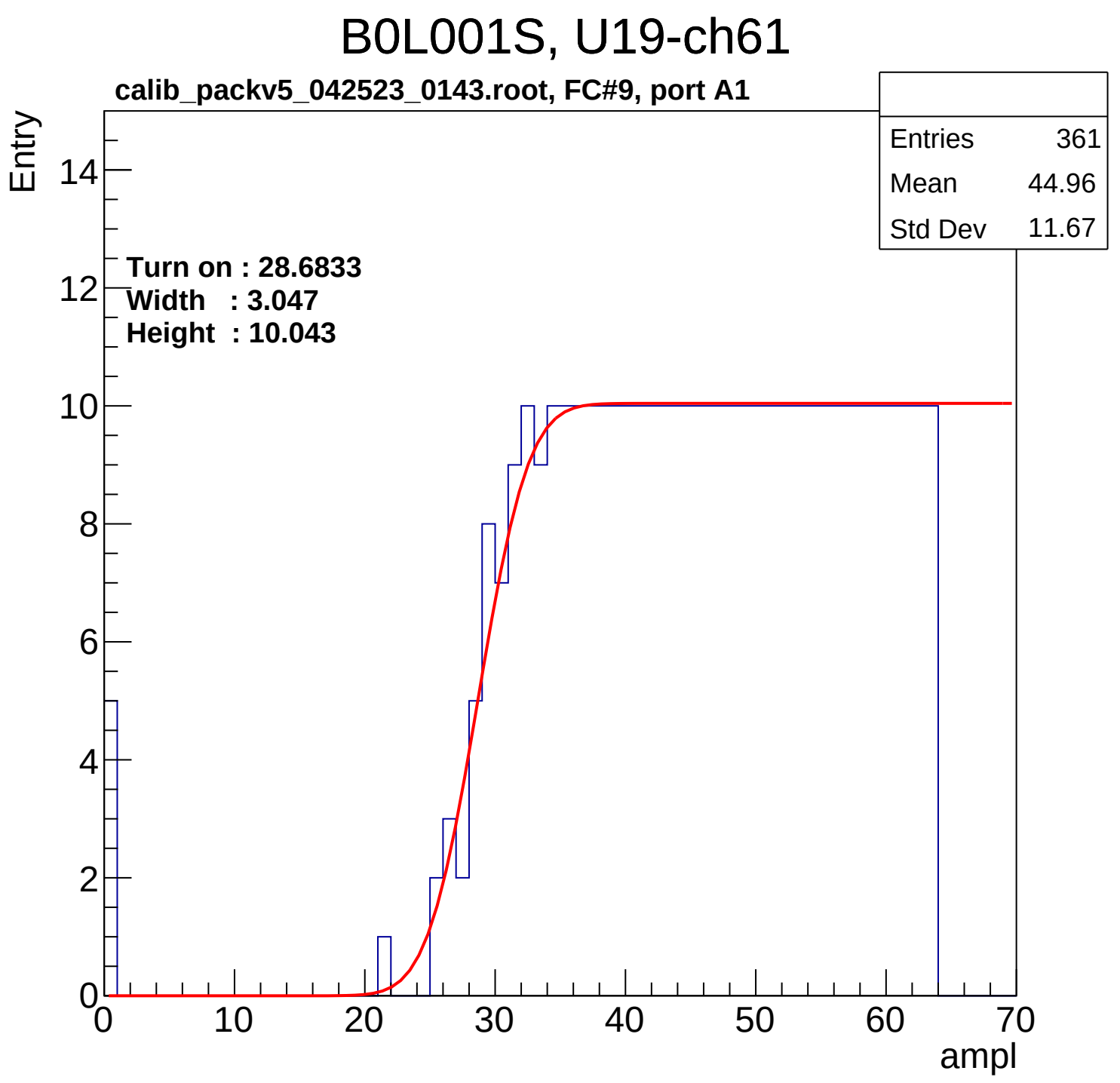
B0L001S, U19-ch61
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 44.96
Std Dev 11.67
Turn on : 28.6833
Width : 3.047
Height : 10.043
Entry
ampl
0
2
4
6
8
10
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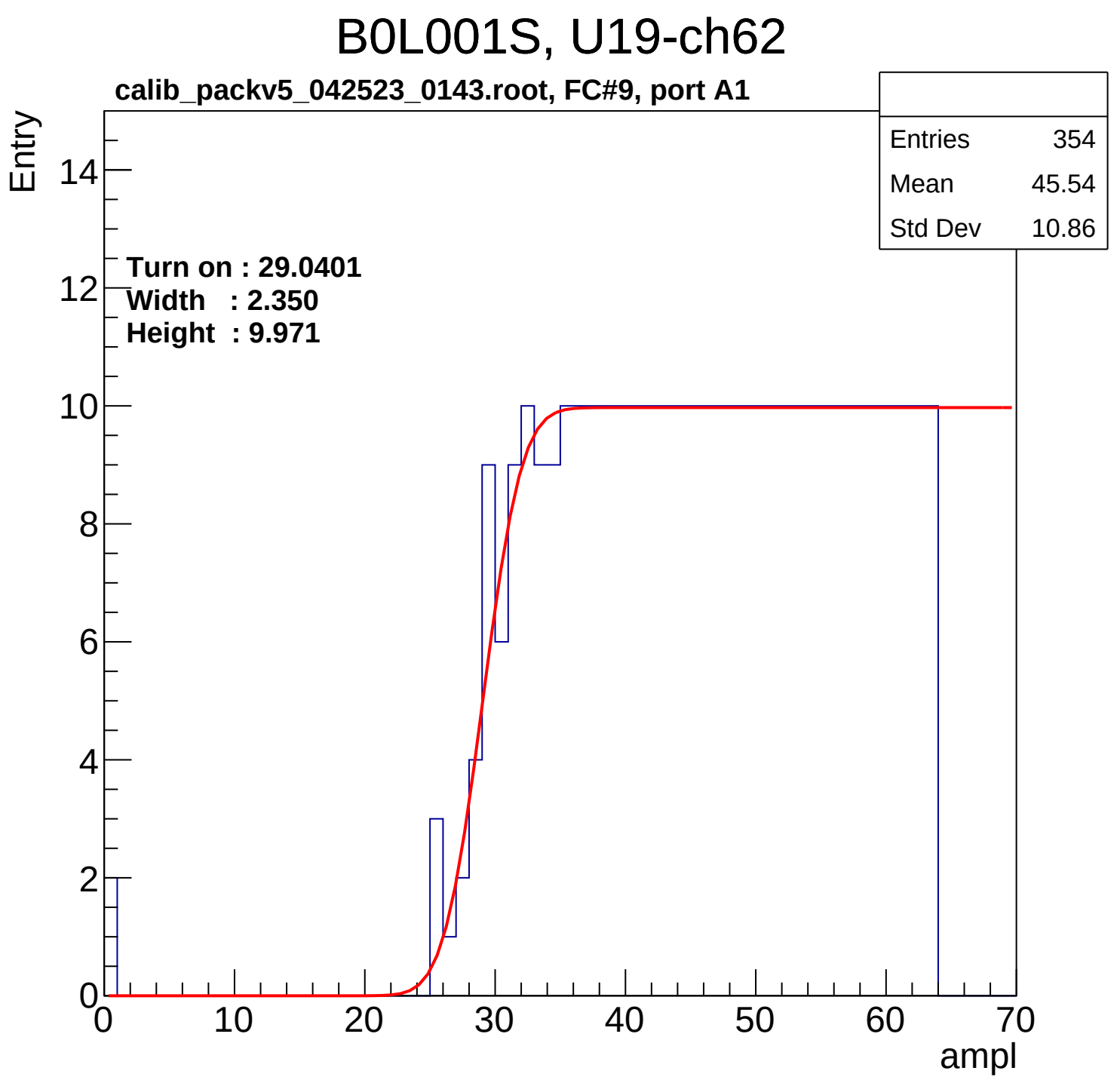
B0L001S, U19-ch62
calib_packv5_042523_0143.root, FC#9, port A1
Entries 354
Mean 45.54
Std Dev 10.86
Turn on : 29.0401
Width : 2.350
Height : 9.971
Entry
ampl
0
2
4
6
8
10
12
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0
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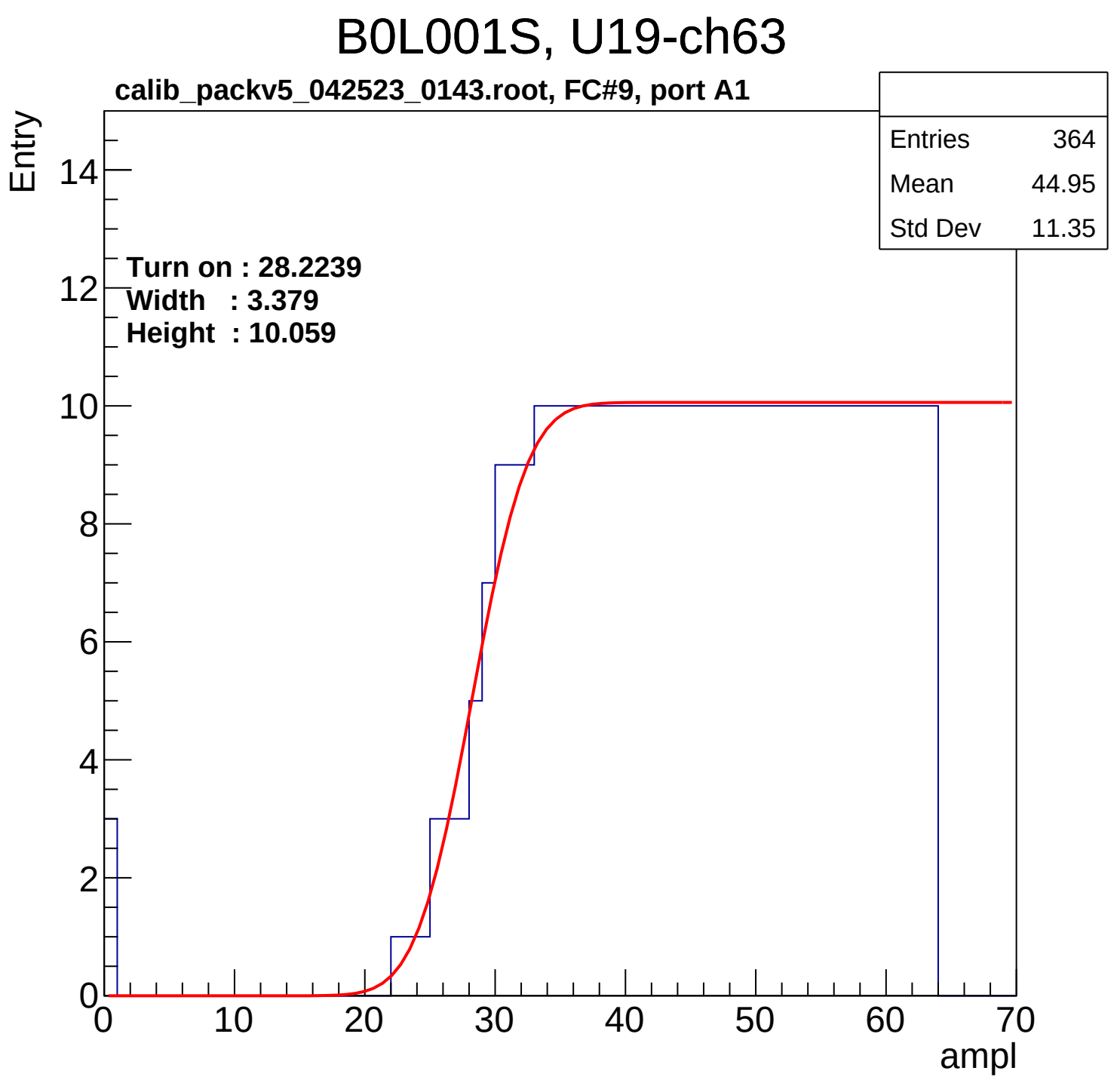
B0L001S, U19-ch63
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 44.95
Std Dev 11.35
Turn on : 28.2239
Width : 3.379
Height : 10.059
Entry
ampl
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2
4
6
8
10
12
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0
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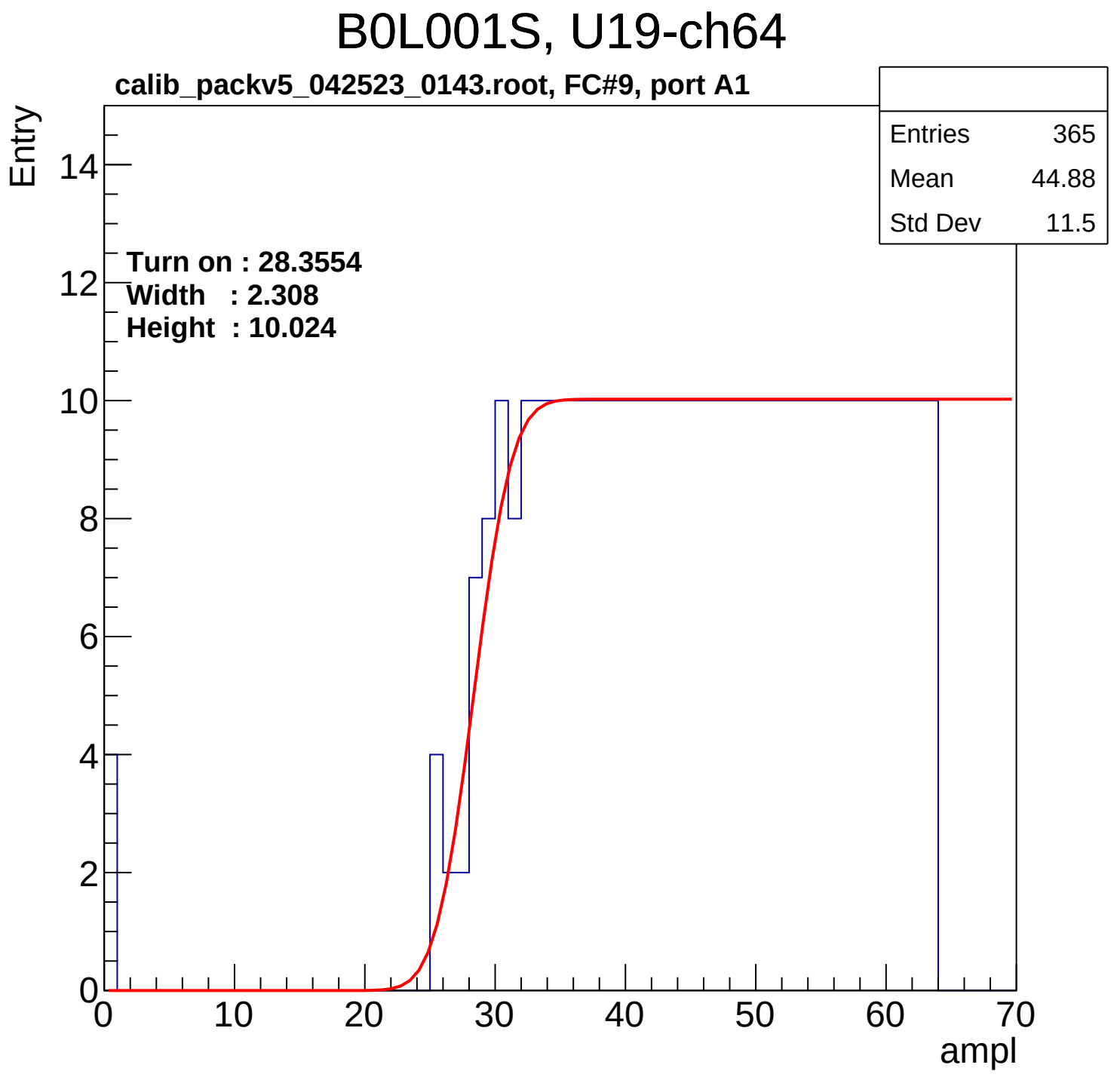
B0L001S, U19-ch64
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 44.88
Std Dev 11.5
Turn on : 28.3554
Width : 2.308
Height : 10.024
Entry
ampl
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2
4
6
8
10
12
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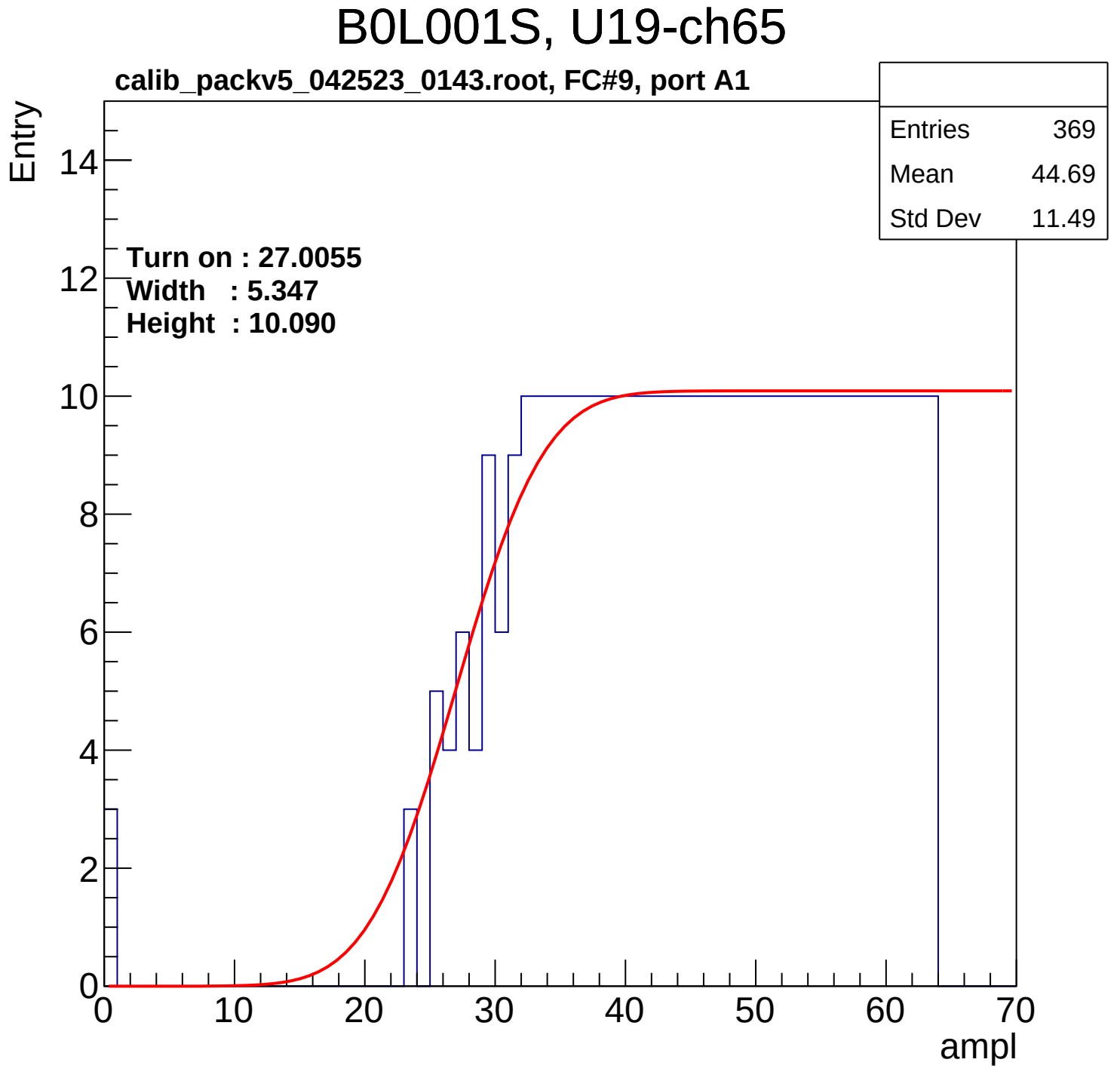
B0L001S, U19-ch65
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.69
Std Dev 11.49
Turn on : 27.0055
Width : 5.347
Height : 10.090
Entry
ampl
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2
4
6
8
10
12
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0
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60
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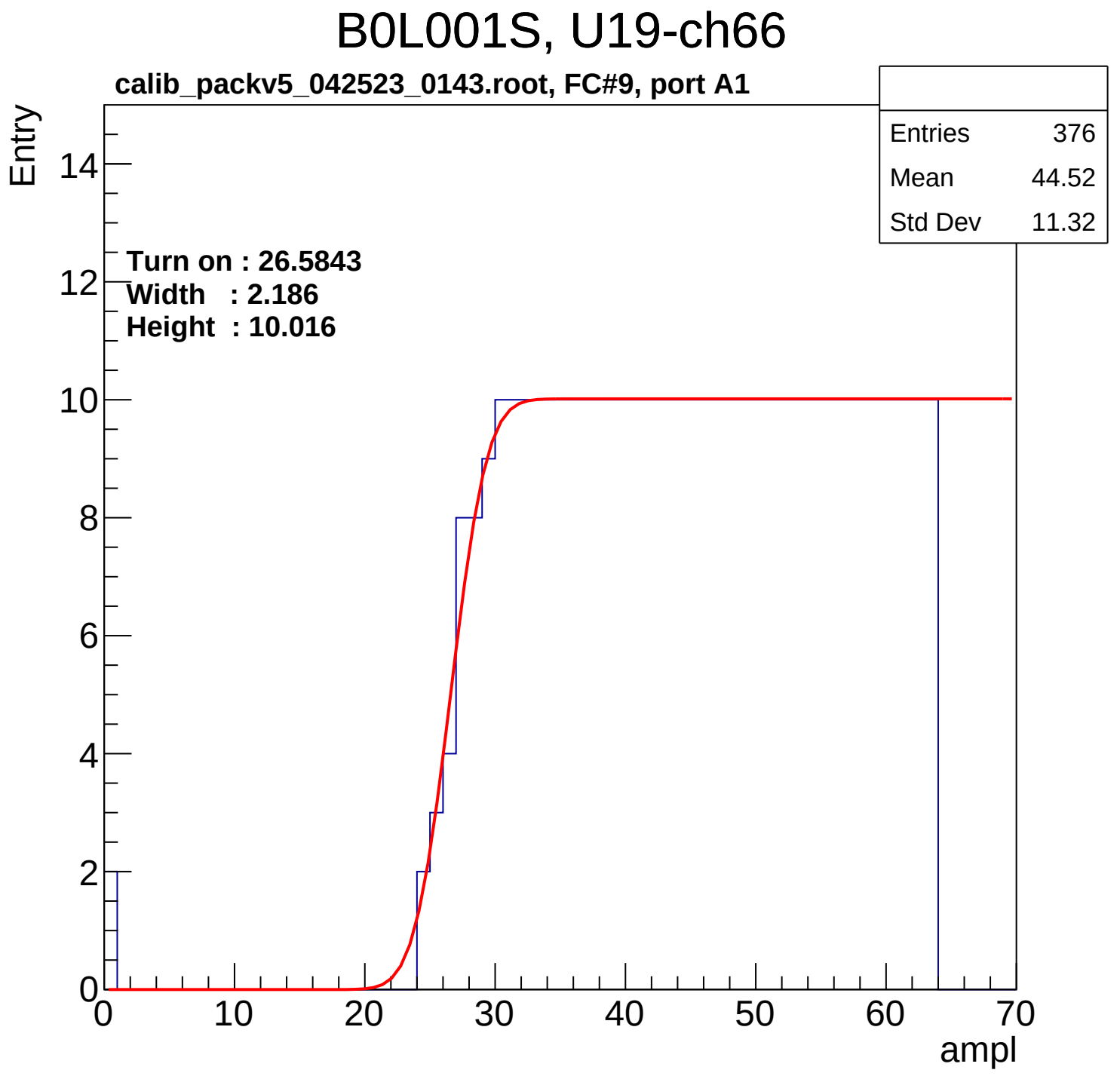
B0L001S, U19-ch66
calib_packv5_042523_0143.root, FC#9, port A1
Entries 376
Mean 44.52
Std Dev 11.32
Turn on : 26.5843
Width : 2.186
Height : 10.016
Entry
ampl
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6
8
10
12
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0
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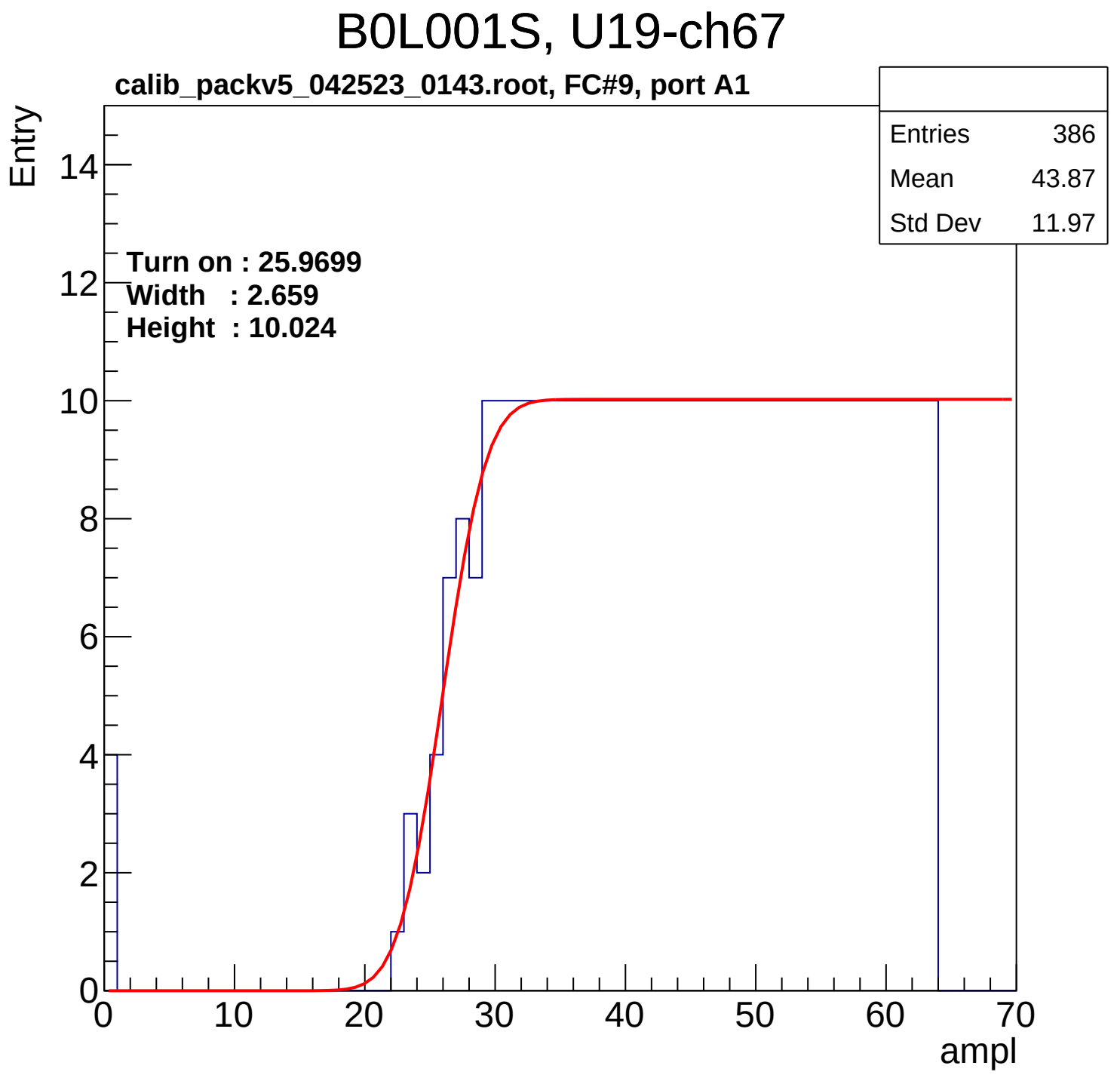
B0L001S, U19-ch67
calib_packv5_042523_0143.root, FC#9, port A1
Entries 386
Mean 43.87
Std Dev 11.97
Turn on : 25.9699
Width : 2.659
Height : 10.024
Entry
ampl
0
2
4
6
8
10
12
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0
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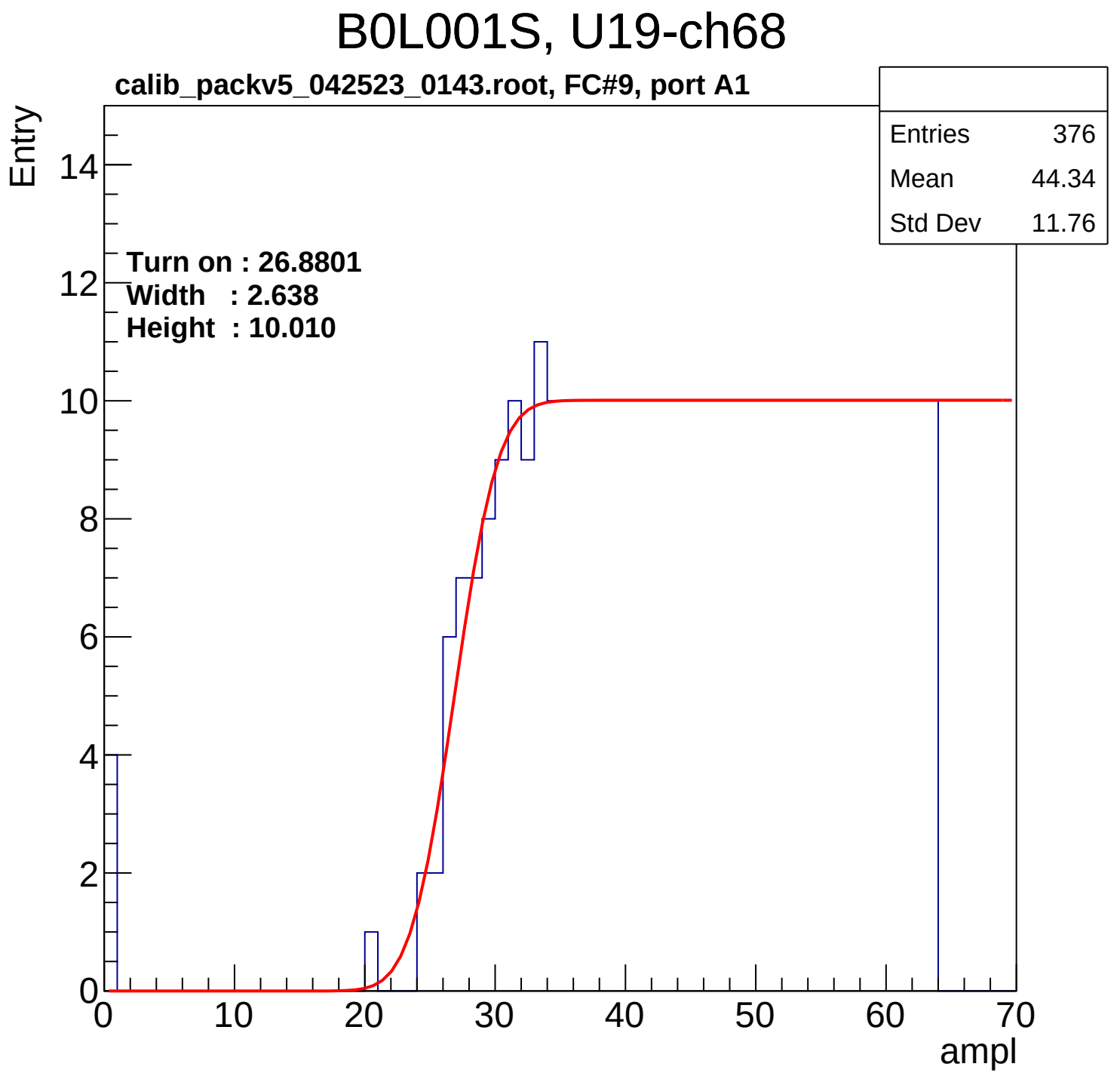
B0L001S, U19-ch68
calib_packv5_042523_0143.root, FC#9, port A1
Entries 376
Mean 44.34
Std Dev 11.76
Turn on : 26.8801
Width : 2.638
Height : 10.010
Entry
ampl
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2
4
6
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10
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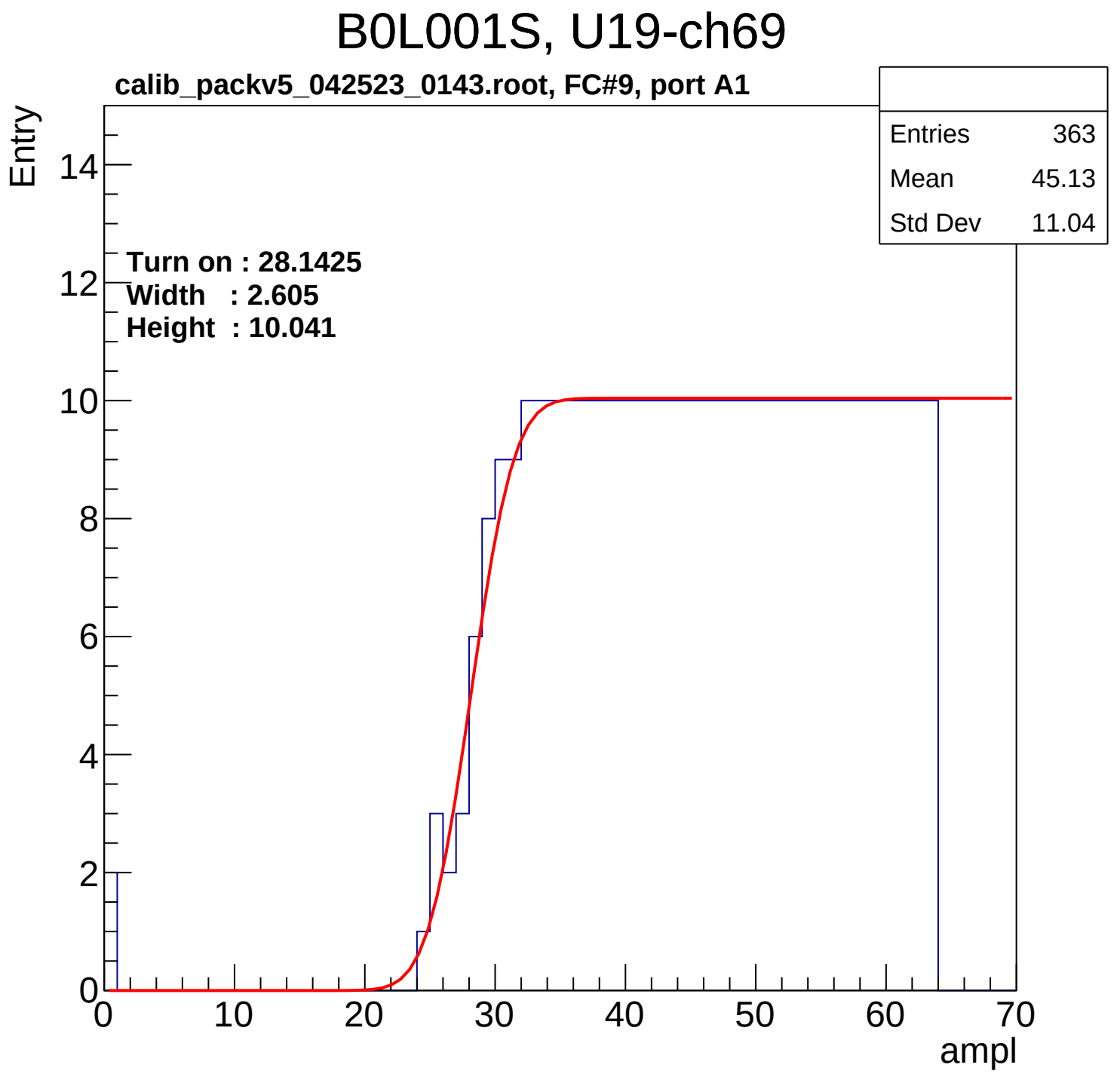
B0L001S, U19-ch69
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 45.13
Std Dev 11.04
Turn on : 28.1425
Width : 2.605
Height : 10.041
Entry
ampl
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8
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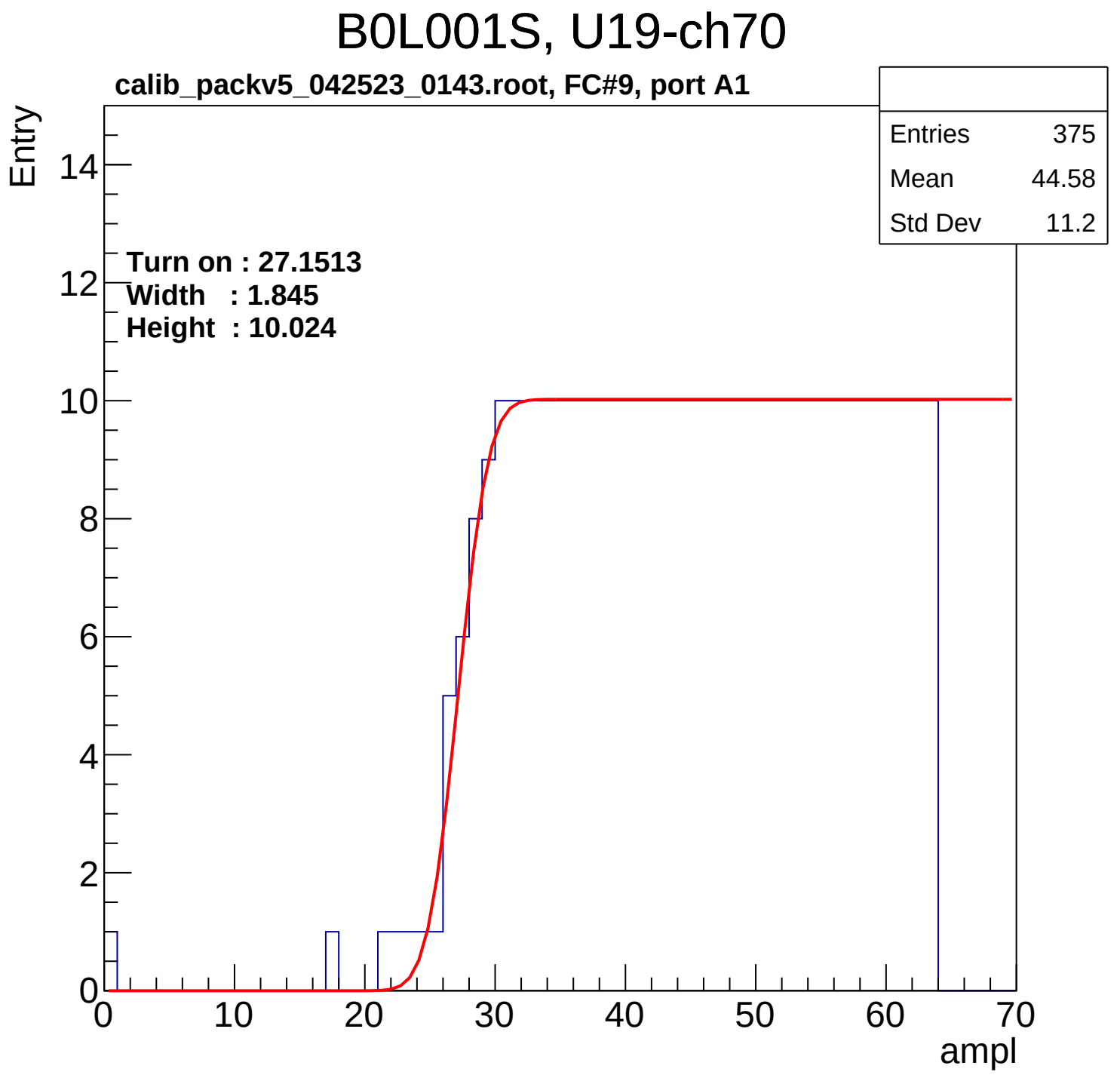
B0L001S, U19-ch70
calib_packv5_042523_0143.root, FC#9, port A1
Entries 375
Mean 44.58
Std Dev 11.2
Turn on : 27.1513
Width : 1.845
Height : 10.024
Entry
ampl
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6
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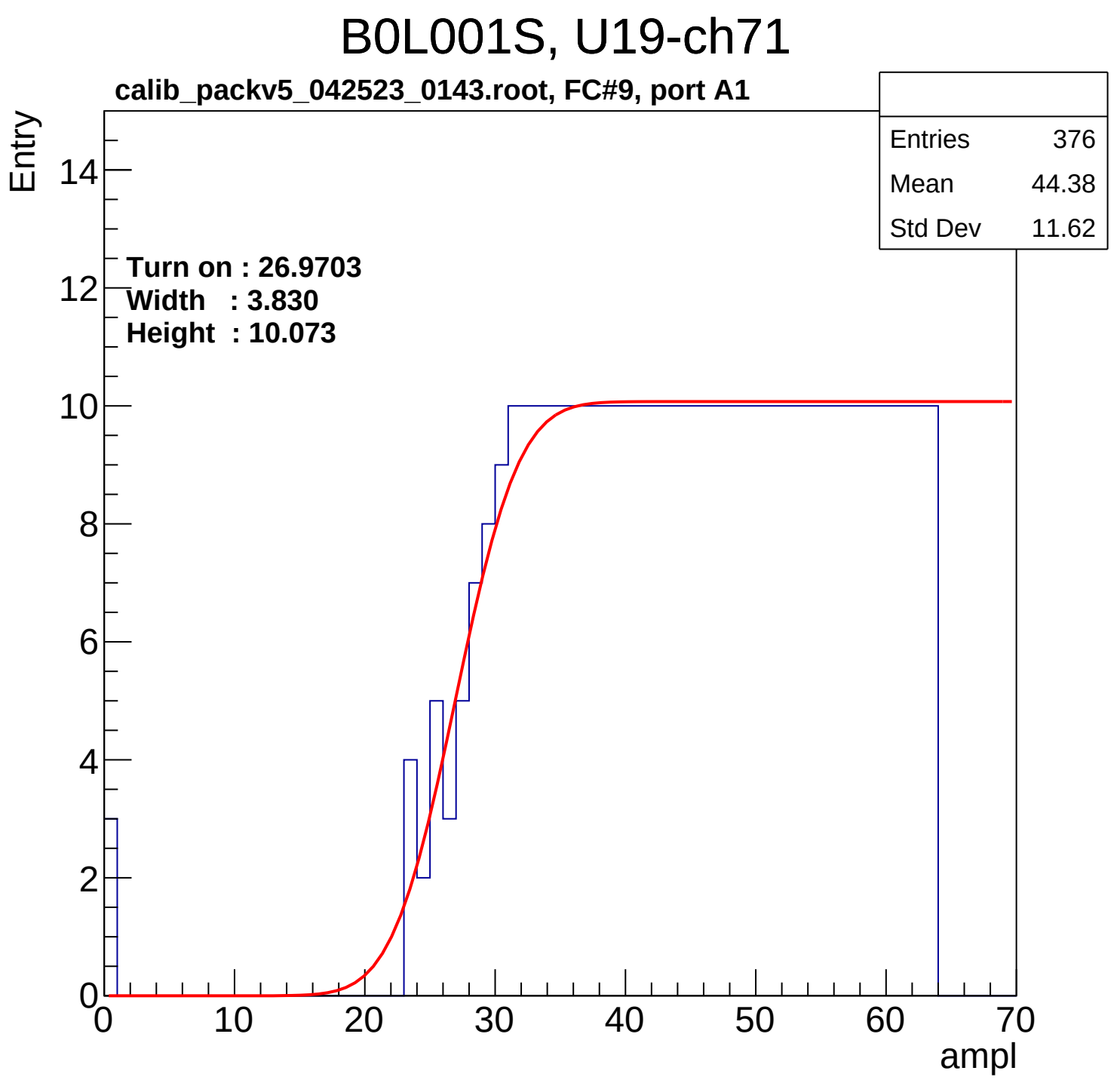
B0L001S, U19-ch71
calib_packv5_042523_0143.root, FC#9, port A1
Entries 376
Mean 44.38
Std Dev 11.62
Turn on : 26.9703
Width : 3.830
Height : 10.073
Entry
ampl
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6
8
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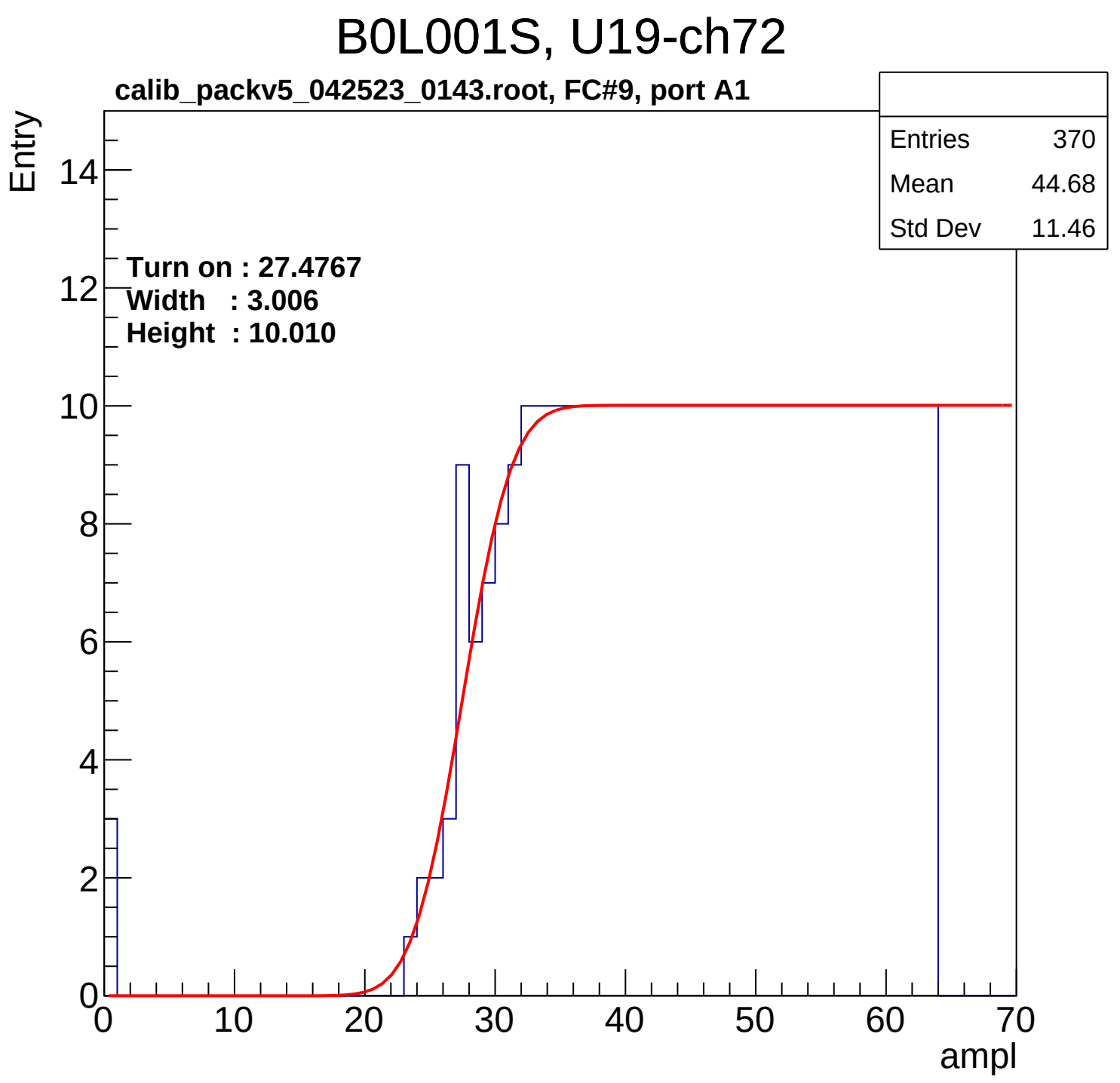
B0L001S, U19-ch72
calib_packv5_042523_0143.root, FC#9, port A1
Entries 370
Mean 44.68
Std Dev 11.46
Turn on : 27.4767
Width : 3.006
Height : 10.010
Entry
ampl
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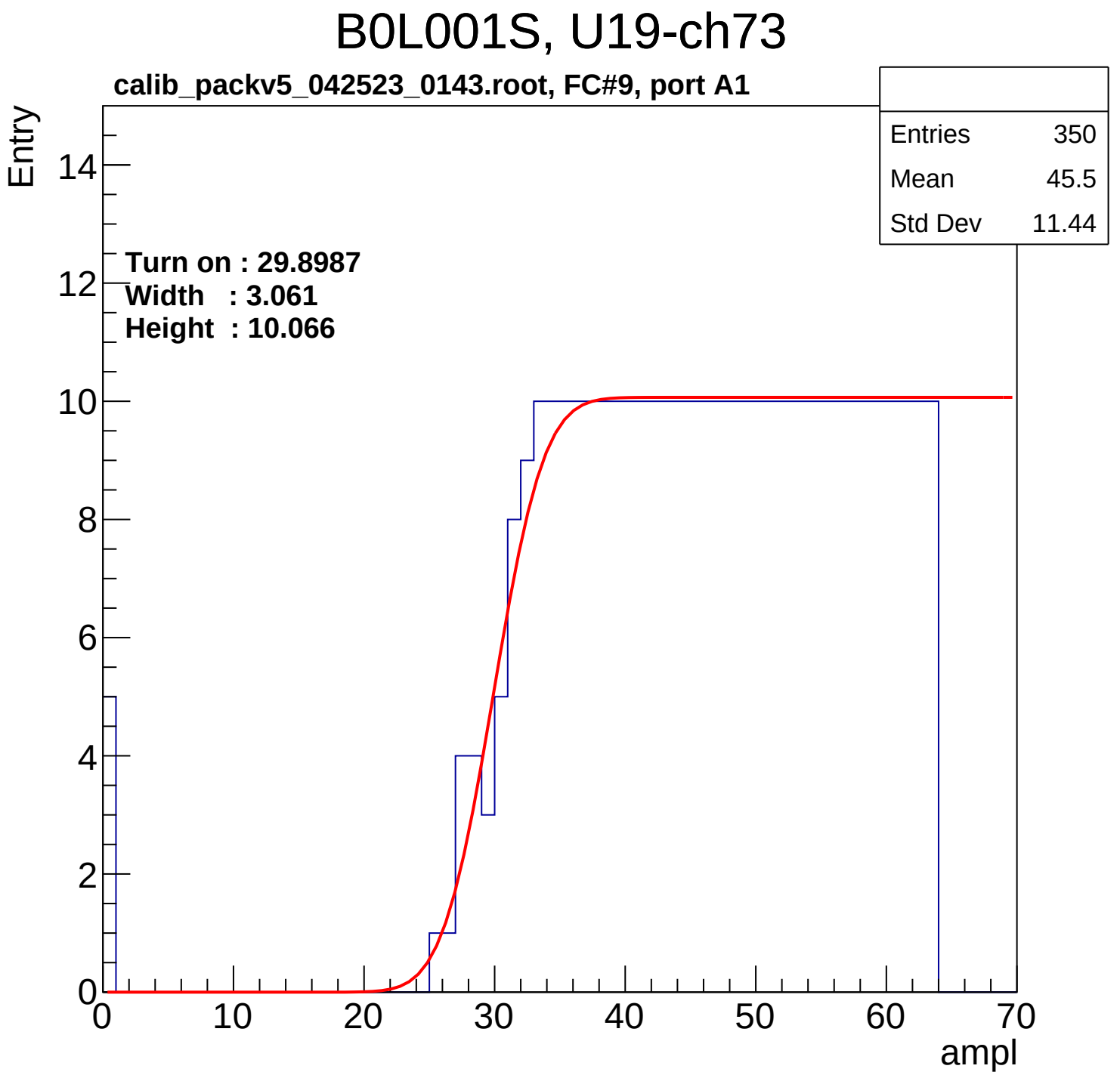
B0L001S, U19-ch73
calib_packv5_042523_0143.root, FC#9, port A1
Entries 350
Mean 45.5
Std Dev 11.44
Turn on : 29.8987
Width : 3.061
Height : 10.066
Entry
ampl
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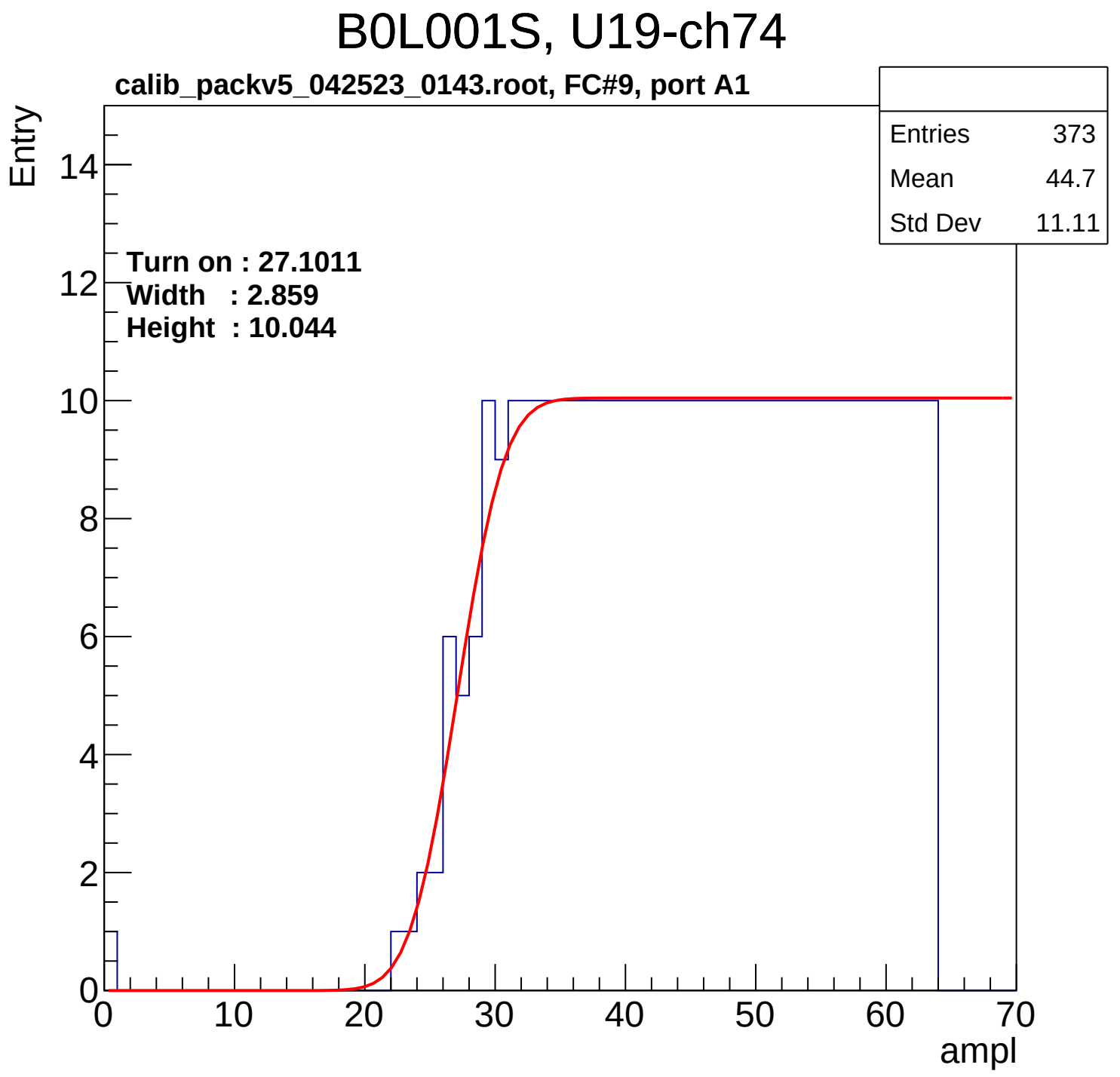
B0L001S, U19-ch74
calib_packv5_042523_0143.root, FC#9, port A1
Entries 373
Mean 44.7
Std Dev 11.11
Turn on : 27.1011
Width : 2.859
Height : 10.044
Entry
ampl
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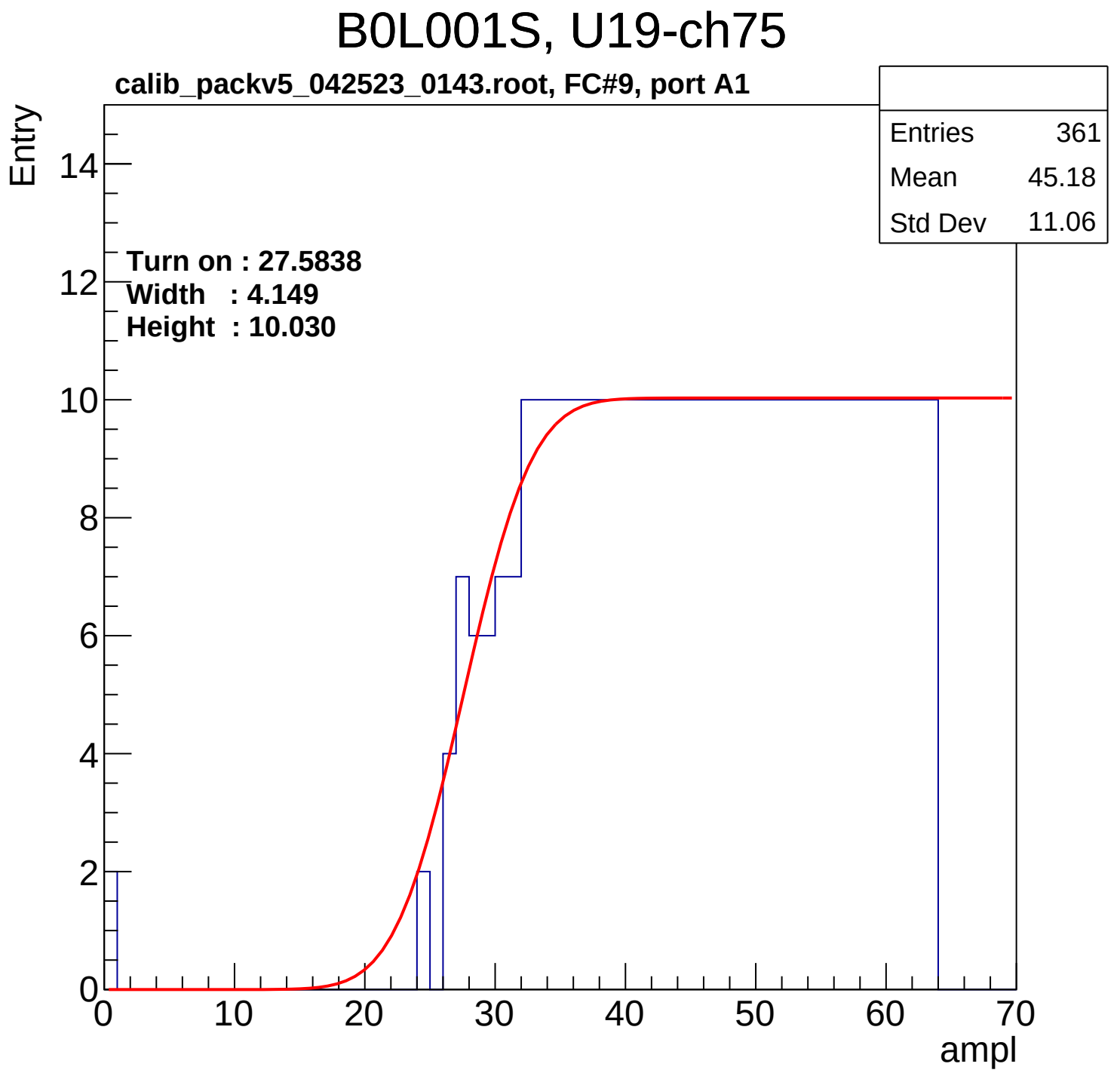
B0L001S, U19-ch75
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 45.18
Std Dev 11.06
Turn on : 27.5838
Width : 4.149
Height : 10.030
Entry
ampl
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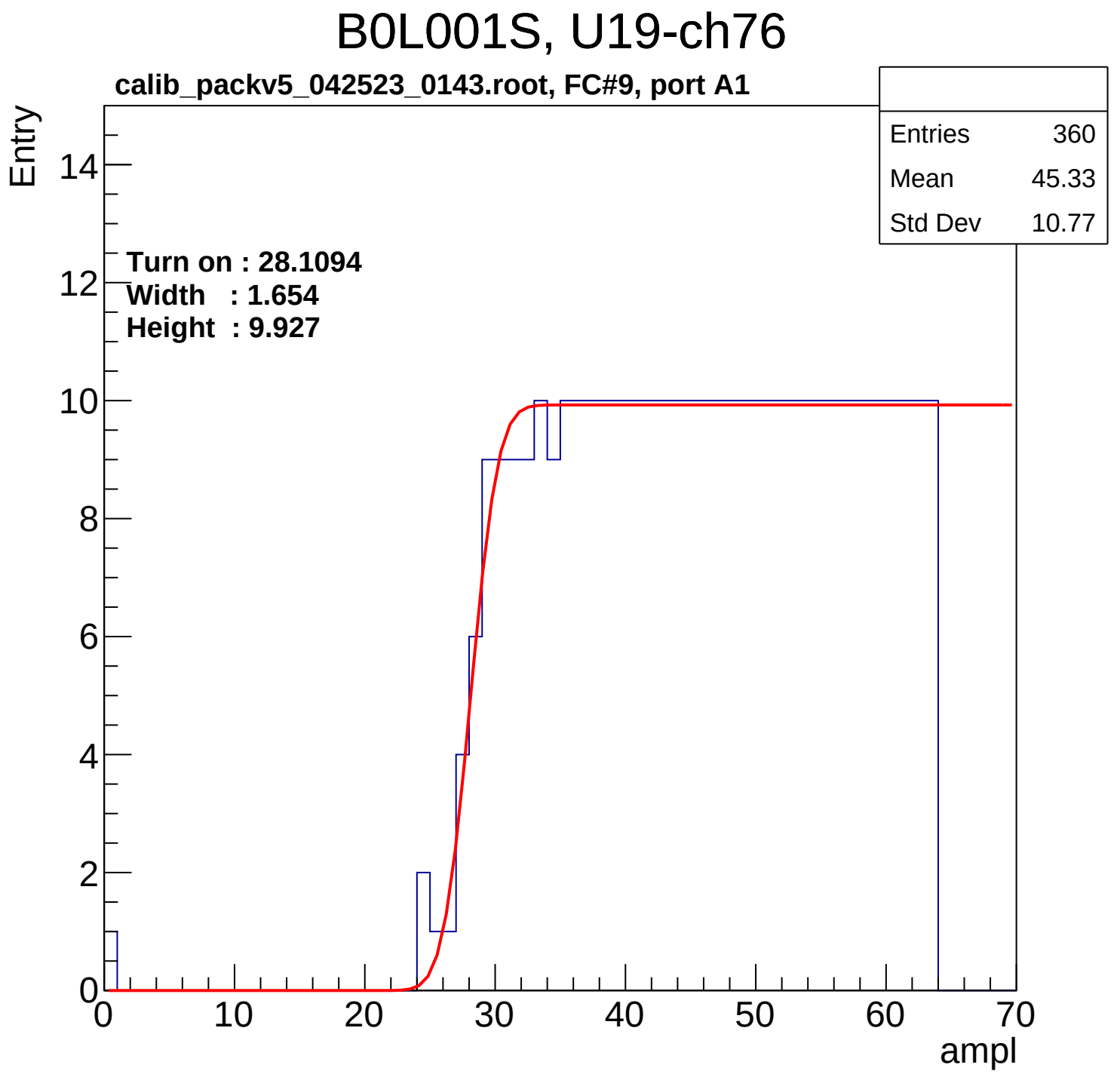
B0L001S, U19-ch76
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 45.33
Std Dev 10.77
Turn on : 28.1094
Width : 1.654
Height : 9.927
Entry
ampl
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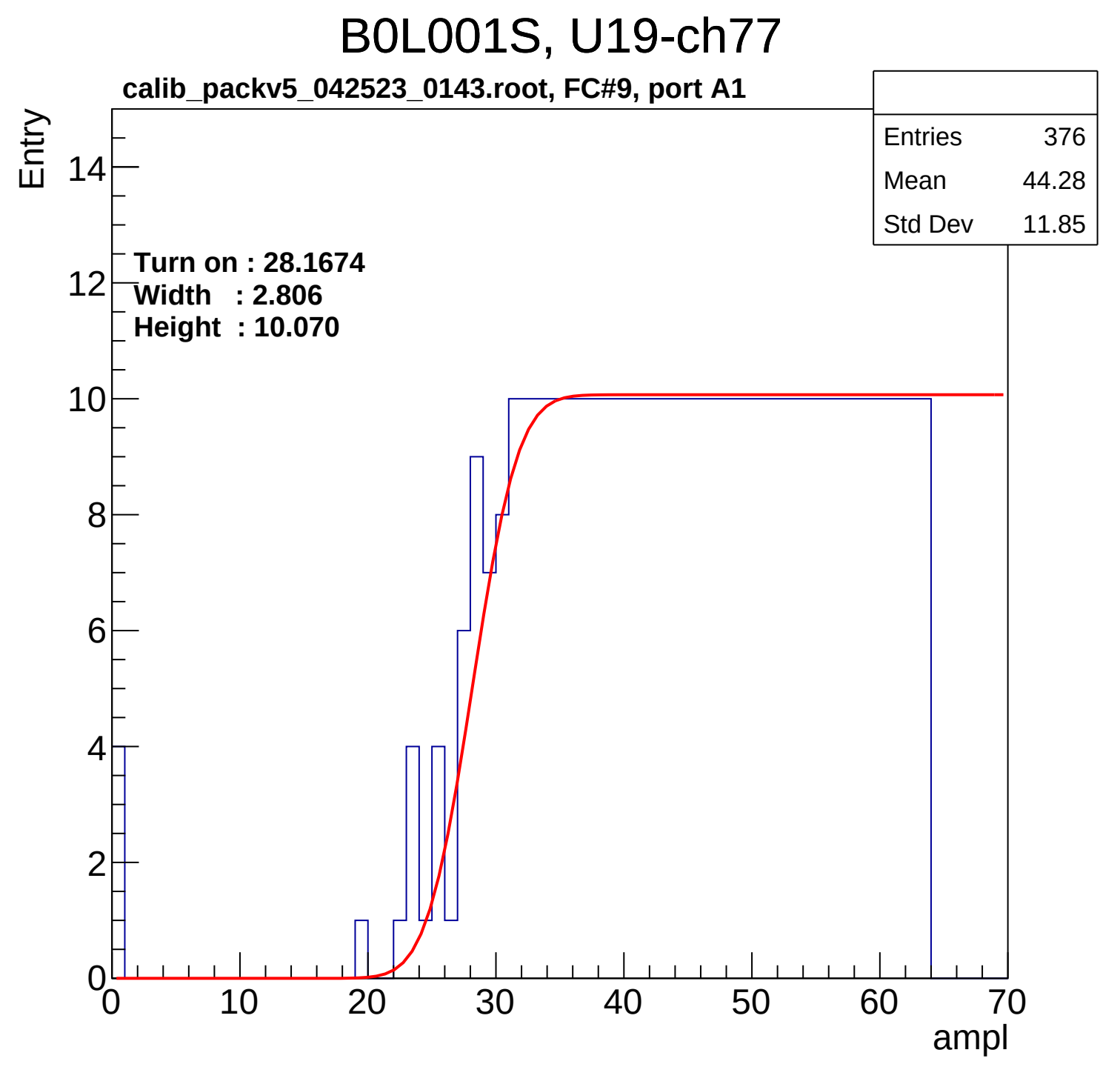
B0L001S, U19-ch77
calib_packv5_042523_0143.root, FC#9, port A1
Entries 376
Mean 44.28
Std Dev 11.85
Turn on : 28.1674
Width : 2.806
Height : 10.070
Entry
ampl
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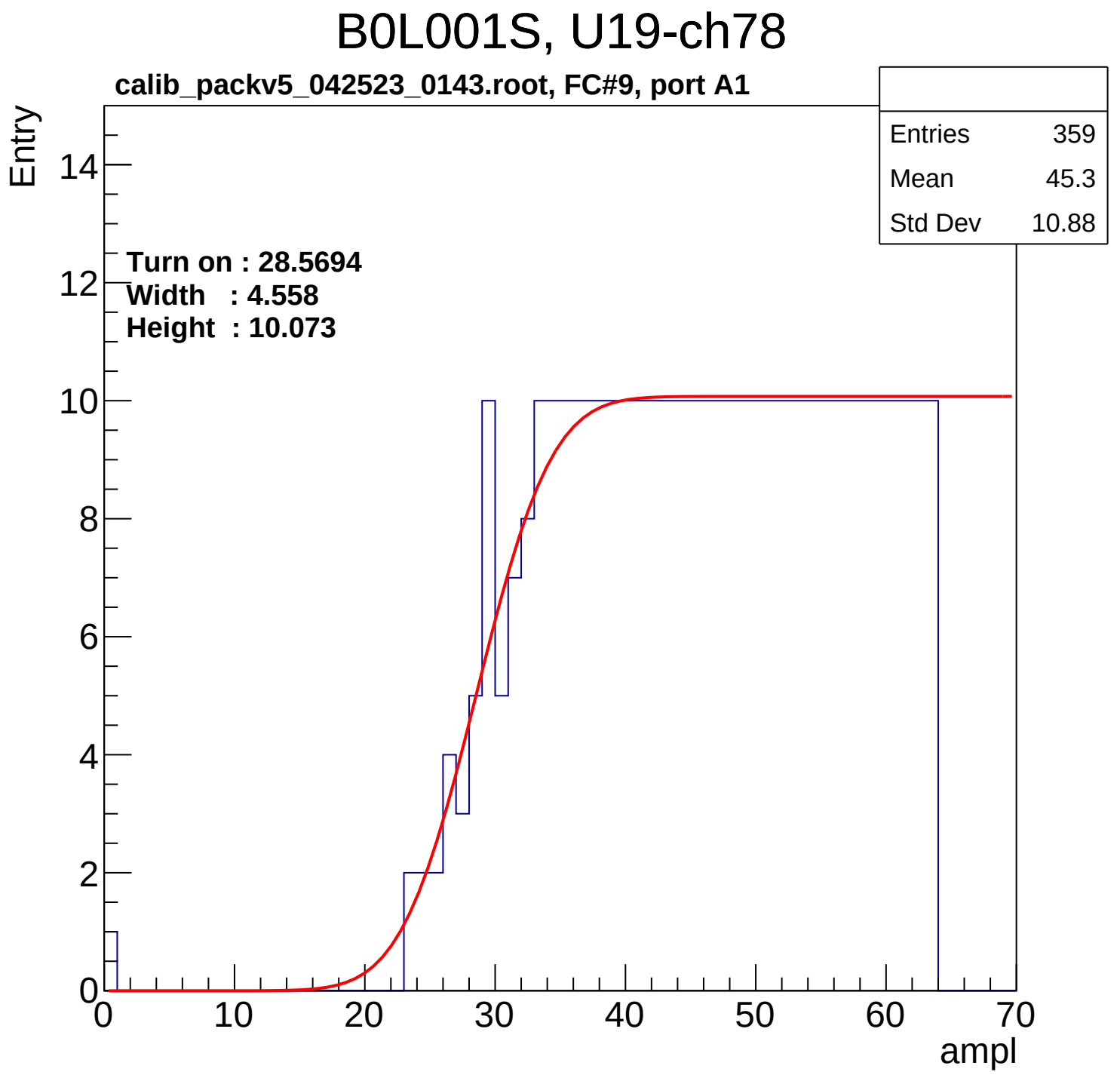
B0L001S, U19-ch78
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 45.3
Std Dev 10.88
Turn on : 28.5694
Width : 4.558
Height : 10.073
Entry
ampl
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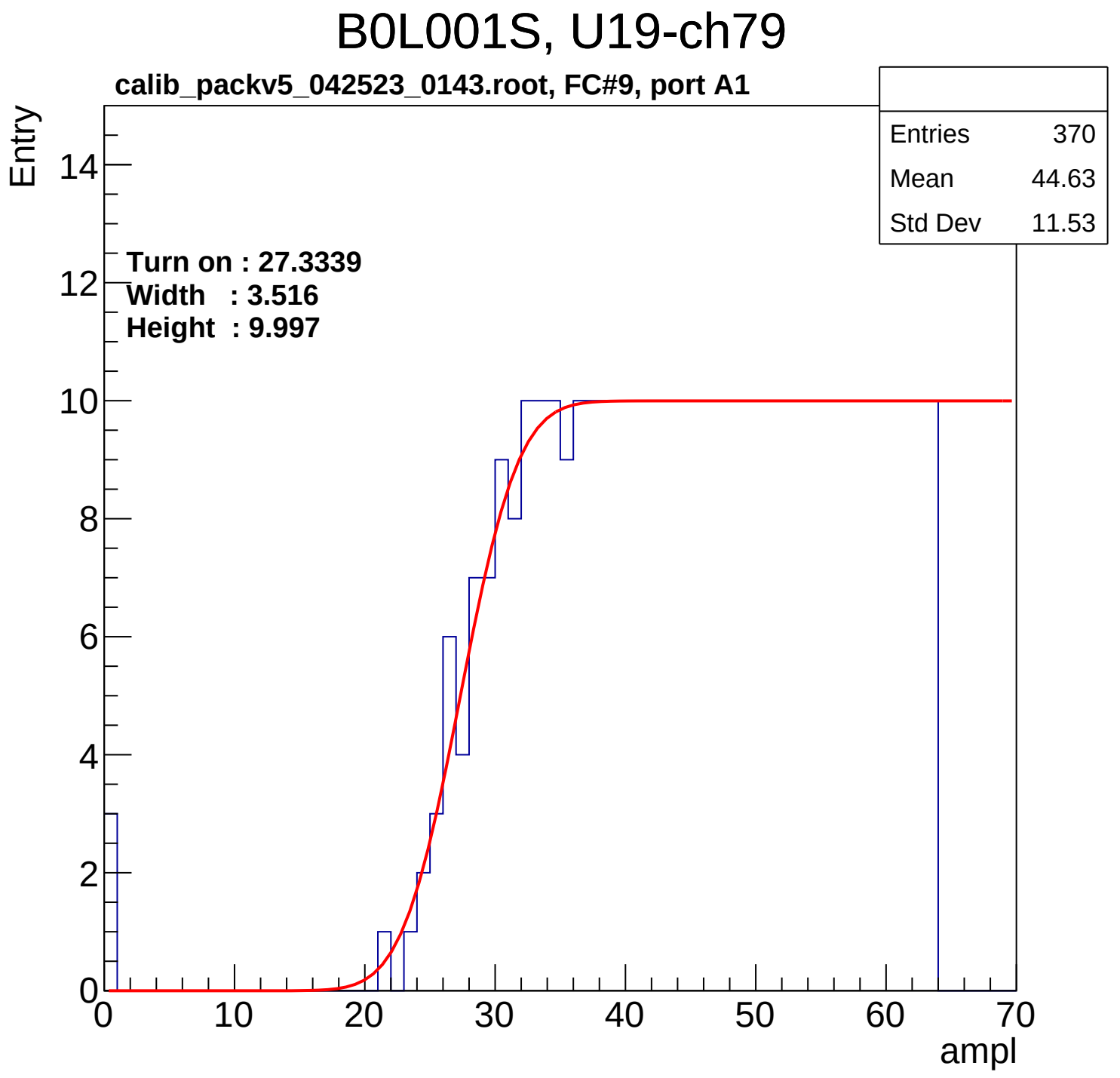
B0L001S, U19-ch79
calib_packv5_042523_0143.root, FC#9, port A1
Entries 370
Mean 44.63
Std Dev 11.53
Turn on : 27.3339
Width : 3.516
Height : 9.997
Entry
ampl
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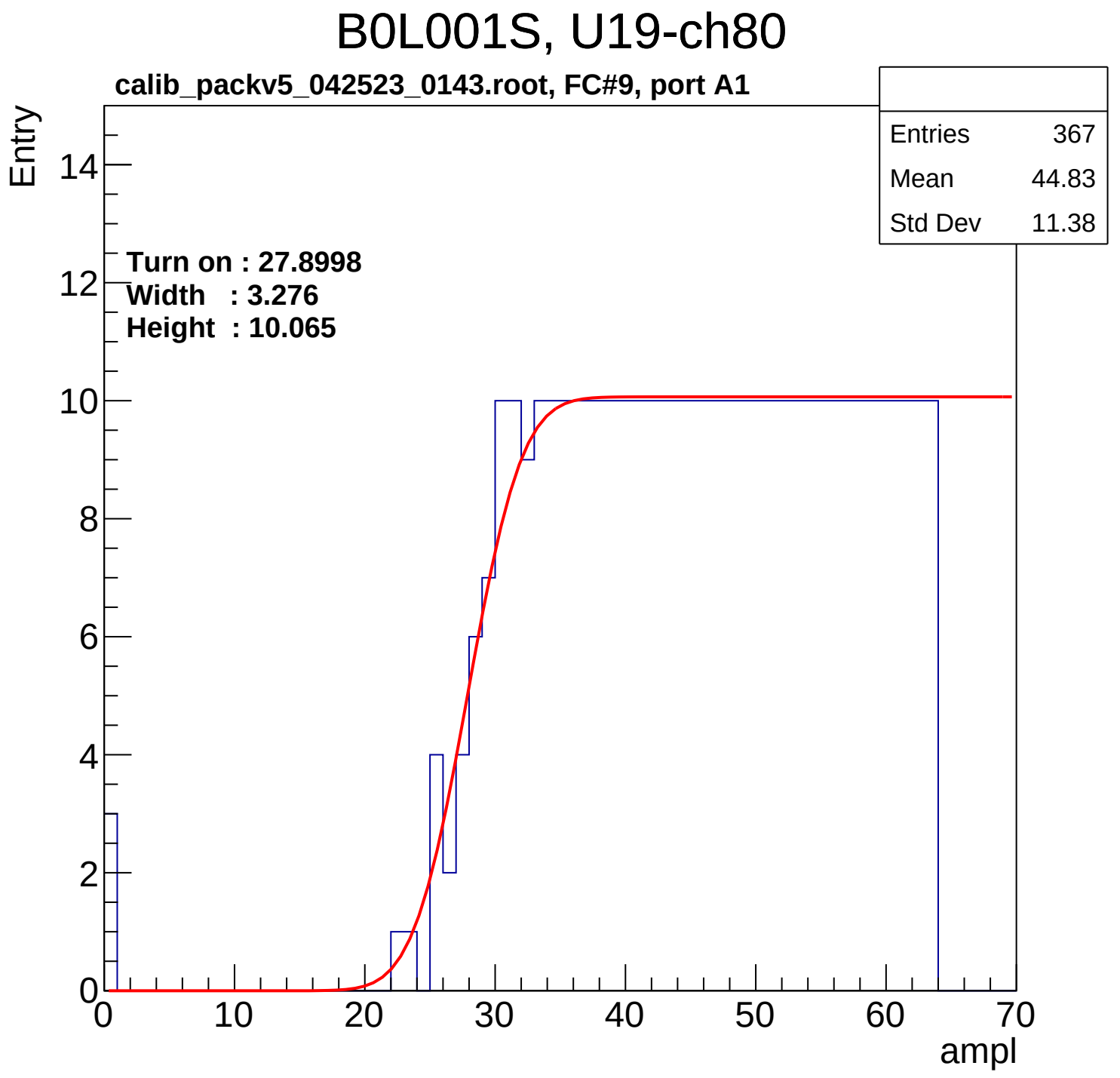
B0L001S, U19-ch80
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.83
Std Dev 11.38
Turn on : 27.8998
Width : 3.276
Height : 10.065
Entry
ampl
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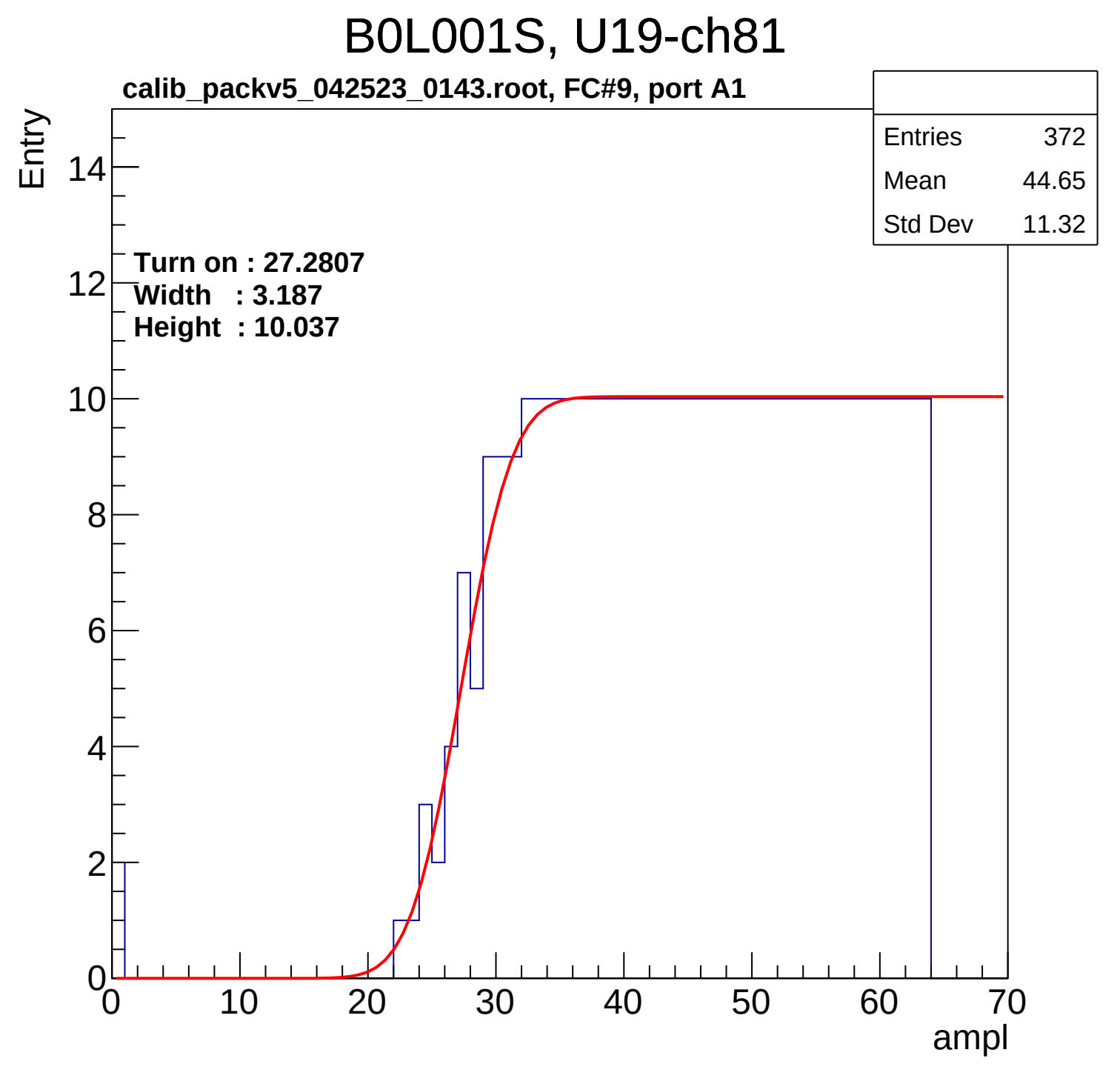
B0L001S, U19-ch81
calib_packv5_042523_0143.root, FC#9, port A1
Entries 372
Mean 44.65
Std Dev 11.32
Turn on : 27.2807
Width : 3.187
Height : 10.037
Entry
ampl
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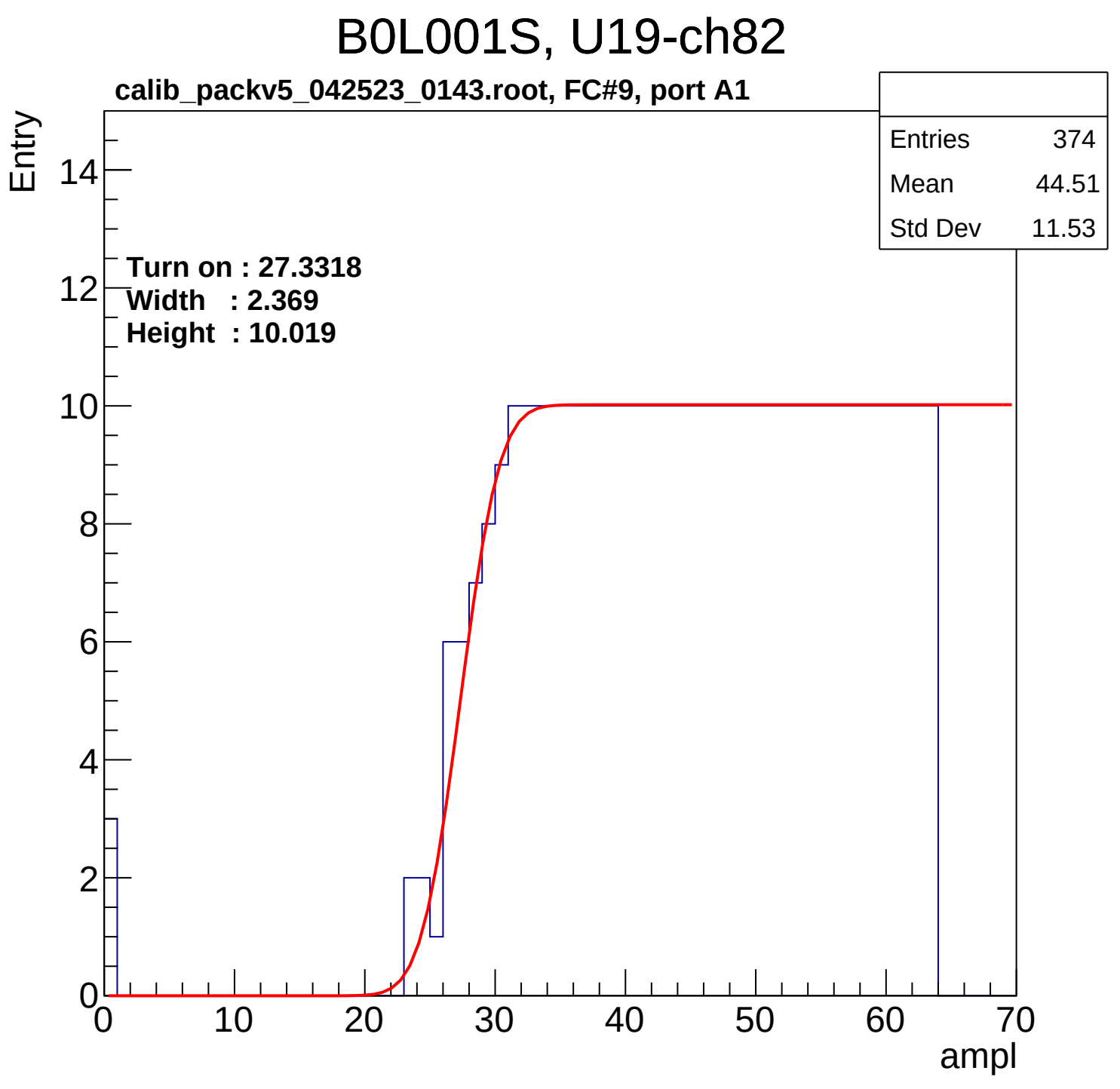
B0L001S, U19-ch82
calib_packv5_042523_0143.root, FC#9, port A1
Entries 374
Mean 44.51
Std Dev 11.53
Turn on : 27.3318
Width : 2.369
Height : 10.019
Entry
ampl
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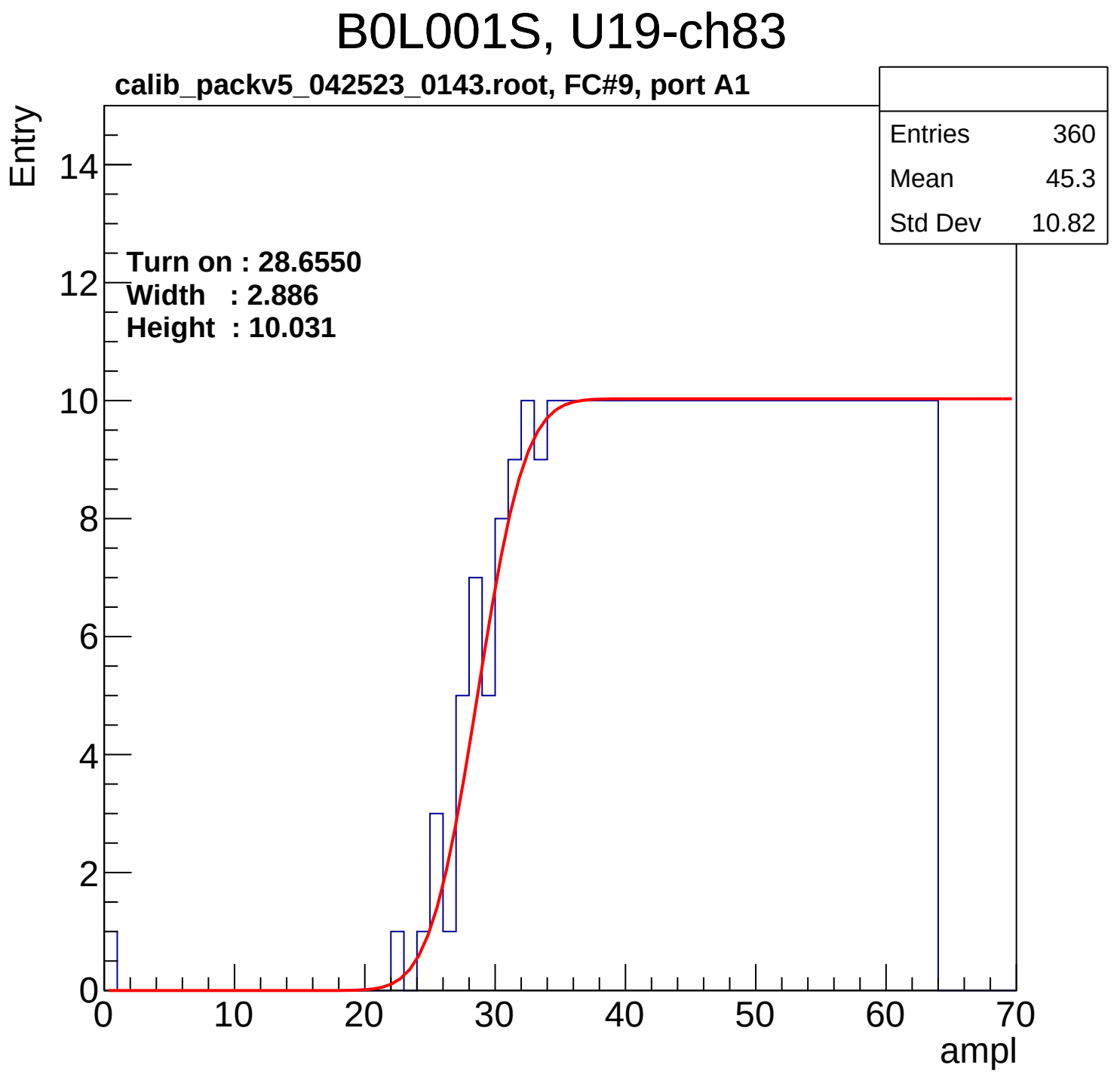
B0L001S, U19-ch83
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 45.3
Std Dev 10.82
Turn on : 28.6550
Width : 2.886
Height : 10.031
Entry
ampl
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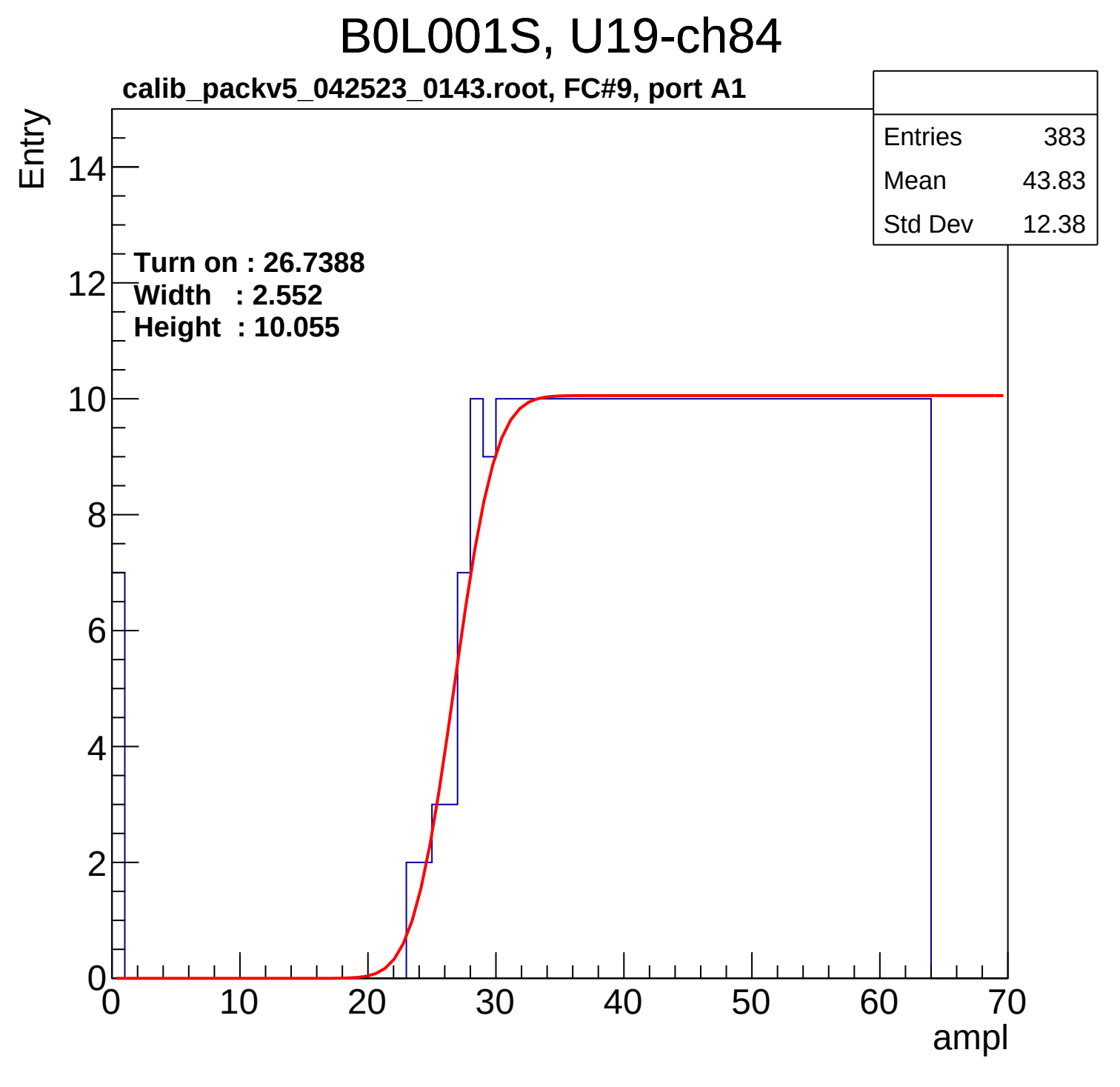
B0L001S, U19-ch84
calib_packv5_042523_0143.root, FC#9, port A1
Entries 383
Mean 43.83
Std Dev 12.38
Turn on : 26.7388
Width : 2.552
Height : 10.055
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ampl
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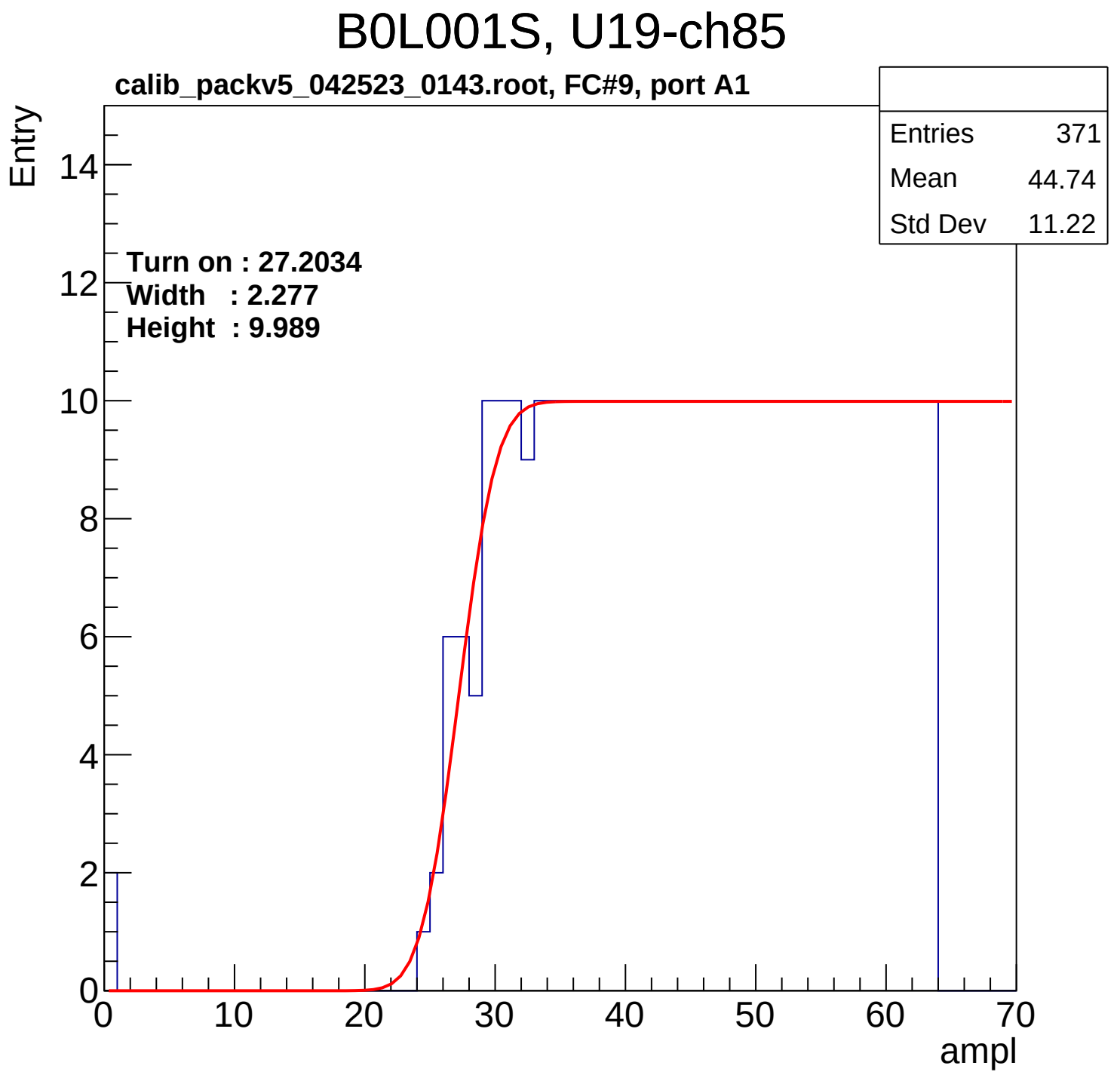
B0L001S, U19-ch85
calib_packv5_042523_0143.root, FC#9, port A1
Entries 371
Mean 44.74
Std Dev 11.22
Turn on : 27.2034
Width : 2.277
Height : 9.989
Entry
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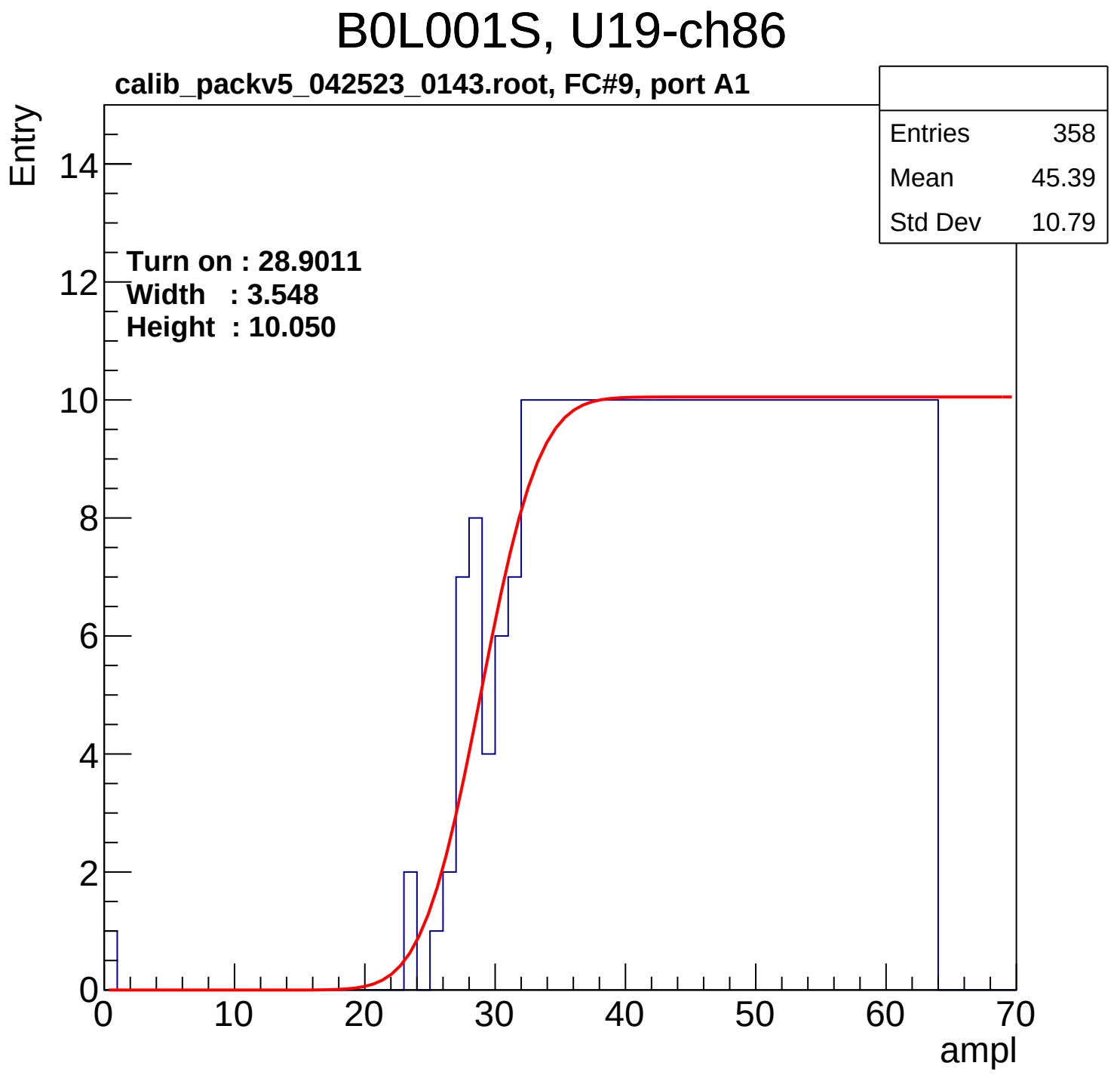
B0L001S, U19-ch86
calib_packv5_042523_0143.root, FC#9, port A1
Entries 358
Mean 45.39
Std Dev 10.79
Turn on : 28.9011
Width : 3.548
Height : 10.050
Entry
ampl
0
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4
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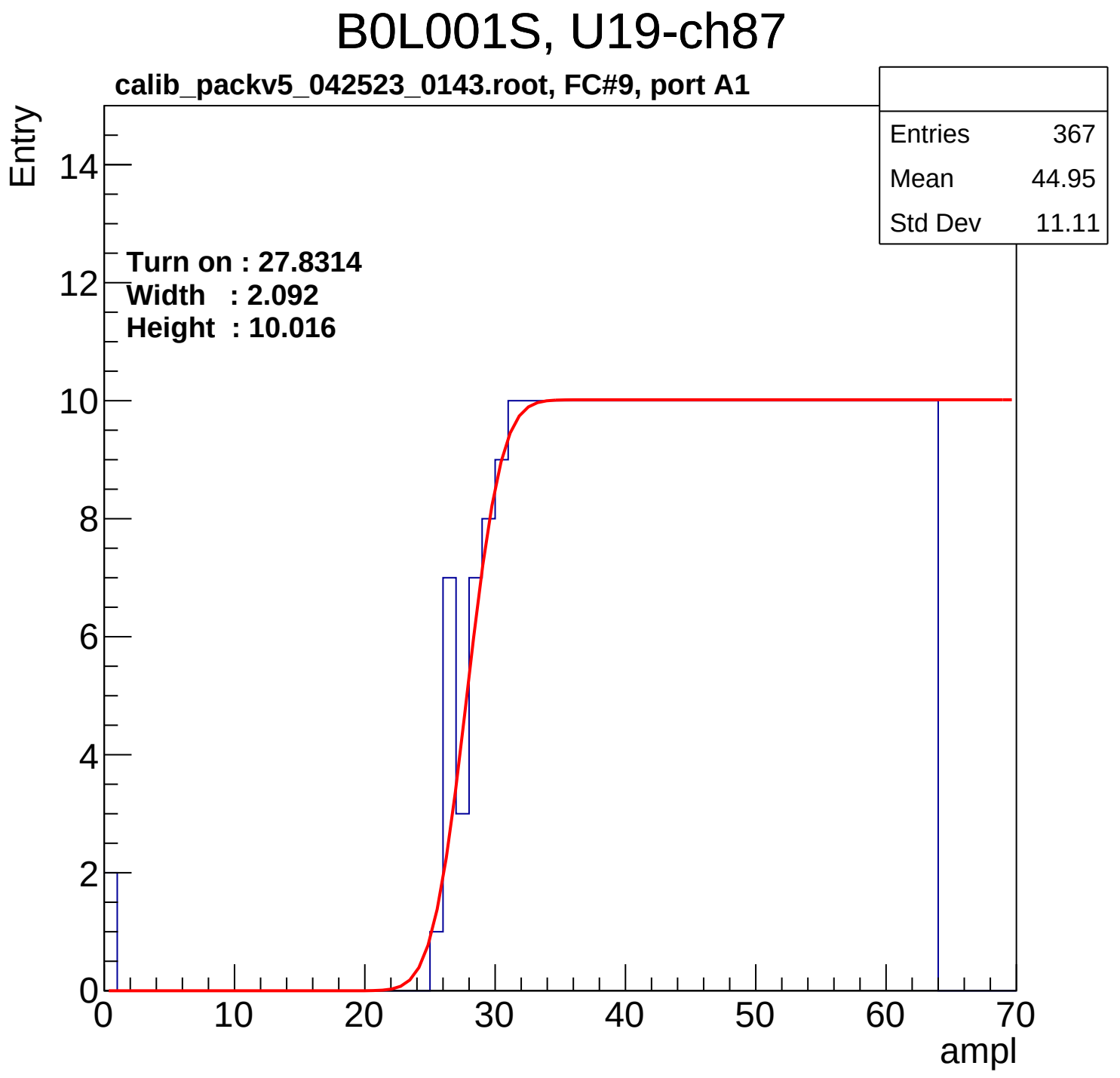
B0L001S, U19-ch87
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.95
Std Dev 11.11
Turn on : 27.8314
Width : 2.092
Height : 10.016
Entry
ampl
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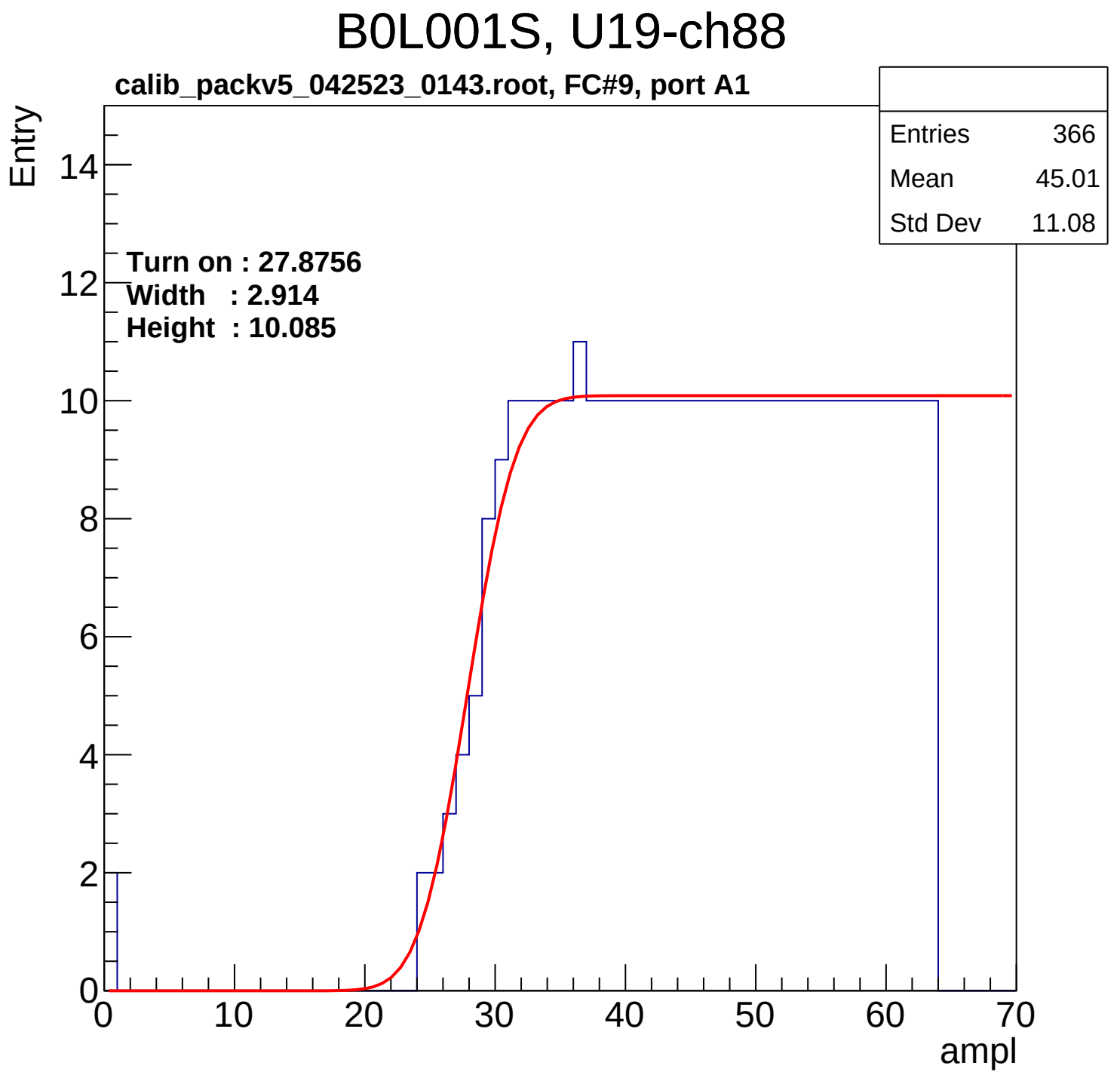
B0L001S, U19-ch88
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 45.01
Std Dev 11.08
Turn on : 27.8756
Width : 2.914
Height : 10.085
Entry
ampl
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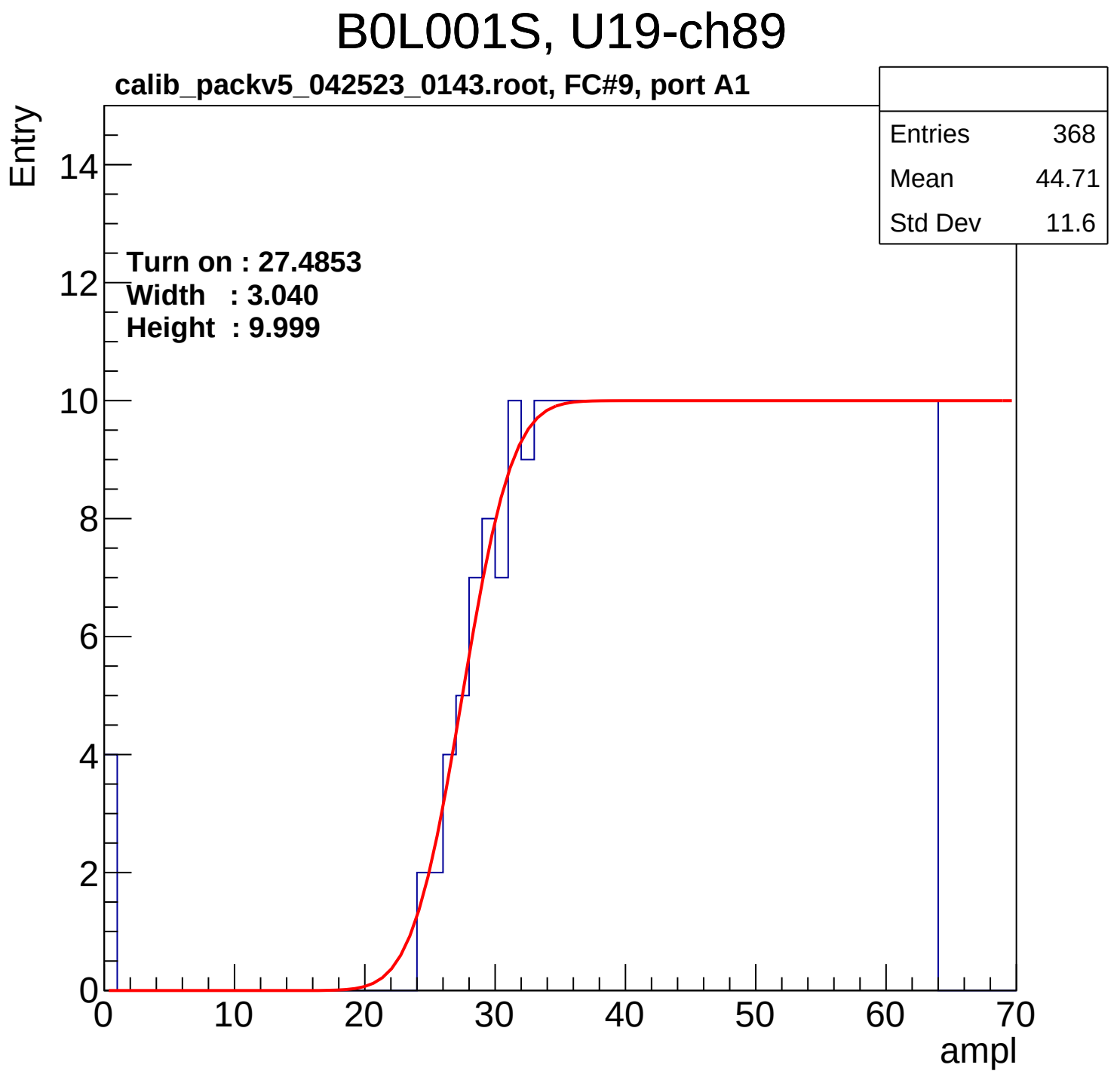
B0L001S, U19-ch89
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.71
Std Dev 11.6
Turn on : 27.4853
Width : 3.040
Height : 9.999
Entry
ampl
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2
4
6
8
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0
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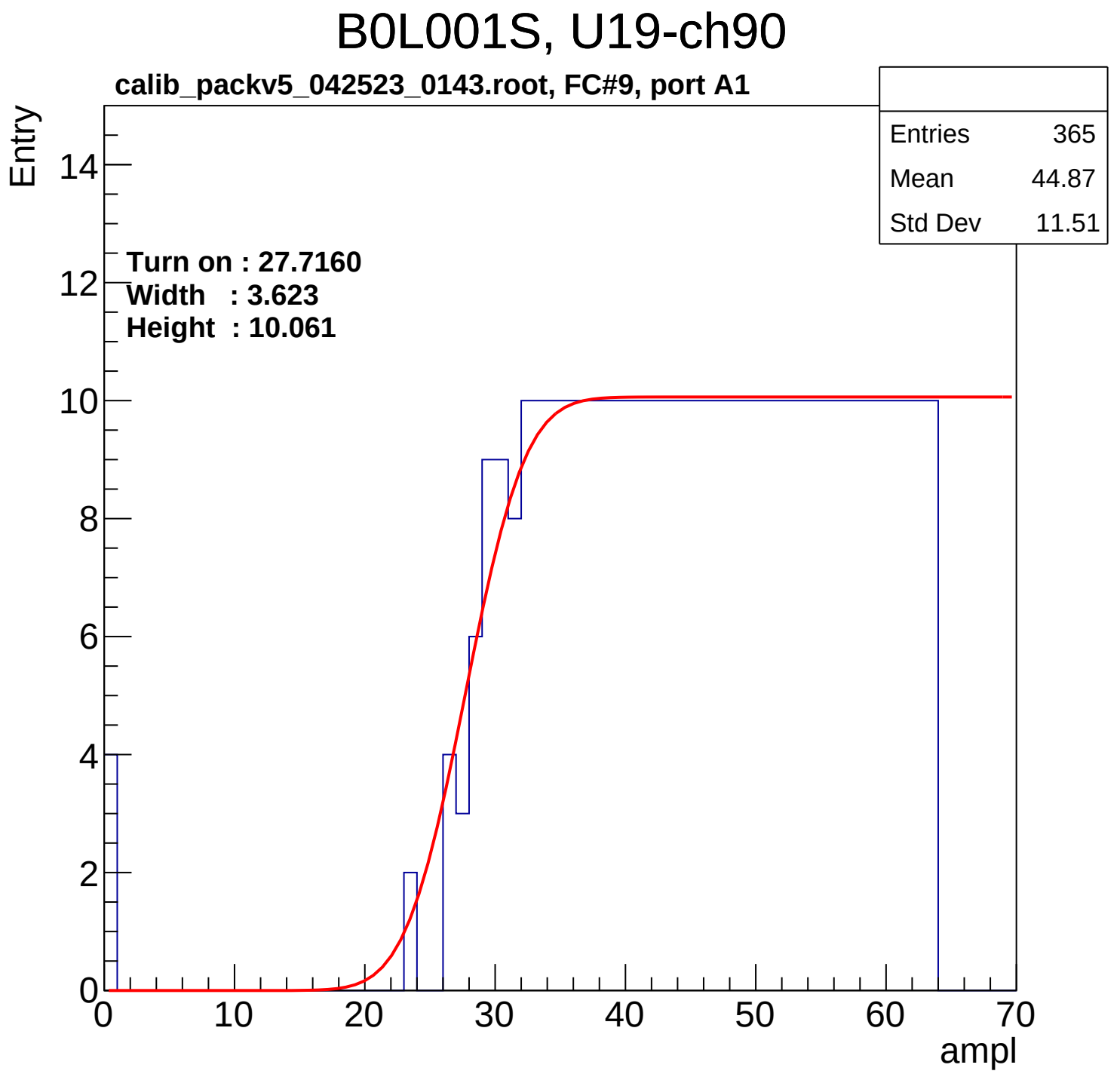
B0L001S, U19-ch90
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 44.87
Std Dev 11.51
Turn on : 27.7160
Width : 3.623
Height : 10.061
Entry
ampl
0
2
4
6
8
10
12
14
0
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60
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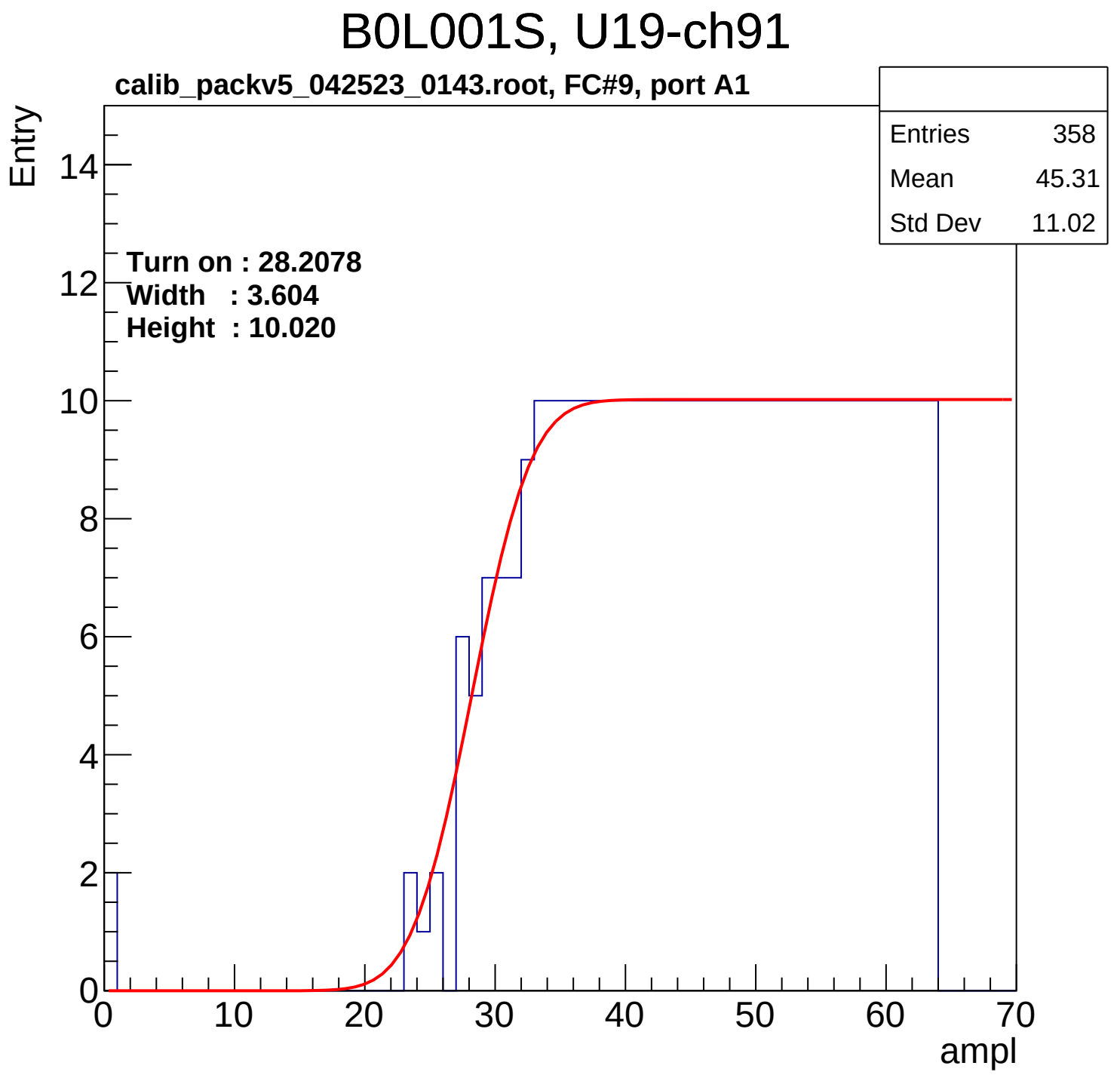
B0L001S, U19-ch91
calib_packv5_042523_0143.root, FC#9, port A1
Entries 358
Mean 45.31
Std Dev 11.02
Turn on : 28.2078
Width : 3.604
Height : 10.020
Entry
ampl
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2
4
6
8
10
12
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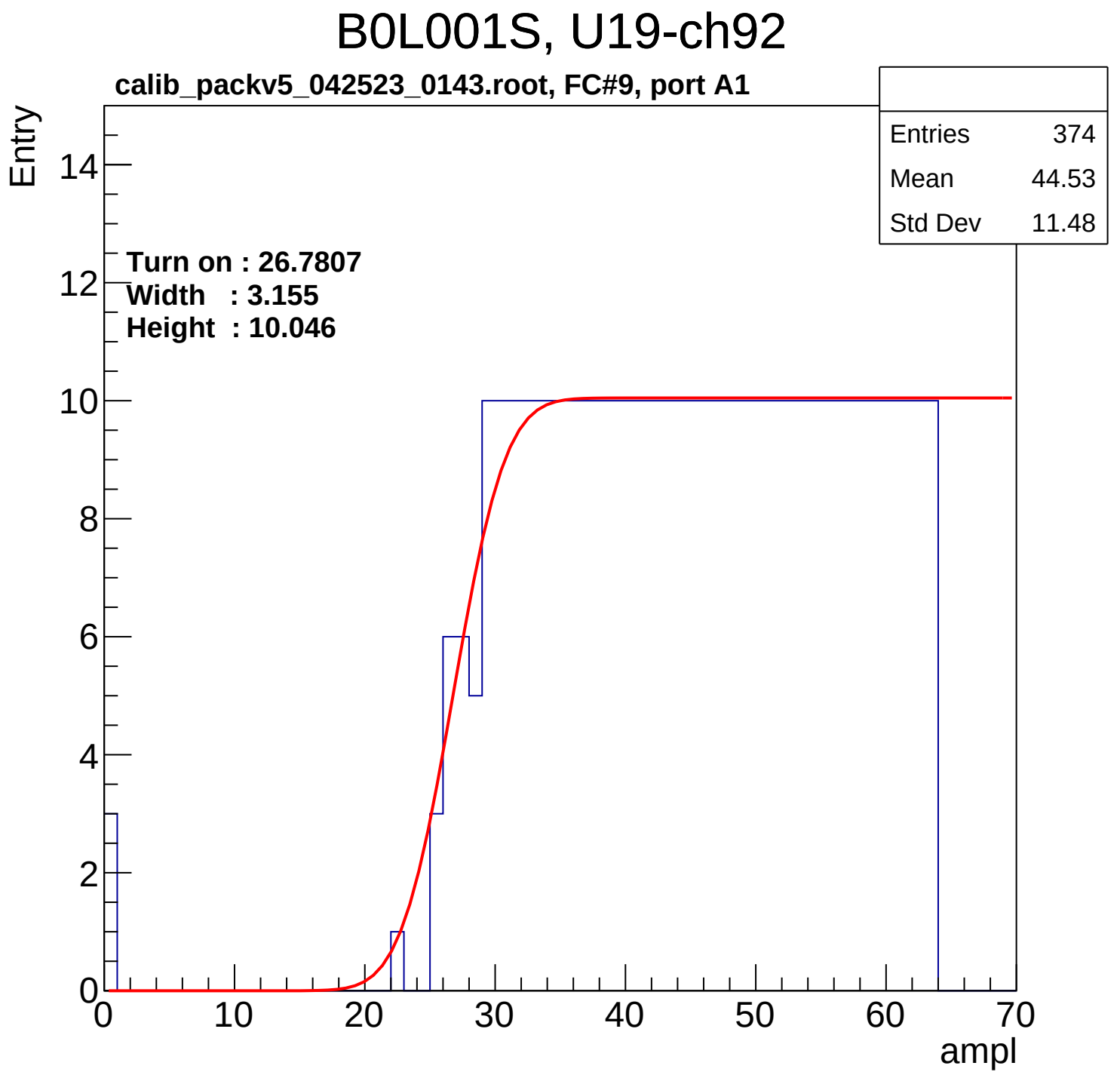
B0L001S, U19-ch92
calib_packv5_042523_0143.root, FC#9, port A1
Entries 374
Mean 44.53
Std Dev 11.48
Turn on : 26.7807
Width : 3.155
Height : 10.046
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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60
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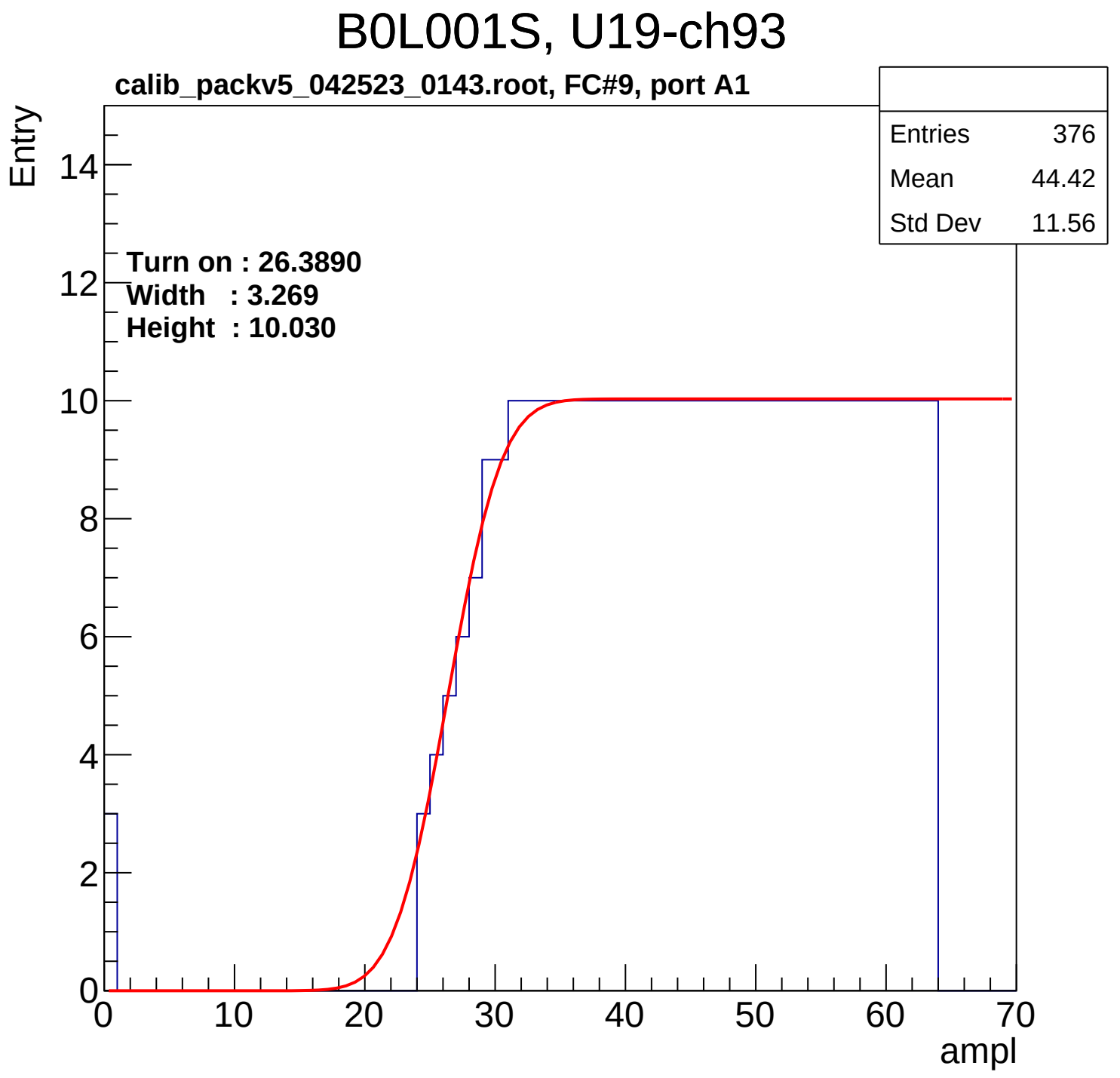
B0L001S, U19-ch93
calib_packv5_042523_0143.root, FC#9, port A1
Entries 376
Mean 44.42
Std Dev 11.56
Turn on : 26.3890
Width : 3.269
Height : 10.030
Entry
ampl
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2
4
6
8
10
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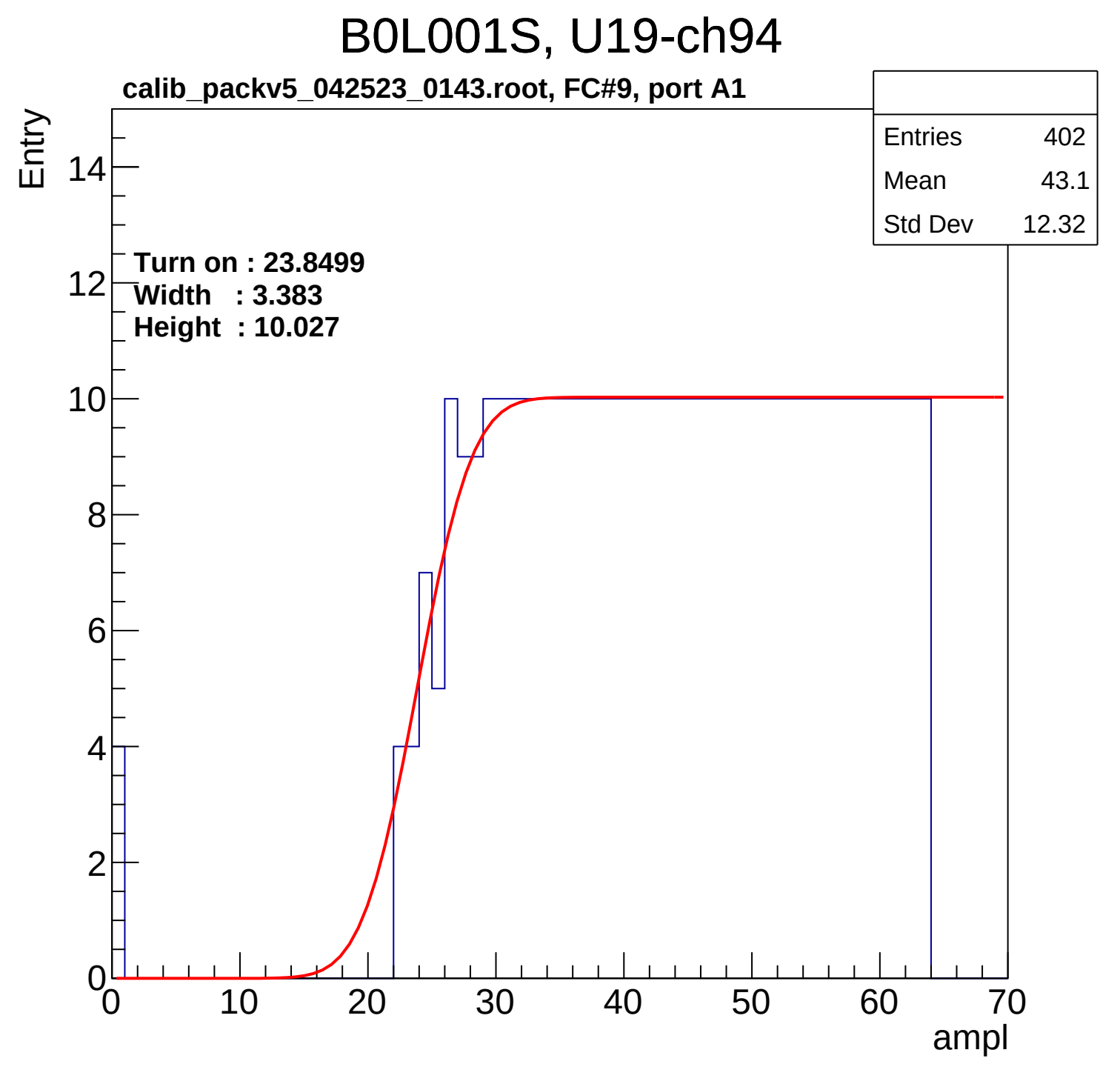
B0L001S, U19-ch94
calib_packv5_042523_0143.root, FC#9, port A1
Entries 402
Mean 43.1
Std Dev 12.32
Turn on : 23.8499
Width : 3.383
Height : 10.027
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
50
60
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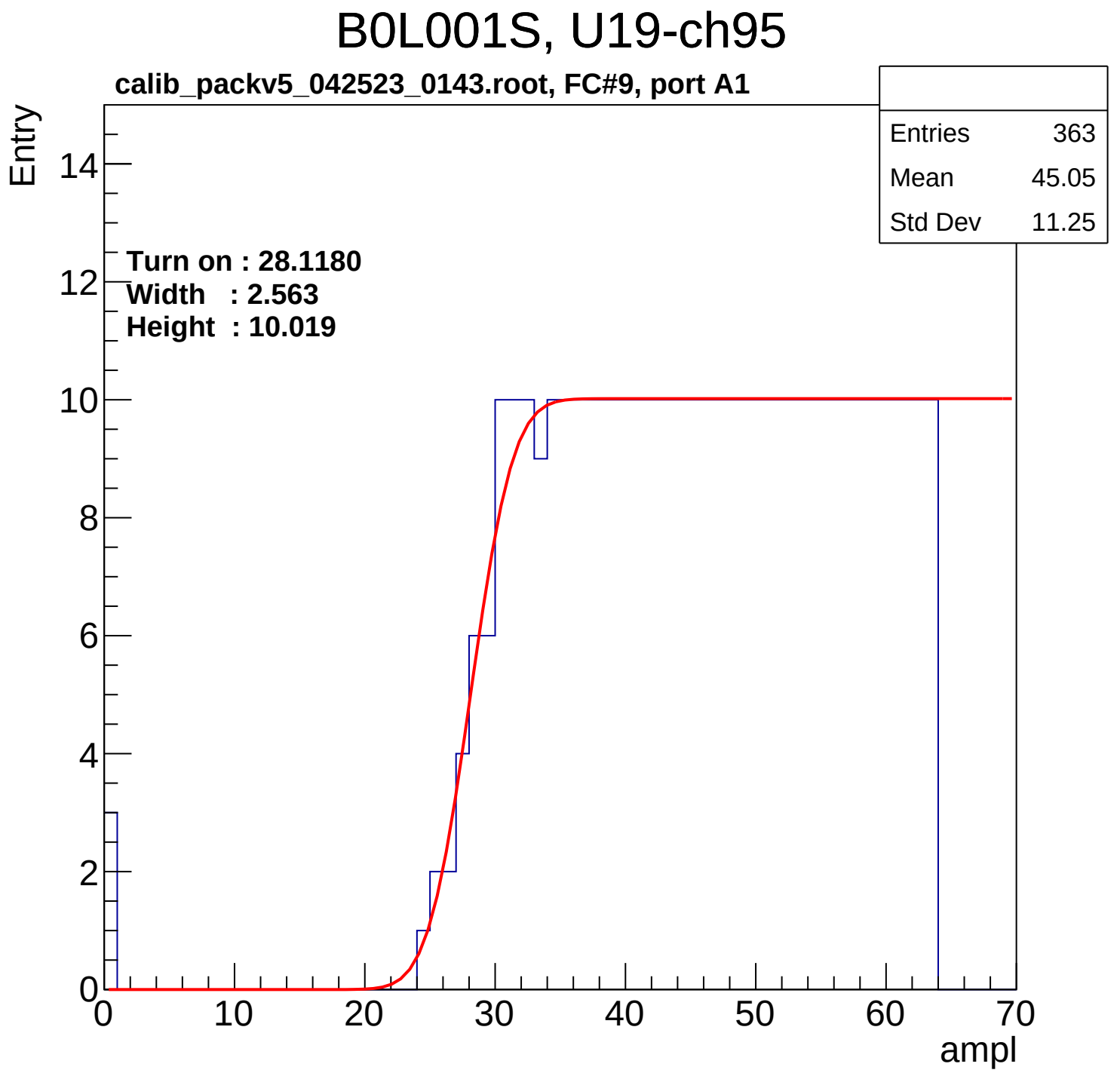
B0L001S, U19-ch95
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 45.05
Std Dev 11.25
Turn on : 28.1180
Width : 2.563
Height : 10.019
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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40
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60
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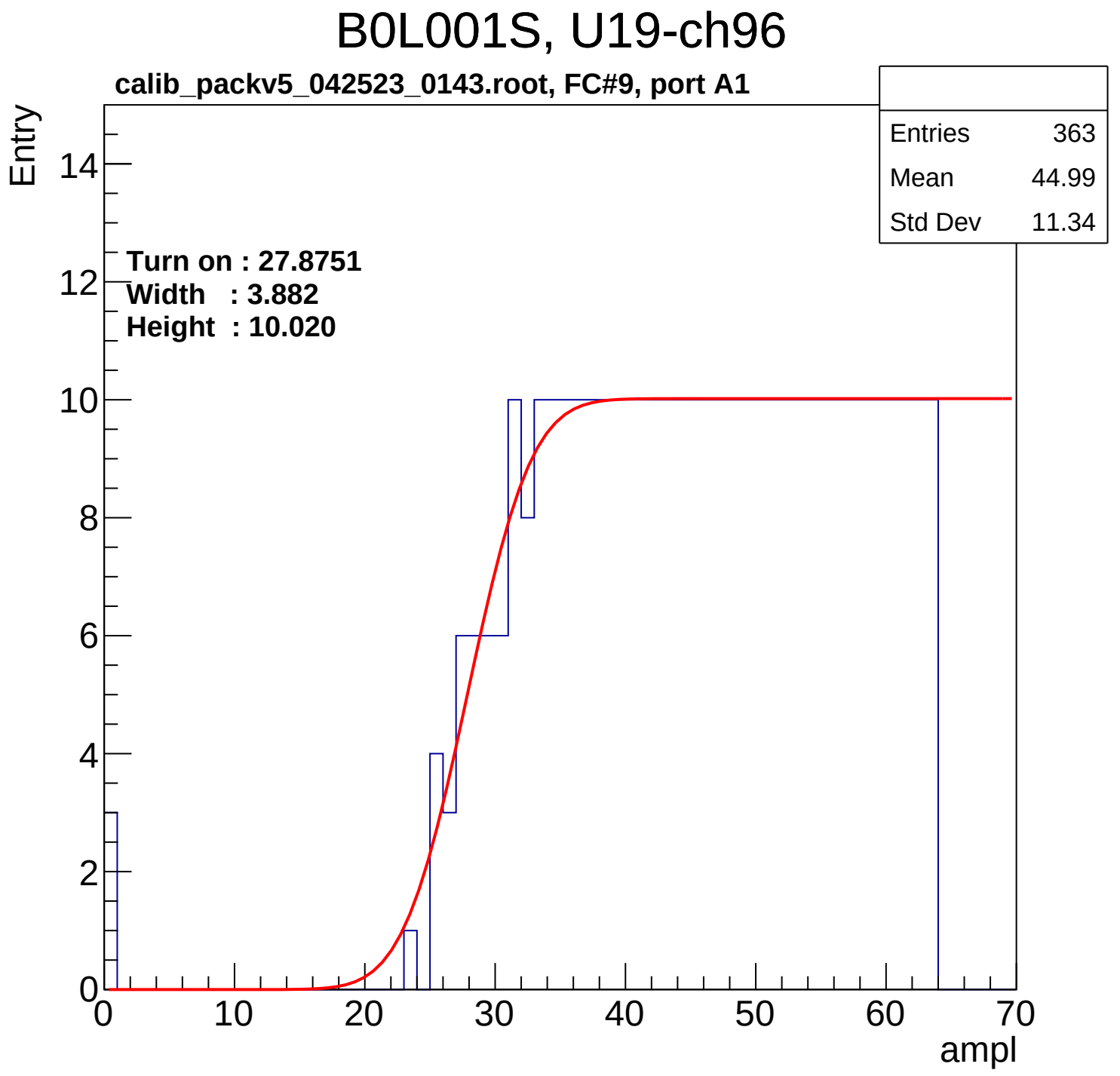
B0L001S, U19-ch96
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 44.99
Std Dev 11.34
Turn on : 27.8751
Width : 3.882
Height : 10.020
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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40
50
60
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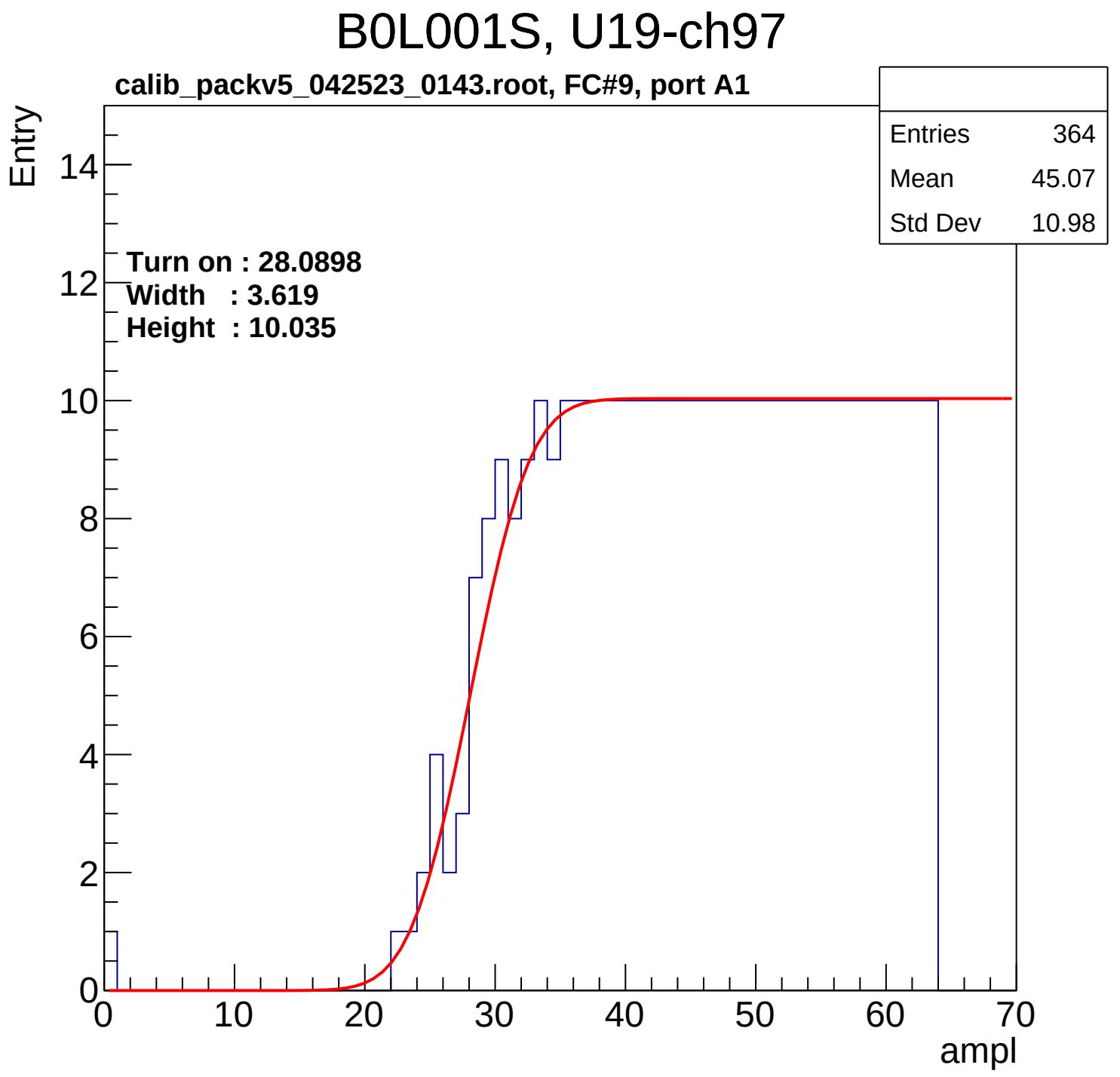
B0L001S, U19-ch97
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 45.07
Std Dev 10.98
Turn on : 28.0898
Width : 3.619
Height : 10.035
Entry
ampl
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2
4
6
8
10
12
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0
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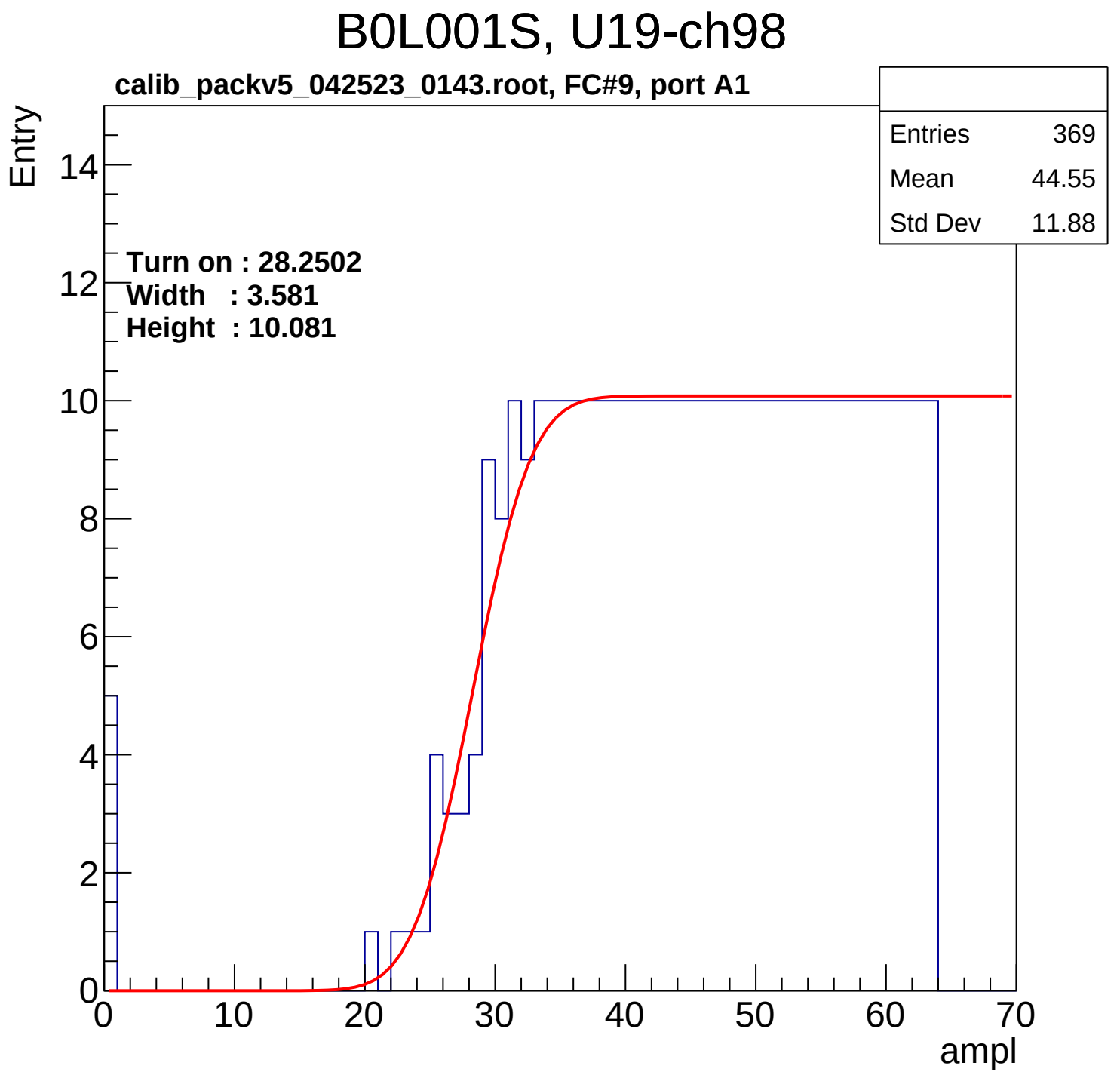
B0L001S, U19-ch98
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.55
Std Dev 11.88
Turn on : 28.2502
Width : 3.581
Height : 10.081
Entry
ampl
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2
4
6
8
10
12
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0
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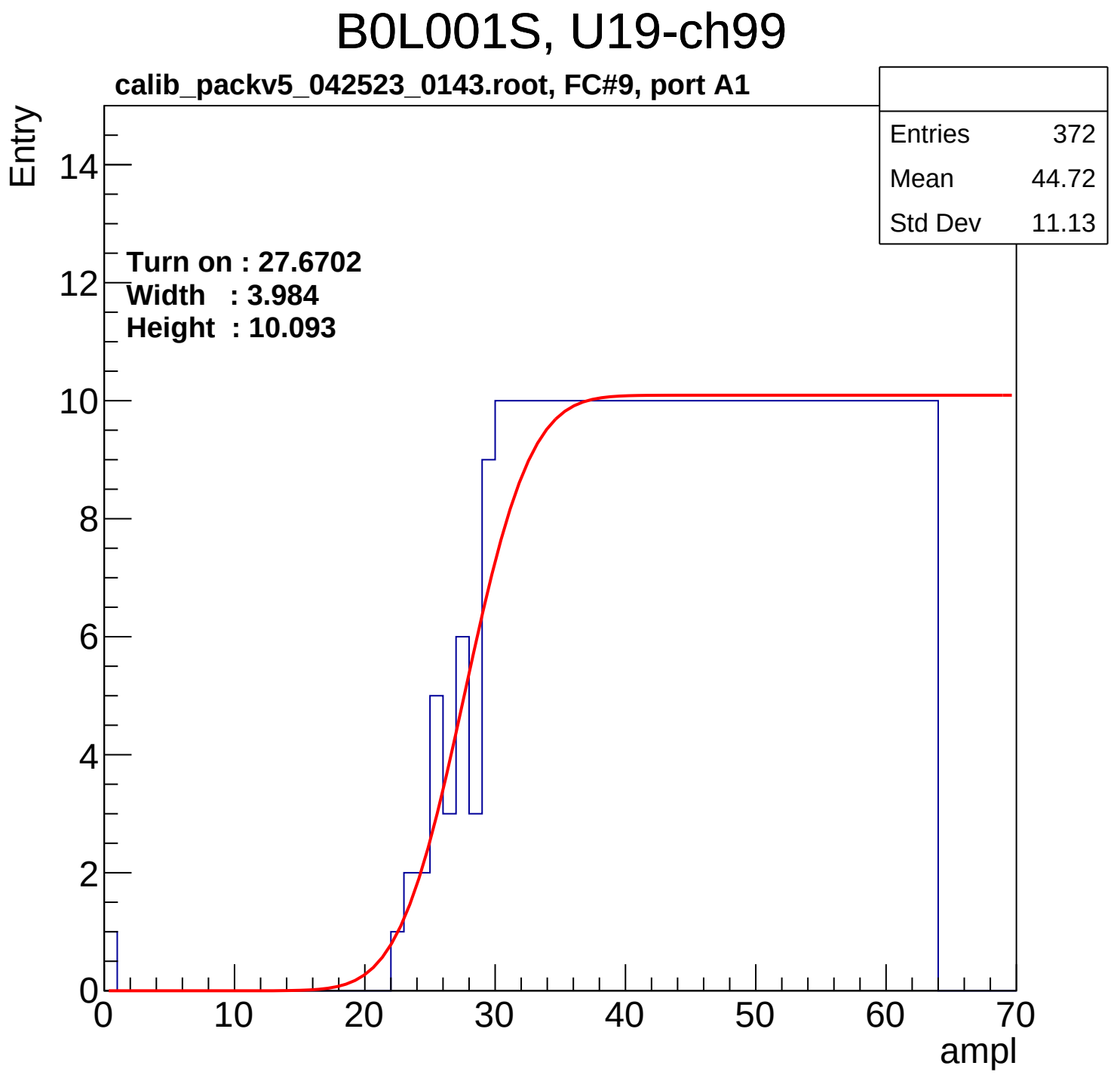
B0L001S, U19-ch99
calib_packv5_042523_0143.root, FC#9, port A1
Entries 372
Mean 44.72
Std Dev 11.13
Turn on : 27.6702
Width : 3.984
Height : 10.093
Entry
ampl
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4
6
8
10
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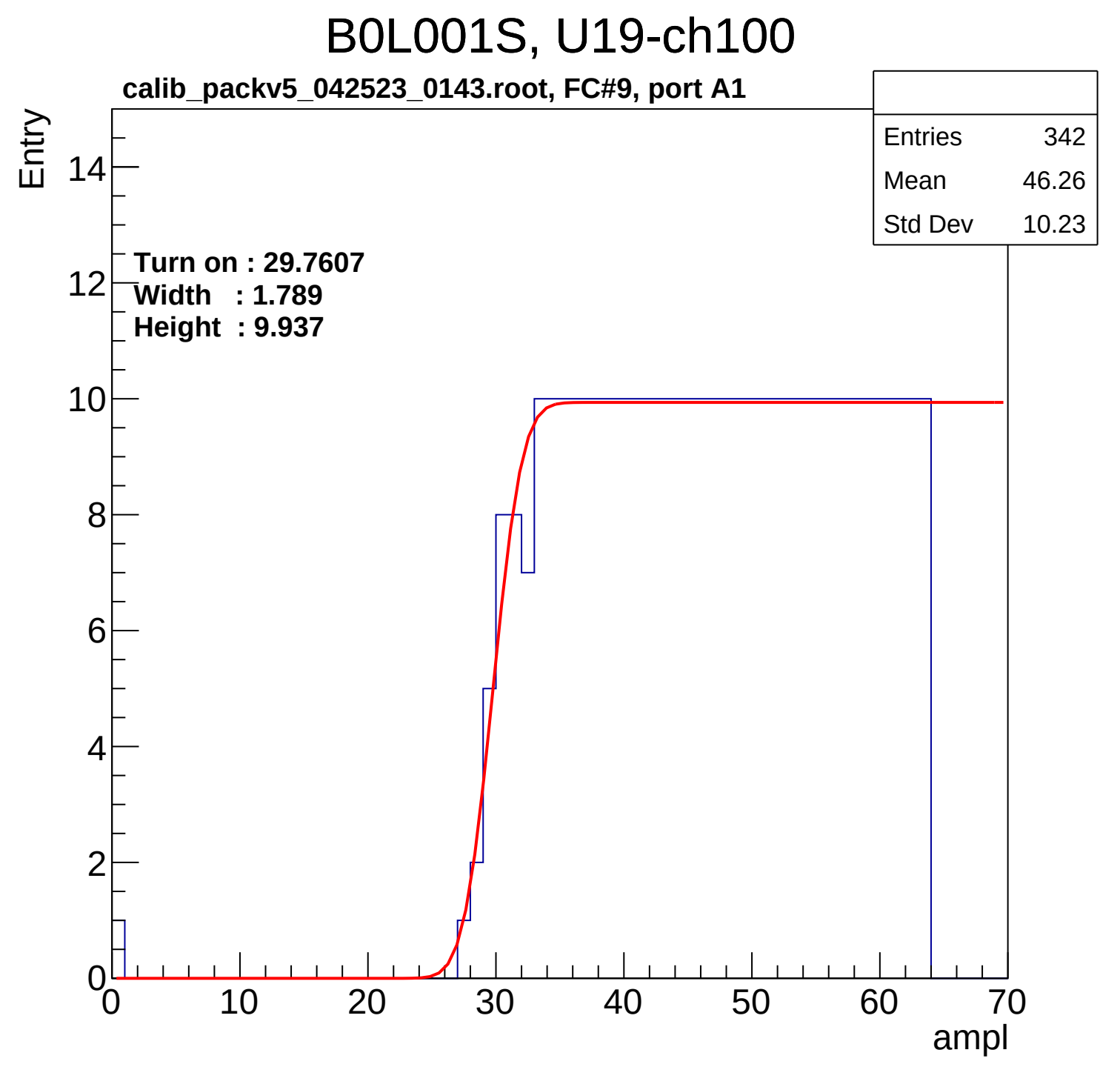
B0L001S, U19-ch100
calib_packv5_042523_0143.root, FC#9, port A1
Entries 342
Mean 46.26
Std Dev 10.23
Turn on : 29.7607
Width : 1.789
Height : 9.937
Entry
ampl
0
2
4
6
8
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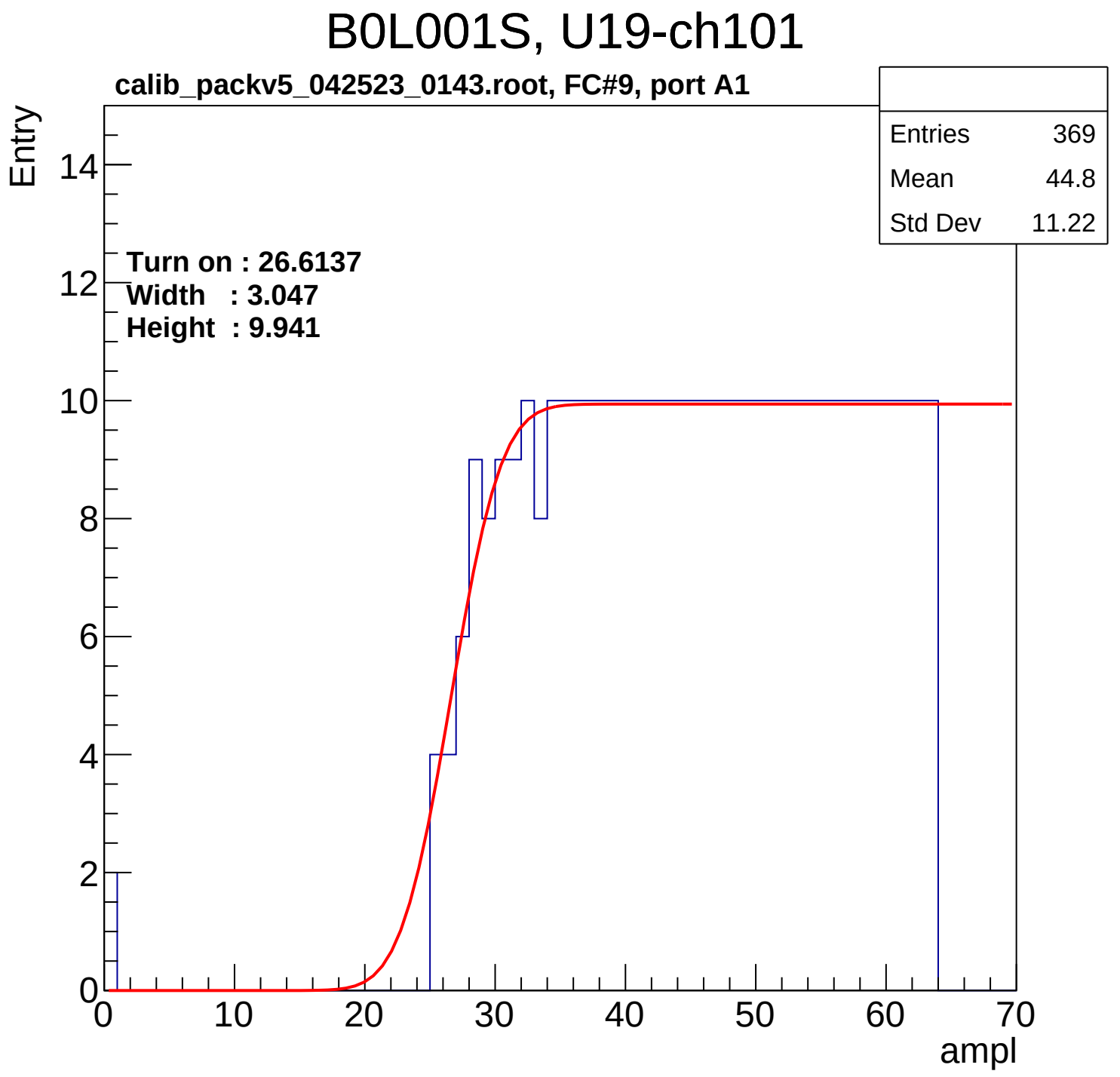
B0L001S, U19-ch101
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.8
Std Dev 11.22
Turn on : 26.6137
Width : 3.047
Height : 9.941
Entry
ampl
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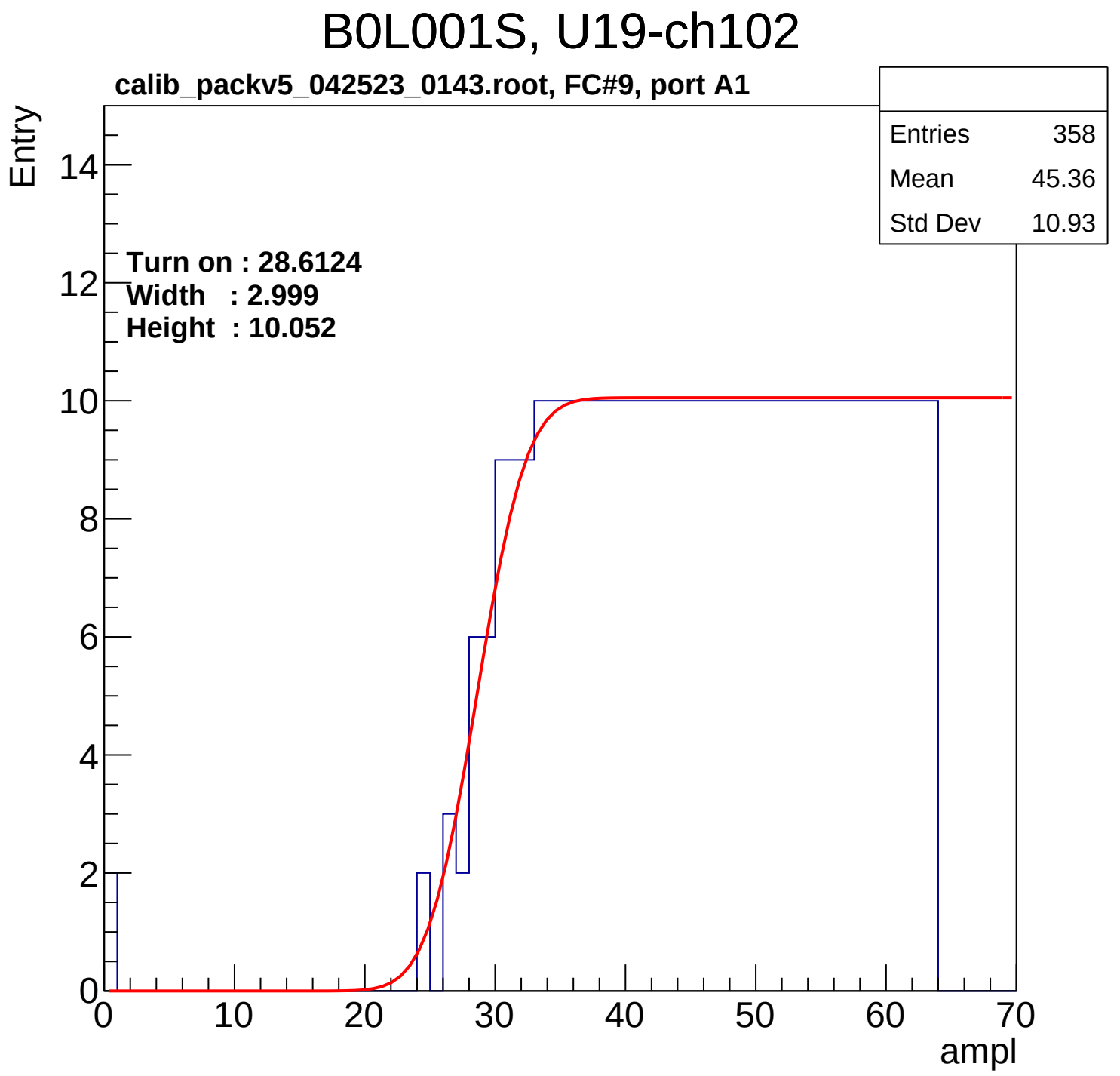
B0L001S, U19-ch102
calib_packv5_042523_0143.root, FC#9, port A1
Entries 358
Mean 45.36
Std Dev 10.93
Turn on : 28.6124
Width : 2.999
Height : 10.052
Entry
ampl
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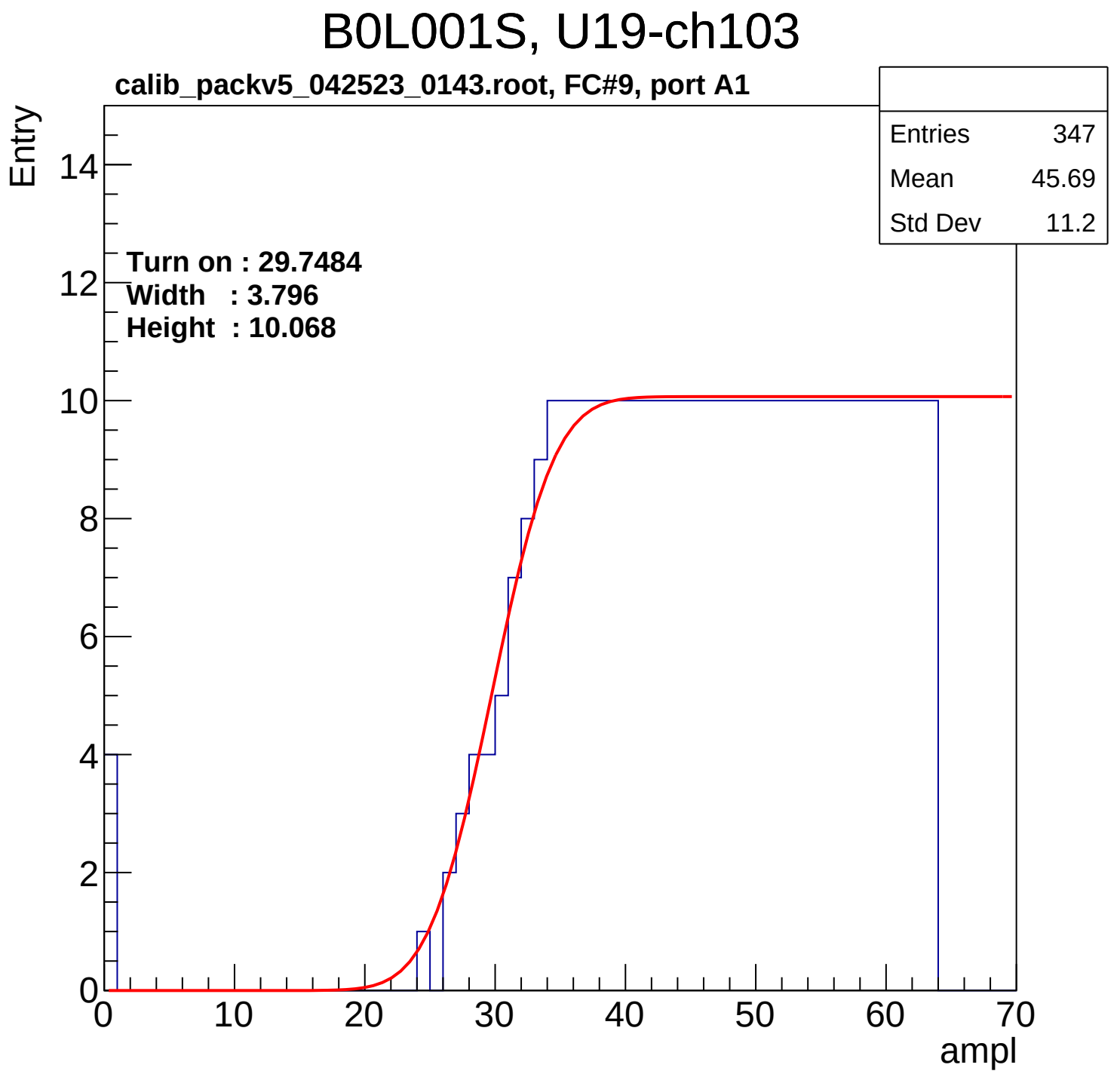
B0L001S, U19-ch103
calib_packv5_042523_0143.root, FC#9, port A1
Entries 347
Mean 45.69
Std Dev 11.2
Turn on : 29.7484
Width : 3.796
Height : 10.068
Entry
ampl
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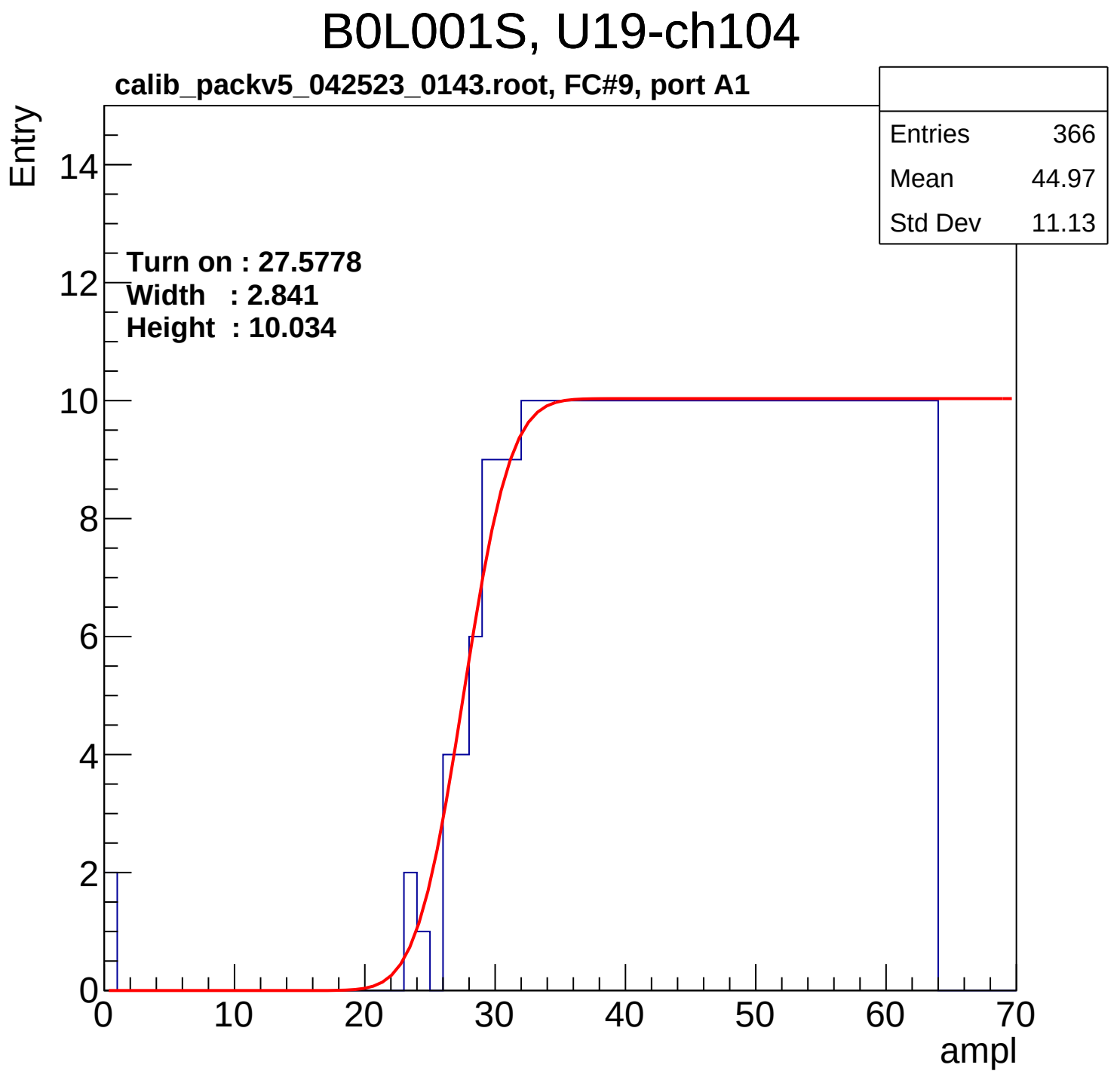
B0L001S, U19-ch104
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.97
Std Dev 11.13
Turn on : 27.5778
Width : 2.841
Height : 10.034
Entry
ampl
0
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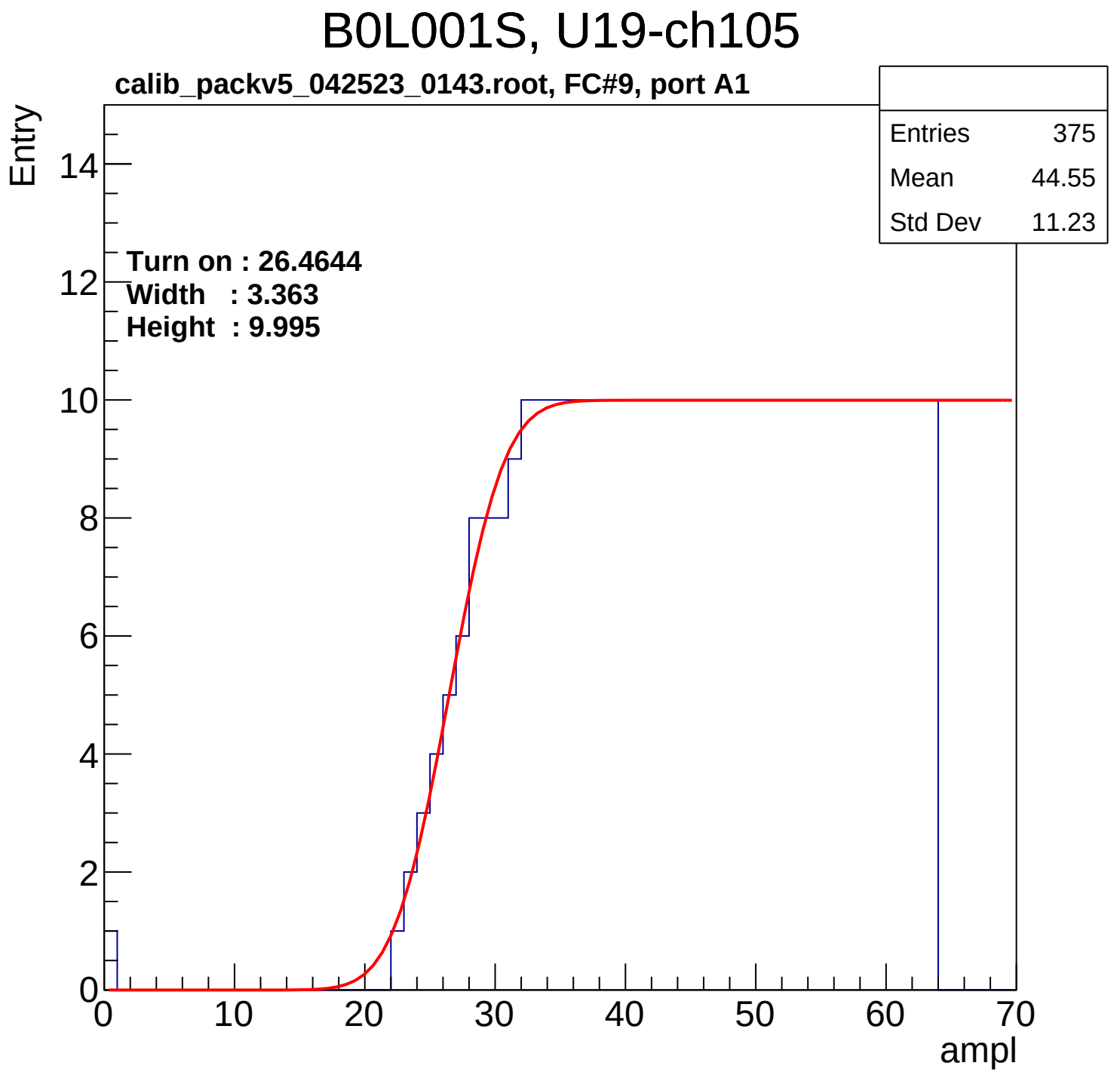
B0L001S, U19-ch105
calib_packv5_042523_0143.root, FC#9, port A1
Entries 375
Mean 44.55
Std Dev 11.23
Turn on : 26.4644
Width : 3.363
Height : 9.995
Entry
ampl
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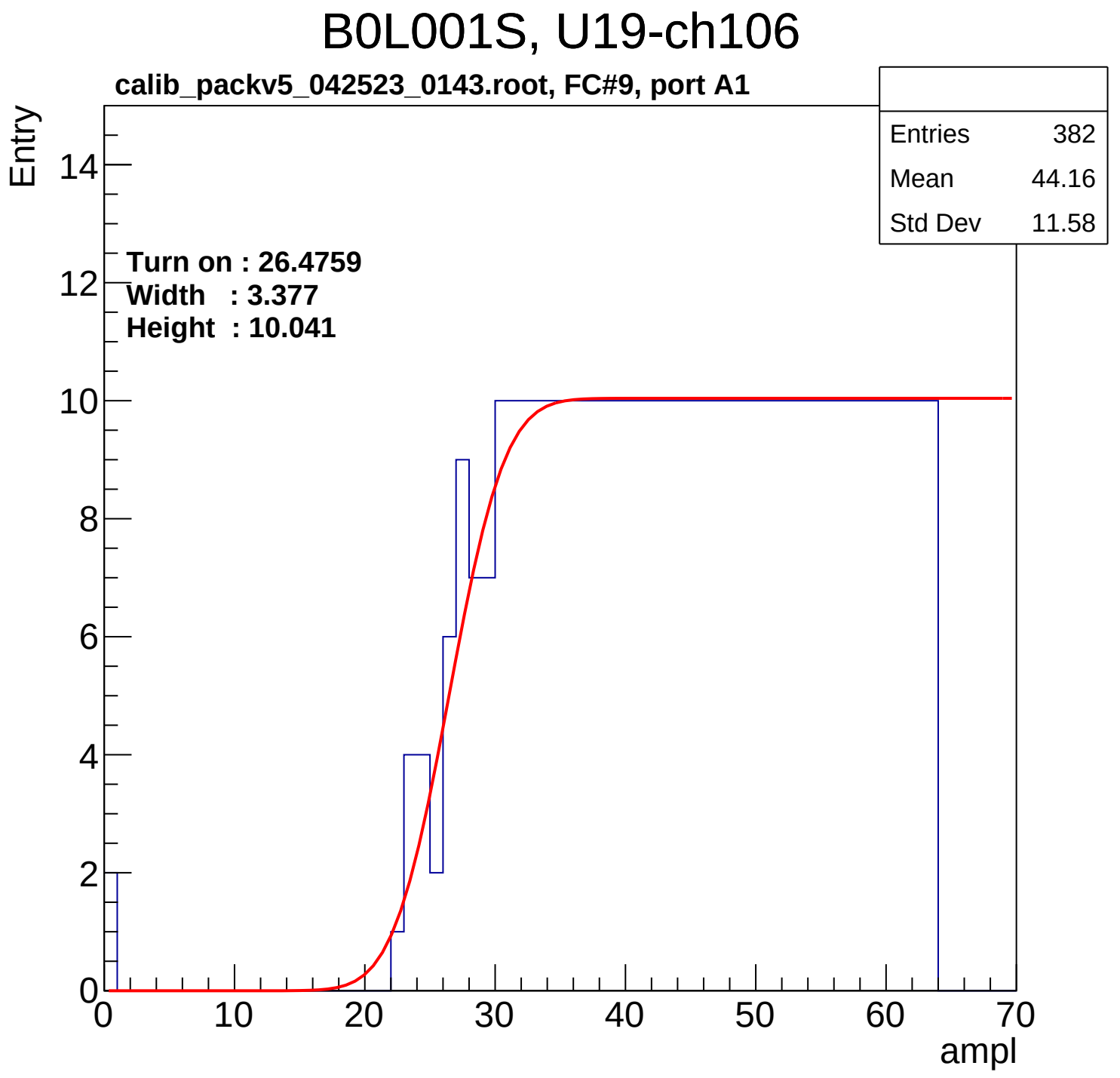
B0L001S, U19-ch106
calib_packv5_042523_0143.root, FC#9, port A1
Entries 382
Mean 44.16
Std Dev 11.58
Turn on : 26.4759
Width : 3.377
Height : 10.041
Entry
ampl
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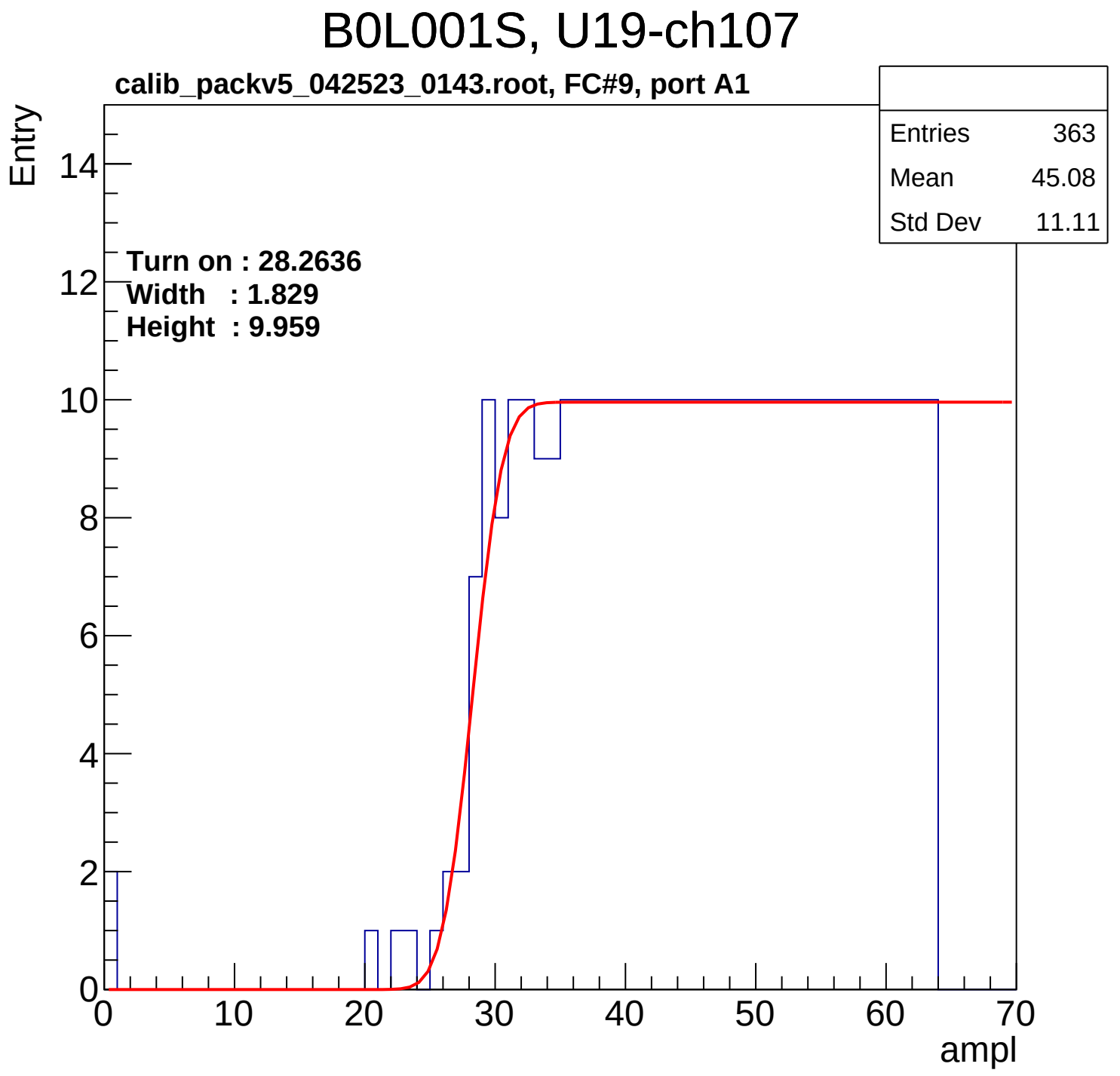
B0L001S, U19-ch107
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 45.08
Std Dev 11.11
Turn on : 28.2636
Width : 1.829
Height : 9.959
Entry
ampl
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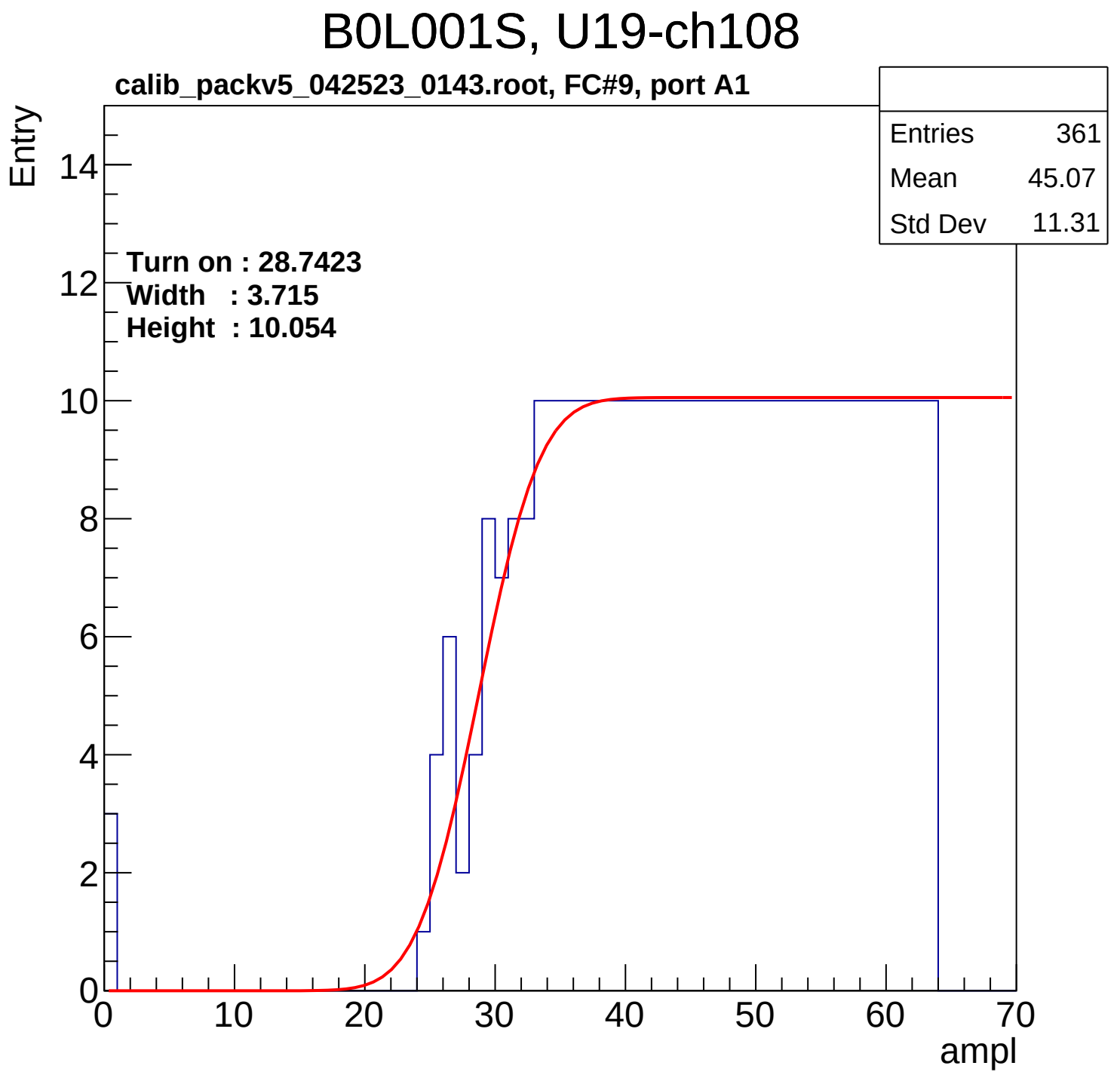
B0L001S, U19-ch108
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 45.07
Std Dev 11.31
Turn on : 28.7423
Width : 3.715
Height : 10.054
Entry
ampl
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4
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8
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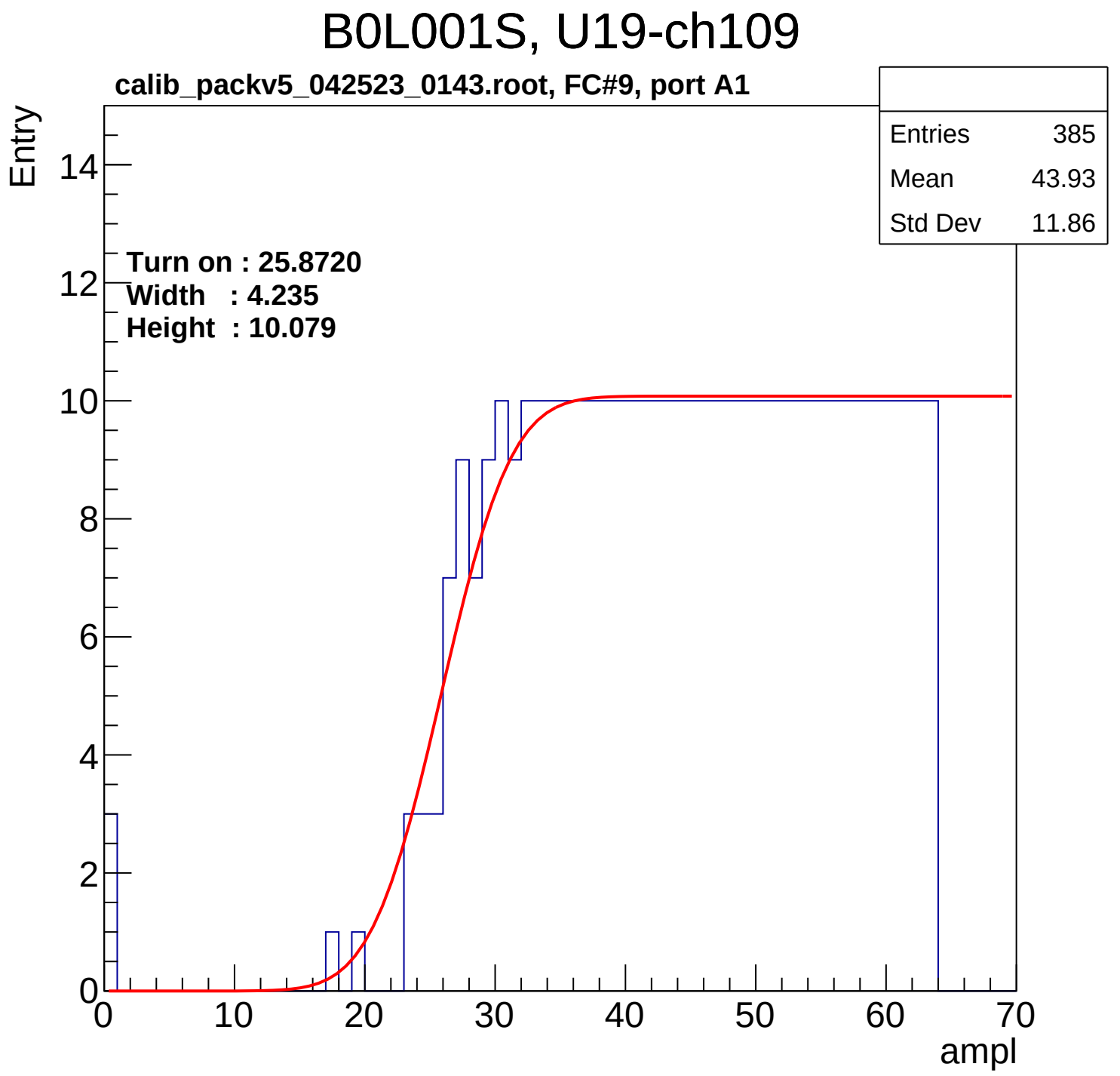
B0L001S, U19-ch109
calib_packv5_042523_0143.root, FC#9, port A1
Entries 385
Mean 43.93
Std Dev 11.86
Turn on : 25.8720
Width : 4.235
Height : 10.079
Entry
ampl
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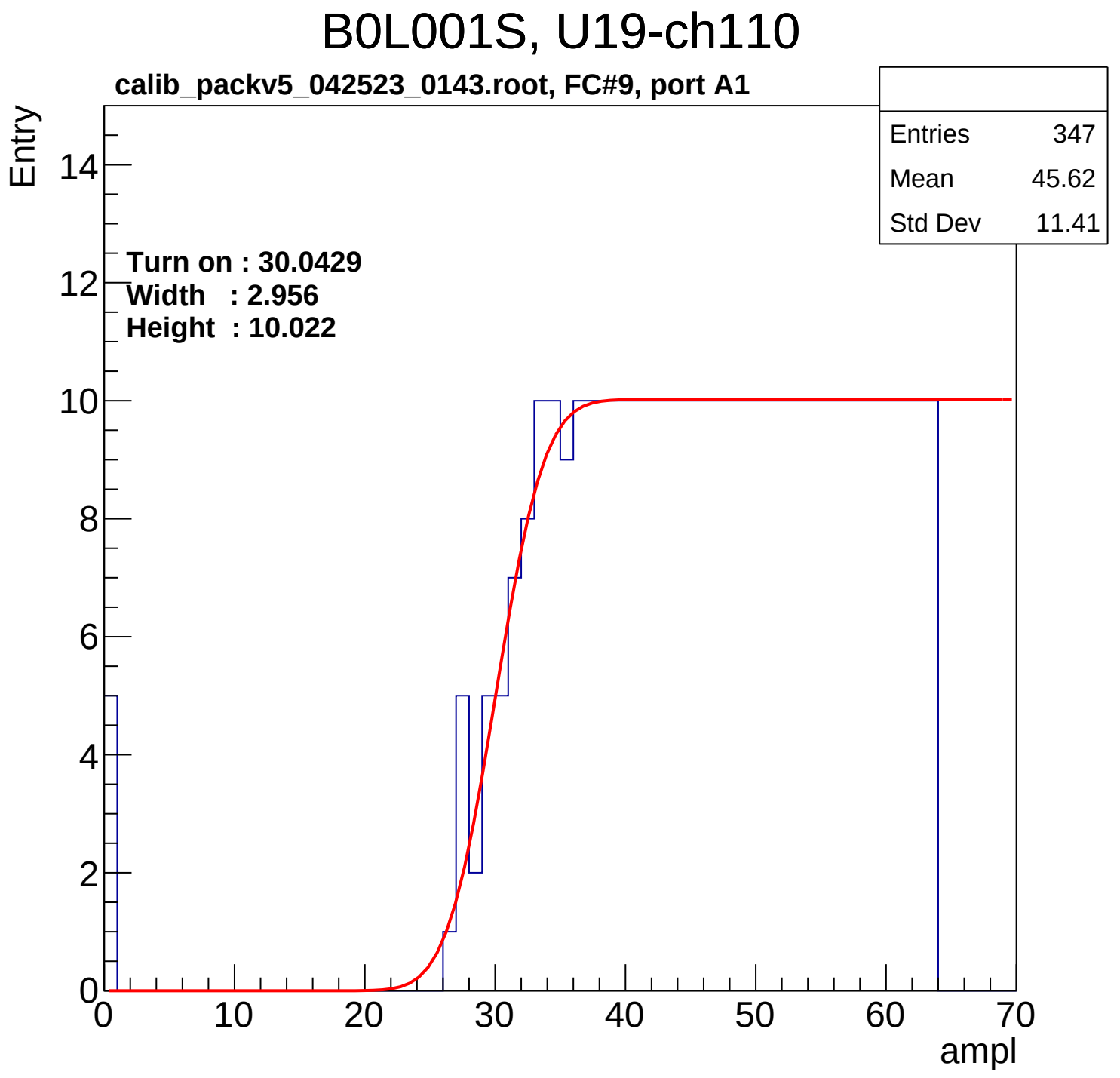
B0L001S, U19-ch110
calib_packv5_042523_0143.root, FC#9, port A1
Entries 347
Mean 45.62
Std Dev 11.41
Turn on : 30.0429
Width : 2.956
Height : 10.022
Entry
ampl
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6
8
10
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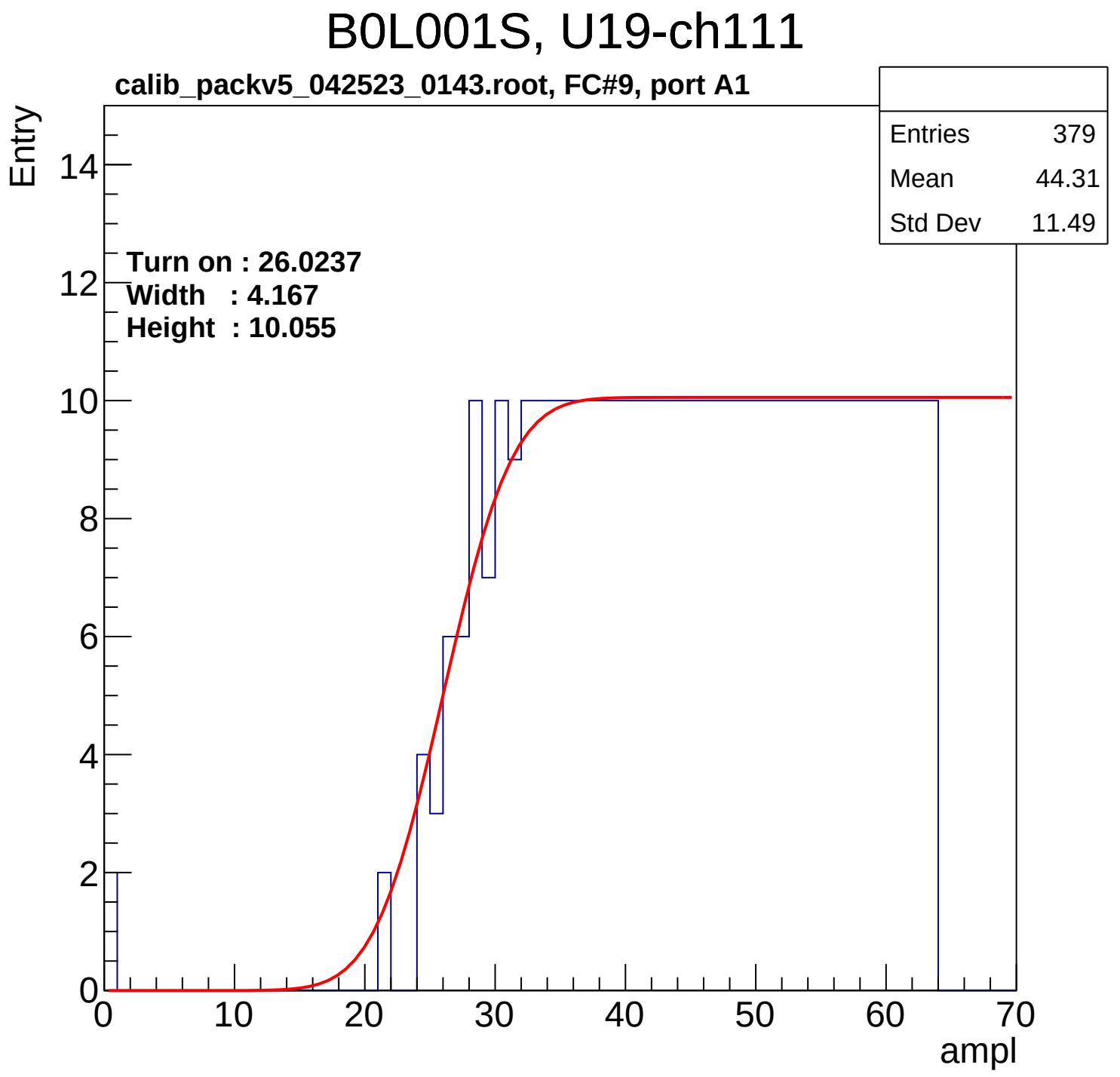
B0L001S, U19-ch111
calib_packv5_042523_0143.root, FC#9, port A1
Entries 379
Mean 44.31
Std Dev 11.49
Turn on : 26.0237
Width : 4.167
Height : 10.055
Entry
ampl
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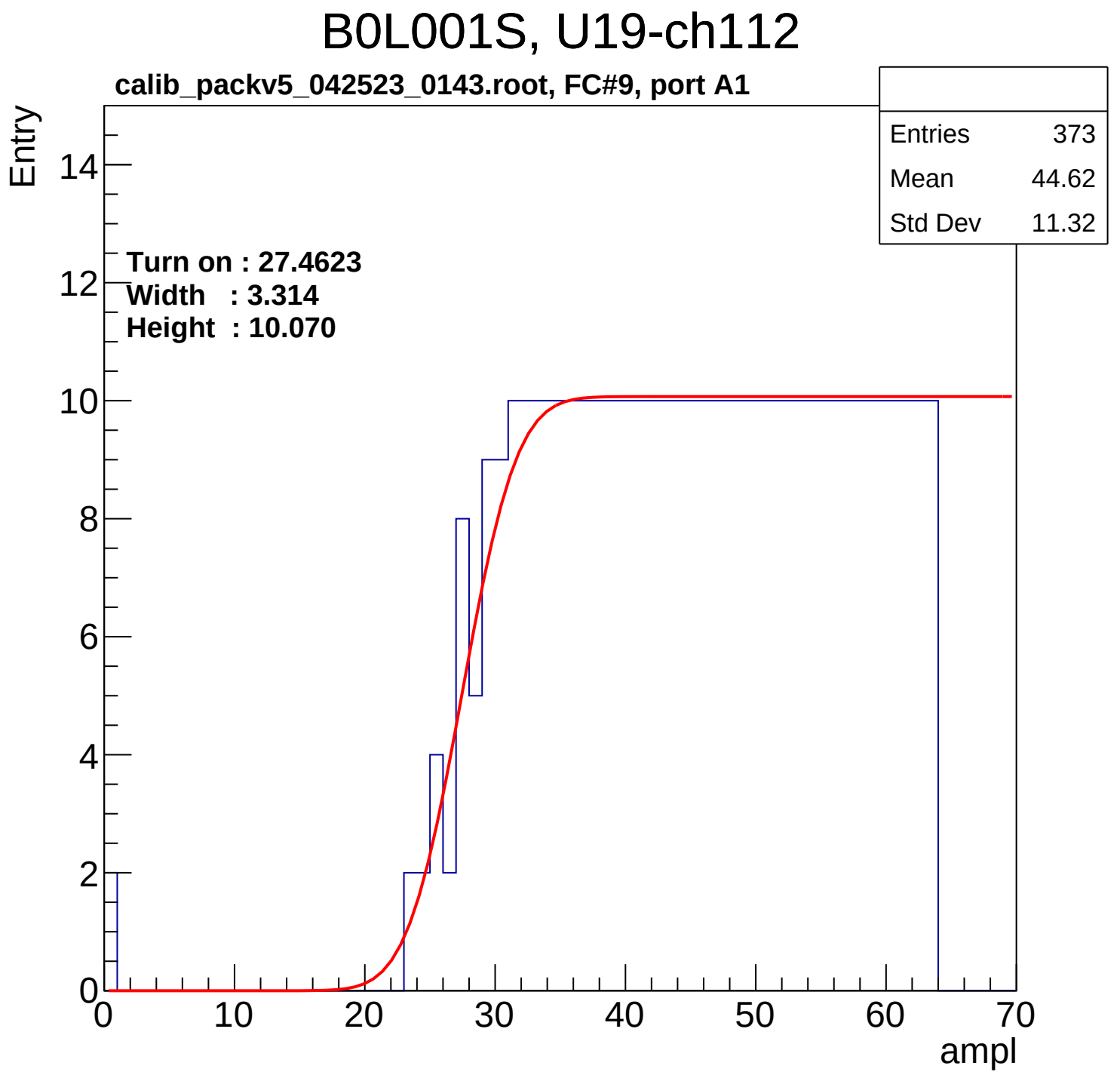
B0L001S, U19-ch112
calib_packv5_042523_0143.root, FC#9, port A1
Entries 373
Mean 44.62
Std Dev 11.32
Turn on : 27.4623
Width : 3.314
Height : 10.070
Entry
ampl
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2
4
6
8
10
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0
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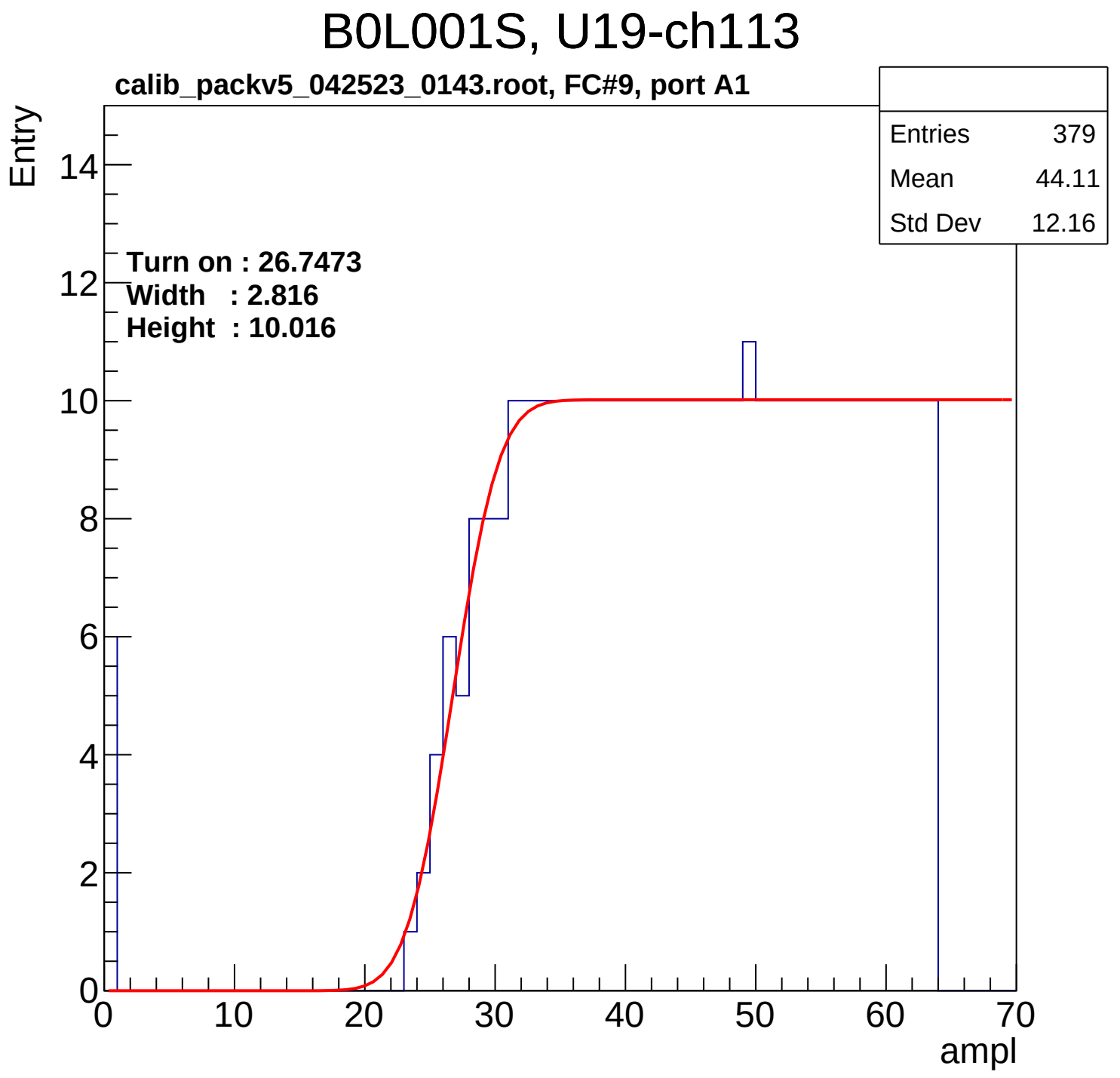
B0L001S, U19-ch113
calib_packv5_042523_0143.root, FC#9, port A1
Entries 379
Mean 44.11
Std Dev 12.16
Turn on : 26.7473
Width : 2.816
Height : 10.016
Entry
ampl
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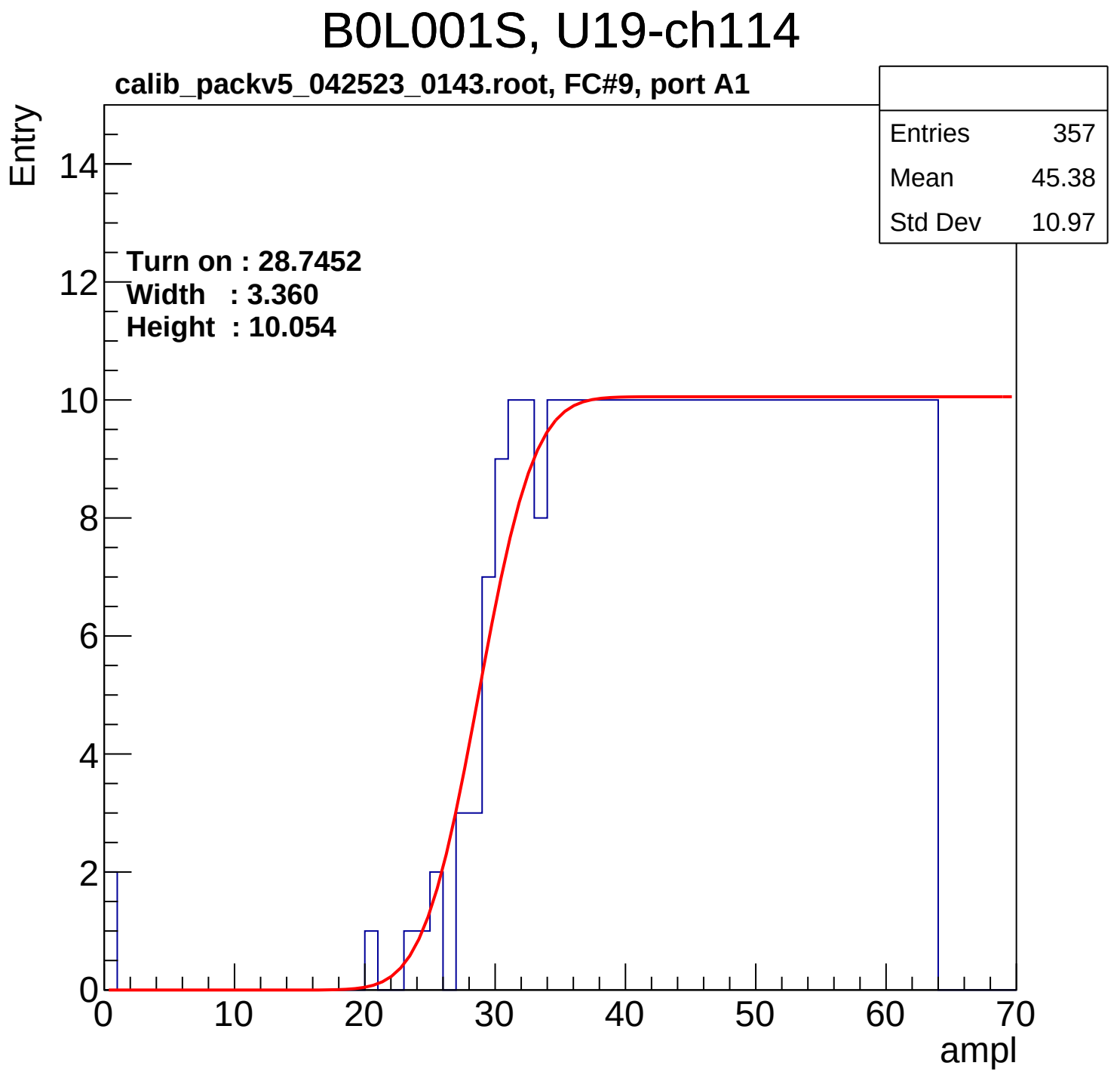
B0L001S, U19-ch114
calib_packv5_042523_0143.root, FC#9, port A1
Entries 357
Mean 45.38
Std Dev 10.97
Turn on : 28.7452
Width : 3.360
Height : 10.054
Entry
ampl
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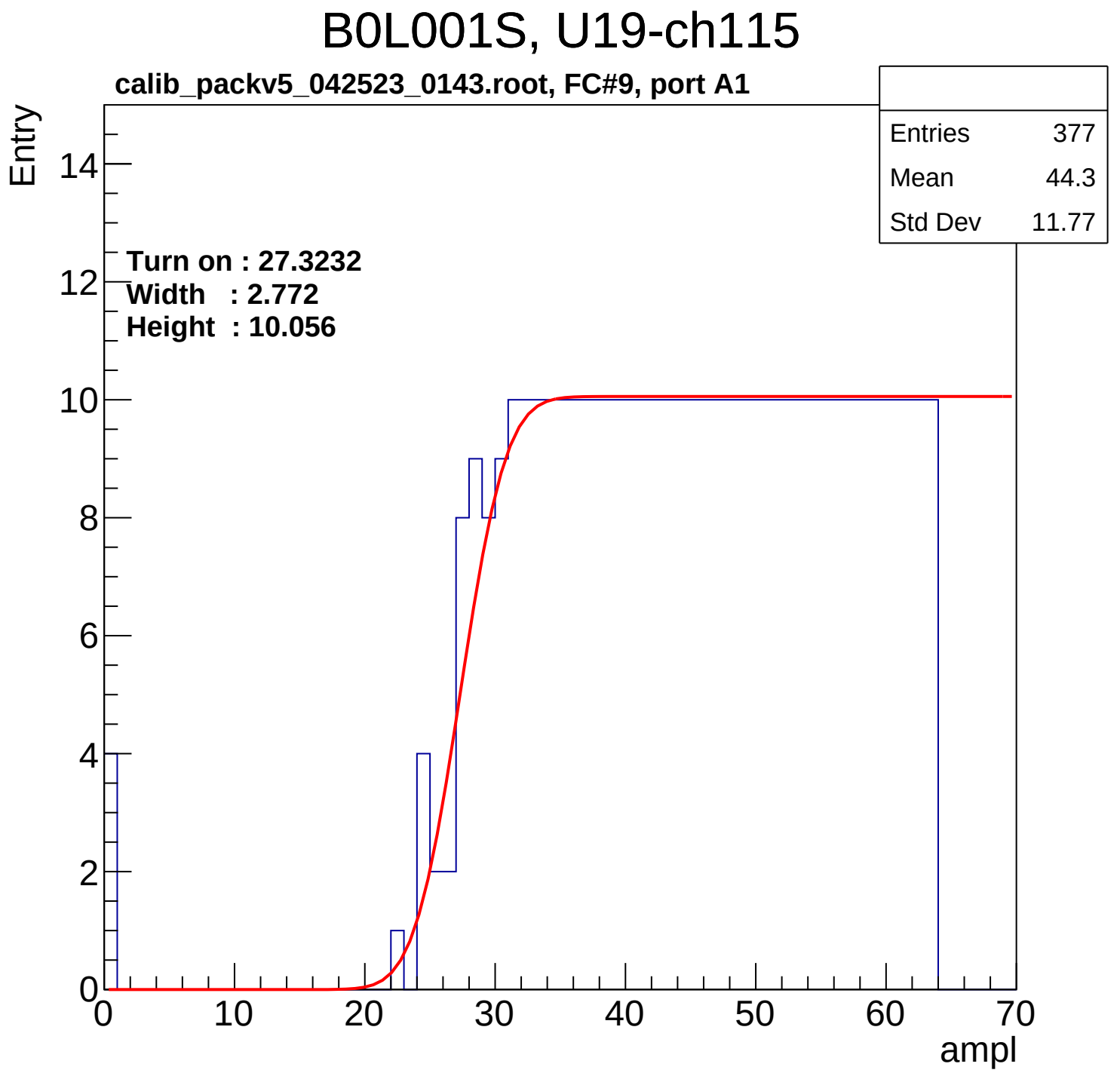
B0L001S, U19-ch115
calib_packv5_042523_0143.root, FC#9, port A1
Entries 377
Mean 44.3
Std Dev 11.77
Turn on : 27.3232
Width : 2.772
Height : 10.056
Entry
ampl
0
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4
6
8
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12
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10
20
30
40
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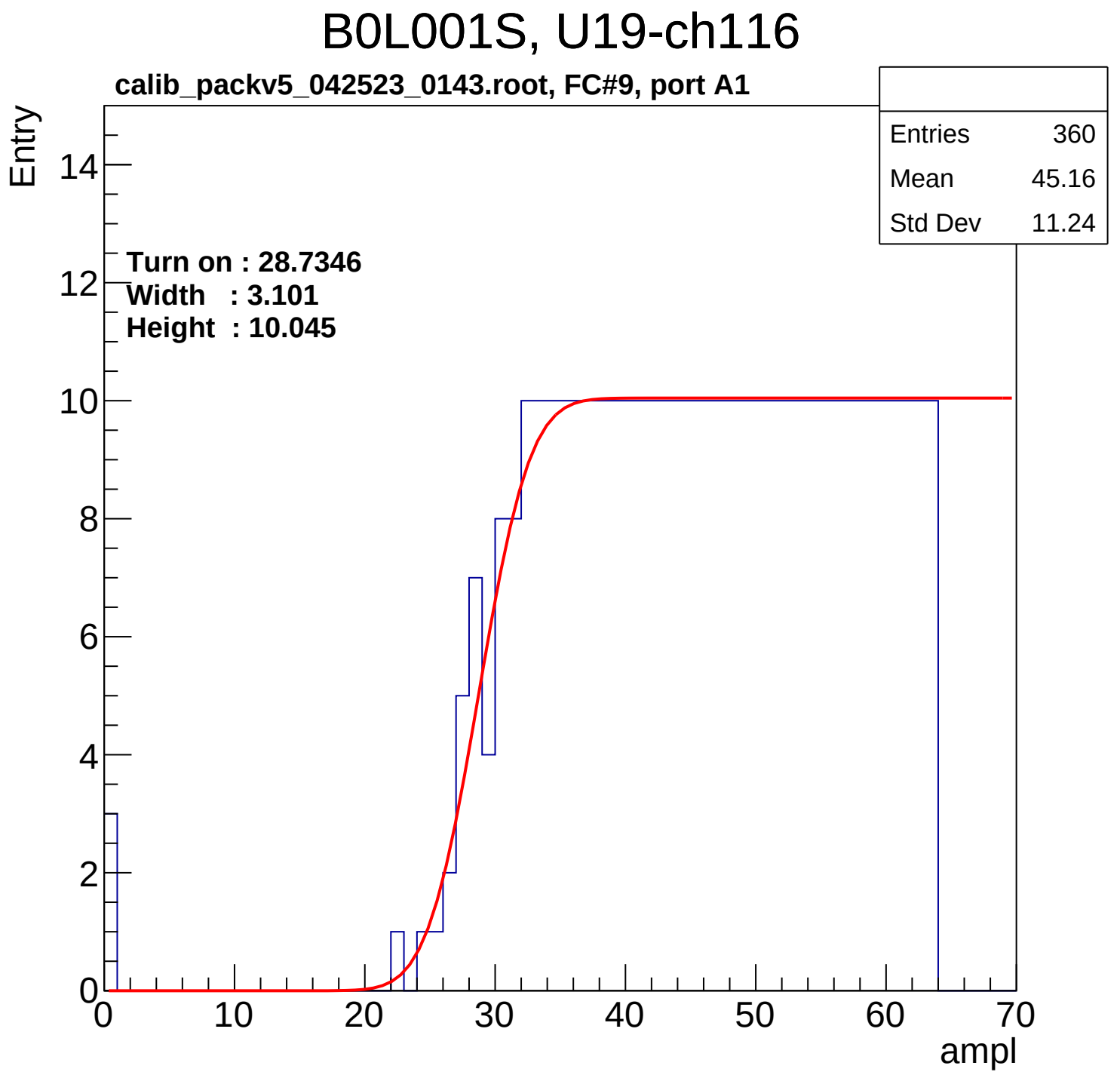
B0L001S, U19-ch116
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 45.16
Std Dev 11.24
Turn on : 28.7346
Width : 3.101
Height : 10.045
Entry
ampl
0
2
4
6
8
10
12
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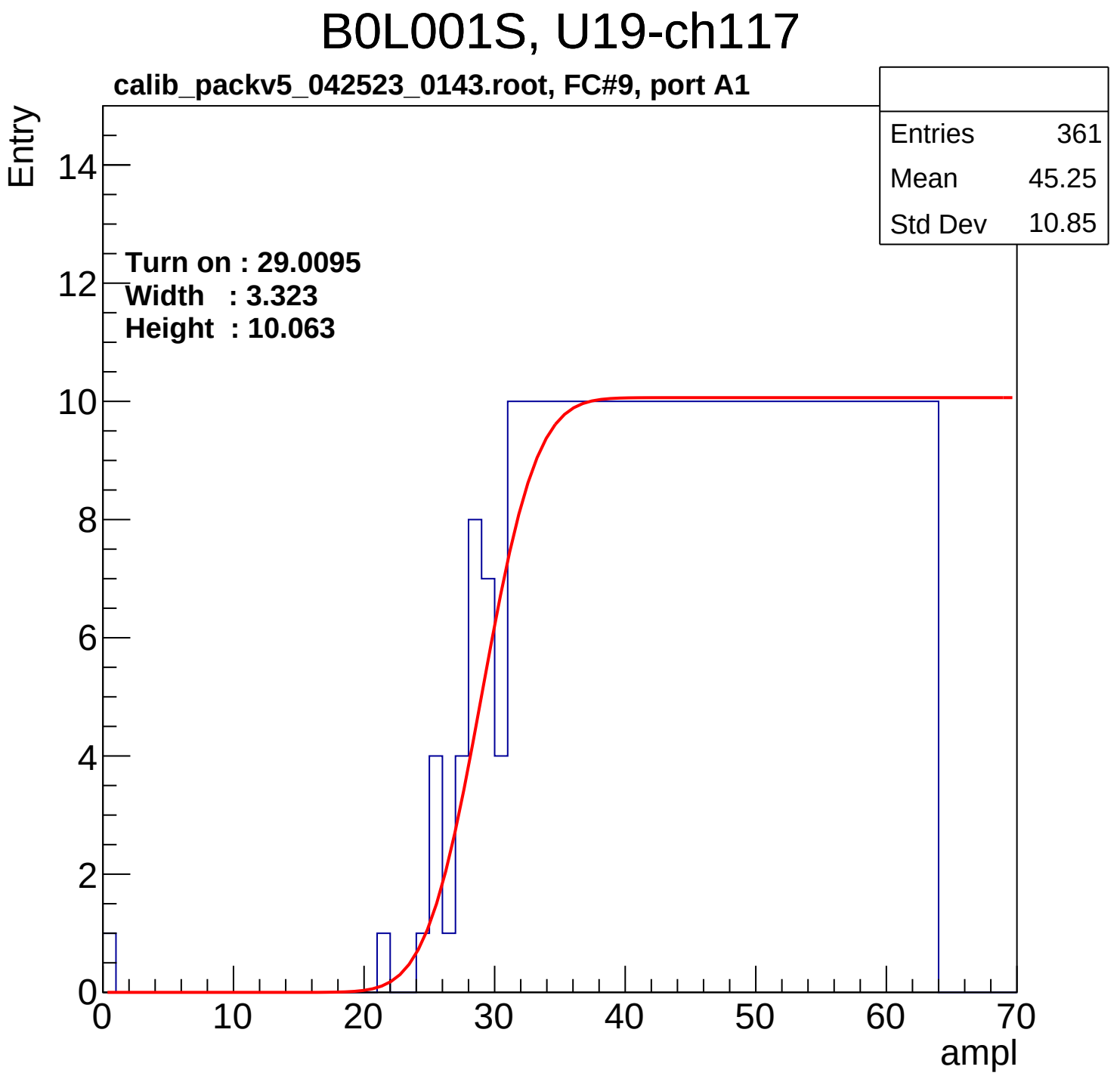
B0L001S, U19-ch117
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 45.25
Std Dev 10.85
Turn on : 29.0095
Width : 3.323
Height : 10.063
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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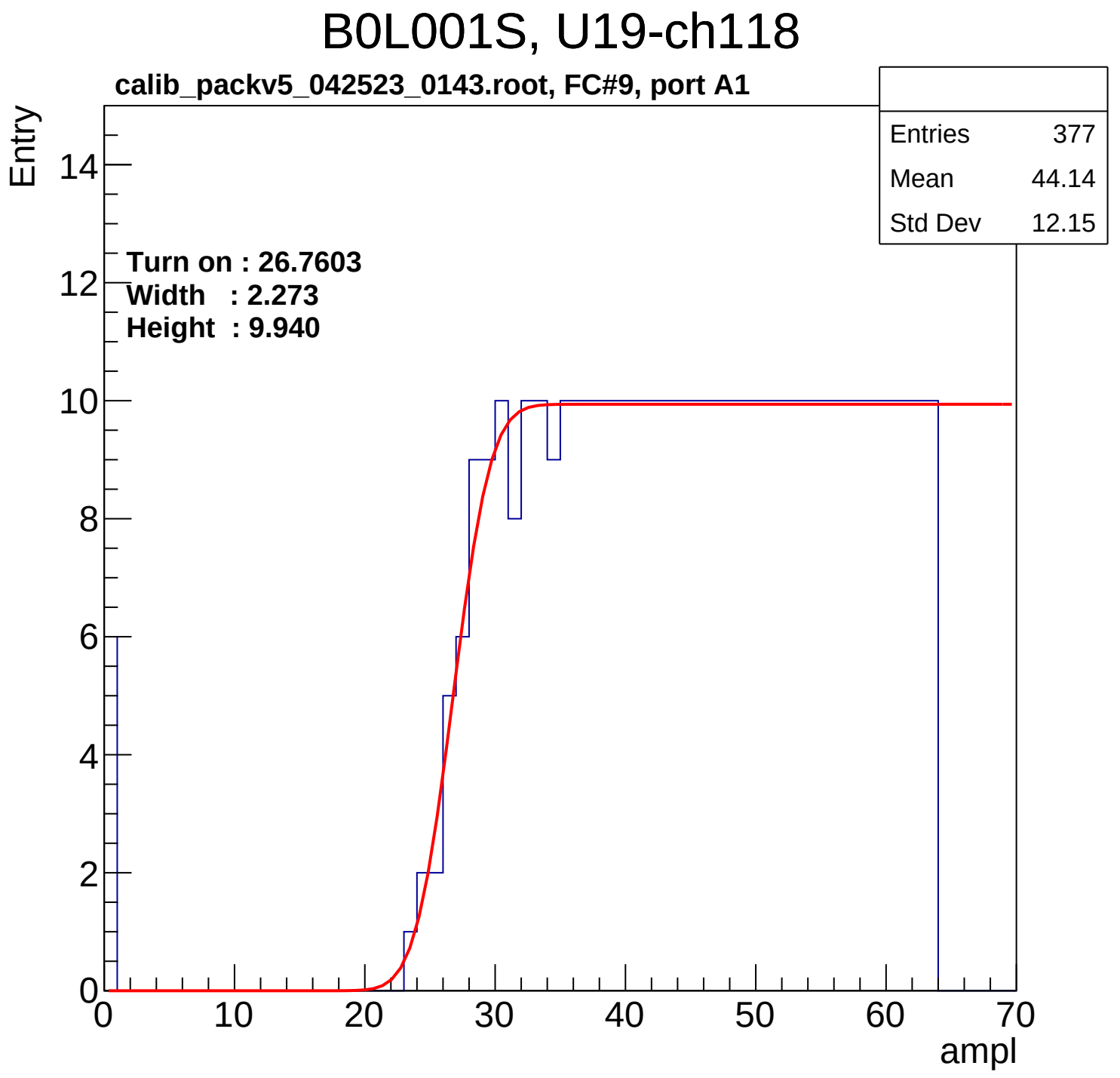
B0L001S, U19-ch118
calib_packv5_042523_0143.root, FC#9, port A1
Entries 377
Mean 44.14
Std Dev 12.15
Turn on : 26.7603
Width : 2.273
Height : 9.940
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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60
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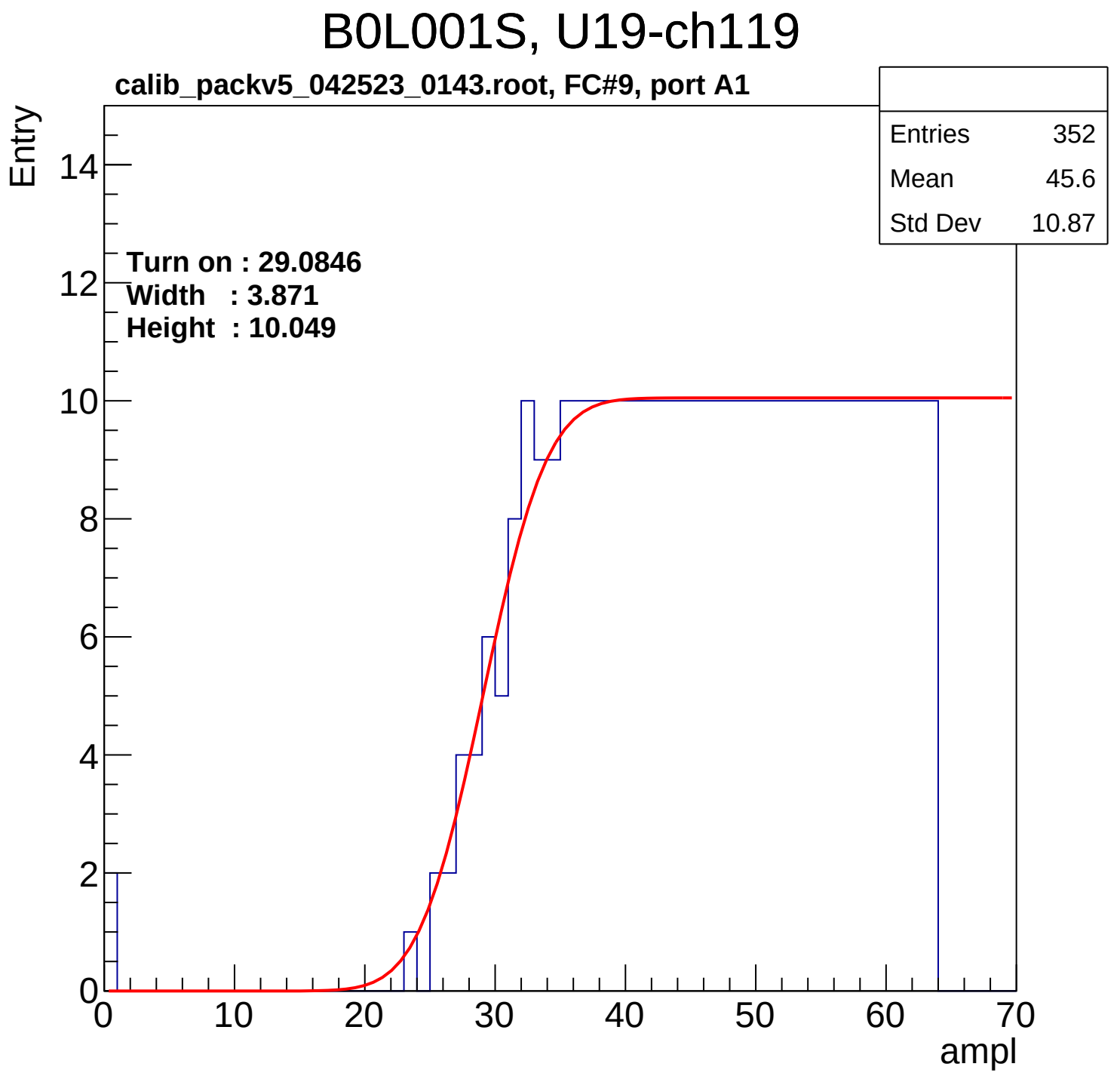
B0L001S, U19-ch119
calib_packv5_042523_0143.root, FC#9, port A1
Entries 352
Mean 45.6
Std Dev 10.87
Turn on : 29.0846
Width : 3.871
Height : 10.049
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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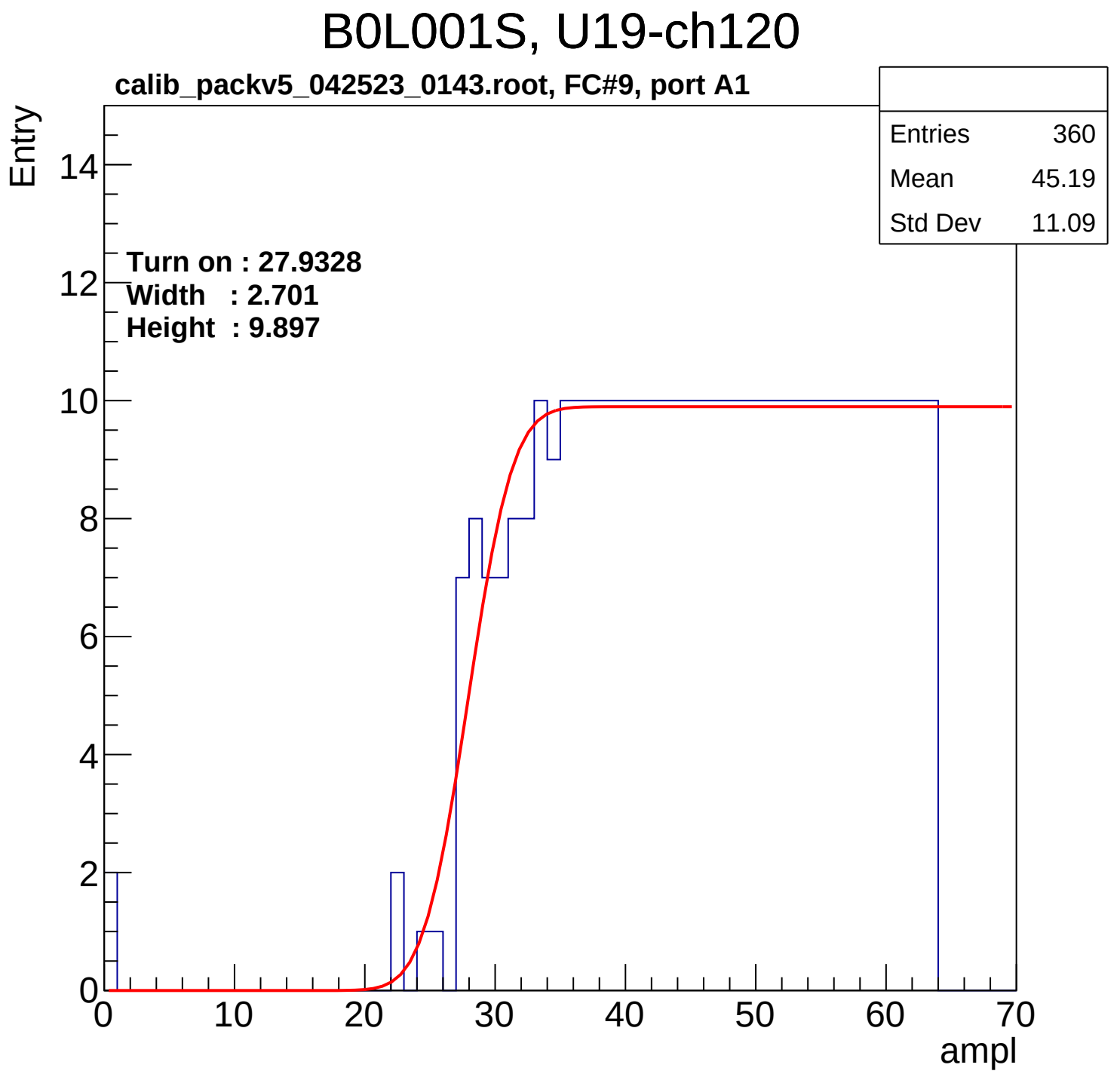
B0L001S, U19-ch120
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 45.19
Std Dev 11.09
Turn on : 27.9328
Width : 2.701
Height : 9.897
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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60
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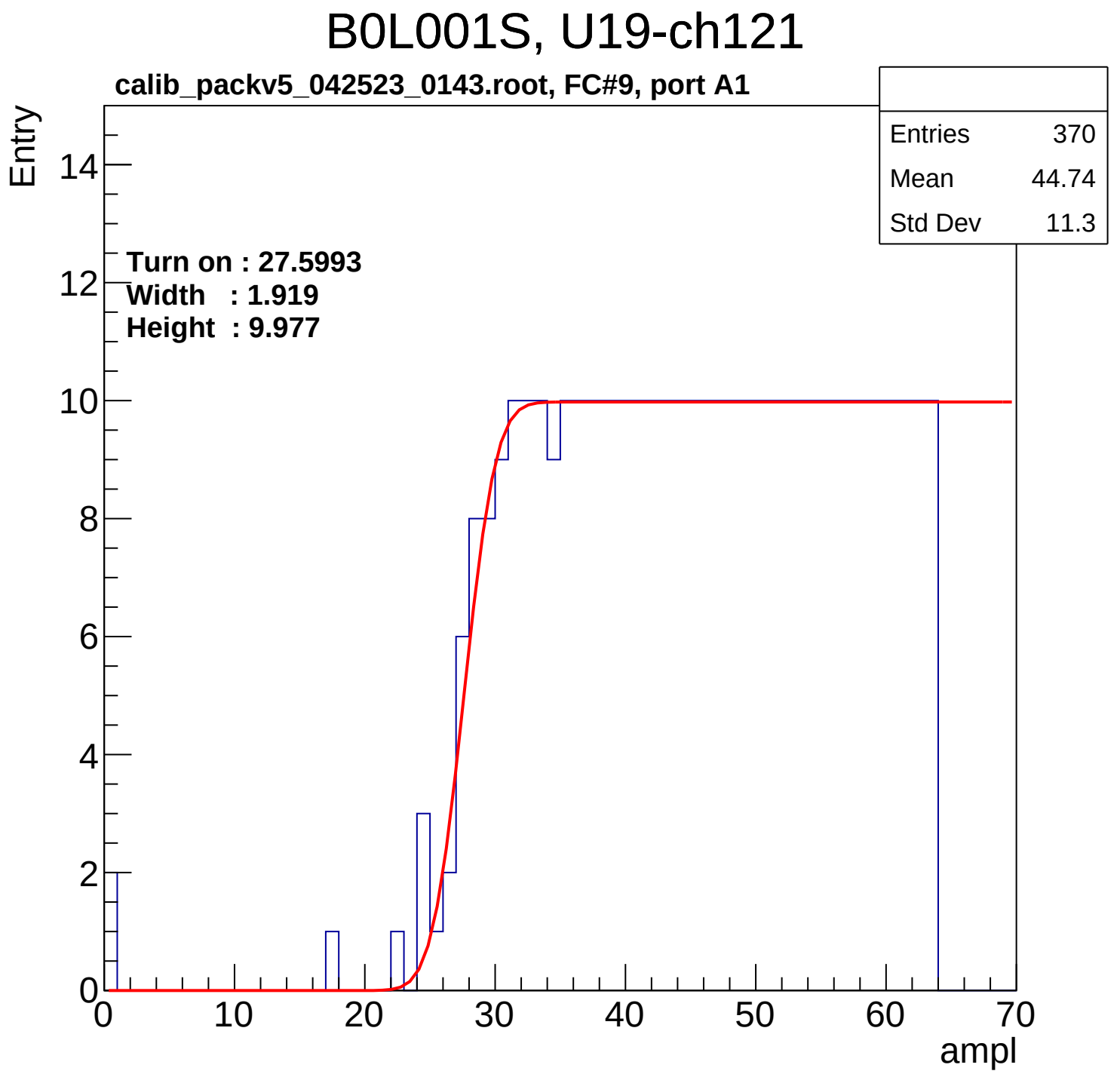
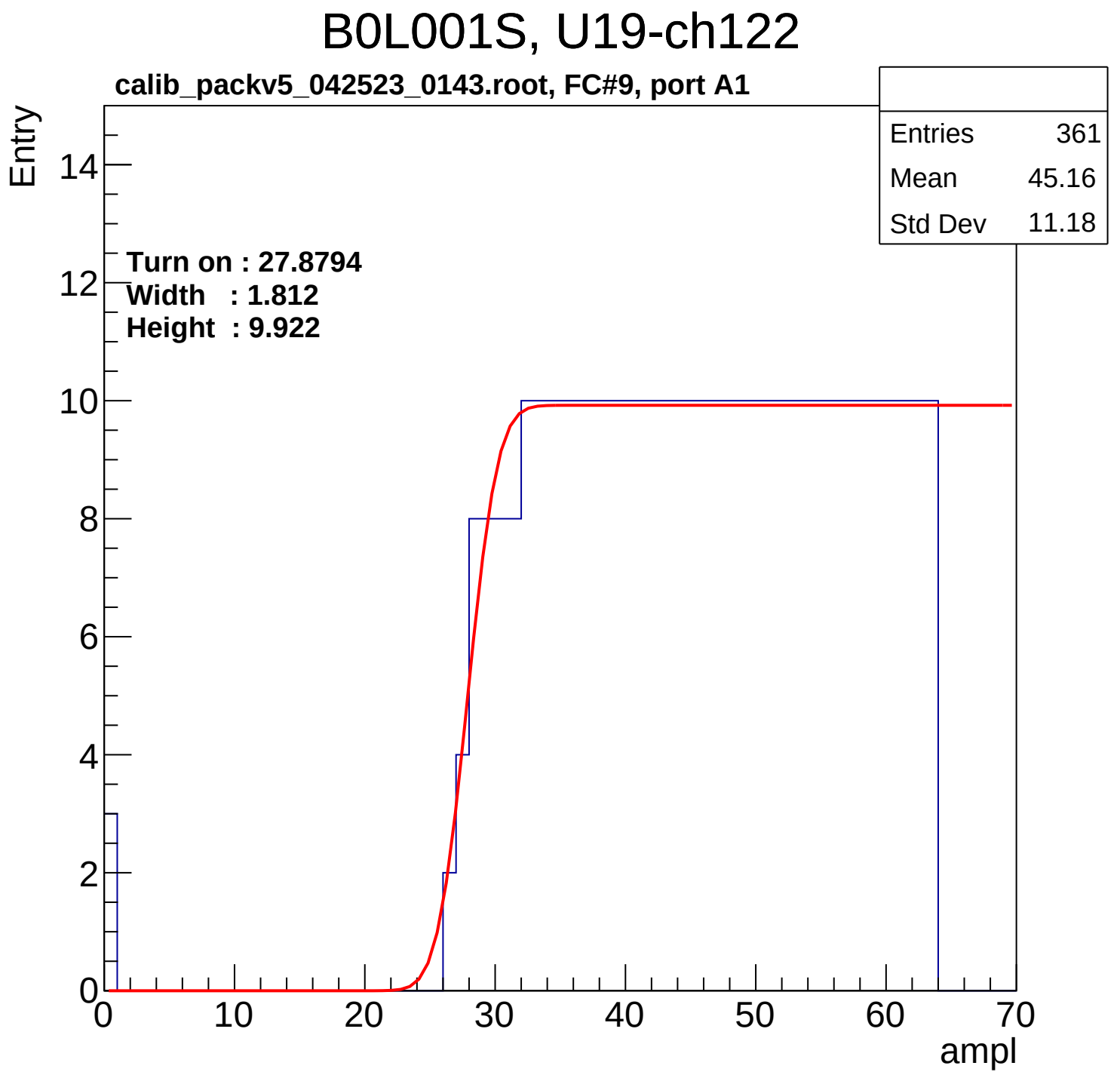

B0L001S, U19-ch121
calib_packv5_042523_0143.root, FC#9, port A1
Entries 370
Mean 44.74
Std Dev 11.3
Turn on : 27.5993
Width : 1.919
Height : 9.977
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U19-ch122
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 45.16
Std Dev 11.18
Turn on : 27.8794
Width : 1.812
Height : 9.922
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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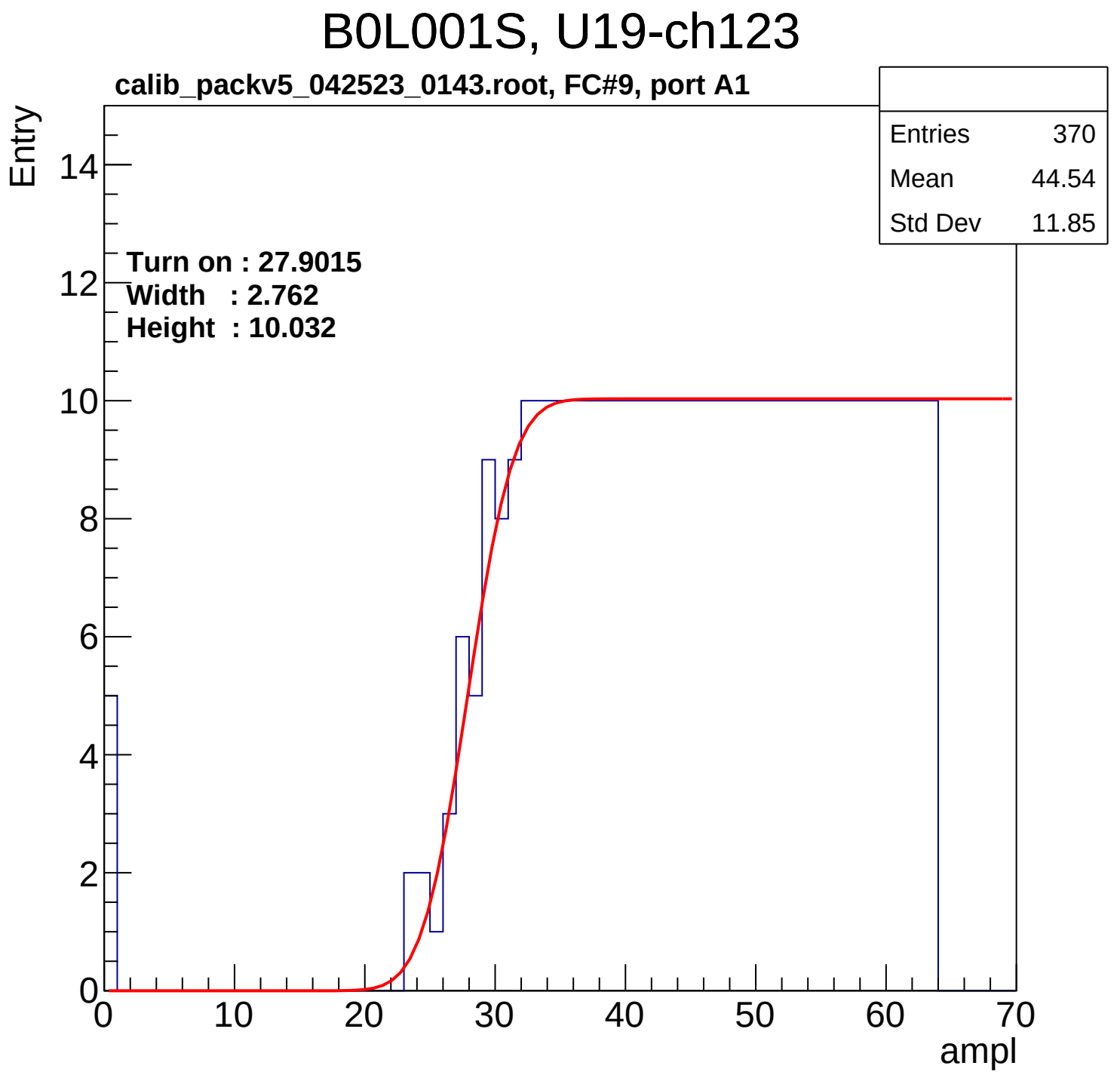
B0L001S, U19-ch123
calib_packv5_042523_0143.root, FC#9, port A1
Entries 370
Mean 44.54
Std Dev 11.85
Turn on : 27.9015
Width : 2.762
Height : 10.032
Entry
ampl
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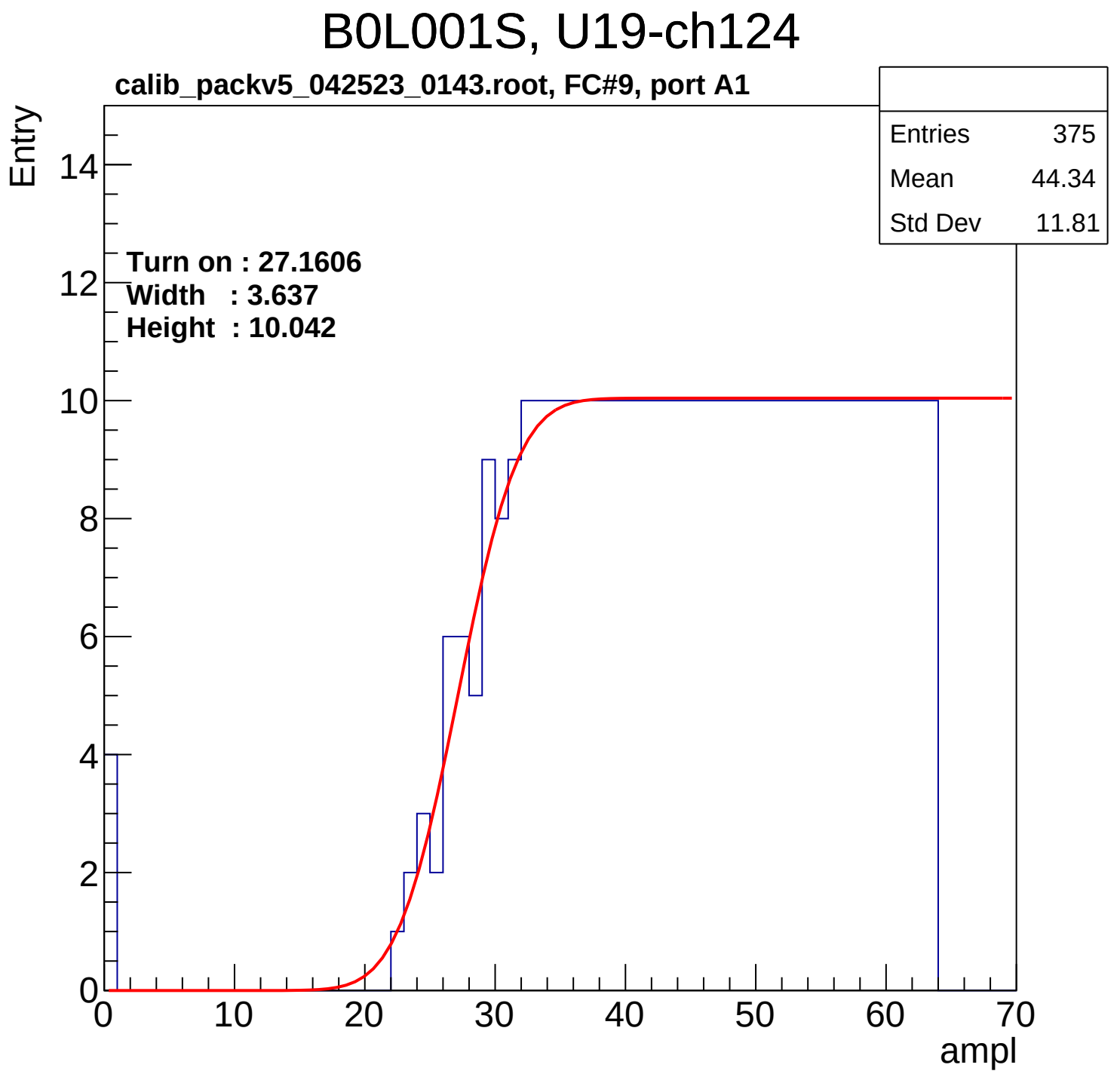
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U19-ch124
calib_packv5_042523_0143.root, FC#9, port A1
Entries 375
Mean 44.34
Std Dev 11.81
Turn on : 27.1606
Width : 3.637
Height : 10.042
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
30
40
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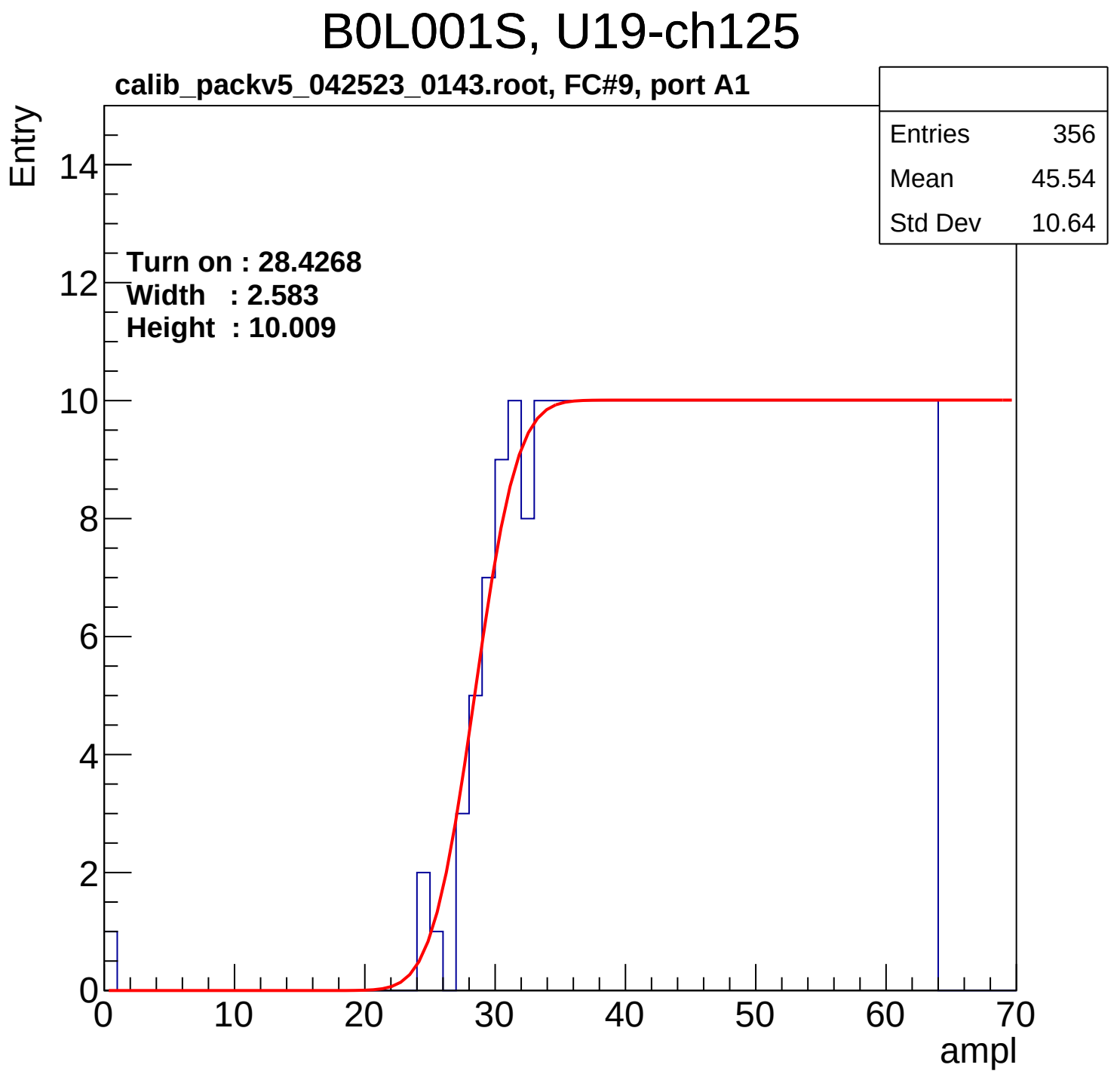
60
70


B0L001S, U19-ch125
calib_packv5_042523_0143.root, FC#9, port A1
Entries 356
Mean 45.54
Std Dev 10.64
Turn on : 28.4268
Width : 2.583
Height : 10.009
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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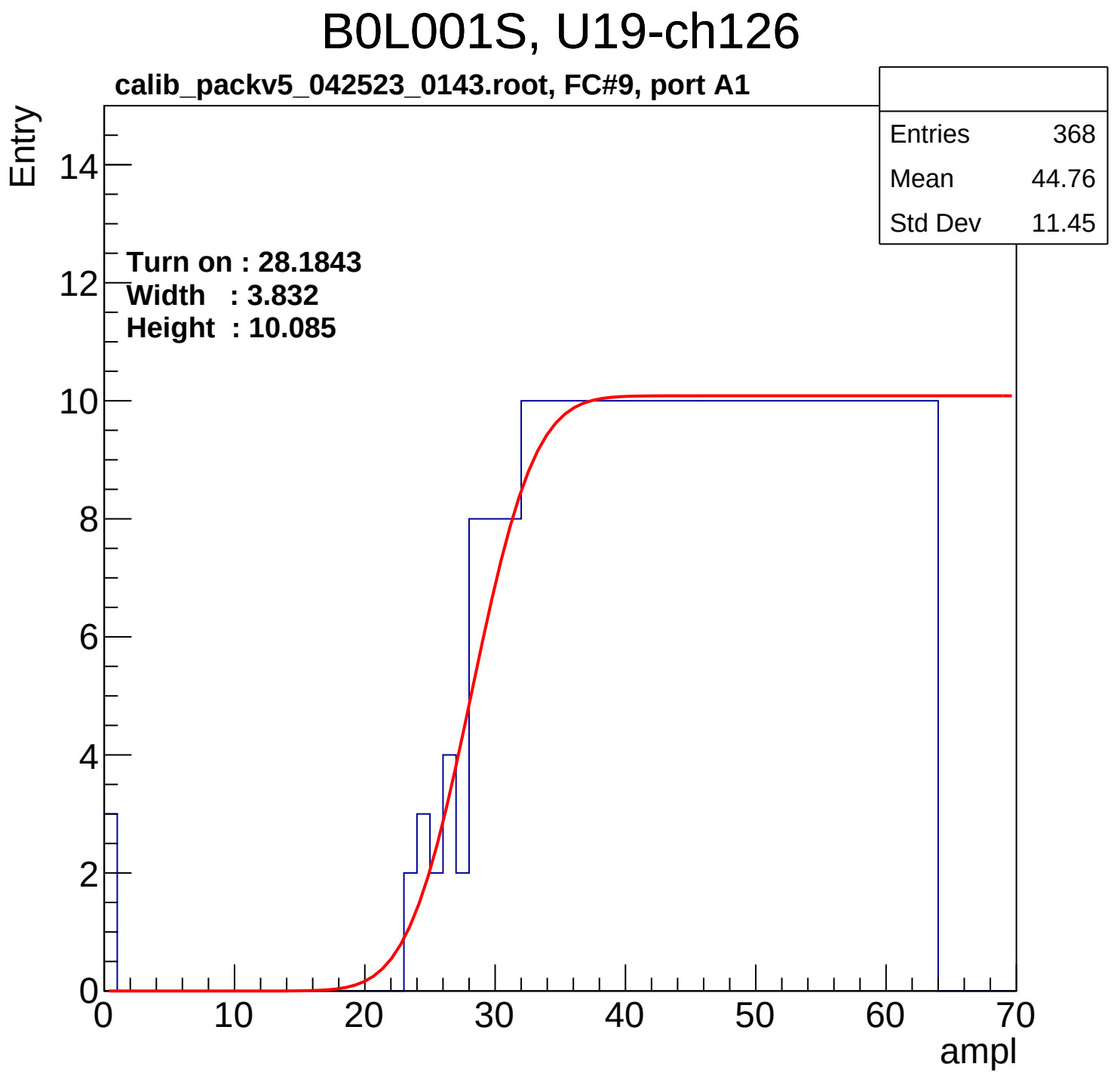
40
50
60
70


B0L001S, U19-ch126
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.76
Std Dev 11.45
Turn on : 28.1843
Width : 3.832
Height : 10.085
Entry
ampl
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2
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6
8
10
12
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0
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20
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60
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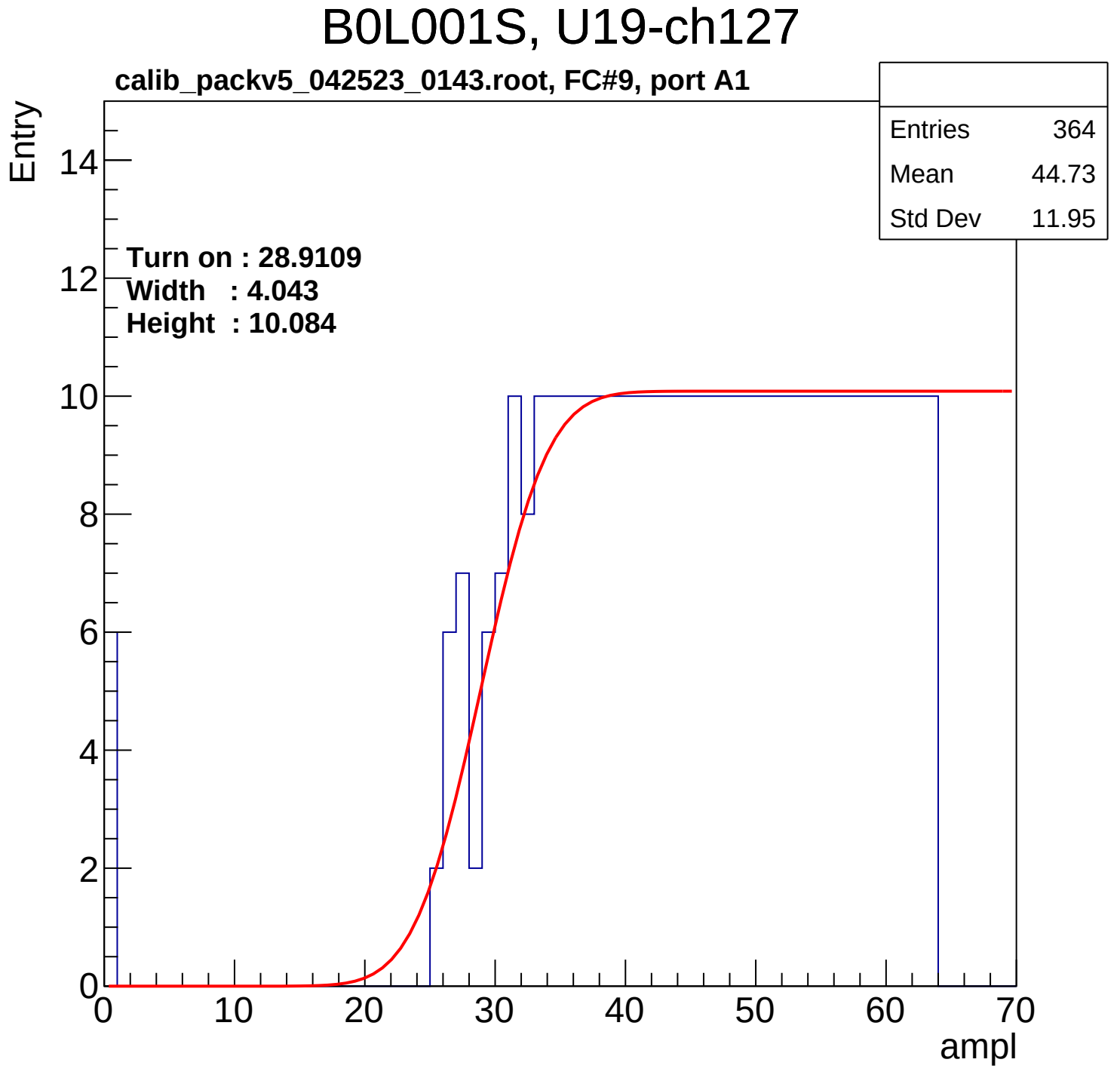
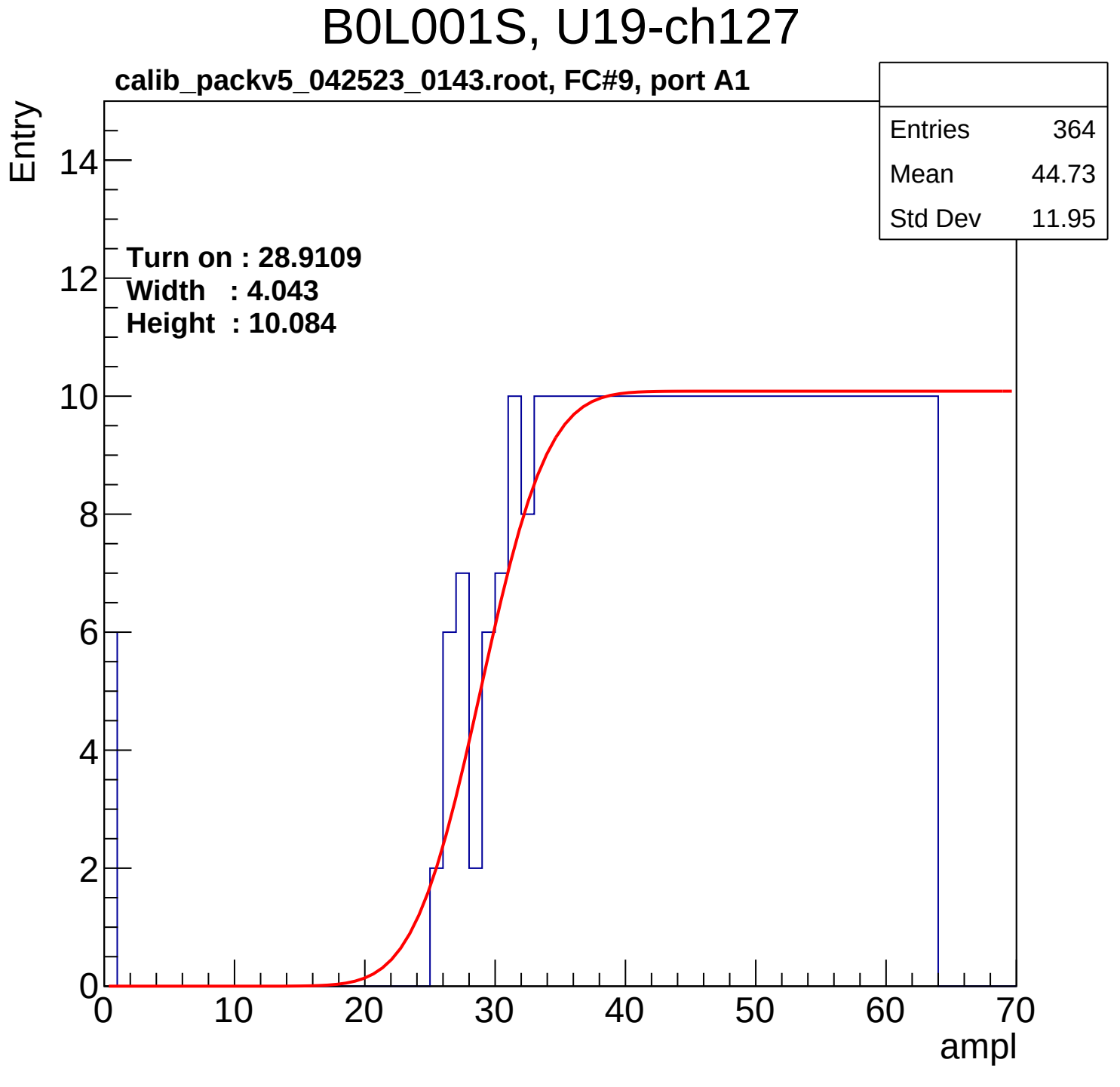

B0L001S, U19-ch127
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 44.73
Std Dev 11.95
Turn on : 28.9109
Width : 4.043
Height : 10.084
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U19-ch127
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 44.73
Std Dev 11.95
Turn on : 28.9109
Width : 4.043
Height : 10.084
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70