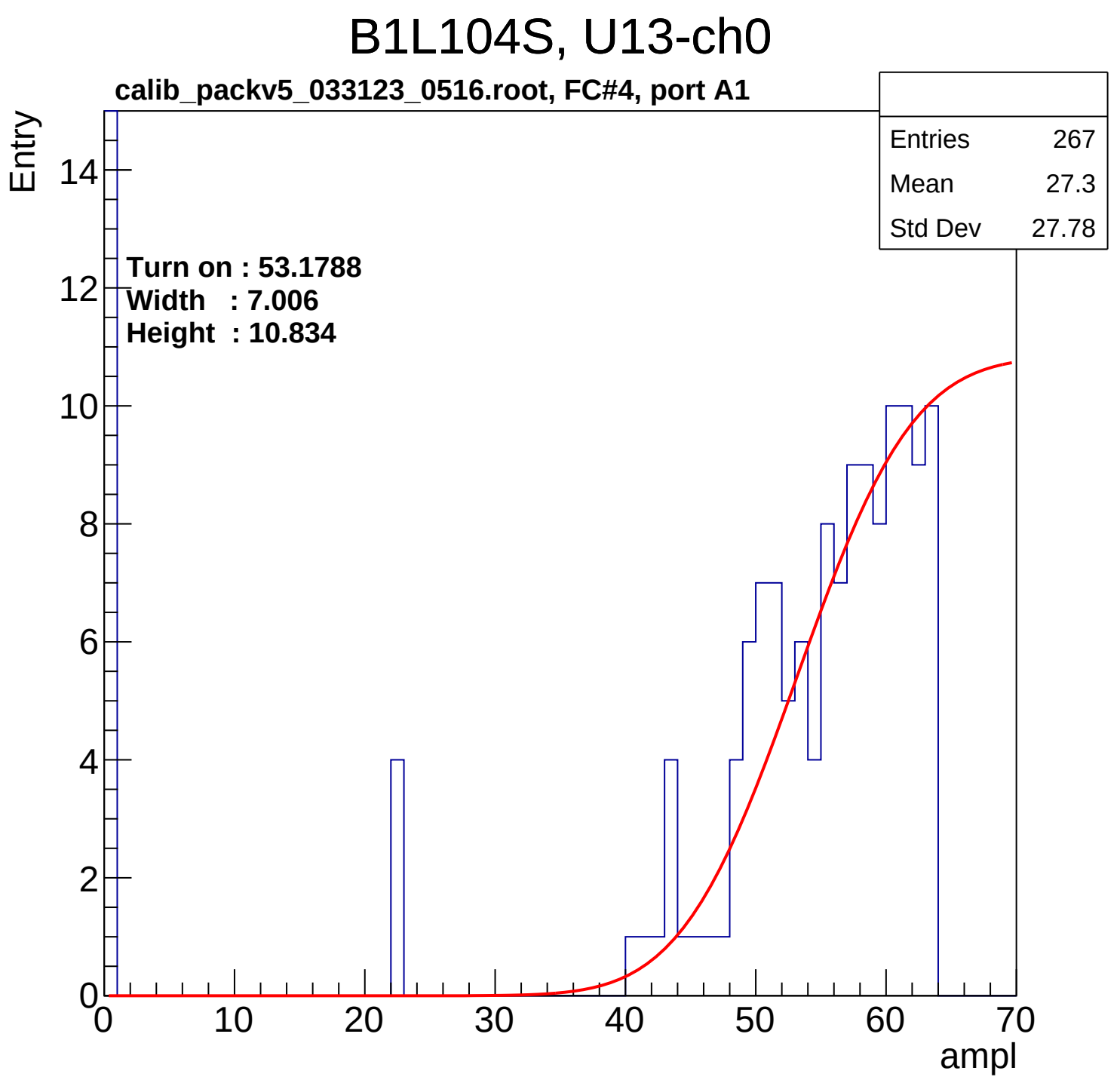
B1L104S, U13-ch0
calib_packv5_033123_0516.root, FC#4, port A1
Entries 267
Mean 27.3
Std Dev 27.78
Turn on : 53.1788
Width : 7.006
Height : 10.834
Entry
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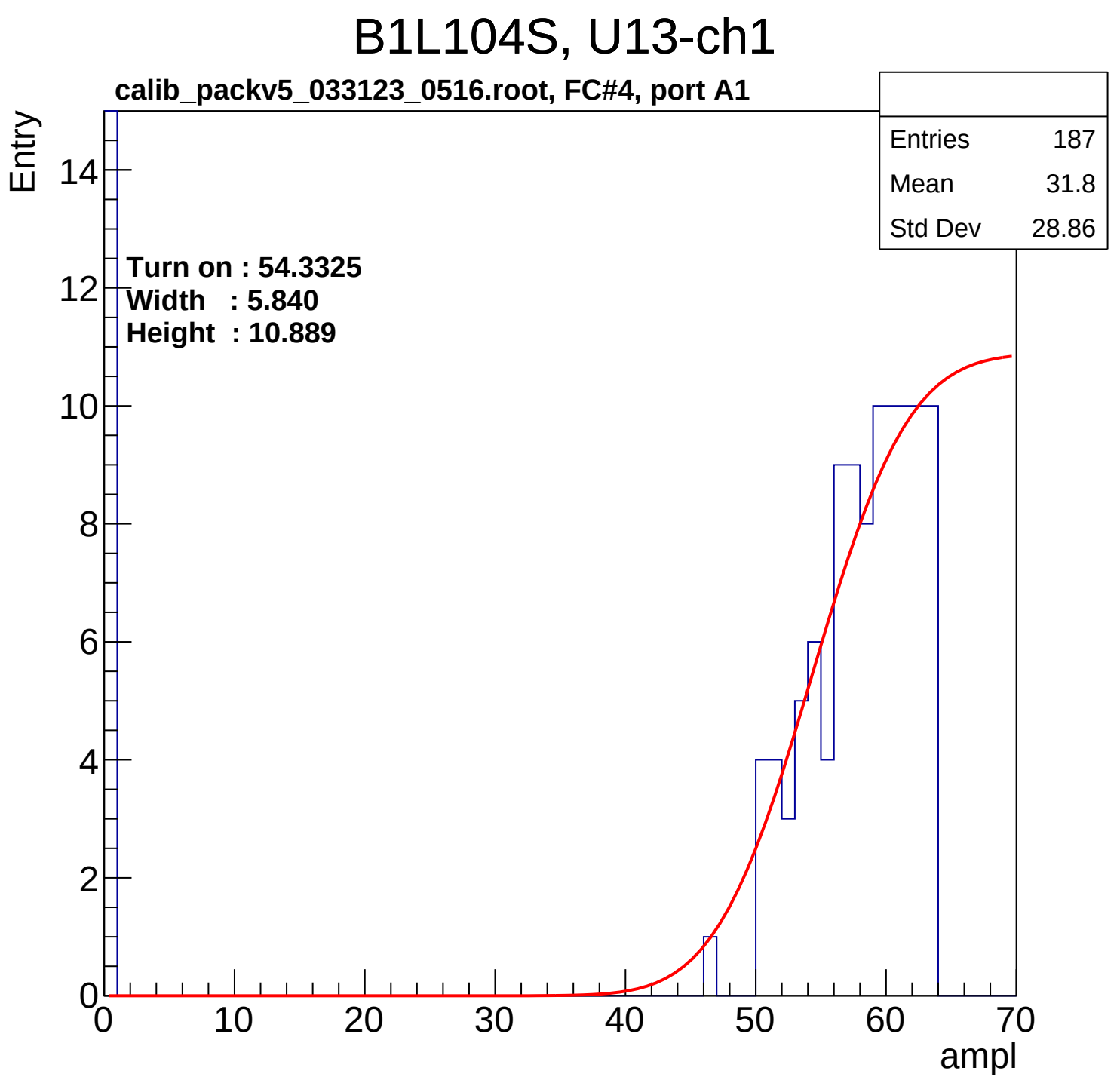
B1L104S, U13-ch1
calib_packv5_033123_0516.root, FC#4, port A1
Entries 187
Mean 31.8
Std Dev 28.86
Turn on : 54.3325
Width : 5.840
Height : 10.889
Entry
ampl
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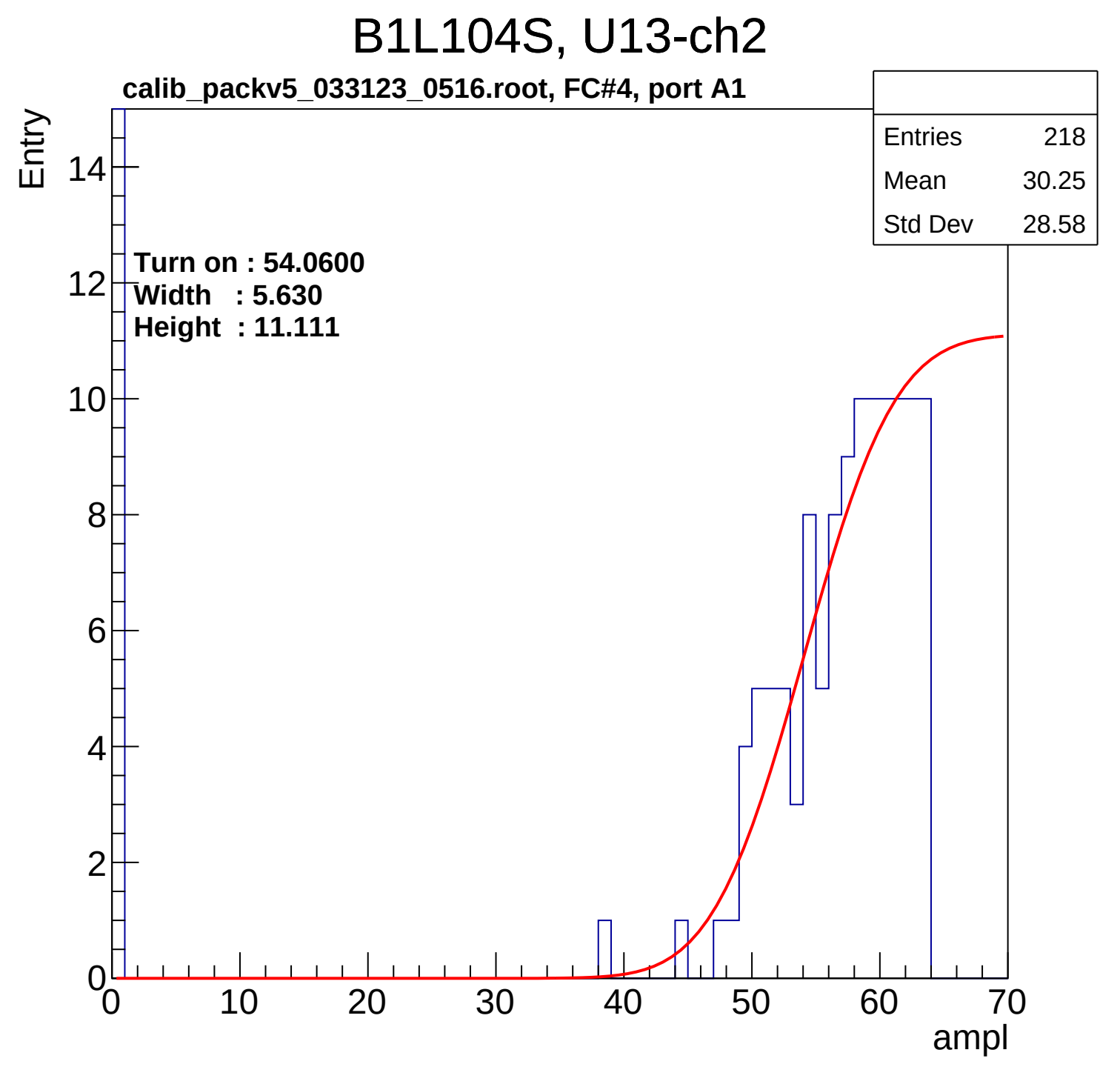
B1L104S, U13-ch2
calib_packv5_033123_0516.root, FC#4, port A1
Entries 218
Mean 30.25
Std Dev 28.58
Turn on : 54.0600
Width : 5.630
Height : 11.111
Entry
ampl
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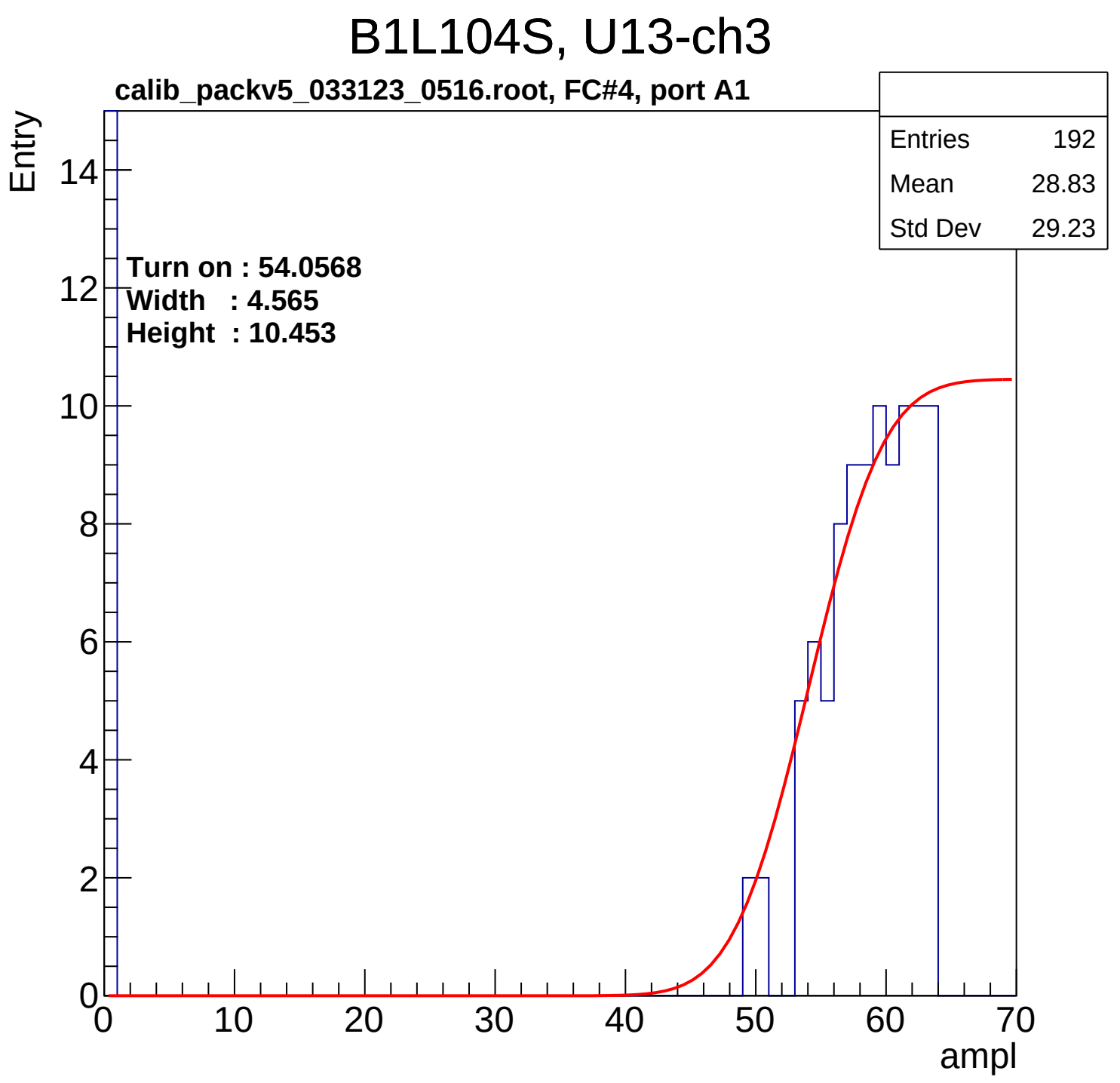
B1L104S, U13-ch3
calib_packv5_033123_0516.root, FC#4, port A1
Entries 192
Mean 28.83
Std Dev 29.23
Turn on : 54.0568
Width : 4.565
Height : 10.453
Entry
ampl
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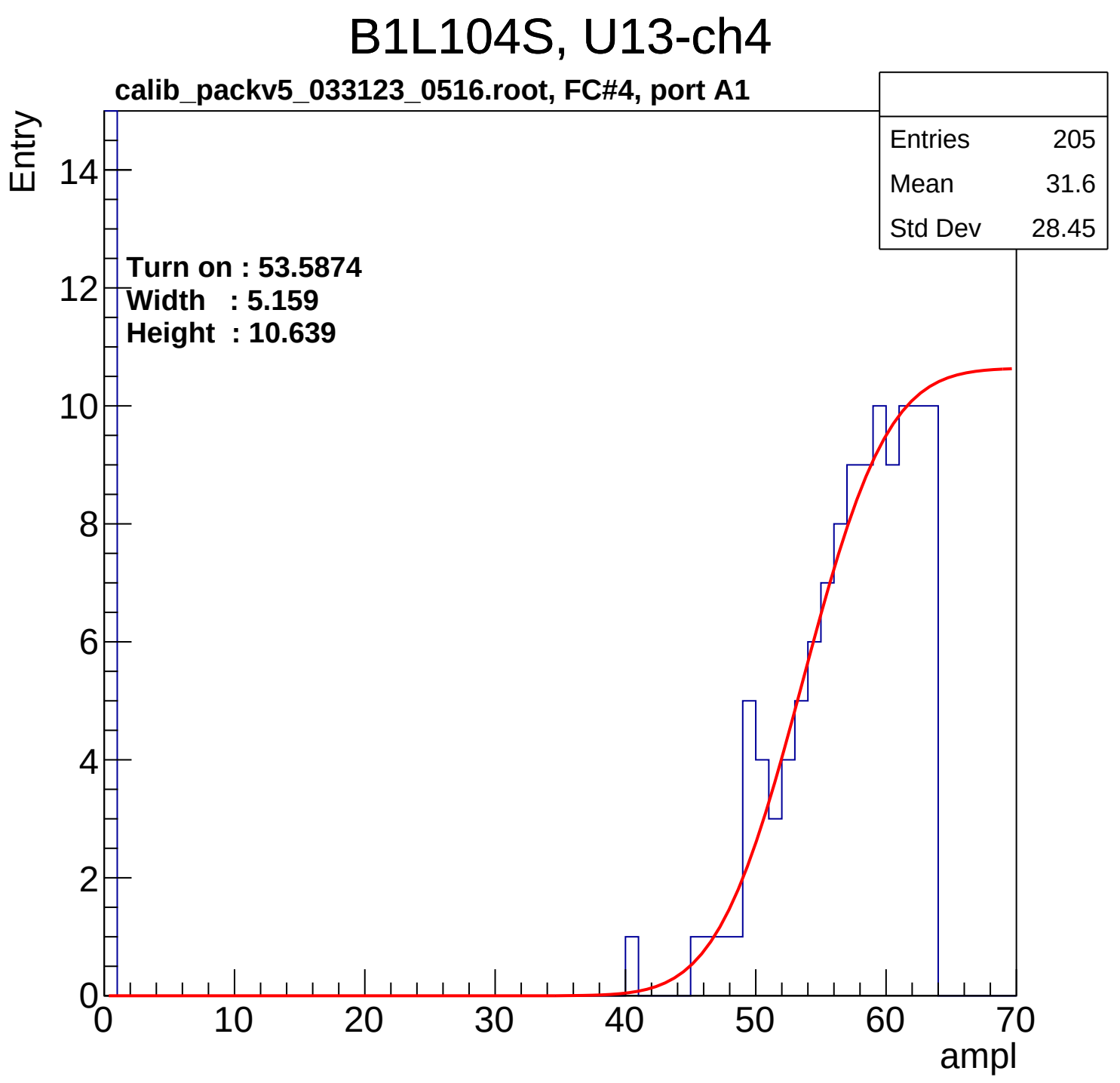
B1L104S, U13-ch4
calib_packv5_033123_0516.root, FC#4, port A1
Entries 205
Mean 31.6
Std Dev 28.45
Turn on : 53.5874
Width : 5.159
Height : 10.639
Entry
ampl
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8
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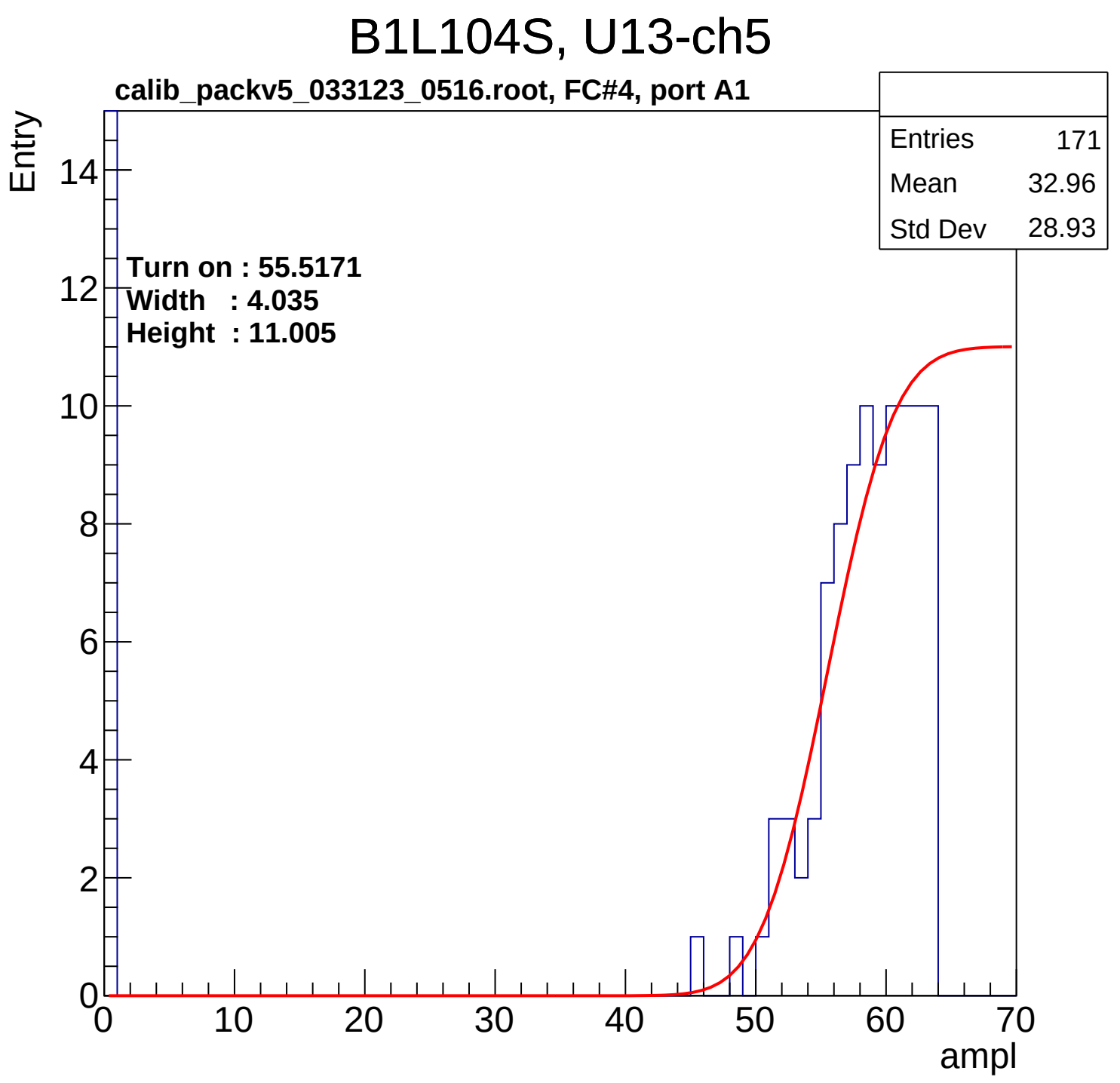
B1L104S, U13-ch5
calib_packv5_033123_0516.root, FC#4, port A1
Entries 171
Mean 32.96
Std Dev 28.93
Turn on : 55.5171
Width : 4.035
Height : 11.005
Entry
ampl
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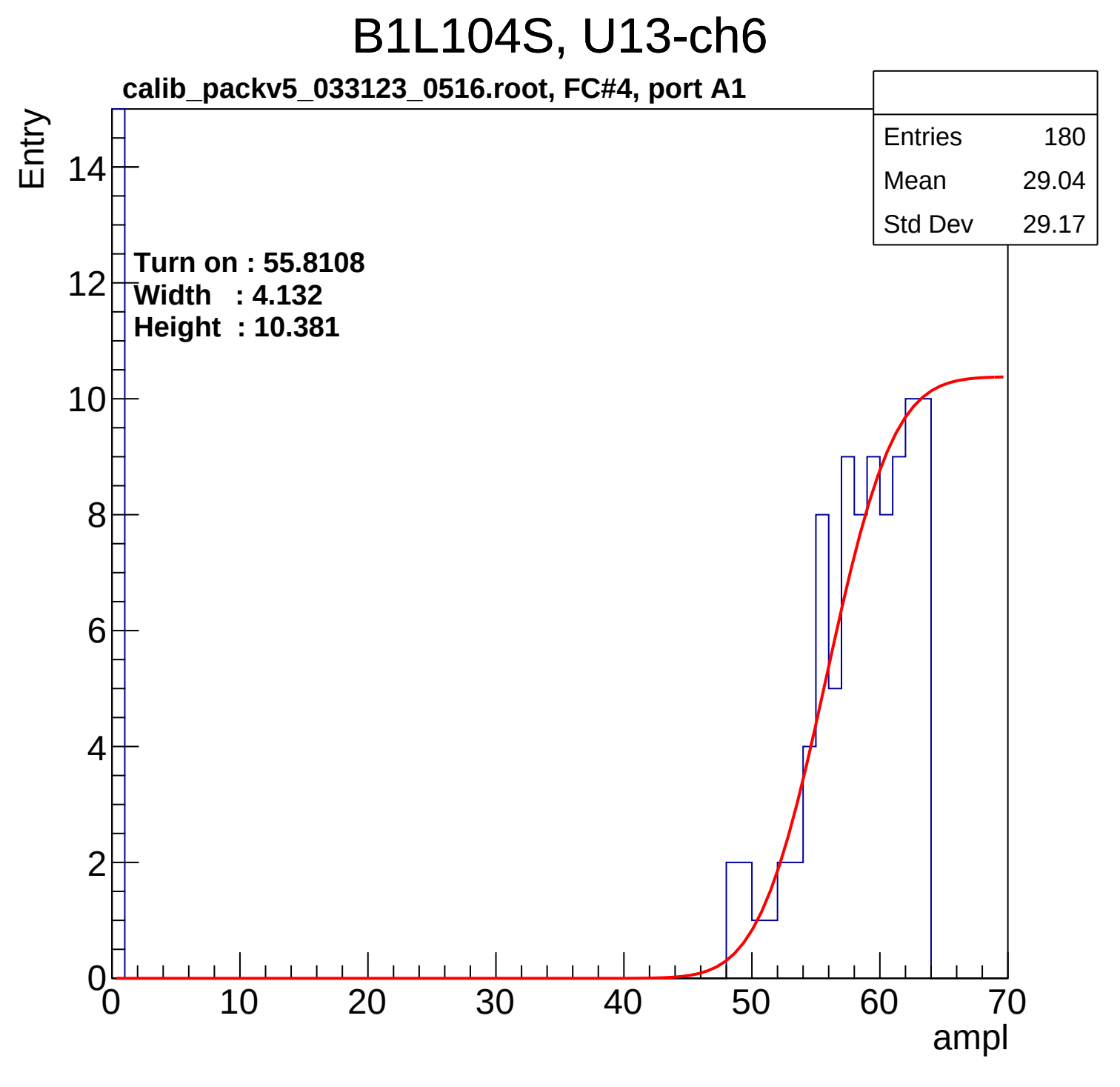
B1L104S, U13-ch6
calib_packv5_033123_0516.root, FC#4, port A1
Entries 180
Mean 29.04
Std Dev 29.17
Turn on : 55.8108
Width : 4.132
Height : 10.381
Entry
ampl
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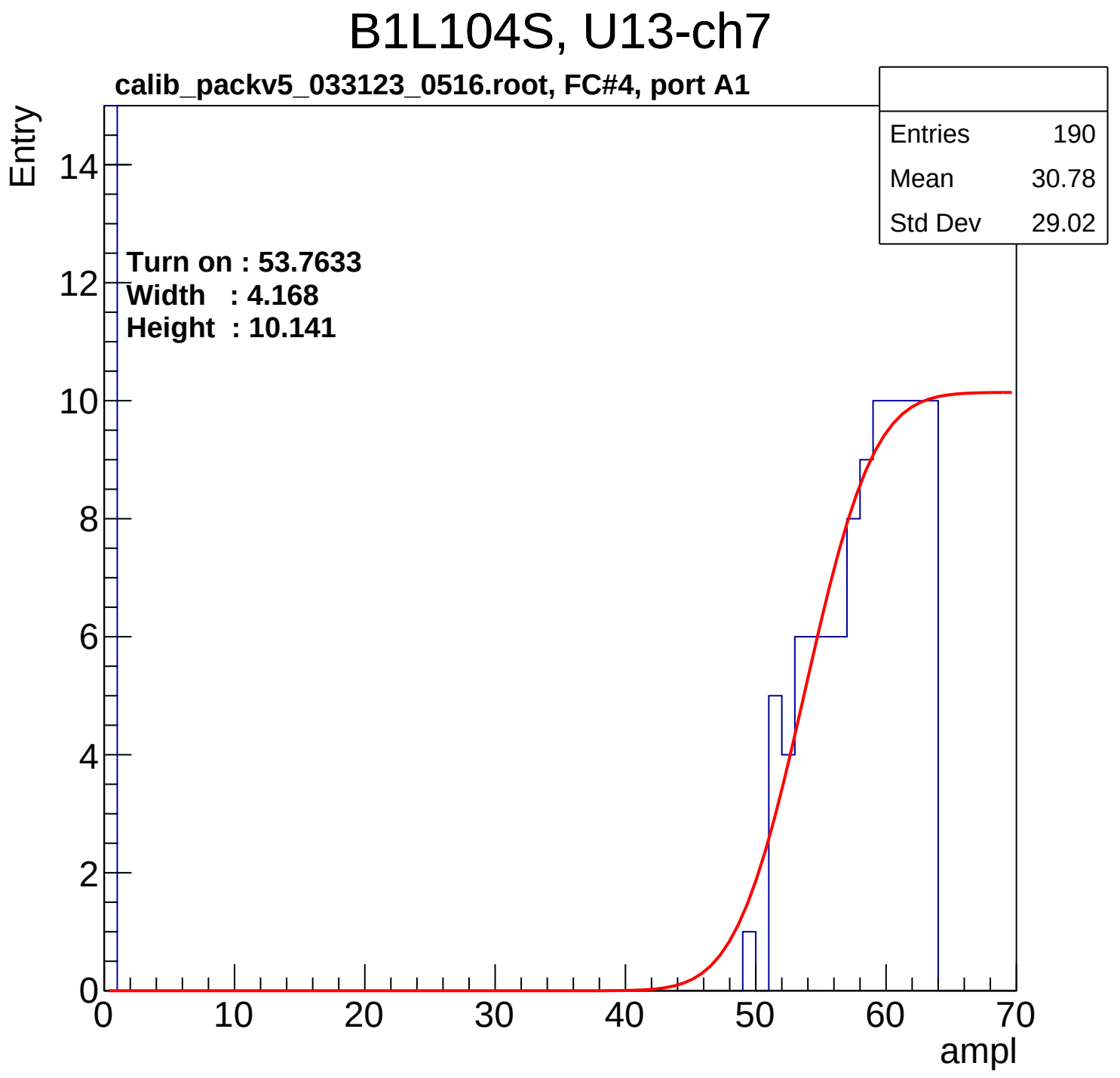
B1L104S, U13-ch7
calib_packv5_033123_0516.root, FC#4, port A1
Entries 190
Mean 30.78
Std Dev 29.02
Turn on : 53.7633
Width : 4.168
Height : 10.141
Entry
ampl
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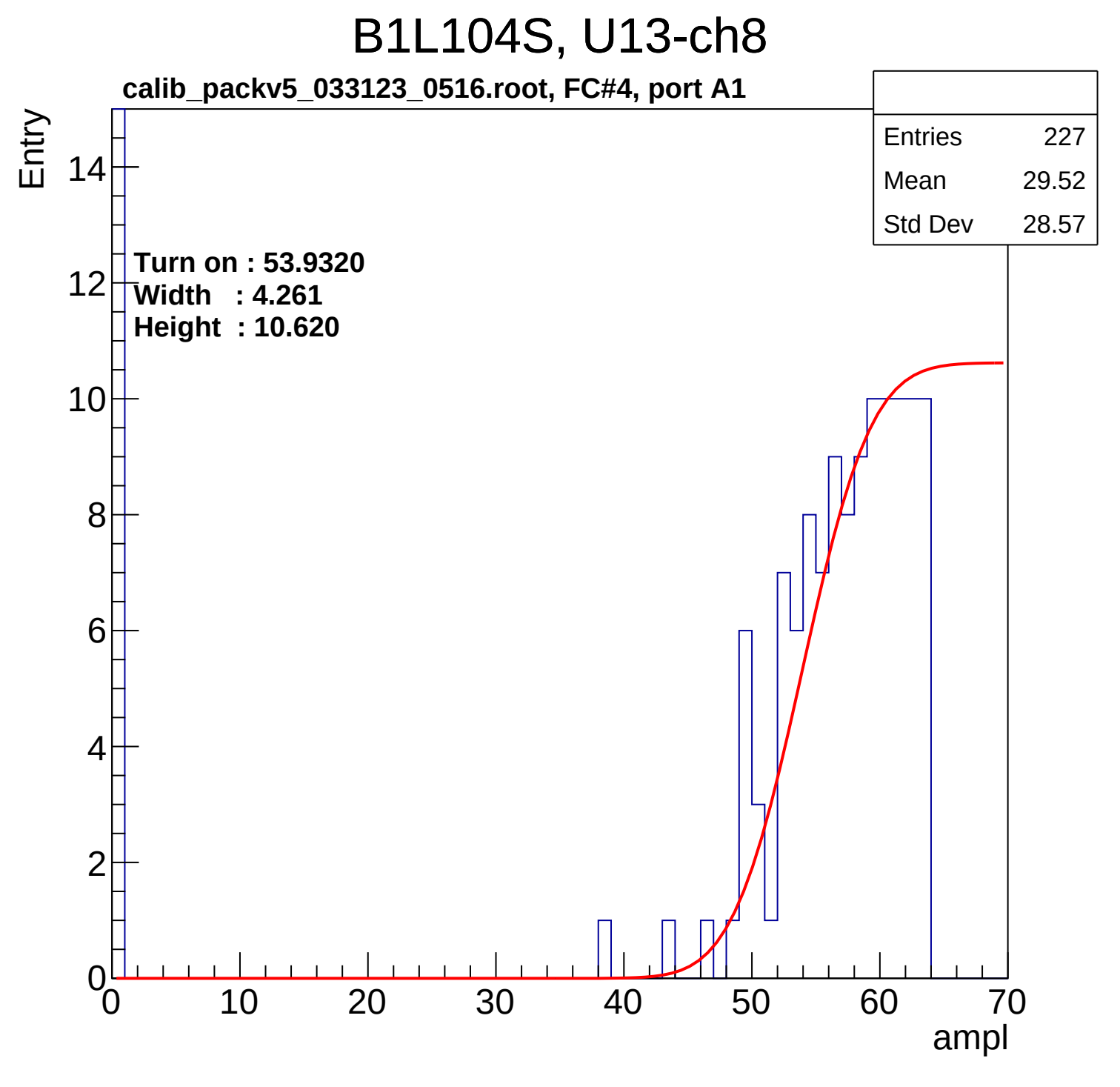
B1L104S, U13-ch8
calib_packv5_033123_0516.root, FC#4, port A1
Entries 227
Mean 29.52
Std Dev 28.57
Turn on : 53.9320
Width : 4.261
Height : 10.620
Entry
ampl
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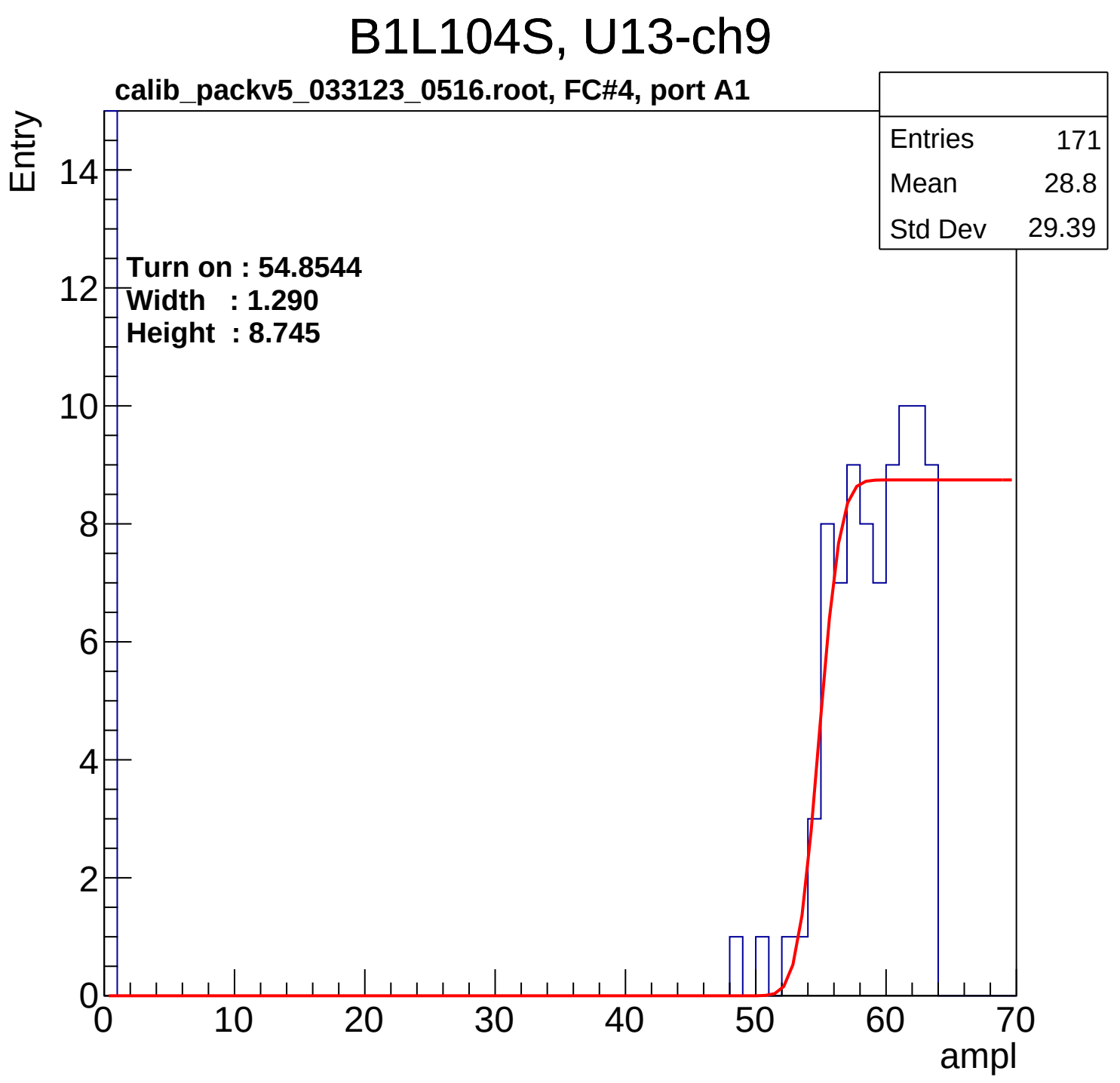
B1L104S, U13-ch9
calib_packv5_033123_0516.root, FC#4, port A1
Entries 171
Mean 28.8
Std Dev 29.39
Turn on : 54.8544
Width : 1.290
Height : 8.745
Entry
ampl
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6
8
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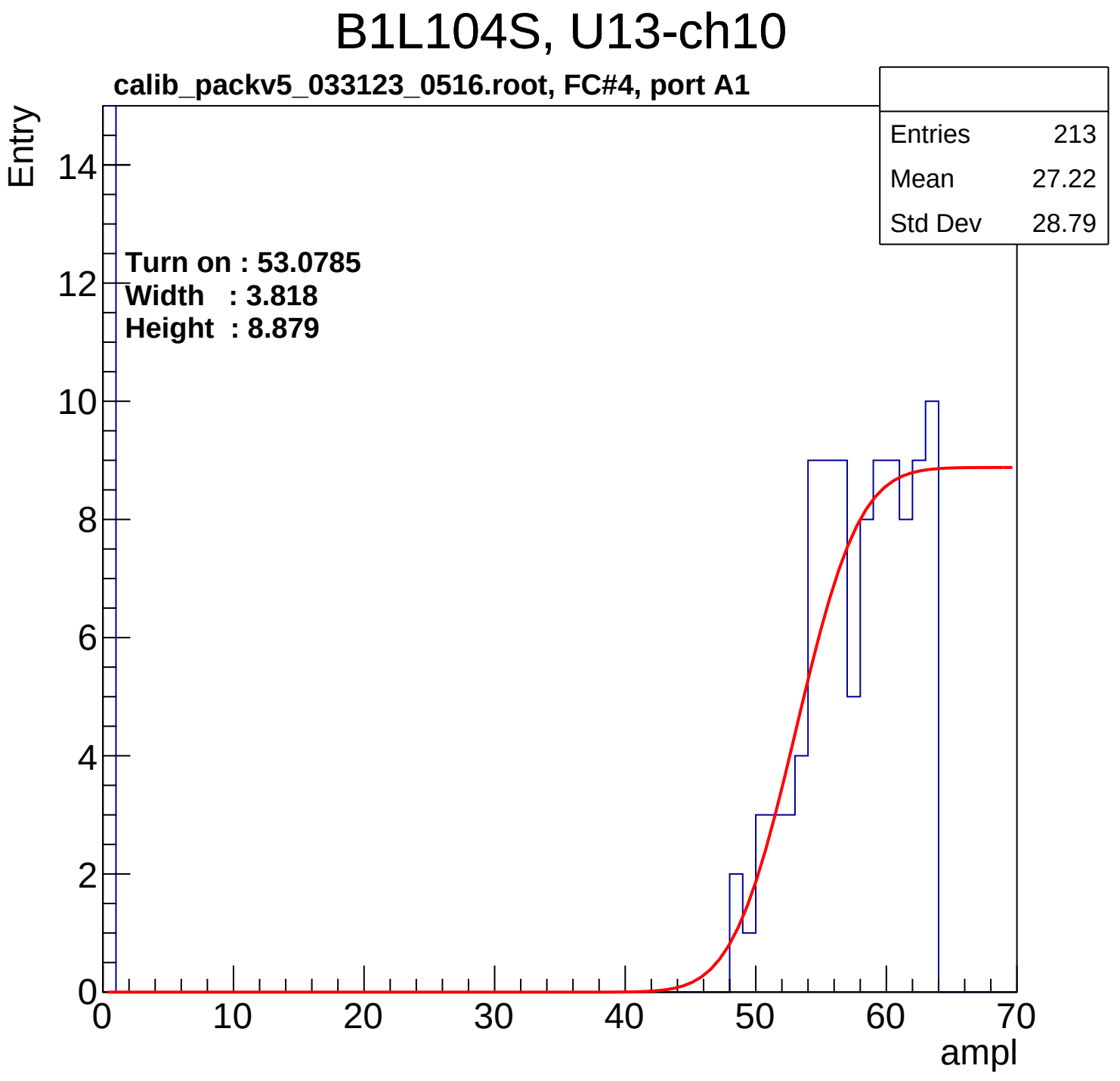
B1L104S, U13-ch10
calib_packv5_033123_0516.root, FC#4, port A1
Entries 213
Mean 27.22
Std Dev 28.79
Turn on : 53.0785
Width : 3.818
Height : 8.879
Entry
ampl
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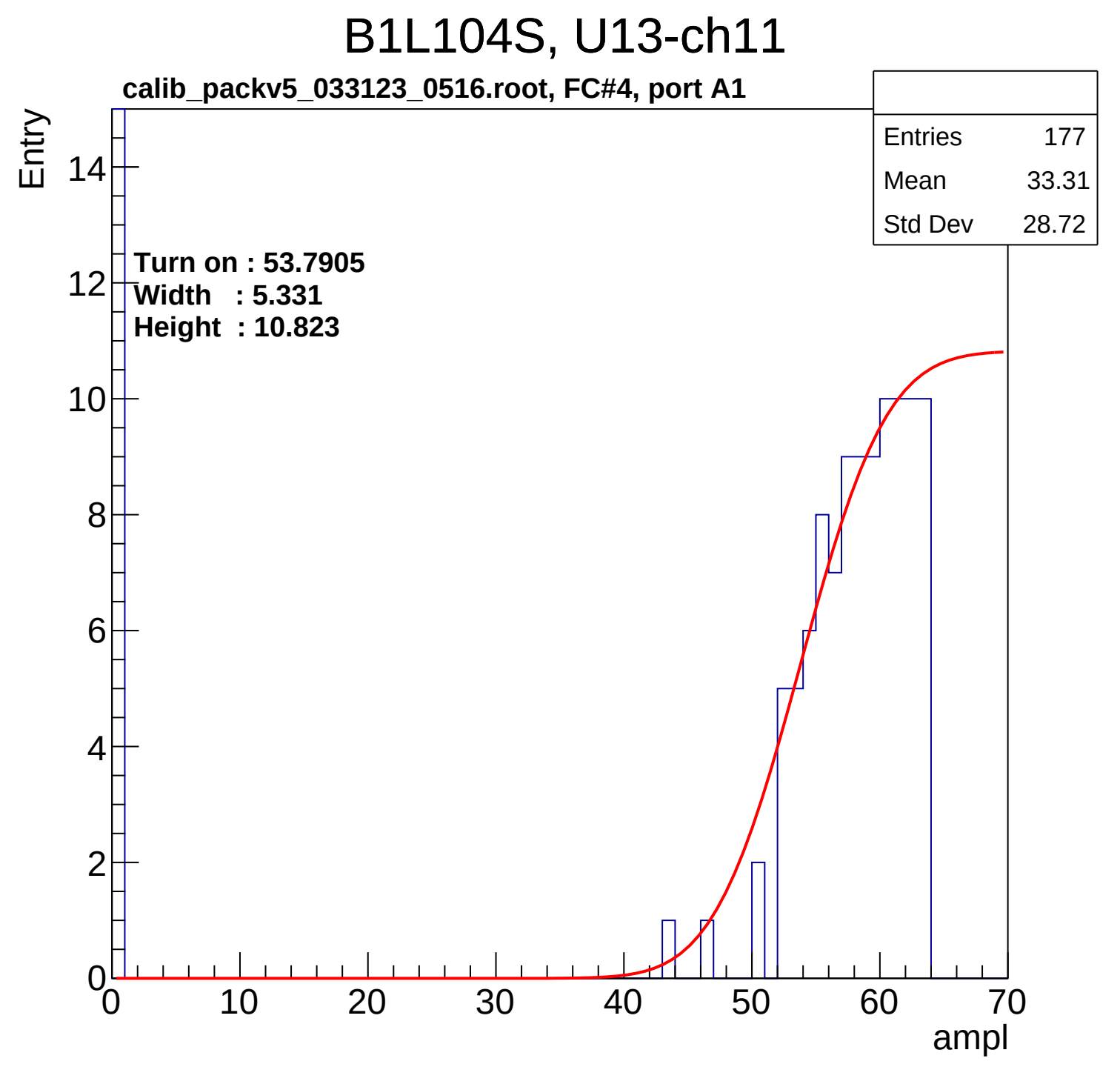
B1L104S, U13-ch11
calib_packv5_033123_0516.root, FC#4, port A1
Entries 177
Mean 33.31
Std Dev 28.72
Turn on : 53.7905
Width : 5.331
Height : 10.823
Entry
ampl
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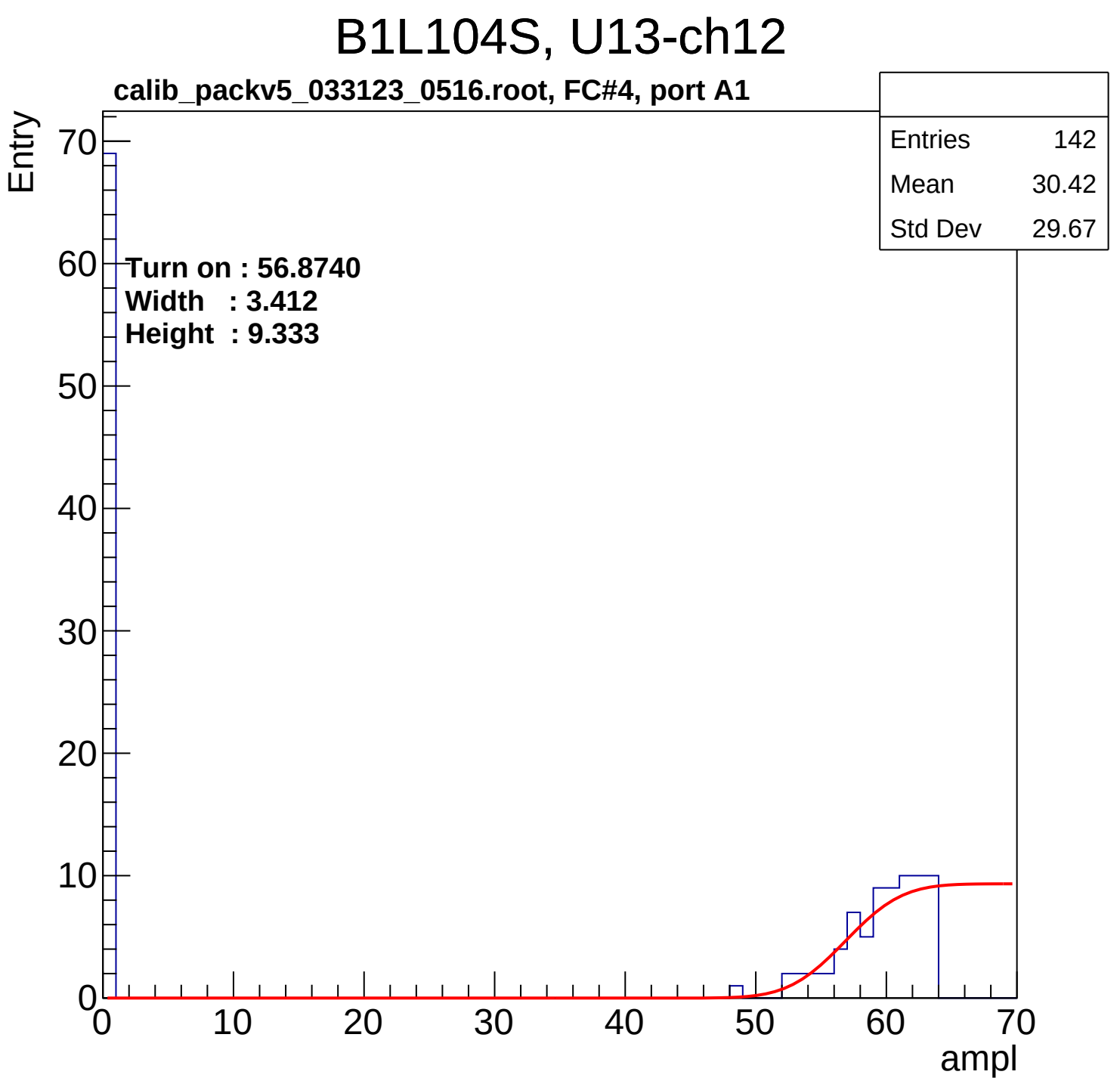
B1L104S, U13-ch12
calib_packv5_033123_0516.root, FC#4, port A1
Entries 142
Mean 30.42
Std Dev 29.67
Turn on : 56.8740
Width : 3.412
Height : 9.333
Entry
ampl
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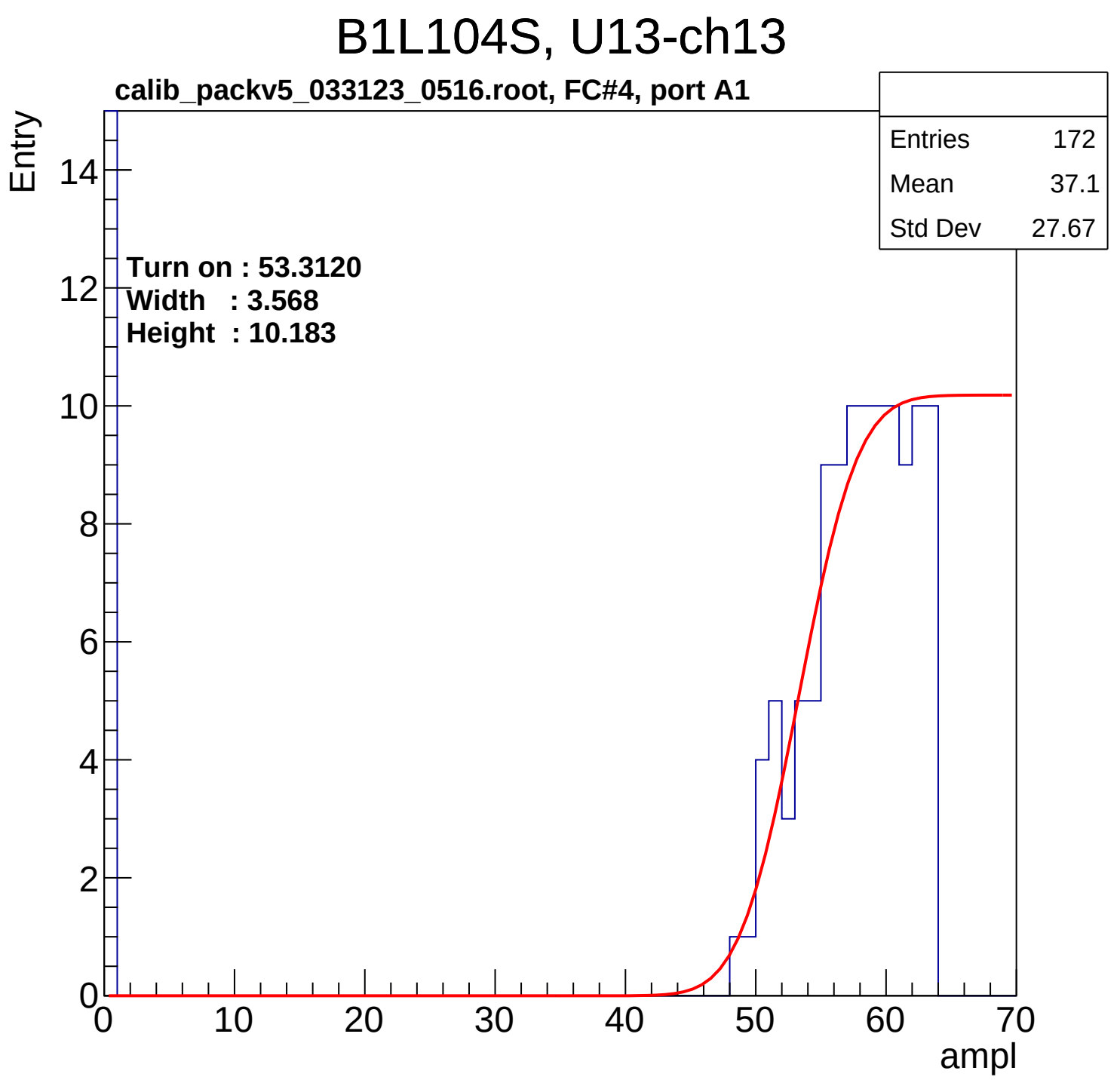
B1L104S, U13-ch13
calib_packv5_033123_0516.root, FC#4, port A1
Entries 172
Mean 37.1
Std Dev 27.67
Turn on : 53.3120
Width : 3.568
Height : 10.183
Entry
ampl
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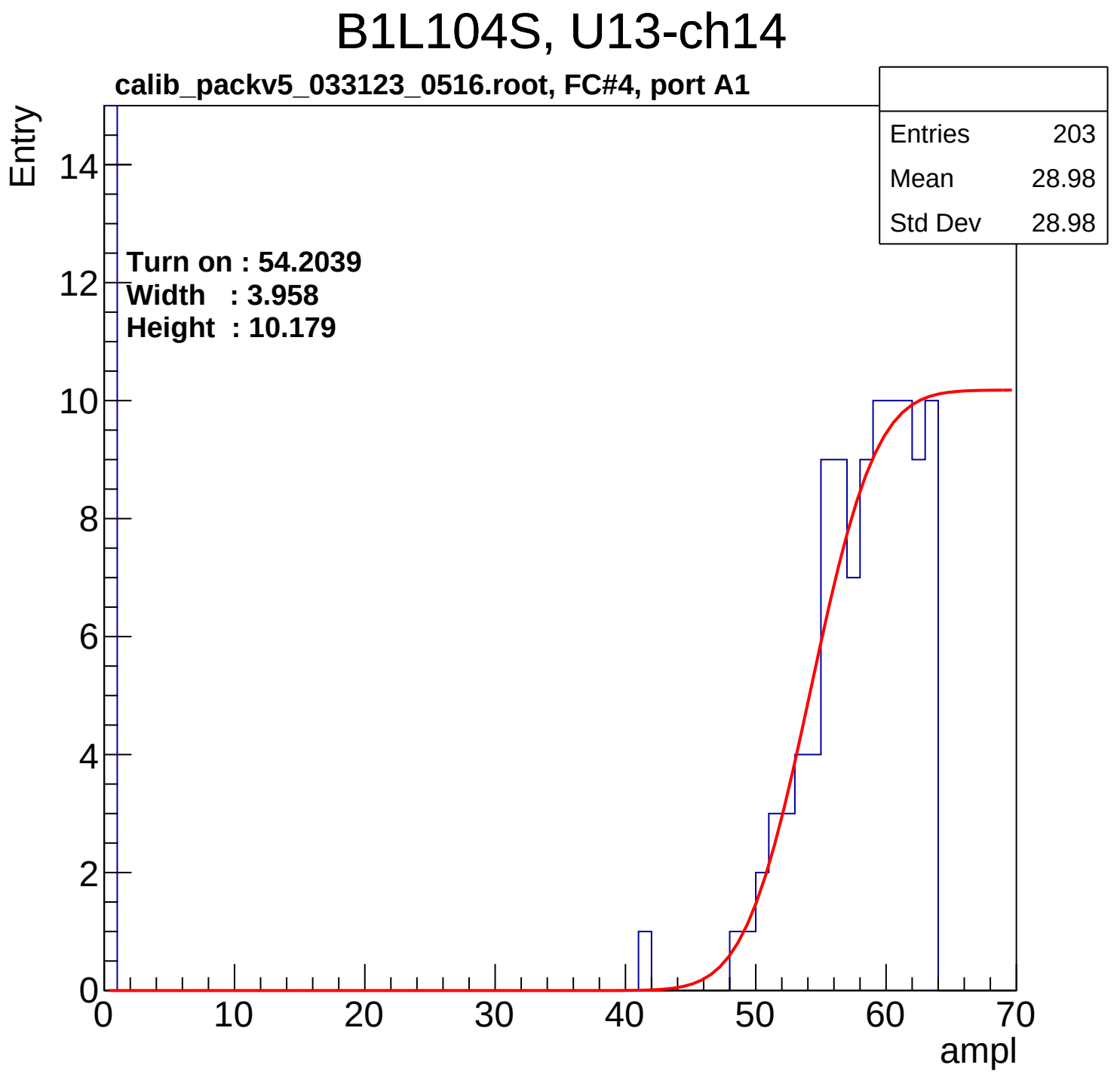
B1L104S, U13-ch14
calib_packv5_033123_0516.root, FC#4, port A1
Entries 203
Mean 28.98
Std Dev 28.98
Turn on : 54.2039
Width : 3.958
Height : 10.179
Entry
ampl
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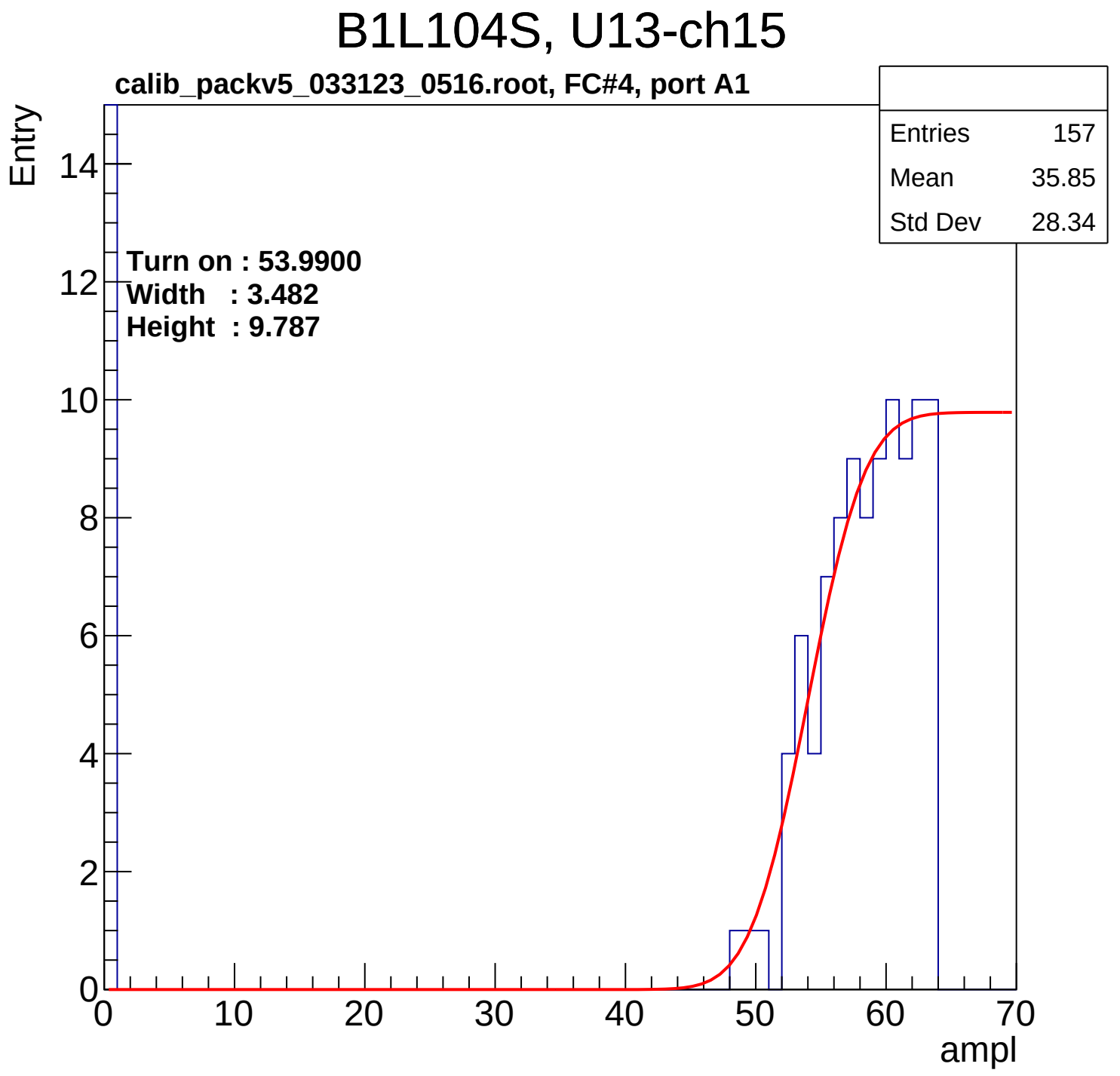
B1L104S, U13-ch15
calib_packv5_033123_0516.root, FC#4, port A1
Entries 157
Mean 35.85
Std Dev 28.34
Turn on : 53.9900
Width : 3.482
Height : 9.787
Entry
ampl
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6
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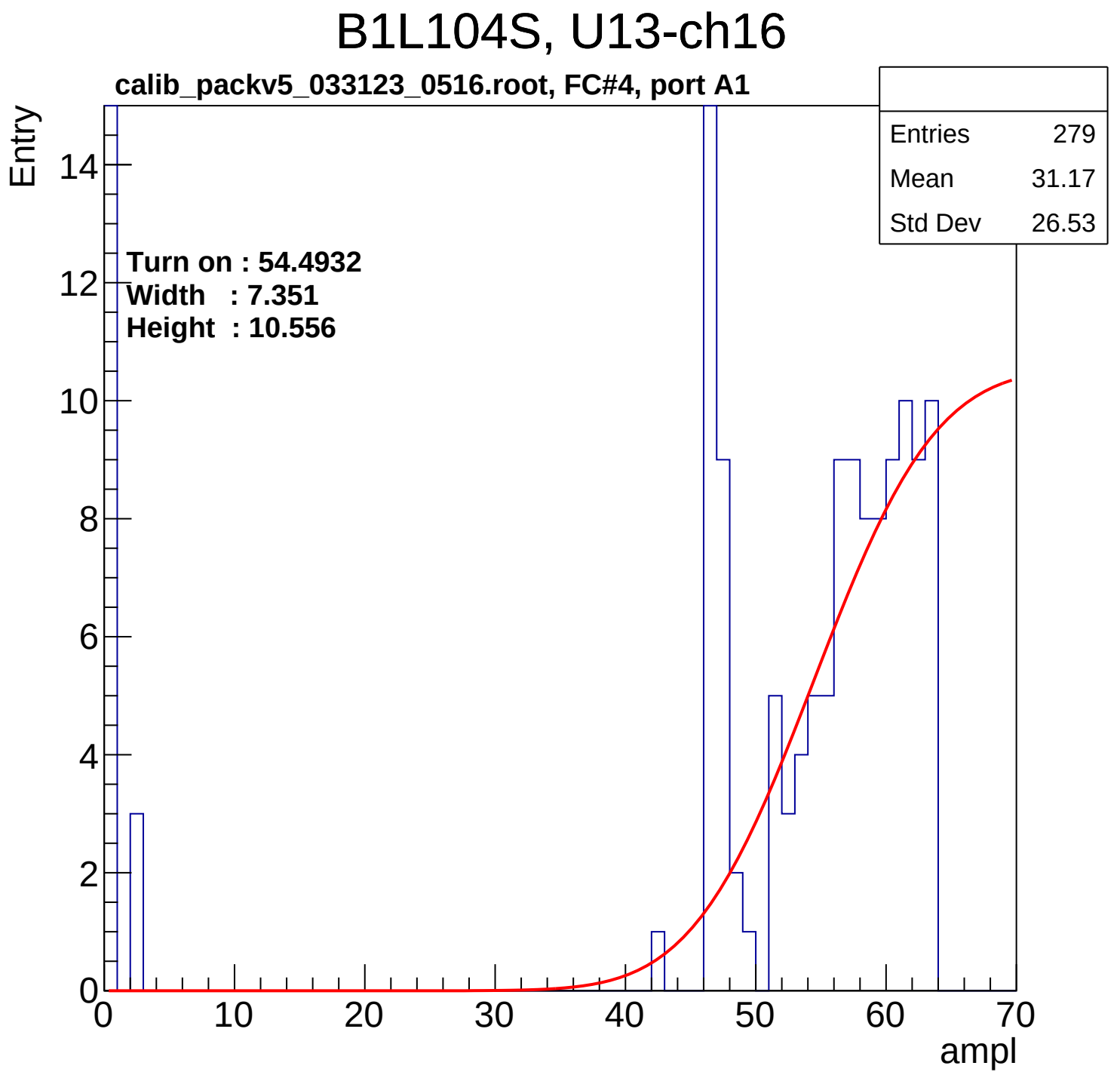
B1L104S, U13-ch16
calib_packv5_033123_0516.root, FC#4, port A1
Entries 279
Mean 31.17
Std Dev 26.53
Turn on : 54.4932
Width : 7.351
Height : 10.556
Entry
ampl
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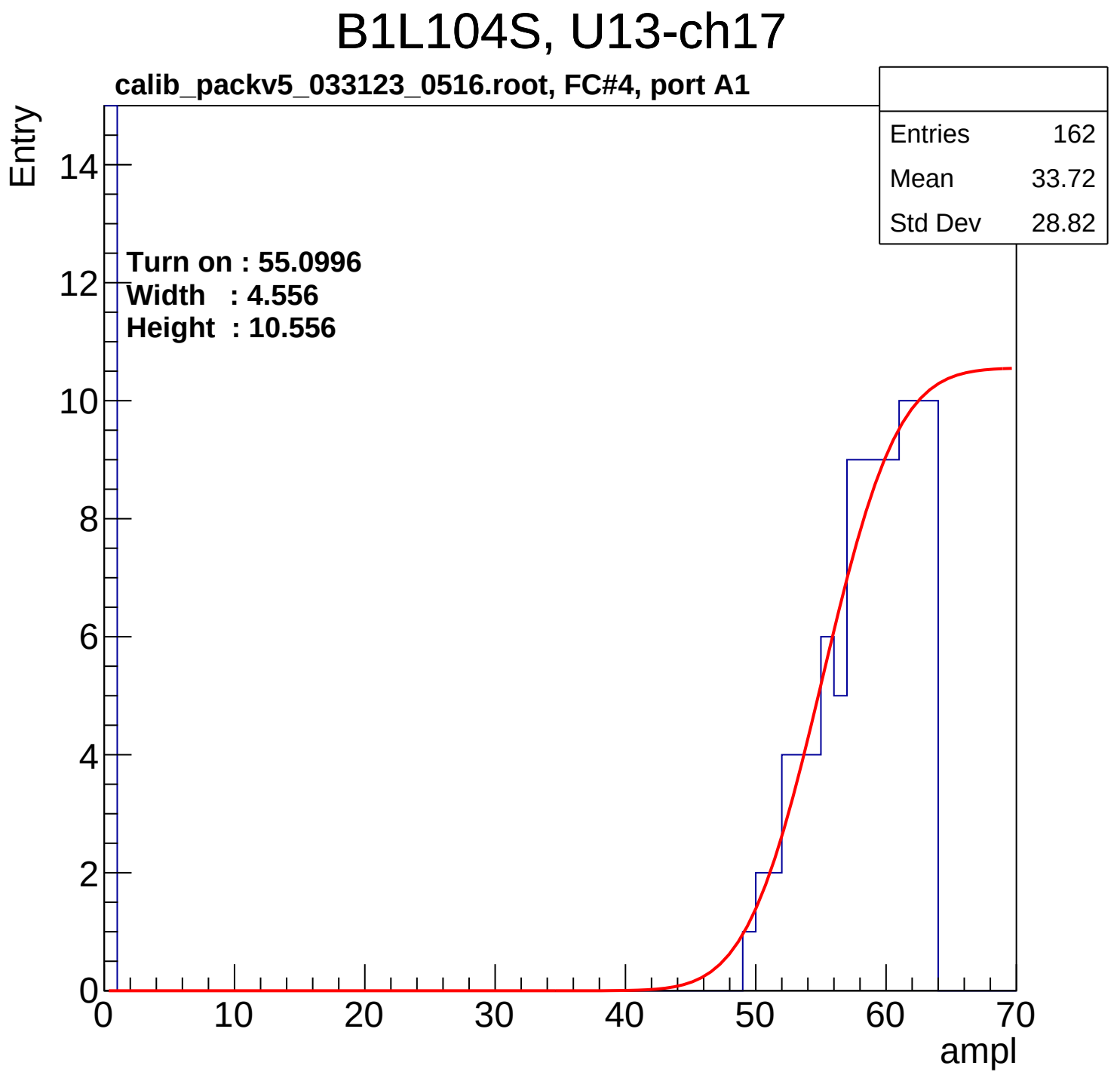
B1L104S, U13-ch17
calib_packv5_033123_0516.root, FC#4, port A1
Entries 162
Mean 33.72
Std Dev 28.82
Turn on : 55.0996
Width : 4.556
Height : 10.556
Entry
ampl
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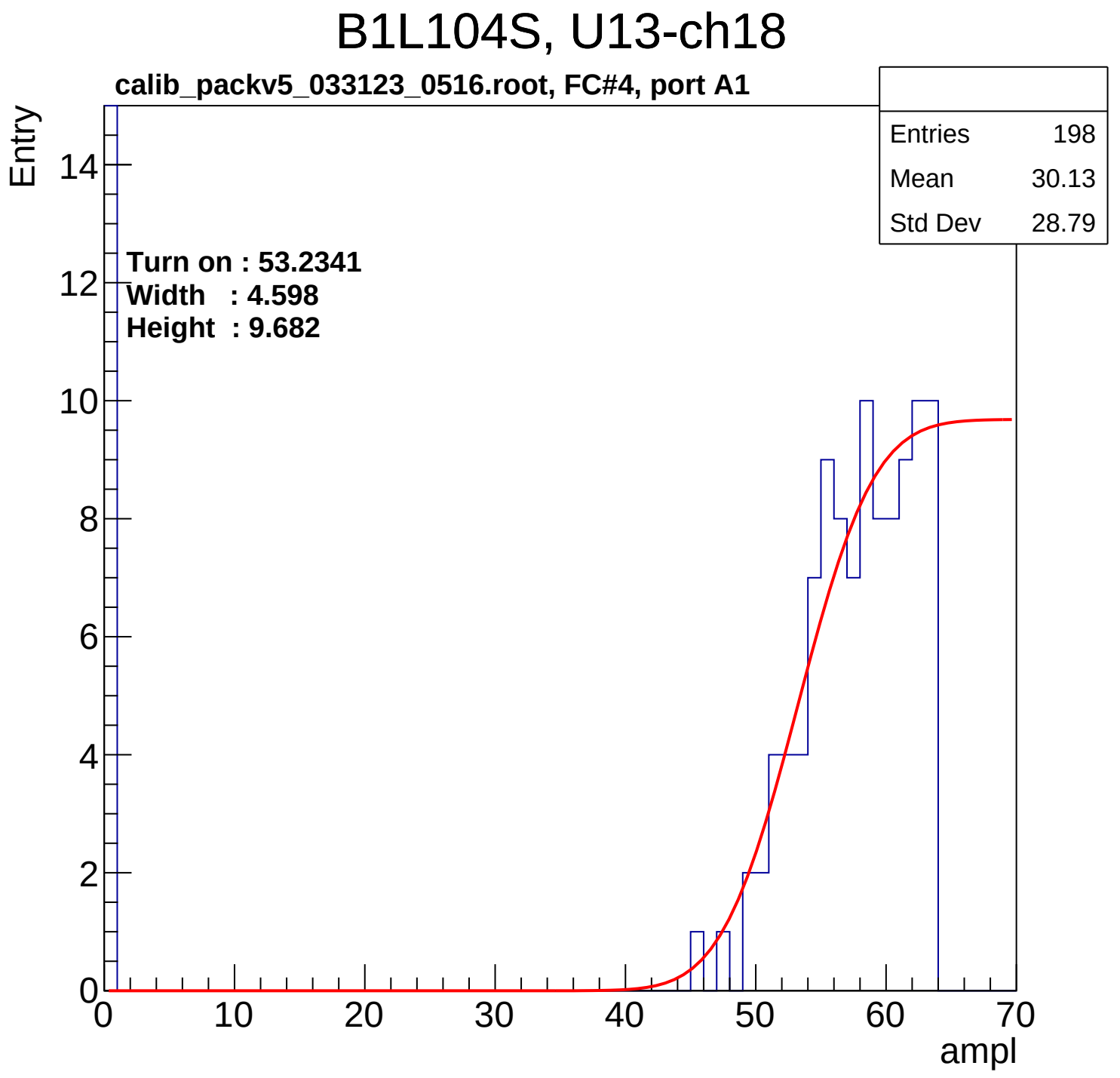
B1L104S, U13-ch18
calib_packv5_033123_0516.root, FC#4, port A1
Entries 198
Mean 30.13
Std Dev 28.79
Turn on : 53.2341
Width : 4.598
Height : 9.682
Entry
ampl
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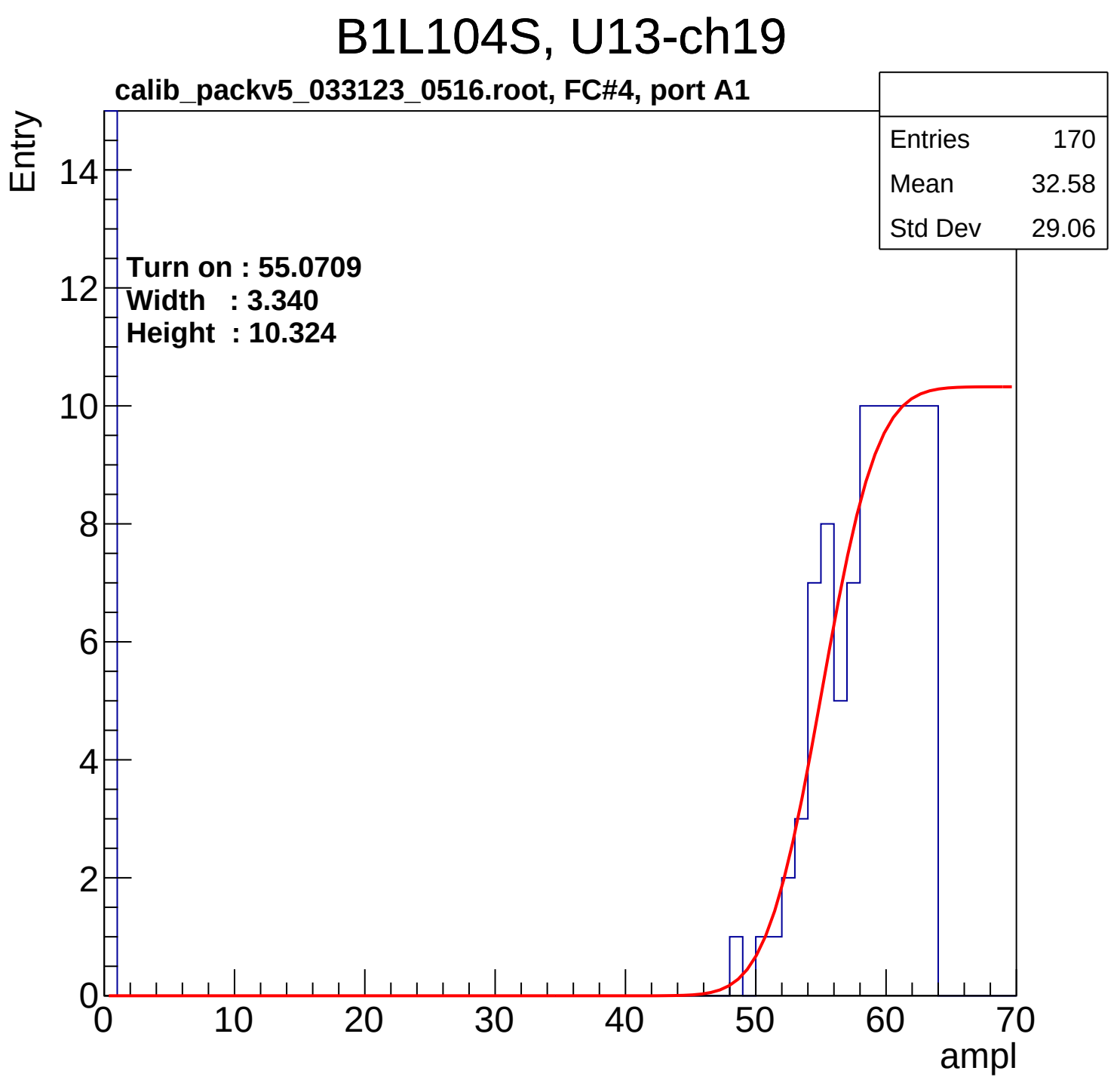
B1L104S, U13-ch19
calib_packv5_033123_0516.root, FC#4, port A1
Entries 170
Mean 32.58
Std Dev 29.06
Turn on : 55.0709
Width : 3.340
Height : 10.324
Entry
ampl
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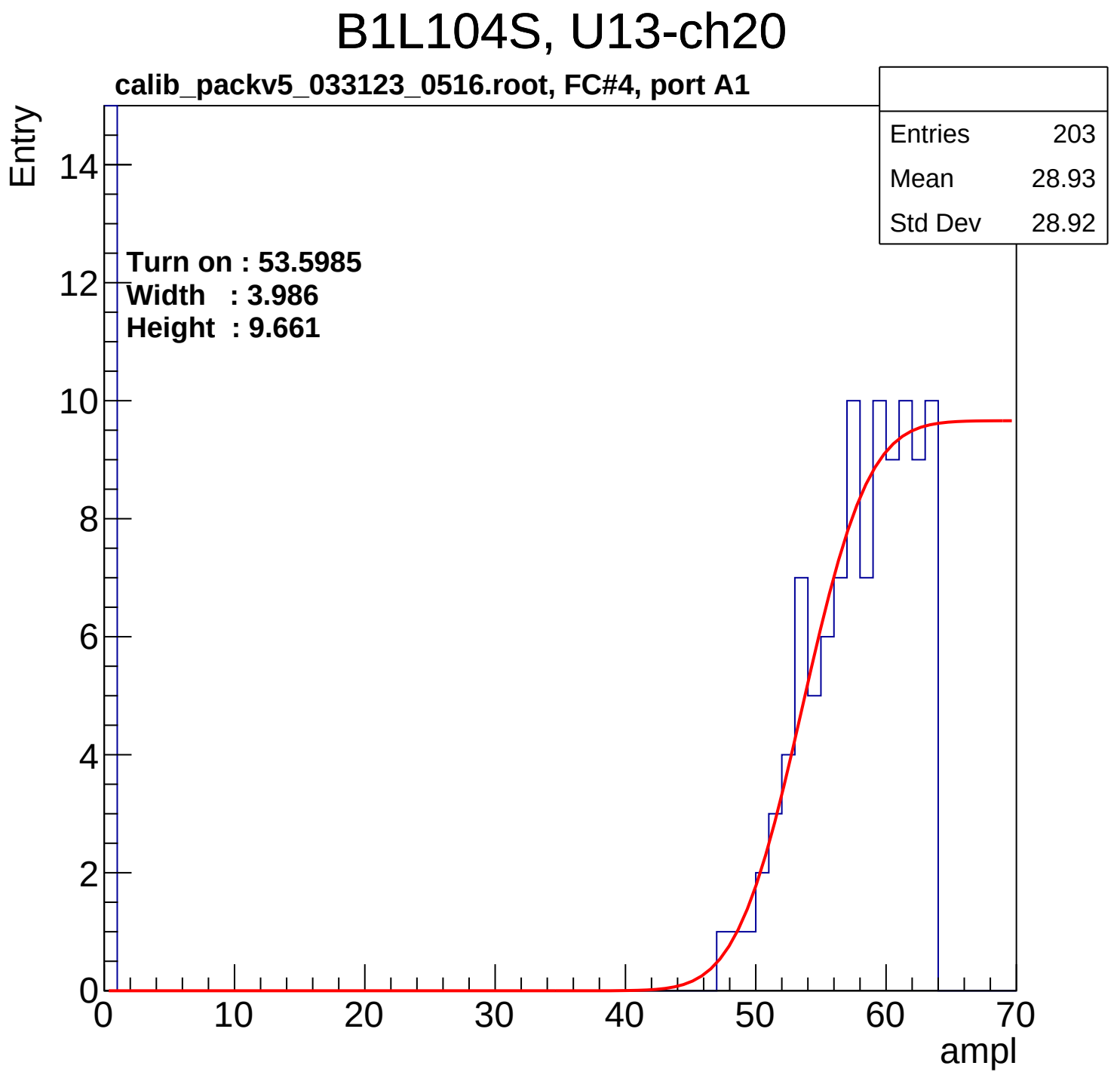
B1L104S, U13-ch20
calib_packv5_033123_0516.root, FC#4, port A1
Entries 203
Mean 28.93
Std Dev 28.92
Turn on : 53.5985
Width : 3.986
Height : 9.661
Entry
ampl
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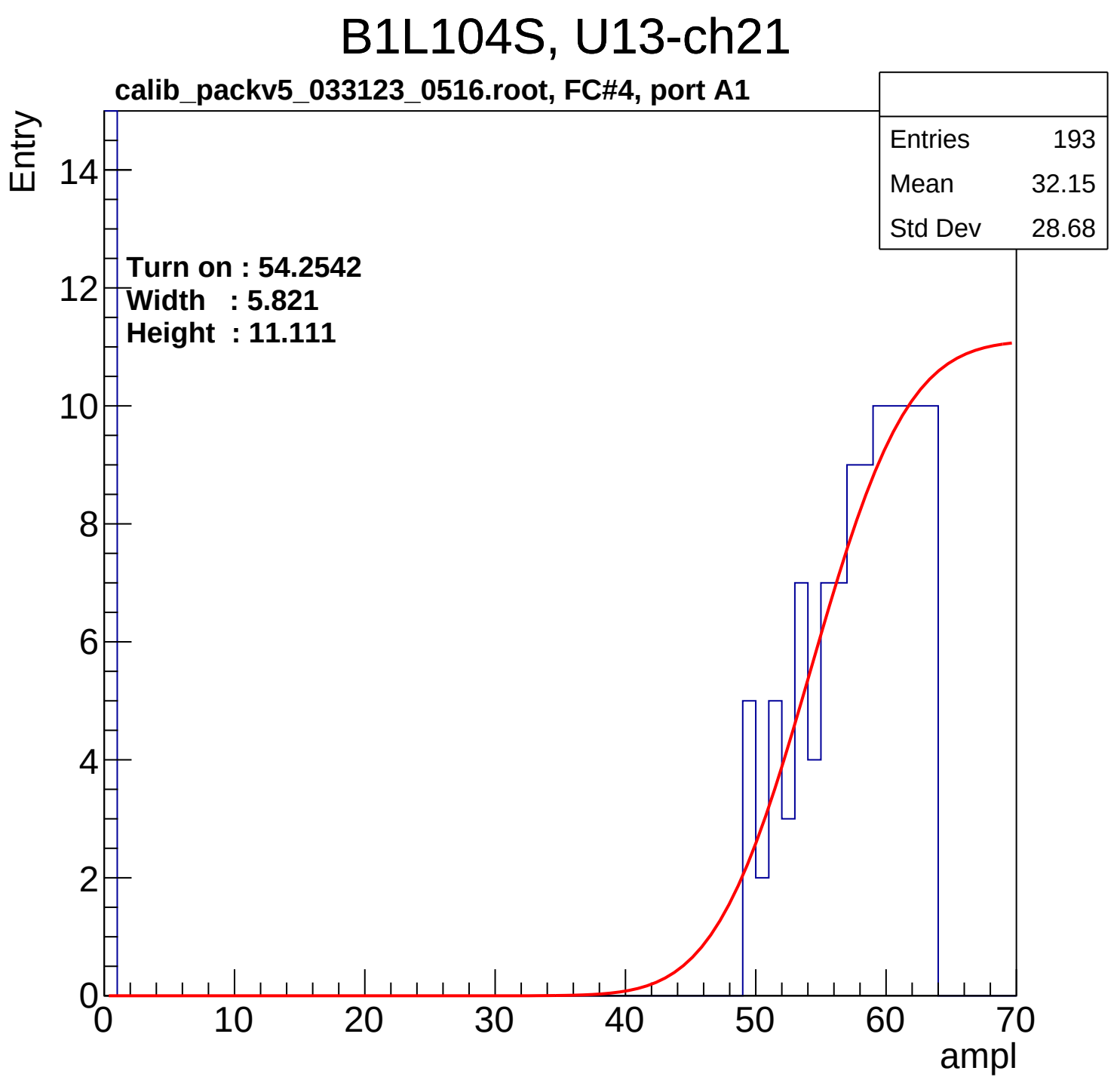
B1L104S, U13-ch21
calib_packv5_033123_0516.root, FC#4, port A1
Entries 193
Mean 32.15
Std Dev 28.68
Turn on : 54.2542
Width : 5.821
Height : 11.111
Entry
ampl
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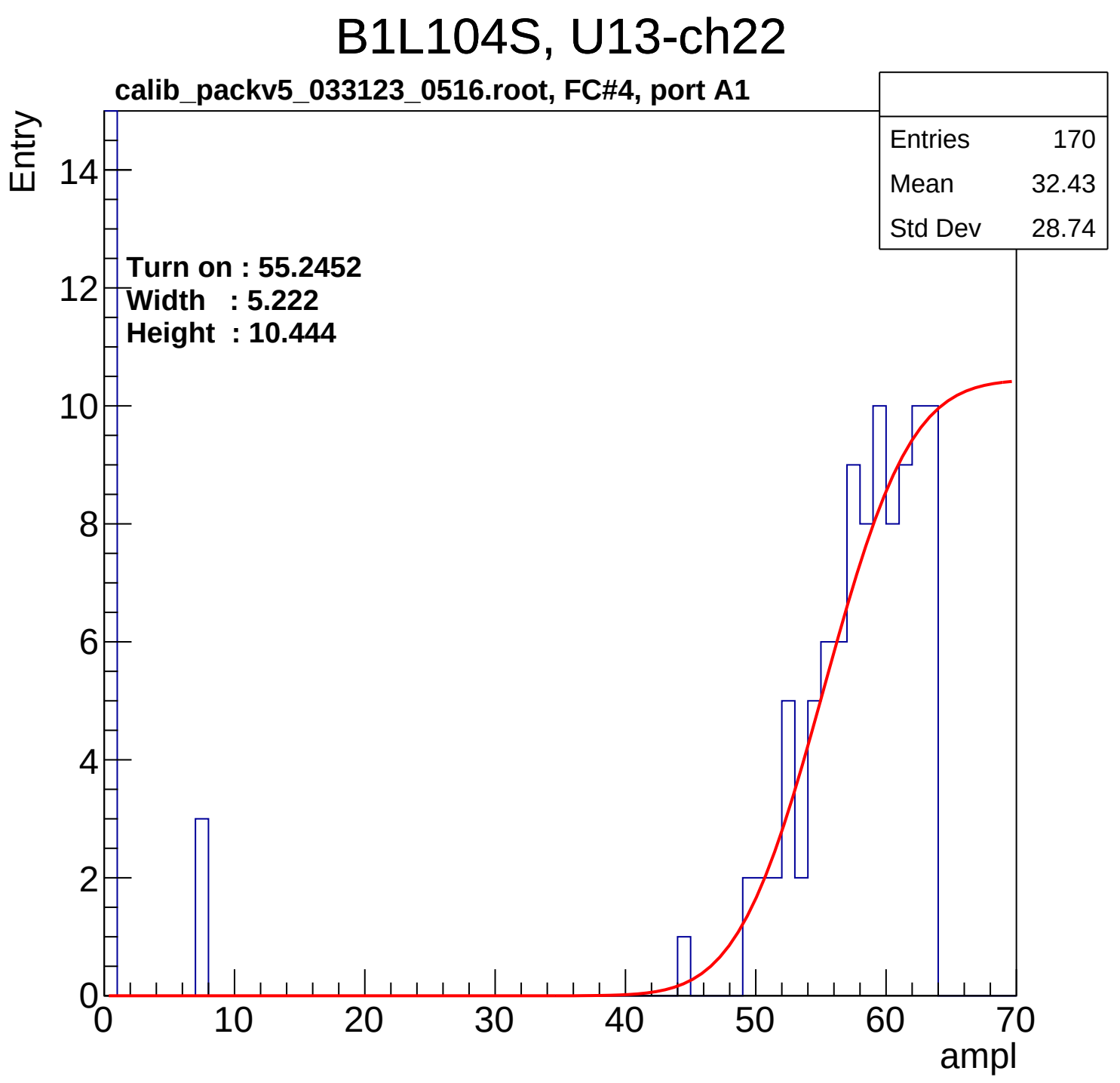
B1L104S, U13-ch22
calib_packv5_033123_0516.root, FC#4, port A1
Entries 170
Mean 32.43
Std Dev 28.74
Turn on : 55.2452
Width : 5.222
Height : 10.444
Entry
ampl
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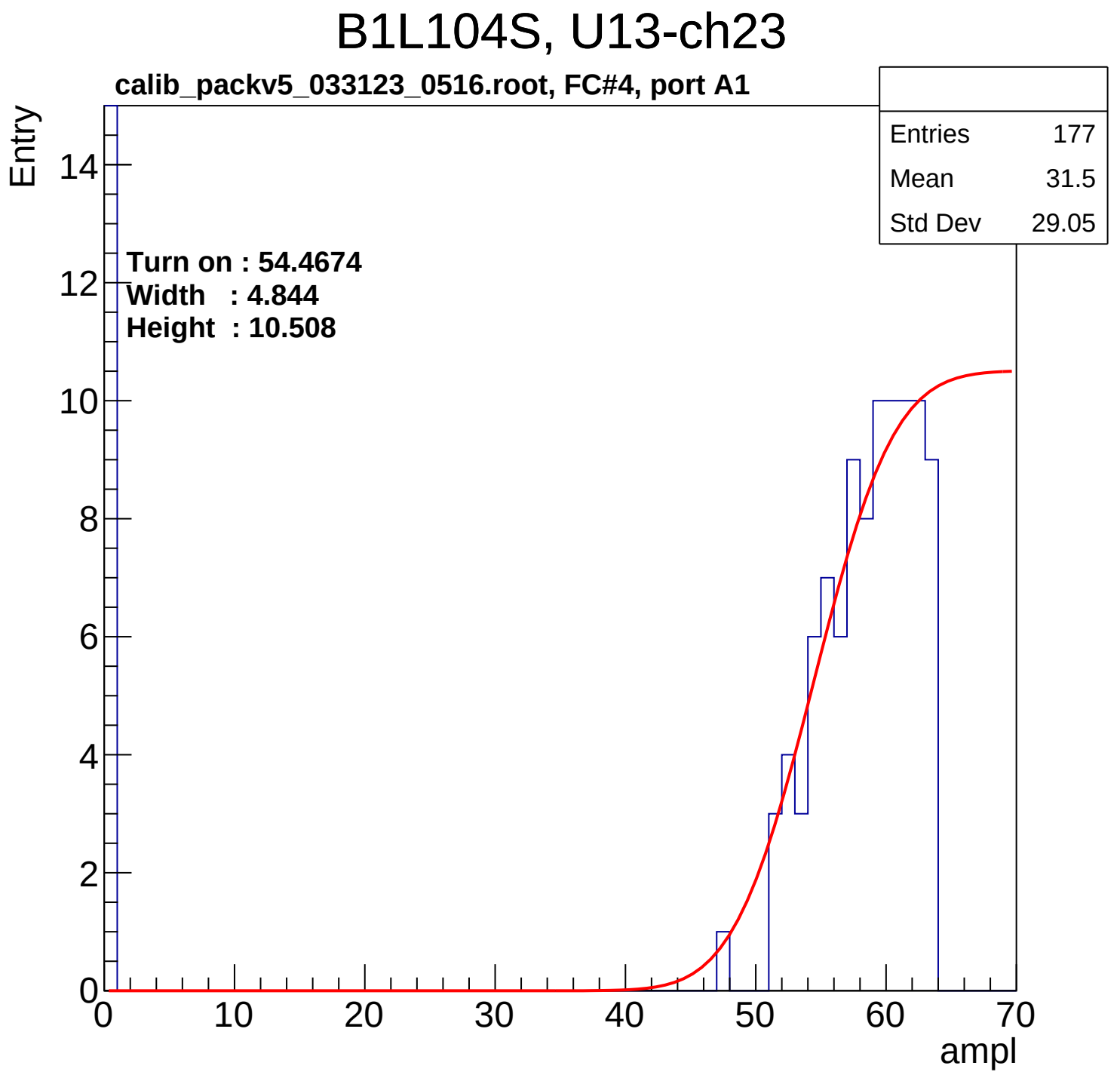
B1L104S, U13-ch23
calib_packv5_033123_0516.root, FC#4, port A1
Entries 177
Mean 31.5
Std Dev 29.05
Turn on : 54.4674
Width : 4.844
Height : 10.508
Entry
ampl
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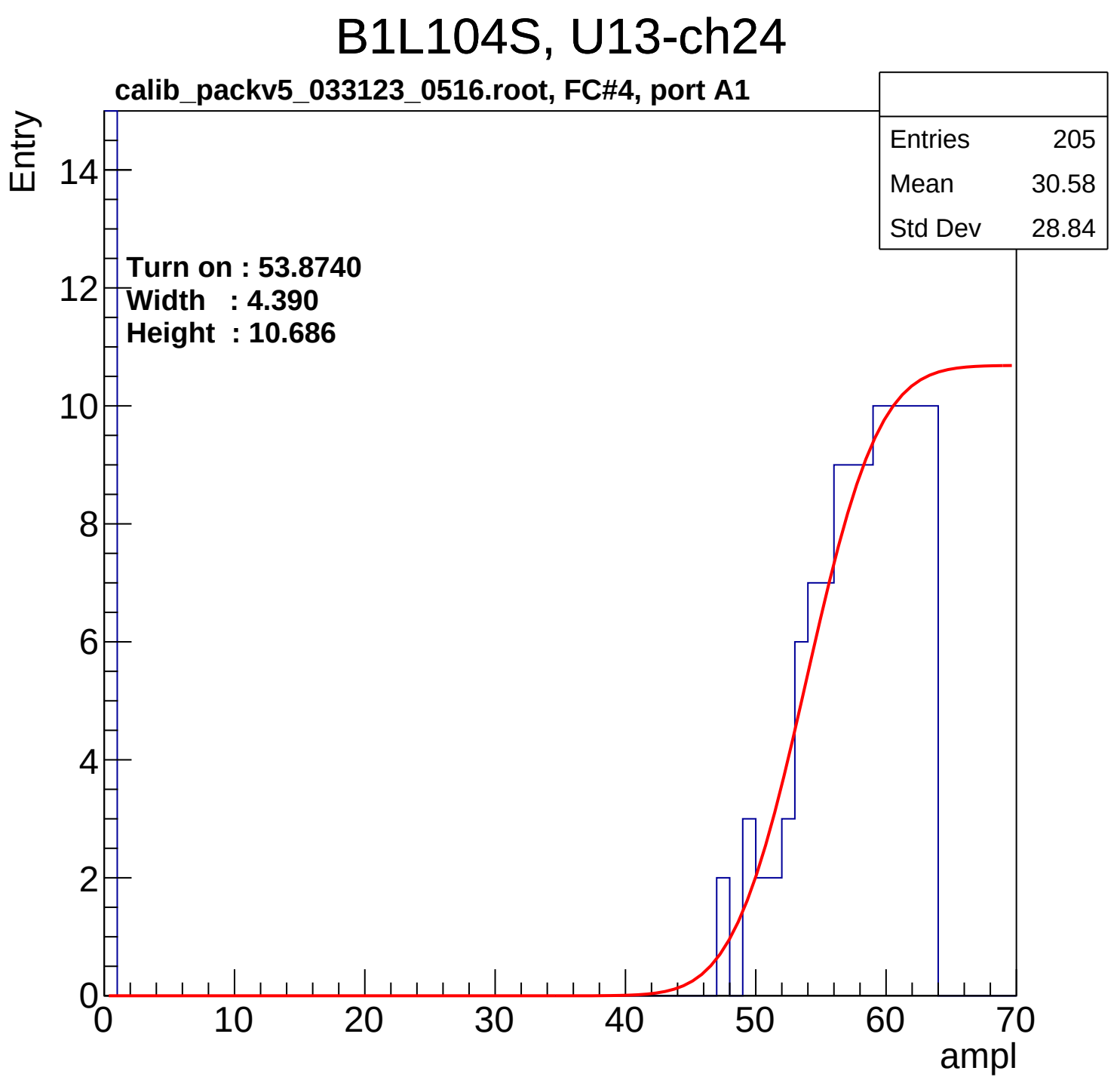
B1L104S, U13-ch24
calib_packv5_033123_0516.root, FC#4, port A1
Entries 205
Mean 30.58
Std Dev 28.84
Turn on : 53.8740
Width : 4.390
Height : 10.686
Entry
ampl
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6
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10
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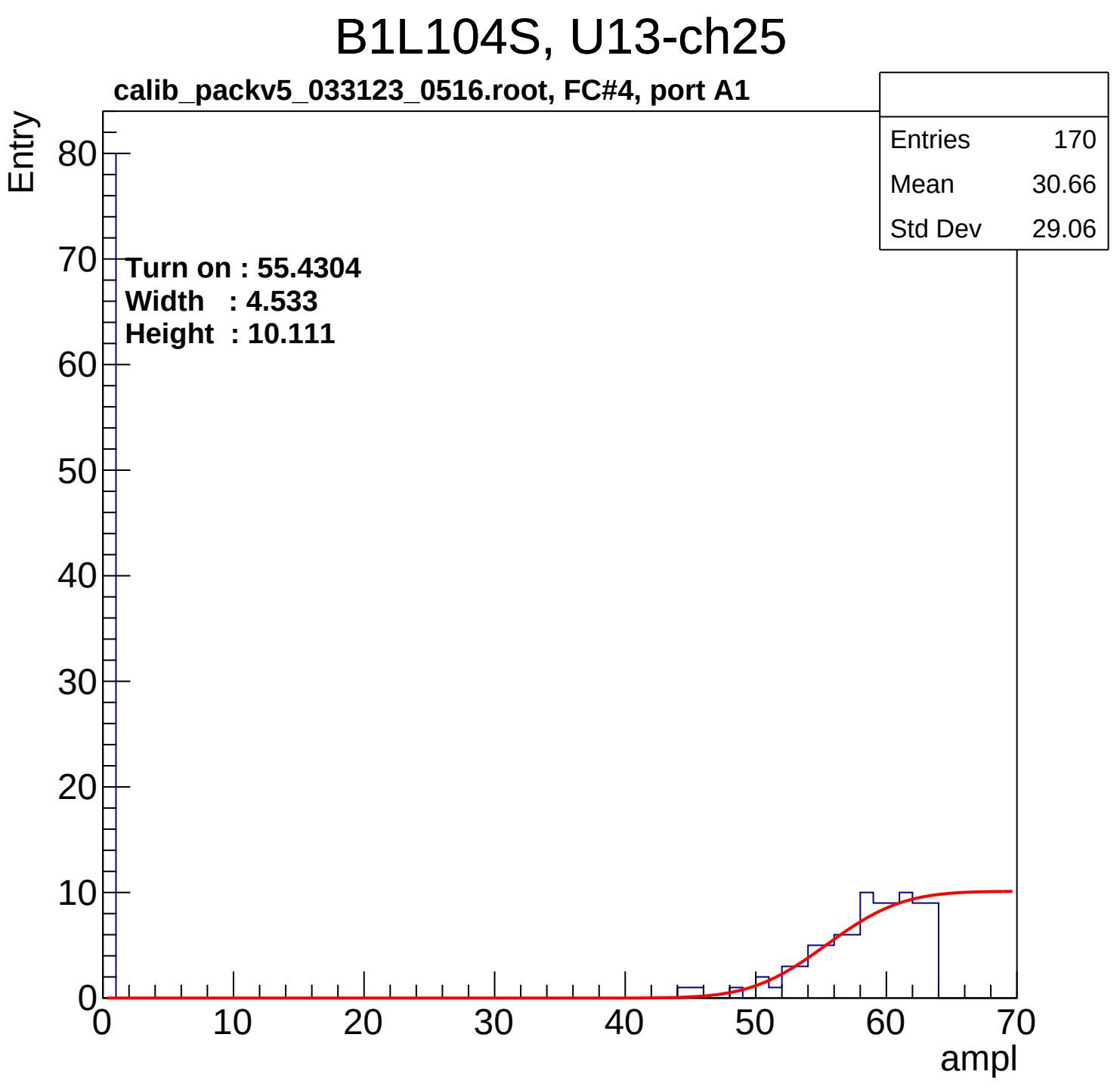
B1L104S, U13-ch25
calib_packv5_033123_0516.root, FC#4, port A1
Entries 170
Mean 30.66
Std Dev 29.06
Turn on : 55.4304
Width : 4.533
Height : 10.111
Entry
ampl
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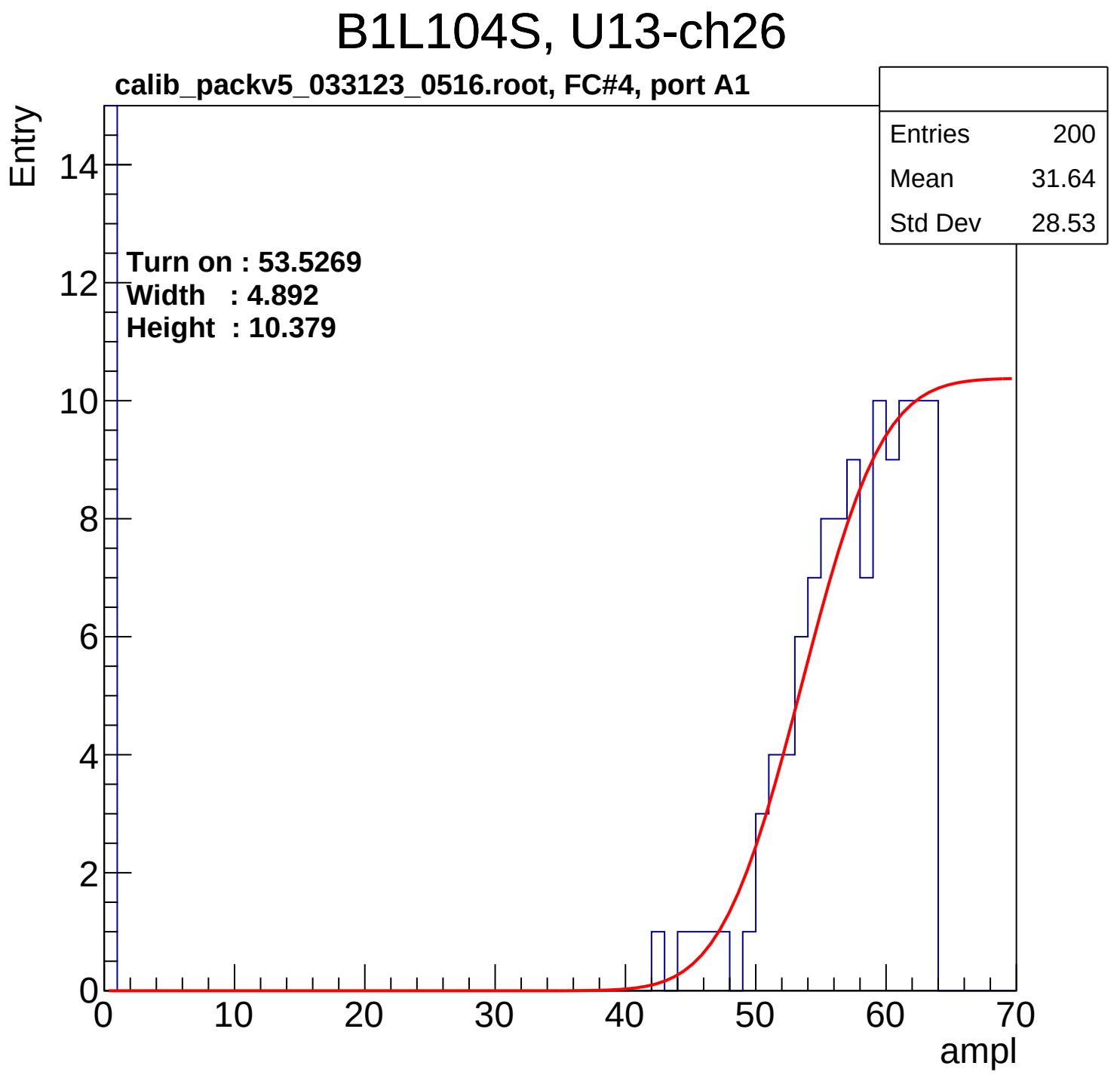
B1L104S, U13-ch26
calib_packv5_033123_0516.root, FC#4, port A1
Entries 200
Mean 31.64
Std Dev 28.53
Turn on : 53.5269
Width : 4.892
Height : 10.379
Entry
ampl
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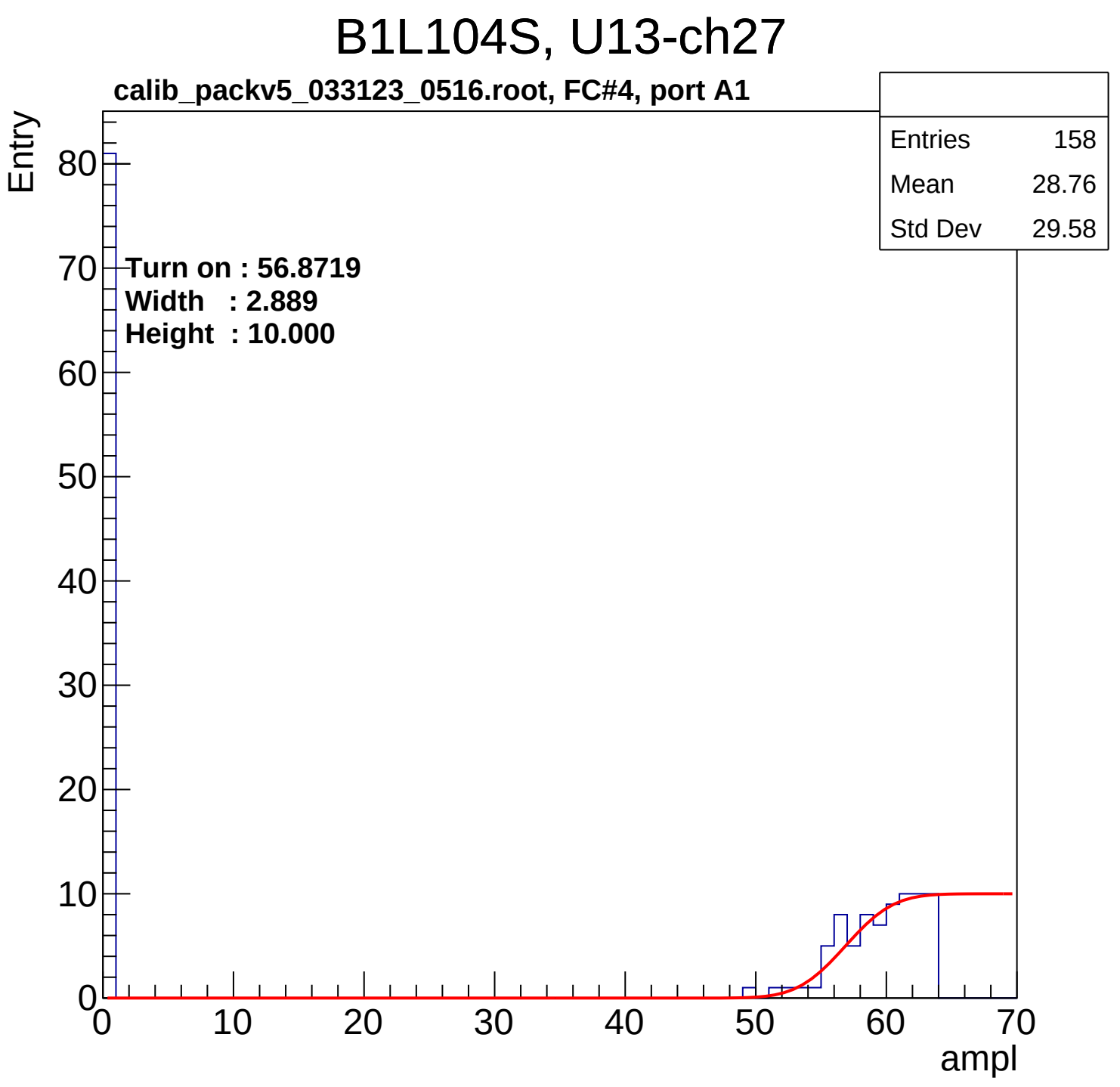
B1L104S, U13-ch27
calib_packv5_033123_0516.root, FC#4, port A1
Entries 158
Mean 28.76
Std Dev 29.58
Turn on : 56.8719
Width : 2.889
Height : 10.000
Entry
ampl
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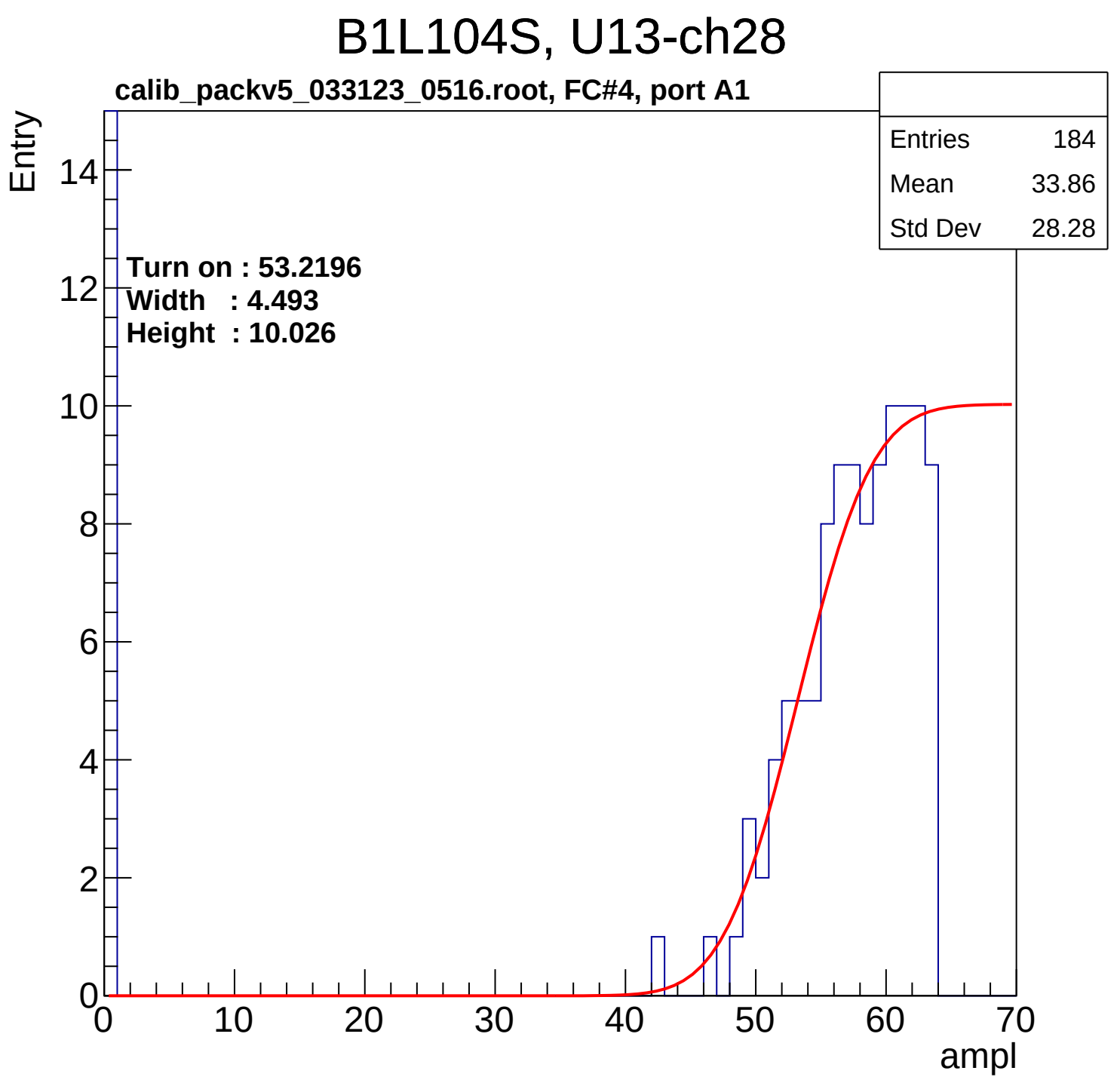
B1L104S, U13-ch28
calib_packv5_033123_0516.root, FC#4, port A1
Entries 184
Mean 33.86
Std Dev 28.28
Turn on : 53.2196
Width : 4.493
Height : 10.026
Entry
ampl
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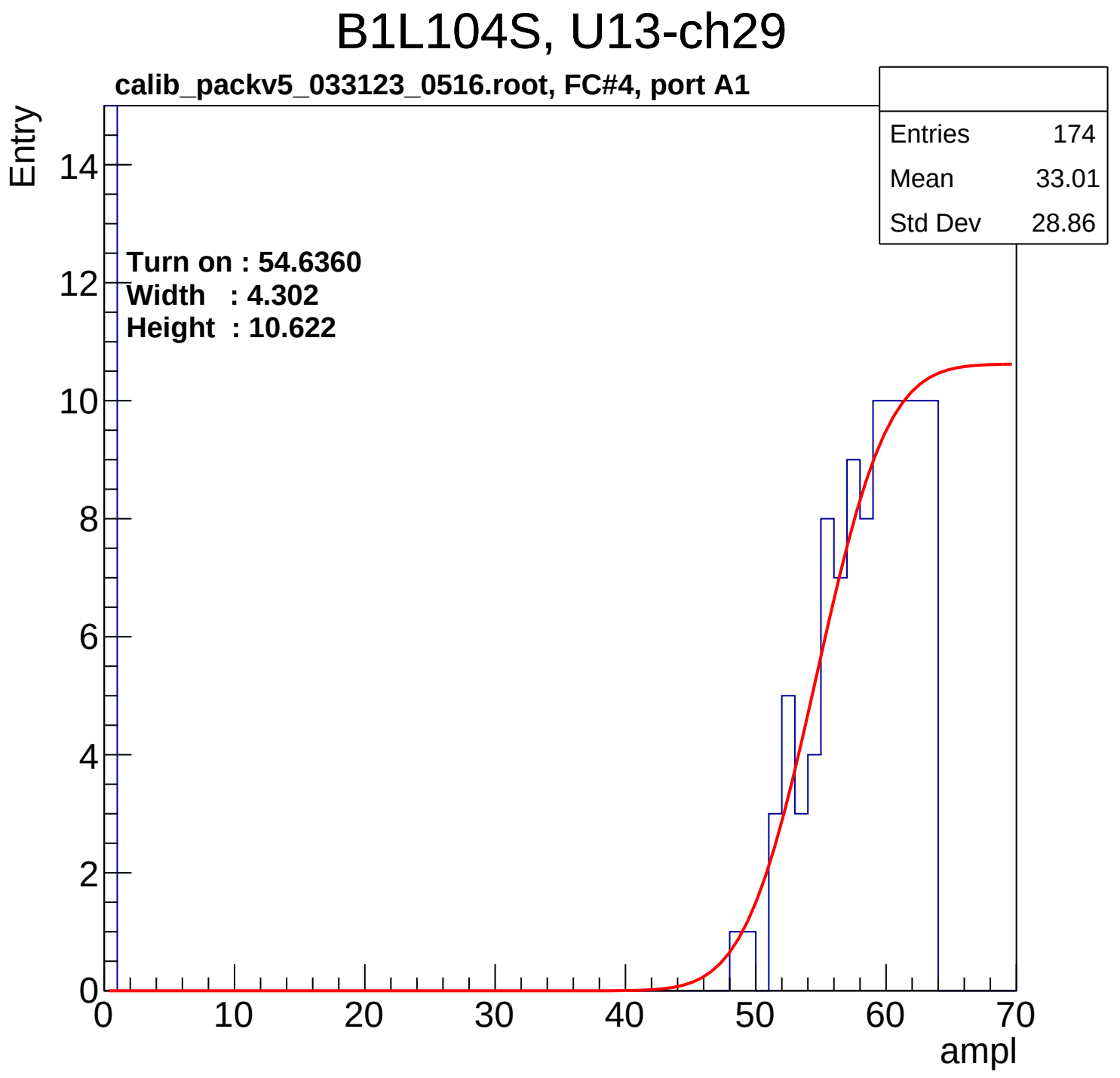
B1L104S, U13-ch29
calib_packv5_033123_0516.root, FC#4, port A1
Entries 174
Mean 33.01
Std Dev 28.86
Turn on : 54.6360
Width : 4.302
Height : 10.622
Entry
ampl
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4
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8
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0
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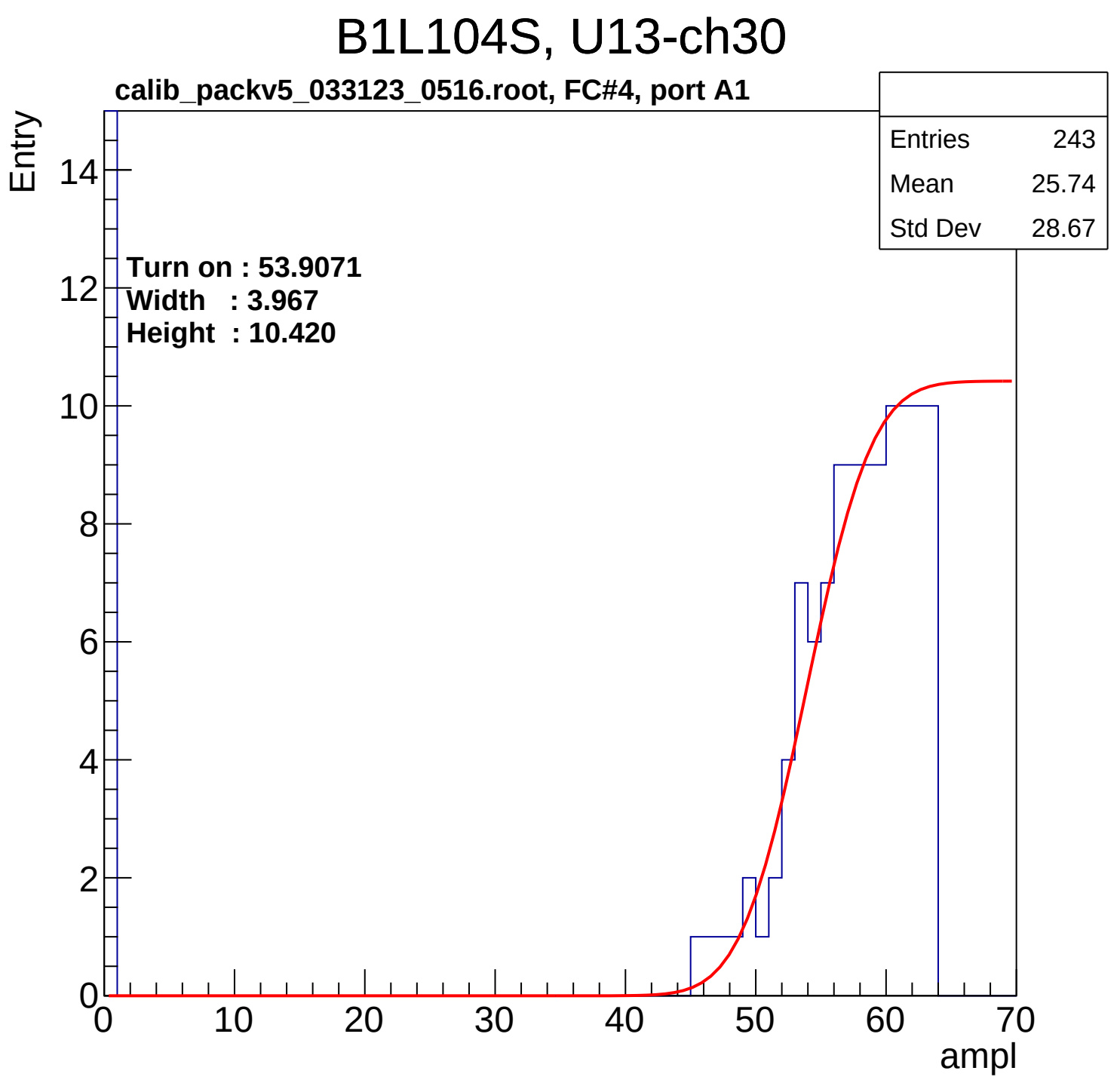
B1L104S, U13-ch30
calib_packv5_033123_0516.root, FC#4, port A1
Entries 243
Mean 25.74
Std Dev 28.67
Turn on : 53.9071
Width : 3.967
Height : 10.420
Entry
ampl
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2
4
6
8
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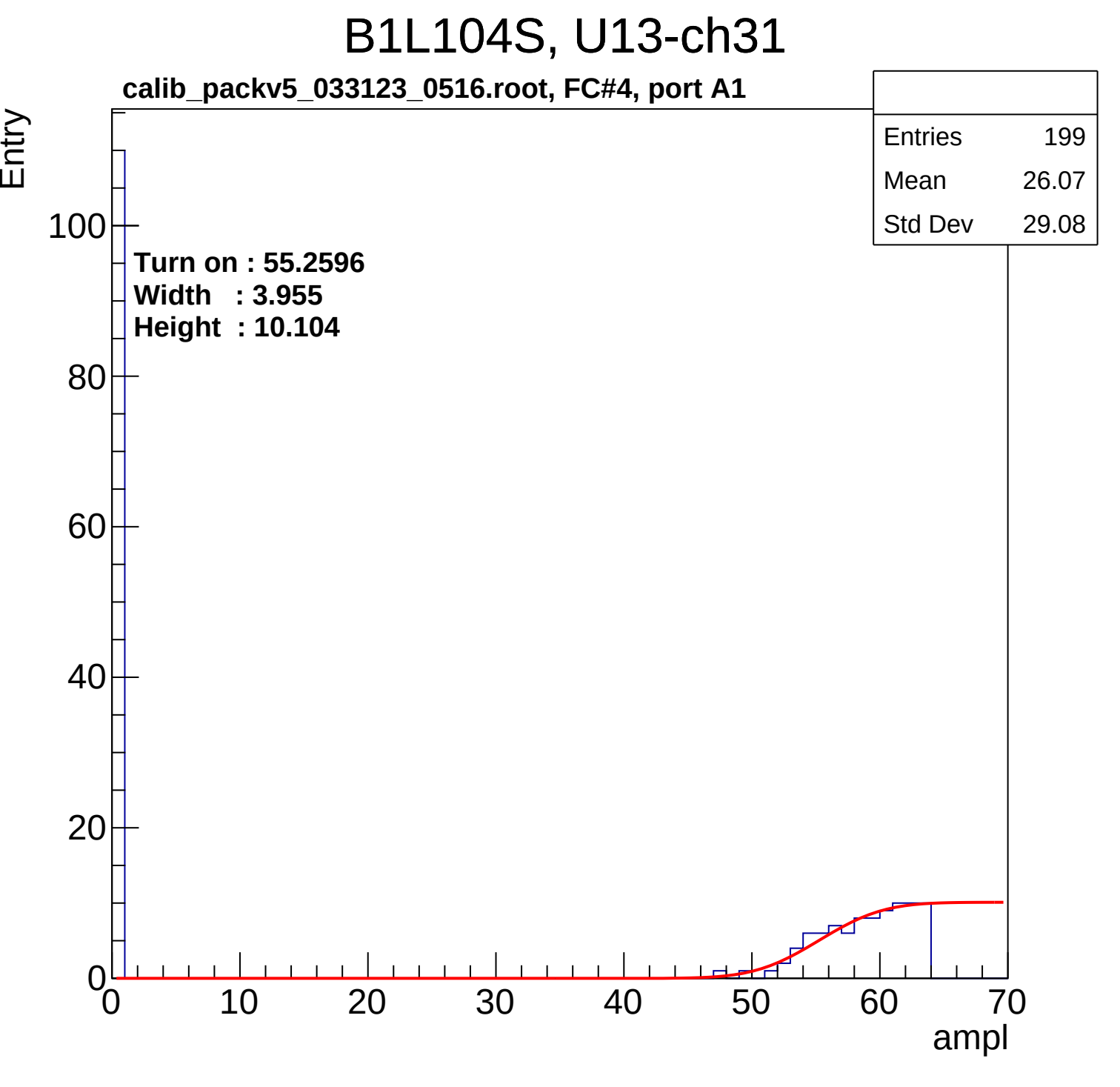
B1L104S, U13-ch31
calib_packv5_033123_0516.root, FC#4, port A1
Entries 199
Mean 26.07
Std Dev 29.08
Turn on : 55.2596
Width : 3.955
Height : 10.104
Entry
ampl
0
20
40
60
80
100
0
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40
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60
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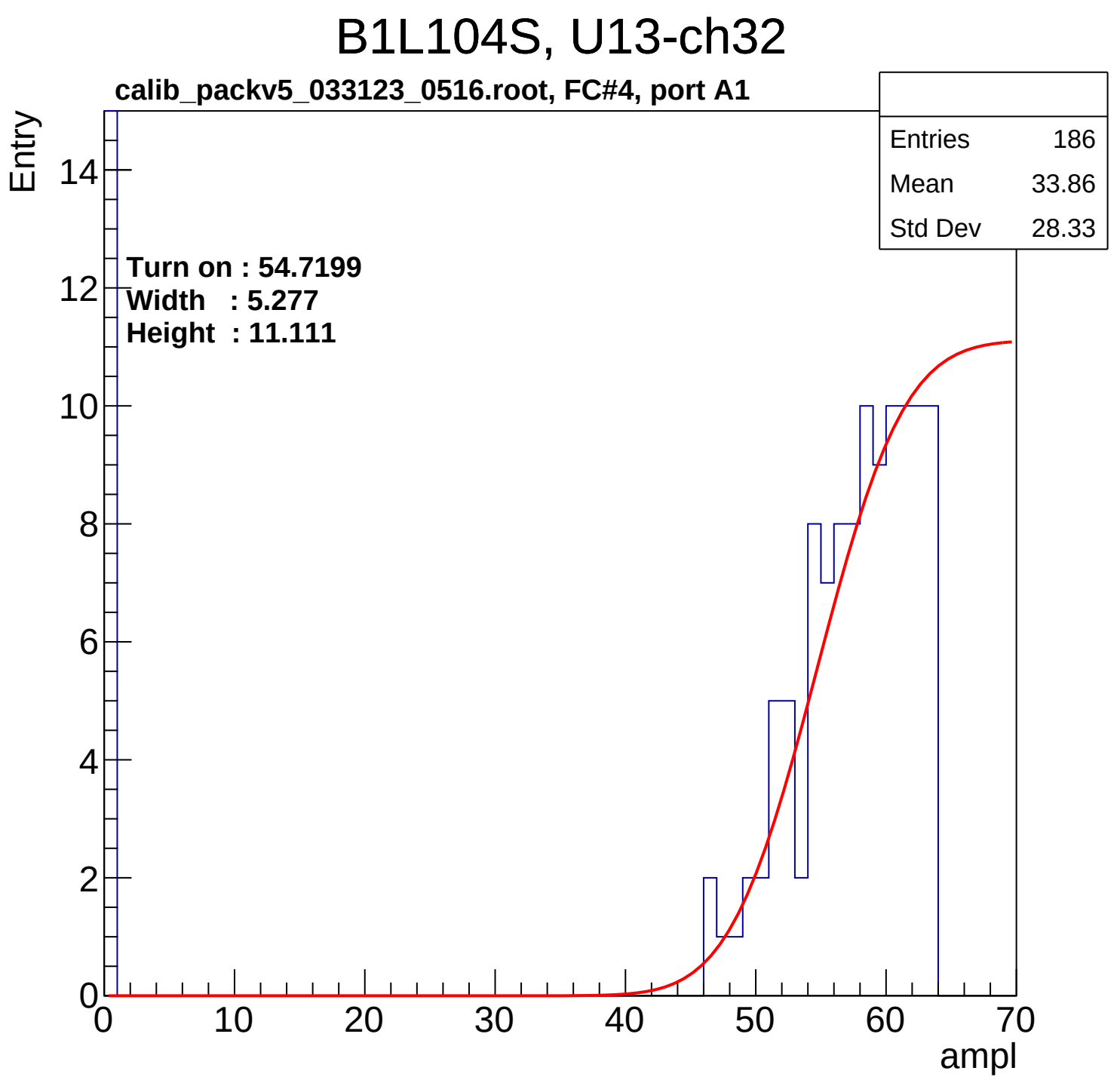
B1L104S, U13-ch32
calib_packv5_033123_0516.root, FC#4, port A1
Entries 186
Mean 33.86
Std Dev 28.33
Turn on : 54.7199
Width : 5.277
Height : 11.111
Entry
ampl
0
2
4
6
8
10
12
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0
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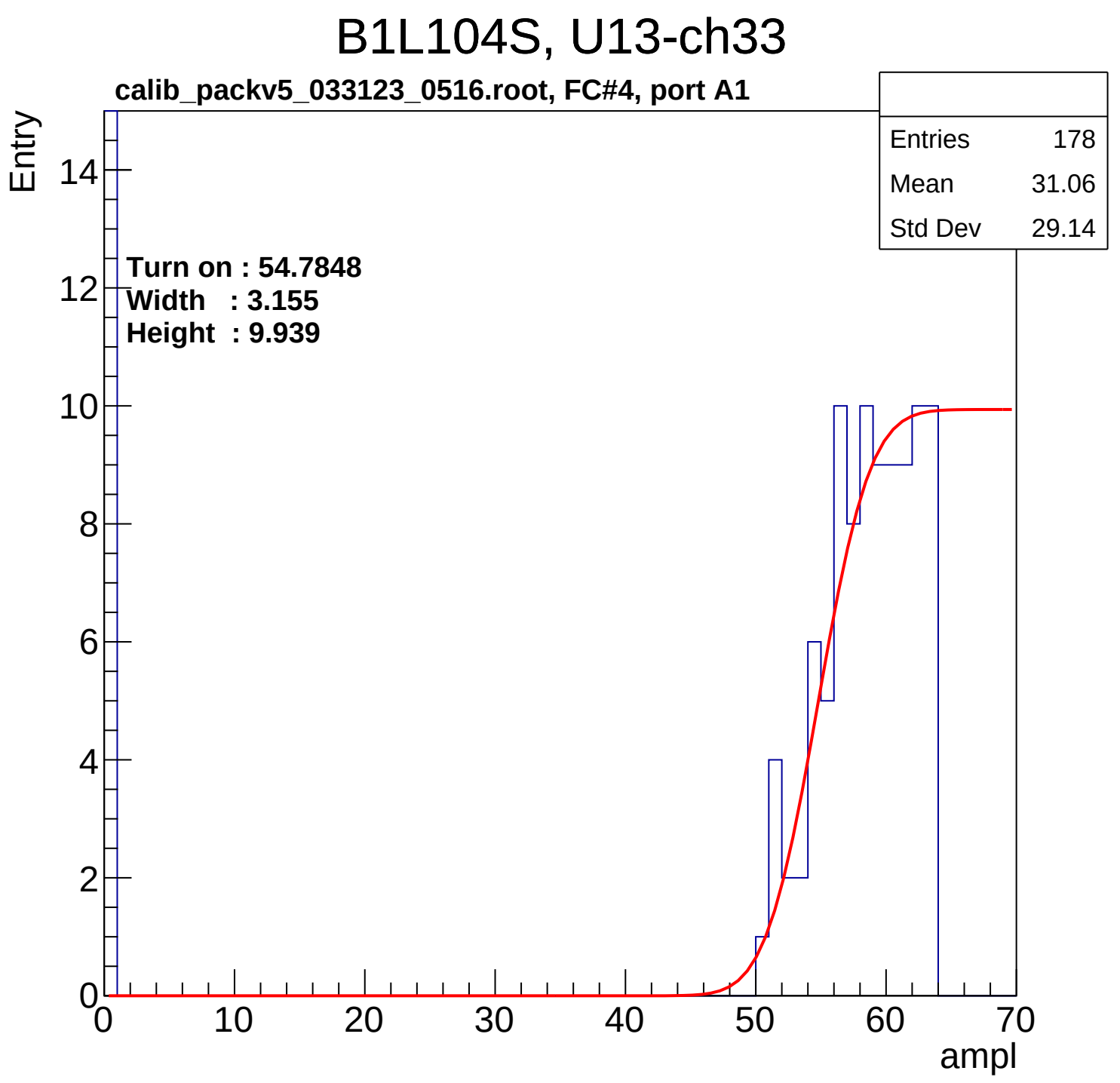
B1L104S, U13-ch33
calib_packv5_033123_0516.root, FC#4, port A1
Entries 178
Mean 31.06
Std Dev 29.14
Turn on : 54.7848
Width : 3.155
Height : 9.939
Entry
ampl
0
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4
6
8
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0
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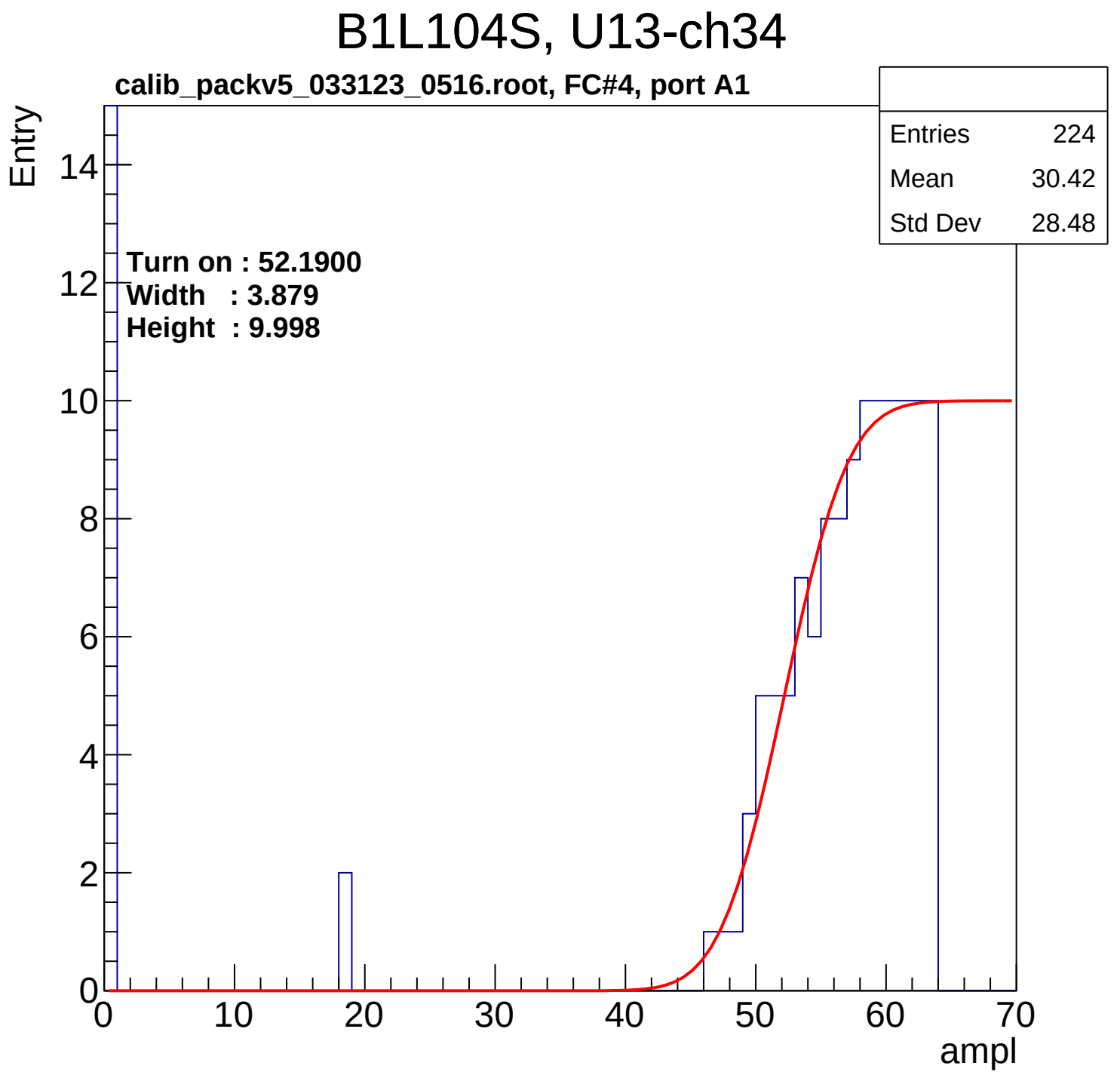
B1L104S, U13-ch34
calib_packv5_033123_0516.root, FC#4, port A1
Entries 224
Mean 30.42
Std Dev 28.48
Turn on : 52.1900
Width : 3.879
Height : 9.998
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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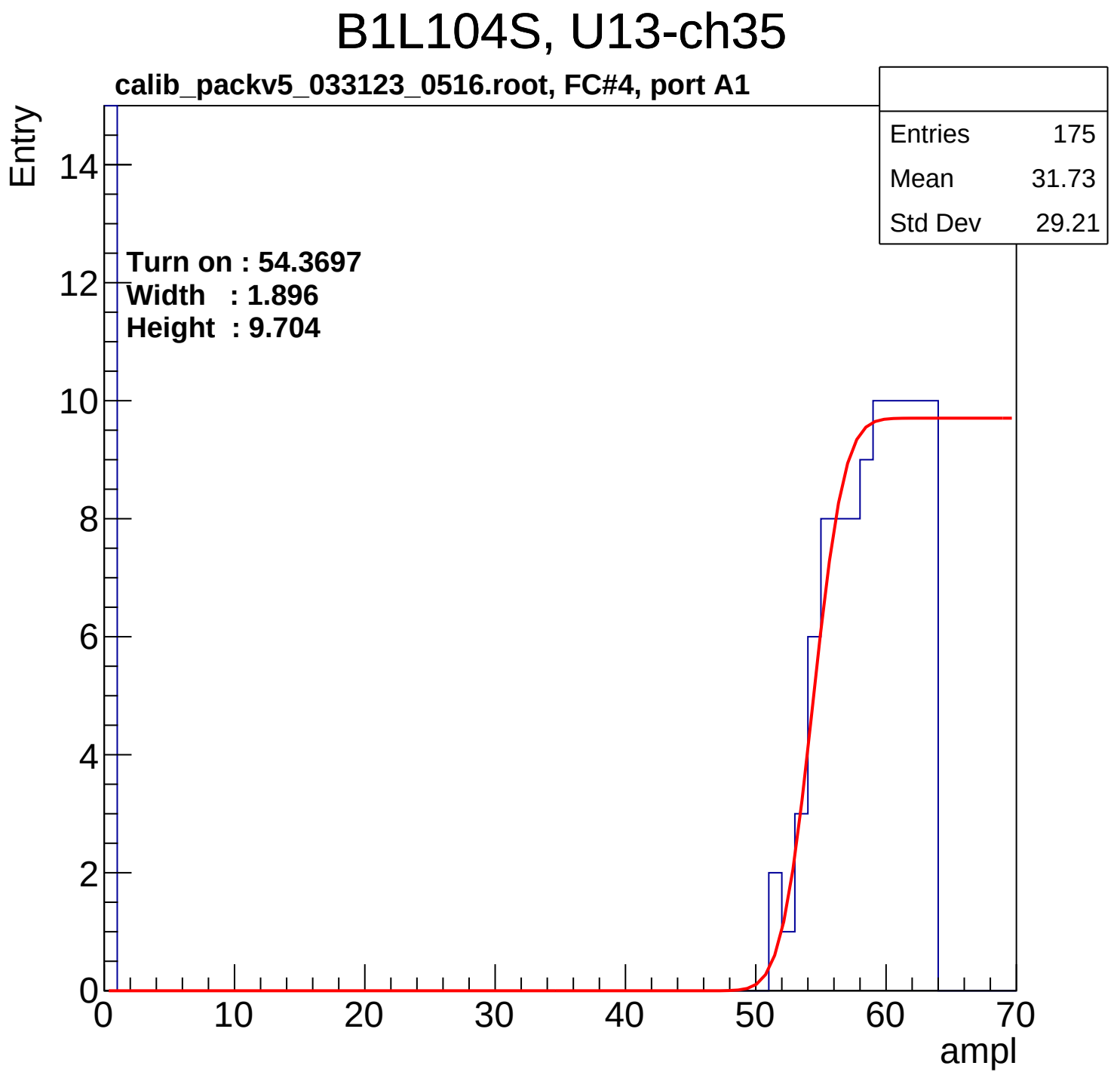
B1L104S, U13-ch35
calib_packv5_033123_0516.root, FC#4, port A1
Entries 175
Mean 31.73
Std Dev 29.21
Turn on : 54.3697
Width : 1.896
Height : 9.704
Entry
ampl
0
2
4
6
8
10
12
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0
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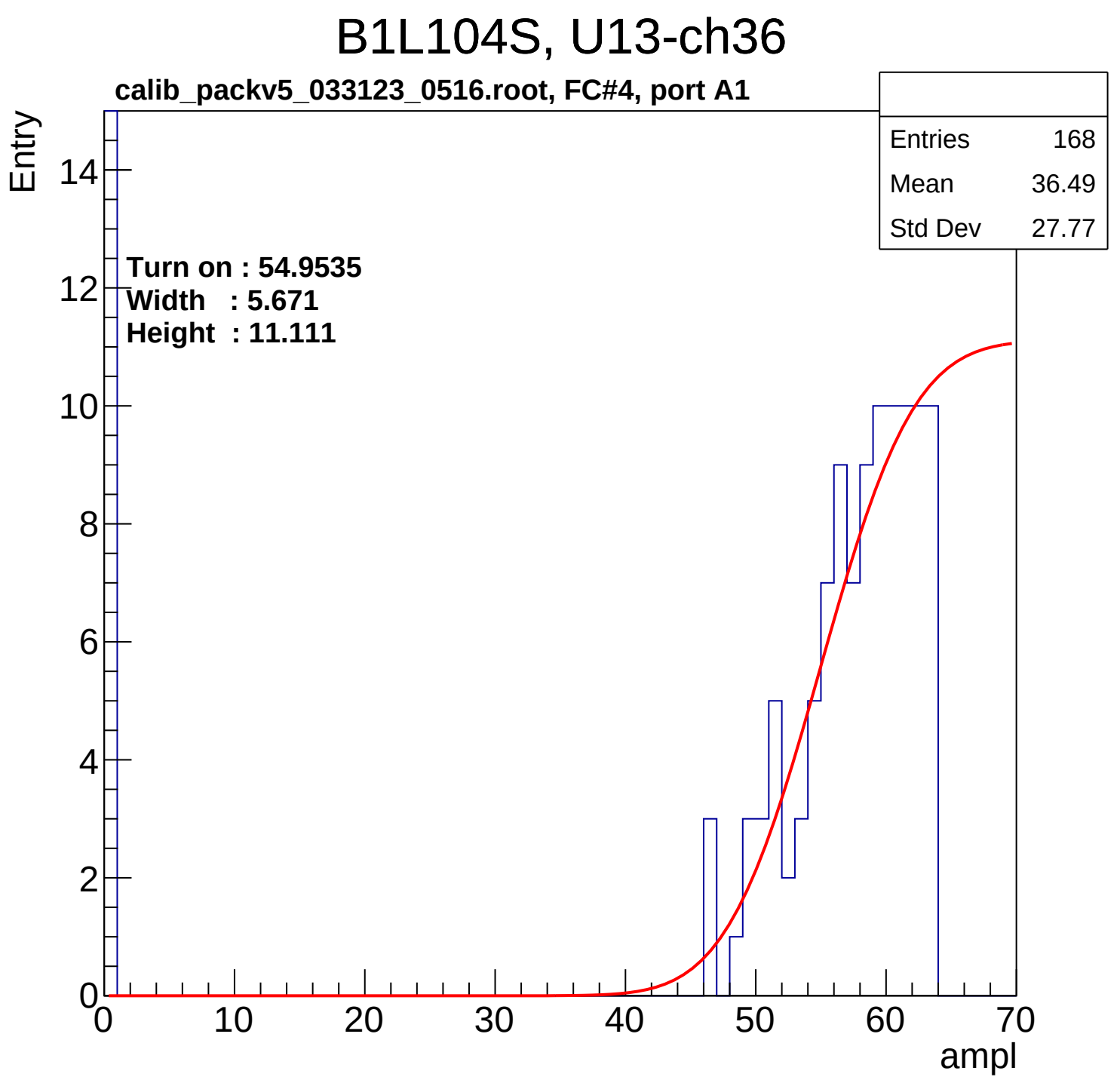
B1L104S, U13-ch36
calib_packv5_033123_0516.root, FC#4, port A1
Entries 168
Mean 36.49
Std Dev 27.77
Turn on : 54.9535
Width : 5.671
Height : 11.111
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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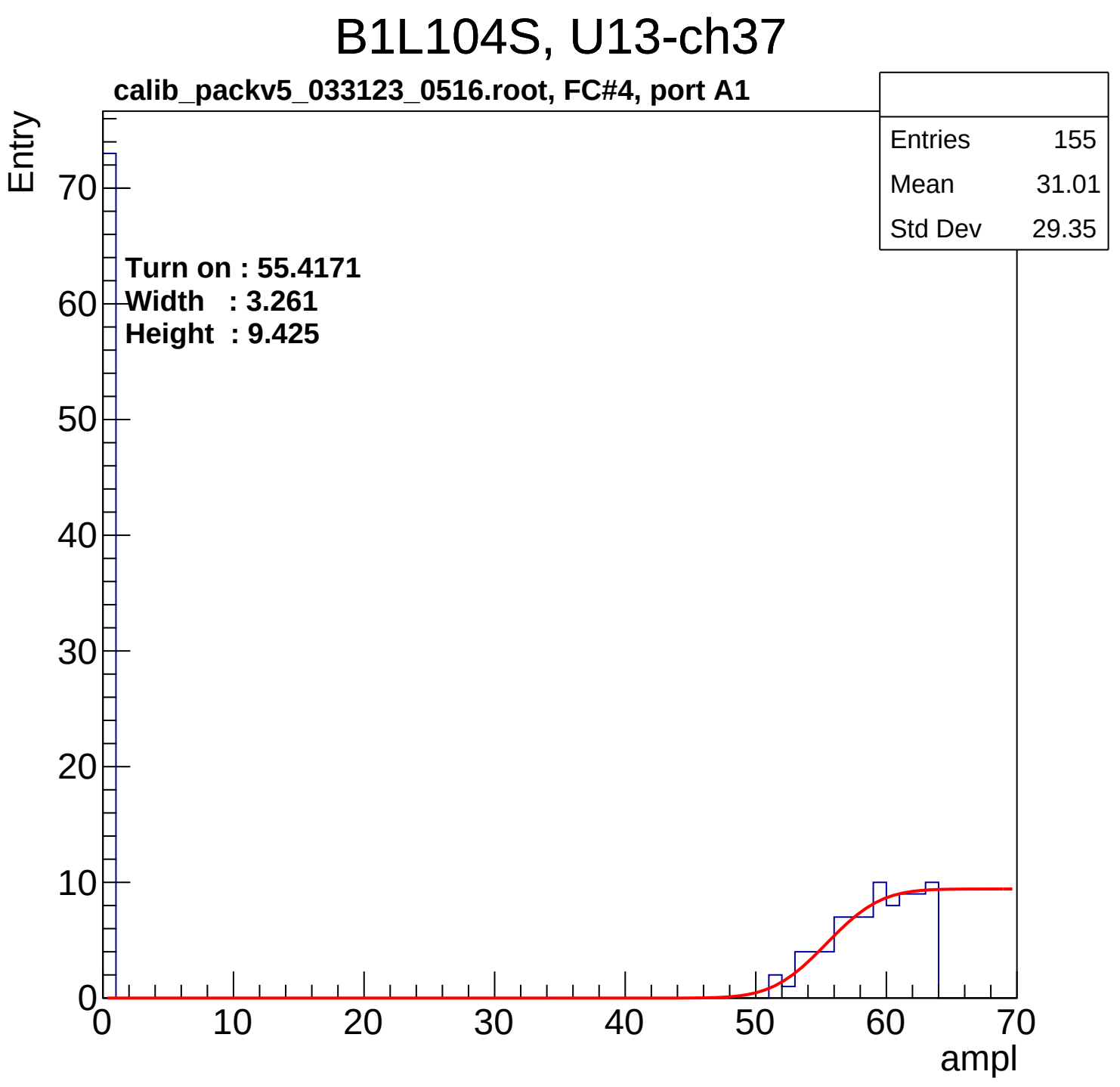
B1L104S, U13-ch37
calib_packv5_033123_0516.root, FC#4, port A1
Entries 155
Mean 31.01
Std Dev 29.35
Turn on : 55.4171
Width : 3.261
Height : 9.425
Entry
ampl
0
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40
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60
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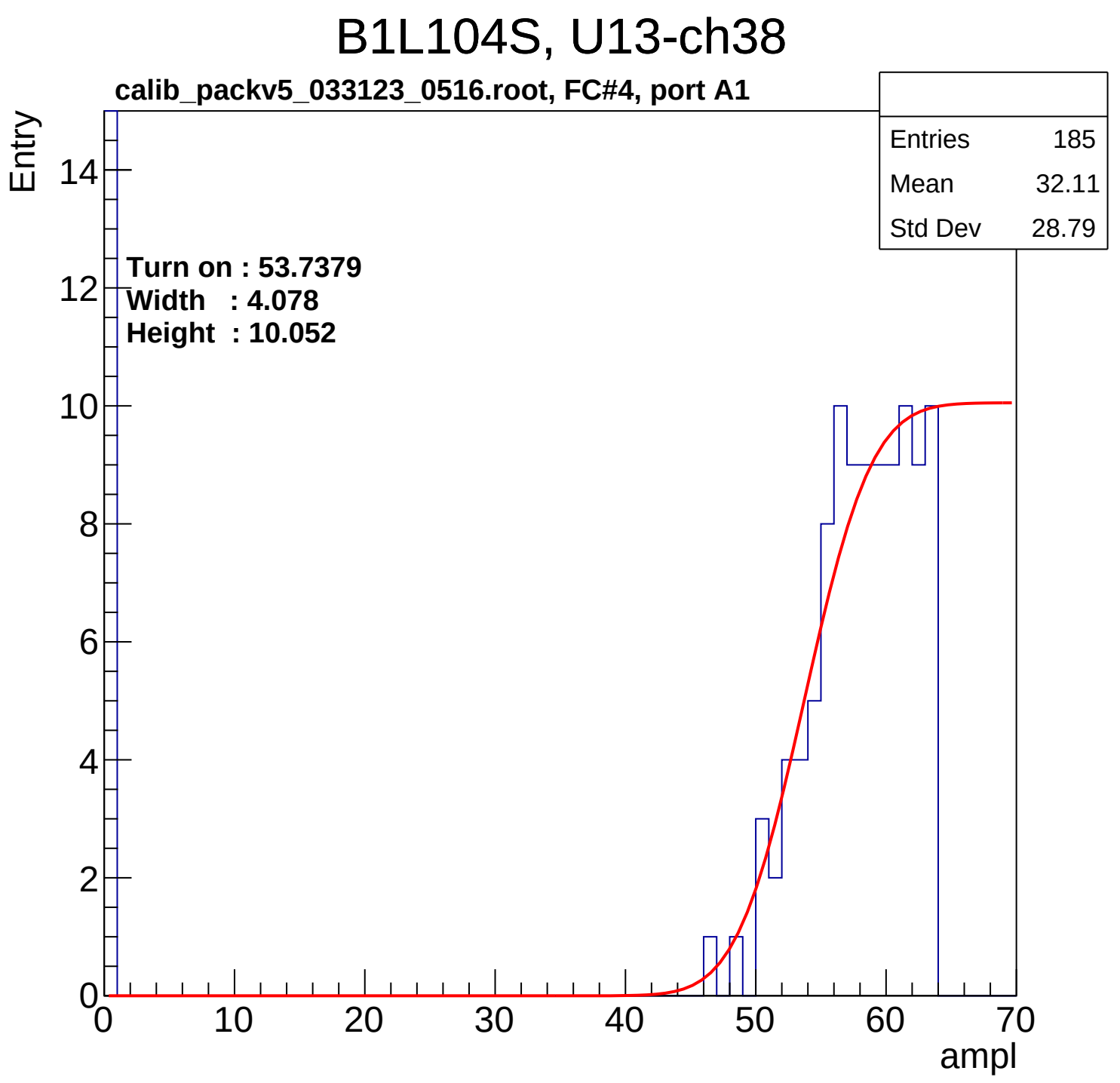
B1L104S, U13-ch38
calib_packv5_033123_0516.root, FC#4, port A1
Entries 185
Mean 32.11
Std Dev 28.79
Turn on : 53.7379
Width : 4.078
Height : 10.052
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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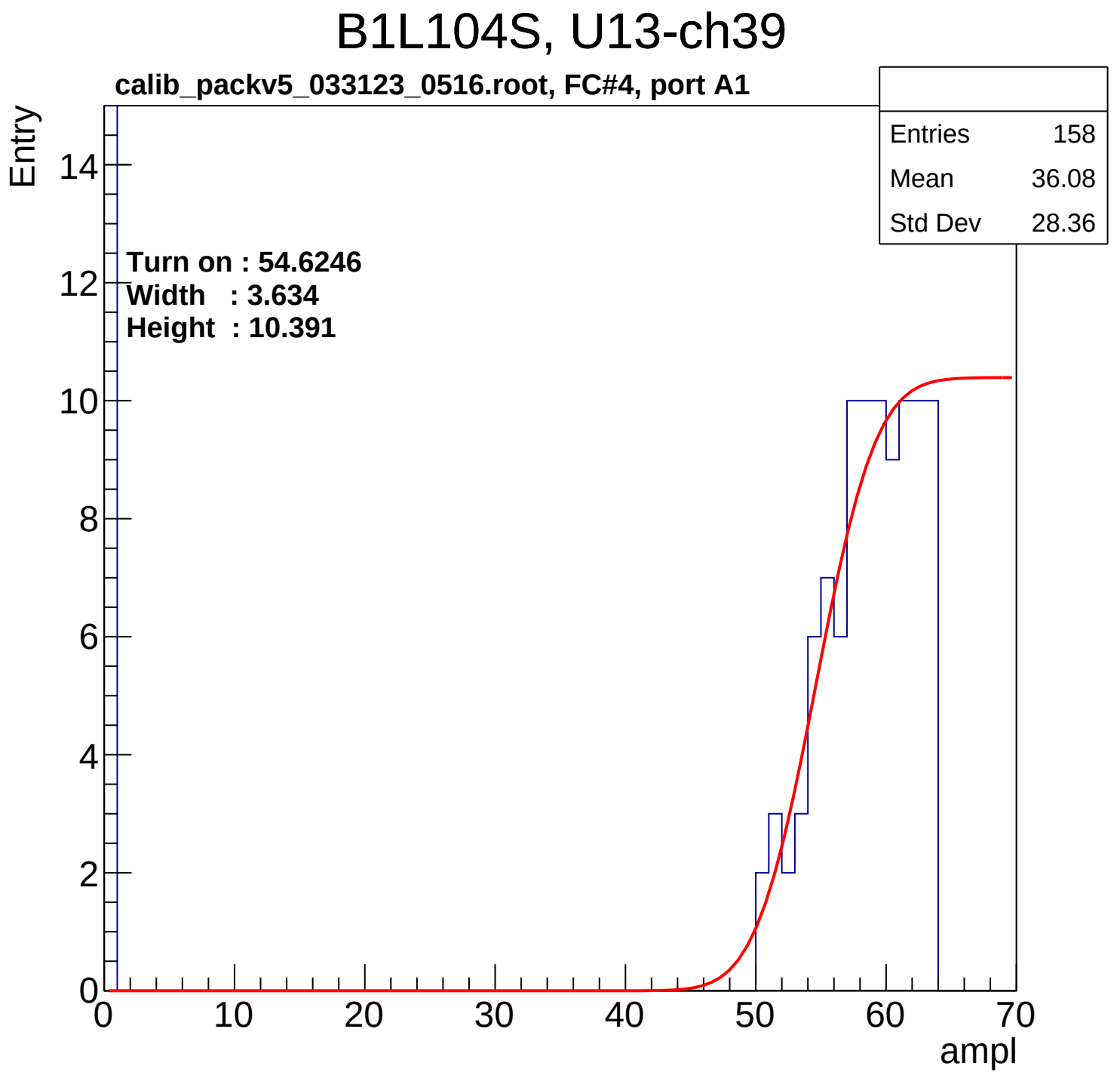
B1L104S, U13-ch39
calib_packv5_033123_0516.root, FC#4, port A1
Entries 158
Mean 36.08
Std Dev 28.36
Turn on : 54.6246
Width : 3.634
Height : 10.391
Entry
ampl
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2
4
6
8
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0
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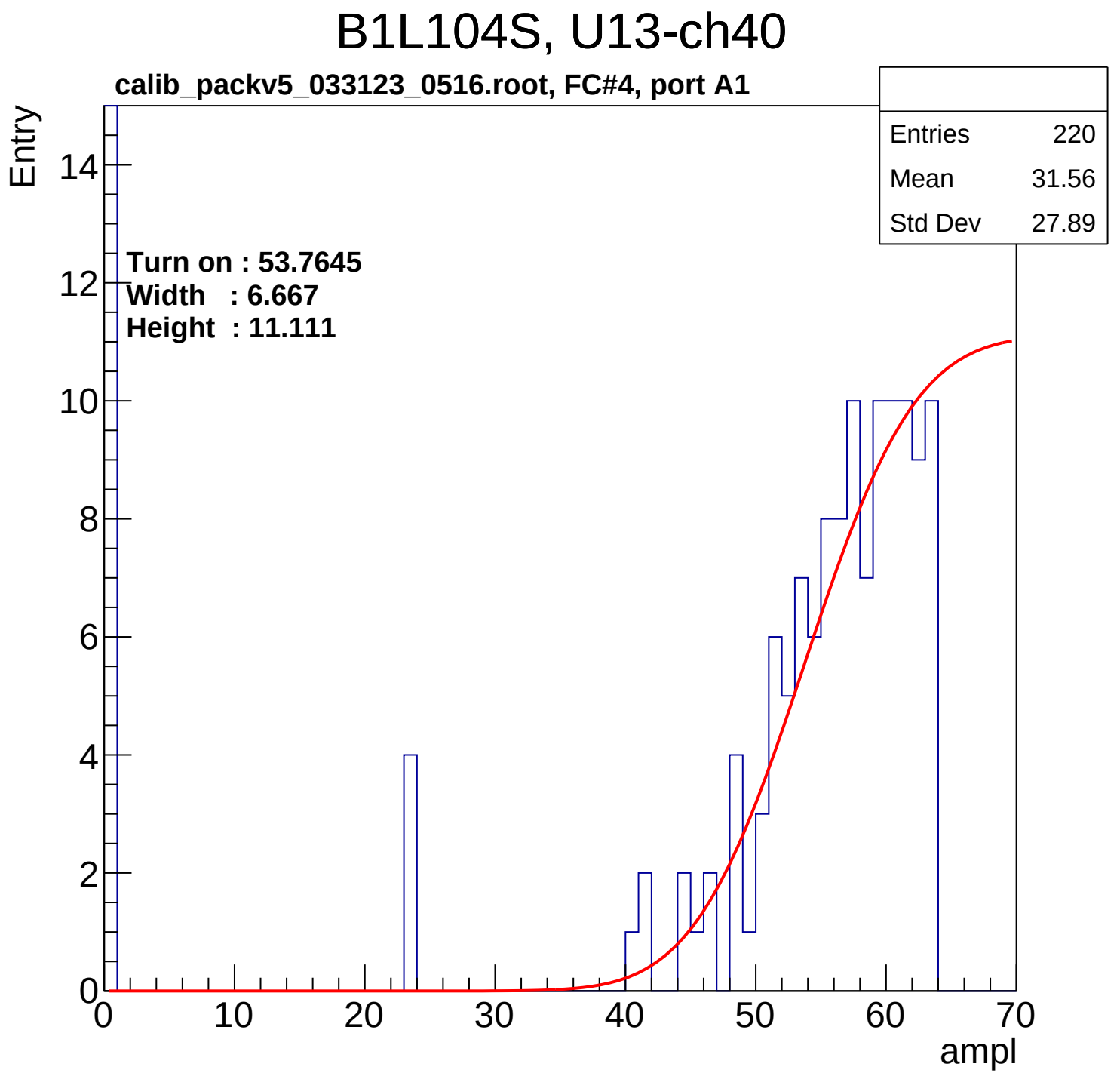
B1L104S, U13-ch40
calib_packv5_033123_0516.root, FC#4, port A1
Entries 220
Mean 31.56
Std Dev 27.89
Turn on : 53.7645
Width : 6.667
Height : 11.111
Entry
ampl
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4
6
8
10
12
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0
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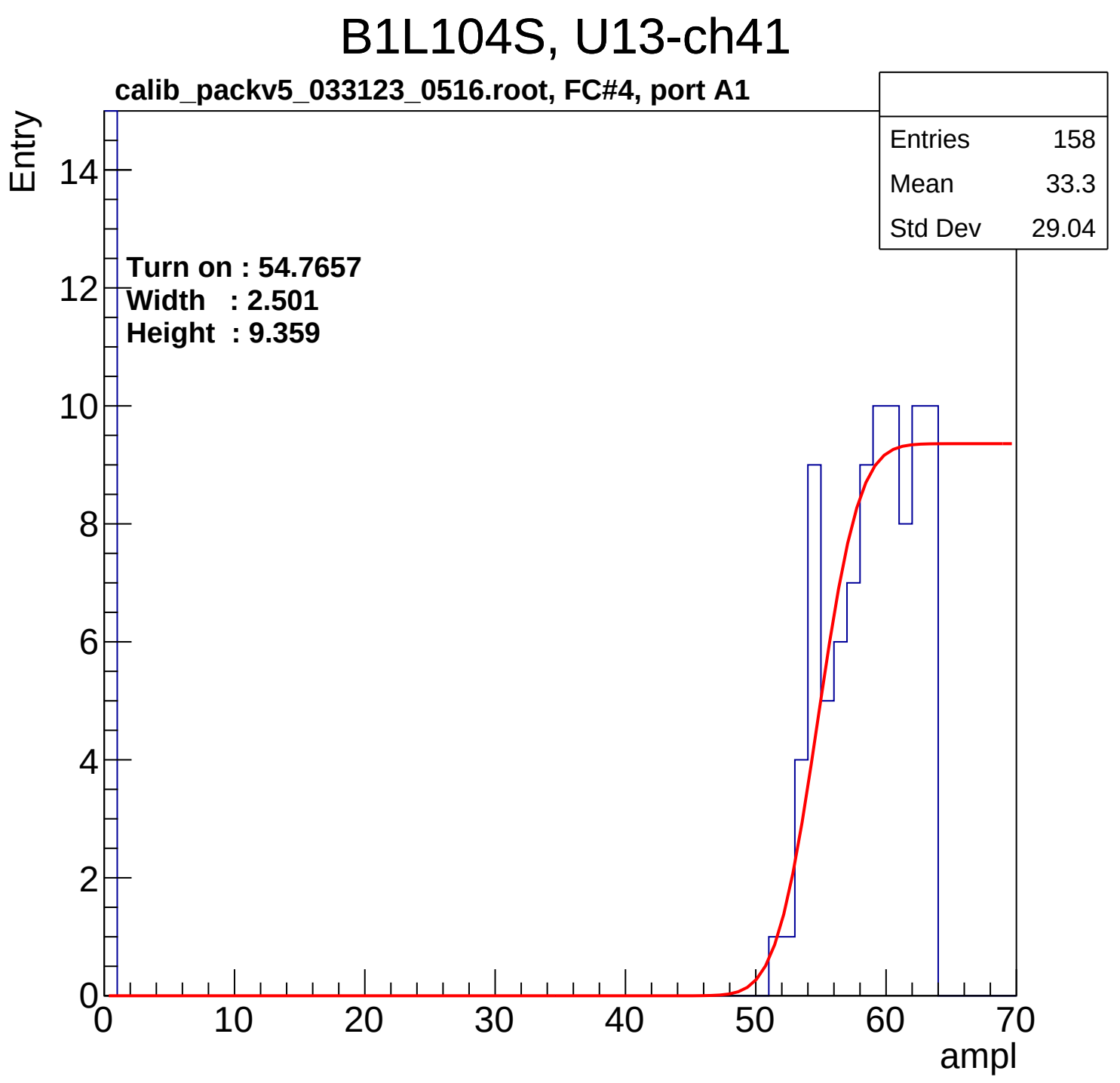
B1L104S, U13-ch41
calib_packv5_033123_0516.root, FC#4, port A1
Entries 158
Mean 33.3
Std Dev 29.04
Turn on : 54.7657
Width : 2.501
Height : 9.359
Entry
ampl
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4
6
8
10
12
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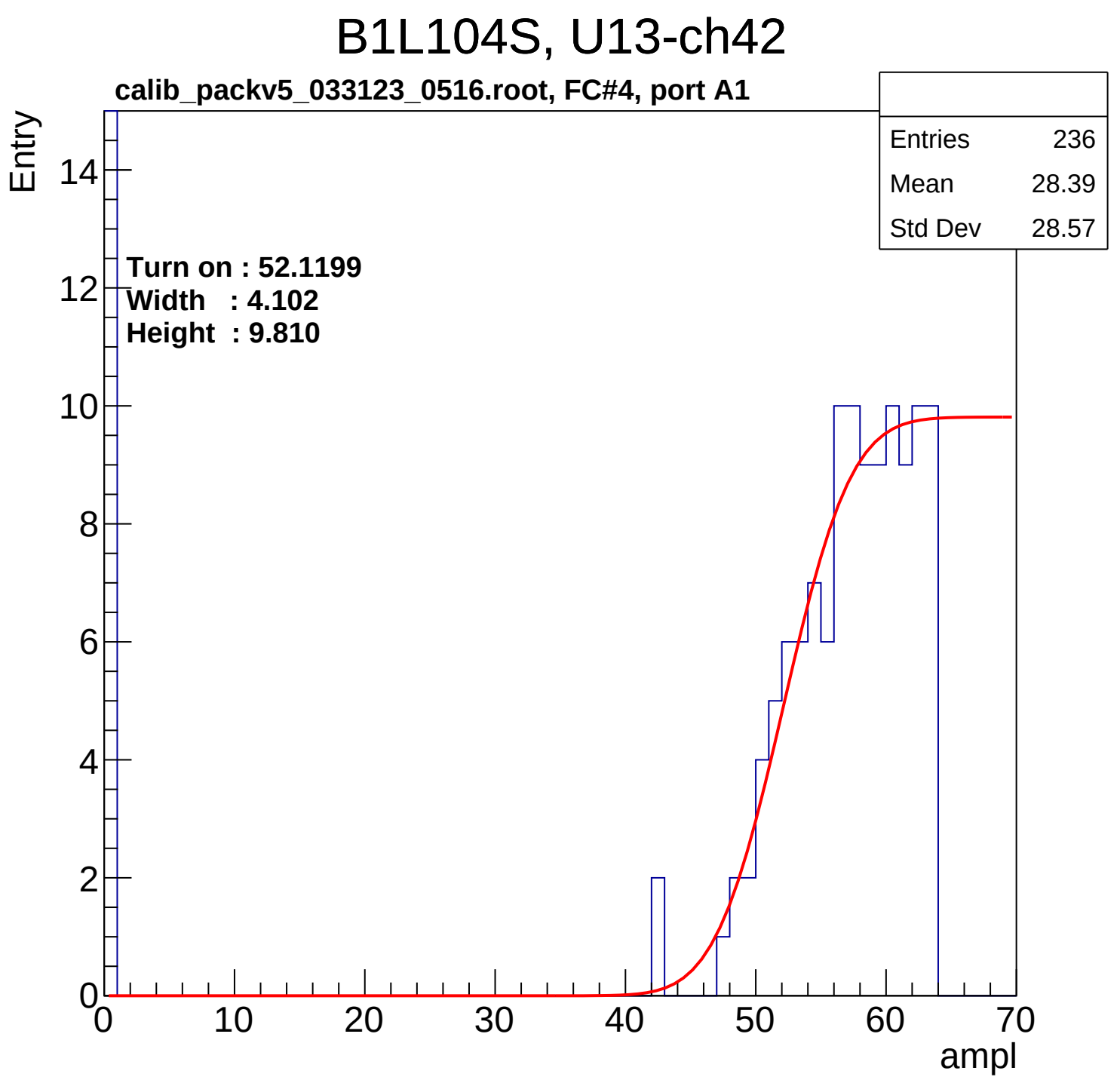
B1L104S, U13-ch42
calib_packv5_033123_0516.root, FC#4, port A1
Entries 236
Mean 28.39
Std Dev 28.57
Turn on : 52.1199
Width : 4.102
Height : 9.810
Entry
ampl
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4
6
8
10
12
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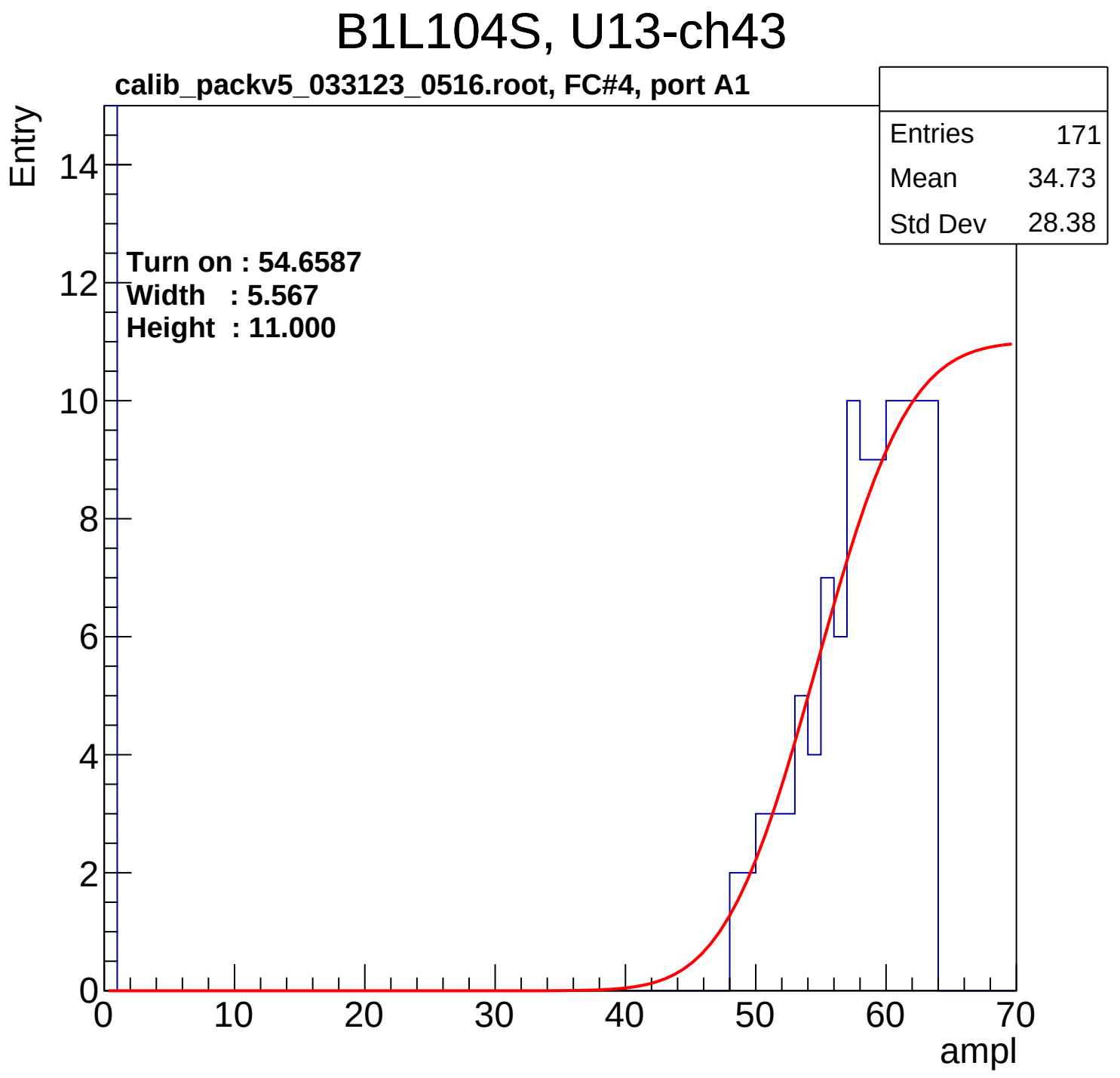
B1L104S, U13-ch43
calib_packv5_033123_0516.root, FC#4, port A1
Entries 171
Mean 34.73
Std Dev 28.38
Turn on : 54.6587
Width : 5.567
Height : 11.000
Entry
ampl
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4
6
8
10
12
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0
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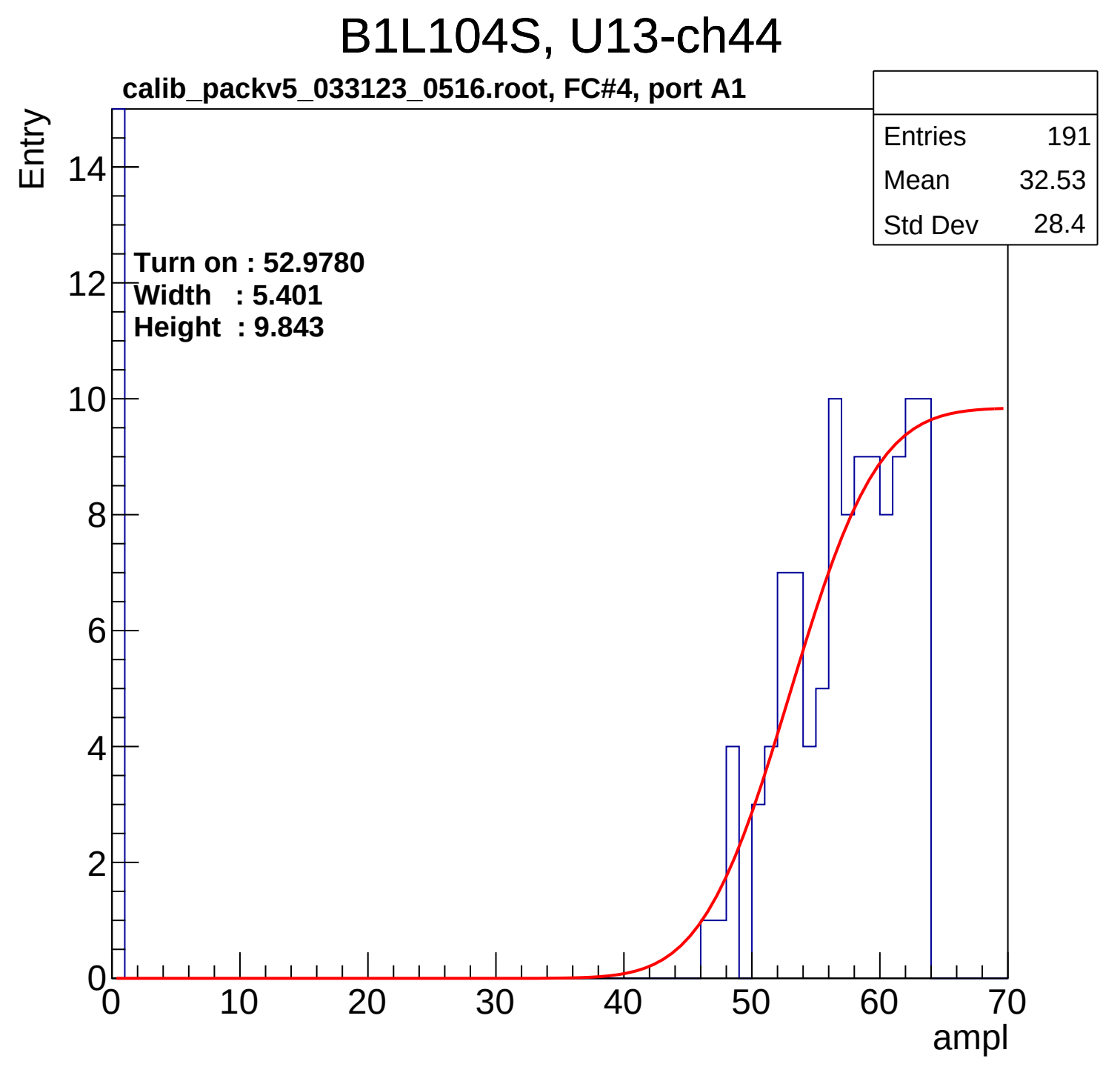
B1L104S, U13-ch44
calib_packv5_033123_0516.root, FC#4, port A1
Entries 191
Mean 32.53
Std Dev 28.4
Turn on : 52.9780
Width : 5.401
Height : 9.843
Entry
ampl
0
2
4
6
8
10
12
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0
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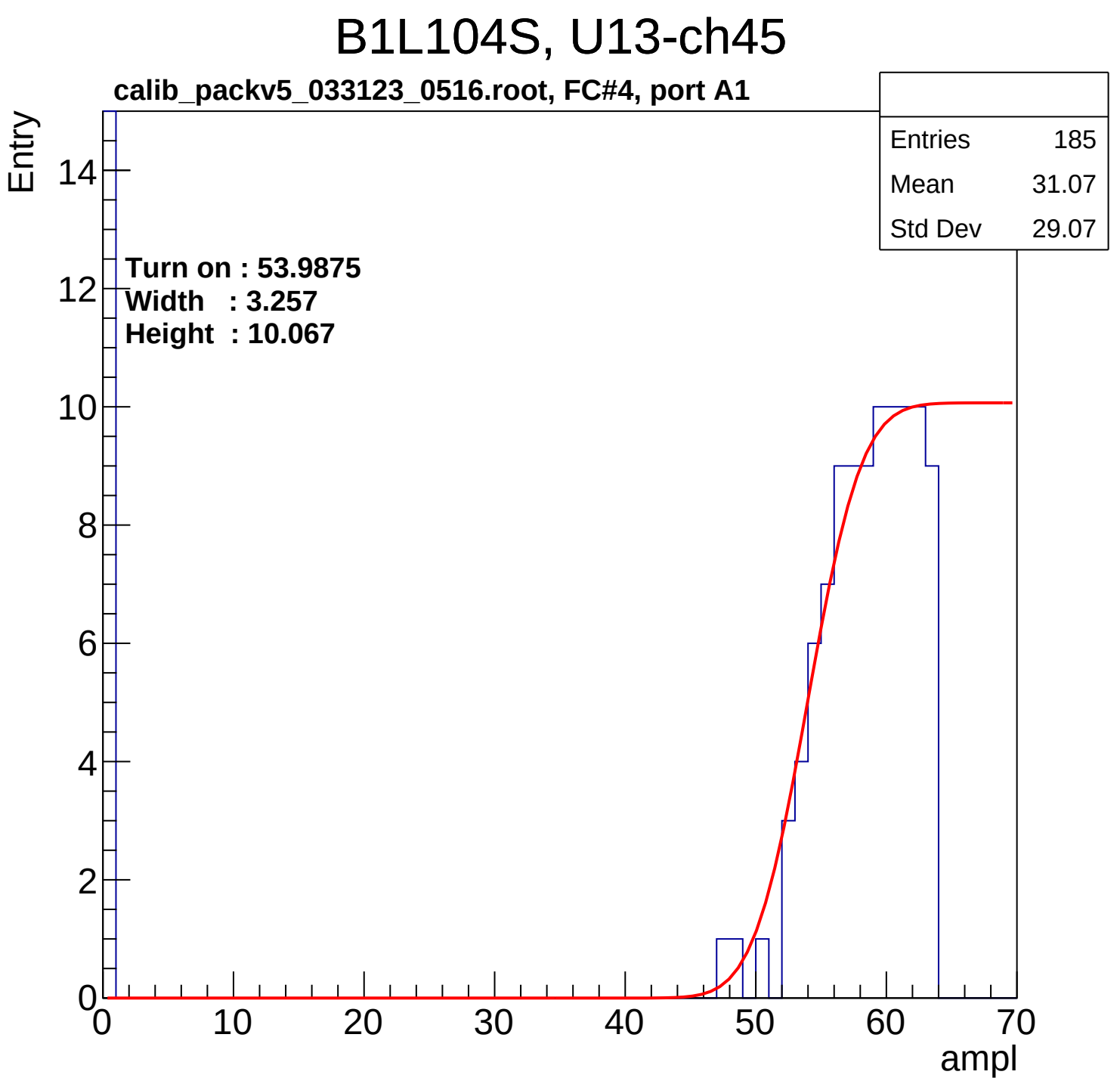
B1L104S, U13-ch45
calib_packv5_033123_0516.root, FC#4, port A1
Entries 185
Mean 31.07
Std Dev 29.07
Turn on : 53.9875
Width : 3.257
Height : 10.067
Entry
ampl
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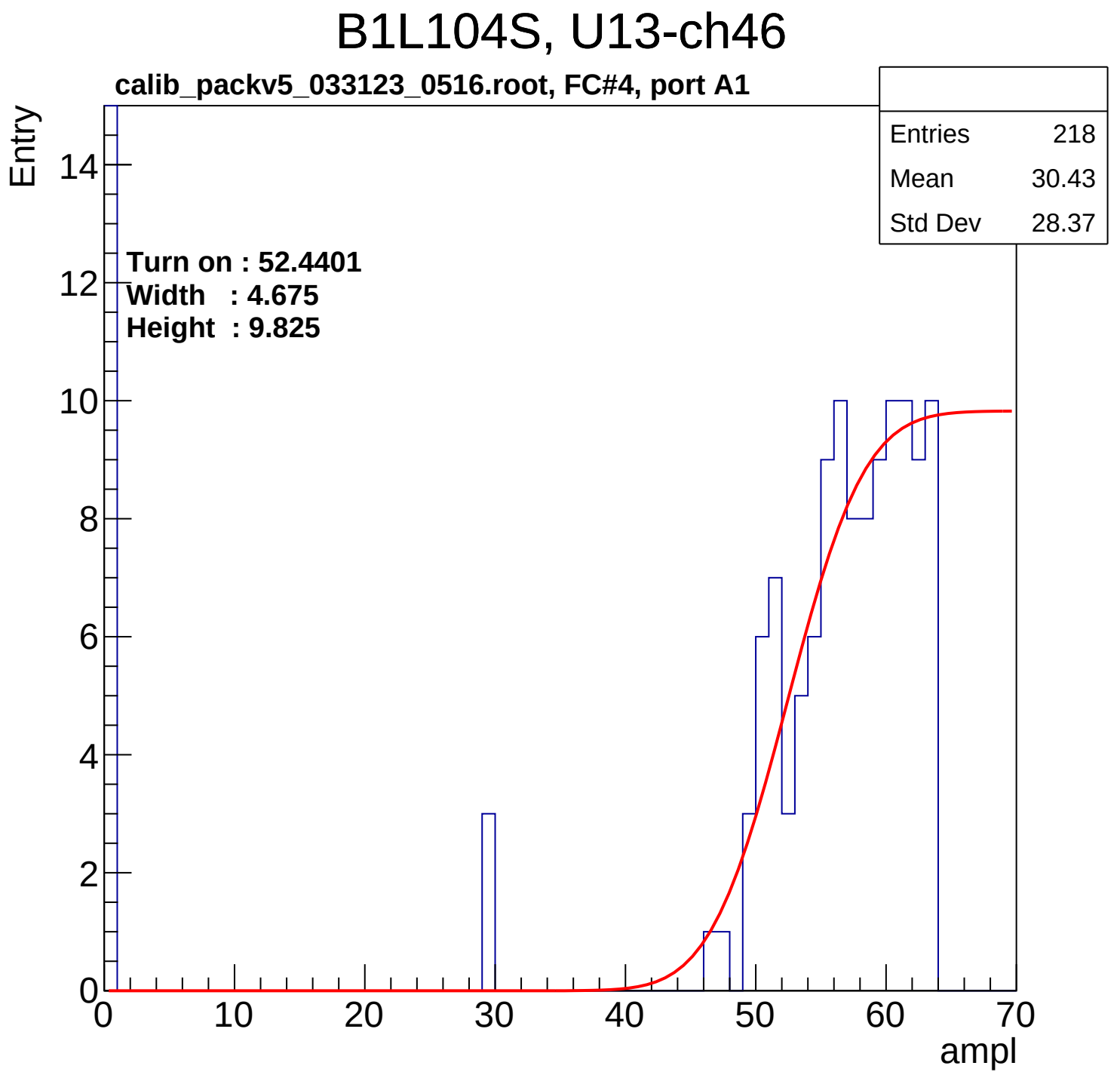
B1L104S, U13-ch46
calib_packv5_033123_0516.root, FC#4, port A1
Entries 218
Mean 30.43
Std Dev 28.37
Turn on : 52.4401
Width : 4.675
Height : 9.825
Entry
ampl
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2
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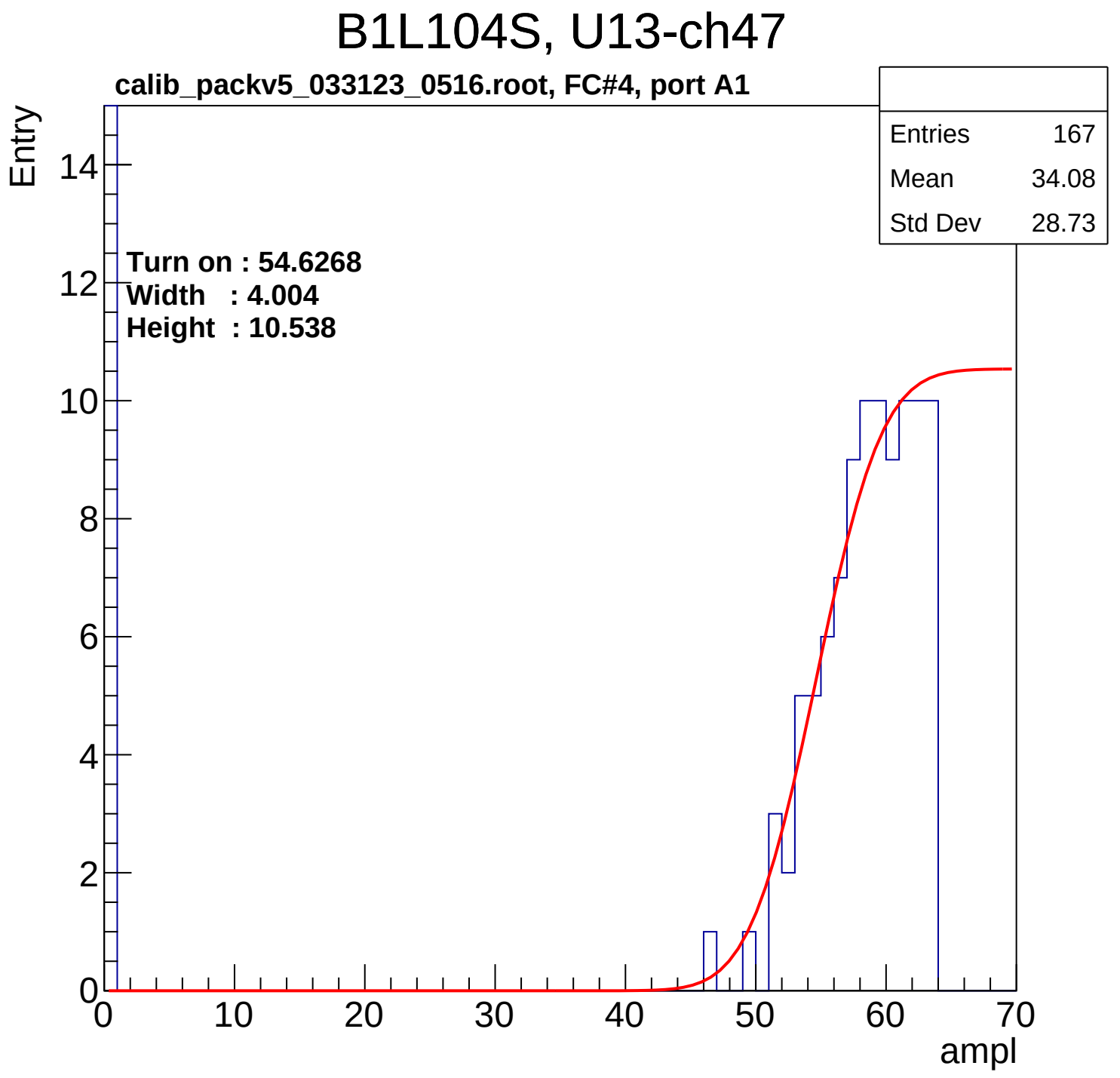
B1L104S, U13-ch47
calib_packv5_033123_0516.root, FC#4, port A1
Entries 167
Mean 34.08
Std Dev 28.73
Turn on : 54.6268
Width : 4.004
Height : 10.538
Entry
ampl
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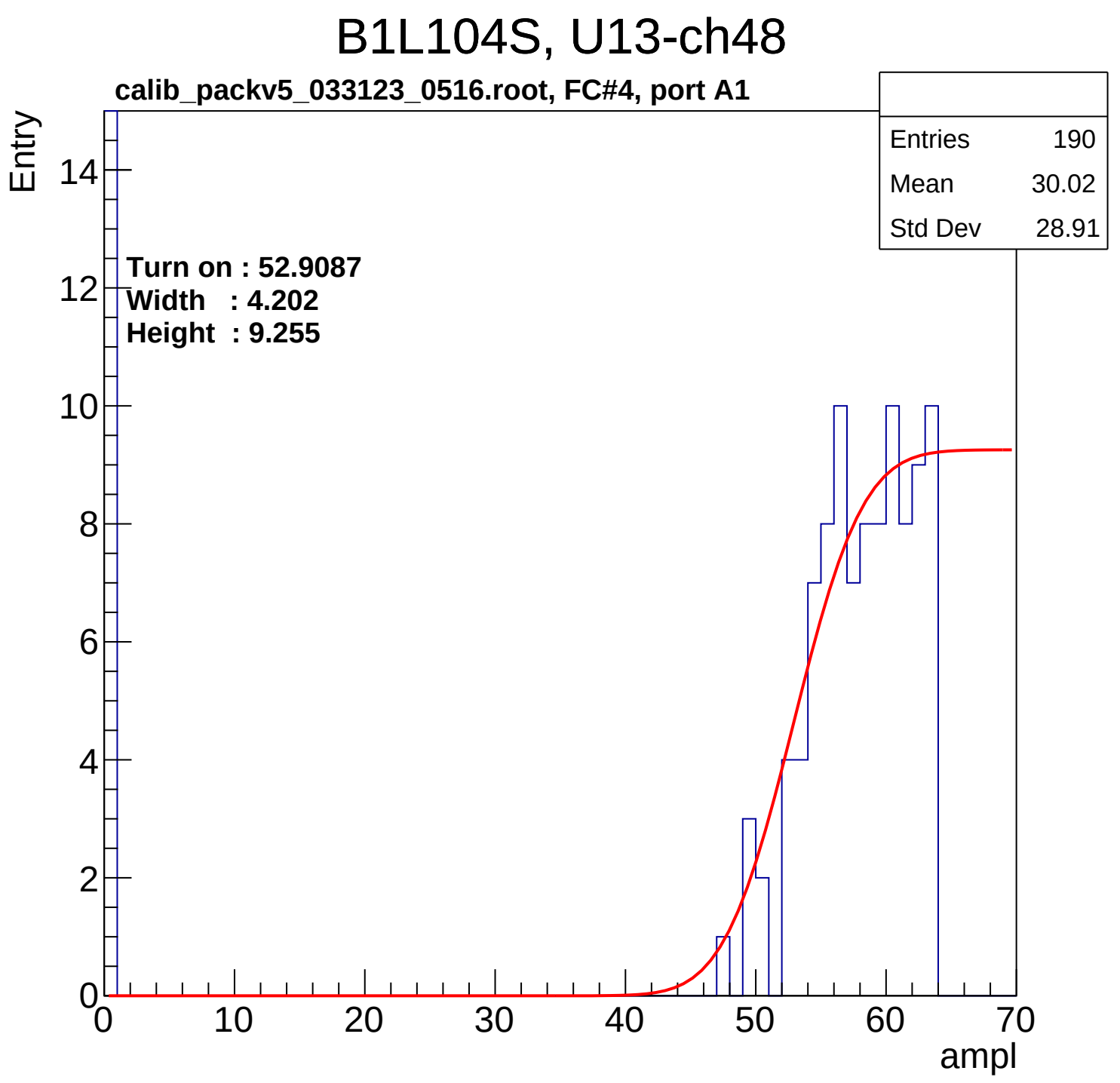
B1L104S, U13-ch48
calib_packv5_033123_0516.root, FC#4, port A1
Entries 190
Mean 30.02
Std Dev 28.91
Turn on : 52.9087
Width : 4.202
Height : 9.255
Entry
ampl
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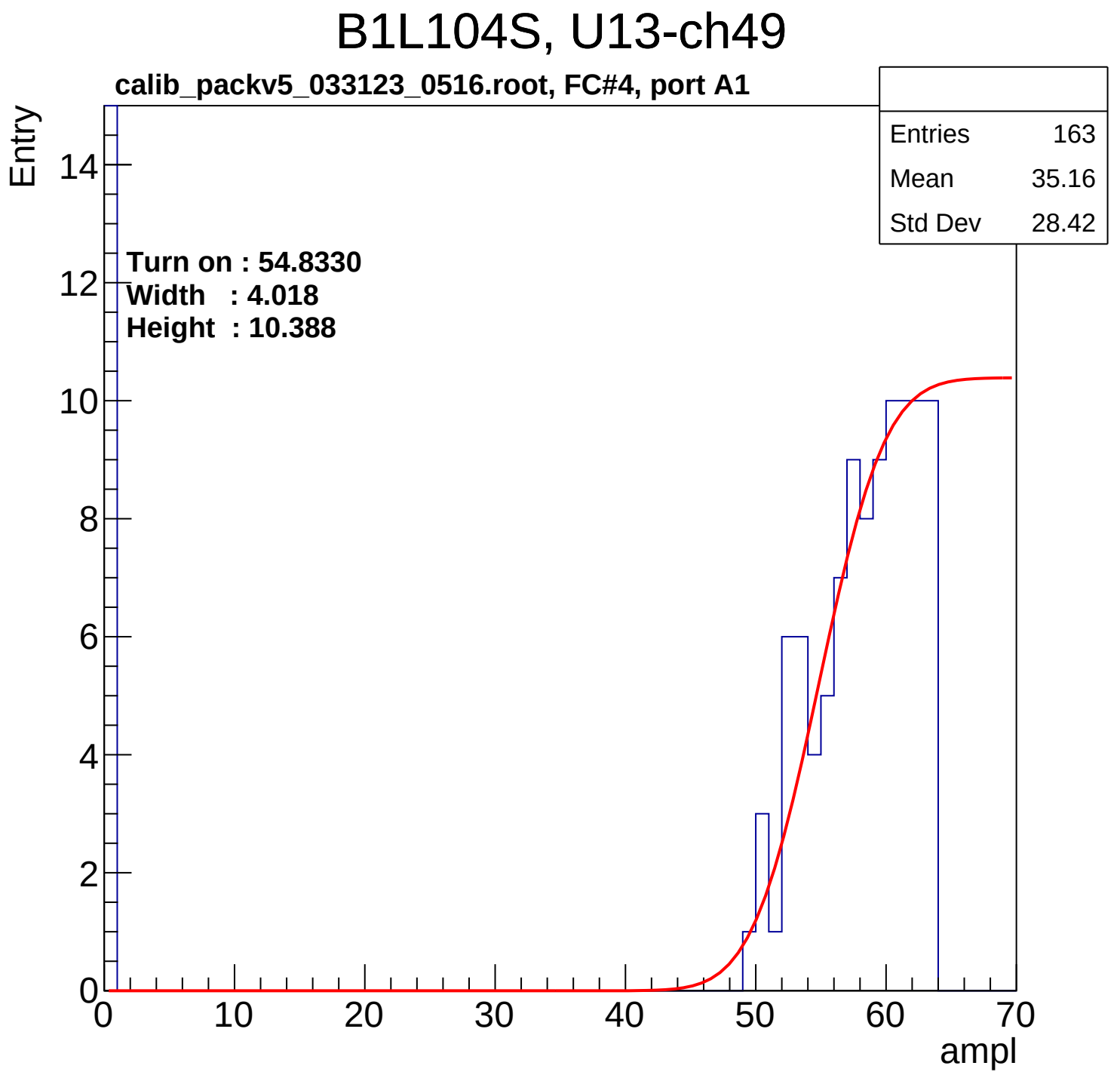
B1L104S, U13-ch49
calib_packv5_033123_0516.root, FC#4, port A1
Entries 163
Mean 35.16
Std Dev 28.42
Turn on : 54.8330
Width : 4.018
Height : 10.388
Entry
ampl
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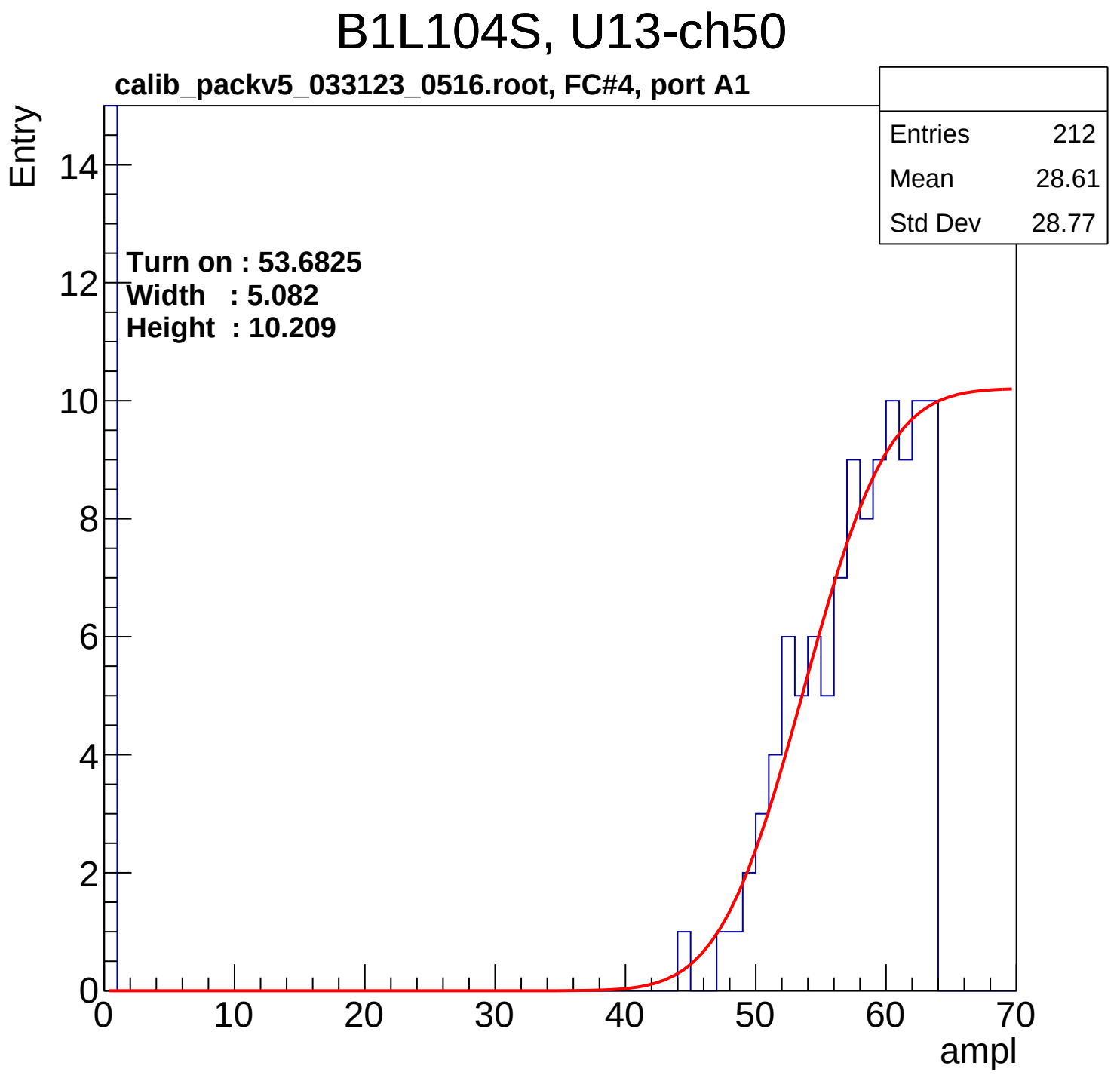
B1L104S, U13-ch50
calib_packv5_033123_0516.root, FC#4, port A1
Entries 212
Mean 28.61
Std Dev 28.77
Turn on : 53.6825
Width : 5.082
Height : 10.209
Entry
ampl
0
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8
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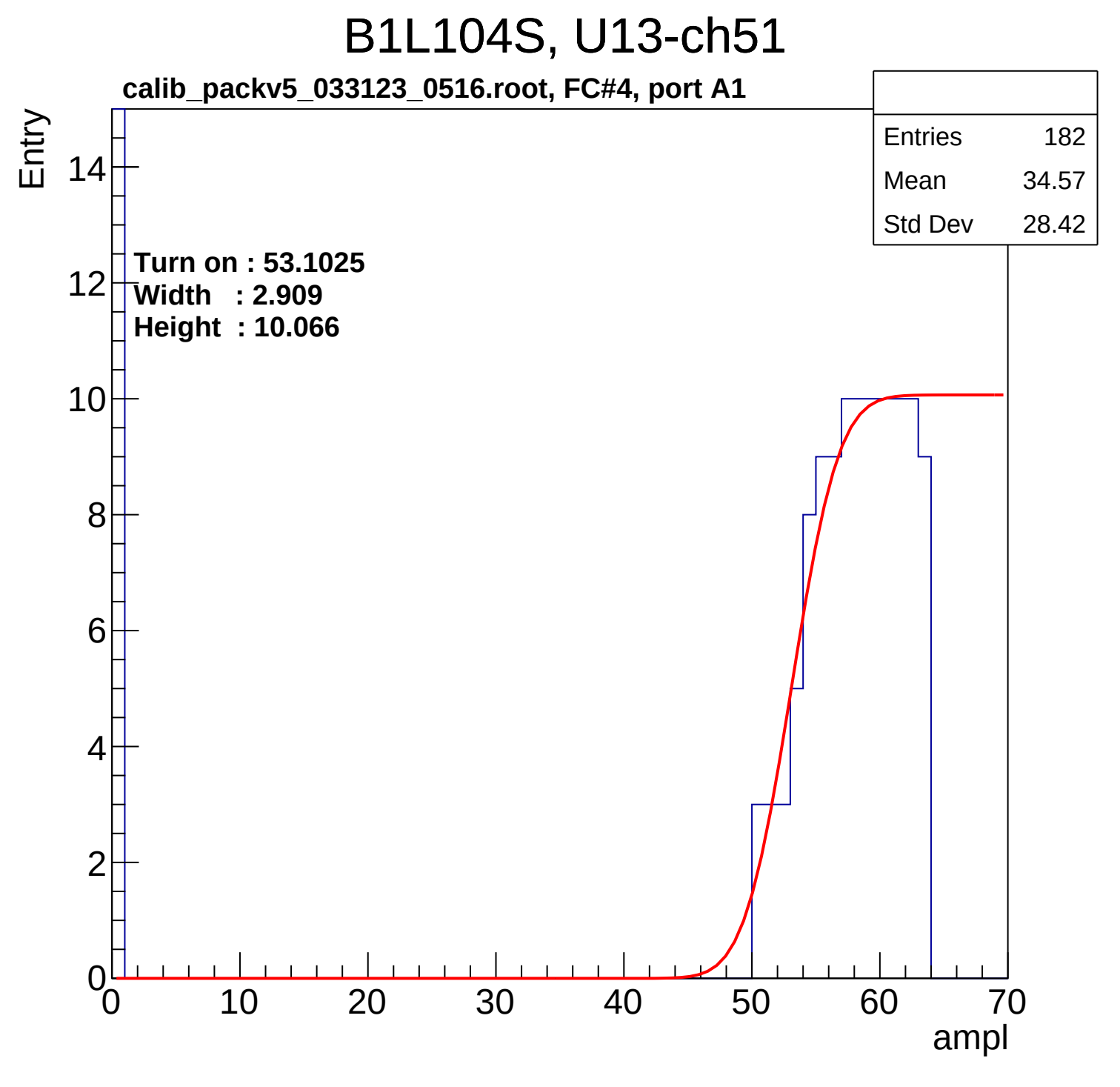
B1L104S, U13-ch51
calib_packv5_033123_0516.root, FC#4, port A1
Entries 182
Mean 34.57
Std Dev 28.42
Turn on : 53.1025
Width : 2.909
Height : 10.066
Entry
ampl
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6
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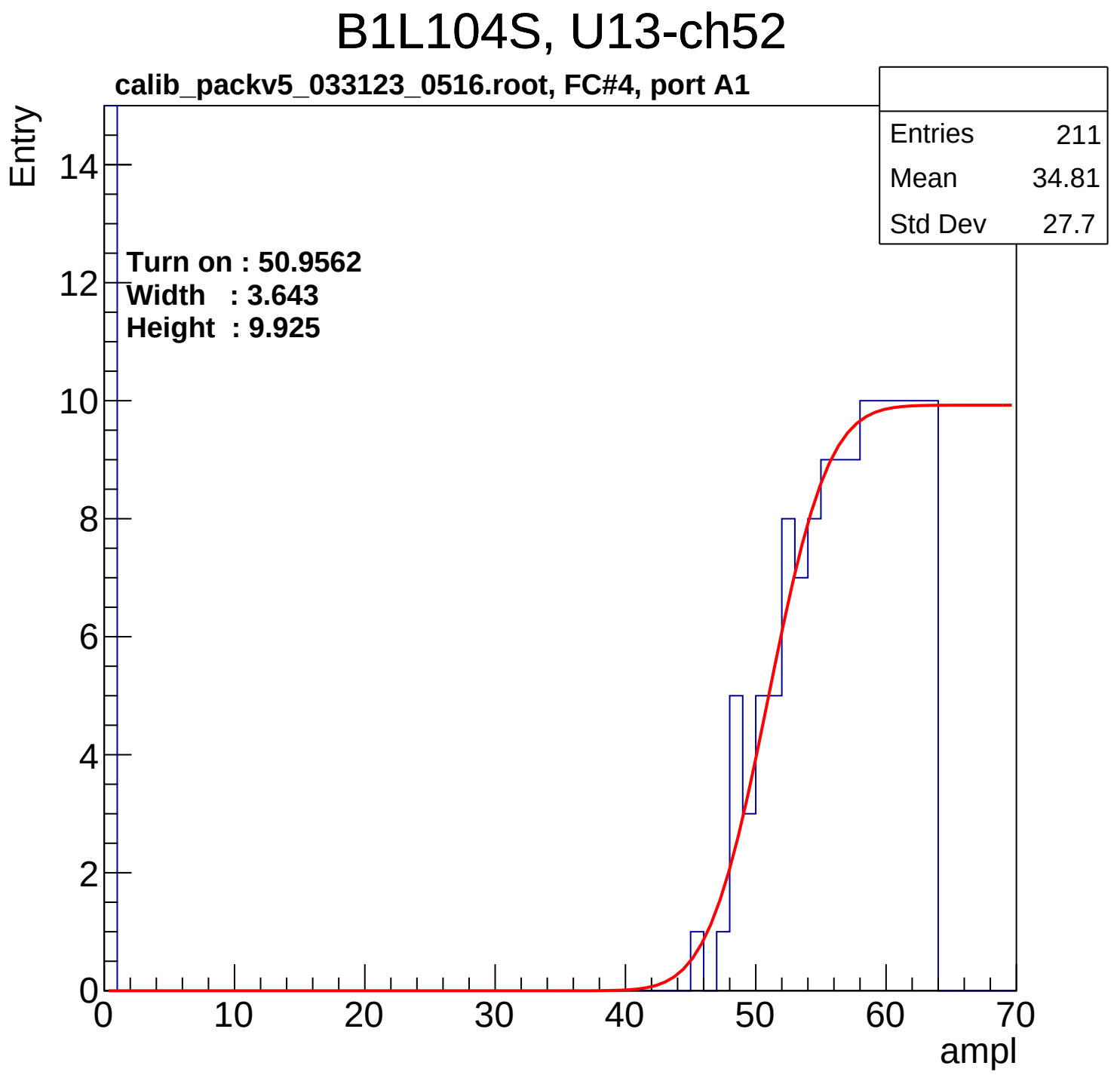
B1L104S, U13-ch52
calib_packv5_033123_0516.root, FC#4, port A1
Entries 211
Mean 34.81
Std Dev 27.7
Turn on : 50.9562
Width : 3.643
Height : 9.925
Entry
ampl
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2
4
6
8
10
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0
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20
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60
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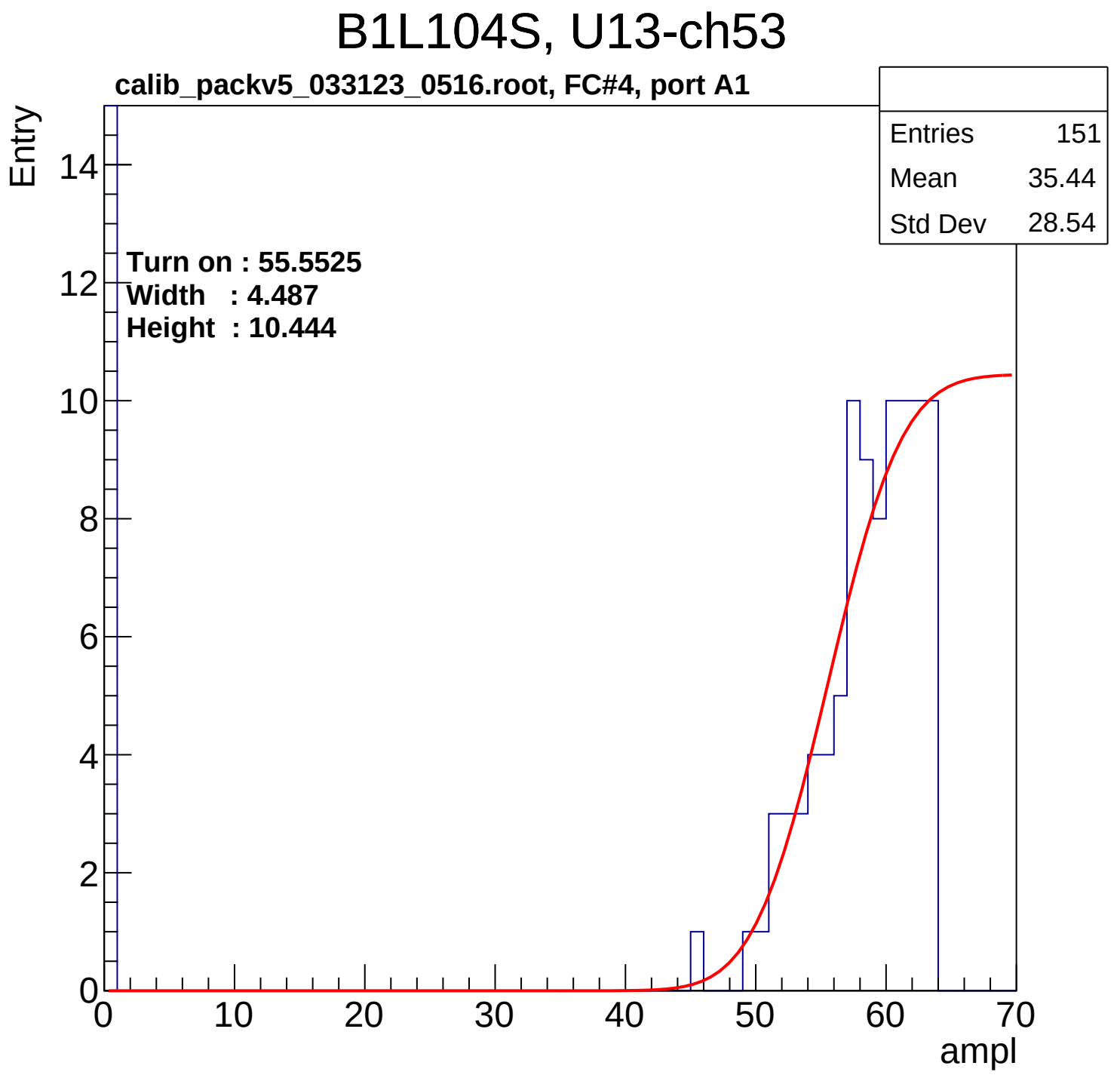
B1L104S, U13-ch53
calib_packv5_033123_0516.root, FC#4, port A1
Entries 151
Mean 35.44
Std Dev 28.54
Turn on : 55.5525
Width : 4.487
Height : 10.444
Entry
ampl
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6
8
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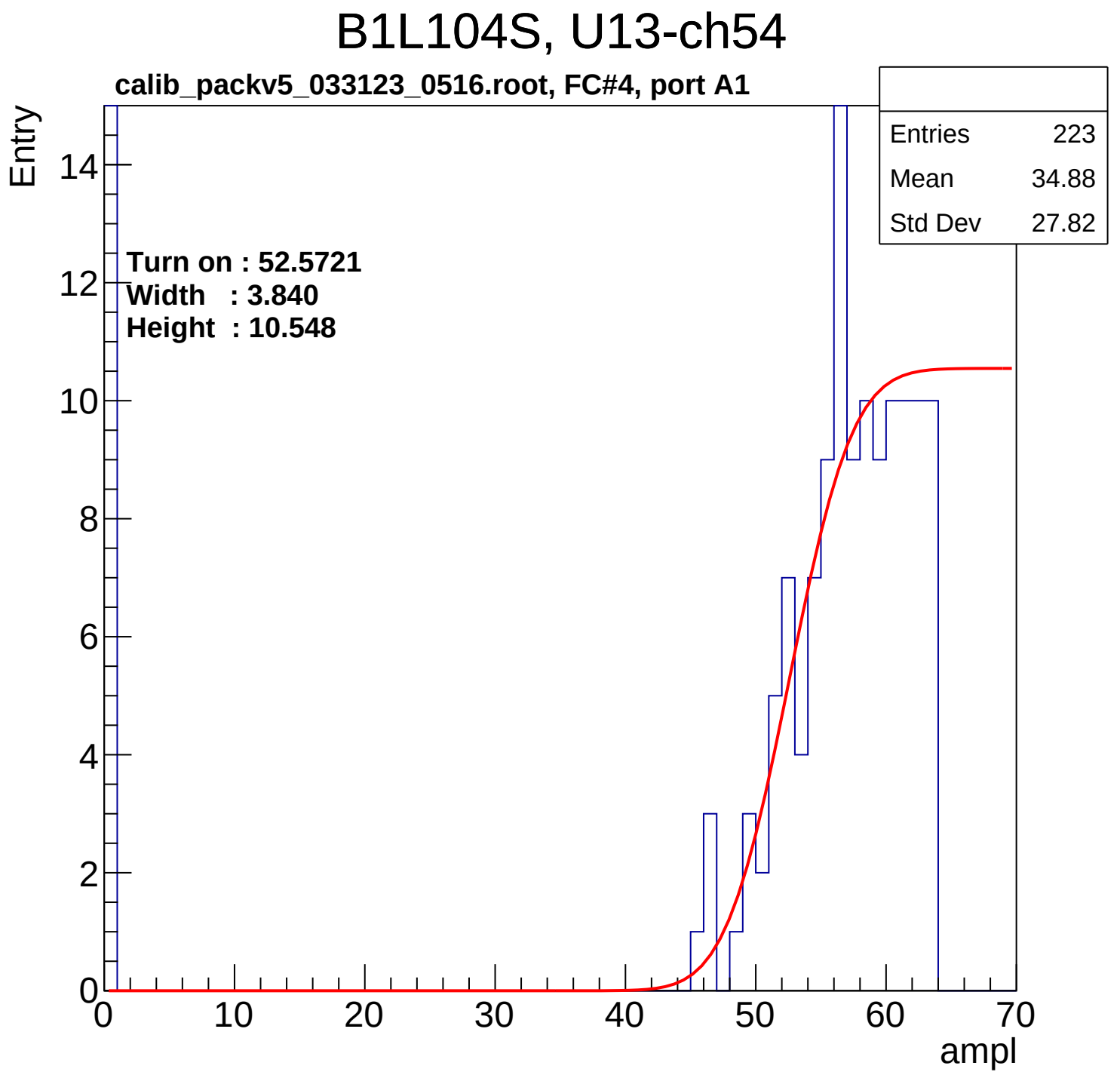
B1L104S, U13-ch54
calib_packv5_033123_0516.root, FC#4, port A1
Entries 223
Mean 34.88
Std Dev 27.82
Turn on : 52.5721
Width : 3.840
Height : 10.548
Entry
ampl
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6
8
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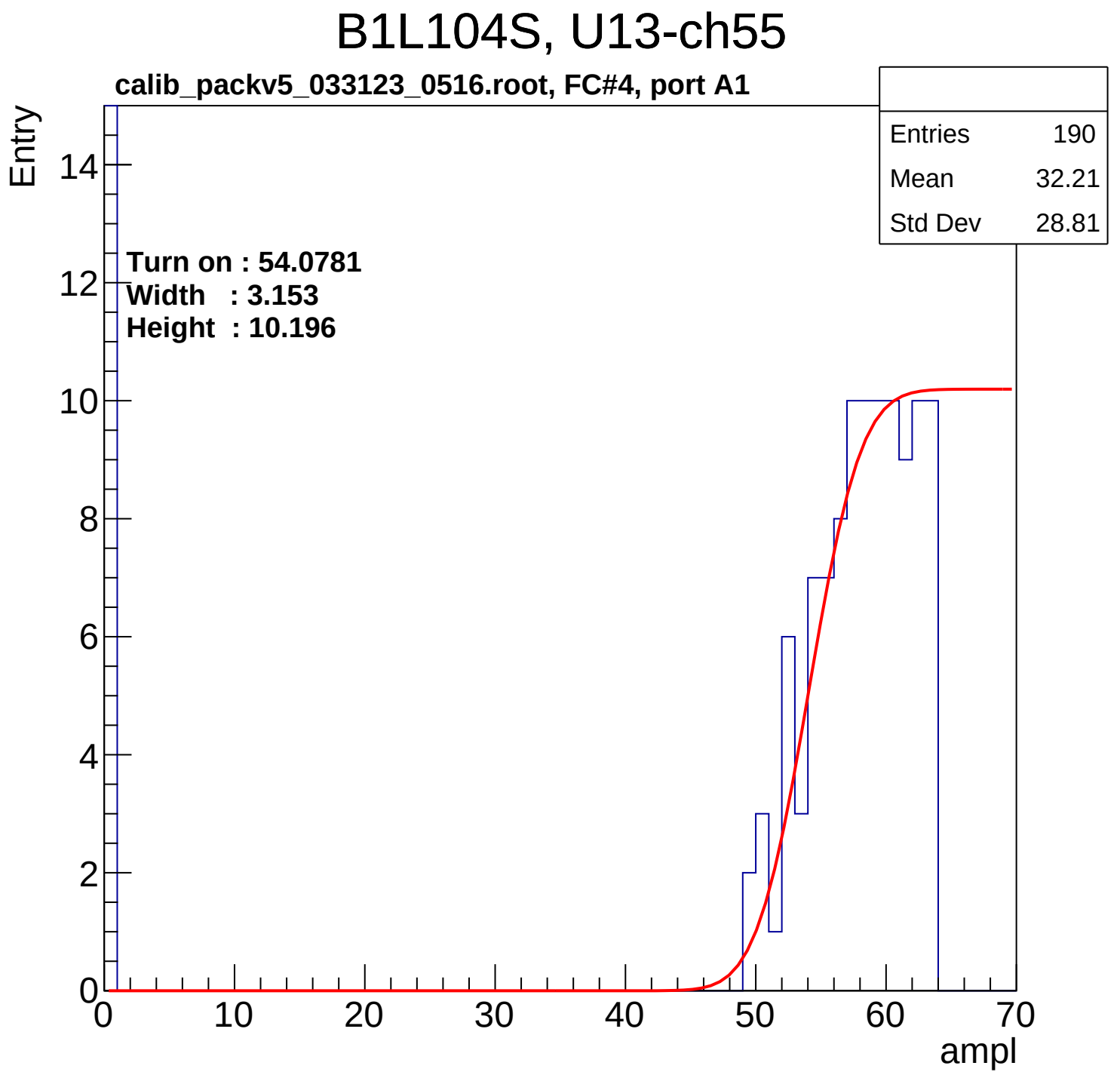
B1L104S, U13-ch55
calib_packv5_033123_0516.root, FC#4, port A1
Entries 190
Mean 32.21
Std Dev 28.81
Turn on : 54.0781
Width : 3.153
Height : 10.196
Entry
ampl
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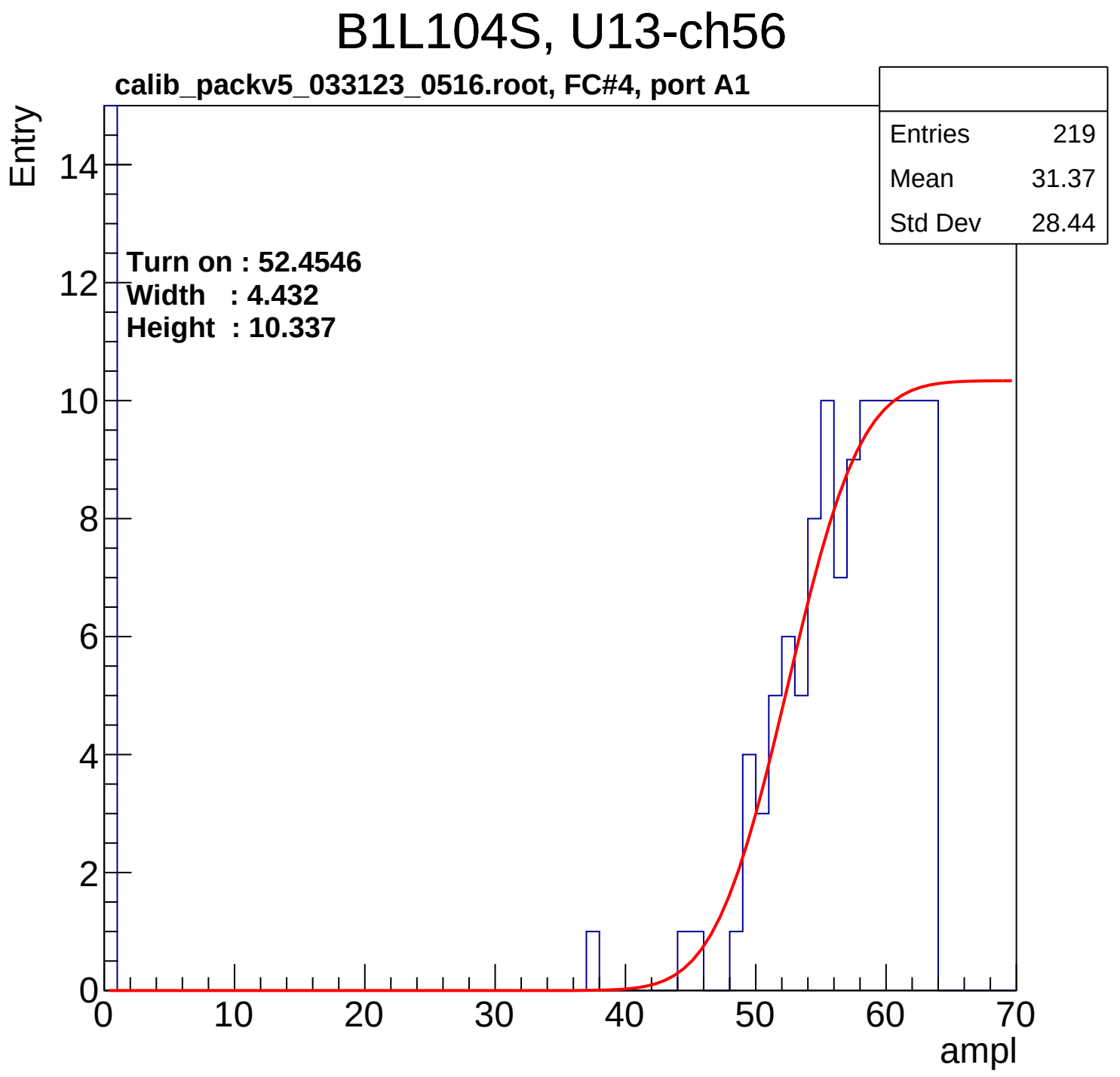
B1L104S, U13-ch56
calib_packv5_033123_0516.root, FC#4, port A1
Entries 219
Mean 31.37
Std Dev 28.44
Turn on : 52.4546
Width : 4.432
Height : 10.337
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ampl
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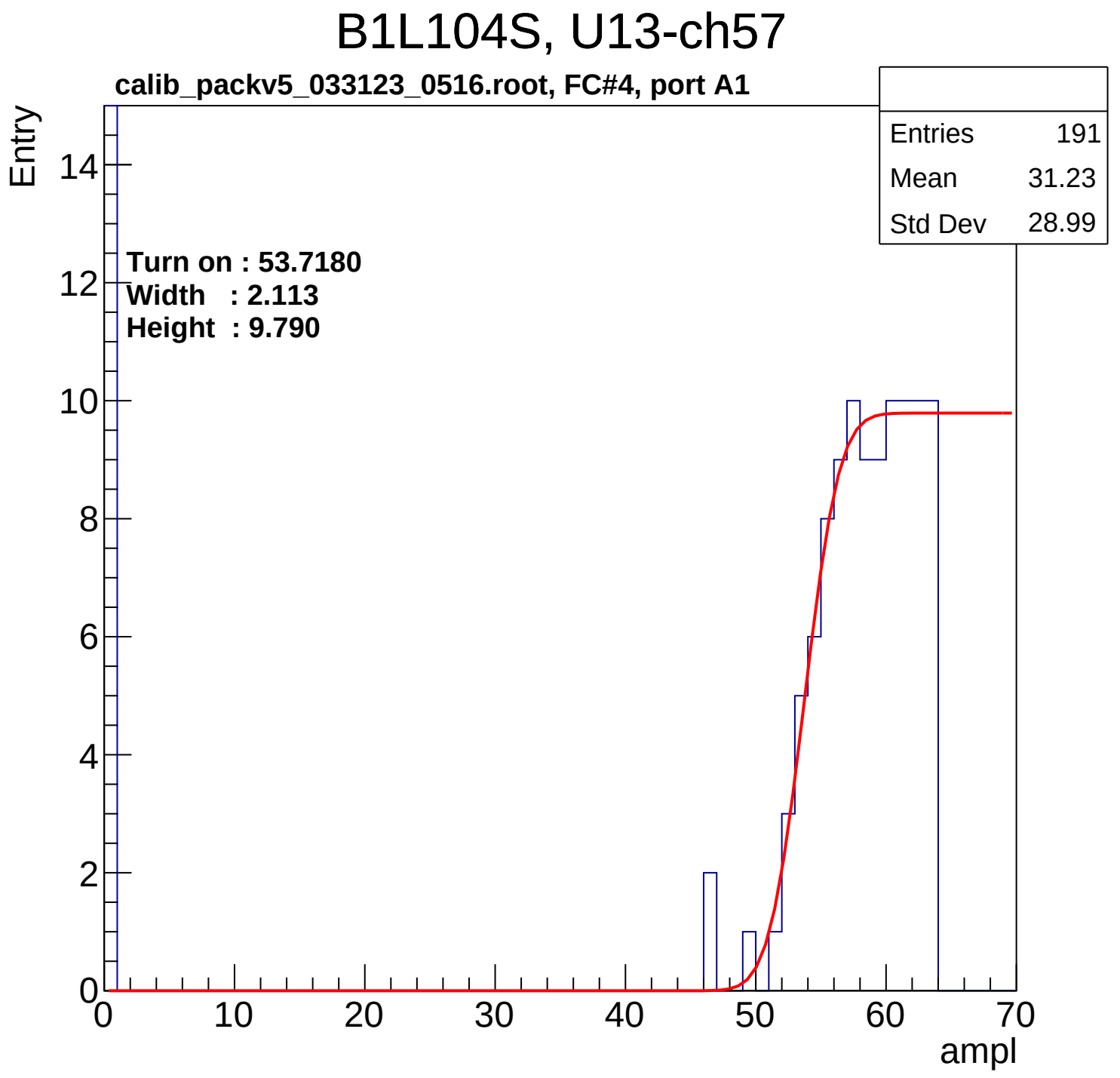
B1L104S, U13-ch57
calib_packv5_033123_0516.root, FC#4, port A1
Entries 191
Mean 31.23
Std Dev 28.99
Turn on : 53.7180
Width : 2.113
Height : 9.790
Entry
ampl
0
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4
6
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12
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20
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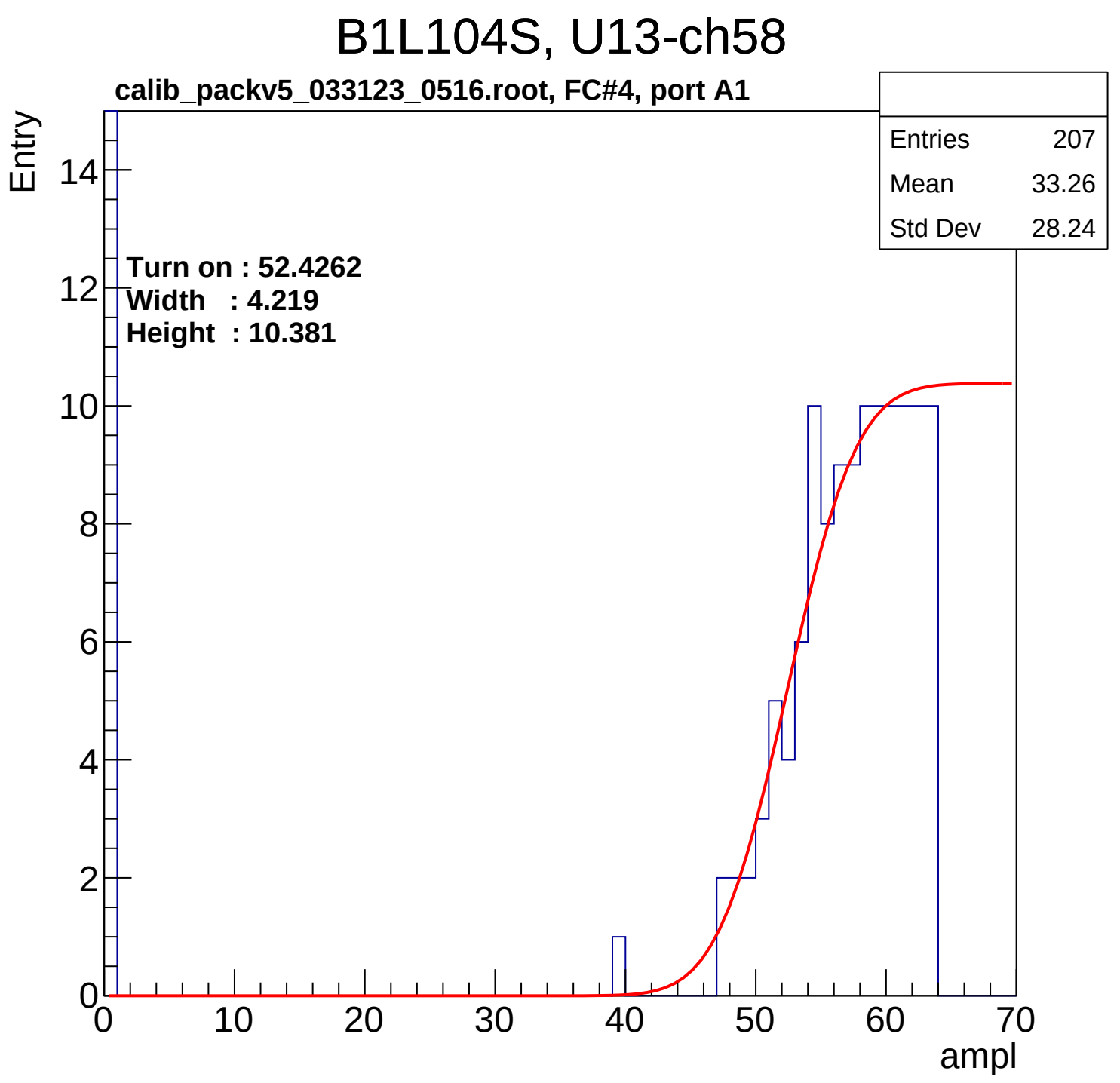
B1L104S, U13-ch58
calib_packv5_033123_0516.root, FC#4, port A1
Entries 207
Mean 33.26
Std Dev 28.24
Turn on : 52.4262
Width : 4.219
Height : 10.381
Entry
ampl
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2
4
6
8
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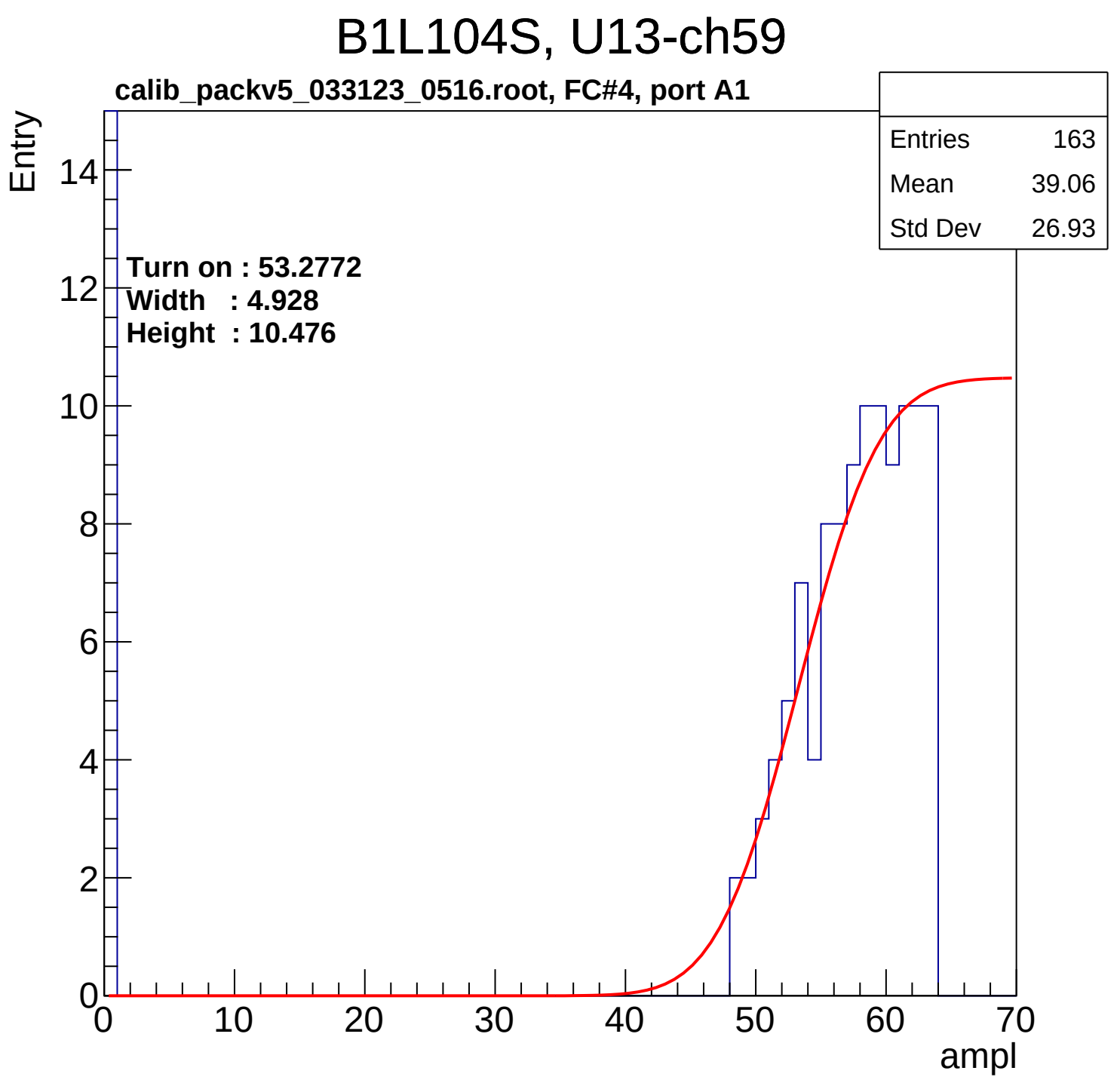
B1L104S, U13-ch59
calib_packv5_033123_0516.root, FC#4, port A1
Entries 163
Mean 39.06
Std Dev 26.93
Turn on : 53.2772
Width : 4.928
Height : 10.476
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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60
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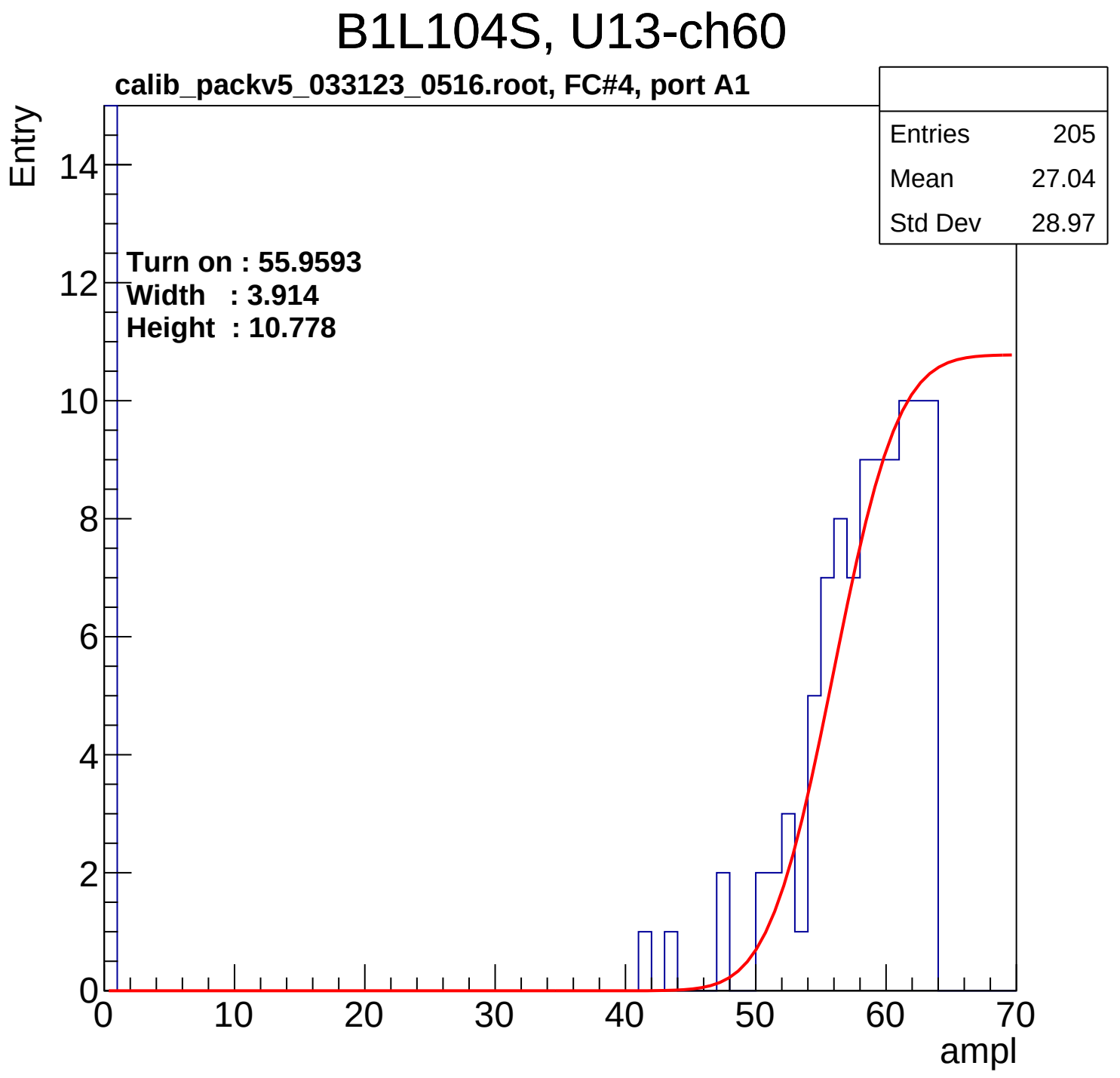
B1L104S, U13-ch60
calib_packv5_033123_0516.root, FC#4, port A1
Entries 205
Mean 27.04
Std Dev 28.97
Turn on : 55.9593
Width : 3.914
Height : 10.778
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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40
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60
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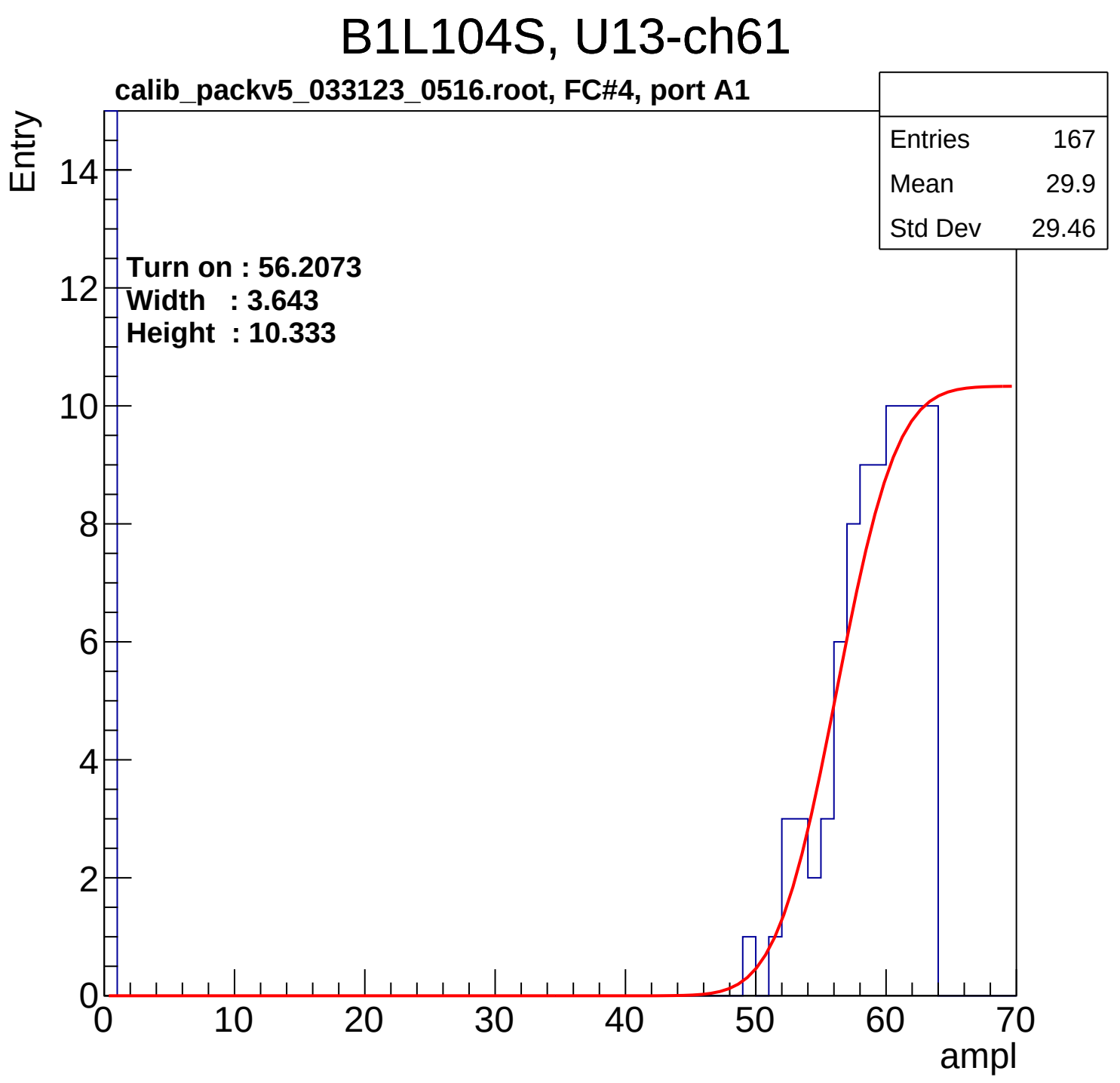
B1L104S, U13-ch61
calib_packv5_033123_0516.root, FC#4, port A1
Entries 167
Mean 29.9
Std Dev 29.46
Turn on : 56.2073
Width : 3.643
Height : 10.333
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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60
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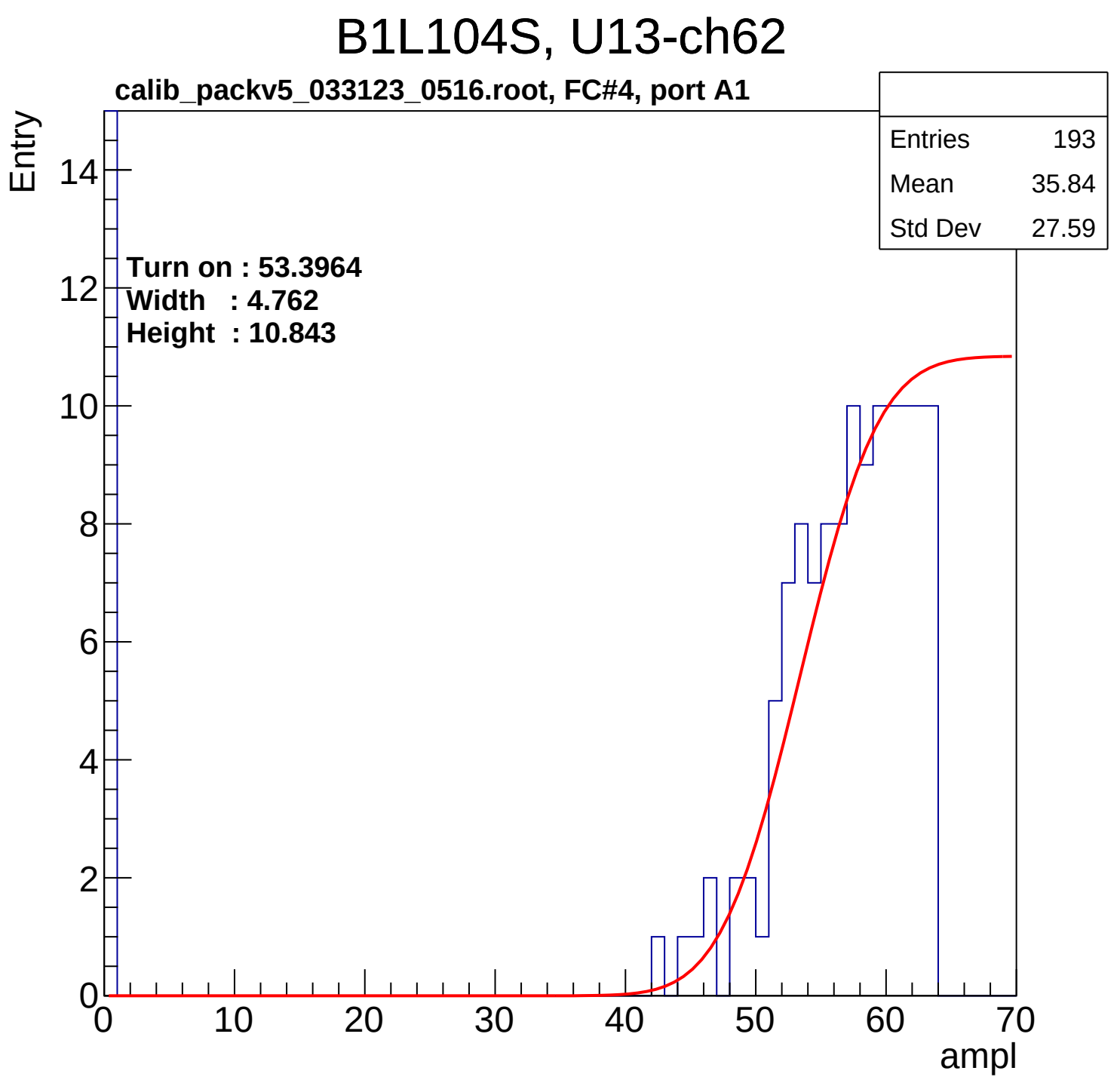
B1L104S, U13-ch62
calib_packv5_033123_0516.root, FC#4, port A1
Entries 193
Mean 35.84
Std Dev 27.59
Turn on : 53.3964
Width : 4.762
Height : 10.843
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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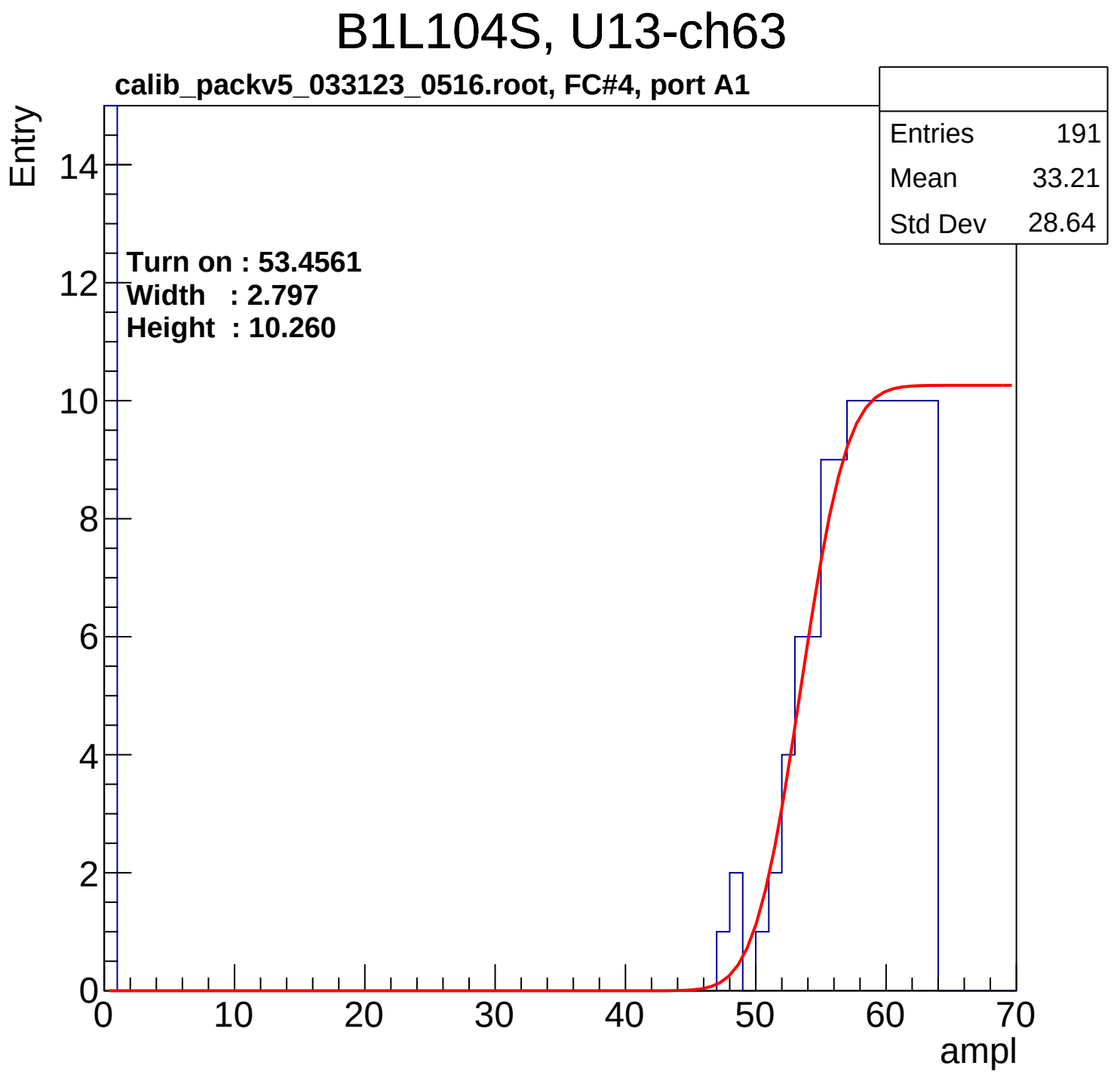
B1L104S, U13-ch63
calib_packv5_033123_0516.root, FC#4, port A1
Entries 191
Mean 33.21
Std Dev 28.64
Turn on : 53.4561
Width : 2.797
Height : 10.260
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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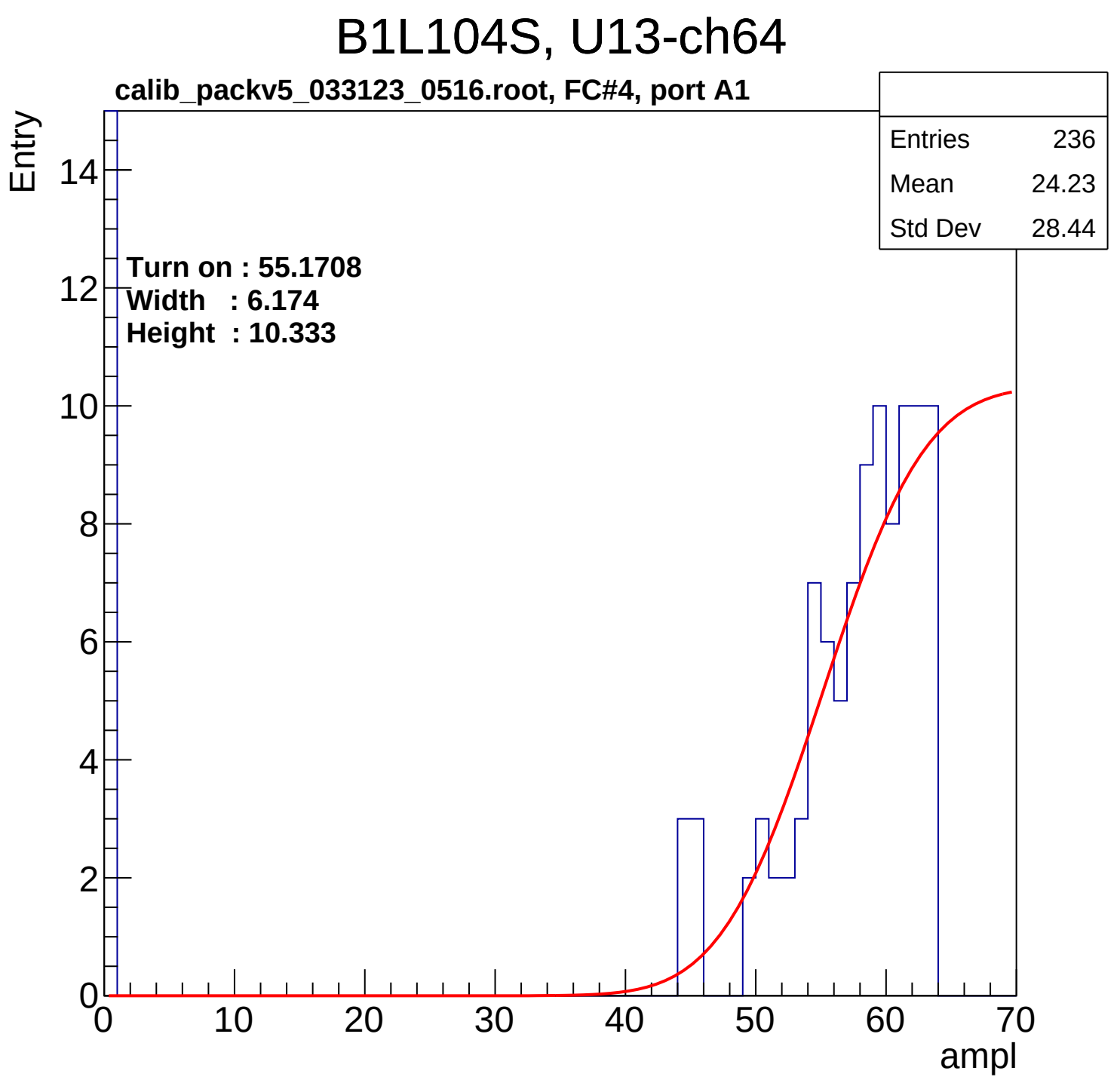
B1L104S, U13-ch64
calib_packv5_033123_0516.root, FC#4, port A1
Entries 236
Mean 24.23
Std Dev 28.44
Turn on : 55.1708
Width : 6.174
Height : 10.333
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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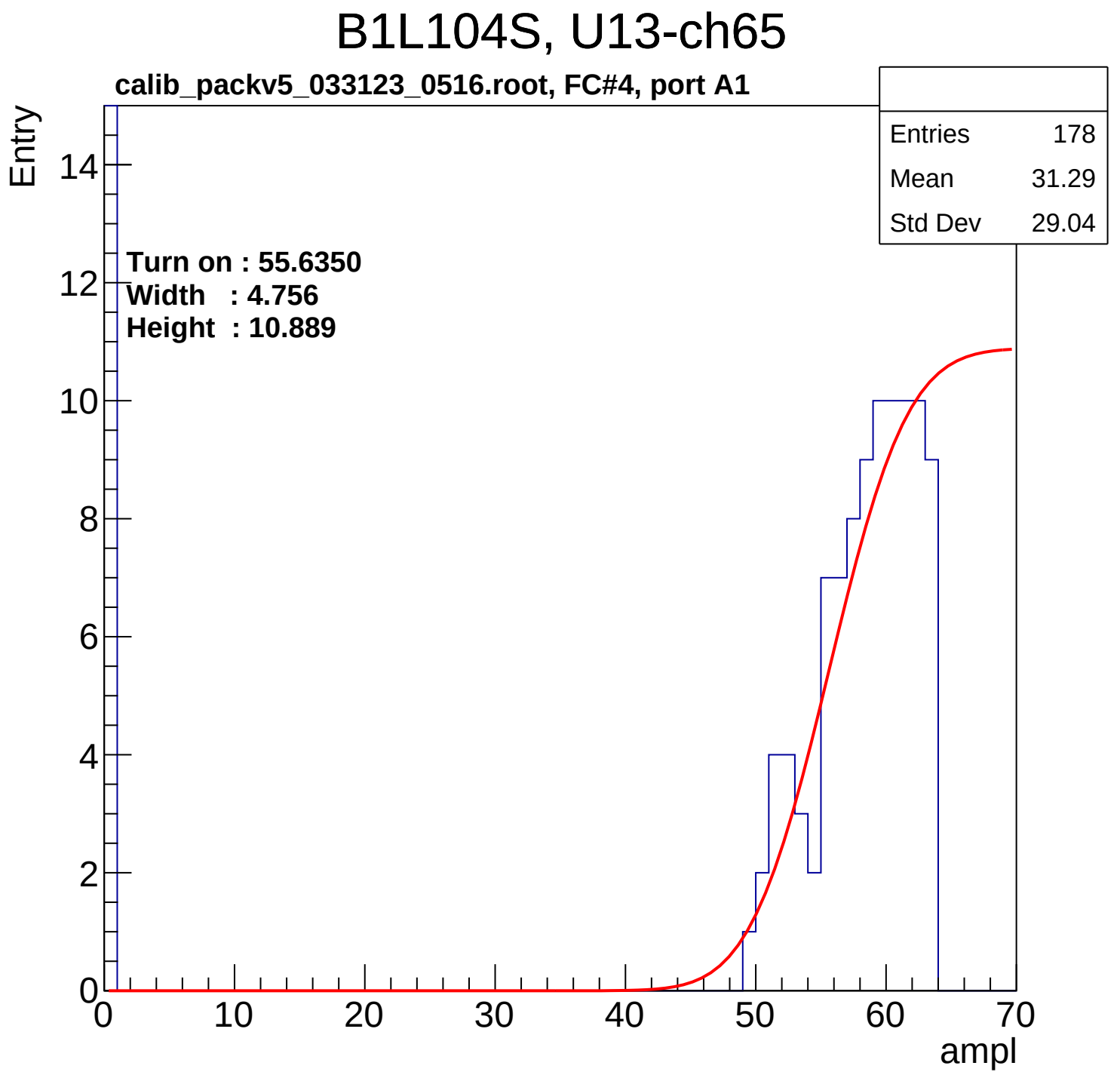
B1L104S, U13-ch65
calib_packv5_033123_0516.root, FC#4, port A1
Entries 178
Mean 31.29
Std Dev 29.04
Turn on : 55.6350
Width : 4.756
Height : 10.889
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
50
60
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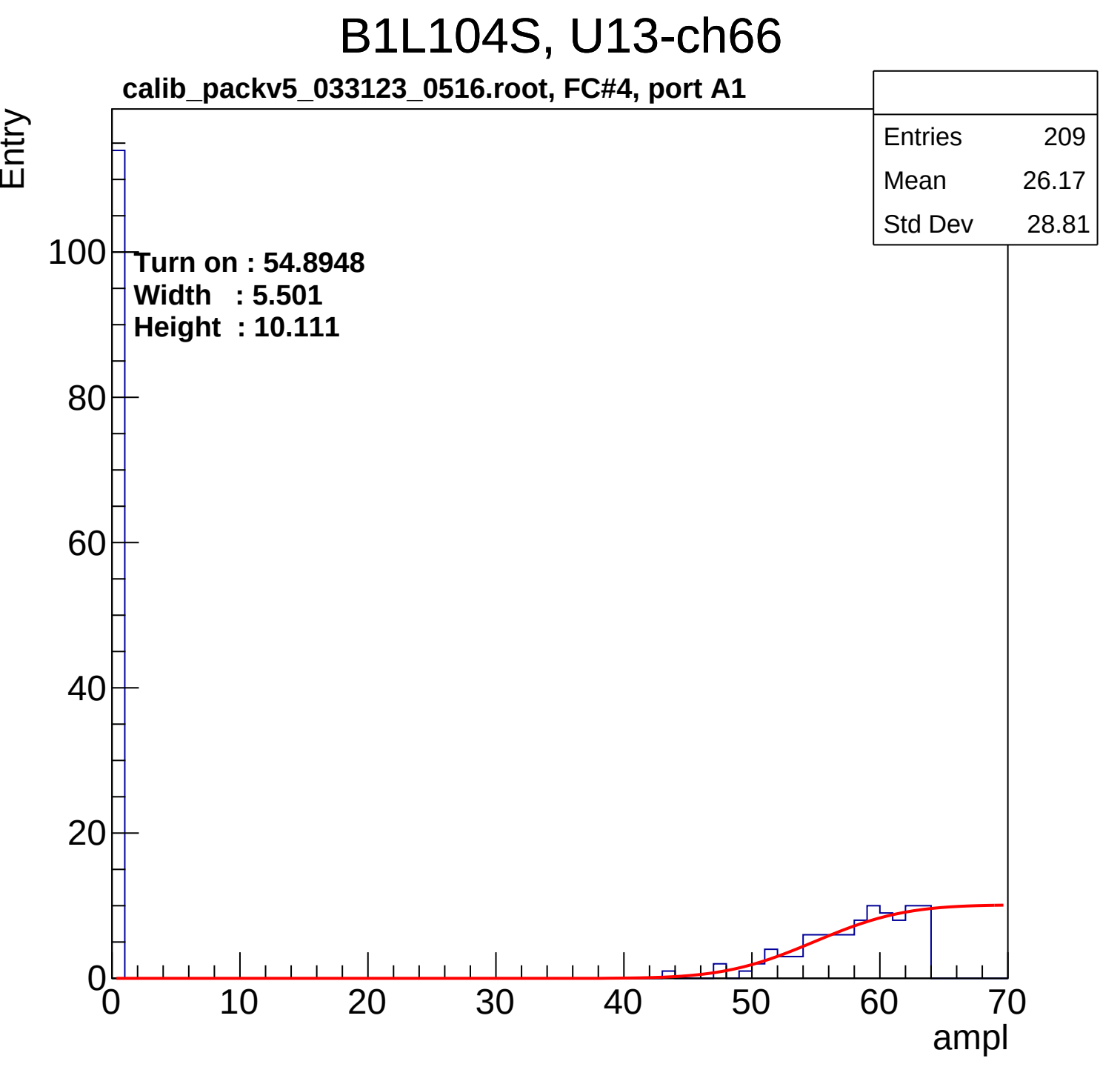
B1L104S, U13-ch66
calib_packv5_033123_0516.root, FC#4, port A1
Entries 209
Mean 26.17
Std Dev 28.81
Turn on : 54.8948
Width : 5.501
Height : 10.111
Entry
ampl
0
20
40
60
80
100
0
10
20
30
40
50
60
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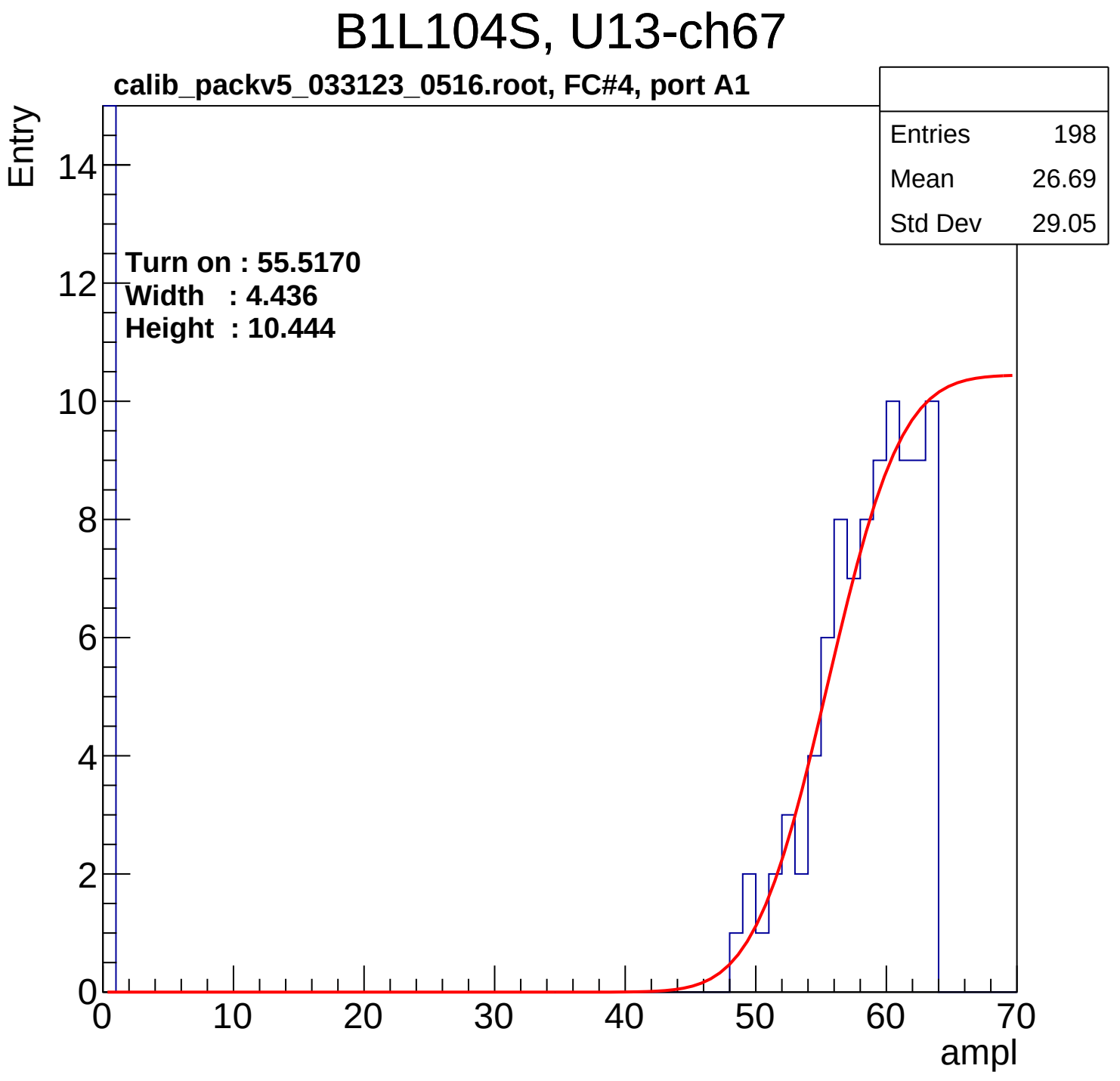
B1L104S, U13-ch67
calib_packv5_033123_0516.root, FC#4, port A1
Entries 198
Mean 26.69
Std Dev 29.05
Turn on : 55.5170
Width : 4.436
Height : 10.444
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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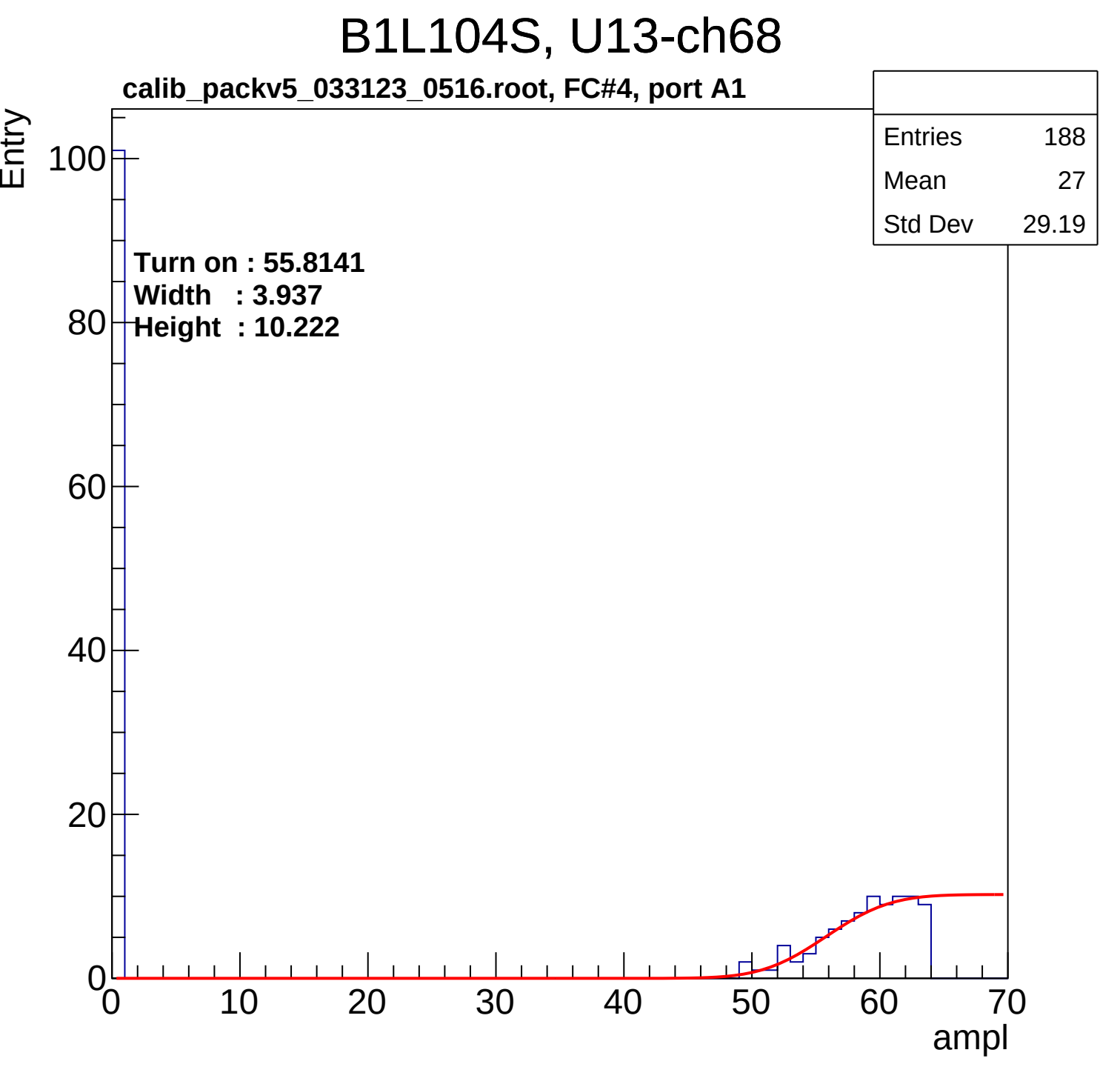
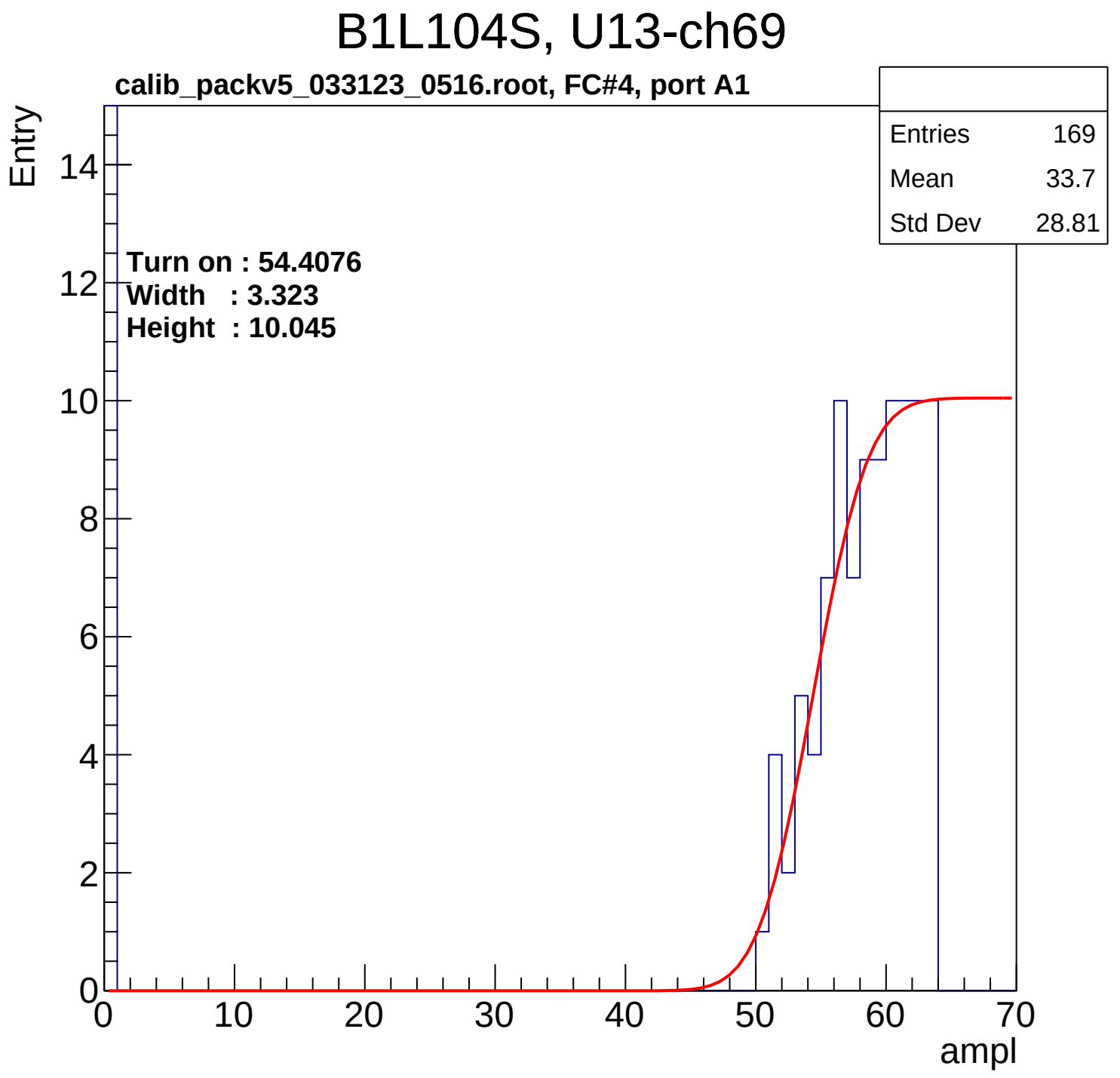

B1L104S, U13-ch68
calib_packv5_033123_0516.root, FC#4, port A1
Entries 188
Mean 27
Std Dev 29.19
Turn on : 55.8141
Width : 3.937
Height : 10.222
Entry
ampl
0
20
40
60
80
100
0
10
20
30
40
50
60
70


B1L104S, U13-ch69
calib_packv5_033123_0516.root, FC#4, port A1
Entries 169
Mean 33.7
Std Dev 28.81
Turn on : 54.4076
Width : 3.323
Height : 10.045
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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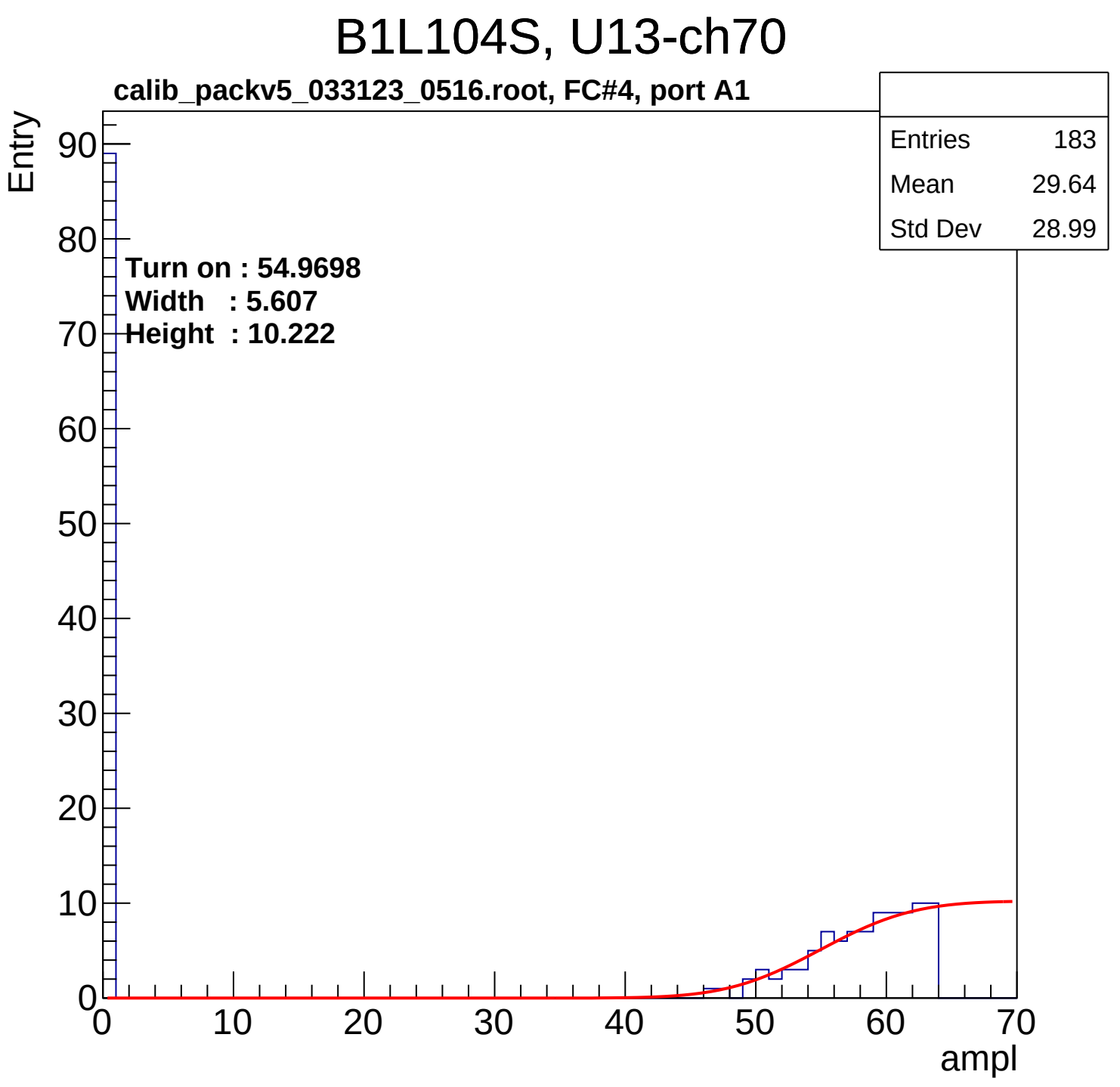
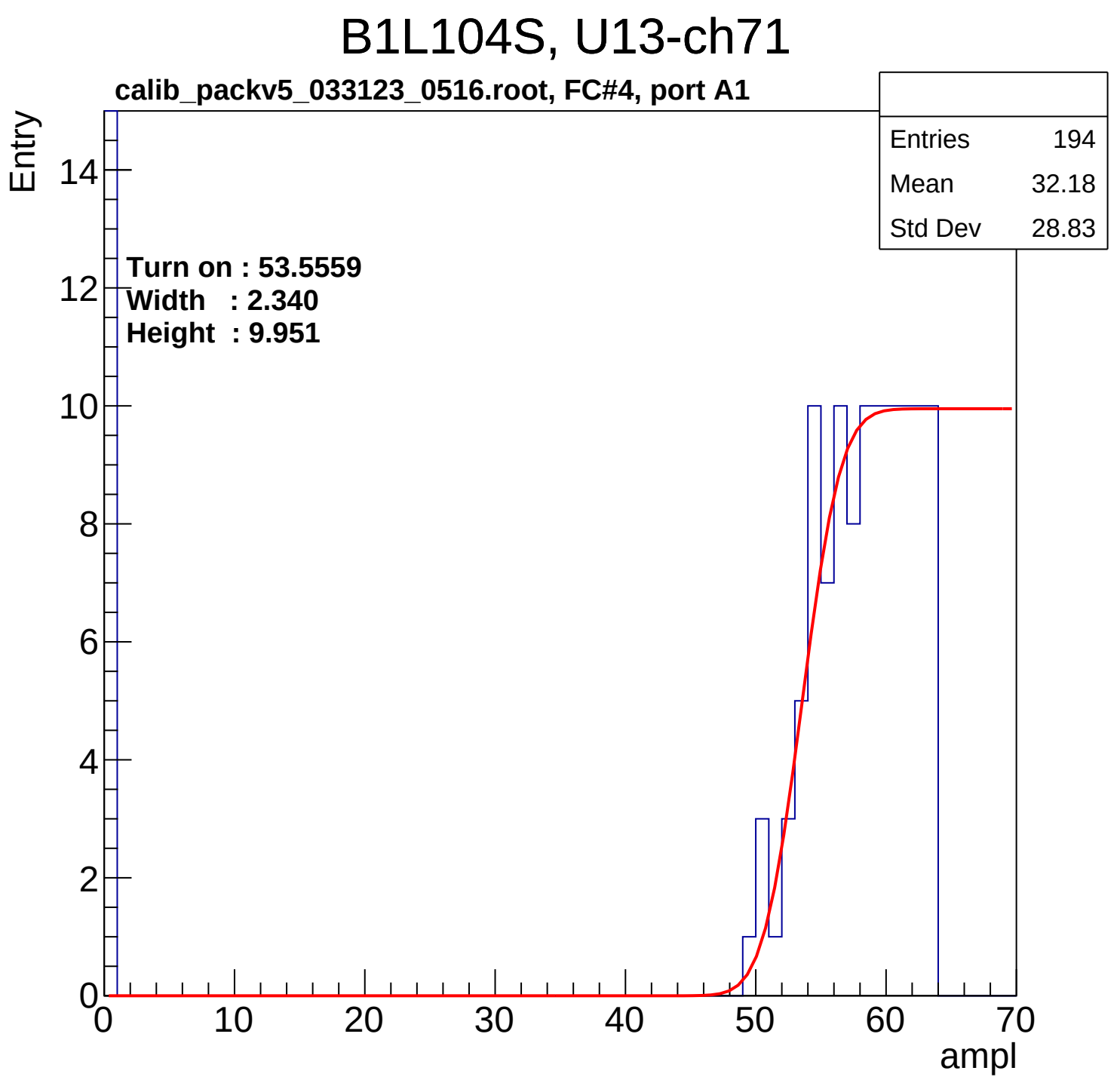

B1L104S, U13-ch70
calib_packv5_033123_0516.root, FC#4, port A1
Entries 183
Mean 29.64
Std Dev 28.99
Turn on : 54.9698
Width : 5.607
Height : 10.222
Entry
ampl
0
10
20
30
40
50
60
70
80
90


B1L104S, U13-ch71
calib_packv5_033123_0516.root, FC#4, port A1
Entries 194
Mean 32.18
Std Dev 28.83
Turn on : 53.5559
Width : 2.340
Height : 9.951
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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40
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60
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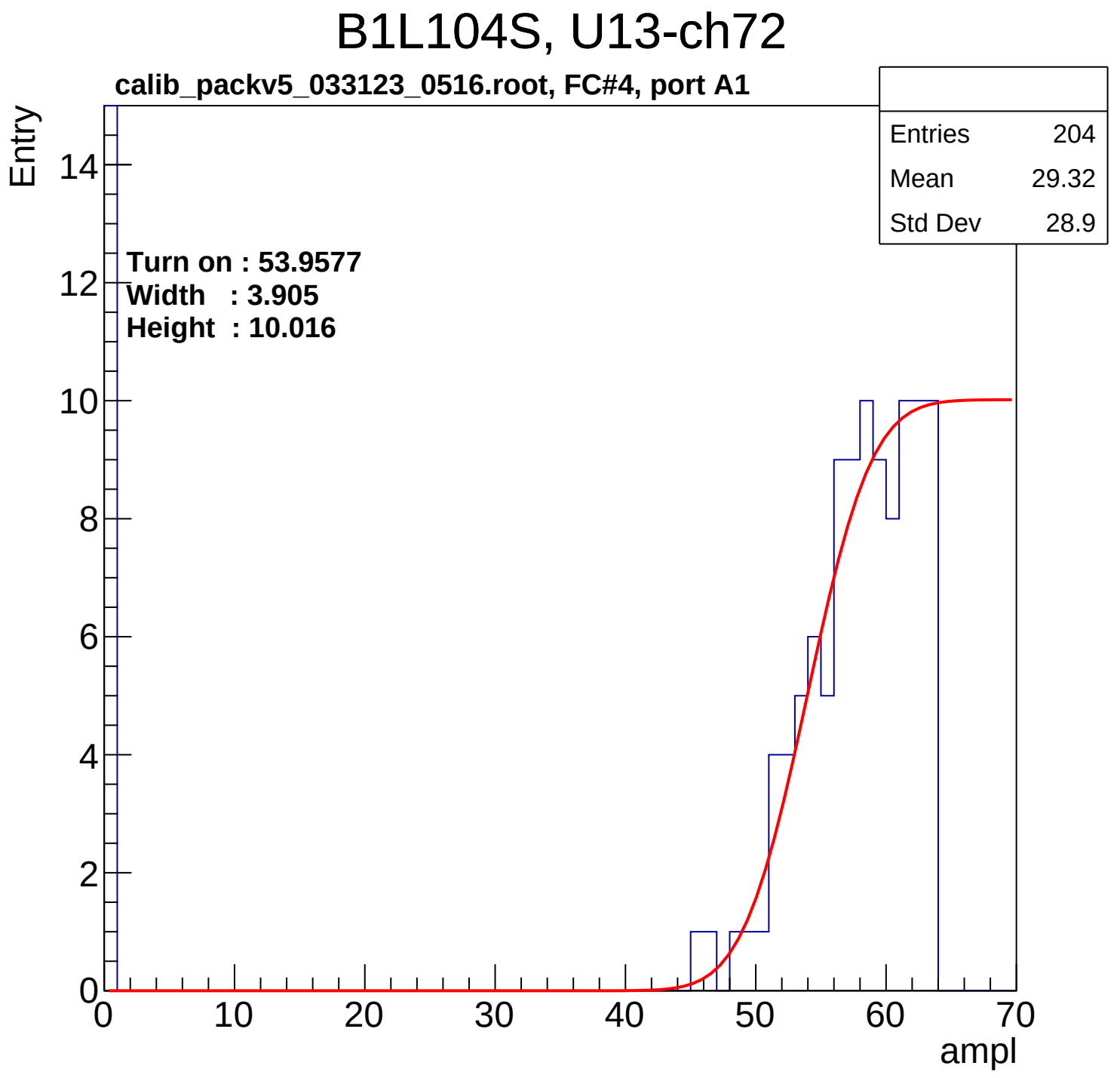
B1L104S, U13-ch72
calib_packv5_033123_0516.root, FC#4, port A1
Entries 204
Mean 29.32
Std Dev 28.9
Turn on : 53.9577
Width : 3.905
Height : 10.016
Entry
ampl
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2
4
6
8
10
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0
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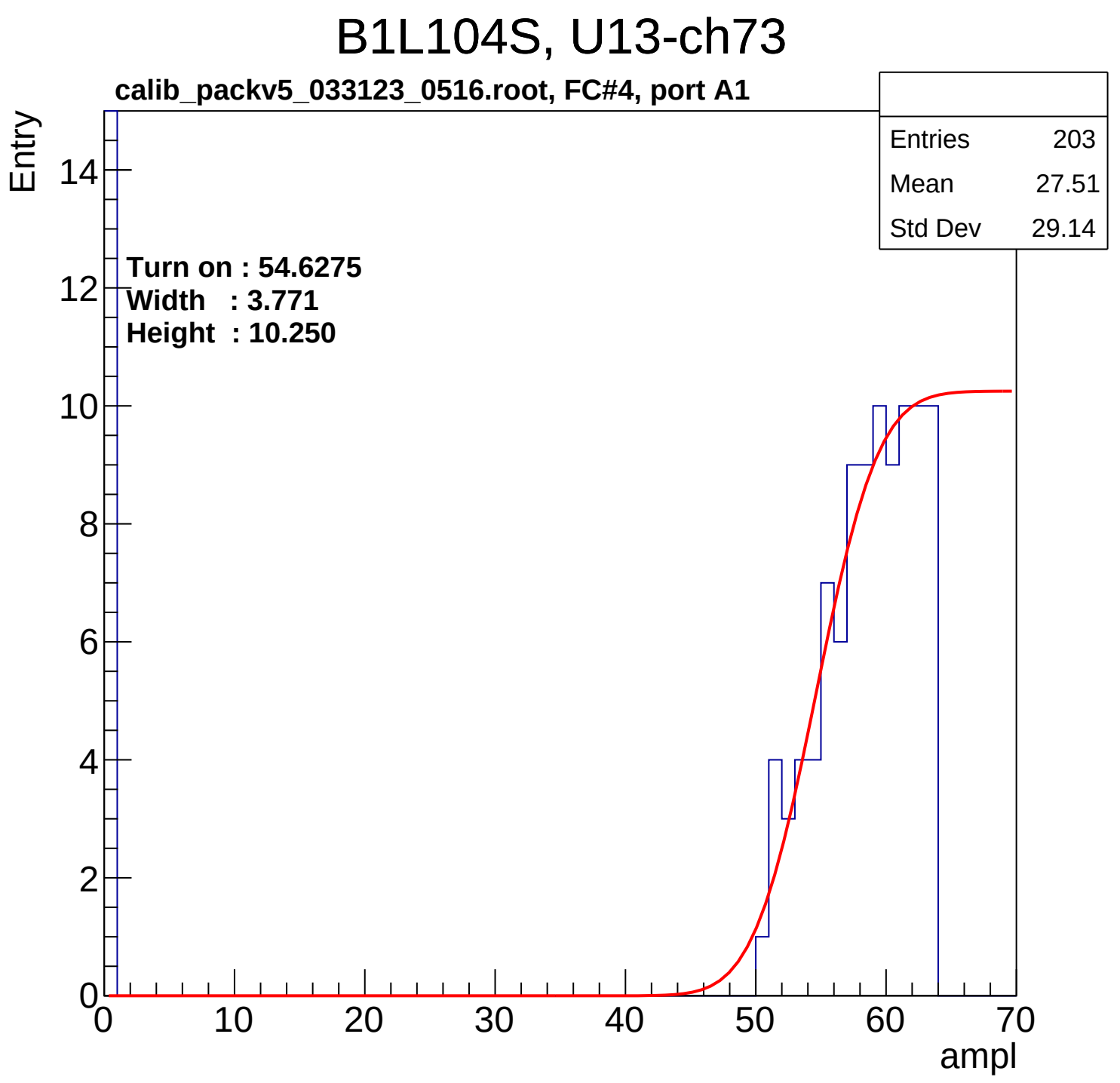
B1L104S, U13-ch73
calib_packv5_033123_0516.root, FC#4, port A1
Entries 203
Mean 27.51
Std Dev 29.14
Turn on : 54.6275
Width : 3.771
Height : 10.250
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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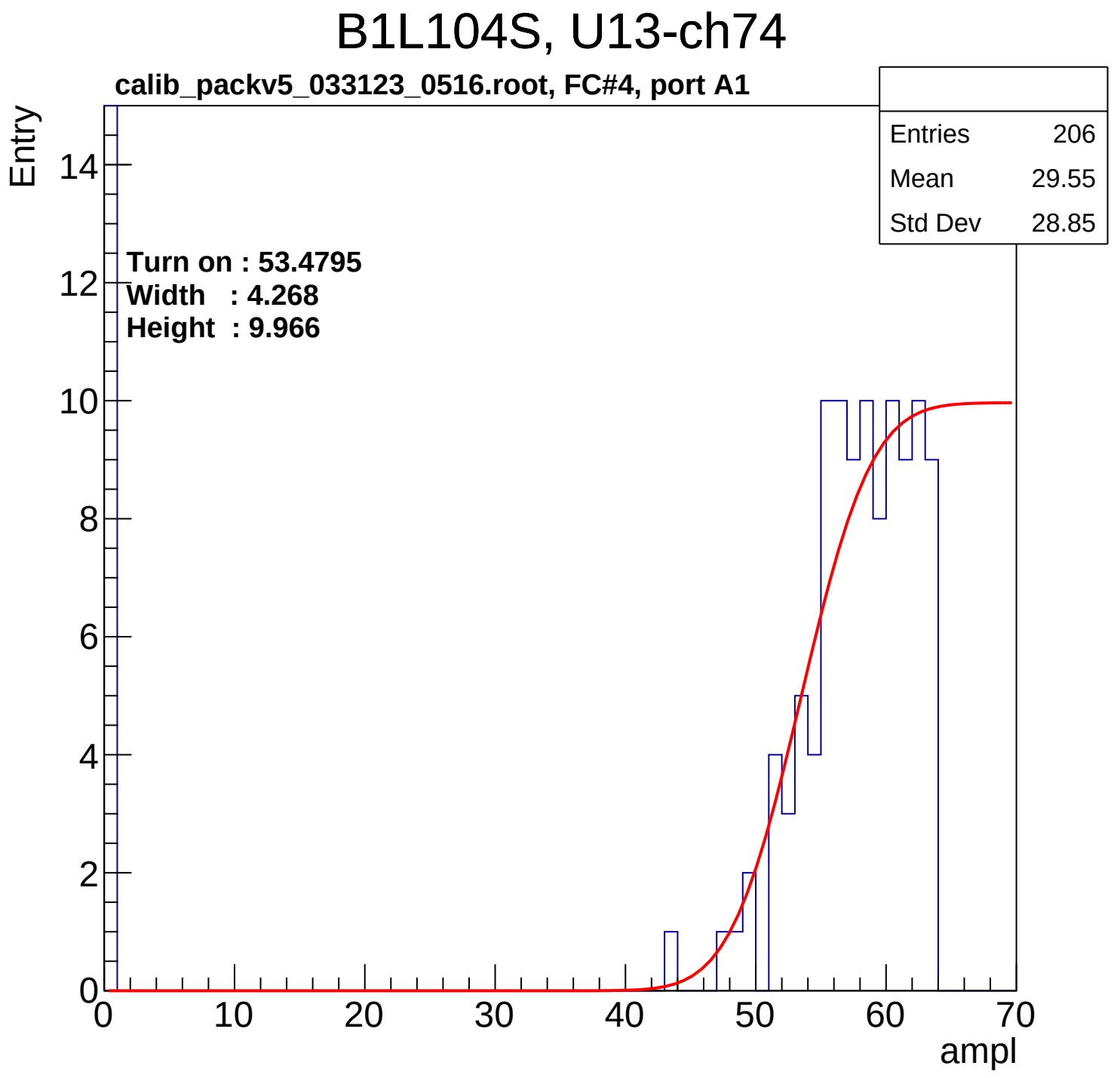
B1L104S, U13-ch74
calib_packv5_033123_0516.root, FC#4, port A1
Entries 206
Mean 29.55
Std Dev 28.85
Turn on : 53.4795
Width : 4.268
Height : 9.966
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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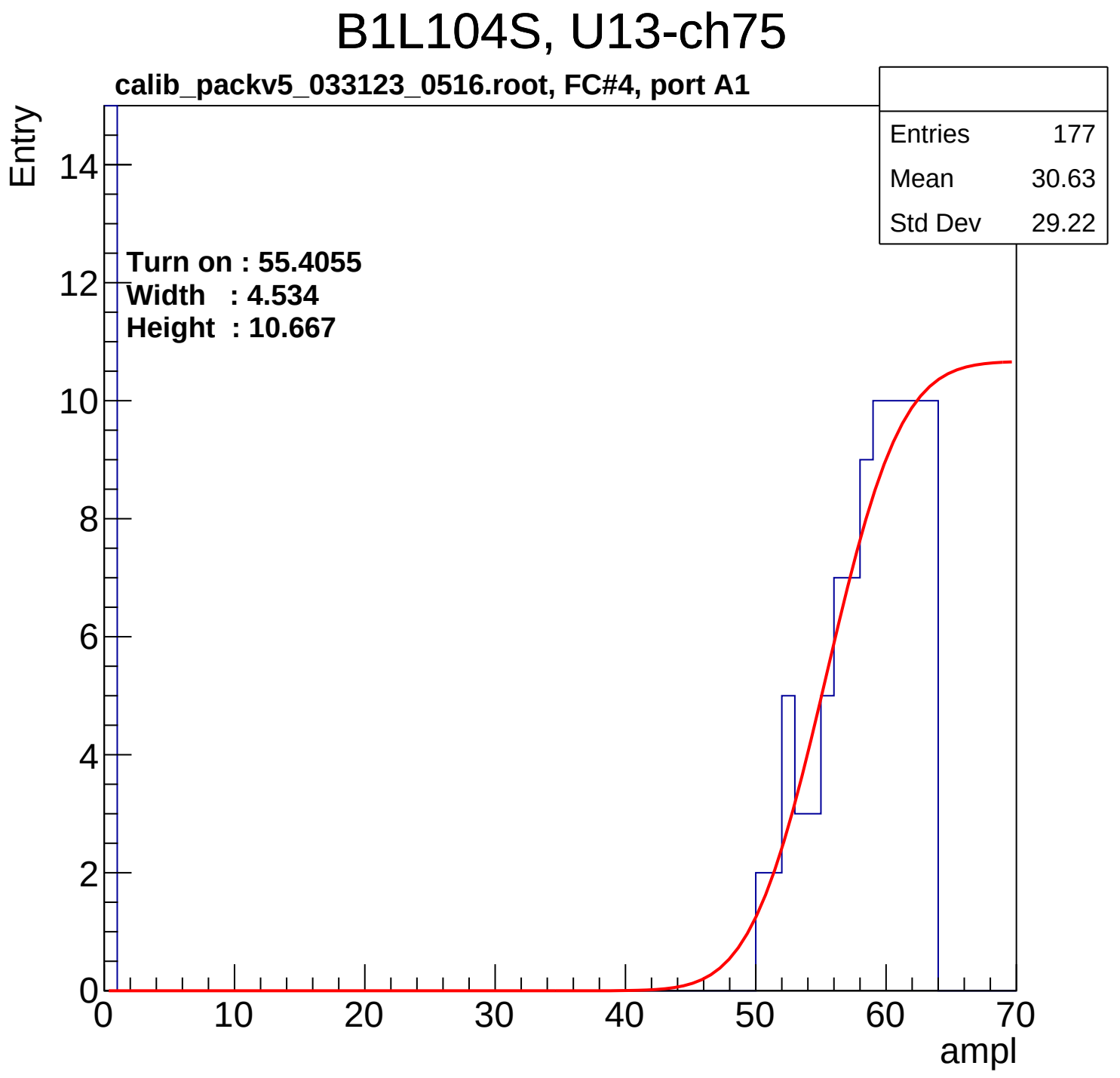
B1L104S, U13-ch75
calib_packv5_033123_0516.root, FC#4, port A1
Entries 177
Mean 30.63
Std Dev 29.22
Turn on : 55.4055
Width : 4.534
Height : 10.667
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
50
60
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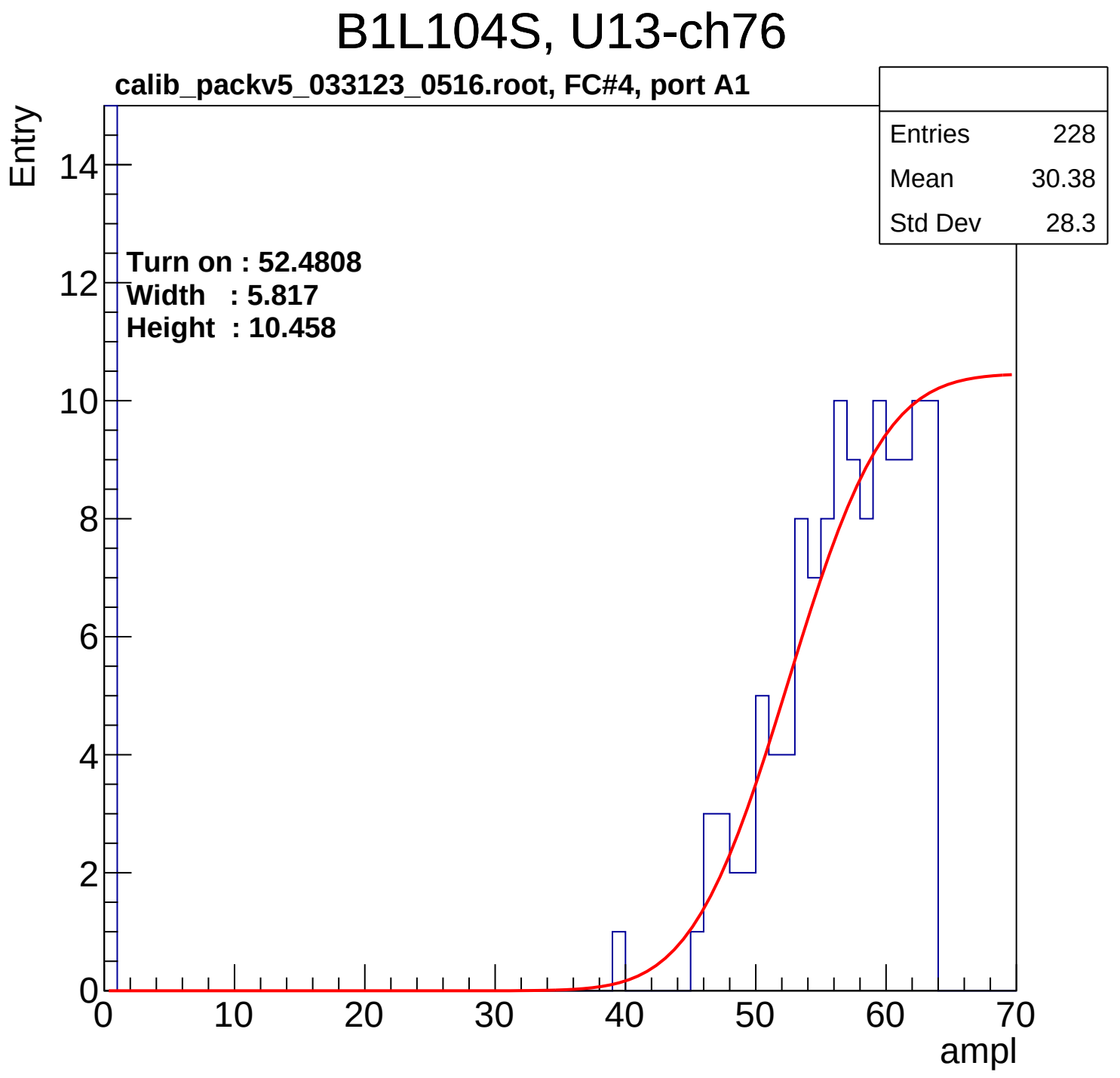
B1L104S, U13-ch76
calib_packv5_033123_0516.root, FC#4, port A1
Entries 228
Mean 30.38
Std Dev 28.3
Turn on : 52.4808
Width : 5.817
Height : 10.458
Entry
ampl
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2
4
6
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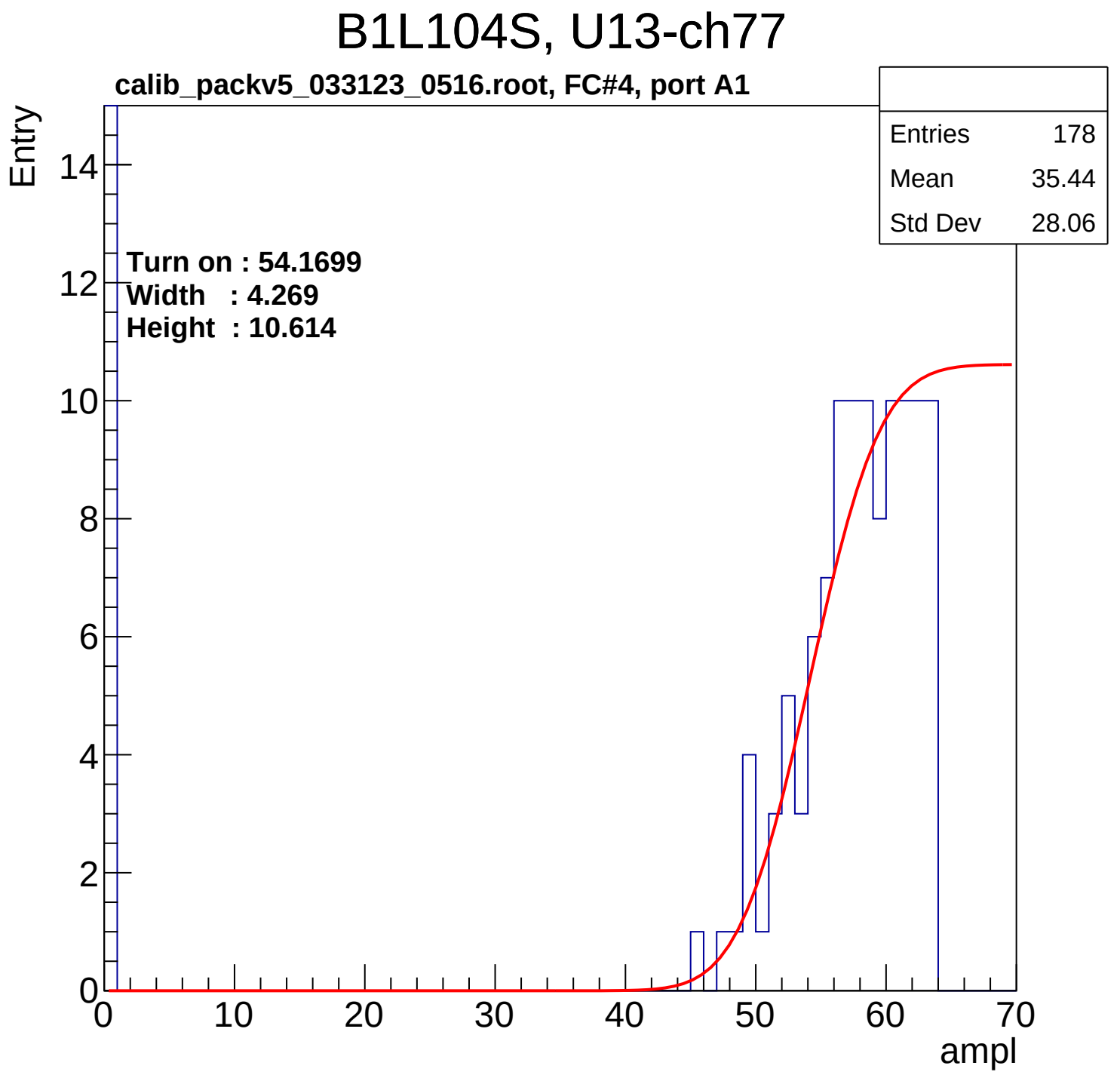
B1L104S, U13-ch77
calib_packv5_033123_0516.root, FC#4, port A1
Entries 178
Mean 35.44
Std Dev 28.06
Turn on : 54.1699
Width : 4.269
Height : 10.614
Entry
ampl
0
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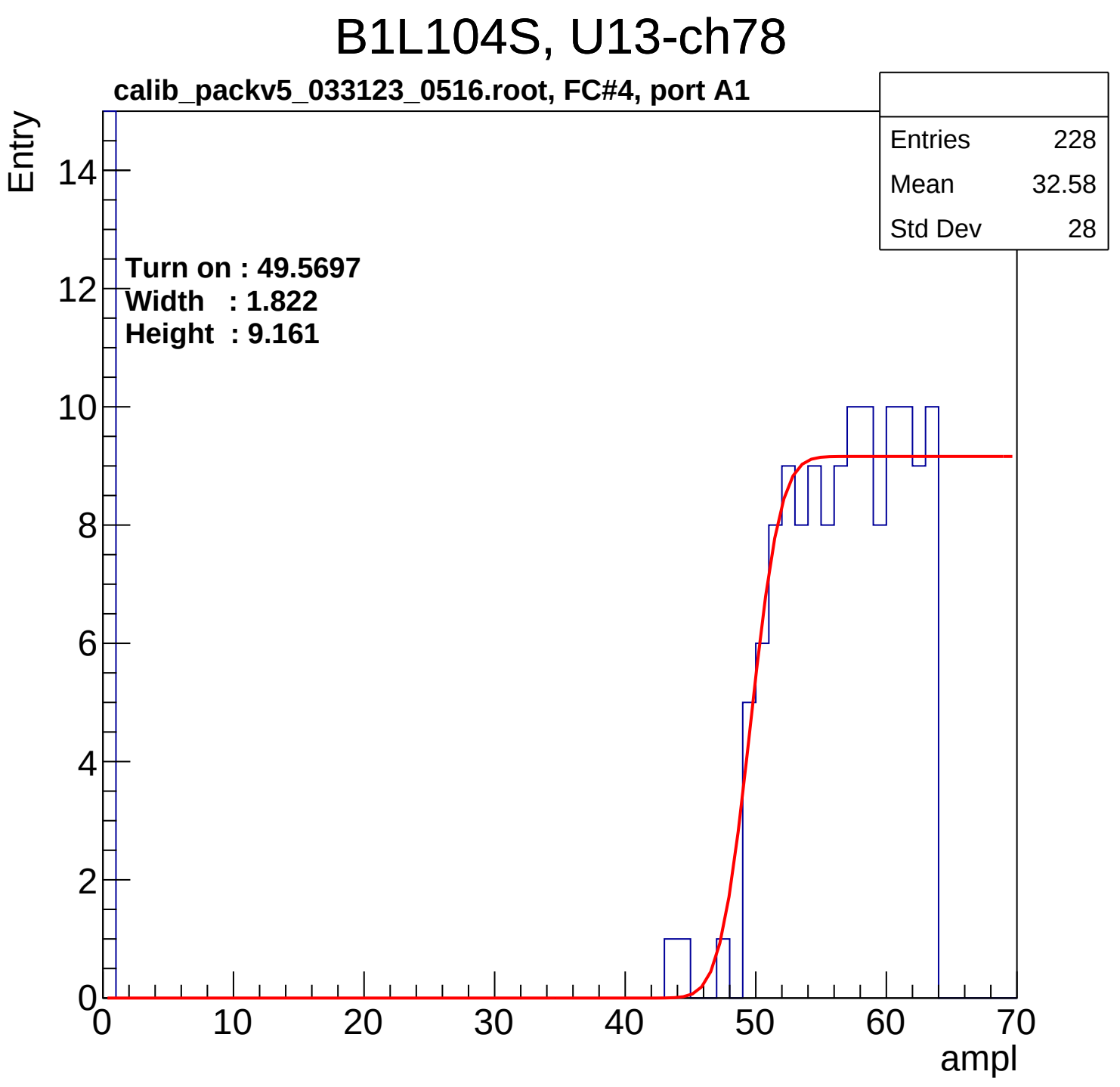
B1L104S, U13-ch78
calib_packv5_033123_0516.root, FC#4, port A1
Entries 228
Mean 32.58
Std Dev 28
Turn on : 49.5697
Width : 1.822
Height : 9.161
Entry
ampl
0
2
4
6
8
10
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0
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60
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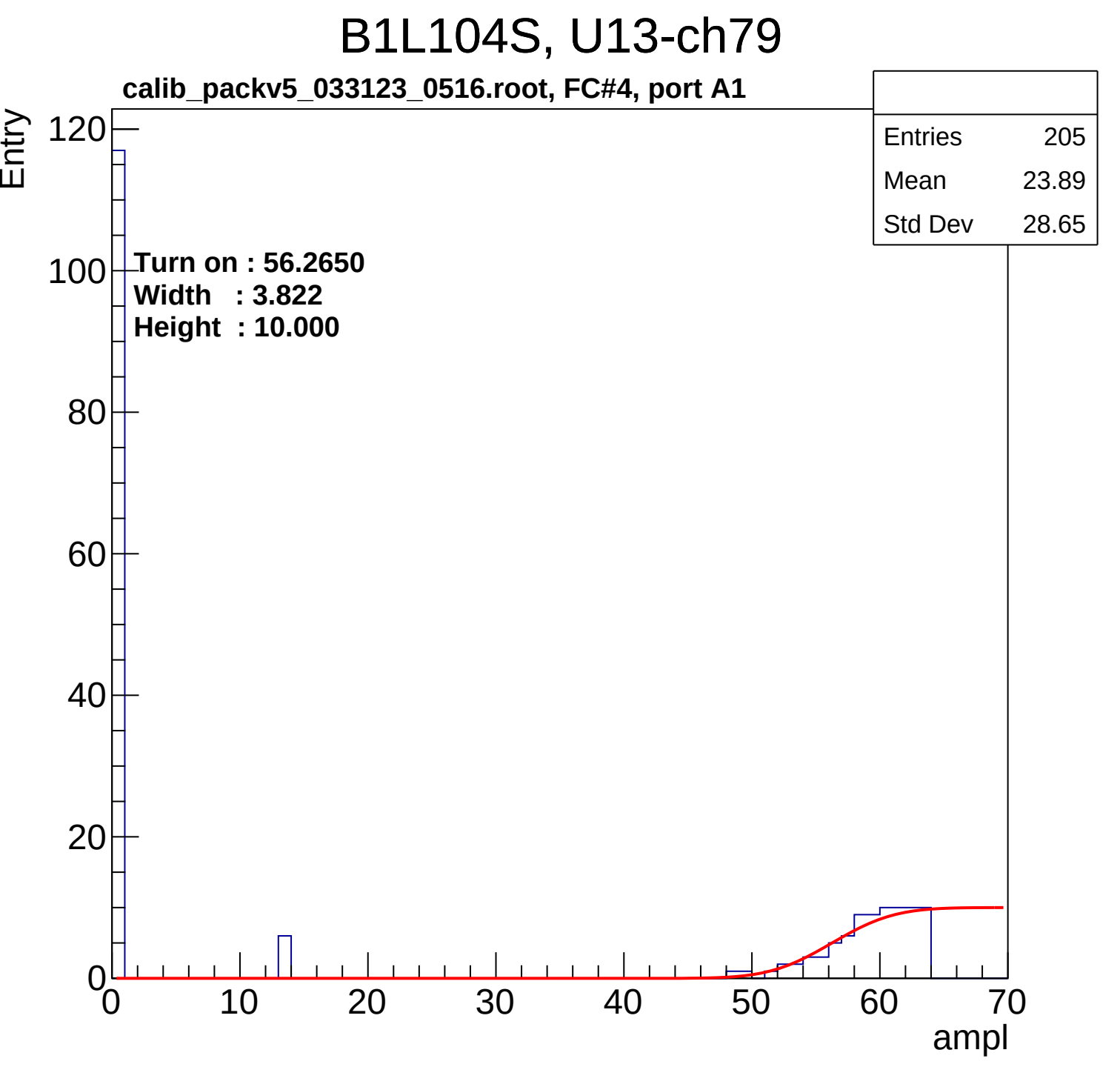
B1L104S, U13-ch79
calib_packv5_033123_0516.root, FC#4, port A1
Entries 205
Mean 23.89
Std Dev 28.65
Turn on : 56.2650
Width : 3.822
Height : 10.000
Entry
120
100
80
60
40
20
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10
20
30
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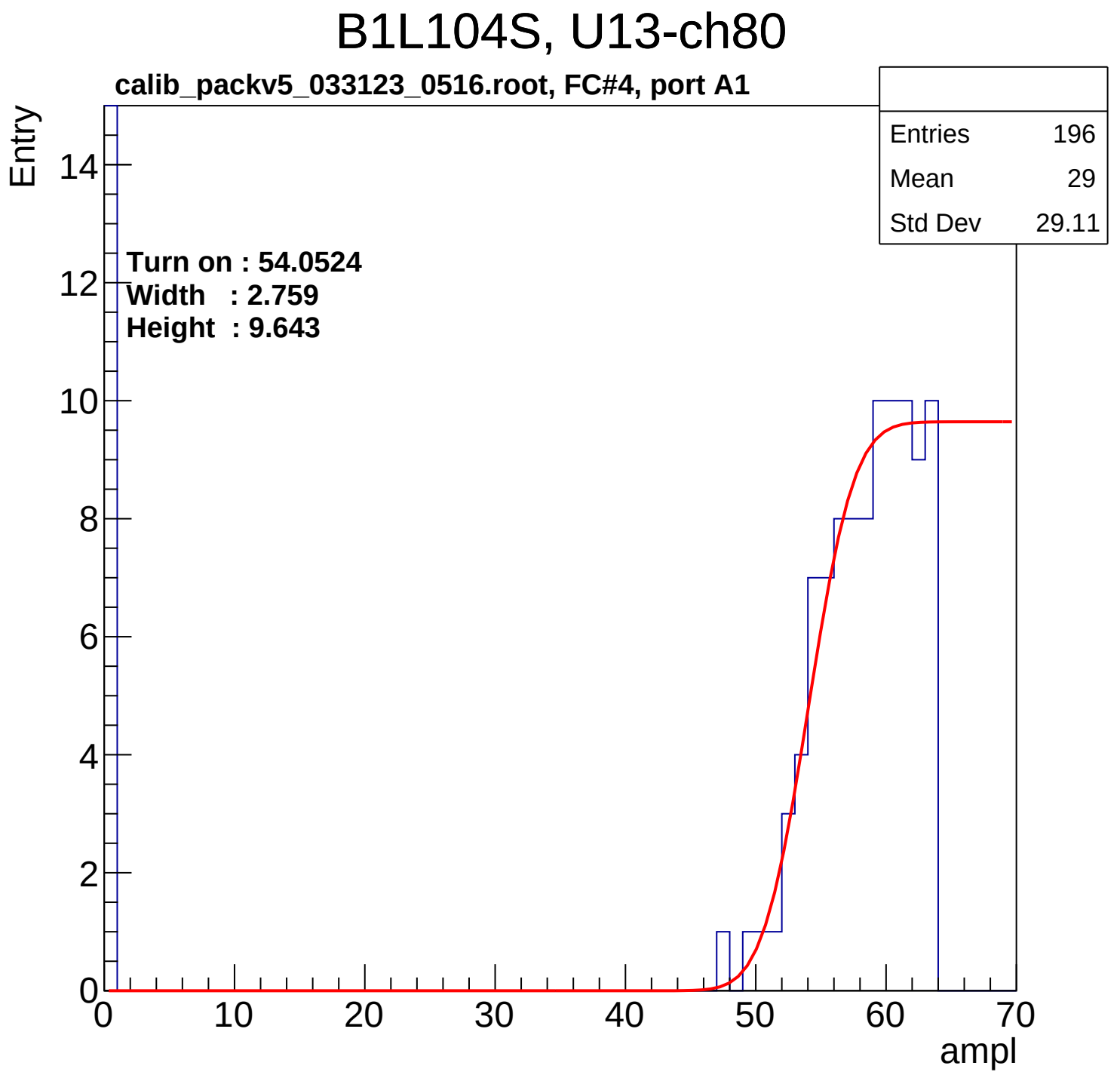
50
60
70
ampl


B1L104S, U13-ch80
calib_packv5_033123_0516.root, FC#4, port A1
Entries 196
Mean 29
Std Dev 29.11
Turn on : 54.0524
Width : 2.759
Height : 9.643
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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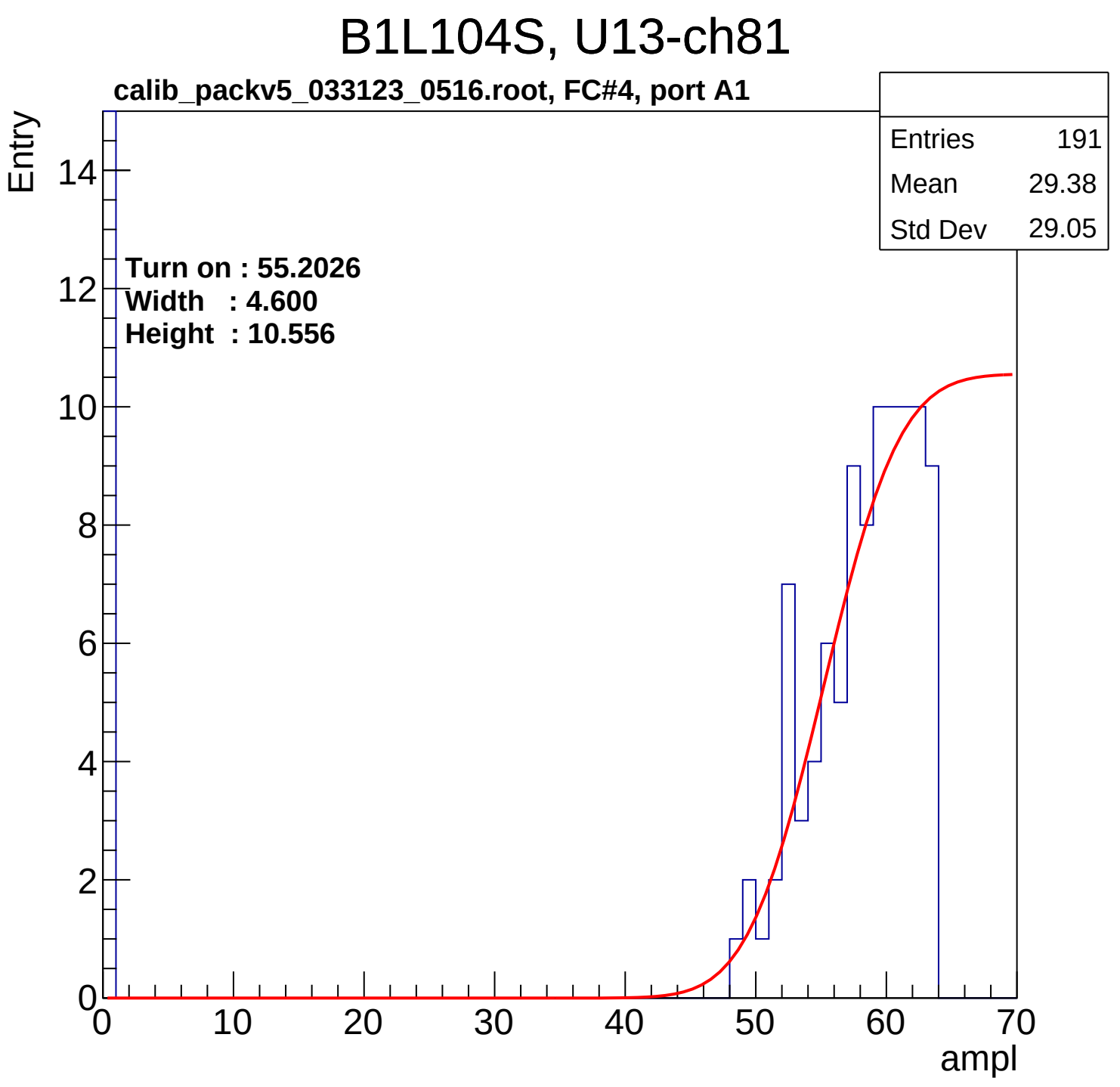
B1L104S, U13-ch81
calib_packv5_033123_0516.root, FC#4, port A1
Entries 191
Mean 29.38
Std Dev 29.05
Turn on : 55.2026
Width : 4.600
Height : 10.556
Entry
ampl
0
2
4
6
8
10
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0
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40
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60
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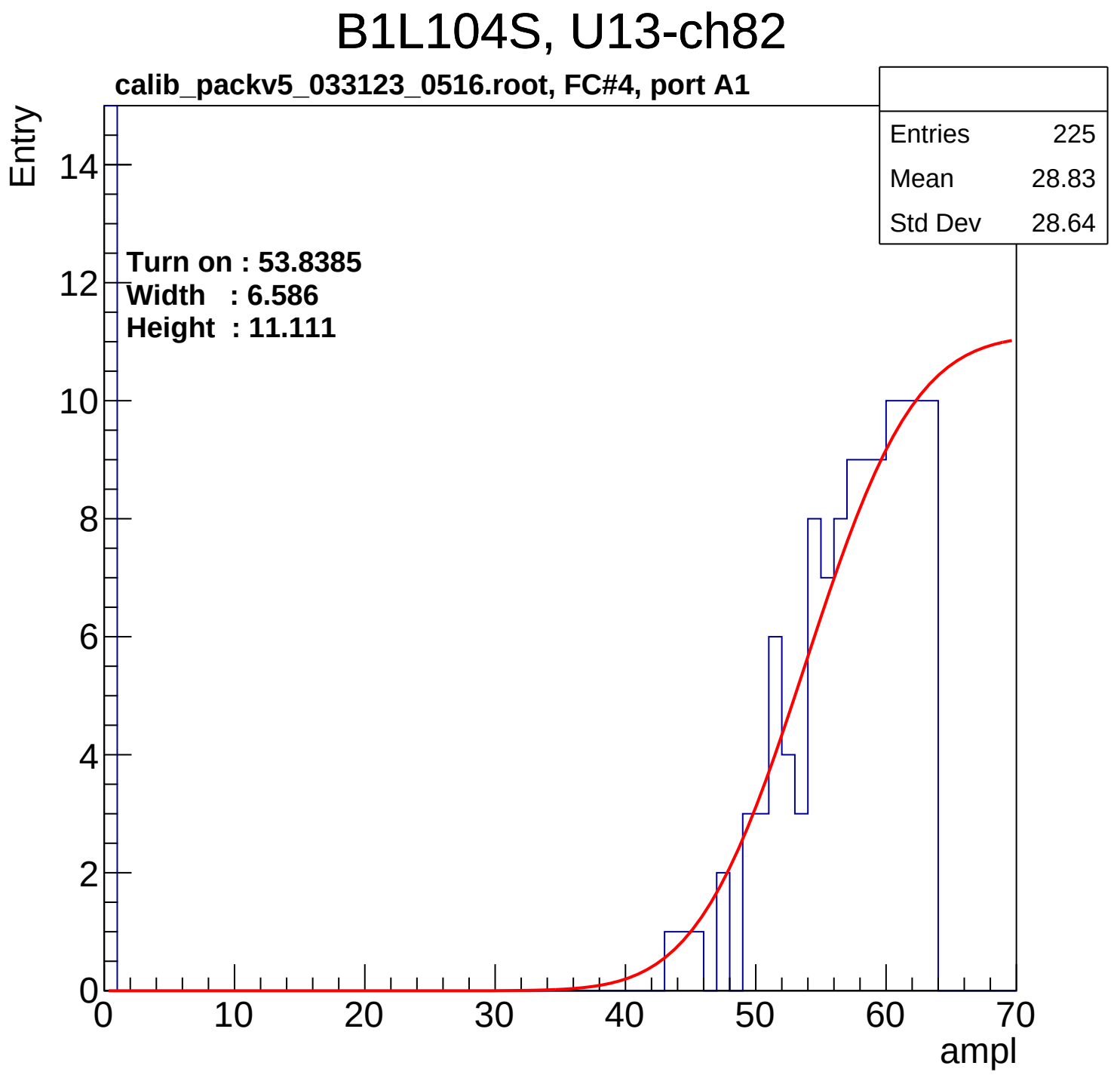
B1L104S, U13-ch82
calib_packv5_033123_0516.root, FC#4, port A1
Entries 225
Mean 28.83
Std Dev 28.64
Turn on : 53.8385
Width : 6.586
Height : 11.111
Entry
ampl
0
2
4
6
8
10
12
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0
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20
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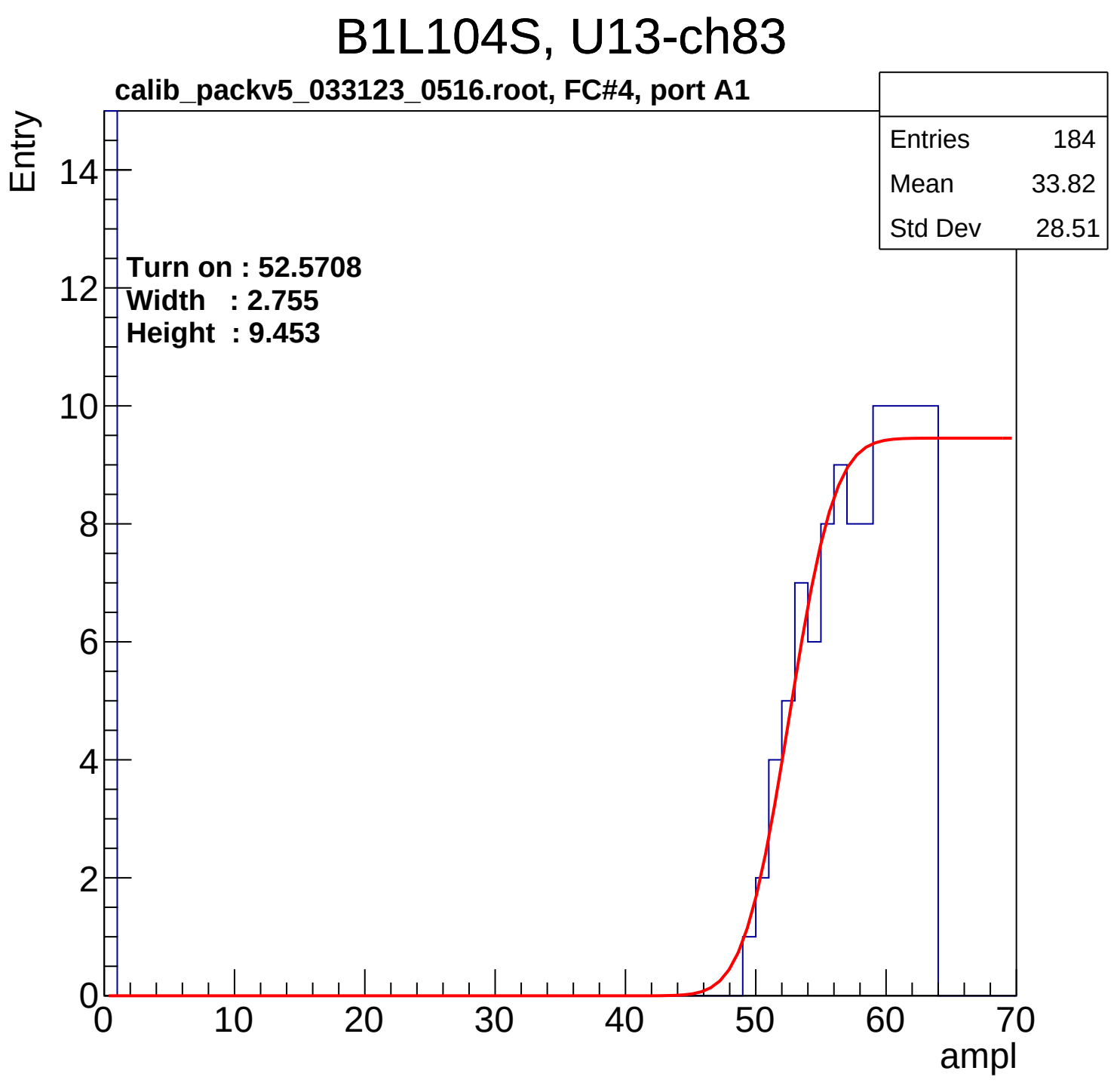
B1L104S, U13-ch83
calib_packv5_033123_0516.root, FC#4, port A1
Entries 184
Mean 33.82
Std Dev 28.51
Turn on : 52.5708
Width : 2.755
Height : 9.453
Entry
ampl
0
2
4
6
8
10
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60
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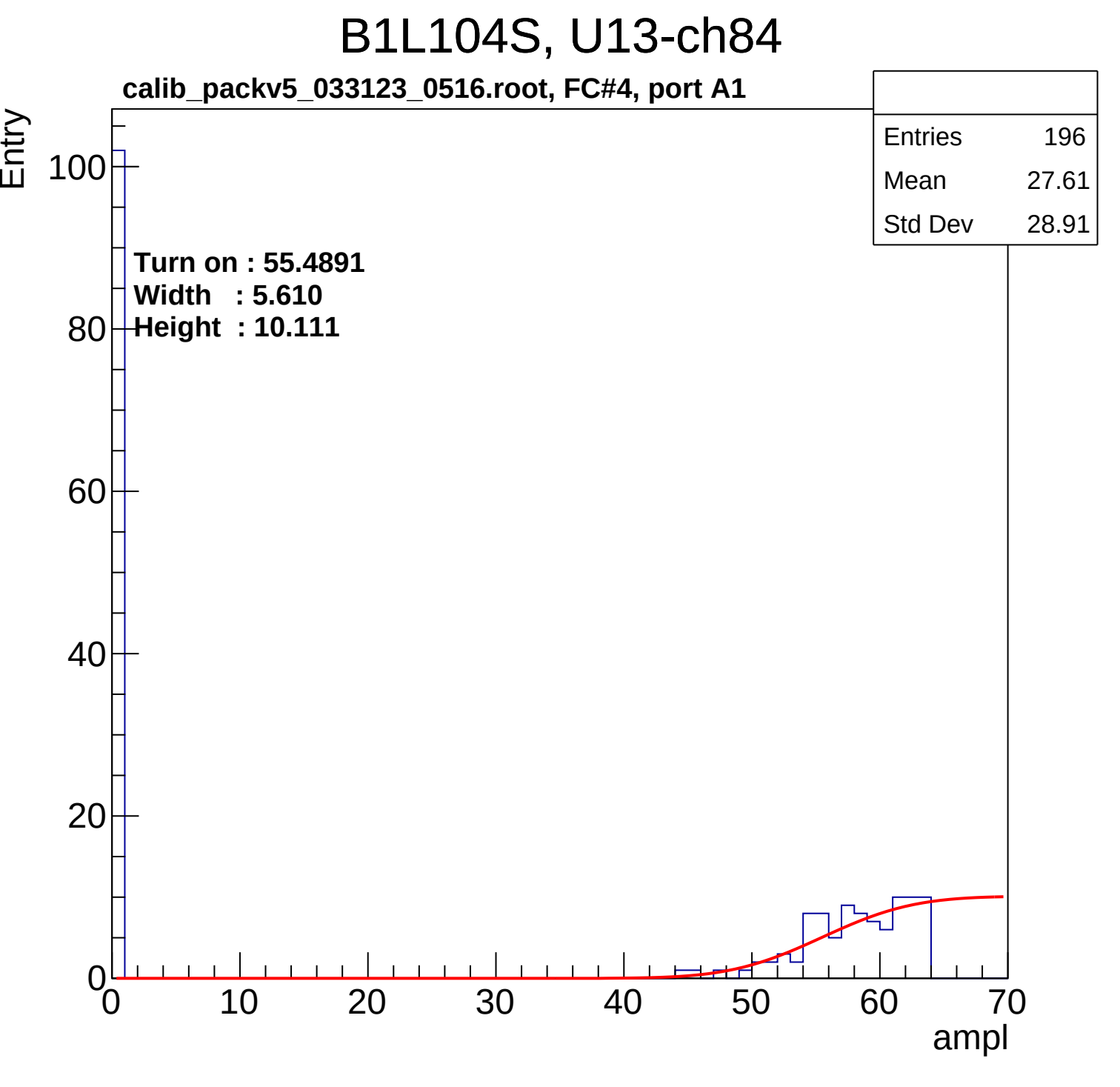
B1L104S, U13-ch84
calib_packv5_033123_0516.root, FC#4, port A1
Entries 196
Mean 27.61
Std Dev 28.91
Turn on : 55.4891
Width : 5.610
Height : 10.111
Entry
ampl
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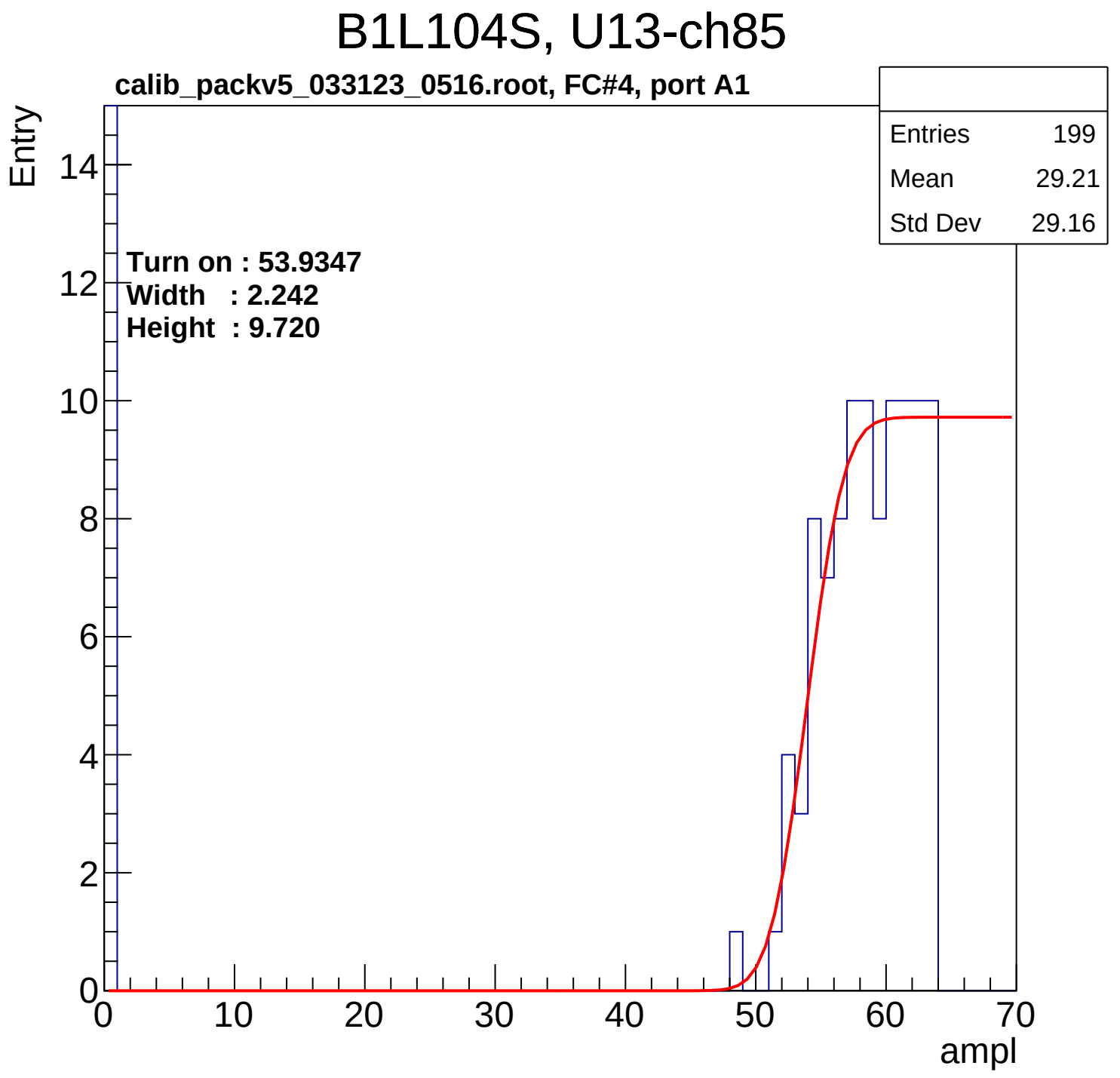
B1L104S, U13-ch85
calib_packv5_033123_0516.root, FC#4, port A1
Entries 199
Mean 29.21
Std Dev 29.16
Turn on : 53.9347
Width : 2.242
Height : 9.720
Entry
ampl
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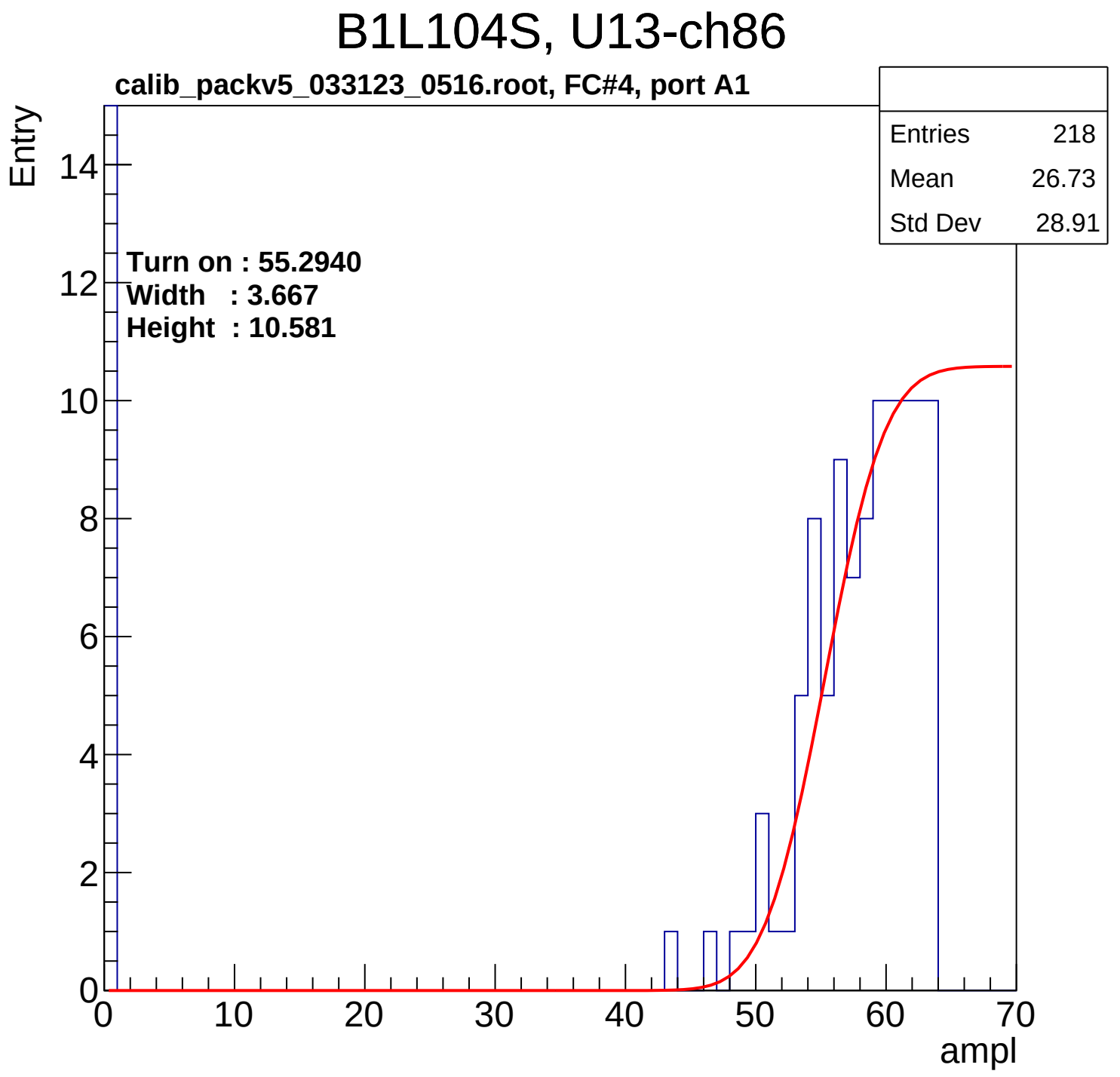
B1L104S, U13-ch86
calib_packv5_033123_0516.root, FC#4, port A1
Entries 218
Mean 26.73
Std Dev 28.91
Turn on : 55.2940
Width : 3.667
Height : 10.581
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
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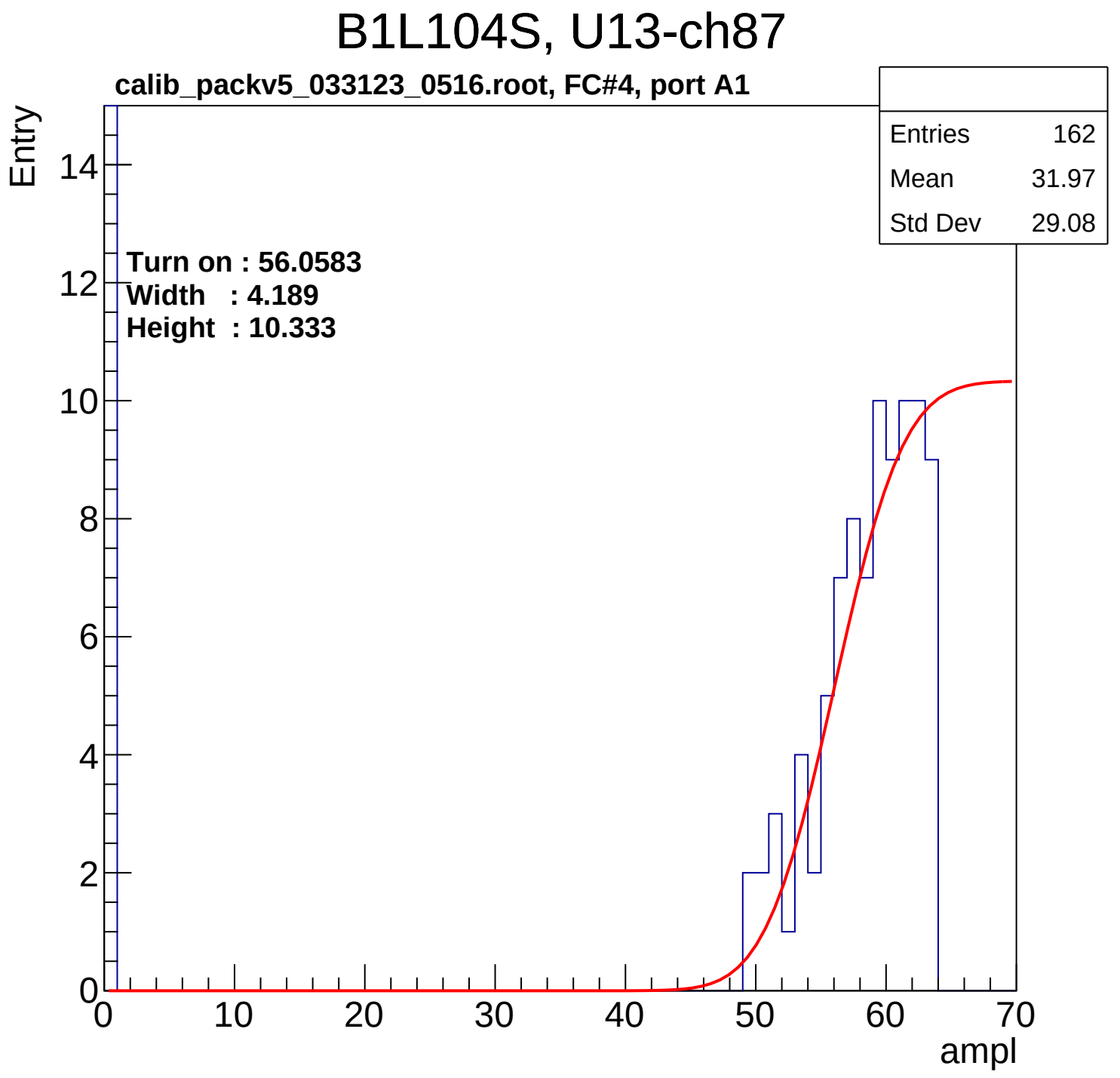
B1L104S, U13-ch87
calib_packv5_033123_0516.root, FC#4, port A1
Entries 162
Mean 31.97
Std Dev 29.08
Turn on : 56.0583
Width : 4.189
Height : 10.333
Entry
ampl
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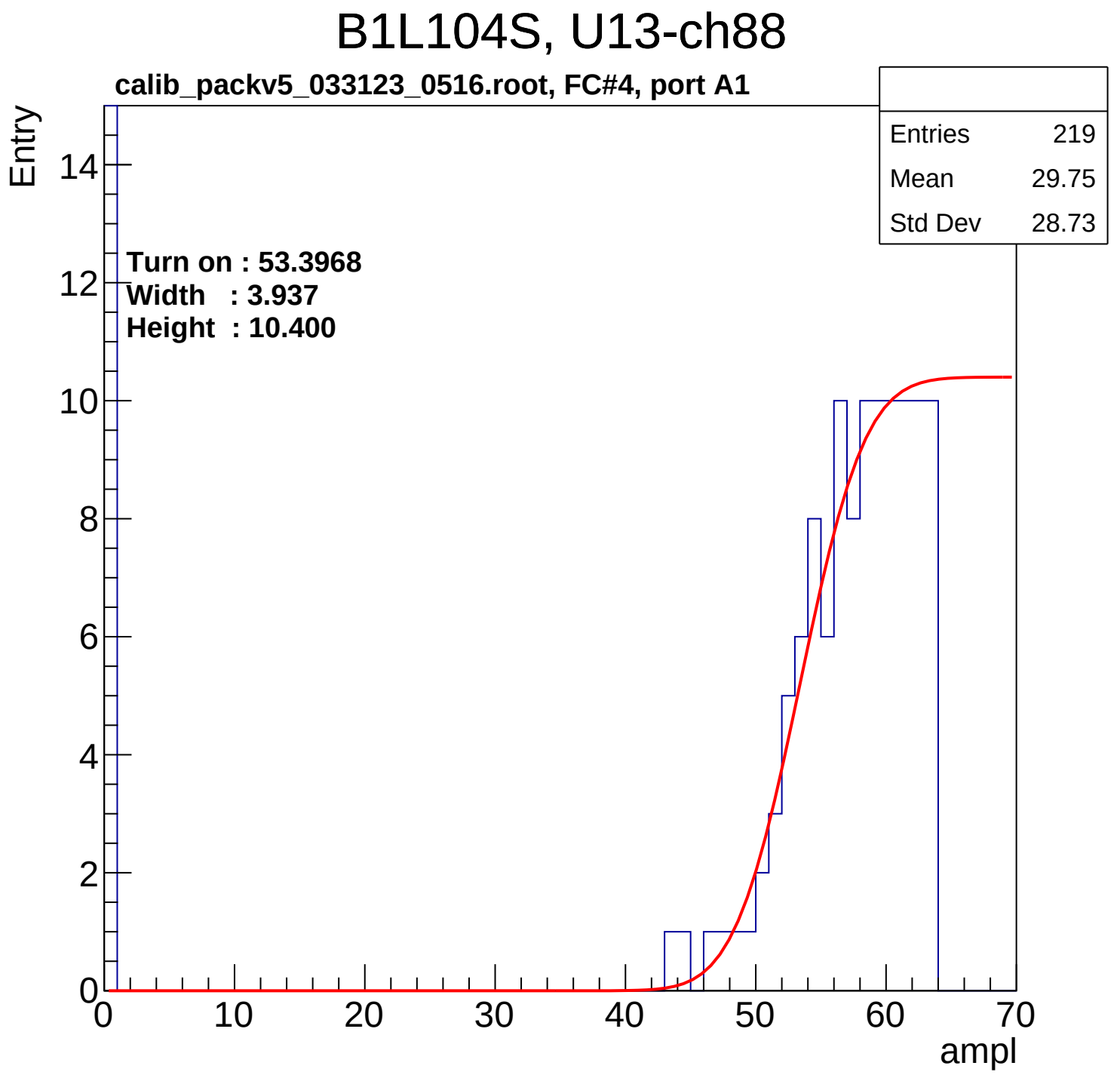
B1L104S, U13-ch88
calib_packv5_033123_0516.root, FC#4, port A1
Entries 219
Mean 29.75
Std Dev 28.73
Turn on : 53.3968
Width : 3.937
Height : 10.400
Entry
ampl
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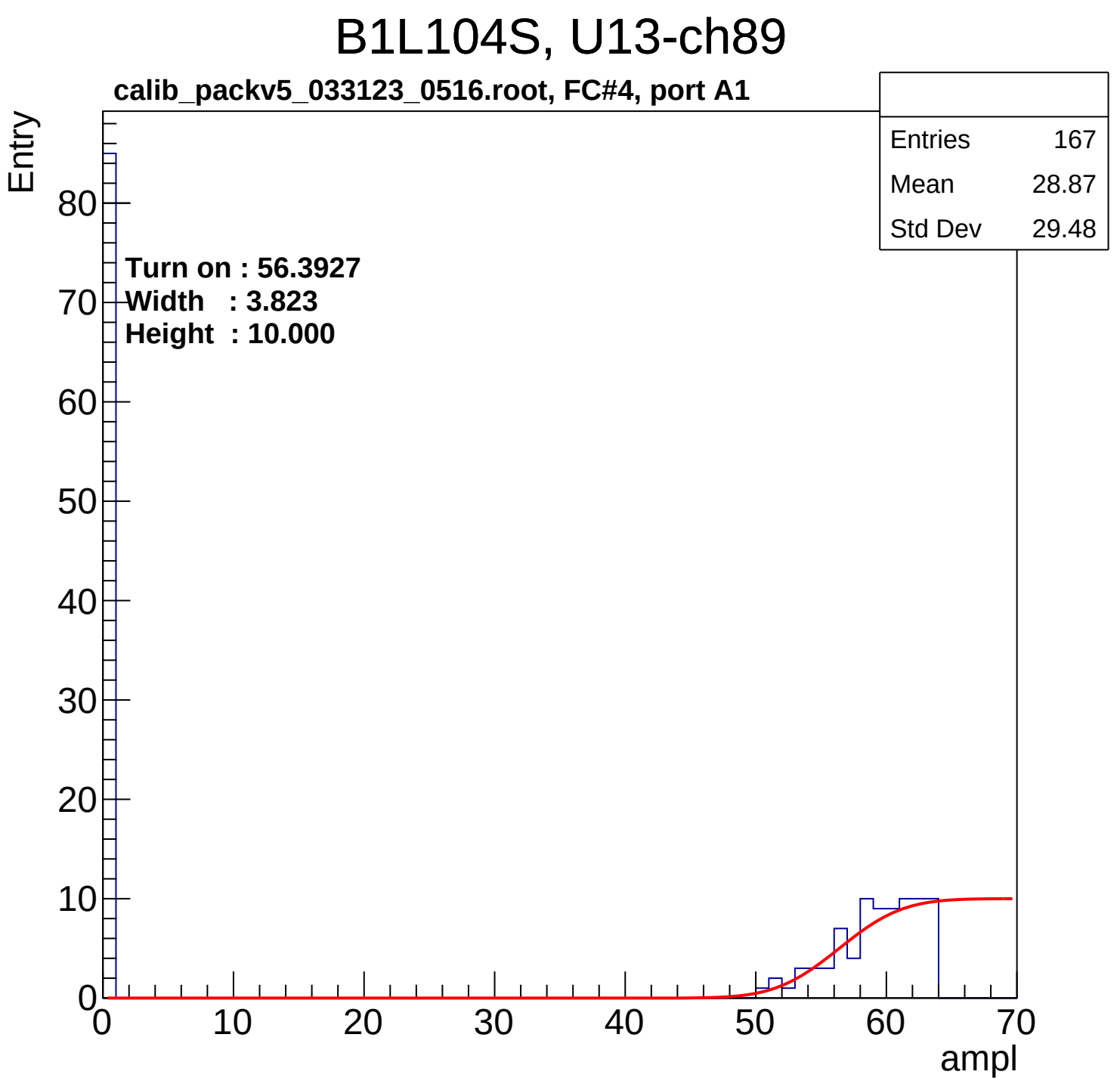
B1L104S, U13-ch89
calib_packv5_033123_0516.root, FC#4, port A1
Entries 167
Mean 28.87
Std Dev 29.48
Turn on : 56.3927
Width : 3.823
Height : 10.000
Entry
ampl
0
10
20
30
40
50
60
70
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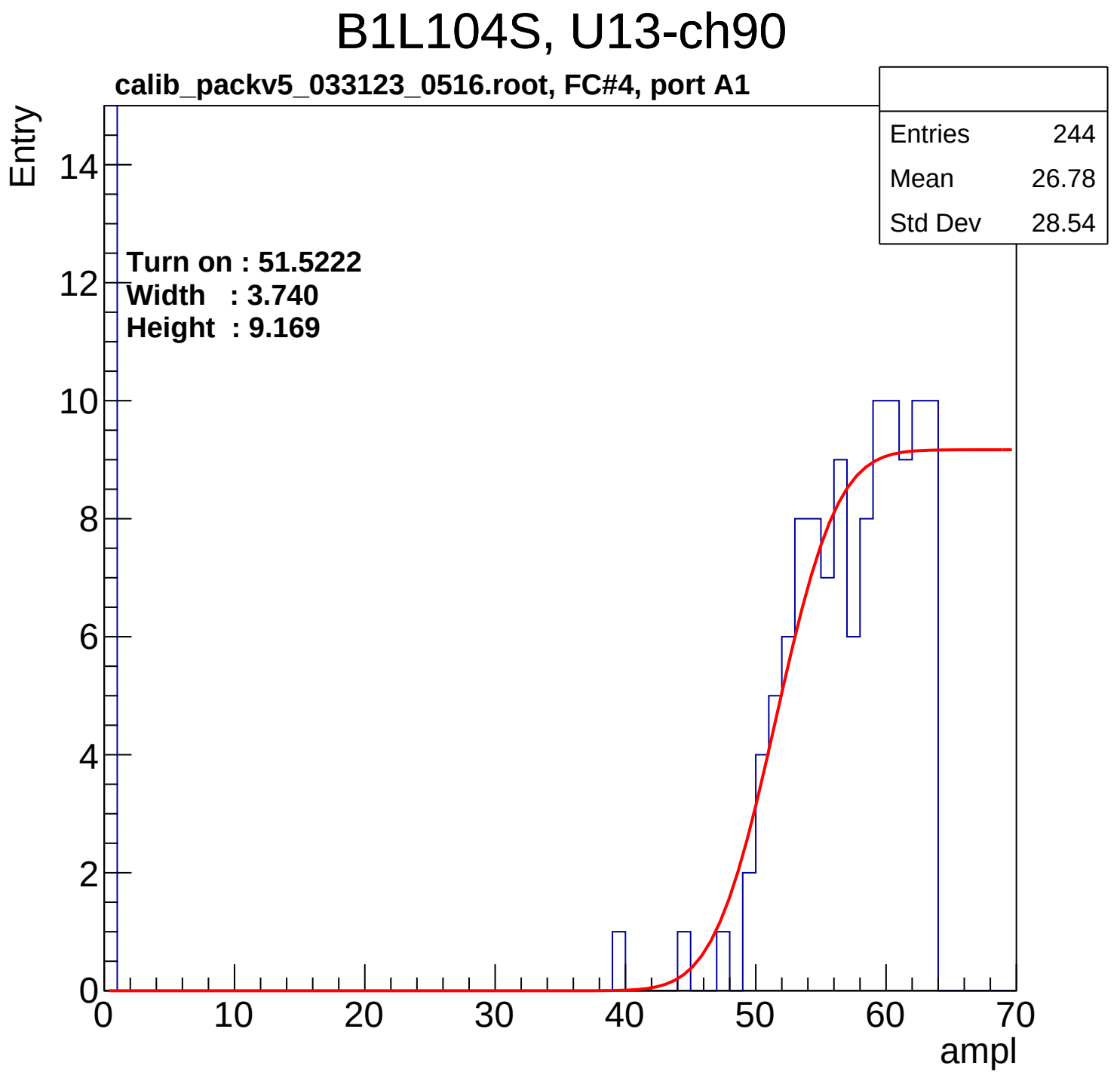
B1L104S, U13-ch90
calib_packv5_033123_0516.root, FC#4, port A1
Entries 244
Mean 26.78
Std Dev 28.54
Turn on : 51.5222
Width : 3.740
Height : 9.169
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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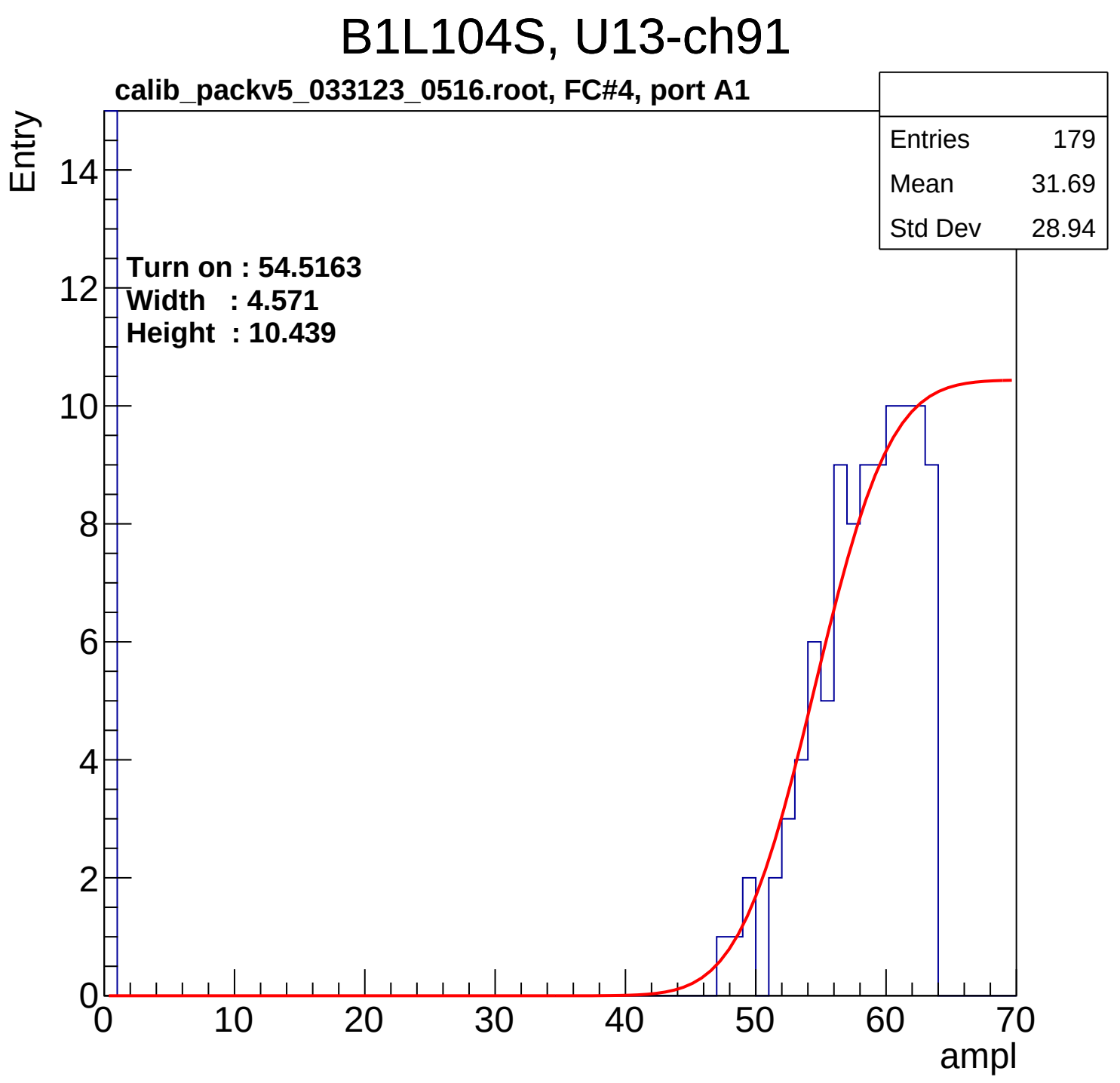
B1L104S, U13-ch91
calib_packv5_033123_0516.root, FC#4, port A1
Entries 179
Mean 31.69
Std Dev 28.94
Turn on : 54.5163
Width : 4.571
Height : 10.439
Entry
ampl
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4
6
8
10
12
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0
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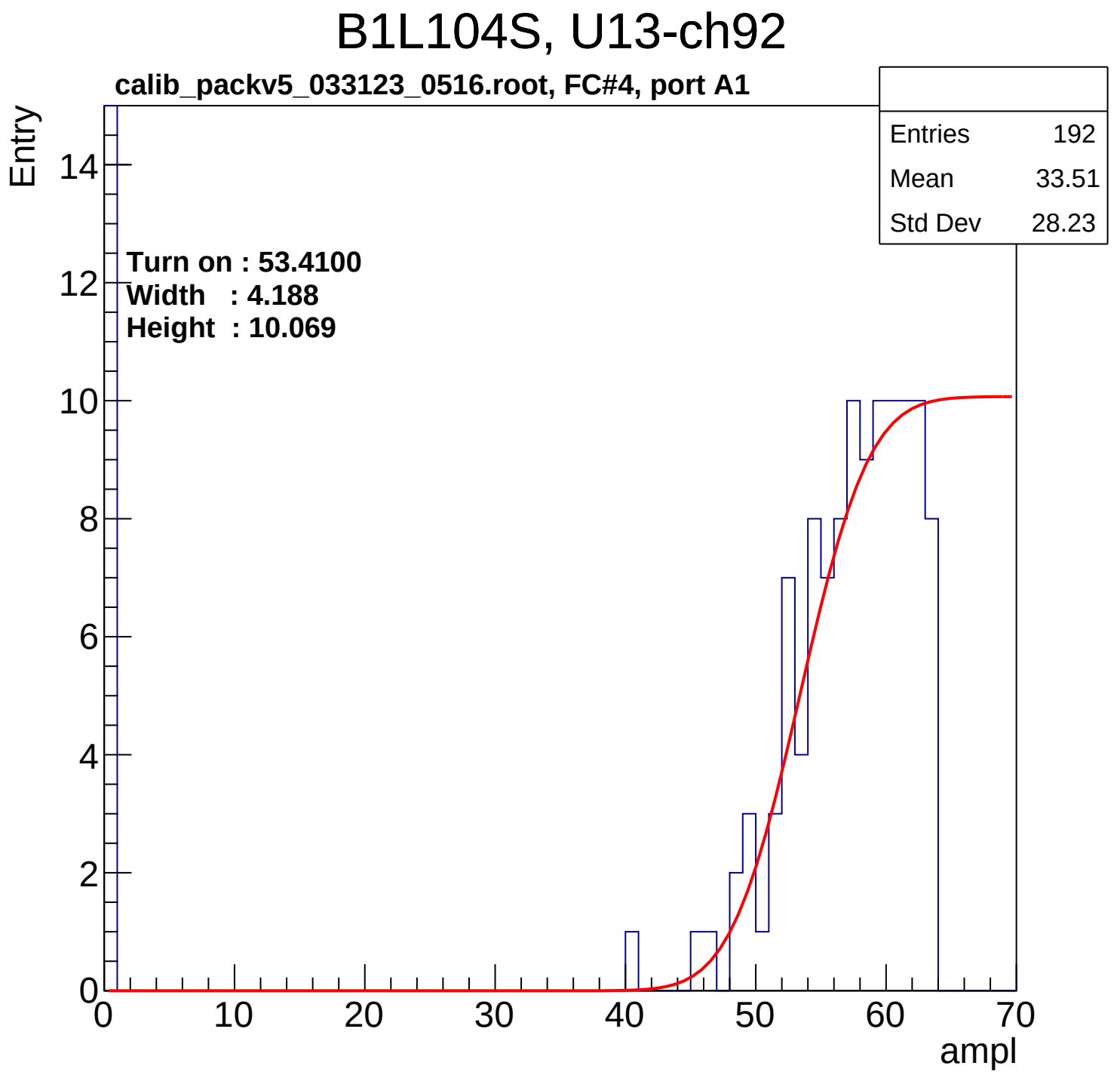
B1L104S, U13-ch92
calib_packv5_033123_0516.root, FC#4, port A1
Entries 192
Mean 33.51
Std Dev 28.23
Turn on : 53.4100
Width : 4.188
Height : 10.069
Entry
ampl
0
2
4
6
8
10
12
14
0
10
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40
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60
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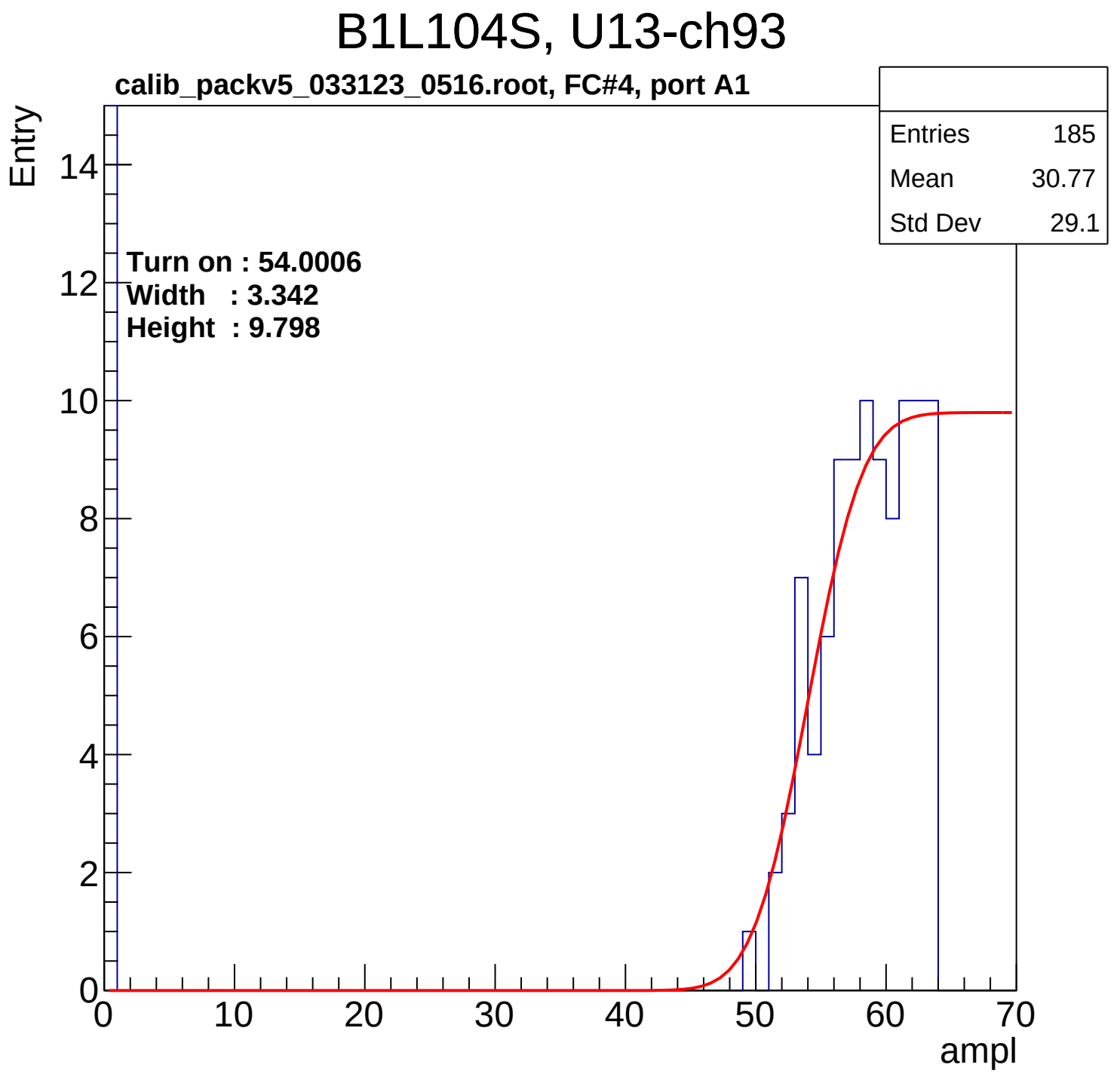
B1L104S, U13-ch93
calib_packv5_033123_0516.root, FC#4, port A1
Entries 185
Mean 30.77
Std Dev 29.1
Turn on : 54.0006
Width : 3.342
Height : 9.798
Entry
ampl
0
2
4
6
8
10
12
14
0
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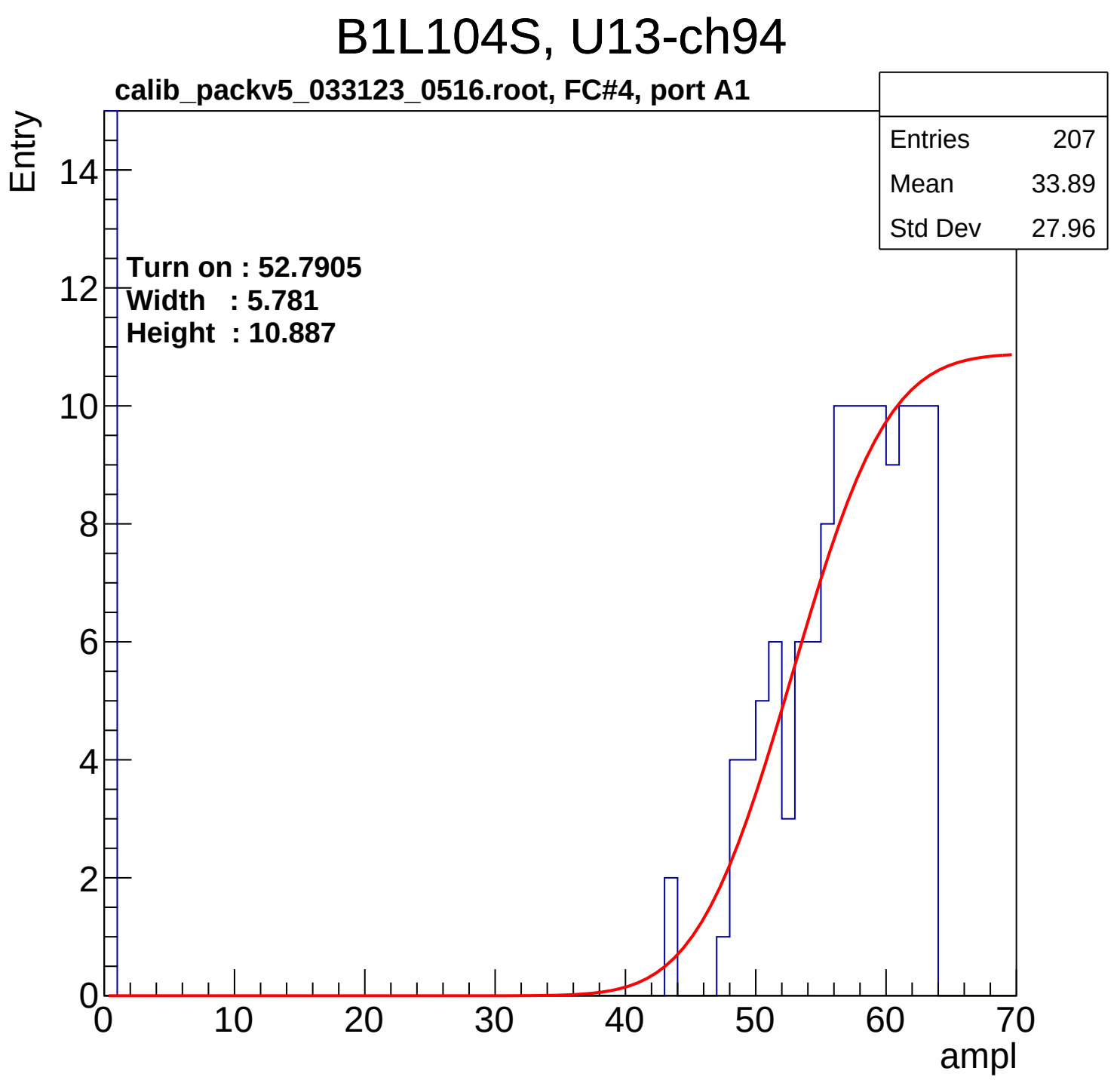
B1L104S, U13-ch94
calib_packv5_033123_0516.root, FC#4, port A1
Entries 207
Mean 33.89
Std Dev 27.96
Turn on : 52.7905
Width : 5.781
Height : 10.887
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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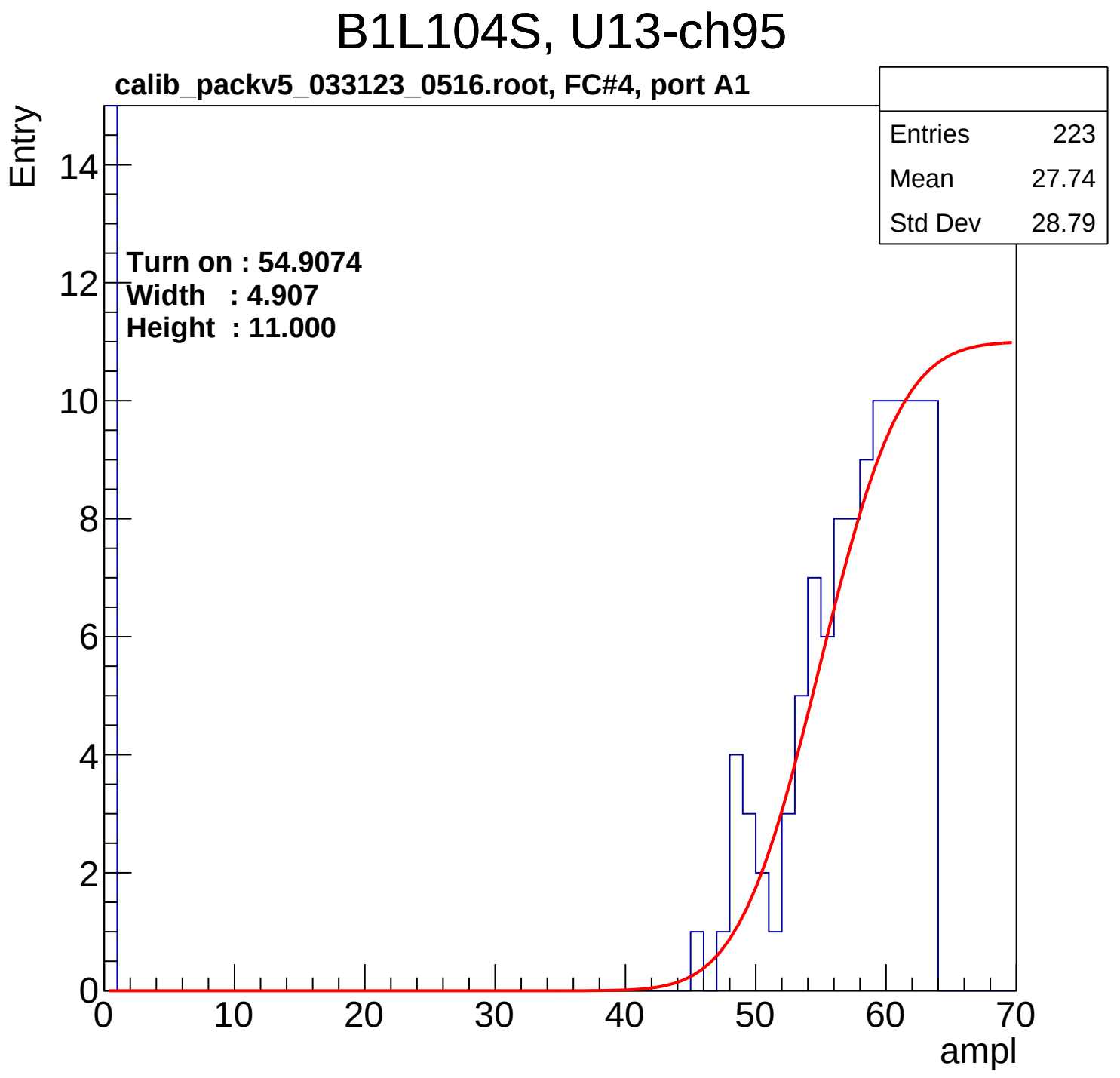
B1L104S, U13-ch95
calib_packv5_033123_0516.root, FC#4, port A1
Entries 223
Mean 27.74
Std Dev 28.79
Turn on : 54.9074
Width : 4.907
Height : 11.000
Entry
ampl
0
2
4
6
8
10
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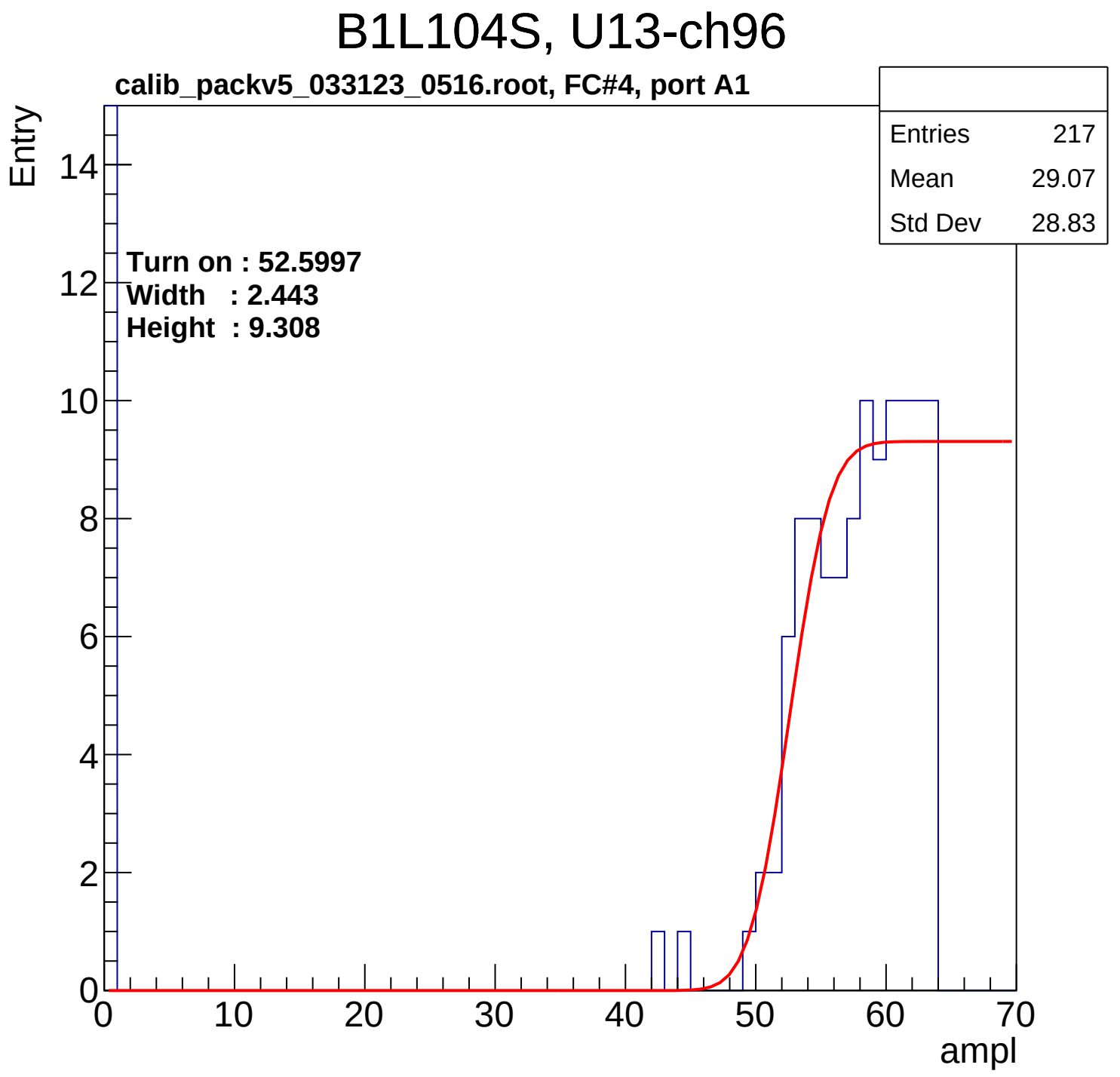
B1L104S, U13-ch96
calib_packv5_033123_0516.root, FC#4, port A1
Entries 217
Mean 29.07
Std Dev 28.83
Turn on : 52.5997
Width : 2.443
Height : 9.308
Entry
ampl
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2
4
6
8
10
12
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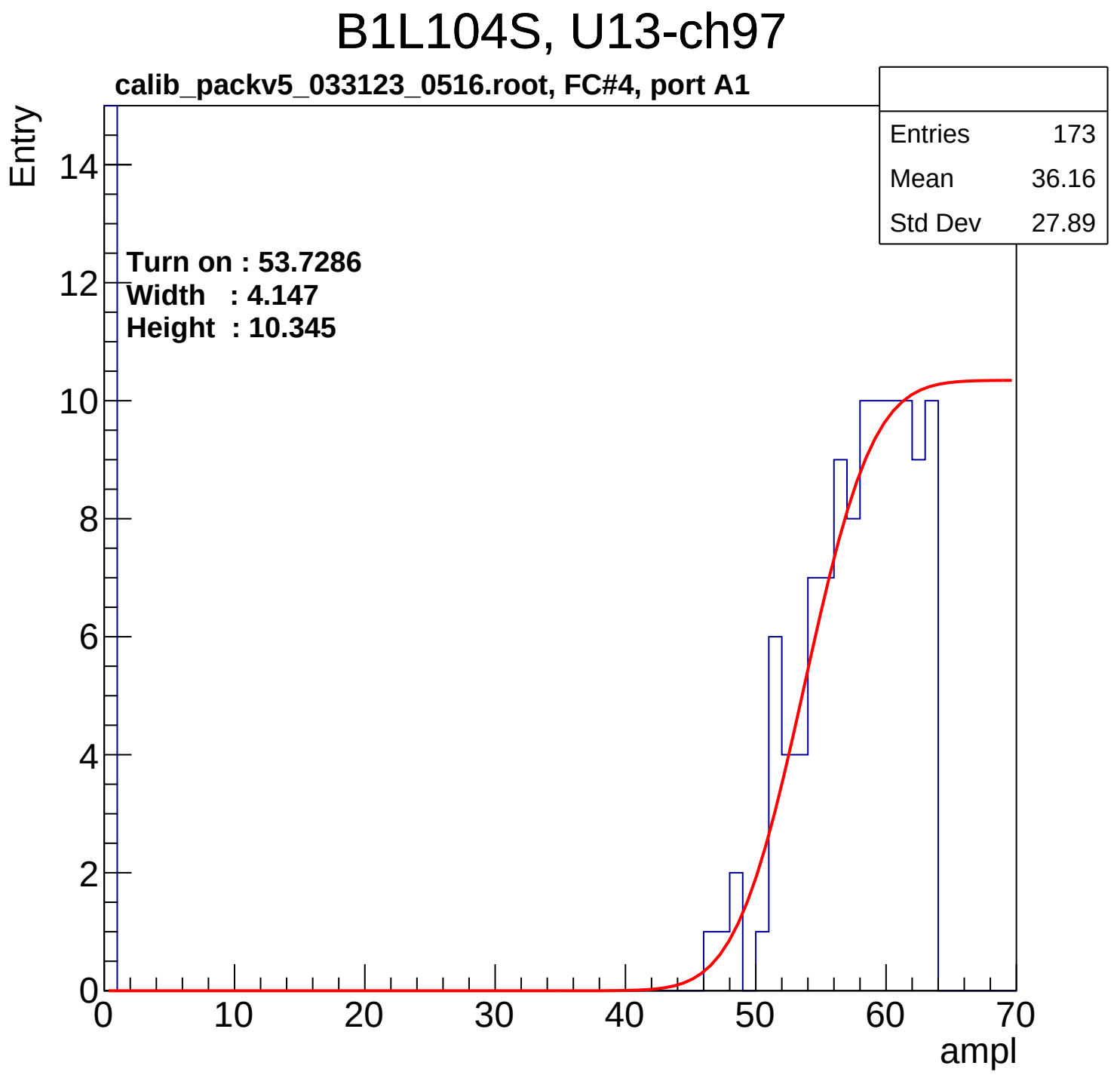
B1L104S, U13-ch97
calib_packv5_033123_0516.root, FC#4, port A1
Entries 173
Mean 36.16
Std Dev 27.89
Turn on : 53.7286
Width : 4.147
Height : 10.345
Entry
ampl
0
2
4
6
8
10
12
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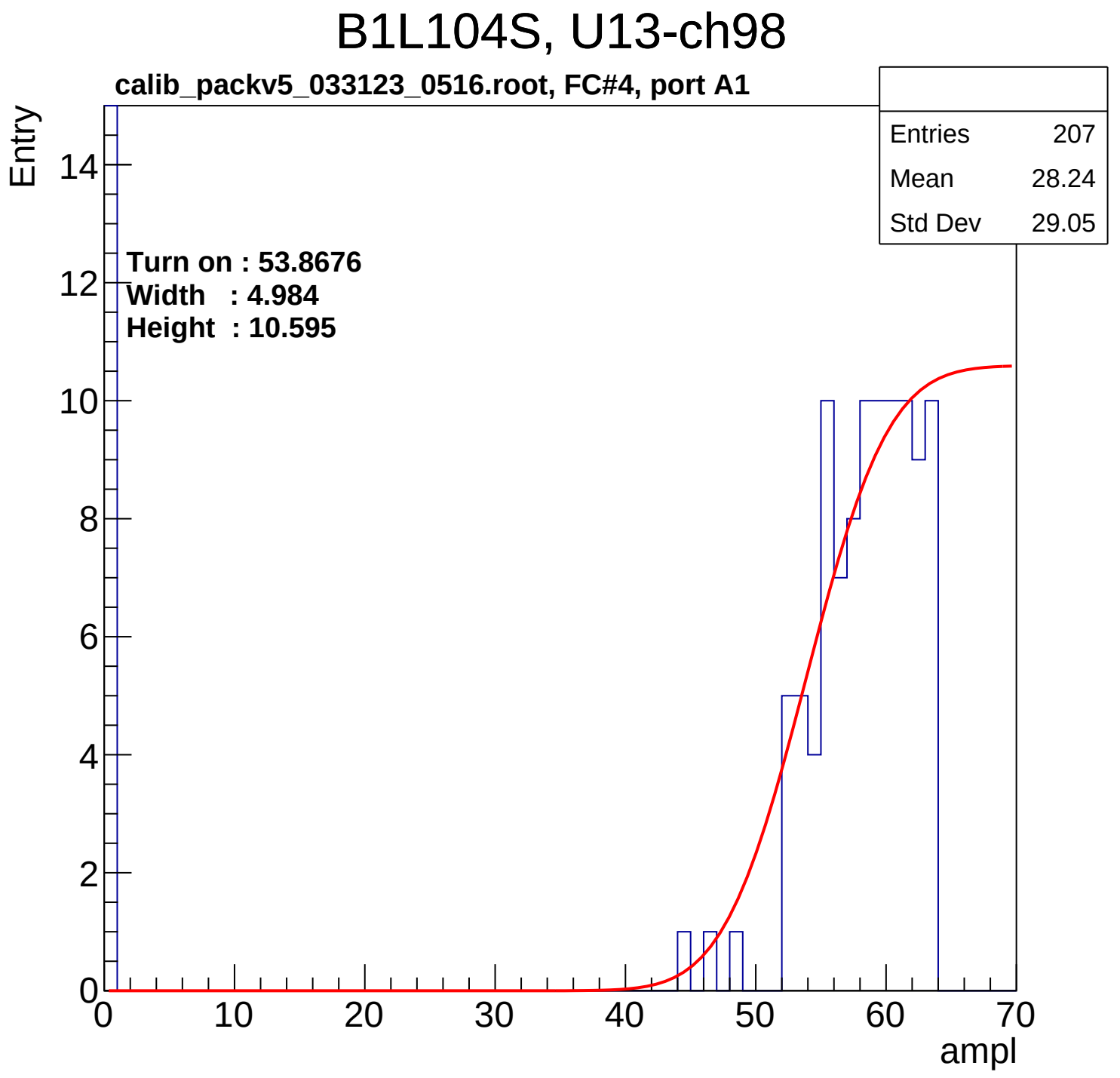
B1L104S, U13-ch98
calib_packv5_033123_0516.root, FC#4, port A1
Entries 207
Mean 28.24
Std Dev 29.05
Turn on : 53.8676
Width : 4.984
Height : 10.595
Entry
ampl
0
2
4
6
8
10
12
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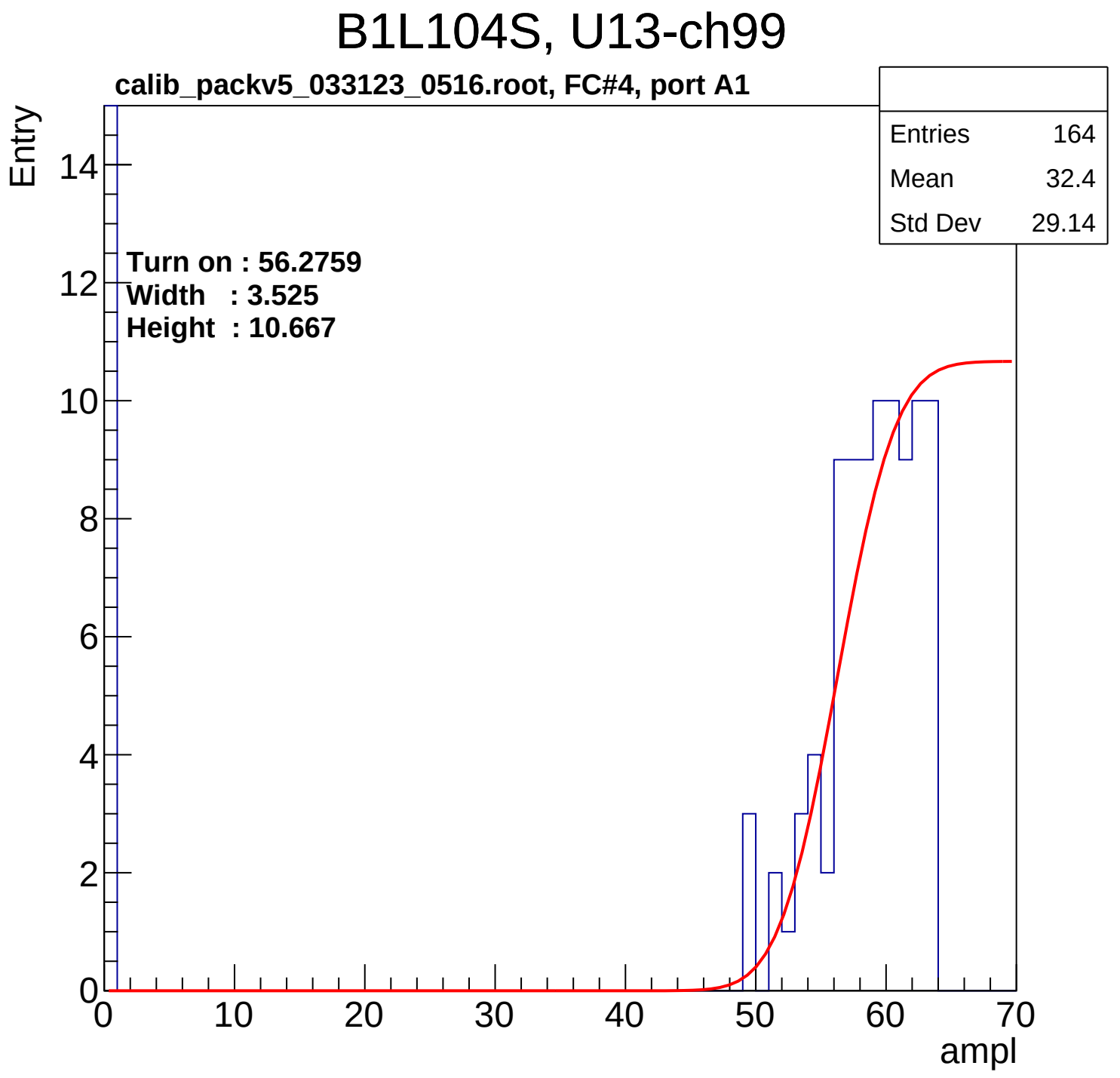
B1L104S, U13-ch99
calib_packv5_033123_0516.root, FC#4, port A1
Entries 164
Mean 32.4
Std Dev 29.14
Turn on : 56.2759
Width : 3.525
Height : 10.667
Entry
ampl
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2
4
6
8
10
12
14
0
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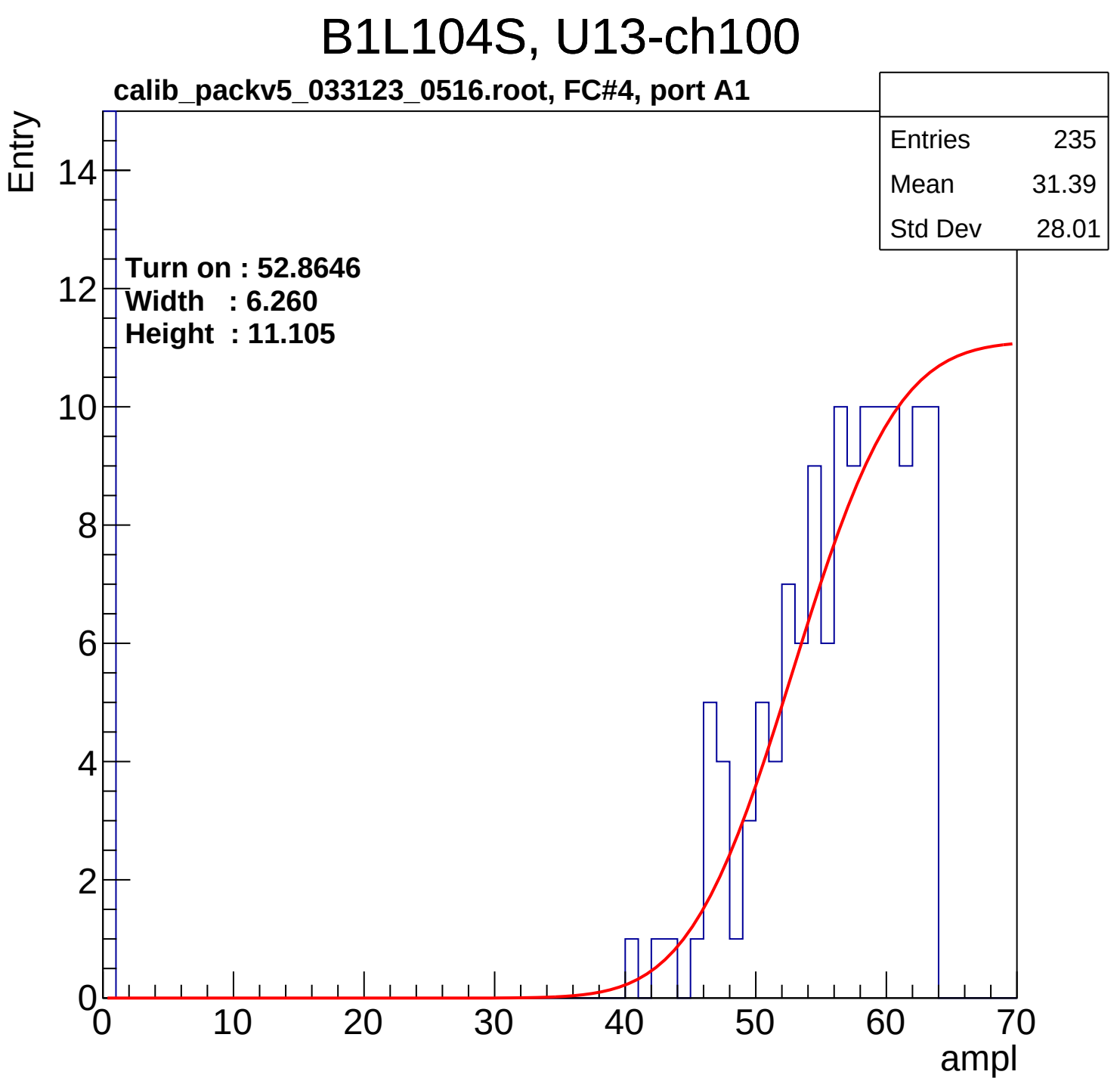
B1L104S, U13-ch100
calib_packv5_033123_0516.root, FC#4, port A1
Entries 235
Mean 31.39
Std Dev 28.01
Turn on : 52.8646
Width : 6.260
Height : 11.105
Entry
ampl
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6
8
10
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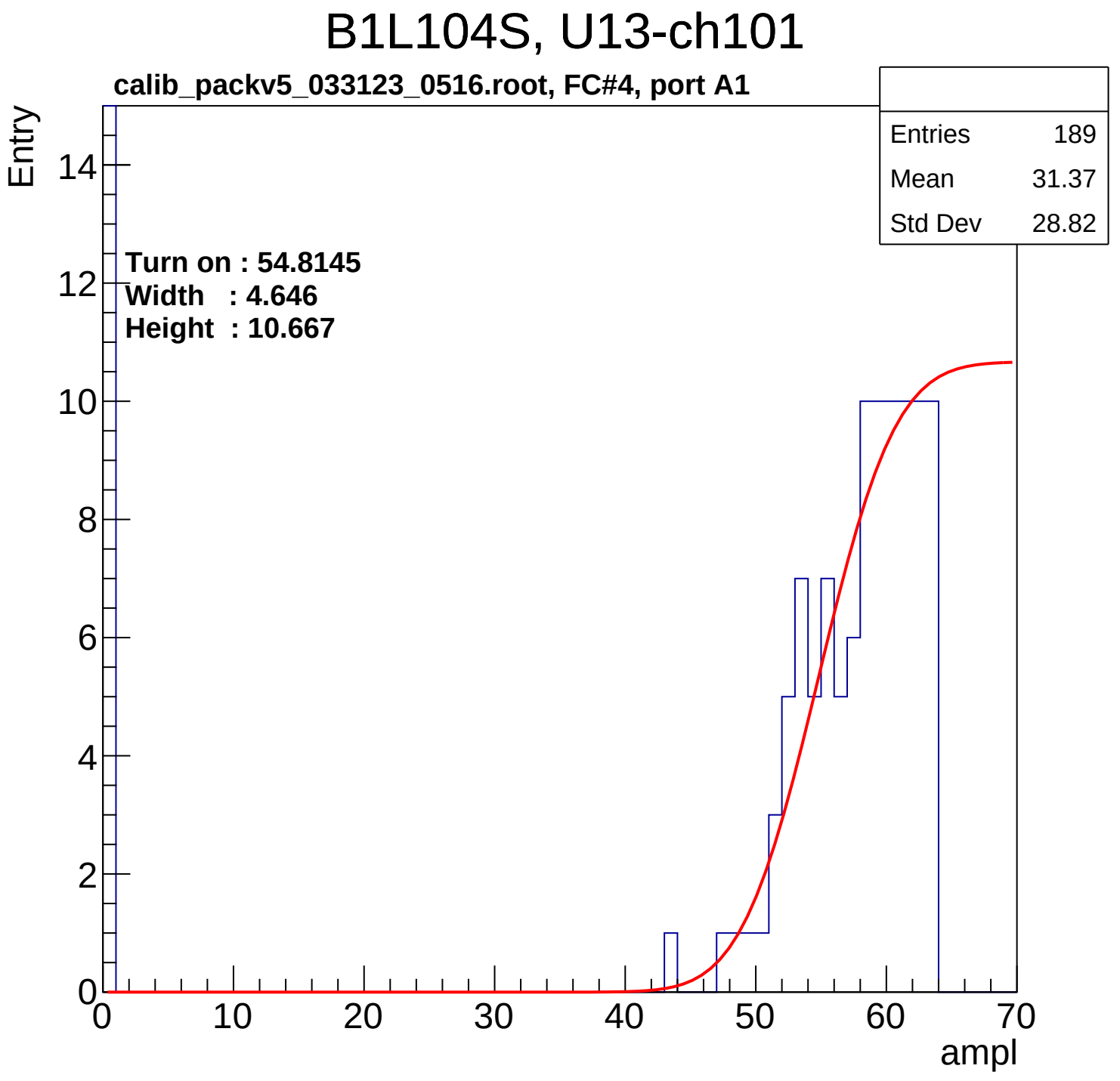
B1L104S, U13-ch101
calib_packv5_033123_0516.root, FC#4, port A1
Entries 189
Mean 31.37
Std Dev 28.82
Turn on : 54.8145
Width : 4.646
Height : 10.667
Entry
ampl
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6
8
10
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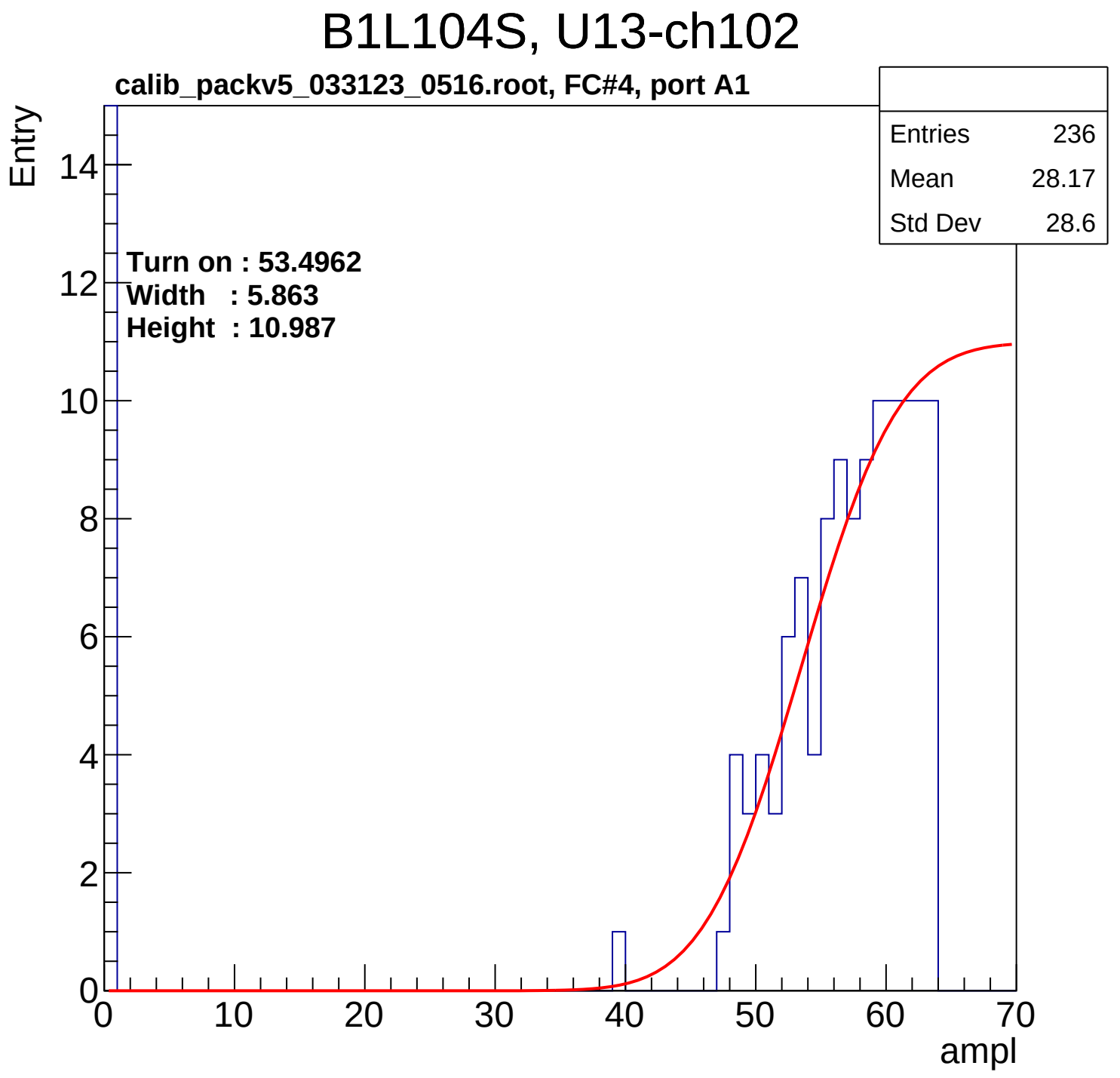
B1L104S, U13-ch102
calib_packv5_033123_0516.root, FC#4, port A1
Entries 236
Mean 28.17
Std Dev 28.6
Turn on : 53.4962
Width : 5.863
Height : 10.987
Entry
ampl
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6
8
10
12
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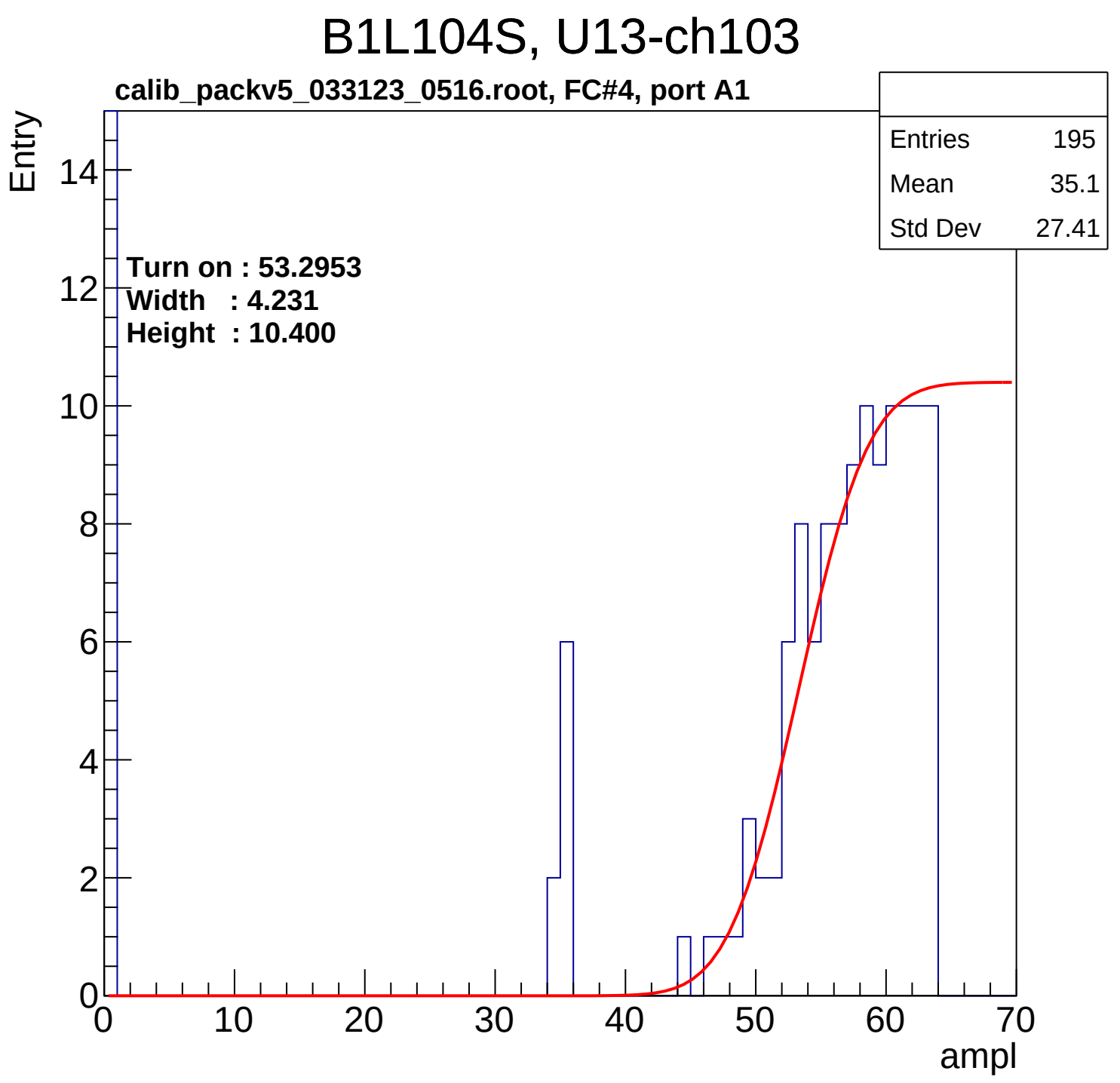
B1L104S, U13-ch103
calib_packv5_033123_0516.root, FC#4, port A1
Entries 195
Mean 35.1
Std Dev 27.41
Turn on : 53.2953
Width : 4.231
Height : 10.400
Entry
ampl
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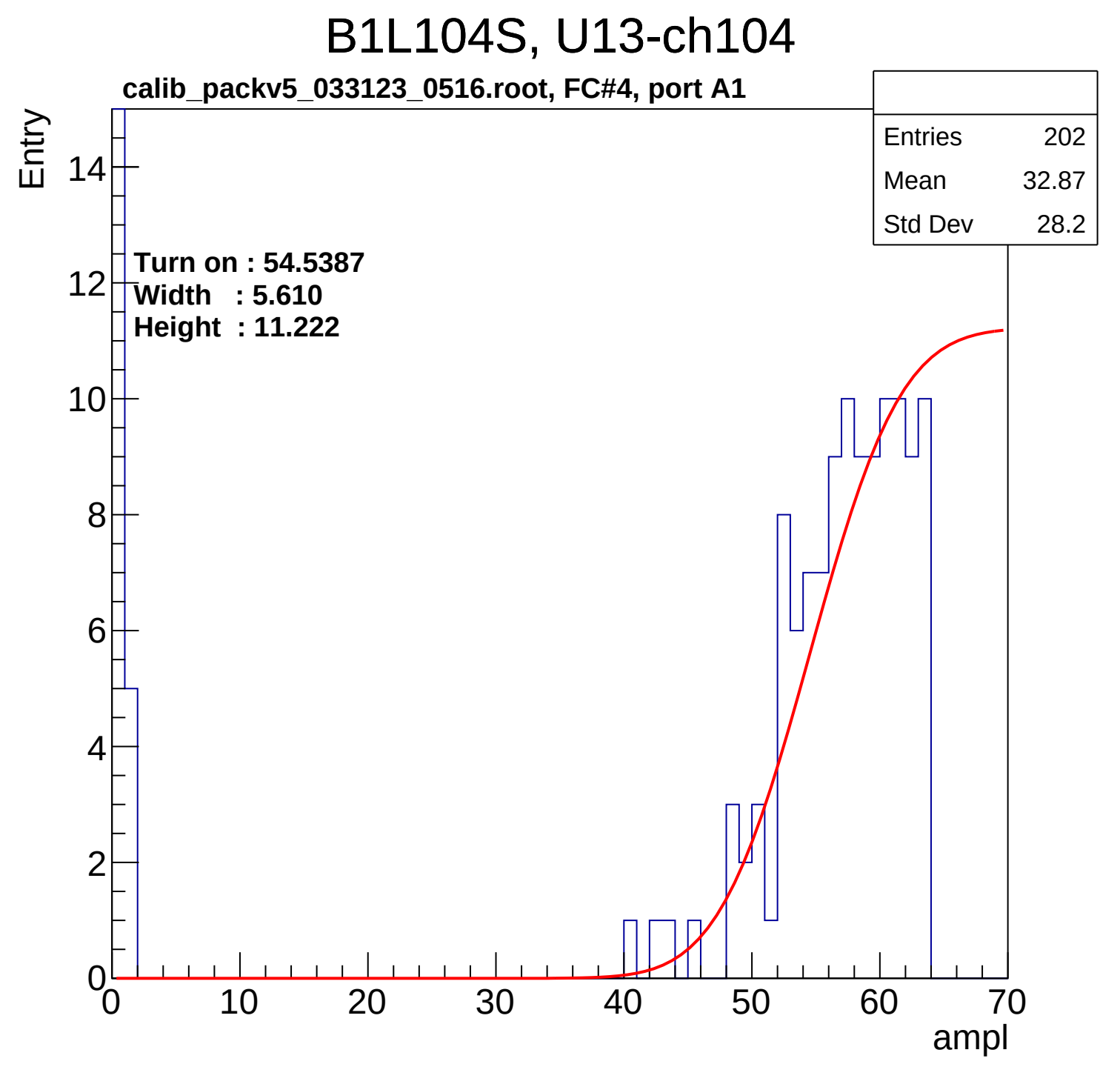
B1L104S, U13-ch104
calib_packv5_033123_0516.root, FC#4, port A1
Entries 202
Mean 32.87
Std Dev 28.2
Turn on : 54.5387
Width : 5.610
Height : 11.222
Entry
ampl
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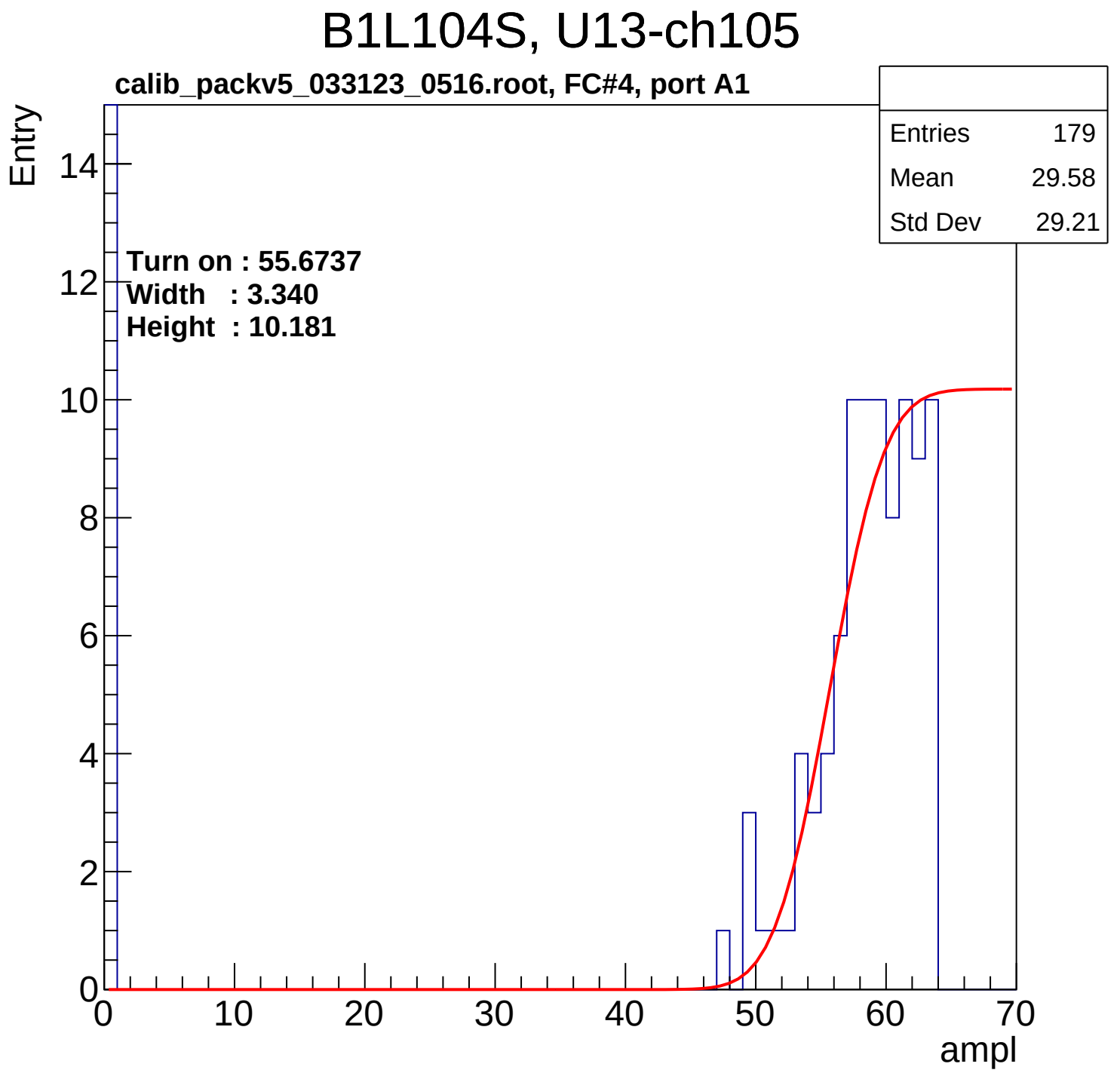
B1L104S, U13-ch105
calib_packv5_033123_0516.root, FC#4, port A1
Entries 179
Mean 29.58
Std Dev 29.21
Turn on : 55.6737
Width : 3.340
Height : 10.181
Entry
ampl
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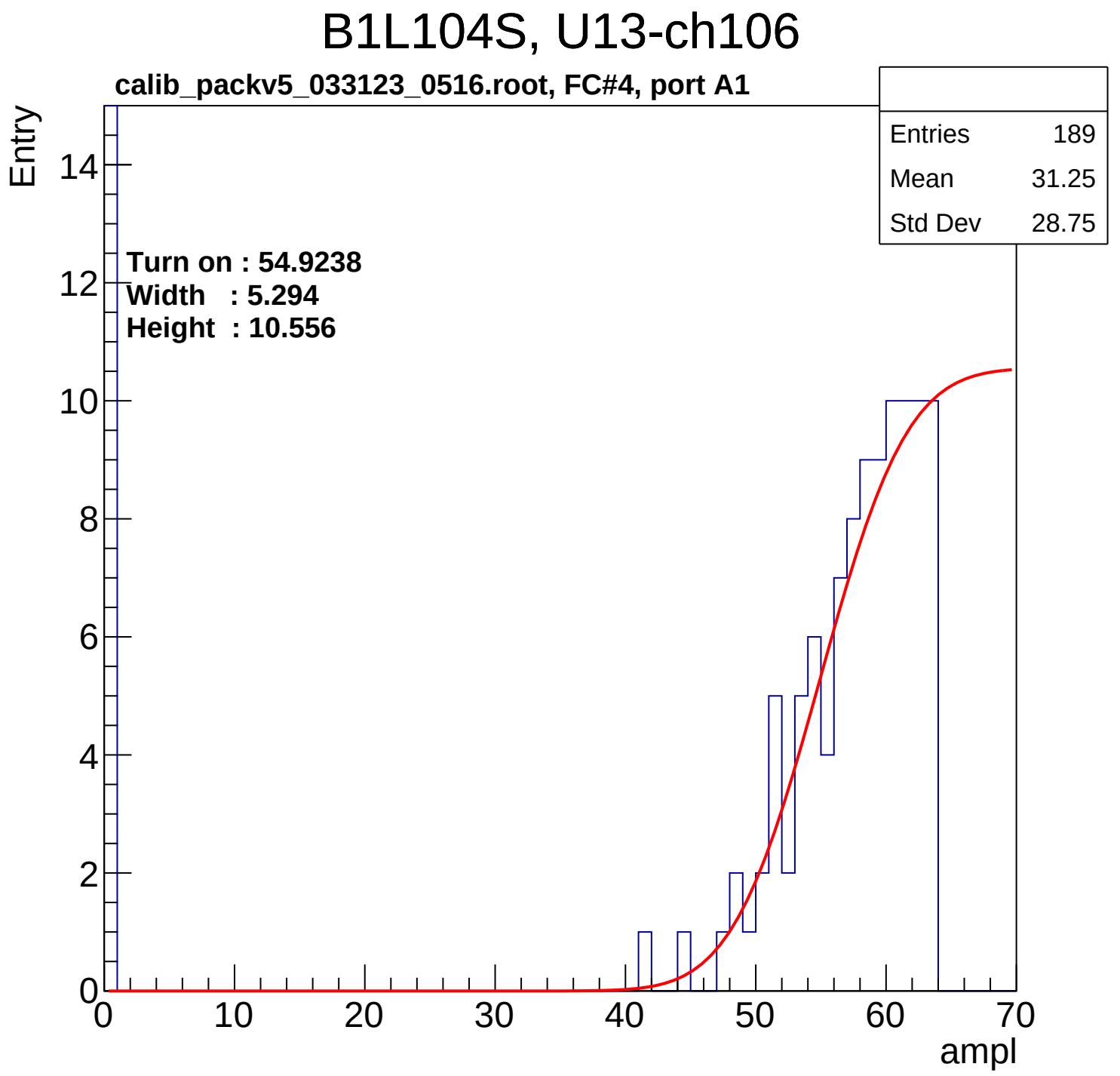
B1L104S, U13-ch106
calib_packv5_033123_0516.root, FC#4, port A1
Entries 189
Mean 31.25
Std Dev 28.75
Turn on : 54.9238
Width : 5.294
Height : 10.556
Entry
ampl
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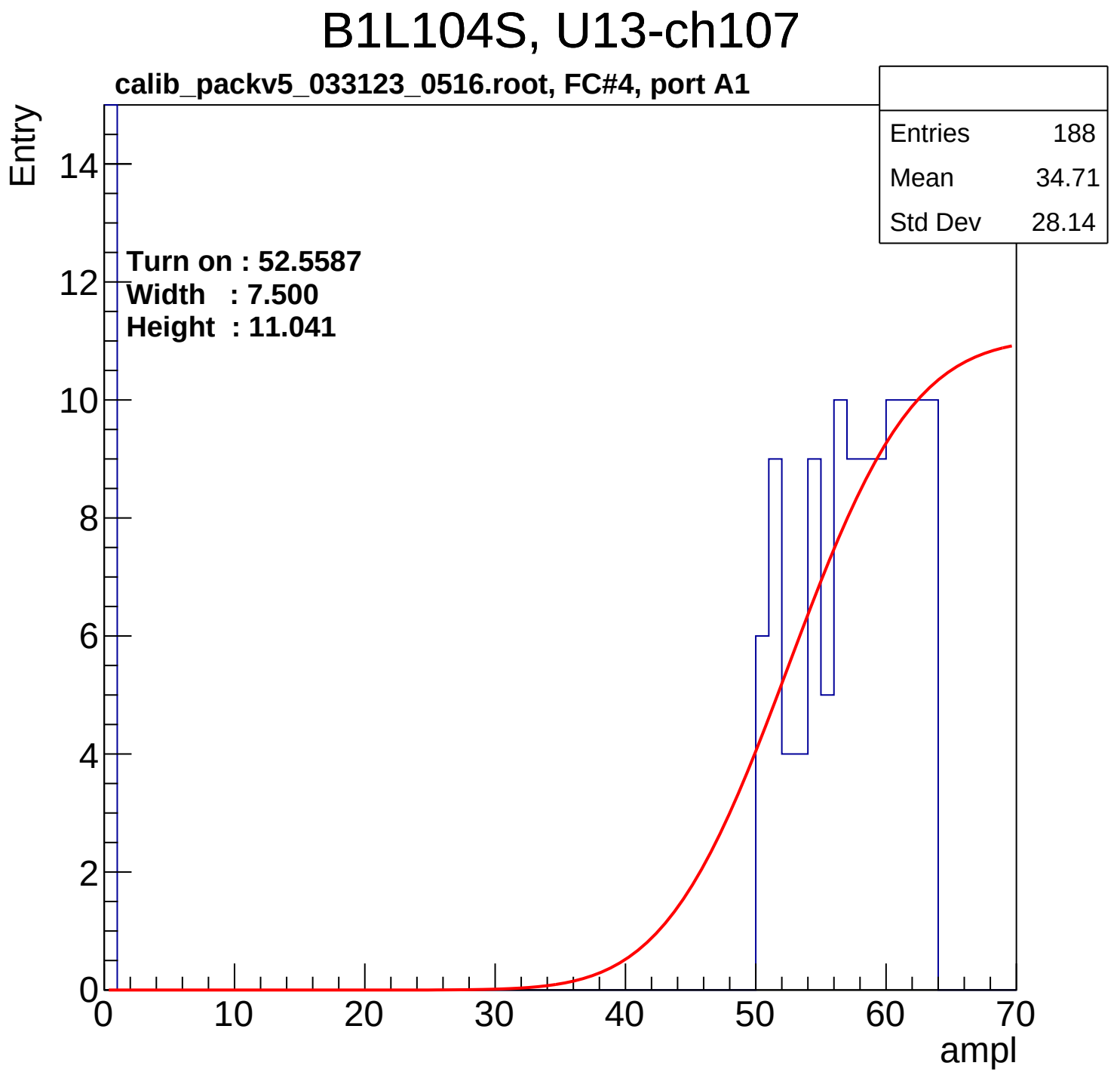
B1L104S, U13-ch107
calib_packv5_033123_0516.root, FC#4, port A1
Entries 188
Mean 34.71
Std Dev 28.14
Turn on : 52.5587
Width : 7.500
Height : 11.041
Entry
ampl
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6
8
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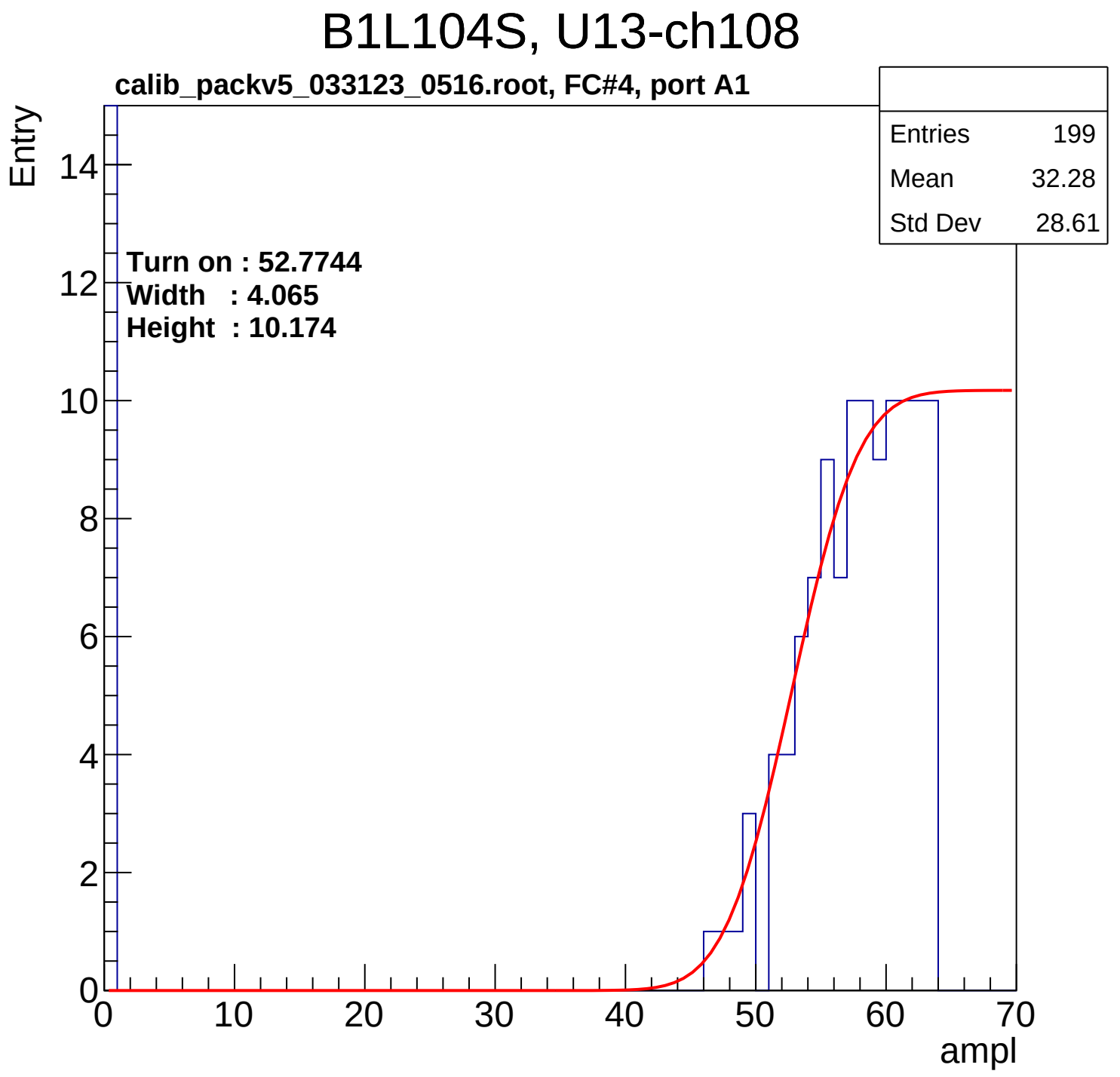
B1L104S, U13-ch108
calib_packv5_033123_0516.root, FC#4, port A1
Entries 199
Mean 32.28
Std Dev 28.61
Turn on : 52.7744
Width : 4.065
Height : 10.174
Entry
ampl
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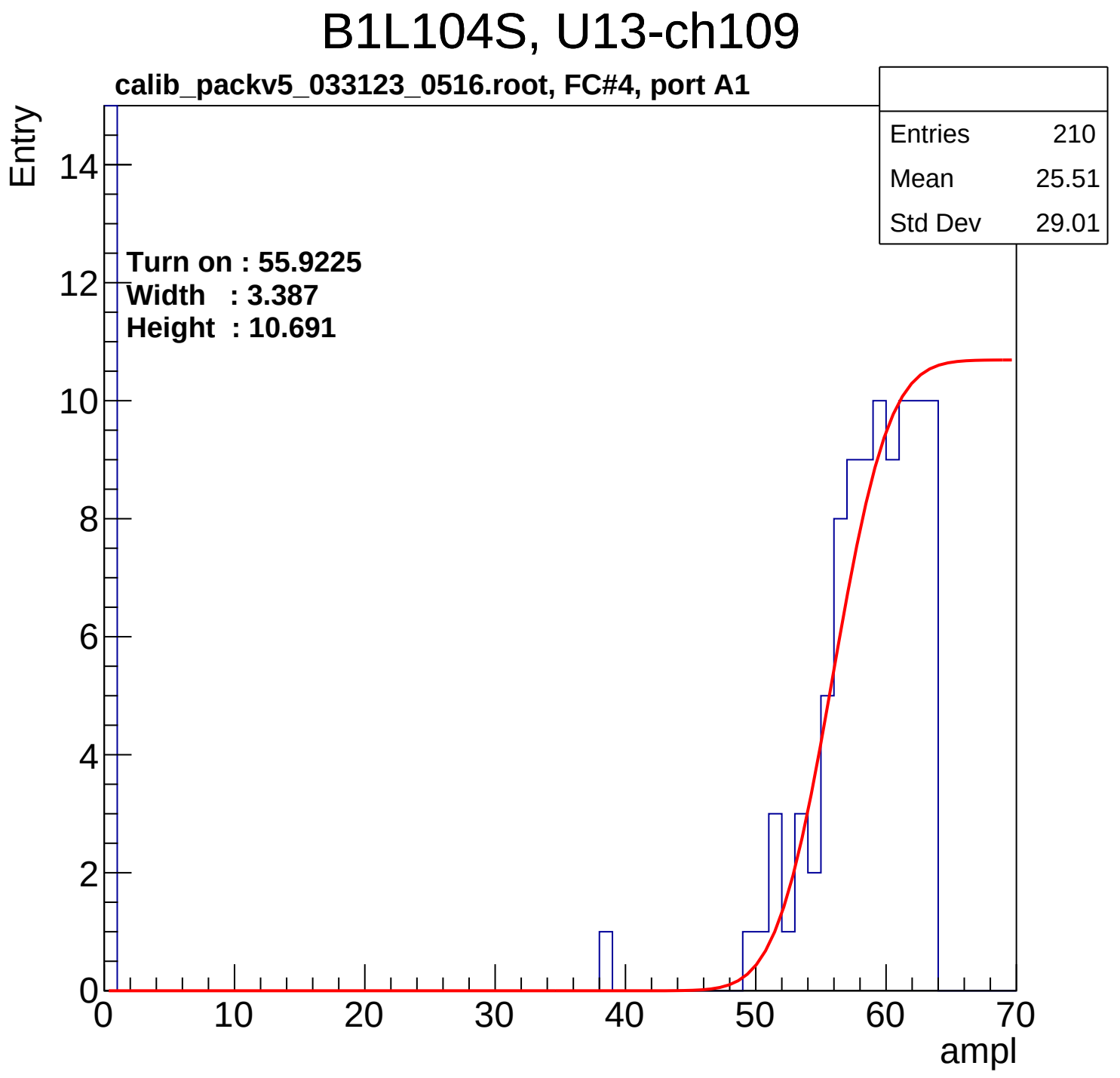
B1L104S, U13-ch109
calib_packv5_033123_0516.root, FC#4, port A1
Entries 210
Mean 25.51
Std Dev 29.01
Turn on : 55.9225
Width : 3.387
Height : 10.691
Entry
ampl
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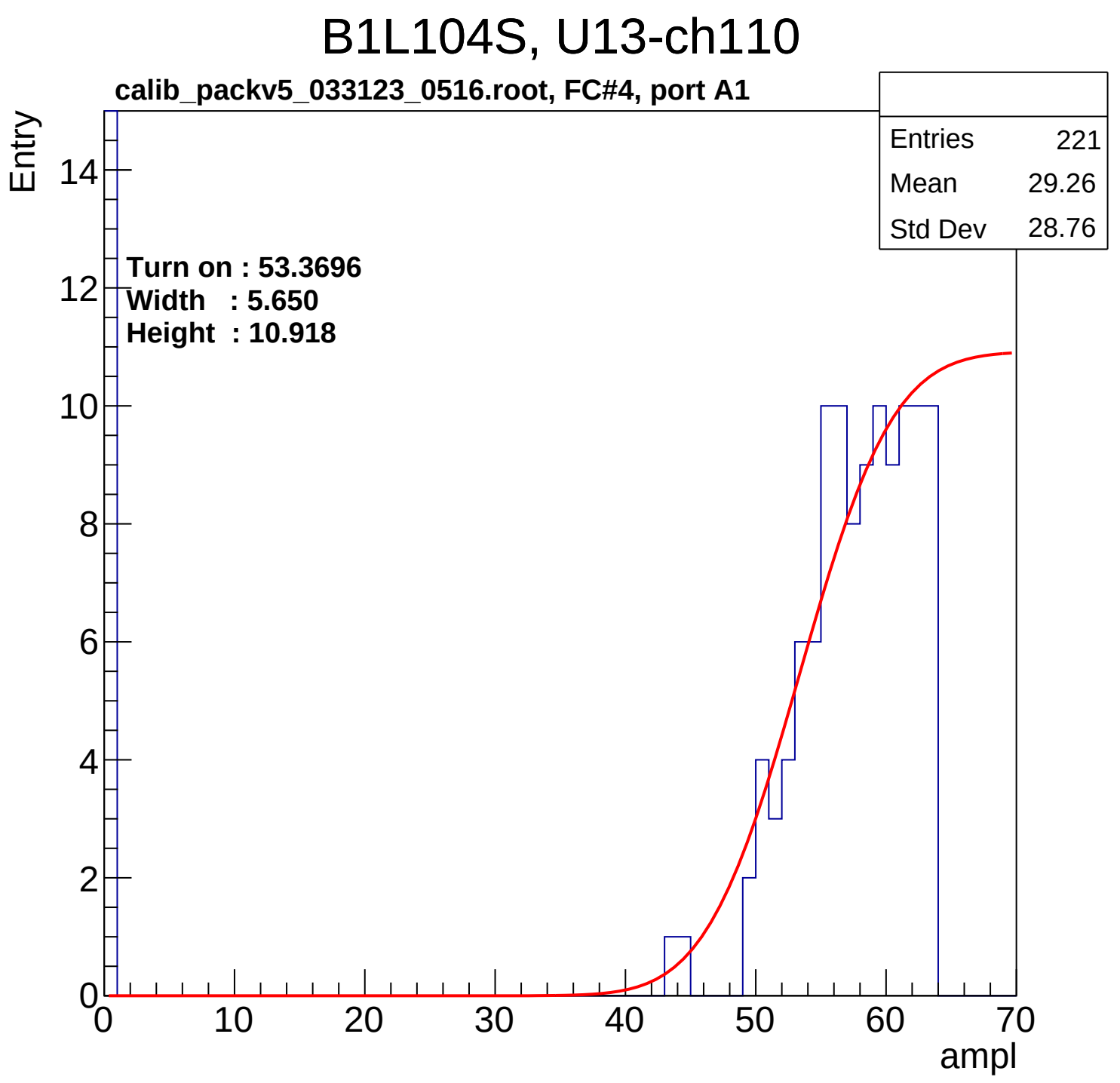
B1L104S, U13-ch110
calib_packv5_033123_0516.root, FC#4, port A1
Entries 221
Mean 29.26
Std Dev 28.76
Turn on : 53.3696
Width : 5.650
Height : 10.918
Entry
ampl
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6
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10
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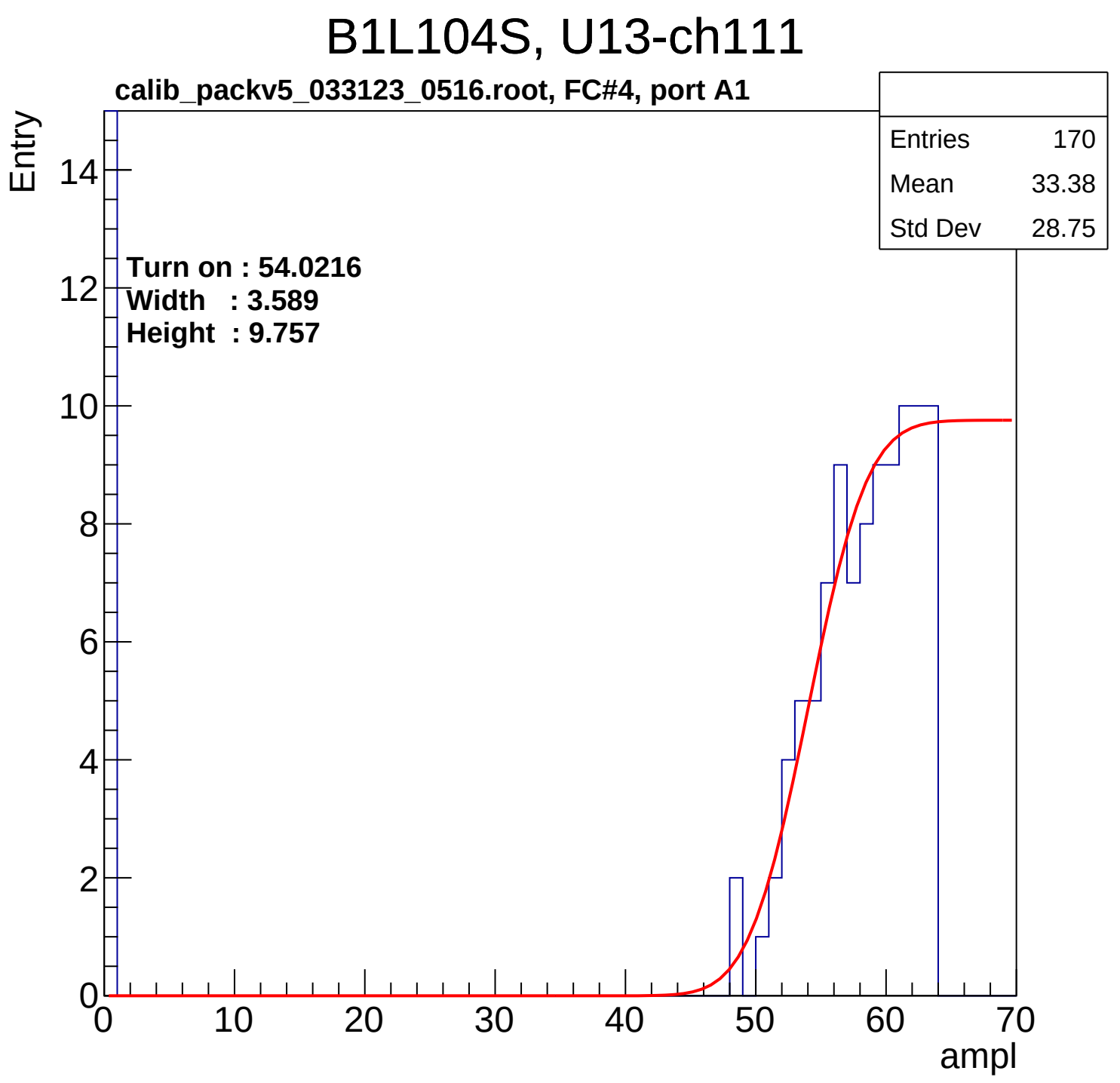
B1L104S, U13-ch111
calib_packv5_033123_0516.root, FC#4, port A1
Entries 170
Mean 33.38
Std Dev 28.75
Turn on : 54.0216
Width : 3.589
Height : 9.757
Entry
ampl
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6
8
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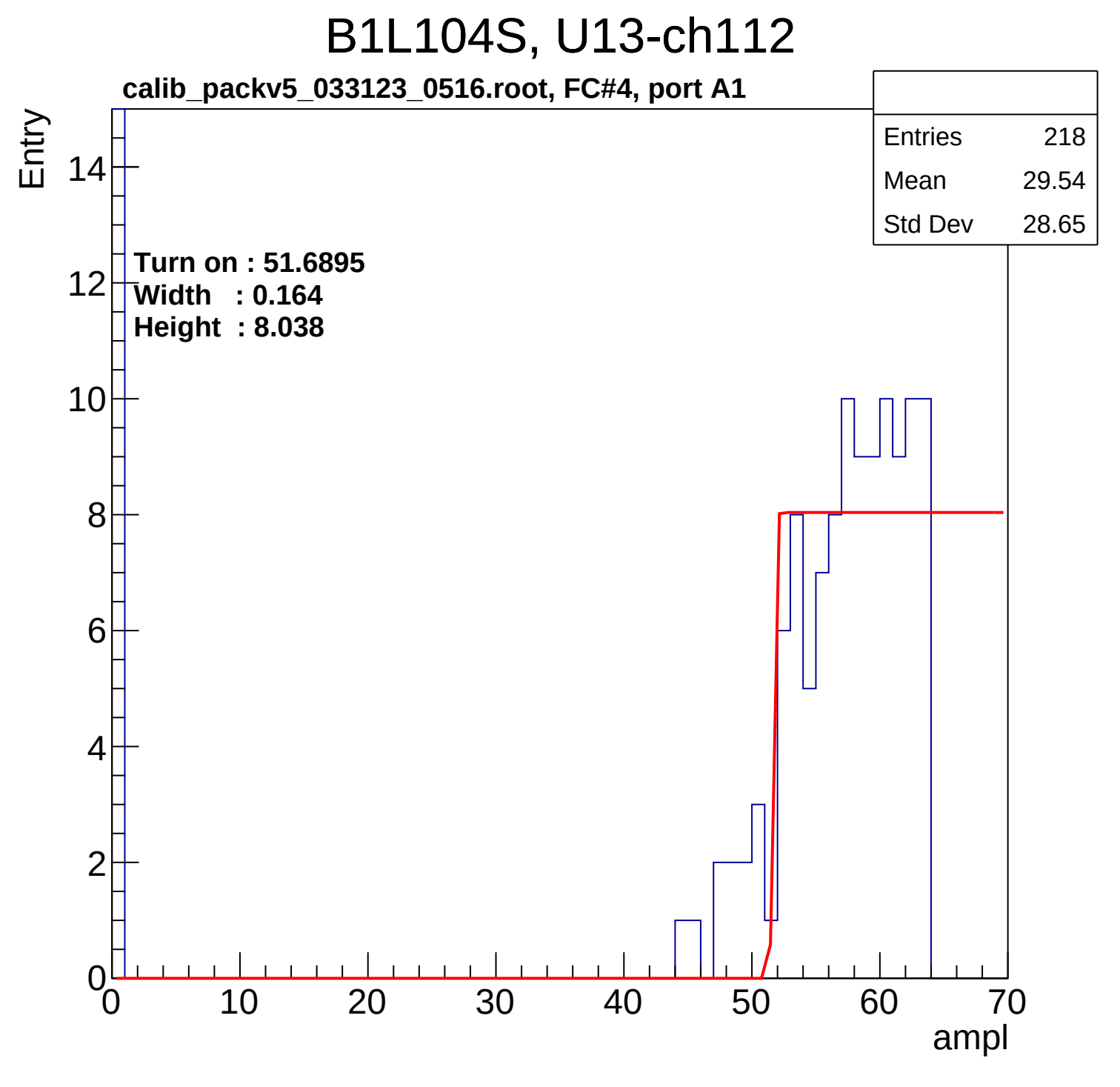
B1L104S, U13-ch112
calib_packv5_033123_0516.root, FC#4, port A1
Entries 218
Mean 29.54
Std Dev 28.65
Turn on : 51.6895
Width : 0.164
Height : 8.038
Entry
ampl
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6
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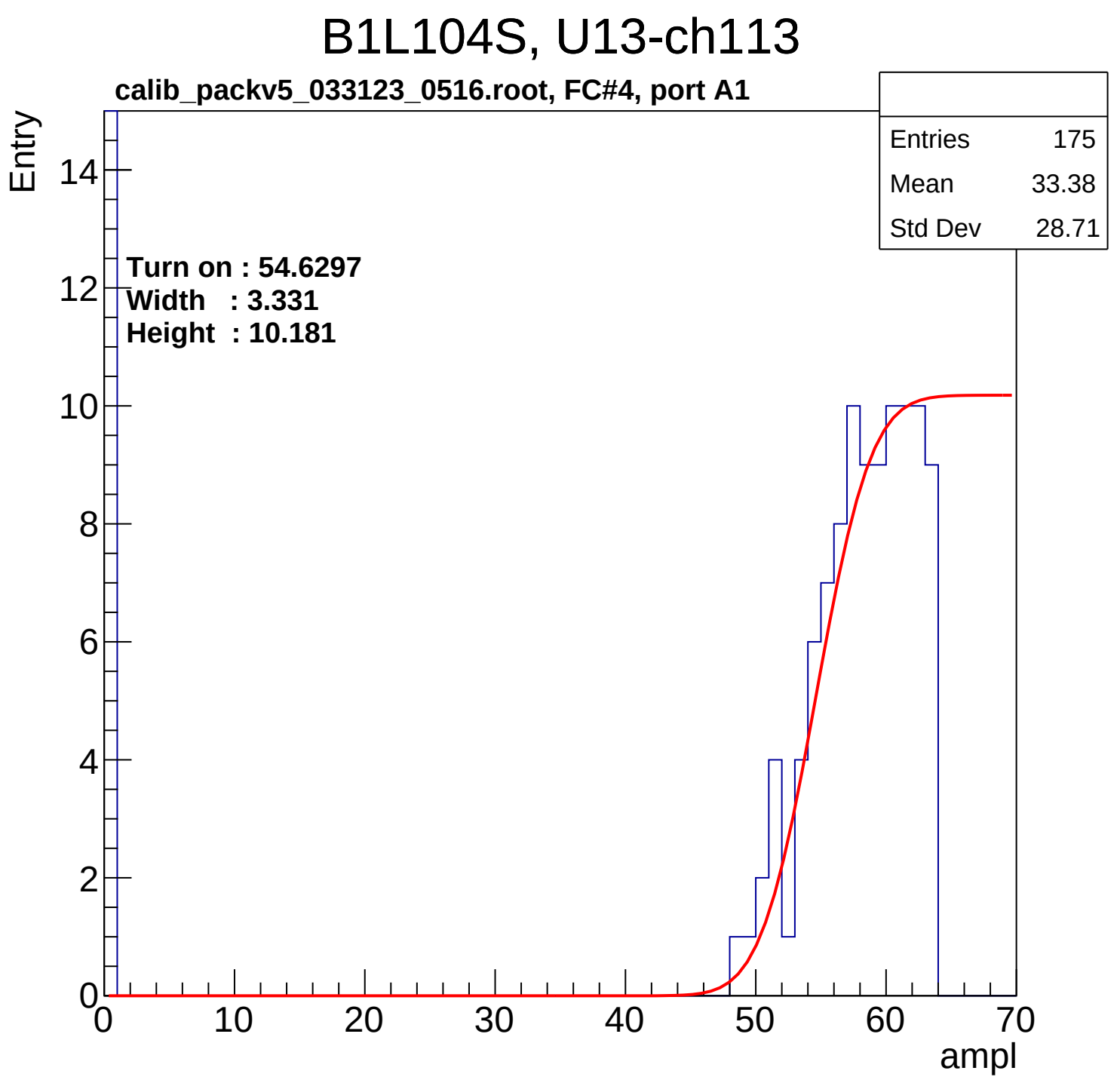
B1L104S, U13-ch113
calib_packv5_033123_0516.root, FC#4, port A1
Entries 175
Mean 33.38
Std Dev 28.71
Turn on : 54.6297
Width : 3.331
Height : 10.181
Entry
ampl
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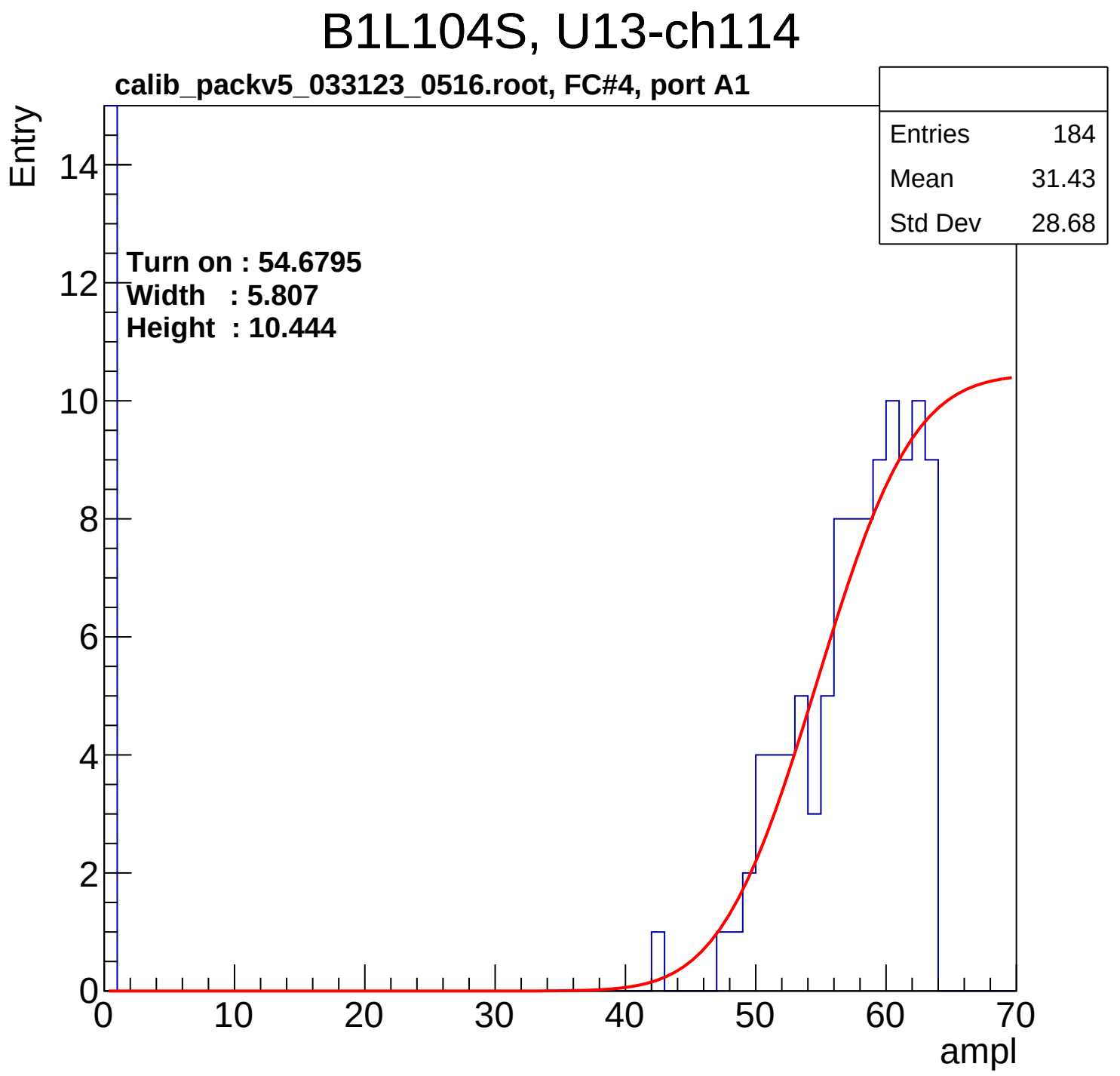
B1L104S, U13-ch114
calib_packv5_033123_0516.root, FC#4, port A1
Entries 184
Mean 31.43
Std Dev 28.68
Turn on : 54.6795
Width : 5.807
Height : 10.444
Entry
ampl
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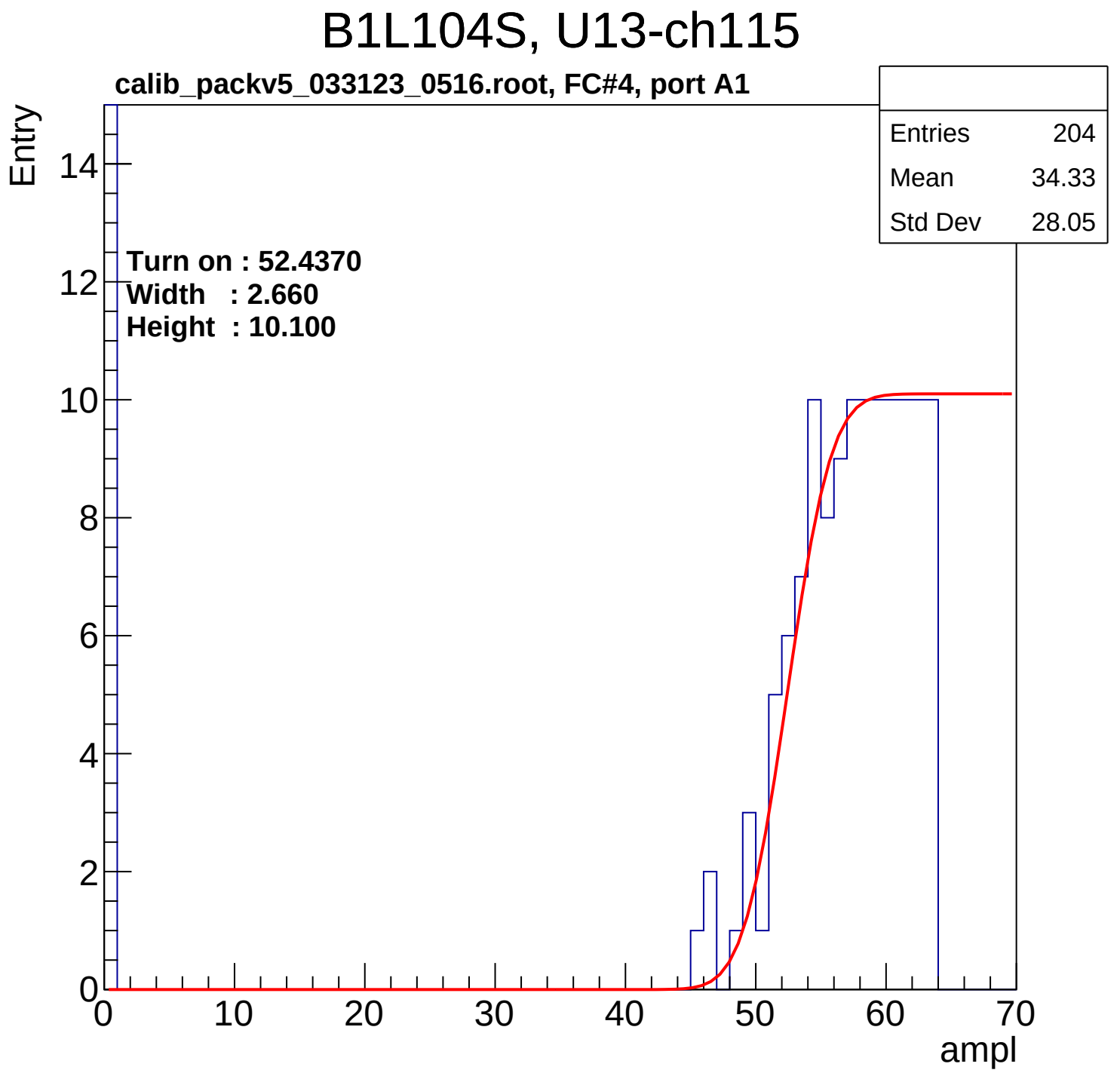
B1L104S, U13-ch115
calib_packv5_033123_0516.root, FC#4, port A1
Entries 204
Mean 34.33
Std Dev 28.05
Turn on : 52.4370
Width : 2.660
Height : 10.100
Entry
ampl
0
2
4
6
8
10
12
14
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10
20
30
40
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60
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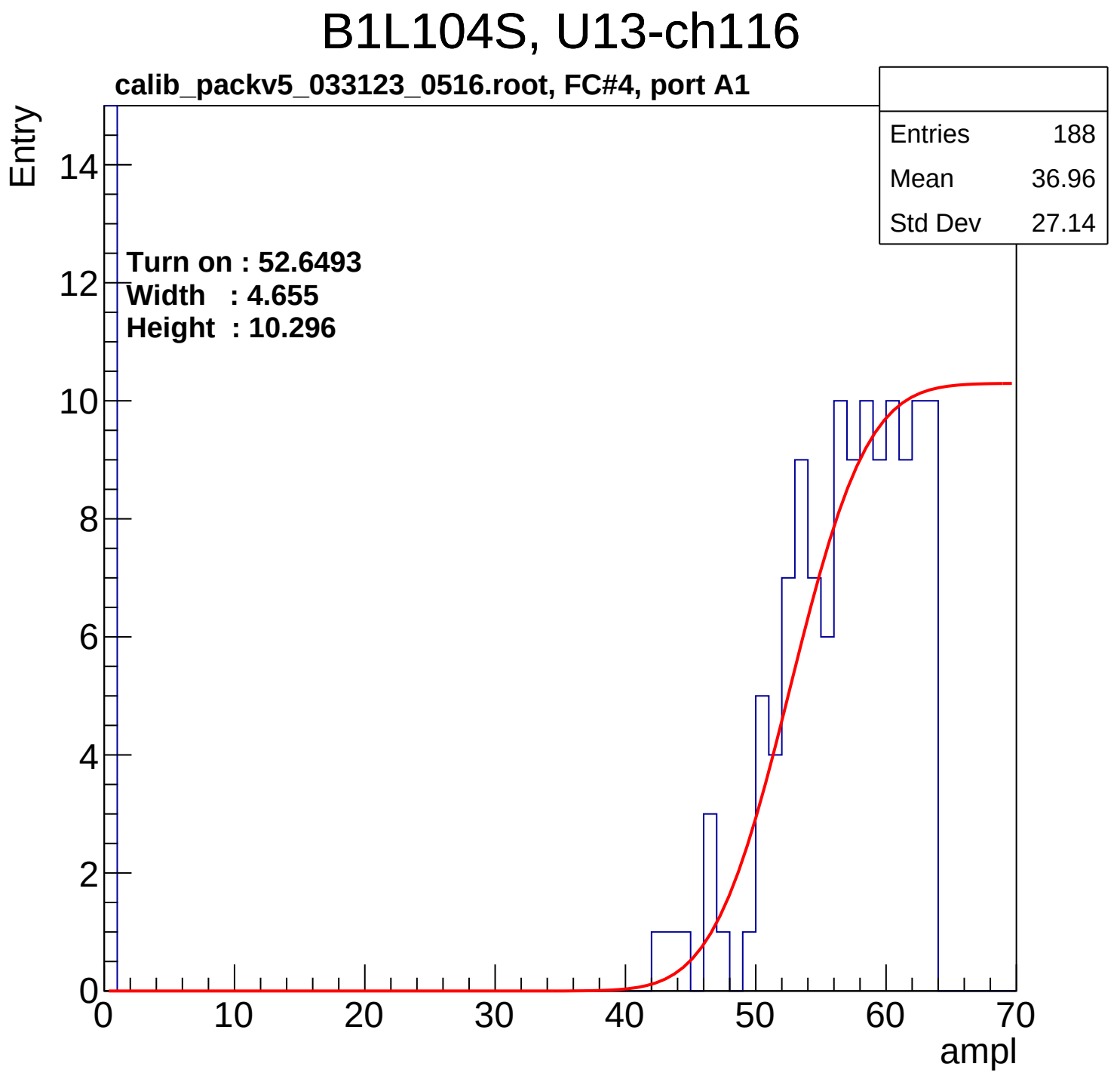
B1L104S, U13-ch116
calib_packv5_033123_0516.root, FC#4, port A1
Entries 188
Mean 36.96
Std Dev 27.14
Turn on : 52.6493
Width : 4.655
Height : 10.296
Entry
ampl
0
2
4
6
8
10
12
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0
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20
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60
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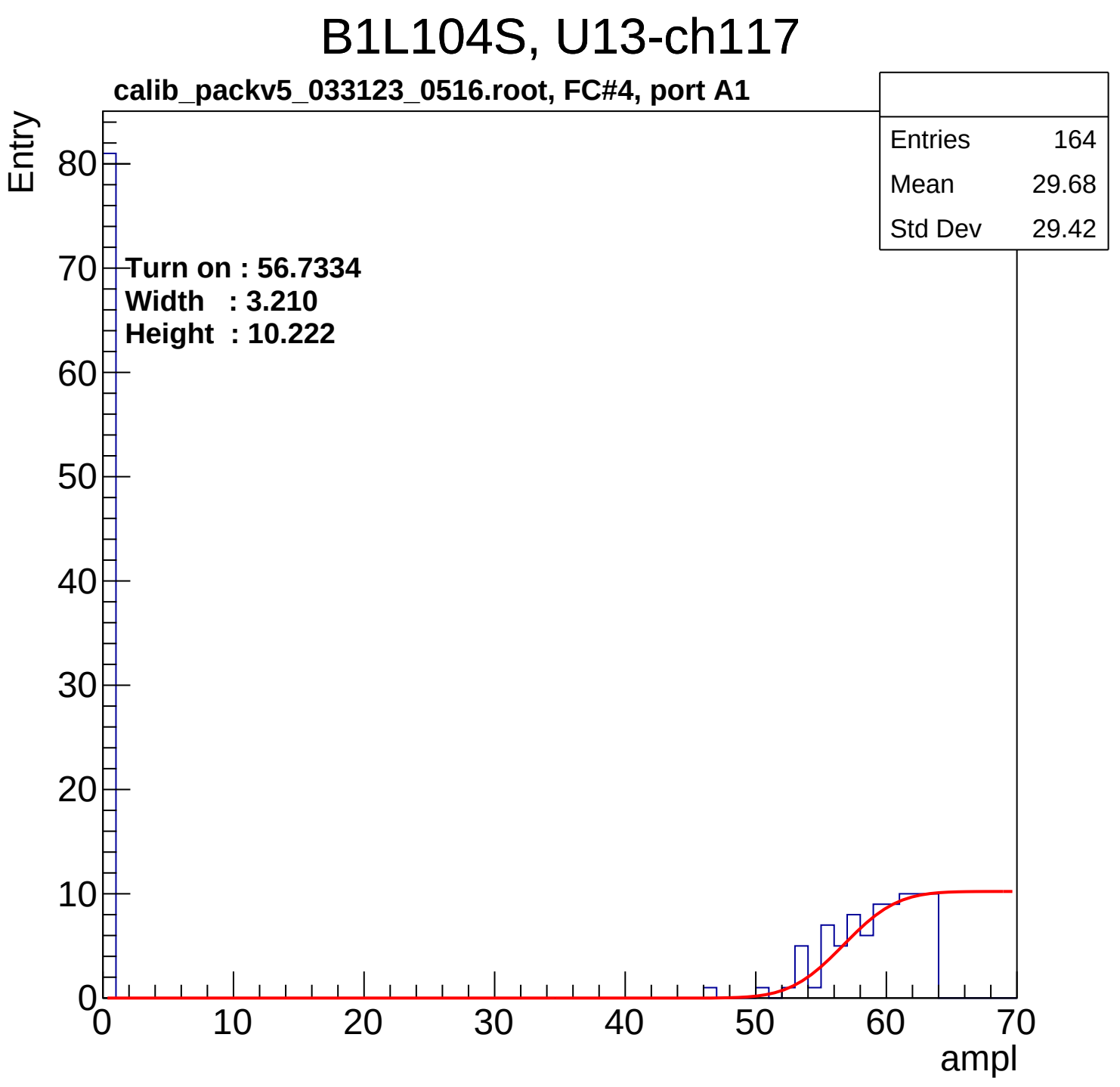
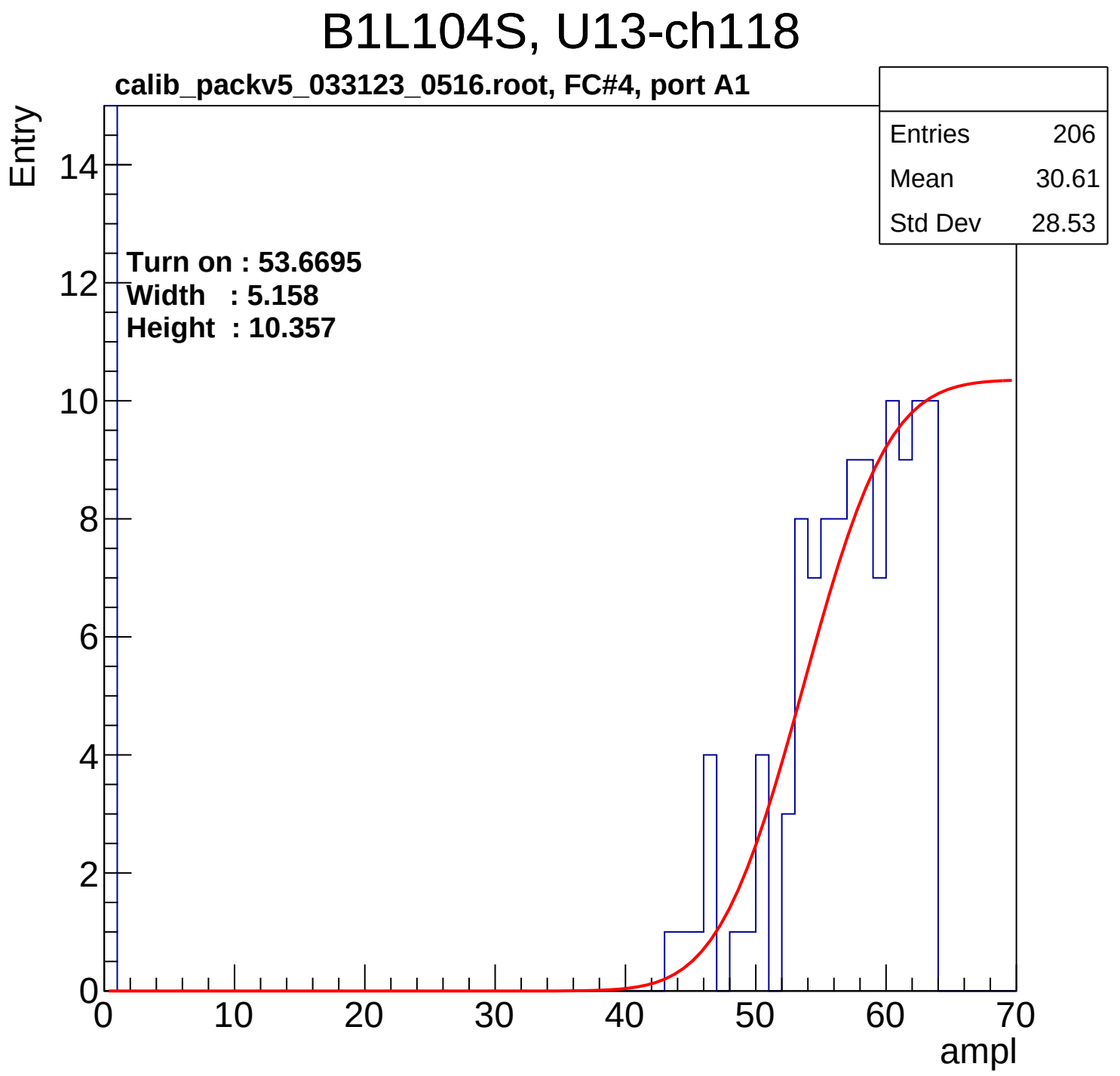

B1L104S, U13-ch117
calib_packv5_033123_0516.root, FC#4, port A1
Entries 164
Mean 29.68
Std Dev 29.42
Turn on : 56.7334
Width : 3.210
Height : 10.222
Entry
ampl
0
10
20
30
40
50
60
70
80


B1L104S, U13-ch118
calib_packv5_033123_0516.root, FC#4, port A1
Entries 206
Mean 30.61
Std Dev 28.53
Turn on : 53.6695
Width : 5.158
Height : 10.357
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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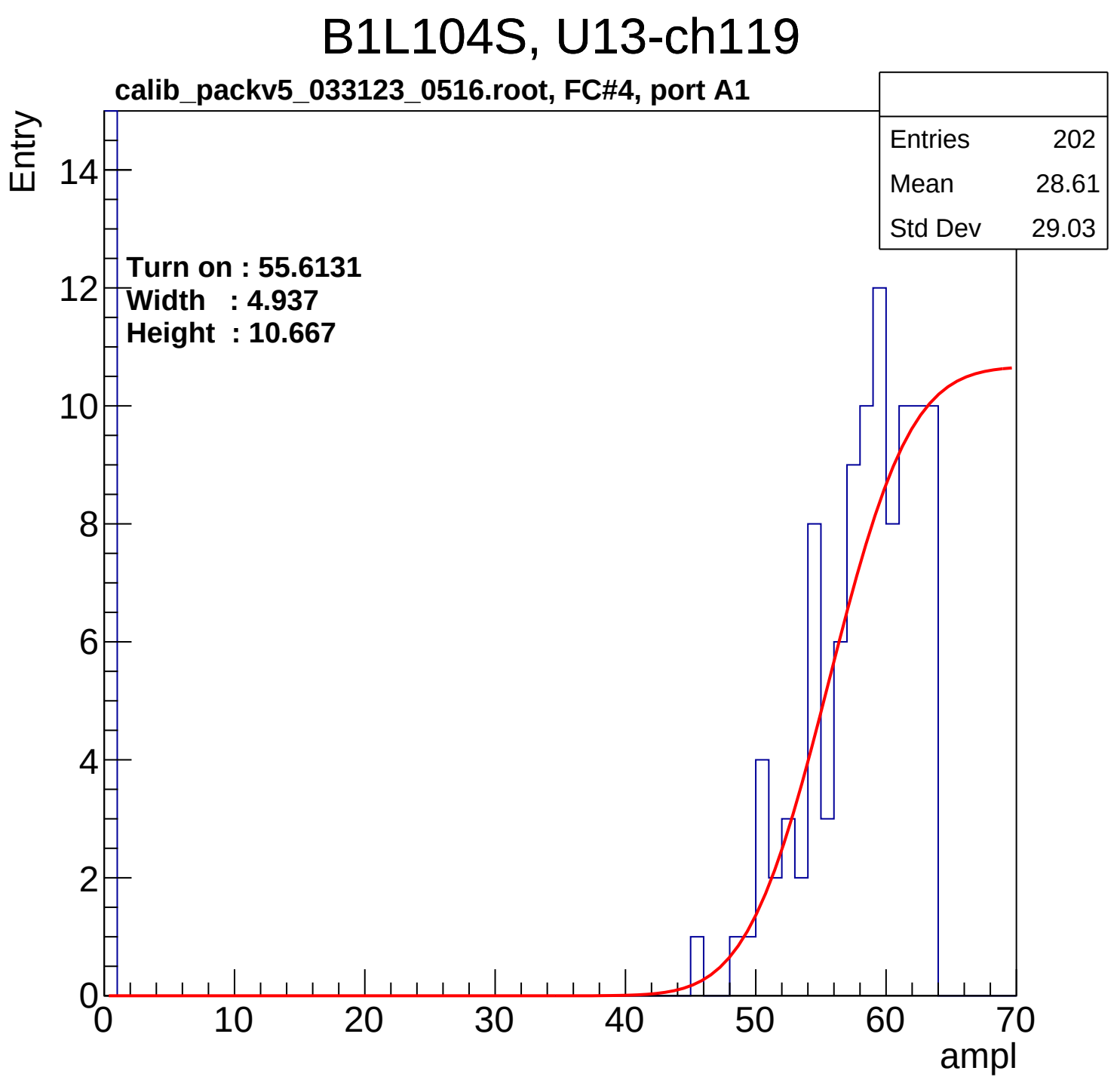
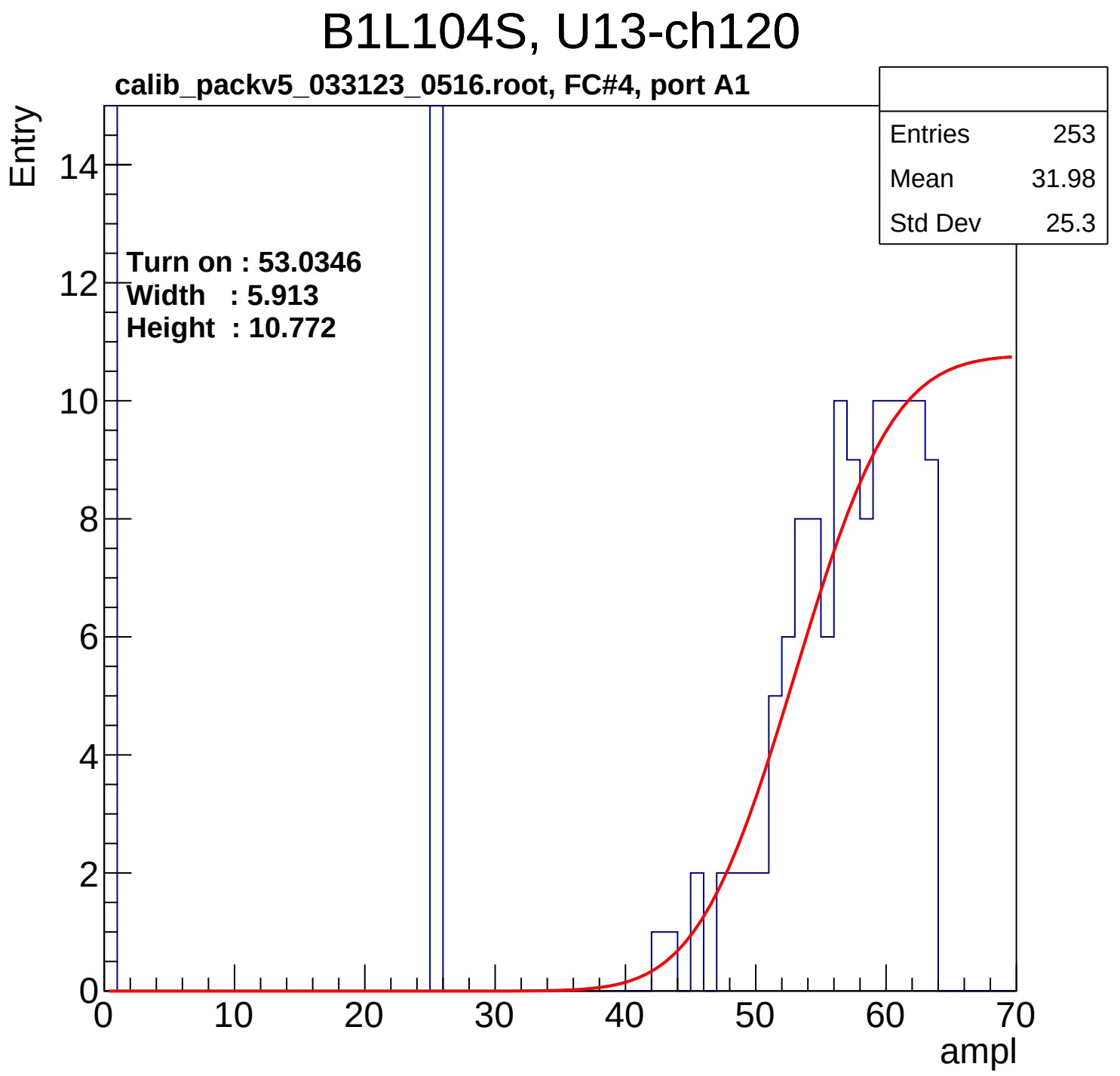
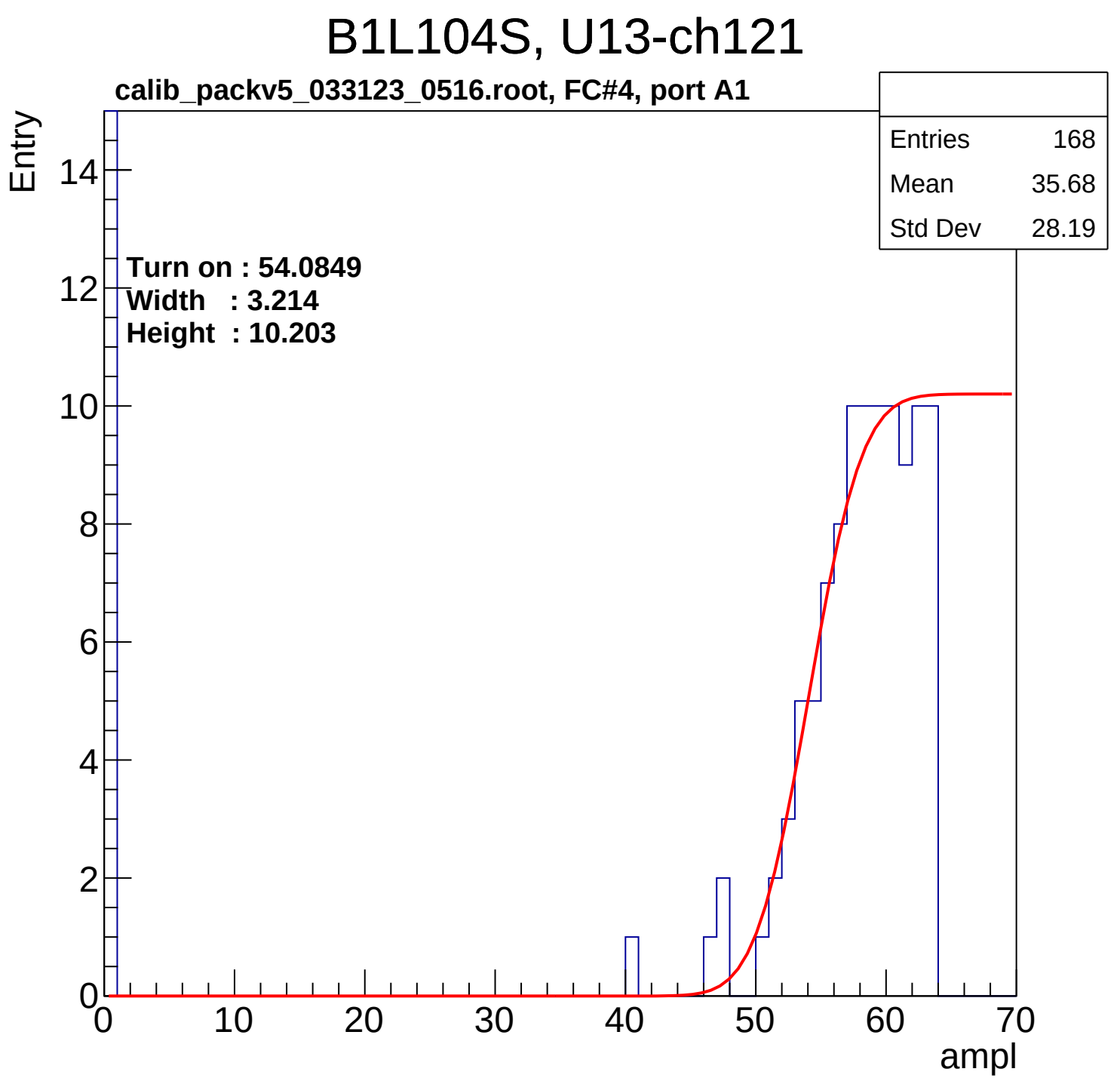
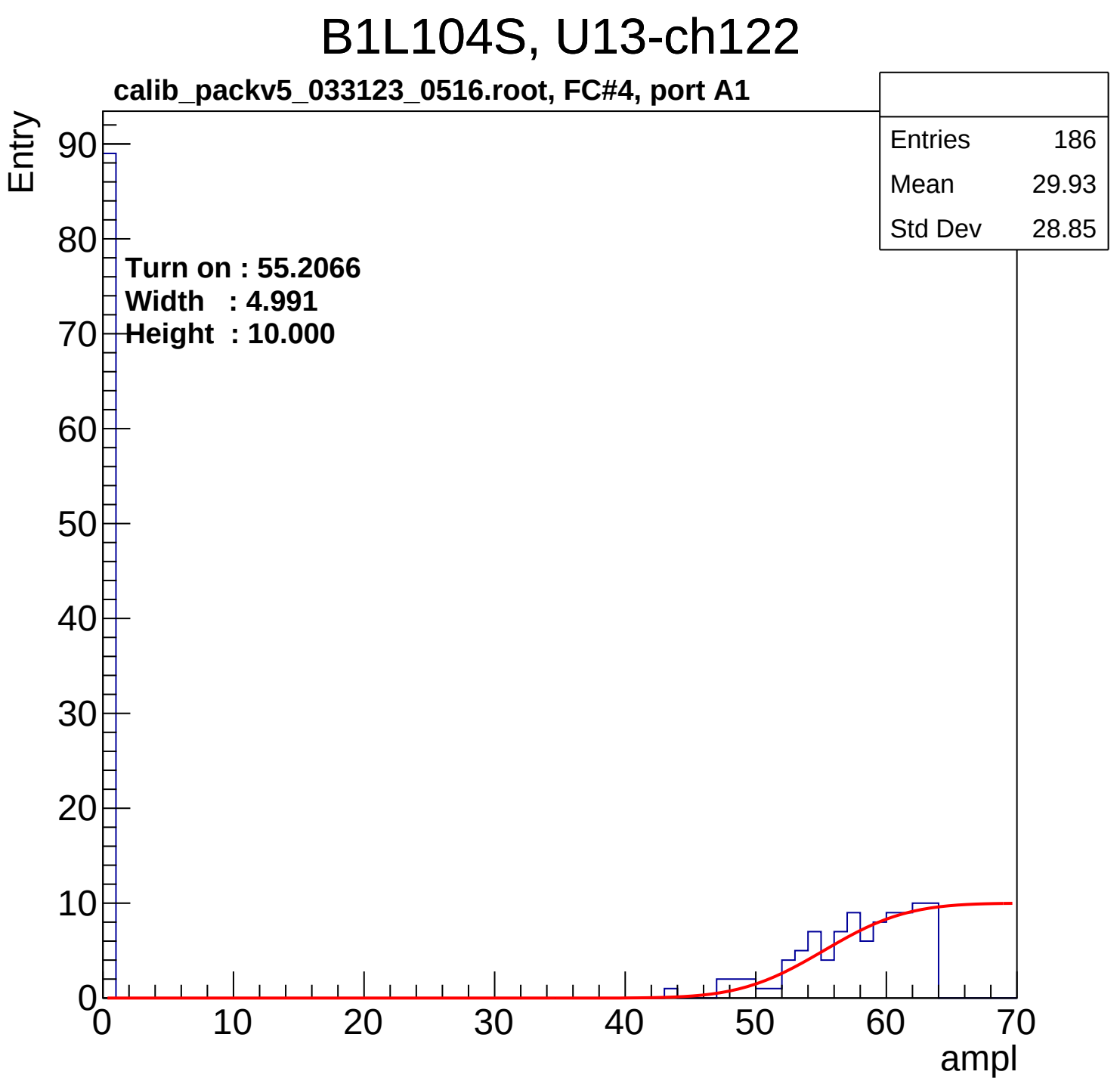
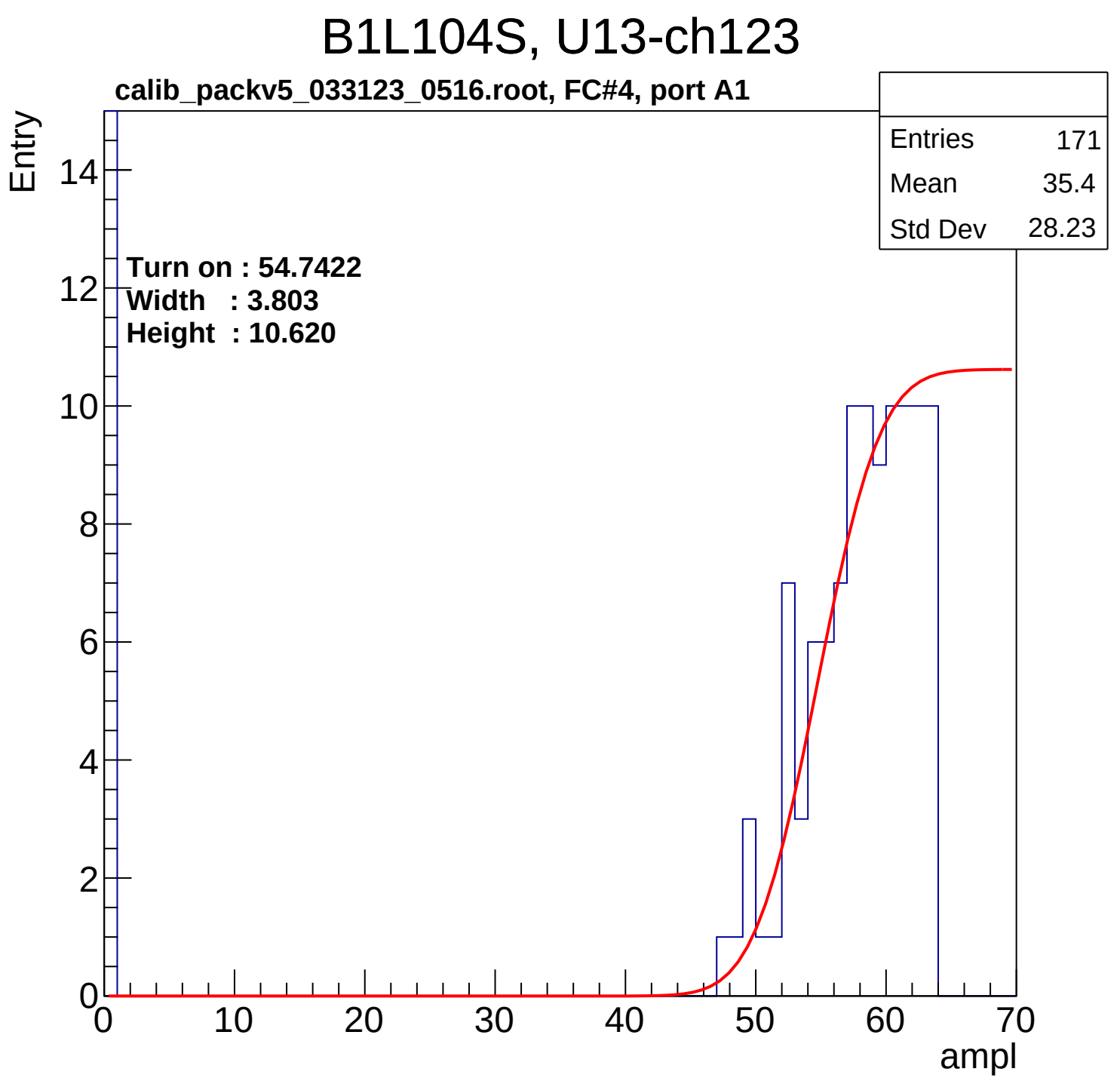
60
70

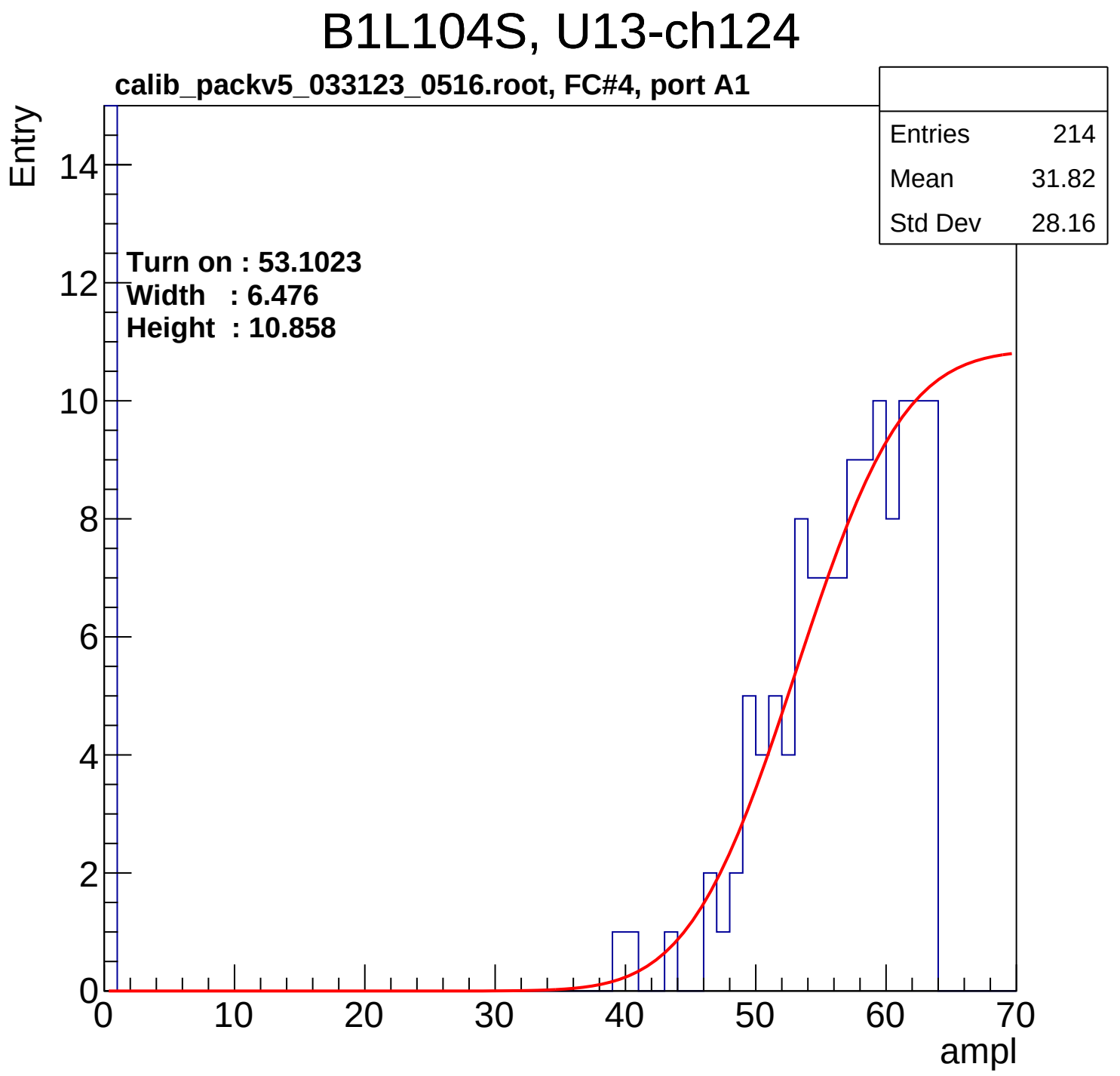

B1L104S, U13-ch119
calib_packv5_033123_0516.root, FC#4, port A1
Entries 202
Mean 28.61
Std Dev 29.03
Turn on : 55.6131
Width : 4.937
Height : 10.667
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

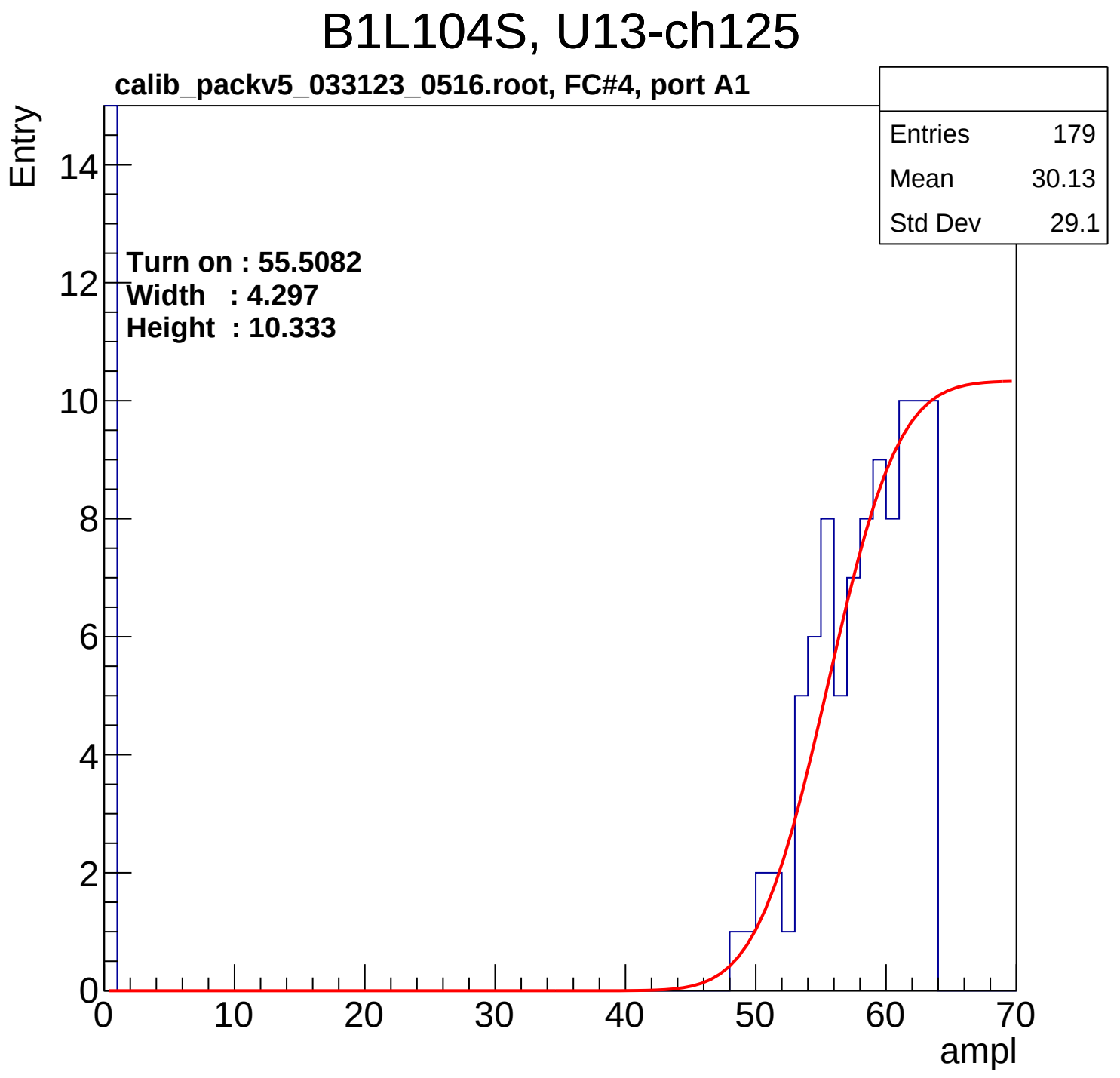

B1L104S, U13-ch120
calib_packv5_033123_0516.root, FC#4, port A1
Entries 253
Mean 31.98
Std Dev 25.3
Turn on : 53.0346
Width : 5.913
Height : 10.772
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

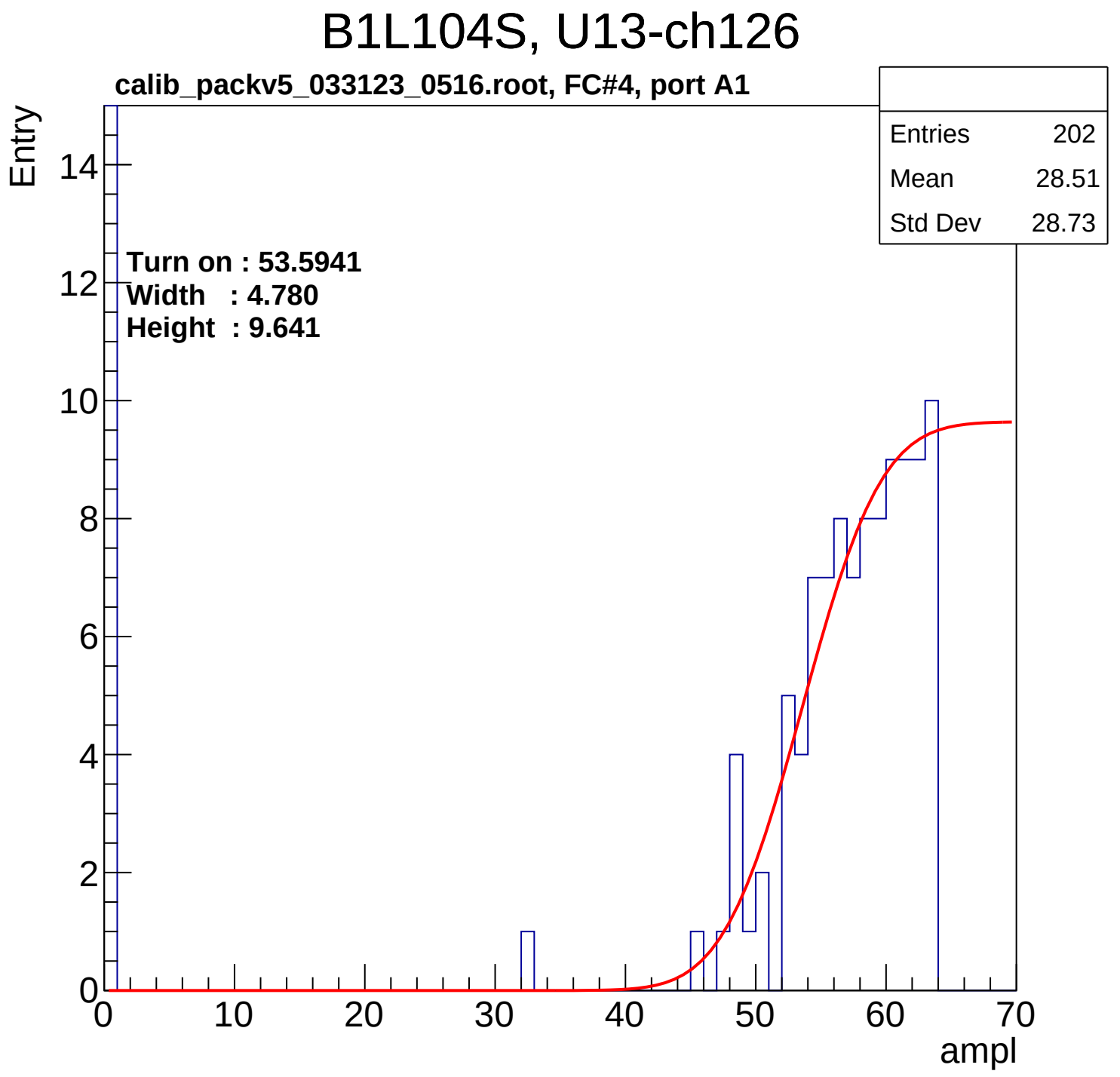

B1L104S, U13-ch121
calib_packv5_033123_0516.root, FC#4, port A1
Entries 168
Mean 35.68
Std Dev 28.19
Turn on : 54.0849
Width : 3.214
Height : 10.203
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L104S, U13-ch122
calib_packv5_033123_0516.root, FC#4, port A1
Entries 186
Mean 29.93
Std Dev 28.85
Turn on : 55.2066
Width : 4.991
Height : 10.000
Entry
ampl
0
10
20
30
40
50
60
70
80
90


B1L104S, U13-ch123
calib_packv5_033123_0516.root, FC#4, port A1
Entries 171
Mean 35.4
Std Dev 28.23
Turn on : 54.7422
Width : 3.803
Height : 10.620
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L104S, U13-ch124
calib_packv5_033123_0516.root, FC#4, port A1
Entries 214
Mean 31.82
Std Dev 28.16
Turn on : 53.1023
Width : 6.476
Height : 10.858
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L104S, U13-ch125
calib_packv5_033123_0516.root, FC#4, port A1
Entries 179
Mean 30.13
Std Dev 29.1
Turn on : 55.5082
Width : 4.297
Height : 10.333
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L104S, U13-ch126
calib_packv5_033123_0516.root, FC#4, port A1
Entries 202
Mean 28.51
Std Dev 28.73
Turn on : 53.5941
Width : 4.780
Height : 9.641
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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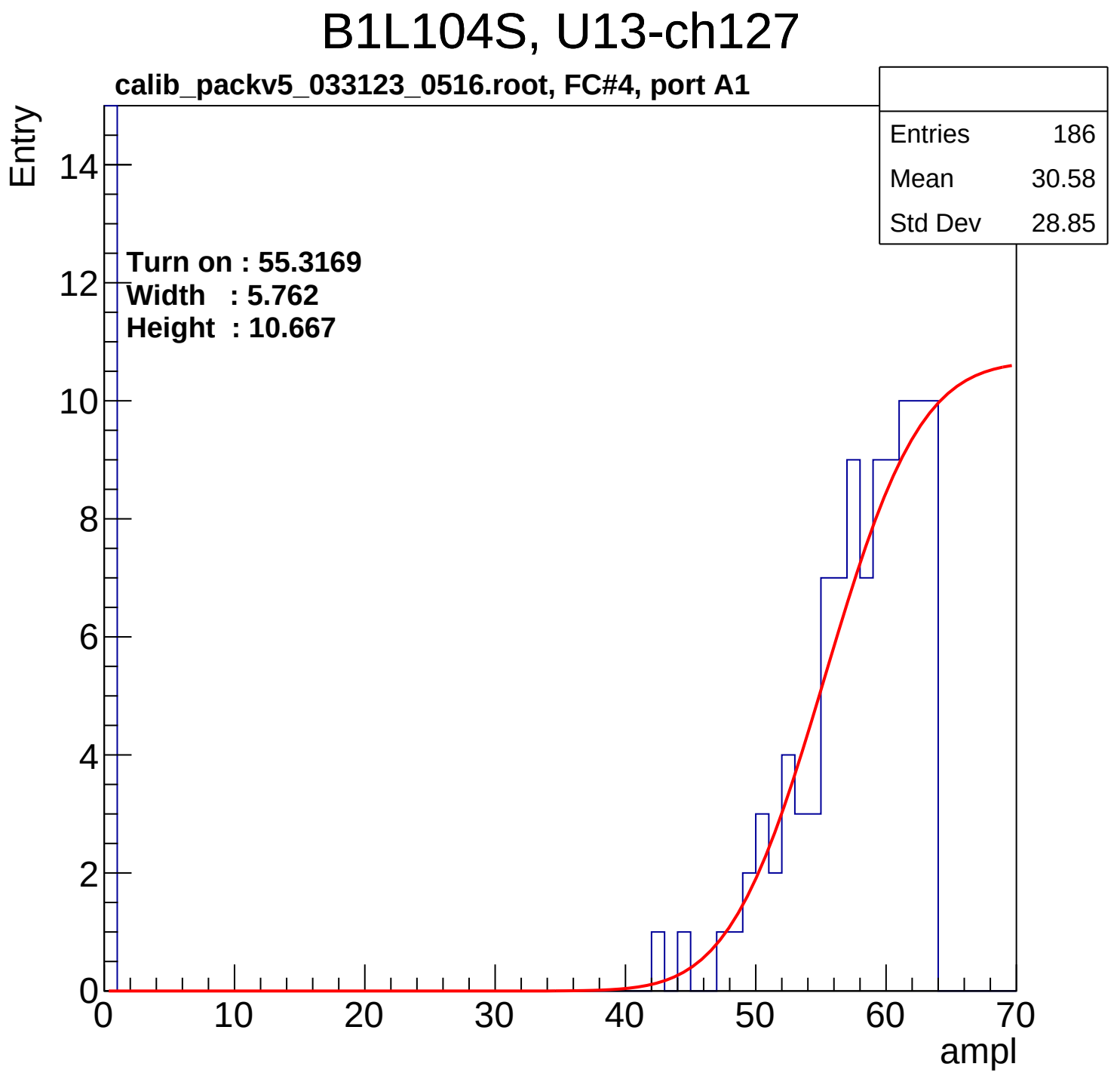
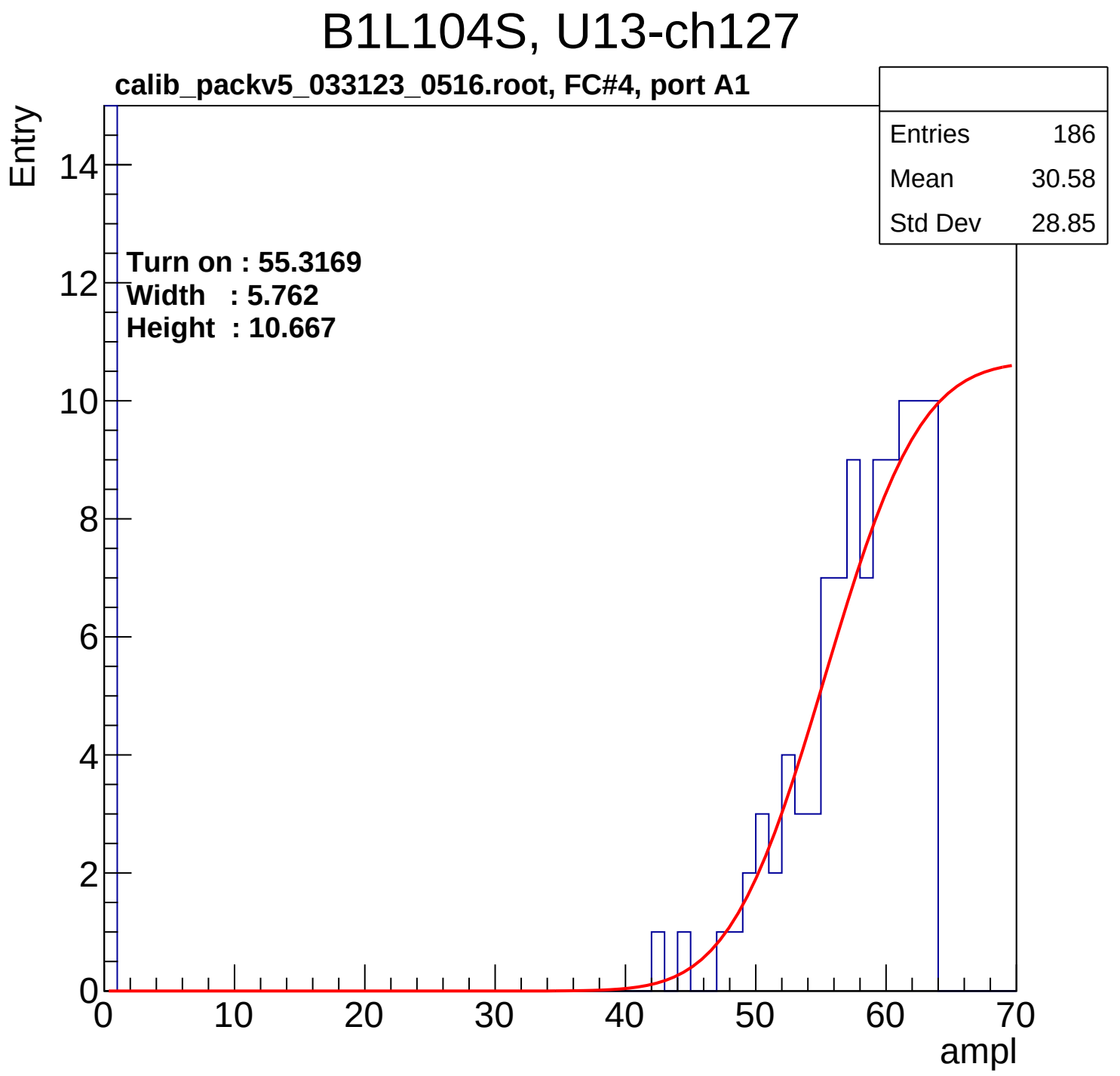
40
50
60
70


B1L104S, U13-ch127
calib_packv5_033123_0516.root, FC#4, port A1
Entries 186
Mean 30.58
Std Dev 28.85
Turn on : 55.3169
Width : 5.762
Height : 10.667
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L104S, U13-ch127
calib_packv5_033123_0516.root, FC#4, port A1
Entries 186
Mean 30.58
Std Dev 28.85
Turn on : 55.3169
Width : 5.762
Height : 10.667
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70