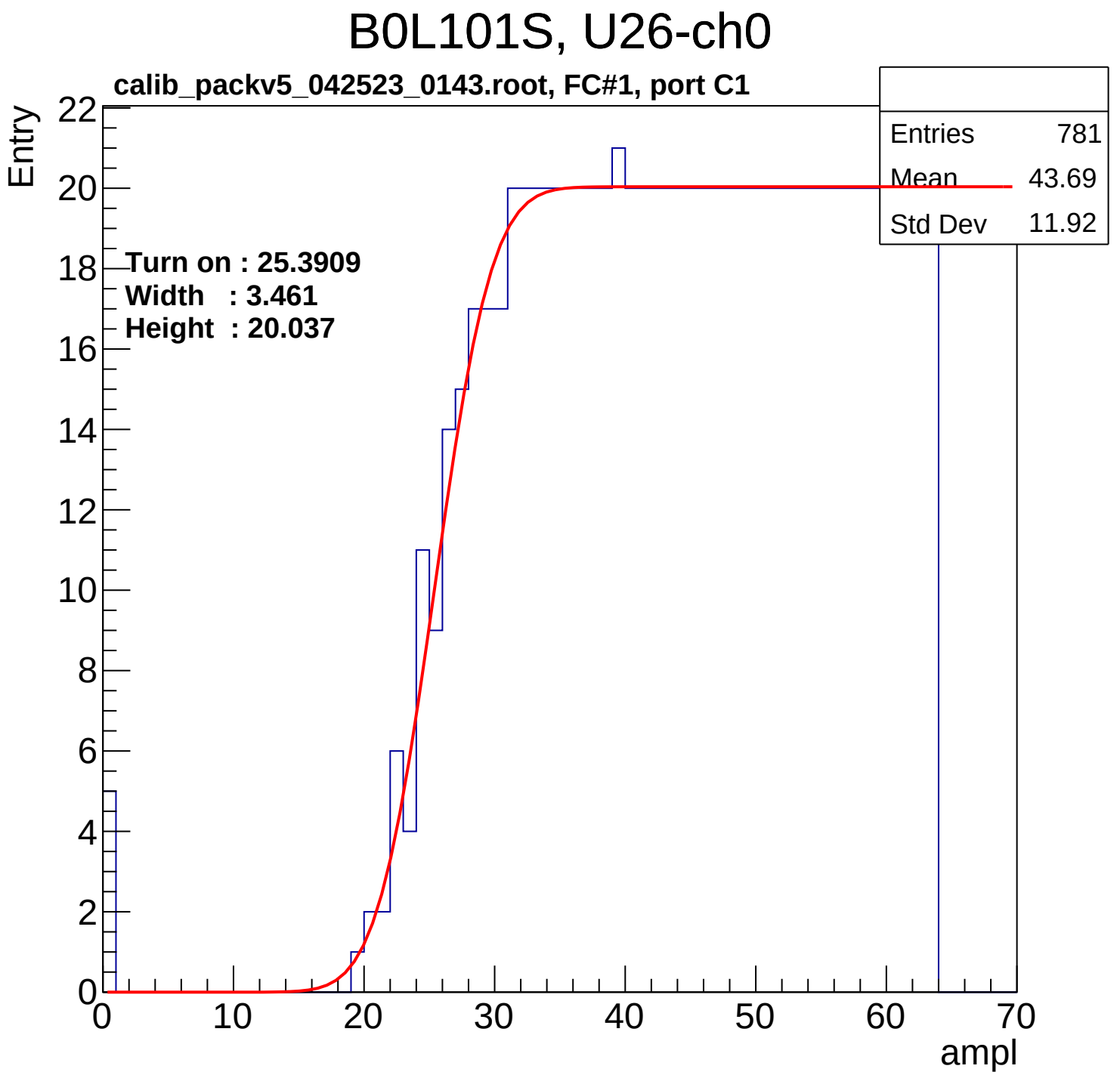
B0L101S, U26-ch0
calib_packv5_042523_0143.root, FC#1, port C1
Entries 781
Mean 43.69
Std Dev 11.92
Turn on : 25.3909
Width : 3.461
Height : 20.037
Entry
ampl
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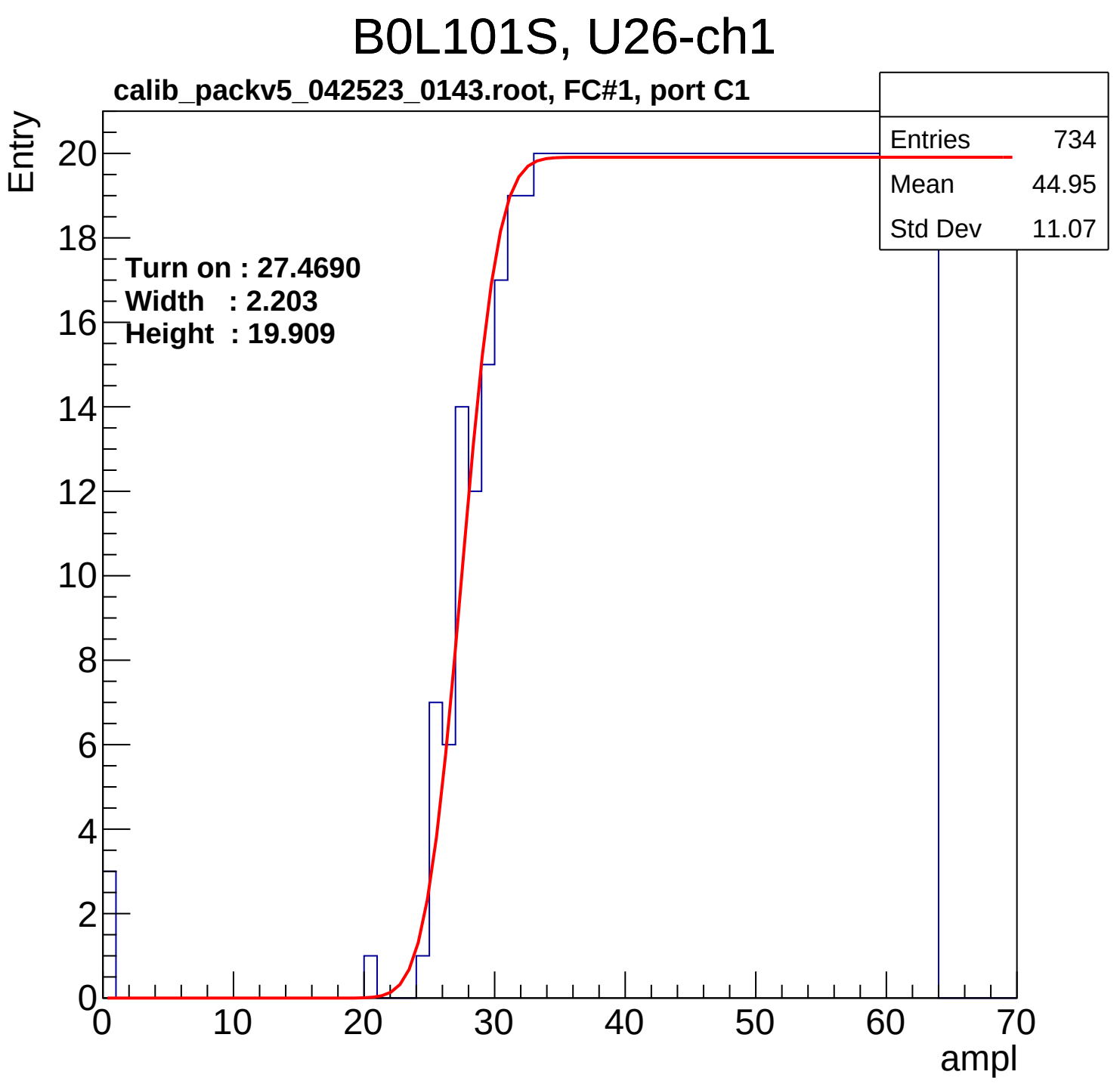
B0L101S, U26-ch1
calib_packv5_042523_0143.root, FC#1, port C1
Entries 734
Mean 44.95
Std Dev 11.07
Turn on : 27.4690
Width : 2.203
Height : 19.909
Entry
ampl
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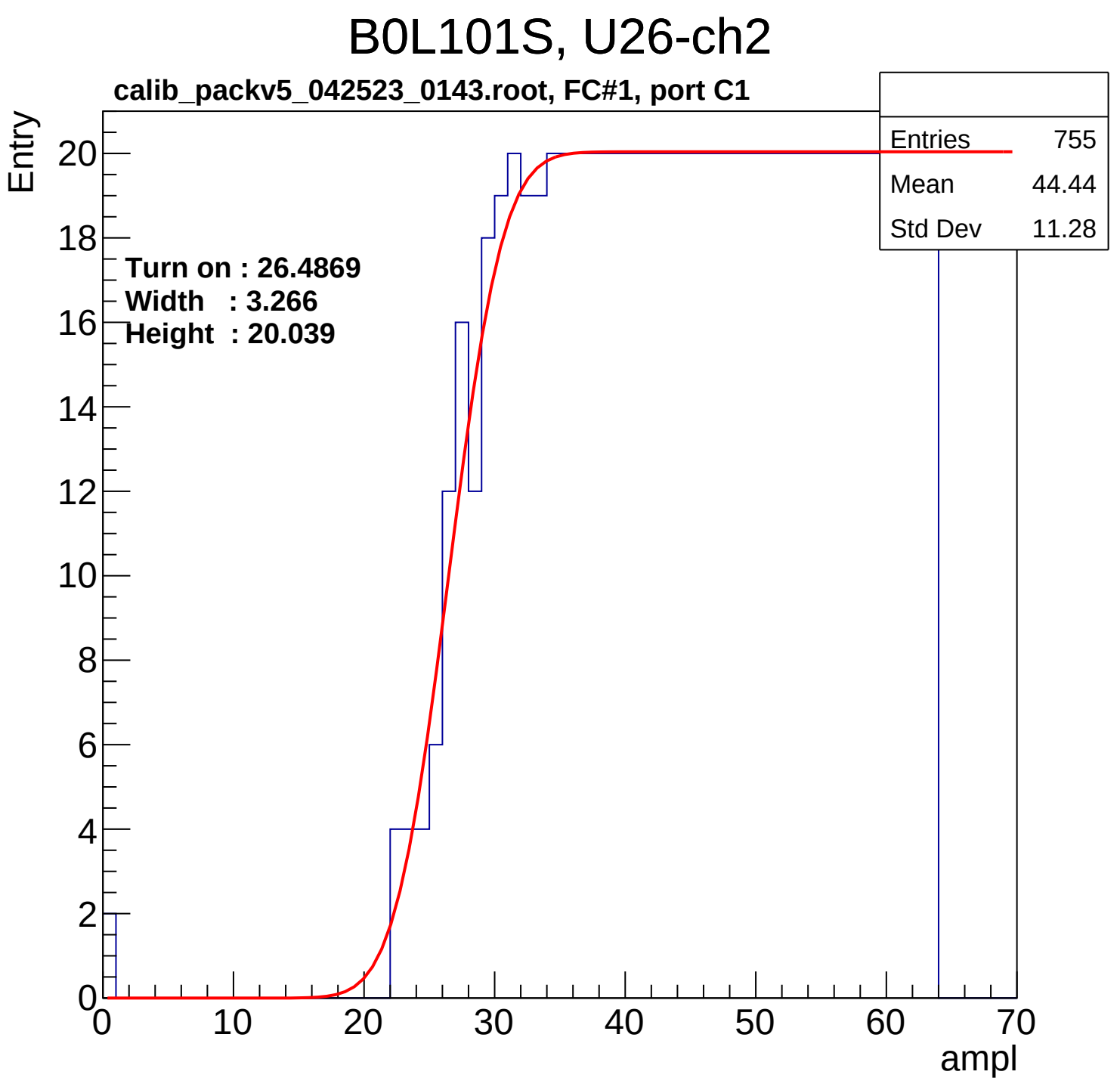
B0L101S, U26-ch2
calib_packv5_042523_0143.root, FC#1, port C1
Entries 755
Mean 44.44
Std Dev 11.28
Turn on : 26.4869
Width : 3.266
Height : 20.039
Entry
ampl
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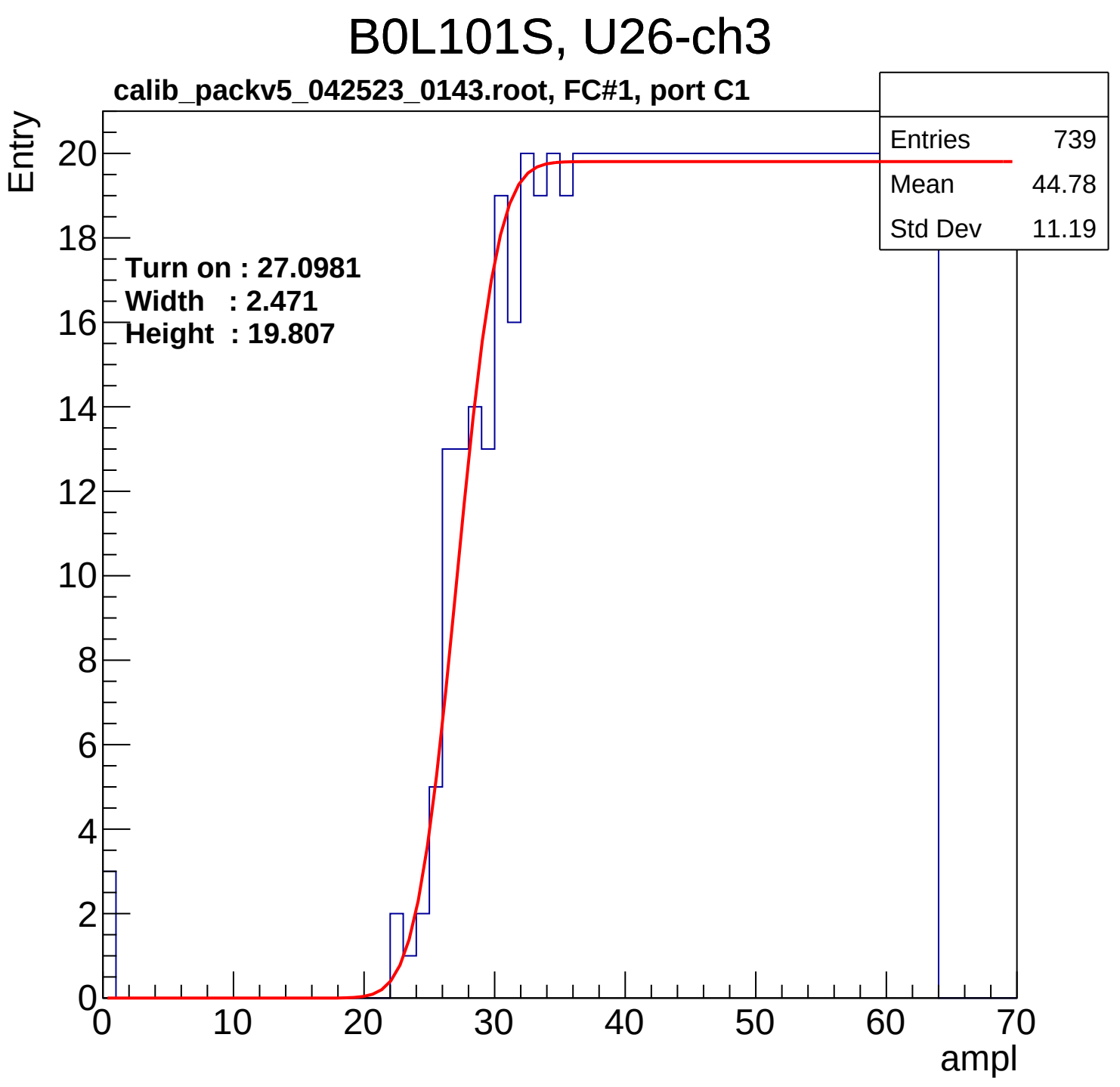
B0L101S, U26-ch3
calib_packv5_042523_0143.root, FC#1, port C1
Entries 739
Mean 44.78
Std Dev 11.19
Turn on : 27.0981
Width : 2.471
Height : 19.807
Entry
ampl
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6
8
10
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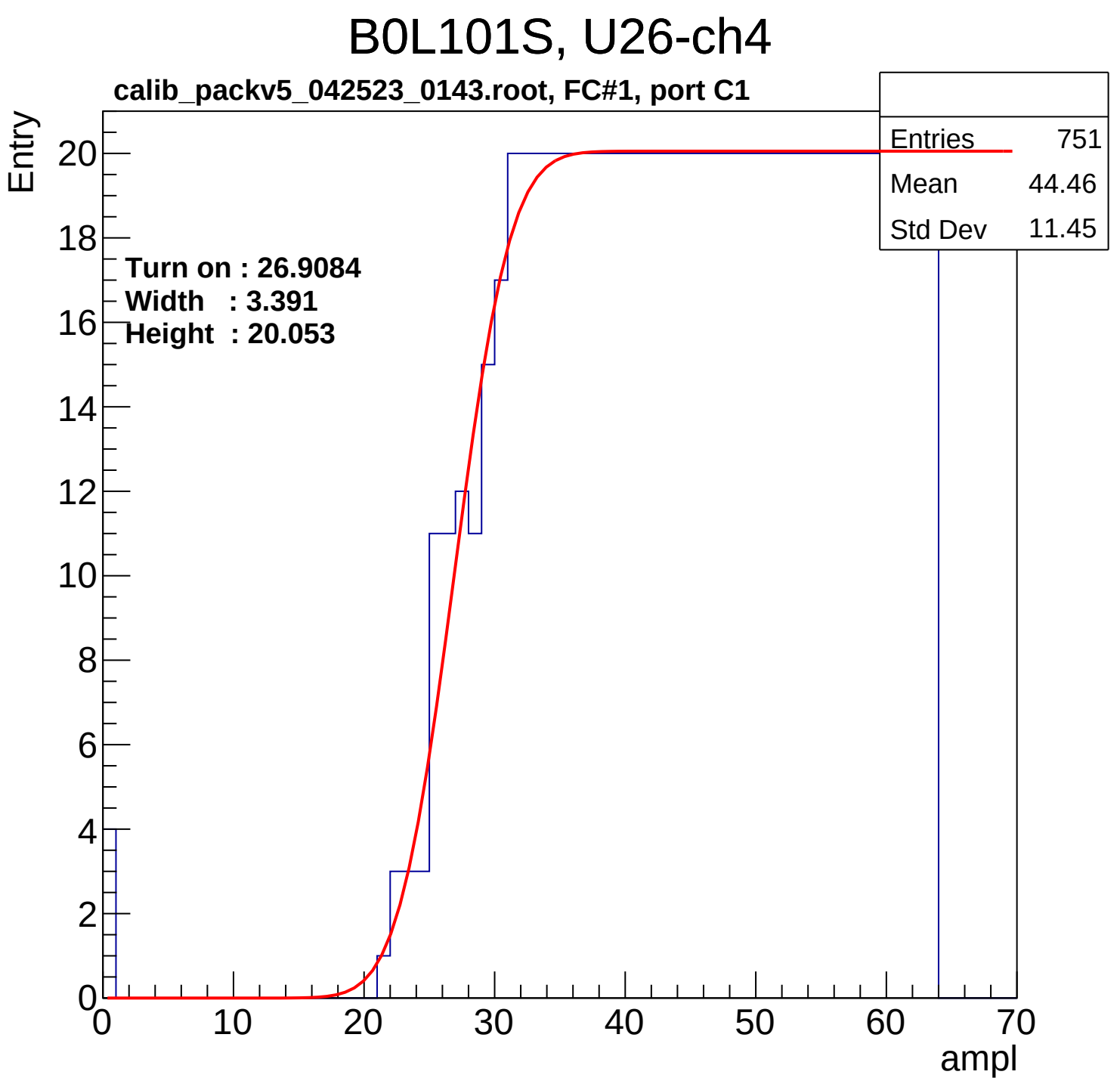
B0L101S, U26-ch4
calib_packv5_042523_0143.root, FC#1, port C1
Entries 751
Mean 44.46
Std Dev 11.45
Turn on : 26.9084
Width : 3.391
Height : 20.053
Entry
ampl
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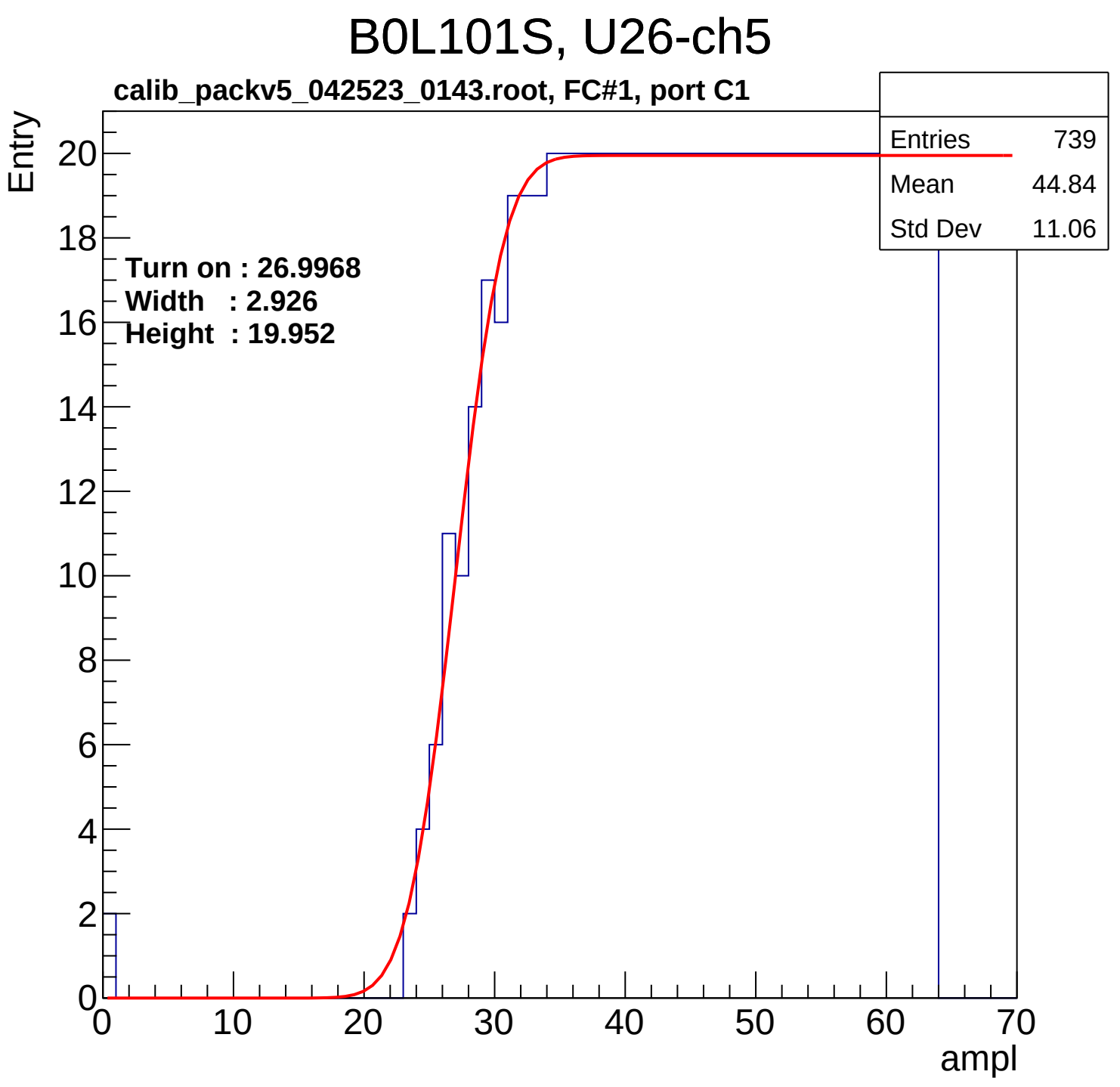
B0L101S, U26-ch5
calib_packv5_042523_0143.root, FC#1, port C1
Entries 739
Mean 44.84
Std Dev 11.06
Turn on : 26.9968
Width : 2.926
Height : 19.952
Entry
ampl
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6
8
10
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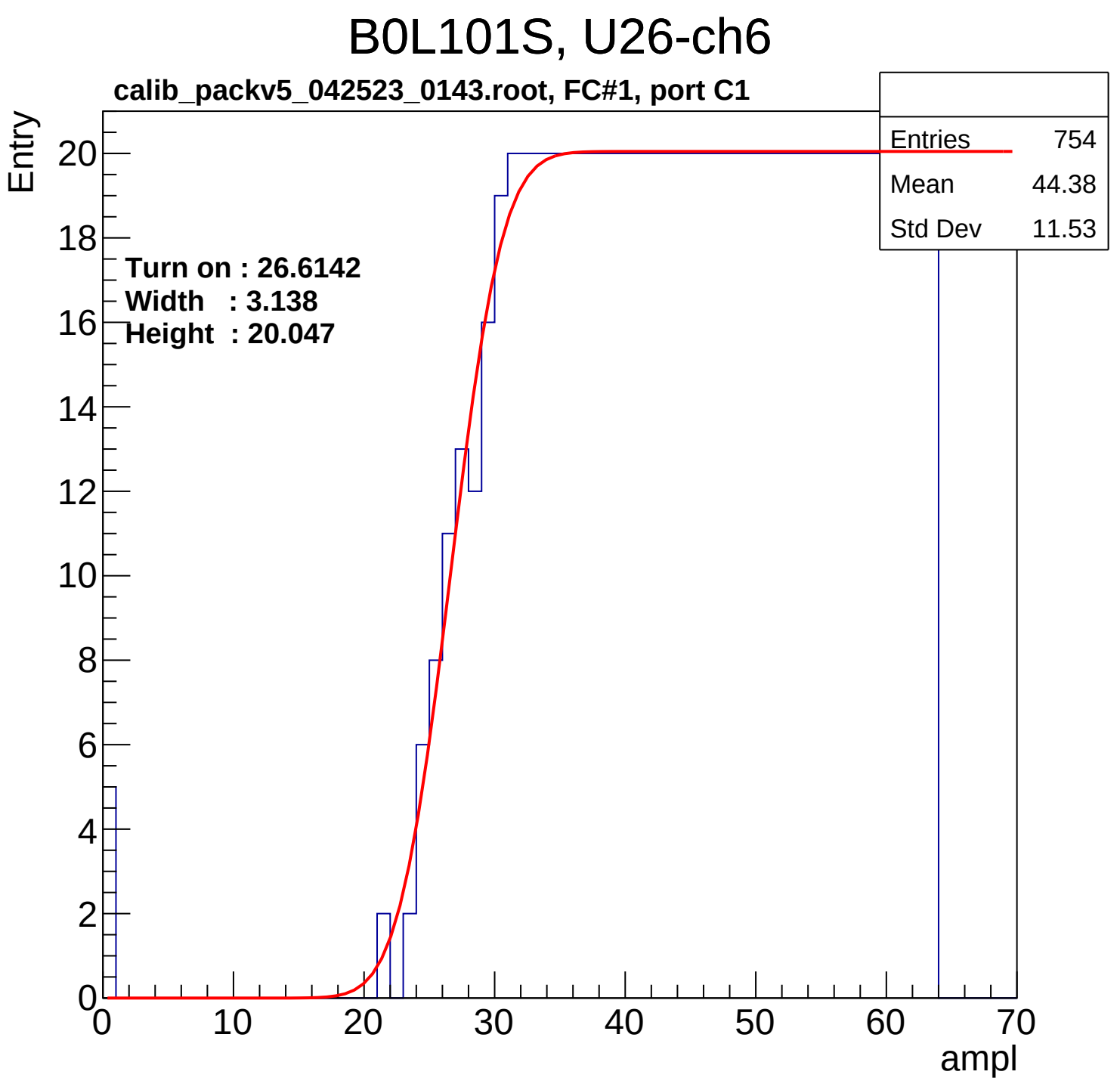
B0L101S, U26-ch6
calib_packv5_042523_0143.root, FC#1, port C1
Entries 754
Mean 44.38
Std Dev 11.53
Turn on : 26.6142
Width : 3.138
Height : 20.047
Entry
ampl
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8
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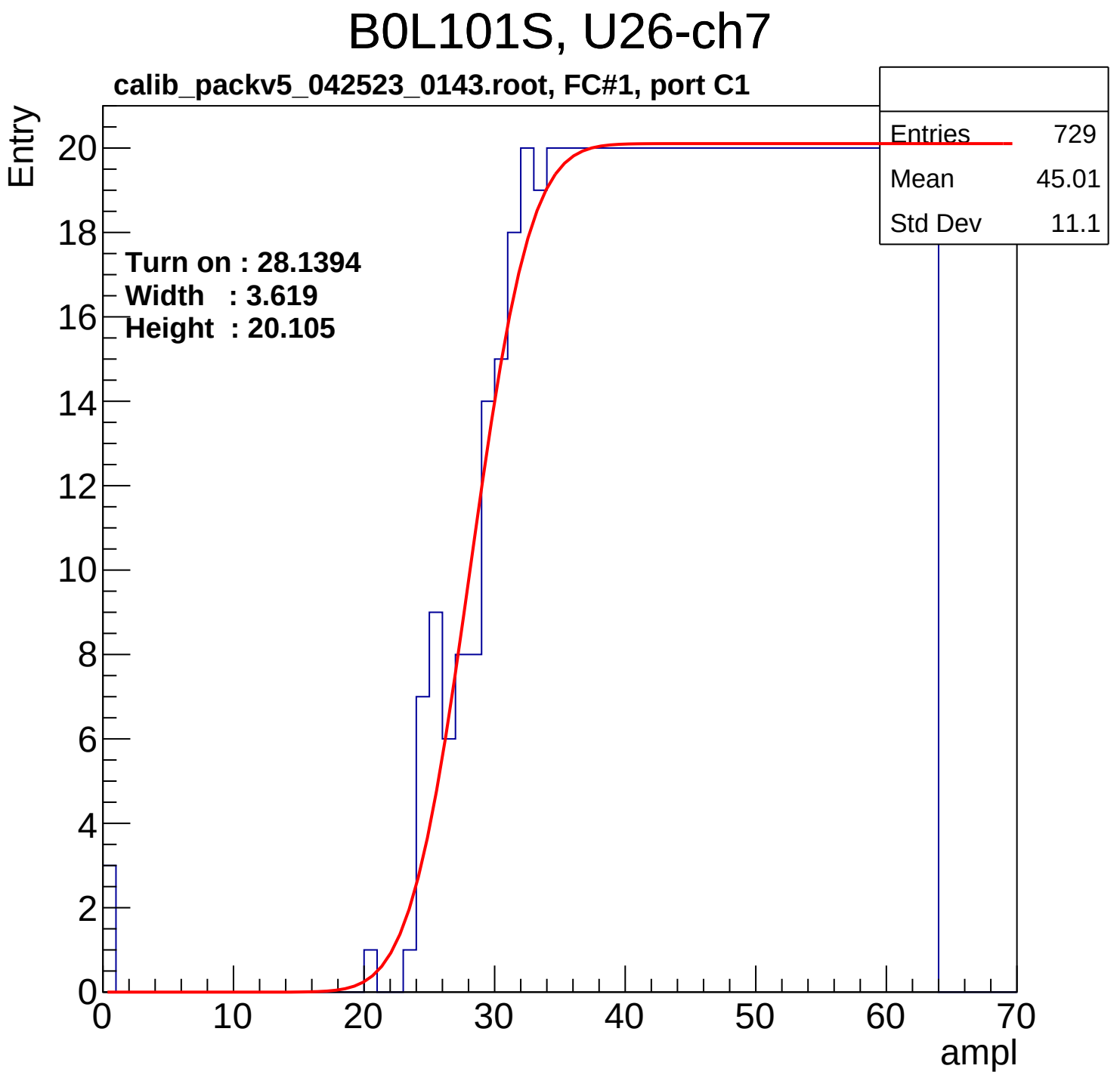
B0L101S, U26-ch7
calib_packv5_042523_0143.root, FC#1, port C1
Entries 729
Mean 45.01
Std Dev 11.1
Turn on : 28.1394
Width : 3.619
Height : 20.105
Entry
ampl
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6
8
10
12
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16
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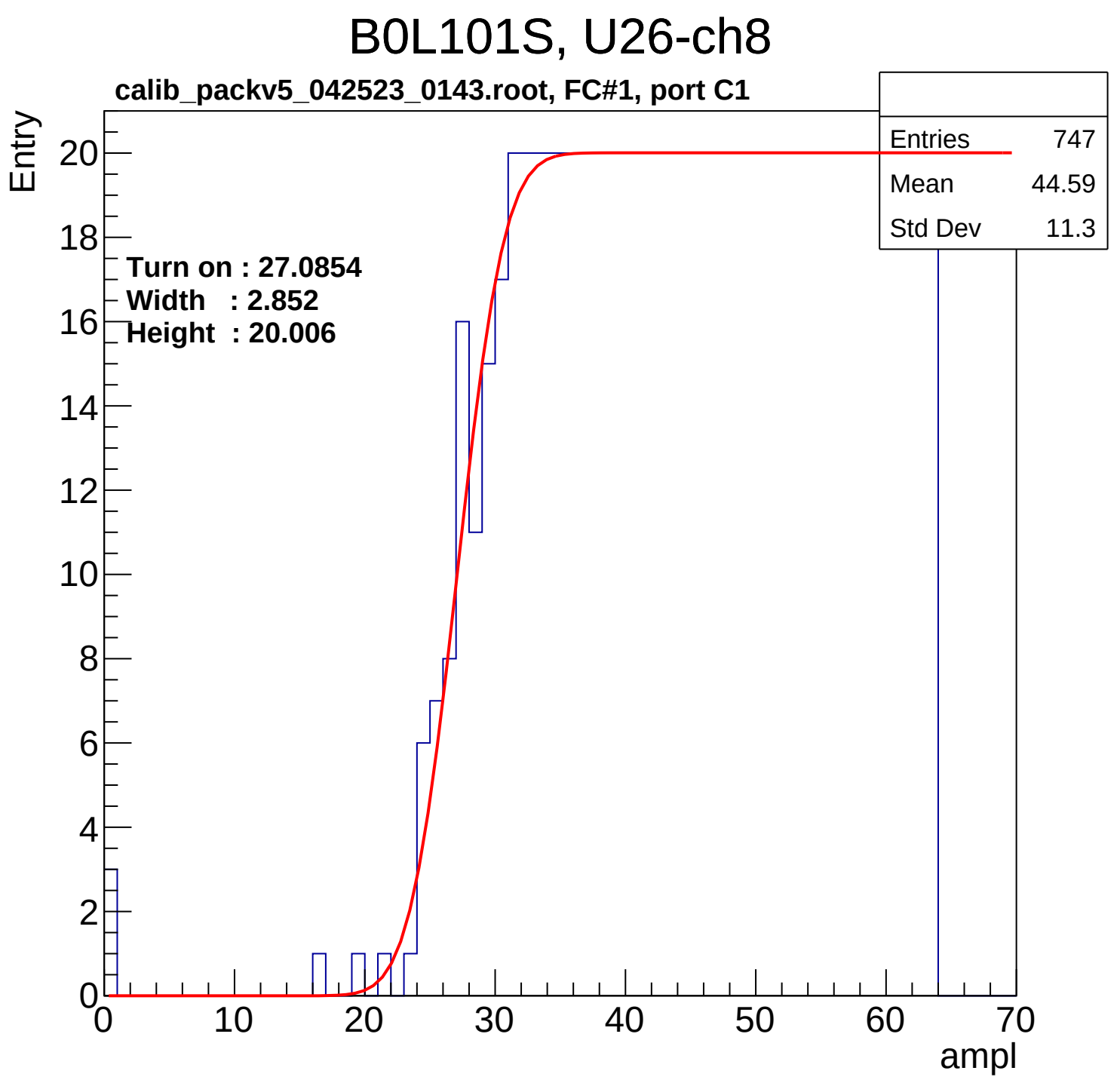
B0L101S, U26-ch8
calib_packv5_042523_0143.root, FC#1, port C1
Entries 747
Mean 44.59
Std Dev 11.3
Turn on : 27.0854
Width : 2.852
Height : 20.006
Entry
ampl
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6
8
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12
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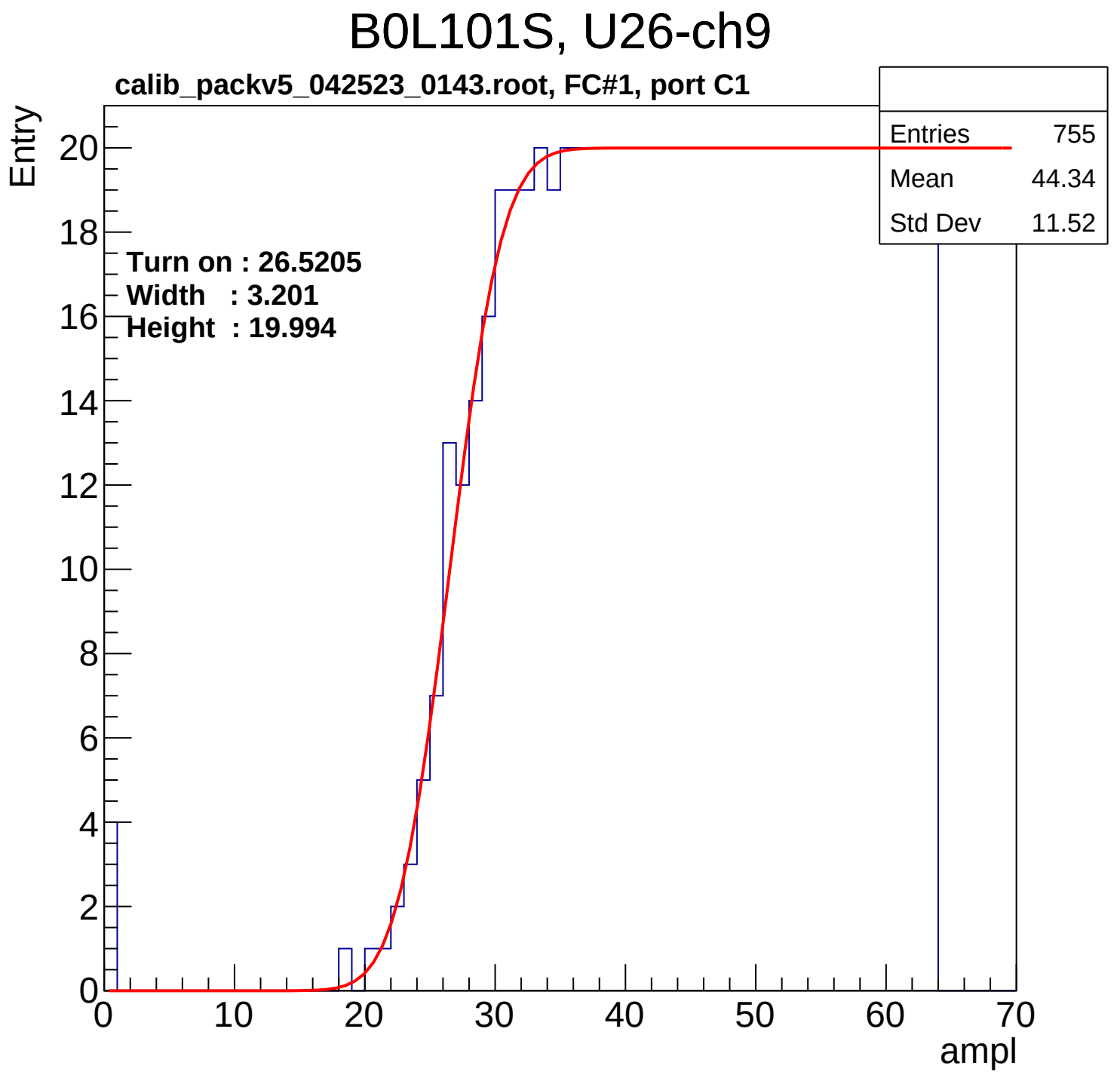
B0L101S, U26-ch9
calib_packv5_042523_0143.root, FC#1, port C1
Entries 755
Mean 44.34
Std Dev 11.52
Turn on : 26.5205
Width : 3.201
Height : 19.994
Entry
ampl
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6
8
10
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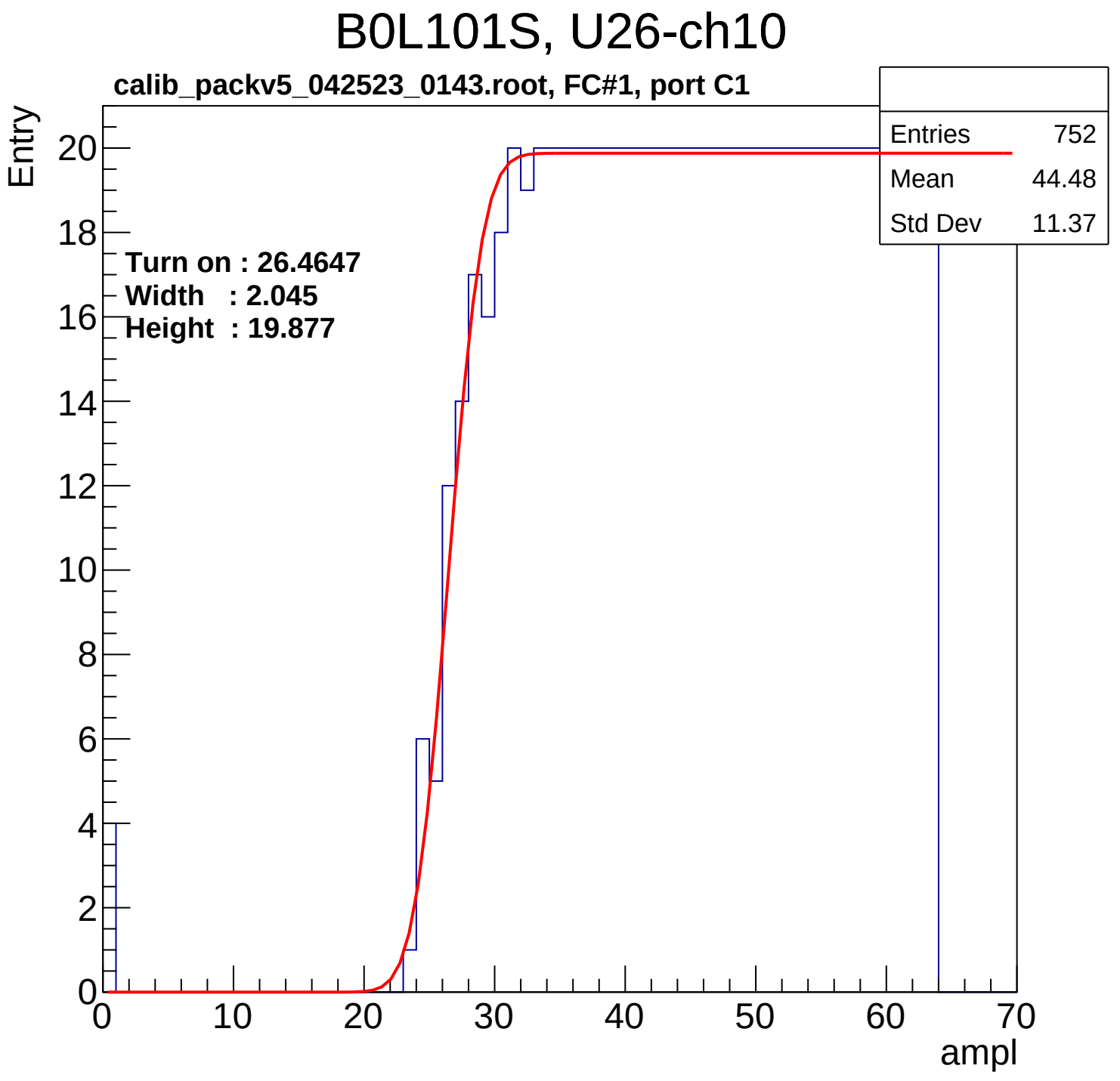
B0L101S, U26-ch10
calib_packv5_042523_0143.root, FC#1, port C1
Entries 752
Mean 44.48
Std Dev 11.37
Turn on : 26.4647
Width : 2.045
Height : 19.877
Entry
ampl
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6
8
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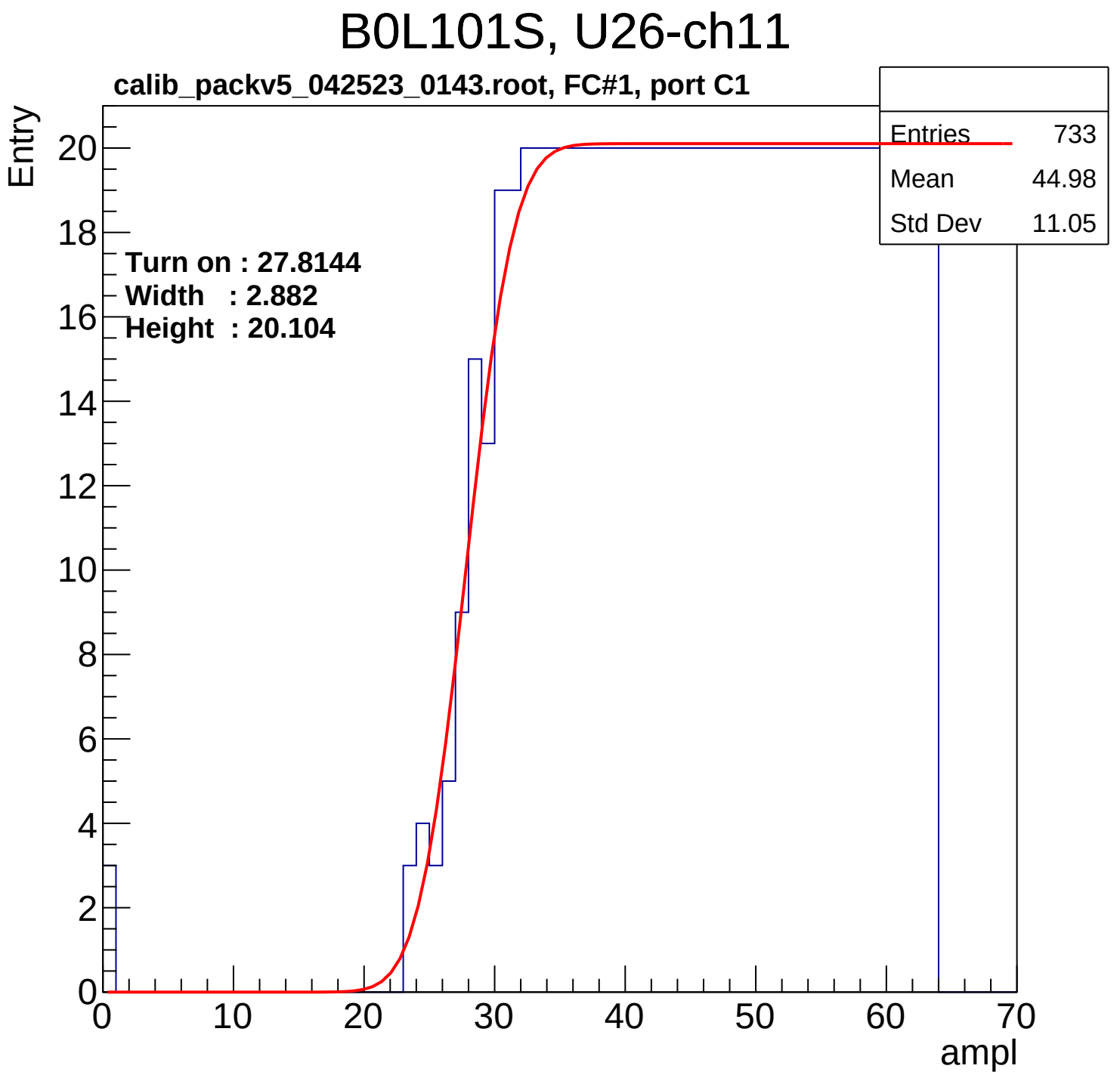
B0L101S, U26-ch11
calib_packv5_042523_0143.root, FC#1, port C1
Entries 733
Mean 44.98
Std Dev 11.05
Turn on : 27.8144
Width : 2.882
Height : 20.104
Entry
ampl
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6
8
10
12
14
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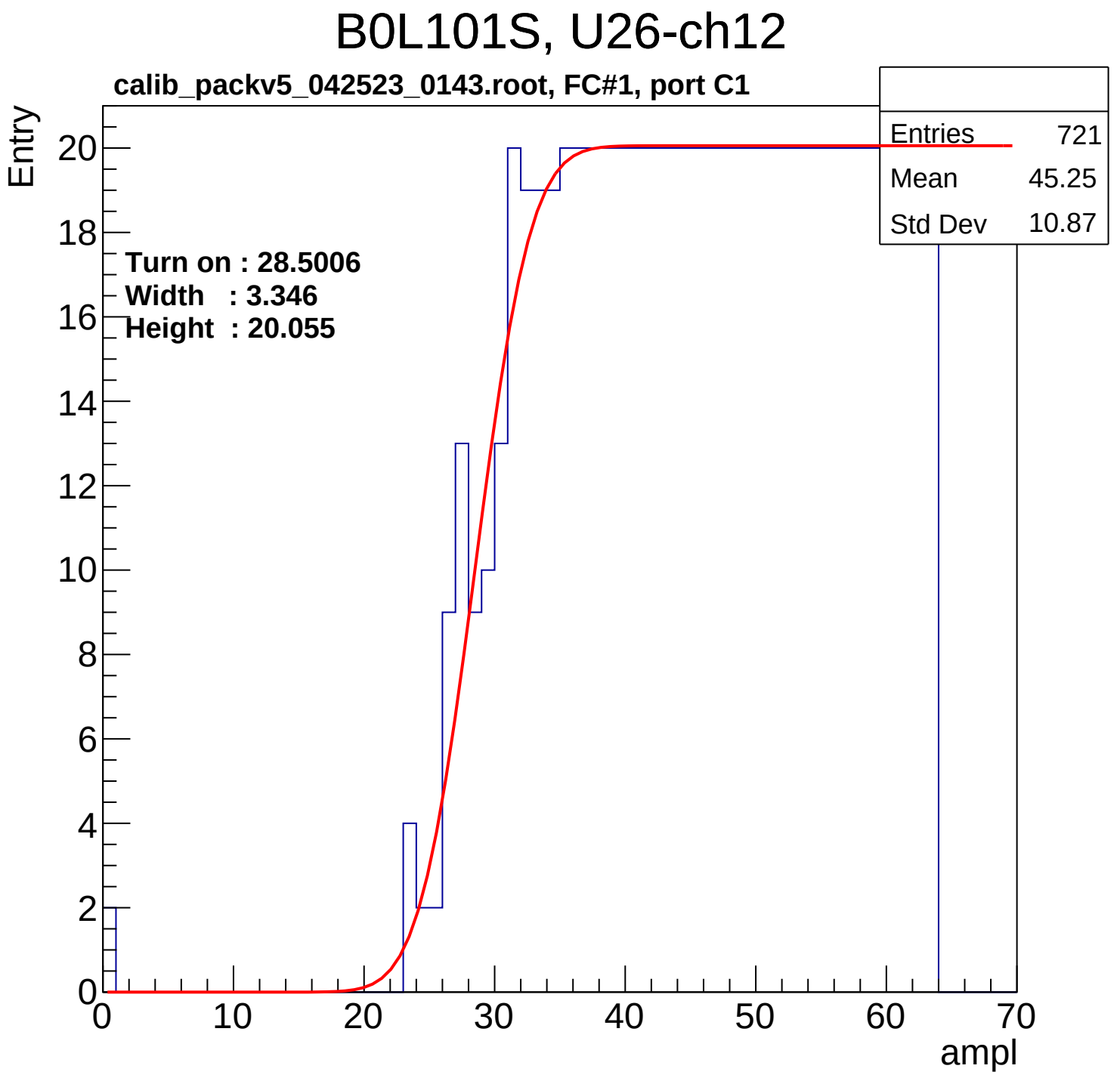
B0L101S, U26-ch12
calib_packv5_042523_0143.root, FC#1, port C1
Entries 721
Mean 45.25
Std Dev 10.87
Turn on : 28.5006
Width : 3.346
Height : 20.055
Entry
ampl
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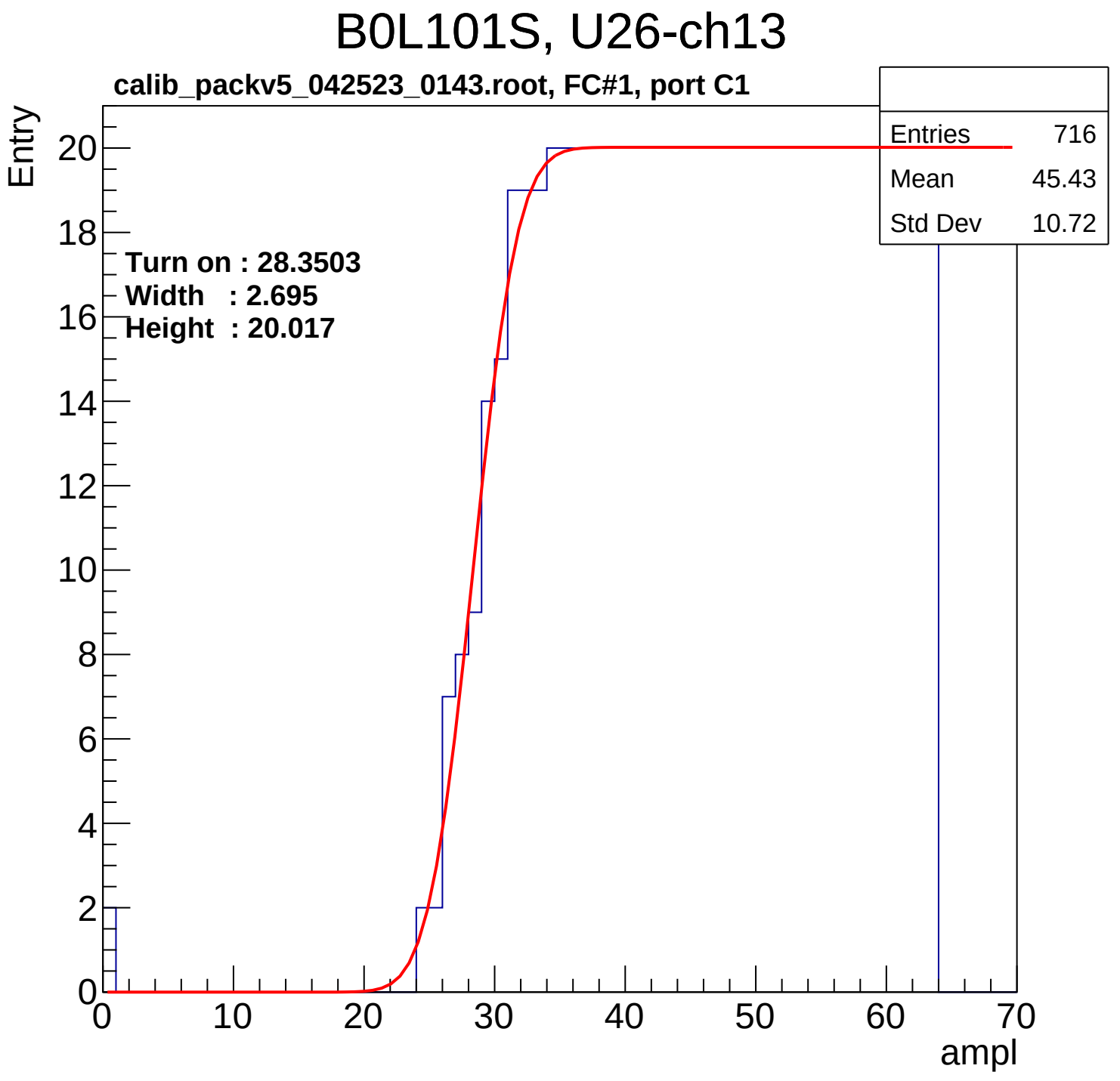
B0L101S, U26-ch13
calib_packv5_042523_0143.root, FC#1, port C1
Entries 716
Mean 45.43
Std Dev 10.72
Turn on : 28.3503
Width : 2.695
Height : 20.017
Entry
ampl
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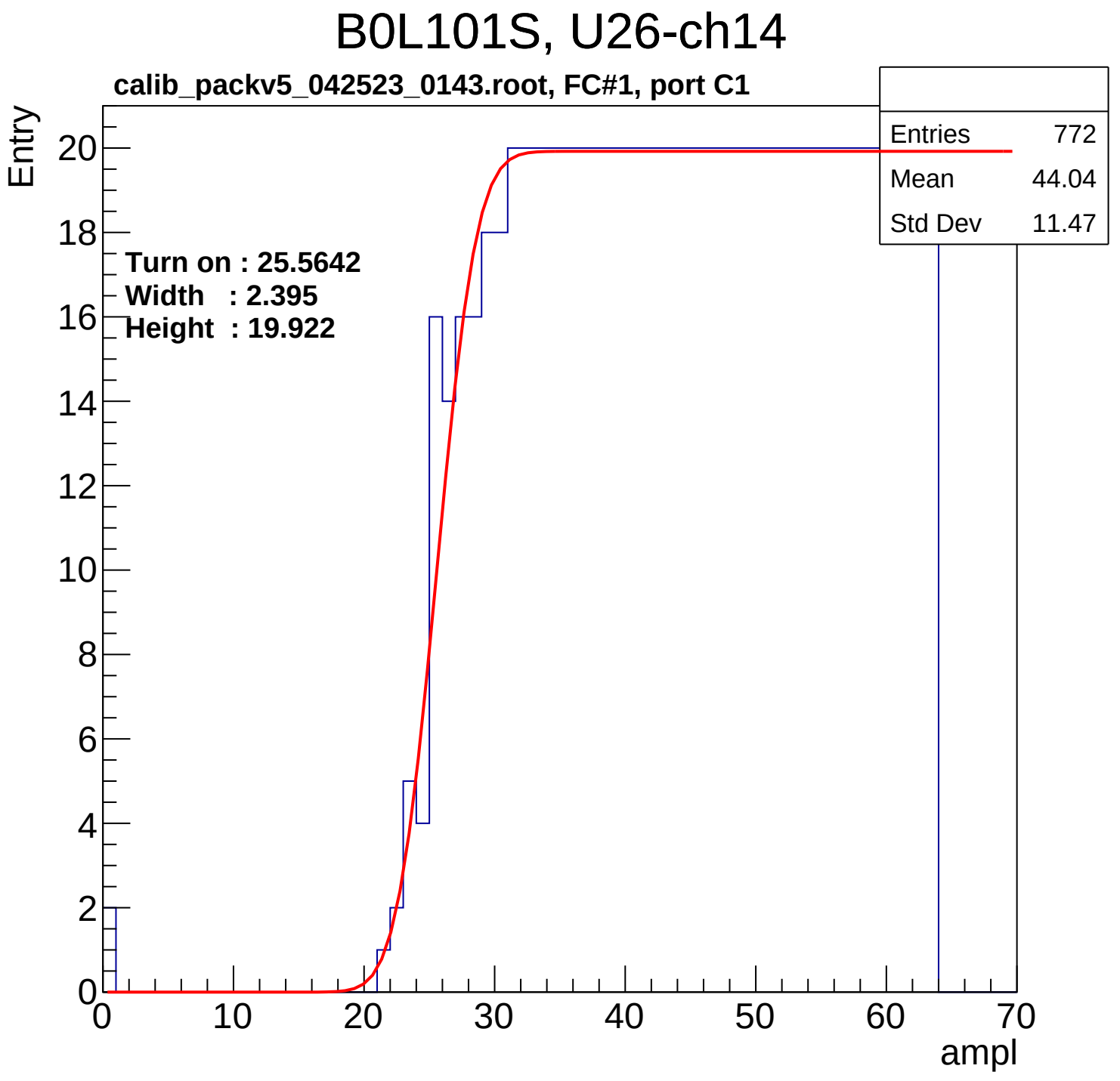
B0L101S, U26-ch14
calib_packv5_042523_0143.root, FC#1, port C1
Entries 772
Mean 44.04
Std Dev 11.47
Turn on : 25.5642
Width : 2.395
Height : 19.922
Entry
ampl
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6
8
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12
14
16
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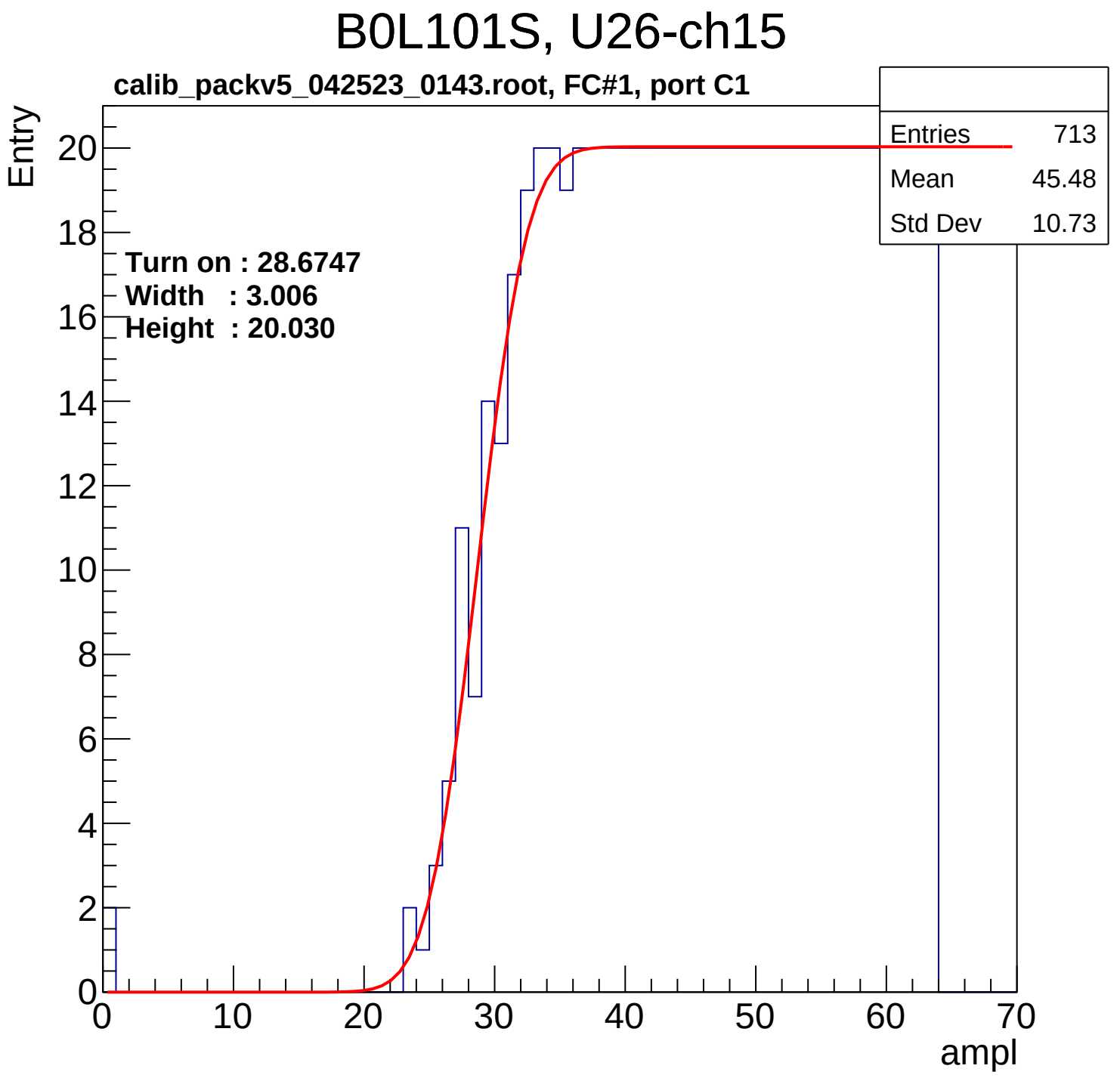
B0L101S, U26-ch15
calib_packv5_042523_0143.root, FC#1, port C1
Entries 713
Mean 45.48
Std Dev 10.73
Turn on : 28.6747
Width : 3.006
Height : 20.030
Entry
ampl
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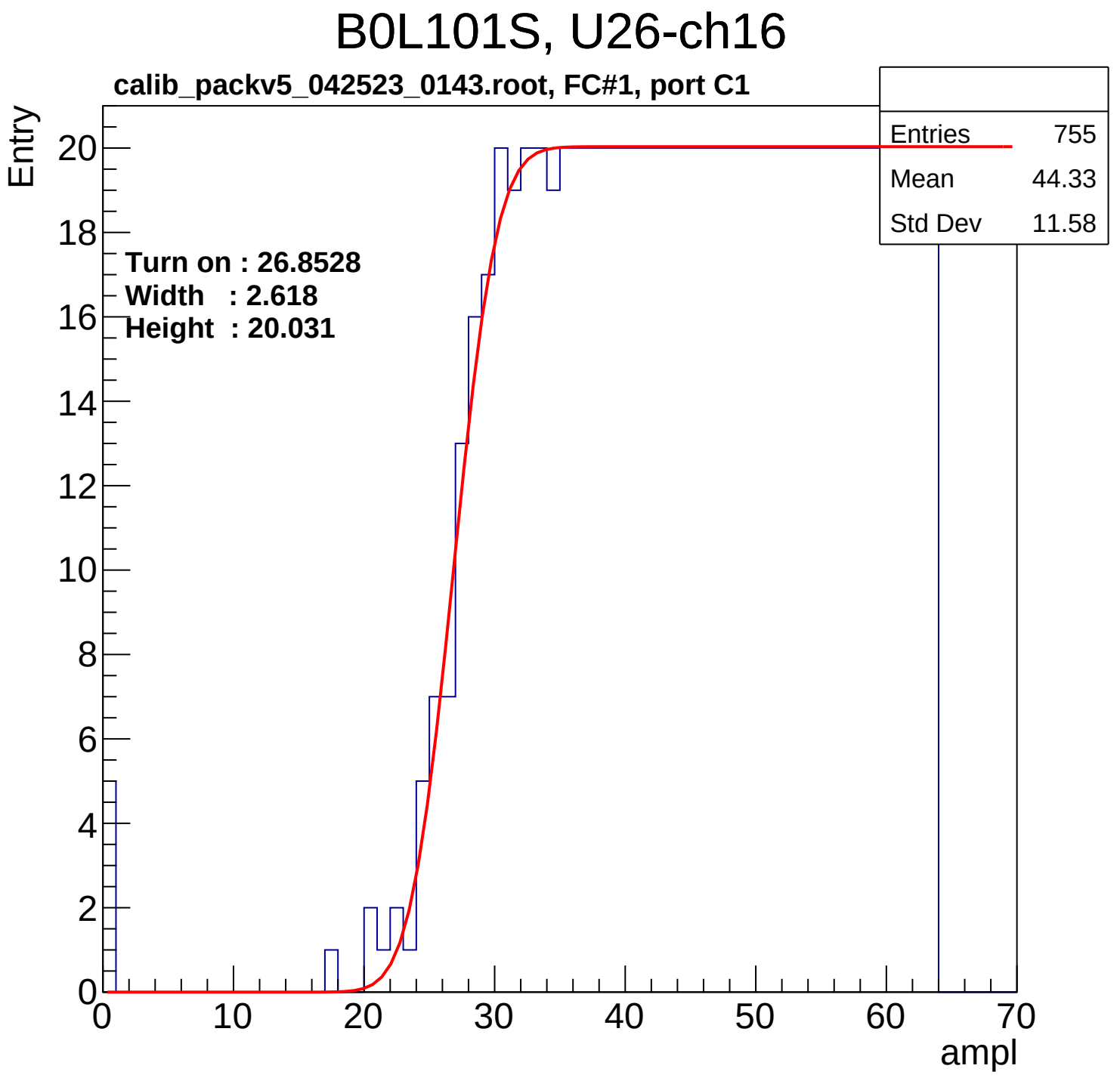
B0L101S, U26-ch16
calib_packv5_042523_0143.root, FC#1, port C1
Entries 755
Mean 44.33
Std Dev 11.58
Turn on : 26.8528
Width : 2.618
Height : 20.031
Entry
ampl
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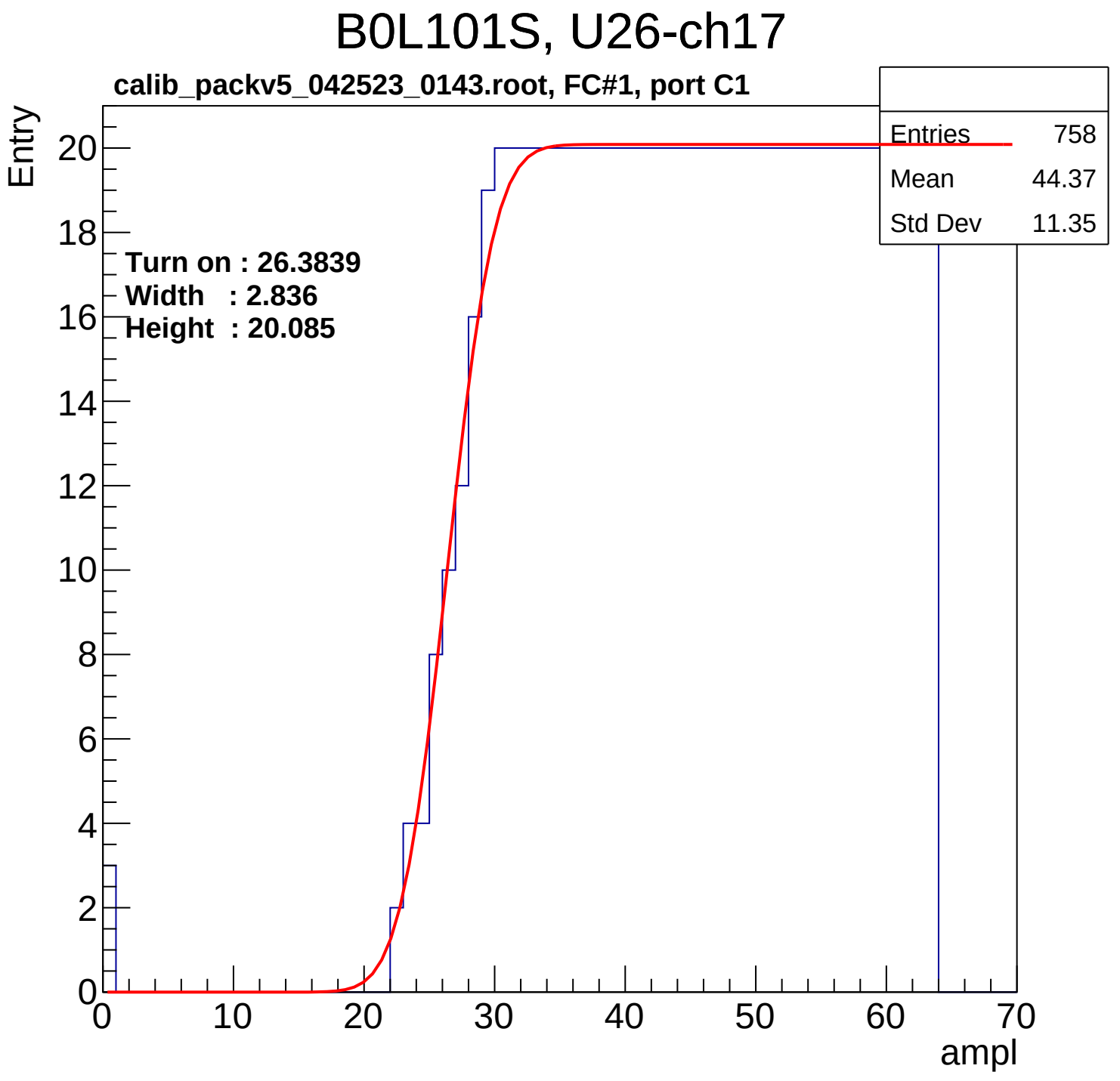
B0L101S, U26-ch17
calib_packv5_042523_0143.root, FC#1, port C1
Entries 758
Mean 44.37
Std Dev 11.35
Turn on : 26.3839
Width : 2.836
Height : 20.085
Entry
ampl
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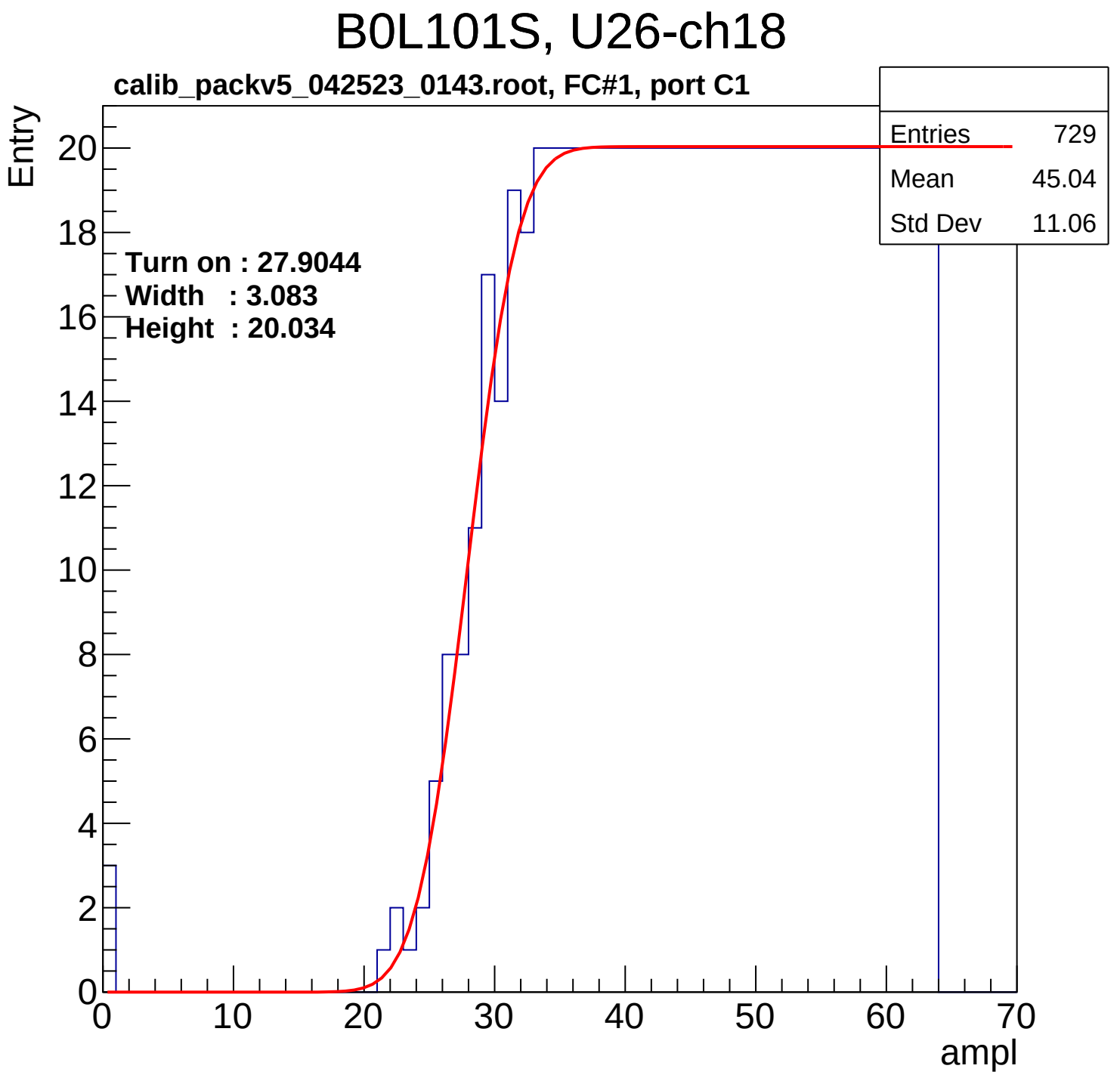
B0L101S, U26-ch18
calib_packv5_042523_0143.root, FC#1, port C1
Entries 729
Mean 45.04
Std Dev 11.06
Turn on : 27.9044
Width : 3.083
Height : 20.034
Entry
ampl
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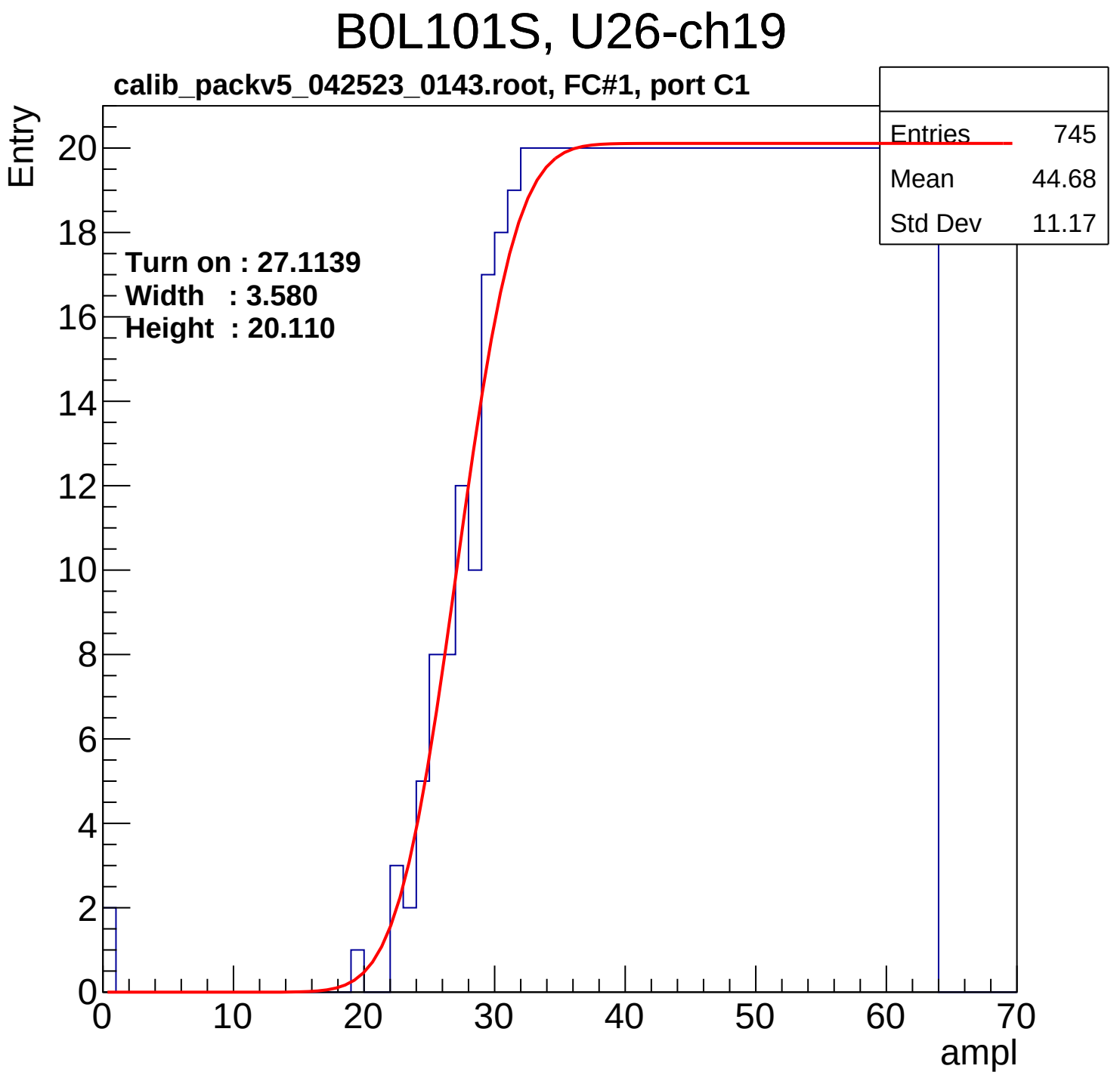
B0L101S, U26-ch19
calib_packv5_042523_0143.root, FC#1, port C1
Entries 745
Mean 44.68
Std Dev 11.17
Turn on : 27.1139
Width : 3.580
Height : 20.110
Entry
ampl
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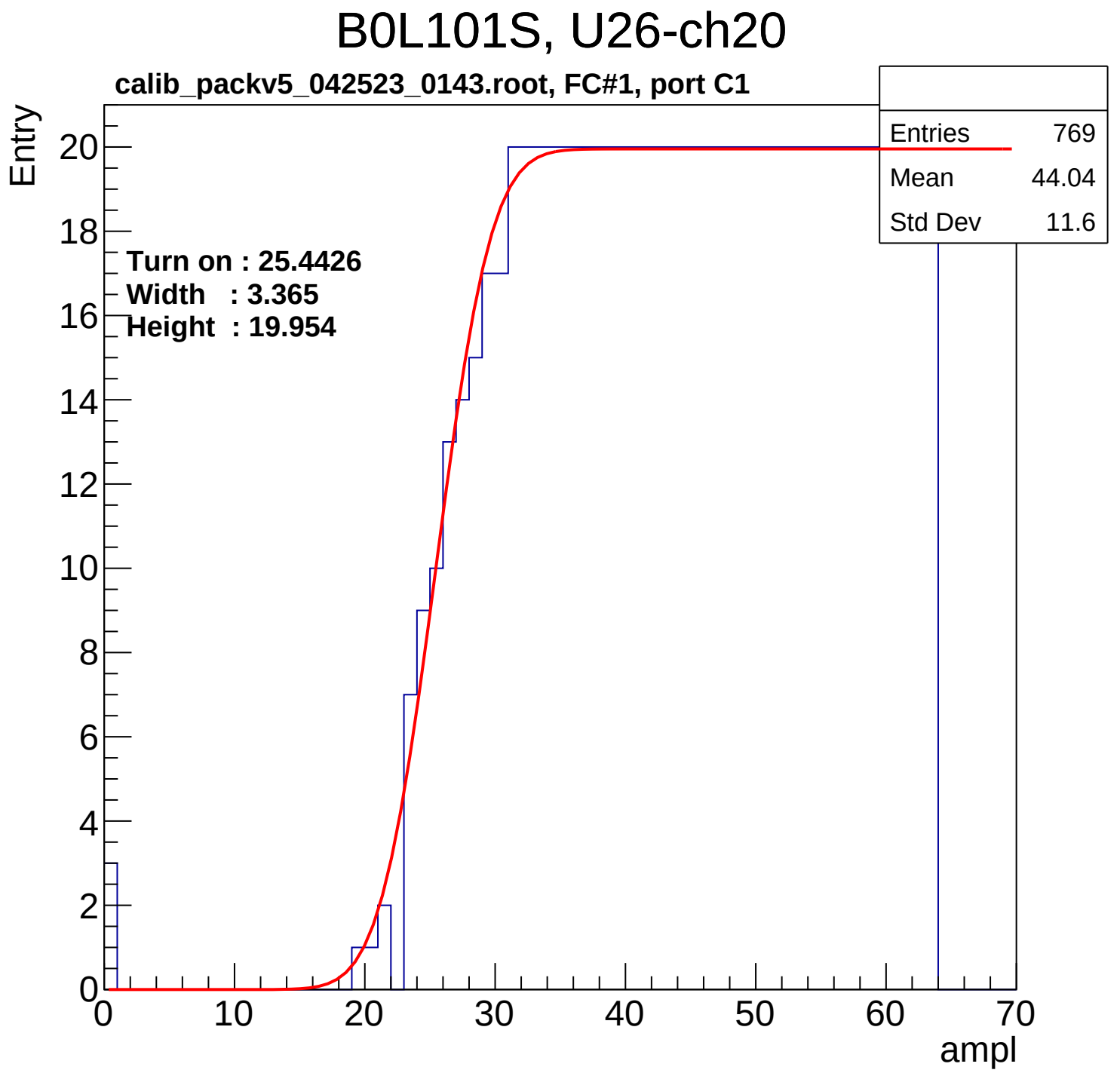
B0L101S, U26-ch20
calib_packv5_042523_0143.root, FC#1, port C1
Entries 769
Mean 44.04
Std Dev 11.6
Turn on : 25.4426
Width : 3.365
Height : 19.954
Entry
ampl
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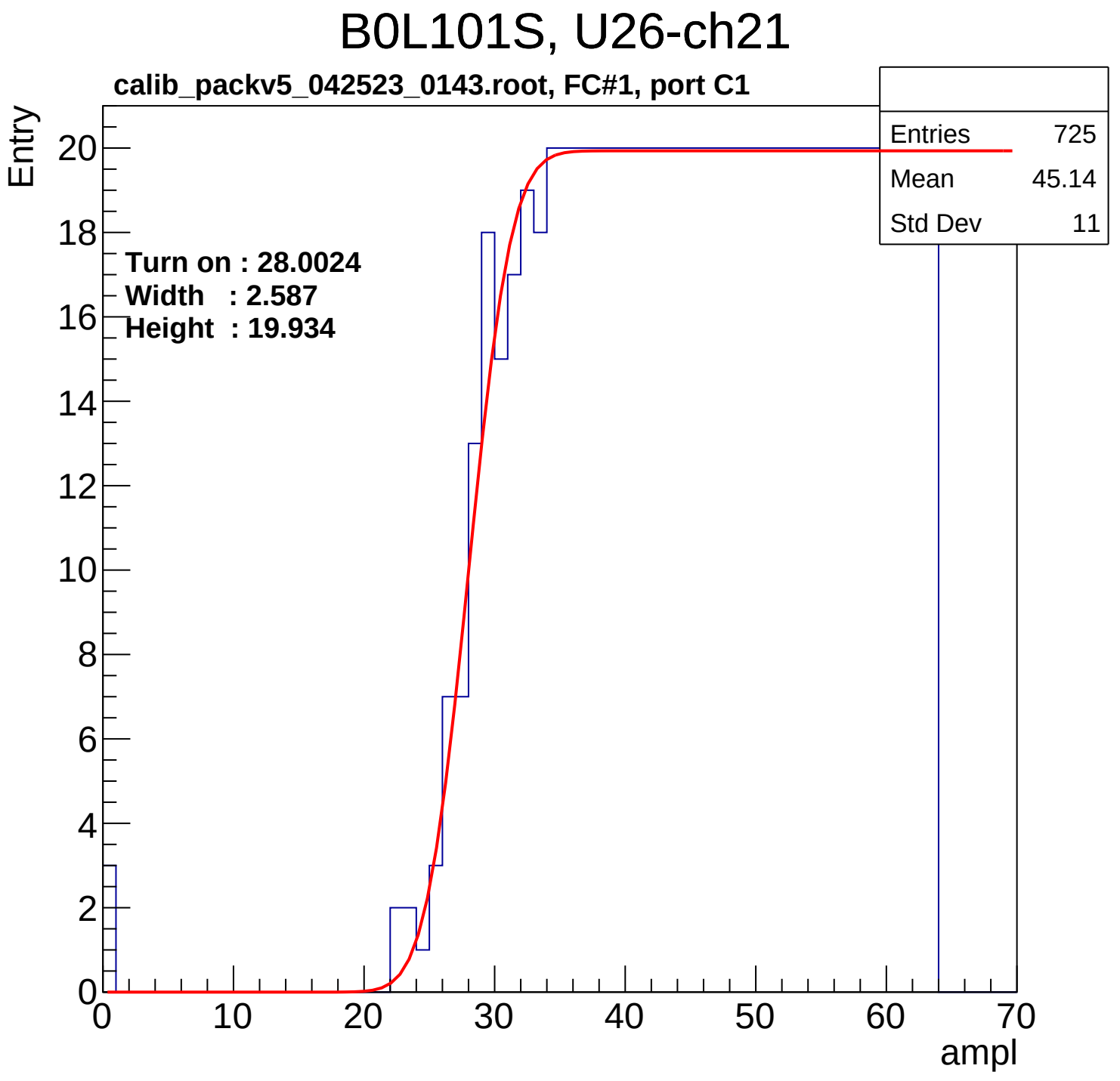
B0L101S, U26-ch21
calib_packv5_042523_0143.root, FC#1, port C1
Entries 725
Mean 45.14
Std Dev 11
Turn on : 28.0024
Width : 2.587
Height : 19.934
Entry
ampl
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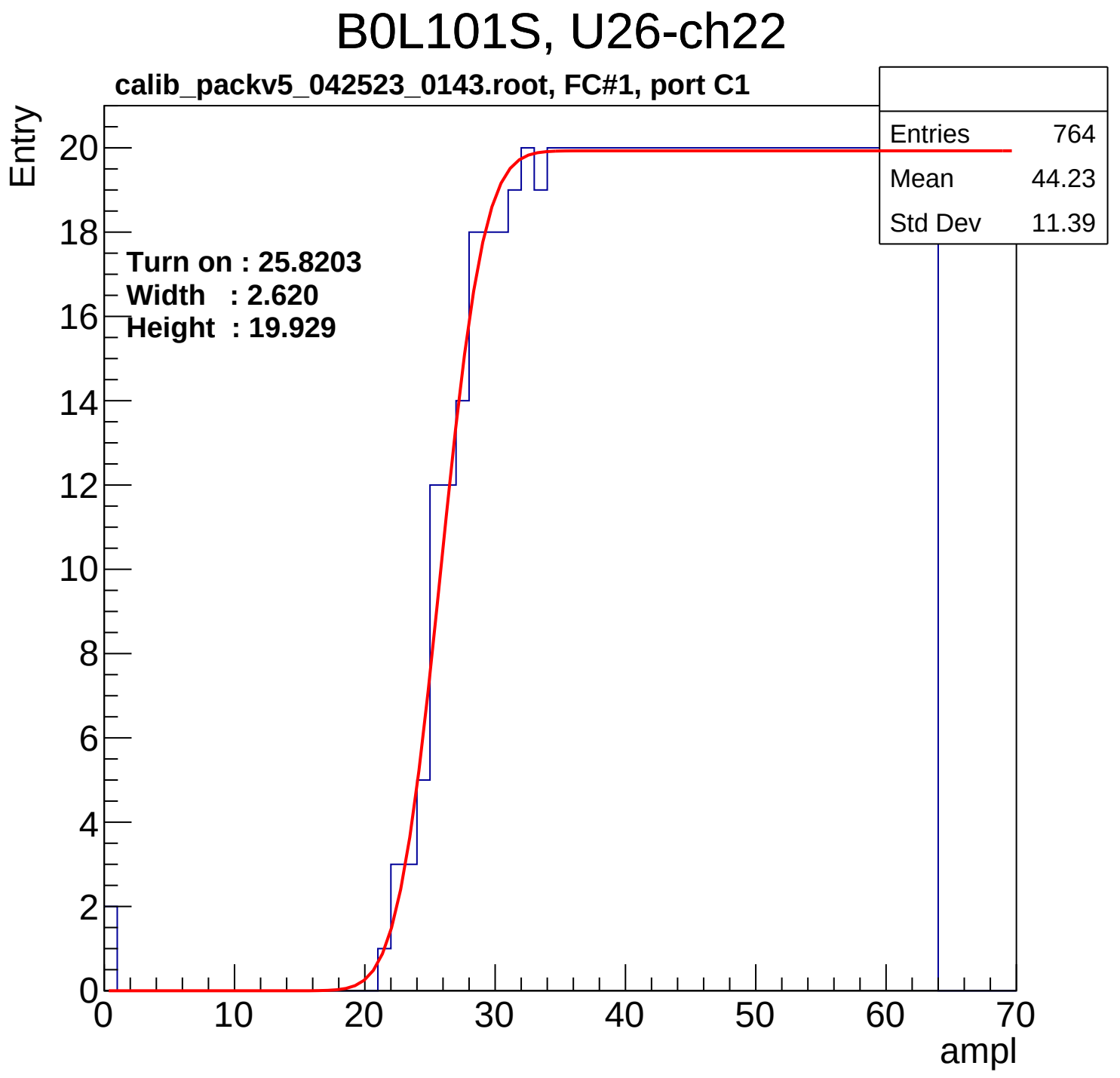
B0L101S, U26-ch22
calib_packv5_042523_0143.root, FC#1, port C1
Entries 764
Mean 44.23
Std Dev 11.39
Turn on : 25.8203
Width : 2.620
Height : 19.929
Entry
ampl
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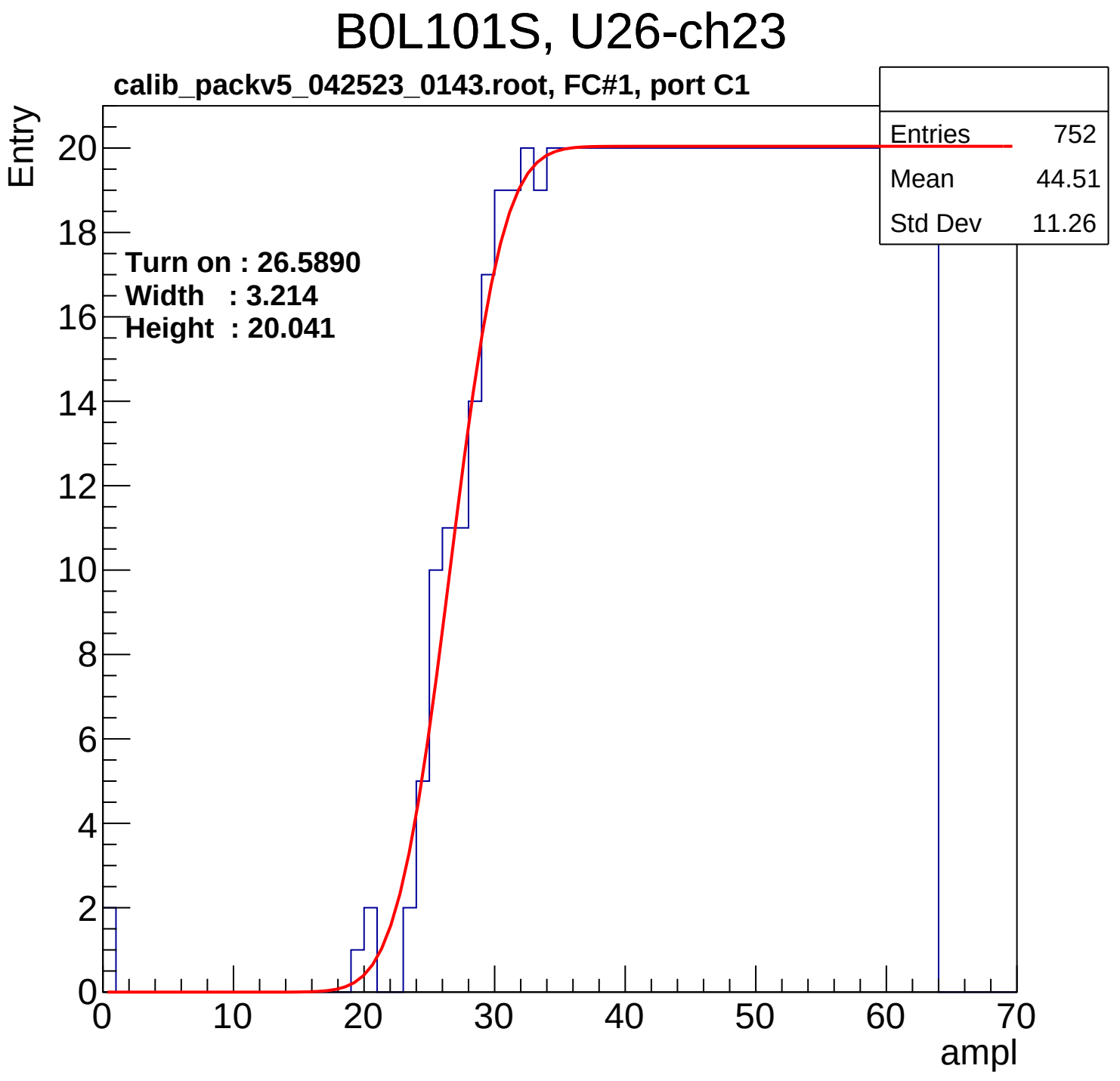
B0L101S, U26-ch23
calib_packv5_042523_0143.root, FC#1, port C1
Entries 752
Mean 44.51
Std Dev 11.26
Turn on : 26.5890
Width : 3.214
Height : 20.041
Entry
ampl
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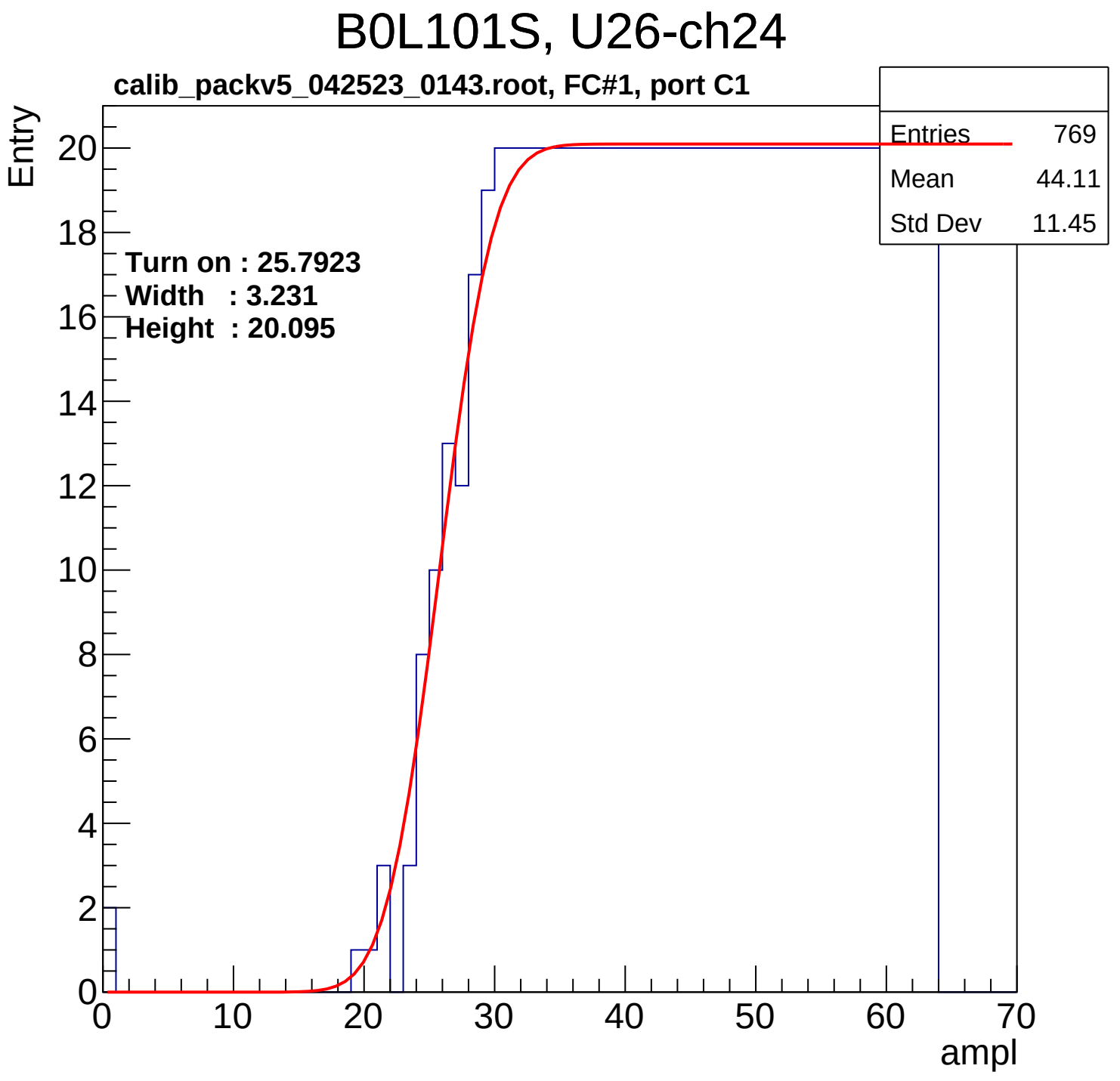
B0L101S, U26-ch24
calib_packv5_042523_0143.root, FC#1, port C1
Entries 769
Mean 44.11
Std Dev 11.45
Turn on : 25.7923
Width : 3.231
Height : 20.095
Entry
ampl
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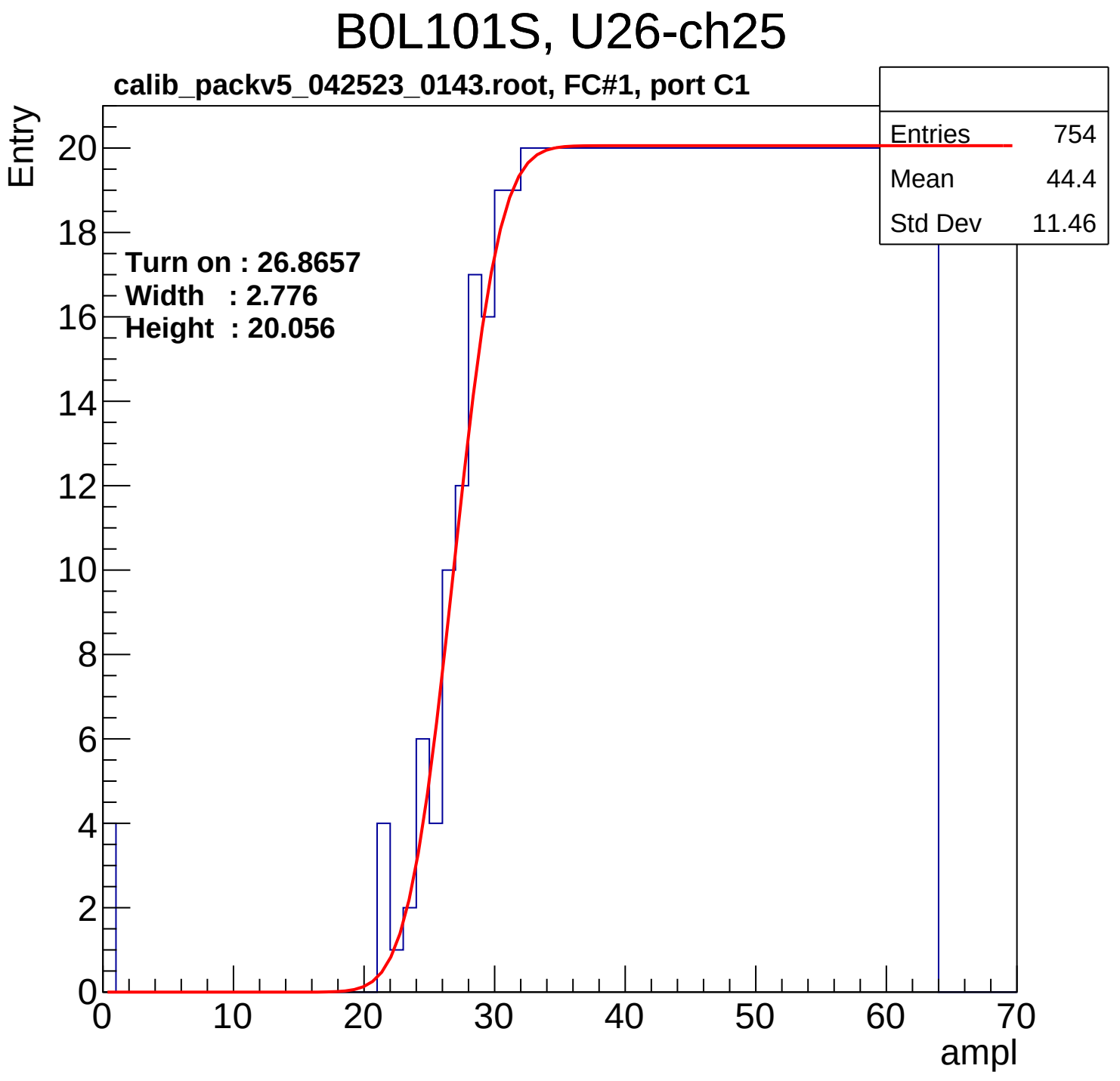
B0L101S, U26-ch25
calib_packv5_042523_0143.root, FC#1, port C1
Entries 754
Mean 44.4
Std Dev 11.46
Turn on : 26.8657
Width : 2.776
Height : 20.056
Entry
ampl
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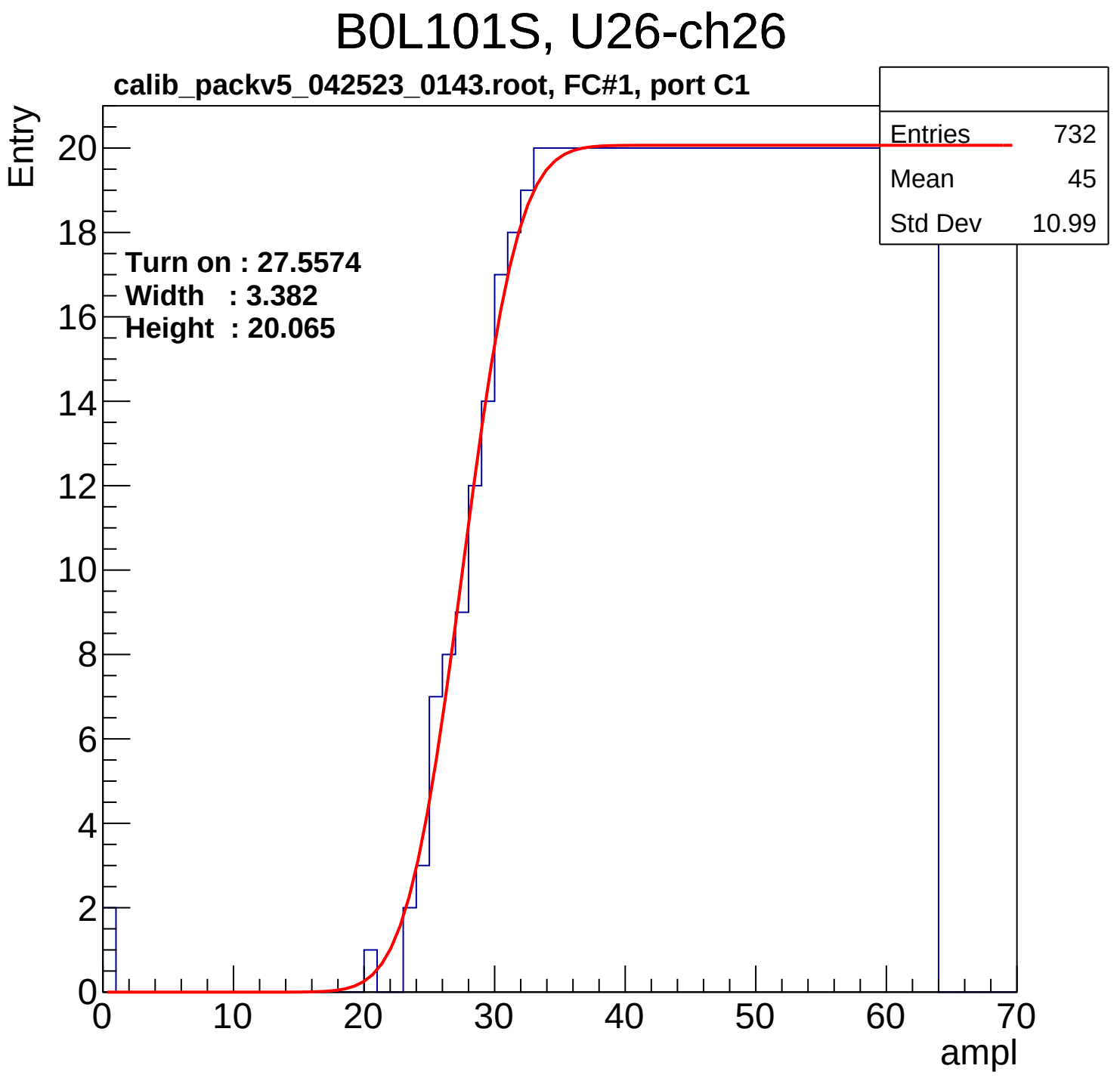
B0L101S, U26-ch26
calib_packv5_042523_0143.root, FC#1, port C1
Entries 732
Mean 45
Std Dev 10.99
Turn on : 27.5574
Width : 3.382
Height : 20.065
Entry
ampl
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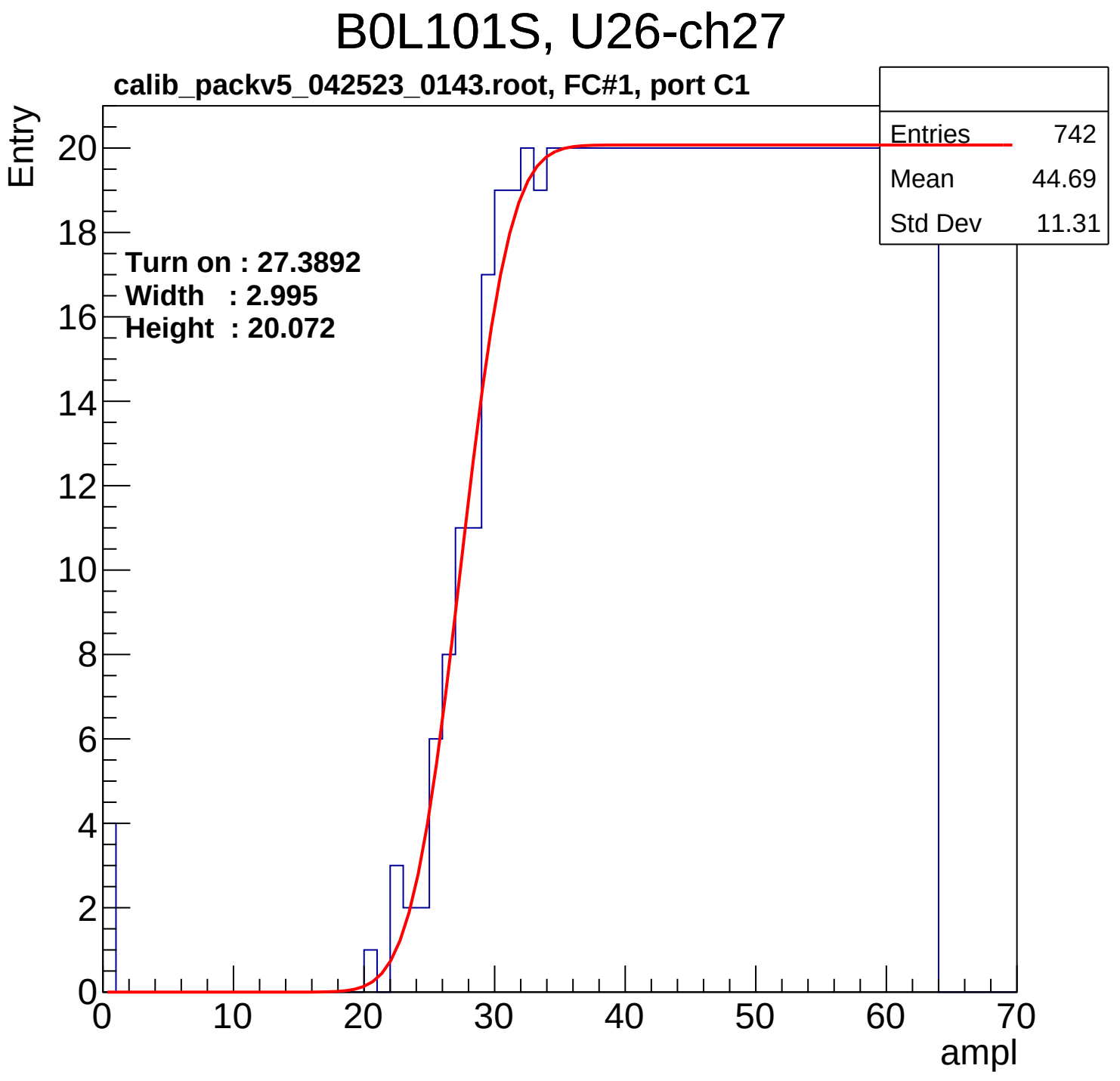
B0L101S, U26-ch27
calib_packv5_042523_0143.root, FC#1, port C1
Entries 742
Mean 44.69
Std Dev 11.31
Turn on : 27.3892
Width : 2.995
Height : 20.072
Entry
ampl
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2
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6
8
10
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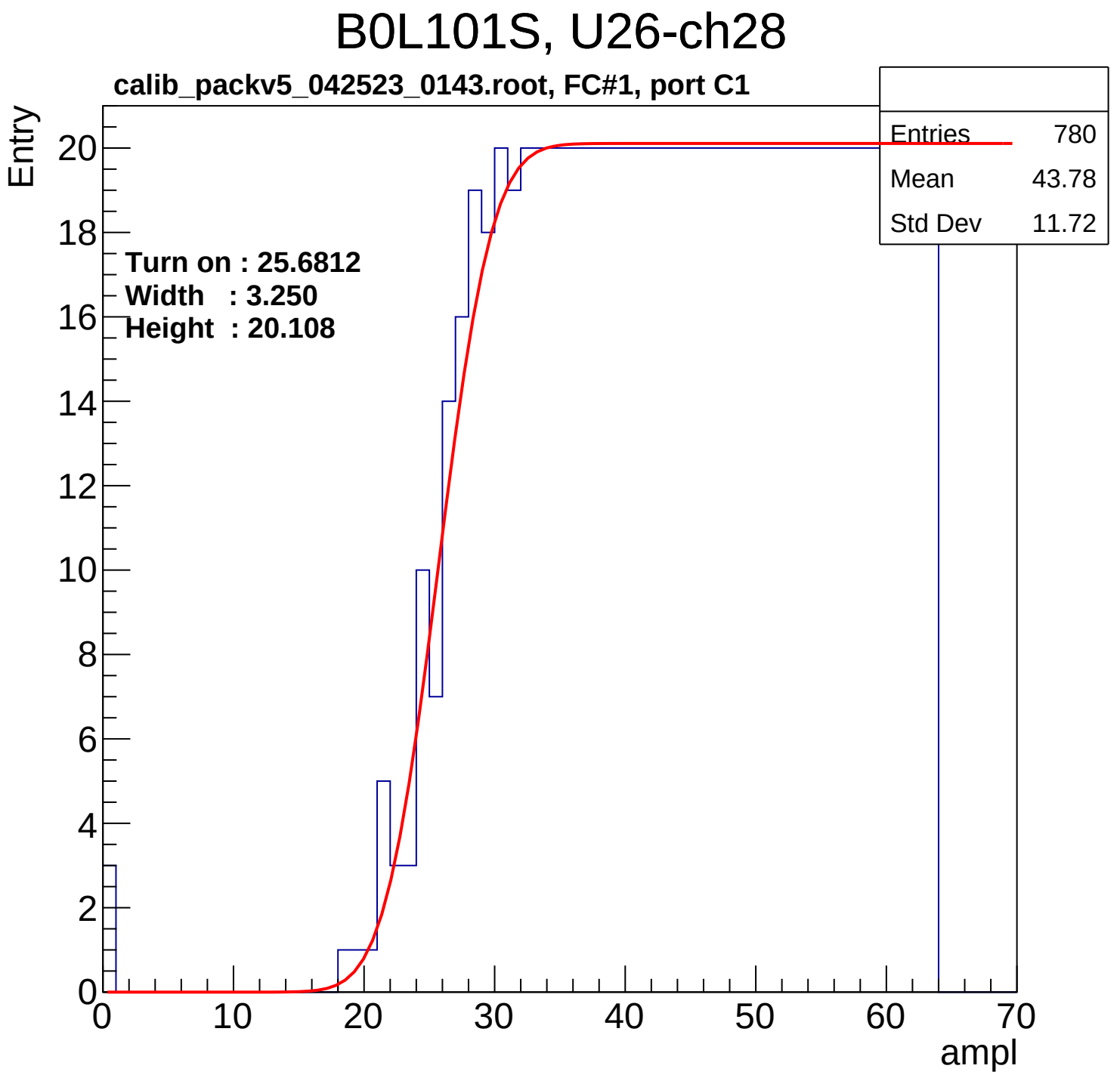
B0L101S, U26-ch28
calib_packv5_042523_0143.root, FC#1, port C1
Entries 780
Mean 43.78
Std Dev 11.72
Turn on : 25.6812
Width : 3.250
Height : 20.108
Entry
ampl
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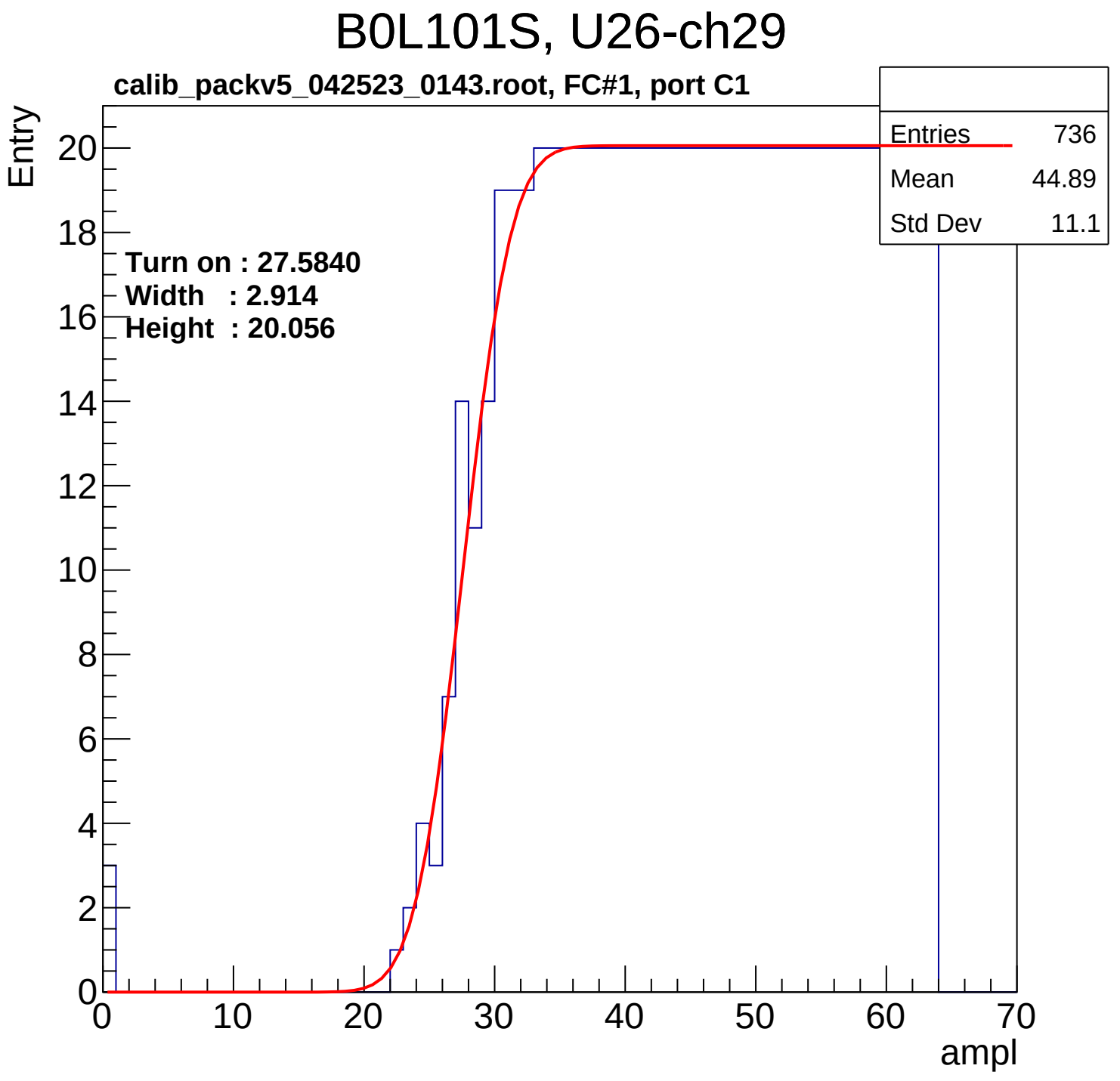
B0L101S, U26-ch29
calib_packv5_042523_0143.root, FC#1, port C1
Entries 736
Mean 44.89
Std Dev 11.1
Turn on : 27.5840
Width : 2.914
Height : 20.056
Entry
ampl
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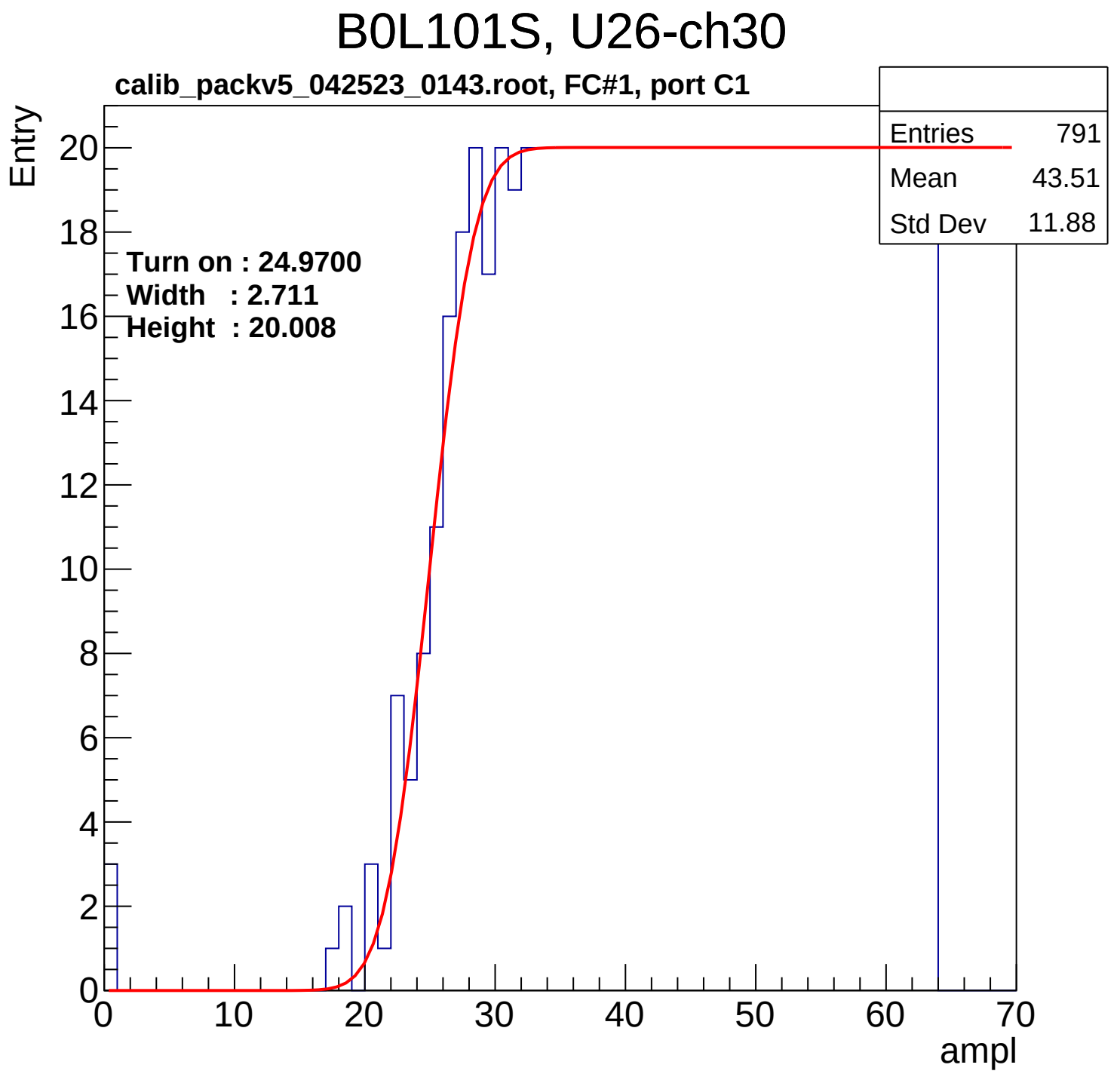
B0L101S, U26-ch30
calib_packv5_042523_0143.root, FC#1, port C1
Entries 791
Mean 43.51
Std Dev 11.88
Turn on : 24.9700
Width : 2.711
Height : 20.008
Entry
ampl
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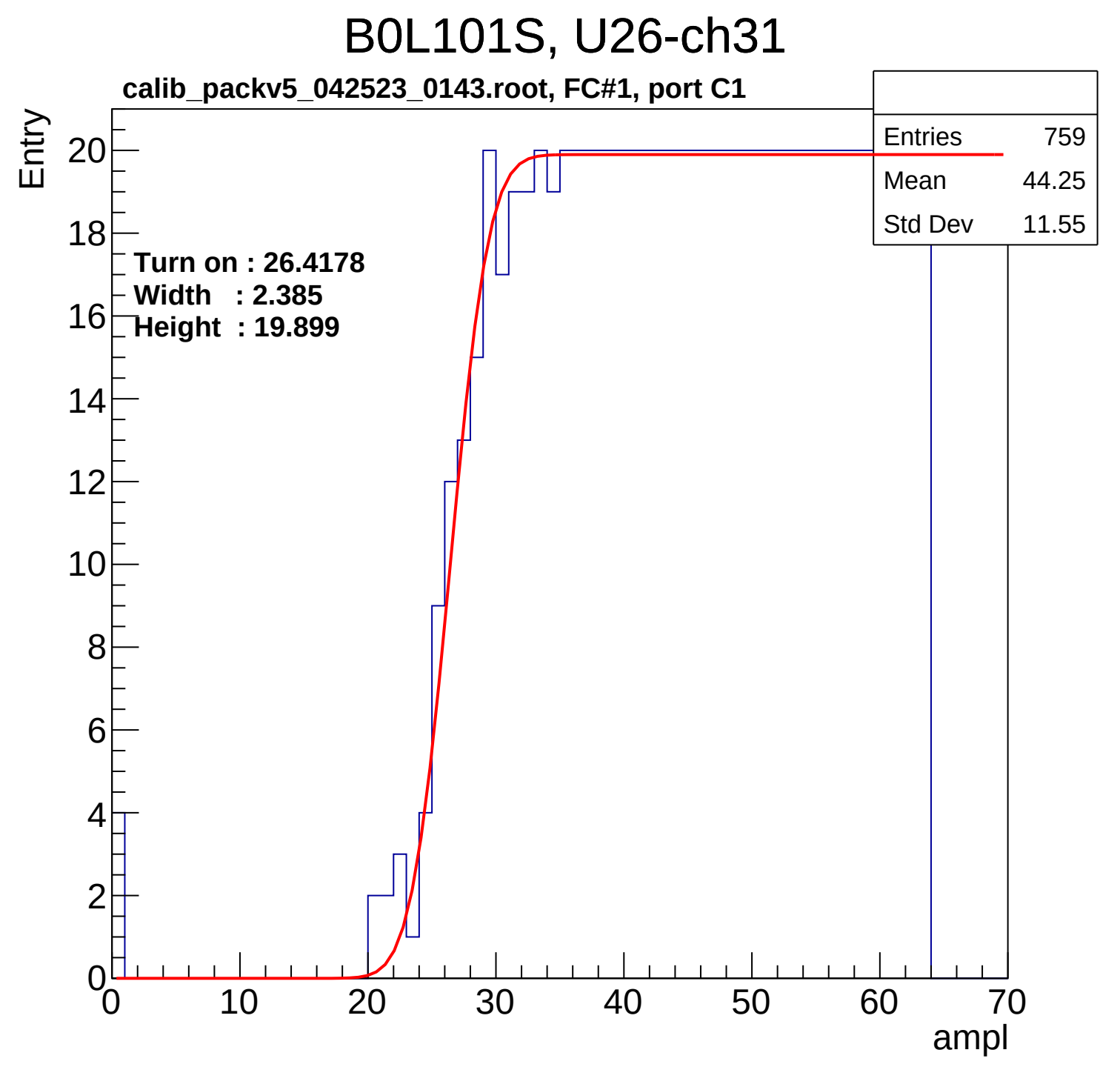
B0L101S, U26-ch31
calib_packv5_042523_0143.root, FC#1, port C1
Entries 759
Mean 44.25
Std Dev 11.55
Turn on : 26.4178
Width : 2.385
Height : 19.899
Entry
ampl
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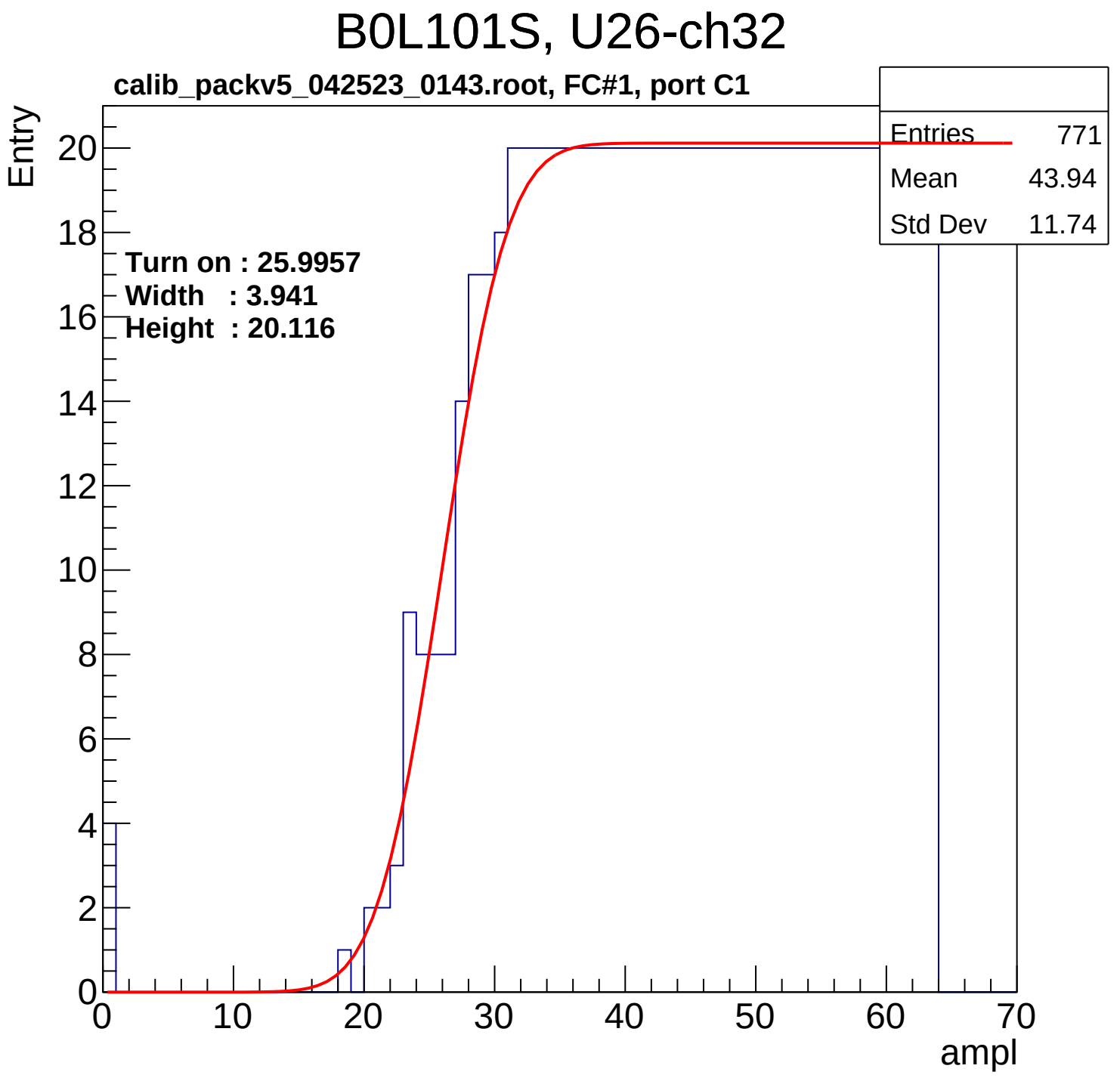
B0L101S, U26-ch32
calib_packv5_042523_0143.root, FC#1, port C1
Entries 771
Mean 43.94
Std Dev 11.74
Turn on : 25.9957
Width : 3.941
Height : 20.116
Entry
ampl
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6
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14
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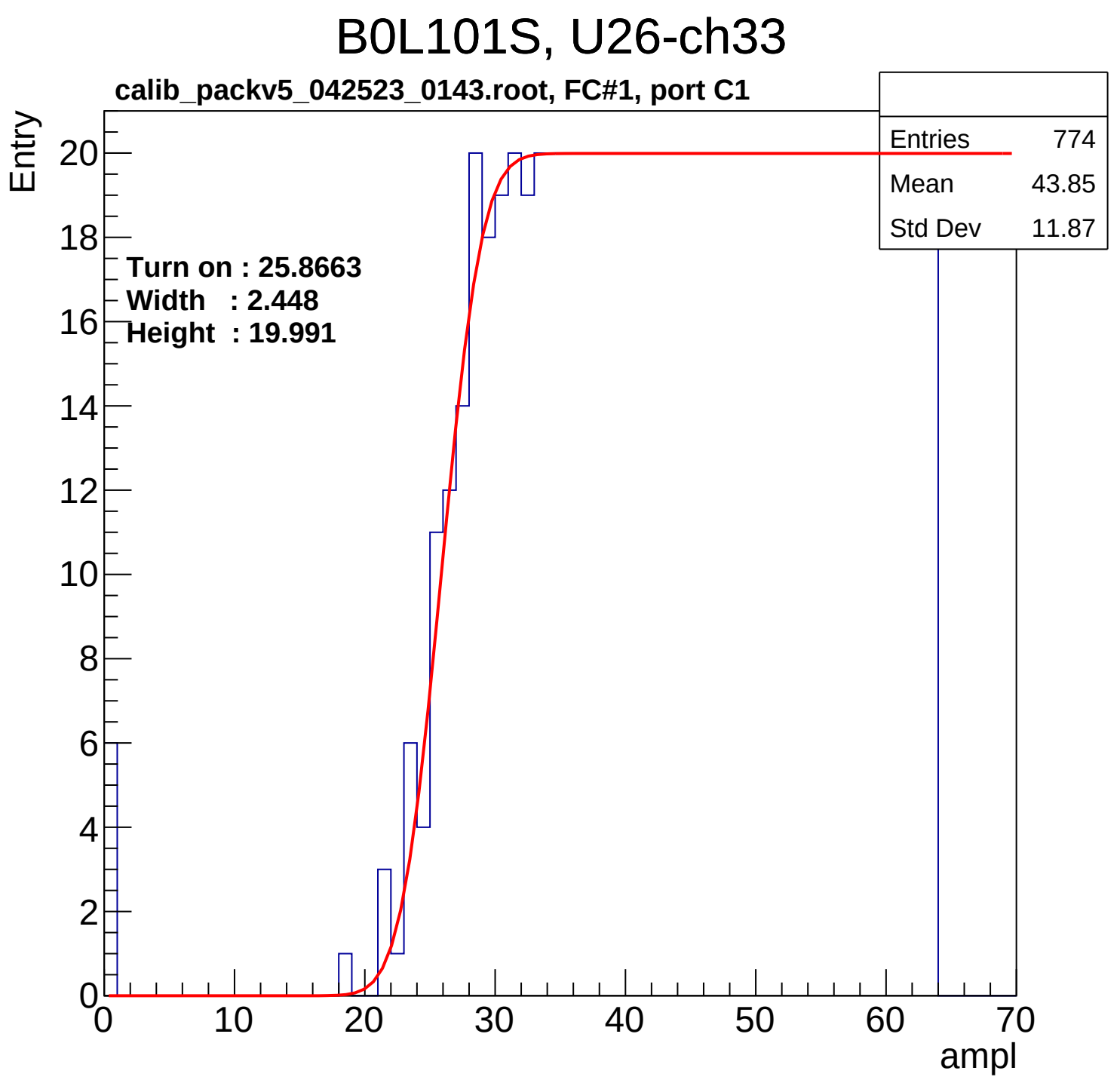
B0L101S, U26-ch33
calib_packv5_042523_0143.root, FC#1, port C1
Entries 774
Mean 43.85
Std Dev 11.87
Turn on : 25.8663
Width : 2.448
Height : 19.991
Entry
ampl
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6
8
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12
14
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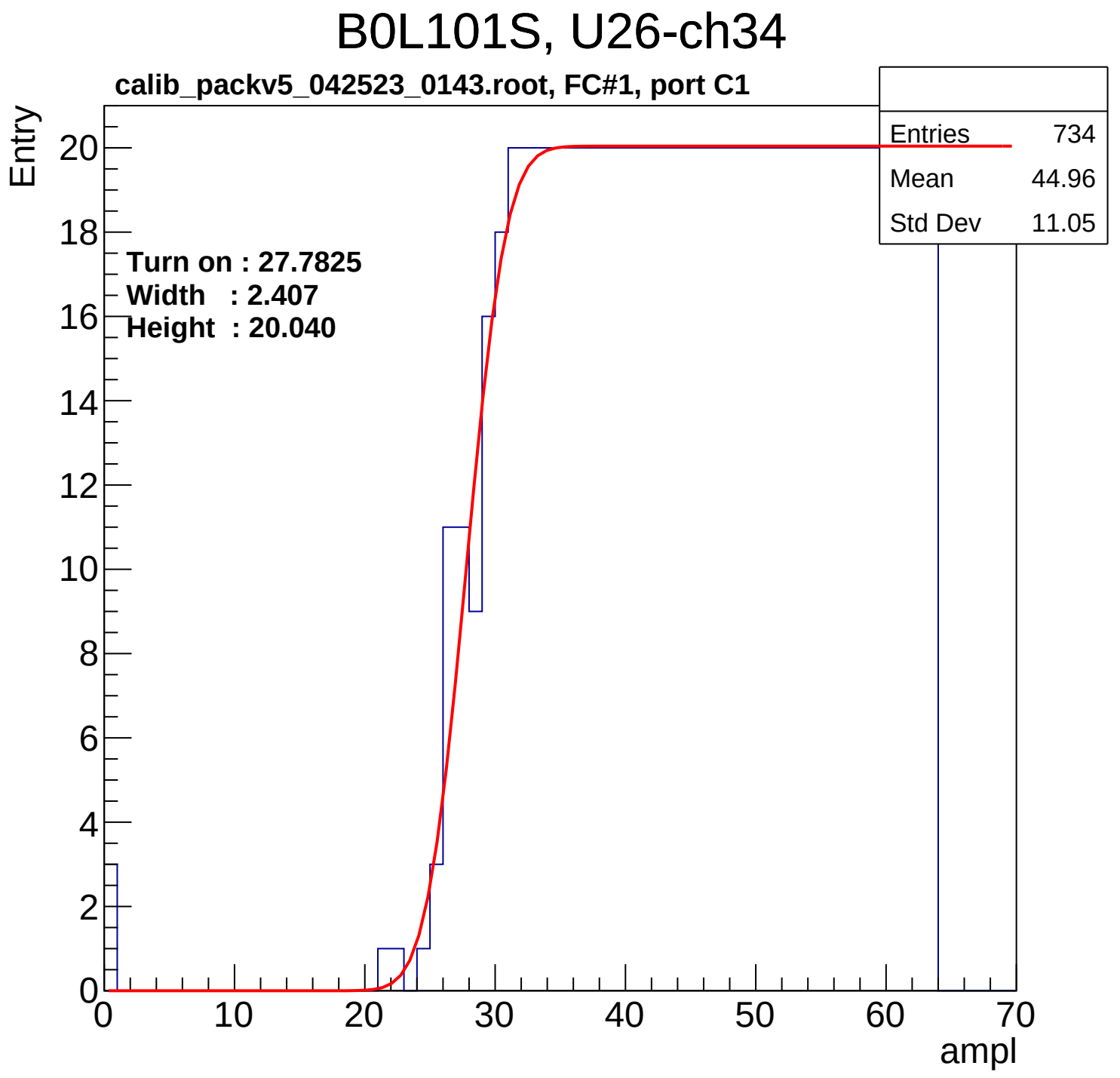
B0L101S, U26-ch34
calib_packv5_042523_0143.root, FC#1, port C1
Entries 734
Mean 44.96
Std Dev 11.05
Turn on : 27.7825
Width : 2.407
Height : 20.040
Entry
ampl
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6
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14
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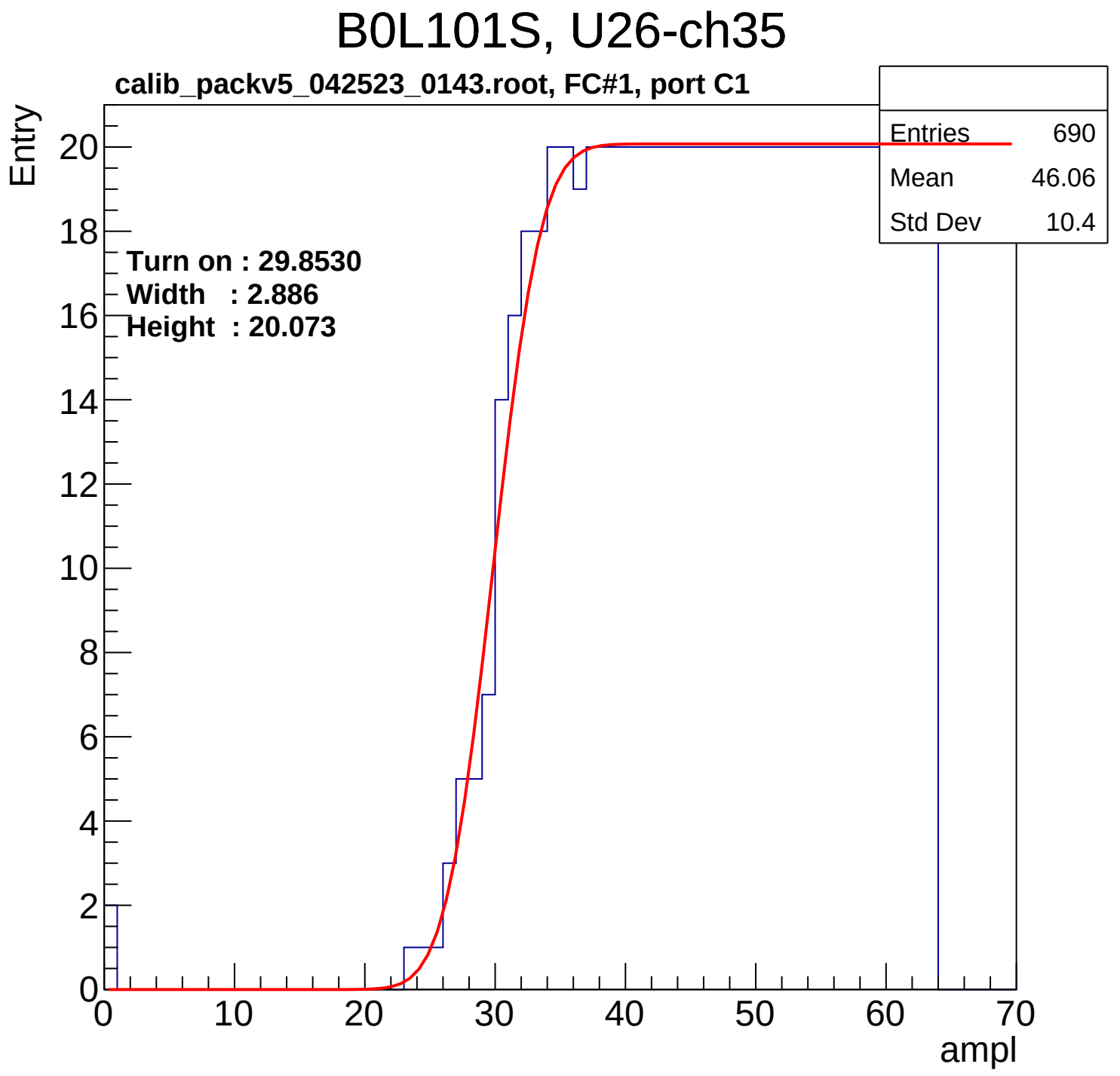
B0L101S, U26-ch35
calib_packv5_042523_0143.root, FC#1, port C1
Entries 690
Mean 46.06
Std Dev 10.4
Turn on : 29.8530
Width : 2.886
Height : 20.073
Entry
ampl
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6
8
10
12
14
16
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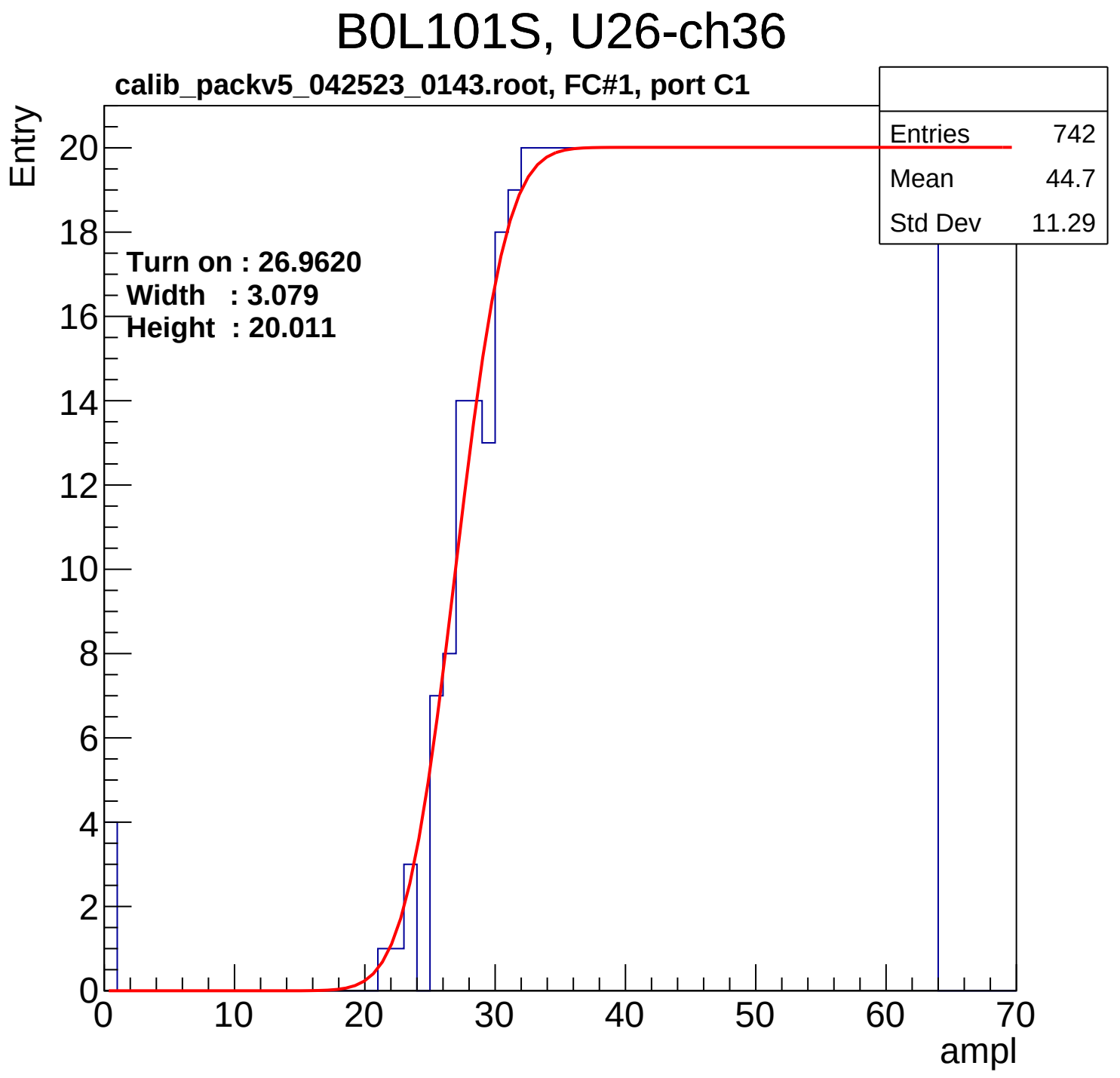
B0L101S, U26-ch36
calib_packv5_042523_0143.root, FC#1, port C1
Entries 742
Mean 44.7
Std Dev 11.29
Turn on : 26.9620
Width : 3.079
Height : 20.011
Entry
ampl
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6
8
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12
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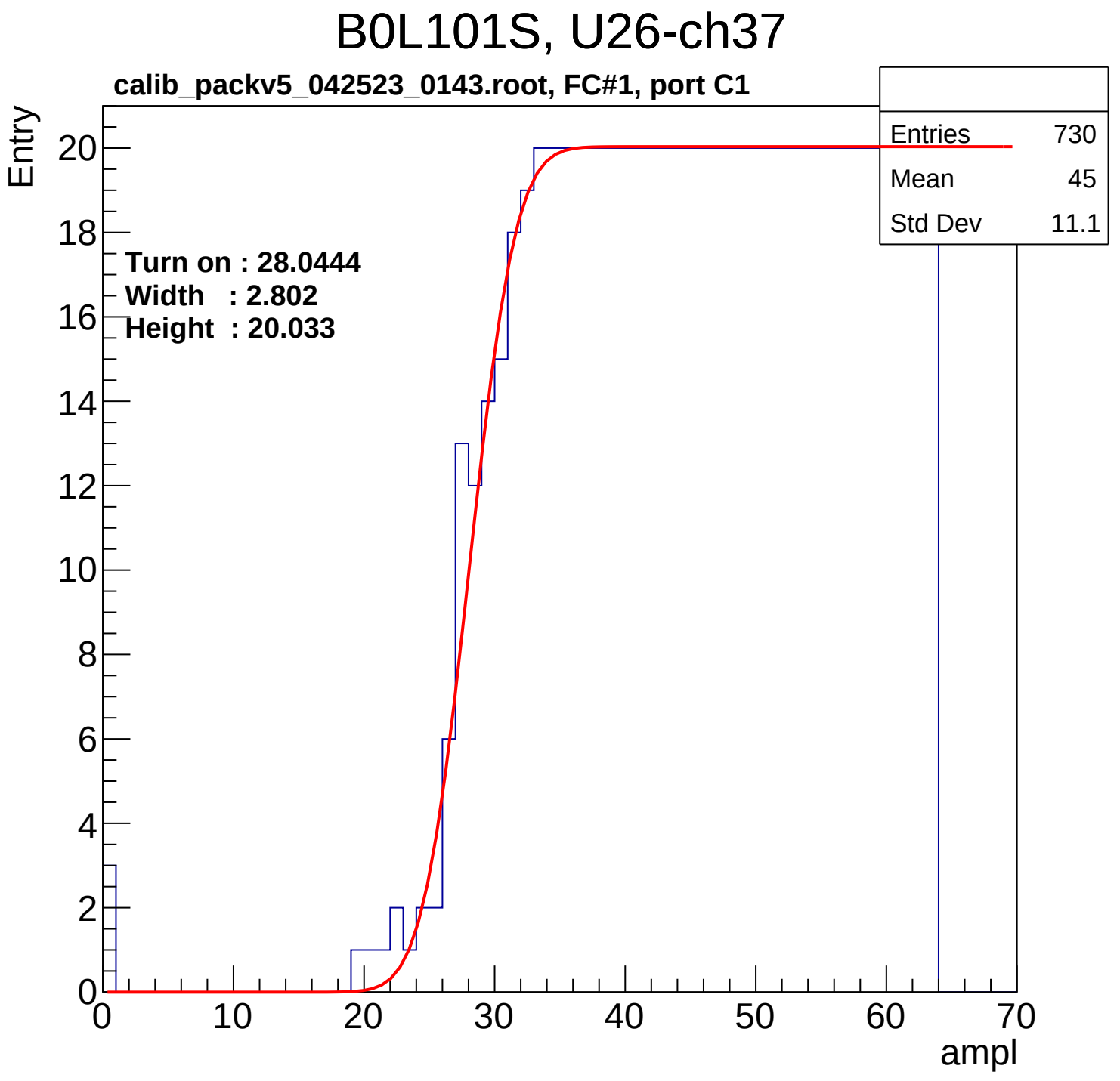
B0L101S, U26-ch37
calib_packv5_042523_0143.root, FC#1, port C1
Entries 730
Mean 45
Std Dev 11.1
Turn on : 28.0444
Width : 2.802
Height : 20.033
Entry
ampl
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6
8
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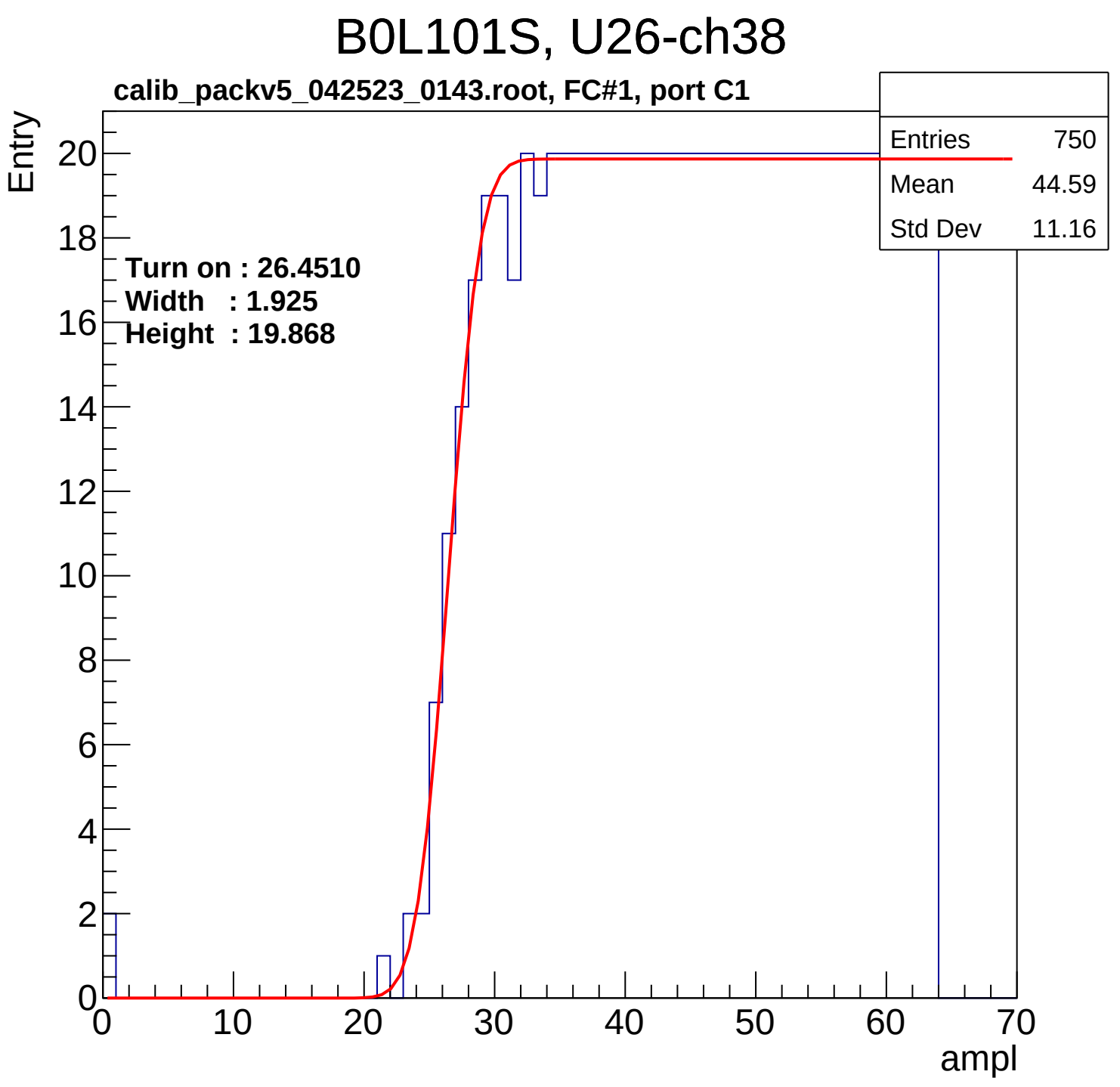
B0L101S, U26-ch38
calib_packv5_042523_0143.root, FC#1, port C1
Entries 750
Mean 44.59
Std Dev 11.16
Turn on : 26.4510
Width : 1.925
Height : 19.868
Entry
ampl
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6
8
10
12
14
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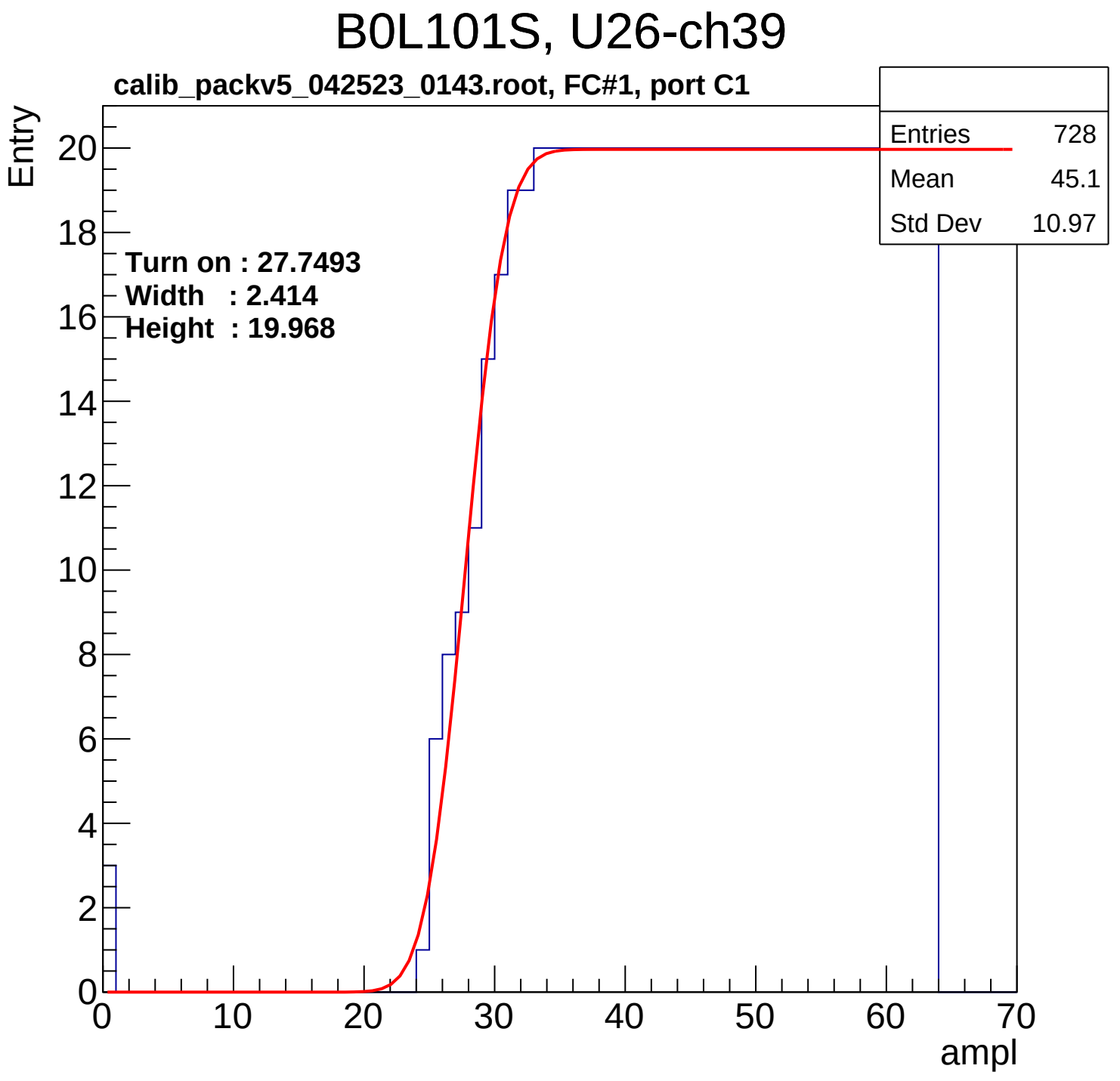
B0L101S, U26-ch39
calib_packv5_042523_0143.root, FC#1, port C1
Entries 728
Mean 45.1
Std Dev 10.97
Turn on : 27.7493
Width : 2.414
Height : 19.968
Entry
ampl
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6
8
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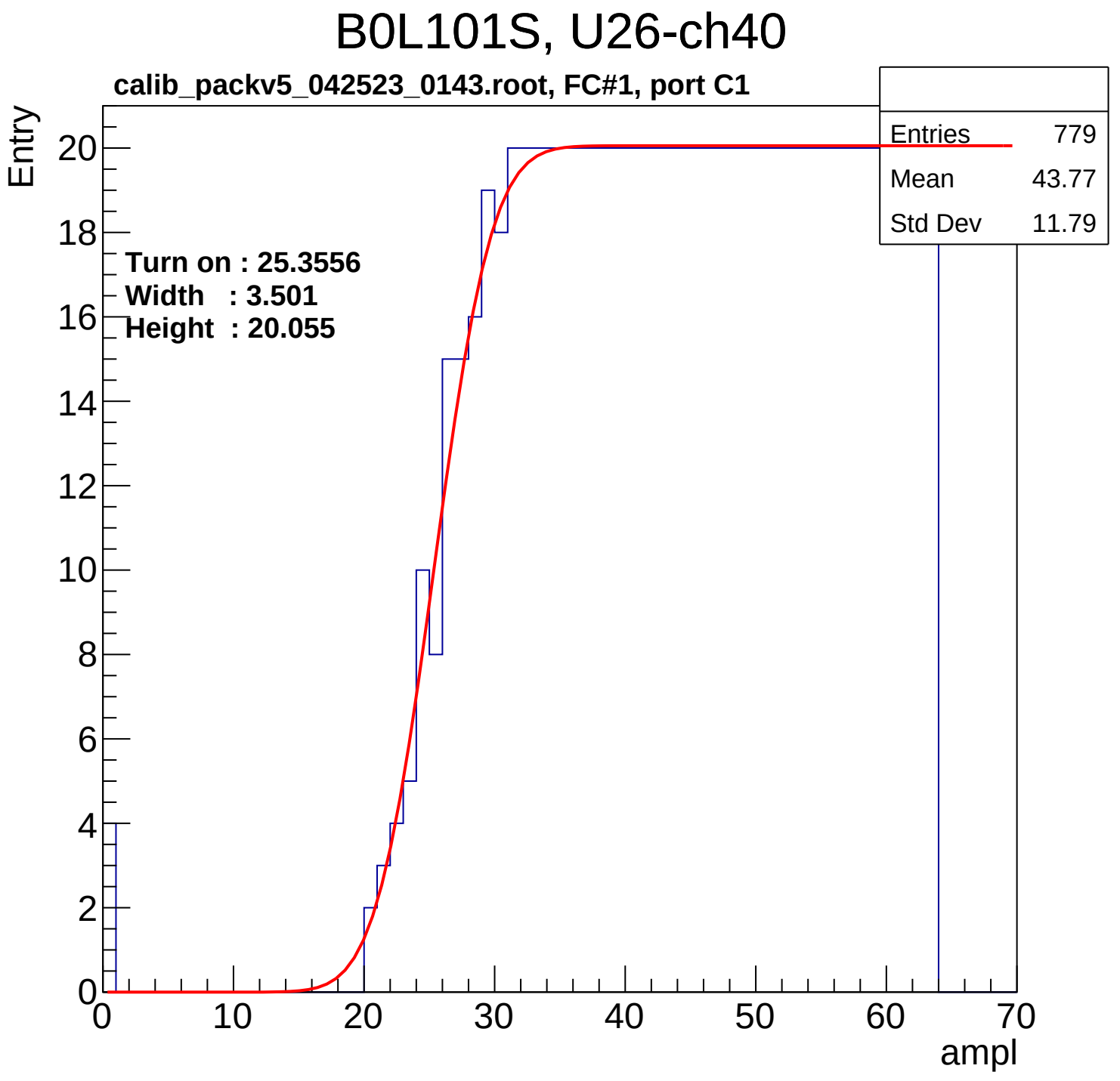
B0L101S, U26-ch40
calib_packv5_042523_0143.root, FC#1, port C1
Entries 779
Mean 43.77
Std Dev 11.79
Turn on : 25.3556
Width : 3.501
Height : 20.055
Entry
ampl
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6
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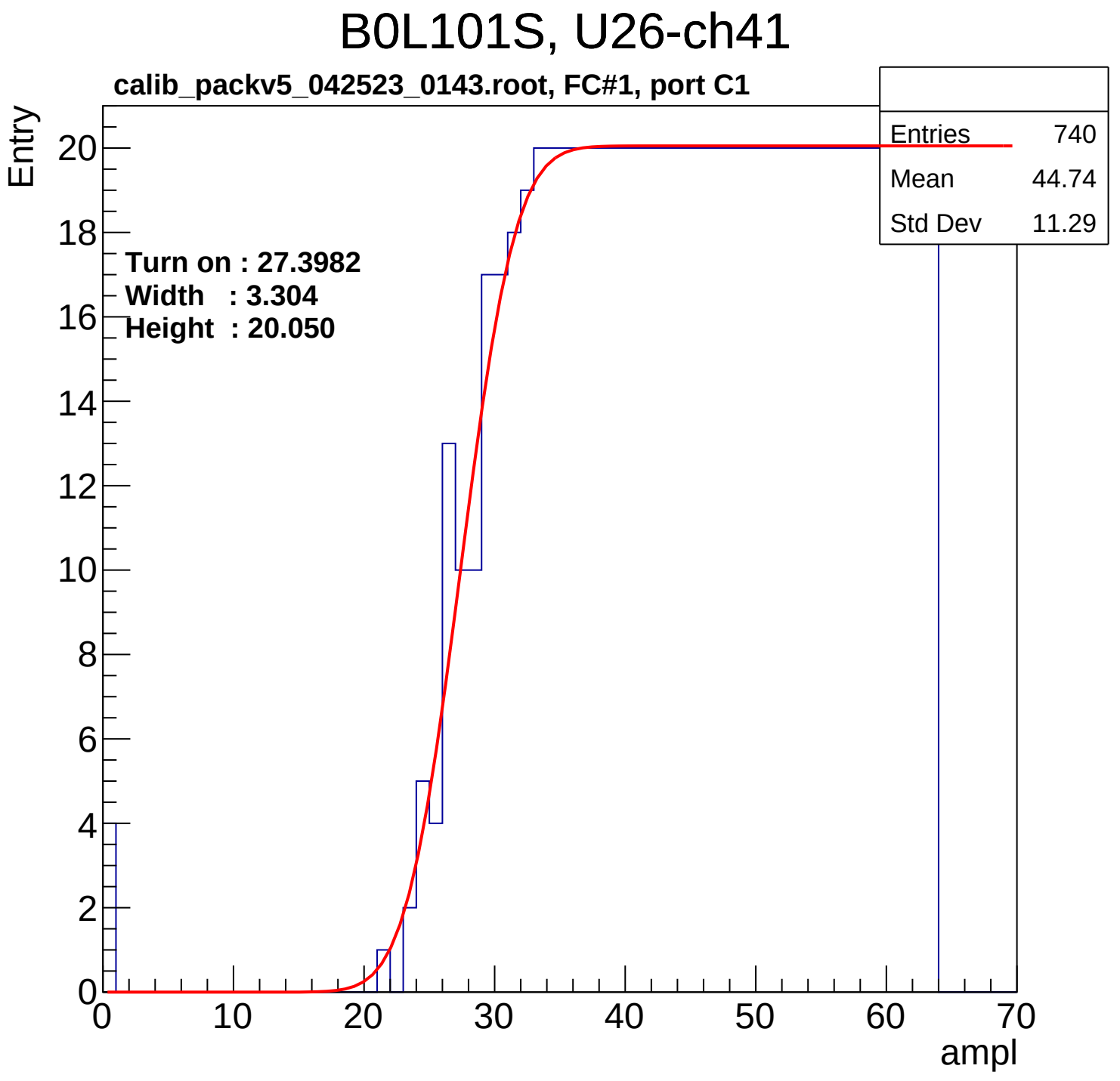
B0L101S, U26-ch41
calib_packv5_042523_0143.root, FC#1, port C1
Entries 740
Mean 44.74
Std Dev 11.29
Turn on : 27.3982
Width : 3.304
Height : 20.050
Entry
ampl
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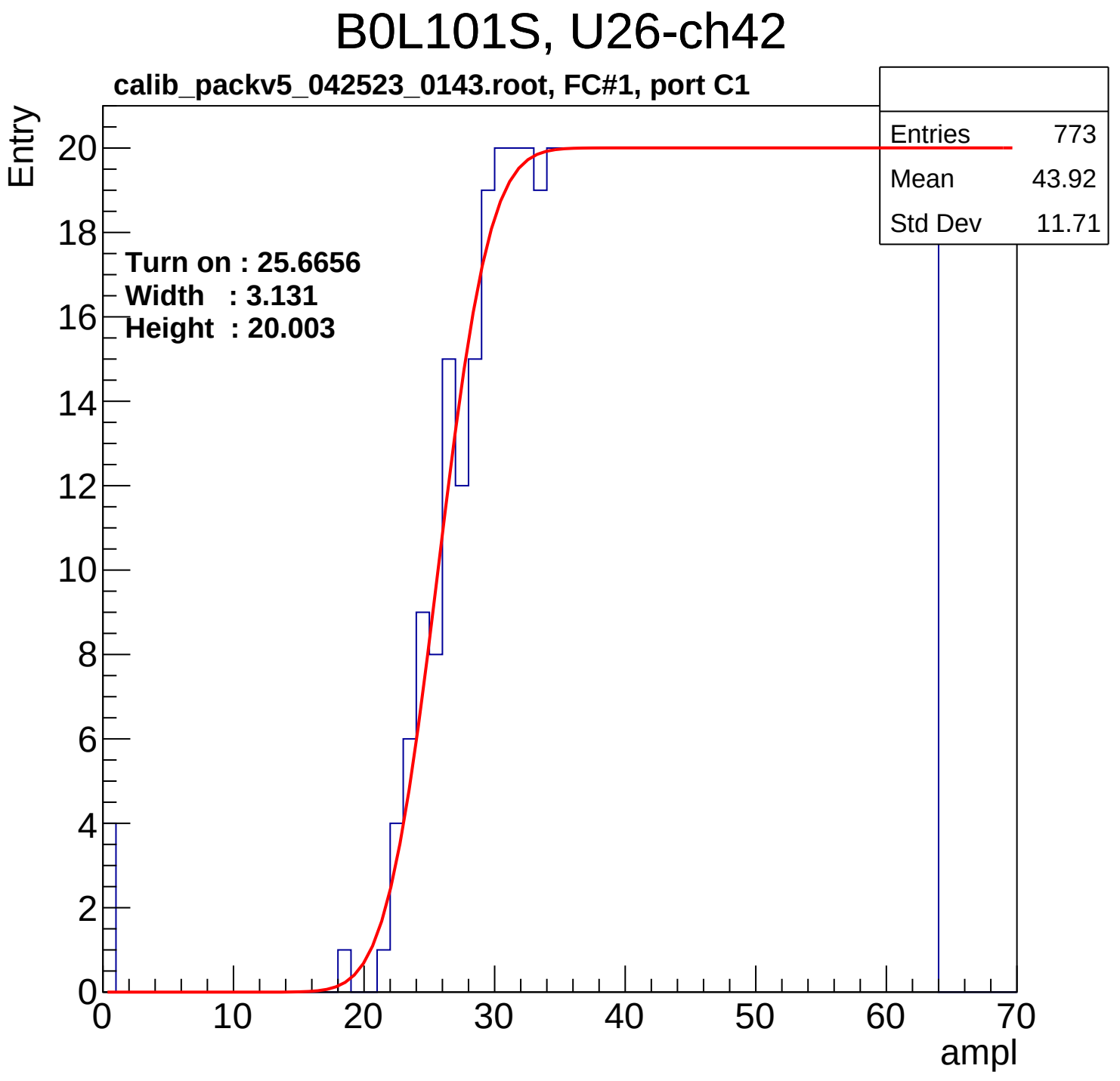
B0L101S, U26-ch42
calib_packv5_042523_0143.root, FC#1, port C1
Entries 773
Mean 43.92
Std Dev 11.71
Turn on : 25.6656
Width : 3.131
Height : 20.003
Entry
ampl
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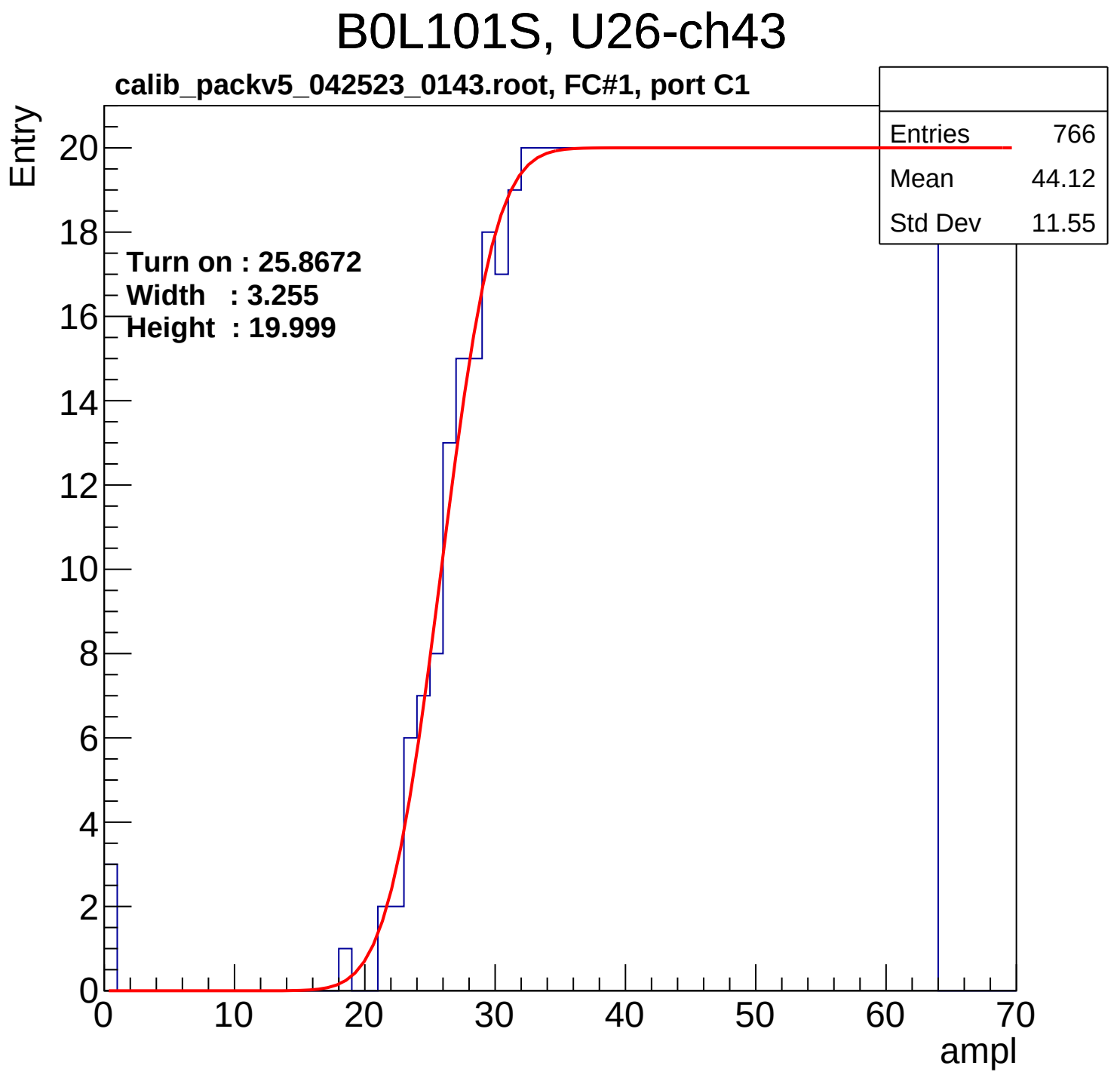
B0L101S, U26-ch43
calib_packv5_042523_0143.root, FC#1, port C1
Entries 766
Mean 44.12
Std Dev 11.55
Turn on : 25.8672
Width : 3.255
Height : 19.999
Entry
ampl
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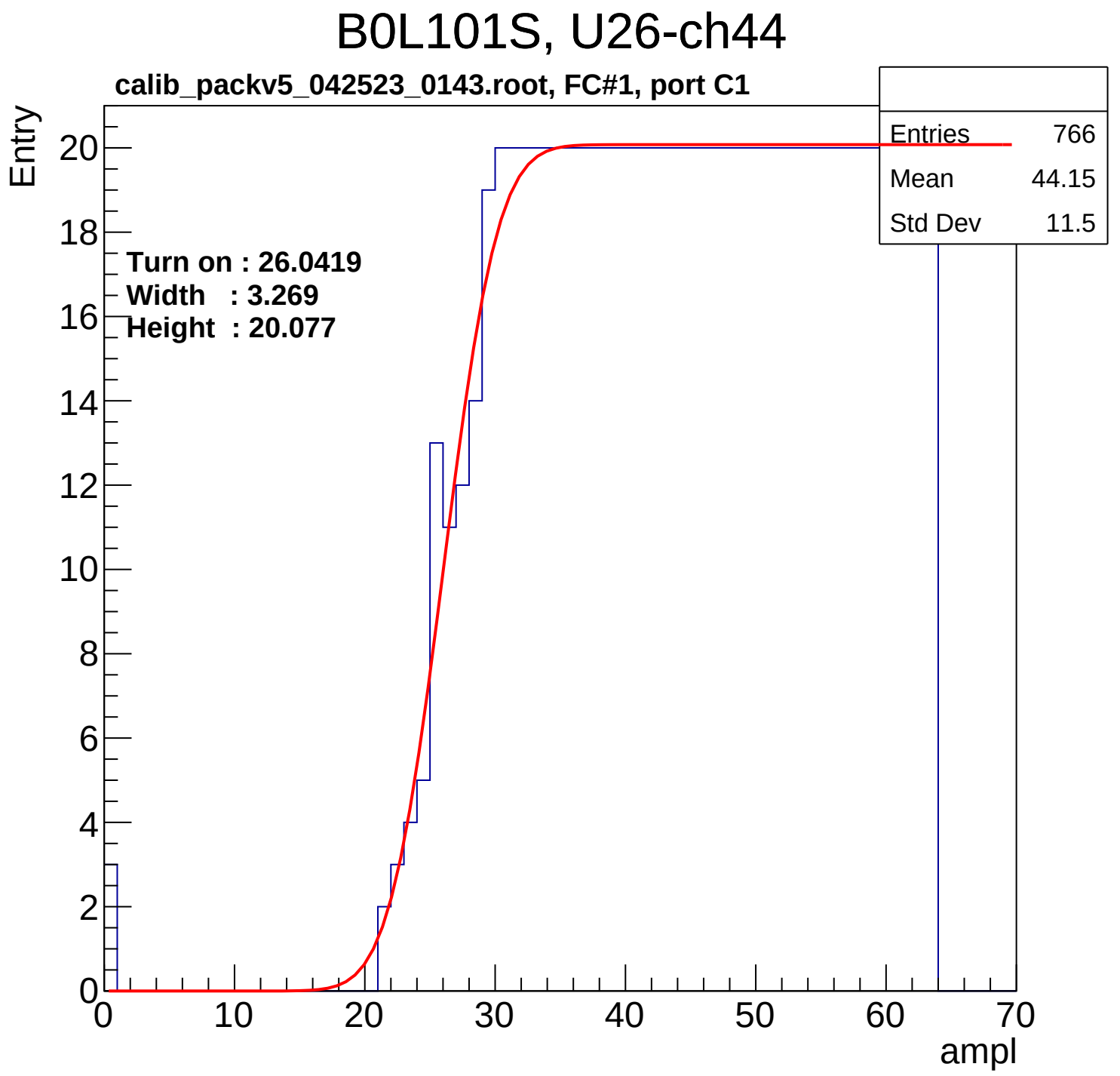
B0L101S, U26-ch44
calib_packv5_042523_0143.root, FC#1, port C1
Entries 766
Mean 44.15
Std Dev 11.5
Turn on : 26.0419
Width : 3.269
Height : 20.077
Entry
ampl
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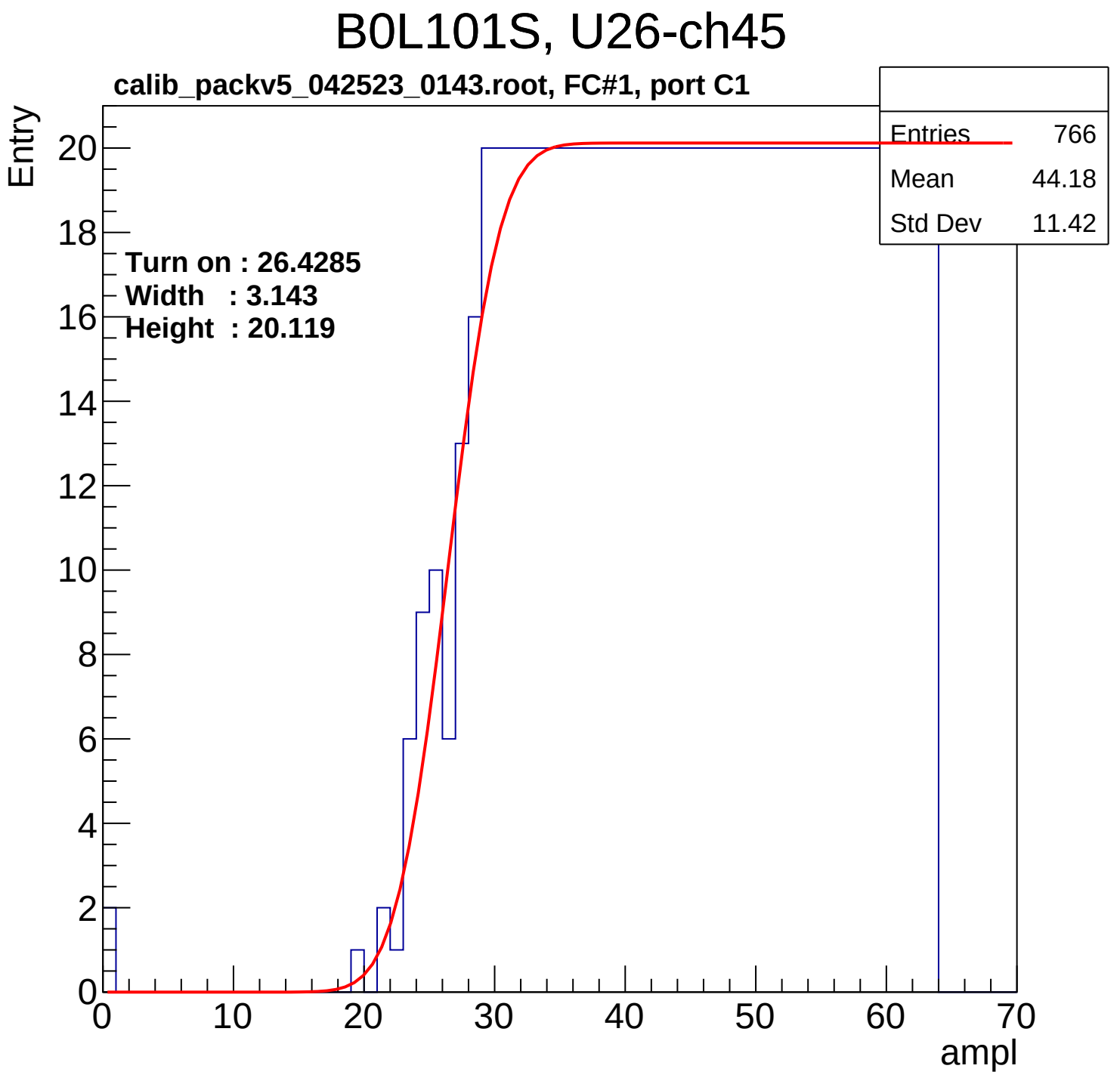
B0L101S, U26-ch45
calib_packv5_042523_0143.root, FC#1, port C1
Entries 766
Mean 44.18
Std Dev 11.42
Turn on : 26.4285
Width : 3.143
Height : 20.119
Entry
ampl
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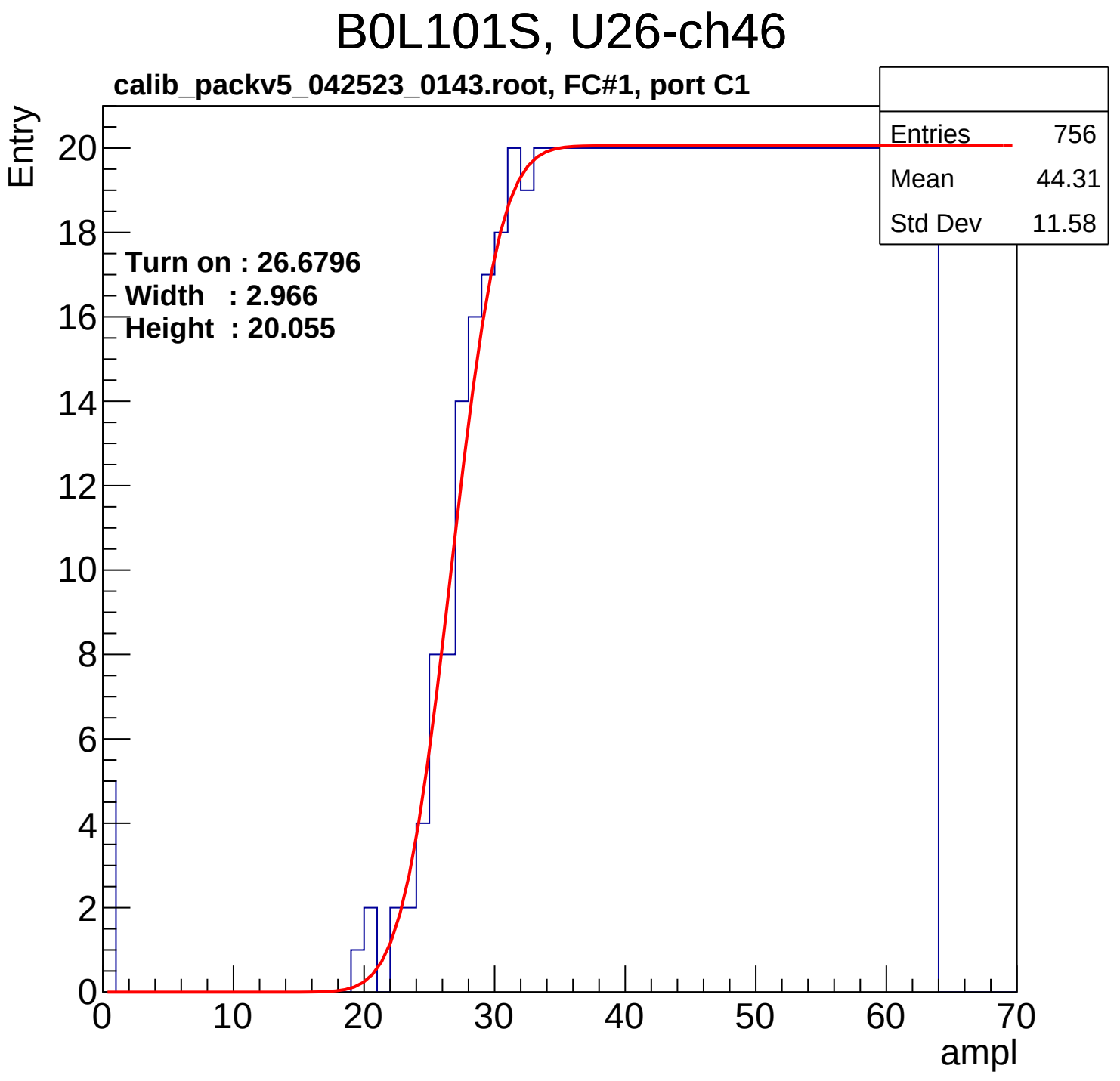
B0L101S, U26-ch46
calib_packv5_042523_0143.root, FC#1, port C1
Entries 756
Mean 44.31
Std Dev 11.58
Turn on : 26.6796
Width : 2.966
Height : 20.055
Entry
ampl
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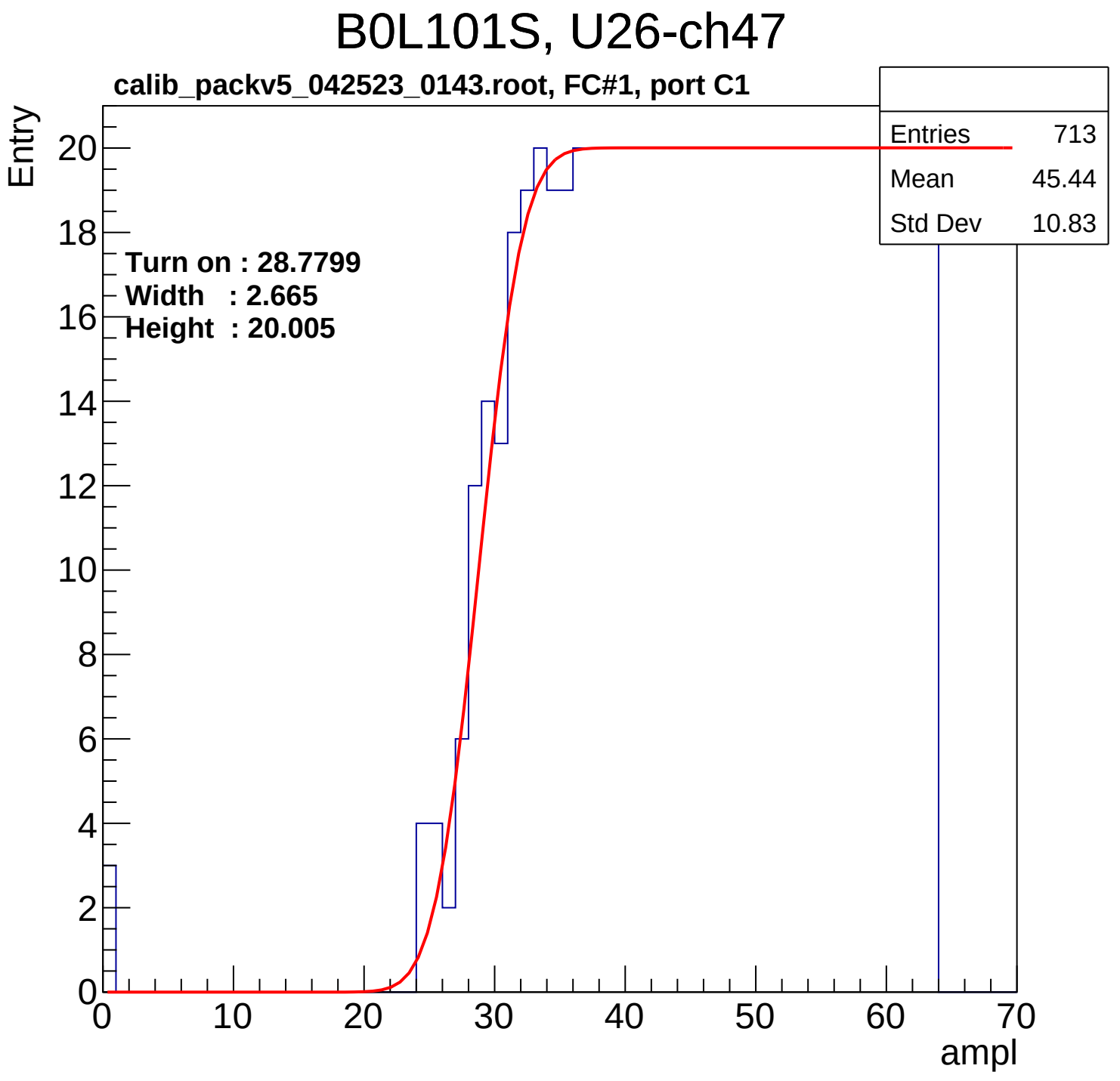
B0L101S, U26-ch47
calib_packv5_042523_0143.root, FC#1, port C1
Entries 713
Mean 45.44
Std Dev 10.83
Turn on : 28.7799
Width : 2.665
Height : 20.005
Entry
ampl
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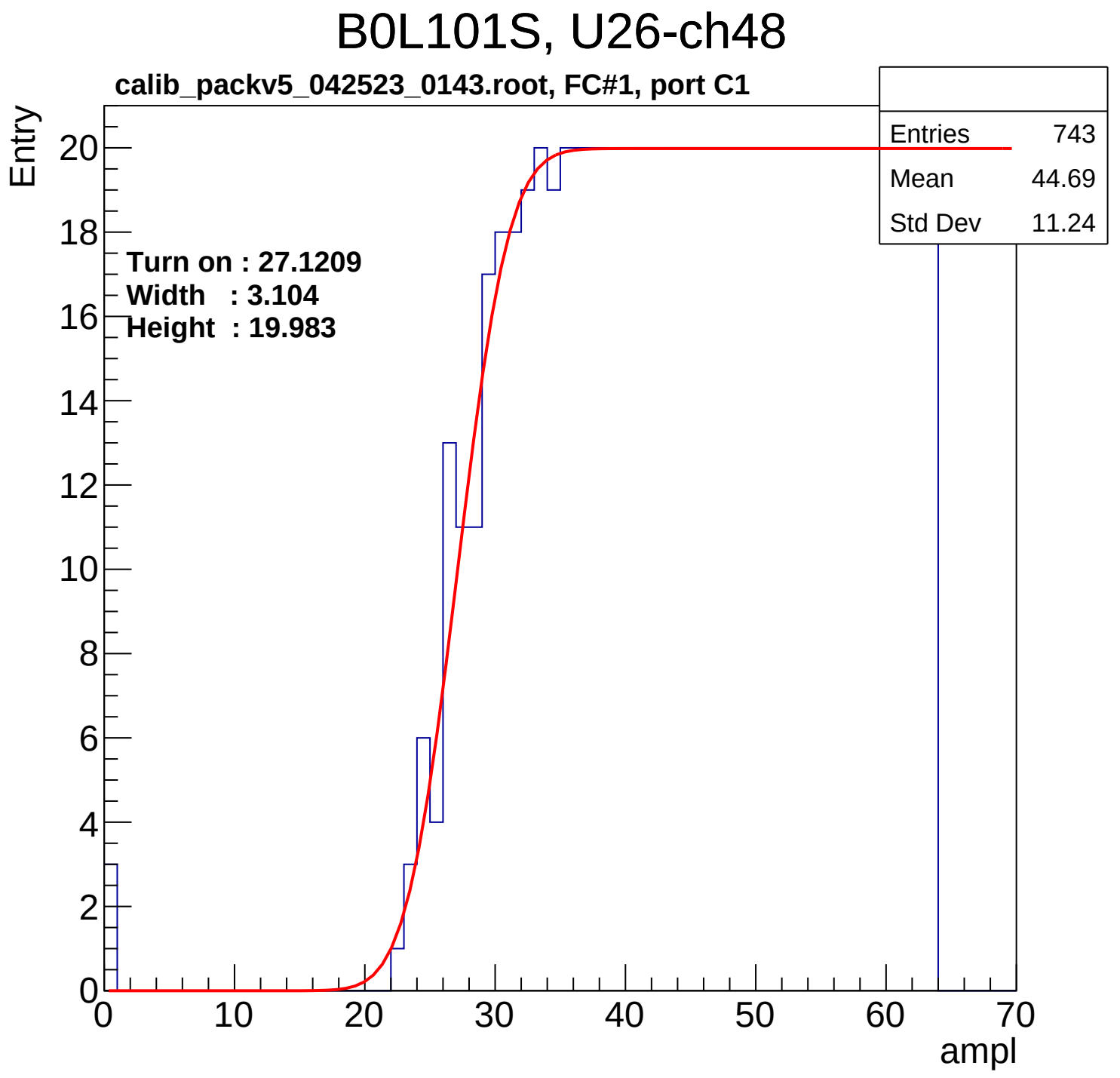
B0L101S, U26-ch48
calib_packv5_042523_0143.root, FC#1, port C1
Entries 743
Mean 44.69
Std Dev 11.24
Turn on : 27.1209
Width : 3.104
Height : 19.983
Entry
ampl
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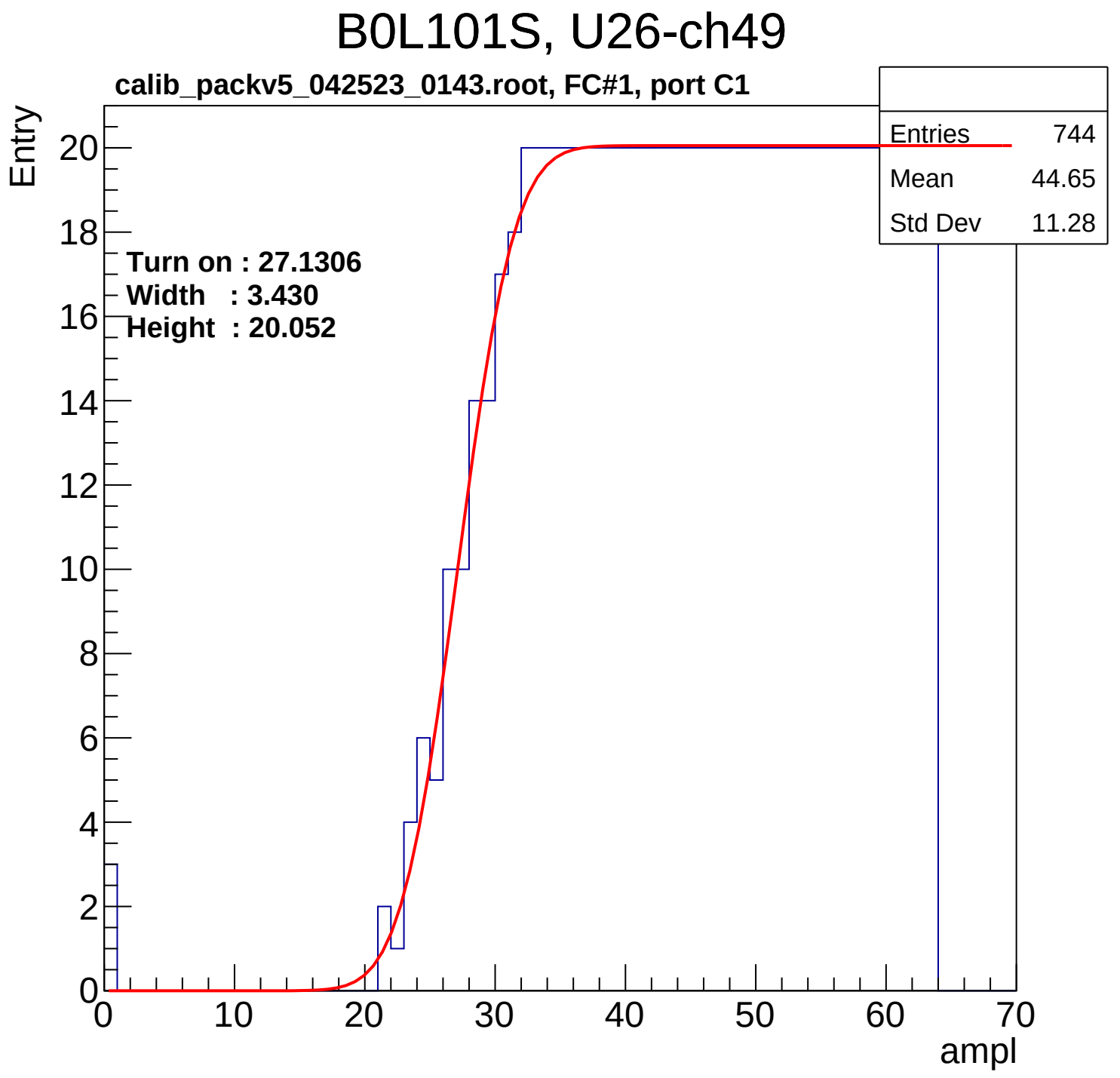
B0L101S, U26-ch49
calib_packv5_042523_0143.root, FC#1, port C1
Entries 744
Mean 44.65
Std Dev 11.28
Turn on : 27.1306
Width : 3.430
Height : 20.052
Entry
ampl
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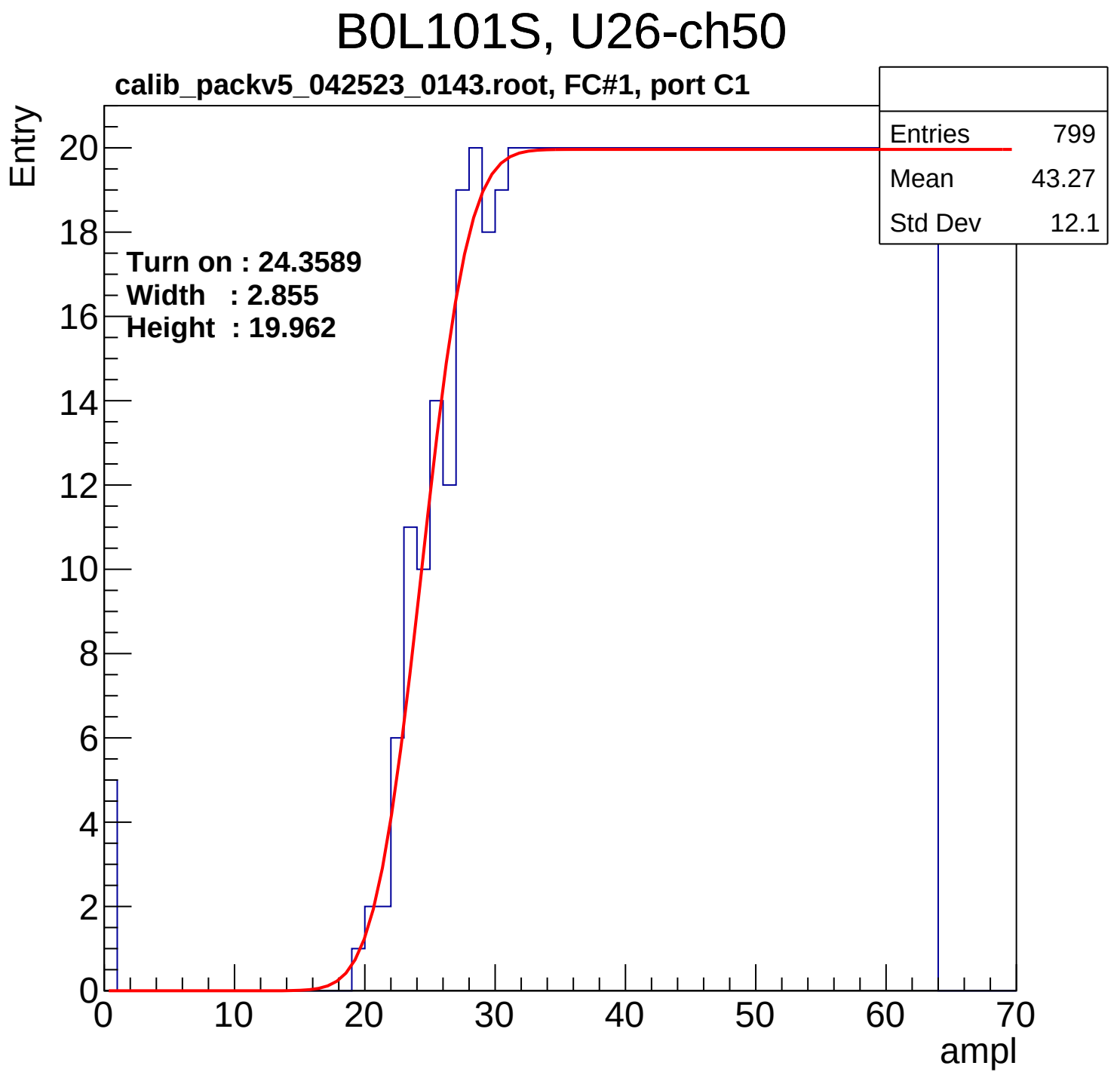
B0L101S, U26-ch50
calib_packv5_042523_0143.root, FC#1, port C1
Entries 799
Mean 43.27
Std Dev 12.1
Turn on : 24.3589
Width : 2.855
Height : 19.962
Entry
ampl
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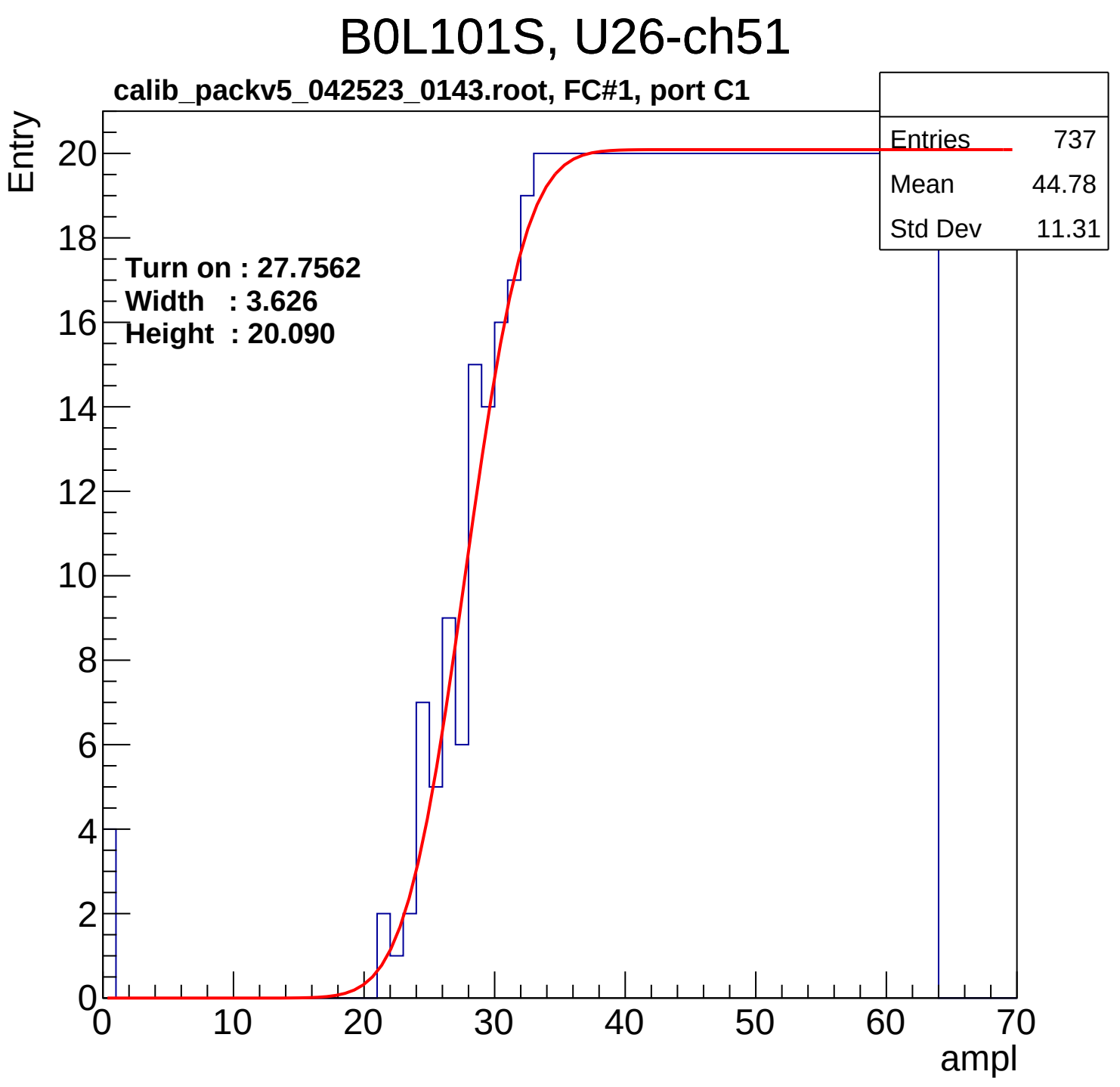
B0L101S, U26-ch51
calib_packv5_042523_0143.root, FC#1, port C1
Entries 737
Mean 44.78
Std Dev 11.31
Turn on : 27.7562
Width : 3.626
Height : 20.090
Entry
ampl
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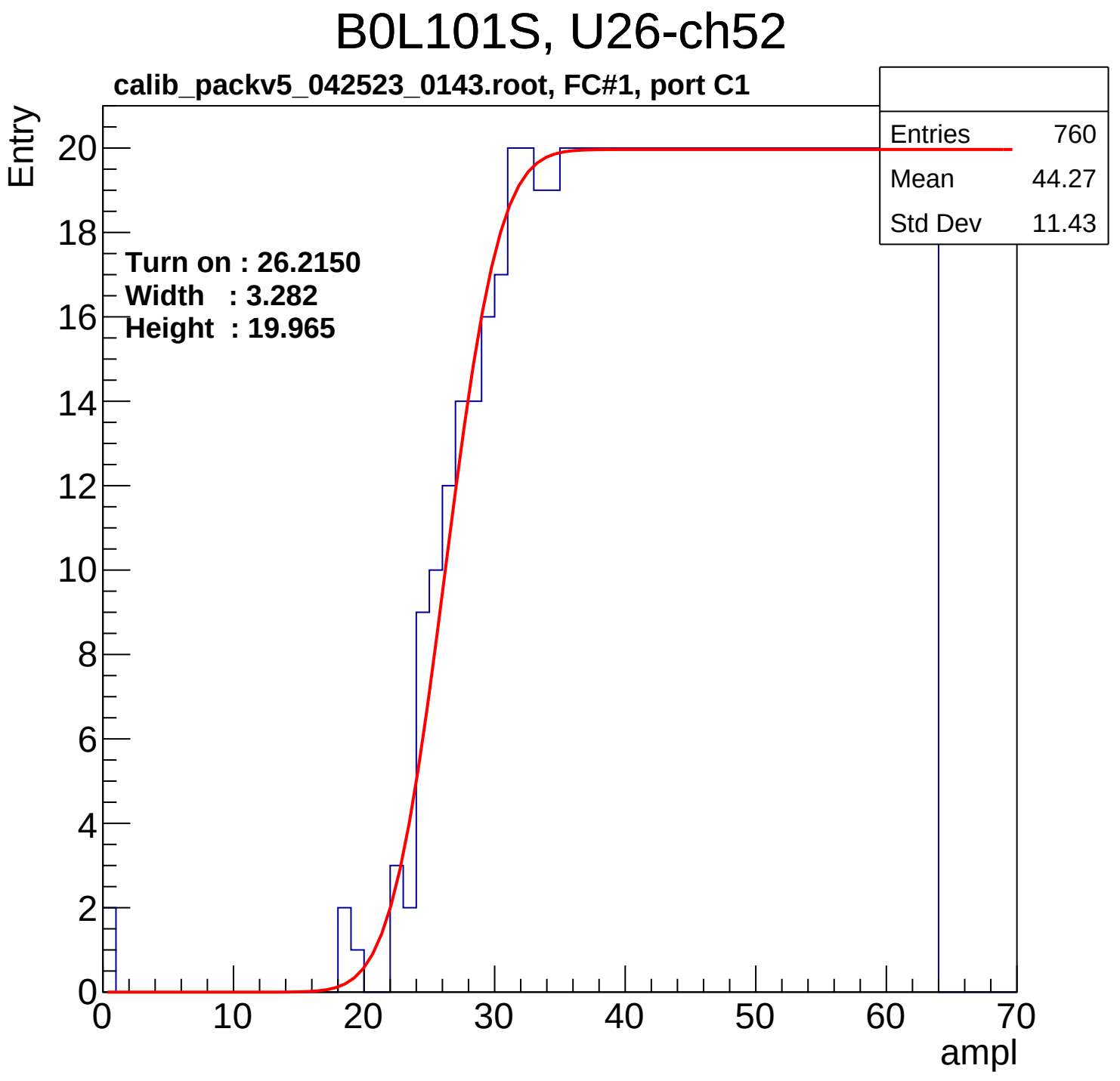
B0L101S, U26-ch52
calib_packv5_042523_0143.root, FC#1, port C1
Entries 760
Mean 44.27
Std Dev 11.43
Turn on : 26.2150
Width : 3.282
Height : 19.965
Entry
ampl
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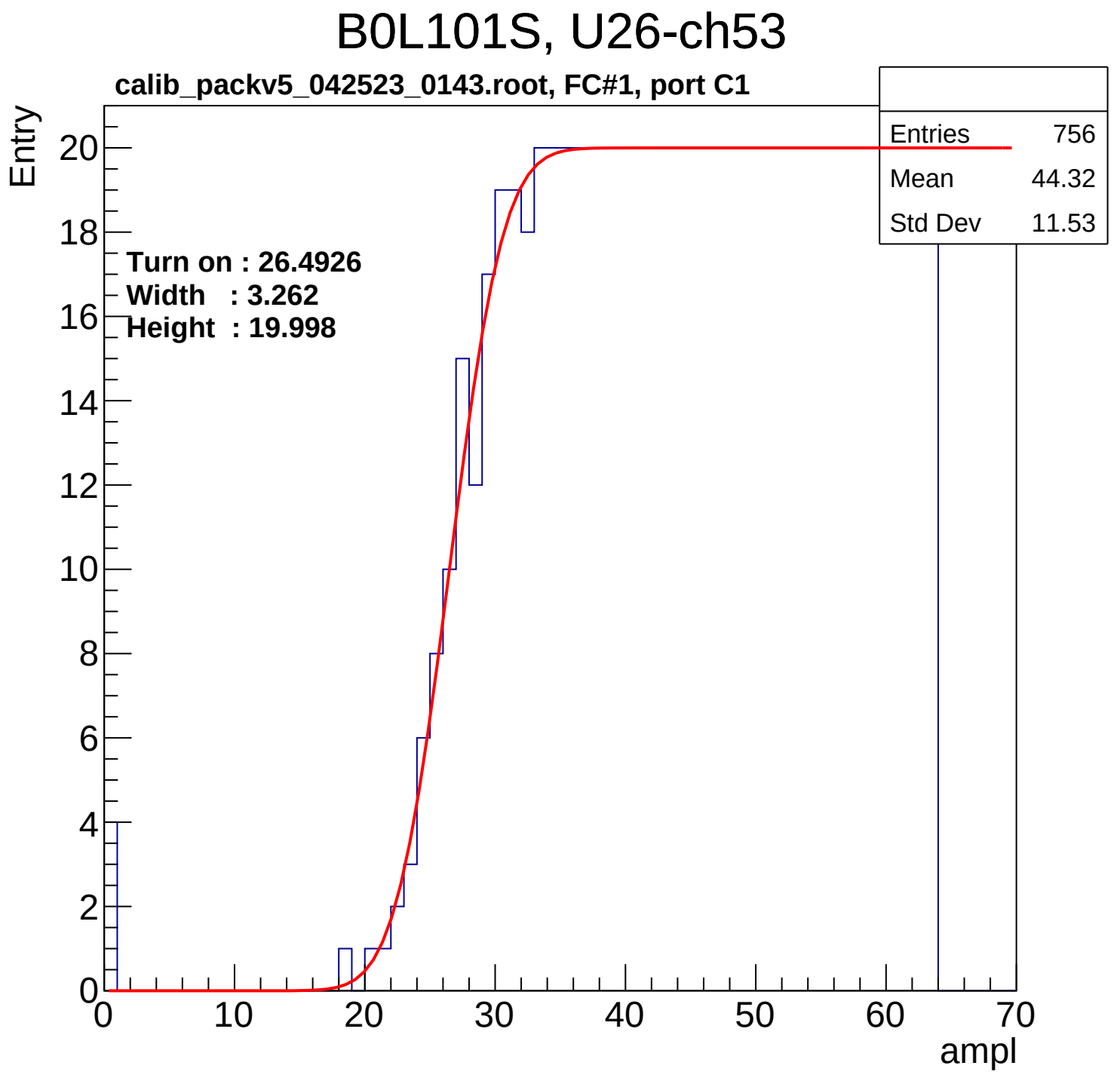
B0L101S, U26-ch53
calib_packv5_042523_0143.root, FC#1, port C1
Entries 756
Mean 44.32
Std Dev 11.53
Turn on : 26.4926
Width : 3.262
Height : 19.998
Entry
ampl
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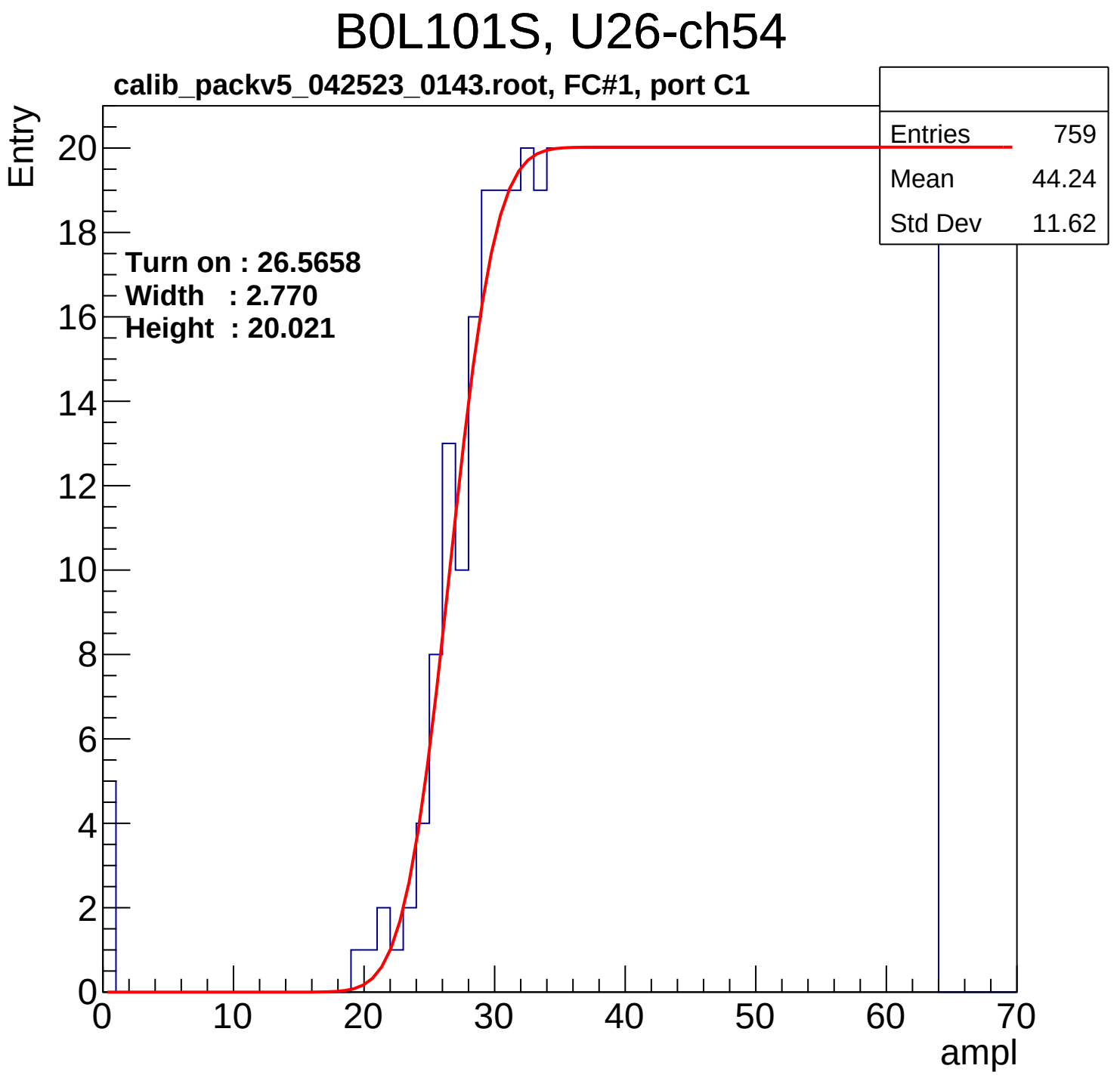
B0L101S, U26-ch54
calib_packv5_042523_0143.root, FC#1, port C1
Entries 759
Mean 44.24
Std Dev 11.62
Turn on : 26.5658
Width : 2.770
Height : 20.021
Entry
ampl
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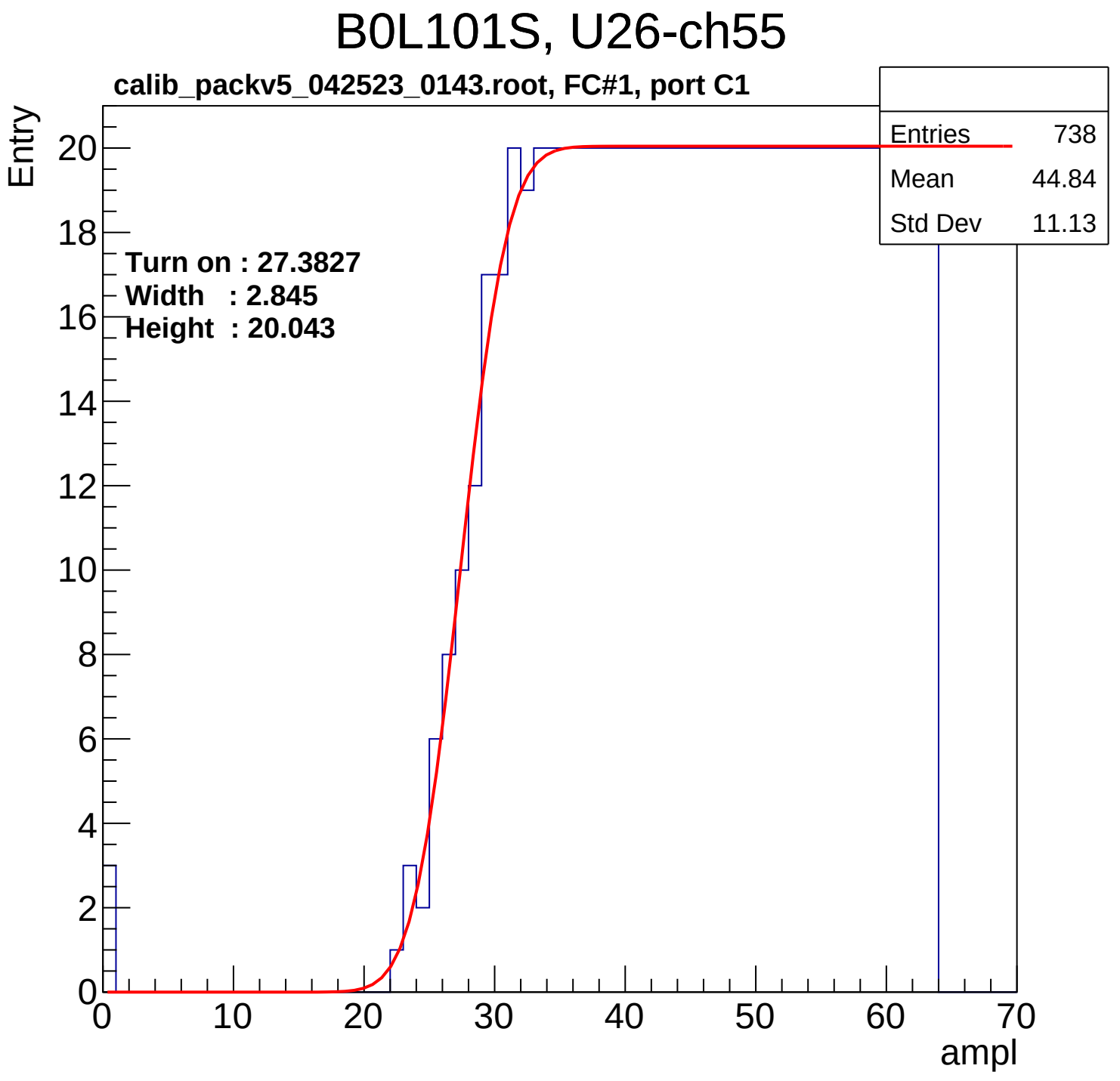
B0L101S, U26-ch55
calib_packv5_042523_0143.root, FC#1, port C1
Entries 738
Mean 44.84
Std Dev 11.13
Turn on : 27.3827
Width : 2.845
Height : 20.043
Entry
ampl
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6
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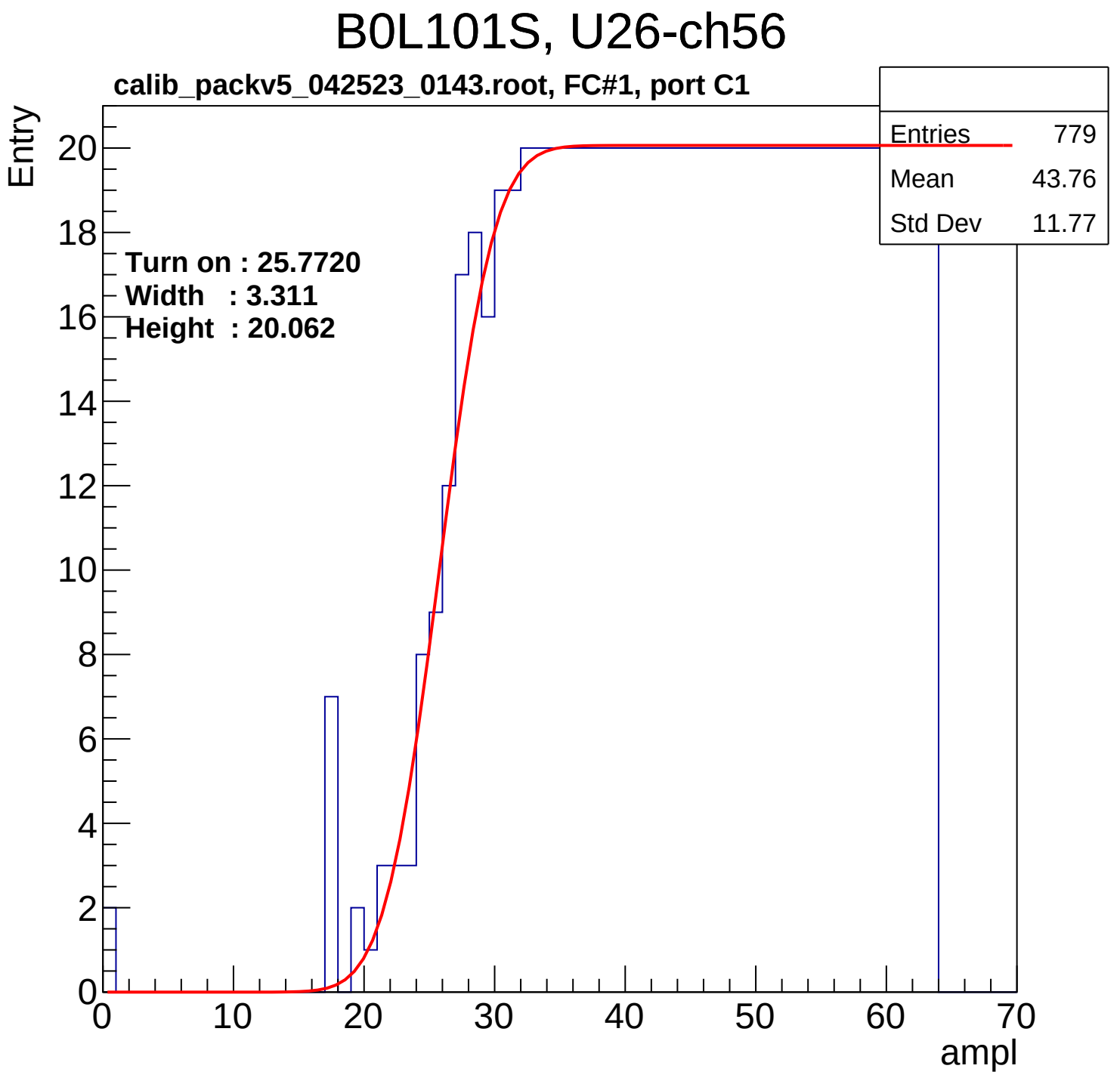
B0L101S, U26-ch56
calib_packv5_042523_0143.root, FC#1, port C1
Entries 779
Mean 43.76
Std Dev 11.77
Turn on : 25.7720
Width : 3.311
Height : 20.062
Entry
ampl
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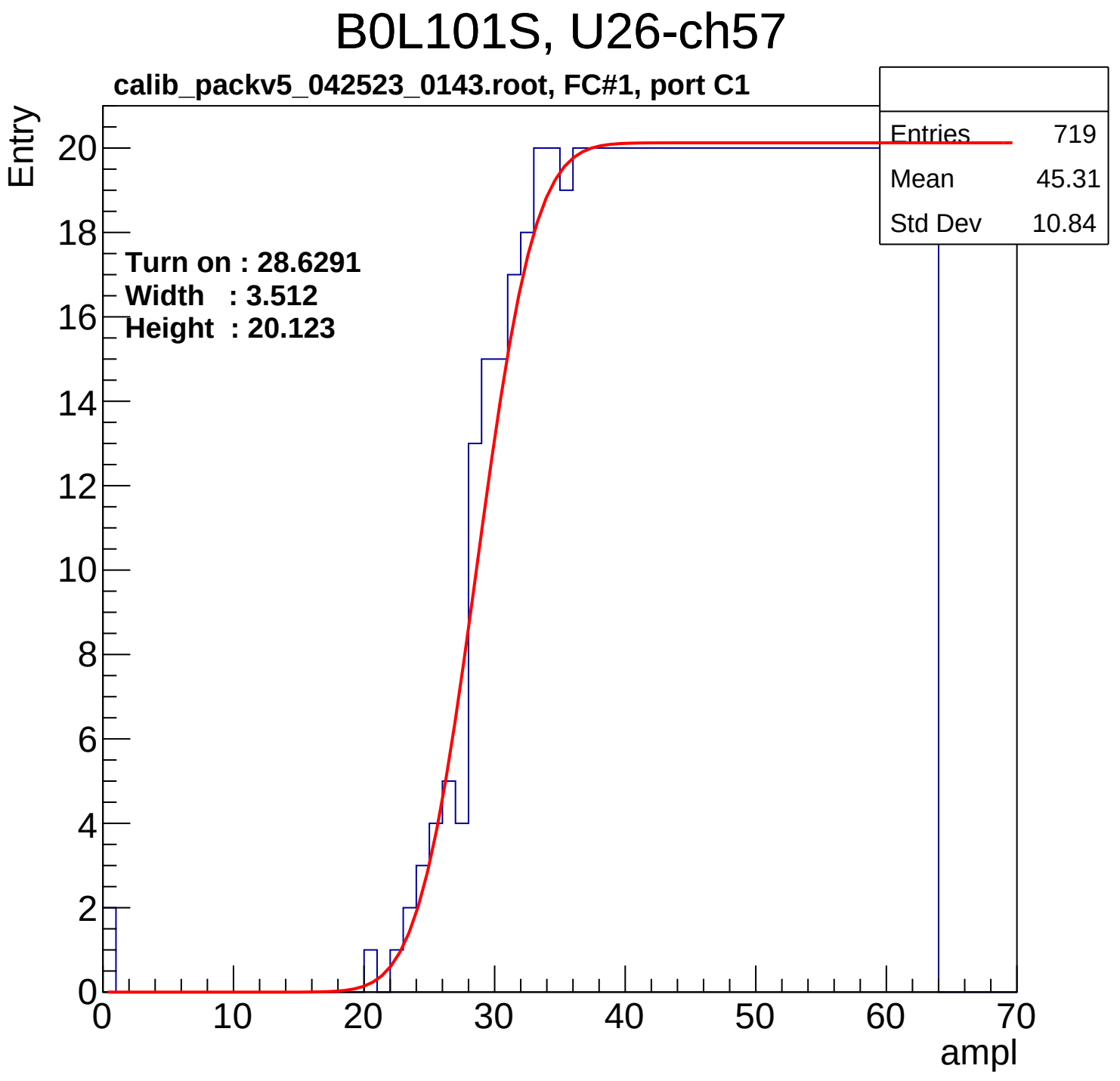
B0L101S, U26-ch57
calib_packv5_042523_0143.root, FC#1, port C1
Entries 719
Mean 45.31
Std Dev 10.84
Turn on : 28.6291
Width : 3.512
Height : 20.123
Entry
ampl
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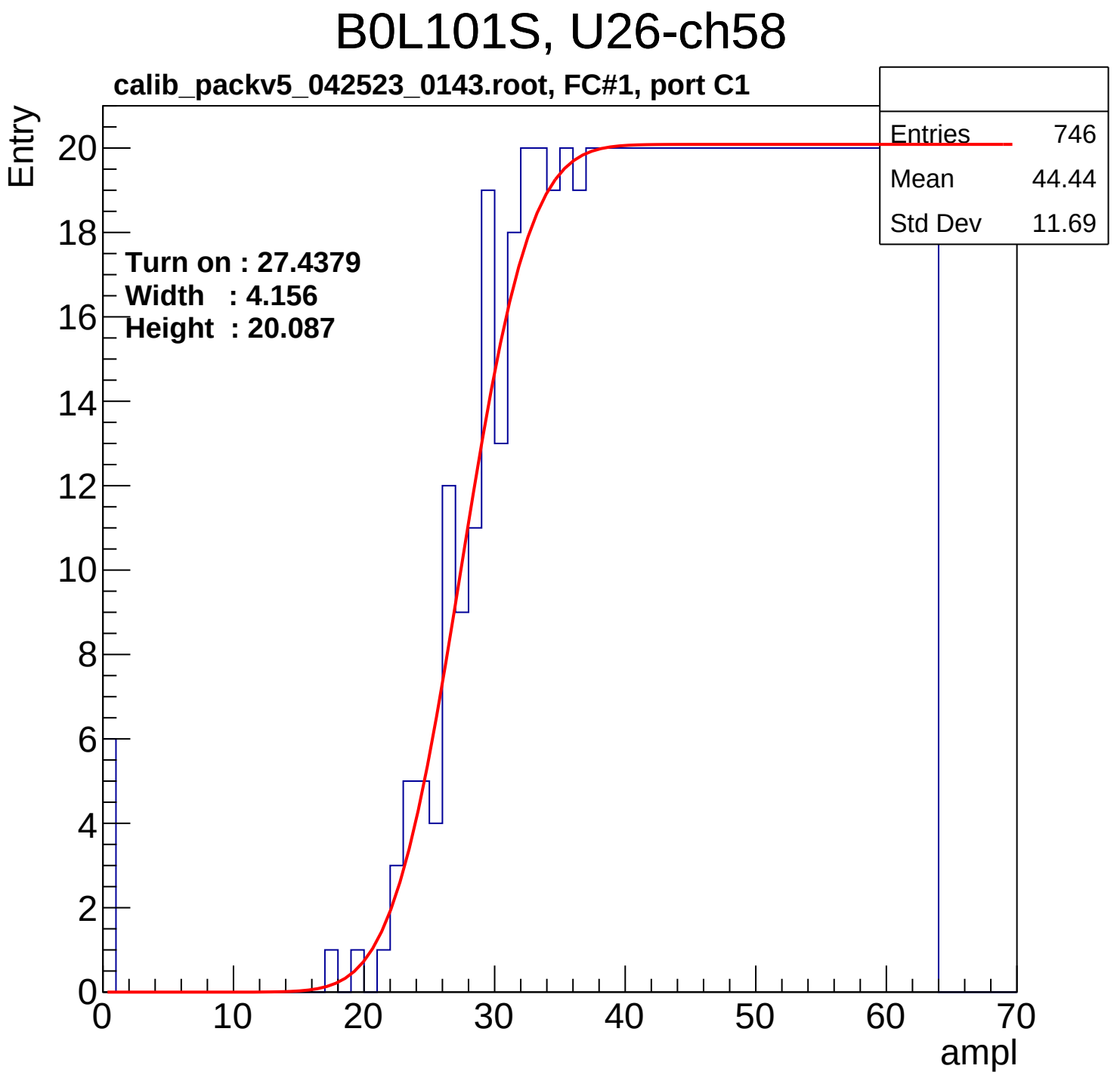
B0L101S, U26-ch58
calib_packv5_042523_0143.root, FC#1, port C1
Entries 746
Mean 44.44
Std Dev 11.69
Turn on : 27.4379
Width : 4.156
Height : 20.087
Entry
ampl
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6
8
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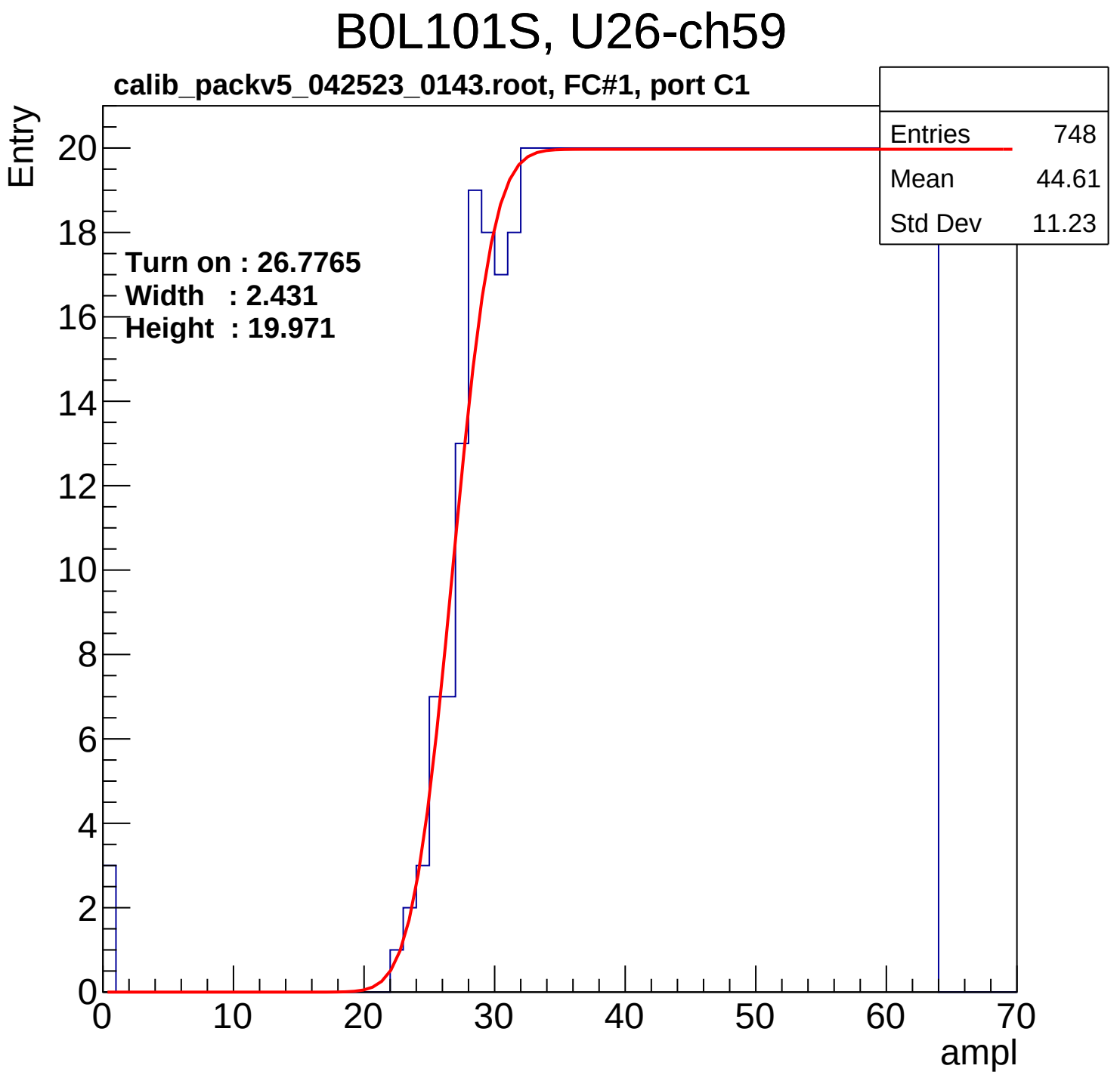
B0L101S, U26-ch59
calib_packv5_042523_0143.root, FC#1, port C1
Entries 748
Mean 44.61
Std Dev 11.23
Turn on : 26.7765
Width : 2.431
Height : 19.971
Entry
ampl
0
2
4
6
8
10
12
14
16
18
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0
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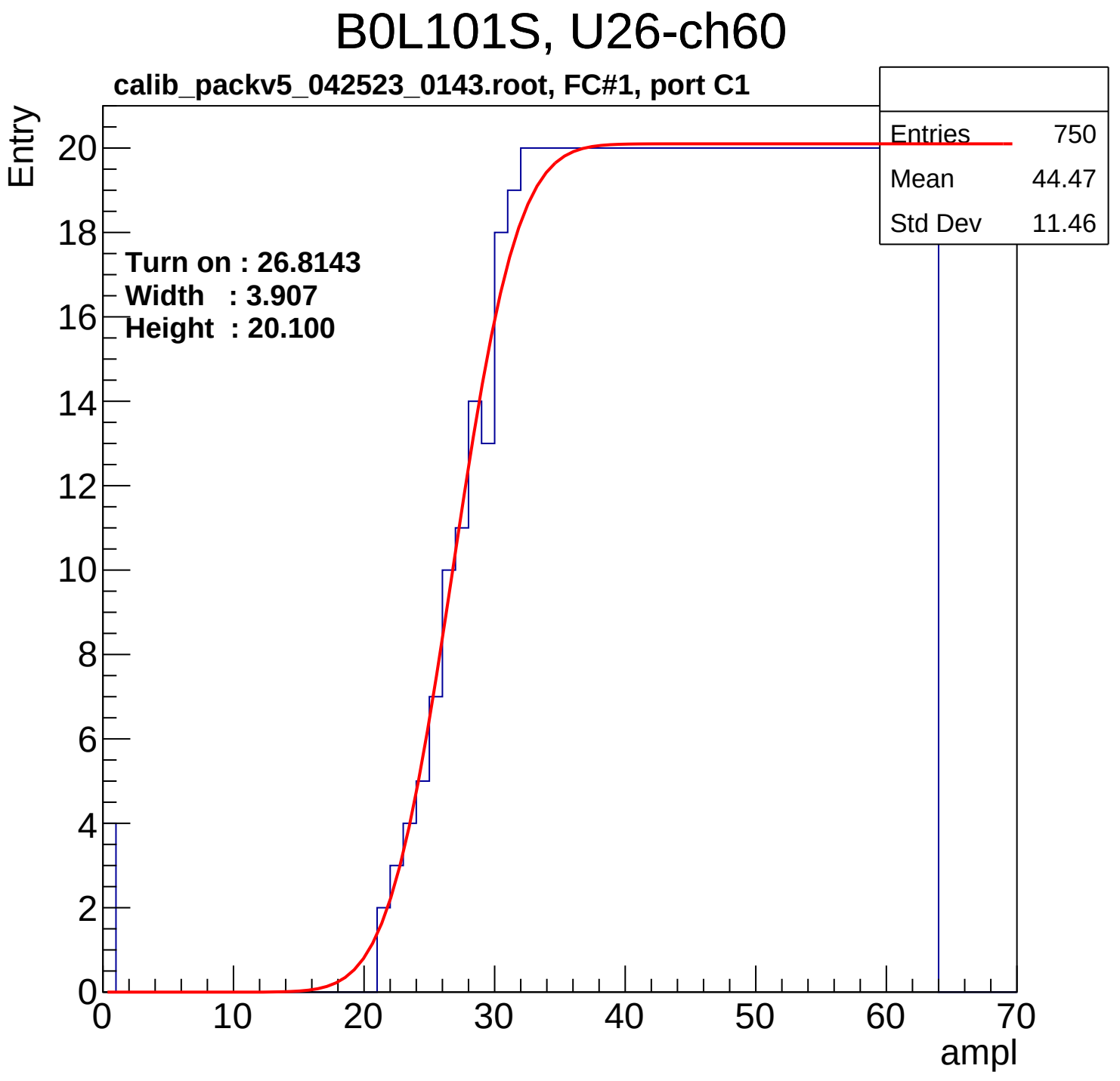
B0L101S, U26-ch60
calib_packv5_042523_0143.root, FC#1, port C1
Entries 750
Mean 44.47
Std Dev 11.46
Turn on : 26.8143
Width : 3.907
Height : 20.100
Entry
ampl
0
2
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6
8
10
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14
16
18
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0
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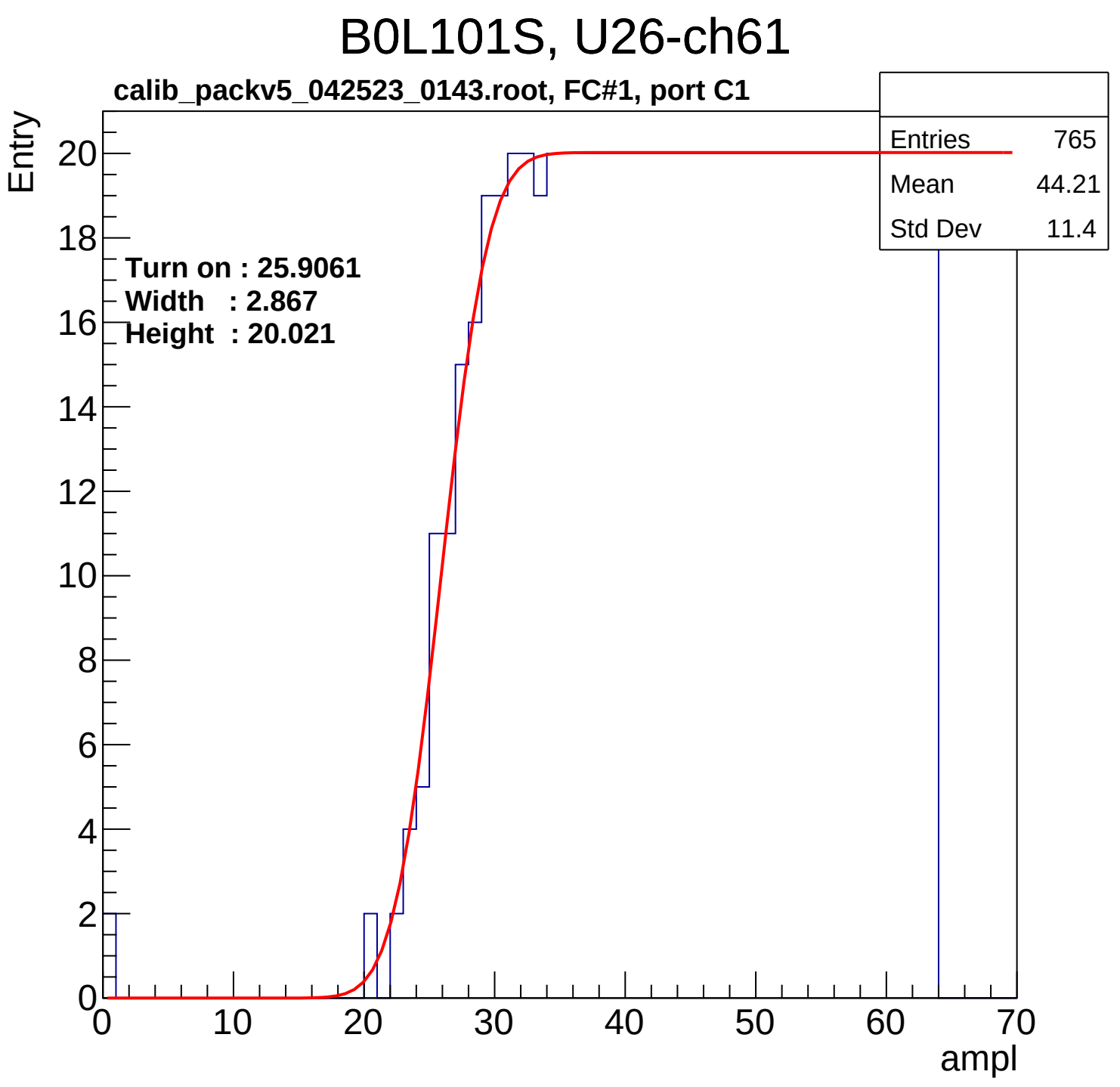
B0L101S, U26-ch61
calib_packv5_042523_0143.root, FC#1, port C1
Entries 765
Mean 44.21
Std Dev 11.4
Turn on : 25.9061
Width : 2.867
Height : 20.021
Entry
ampl
0
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4
6
8
10
12
14
16
18
20
0
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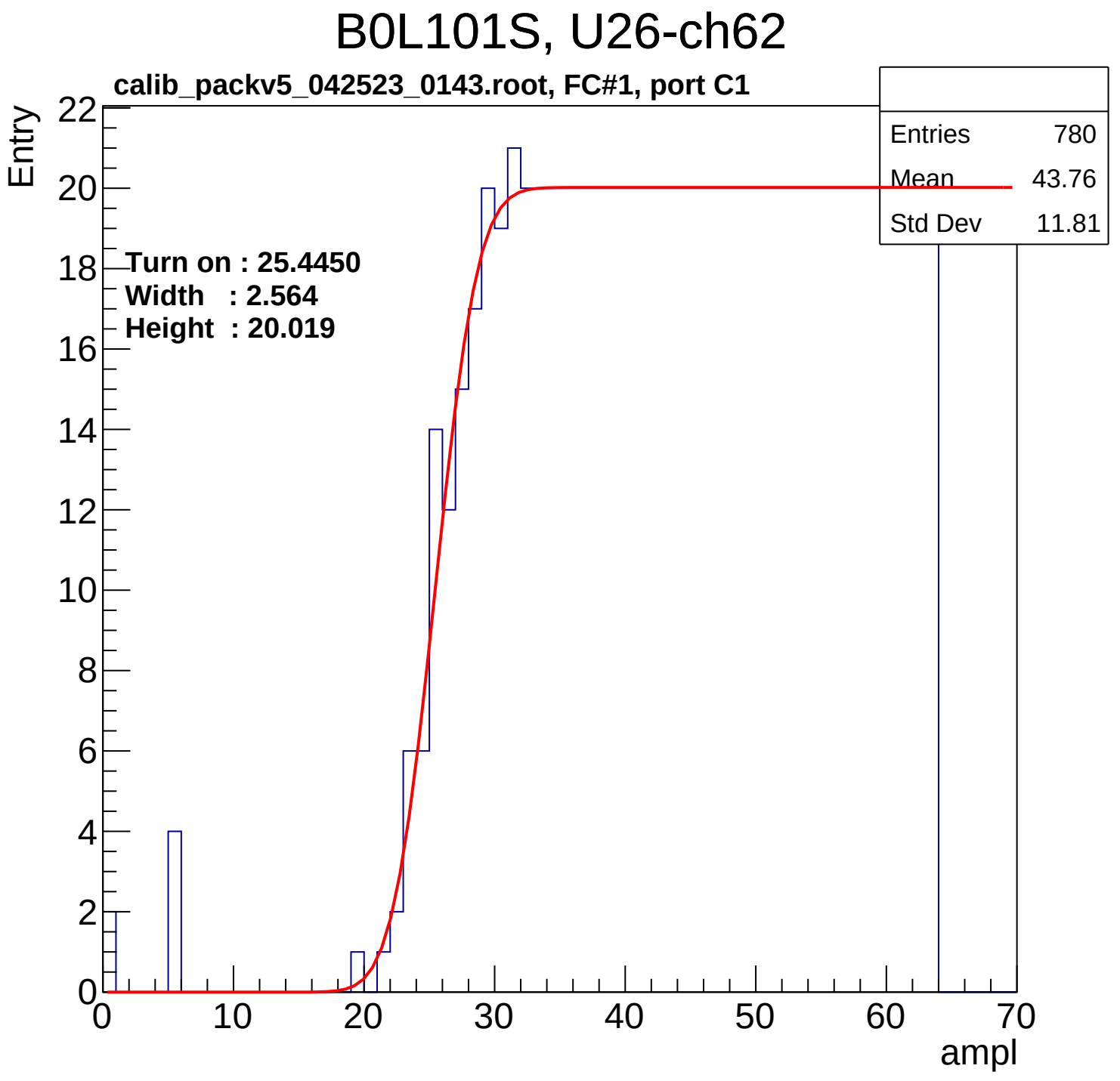
B0L101S, U26-ch62
calib_packv5_042523_0143.root, FC#1, port C1
Entries 780
Mean 43.76
Std Dev 11.81
Turn on : 25.4450
Width : 2.564
Height : 20.019
Entry
ampl
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8
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16
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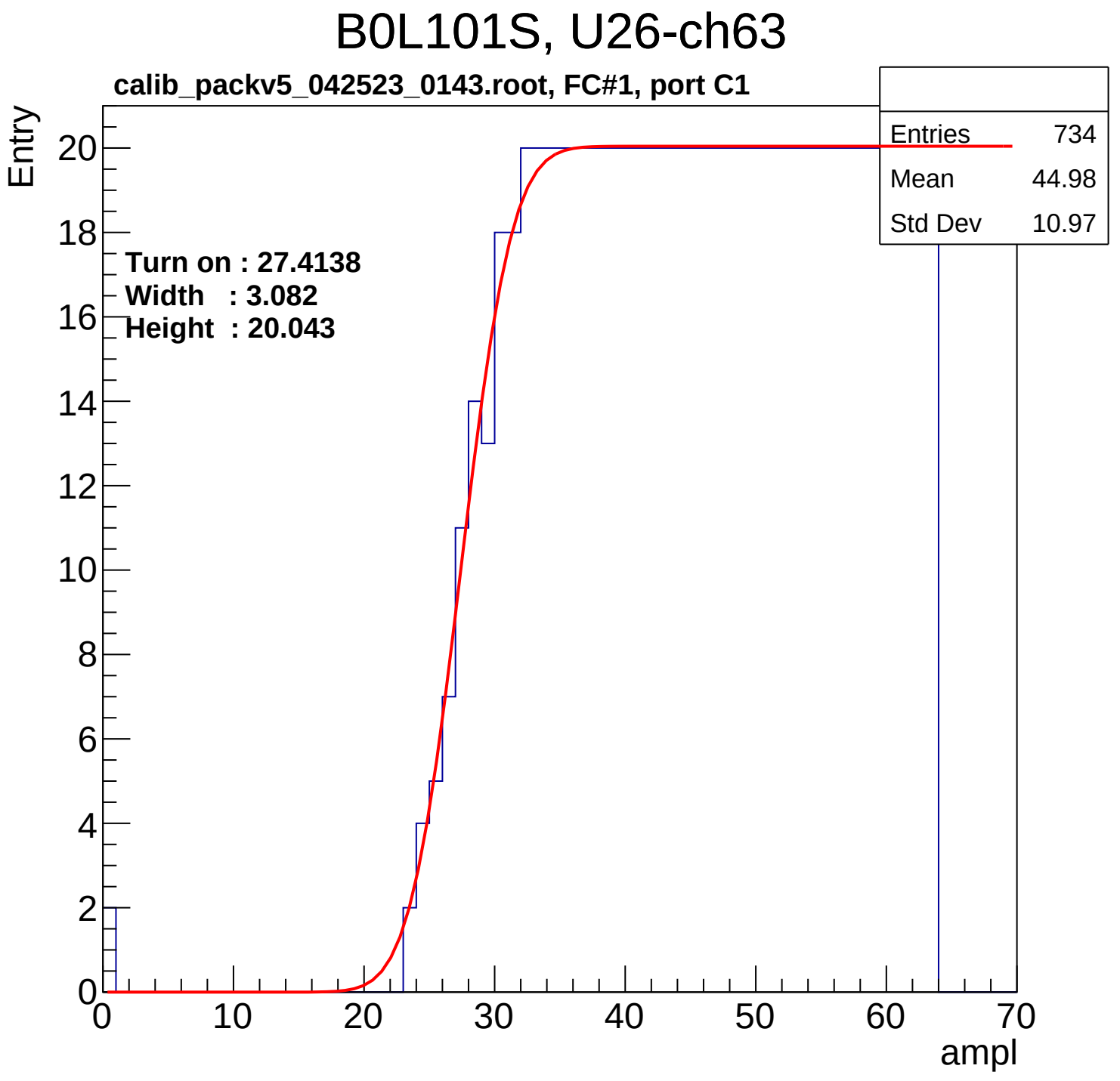
B0L101S, U26-ch63
calib_packv5_042523_0143.root, FC#1, port C1
Entries 734
Mean 44.98
Std Dev 10.97
Turn on : 27.4138
Width : 3.082
Height : 20.043
Entry
ampl
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6
8
10
12
14
16
18
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0
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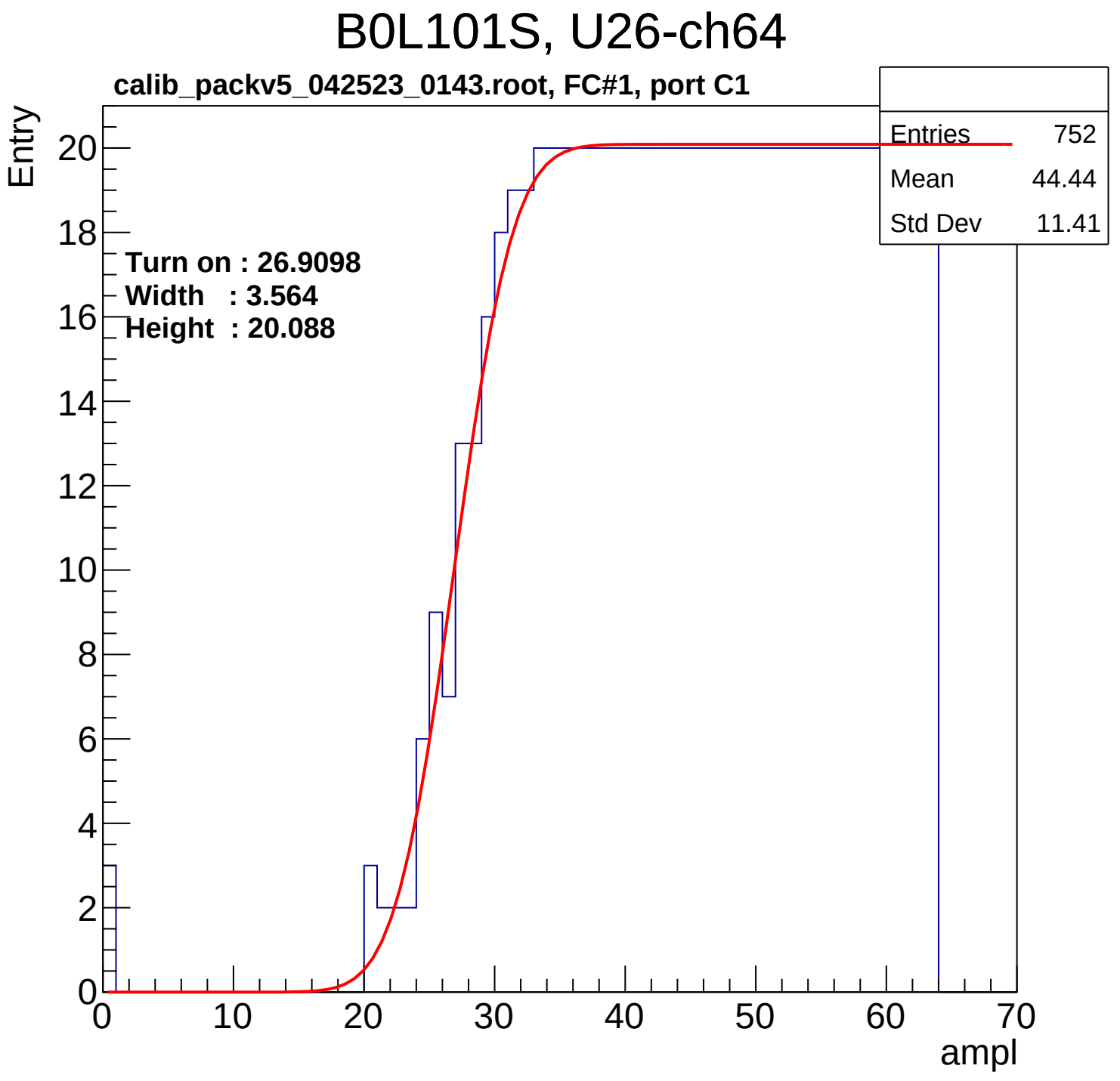
B0L101S, U26-ch64
calib_packv5_042523_0143.root, FC#1, port C1
Entries 752
Mean 44.44
Std Dev 11.41
Turn on : 26.9098
Width : 3.564
Height : 20.088
Entry
ampl
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6
8
10
12
14
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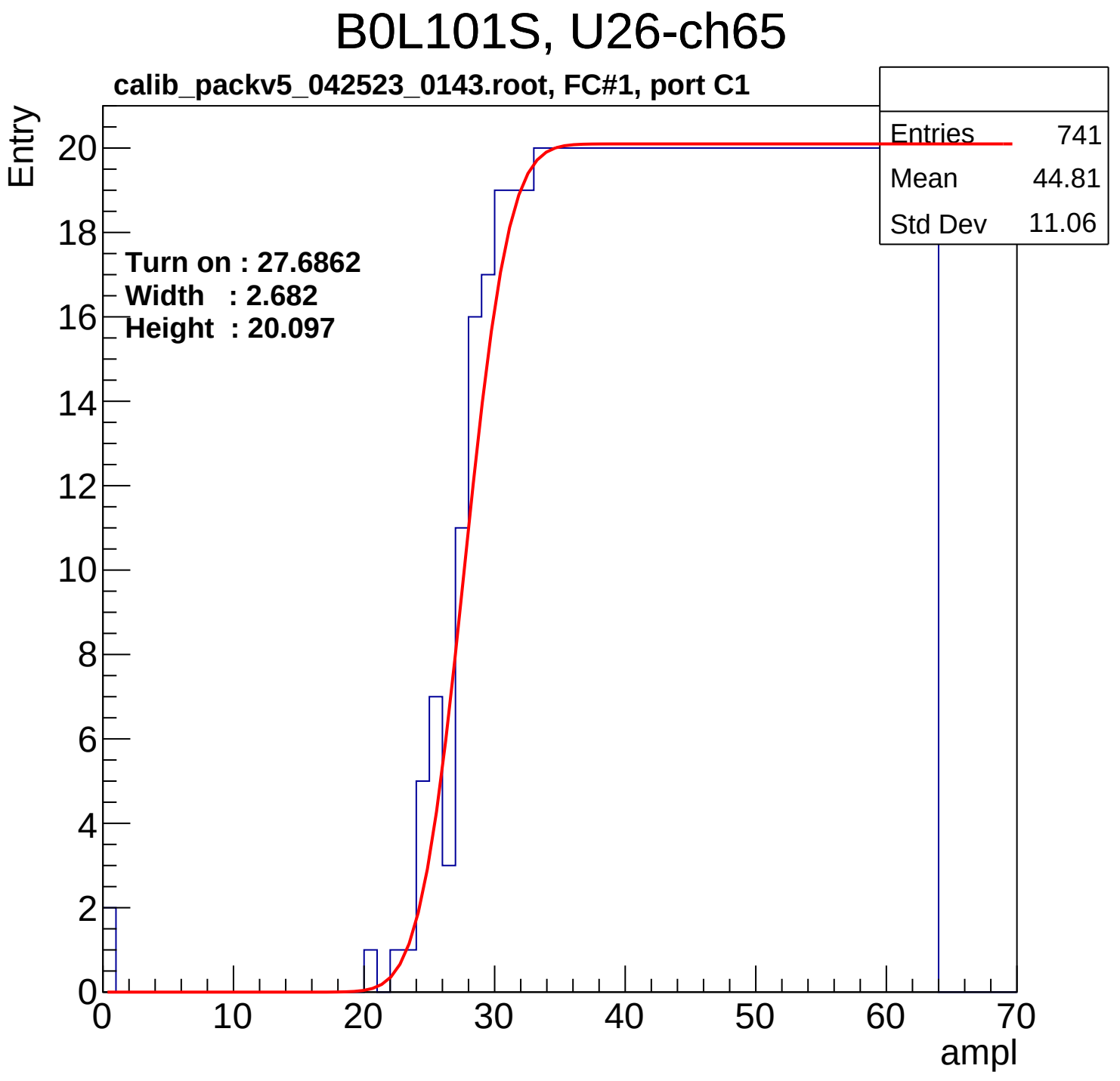
B0L101S, U26-ch65
calib_packv5_042523_0143.root, FC#1, port C1
Entries 741
Mean 44.81
Std Dev 11.06
Turn on : 27.6862
Width : 2.682
Height : 20.097
Entry
ampl
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6
8
10
12
14
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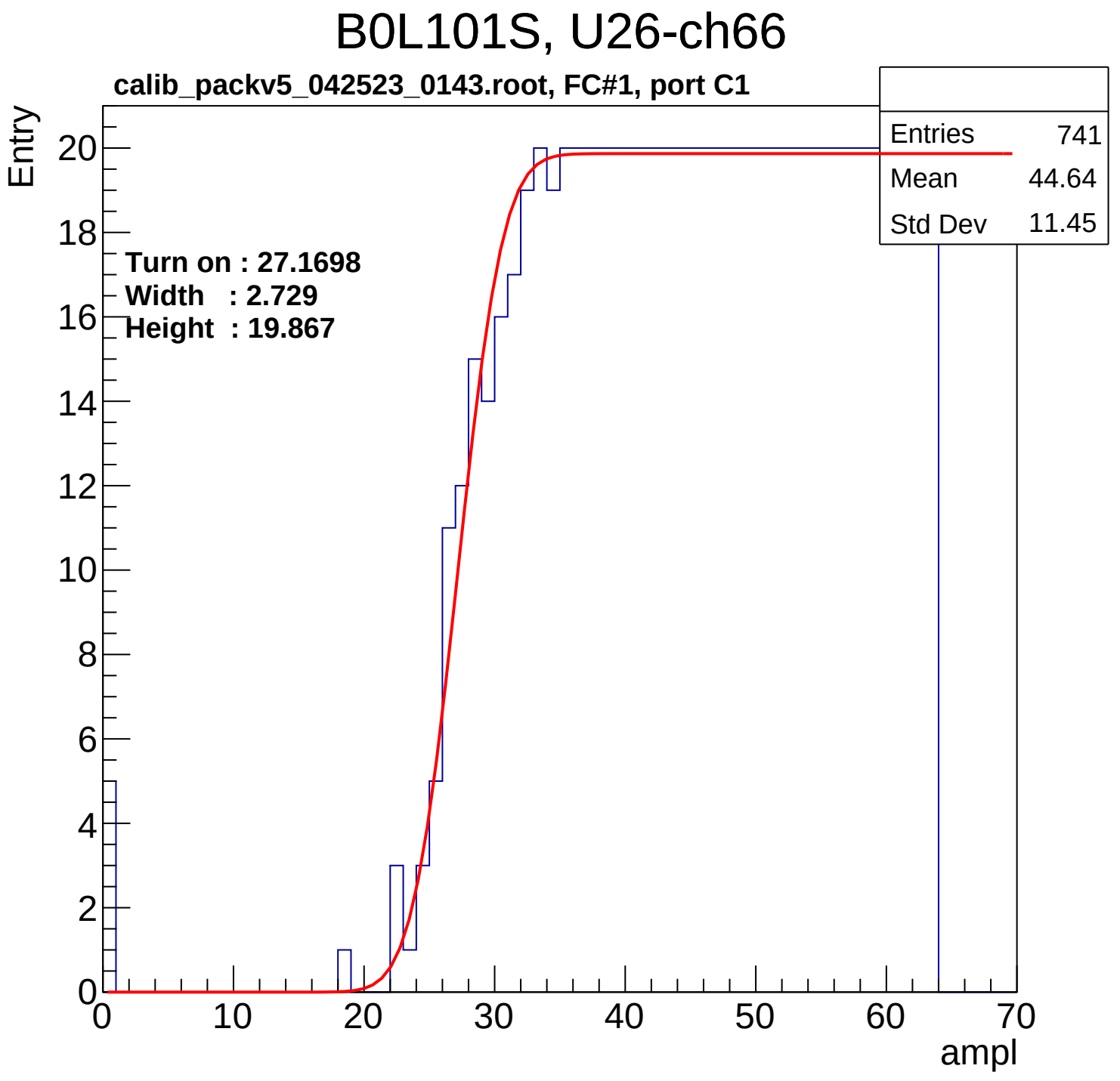
B0L101S, U26-ch66
calib_packv5_042523_0143.root, FC#1, port C1
Entries 741
Mean 44.64
Std Dev 11.45
Turn on : 27.1698
Width : 2.729
Height : 19.867
Entry
ampl
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6
8
10
12
14
16
18
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0
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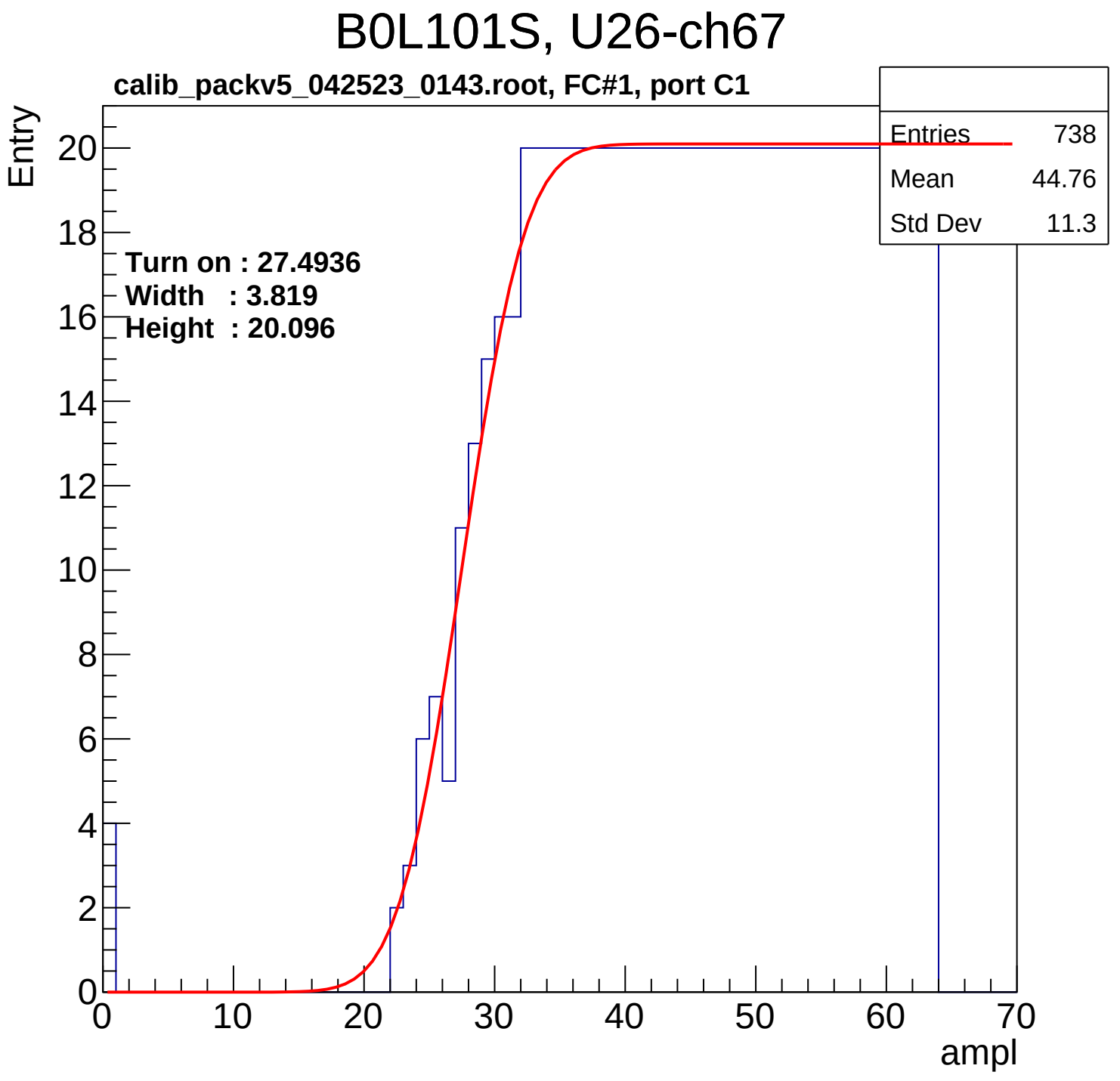
B0L101S, U26-ch67
calib_packv5_042523_0143.root, FC#1, port C1
Entries 738
Mean 44.76
Std Dev 11.3
Turn on : 27.4936
Width : 3.819
Height : 20.096
Entry
ampl
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6
8
10
12
14
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0
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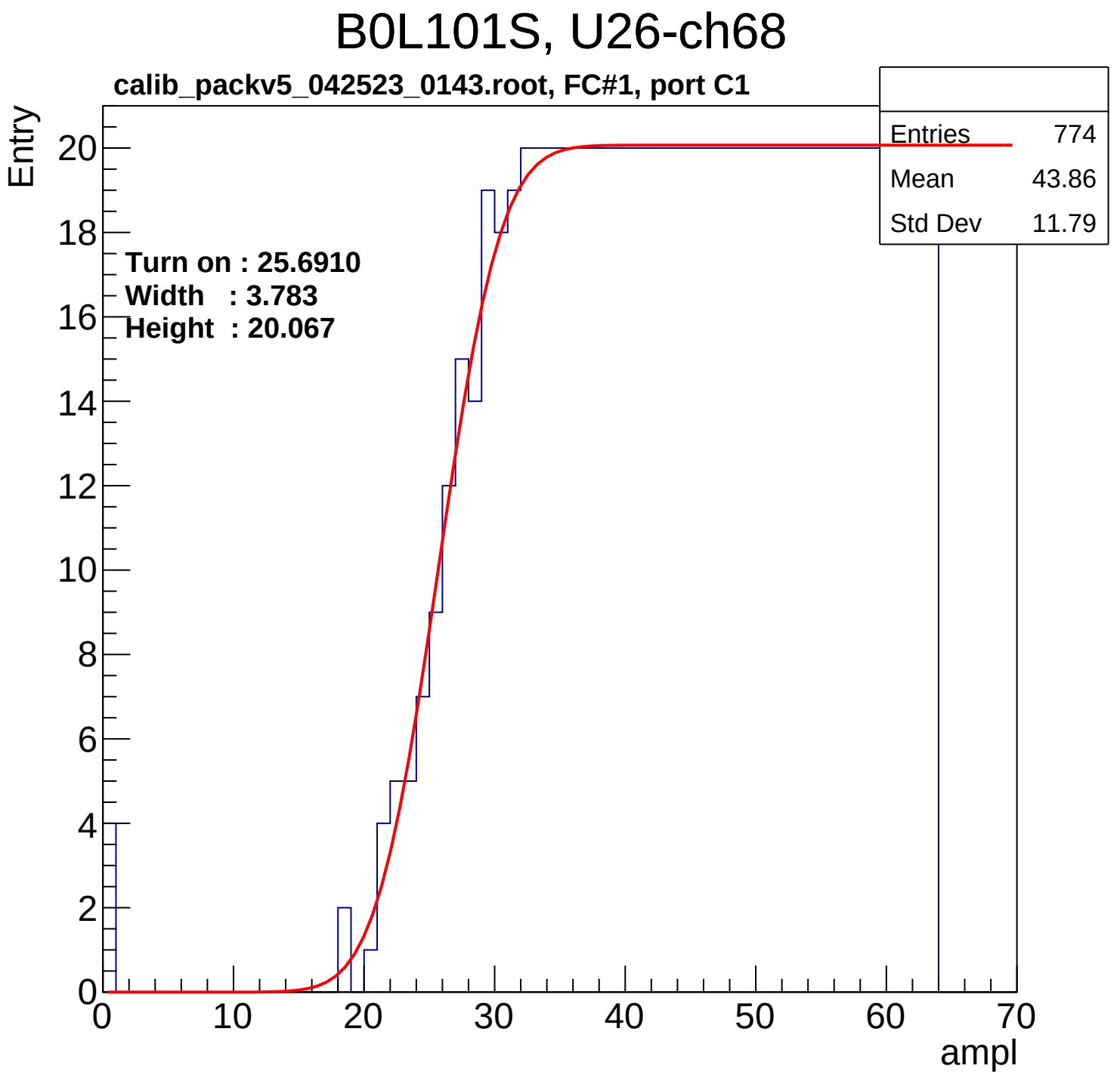
B0L101S, U26-ch68
calib_packv5_042523_0143.root, FC#1, port C1
Entries 774
Mean 43.86
Std Dev 11.79
Turn on : 25.6910
Width : 3.783
Height : 20.067
Entry
ampl
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6
8
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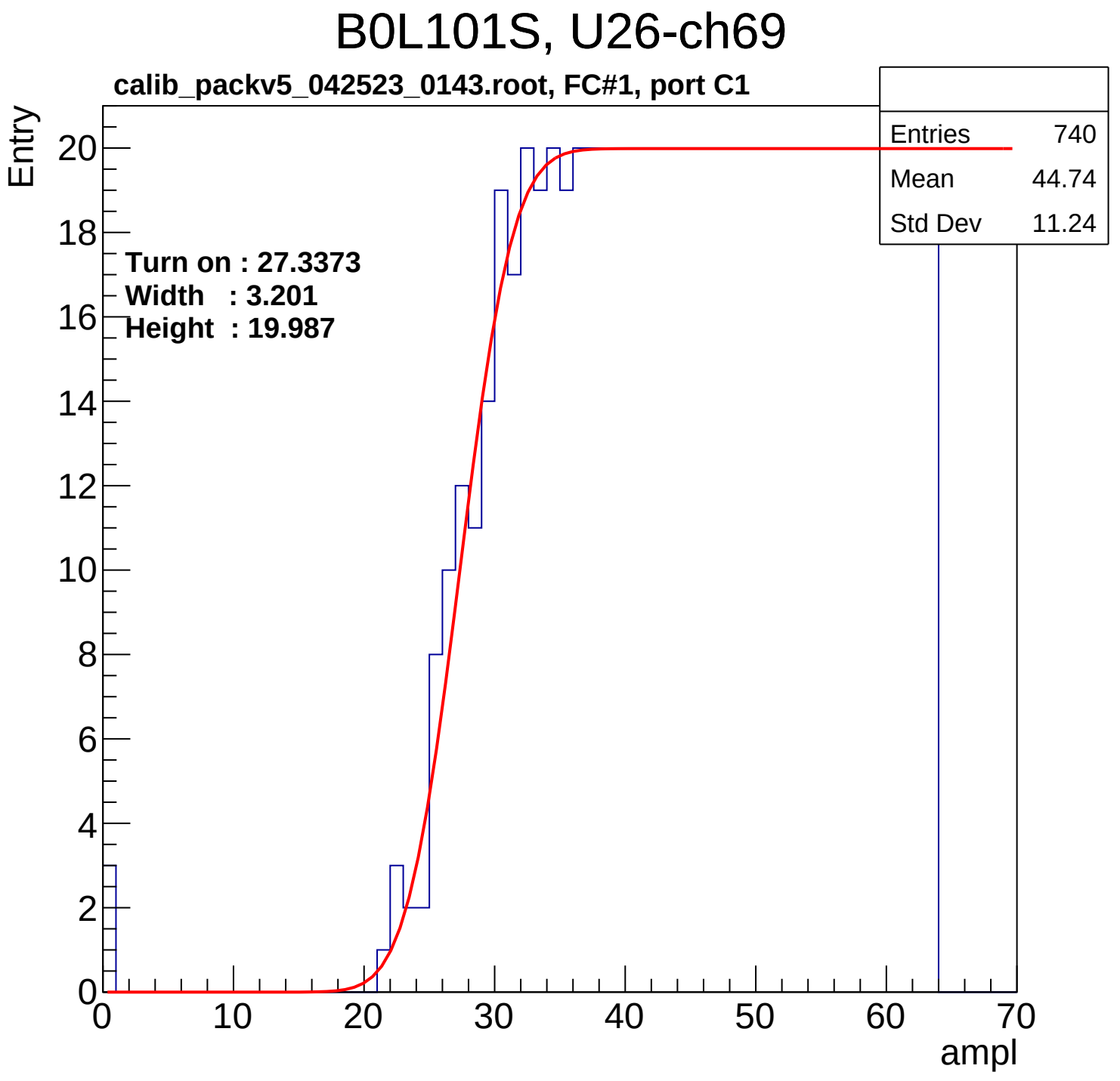
B0L101S, U26-ch69
calib_packv5_042523_0143.root, FC#1, port C1
Entries 740
Mean 44.74
Std Dev 11.24
Turn on : 27.3373
Width : 3.201
Height : 19.987
Entry
ampl
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6
8
10
12
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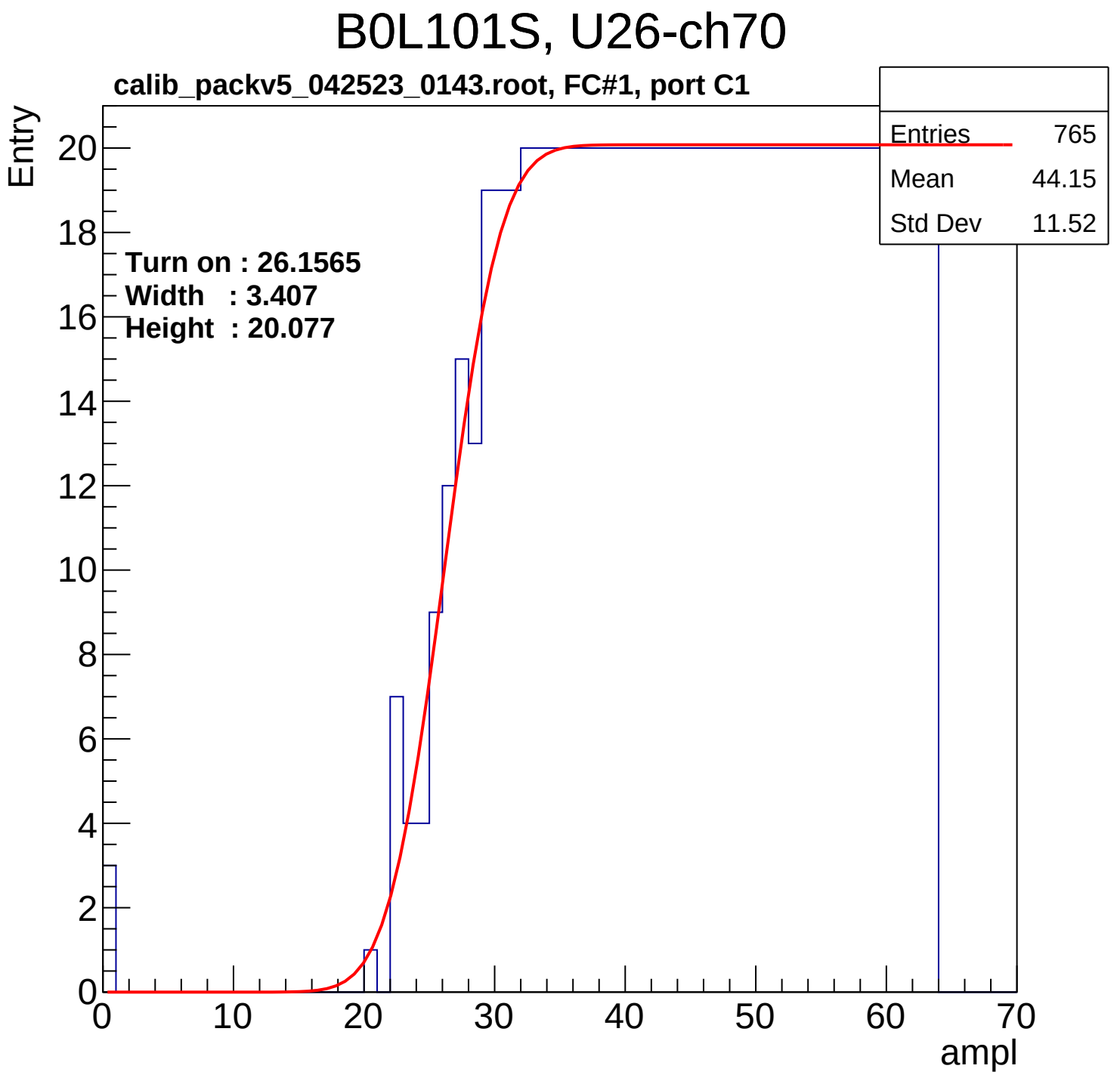
B0L101S, U26-ch70
calib_packv5_042523_0143.root, FC#1, port C1
Entries 765
Mean 44.15
Std Dev 11.52
Turn on : 26.1565
Width : 3.407
Height : 20.077
Entry
ampl
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6
8
10
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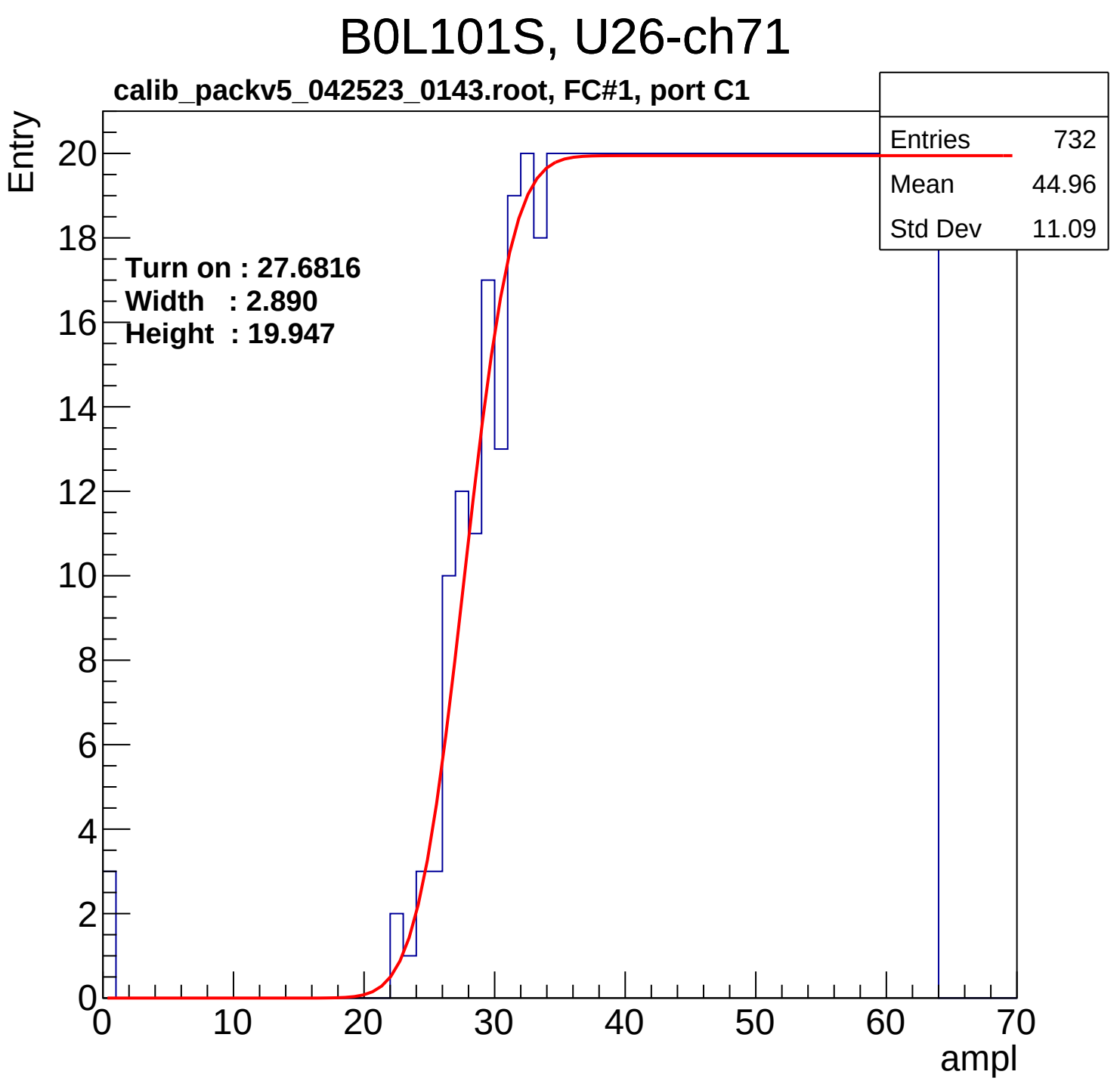
B0L101S, U26-ch71
calib_packv5_042523_0143.root, FC#1, port C1
Entries 732
Mean 44.96
Std Dev 11.09
Turn on : 27.6816
Width : 2.890
Height : 19.947
Entry
ampl
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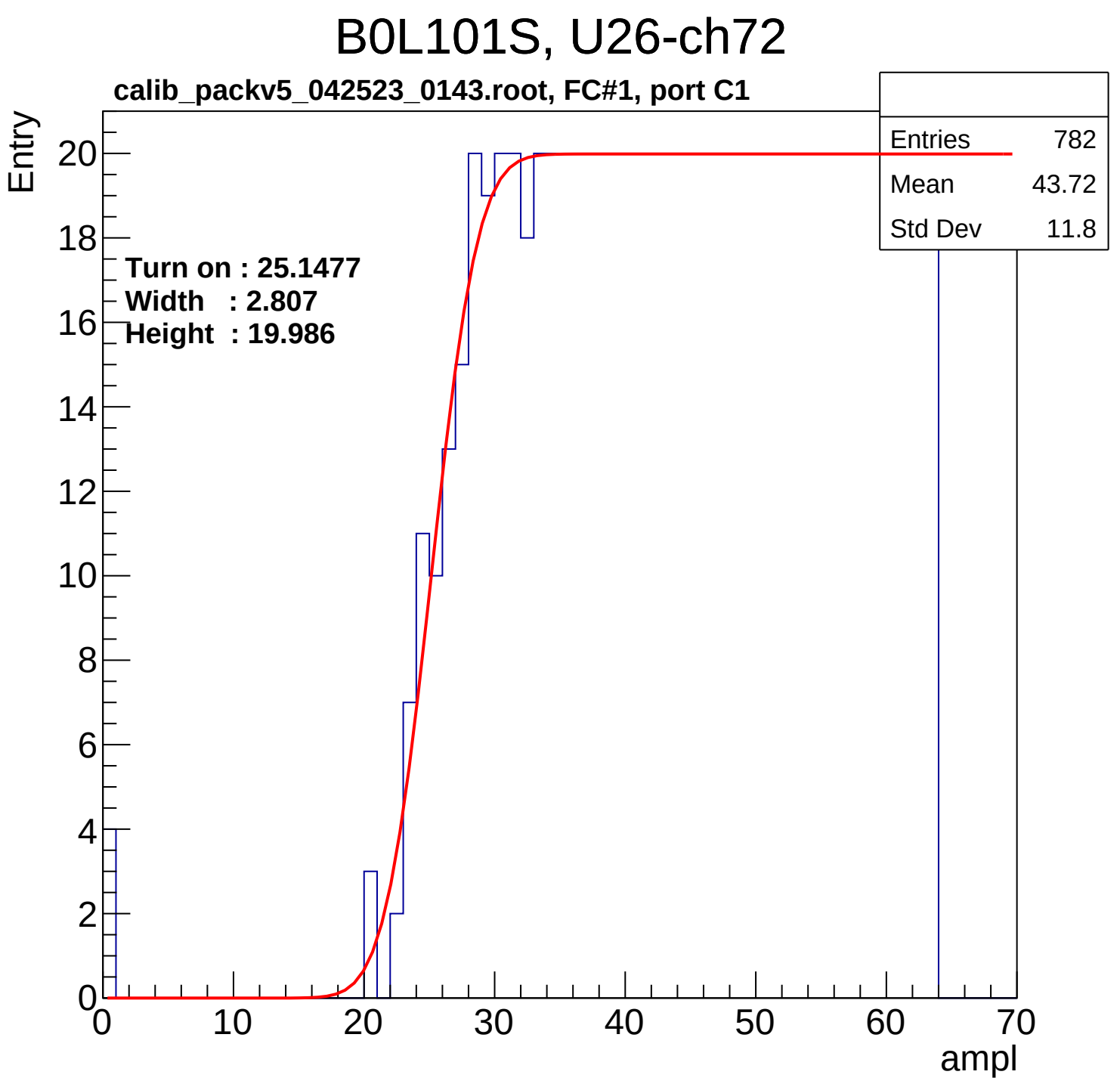
B0L101S, U26-ch72
calib_packv5_042523_0143.root, FC#1, port C1
Entries 782
Mean 43.72
Std Dev 11.8
Turn on : 25.1477
Width : 2.807
Height : 19.986
Entry
ampl
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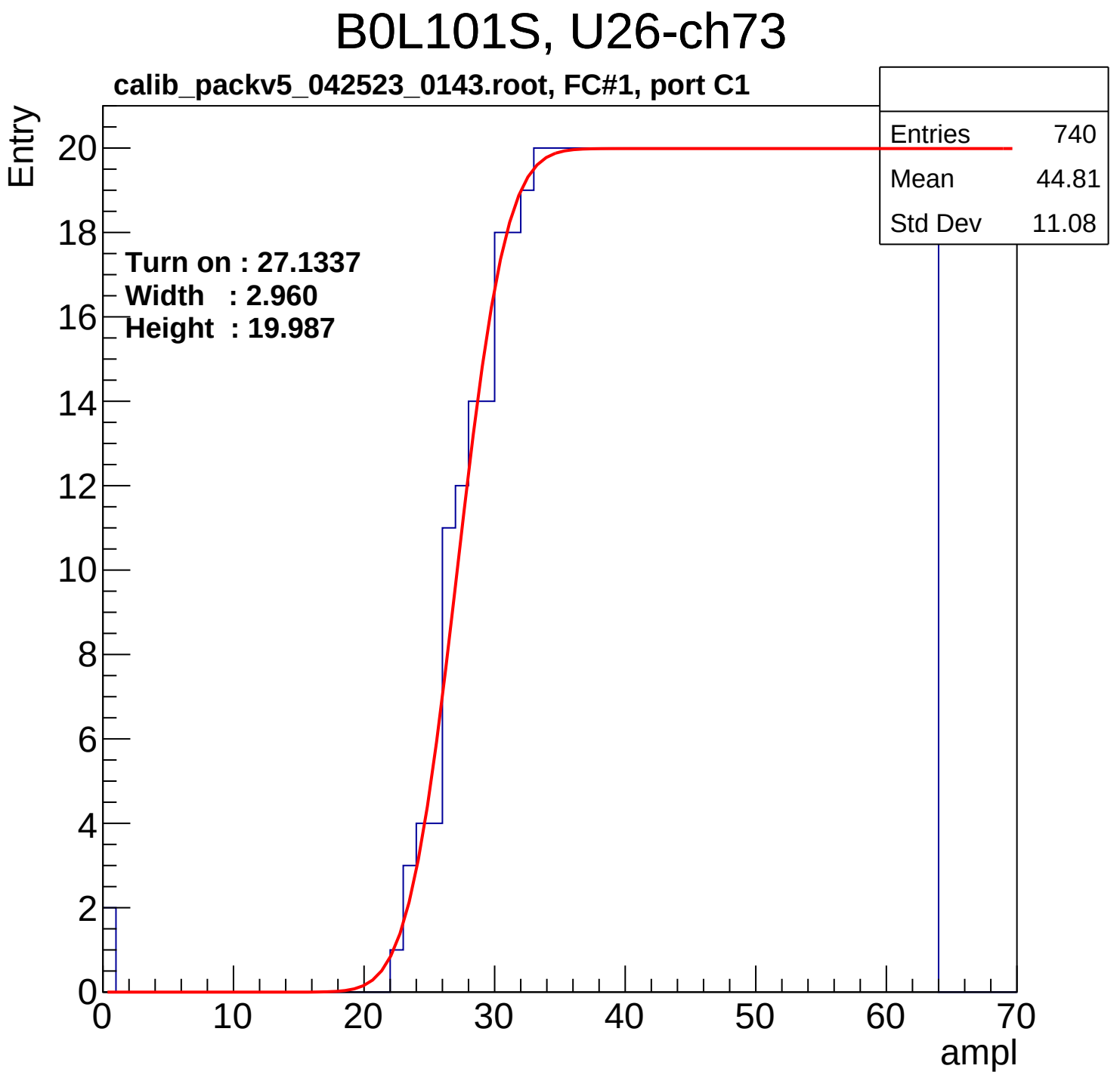
B0L101S, U26-ch73
calib_packv5_042523_0143.root, FC#1, port C1
Entries 740
Mean 44.81
Std Dev 11.08
Turn on : 27.1337
Width : 2.960
Height : 19.987
Entry
ampl
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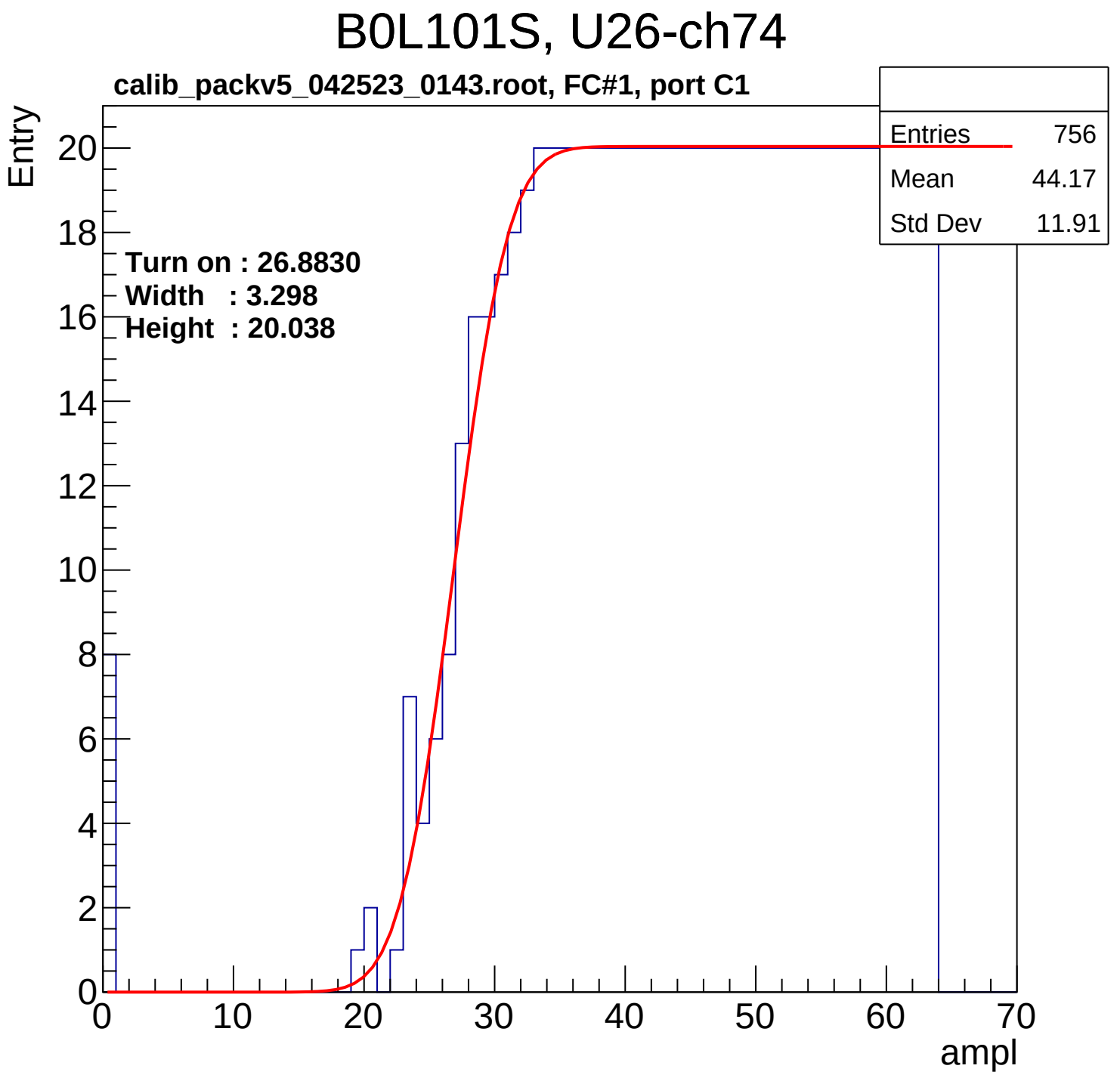
B0L101S, U26-ch74
calib_packv5_042523_0143.root, FC#1, port C1
Entries 756
Mean 44.17
Std Dev 11.91
Turn on : 26.8830
Width : 3.298
Height : 20.038
Entry
ampl
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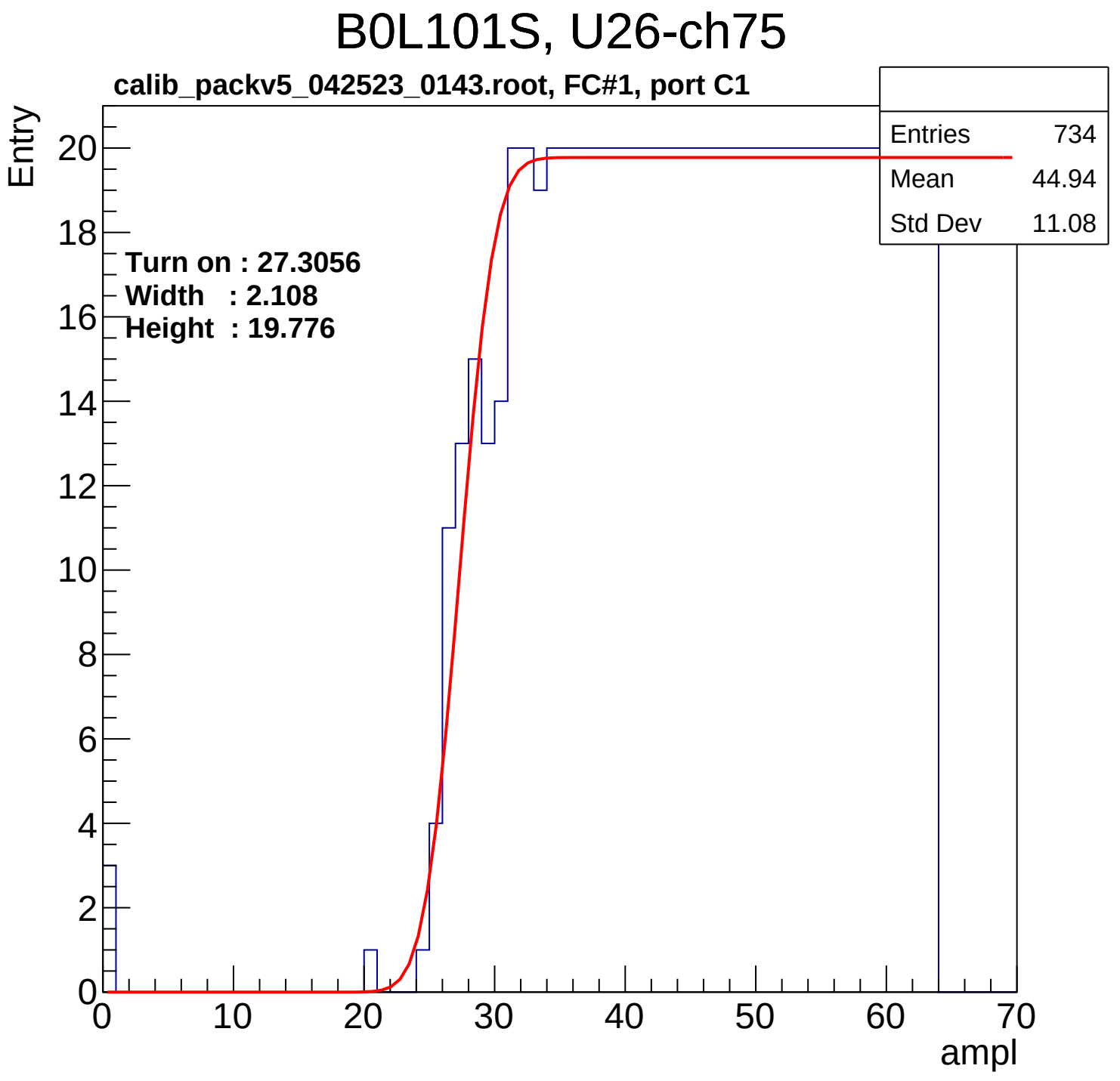
B0L101S, U26-ch75
calib_packv5_042523_0143.root, FC#1, port C1
Entries 734
Mean 44.94
Std Dev 11.08
Turn on : 27.3056
Width : 2.108
Height : 19.776
Entry
ampl
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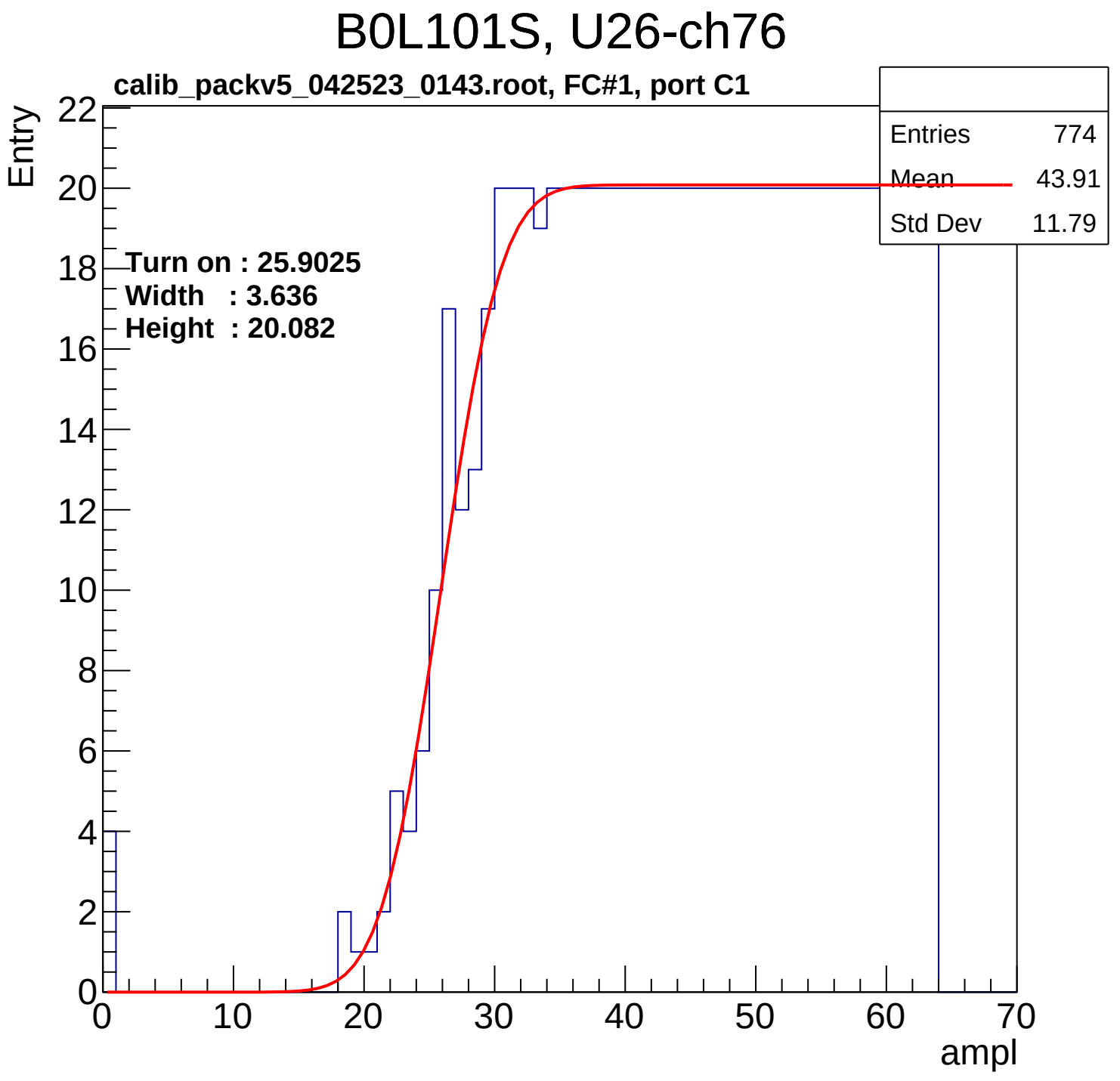
B0L101S, U26-ch76
calib_packv5_042523_0143.root, FC#1, port C1
Entries 774
Mean 43.91
Std Dev 11.79
Turn on : 25.9025
Width : 3.636
Height : 20.082
Entry
ampl
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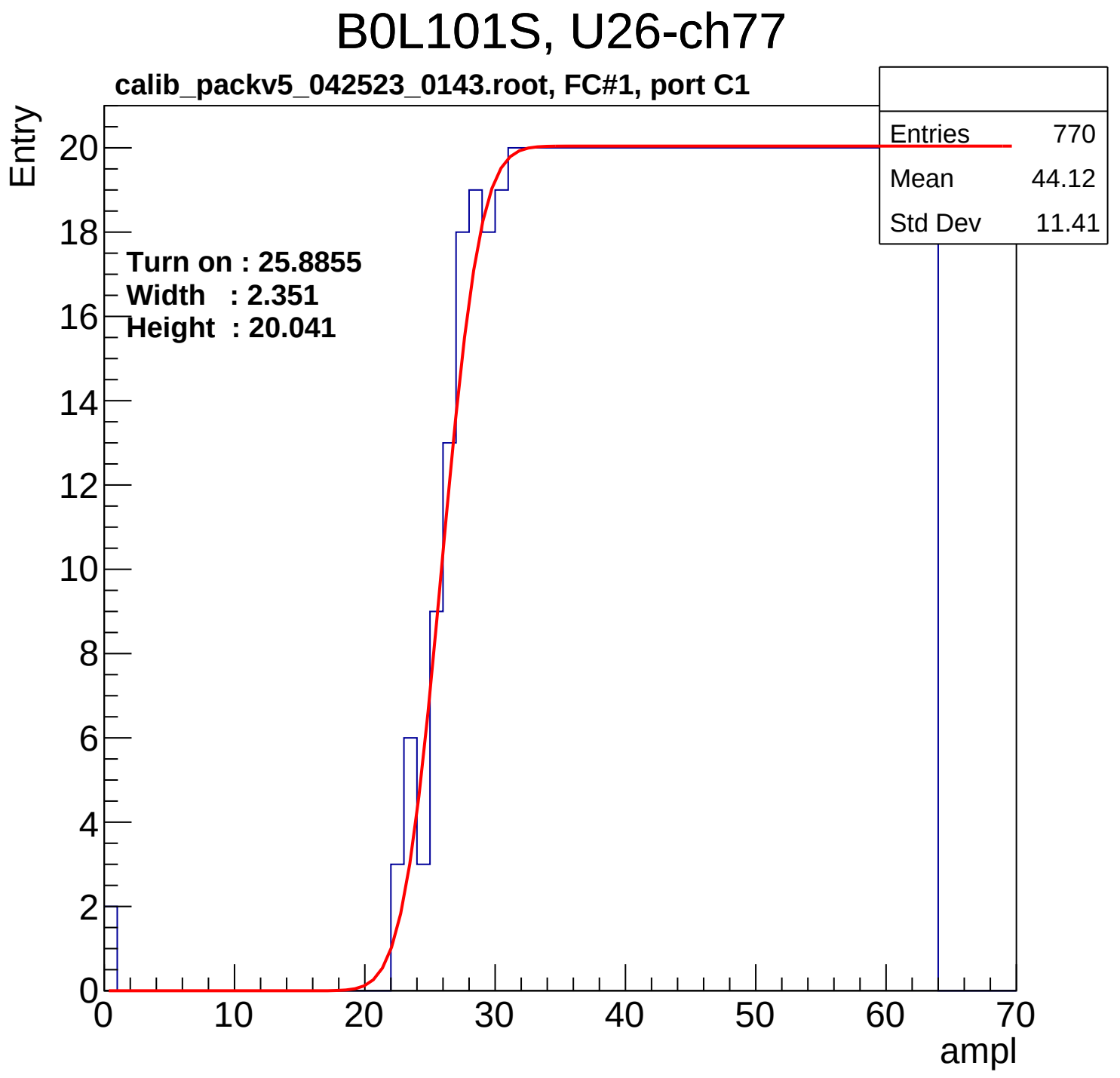
B0L101S, U26-ch77
calib_packv5_042523_0143.root, FC#1, port C1
Entries 770
Mean 44.12
Std Dev 11.41
Turn on : 25.8855
Width : 2.351
Height : 20.041
Entry
ampl
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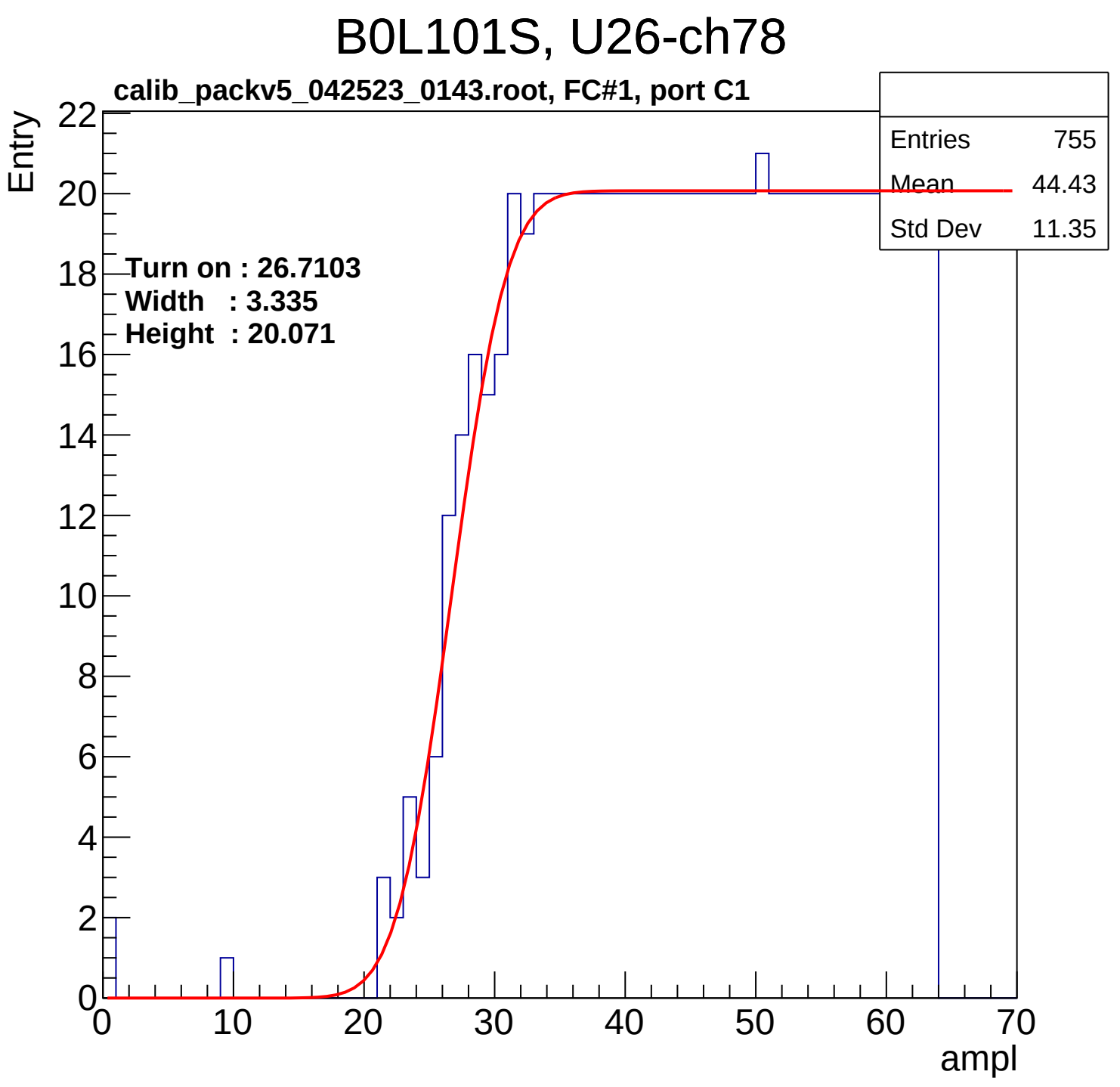
B0L101S, U26-ch78
calib_packv5_042523_0143.root, FC#1, port C1
Entries 755
Mean 44.43
Std Dev 11.35
Turn on : 26.7103
Width : 3.335
Height : 20.071
Entry
ampl
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8
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12
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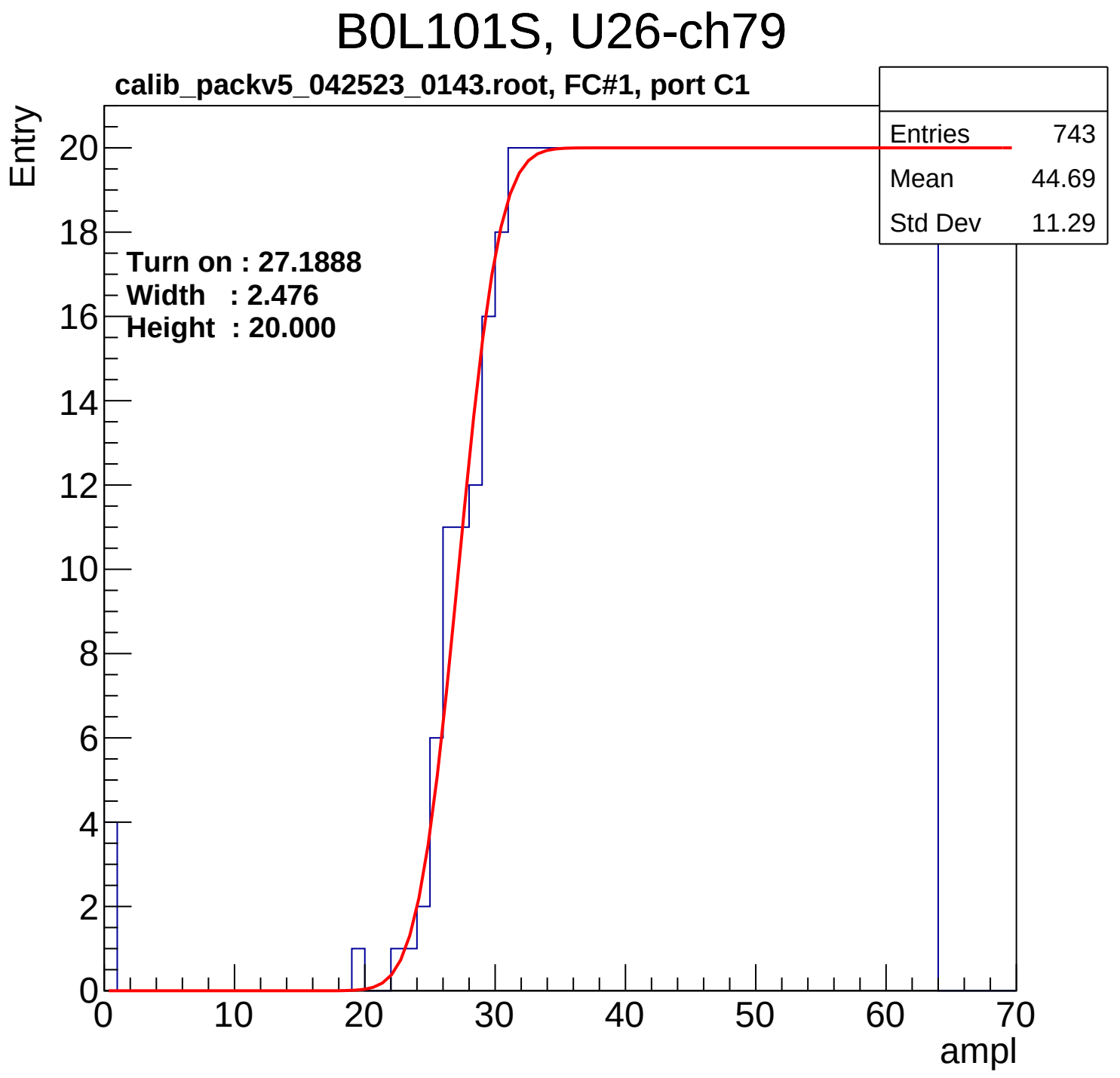
B0L101S, U26-ch79
calib_packv5_042523_0143.root, FC#1, port C1
Entries 743
Mean 44.69
Std Dev 11.29
Turn on : 27.1888
Width : 2.476
Height : 20.000
Entry
ampl
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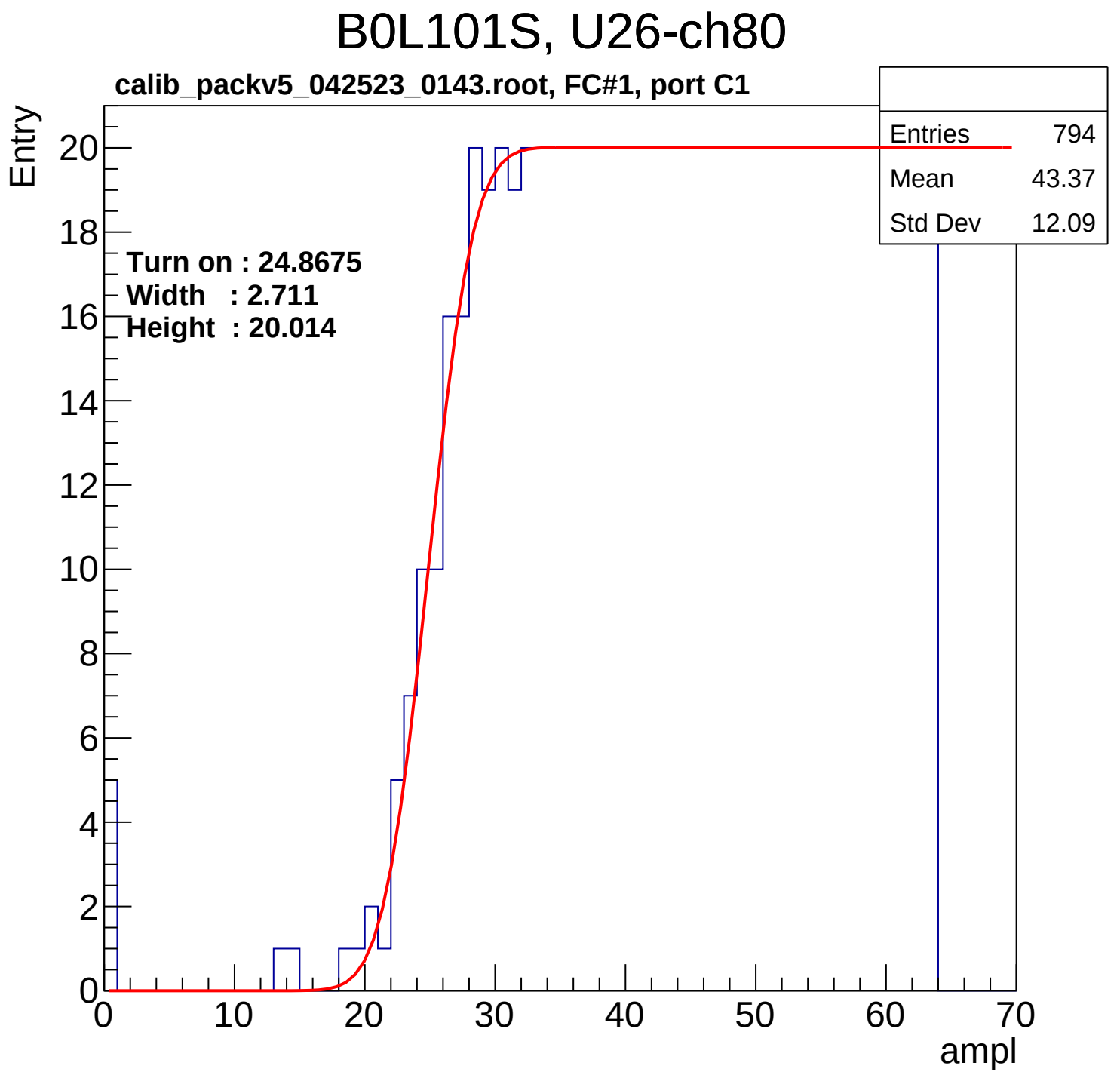
B0L101S, U26-ch80
calib_packv5_042523_0143.root, FC#1, port C1
Entries 794
Mean 43.37
Std Dev 12.09
Turn on : 24.8675
Width : 2.711
Height : 20.014
Entry
ampl
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14
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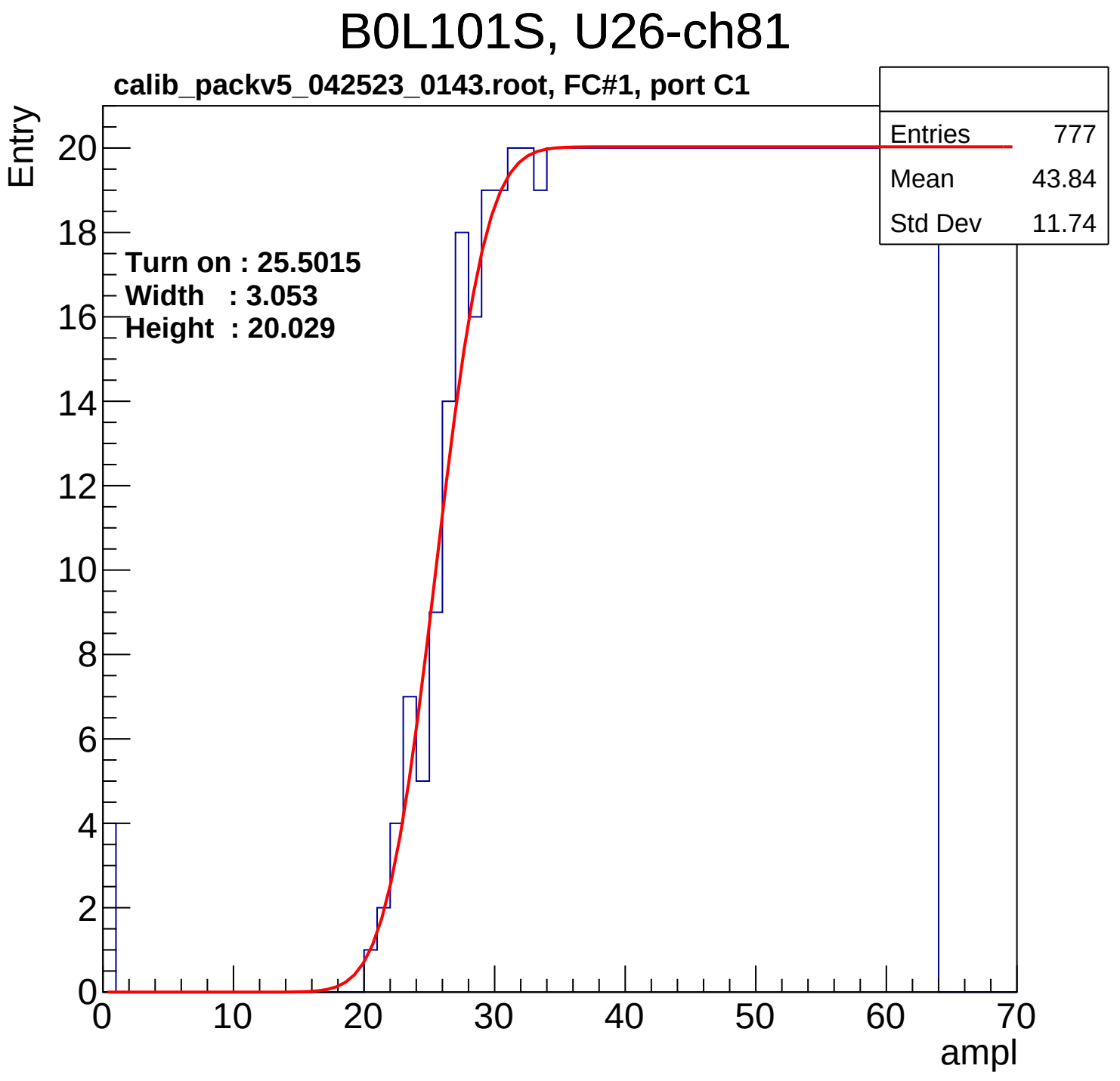
B0L101S, U26-ch81
calib_packv5_042523_0143.root, FC#1, port C1
Entries 777
Mean 43.84
Std Dev 11.74
Turn on : 25.5015
Width : 3.053
Height : 20.029
Entry
ampl
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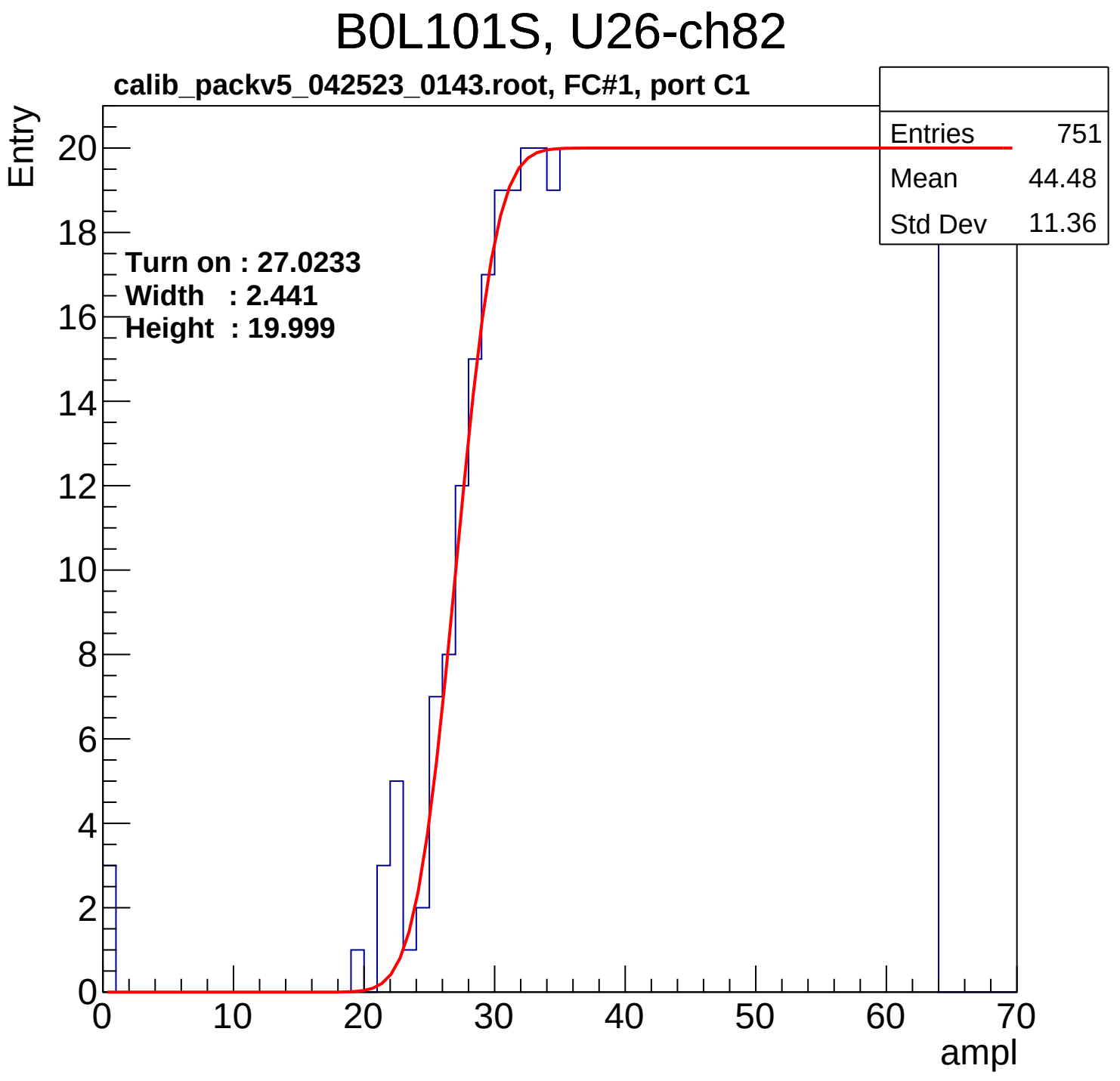
B0L101S, U26-ch82
calib_packv5_042523_0143.root, FC#1, port C1
Entries 751
Mean 44.48
Std Dev 11.36
Turn on : 27.0233
Width : 2.441
Height : 19.999
Entry
ampl
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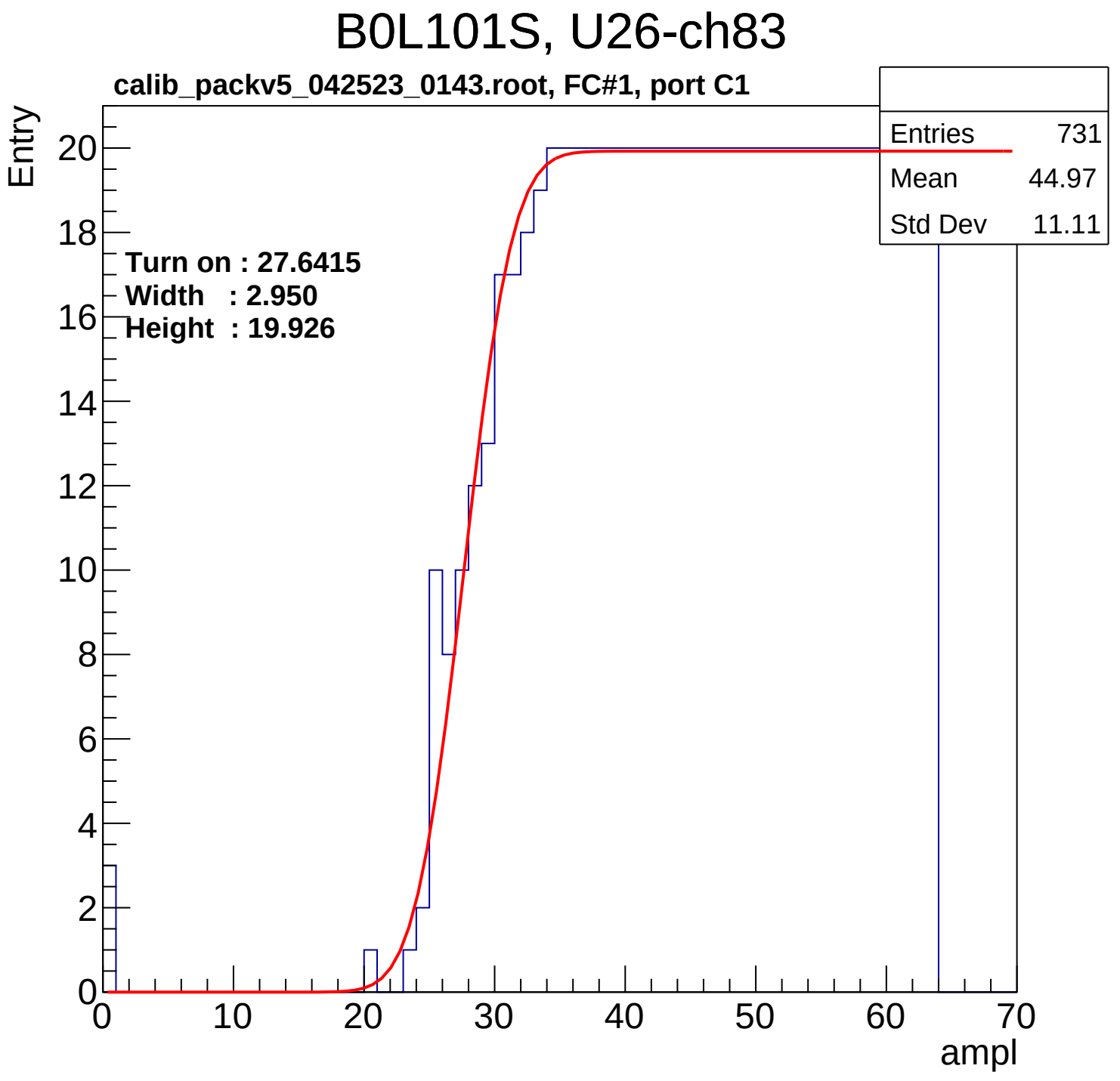
B0L101S, U26-ch83
calib_packv5_042523_0143.root, FC#1, port C1
Entries 731
Mean 44.97
Std Dev 11.11
Turn on : 27.6415
Width : 2.950
Height : 19.926
Entry
ampl
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6
8
10
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16
18
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0
10
20
30
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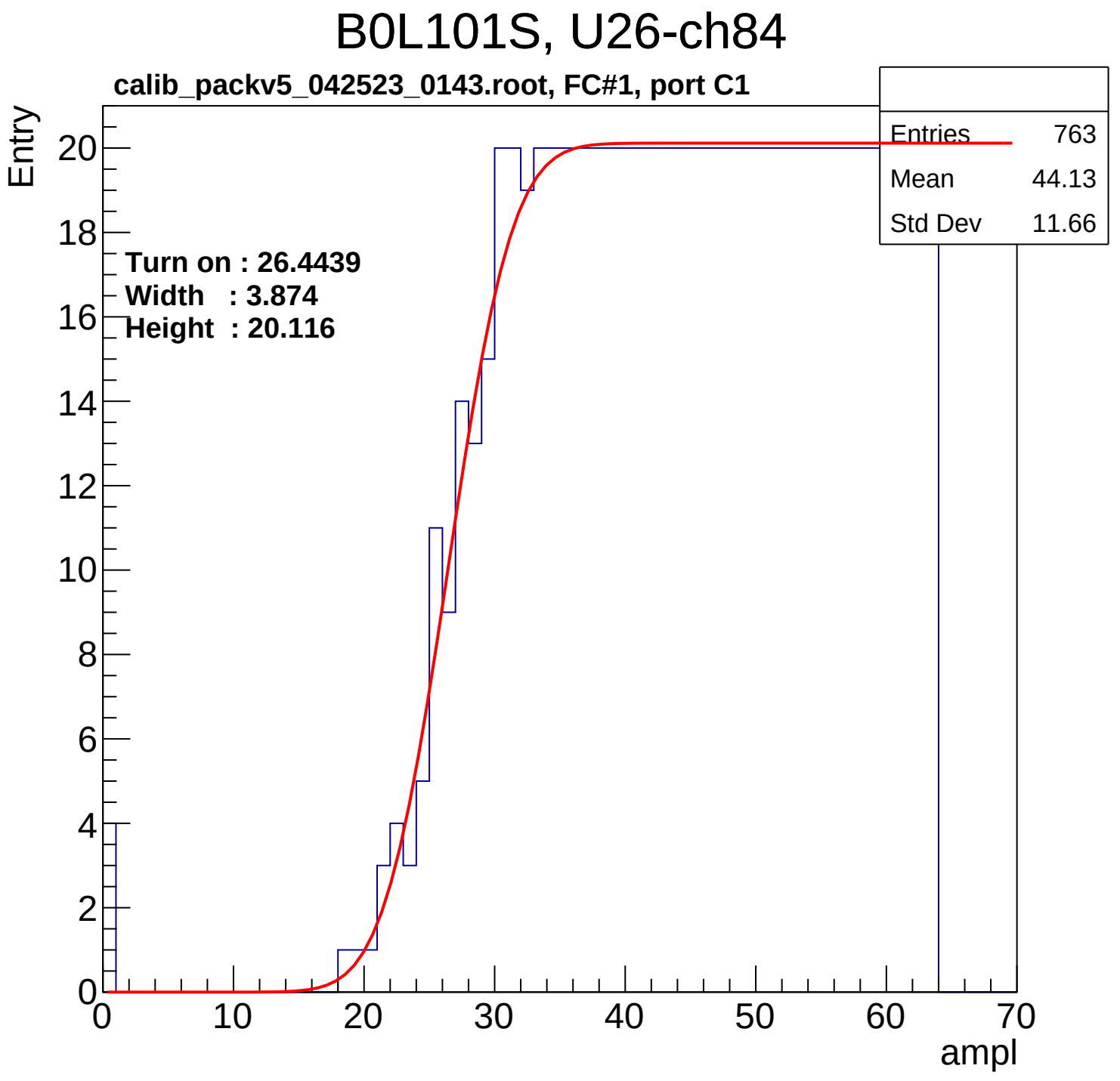
B0L101S, U26-ch84
calib_packv5_042523_0143.root, FC#1, port C1
Entries 763
Mean 44.13
Std Dev 11.66
Turn on : 26.4439
Width : 3.874
Height : 20.116
Entry
ampl
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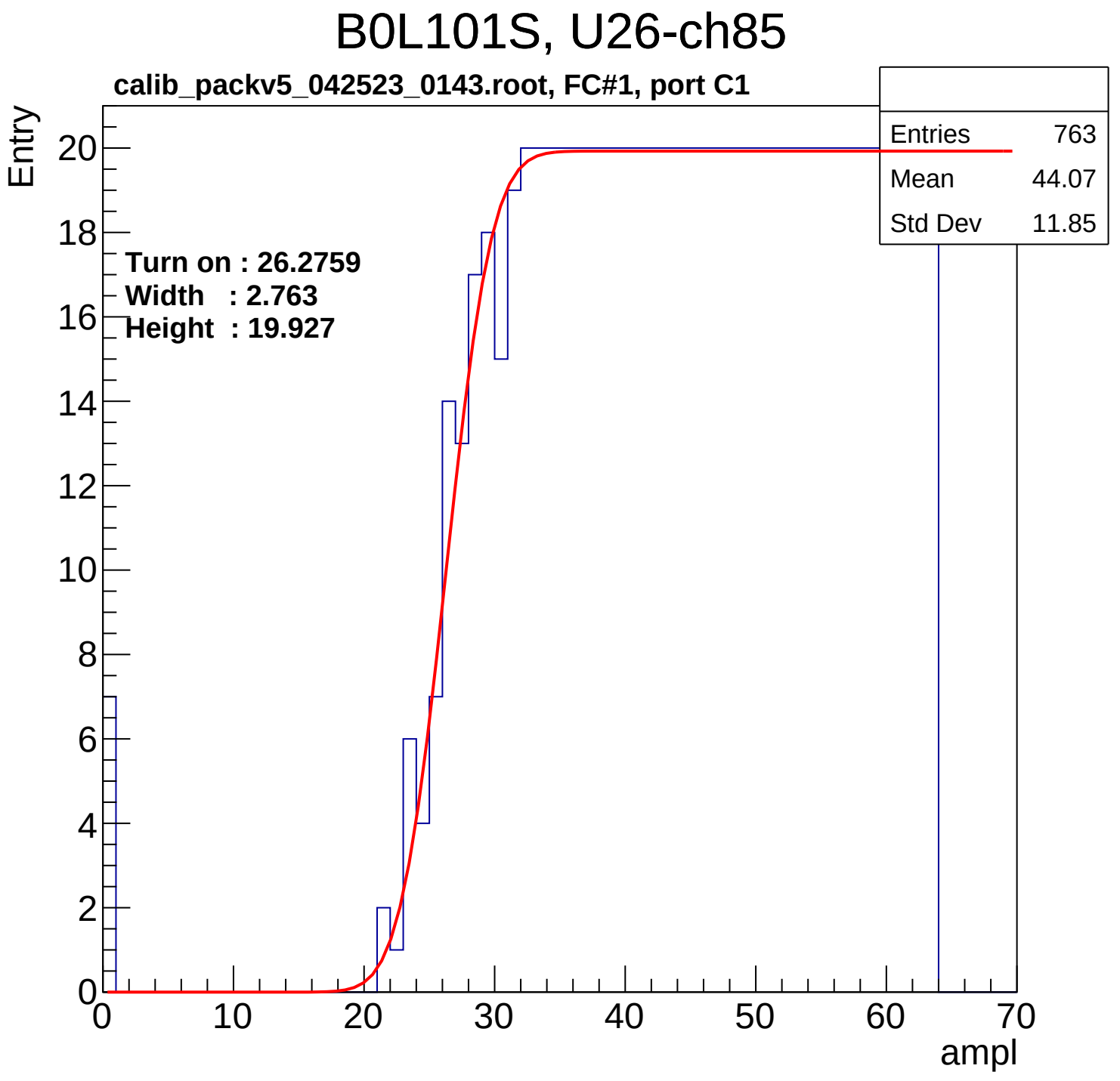
B0L101S, U26-ch85
calib_packv5_042523_0143.root, FC#1, port C1
Entries 763
Mean 44.07
Std Dev 11.85
Turn on : 26.2759
Width : 2.763
Height : 19.927
Entry
ampl
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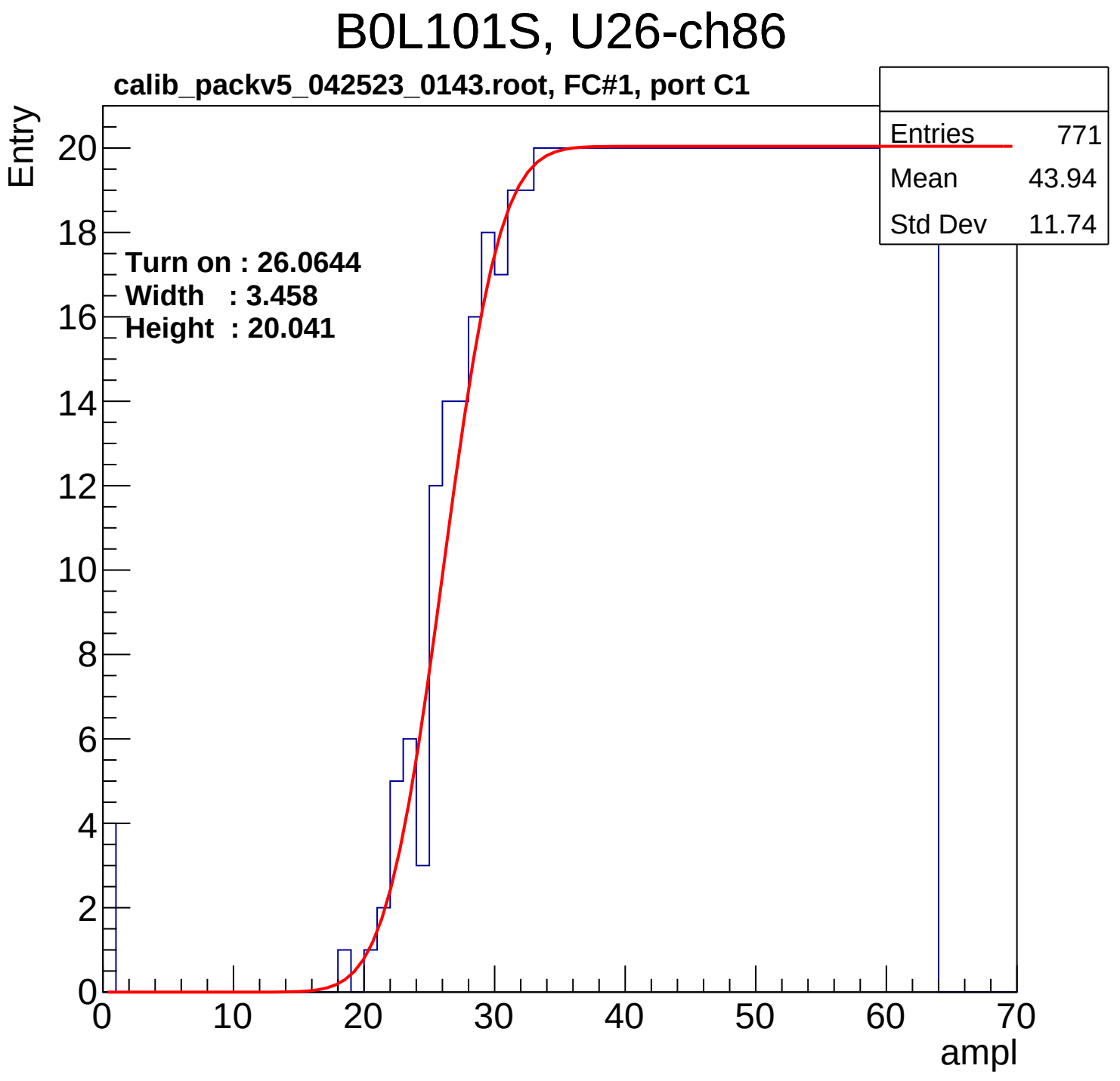
B0L101S, U26-ch86
calib_packv5_042523_0143.root, FC#1, port C1
Entries 771
Mean 43.94
Std Dev 11.74
Turn on : 26.0644
Width : 3.458
Height : 20.041
Entry
ampl
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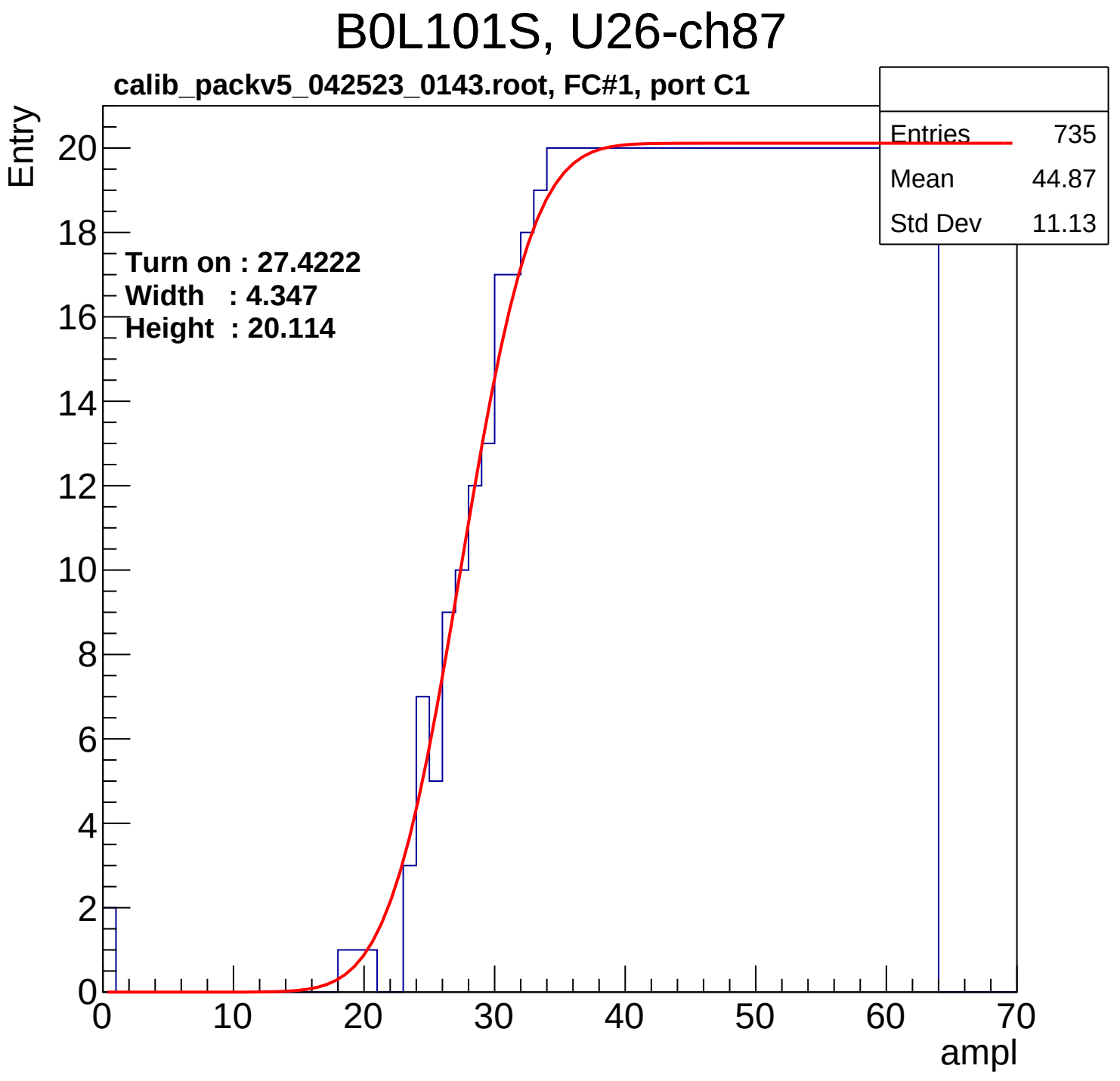
B0L101S, U26-ch87
calib_packv5_042523_0143.root, FC#1, port C1
Entries 735
Mean 44.87
Std Dev 11.13
Turn on : 27.4222
Width : 4.347
Height : 20.114
Entry
ampl
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6
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10
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14
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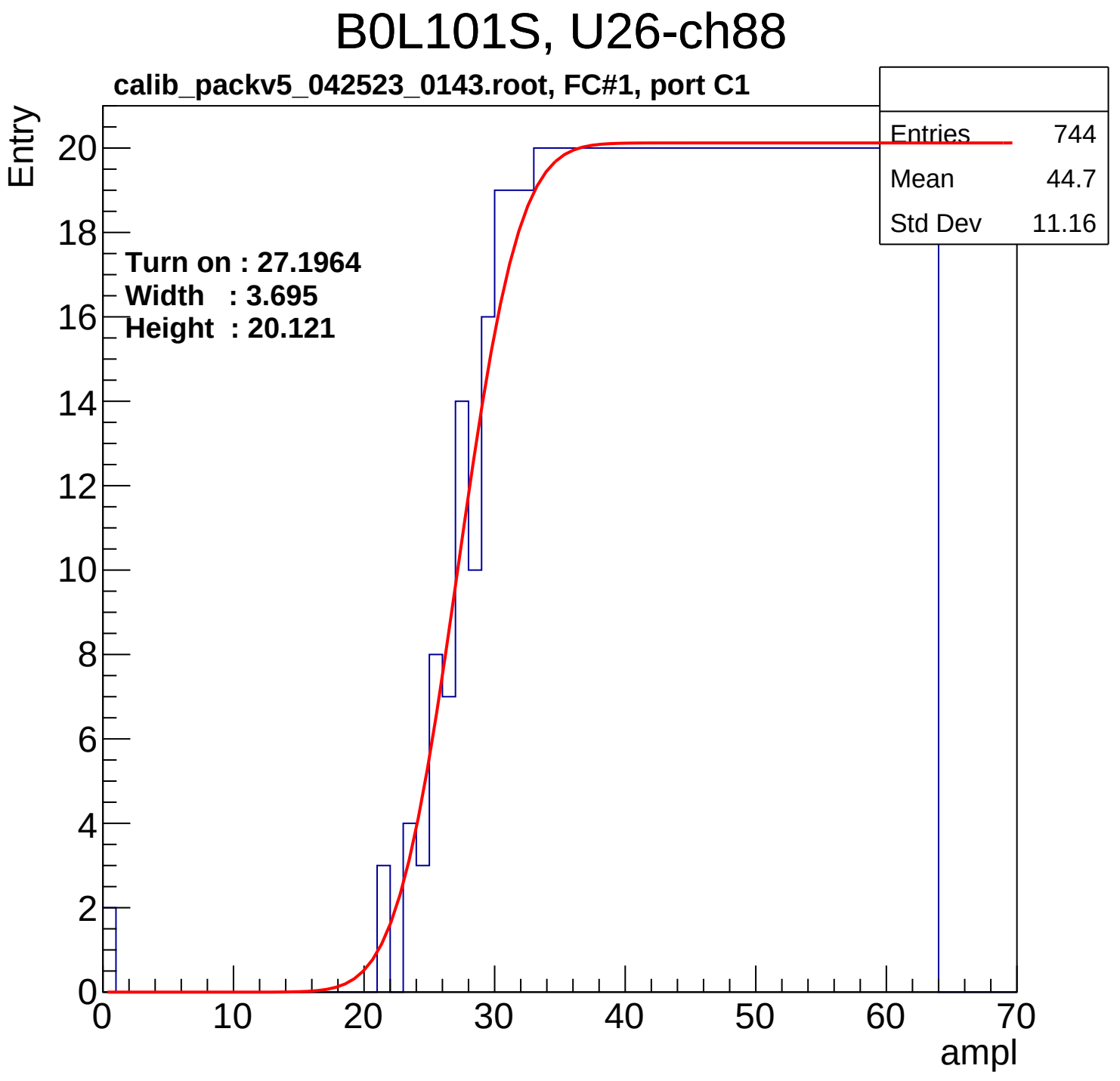
B0L101S, U26-ch88
calib_packv5_042523_0143.root, FC#1, port C1
Entries 744
Mean 44.7
Std Dev 11.16
Turn on : 27.1964
Width : 3.695
Height : 20.121
Entry
ampl
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6
8
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14
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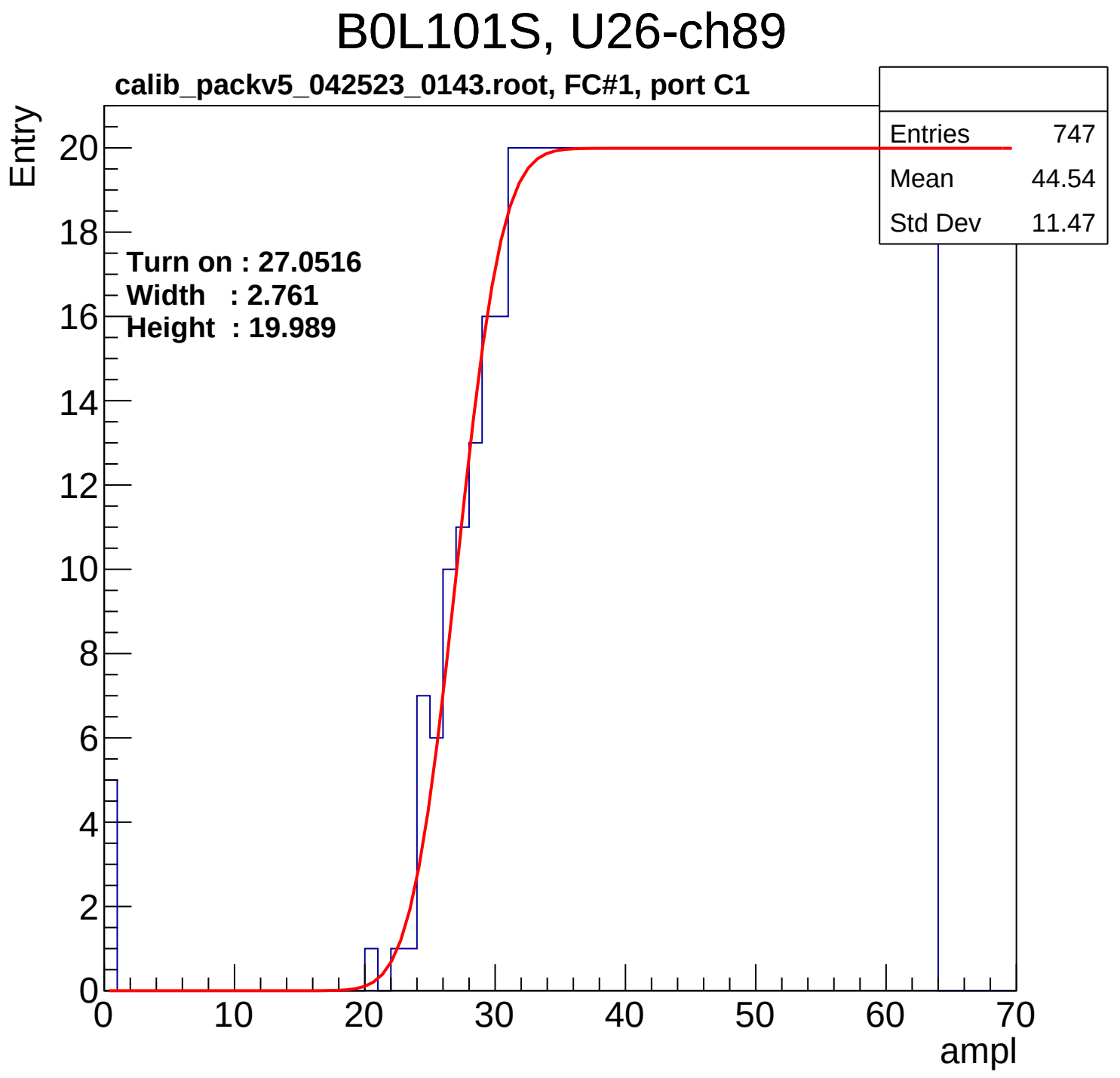
B0L101S, U26-ch89
calib_packv5_042523_0143.root, FC#1, port C1
Entries 747
Mean 44.54
Std Dev 11.47
Turn on : 27.0516
Width : 2.761
Height : 19.989
Entry
ampl
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6
8
10
12
14
16
18
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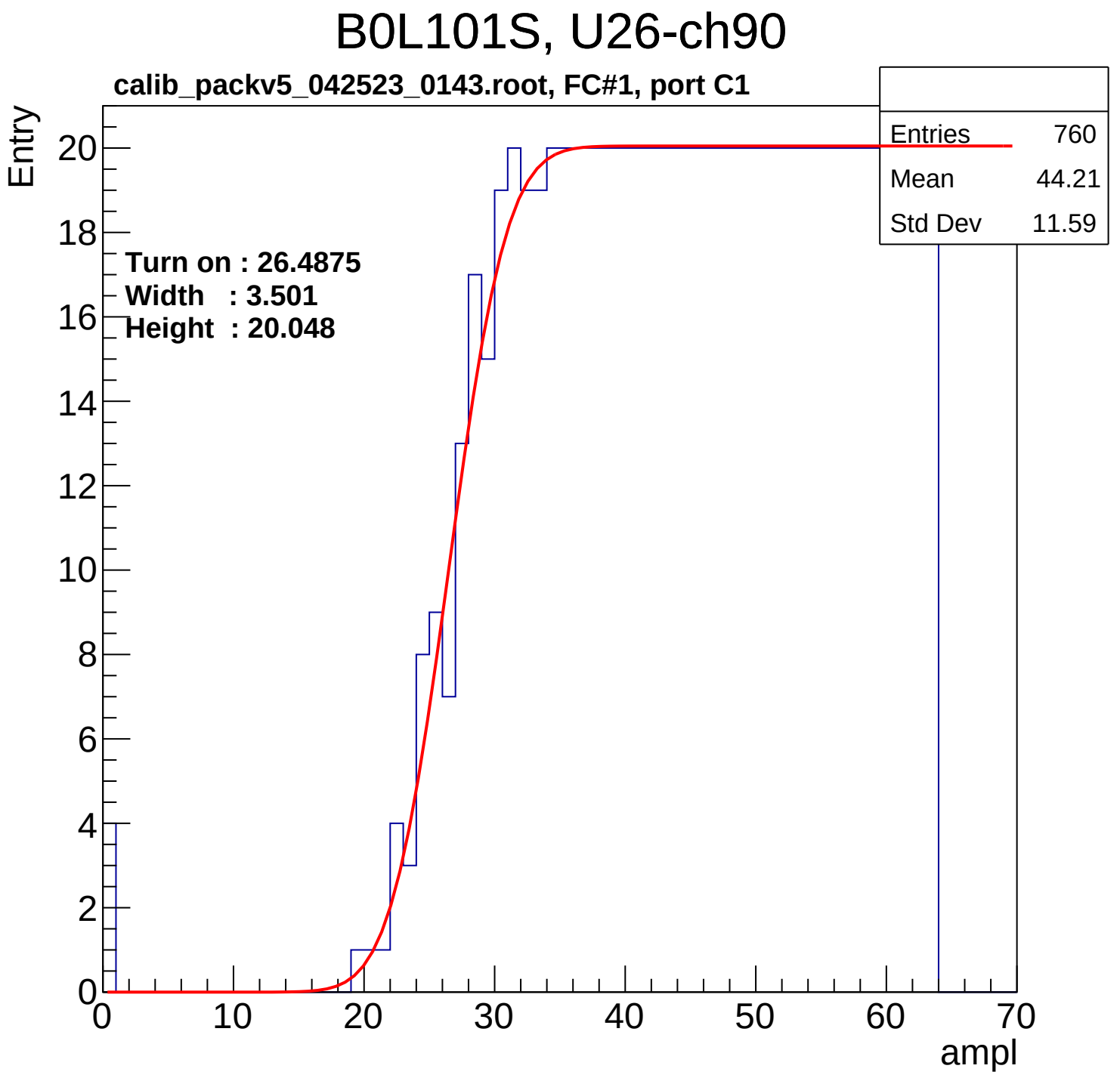
B0L101S, U26-ch90
calib_packv5_042523_0143.root, FC#1, port C1
Entries 760
Mean 44.21
Std Dev 11.59
Turn on : 26.4875
Width : 3.501
Height : 20.048
Entry
ampl
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8
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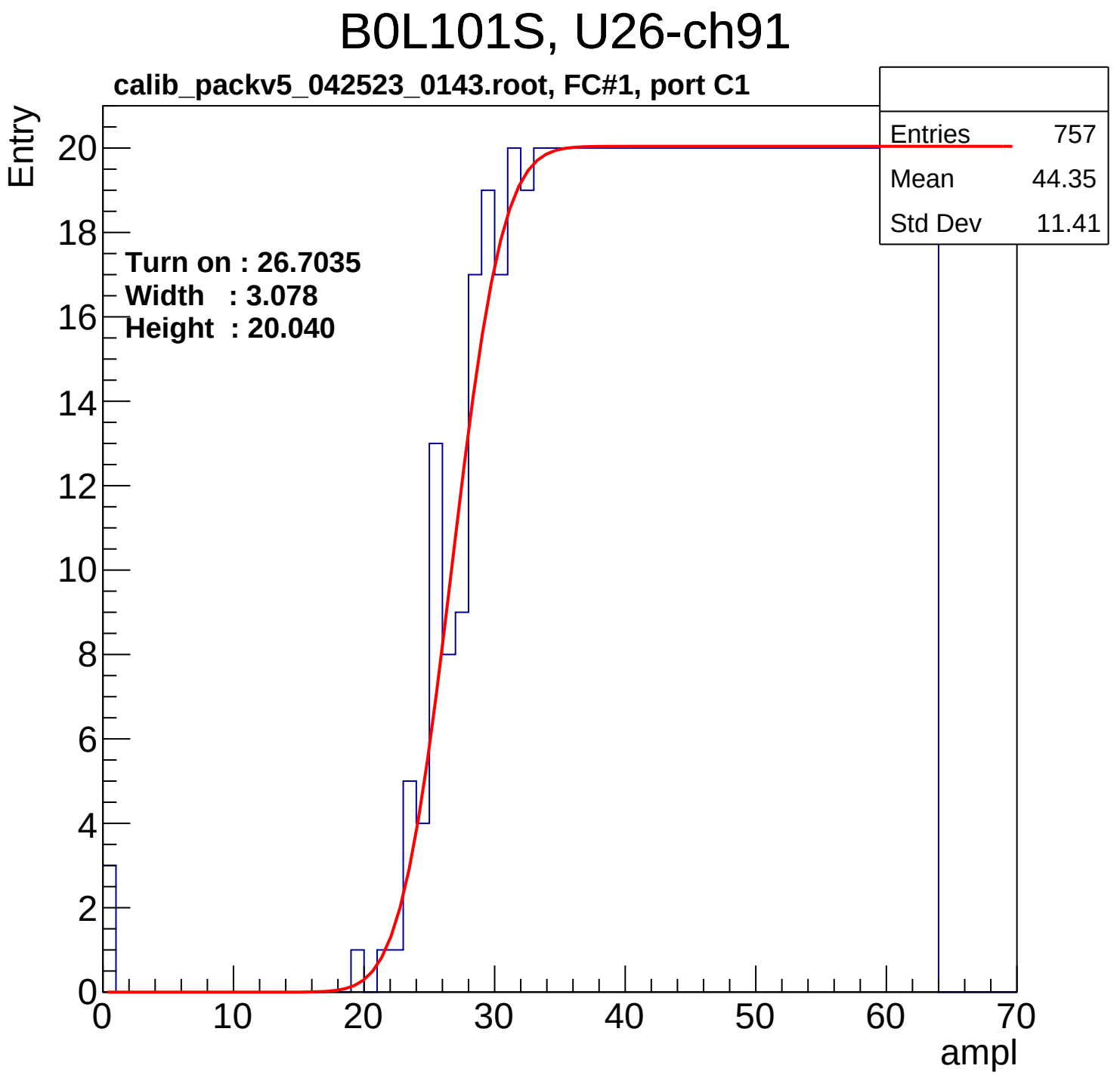
B0L101S, U26-ch91
calib_packv5_042523_0143.root, FC#1, port C1
Entries 757
Mean 44.35
Std Dev 11.41
Turn on : 26.7035
Width : 3.078
Height : 20.040
Entry
ampl
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6
8
10
12
14
16
18
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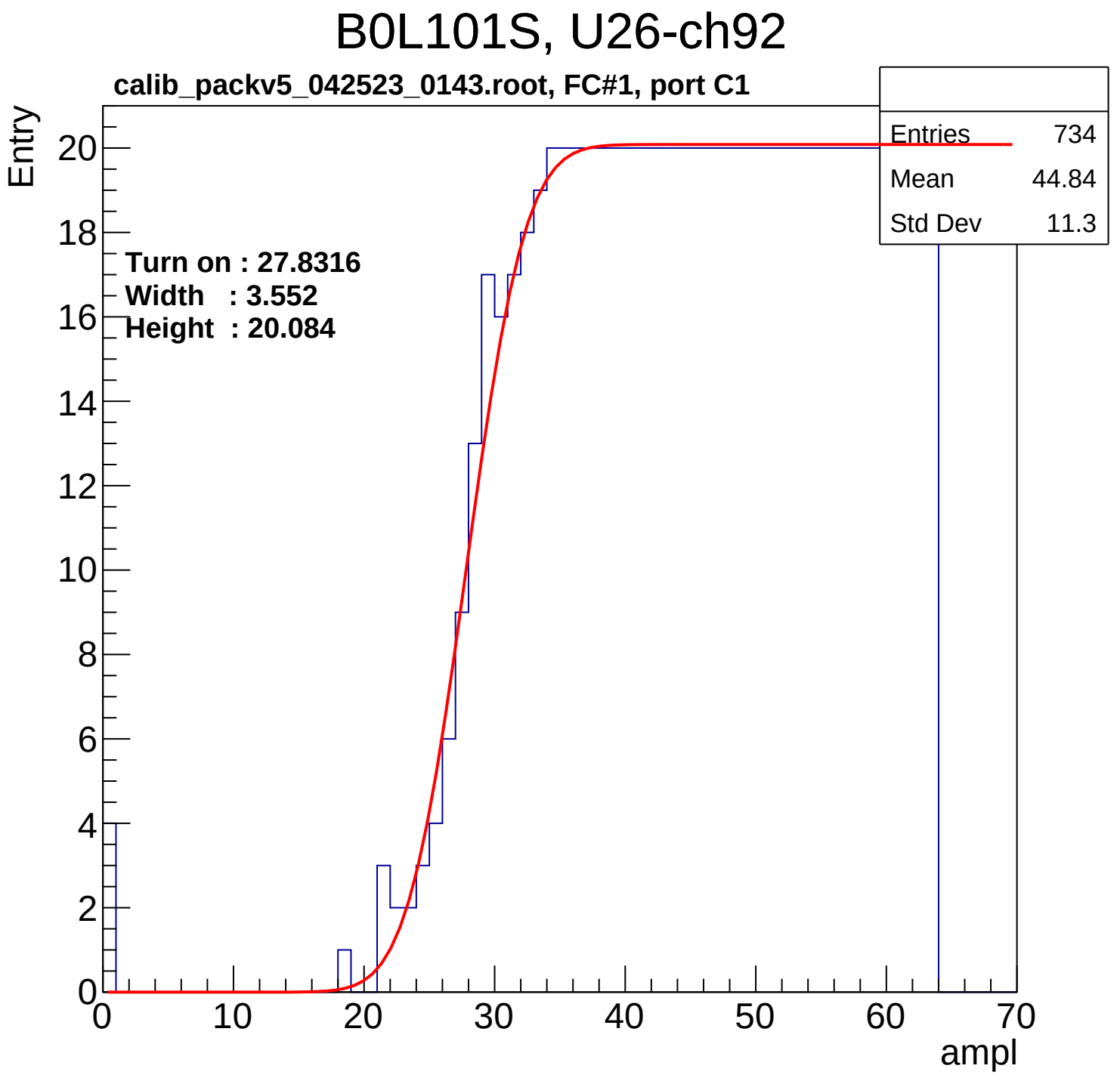
B0L101S, U26-ch92
calib_packv5_042523_0143.root, FC#1, port C1
Entries 734
Mean 44.84
Std Dev 11.3
Turn on : 27.8316
Width : 3.552
Height : 20.084
Entry
ampl
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6
8
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12
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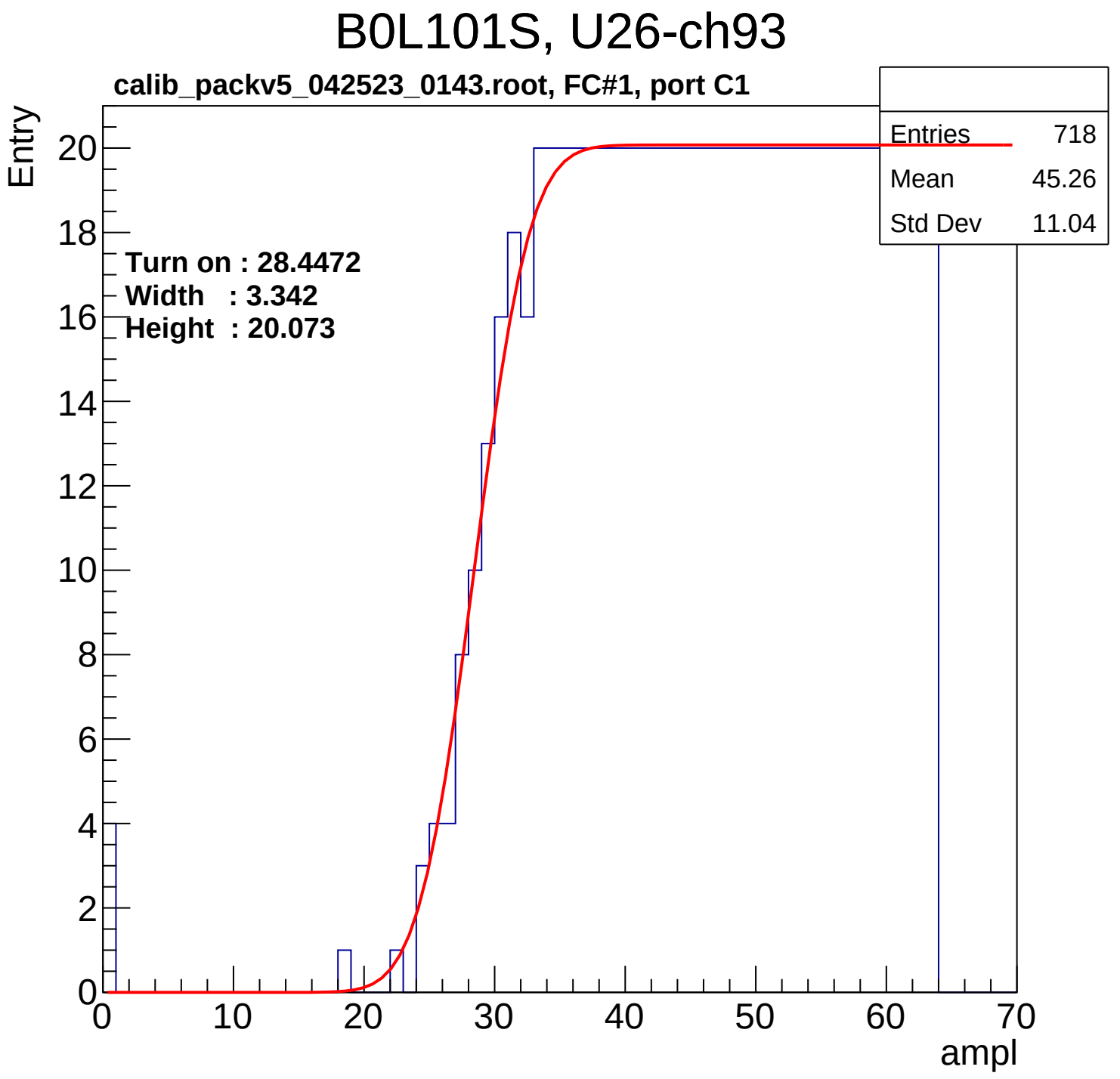
B0L101S, U26-ch93
calib_packv5_042523_0143.root, FC#1, port C1
Entries 718
Mean 45.26
Std Dev 11.04
Turn on : 28.4472
Width : 3.342
Height : 20.073
Entry
ampl
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8
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14
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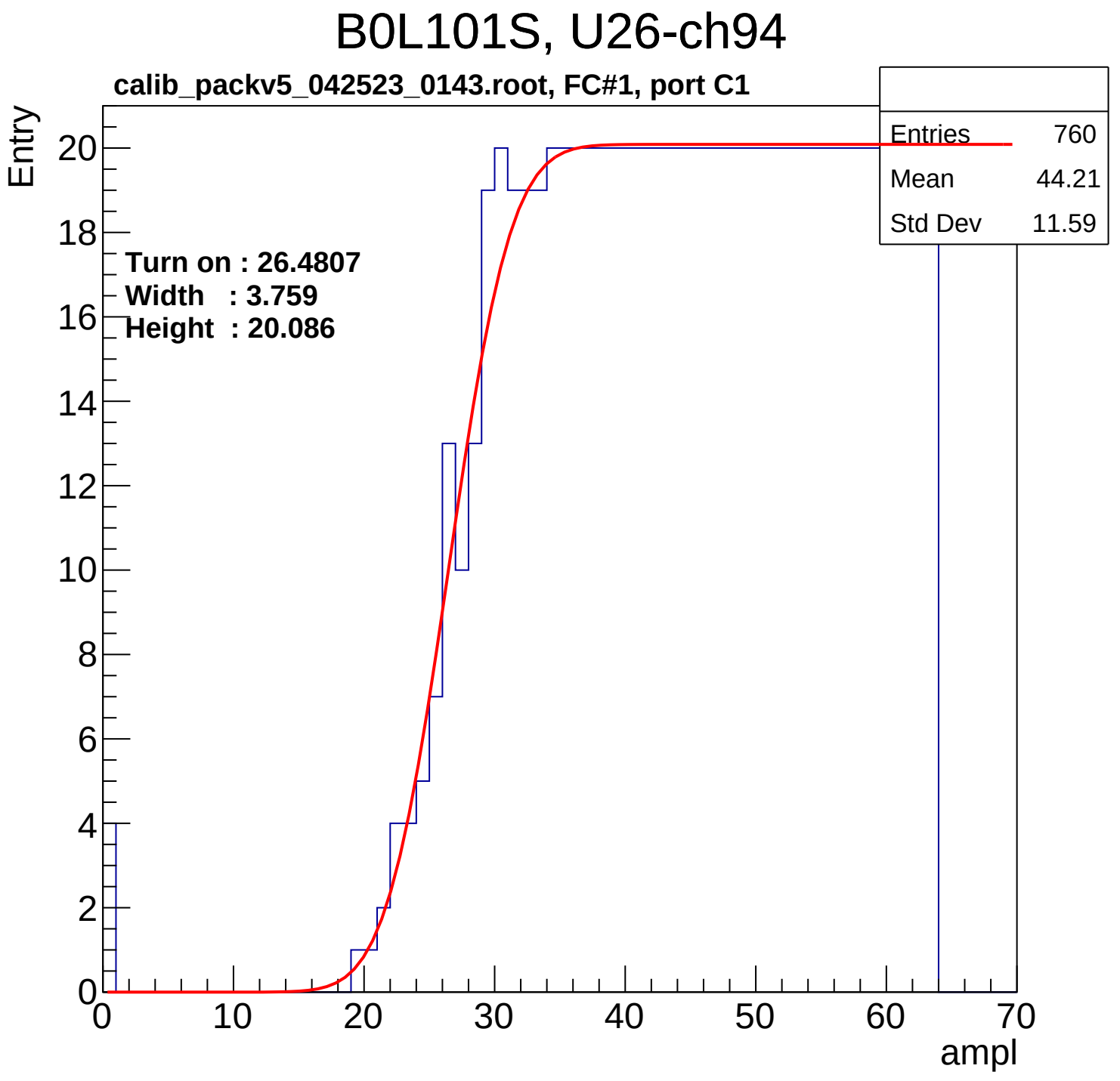
B0L101S, U26-ch94
calib_packv5_042523_0143.root, FC#1, port C1
Entries 760
Mean 44.21
Std Dev 11.59
Turn on : 26.4807
Width : 3.759
Height : 20.086
Entry
ampl
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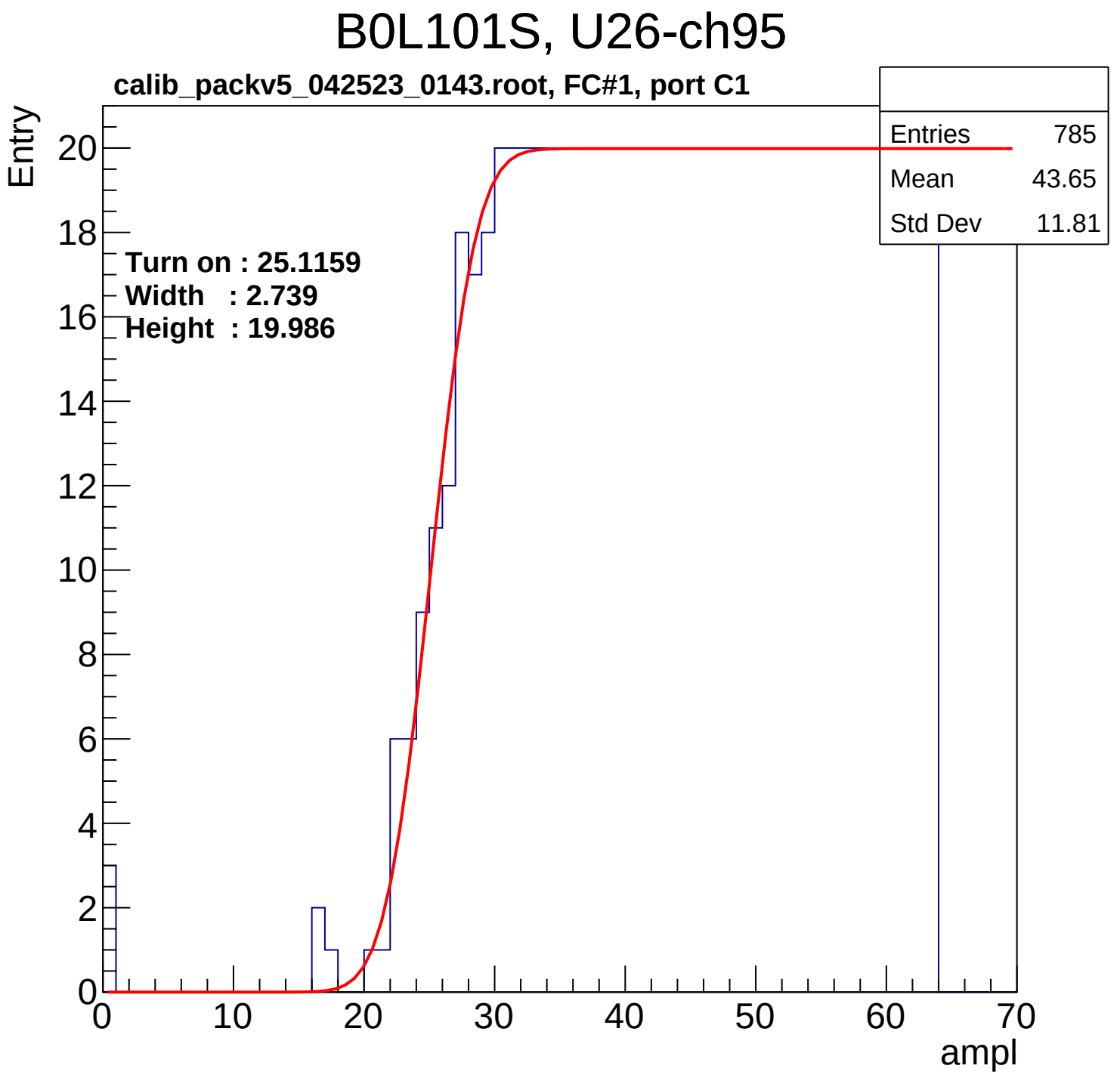
B0L101S, U26-ch95
calib_packv5_042523_0143.root, FC#1, port C1
Entries 785
Mean 43.65
Std Dev 11.81
Turn on : 25.1159
Width : 2.739
Height : 19.986
Entry
ampl
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6
8
10
12
14
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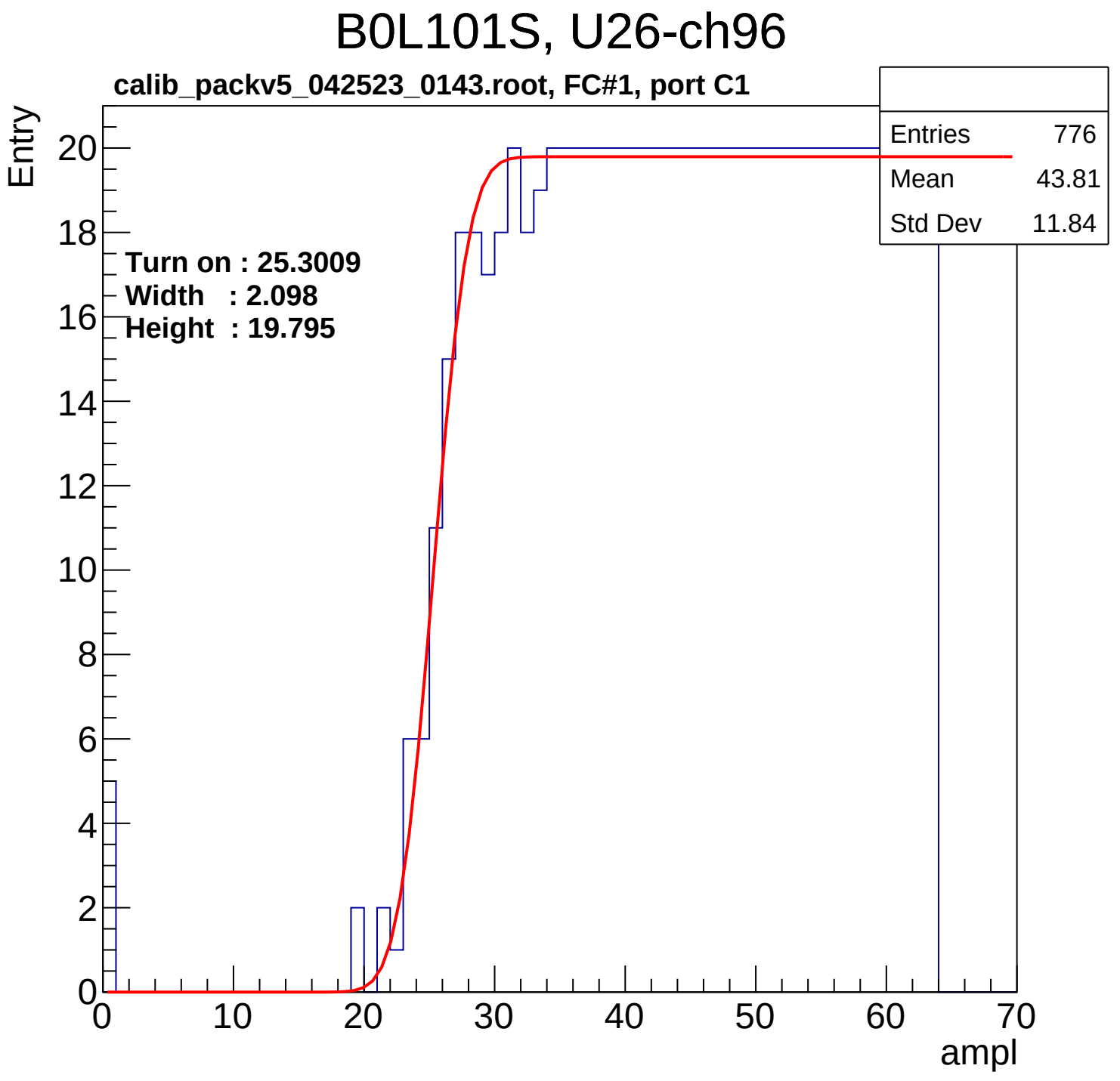
B0L101S, U26-ch96
calib_packv5_042523_0143.root, FC#1, port C1
Entries 776
Mean 43.81
Std Dev 11.84
Turn on : 25.3009
Width : 2.098
Height : 19.795
Entry
ampl
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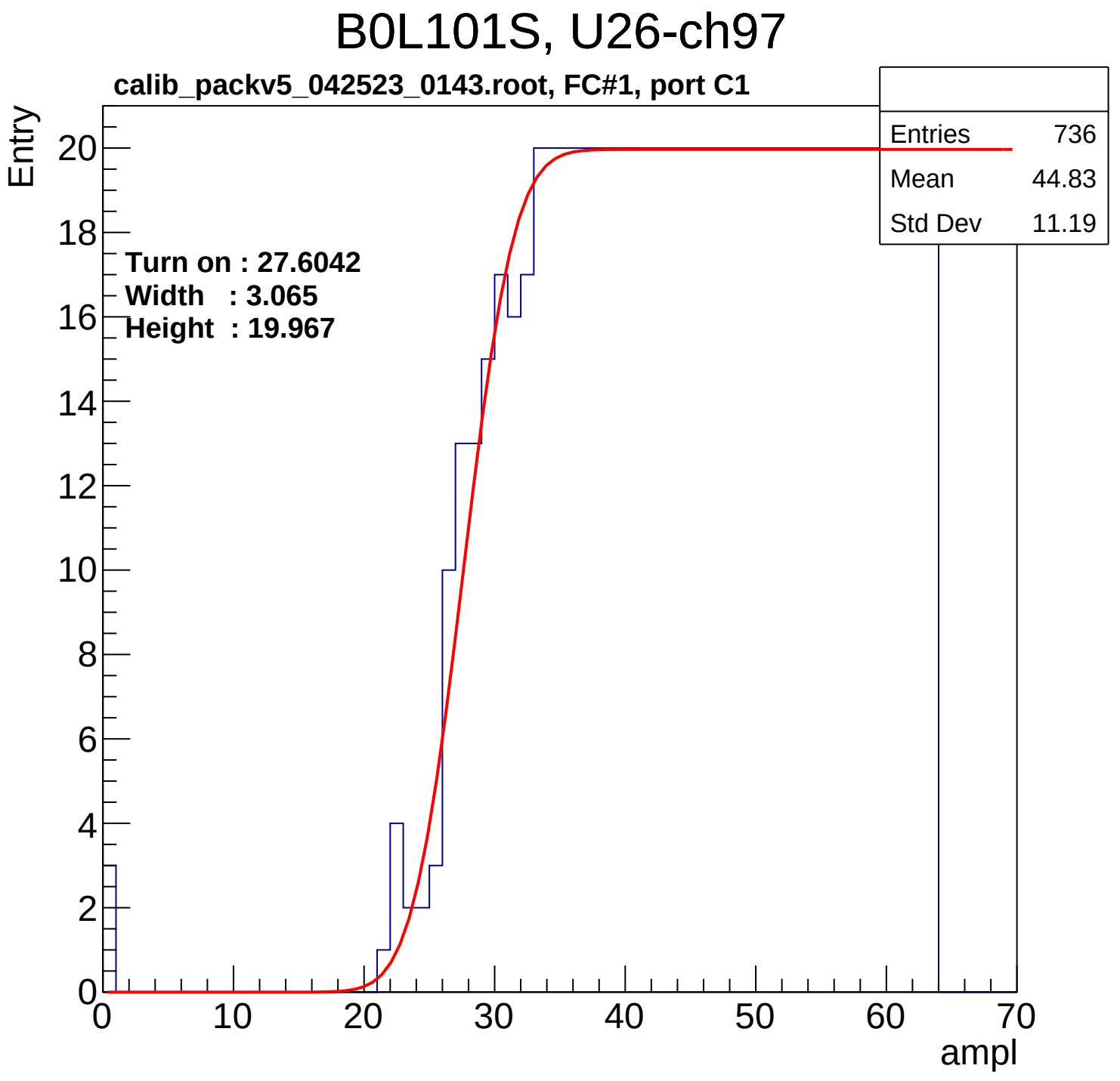
B0L101S, U26-ch97
calib_packv5_042523_0143.root, FC#1, port C1
Entries 736
Mean 44.83
Std Dev 11.19
Turn on : 27.6042
Width : 3.065
Height : 19.967
Entry
ampl
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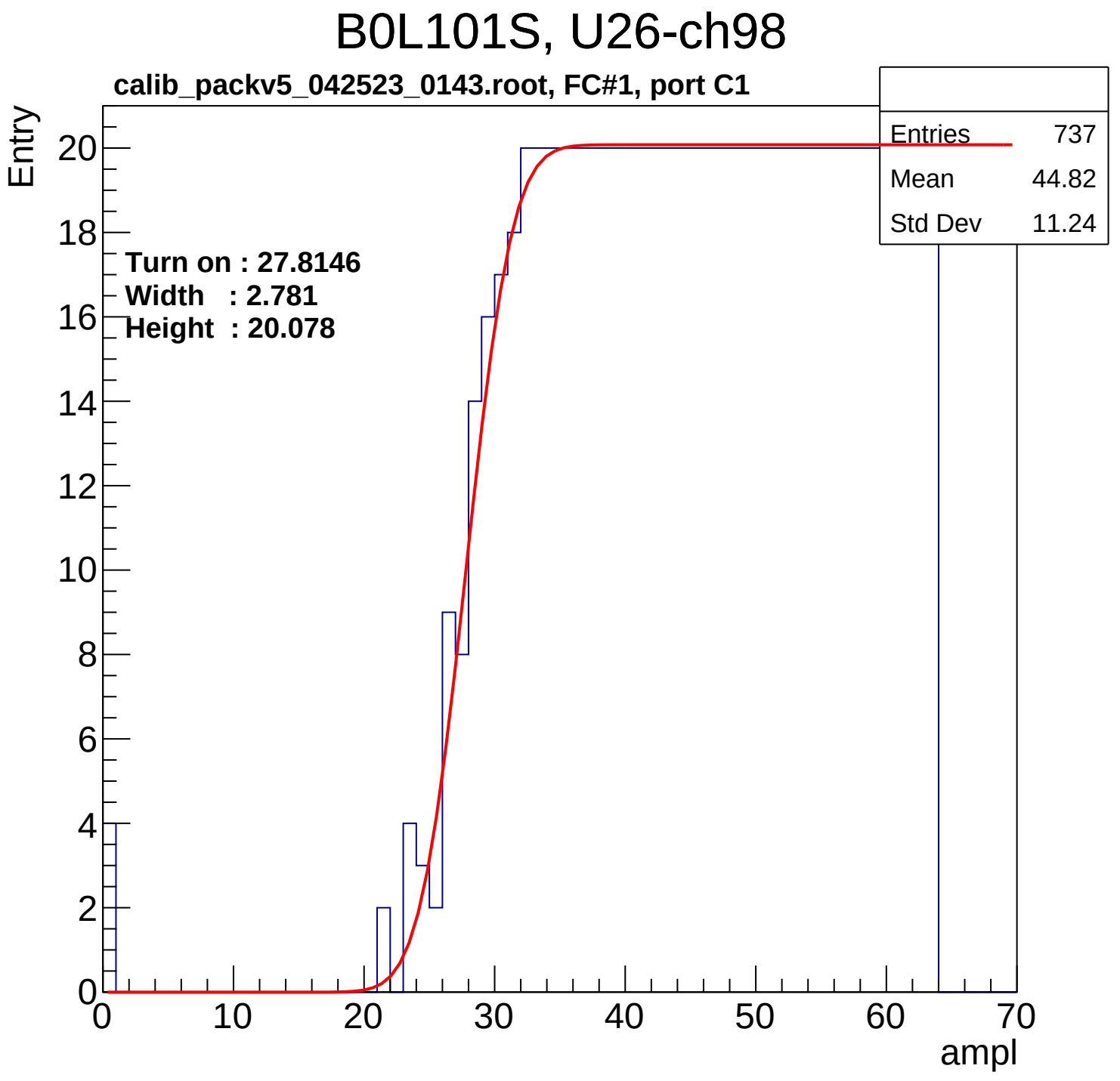
B0L101S, U26-ch98
calib_packv5_042523_0143.root, FC#1, port C1
Entries 737
Mean 44.82
Std Dev 11.24
Turn on : 27.8146
Width : 2.781
Height : 20.078
Entry
ampl
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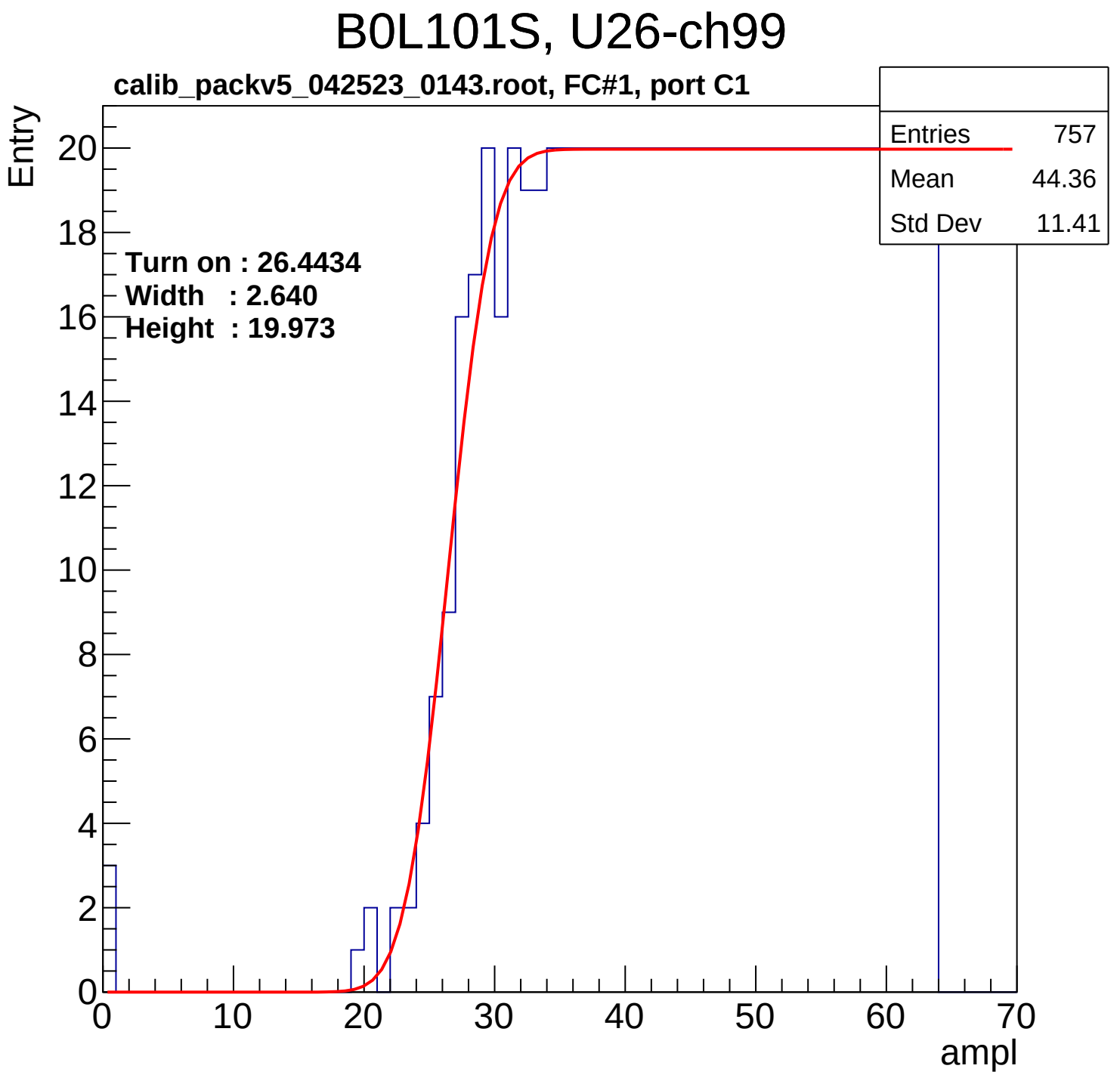
B0L101S, U26-ch99
calib_packv5_042523_0143.root, FC#1, port C1
Entries 757
Mean 44.36
Std Dev 11.41
Turn on : 26.4434
Width : 2.640
Height : 19.973
Entry
ampl
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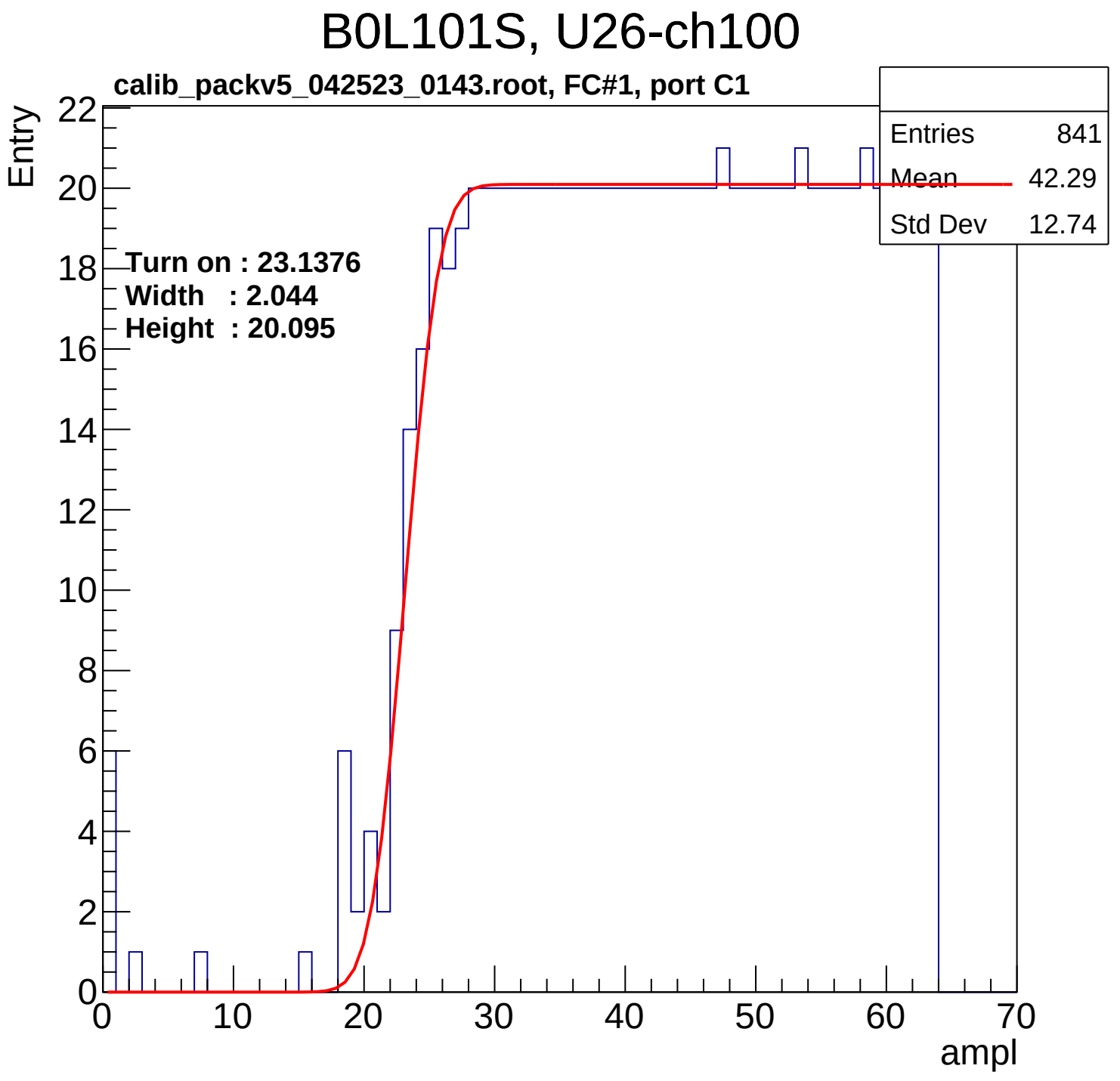
B0L101S, U26-ch100
calib_packv5_042523_0143.root, FC#1, port C1
Entries 841
Mean 42.29
Std Dev 12.74
Turn on : 23.1376
Width : 2.044
Height : 20.095
Entry
ampl
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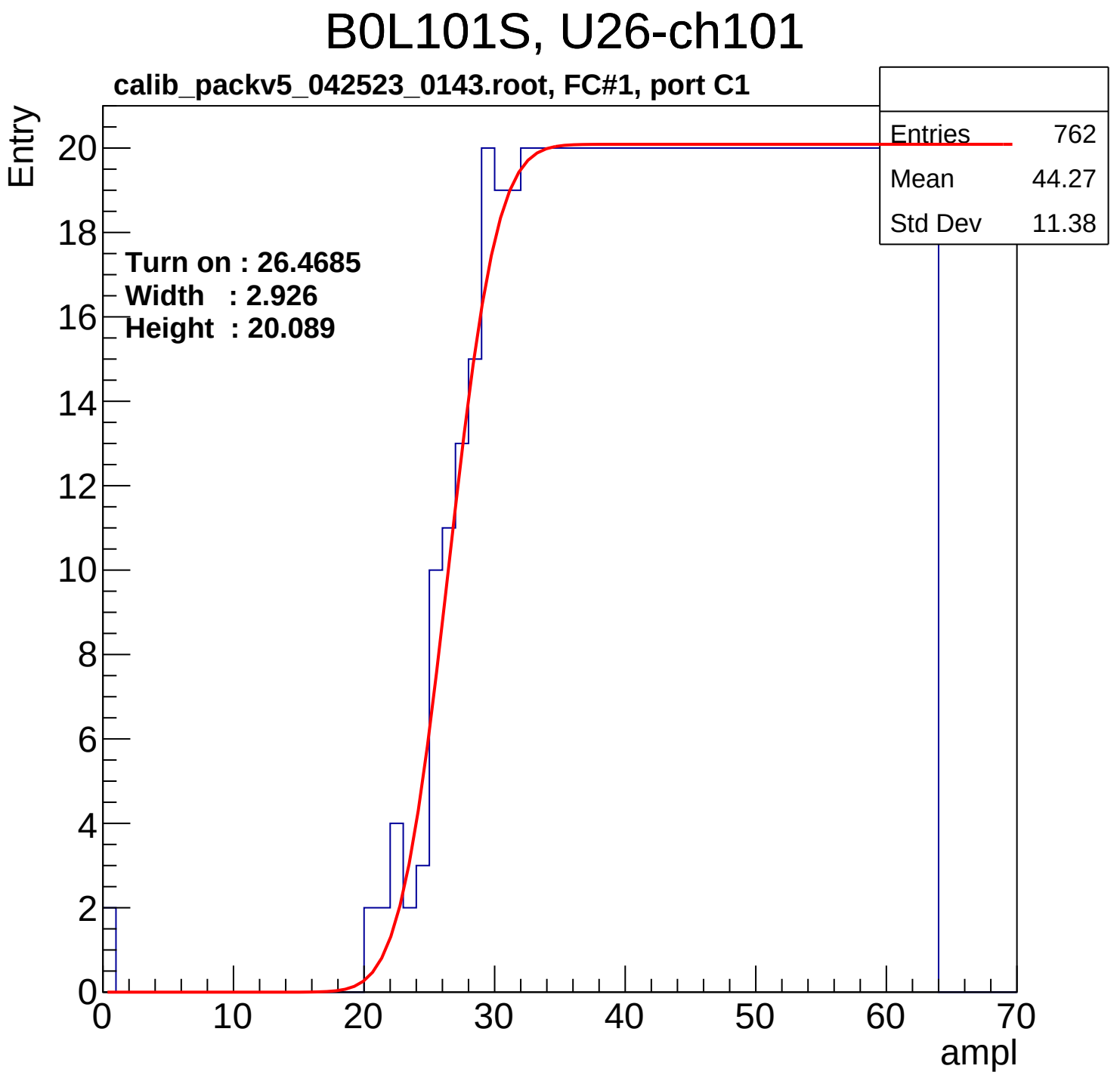
B0L101S, U26-ch101
calib_packv5_042523_0143.root, FC#1, port C1
Entries 762
Mean 44.27
Std Dev 11.38
Turn on : 26.4685
Width : 2.926
Height : 20.089
Entry
ampl
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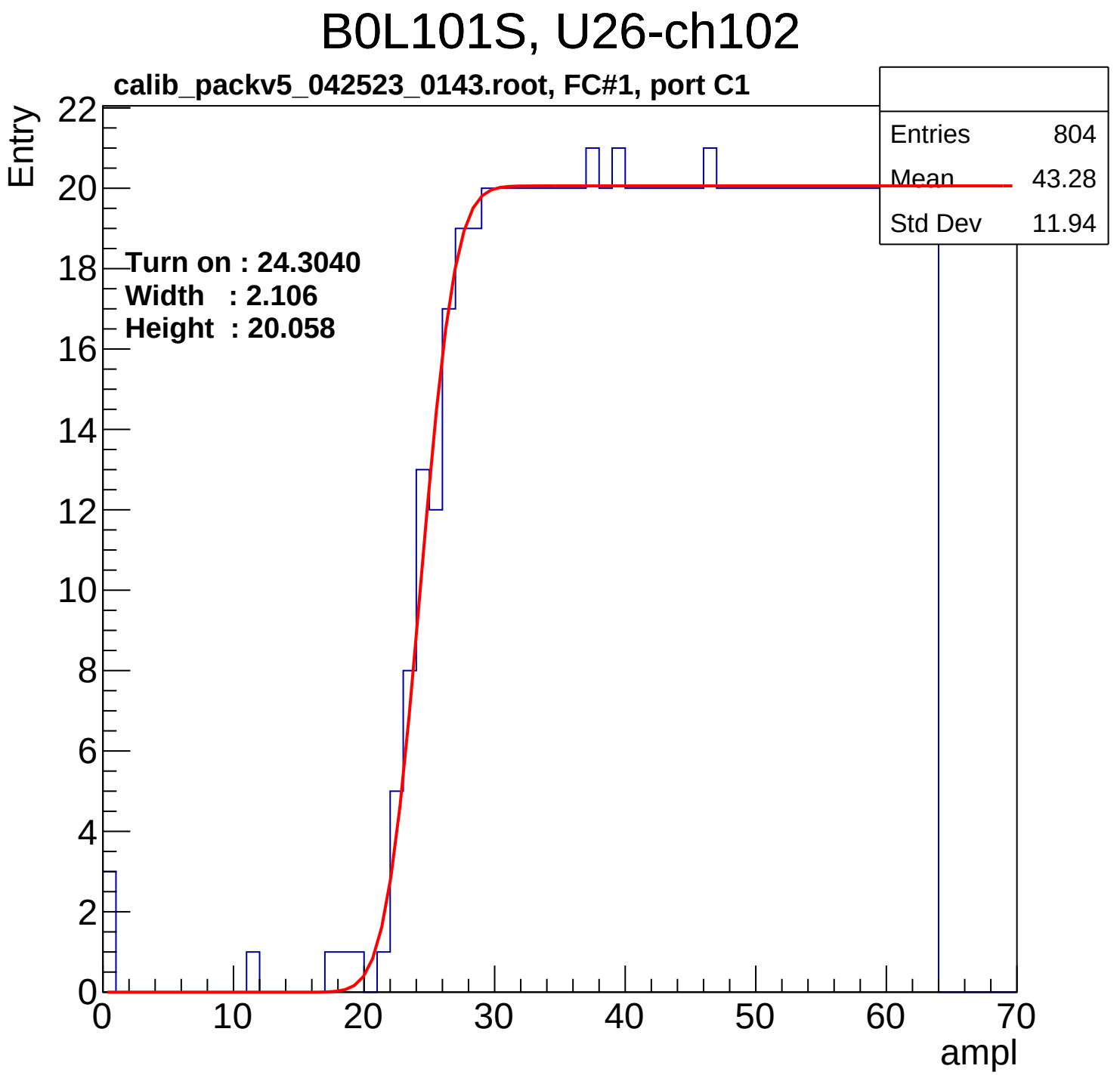
B0L101S, U26-ch102
calib_packv5_042523_0143.root, FC#1, port C1
Entries 804
Mean 43.28
Std Dev 11.94
Turn on : 24.3040
Width : 2.106
Height : 20.058
Entry
ampl
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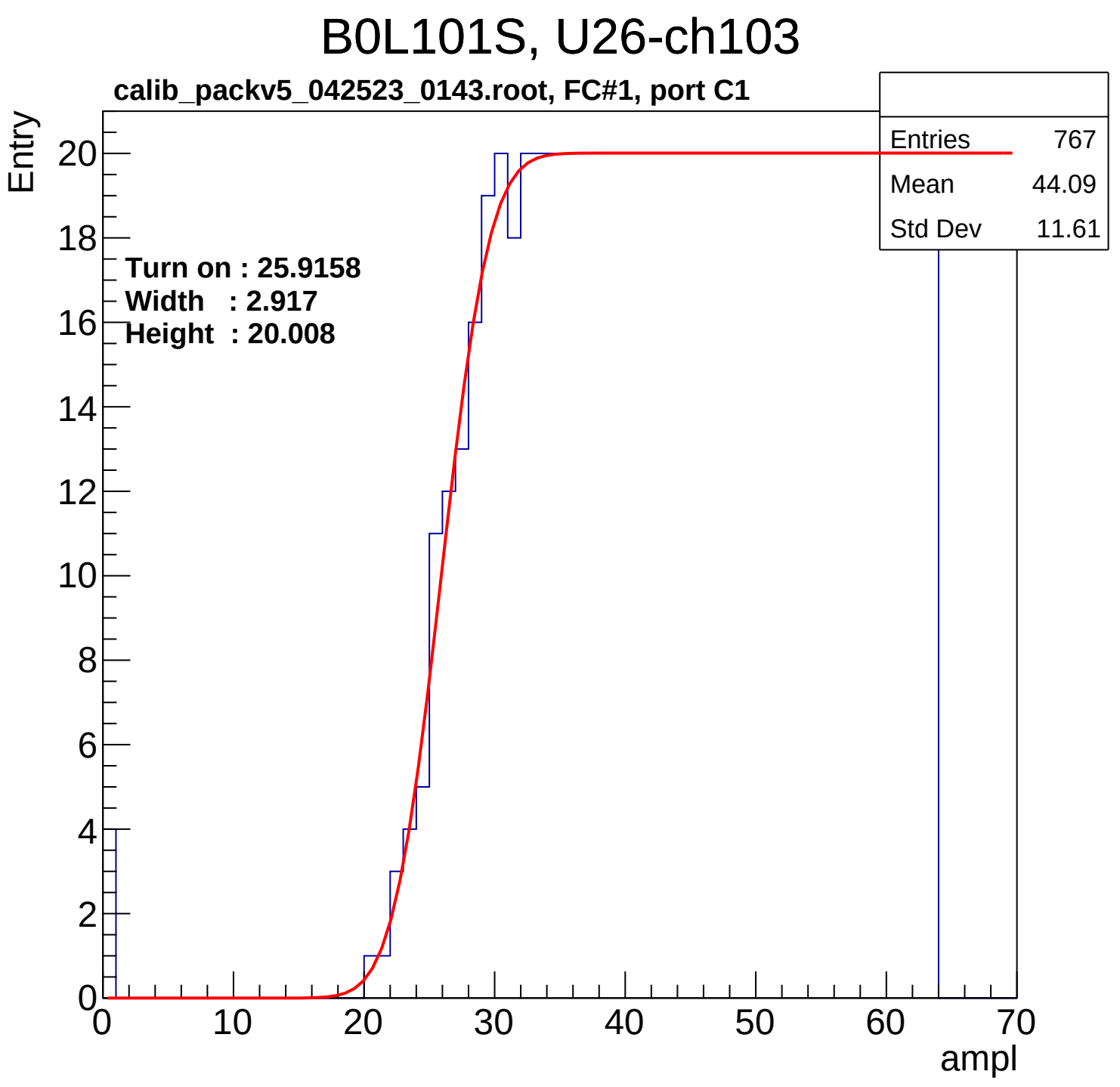
B0L101S, U26-ch103
calib_packv5_042523_0143.root, FC#1, port C1
Entries 767
Mean 44.09
Std Dev 11.61
Turn on : 25.9158
Width : 2.917
Height : 20.008
Entry
ampl
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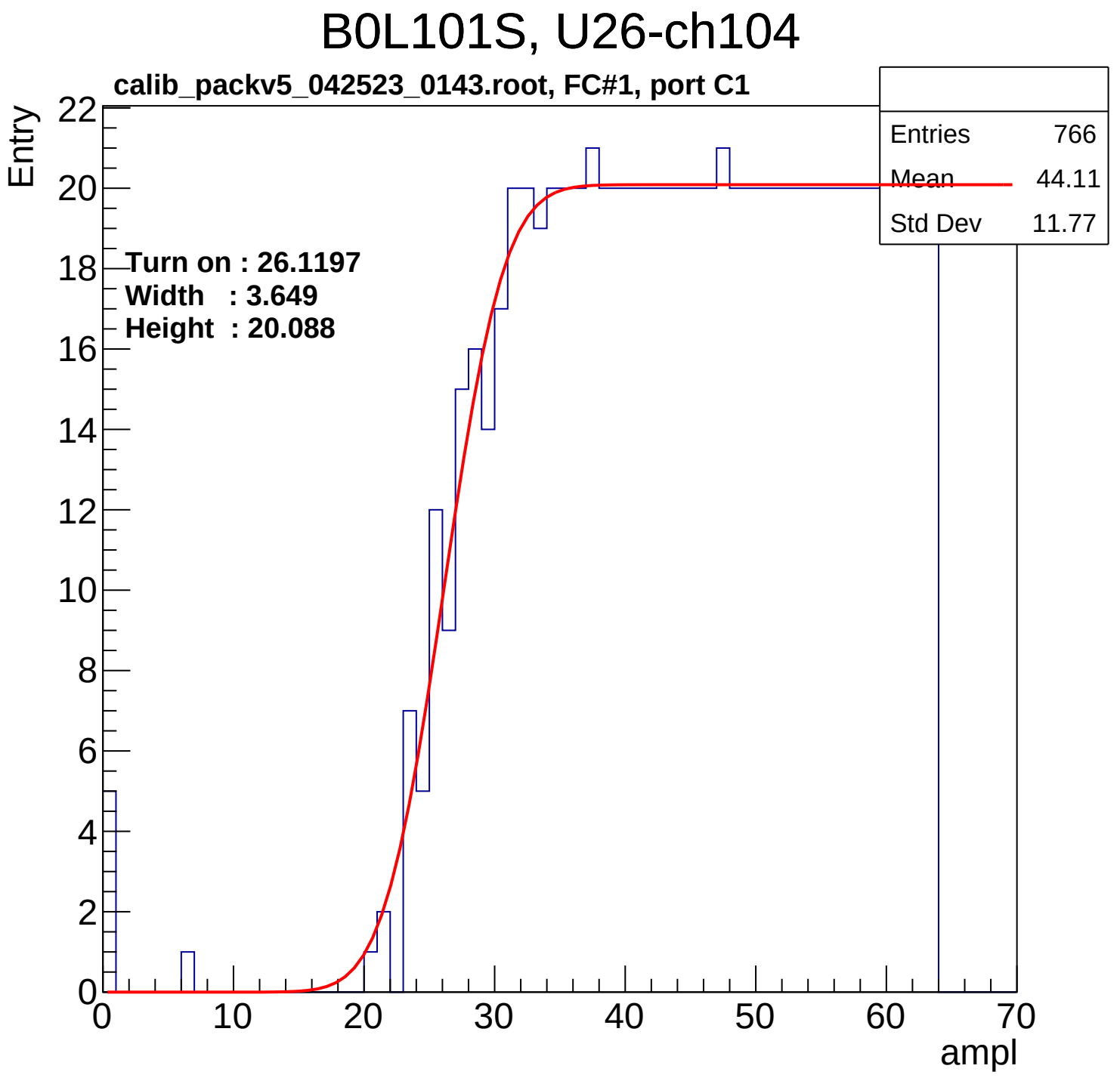
B0L101S, U26-ch104
calib_packv5_042523_0143.root, FC#1, port C1
Entries 766
Mean 44.11
Std Dev 11.77
Turn on : 26.1197
Width : 3.649
Height : 20.088
Entry
ampl
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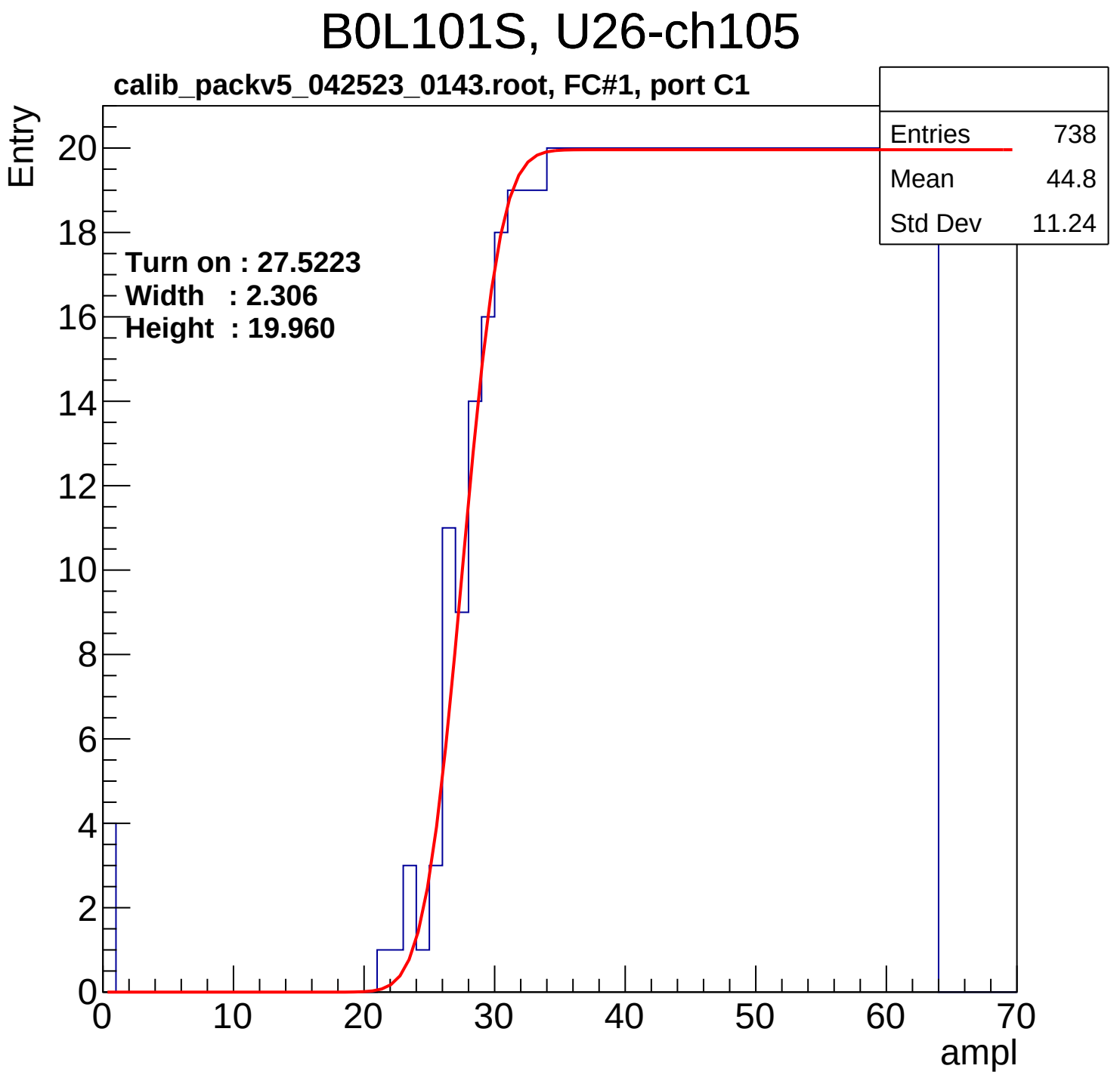
B0L101S, U26-ch105
calib_packv5_042523_0143.root, FC#1, port C1
Entries 738
Mean 44.8
Std Dev 11.24
Turn on : 27.5223
Width : 2.306
Height : 19.960
Entry
ampl
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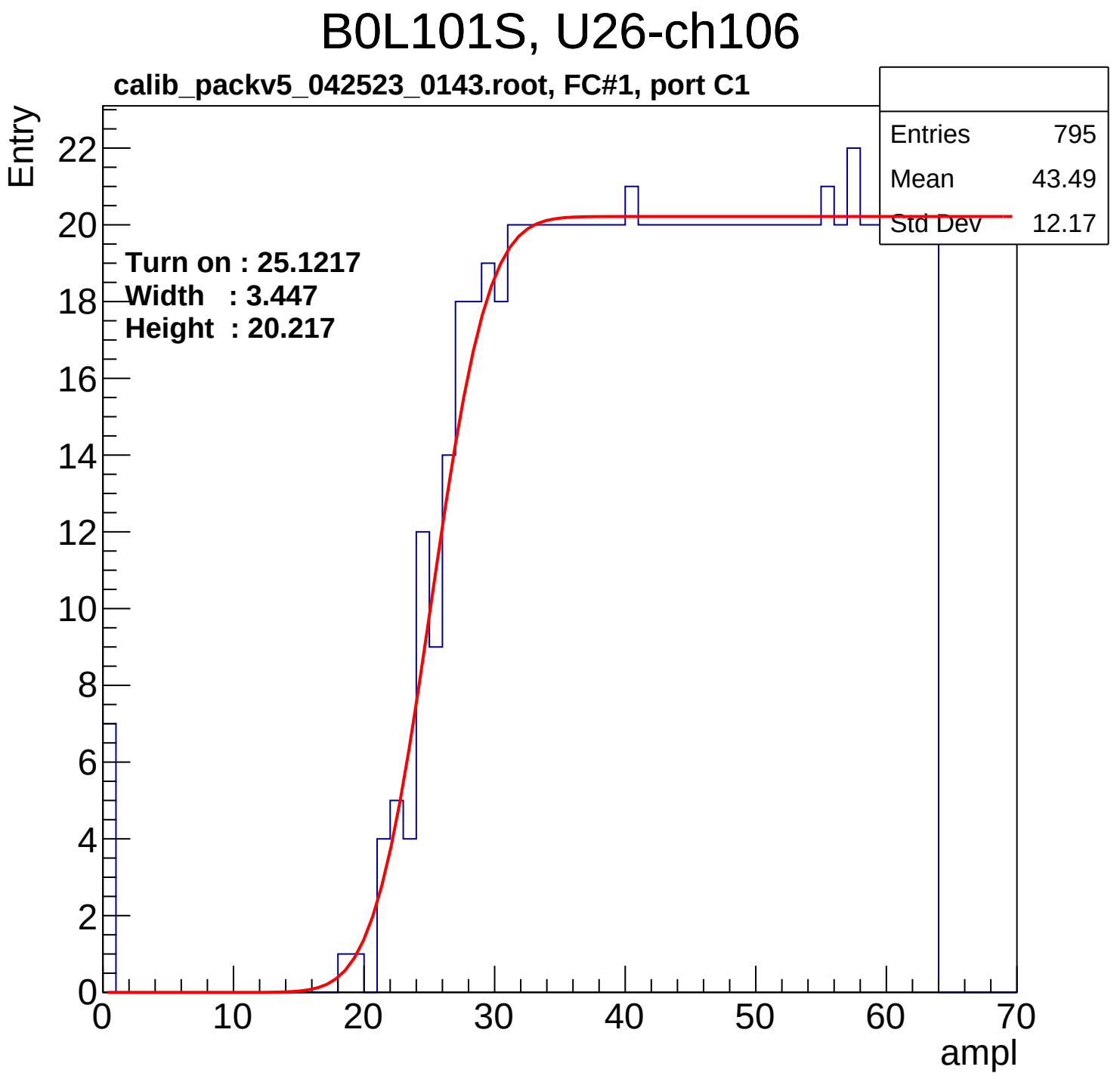
B0L101S, U26-ch106
calib_packv5_042523_0143.root, FC#1, port C1
Entries 795
Mean 43.49
Std Dev 12.17
Turn on : 25.1217
Width : 3.447
Height : 20.217
Entry
ampl
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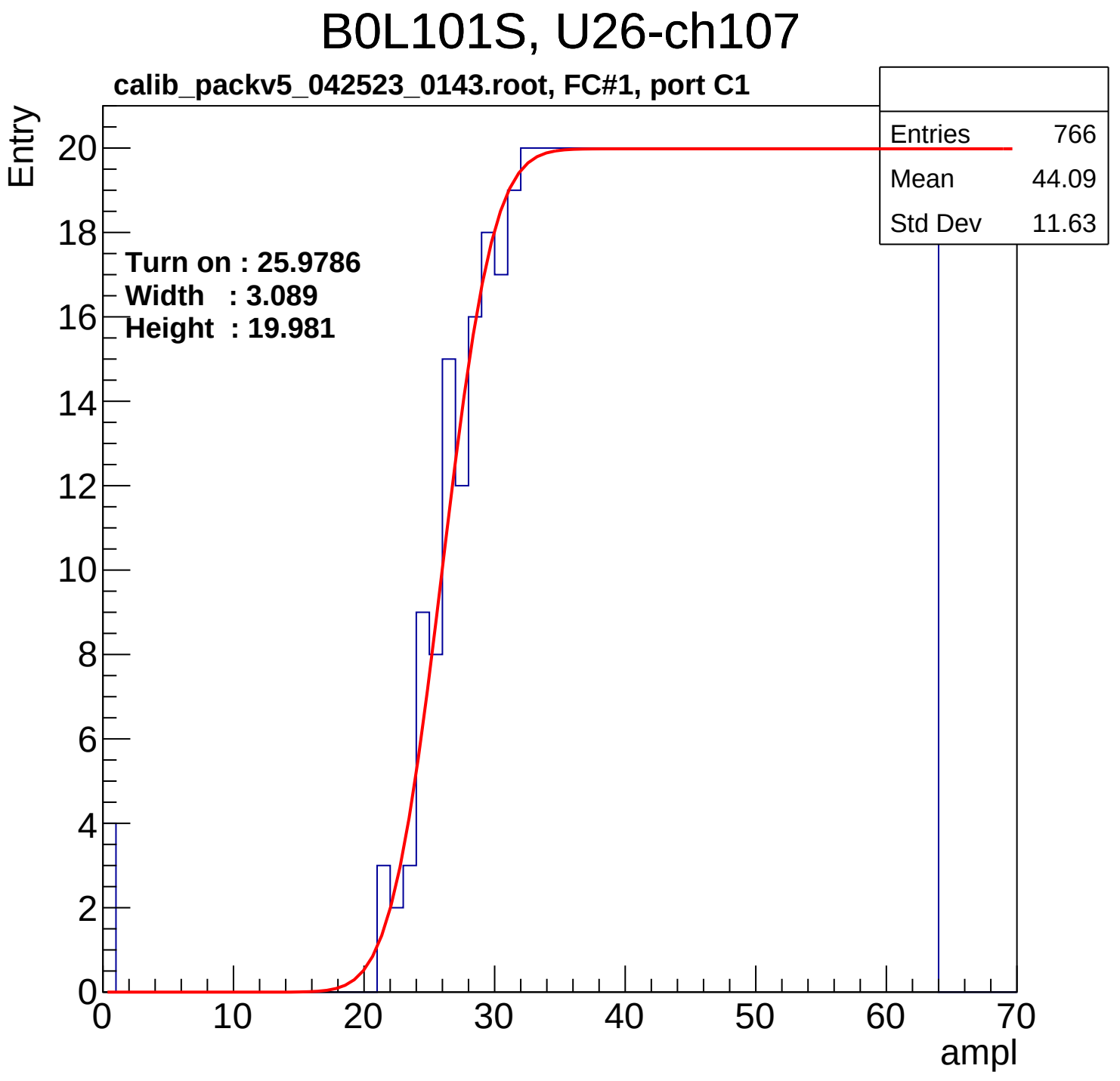
B0L101S, U26-ch107
calib_packv5_042523_0143.root, FC#1, port C1
Entries 766
Mean 44.09
Std Dev 11.63
Turn on : 25.9786
Width : 3.089
Height : 19.981
Entry
ampl
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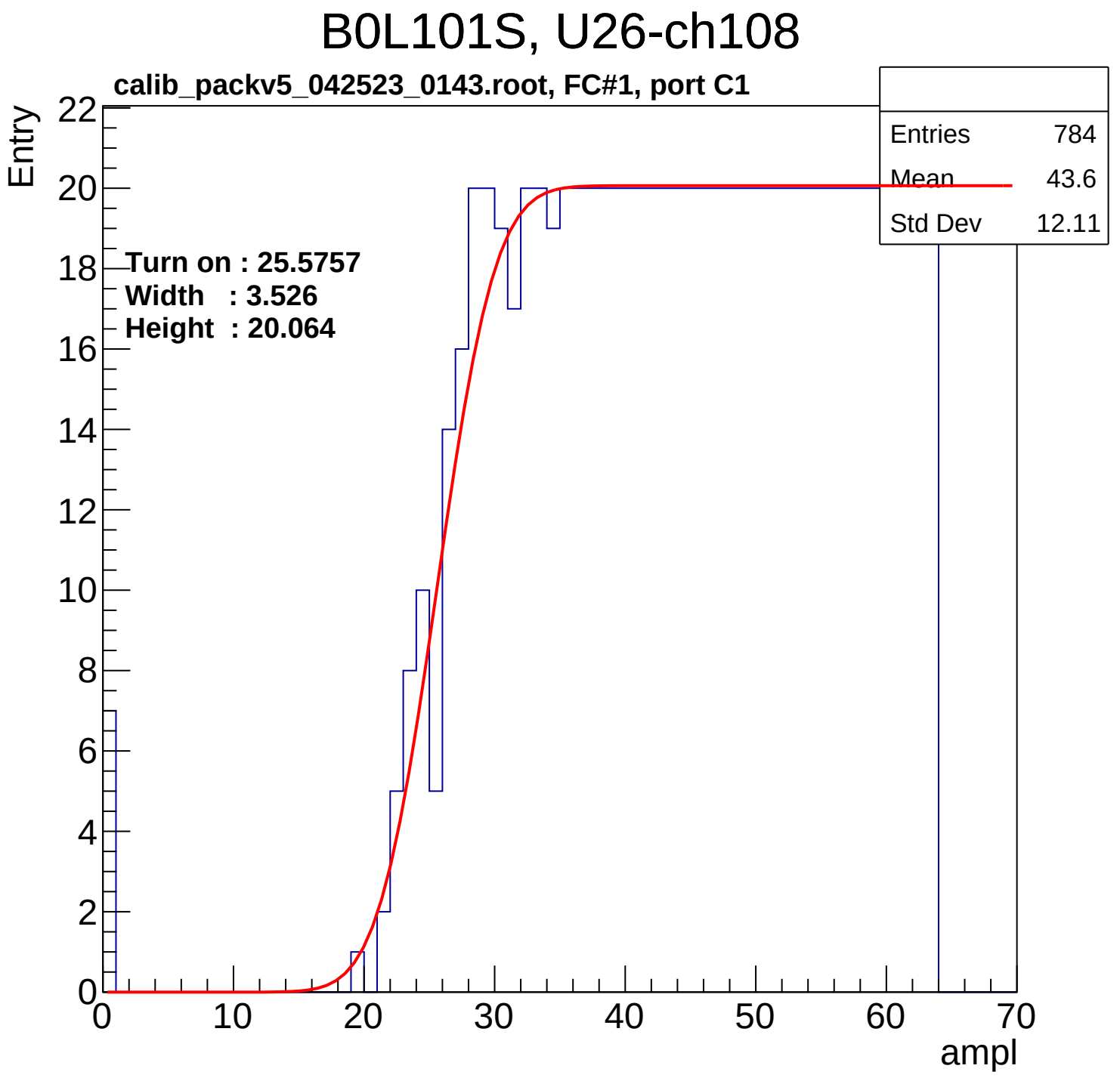
B0L101S, U26-ch108
calib_packv5_042523_0143.root, FC#1, port C1
Entries 784
Mean 43.6
Std Dev 12.11
Turn on : 25.5757
Width : 3.526
Height : 20.064
Entry
ampl
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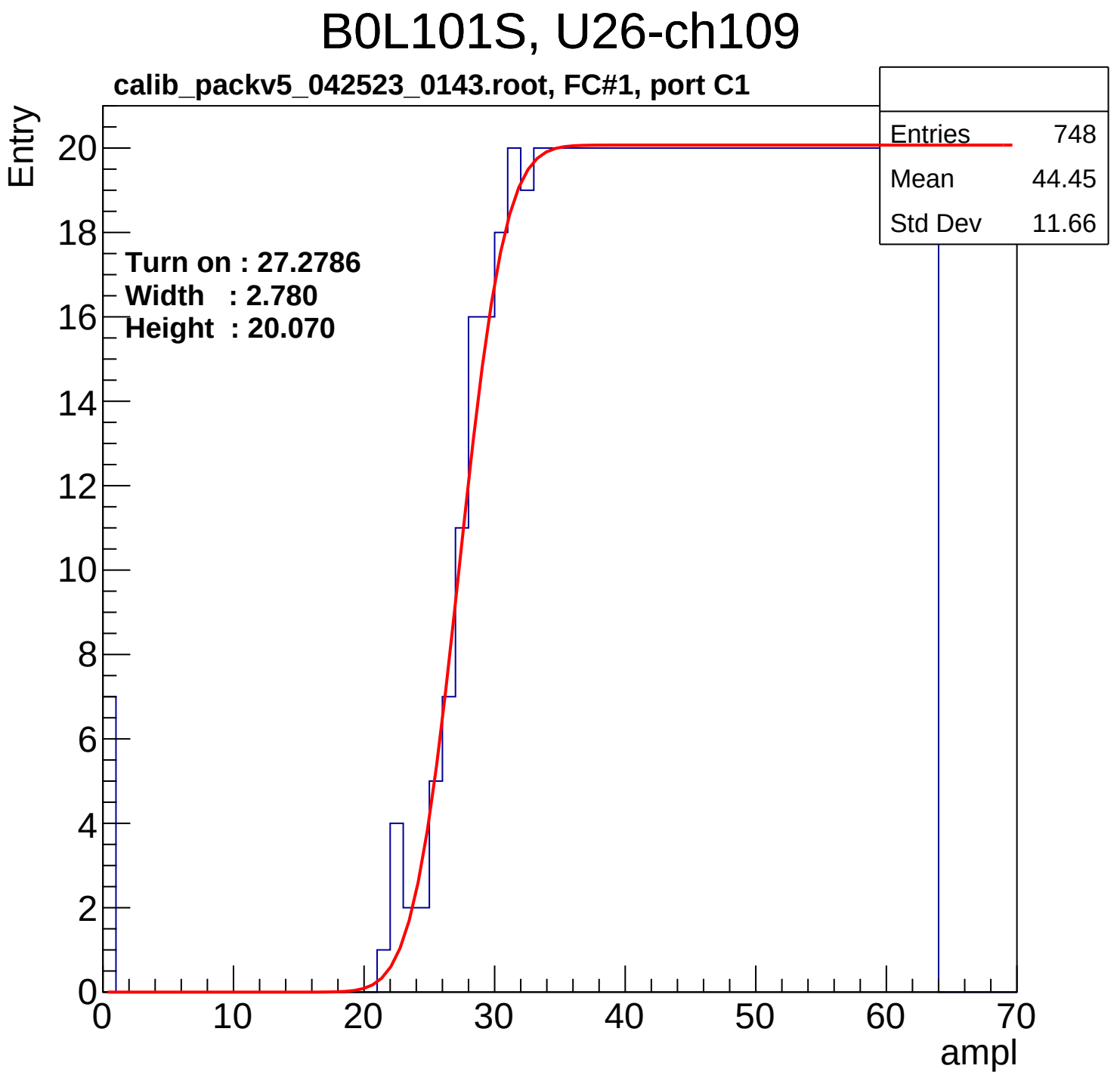
B0L101S, U26-ch109
calib_packv5_042523_0143.root, FC#1, port C1
Entries 748
Mean 44.45
Std Dev 11.66
Turn on : 27.2786
Width : 2.780
Height : 20.070
Entry
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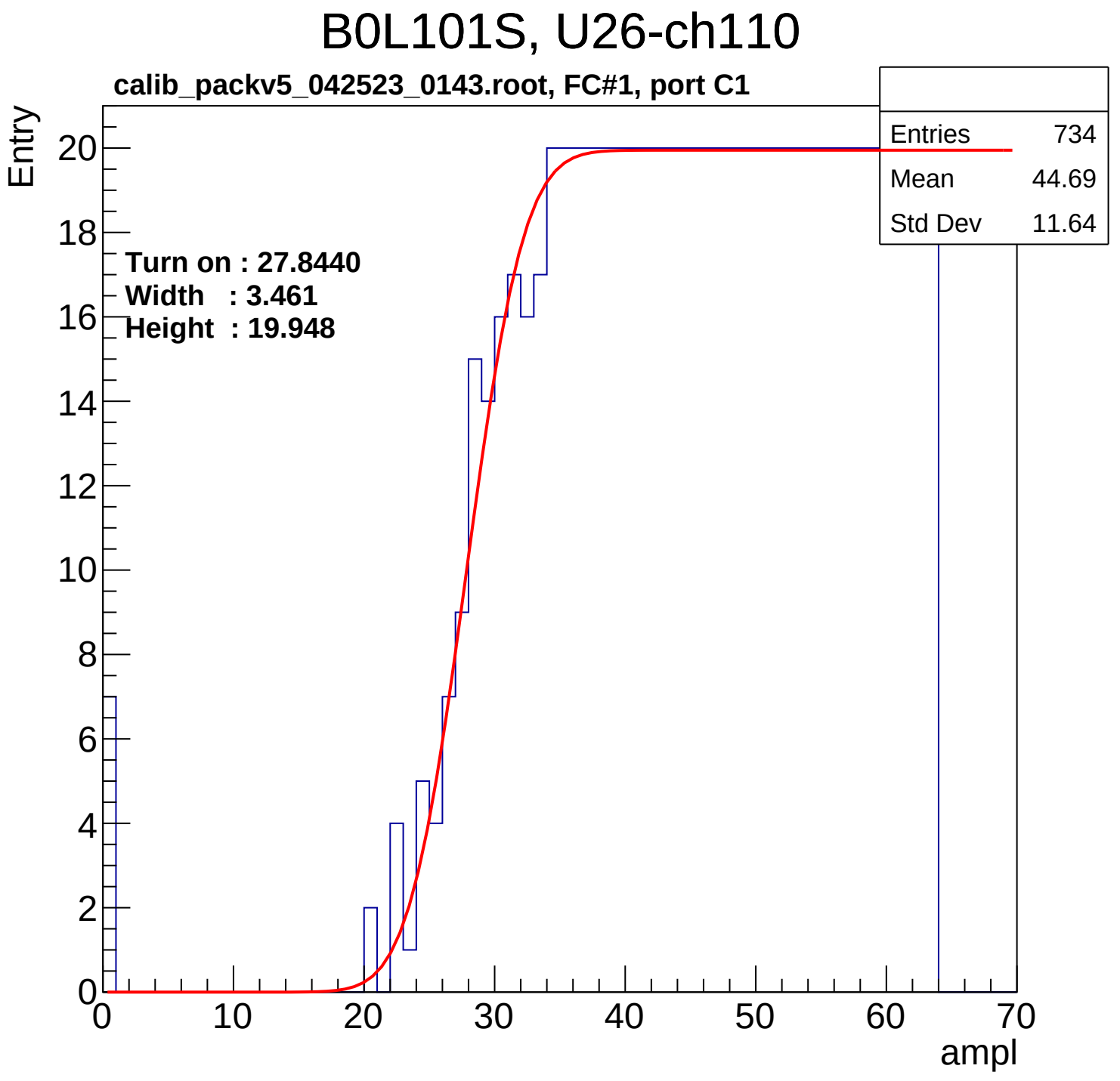
B0L101S, U26-ch110
calib_packv5_042523_0143.root, FC#1, port C1
Entries 734
Mean 44.69
Std Dev 11.64
Turn on : 27.8440
Width : 3.461
Height : 19.948
Entry
ampl
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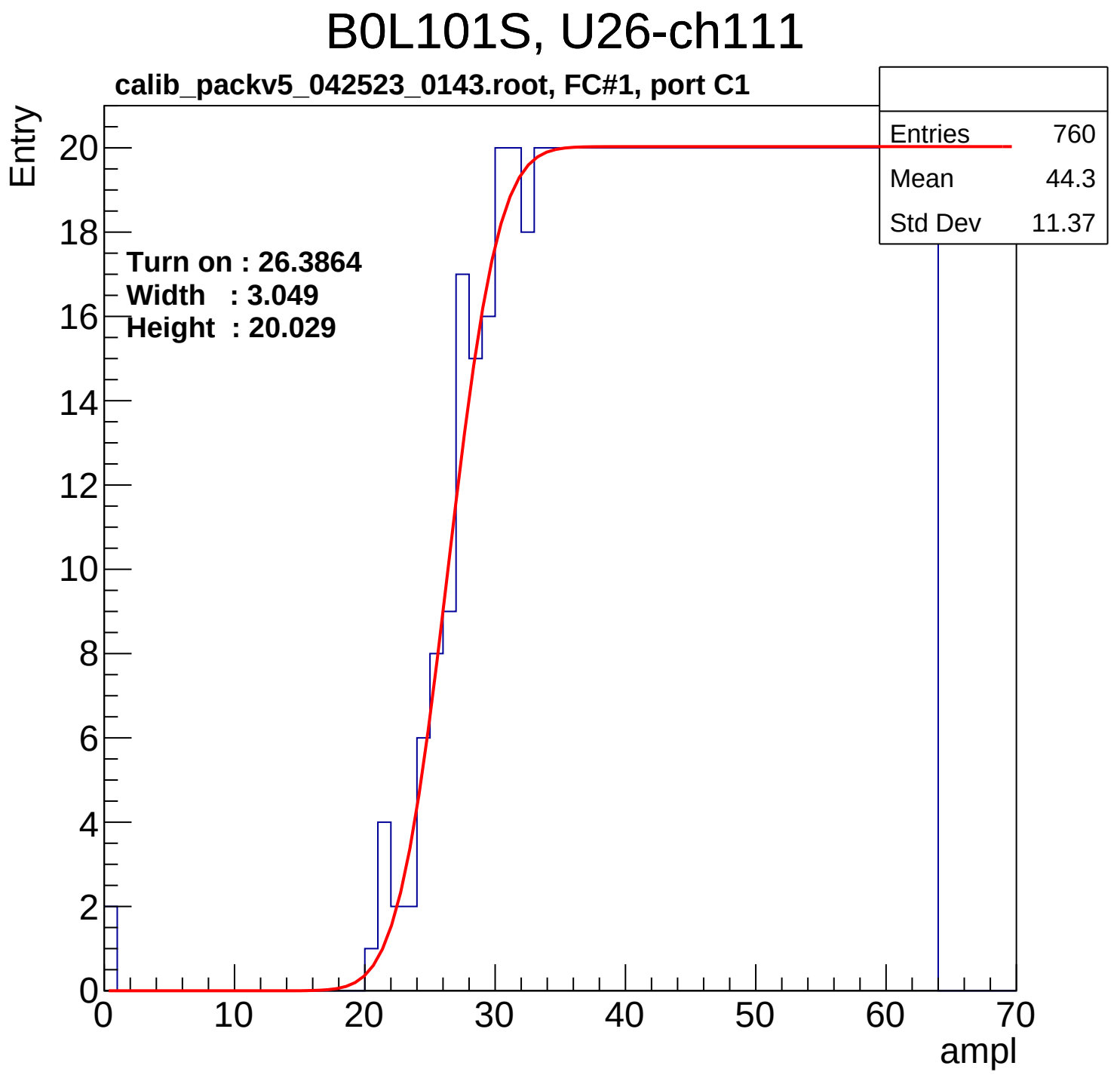
B0L101S, U26-ch111
calib_packv5_042523_0143.root, FC#1, port C1
Entries 760
Mean 44.3
Std Dev 11.37
Turn on : 26.3864
Width : 3.049
Height : 20.029
Entry
ampl
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6
8
10
12
14
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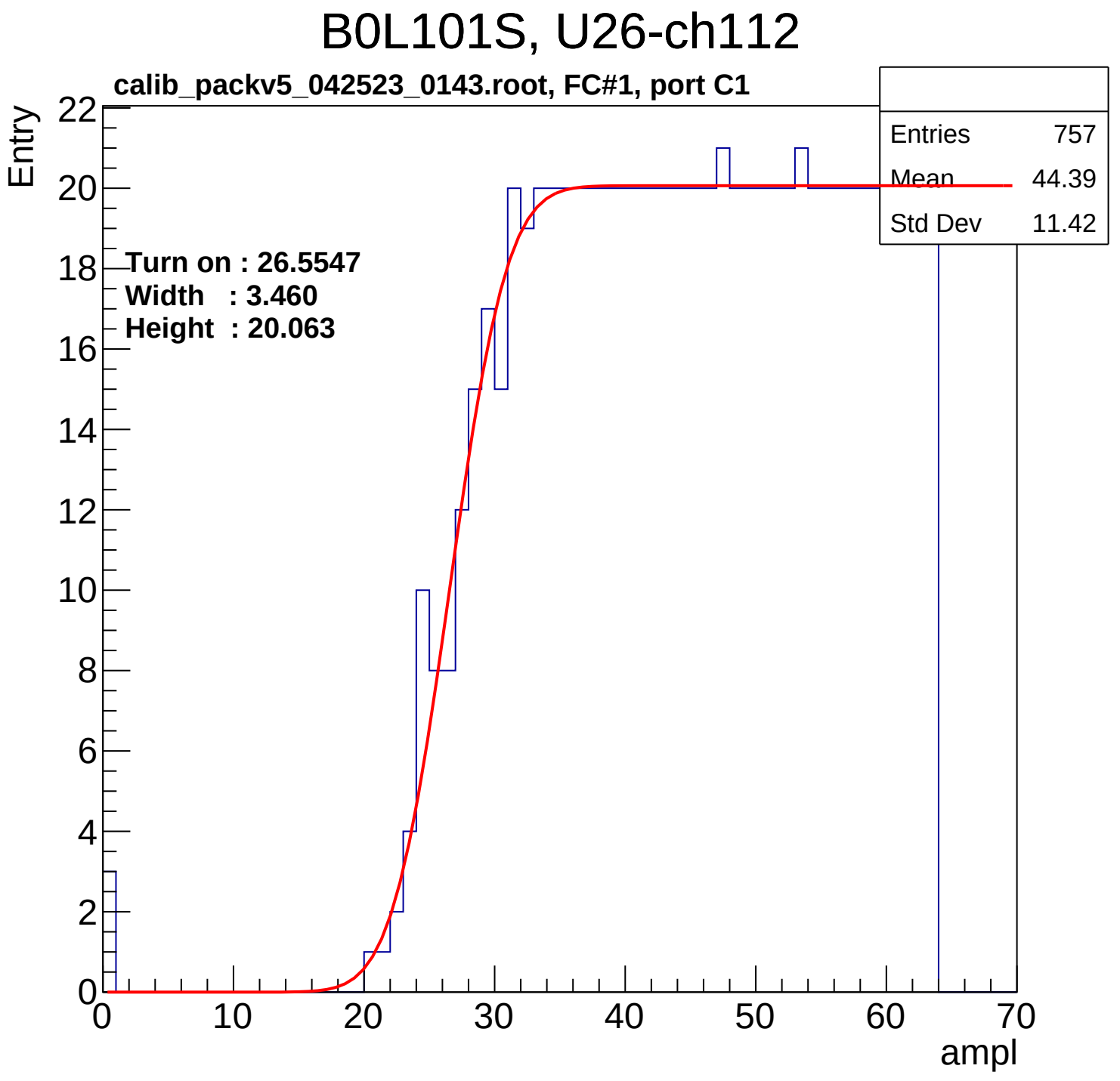
B0L101S, U26-ch112
calib_packv5_042523_0143.root, FC#1, port C1
Entries 757
Mean 44.39
Std Dev 11.42
Turn on : 26.5547
Width : 3.460
Height : 20.063
Entry
ampl
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16
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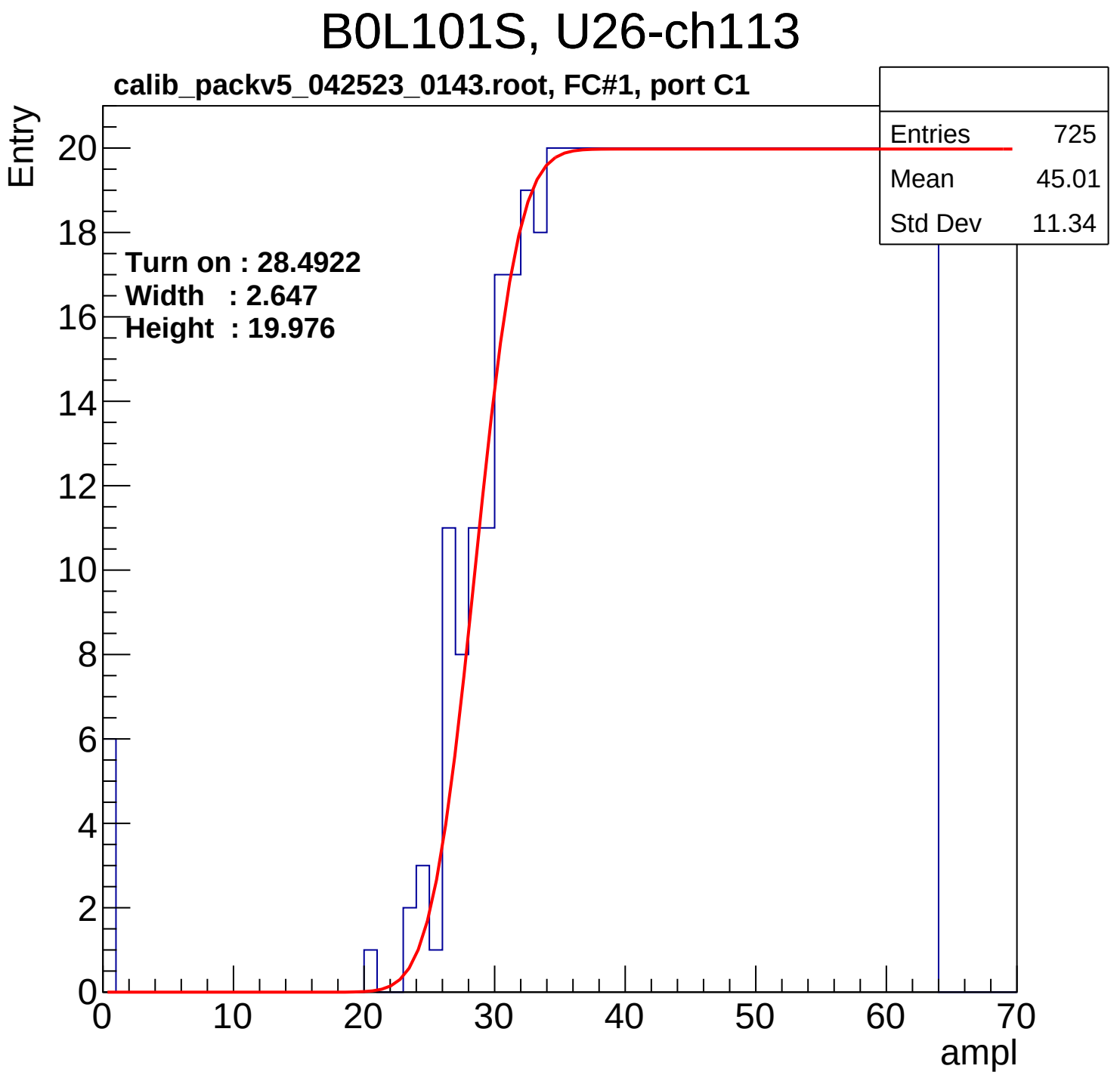
B0L101S, U26-ch113
calib_packv5_042523_0143.root, FC#1, port C1
Entries 725
Mean 45.01
Std Dev 11.34
Turn on : 28.4922
Width : 2.647
Height : 19.976
Entry
ampl
0
2
4
6
8
10
12
14
16
18
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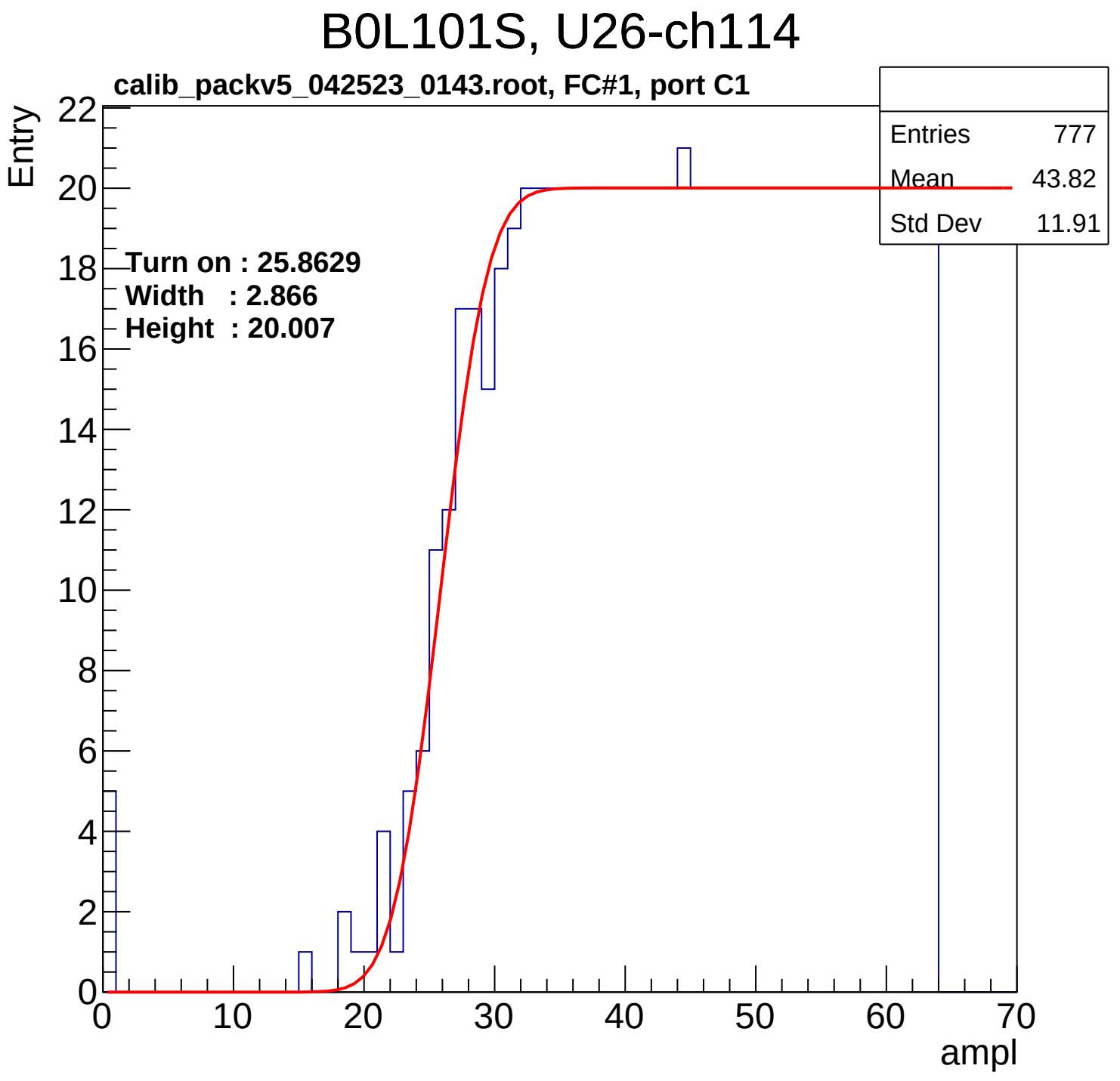
B0L101S, U26-ch114
calib_packv5_042523_0143.root, FC#1, port C1
Entries 777
Mean 43.82
Std Dev 11.91
Turn on : 25.8629
Width : 2.866
Height : 20.007
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
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0
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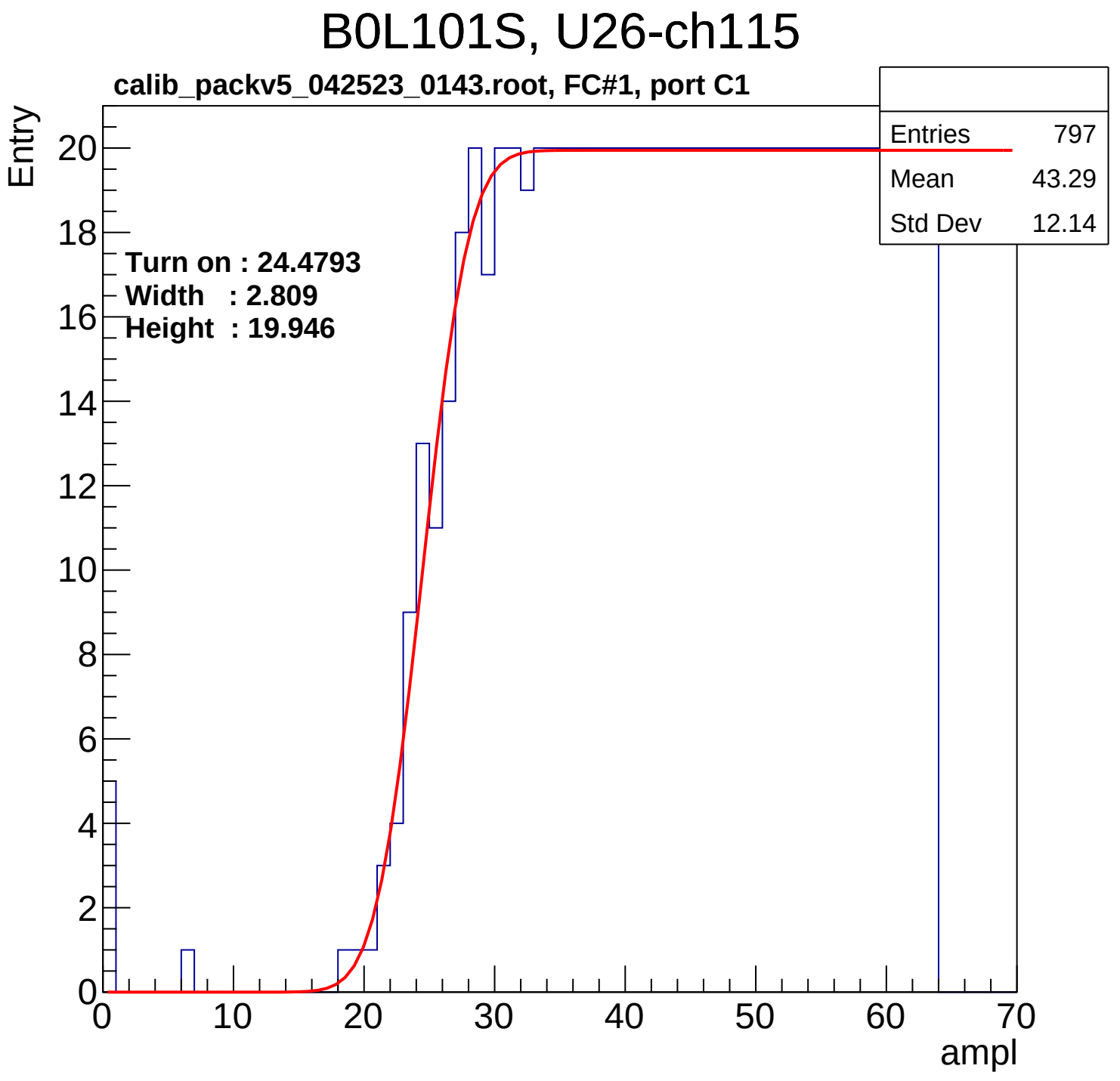
B0L101S, U26-ch115
calib_packv5_042523_0143.root, FC#1, port C1
Entries 797
Mean 43.29
Std Dev 12.14
Turn on : 24.4793
Width : 2.809
Height : 19.946
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
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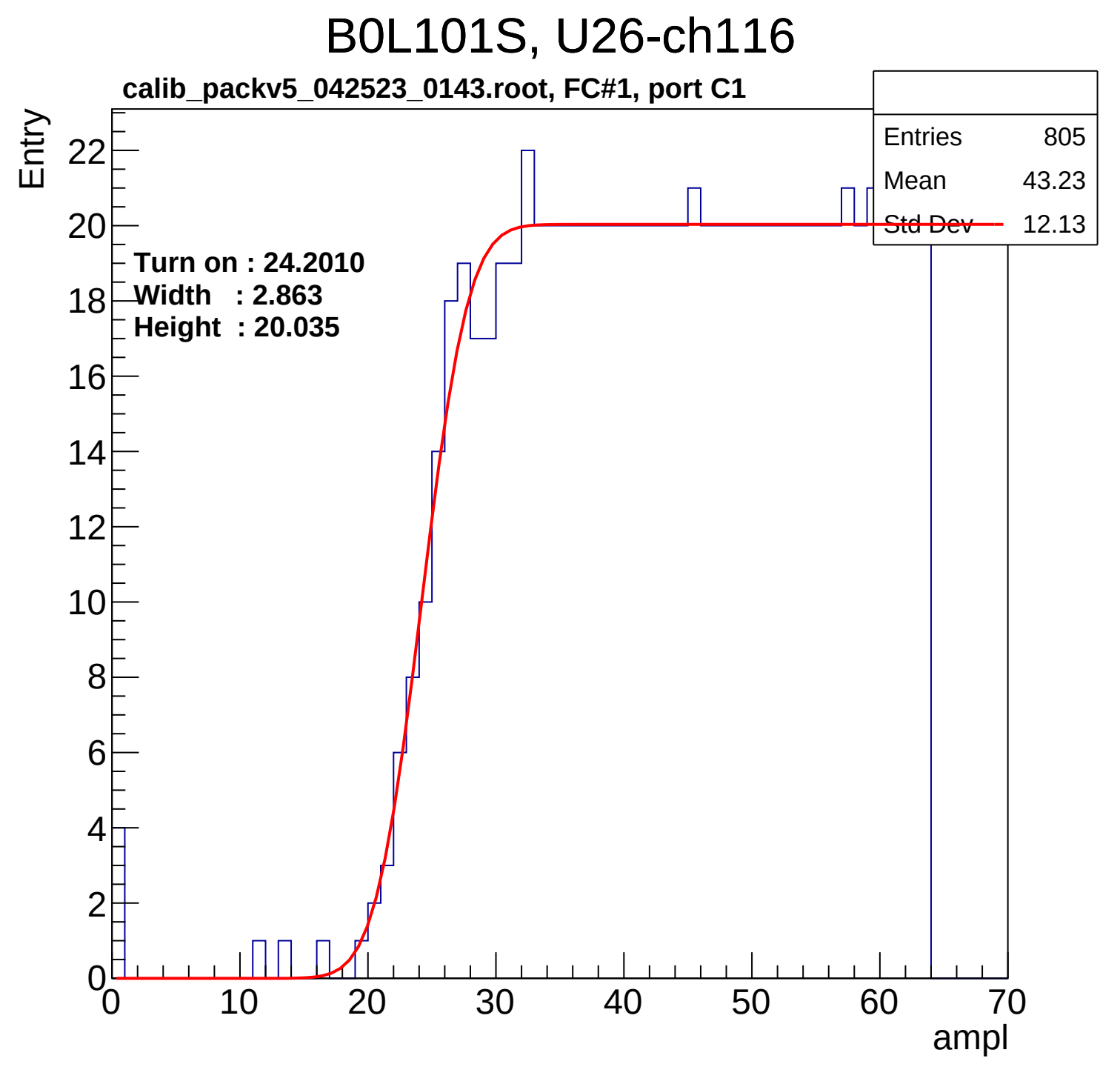
B0L101S, U26-ch116
calib_packv5_042523_0143.root, FC#1, port C1
Entries 805
Mean 43.23
Std Dev 12.13
Turn on : 24.2010
Width : 2.863
Height : 20.035
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
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60
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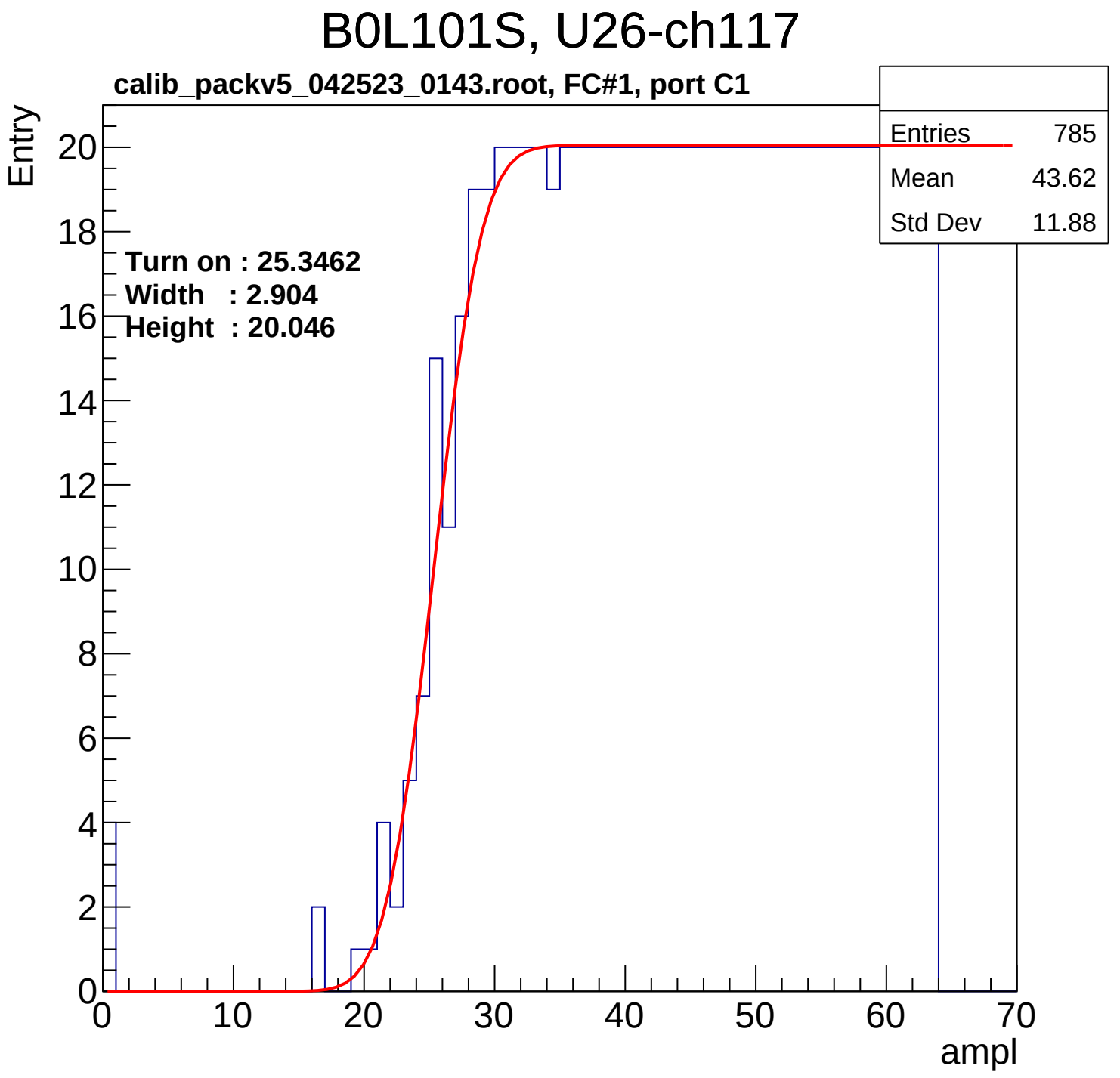
B0L101S, U26-ch117
calib_packv5_042523_0143.root, FC#1, port C1
Entries 785
Mean 43.62
Std Dev 11.88
Turn on : 25.3462
Width : 2.904
Height : 20.046
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
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20
30
40
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60
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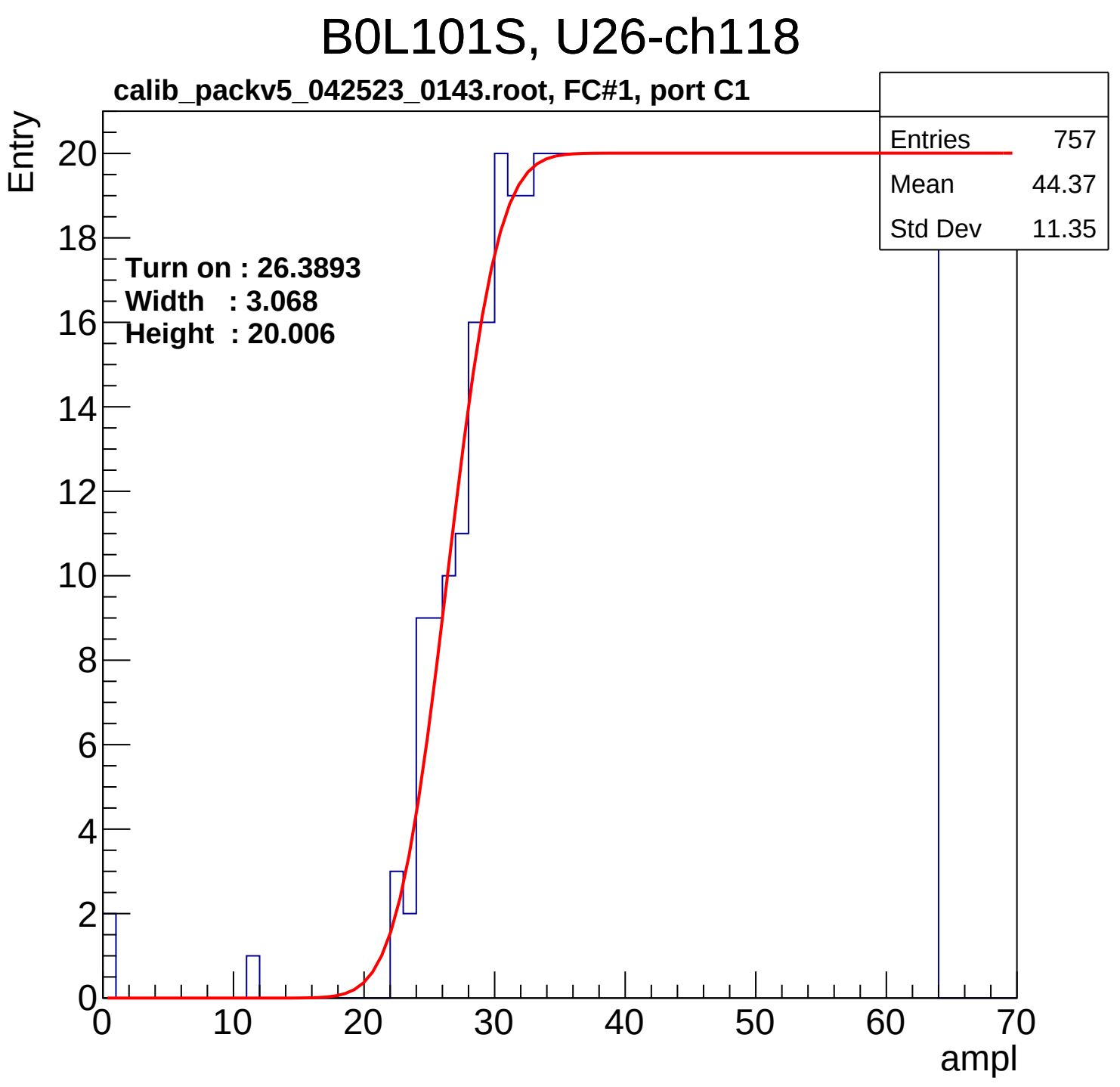
B0L101S, U26-ch118
calib_packv5_042523_0143.root, FC#1, port C1
Entries 757
Mean 44.37
Std Dev 11.35
Turn on : 26.3893
Width : 3.068
Height : 20.006
Entry
ampl
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6
8
10
12
14
16
18
20
0
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20
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60
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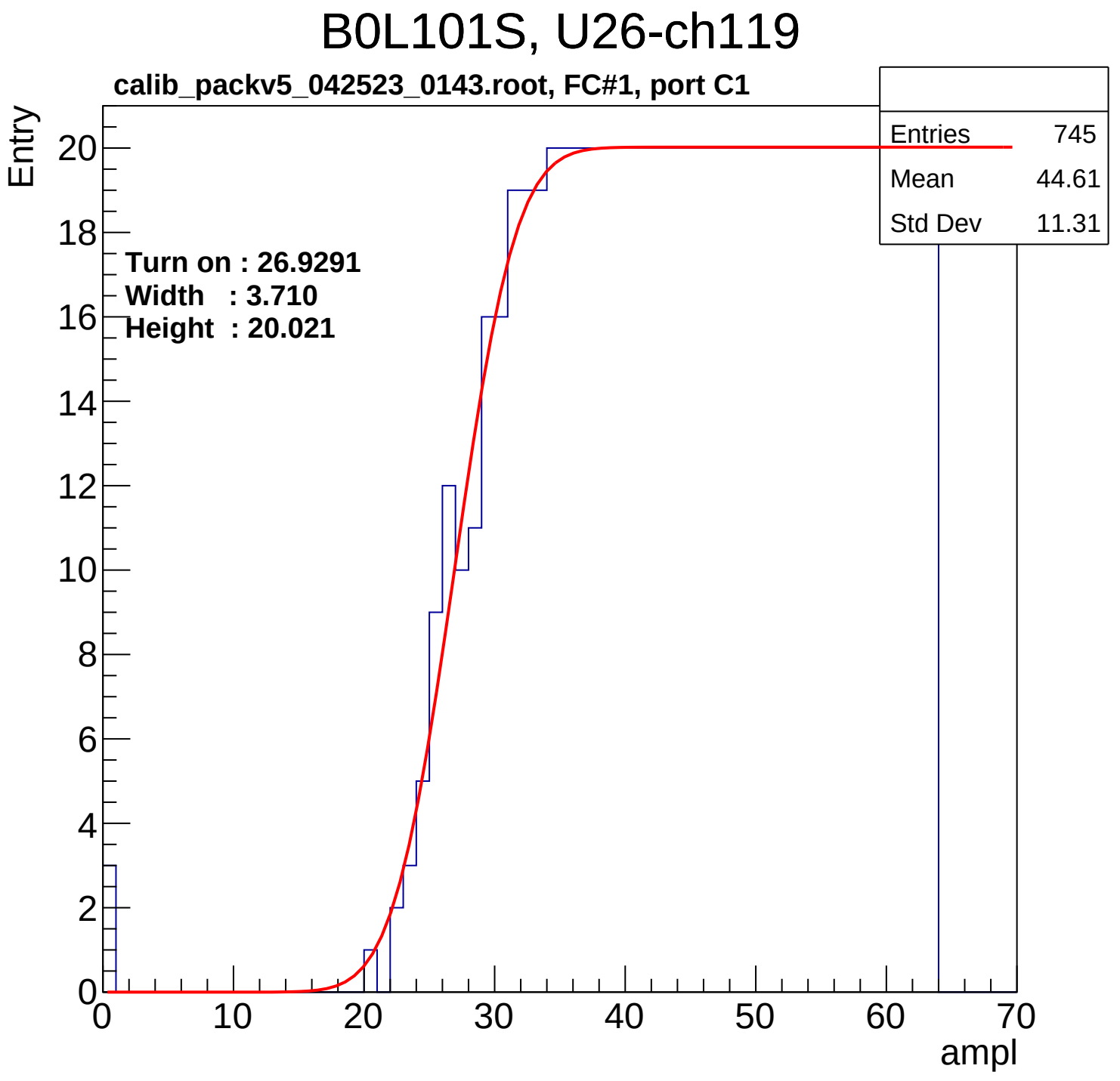
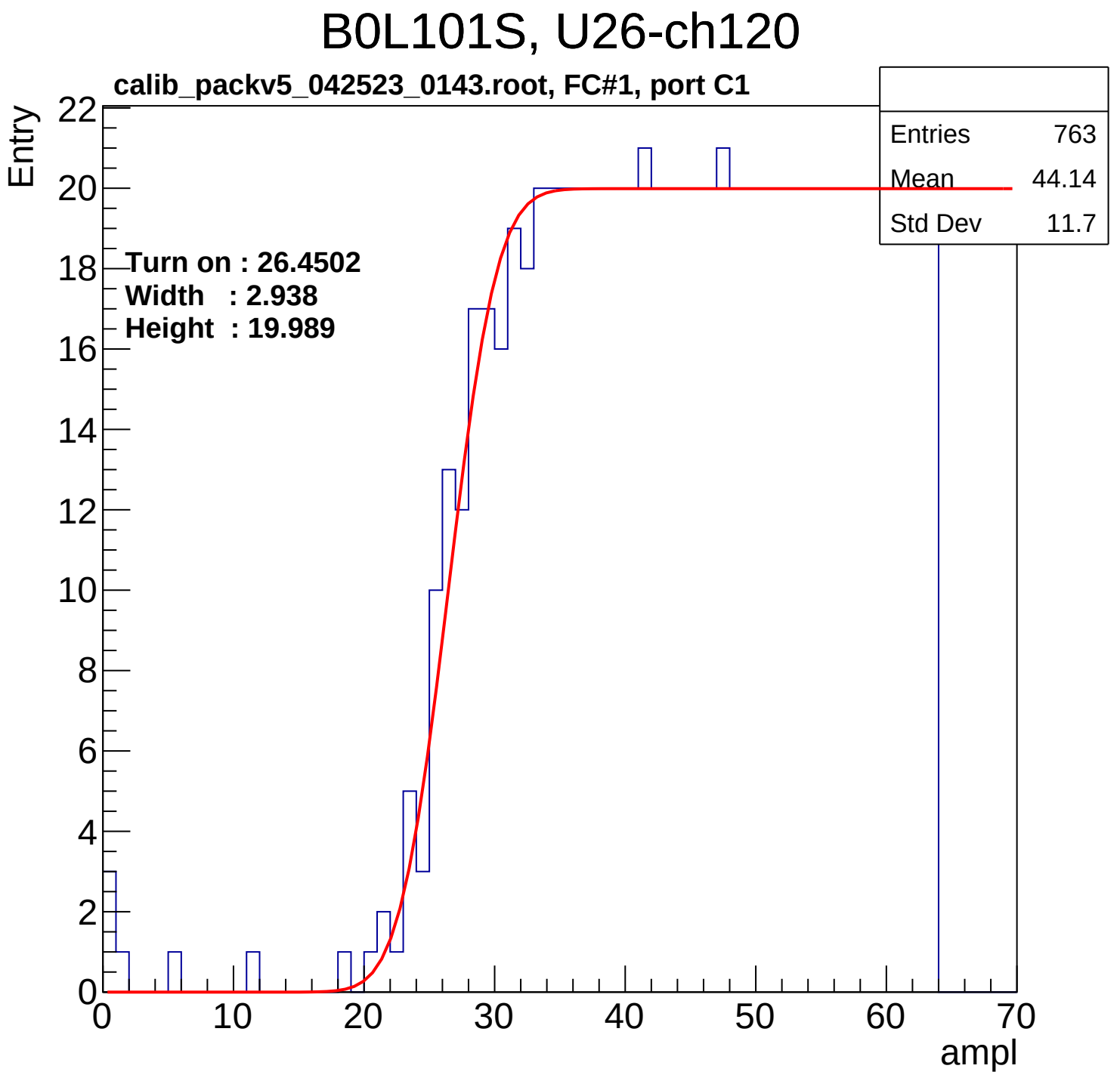

B0L101S, U26-ch119
calib_packv5_042523_0143.root, FC#1, port C1
Entries 745
Mean 44.61
Std Dev 11.31
Turn on : 26.9291
Width : 3.710
Height : 20.021
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70


B0L101S, U26-ch120
calib_packv5_042523_0143.root, FC#1, port C1
Entries 763
Mean 44.14
Std Dev 11.7
Turn on : 26.4502
Width : 2.938
Height : 19.989
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
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20
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40
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60
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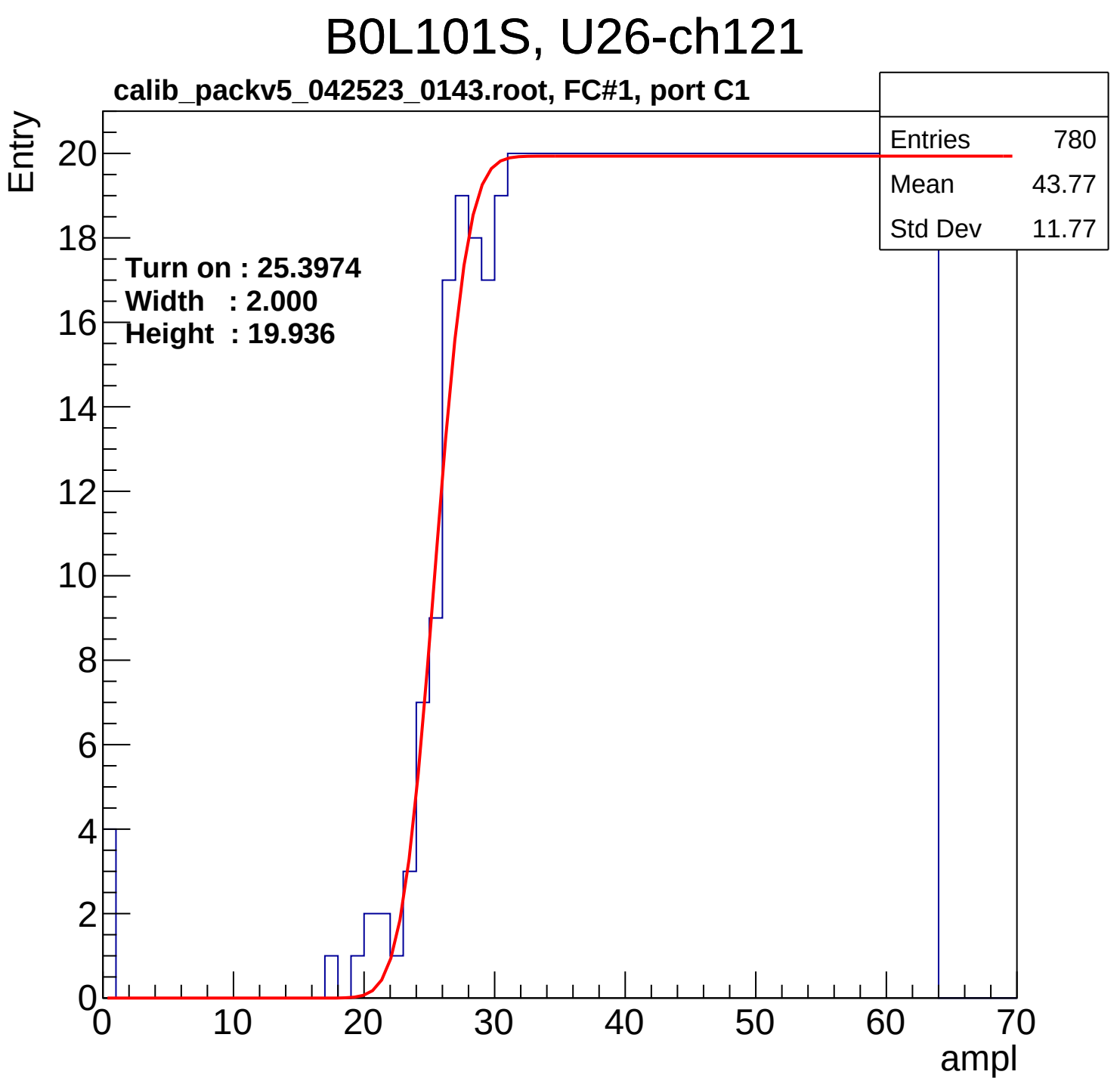
B0L101S, U26-ch121
calib_packv5_042523_0143.root, FC#1, port C1
Entries 780
Mean 43.77
Std Dev 11.77
Turn on : 25.3974
Width : 2.000
Height : 19.936
Entry
ampl
0
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6
8
10
12
14
16
18
20
0
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20
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40
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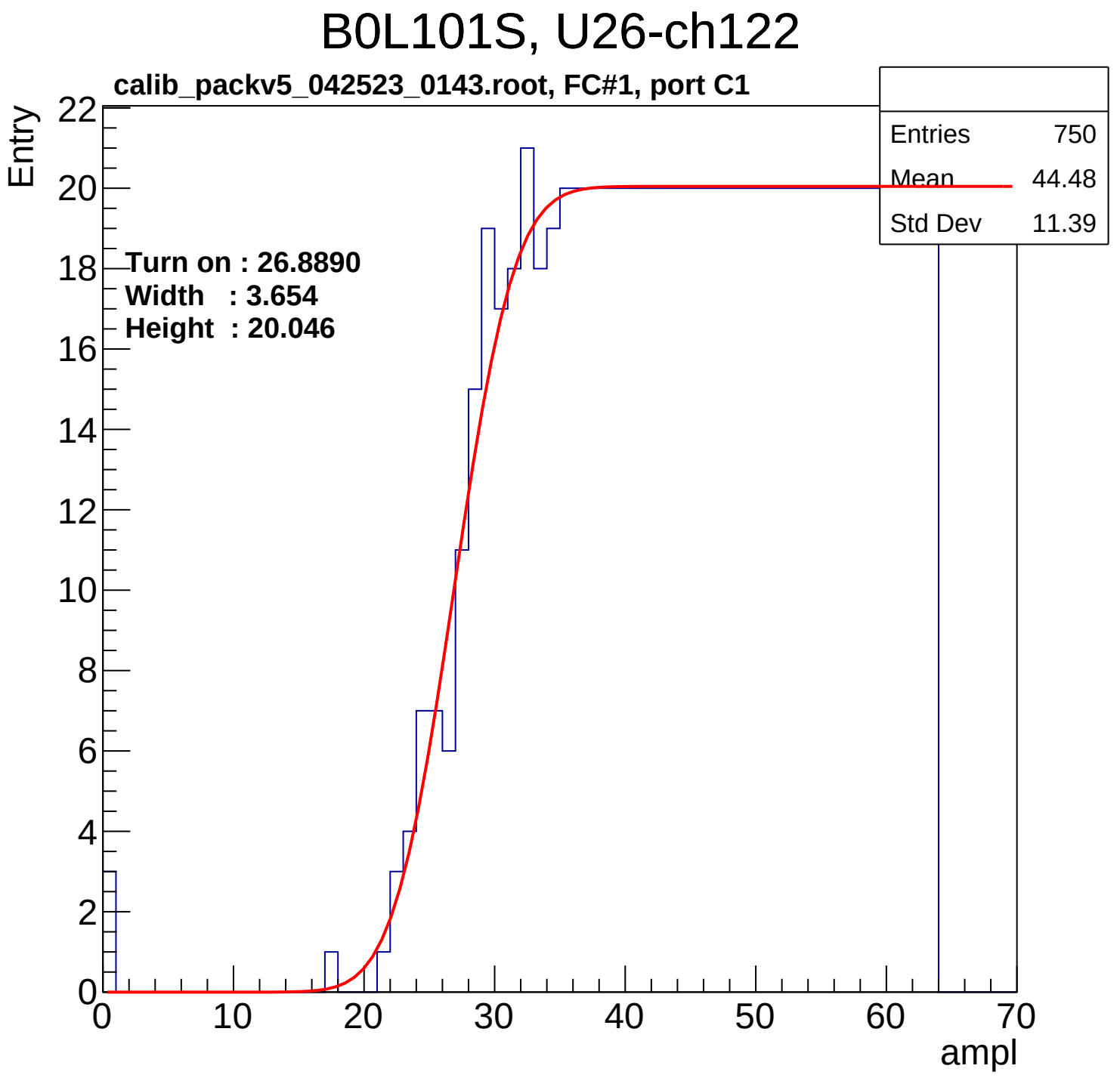
60
70


B0L101S, U26-ch122
calib_packv5_042523_0143.root, FC#1, port C1
Entries 750
Mean 44.48
Std Dev 11.39
Turn on : 26.8890
Width : 3.654
Height : 20.046
Entry
ampl
0
2
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6
8
10
12
14
16
18
20
22
0
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20
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40
50
60
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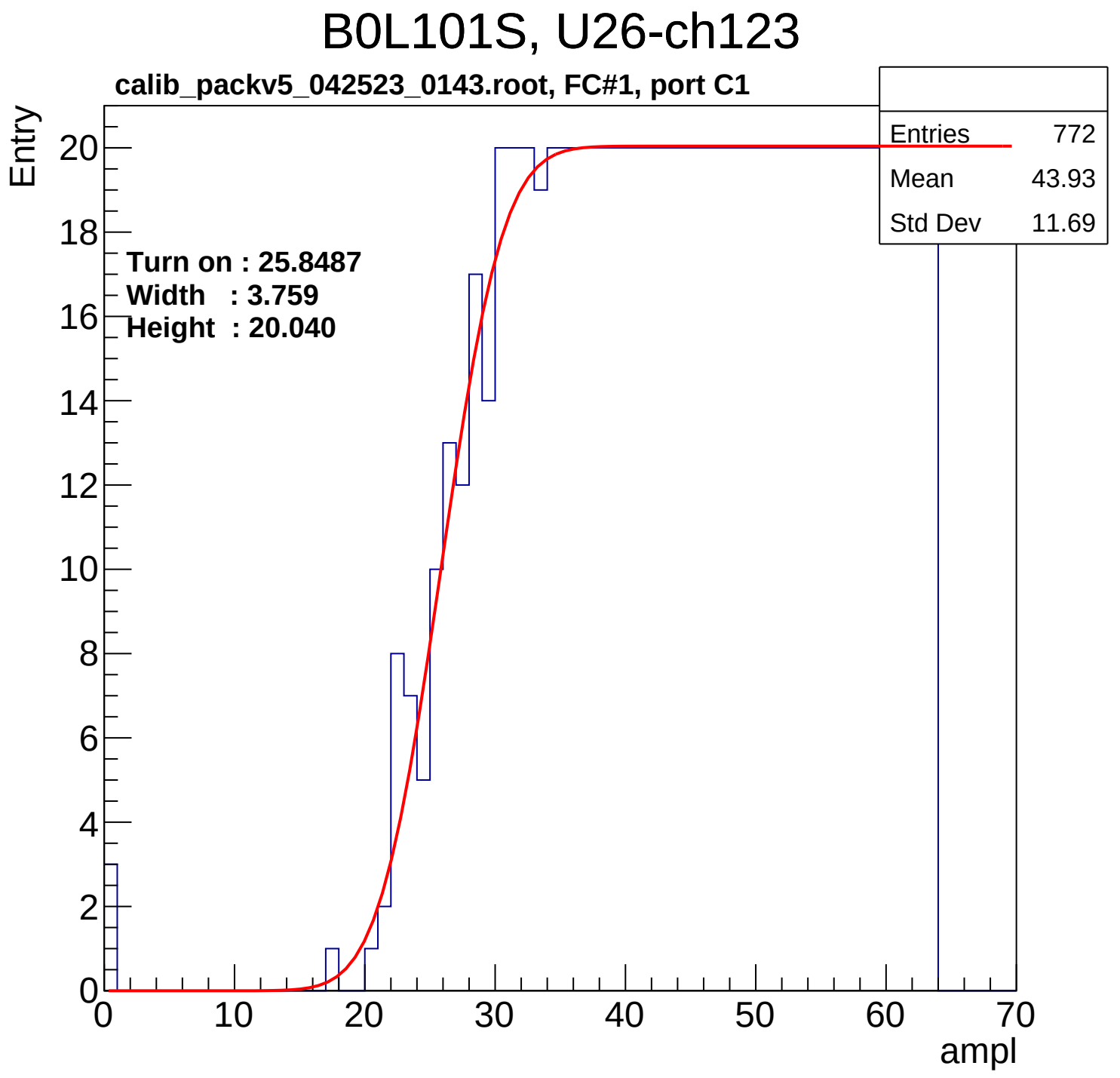
B0L101S, U26-ch123
calib_packv5_042523_0143.root, FC#1, port C1
Entries 772
Mean 43.93
Std Dev 11.69
Turn on : 25.8487
Width : 3.759
Height : 20.040
Entry
ampl
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4
6
8
10
12
14
16
18
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0
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60
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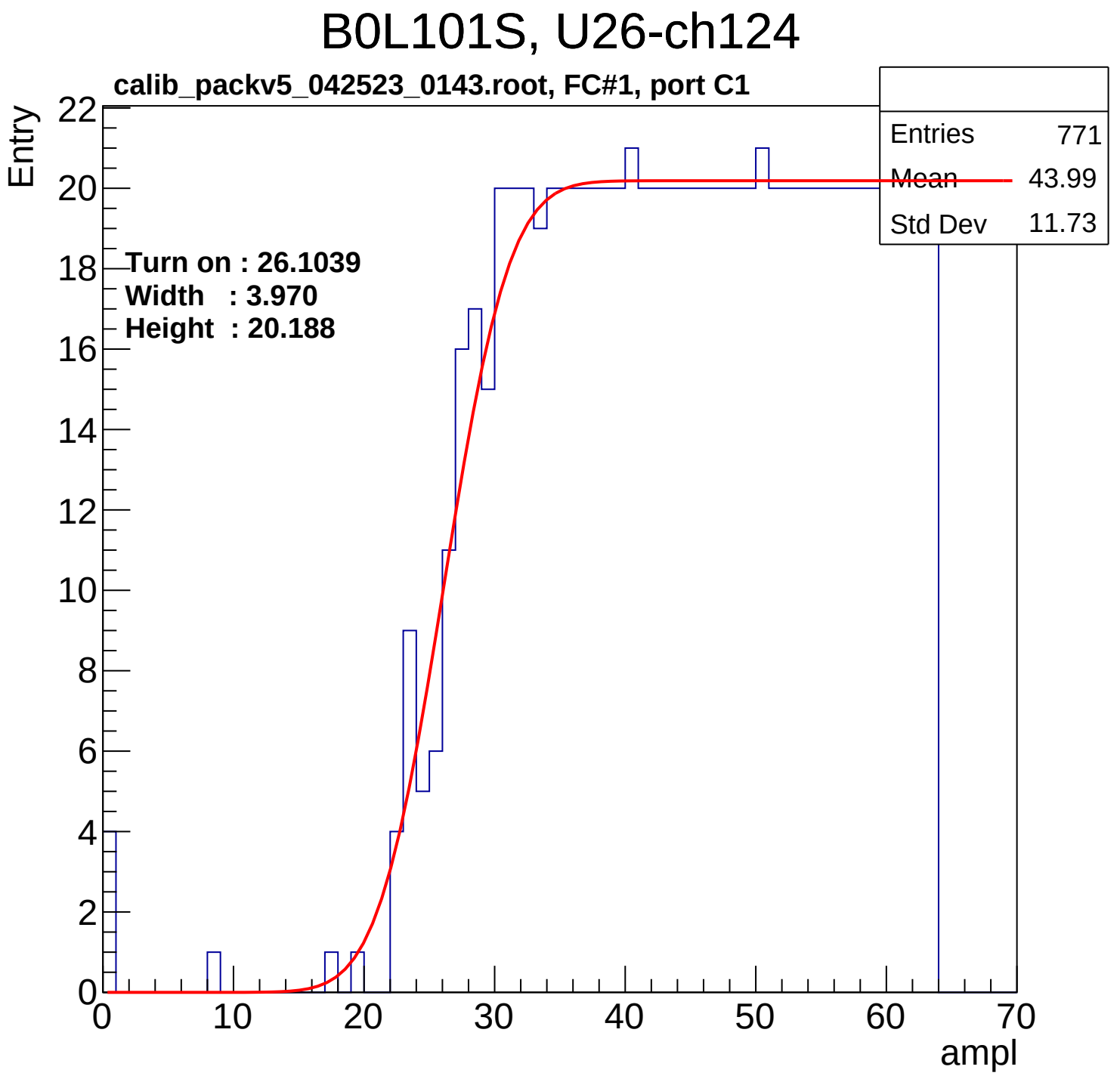
B0L101S, U26-ch124
calib_packv5_042523_0143.root, FC#1, port C1
Entries 771
Mean 43.99
Std Dev 11.73
Turn on : 26.1039
Width : 3.970
Height : 20.188
Entry
ampl
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6
8
10
12
14
16
18
20
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60
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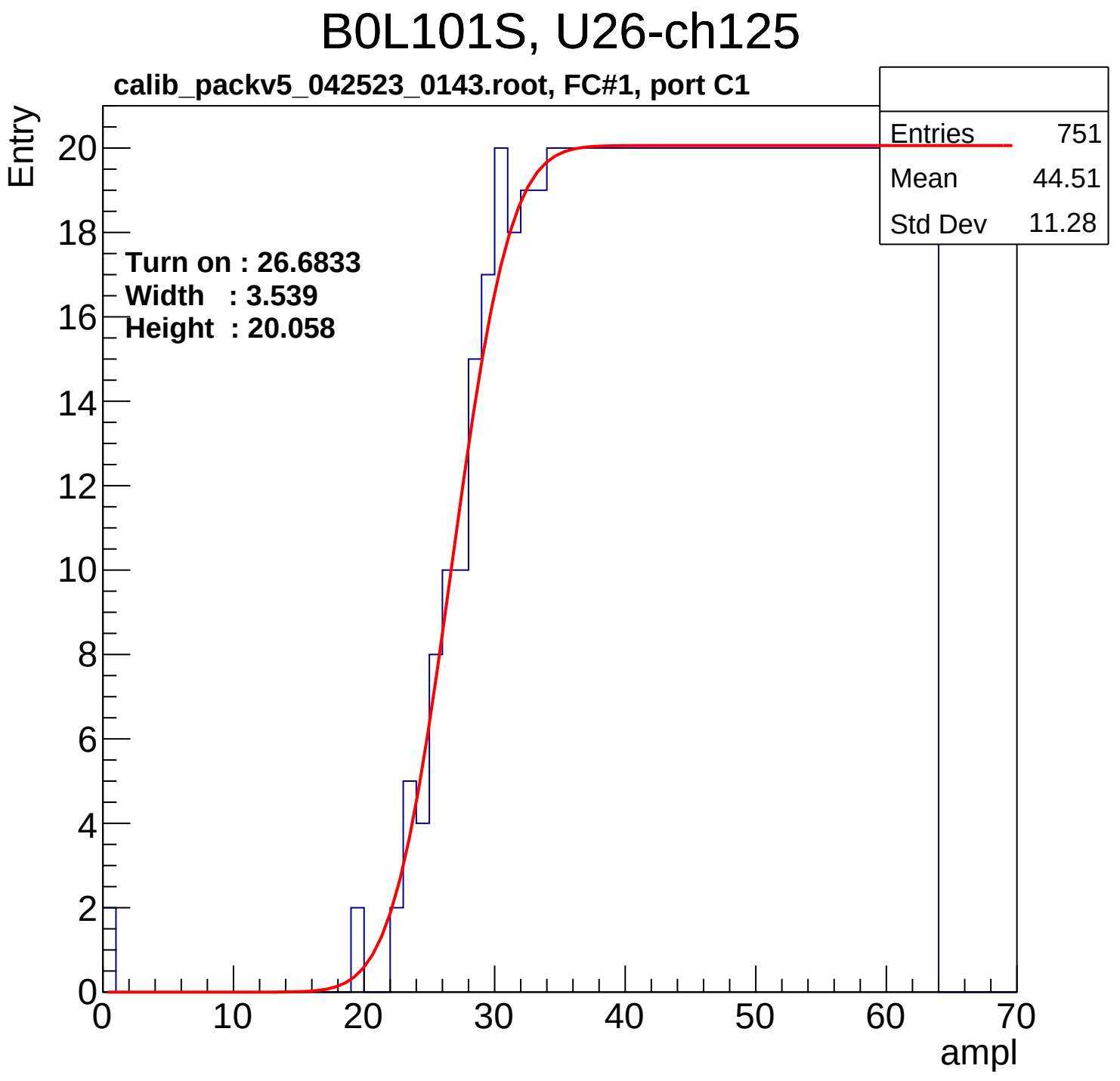
B0L101S, U26-ch125
calib_packv5_042523_0143.root, FC#1, port C1
Entries 751
Mean 44.51
Std Dev 11.28
Turn on : 26.6833
Width : 3.539
Height : 20.058
Entry
ampl
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6
8
10
12
14
16
18
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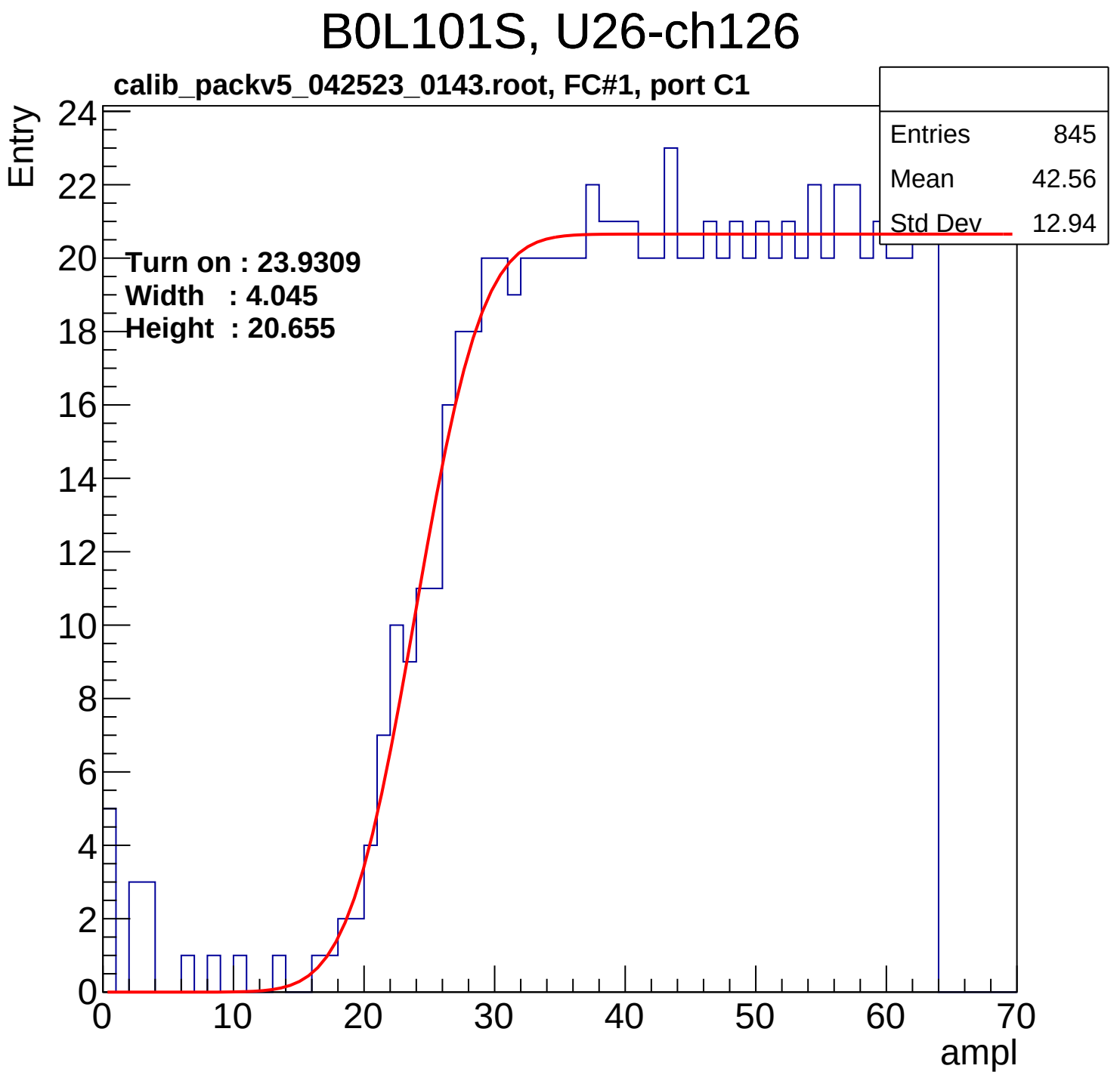
B0L101S, U26-ch126
calib_packv5_042523_0143.root, FC#1, port C1
Entries 845
Mean 42.56
Std Dev 12.94
Turn on : 23.9309
Width : 4.045
Height : 20.655
Entry
ampl
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10
12
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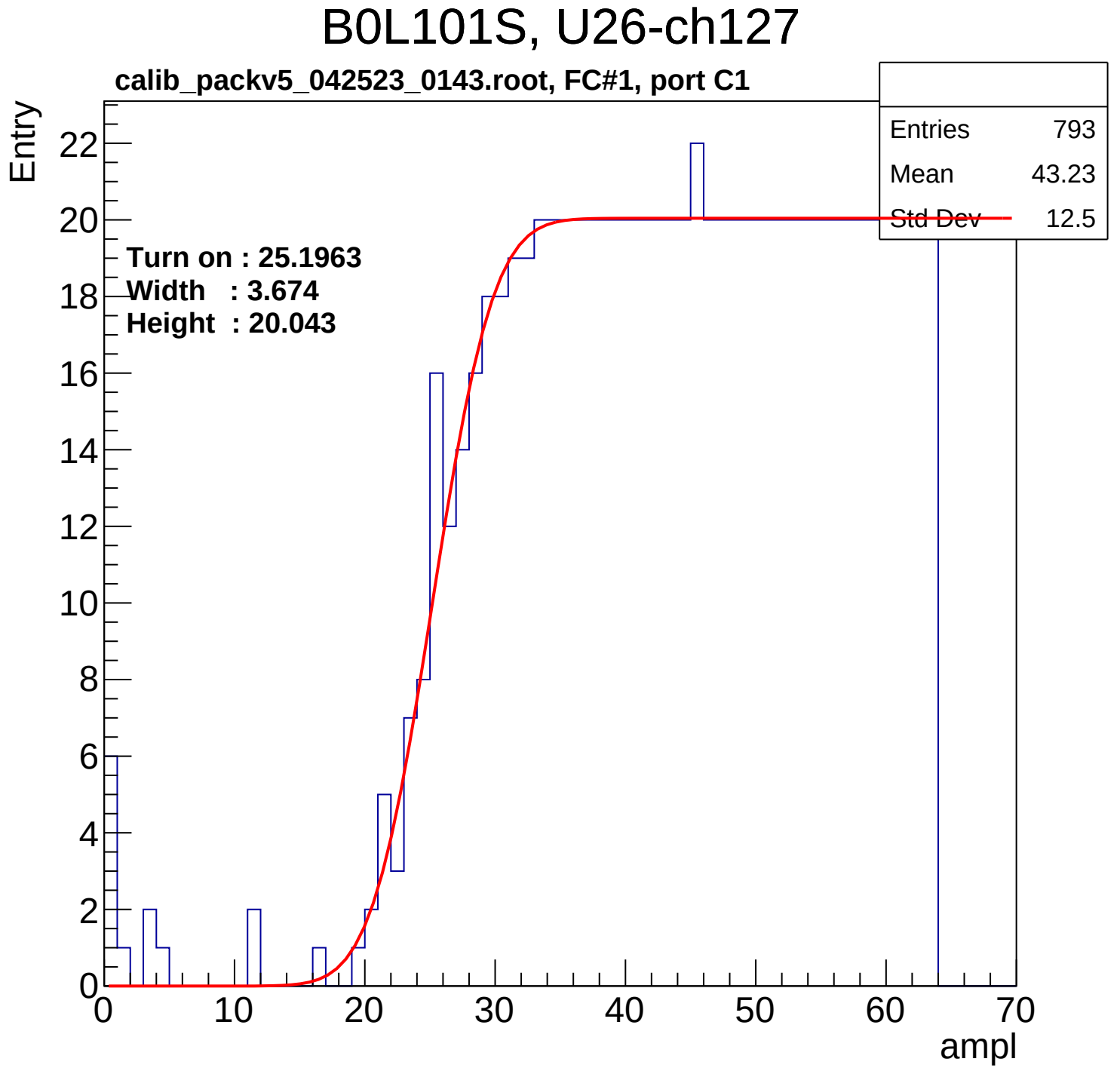
B0L101S, U26-ch127
calib_packv5_042523_0143.root, FC#1, port C1
Entries 793
Mean 43.23
Std Dev 12.5
Turn on : 25.1963
Width : 3.674
Height : 20.043
Entry
ampl
0
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8
10
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20
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0
10
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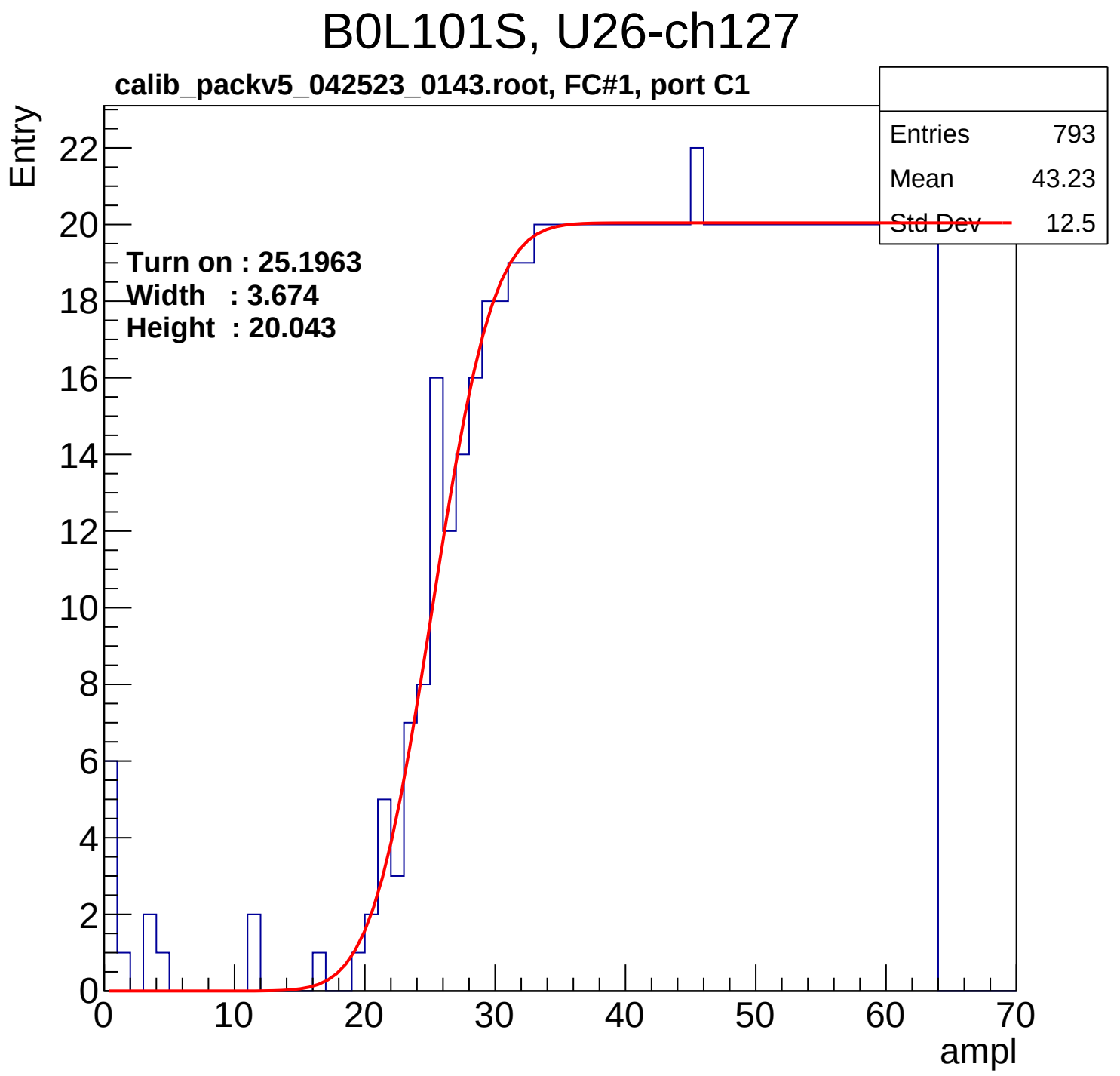
70


B0L101S, U26-ch127
calib_packv5_042523_0143.root, FC#1, port C1
Entries 793
Mean 43.23
Std Dev 12.5
Turn on : 25.1963
Width : 3.674
Height : 20.043
Entry
ampl
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6
8
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14
16
18
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