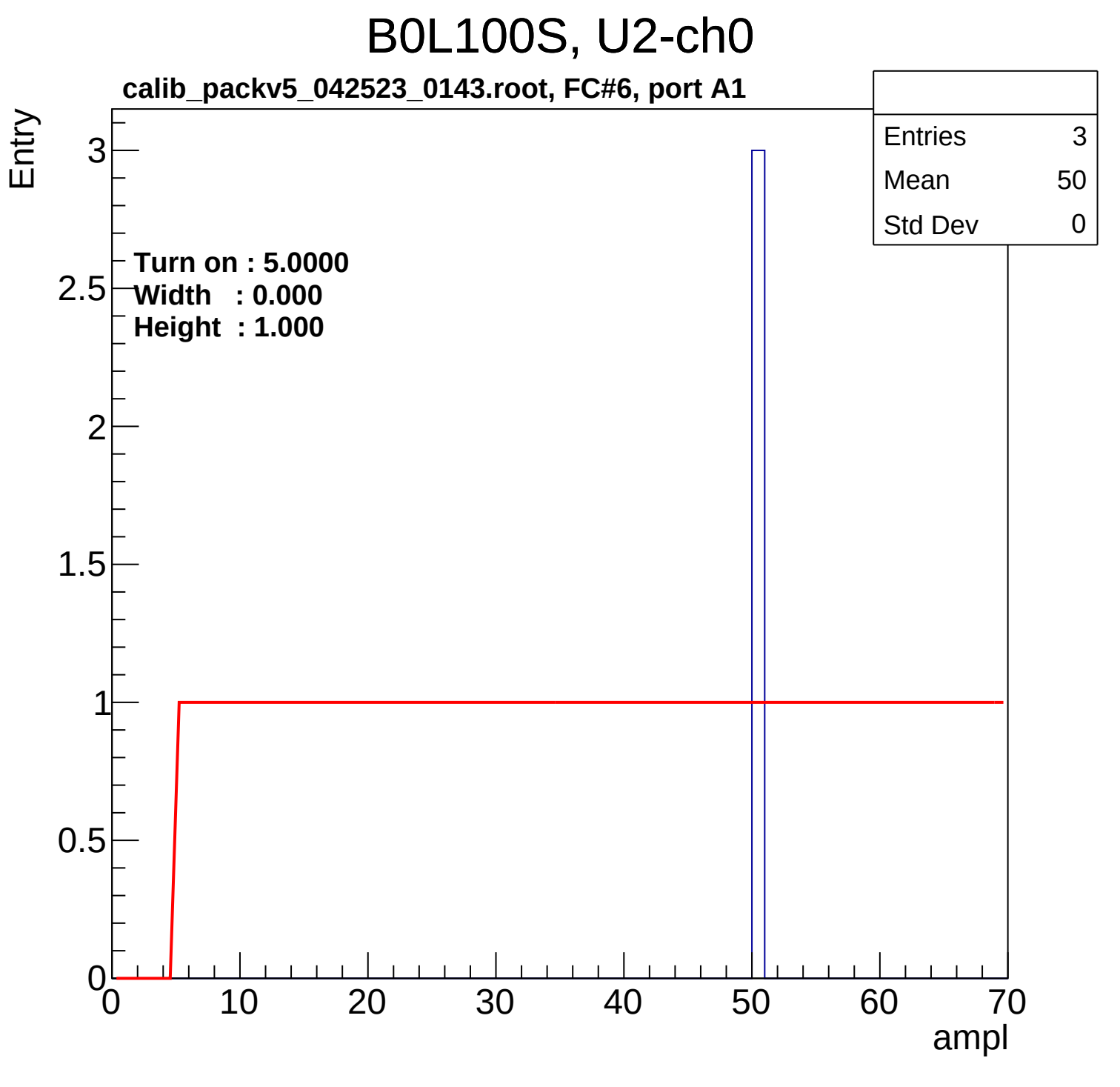
B0L100S, U2-ch0
calib_packv5_042523_0143.root, FC#6, port A1
Entries 3
Mean 50
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
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60
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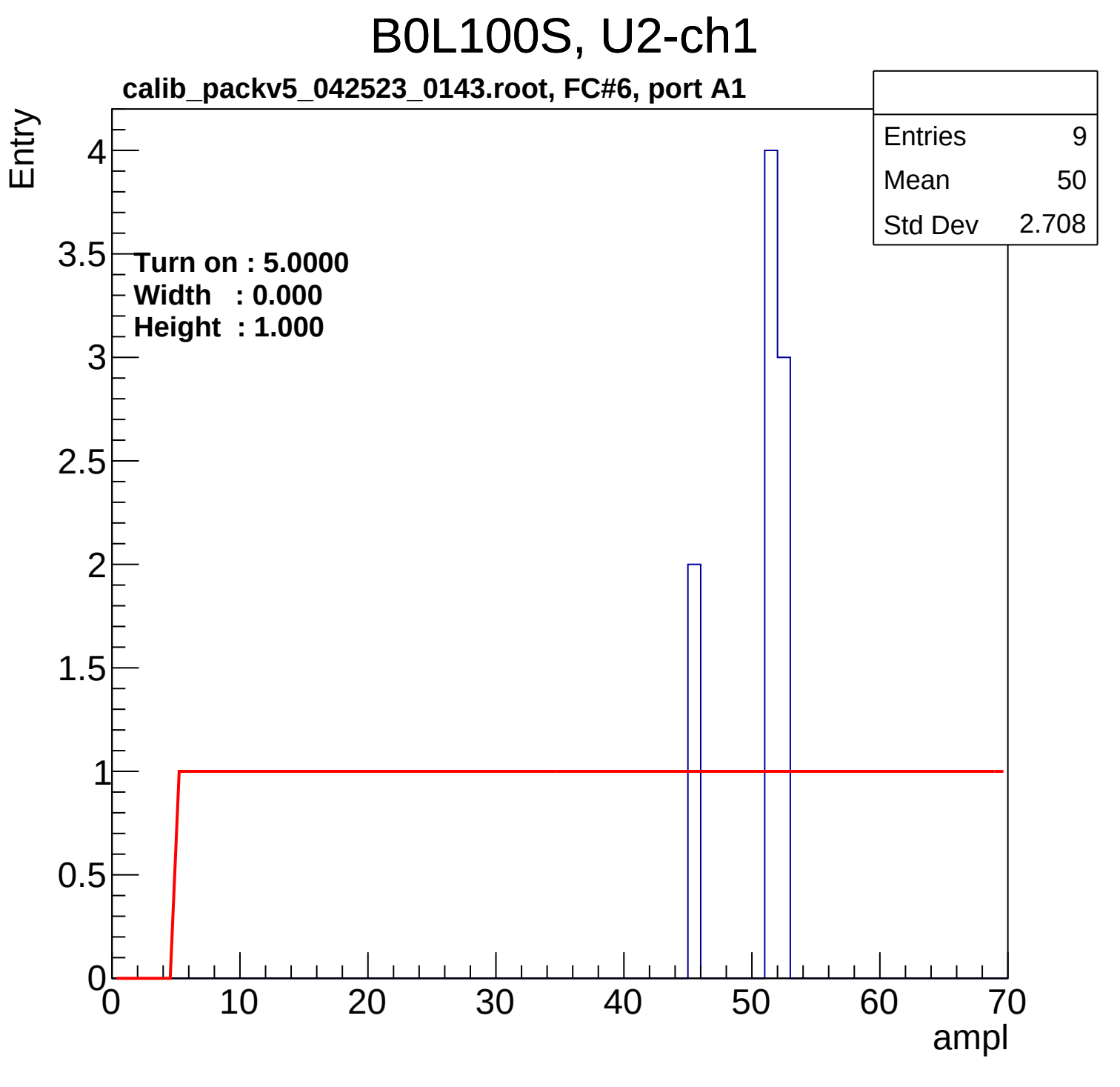
B0L100S, U2-ch1
calib_packv5_042523_0143.root, FC#6, port A1
Entries 9
Mean 50
Std Dev 2.708
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
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60
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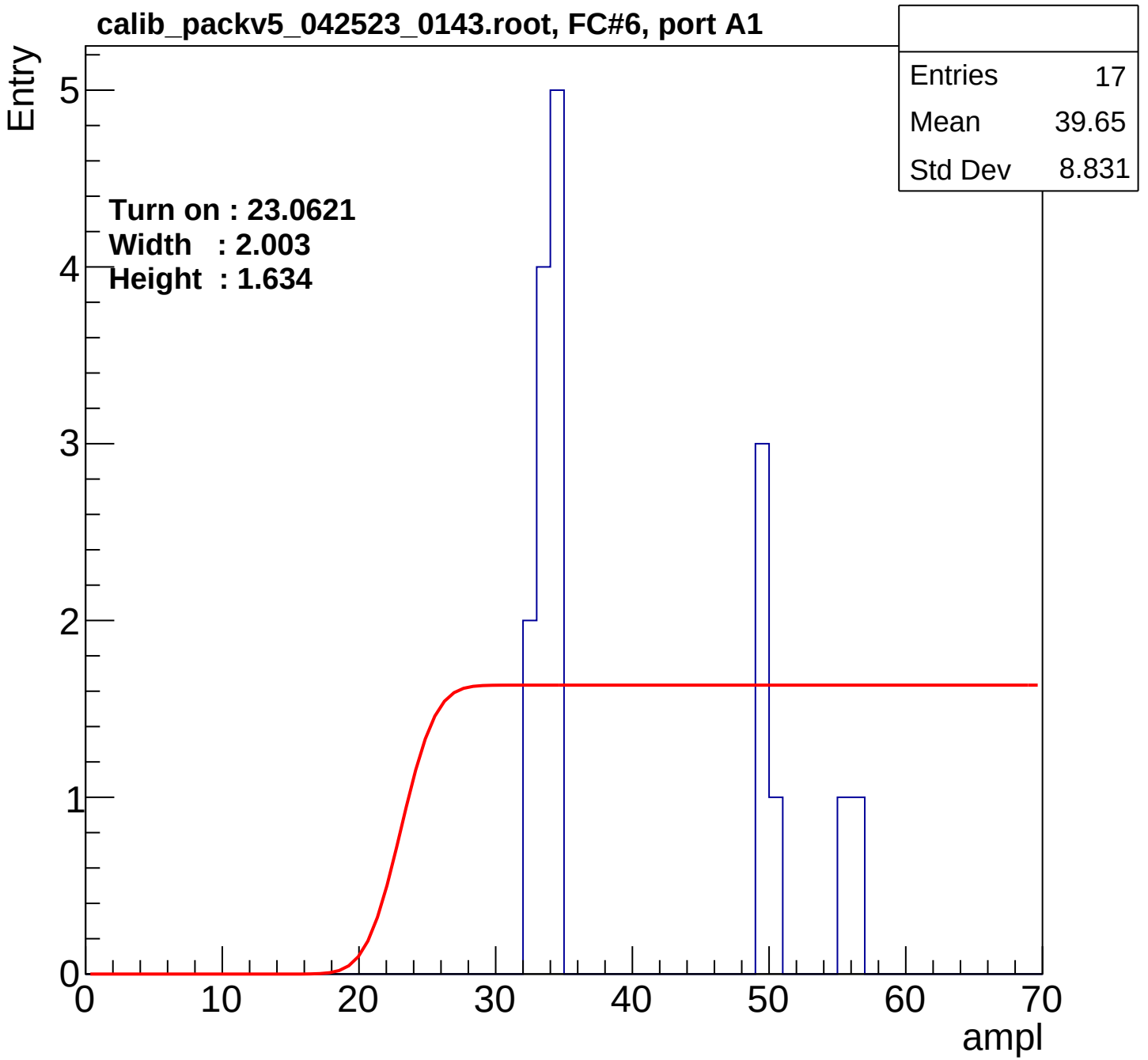
B0L100S, U2-ch2
calib_packv5_042523_0143.root, FC#6, port A1
Entries 17
Mean 39.65
Std Dev 8.831
Turn on : 23.0621
Width : 2.003
Height : 1.634
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
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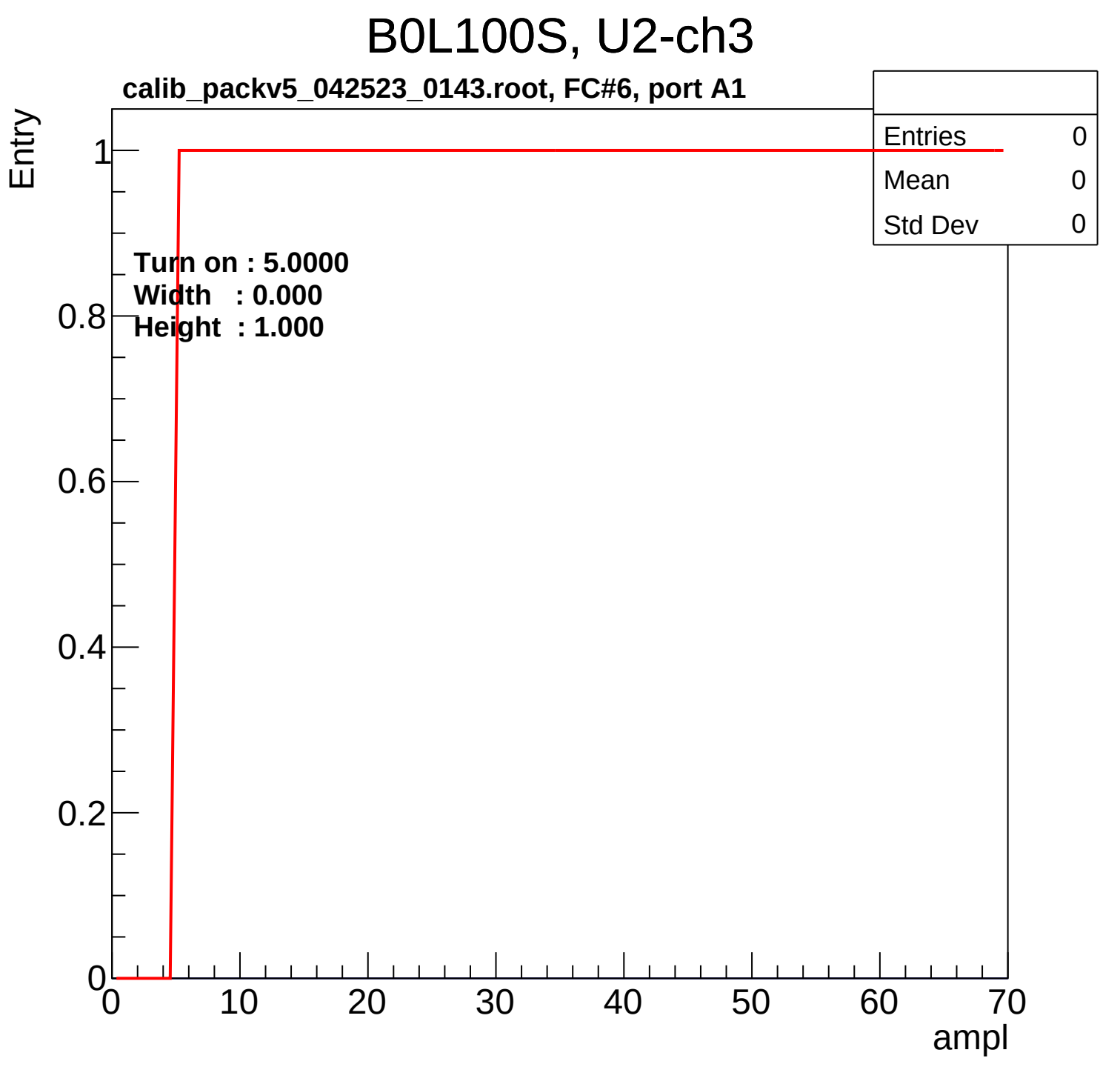
B0L100S, U2-ch3
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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0.8
0.6
0.4
0.2
0
0
10
20
30
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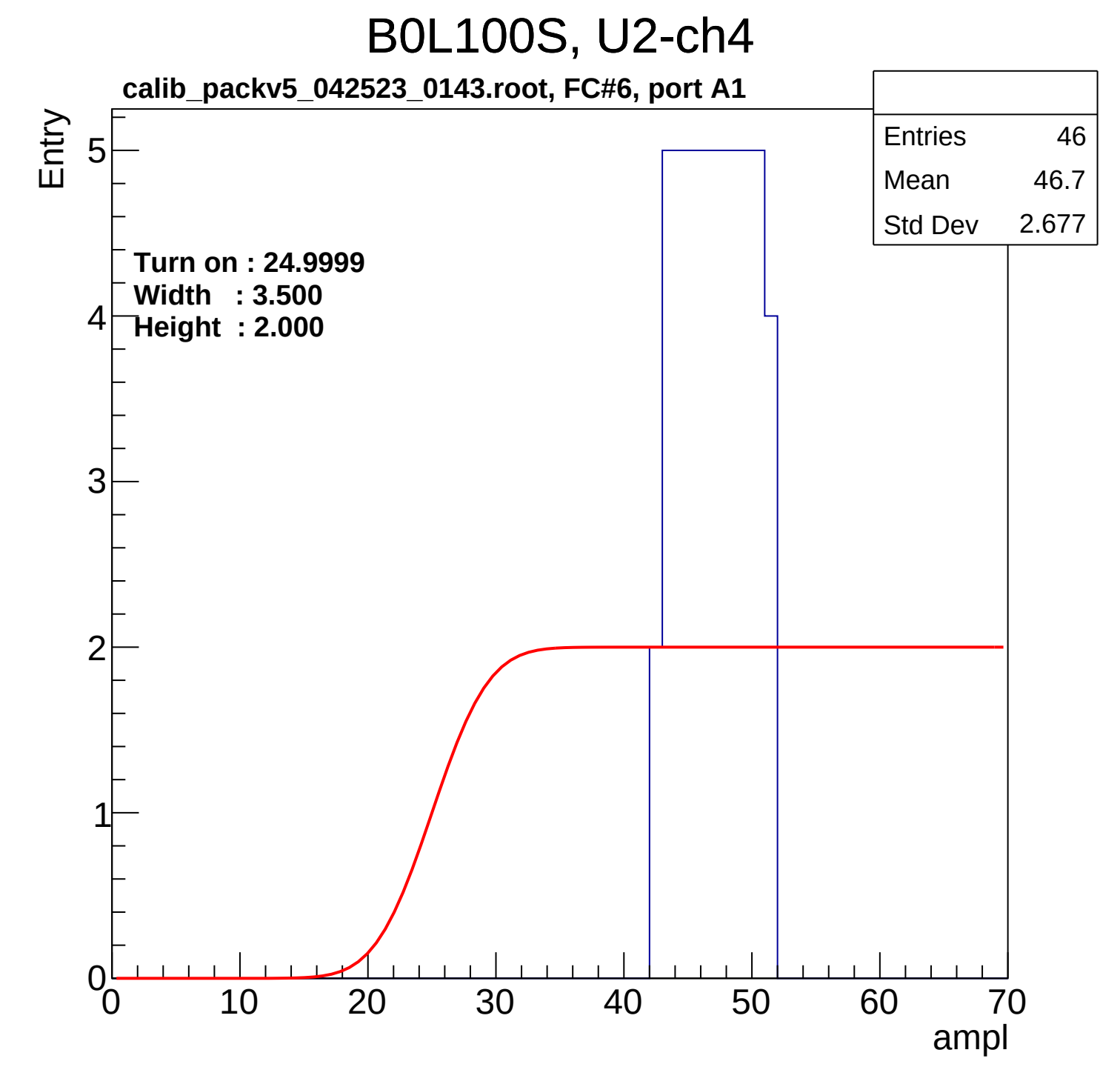
50
60
70
ampl


B0L100S, U2-ch4
calib_packv5_042523_0143.root, FC#6, port A1
Entries 46
Mean 46.7
Std Dev 2.677
Turn on : 24.9999
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
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40
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60
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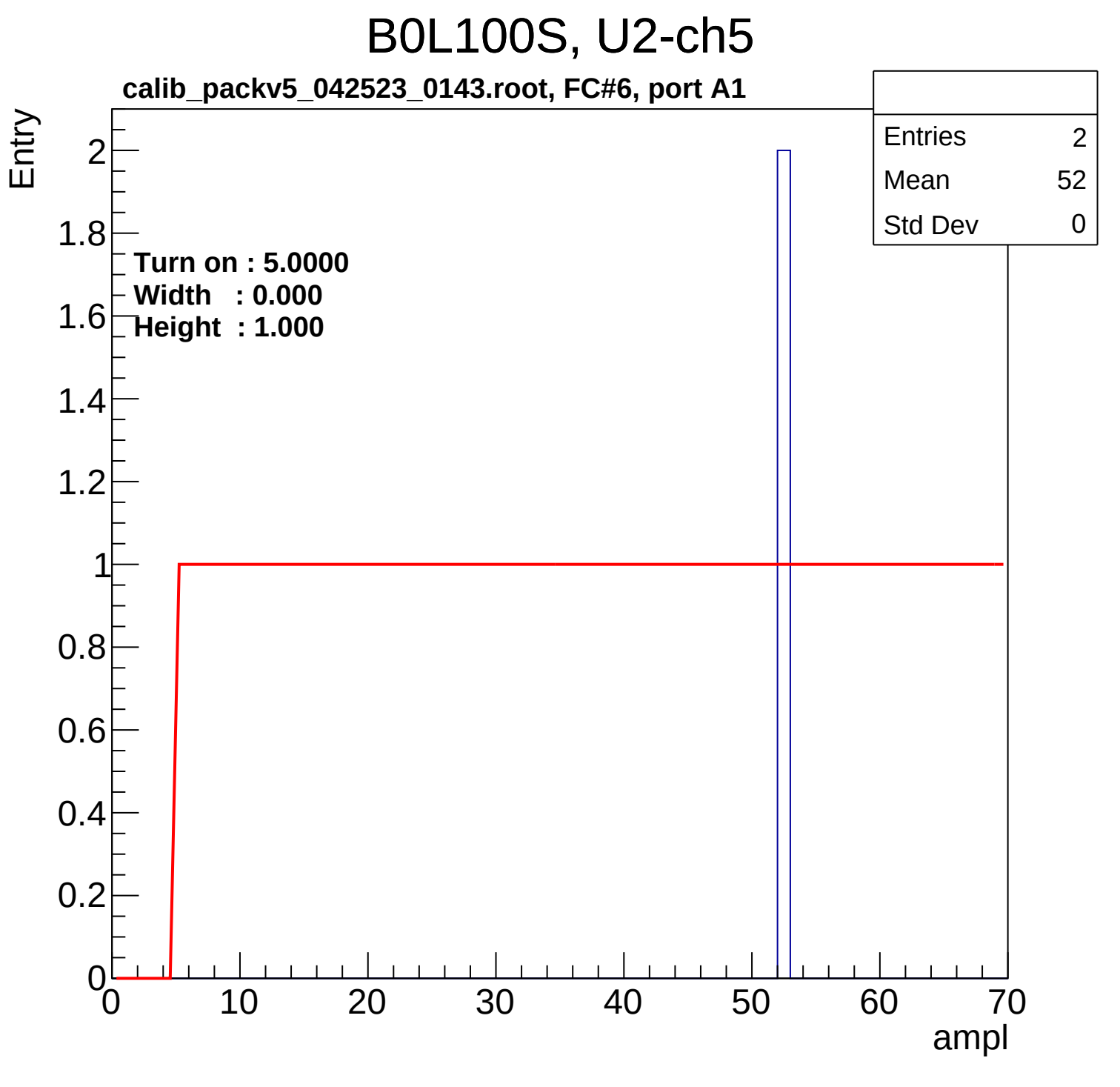
B0L100S, U2-ch5
calib_packv5_042523_0143.root, FC#6, port A1
Entries 2
Mean 52
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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40
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60
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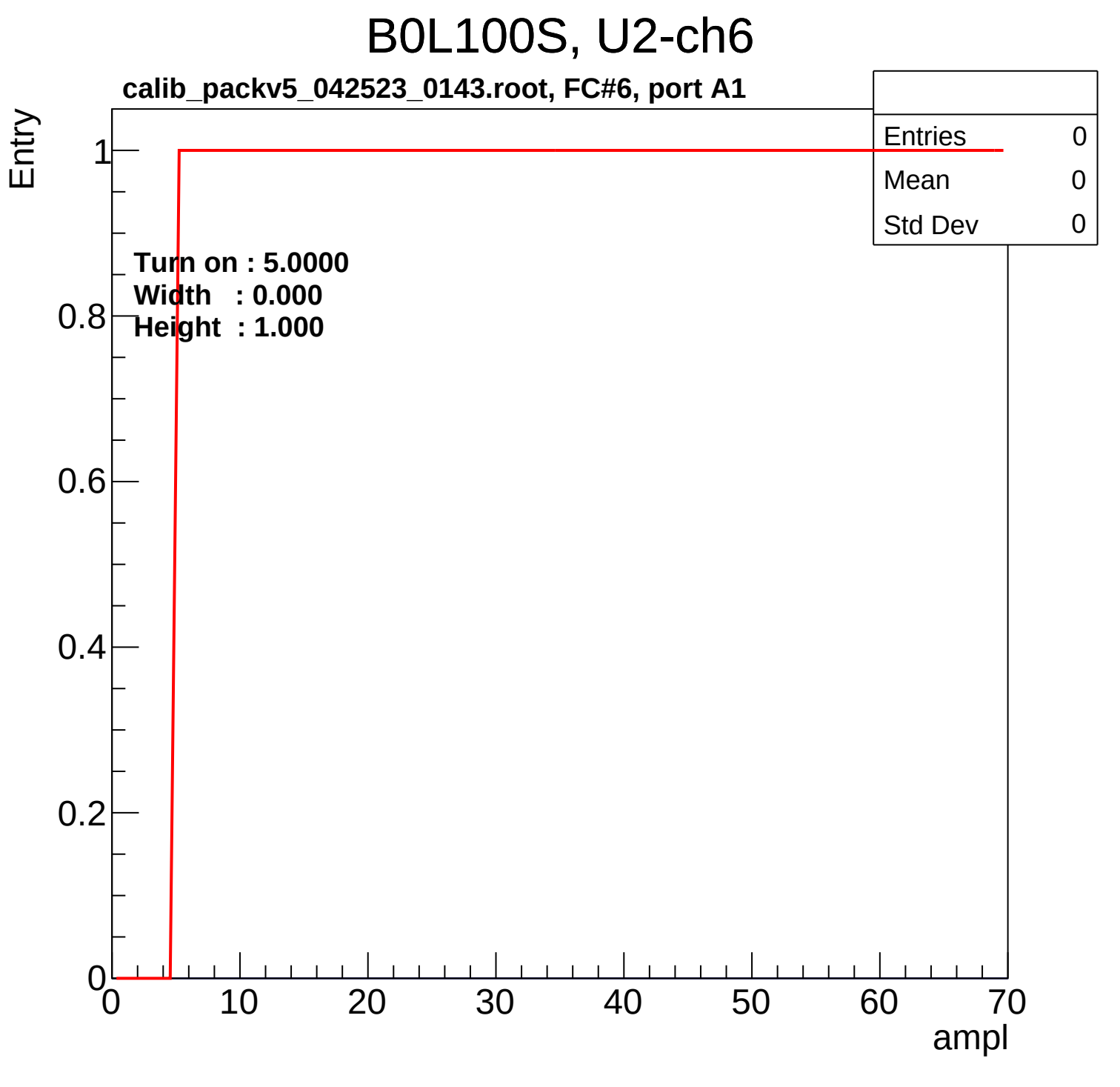
B0L100S, U2-ch6
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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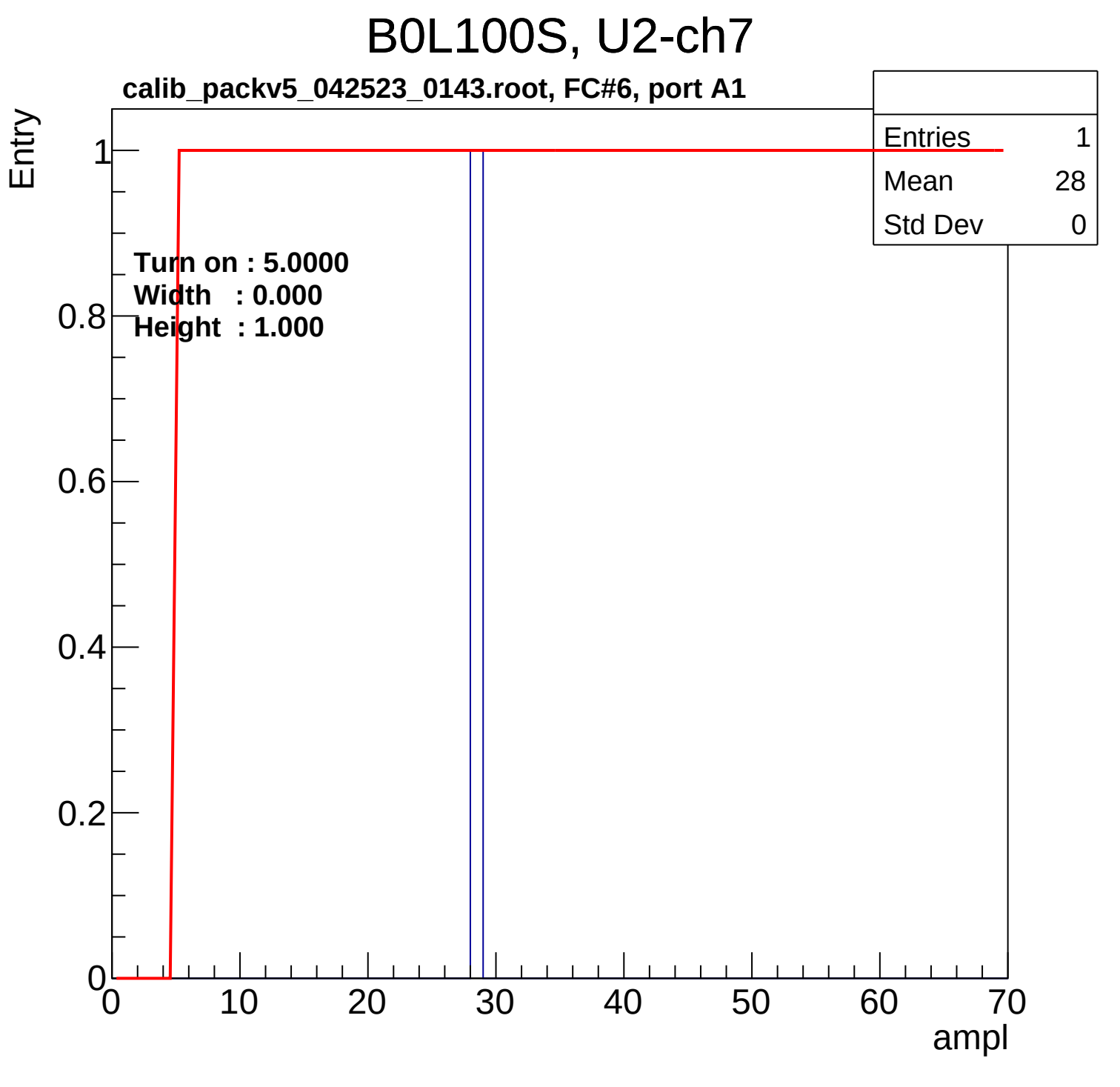
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U2-ch7
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 28
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
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40
50
60
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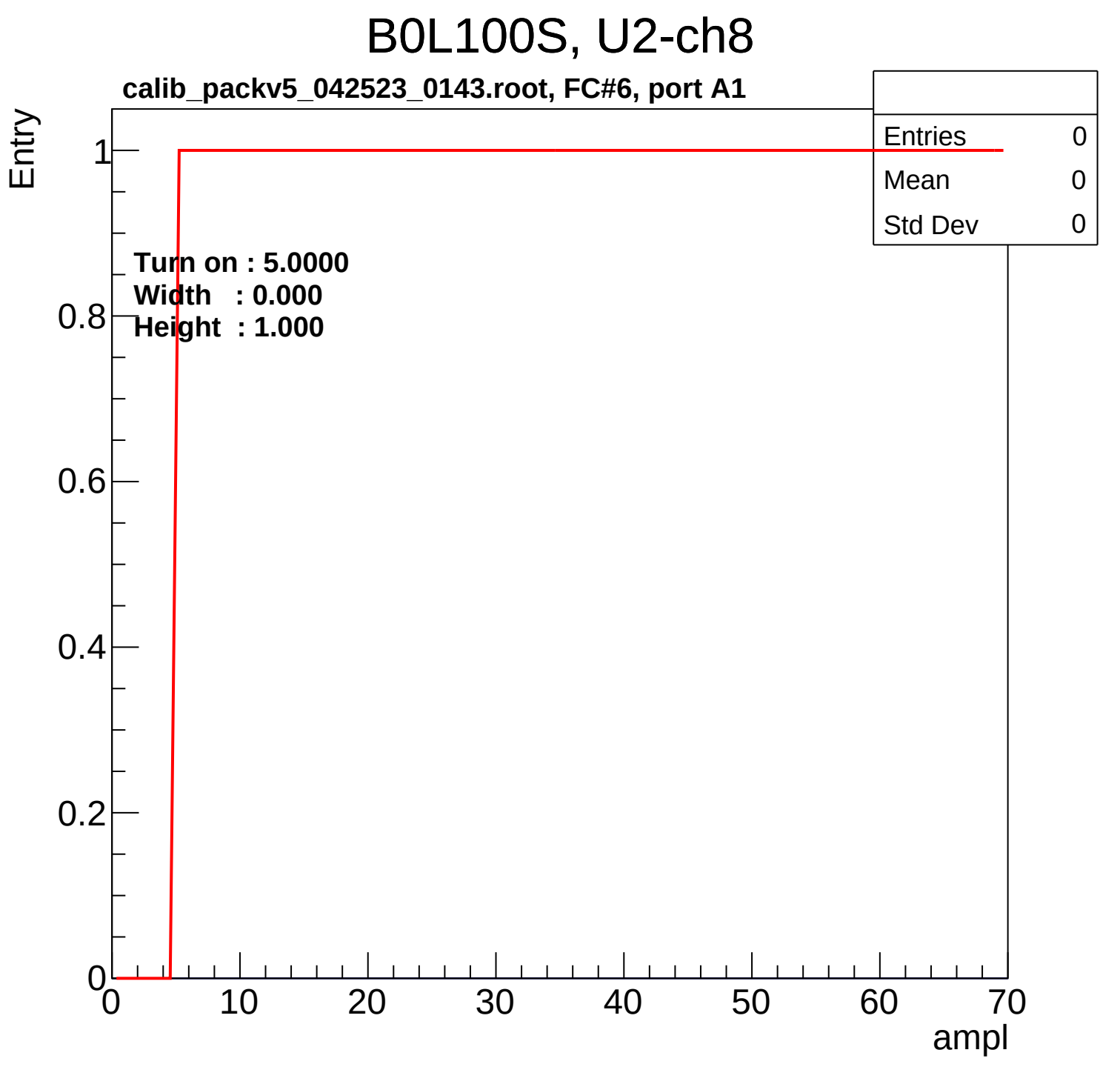
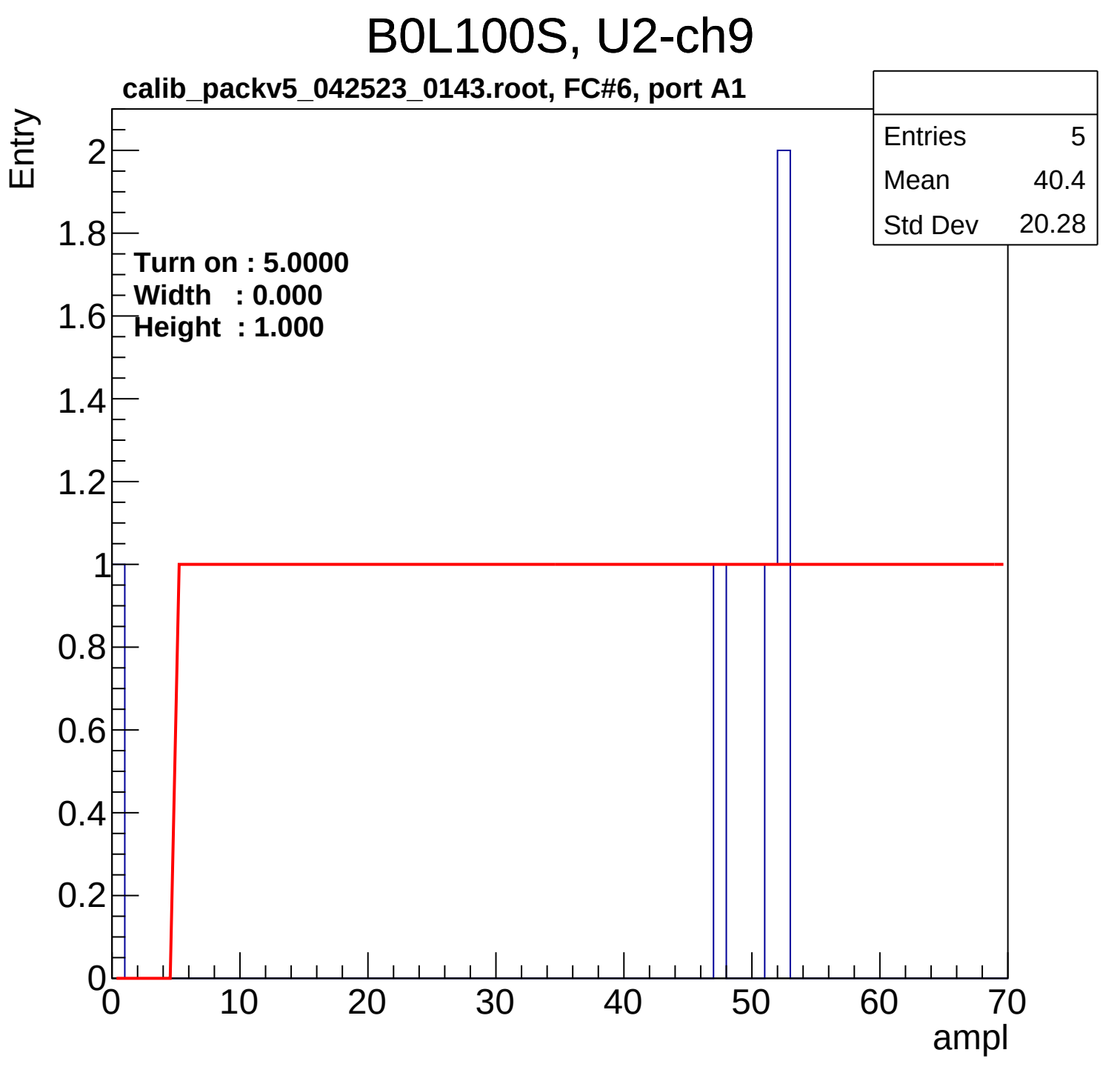

B0L100S, U2-ch8
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U2-ch9
calib_packv5_042523_0143.root, FC#6, port A1
Entries 5
Mean 40.4
Std Dev 20.28
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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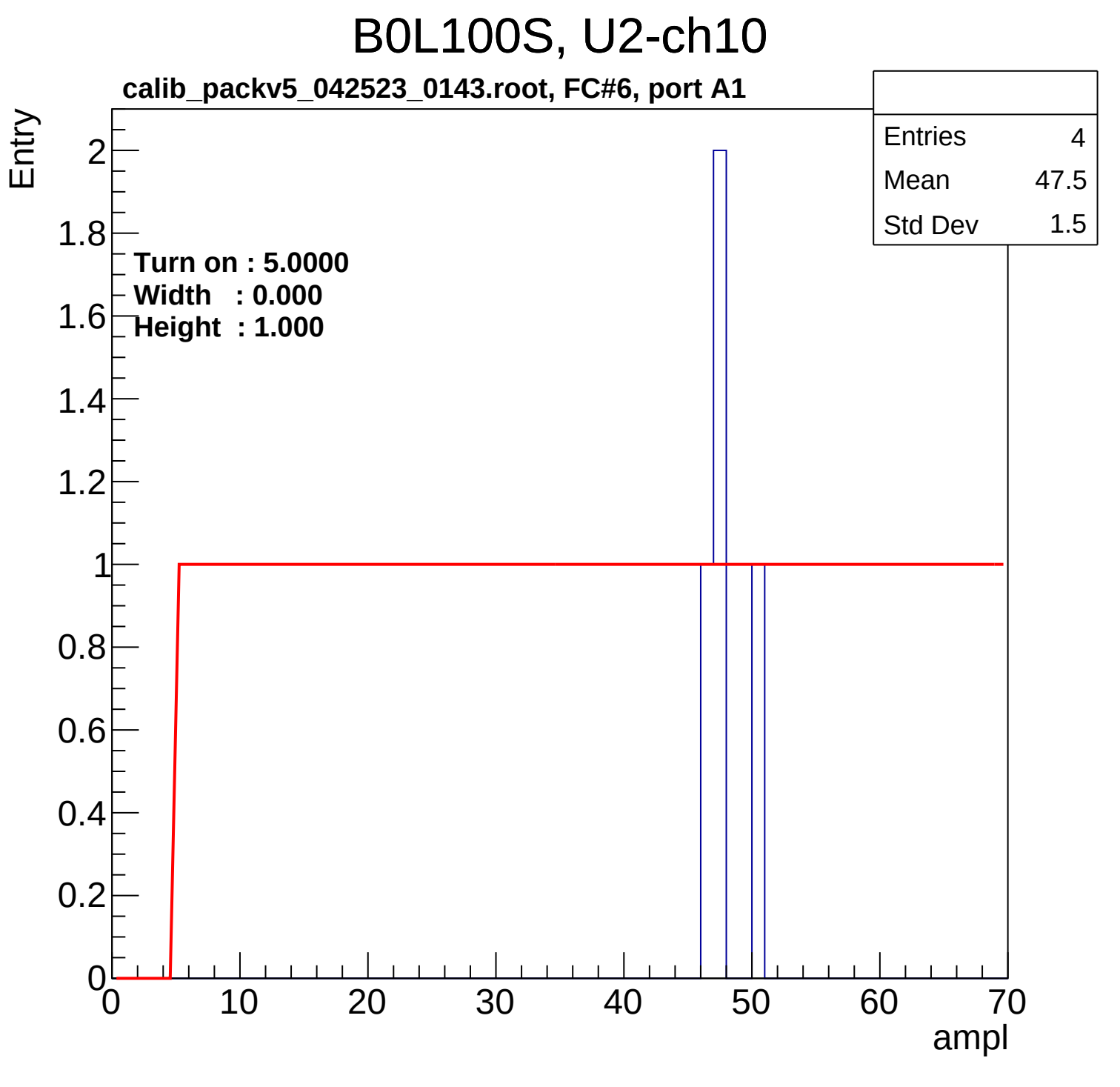
B0L100S, U2-ch10
calib_packv5_042523_0143.root, FC#6, port A1
Entries 4
Mean 47.5
Std Dev 1.5
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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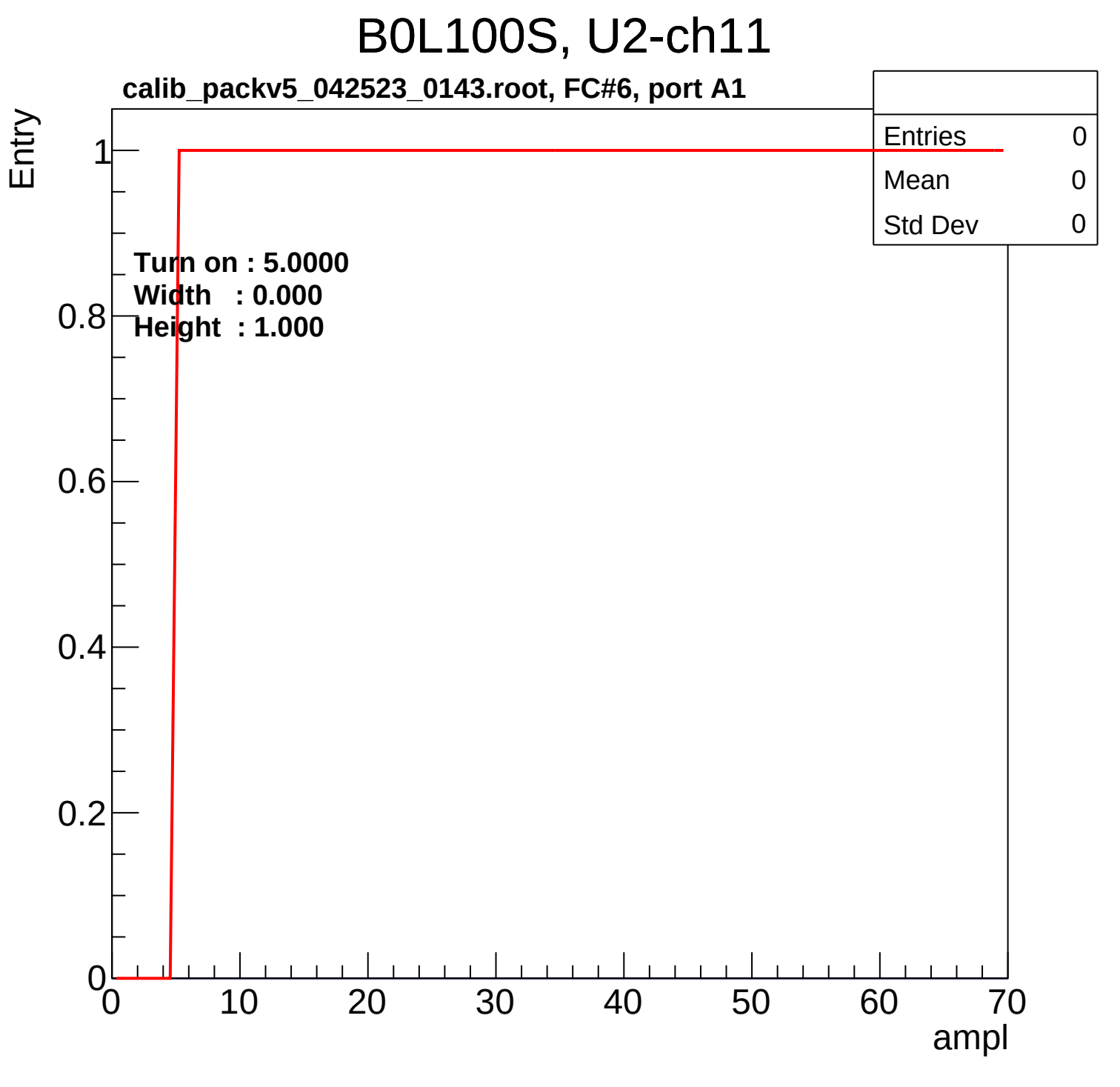
B0L100S, U2-ch11
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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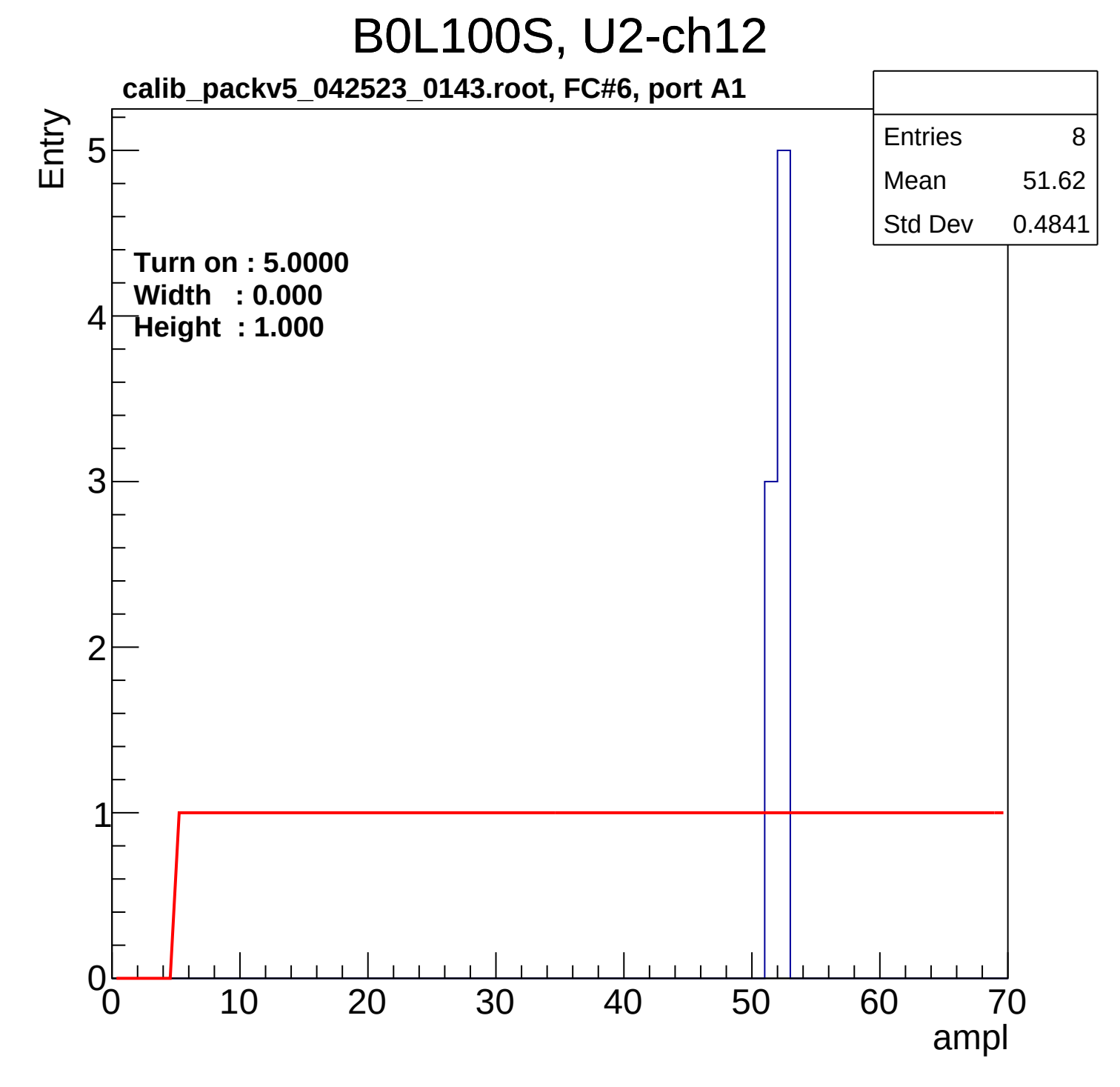
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U2-ch12
calib_packv5_042523_0143.root, FC#6, port A1
Entries 8
Mean 51.62
Std Dev 0.4841
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
1
2
3
4
5
0
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60
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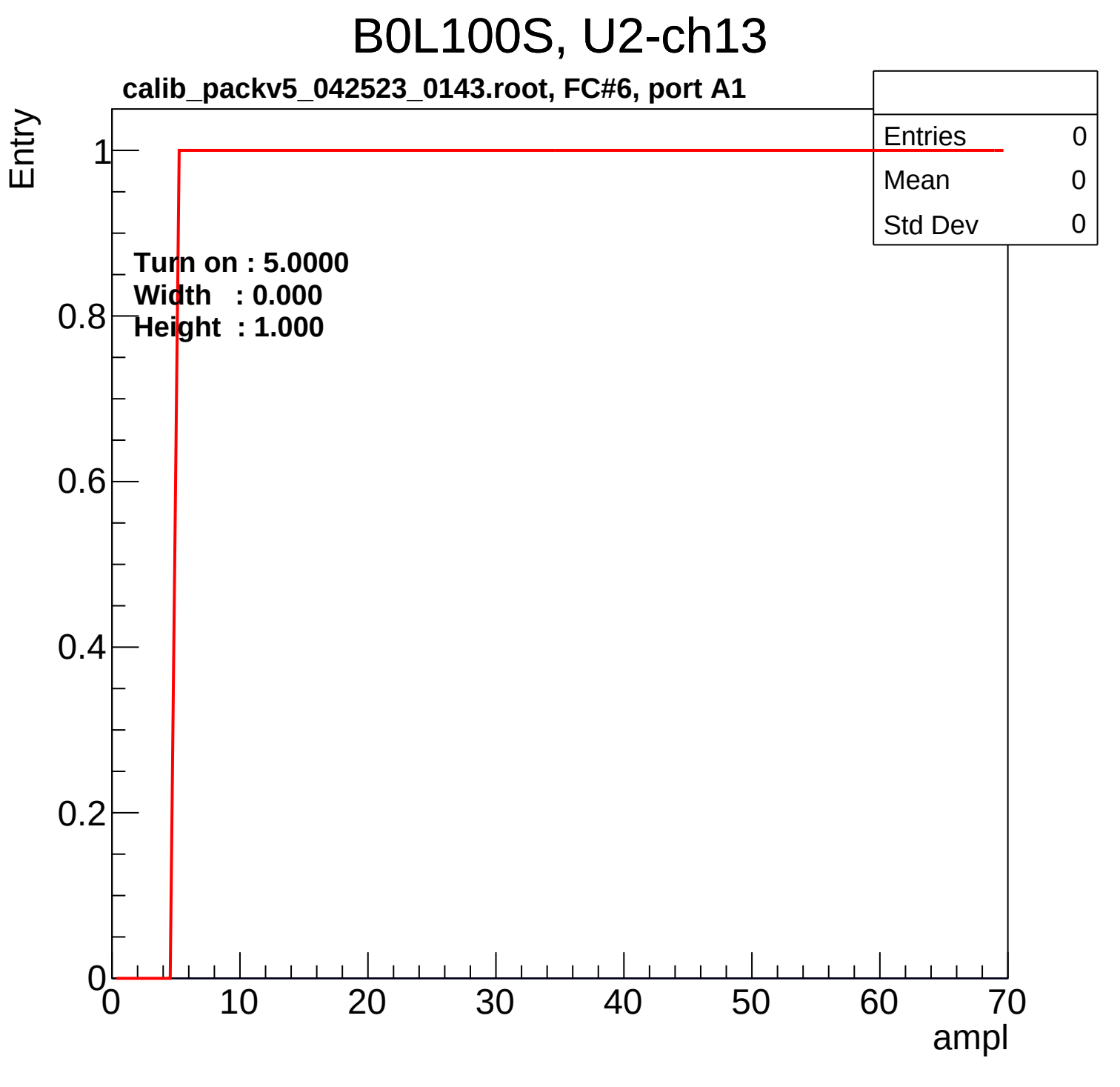
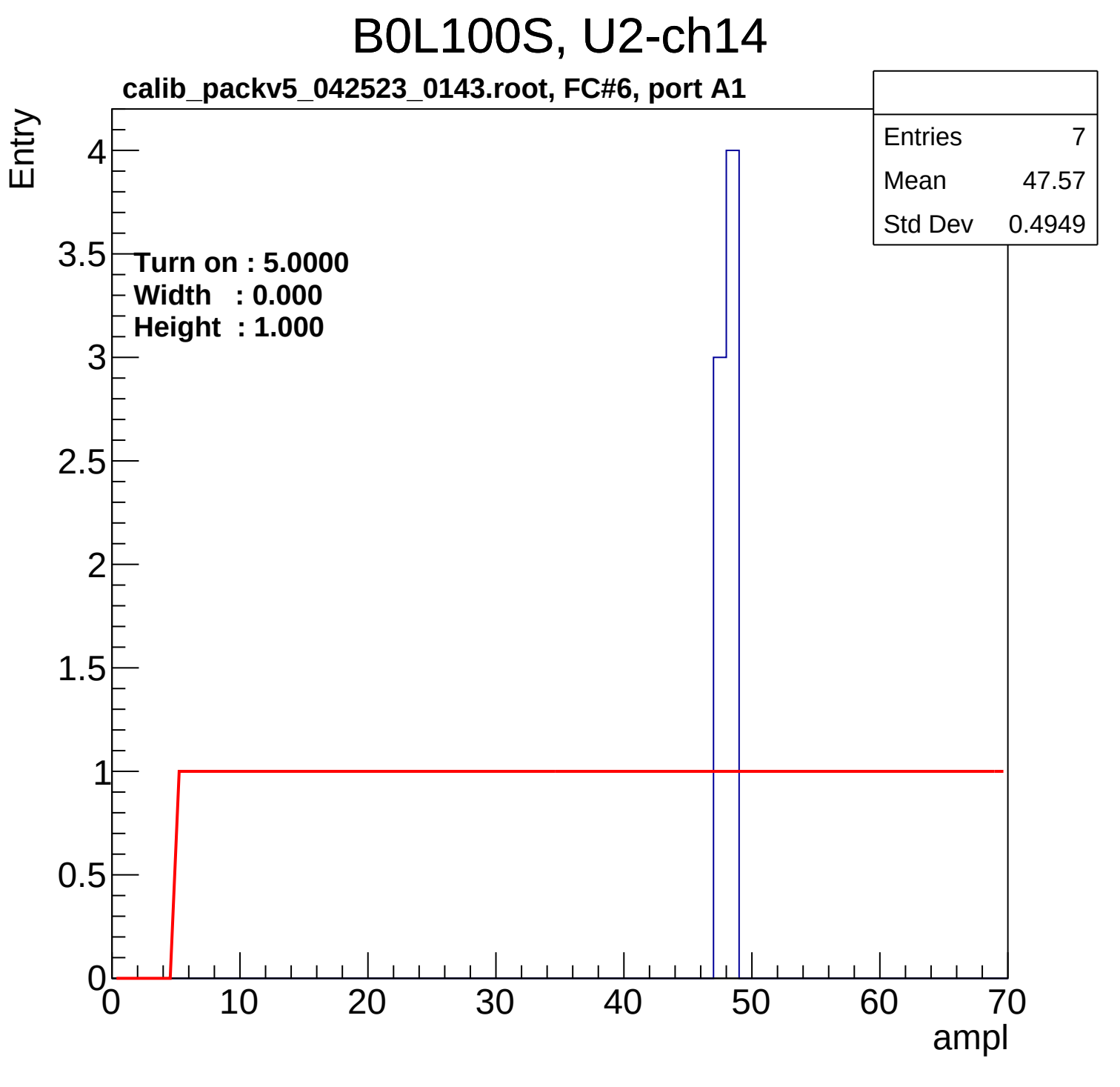

B0L100S, U2-ch13
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U2-ch14
calib_packv5_042523_0143.root, FC#6, port A1
Entries 7
Mean 47.57
Std Dev 0.4949
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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1.5
2
2.5
3
3.5
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0
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60
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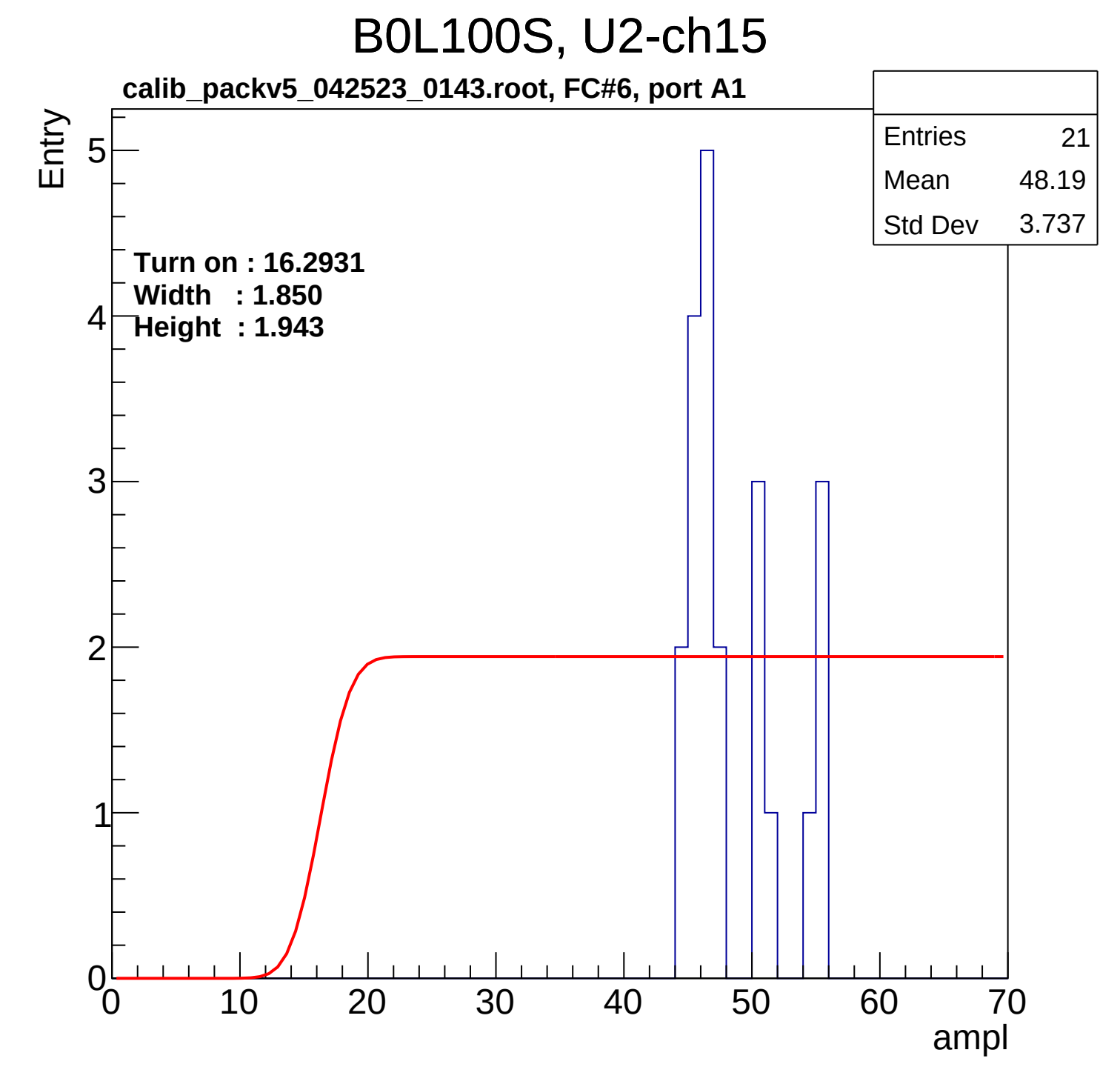
B0L100S, U2-ch15
calib_packv5_042523_0143.root, FC#6, port A1
Entries 21
Mean 48.19
Std Dev 3.737
Turn on : 16.2931
Width : 1.850
Height : 1.943
Entry
ampl
0
1
2
3
4
5
0
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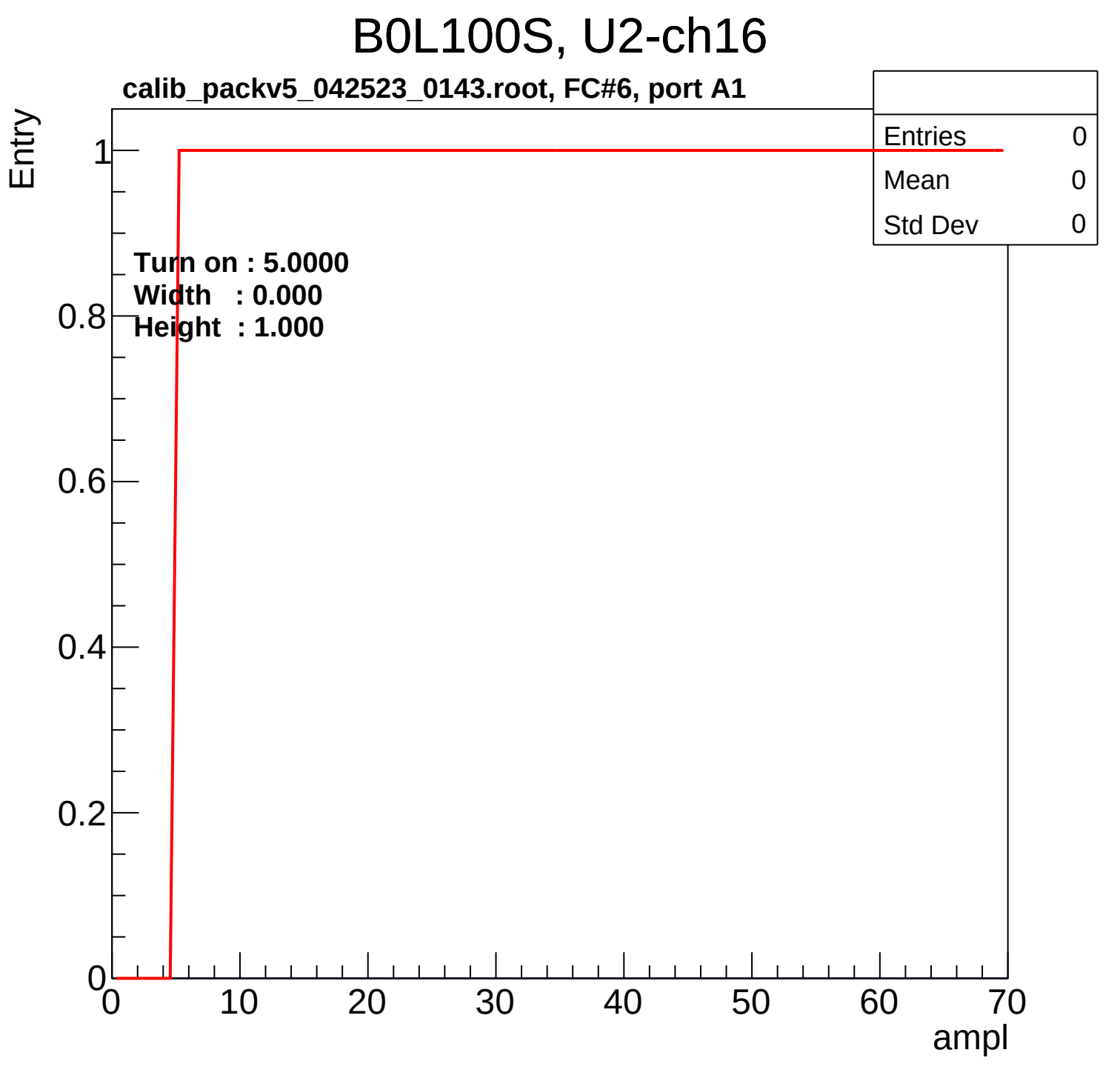
B0L100S, U2-ch16
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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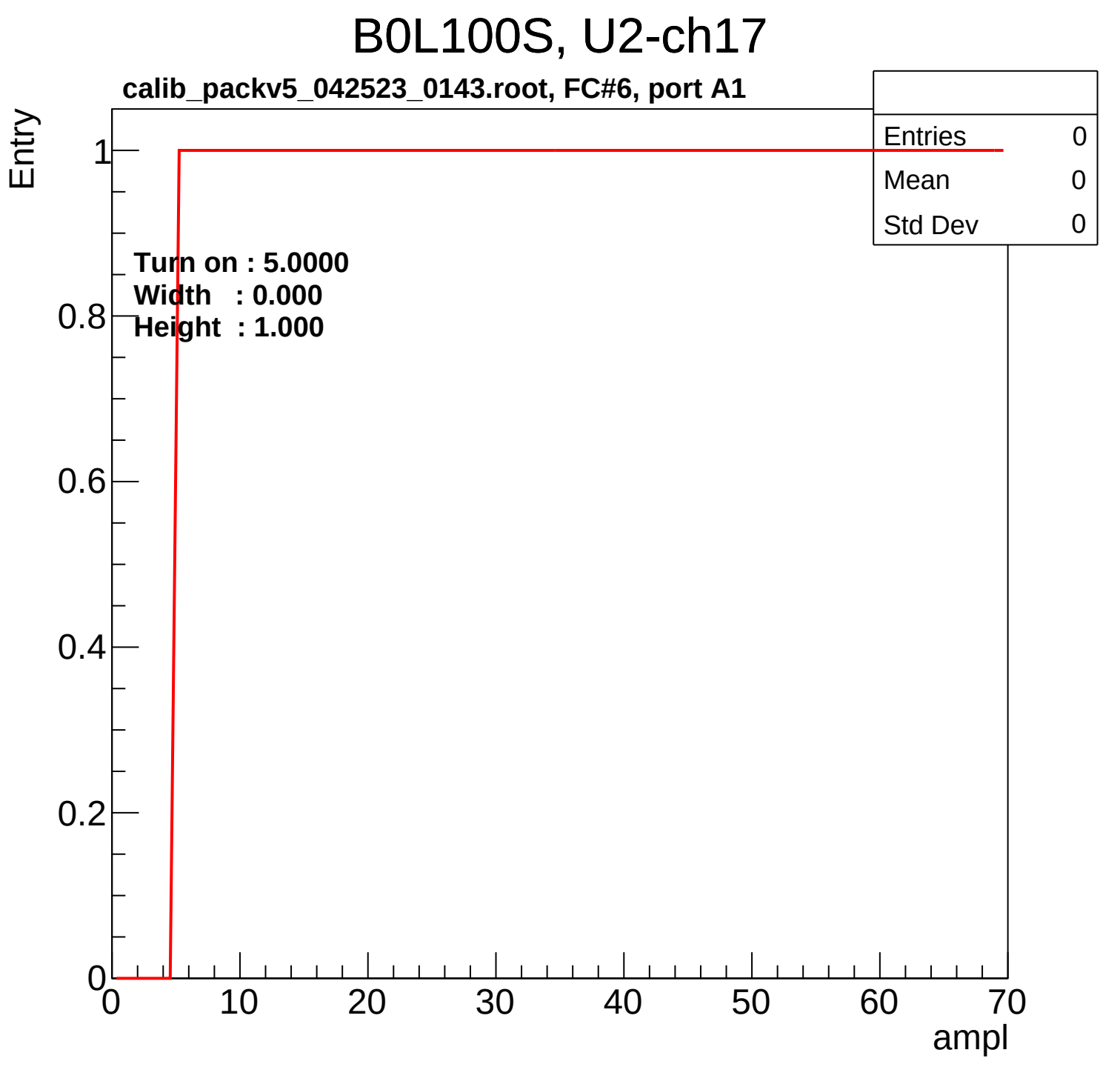
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U2-ch17
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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0.8
0.6
0.4
0.2
0
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10
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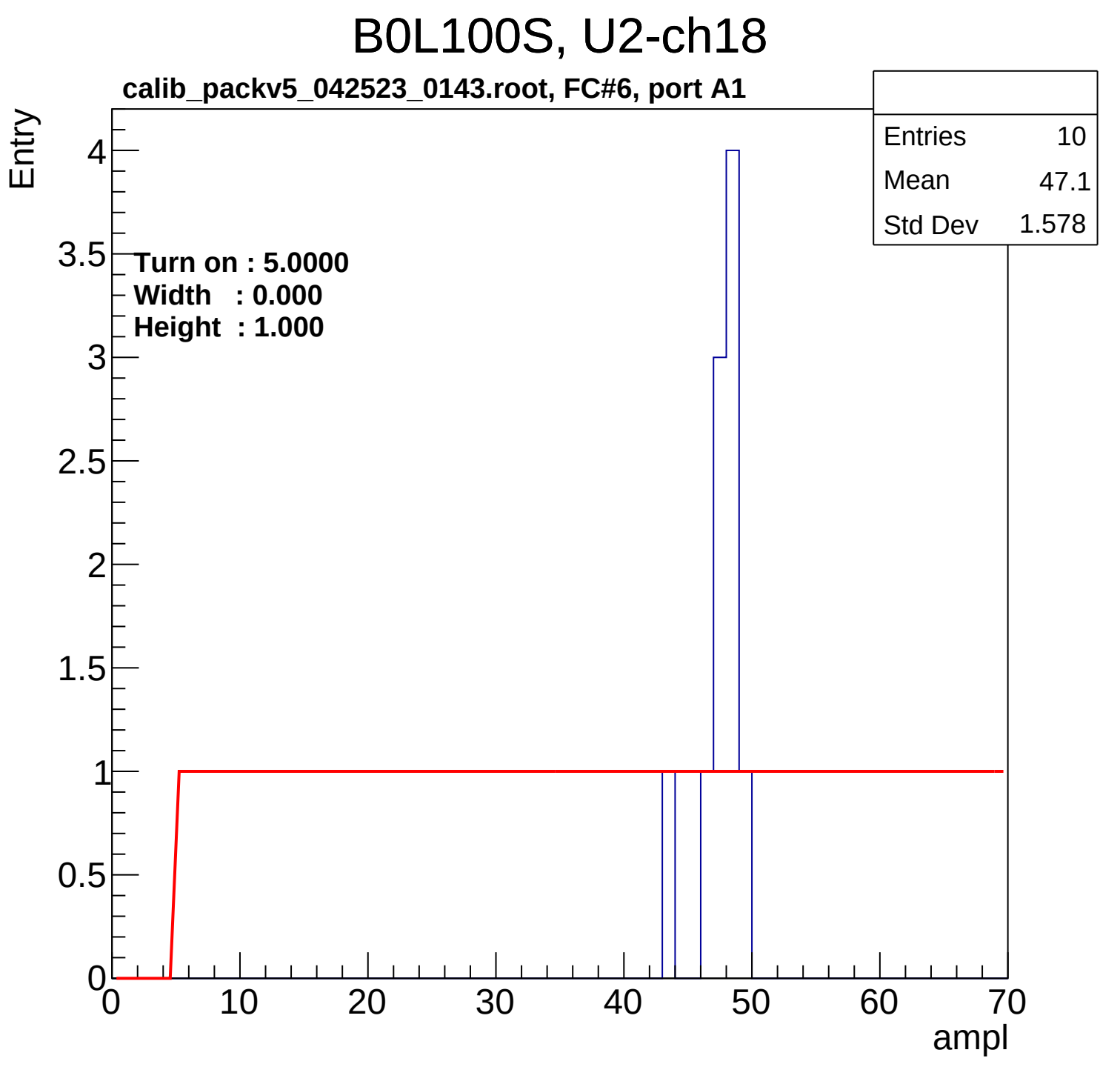
70
ampl


B0L100S, U2-ch18
calib_packv5_042523_0143.root, FC#6, port A1
Entries 10
Mean 47.1
Std Dev 1.578
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.5
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1.5
2
2.5
3
3.5
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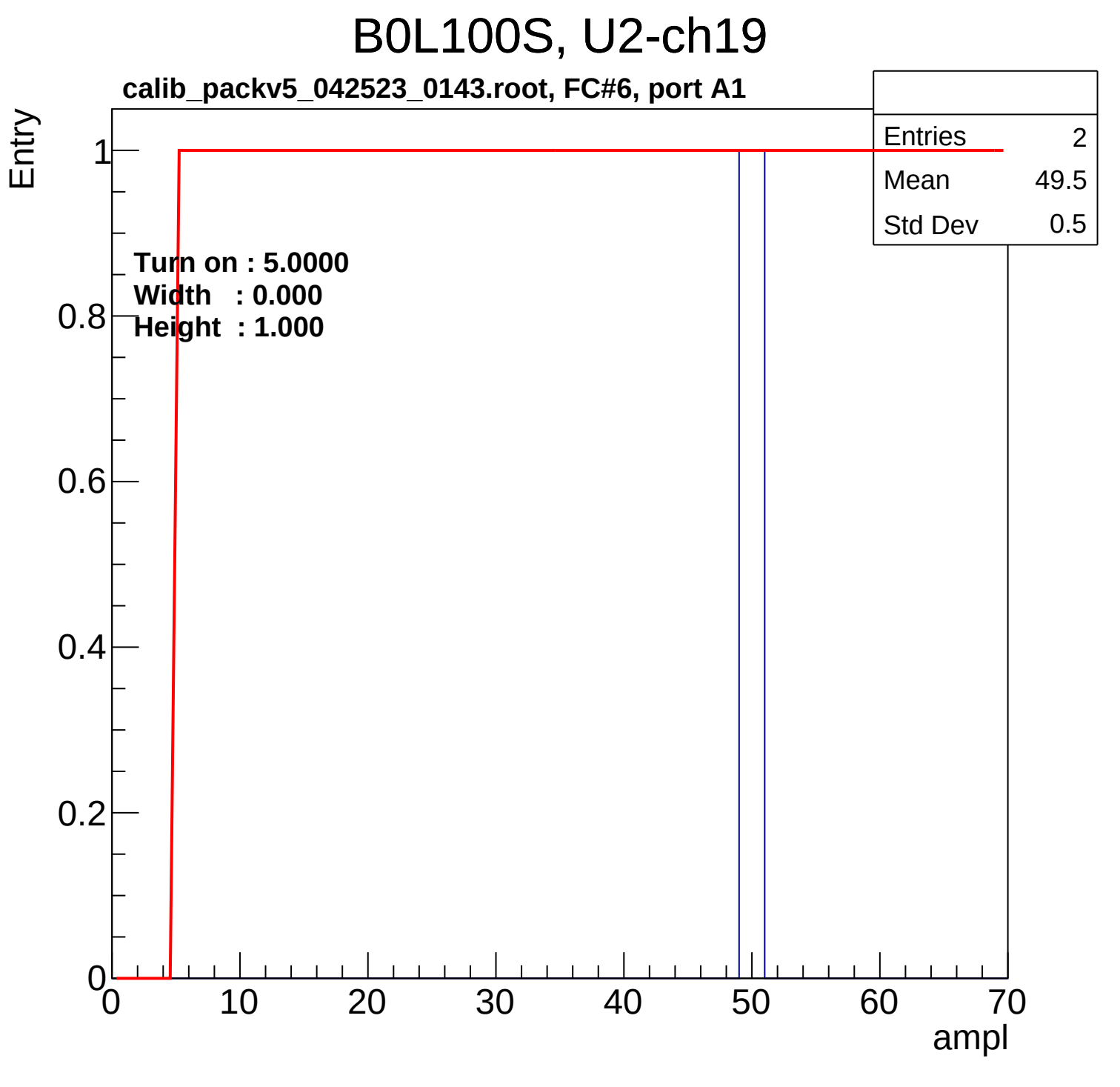
B0L100S, U2-ch19
calib_packv5_042523_0143.root, FC#6, port A1
Entries 2
Mean 49.5
Std Dev 0.5
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.2
0.4
0.6
0.8
1
0
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40
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60
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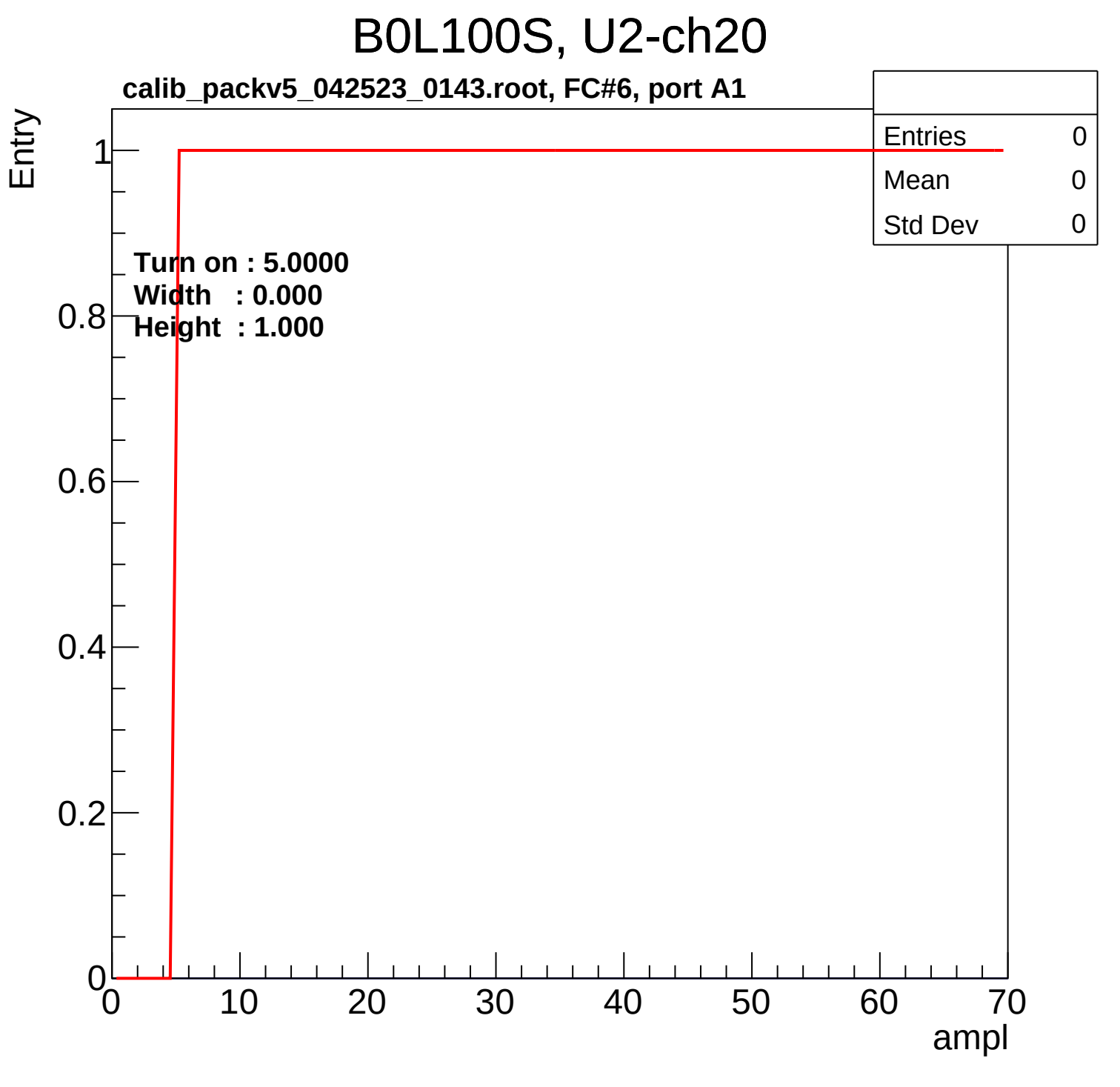
B0L100S, U2-ch20
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
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20
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40
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60
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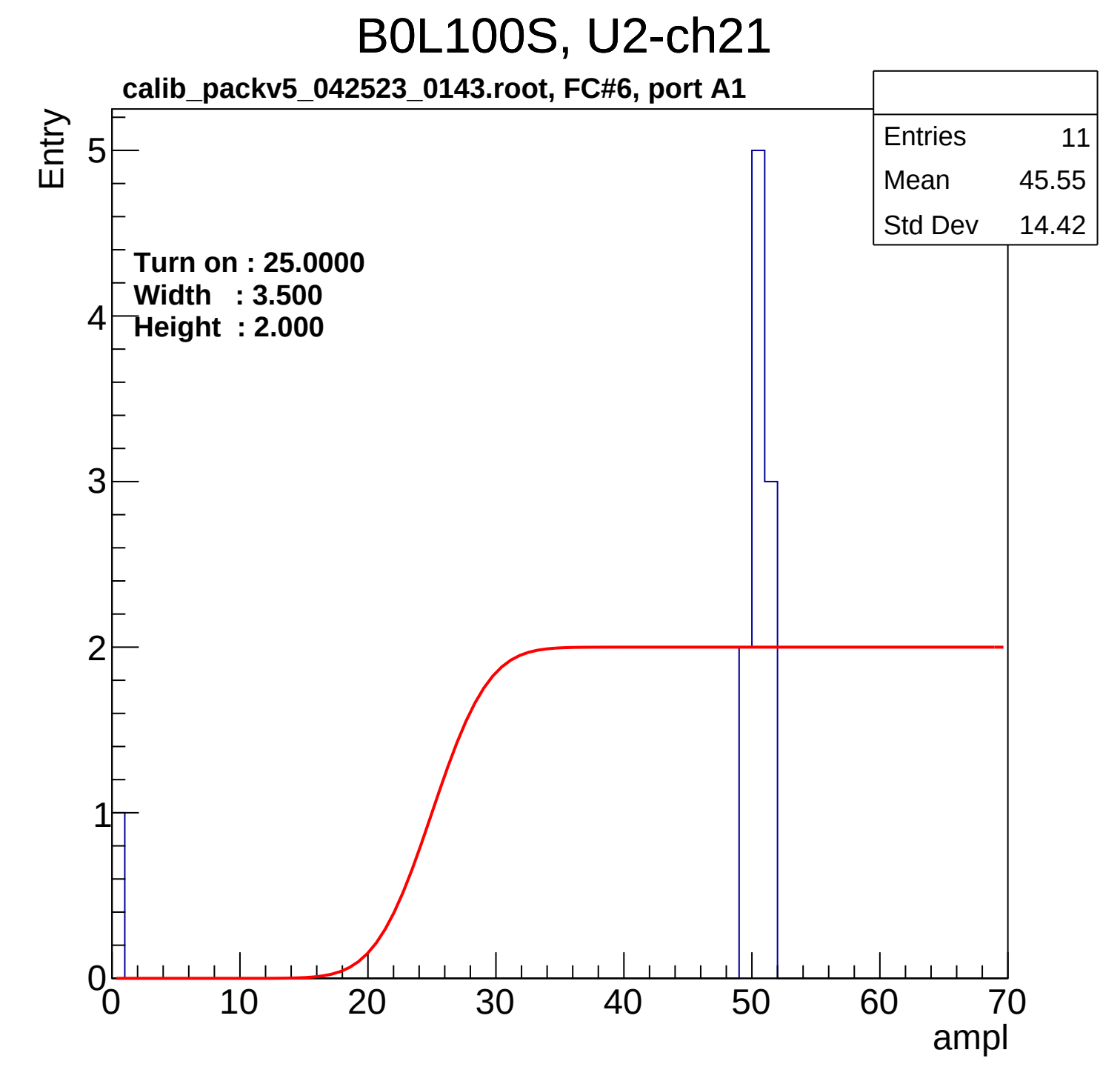
B0L100S, U2-ch21
calib_packv5_042523_0143.root, FC#6, port A1
Entries 11
Mean 45.55
Std Dev 14.42
Turn on : 25.0000
Width : 3.500
Height : 2.000
Entry
ampl
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2
3
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0
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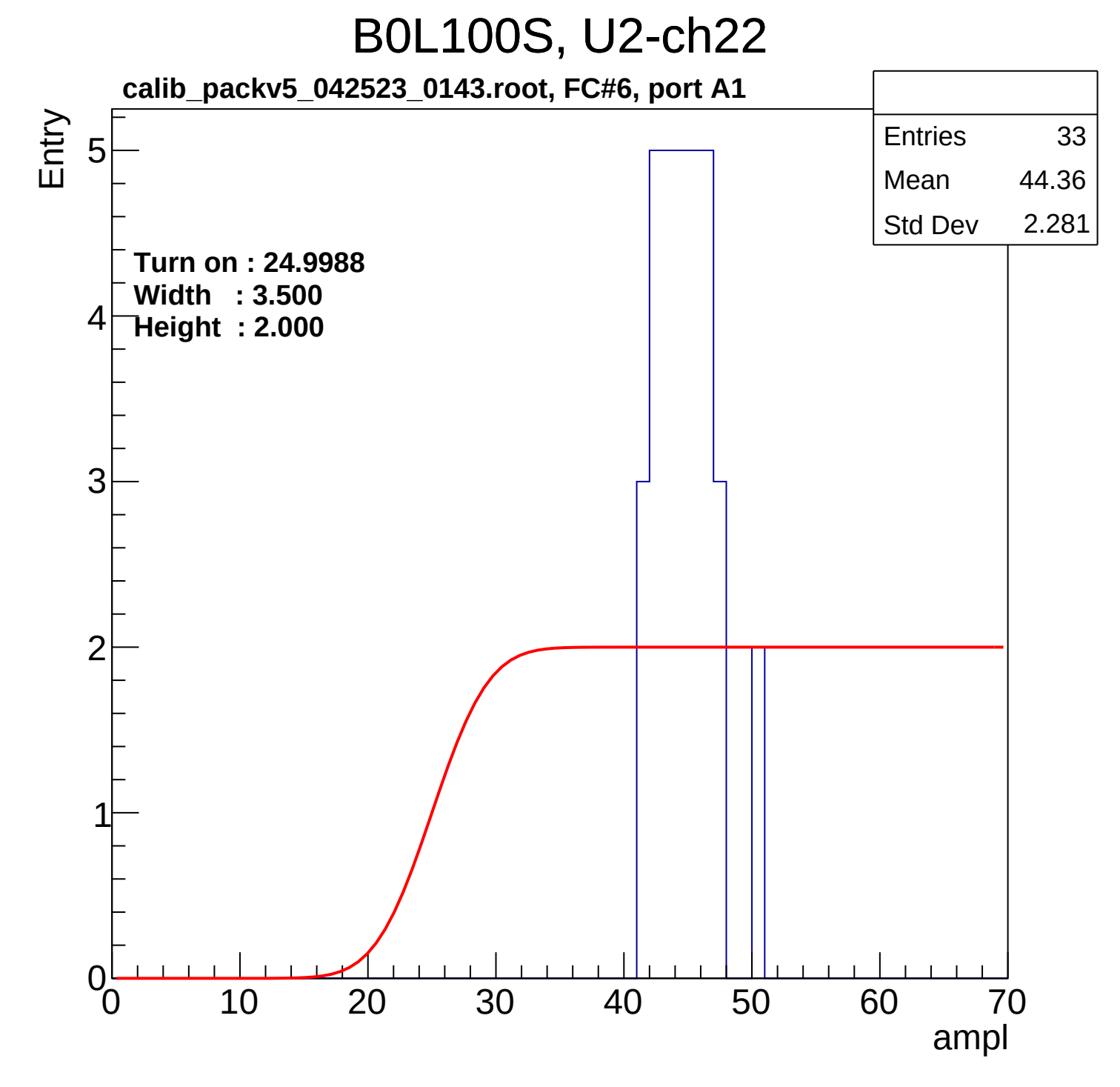
B0L100S, U2-ch22
calib_packv5_042523_0143.root, FC#6, port A1
Entries 33
Mean 44.36
Std Dev 2.281
Turn on : 24.9988
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Height : 2.000
Entry
ampl
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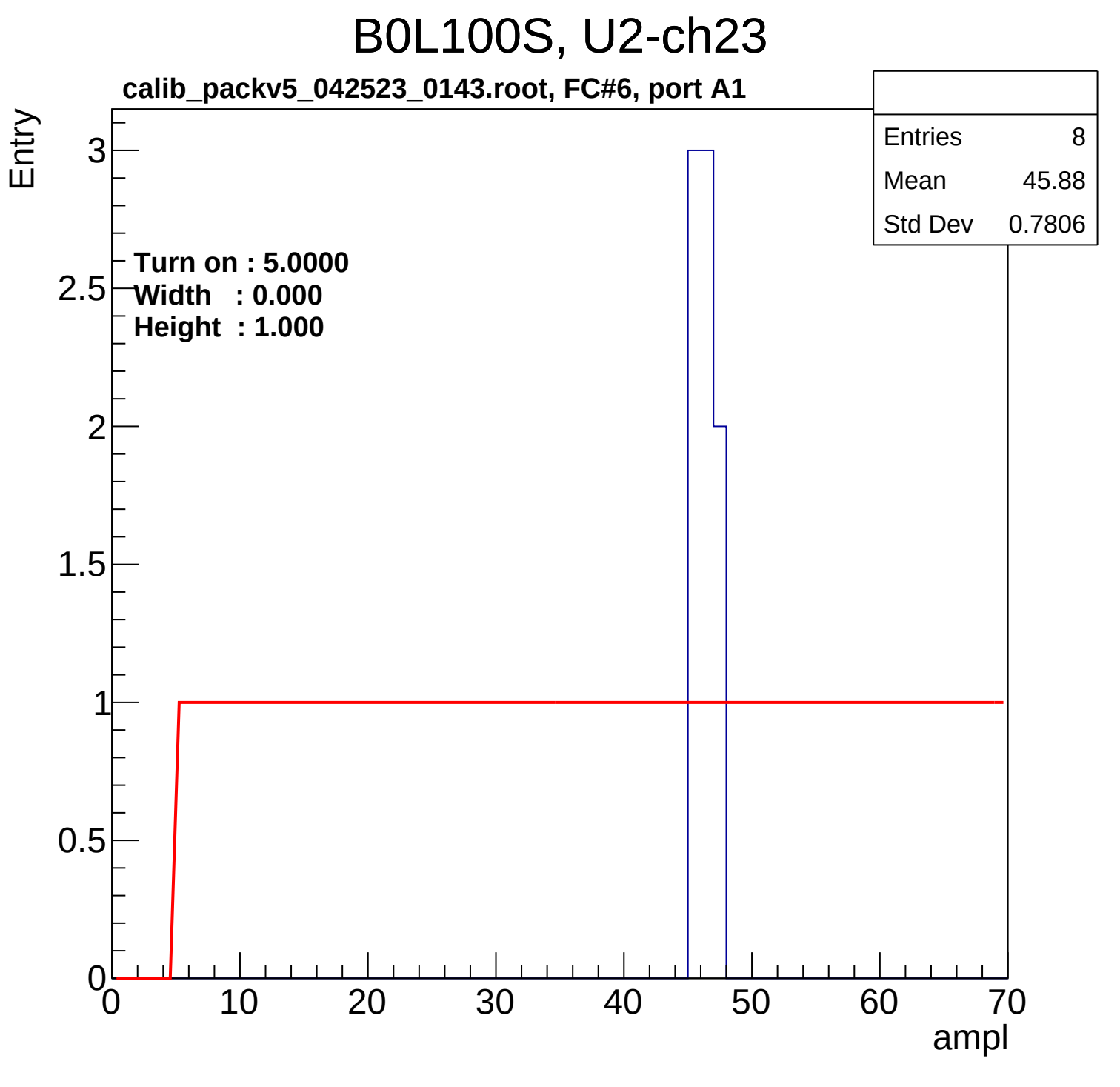
B0L100S, U2-ch23
calib_packv5_042523_0143.root, FC#6, port A1
Entries 8
Mean 45.88
Std Dev 0.7806
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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0.5
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2.5
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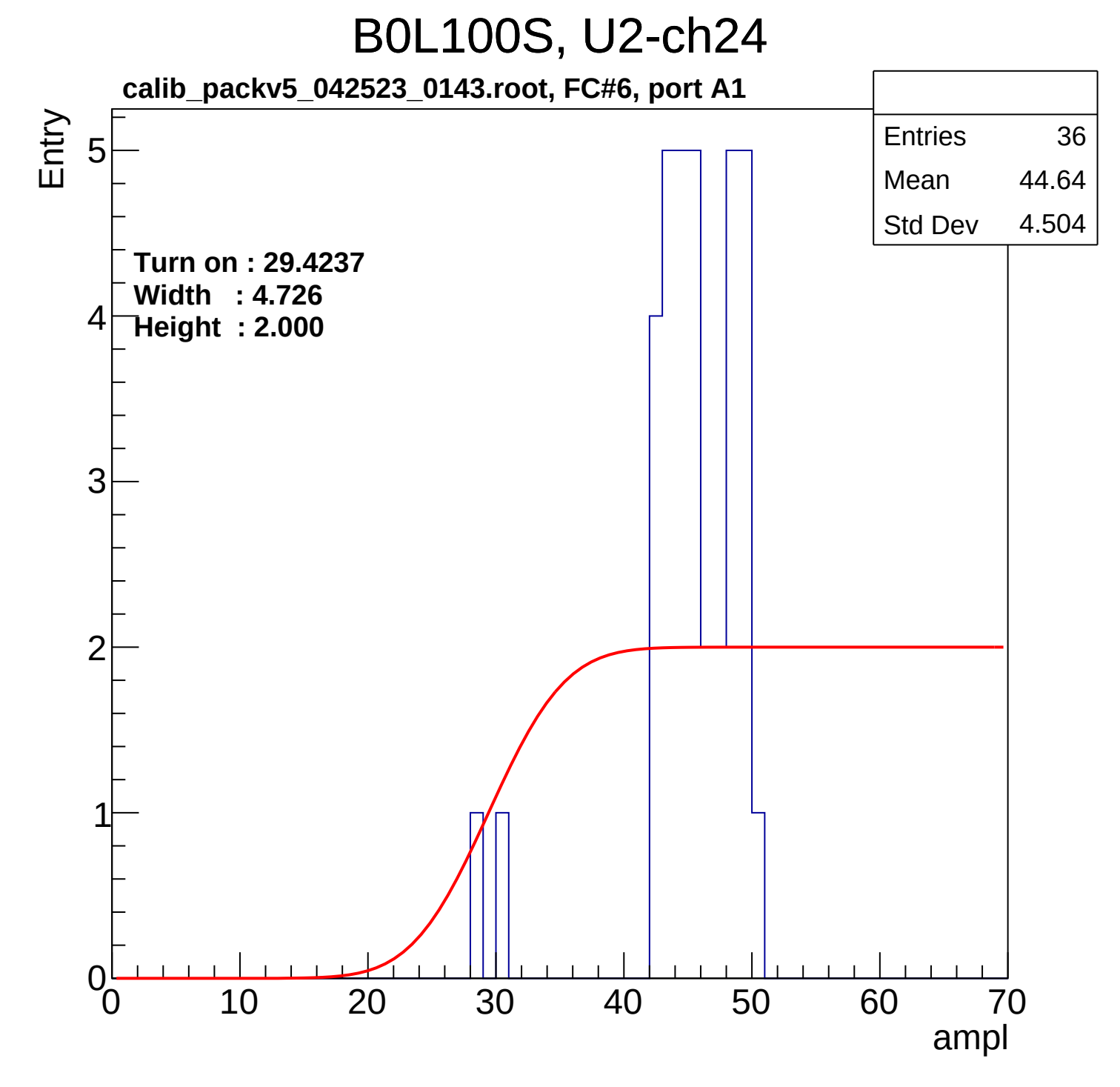
B0L100S, U2-ch24
calib_packv5_042523_0143.root, FC#6, port A1
Entries 36
Mean 44.64
Std Dev 4.504
Turn on : 29.4237
Width : 4.726
Height : 2.000
Entry
ampl
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1
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3
4
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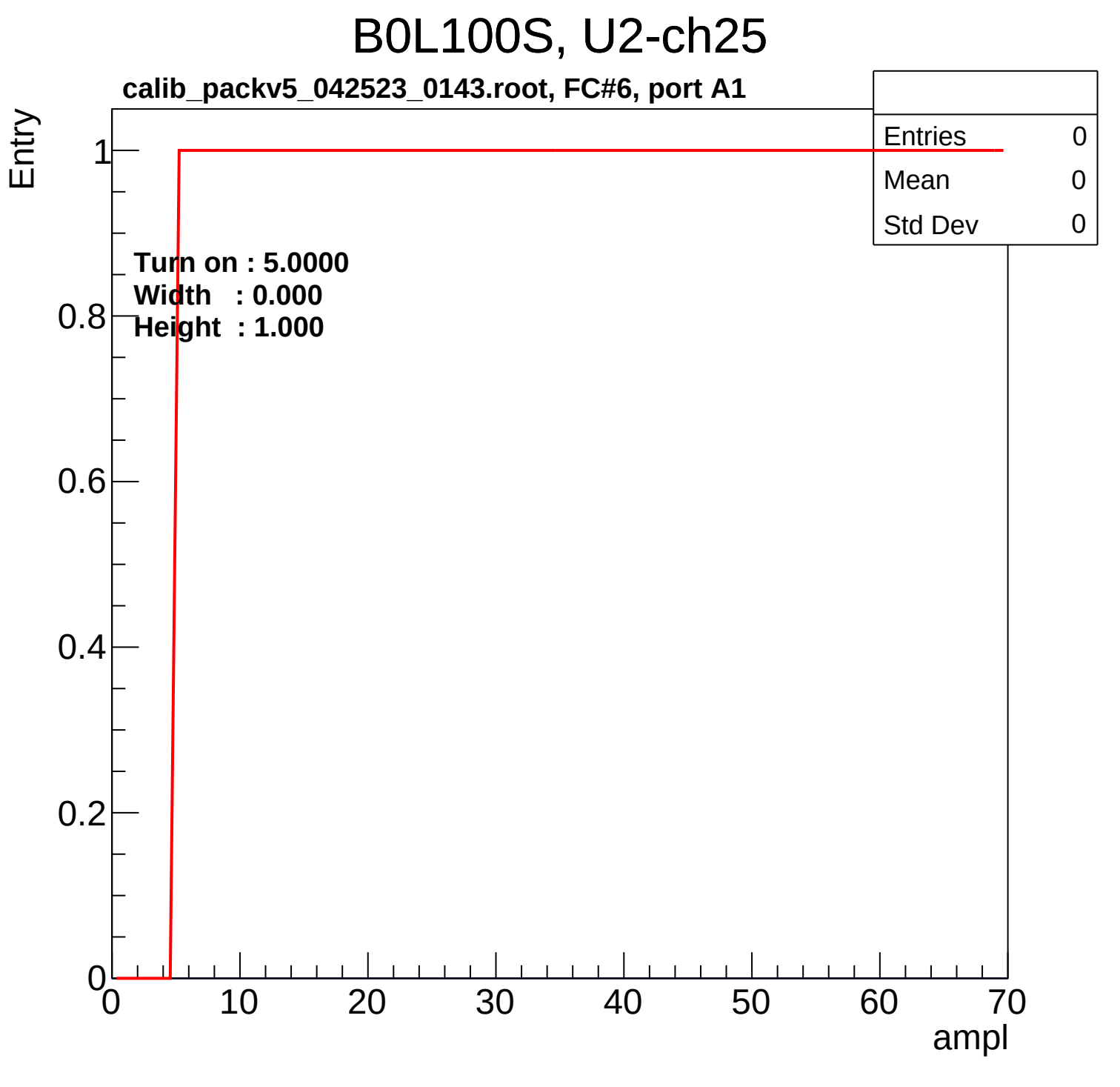
B0L100S, U2-ch25
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.2
0.4
0.6
0.8
1
0
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20
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40
50
60
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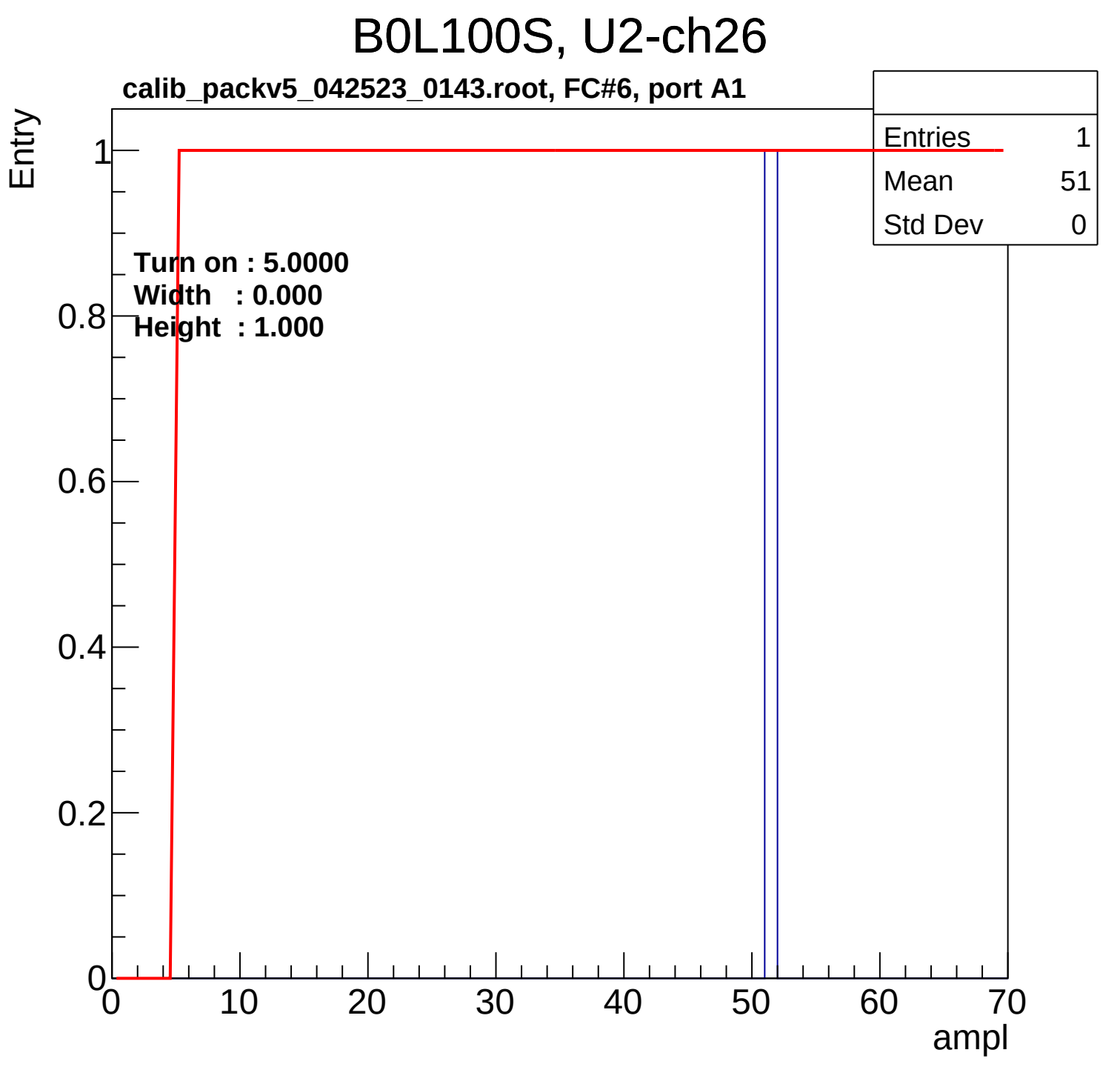
B0L100S, U2-ch26
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 51
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
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0.4
0.6
0.8
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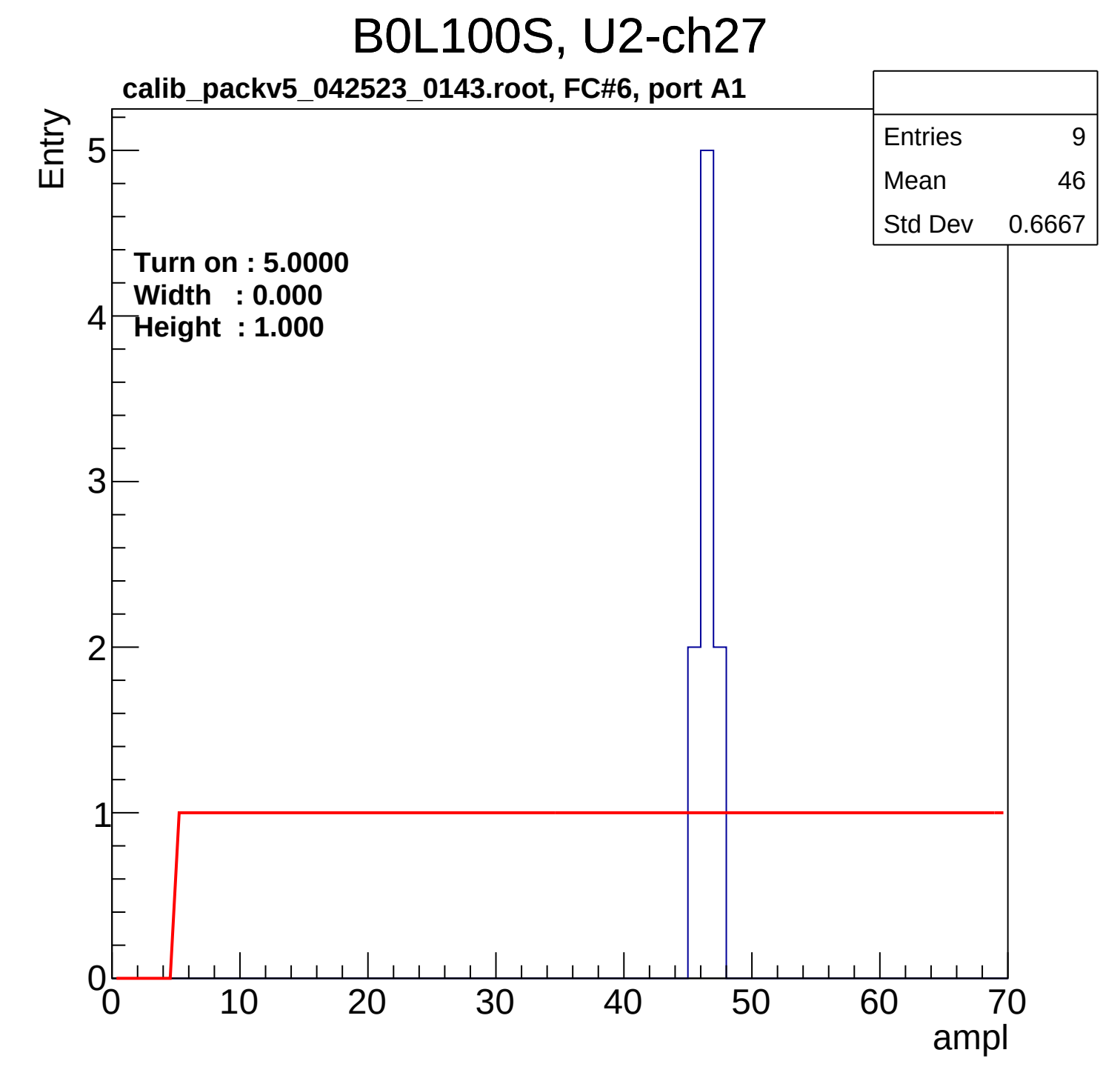
B0L100S, U2-ch27
calib_packv5_042523_0143.root, FC#6, port A1
Entries 9
Mean 46
Std Dev 0.6667
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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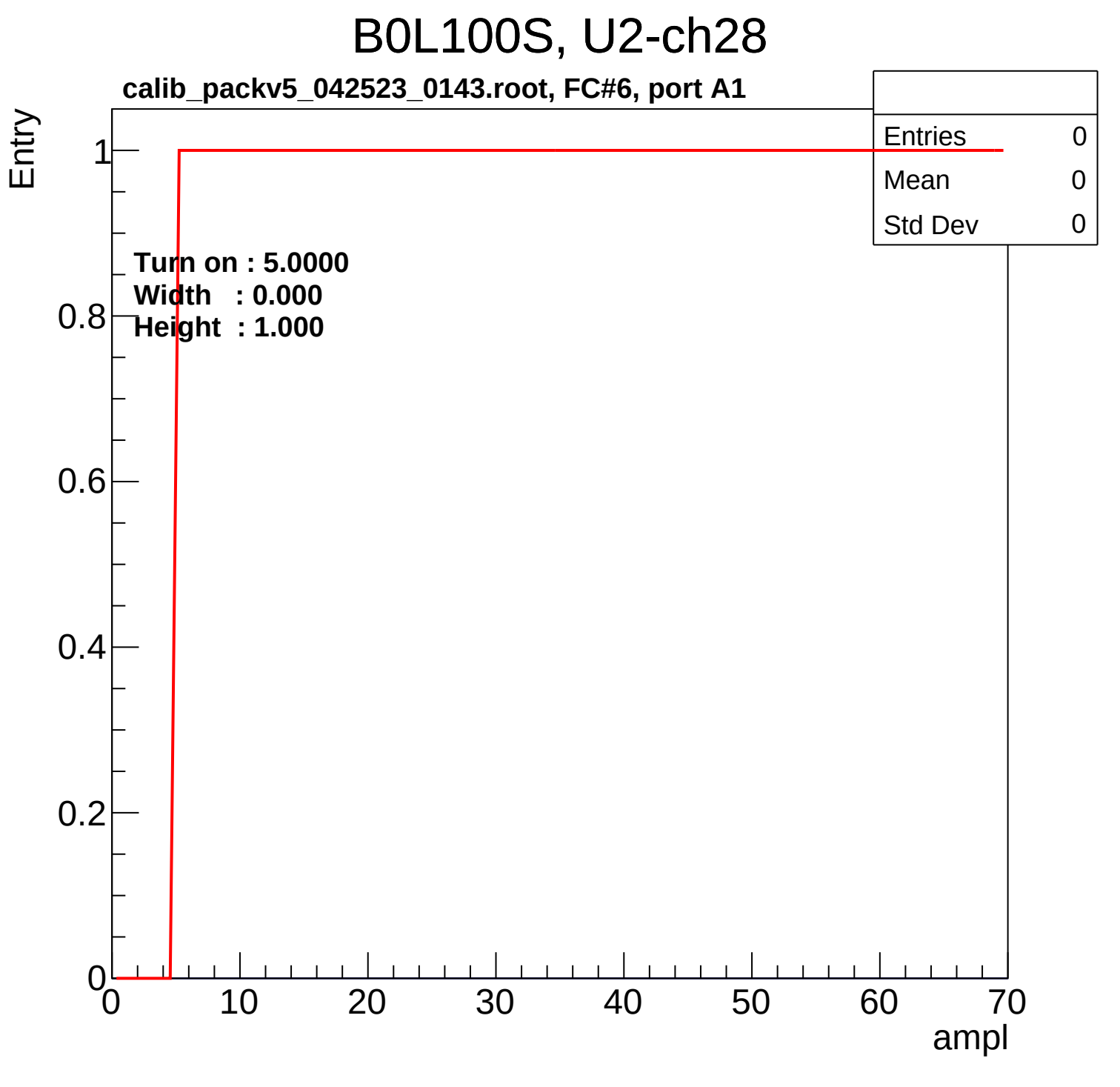
B0L100S, U2-ch28
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
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50
60
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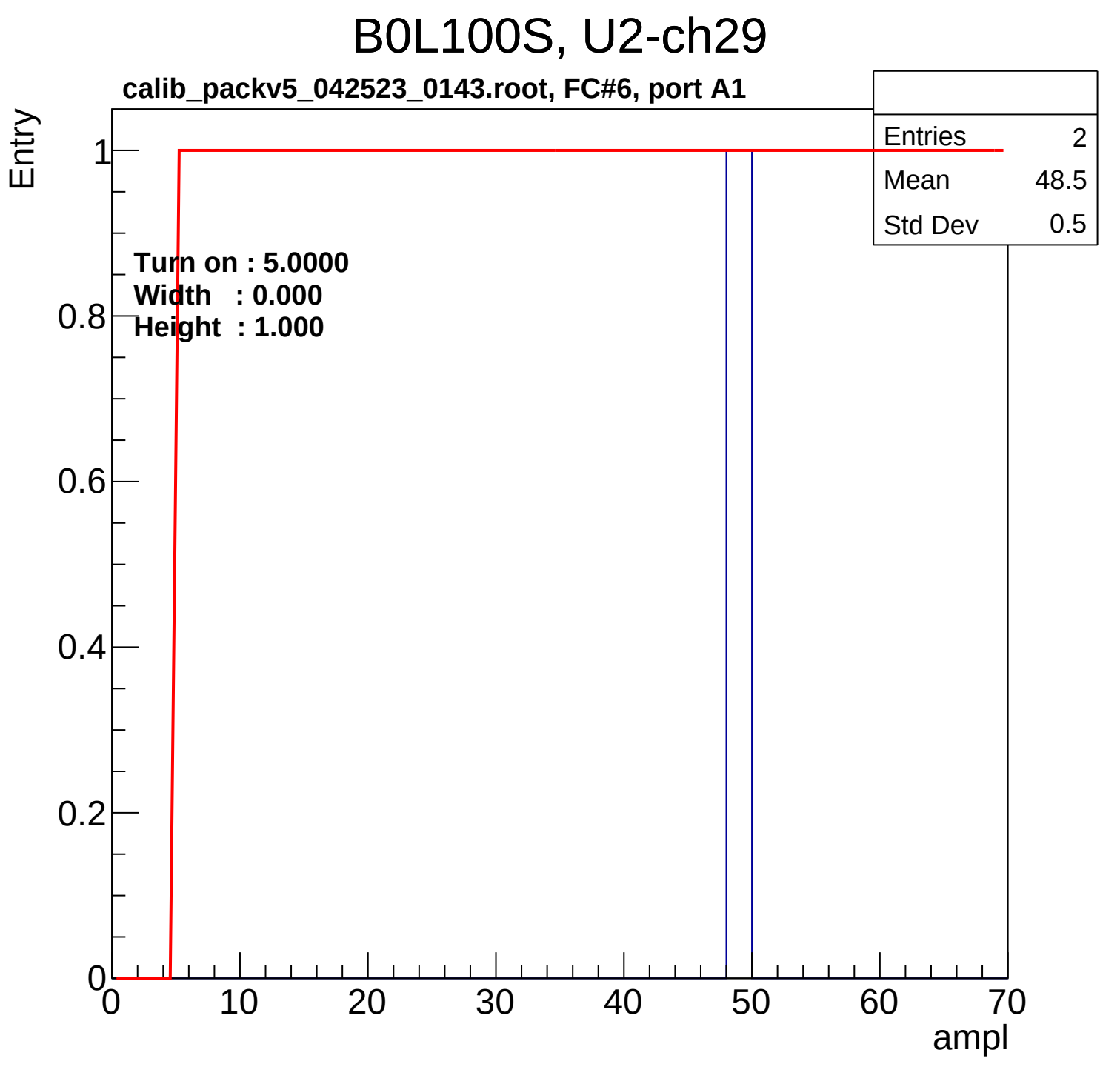
B0L100S, U2-ch29
calib_packv5_042523_0143.root, FC#6, port A1
Entries 2
Mean 48.5
Std Dev 0.5
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
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60
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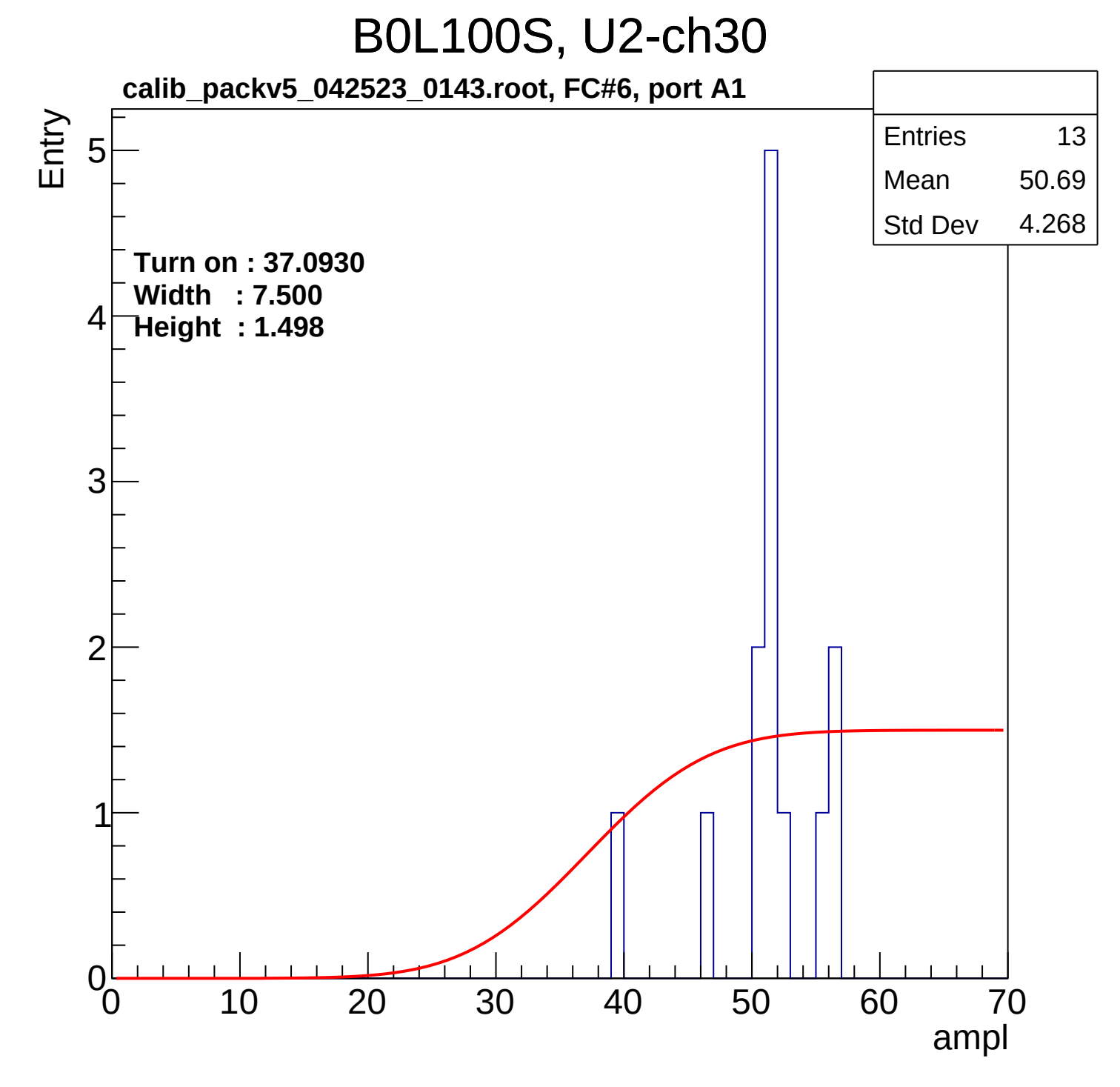
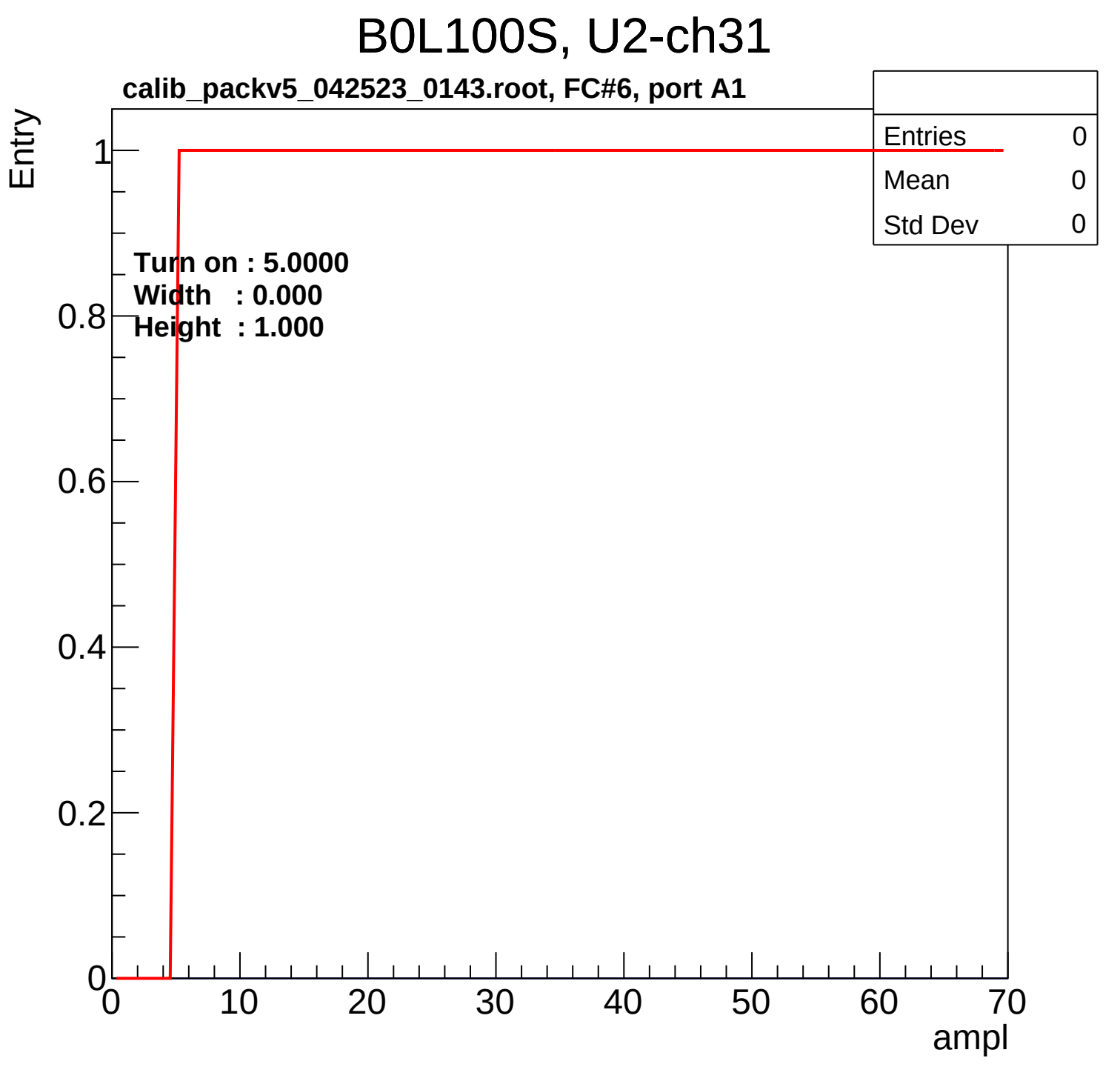
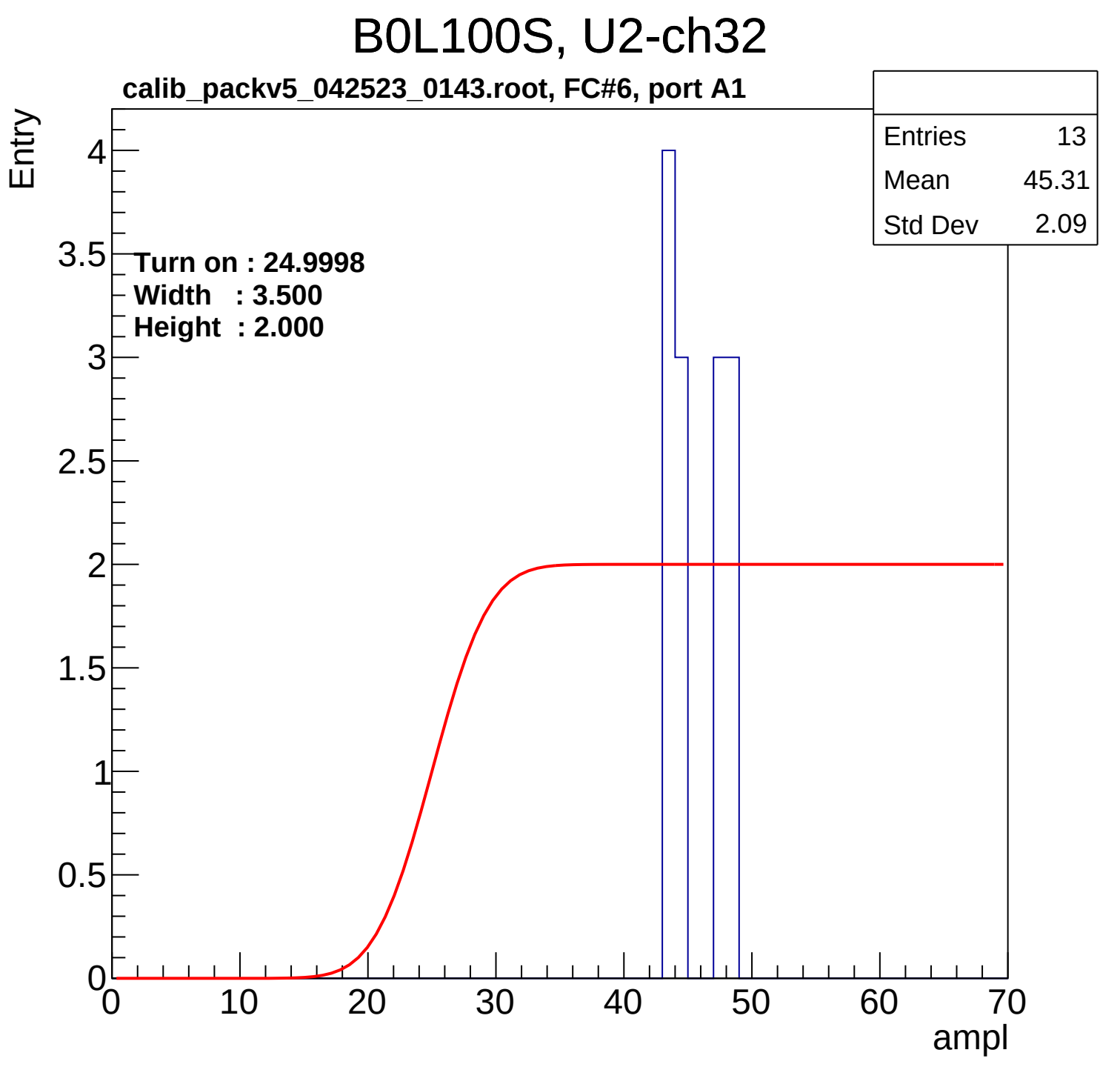
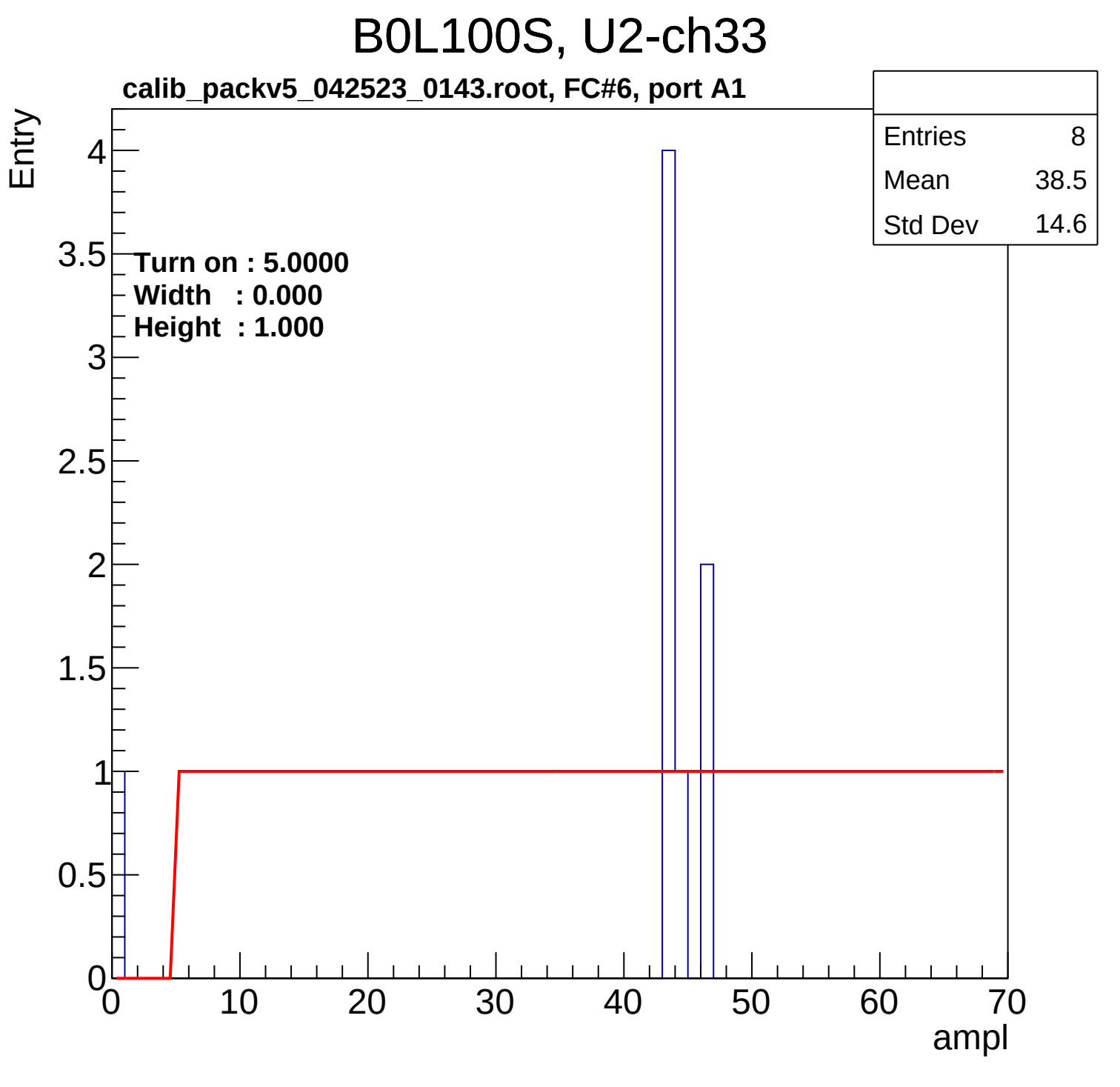
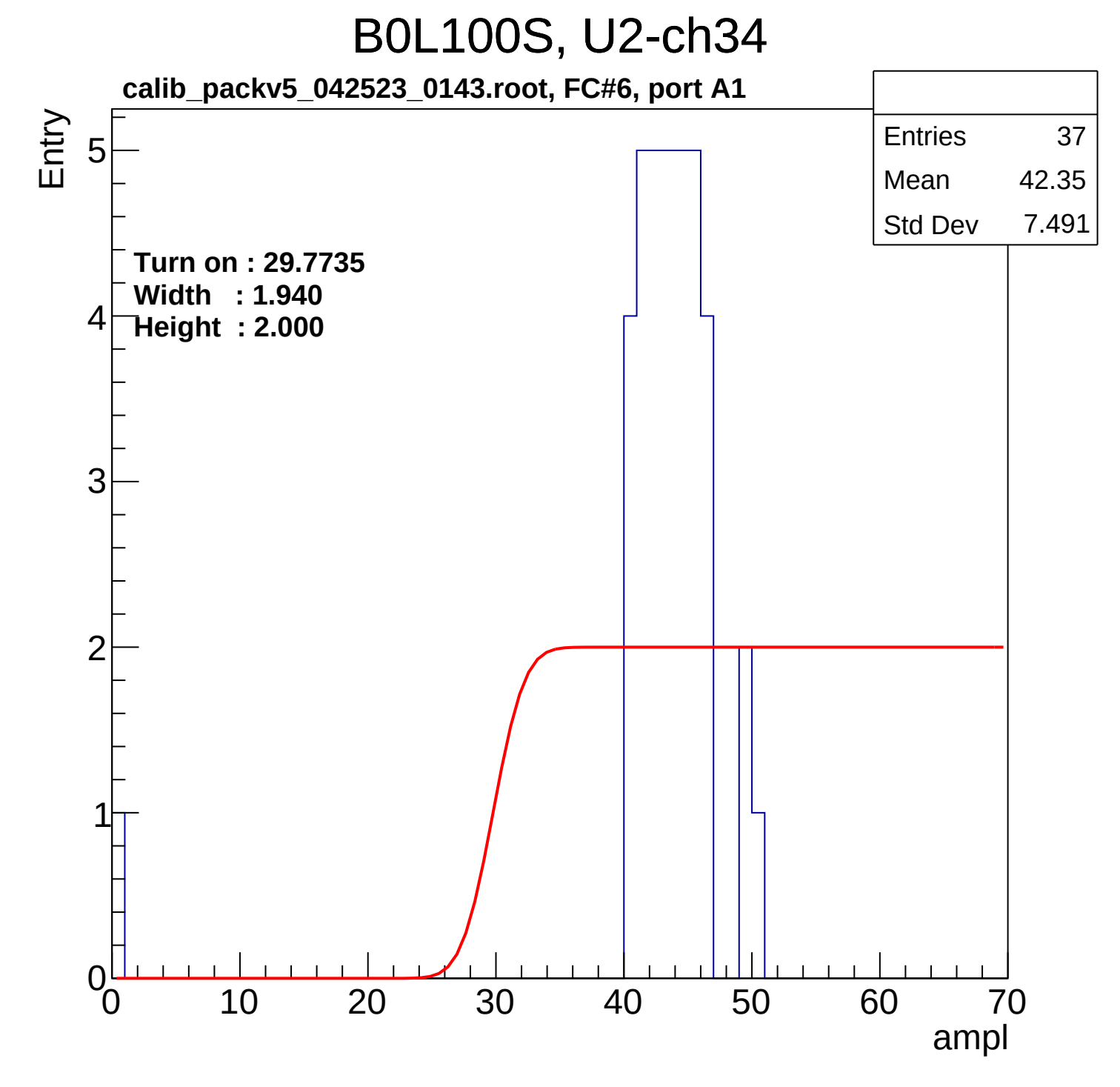
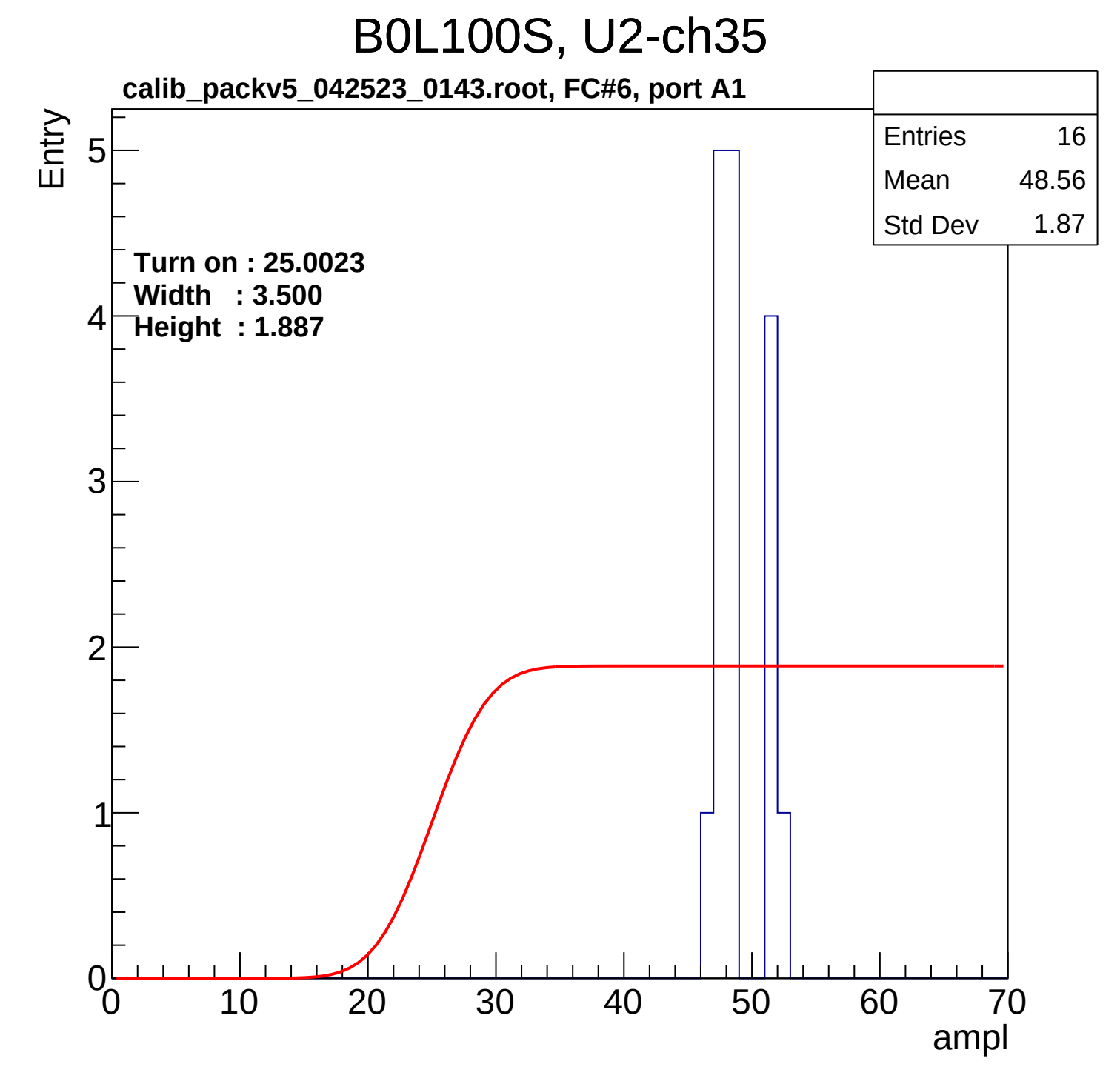

B0L100S, U2-ch30
calib_packv5_042523_0143.root, FC#6, port A1
Entries 13
Mean 50.69
Std Dev 4.268
Turn on : 37.0930
Width : 7.500
Height : 1.498
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5

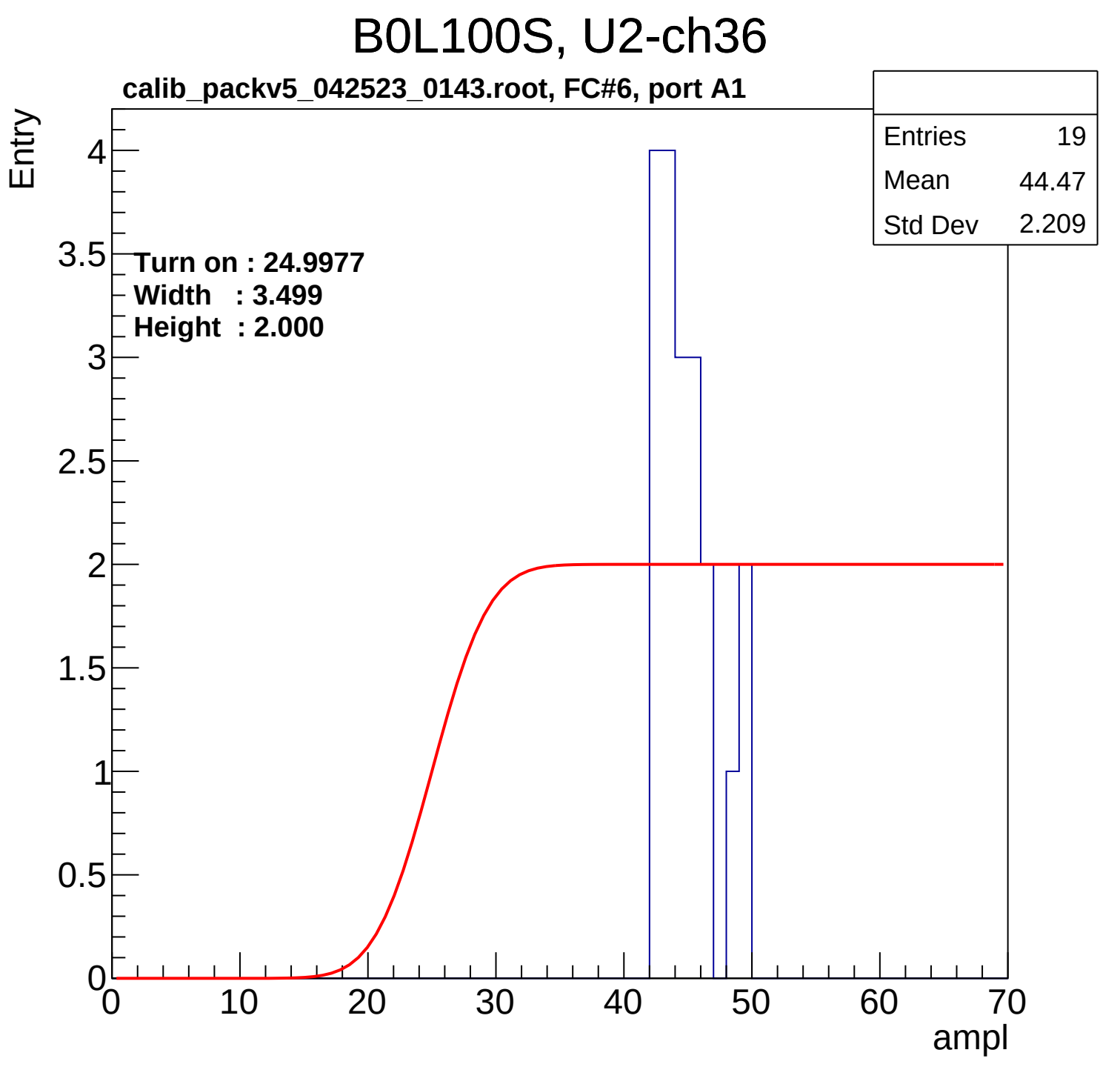

B0L100S, U2-ch31
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

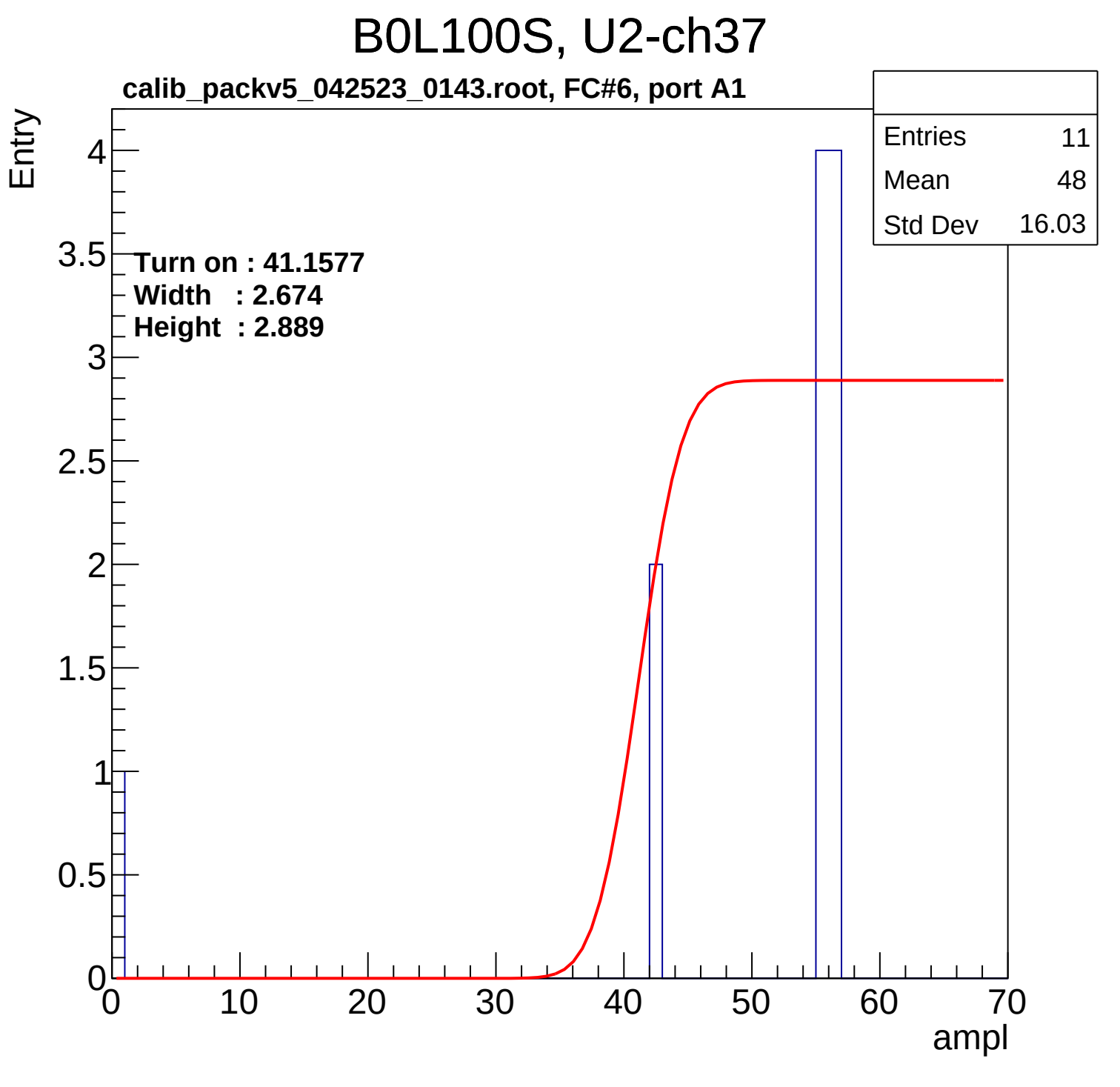

B0L100S, U2-ch32
calib_packv5_042523_0143.root, FC#6, port A1
Entries 13
Mean 45.31
Std Dev 2.09
Turn on : 24.9998
Width : 3.500
Height : 2.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

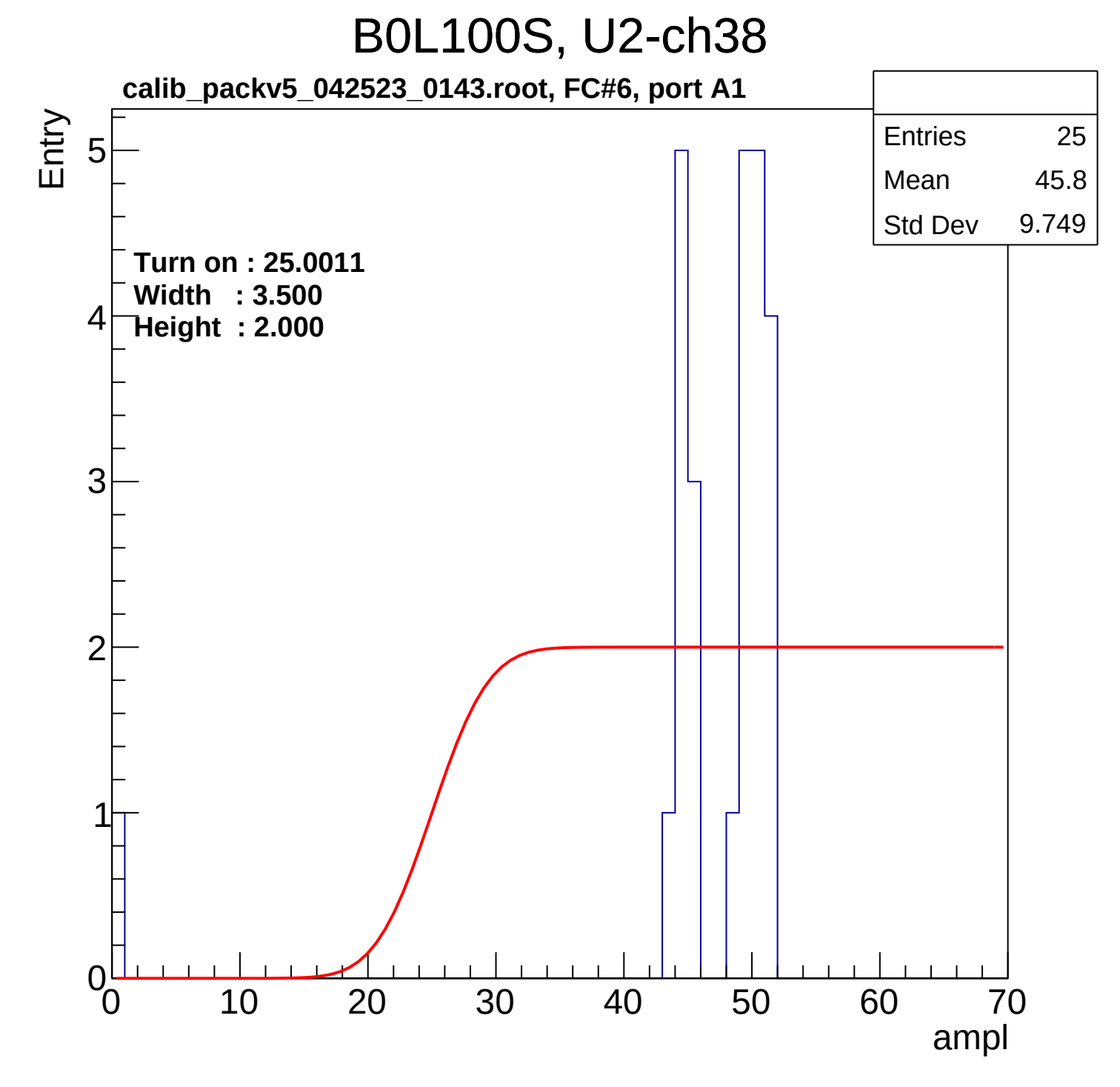

B0L100S, U2-ch33
calib_packv5_042523_0143.root, FC#6, port A1
Entries 8
Mean 38.5
Std Dev 14.6
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

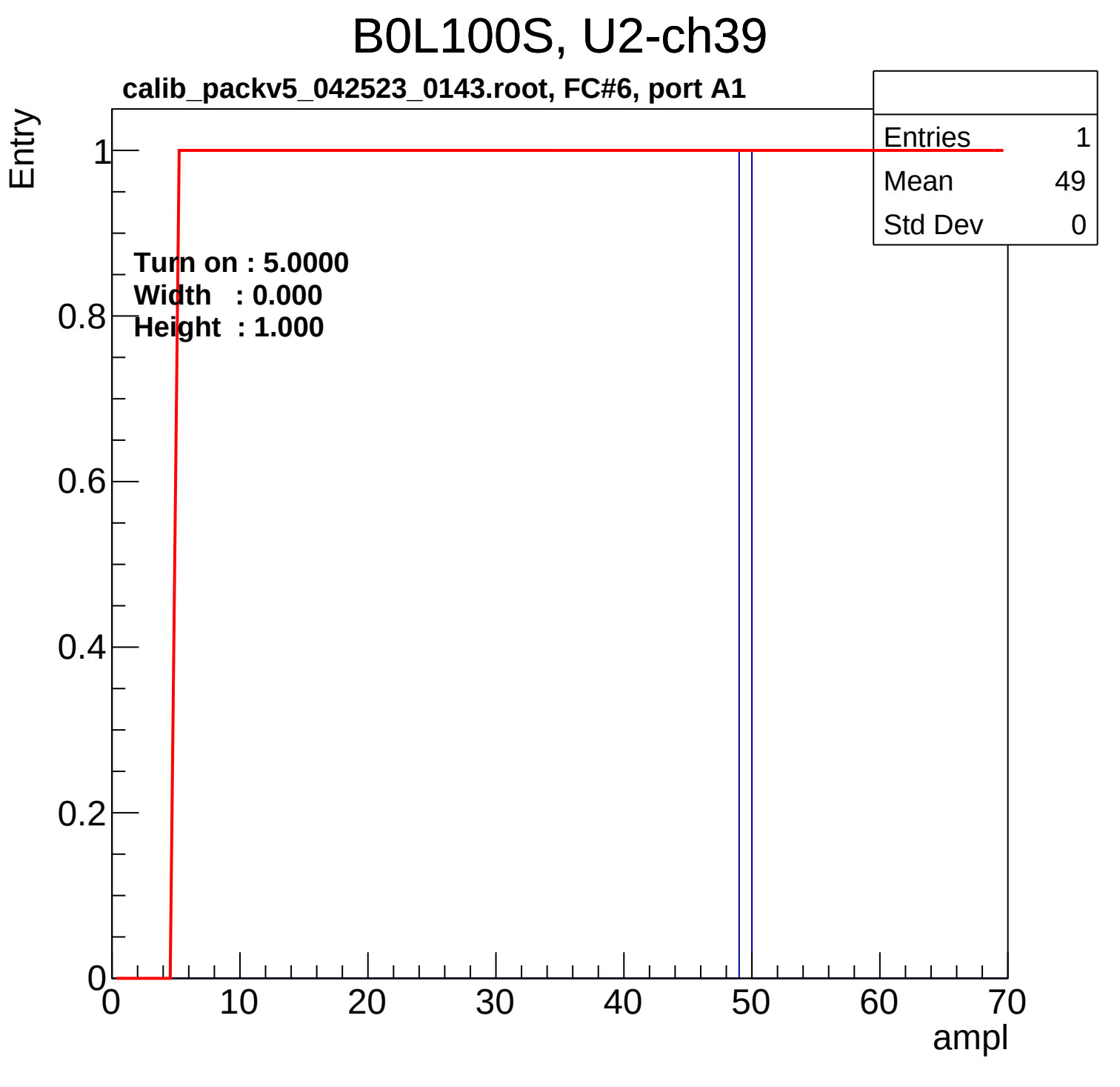

B0L100S, U2-ch34
calib_packv5_042523_0143.root, FC#6, port A1
Entries 37
Mean 42.35
Std Dev 7.491
Turn on : 29.7735
Width : 1.940
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

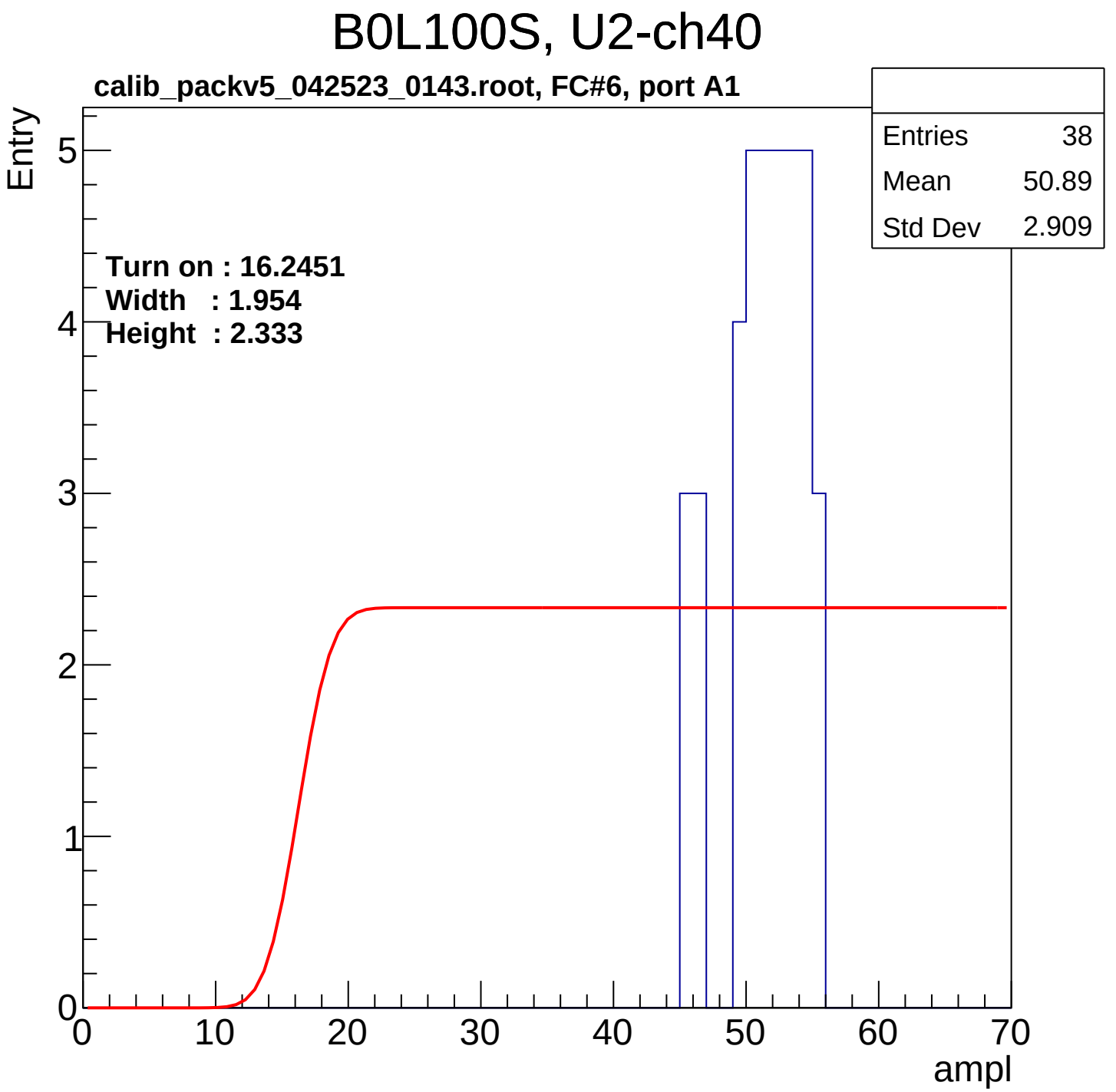

B0L100S, U2-ch35
calib_packv5_042523_0143.root, FC#6, port A1
Entries 16
Mean 48.56
Std Dev 1.87
Turn on : 25.0023
Width : 3.500
Height : 1.887
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

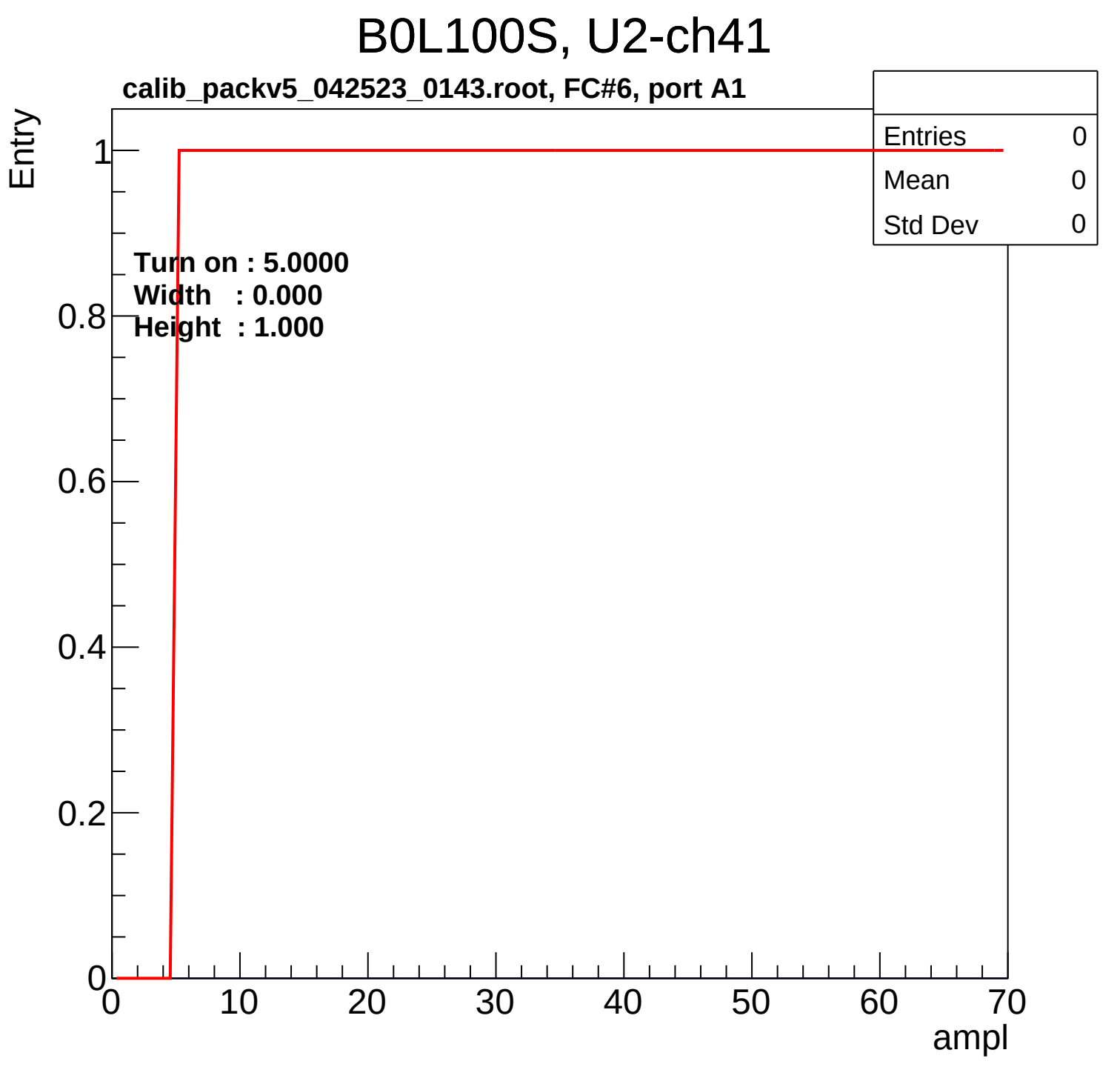

B0L100S, U2-ch36
calib_packv5_042523_0143.root, FC#6, port A1
Entries 19
Mean 44.47
Std Dev 2.209
Turn on : 24.9977
Width : 3.499
Height : 2.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

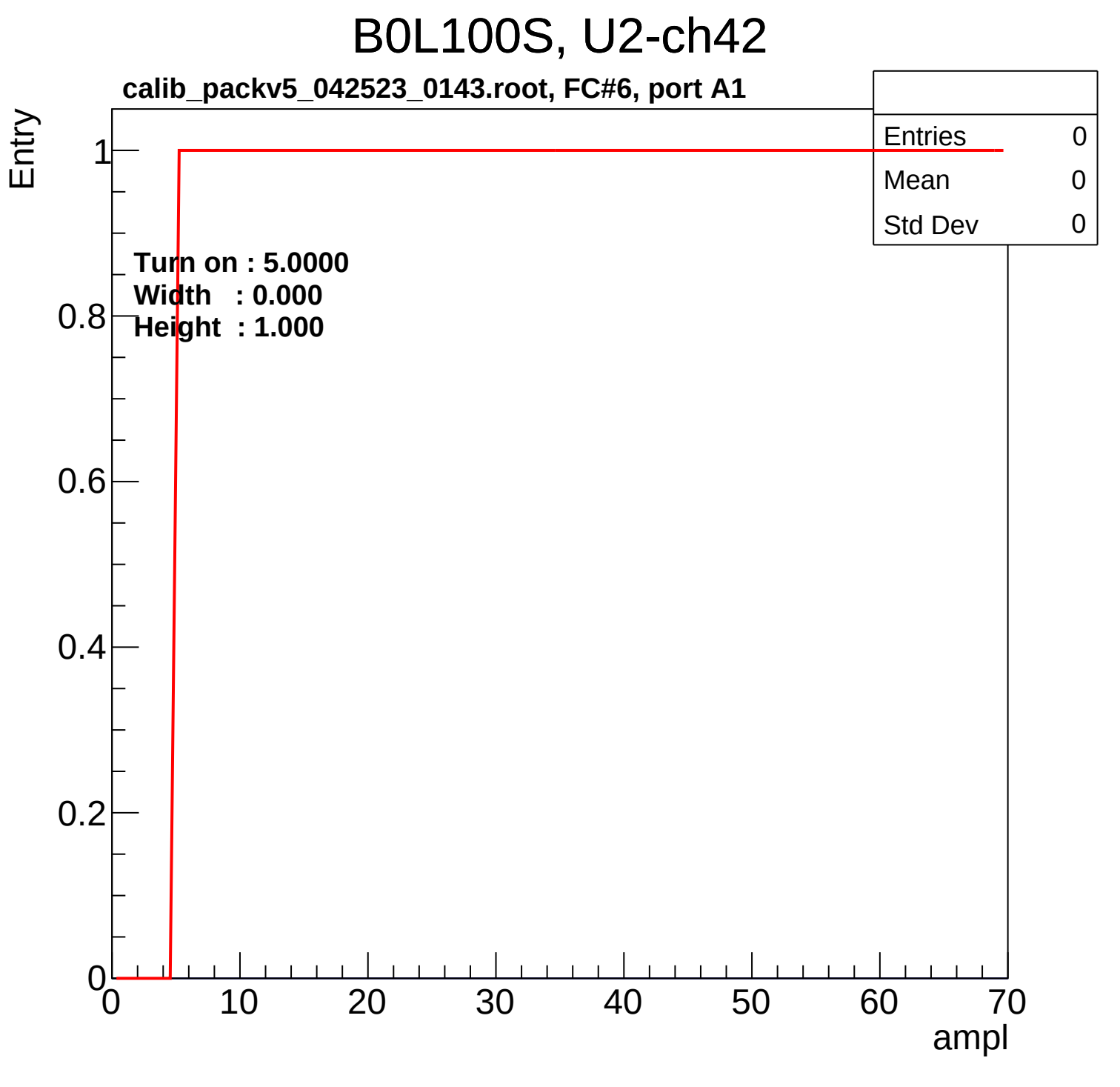

B0L100S, U2-ch37
calib_packv5_042523_0143.root, FC#6, port A1
Entries 11
Mean 48
Std Dev 16.03
Turn on : 41.1577
Width : 2.674
Height : 2.889
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

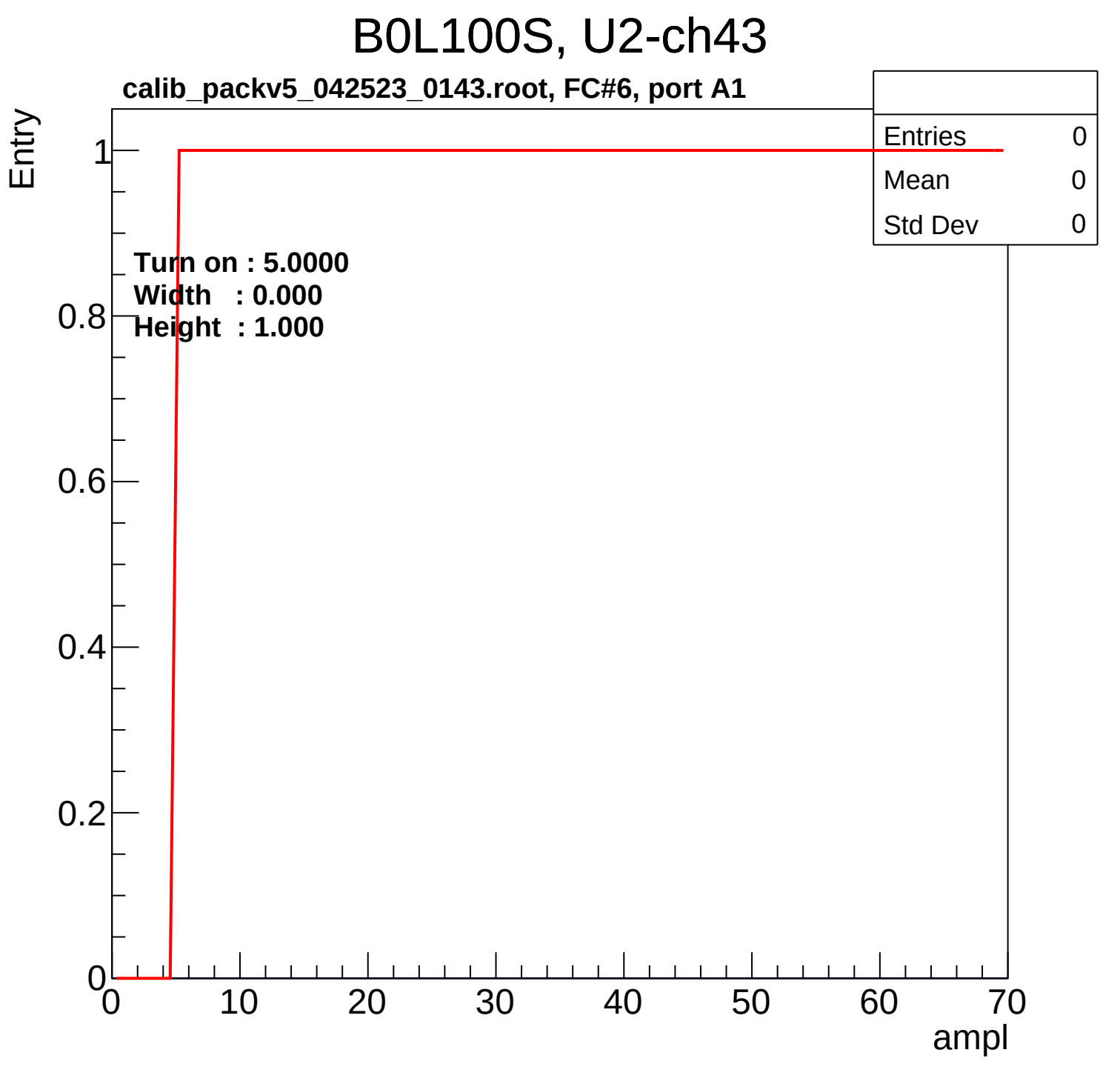

B0L100S, U2-ch38
calib_packv5_042523_0143.root, FC#6, port A1
Entries 25
Mean 45.8
Std Dev 9.749
Turn on : 25.0011
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

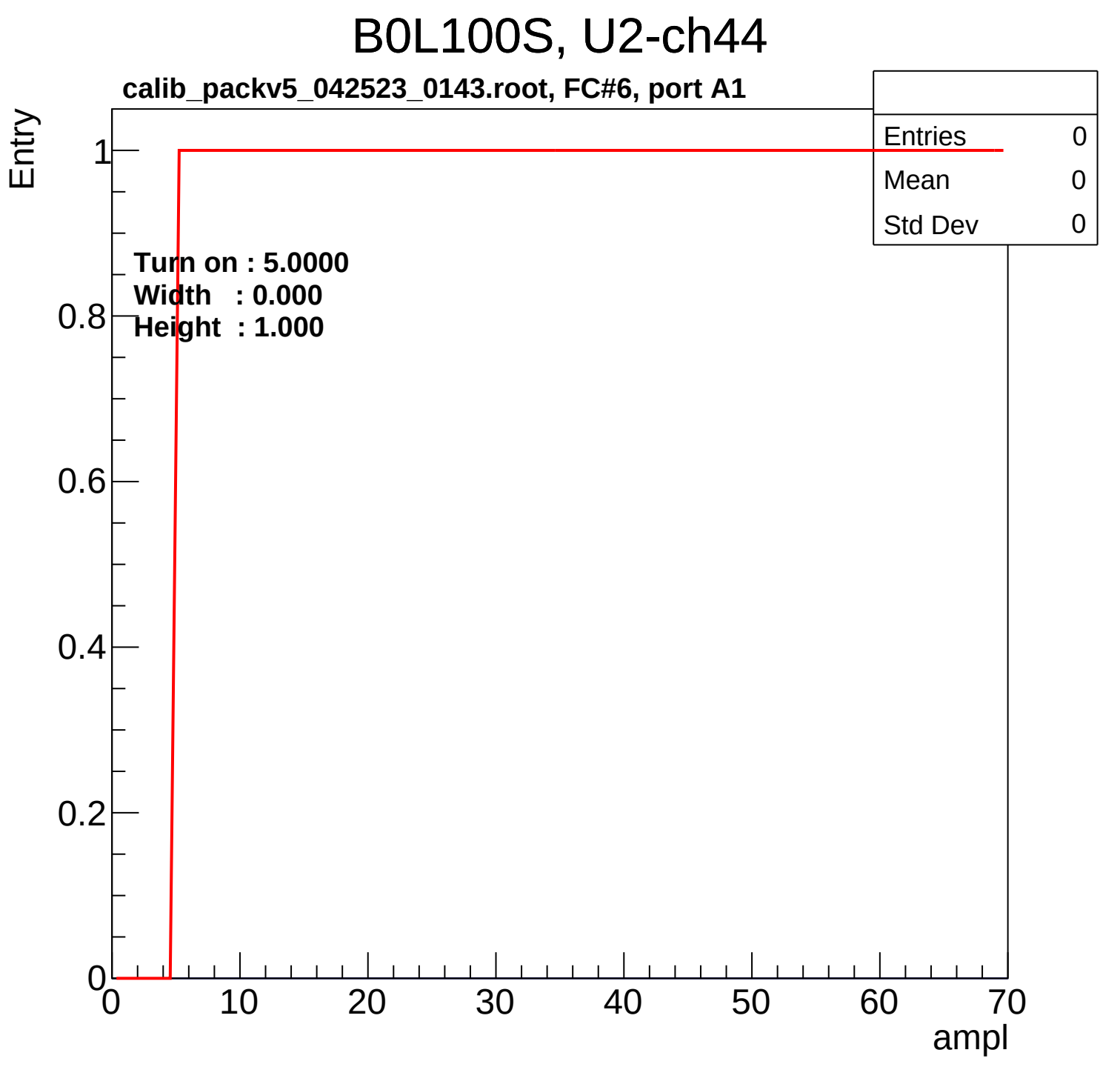

B0L100S, U2-ch39
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 49
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

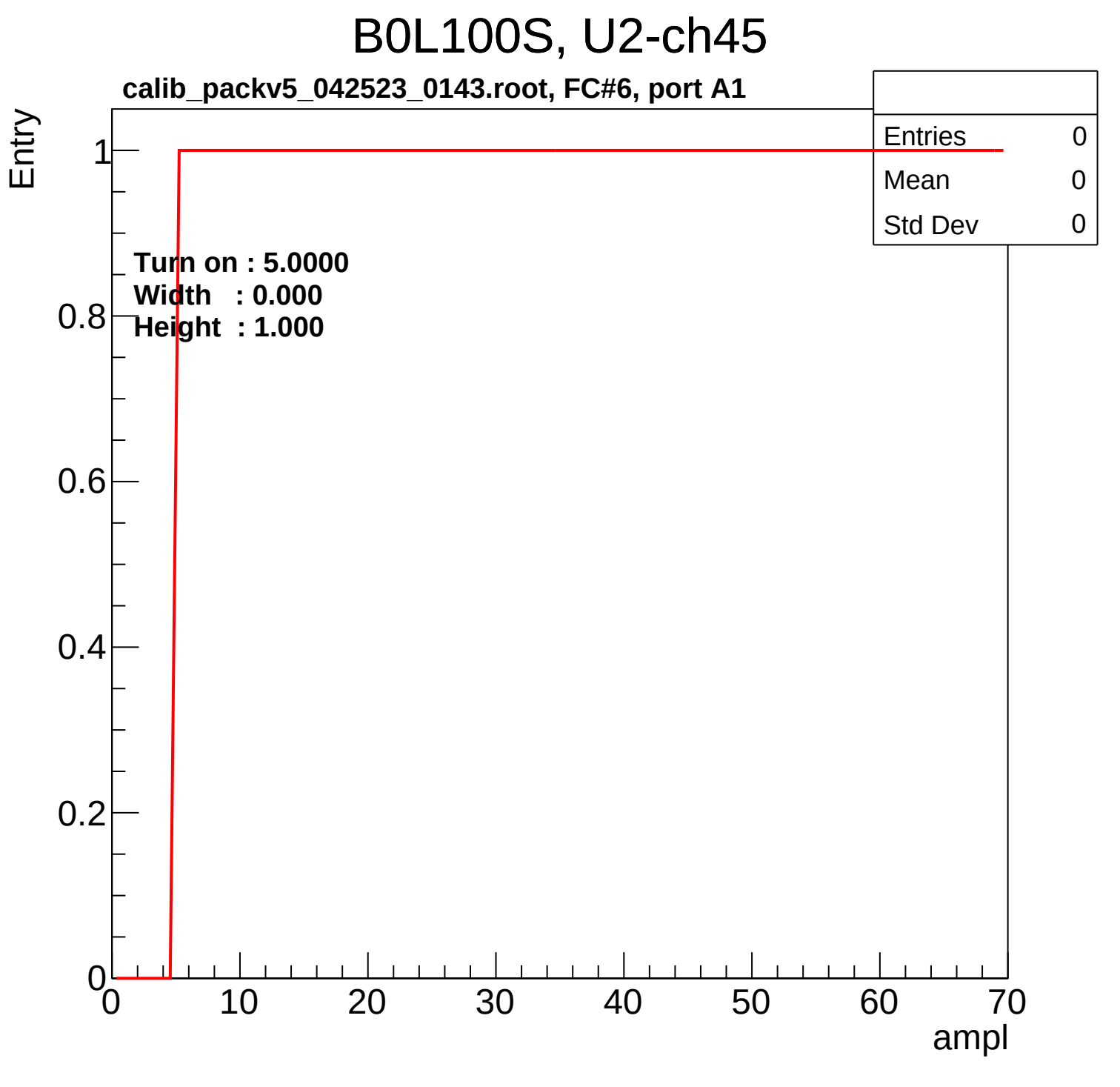

B0L100S, U2-ch40
calib_packv5_042523_0143.root, FC#6, port A1
Entries 38
Mean 50.89
Std Dev 2.909
Turn on : 16.2451
Width : 1.954
Height : 2.333
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

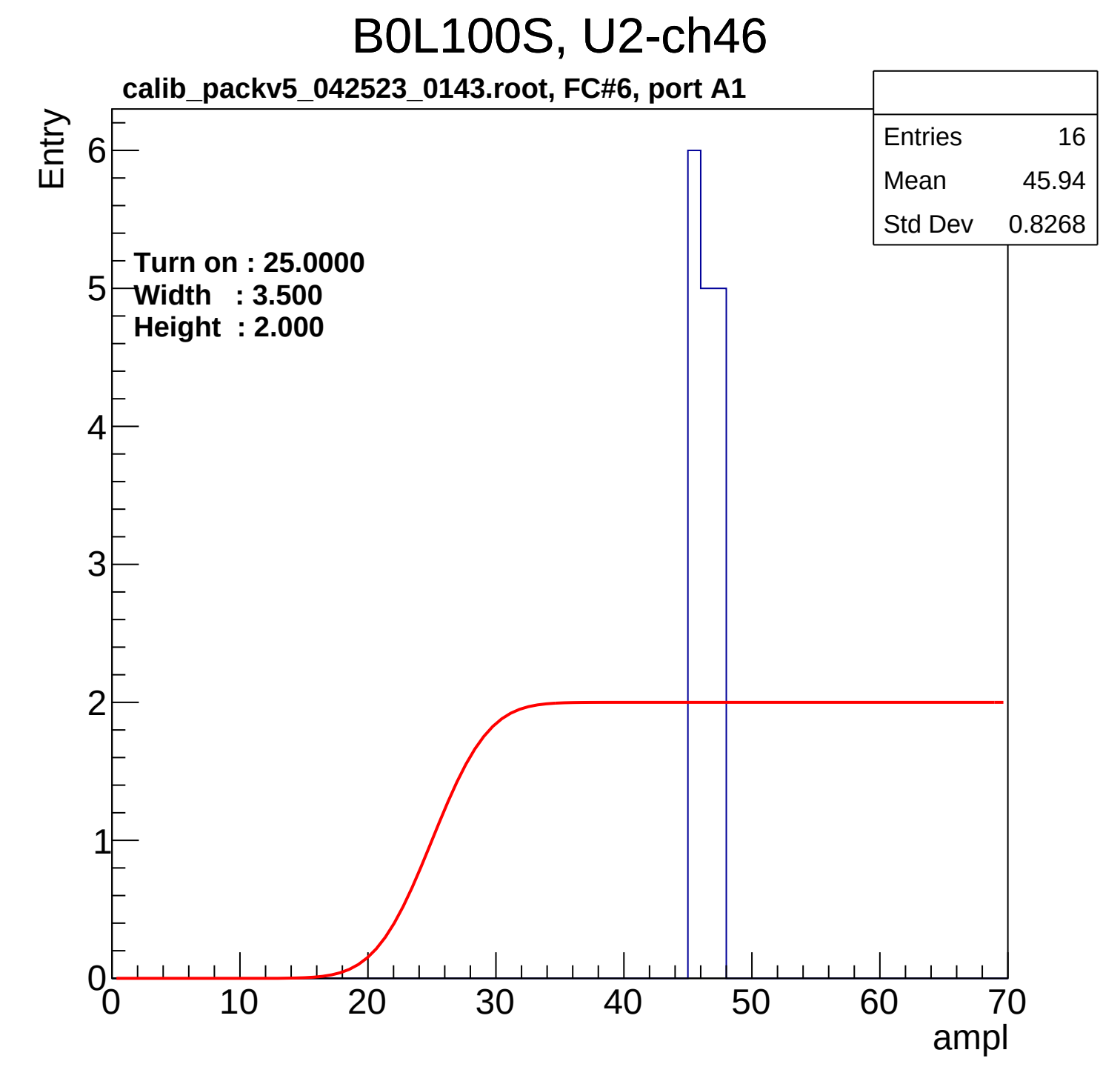

B0L100S, U2-ch41
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

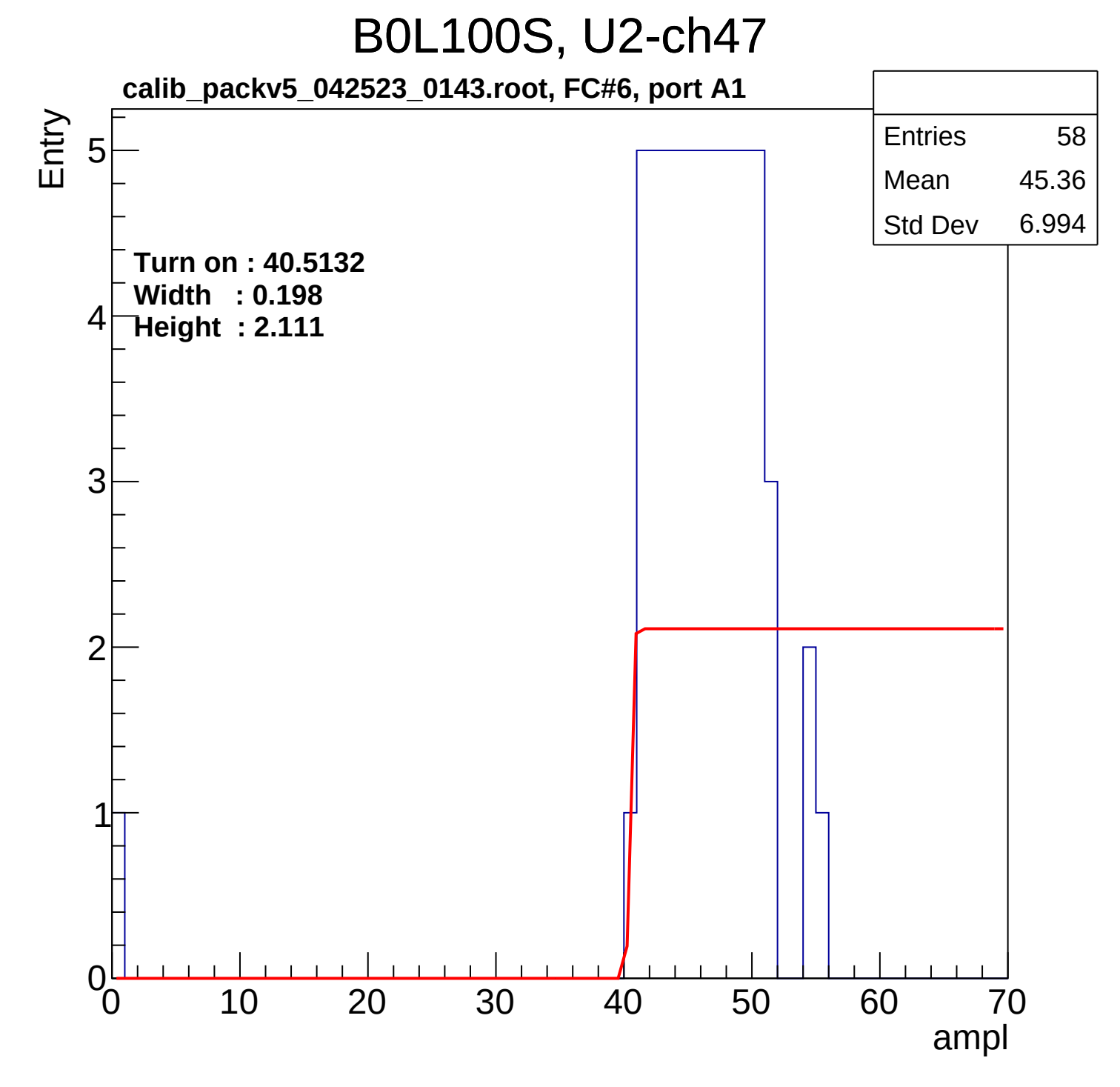

B0L100S, U2-ch42
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B0L100S, U2-ch43
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B0L100S, U2-ch44
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U2-ch45
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U2-ch46
calib_packv5_042523_0143.root, FC#6, port A1
Entries 16
Mean 45.94
Std Dev 0.8268
Turn on : 25.0000
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B0L100S, U2-ch47
calib_packv5_042523_0143.root, FC#6, port A1
Entries 58
Mean 45.36
Std Dev 6.994
Turn on : 40.5132
Width : 0.198
Height : 2.111
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
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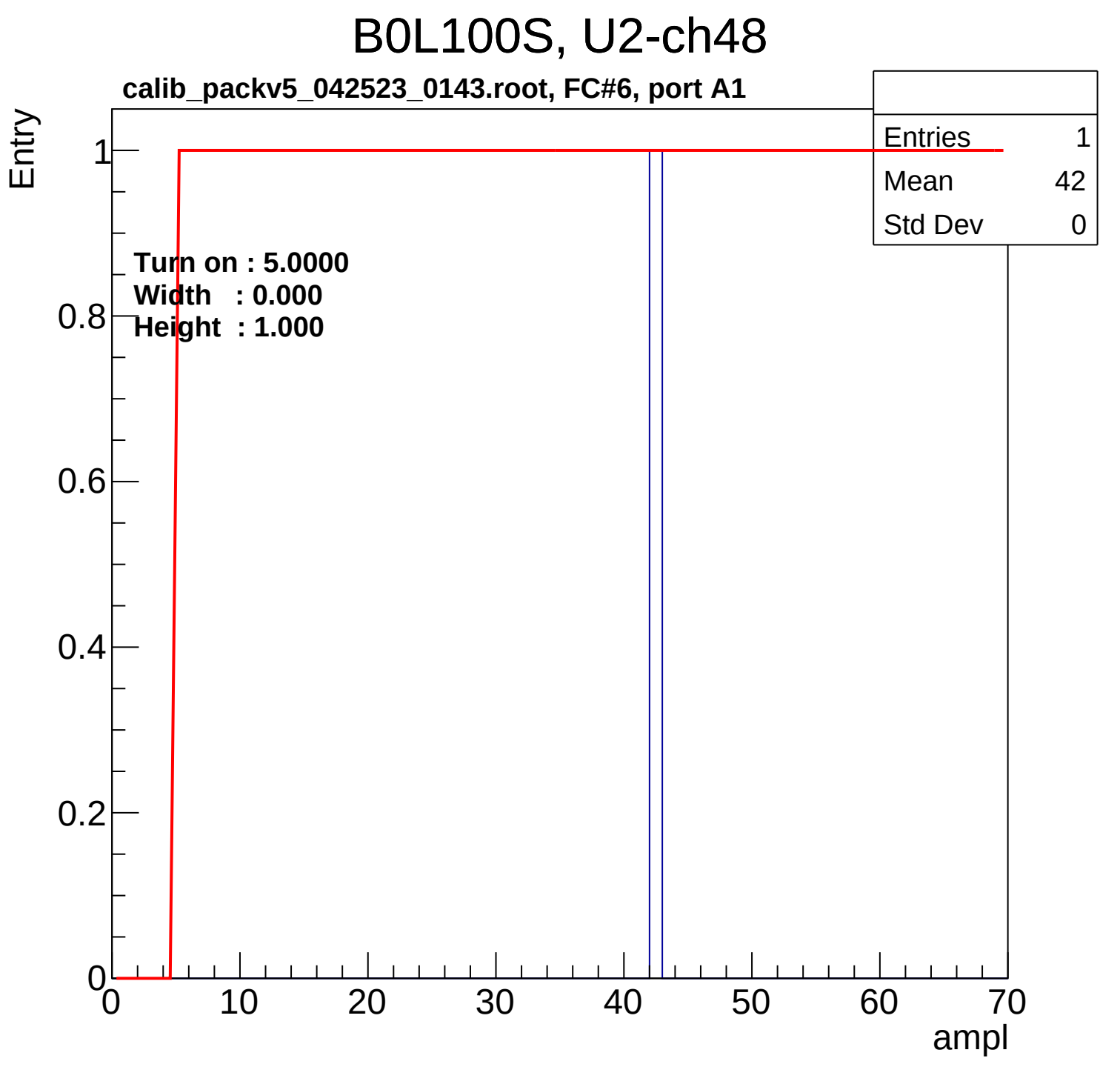
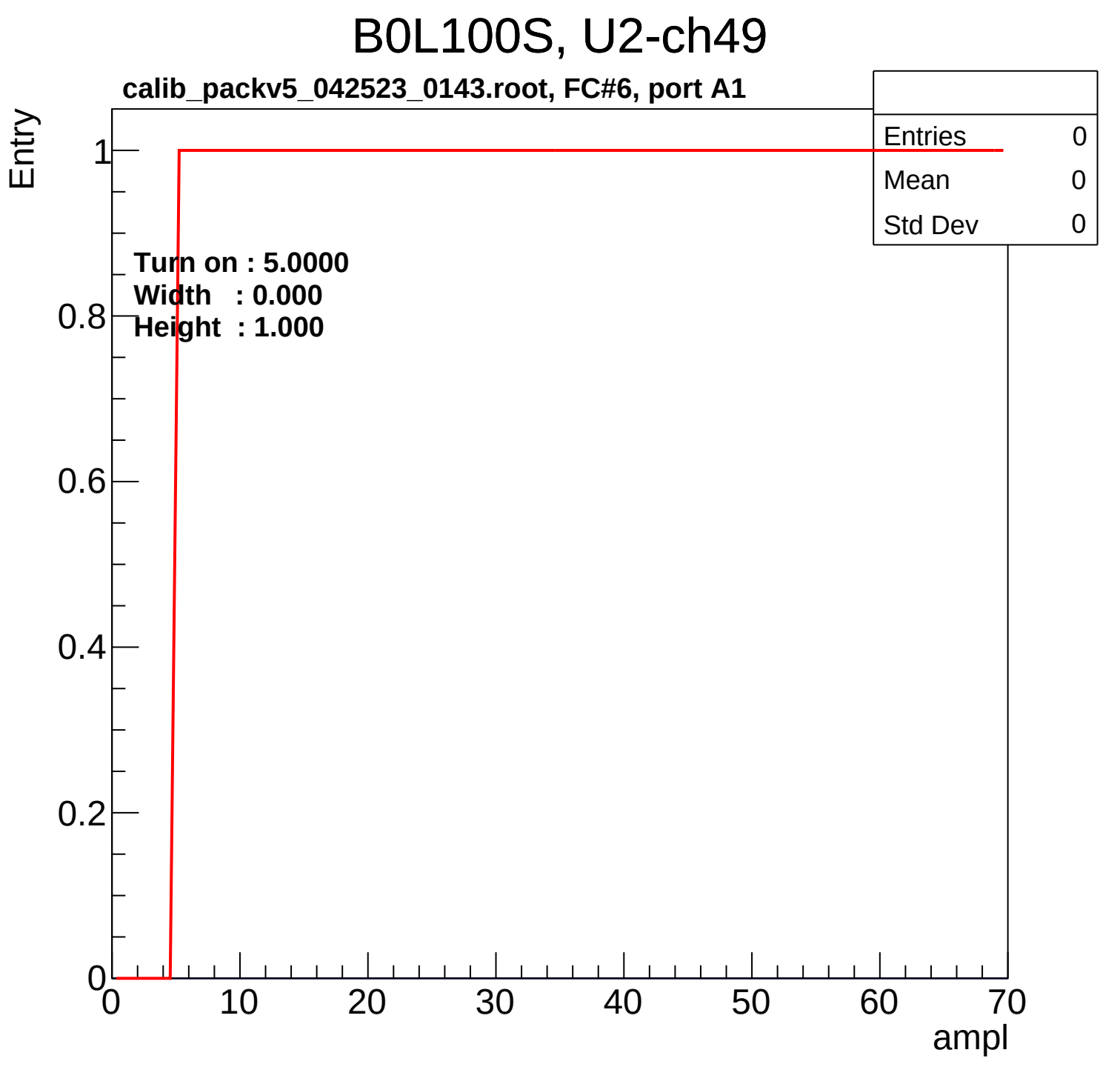
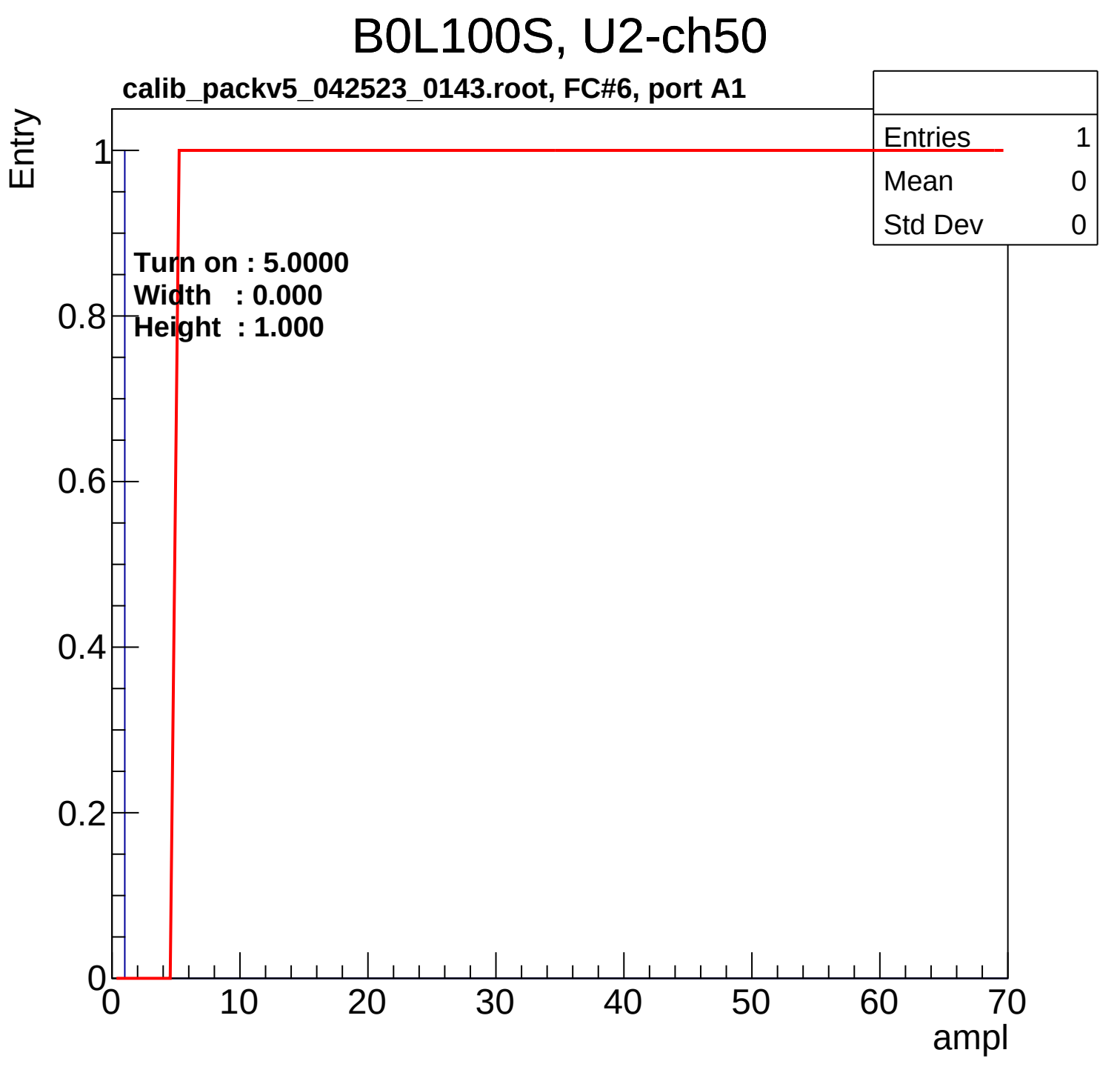
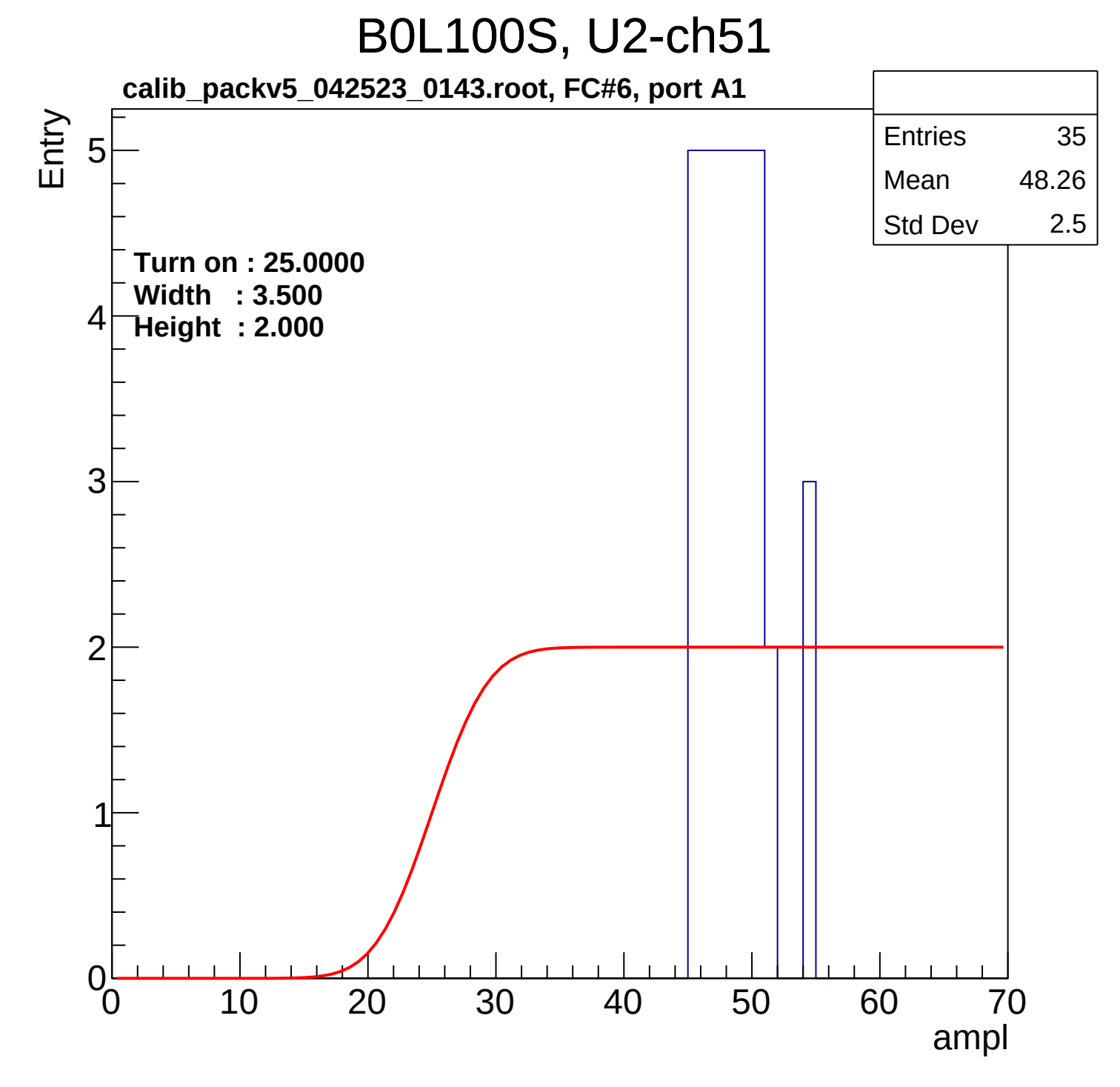
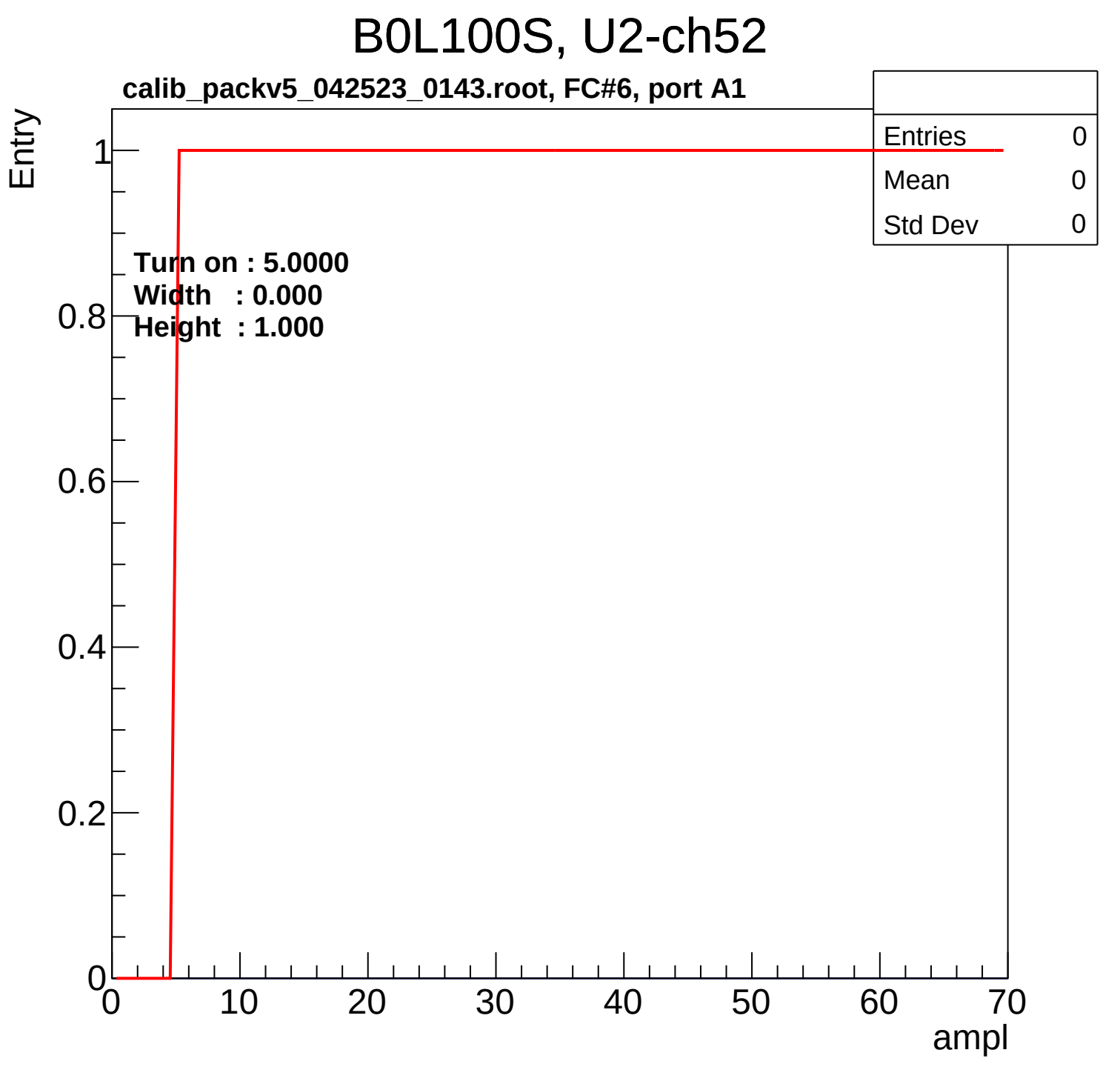
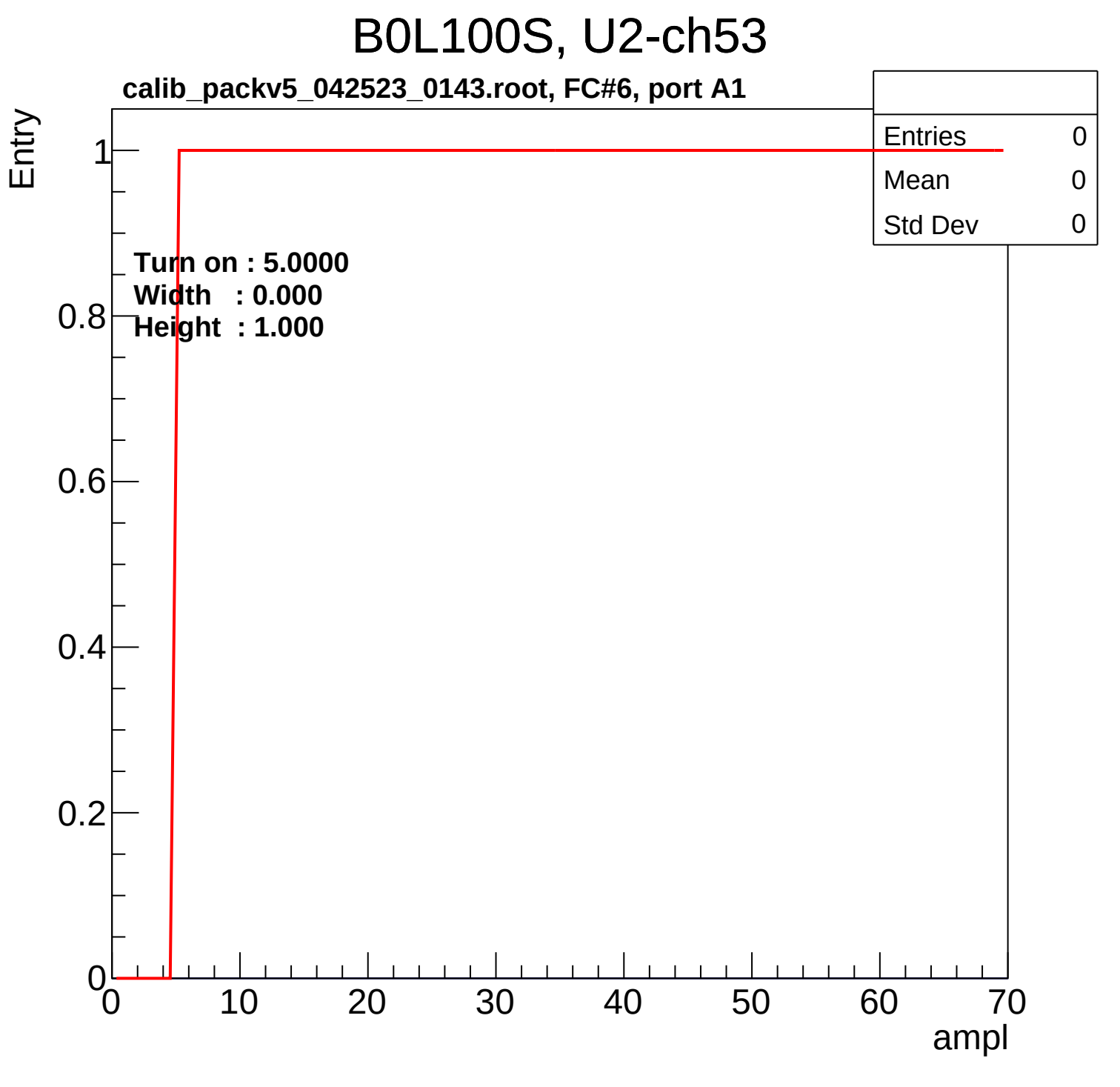

B0L100S, U2-ch48
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 42
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

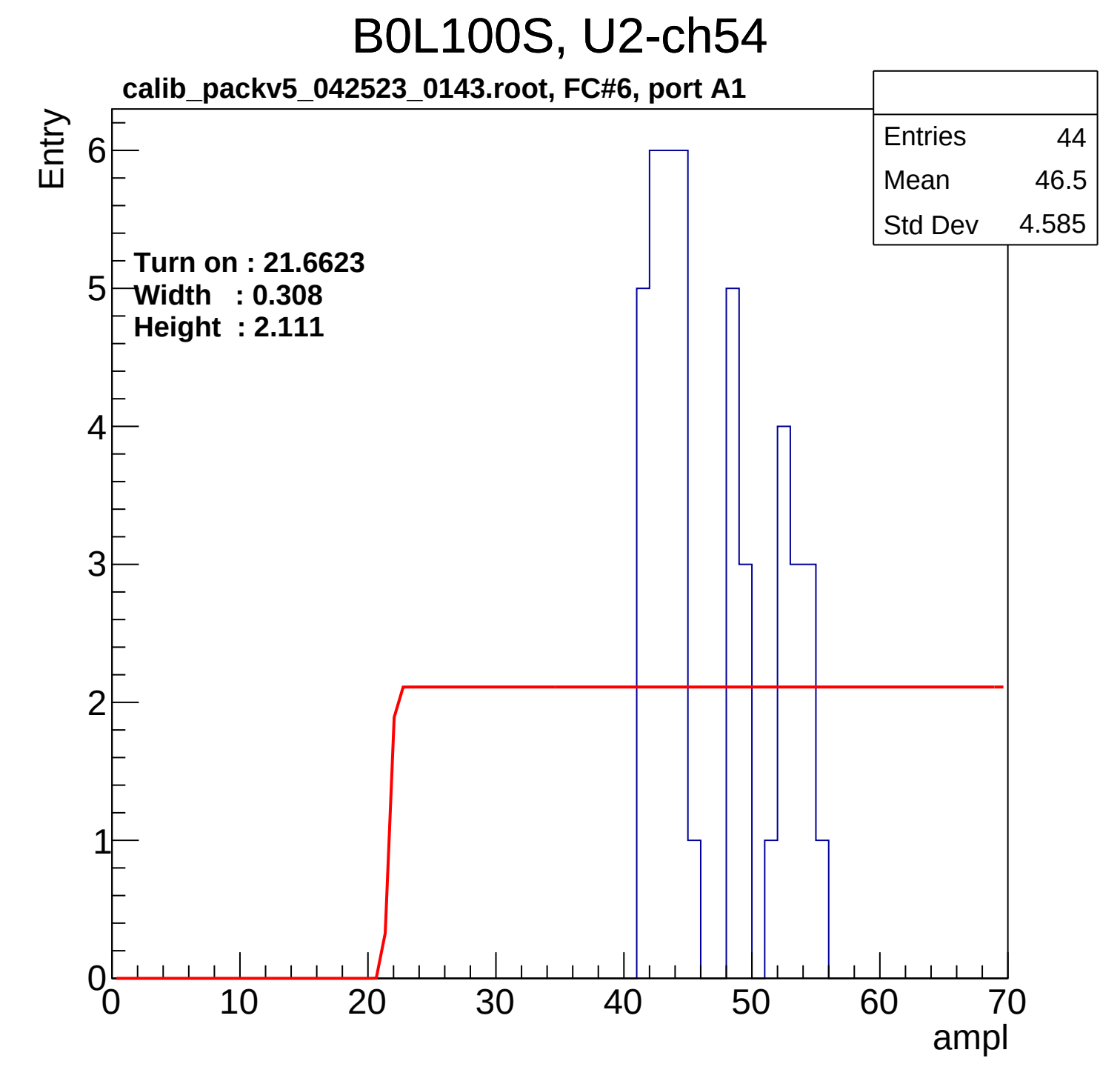

B0L100S, U2-ch49
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U2-ch50
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U2-ch51
calib_packv5_042523_0143.root, FC#6, port A1
Entries 35
Mean 48.26
Std Dev 2.5
Turn on : 25.0000
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B0L100S, U2-ch52
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U2-ch53
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U2-ch54
calib_packv5_042523_0143.root, FC#6, port A1
Entries 44
Mean 46.5
Std Dev 4.585
Turn on : 21.6623
Width : 0.308
Height : 2.111
Entry
ampl
0
1
2
3
4
5
6
0
10
20
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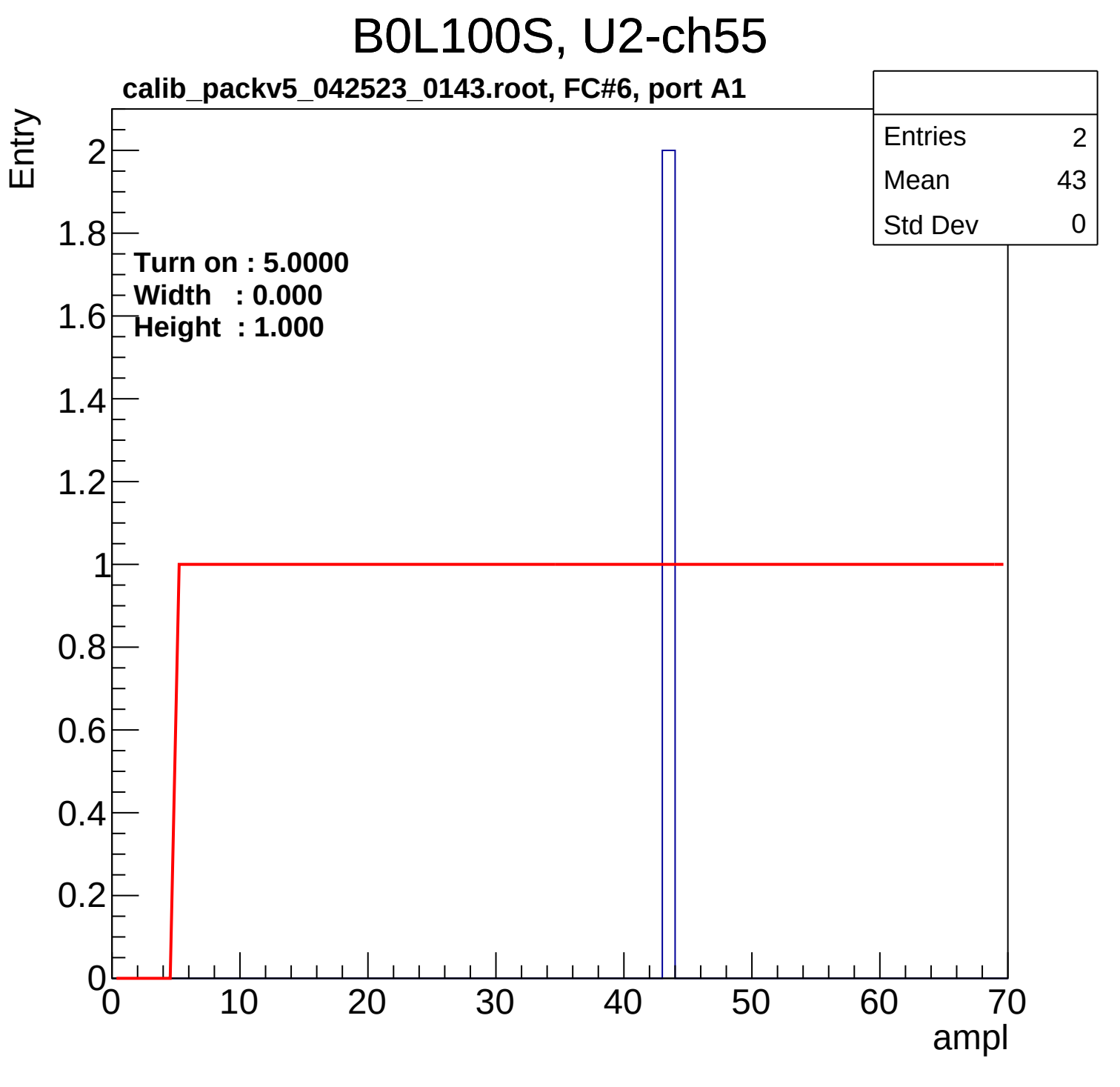
40
50
60
70


B0L100S, U2-ch55
calib_packv5_042523_0143.root, FC#6, port A1
Entries 2
Mean 43
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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40
50
60
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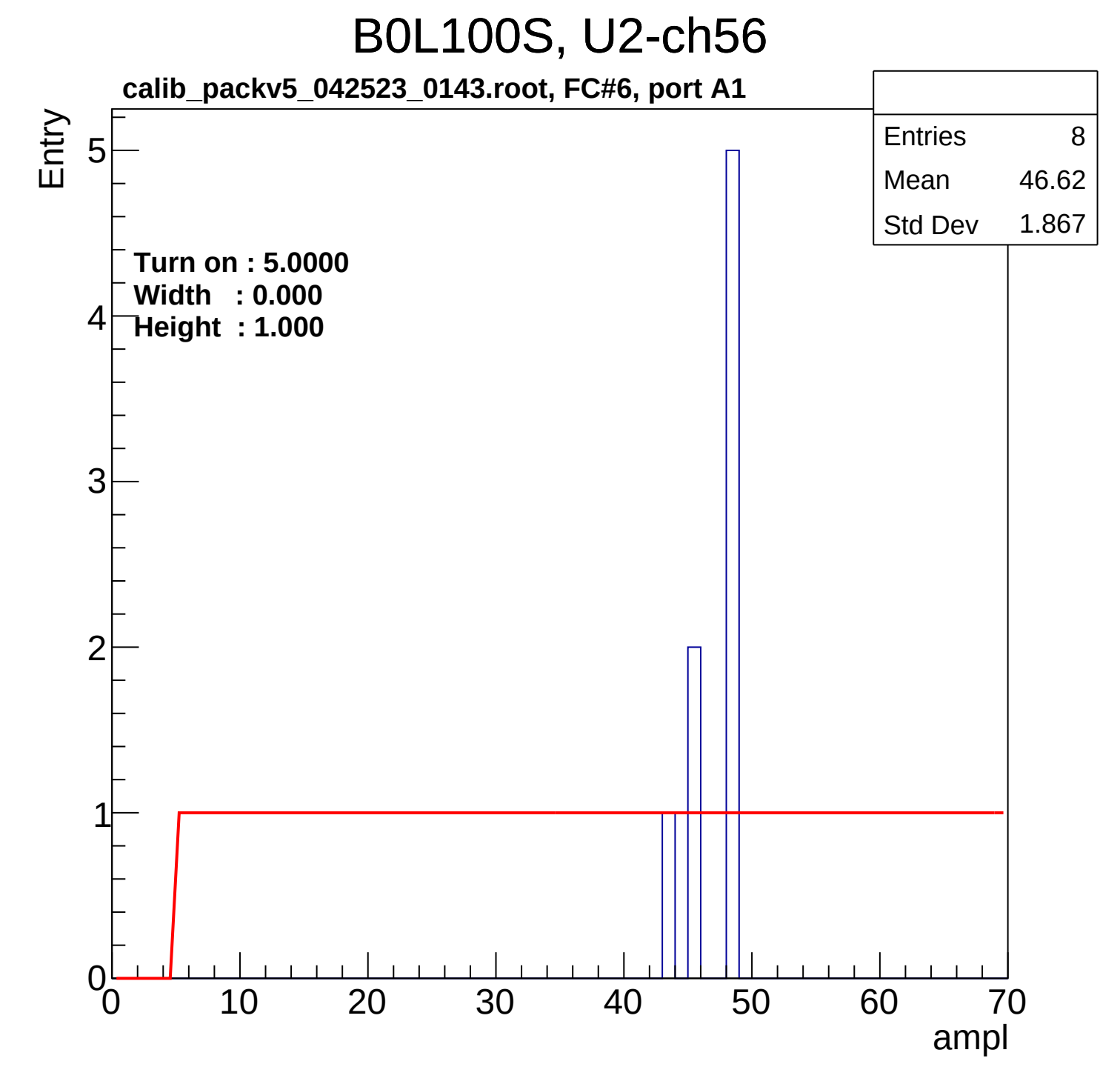
B0L100S, U2-ch56
calib_packv5_042523_0143.root, FC#6, port A1
Entries 8
Mean 46.62
Std Dev 1.867
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
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2
3
4
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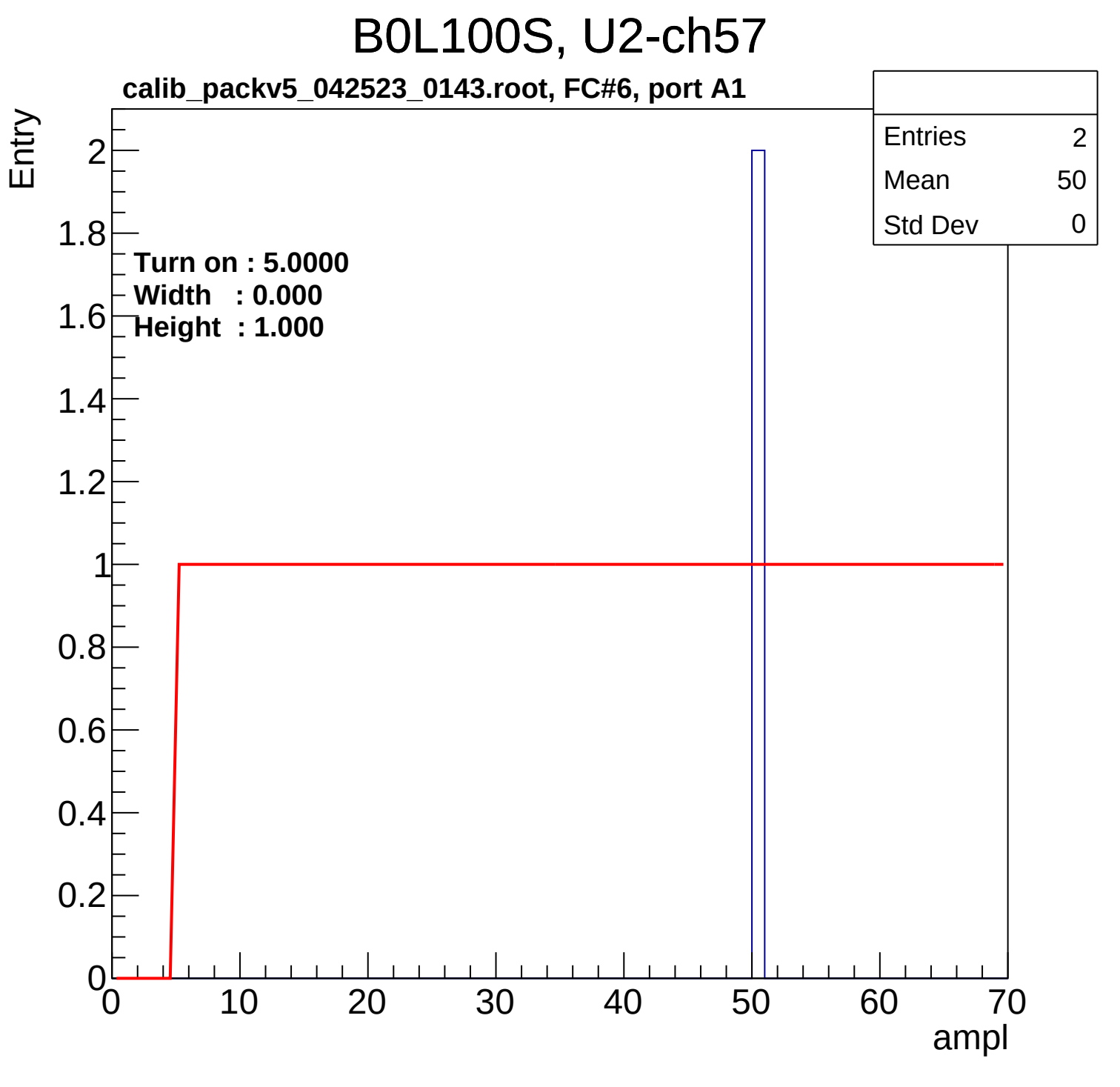
B0L100S, U2-ch57
calib_packv5_042523_0143.root, FC#6, port A1
Entries 2
Mean 50
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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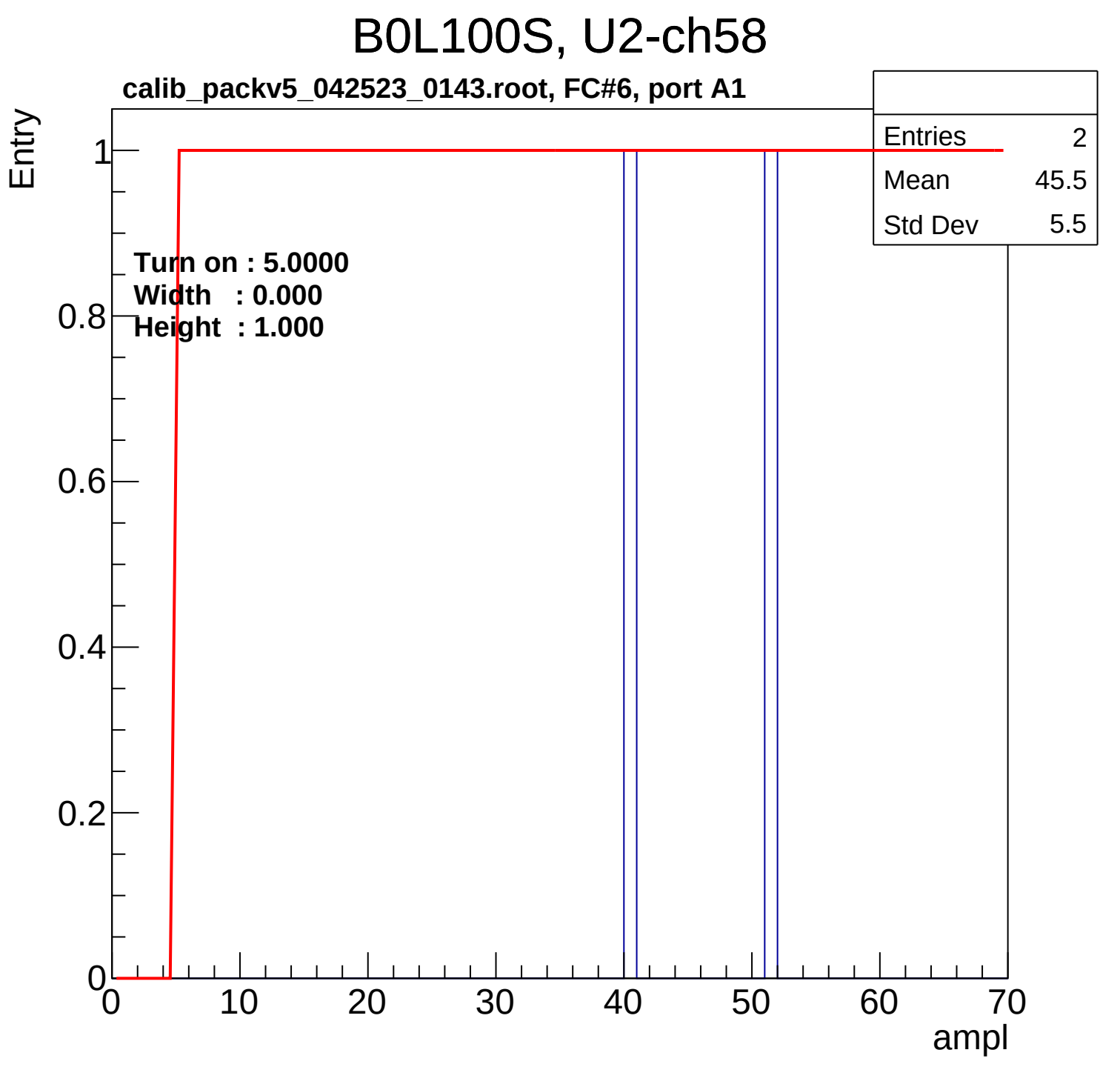
B0L100S, U2-ch58
calib_packv5_042523_0143.root, FC#6, port A1
Entries 2
Mean 45.5
Std Dev 5.5
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.2
0.4
0.6
0.8
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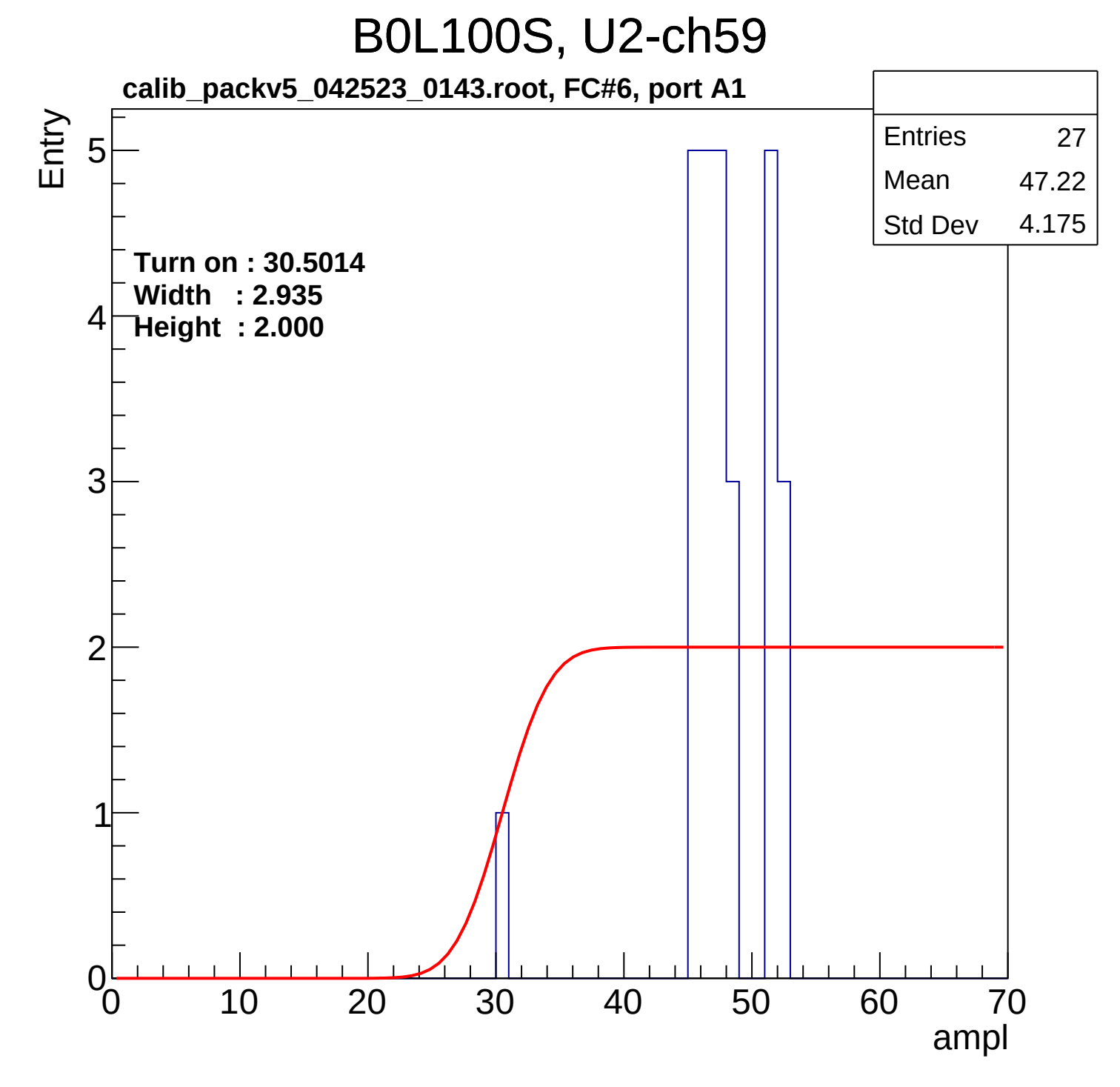
B0L100S, U2-ch59
calib_packv5_042523_0143.root, FC#6, port A1
Entries 27
Mean 47.22
Std Dev 4.175
Turn on : 30.5014
Width : 2.935
Height : 2.000
Entry
ampl
0
1
2
3
4
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0
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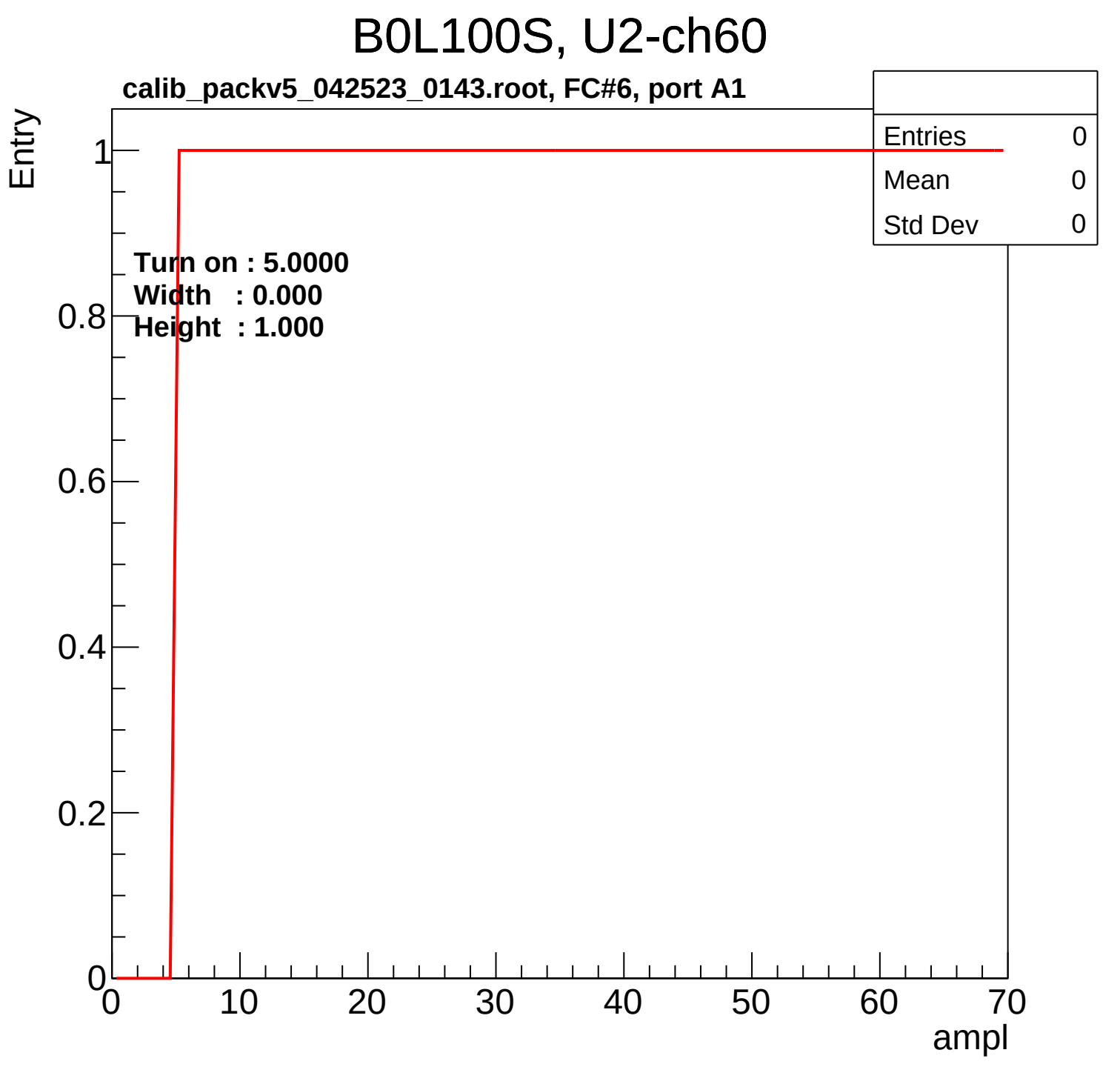
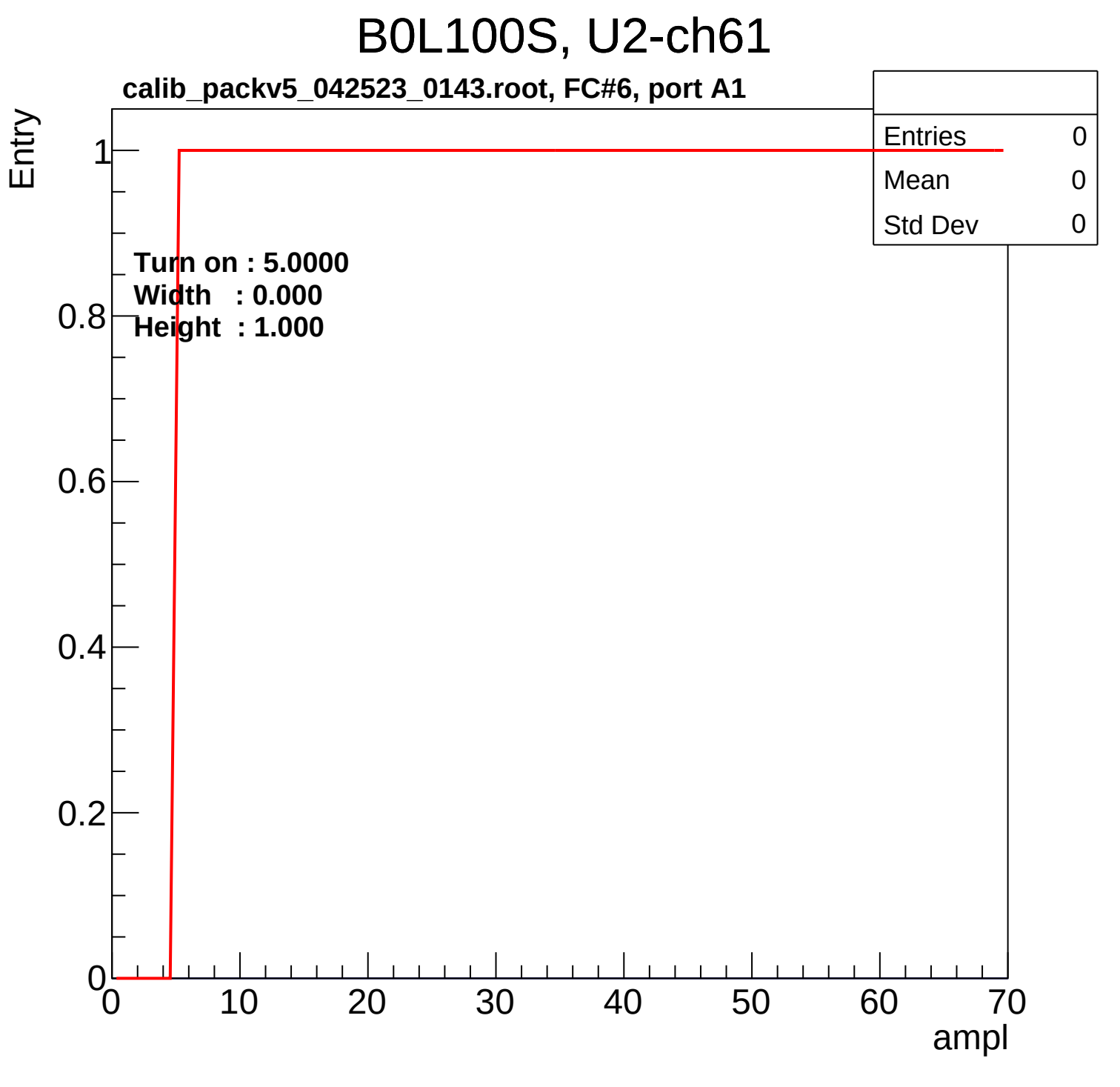
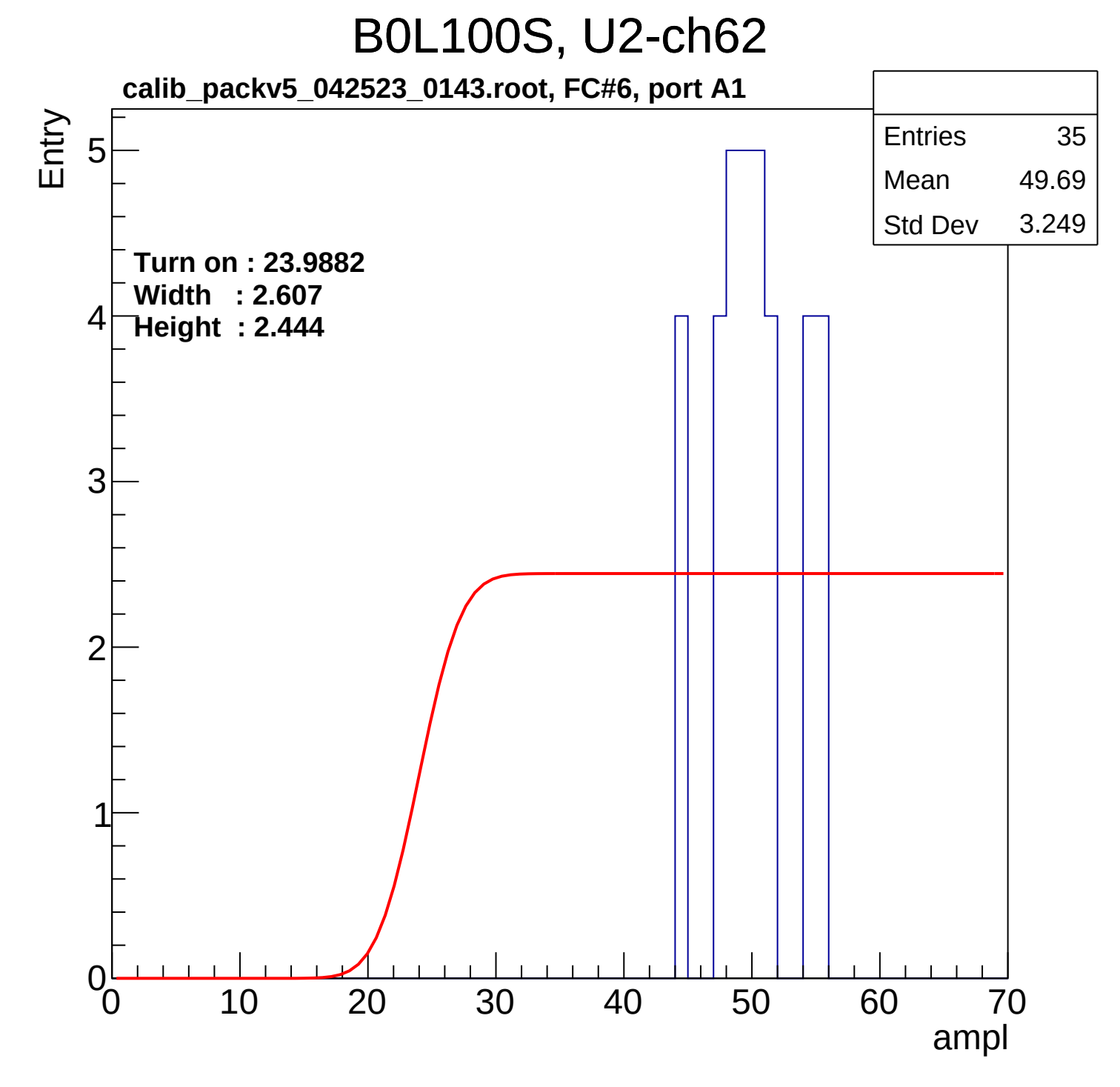

B0L100S, U2-ch60
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U2-ch61
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U2-ch62
calib_packv5_042523_0143.root, FC#6, port A1
Entries 35
Mean 49.69
Std Dev 3.249
Turn on : 23.9882
Width : 2.607
Height : 2.444
Entry
ampl
0
1
2
3
4
5
0
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40
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60
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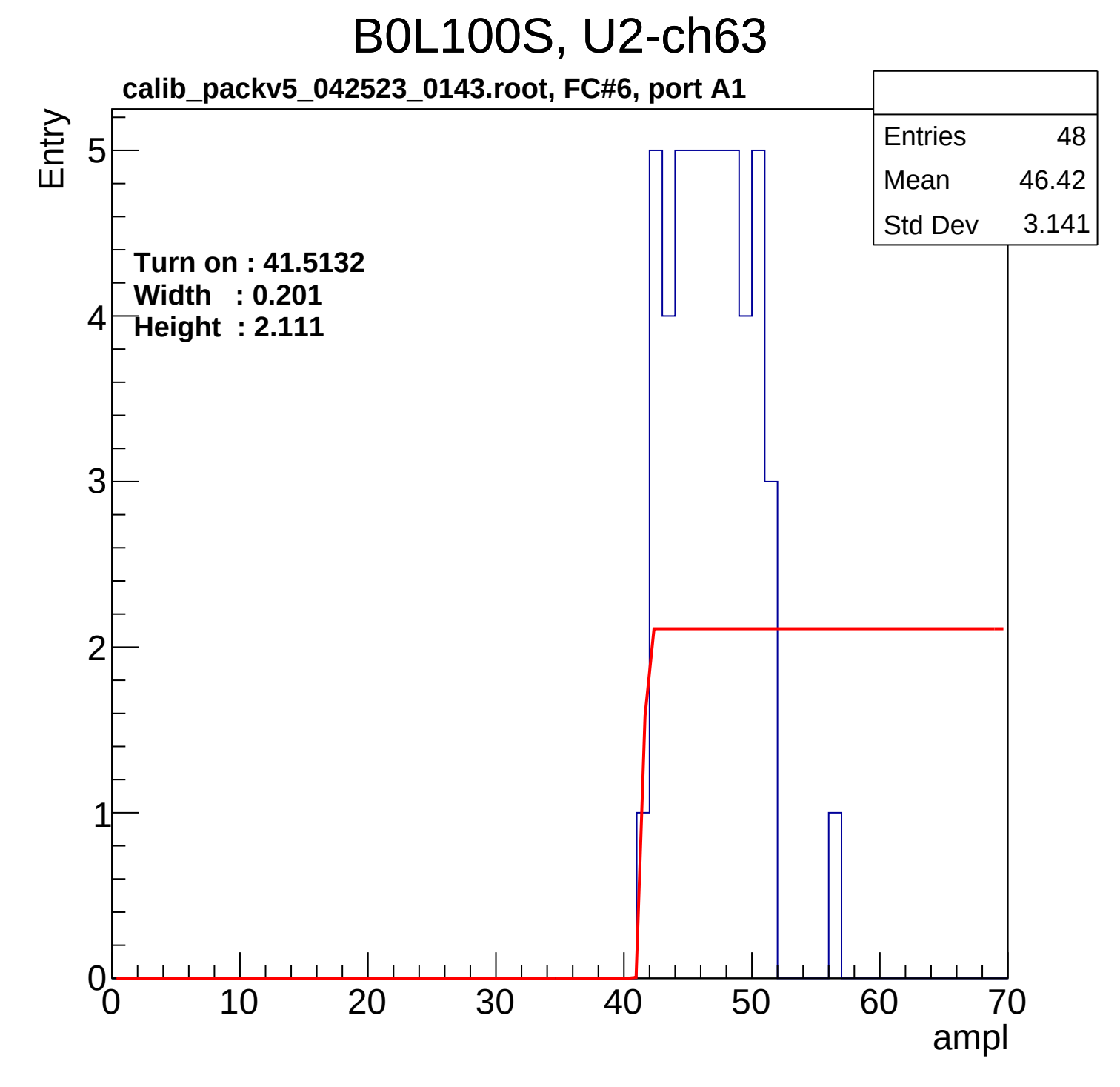
B0L100S, U2-ch63
calib_packv5_042523_0143.root, FC#6, port A1
Entries 48
Mean 46.42
Std Dev 3.141
Turn on : 41.5132
Width : 0.201
Height : 2.111
Entry
ampl
0
1
2
3
4
5
0
10
20
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40
50
60
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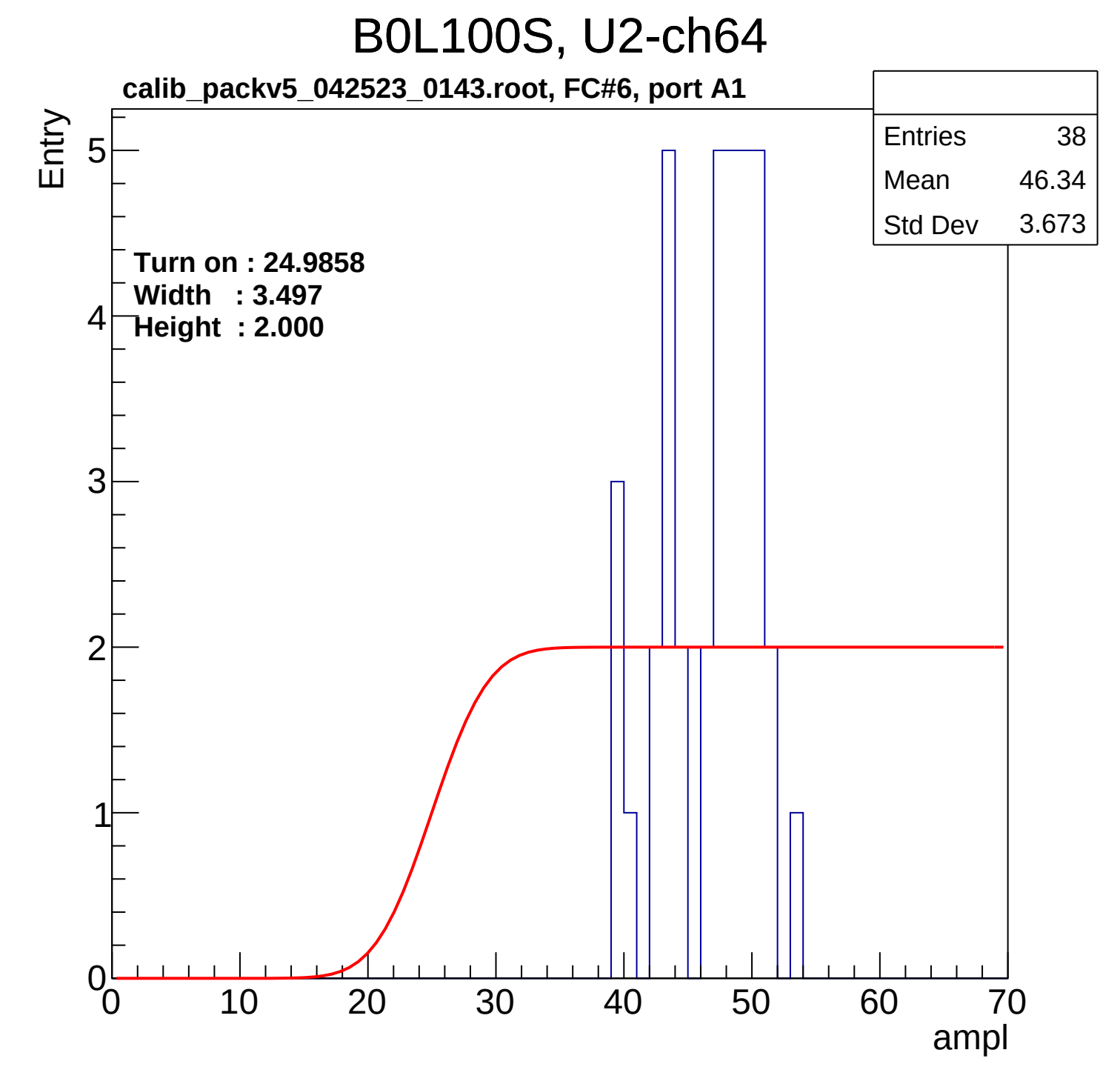
B0L100S, U2-ch64
calib_packv5_042523_0143.root, FC#6, port A1
Entries 38
Mean 46.34
Std Dev 3.673
Turn on : 24.9858
Width : 3.497
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
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40
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60
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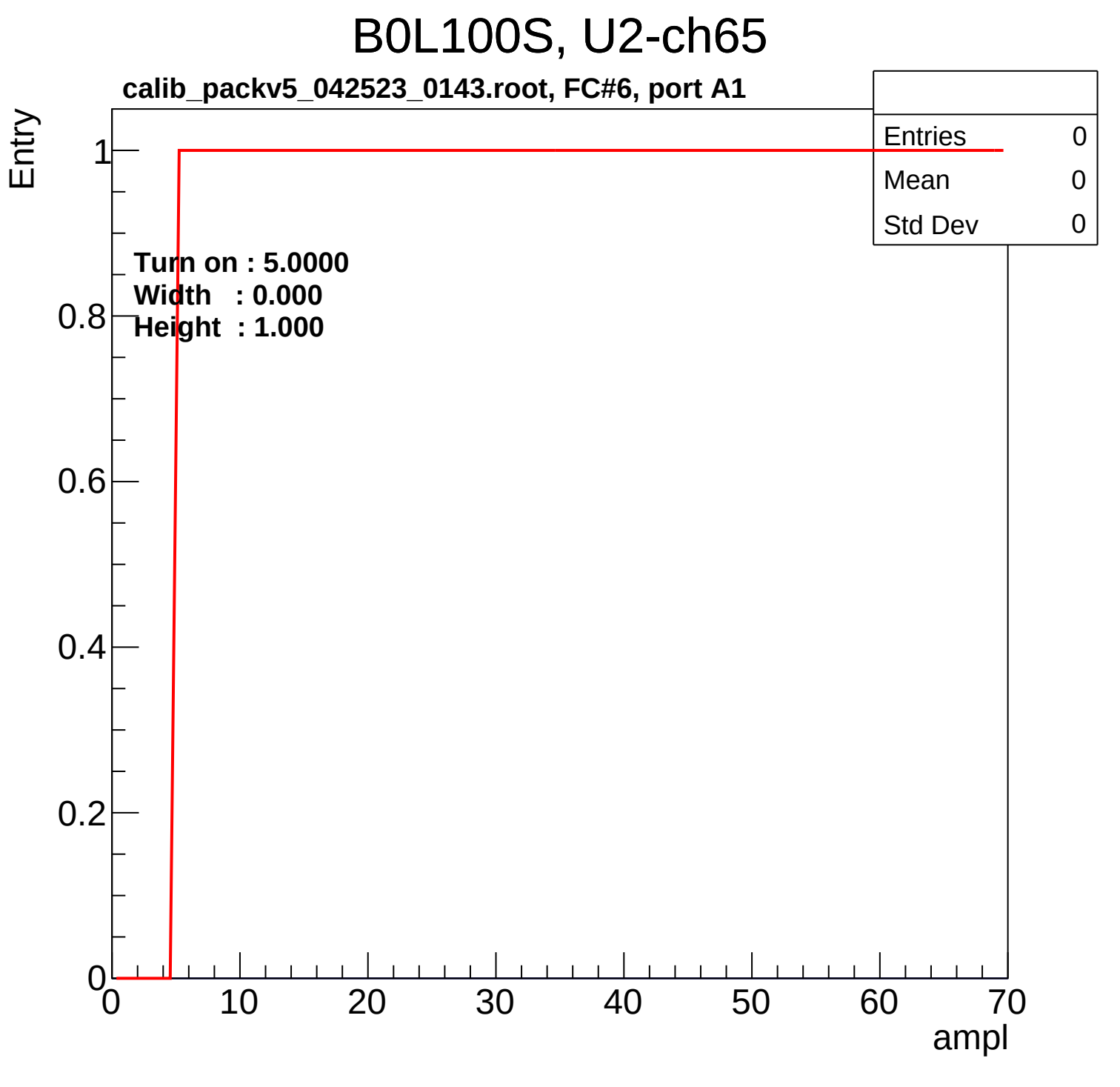
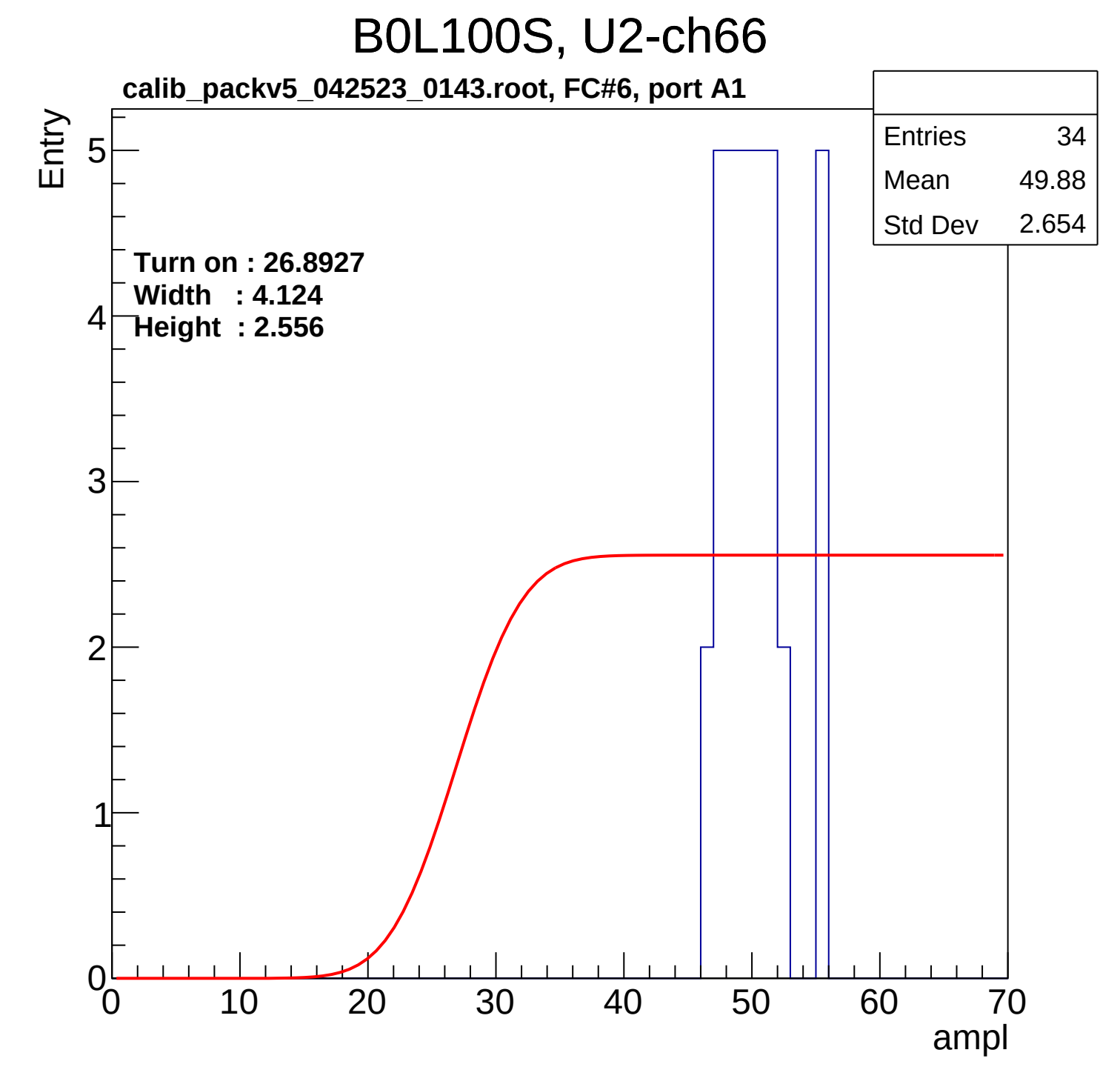

B0L100S, U2-ch65
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B0L100S, U2-ch66
calib_packv5_042523_0143.root, FC#6, port A1
Entries 34
Mean 49.88
Std Dev 2.654
Turn on : 26.8927
Width : 4.124
Height : 2.556
Entry
ampl
0
1
2
3
4
5
0
10
20
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40
50
60
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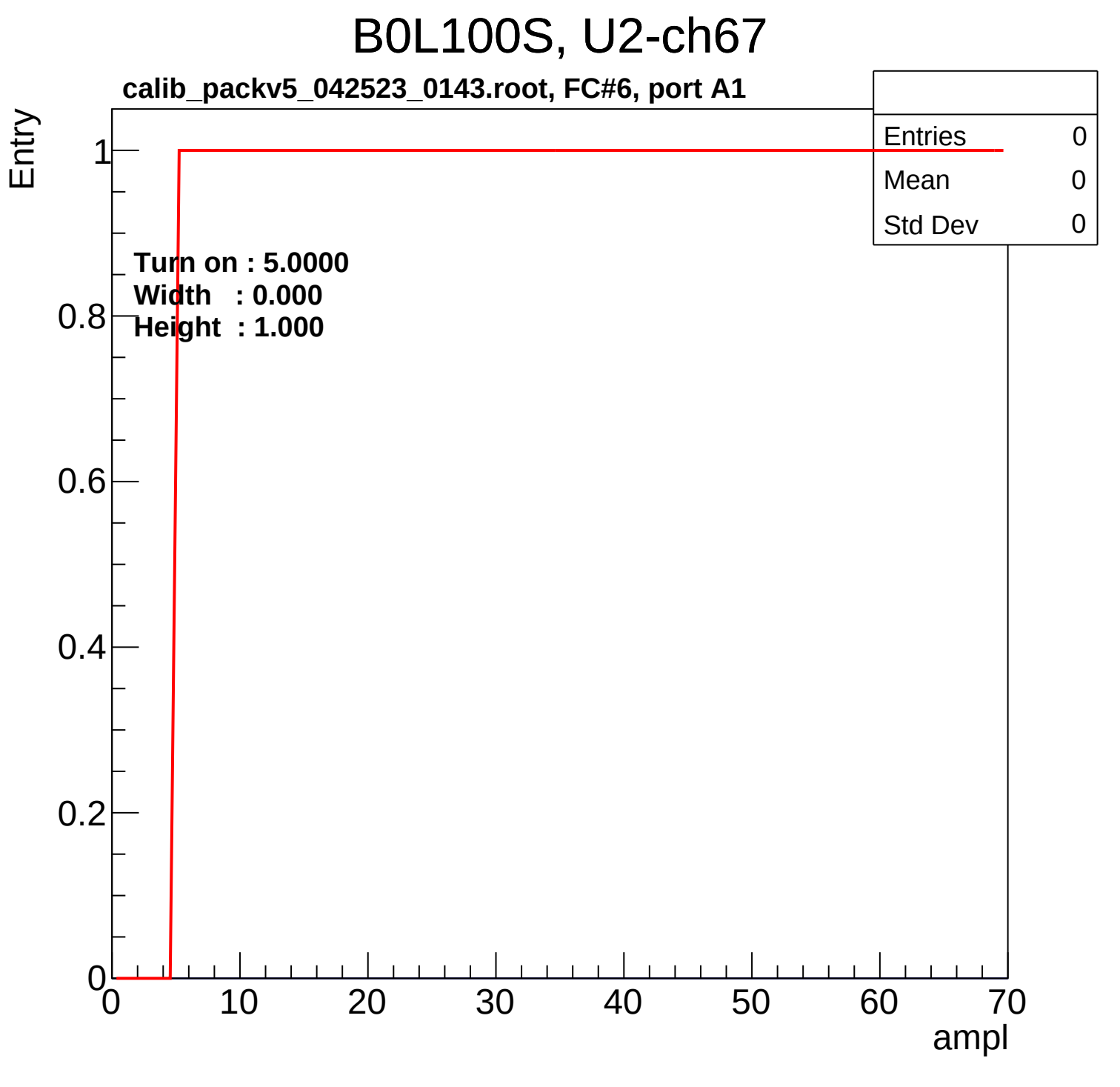
B0L100S, U2-ch67
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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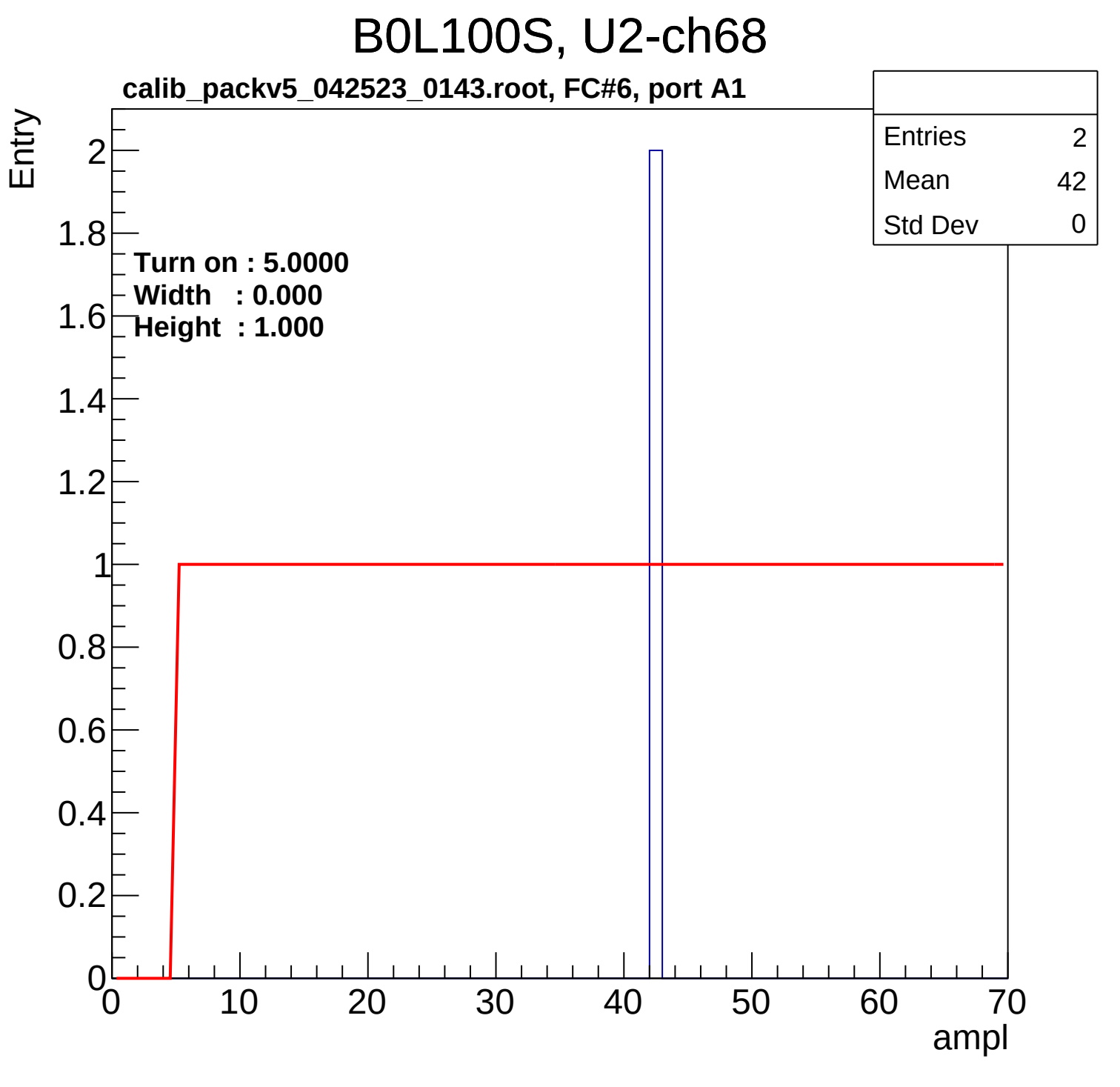
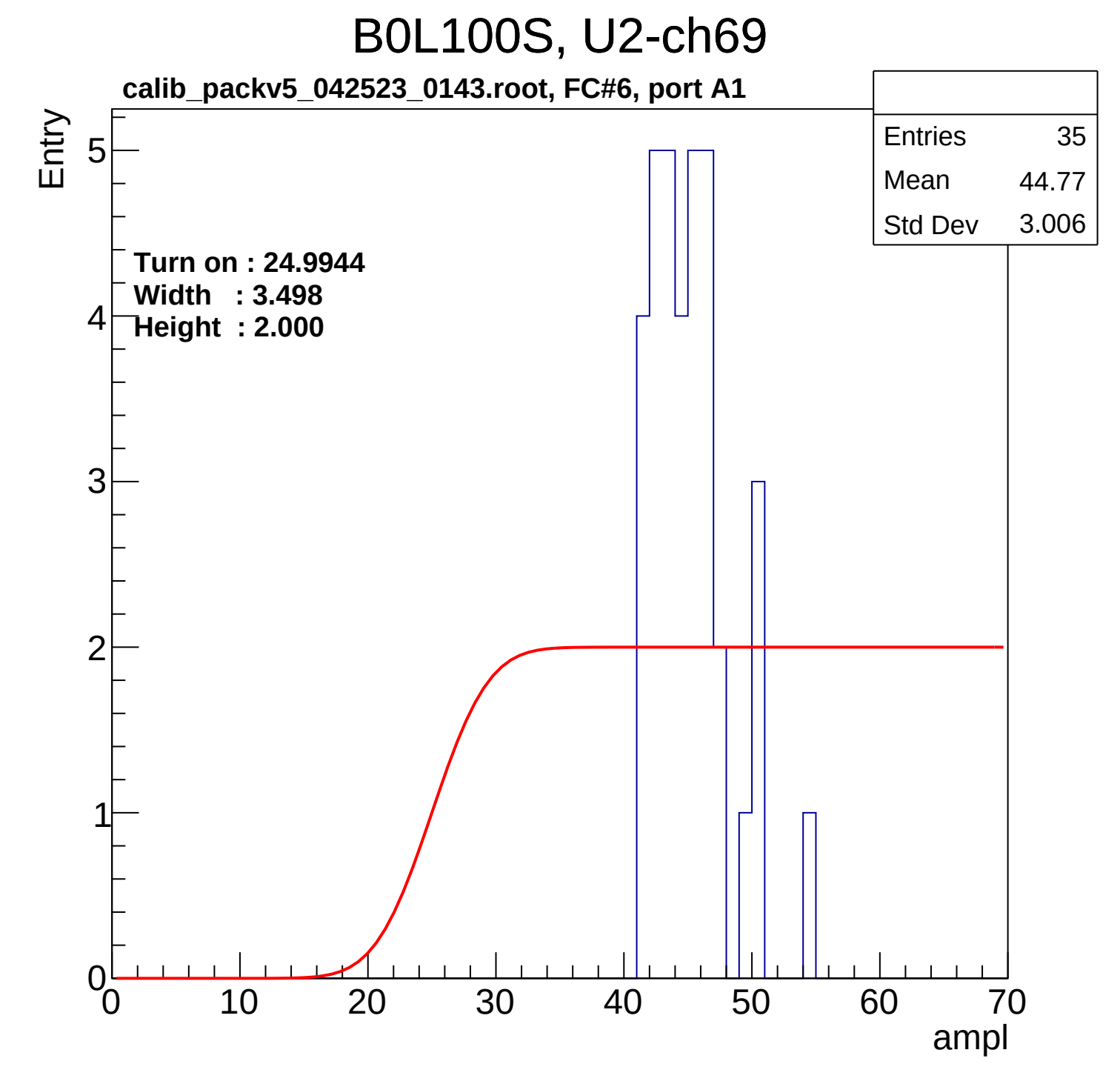
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U2-ch68
calib_packv5_042523_0143.root, FC#6, port A1
Entries 2
Mean 42
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B0L100S, U2-ch69
calib_packv5_042523_0143.root, FC#6, port A1
Entries 35
Mean 44.77
Std Dev 3.006
Turn on : 24.9944
Width : 3.498
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
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40
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60
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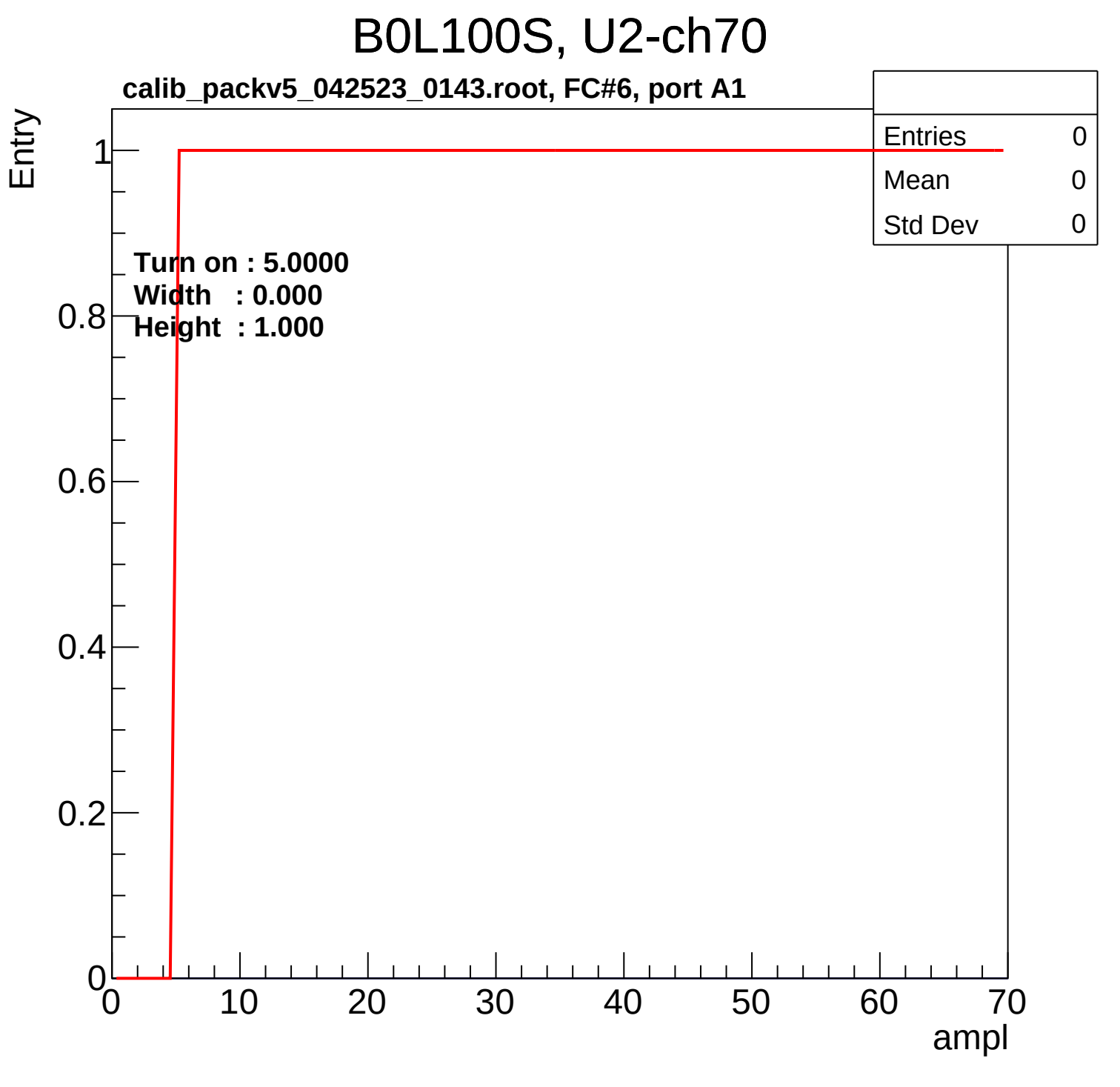
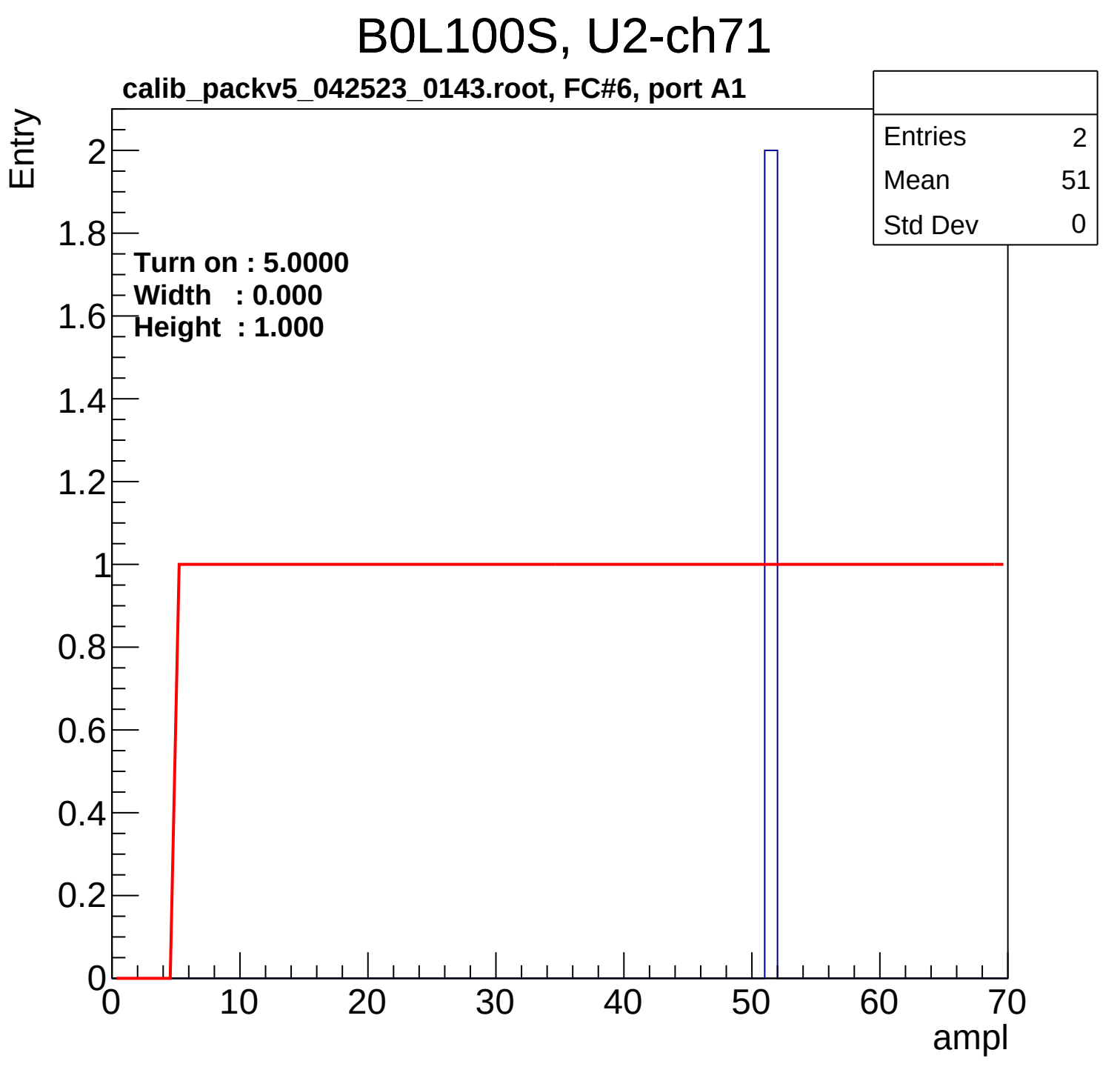
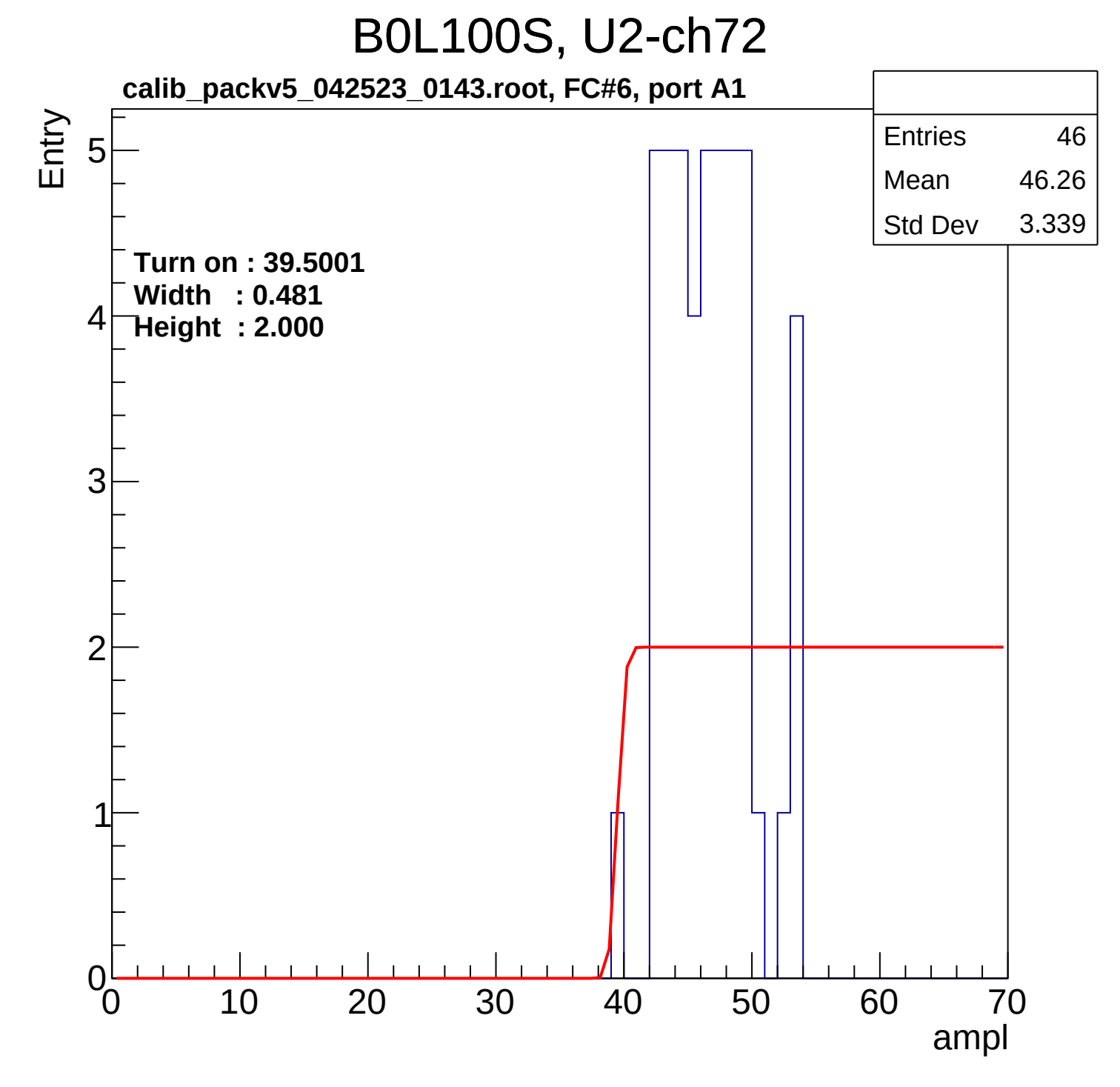

B0L100S, U2-ch70
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U2-ch71
calib_packv5_042523_0143.root, FC#6, port A1
Entries 2
Mean 51
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B0L100S, U2-ch72
calib_packv5_042523_0143.root, FC#6, port A1
Entries 46
Mean 46.26
Std Dev 3.339
Turn on : 39.5001
Width : 0.481
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
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60
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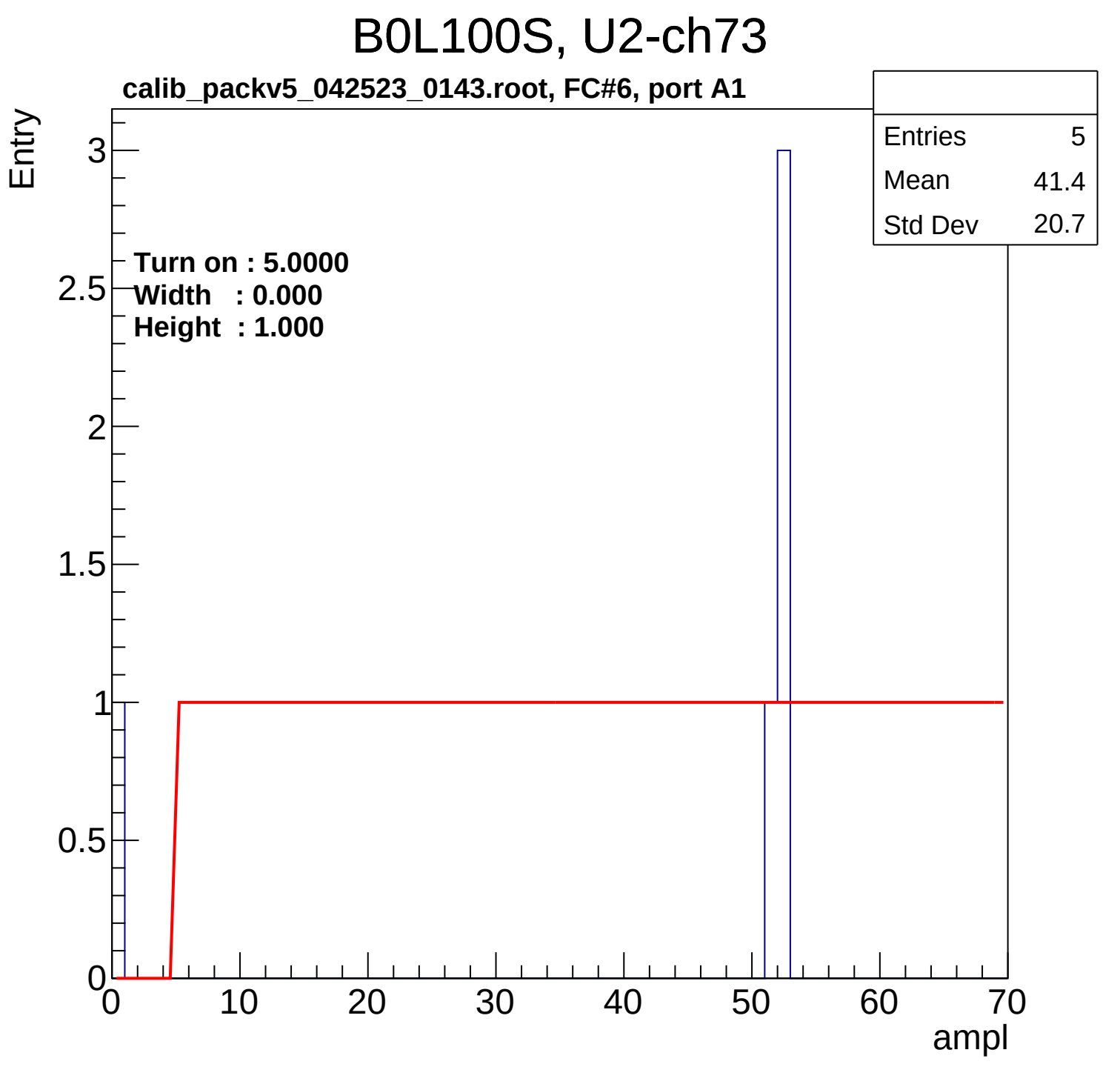
B0L100S, U2-ch73
calib_packv5_042523_0143.root, FC#6, port A1
Entries 5
Mean 41.4
Std Dev 20.7
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
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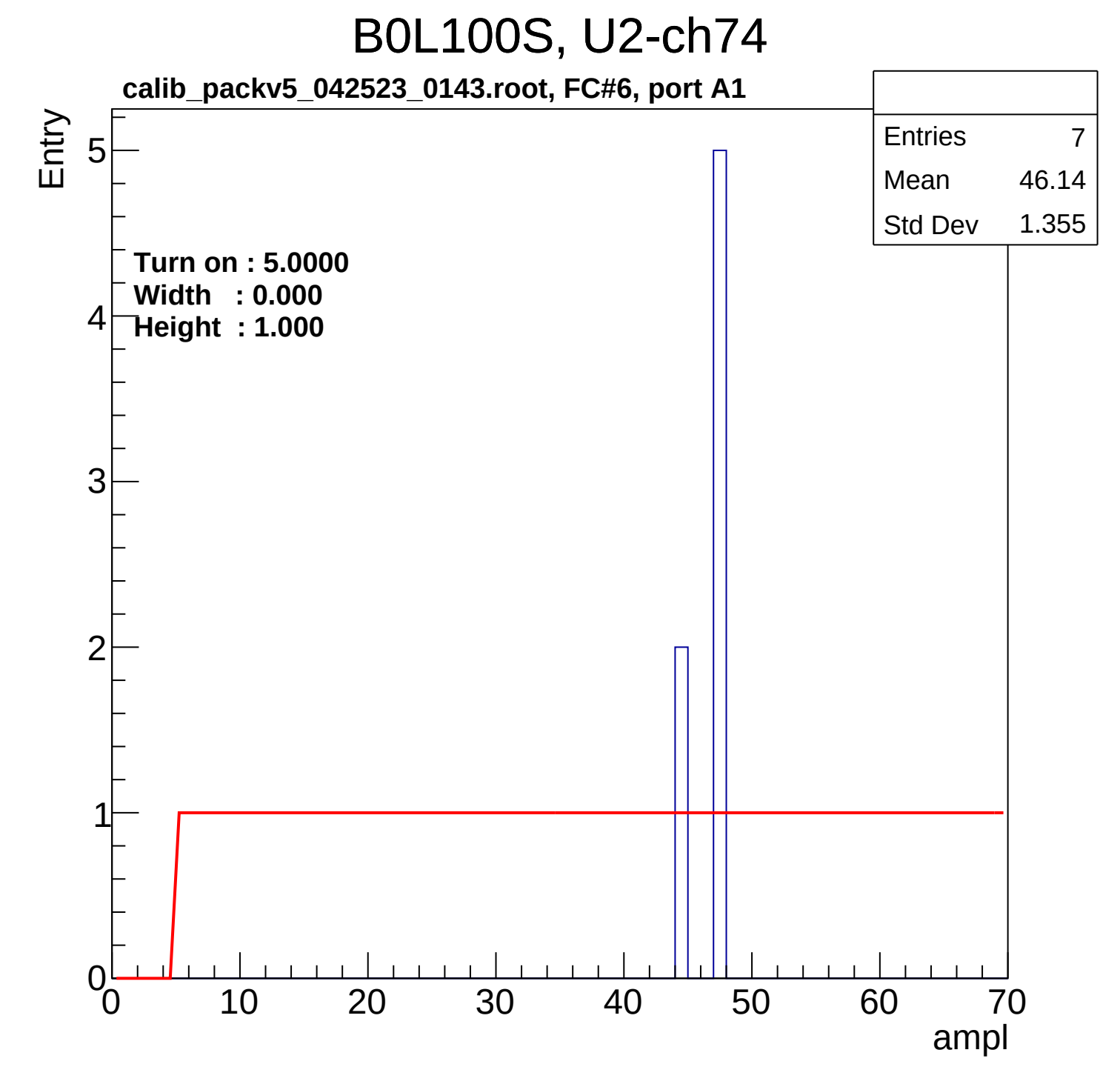
B0L100S, U2-ch74
calib_packv5_042523_0143.root, FC#6, port A1
Entries 7
Mean 46.14
Std Dev 1.355
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
1
2
3
4
5
0
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40
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60
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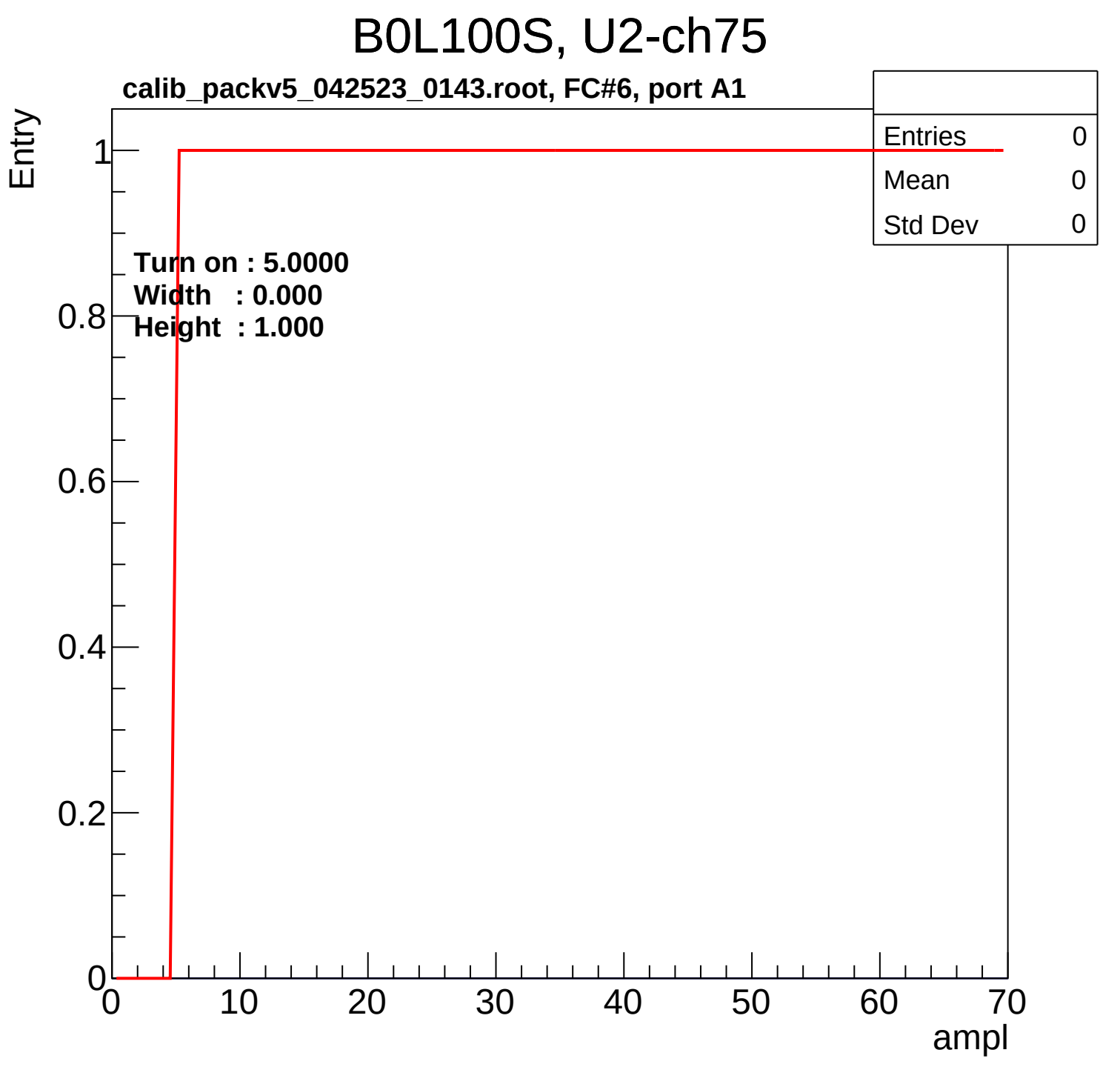
B0L100S, U2-ch75
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
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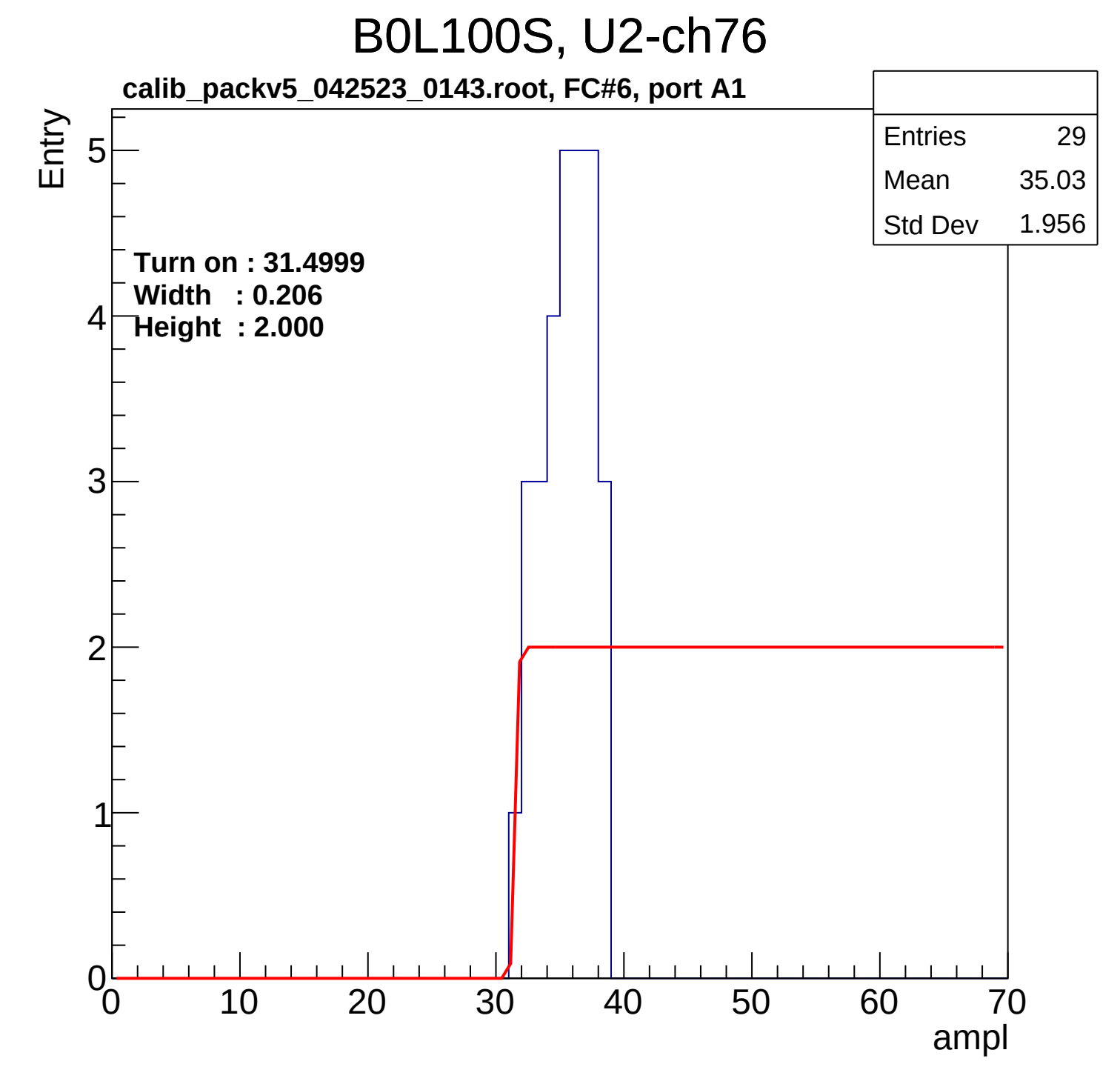
50
60
70
ampl


B0L100S, U2-ch76
calib_packv5_042523_0143.root, FC#6, port A1
Entries 29
Mean 35.03
Std Dev 1.956
Turn on : 31.4999
Width : 0.206
Height : 2.000
Entry
ampl
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1
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3
4
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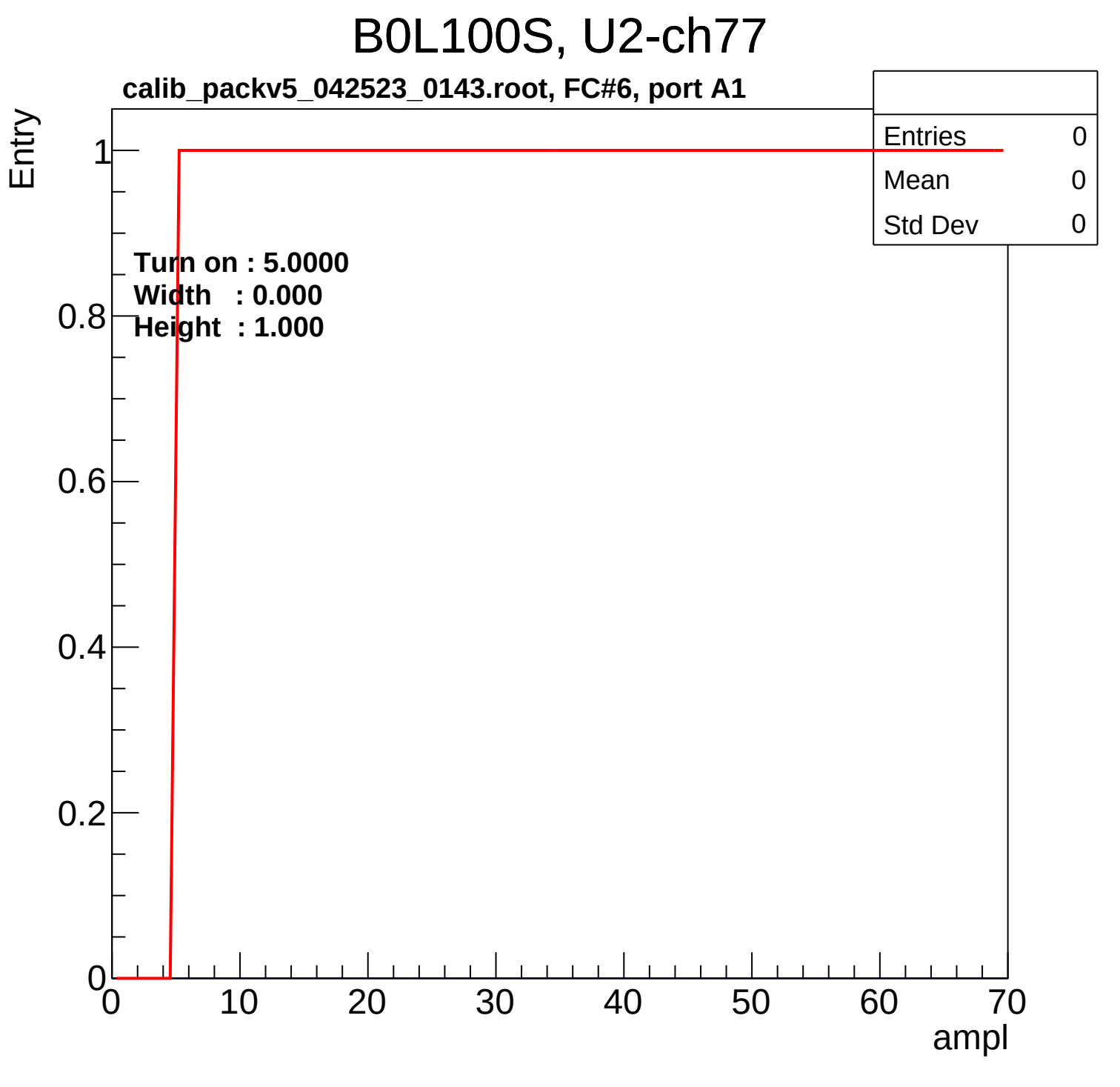
B0L100S, U2-ch77
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
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10
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30
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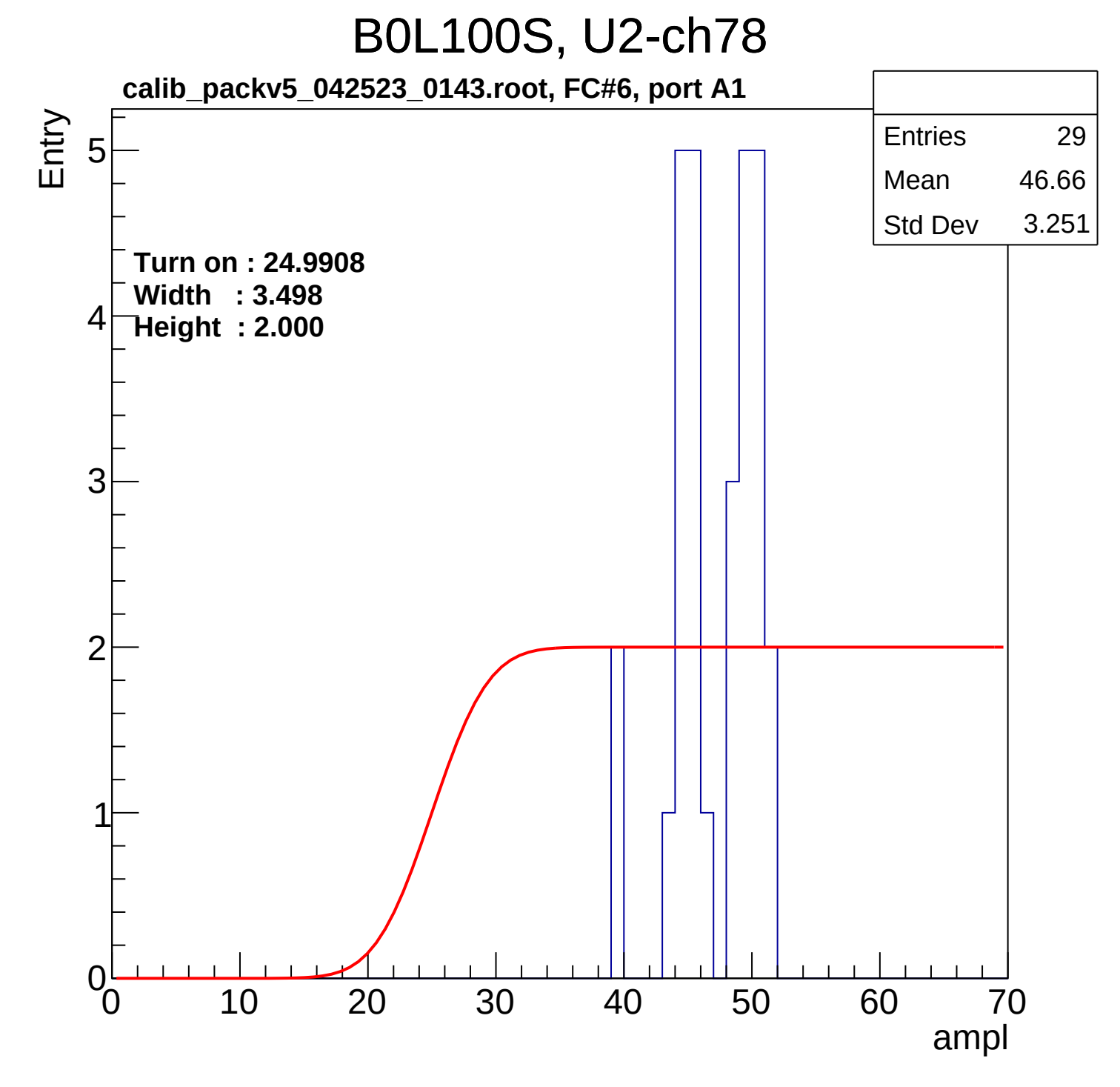
50
60
70
ampl


B0L100S, U2-ch78
calib_packv5_042523_0143.root, FC#6, port A1
Entries 29
Mean 46.66
Std Dev 3.251
Turn on : 24.9908
Width : 3.498
Height : 2.000
Entry
ampl
0
1
2
3
4
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0
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60
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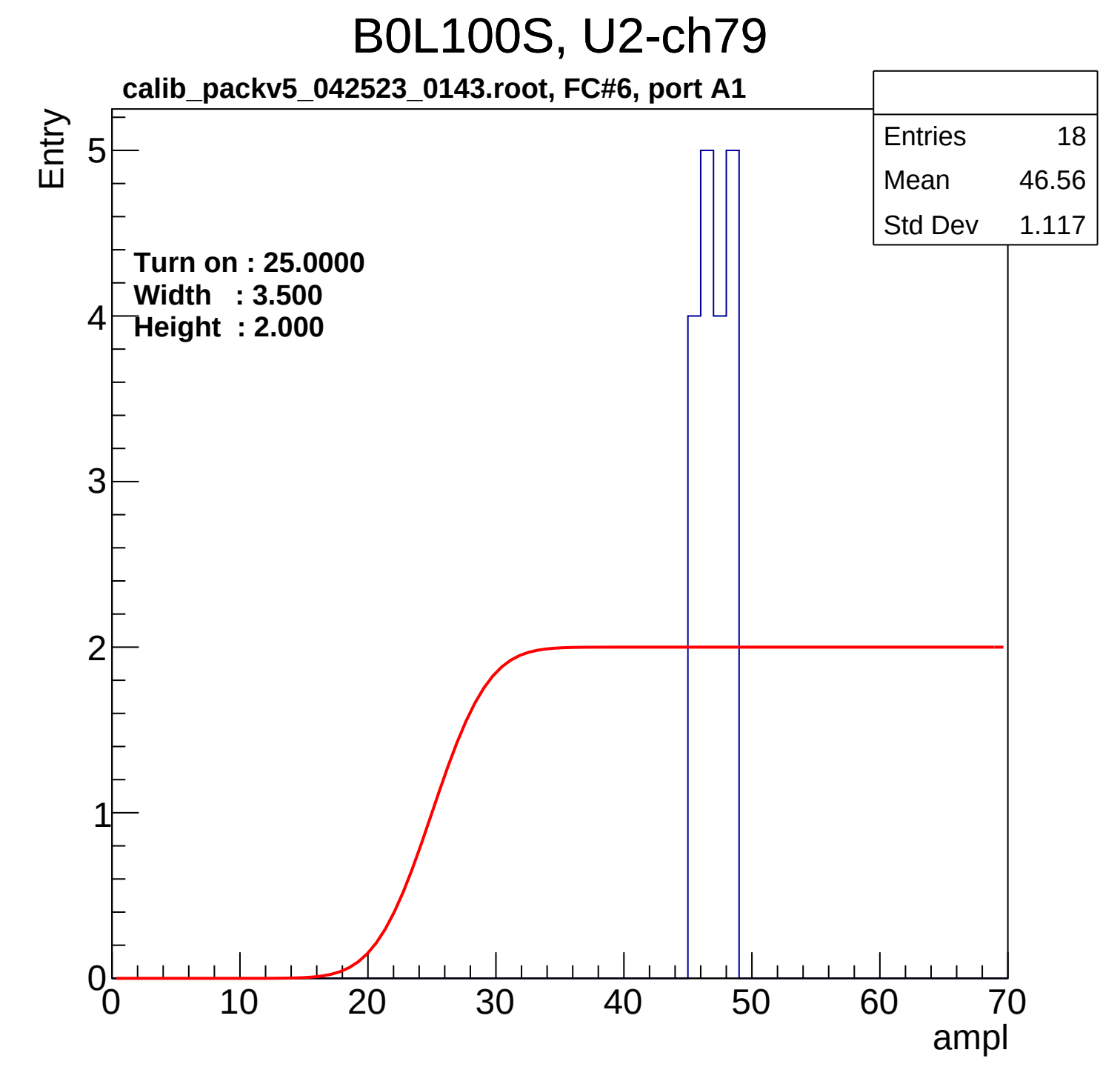
B0L100S, U2-ch79
calib_packv5_042523_0143.root, FC#6, port A1
Entries 18
Mean 46.56
Std Dev 1.117
Turn on : 25.0000
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
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0
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60
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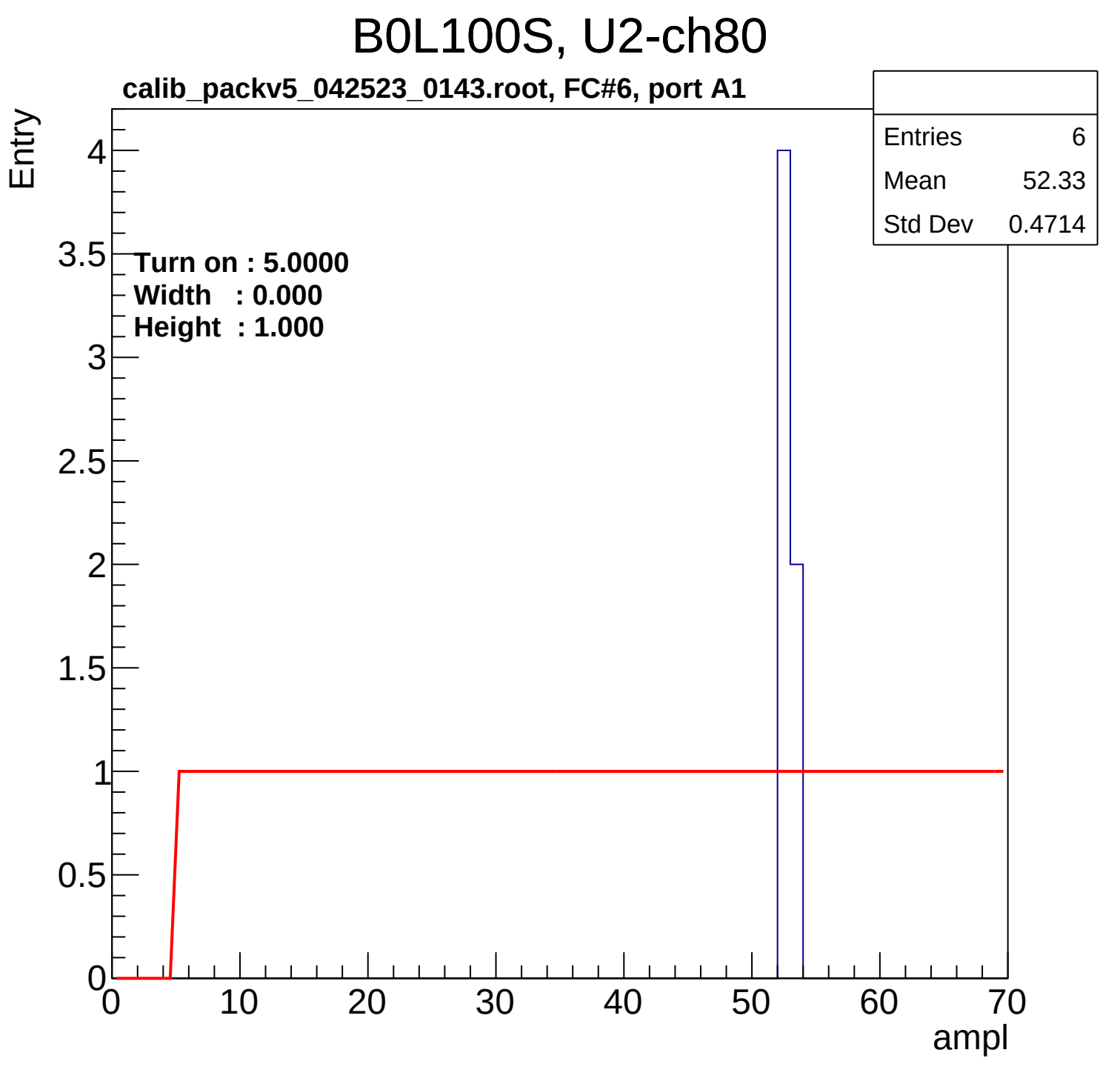
B0L100S, U2-ch80
calib_packv5_042523_0143.root, FC#6, port A1
Entries 6
Mean 52.33
Std Dev 0.4714
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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1.5
2
2.5
3
3.5
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0
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60
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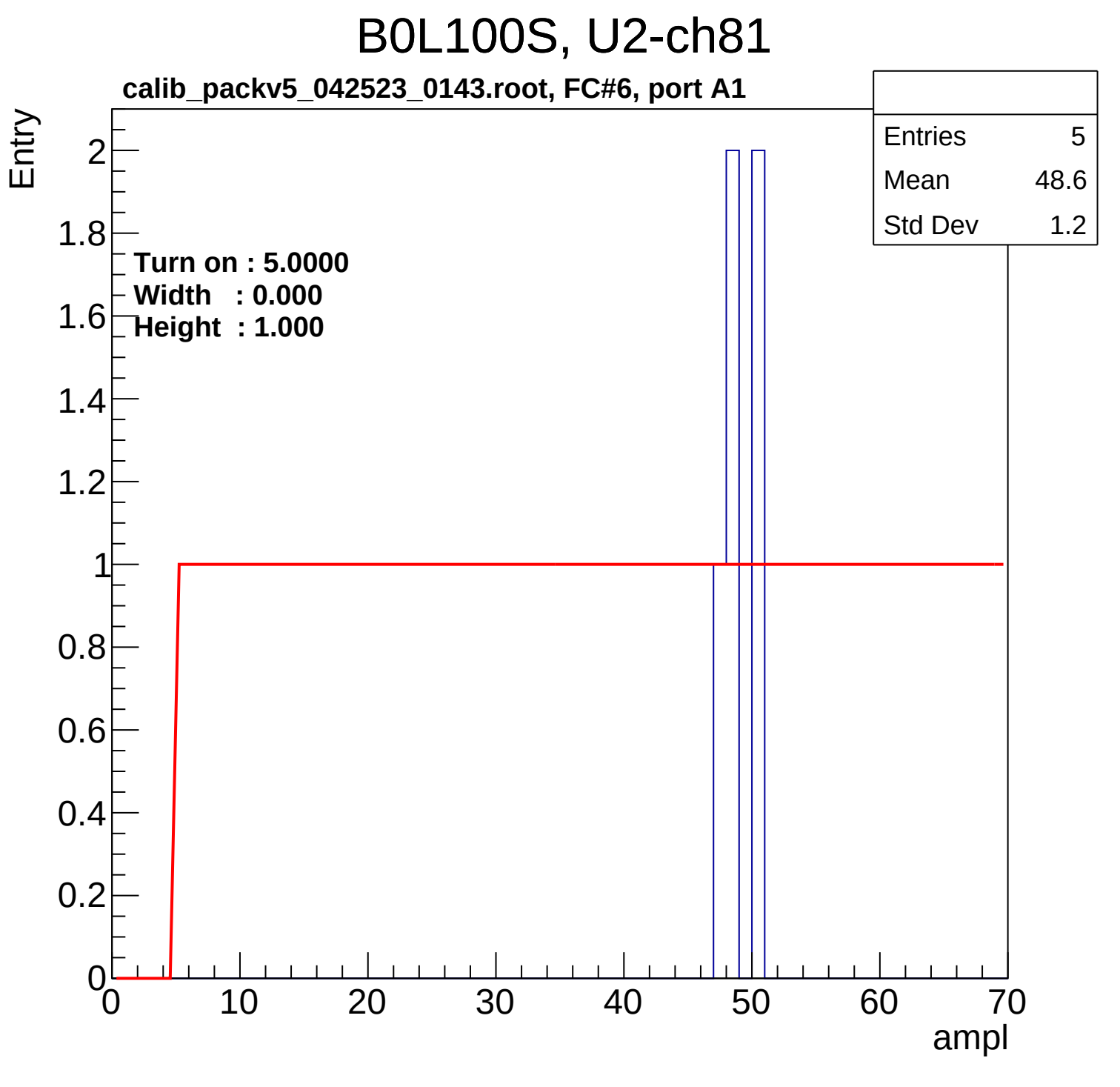
B0L100S, U2-ch81
calib_packv5_042523_0143.root, FC#6, port A1
Entries 5
Mean 48.6
Std Dev 1.2
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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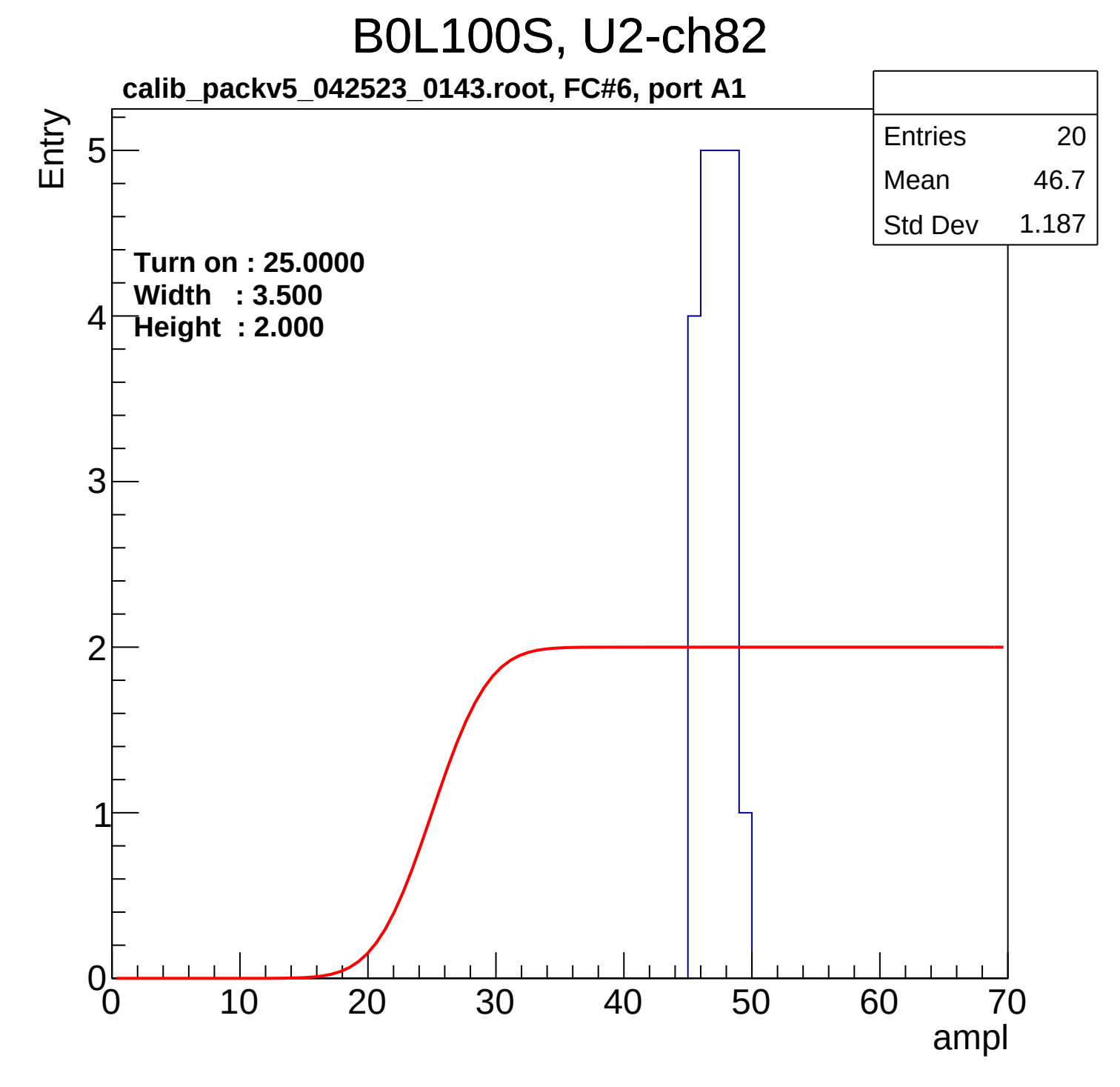
B0L100S, U2-ch82
calib_packv5_042523_0143.root, FC#6, port A1
Entries 20
Mean 46.7
Std Dev 1.187
Turn on : 25.0000
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
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0
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20
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40
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60
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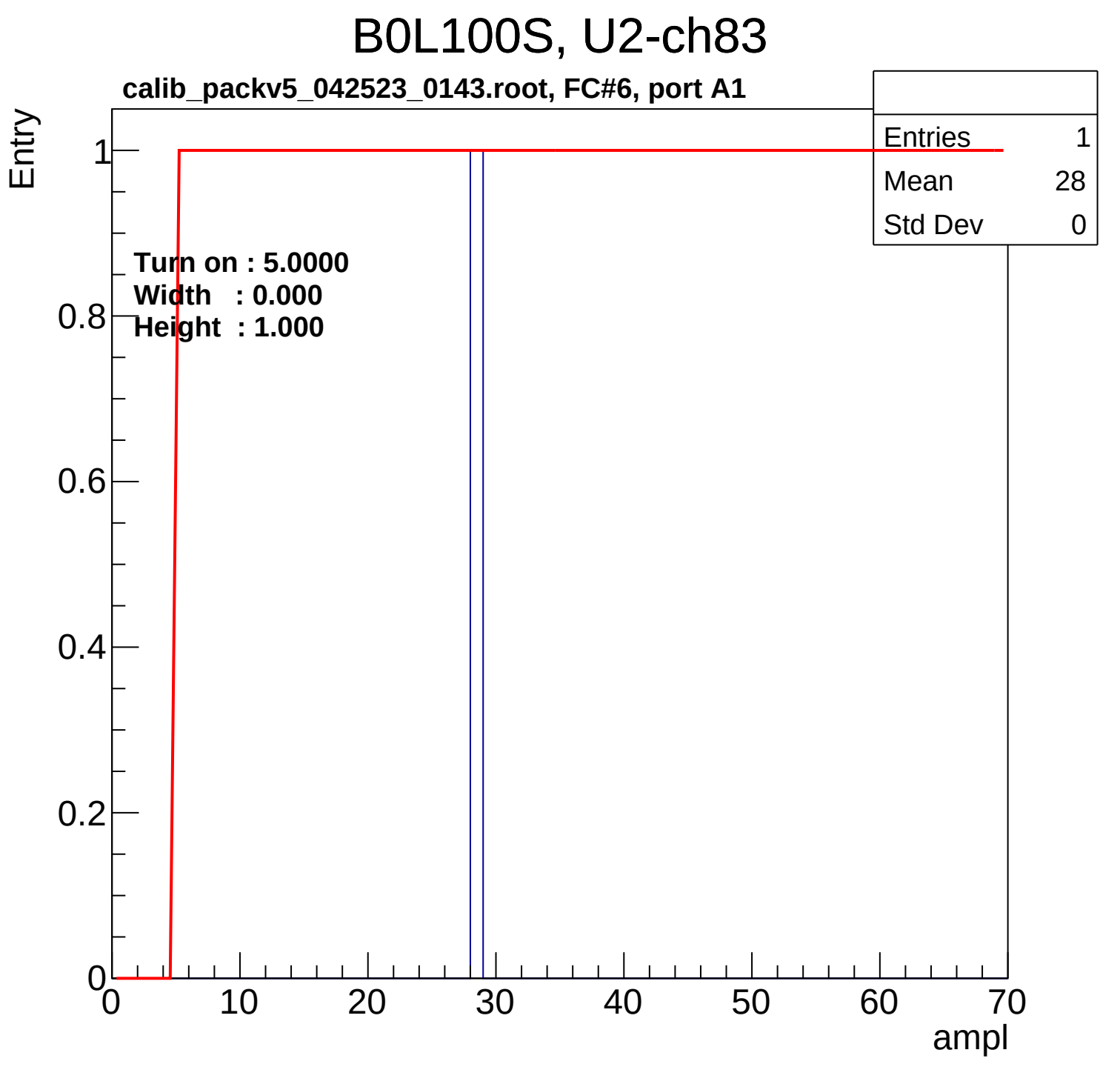
B0L100S, U2-ch83
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 28
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
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40
50
60
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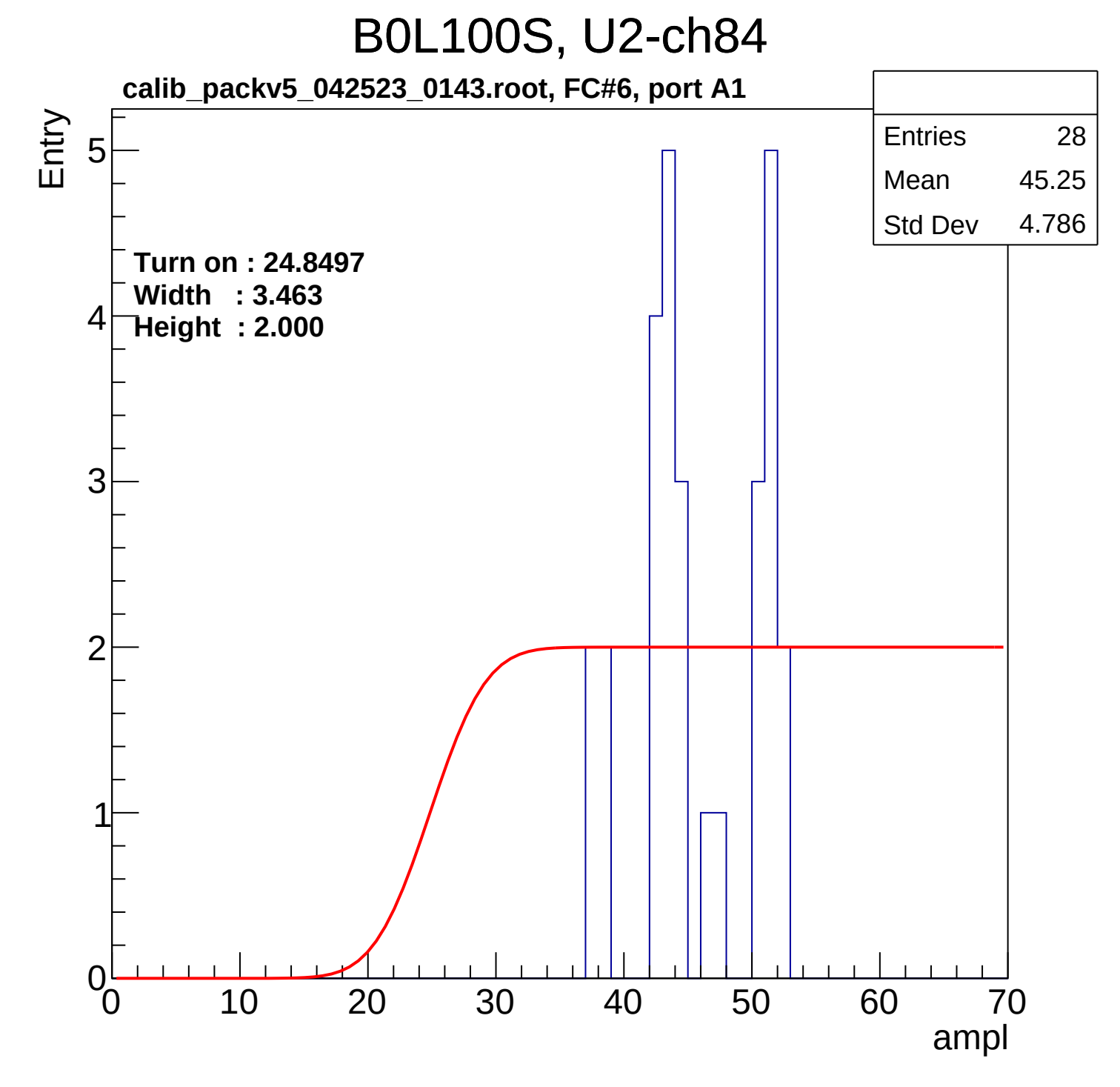
B0L100S, U2-ch84
calib_packv5_042523_0143.root, FC#6, port A1
Entries 28
Mean 45.25
Std Dev 4.786
Turn on : 24.8497
Width : 3.463
Height : 2.000
Entry
ampl
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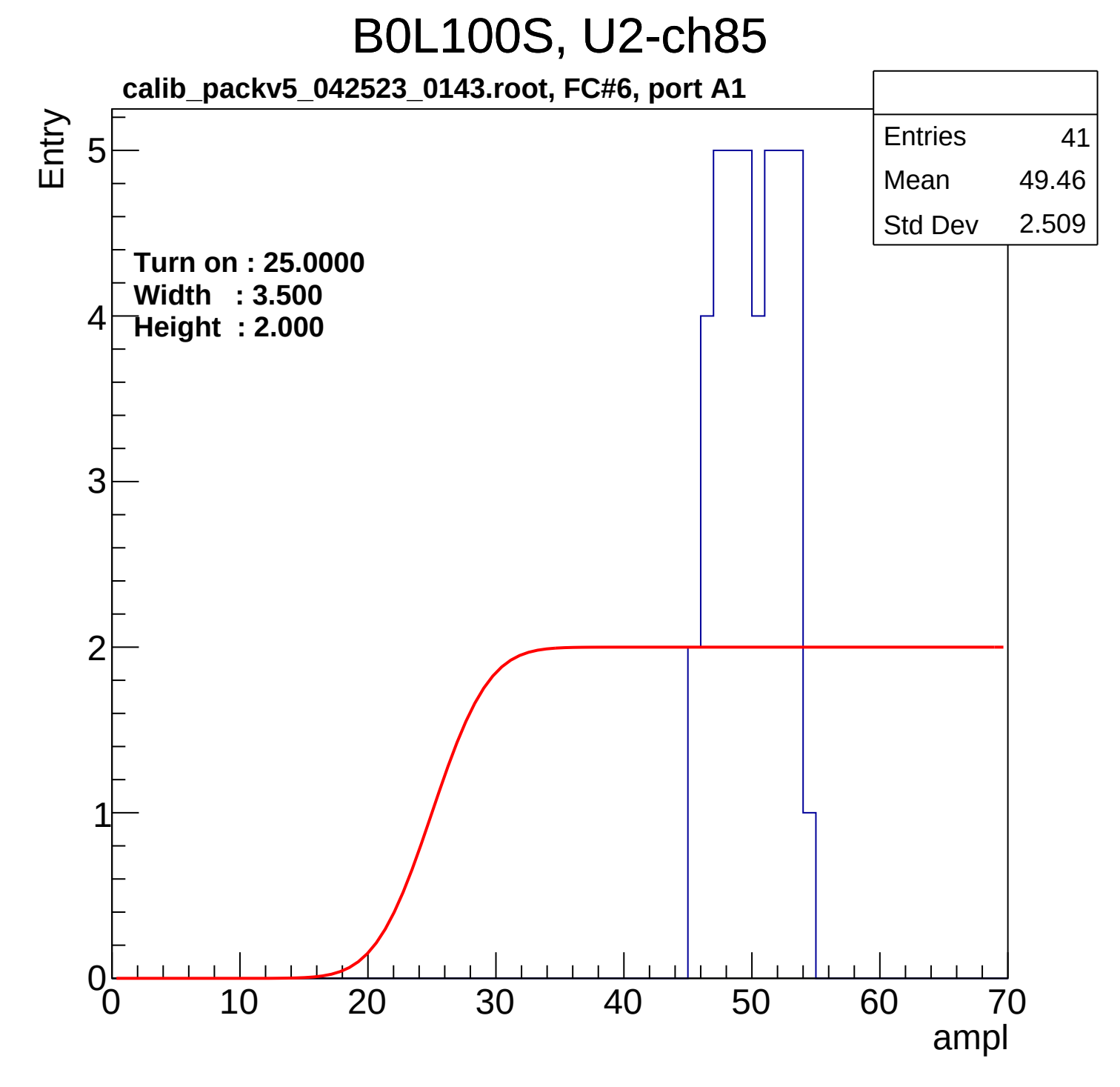
B0L100S, U2-ch85
calib_packv5_042523_0143.root, FC#6, port A1
Entries 41
Mean 49.46
Std Dev 2.509
Turn on : 25.0000
Width : 3.500
Height : 2.000
Entry
ampl
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4
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0
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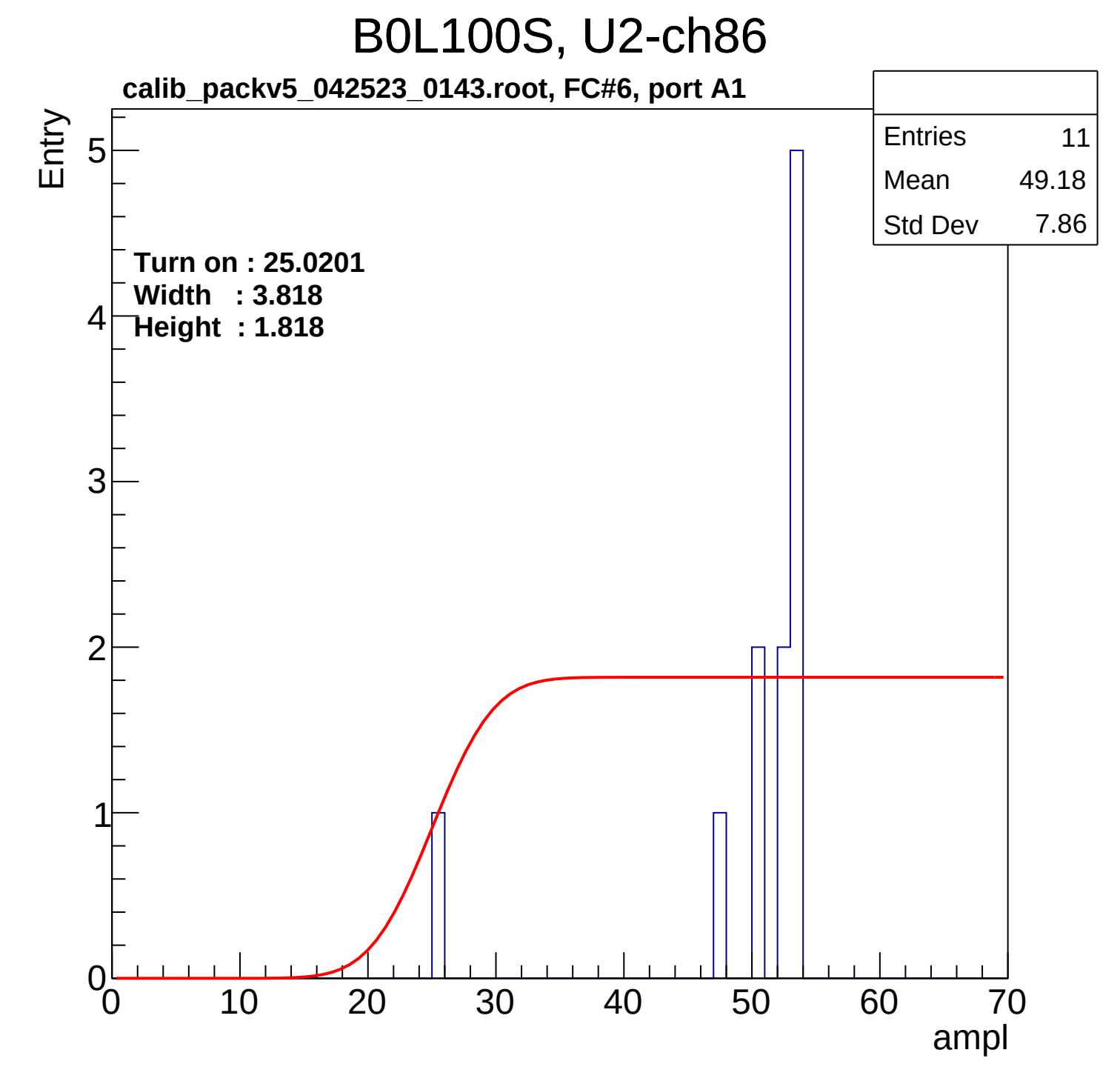
B0L100S, U2-ch86
calib_packv5_042523_0143.root, FC#6, port A1
Entries 11
Mean 49.18
Std Dev 7.86
Turn on : 25.0201
Width : 3.818
Height : 1.818
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
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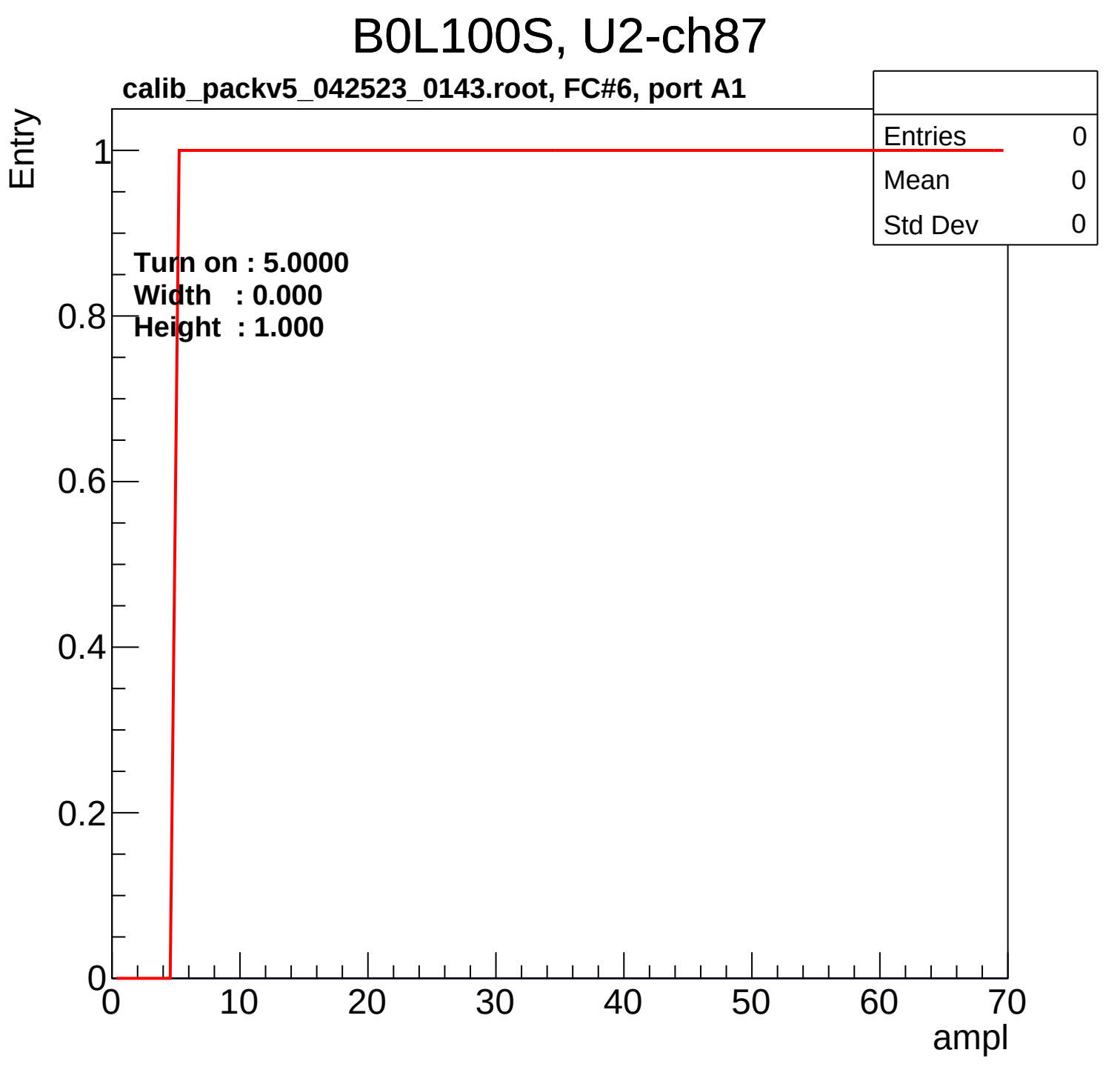
B0L100S, U2-ch87
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.2
0.4
0.6
0.8
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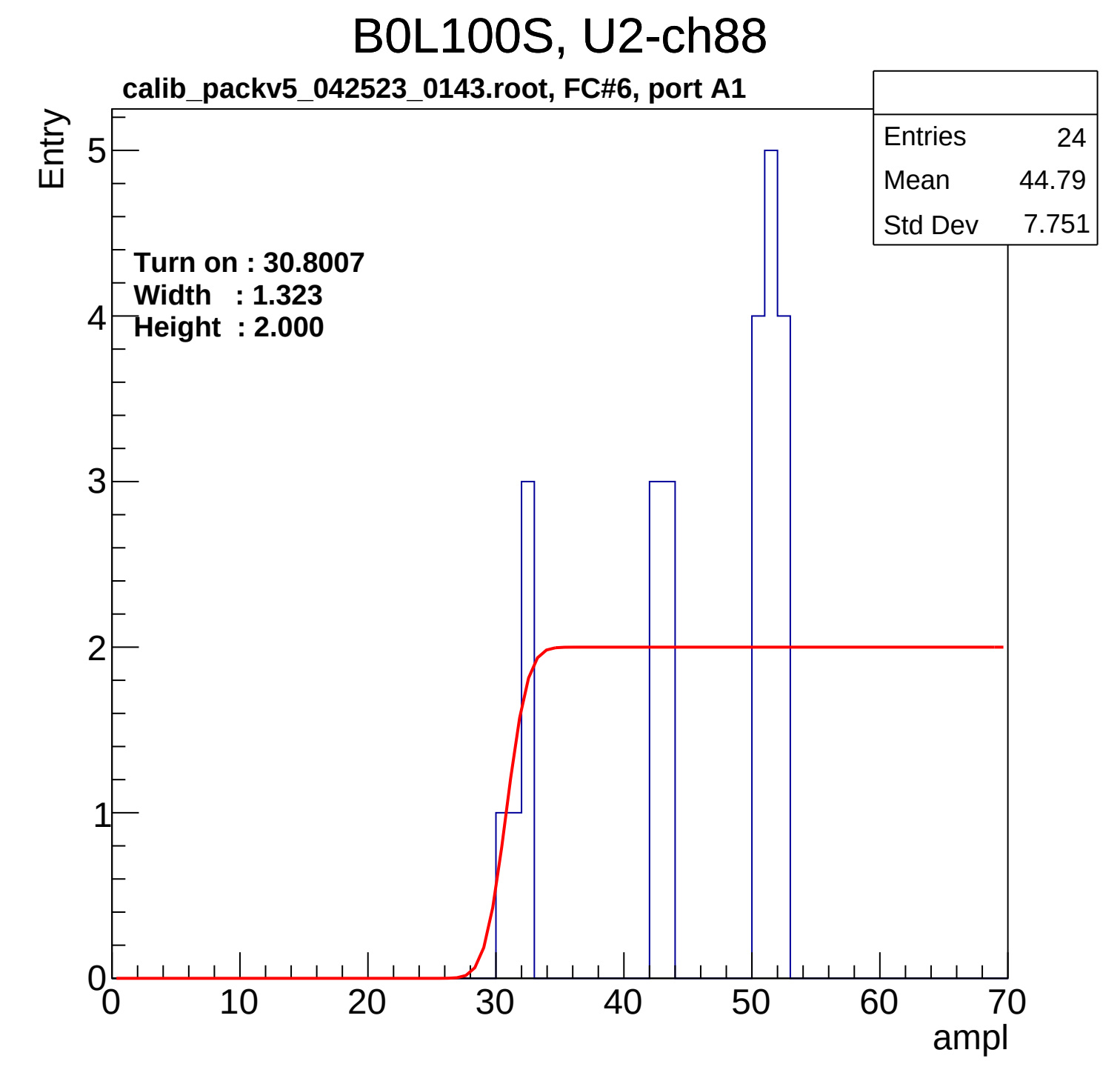
B0L100S, U2-ch88
calib_packv5_042523_0143.root, FC#6, port A1
Entries 24
Mean 44.79
Std Dev 7.751
Turn on : 30.8007
Width : 1.323
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
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60
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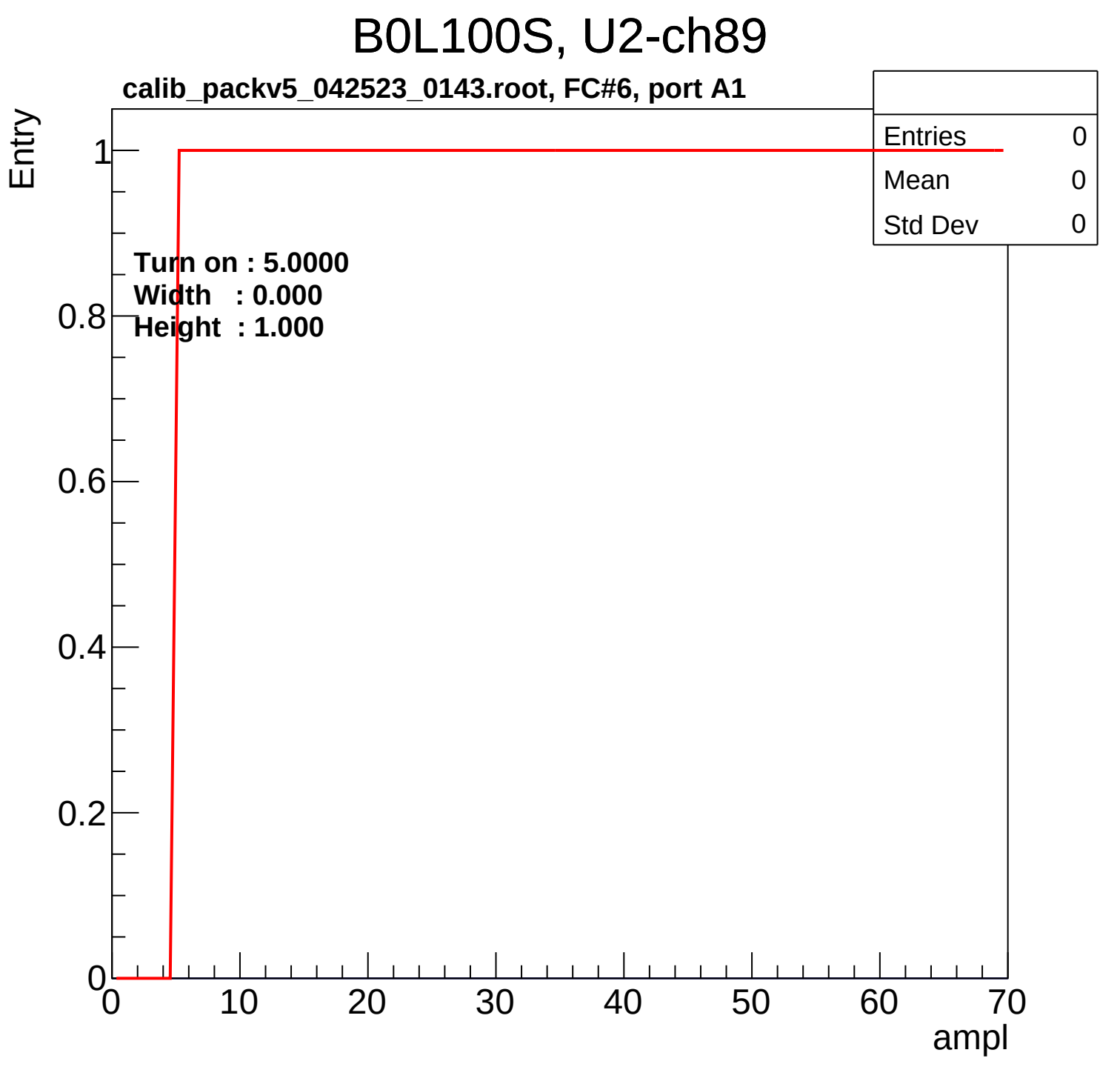
B0L100S, U2-ch89
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
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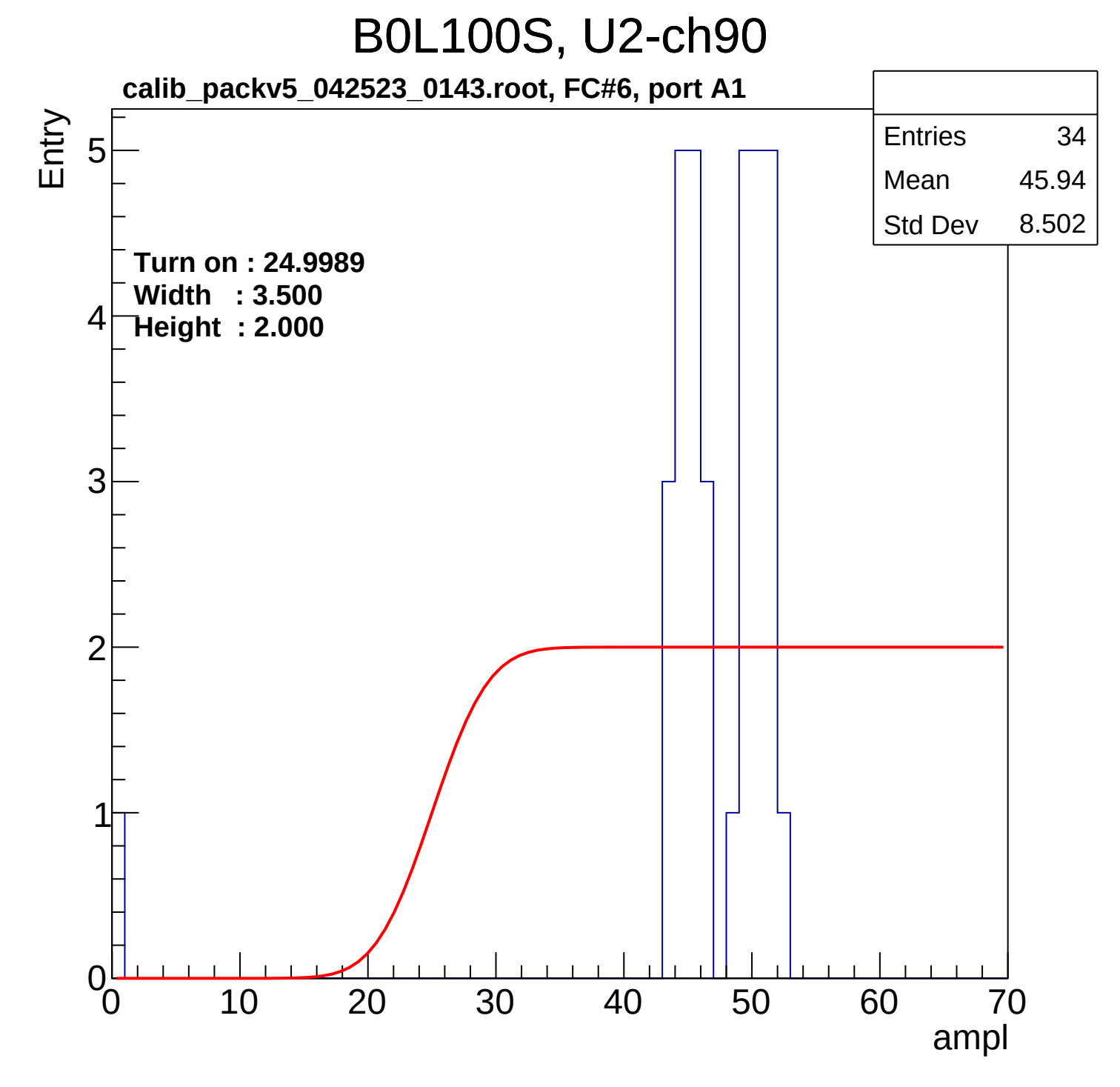
70
ampl


B0L100S, U2-ch90
calib_packv5_042523_0143.root, FC#6, port A1
Entries 34
Mean 45.94
Std Dev 8.502
Turn on : 24.9989
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
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20
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40
50
60
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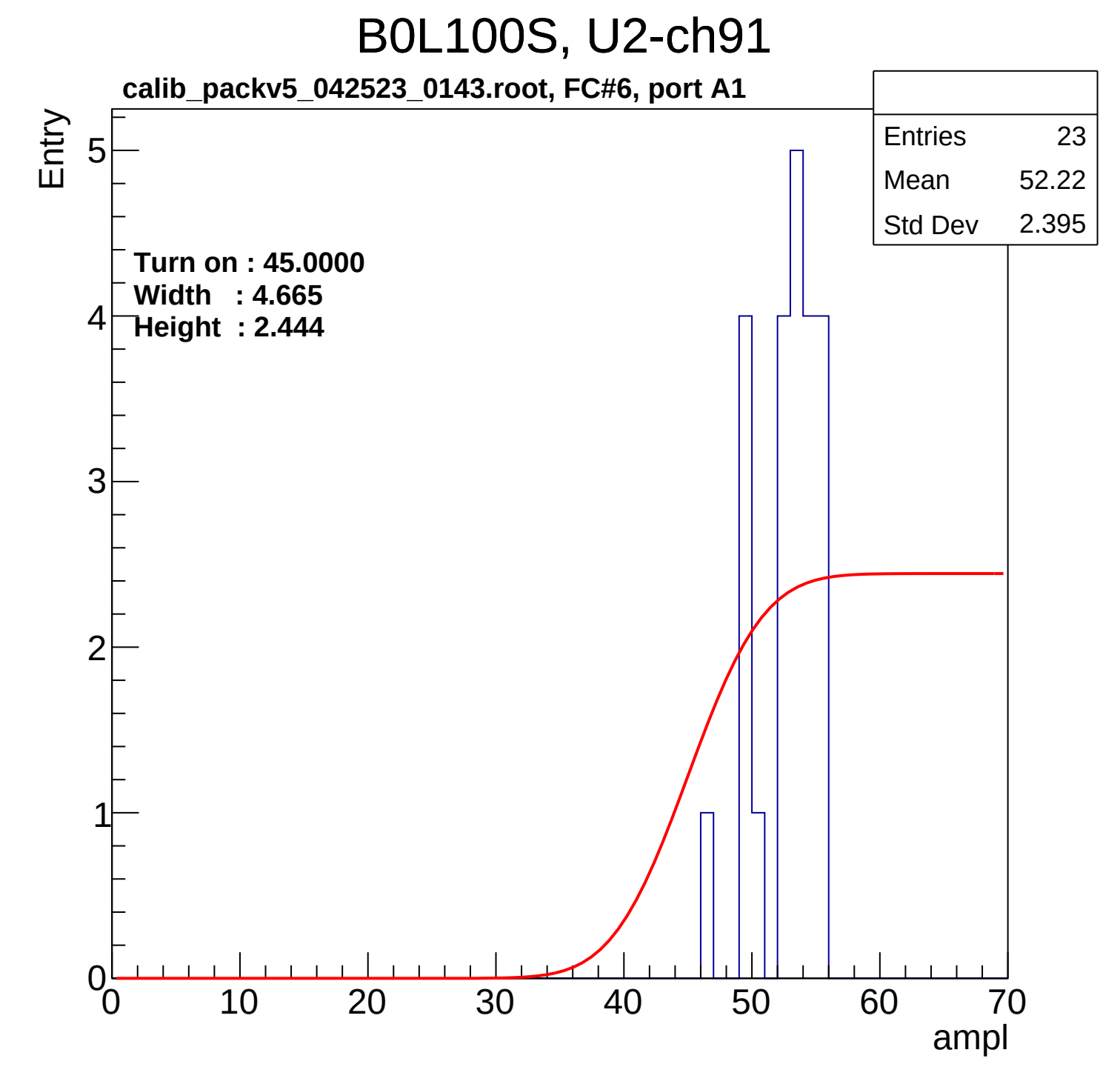
B0L100S, U2-ch91
calib_packv5_042523_0143.root, FC#6, port A1
Entries 23
Mean 52.22
Std Dev 2.395
Turn on : 45.0000
Width : 4.665
Height : 2.444
Entry
ampl
0
1
2
3
4
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0
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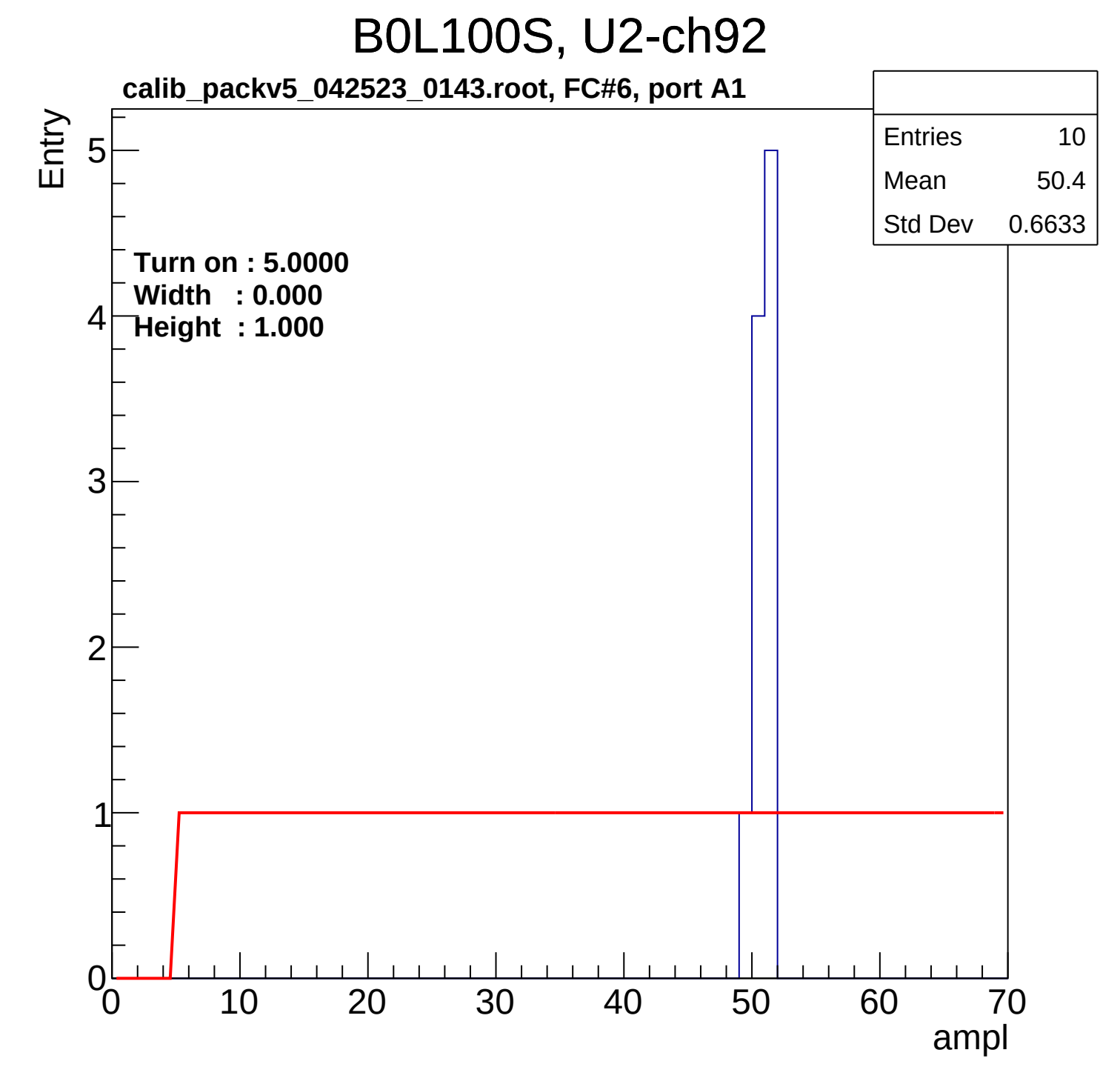
B0L100S, U2-ch92
calib_packv5_042523_0143.root, FC#6, port A1
Entries 10
Mean 50.4
Std Dev 0.6633
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
1
2
3
4
5
0
10
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30
40
50
60
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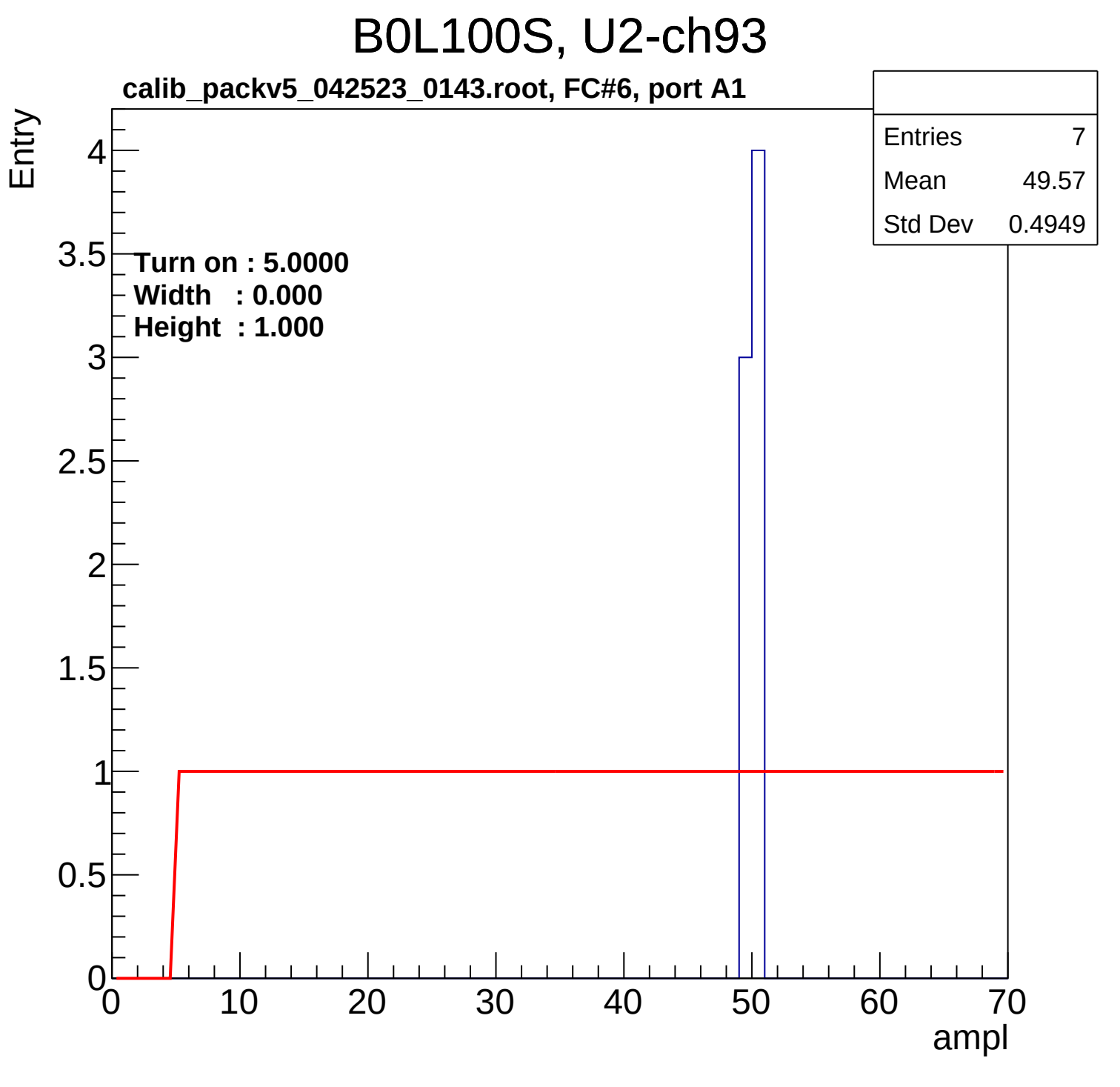
B0L100S, U2-ch93
calib_packv5_042523_0143.root, FC#6, port A1
Entries 7
Mean 49.57
Std Dev 0.4949
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
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40
50
60
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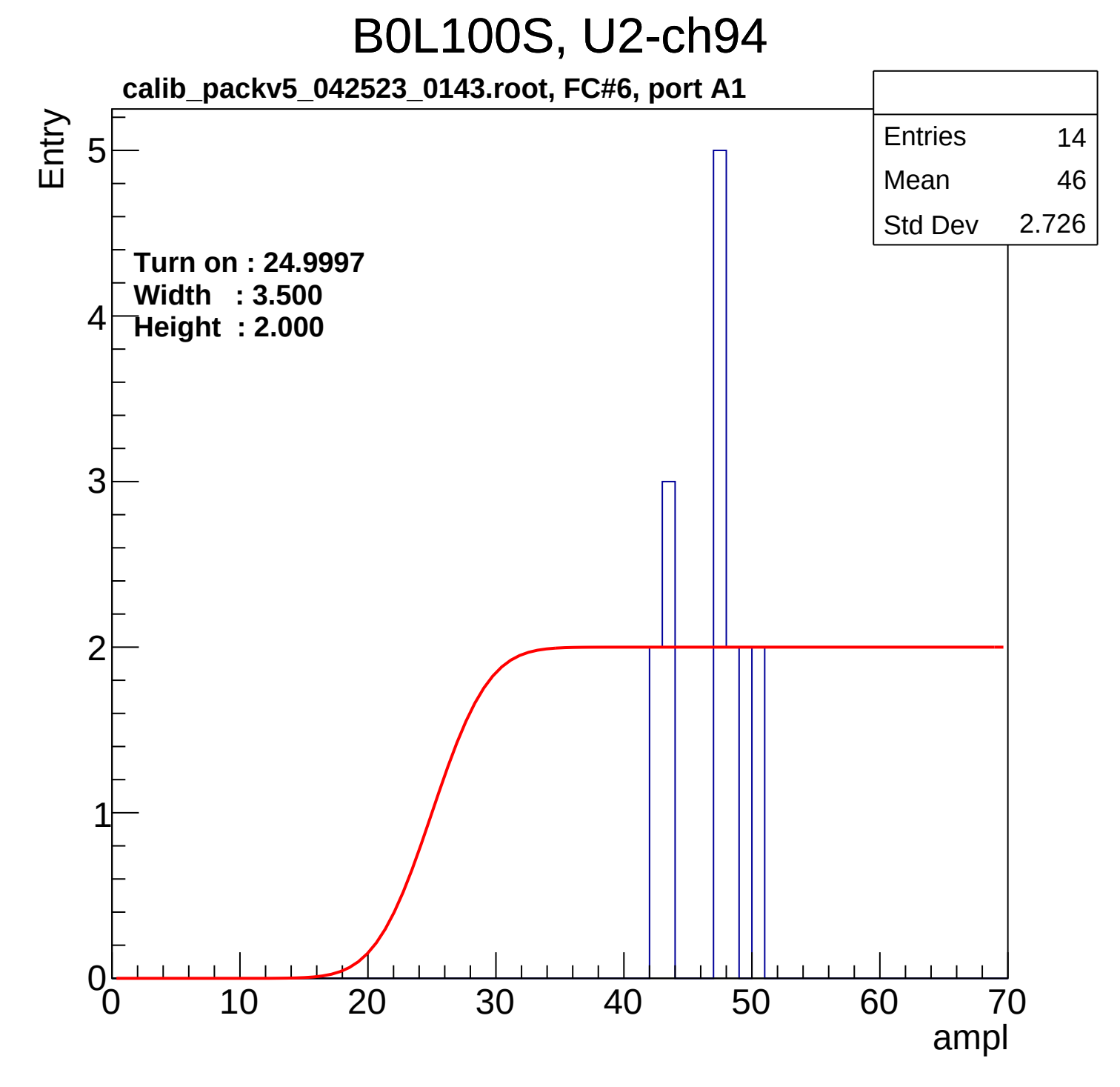
B0L100S, U2-ch94
calib_packv5_042523_0143.root, FC#6, port A1
Entries 14
Mean 46
Std Dev 2.726
Turn on : 24.9997
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
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40
50
60
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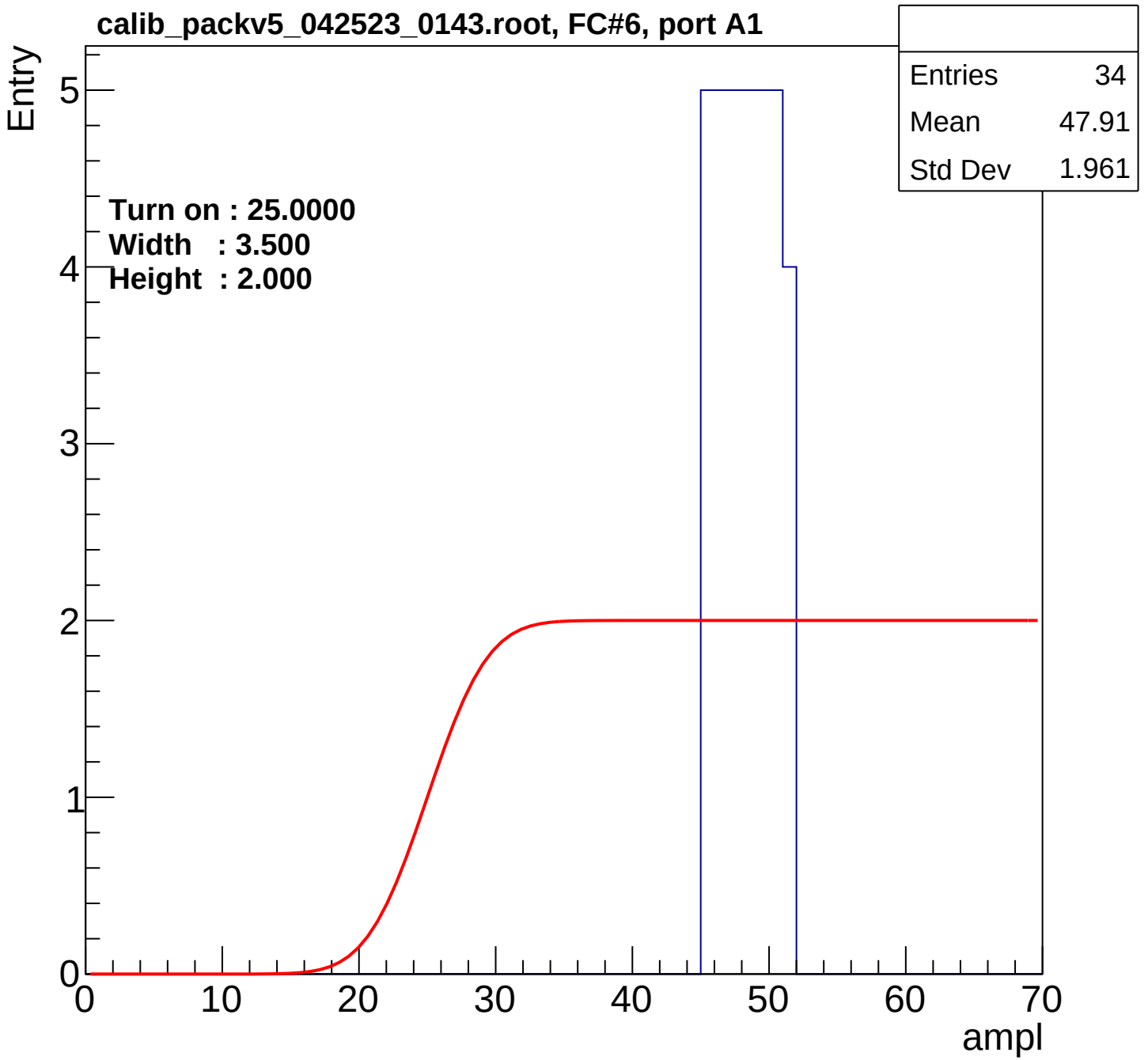
B0L100S, U2-ch95
calib_packv5_042523_0143.root, FC#6, port A1
Entries 34
Mean 47.91
Std Dev 1.961
Turn on : 25.0000
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
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40
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60
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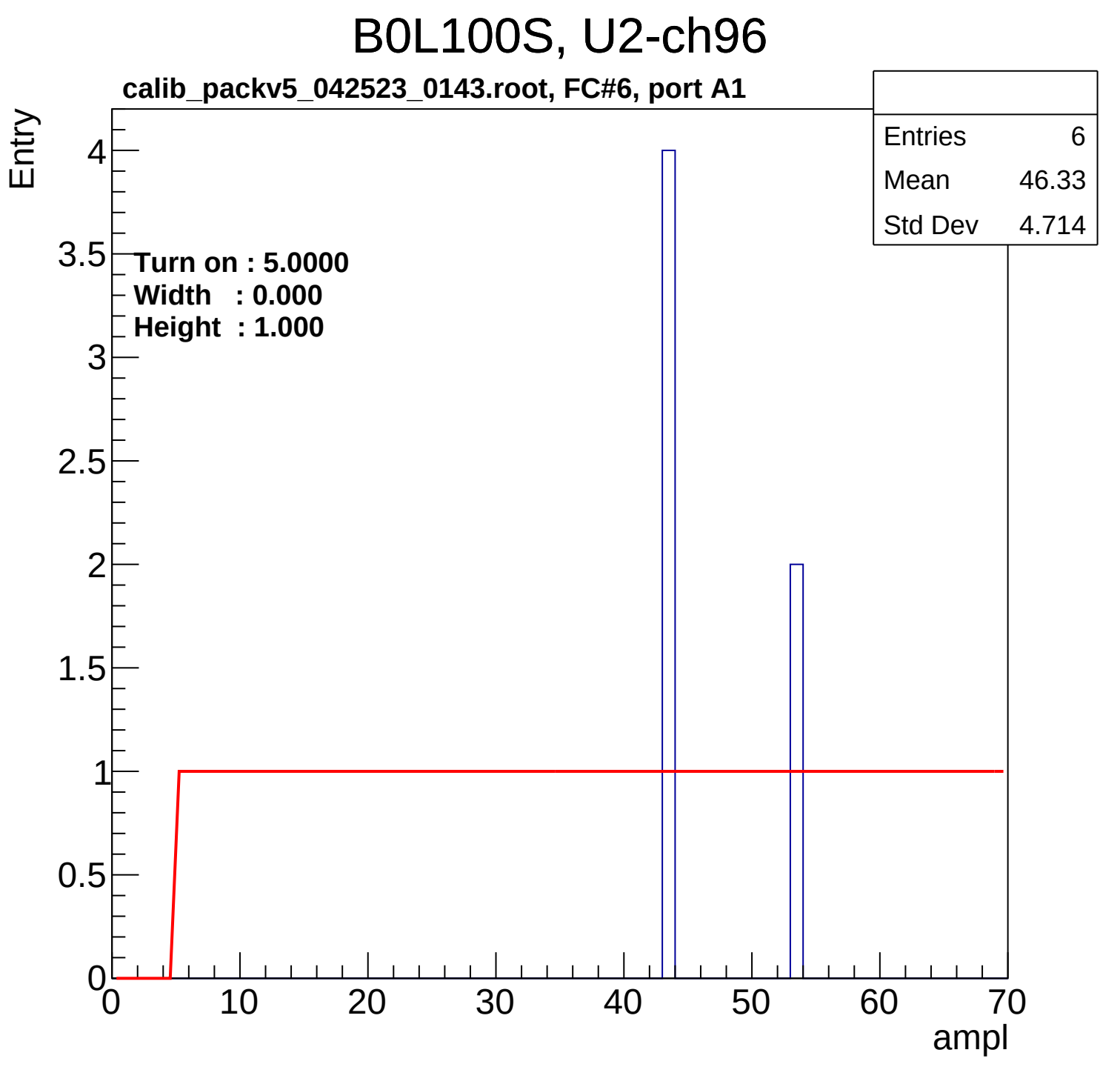
B0L100S, U2-ch96
calib_packv5_042523_0143.root, FC#6, port A1
Entries 6
Mean 46.33
Std Dev 4.714
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
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40
50
60
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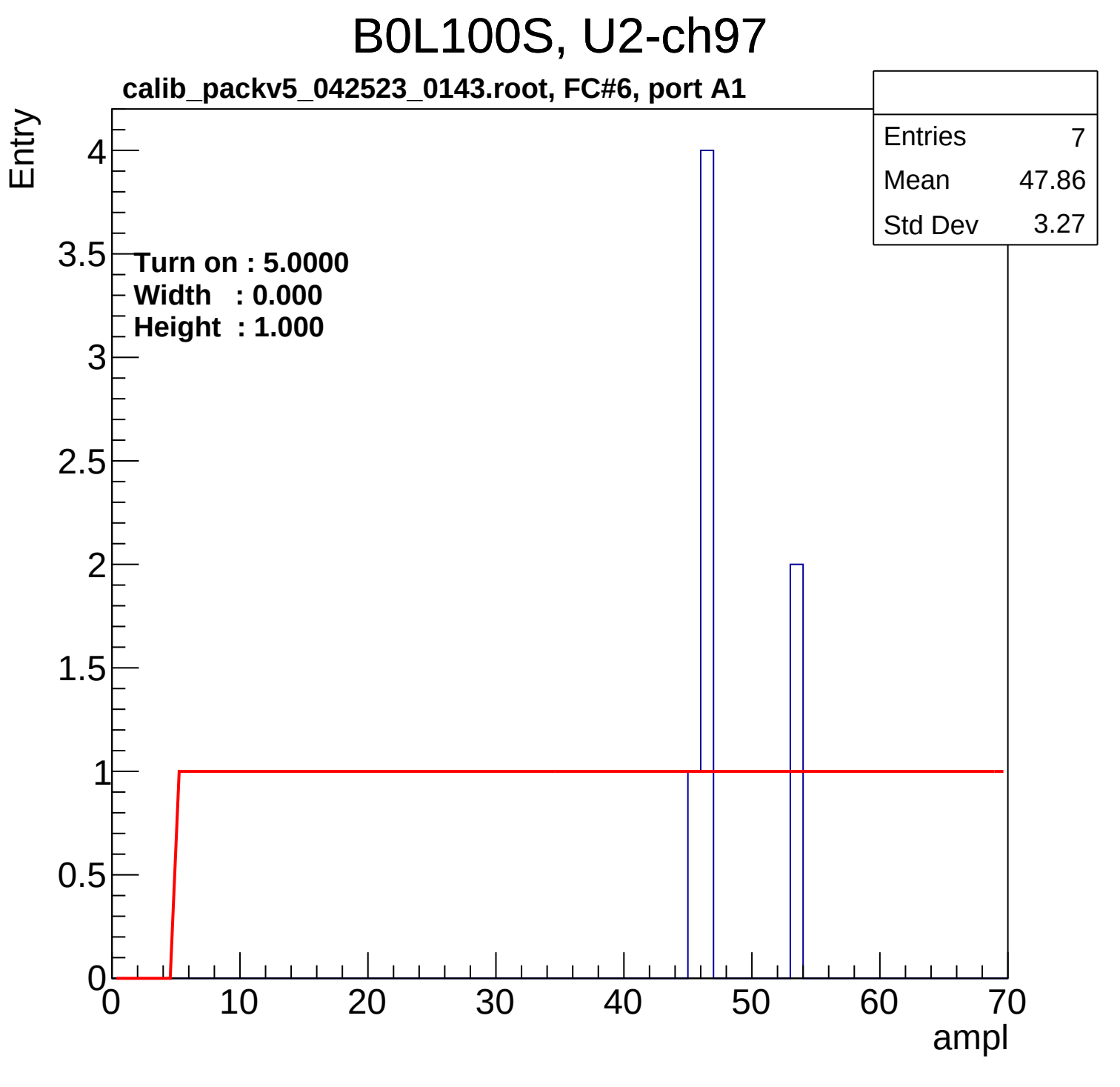
B0L100S, U2-ch97
calib_packv5_042523_0143.root, FC#6, port A1
Entries 7
Mean 47.86
Std Dev 3.27
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.5
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1.5
2
2.5
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3.5
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0
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60
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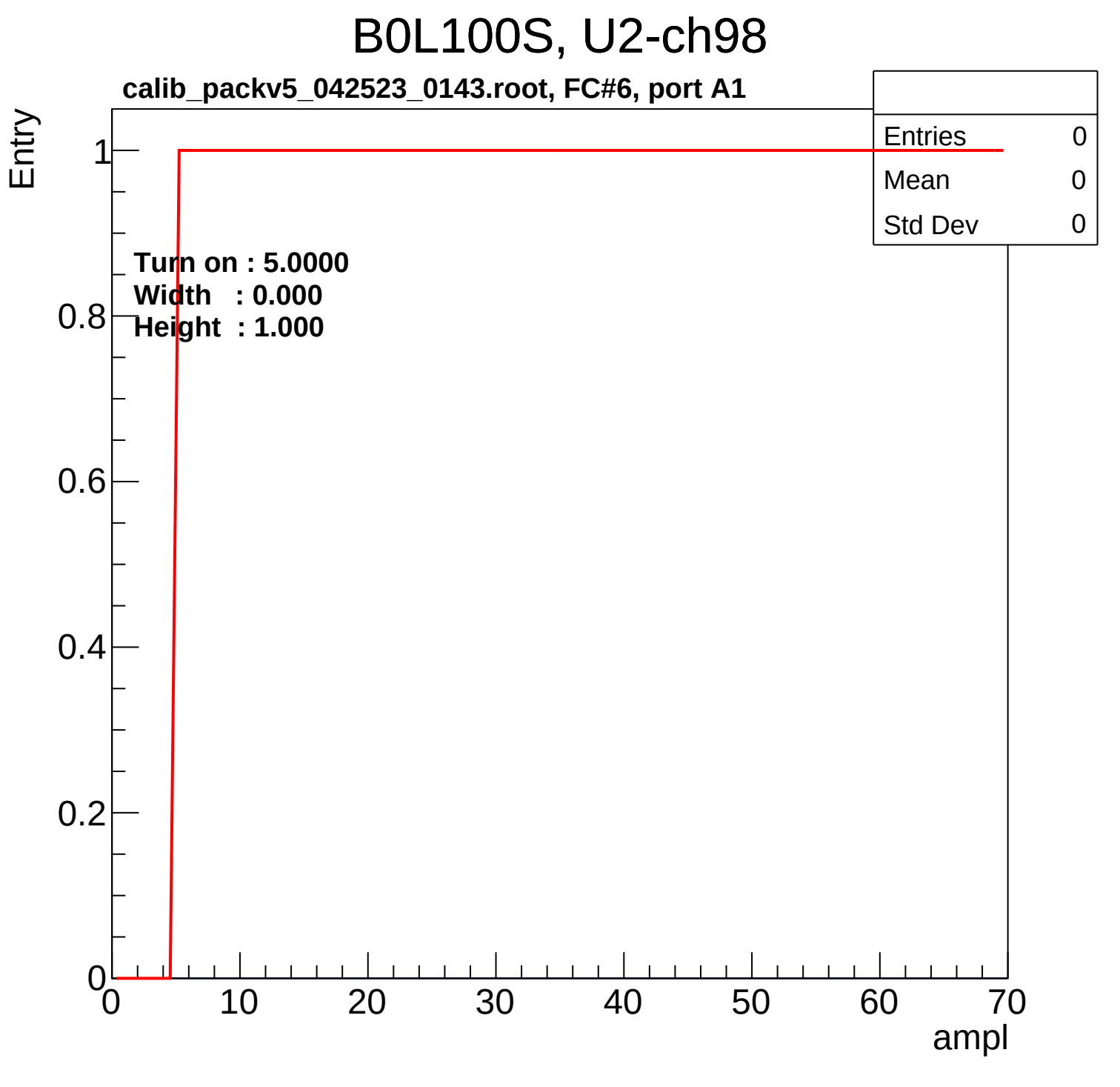
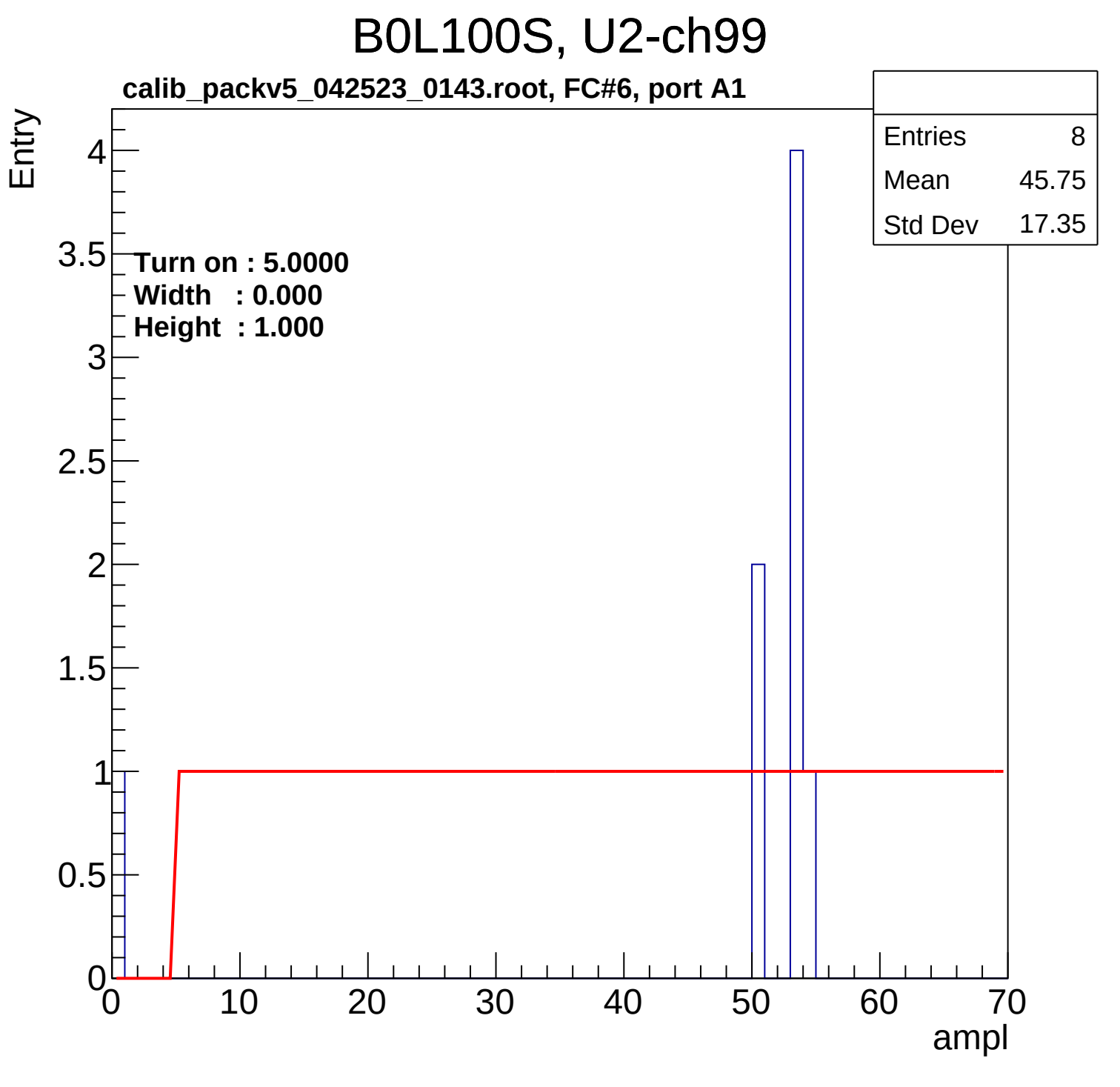

B0L100S, U2-ch98
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B0L100S, U2-ch99
calib_packv5_042523_0143.root, FC#6, port A1
Entries 8
Mean 45.75
Std Dev 17.35
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
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20
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60
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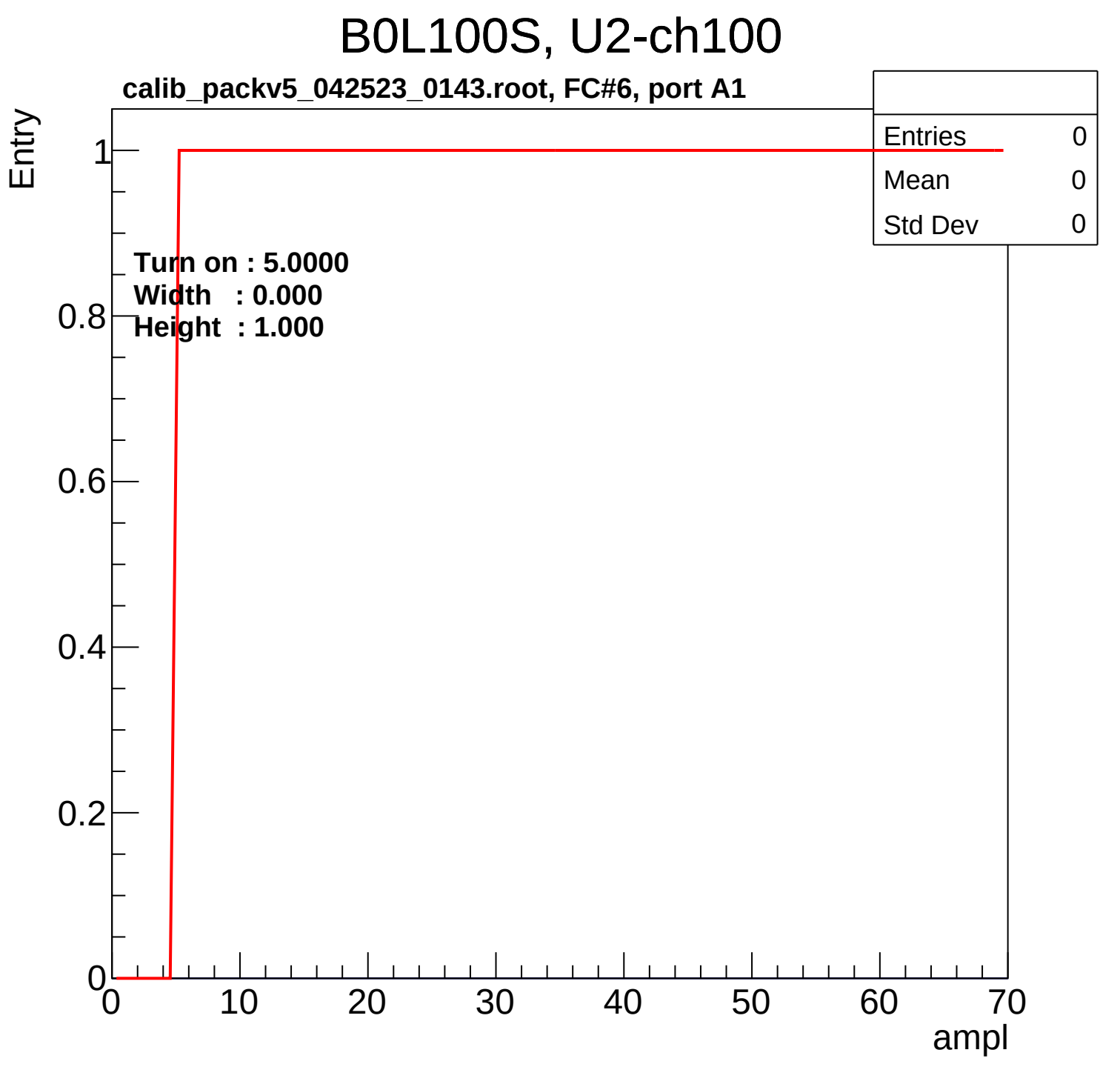
B0L100S, U2-ch100
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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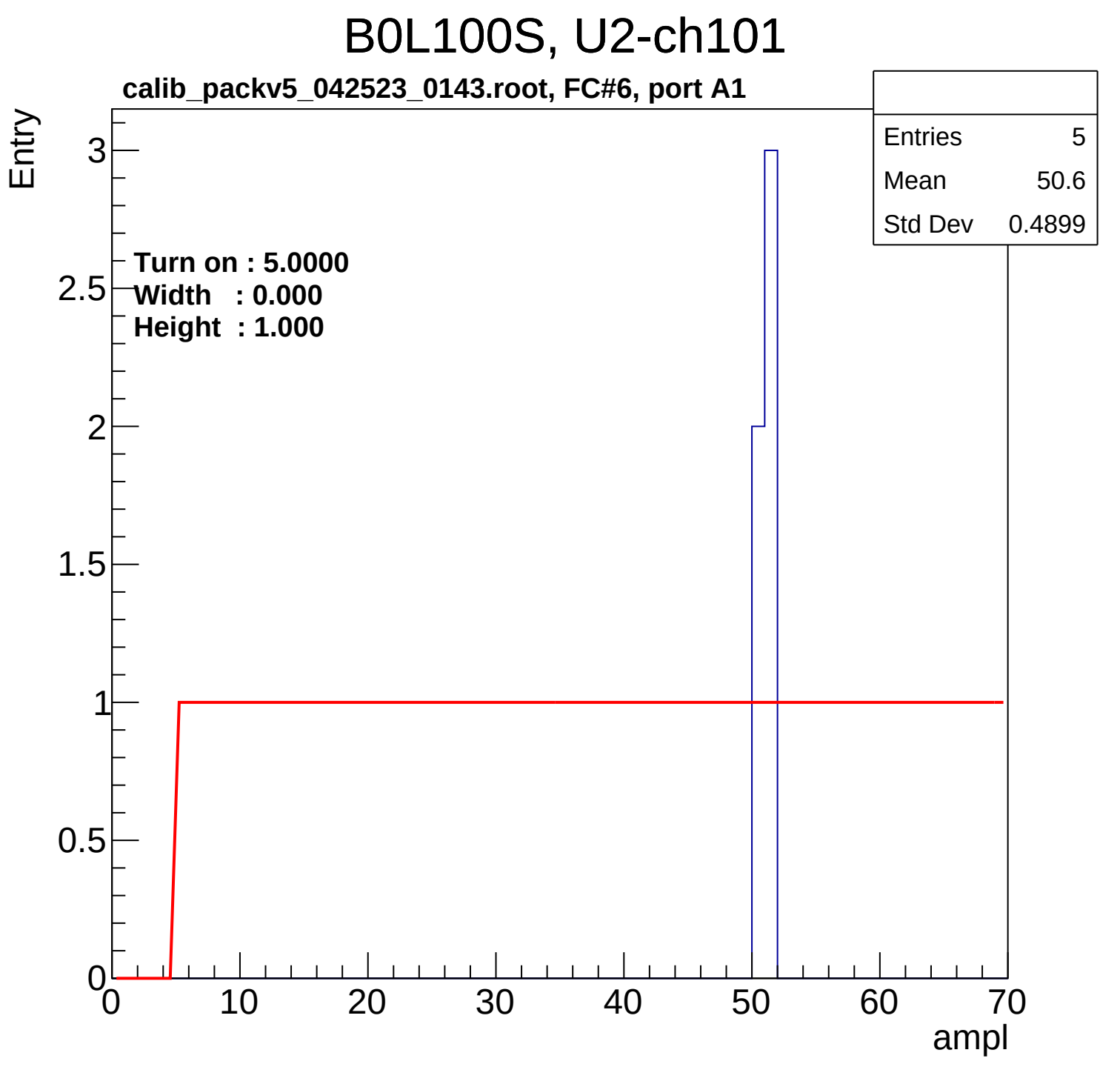
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U2-ch101
calib_packv5_042523_0143.root, FC#6, port A1
Entries 5
Mean 50.6
Std Dev 0.4899
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
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20
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40
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60
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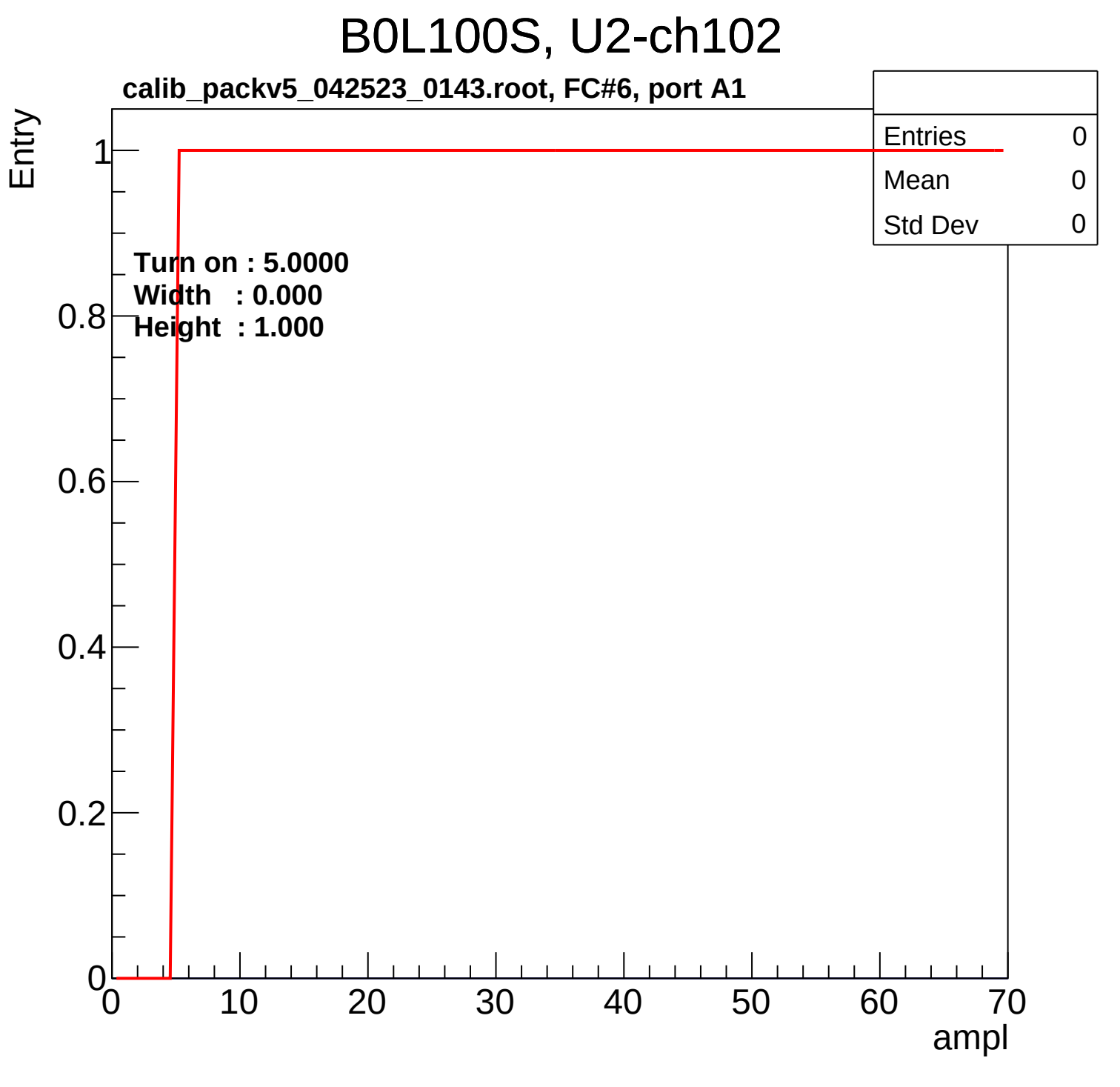
B0L100S, U2-ch102
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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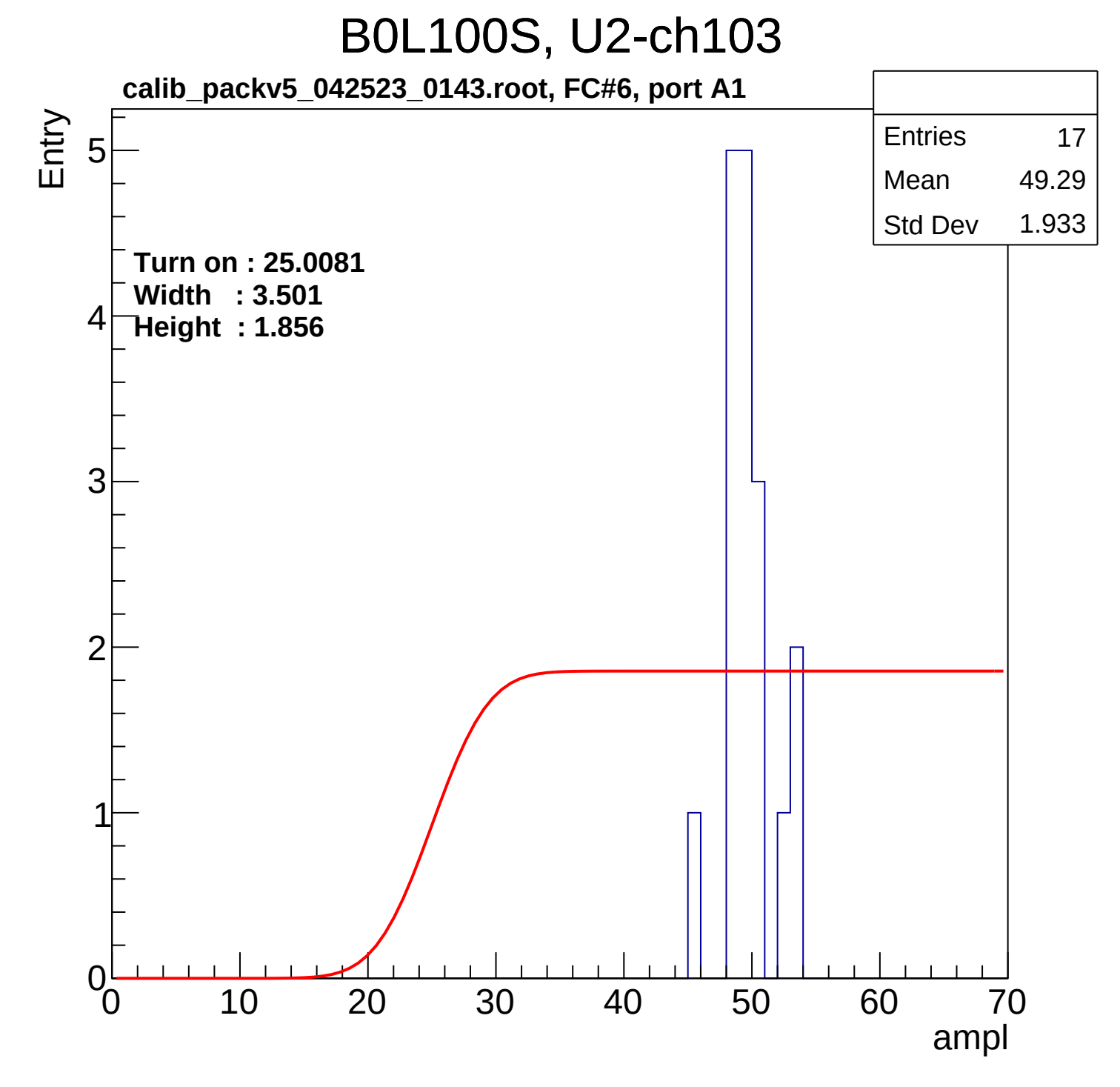
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U2-ch103
calib_packv5_042523_0143.root, FC#6, port A1
Entries 17
Mean 49.29
Std Dev 1.933
Turn on : 25.0081
Width : 3.501
Height : 1.856
Entry
ampl
0
1
2
3
4
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0
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20
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40
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60
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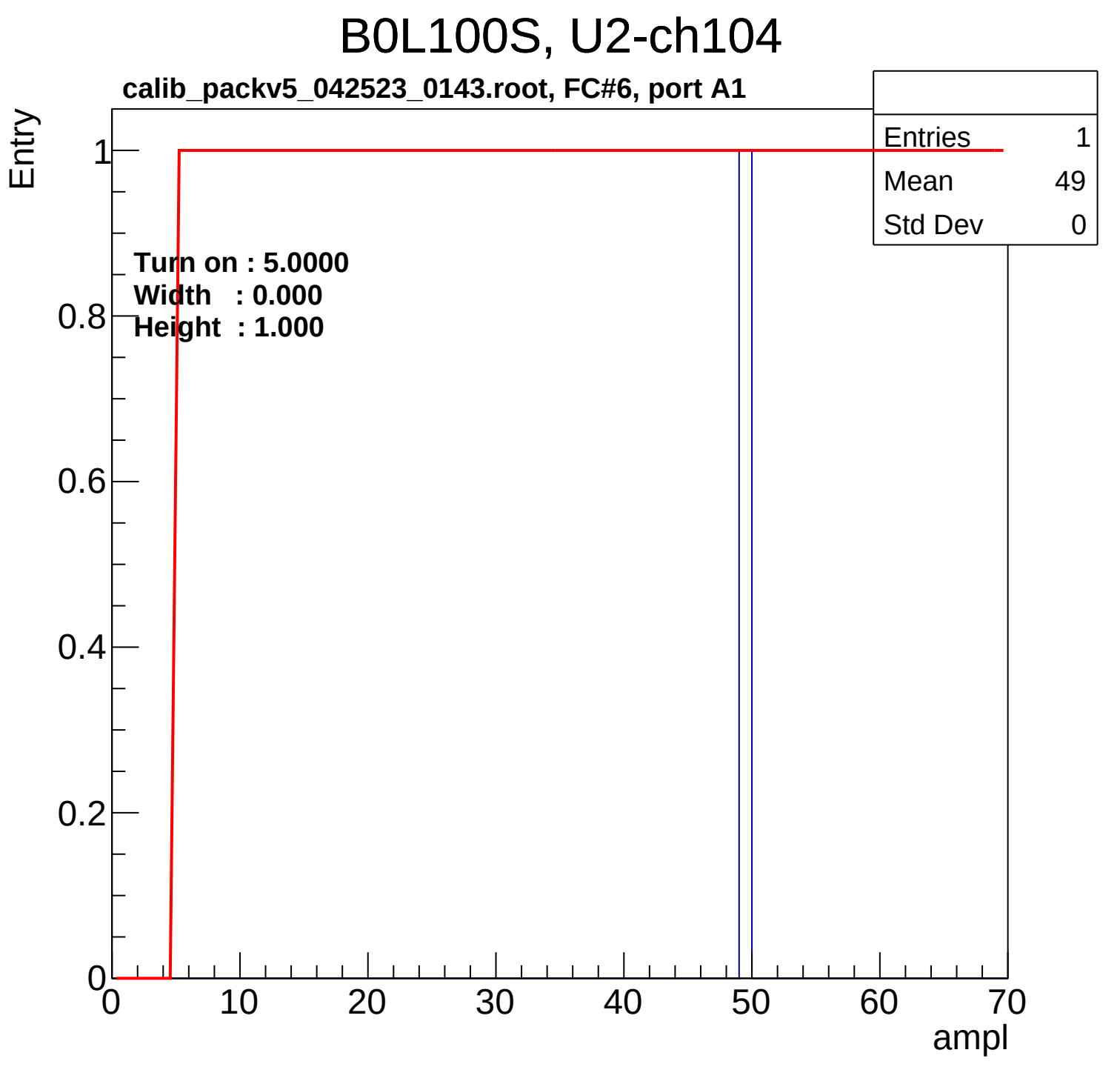
B0L100S, U2-ch104
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 49
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.2
0.4
0.6
0.8
1
0
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20
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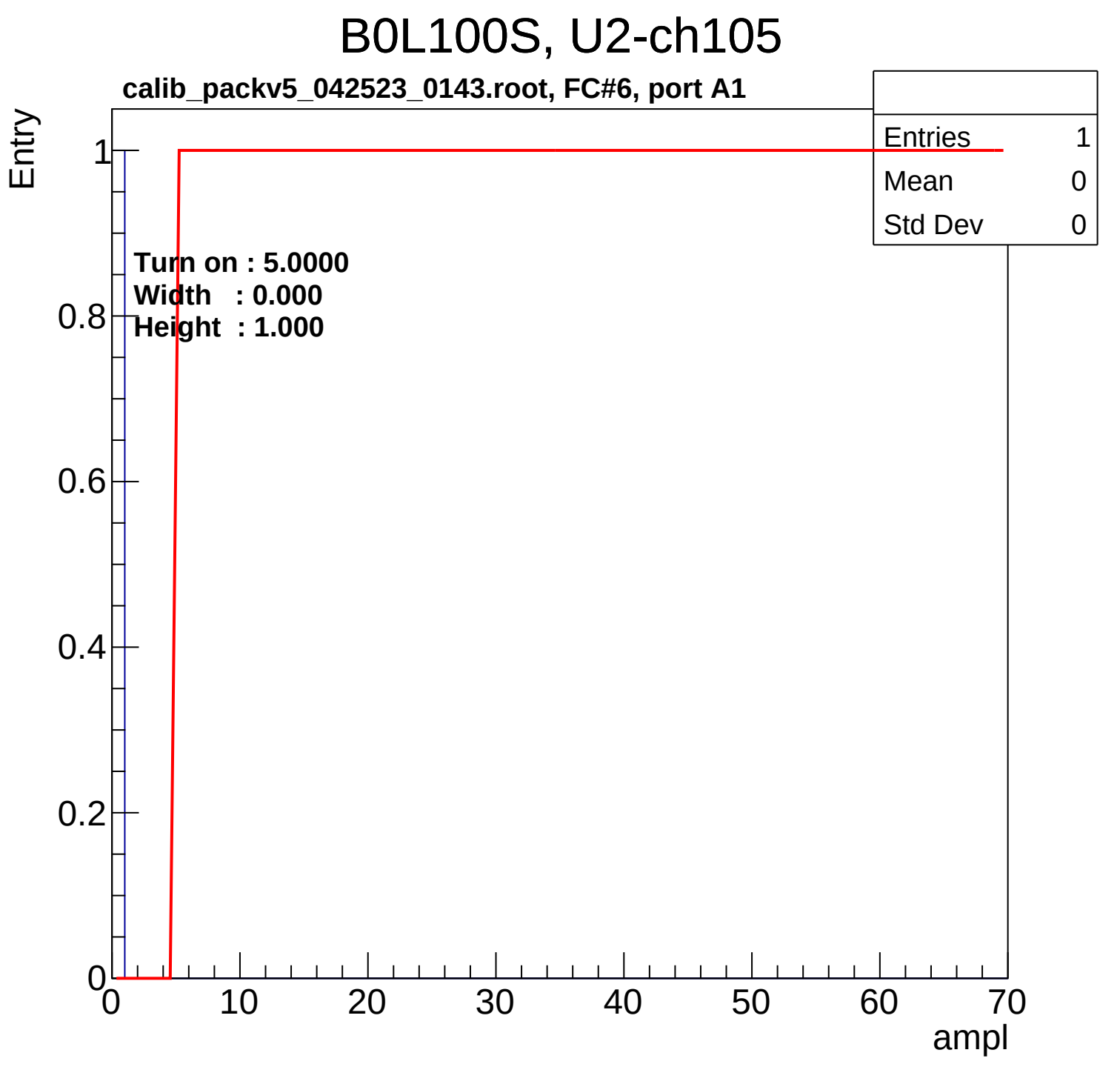
40
50
60
70


B0L100S, U2-ch105
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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0.8
0.6
0.4
0.2
0
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10
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30
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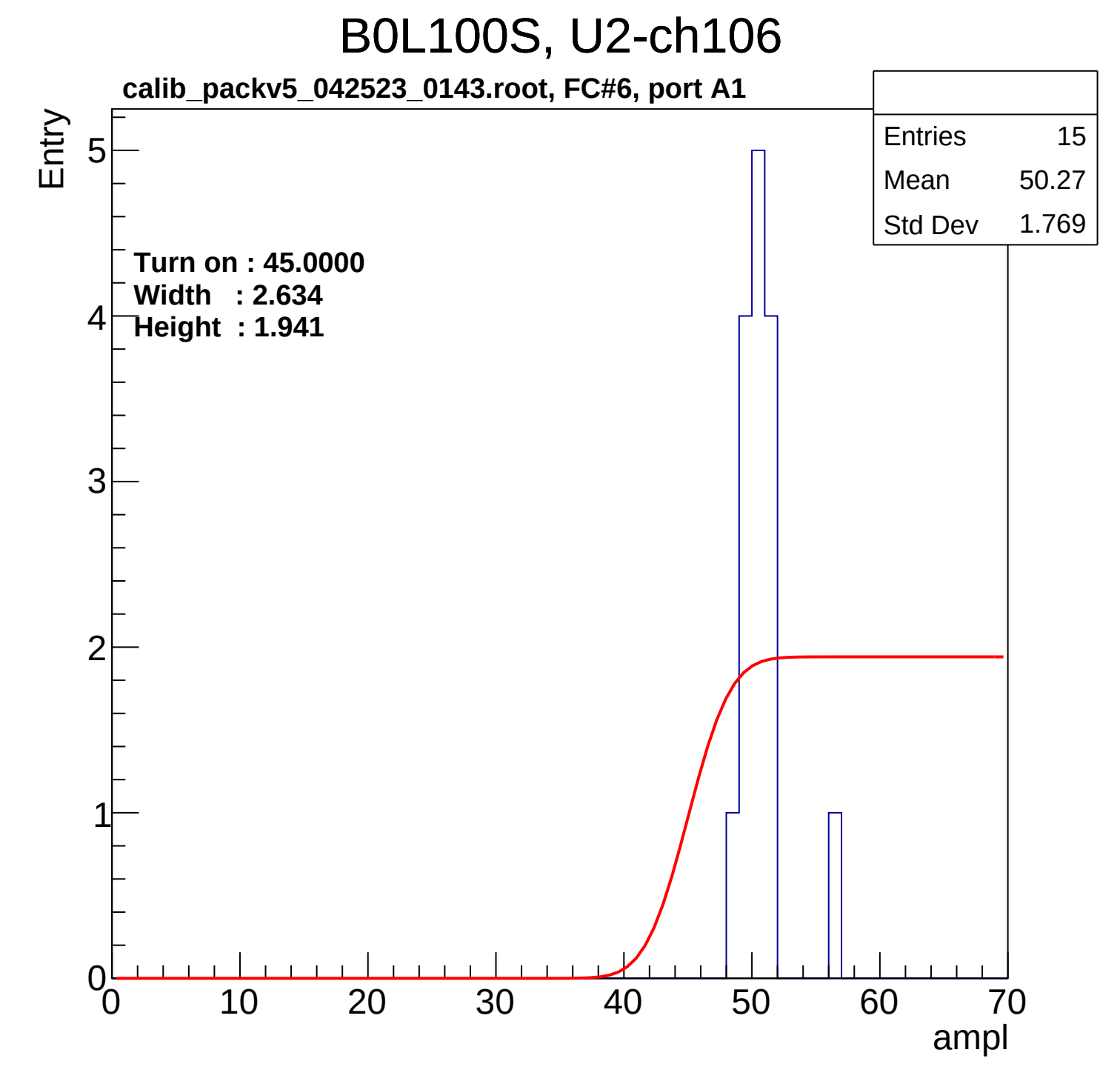
50
60
70
ampl


B0L100S, U2-ch106
calib_packv5_042523_0143.root, FC#6, port A1
Entries 15
Mean 50.27
Std Dev 1.769
Turn on : 45.0000
Width : 2.634
Height : 1.941
Entry
ampl
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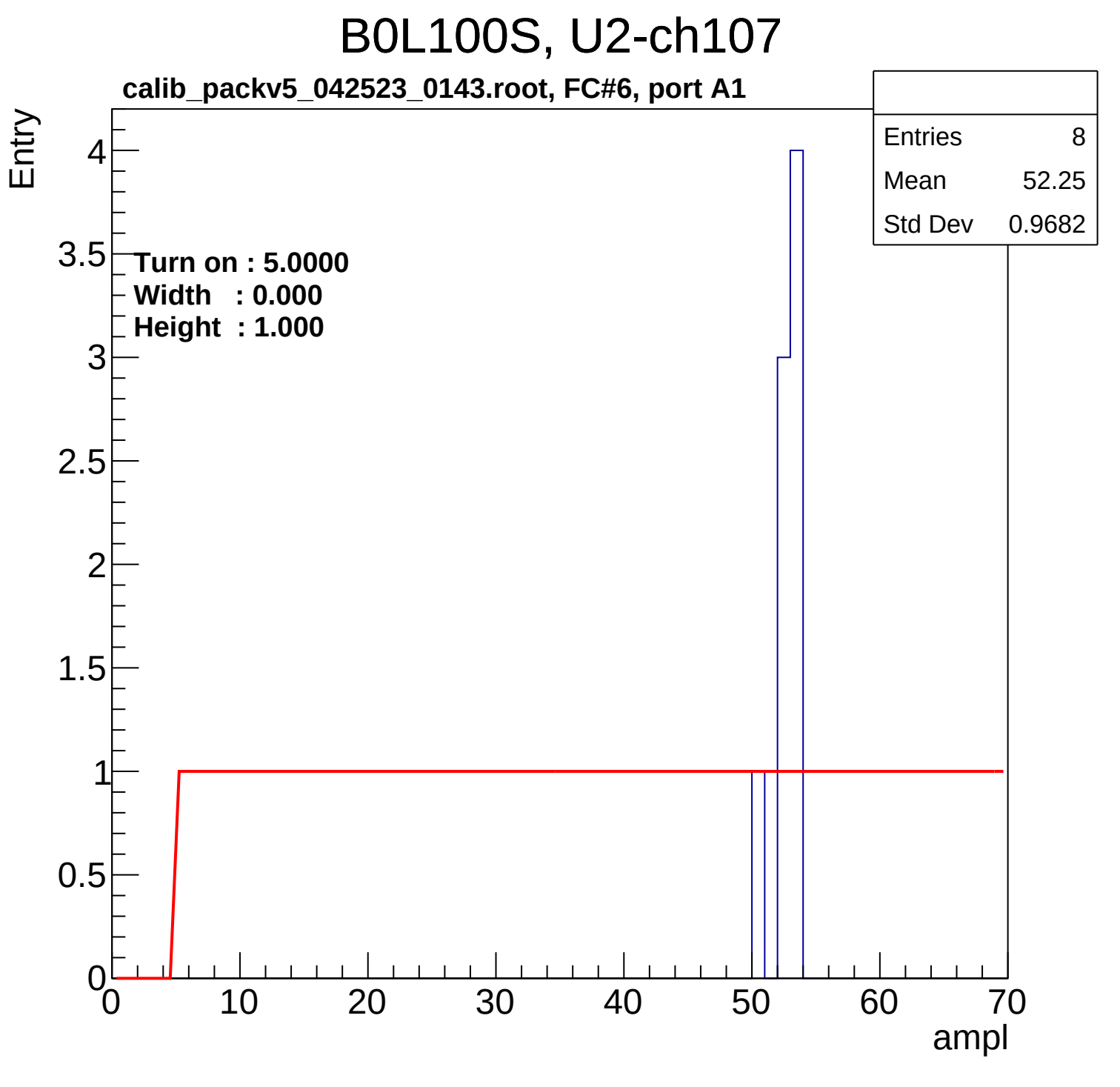
B0L100S, U2-ch107
calib_packv5_042523_0143.root, FC#6, port A1
Entries 8
Mean 52.25
Std Dev 0.9682
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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1.5
2
2.5
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3.5
4
0
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60
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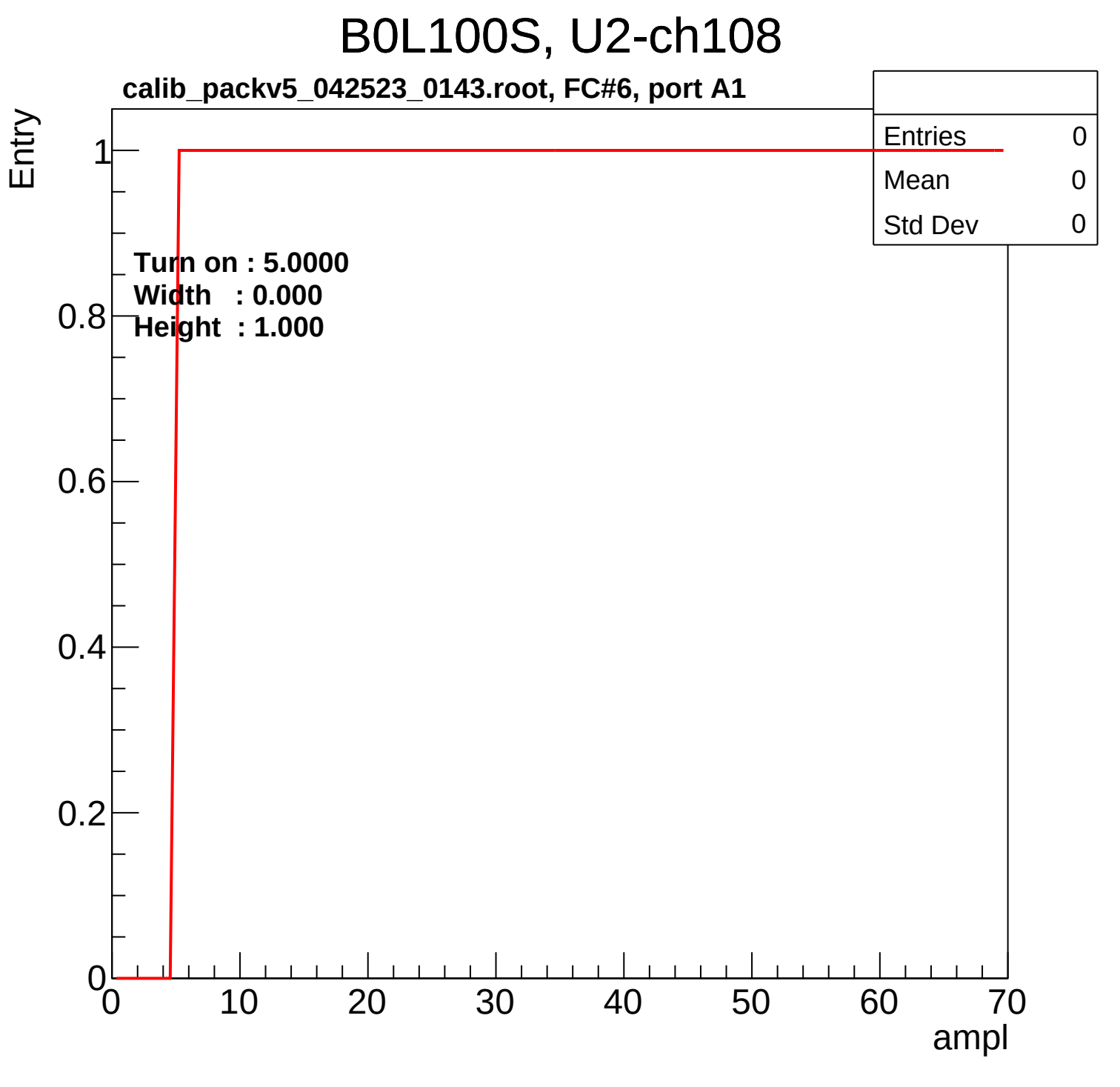
B0L100S, U2-ch108
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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0.8
0.6
0.4
0.2
0
0
10
20
30
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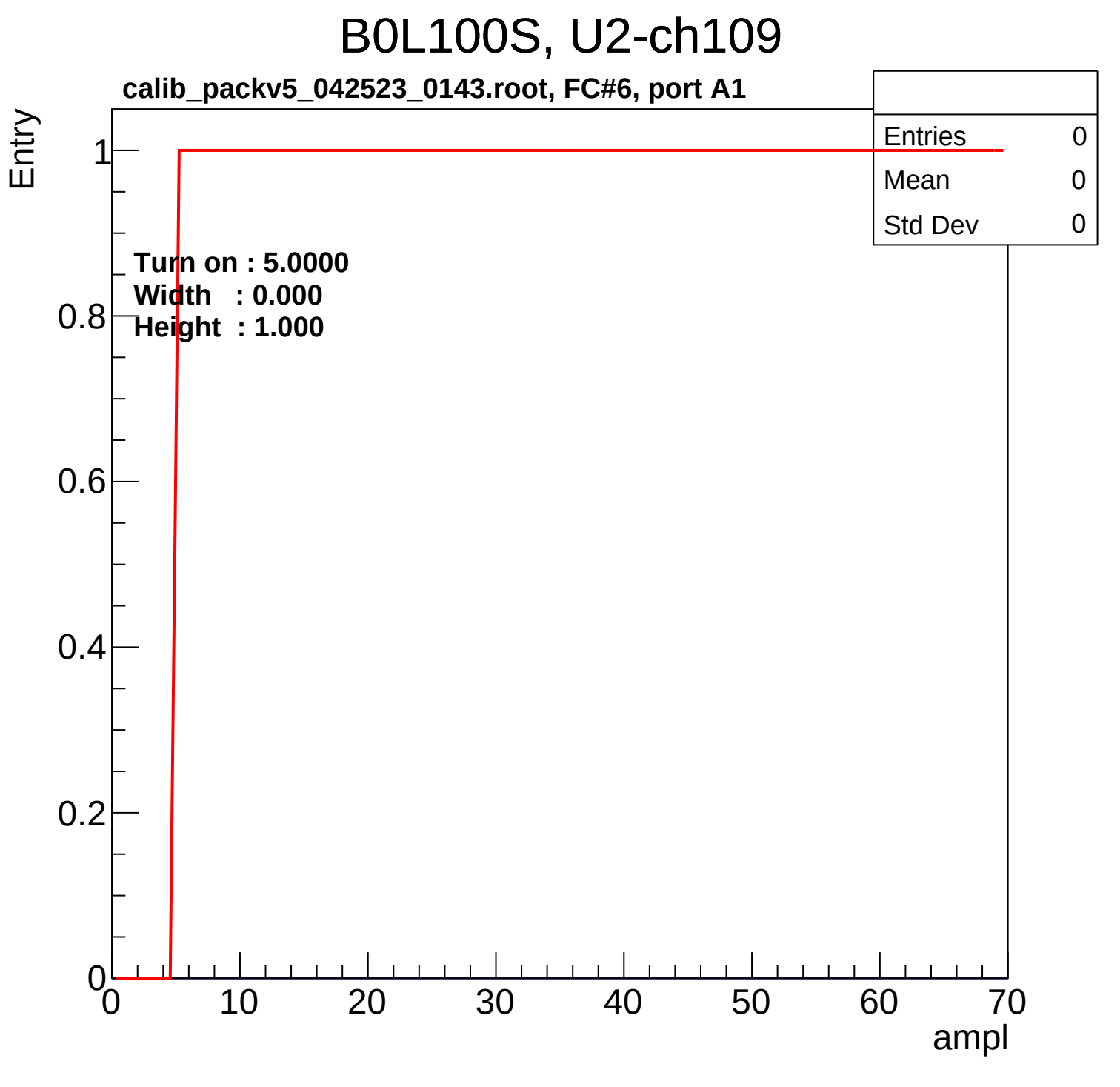
50
60
70
ampl


B0L100S, U2-ch109
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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0.8
0.6
0.4
0.2
0
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10
20
30
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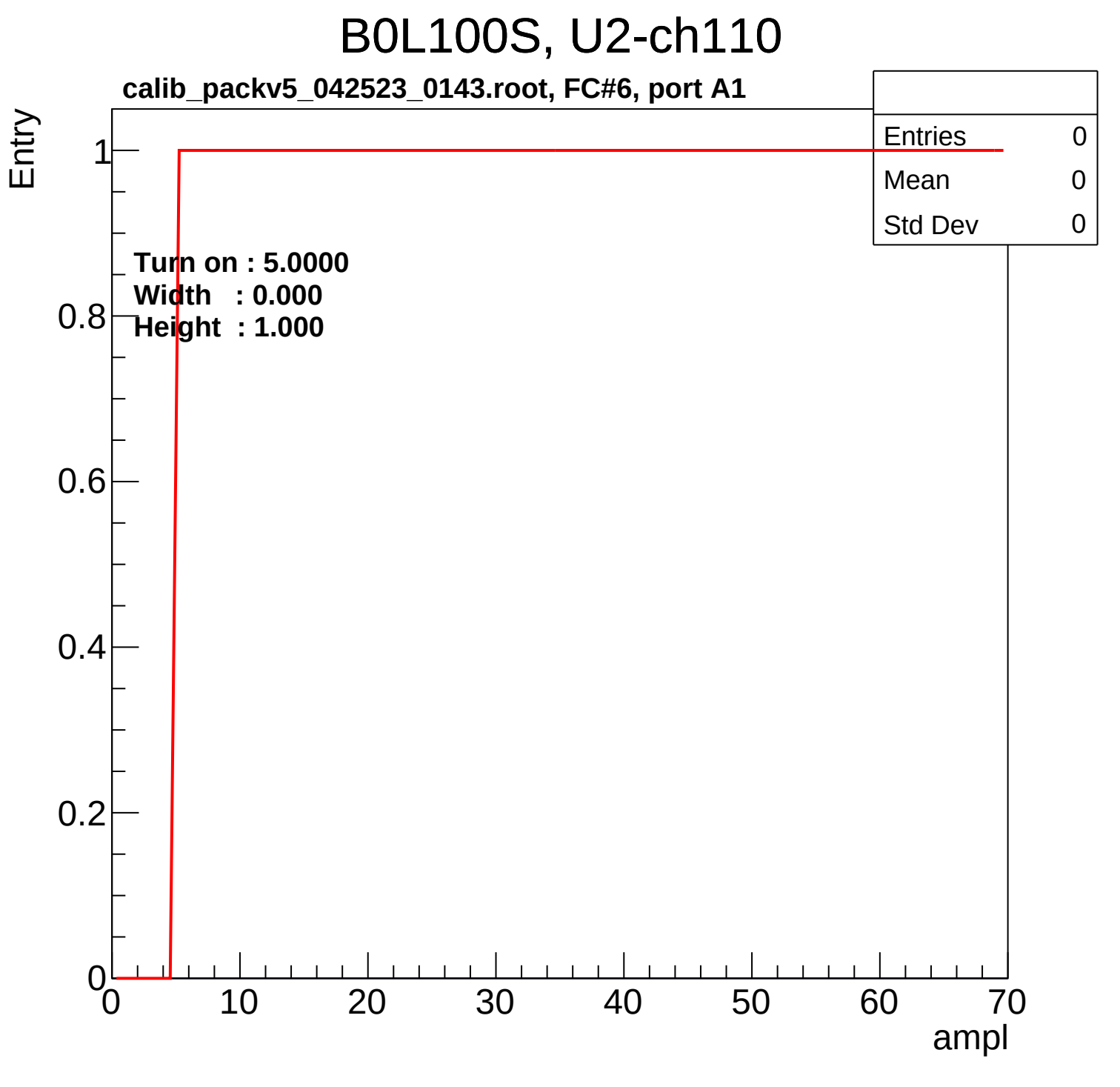
50
60
70
ampl


B0L100S, U2-ch110
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
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0.6
0.4
0.2
0
0
10
20
30
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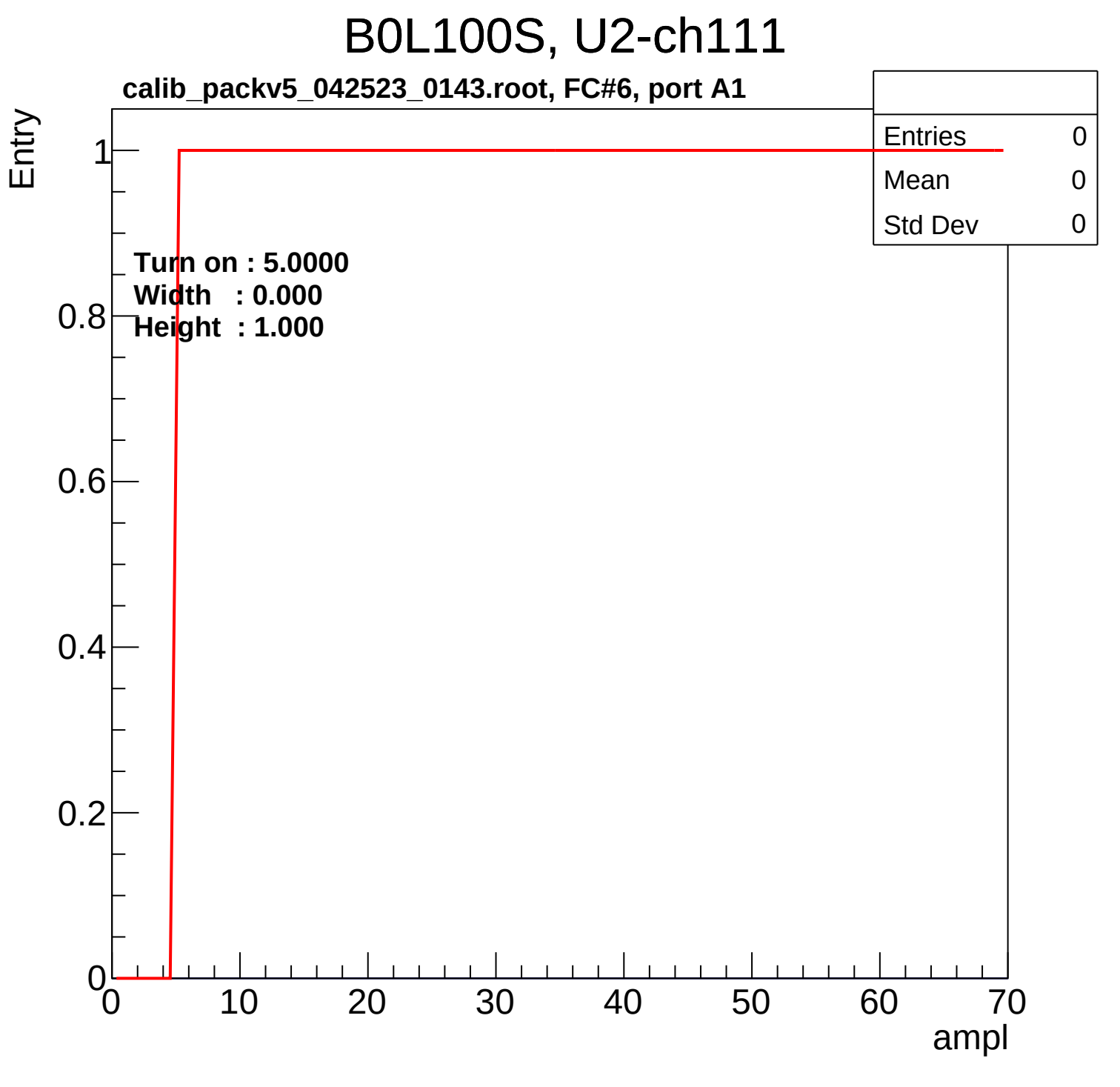
50
60
70
ampl


B0L100S, U2-ch111
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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0.6
0.4
0.2
0
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10
20
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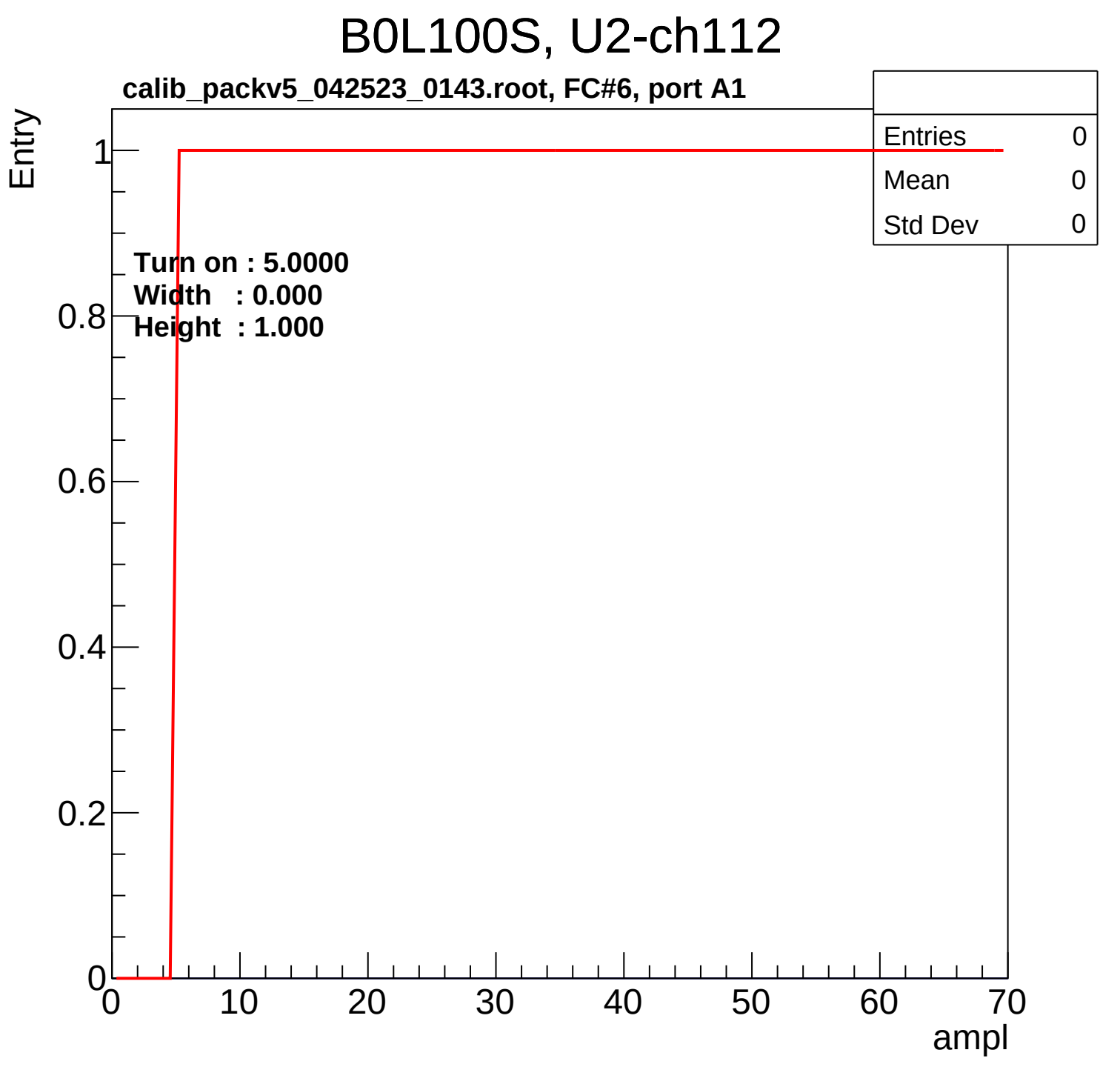
50
60
70
ampl


B0L100S, U2-ch112
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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0.6
0.4
0.2
0
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10
20
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50
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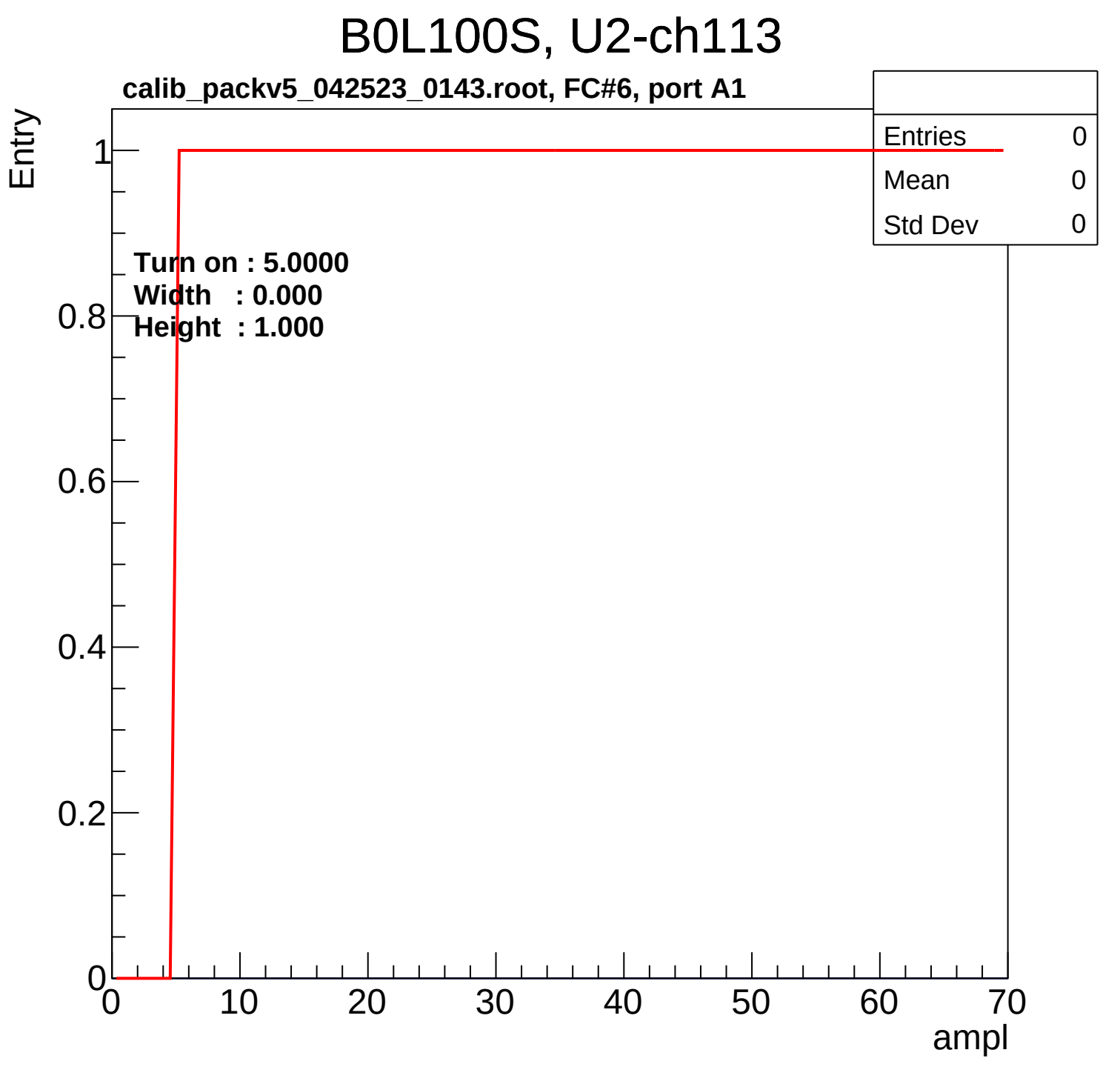
70
ampl


B0L100S, U2-ch113
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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0.6
0.4
0.2
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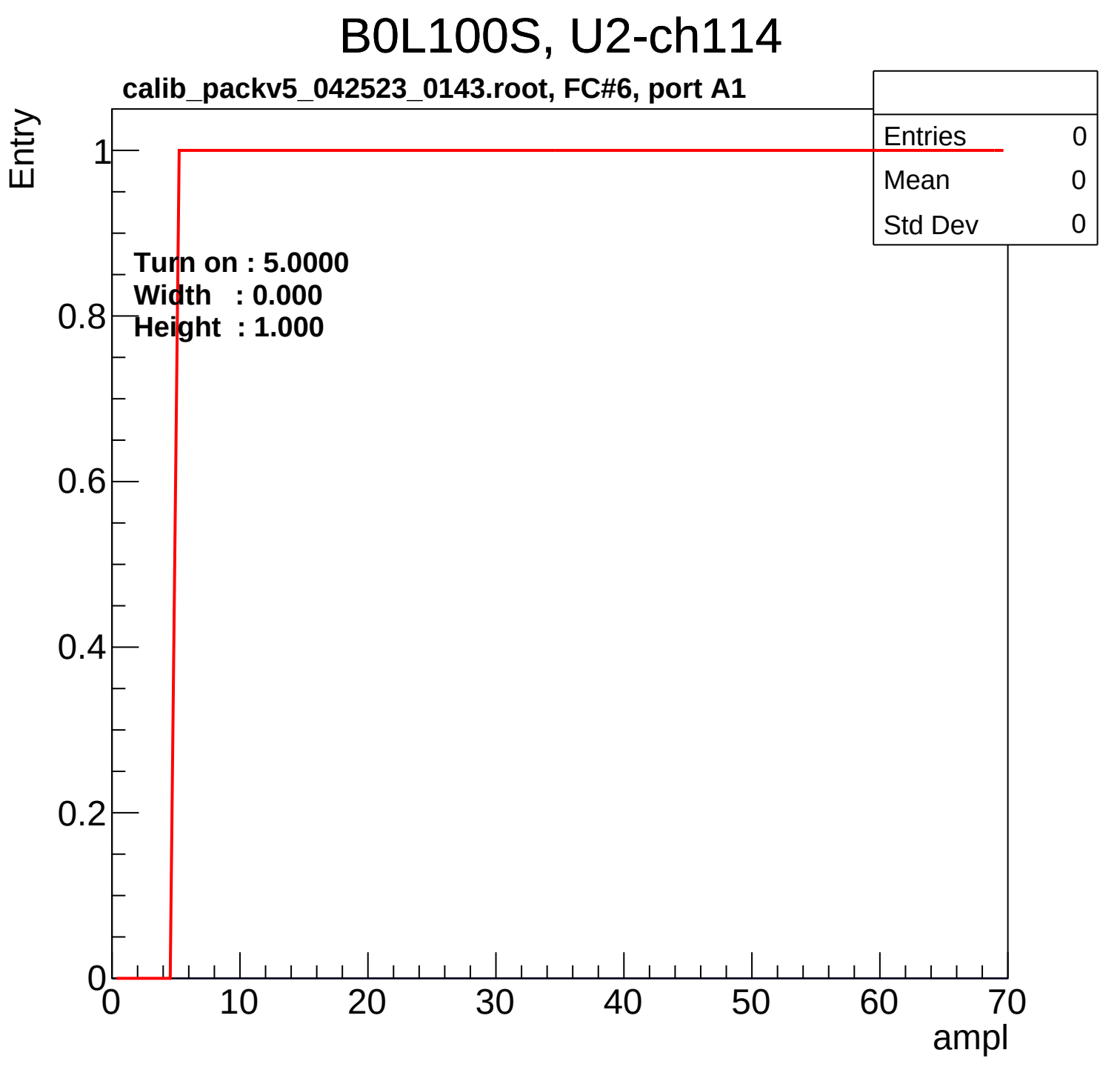
ampl


B0L100S, U2-ch114
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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0.8
0.6
0.4
0.2
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10
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50
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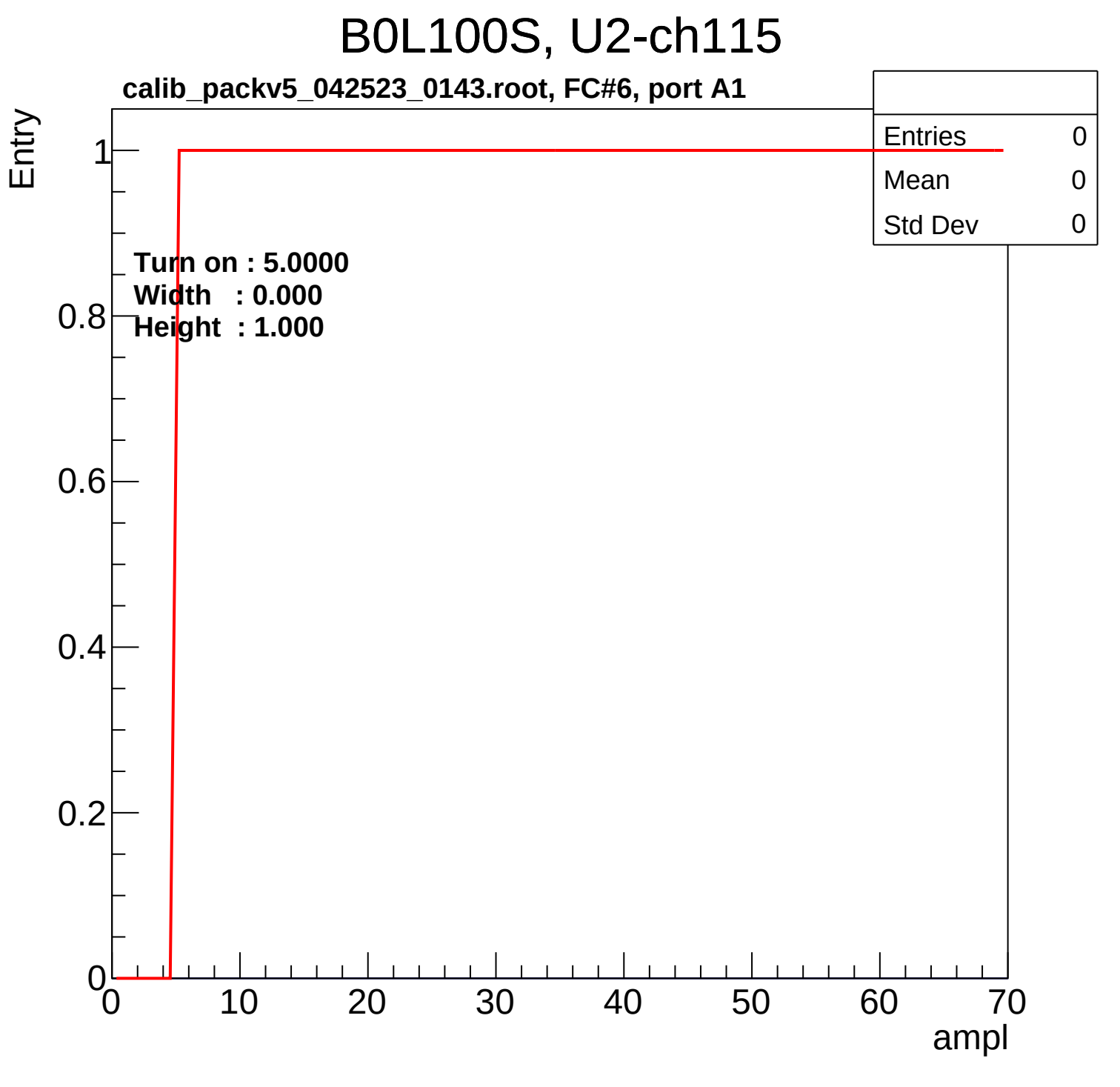
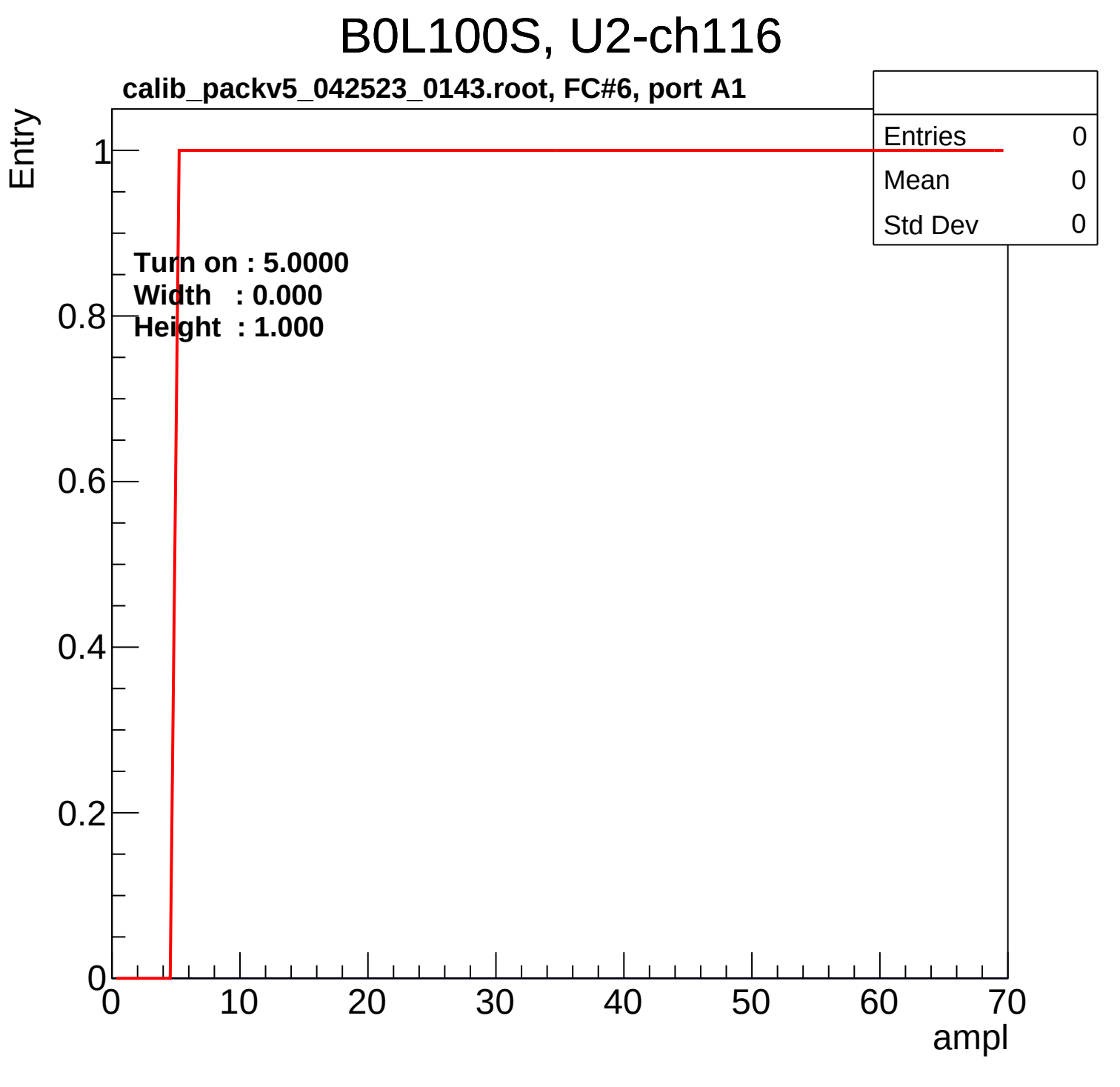
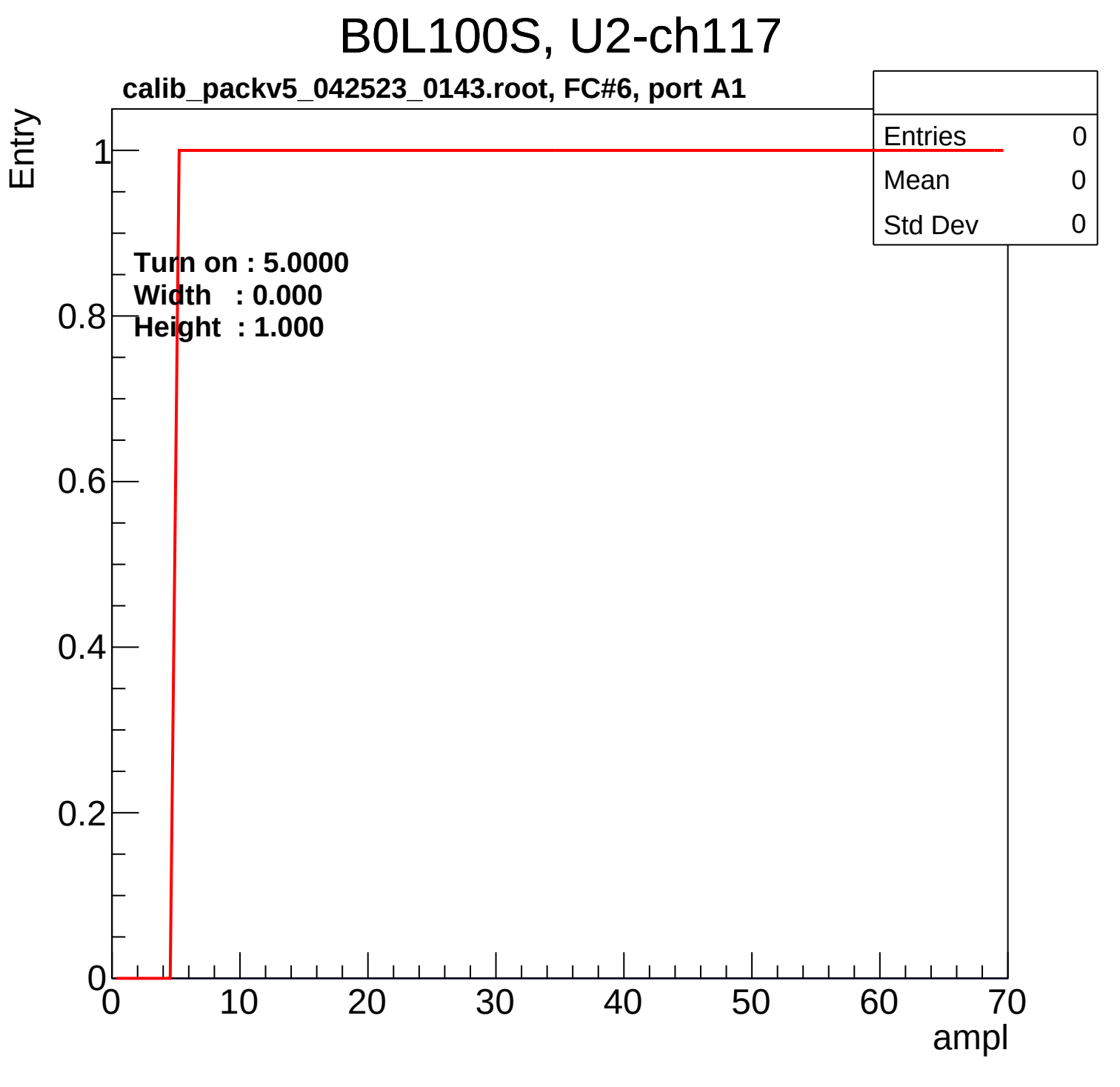
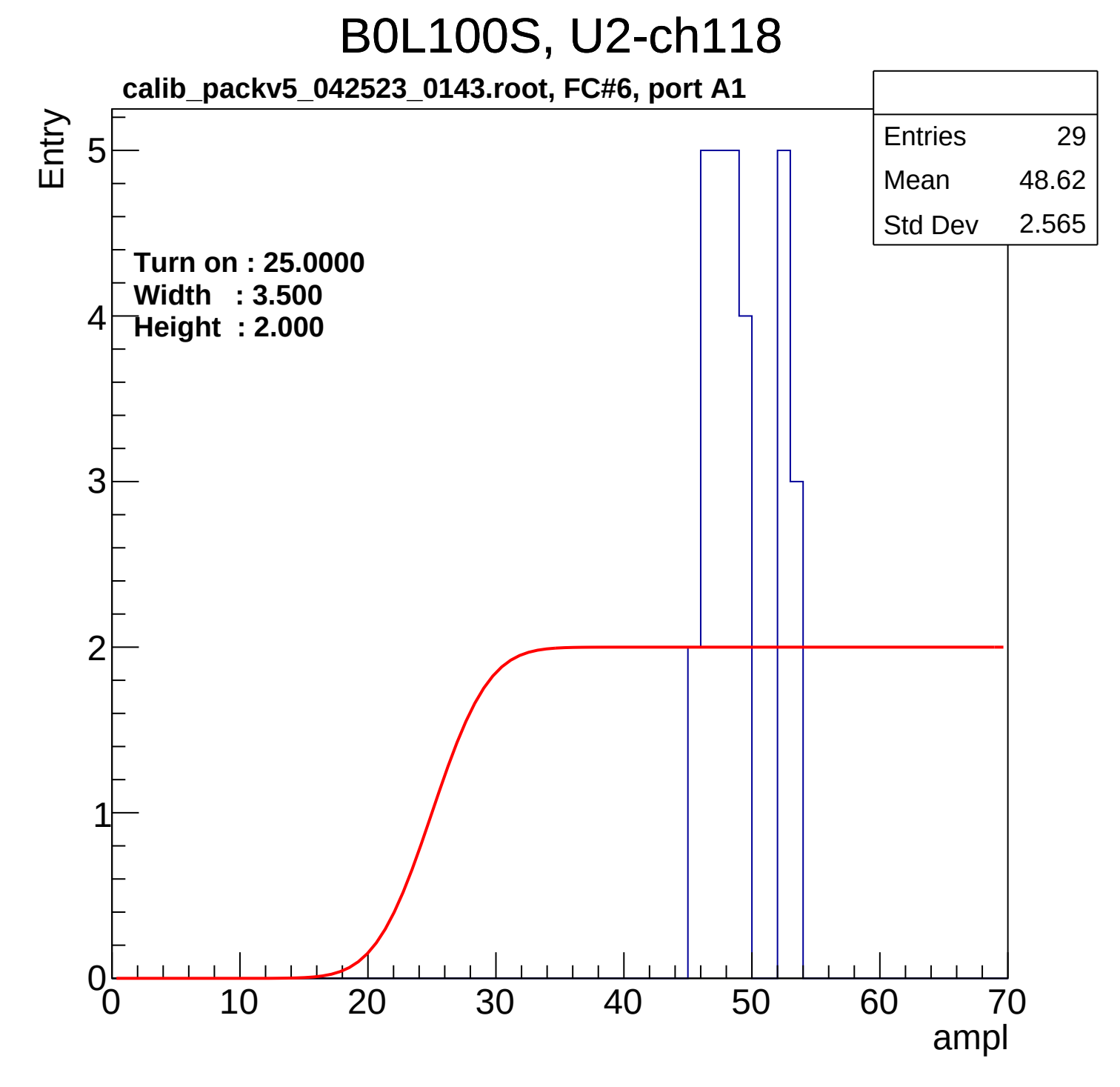
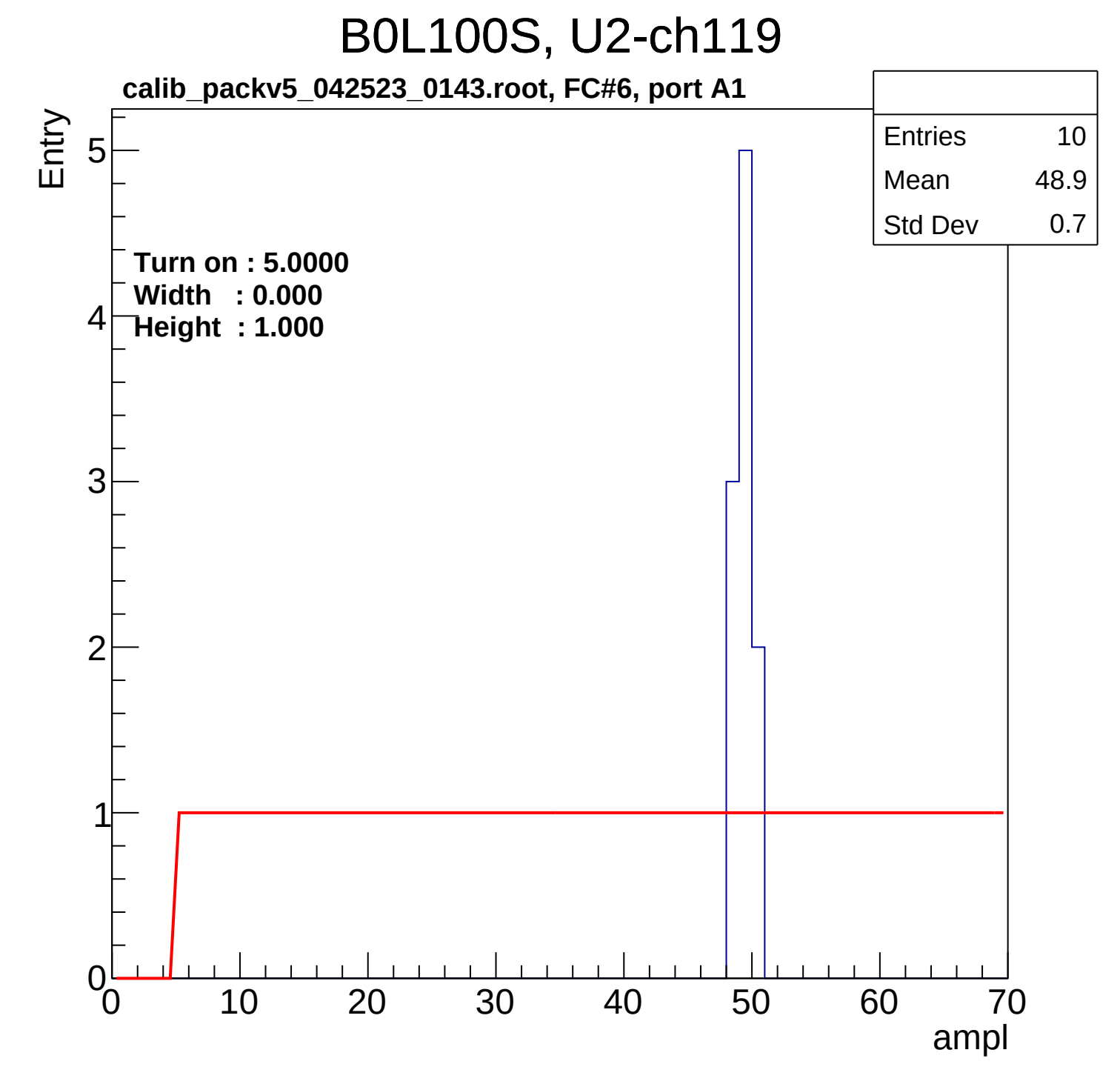
70
ampl

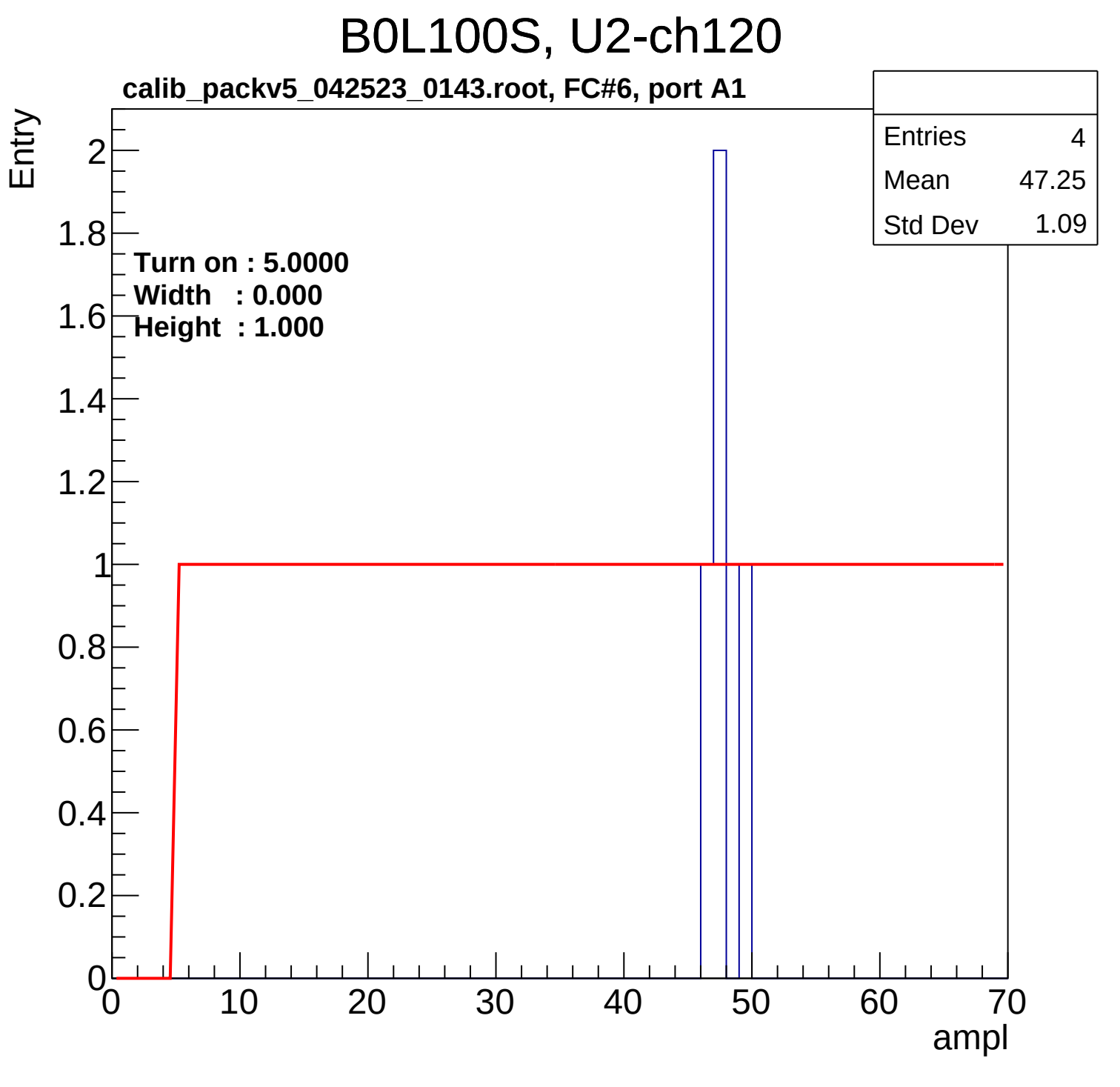

B0L100S, U2-ch115
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

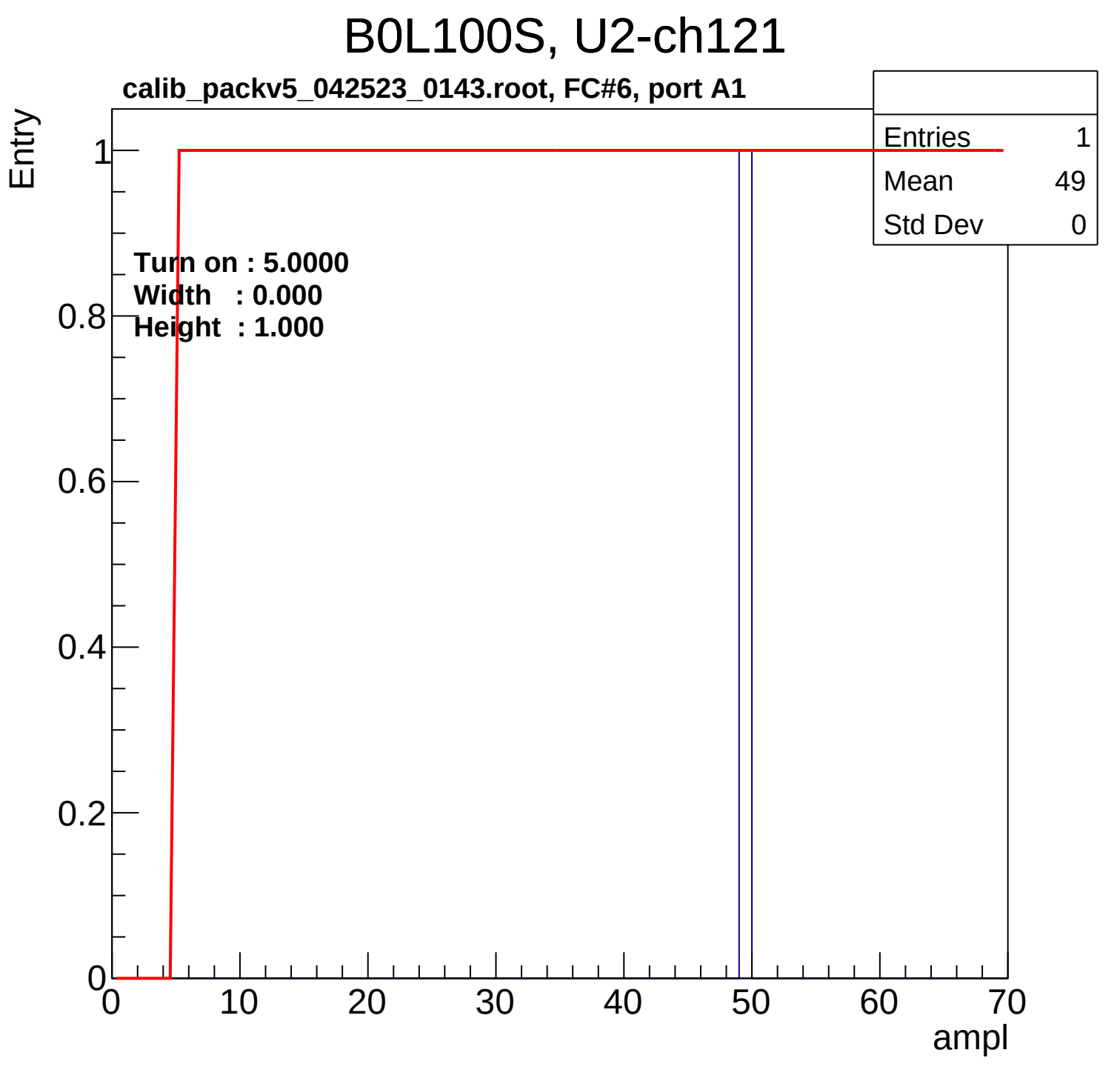

B0L100S, U2-ch116
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

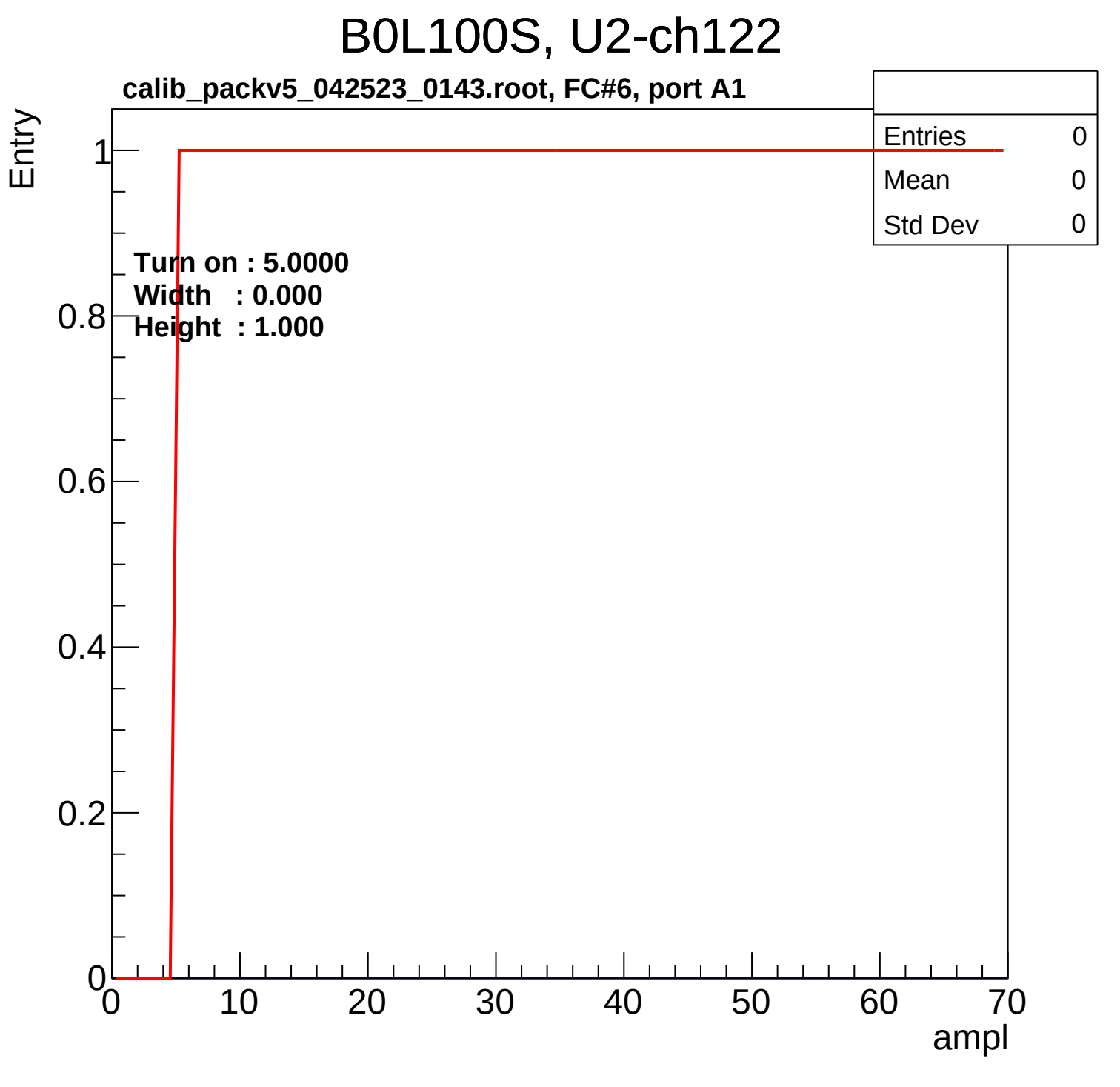

B0L100S, U2-ch117
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

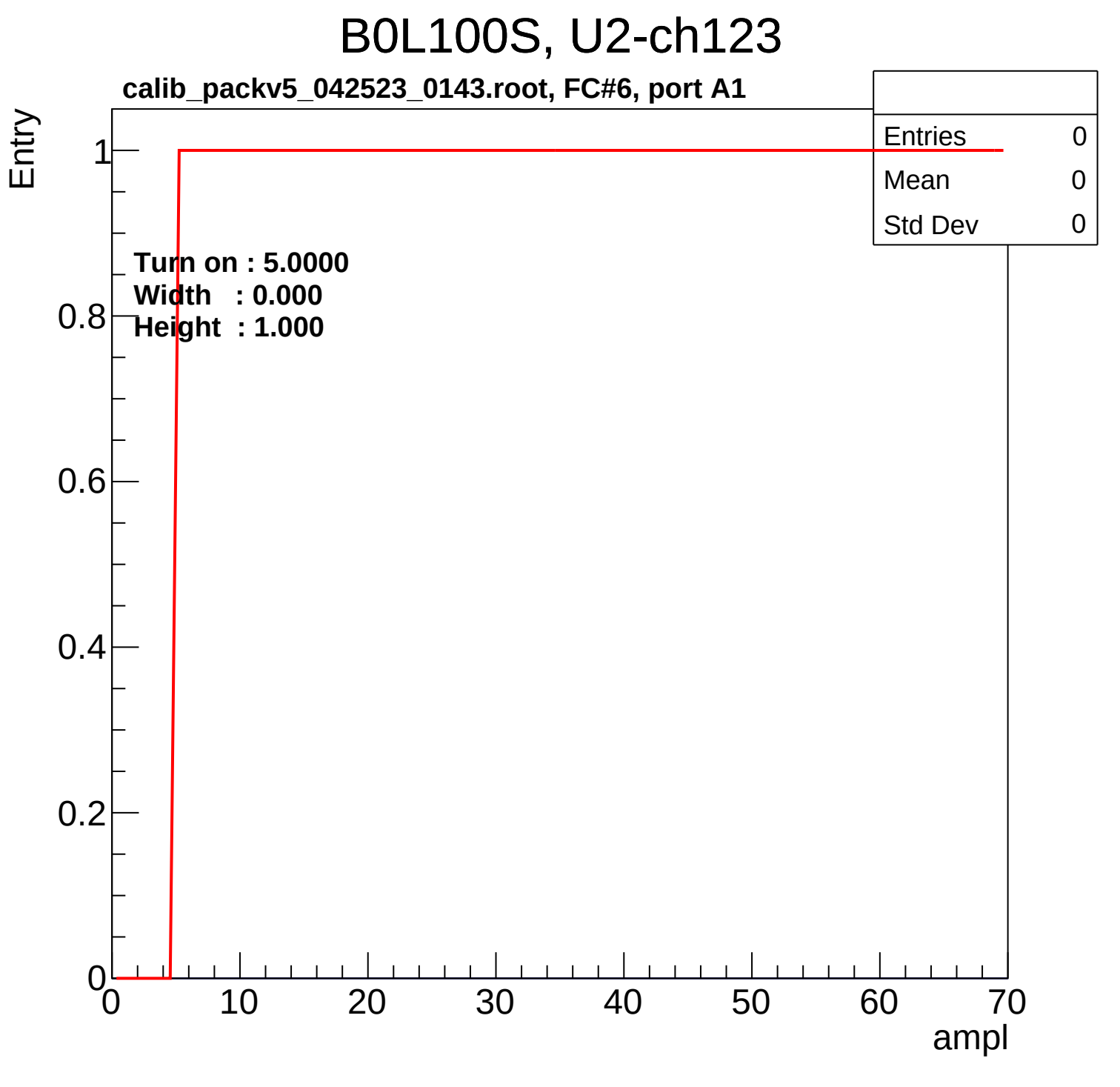

B0L100S, U2-ch118
calib_packv5_042523_0143.root, FC#6, port A1
Entries 29
Mean 48.62
Std Dev 2.565
Turn on : 25.0000
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

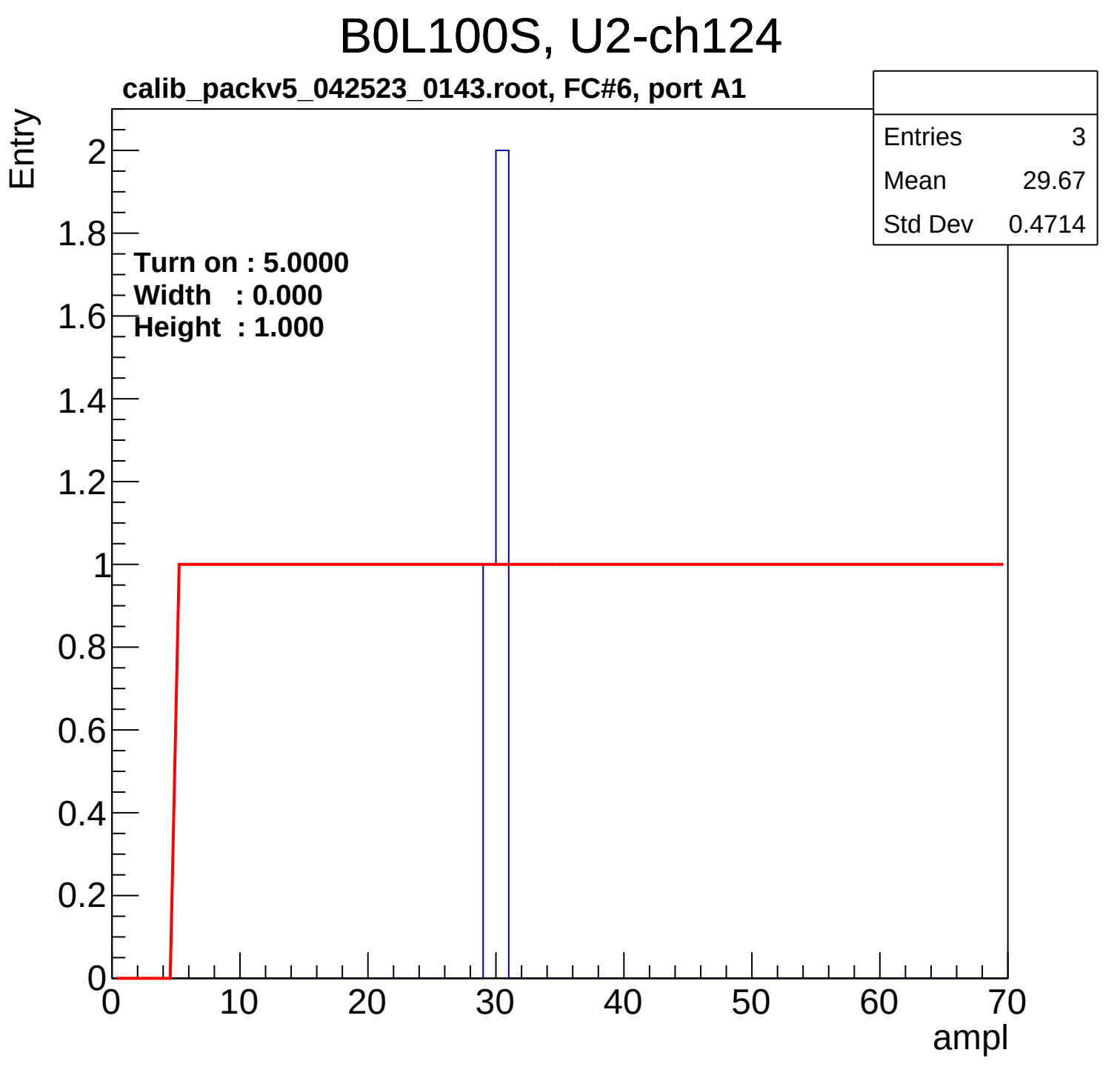

B0L100S, U2-ch119
calib_packv5_042523_0143.root, FC#6, port A1
Entries 10
Mean 48.9
Std Dev 0.7
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

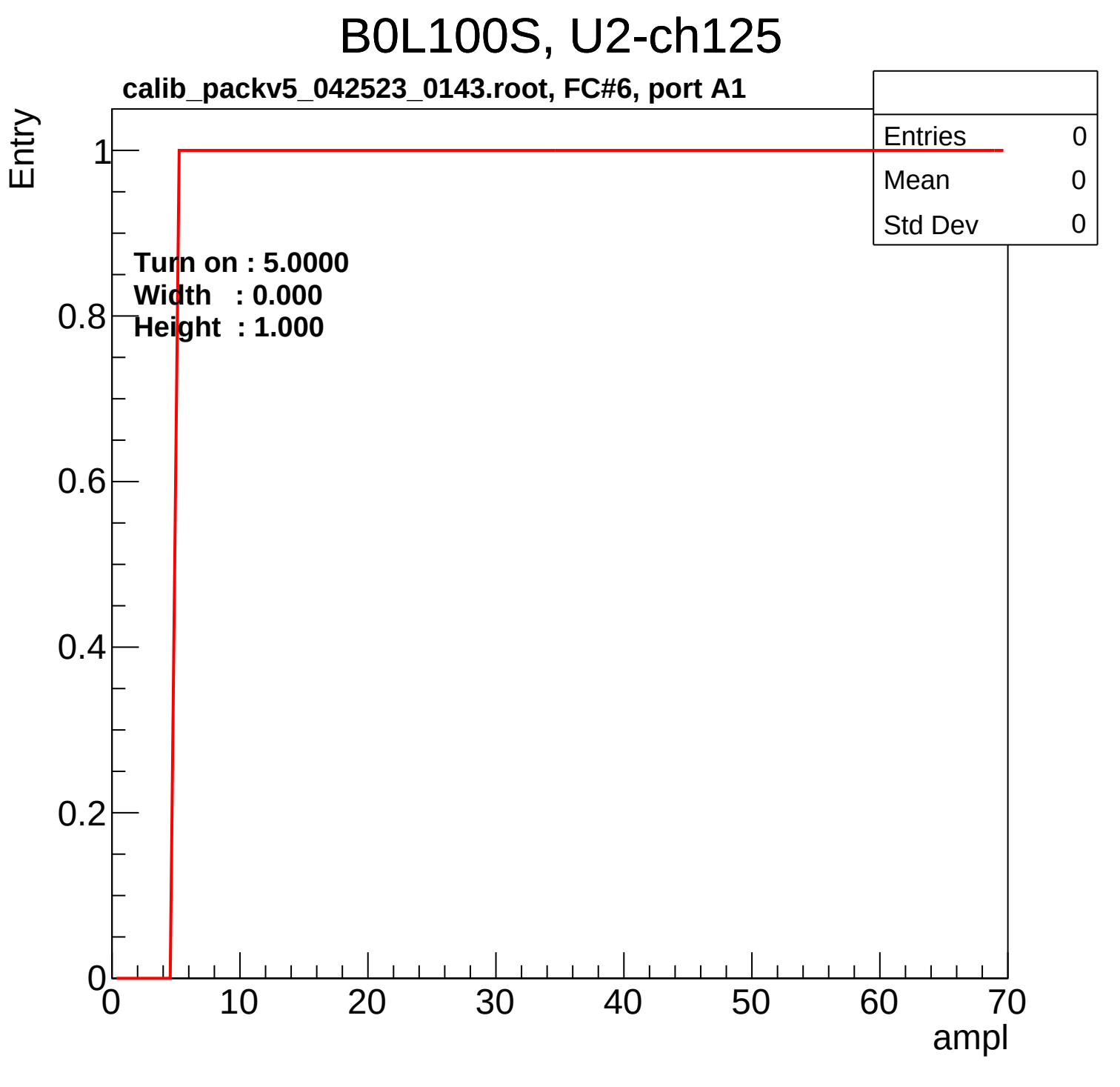

B0L100S, U2-ch120
calib_packv5_042523_0143.root, FC#6, port A1
Entries 4
Mean 47.25
Std Dev 1.09
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

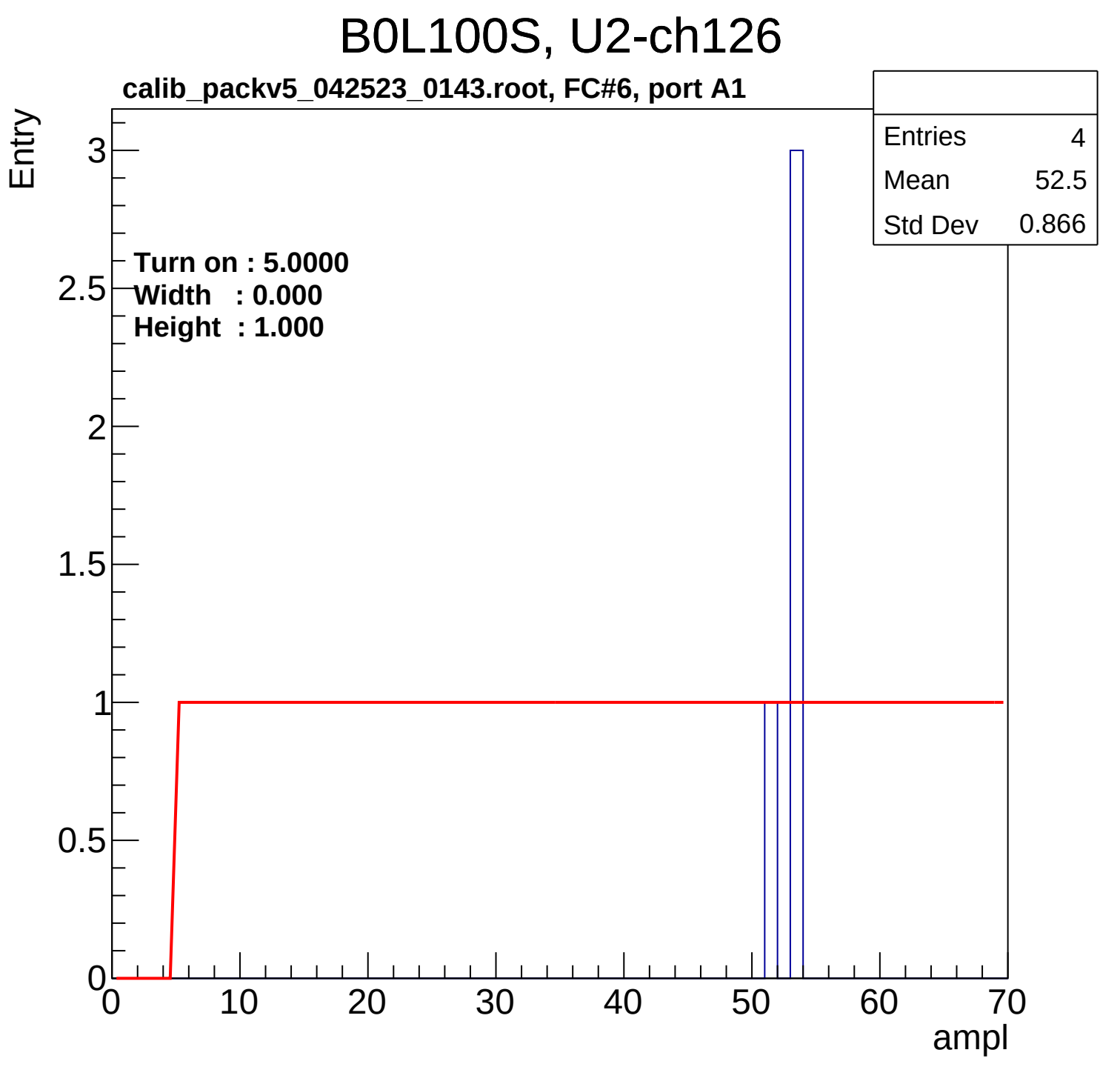

B0L100S, U2-ch121
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 49
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

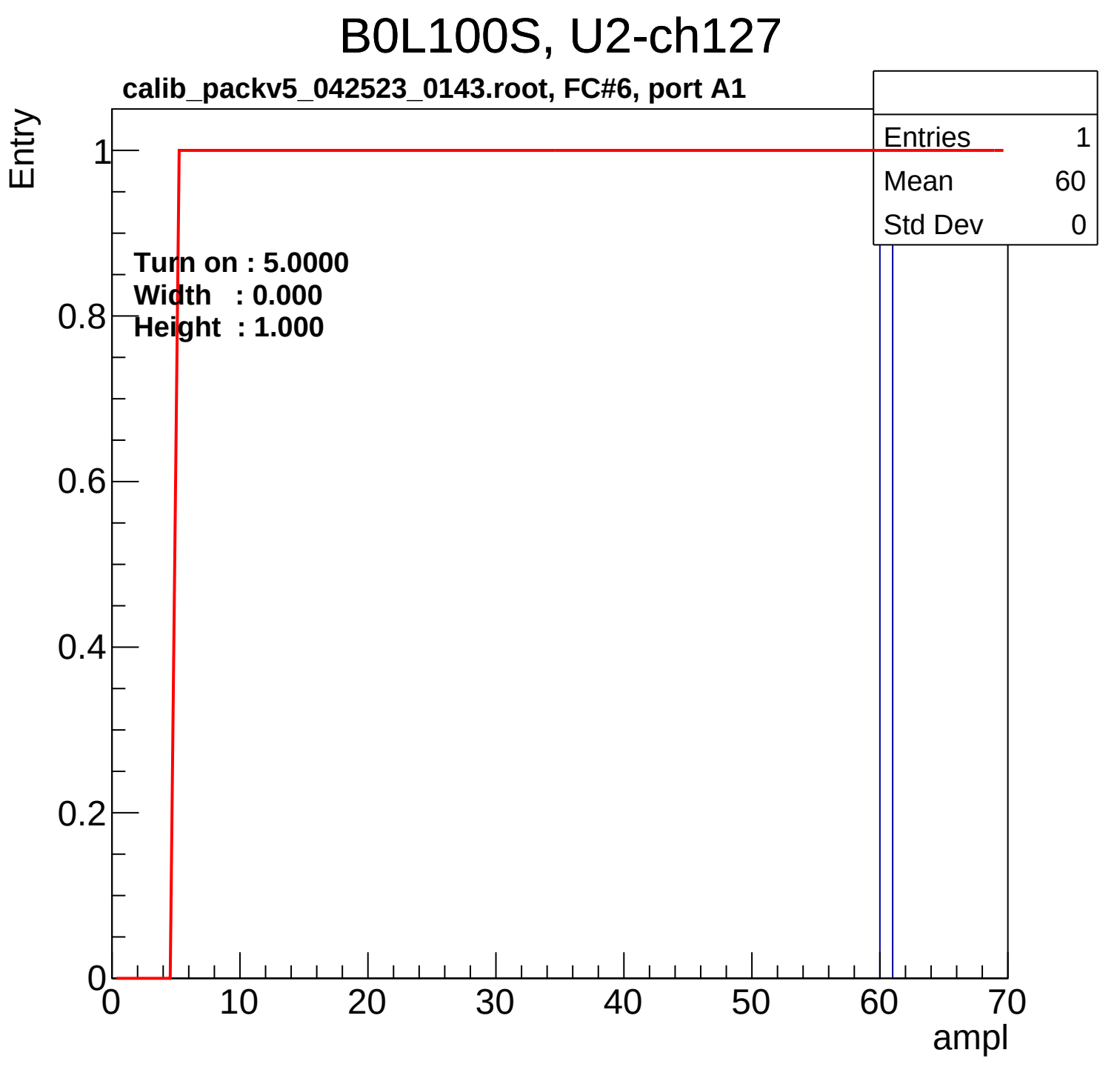

B0L100S, U2-ch122
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

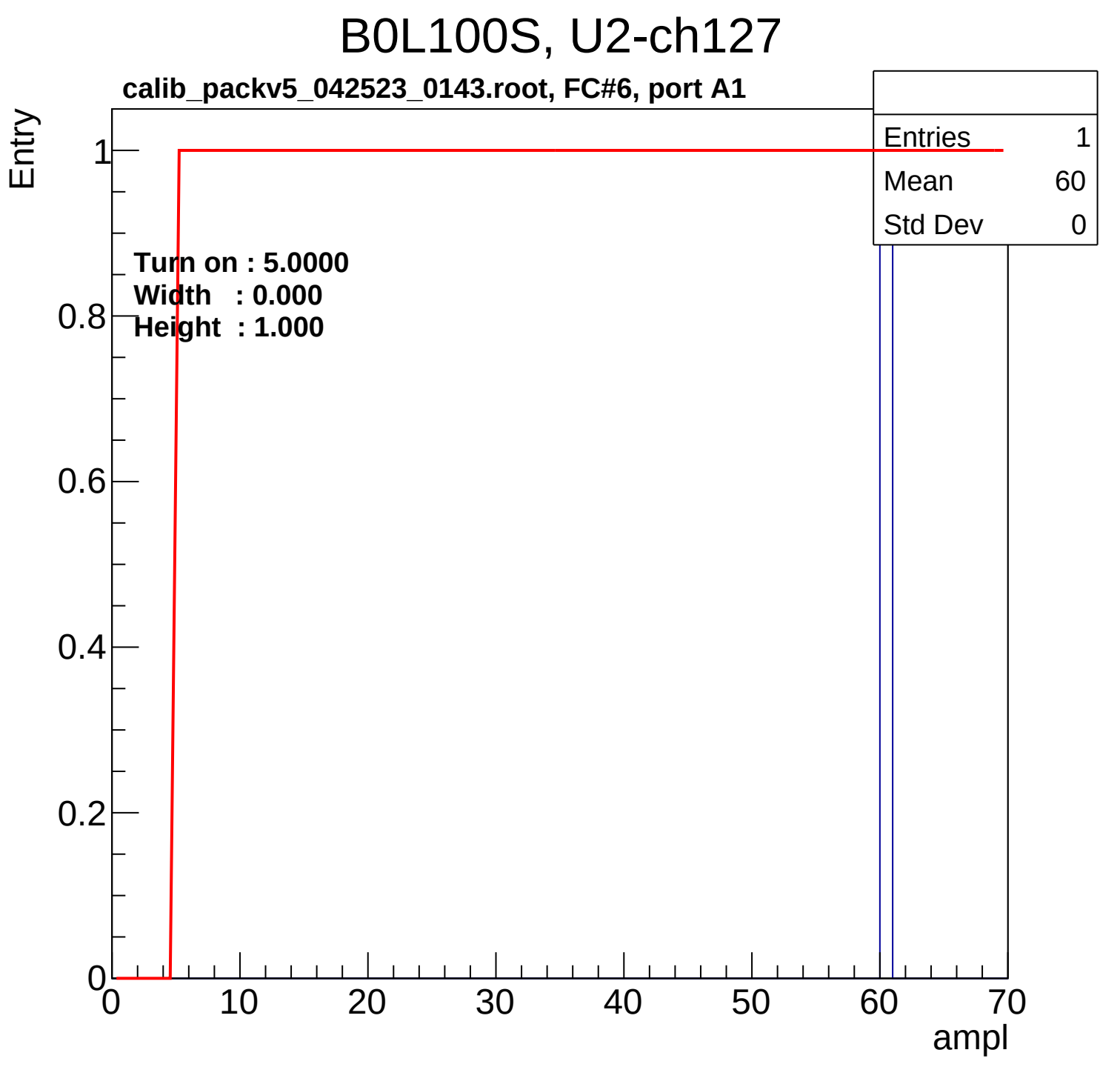

B0L100S, U2-ch123
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B0L100S, U2-ch124
calib_packv5_042523_0143.root, FC#6, port A1
Entries 3
Mean 29.67
Std Dev 0.4714
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B0L100S, U2-ch125
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U2-ch126
calib_packv5_042523_0143.root, FC#6, port A1
Entries 4
Mean 52.5
Std Dev 0.866
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B0L100S, U2-ch127
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 60
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B0L100S, U2-ch127
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 60
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70