

B1L101S, U14-ch0

calib_packv5_042523_0143.root, FC#0, port D2

Entries	406
Mean	42.8
Std Dev	12.63

Turn on : 23.9376

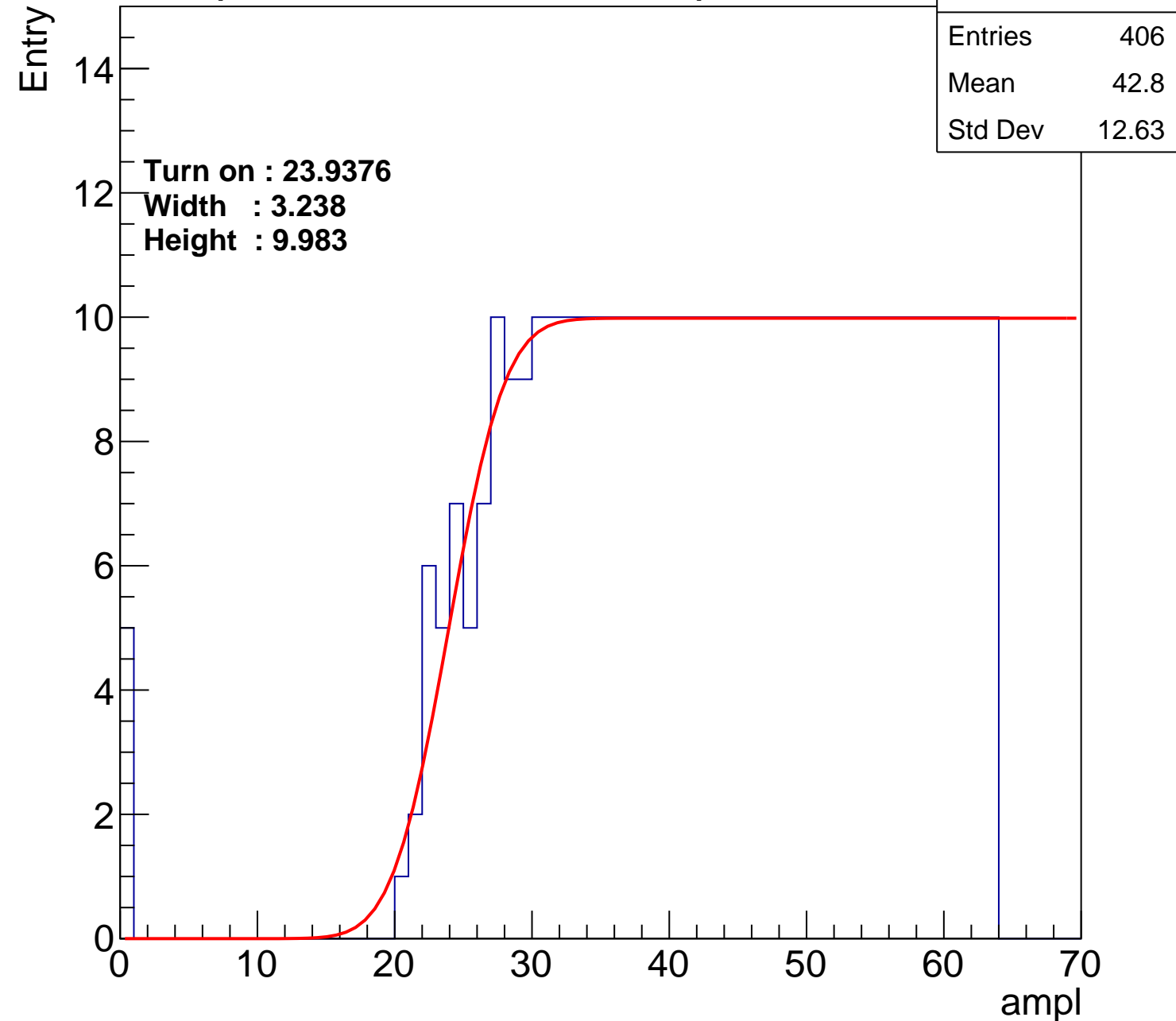
Width : 3.238

Height : 9.983

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch1

calib_packv5_042523_0143.root, FC#0, port D2

Entries	373
Mean	44.28
Std Dev	12.14

Turn on : 27.2390

Width : 3.137

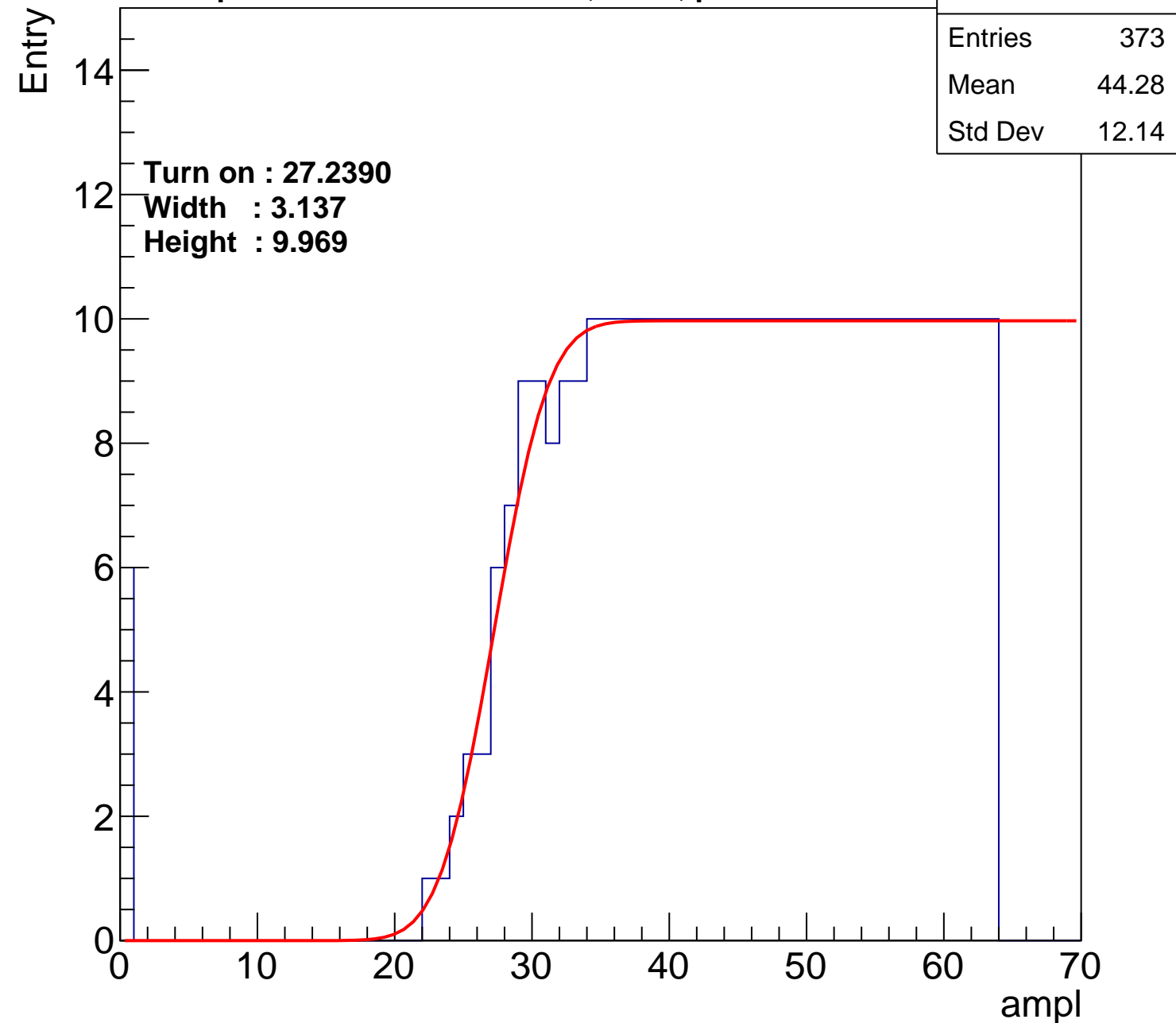
Height : 9.969

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L101S, U14-ch2

calib_packv5_042523_0143.root, FC#0, port D2

Entries	396
Mean	43.3
Std Dev	12.33

Turn on : 26.1395

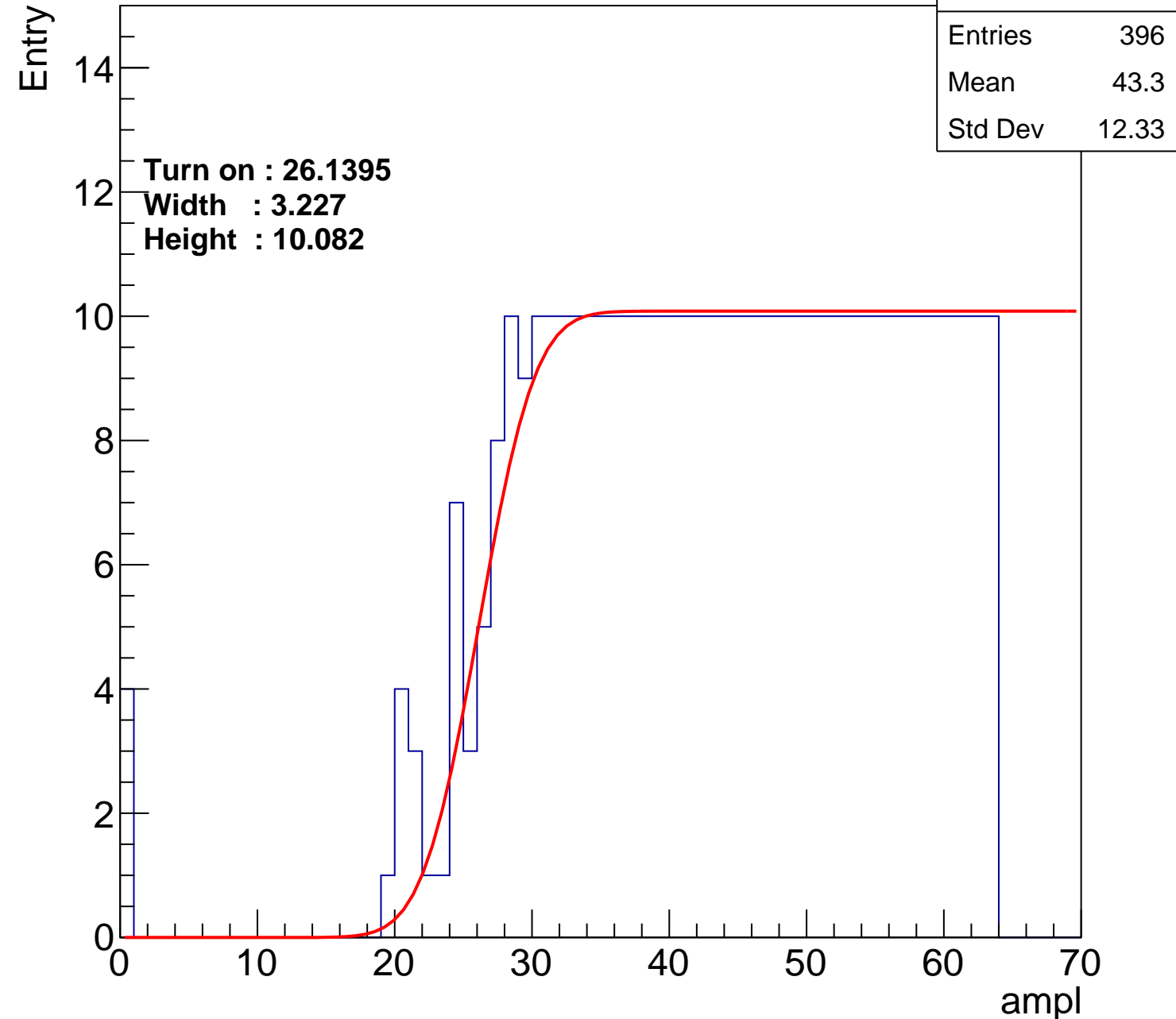
Width : 3.227

Height : 10.082

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch3

calib_packv5_042523_0143.root, FC#0, port D2

Entries	364
Mean	45.07
Std Dev	11

Turn on : 28.2432

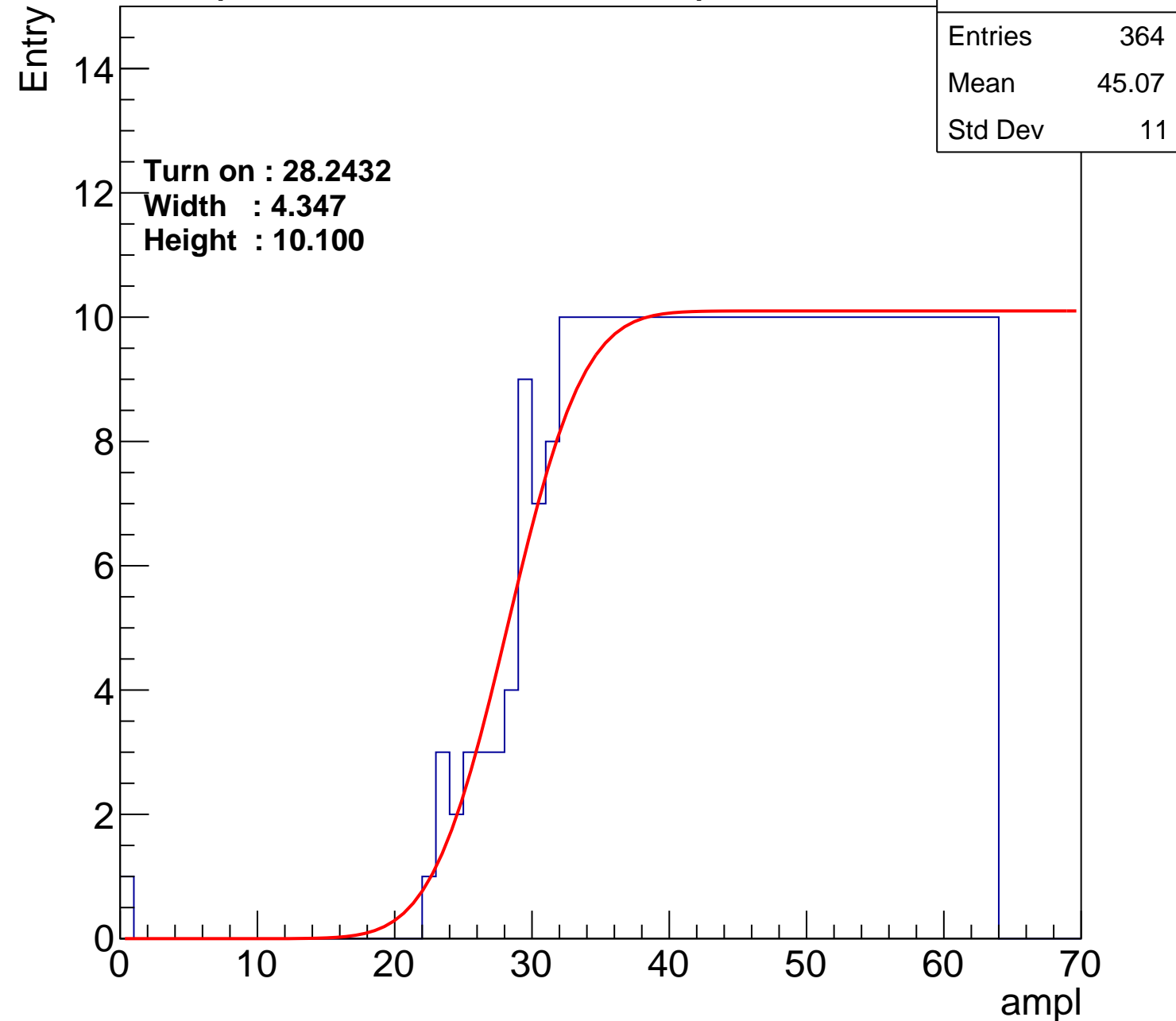
Width : 4.347

Height : 10.100

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch4

calib_packv5_042523_0143.root, FC#0, port D2

Entries	383
Mean	43.99
Std Dev	11.86

Turn on : 25.9984

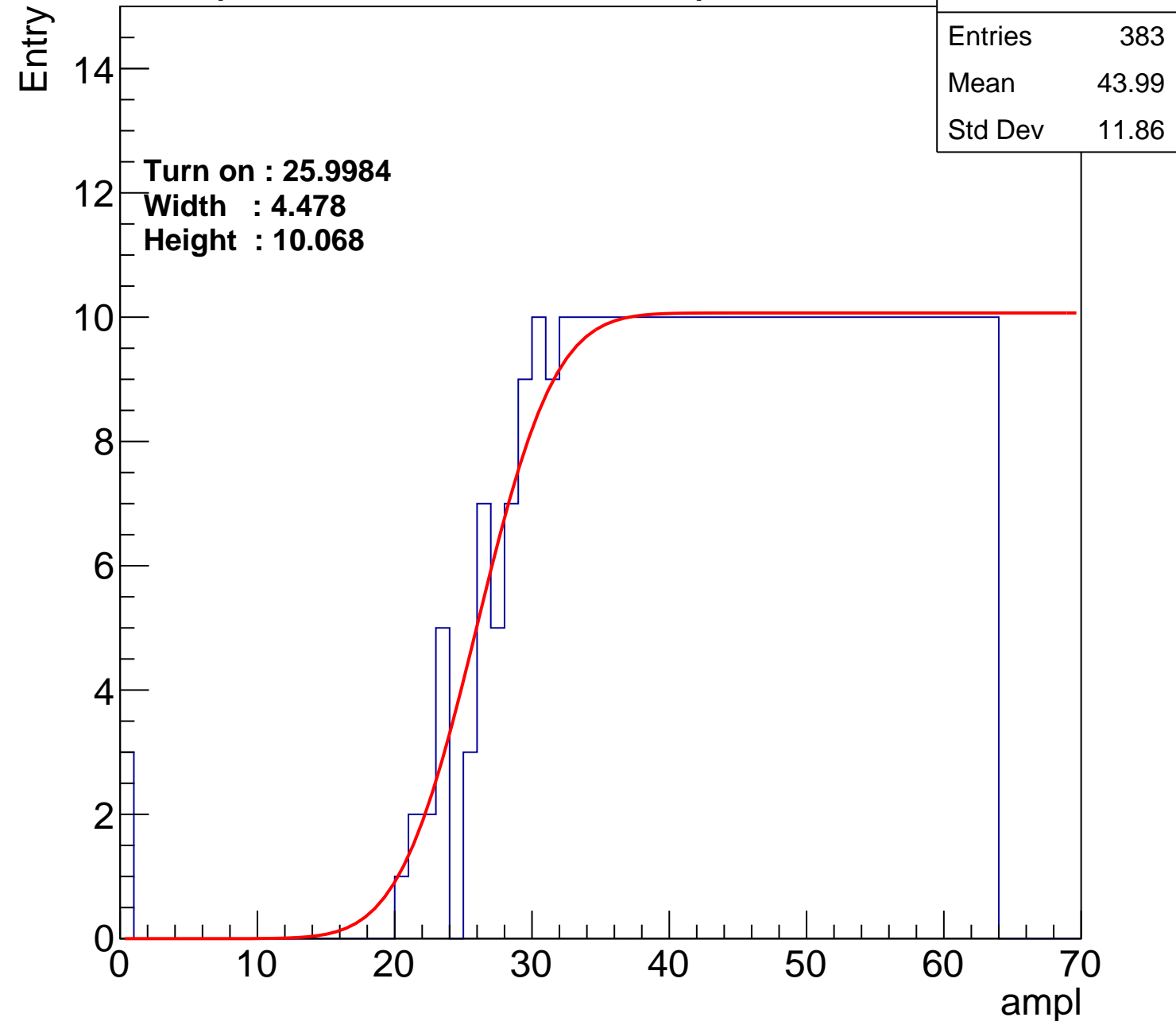
Width : 4.478

Height : 10.068

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch5

calib_packv5_042523_0143.root, FC#0, port D2

Entries	368
Mean	44.71
Std Dev	11.51

Turn on : 27.3261

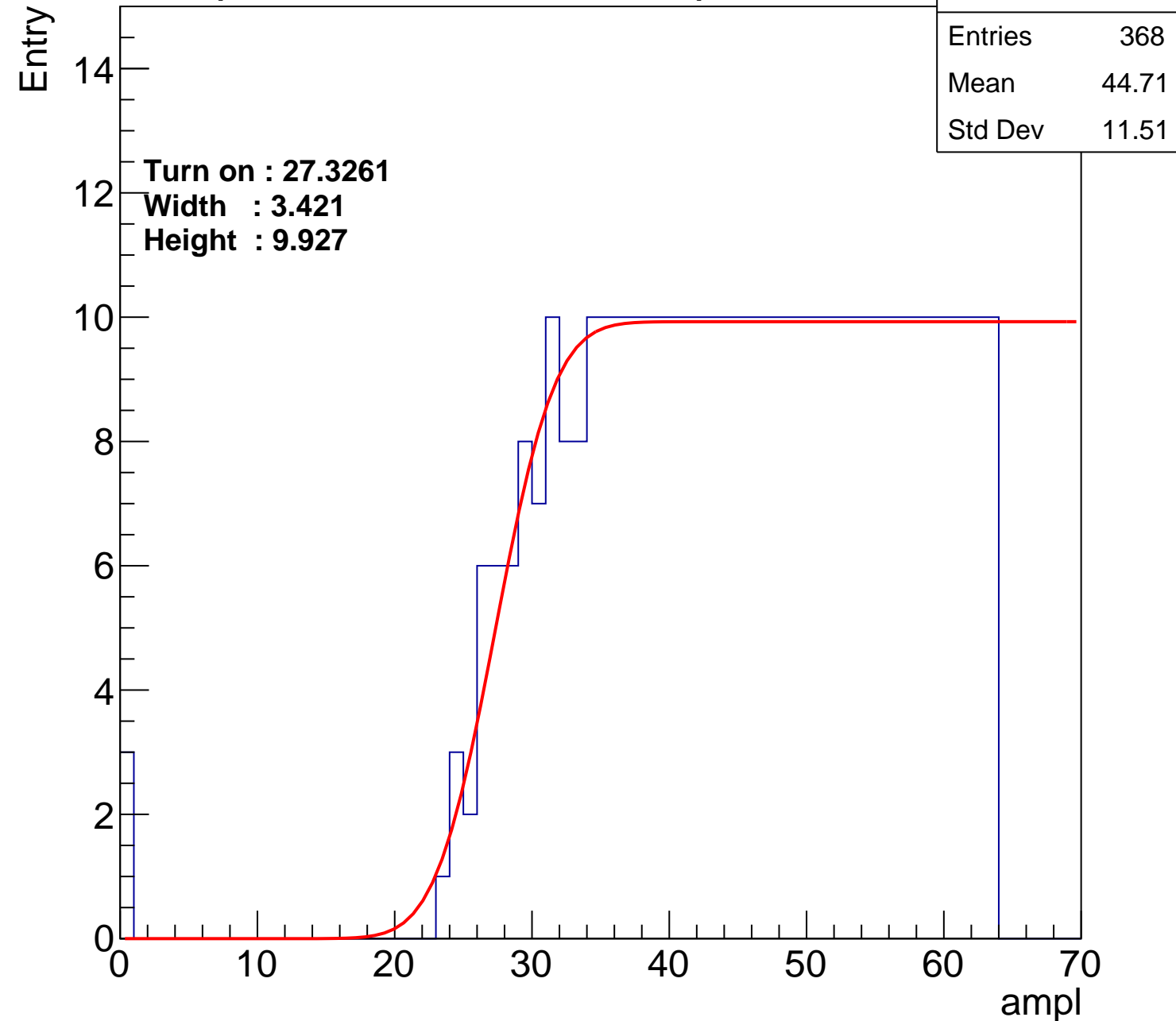
Width : 3.421

Height : 9.927

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch6

calib_packv5_042523_0143.root, FC#0, port D2

Entries	353
Mean	45.6
Std Dev	10.81

Turn on : 29.0559

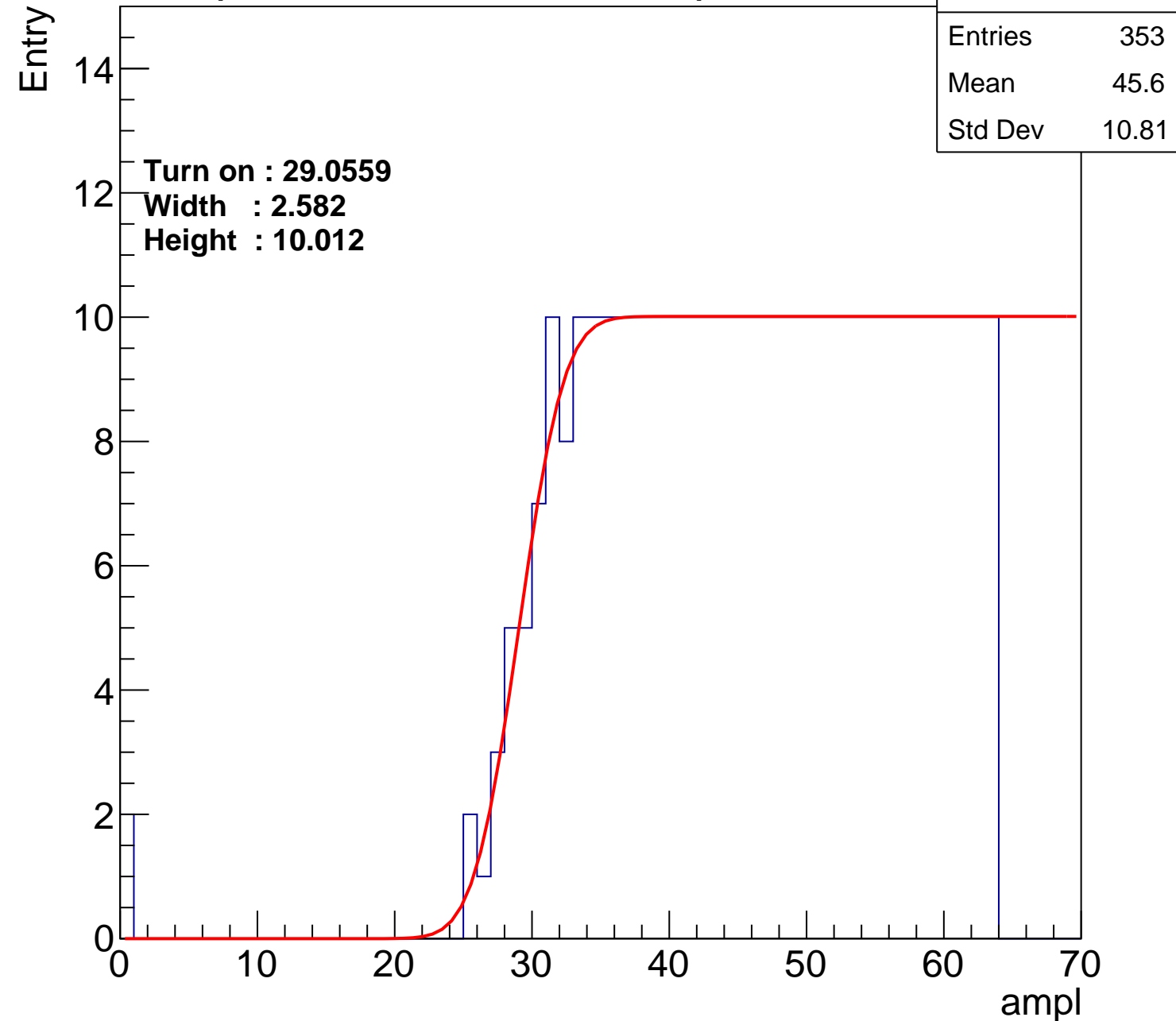
Width : 2.582

Height : 10.012

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch7

calib_packv5_042523_0143.root, FC#0, port D2

Entries	356
Mean	45.4
Std Dev	10.98

Turn on : 28.6687

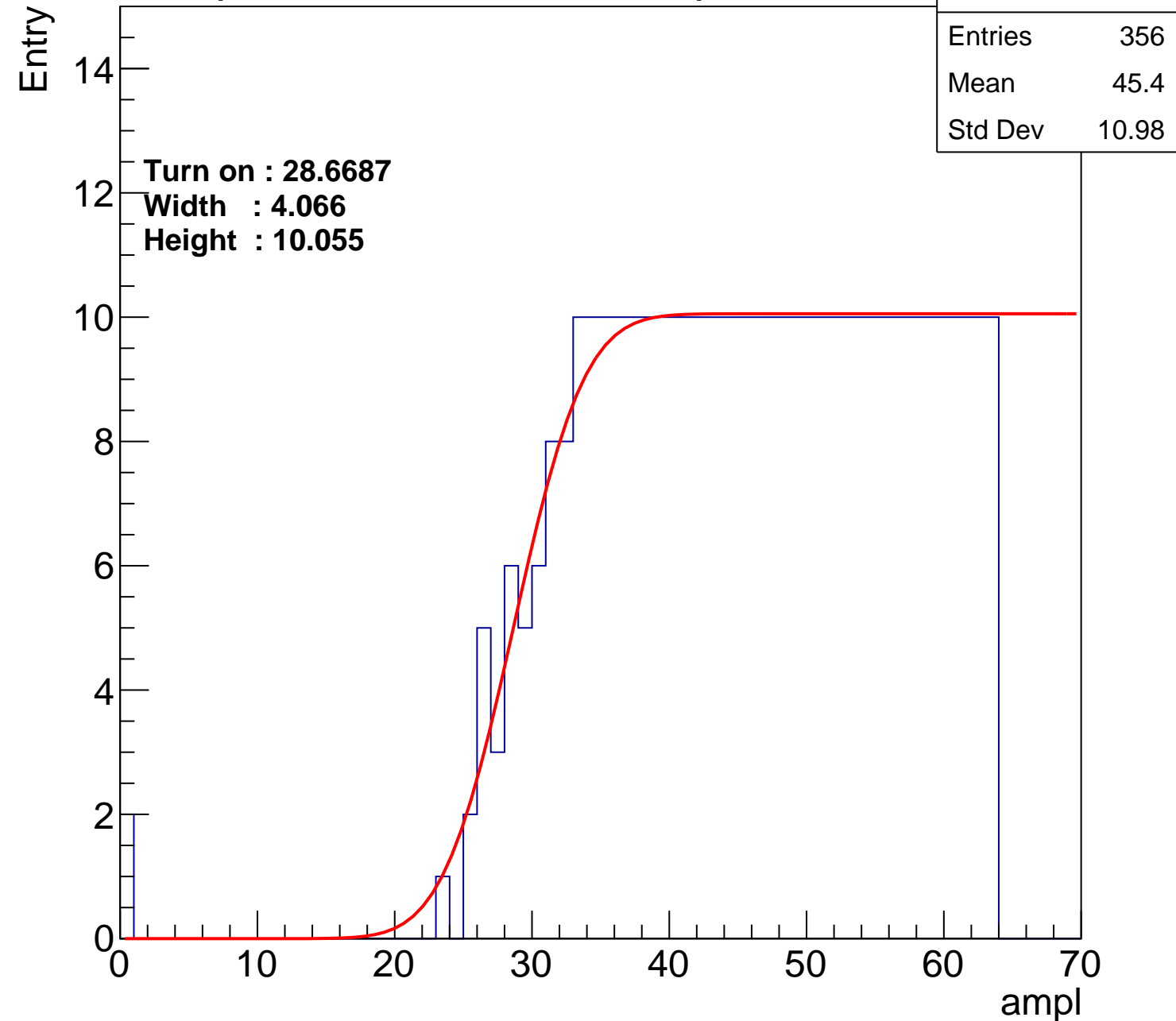
Width : 4.066

Height : 10.055

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch8

calib_packv5_042523_0143.root, FC#0, port D2

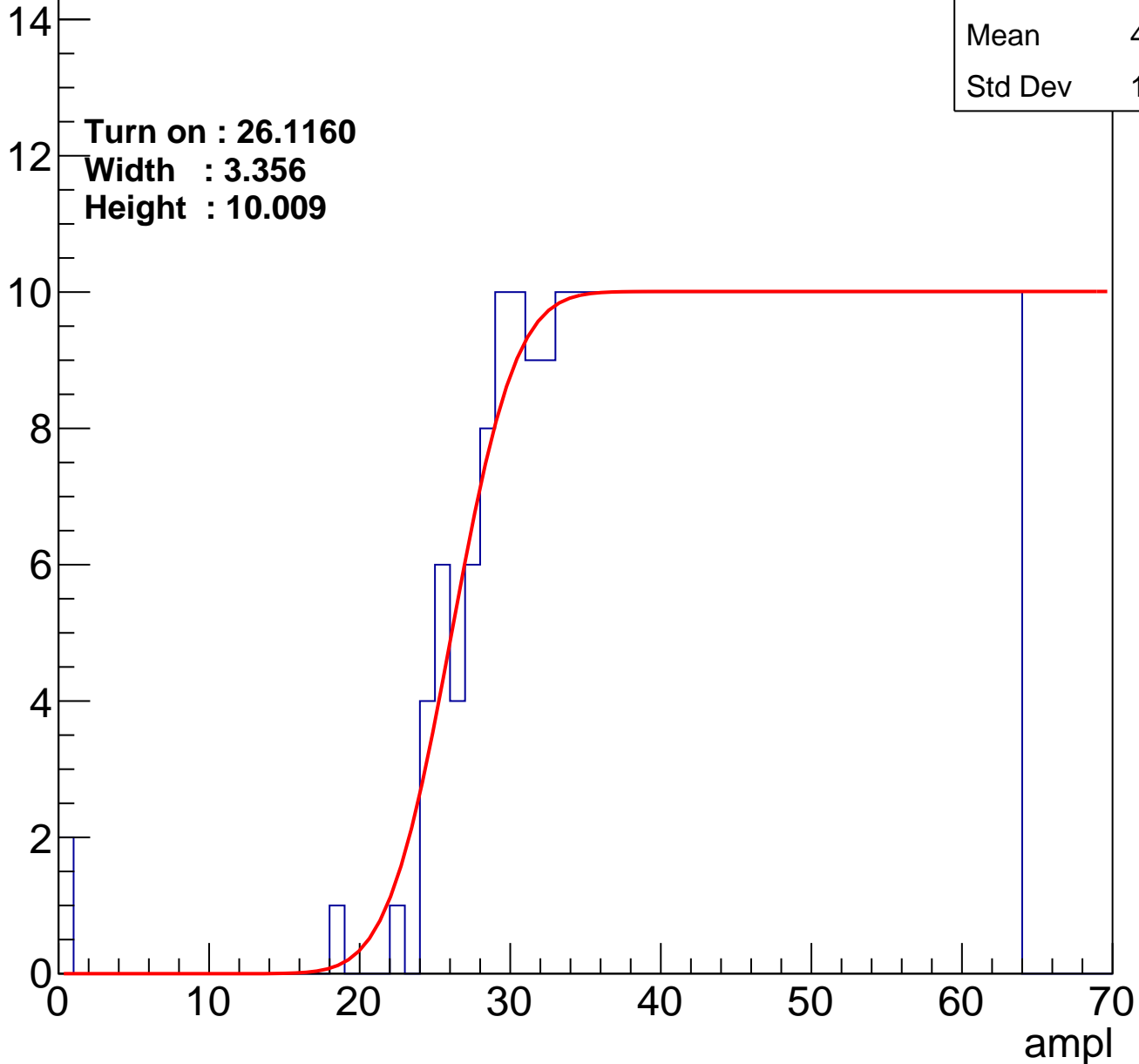
Entries	380
Mean	44.24
Std Dev	11.54

Turn on : 26.1160

Width : 3.356

Height : 10.009

Entry



B1L101S, U14-ch9

calib_packv5_042523_0143.root, FC#0, port D2

Entries	385
Mean	43.99
Std Dev	11.76

Turn on : 26.0757

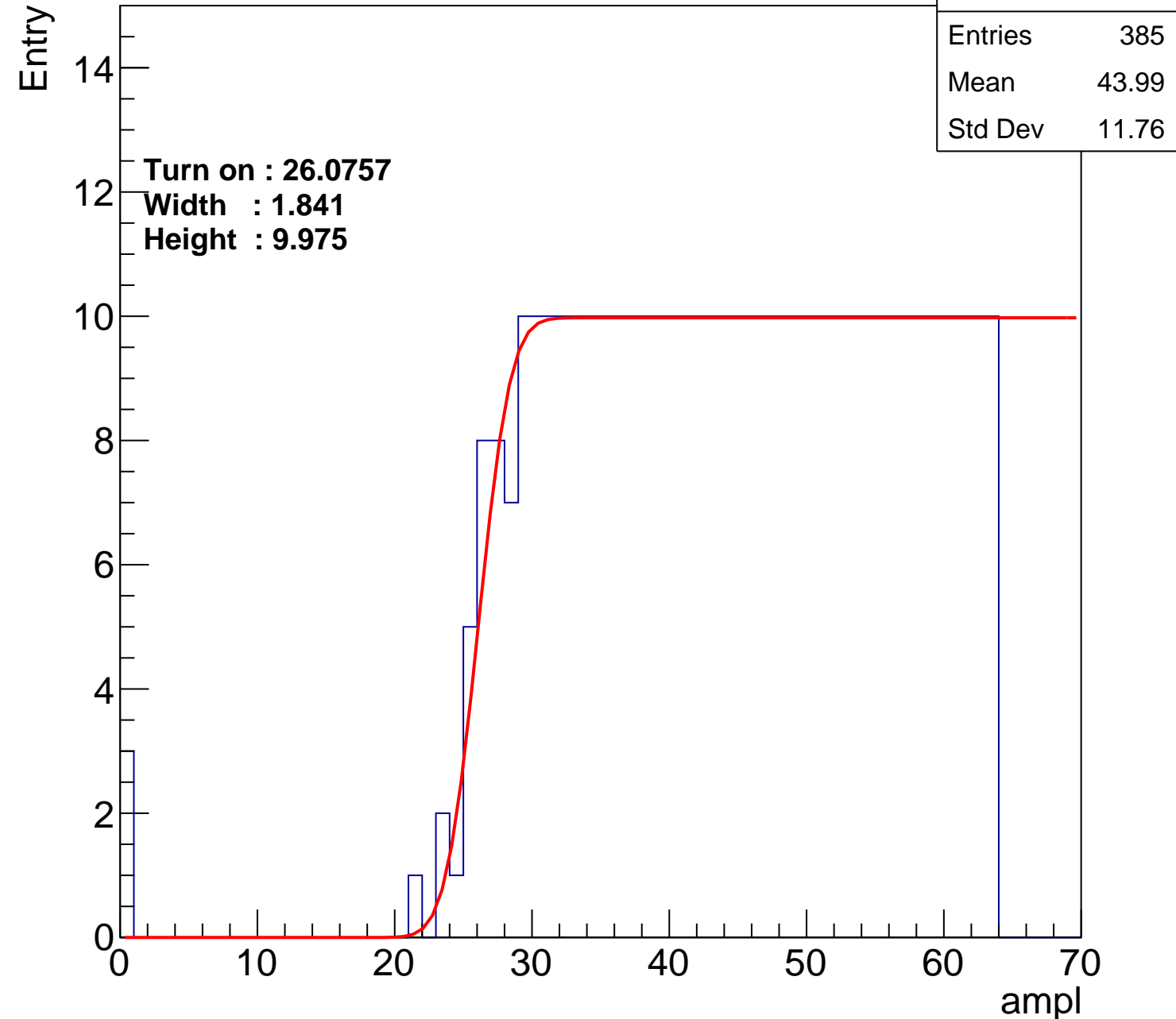
Width : 1.841

Height : 9.975

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch10

calib_packv5_042523_0143.root, FC#0, port D2

Entries	367
Mean	44.79
Std Dev	11.46

Turn on : 28.1856

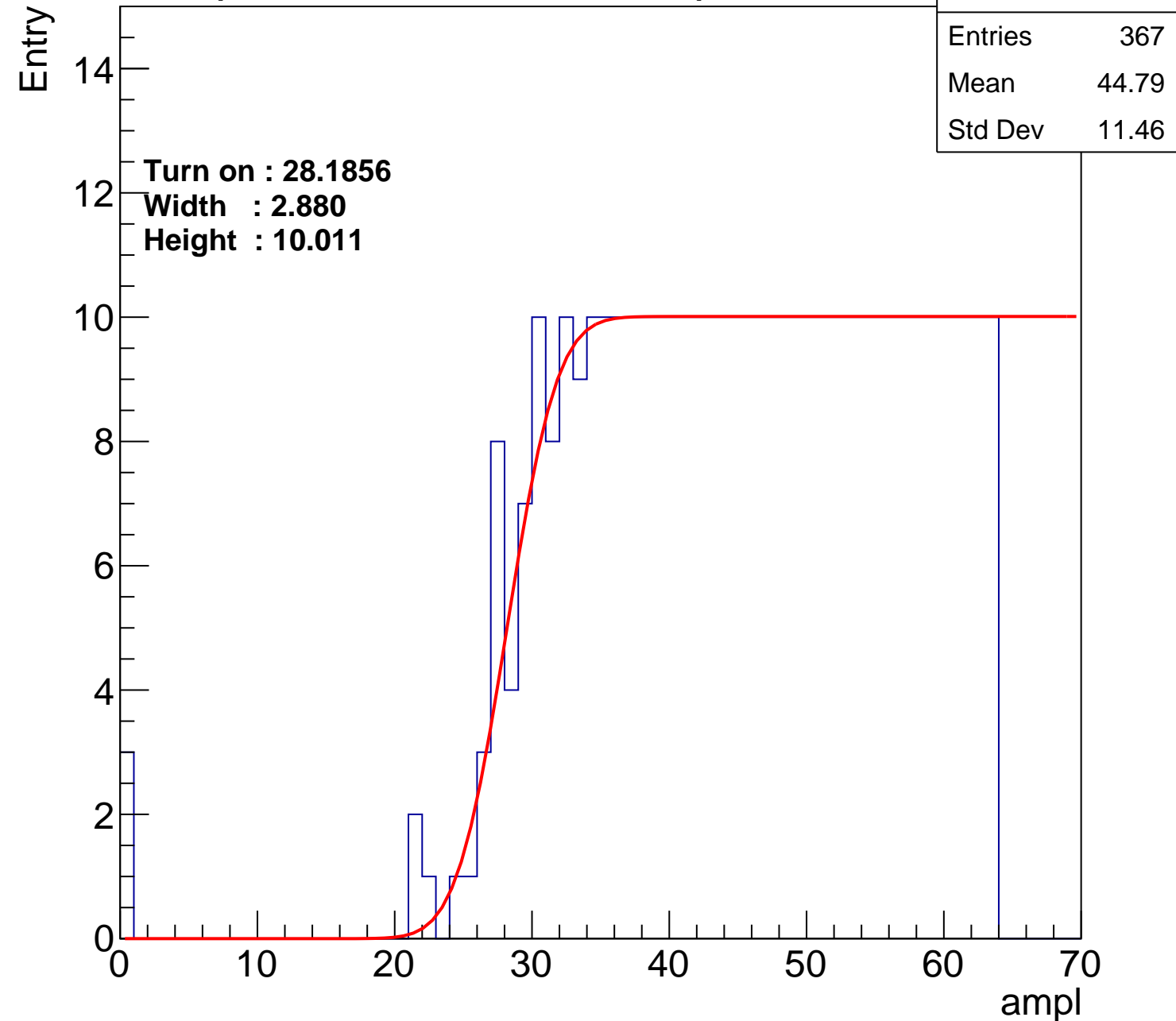
Width : 2.880

Height : 10.011

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch11

calib_packv5_042523_0143.root, FC#0, port D2

Entries	371
Mean	44.7
Std Dev	11.29

Turn on : 26.7834

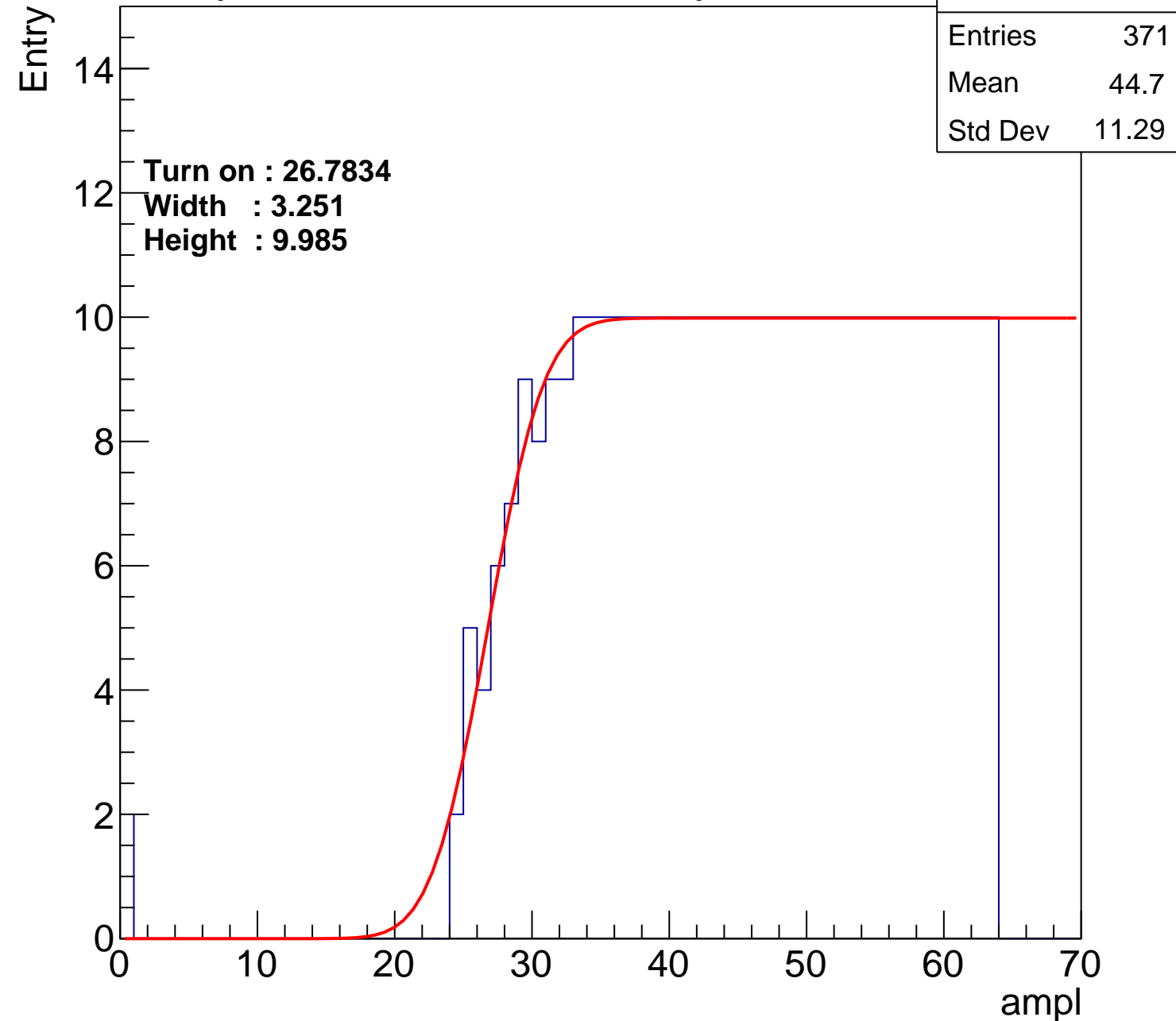
Width : 3.251

Height : 9.985

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch12

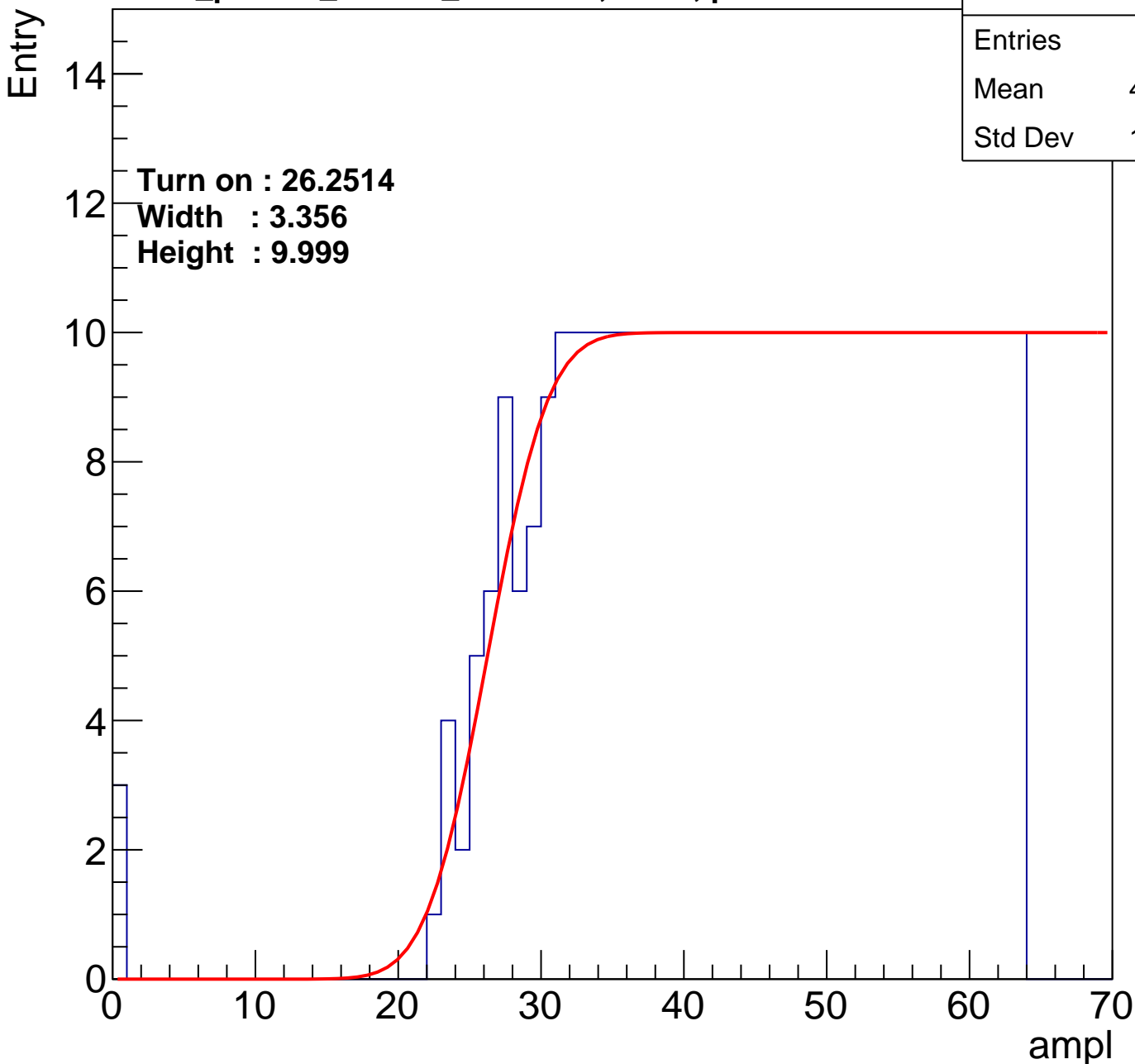
calib_packv5_042523_0143.root, FC#0, port D2

Entries	382
Mean	44.08
Std Dev	11.78

Turn on : 26.2514

Width : 3.356

Height : 9.999



B1L101S, U14-ch13

calib_packv5_042523_0143.root, FC#0, port D2

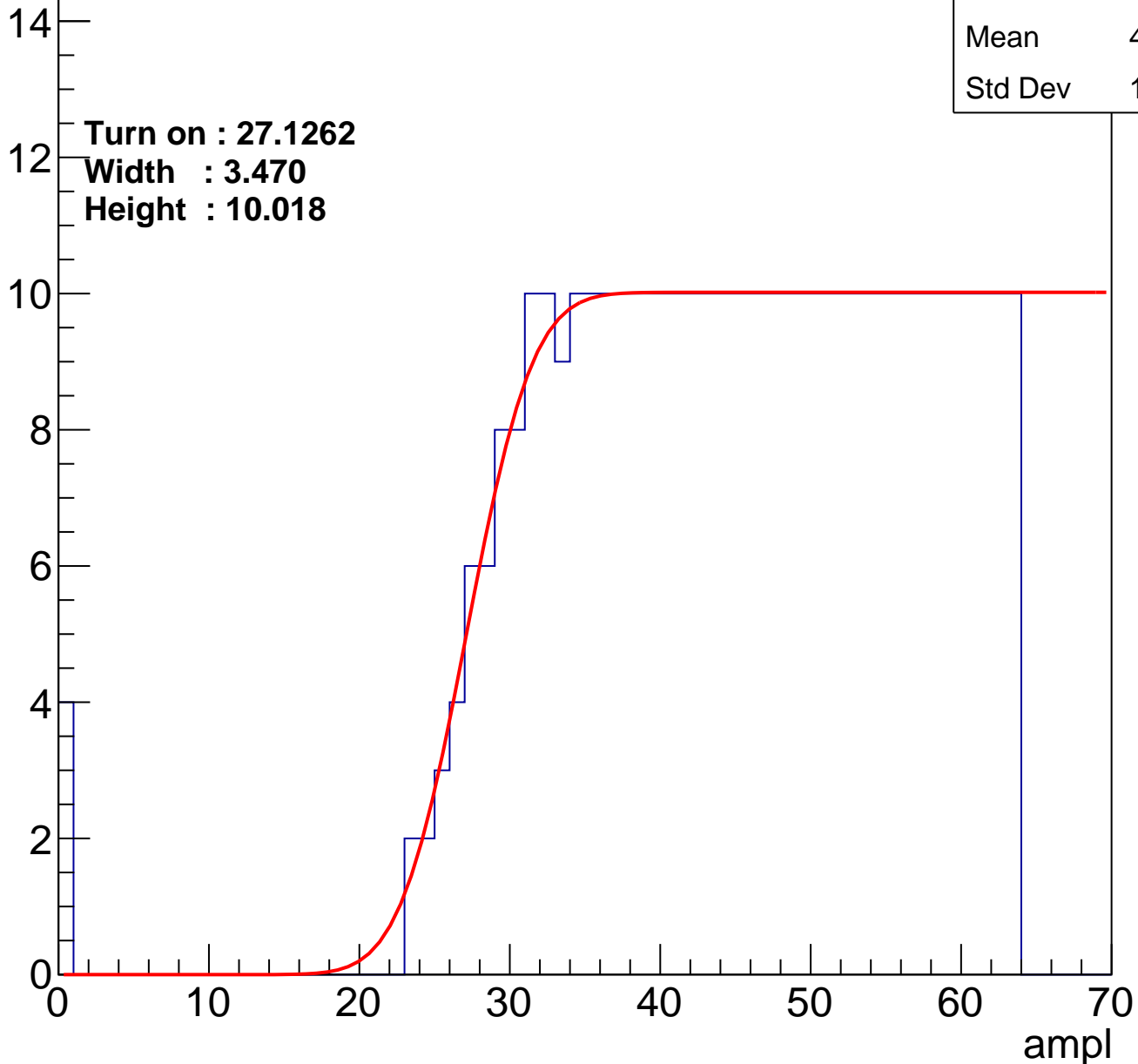
Entries	372
Mean	44.49
Std Dev	11.72

Turn on : 27.1262

Width : 3.470

Height : 10.018

Entry



B1L101S, U14-ch14

calib_packv5_042523_0143.root, FC#0, port D2

Entries	370
Mean	44.75
Std Dev	11.27

Turn on : 27.2627

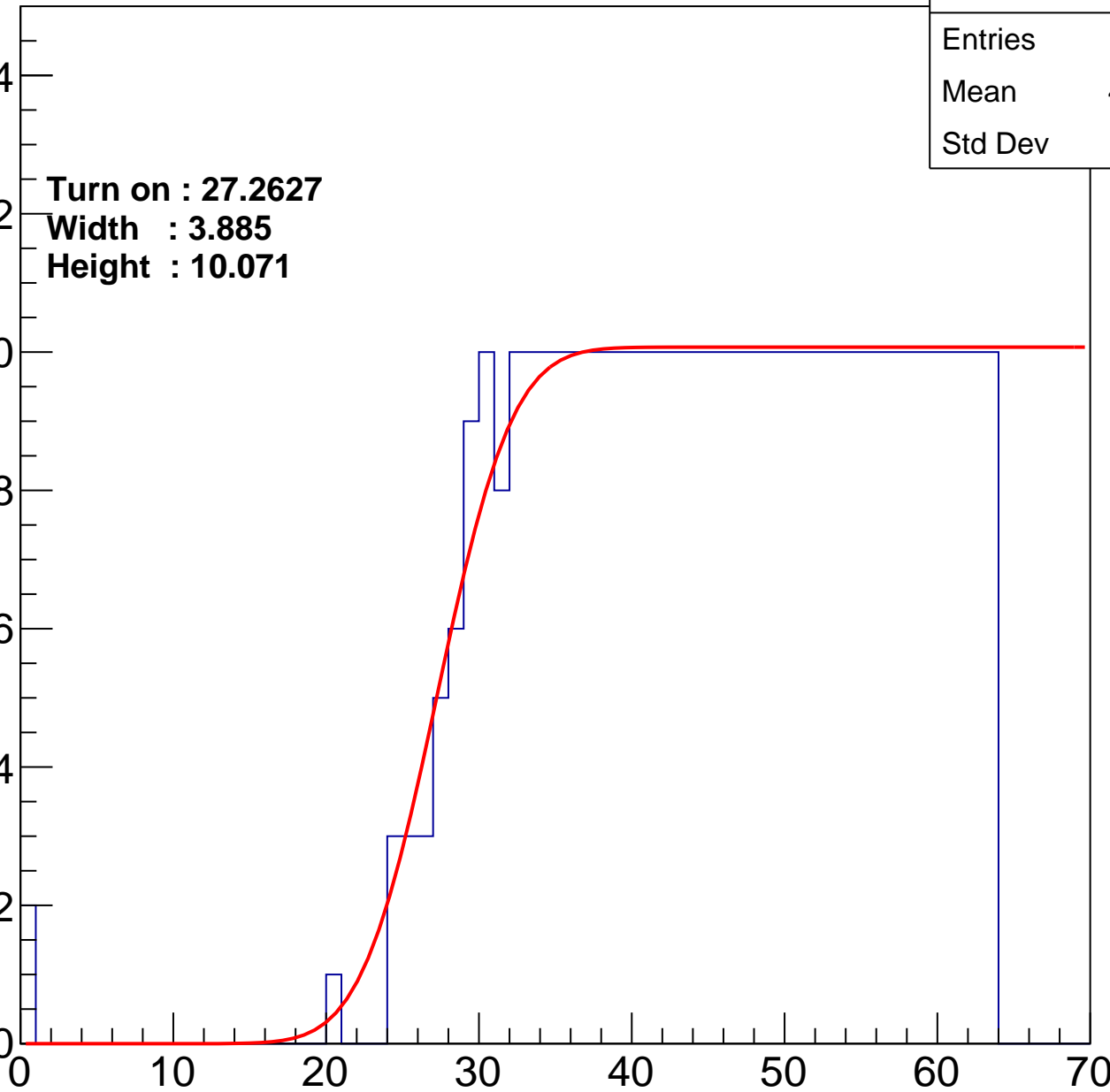
Width : 3.885

Height : 10.071

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch15

calib_packv5_042523_0143.root, FC#0, port D2

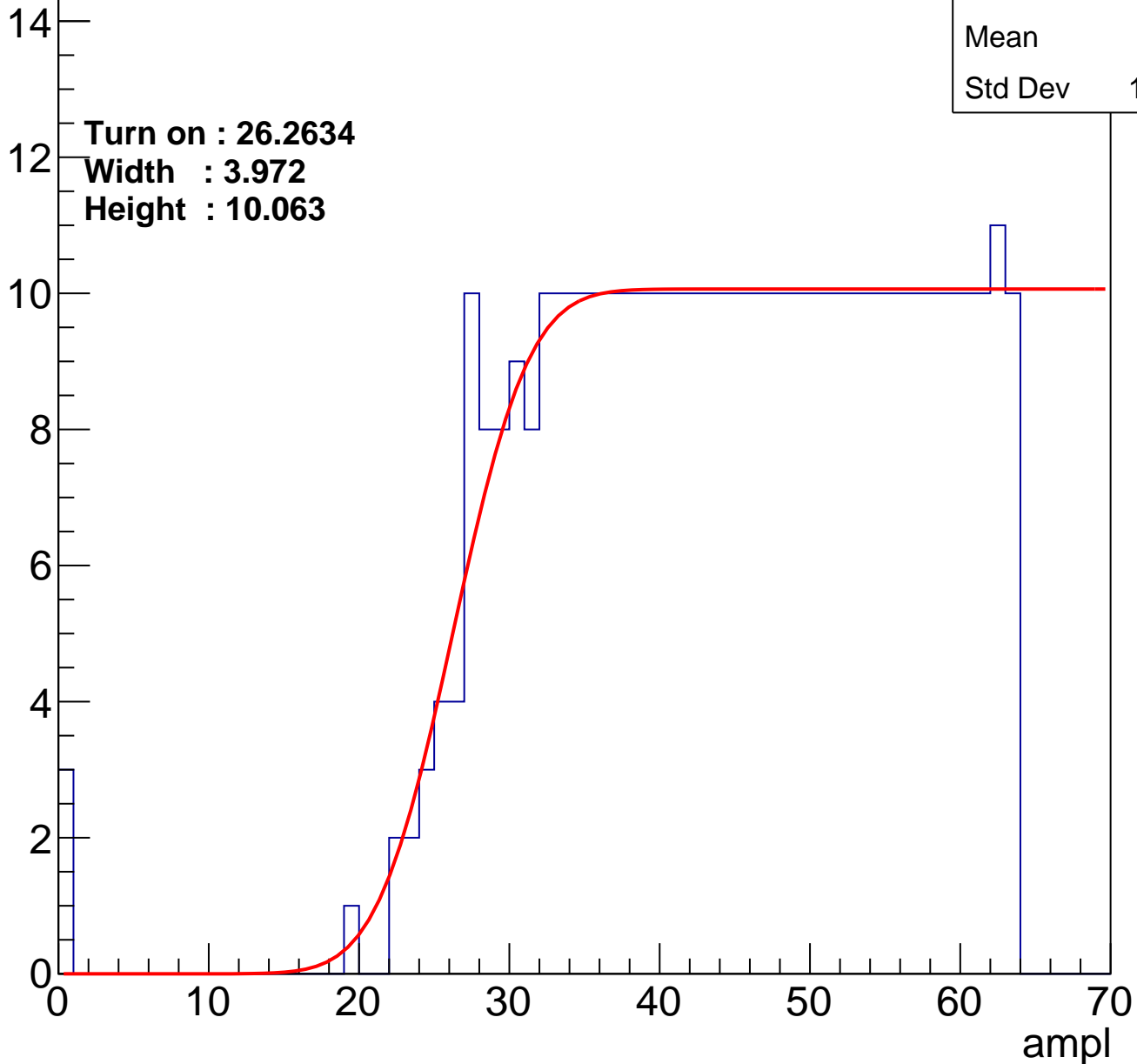
Entries	383
Mean	44.1
Std Dev	11.83

Turn on : 26.2634

Width : 3.972

Height : 10.063

Entry



B1L101S, U14-ch16

calib_packv5_042523_0143.root, FC#0, port D2

Entries	385
Mean	43.91
Std Dev	11.96

Turn on : 25.9784

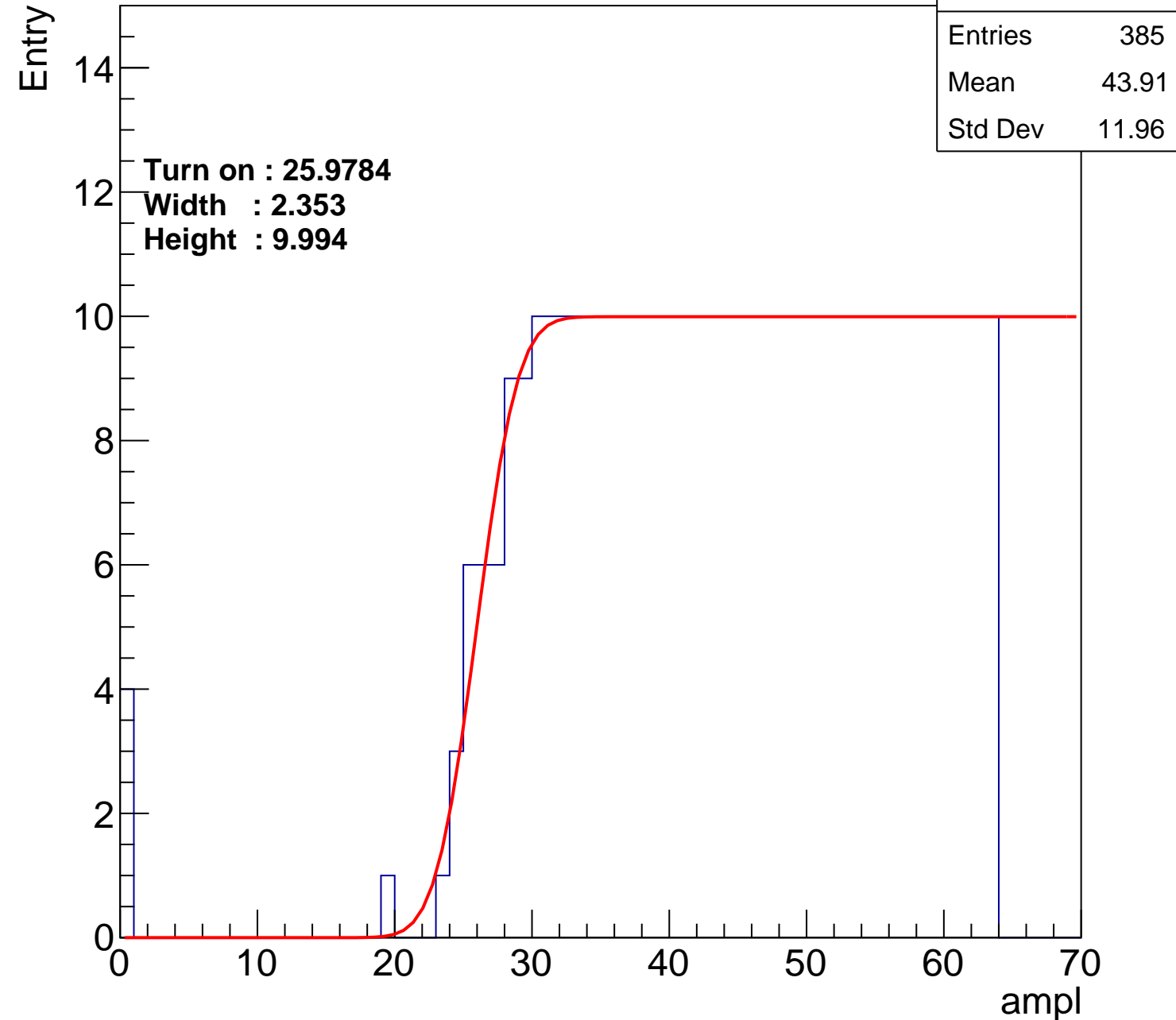
Width : 2.353

Height : 9.994

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch17

calib_packv5_042523_0143.root, FC#0, port D2

Entries	372
Mean	44.69
Std Dev	11.25

Turn on : 27.2146

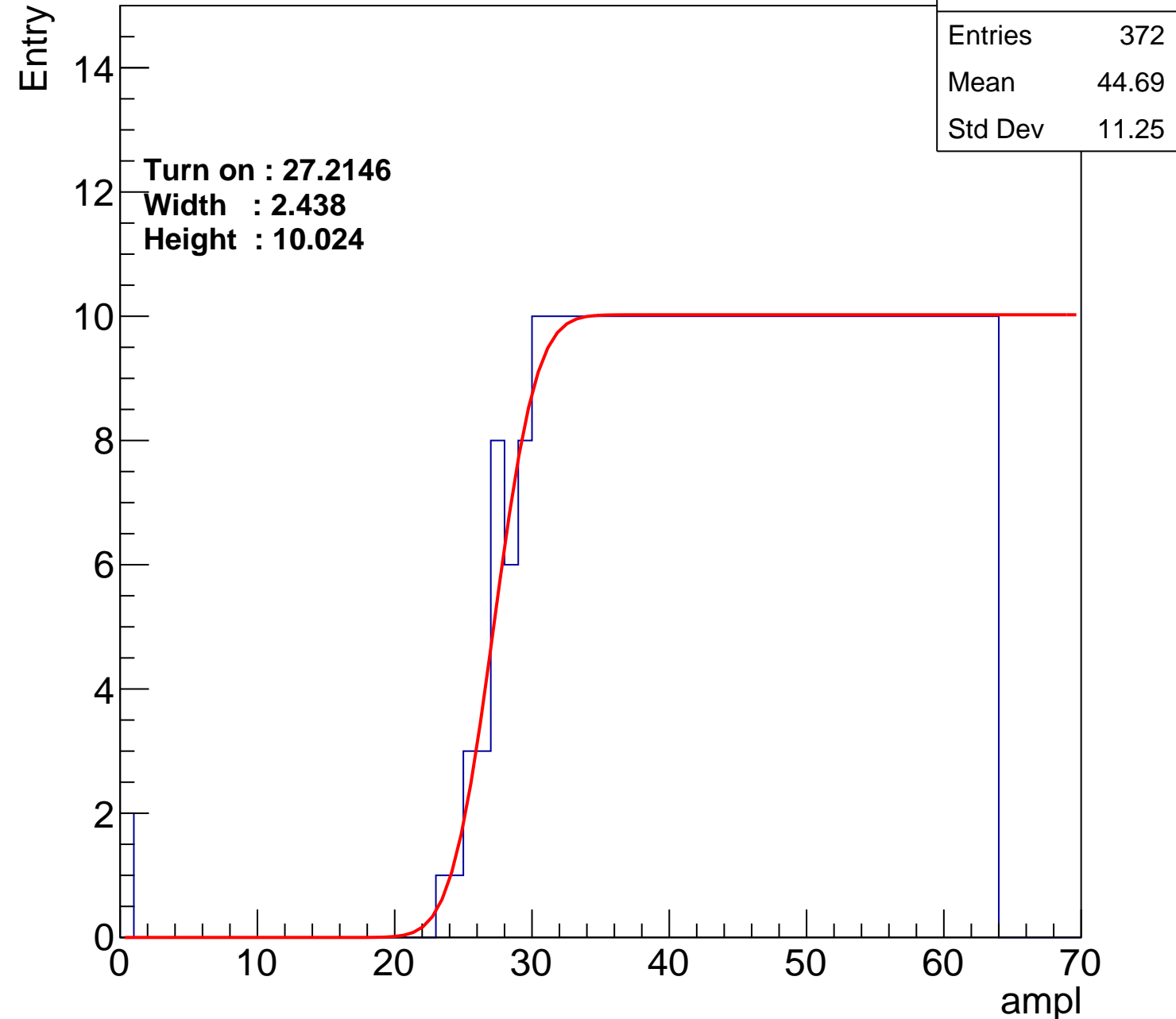
Width : 2.438

Height : 10.024

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch18

calib_packv5_042523_0143.root, FC#0, port D2

Entries	378
Mean	44.15
Std Dev	12.02

Turn on : 26.7406

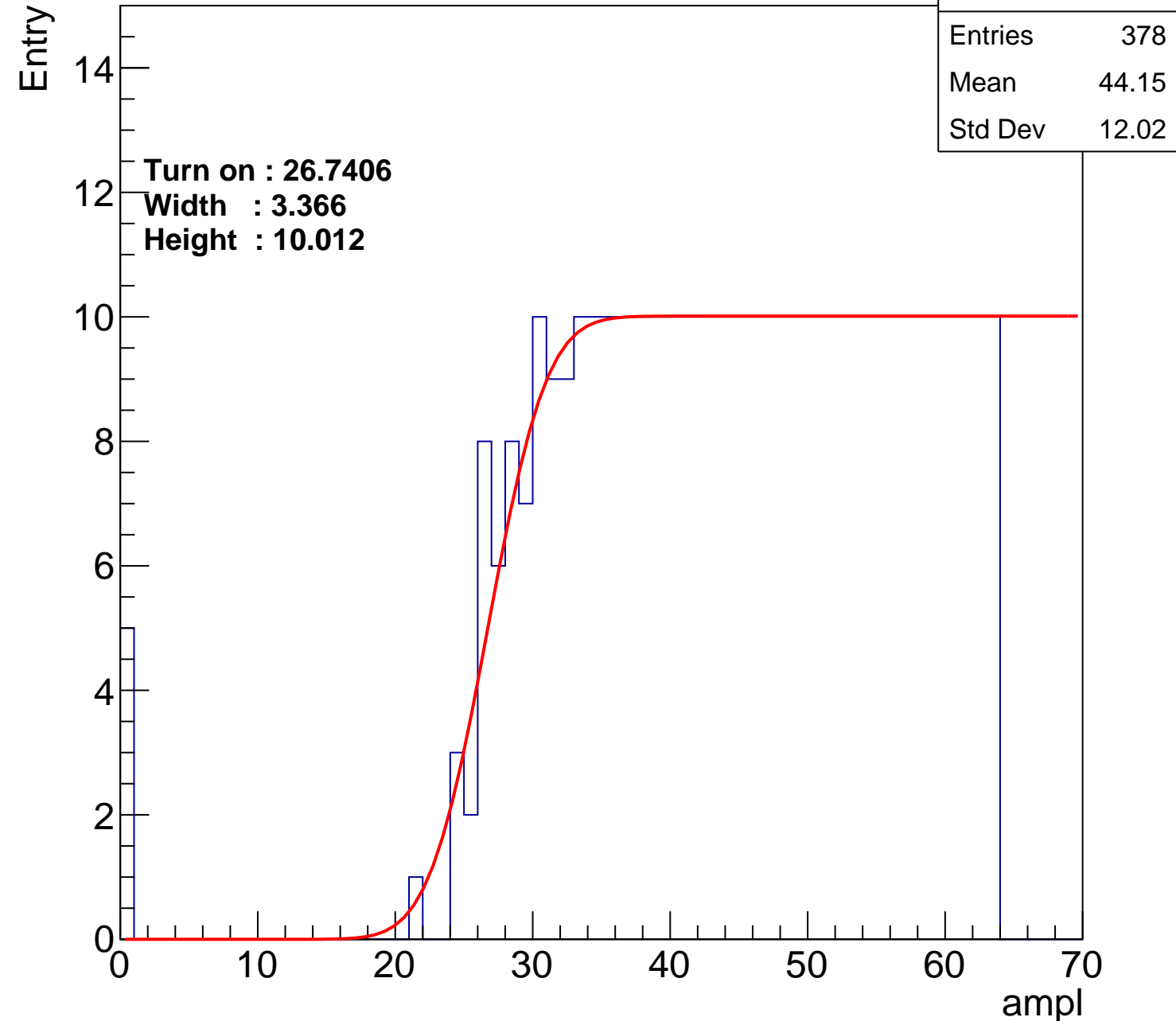
Width : 3.366

Height : 10.012

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch19

calib_packv5_042523_0143.root, FC#0, port D2

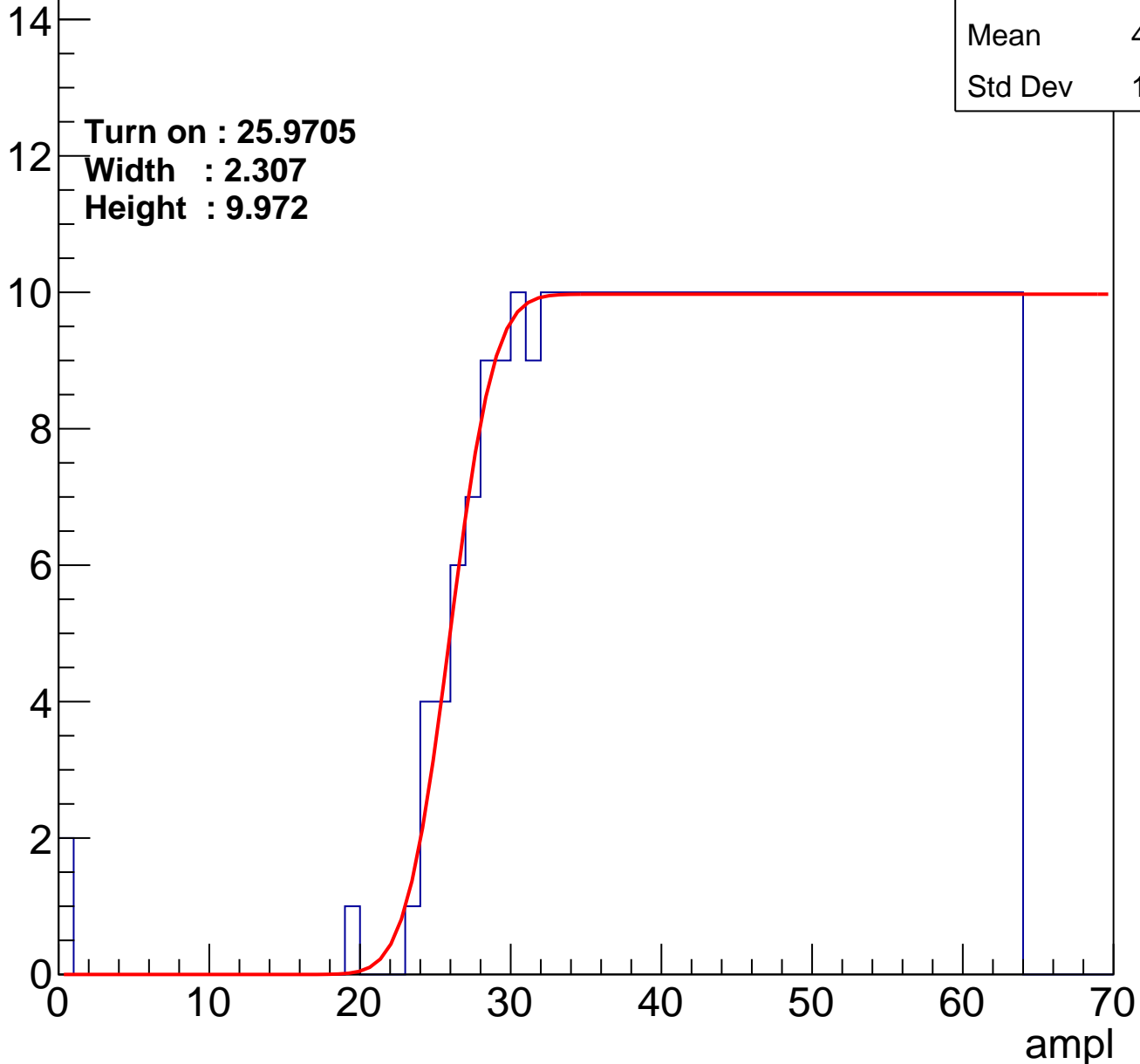
Entries	382
Mean	44.18
Std Dev	11.55

Turn on : 25.9705

Width : 2.307

Height : 9.972

Entry



B1L101S, U14-ch20

calib_packv5_042523_0143.root, FC#0, port D2

Entries	349
Mean	45.9
Std Dev	10.44

Turn on : 29.4537

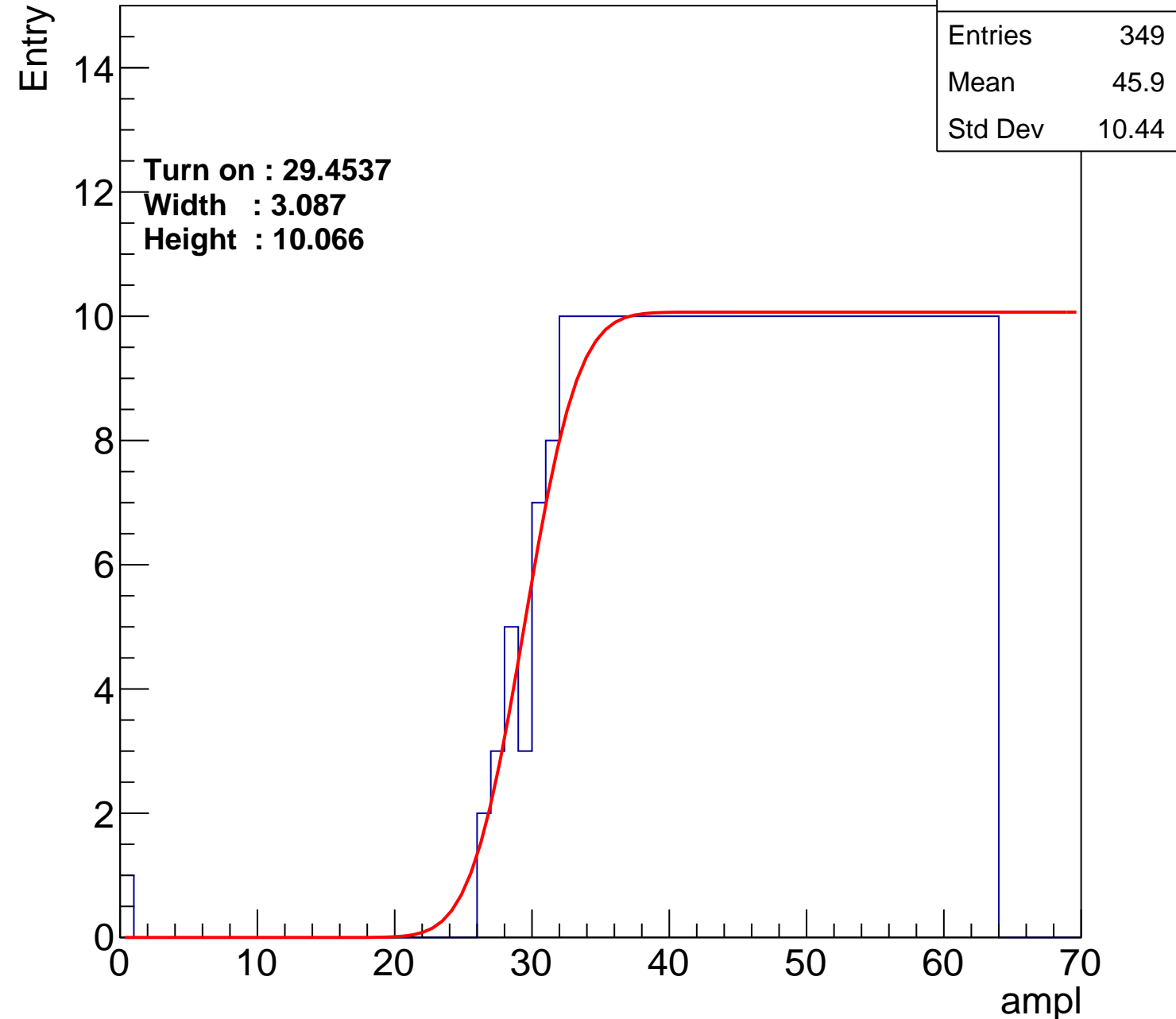
Width : 3.087

Height : 10.066

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch21

calib_packv5_042523_0143.root, FC#0, port D2

Entries	365
Mean	44.92
Std Dev	11.35

Turn on : 27.6859

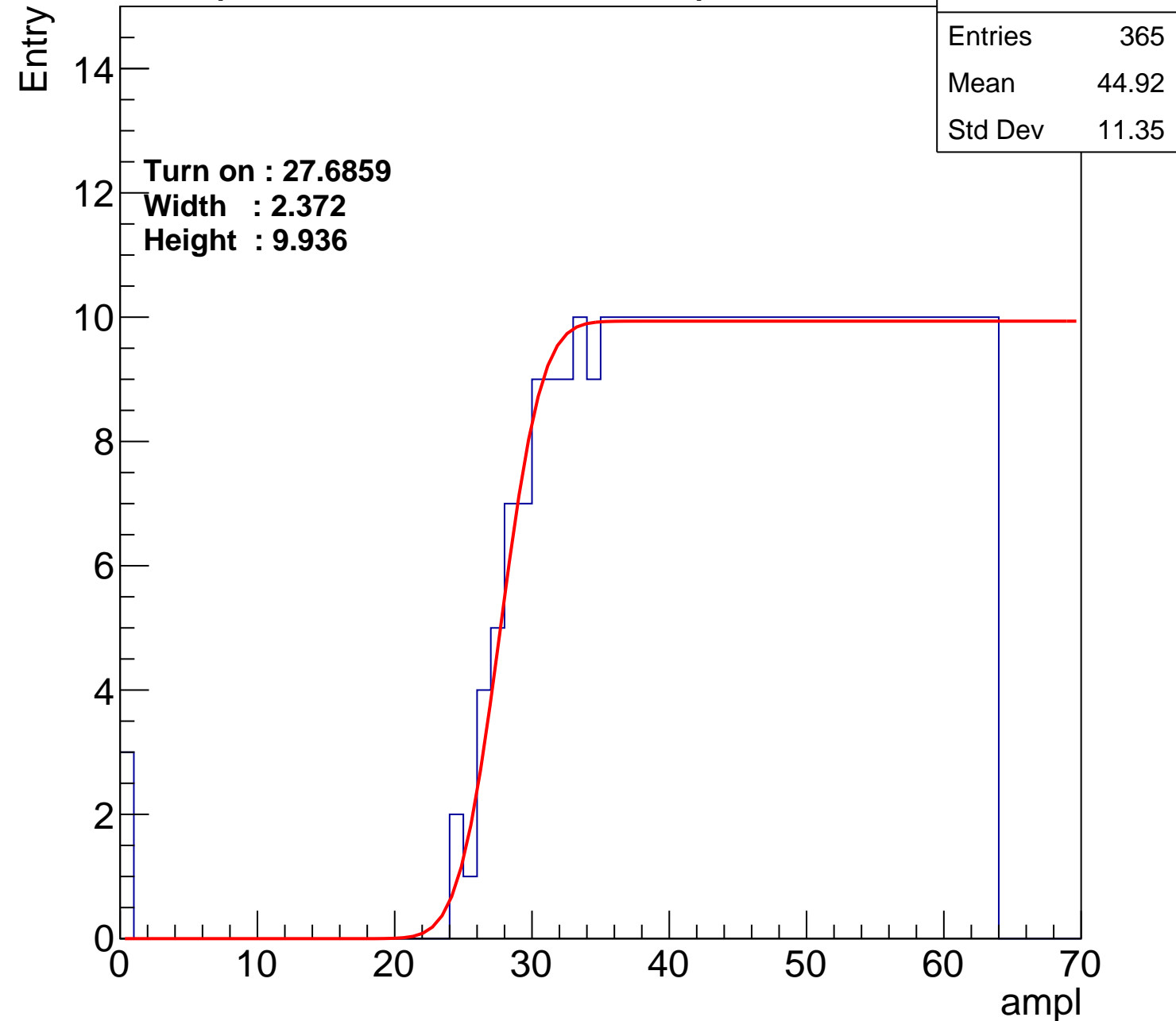
Width : 2.372

Height : 9.936

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch22

calib_packv5_042523_0143.root, FC#0, port D2

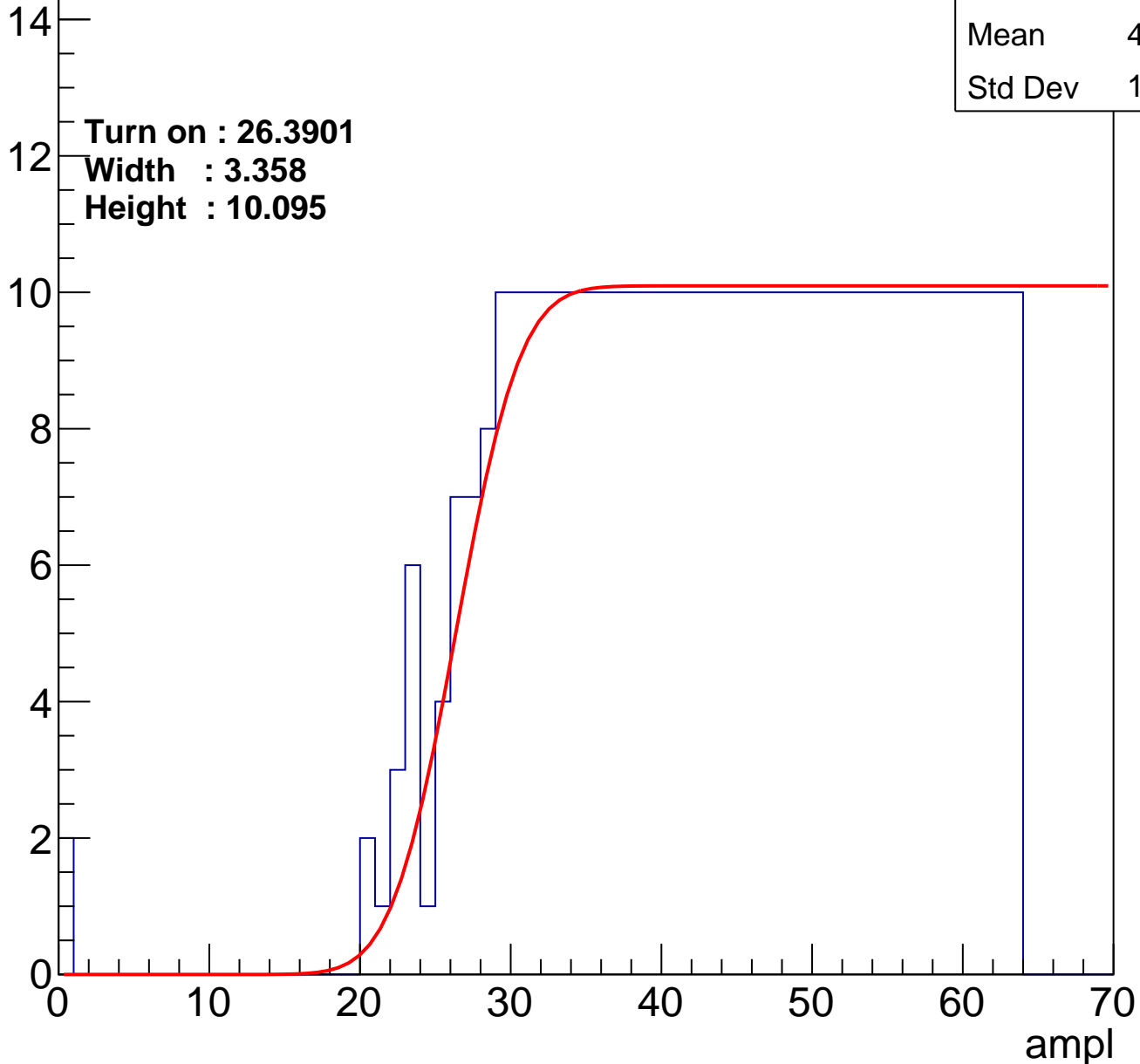
Entries	391
Mean	43.69
Std Dev	11.85

Turn on : 26.3901

Width : 3.358

Height : 10.095

Entry



B1L101S, U14-ch23

calib_packv5_042523_0143.root, FC#0, port D2

Entries	393
Mean	43.58
Std Dev	11.98

Turn on : 25.2871

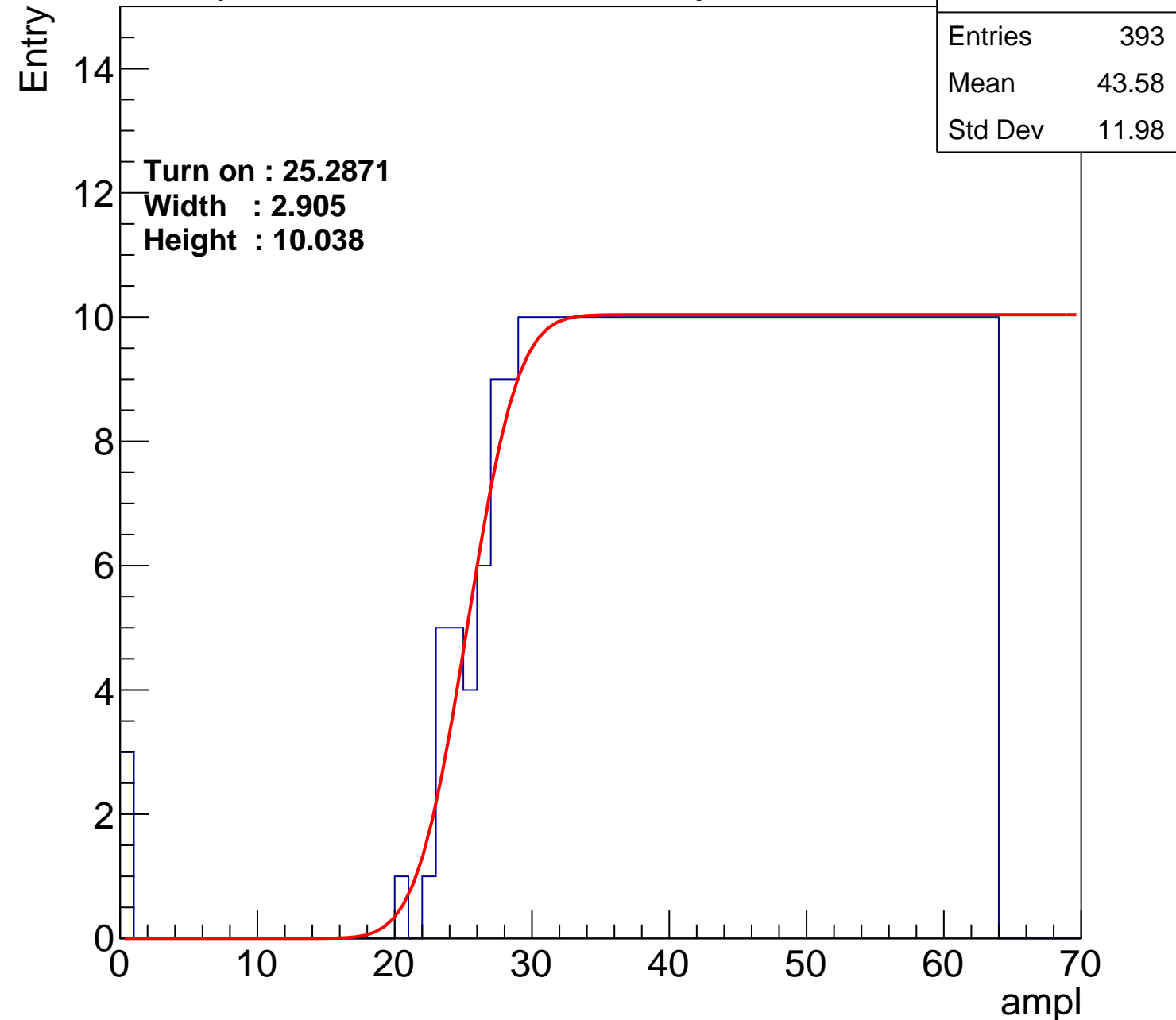
Width : 2.905

Height : 10.038

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch24

calib_packv5_042523_0143.root, FC#0, port D2

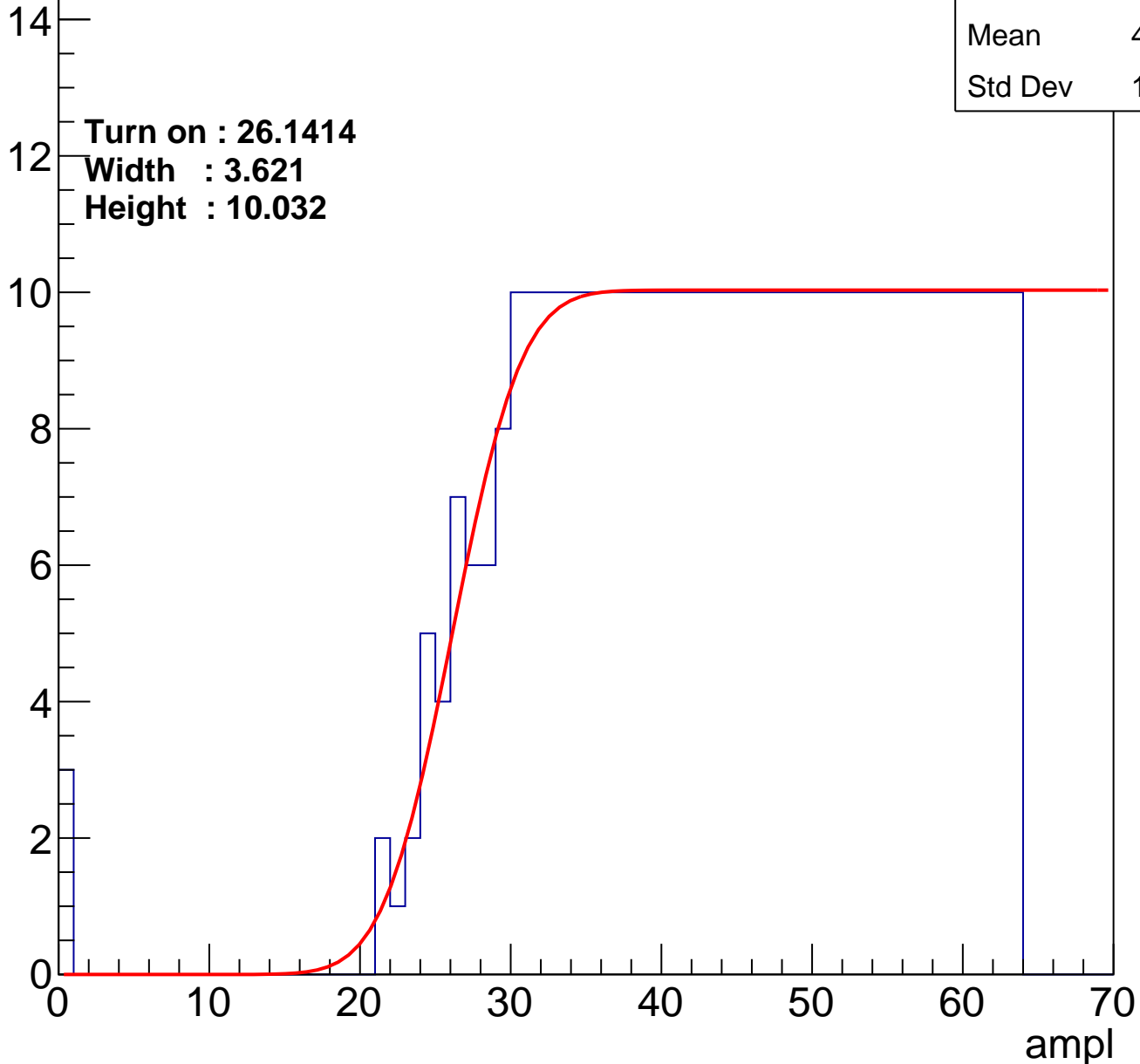
Entries	384
Mean	43.97
Std Dev	11.84

Turn on : 26.1414

Width : 3.621

Height : 10.032

Entry



B1L101S, U14-ch25

calib_packv5_042523_0143.root, FC#0, port D2

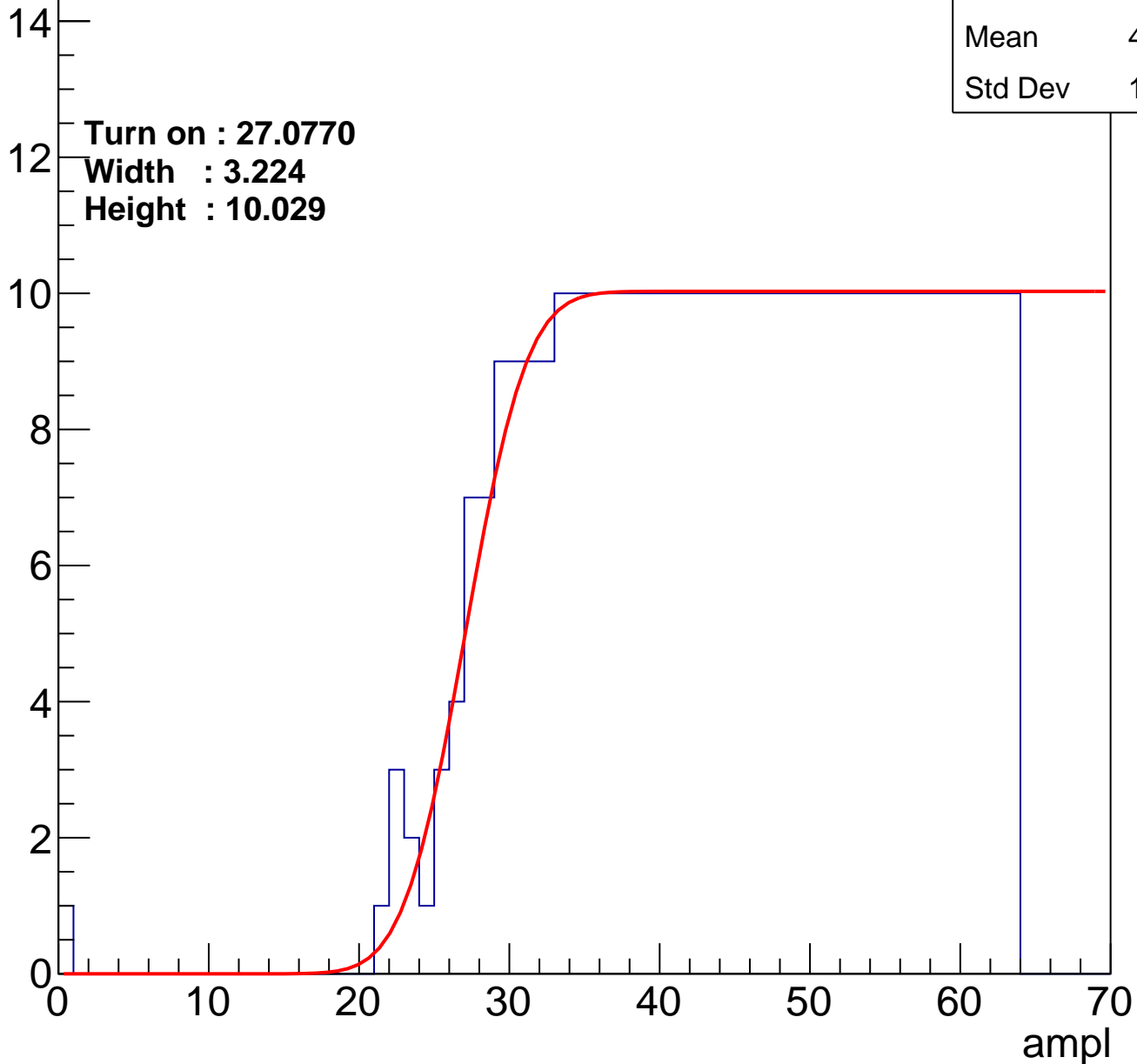
Entries	375
Mean	44.53
Std Dev	11.27

Turn on : 27.0770

Width : 3.224

Height : 10.029

Entry



B1L101S, U14-ch26

calib_packv5_042523_0143.root, FC#0, port D2

Entries	363
Mean	44.8
Std Dev	11.9

Turn on : 27.6279

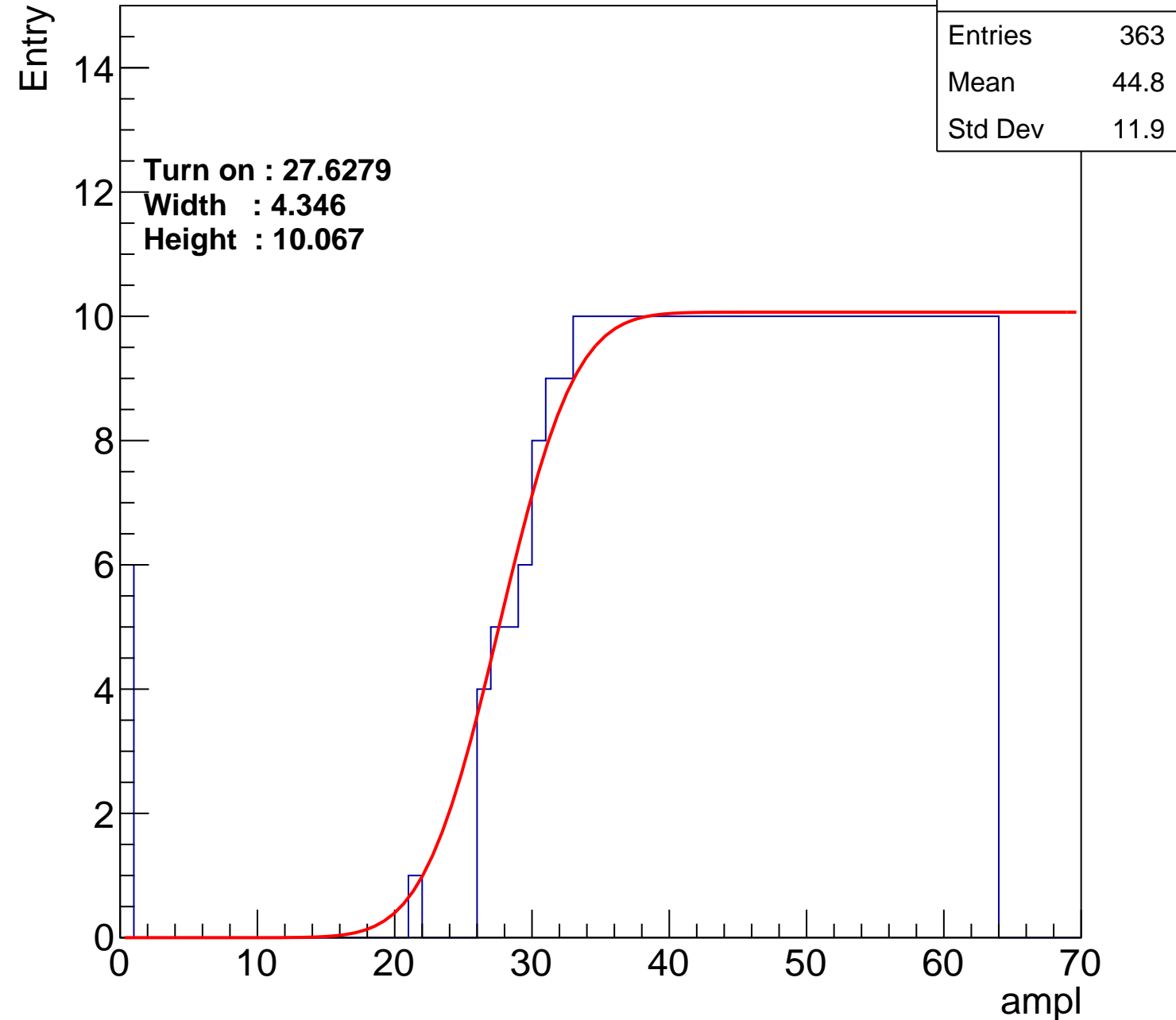
Width : 4.346

Height : 10.067

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch27

calib_packv5_042523_0143.root, FC#0, port D2

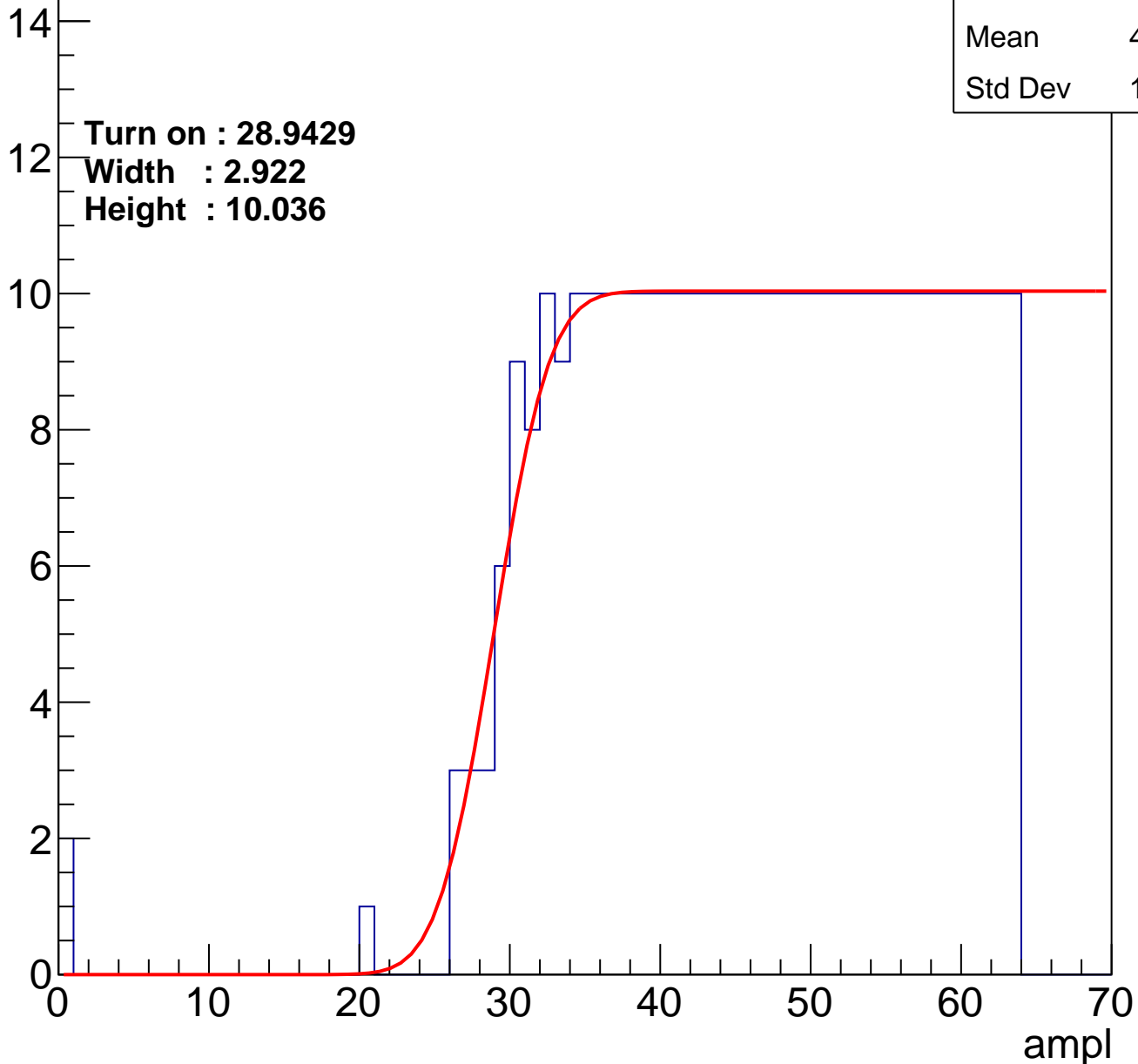
Entries	354
Mean	45.54
Std Dev	10.86

Turn on : 28.9429

Width : 2.922

Height : 10.036

Entry



B1L101S, U14-ch28

calib_packv5_042523_0143.root, FC#0, port D2

Entries	360
Mean	45.2
Std Dev	11.08

Turn on : 28.7108

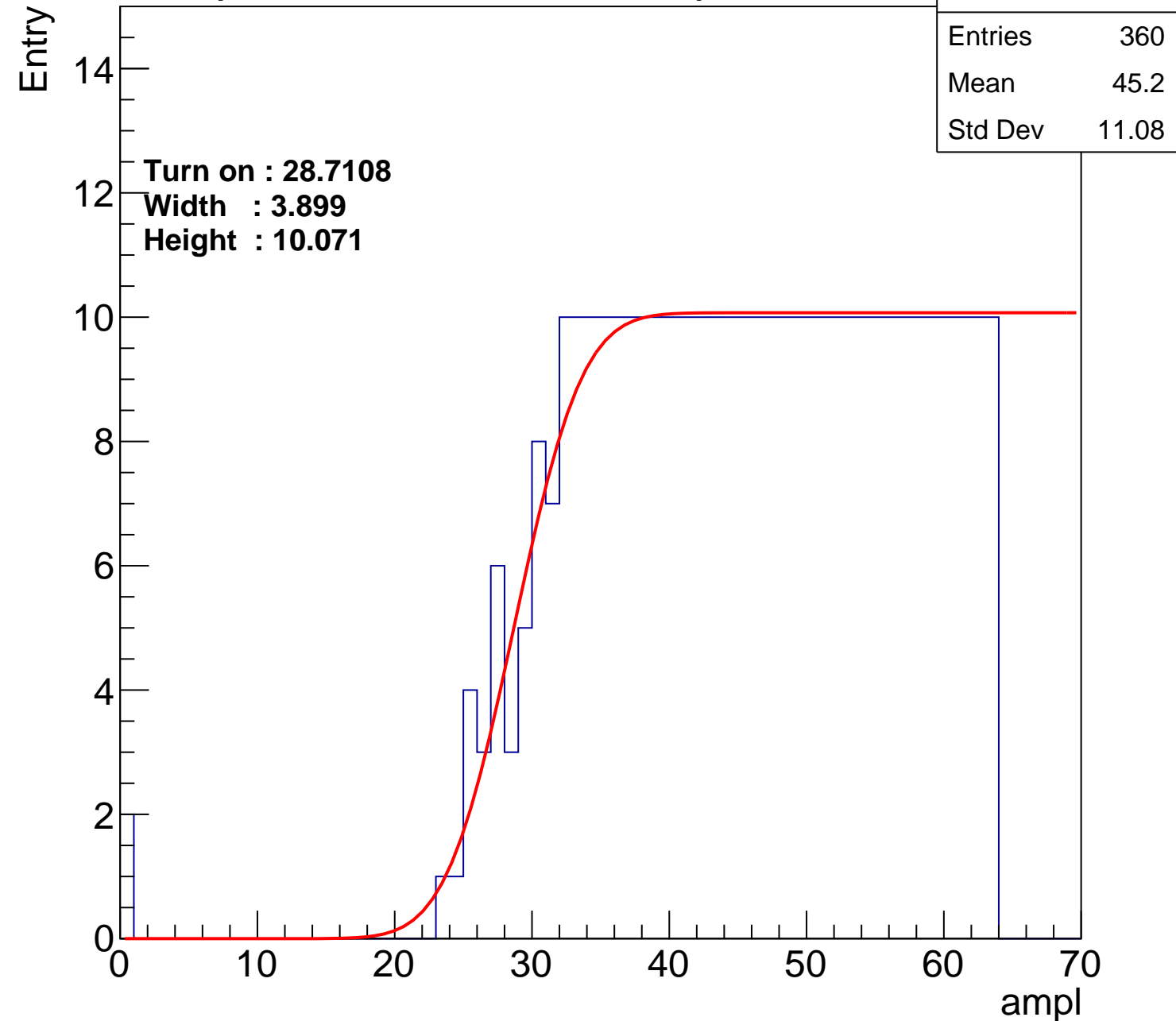
Width : 3.899

Height : 10.071

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch29

calib_packv5_042523_0143.root, FC#0, port D2

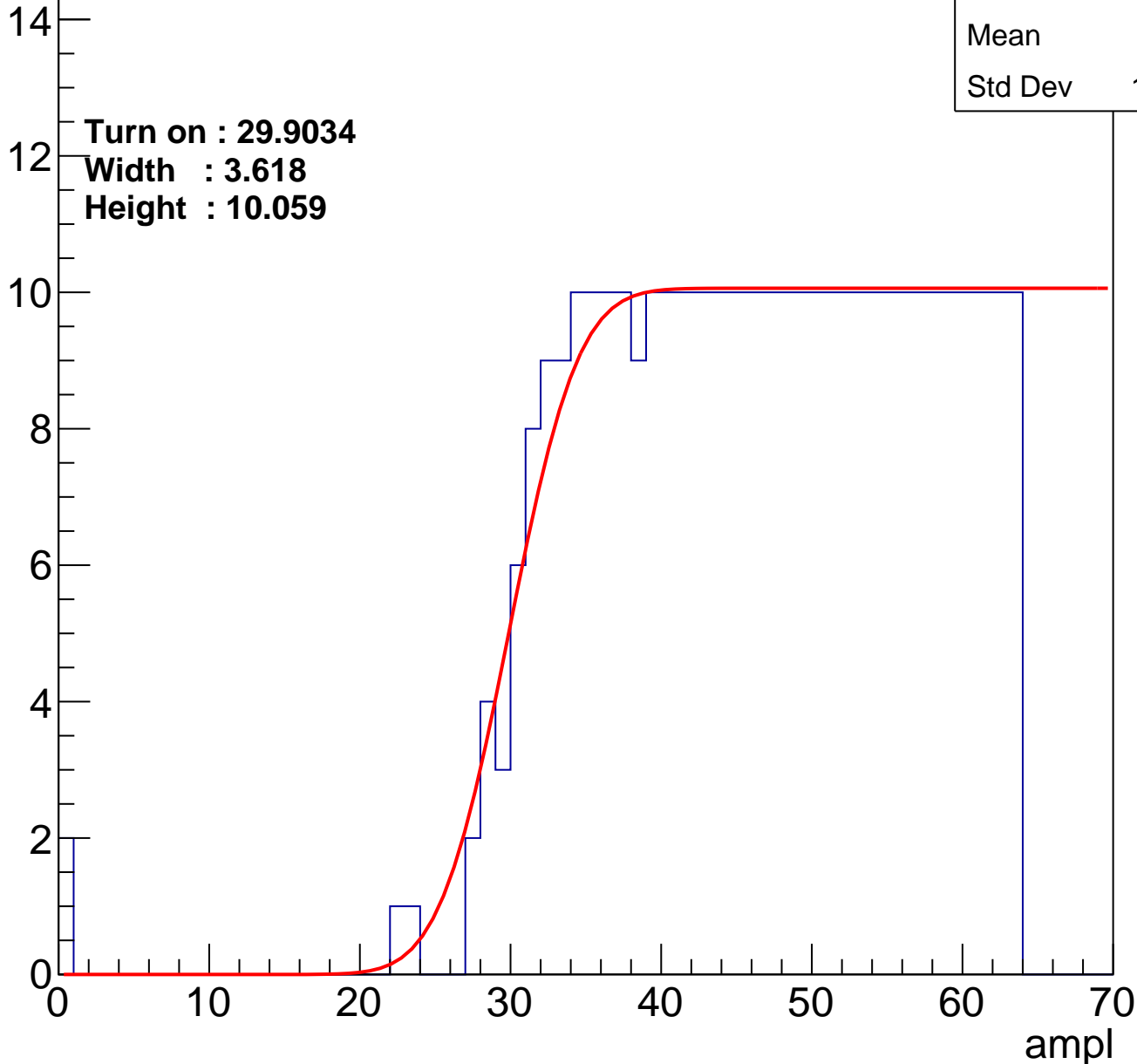
Entries	344
Mean	46
Std Dev	10.67

Turn on : 29.9034

Width : 3.618

Height : 10.059

Entry



B1L101S, U14-ch30

calib_packv5_042523_0143.root, FC#0, port D2

Entries	365
Mean	44.87
Std Dev	11.51

Turn on : 27.4058

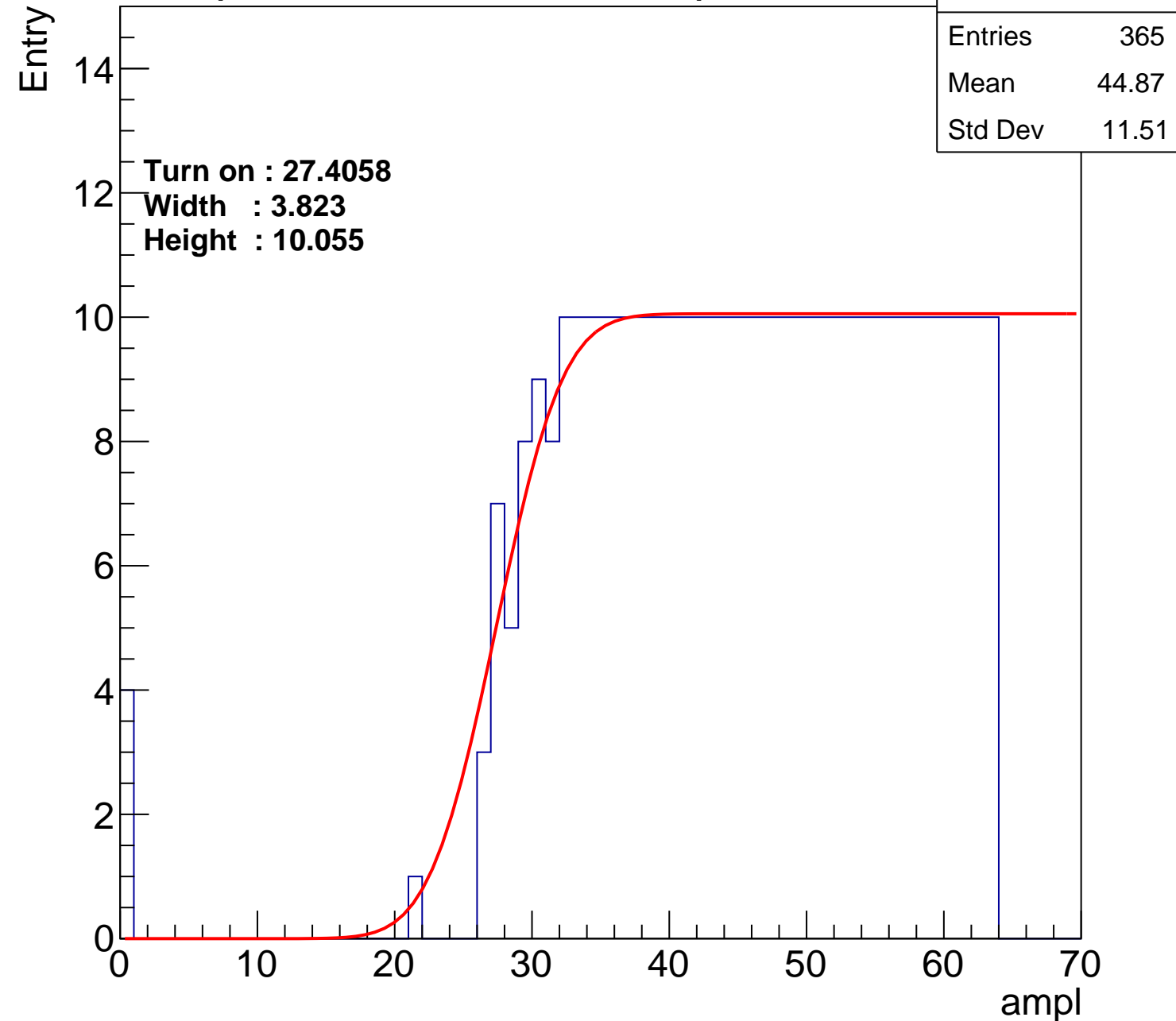
Width : 3.823

Height : 10.055

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch31

calib_packv5_042523_0143.root, FC#0, port D2

Entries	393
Mean	43.26
Std Dev	12.73

Turn on : 25.9455

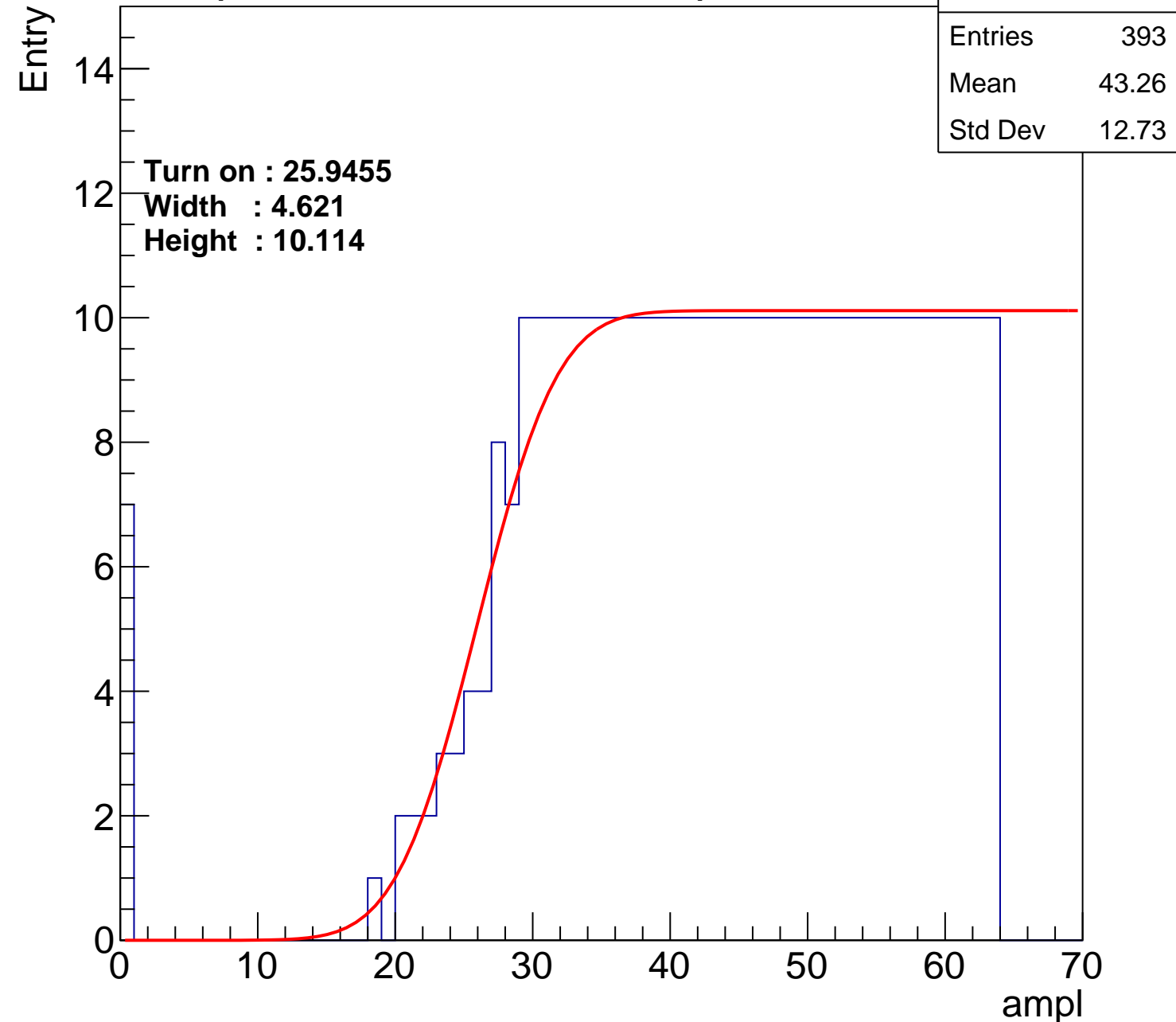
Width : 4.621

Height : 10.114

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch32

calib_packv5_042523_0143.root, FC#0, port D2

Entries	386
Mean	43.7
Std Dev	12.35

Turn on : 26.2656

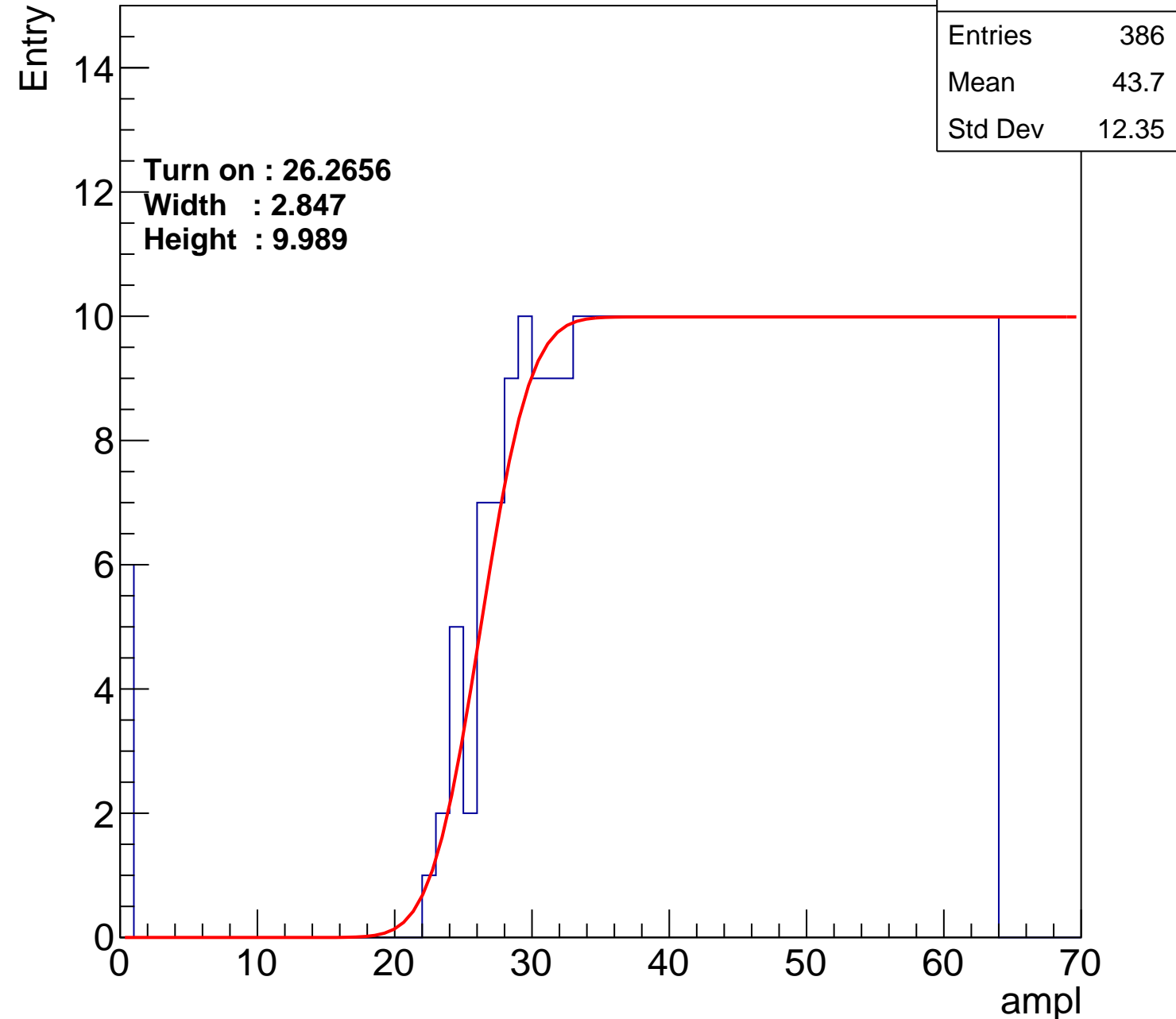
Width : 2.847

Height : 9.989

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch33

calib_packv5_042523_0143.root, FC#0, port D2

Entries	381
Mean	44.19
Std Dev	11.57

Turn on : 26.6175

Width : 3.024

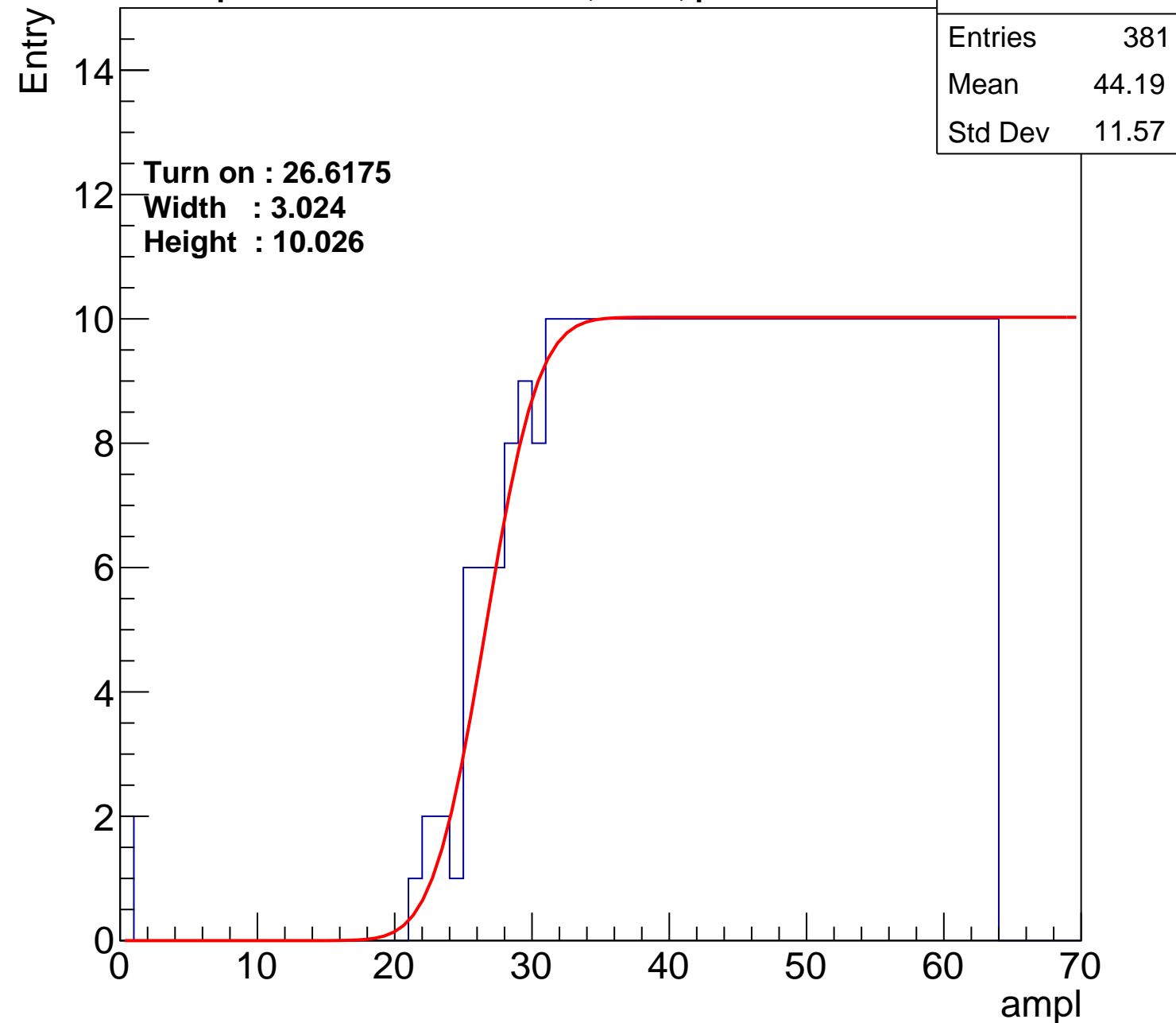
Height : 10.026

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L101S, U14-ch34

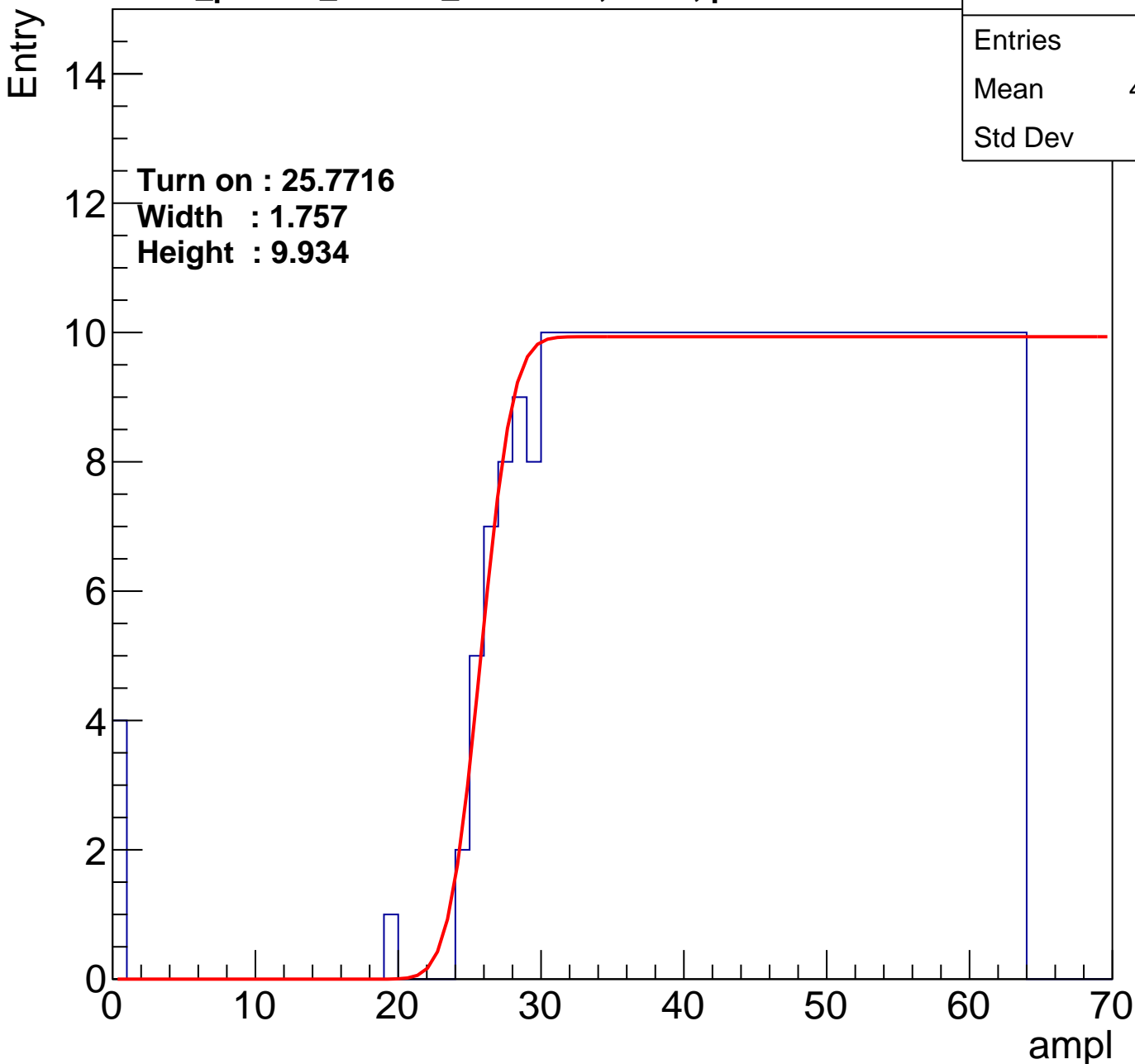
calib_packv5_042523_0143.root, FC#0, port D2

Entries	384
Mean	43.97
Std Dev	11.91

Turn on : 25.7716

Width : 1.757

Height : 9.934



B1L101S, U14-ch35

calib_packv5_042523_0143.root, FC#0, port D2

Entries	374
Mean	44.36
Std Dev	11.91

Turn on : 27.1356

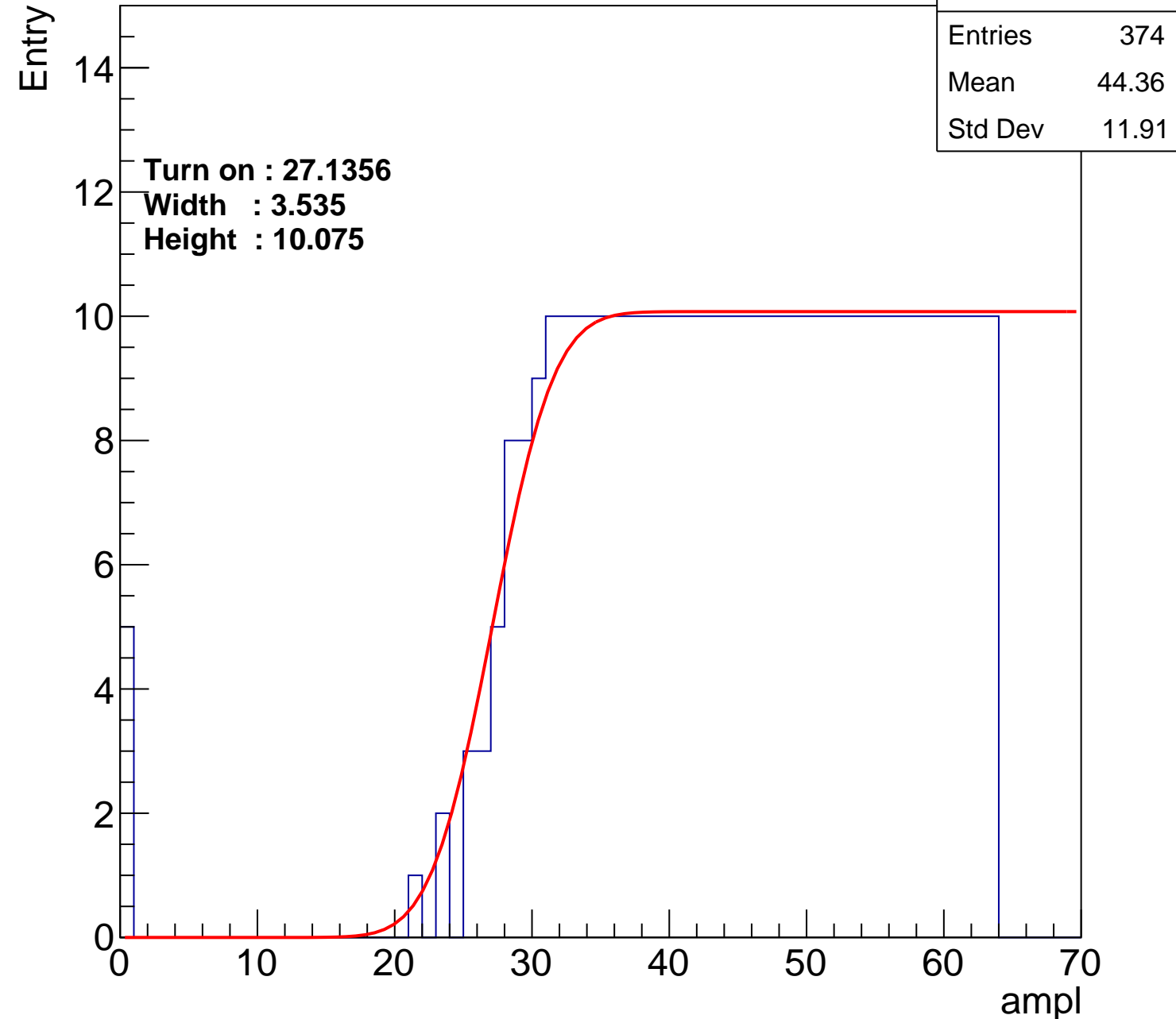
Width : 3.535

Height : 10.075

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch36

calib_packv5_042523_0143.root, FC#0, port D2

Entries	361
Mean	45.19
Std Dev	10.95

Turn on : 28.3715

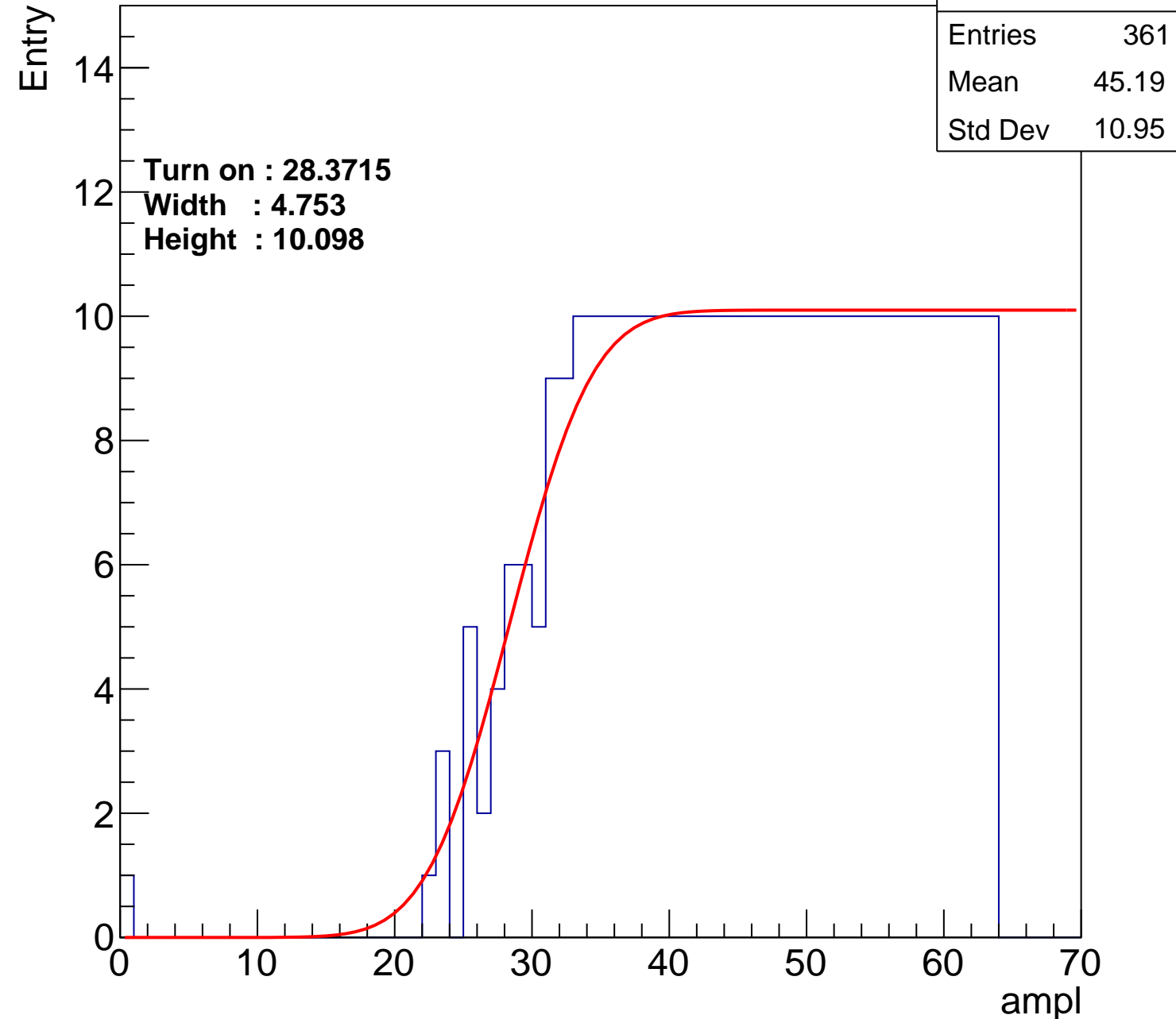
Width : 4.753

Height : 10.098

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch37

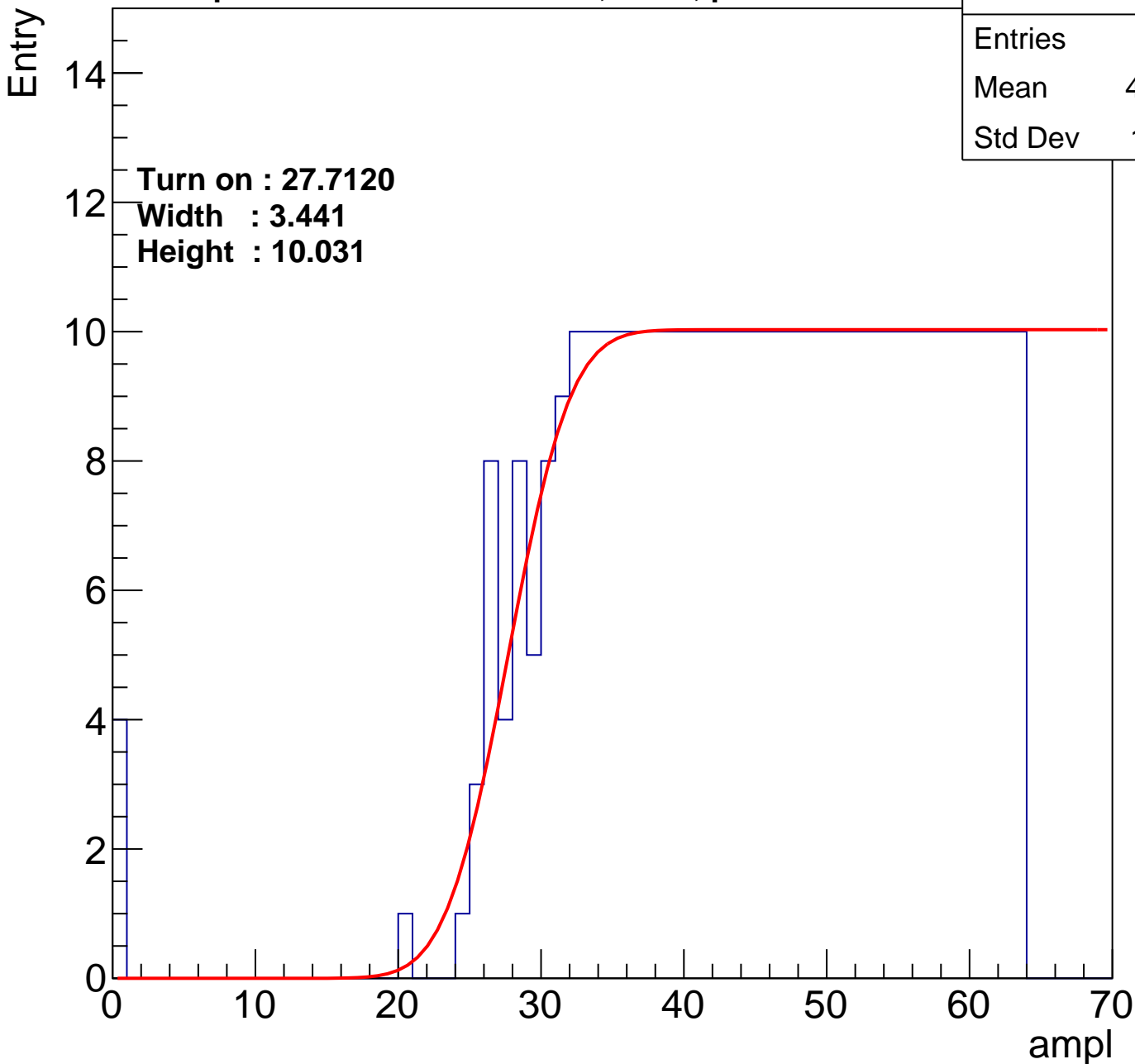
calib_packv5_042523_0143.root, FC#0, port D2

Entries	371
Mean	44.54
Std Dev	11.71

Turn on : 27.7120

Width : 3.441

Height : 10.031



B1L101S, U14-ch38

calib_packv5_042523_0143.root, FC#0, port D2

Entries	391
Mean	43.58
Std Dev	12.21

Turn on : 25.5813

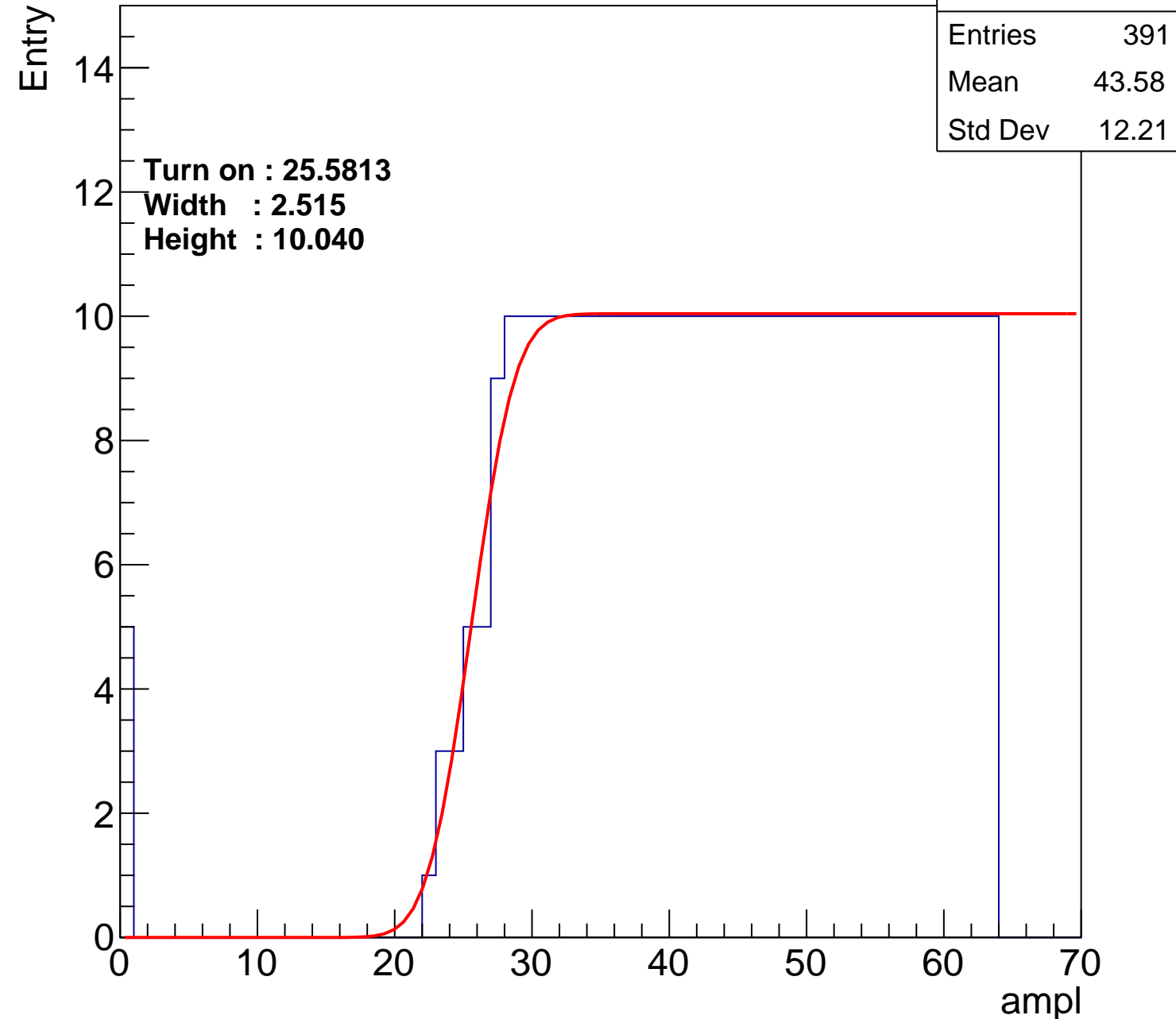
Width : 2.515

Height : 10.040

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch39

calib_packv5_042523_0143.root, FC#0, port D2

Entries	367
Mean	44.76
Std Dev	11.58

Turn on : 27.7839

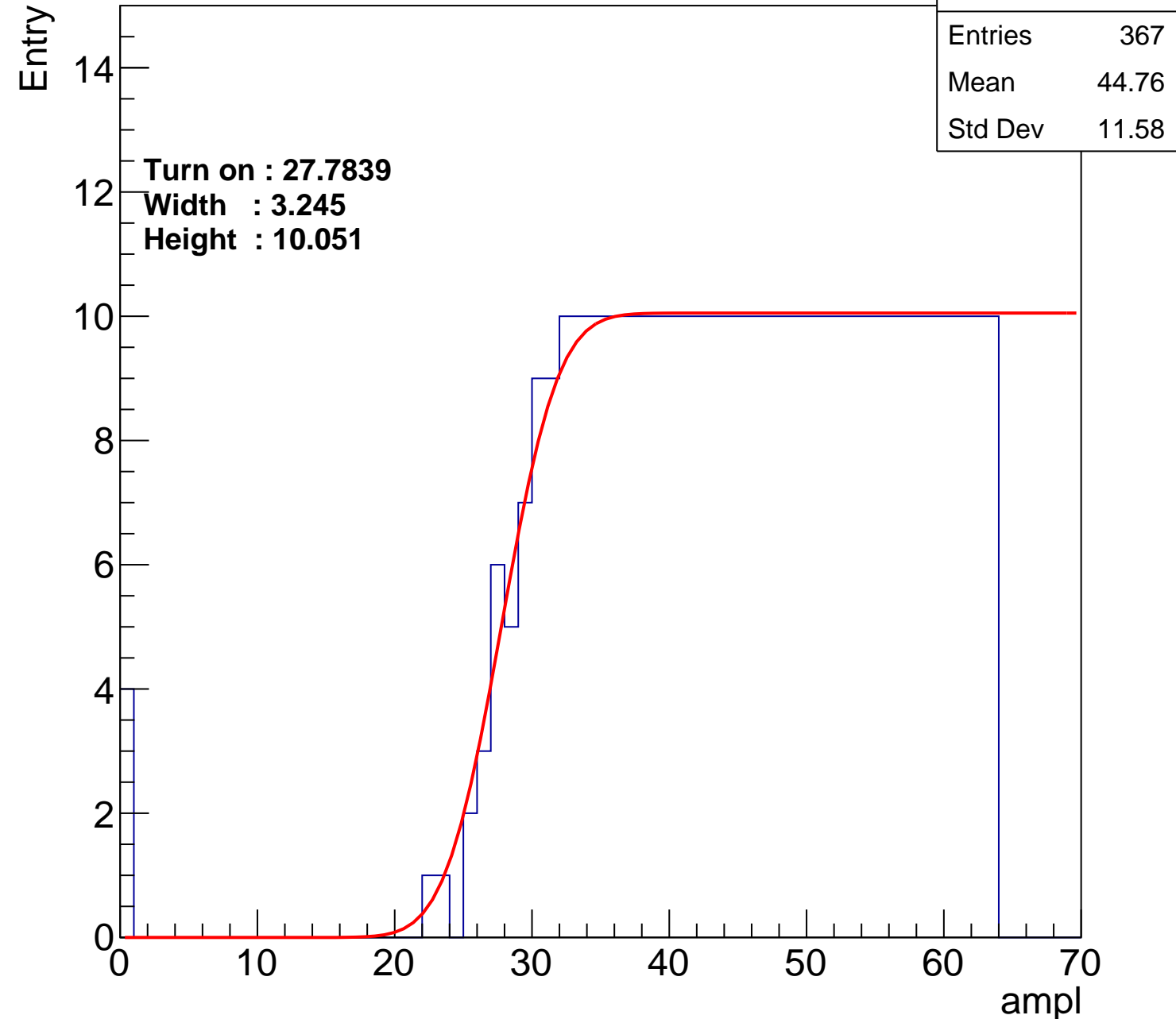
Width : 3.245

Height : 10.051

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch40

calib_packv5_042523_0143.root, FC#0, port D2

Entries	366
Mean	44.8
Std Dev	11.56

Turn on : 27.8620

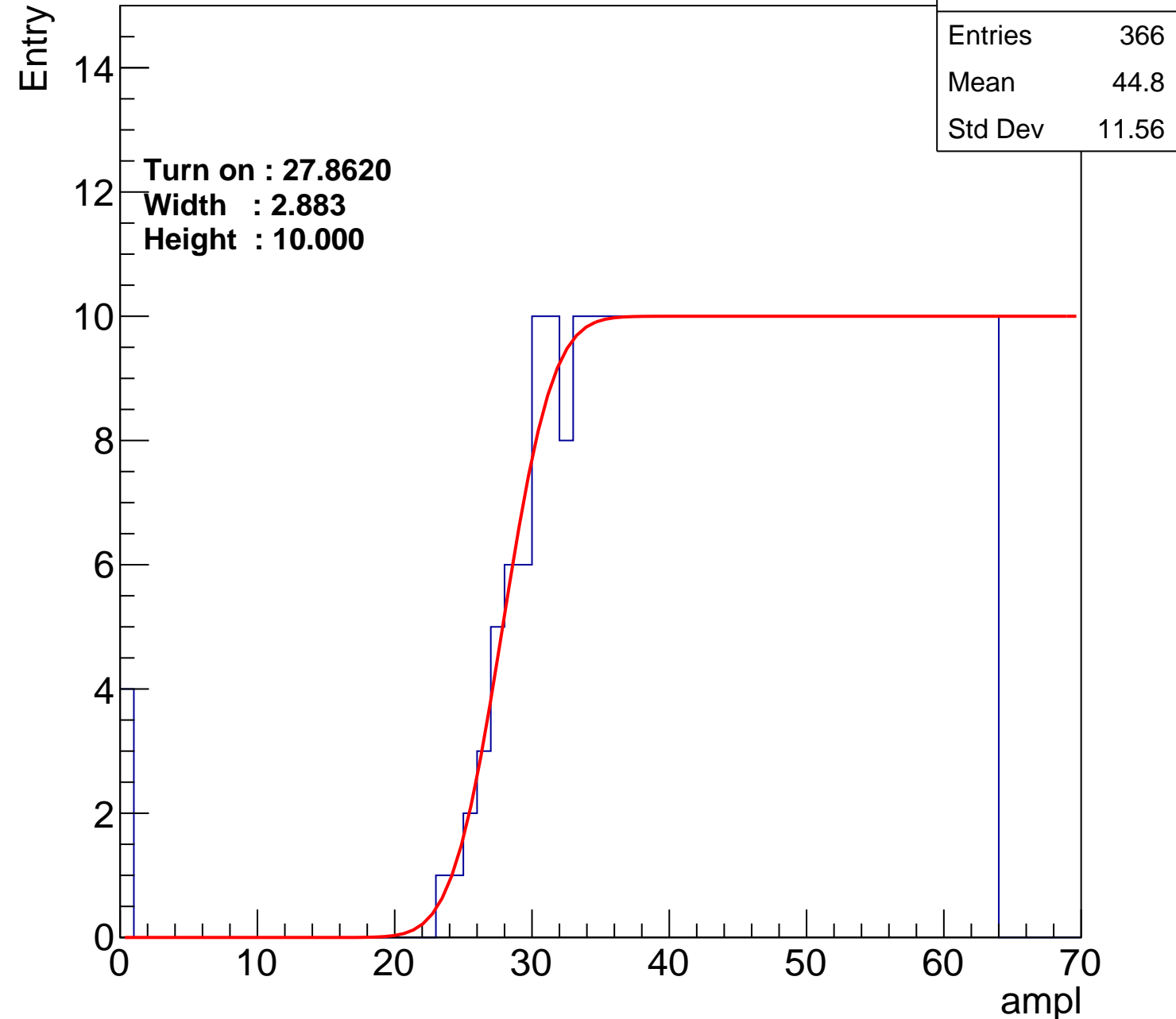
Width : 2.883

Height : 10.000

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch41

calib_packv5_042523_0143.root, FC#0, port D2

Entries	374
Mean	44.49
Std Dev	11.56

Turn on : 26.9747

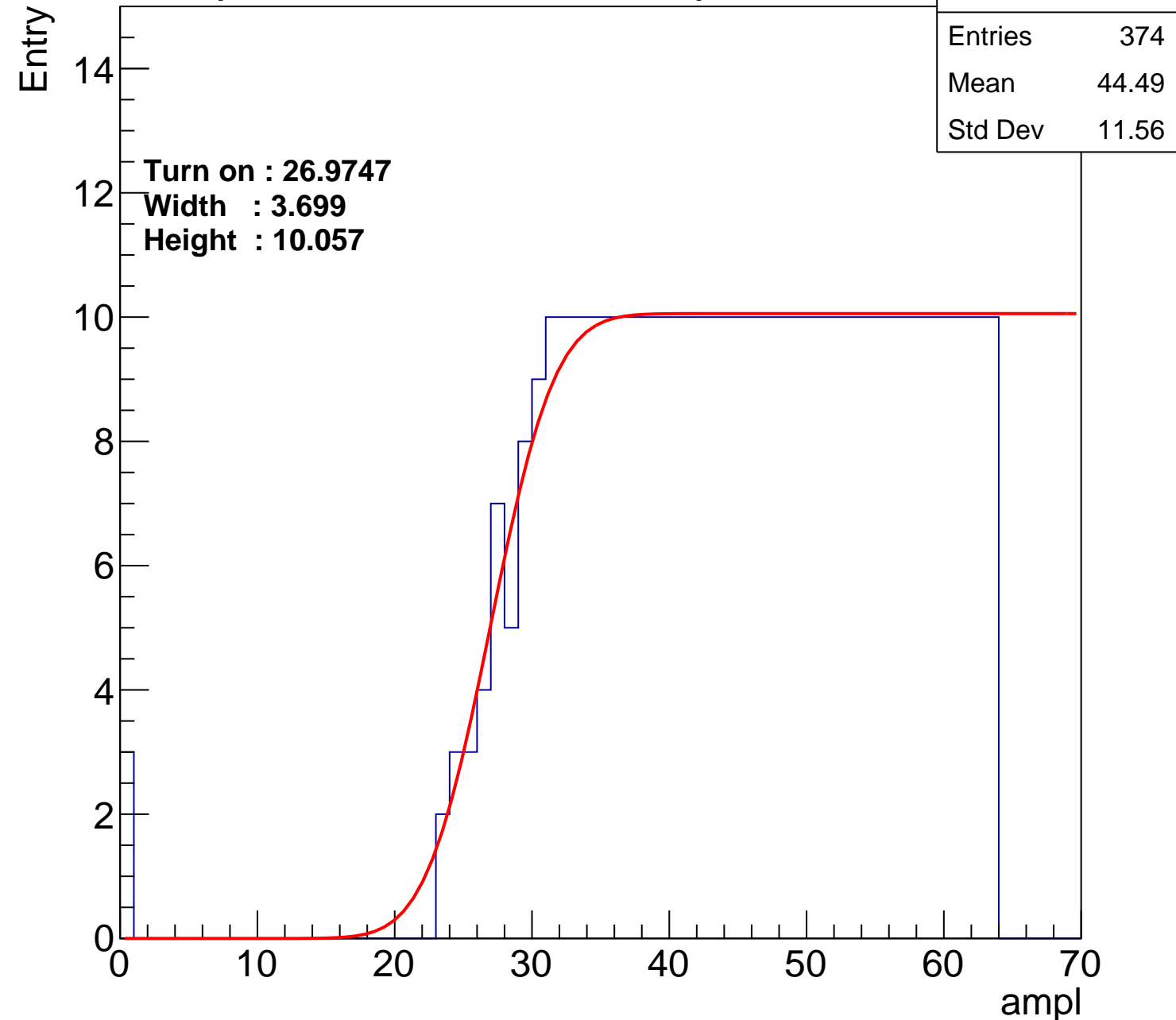
Width : 3.699

Height : 10.057

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch42

calib_packv5_042523_0143.root, FC#0, port D2

Entries	387
Mean	43.93
Std Dev	11.67

Turn on : 25.2997

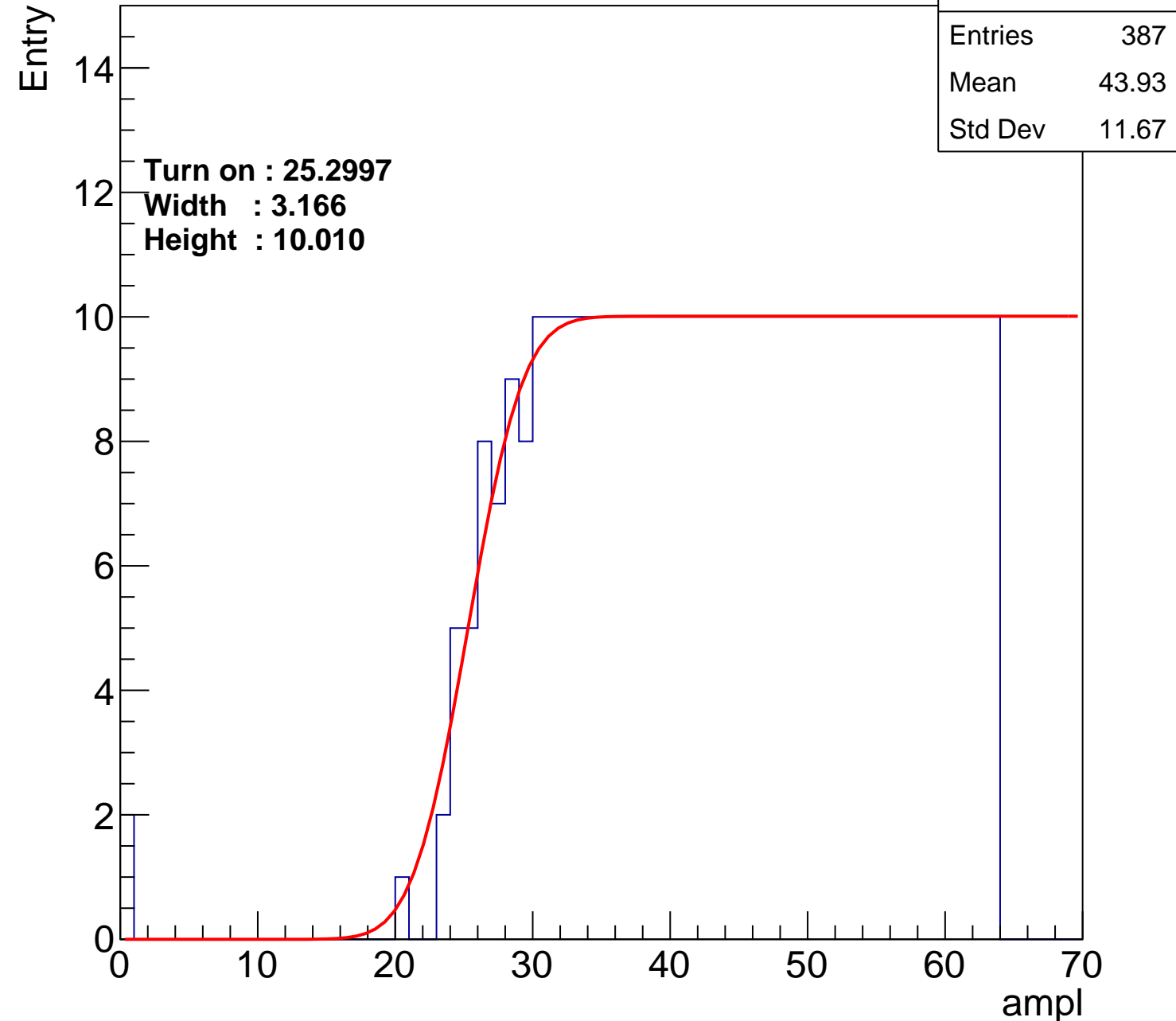
Width : 3.166

Height : 10.010

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch43

calib_packv5_042523_0143.root, FC#0, port D2

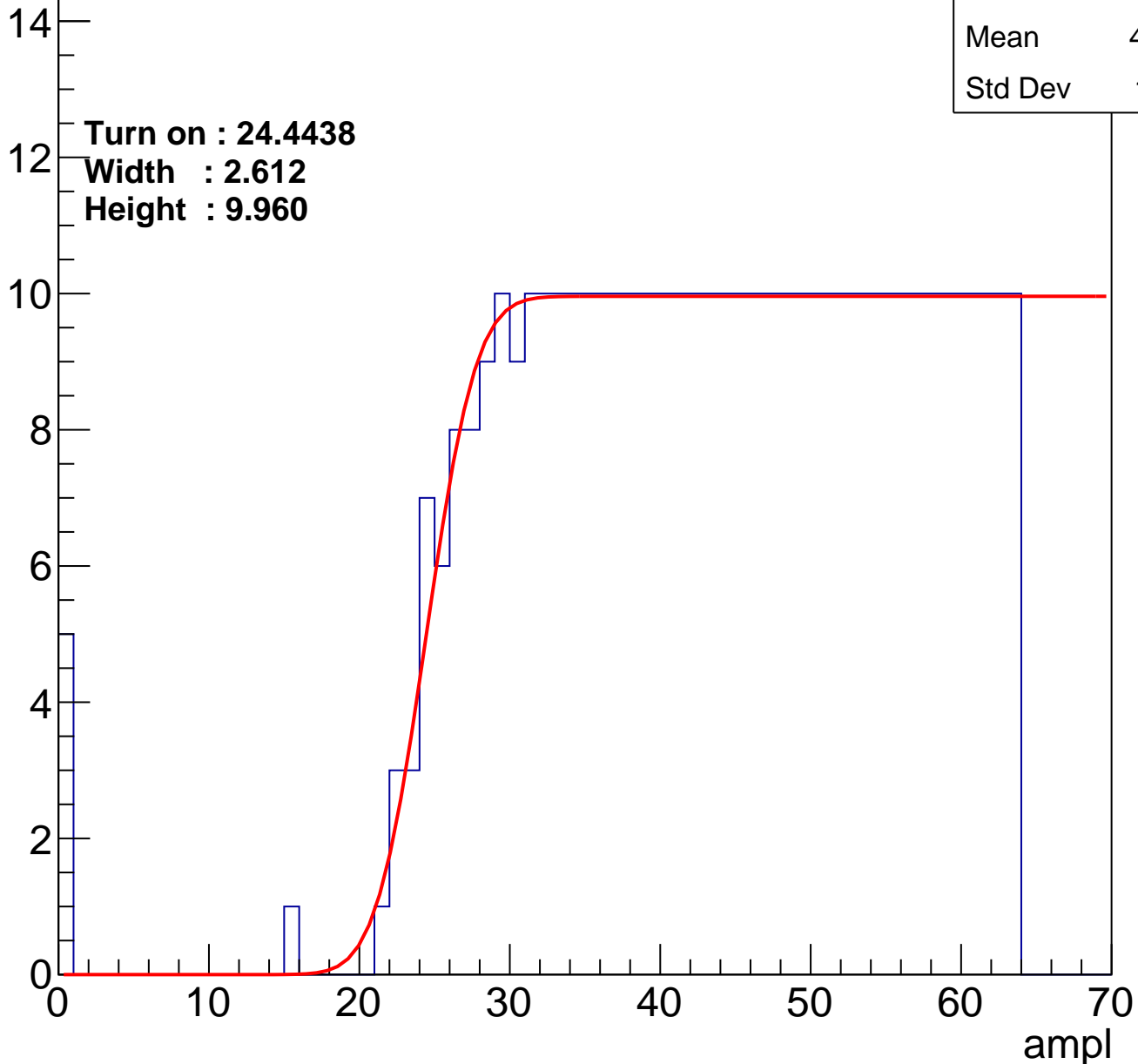
Entries	400
Mean	43.09
Std Dev	12.51

Turn on : 24.4438

Width : 2.612

Height : 9.960

Entry



B1L101S, U14-ch44

calib_packv5_042523_0143.root, FC#0, port D2

Entries	365
Mean	44.97
Std Dev	11.17

Turn on : 27.6908

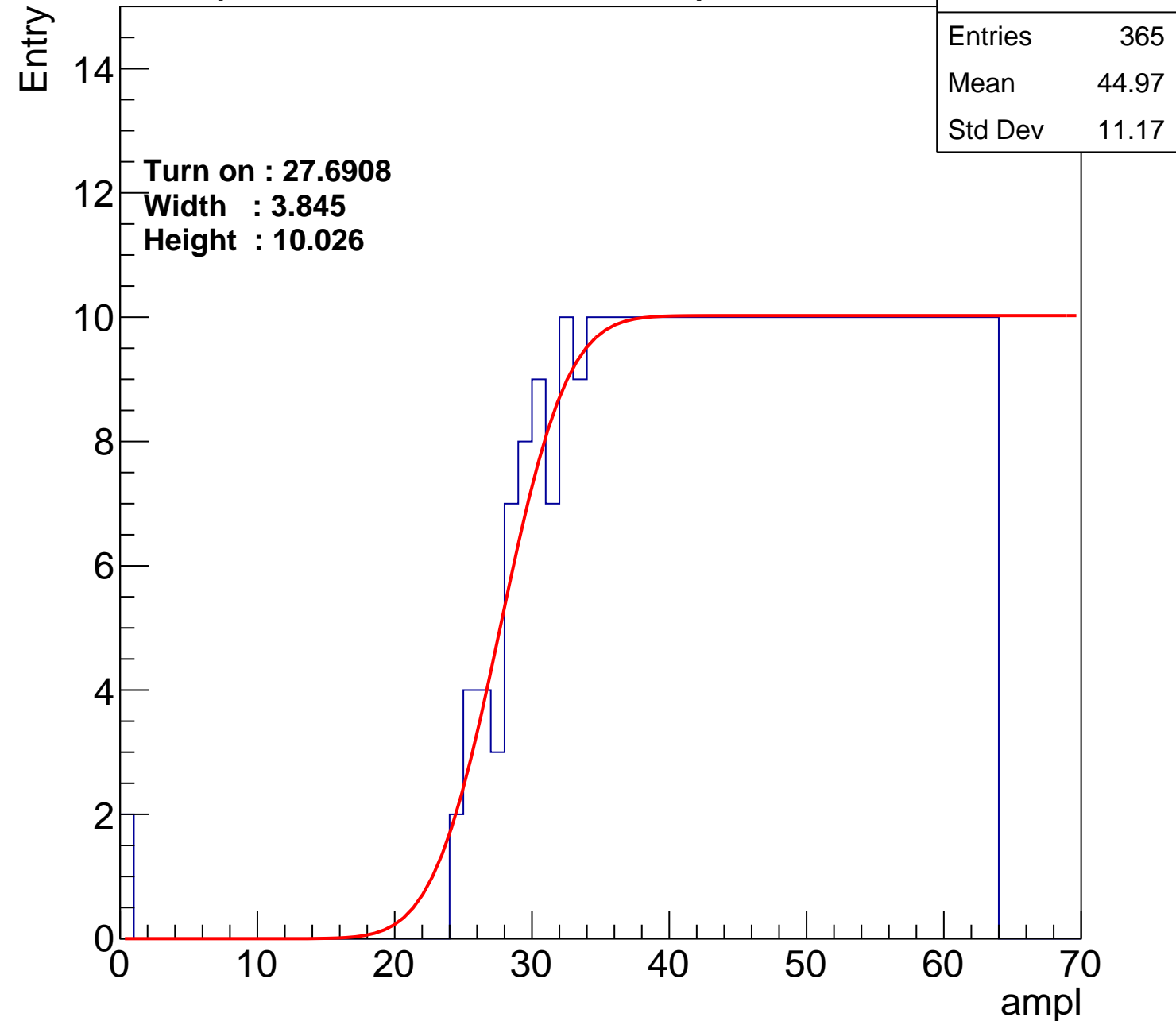
Width : 3.845

Height : 10.026

Entry

14
12
10
8
6
4
2
0

ampl



calib_packv5_042523_0143.root, FC#0, port D2

calib_packv5_042523_0143.root, FC#0, port D2

Turn on : 28.4058
Width : 2.964
Height : 10.061



B1L101S, U14-ch46

calib_packv5_042523_0143.root, FC#0, port D2

Entries	371
Mean	44.71
Std Dev	11.28

Turn on : 27.4804

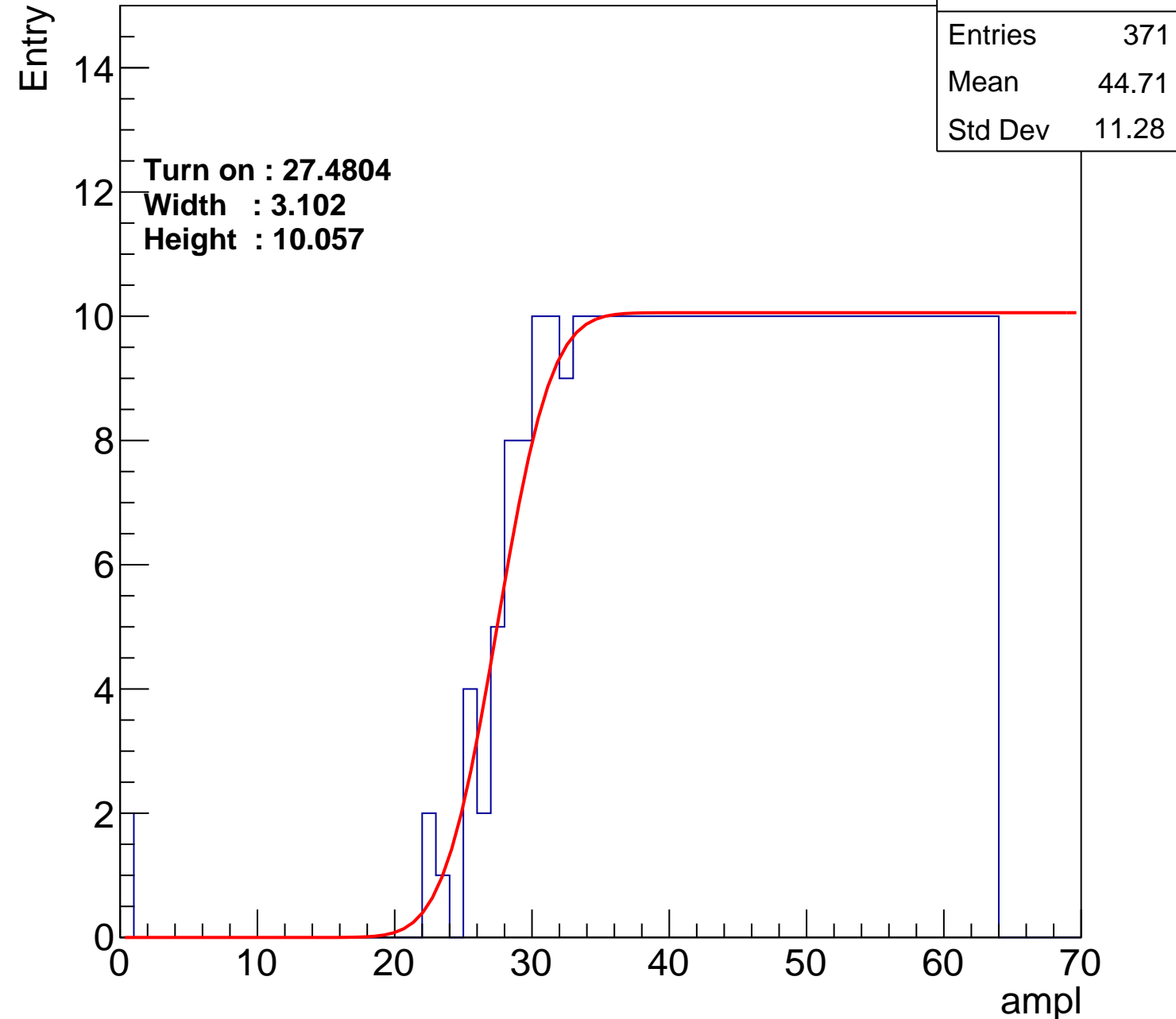
Width : 3.102

Height : 10.057

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch47

calib_packv5_042523_0143.root, FC#0, port D2

Entries	378
Mean	44.31
Std Dev	11.62

Turn on : 26.4853

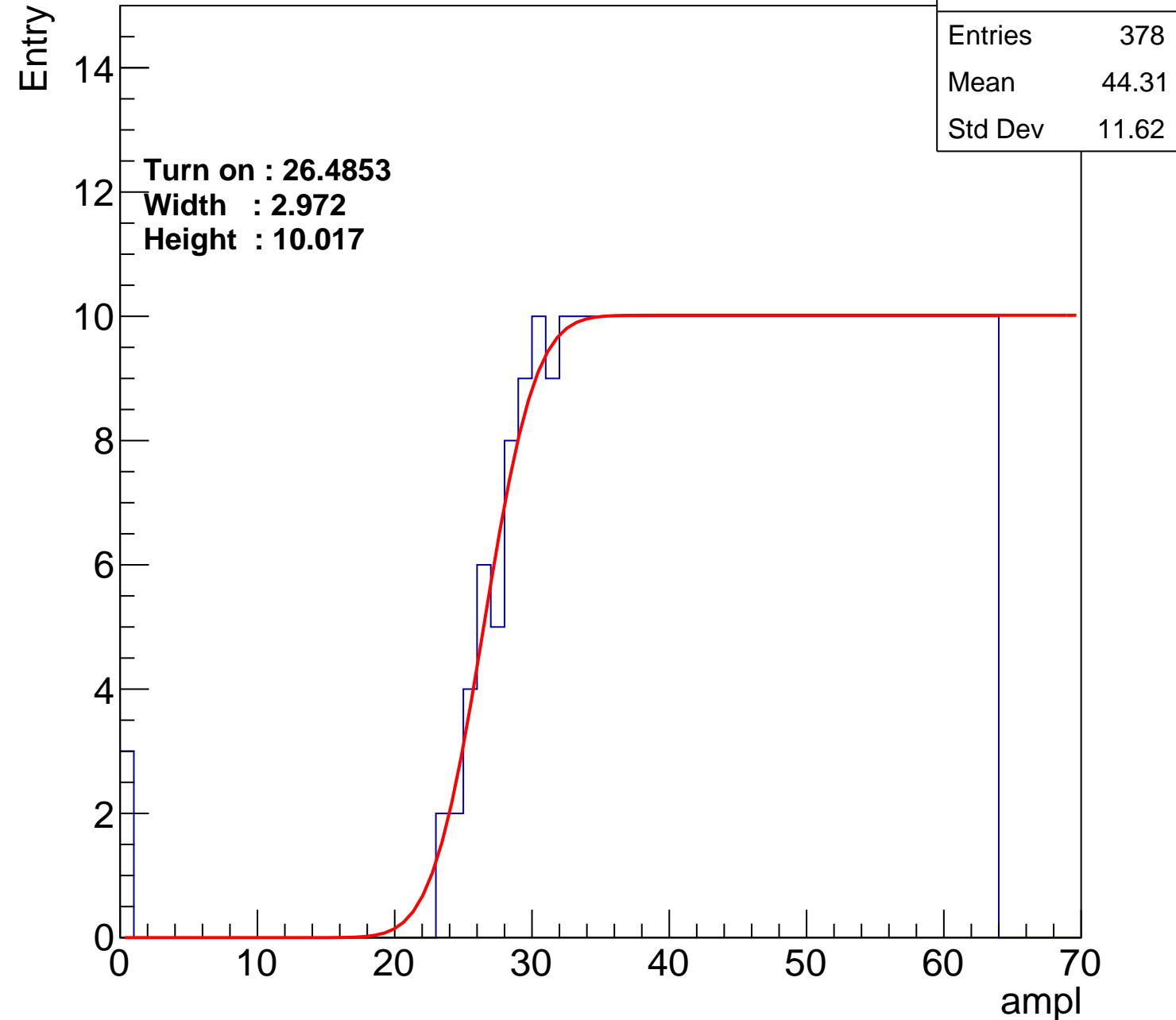
Width : 2.972

Height : 10.017

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch48

calib_packv5_042523_0143.root, FC#0, port D2

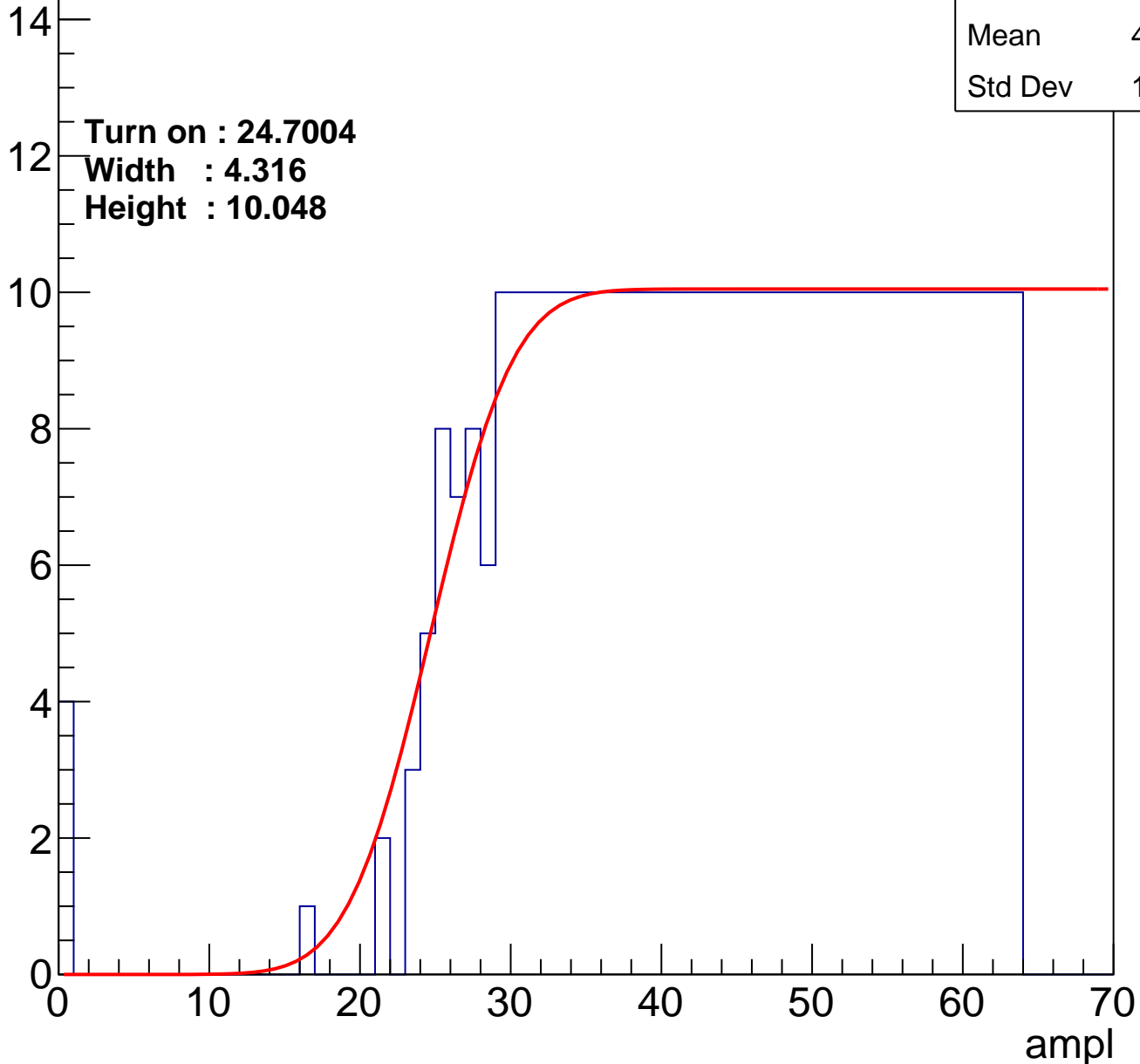
Entries	394
Mean	43.43
Std Dev	12.23

Turn on : 24.7004

Width : 4.316

Height : 10.048

Entry



B1L101S, U14-ch49

calib_packv5_042523_0143.root, FC#0, port D2

Entries	377
Mean	44.19
Std Dev	12.02

Turn on : 27.5071

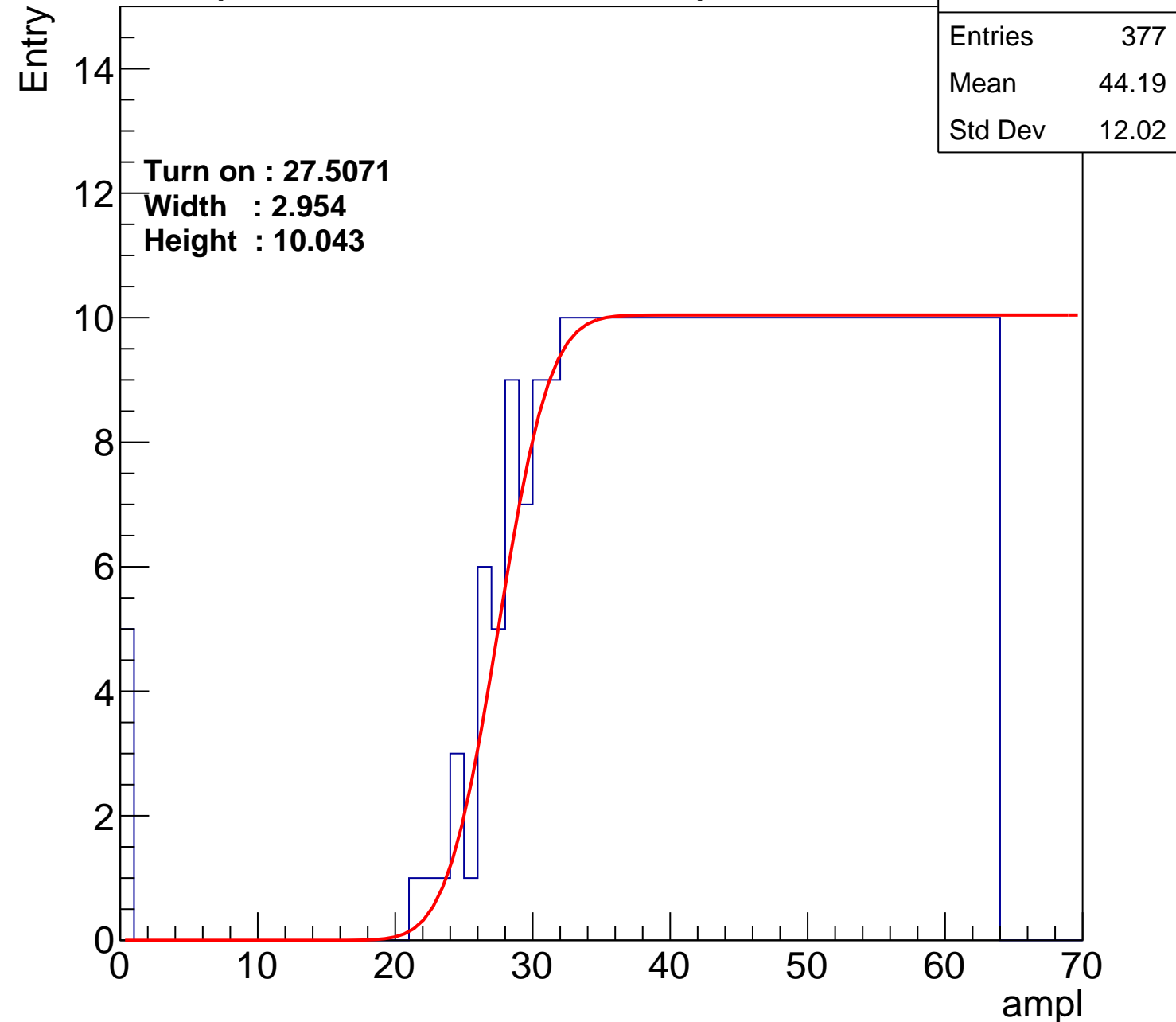
Width : 2.954

Height : 10.043

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch50

calib_packv5_042523_0143.root, FC#0, port D2

Entries	380
Mean	44.18
Std Dev	11.8

Turn on : 26.9566

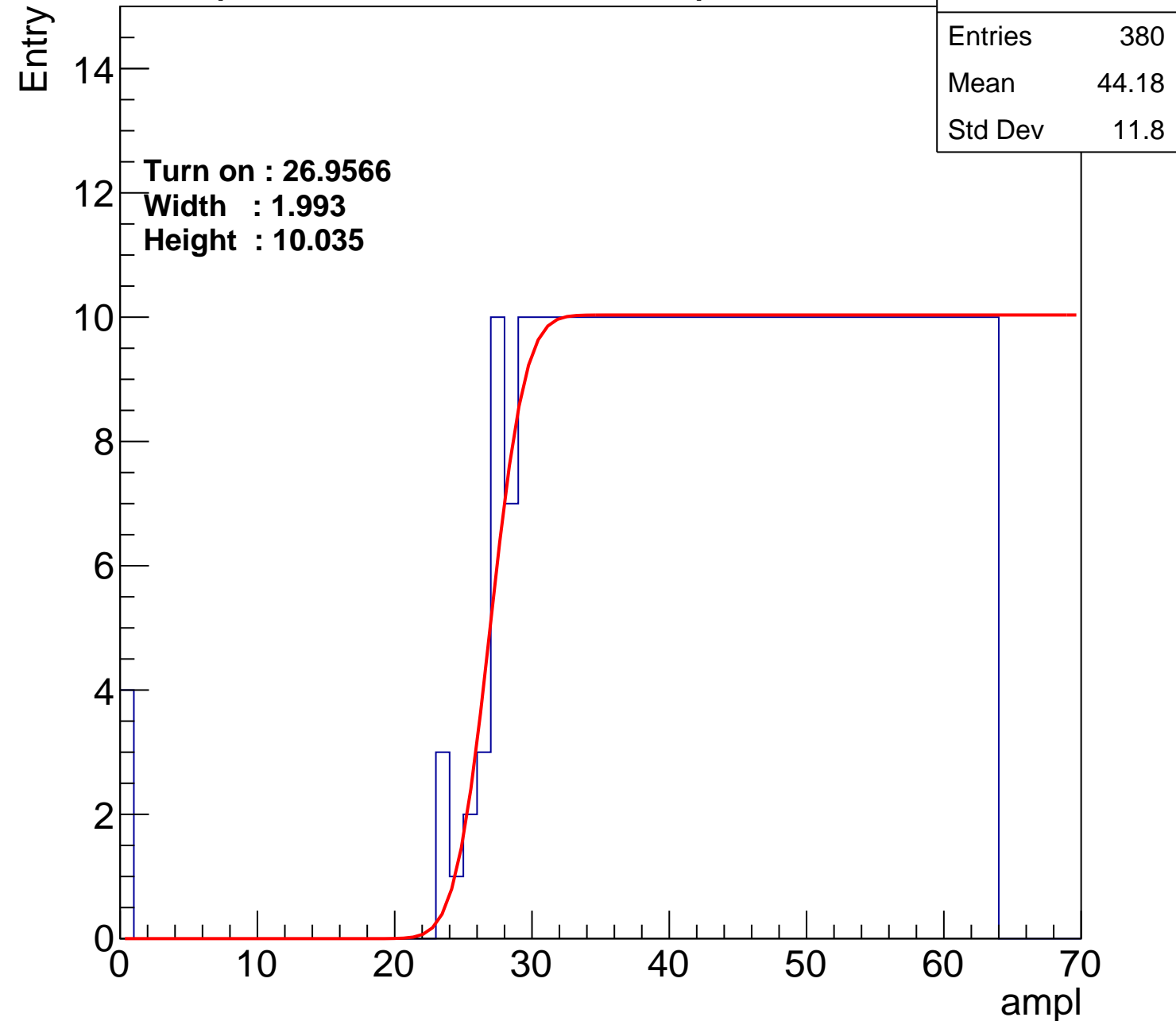
Width : 1.993

Height : 10.035

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch51

calib_packv5_042523_0143.root, FC#0, port D2

Entries	349
Mean	45.65
Std Dev	11.05

Turn on : 29.9203

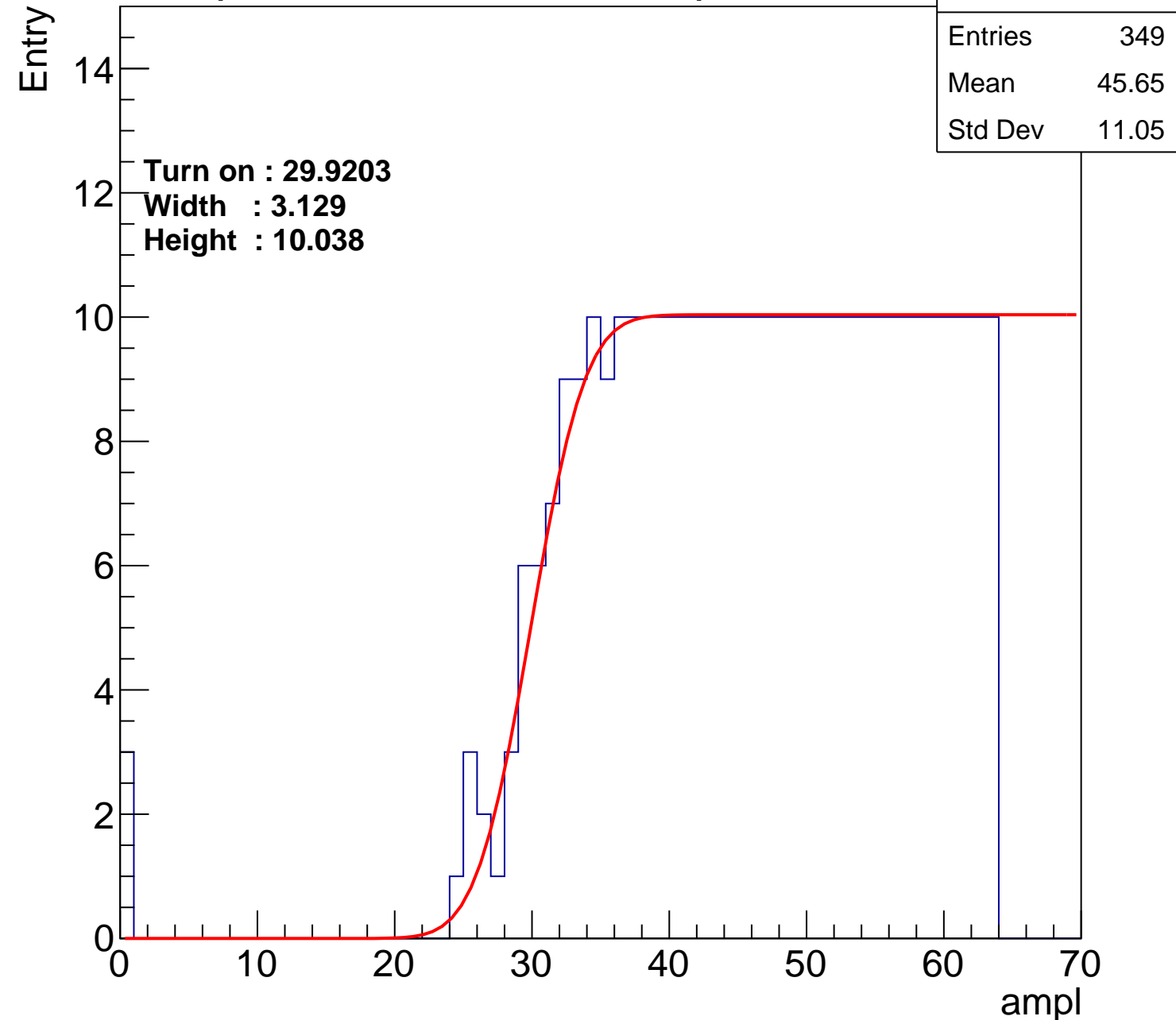
Width : 3.129

Height : 10.038

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch52

calib_packv5_042523_0143.root, FC#0, port D2

Entries	388
Mean	43.69
Std Dev	12.13

Turn on : 25.5341

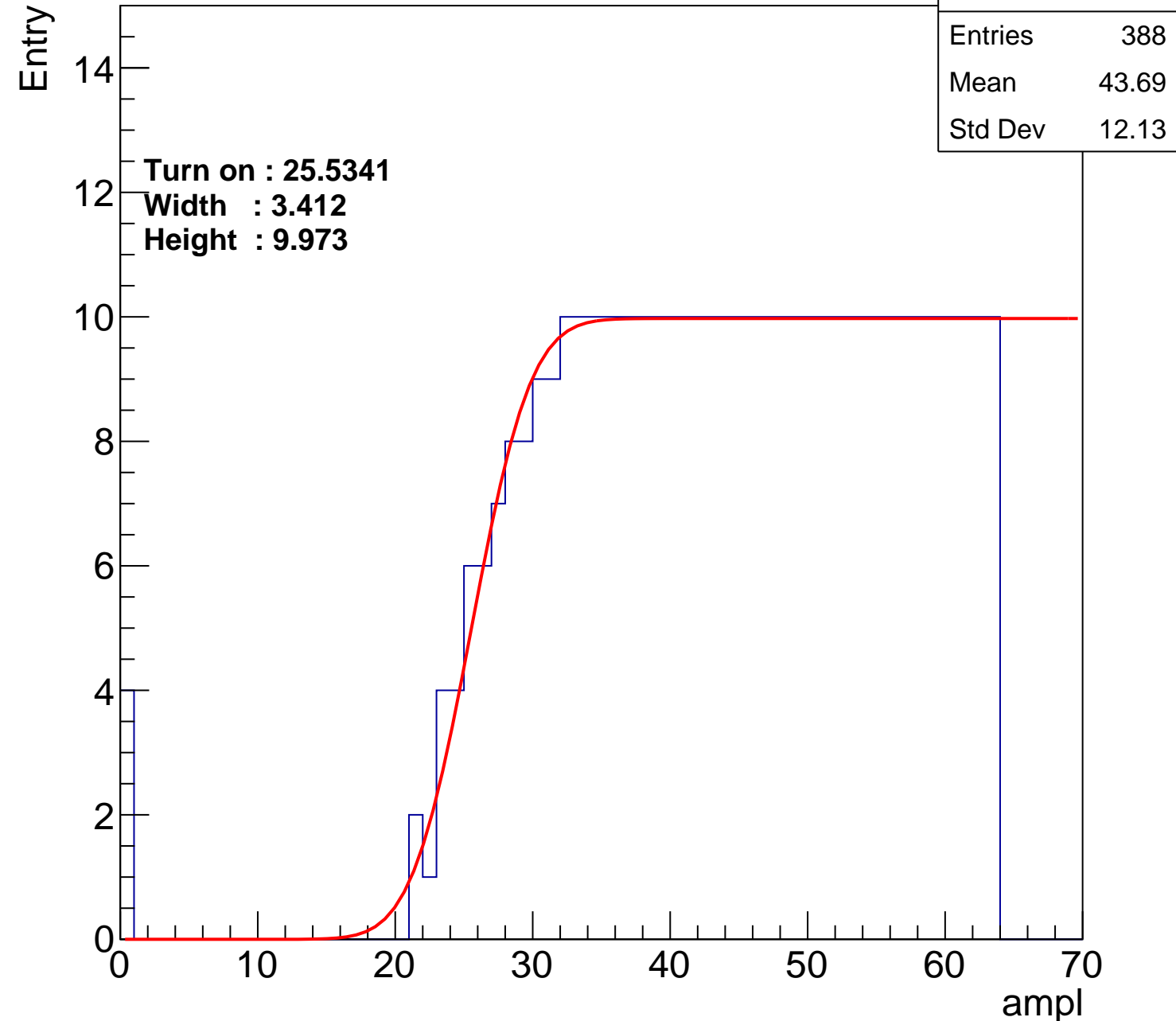
Width : 3.412

Height : 9.973

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch53

calib_packv5_042523_0143.root, FC#0, port D2

Entries	359
Mean	45.26
Std Dev	11.04

Turn on : 29.0920

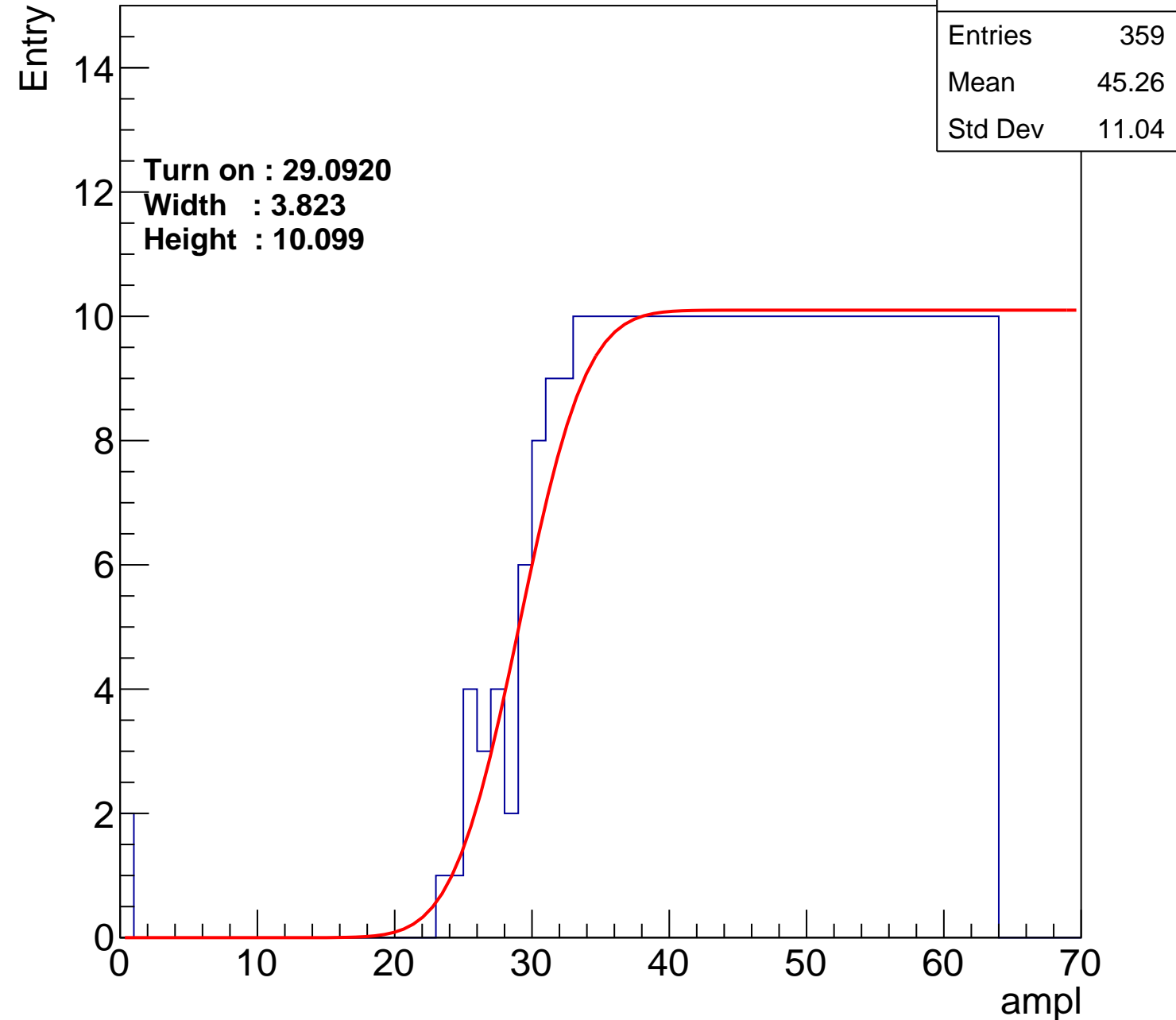
Width : 3.823

Height : 10.099

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch54

calib_packv5_042523_0143.root, FC#0, port D2

Entries	384
Mean	44.04
Std Dev	11.65

Turn on : 25.9177

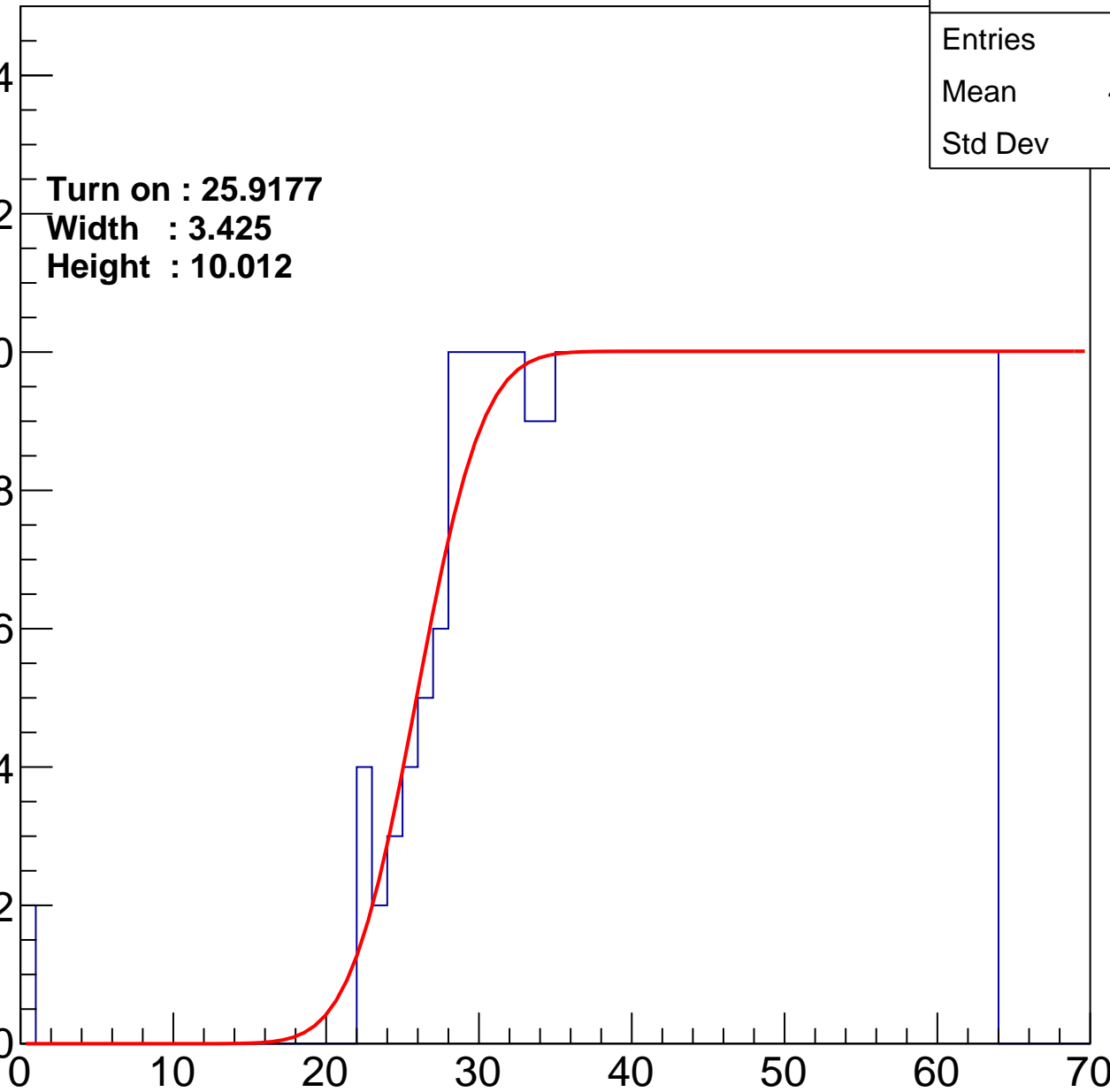
Width : 3.425

Height : 10.012

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch55

calib_packv5_042523_0143.root, FC#0, port D2

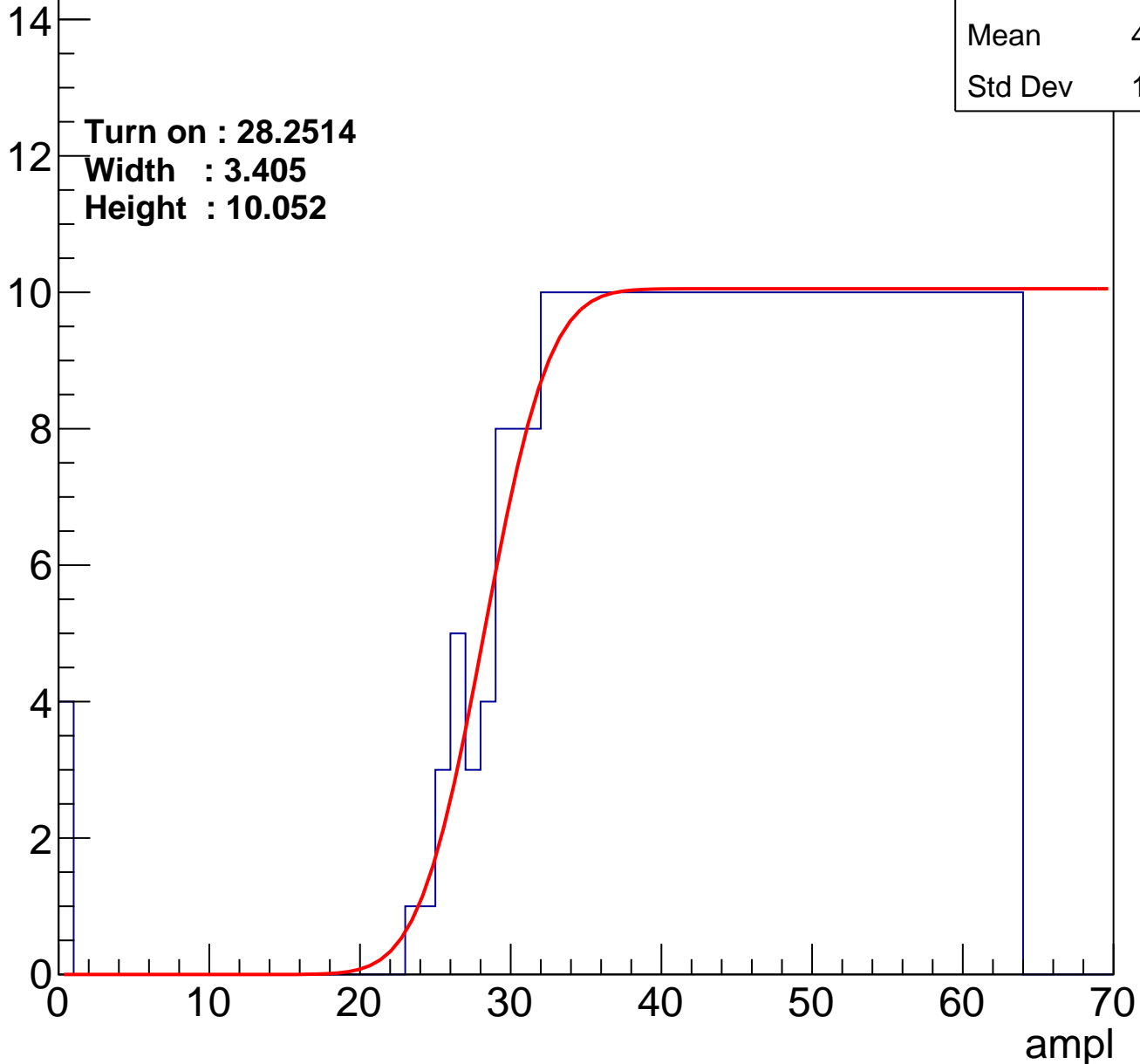
Entries	365
Mean	44.84
Std Dev	11.57

Turn on : 28.2514

Width : 3.405

Height : 10.052

Entry



B1L101S, U14-ch56

calib_packv5_042523_0143.root, FC#0, port D2

Entries	388
Mean	43.75
Std Dev	11.99

Turn on : 26.1407

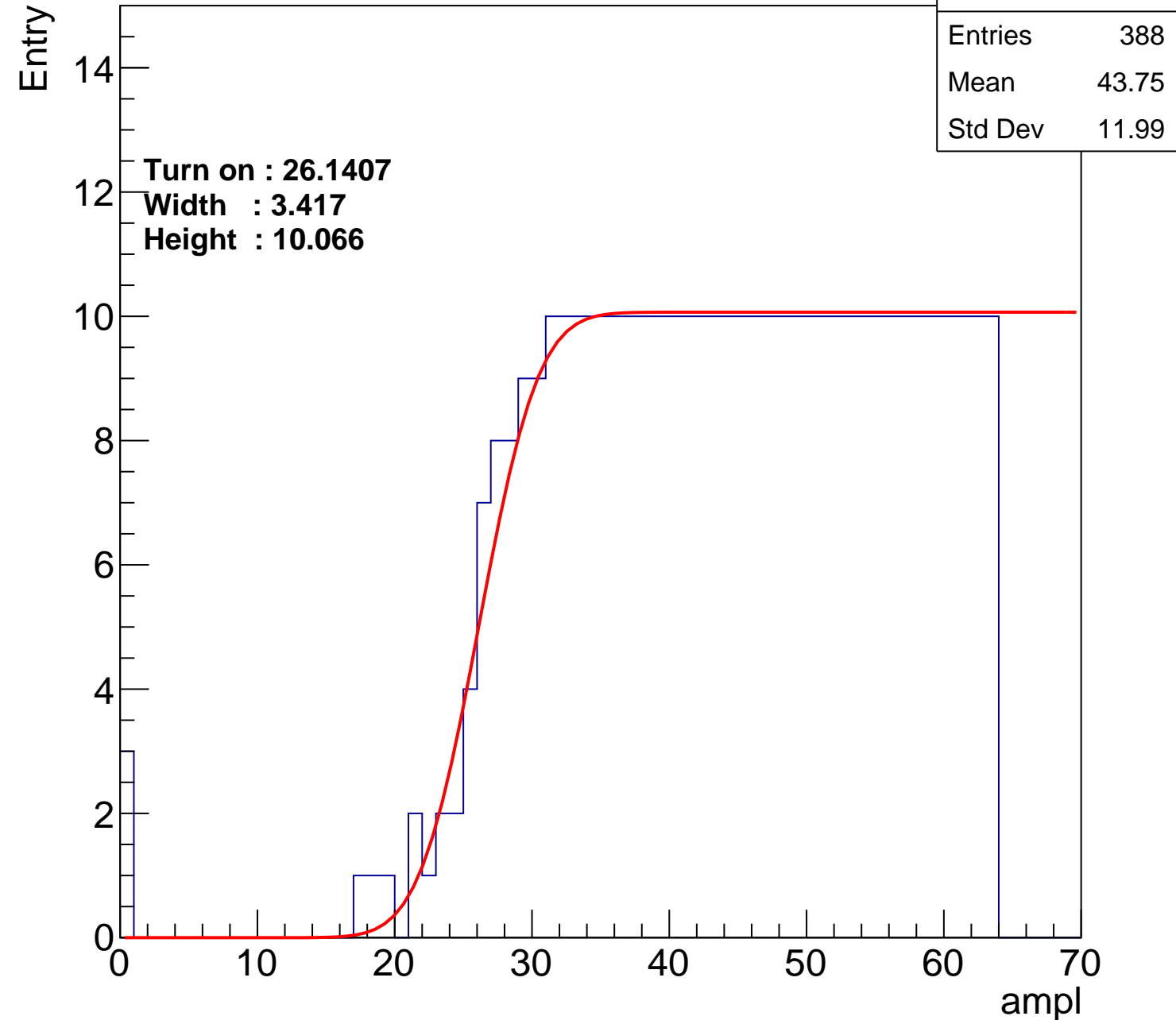
Width : 3.417

Height : 10.066

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch57

calib_packv5_042523_0143.root, FC#0, port D2

Entries	367
Mean	44.81
Std Dev	11.41

Turn on : 27.7916

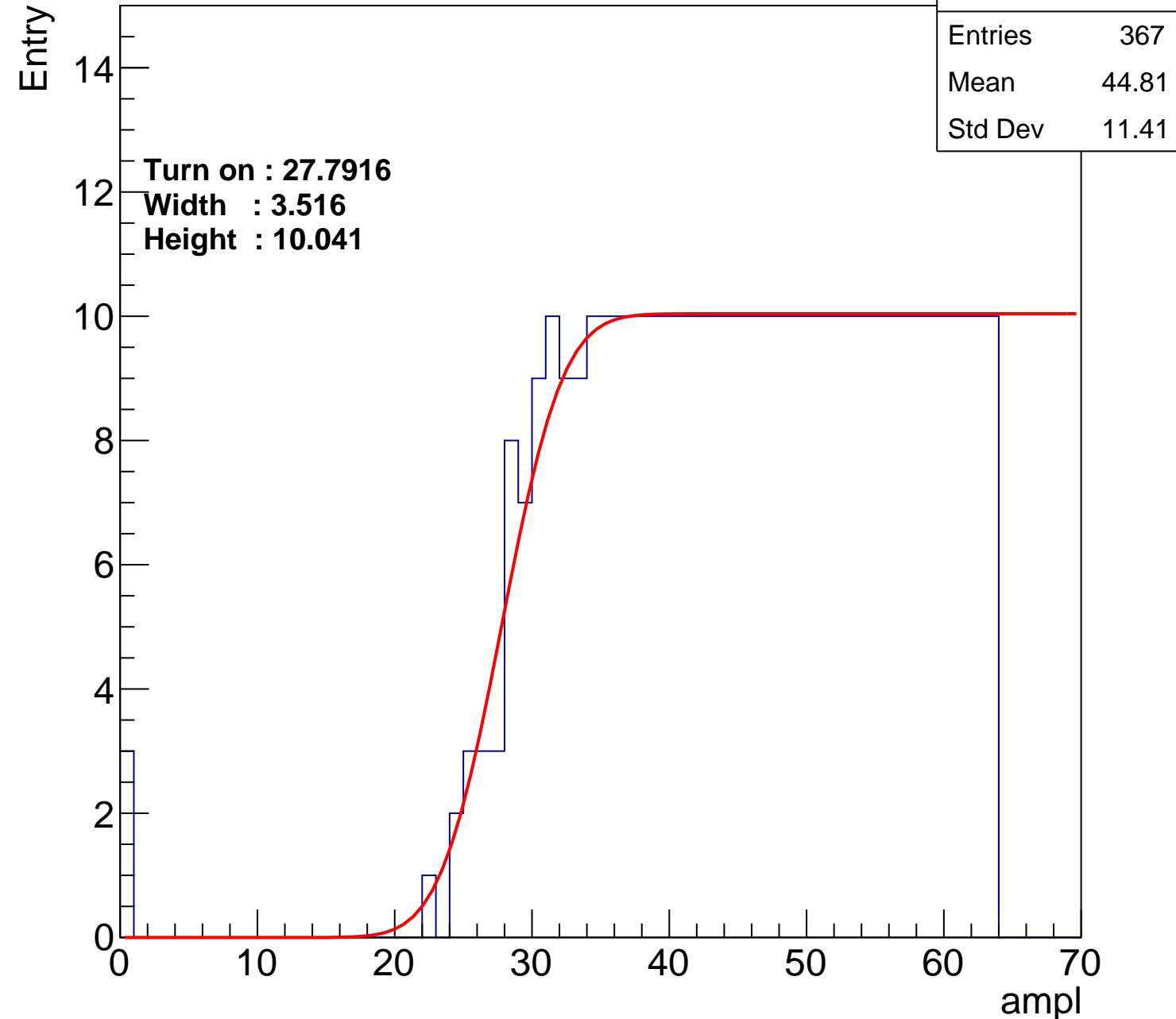
Width : 3.516

Height : 10.041

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch58

calib_packv5_042523_0143.root, FC#0, port D2

Entries	386
Mean	43.83
Std Dev	12.09

Turn on : 26.1124

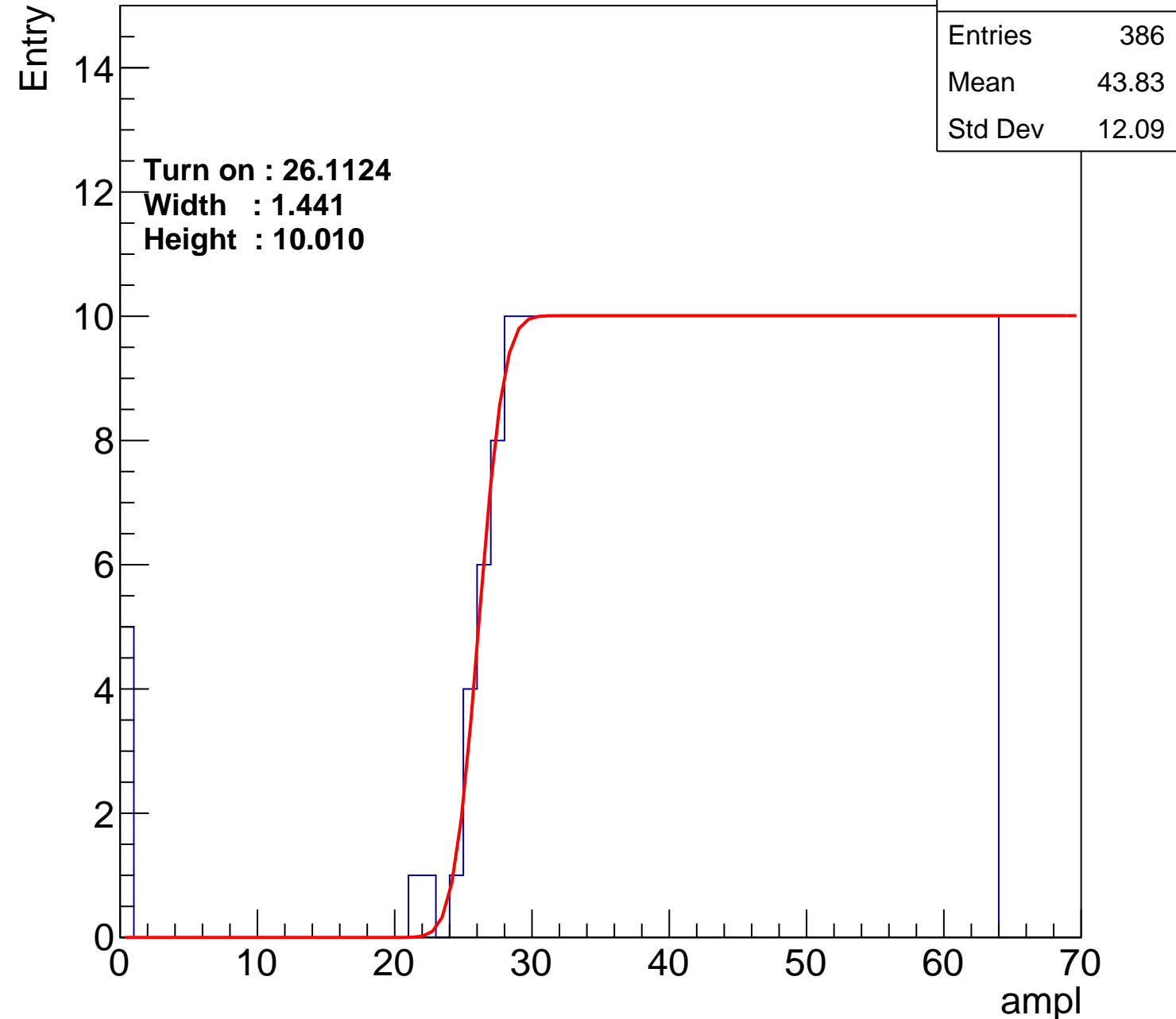
Width : 1.441

Height : 10.010

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch59

calib_packv5_042523_0143.root, FC#0, port D2

Entries	379
Mean	44.22
Std Dev	11.78

Turn on : 26.7273

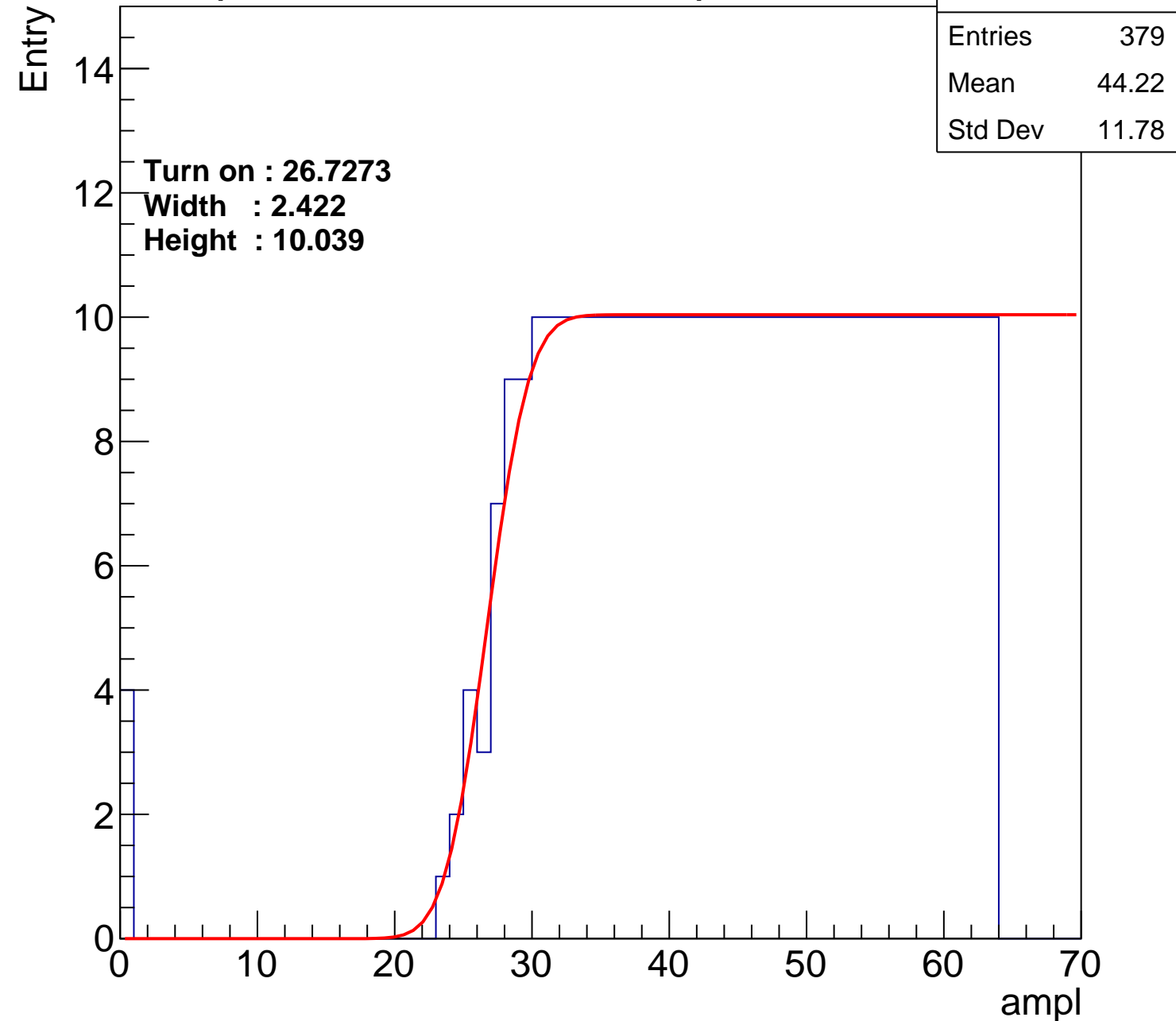
Width : 2.422

Height : 10.039

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch60

calib_packv5_042523_0143.root, FC#0, port D2

Entries	379
Mean	44.34
Std Dev	11.38

Turn on : 26.7395

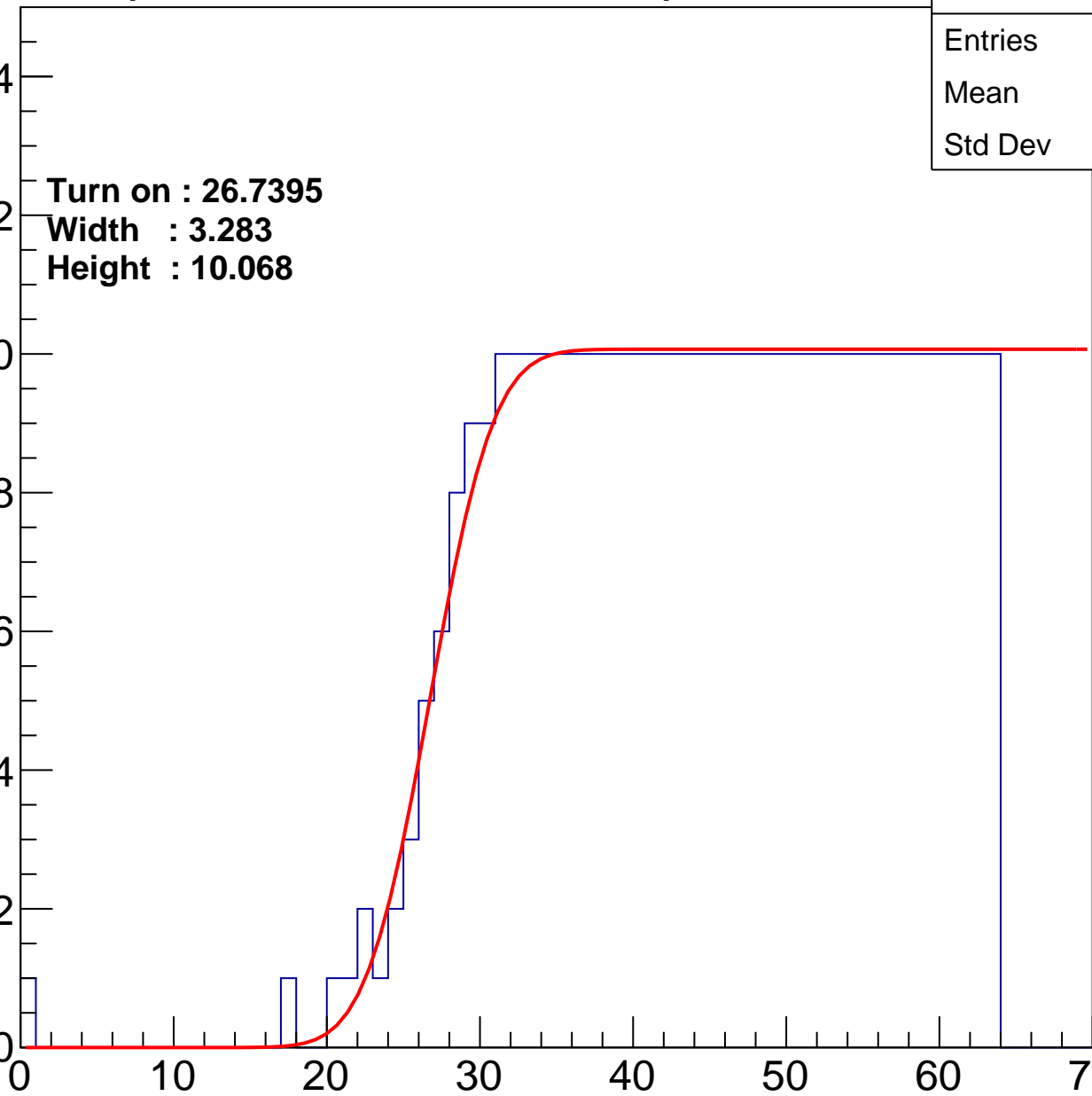
Width : 3.283

Height : 10.068

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch61

calib_packv5_042523_0143.root, FC#0, port D2

Entries	373
Mean	44.43
Std Dev	11.77

Turn on : 27.5084

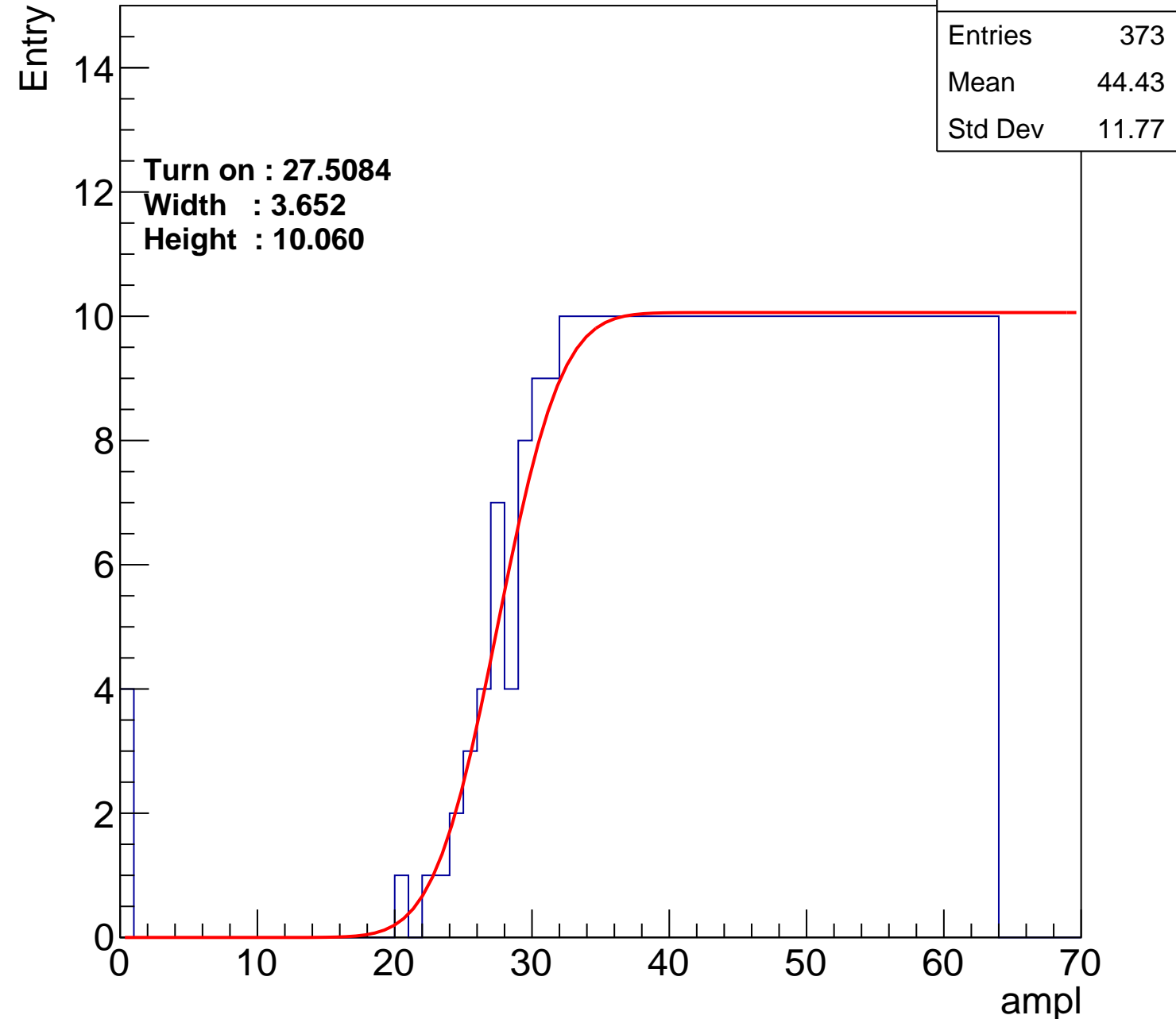
Width : 3.652

Height : 10.060

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch62

calib_packv5_042523_0143.root, FC#0, port D2

Entries	376
Mean	44.25
Std Dev	11.89

Turn on : 26.9996

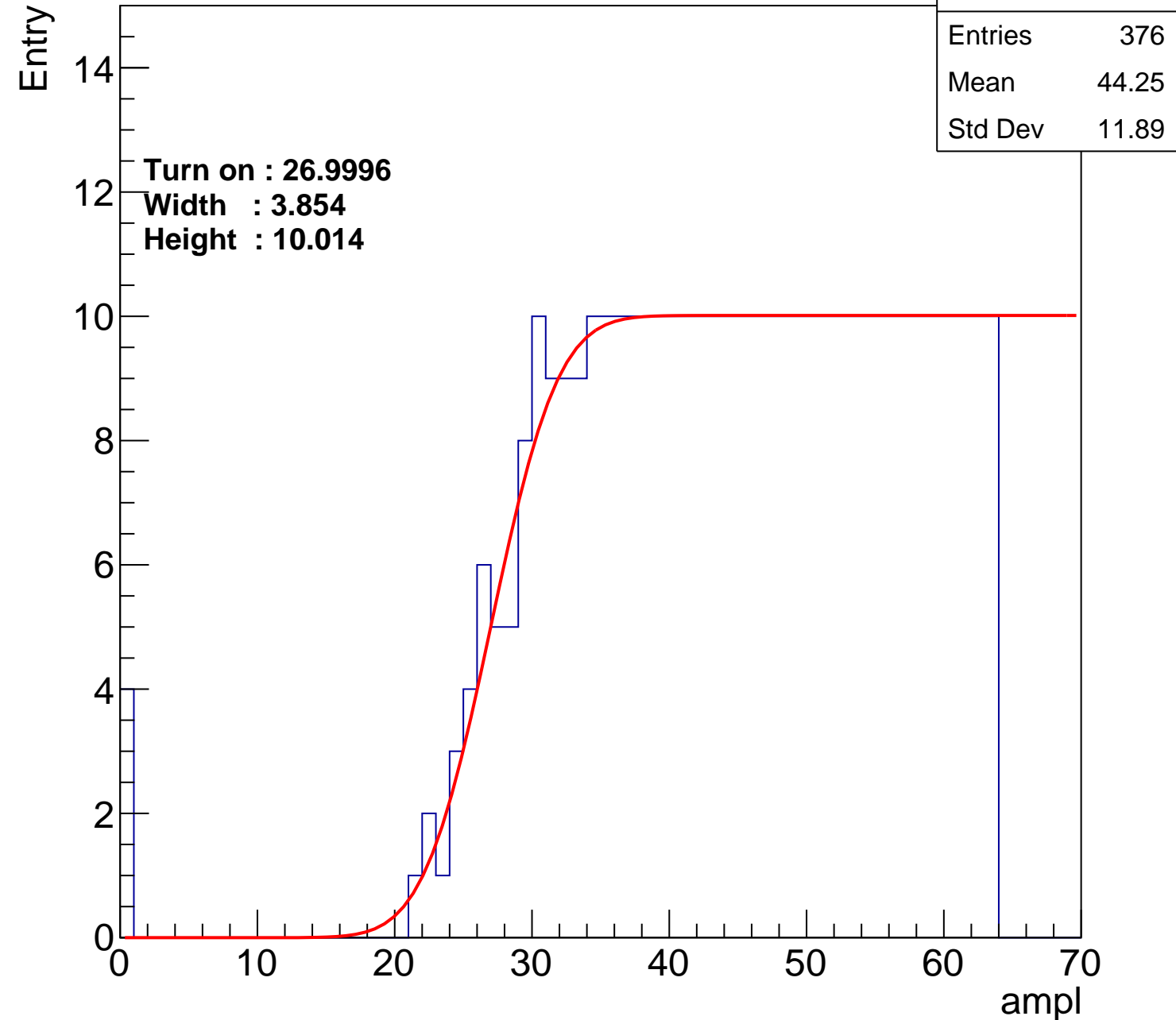
Width : 3.854

Height : 10.014

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch63

calib_packv5_042523_0143.root, FC#0, port D2

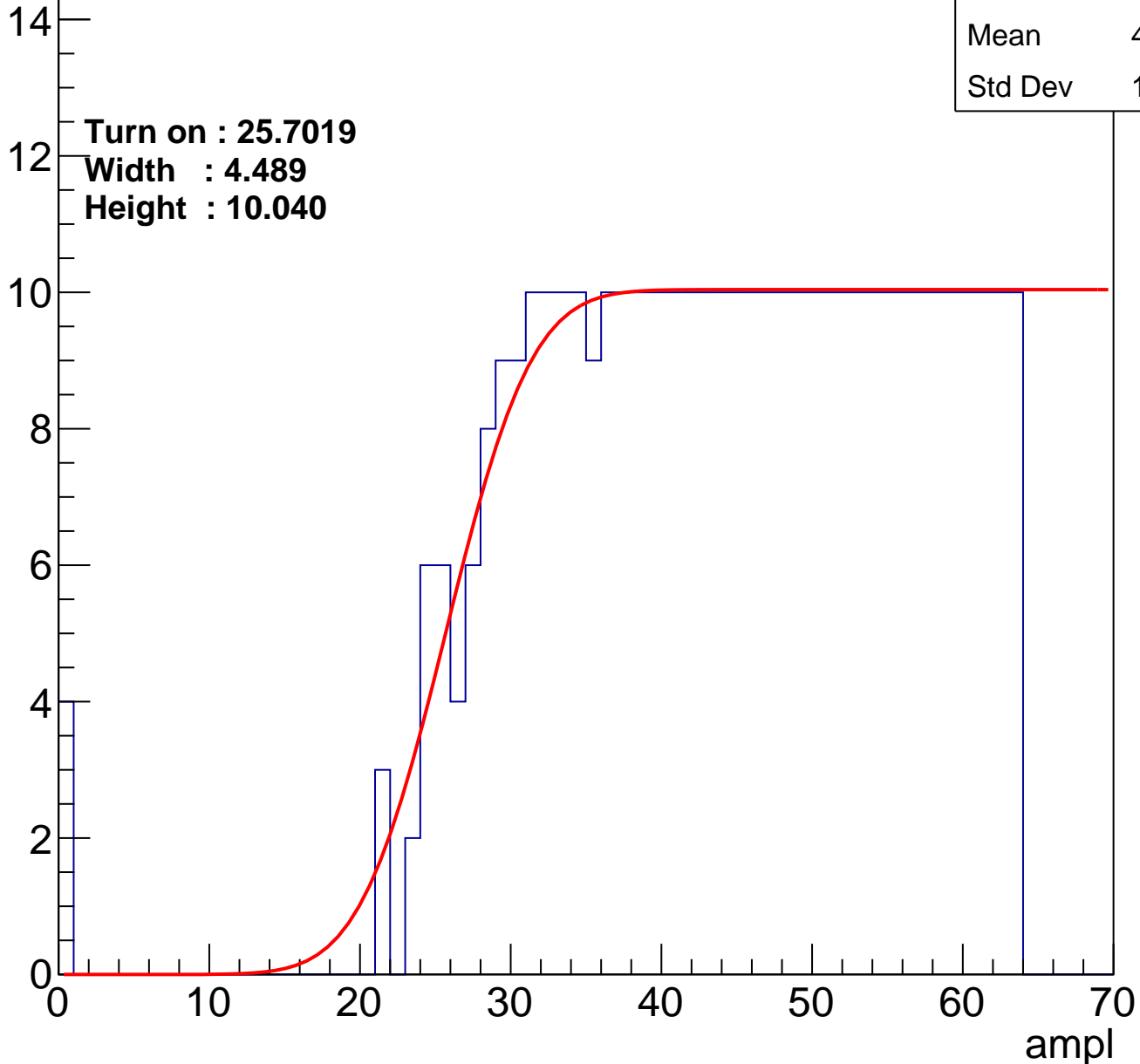
Entries	386
Mean	43.78
Std Dev	12.09

Turn on : 25.7019

Width : 4.489

Height : 10.040

Entry



B1L101S, U14-ch64

calib_packv5_042523_0143.root, FC#0, port D2

Entries	389
Mean	43.71
Std Dev	12.05

Turn on : 25.5357

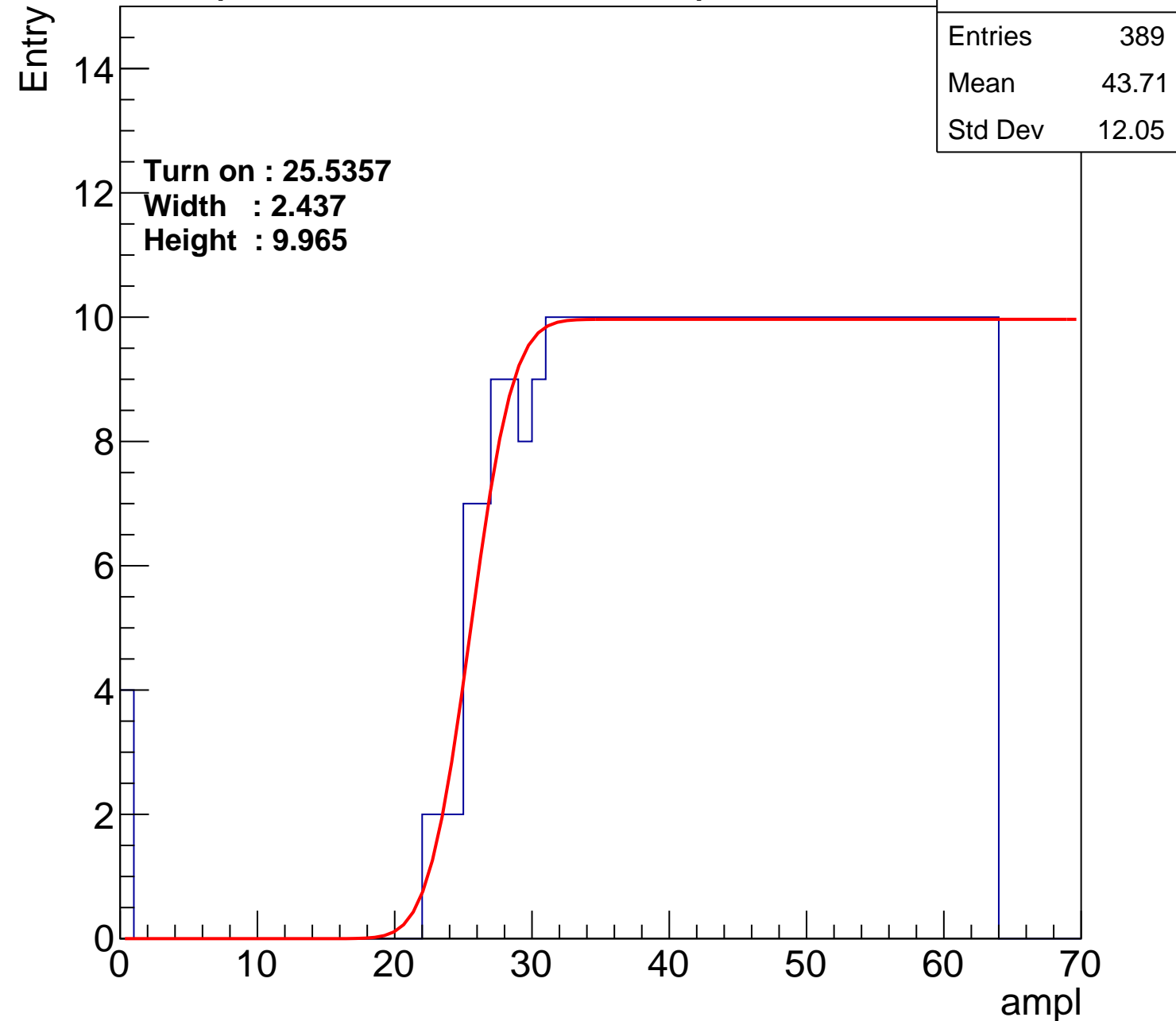
Width : 2.437

Height : 9.965

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch65

calib_packv5_042523_0143.root, FC#0, port D2

Entries	386
Mean	43.89
Std Dev	11.86

Turn on : 25.8097

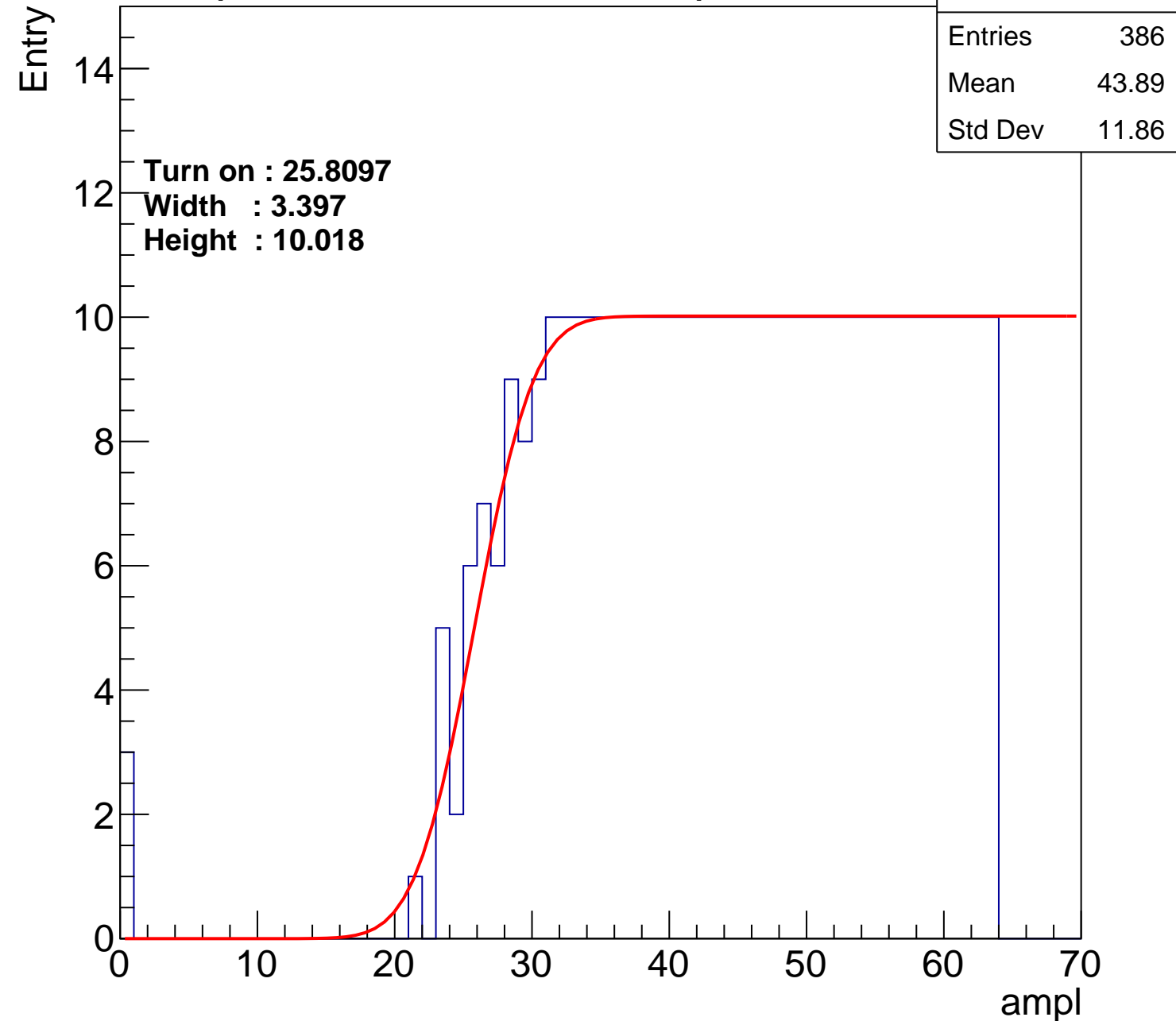
Width : 3.397

Height : 10.018

Entry

14
12
10
8
6
4
2
0

ampl

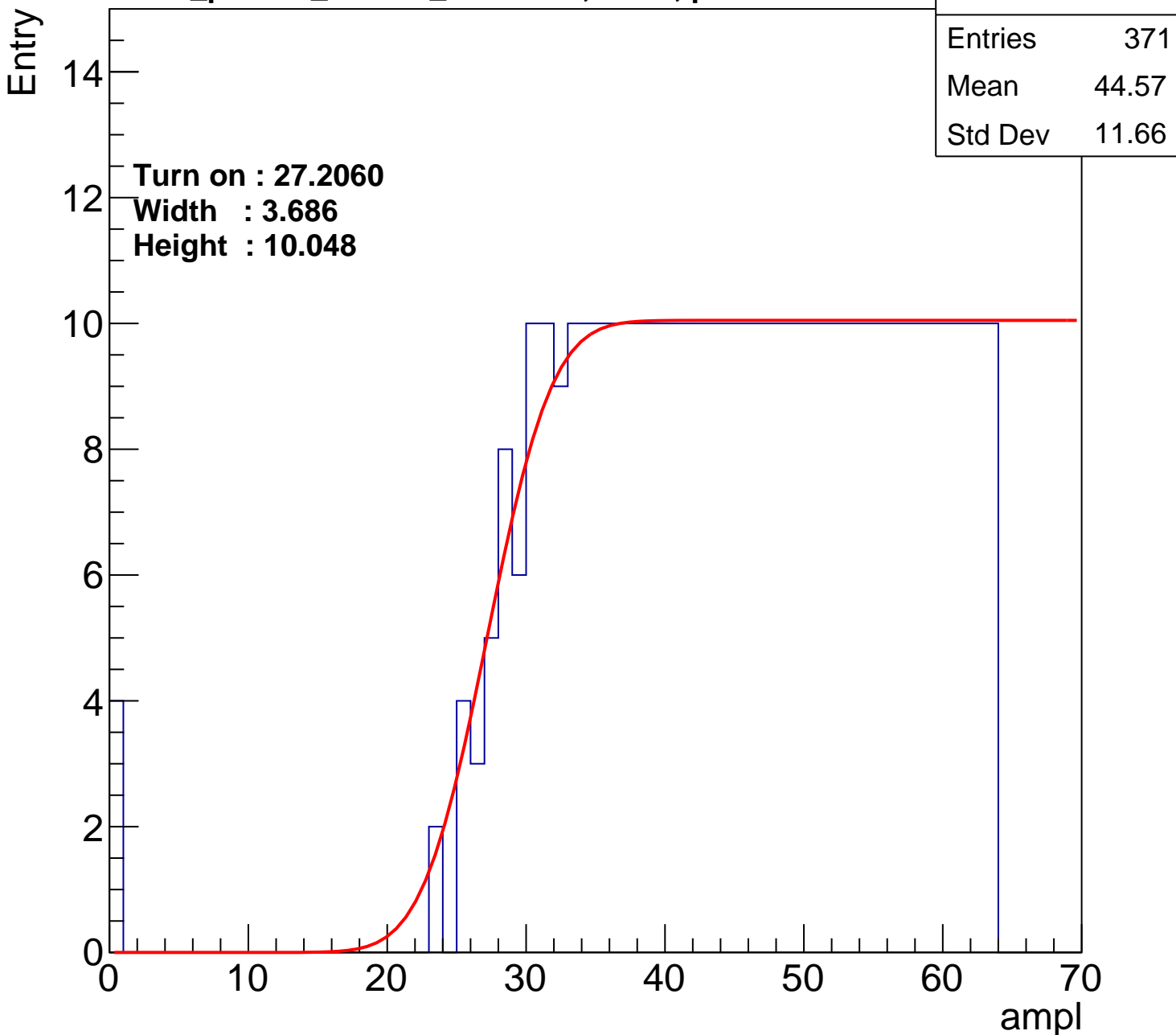


calib_packv5_042523_0143.root, FC#0, port D2

calib_packv5_042523_0143.root, FC#0, port D2

Entries	371
Mean	44.57
Std Dev	11.66

Height : 10.048



B1L101S, U14-ch67

calib_packv5_042523_0143.root, FC#0, port D2

Entries	369
Mean	44.55
Std Dev	11.88

Turn on : 27.8124

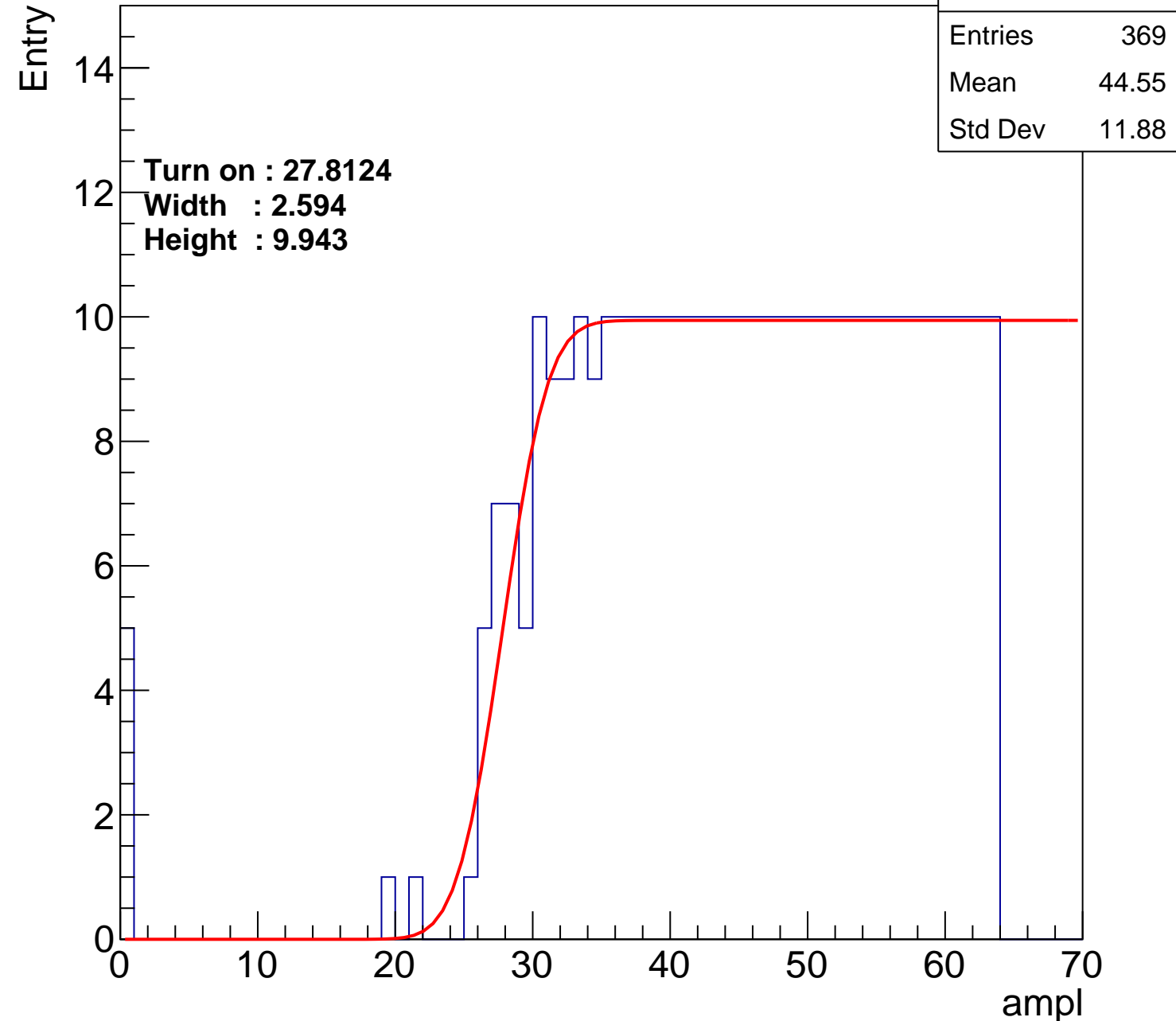
Width : 2.594

Height : 9.943

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch68

calib_packv5_042523_0143.root, FC#0, port D2

Entries	367
Mean	44.72
Std Dev	11.63

Turn on : 28.4883

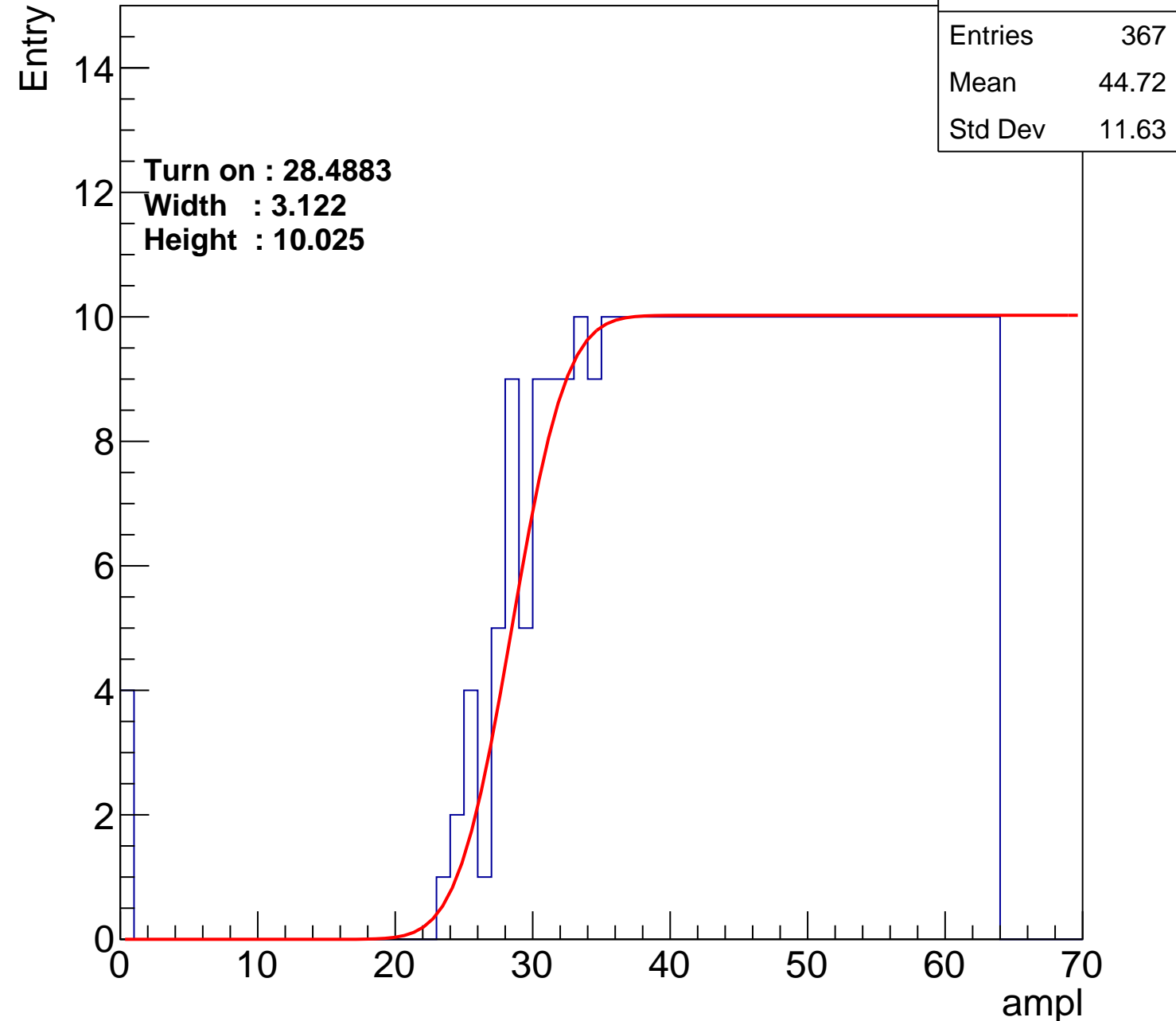
Width : 3.122

Height : 10.025

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch69

calib_packv5_042523_0143.root, FC#0, port D2

Entries	376
Mean	44.35
Std Dev	11.66

Turn on : 26.8503

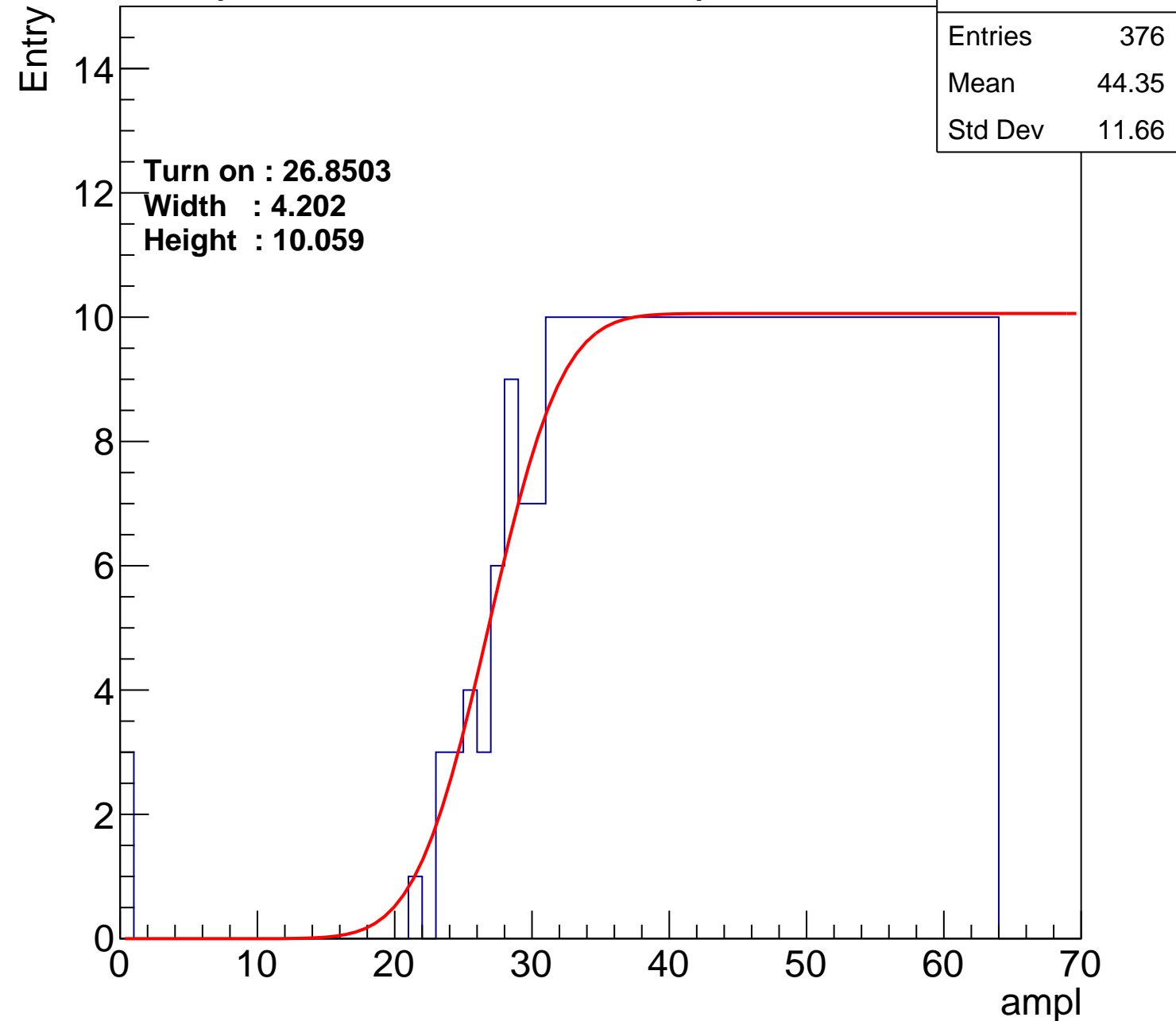
Width : 4.202

Height : 10.059

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch70

calib_packv5_042523_0143.root, FC#0, port D2

Entries	390
Mean	43.53
Std Dev	12.41

Turn on : 25.9273

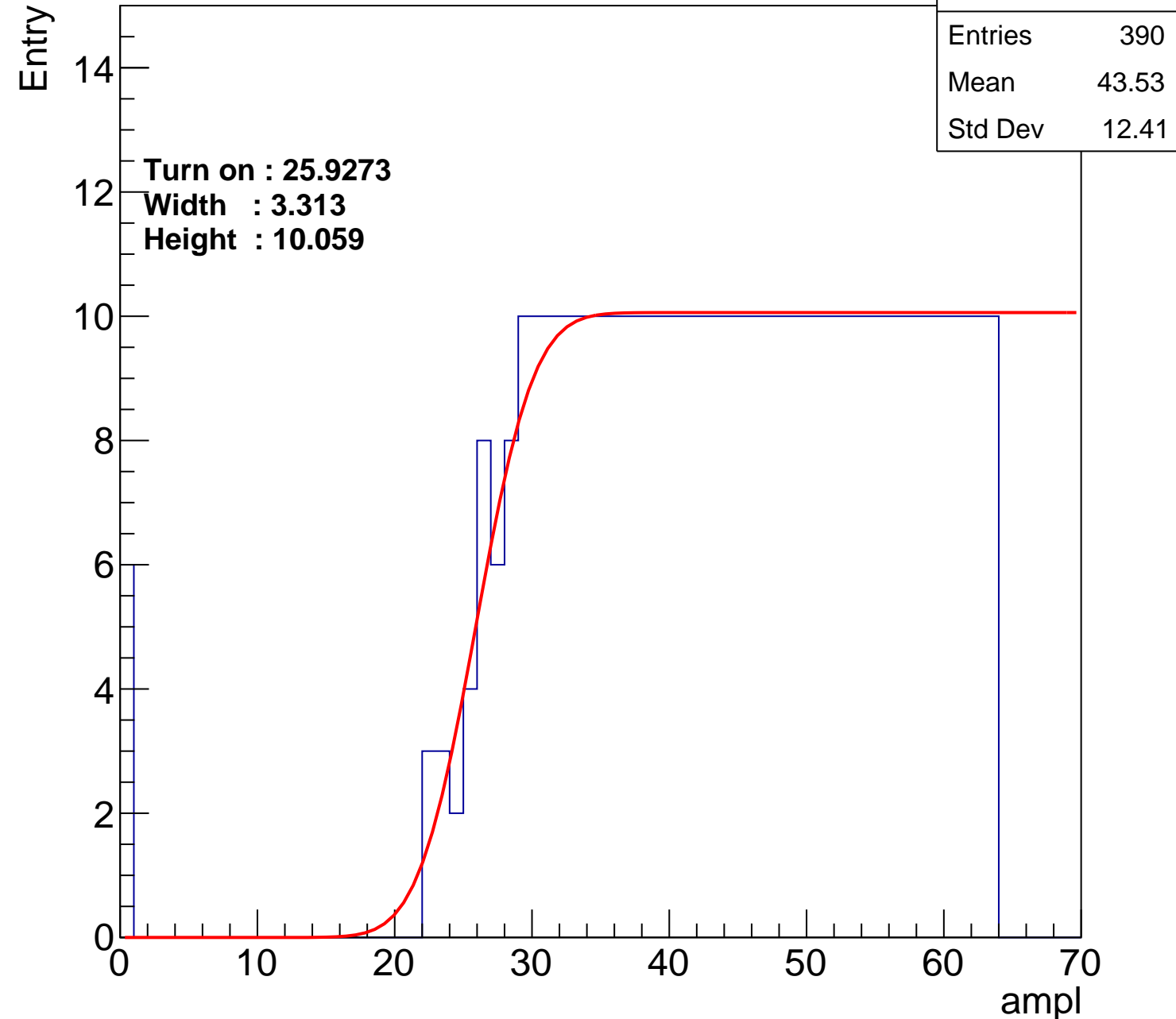
Width : 3.313

Height : 10.059

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch71

calib_packv5_042523_0143.root, FC#0, port D2

Entries	359
Mean	45.29
Std Dev	10.99

Turn on : 28.1104

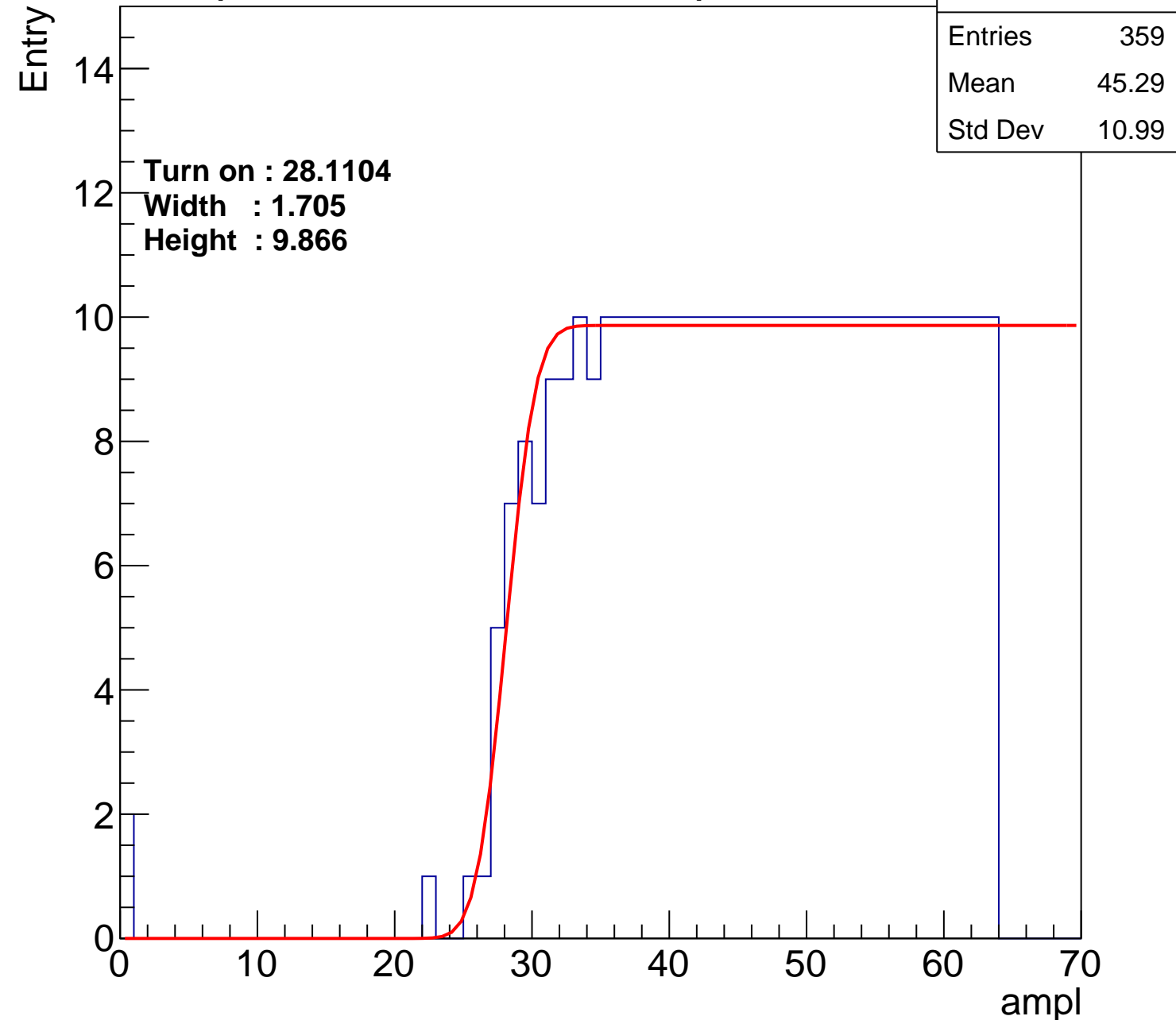
Width : 1.705

Height : 9.866

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch72

calib_packv5_042523_0143.root, FC#0, port D2

Entries	386
Mean	43.88
Std Dev	11.87

Turn on : 25.7267

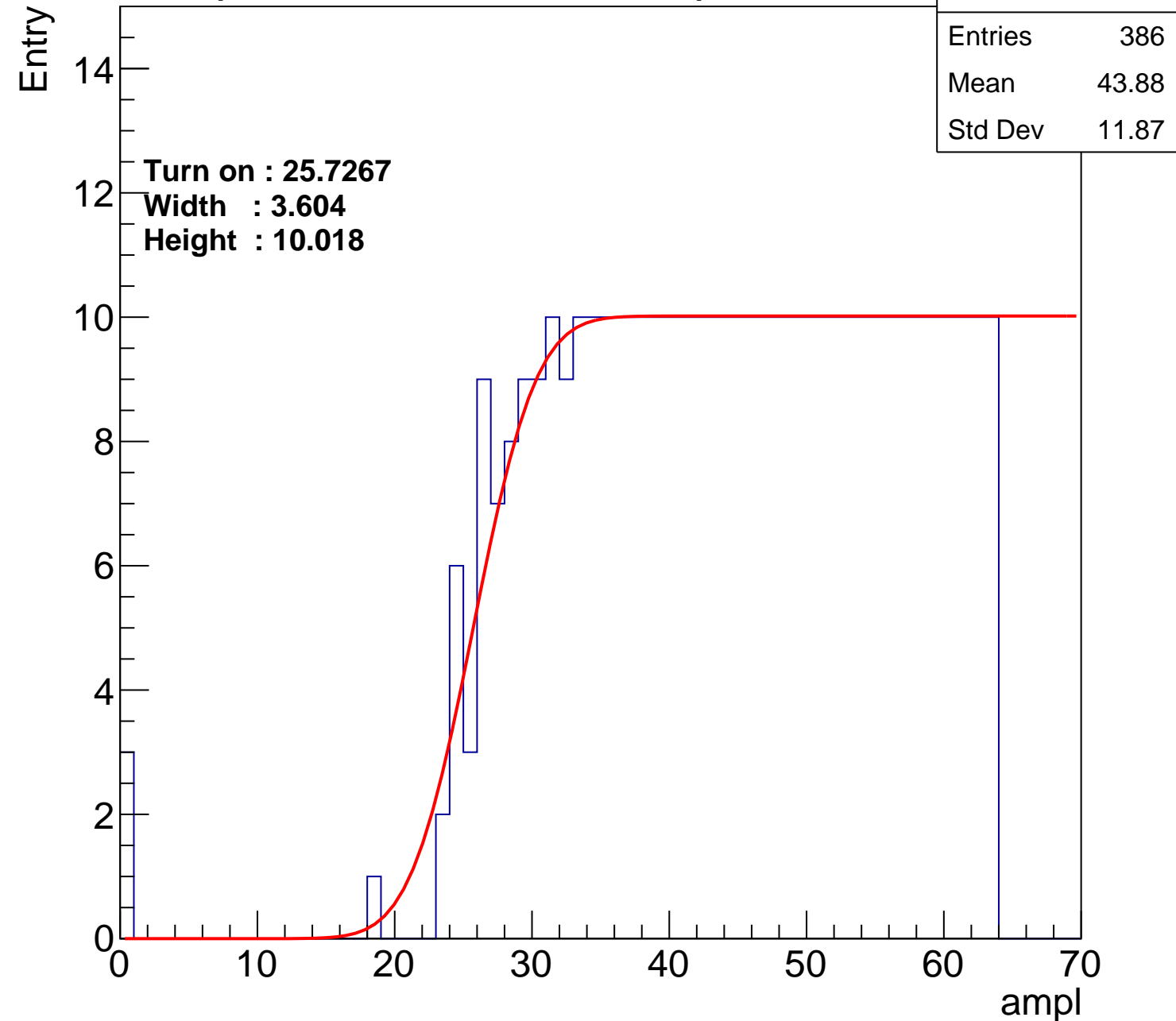
Width : 3.604

Height : 10.018

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch73

calib_packv5_042523_0143.root, FC#0, port D2

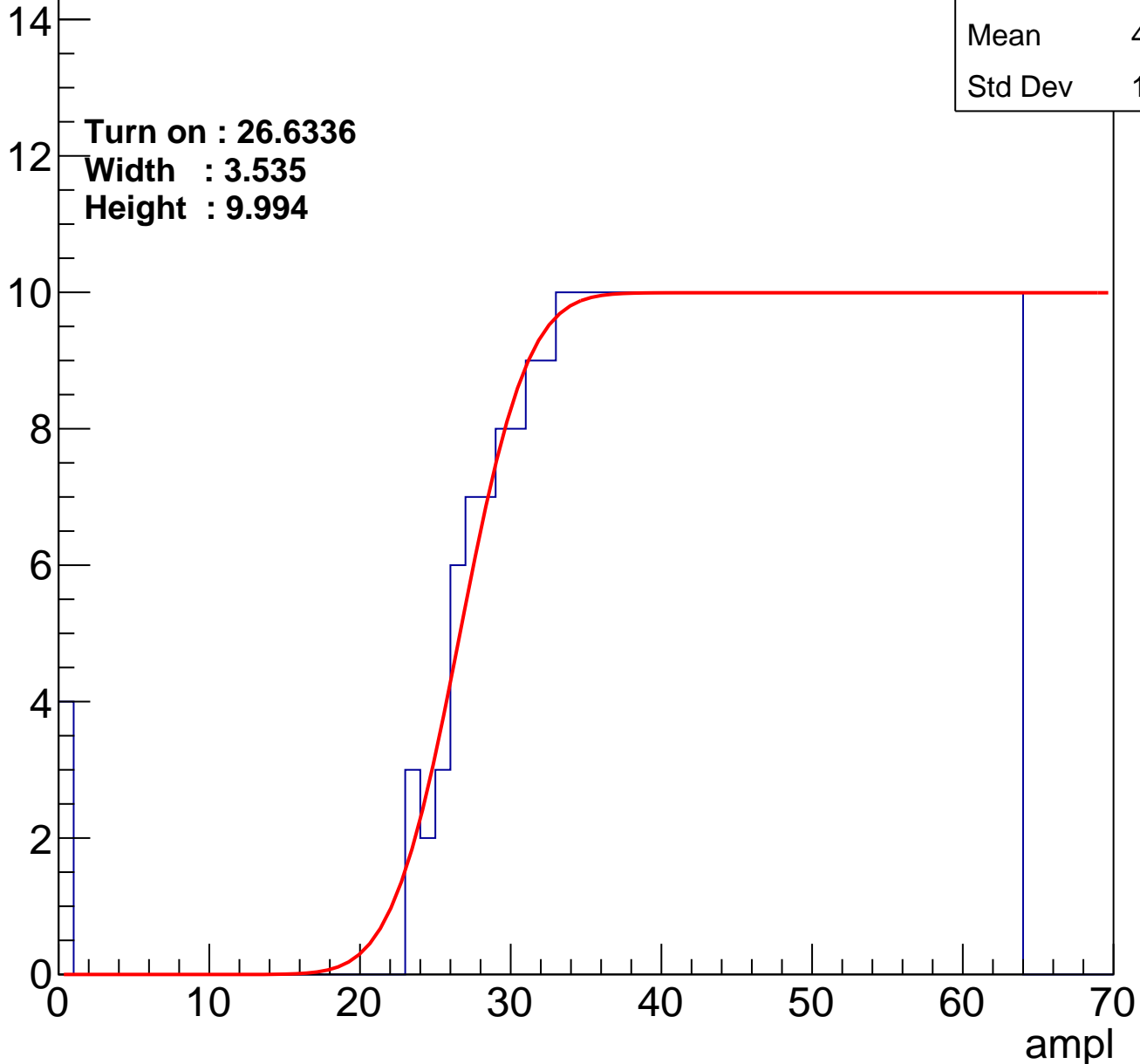
Entries	376
Mean	44.29
Std Dev	11.83

Turn on : 26.6336

Width : 3.535

Height : 9.994

Entry



B1L101S, U14-ch74

calib_packv5_042523_0143.root, FC#0, port D2

Entries	381
Mean	44.28
Std Dev	11.34

Turn on : 25.8040

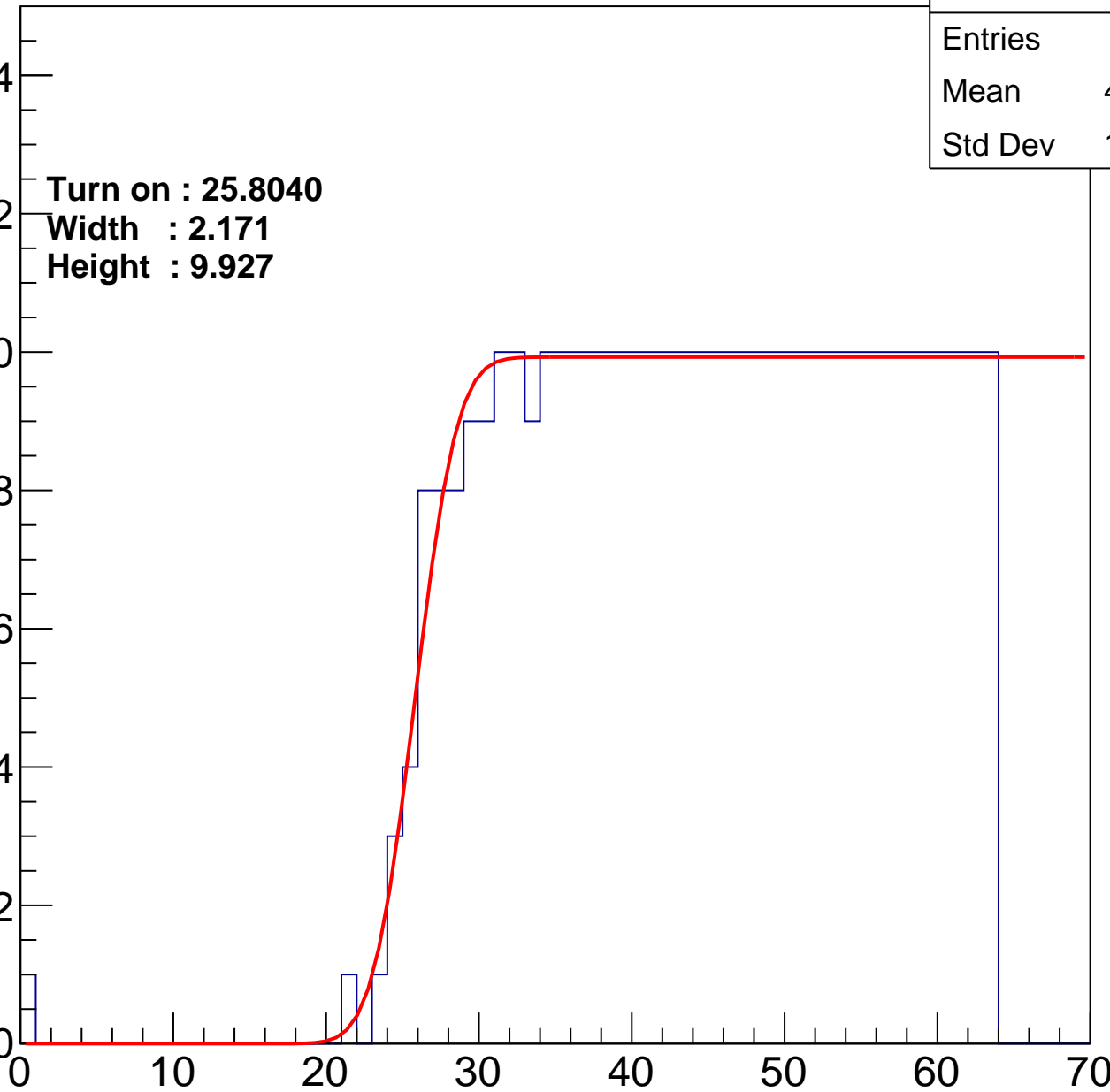
Width : 2.171

Height : 9.927

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch75

calib_packv5_042523_0143.root, FC#0, port D2

Entries	370
Mean	44.63
Std Dev	11.62

Turn on : 27.3318

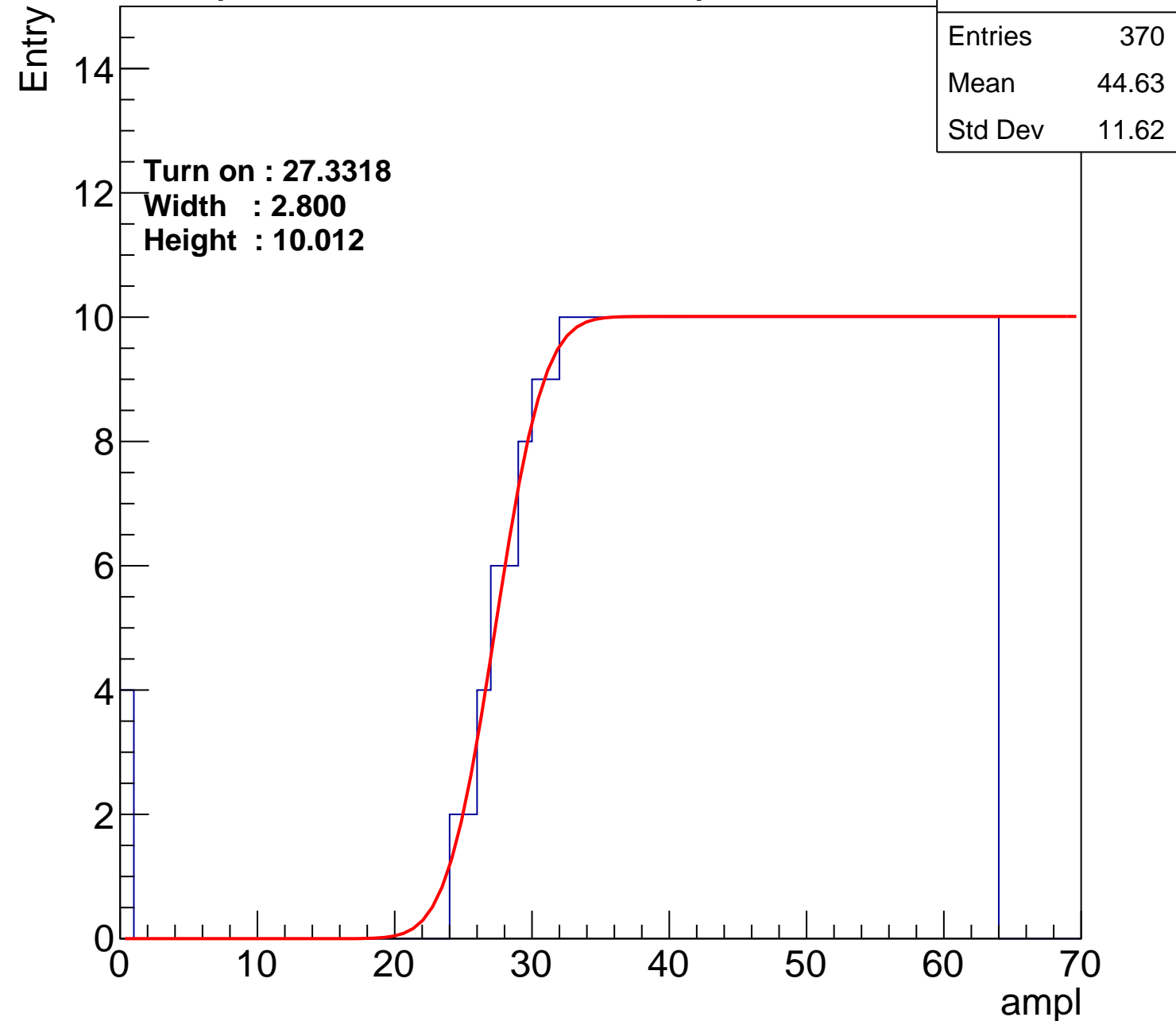
Width : 2.800

Height : 10.012

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch76

calib_packv5_042523_0143.root, FC#0, port D2

Entries	413
Mean	42.53
Std Dev	12.65

Turn on : 23.1291

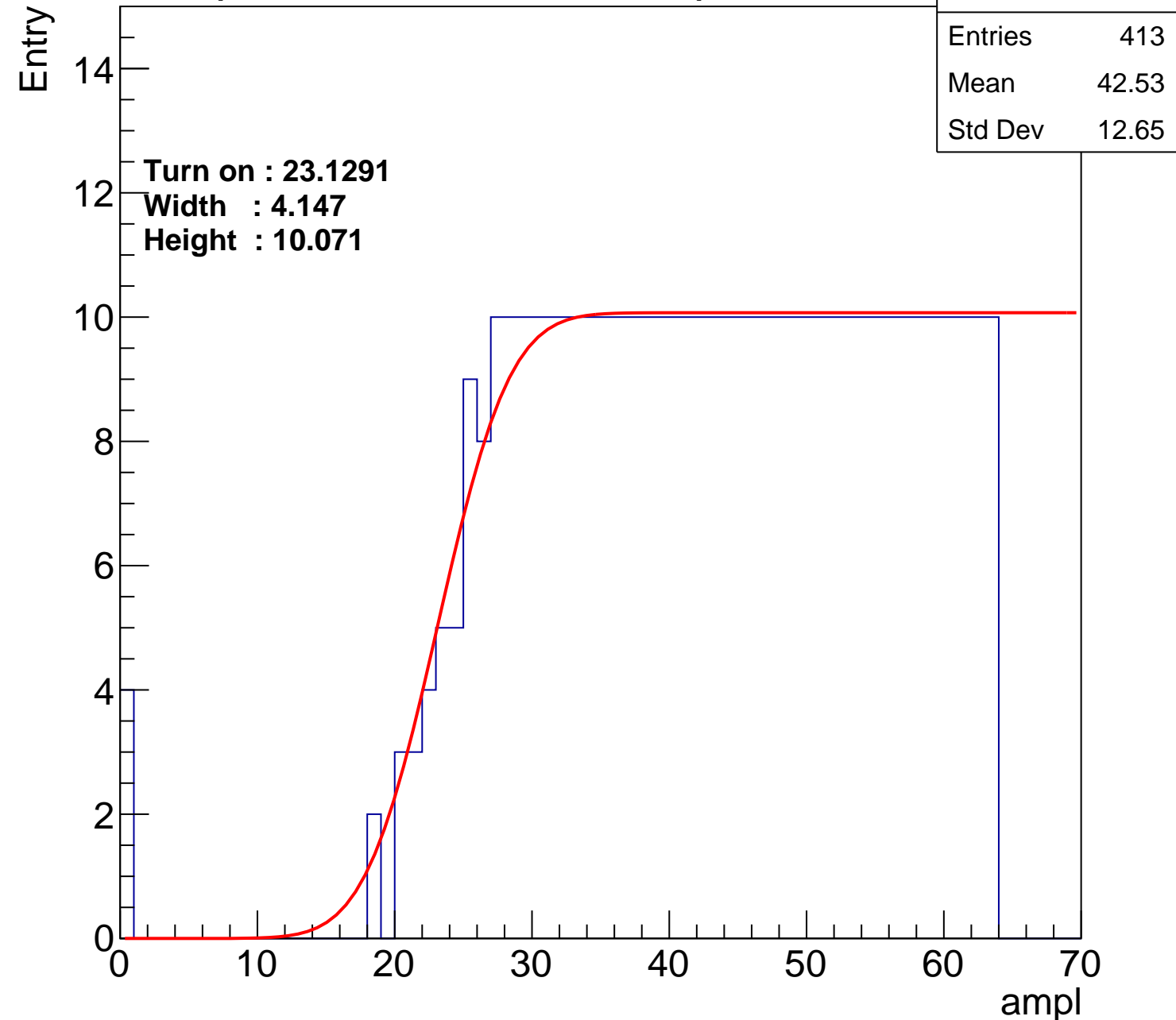
Width : 4.147

Height : 10.071

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch77

calib_packv5_042523_0143.root, FC#0, port D2

Entries	383
Mean	44.11
Std Dev	11.6

Turn on : 25.9778

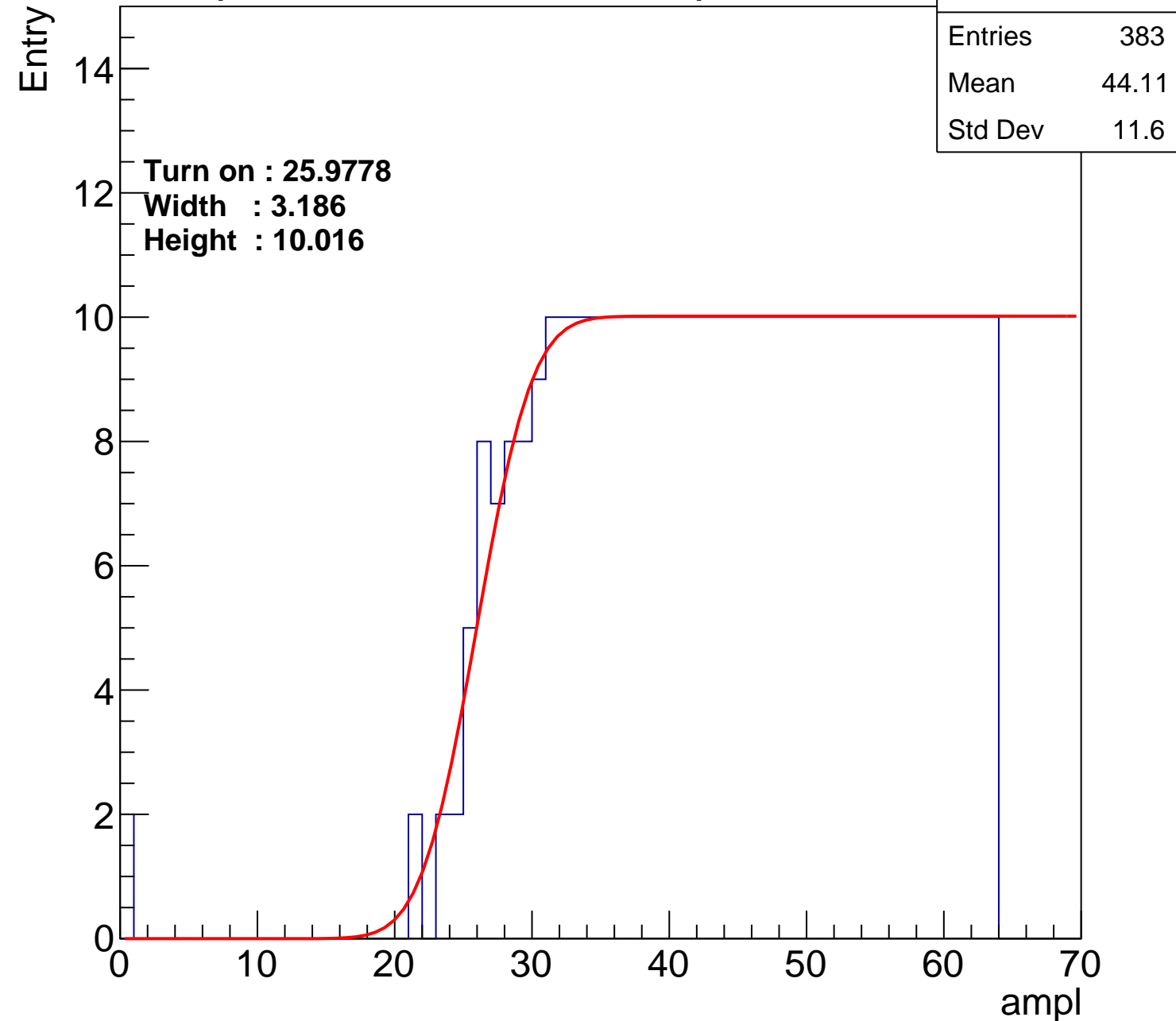
Width : 3.186

Height : 10.016

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch78

calib_packv5_042523_0143.root, FC#0, port D2

Entries	377
Mean	44.37
Std Dev	11.59

Turn on : 26.6551

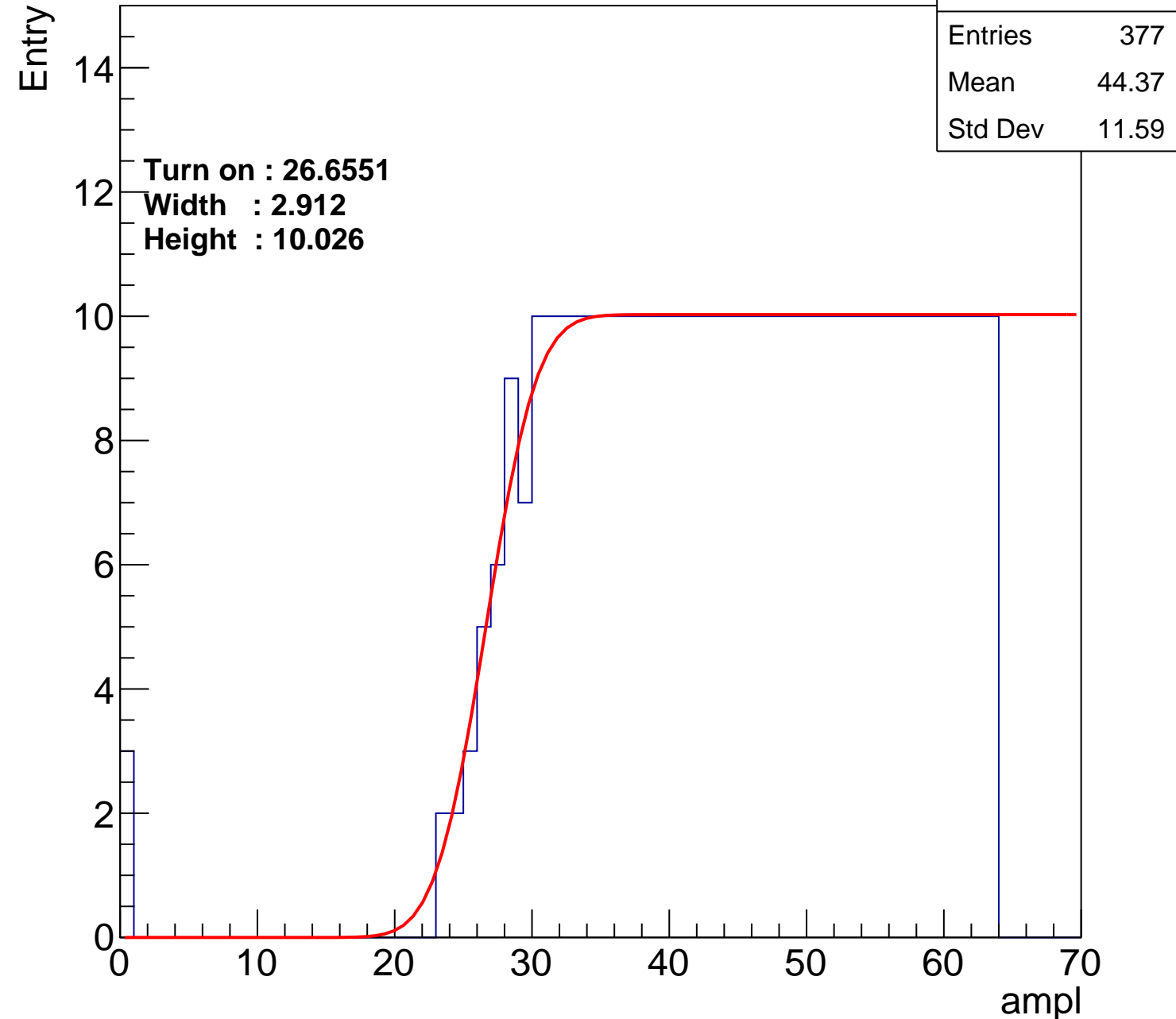
Width : 2.912

Height : 10.026

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch79

calib_packv5_042523_0143.root, FC#0, port D2

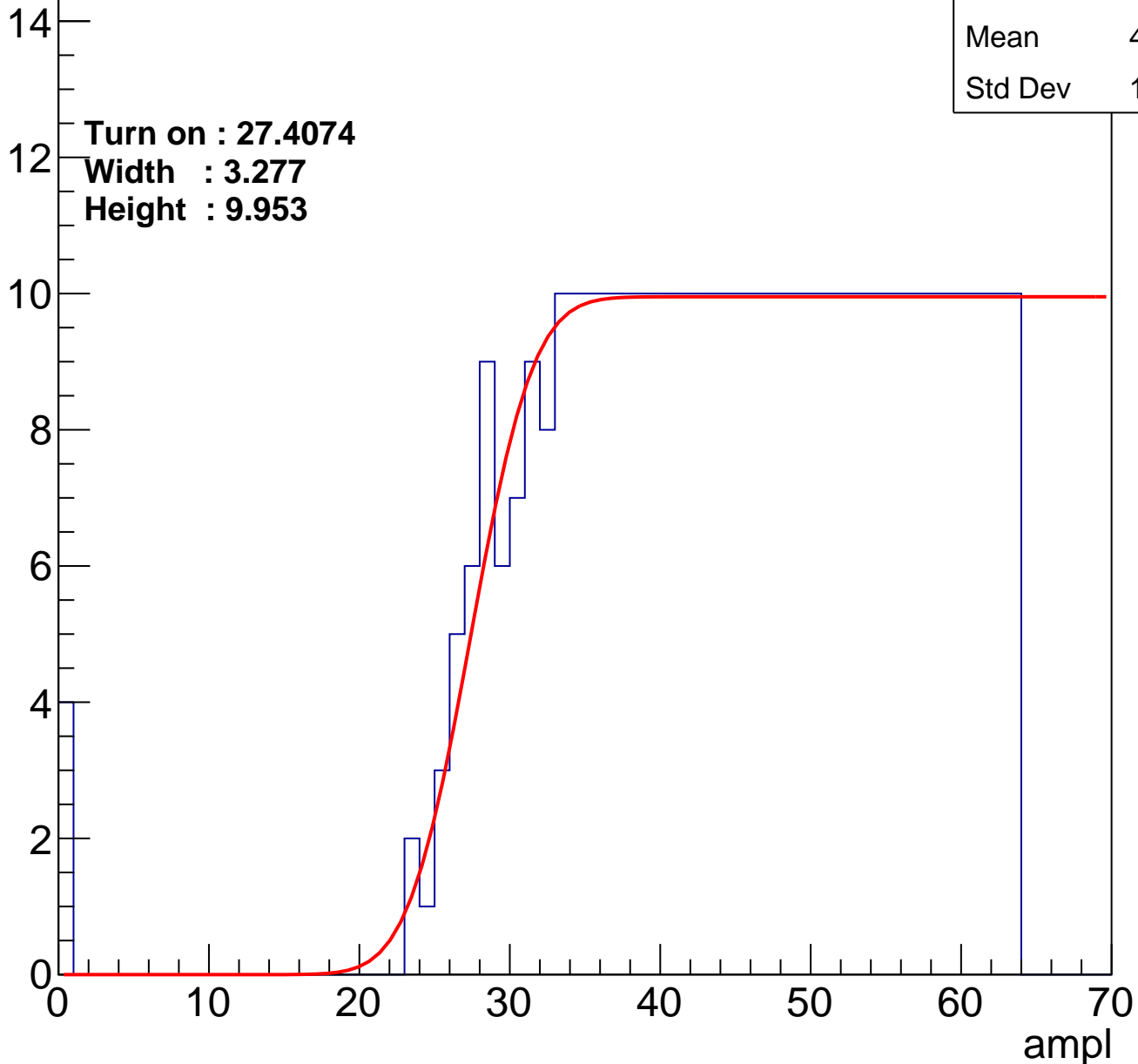
Entries	370
Mean	44.56
Std Dev	11.72

Turn on : 27.4074

Width : 3.277

Height : 9.953

Entry



B1L101S, U14-ch80

calib_packv5_042523_0143.root, FC#0, port D2

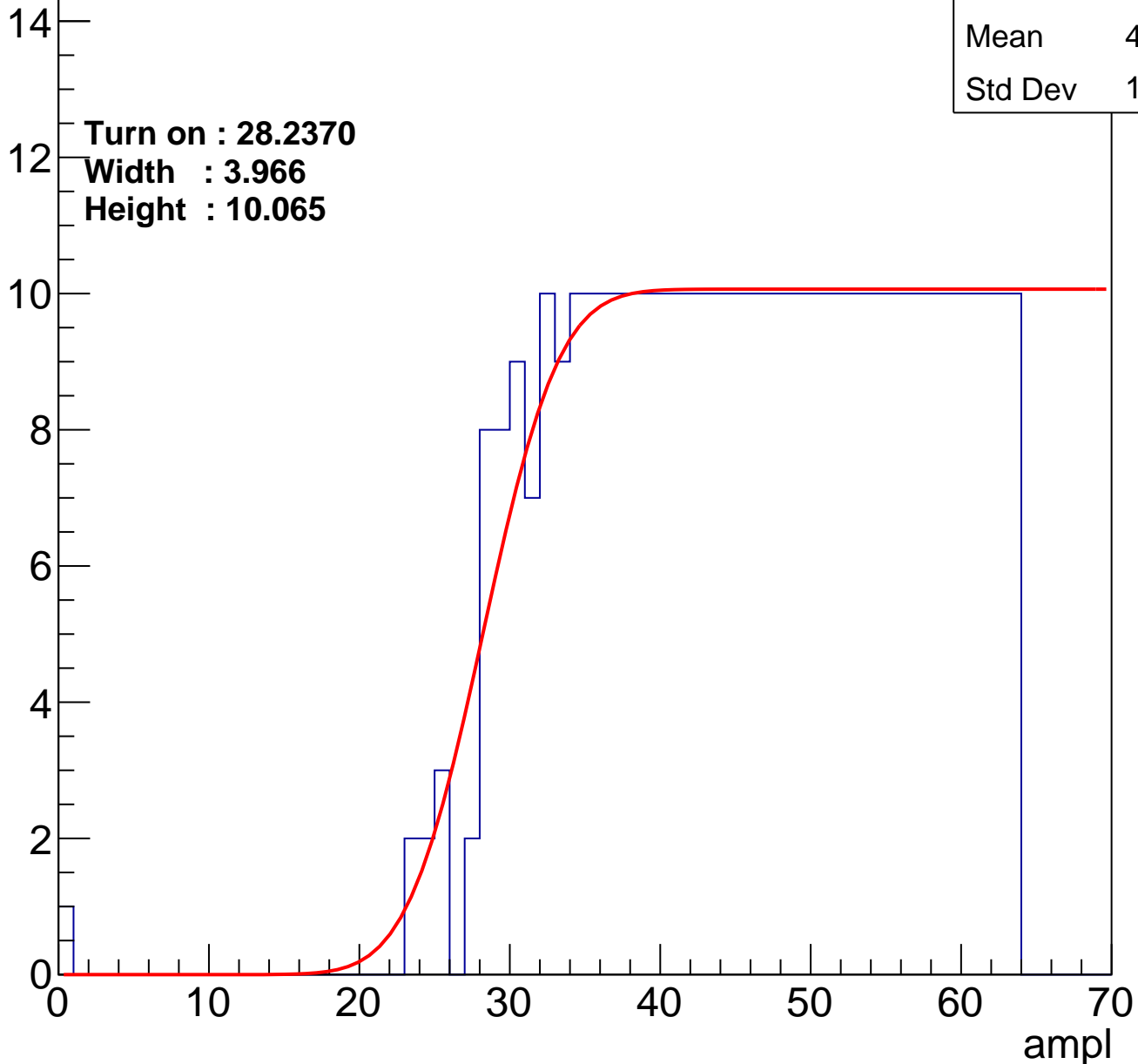
Entries	361
Mean	45.24
Std Dev	10.86

Turn on : 28.2370

Width : 3.966

Height : 10.065

Entry



B1L101S, U14-ch81

calib_packv5_042523_0143.root, FC#0, port D2

Entries	368
Mean	44.74
Std Dev	11.39

Turn on : 27.5729

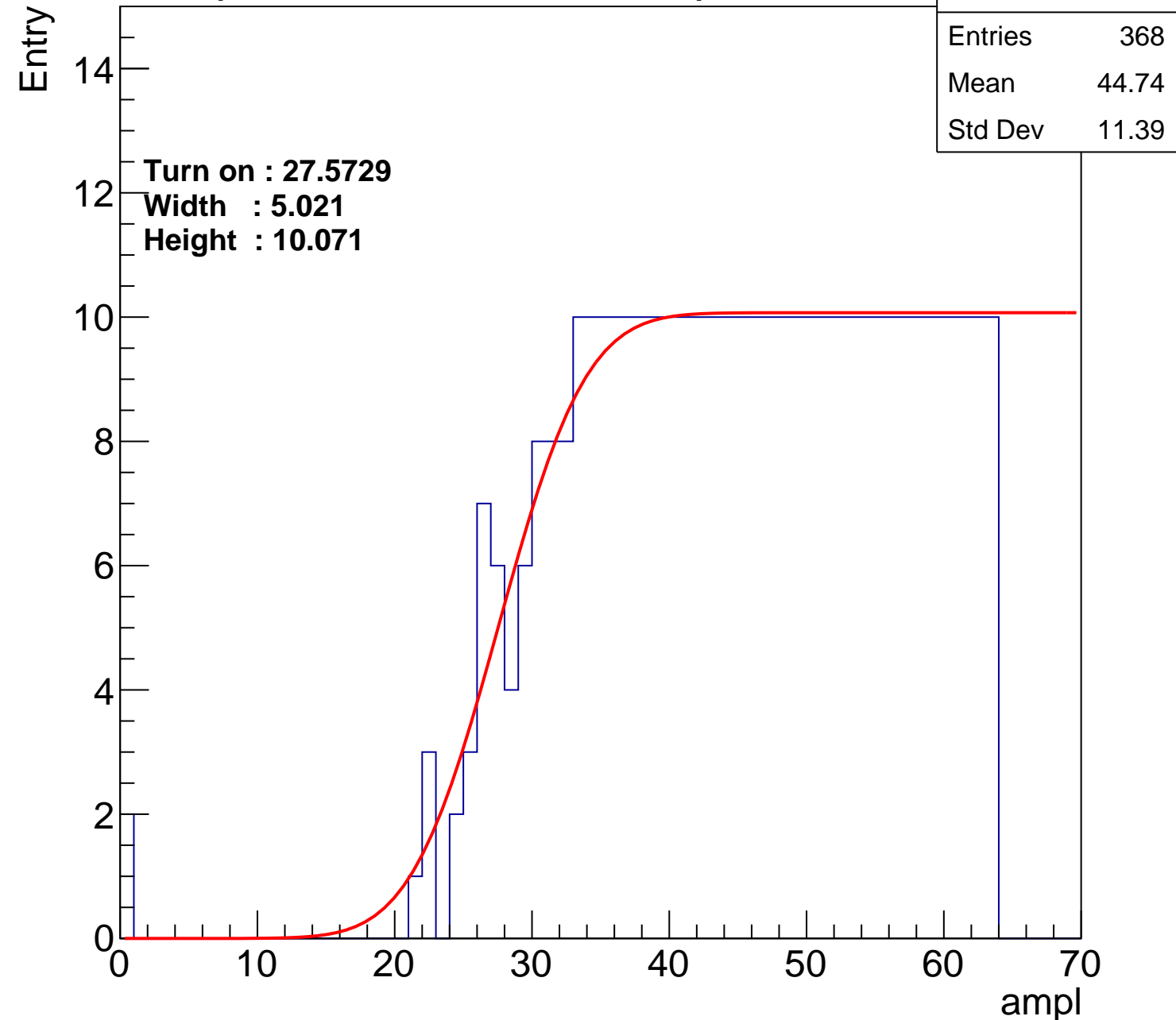
Width : 5.021

Height : 10.071

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch82

calib_packv5_042523_0143.root, FC#0, port D2

Entries	386
Mean	43.76
Std Dev	12.19

Turn on : 25.9596

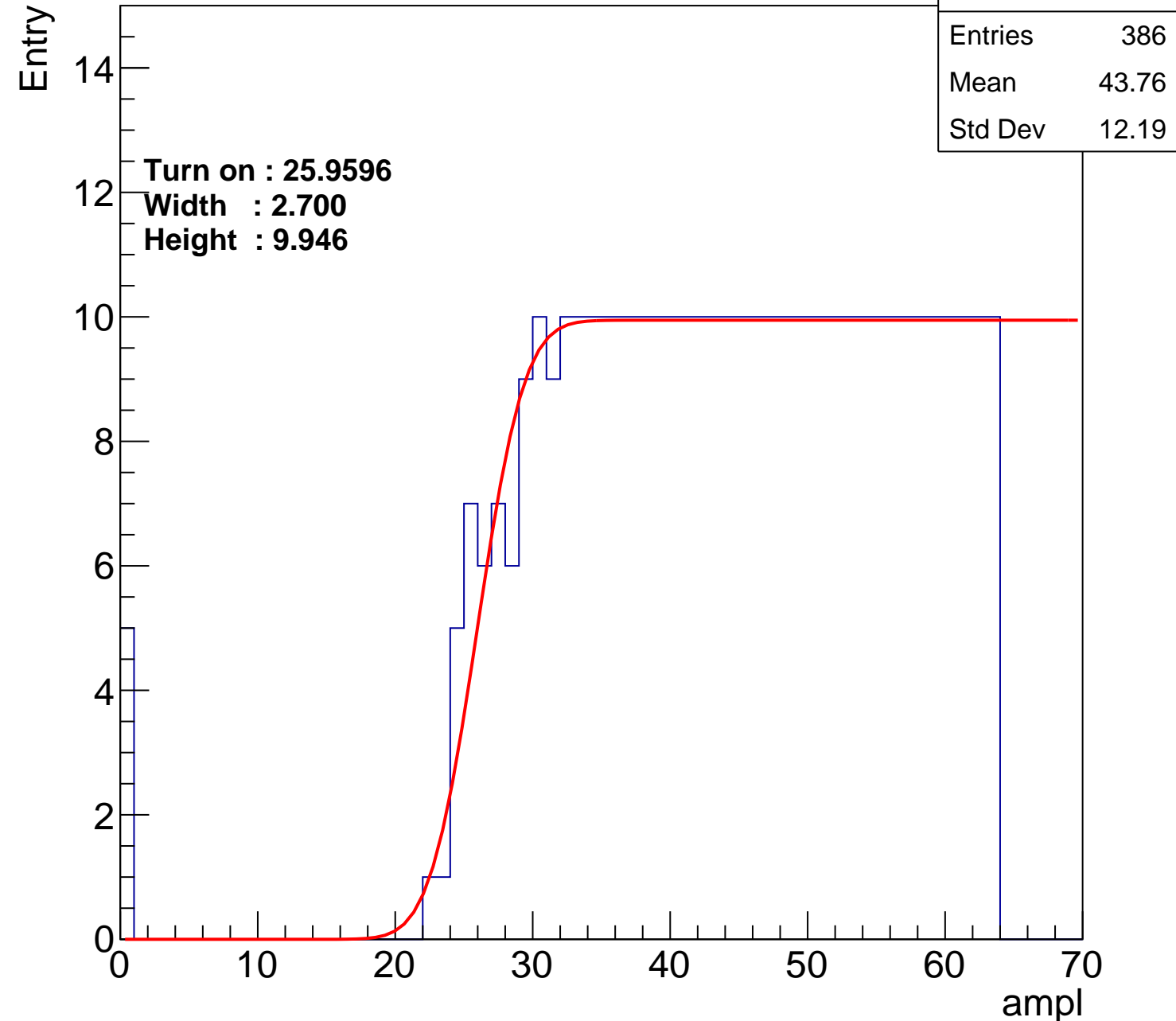
Width : 2.700

Height : 9.946

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch83

calib_packv5_042523_0143.root, FC#0, port D2

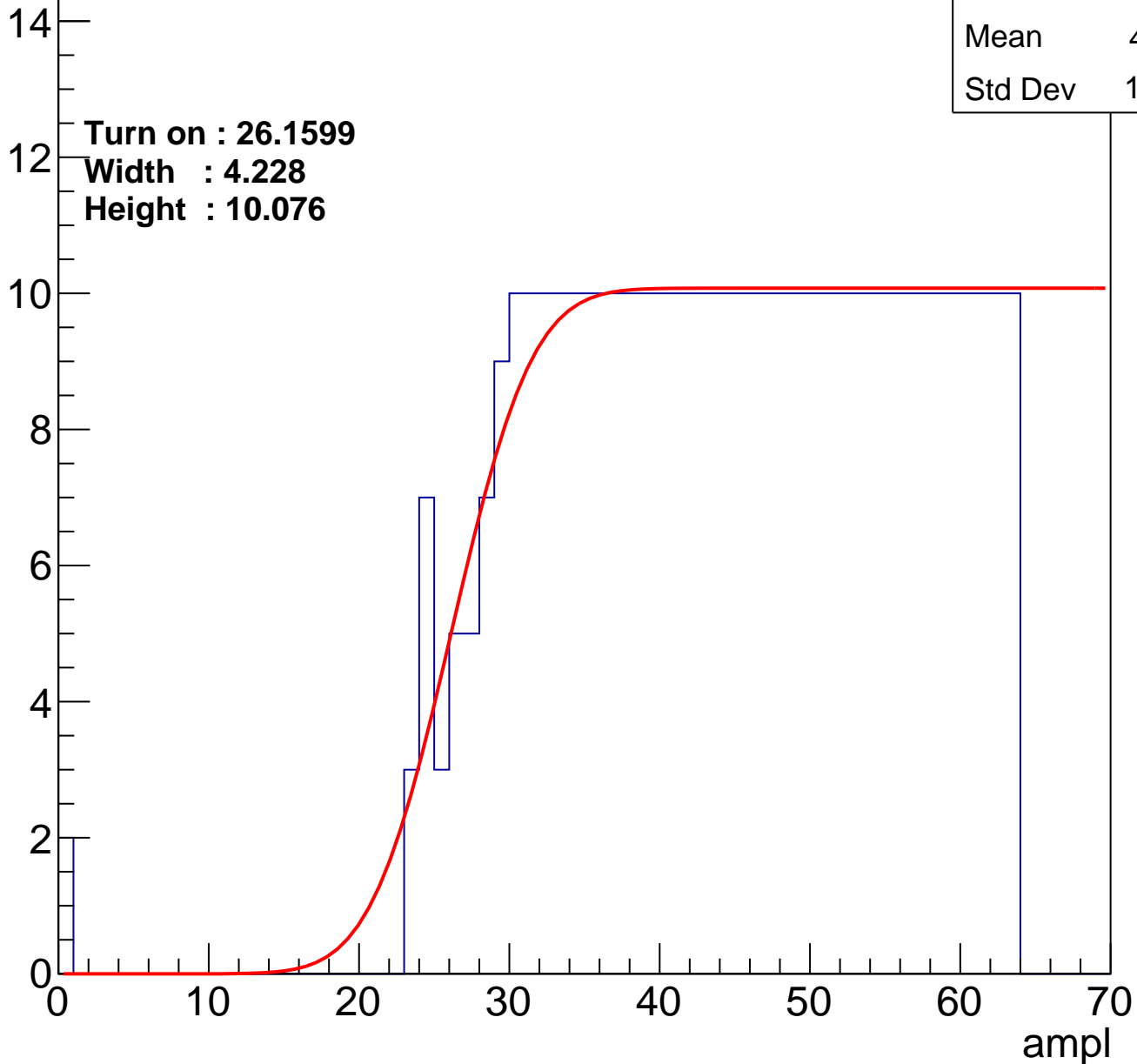
Entries	381
Mean	44.21
Std Dev	11.55

Turn on : 26.1599

Width : 4.228

Height : 10.076

Entry



B1L101S, U14-ch84

calib_packv5_042523_0143.root, FC#0, port D2

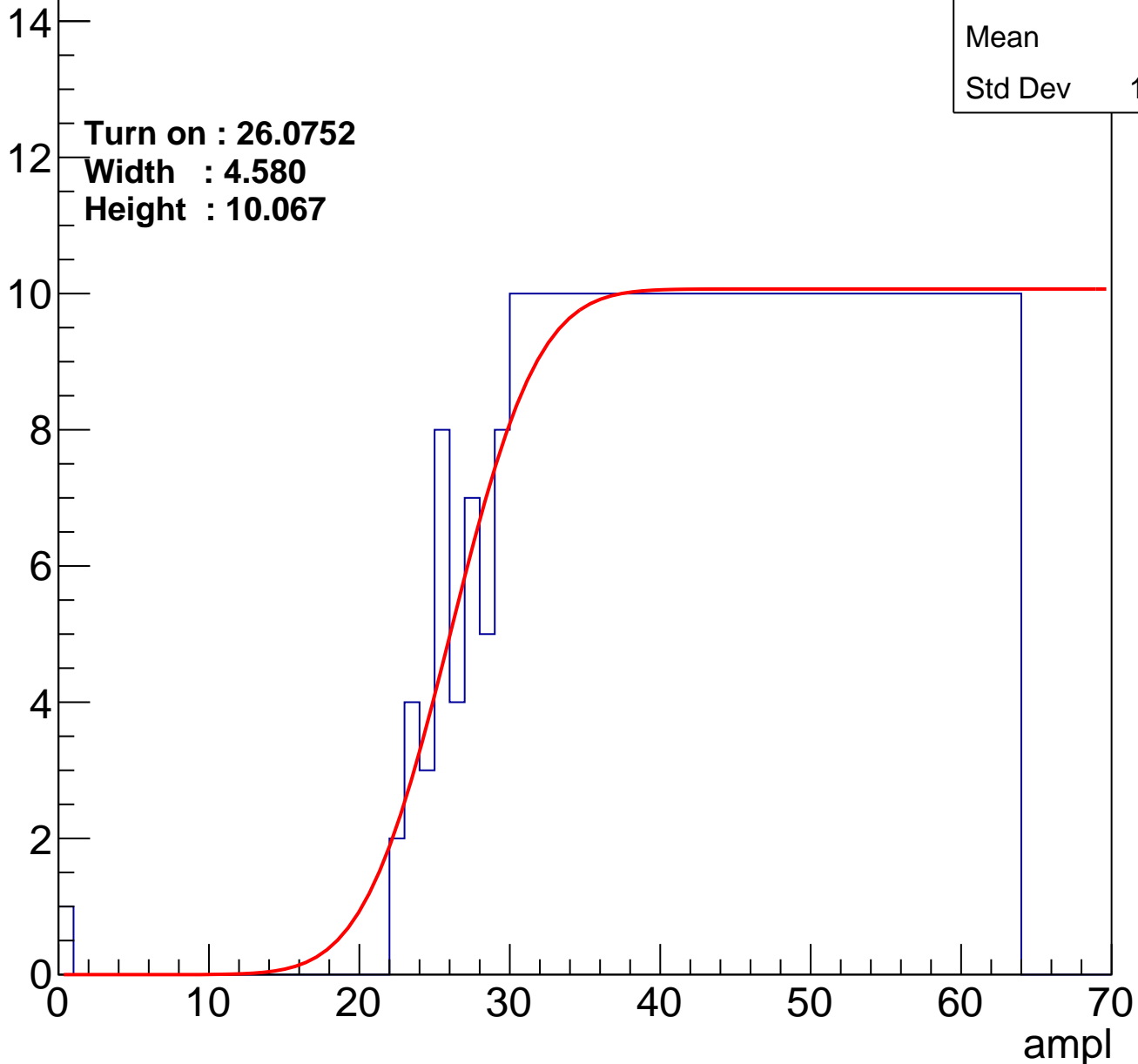
Entries	382
Mean	44.2
Std Dev	11.44

Turn on : 26.0752

Width : 4.580

Height : 10.067

Entry



B1L101S, U14-ch85

calib_packv5_042523_0143.root, FC#0, port D2

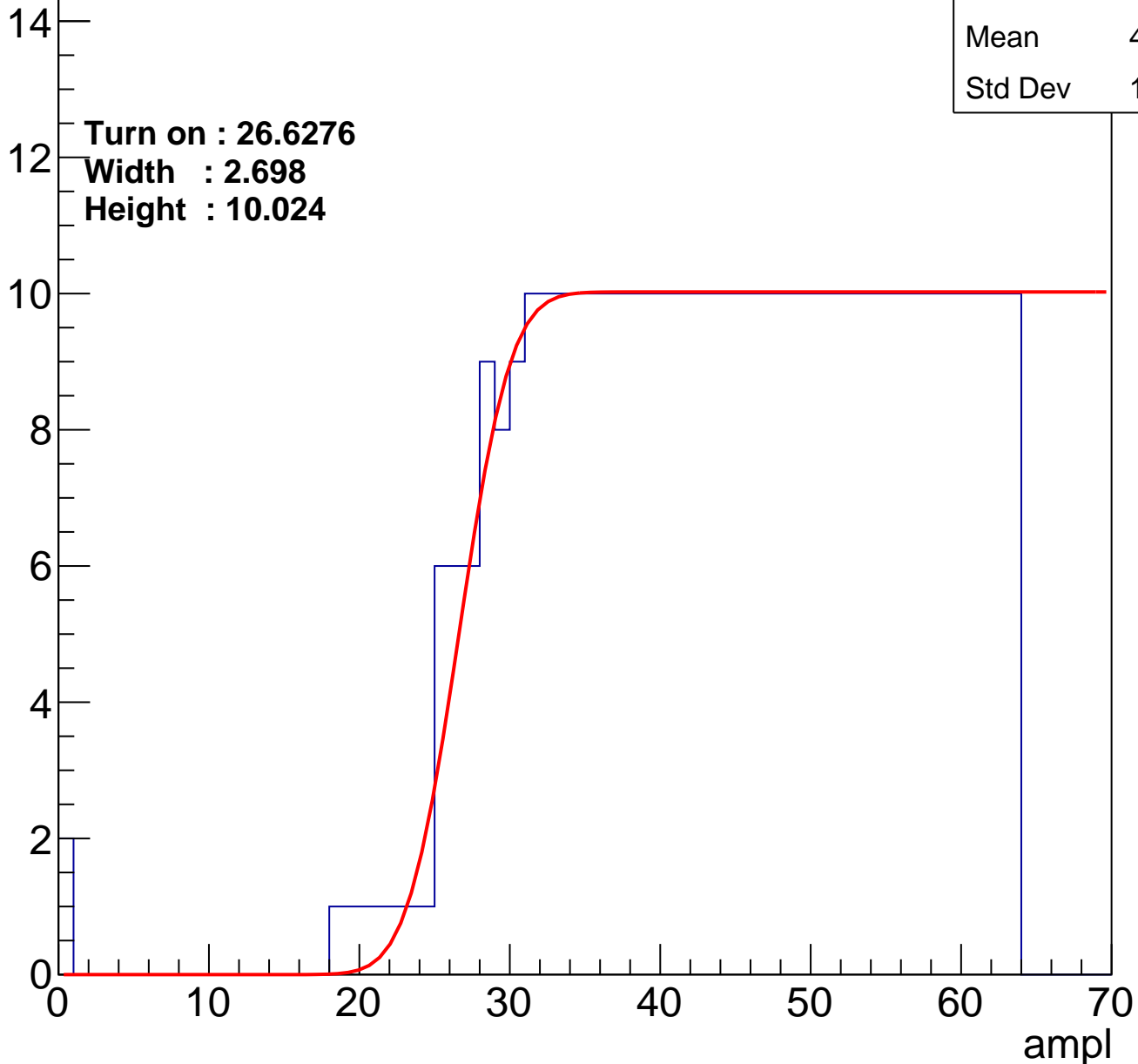
Entries	383
Mean	44.07
Std Dev	11.67

Turn on : 26.6276

Width : 2.698

Height : 10.024

Entry



B1L101S, U14-ch86

calib_packv5_042523_0143.root, FC#0, port D2

Entries	387
Mean	43.58
Std Dev	12.48

Turn on : 25.7525

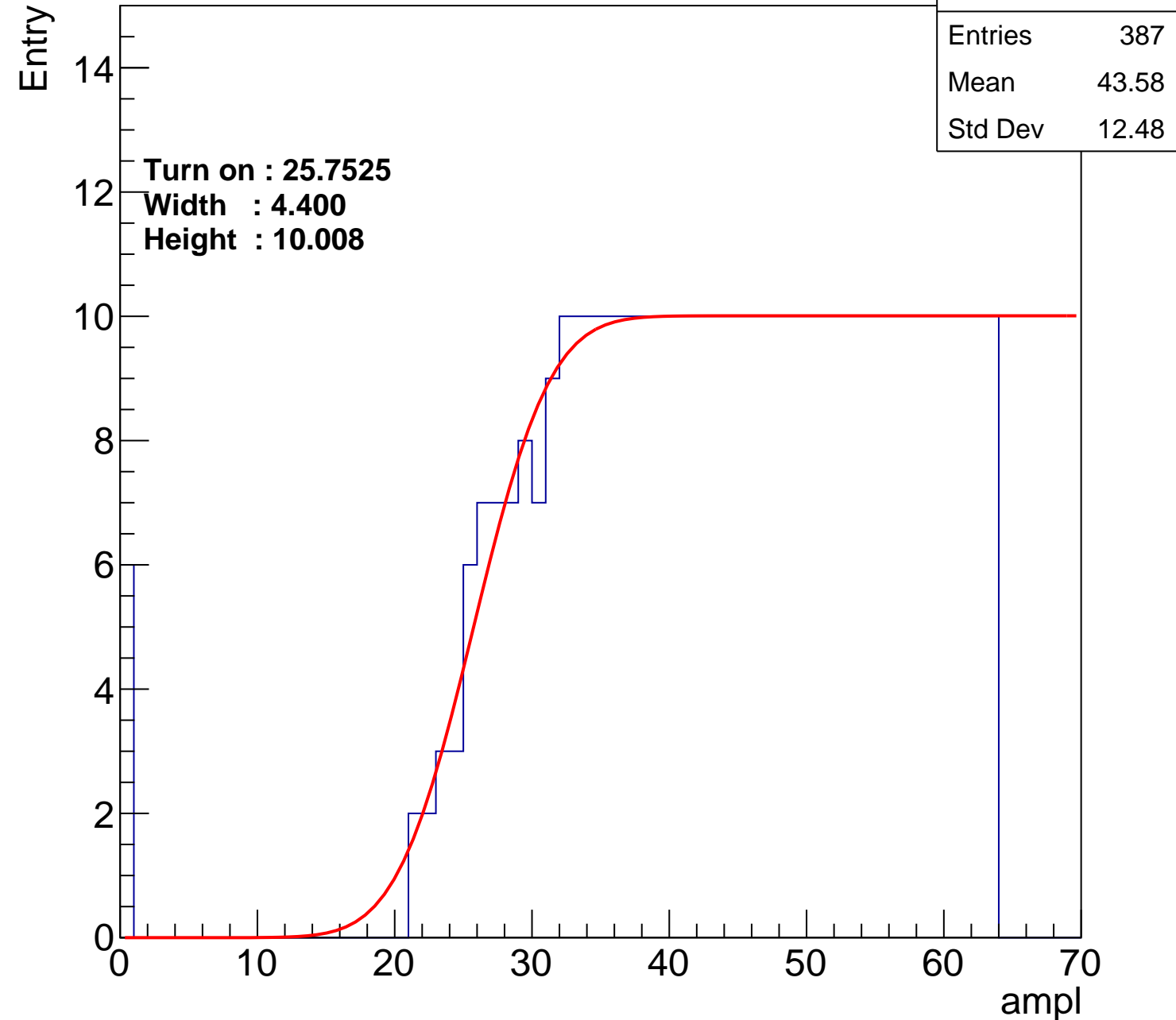
Width : 4.400

Height : 10.008

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch87

calib_packv5_042523_0143.root, FC#0, port D2

Entries	385
Mean	43.88
Std Dev	12

Turn on : 26.4337

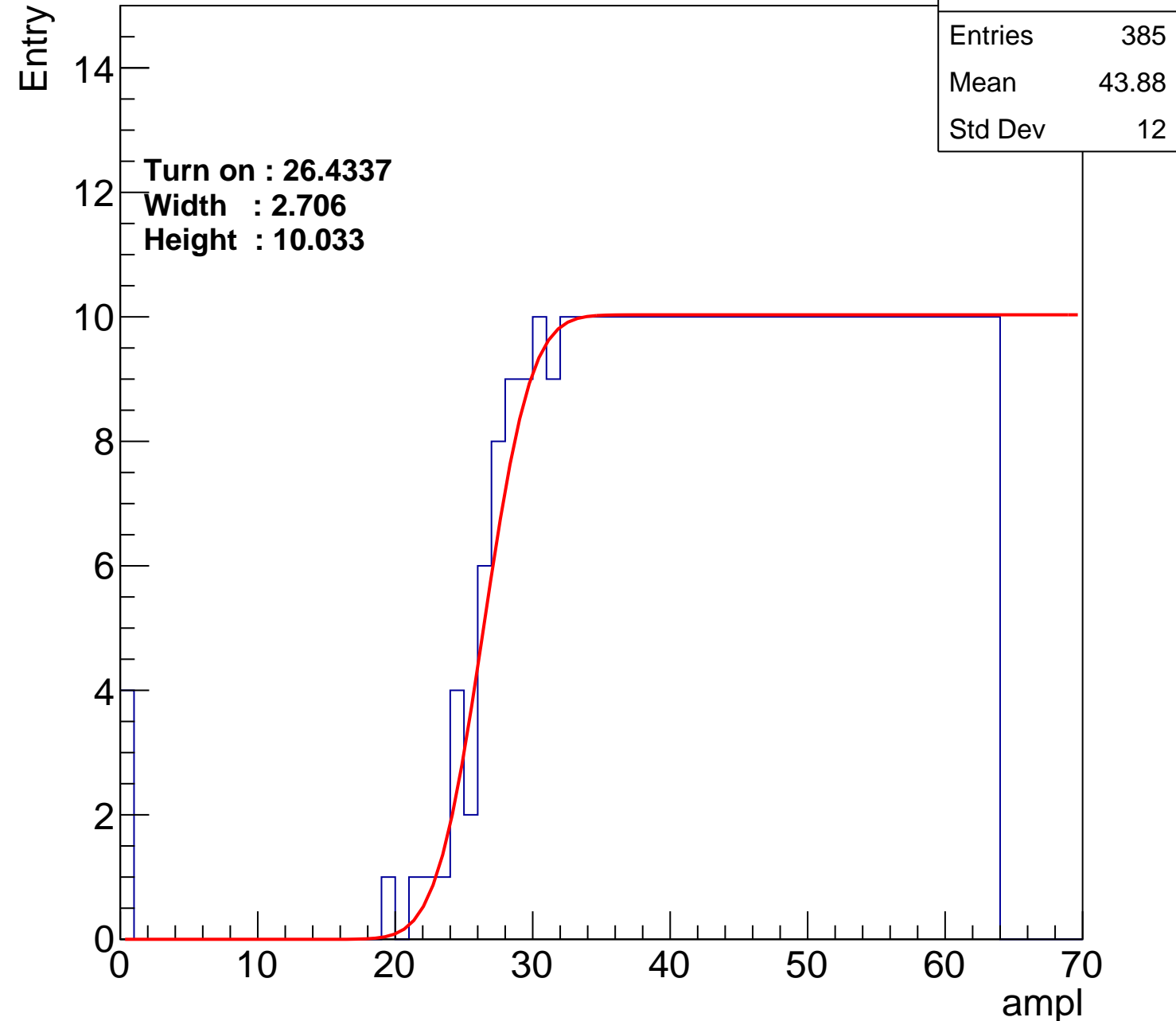
Width : 2.706

Height : 10.033

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch88

calib_packv5_042523_0143.root, FC#0, port D2

Entries	379
Mean	44.14
Std Dev	11.9

Turn on : 26.1563

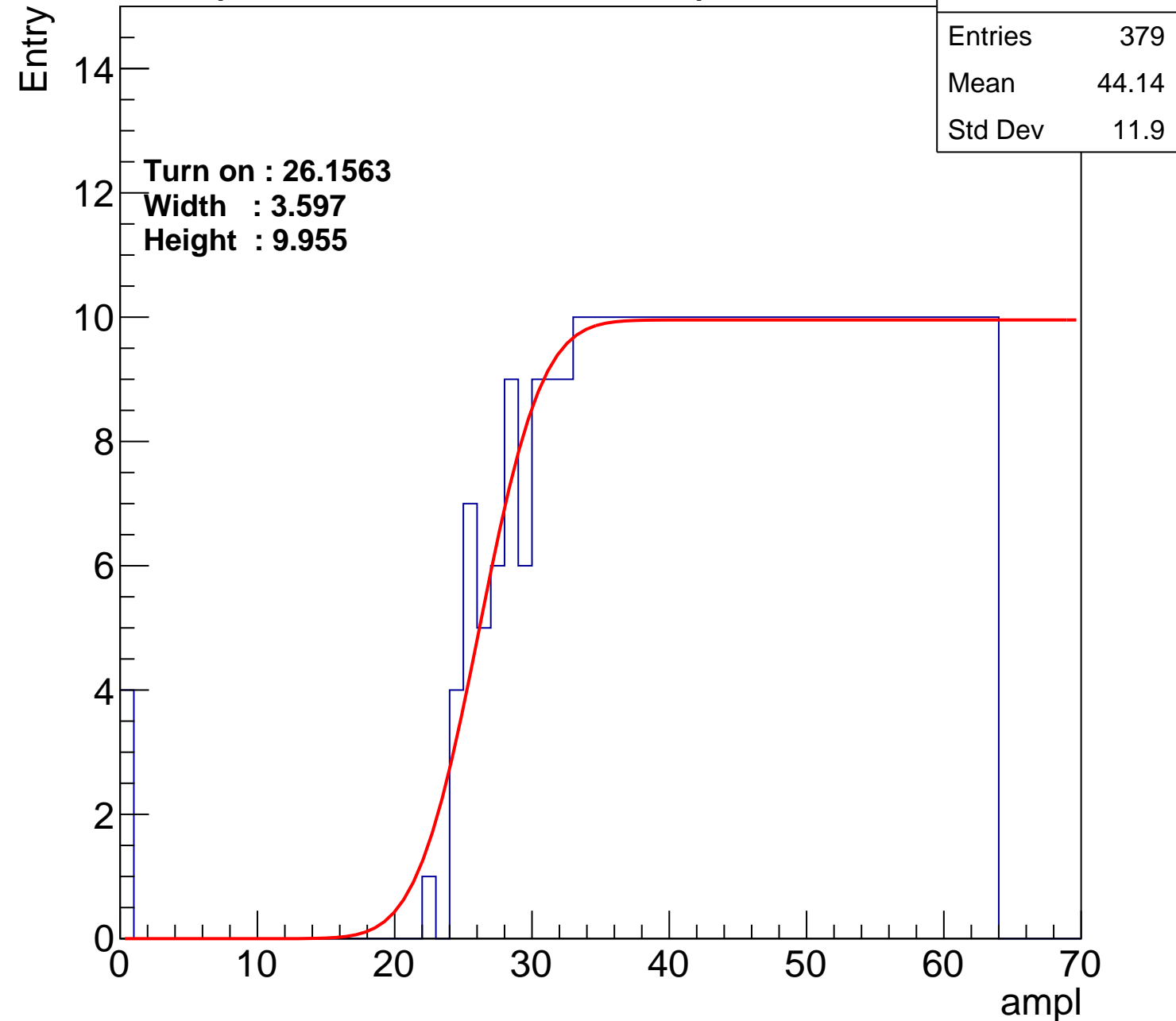
Width : 3.597

Height : 9.955

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch89

calib_packv5_042523_0143.root, FC#0, port D2

Entries	380
Mean	43.97
Std Dev	12.25

Turn on : 26.8643

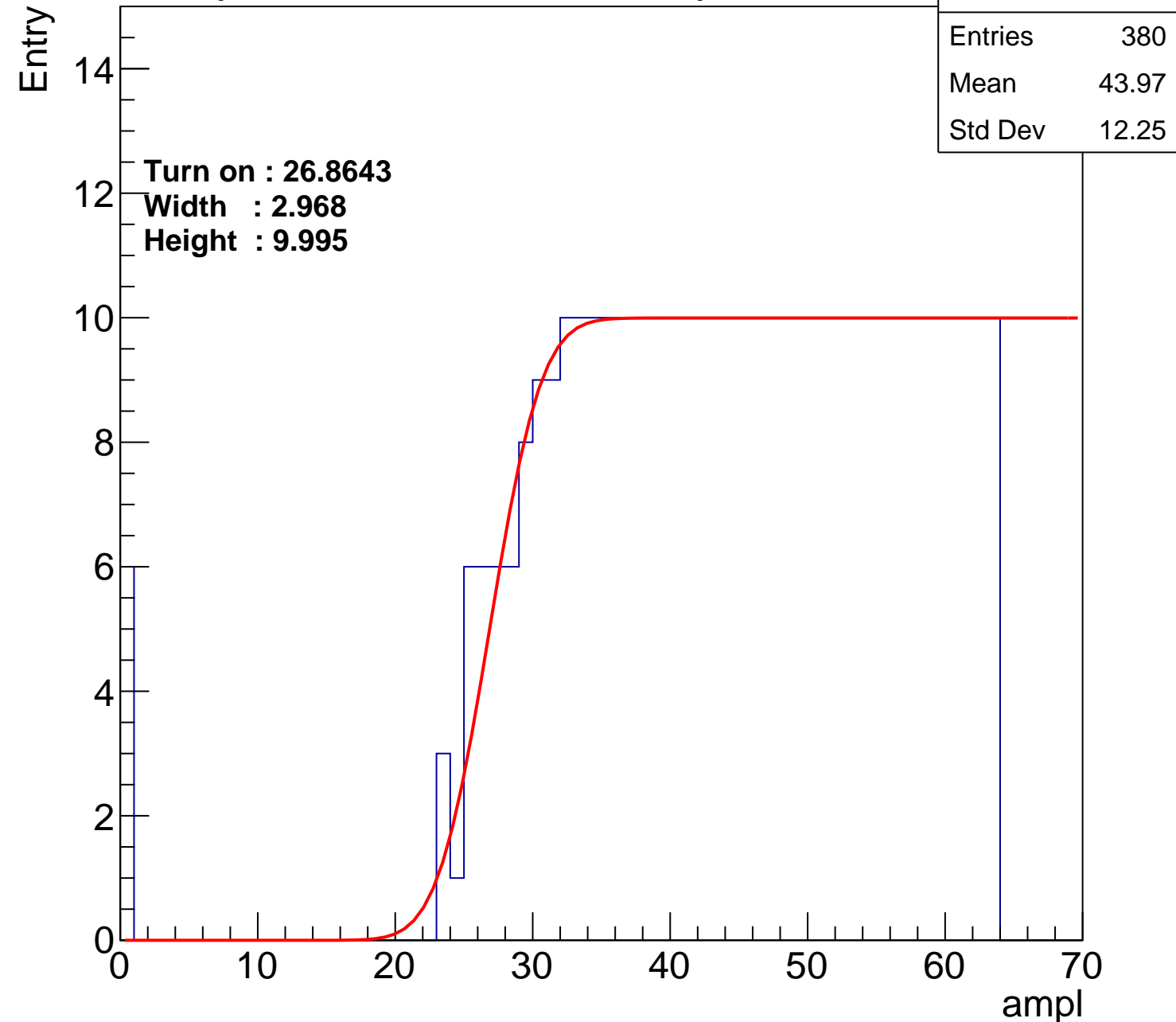
Width : 2.968

Height : 9.995

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch90

calib_packv5_042523_0143.root, FC#0, port D2

Entries	385
Mean	43.93
Std Dev	11.86

Turn on : 26.0622

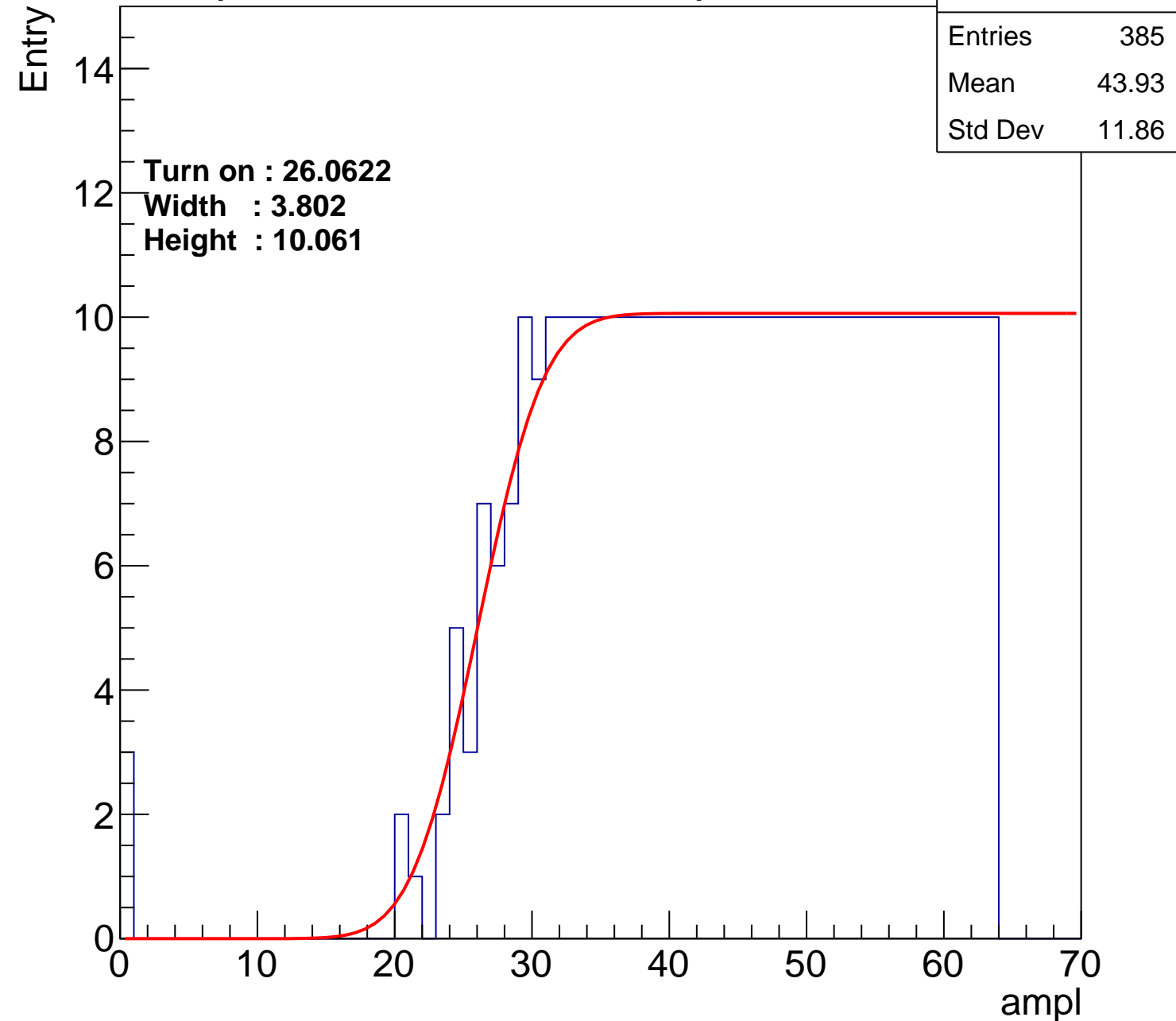
Width : 3.802

Height : 10.061

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch91

calib_packv5_042523_0143.root, FC#0, port D2

Entries	379
Mean	44.11
Std Dev	11.94

Turn on : 26.5944

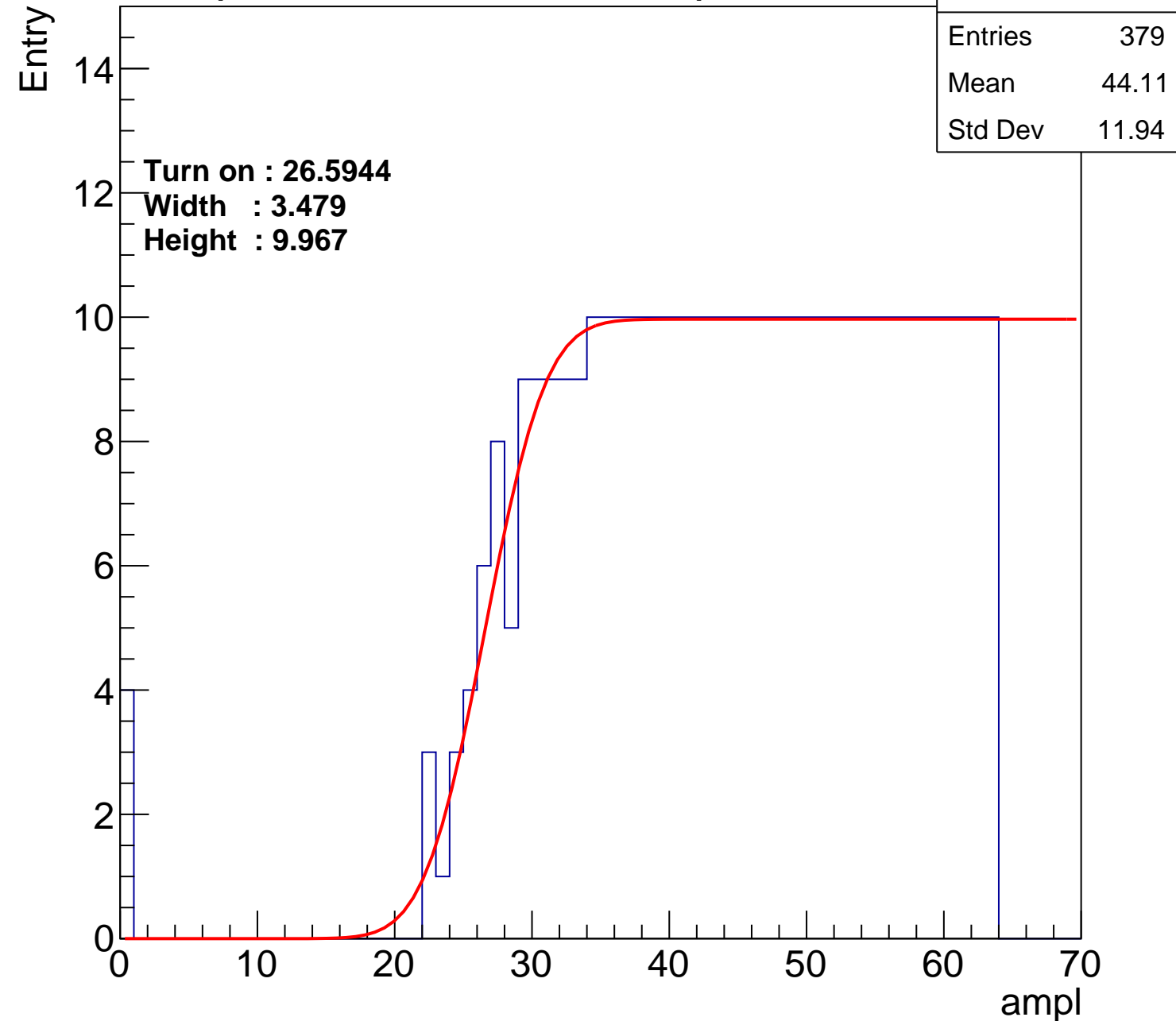
Width : 3.479

Height : 9.967

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch92

calib_packv5_042523_0143.root, FC#0, port D2

Entries	388
Mean	43.79
Std Dev	11.92

Turn on : 25.3321

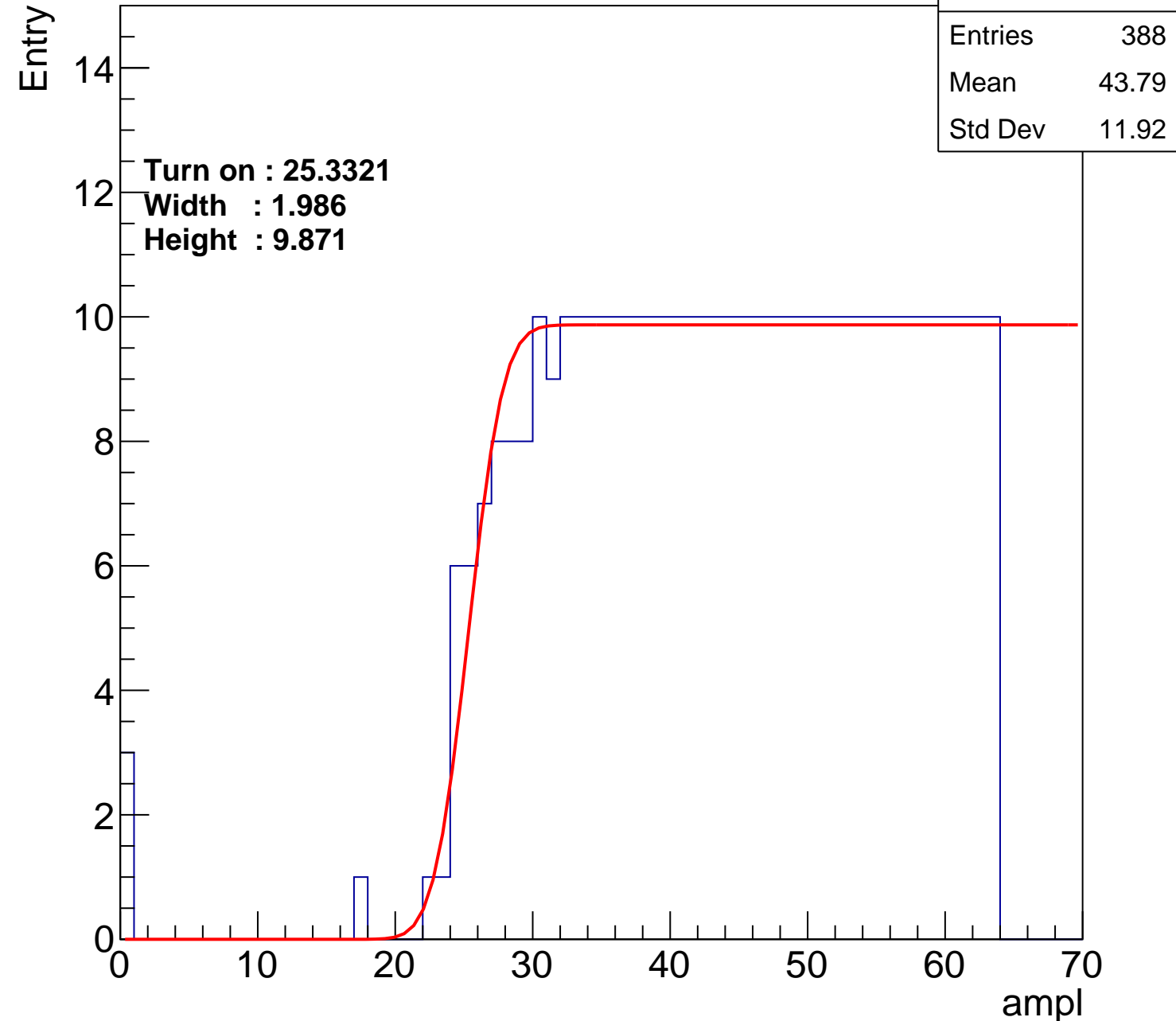
Width : 1.986

Height : 9.871

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch93

calib_packv5_042523_0143.root, FC#0, port D2

Entries	374
Mean	44.6
Std Dev	11.21

Turn on : 26.6740

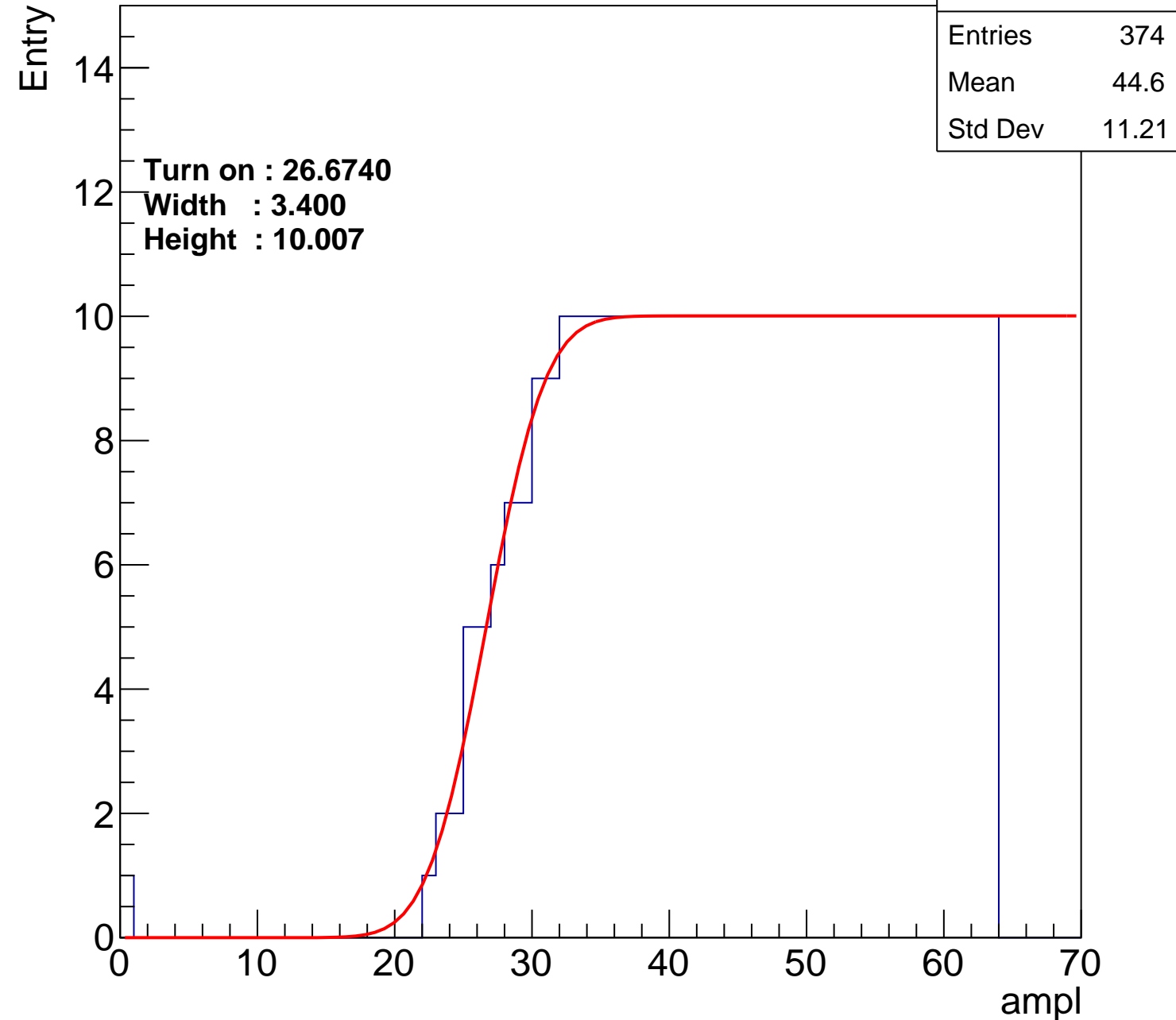
Width : 3.400

Height : 10.007

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch94

calib_packv5_042523_0143.root, FC#0, port D2

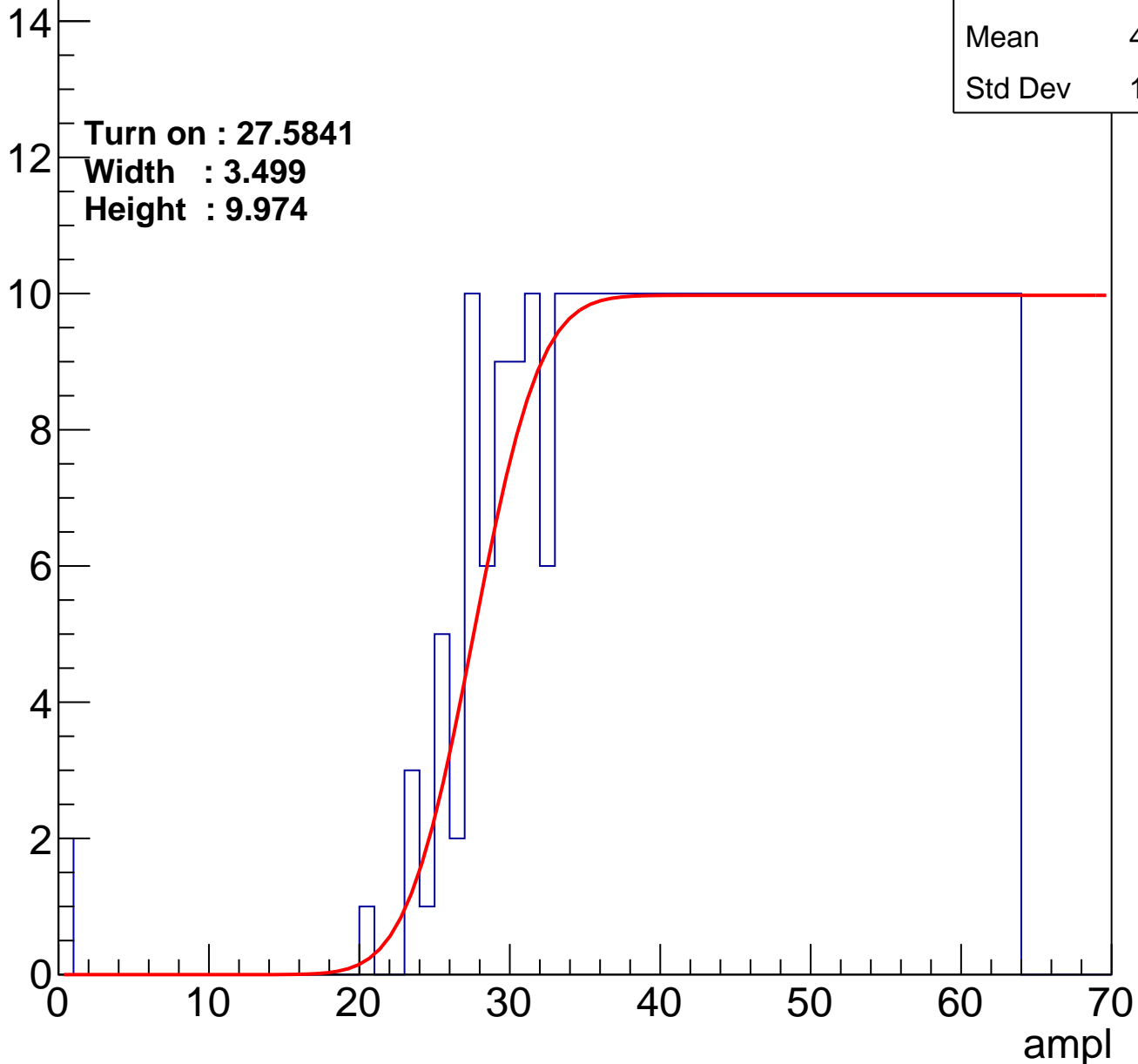
Entries	374
Mean	44.49
Std Dev	11.45

Turn on : 27.5841

Width : 3.499

Height : 9.974

Entry



B1L101S, U14-ch95

calib_packv5_042523_0143.root, FC#0, port D2

Entries	360
Mean	45.02
Std Dev	11.56

Turn on : 29.0776

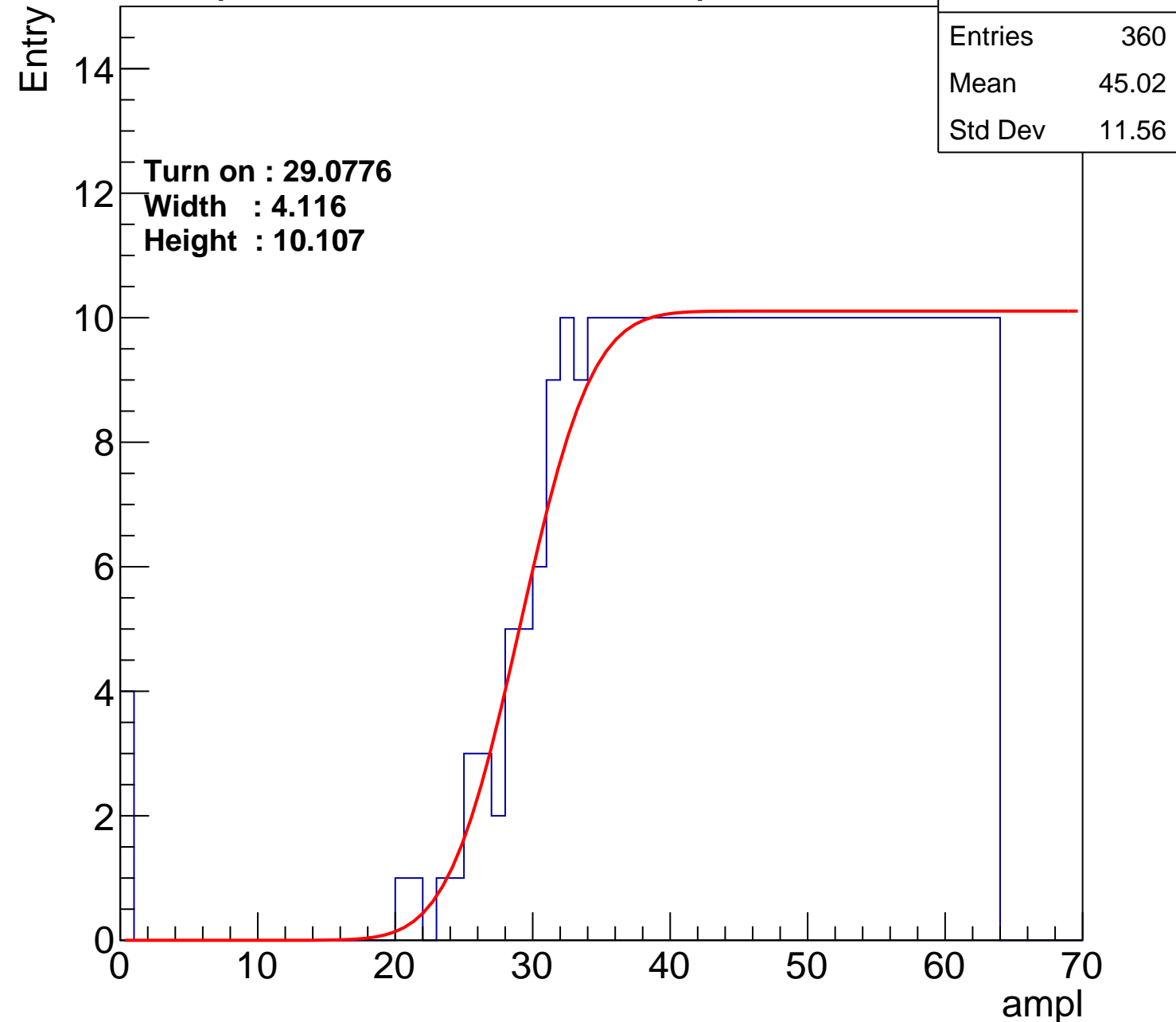
Width : 4.116

Height : 10.107

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch96

calib_packv5_042523_0143.root, FC#0, port D2

Entries	371
Mean	44.61
Std Dev	11.51

Turn on : 27.6153

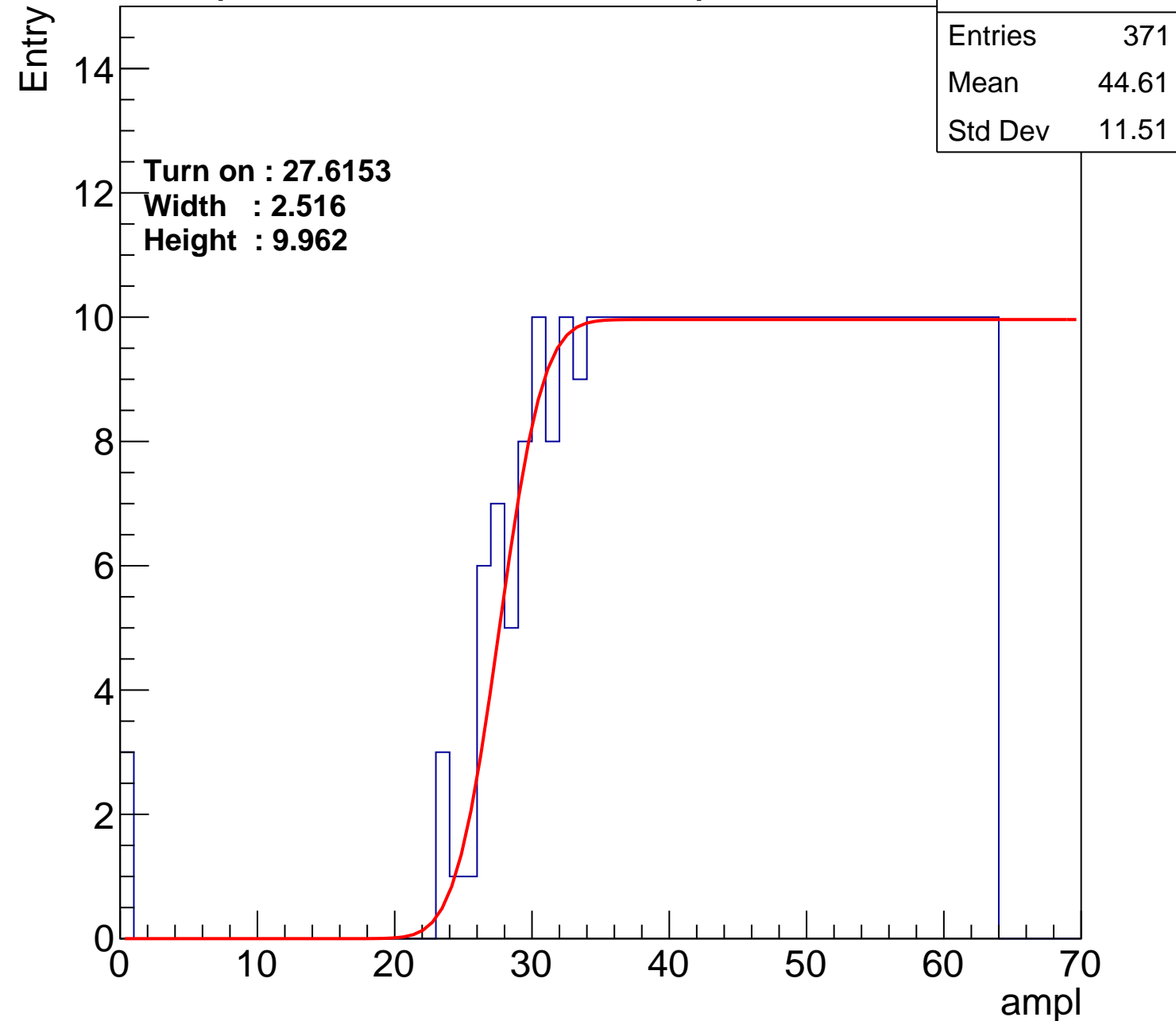
Width : 2.516

Height : 9.962

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch97

calib_packv5_042523_0143.root, FC#0, port D2

Entries	364
Mean	45.12
Std Dev	10.9

Turn on : 28.3534

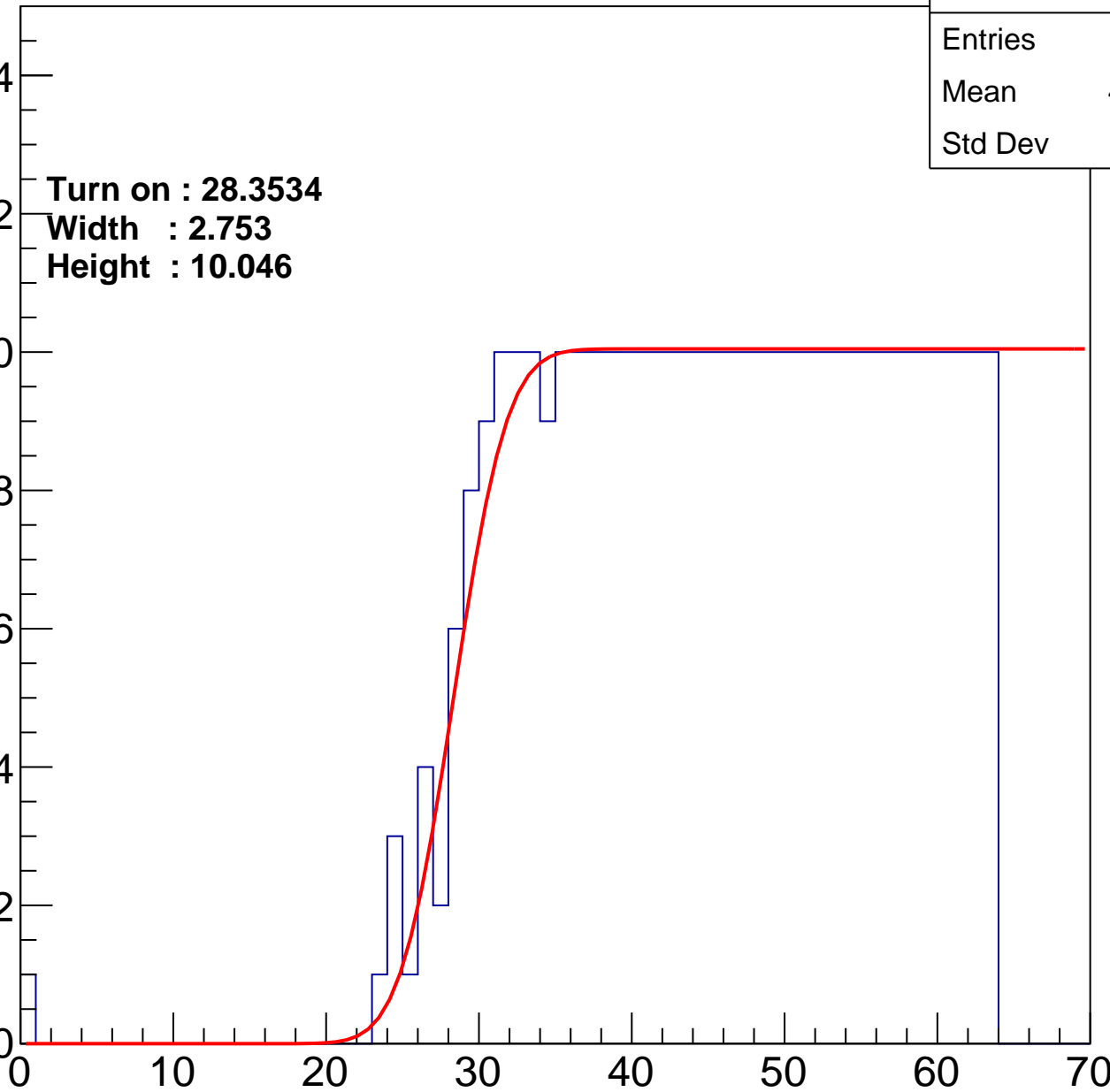
Width : 2.753

Height : 10.046

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch98

calib_packv5_042523_0143.root, FC#0, port D2

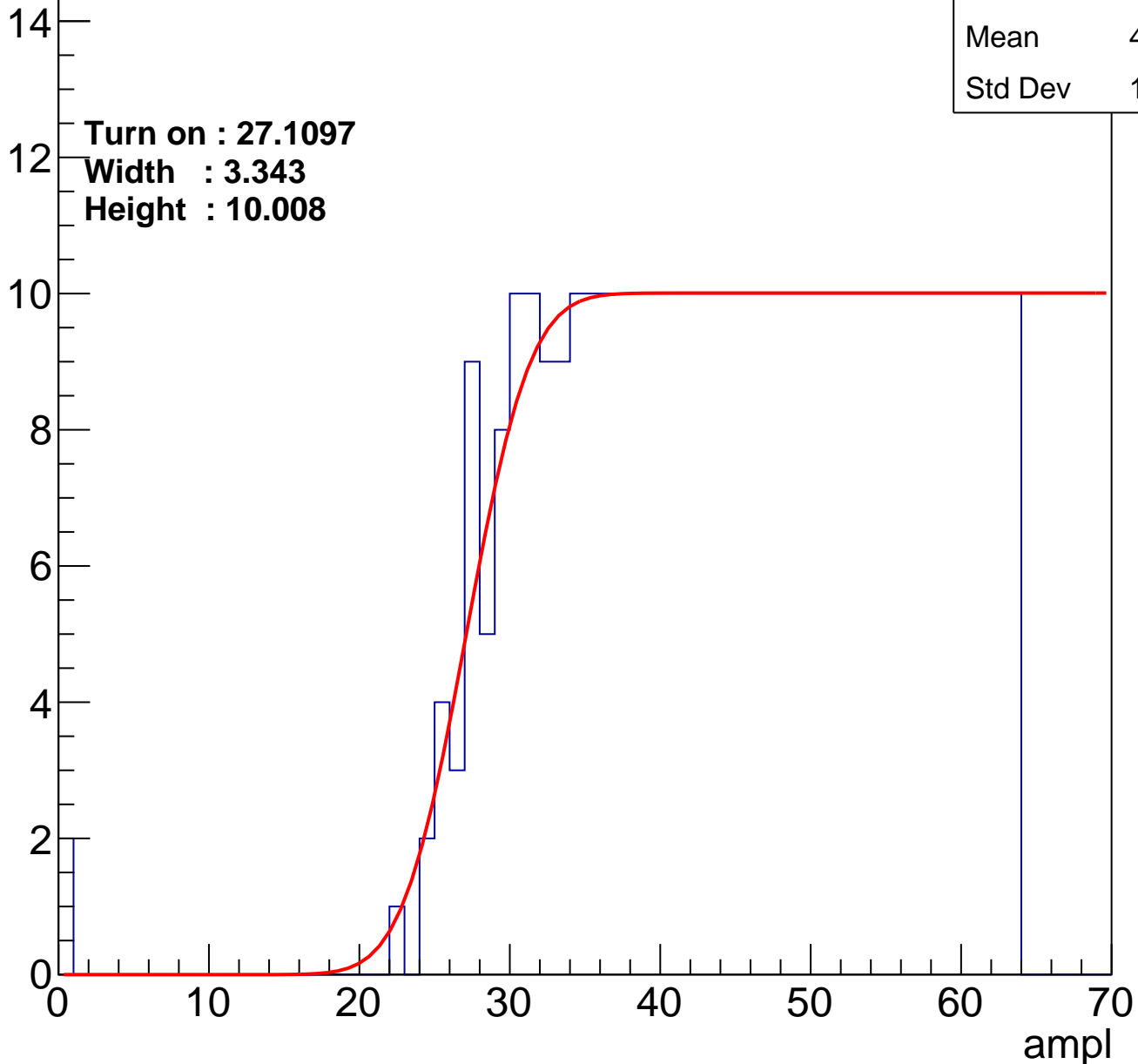
Entries	372
Mean	44.65
Std Dev	11.32

Turn on : 27.1097

Width : 3.343

Height : 10.008

Entry



B1L101S, U14-ch99

calib_packv5_042523_0143.root, FC#0, port D2

Entries	363
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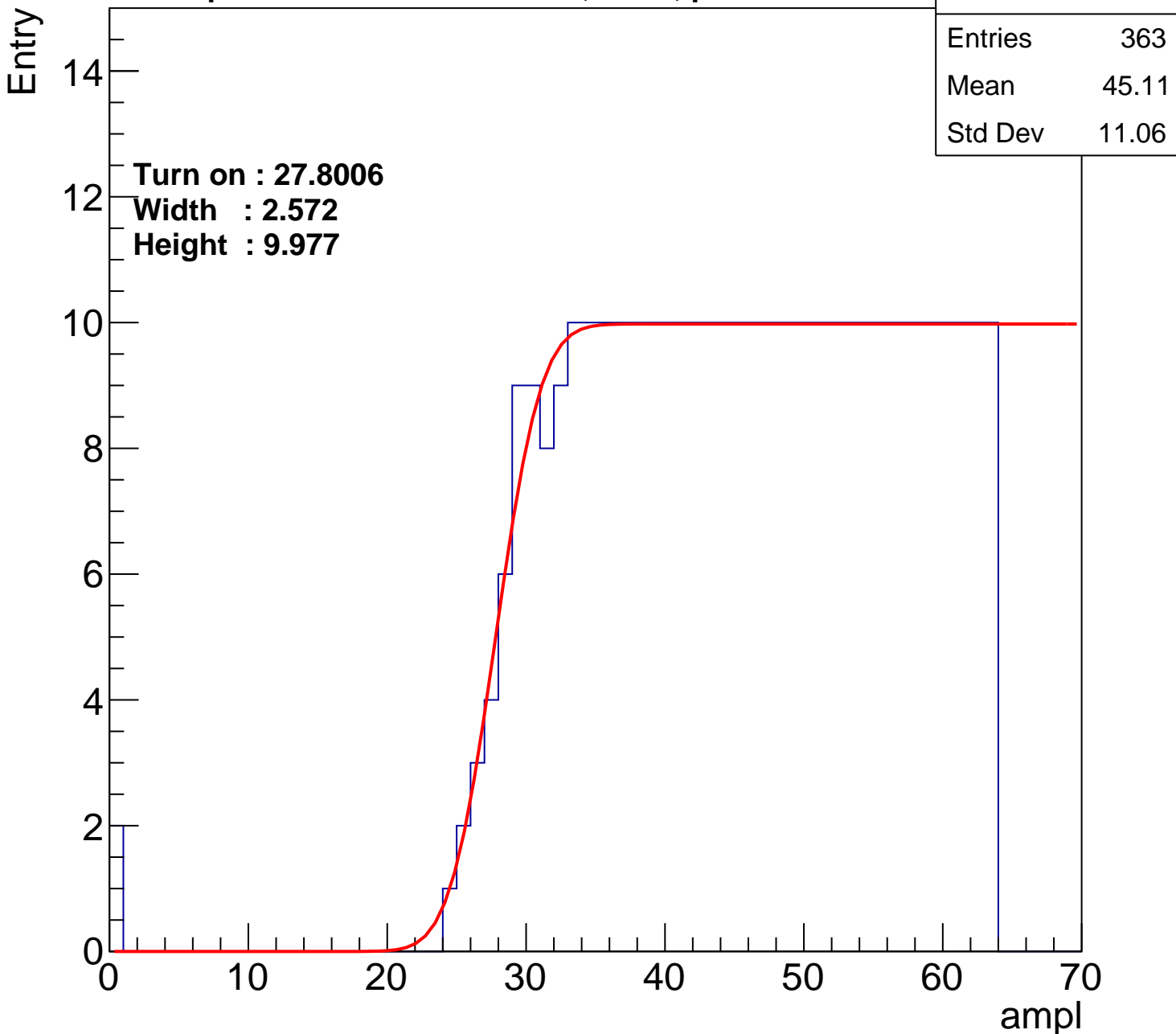
Mean	45.11
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Std Dev	11.06
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Turn on : 27.8006

Width : 2.572

Height : 9.977



B1L101S, U14-ch100

calib_packv5_042523_0143.root, FC#0, port D2

Entries	373
Mean	44.61
Std Dev	11.33

Turn on : 26.7538

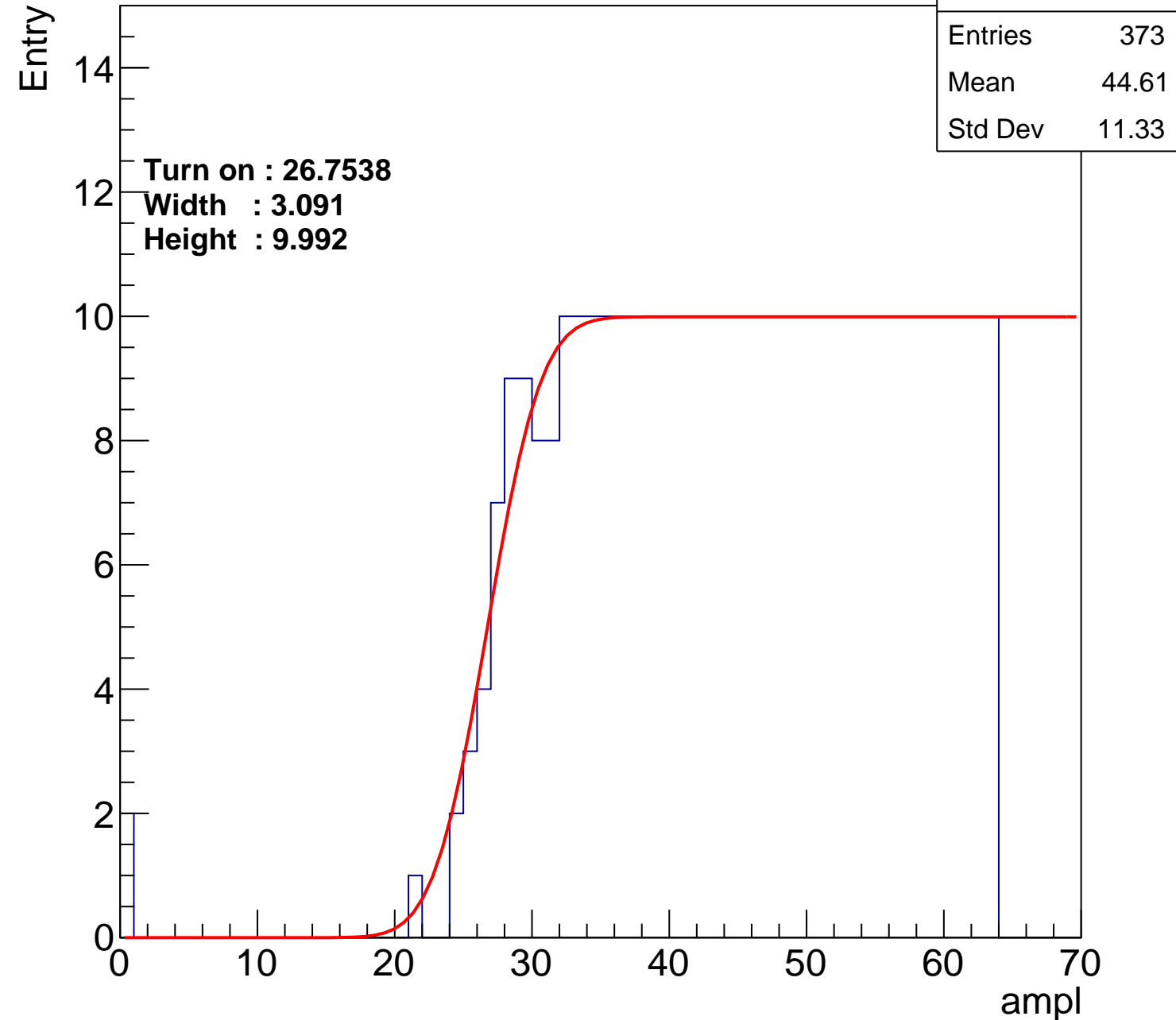
Width : 3.091

Height : 9.992

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch101

calib_packv5_042523_0143.root, FC#0, port D2

Entries	393
Mean	43.55
Std Dev	12.02

Turn on : 25.1553

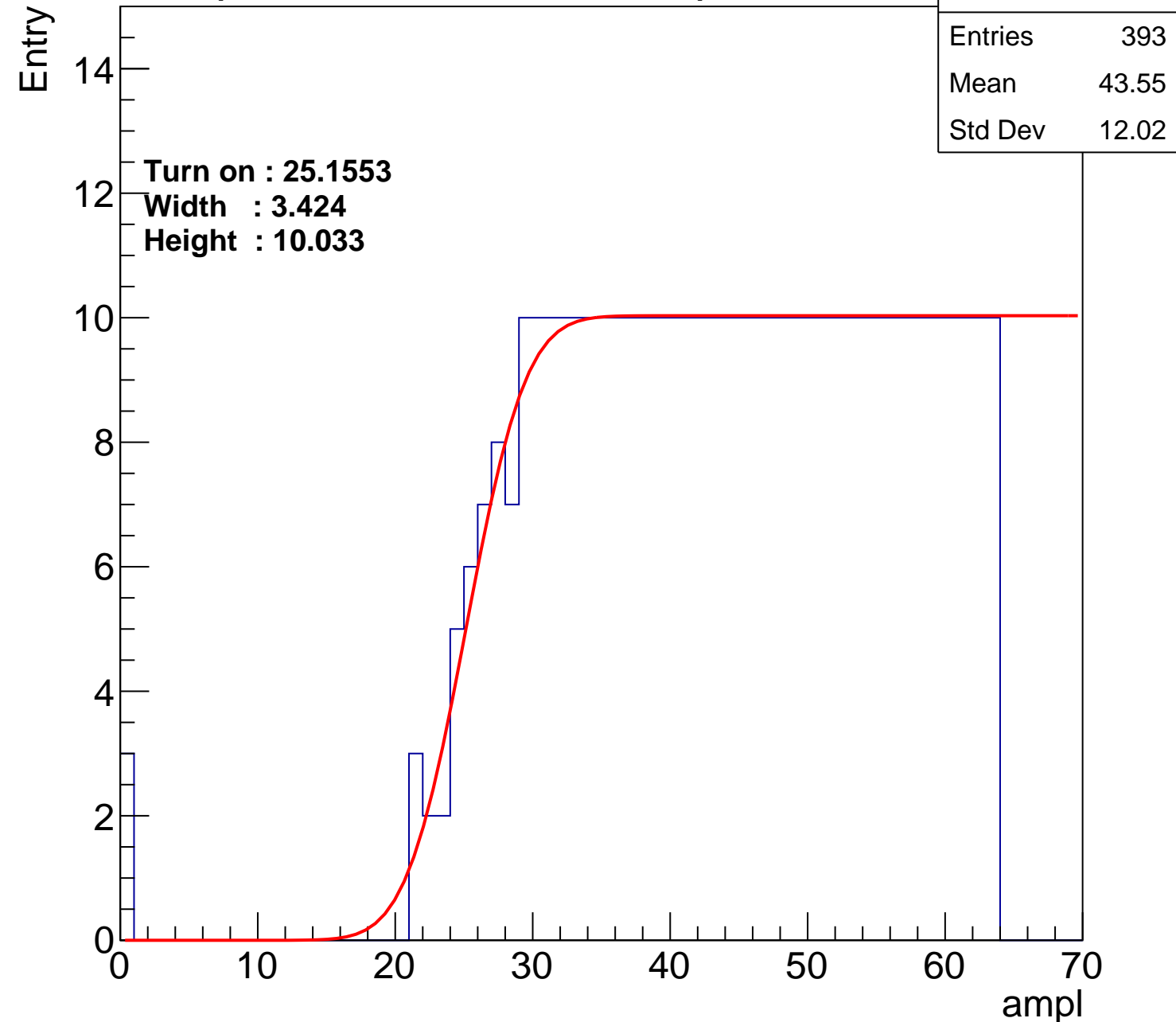
Width : 3.424

Height : 10.033

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch102

calib_packv5_042523_0143.root, FC#0, port D2

Entries	392
Mean	43.4
Std Dev	12.44

Turn on : 25.4228

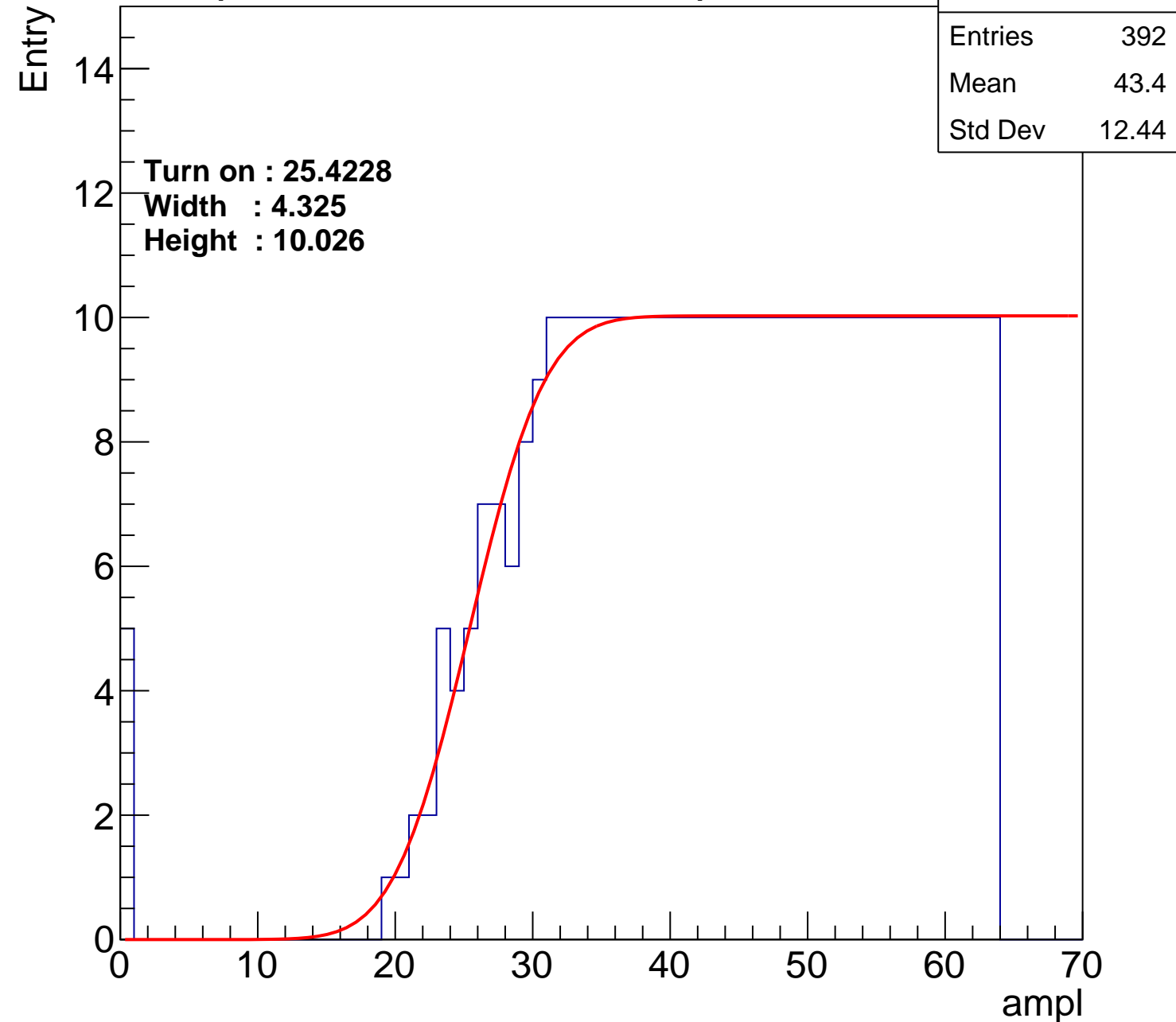
Width : 4.325

Height : 10.026

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch103

calib_packv5_042523_0143.root, FC#0, port D2

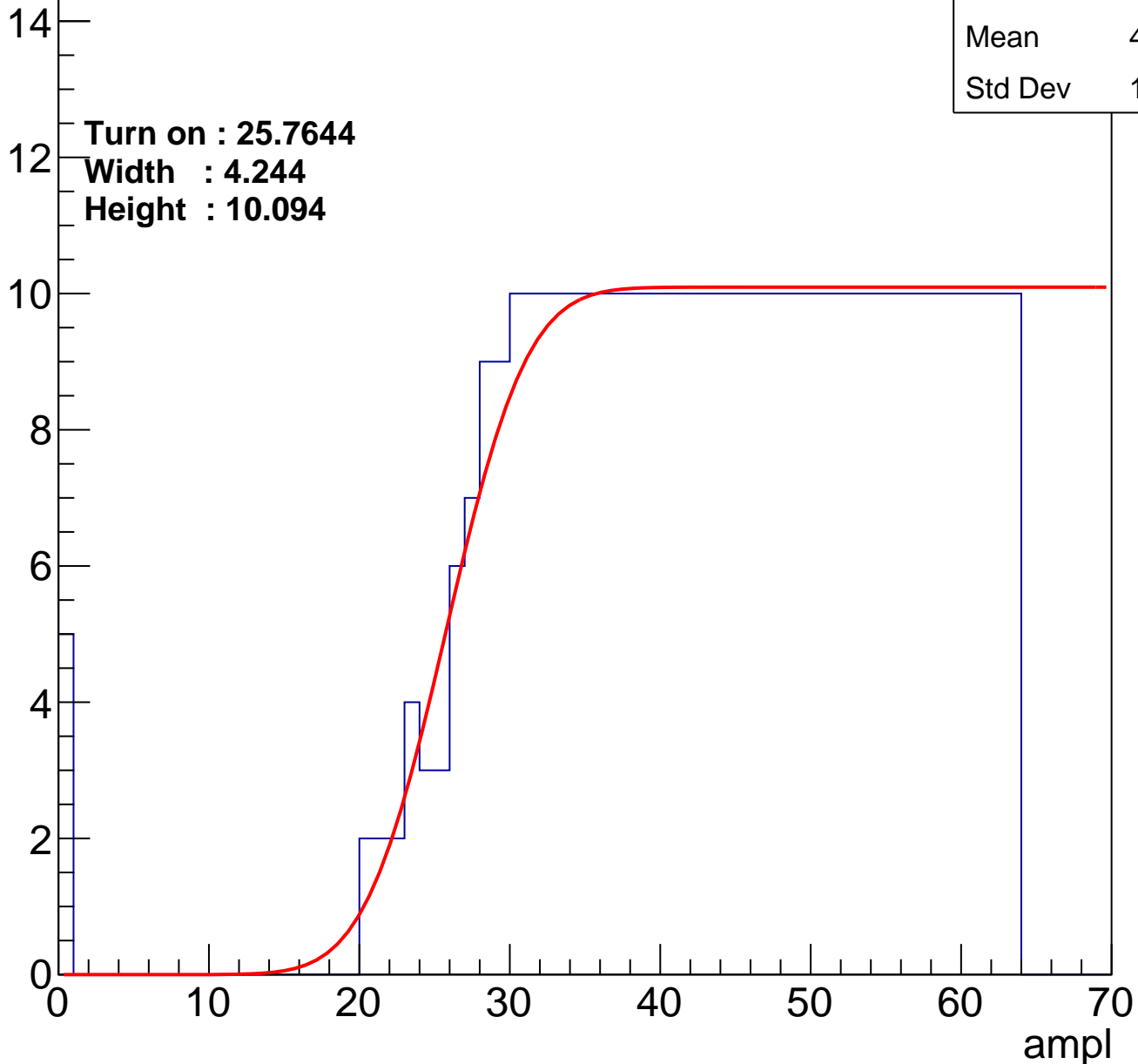
Entries	392
Mean	43.45
Std Dev	12.36

Turn on : 25.7644

Width : 4.244

Height : 10.094

Entry



B1L101S, U14-ch104

calib_packv5_042523_0143.root, FC#0, port D2

Entries	406
Mean	42.88
Std Dev	12.47

Turn on : 24.3902

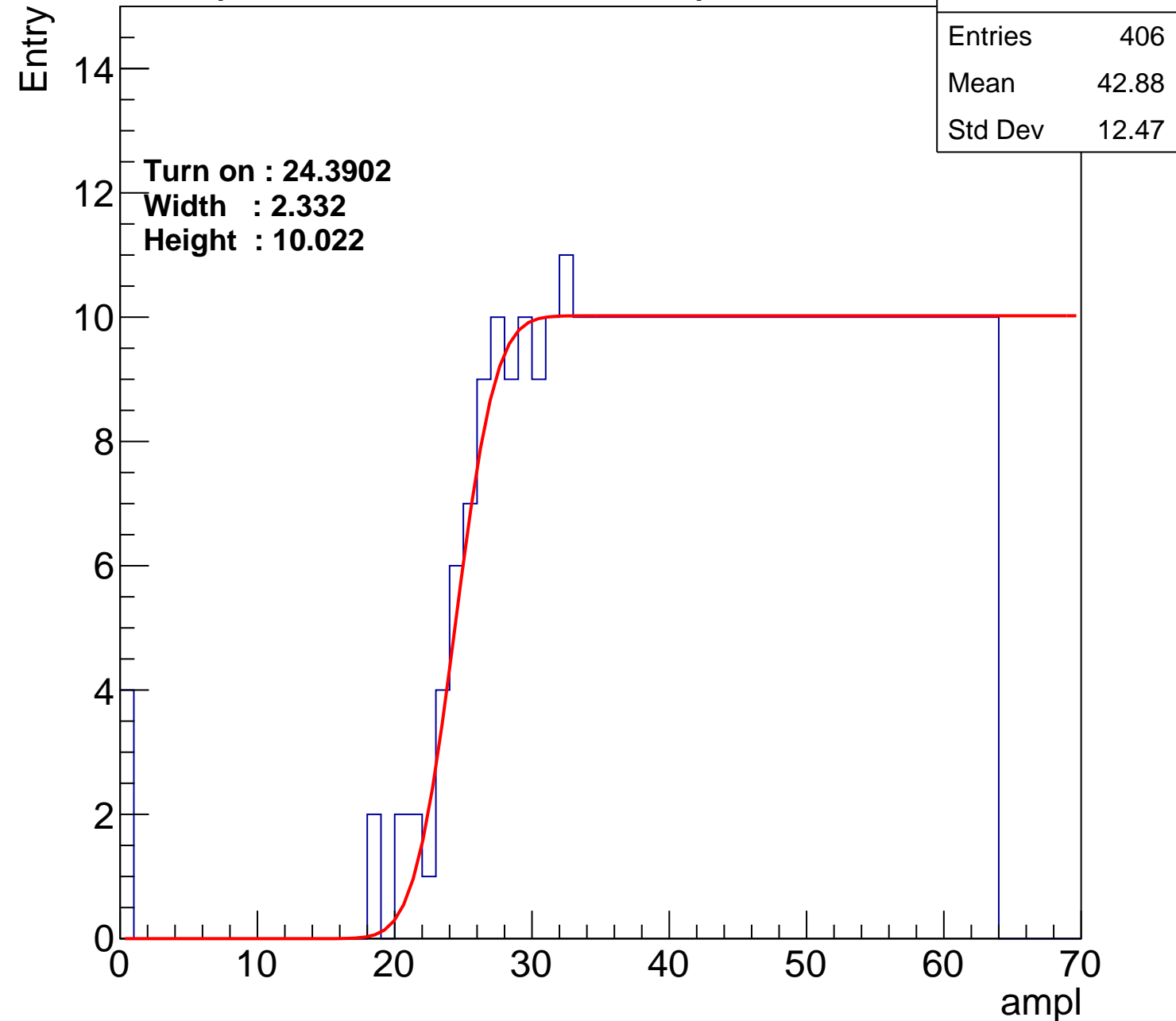
Width : 2.332

Height : 10.022

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch105

calib_packv5_042523_0143.root, FC#0, port D2

Entries	377
Mean	44.45
Std Dev	11.38

Turn on : 26.8153

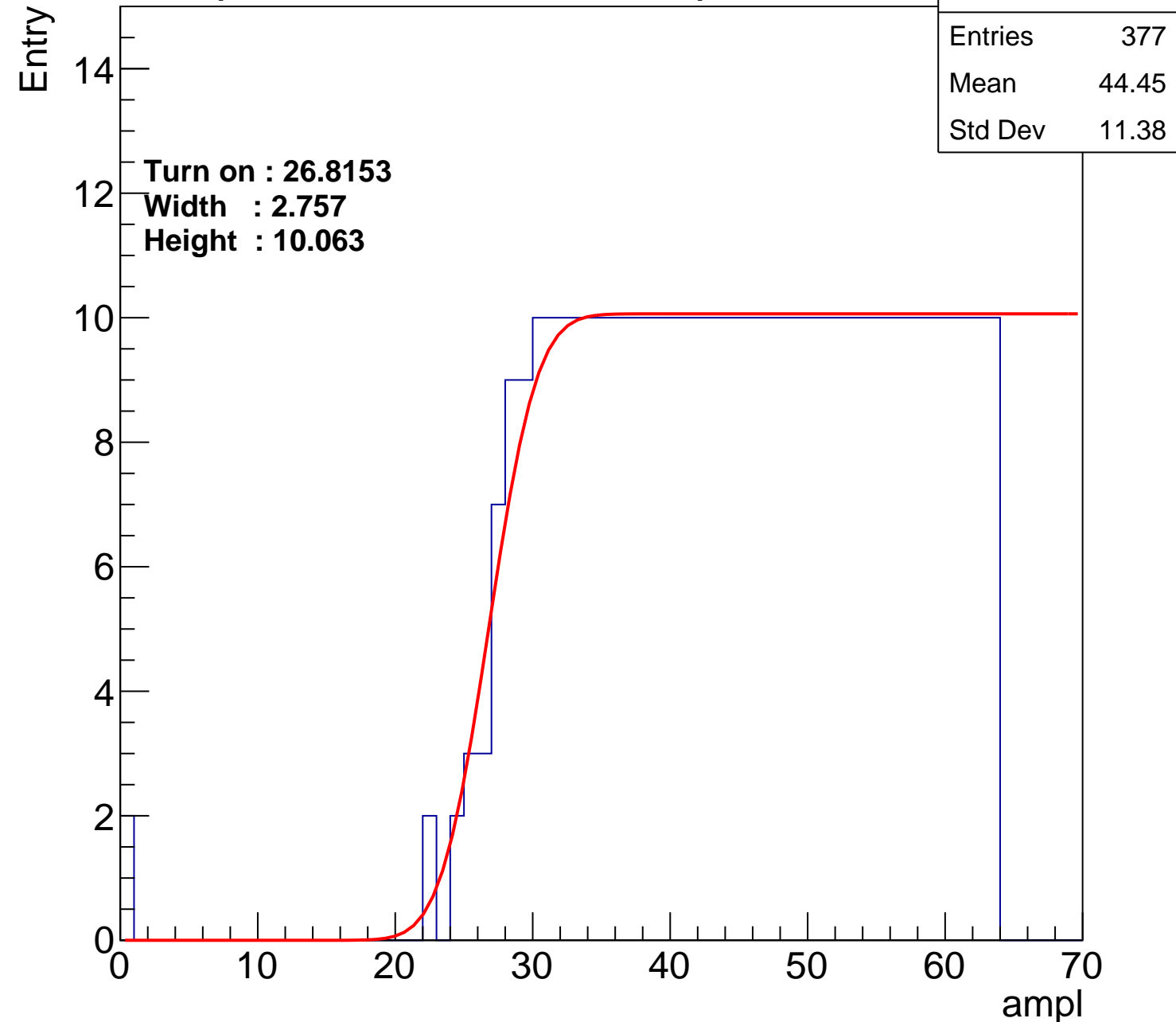
Width : 2.757

Height : 10.063

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch106

calib_packv5_042523_0143.root, FC#0, port D2

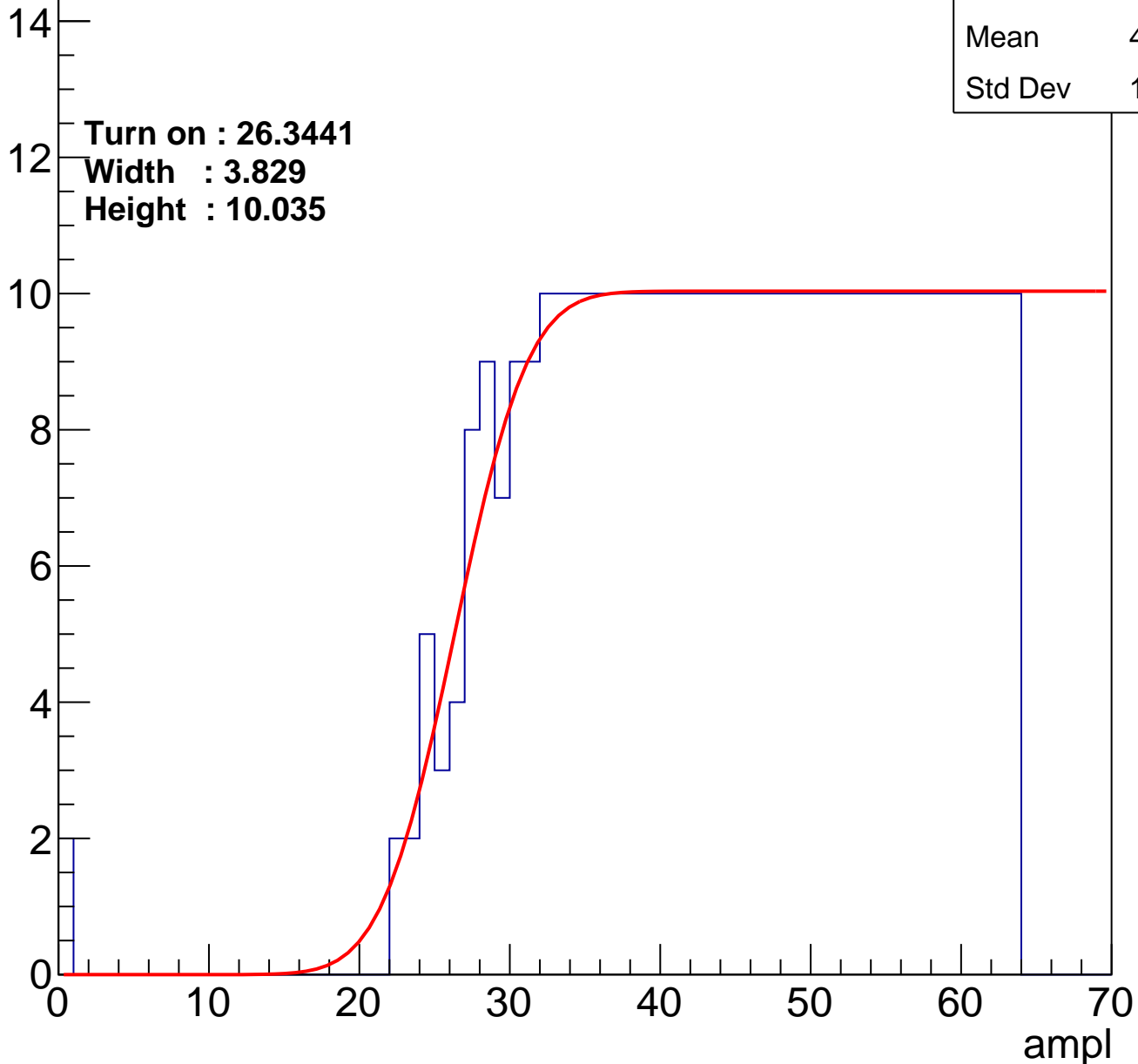
Entries	380
Mean	44.23
Std Dev	11.56

Turn on : 26.3441

Width : 3.829

Height : 10.035

Entry



B1L101S, U14-ch107

calib_packv5_042523_0143.root, FC#0, port D2

Entries	367
Mean	44.77
Std Dev	11.56

Turn on : 27.8383

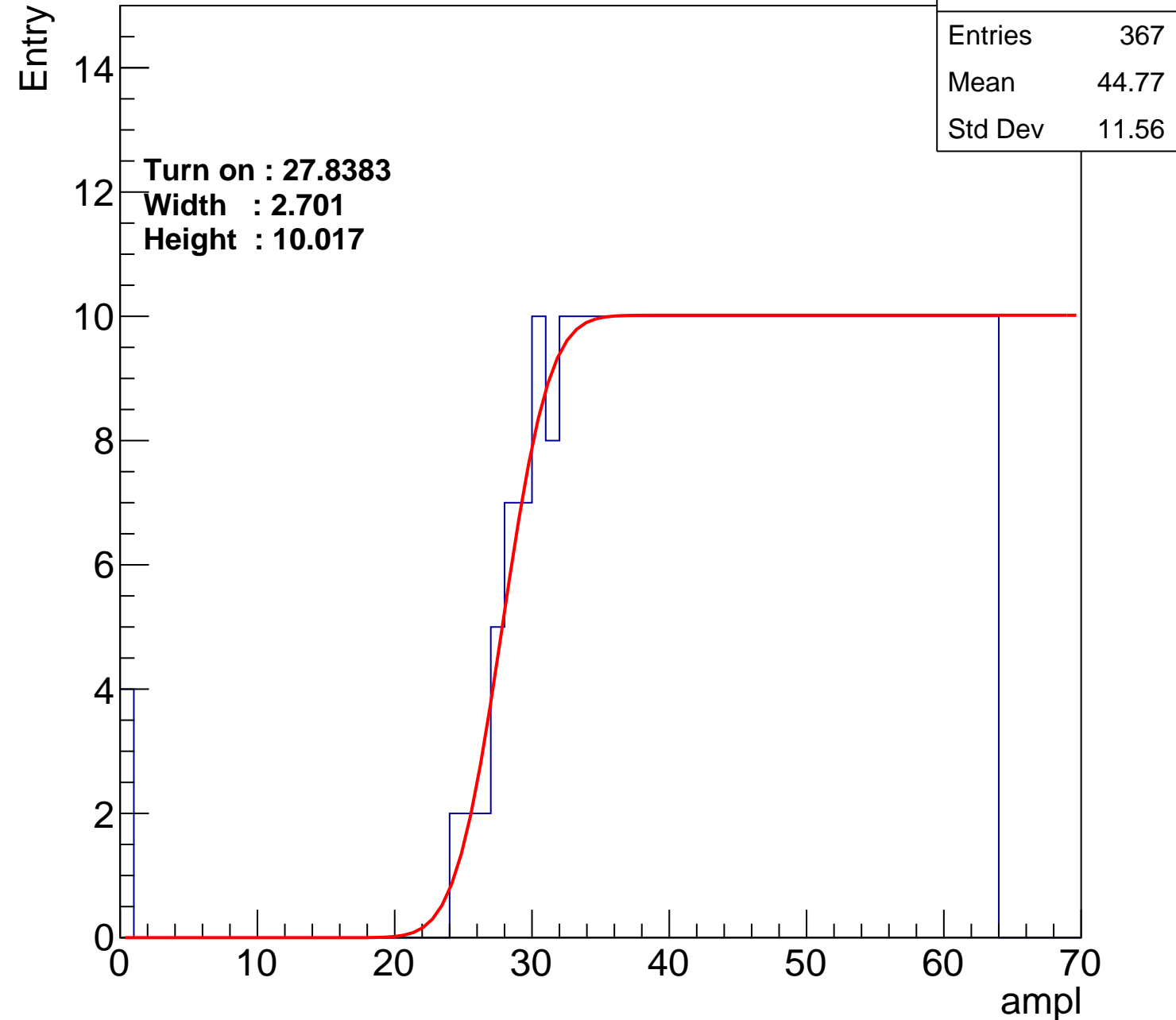
Width : 2.701

Height : 10.017

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch108

calib_packv5_042523_0143.root, FC#0, port D2

Entries	394
Mean	43.57
Std Dev	11.88

Turn on : 25.3267

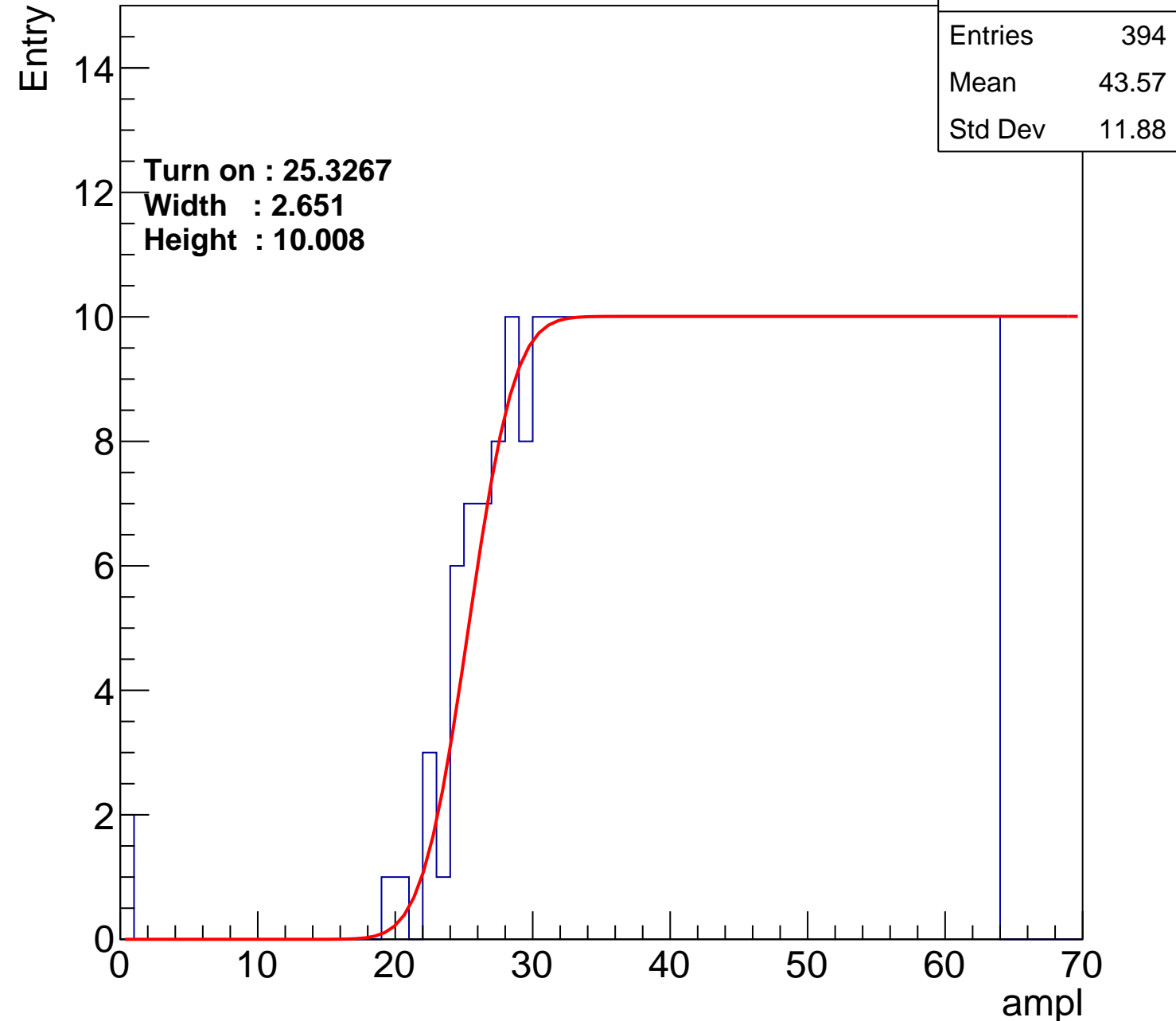
Width : 2.651

Height : 10.008

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch109

calib_packv5_042523_0143.root, FC#0, port D2

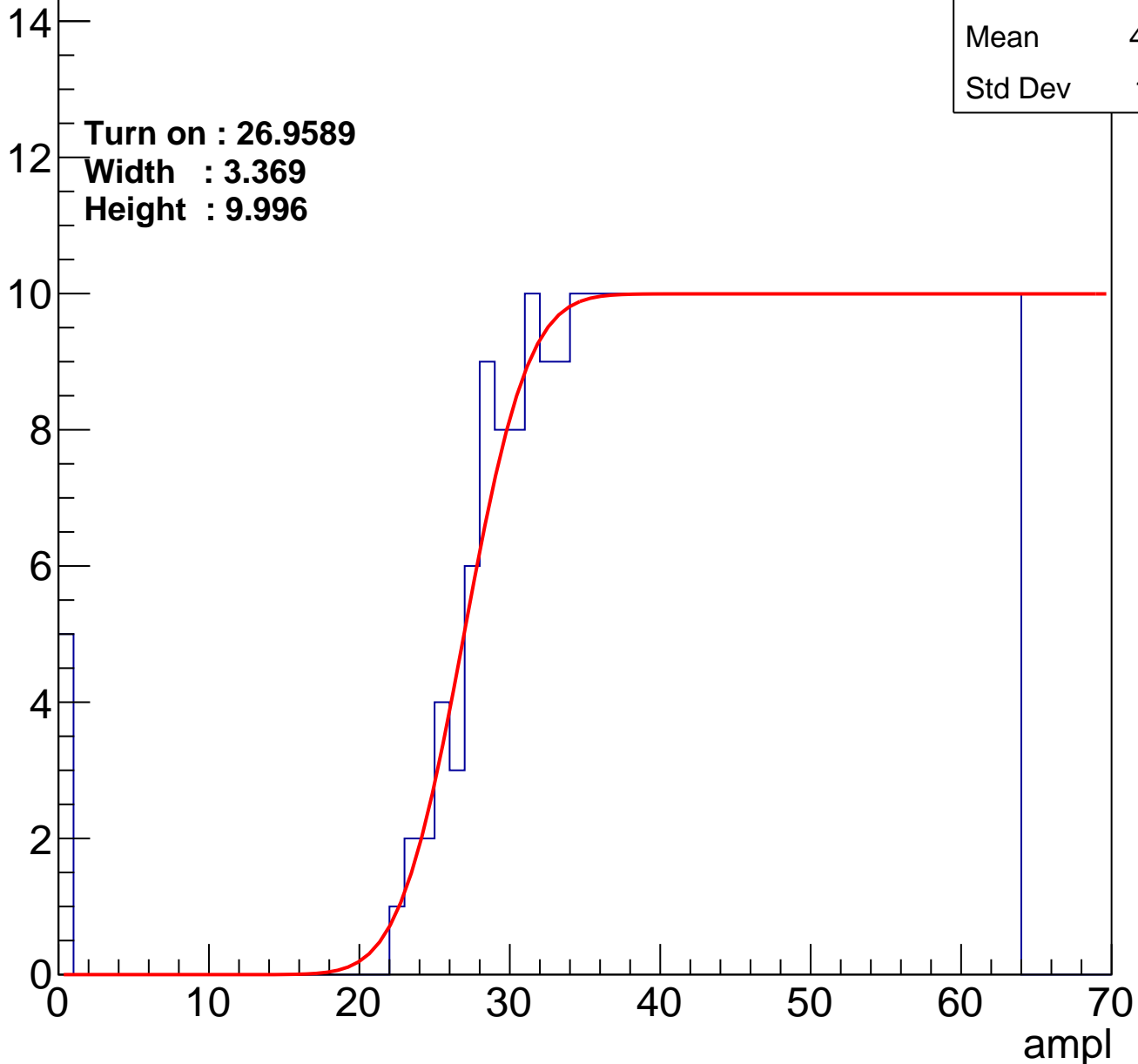
Entries	376
Mean	44.22
Std Dev	12.01

Turn on : 26.9589

Width : 3.369

Height : 9.996

Entry



B1L101S, U14-ch110

calib_packv5_042523_0143.root, FC#0, port D2

Entries	388
Mean	43.44
Std Dev	12.76

Turn on : 25.9594

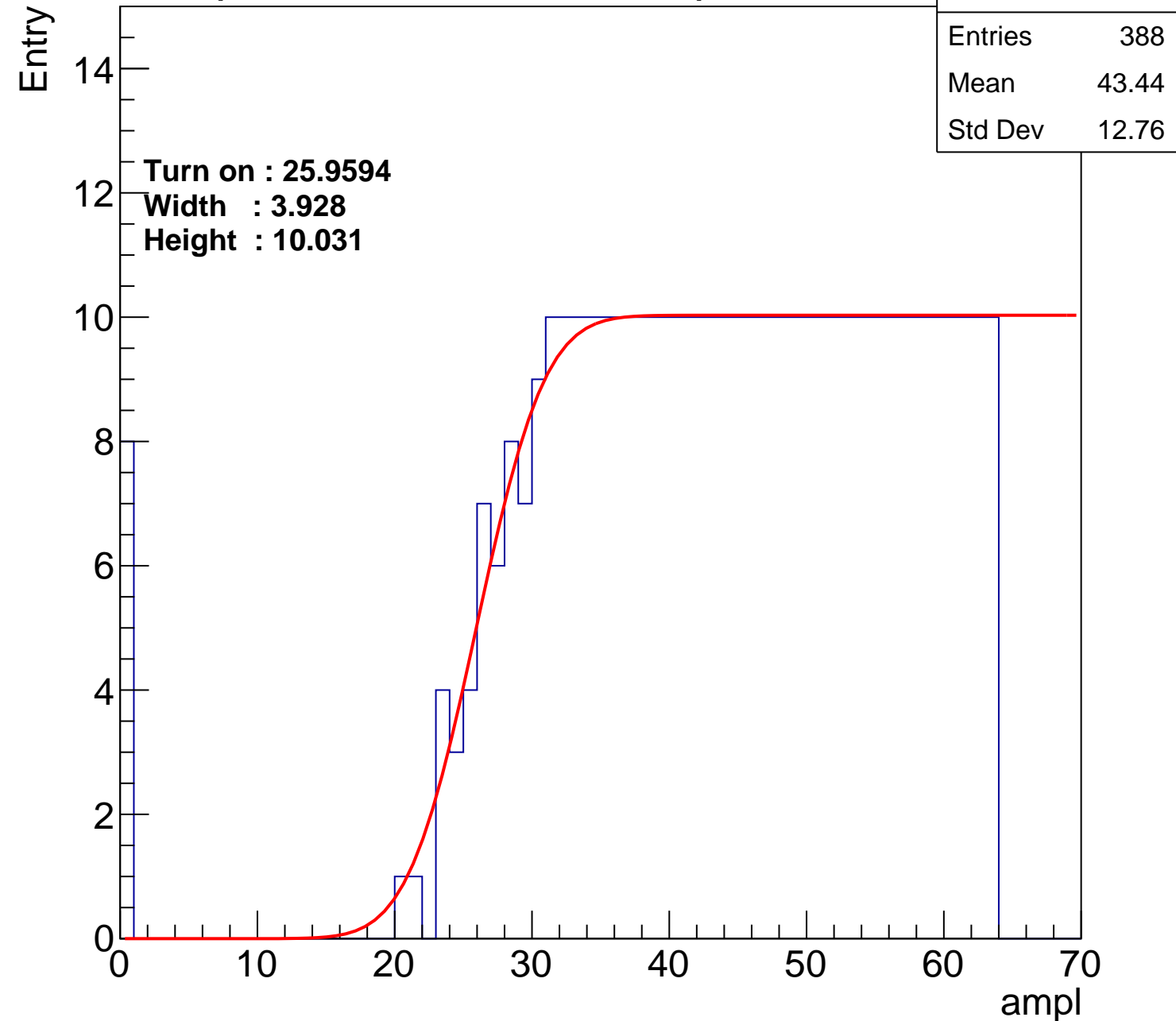
Width : 3.928

Height : 10.031

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch111

calib_packv5_042523_0143.root, FC#0, port D2

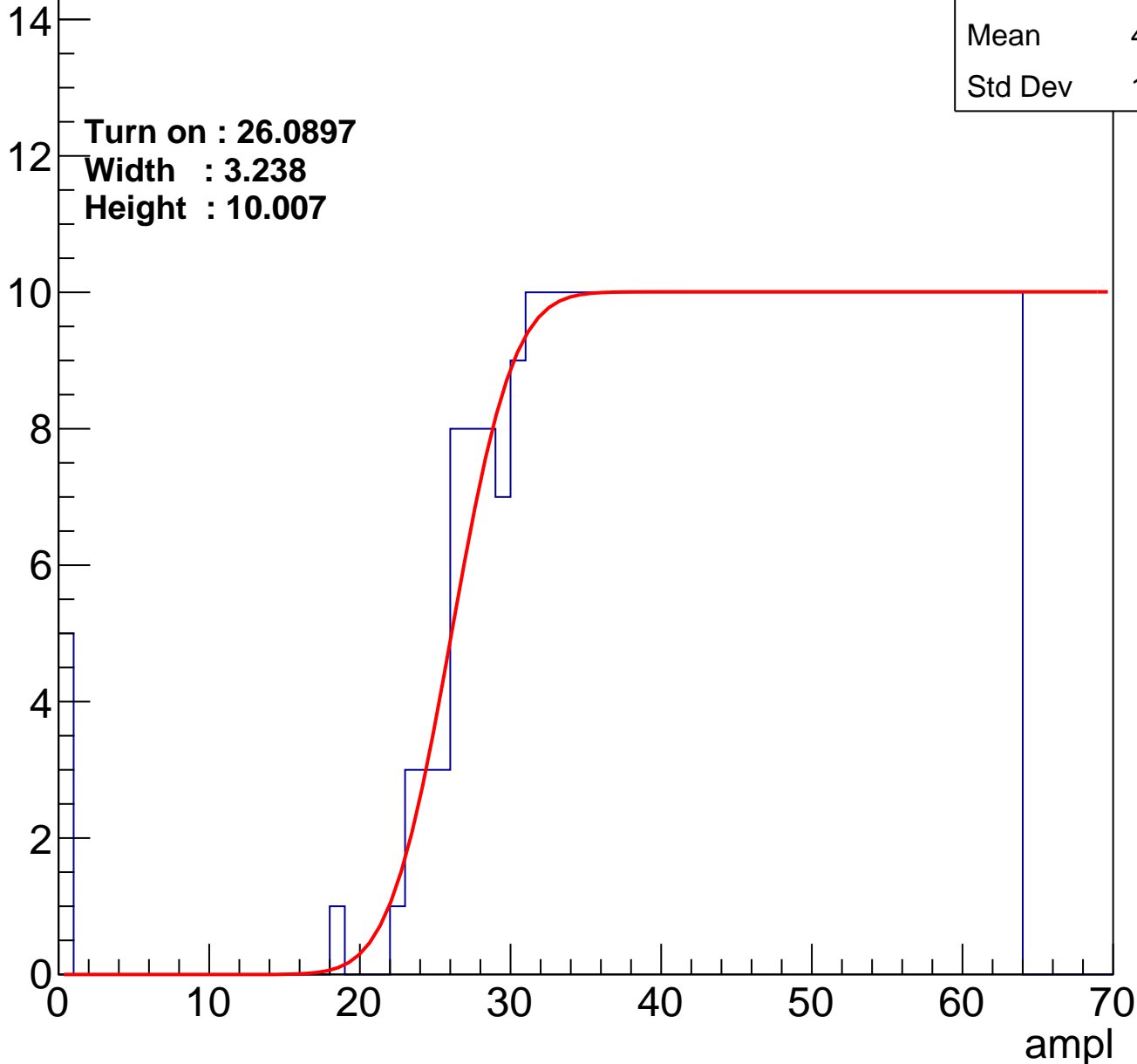
Entries	386
Mean	43.75
Std Dev	12.22

Turn on : 26.0897

Width : 3.238

Height : 10.007

Entry



B1L101S, U14-ch112

calib_packv5_042523_0143.root, FC#0, port D2

Entries	364
Mean	44.97
Std Dev	11.32

Turn on : 27.9574

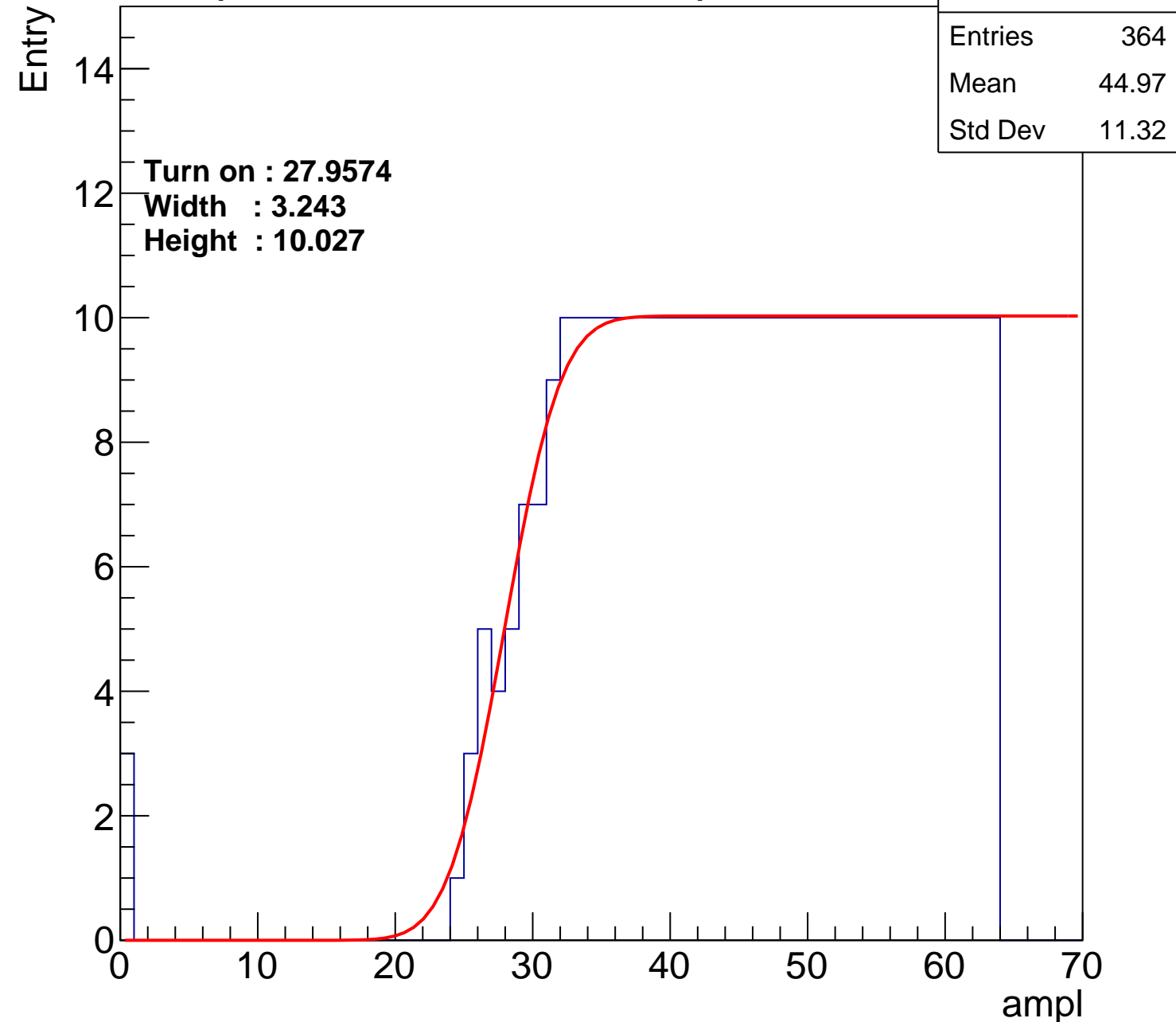
Width : 3.243

Height : 10.027

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch113

calib_packv5_042523_0143.root, FC#0, port D2

Entries	364
Mean	44.98
Std Dev	11.31

Turn on : 27.6740

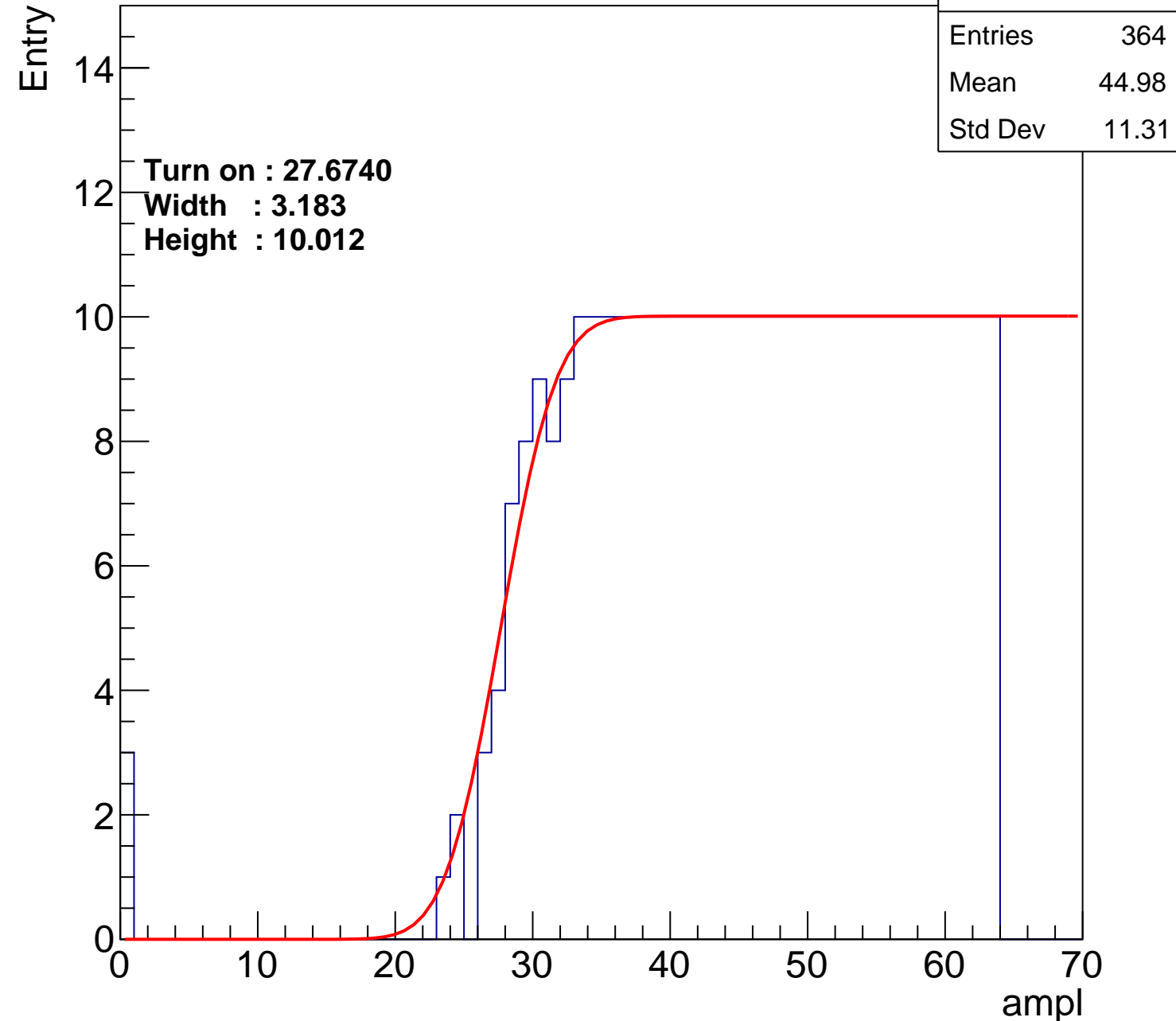
Width : 3.183

Height : 10.012

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch114

calib_packv5_042523_0143.root, FC#0, port D2

Entries	380
Mean	44.12
Std Dev	11.81

Turn on : 26.8753

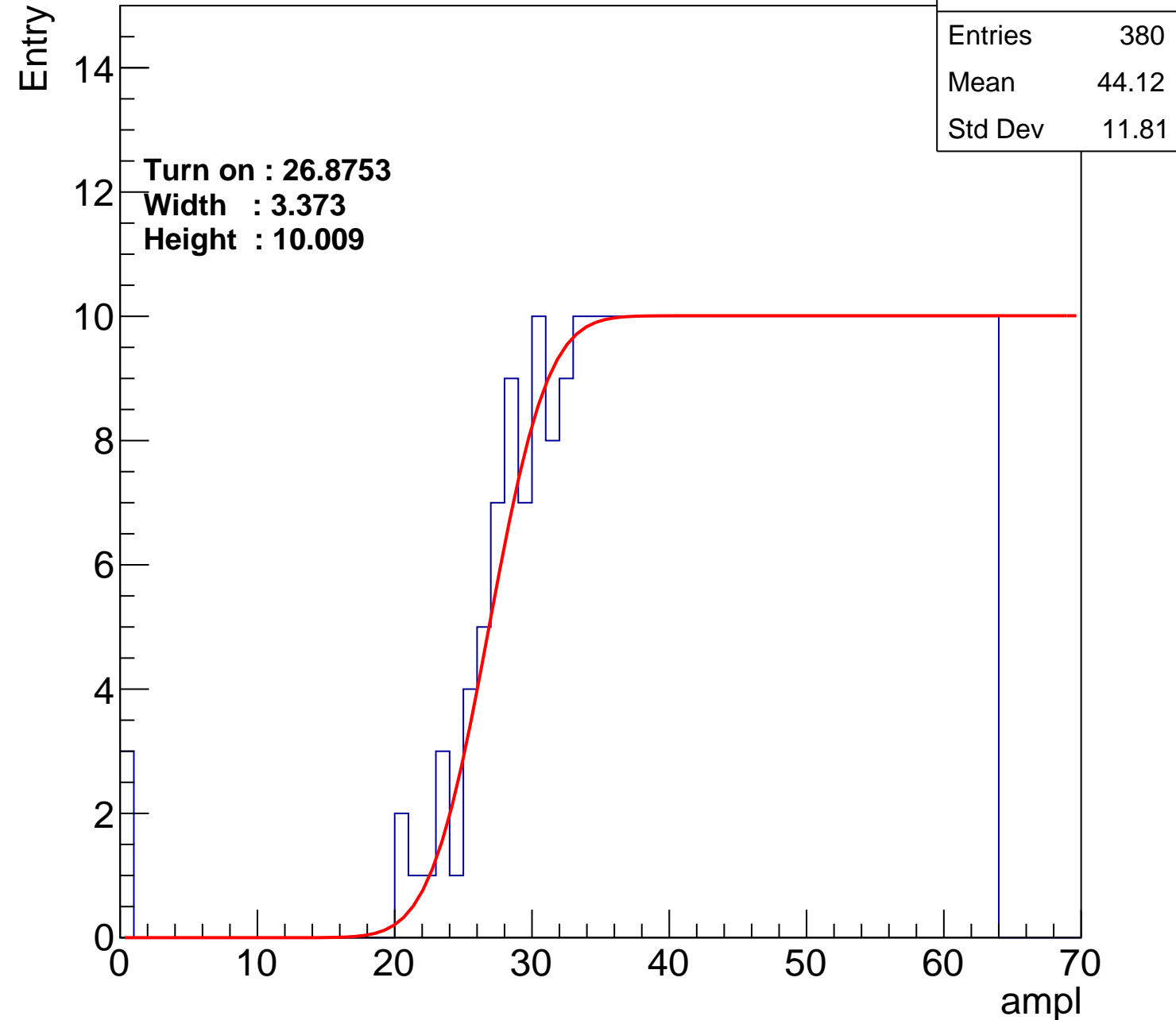
Width : 3.373

Height : 10.009

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch115

calib_packv5_042523_0143.root, FC#0, port D2

Entries	363
Mean	45.09
Std Dev	11.09

Turn on : 28.1334

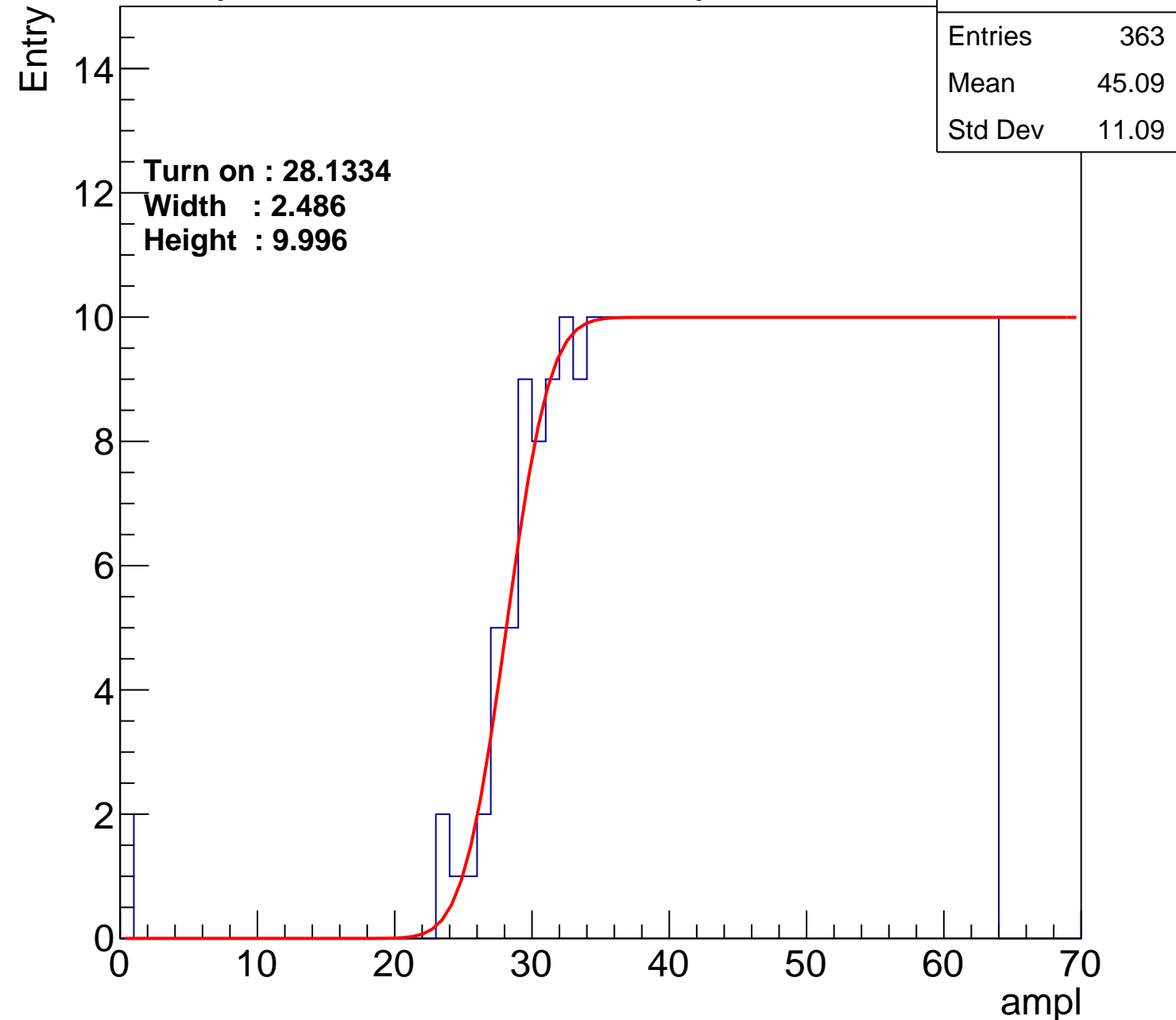
Width : 2.486

Height : 9.996

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch116

calib_packv5_042523_0143.root, FC#0, port D2

Entries	376
Mean	44.32
Std Dev	11.8

Turn on : 27.3304

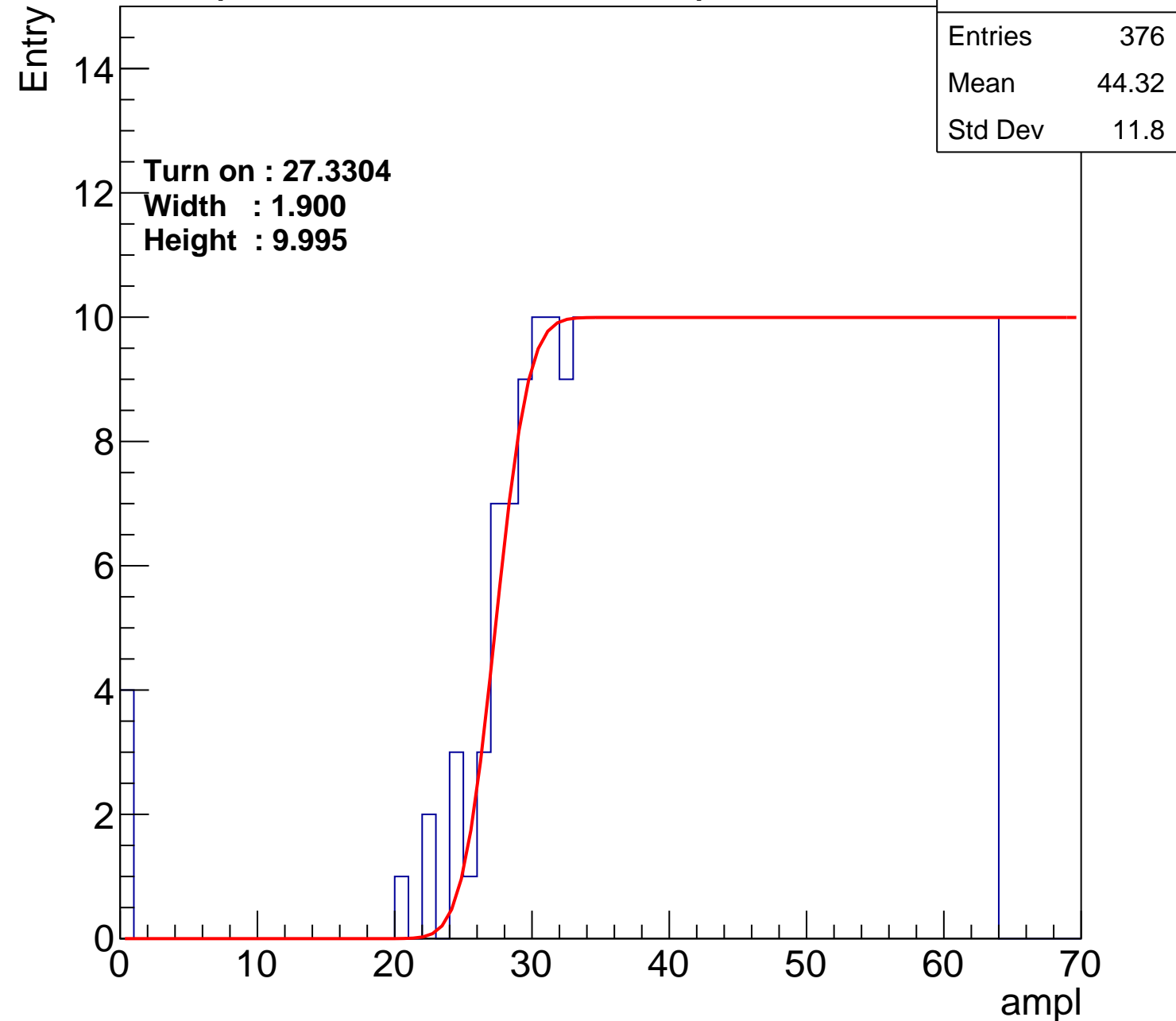
Width : 1.900

Height : 9.995

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch117

calib_packv5_042523_0143.root, FC#0, port D2

Entries	375
Mean	44.43
Std Dev	11.51

Turn on : 27.4829

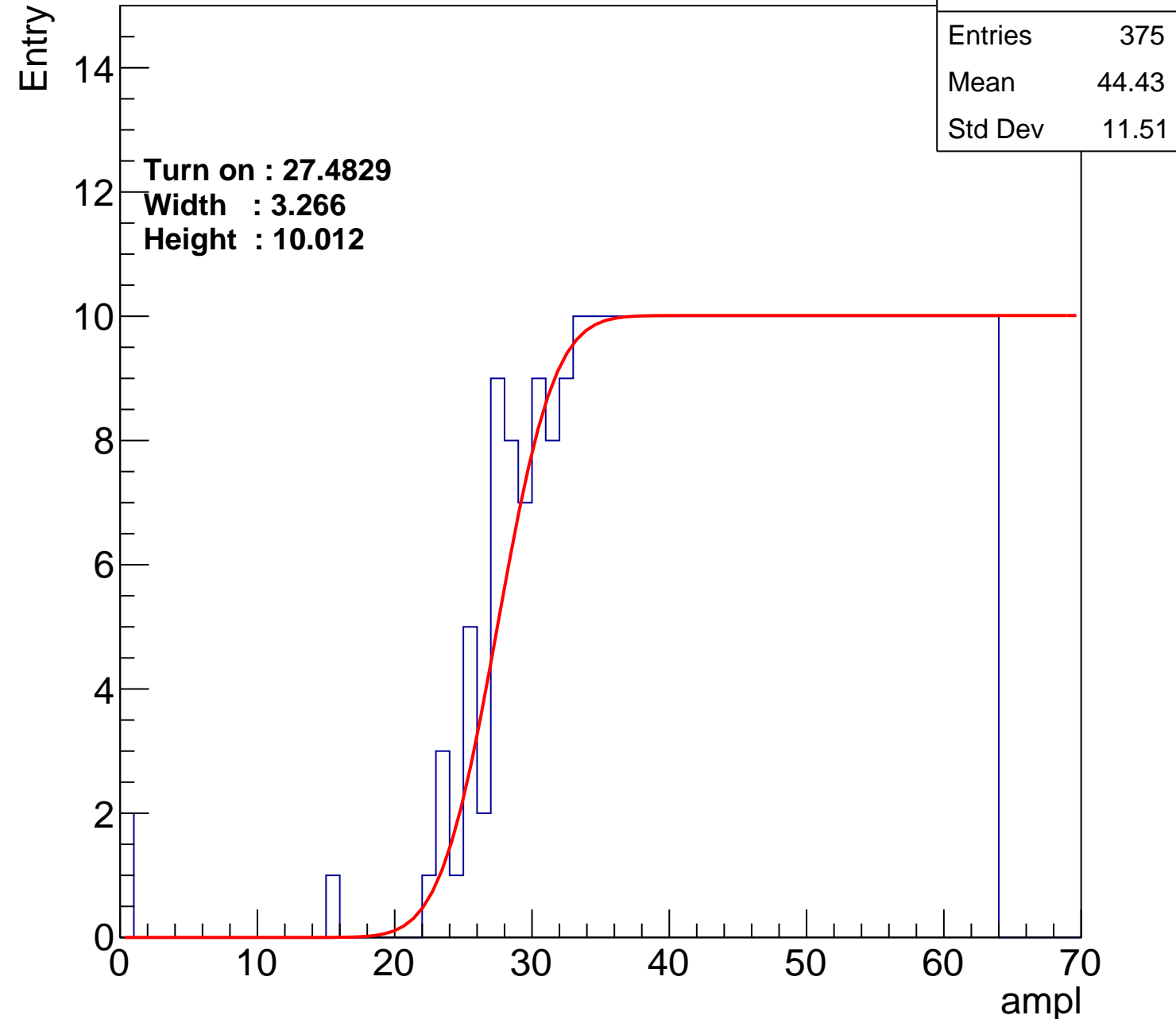
Width : 3.266

Height : 10.012

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch118

calib_packv5_042523_0143.root, FC#0, port D2

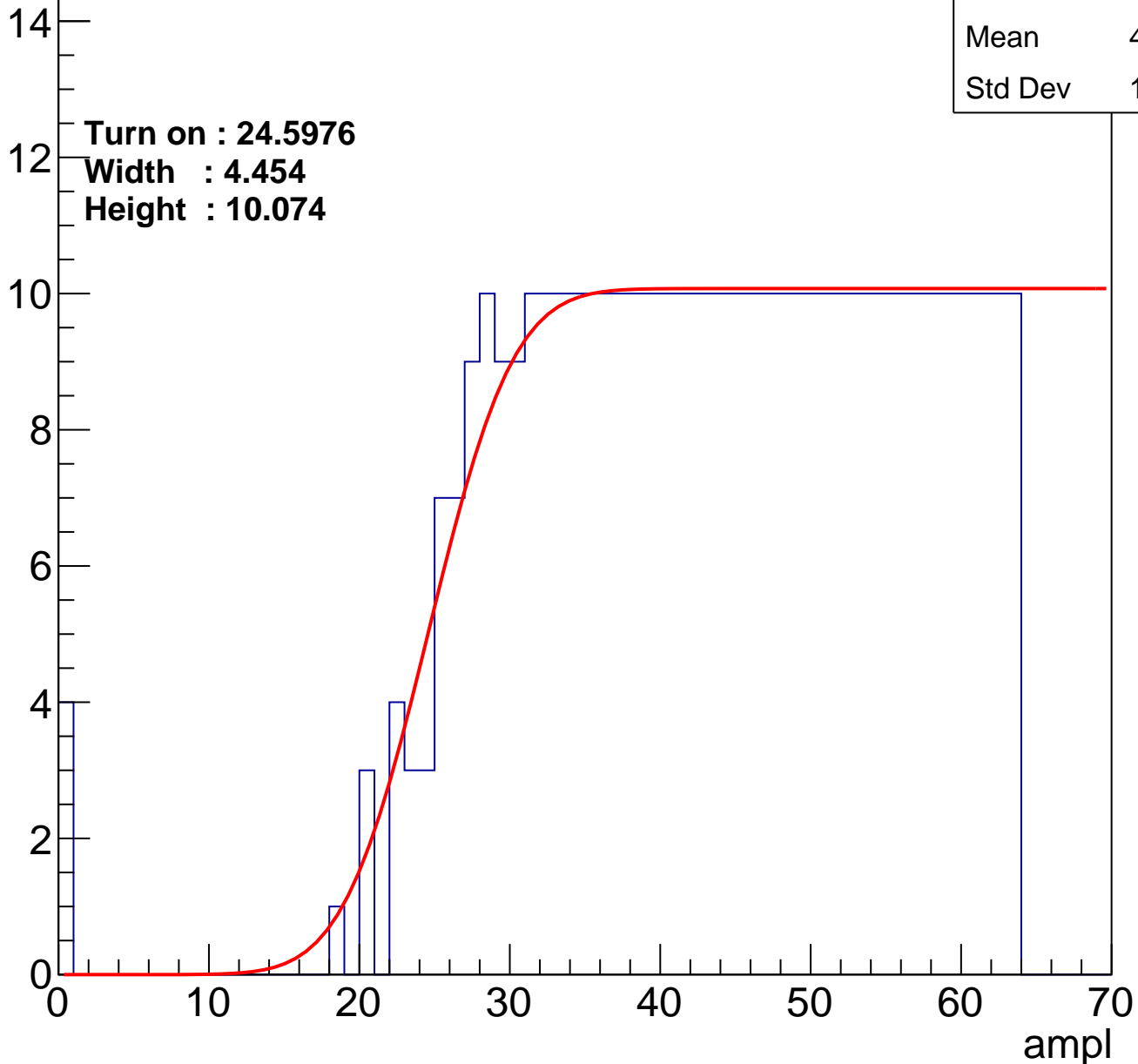
Entries	399
Mean	43.18
Std Dev	12.36

Turn on : 24.5976

Width : 4.454

Height : 10.074

Entry



B1L101S, U14-ch119

calib_packv5_042523_0143.root, FC#0, port D2

Entries	391
Mean	43.54
Std Dev	12.2

Turn on : 25.3873

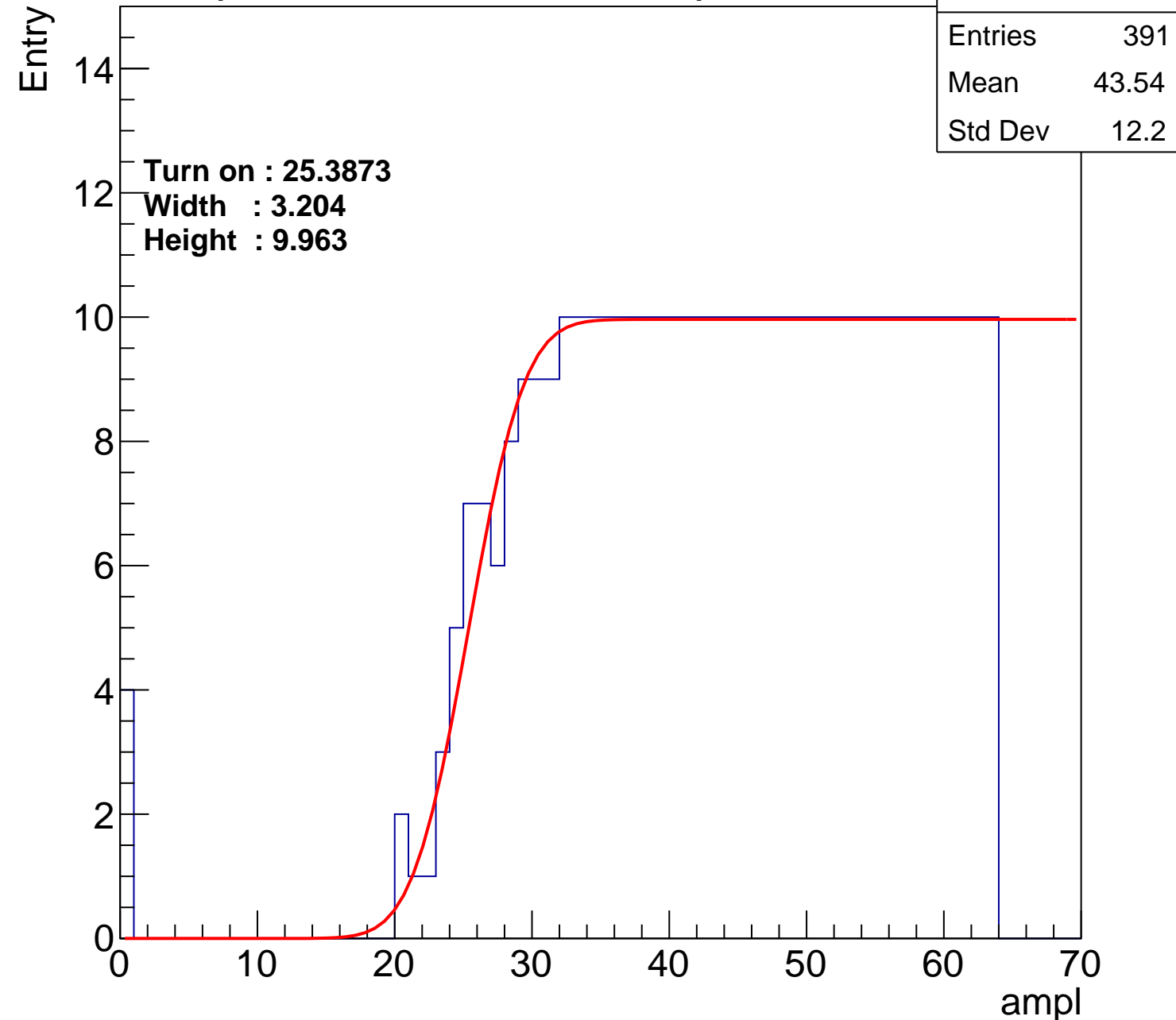
Width : 3.204

Height : 9.963

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch120

calib_packv5_042523_0143.root, FC#0, port D2

Entries	377
Mean	44.34
Std Dev	11.62

Turn on : 26.5275

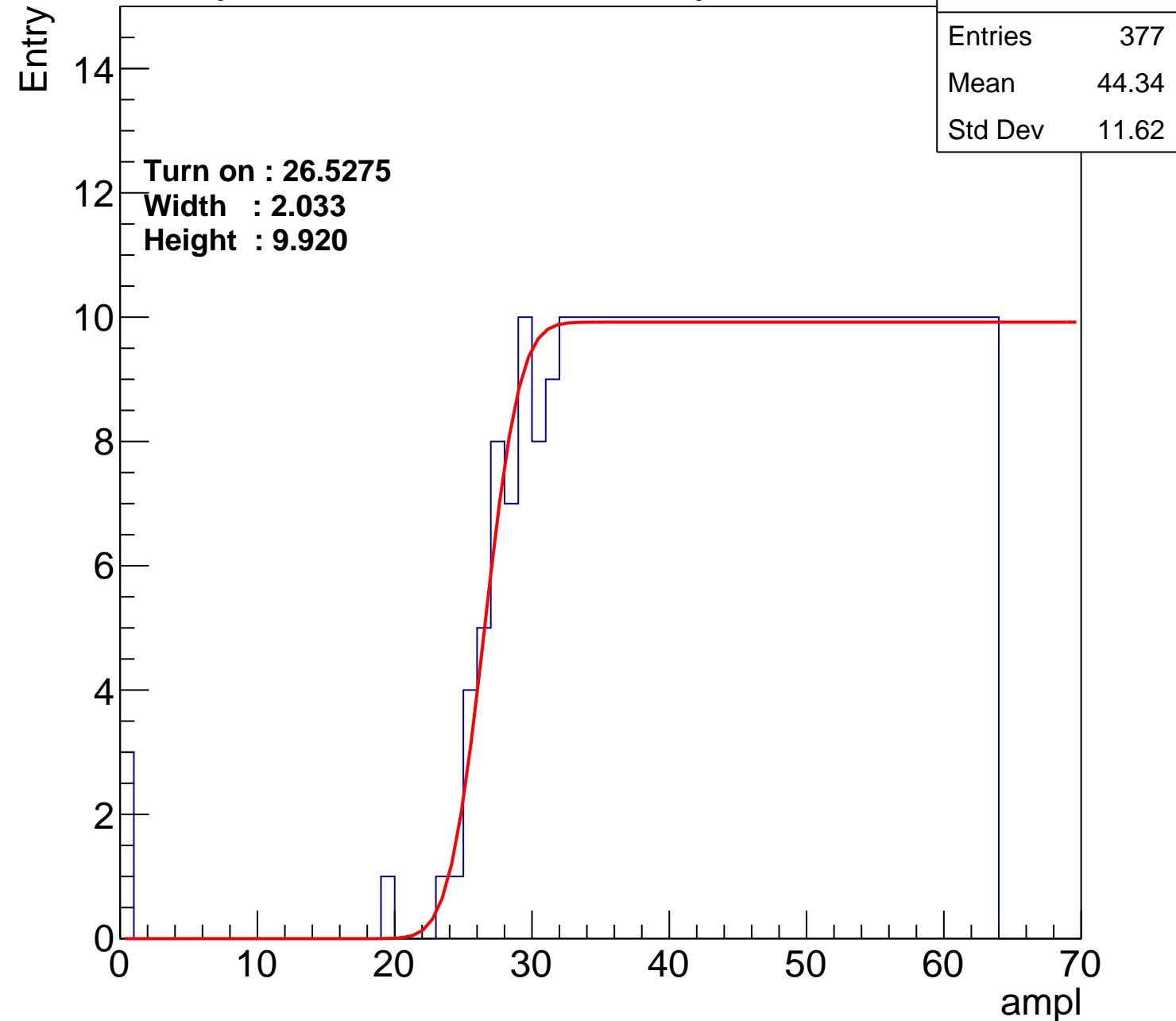
Width : 2.033

Height : 9.920

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch121

calib_packv5_042523_0143.root, FC#0, port D2

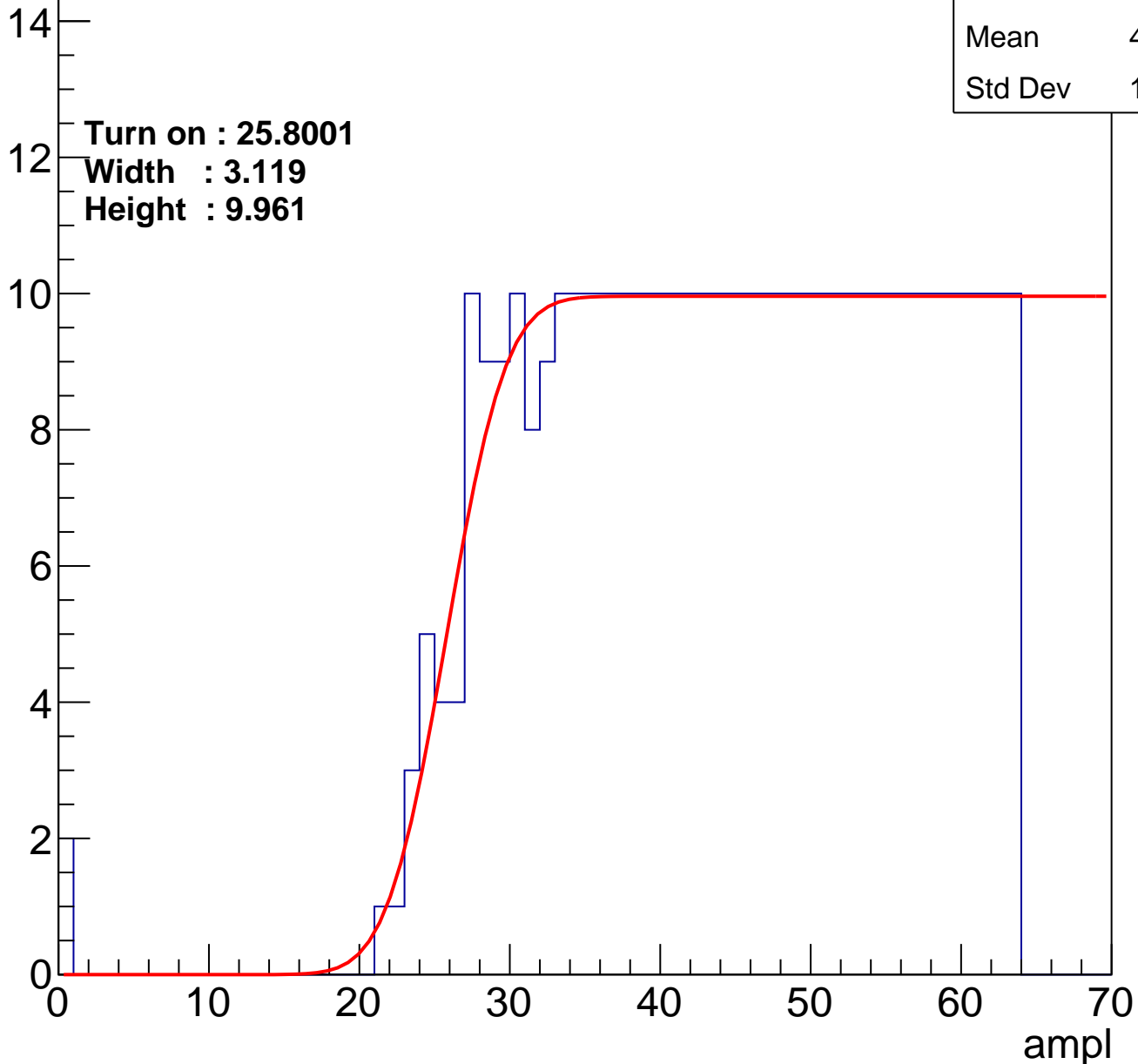
Entries	385
Mean	43.99
Std Dev	11.68

Turn on : 25.8001

Width : 3.119

Height : 9.961

Entry



B1L101S, U14-ch122

calib_packv5_042523_0143.root, FC#0, port D2

Entries	371
Mean	44.42
Std Dev	11.96

Turn on : 27.1370

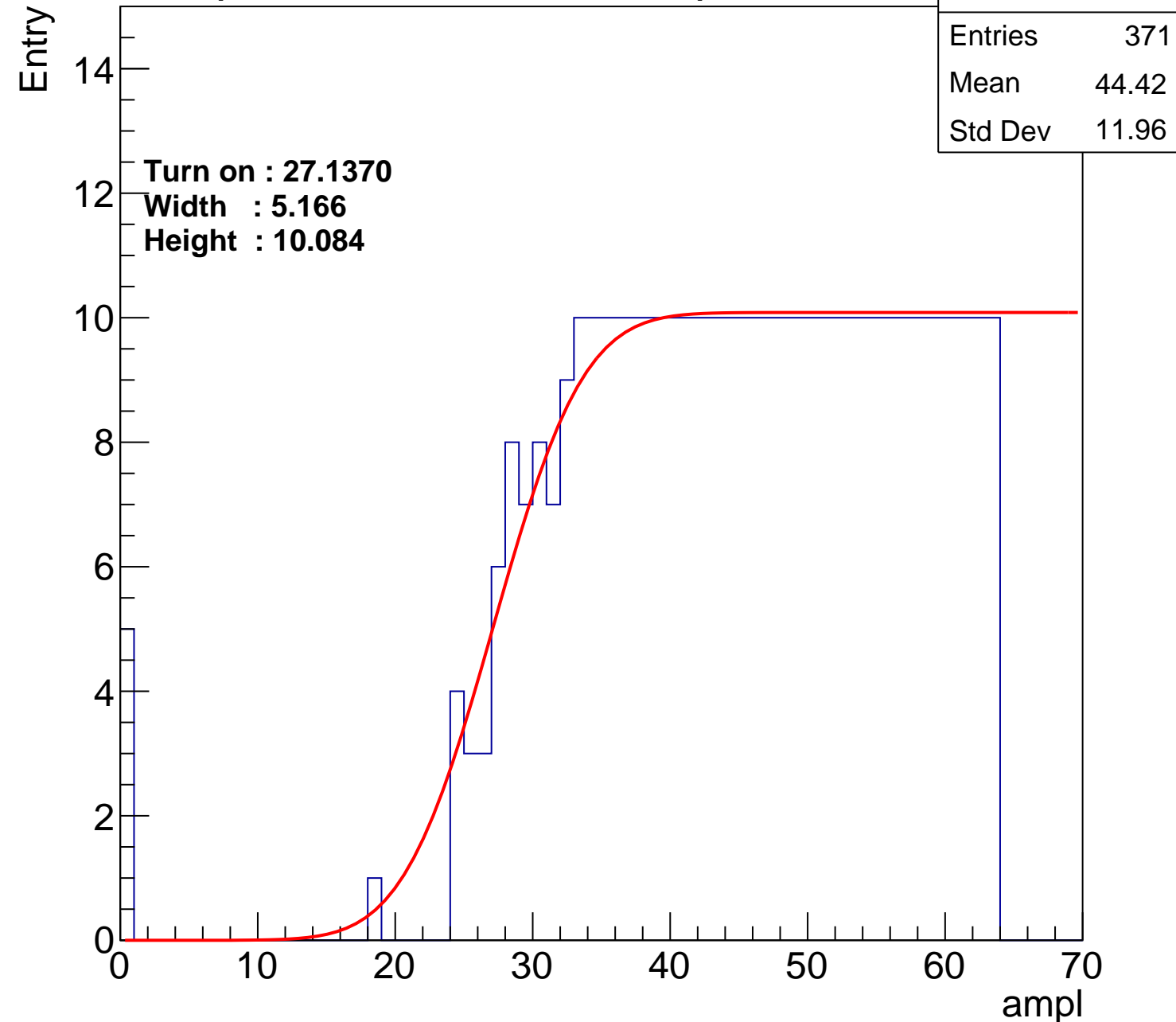
Width : 5.166

Height : 10.084

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch123

calib_packv5_042523_0143.root, FC#0, port D2

Entries	377
Mean	44.46
Std Dev	11.37

Turn on : 26.8438

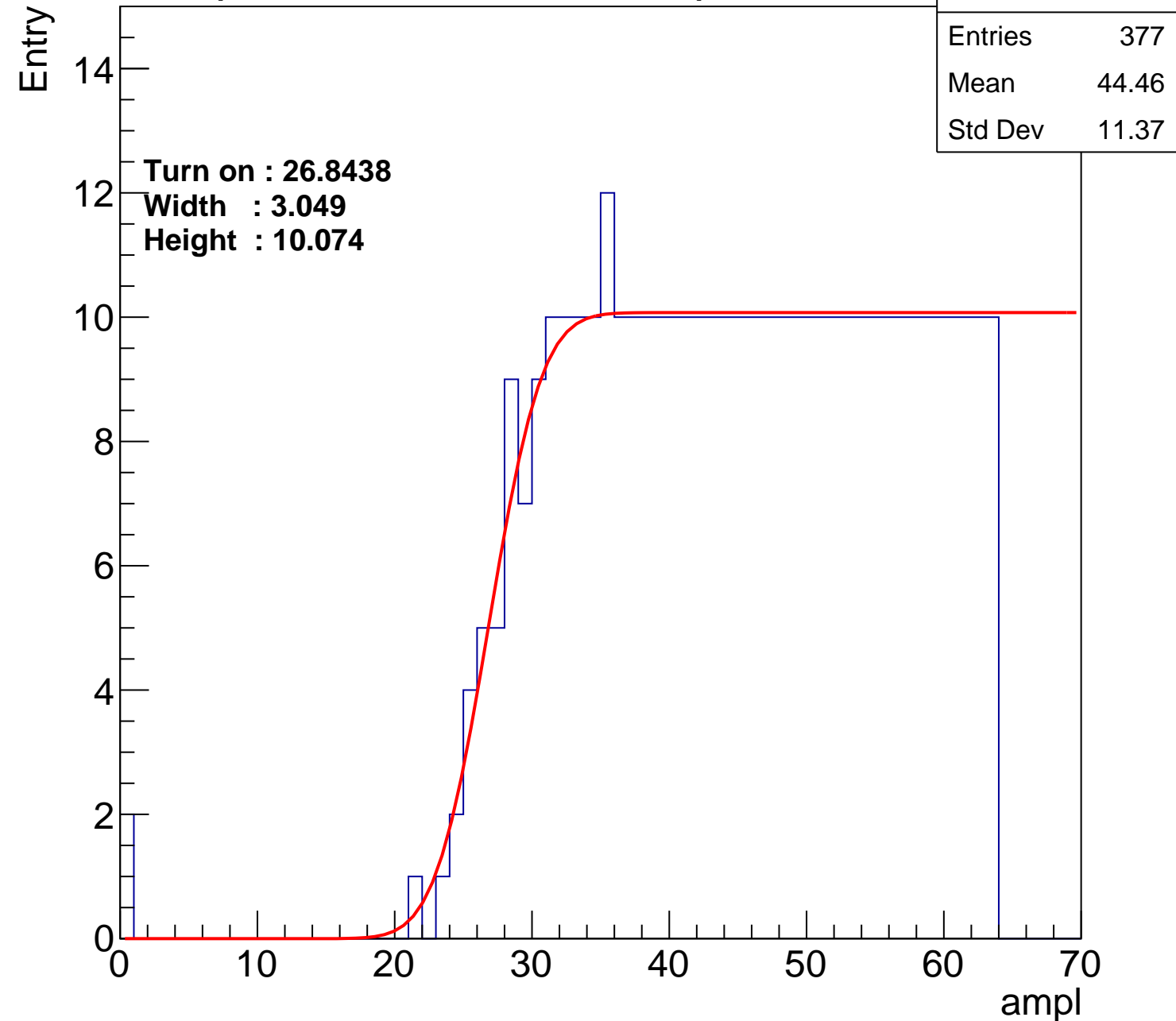
Width : 3.049

Height : 10.074

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch124

calib_packv5_042523_0143.root, FC#0, port D2

Entries	378
Mean	44.08
Std Dev	12.12

Turn on : 26.9422

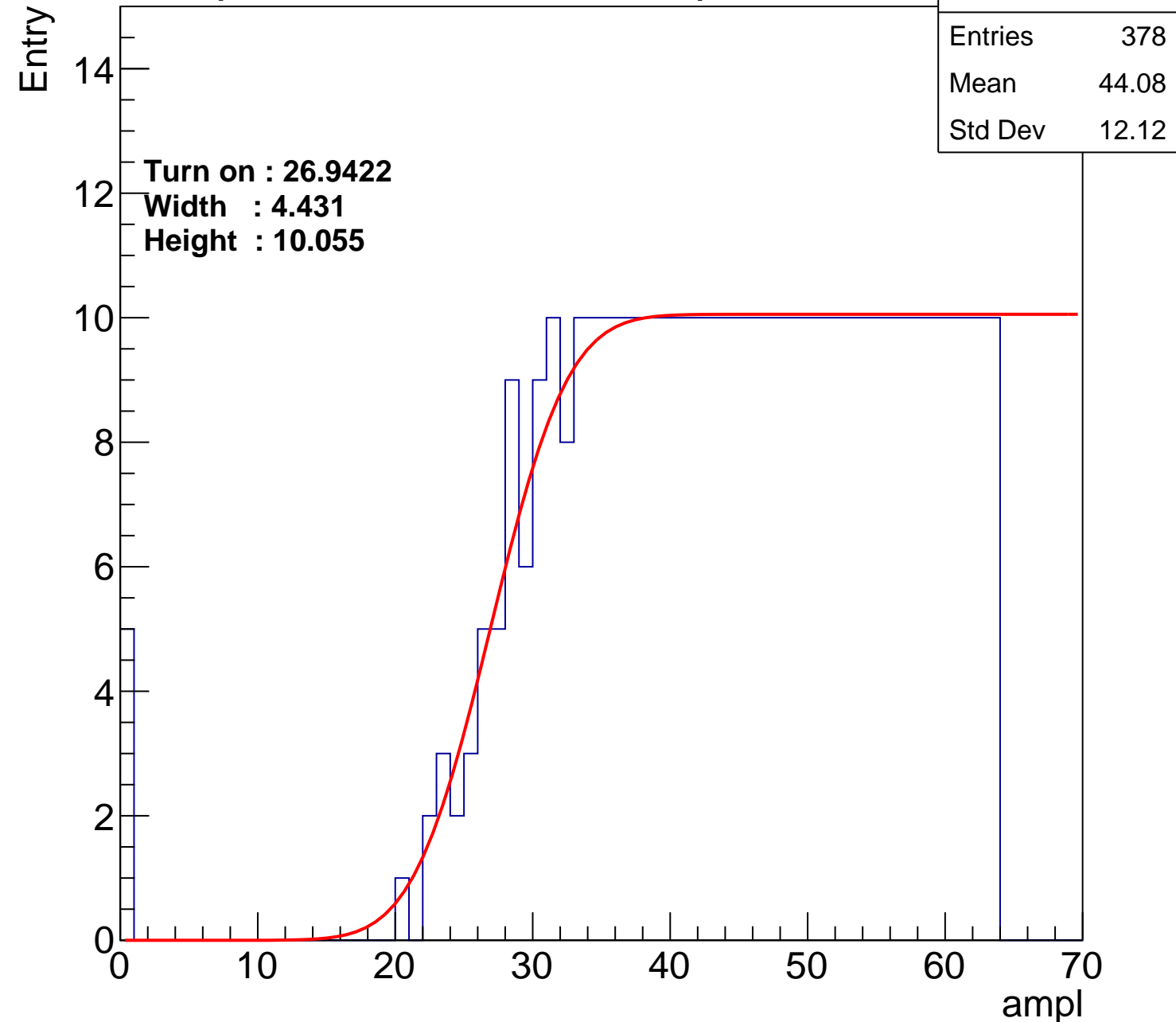
Width : 4.431

Height : 10.055

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch125

calib_packv5_042523_0143.root, FC#0, port D2

Entries	359
Mean	45.03
Std Dev	11.68

Turn on : 28.7106

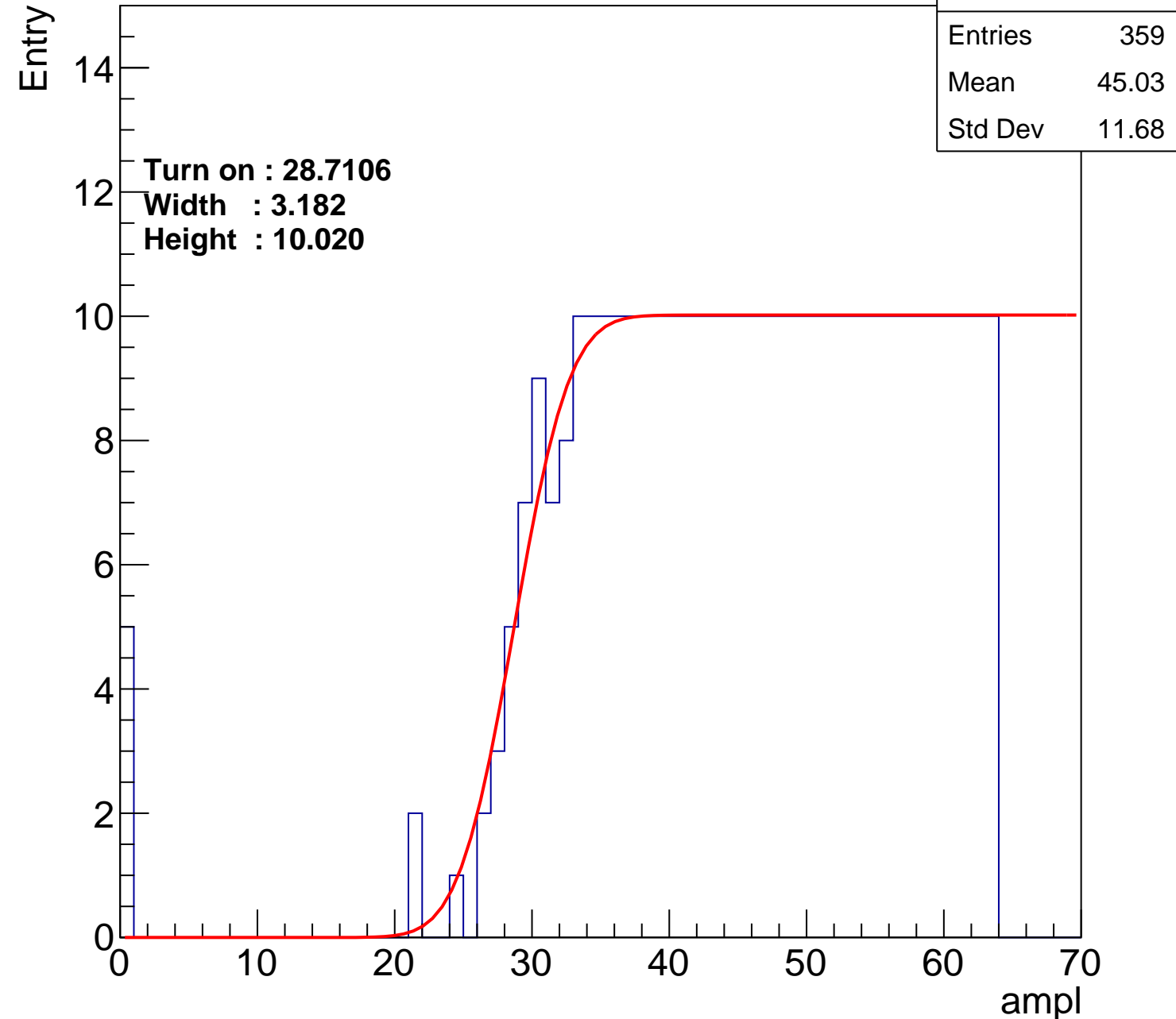
Width : 3.182

Height : 10.020

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch126

calib_packv5_042523_0143.root, FC#0, port D2

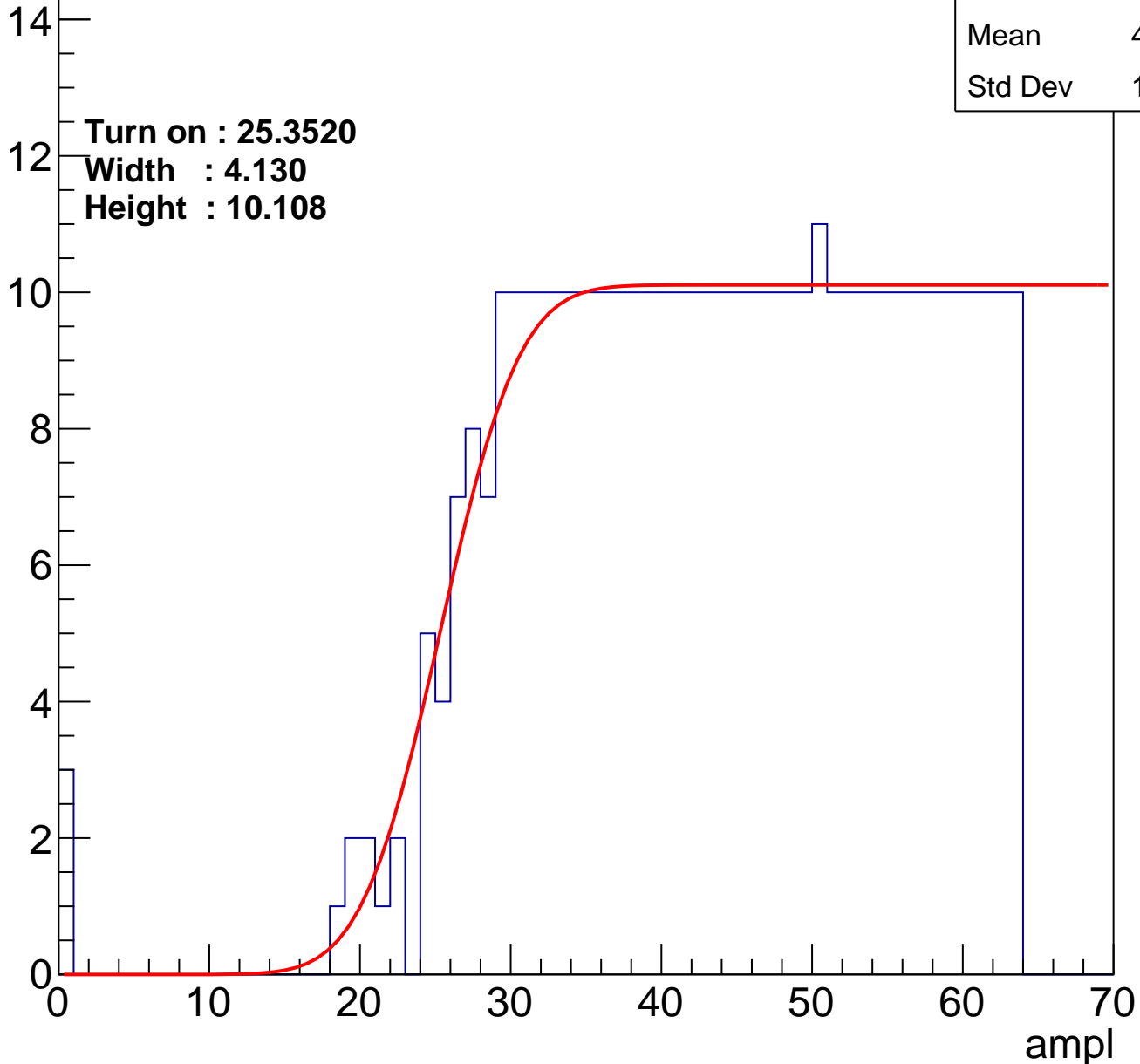
Entries	393
Mean	43.58
Std Dev	12.07

Turn on : 25.3520

Width : 4.130

Height : 10.108

Entry



B1L101S, U14-ch127

calib_packv5_042523_0143.root, FC#0, port D2

Entries	367
Mean	44.58
Std Dev	12.01

Turn on : 28.0955

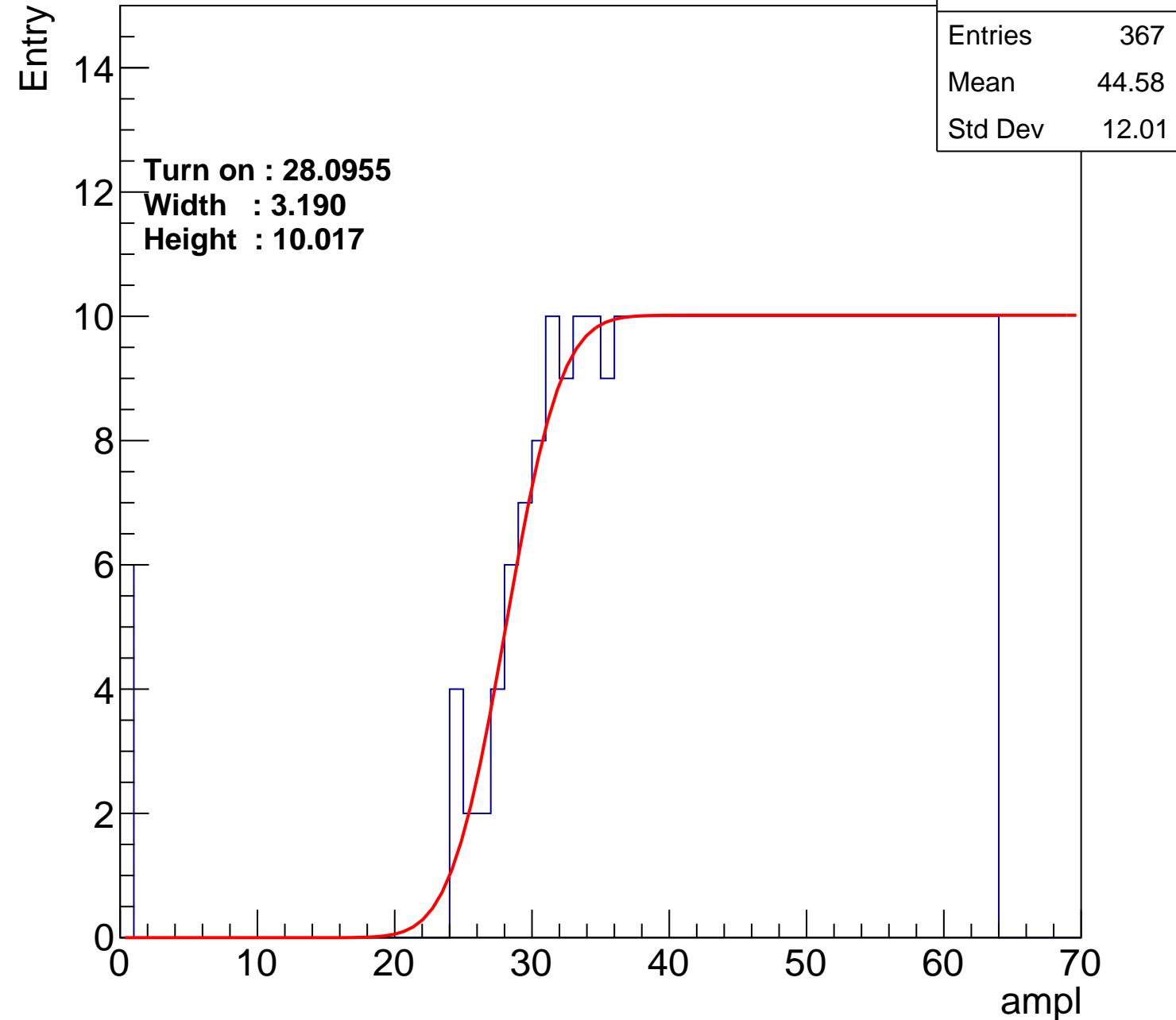
Width : 3.190

Height : 10.017

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U14-ch127

calib_packv5_042523_0143.root, FC#0, port D2

Entries	367
Mean	44.58
Std Dev	12.01

Turn on : 28.0955

Width : 3.190

Height : 10.017

Entry

14
12
10
8
6
4
2
0

ampl

