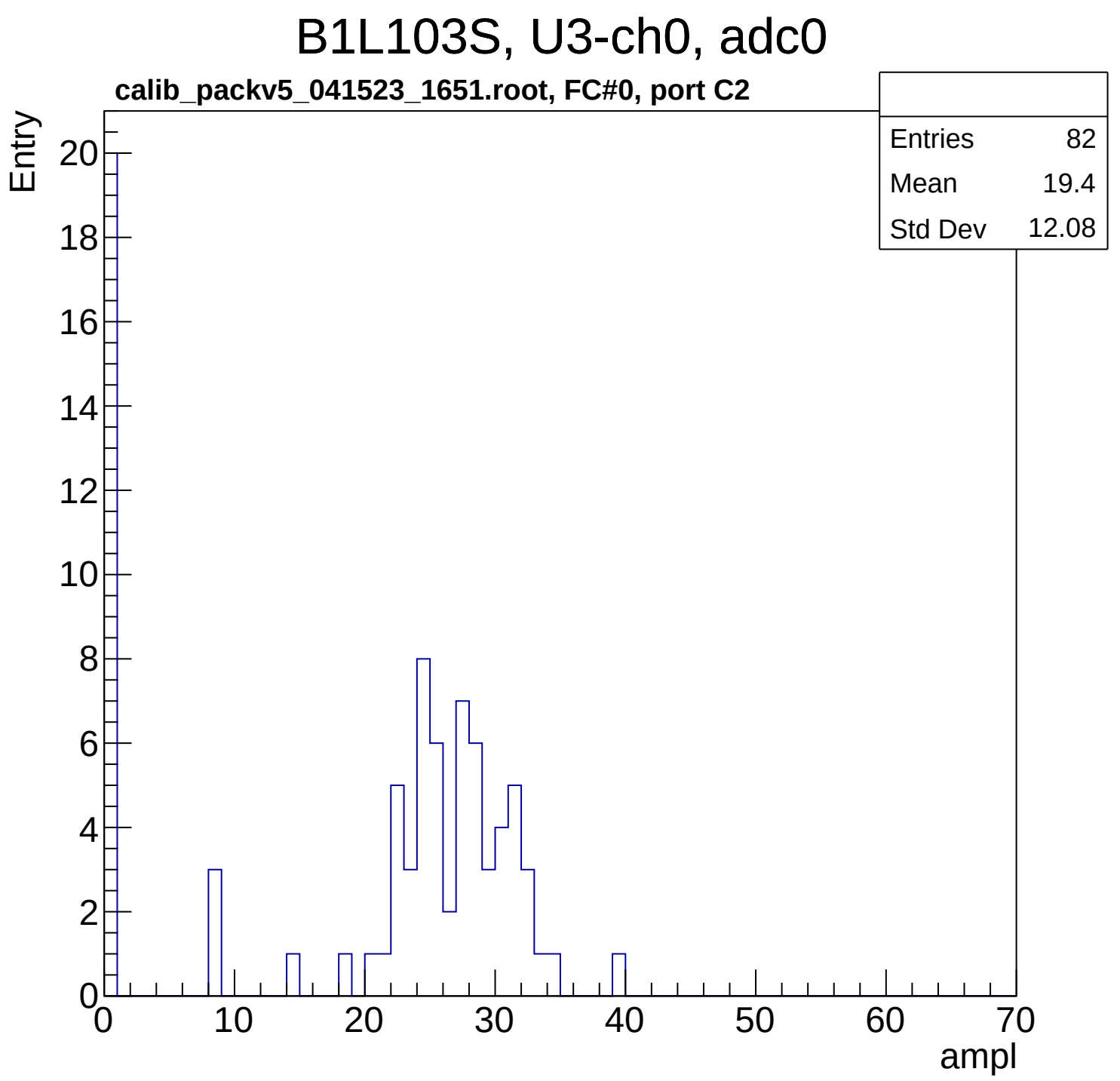
B1L103S, U3-ch0, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 19.4
Std Dev 12.08
Entry
ampl
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6
8
10
12
14
16
18
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0
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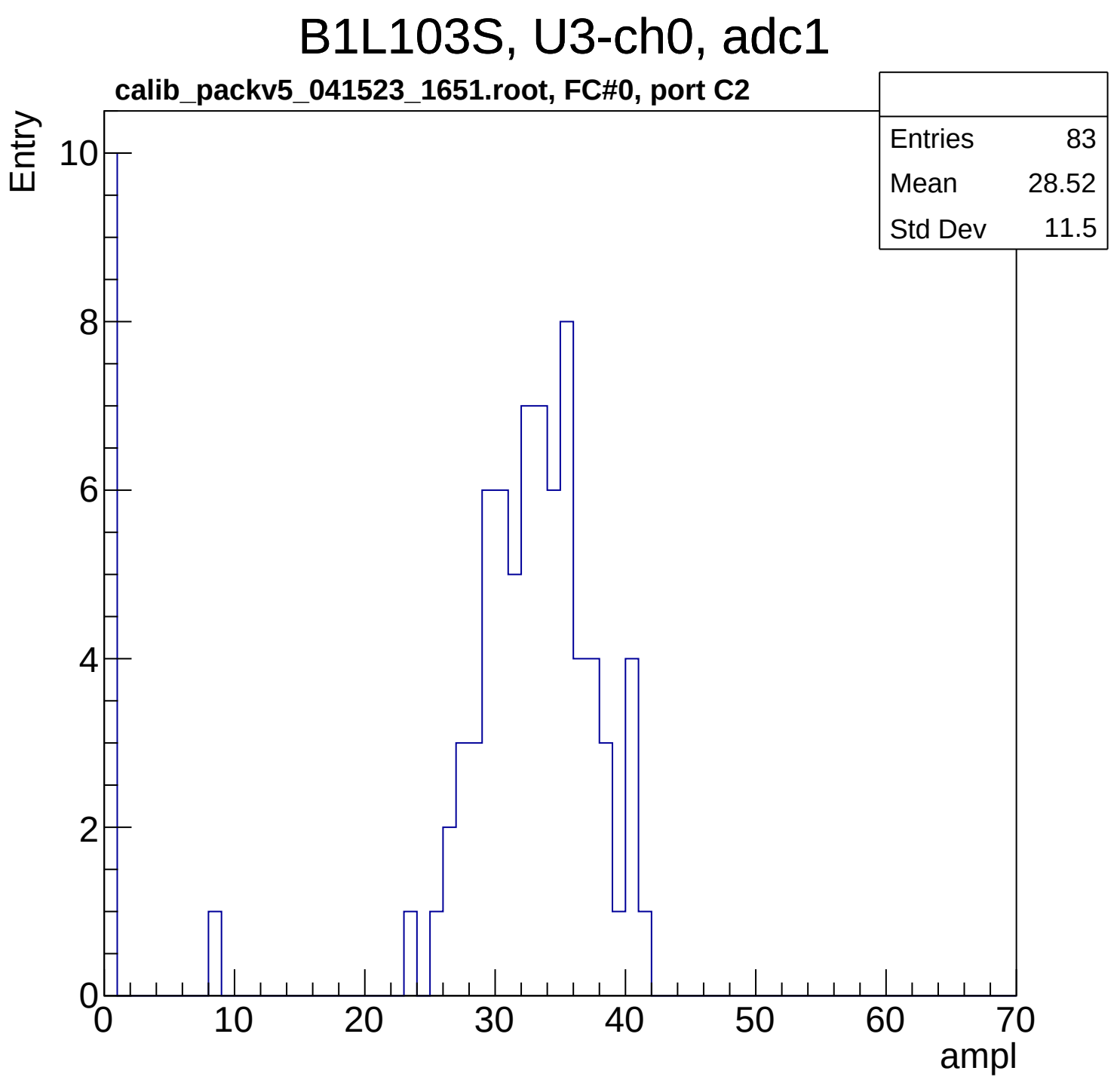
B1L103S, U3-ch0, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 28.52
Std Dev 11.5
Entry
ampl
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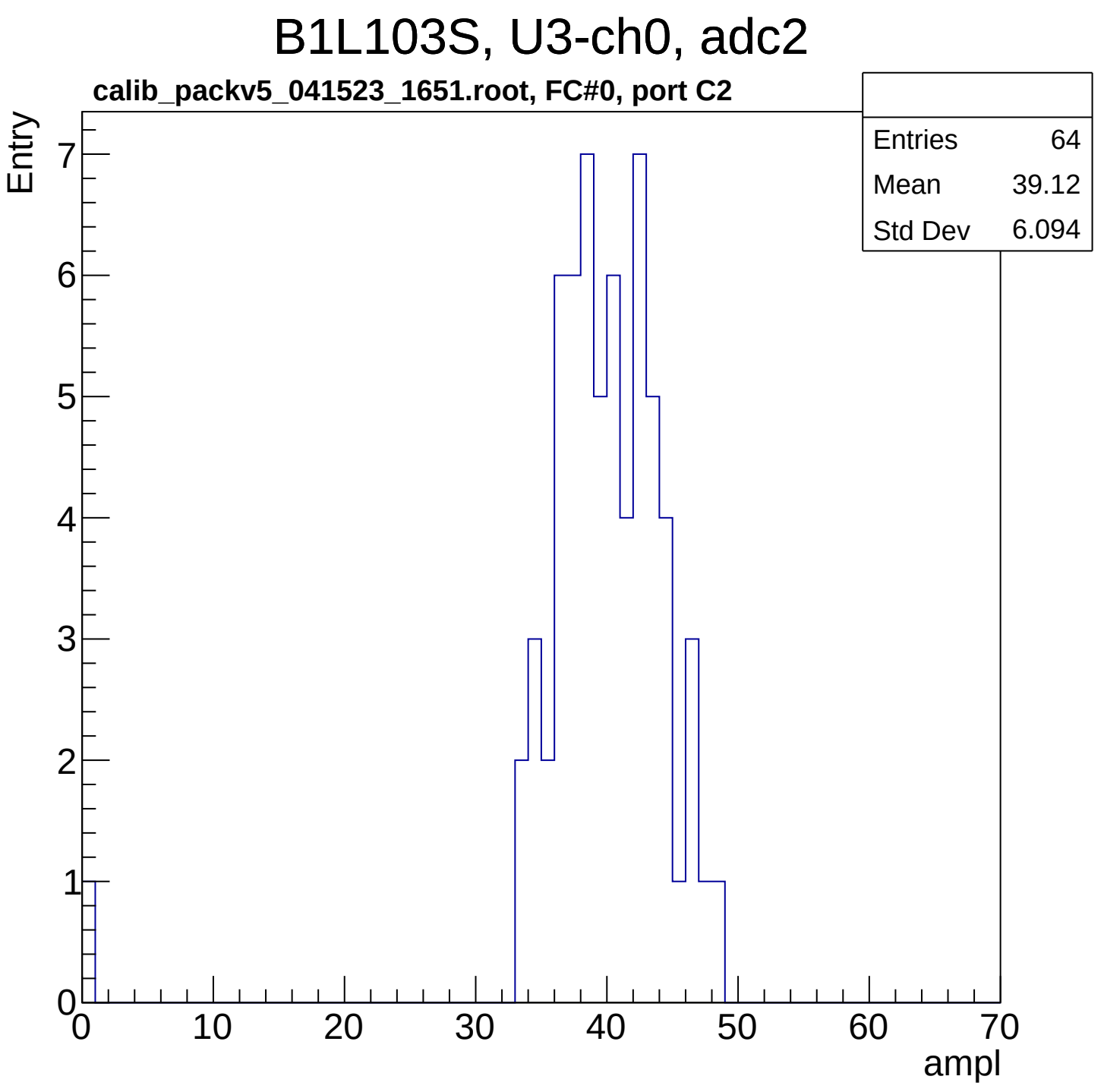
B1L103S, U3-ch0, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 39.12
Std Dev 6.094
Entry
ampl
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1
2
3
4
5
6
7
0
10
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40
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60
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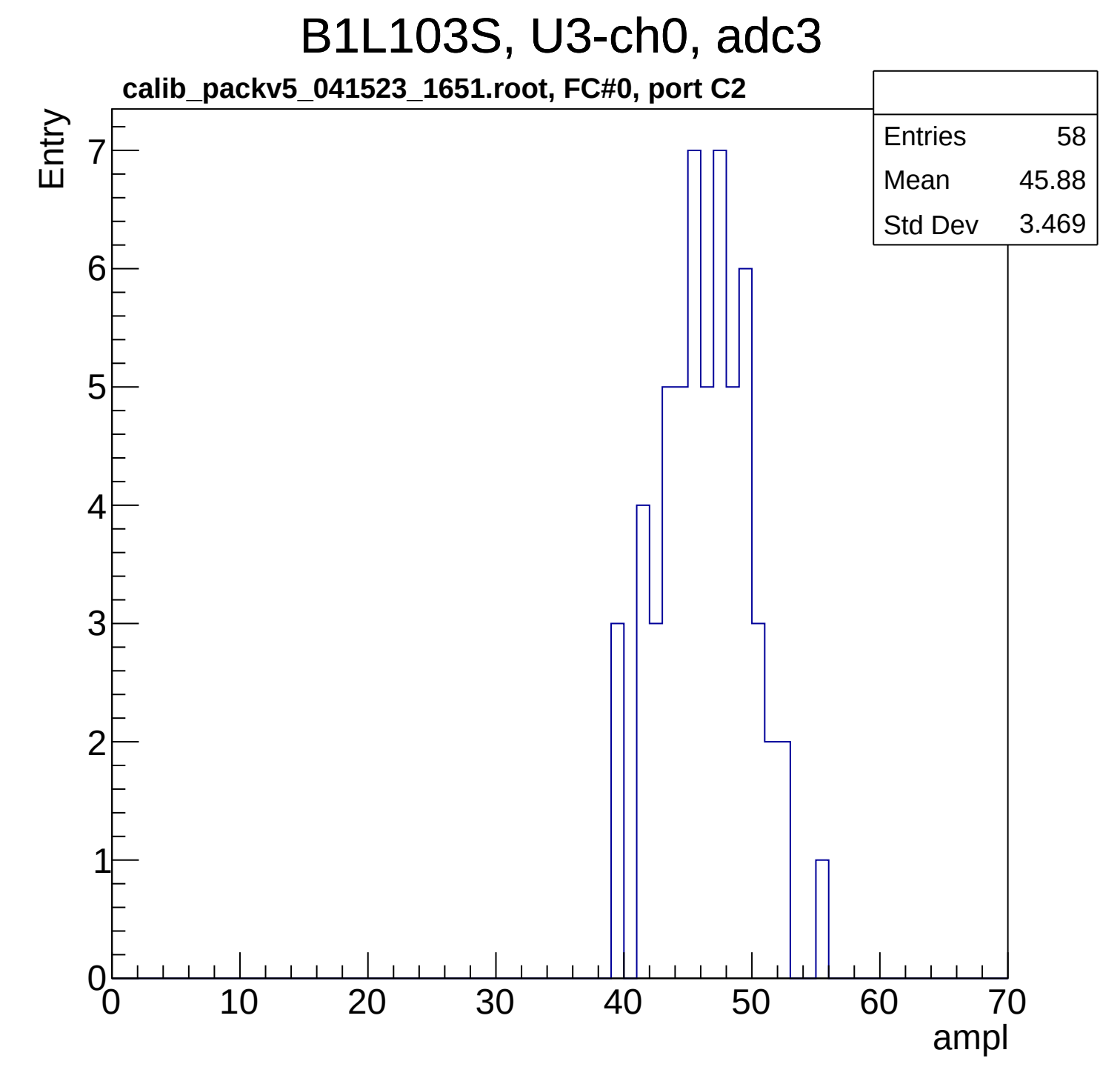
B1L103S, U3-ch0, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 45.88
Std Dev 3.469
Entry
ampl
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1
2
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4
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6
7
0
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60
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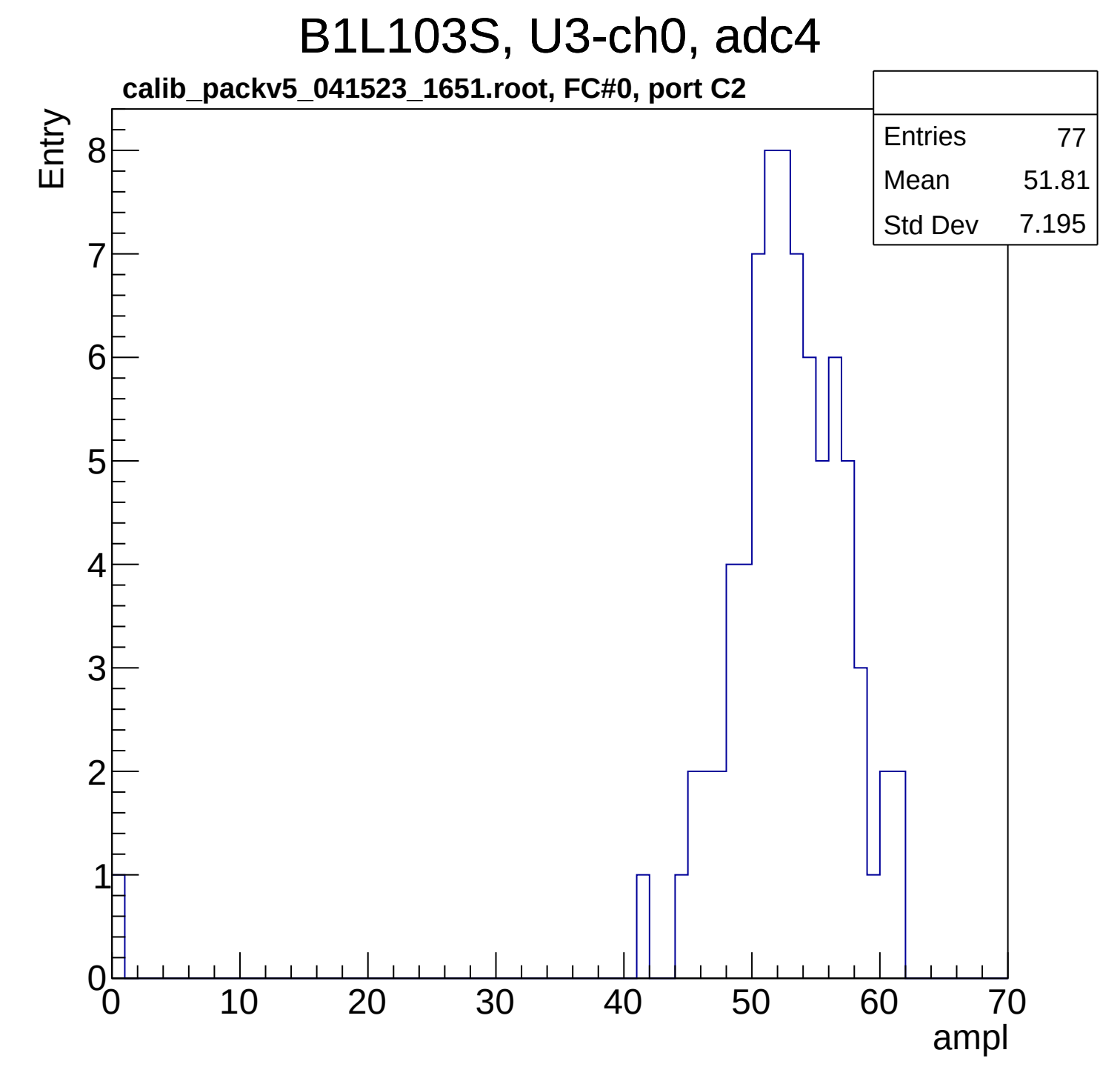
B1L103S, U3-ch0, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 51.81
Std Dev 7.195
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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40
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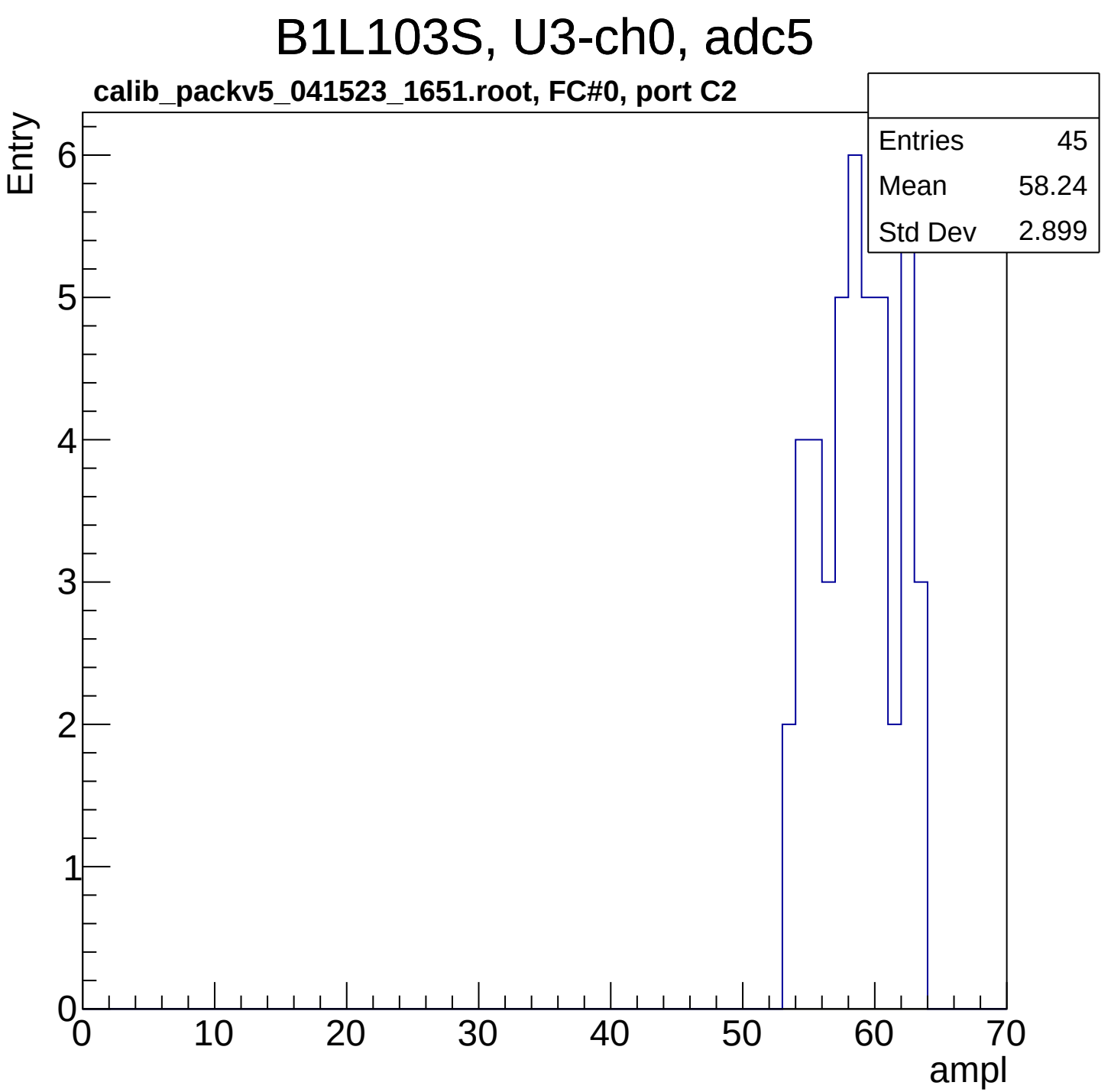
B1L103S, U3-ch0, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 58.24
Std Dev 2.899
Entry
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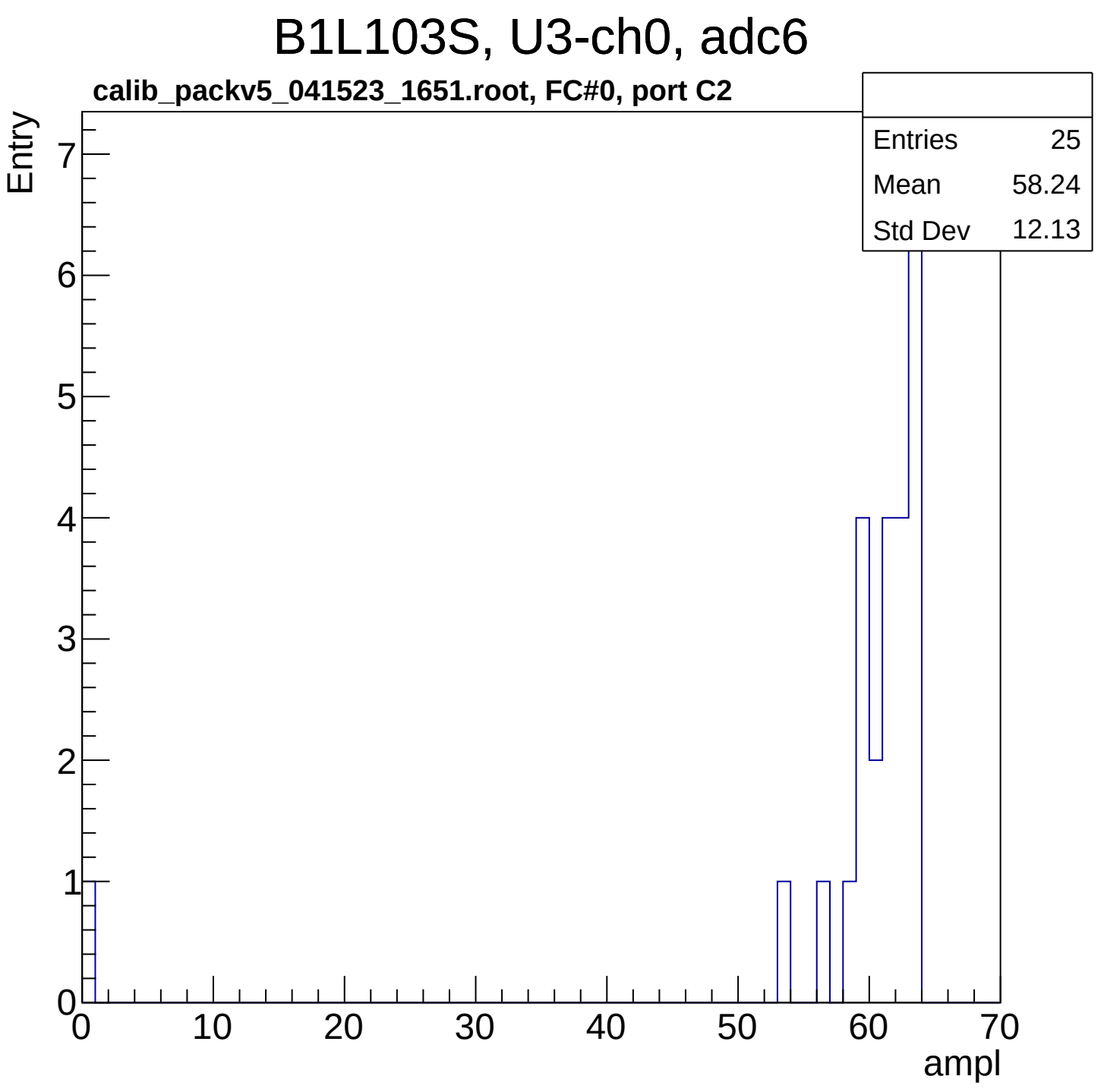
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch0, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 58.24
Std Dev 12.13
Entry
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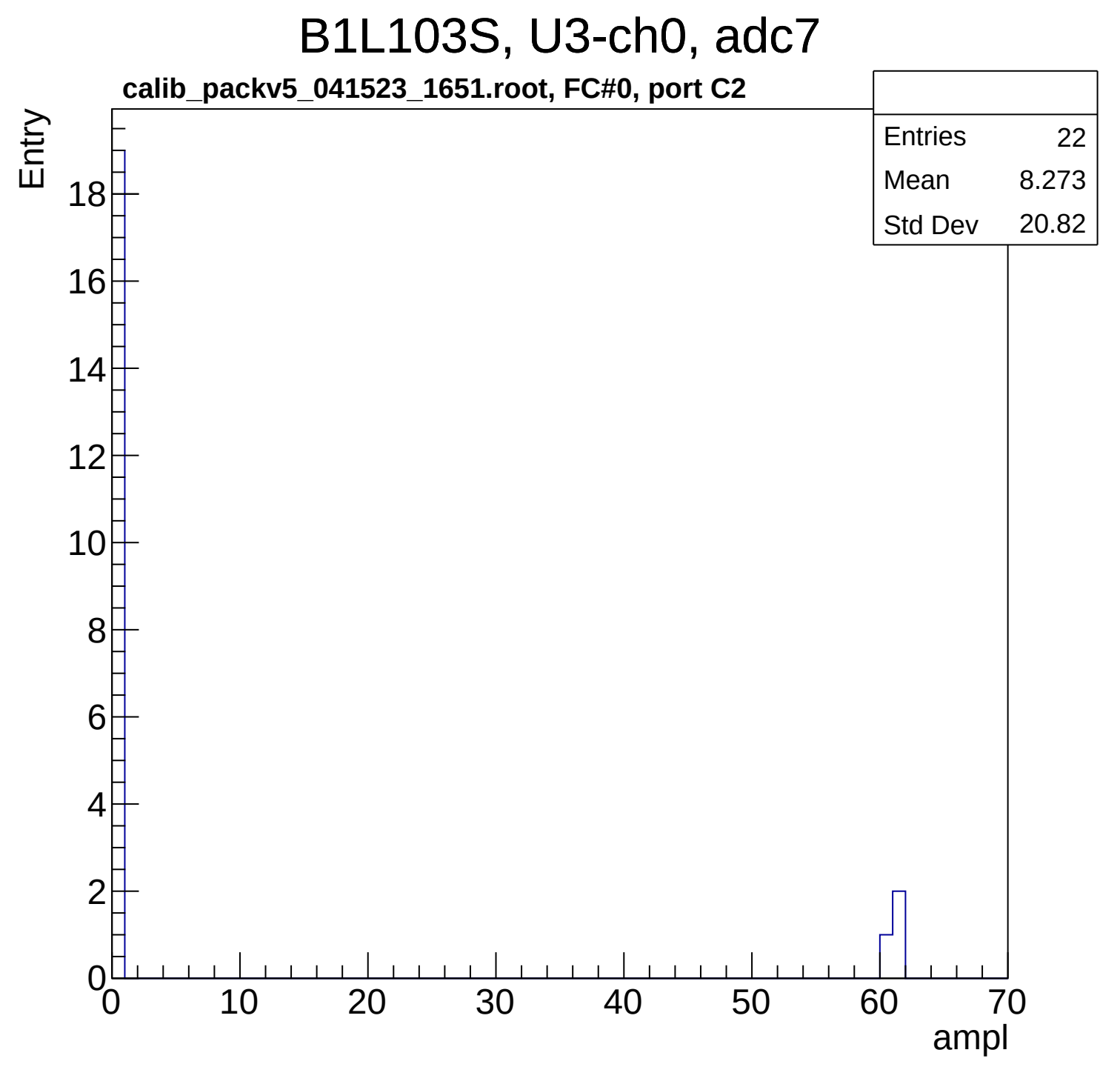
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch0, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.273
Std Dev 20.82
Entry
0
2
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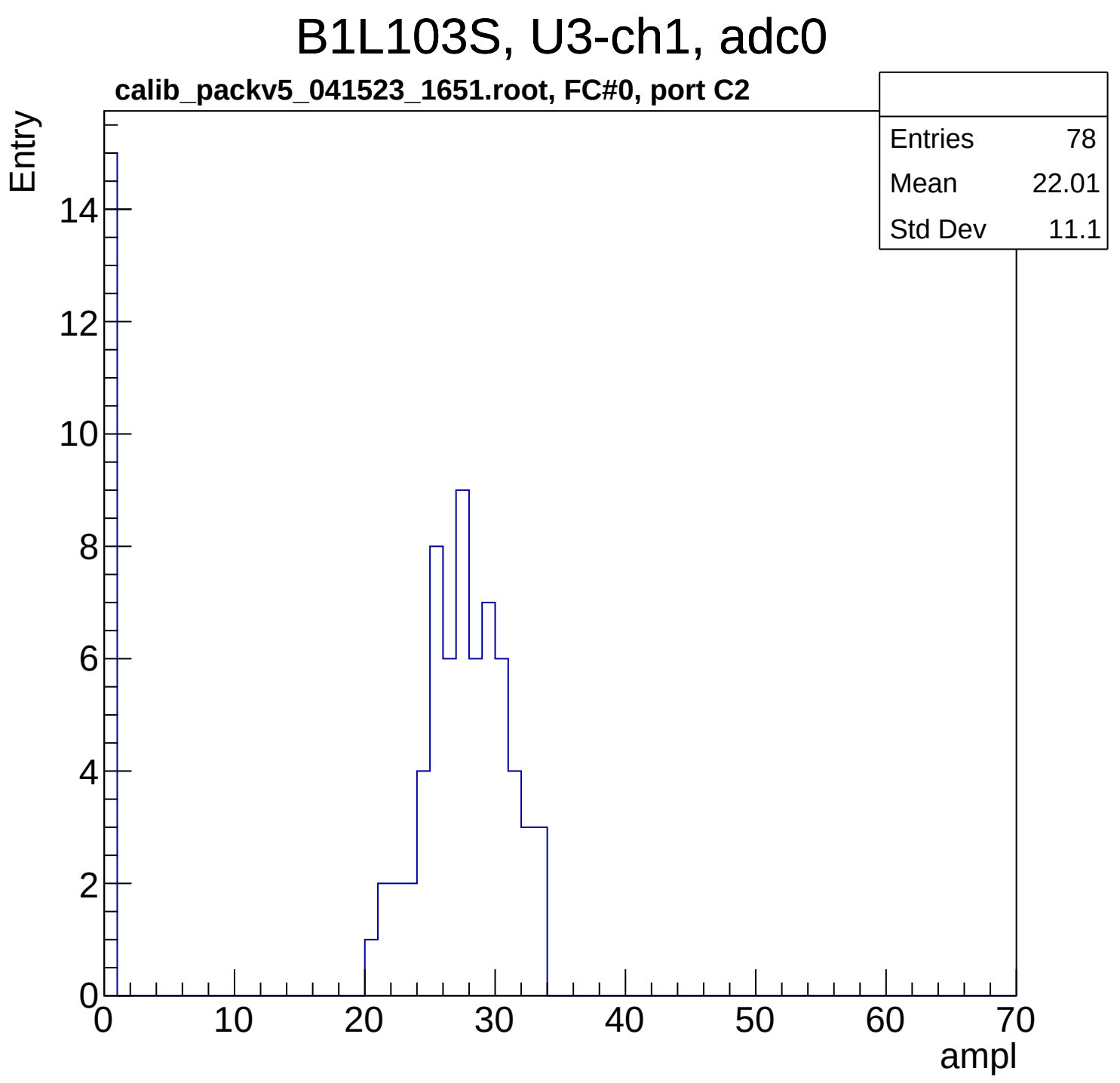
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch1, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 22.01
Std Dev 11.1
Entry
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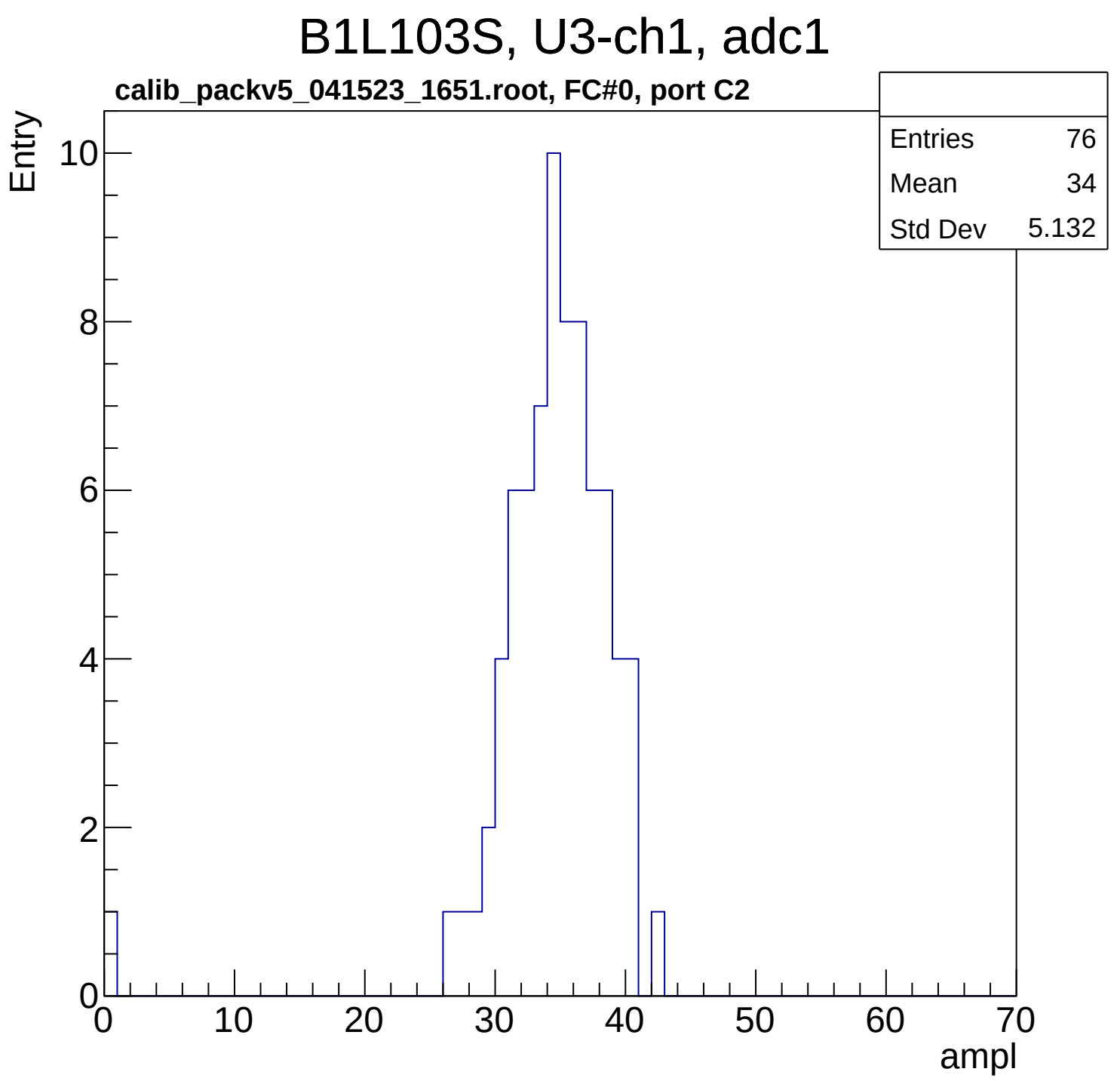
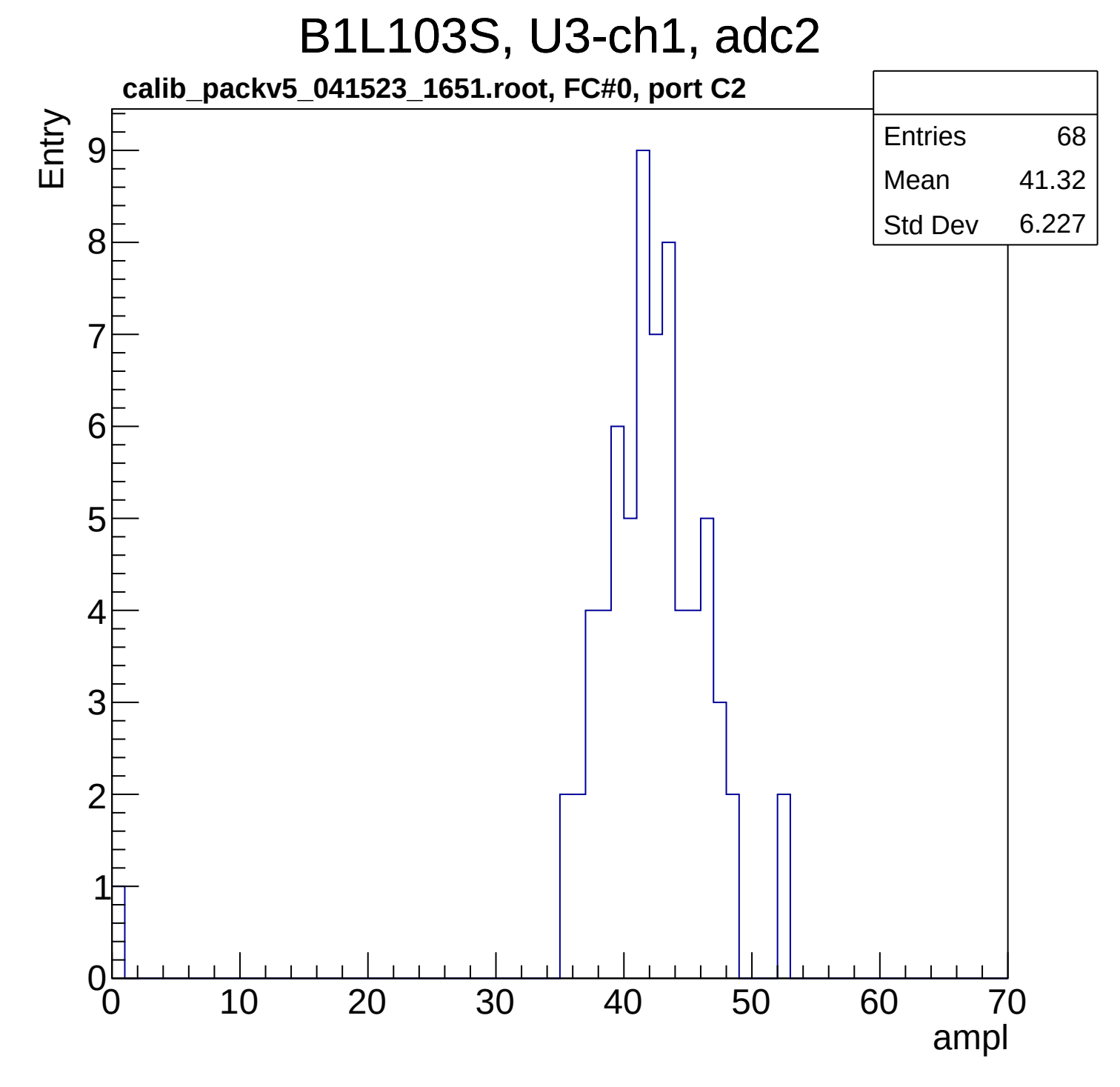
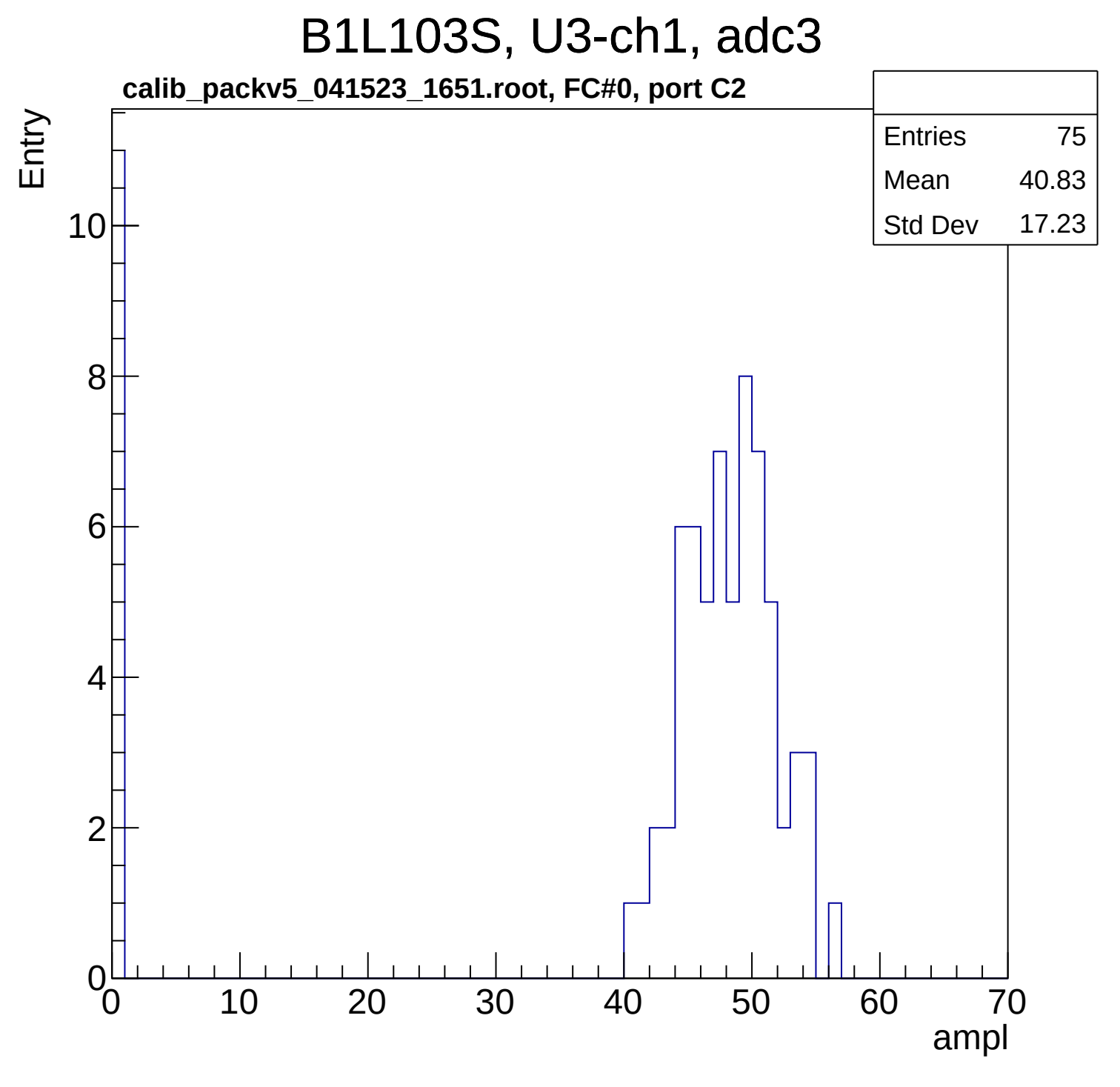
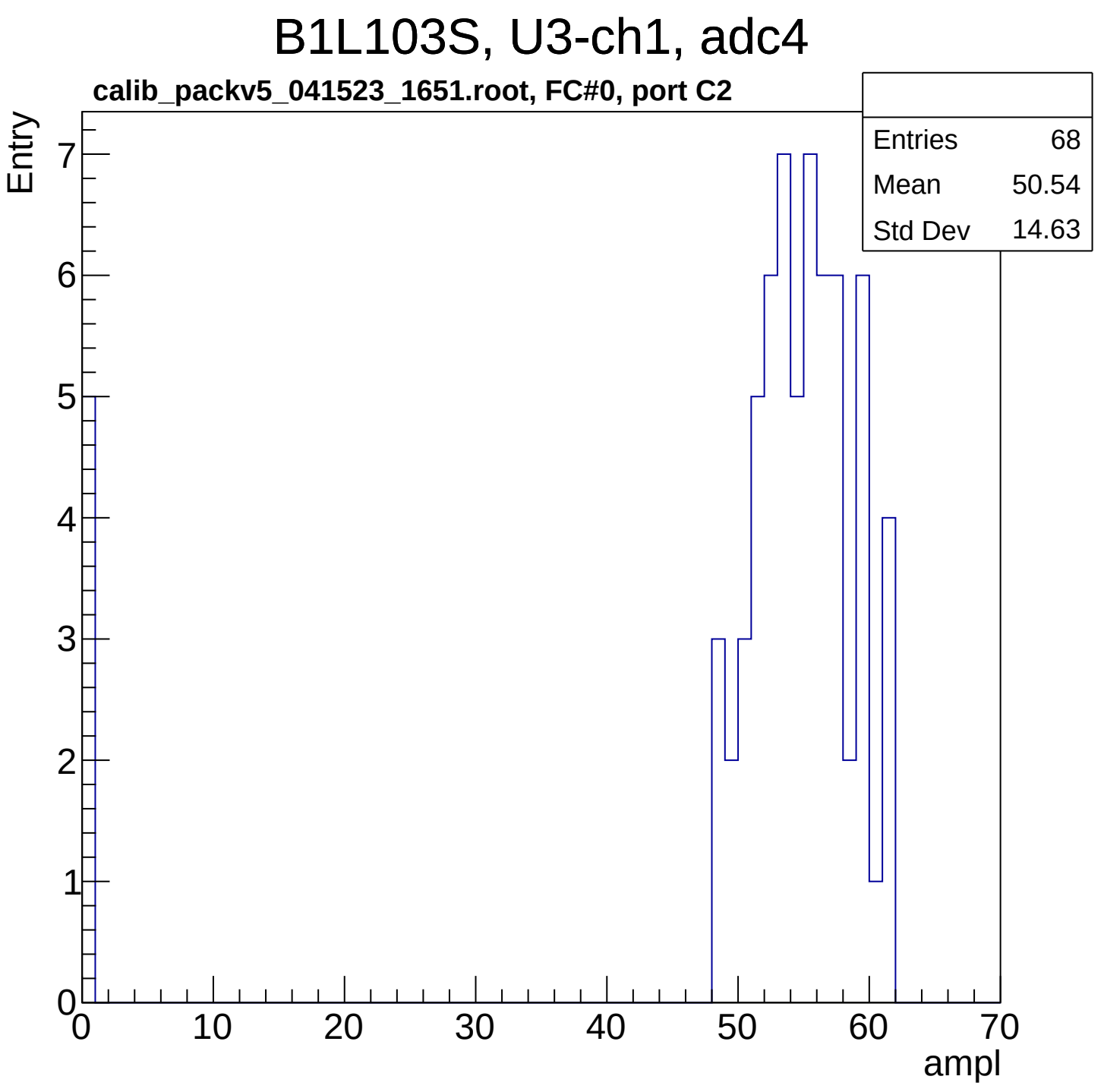
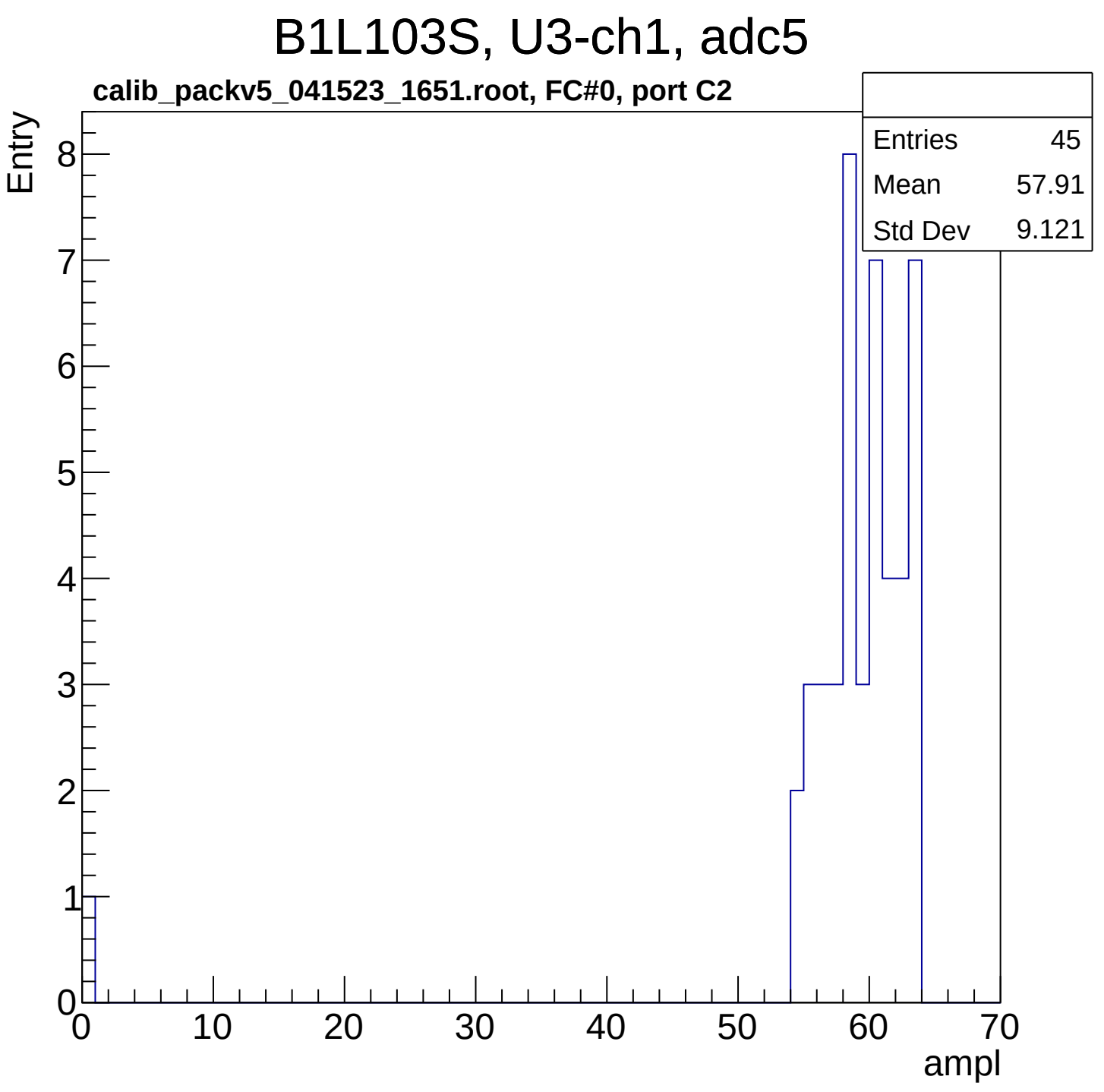
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

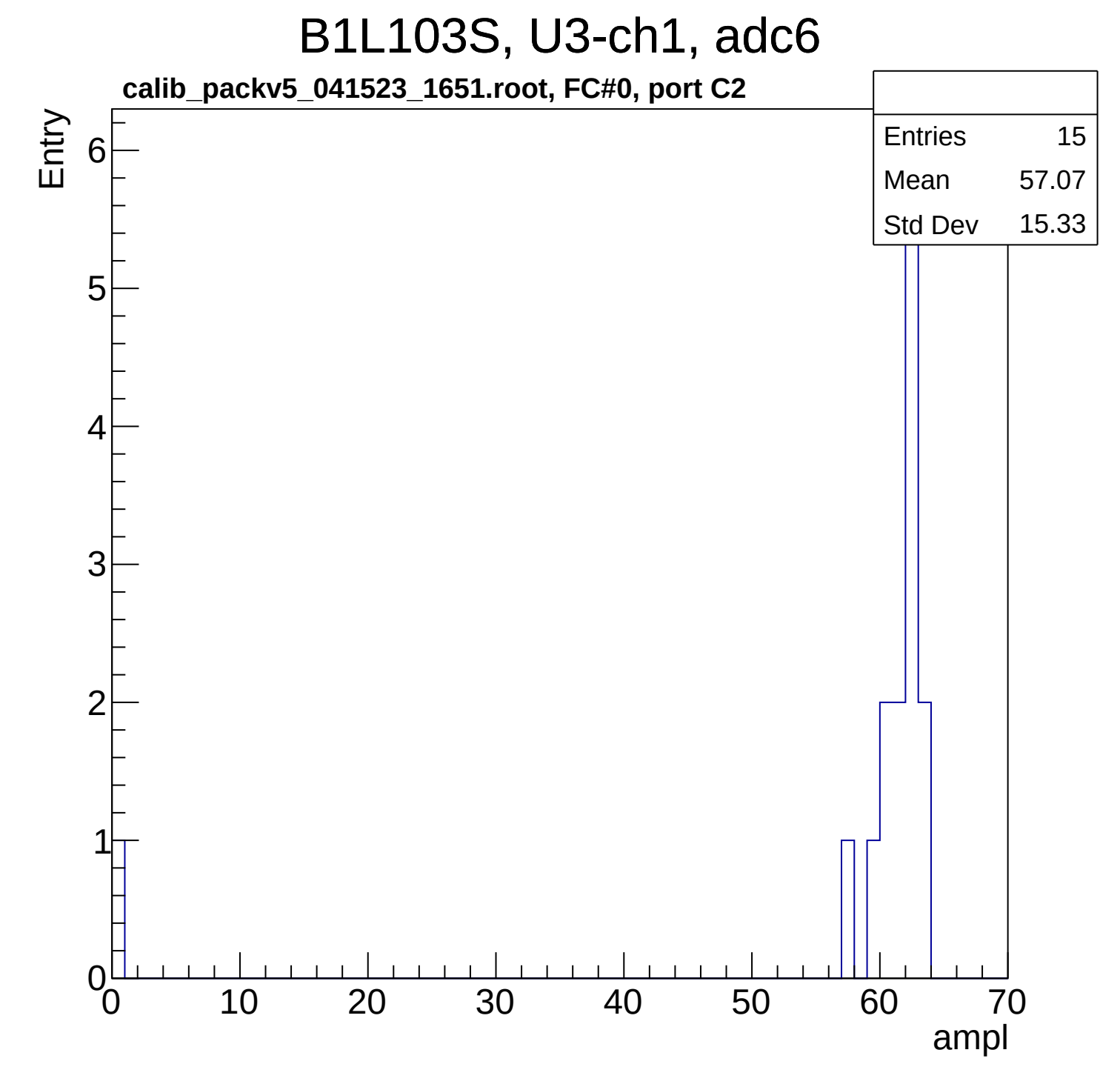

B1L103S, U3-ch1, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 34
Std Dev 5.132
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

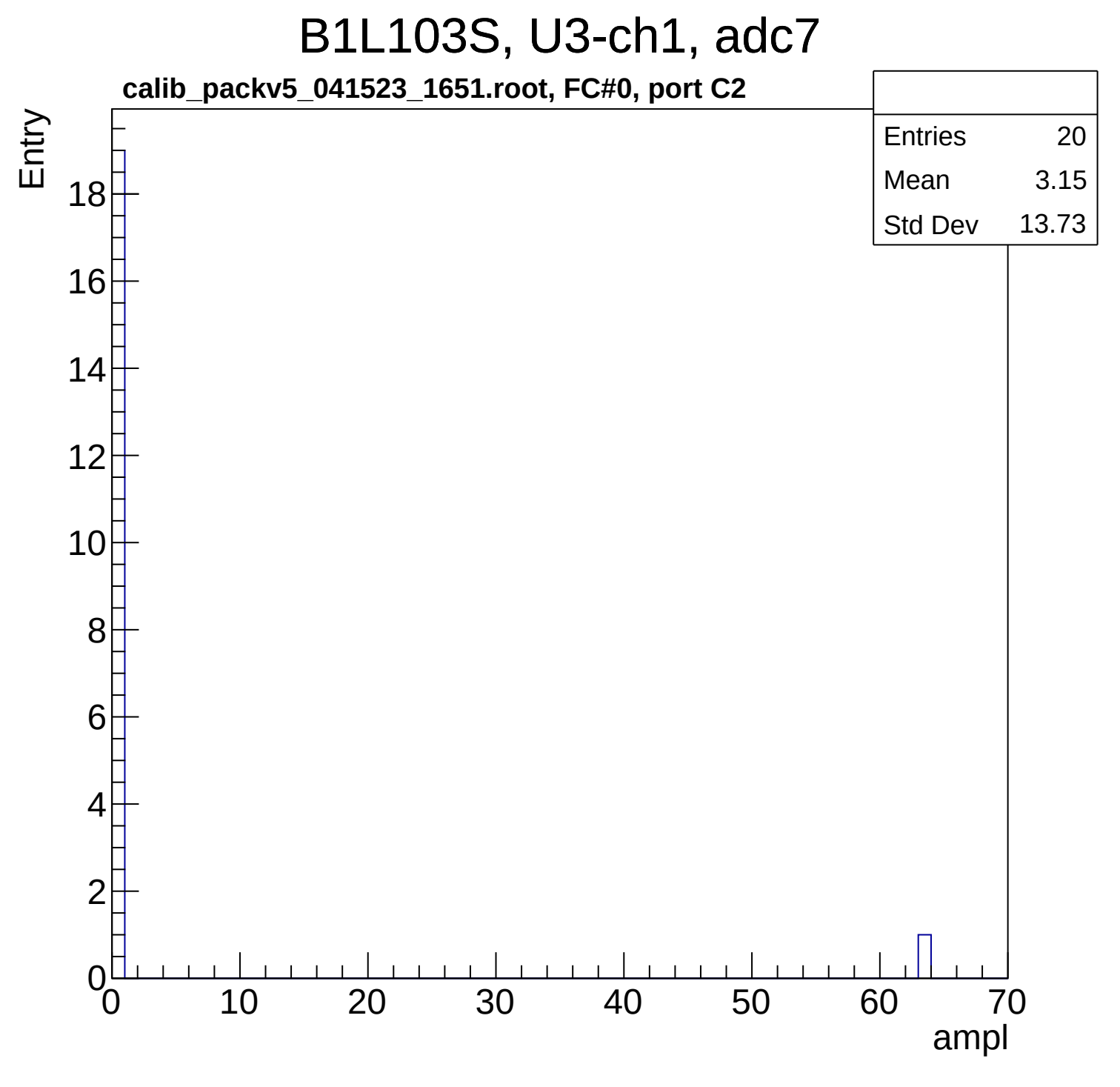

B1L103S, U3-ch1, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 41.32
Std Dev 6.227
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

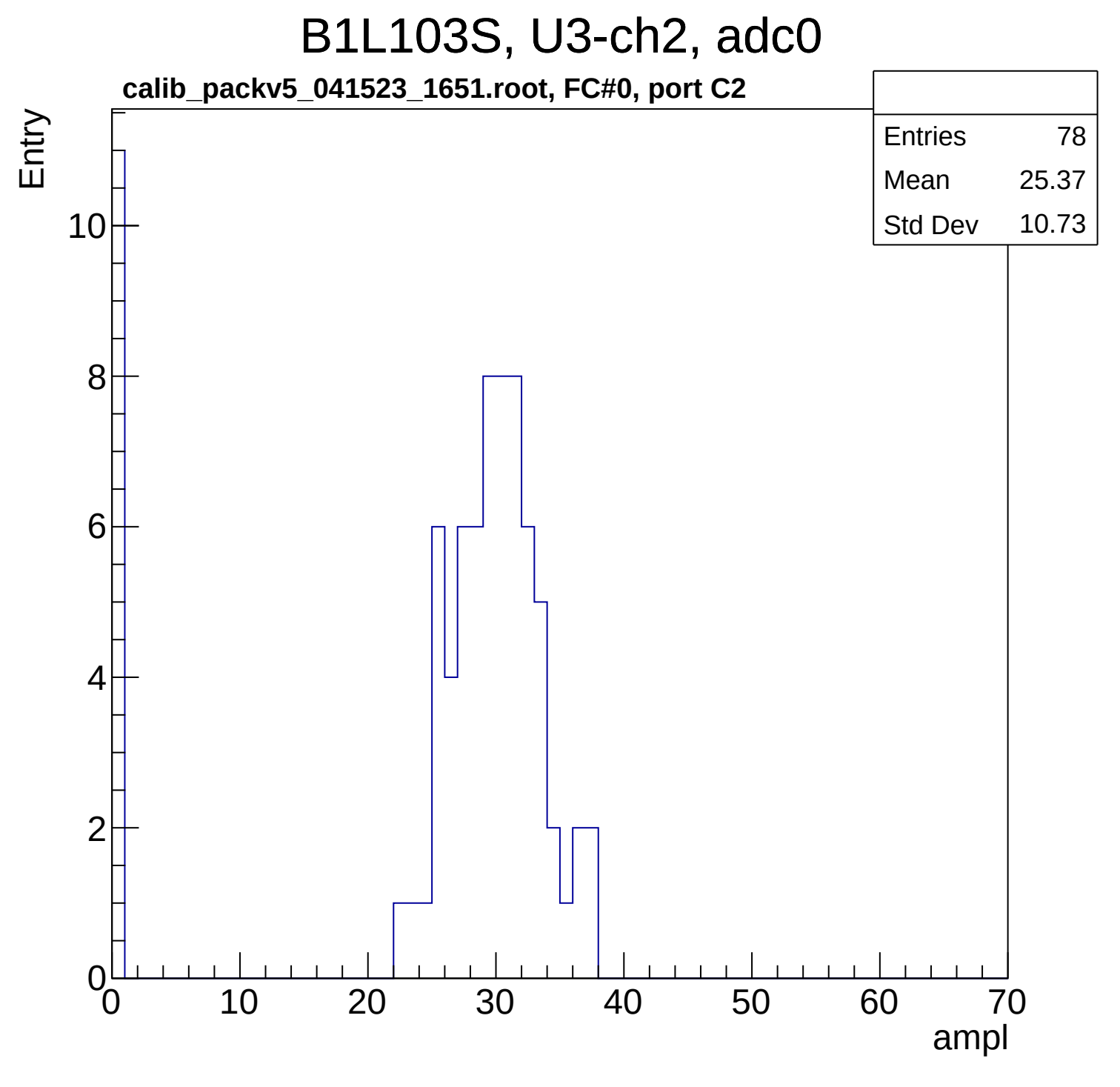

B1L103S, U3-ch1, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 40.83
Std Dev 17.23
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

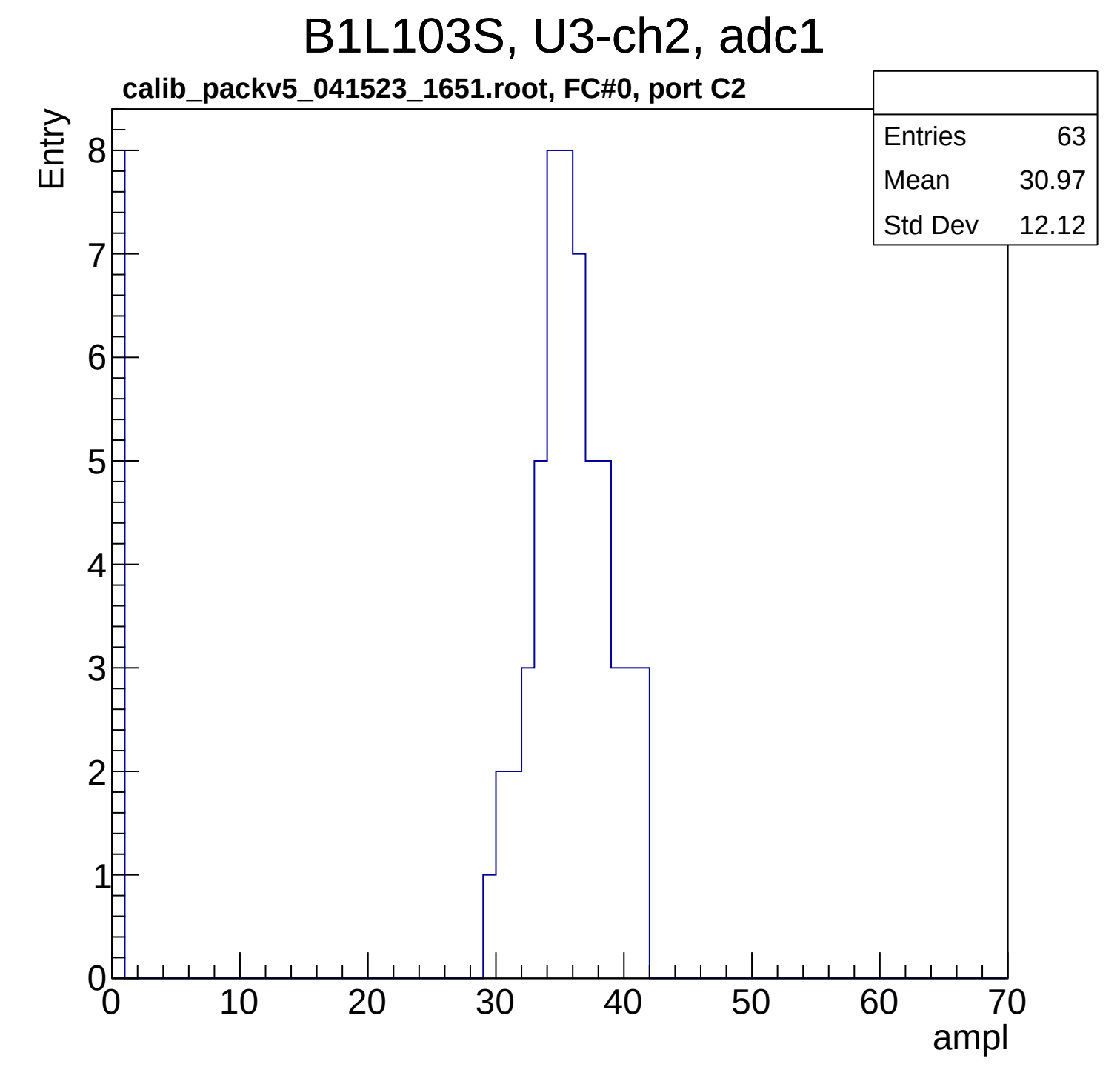

B1L103S, U3-ch1, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 50.54
Std Dev 14.63
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch1, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 57.91
Std Dev 9.121
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch1, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 57.07
Std Dev 15.33
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U3-ch1, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch2, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 25.37
Std Dev 10.73
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch2, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 30.97
Std Dev 12.12
Entry
ampl
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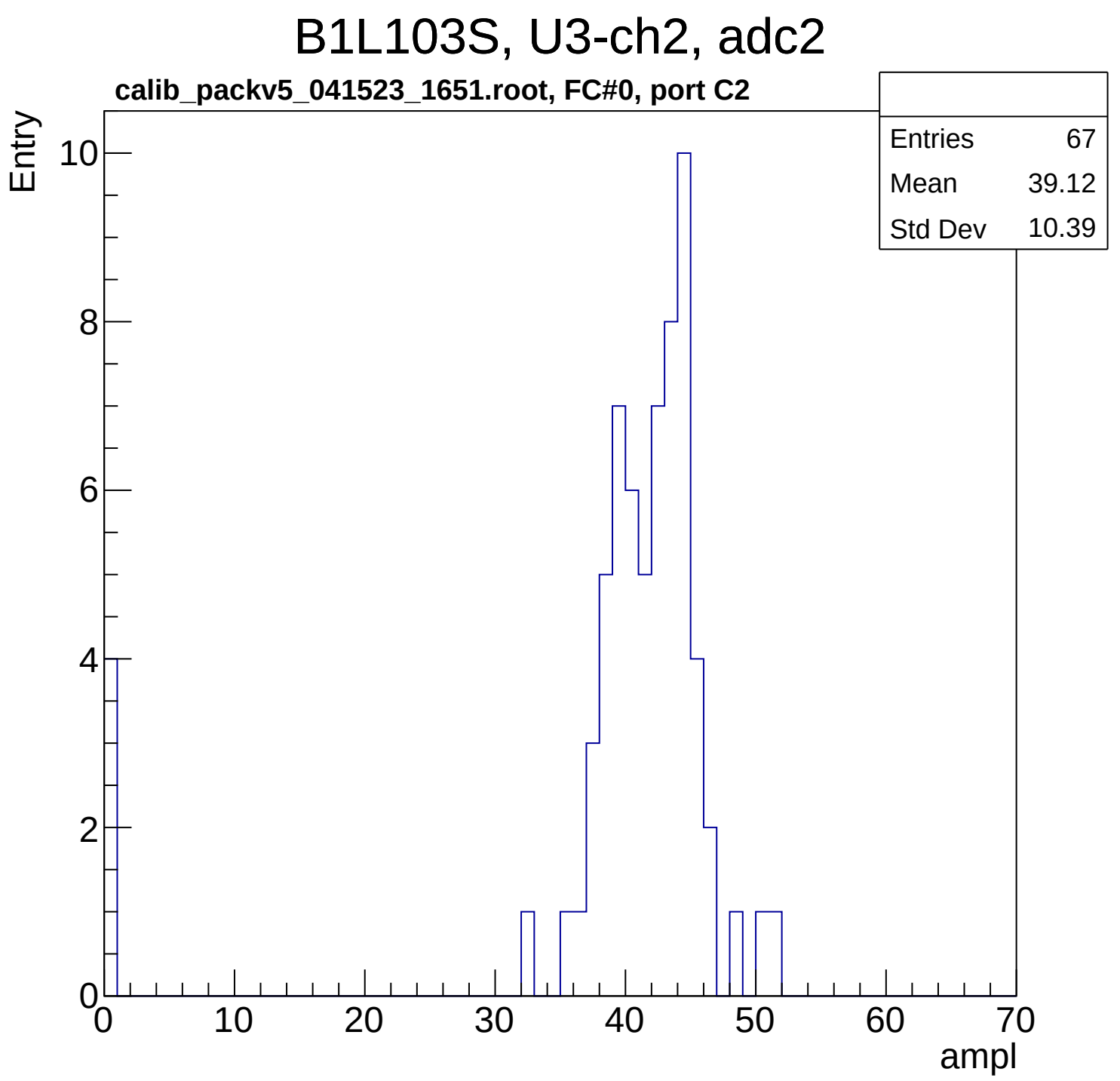
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch2, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 39.12
Std Dev 10.39
Entry
ampl
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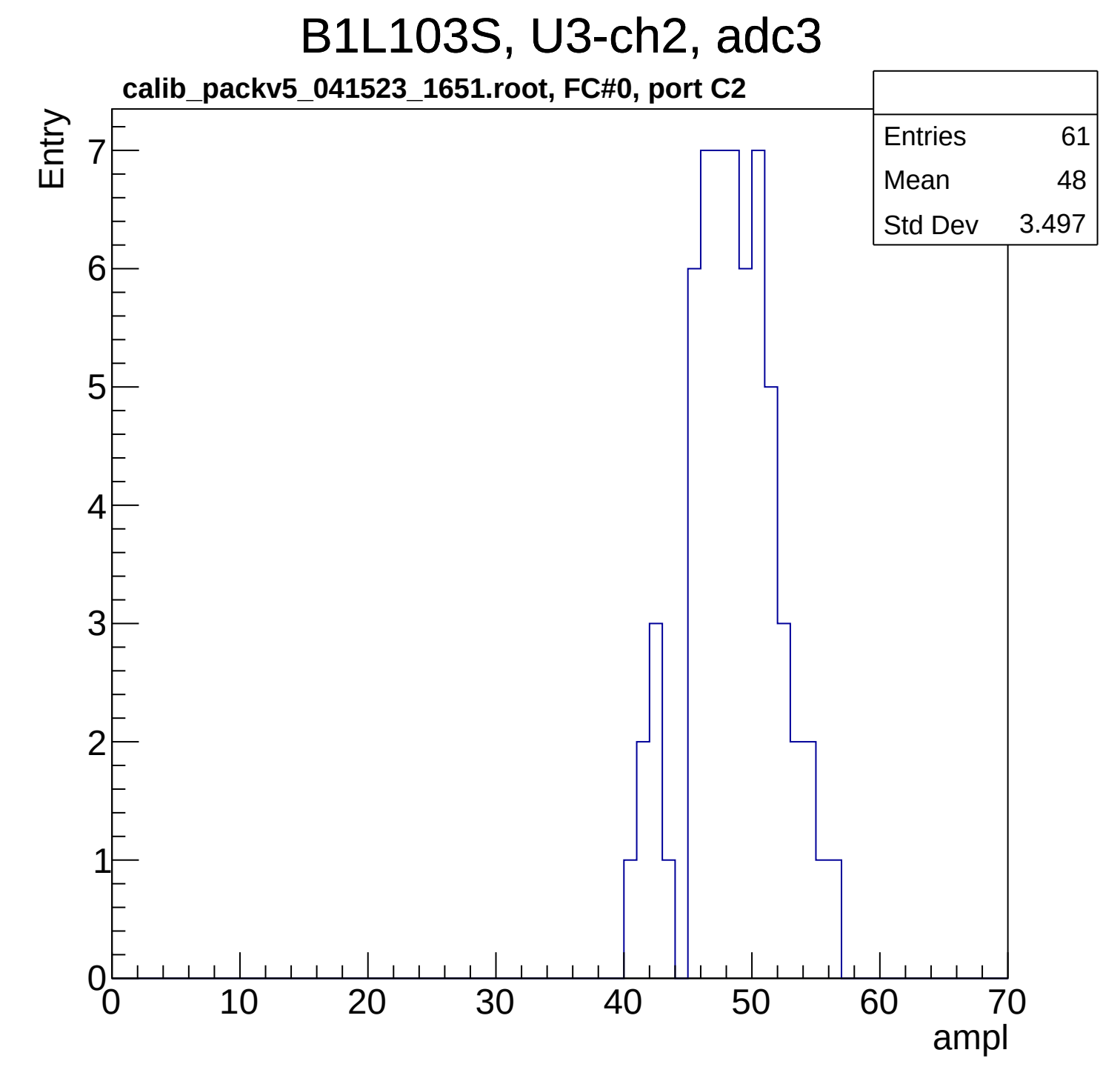
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U3-ch2, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 48
Std Dev 3.497
Entry
ampl
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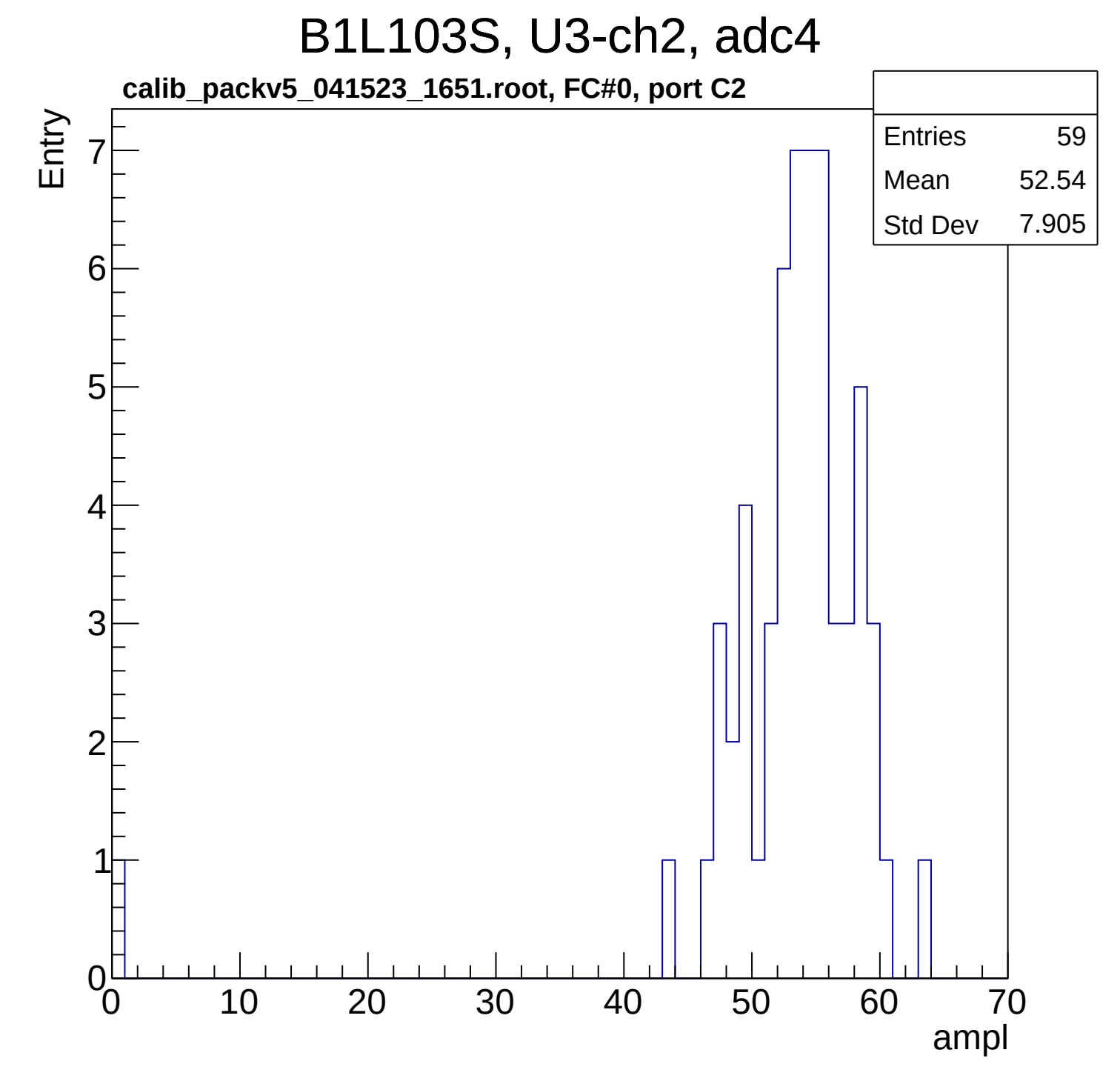
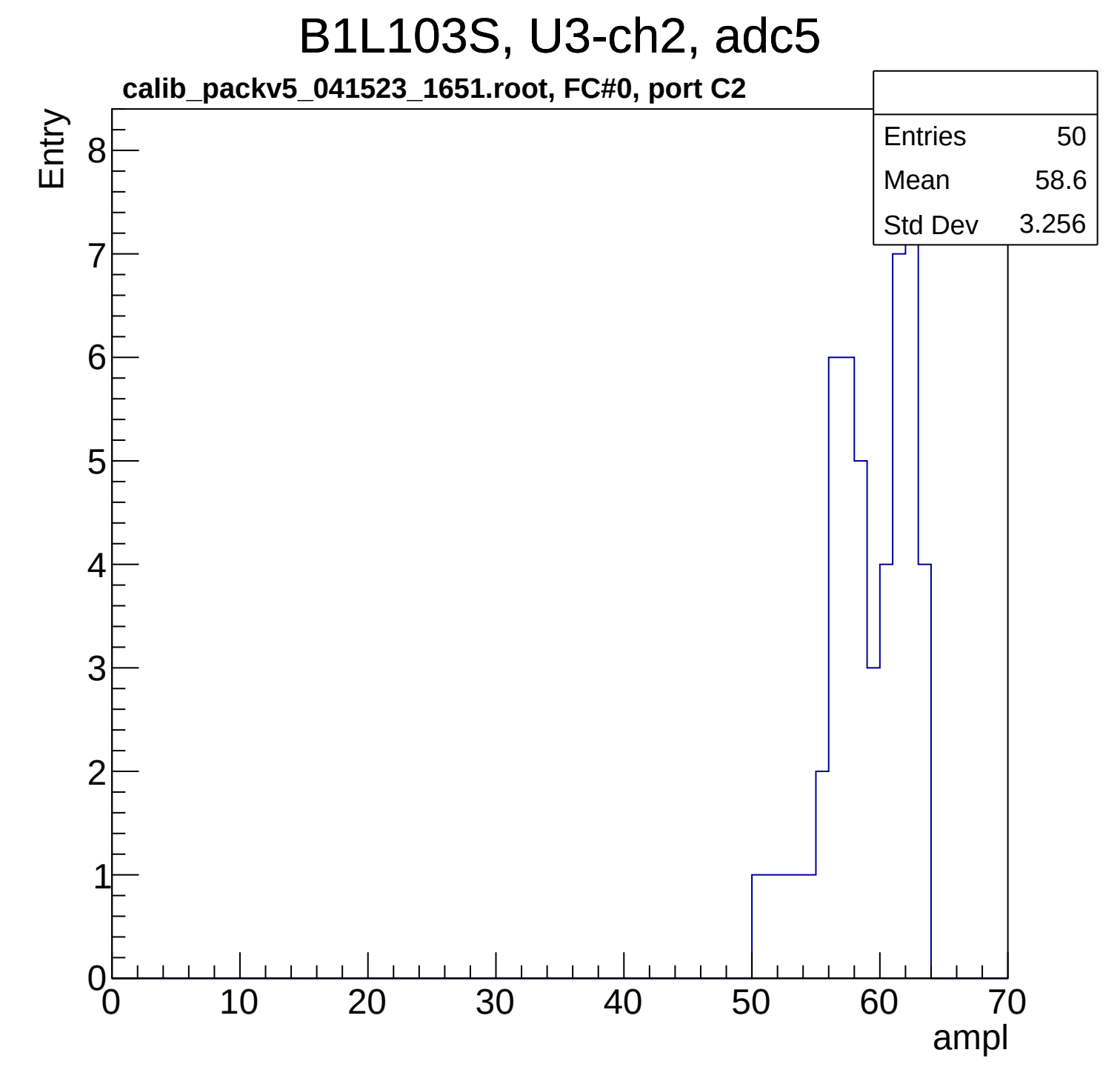
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch2, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 52.54
Std Dev 7.905
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch2, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 58.6
Std Dev 3.256
Entry
ampl
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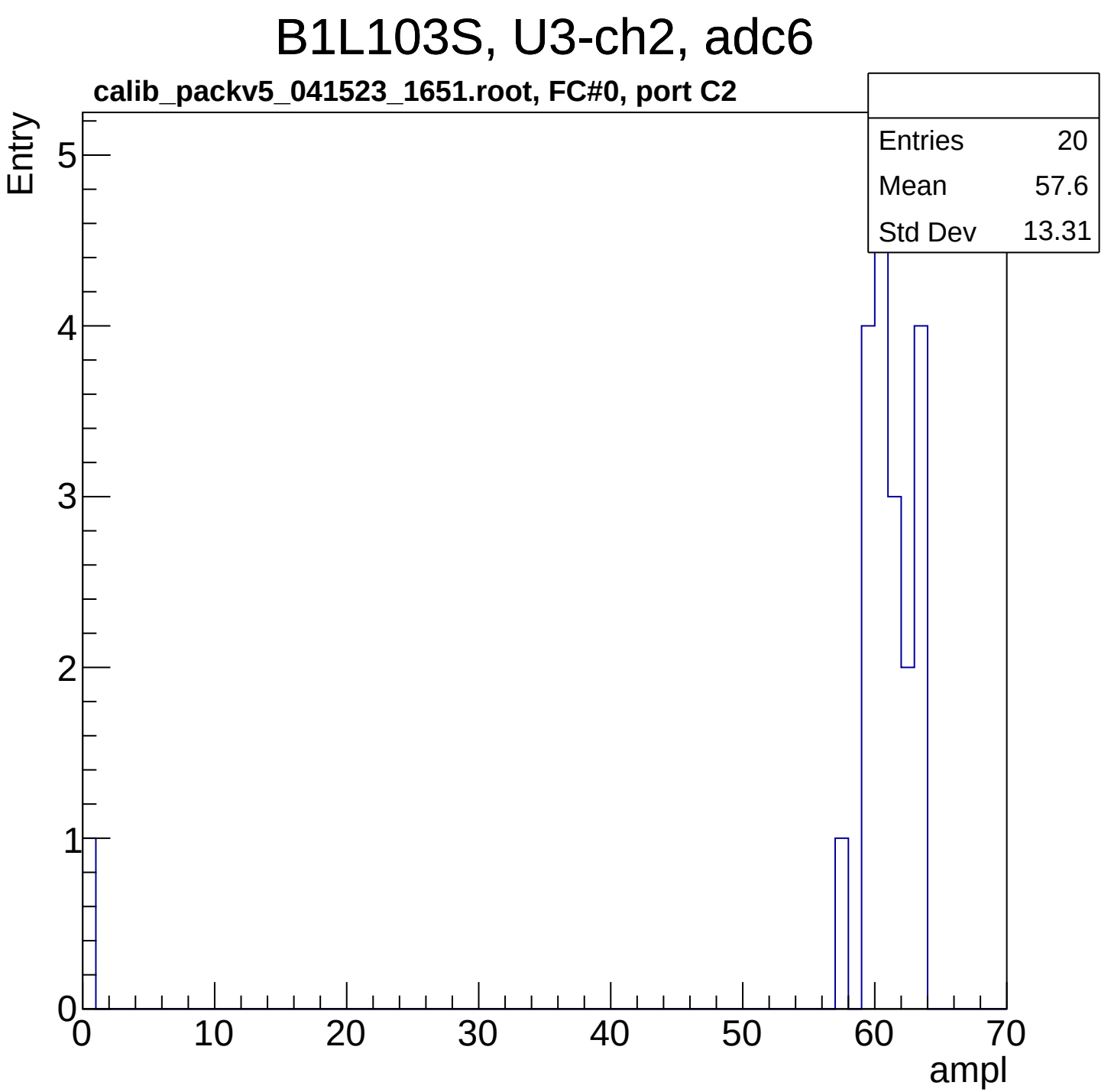
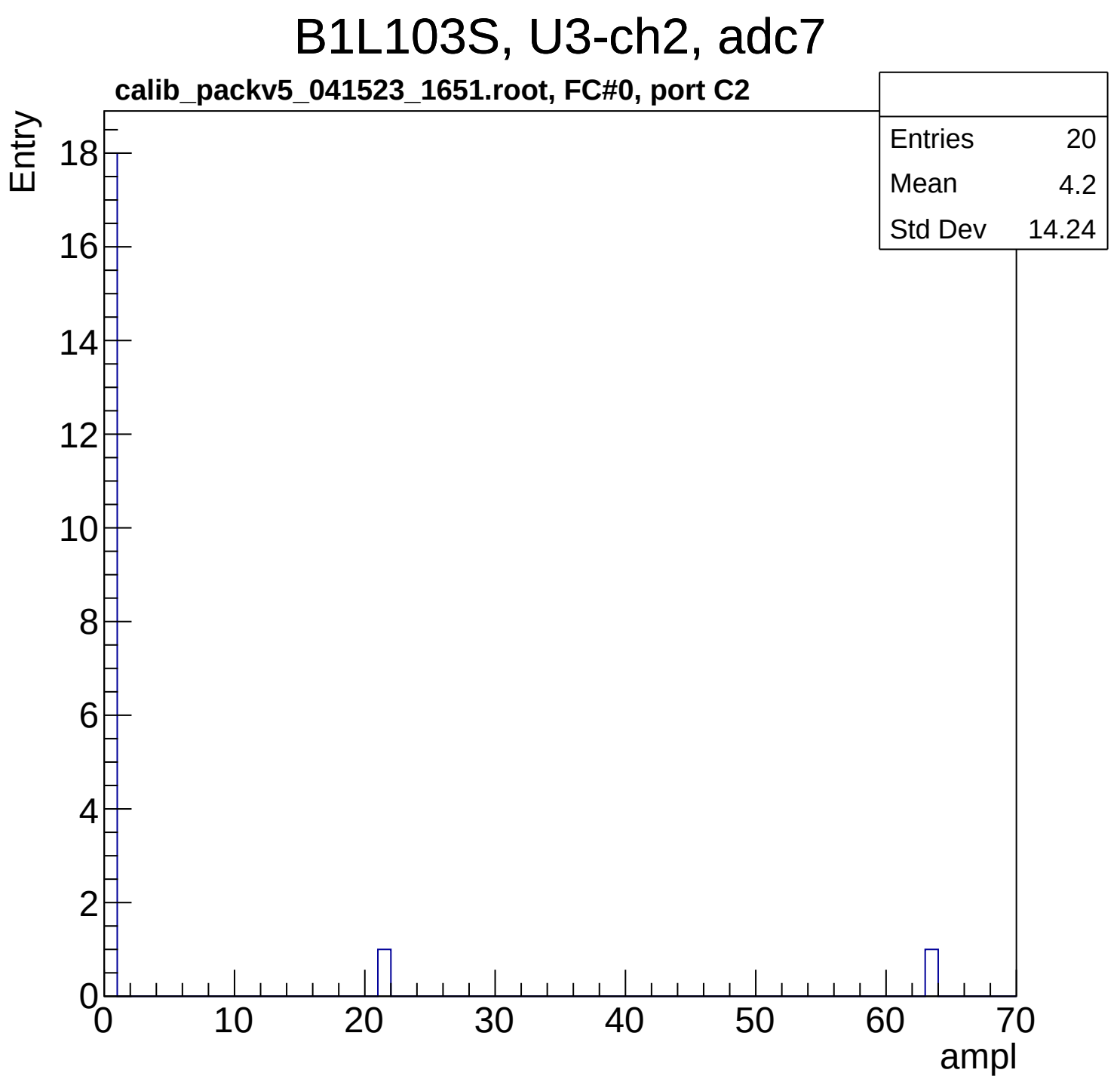
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch2, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 57.6
Std Dev 13.31
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch2, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4.2
Std Dev 14.24
Entry
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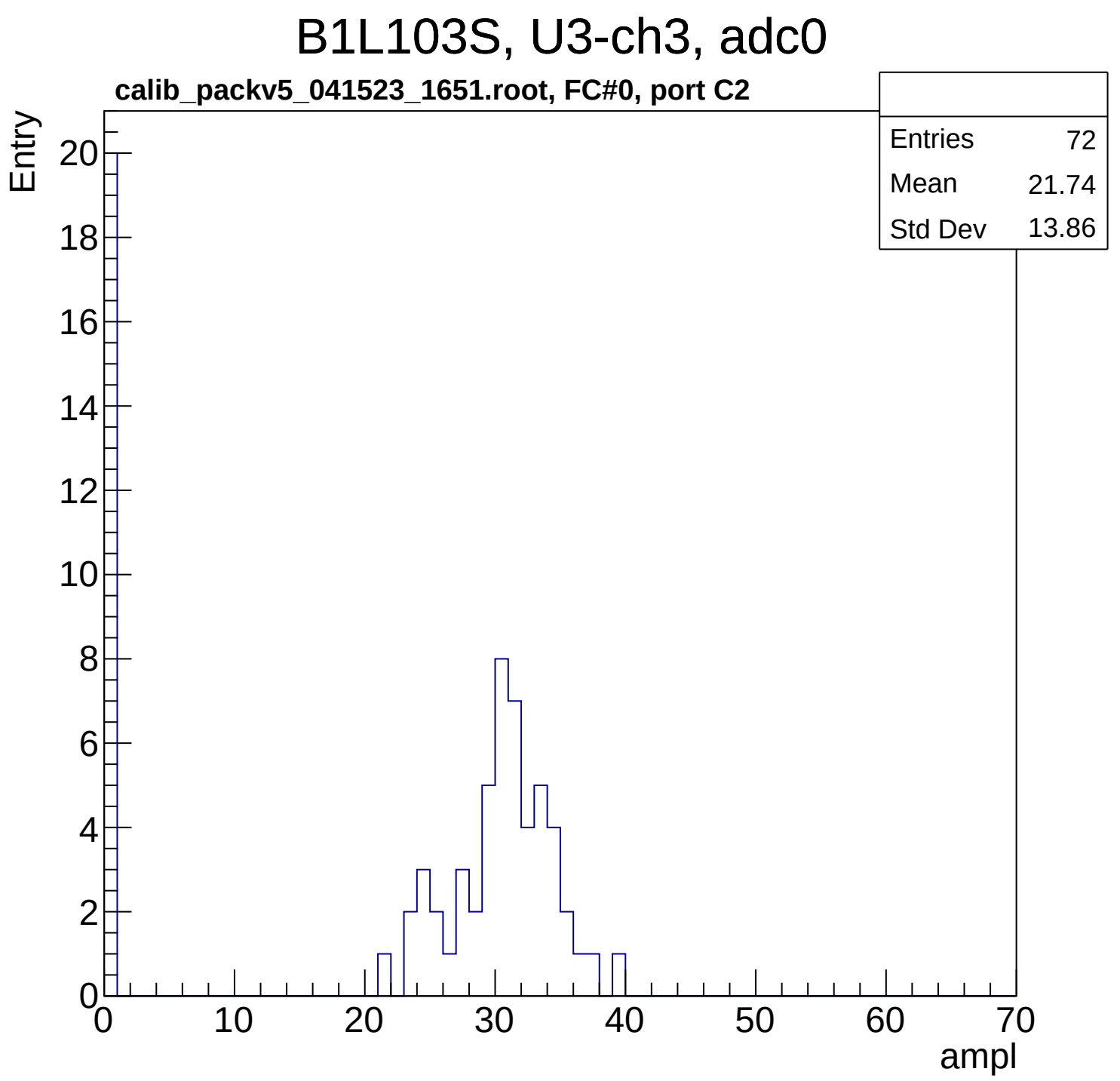
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch3, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 21.74
Std Dev 13.86
Entry
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8
10
12
14
16
18
20
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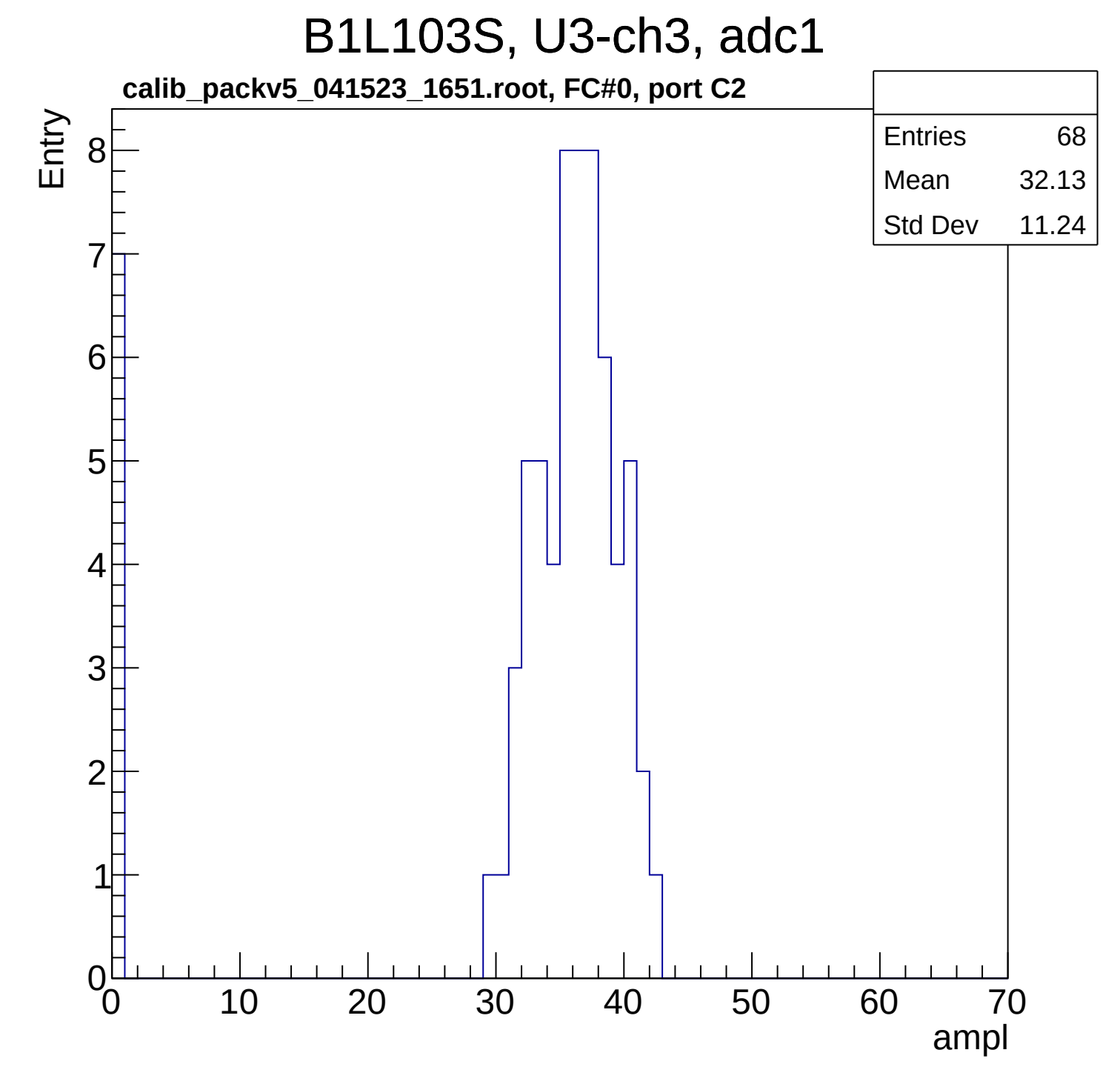
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch3, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 32.13
Std Dev 11.24
Entry
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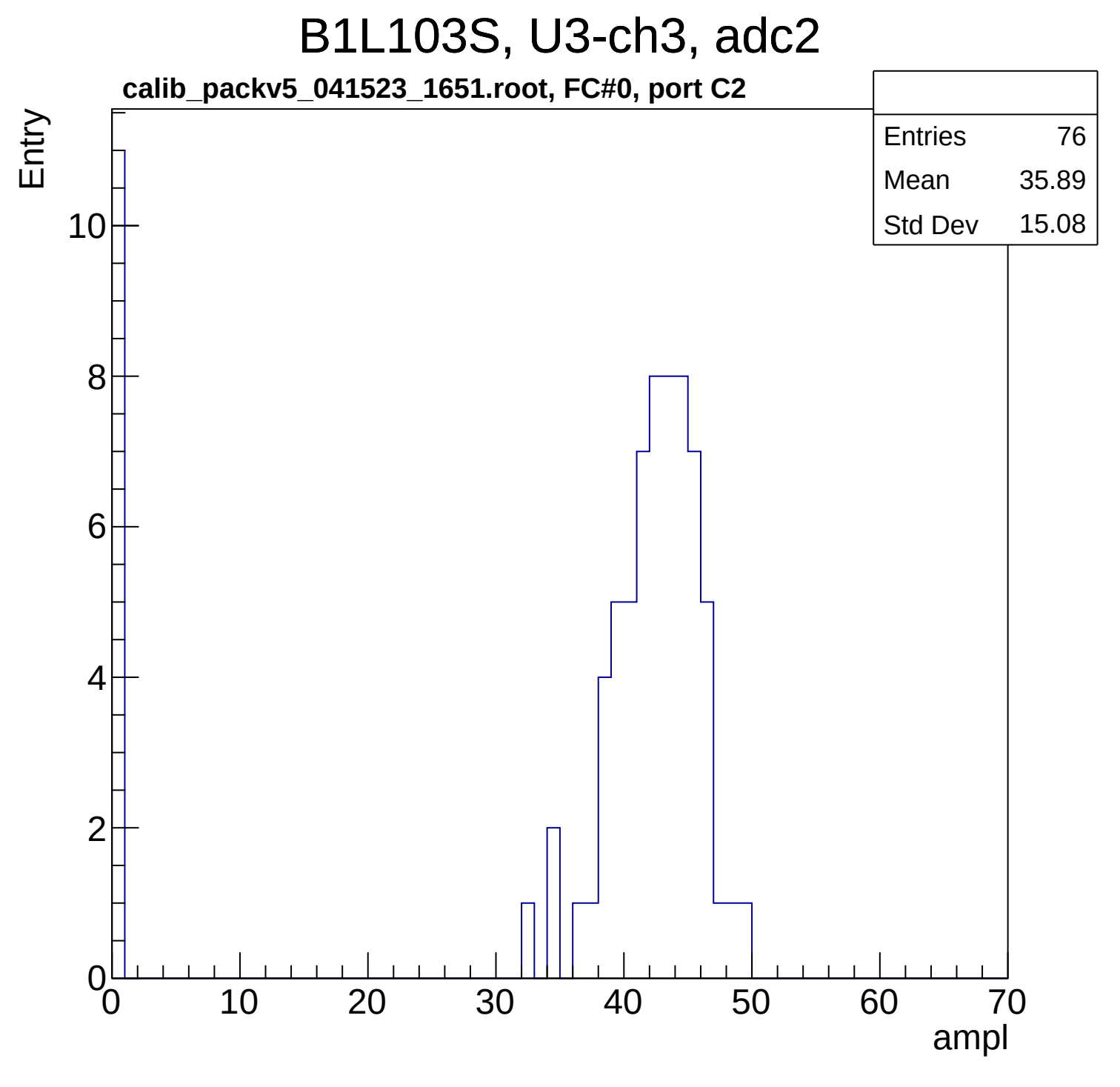
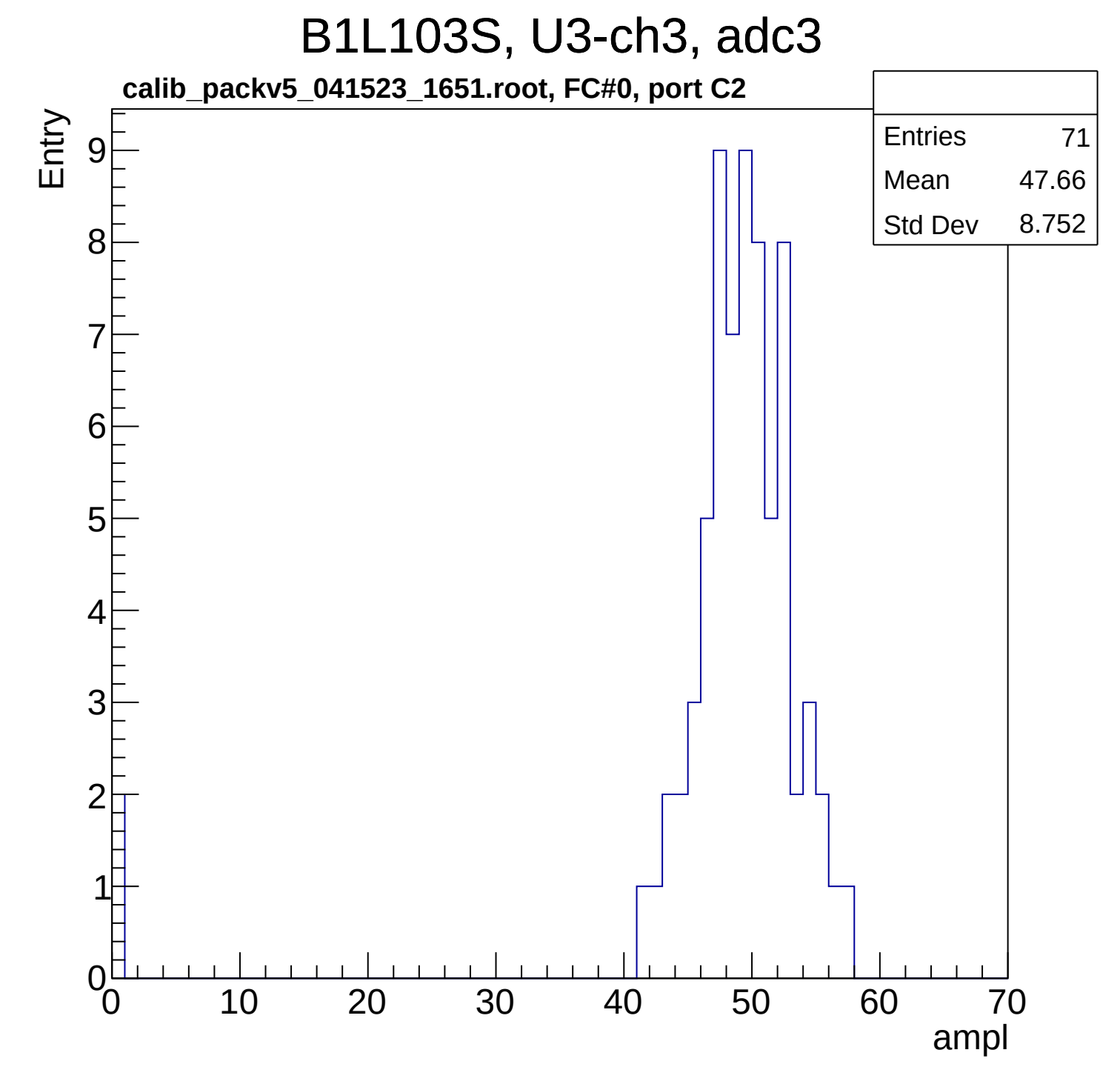
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch3, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 35.89
Std Dev 15.08
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch3, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 47.66
Std Dev 8.752
Entry
ampl
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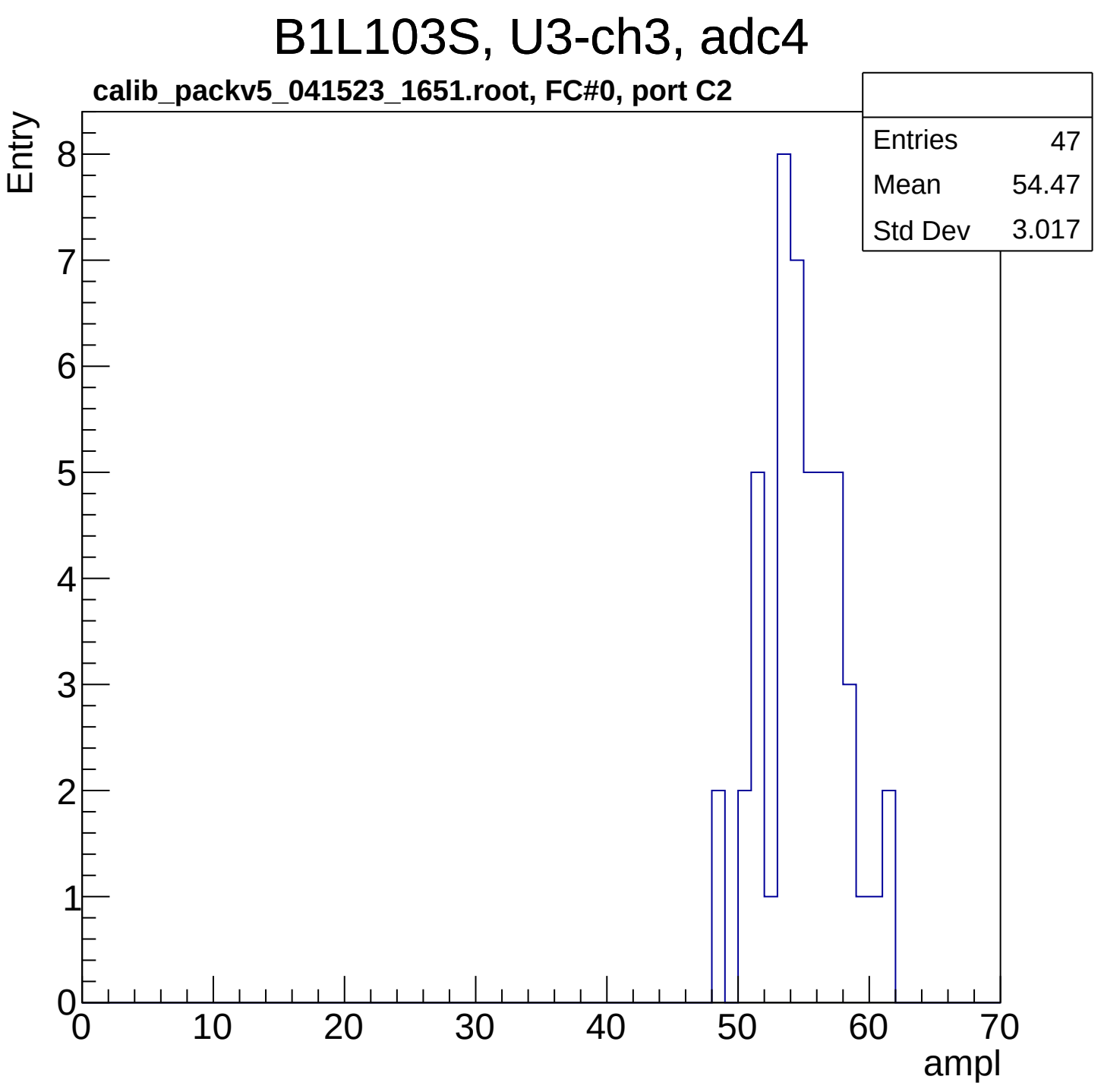
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch3, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 54.47
Std Dev 3.017
Entry
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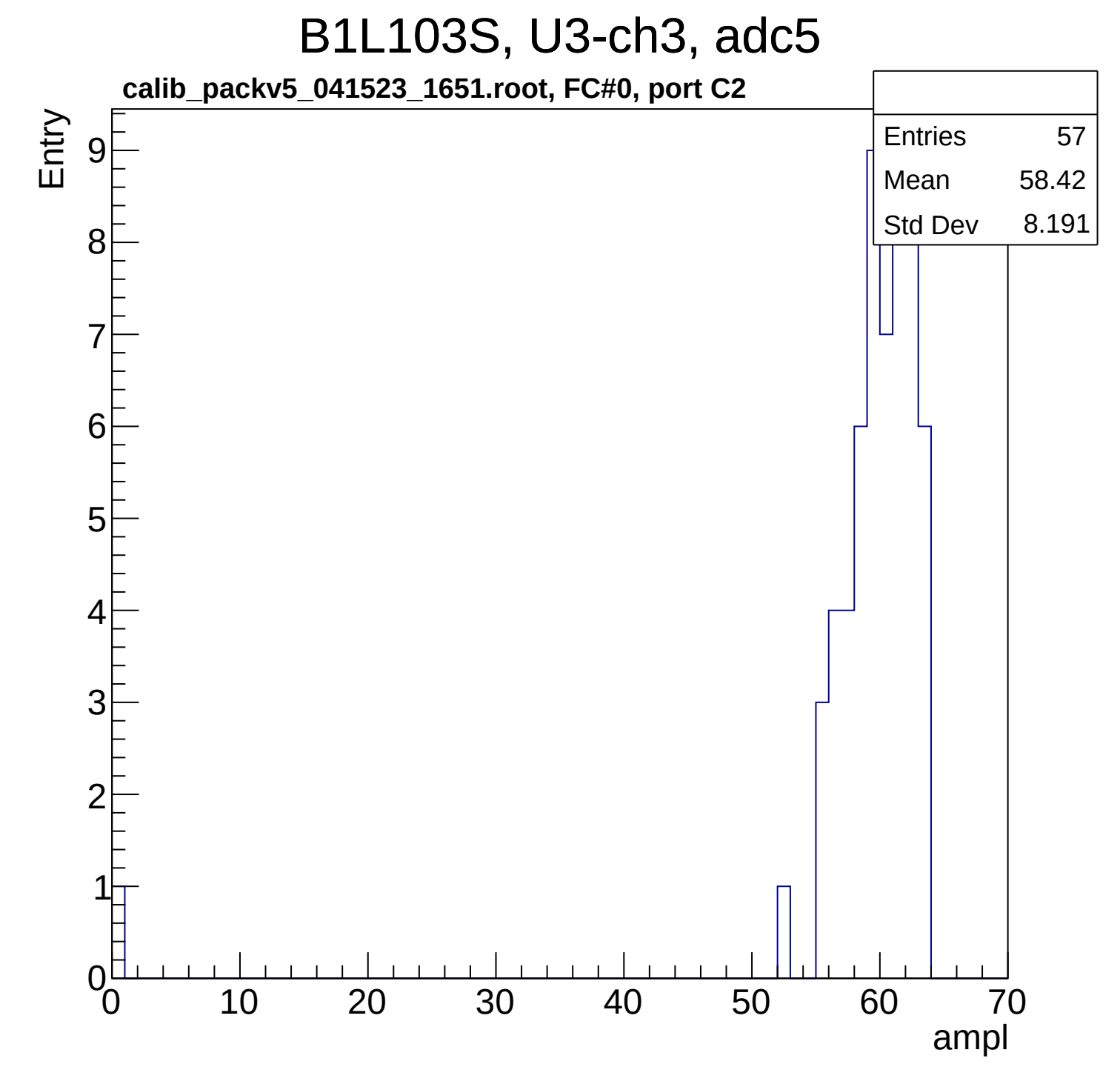
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch3, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 58.42
Std Dev 8.191
Entry
ampl
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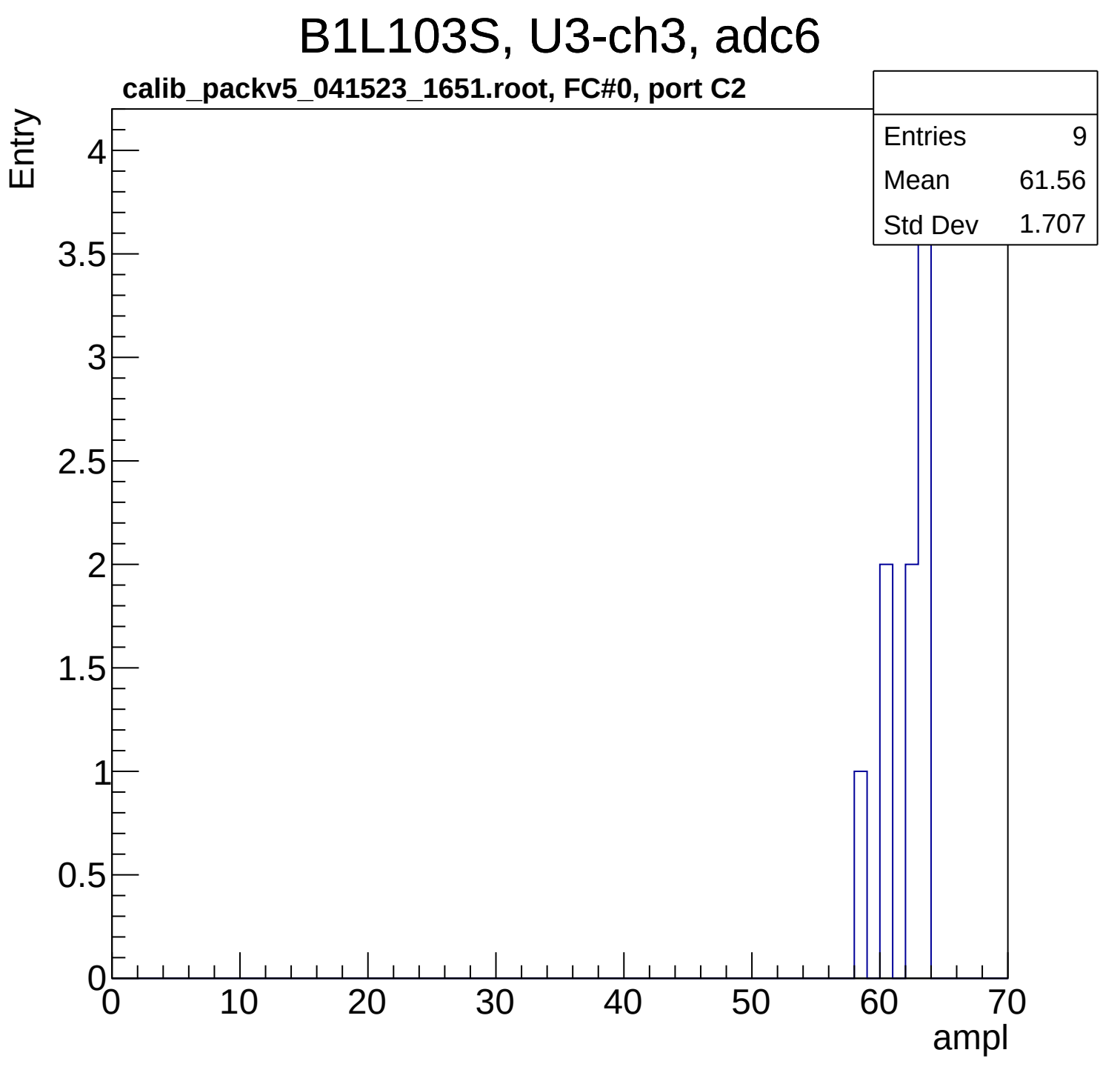
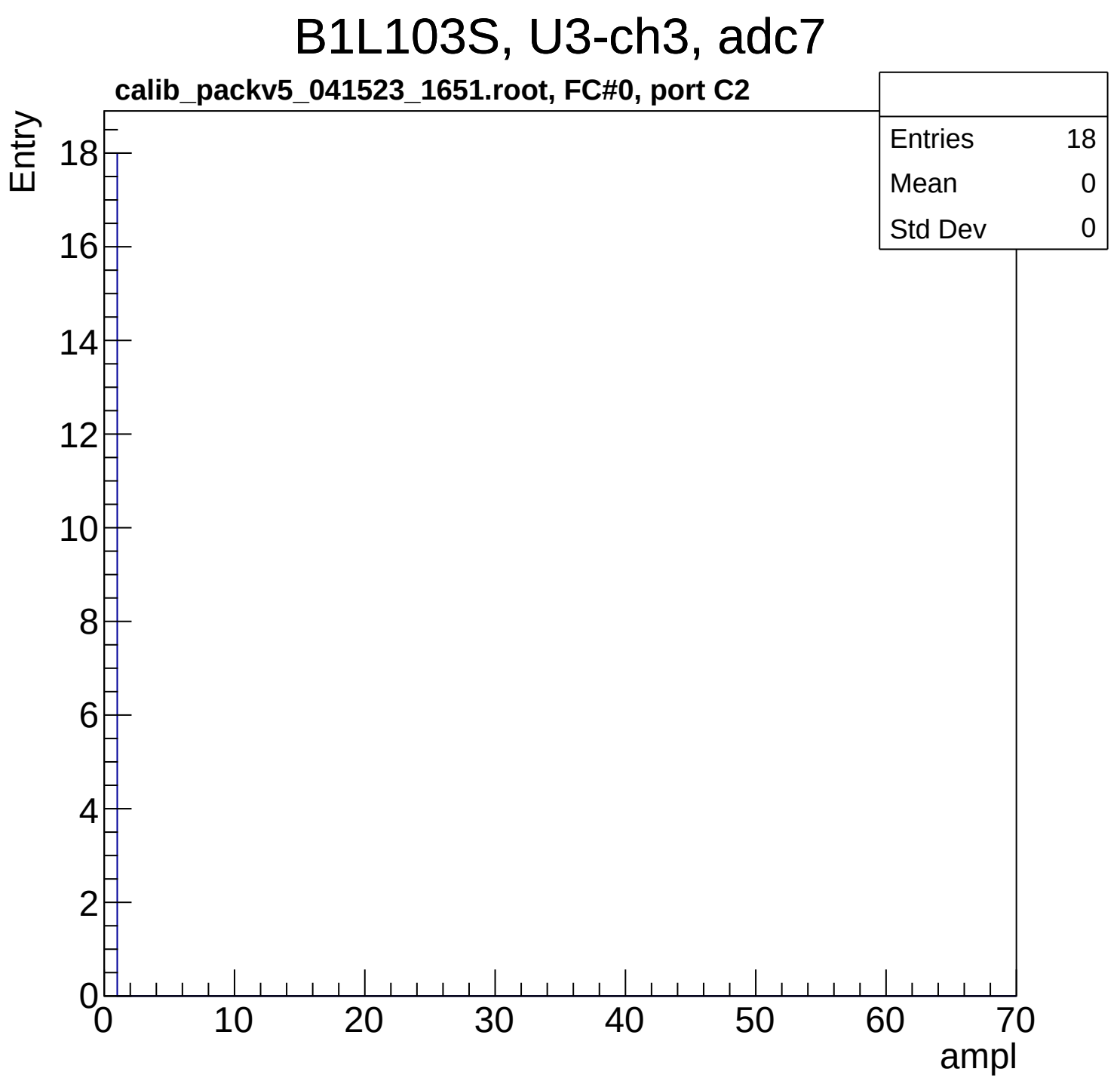
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch3, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 61.56
Std Dev 1.707
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U3-ch3, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
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10
20
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50
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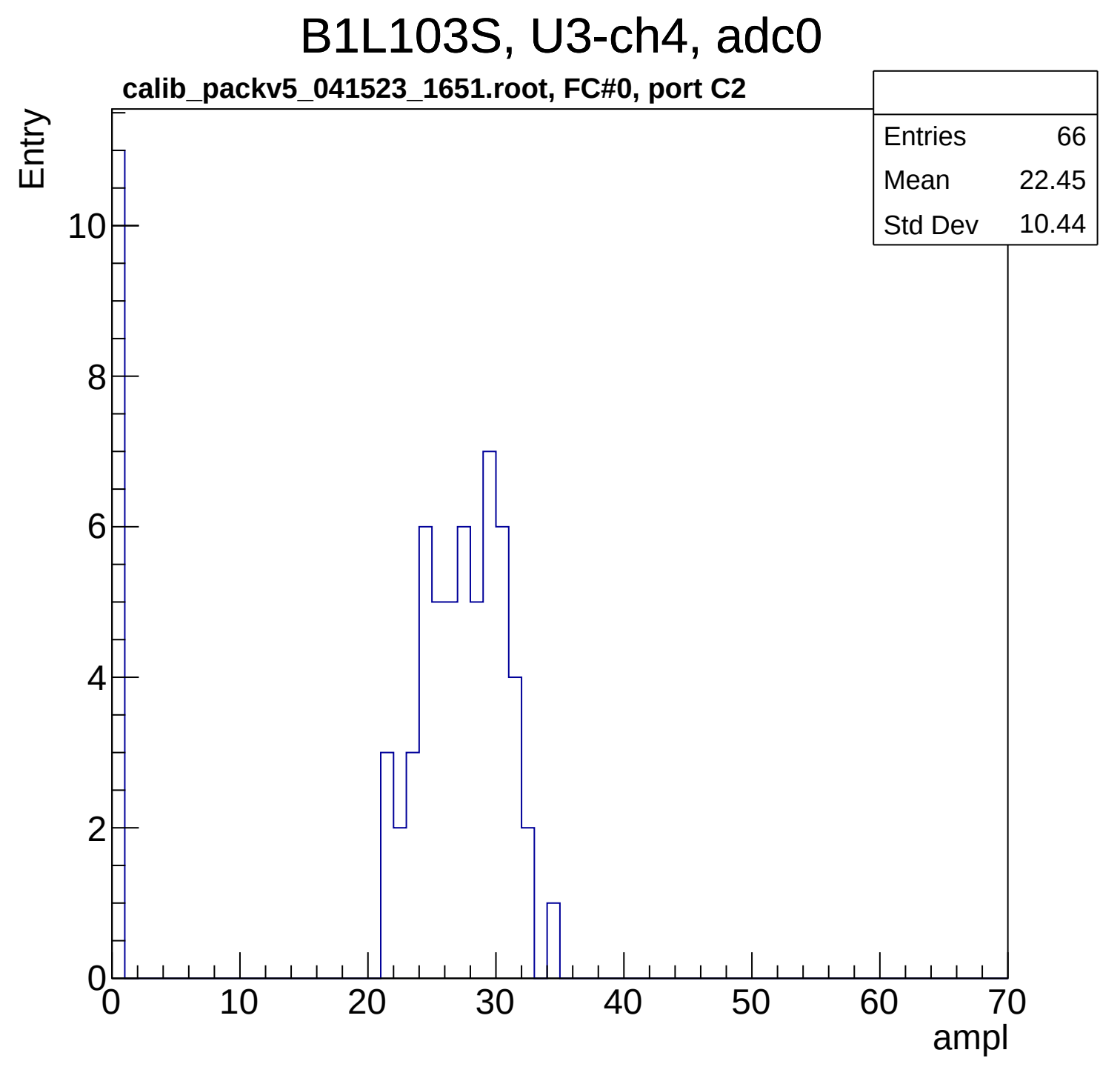
70
ampl


B1L103S, U3-ch4, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 22.45
Std Dev 10.44
Entry
0
2
4
6
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10
0
10
20
30
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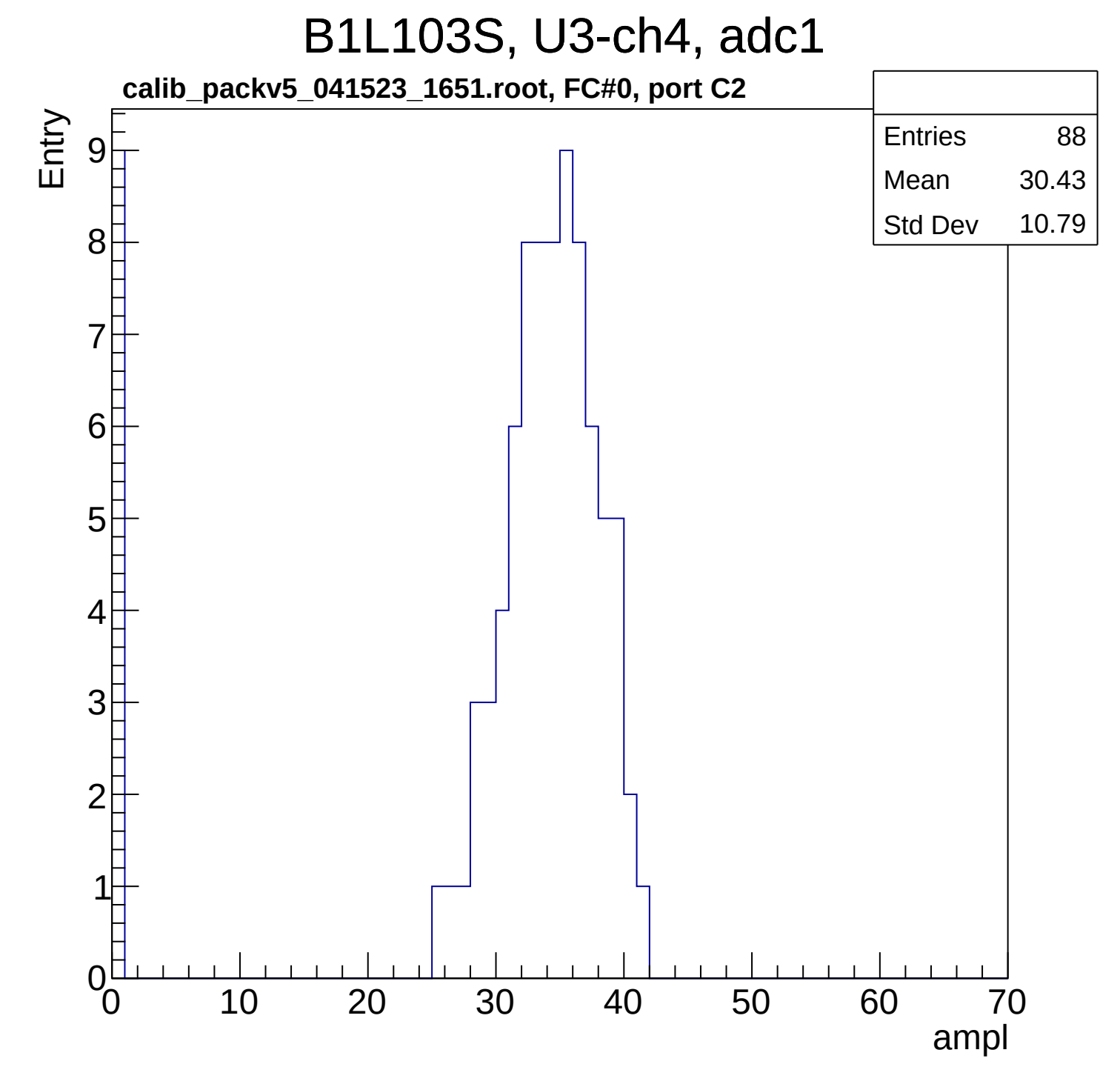
50
60
70
ampl


B1L103S, U3-ch4, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 30.43
Std Dev 10.79
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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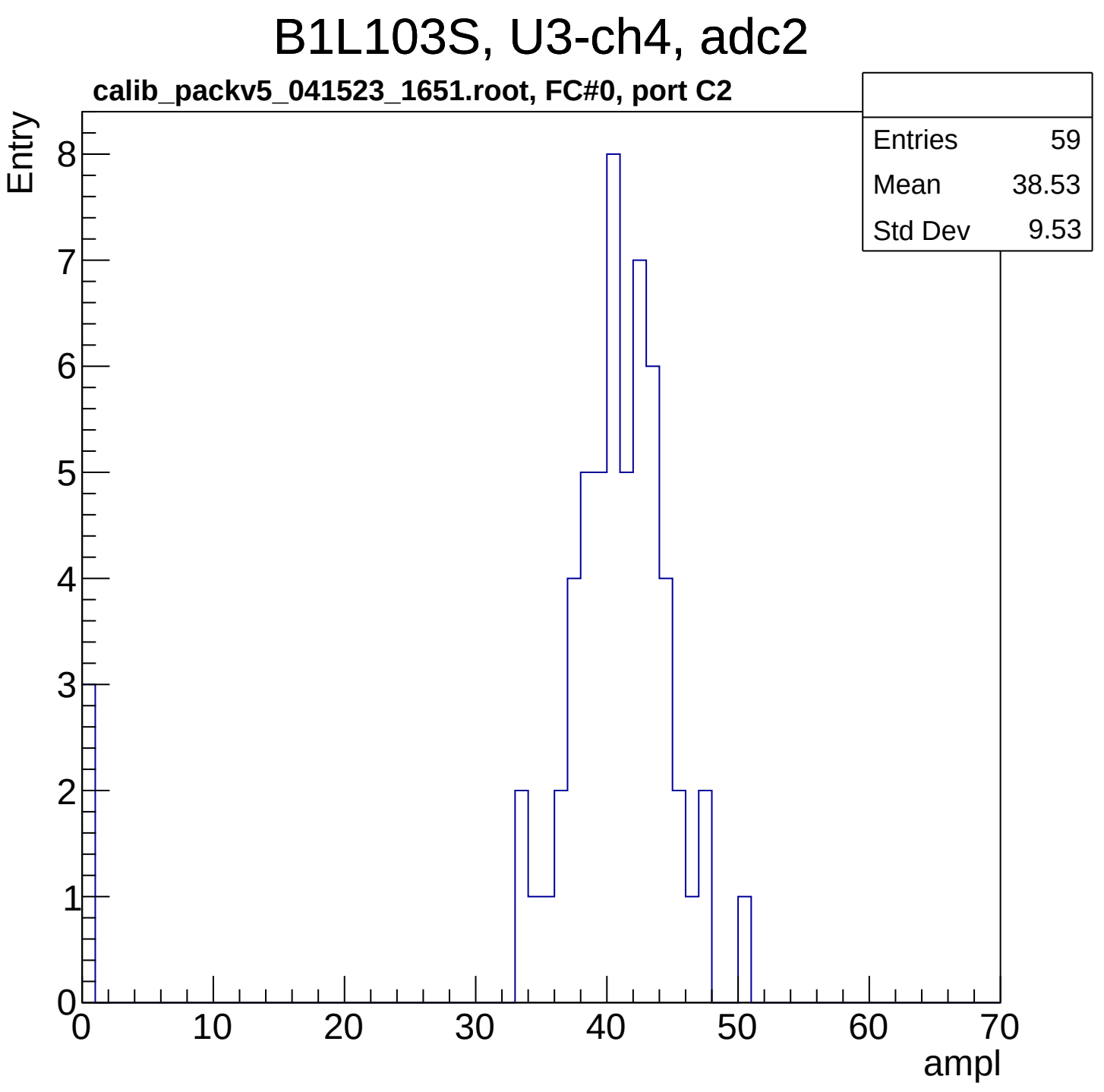
B1L103S, U3-ch4, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 38.53
Std Dev 9.53
Entry
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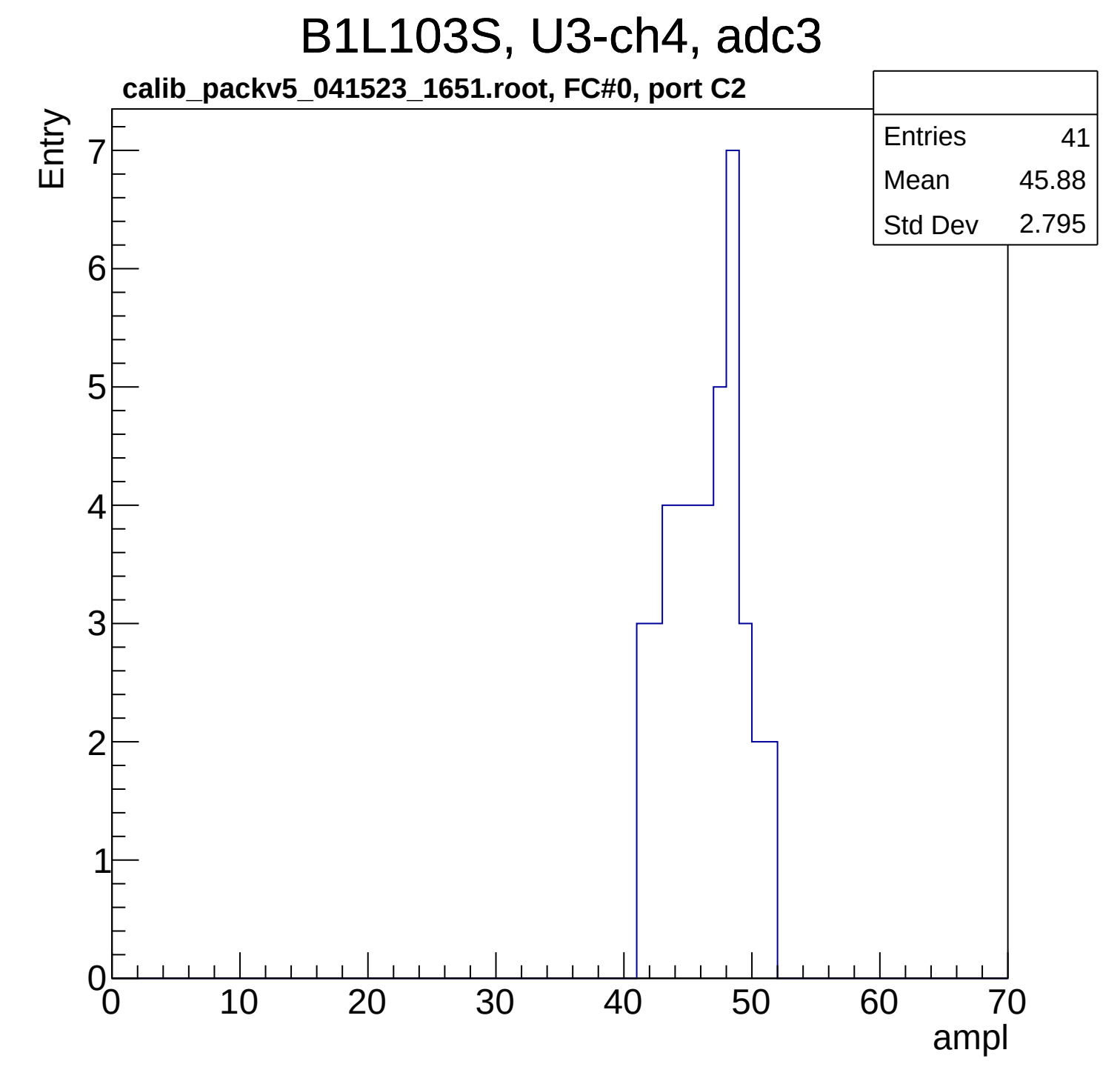
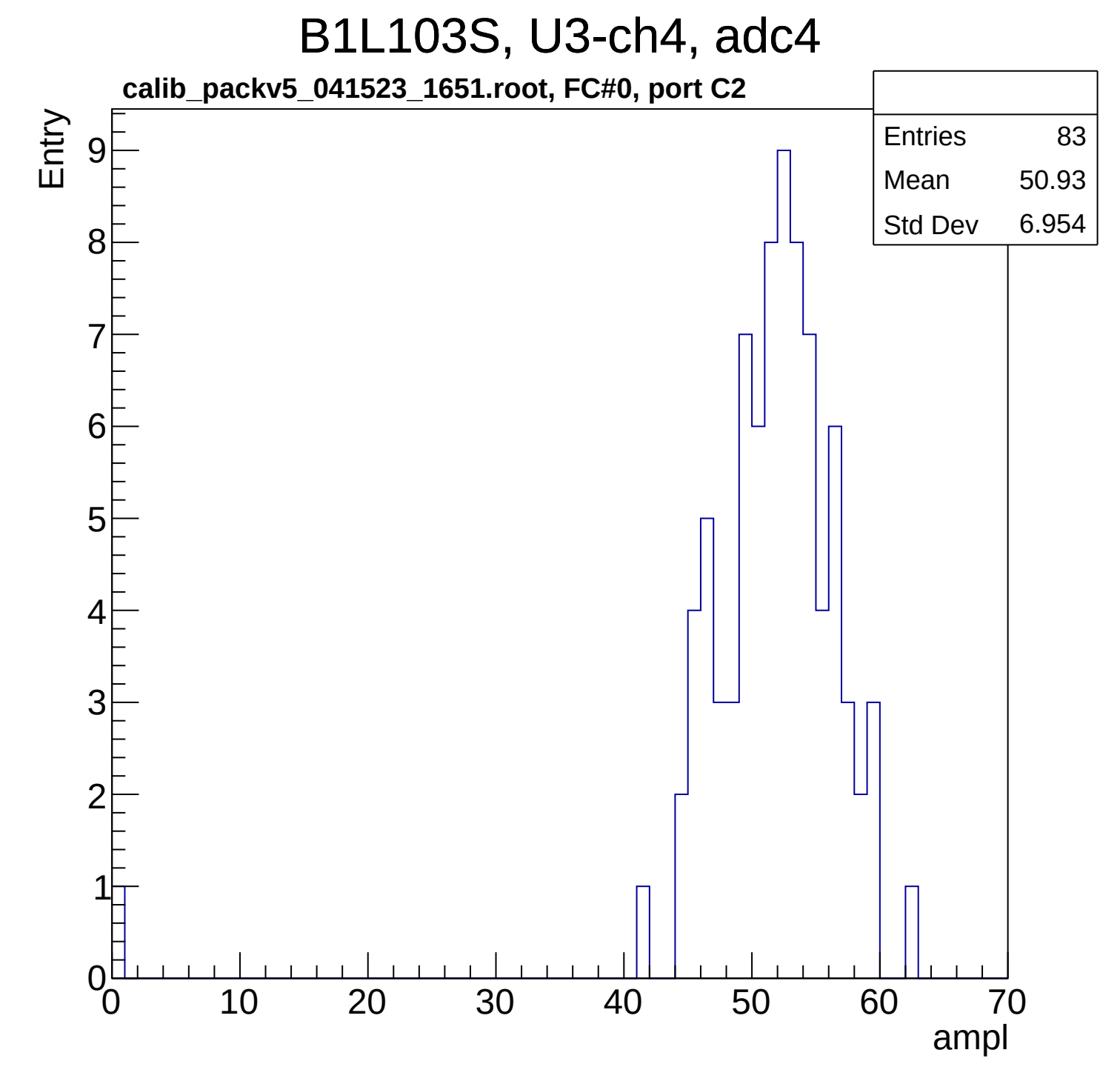
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch4, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 45.88
Std Dev 2.795
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch4, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 50.93
Std Dev 6.954
Entry
ampl
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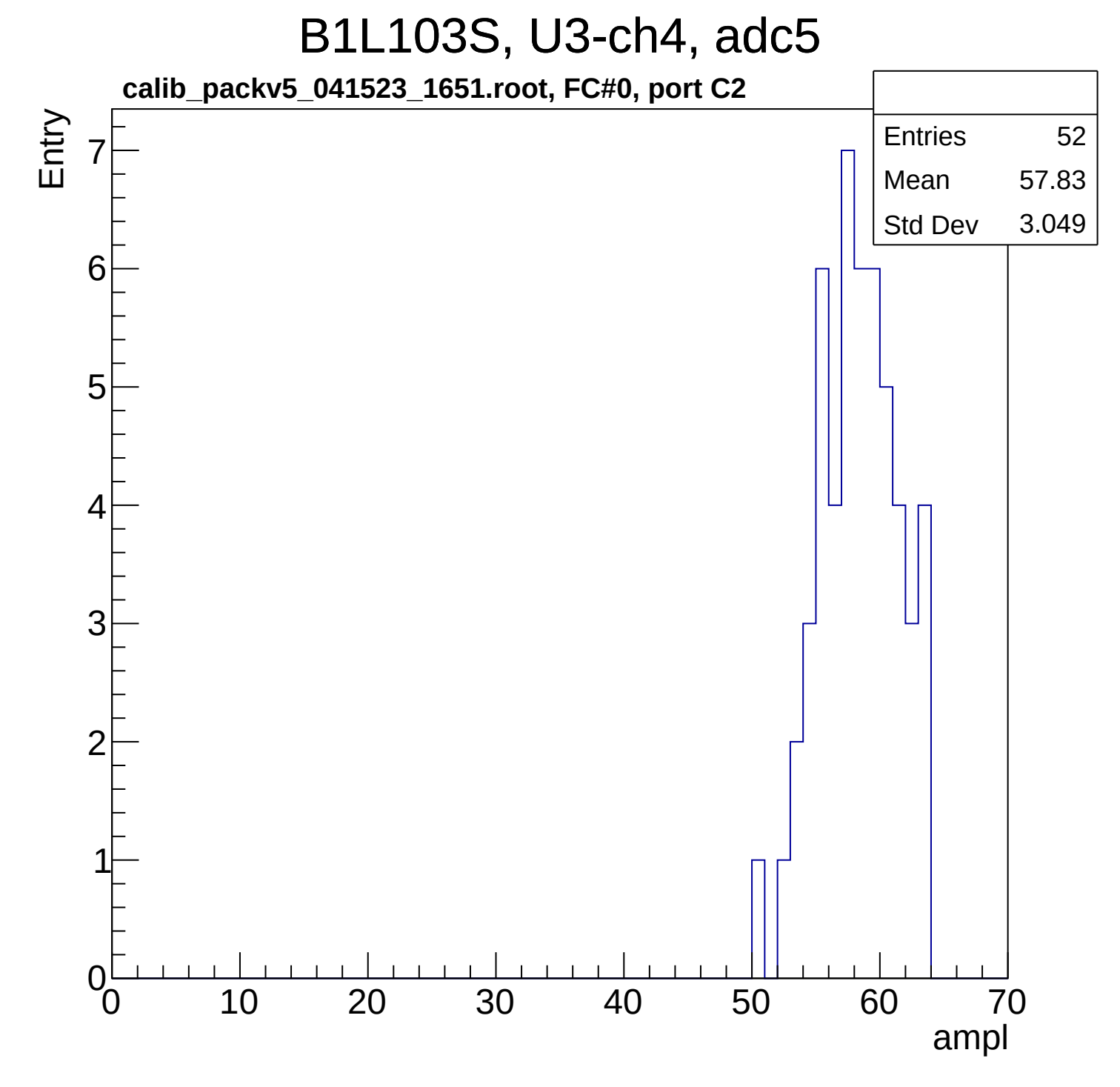
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch4, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 57.83
Std Dev 3.049
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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40
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60
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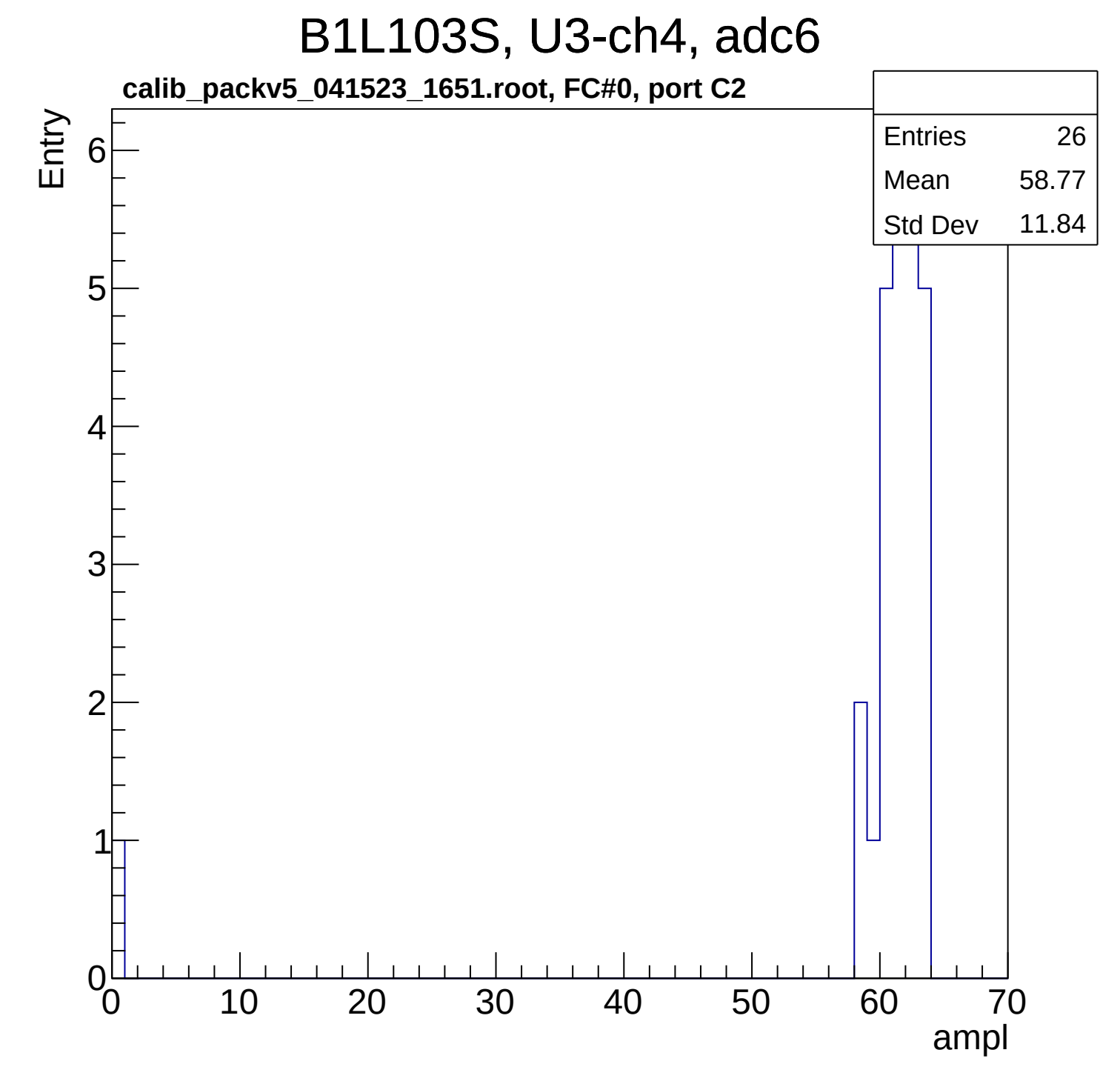
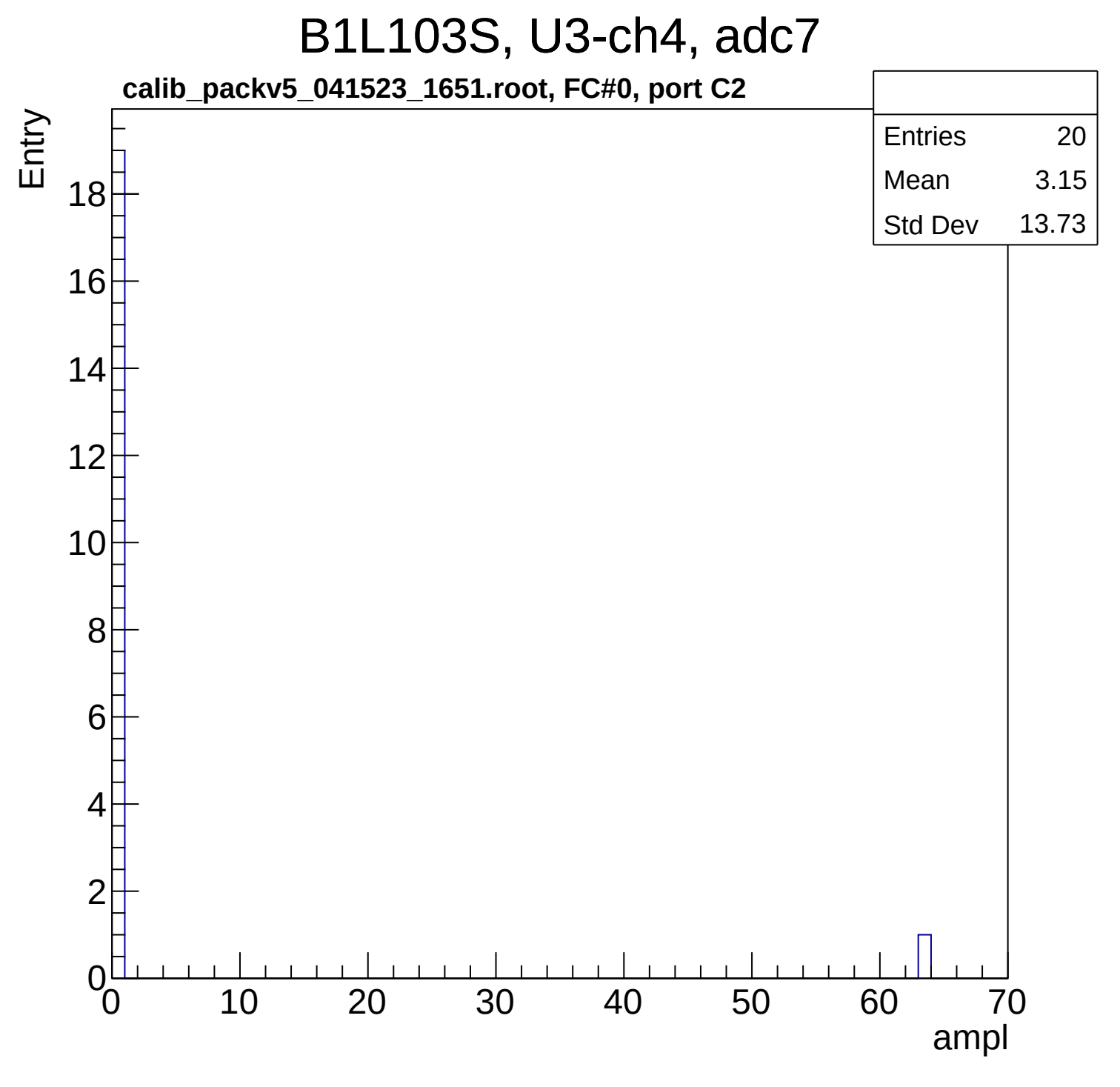
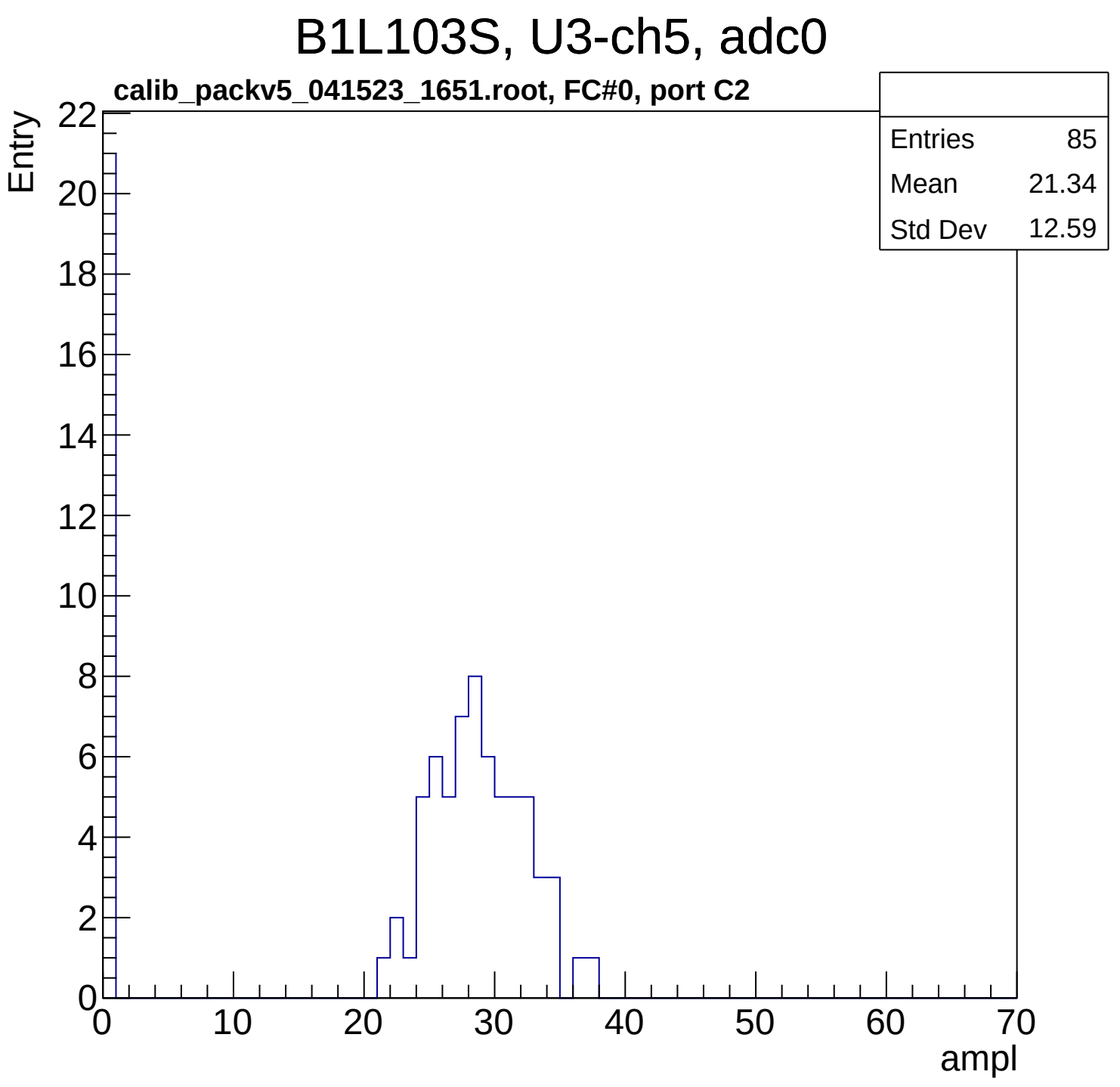
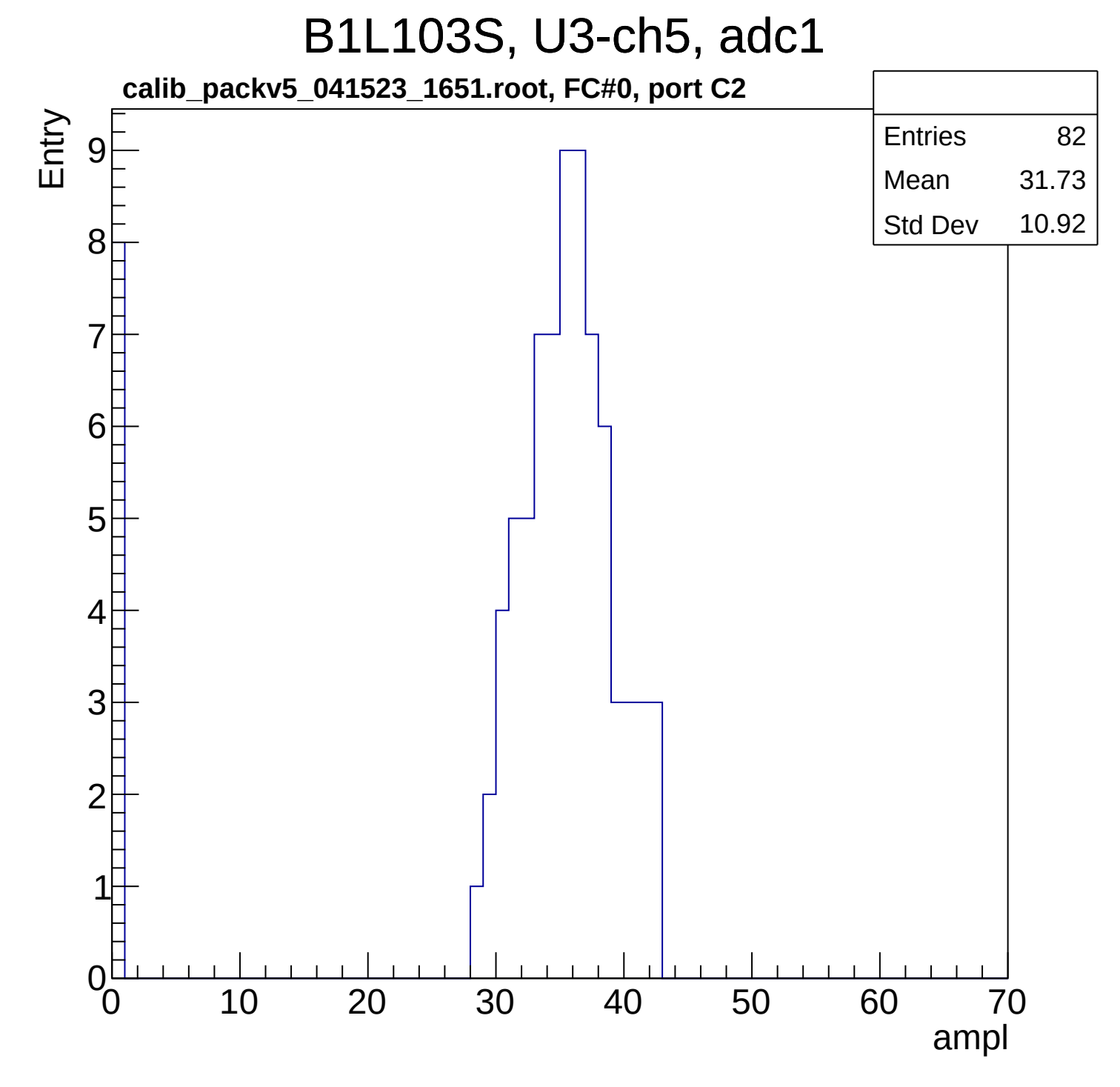

B1L103S, U3-ch4, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 58.77
Std Dev 11.84
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U3-ch4, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch5, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 21.34
Std Dev 12.59
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70


B1L103S, U3-ch5, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 31.73
Std Dev 10.92
Entry
ampl
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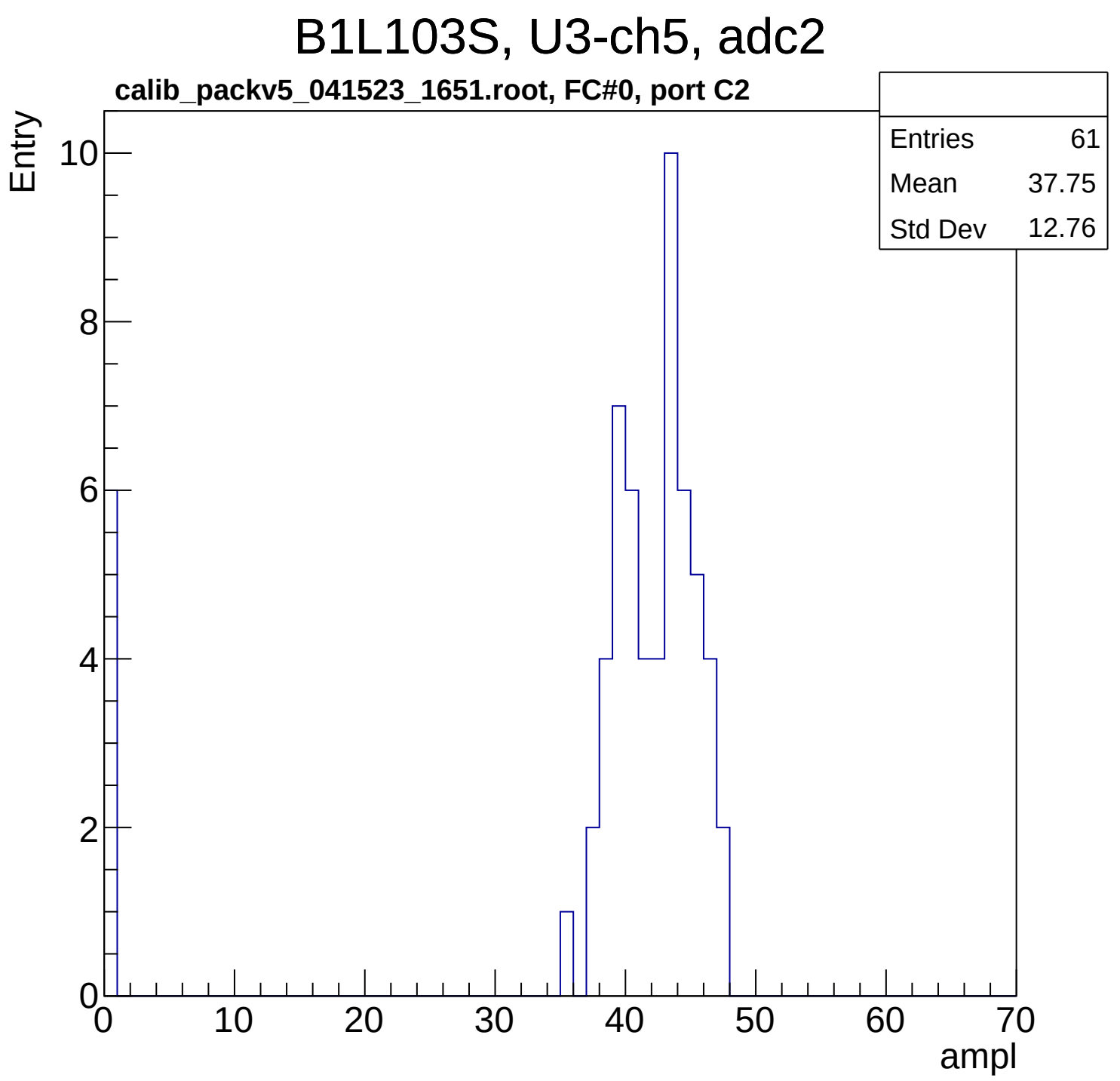
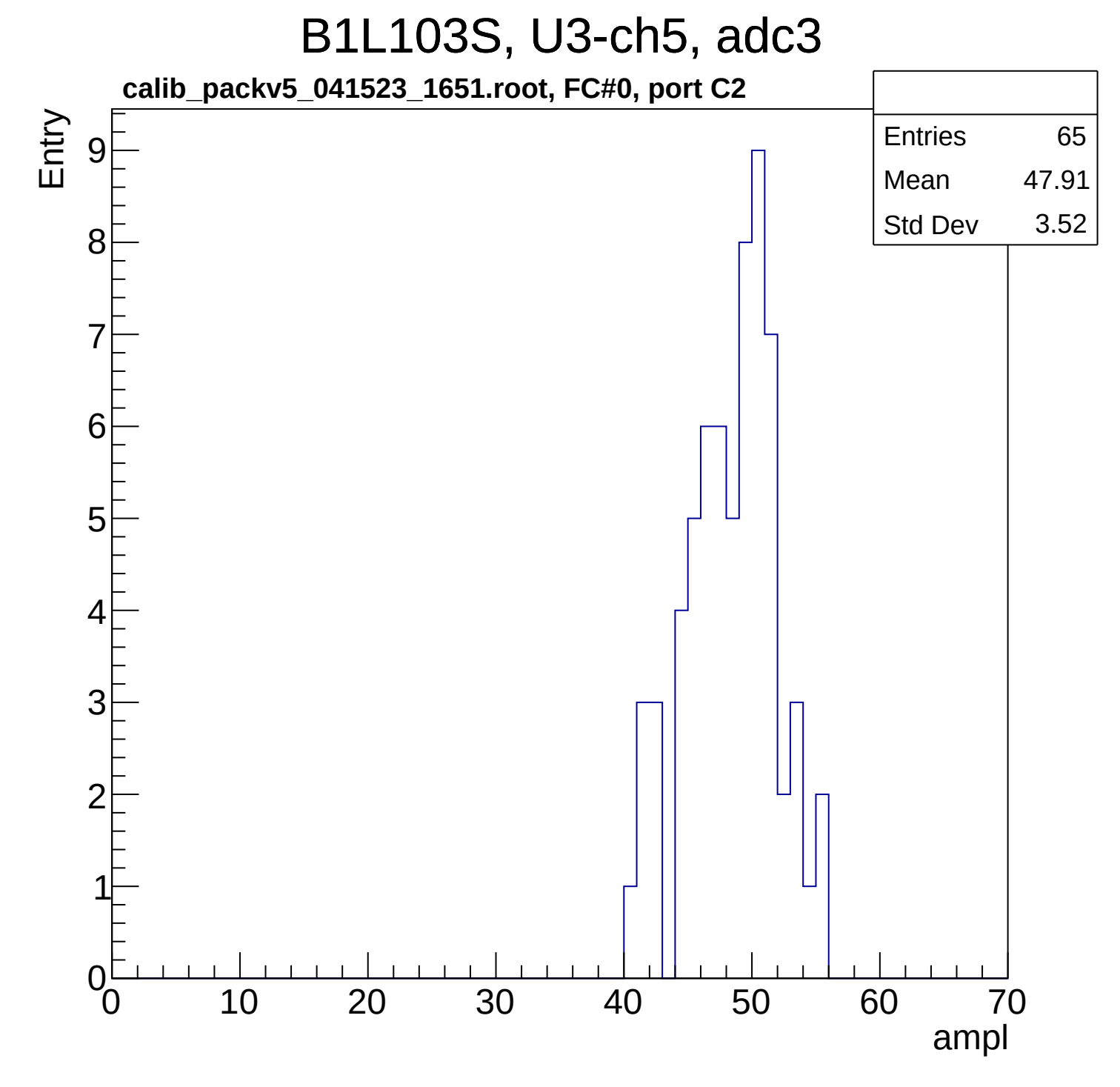
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch5, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 37.75
Std Dev 12.76
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U3-ch5, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 47.91
Std Dev 3.52
Entry
ampl
0
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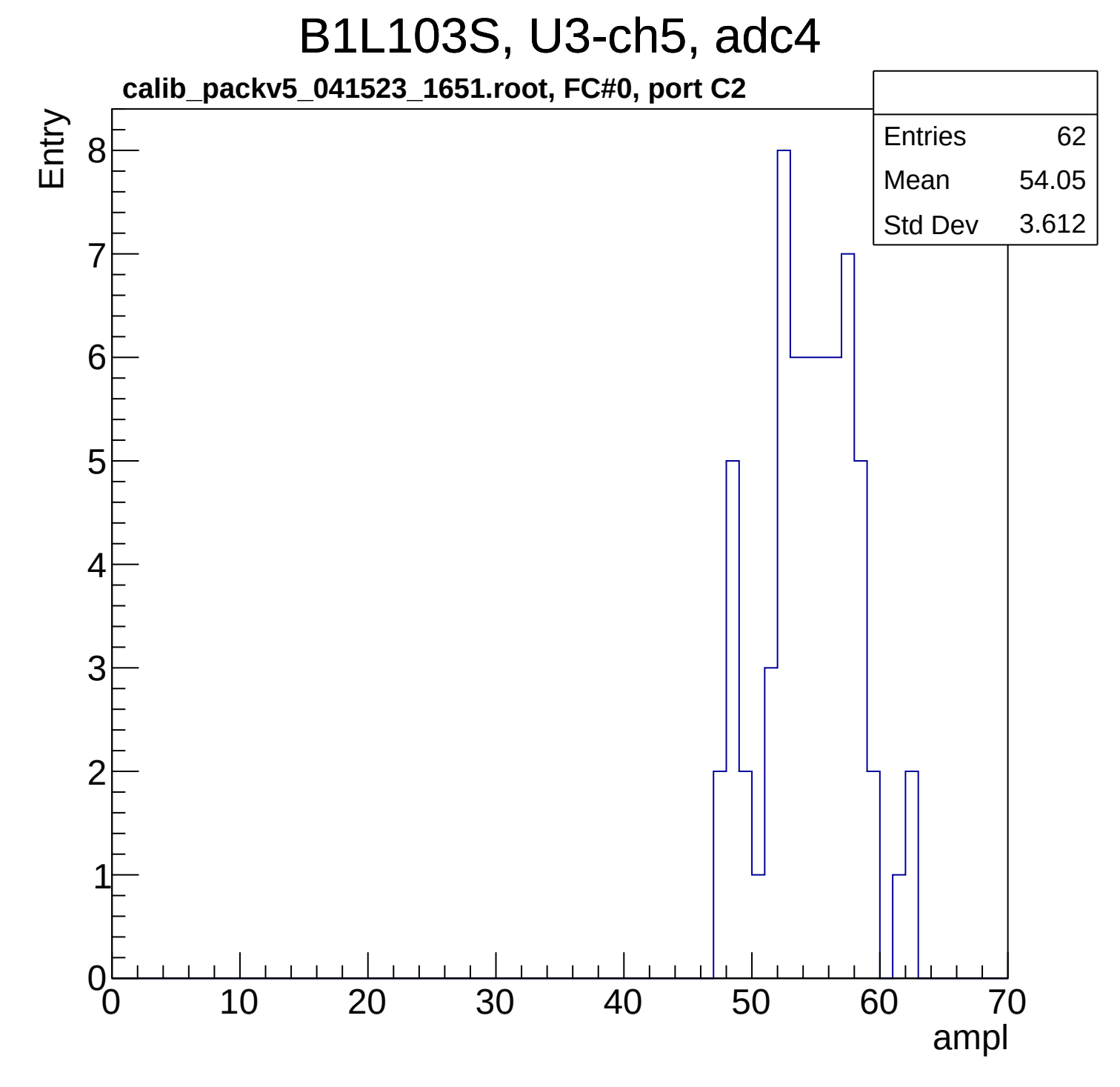
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch5, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 54.05
Std Dev 3.612
Entry
ampl
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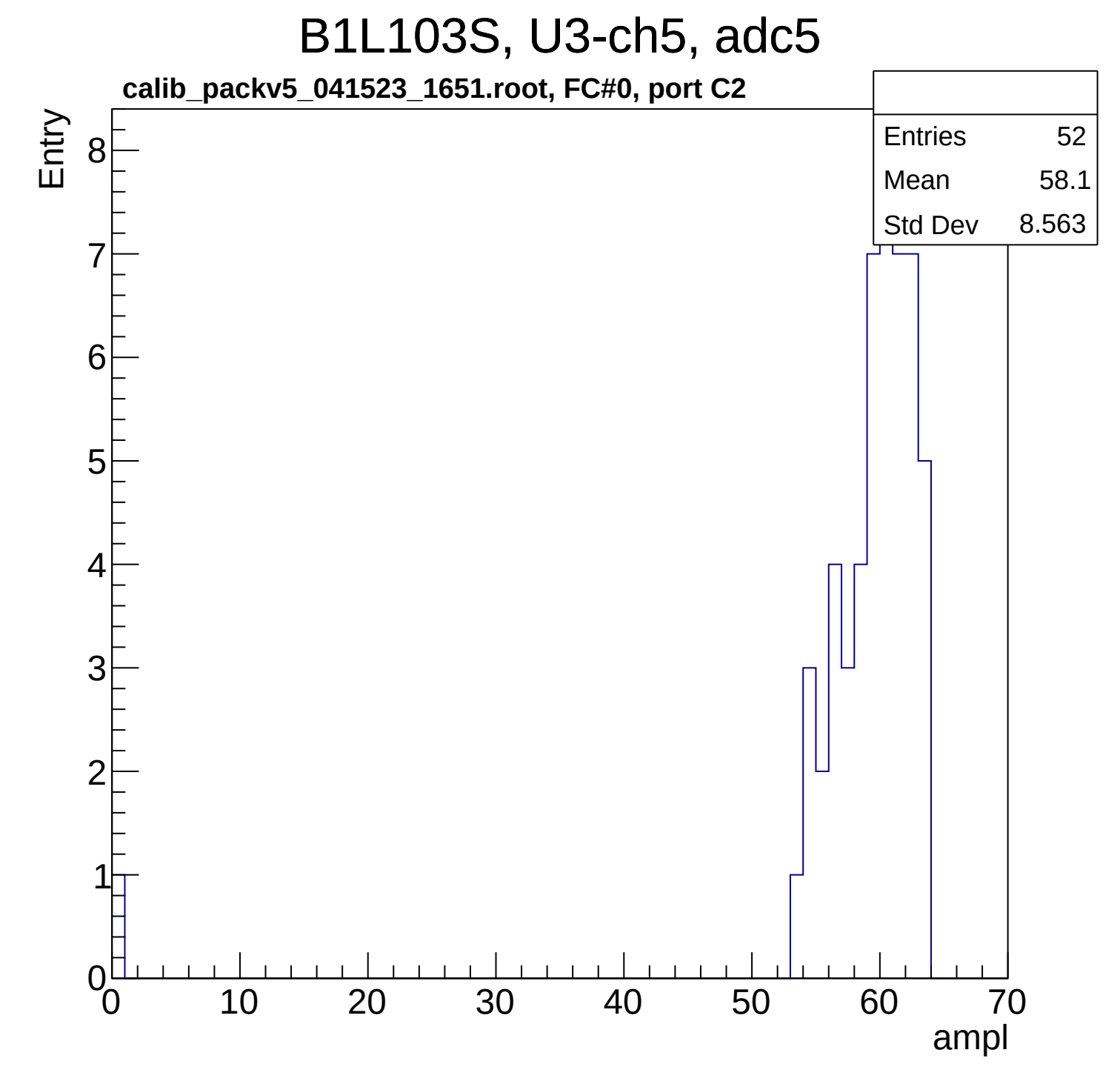
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch5, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 58.1
Std Dev 8.563
Entry
ampl
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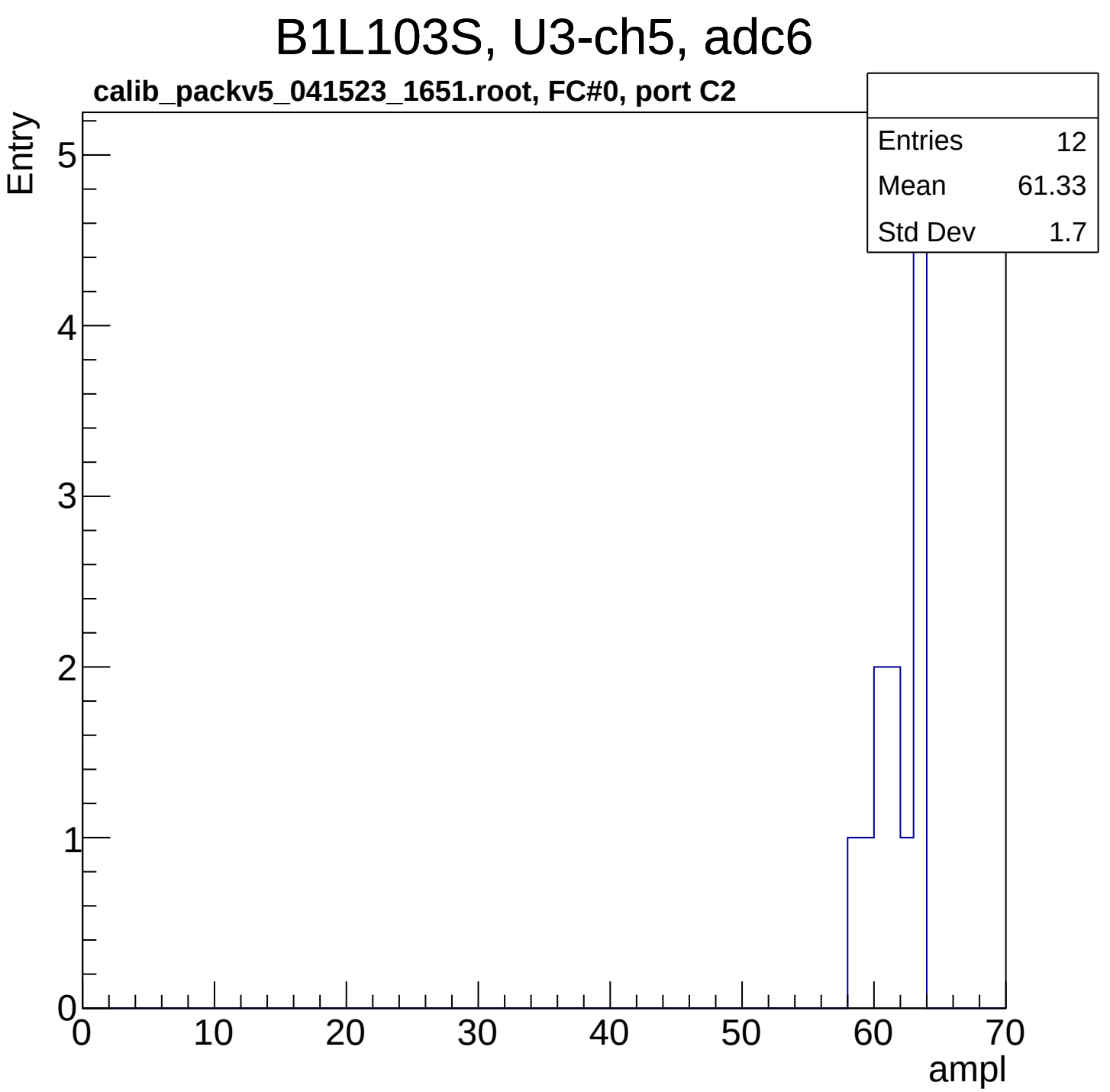
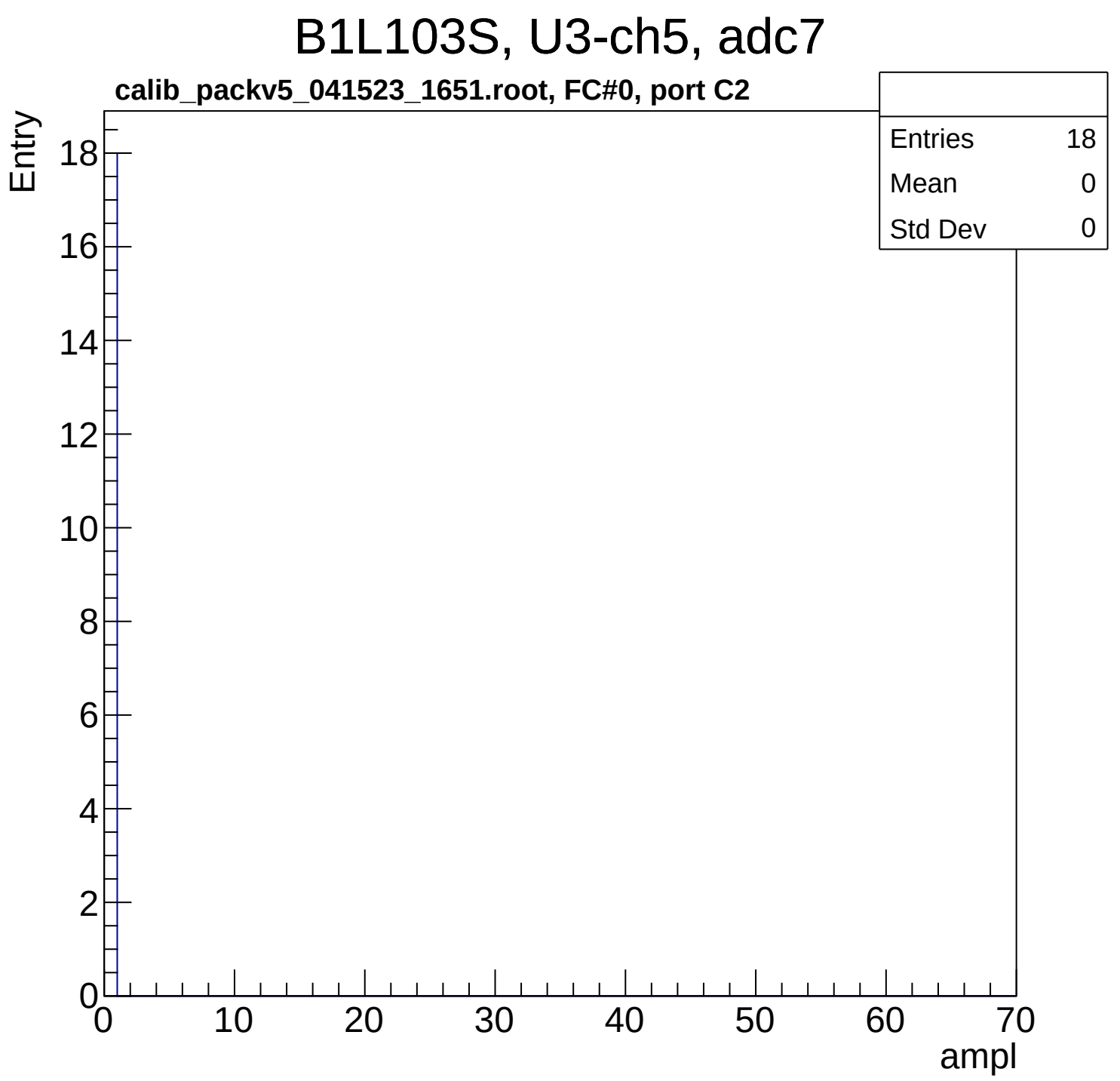
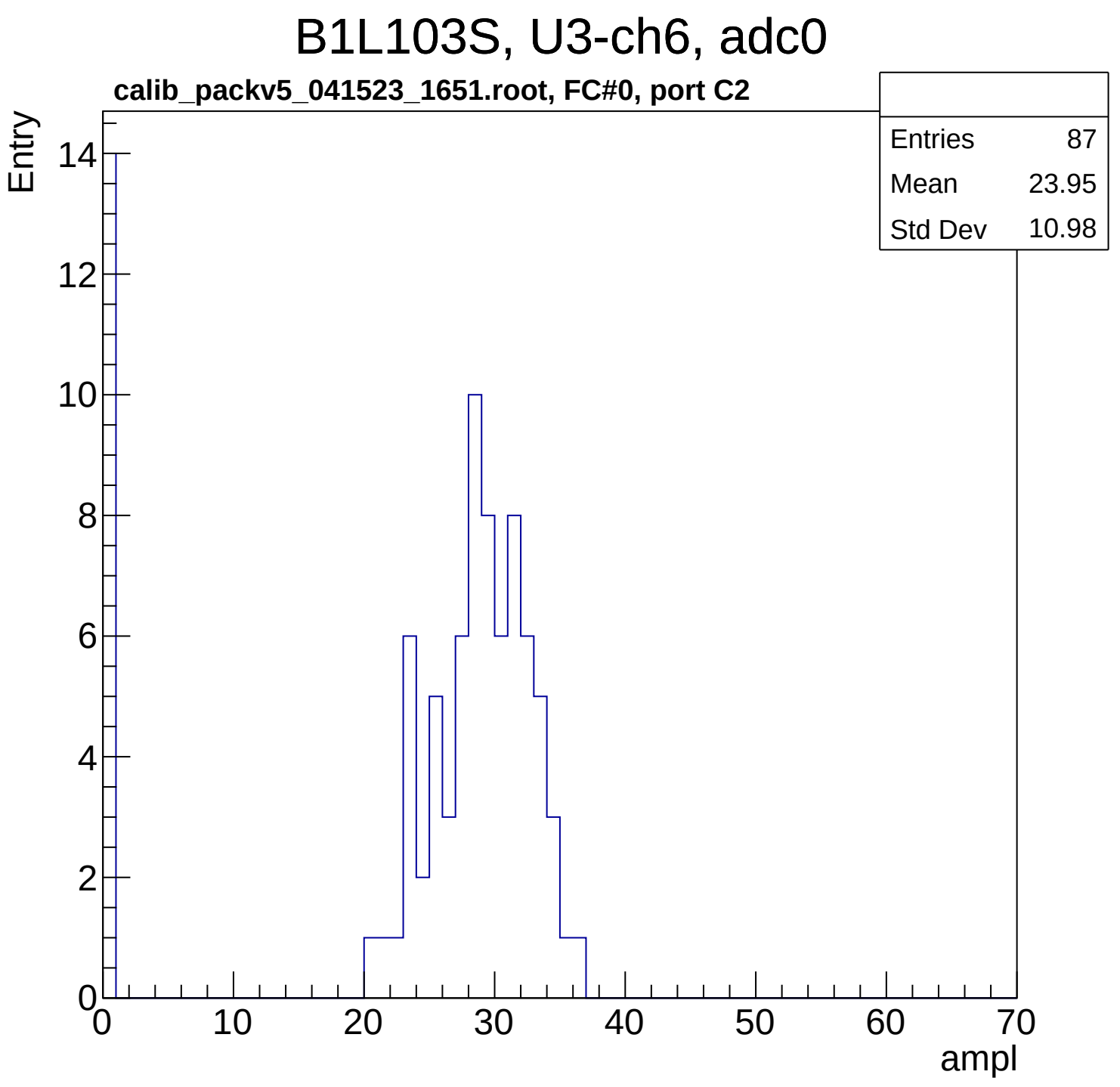
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch5, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.33
Std Dev 1.7
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U3-ch5, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch6, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 23.95
Std Dev 10.98
Entry
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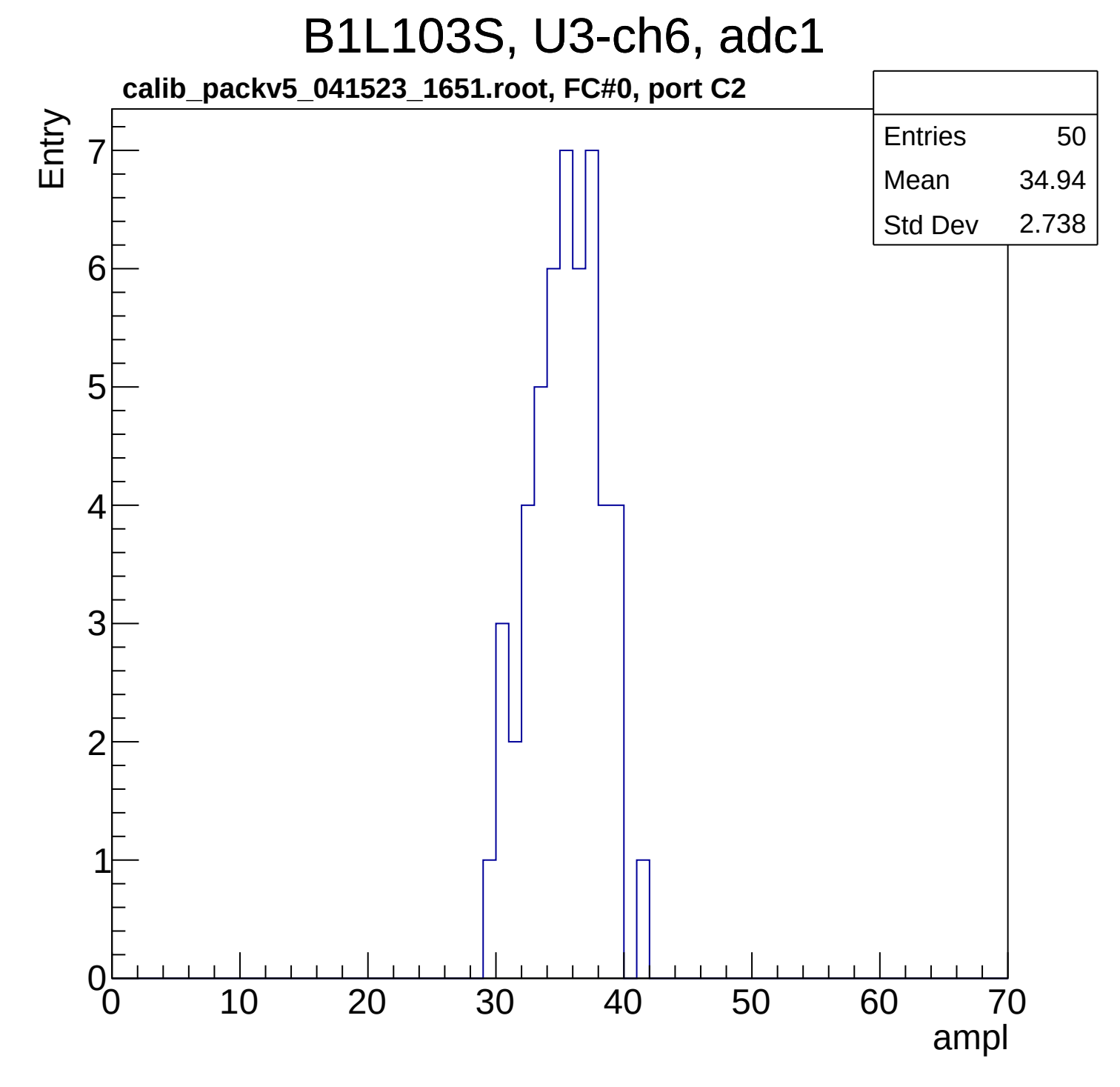
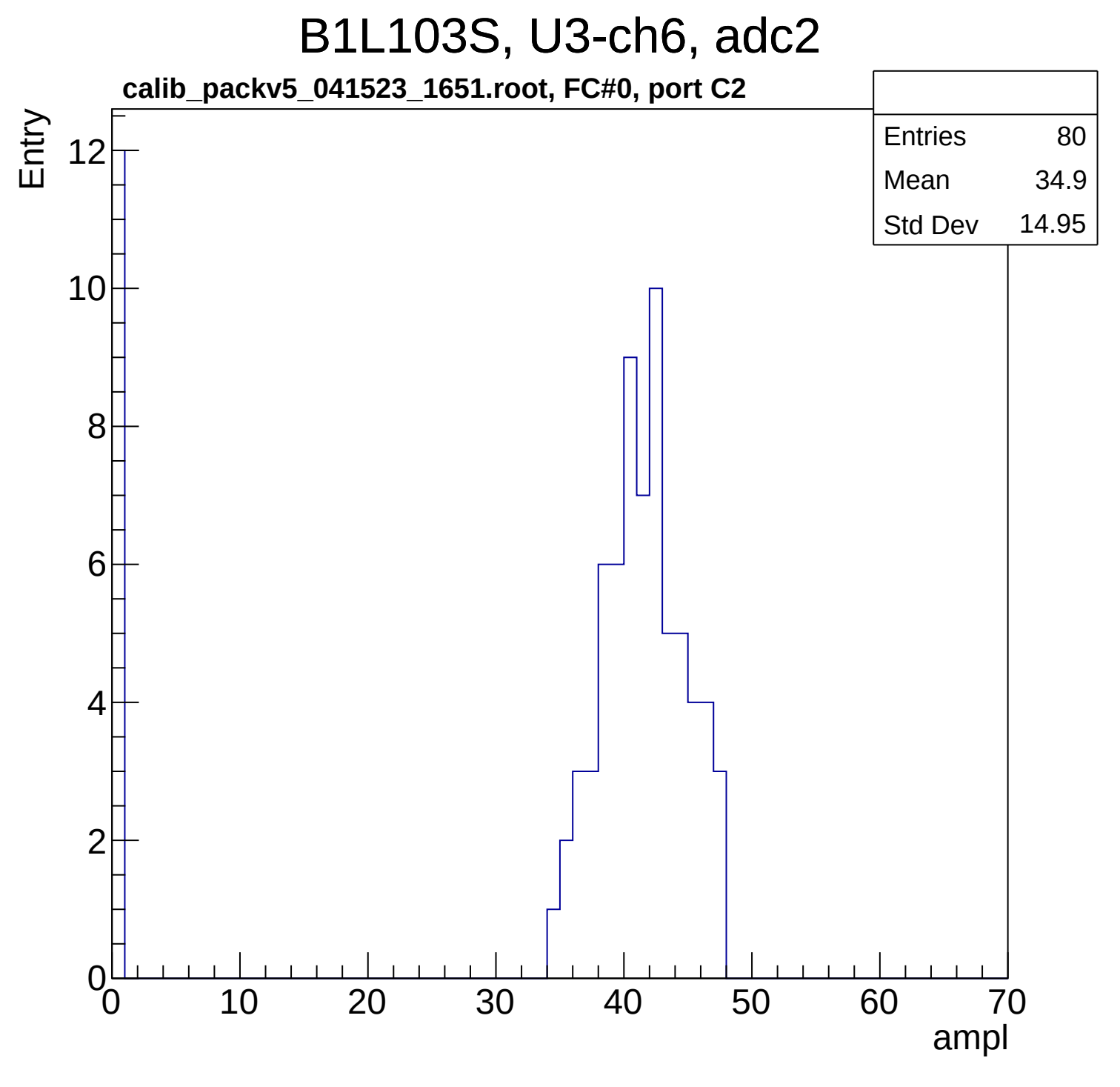
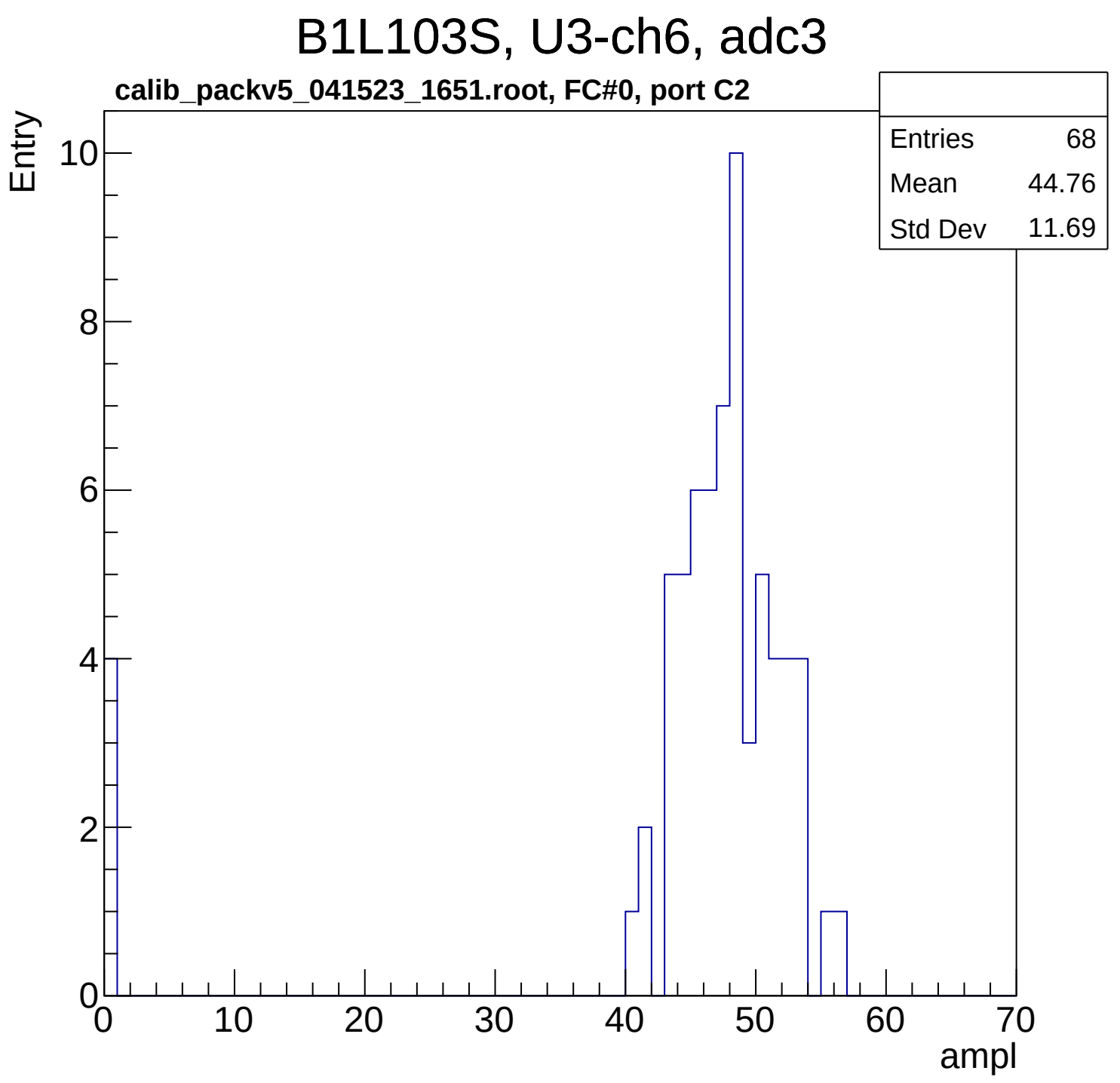
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch6, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 34.94
Std Dev 2.738
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch6, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 34.9
Std Dev 14.95
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch6, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 44.76
Std Dev 11.69
Entry
ampl
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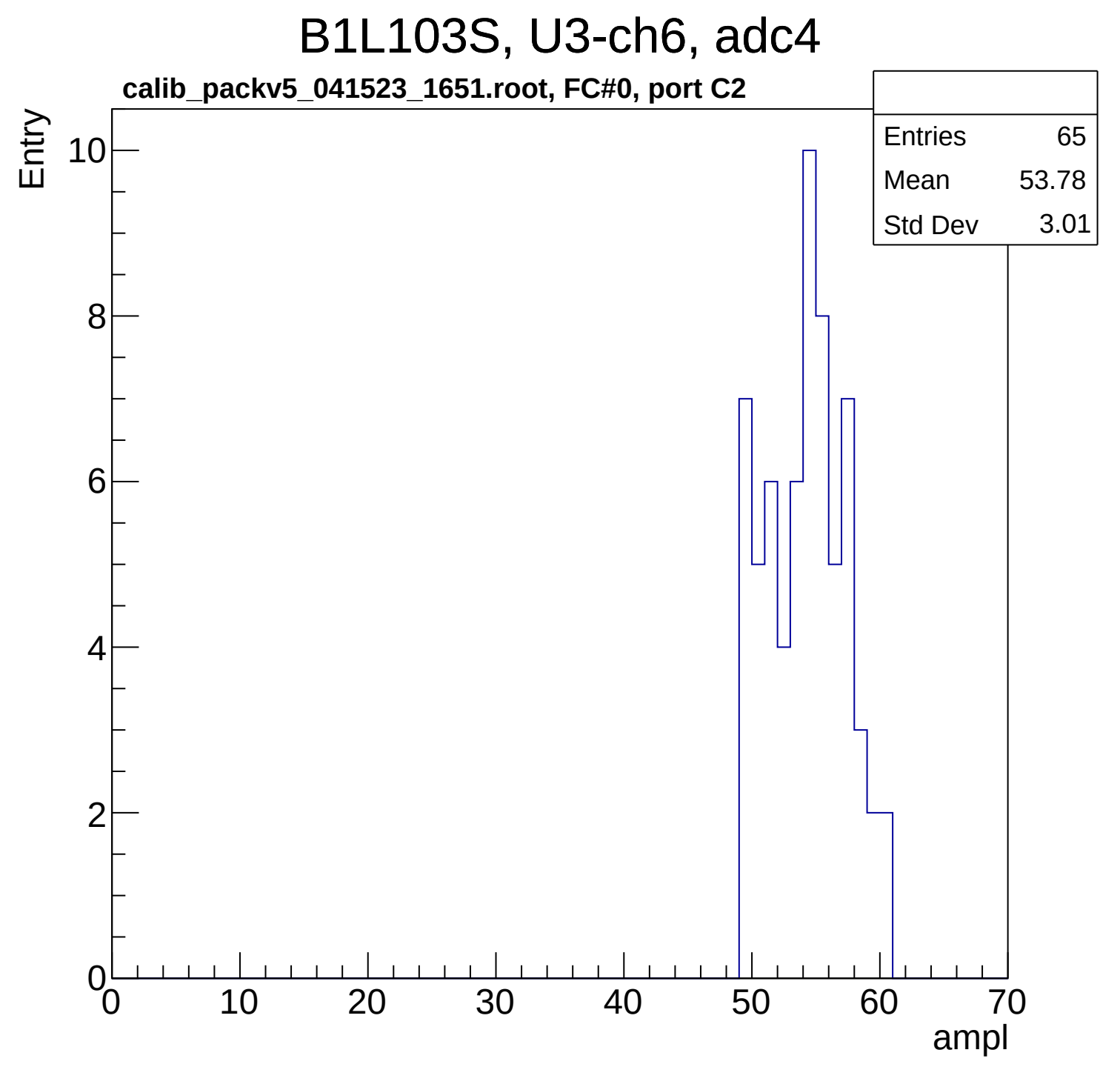
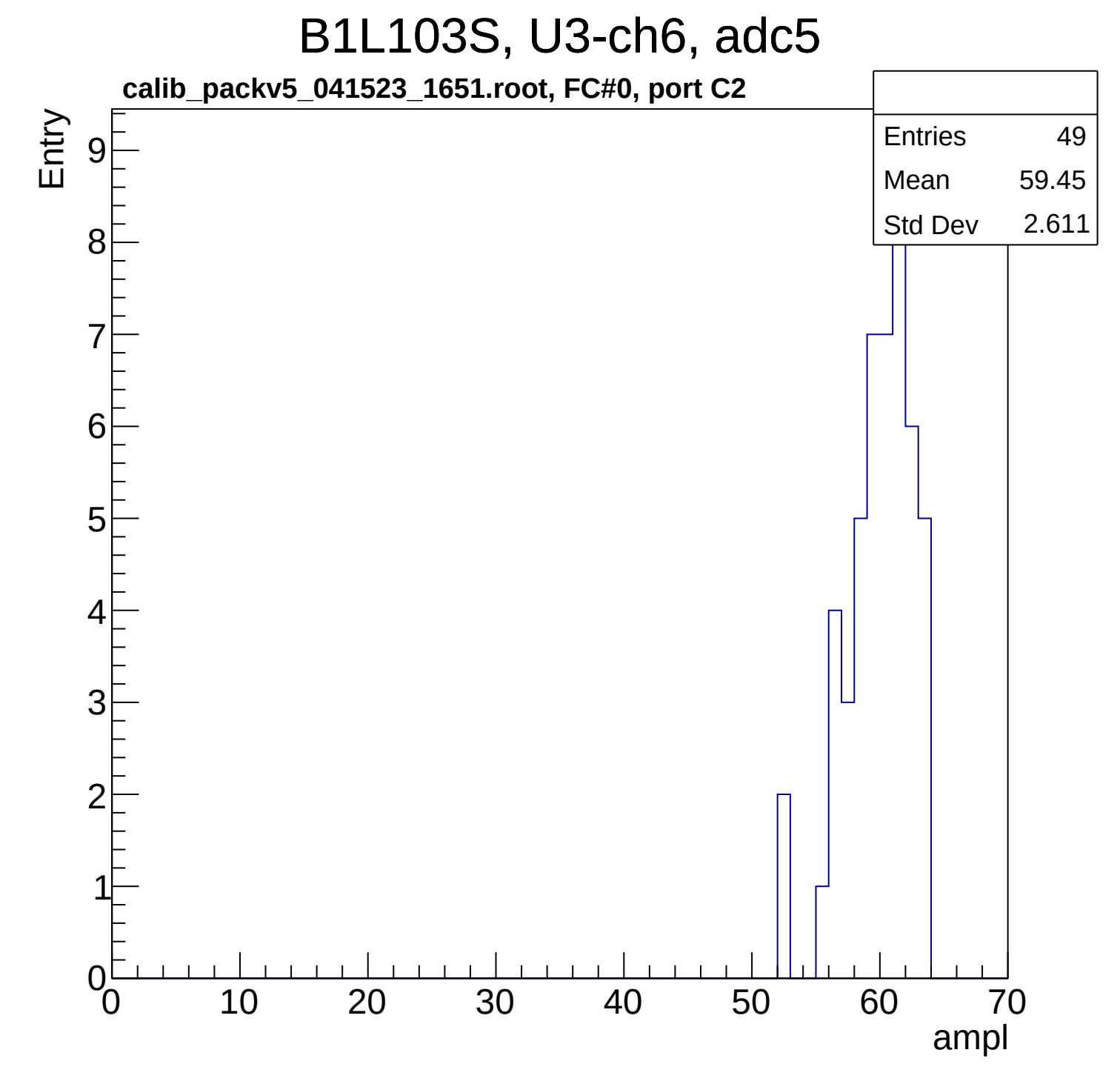
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U3-ch6, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 53.78
Std Dev 3.01
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U3-ch6, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 59.45
Std Dev 2.611
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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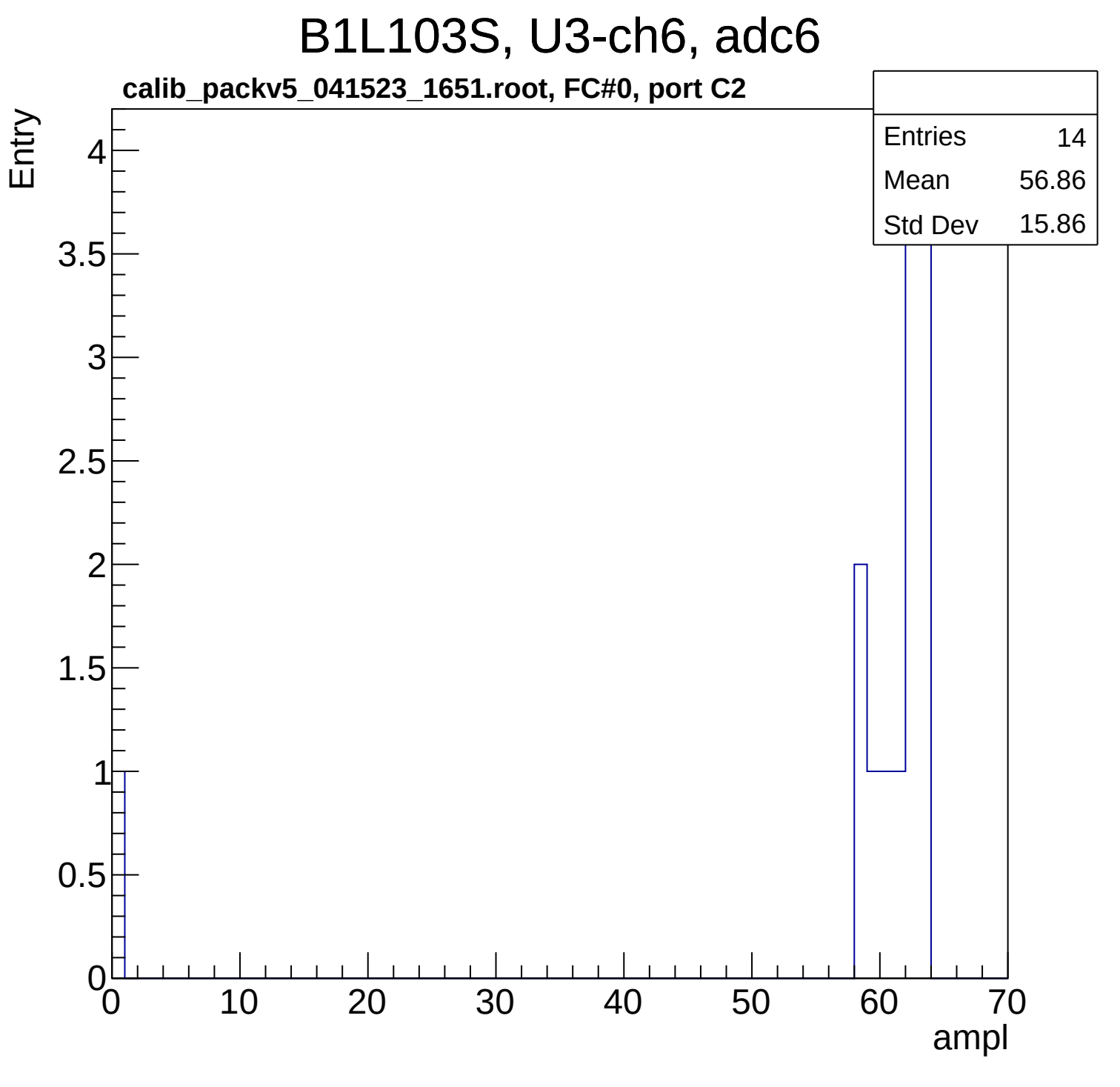
30
40
50
60
70


B1L103S, U3-ch6, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 56.86
Std Dev 15.86
Entry
ampl
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1
1.5
2
2.5
3
3.5
4
0
10
20
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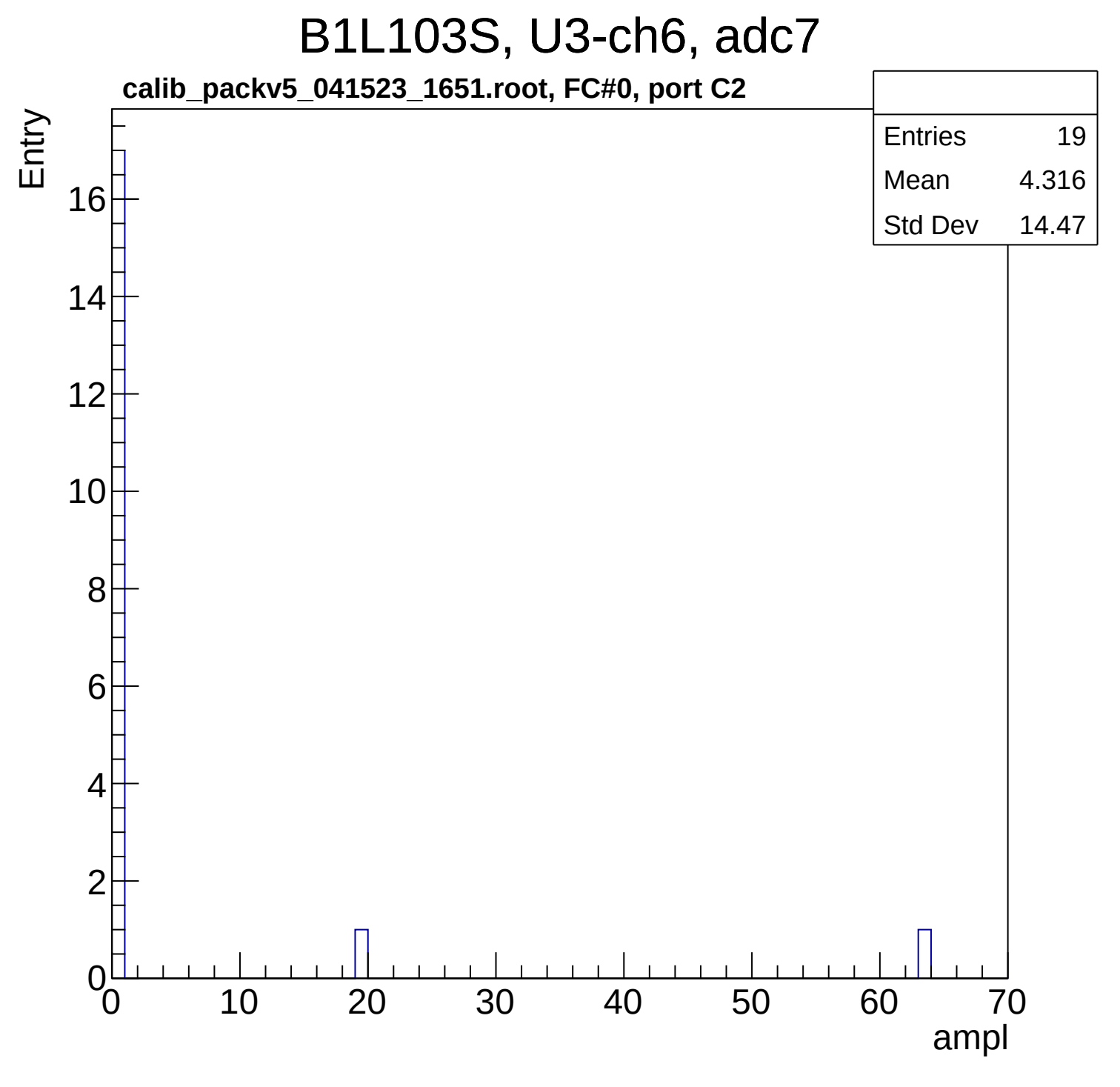
40
50
60
70


B1L103S, U3-ch6, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 4.316
Std Dev 14.47
Entry
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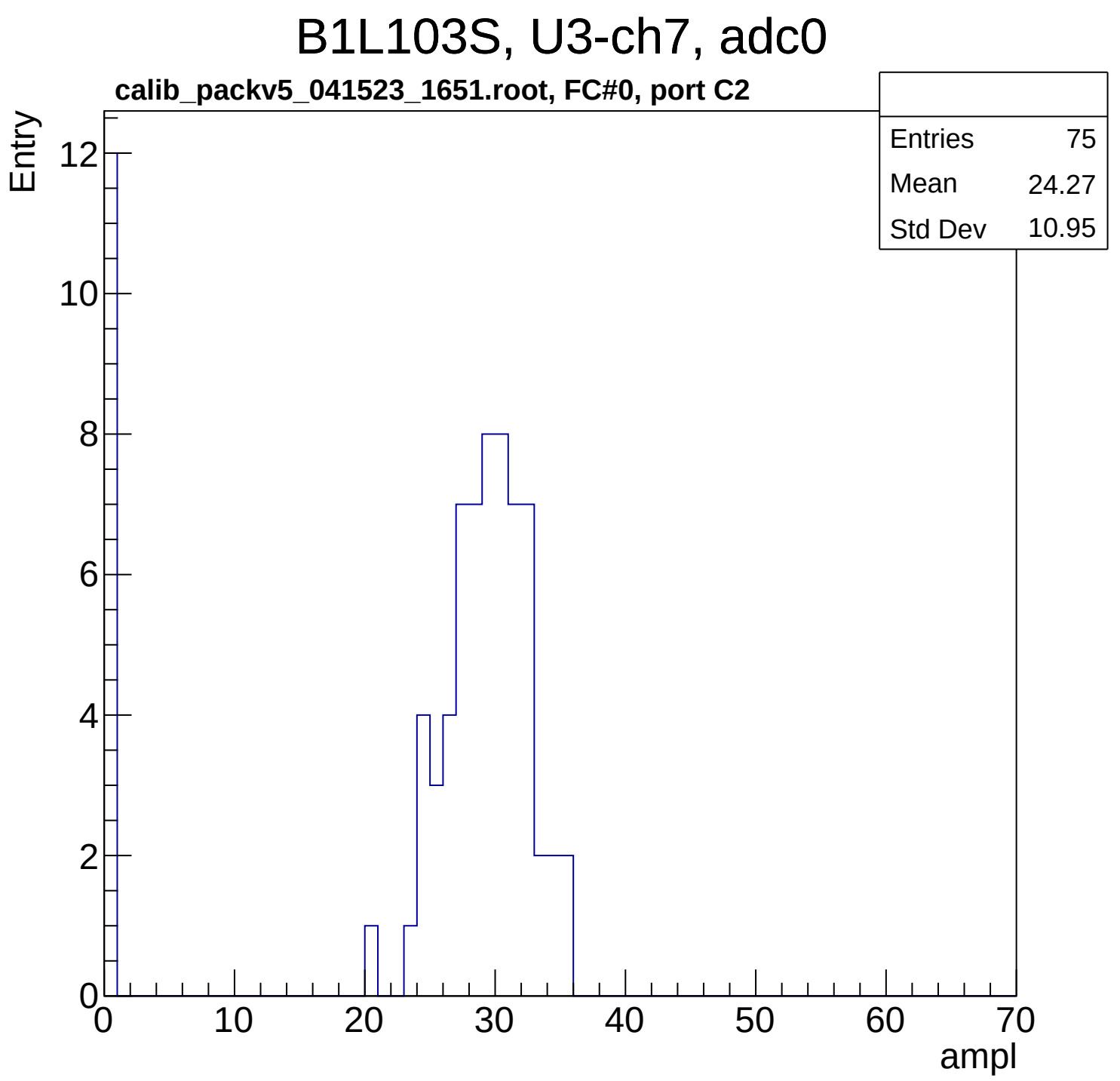
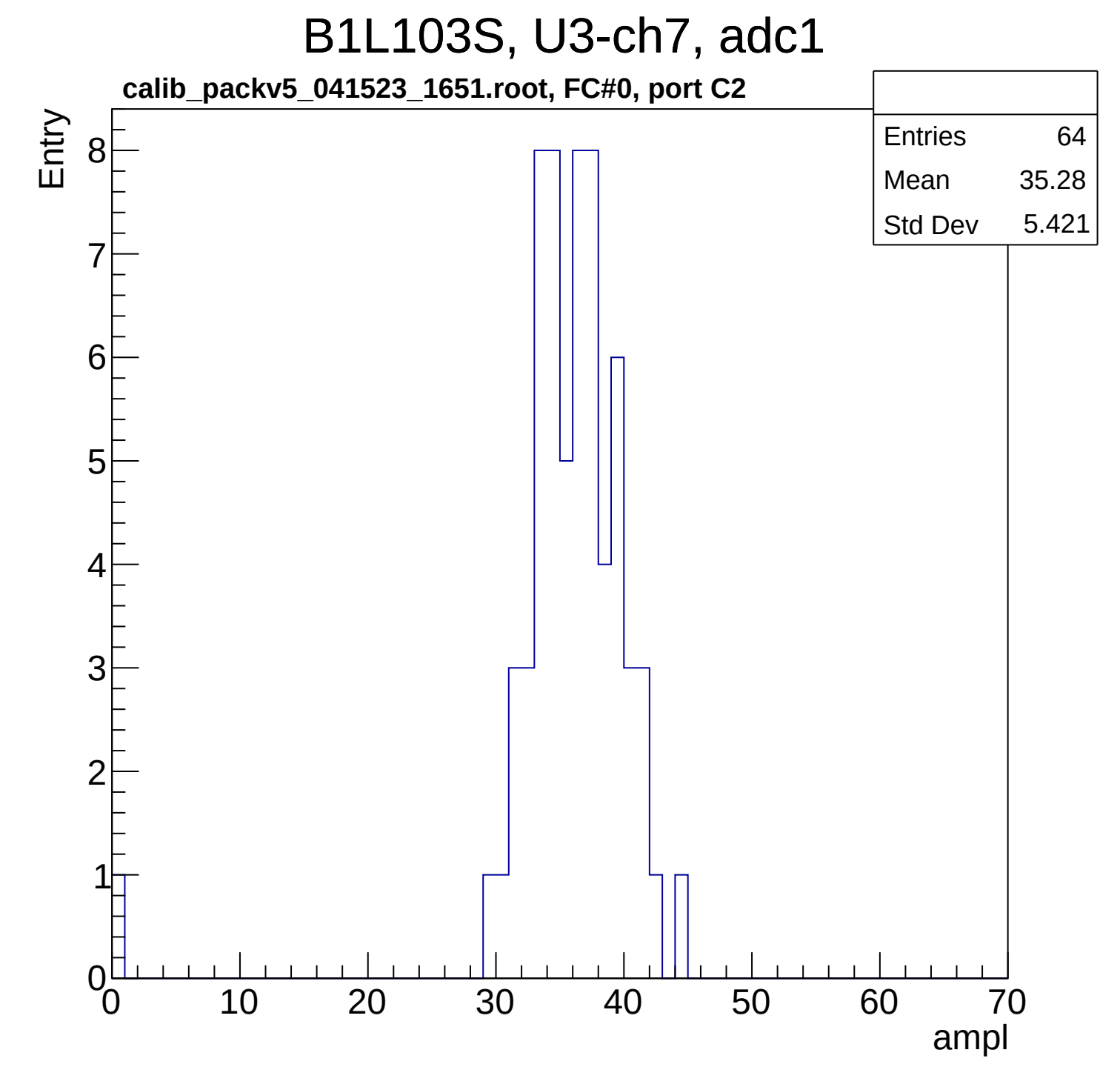
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch7, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 24.27
Std Dev 10.95
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch7, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 35.28
Std Dev 5.421
Entry
ampl
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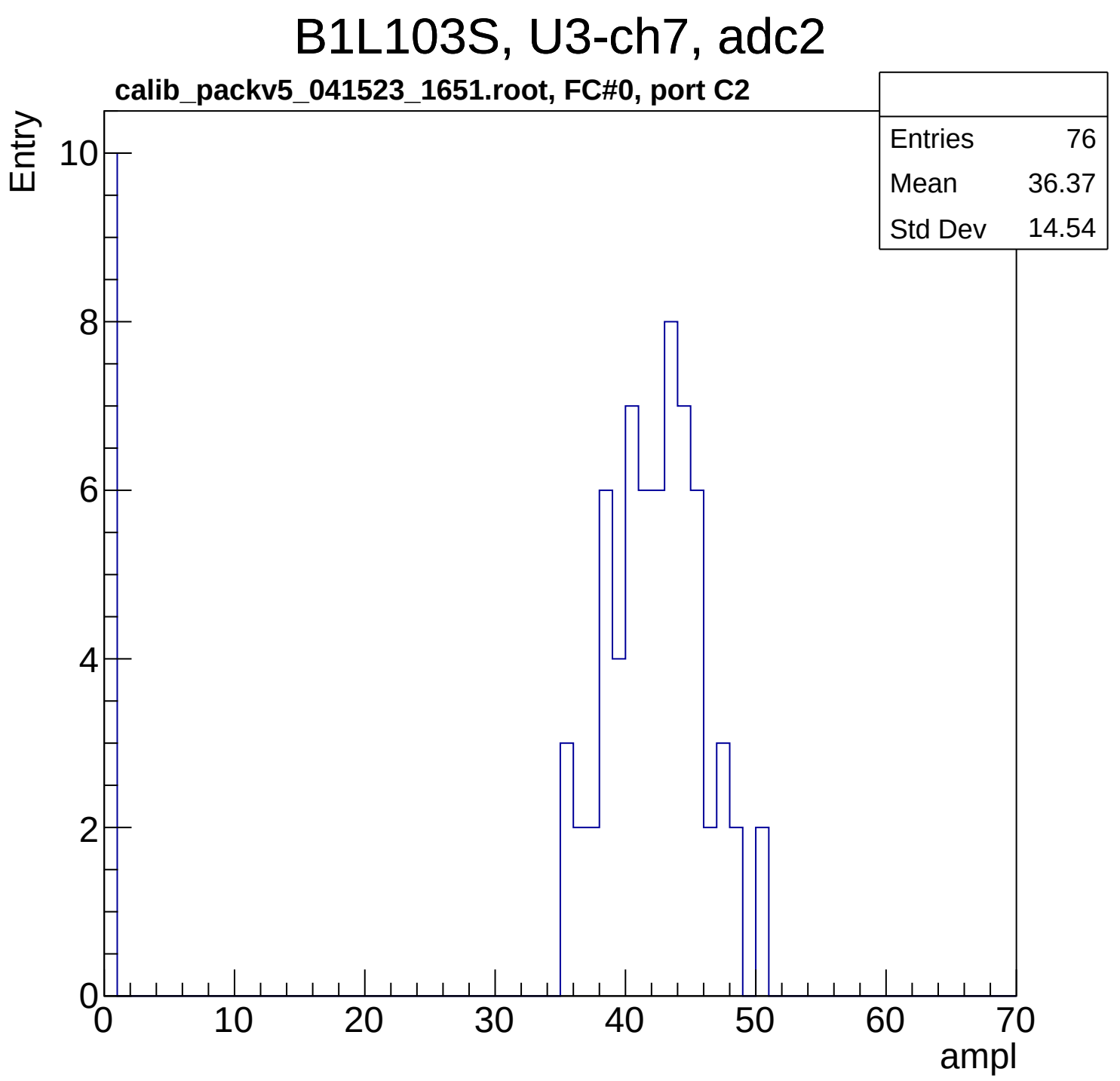
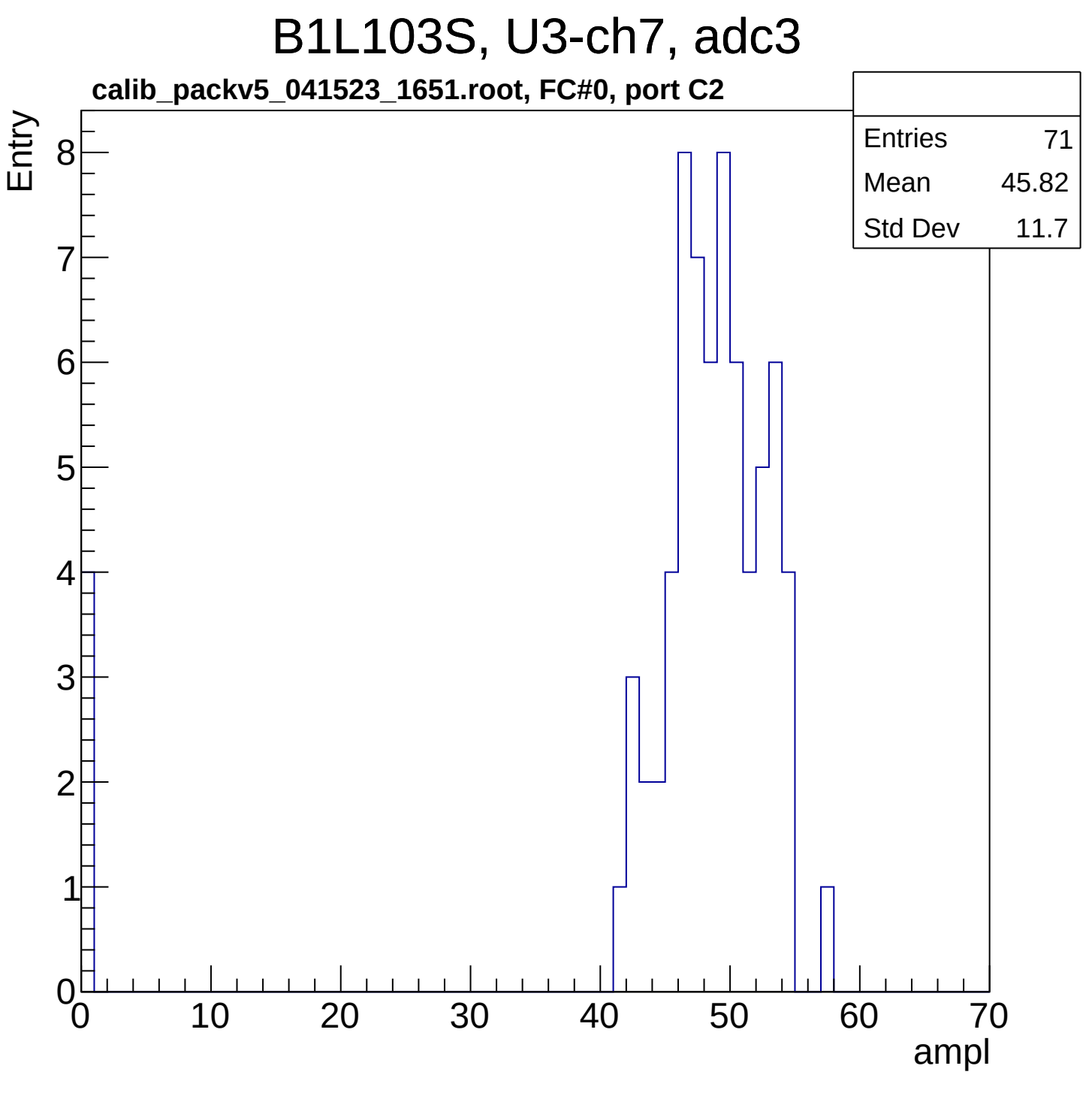
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch7, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 36.37
Std Dev 14.54
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U3-ch7, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 45.82
Std Dev 11.7
Entry
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2
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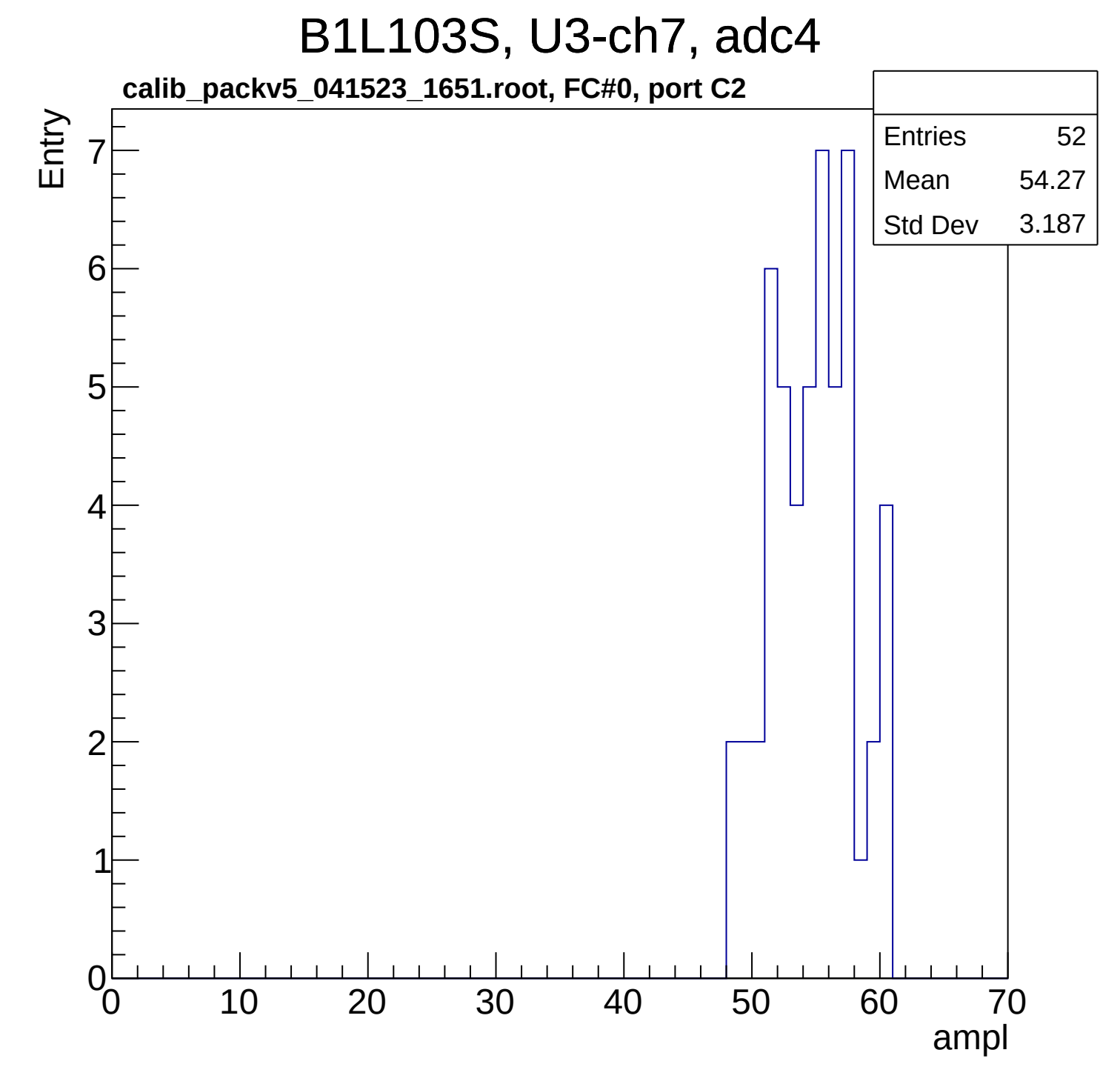
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch7, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 54.27
Std Dev 3.187
Entry
ampl
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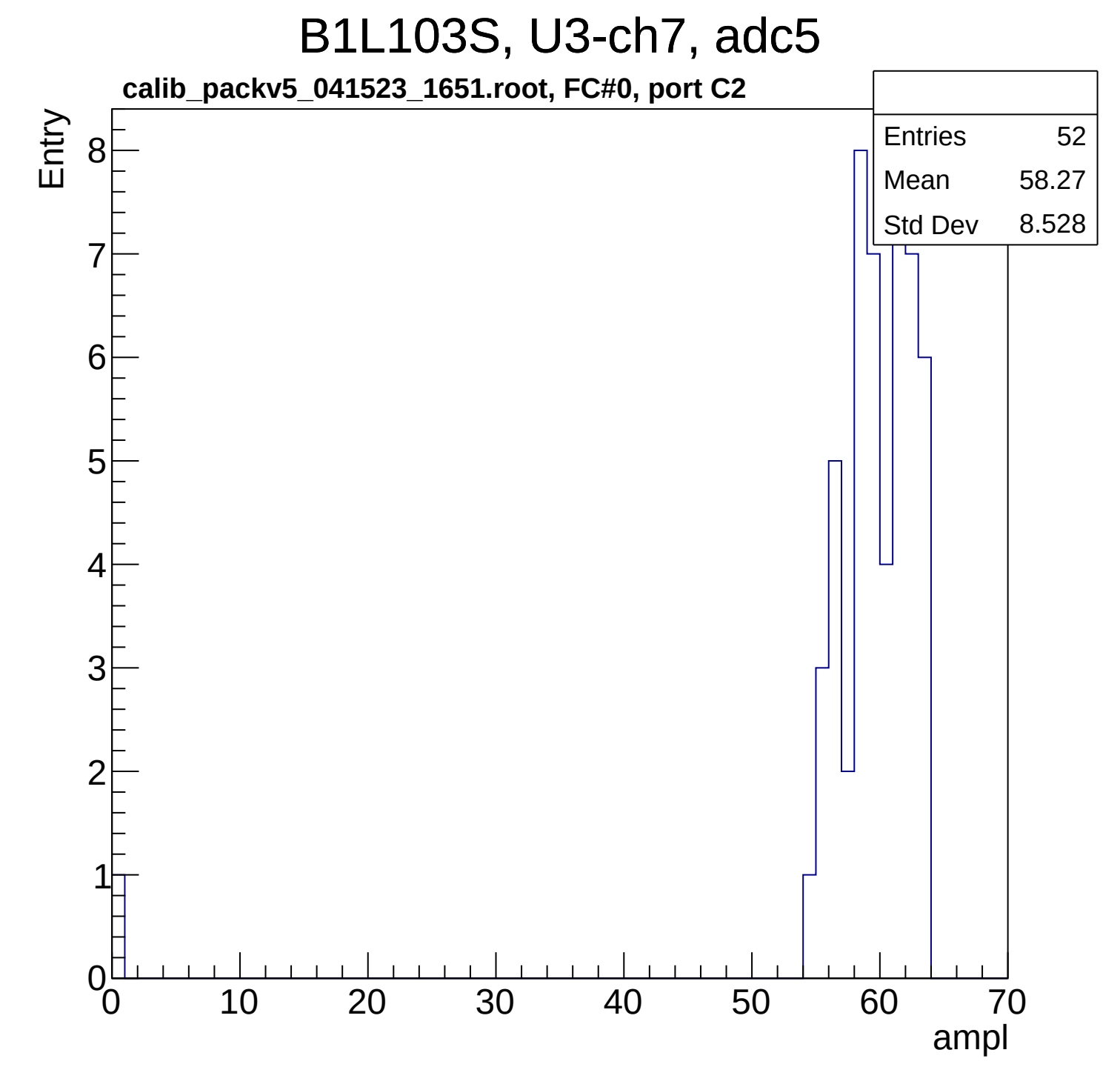
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch7, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 58.27
Std Dev 8.528
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
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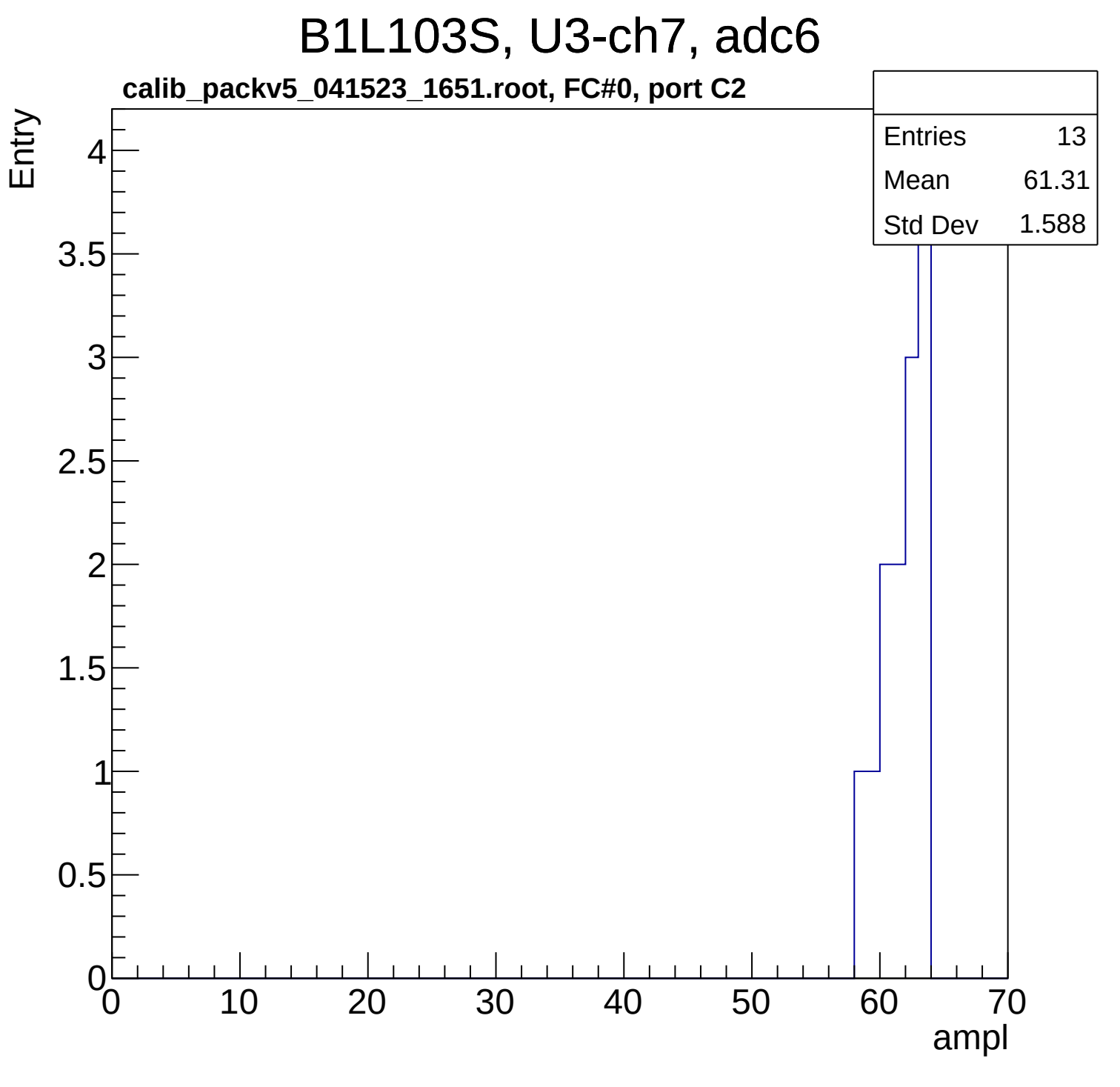
30
40
50
60
70


B1L103S, U3-ch7, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 61.31
Std Dev 1.588
Entry
ampl
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1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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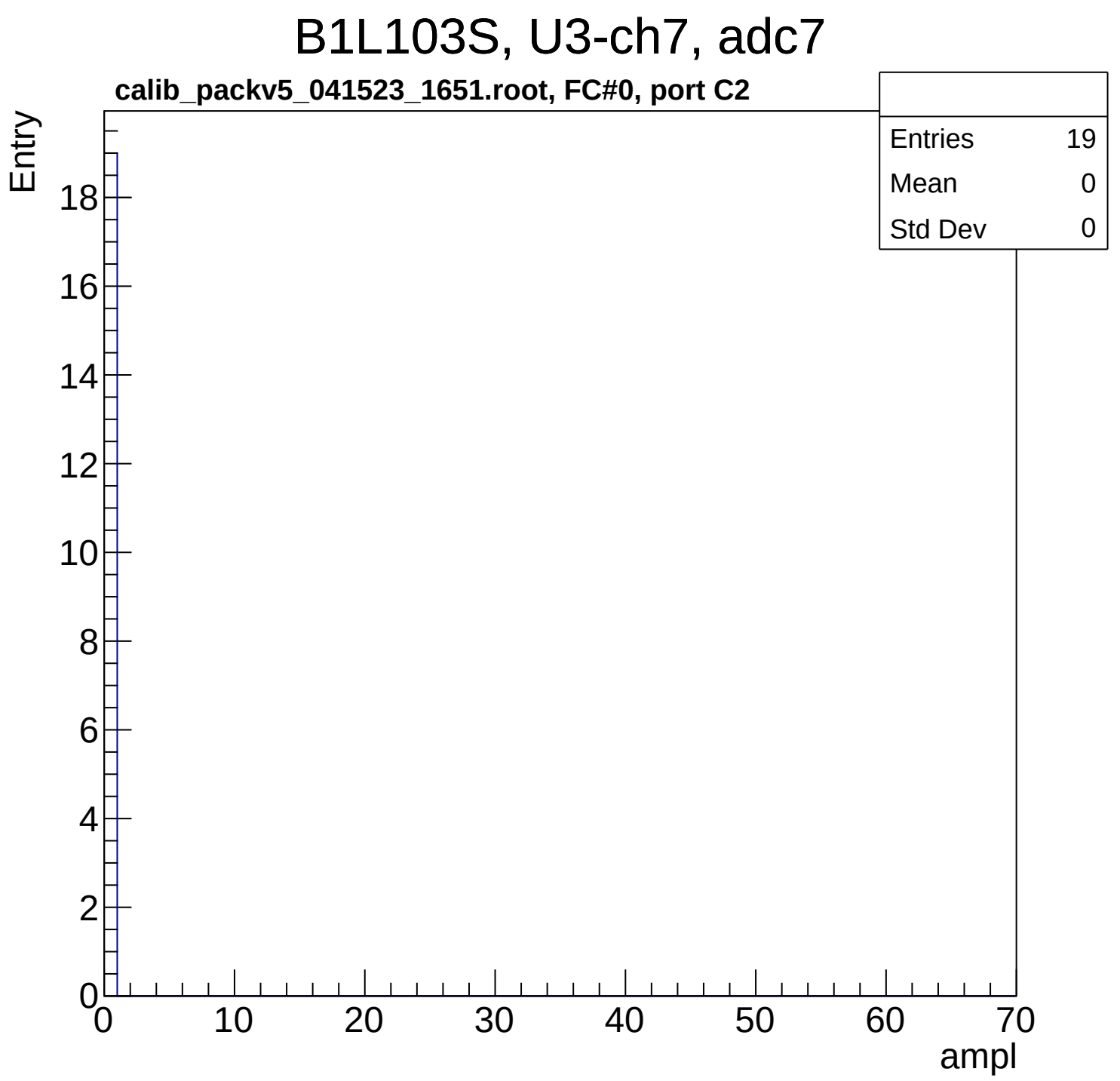
B1L103S, U3-ch7, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
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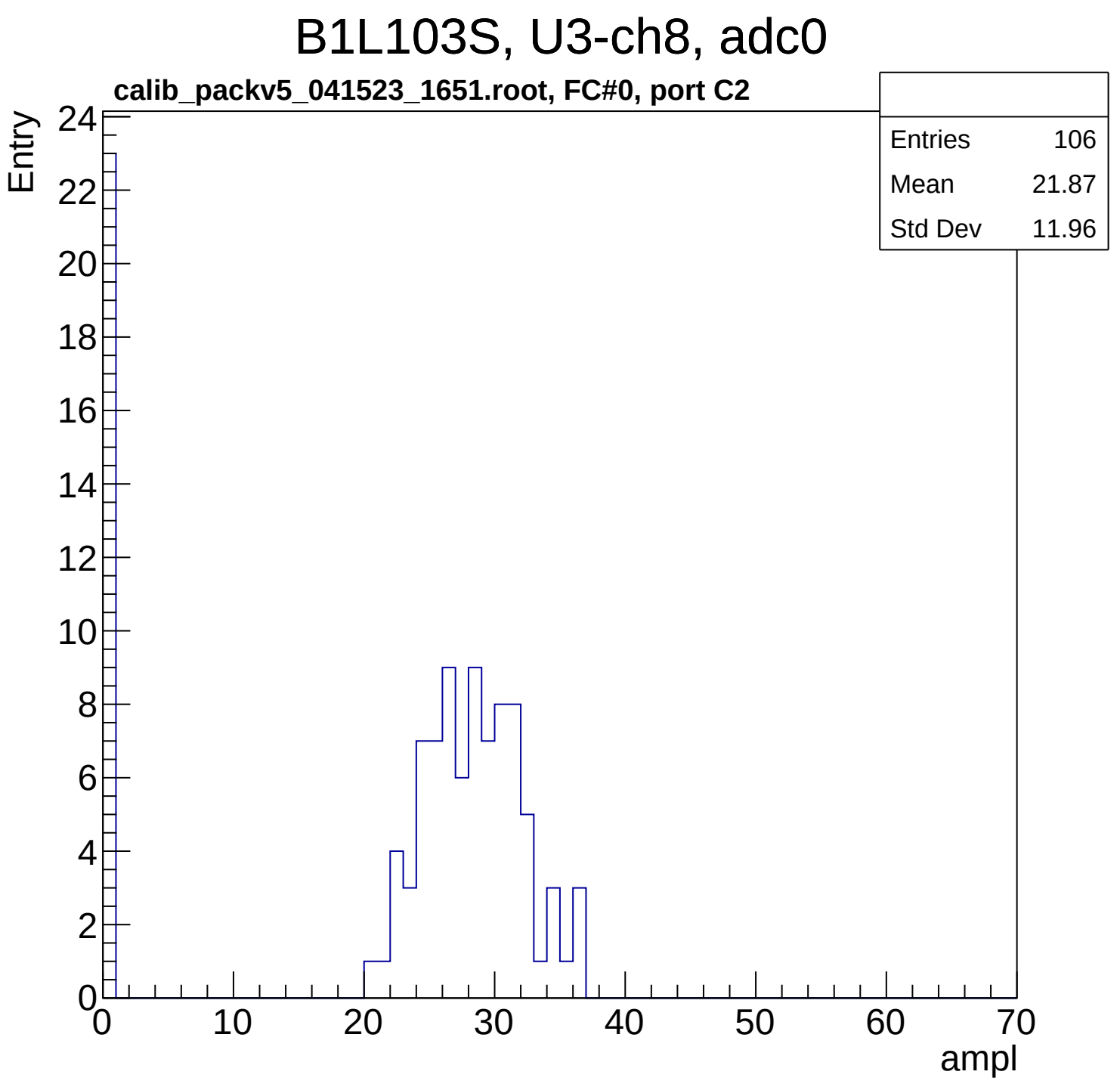
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch8, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 106
Mean 21.87
Std Dev 11.96
Entry
ampl
0
2
4
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8
10
12
14
16
18
20
22
24
0
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40
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60
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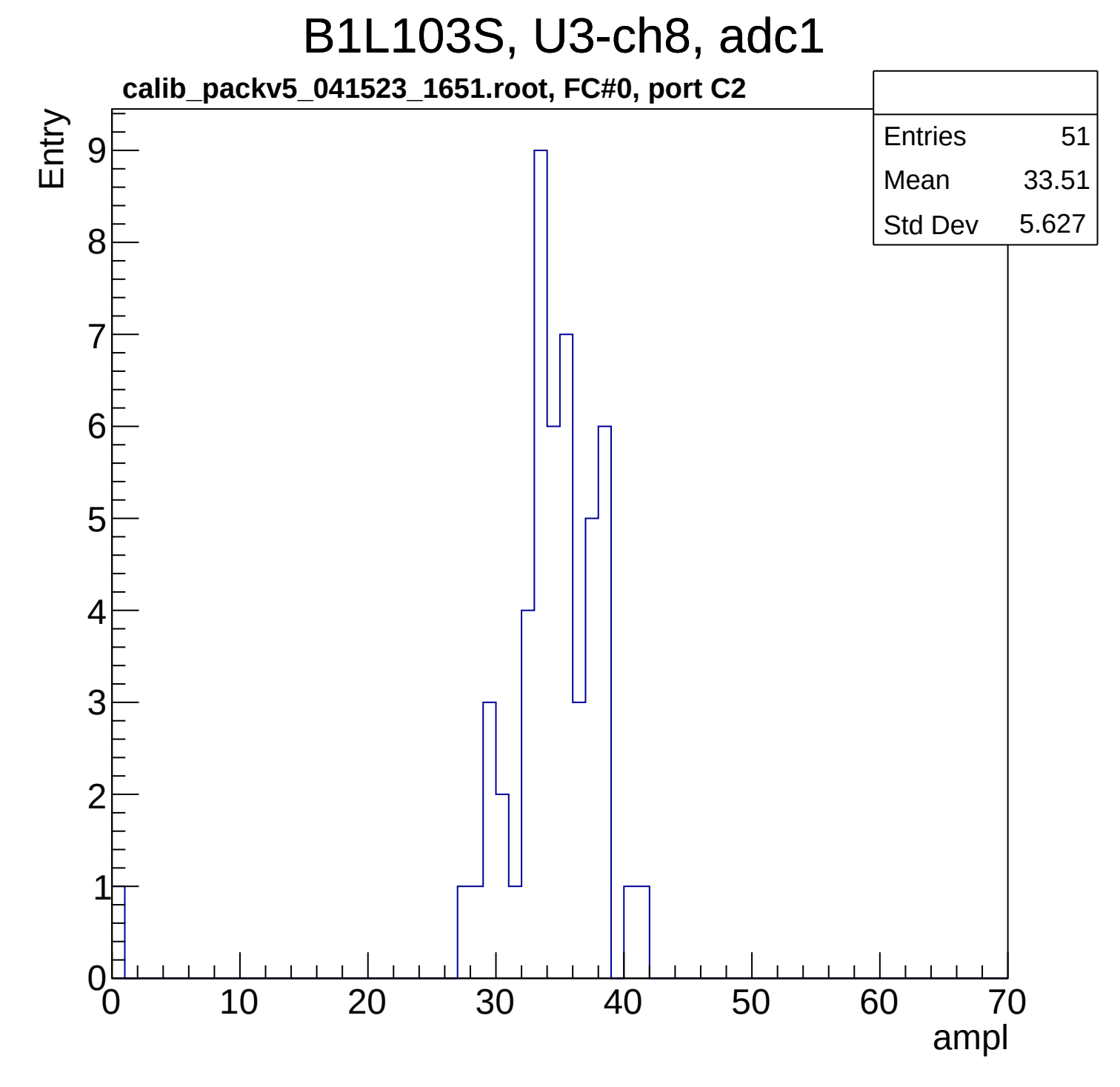
B1L103S, U3-ch8, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 33.51
Std Dev 5.627
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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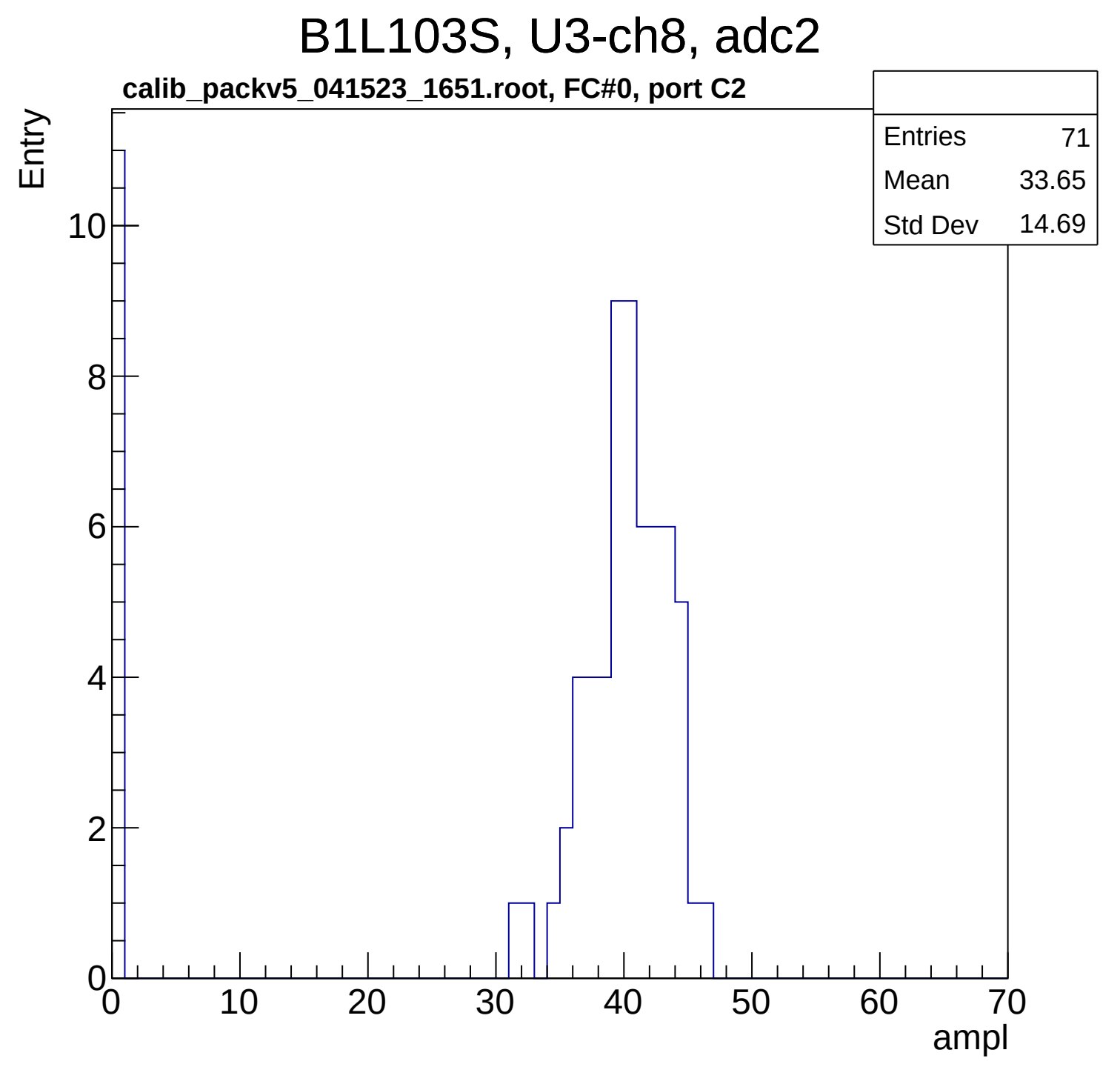
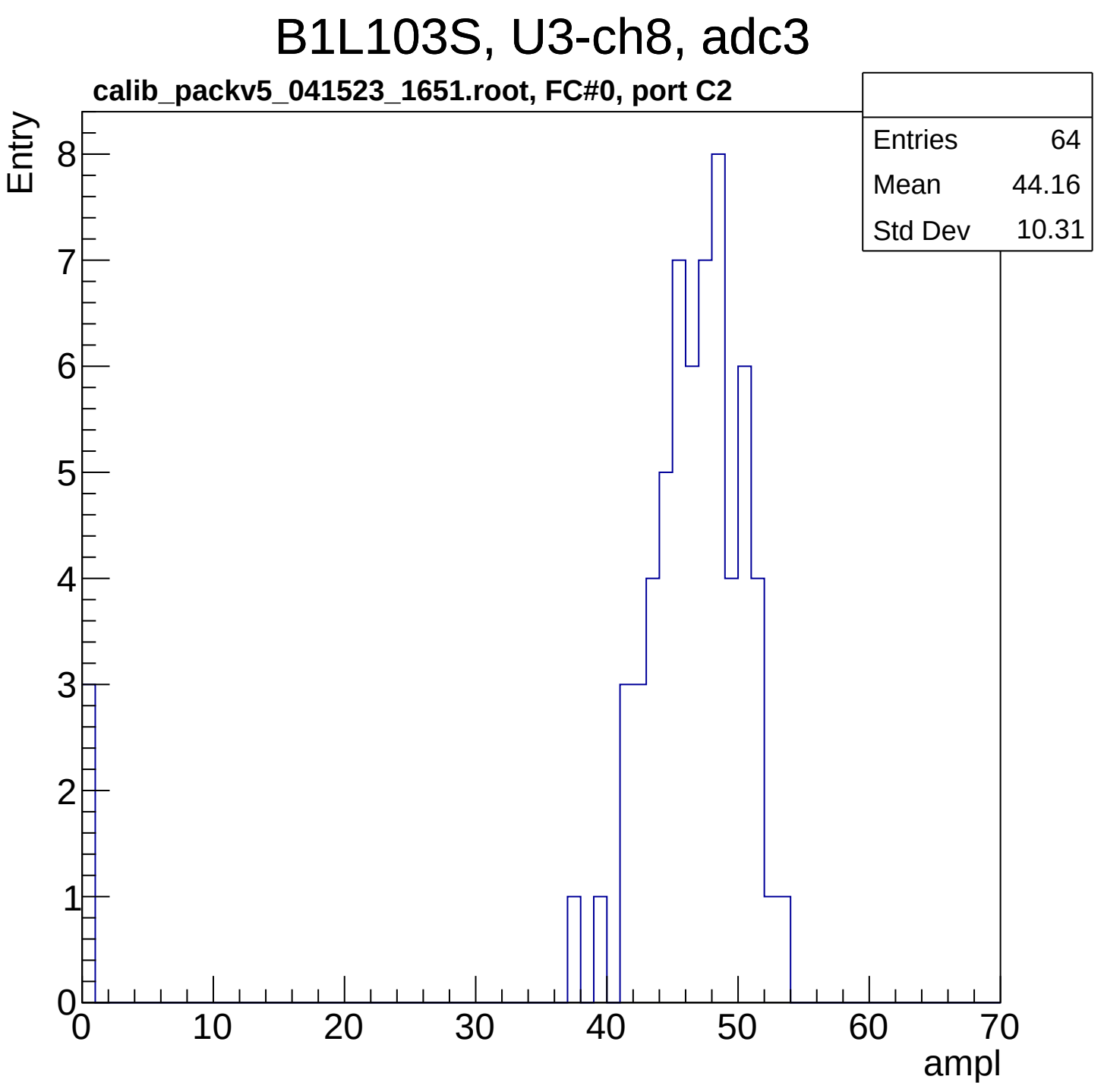

B1L103S, U3-ch8, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 33.65
Std Dev 14.69
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch8, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 44.16
Std Dev 10.31
Entry
ampl
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2
3
4
5
6
7
8
0
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40
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60
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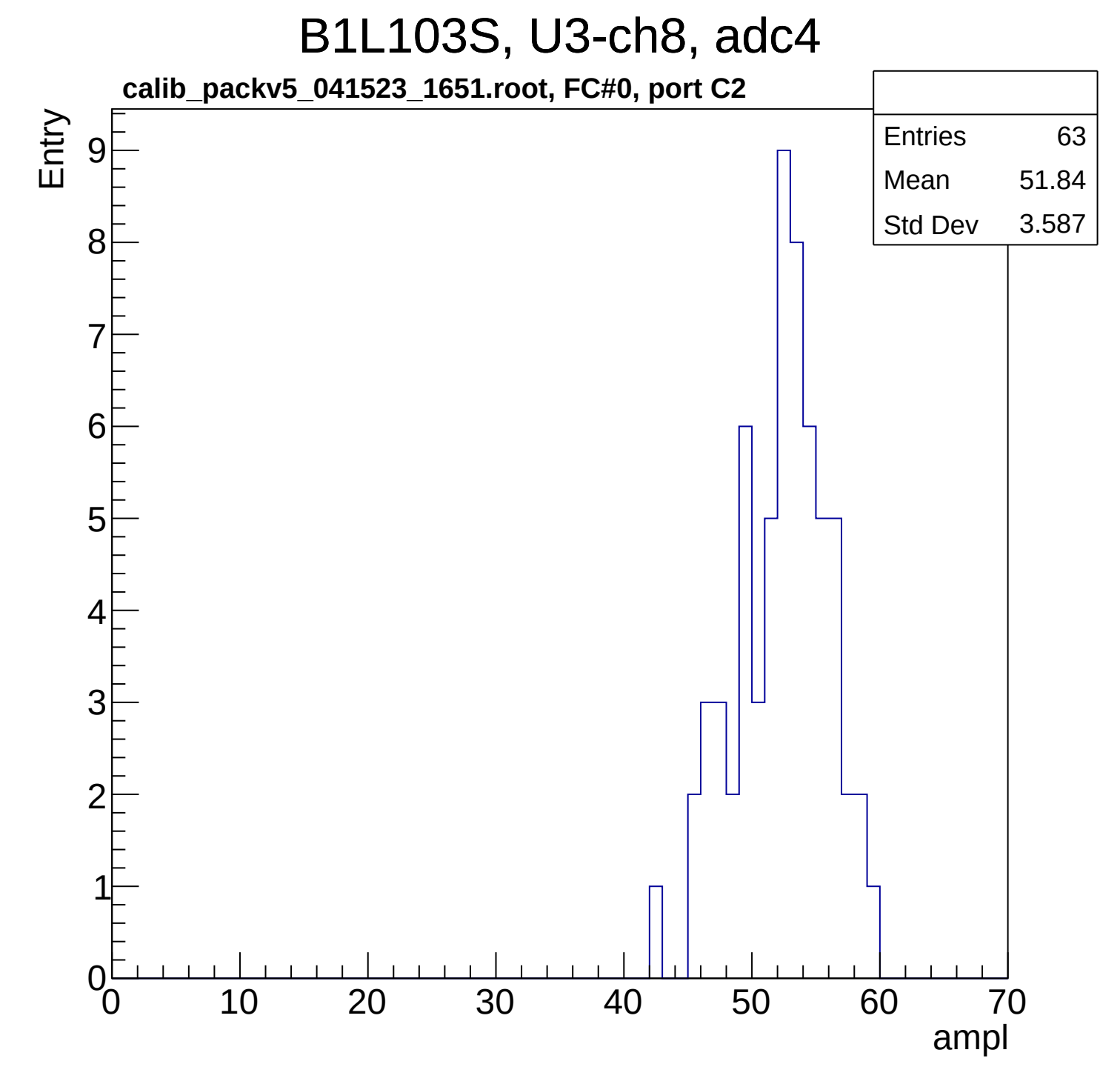
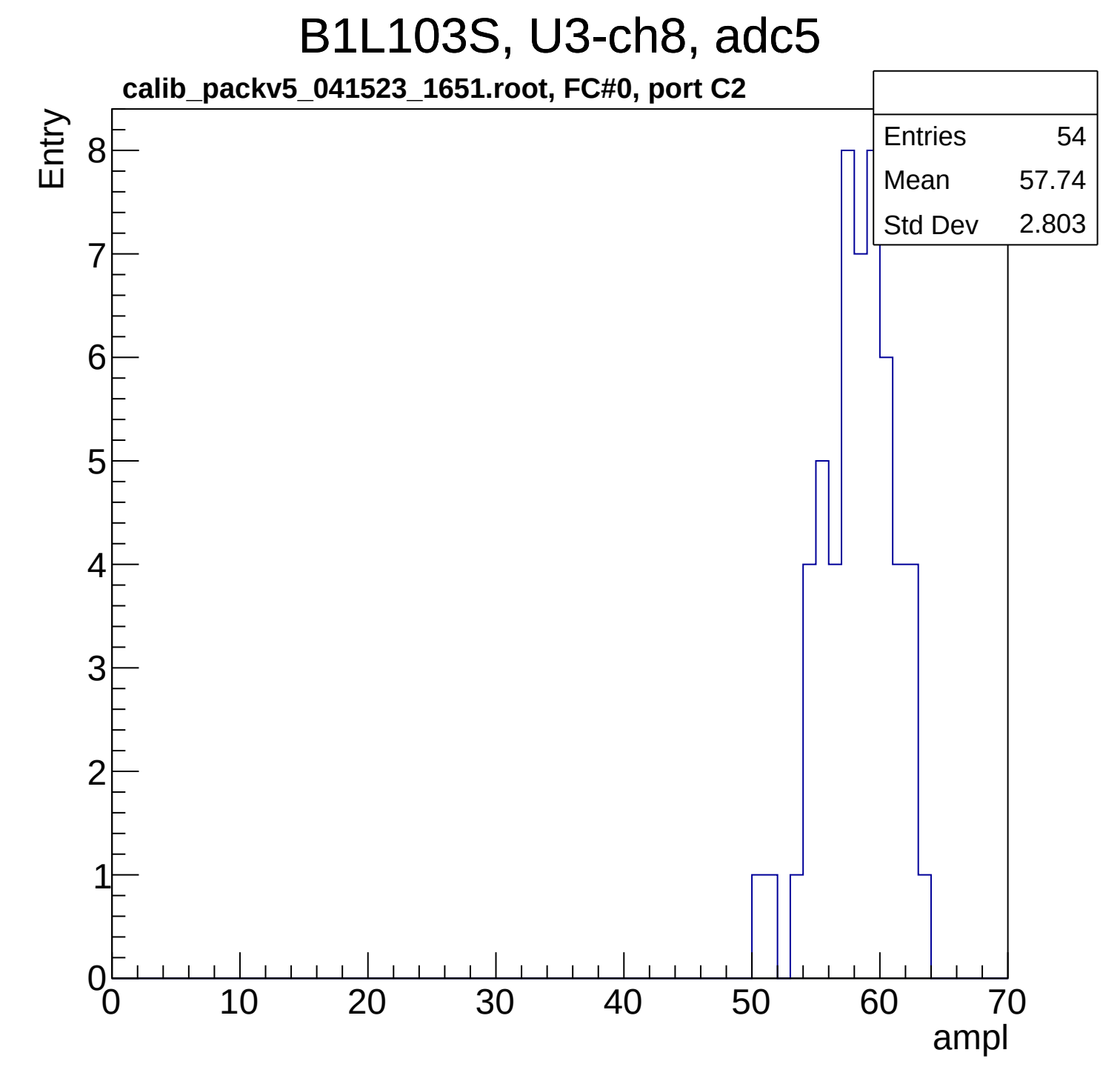

B1L103S, U3-ch8, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 51.84
Std Dev 3.587
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch8, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 57.74
Std Dev 2.803
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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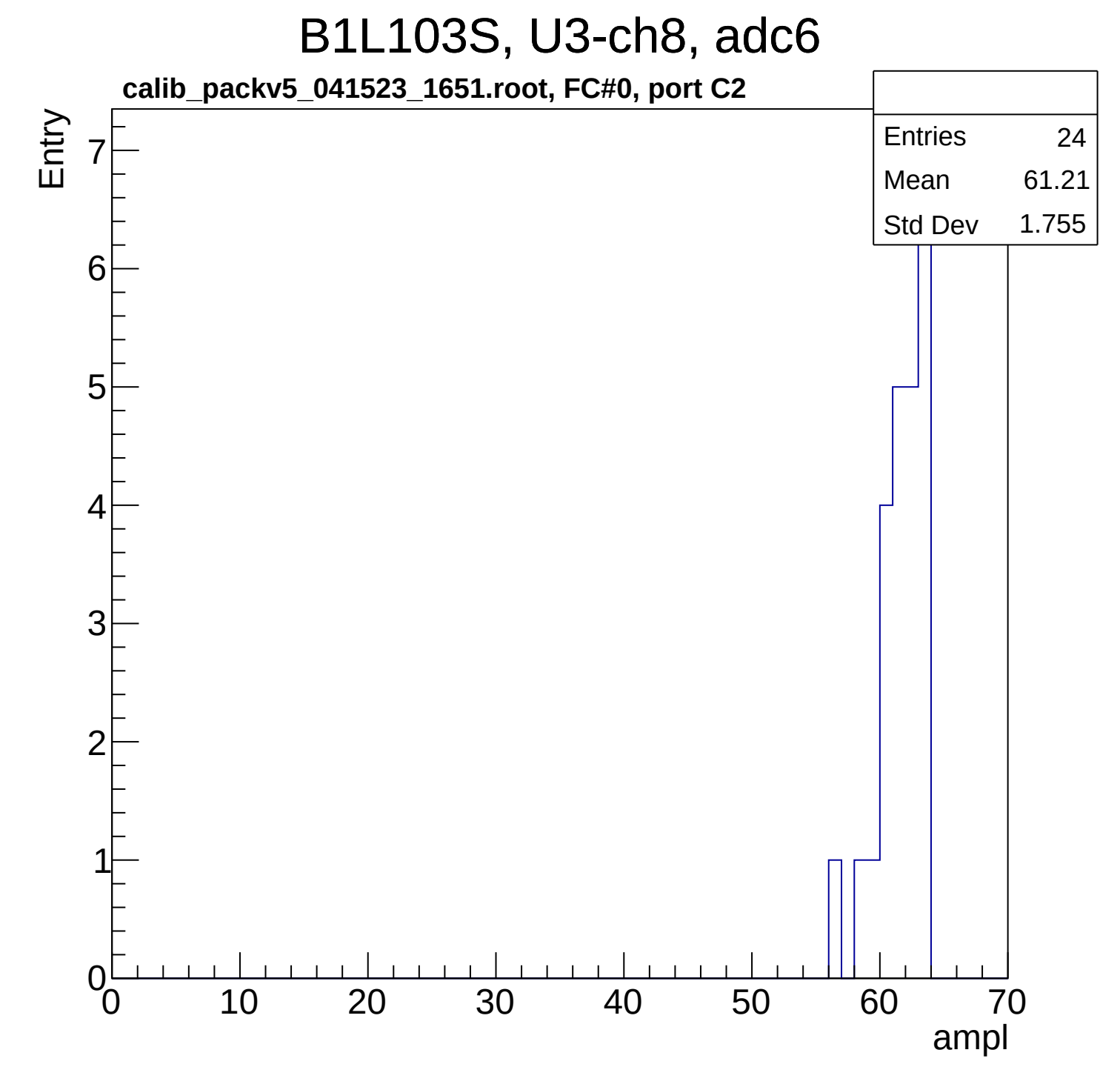
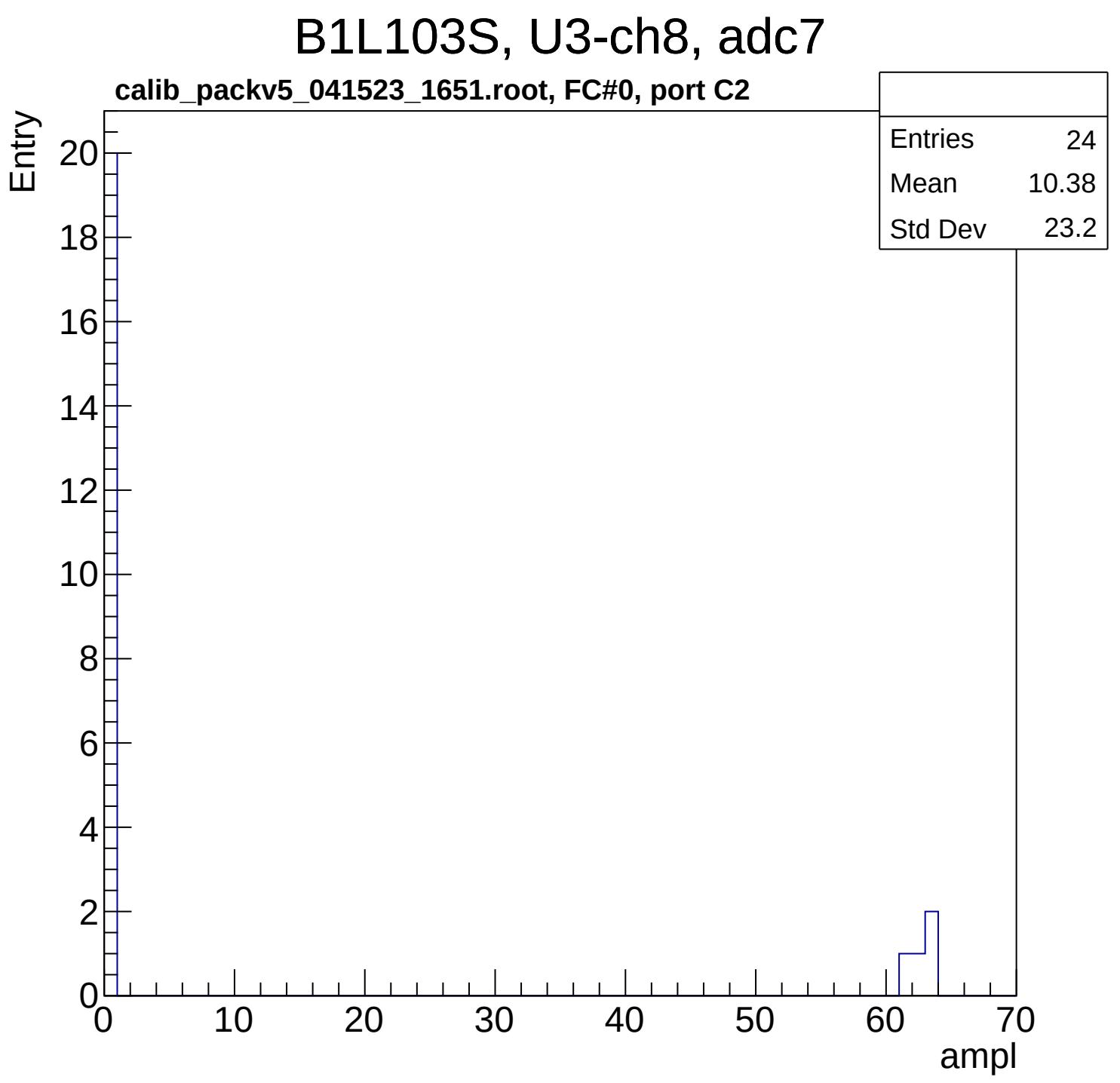
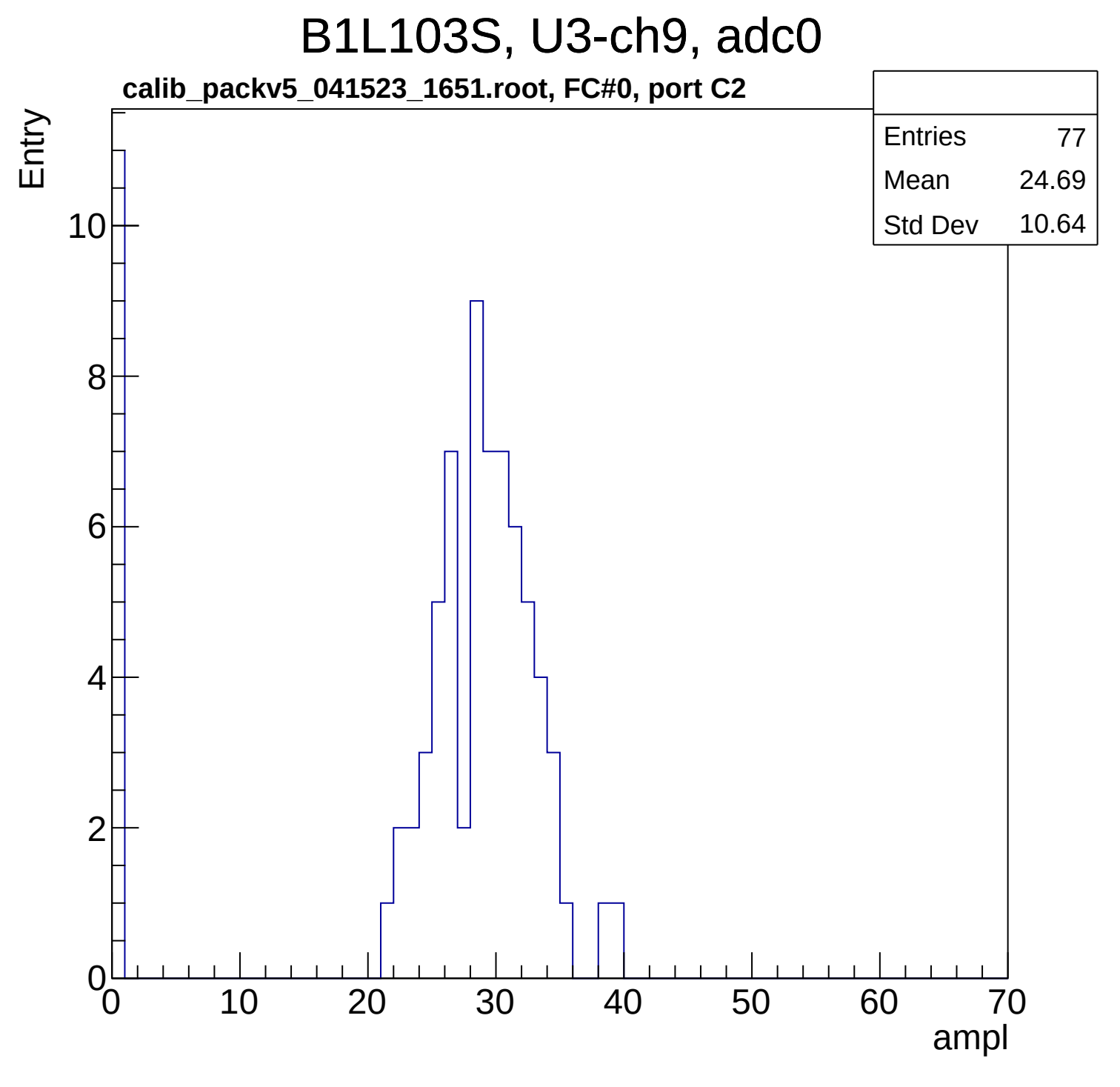
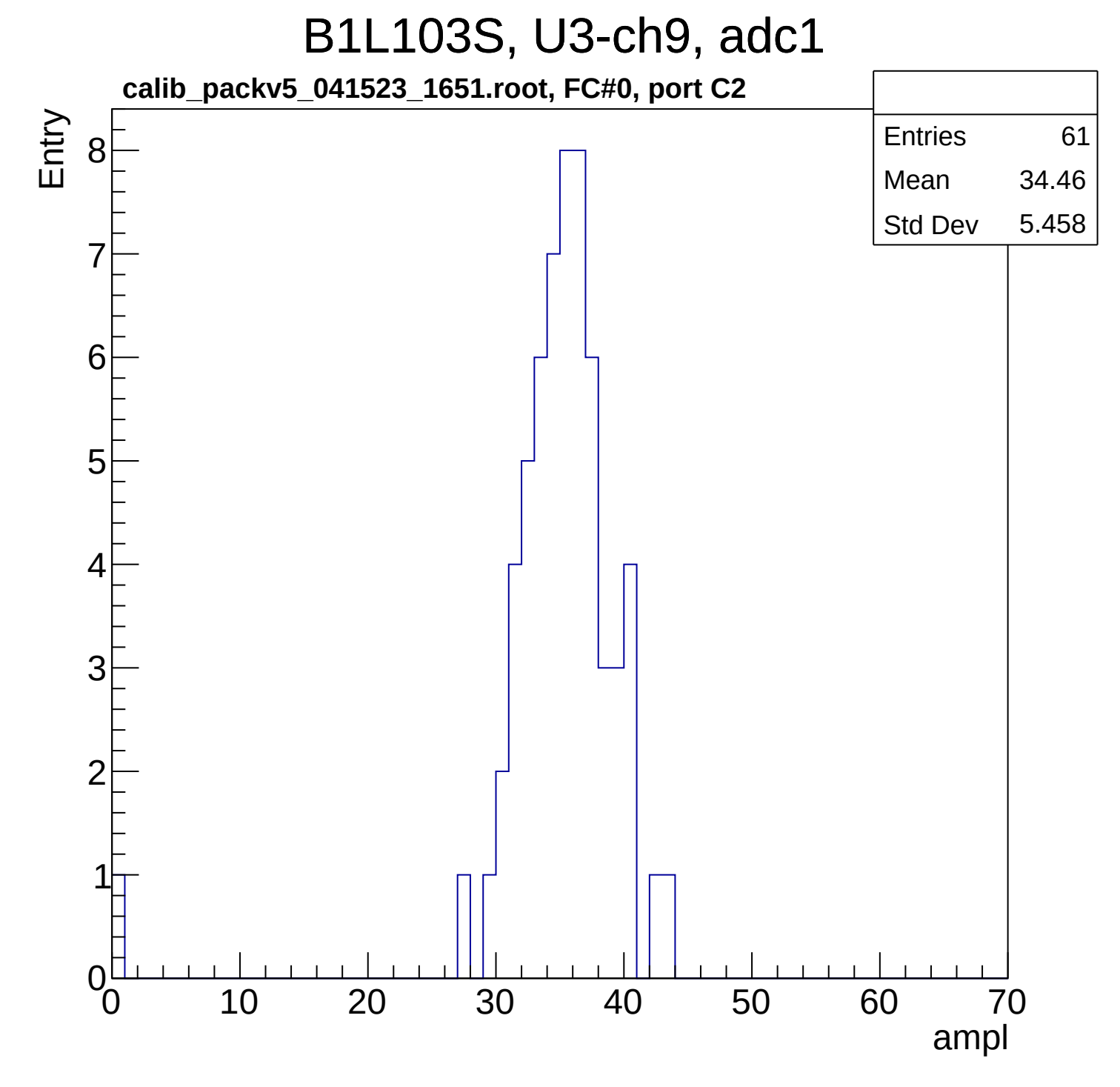
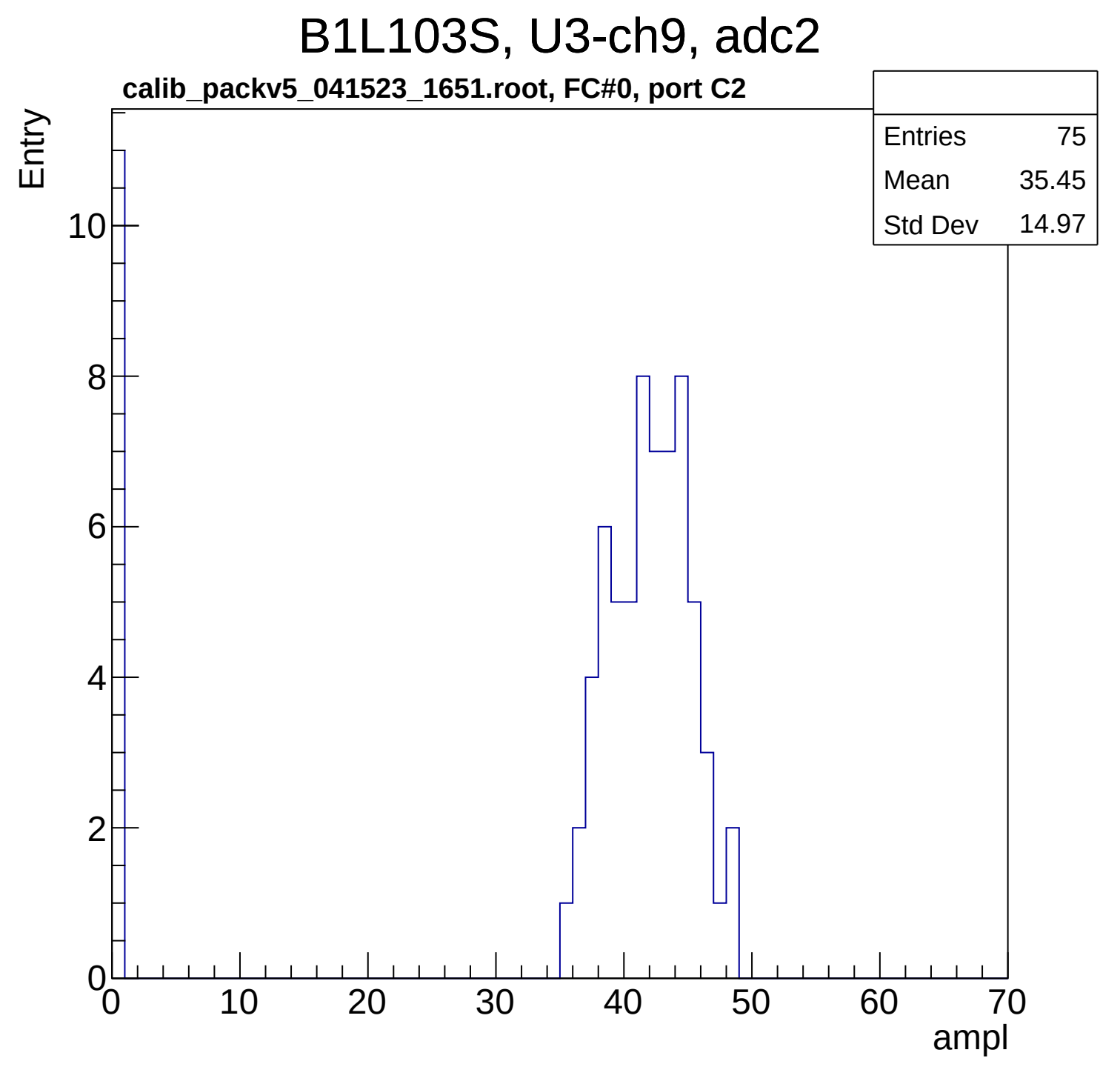
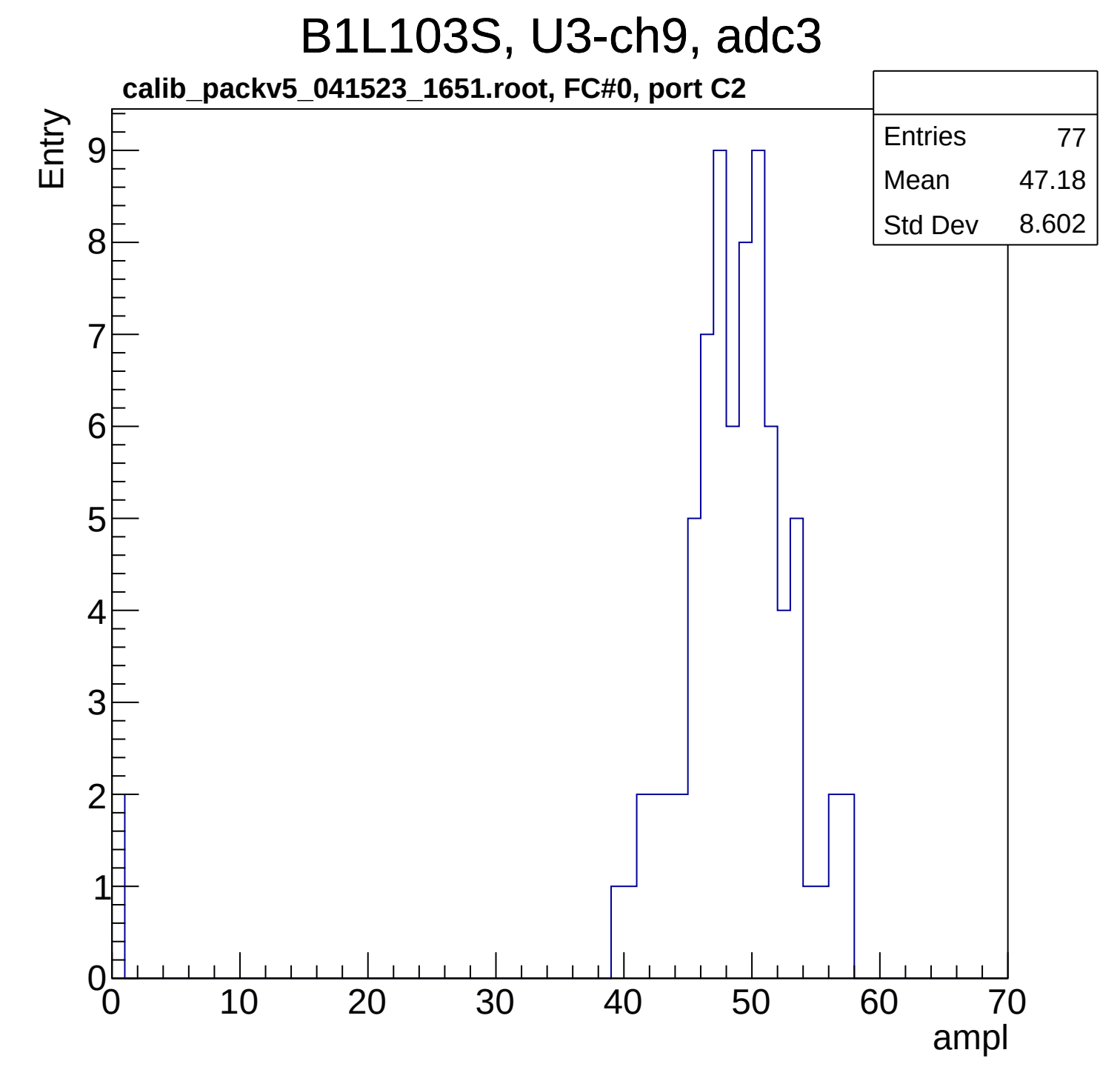

B1L103S, U3-ch8, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 61.21
Std Dev 1.755
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

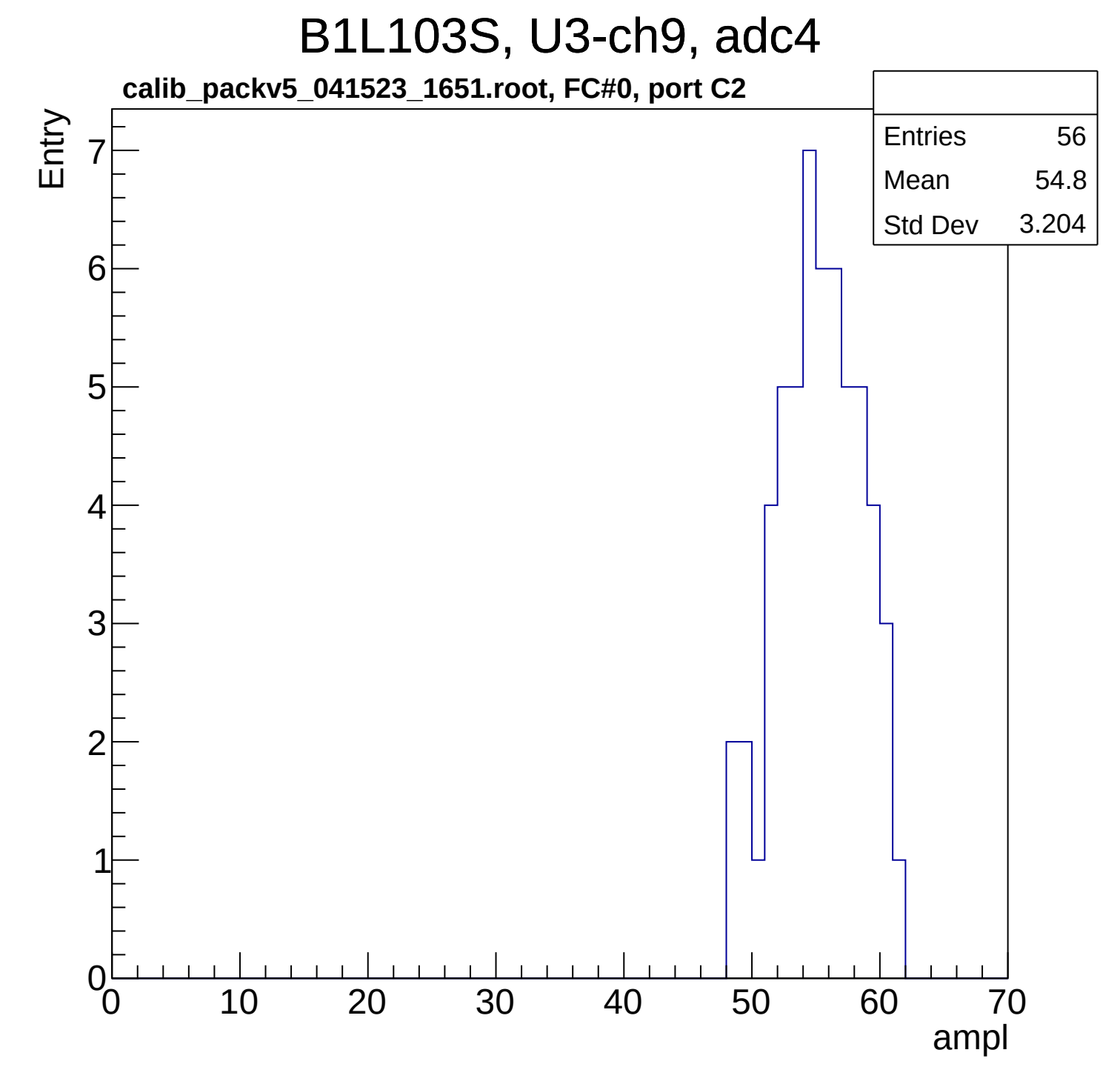

B1L103S, U3-ch8, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 10.38
Std Dev 23.2
Entry
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70
ampl

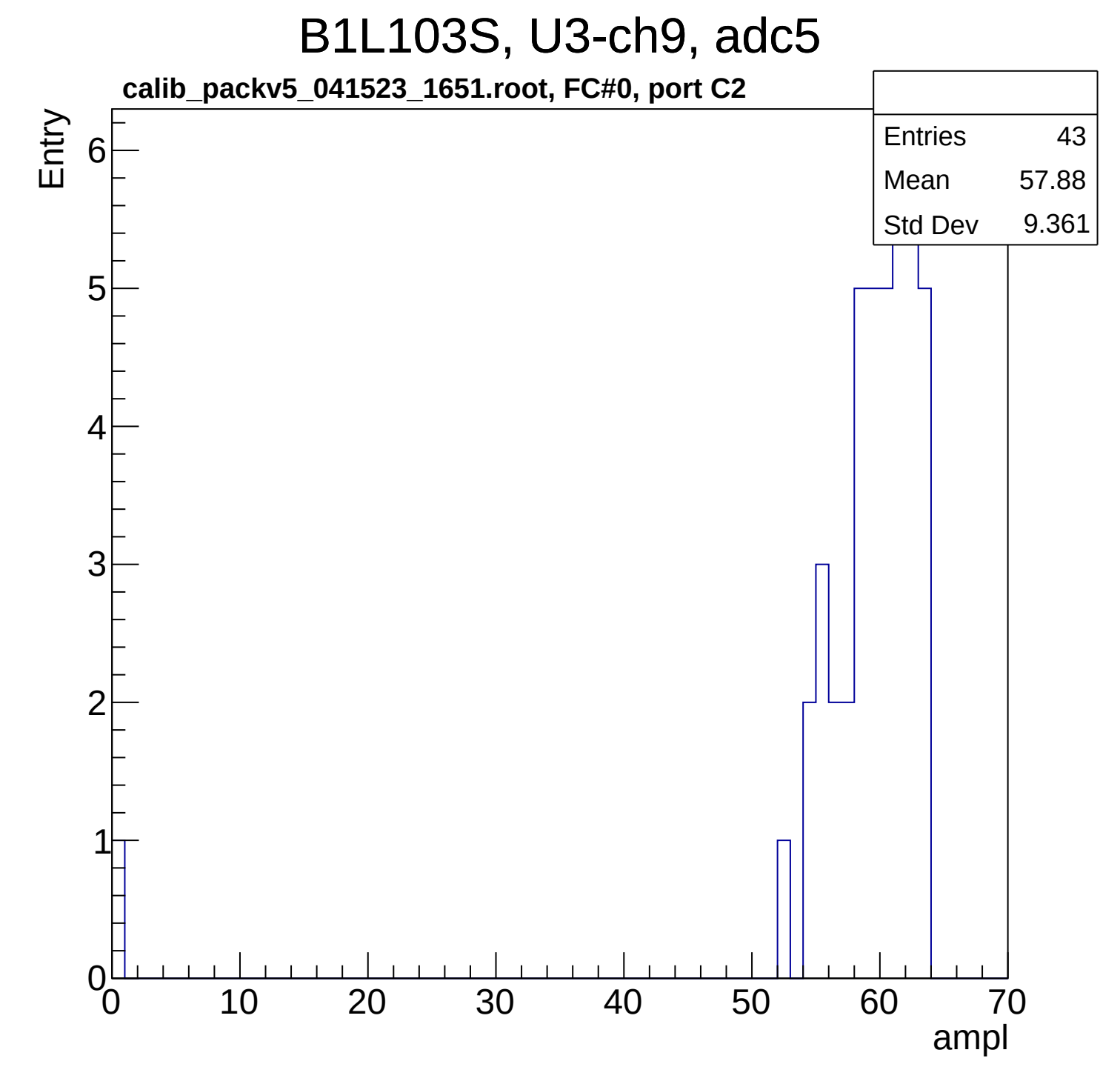

B1L103S, U3-ch9, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 24.69
Std Dev 10.64
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

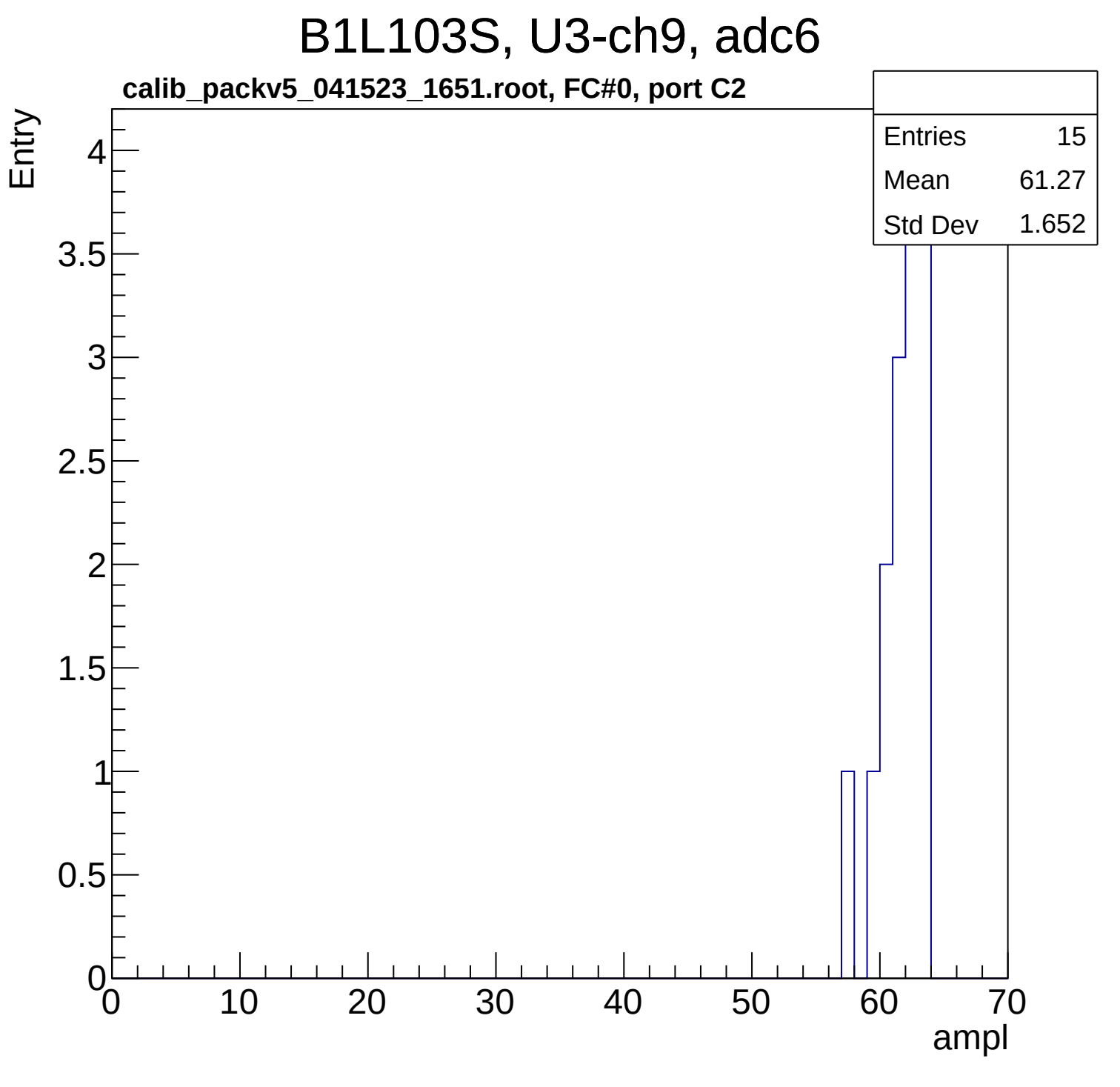

B1L103S, U3-ch9, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 34.46
Std Dev 5.458
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch9, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 35.45
Std Dev 14.97
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch9, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 47.18
Std Dev 8.602
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch9, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 54.8
Std Dev 3.204
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch9, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 57.88
Std Dev 9.361
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U3-ch9, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 61.27
Std Dev 1.652
Entry
ampl
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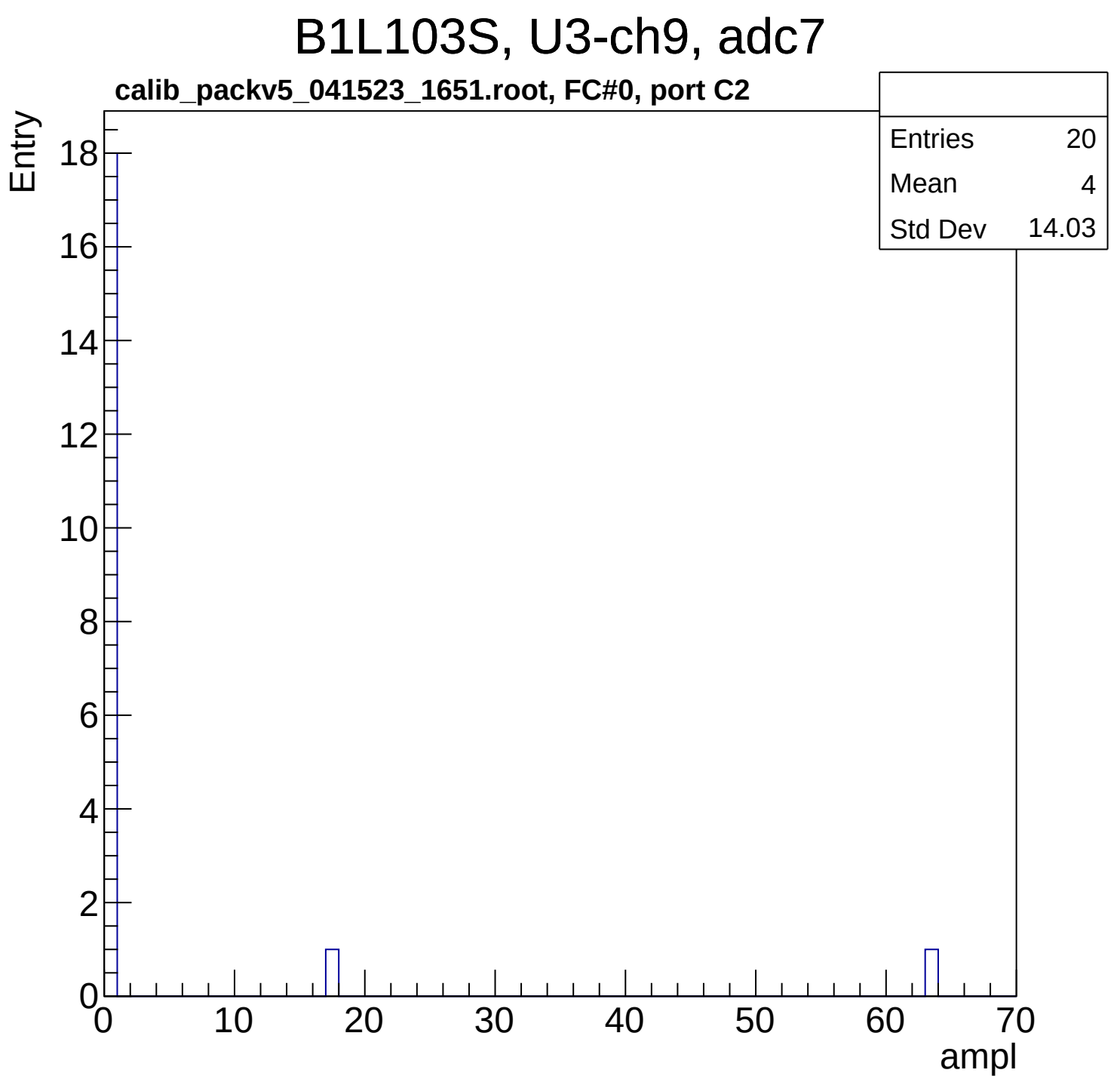
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U3-ch9, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4
Std Dev 14.03
Entry
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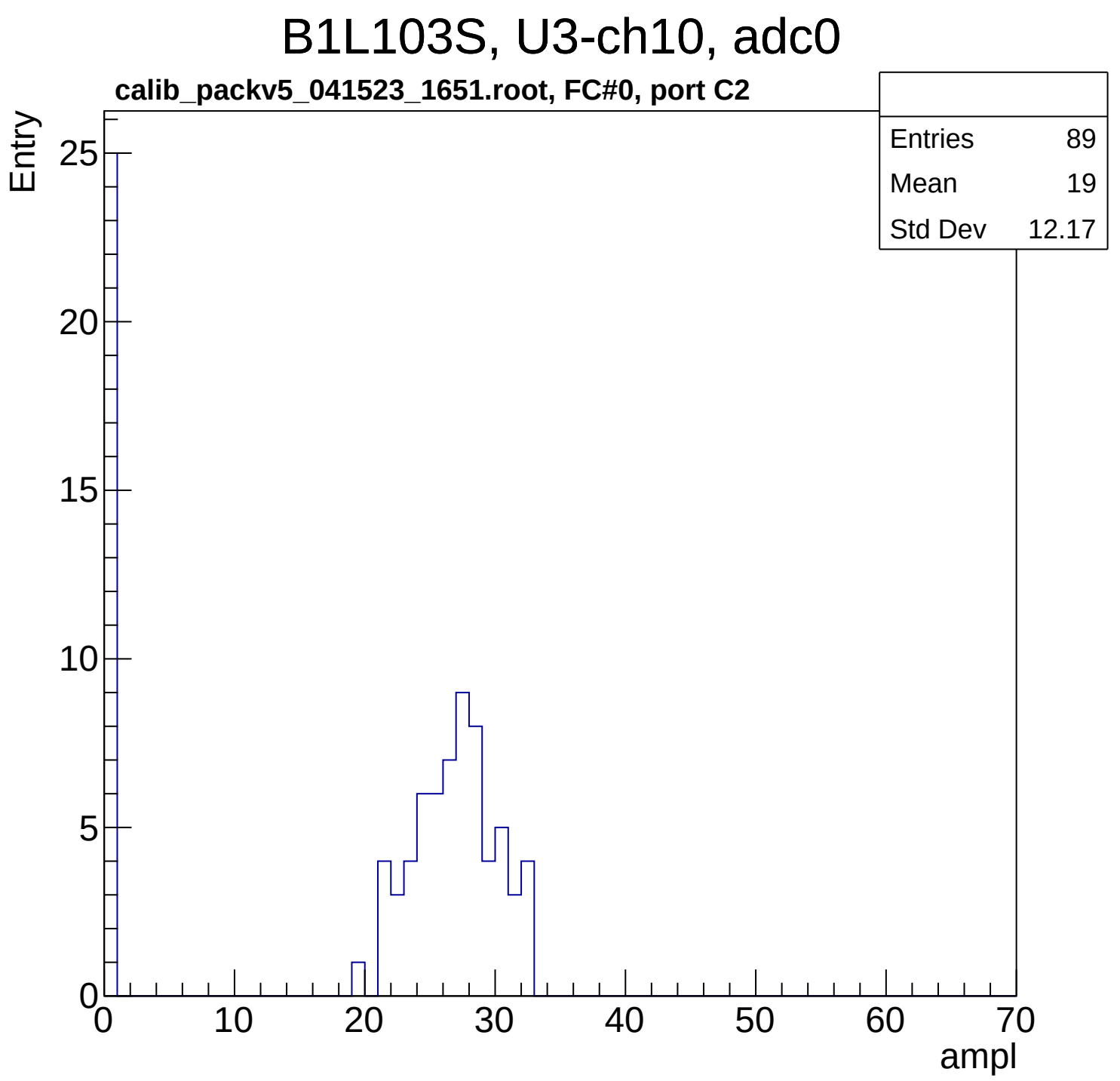
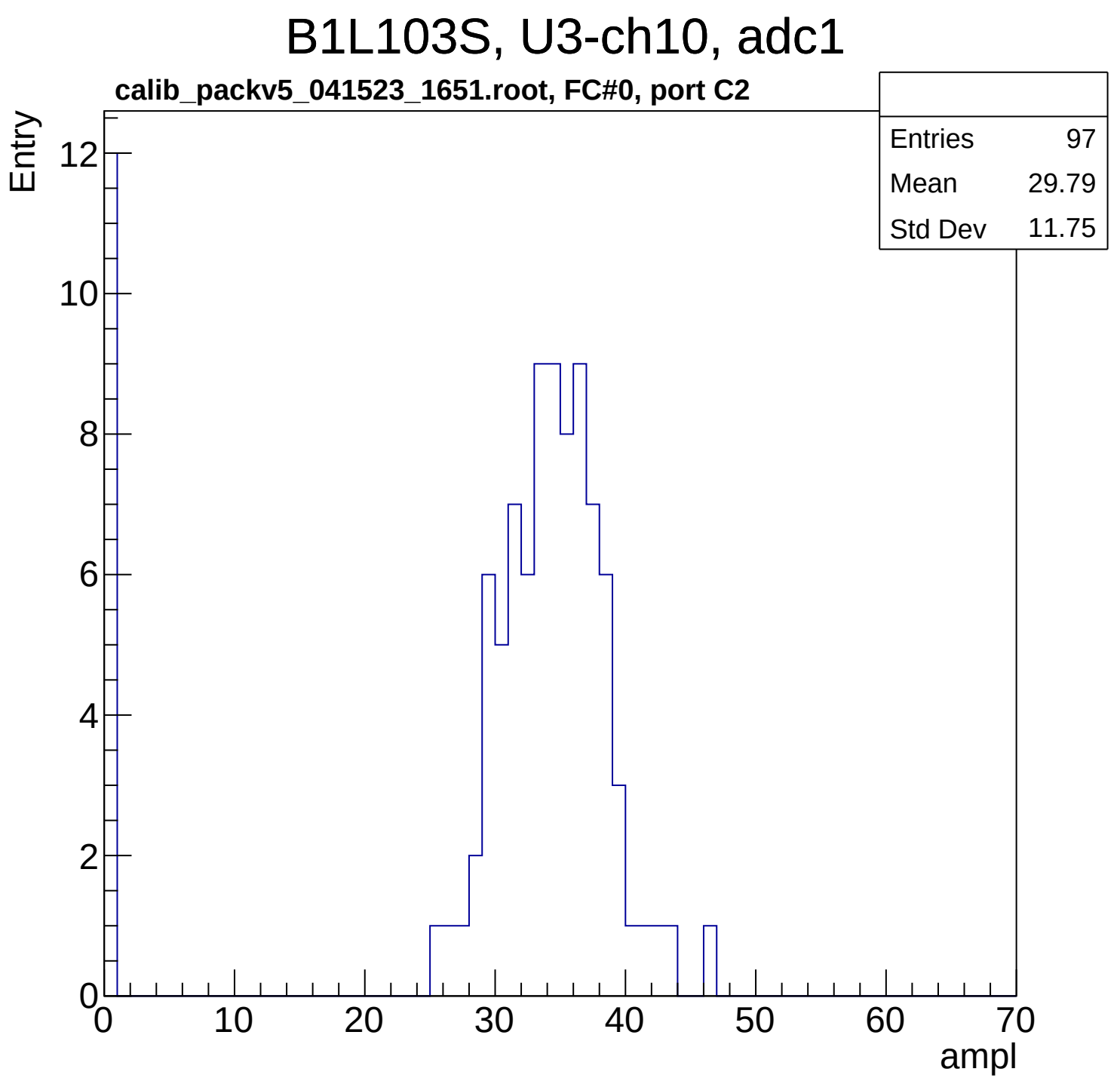
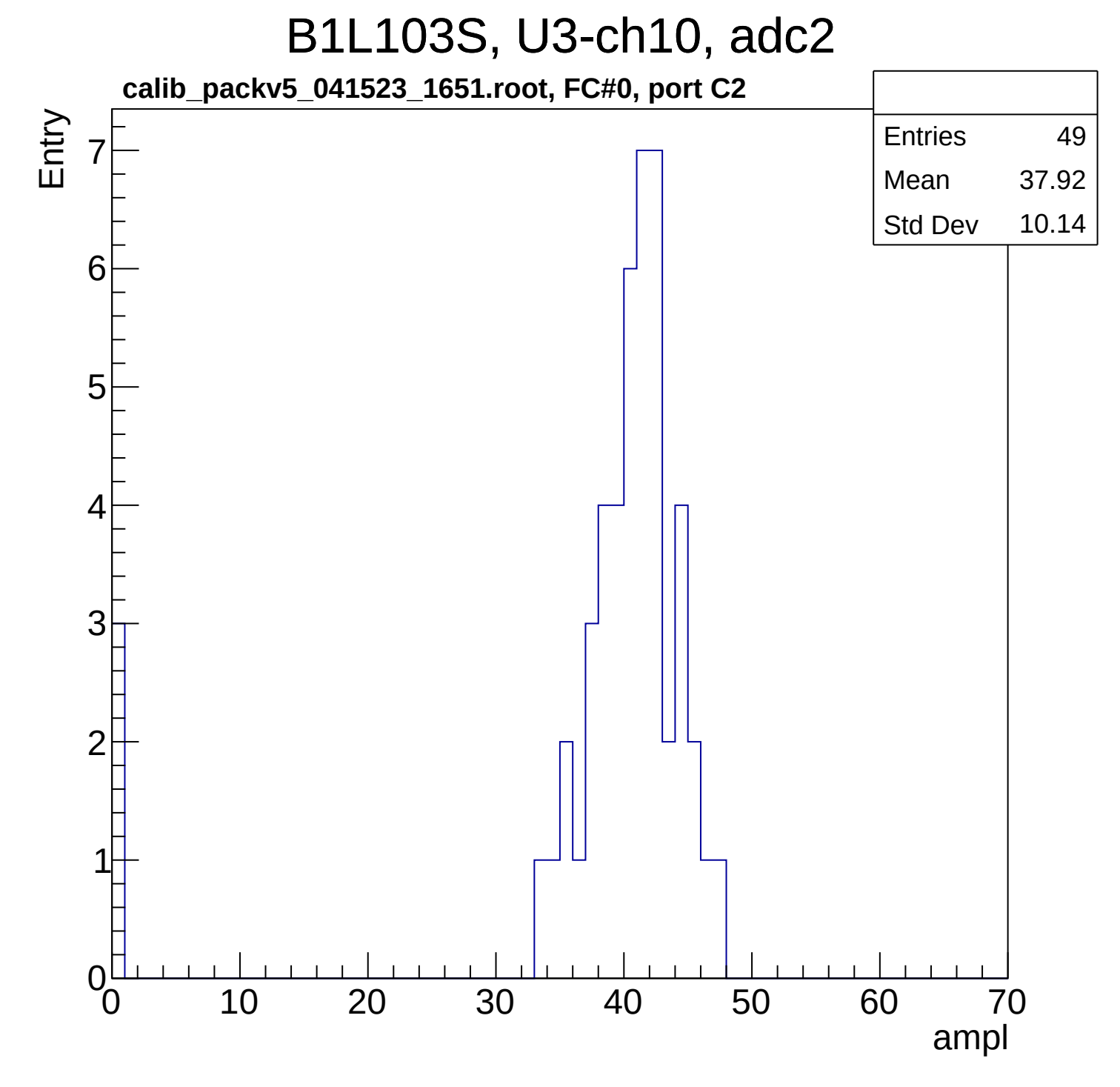
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch10, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 19
Std Dev 12.17
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch10, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 29.79
Std Dev 11.75
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch10, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 37.92
Std Dev 10.14
Entry
ampl
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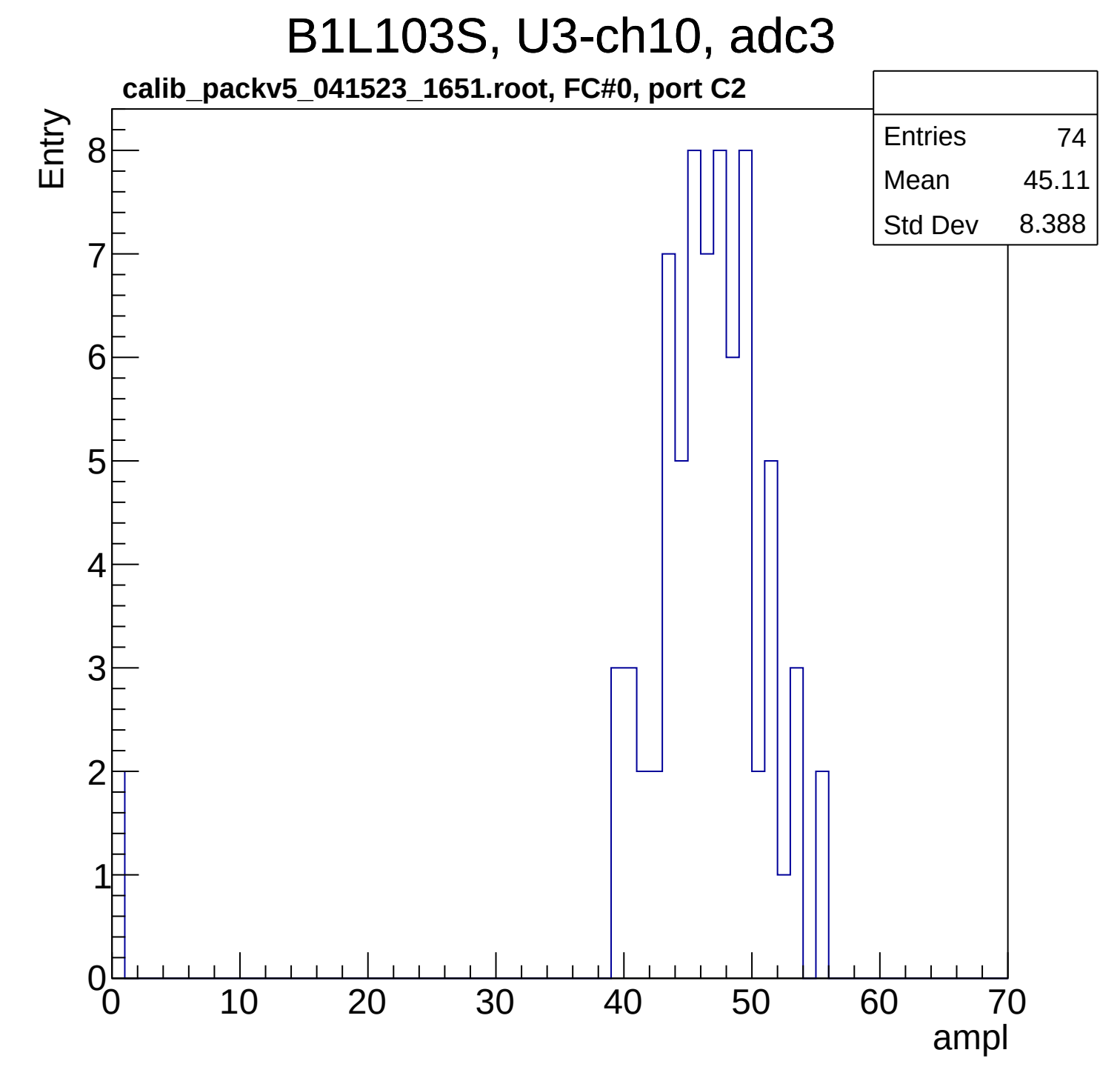
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch10, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 45.11
Std Dev 8.388
Entry
ampl
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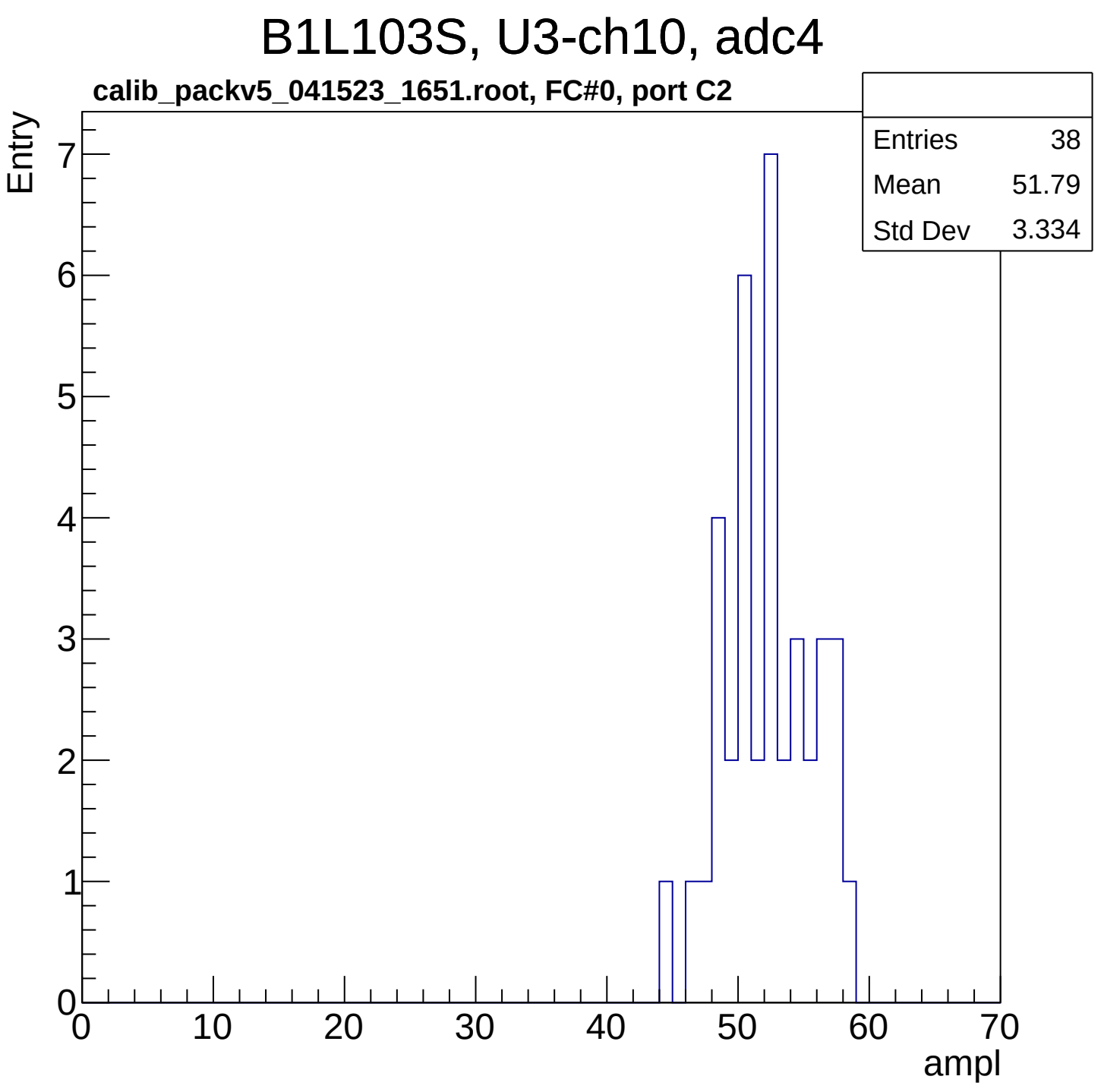
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch10, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 51.79
Std Dev 3.334
Entry
ampl
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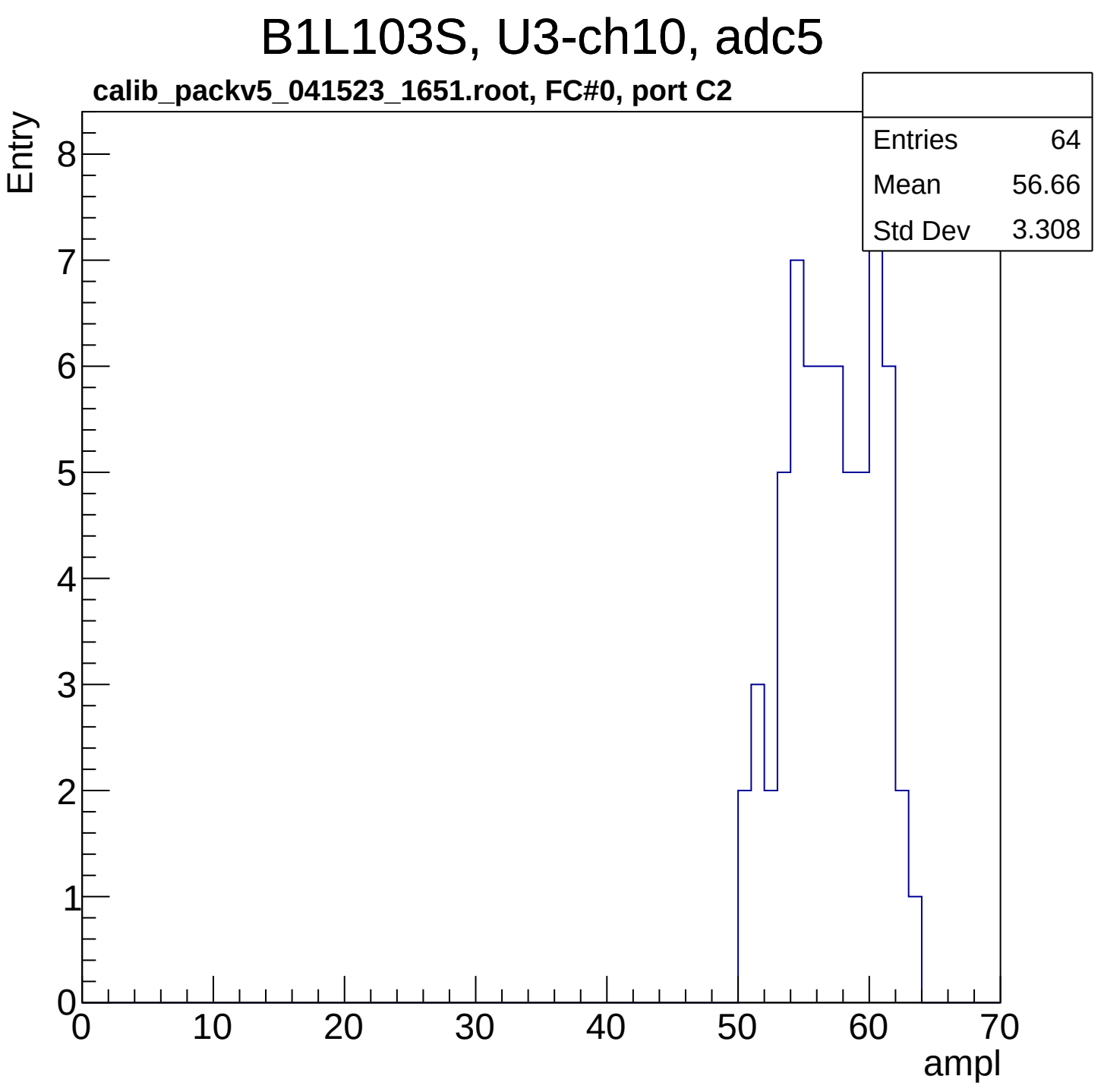
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch10, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 56.66
Std Dev 3.308
Entry
ampl
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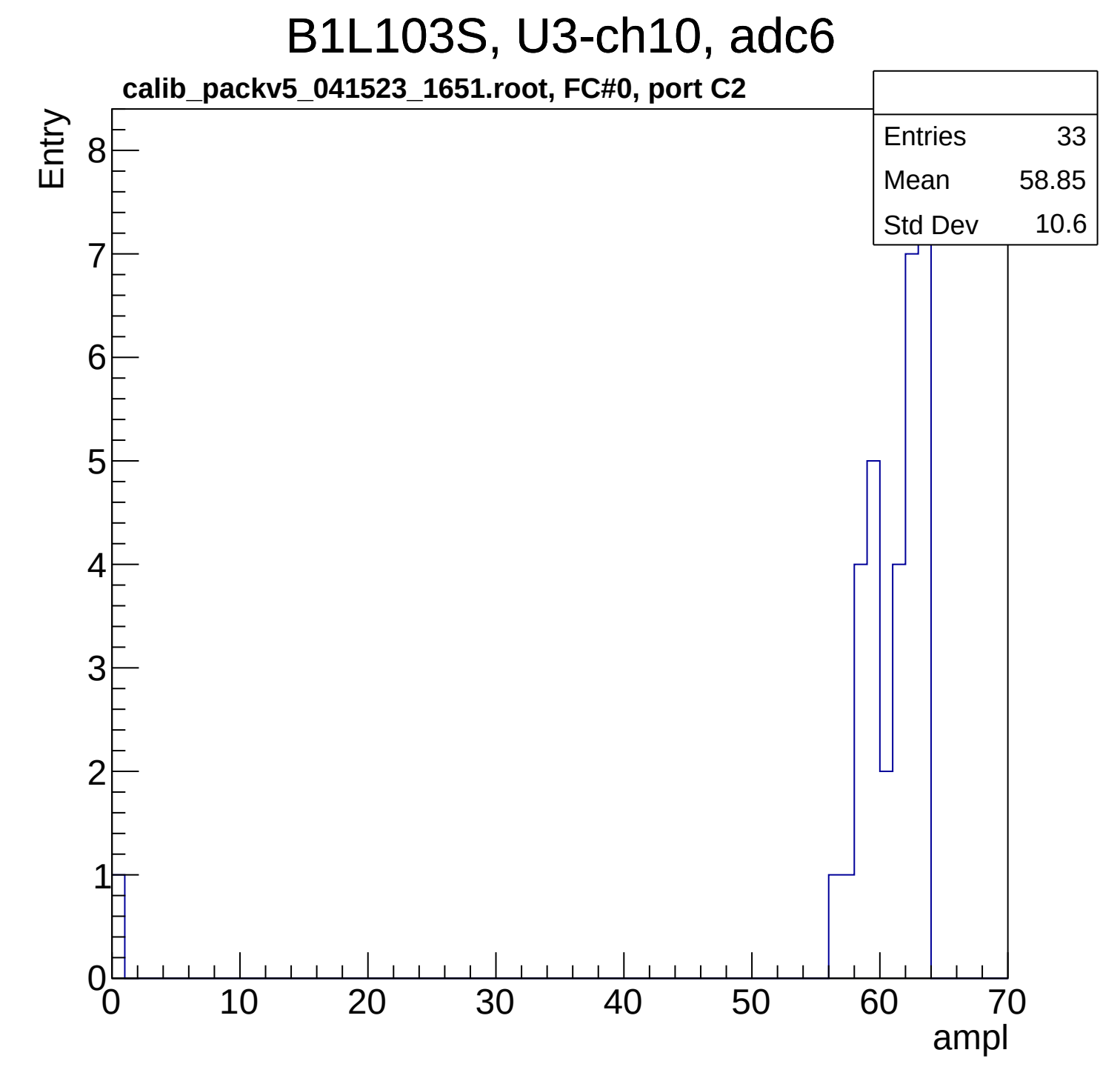
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch10, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 58.85
Std Dev 10.6
Entry
ampl
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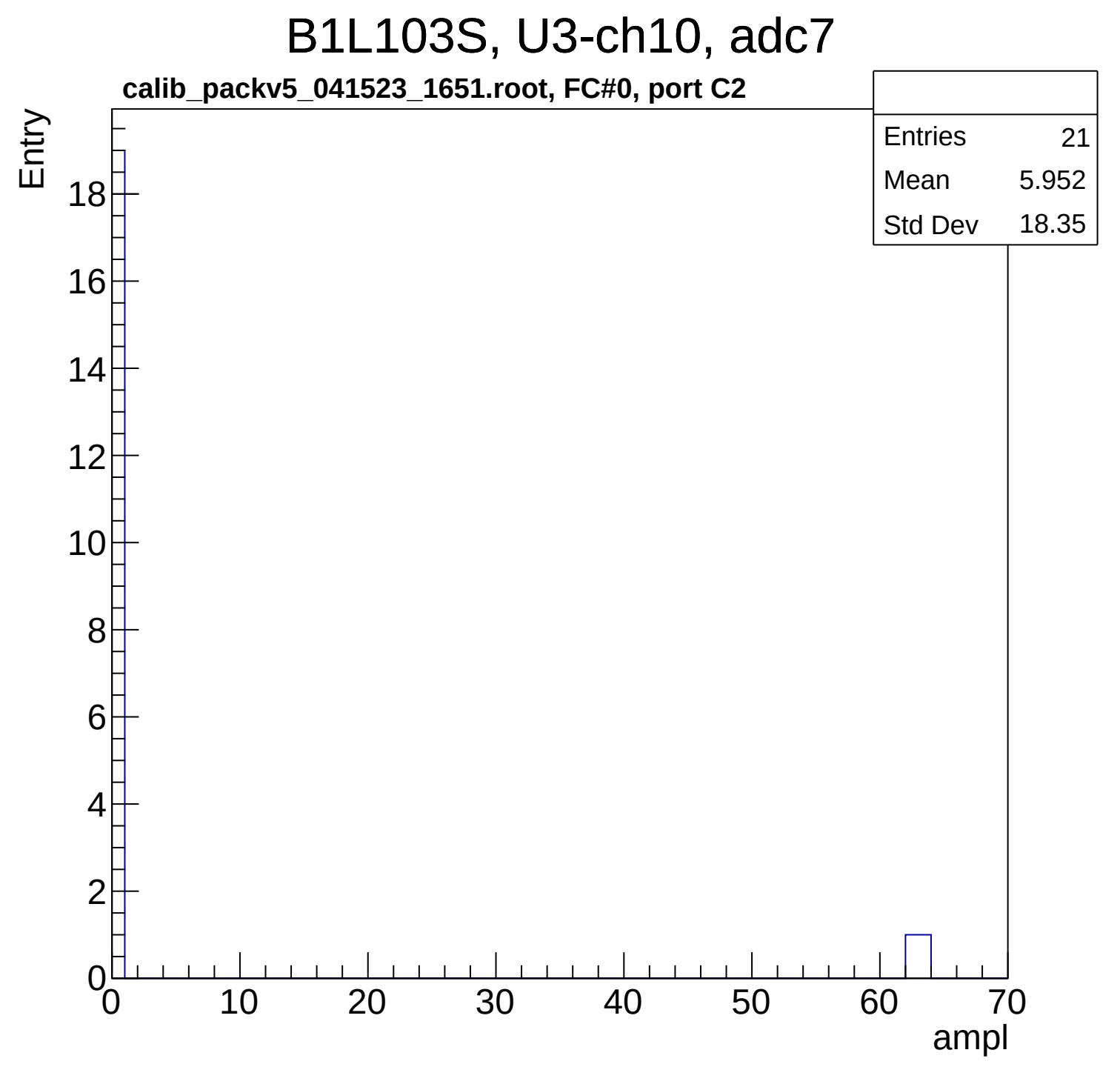
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch10, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.952
Std Dev 18.35
Entry
0
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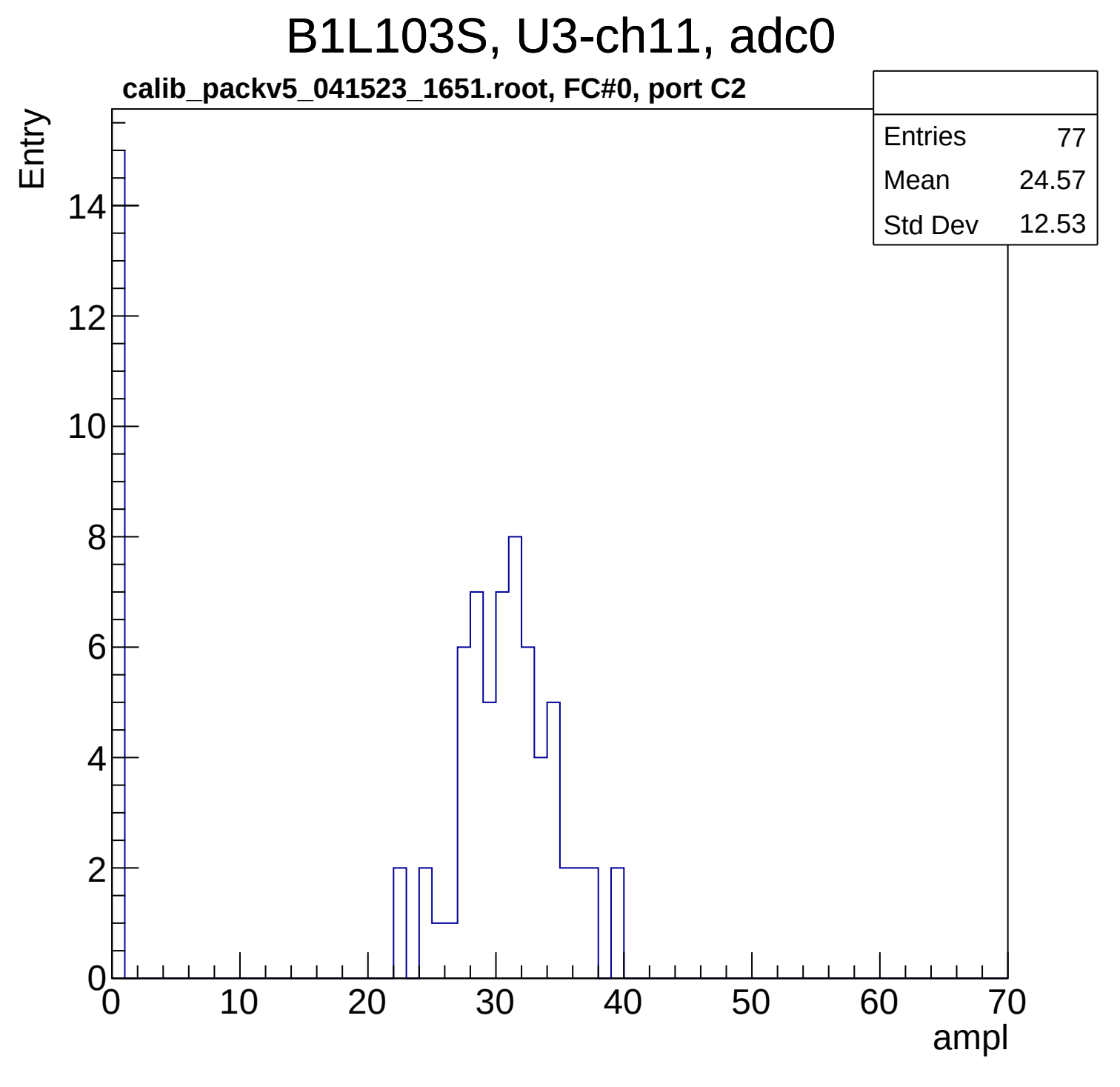
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch11, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 24.57
Std Dev 12.53
Entry
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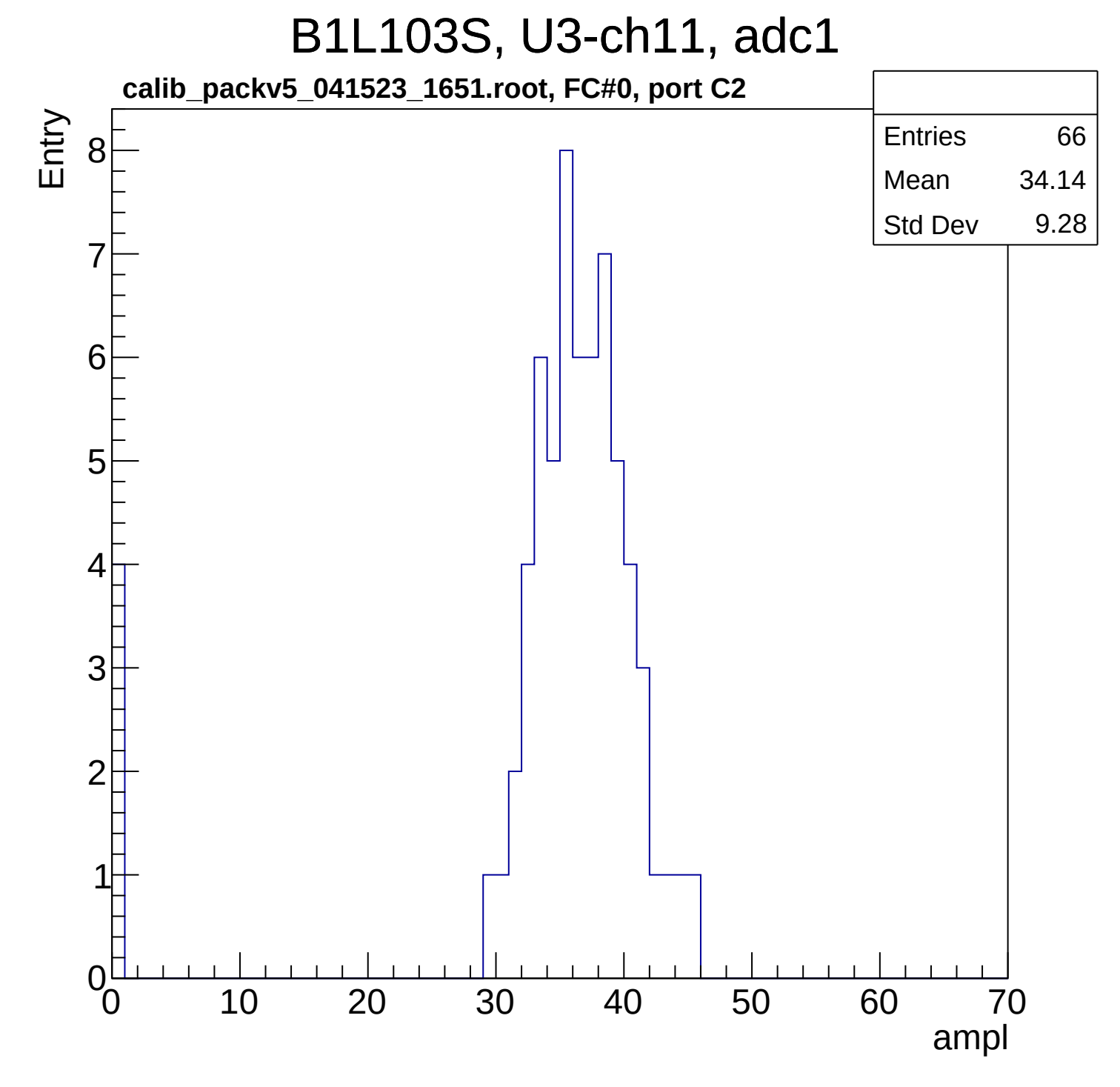
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch11, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 34.14
Std Dev 9.28
Entry
ampl
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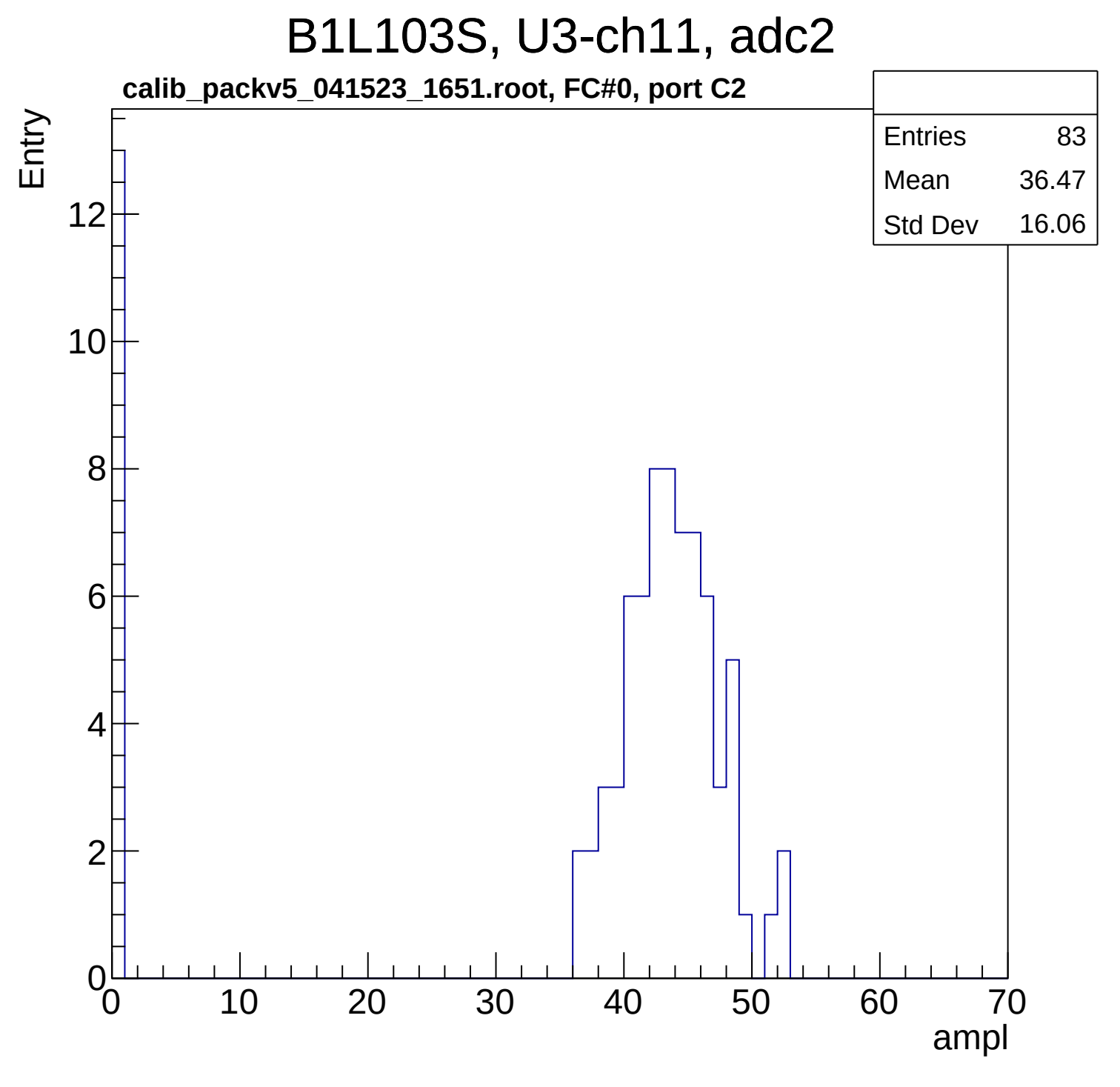
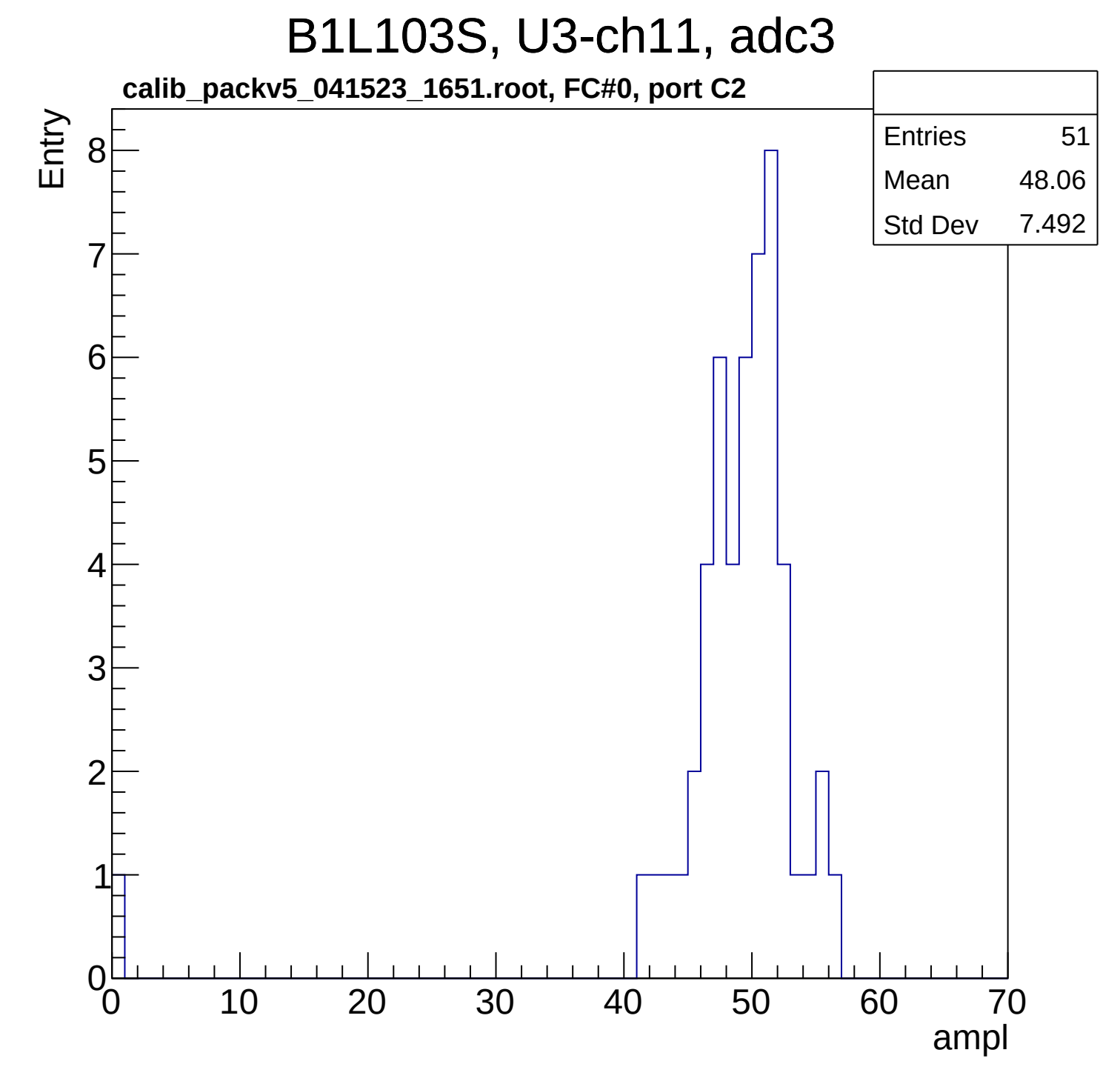
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch11, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 36.47
Std Dev 16.06
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch11, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 48.06
Std Dev 7.492
Entry
ampl
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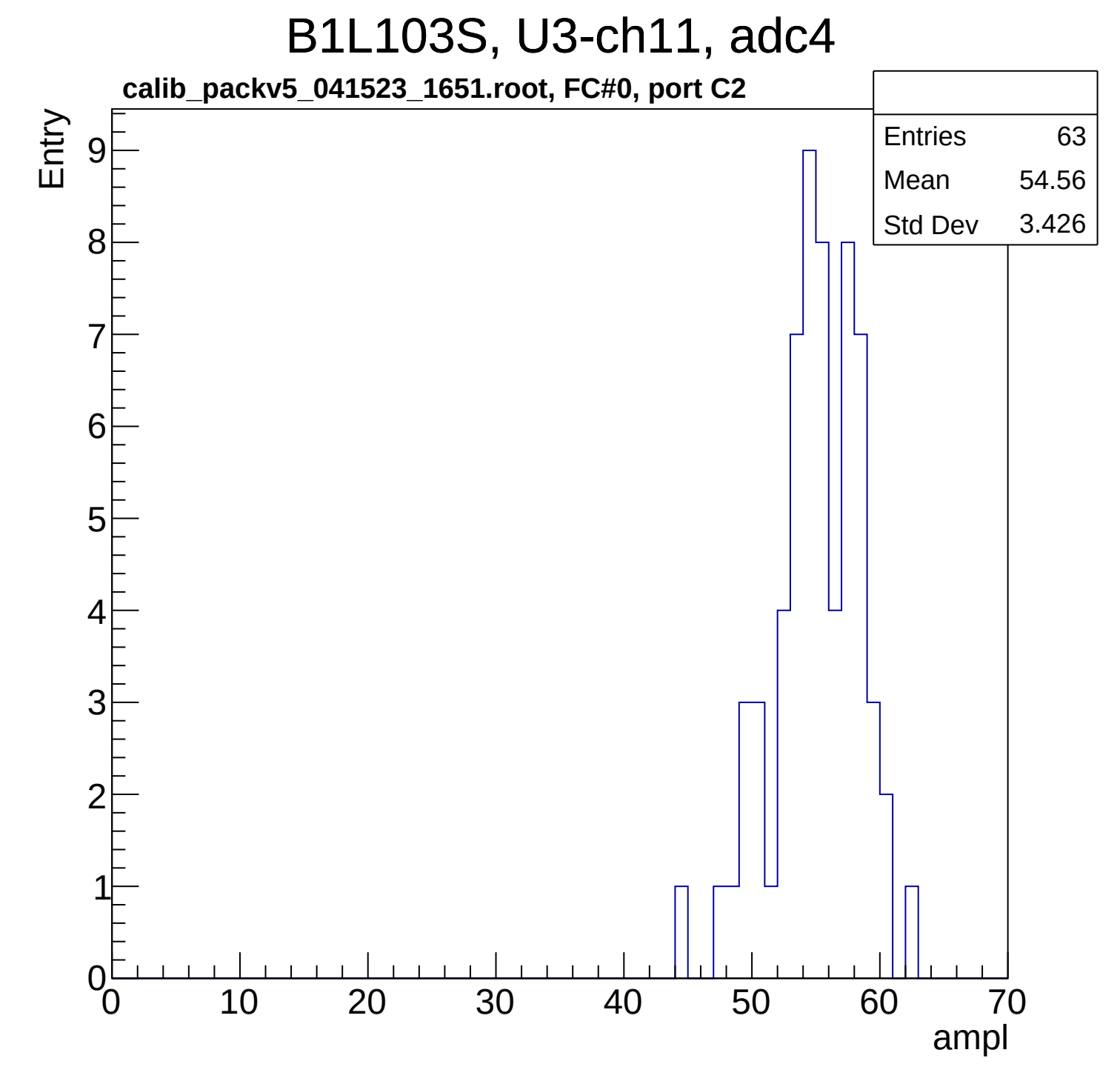
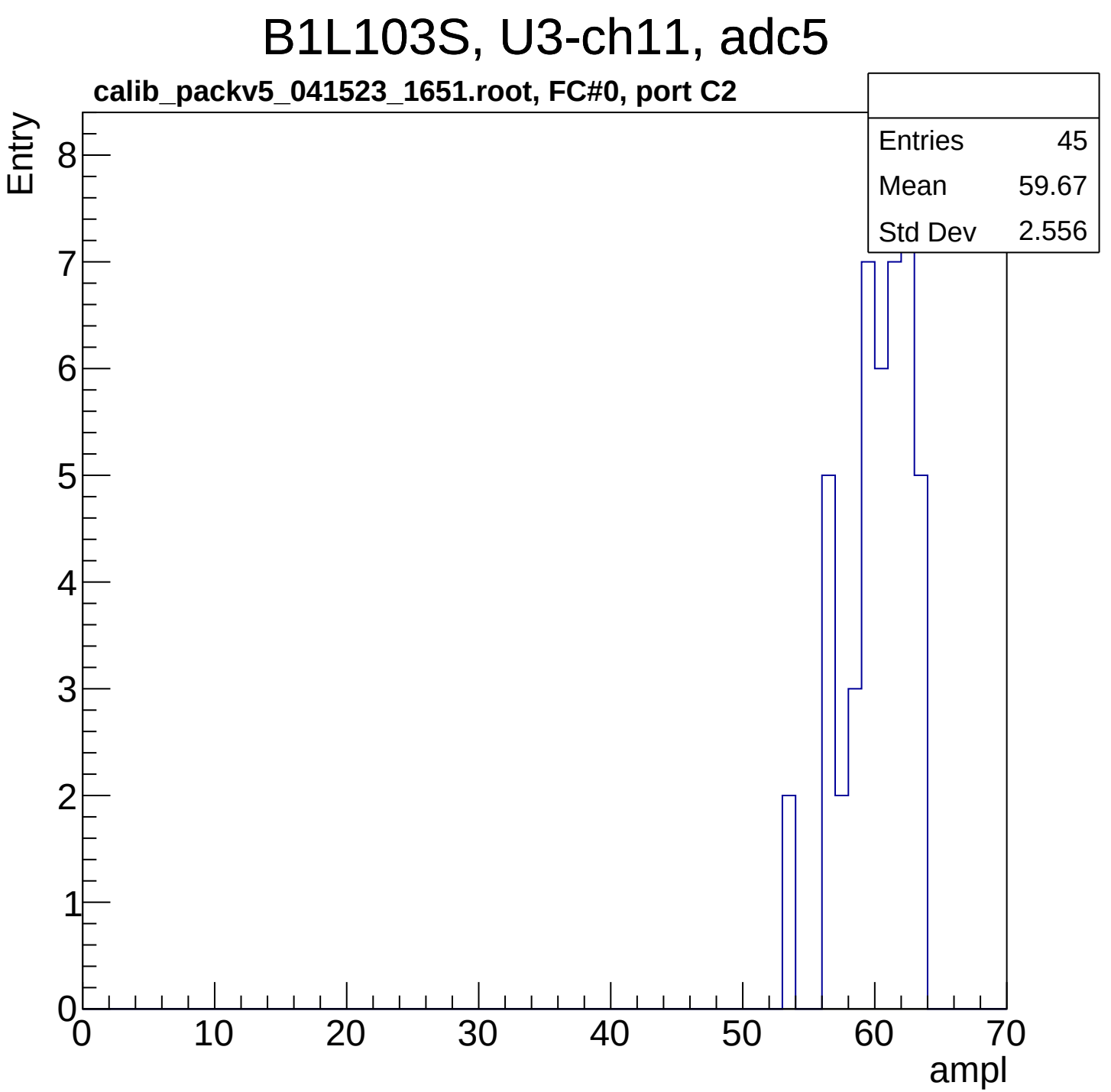
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch11, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 54.56
Std Dev 3.426
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch11, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 59.67
Std Dev 2.556
Entry
ampl
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2
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4
5
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7
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0
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60
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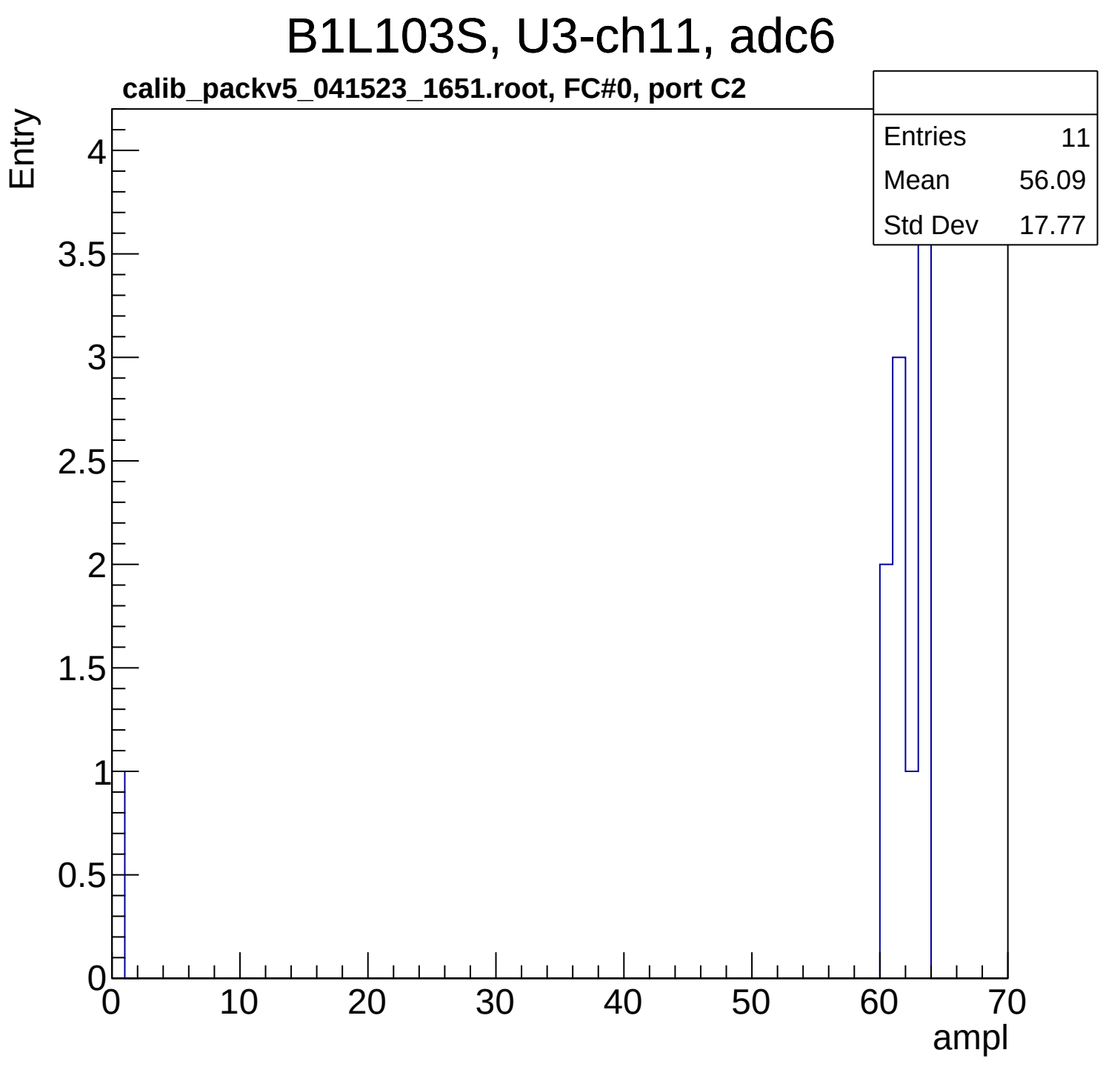
B1L103S, U3-ch11, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 56.09
Std Dev 17.77
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
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60
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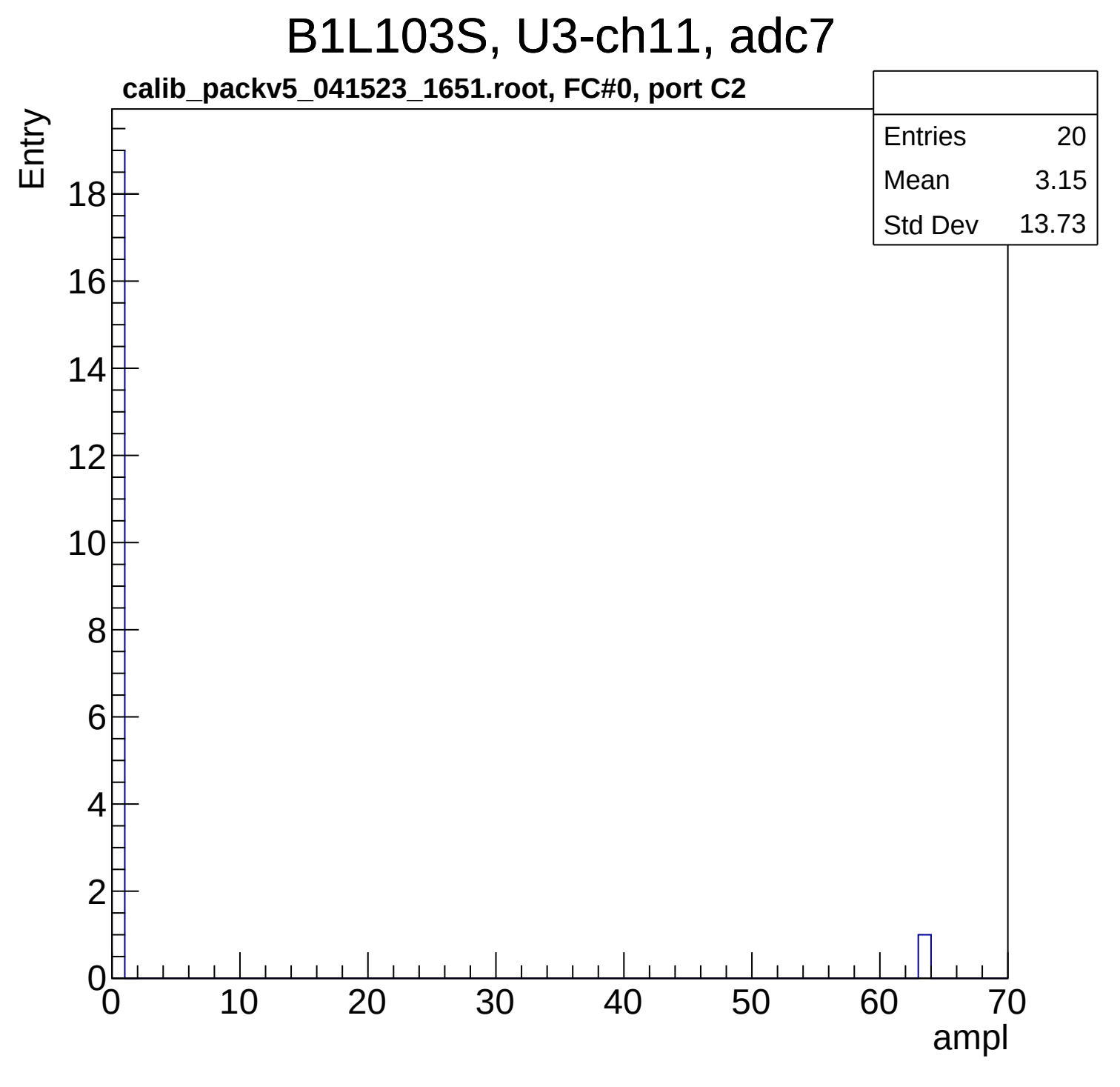
B1L103S, U3-ch11, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
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6
8
10
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18
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10
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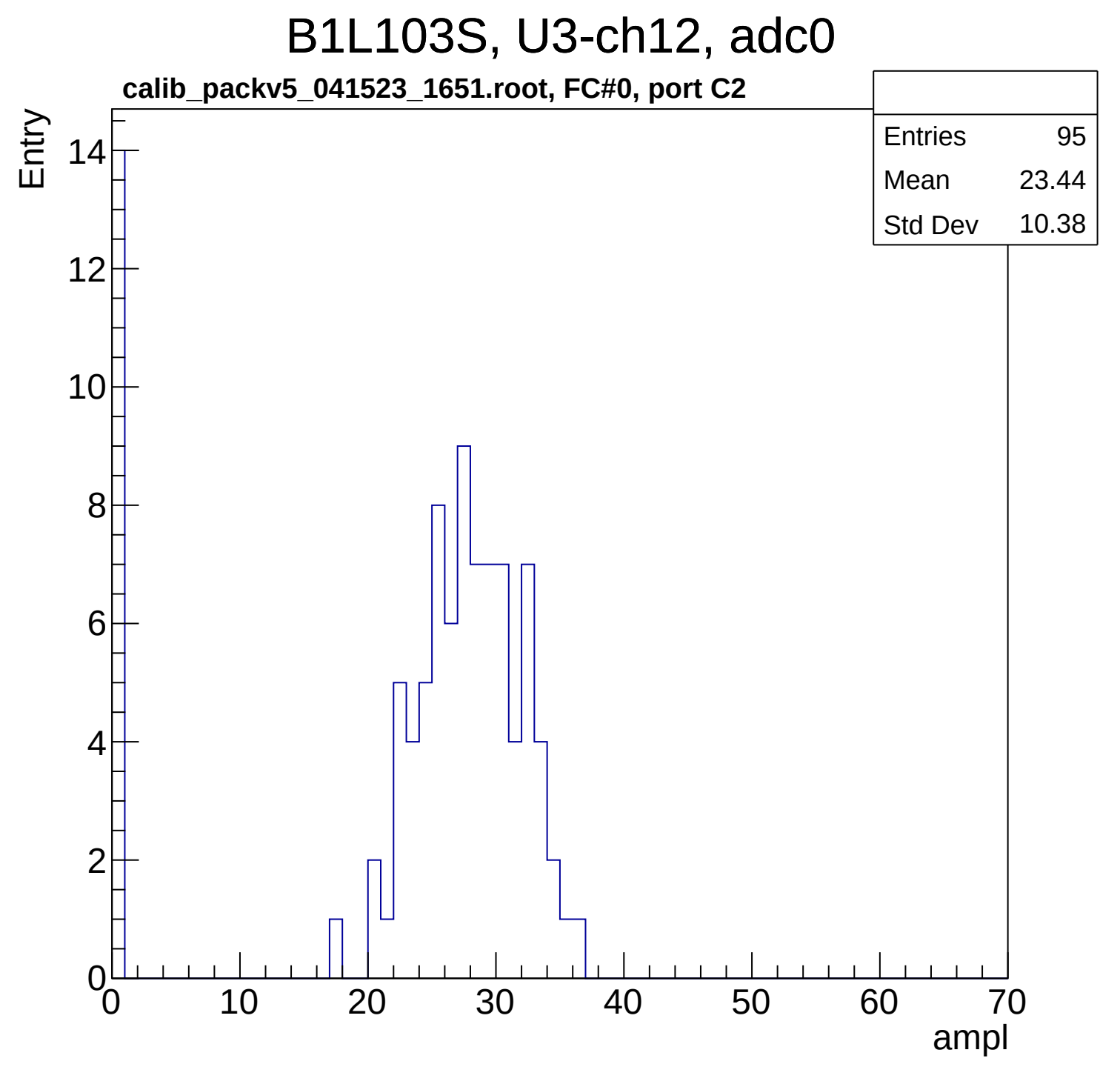
70
ampl


B1L103S, U3-ch12, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 23.44
Std Dev 10.38
Entry
ampl
0
2
4
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0
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60
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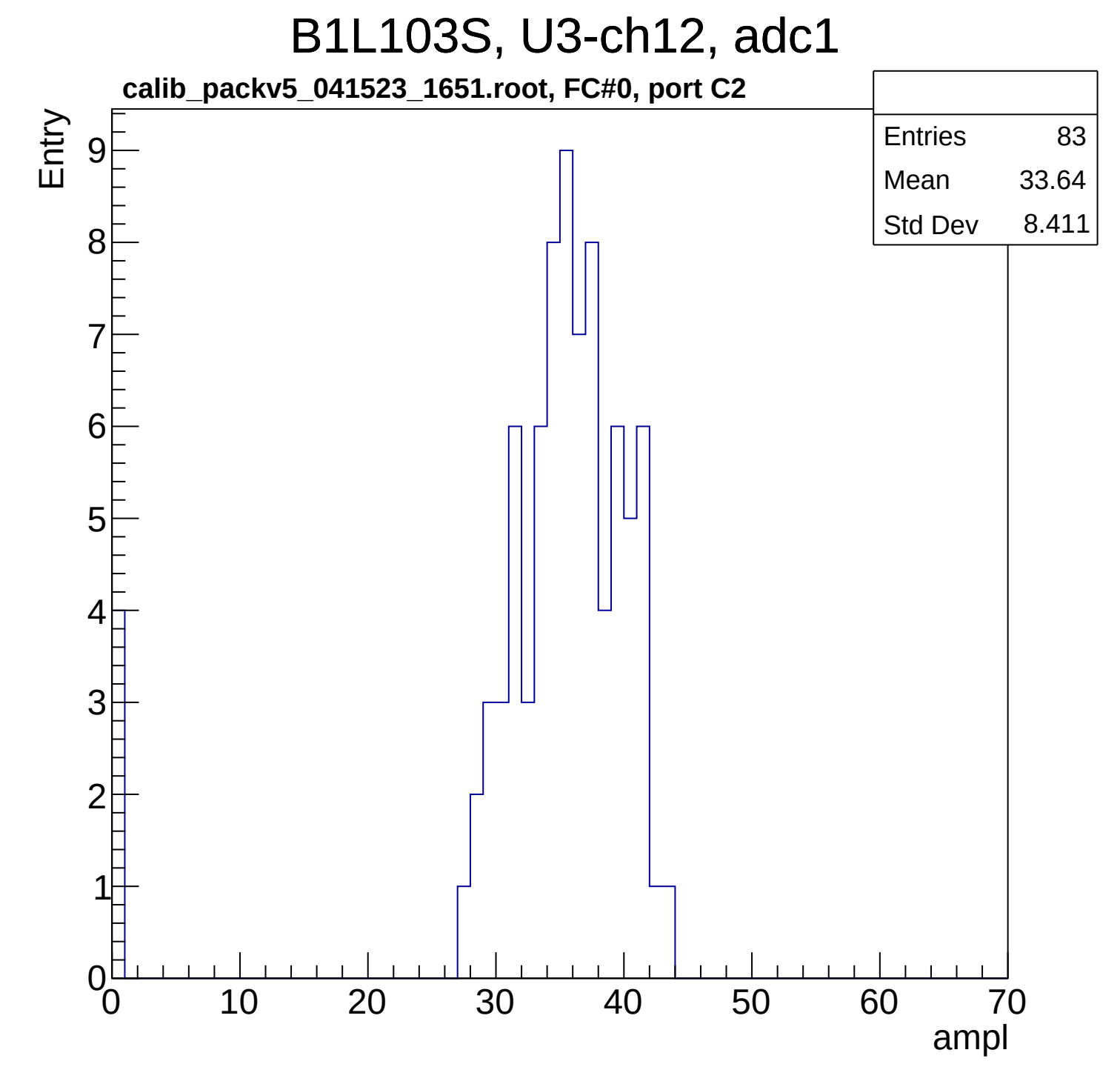
B1L103S, U3-ch12, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 33.64
Std Dev 8.411
Entry
ampl
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2
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4
5
6
7
8
9
0
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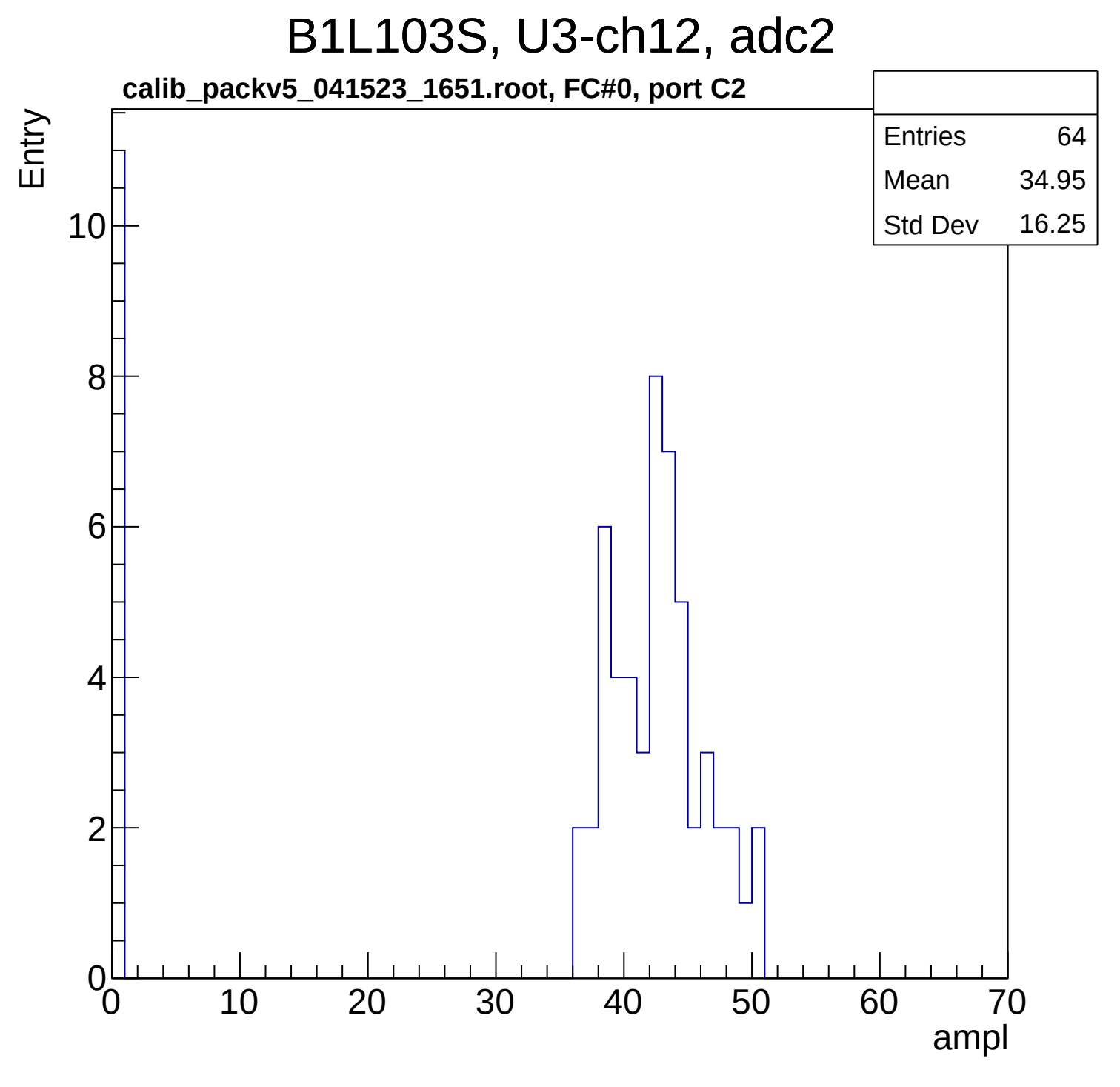
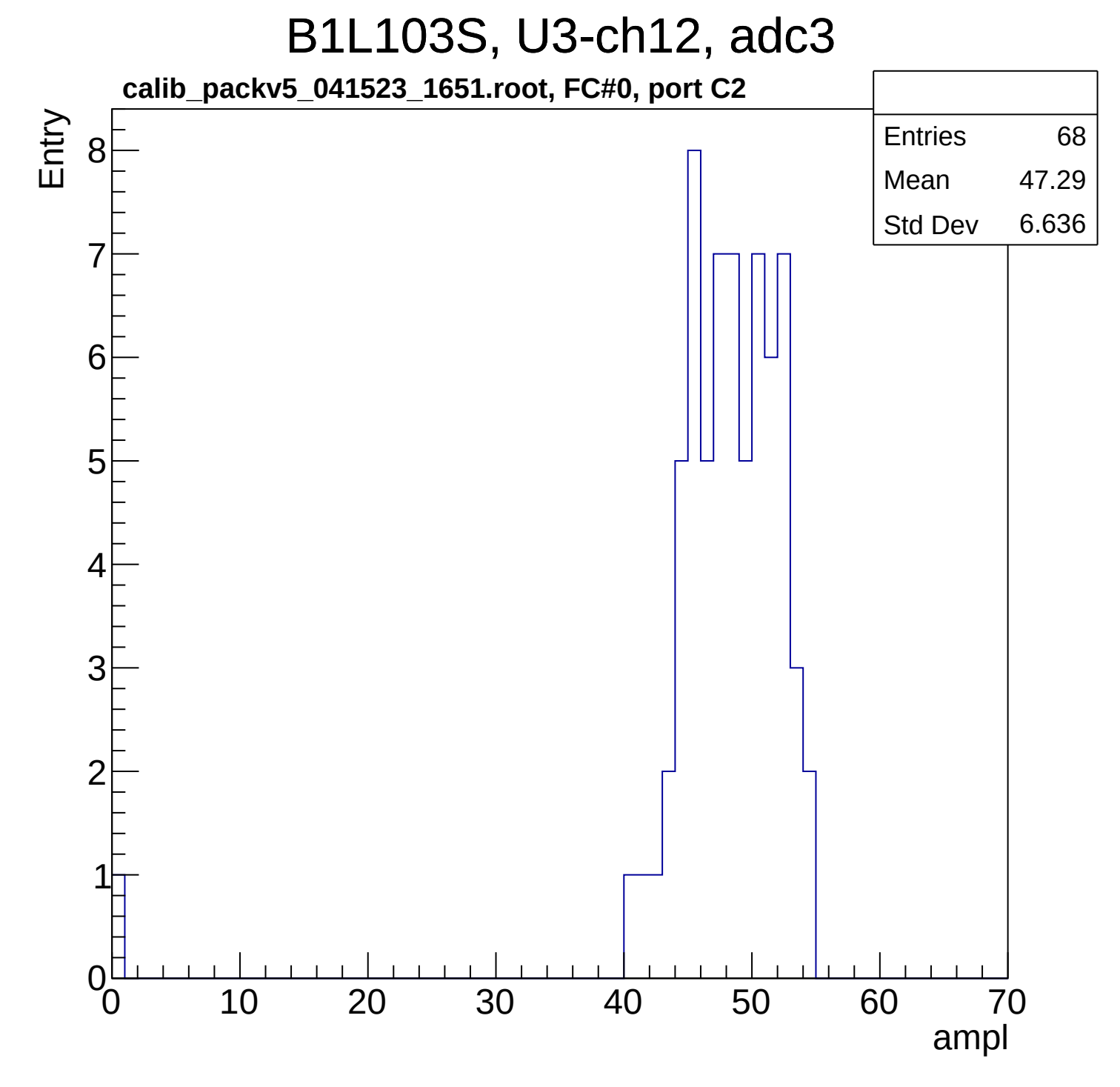

B1L103S, U3-ch12, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 34.95
Std Dev 16.25
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch12, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 47.29
Std Dev 6.636
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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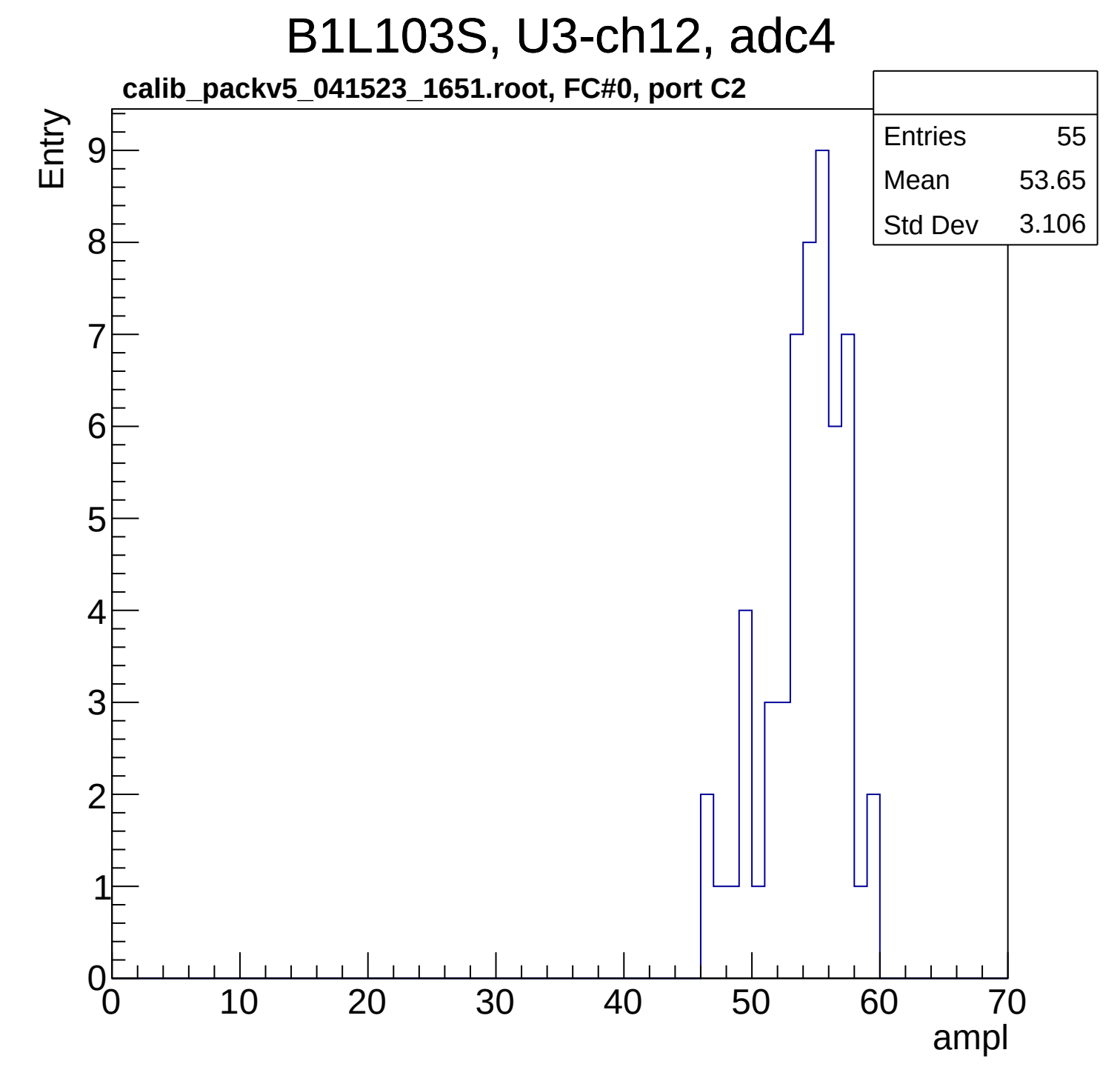
B1L103S, U3-ch12, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 53.65
Std Dev 3.106
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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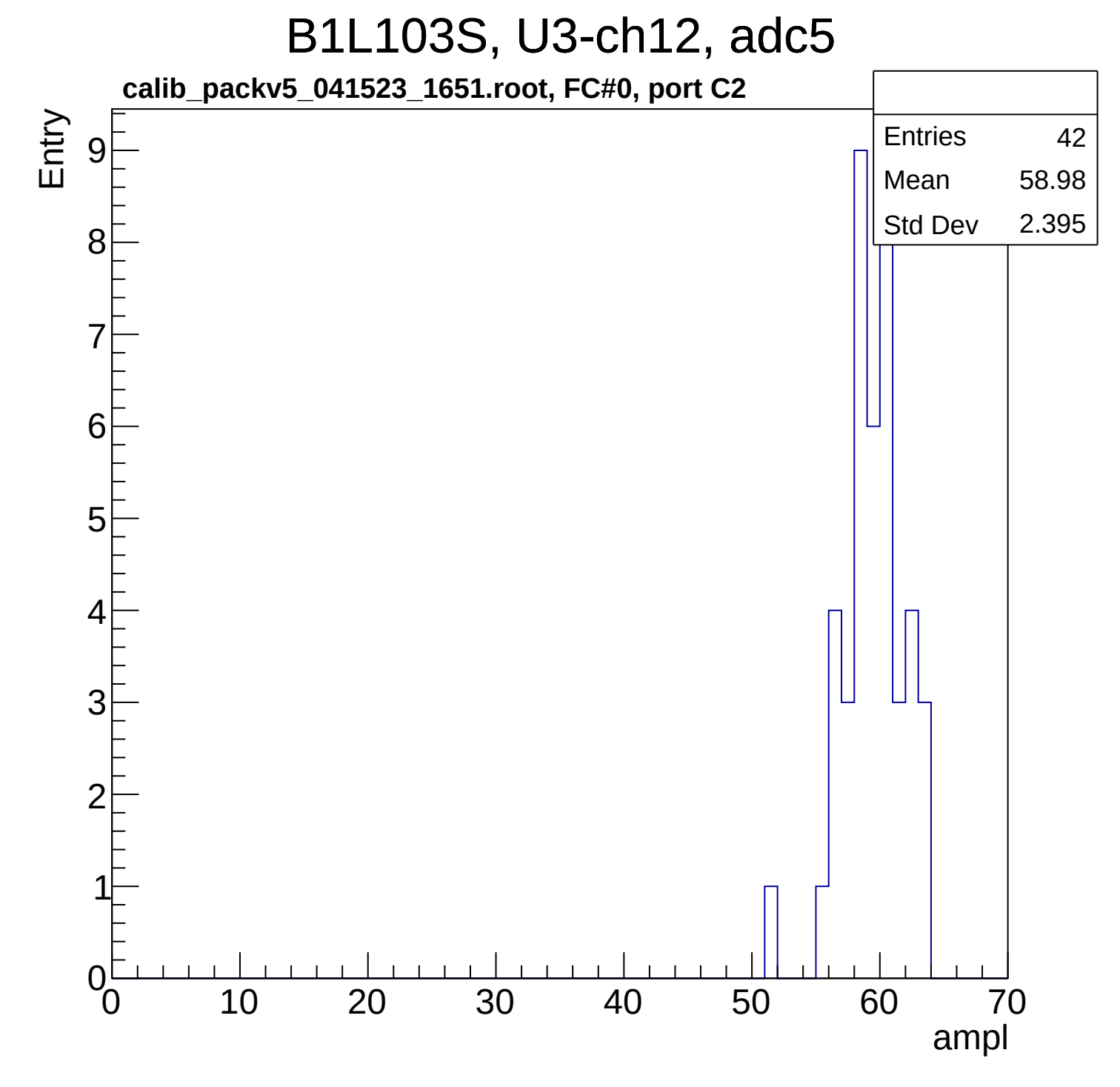
B1L103S, U3-ch12, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 58.98
Std Dev 2.395
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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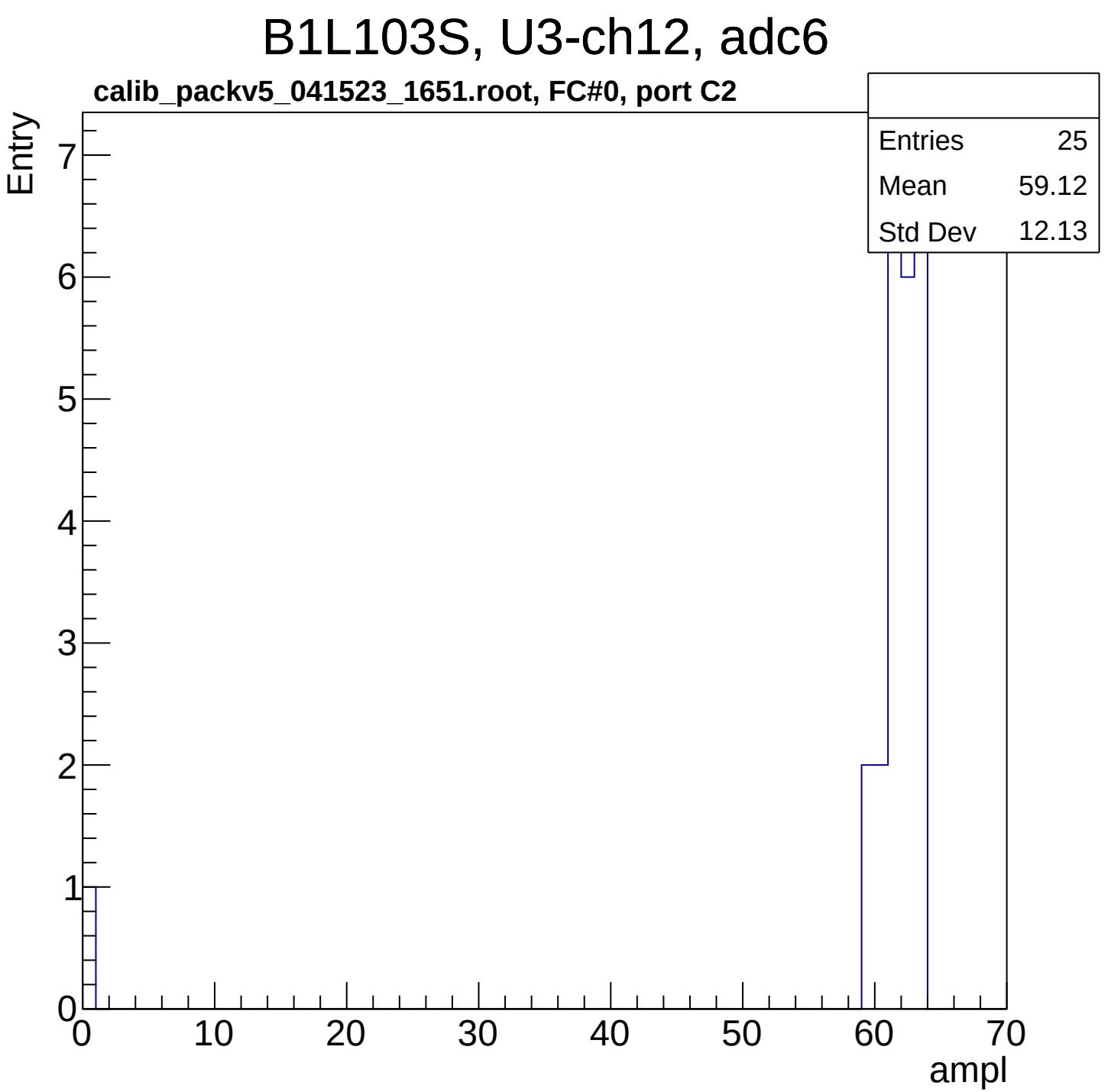
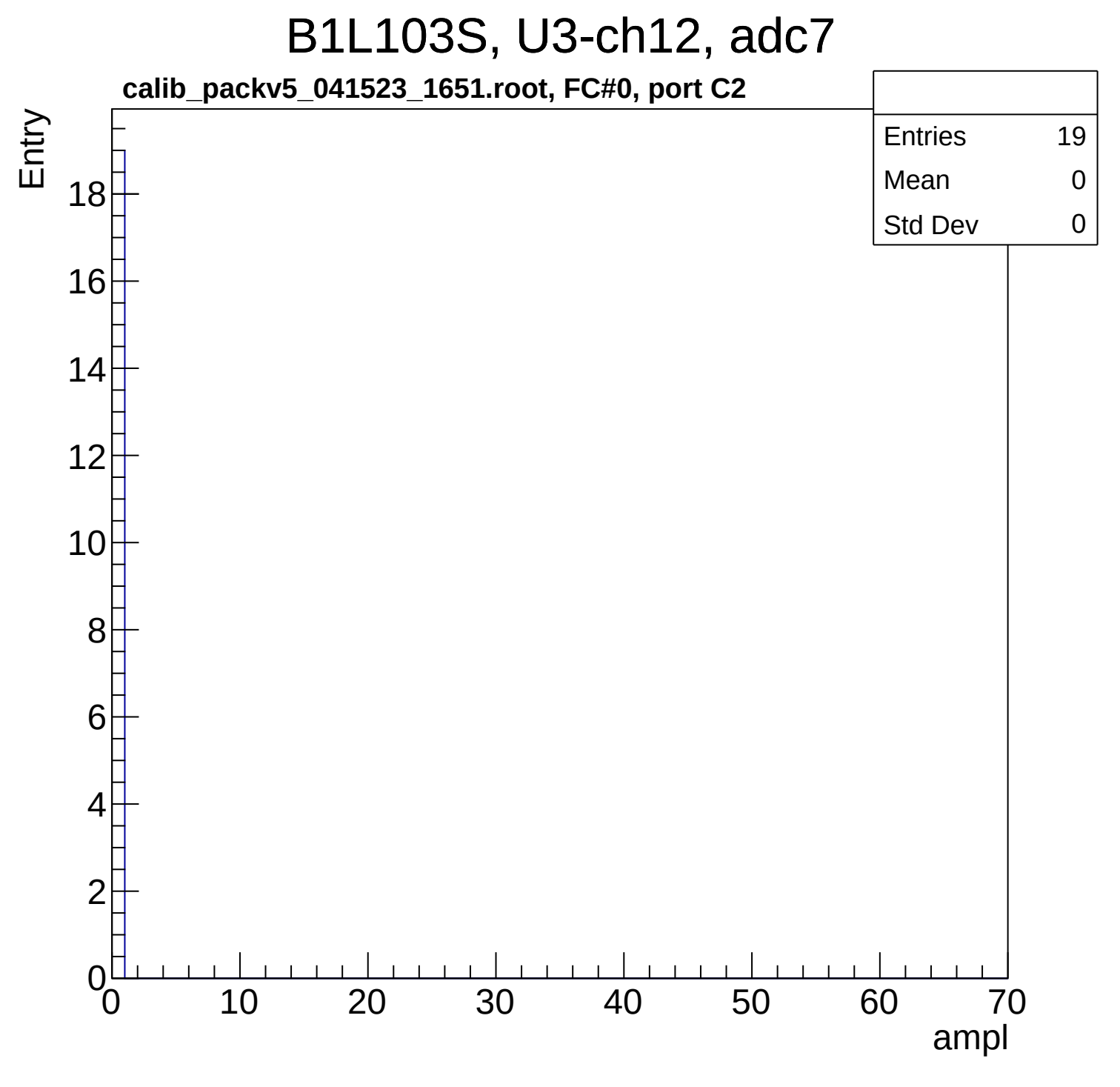
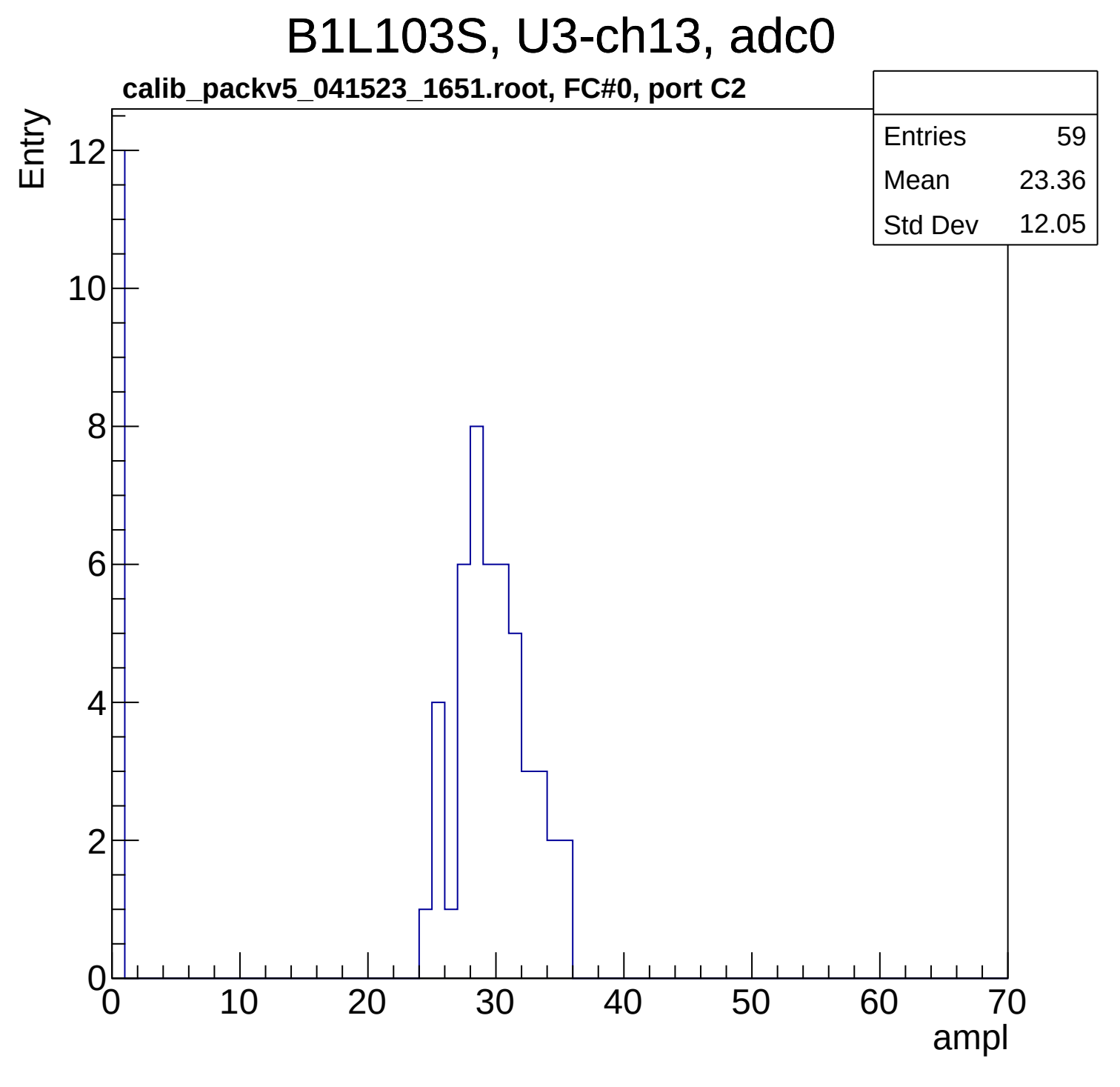
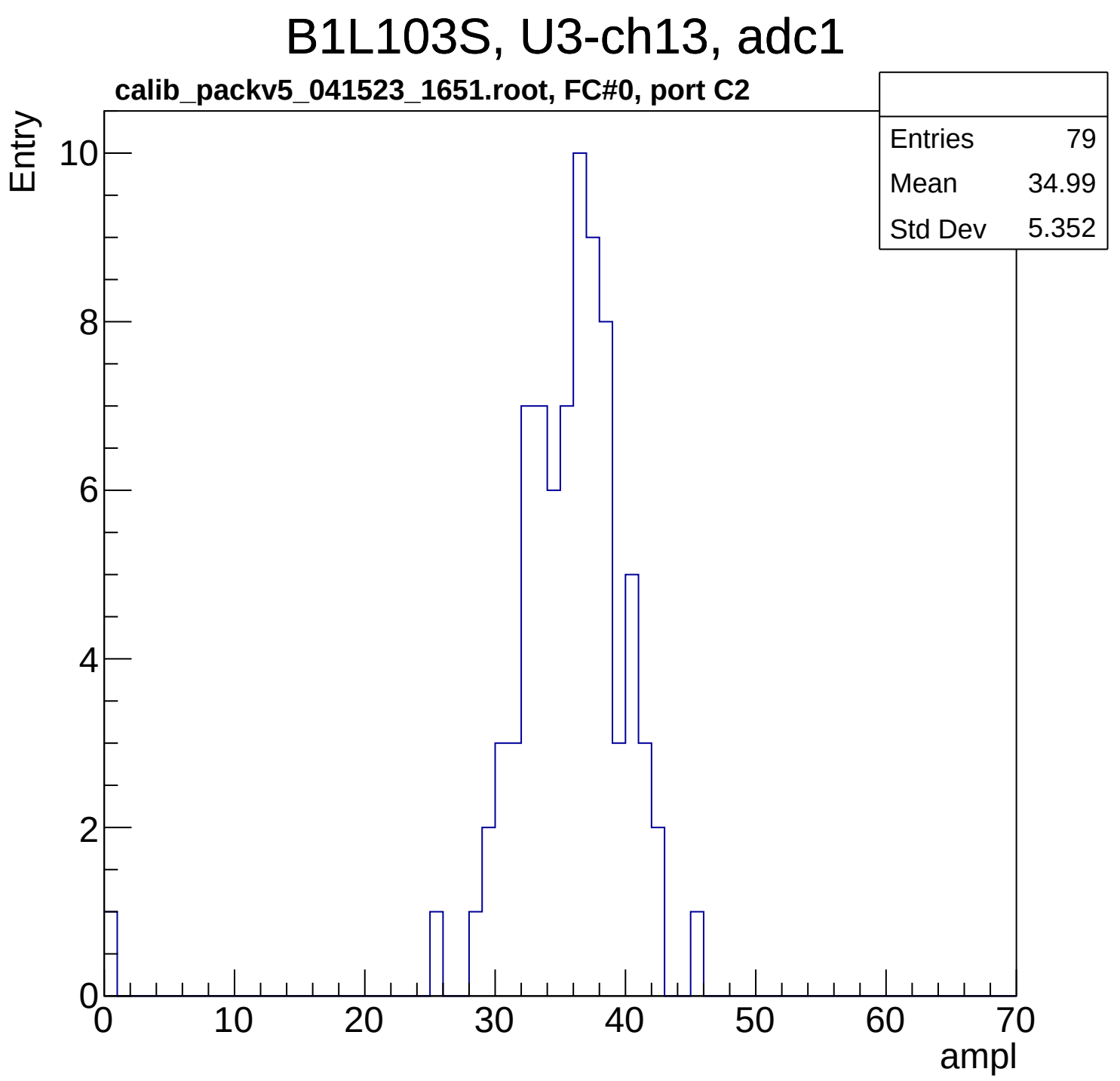
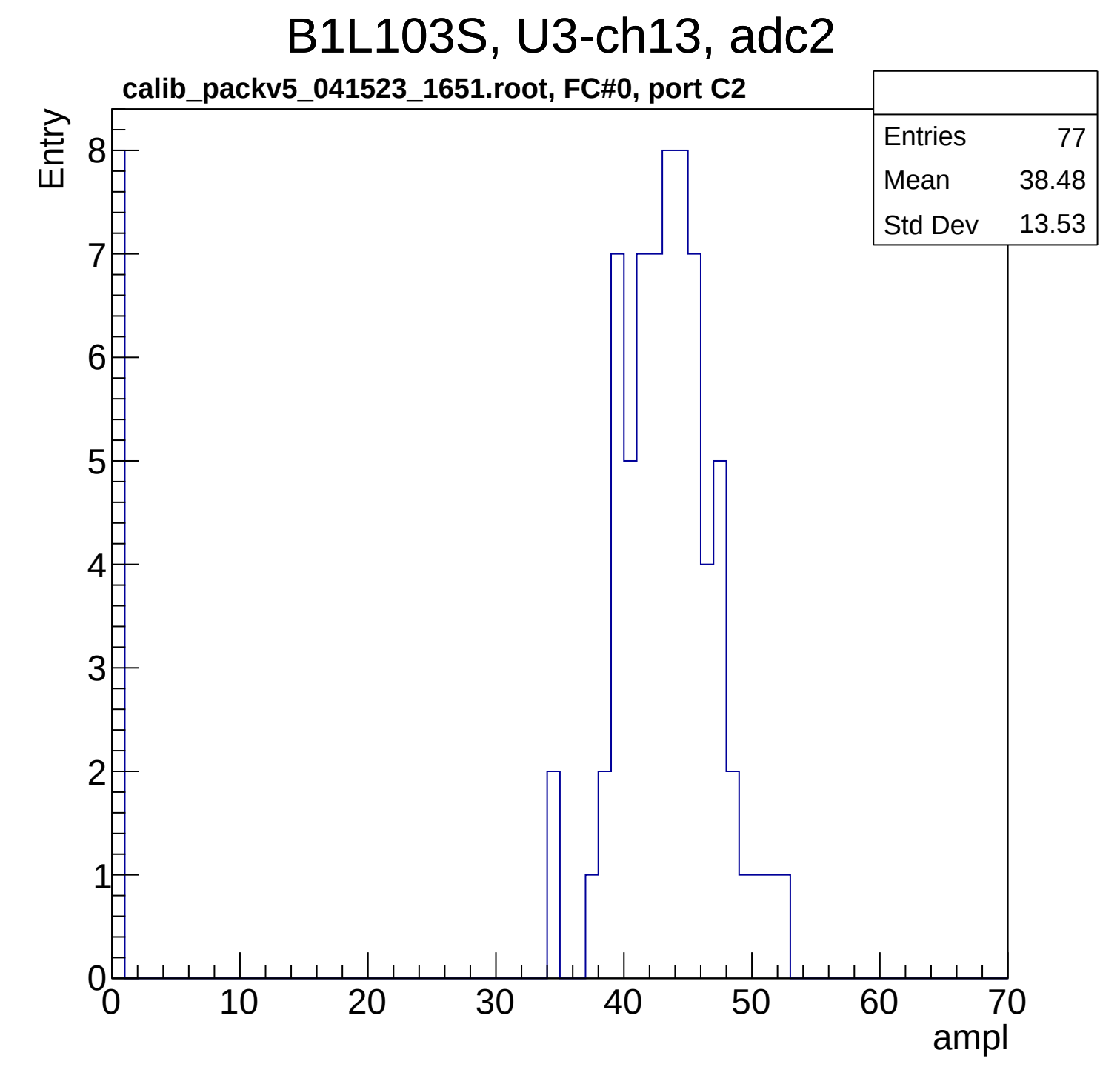

B1L103S, U3-ch12, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 59.12
Std Dev 12.13
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch12, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch13, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 23.36
Std Dev 12.05
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch13, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 34.99
Std Dev 5.352
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U3-ch13, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 38.48
Std Dev 13.53
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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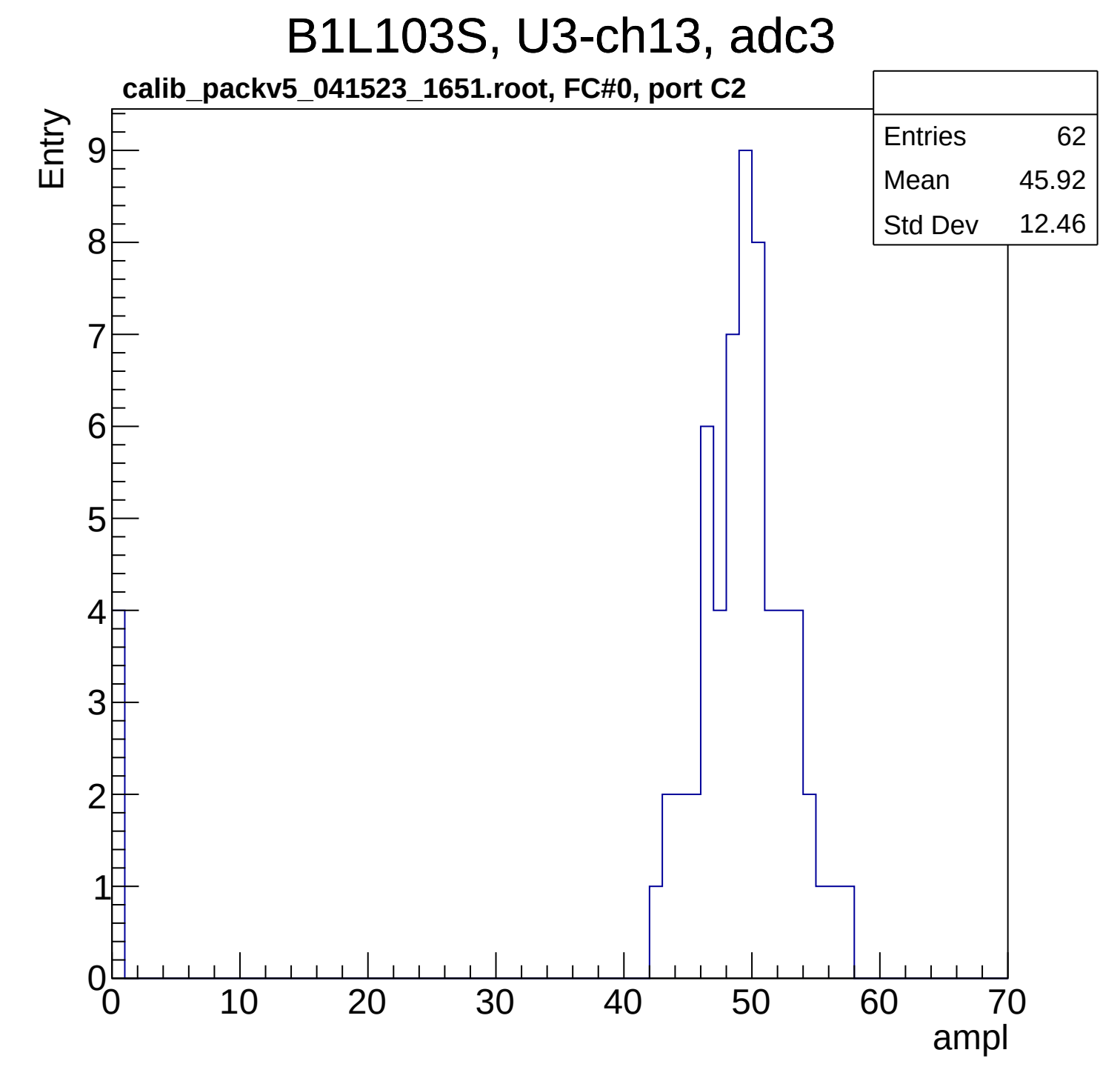
40
50
60
70


B1L103S, U3-ch13, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 45.92
Std Dev 12.46
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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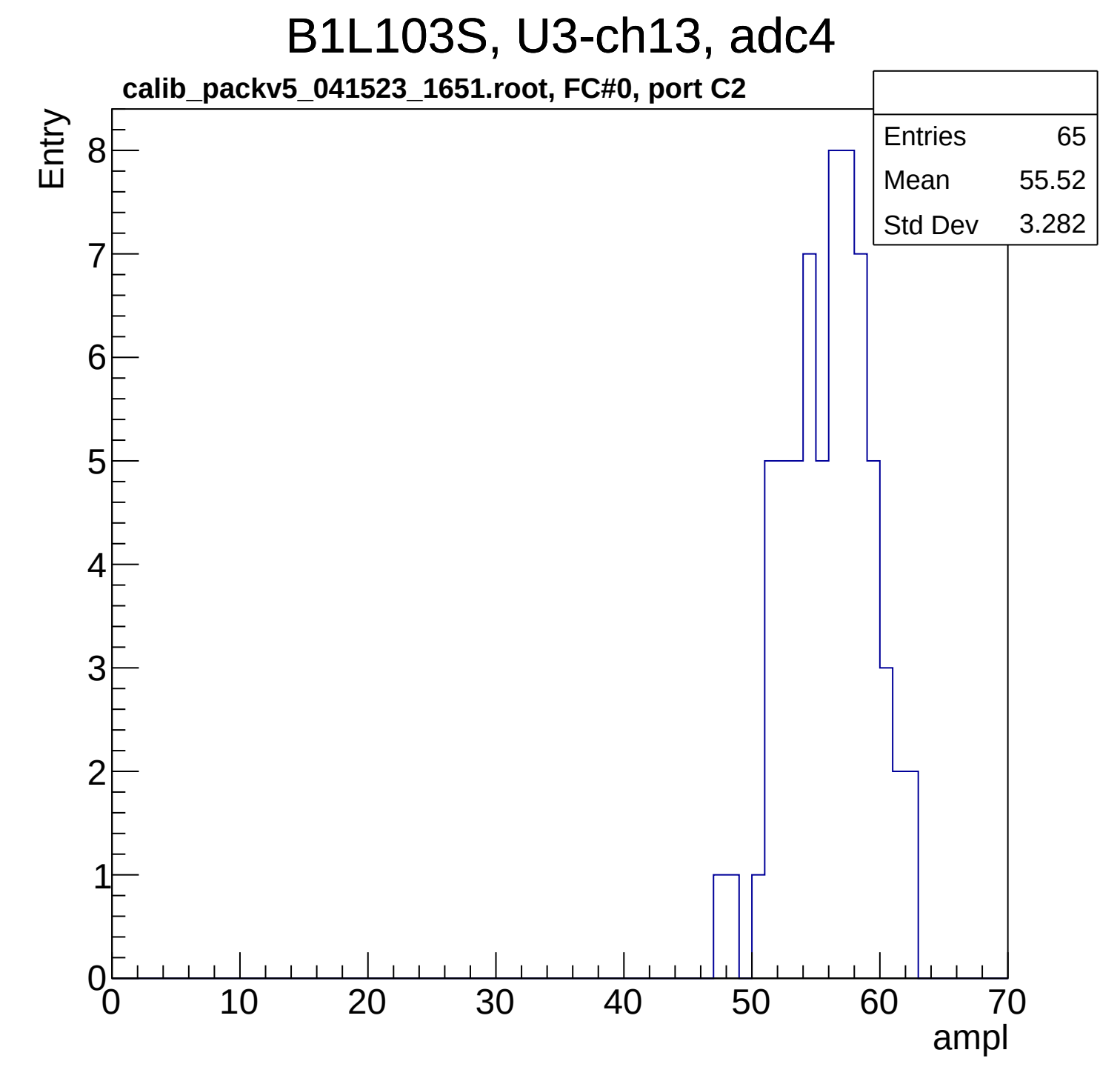
B1L103S, U3-ch13, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 55.52
Std Dev 3.282
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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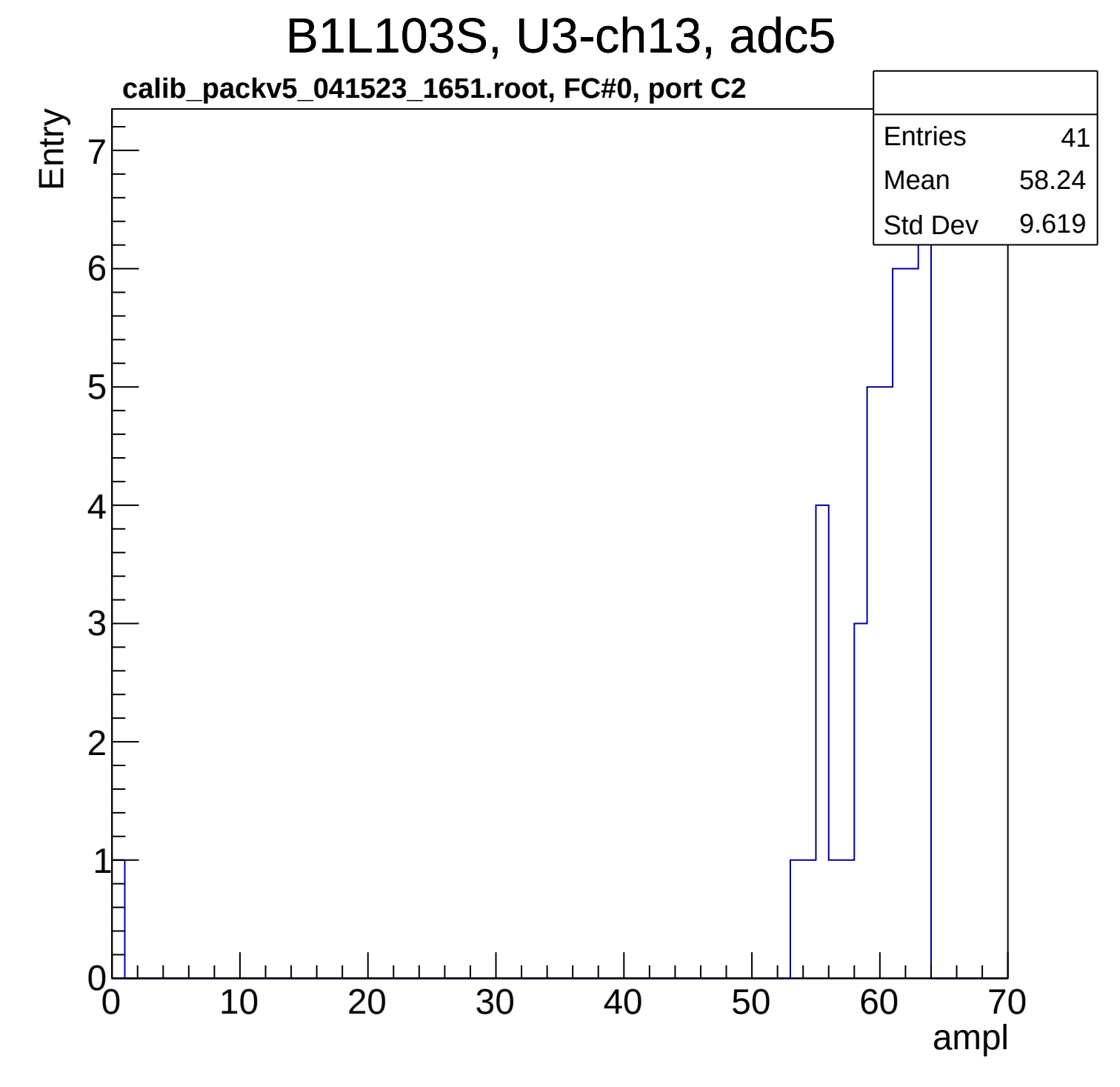
B1L103S, U3-ch13, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 58.24
Std Dev 9.619
Entry
ampl
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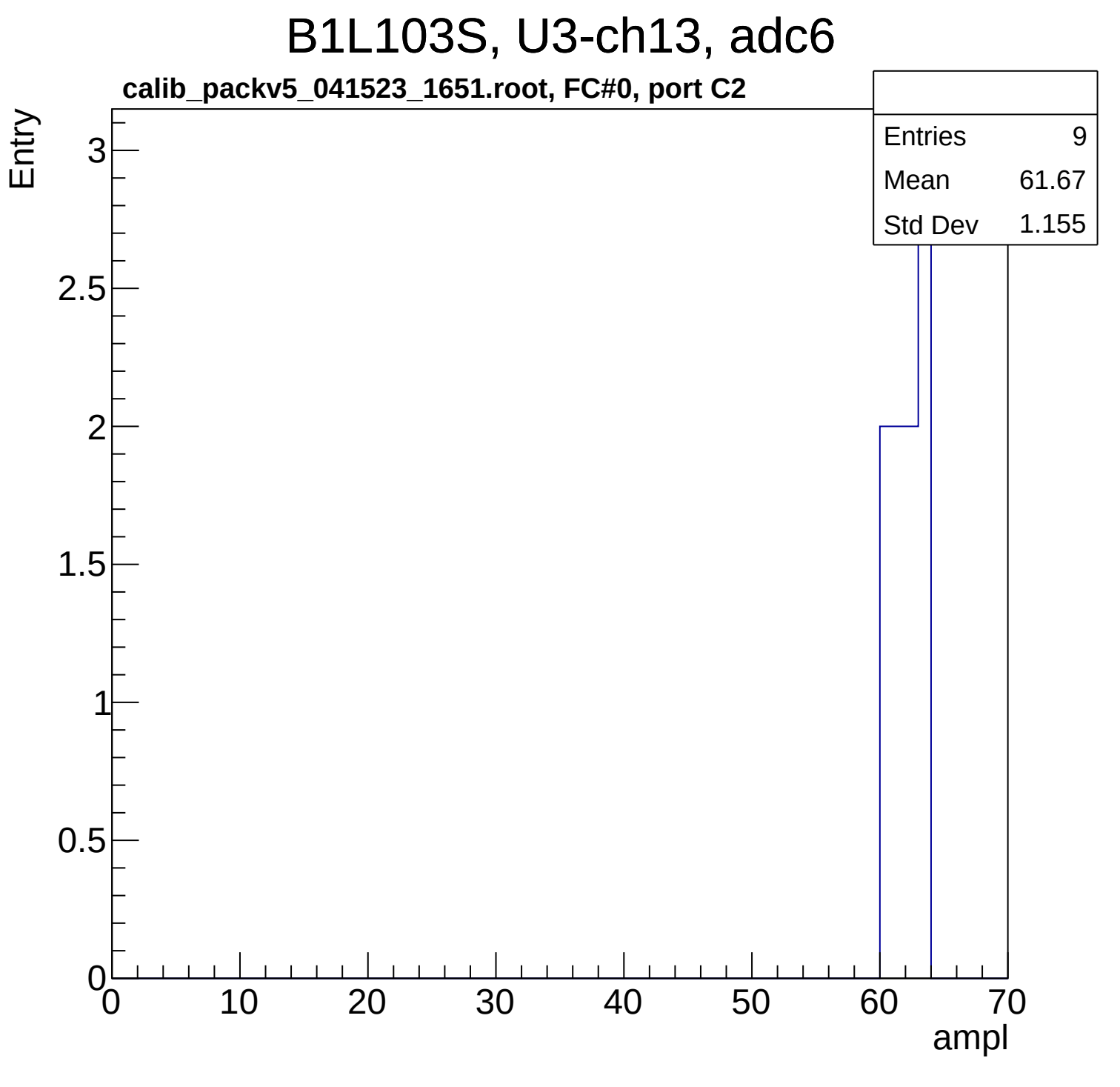
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch13, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 61.67
Std Dev 1.155
Entry
ampl
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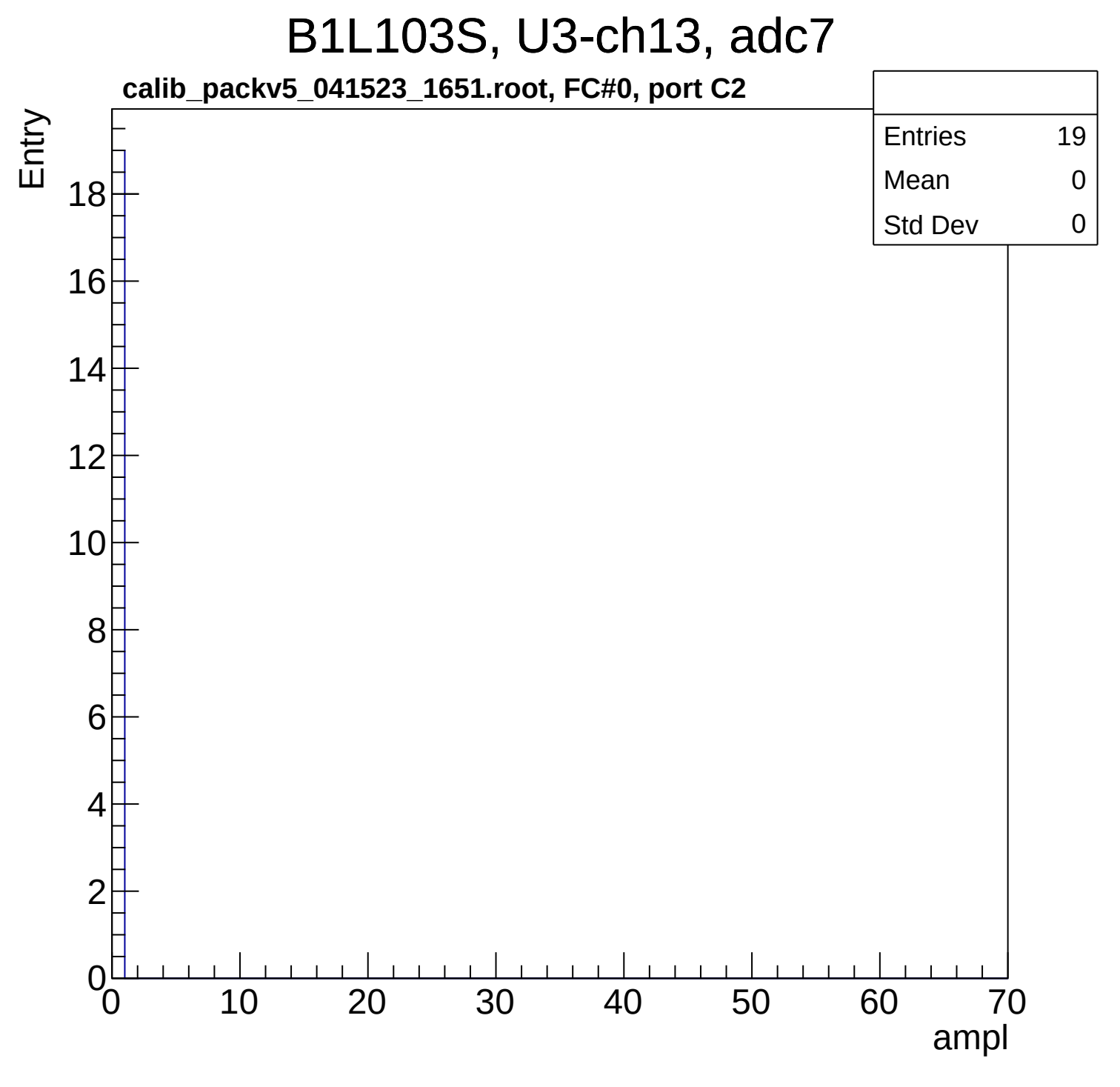
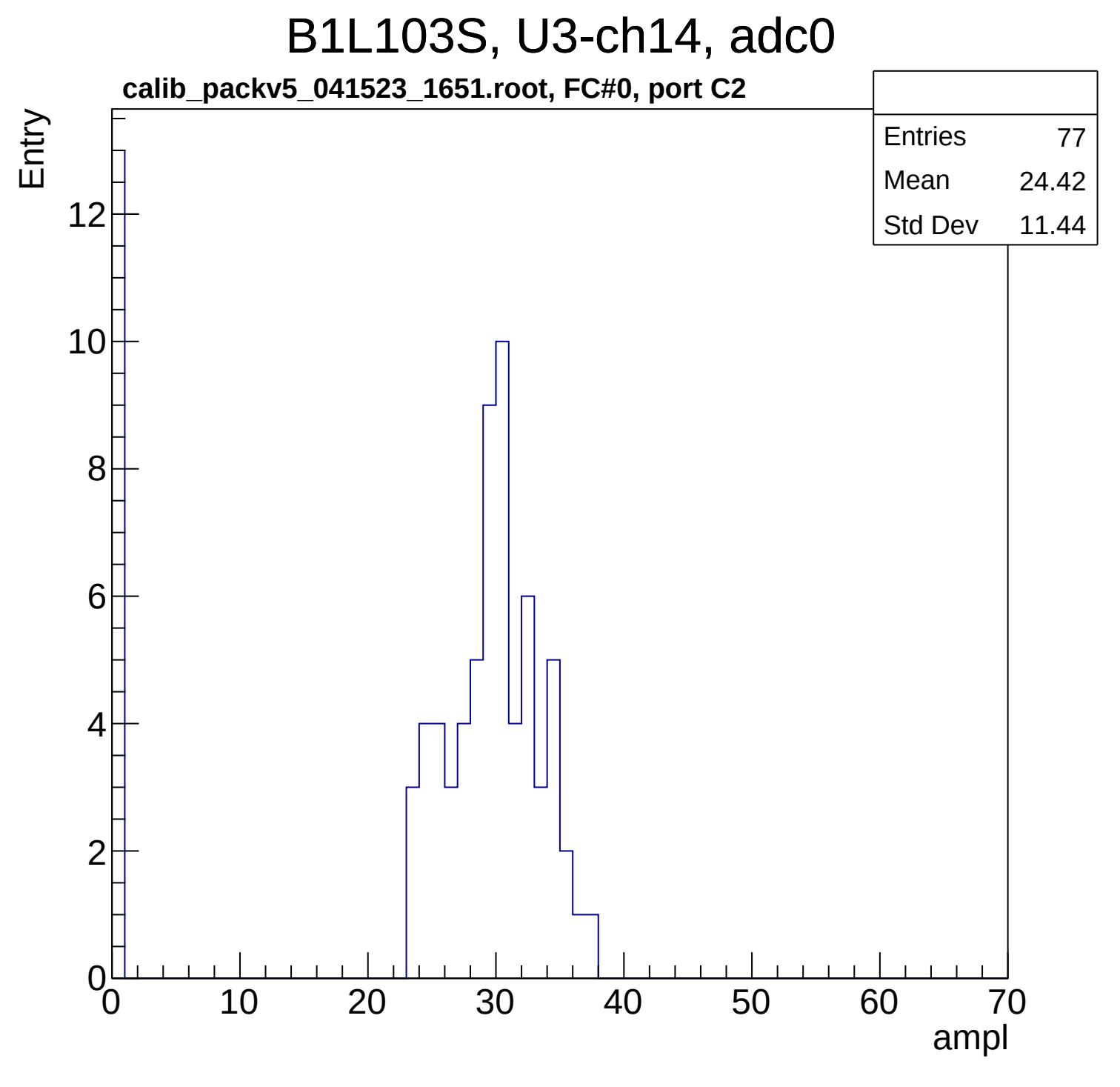
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U3-ch13, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch14, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 24.42
Std Dev 11.44
Entry
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2
4
6
8
10
12
0
10
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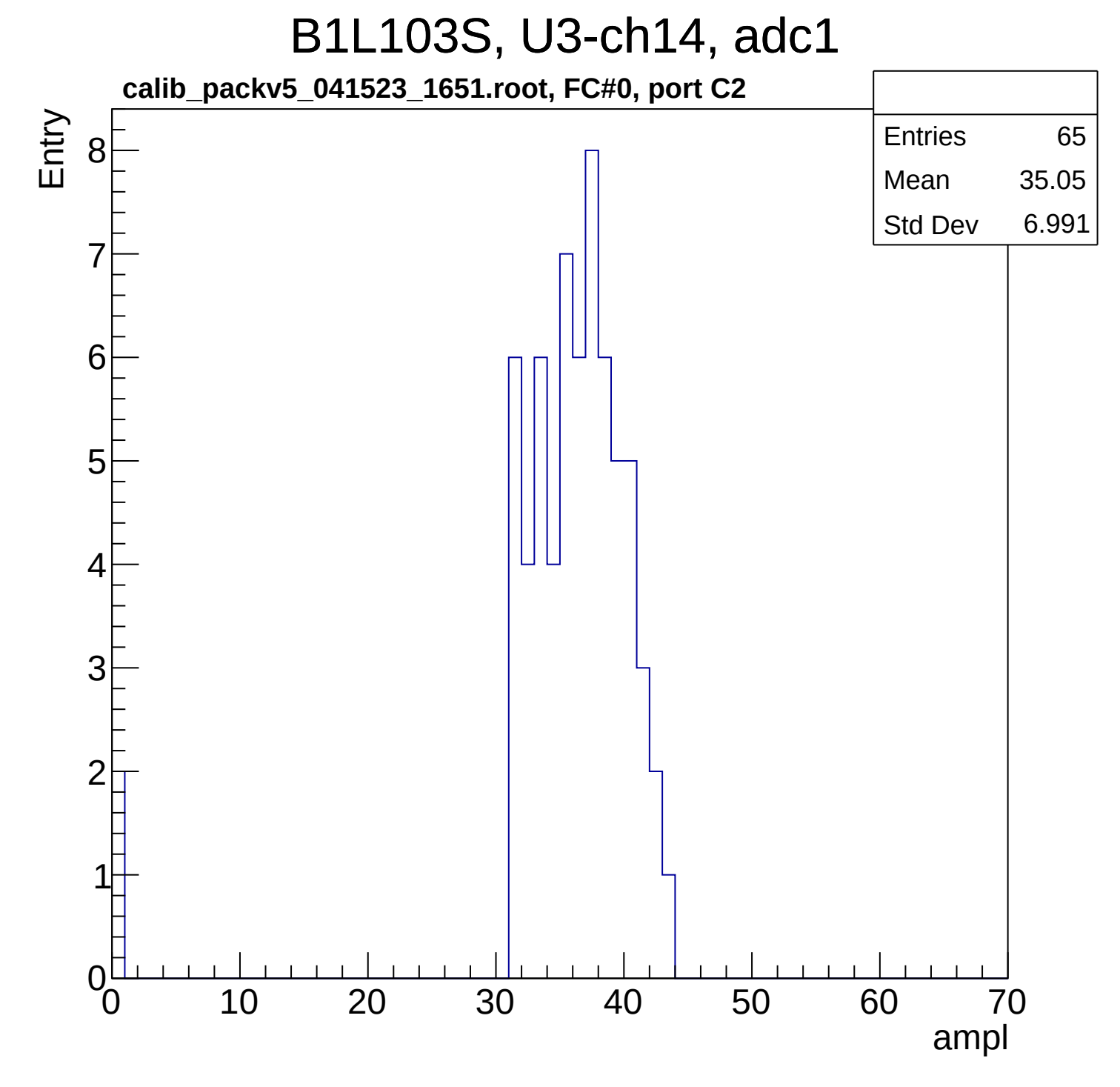
60
70
ampl


B1L103S, U3-ch14, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 35.05
Std Dev 6.991
Entry
ampl
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3
4
5
6
7
8
0
10
20
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40
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60
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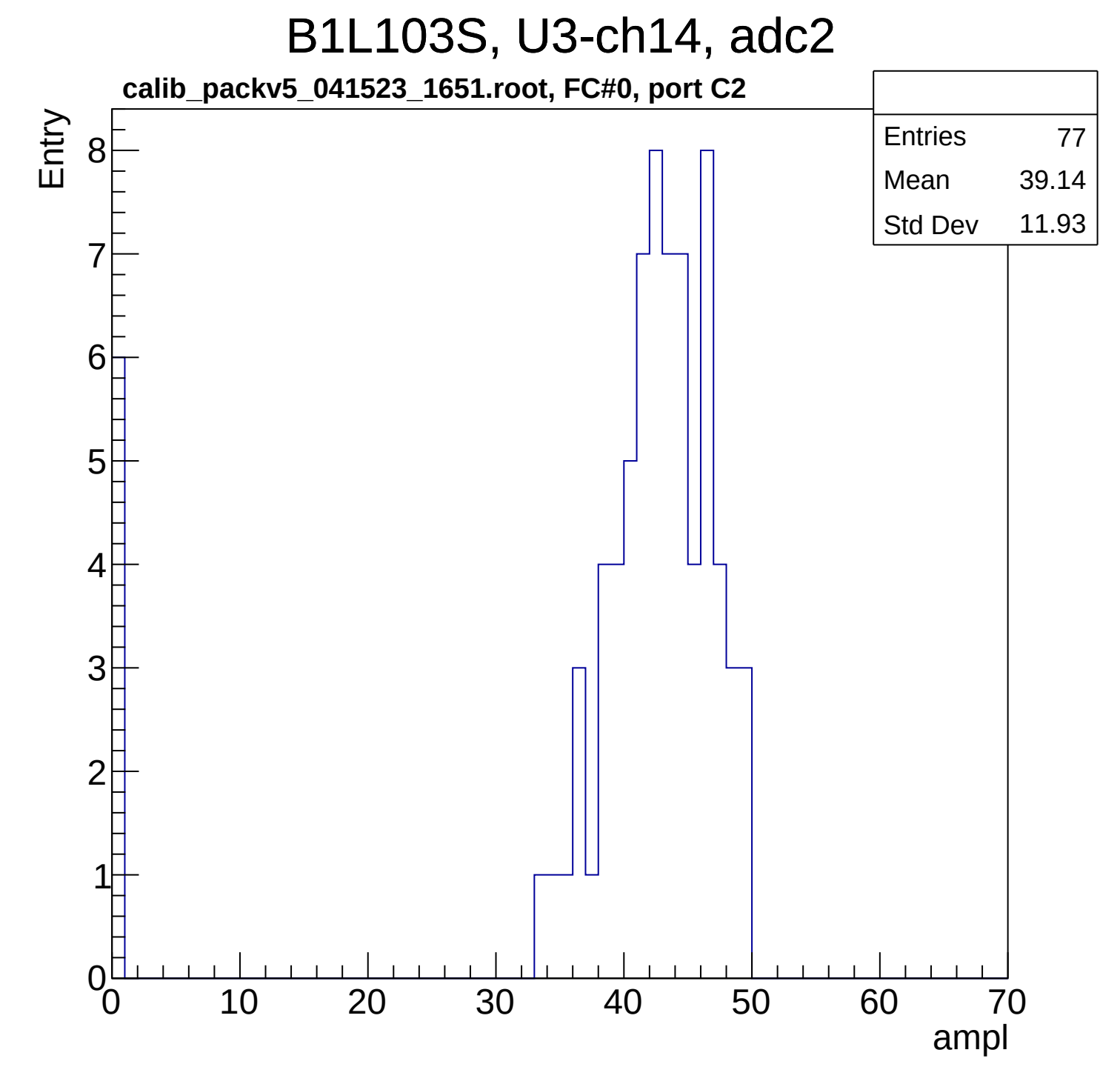
B1L103S, U3-ch14, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 39.14
Std Dev 11.93
Entry
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2
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4
5
6
7
8
0
10
20
30
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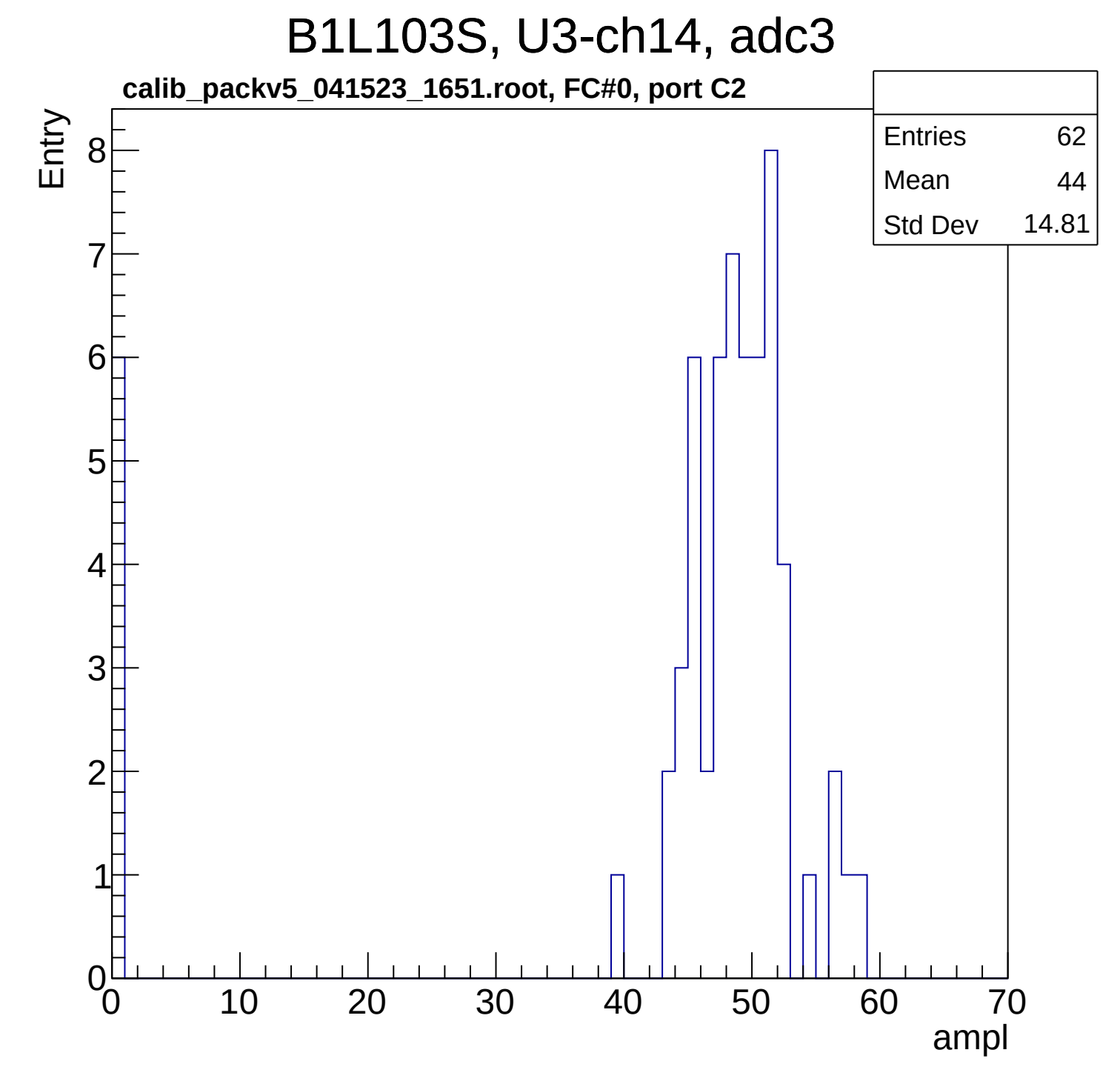
50
60
70
ampl


B1L103S, U3-ch14, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 44
Std Dev 14.81
Entry
ampl
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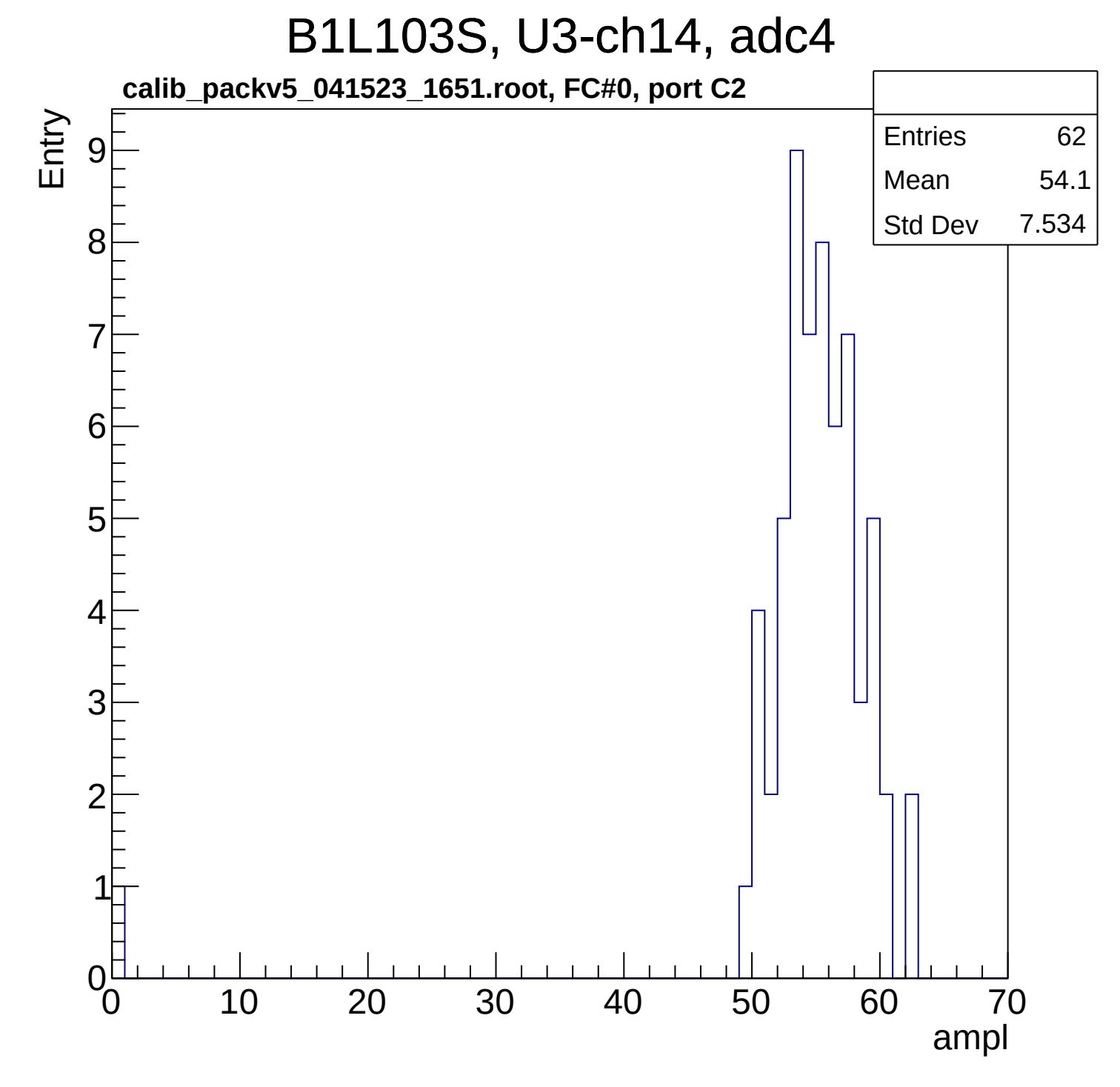
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch14, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 54.1
Std Dev 7.534
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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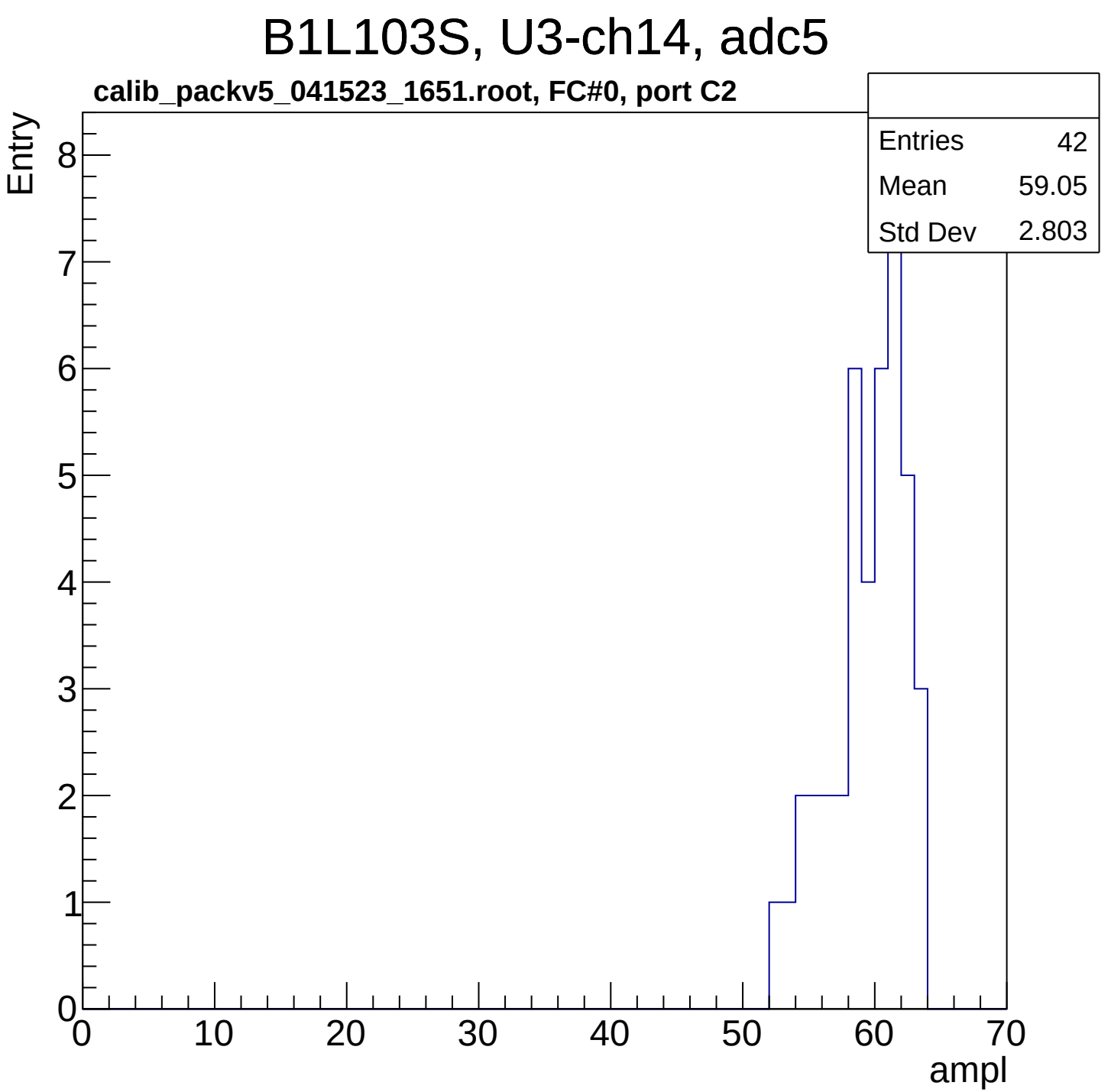
B1L103S, U3-ch14, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 59.05
Std Dev 2.803
Entry
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3
4
5
6
7
8
0
10
20
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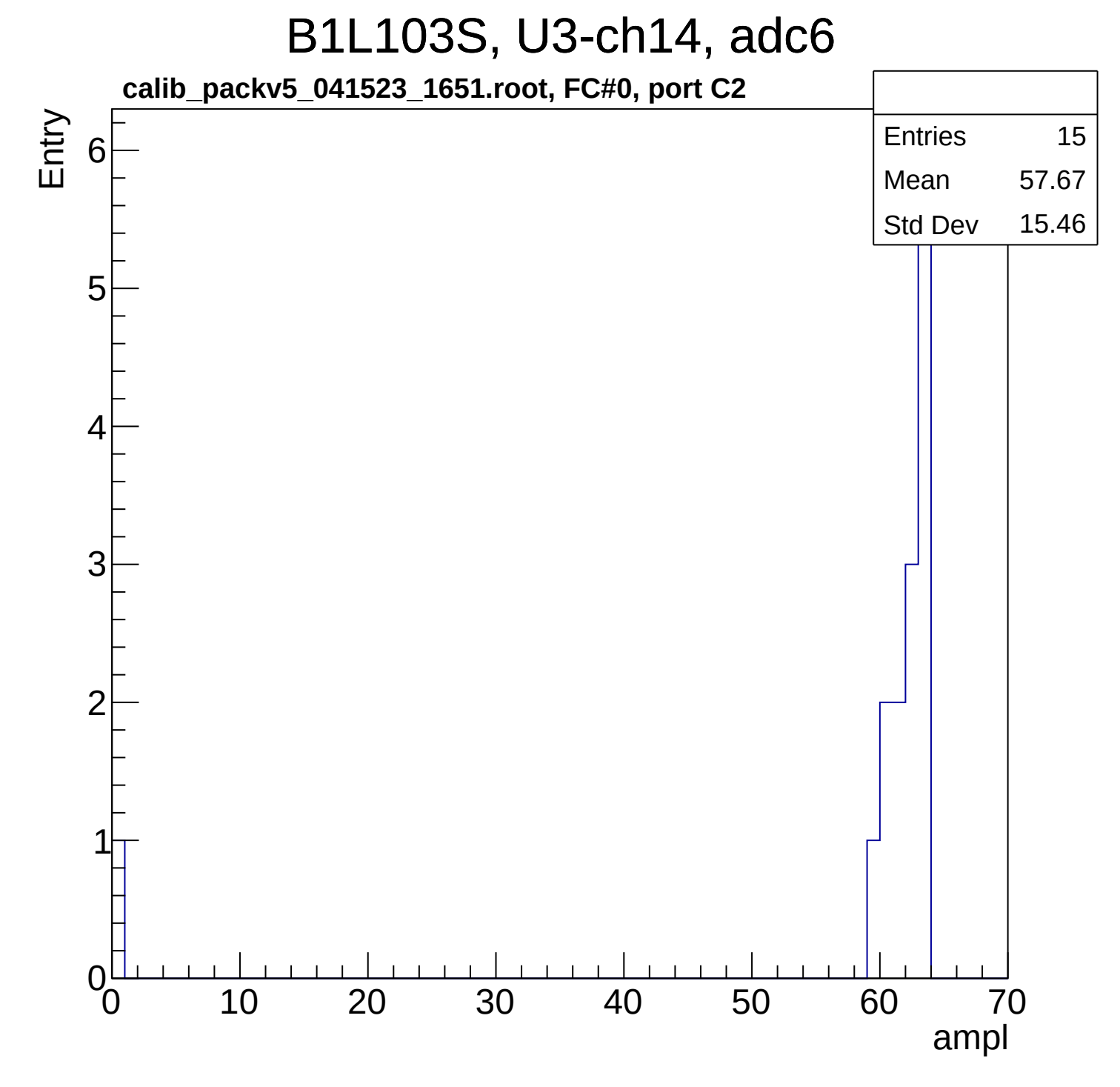
50
60
70
ampl


B1L103S, U3-ch14, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 57.67
Std Dev 15.46
Entry
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2
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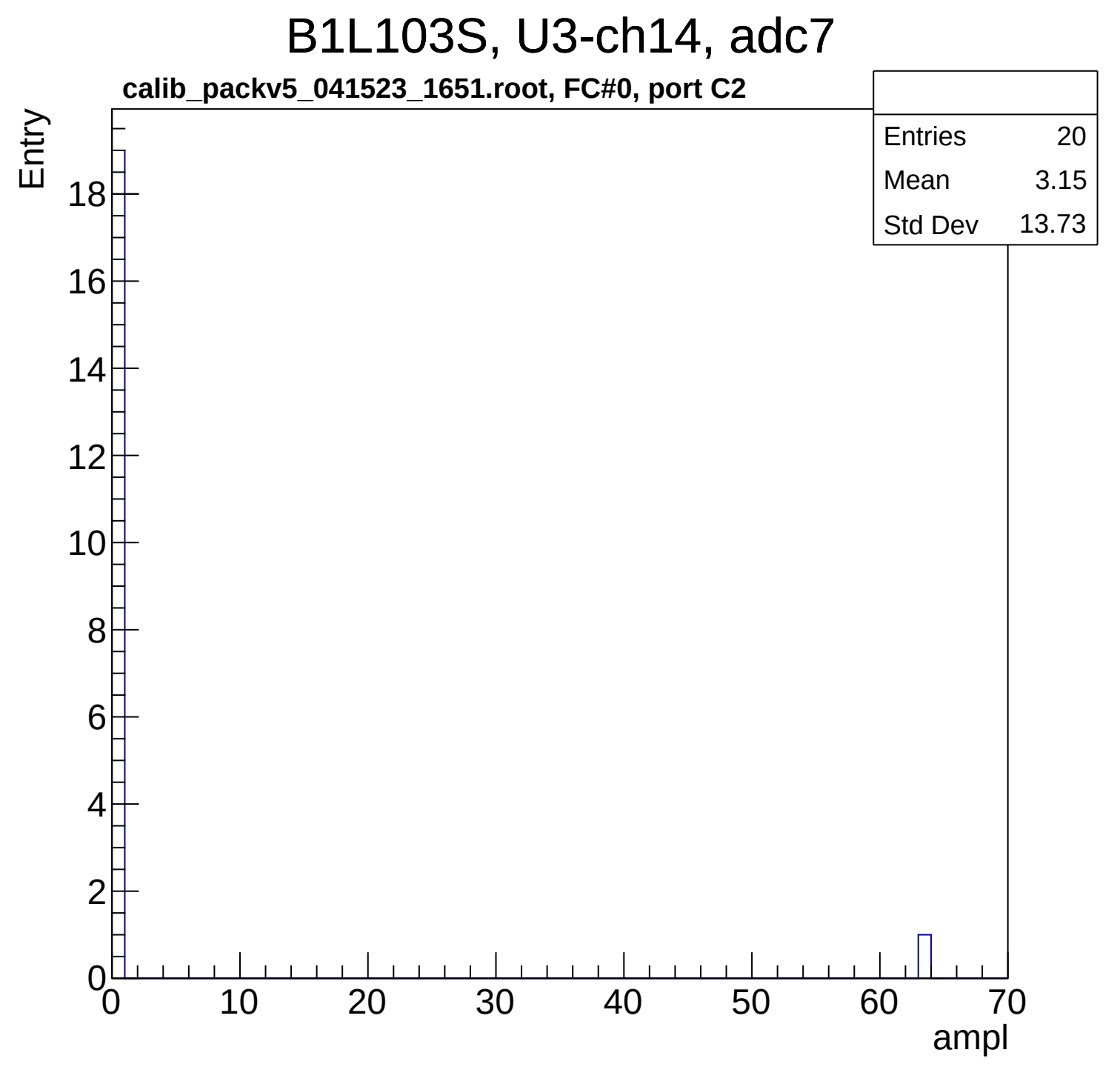
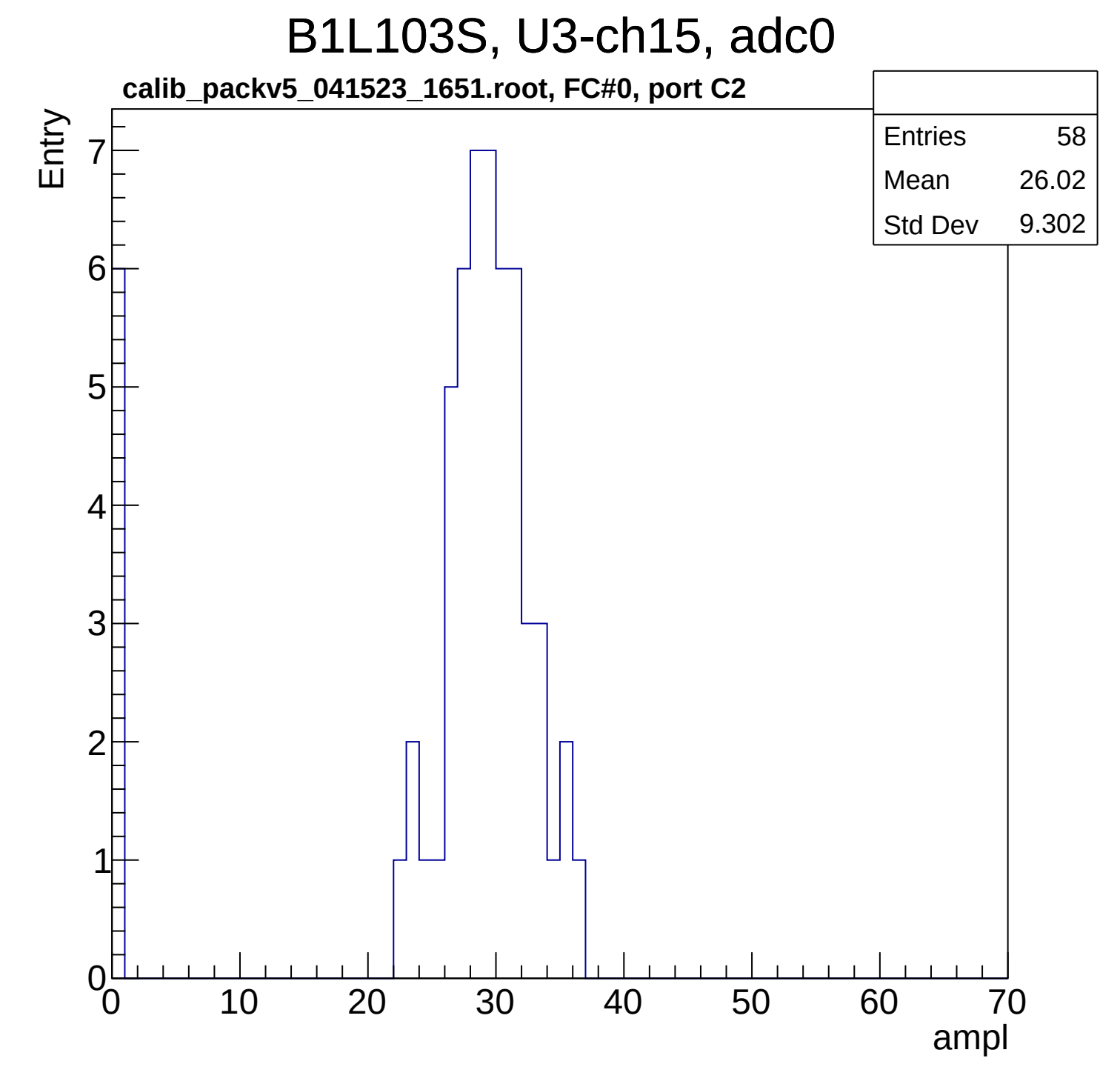
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch14, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch15, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 26.02
Std Dev 9.302
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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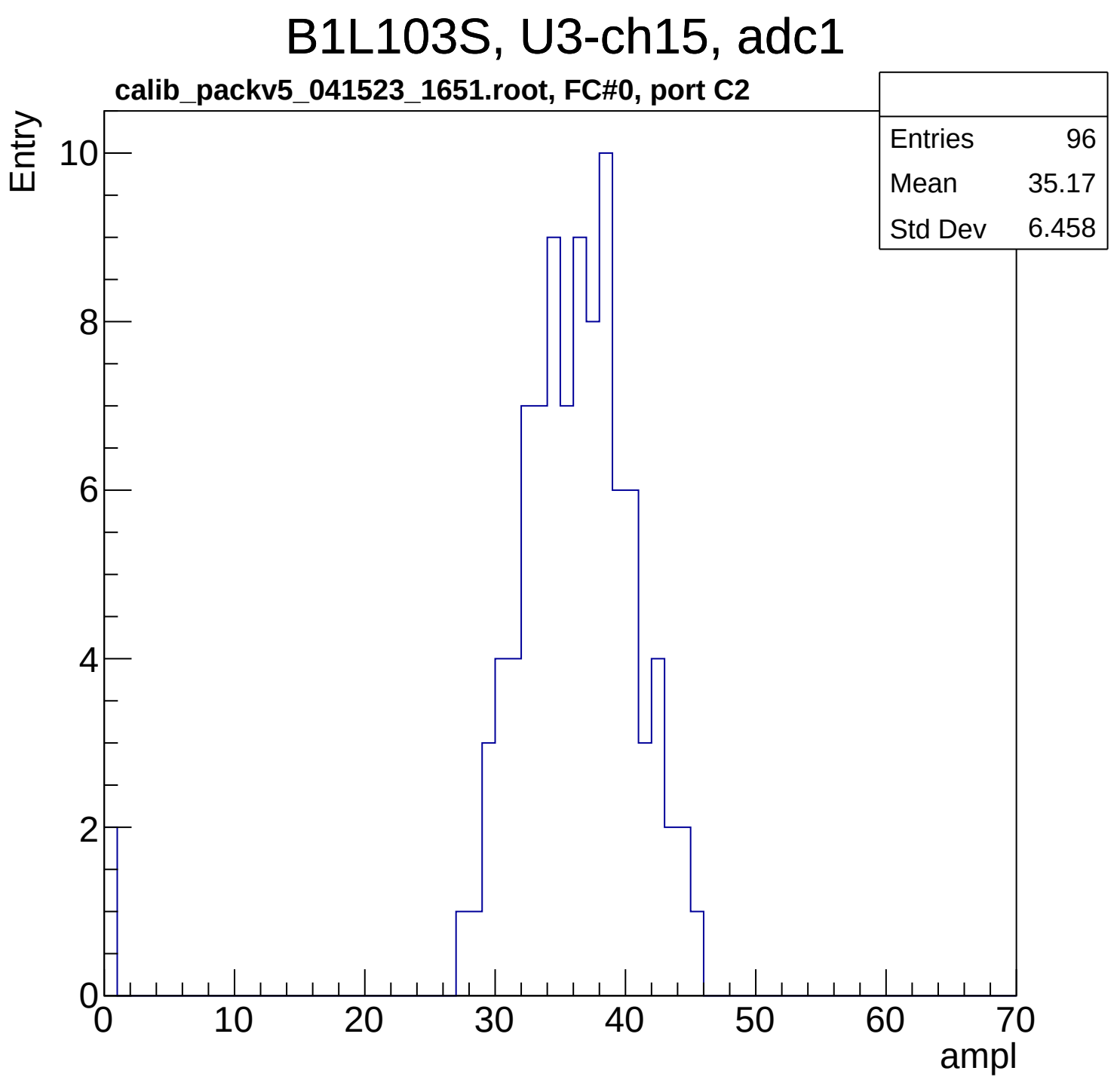
B1L103S, U3-ch15, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 96
Mean 35.17
Std Dev 6.458
Entry
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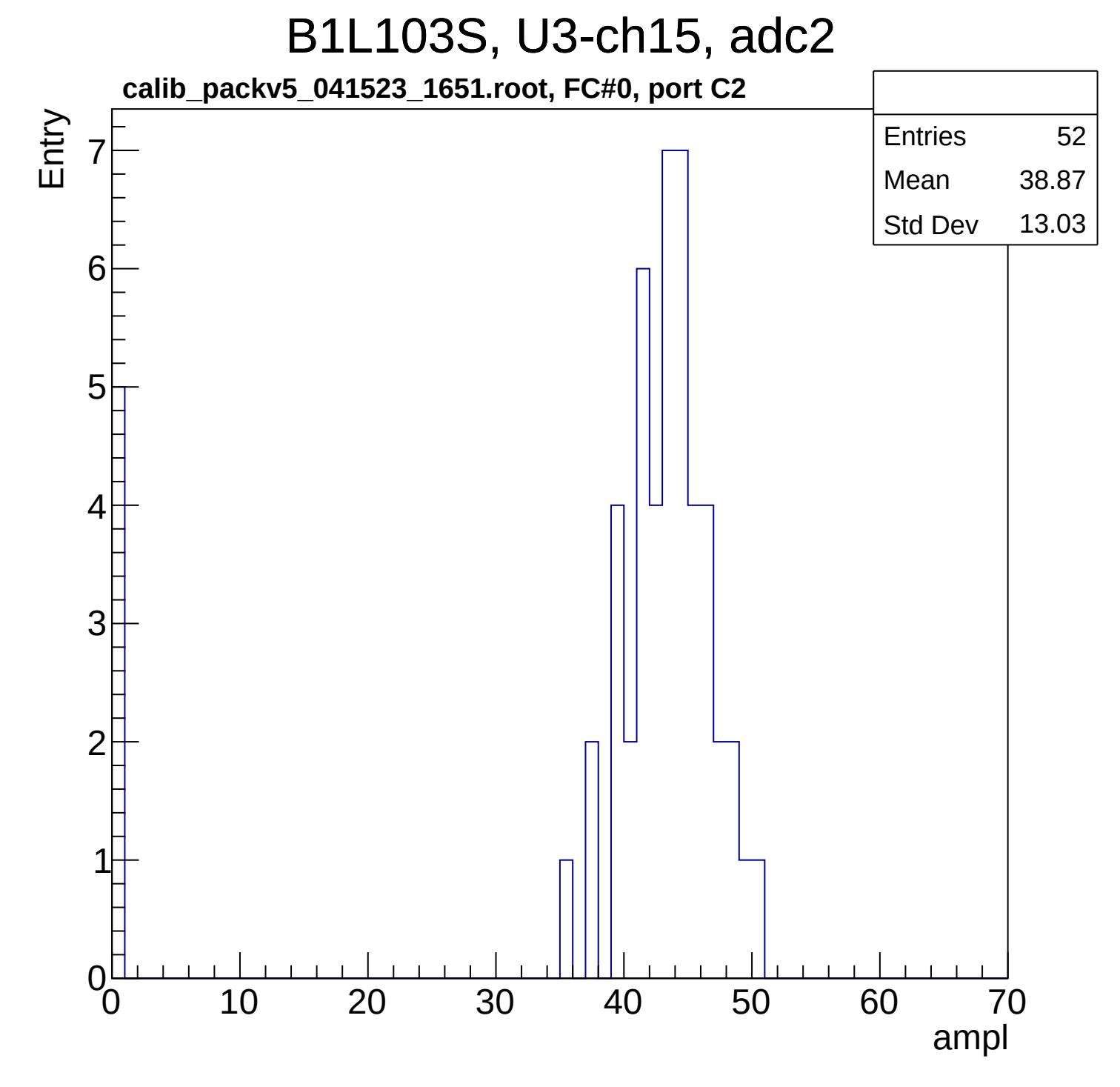
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch15, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 38.87
Std Dev 13.03
Entry
ampl
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4
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0
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20
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40
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60
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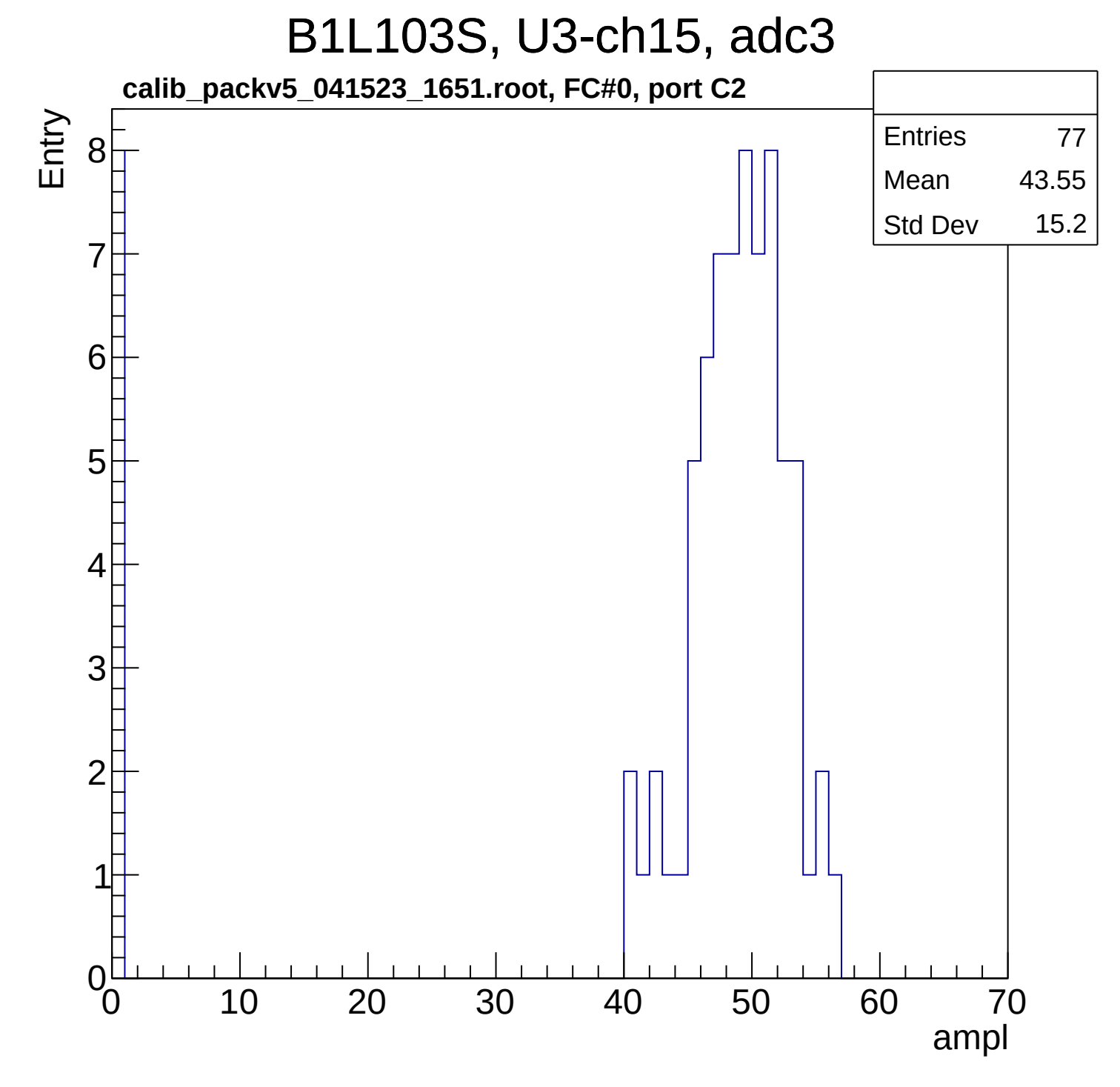
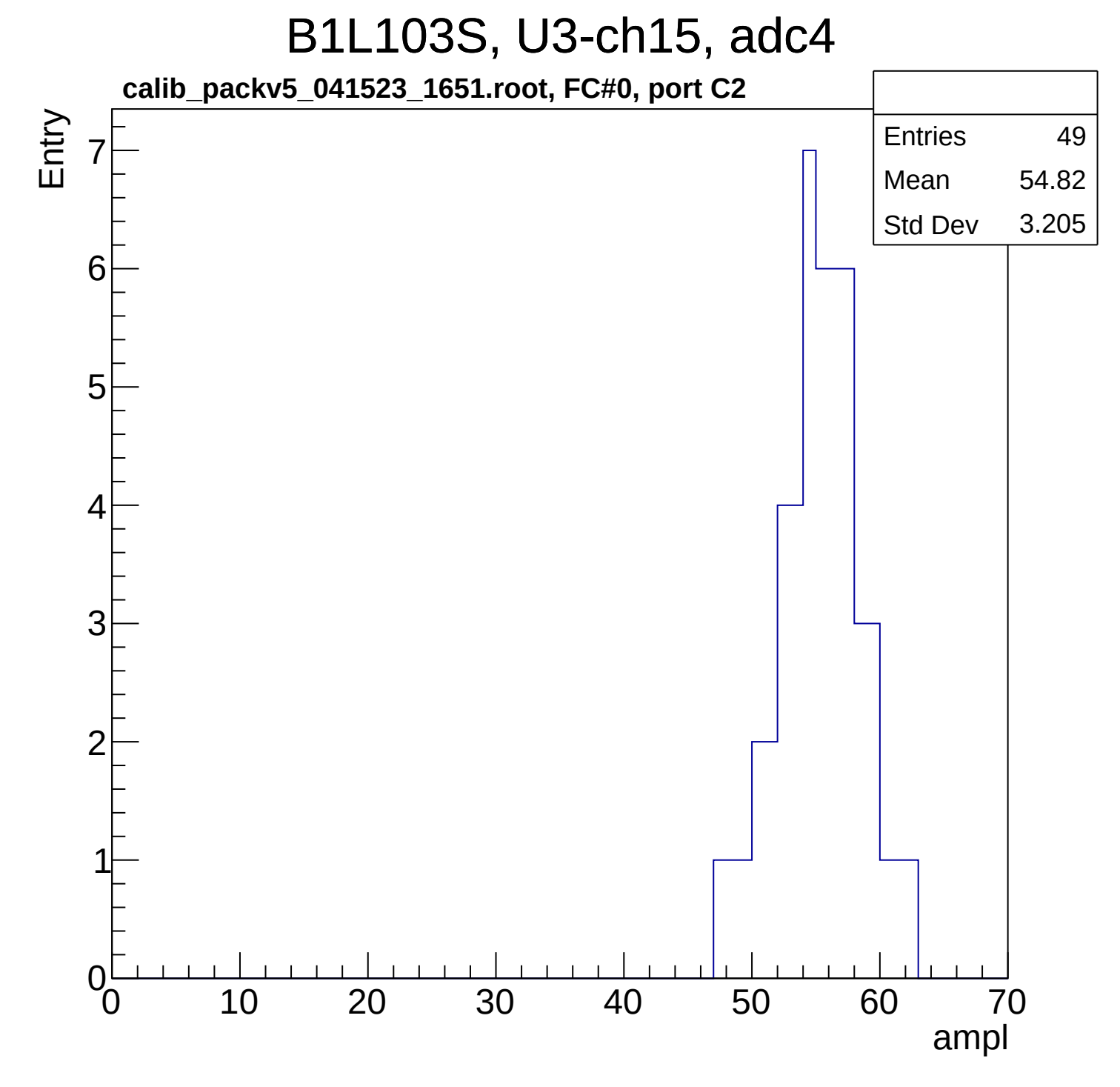

B1L103S, U3-ch15, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 43.55
Std Dev 15.2
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch15, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 54.82
Std Dev 3.205
Entry
ampl
0
1
2
3
4
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6
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0
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40
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60
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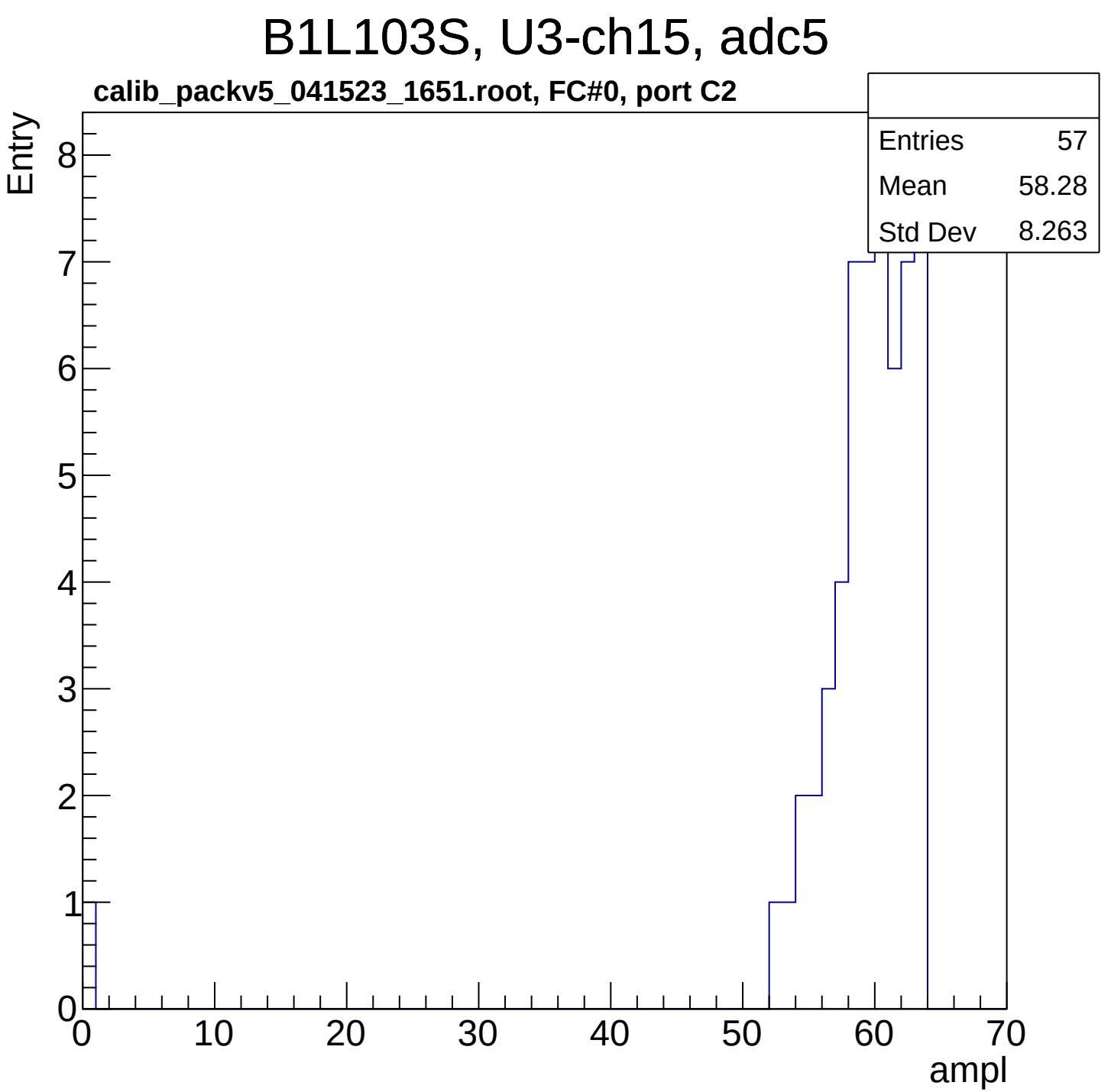
B1L103S, U3-ch15, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 58.28
Std Dev 8.263
Entry
ampl
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2
3
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5
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7
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0
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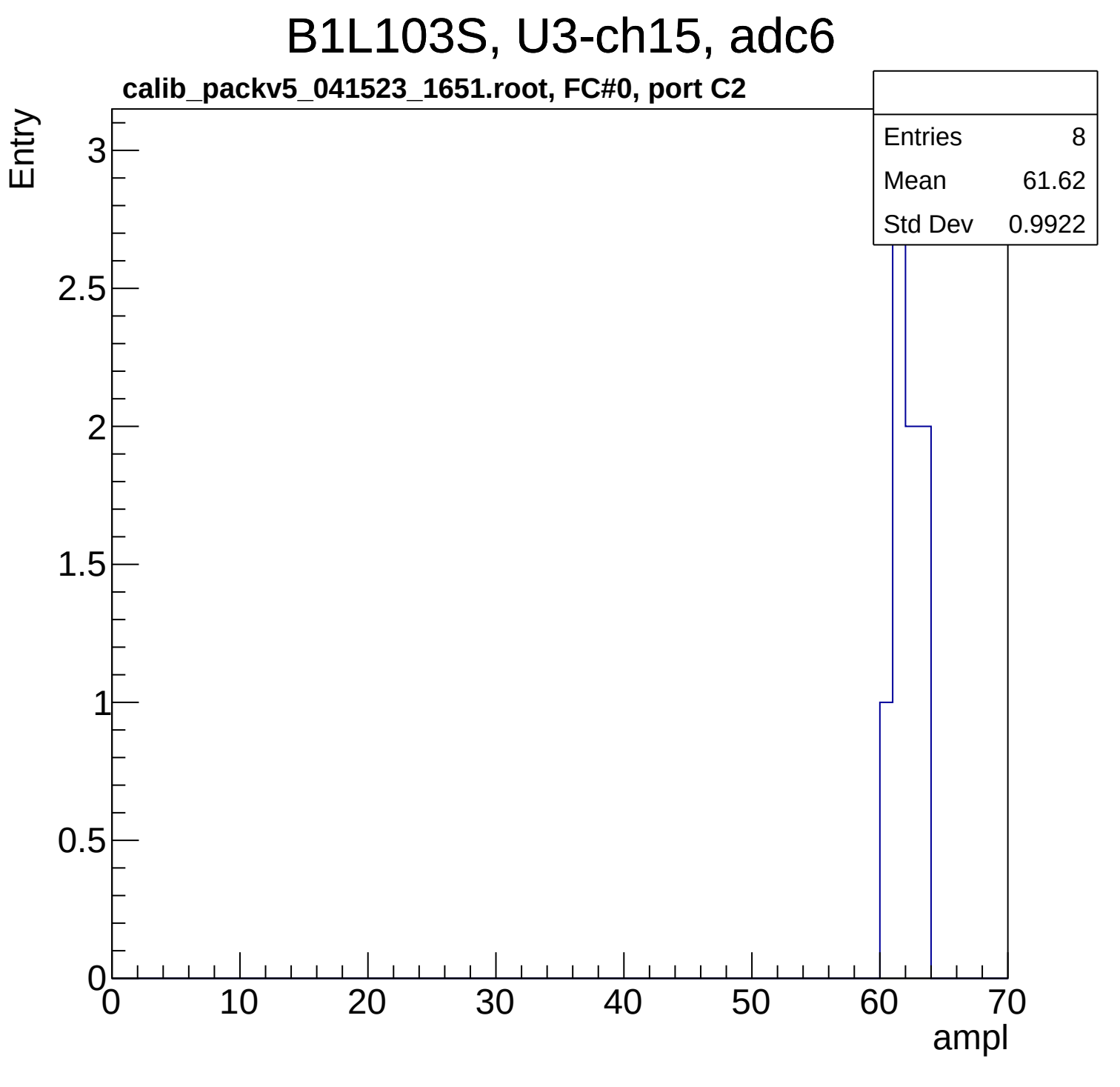
B1L103S, U3-ch15, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 61.62
Std Dev 0.9922
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
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40
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60
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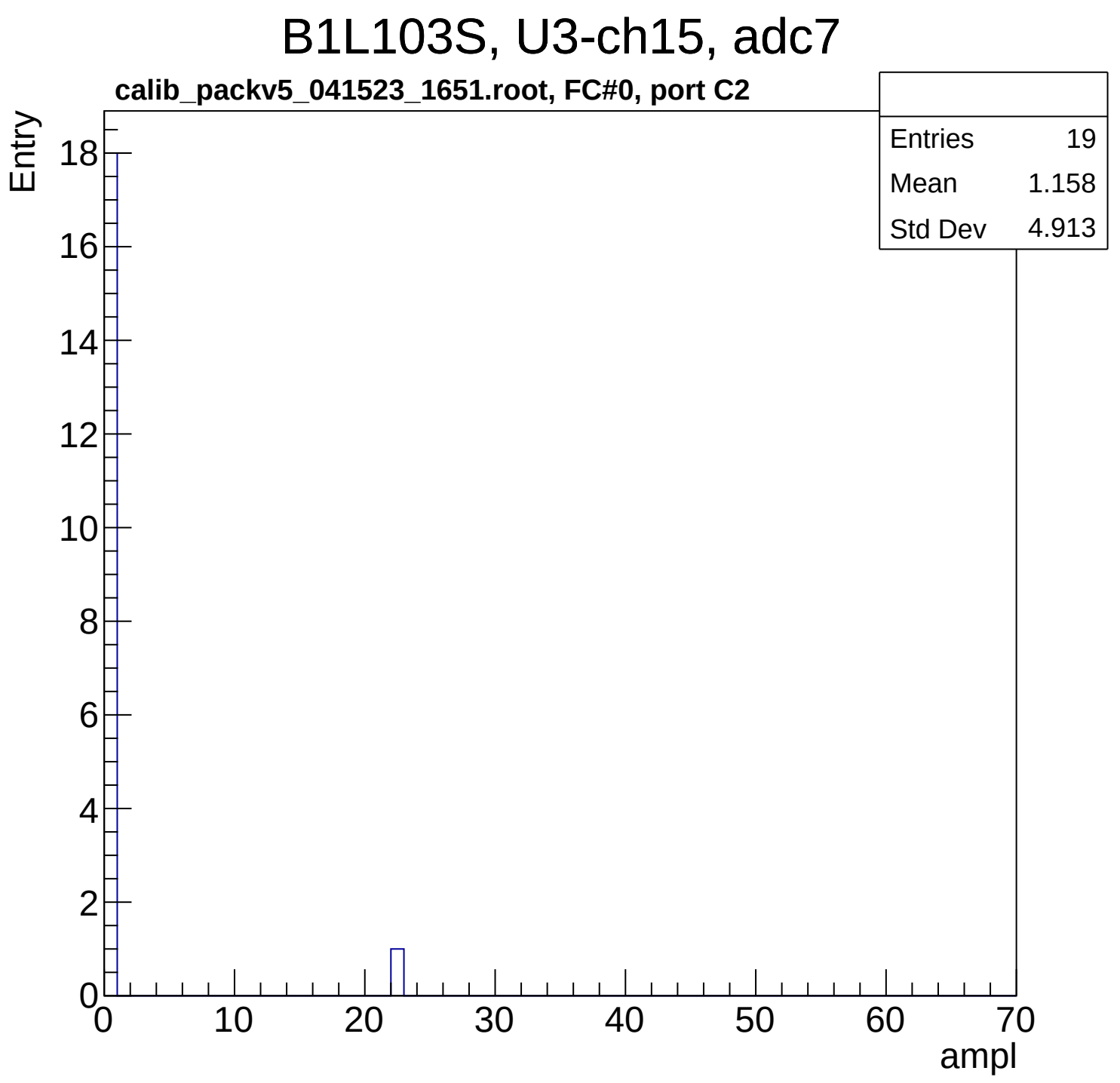
B1L103S, U3-ch15, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.158
Std Dev 4.913
Entry
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6
8
10
12
14
16
18
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10
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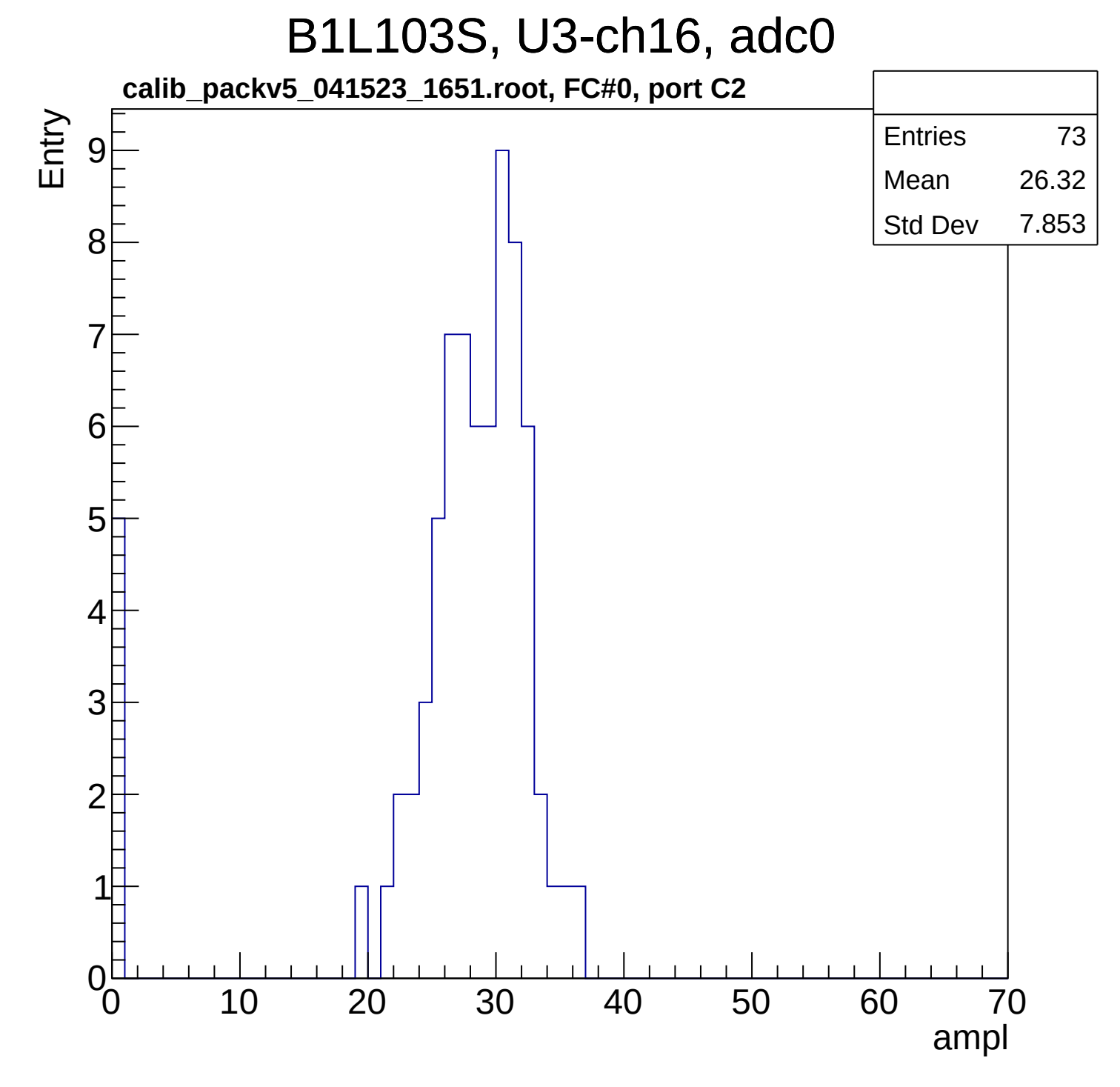
50
60
70
ampl


B1L103S, U3-ch16, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 26.32
Std Dev 7.853
Entry
ampl
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2
3
4
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6
7
8
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0
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60
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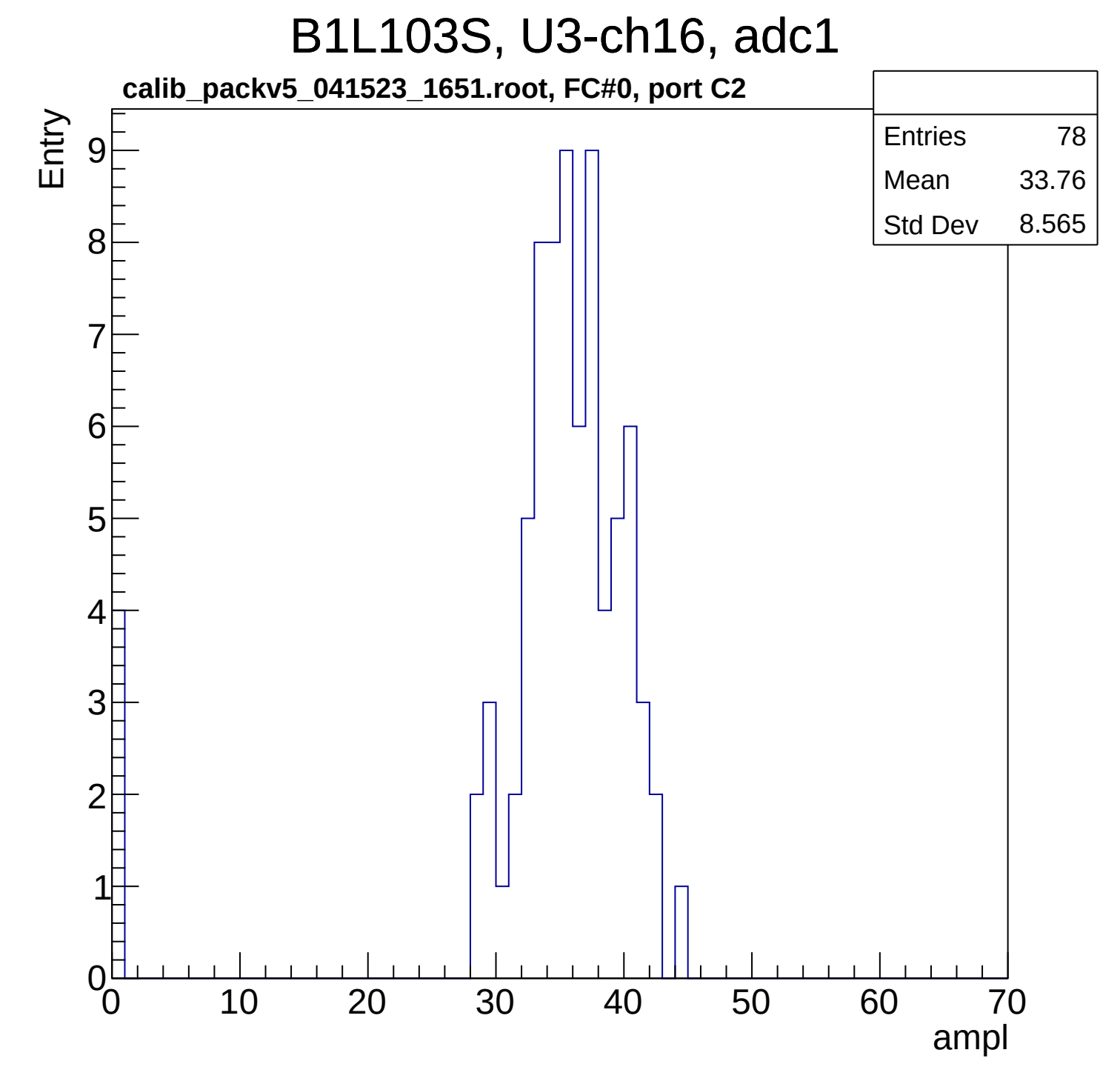
B1L103S, U3-ch16, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 33.76
Std Dev 8.565
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
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60
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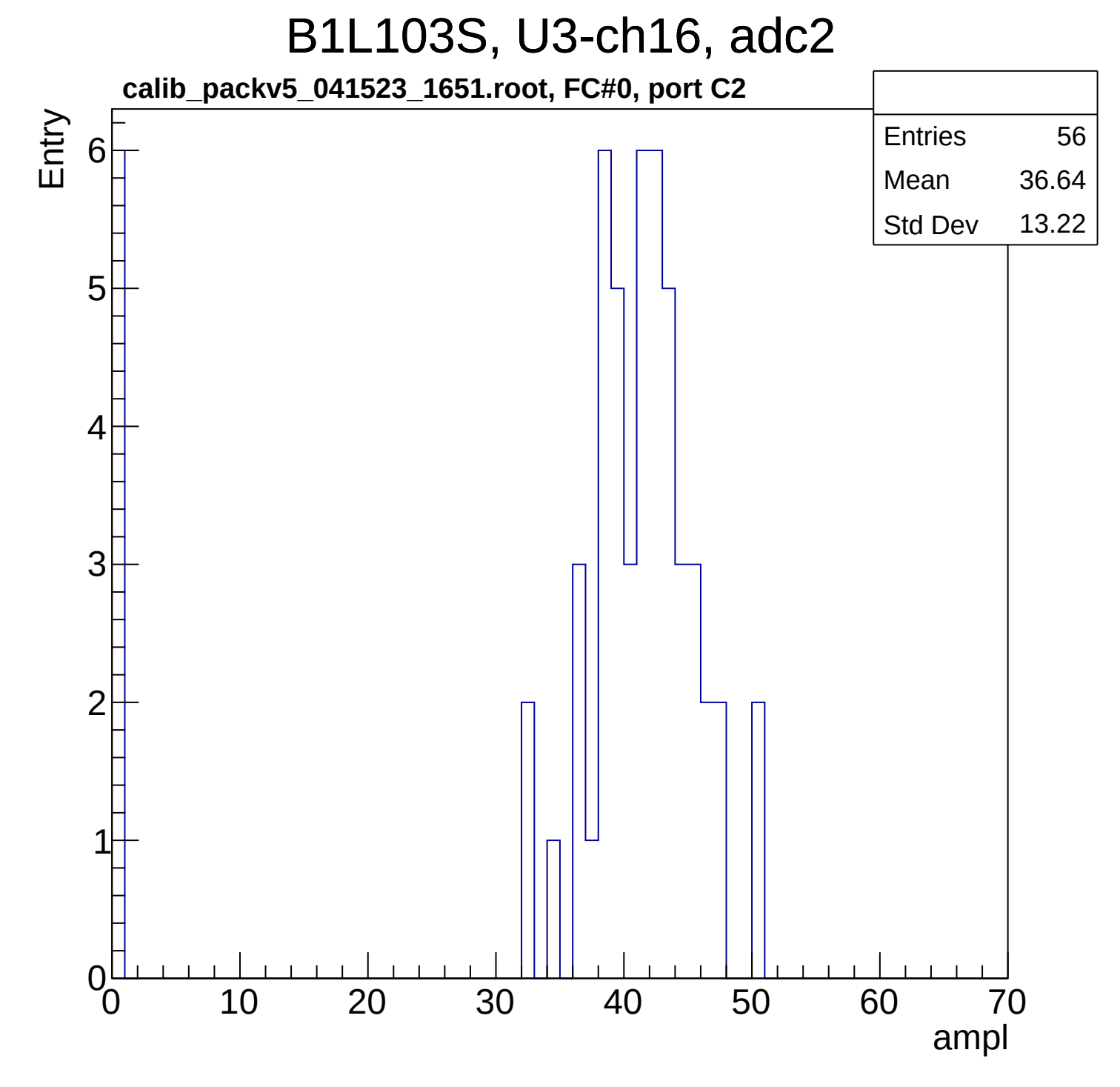
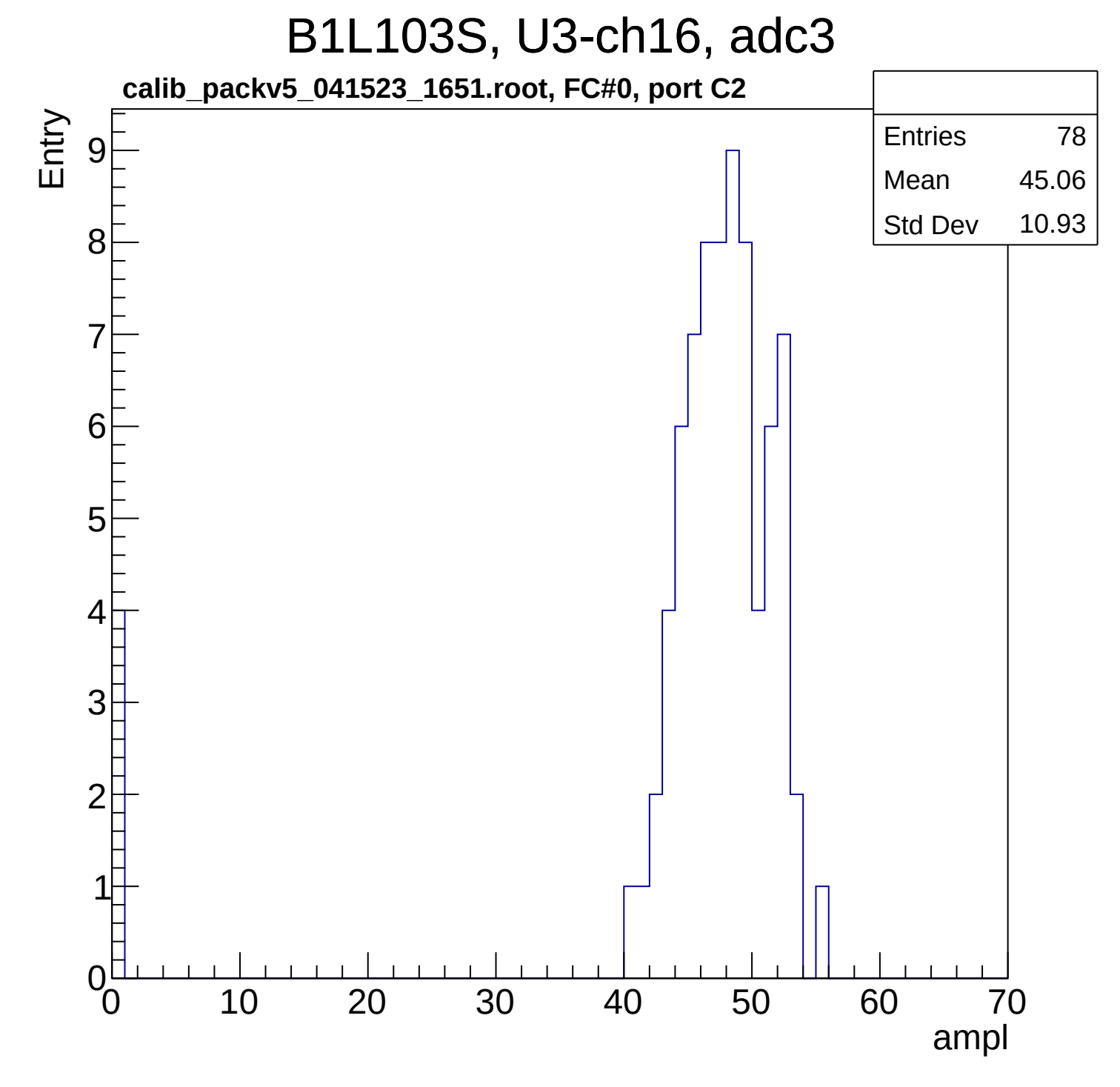

B1L103S, U3-ch16, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 36.64
Std Dev 13.22
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch16, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 45.06
Std Dev 10.93
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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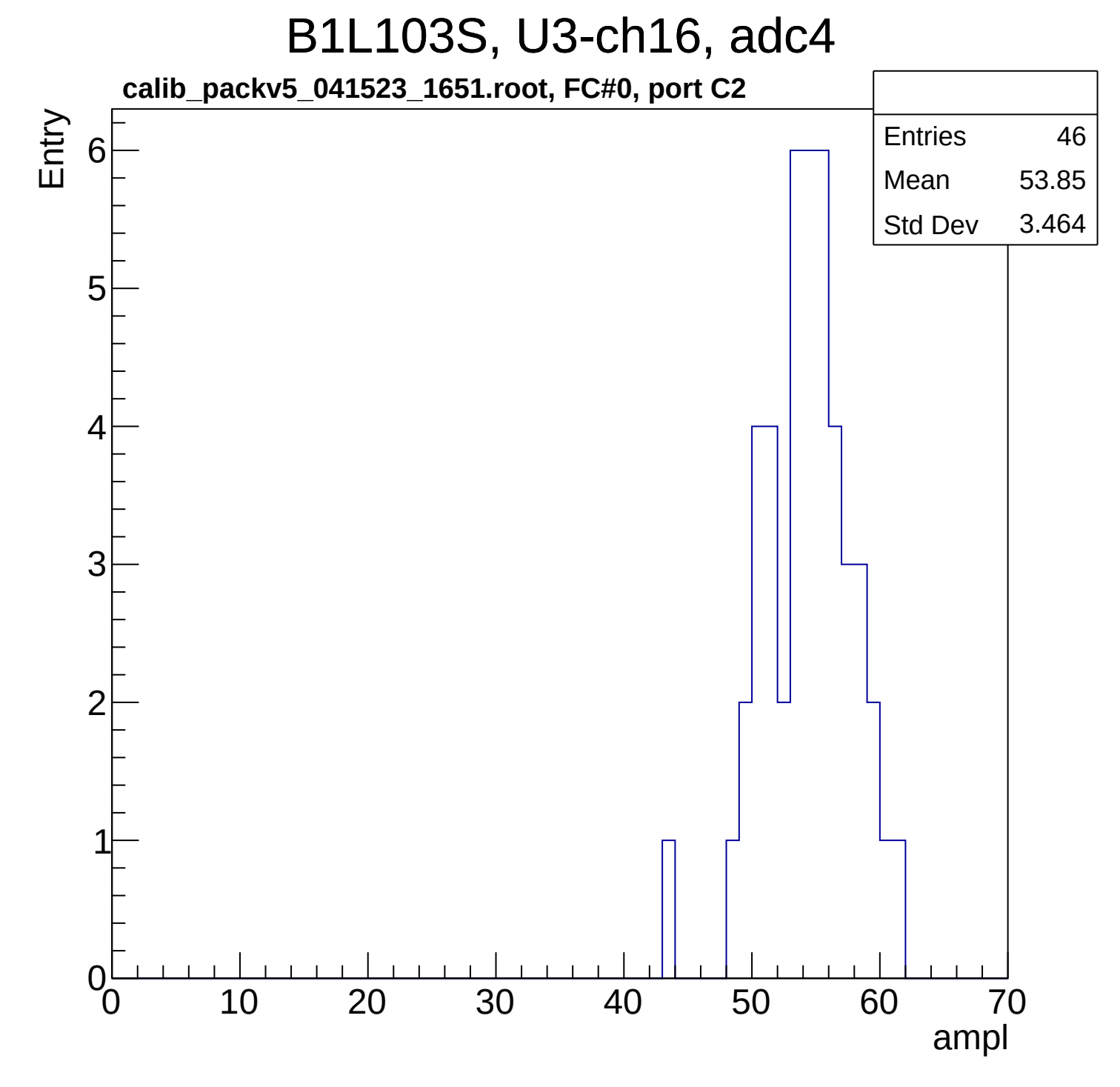
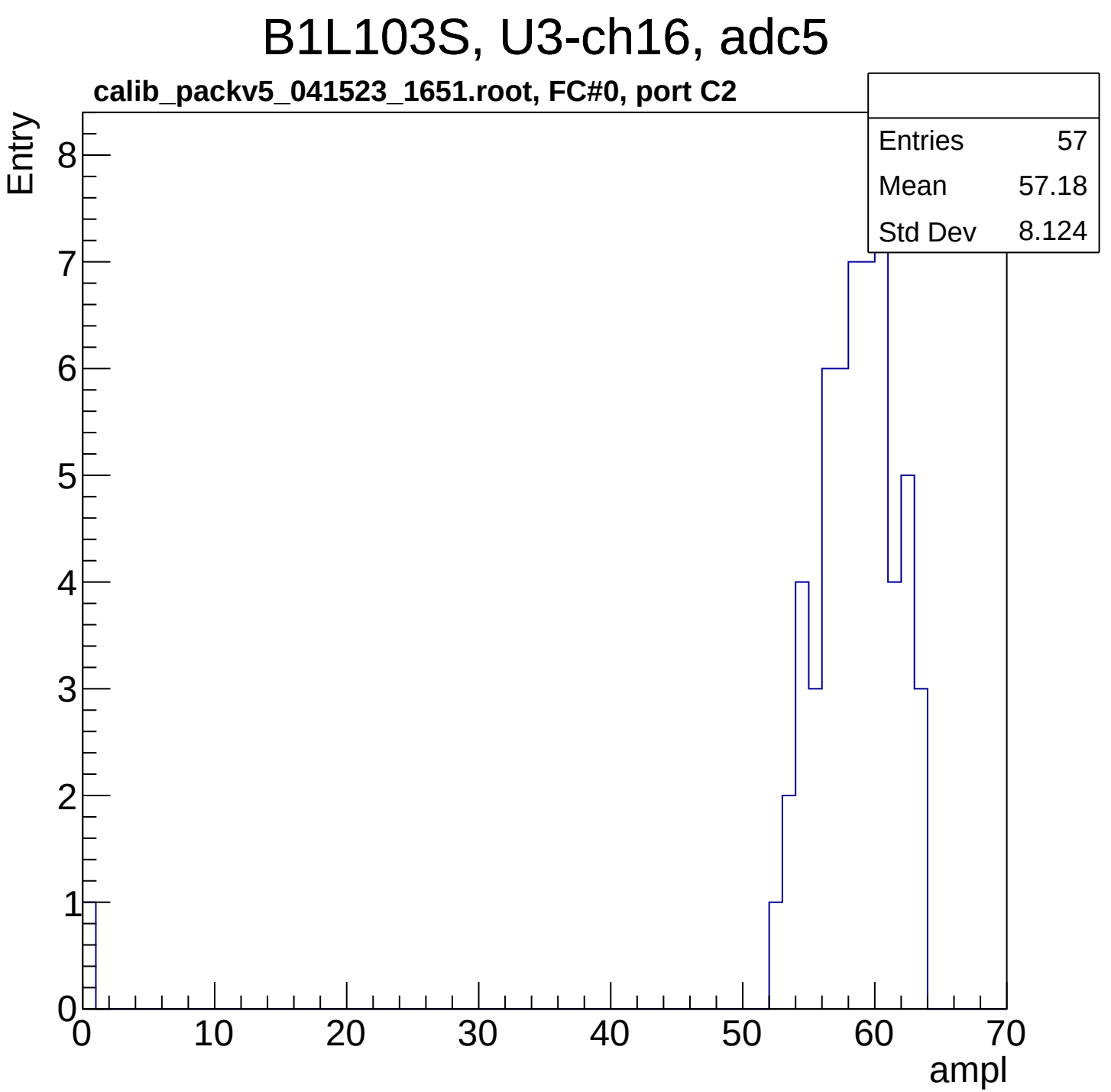
30
40
50
60
70


B1L103S, U3-ch16, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 53.85
Std Dev 3.464
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U3-ch16, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 57.18
Std Dev 8.124
Entry
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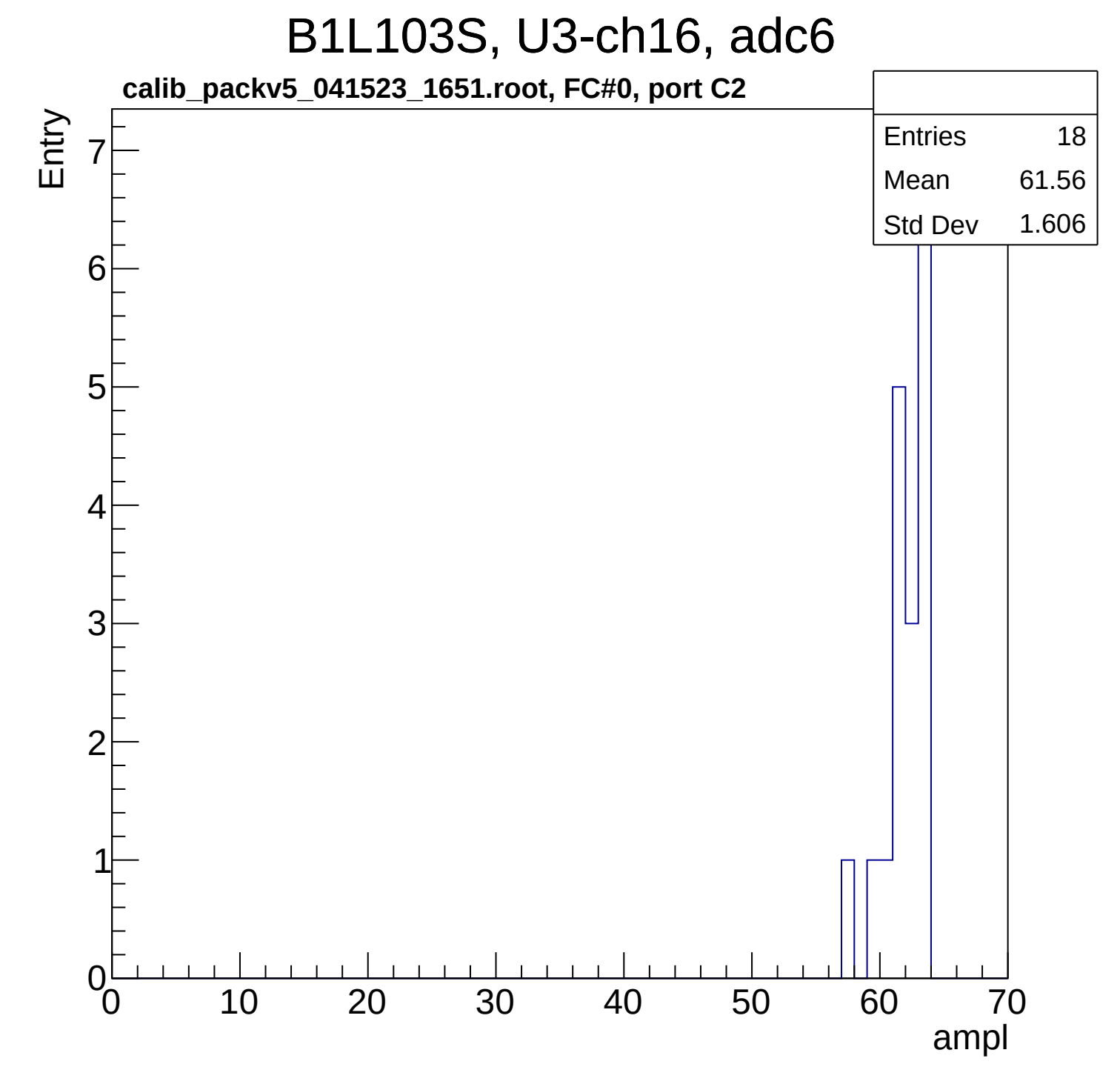
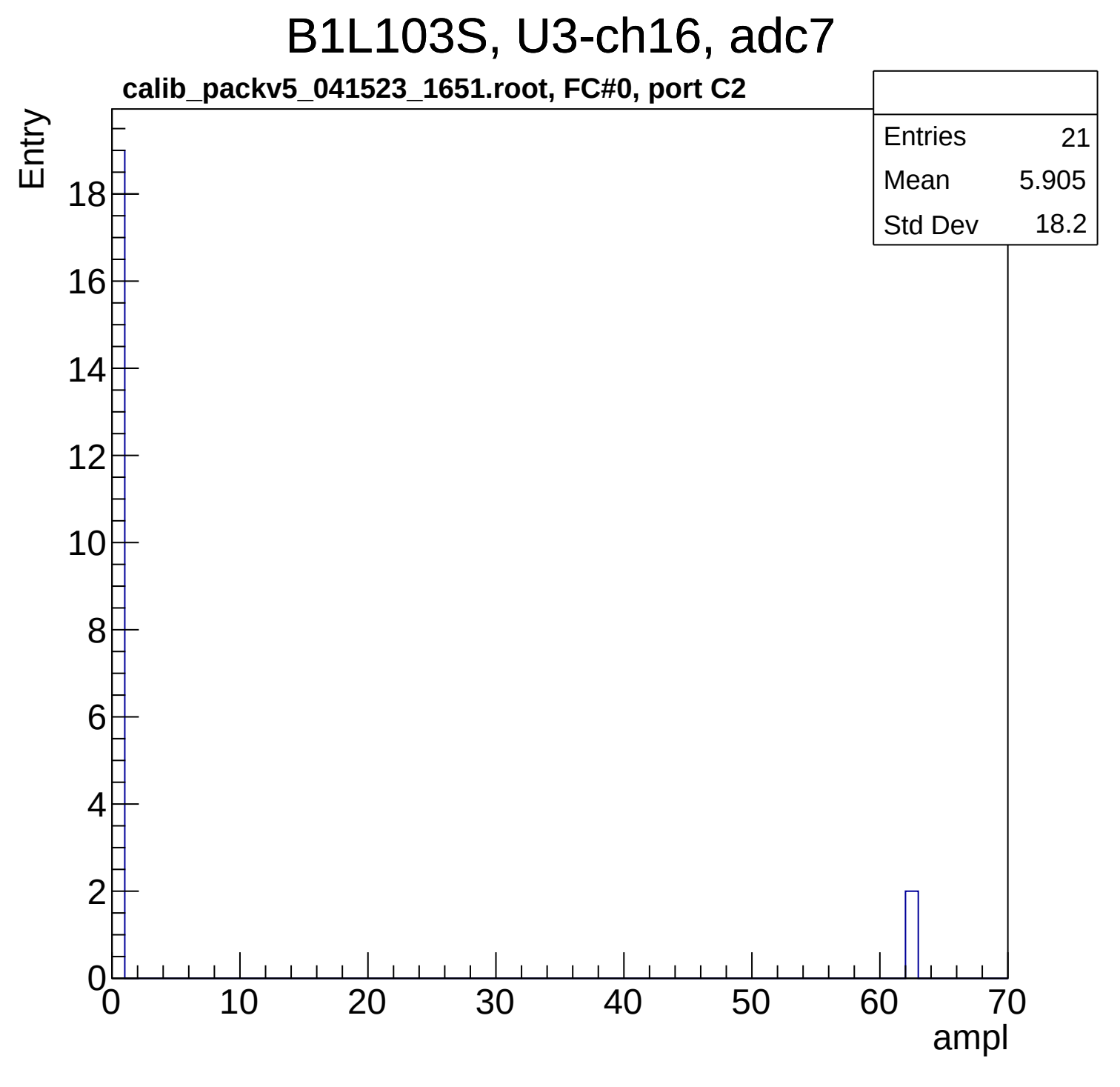
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch16, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 61.56
Std Dev 1.606
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch16, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.905
Std Dev 18.2
Entry
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2
4
6
8
10
12
14
16
18
0
10
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30
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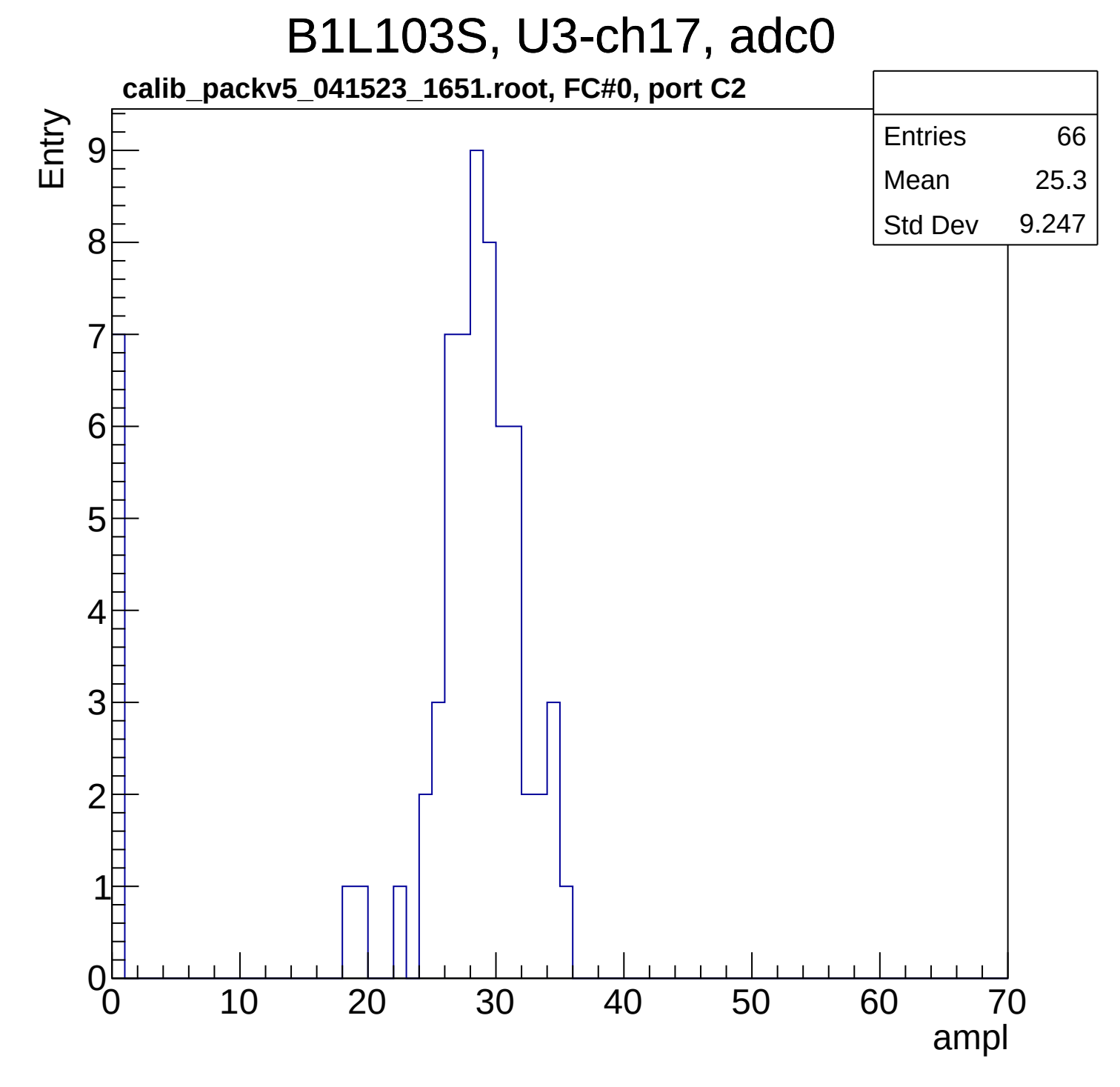
50
60
70
ampl


B1L103S, U3-ch17, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 25.3
Std Dev 9.247
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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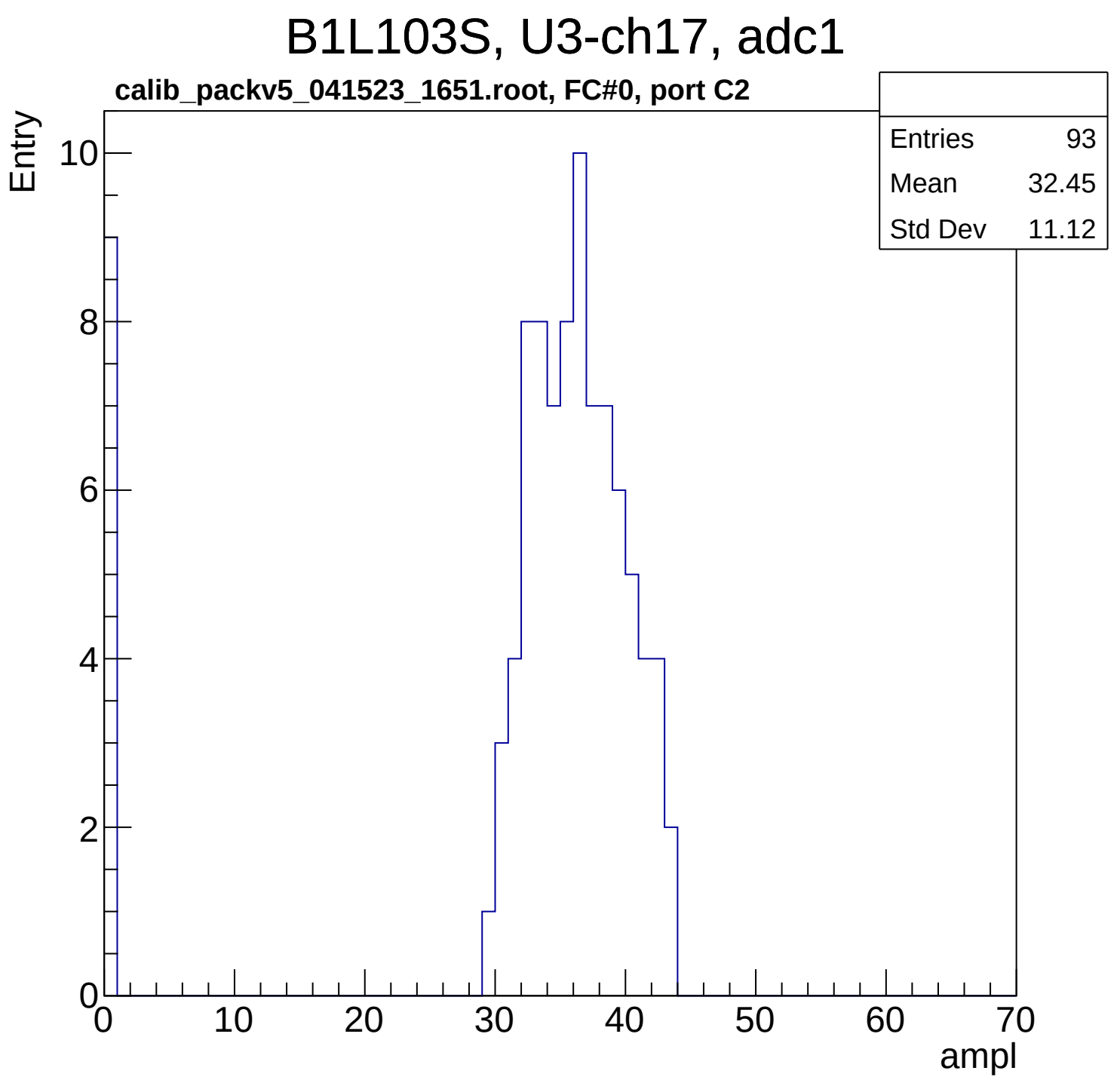
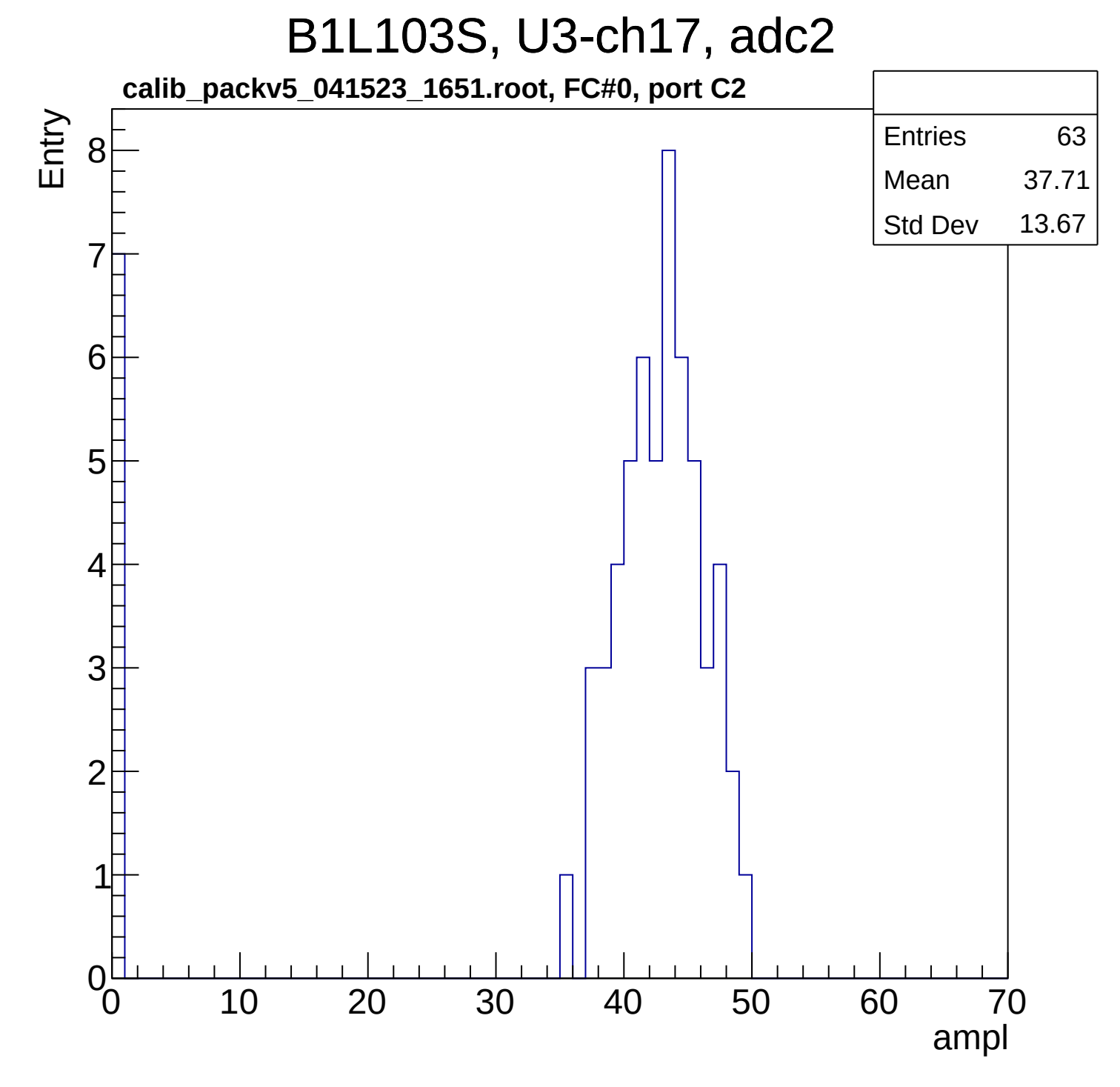

B1L103S, U3-ch17, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 32.45
Std Dev 11.12
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch17, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 37.71
Std Dev 13.67
Entry
ampl
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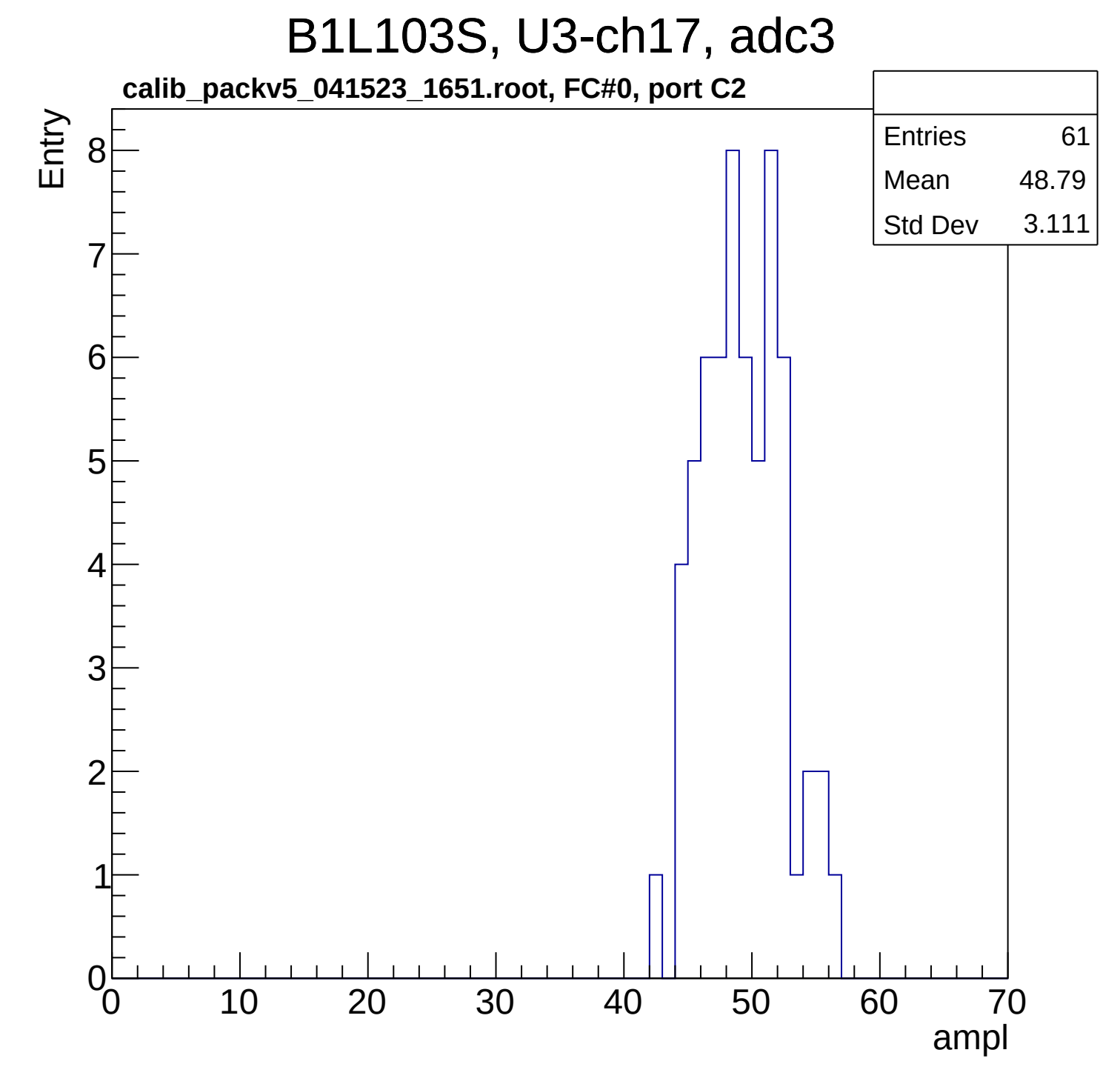
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch17, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 48.79
Std Dev 3.111
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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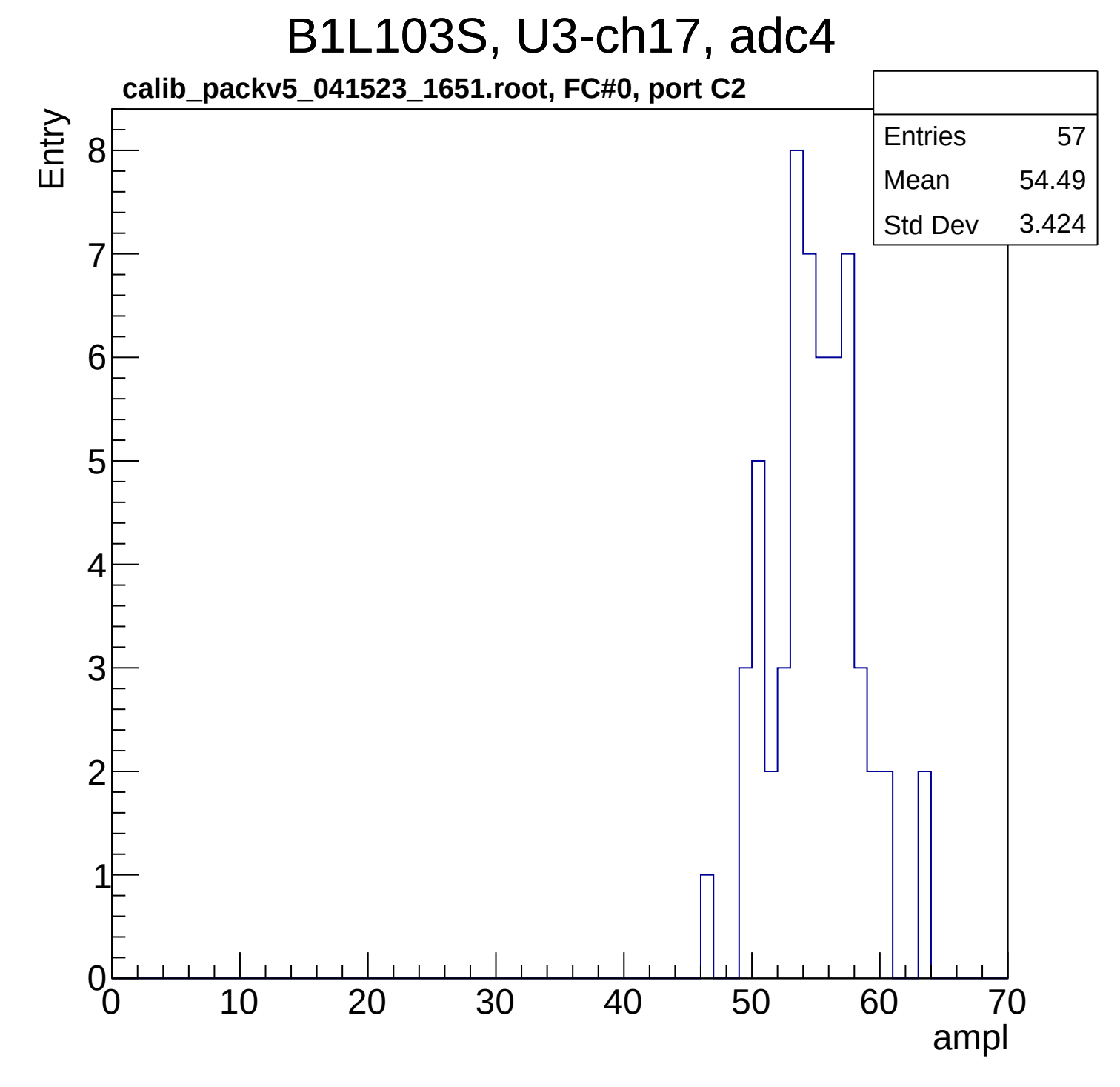
B1L103S, U3-ch17, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 54.49
Std Dev 3.424
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
50
60
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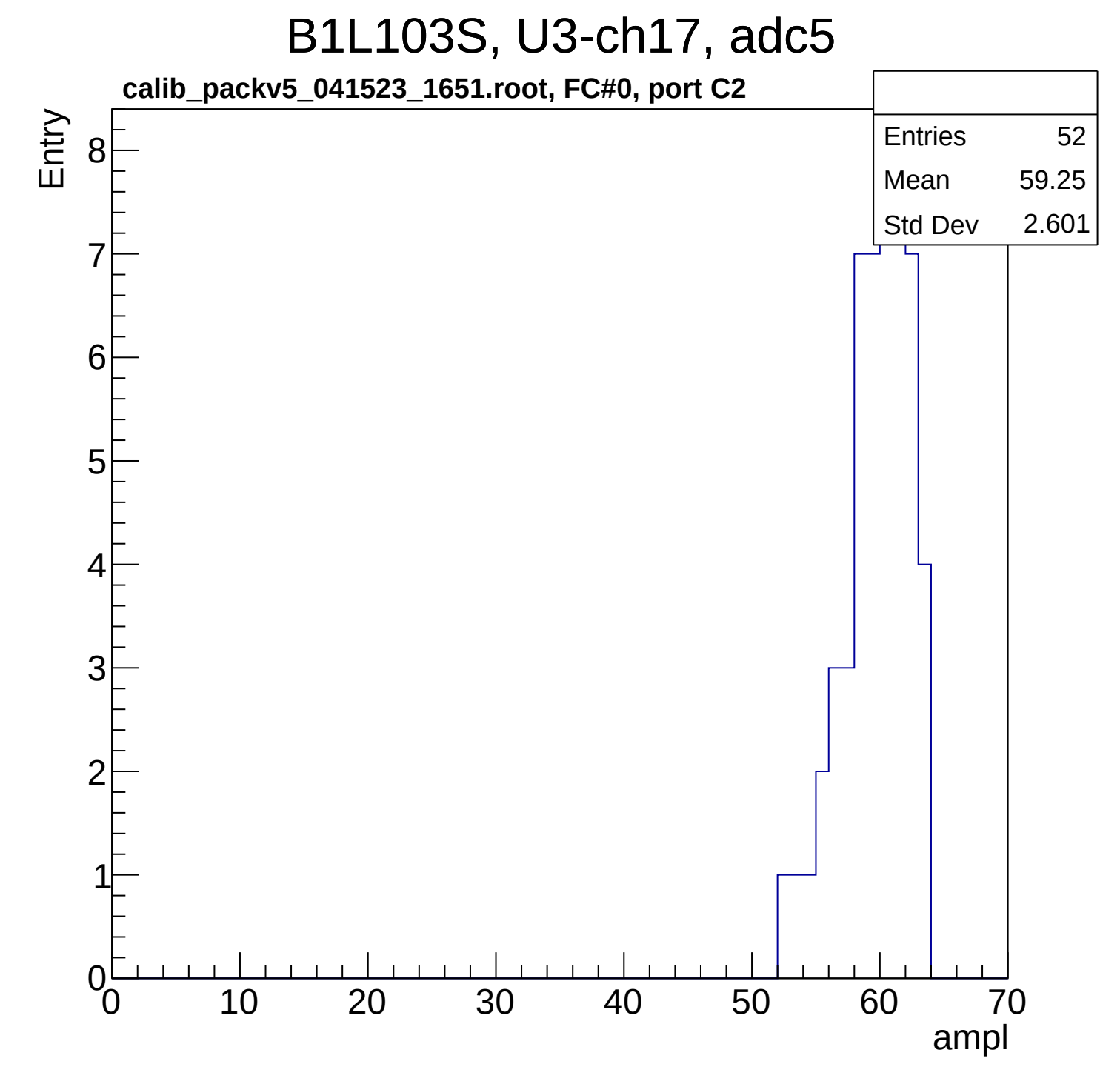
B1L103S, U3-ch17, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 59.25
Std Dev 2.601
Entry
ampl
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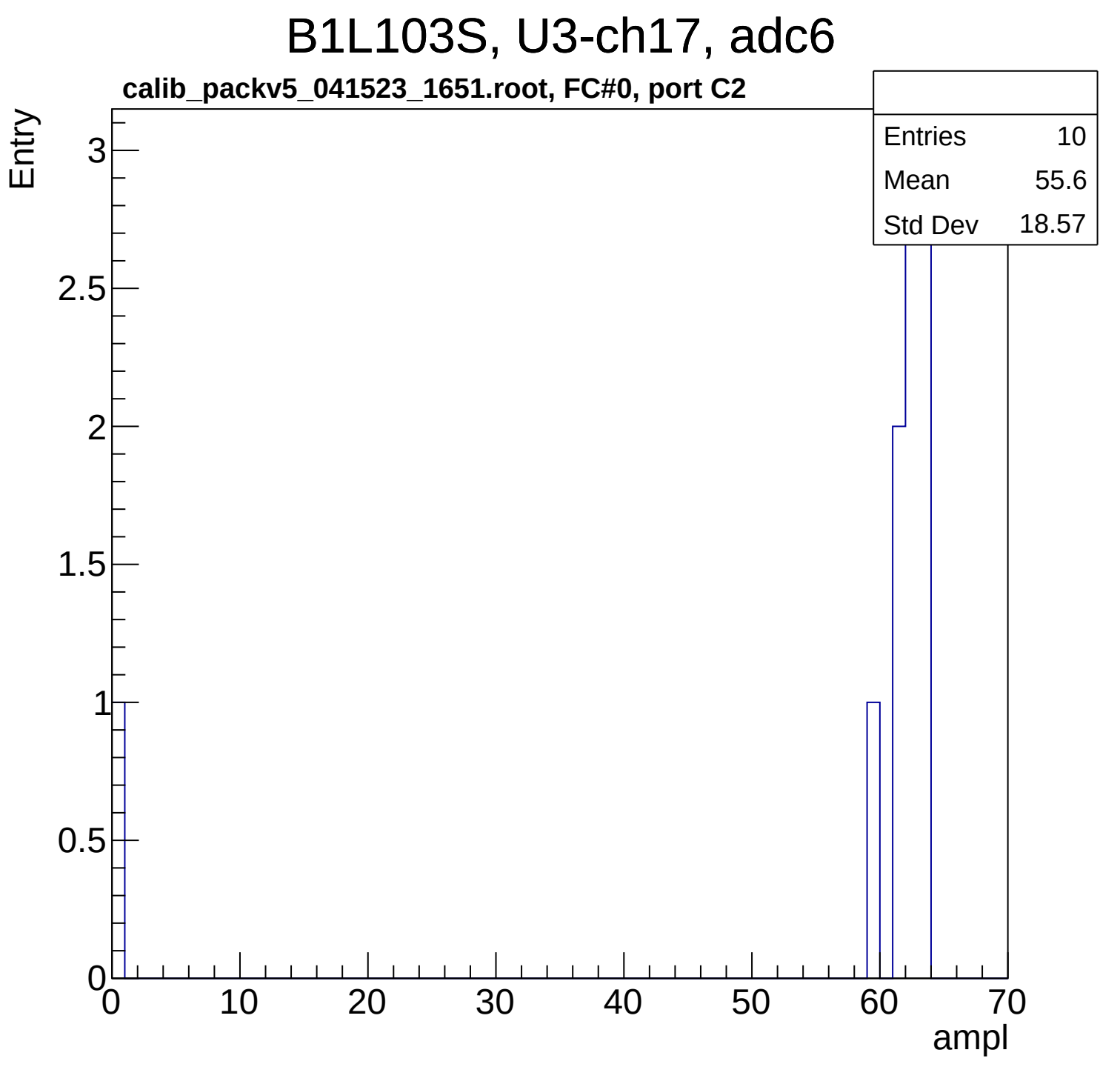
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch17, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 55.6
Std Dev 18.57
Entry
ampl
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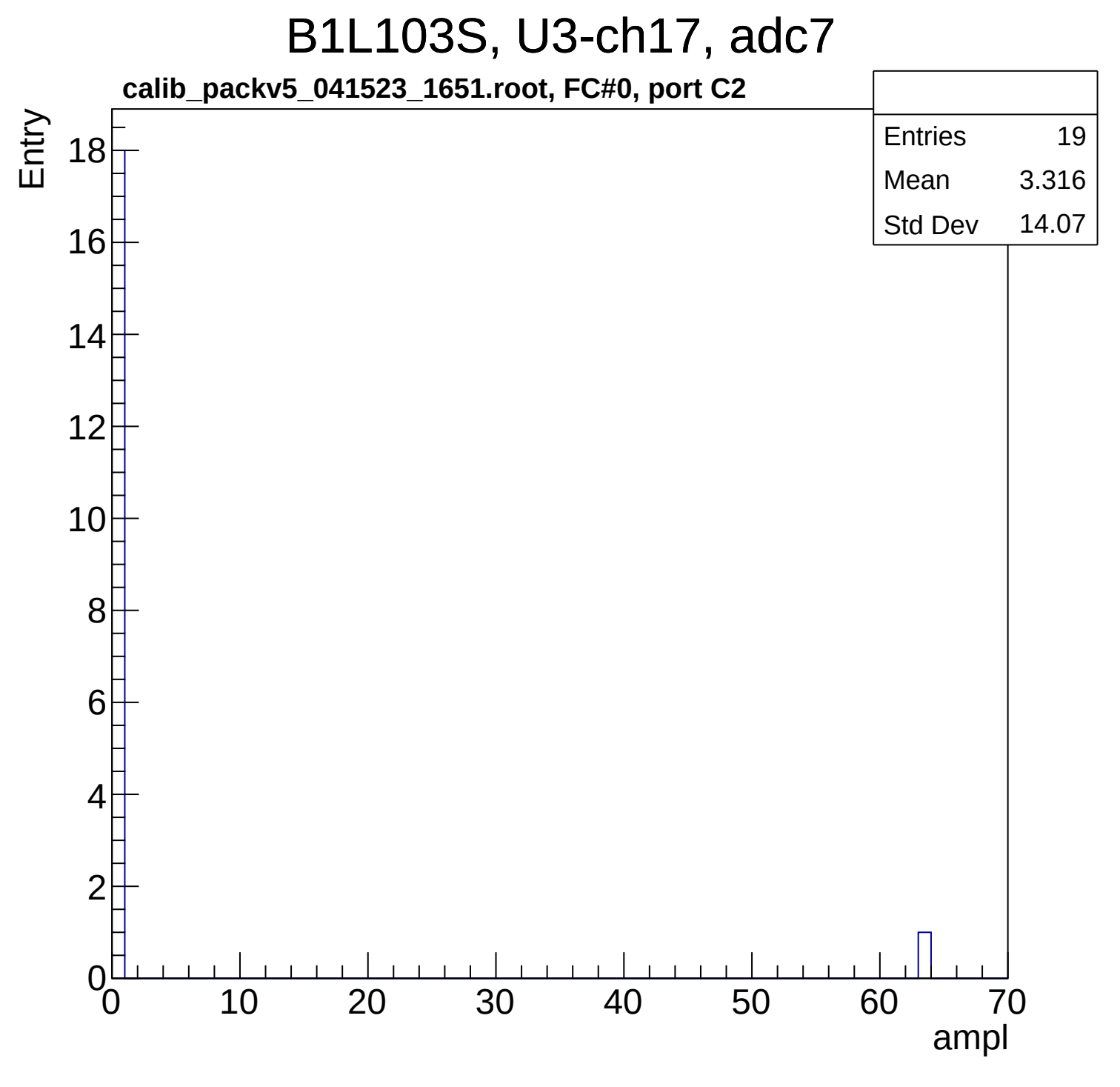
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U3-ch17, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.316
Std Dev 14.07
Entry
0
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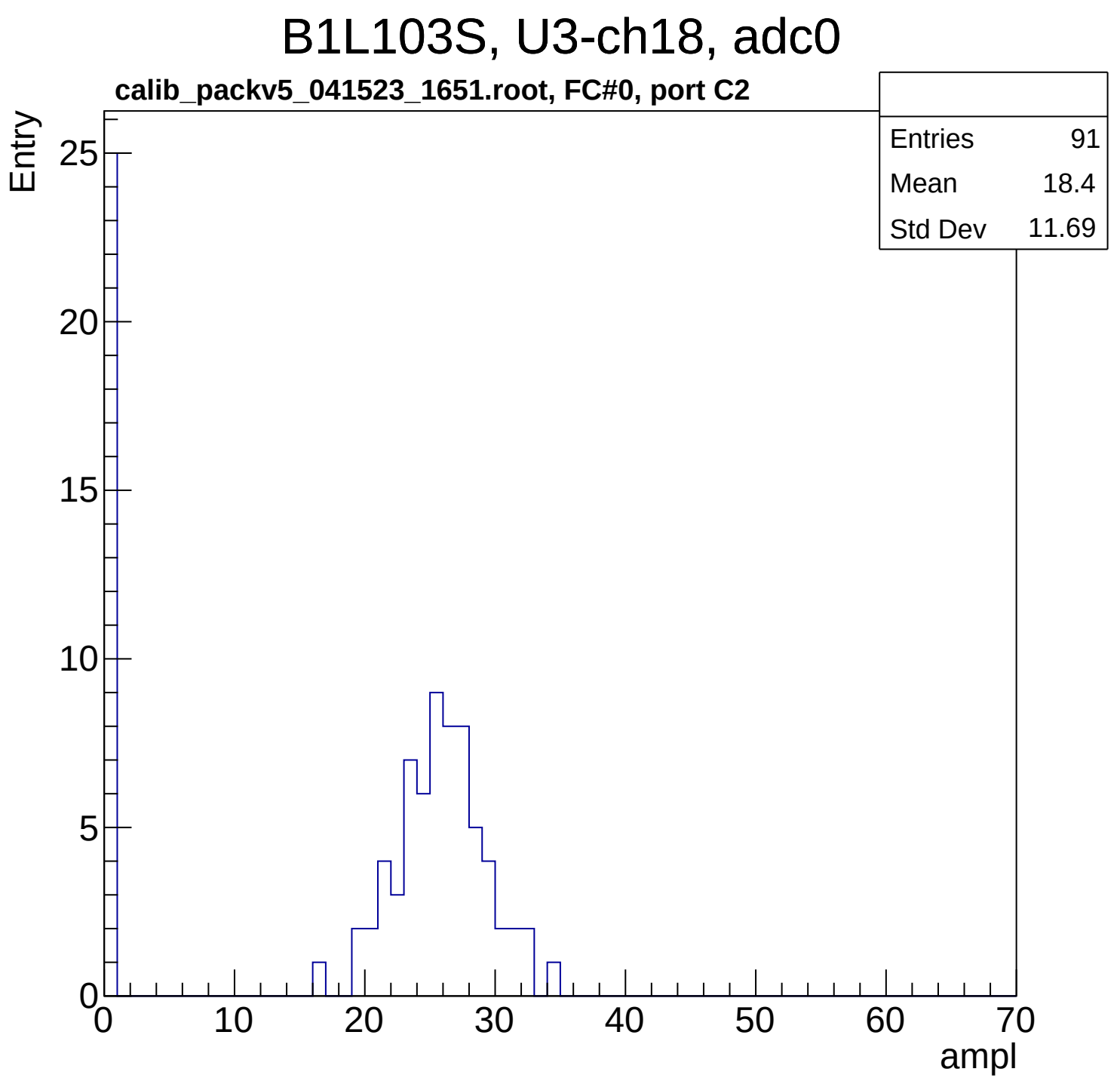
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch18, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 18.4
Std Dev 11.69
Entry
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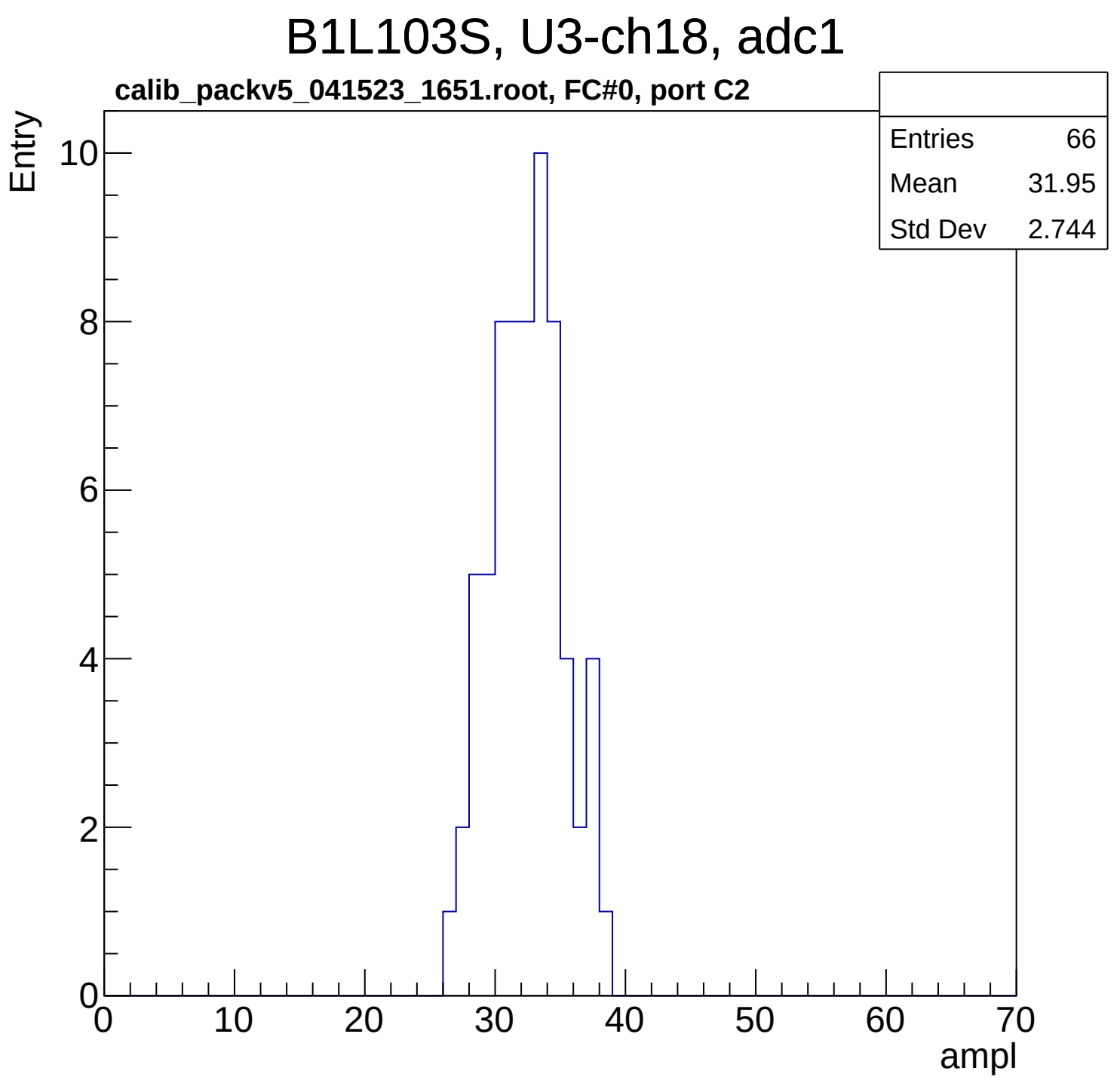
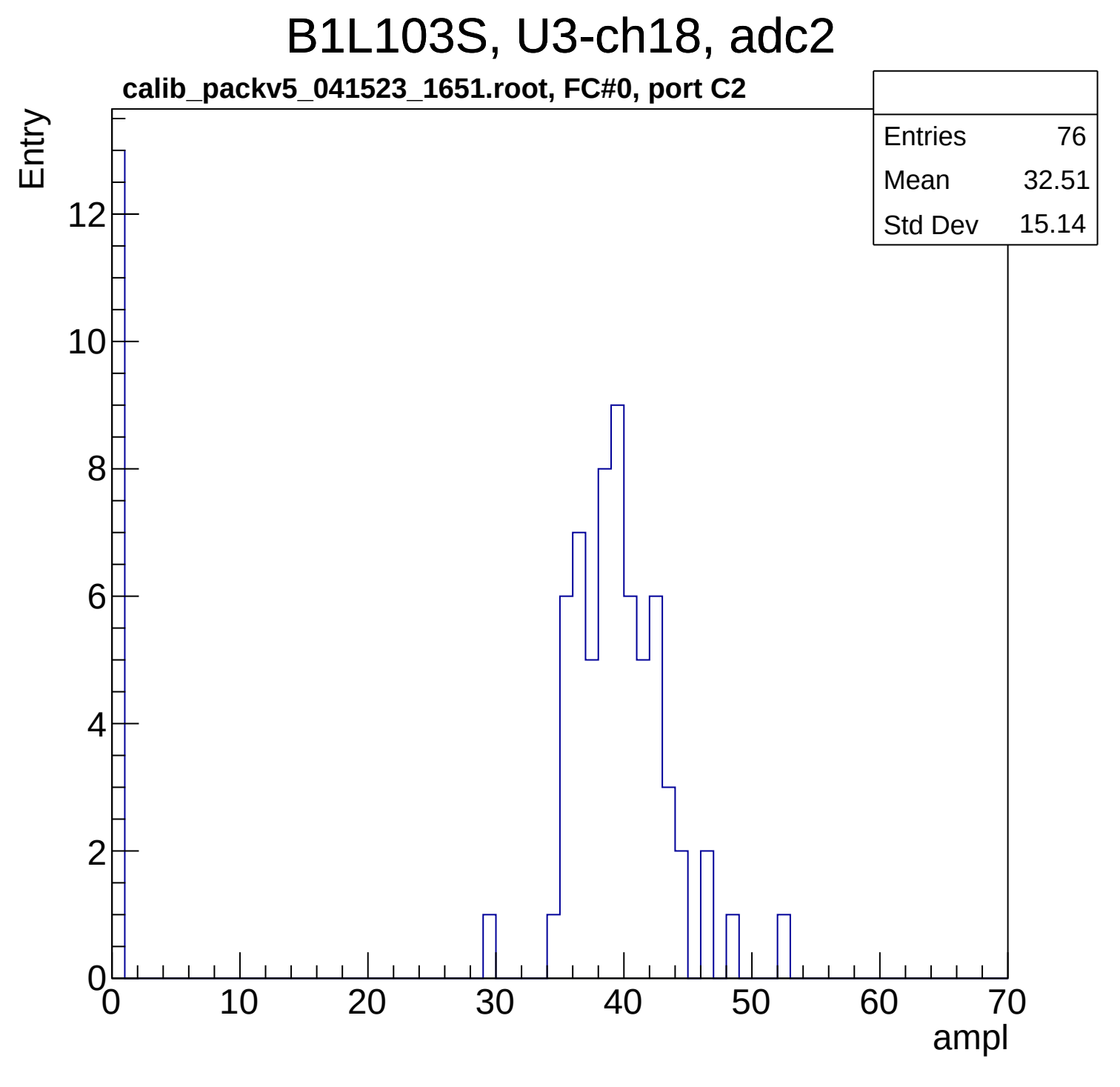
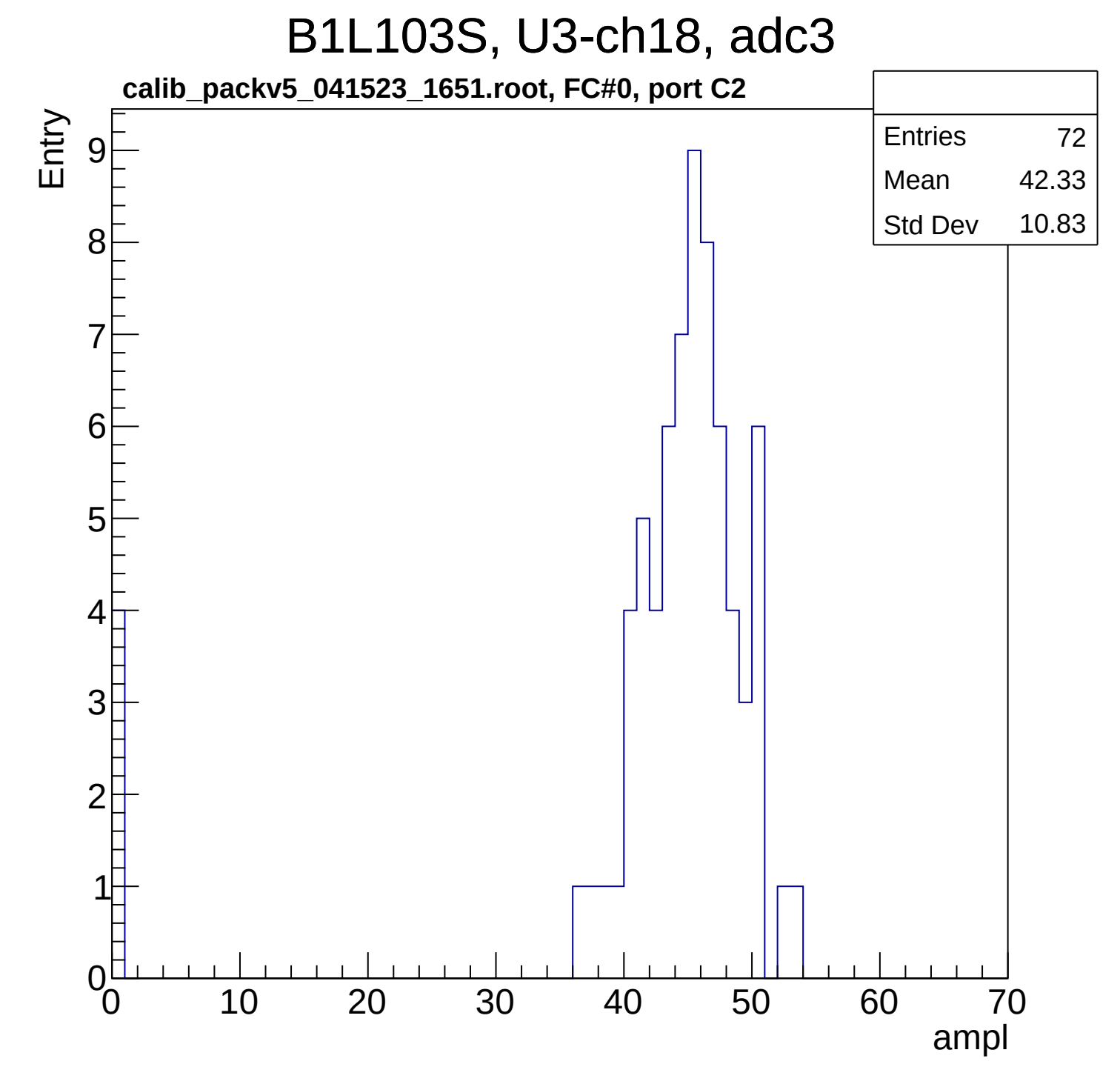
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch18, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 31.95
Std Dev 2.744
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch18, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 32.51
Std Dev 15.14
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U3-ch18, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 42.33
Std Dev 10.83
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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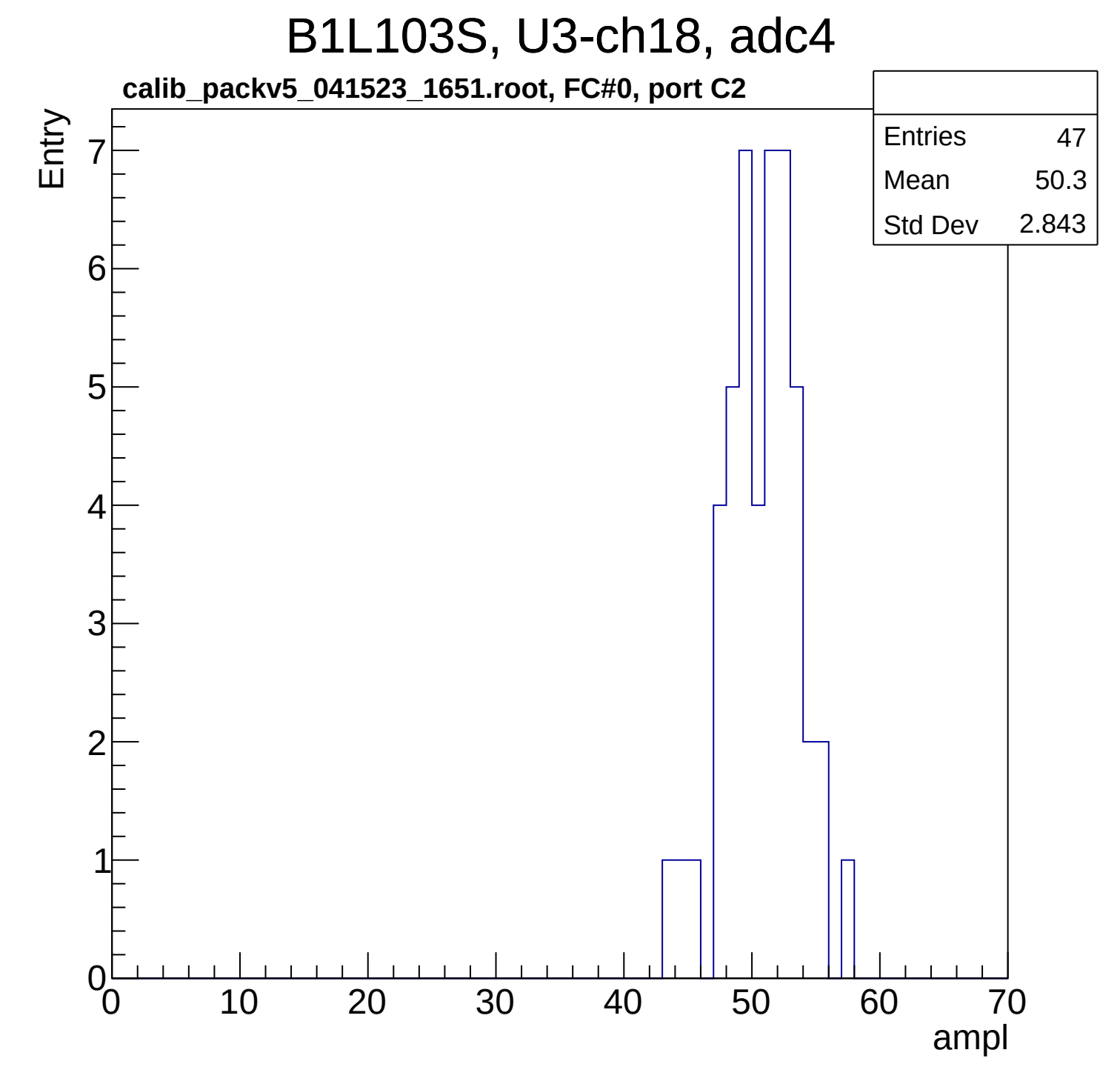
40
50
60
70


B1L103S, U3-ch18, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 50.3
Std Dev 2.843
Entry
ampl
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1
2
3
4
5
6
7
0
10
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40
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60
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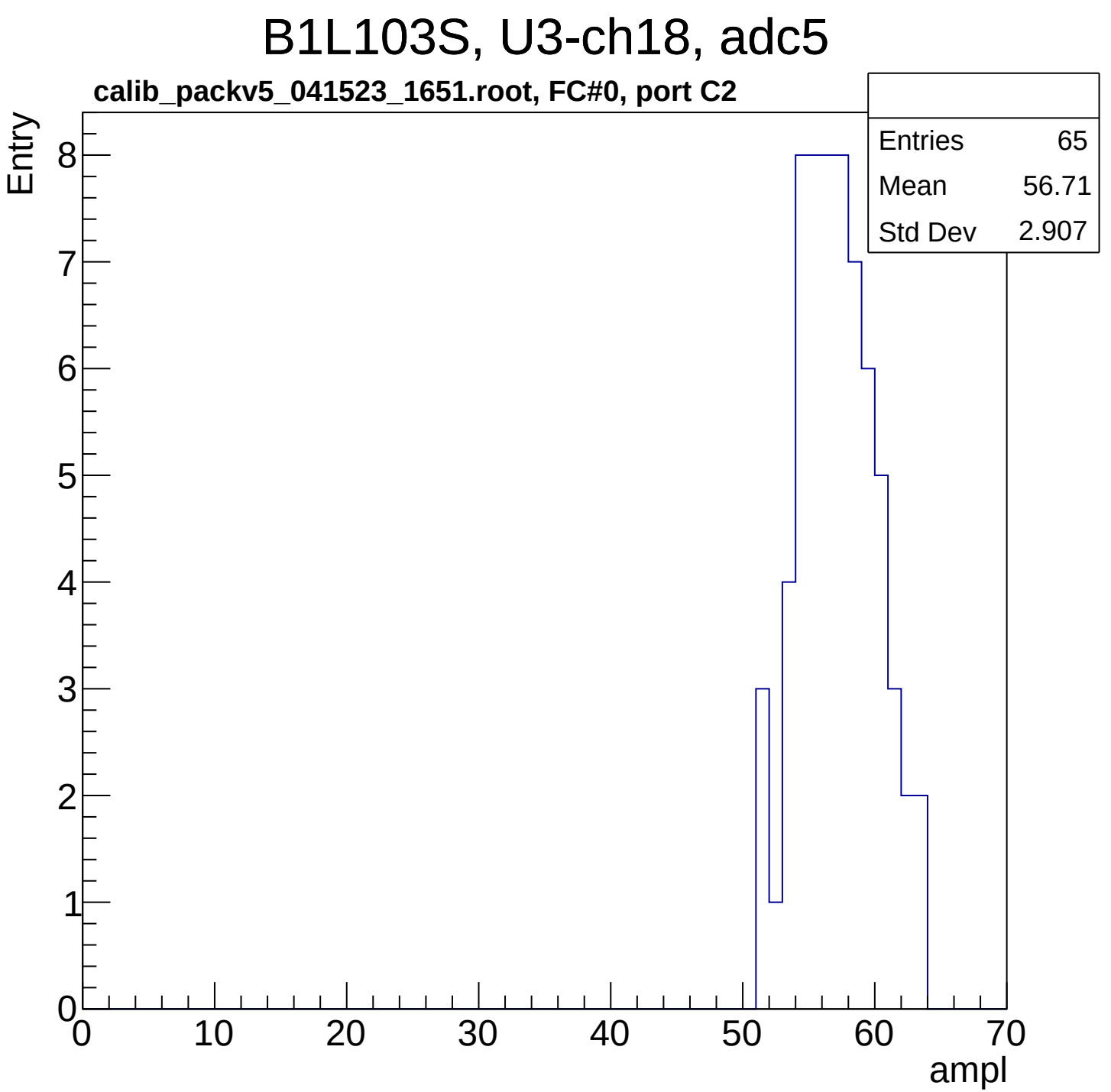
B1L103S, U3-ch18, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 56.71
Std Dev 2.907
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
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40
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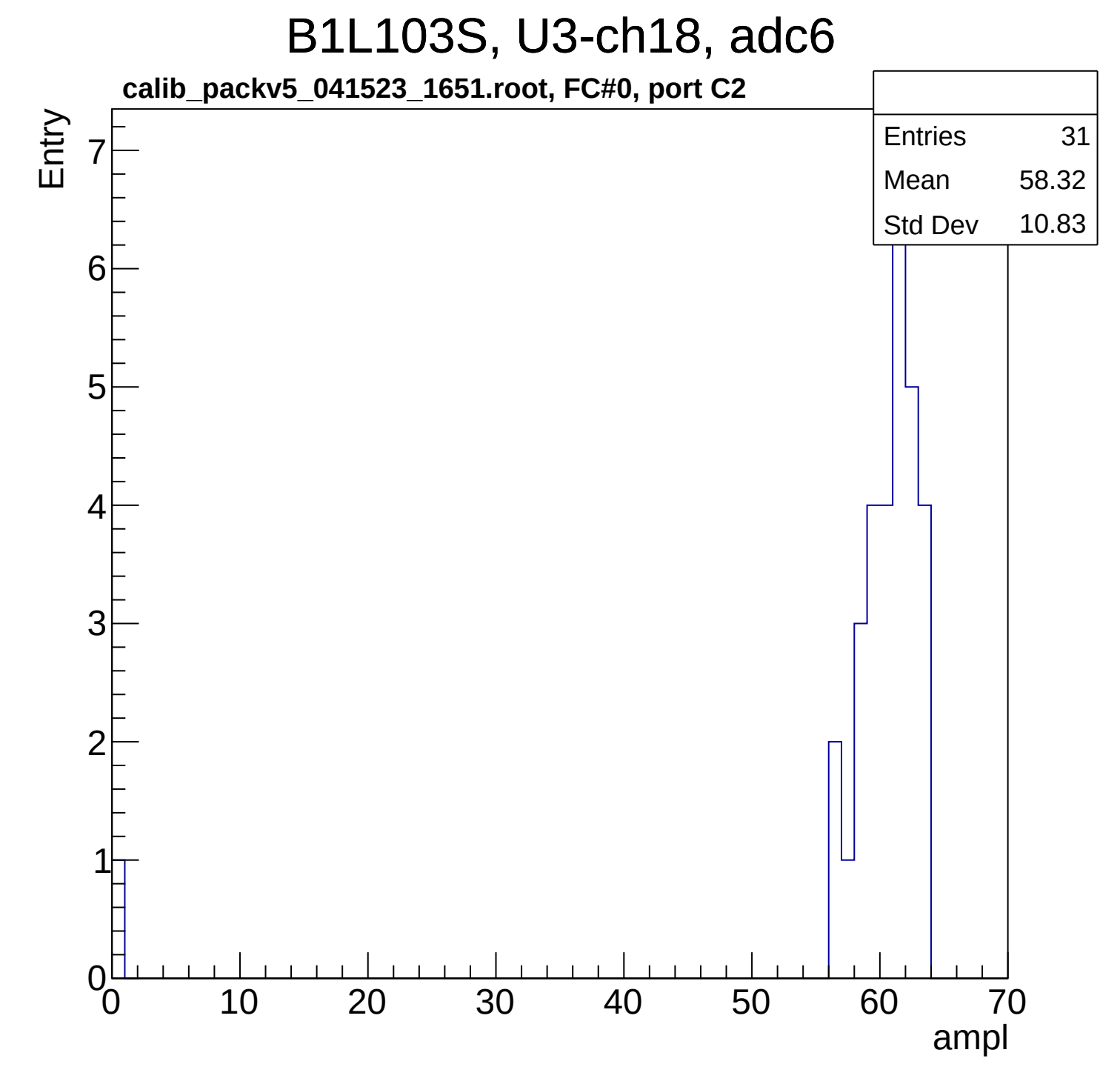
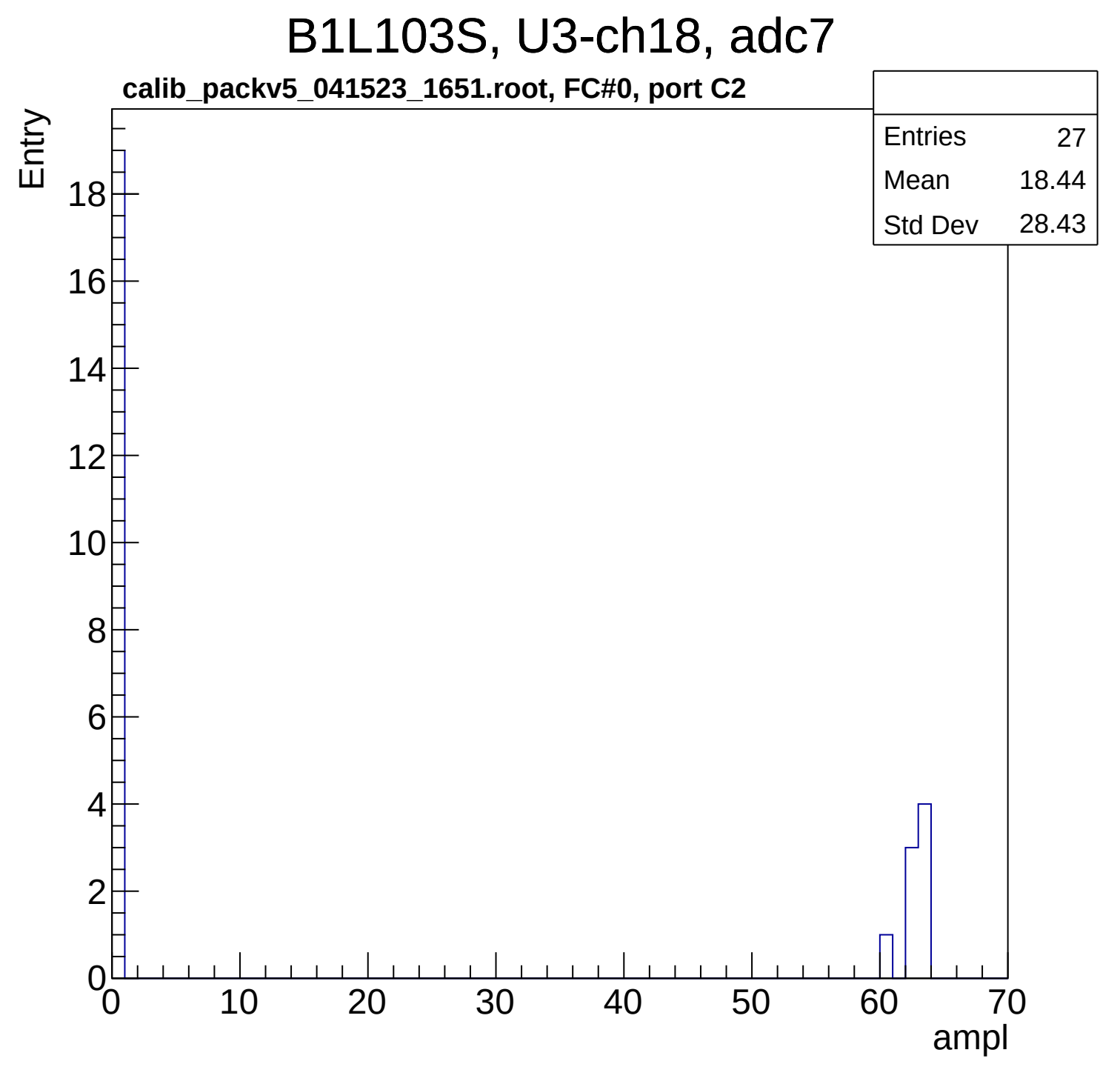
60
70


B1L103S, U3-ch18, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 58.32
Std Dev 10.83
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch18, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 18.44
Std Dev 28.43
Entry
ampl
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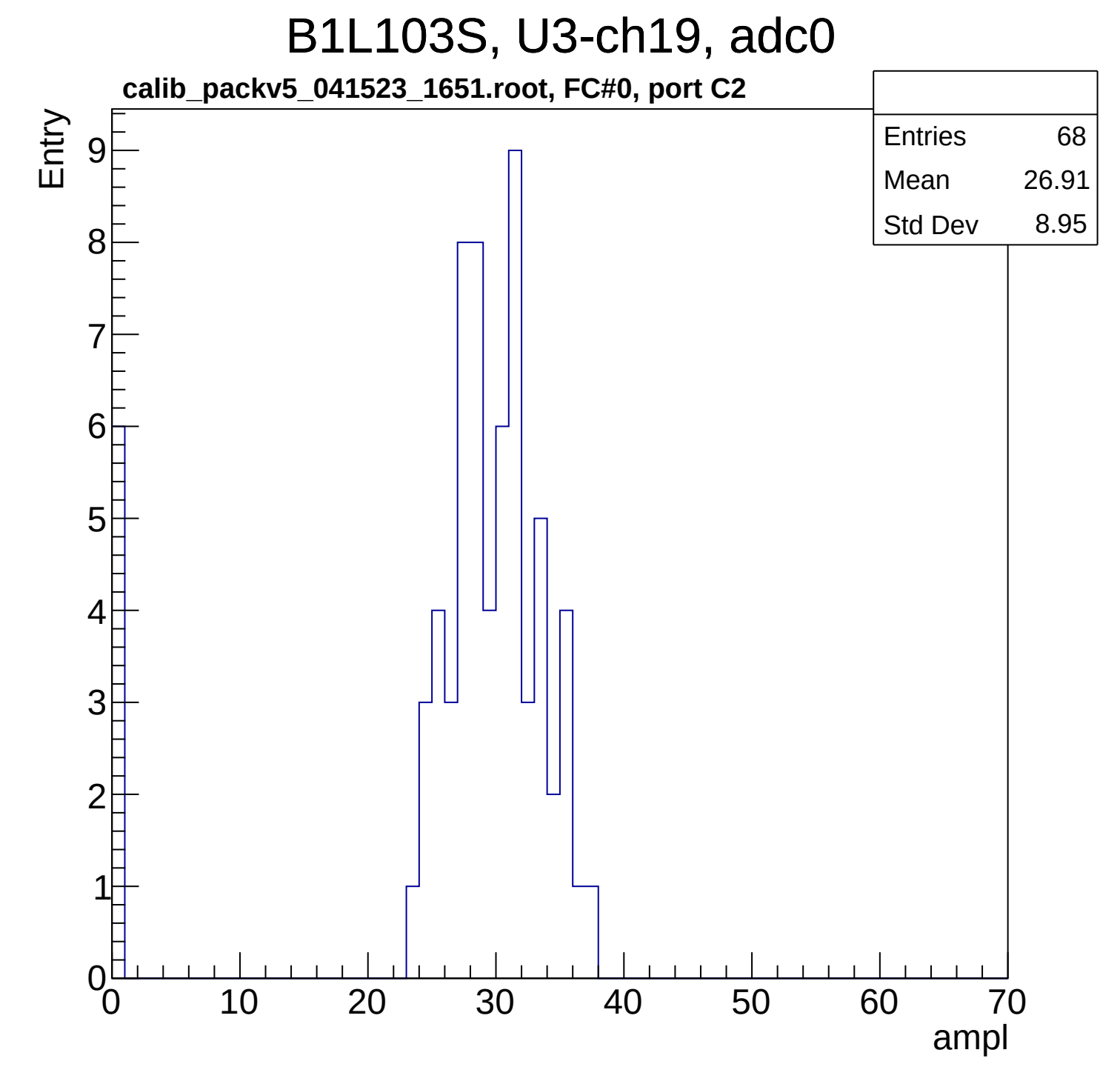
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L103S, U3-ch19, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 26.91
Std Dev 8.95
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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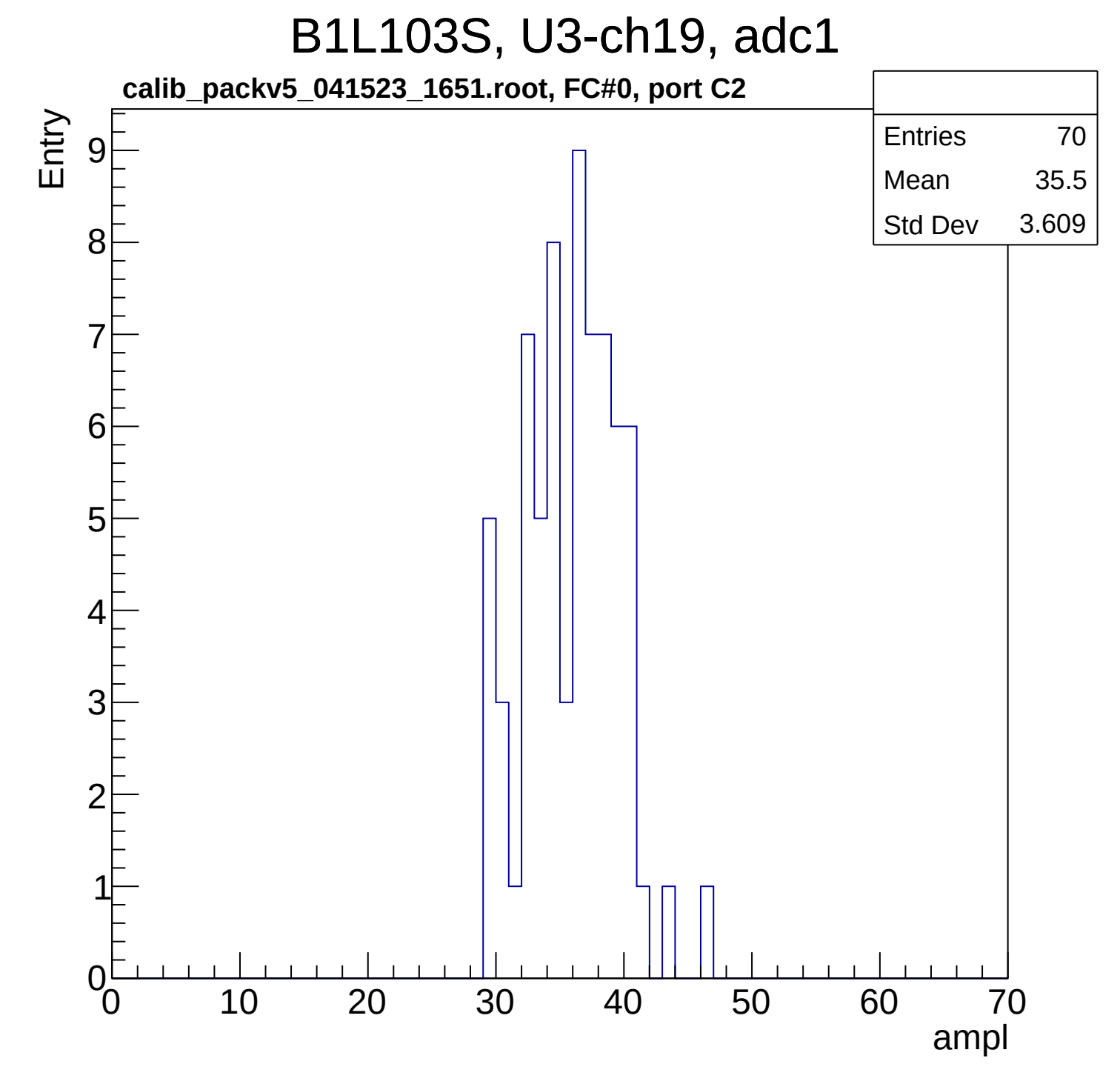
40
50
60
70


B1L103S, U3-ch19, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 35.5
Std Dev 3.609
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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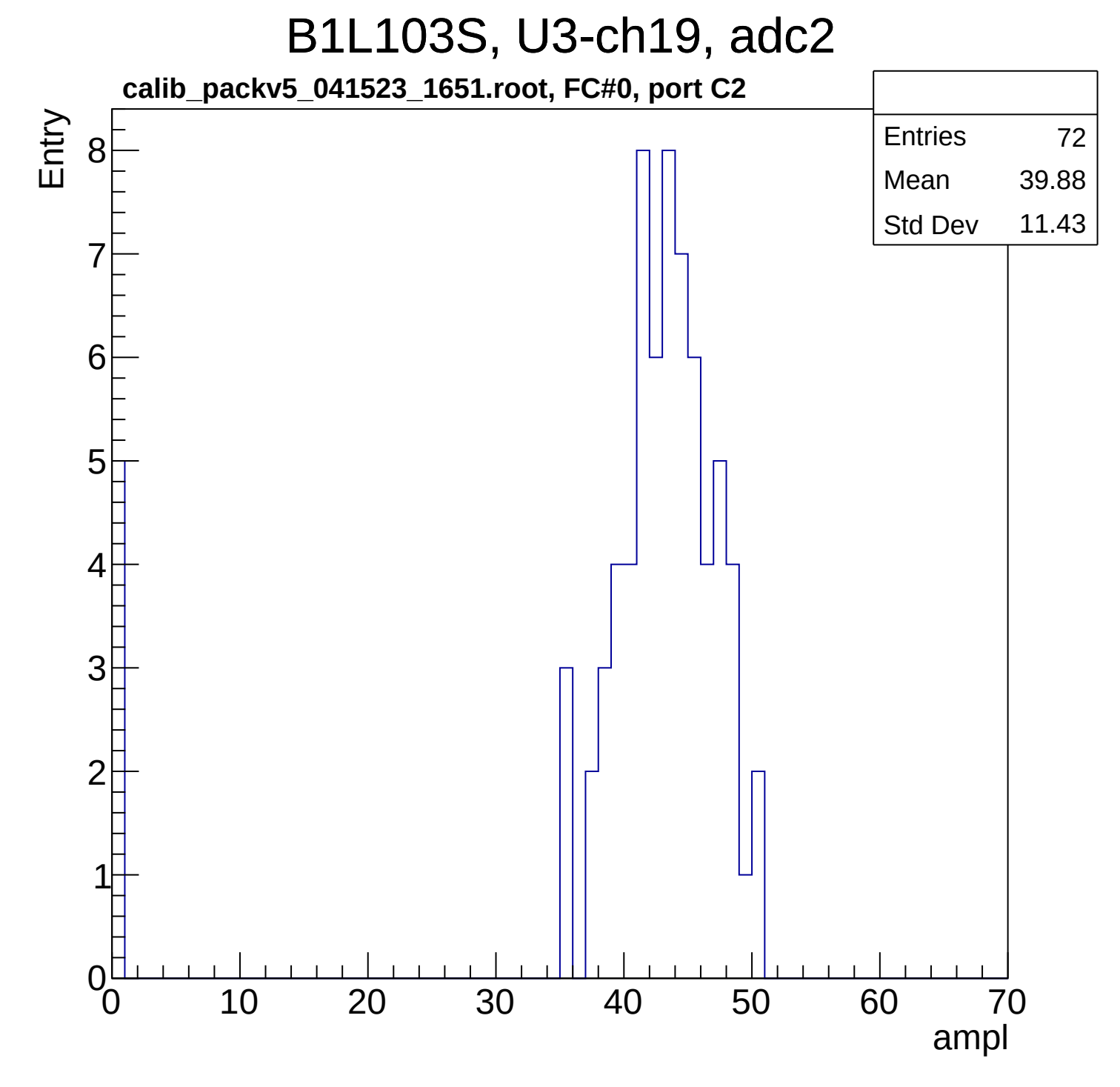
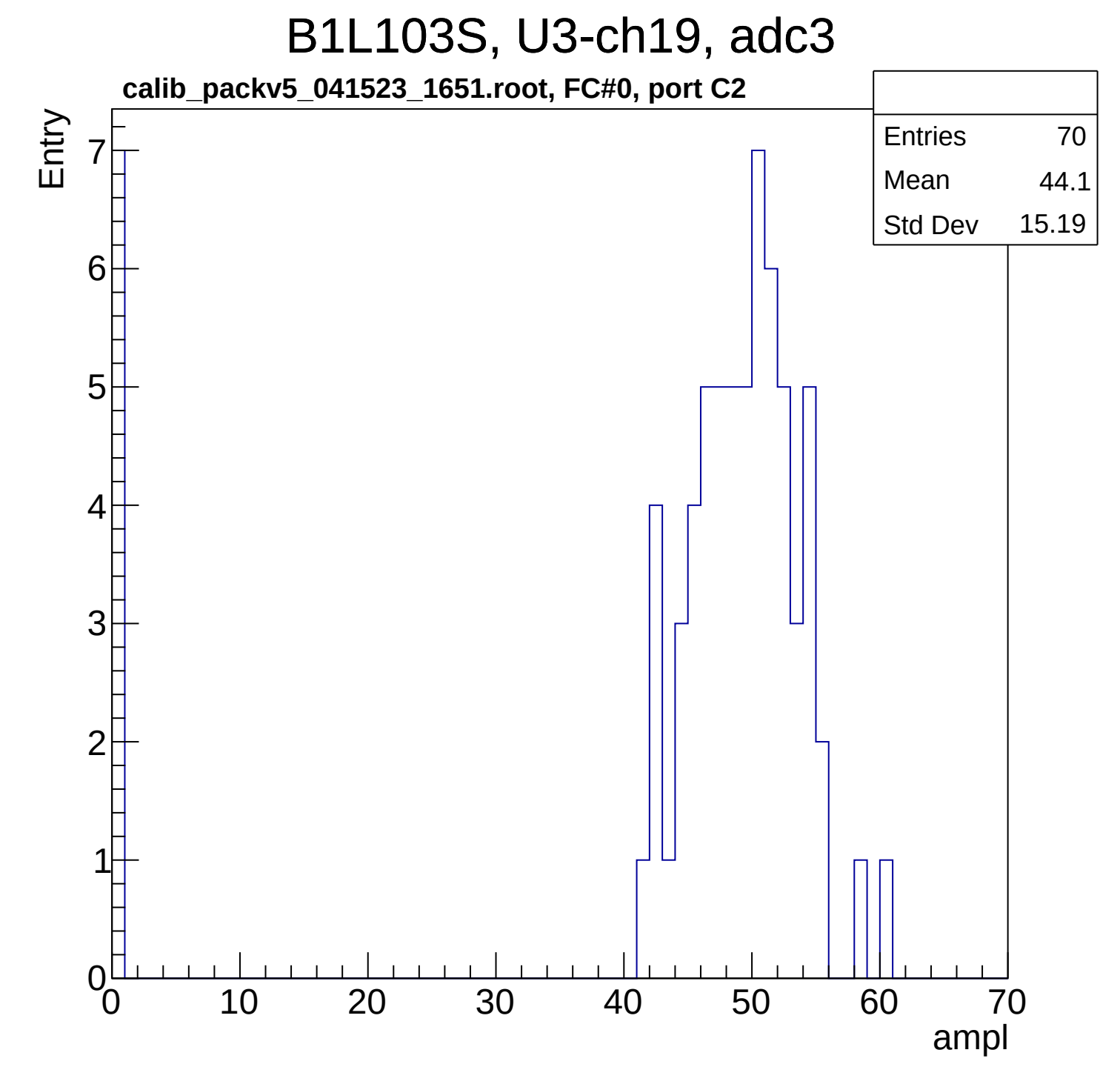
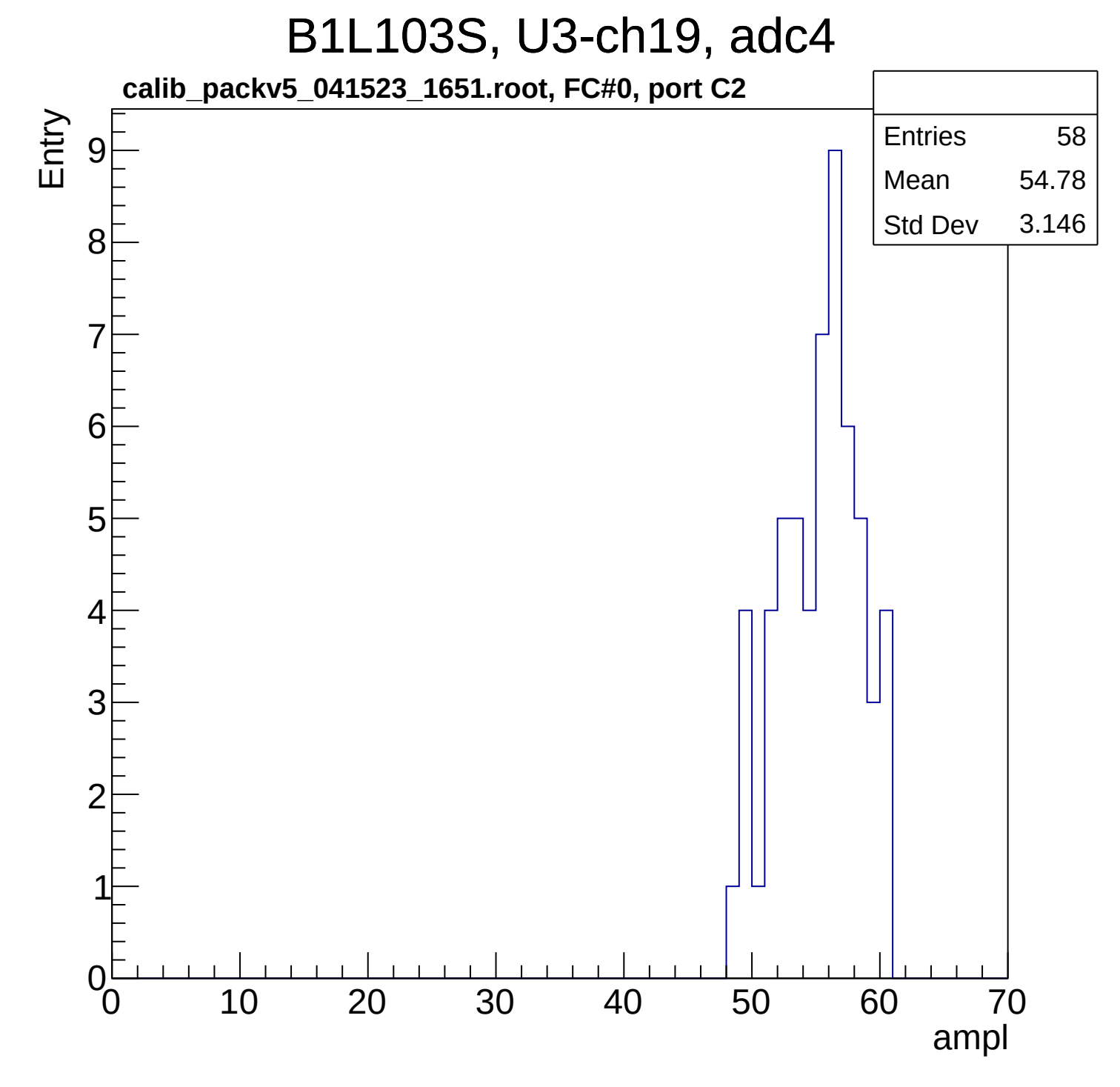
40
50
60
70


B1L103S, U3-ch19, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 39.88
Std Dev 11.43
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch19, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 44.1
Std Dev 15.19
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch19, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 54.78
Std Dev 3.146
Entry
ampl
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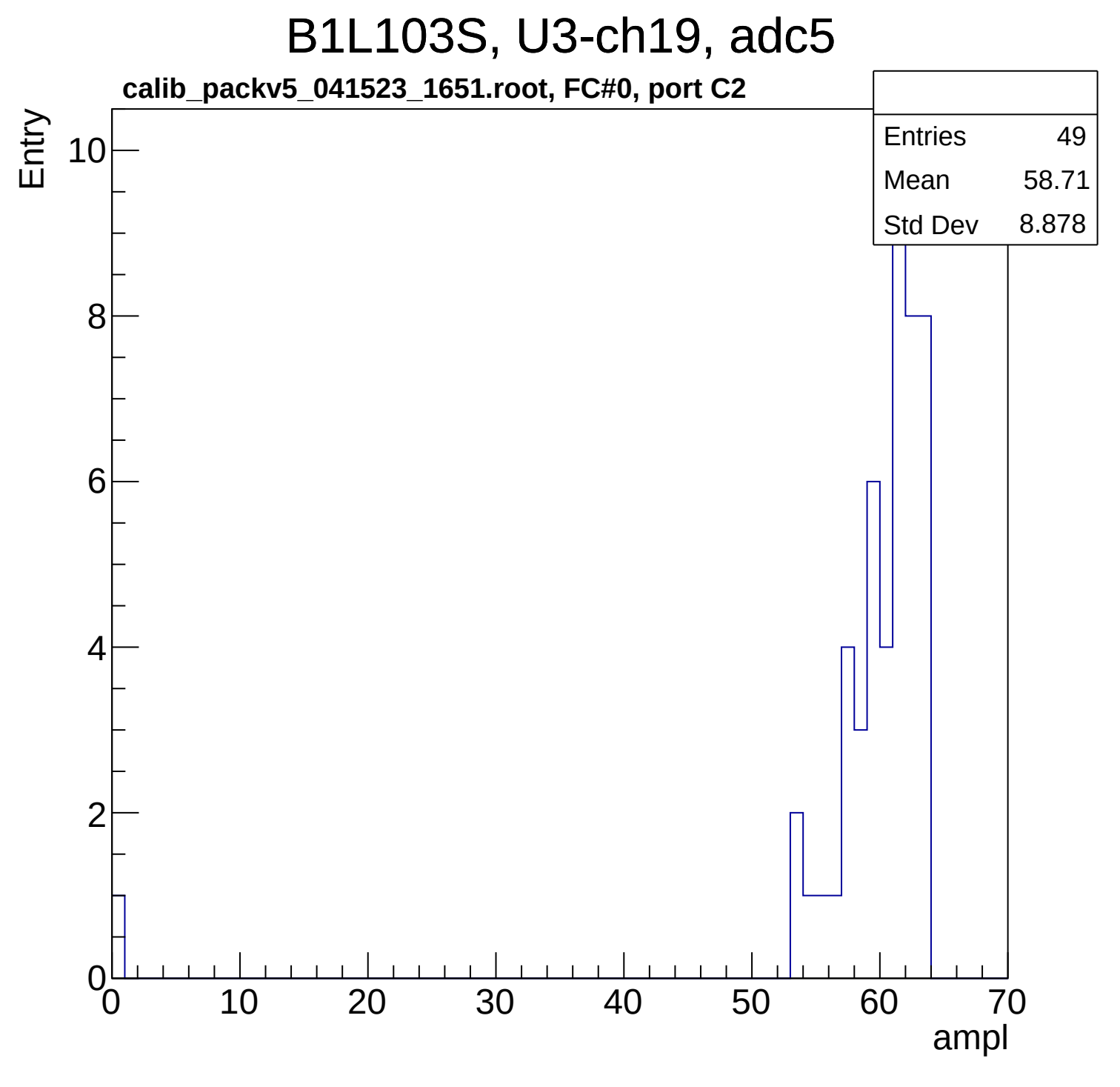
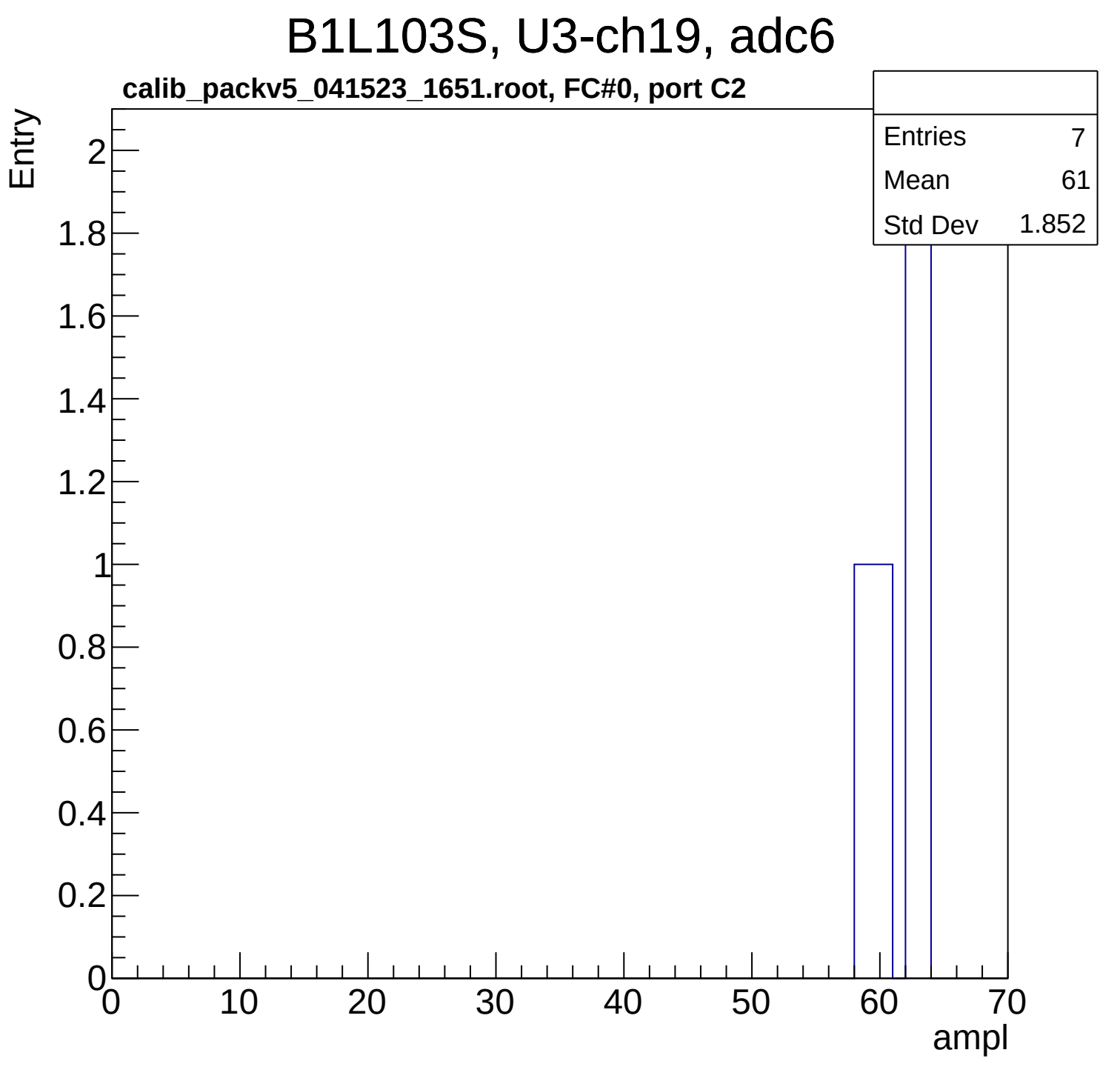
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch19, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 58.71
Std Dev 8.878
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U3-ch19, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 61
Std Dev 1.852
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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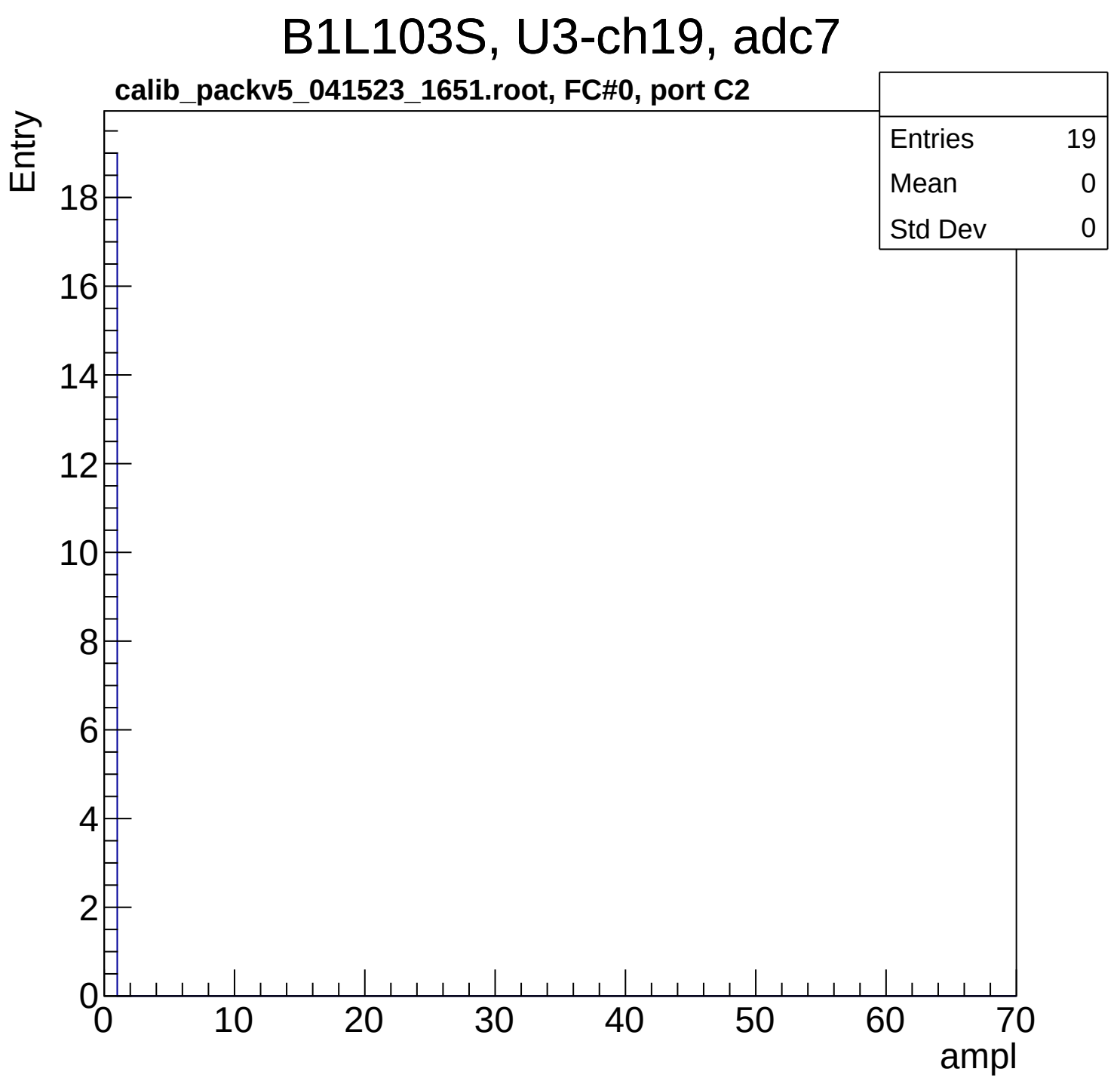
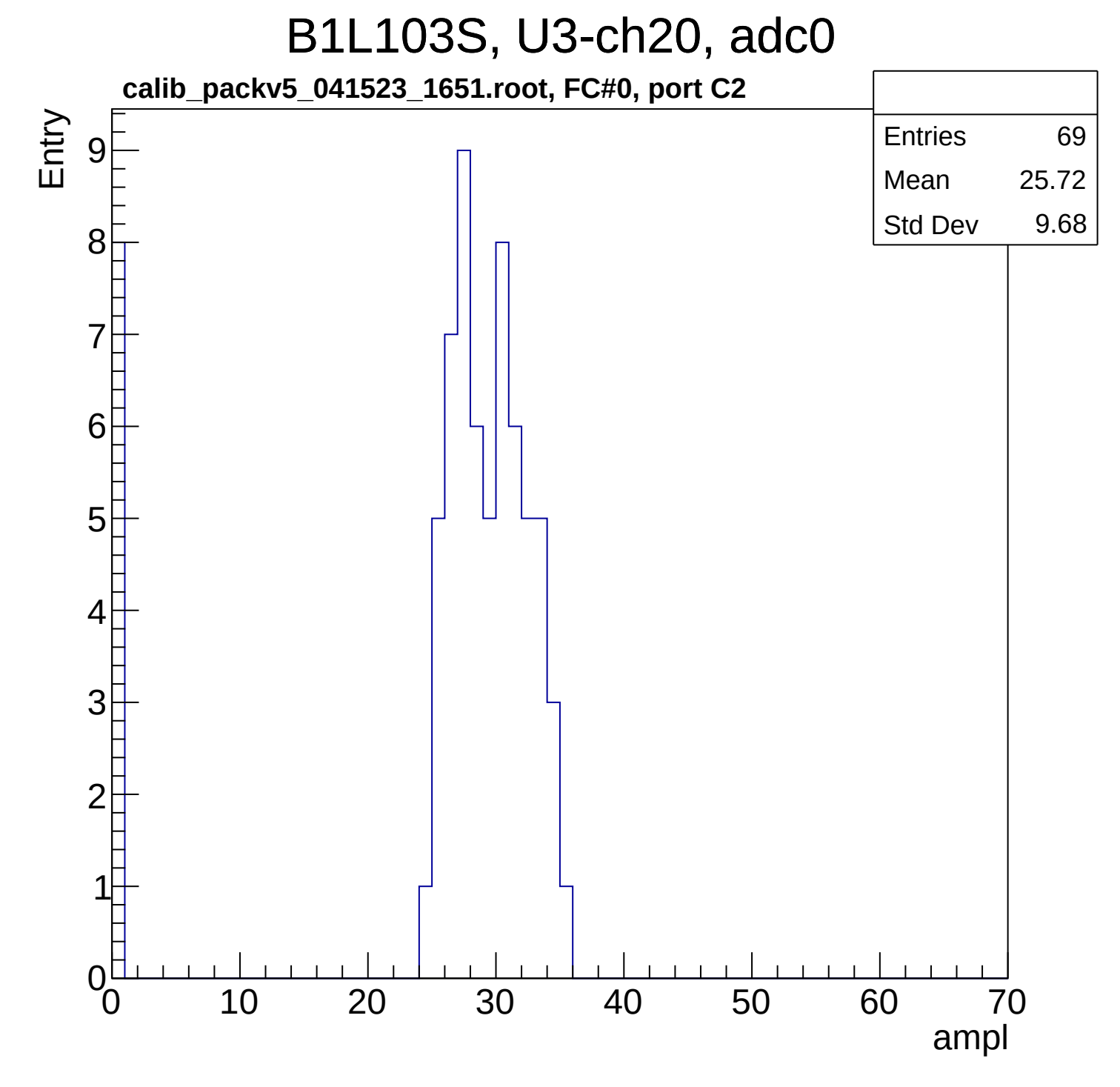
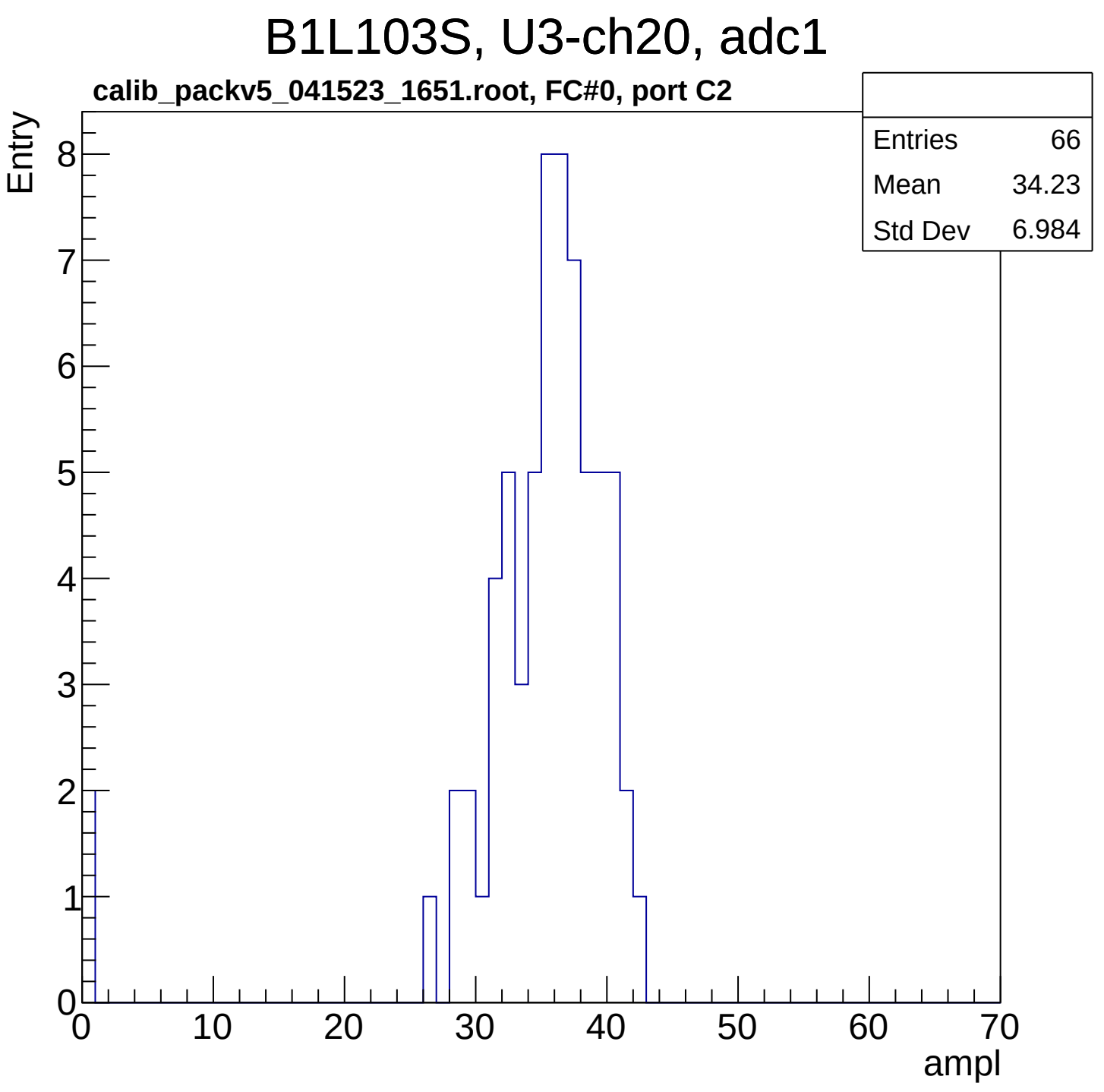
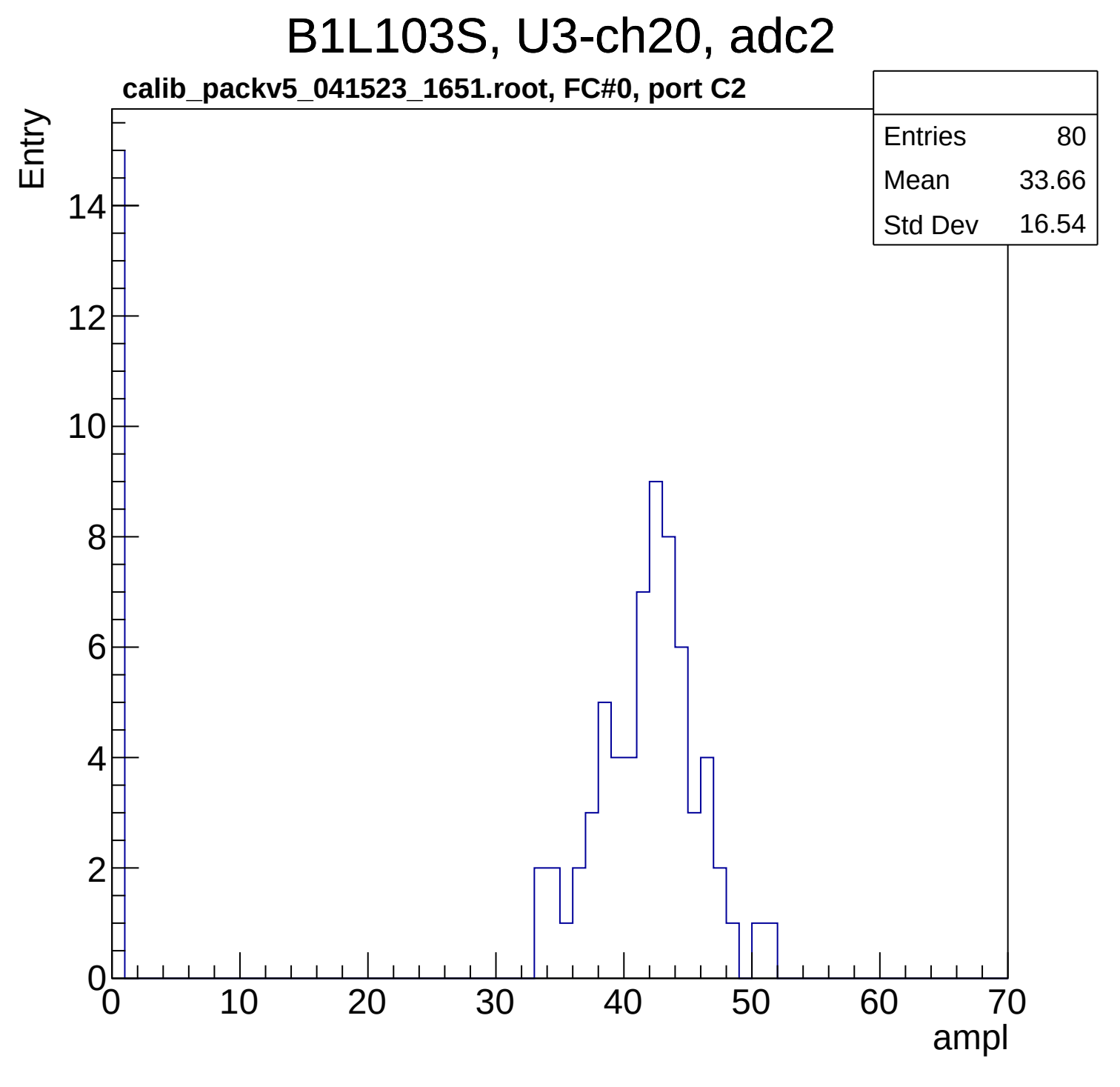
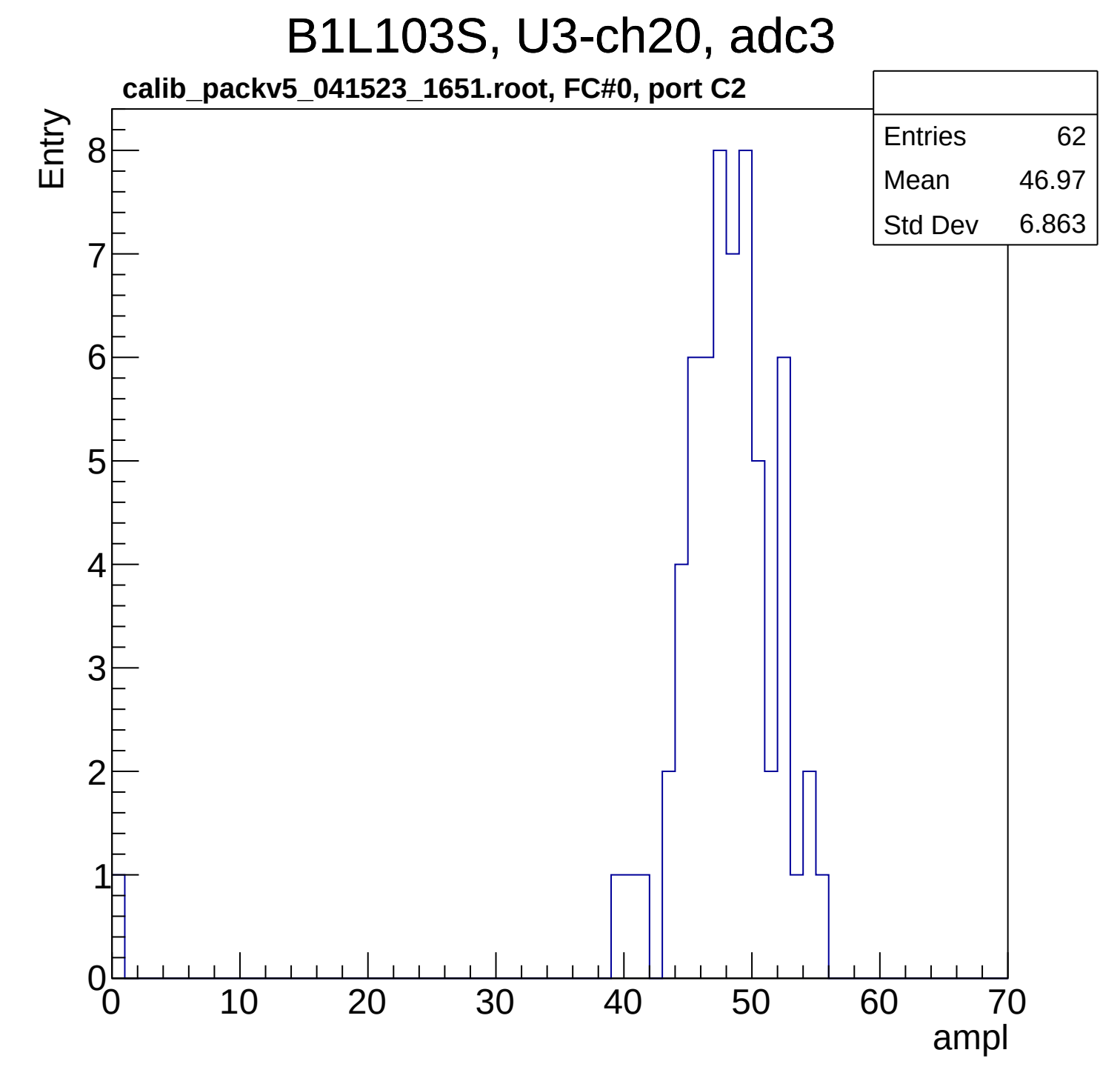
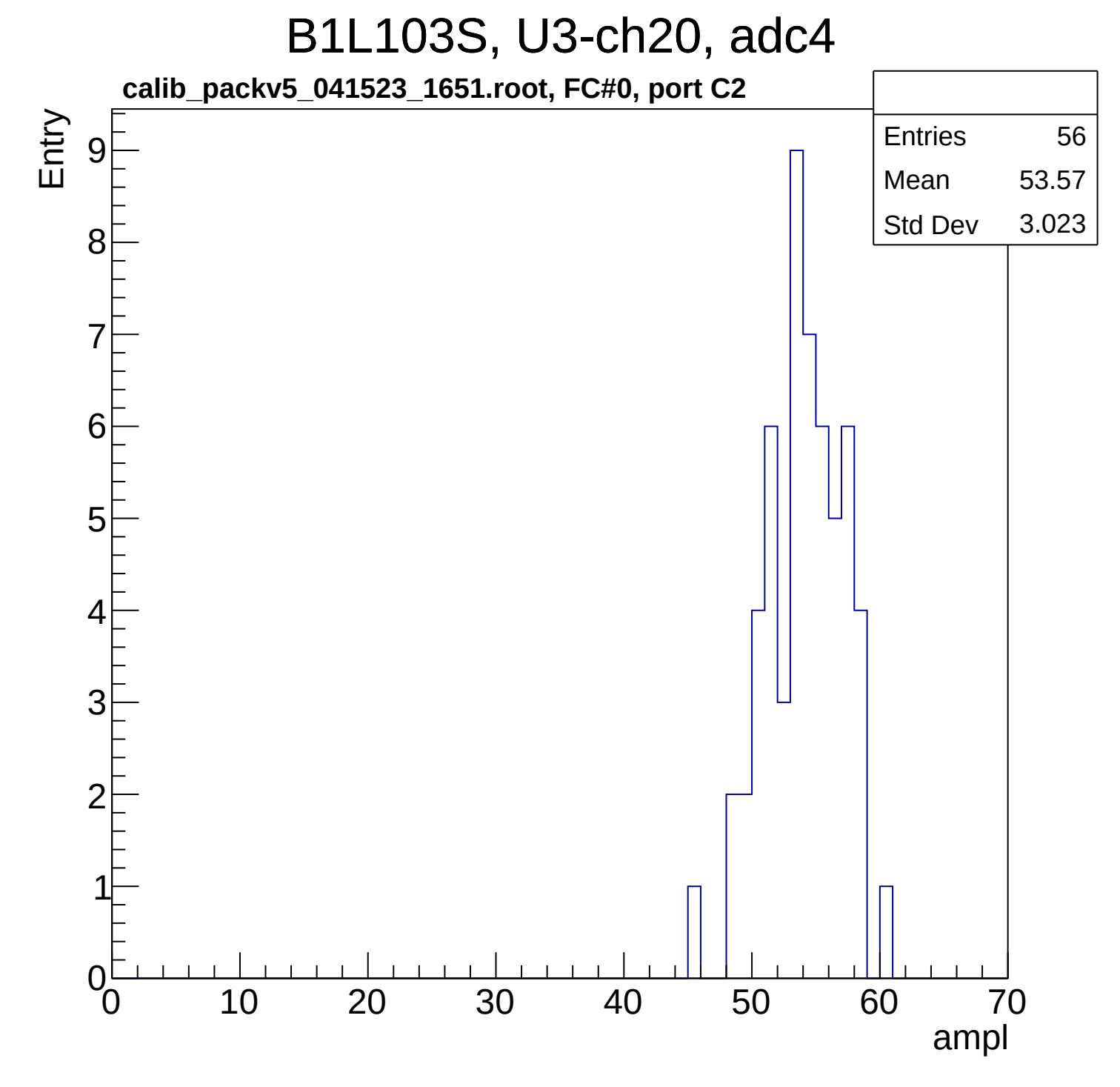

B1L103S, U3-ch19, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

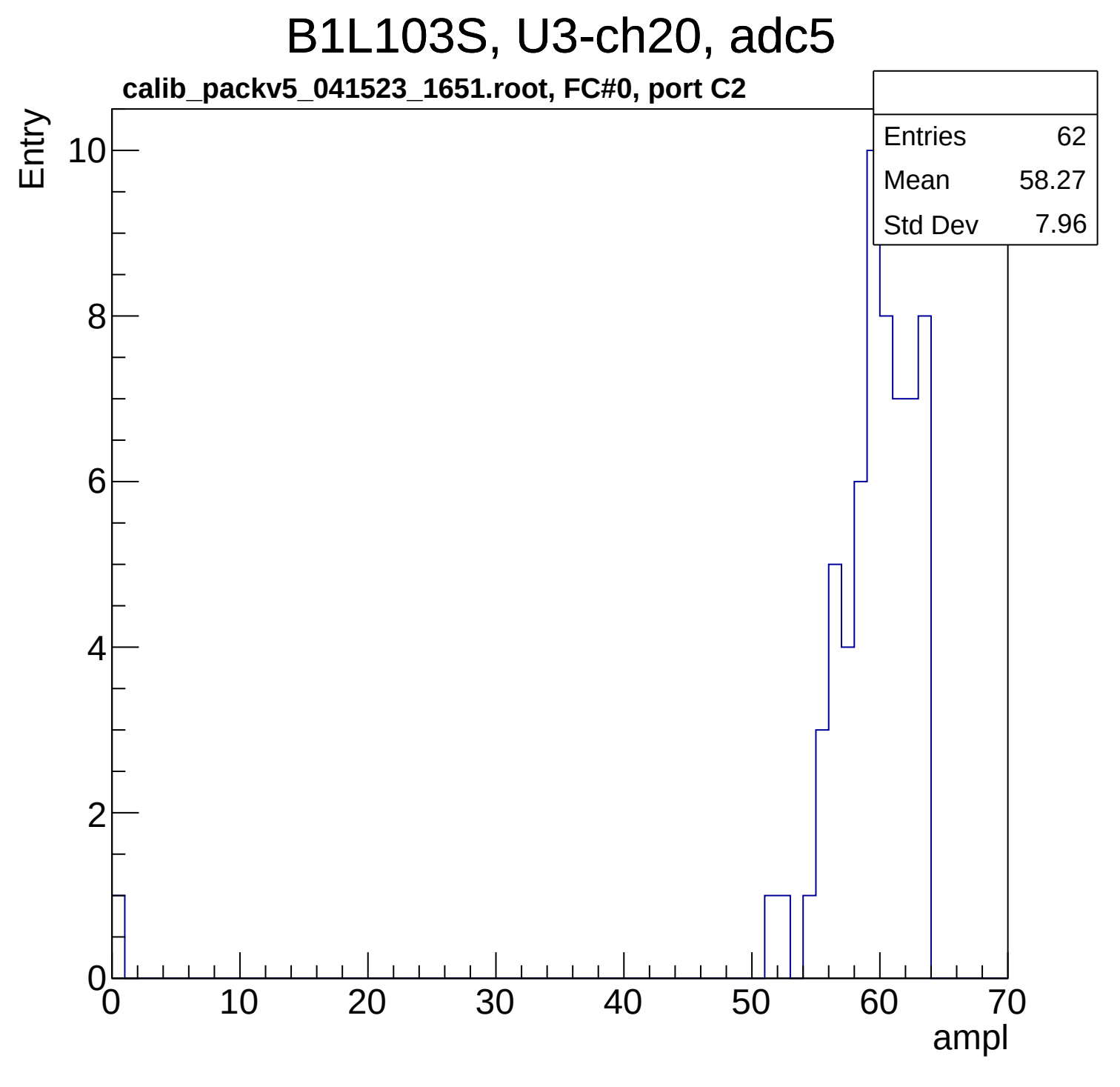

B1L103S, U3-ch20, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 25.72
Std Dev 9.68
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

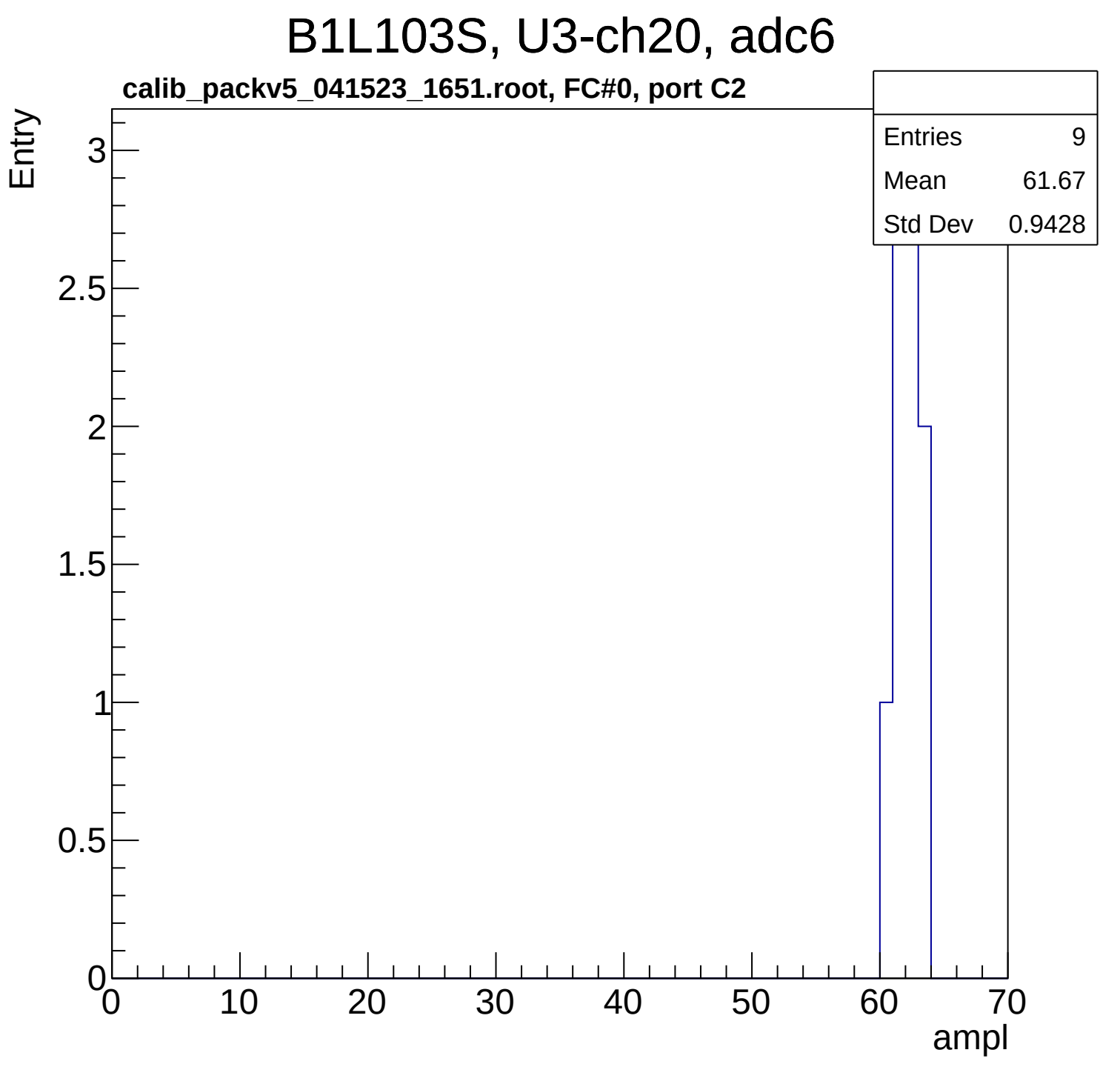

B1L103S, U3-ch20, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 34.23
Std Dev 6.984
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch20, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 33.66
Std Dev 16.54
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch20, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 46.97
Std Dev 6.863
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch20, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 53.57
Std Dev 3.023
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch20, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 58.27
Std Dev 7.96
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch20, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 61.67
Std Dev 0.9428
Entry
ampl
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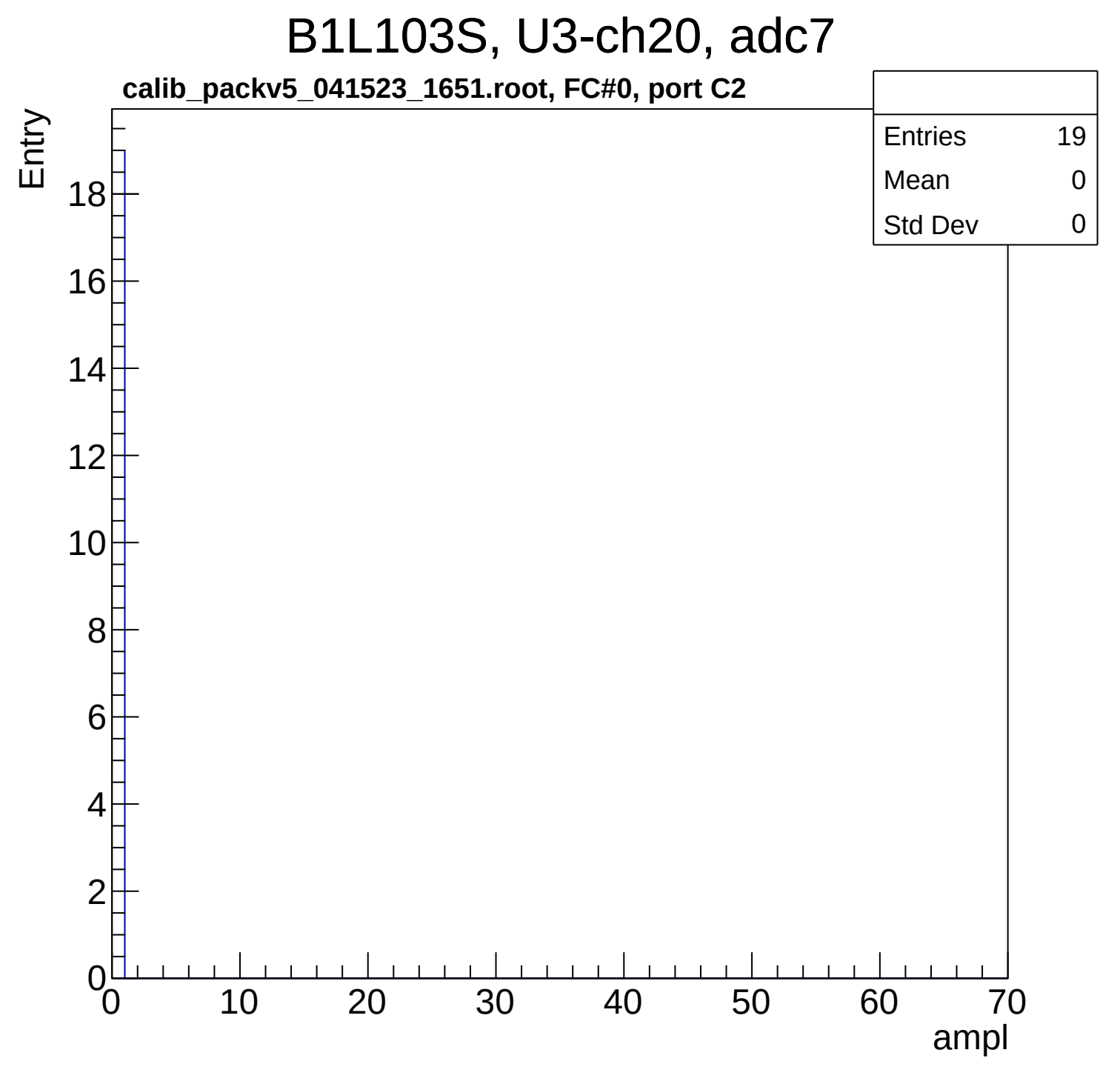
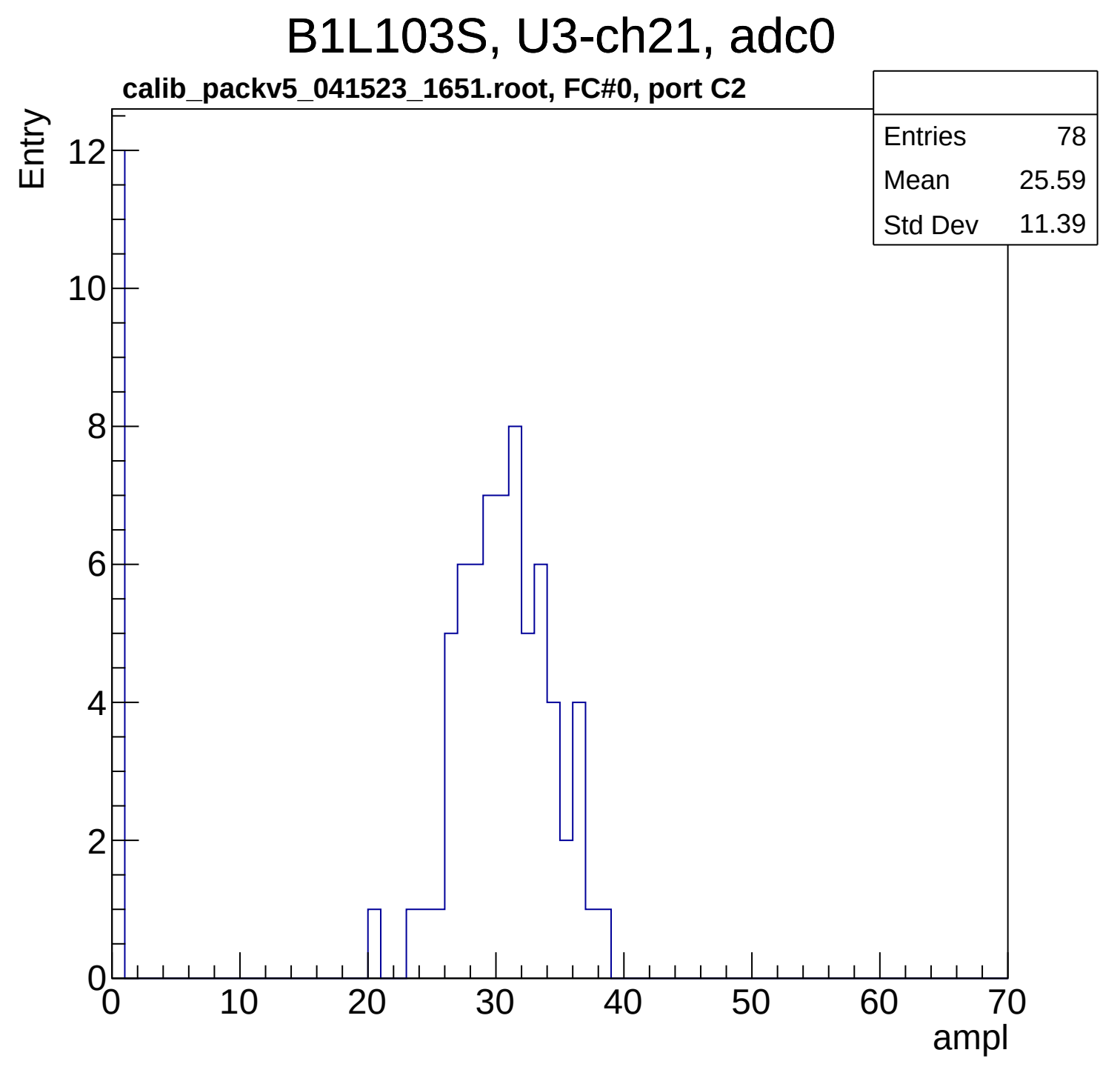
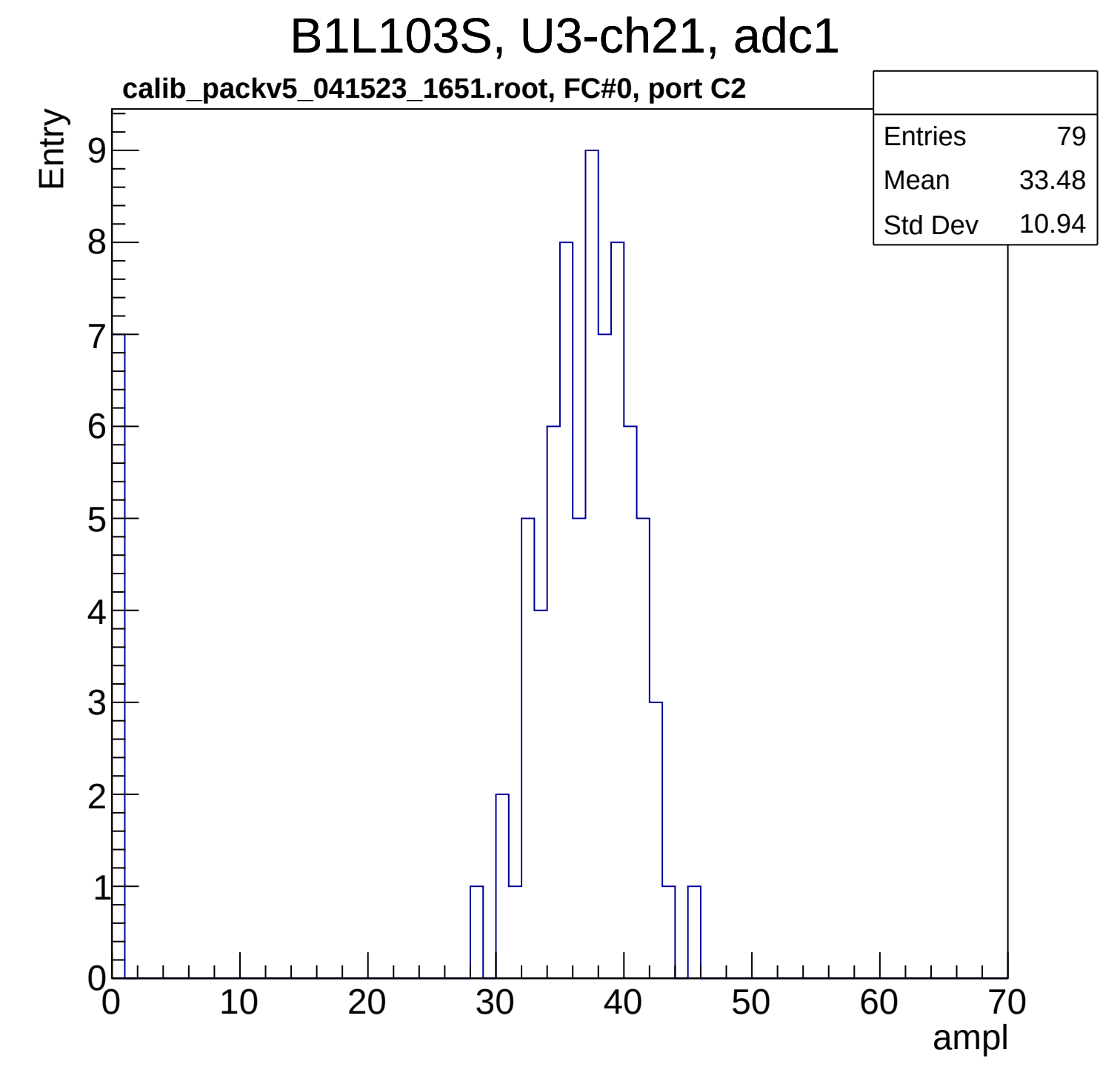
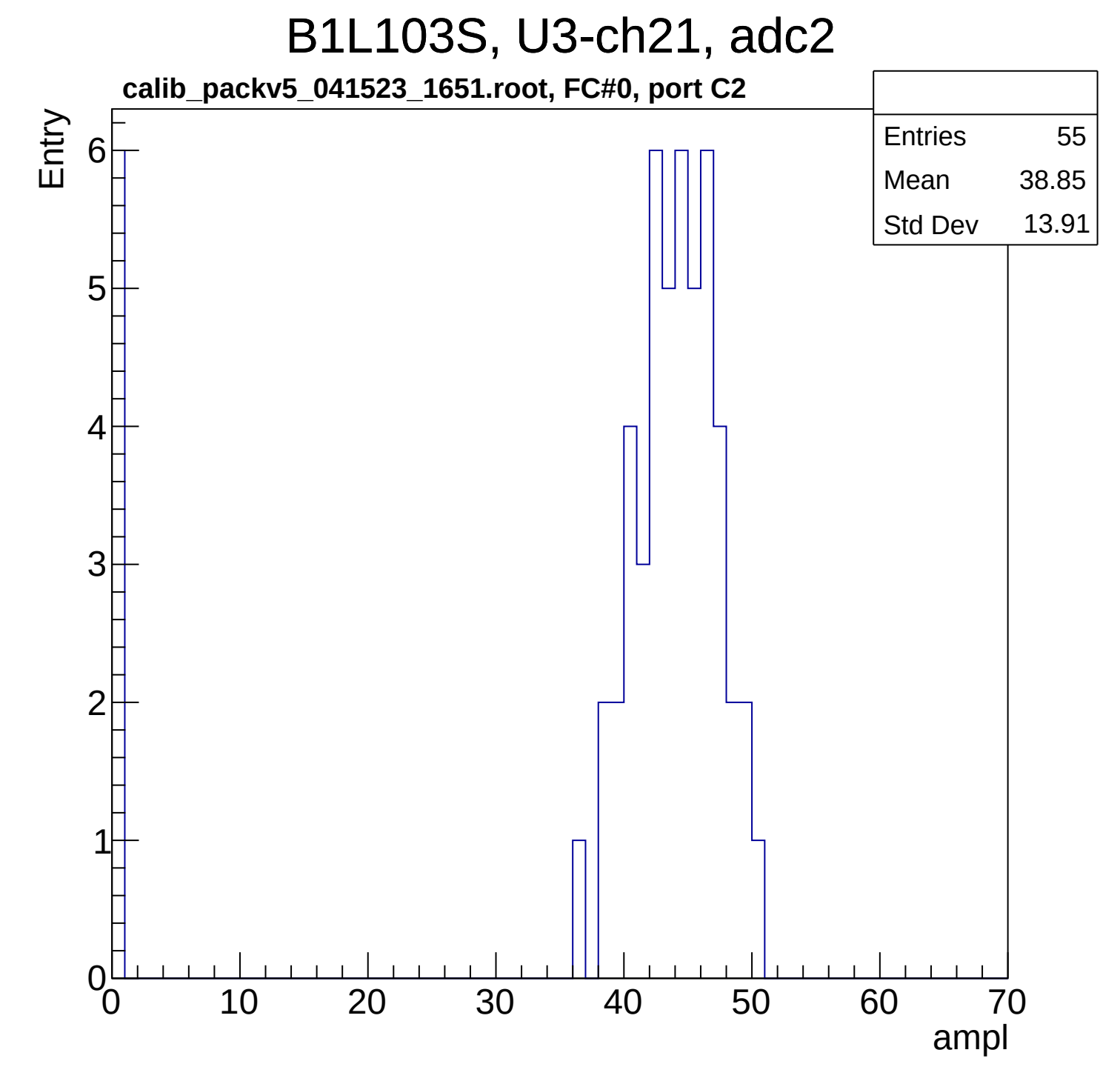
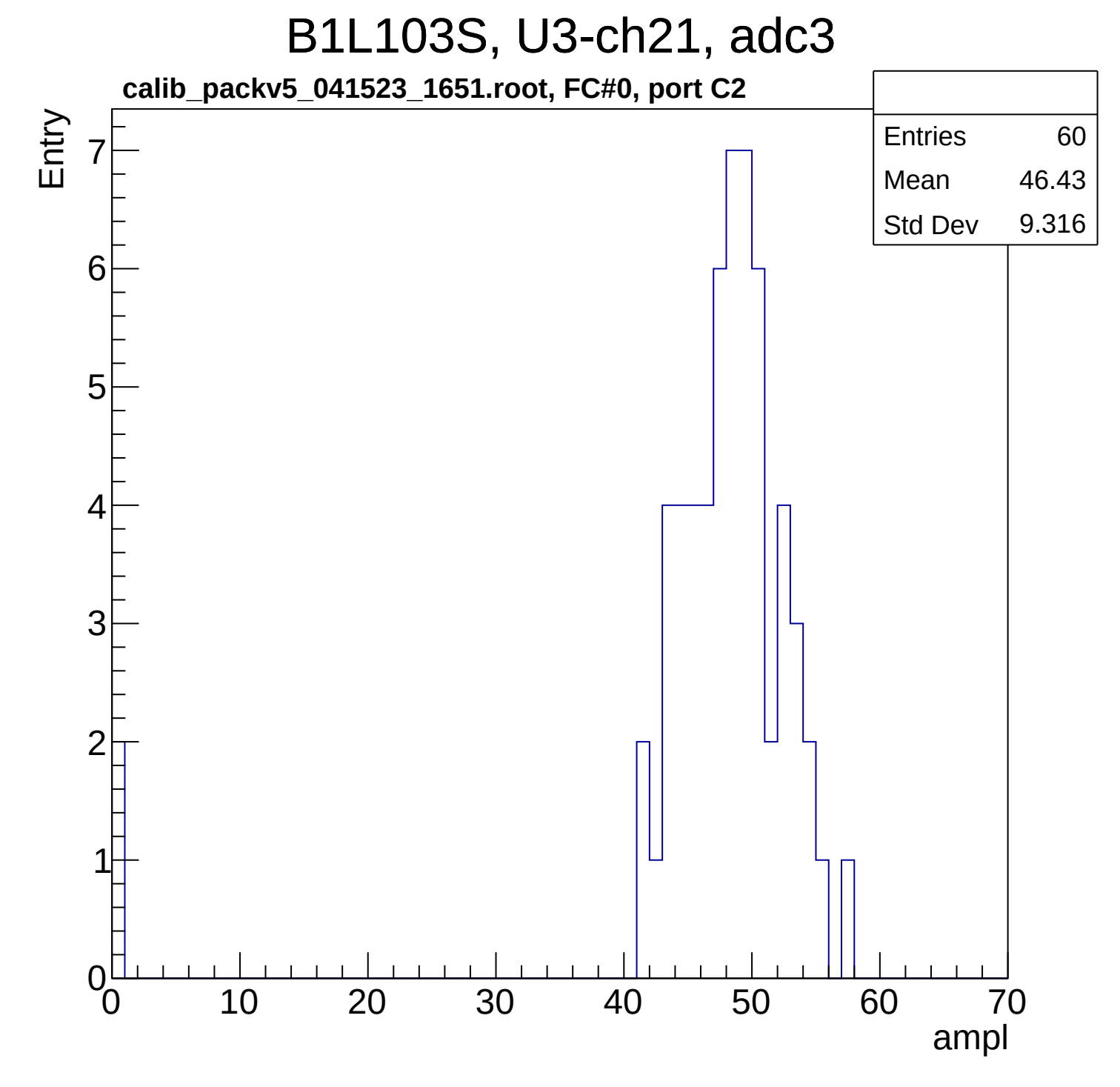
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

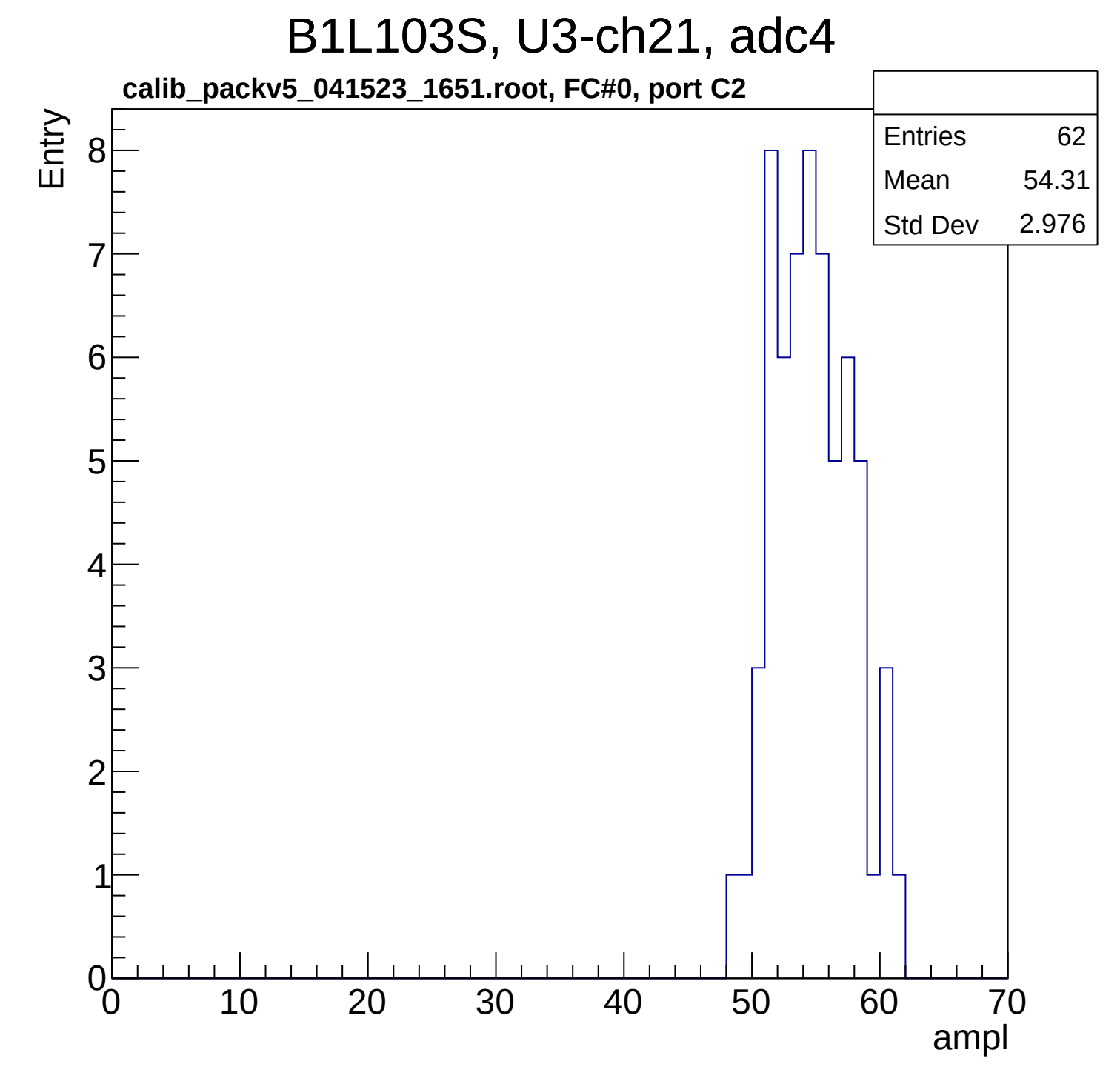

B1L103S, U3-ch20, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

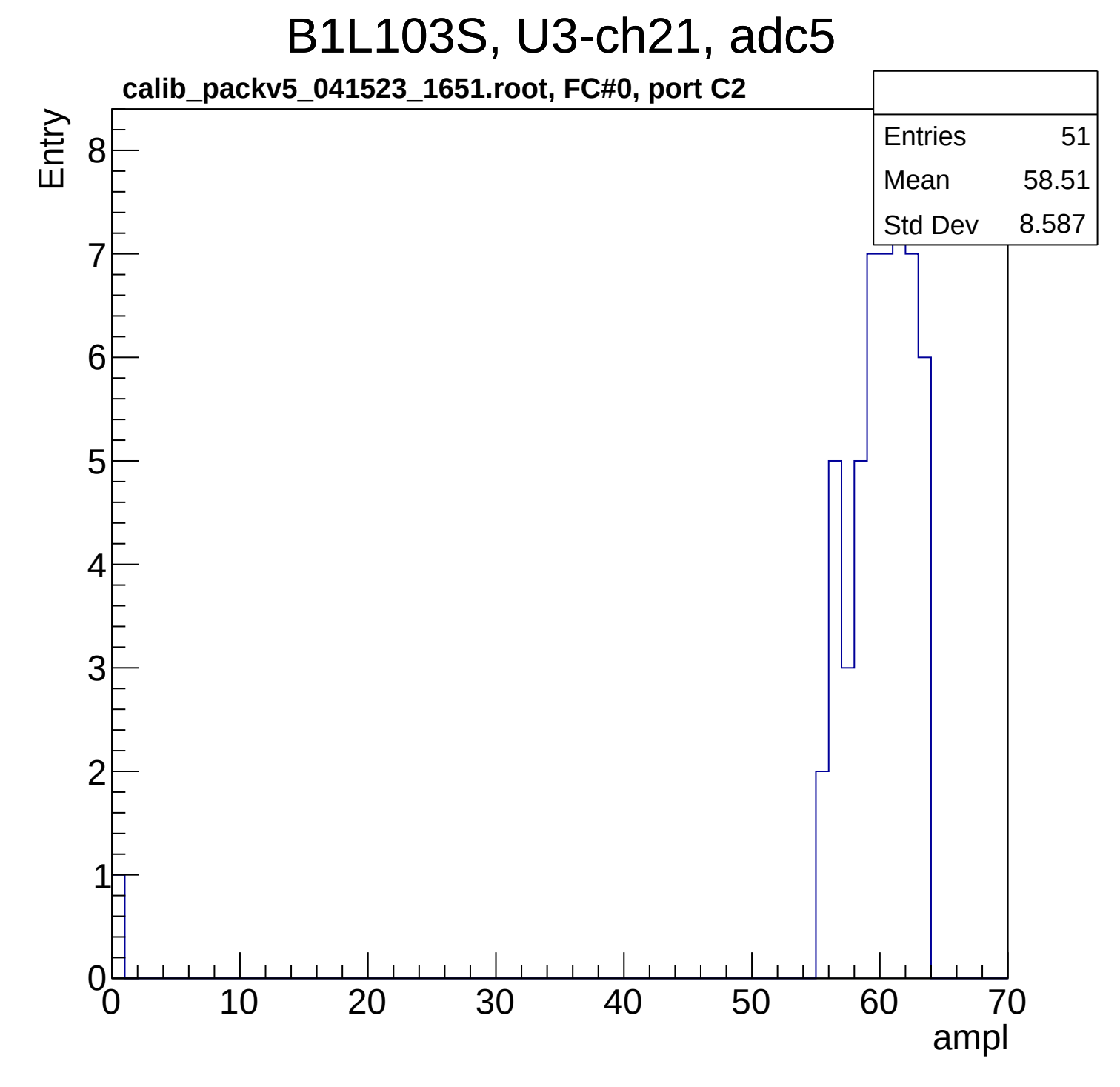

B1L103S, U3-ch21, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 25.59
Std Dev 11.39
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U3-ch21, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 33.48
Std Dev 10.94
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch21, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 38.85
Std Dev 13.91
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch21, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 46.43
Std Dev 9.316
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch21, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 54.31
Std Dev 2.976
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch21, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 58.51
Std Dev 8.587
Entry
ampl
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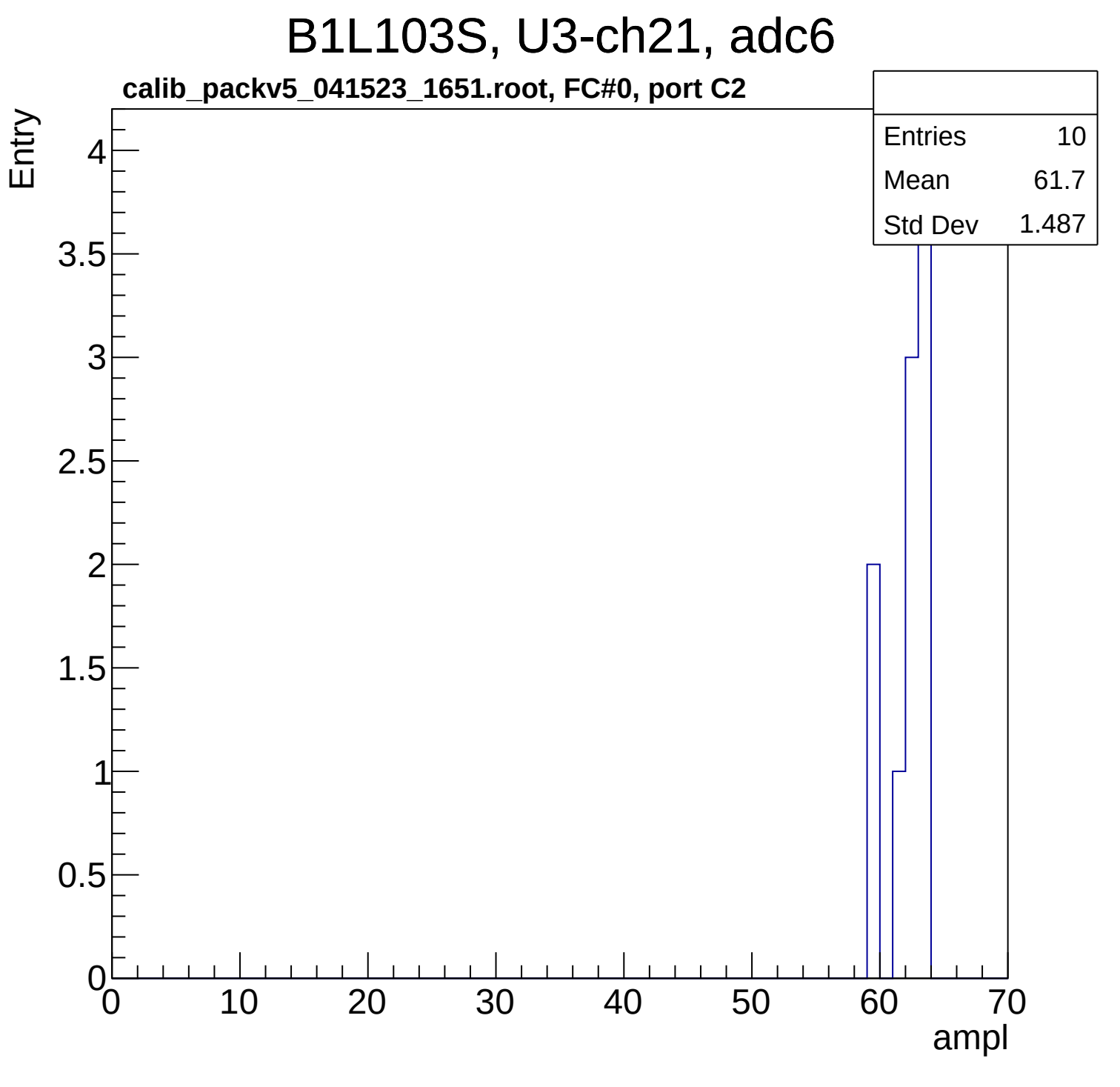
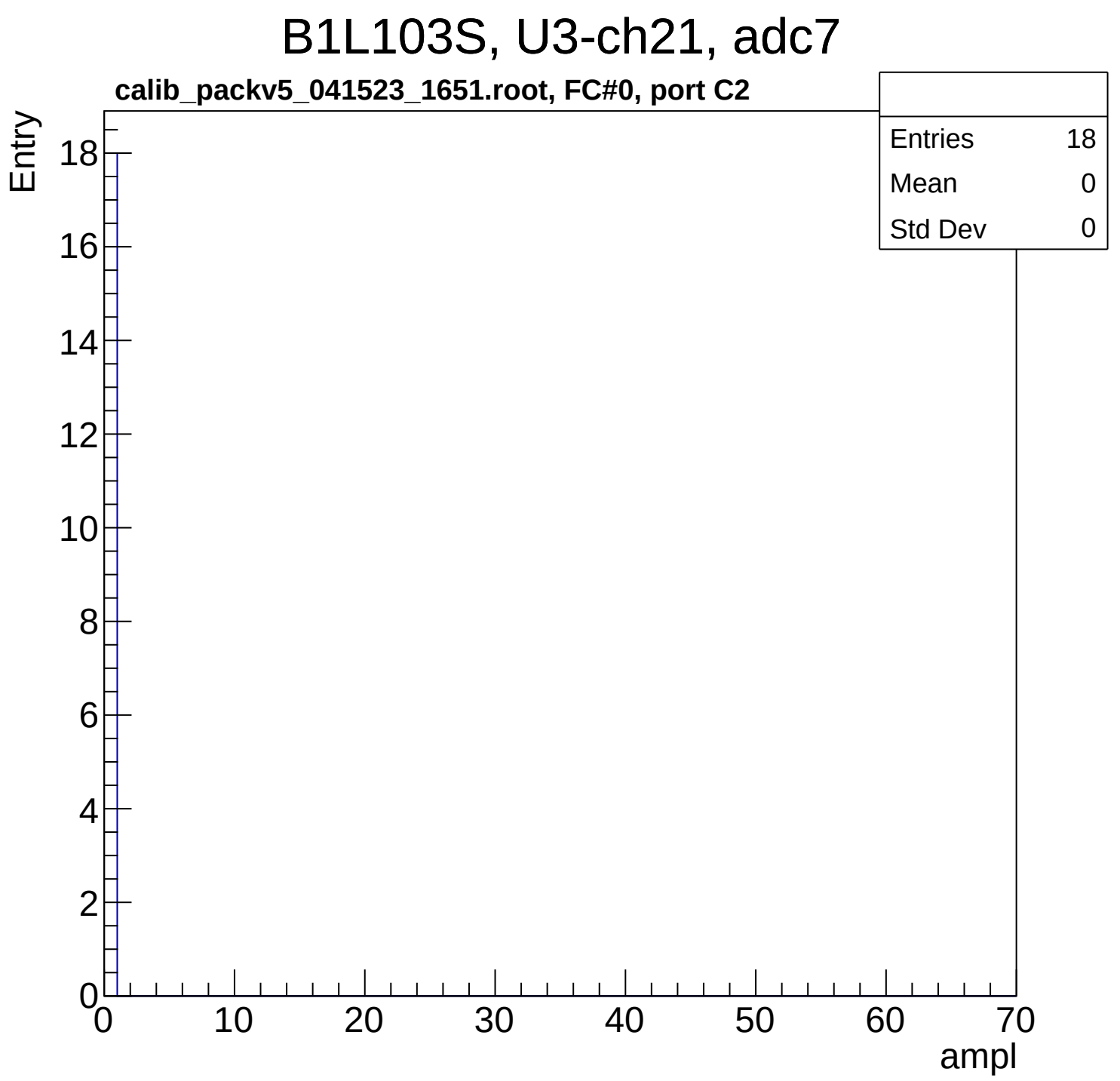
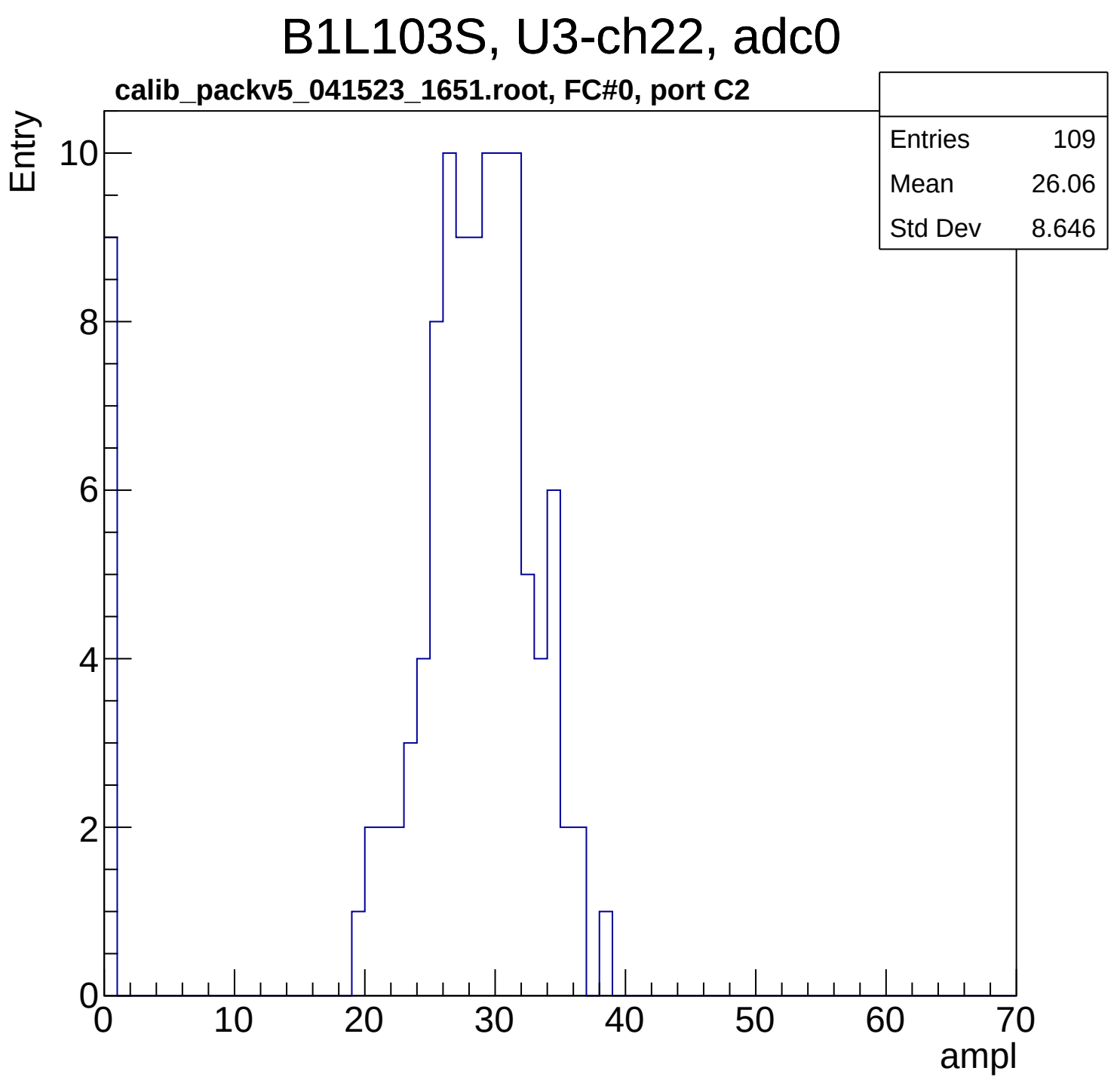
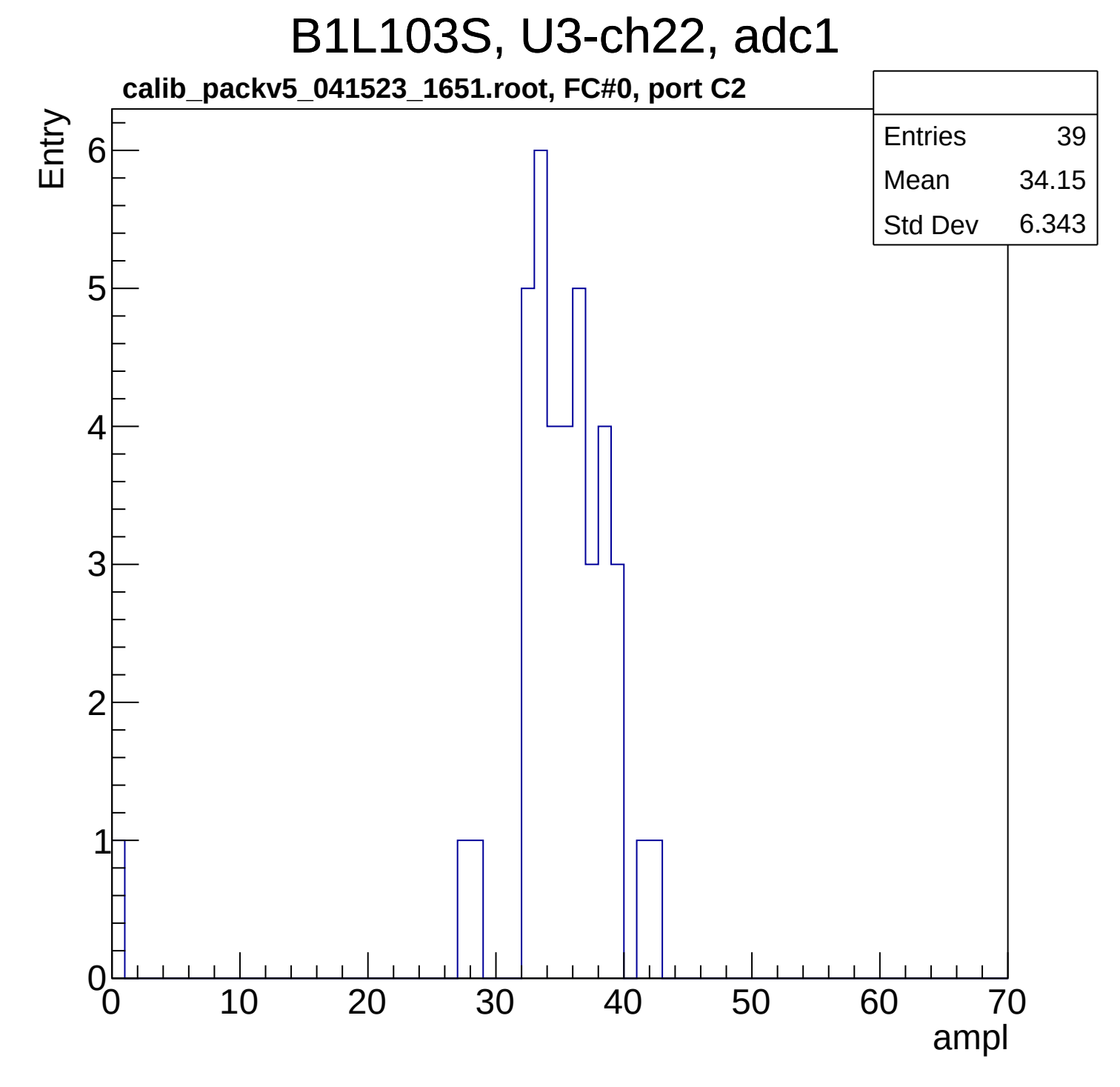
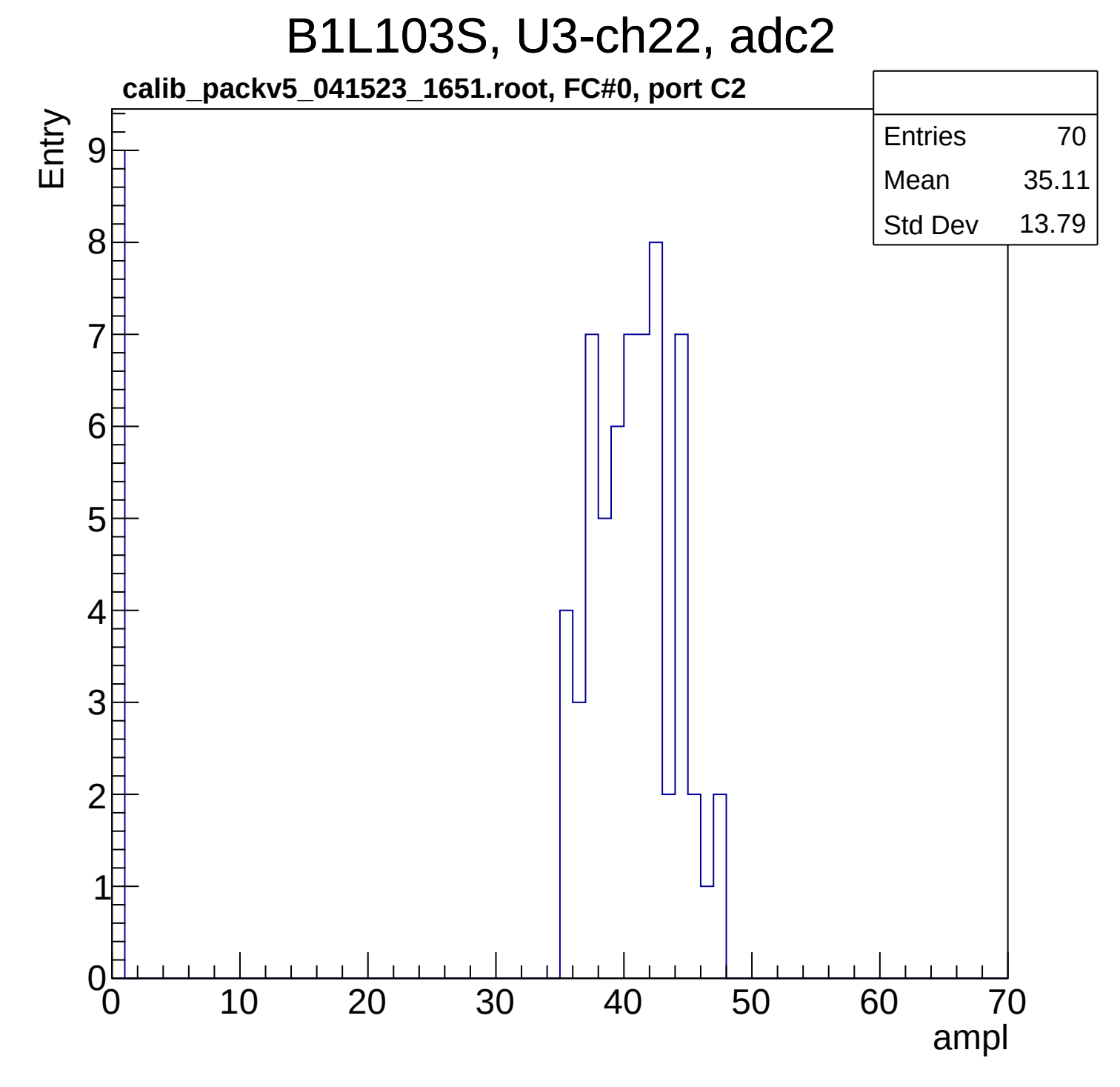
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

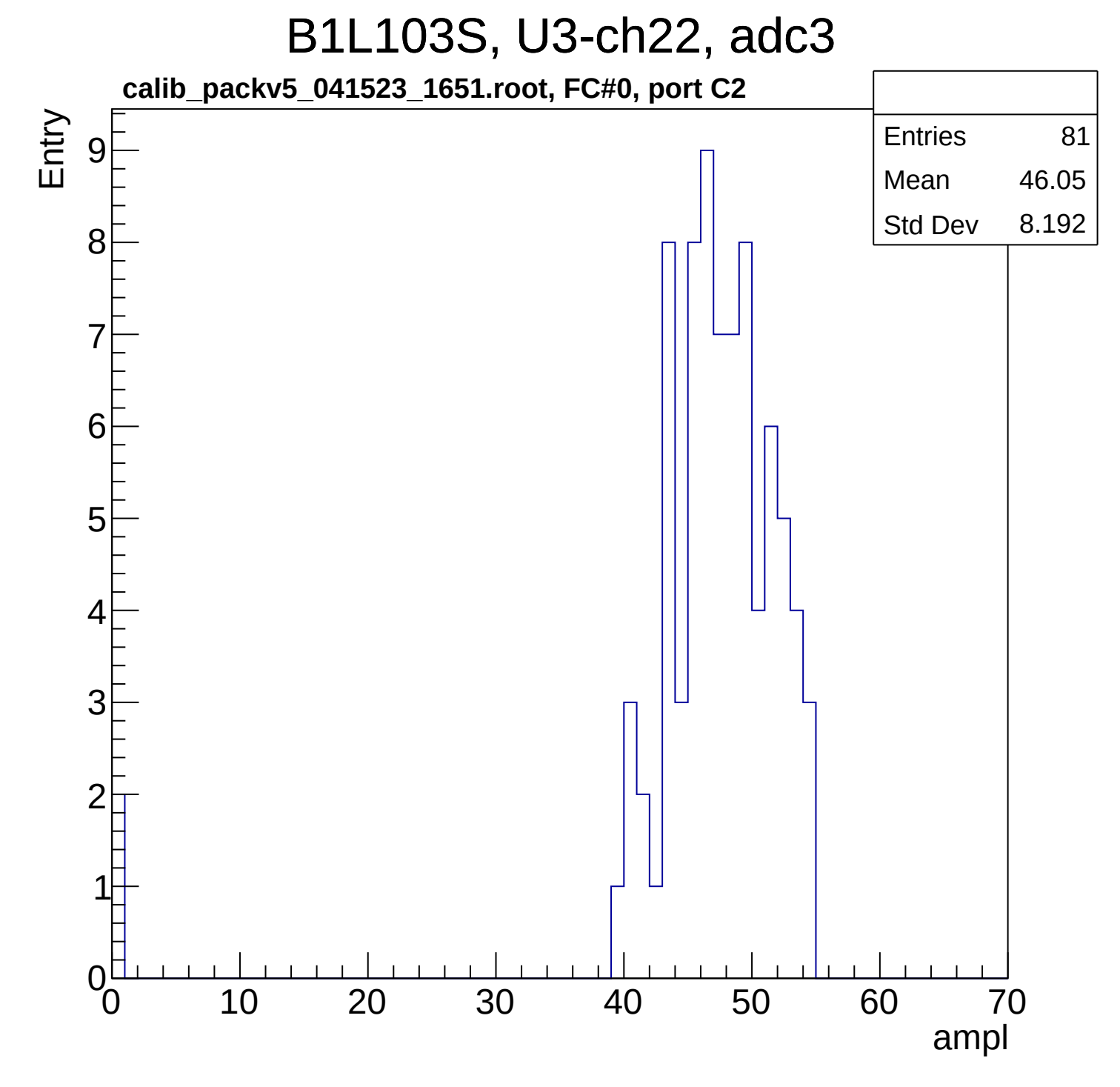

B1L103S, U3-ch21, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61.7
Std Dev 1.487
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U3-ch21, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch22, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 109
Mean 26.06
Std Dev 8.646
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U3-ch22, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 34.15
Std Dev 6.343
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U3-ch22, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 35.11
Std Dev 13.79
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch22, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 46.05
Std Dev 8.192
Entry
ampl
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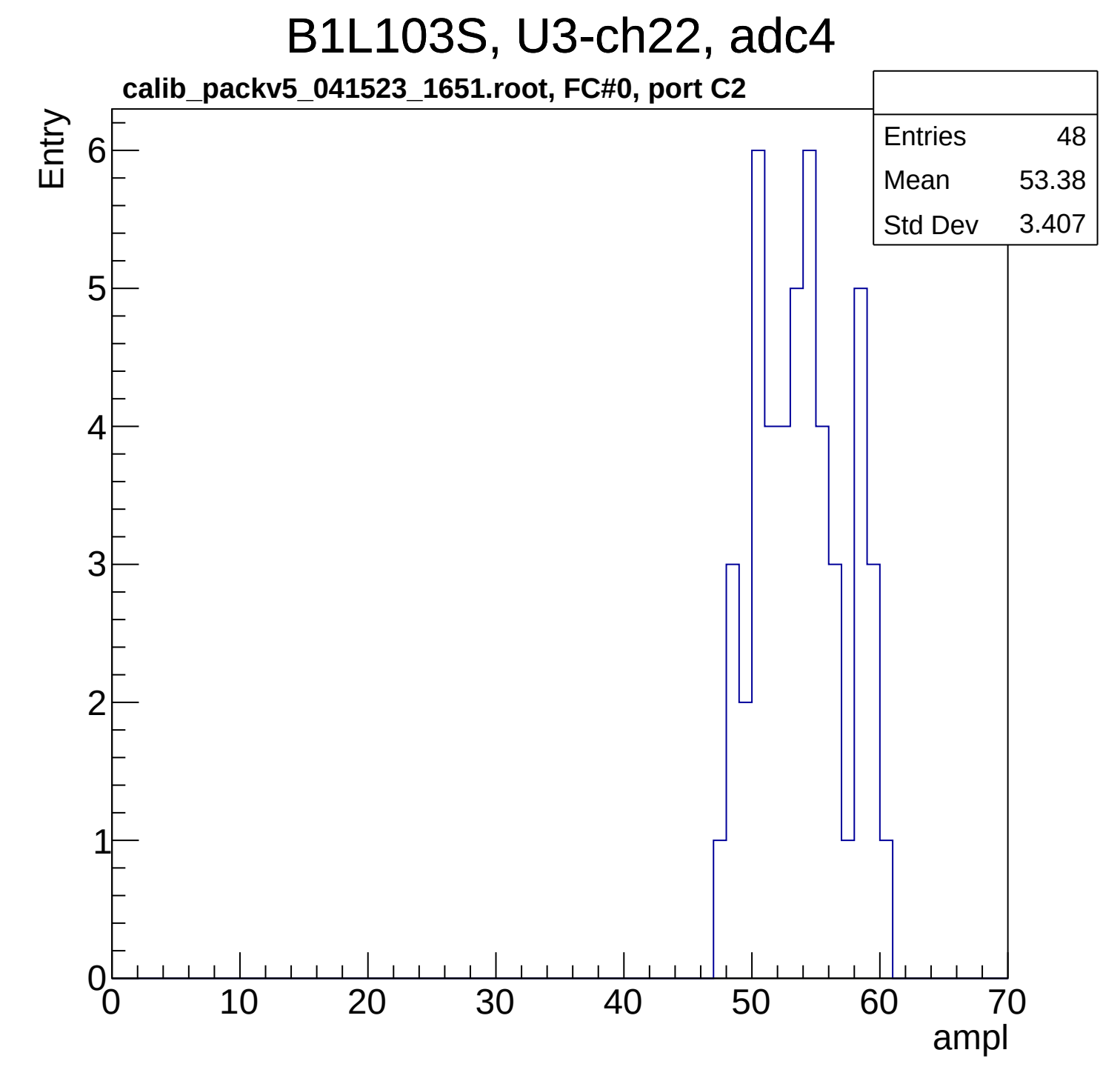
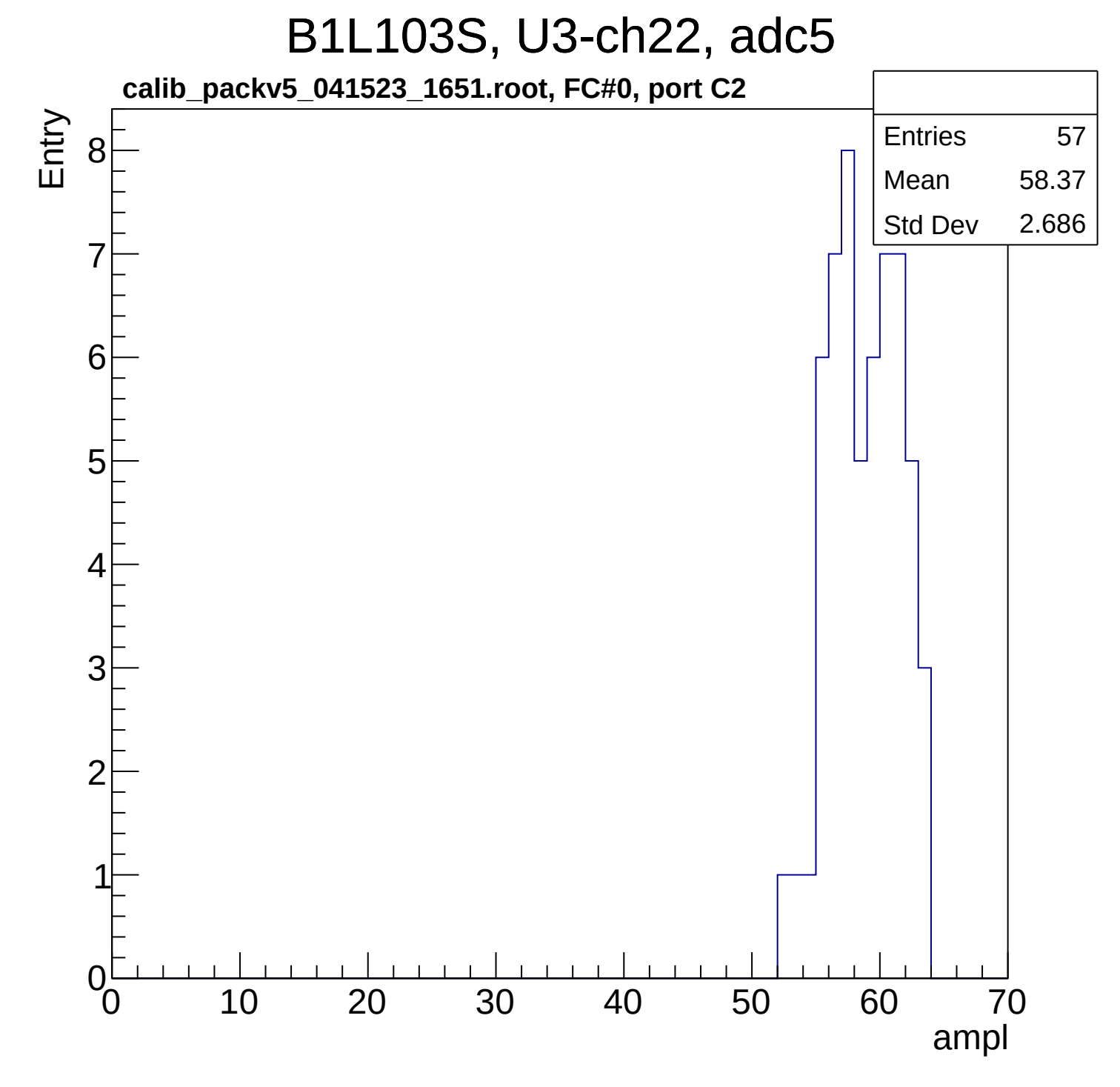
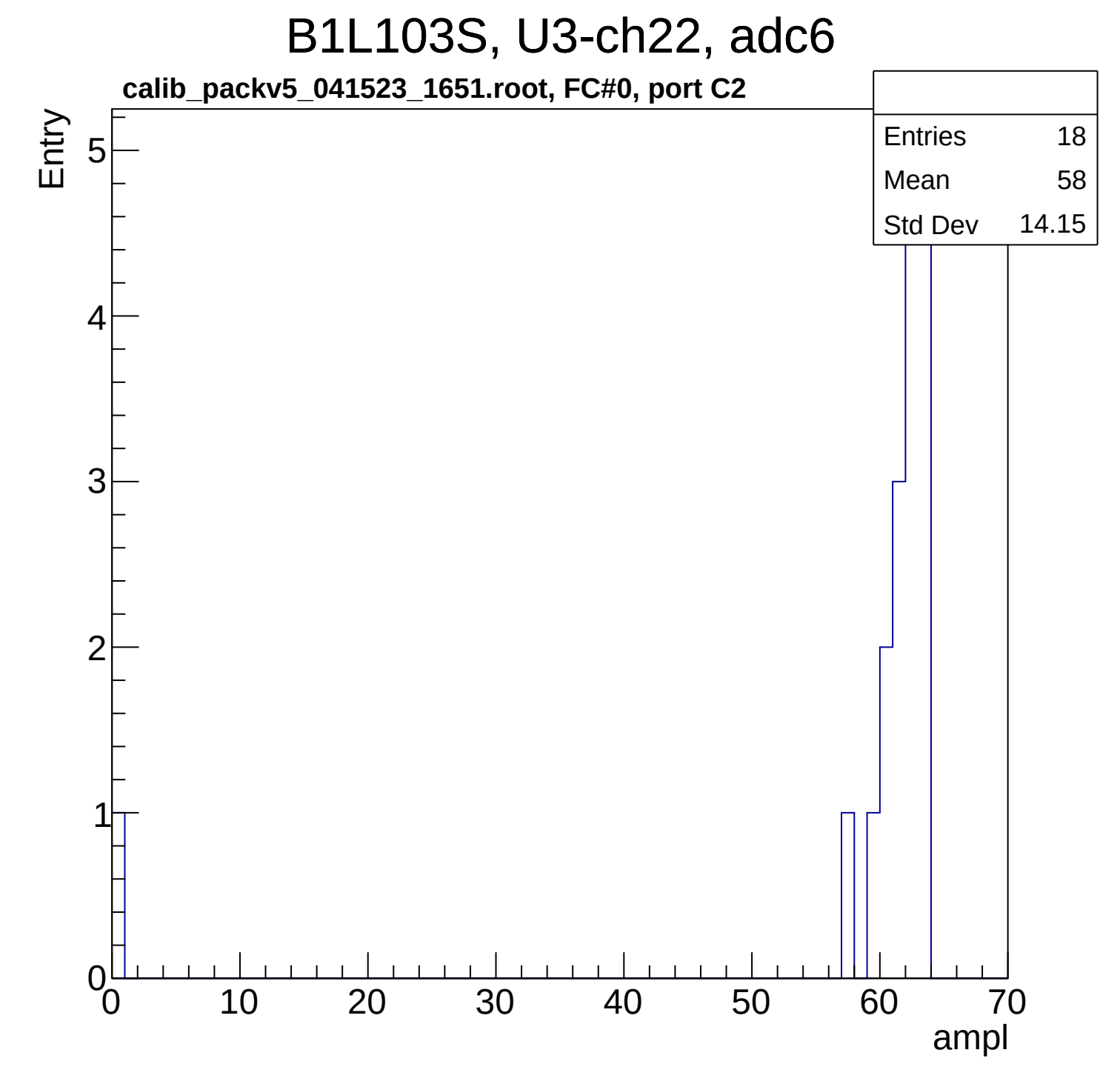
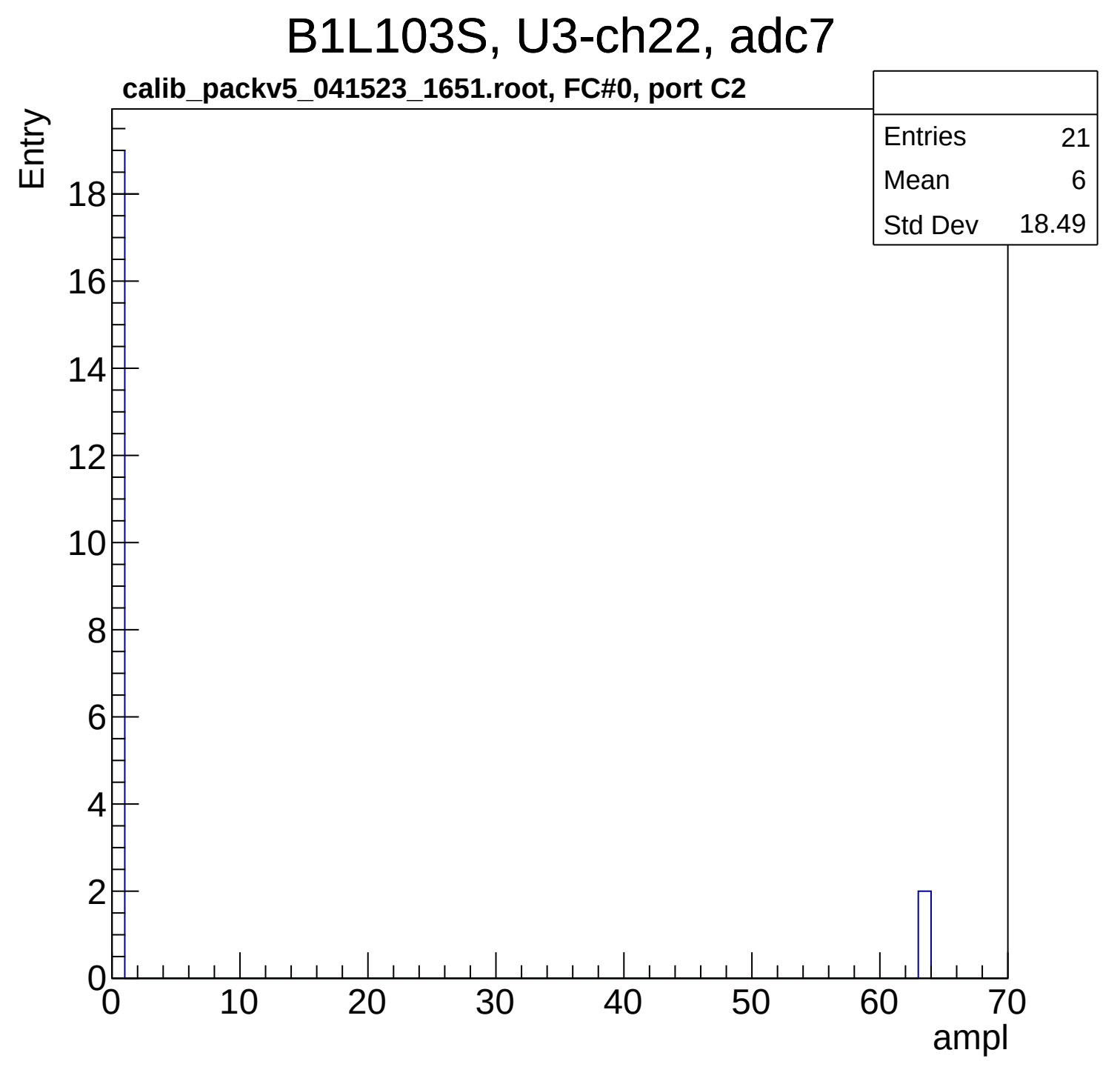
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch22, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 53.38
Std Dev 3.407
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch22, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 58.37
Std Dev 2.686
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch22, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 58
Std Dev 14.15
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch22, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 6
Std Dev 18.49
Entry
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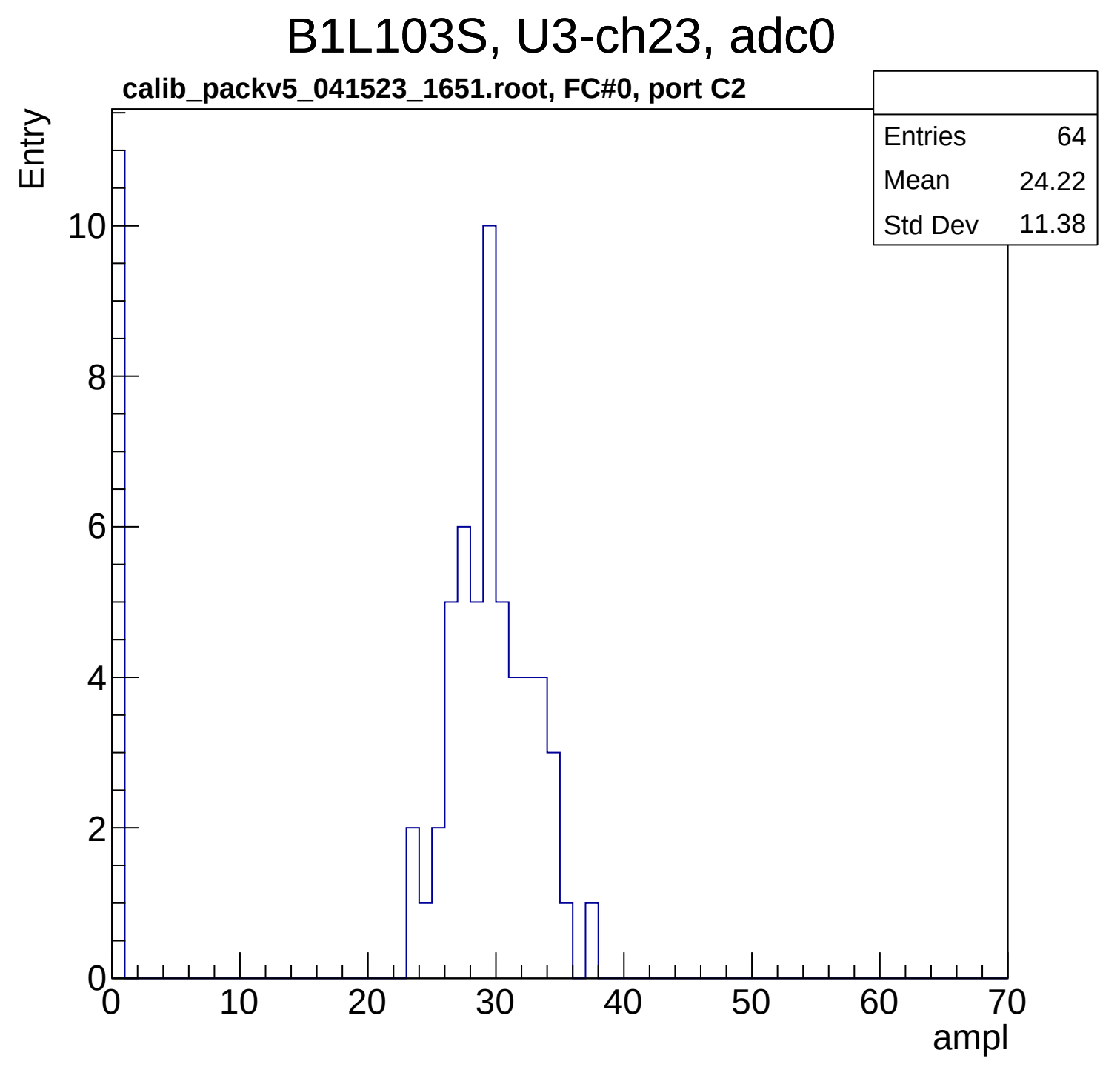
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch23, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 24.22
Std Dev 11.38
Entry
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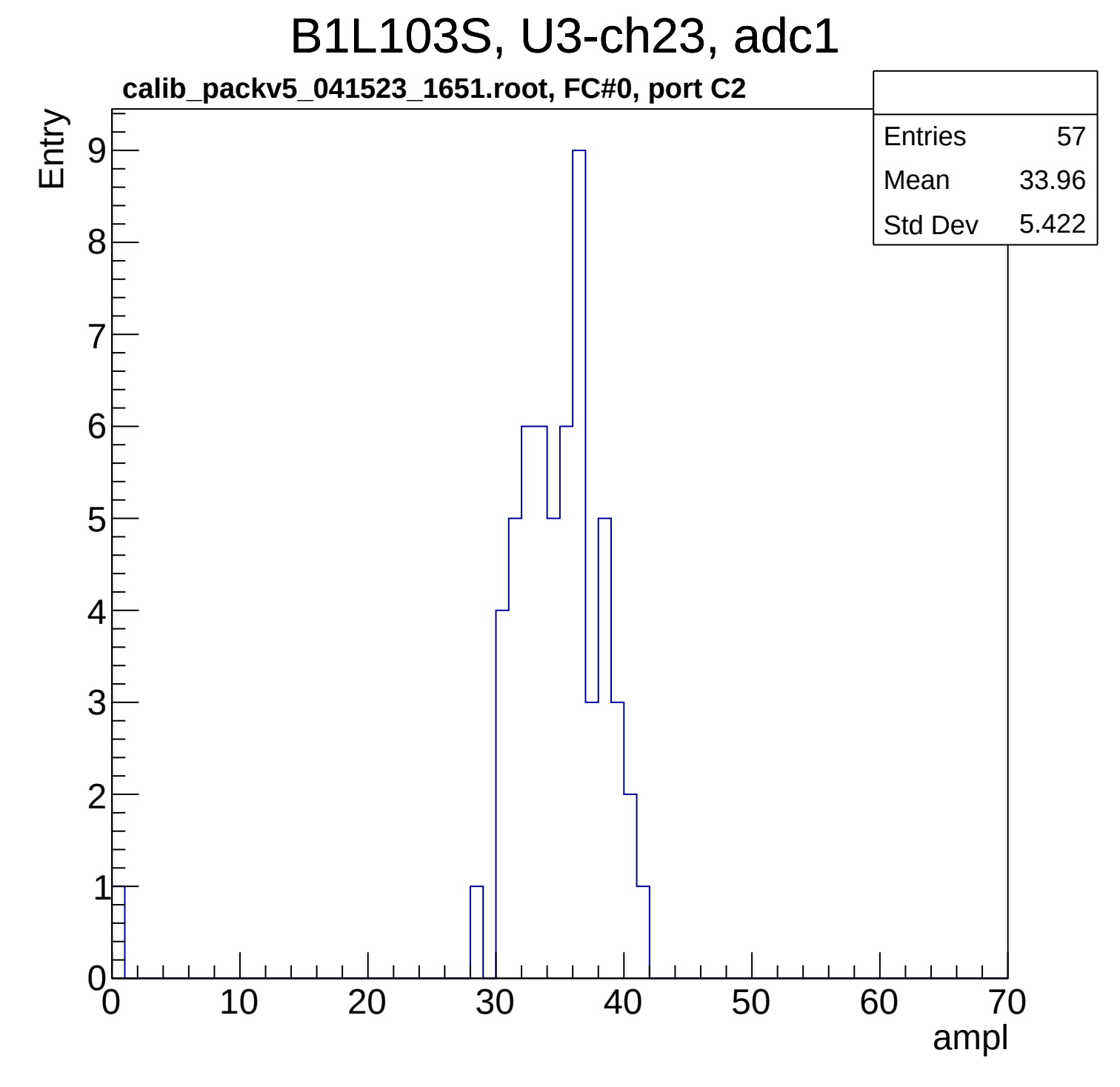
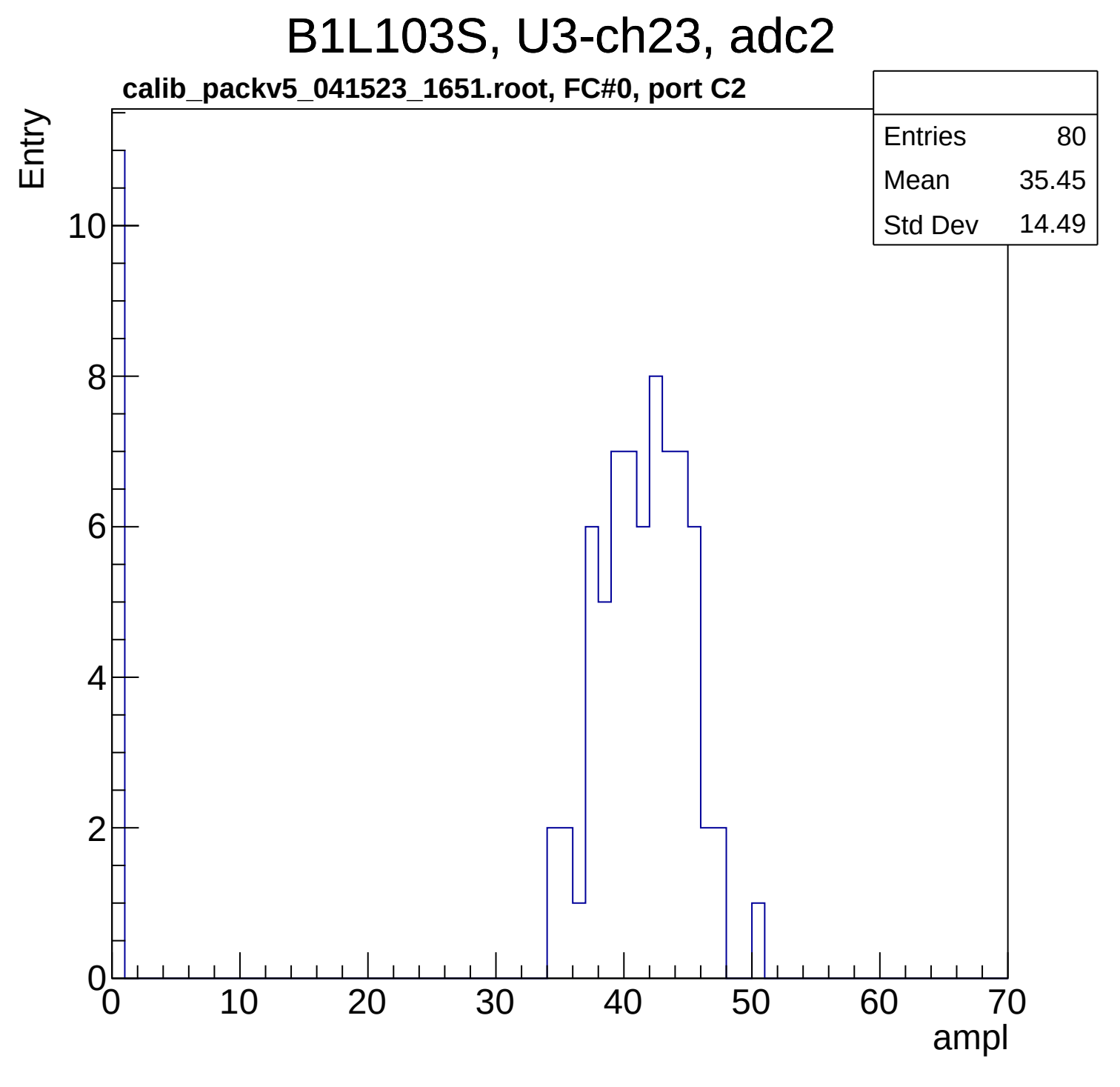
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch23, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 33.96
Std Dev 5.422
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch23, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 35.45
Std Dev 14.49
Entry
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2
4
6
8
10
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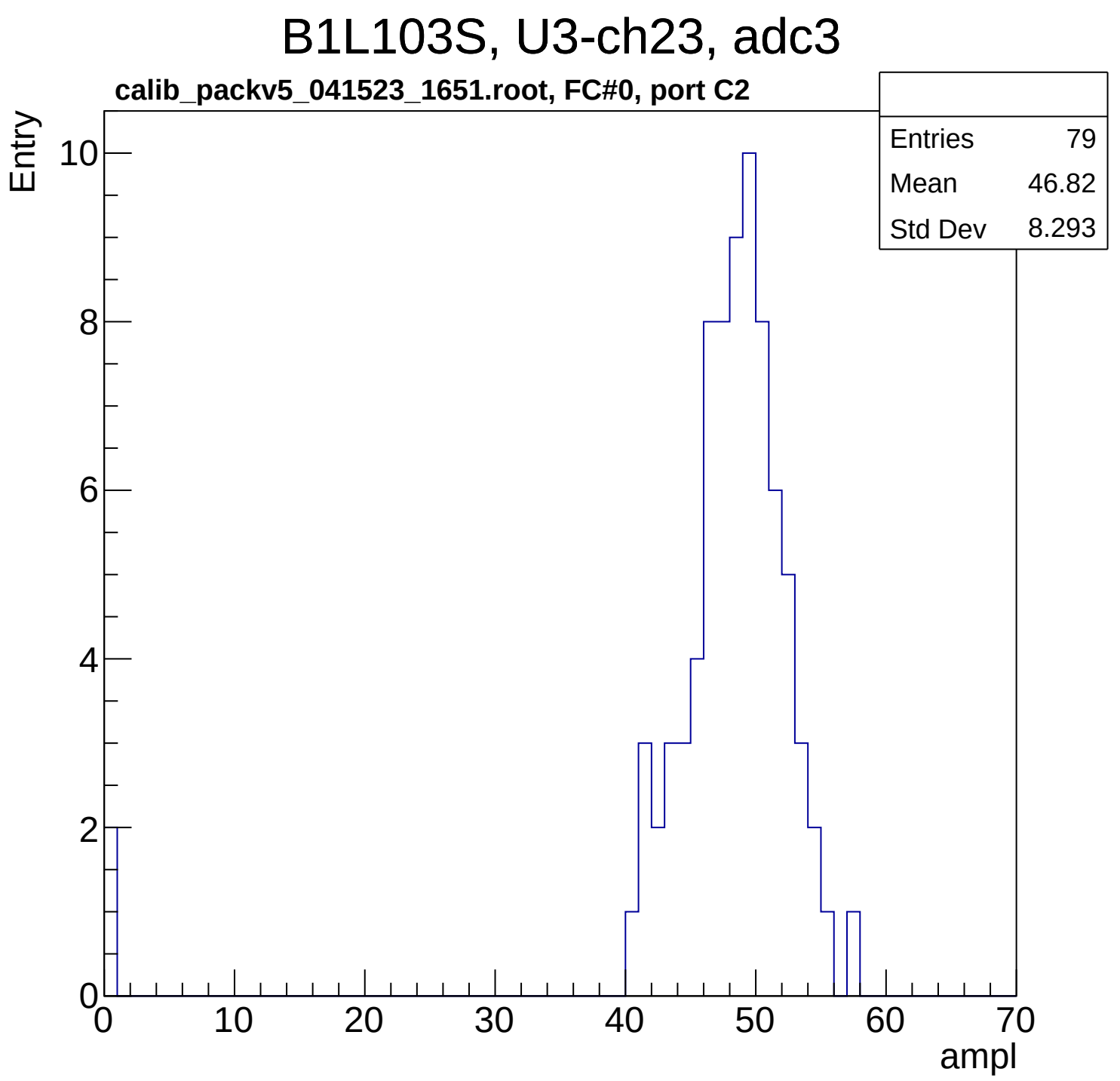
ampl


B1L103S, U3-ch23, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 46.82
Std Dev 8.293
Entry
ampl
0
2
4
6
8
10
0
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40
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60
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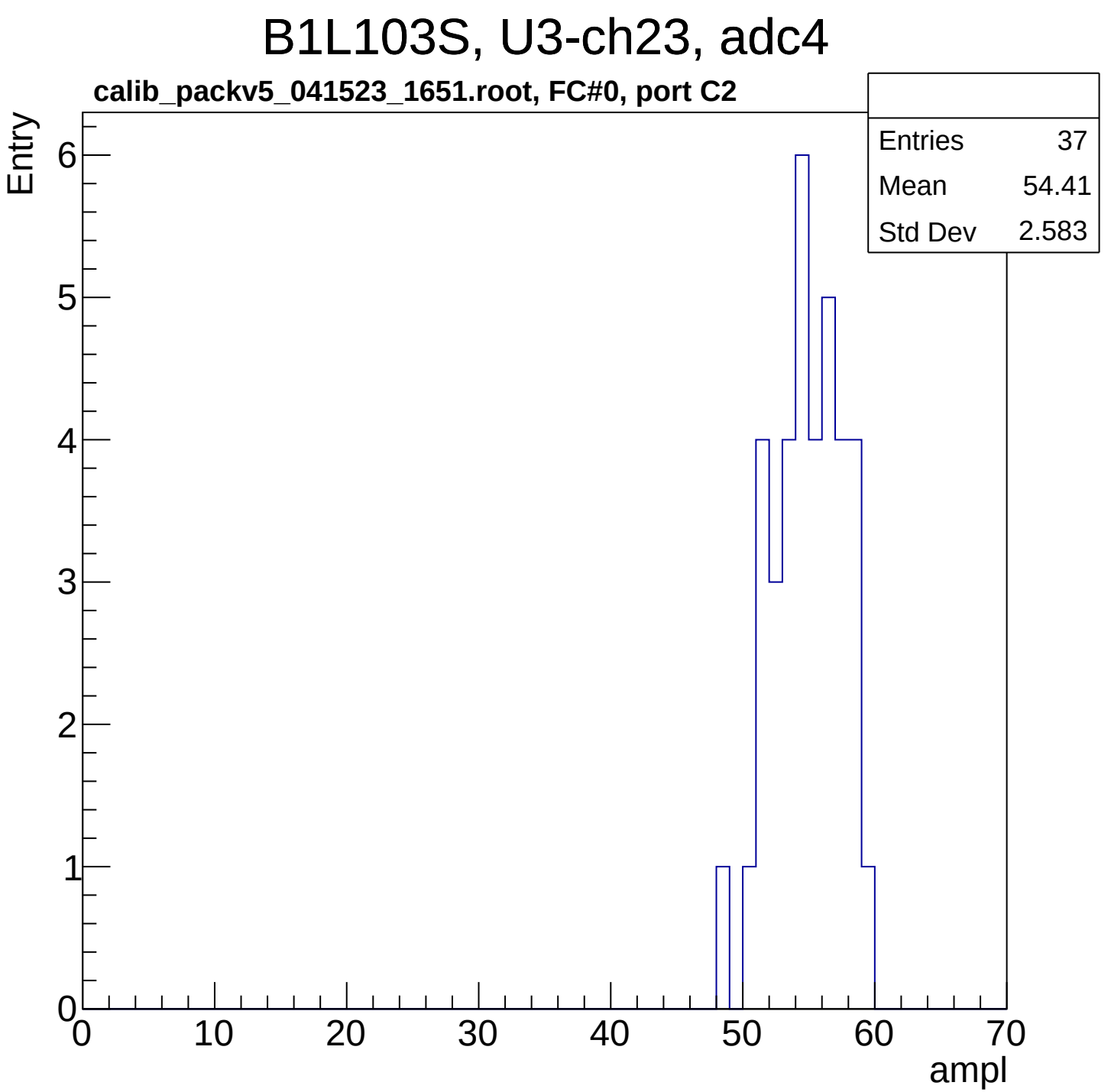
B1L103S, U3-ch23, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 54.41
Std Dev 2.583
Entry
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4
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6
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10
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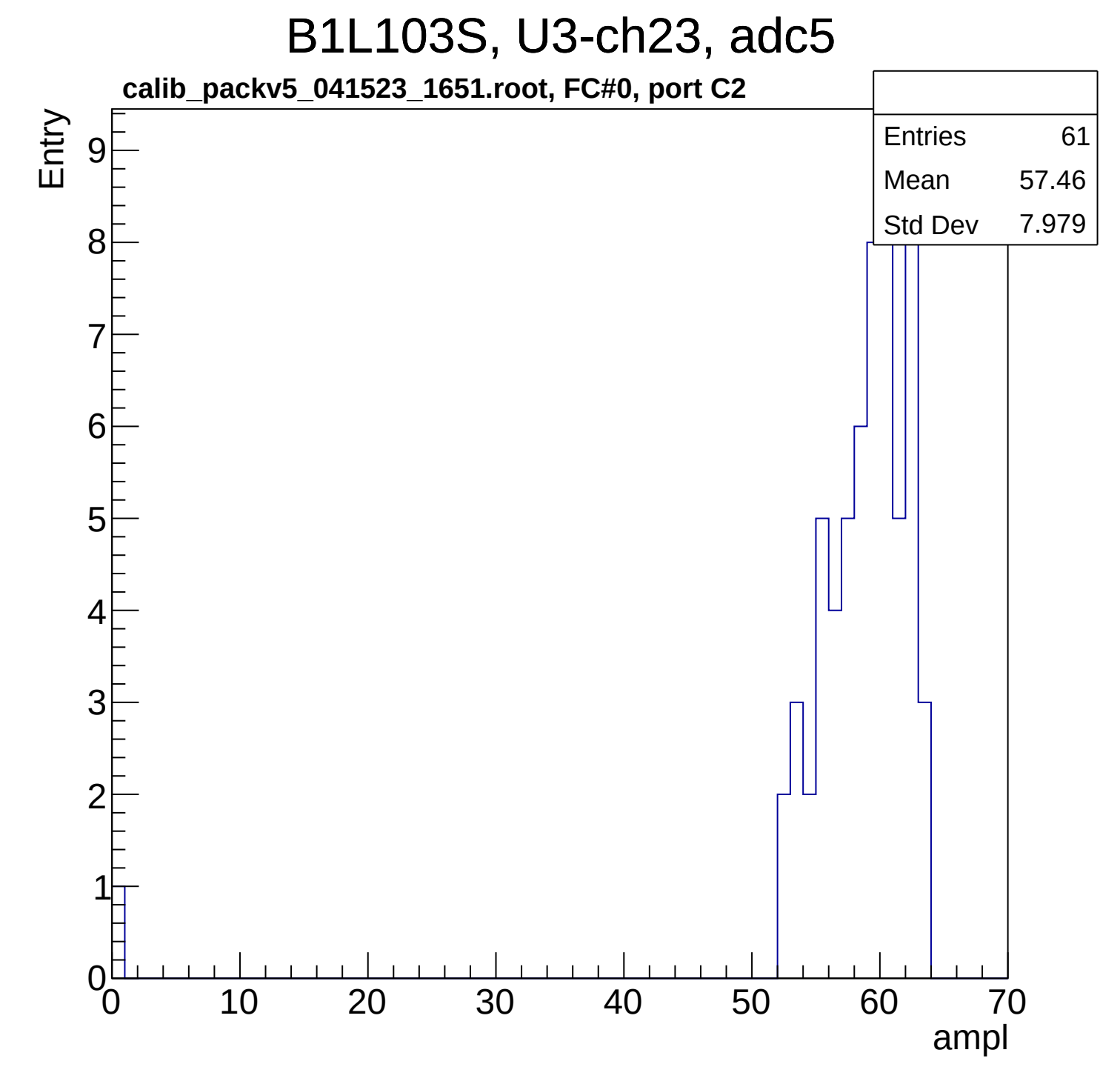
70
ampl


B1L103S, U3-ch23, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 57.46
Std Dev 7.979
Entry
ampl
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3
4
5
6
7
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0
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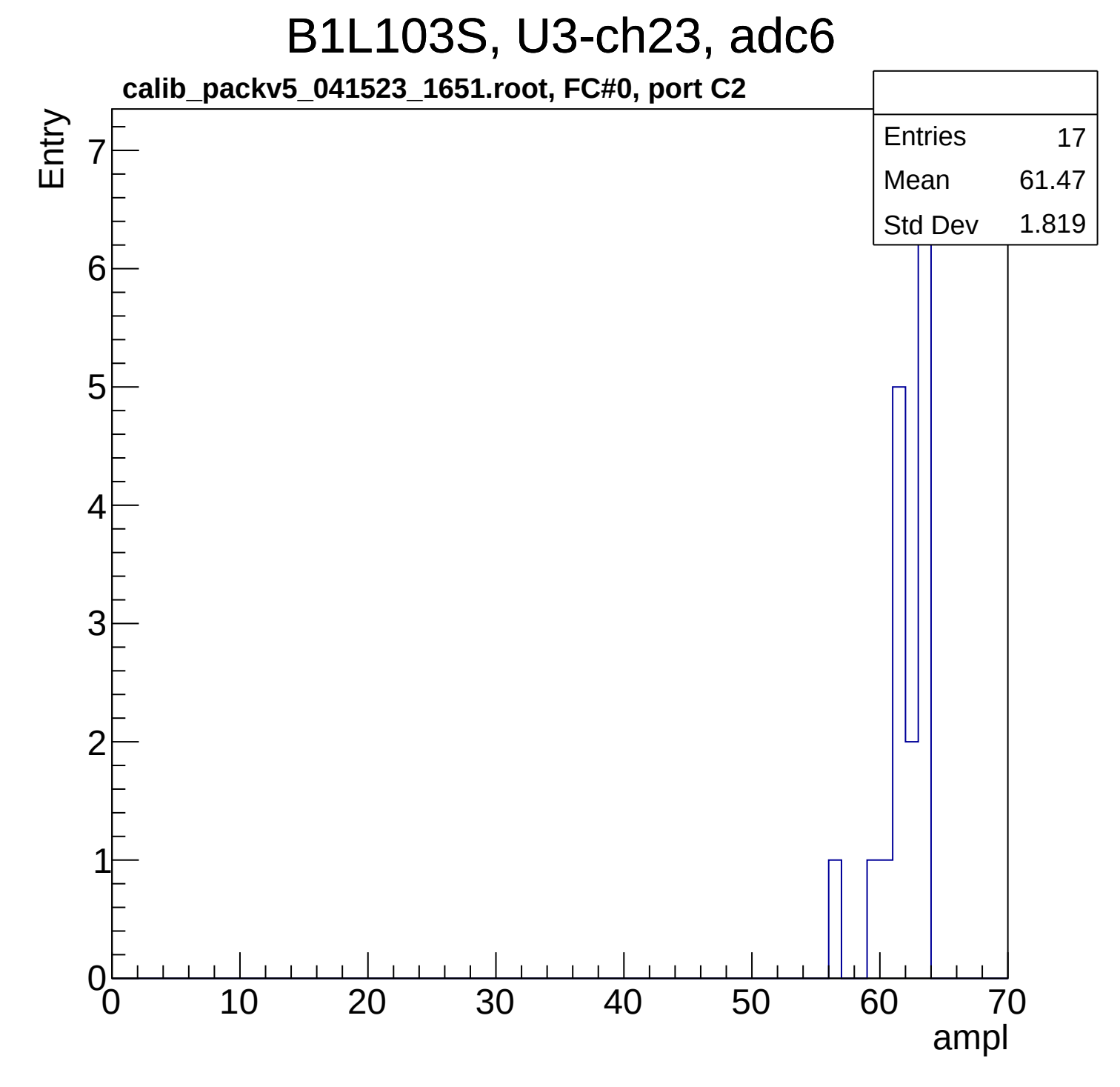
B1L103S, U3-ch23, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 61.47
Std Dev 1.819
Entry
ampl
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2
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4
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0
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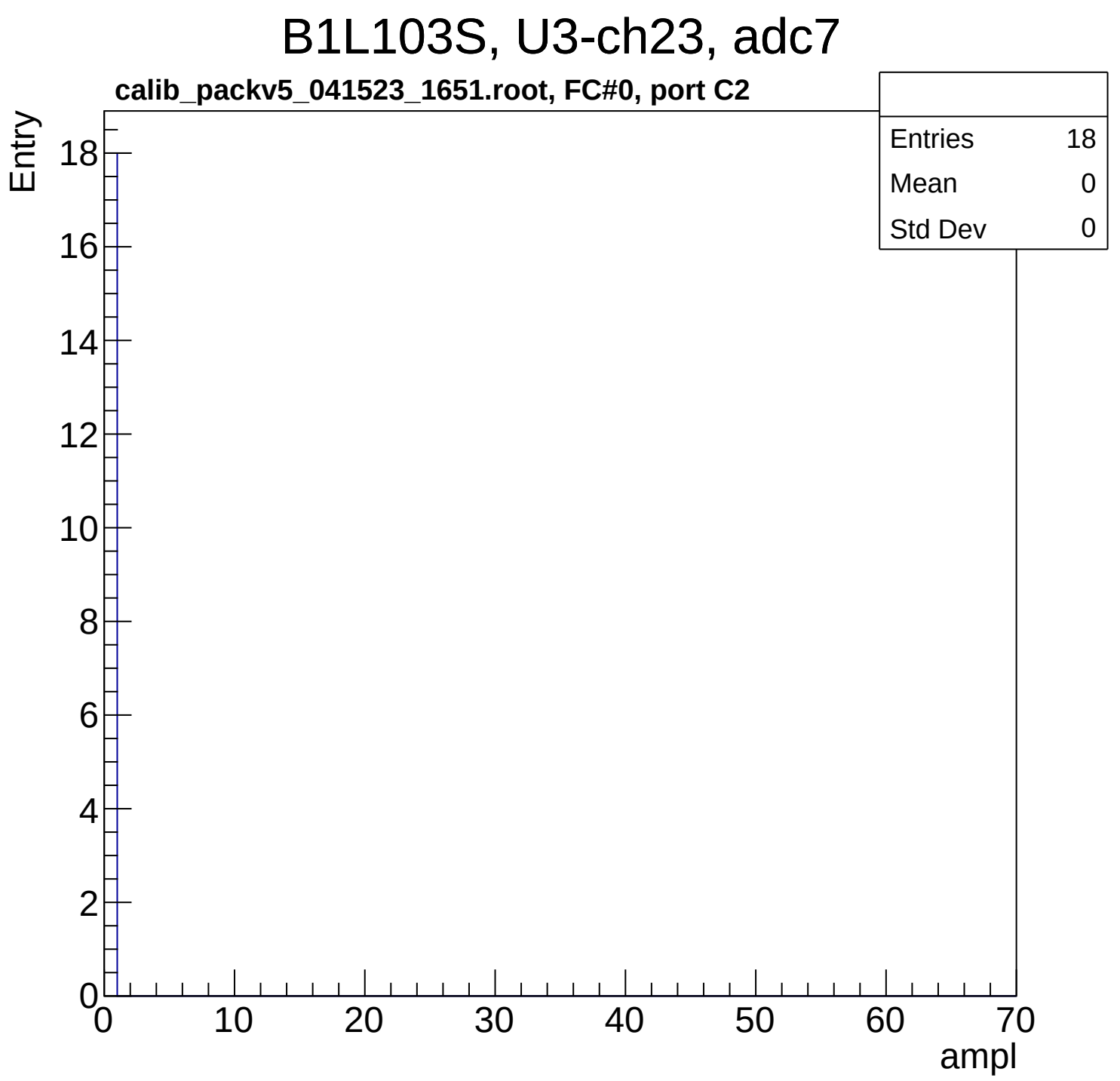
B1L103S, U3-ch23, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
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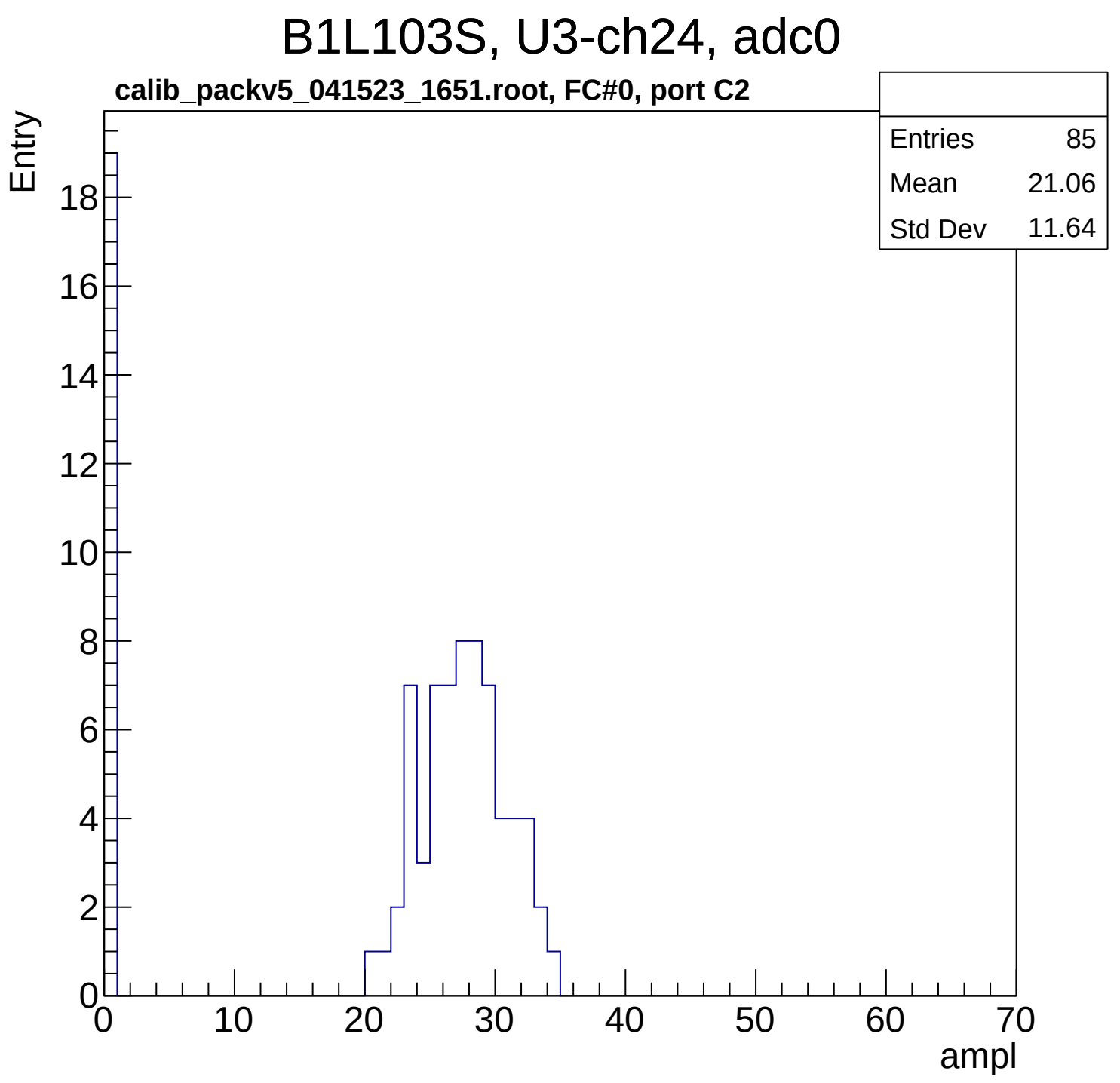
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch24, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 21.06
Std Dev 11.64
Entry
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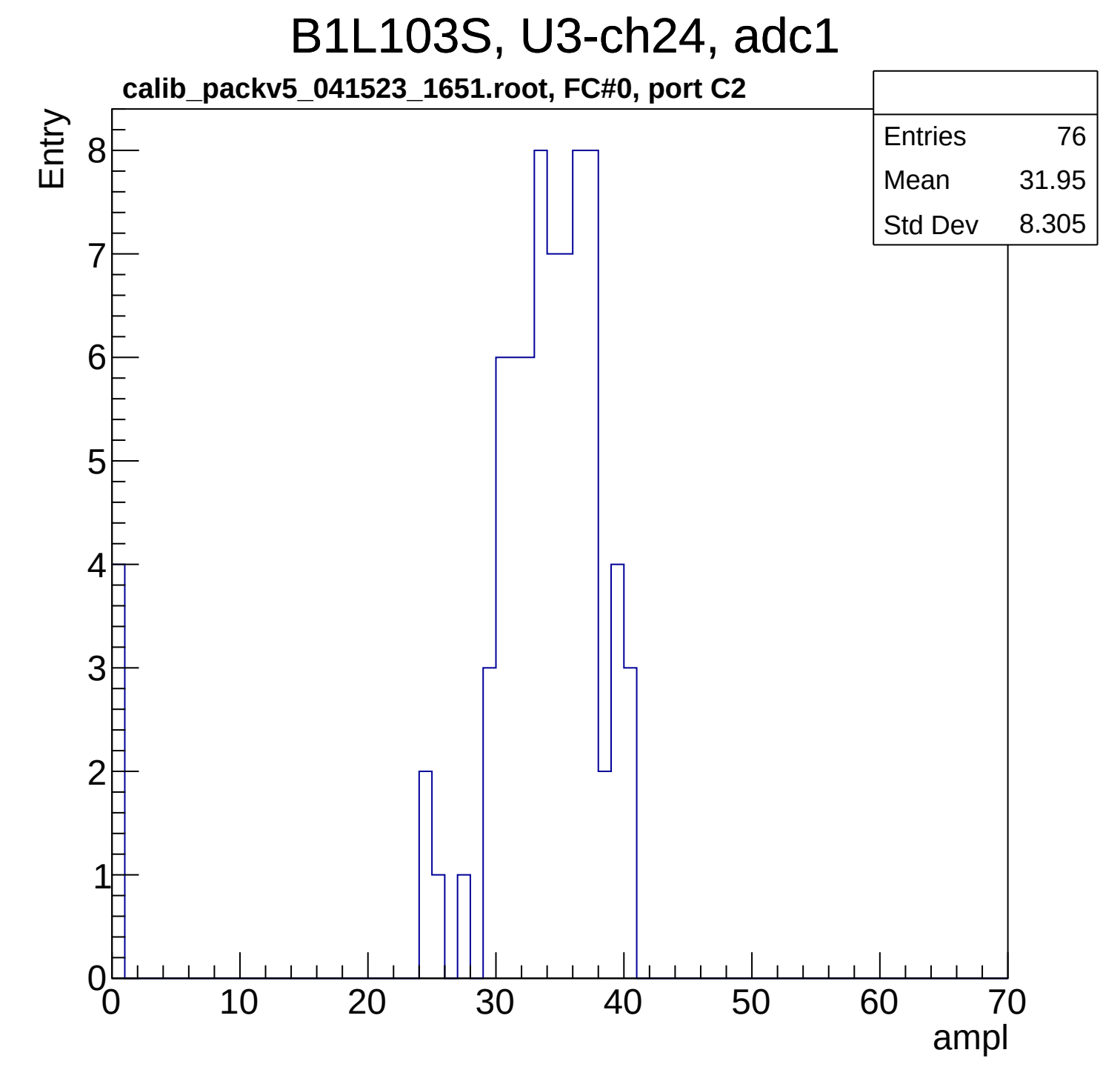
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch24, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 31.95
Std Dev 8.305
Entry
ampl
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2
3
4
5
6
7
8
0
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40
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60
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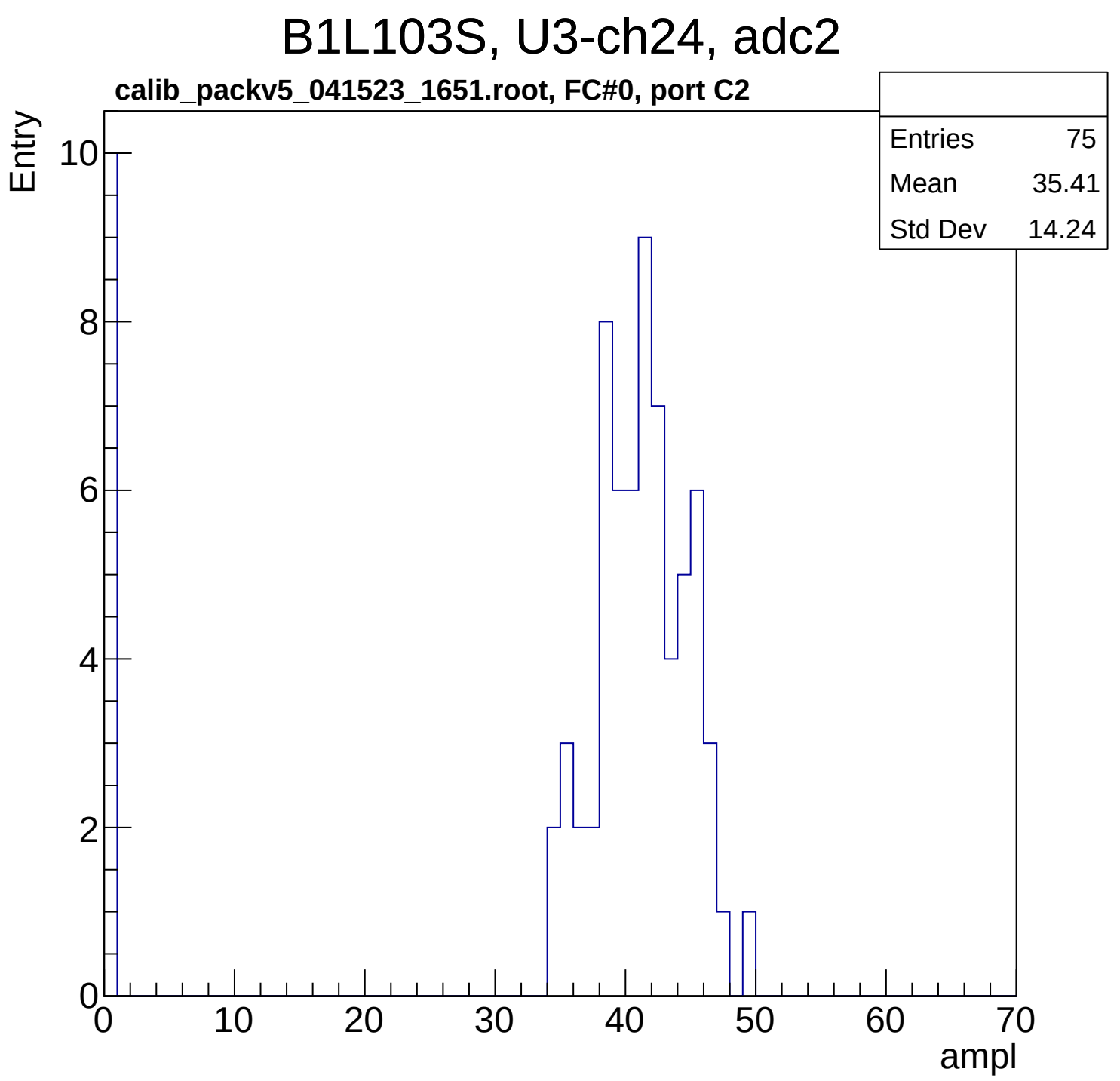
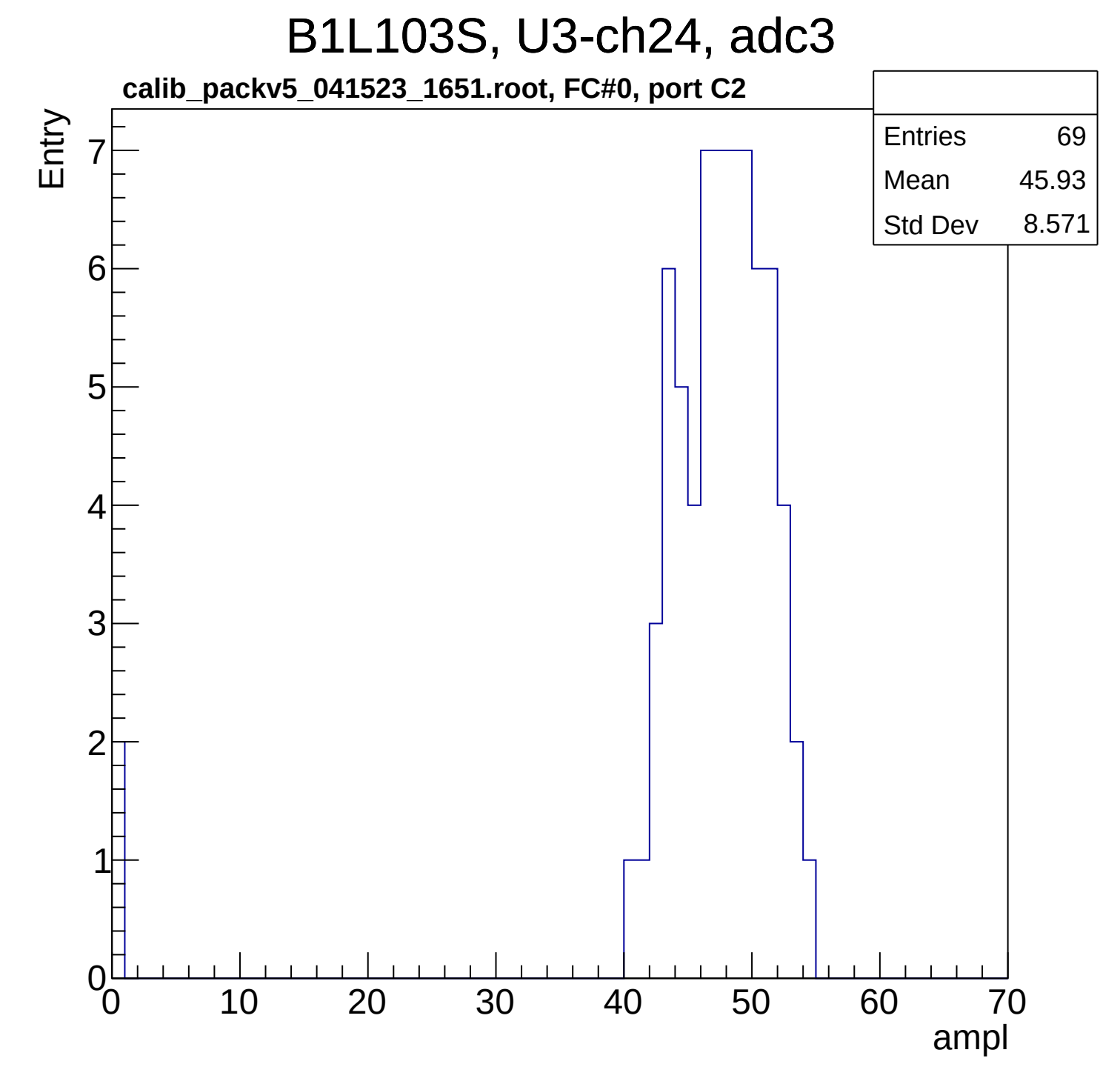
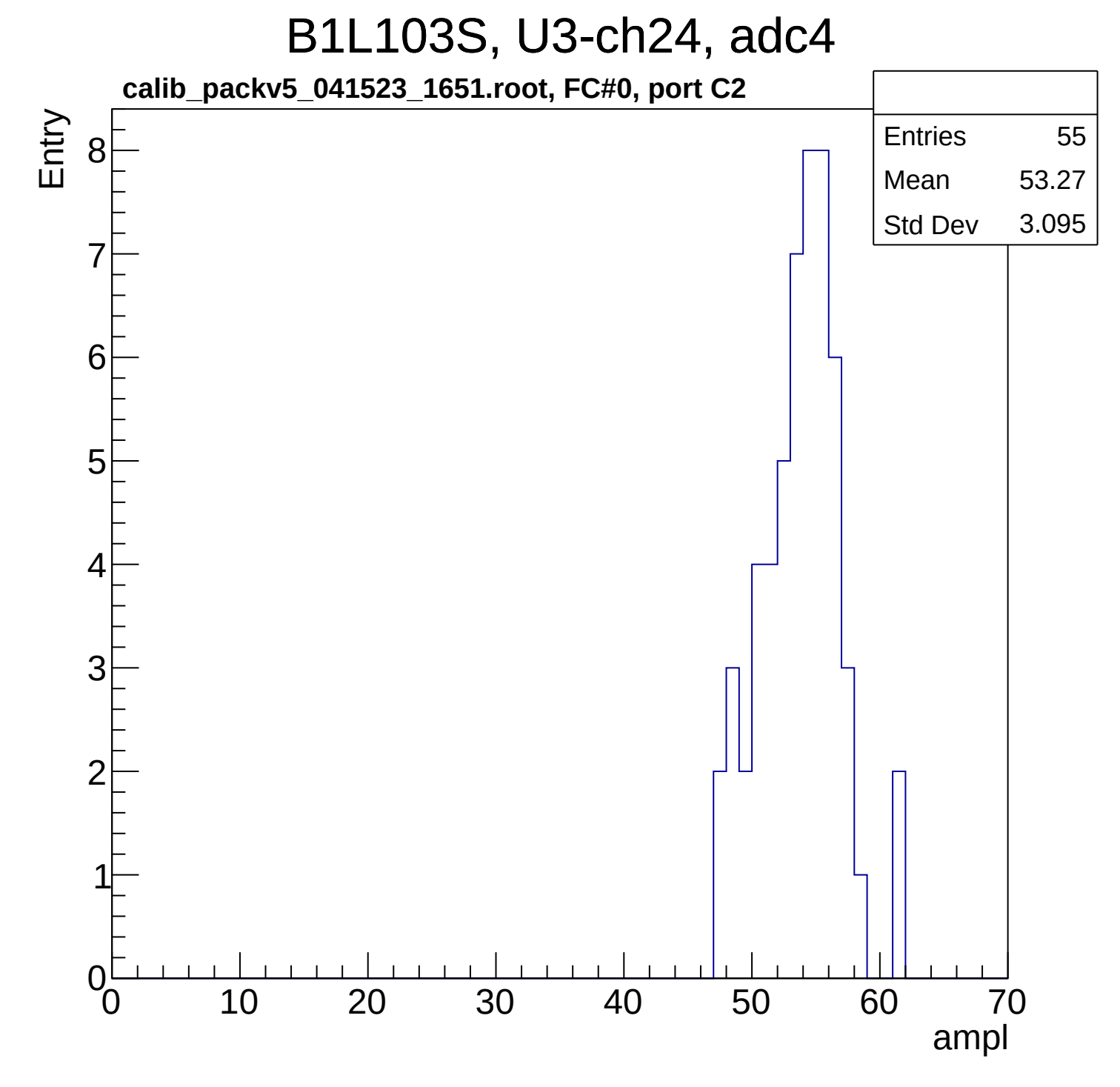
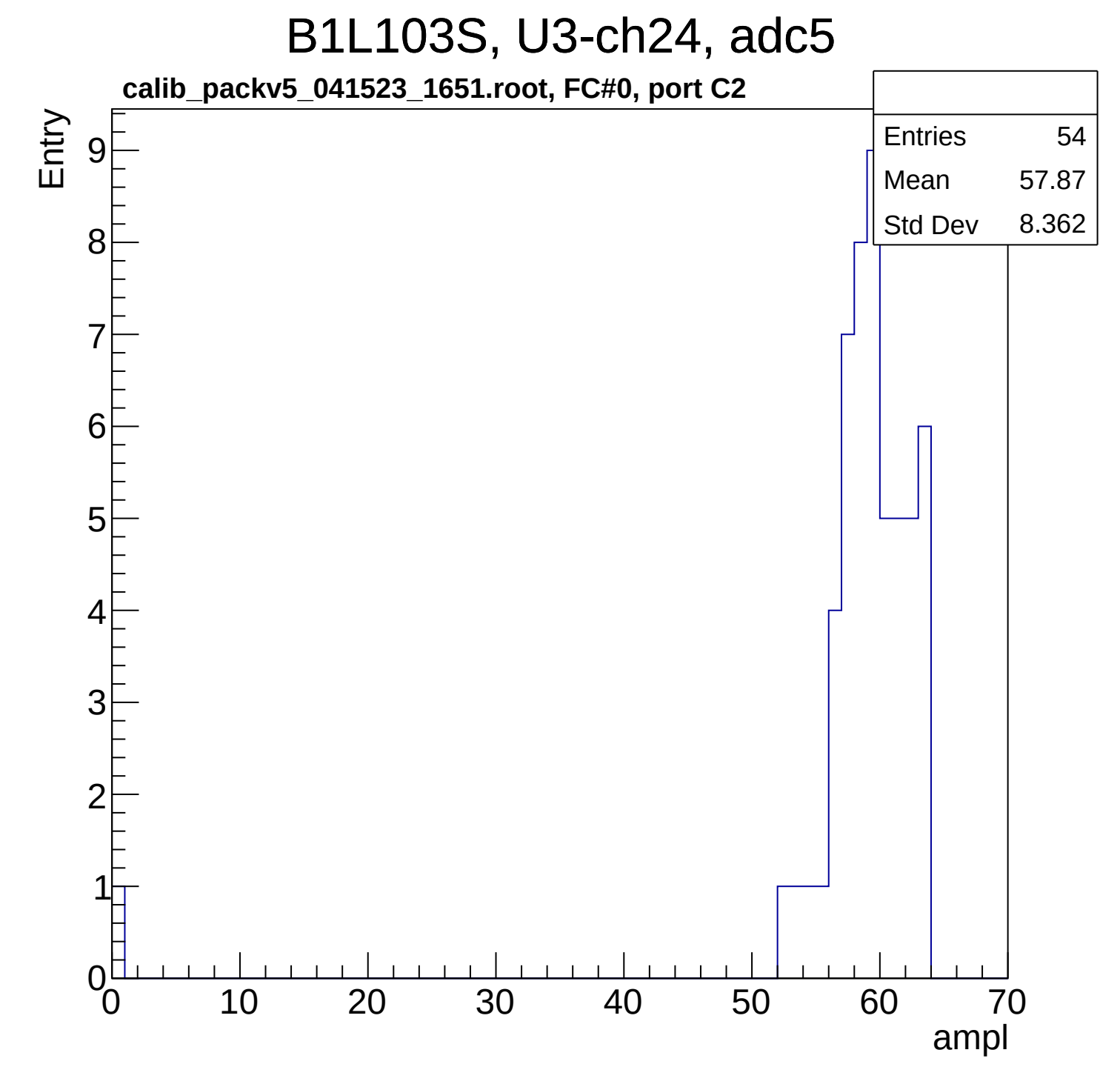

B1L103S, U3-ch24, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 35.41
Std Dev 14.24
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch24, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 45.93
Std Dev 8.571
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch24, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 53.27
Std Dev 3.095
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch24, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 57.87
Std Dev 8.362
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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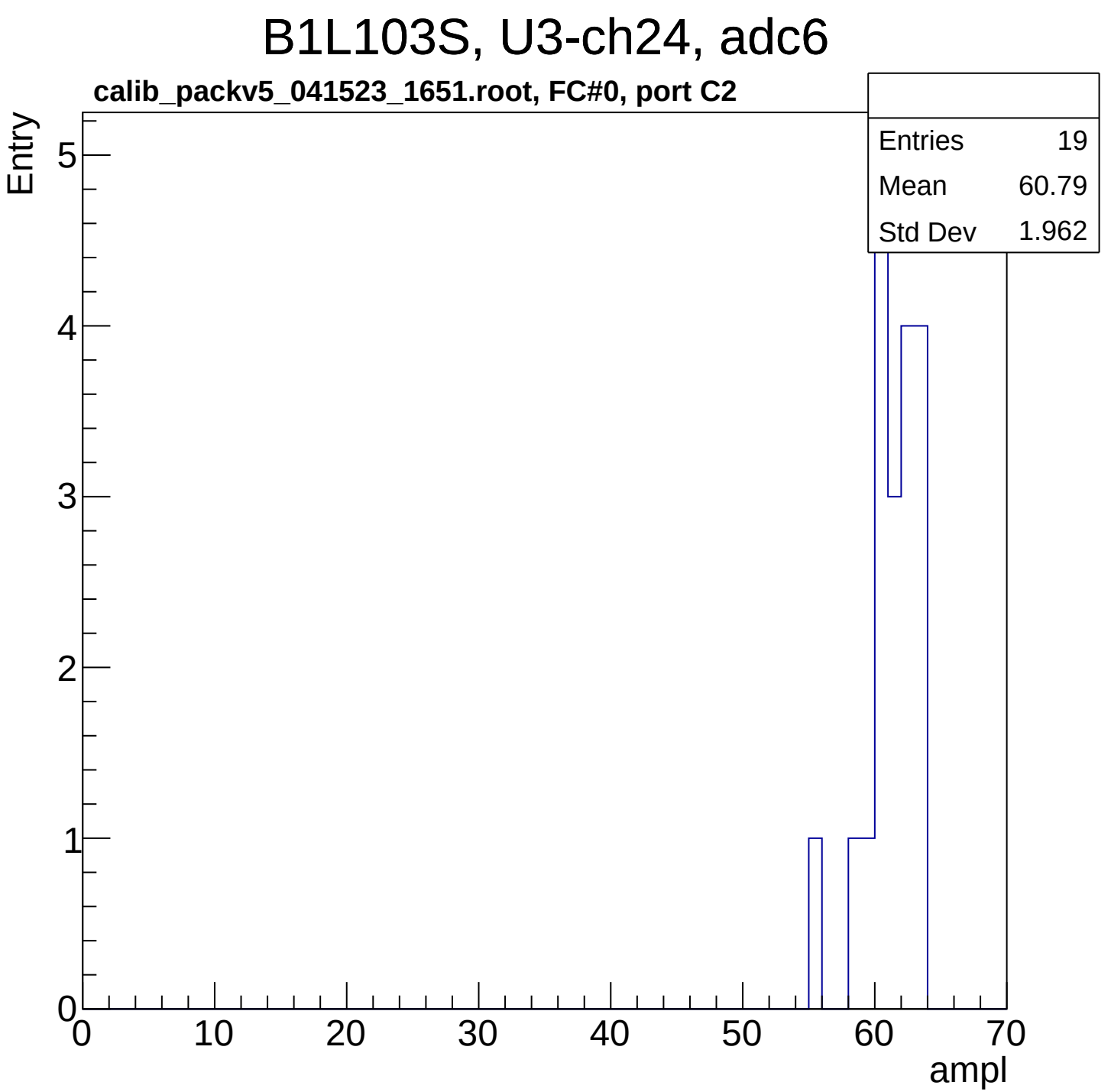
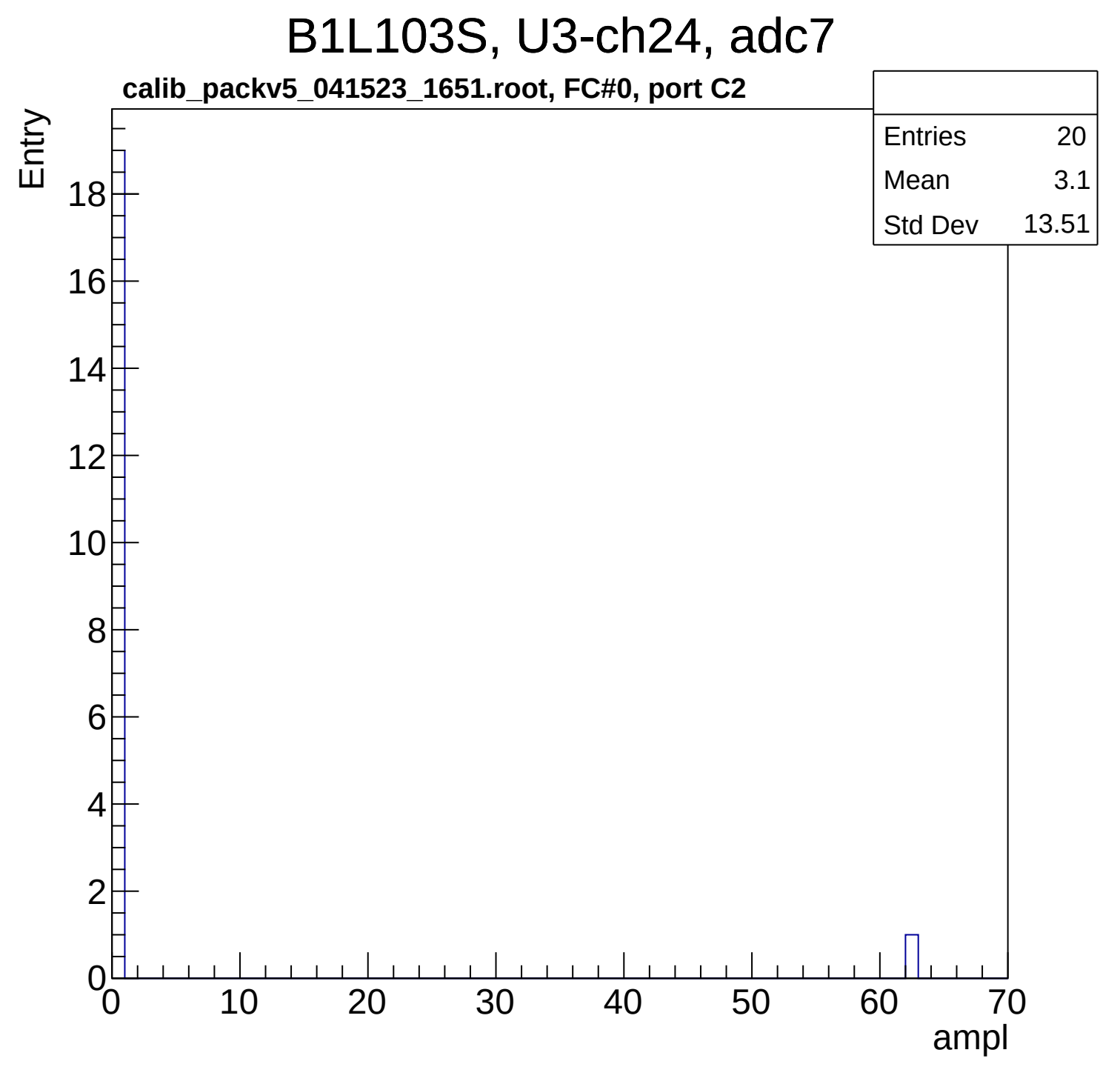

B1L103S, U3-ch24, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 60.79
Std Dev 1.962
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U3-ch24, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
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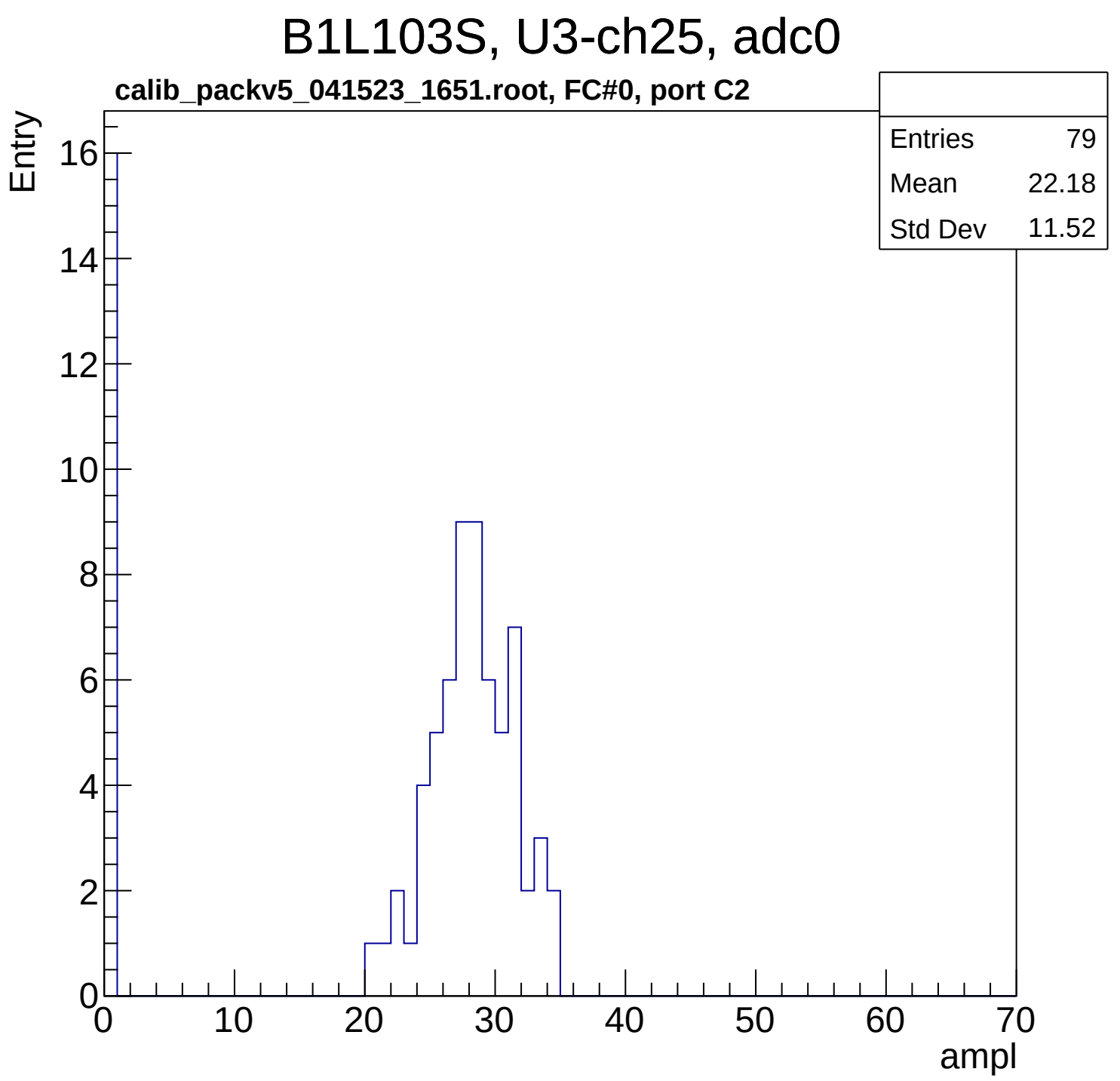
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch25, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 22.18
Std Dev 11.52
Entry
ampl
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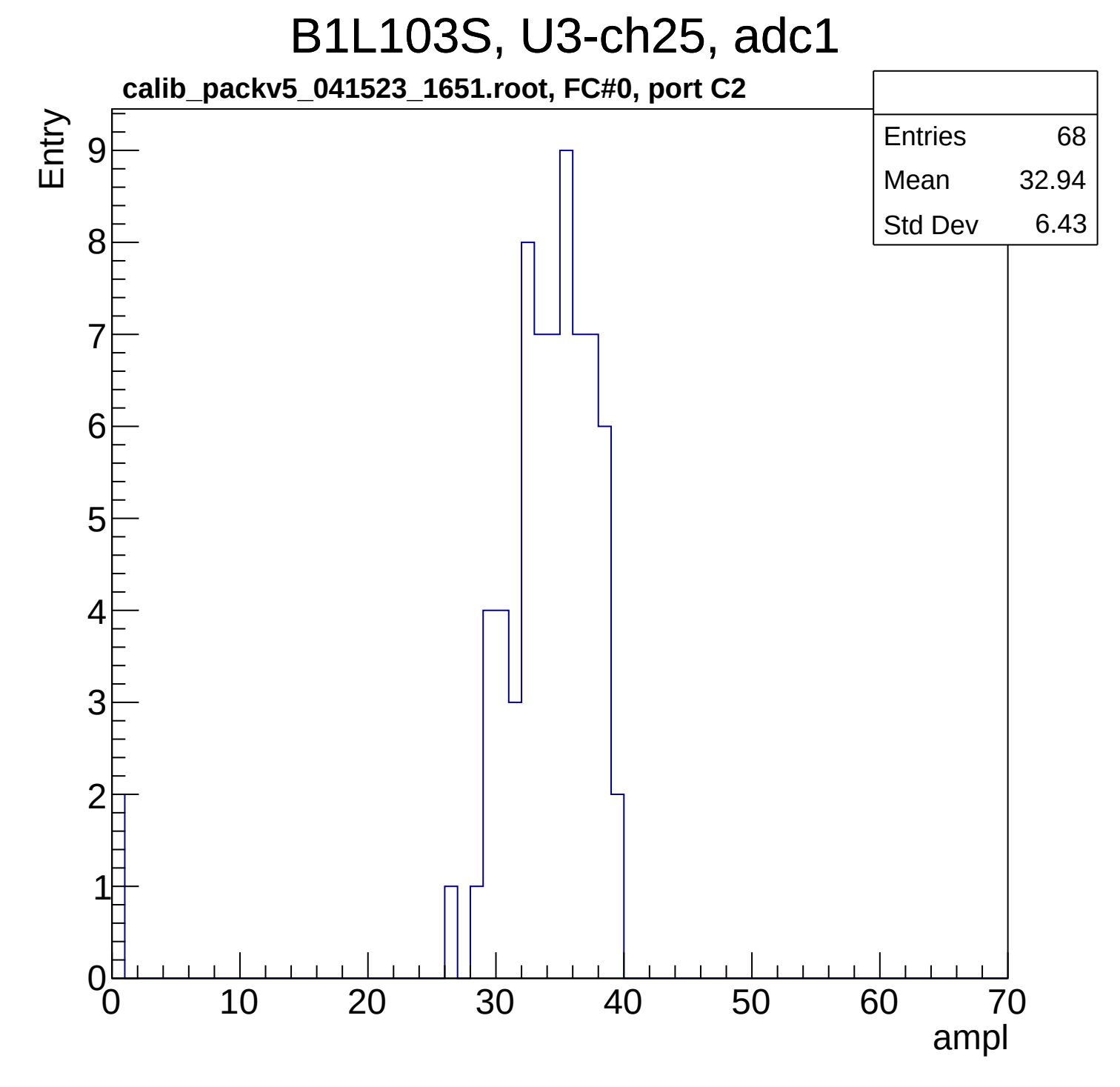
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L103S, U3-ch25, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 32.94
Std Dev 6.43
Entry
ampl
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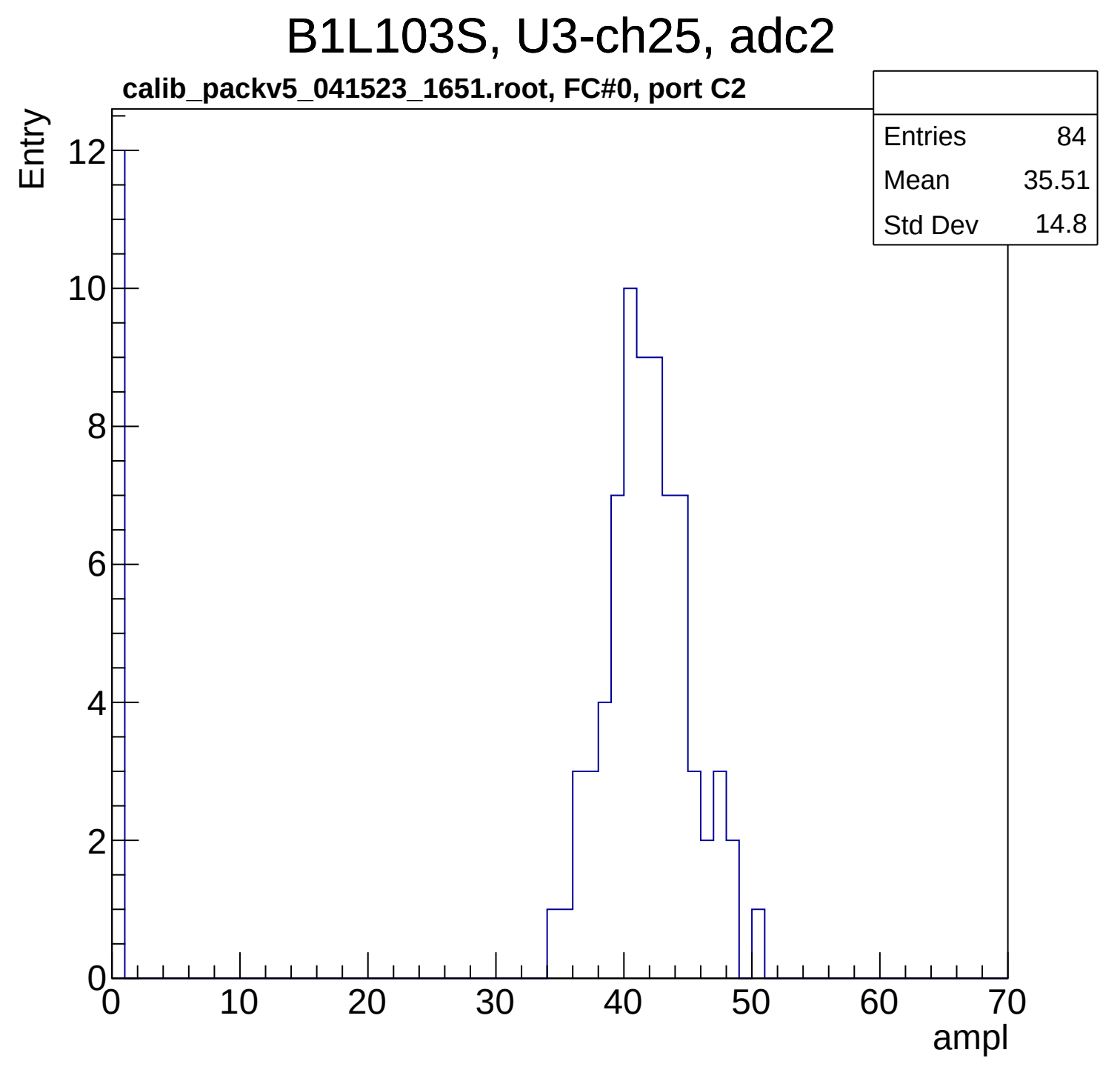
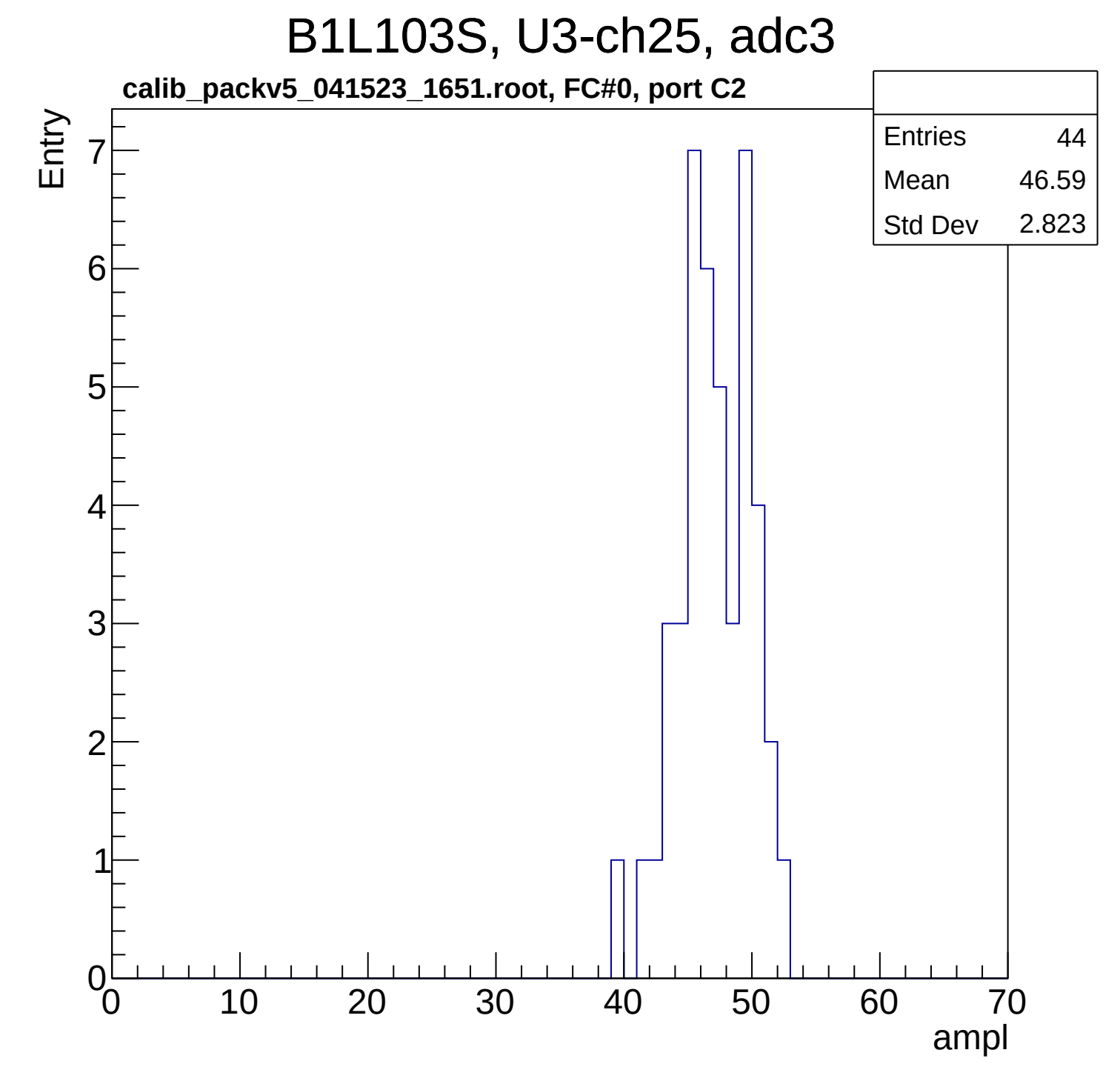
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch25, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 35.51
Std Dev 14.8
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch25, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 46.59
Std Dev 2.823
Entry
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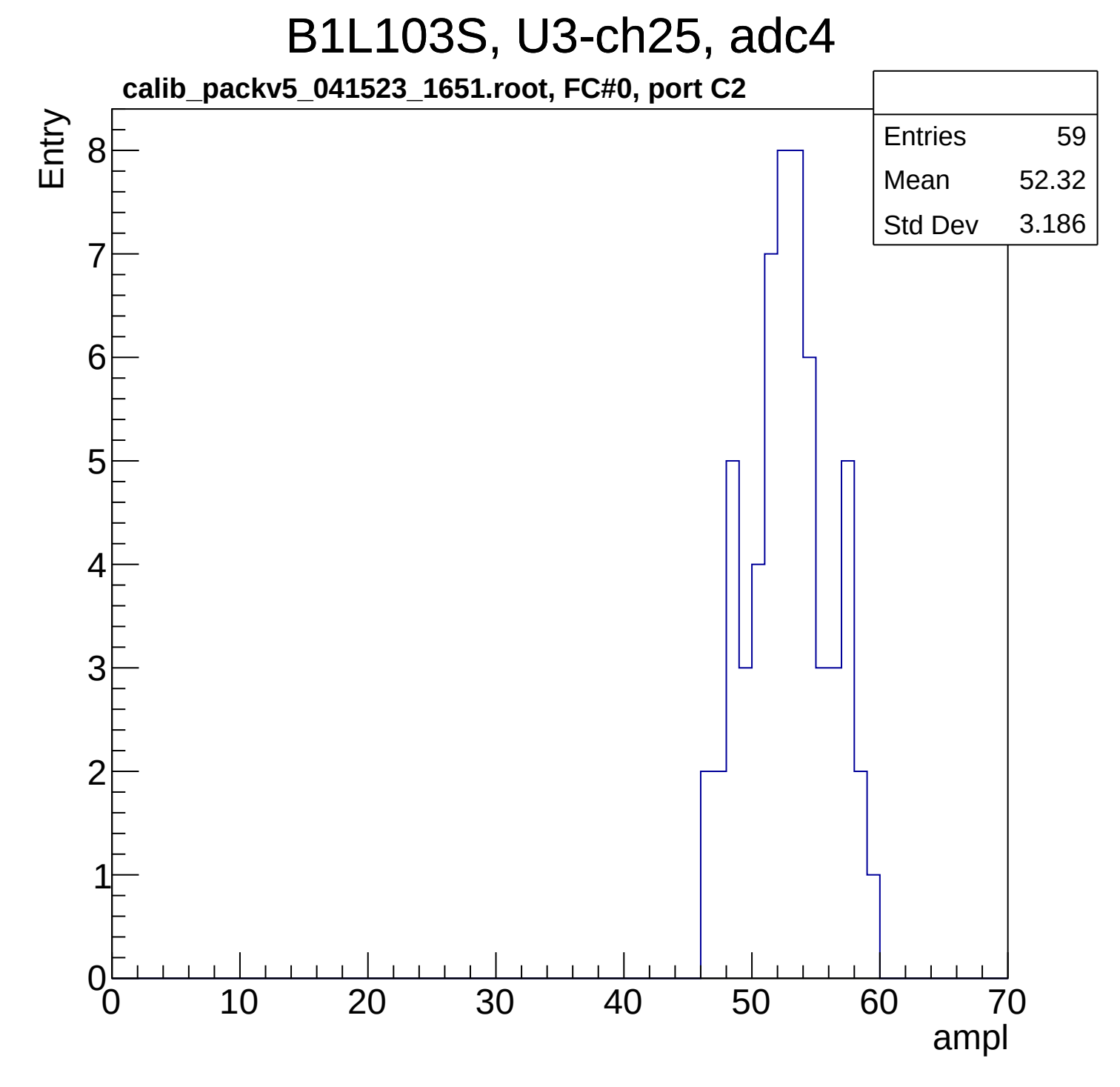
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch25, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 52.32
Std Dev 3.186
Entry
ampl
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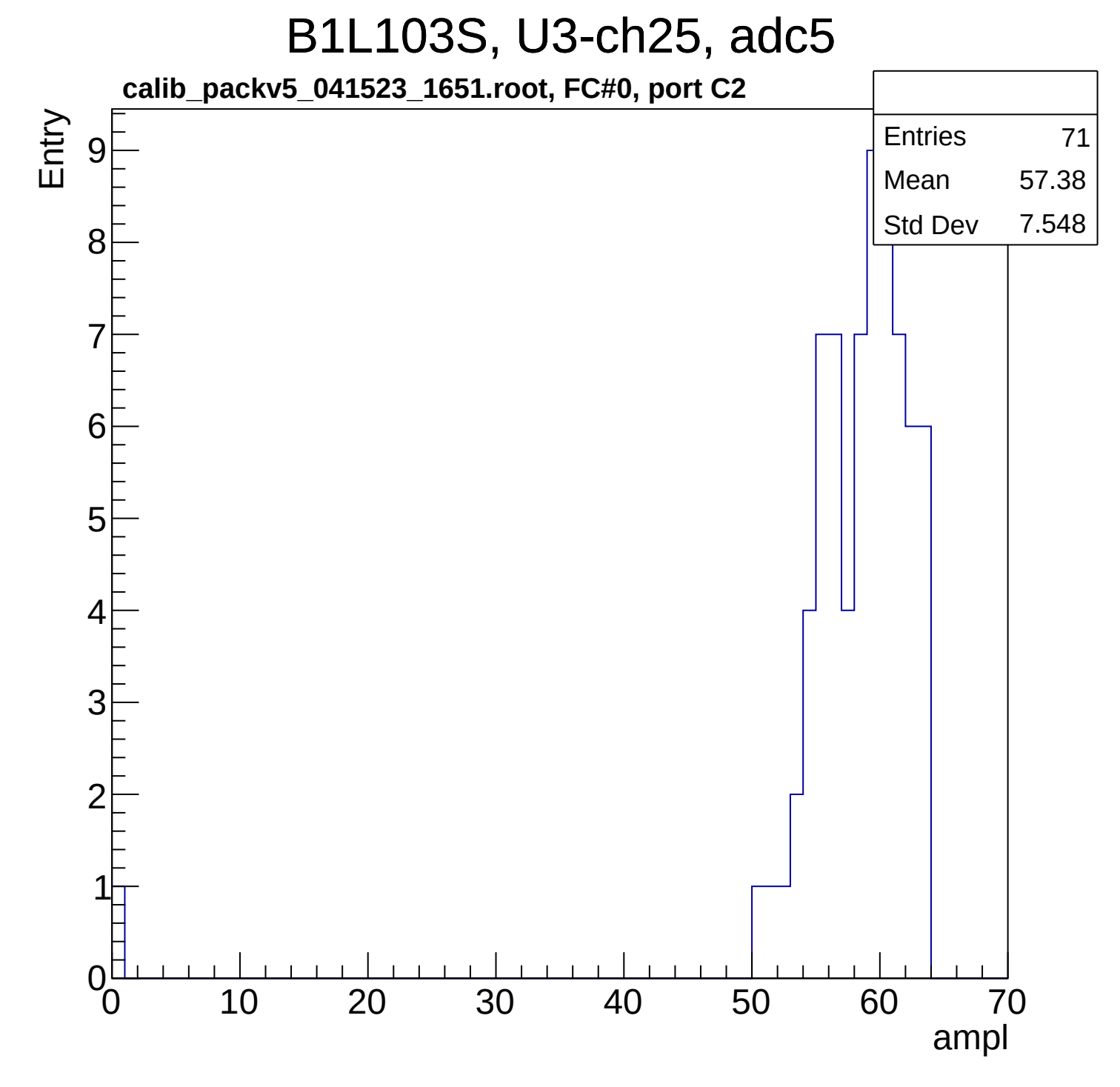
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch25, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 57.38
Std Dev 7.548
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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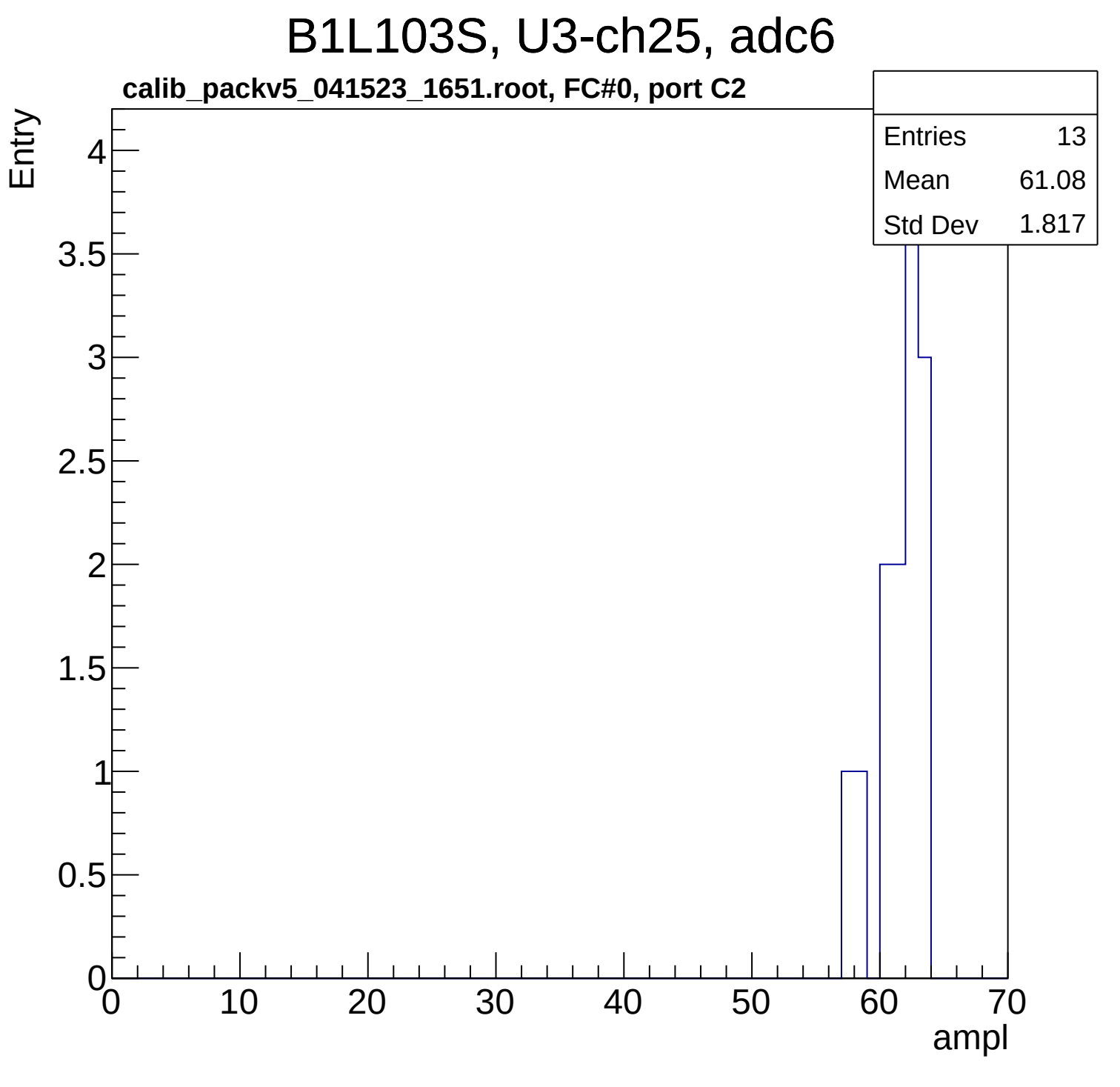
60
70


B1L103S, U3-ch25, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 61.08
Std Dev 1.817
Entry
ampl
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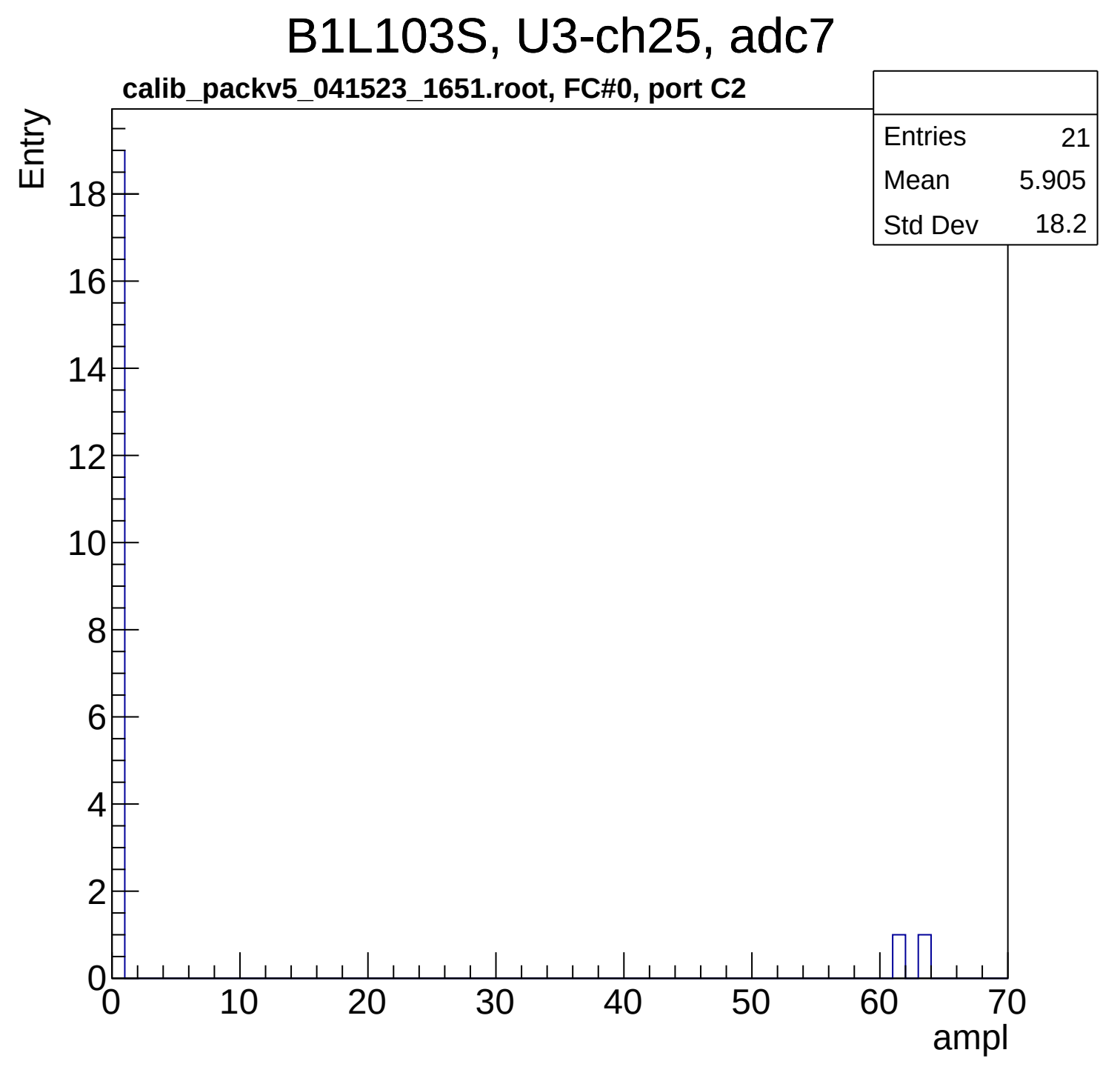
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U3-ch25, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.905
Std Dev 18.2
Entry
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6
8
10
12
14
16
18
0
10
20
30
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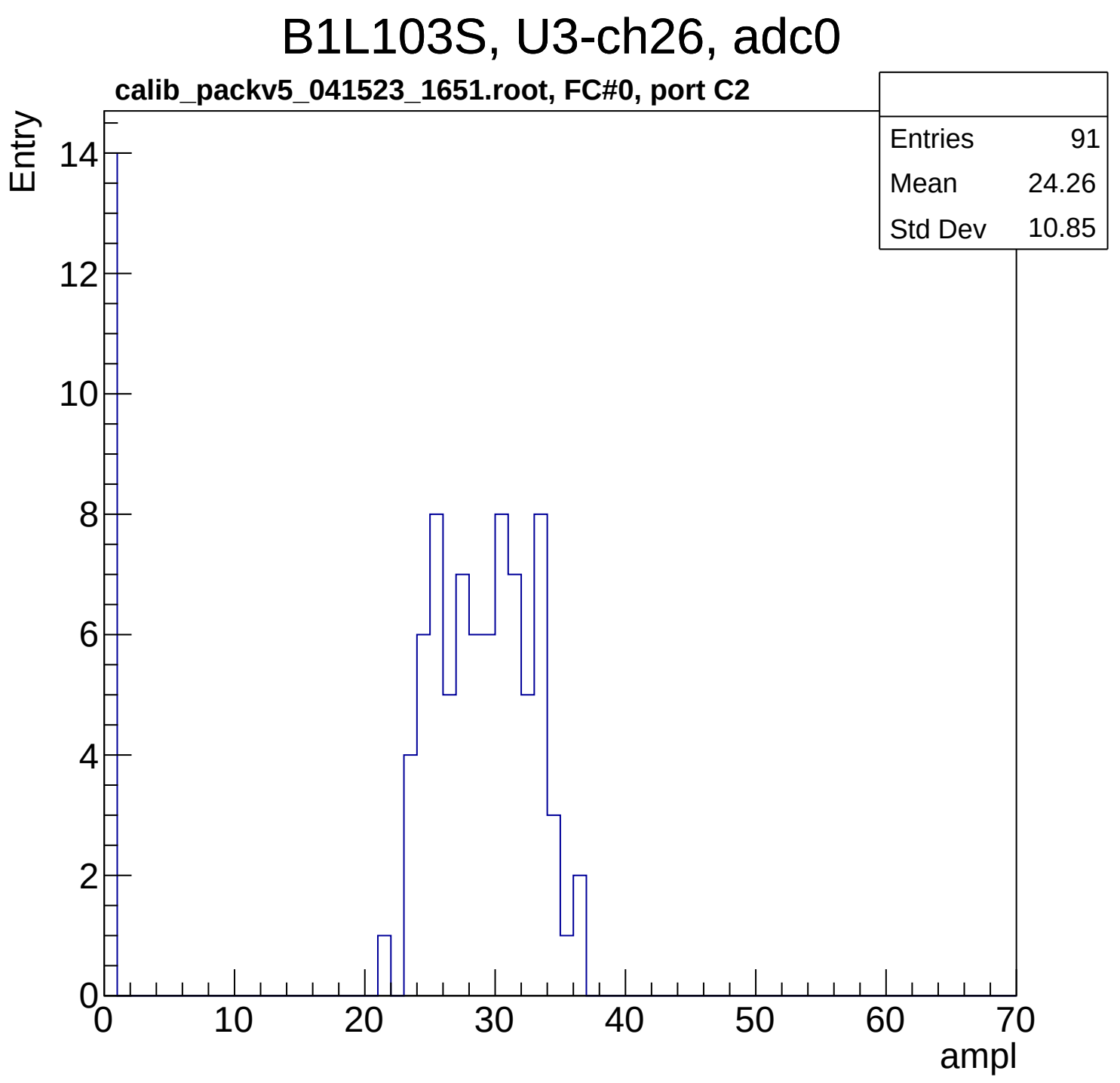
50
60
70
ampl


B1L103S, U3-ch26, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 24.26
Std Dev 10.85
Entry
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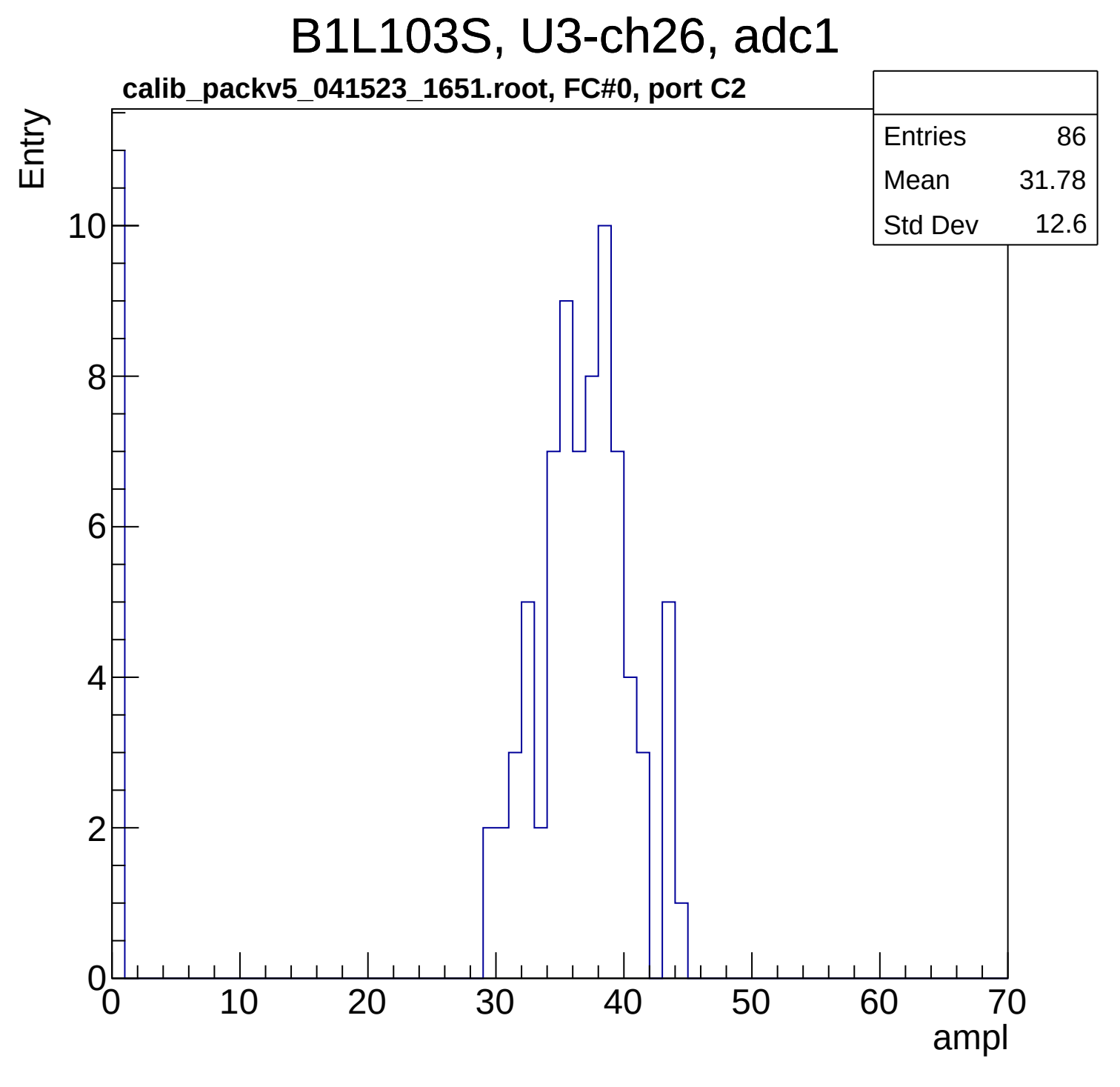
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch26, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 31.78
Std Dev 12.6
Entry
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4
6
8
10
0
10
20
30
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50
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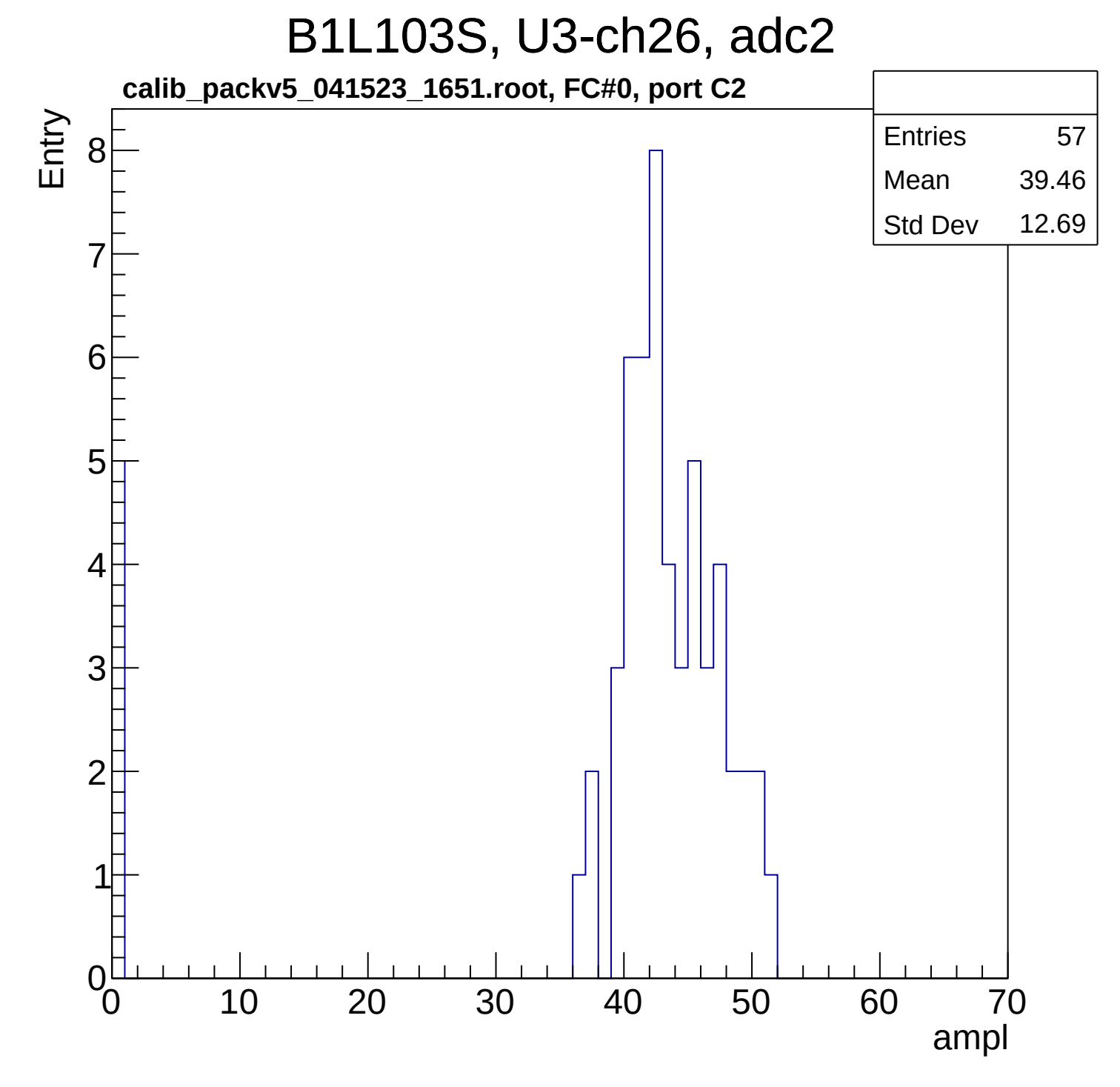
70
ampl


B1L103S, U3-ch26, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 39.46
Std Dev 12.69
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
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40
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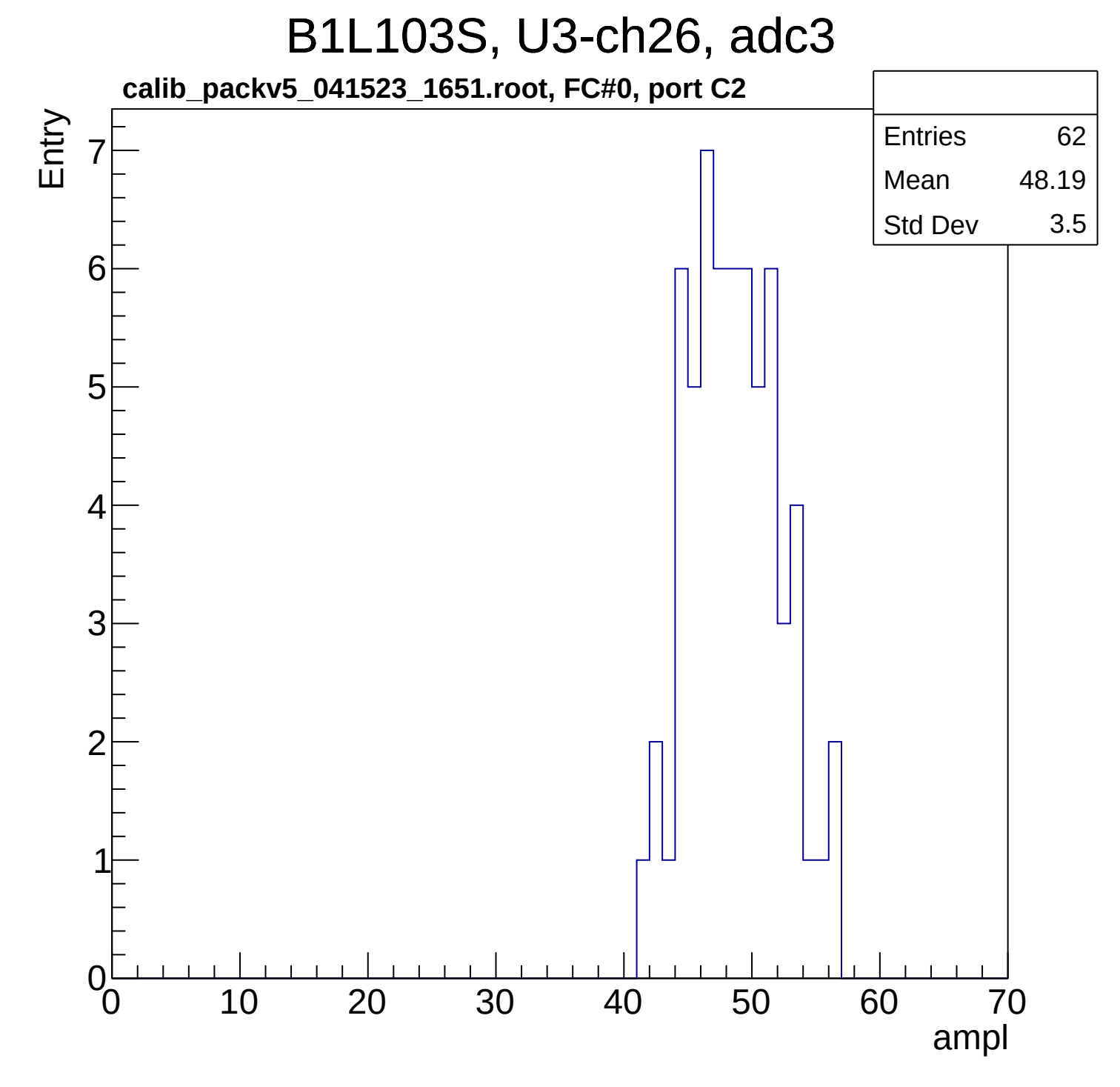
60
70


B1L103S, U3-ch26, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 48.19
Std Dev 3.5
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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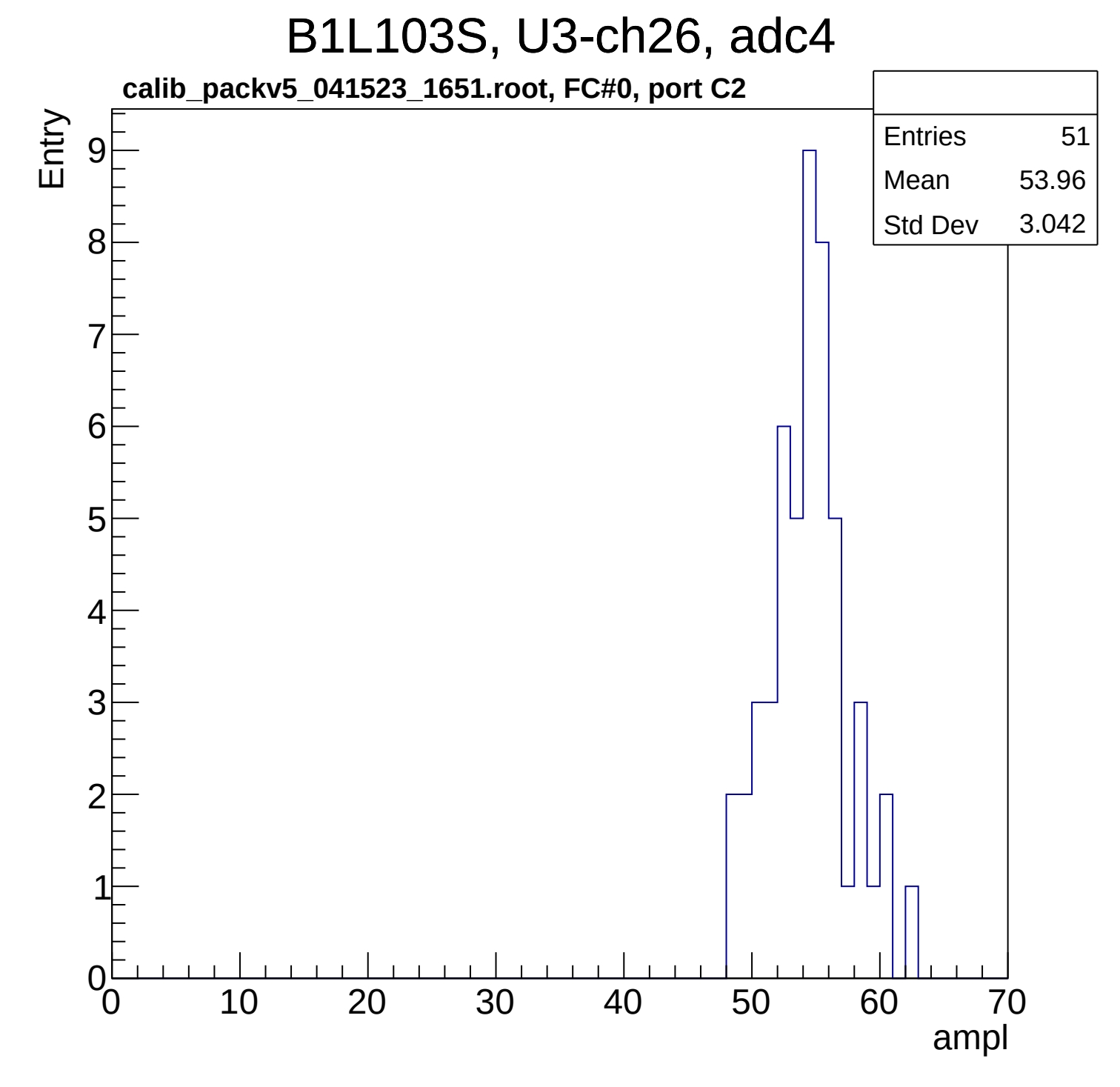
40
50
60
70


B1L103S, U3-ch26, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 53.96
Std Dev 3.042
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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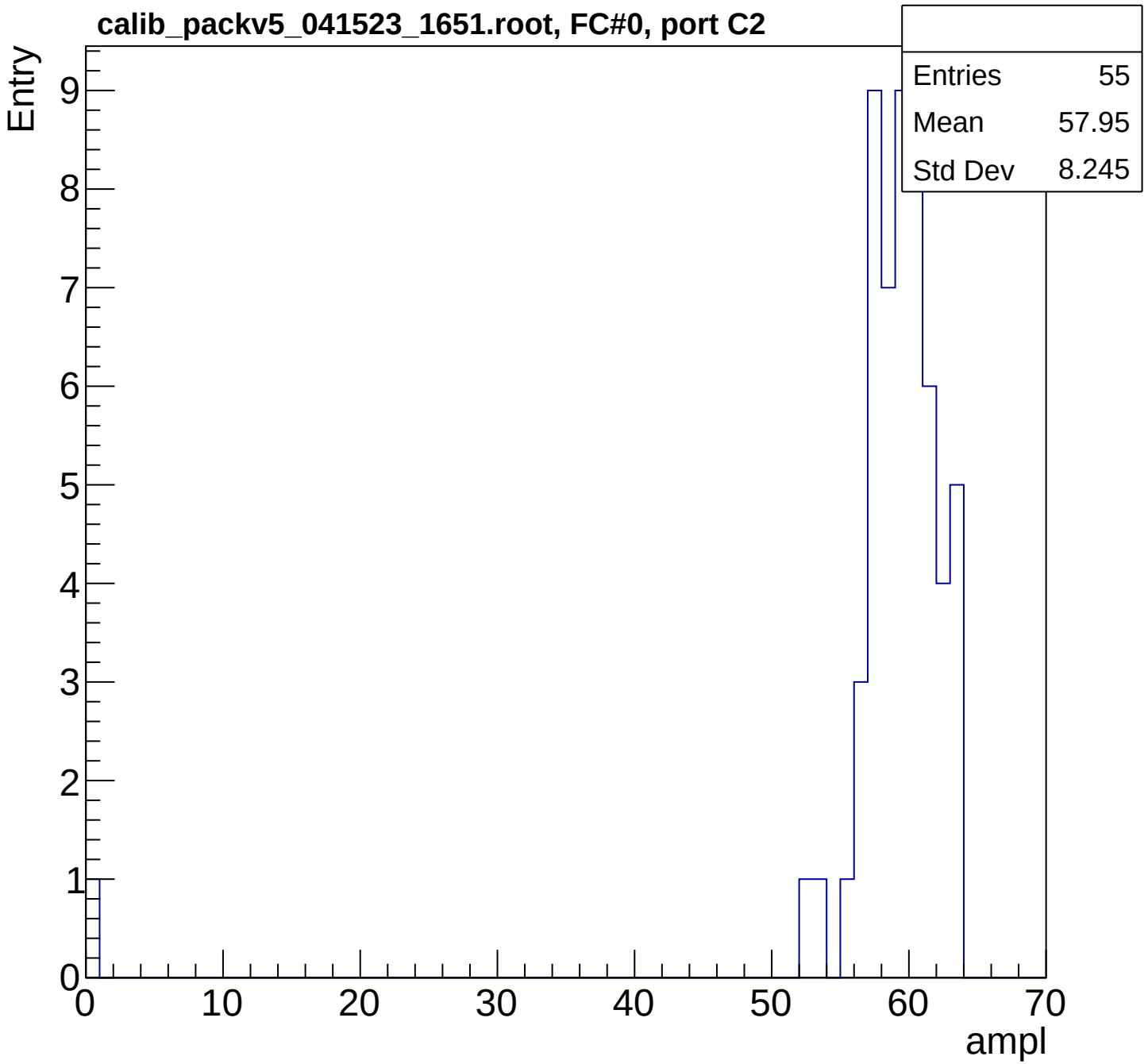
40
50
60
70


B1L103S, U3-ch26, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 57.95
Std Dev 8.245
Entry
ampl
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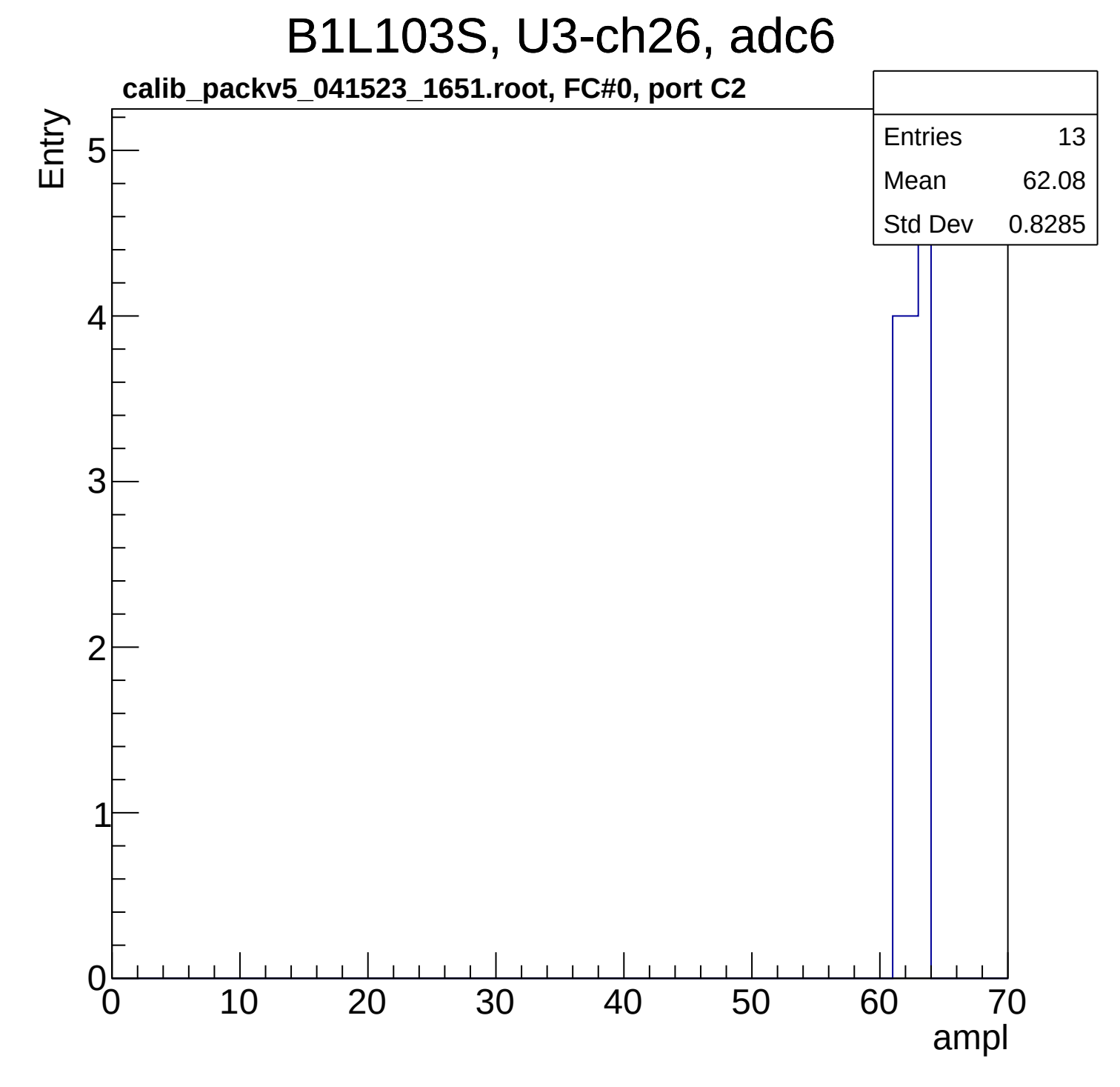
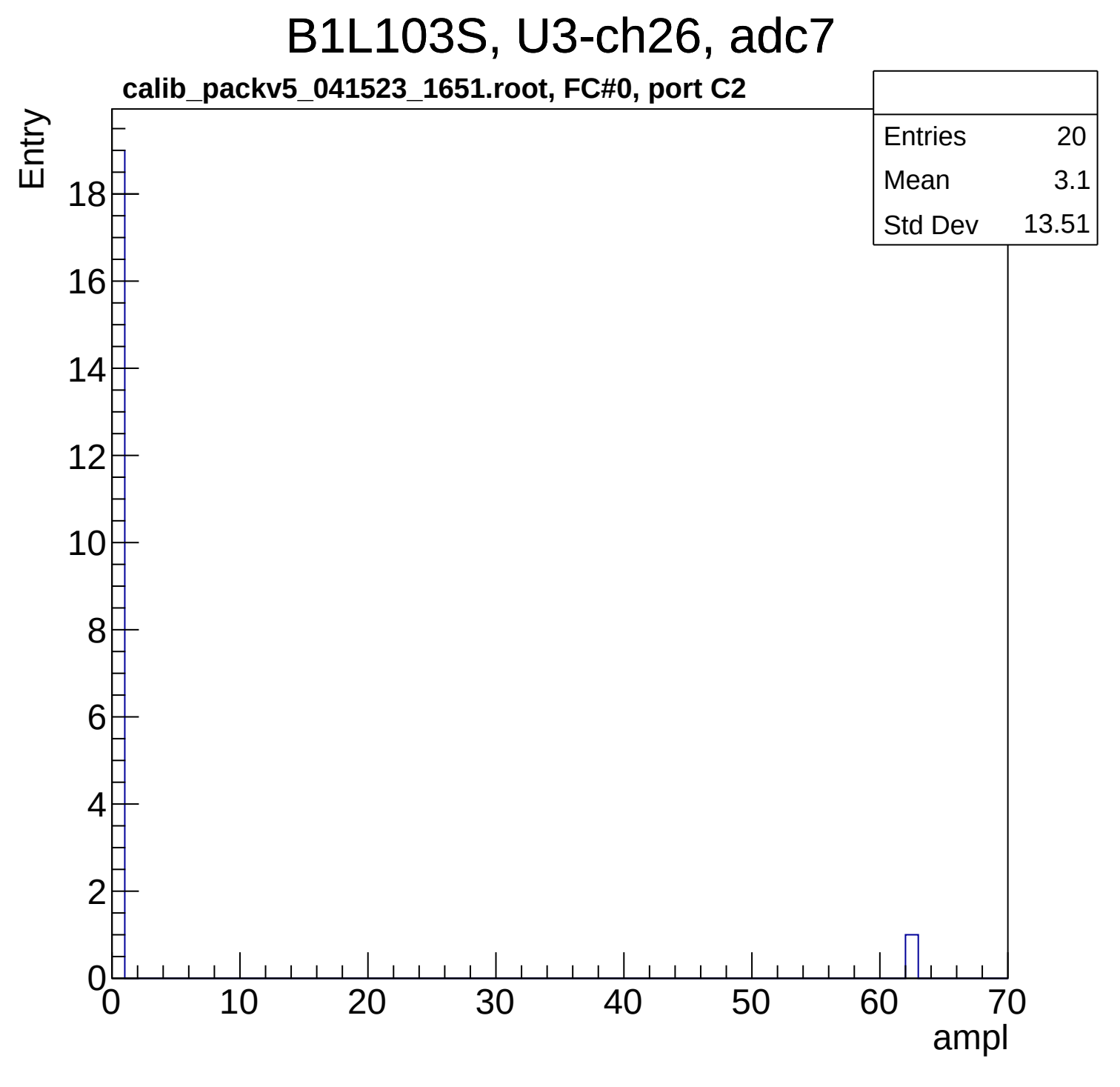
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch26, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 62.08
Std Dev 0.8285
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch26, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
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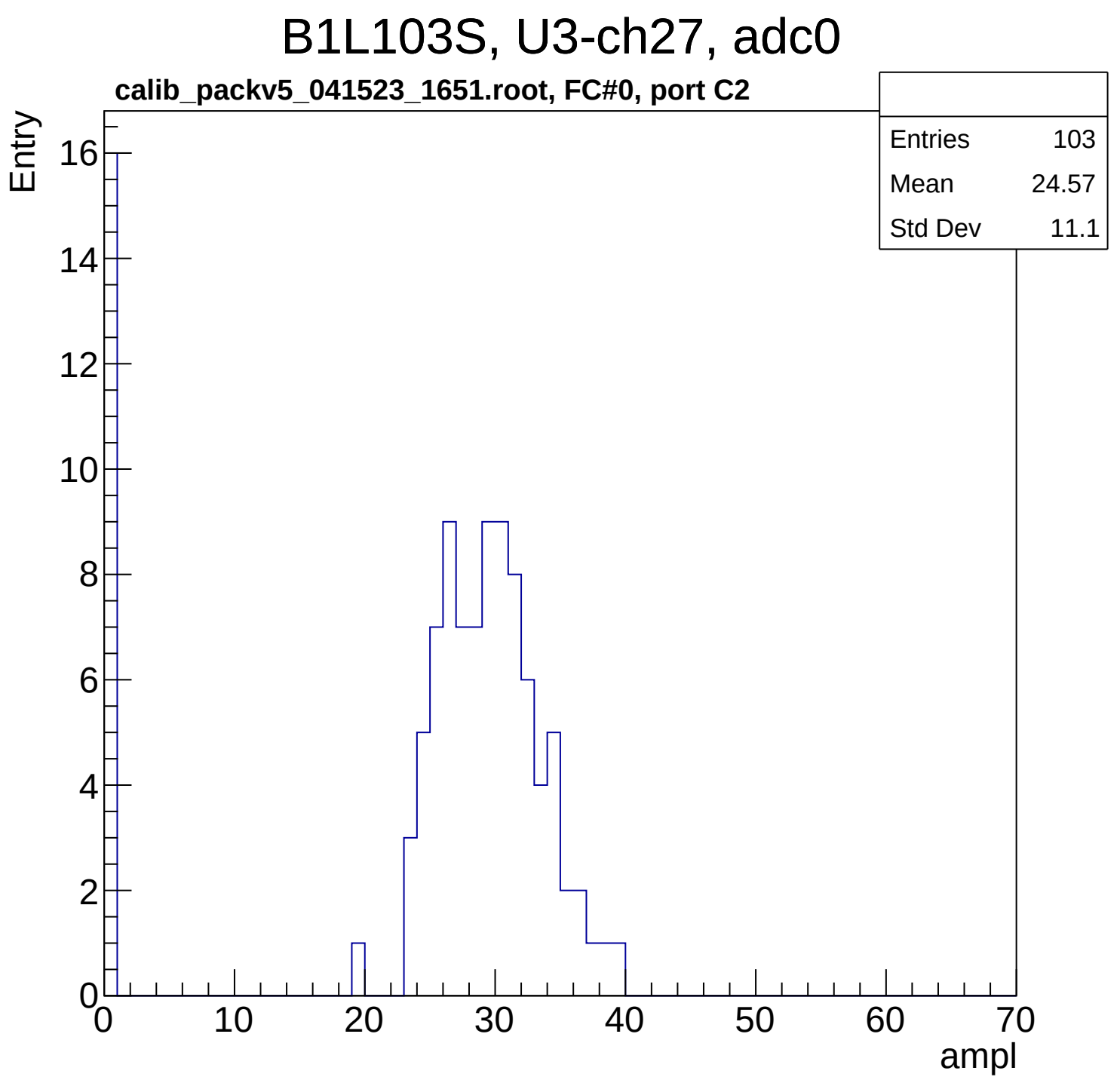
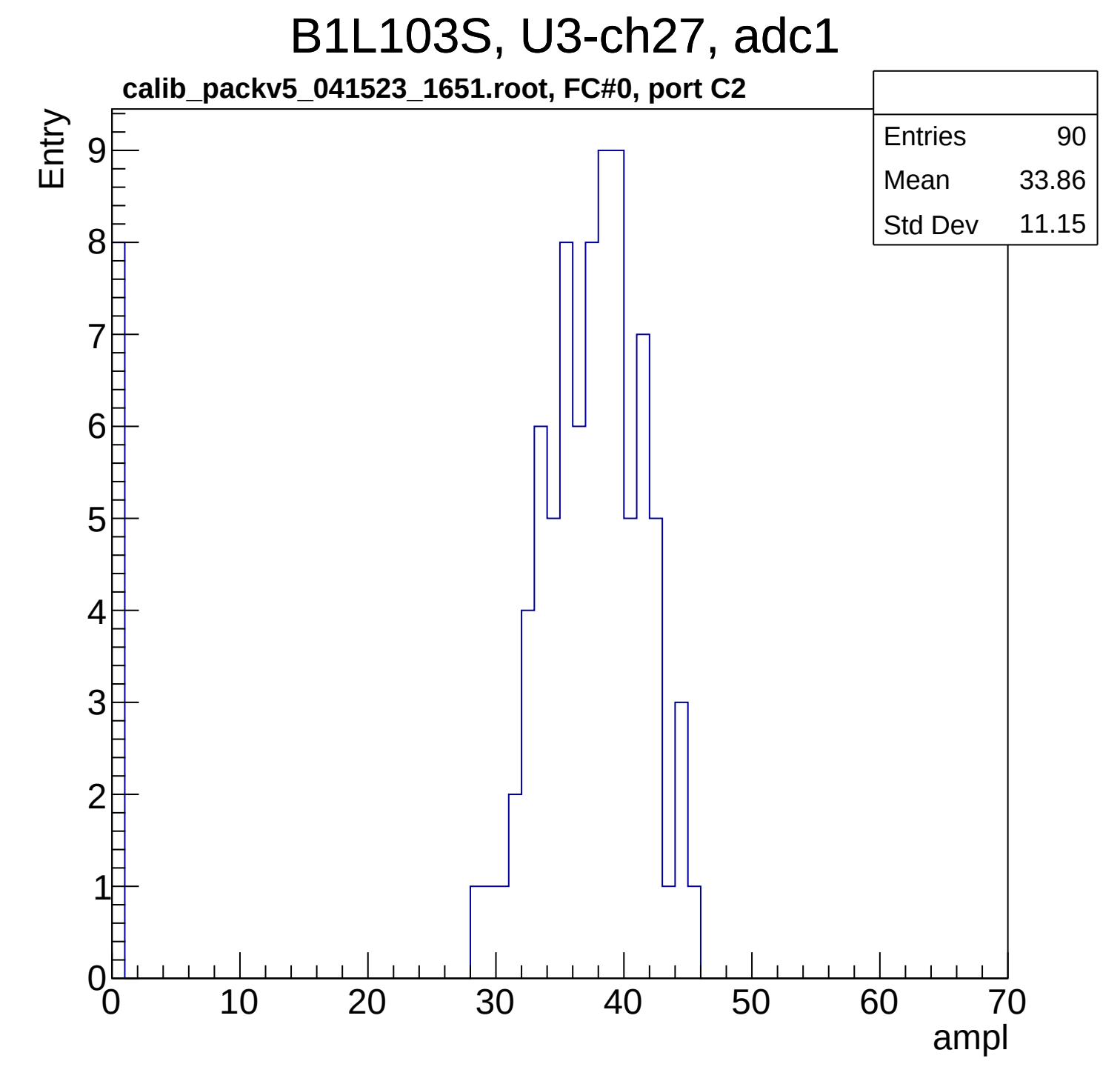
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch27, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 103
Mean 24.57
Std Dev 11.1
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch27, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 33.86
Std Dev 11.15
Entry
ampl
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2
3
4
5
6
7
8
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0
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60
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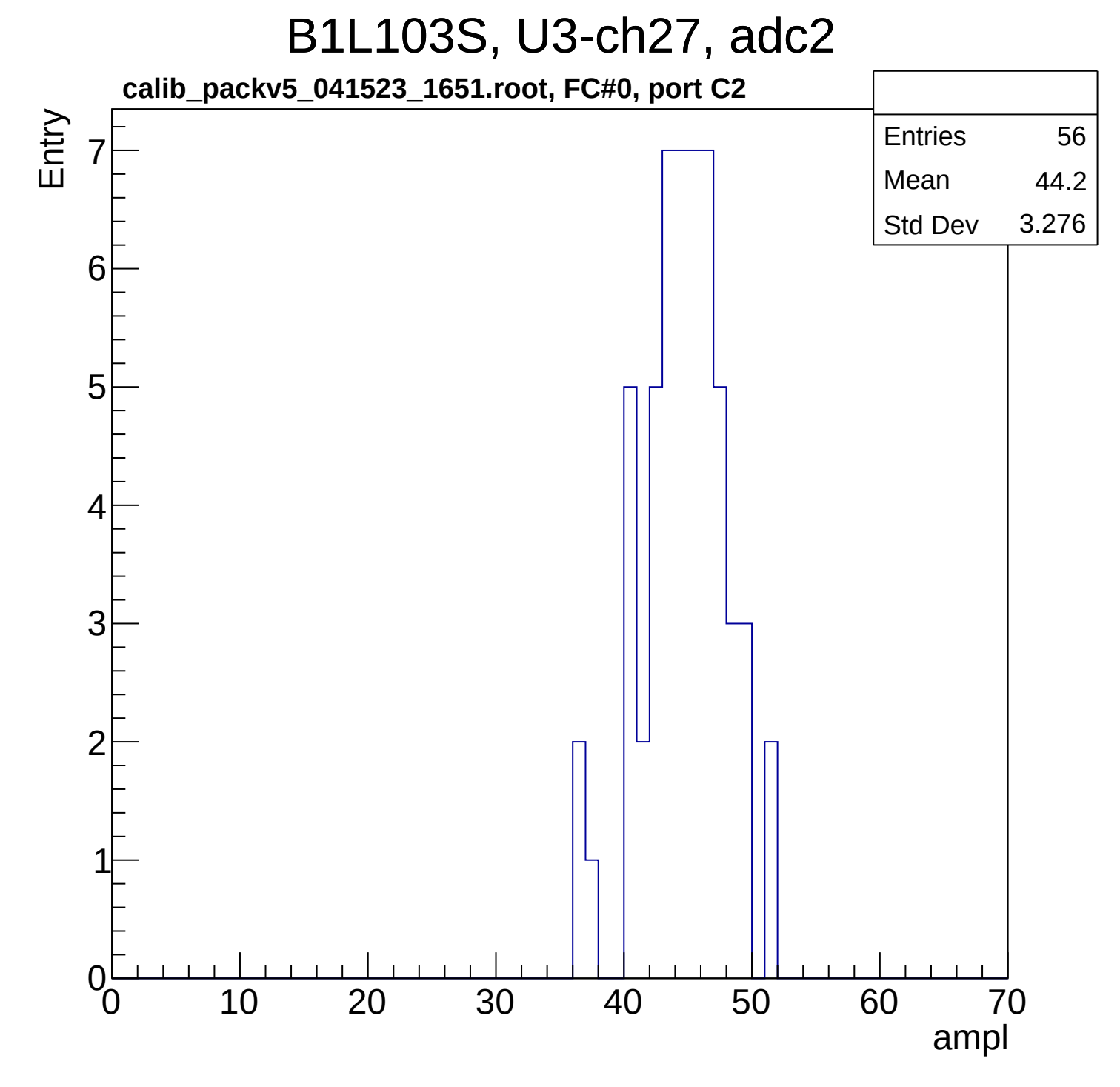
B1L103S, U3-ch27, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 44.2
Std Dev 3.276
Entry
ampl
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60
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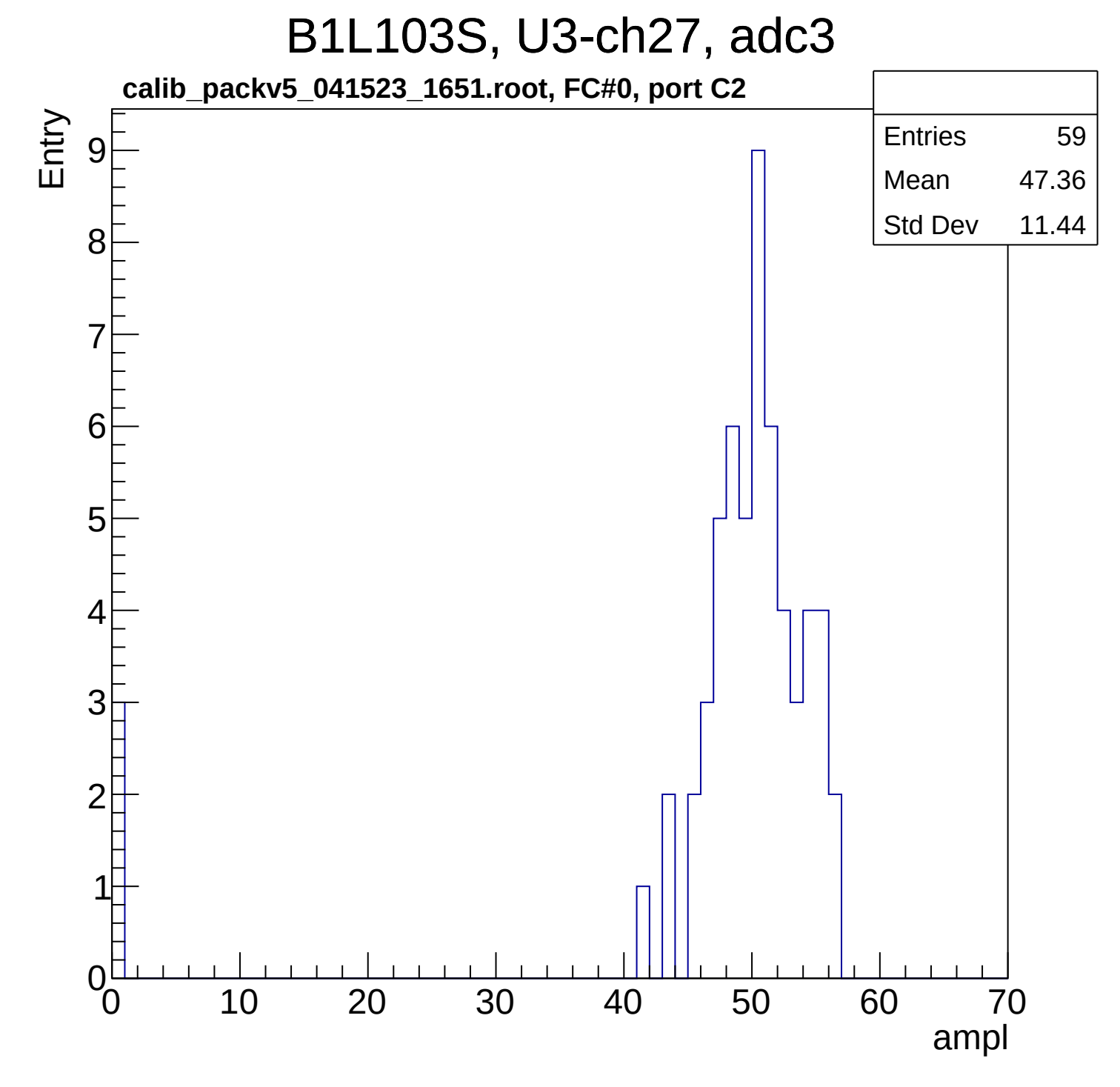
B1L103S, U3-ch27, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 47.36
Std Dev 11.44
Entry
ampl
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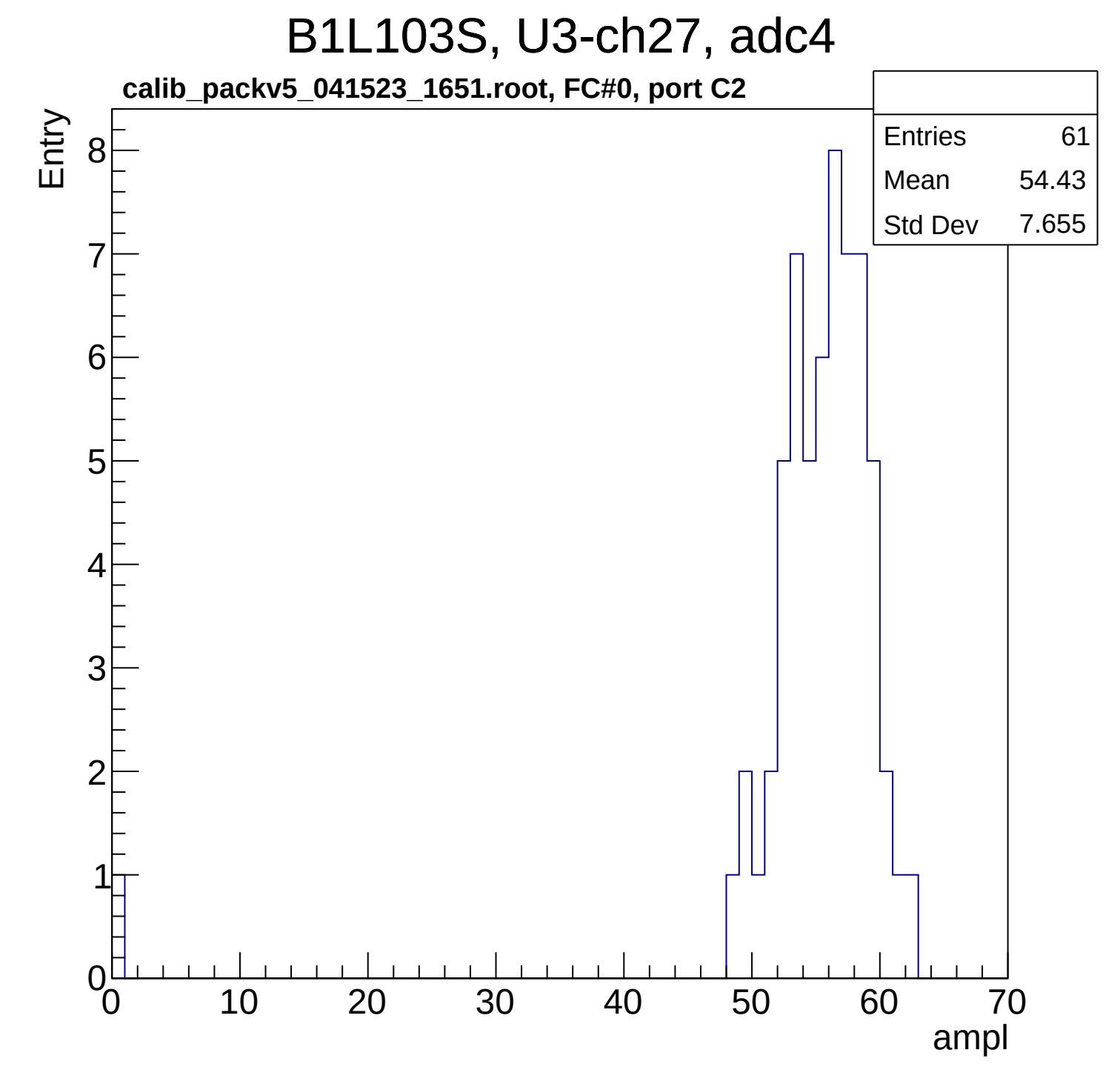
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L103S, U3-ch27, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 54.43
Std Dev 7.655
Entry
ampl
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2
3
4
5
6
7
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0
10
20
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40
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60
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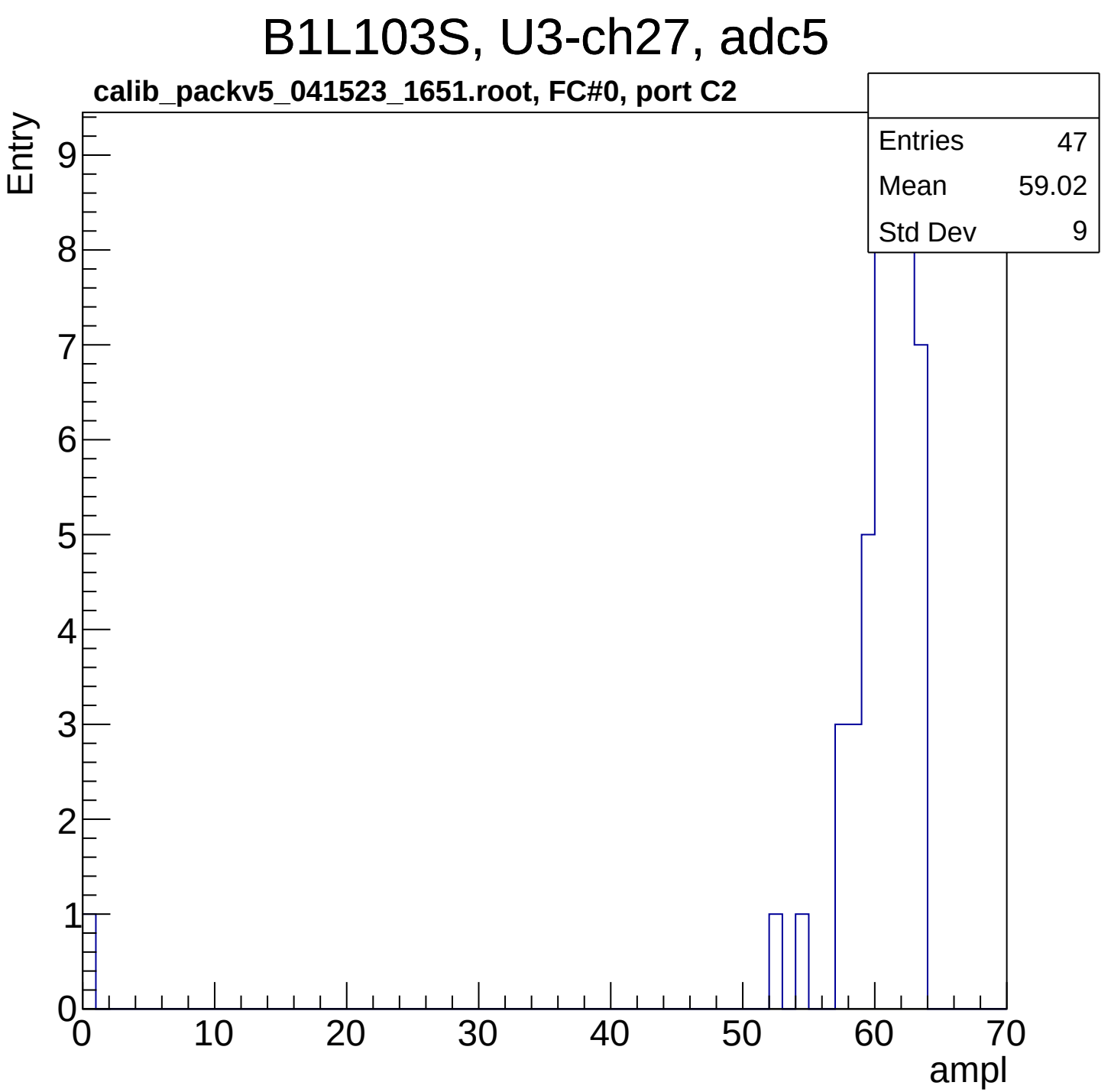
B1L103S, U3-ch27, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 59.02
Std Dev 9
Entry
ampl
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3
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5
6
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8
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0
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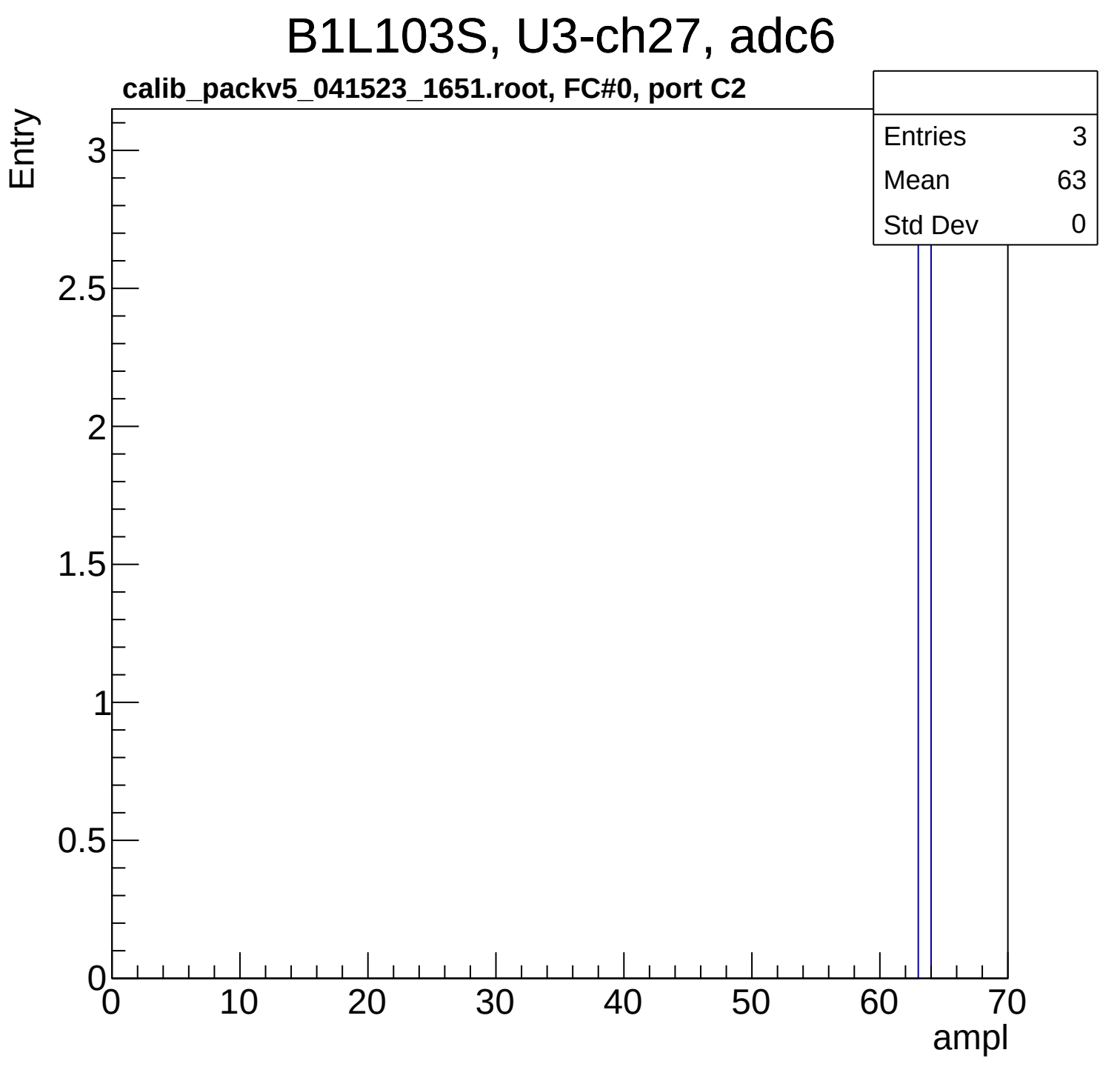
B1L103S, U3-ch27, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 63
Std Dev 0
Entry
ampl
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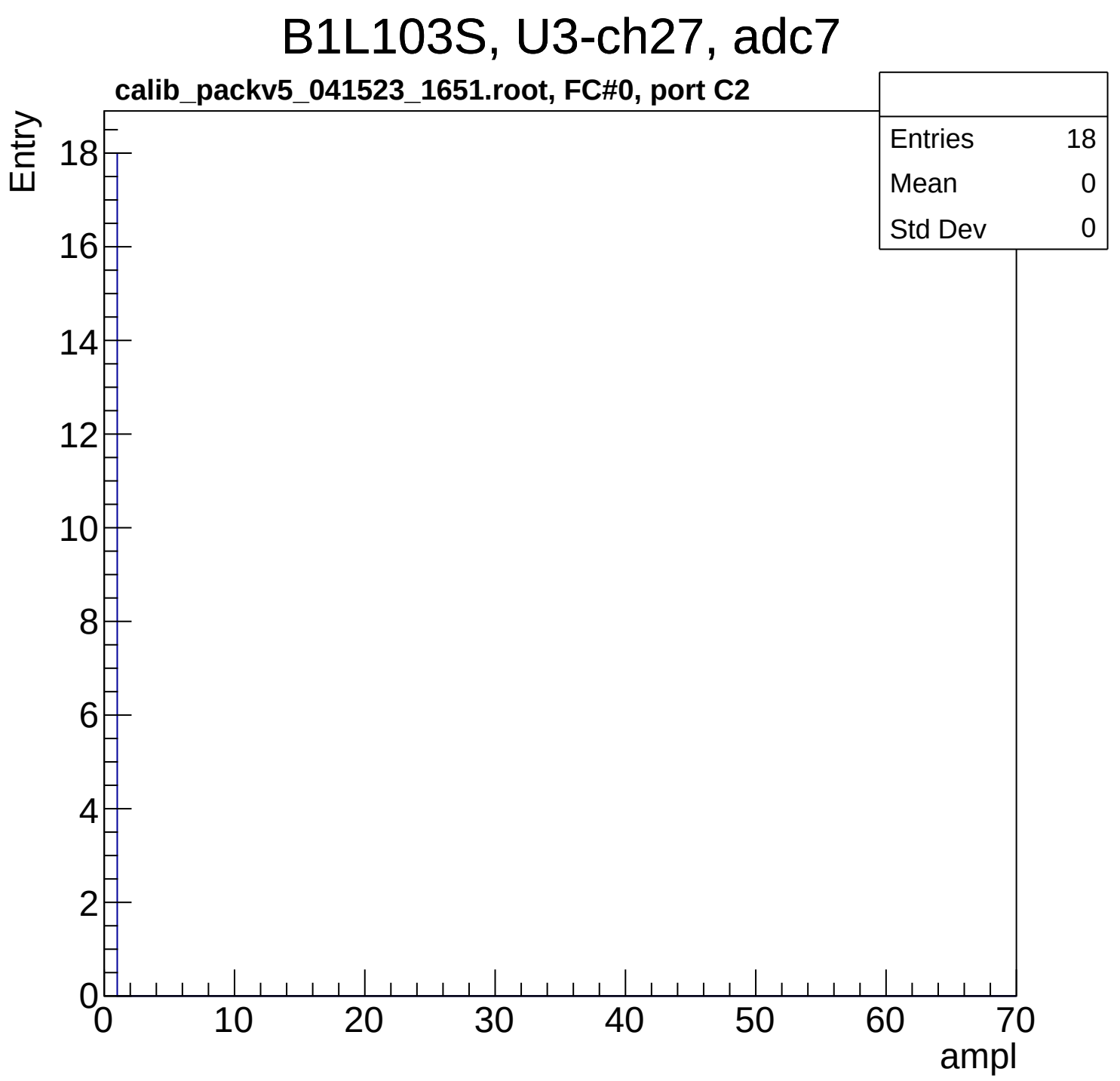
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U3-ch27, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
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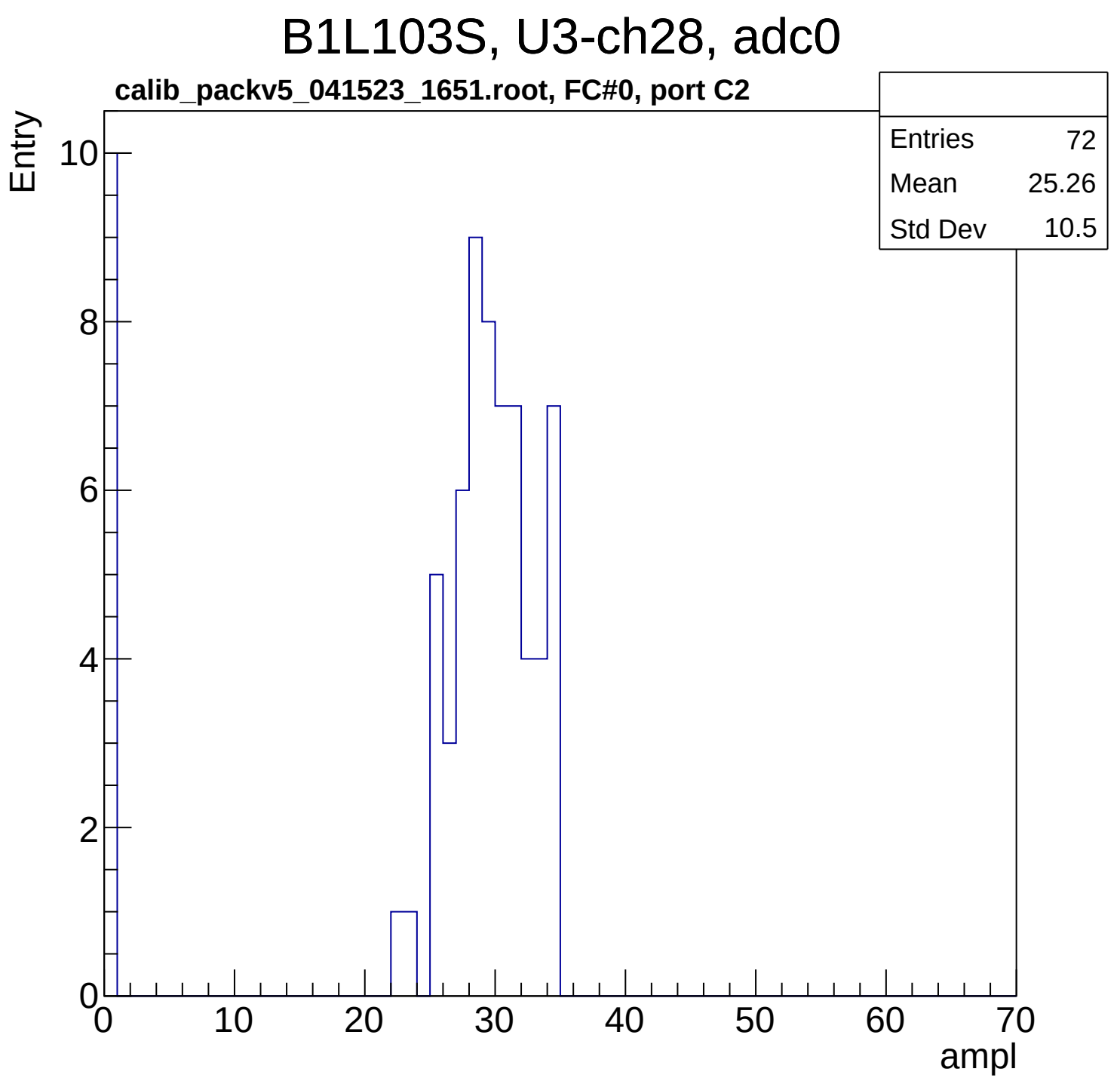
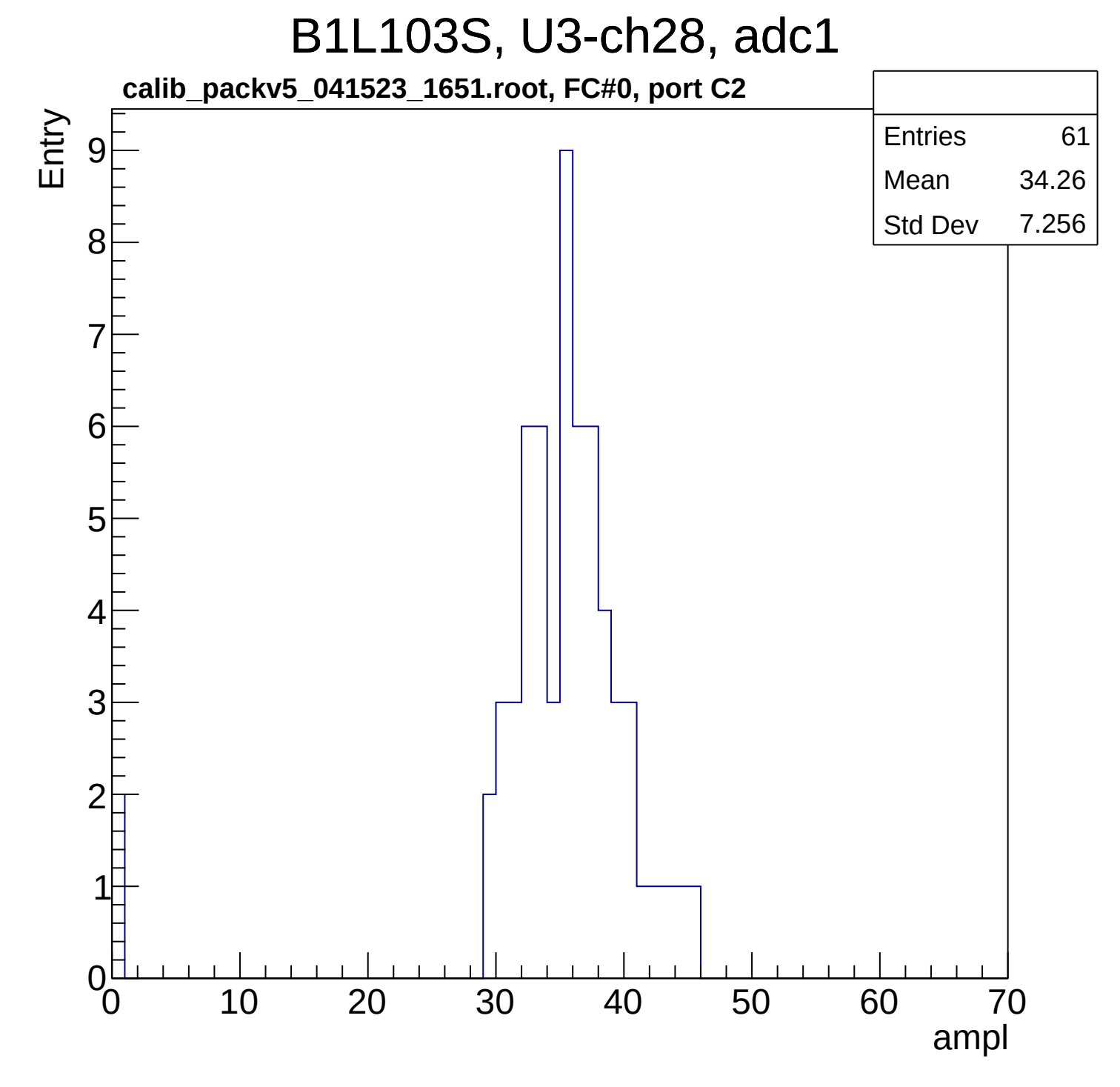
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch28, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 25.26
Std Dev 10.5
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch28, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 34.26
Std Dev 7.256
Entry
ampl
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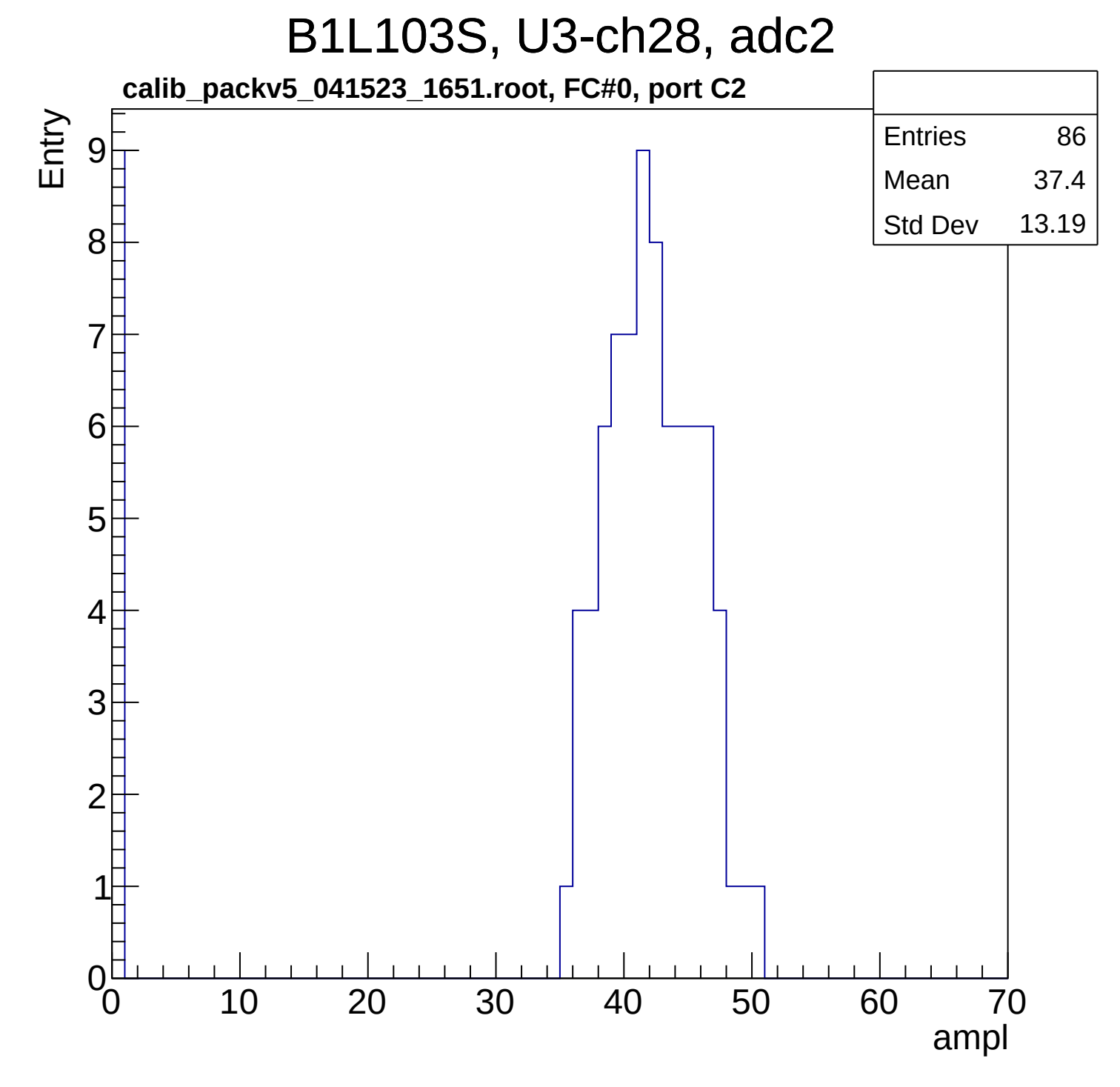
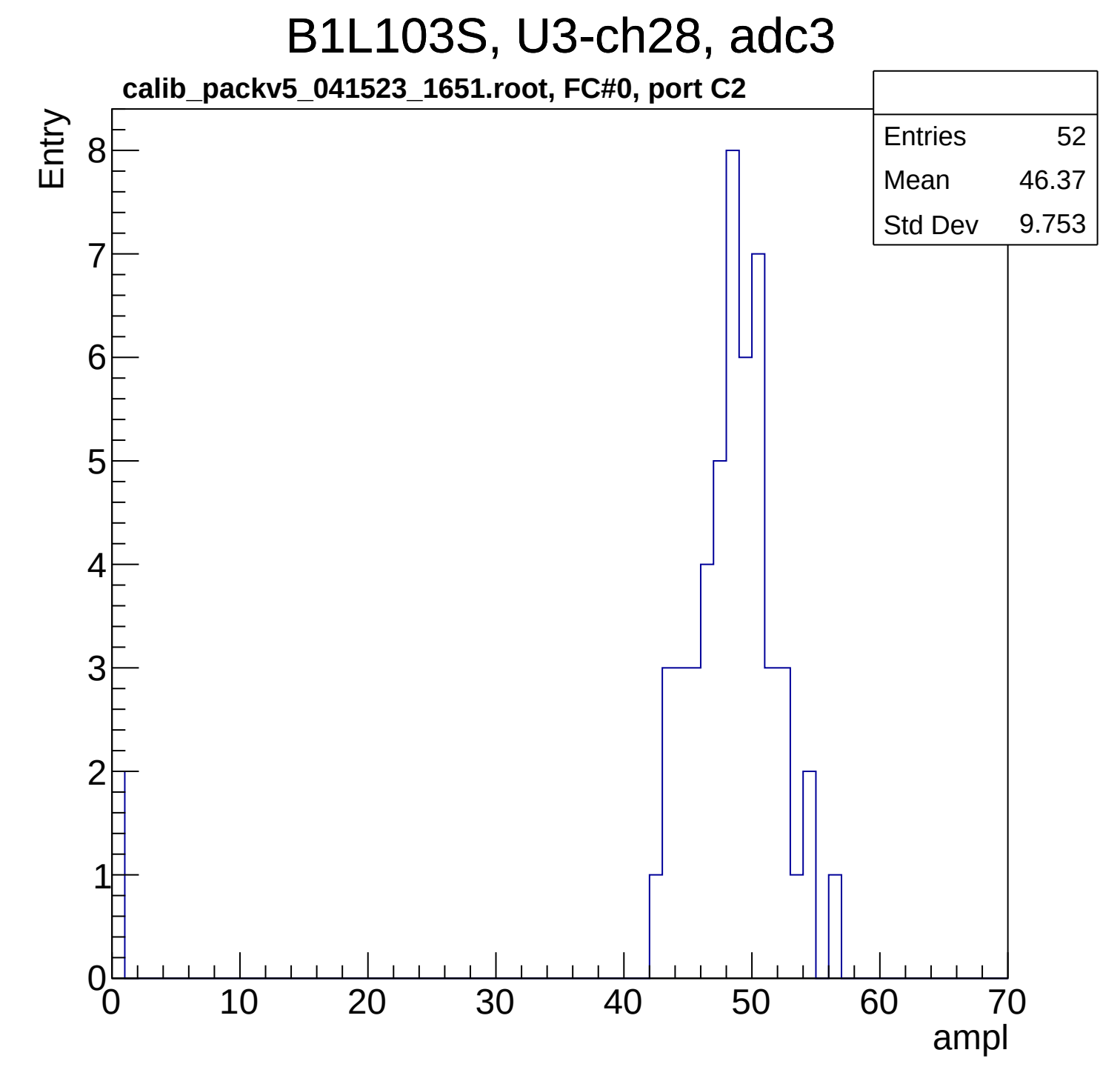
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch28, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 37.4
Std Dev 13.19
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch28, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 46.37
Std Dev 9.753
Entry
ampl
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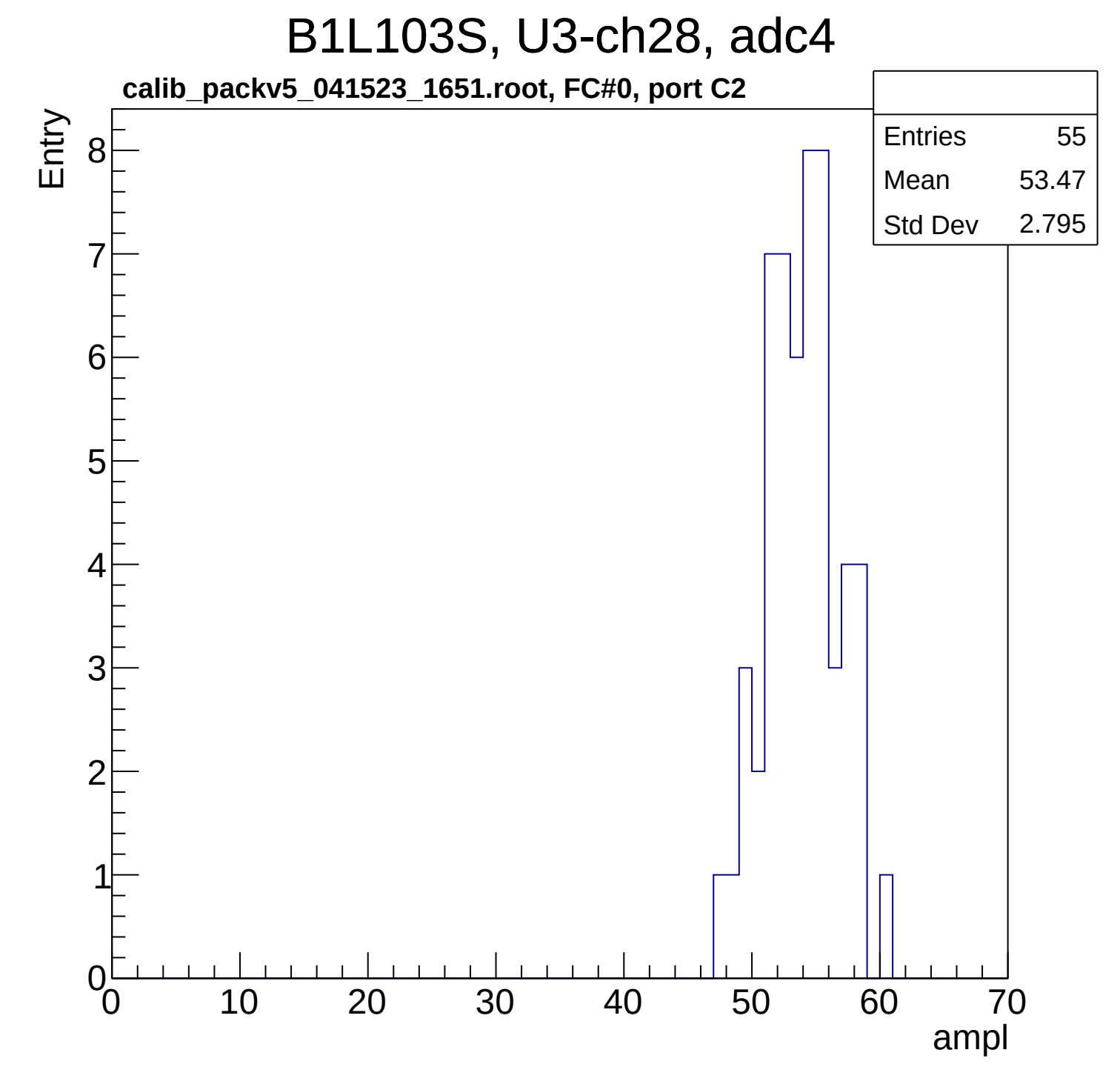
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch28, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 53.47
Std Dev 2.795
Entry
ampl
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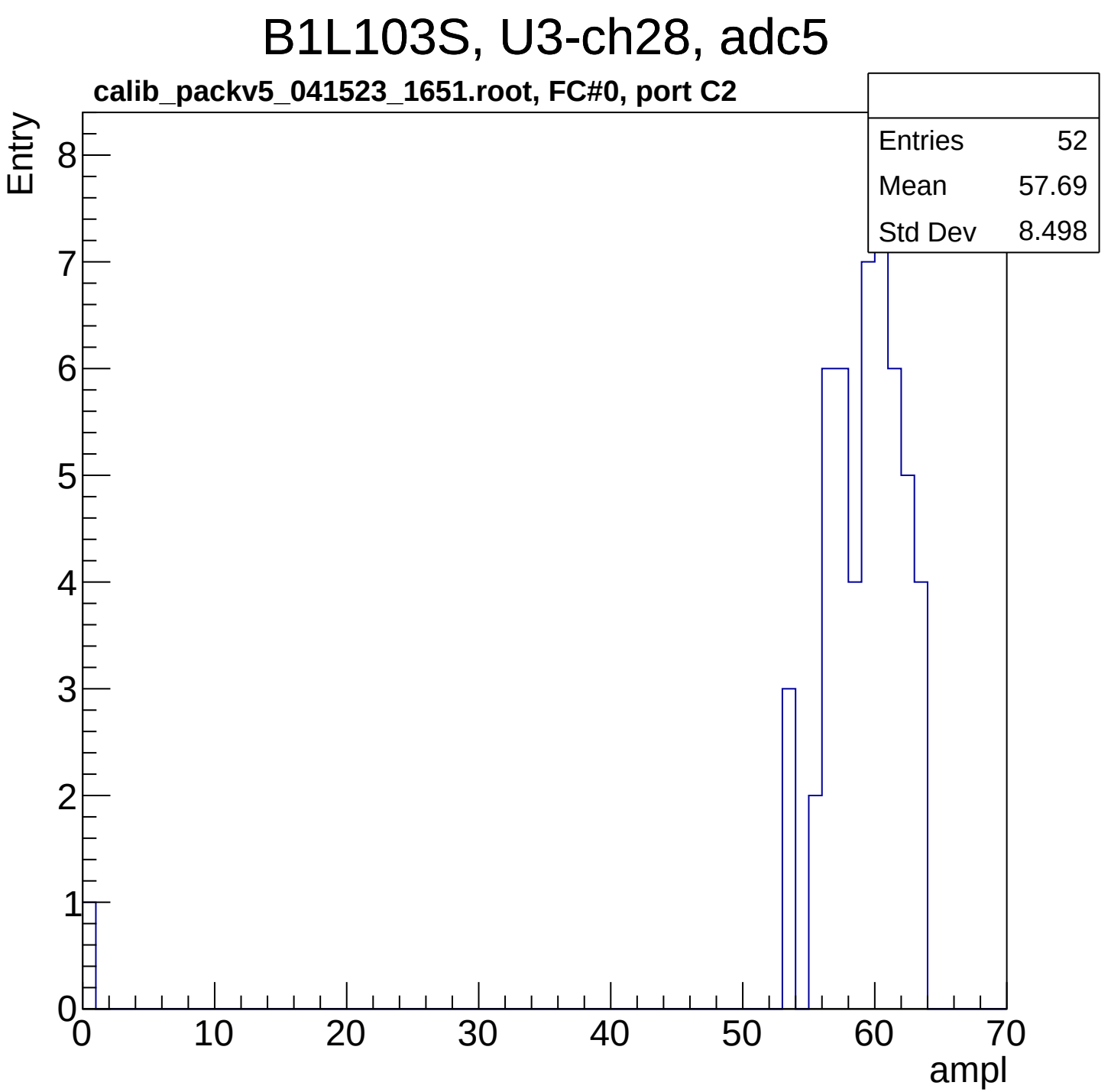
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch28, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 57.69
Std Dev 8.498
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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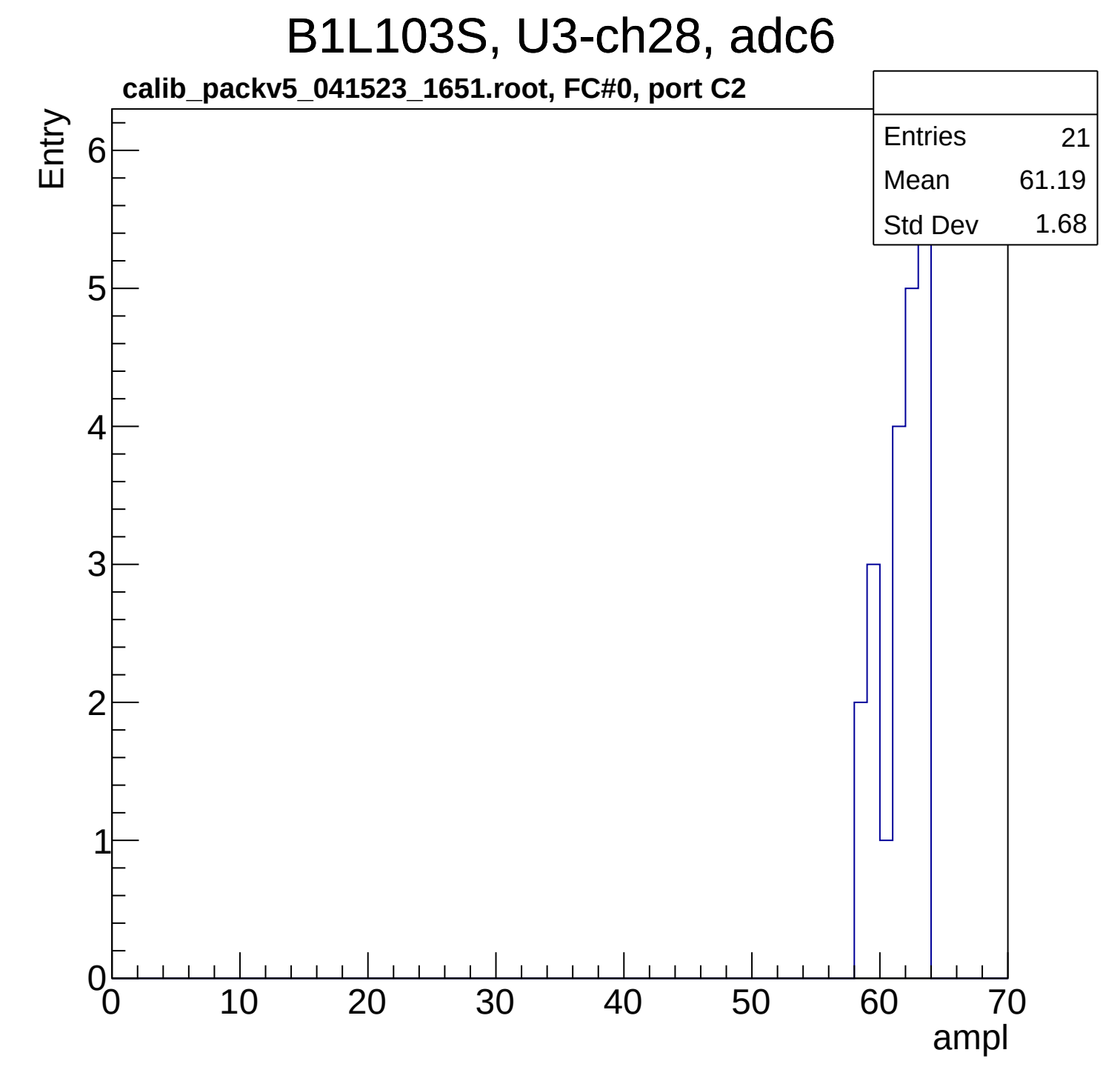
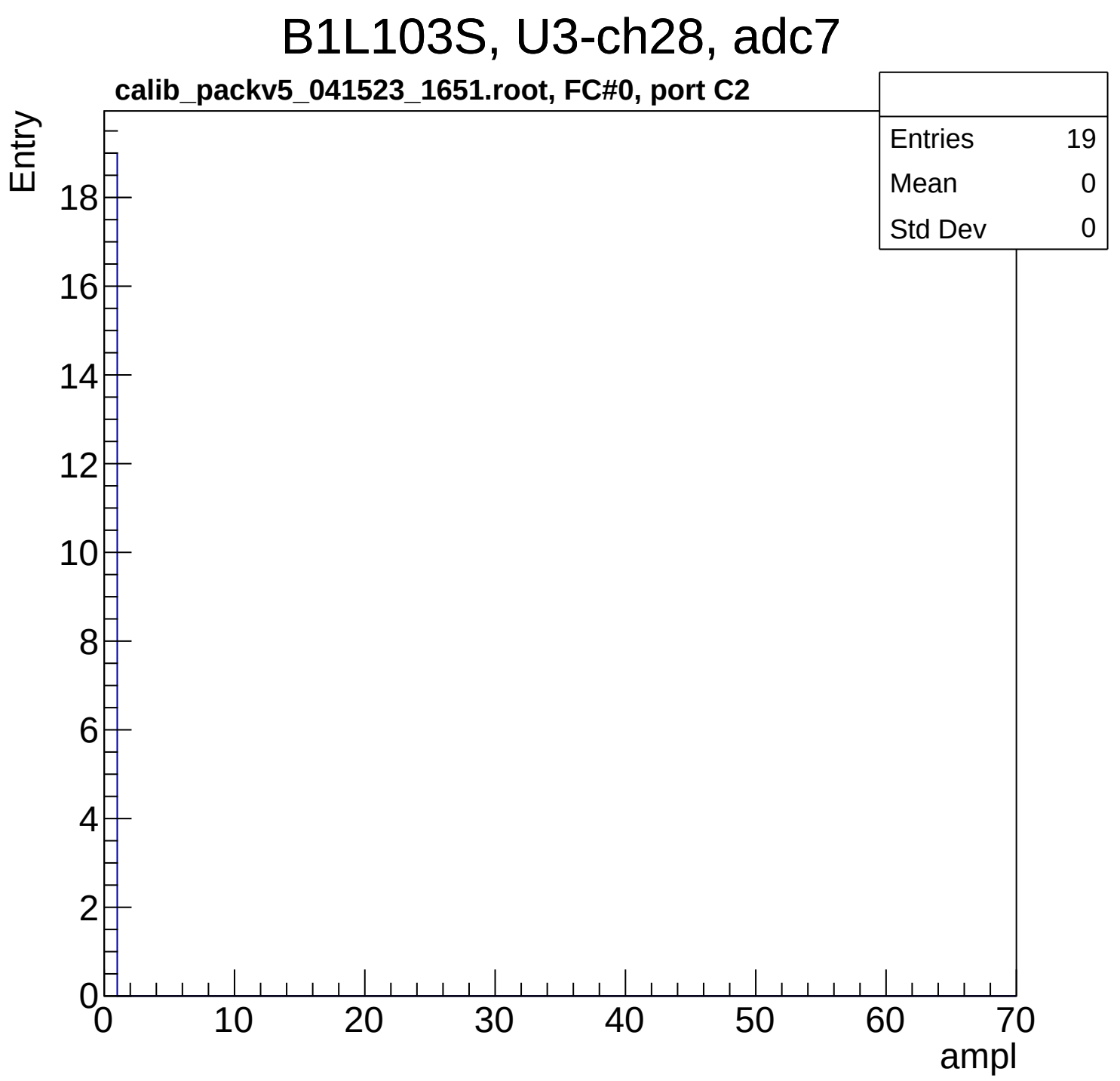
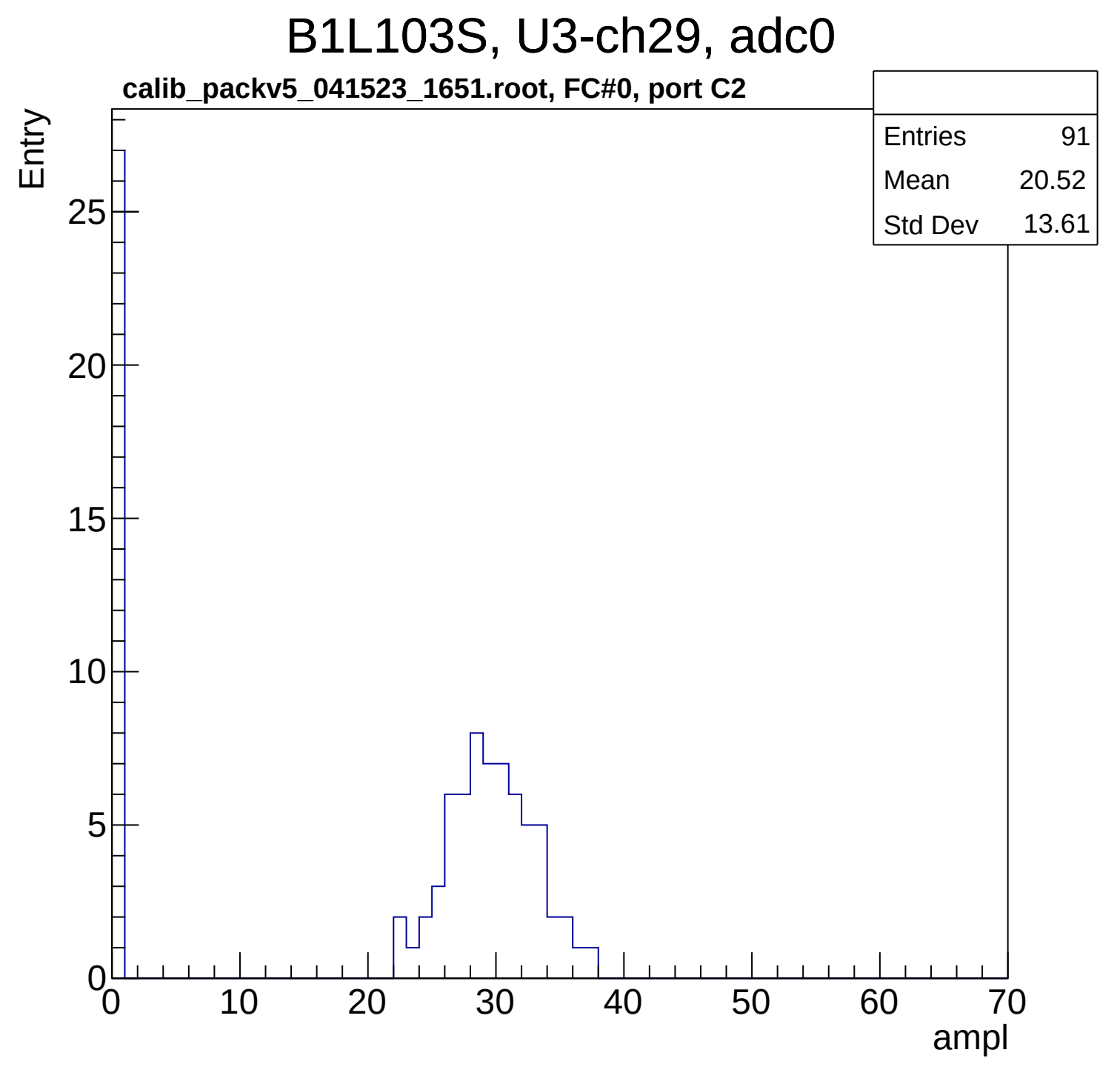
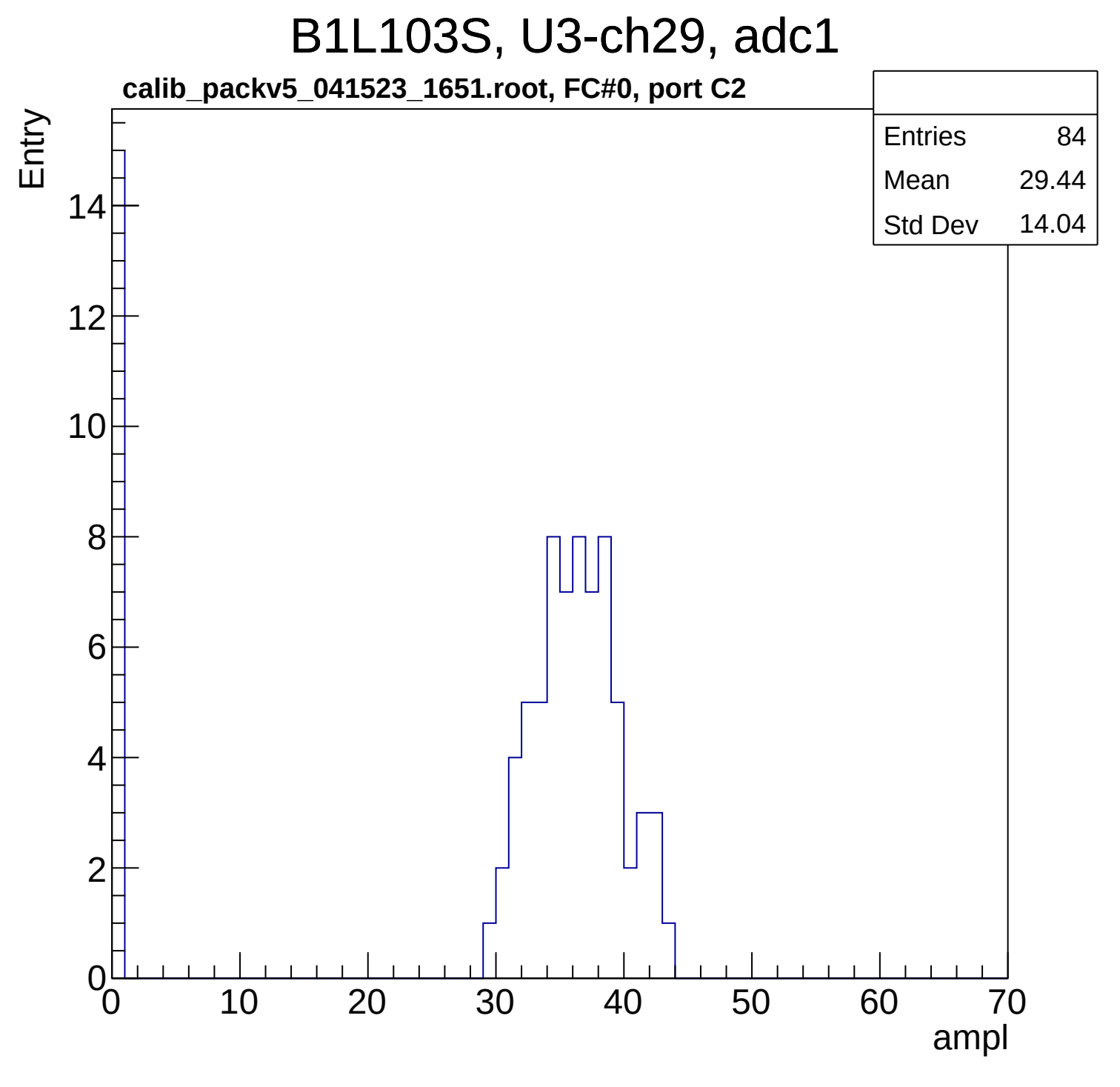

B1L103S, U3-ch28, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 61.19
Std Dev 1.68
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U3-ch28, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch29, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 20.52
Std Dev 13.61
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch29, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 29.44
Std Dev 14.04
Entry
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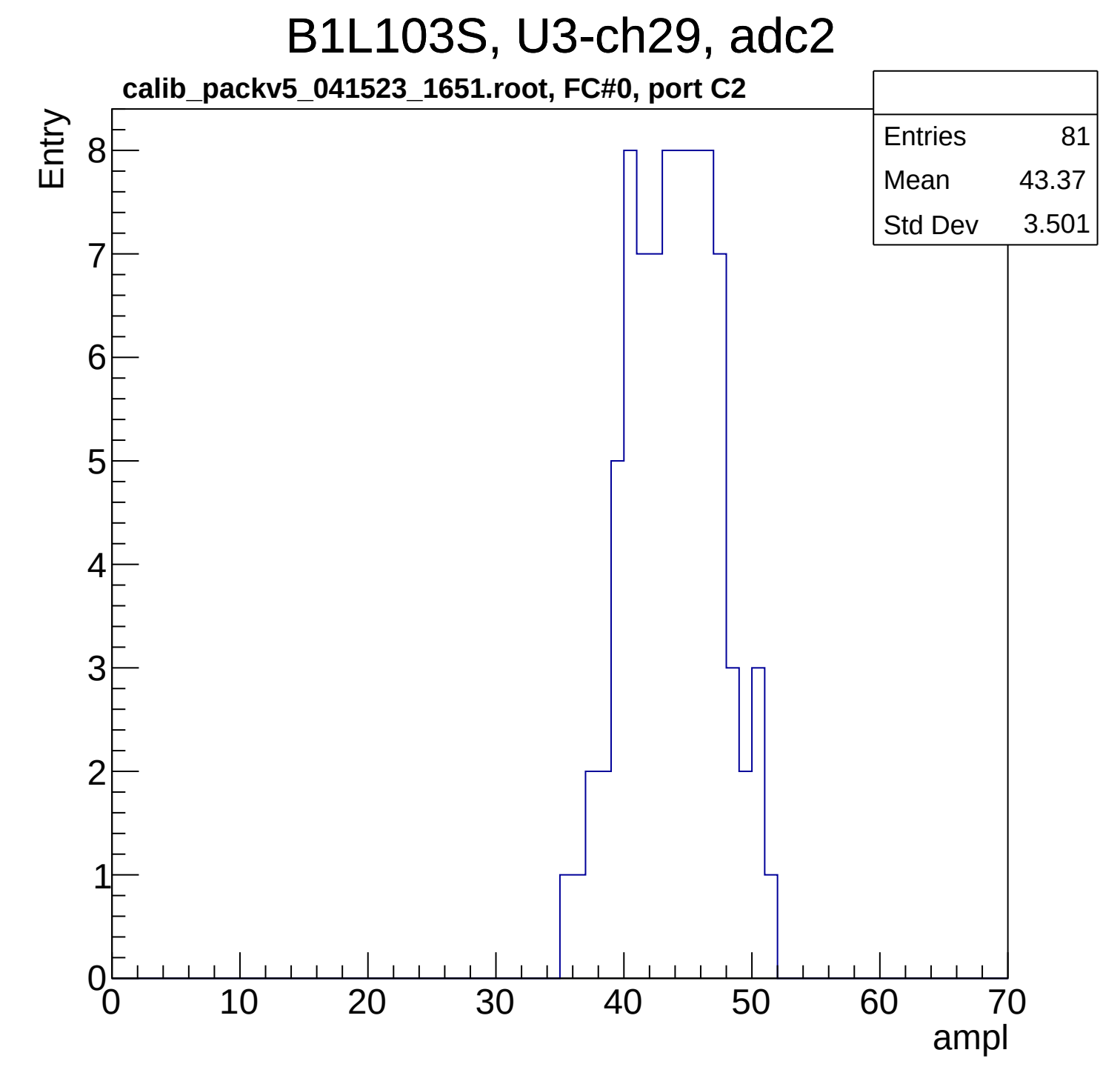
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch29, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 43.37
Std Dev 3.501
Entry
ampl
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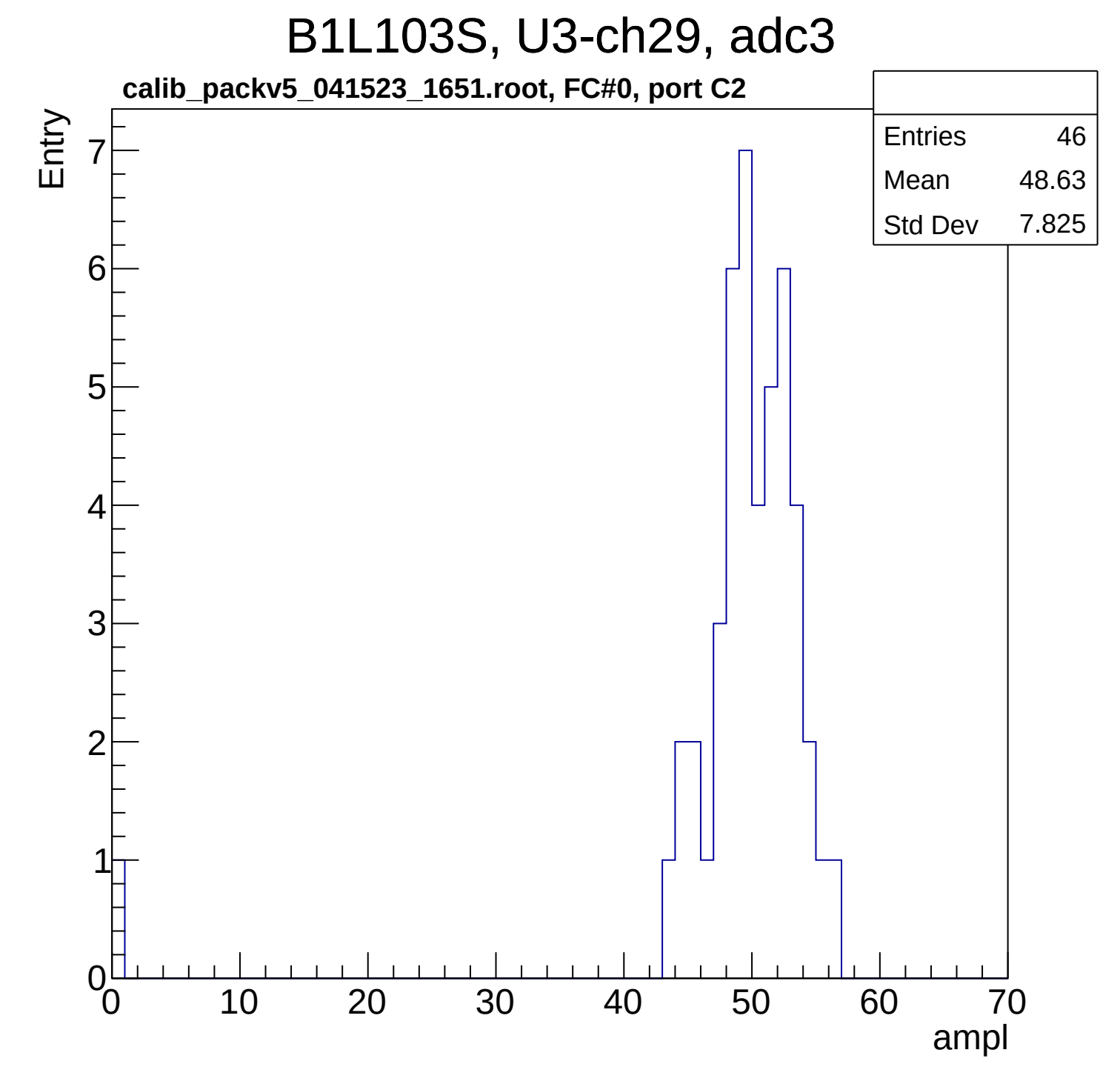
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch29, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 48.63
Std Dev 7.825
Entry
ampl
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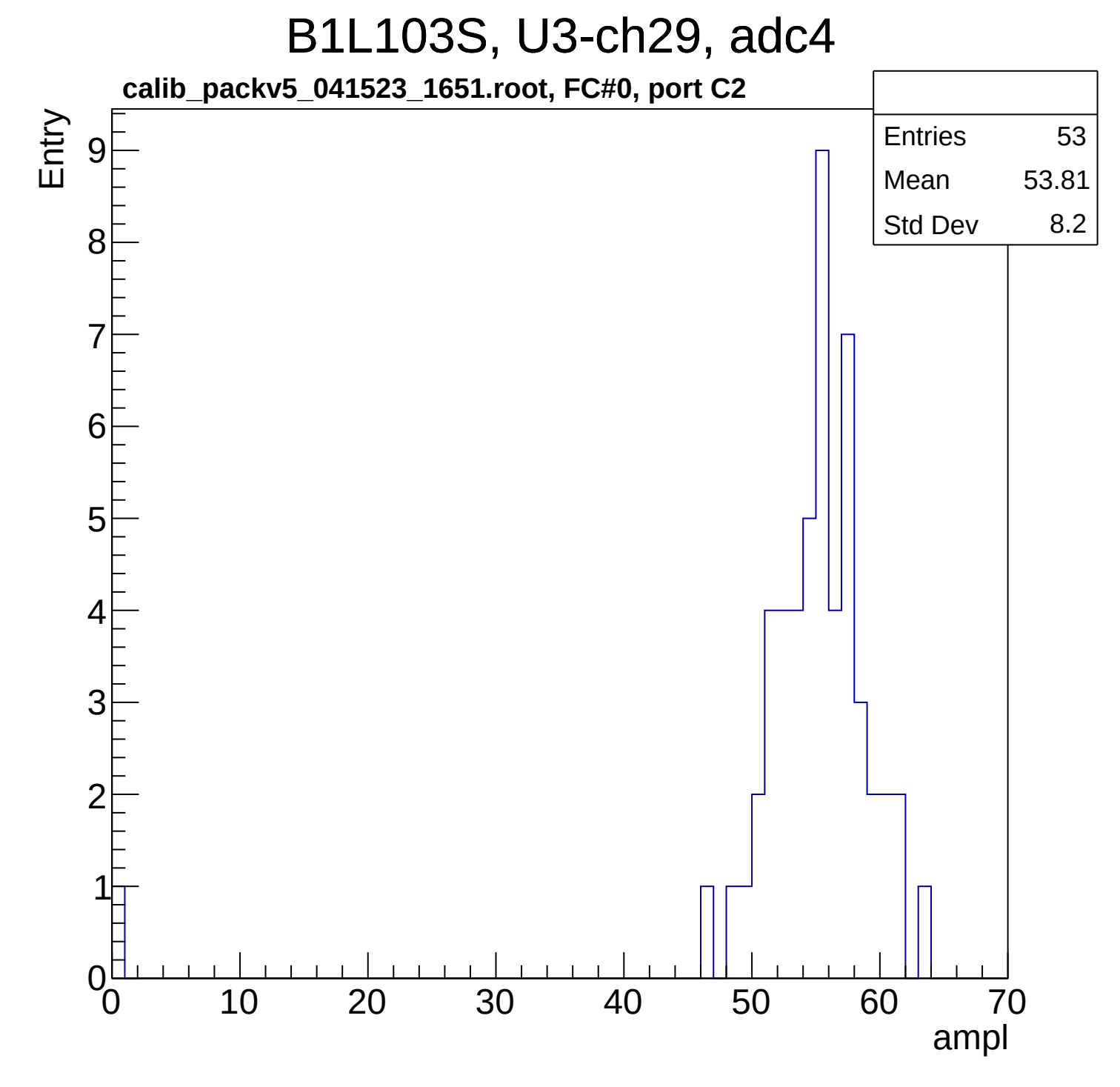
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch29, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 53.81
Std Dev 8.2
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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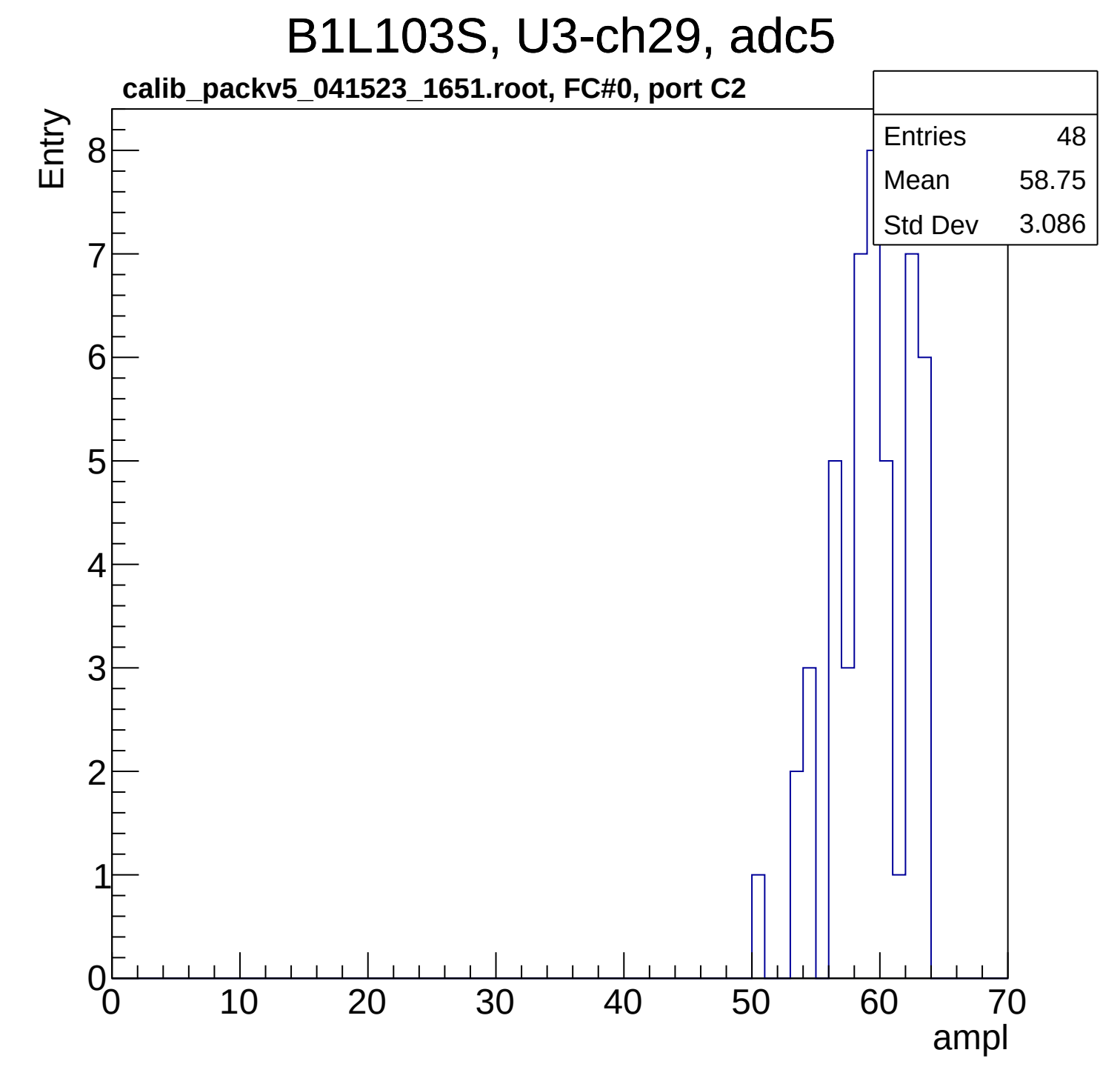
B1L103S, U3-ch29, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 58.75
Std Dev 3.086
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
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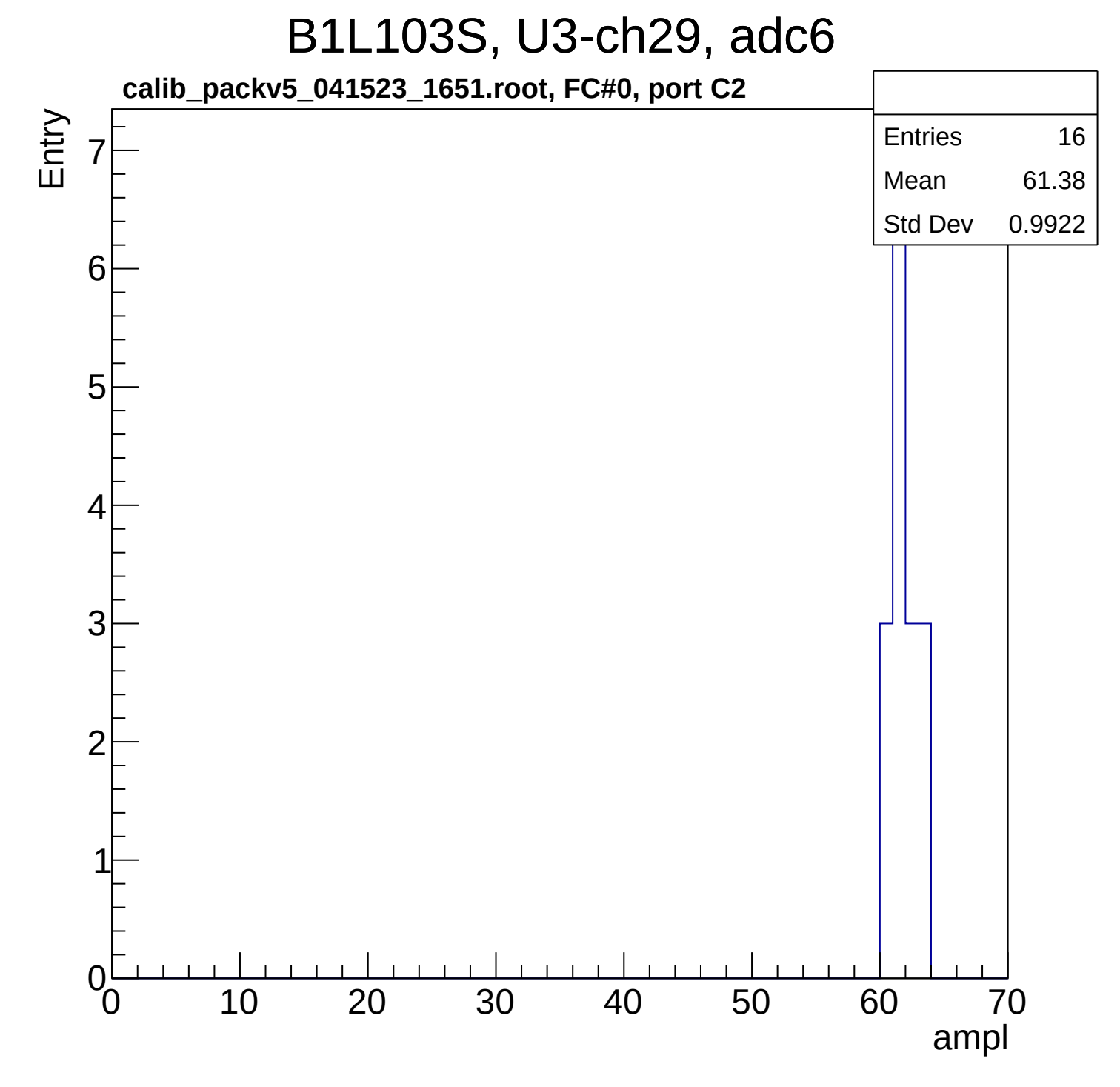
B1L103S, U3-ch29, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 61.38
Std Dev 0.9922
Entry
ampl
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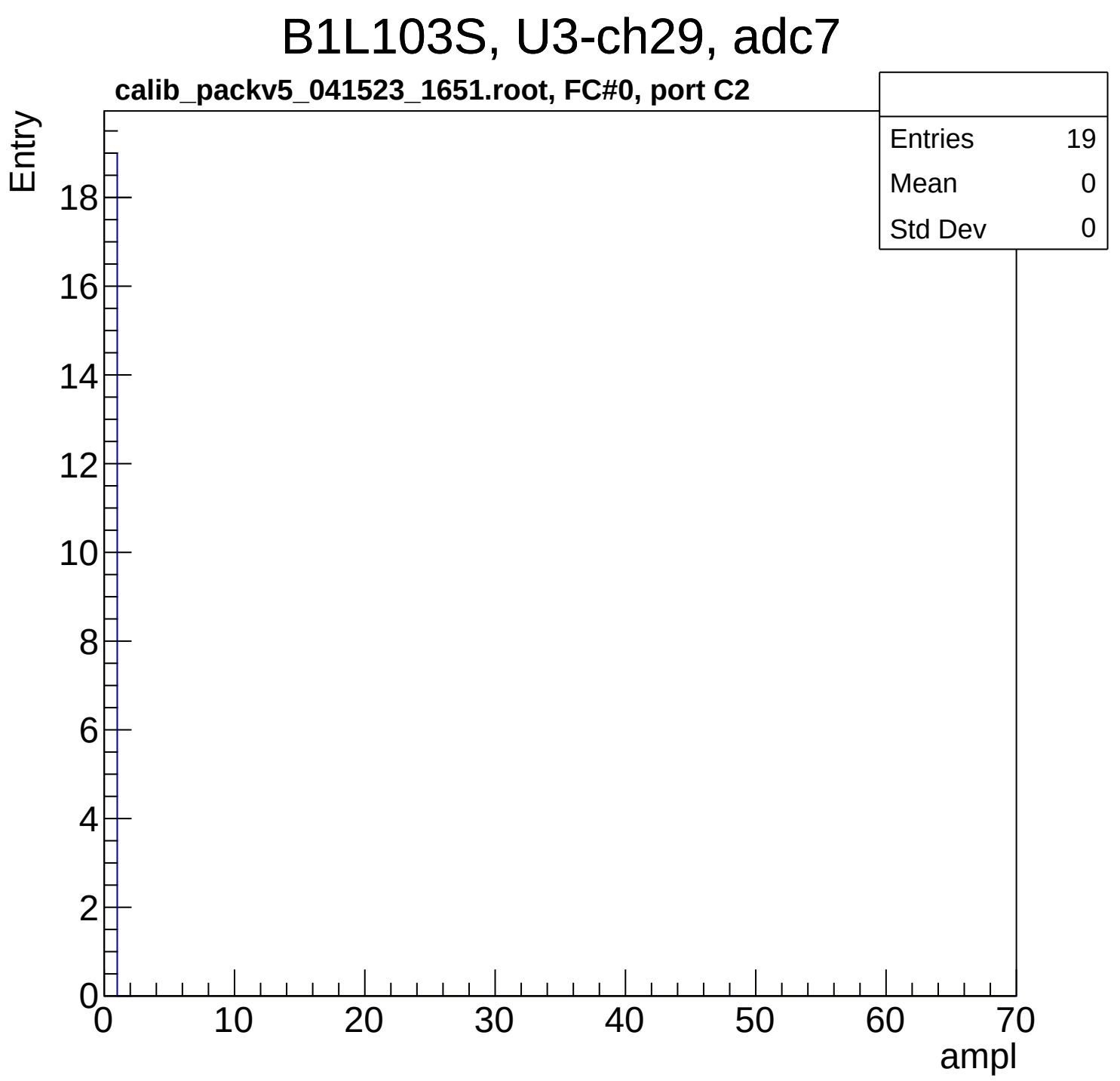
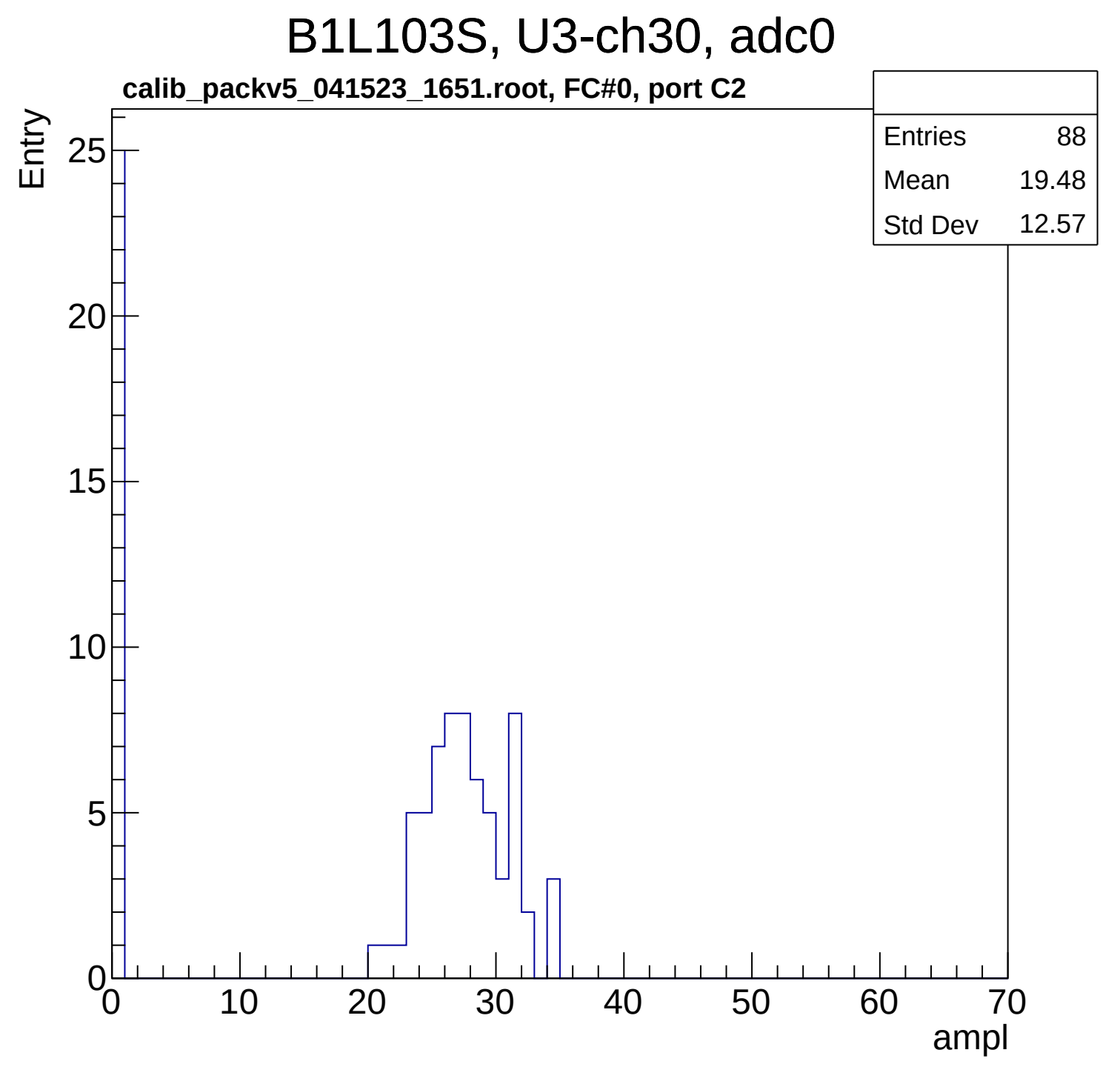
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch29, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch30, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 19.48
Std Dev 12.57
Entry
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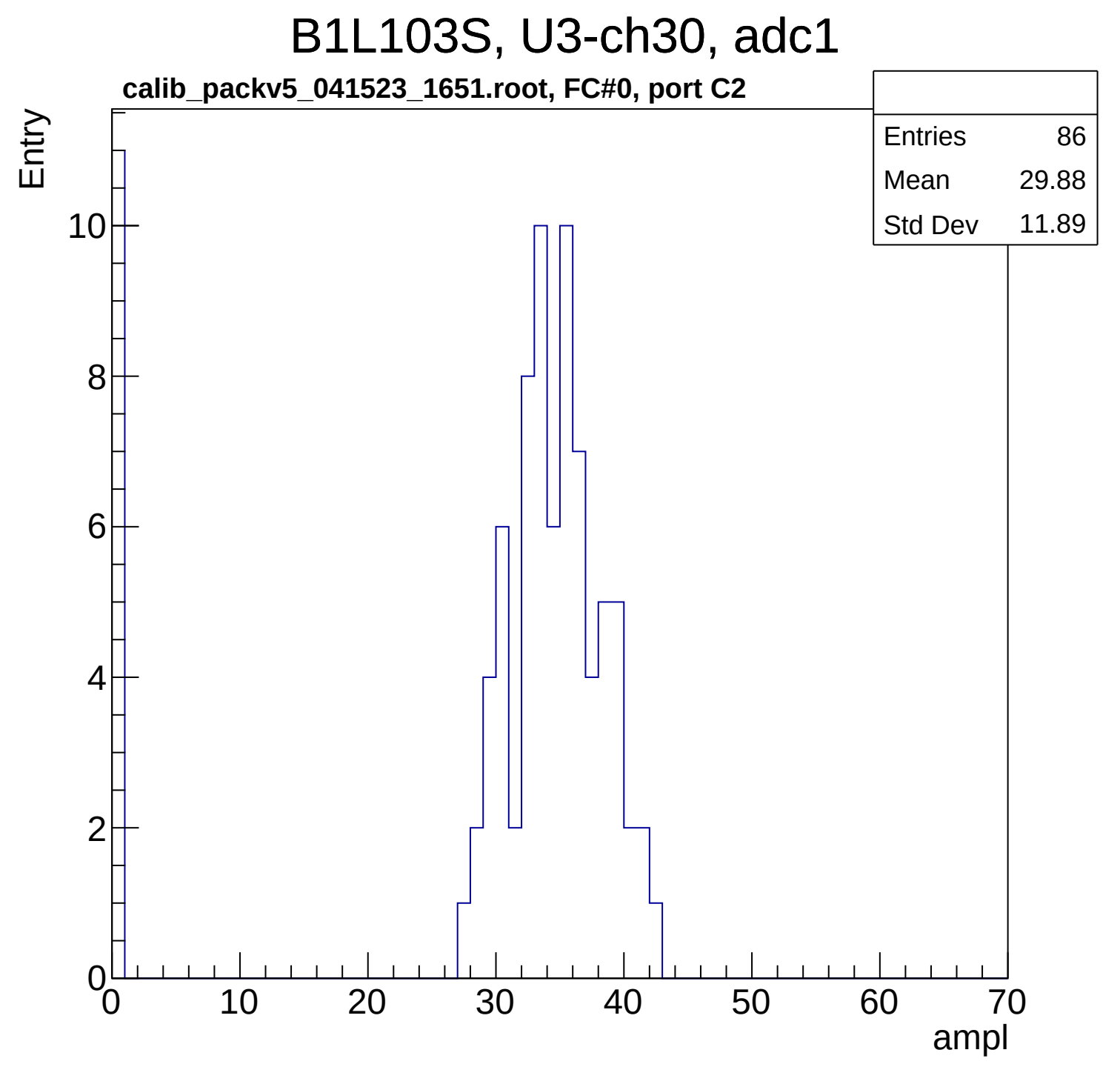
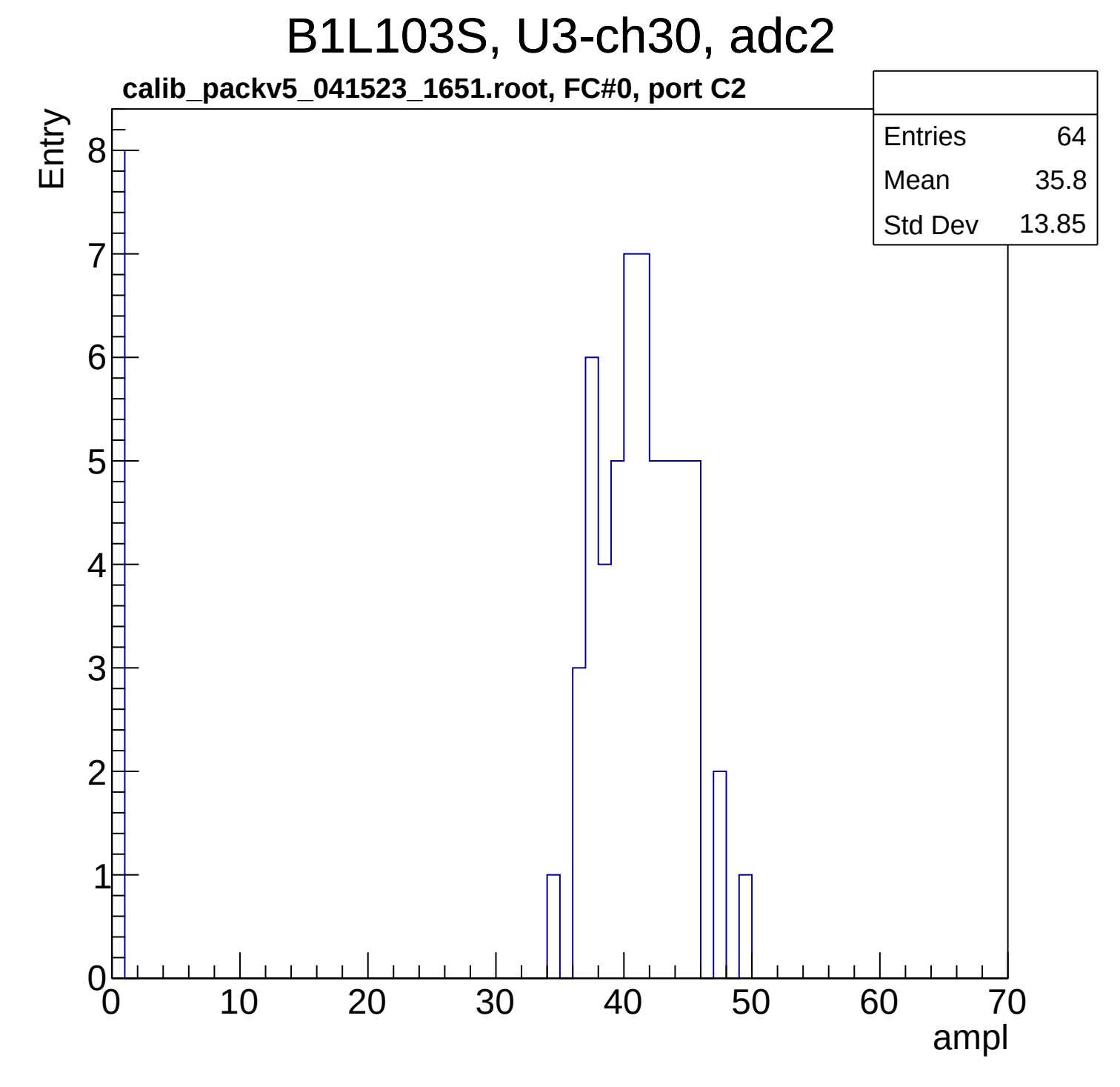
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch30, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 29.88
Std Dev 11.89
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch30, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 35.8
Std Dev 13.85
Entry
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2
3
4
5
6
7
8
0
10
20
30
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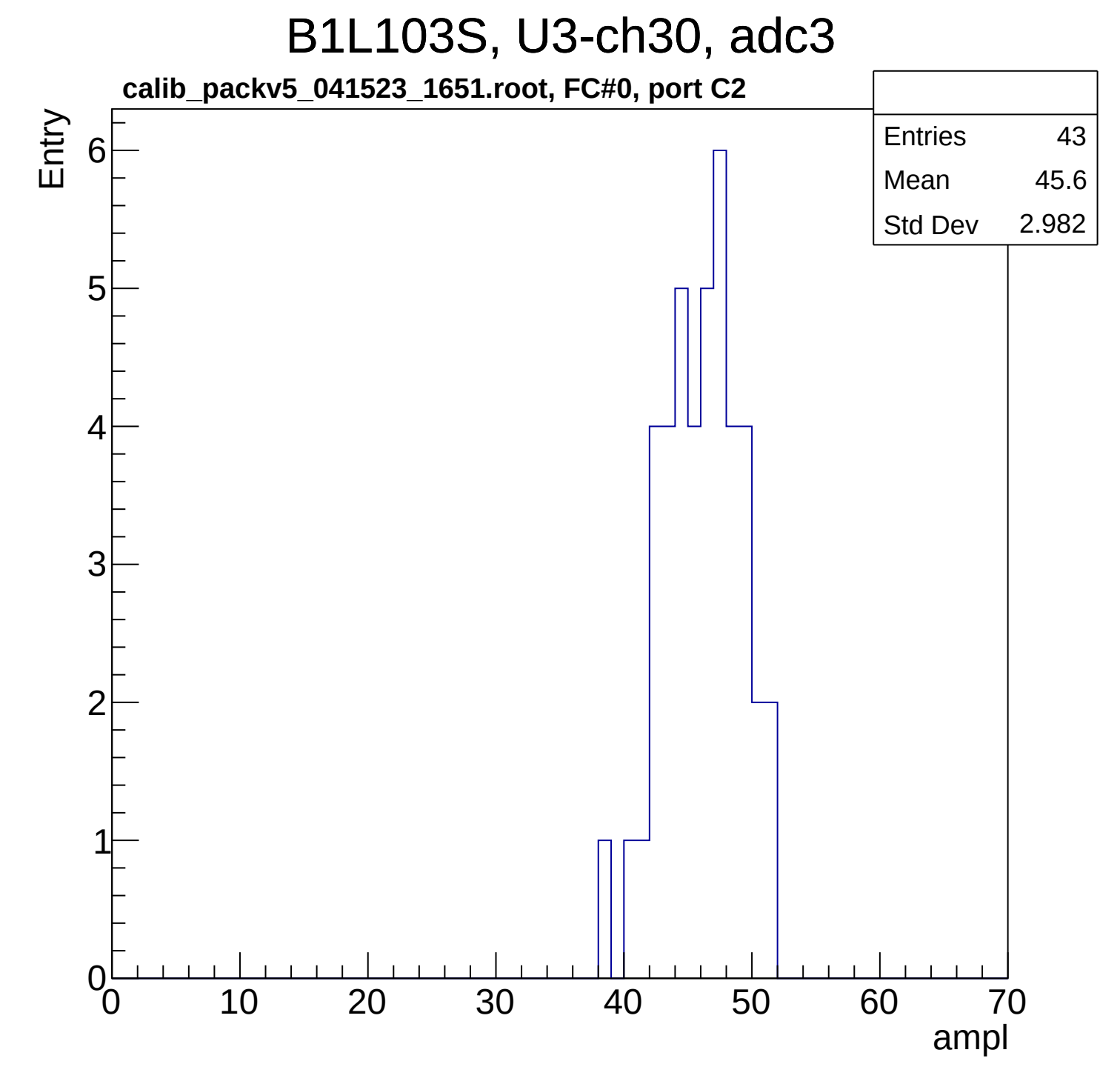
50
60
70
ampl


B1L103S, U3-ch30, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 45.6
Std Dev 2.982
Entry
ampl
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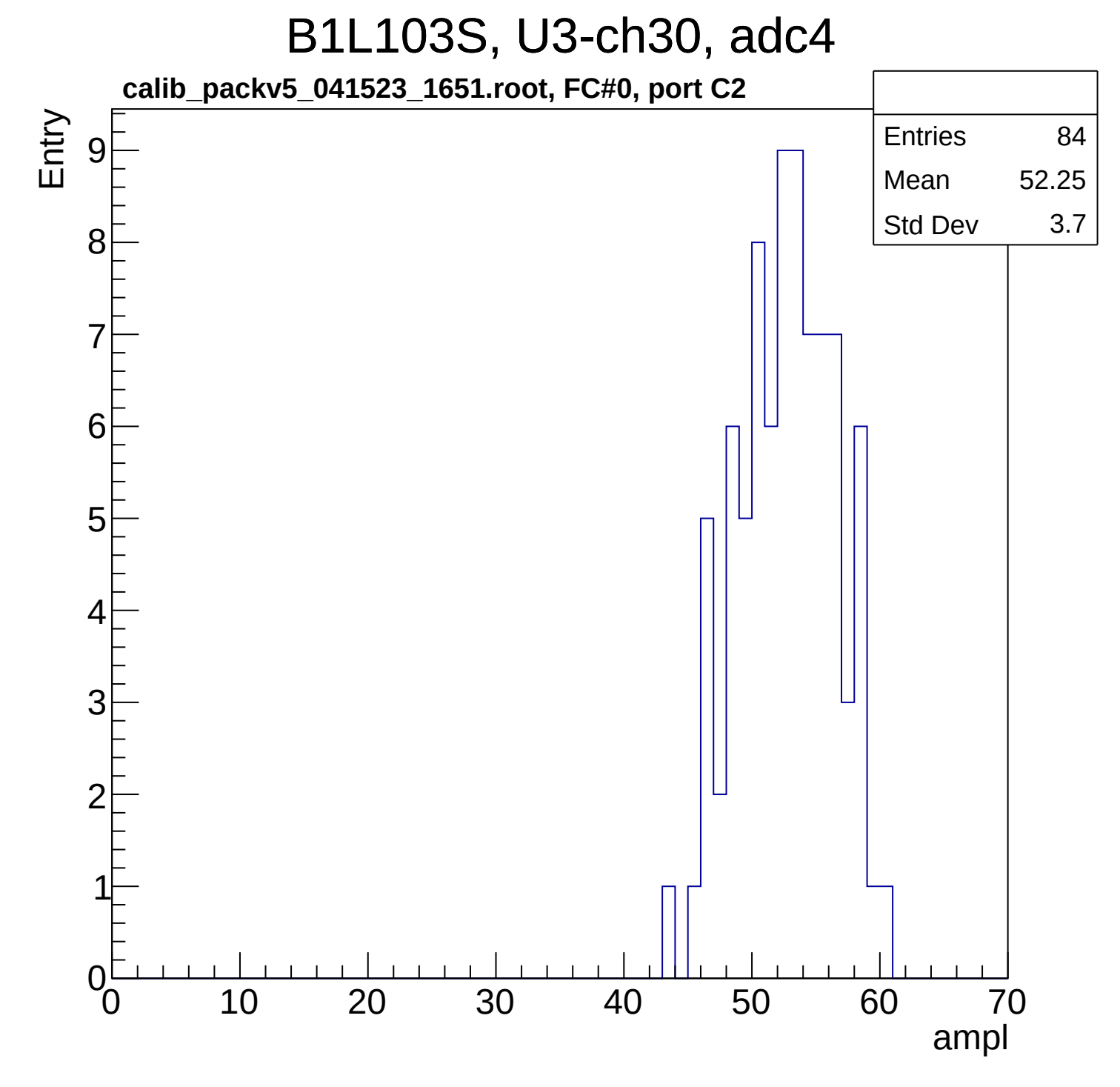
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U3-ch30, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 52.25
Std Dev 3.7
Entry
ampl
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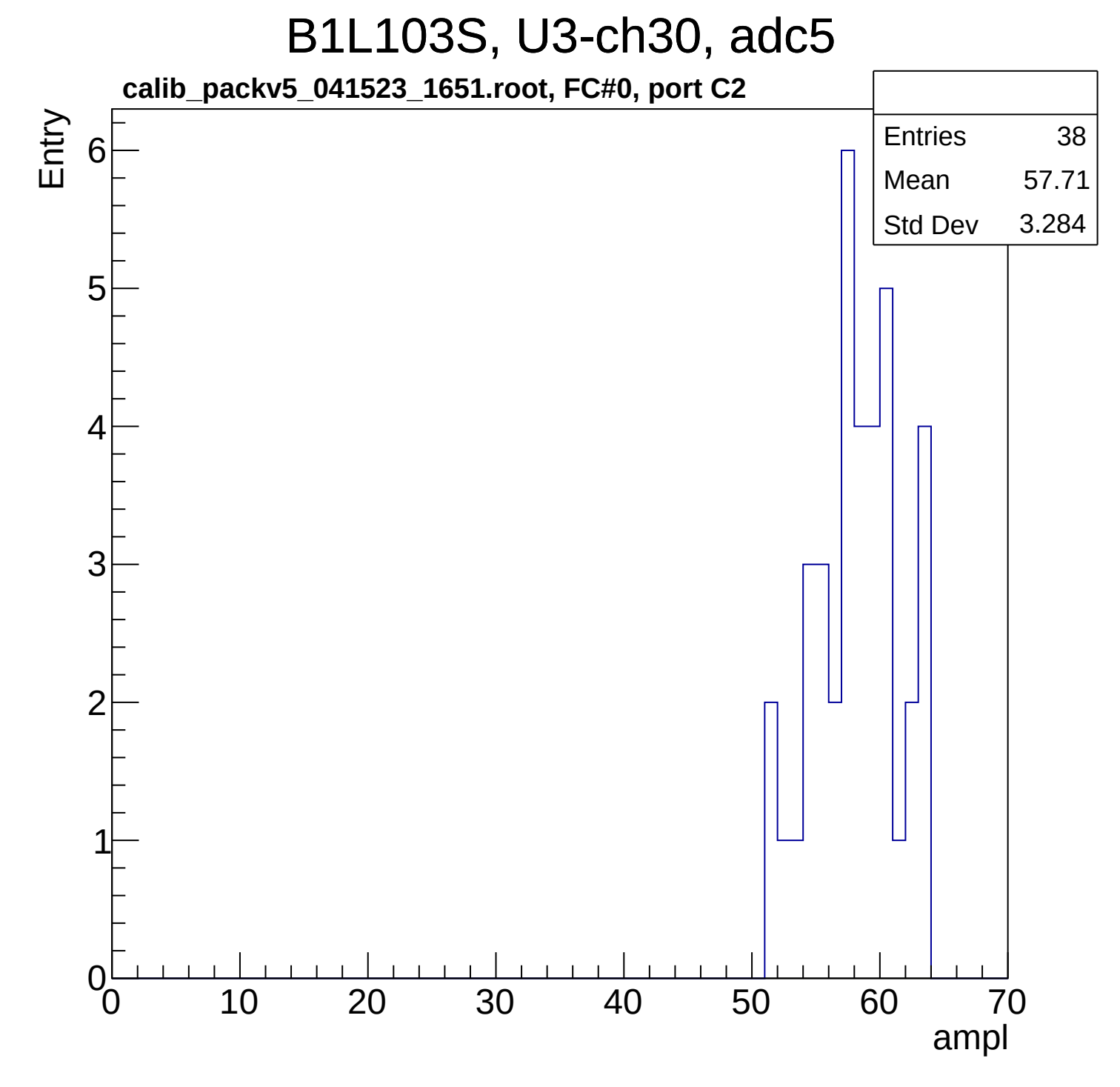
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch30, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 57.71
Std Dev 3.284
Entry
ampl
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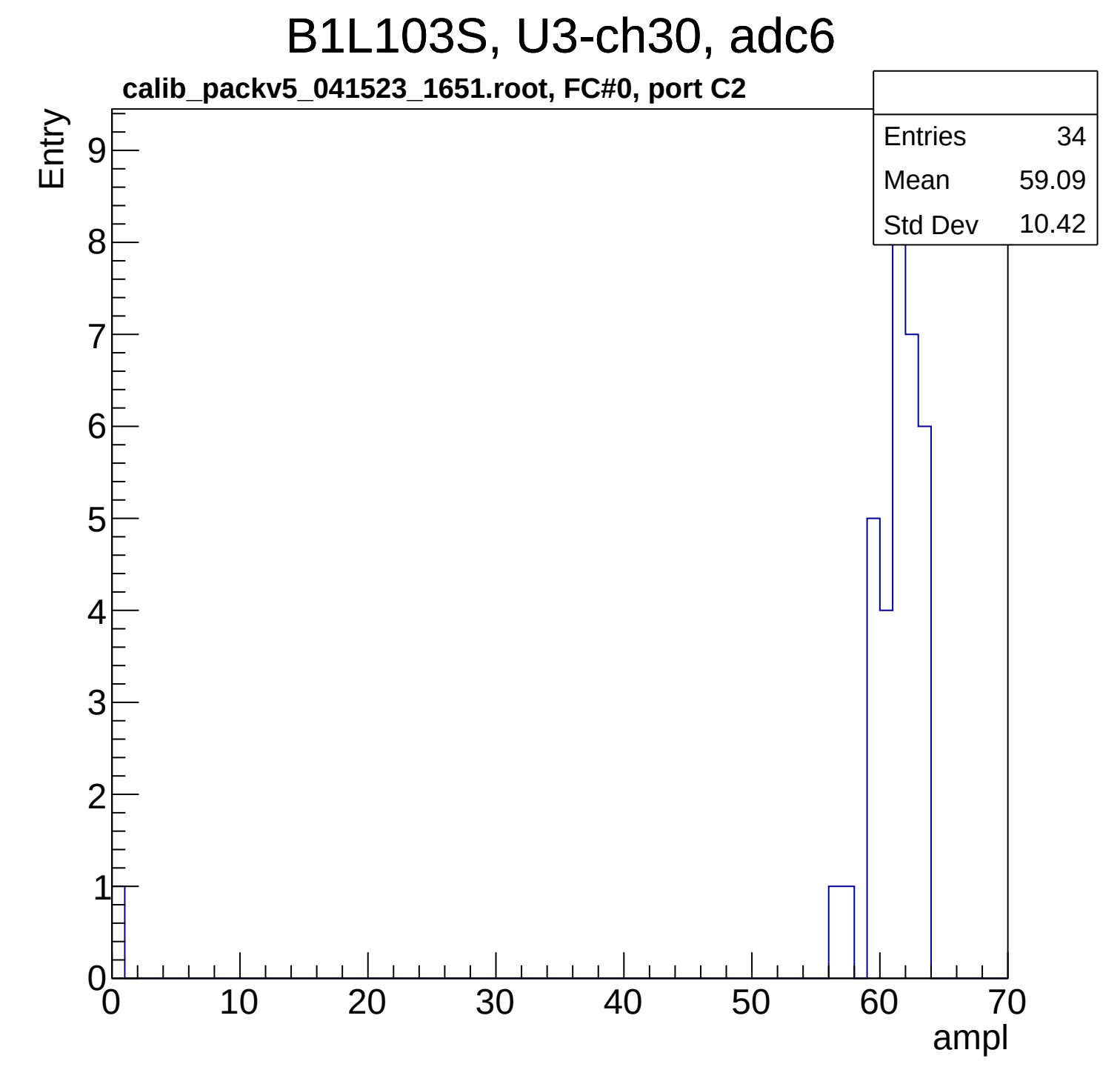
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U3-ch30, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 59.09
Std Dev 10.42
Entry
ampl
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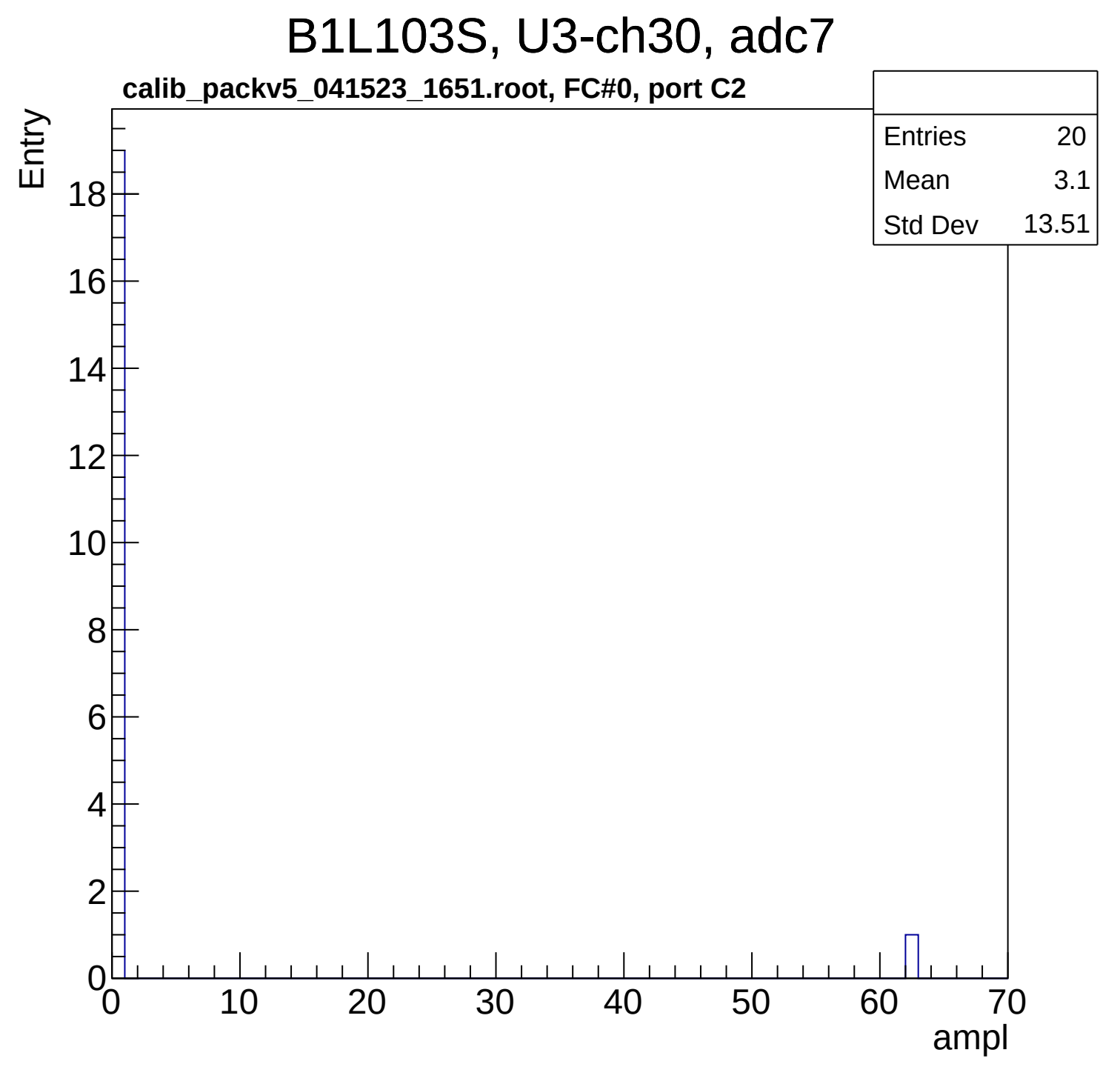
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch30, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
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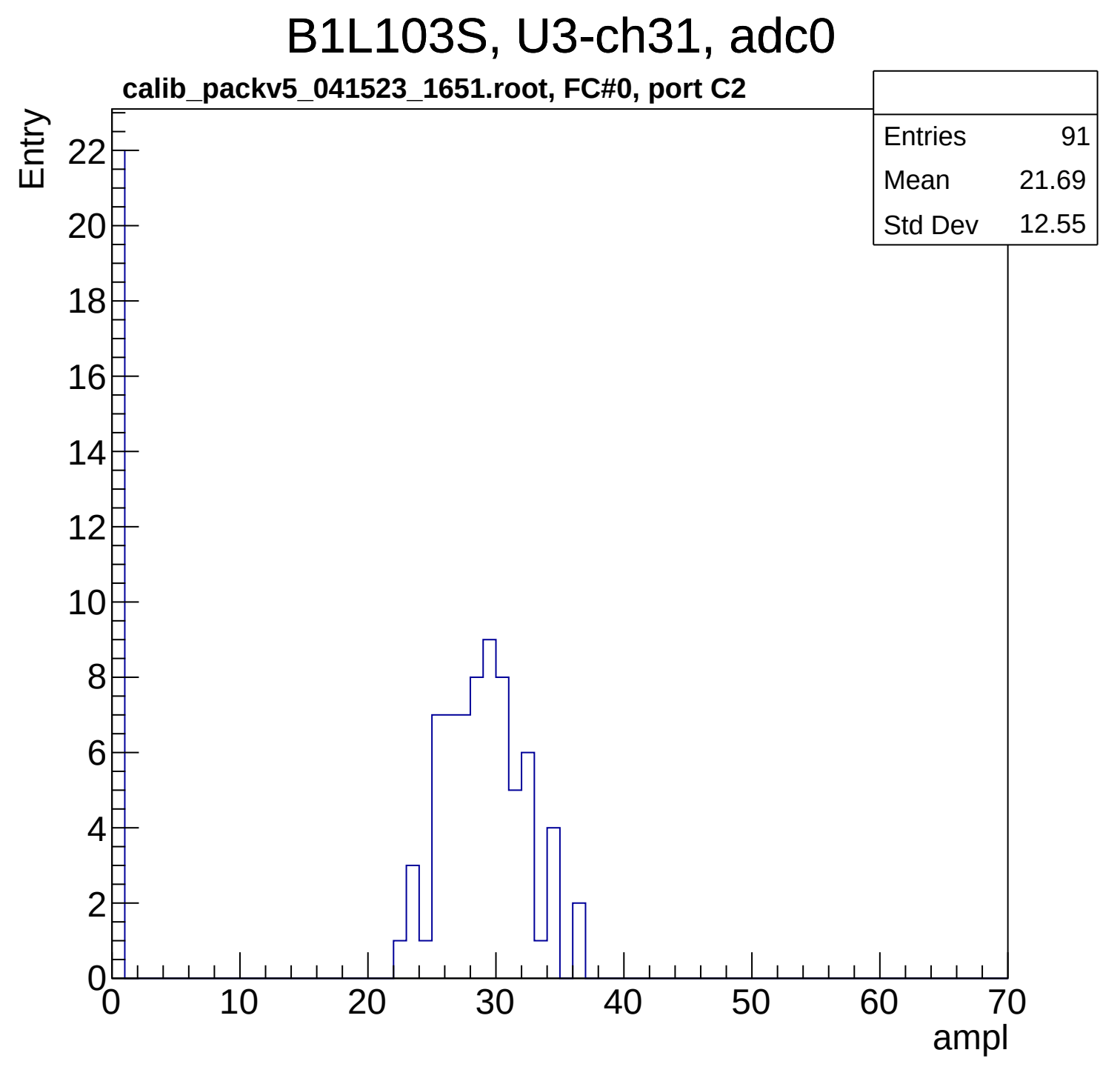
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch31, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 21.69
Std Dev 12.55
Entry
ampl
0
2
4
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8
10
12
14
16
18
20
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0
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60
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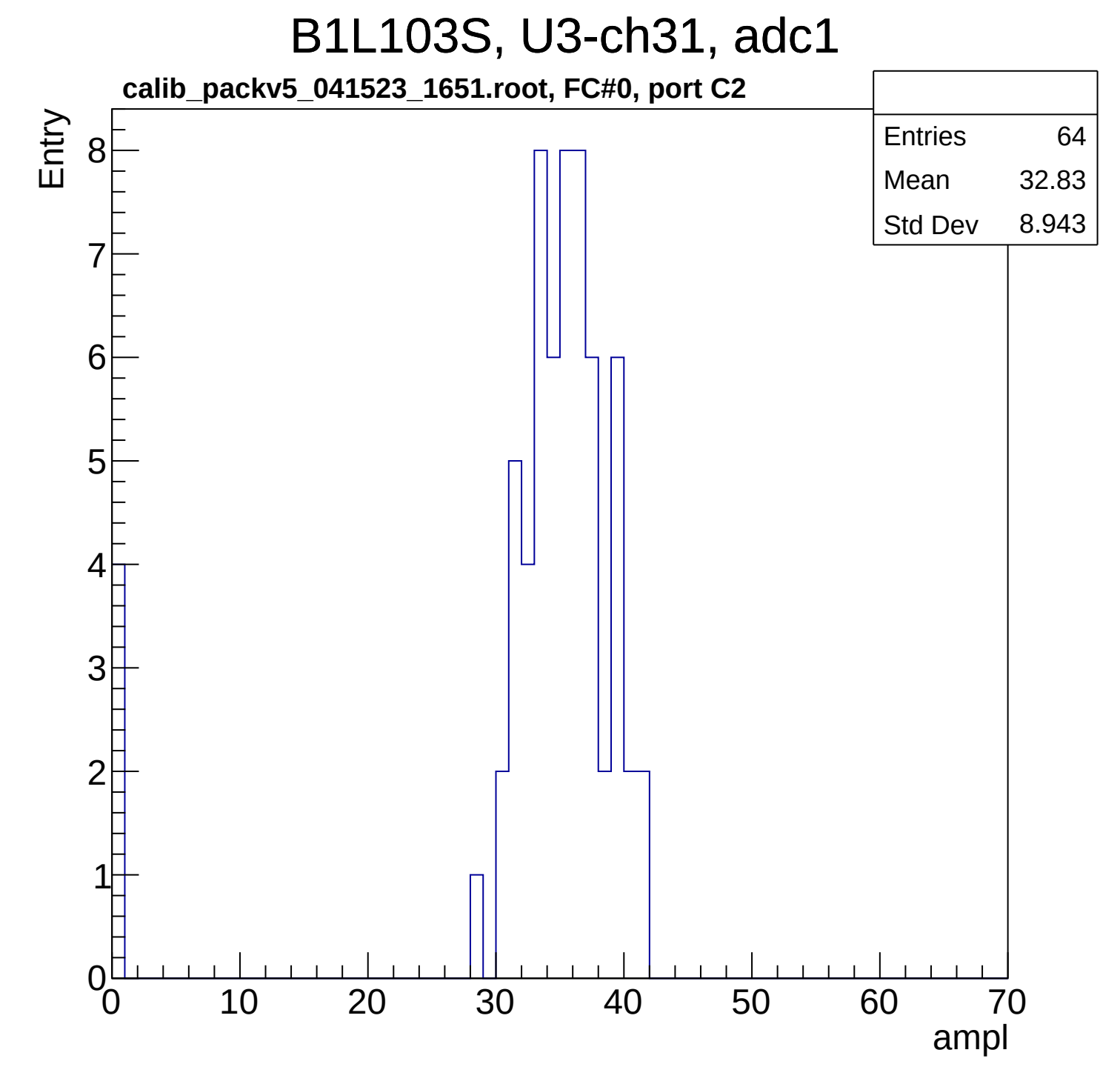
B1L103S, U3-ch31, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 32.83
Std Dev 8.943
Entry
ampl
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1
2
3
4
5
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7
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0
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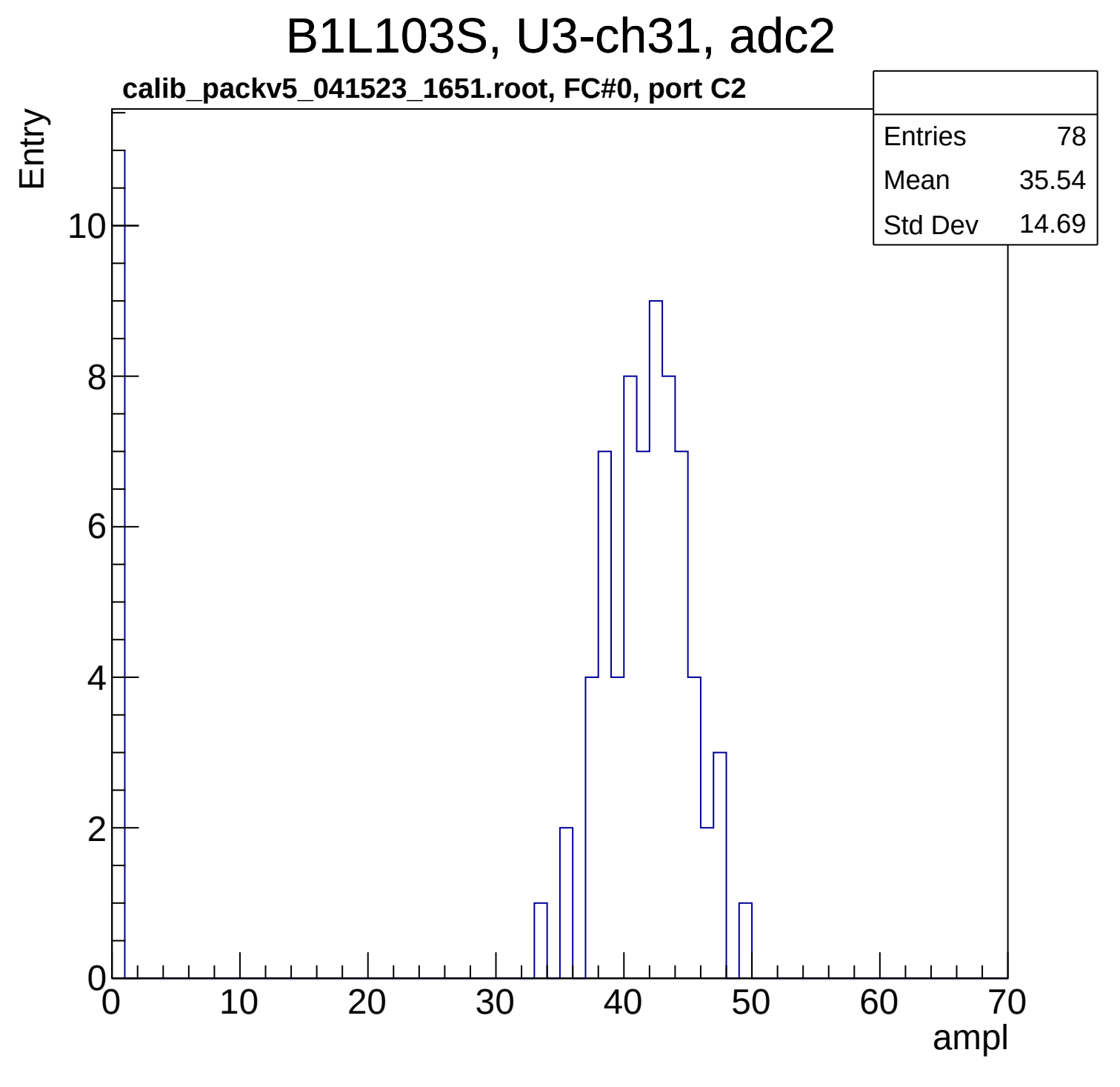
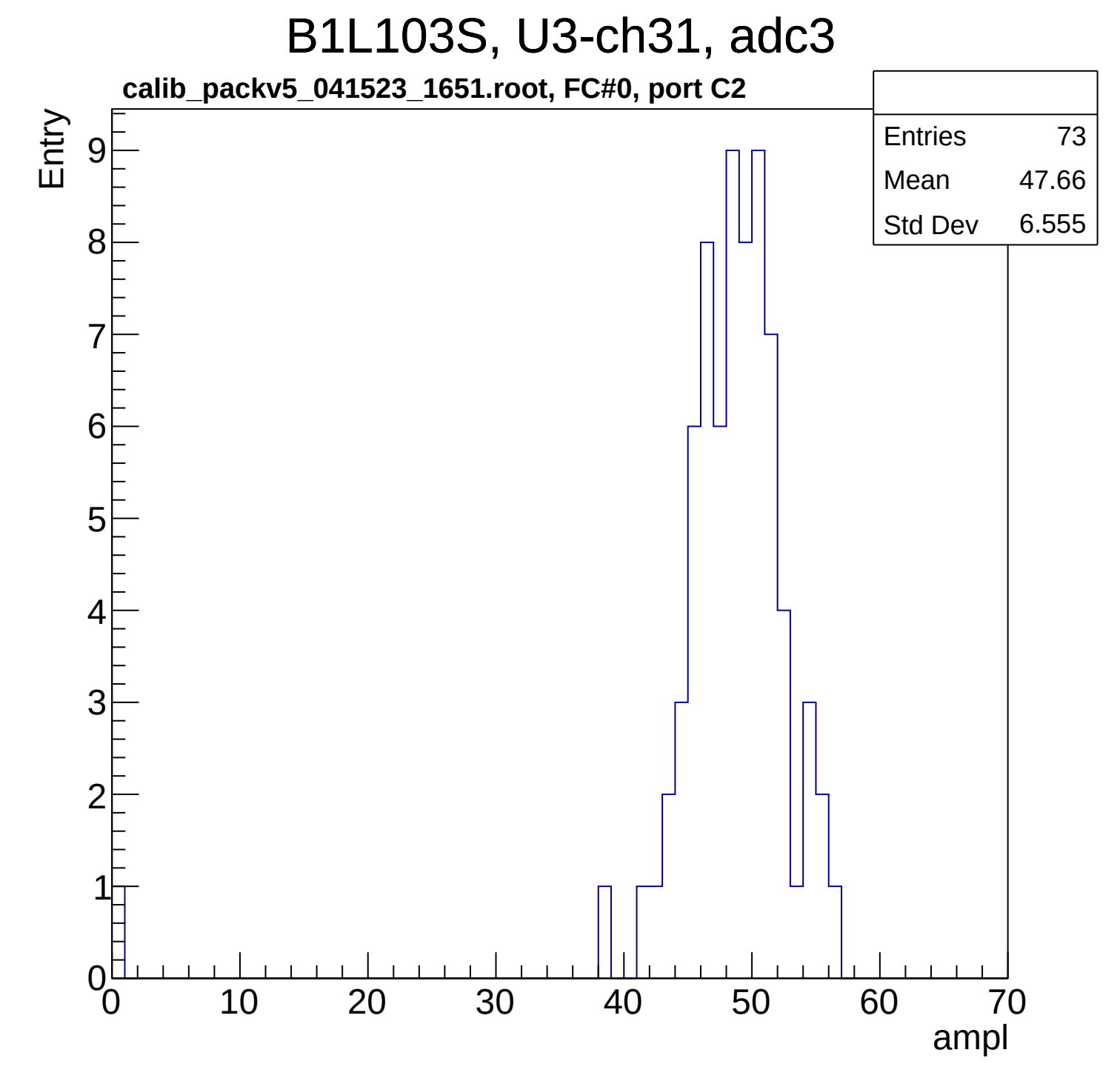

B1L103S, U3-ch31, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 35.54
Std Dev 14.69
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch31, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 47.66
Std Dev 6.555
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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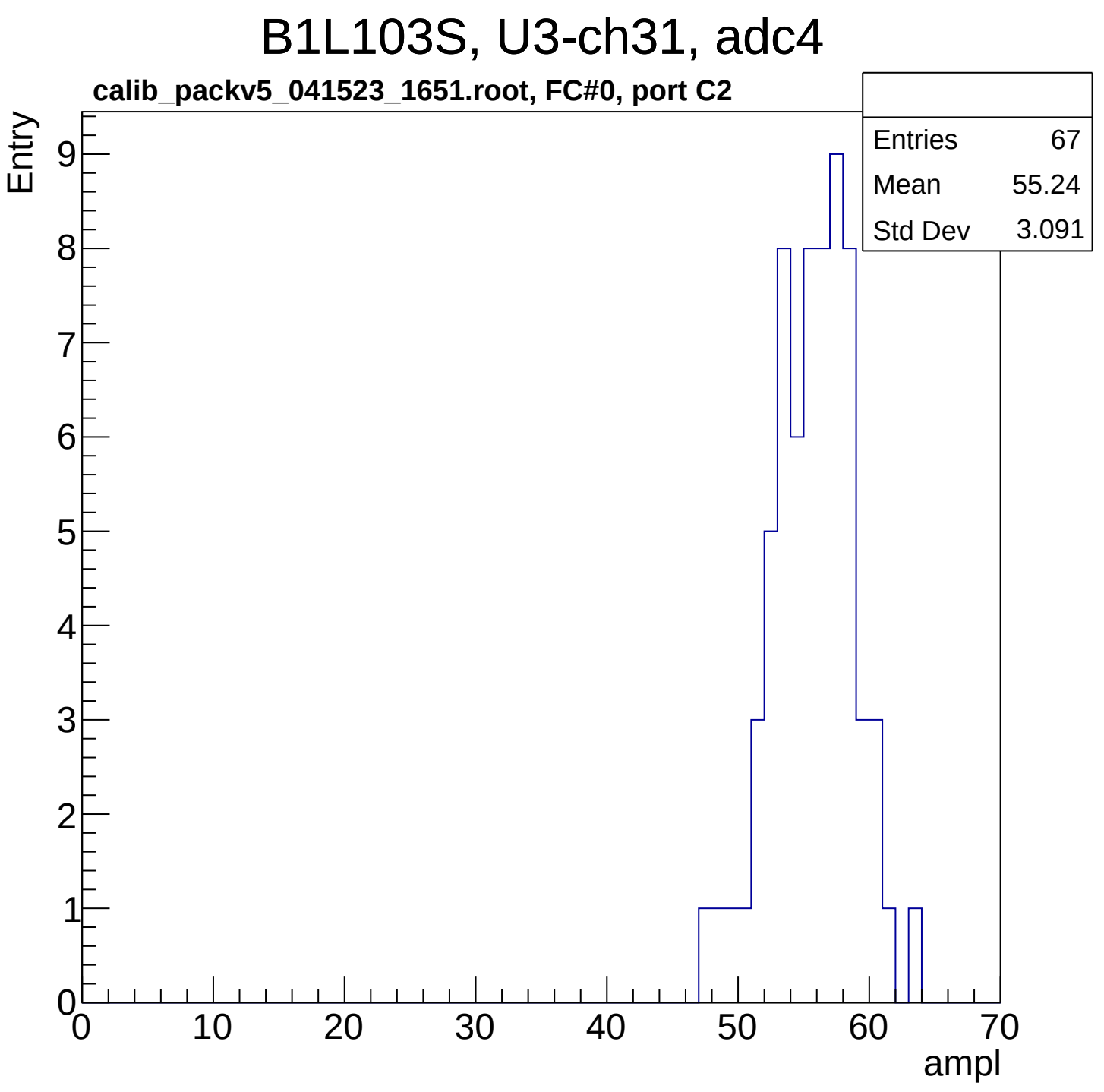
B1L103S, U3-ch31, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 55.24
Std Dev 3.091
Entry
ampl
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2
3
4
5
6
7
8
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0
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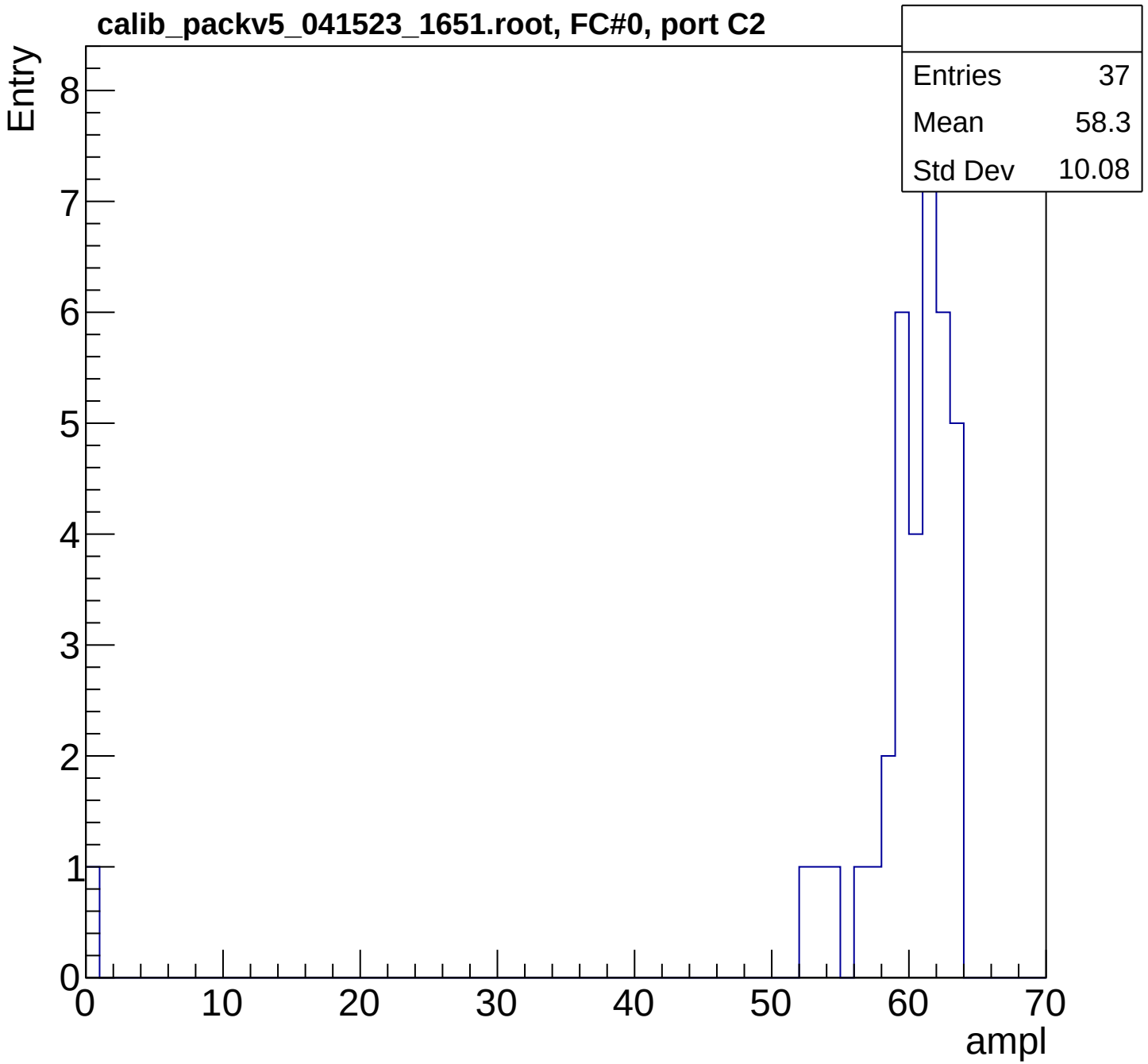
B1L103S, U3-ch31, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 58.3
Std Dev 10.08
Entry
ampl
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1
2
3
4
5
6
7
8
0
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40
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60
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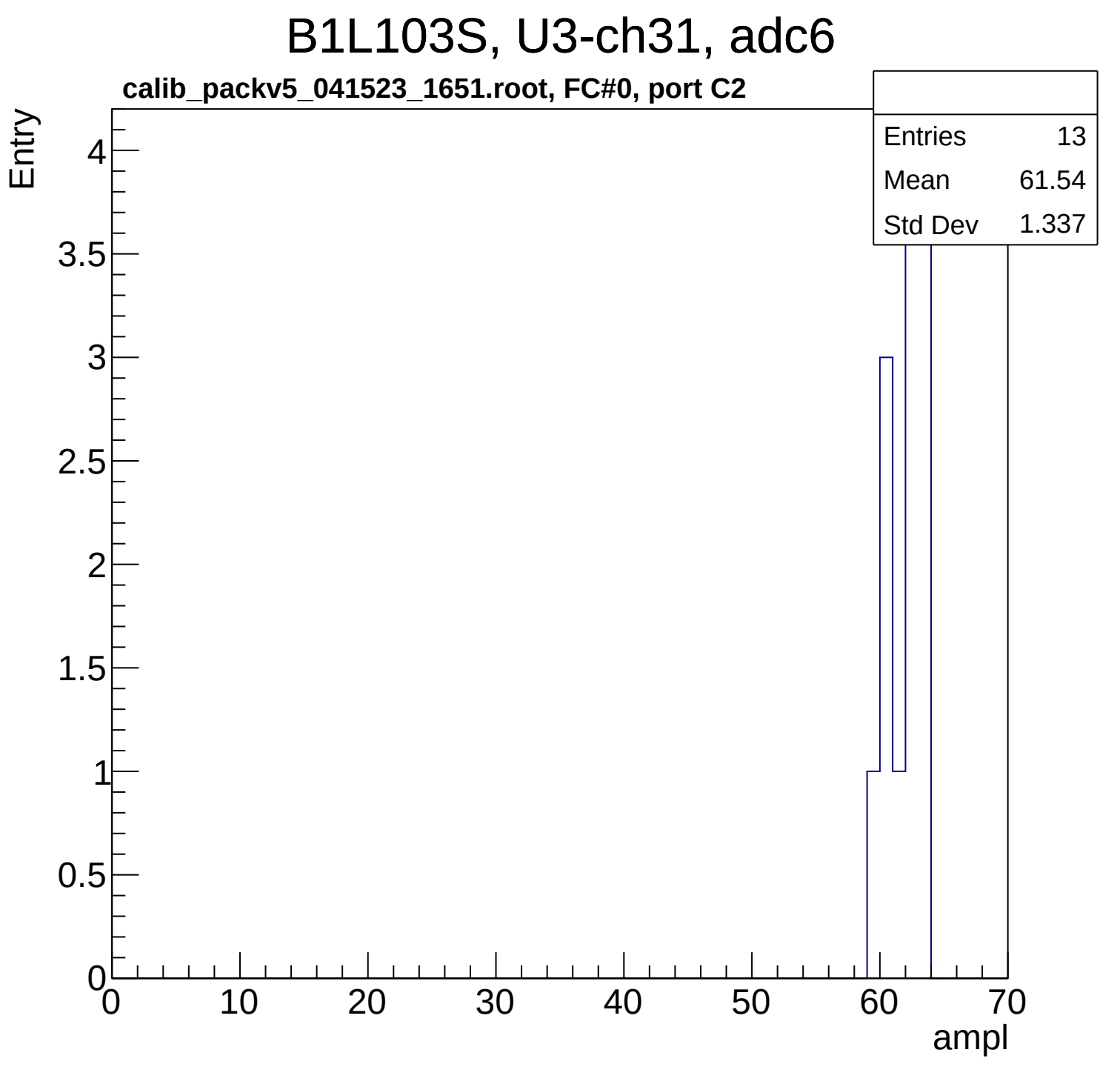
B1L103S, U3-ch31, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 61.54
Std Dev 1.337
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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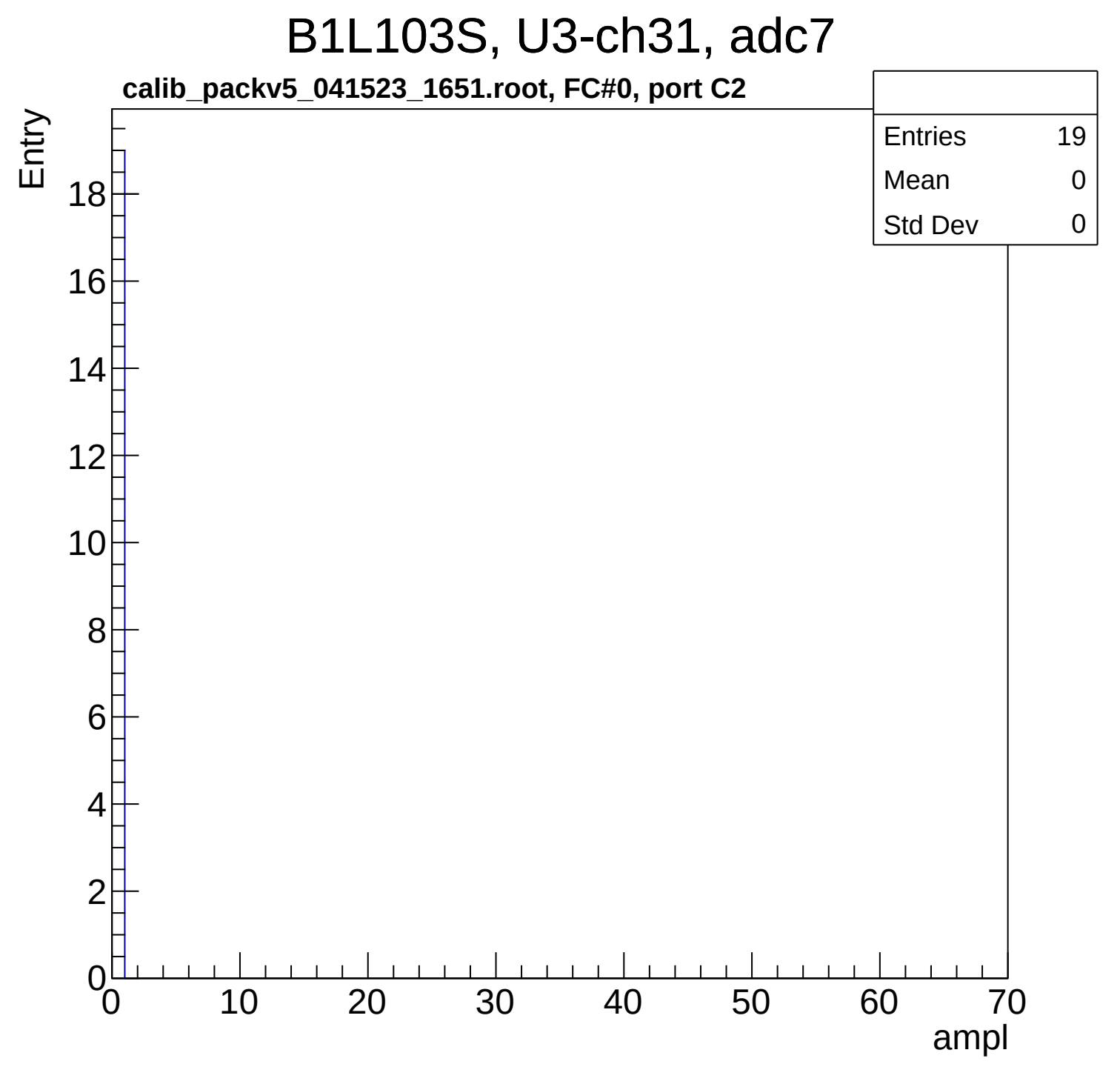
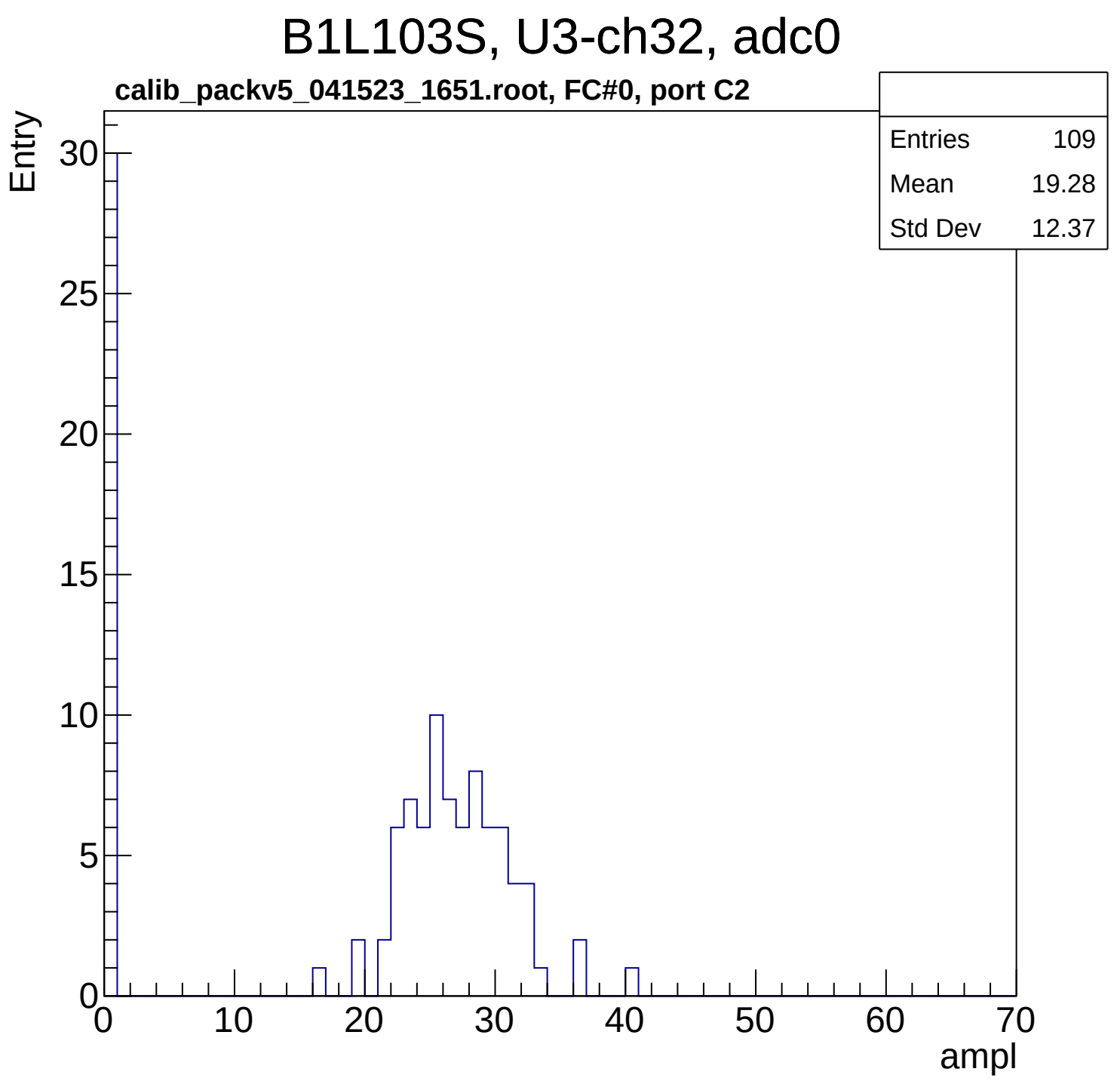
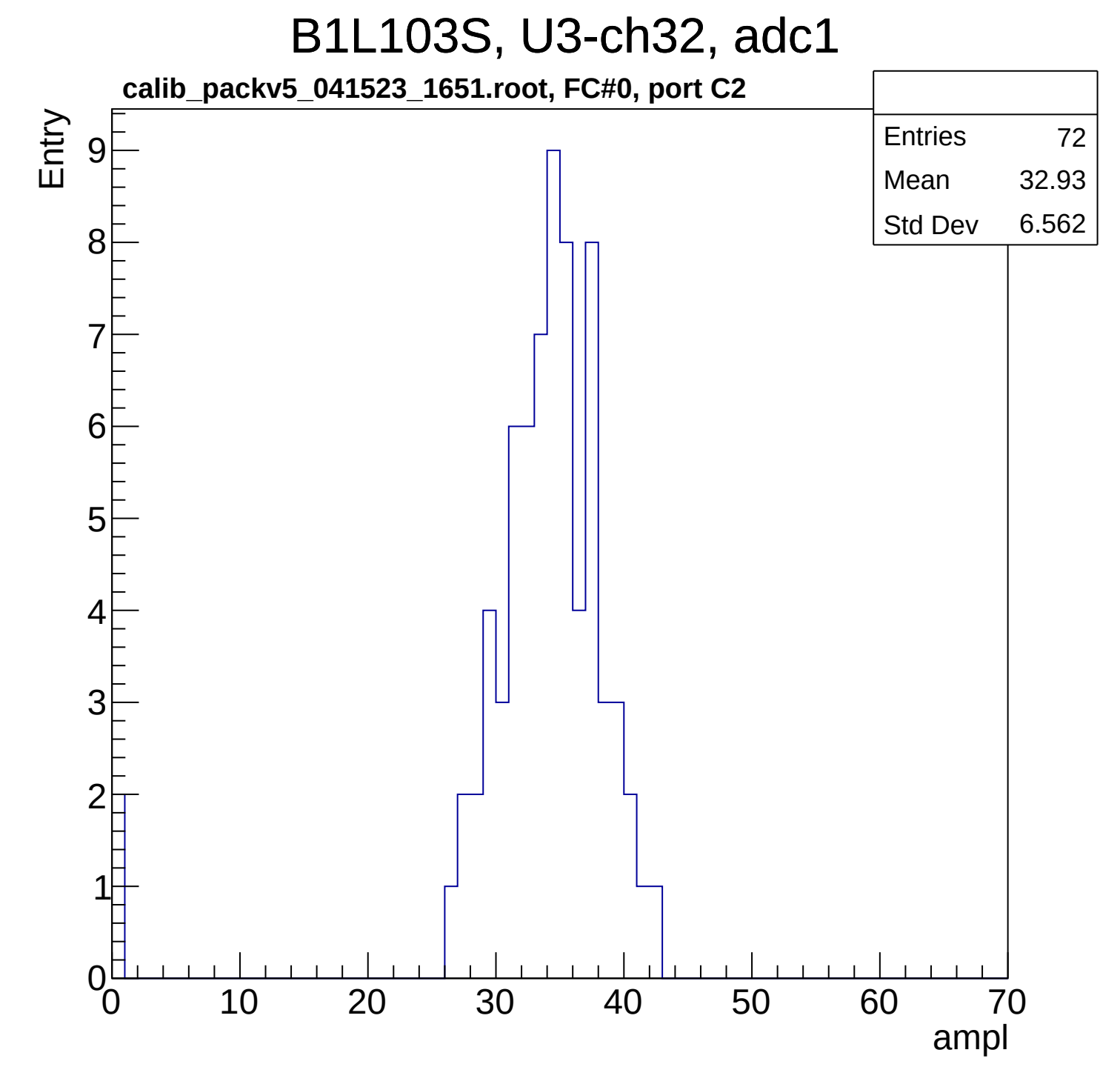

B1L103S, U3-ch31, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch32, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 109
Mean 19.28
Std Dev 12.37
Entry
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch32, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 32.93
Std Dev 6.562
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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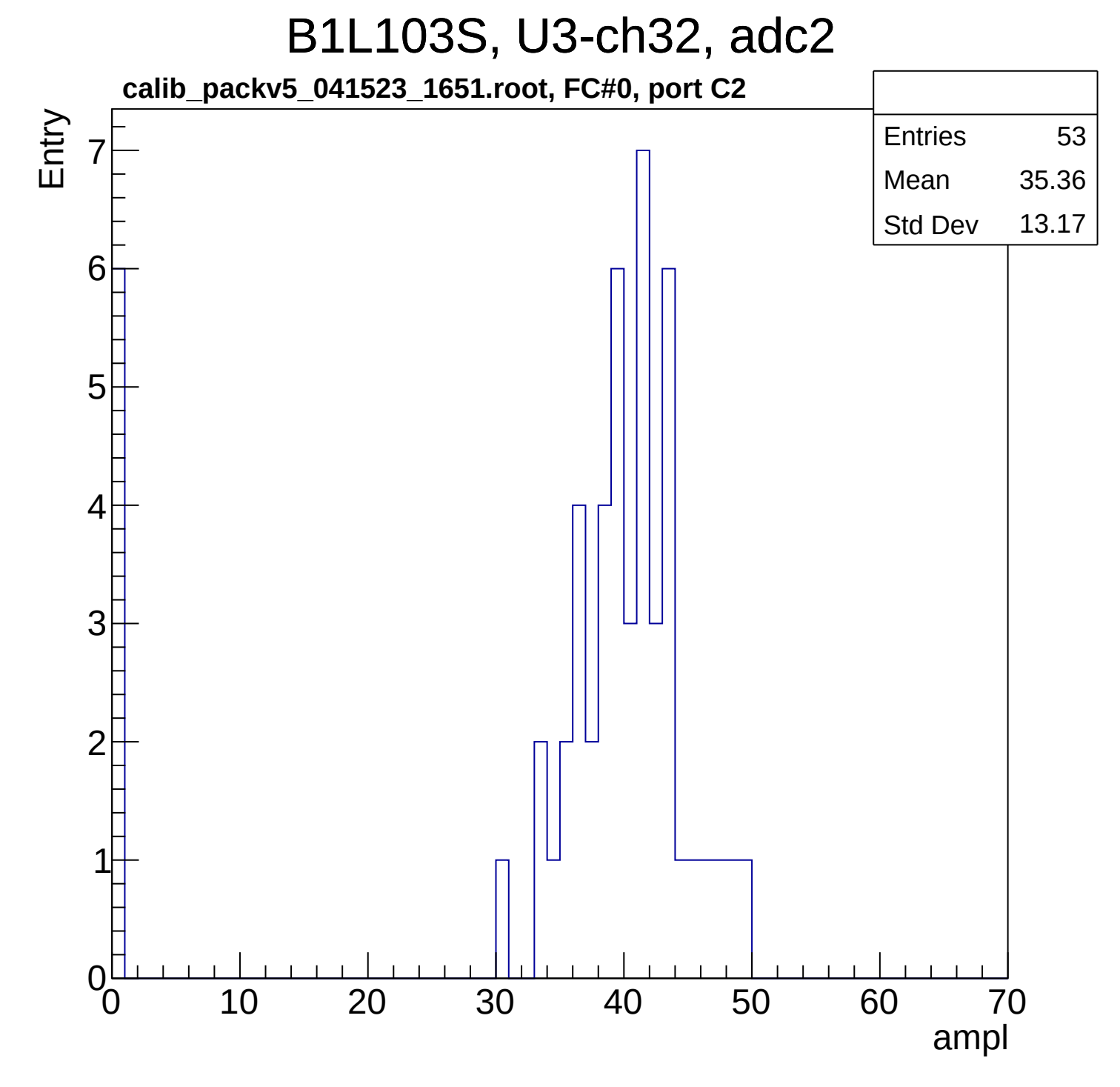
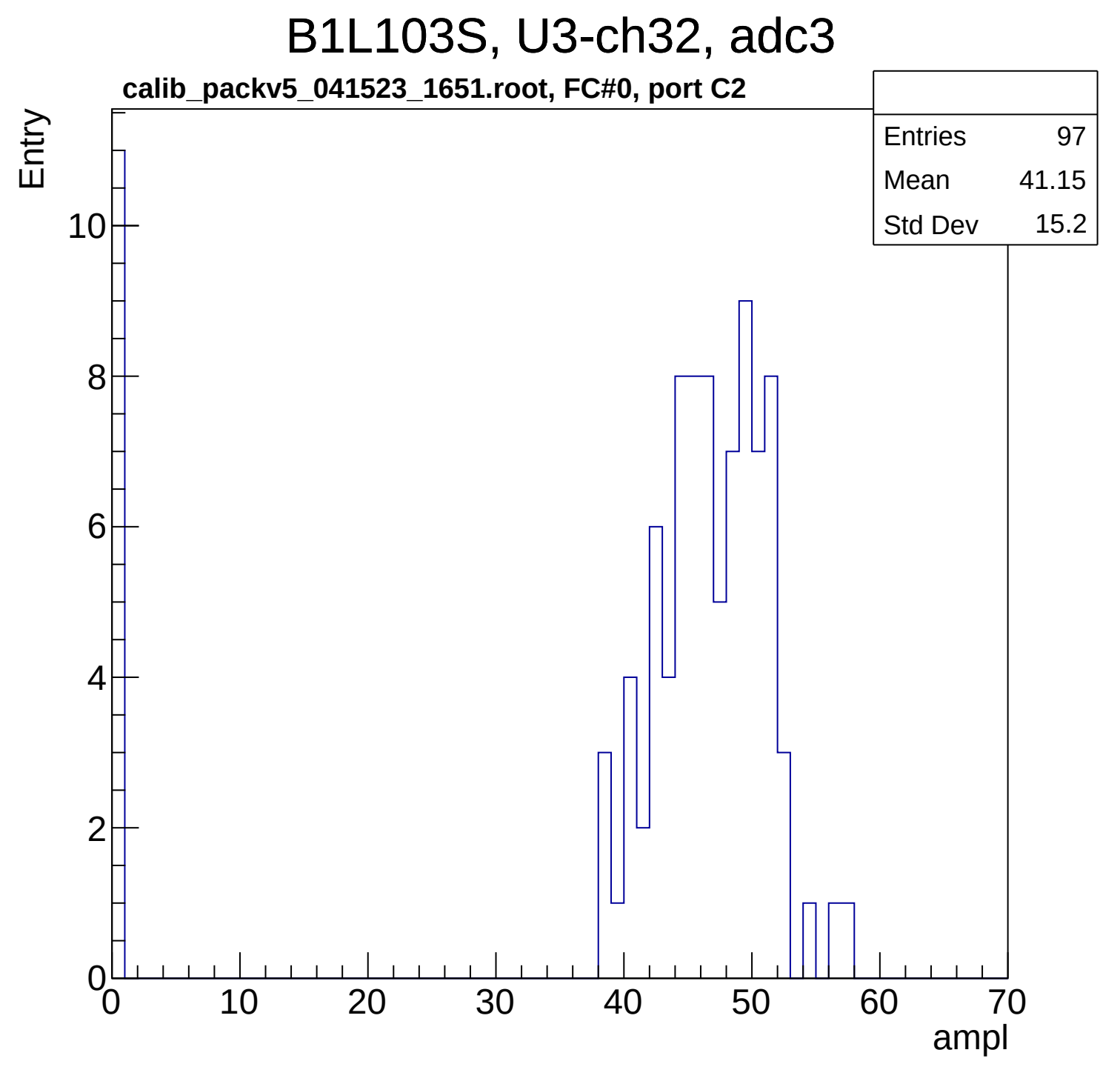
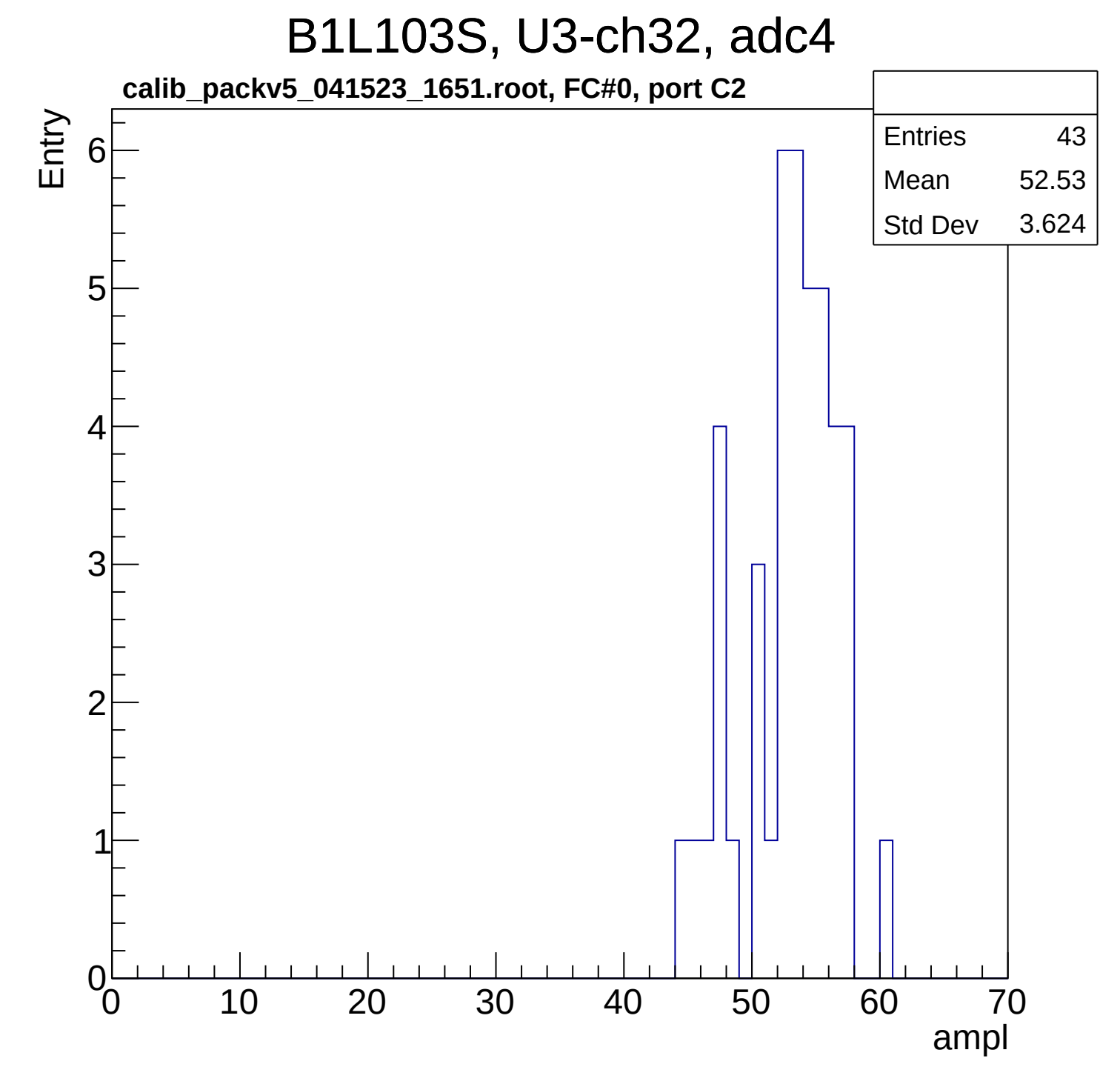
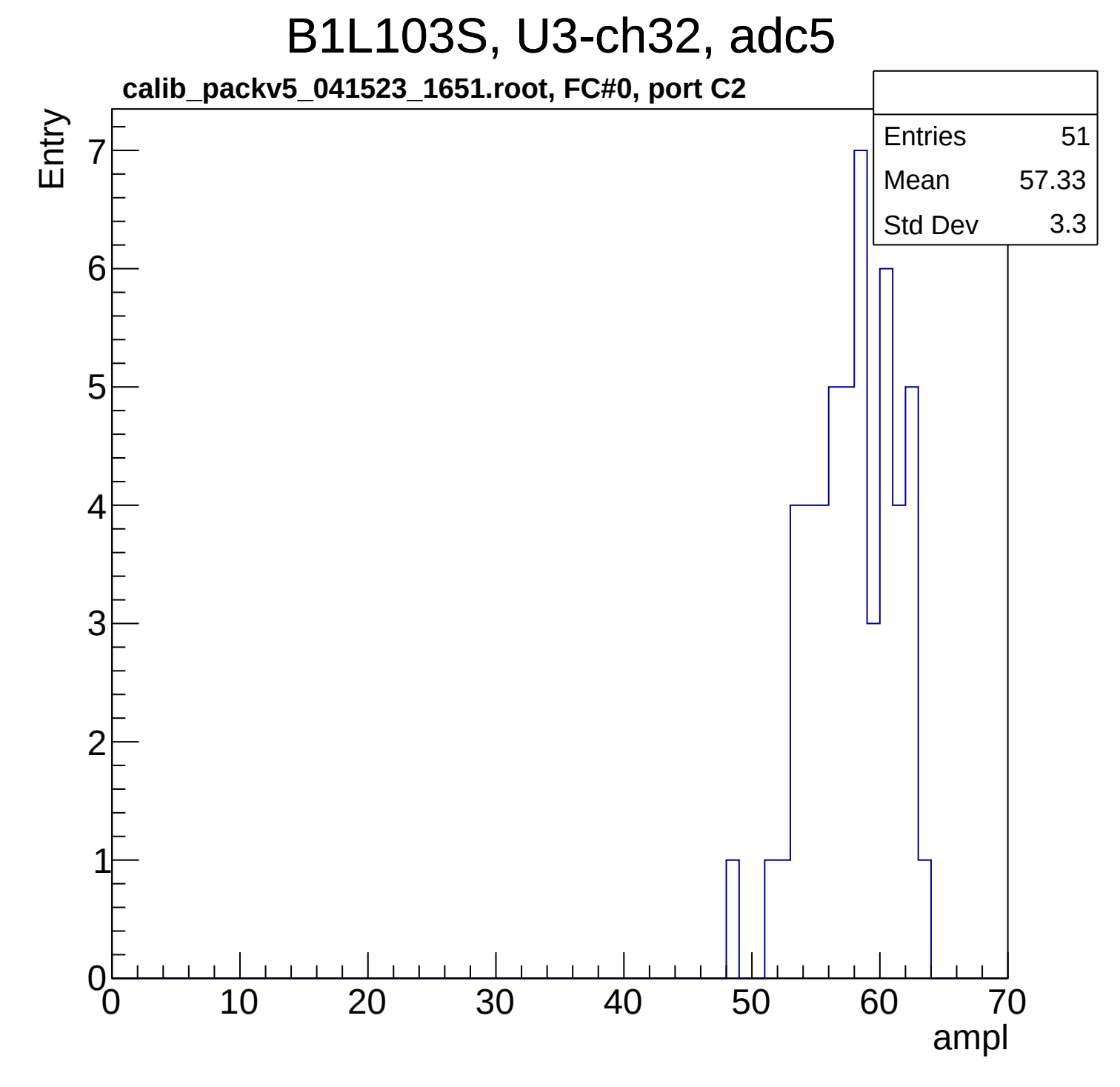
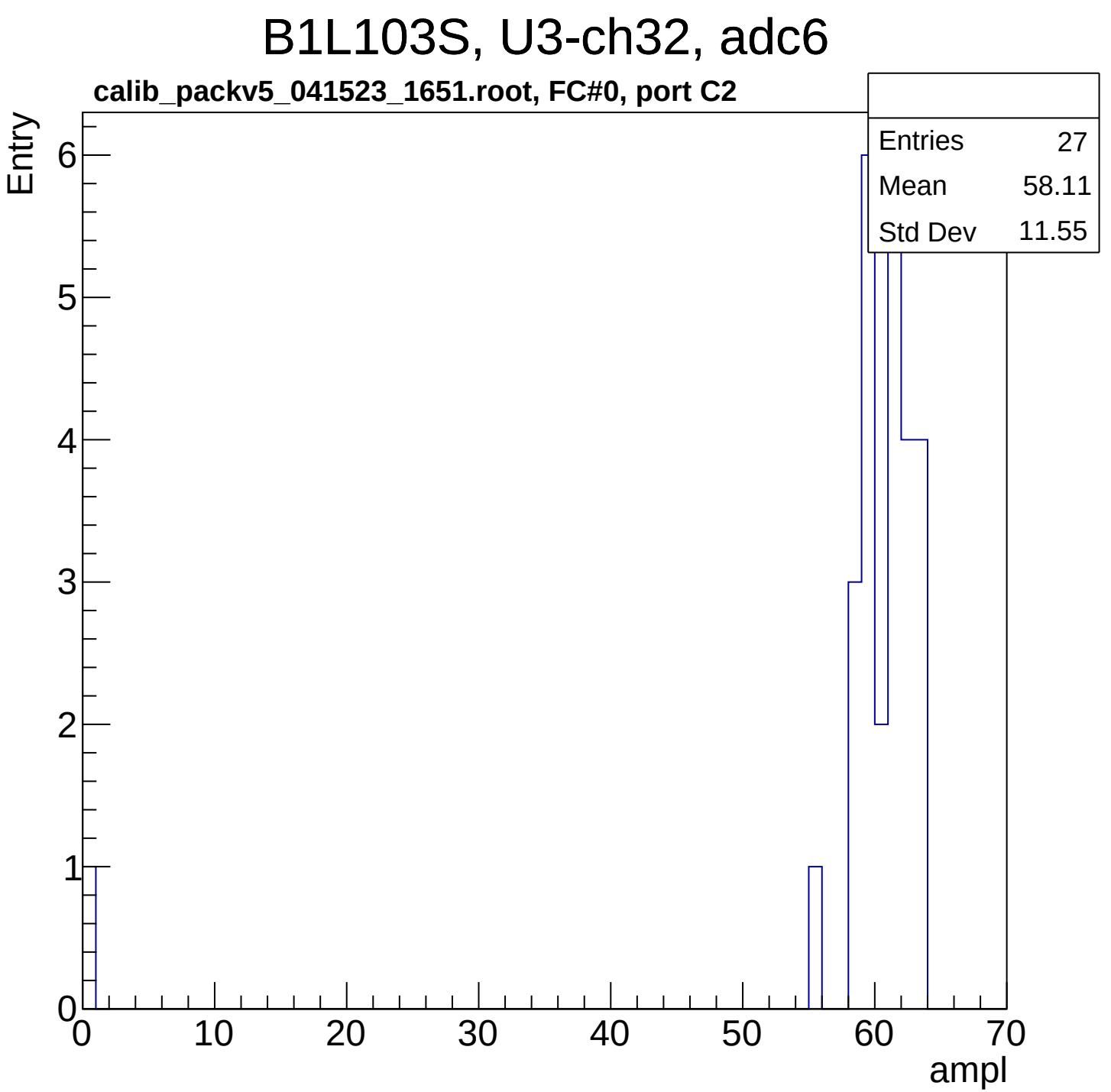
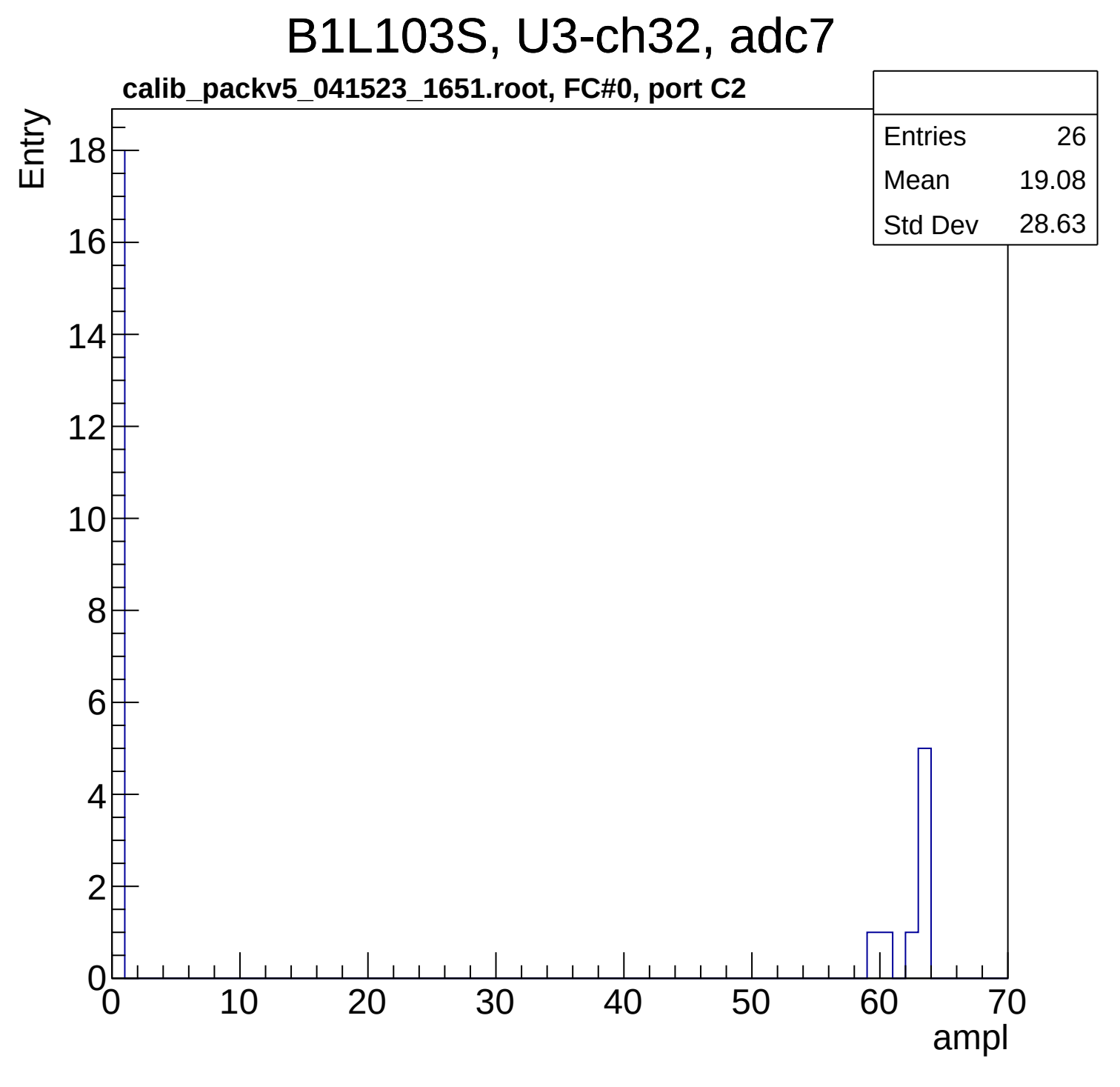

B1L103S, U3-ch32, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 35.36
Std Dev 13.17
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch32, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 41.15
Std Dev 15.2
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch32, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 52.53
Std Dev 3.624
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U3-ch32, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 57.33
Std Dev 3.3
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch32, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 58.11
Std Dev 11.55
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch32, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 19.08
Std Dev 28.63
Entry
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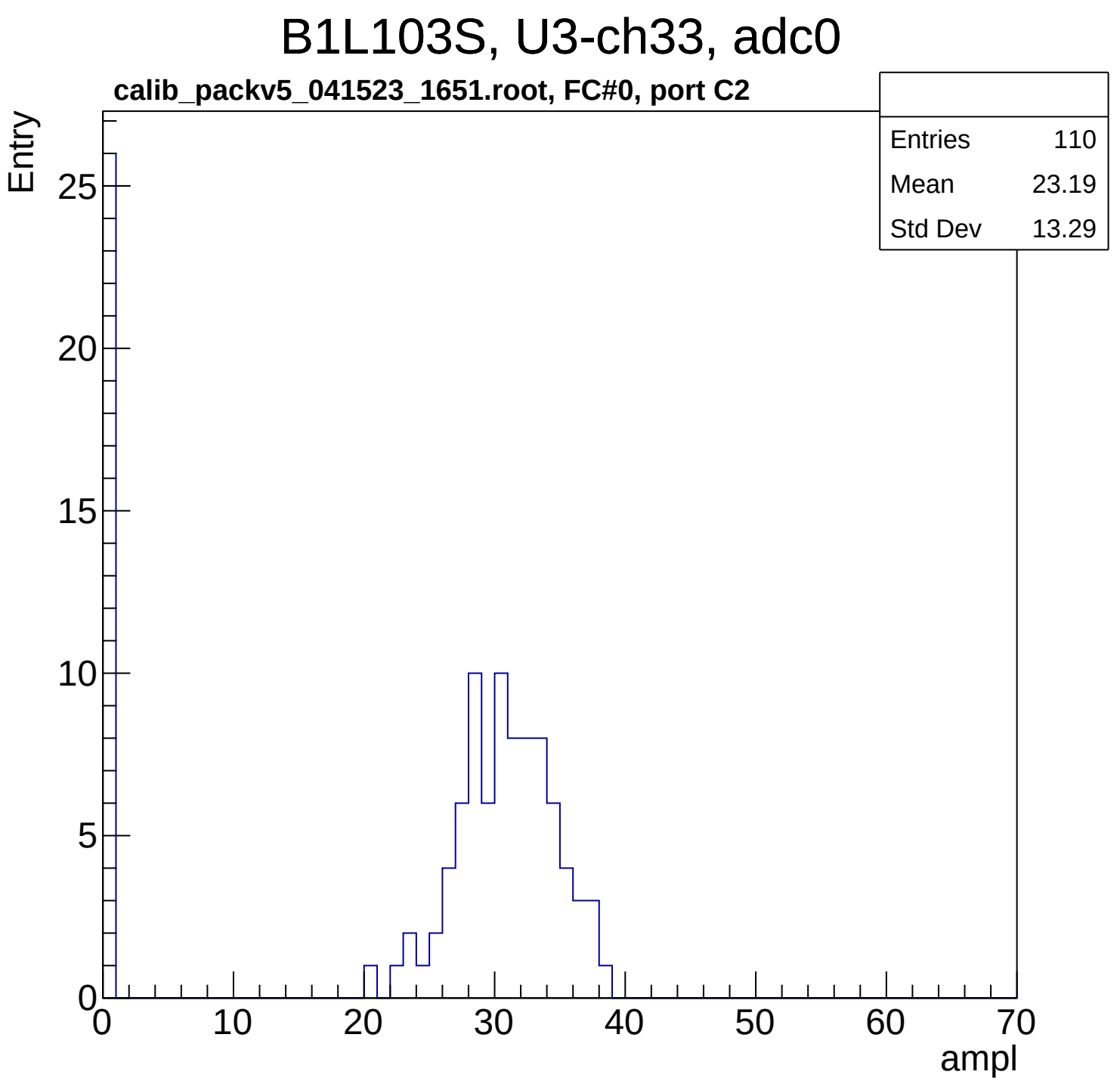
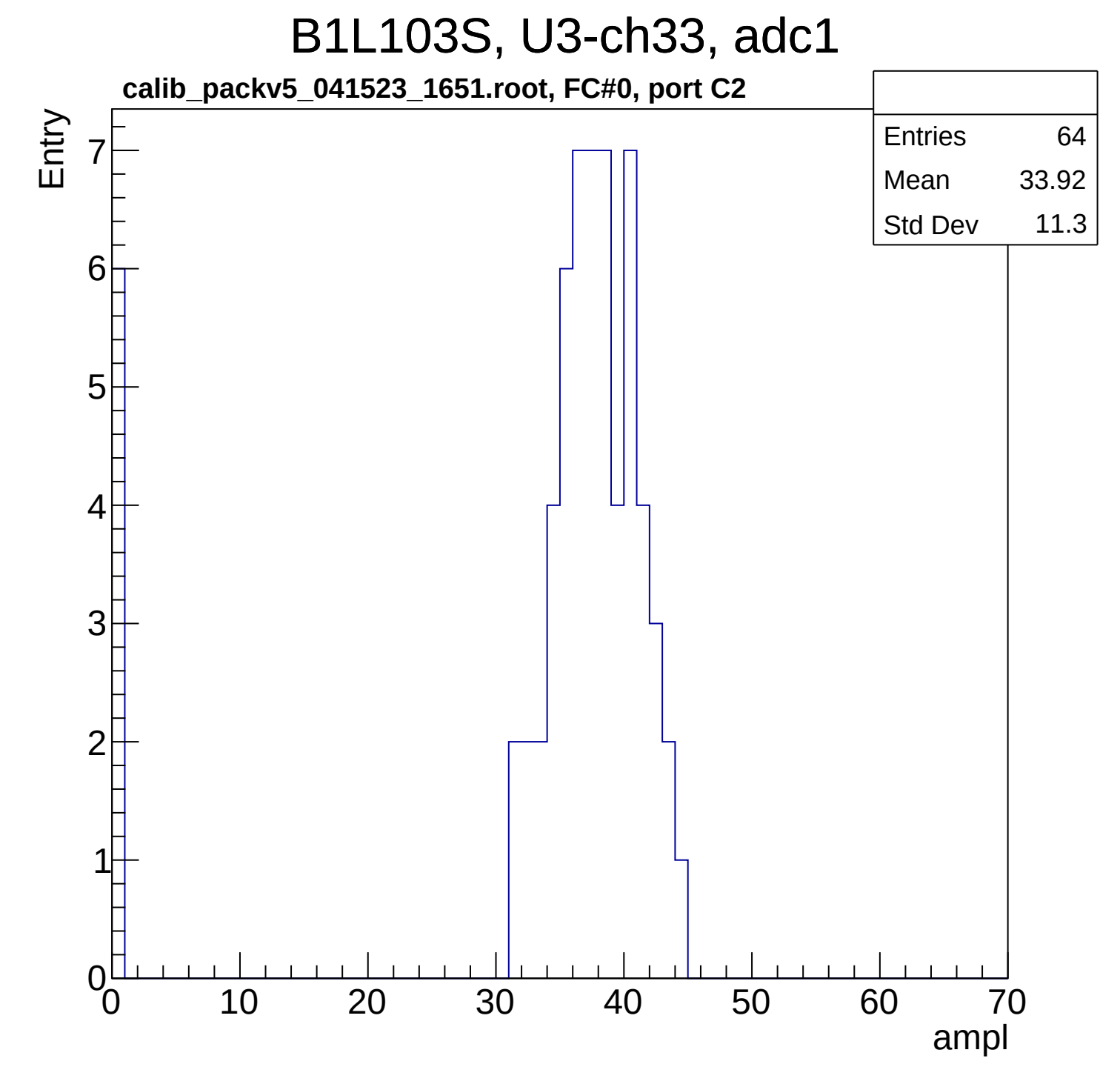
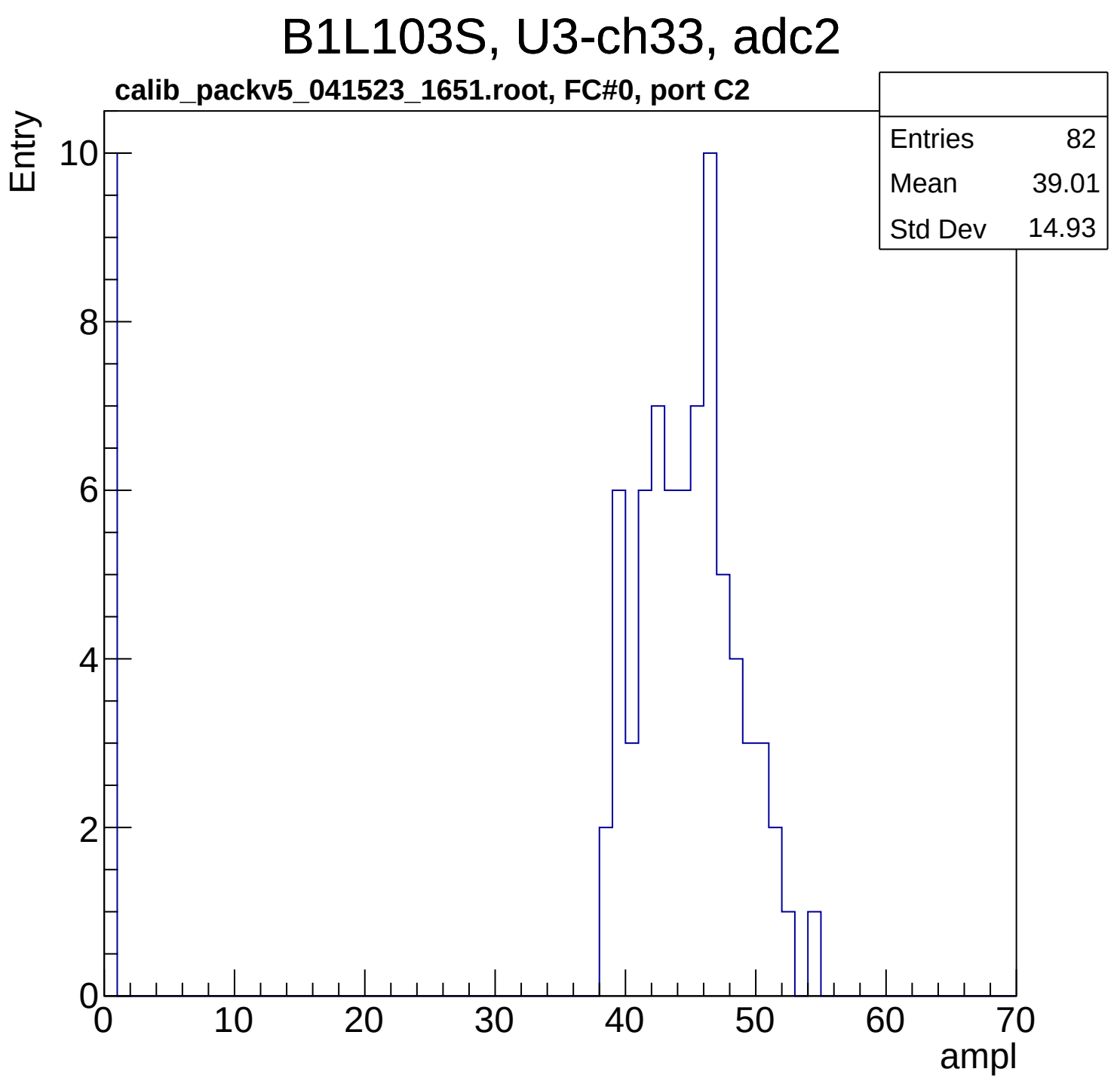
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch33, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 110
Mean 23.19
Std Dev 13.29
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch33, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 33.92
Std Dev 11.3
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch33, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 39.01
Std Dev 14.93
Entry
ampl
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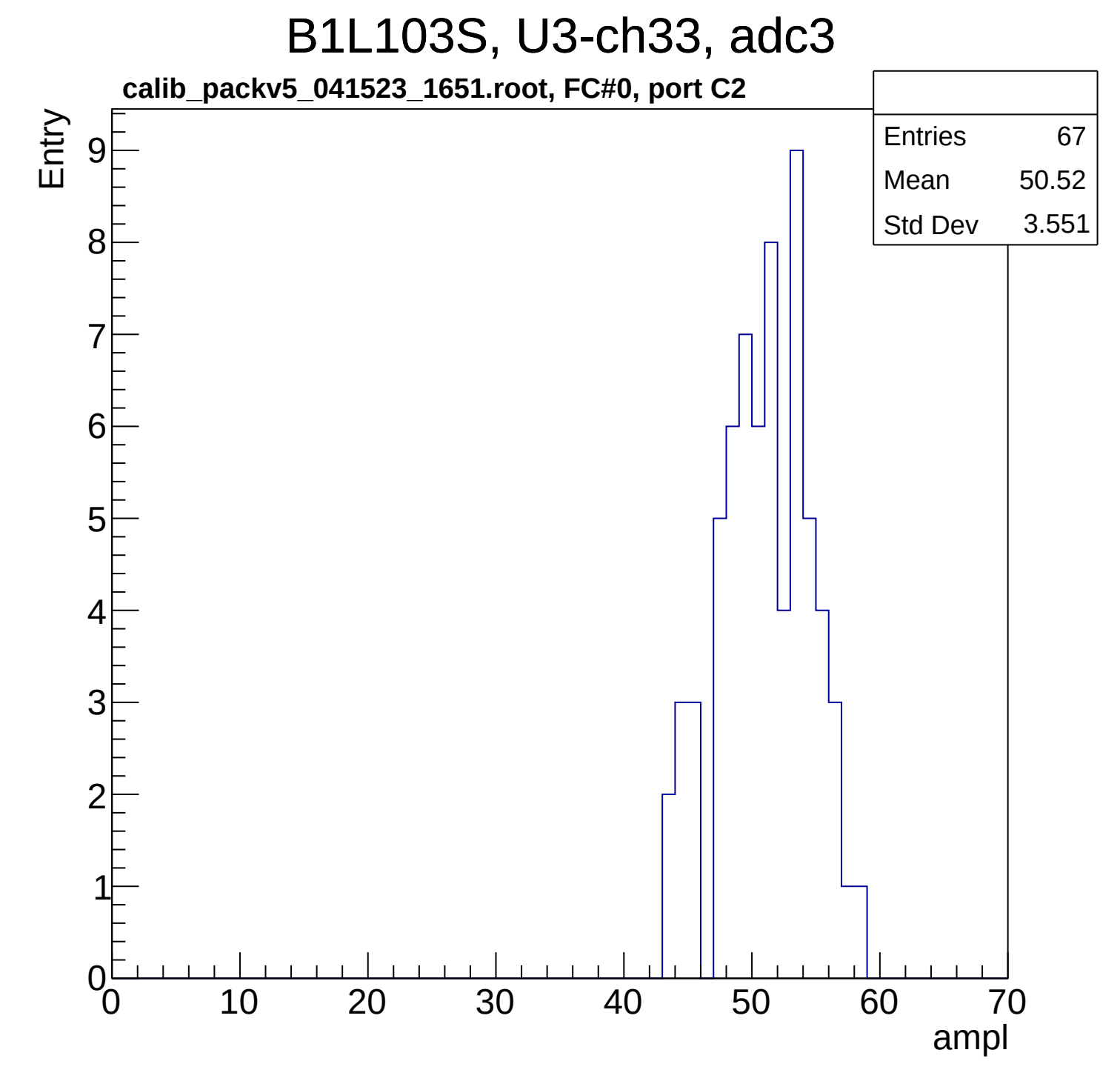
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U3-ch33, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 50.52
Std Dev 3.551
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
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60
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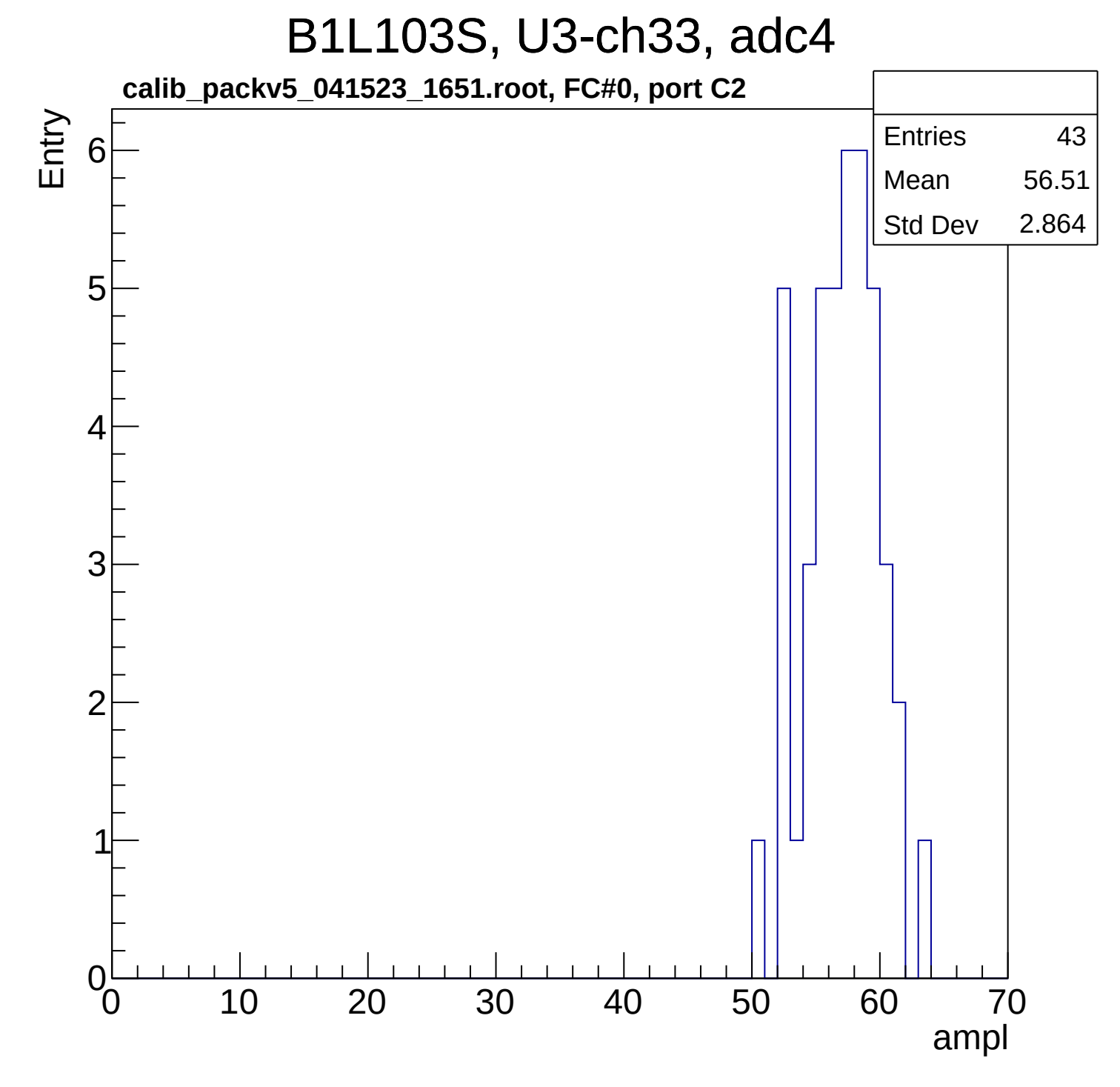
B1L103S, U3-ch33, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 56.51
Std Dev 2.864
Entry
ampl
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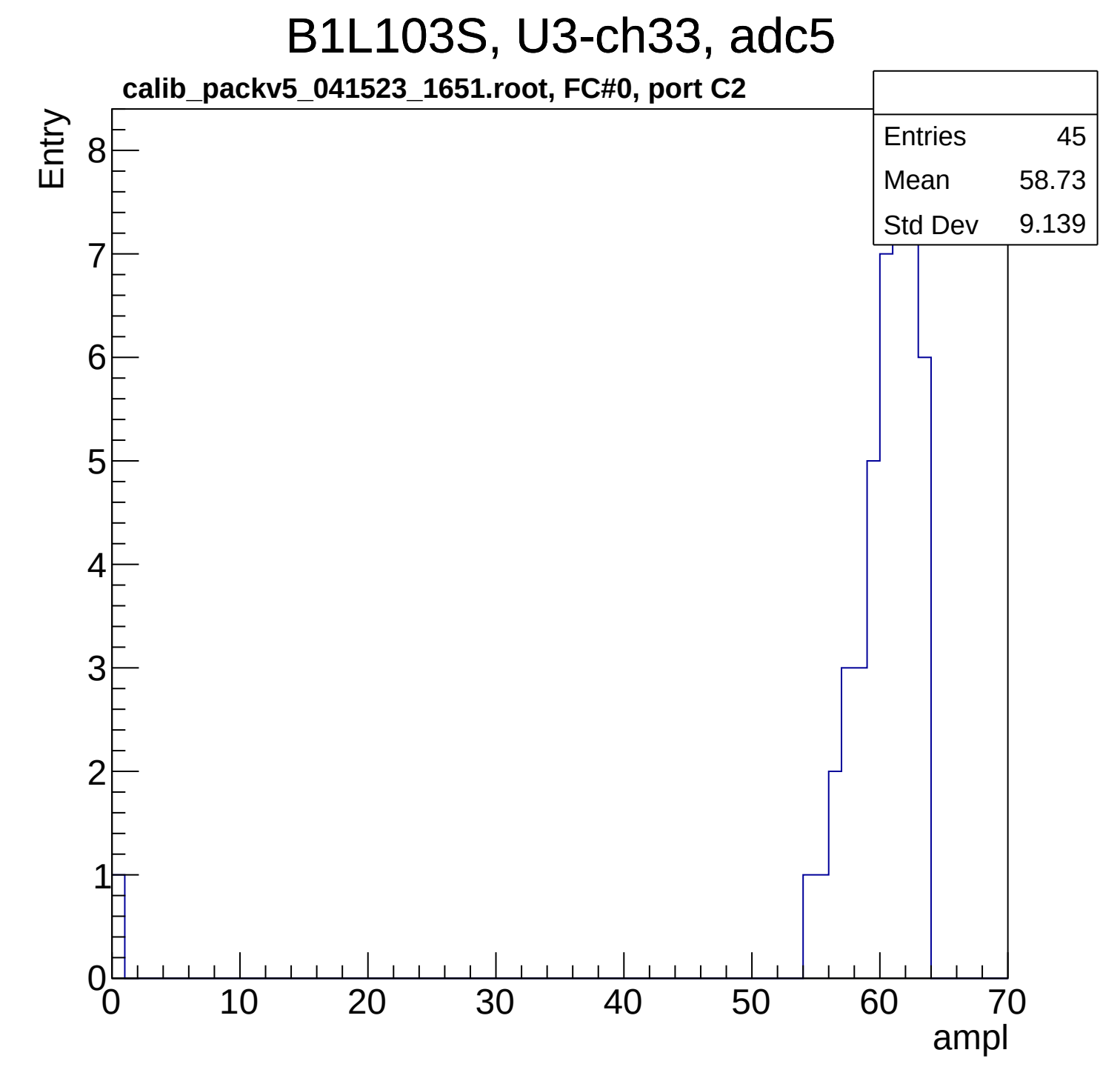
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U3-ch33, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 58.73
Std Dev 9.139
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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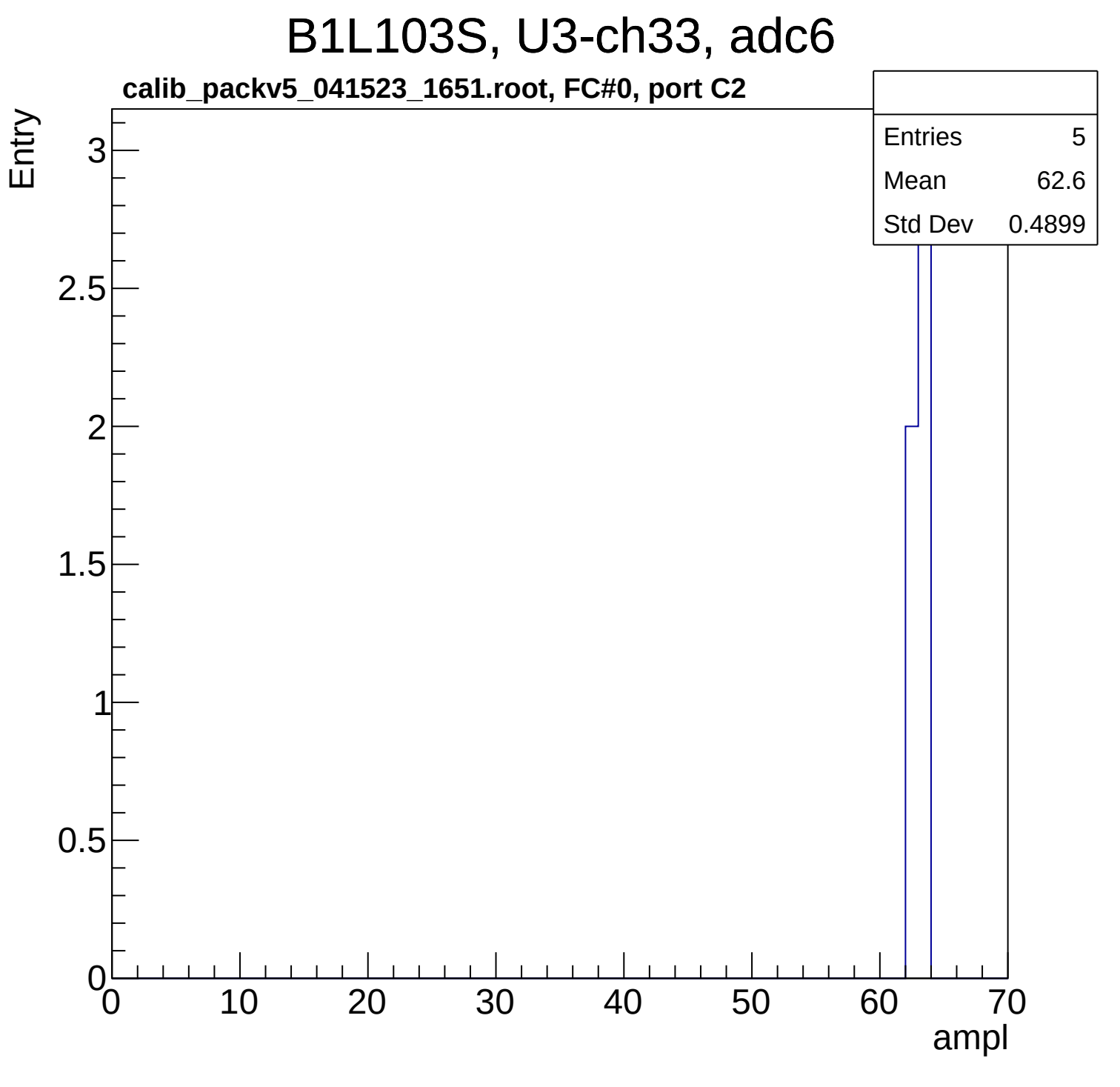
B1L103S, U3-ch33, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 62.6
Std Dev 0.4899
Entry
ampl
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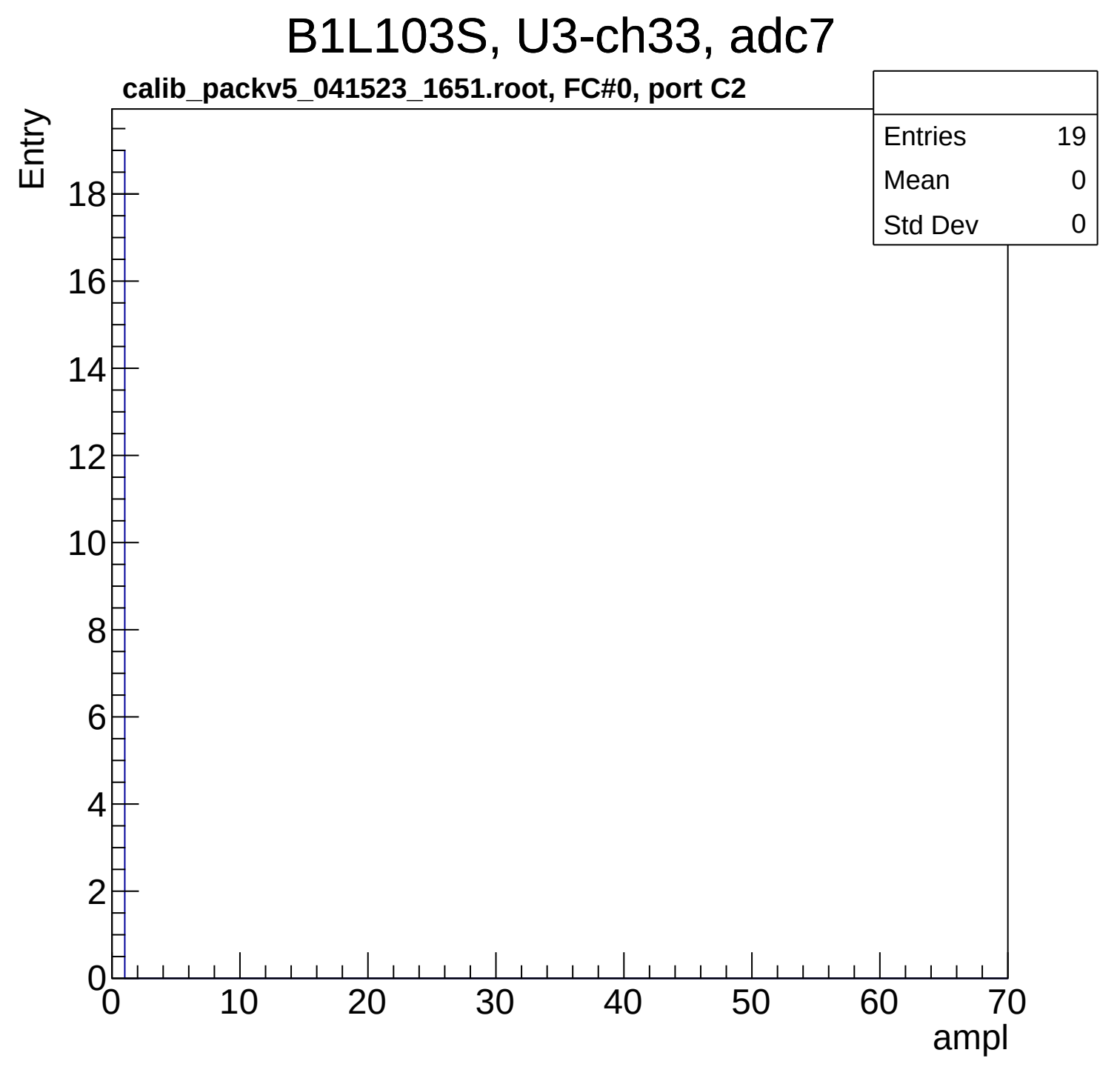
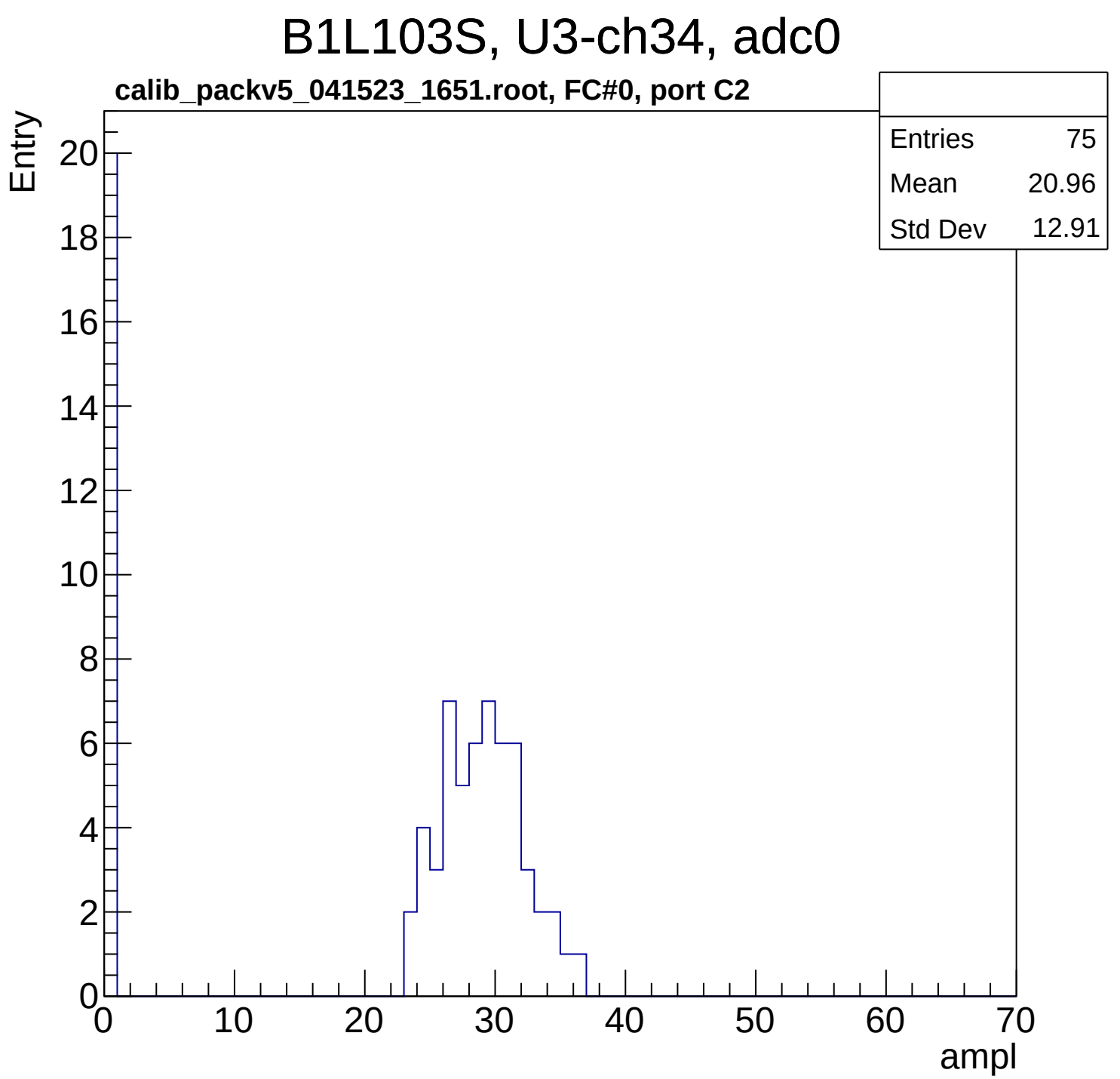
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U3-ch33, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch34, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 20.96
Std Dev 12.91
Entry
ampl
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6
8
10
12
14
16
18
20
0
10
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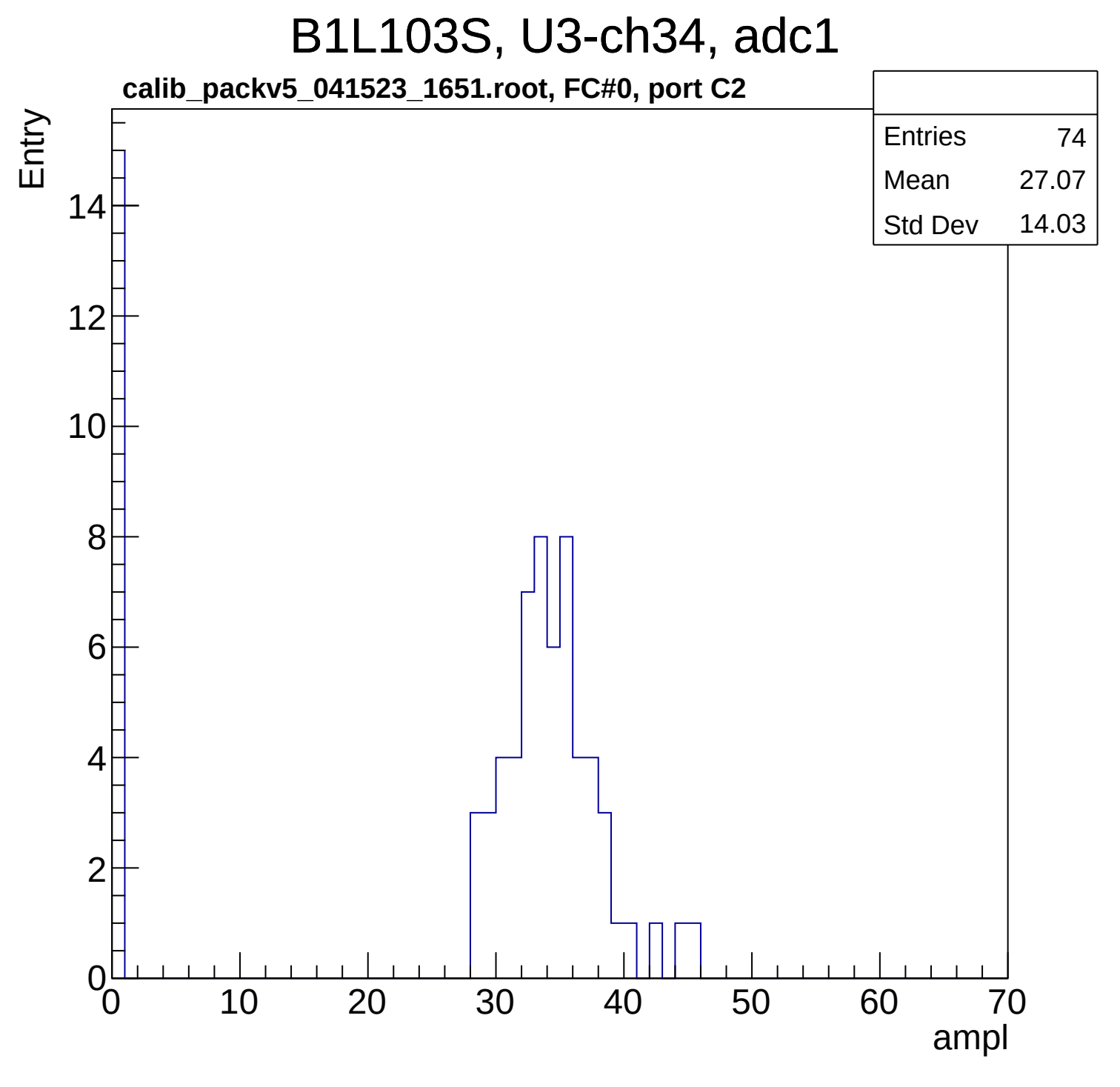
B1L103S, U3-ch34, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 27.07
Std Dev 14.03
Entry
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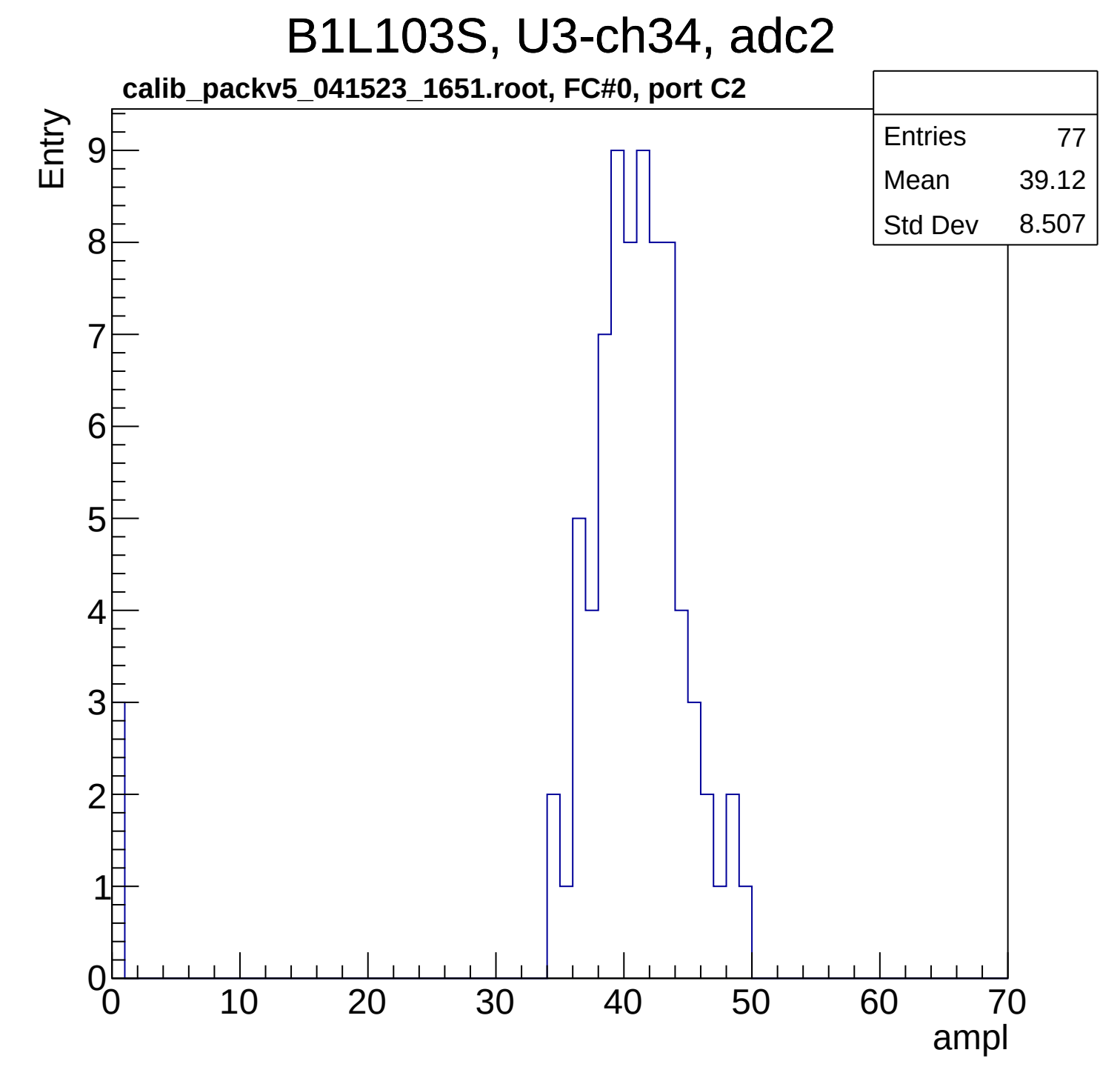
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch34, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 39.12
Std Dev 8.507
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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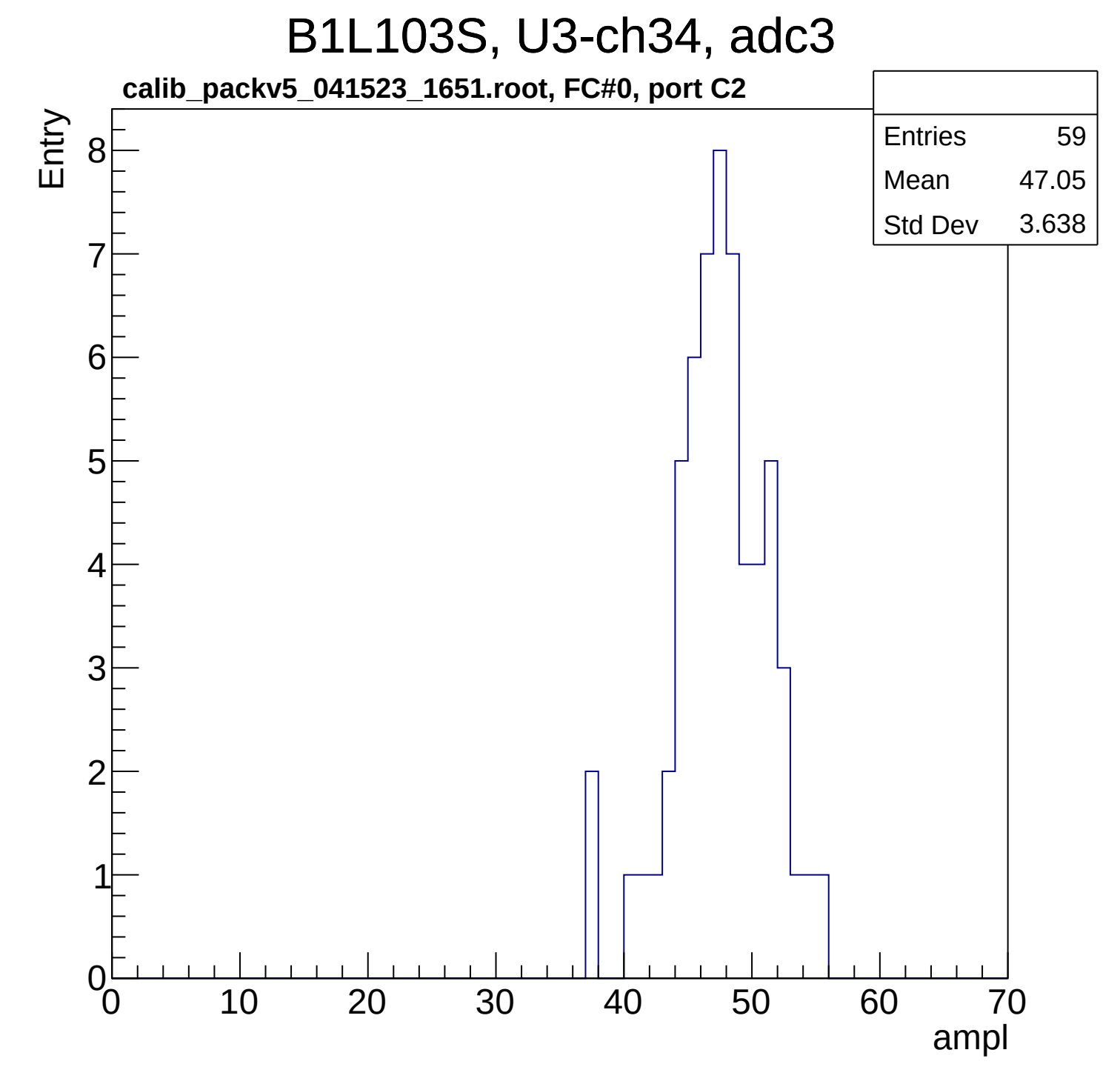
B1L103S, U3-ch34, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 47.05
Std Dev 3.638
Entry
ampl
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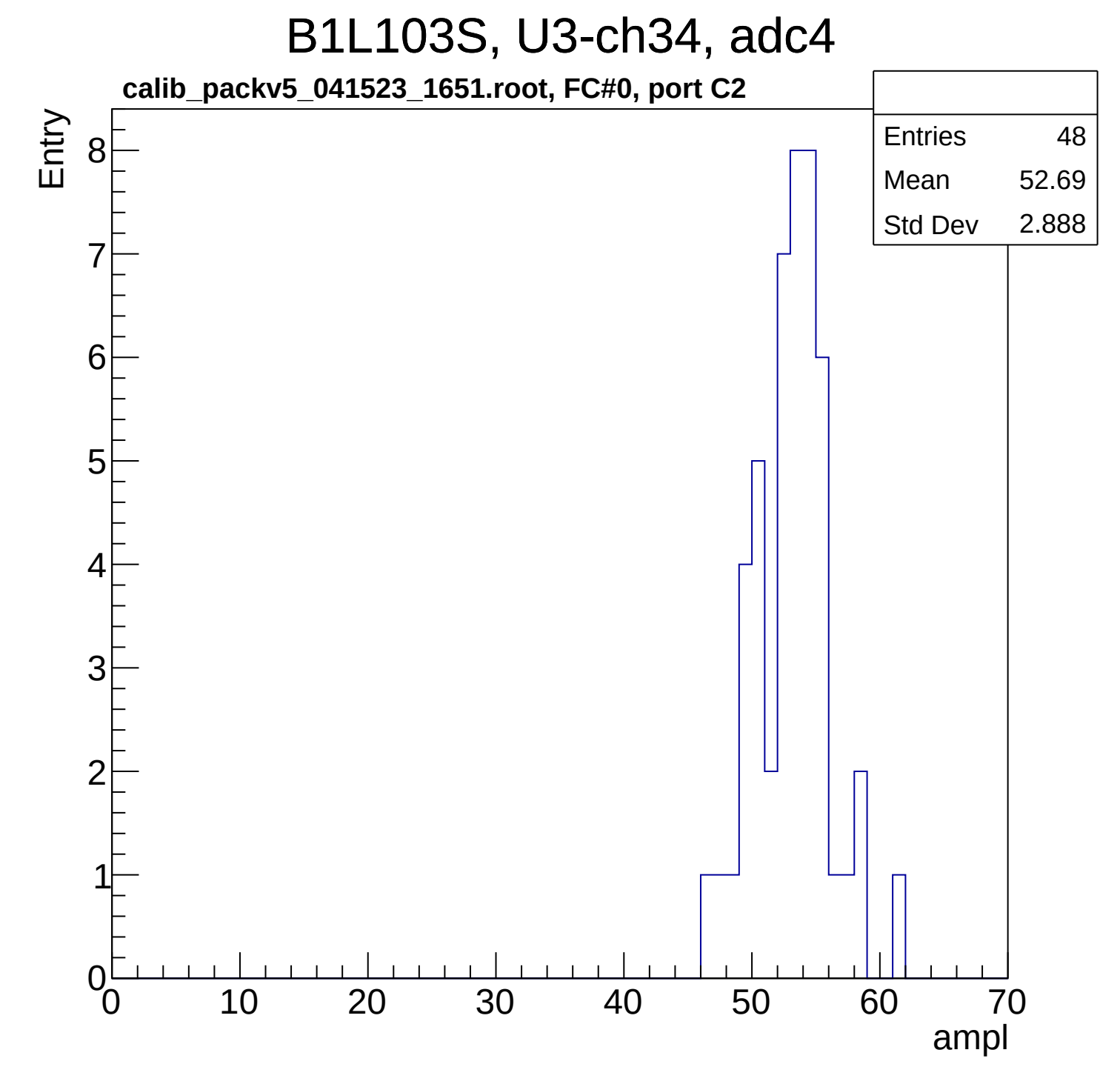
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch34, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 52.69
Std Dev 2.888
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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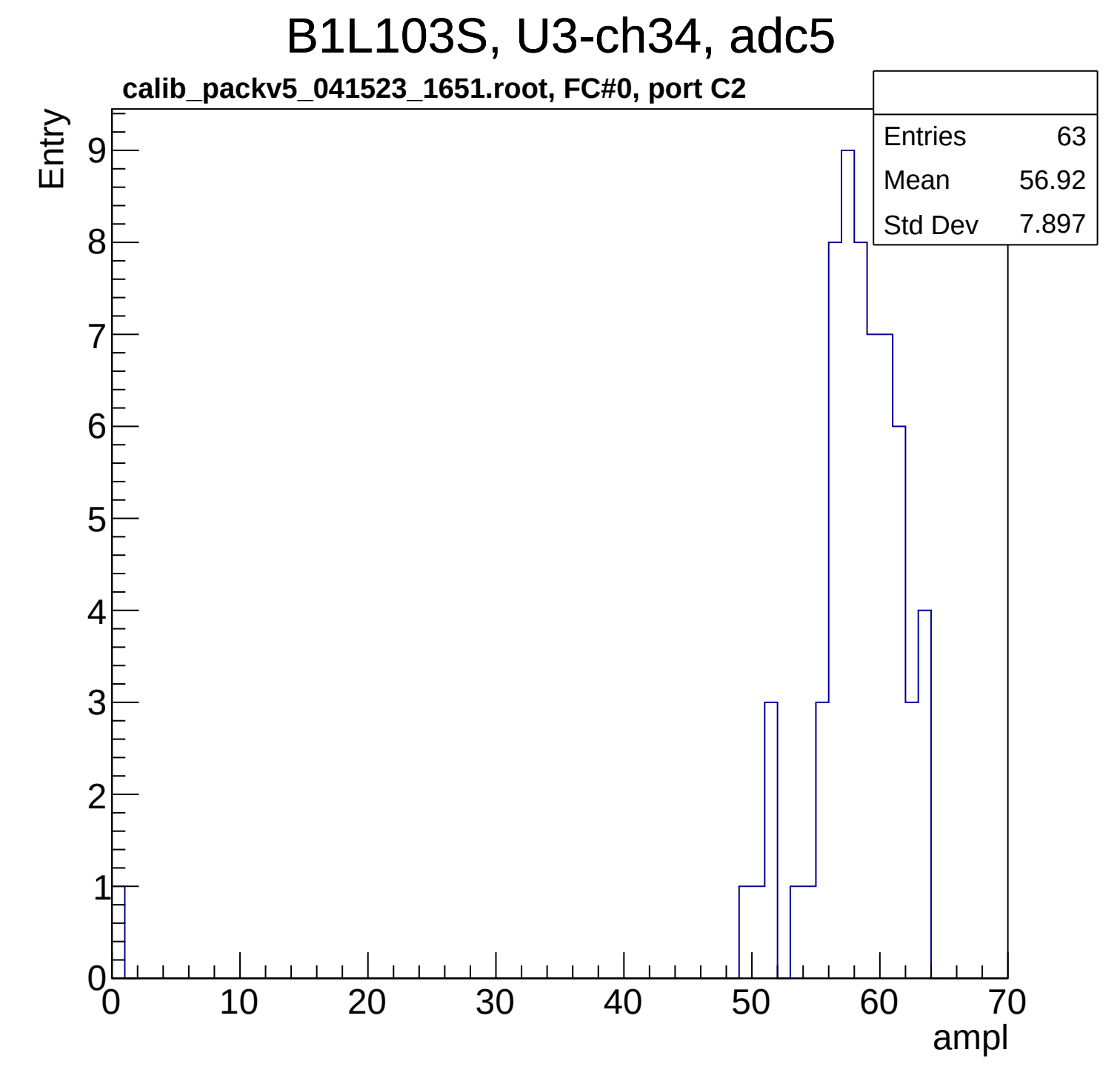
B1L103S, U3-ch34, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 56.92
Std Dev 7.897
Entry
ampl
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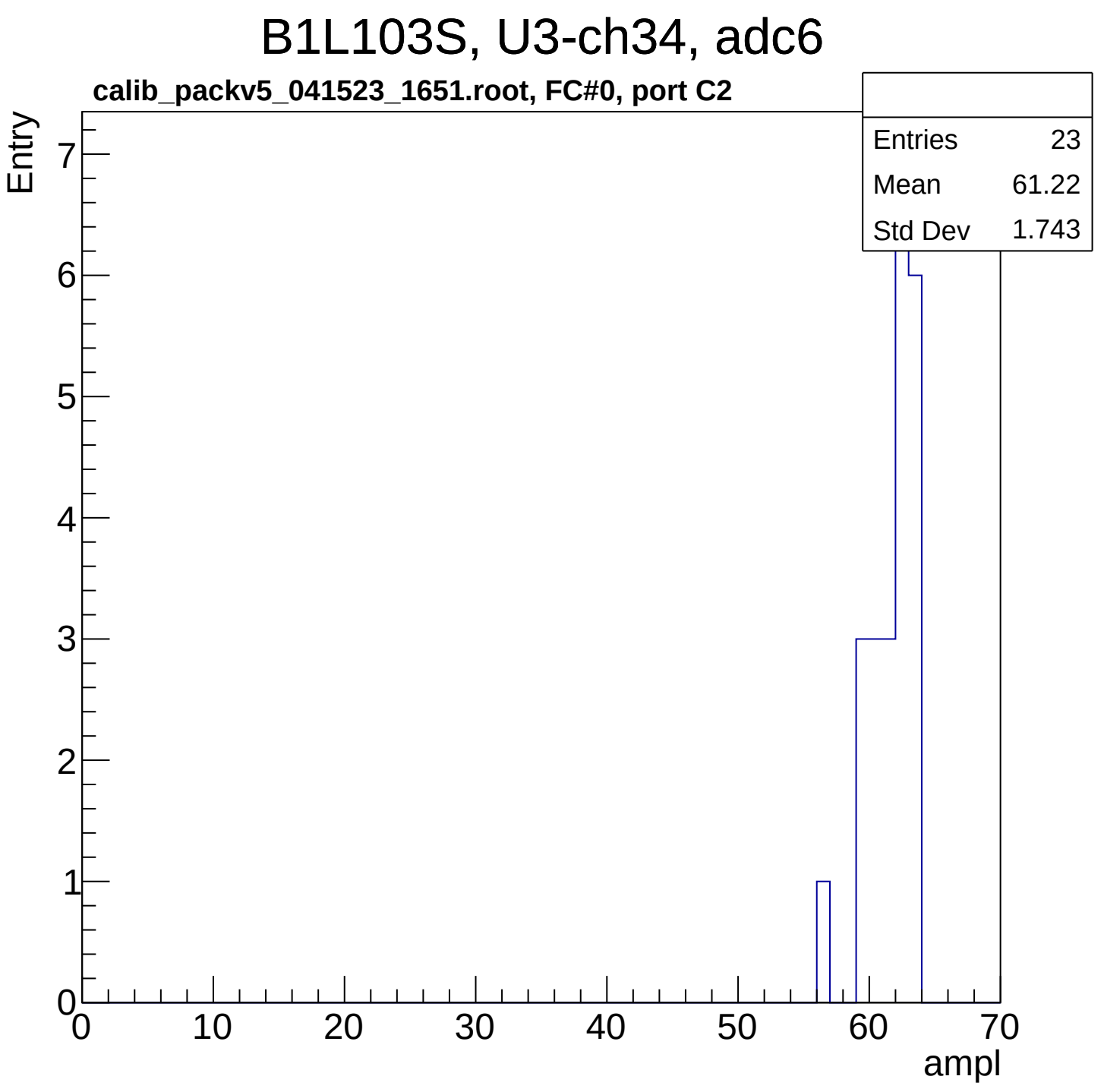
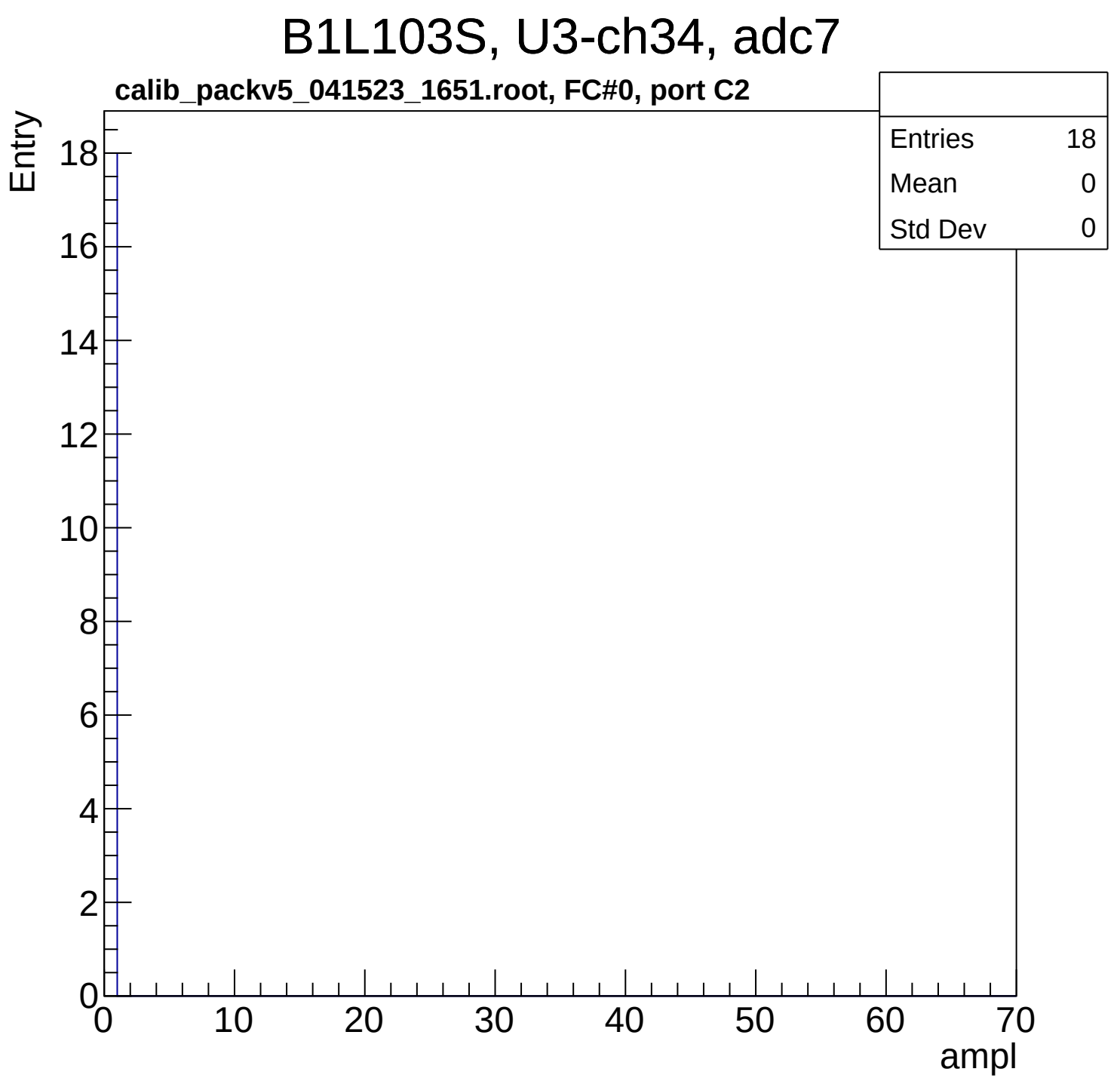
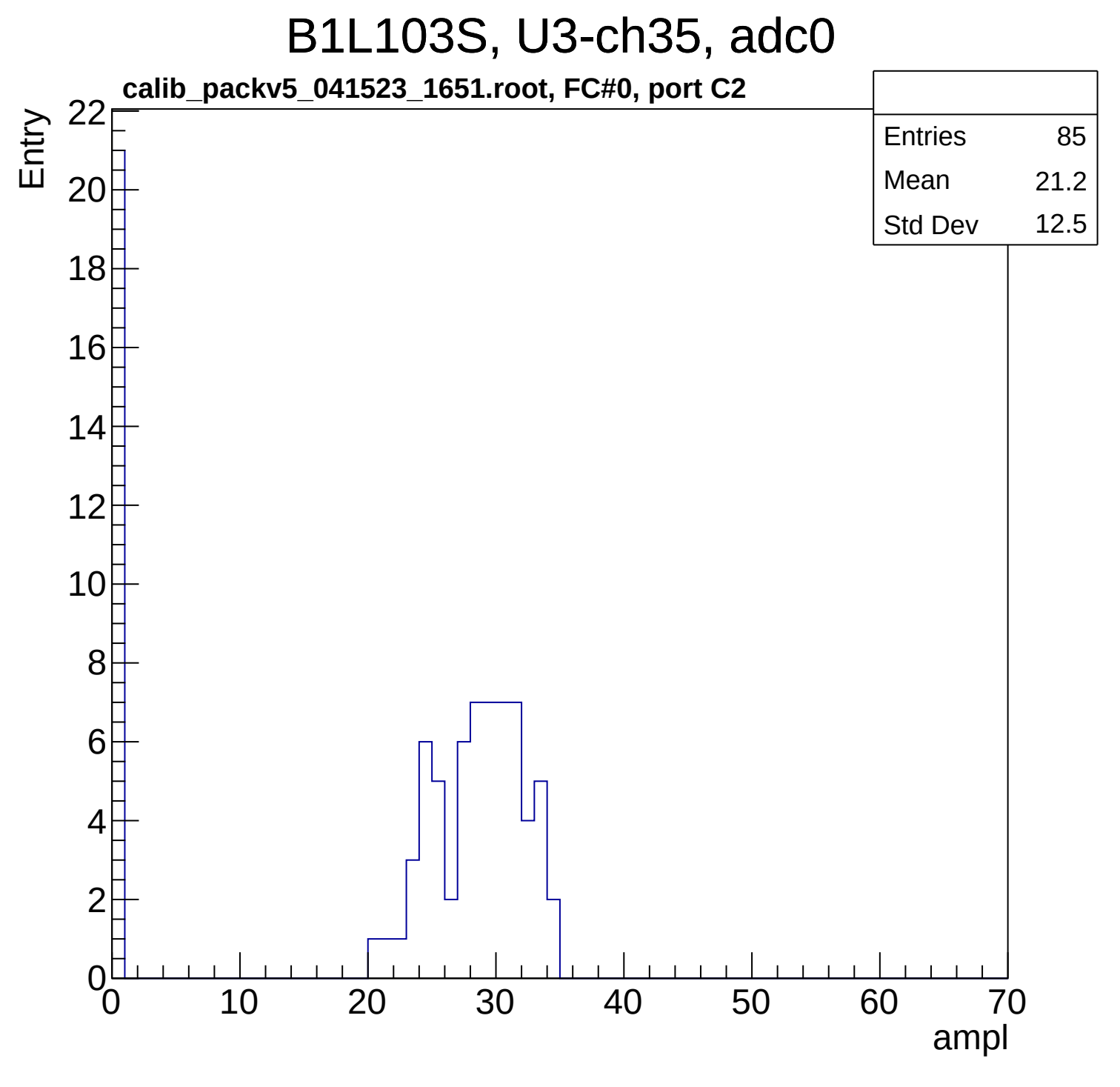
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch34, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 61.22
Std Dev 1.743
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch34, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch35, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 21.2
Std Dev 12.5
Entry
ampl
0
2
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8
10
12
14
16
18
20
22
0
10
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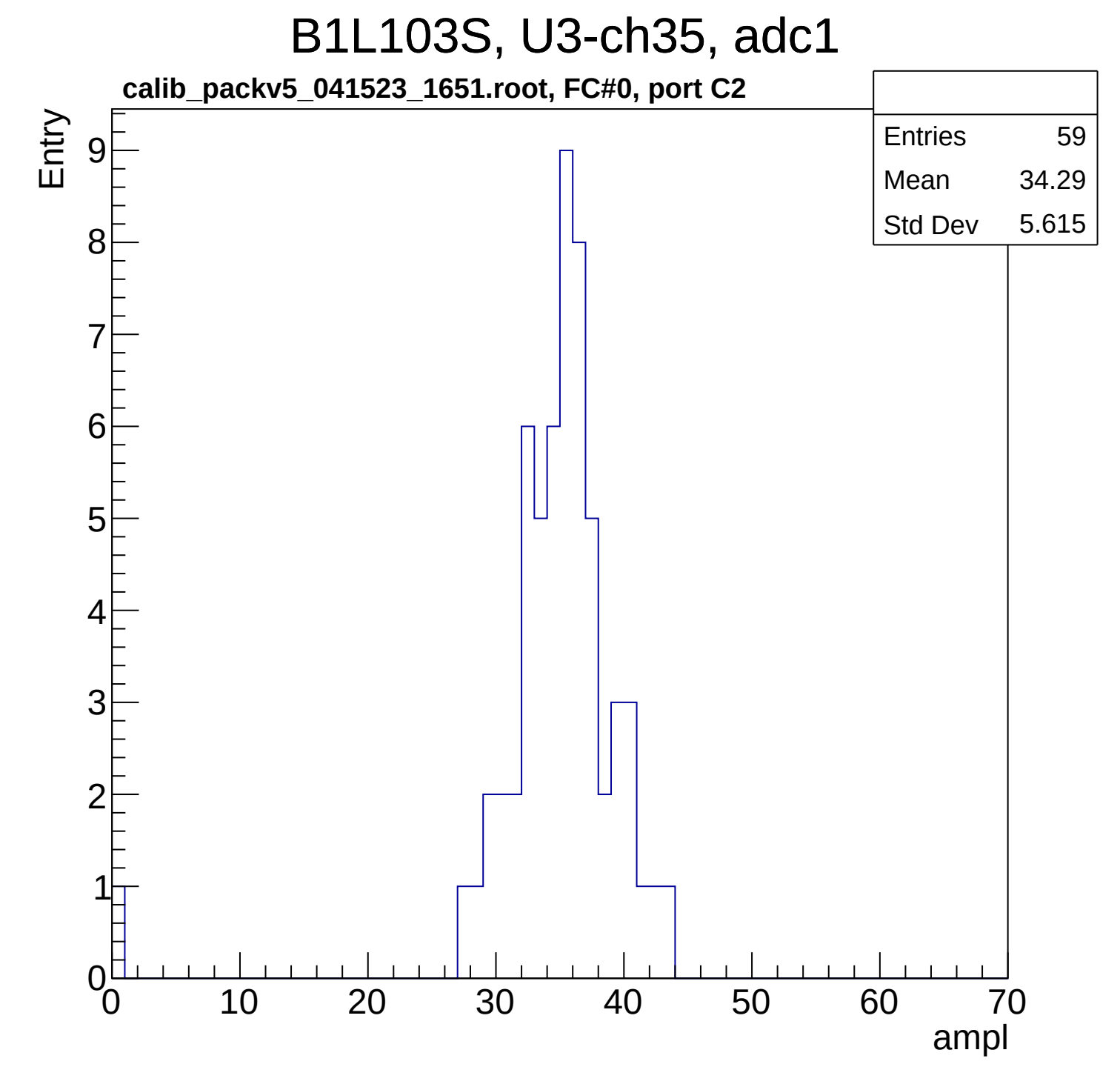
40
50
60
70


B1L103S, U3-ch35, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 34.29
Std Dev 5.615
Entry
ampl
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3
4
5
6
7
8
9
0
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40
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60
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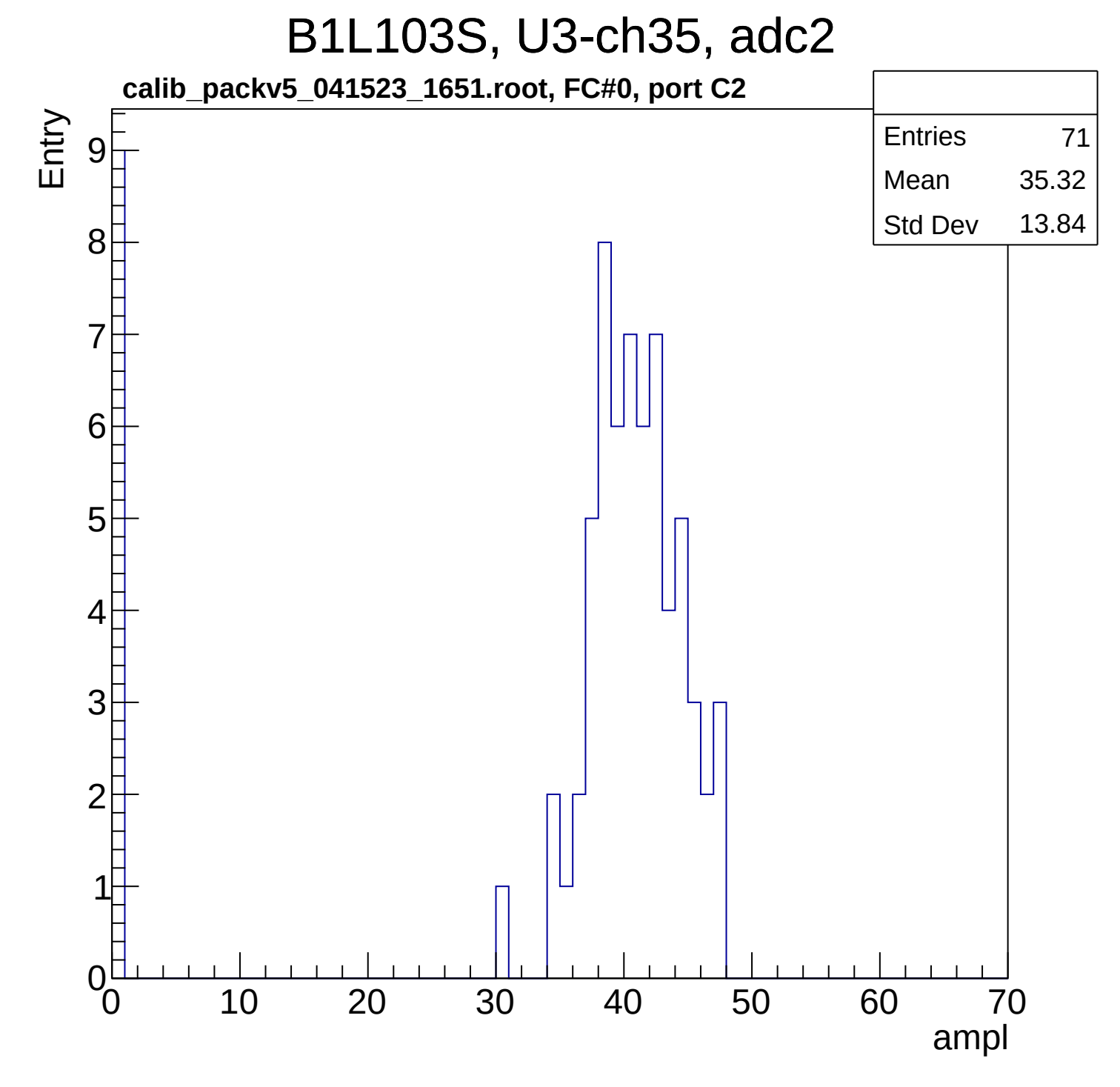
B1L103S, U3-ch35, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 35.32
Std Dev 13.84
Entry
ampl
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2
3
4
5
6
7
8
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0
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30
40
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60
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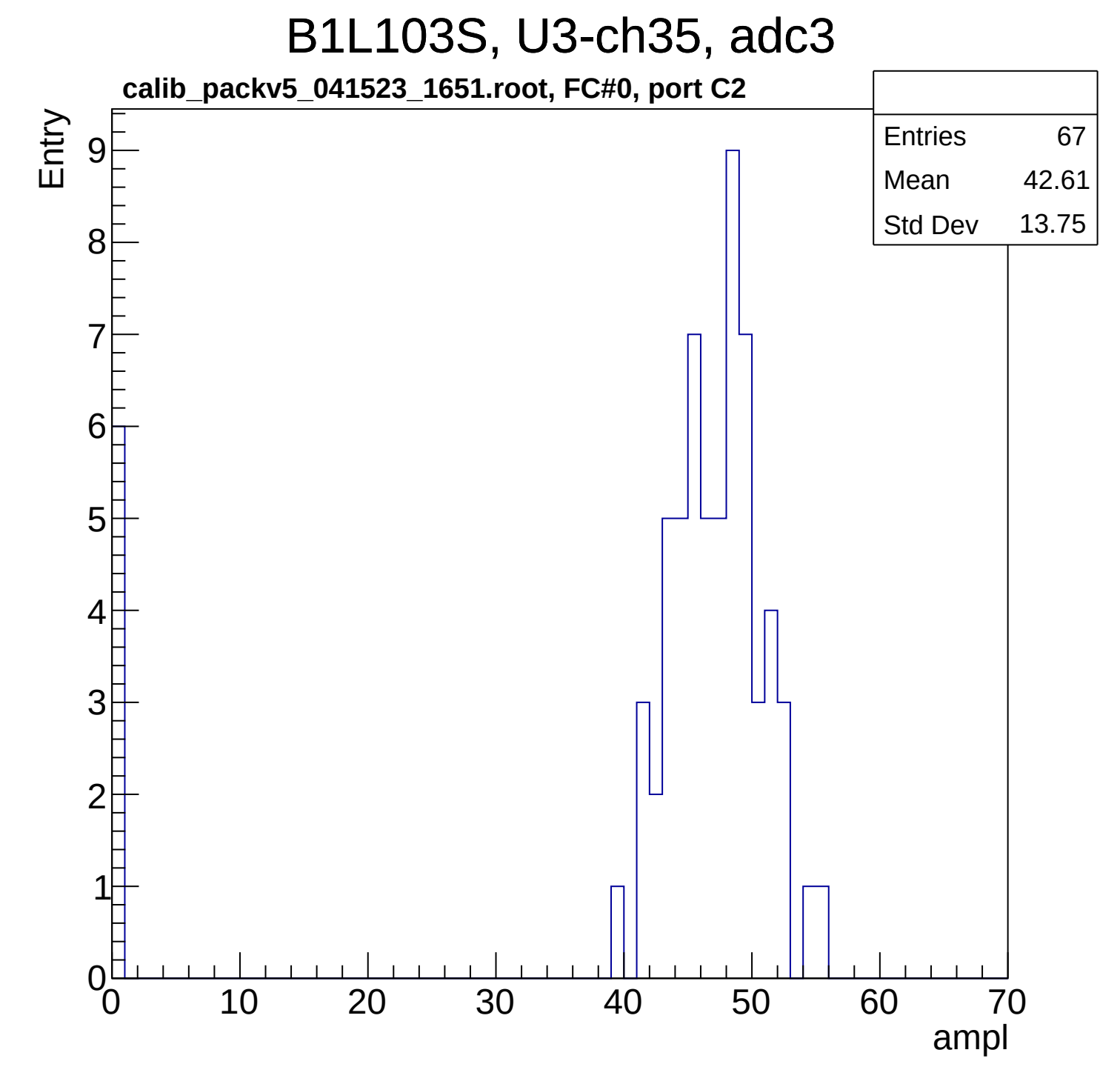
B1L103S, U3-ch35, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 42.61
Std Dev 13.75
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
50
60
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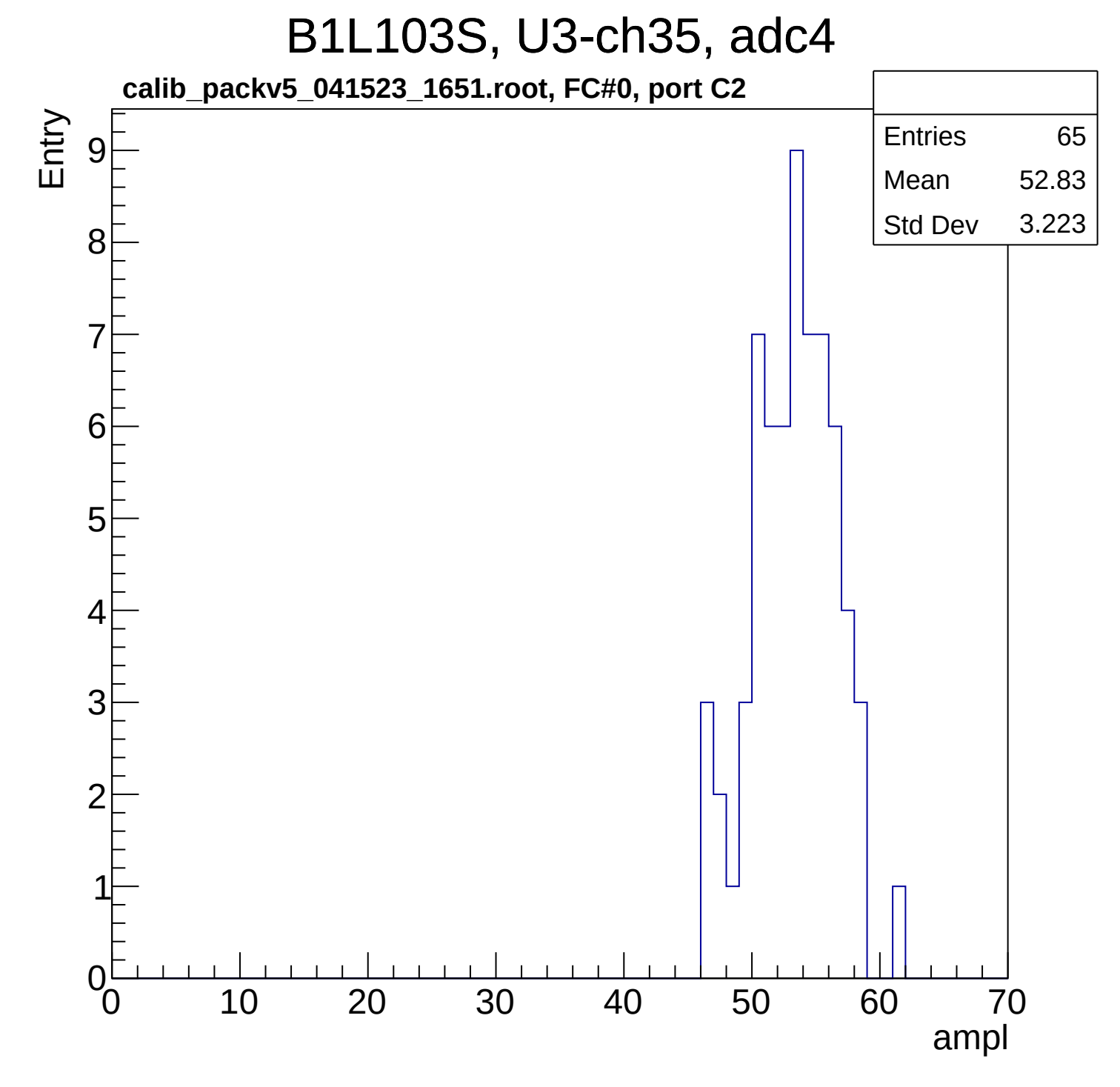
B1L103S, U3-ch35, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 52.83
Std Dev 3.223
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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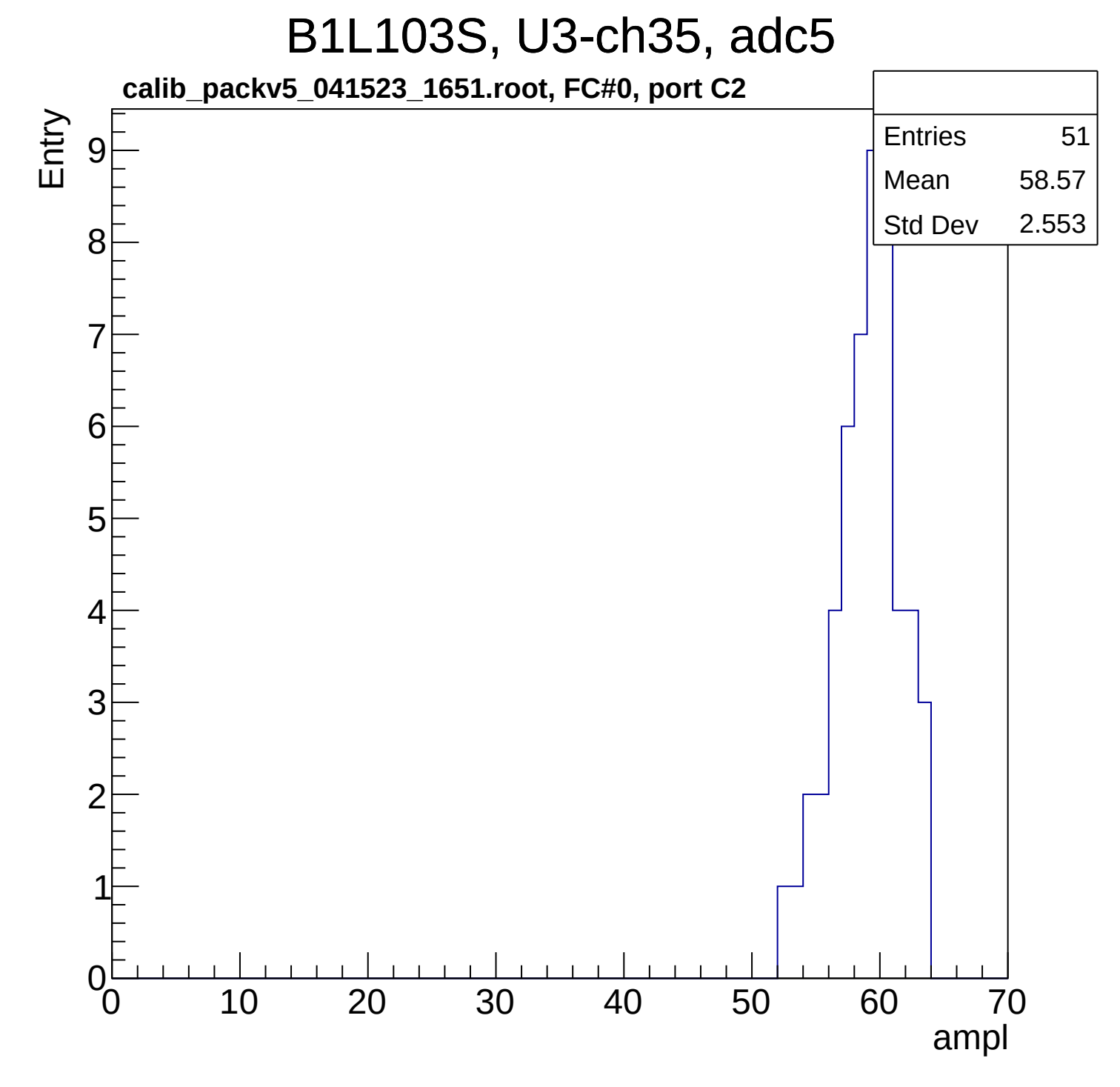
B1L103S, U3-ch35, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 58.57
Std Dev 2.553
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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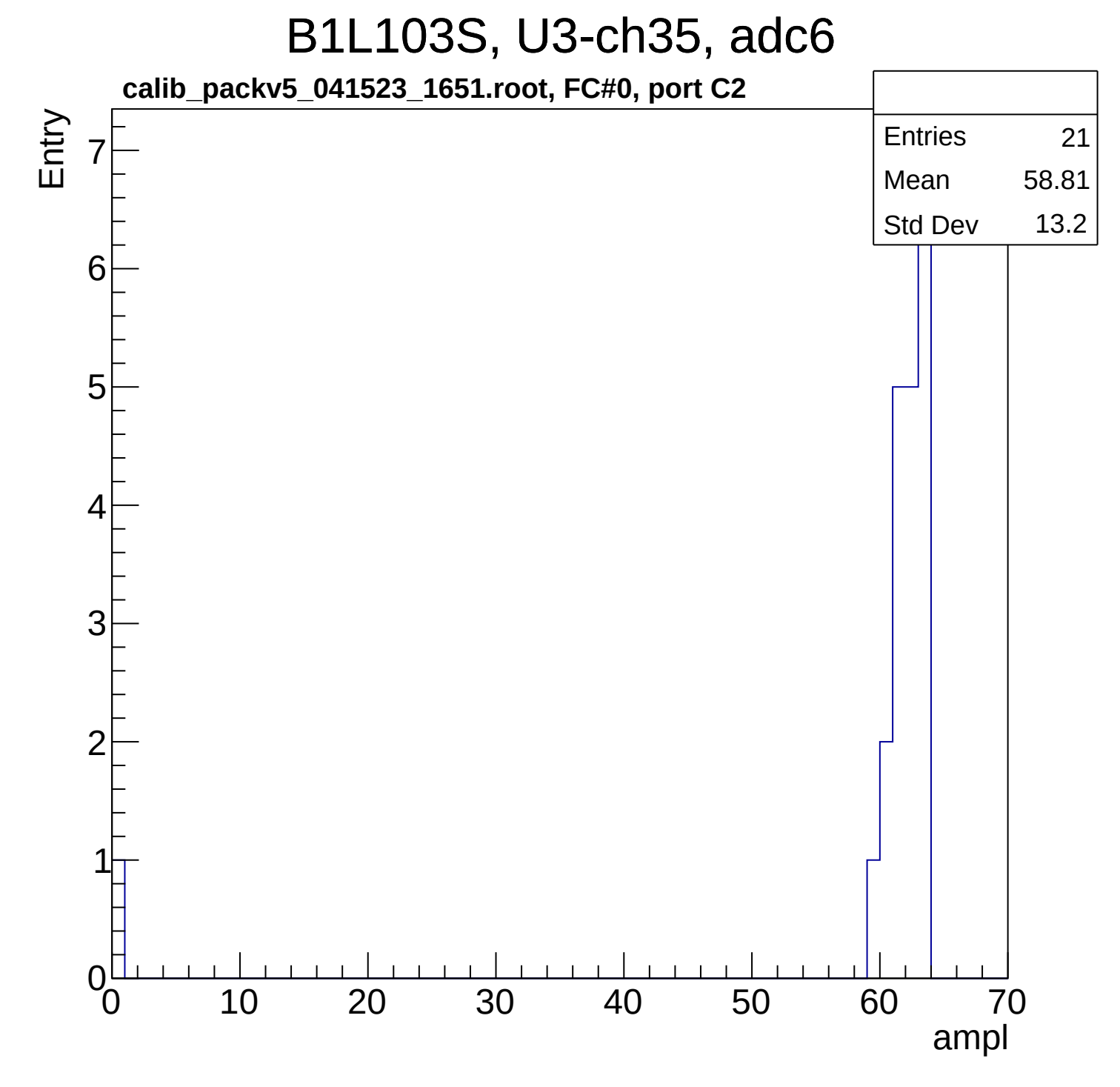
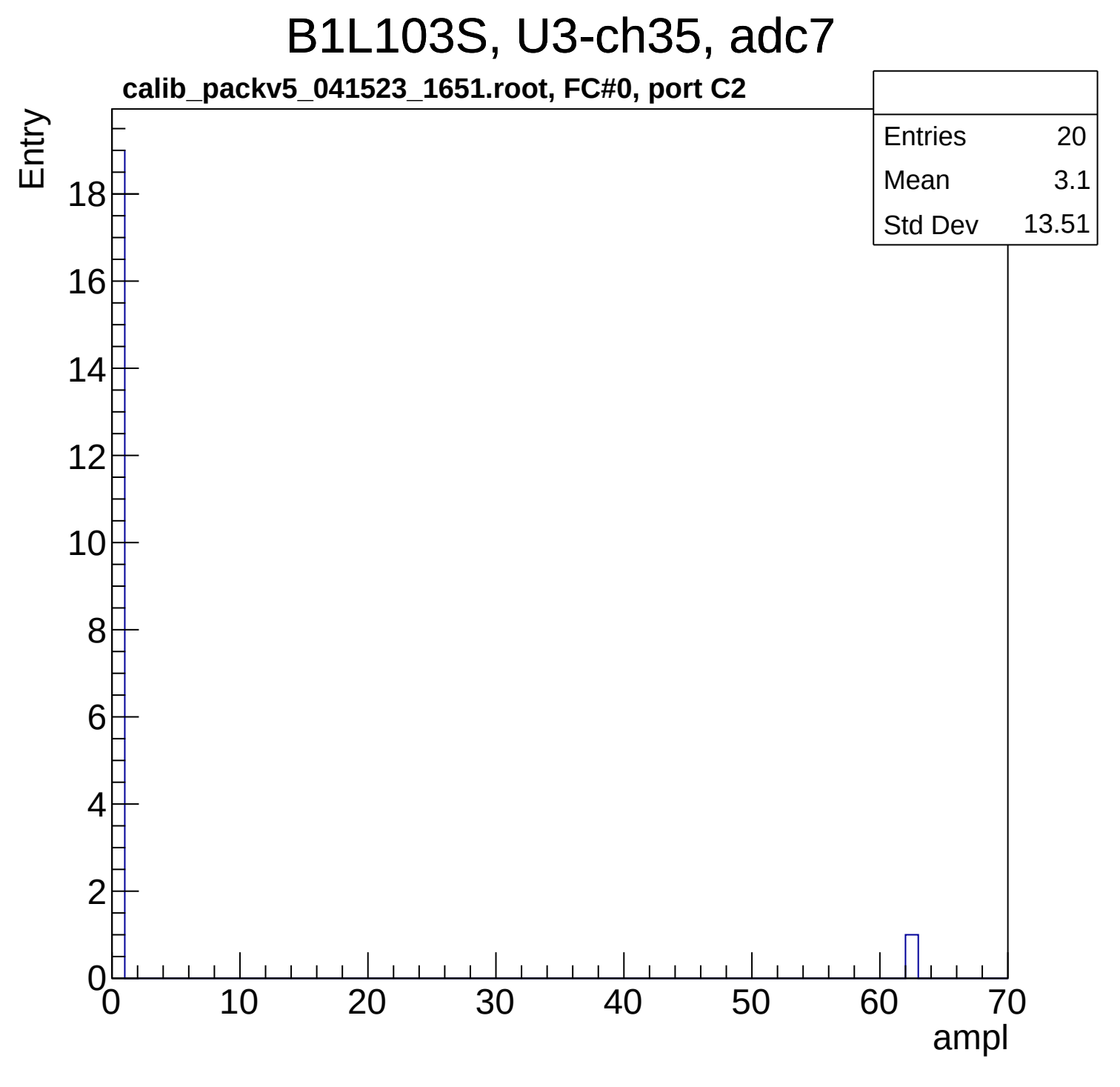
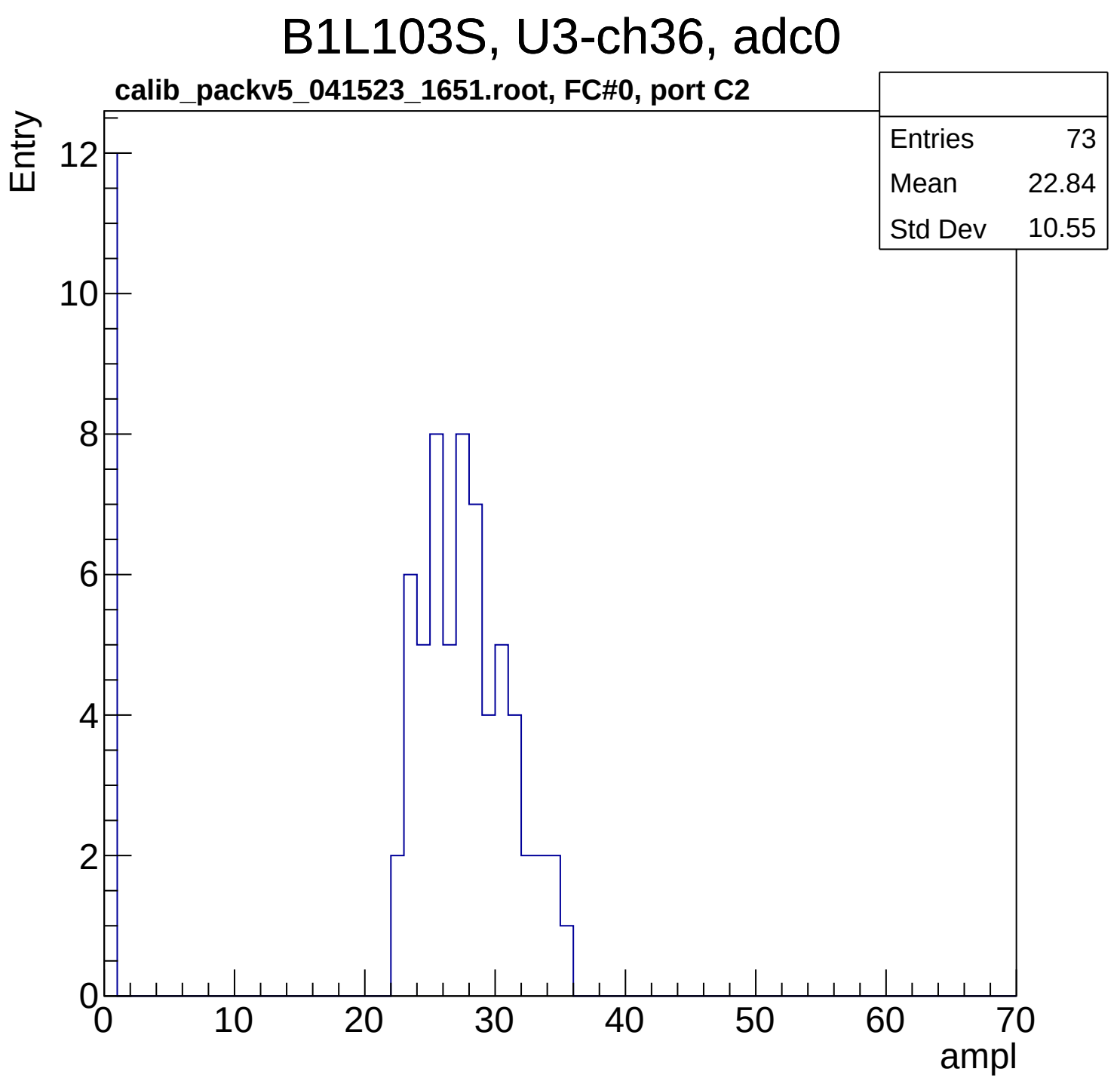
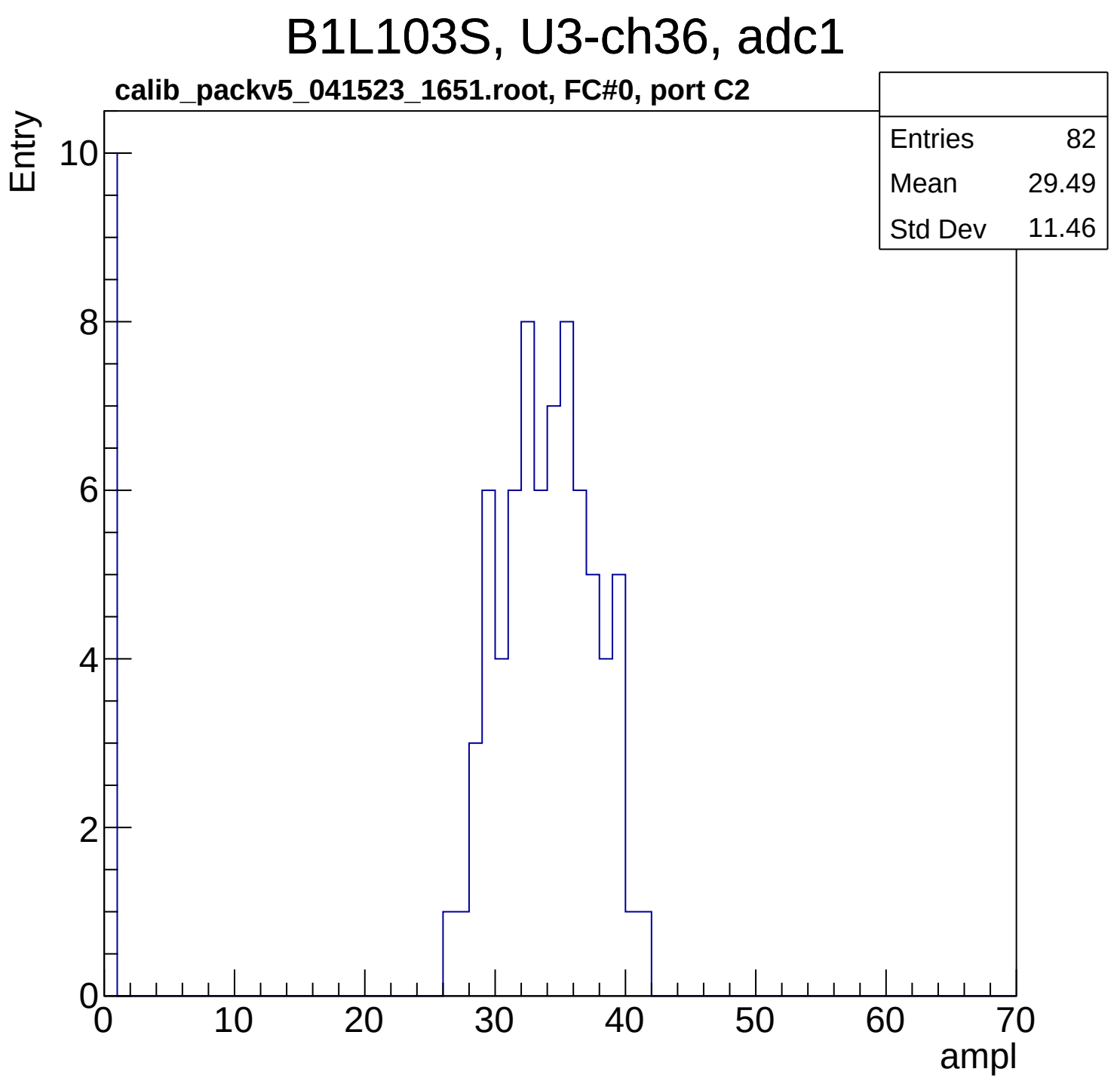
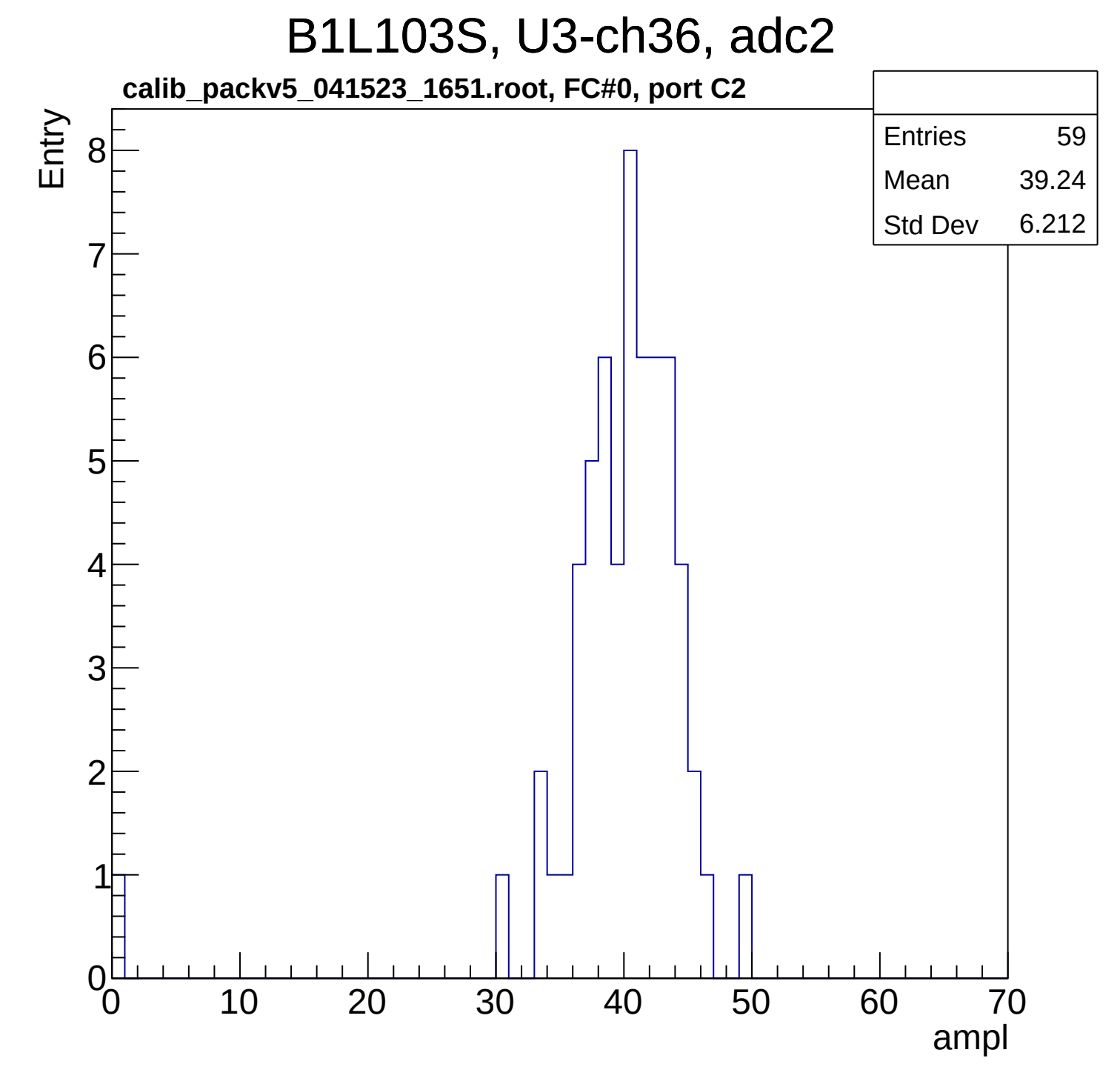

B1L103S, U3-ch35, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 58.81
Std Dev 13.2
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch35, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch36, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 22.84
Std Dev 10.55
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch36, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 29.49
Std Dev 11.46
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch36, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 39.24
Std Dev 6.212
Entry
ampl
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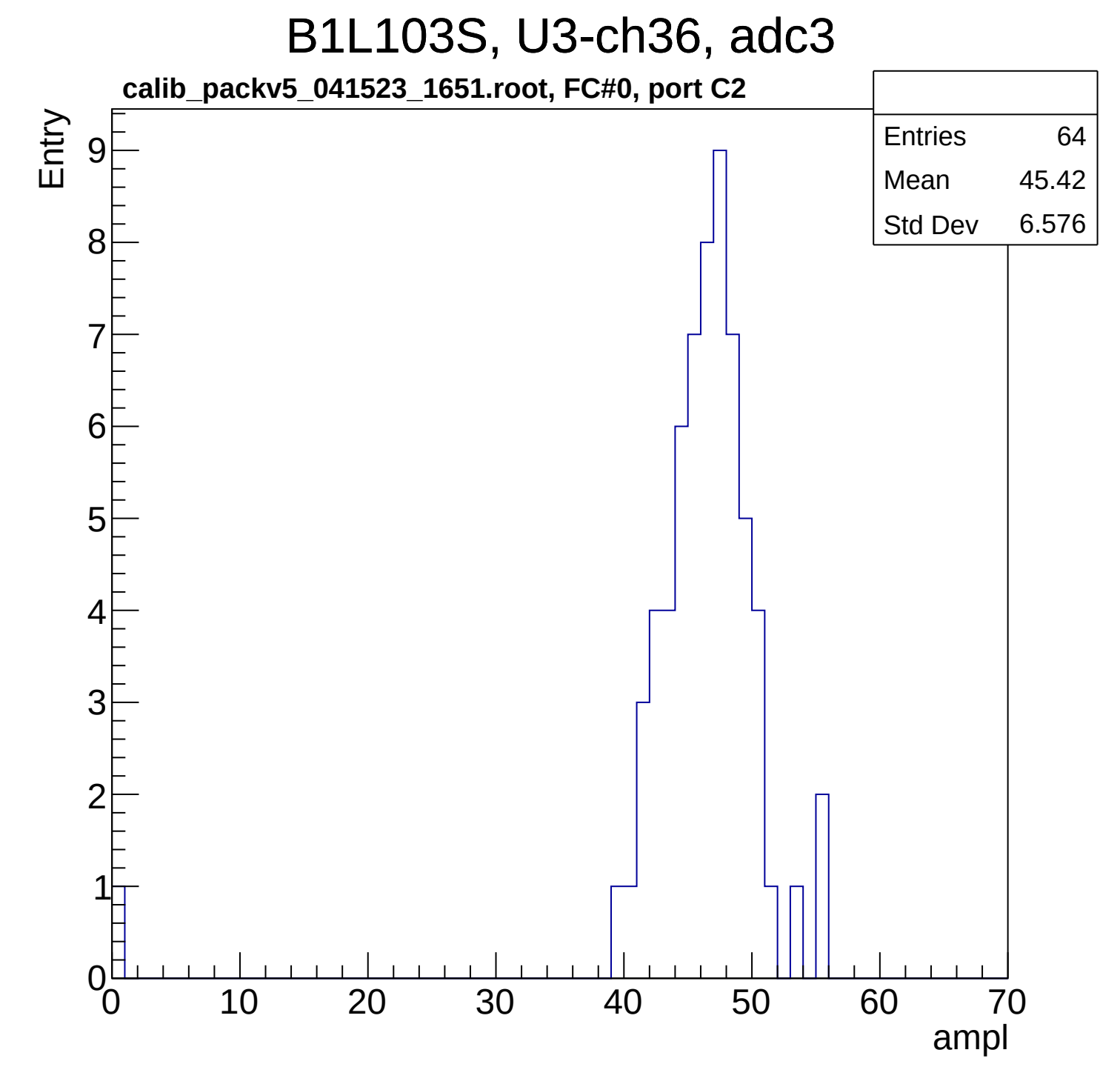
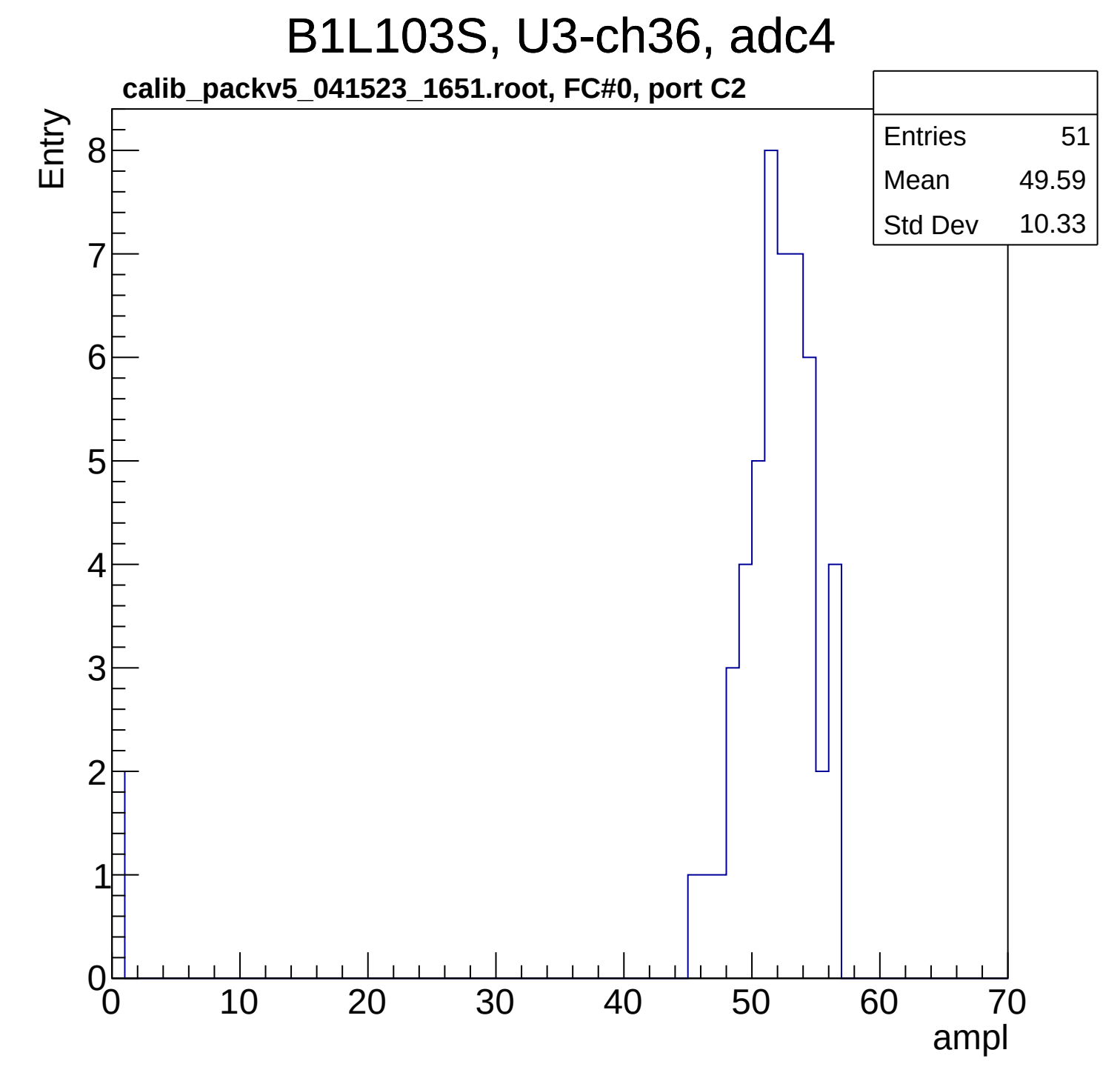
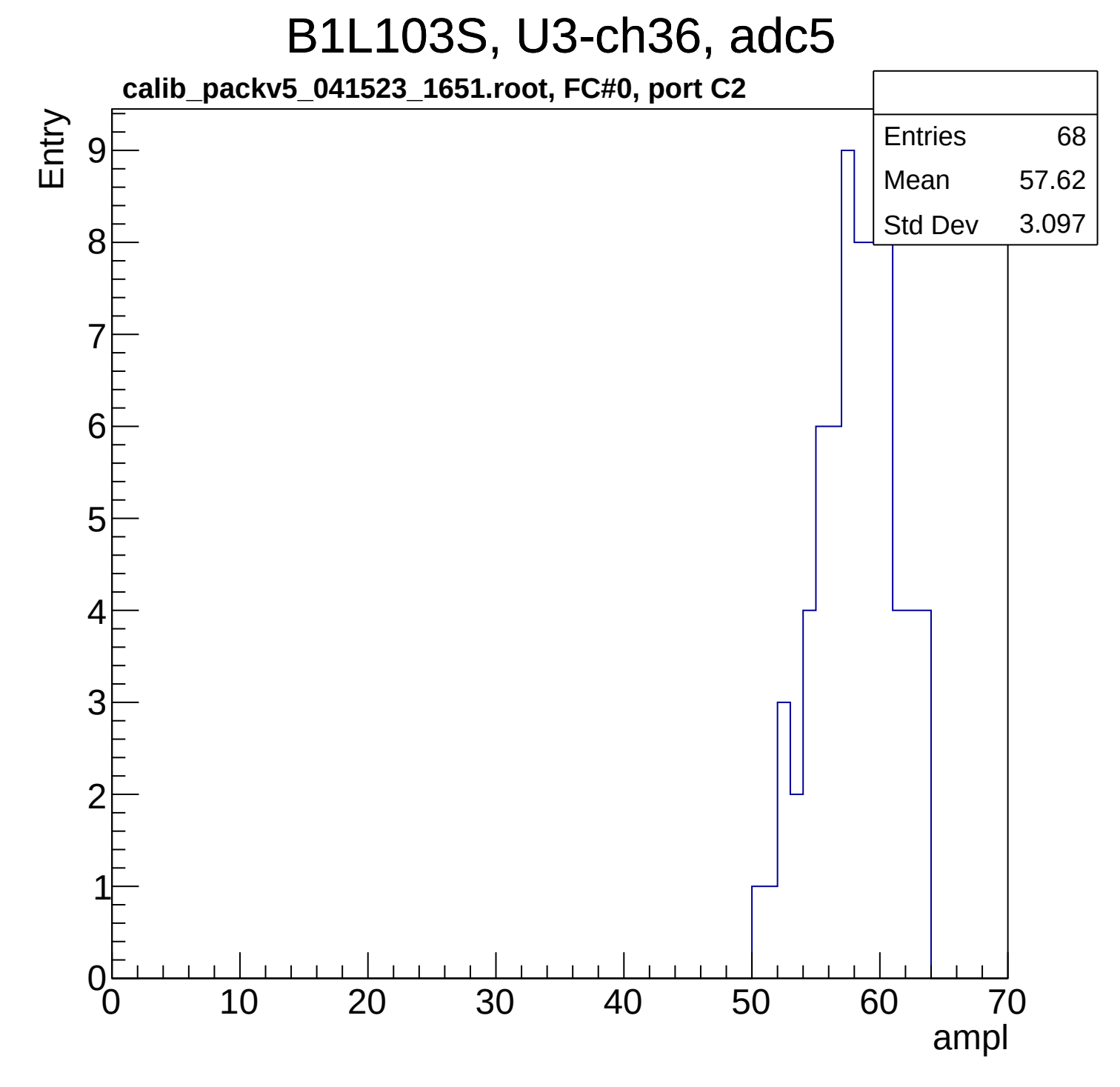
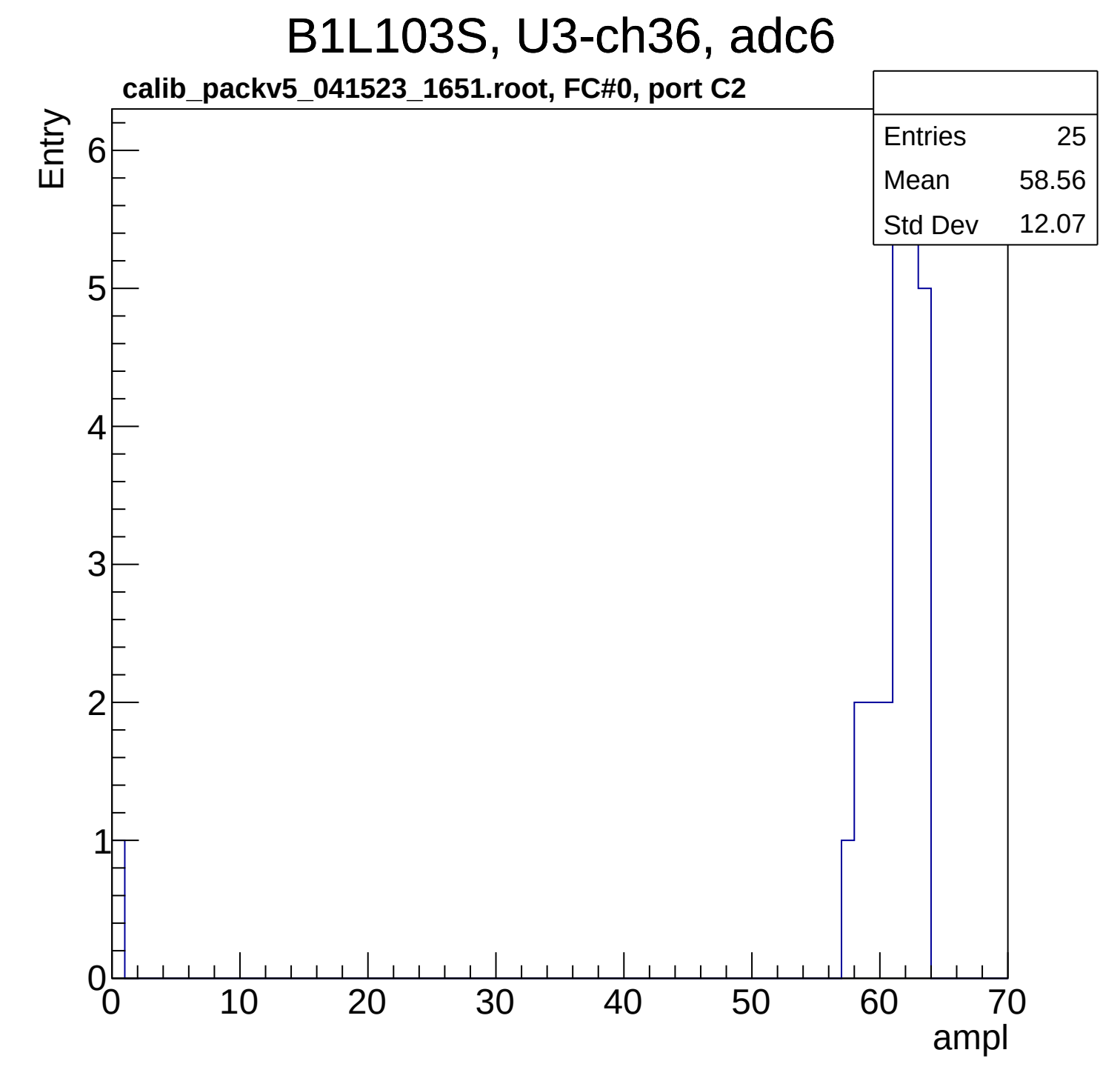
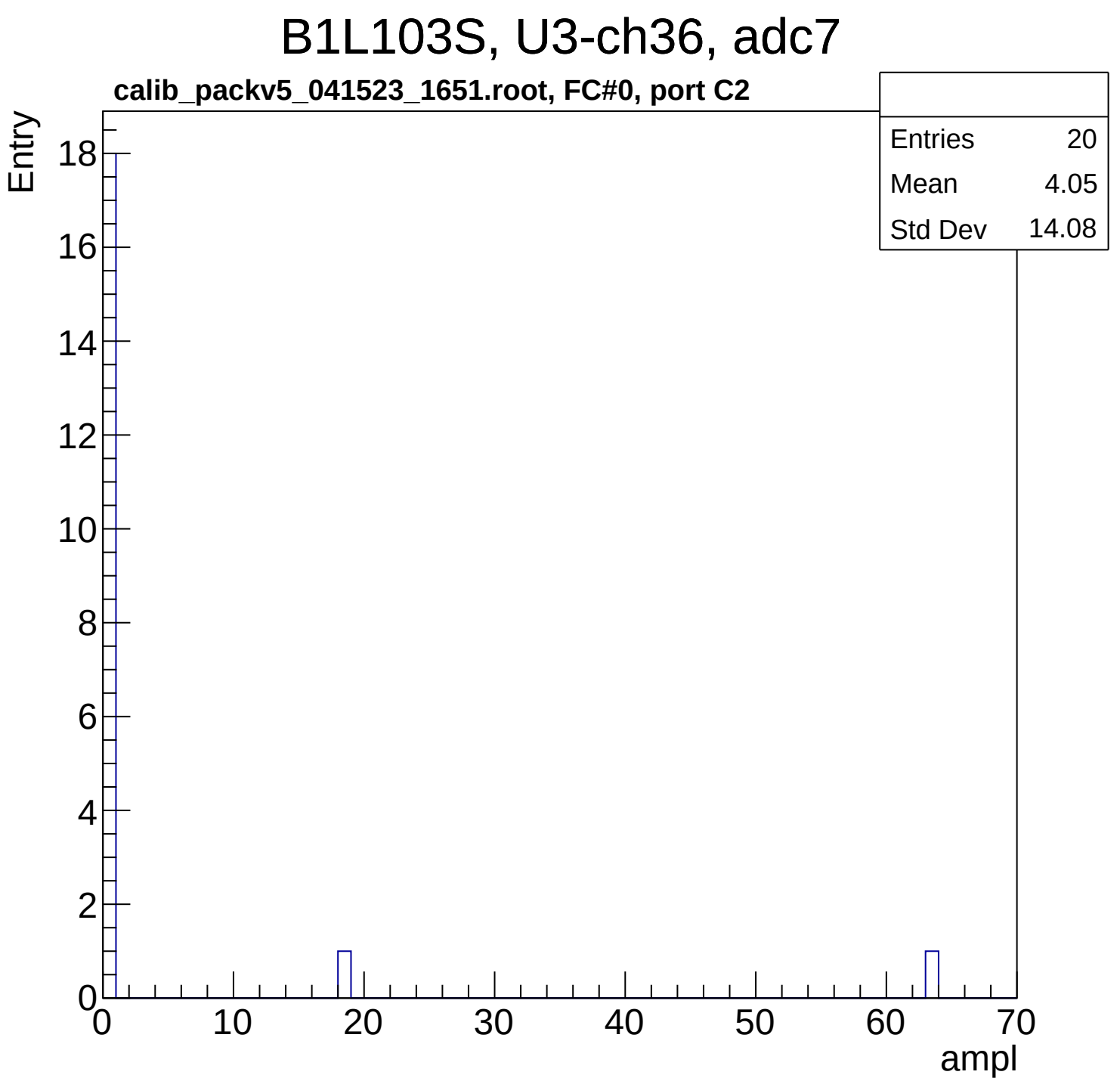
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

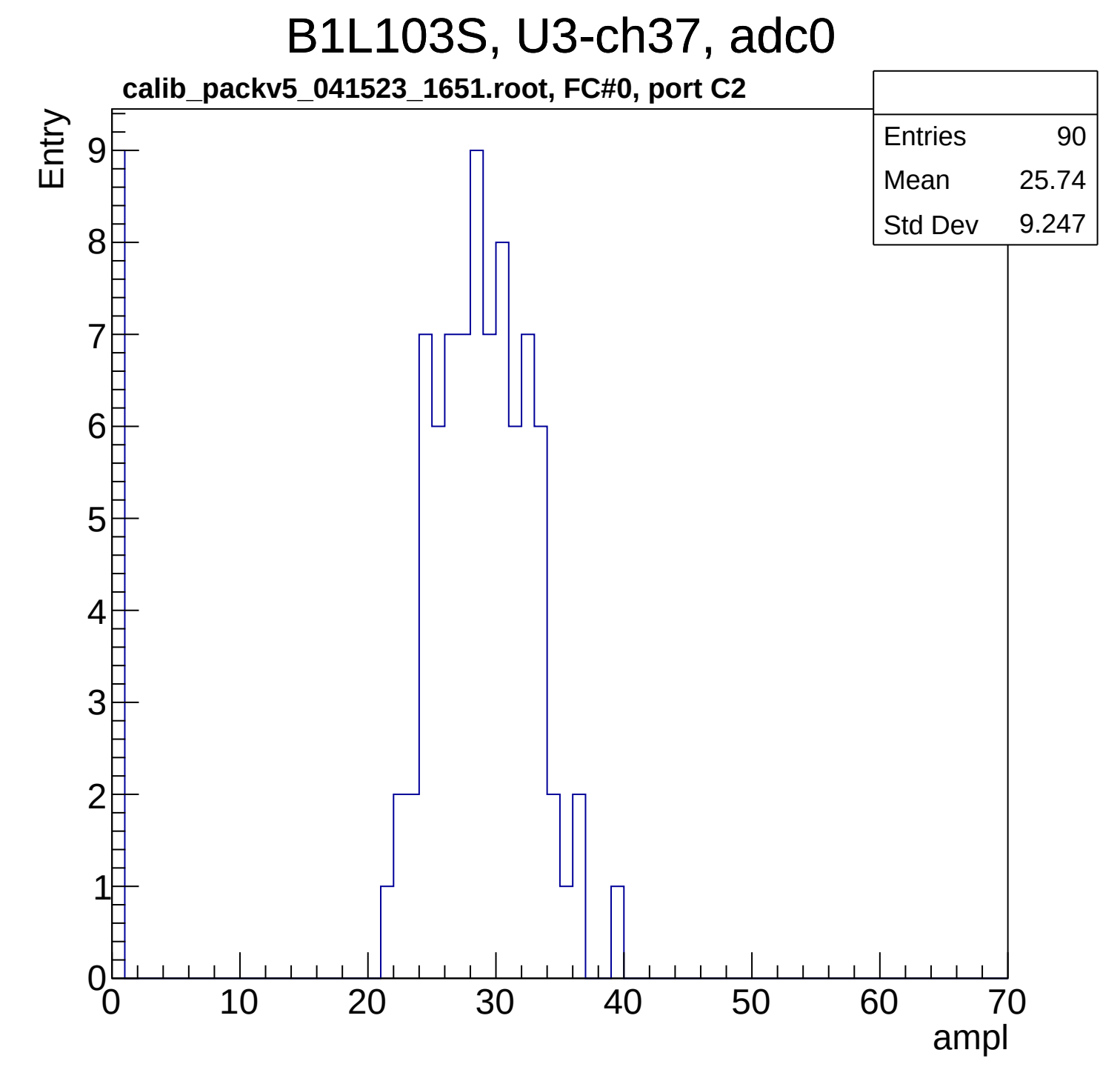

B1L103S, U3-ch36, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 45.42
Std Dev 6.576
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch36, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 49.59
Std Dev 10.33
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch36, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 57.62
Std Dev 3.097
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch36, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 58.56
Std Dev 12.07
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch36, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4.05
Std Dev 14.08
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch37, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 25.74
Std Dev 9.247
Entry
ampl
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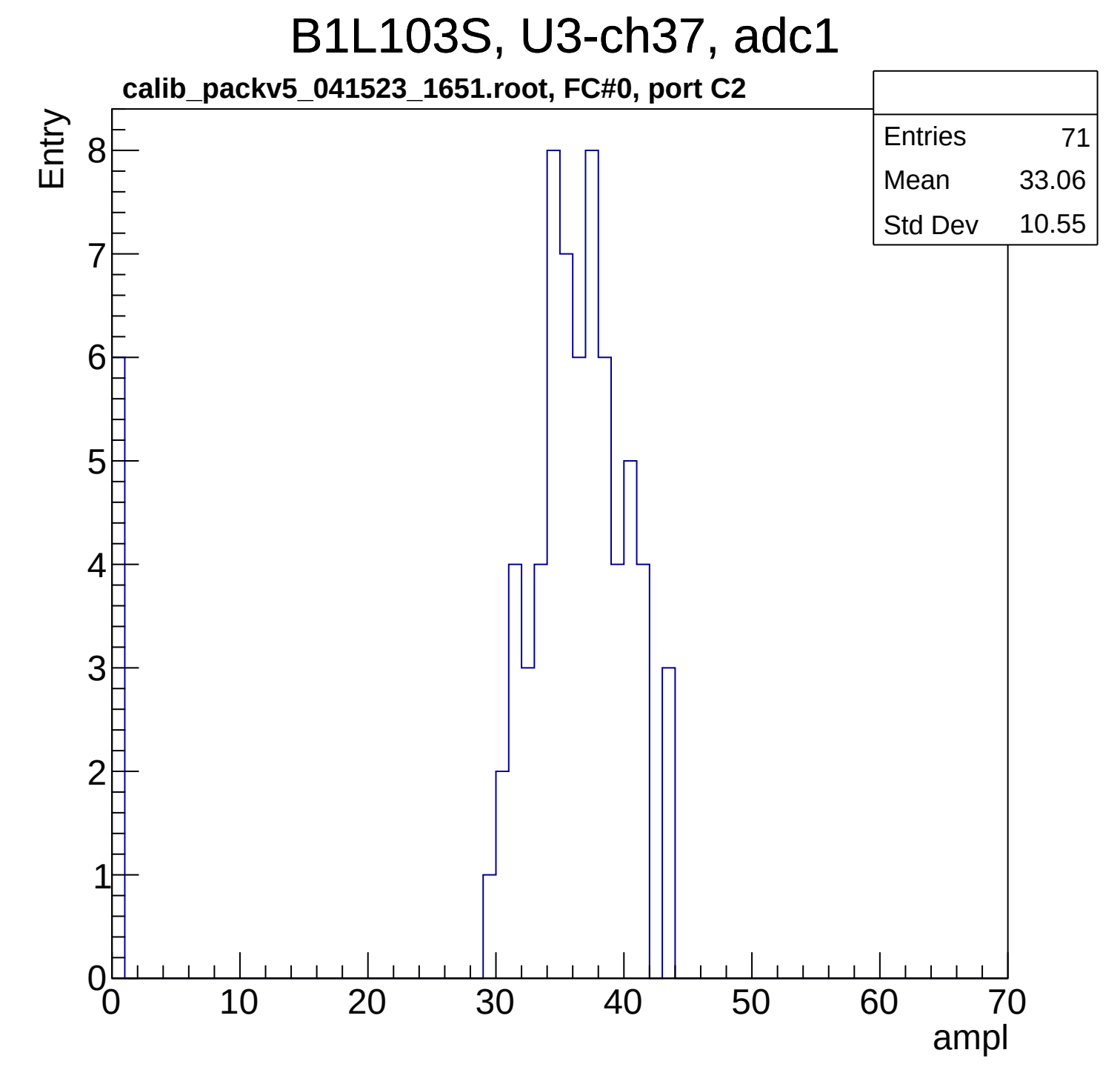
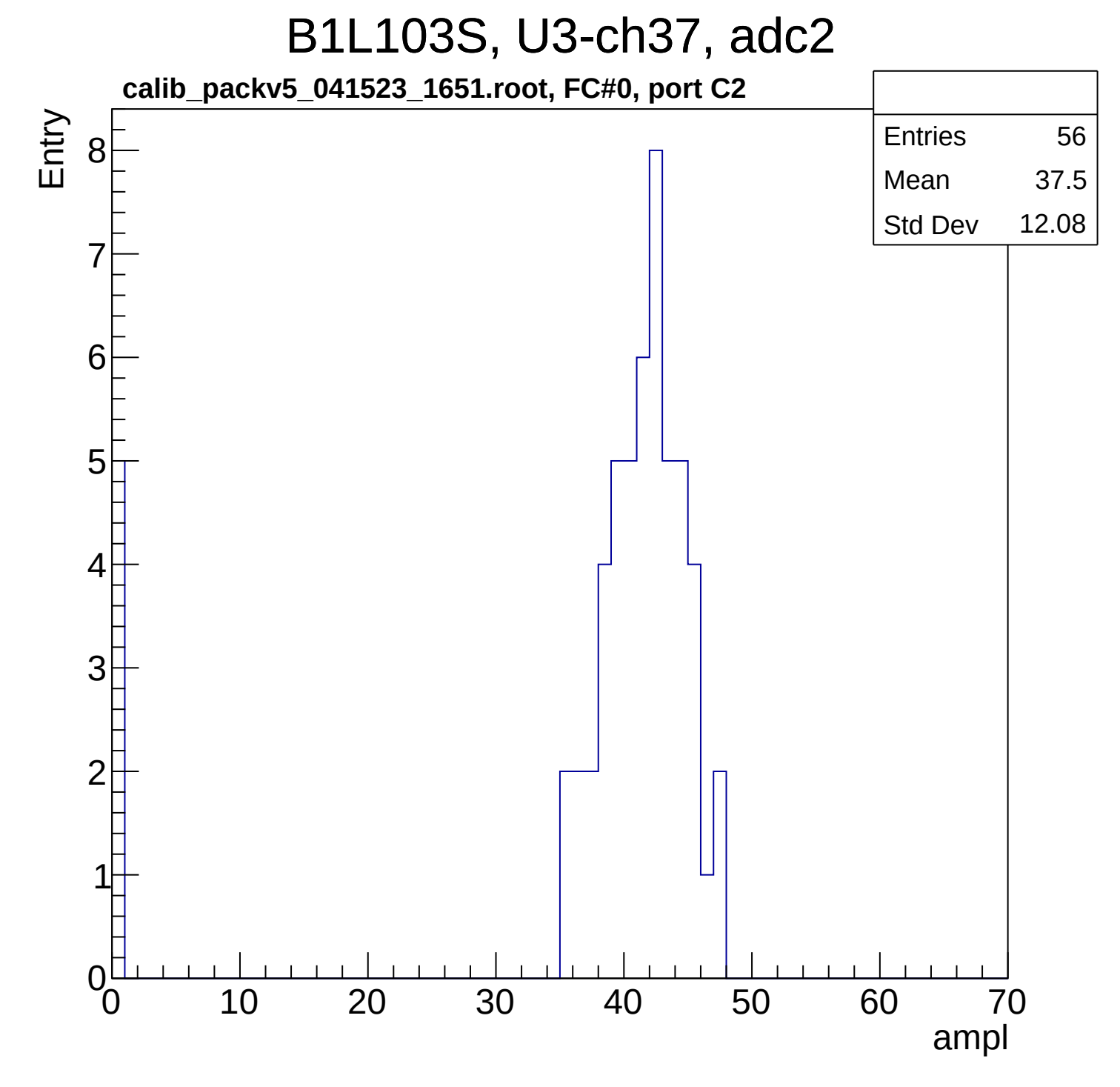
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch37, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 33.06
Std Dev 10.55
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch37, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 37.5
Std Dev 12.08
Entry
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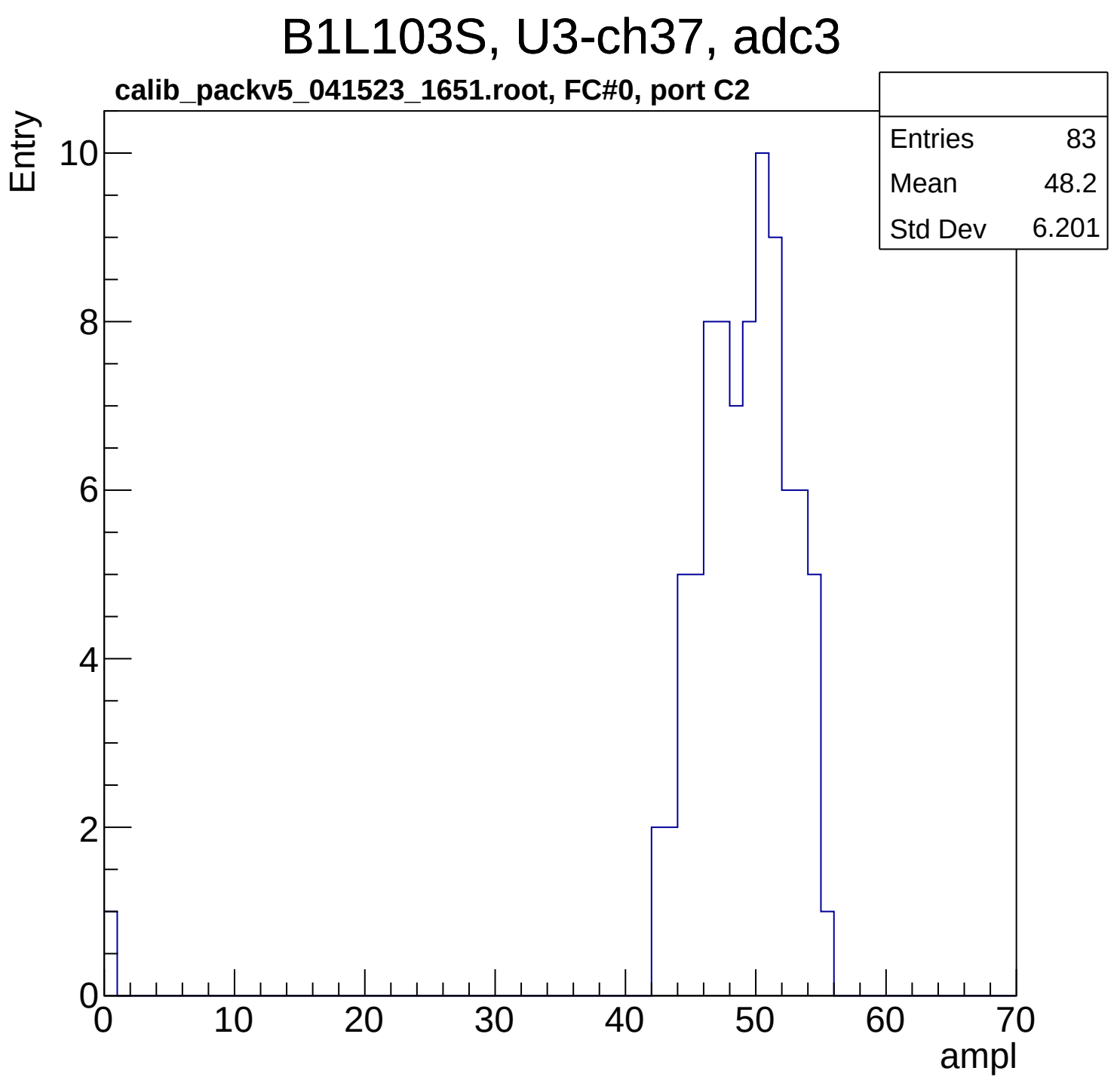
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch37, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 48.2
Std Dev 6.201
Entry
ampl
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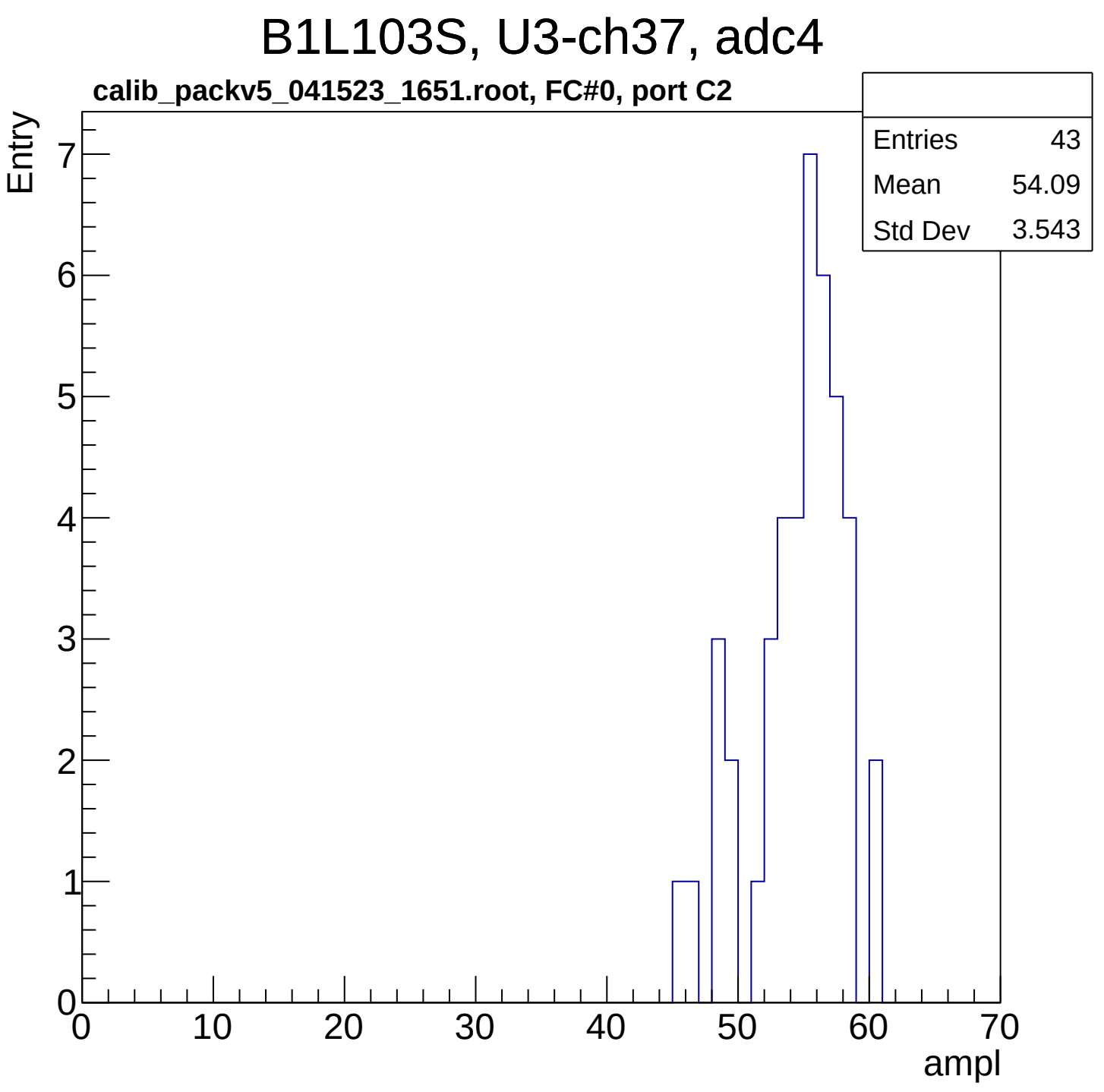
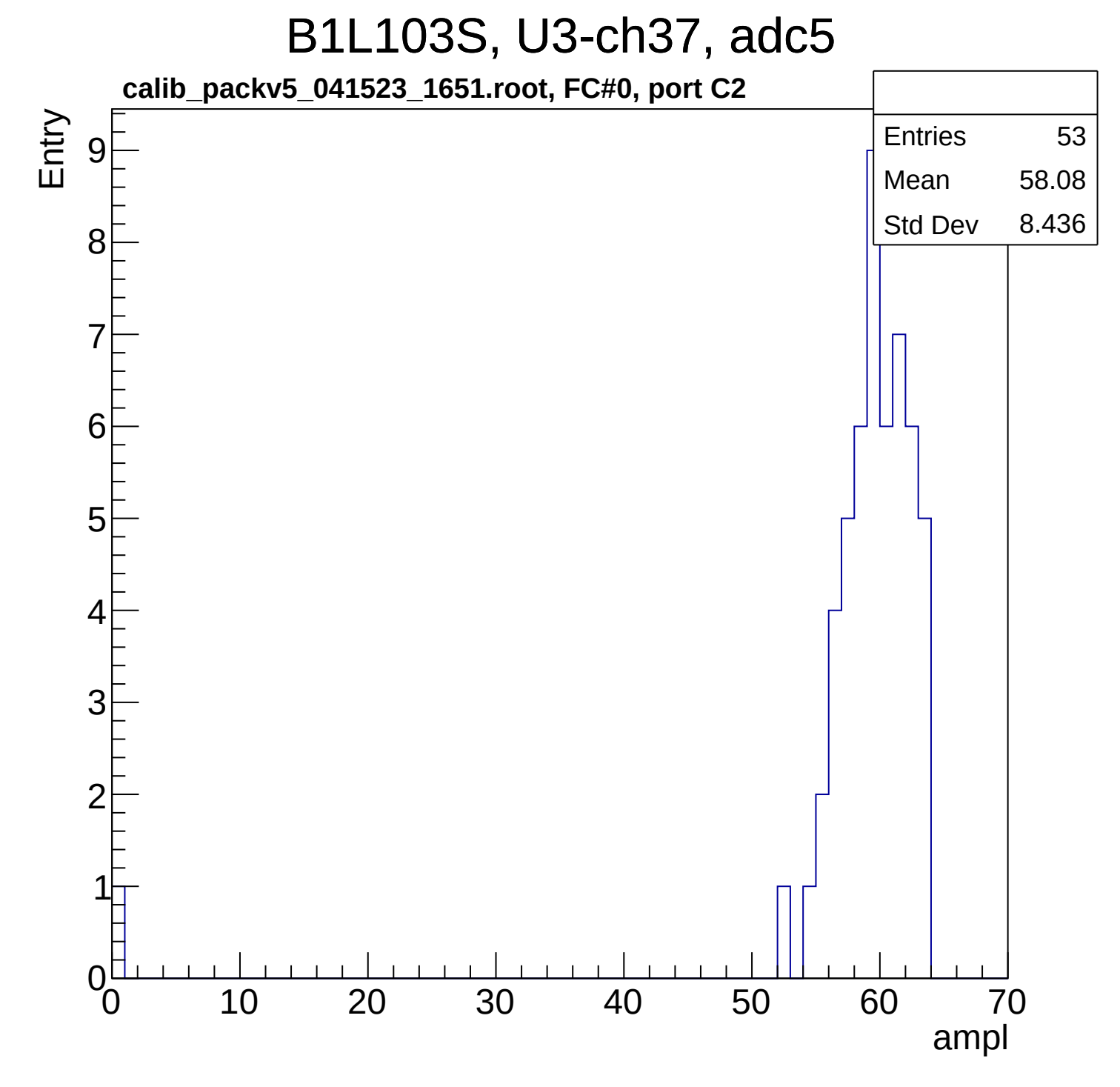
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U3-ch37, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 54.09
Std Dev 3.543
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch37, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 58.08
Std Dev 8.436
Entry
ampl
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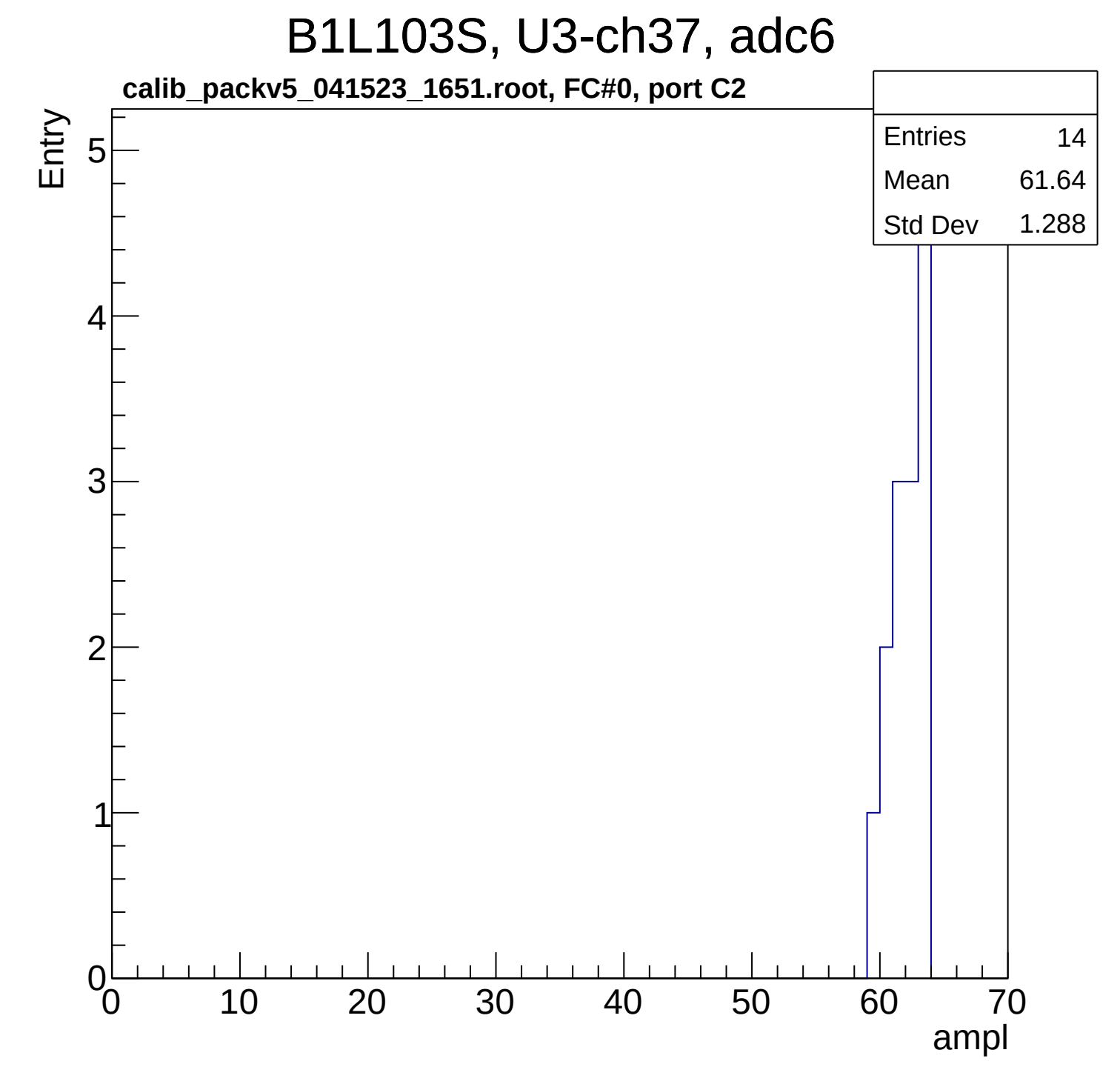
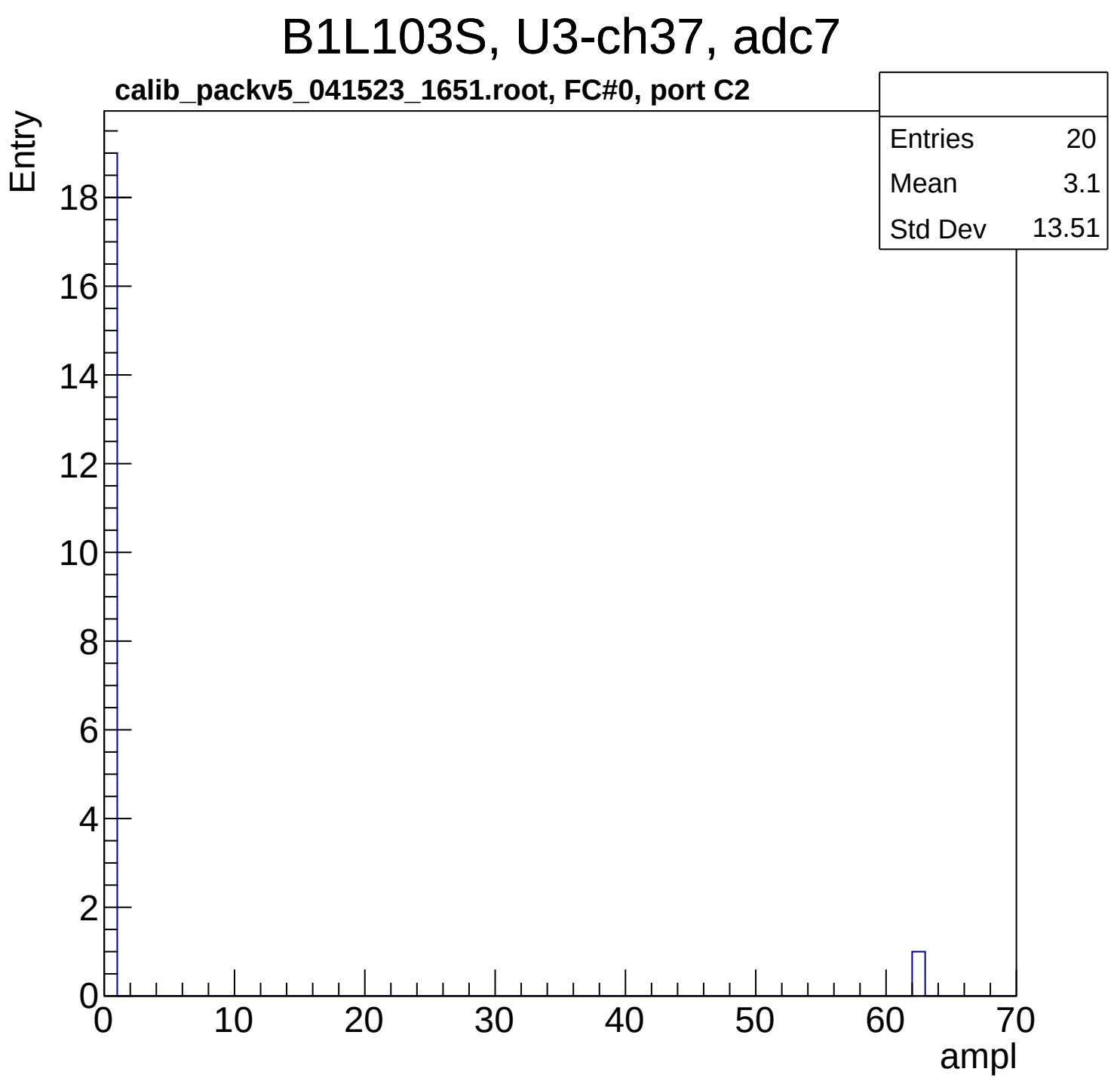
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch37, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 61.64
Std Dev 1.288
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U3-ch37, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
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4
6
8
10
12
14
16
18
0
10
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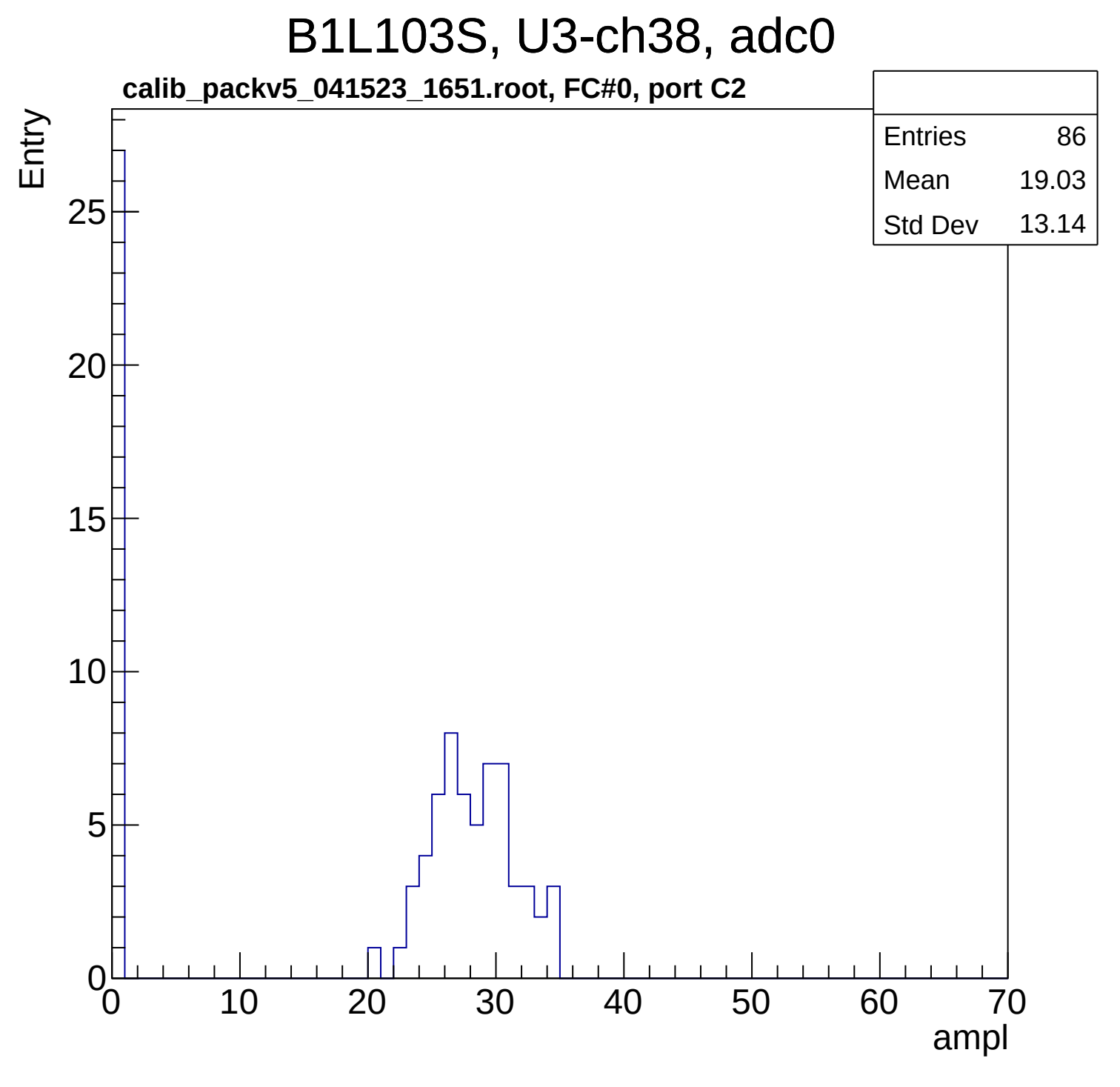
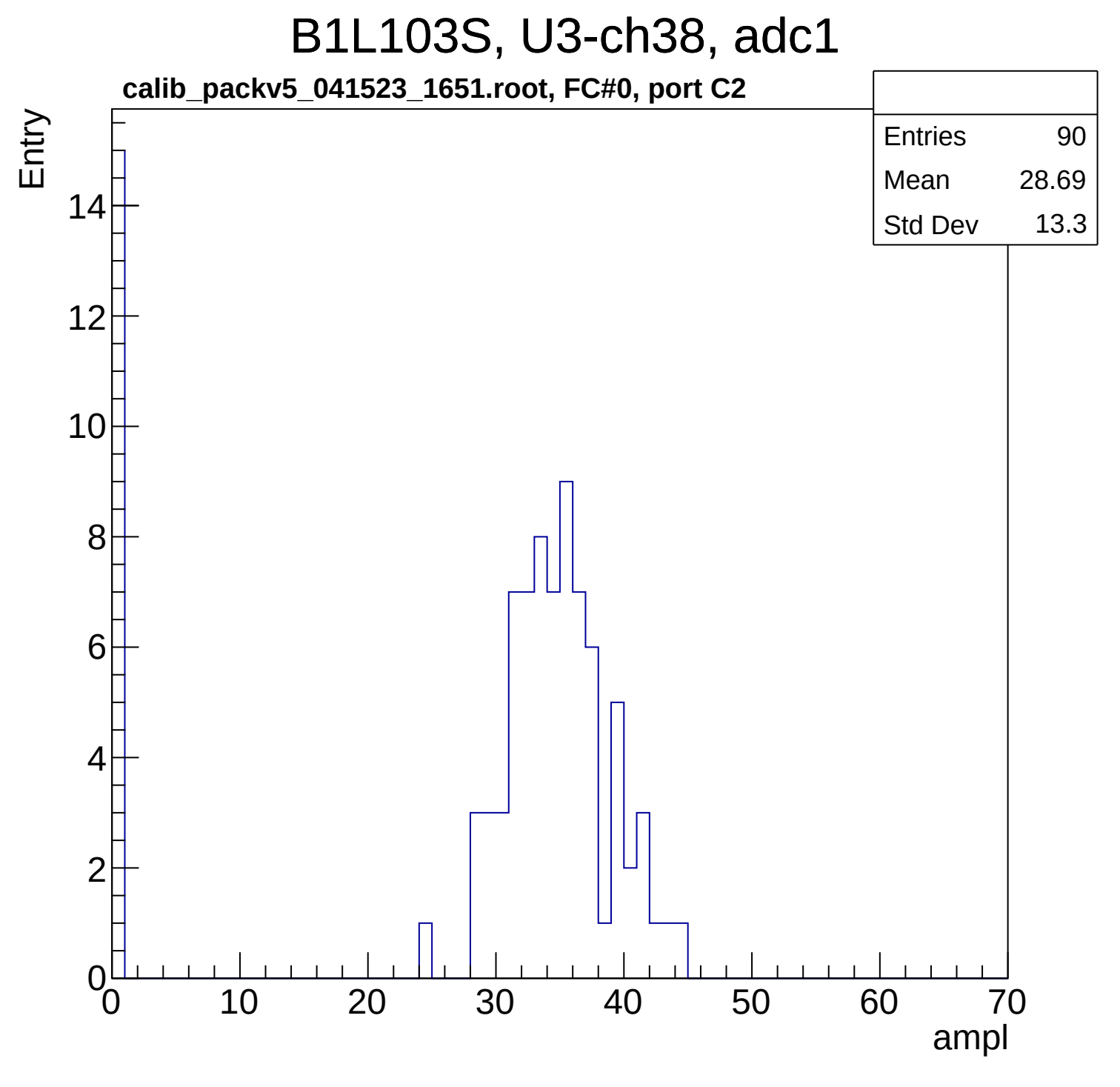
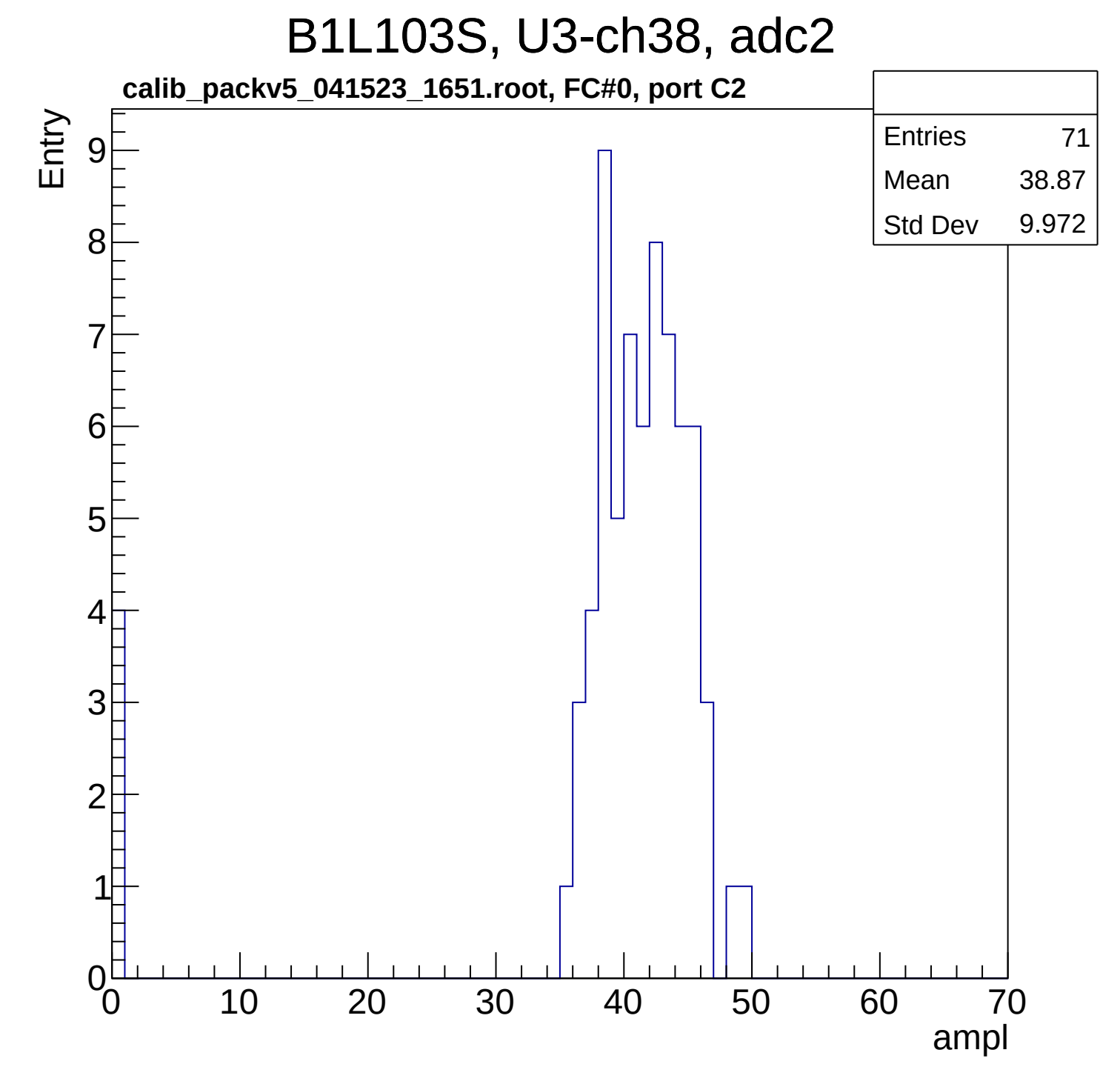
30
40
50
60
70
ampl


B1L103S, U3-ch38, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 19.03
Std Dev 13.14
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch38, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 28.69
Std Dev 13.3
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U3-ch38, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 38.87
Std Dev 9.972
Entry
ampl
0
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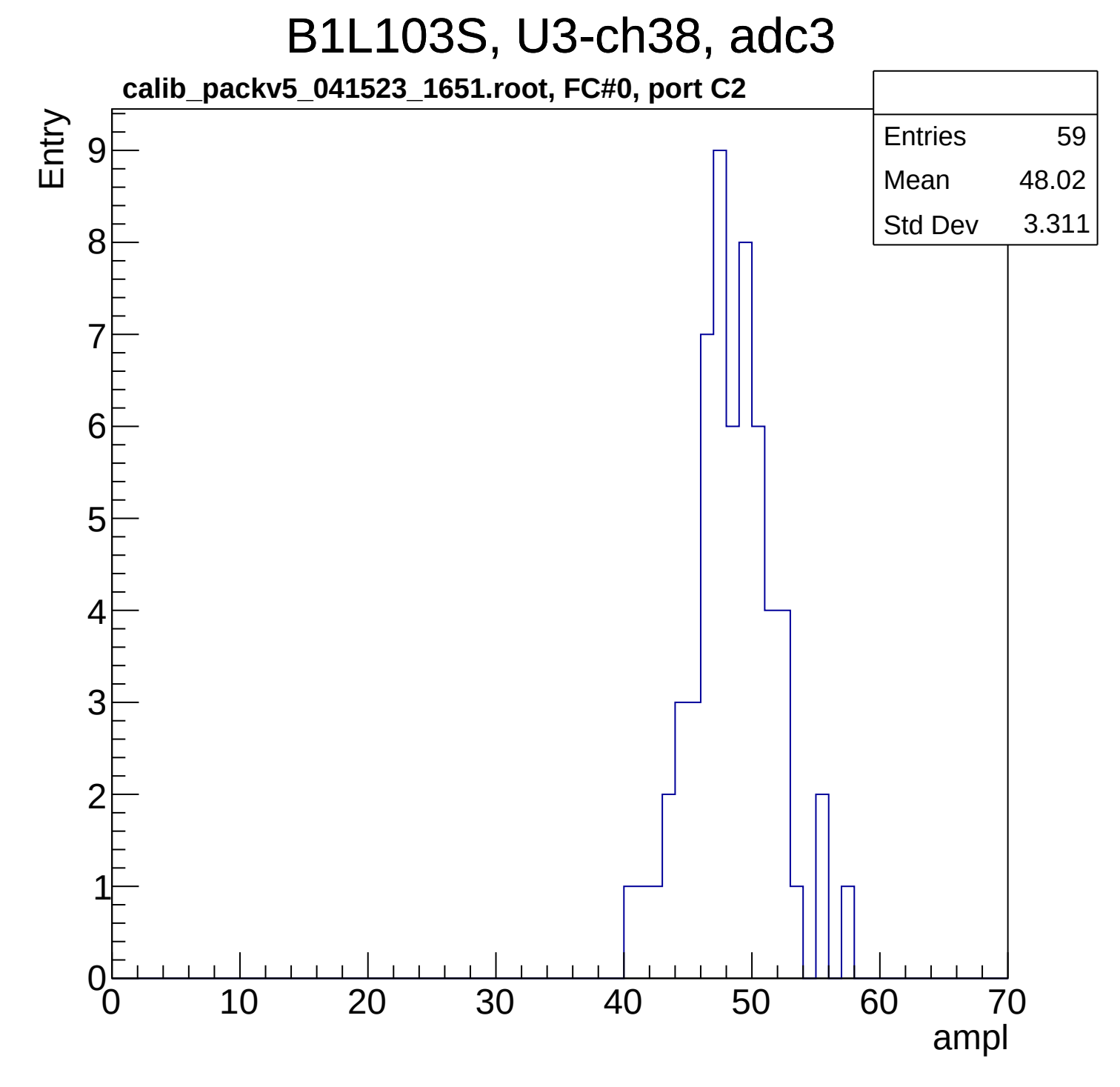
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch38, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 48.02
Std Dev 3.311
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
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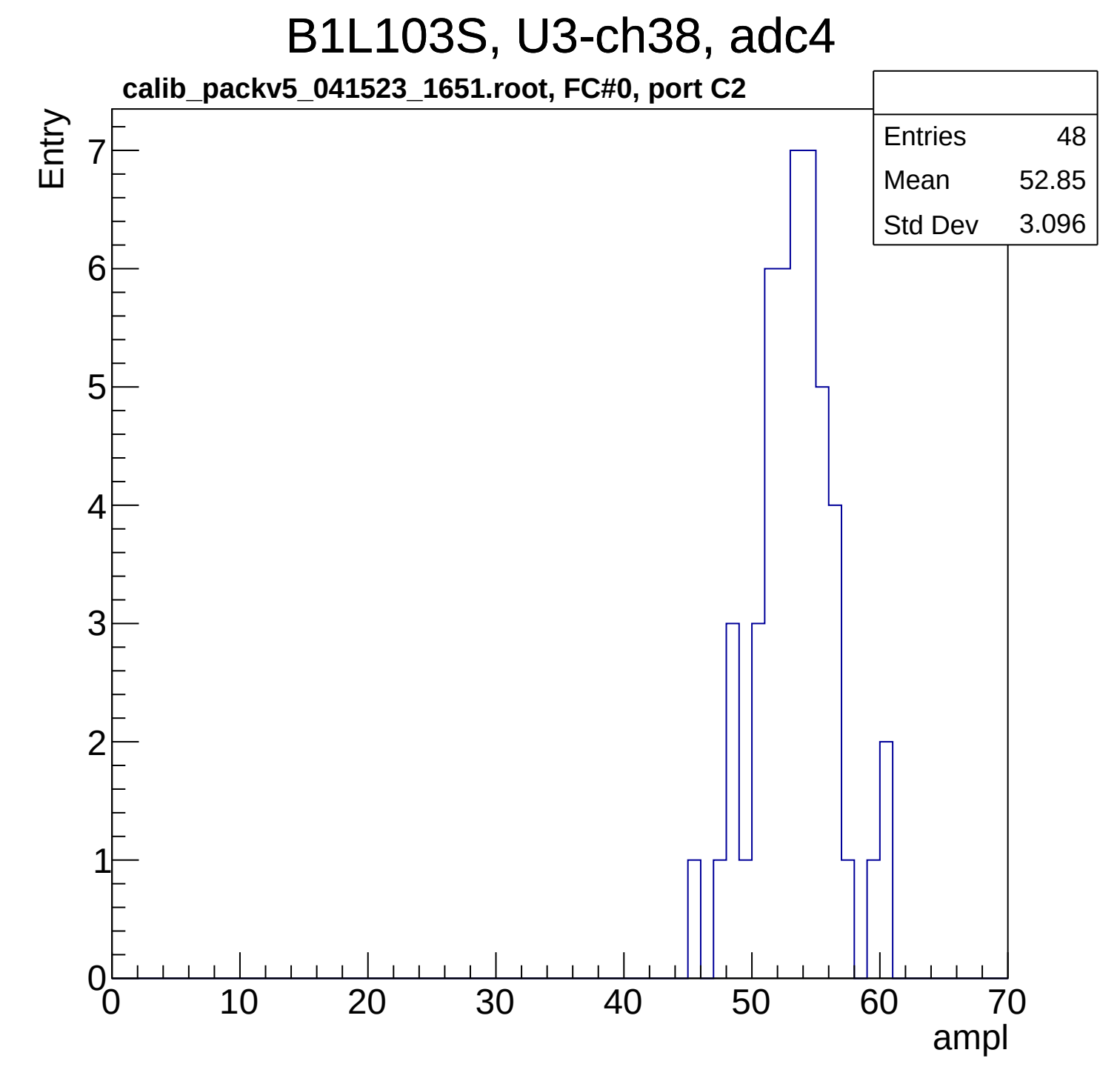
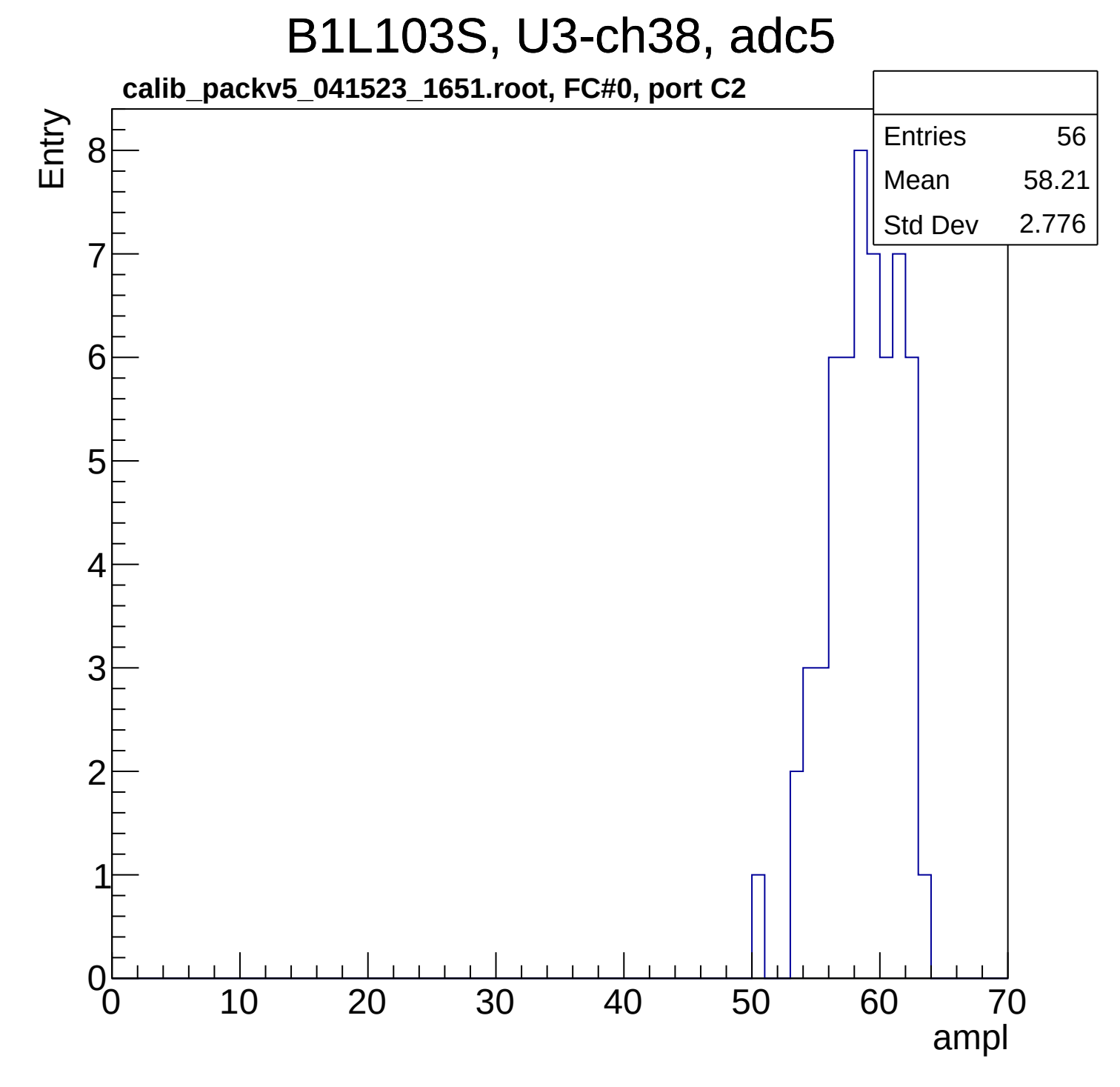
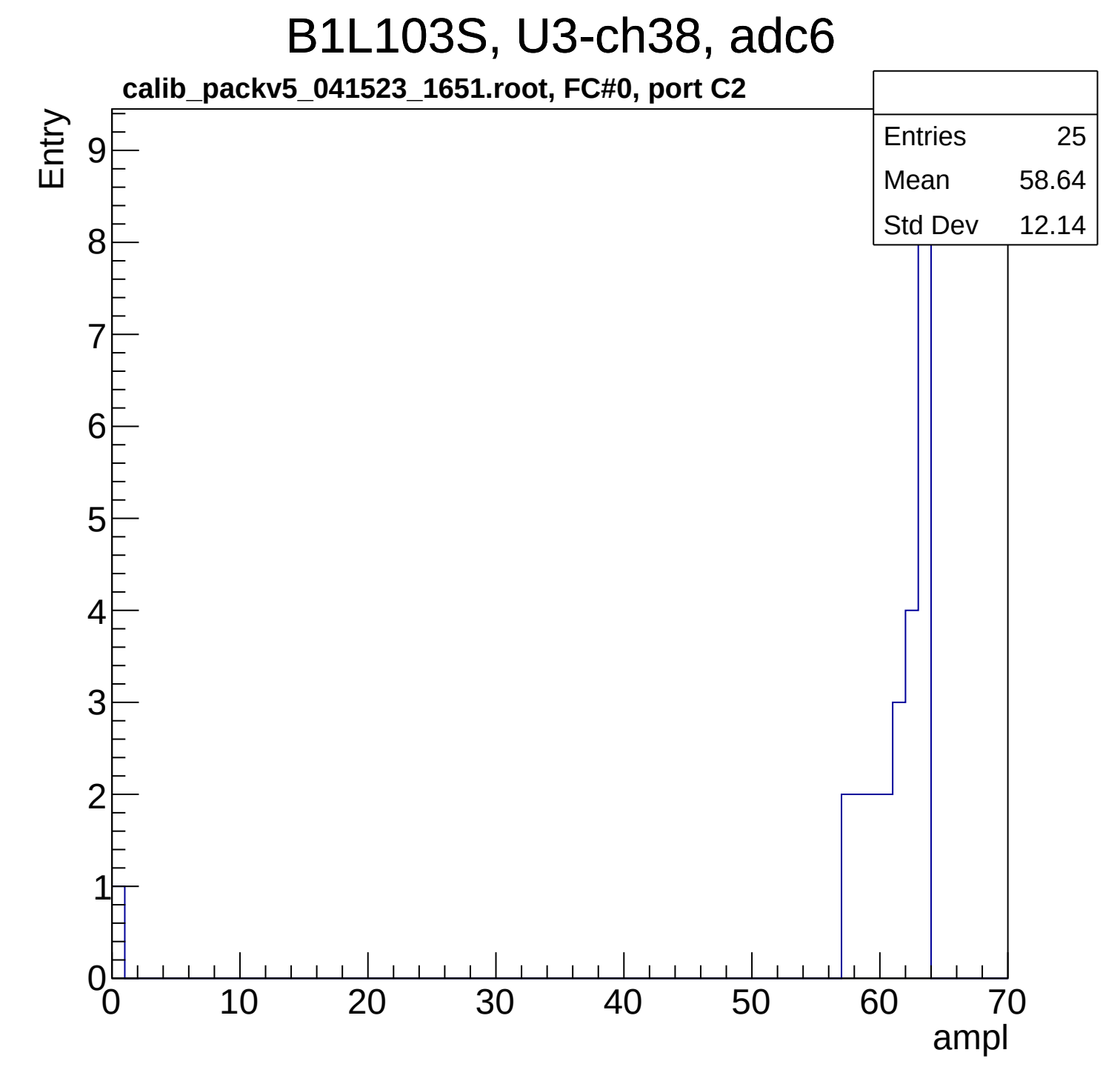
60
70


B1L103S, U3-ch38, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 52.85
Std Dev 3.096
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch38, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 58.21
Std Dev 2.776
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch38, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 58.64
Std Dev 12.14
Entry
ampl
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2
3
4
5
6
7
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0
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60
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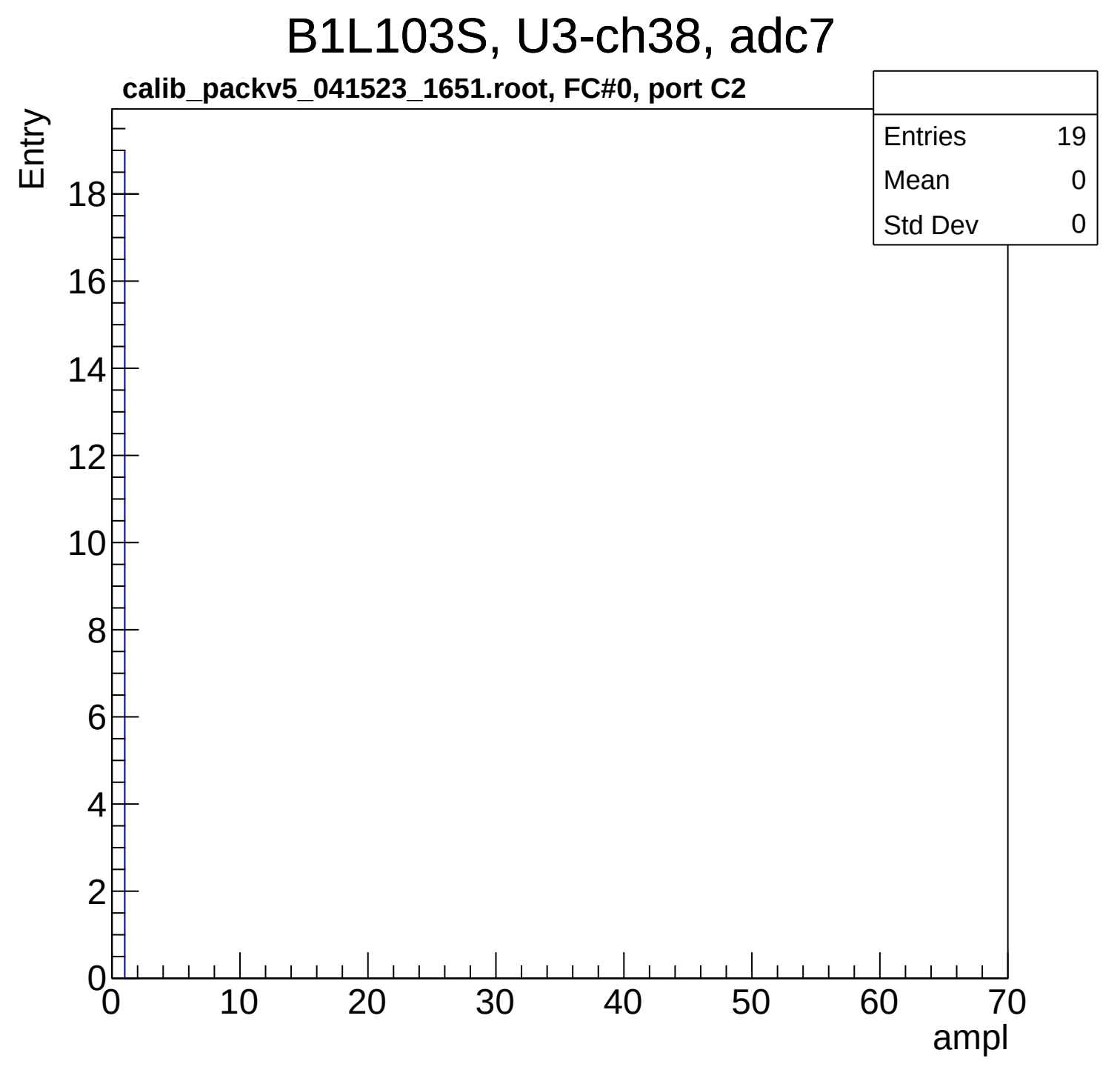
B1L103S, U3-ch38, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
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4
6
8
10
12
14
16
18
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10
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50
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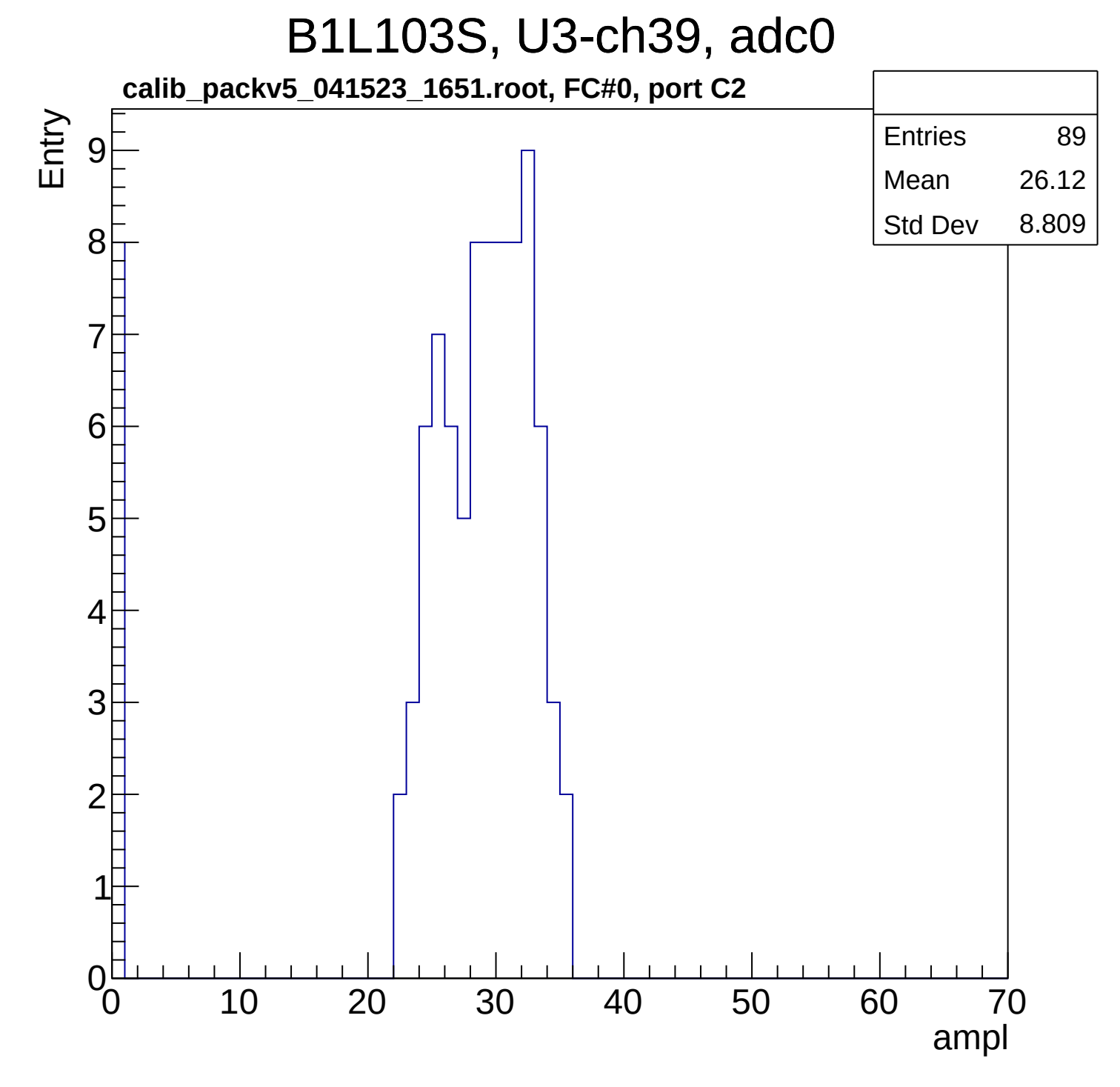
70
ampl


B1L103S, U3-ch39, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 26.12
Std Dev 8.809
Entry
ampl
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6
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8
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0
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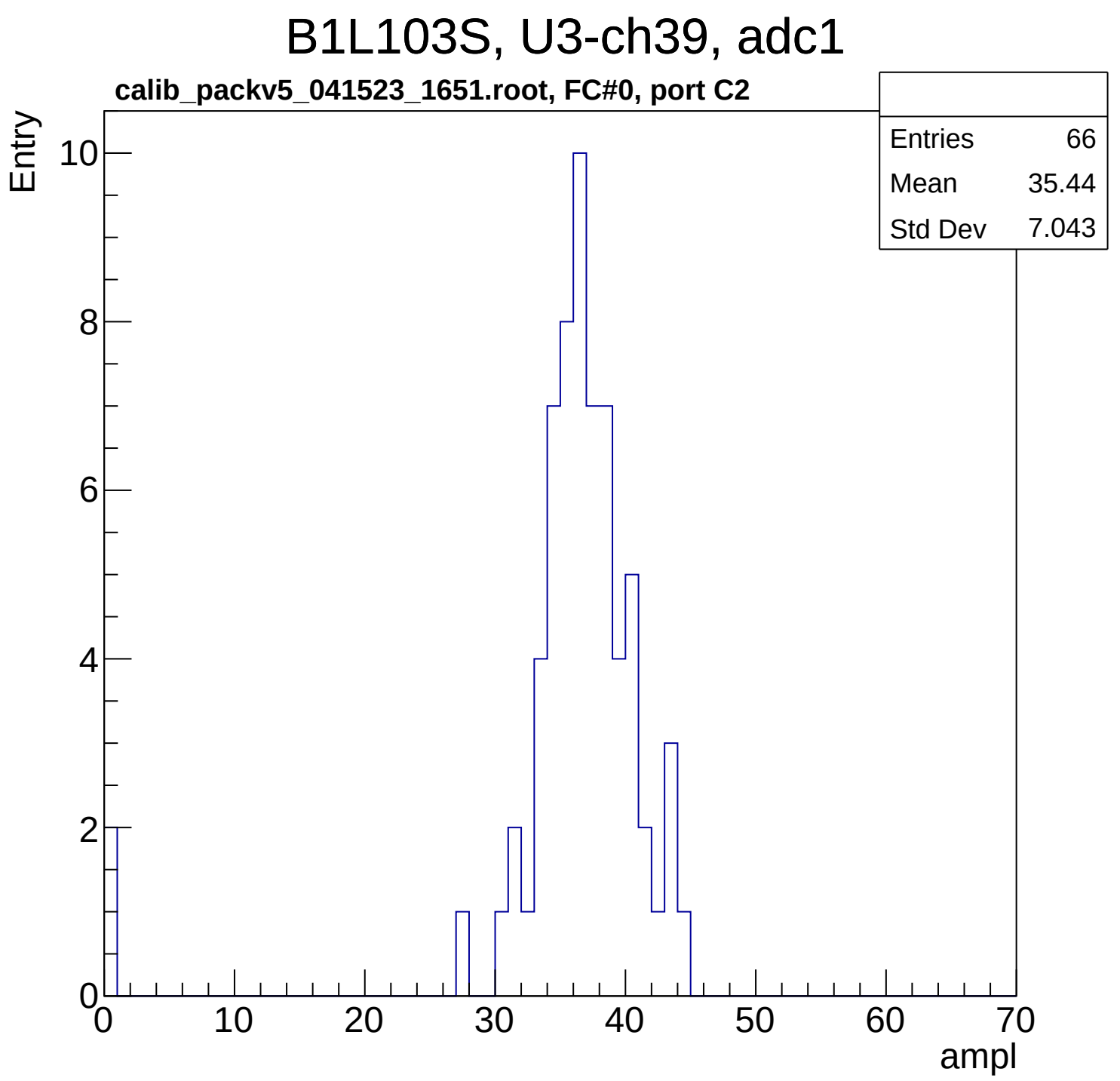
B1L103S, U3-ch39, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 35.44
Std Dev 7.043
Entry
ampl
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0
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40
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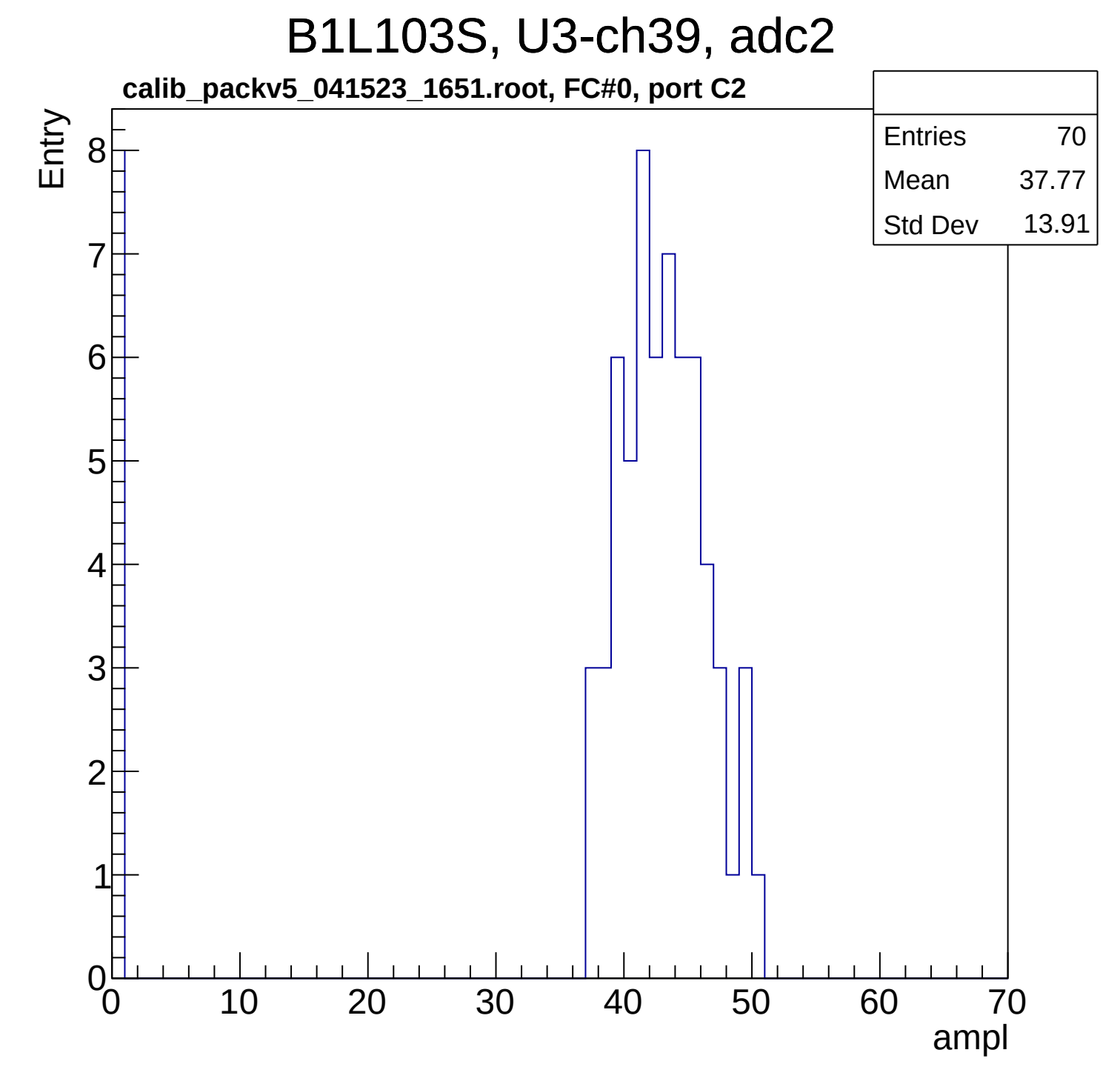
B1L103S, U3-ch39, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 37.77
Std Dev 13.91
Entry
0
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2
3
4
5
6
7
8
0
10
20
30
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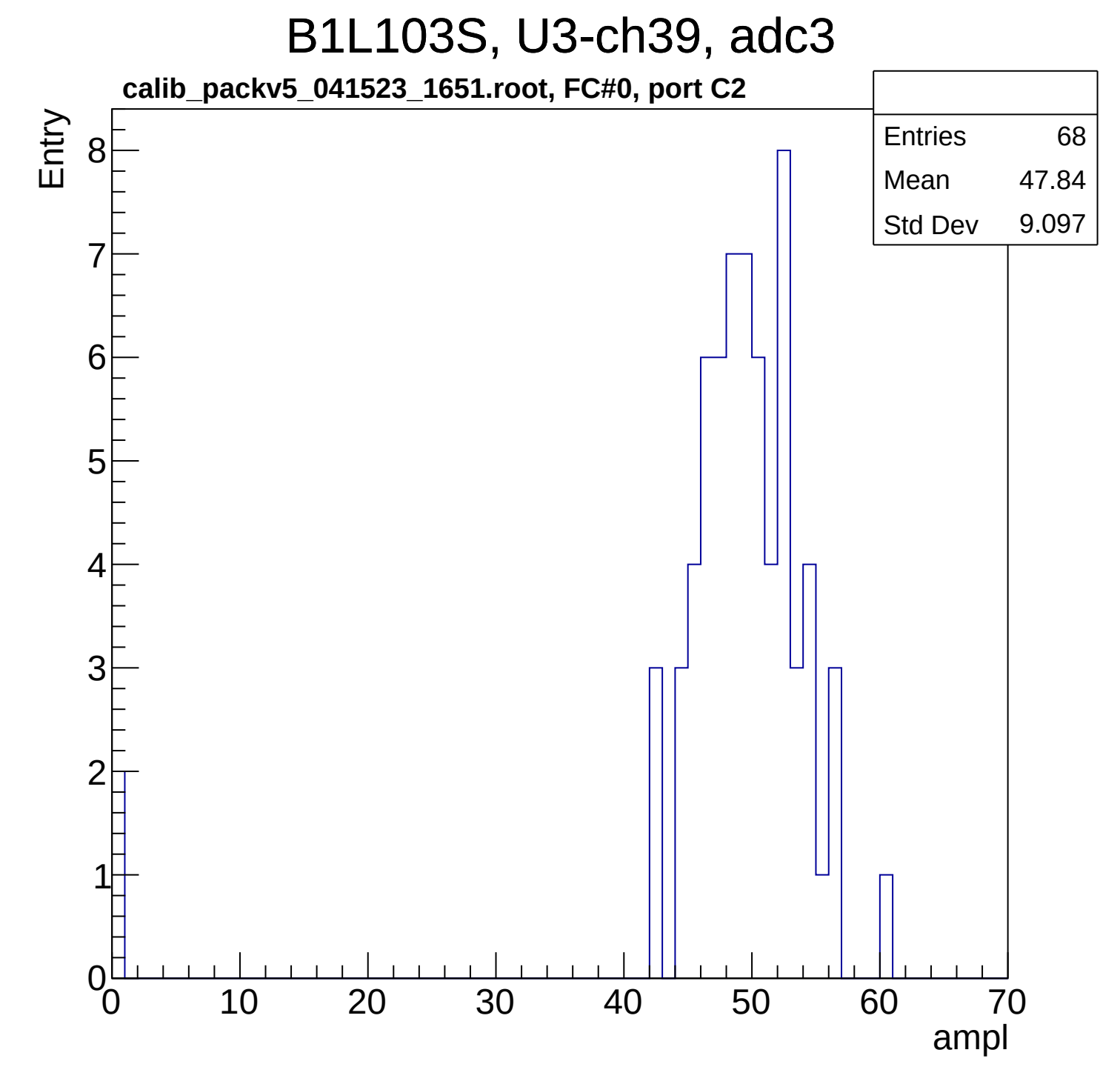
50
60
70
ampl


B1L103S, U3-ch39, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 47.84
Std Dev 9.097
Entry
ampl
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2
3
4
5
6
7
8
0
10
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40
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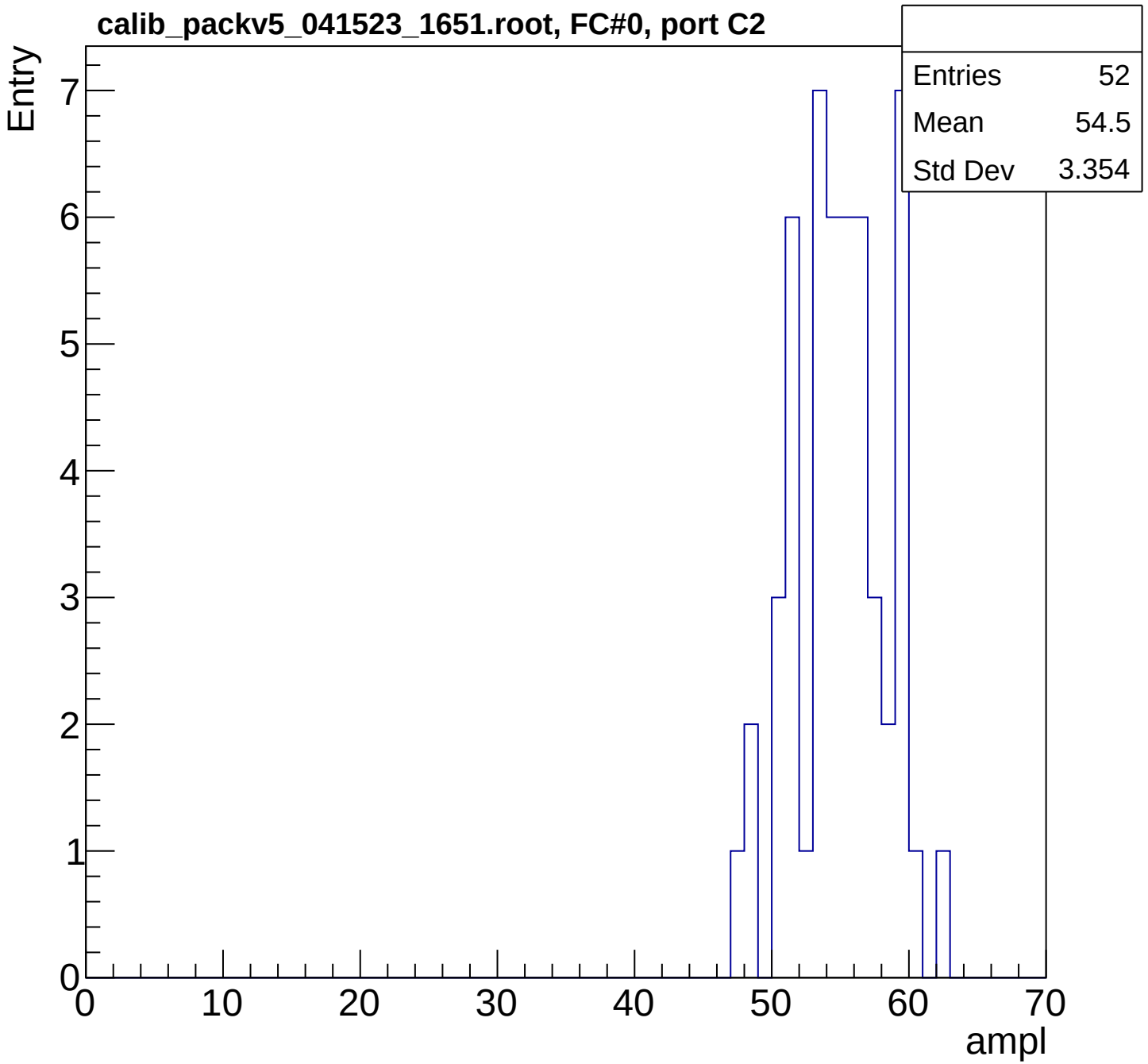
B1L103S, U3-ch39, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 54.5
Std Dev 3.354
Entry
ampl
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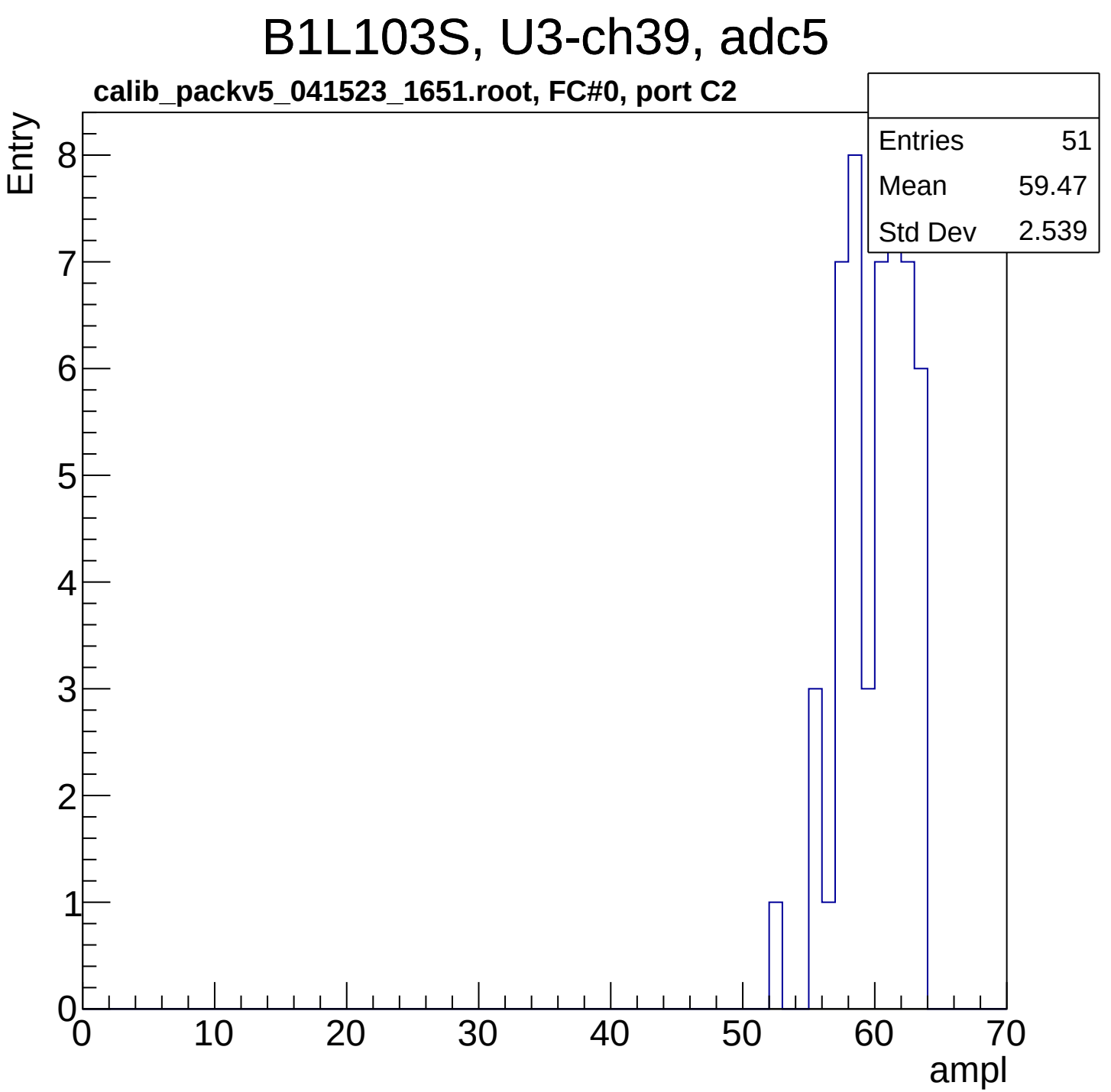
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch39, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 59.47
Std Dev 2.539
Entry
ampl
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1
2
3
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6
7
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0
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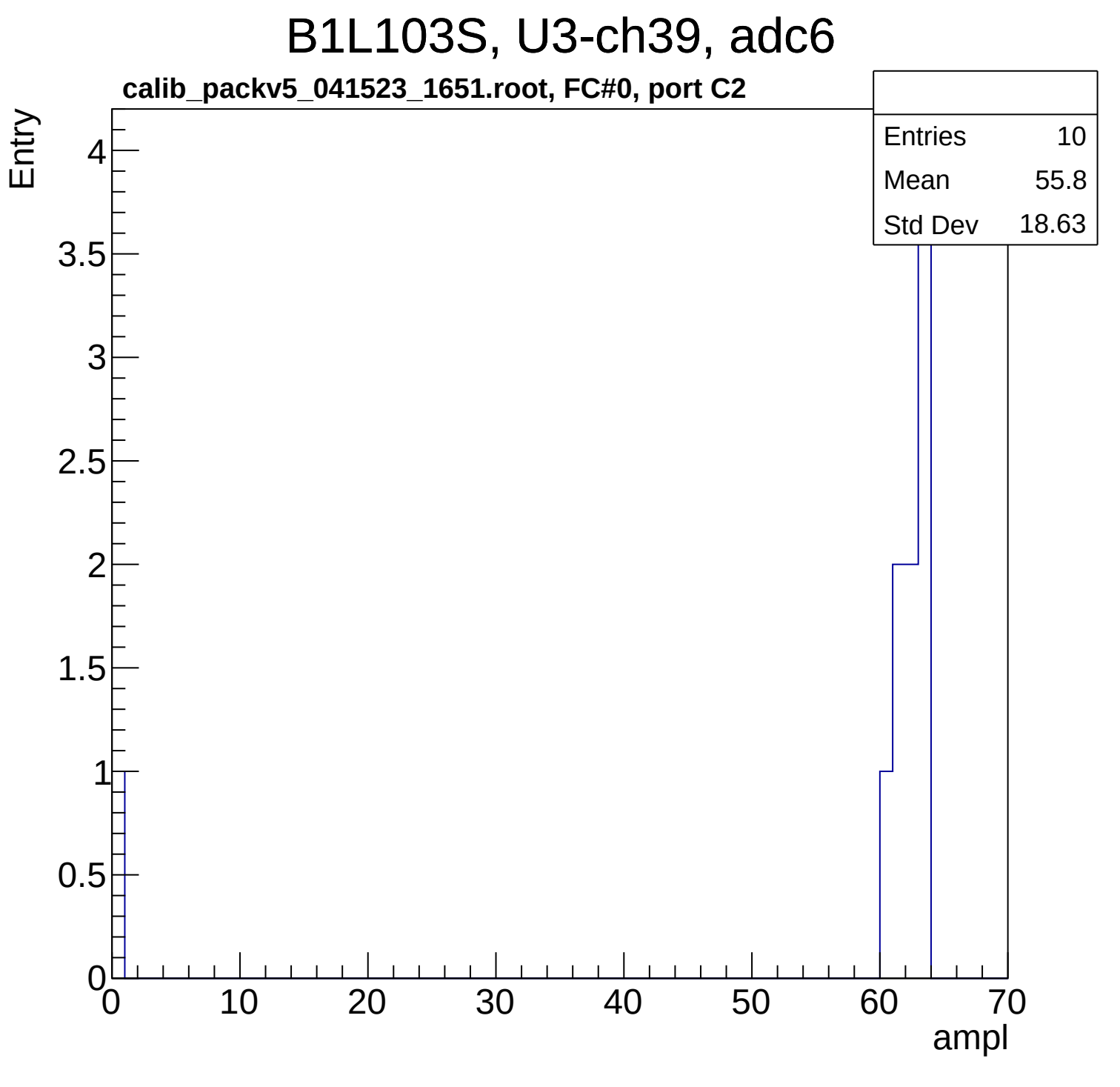
B1L103S, U3-ch39, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 55.8
Std Dev 18.63
Entry
ampl
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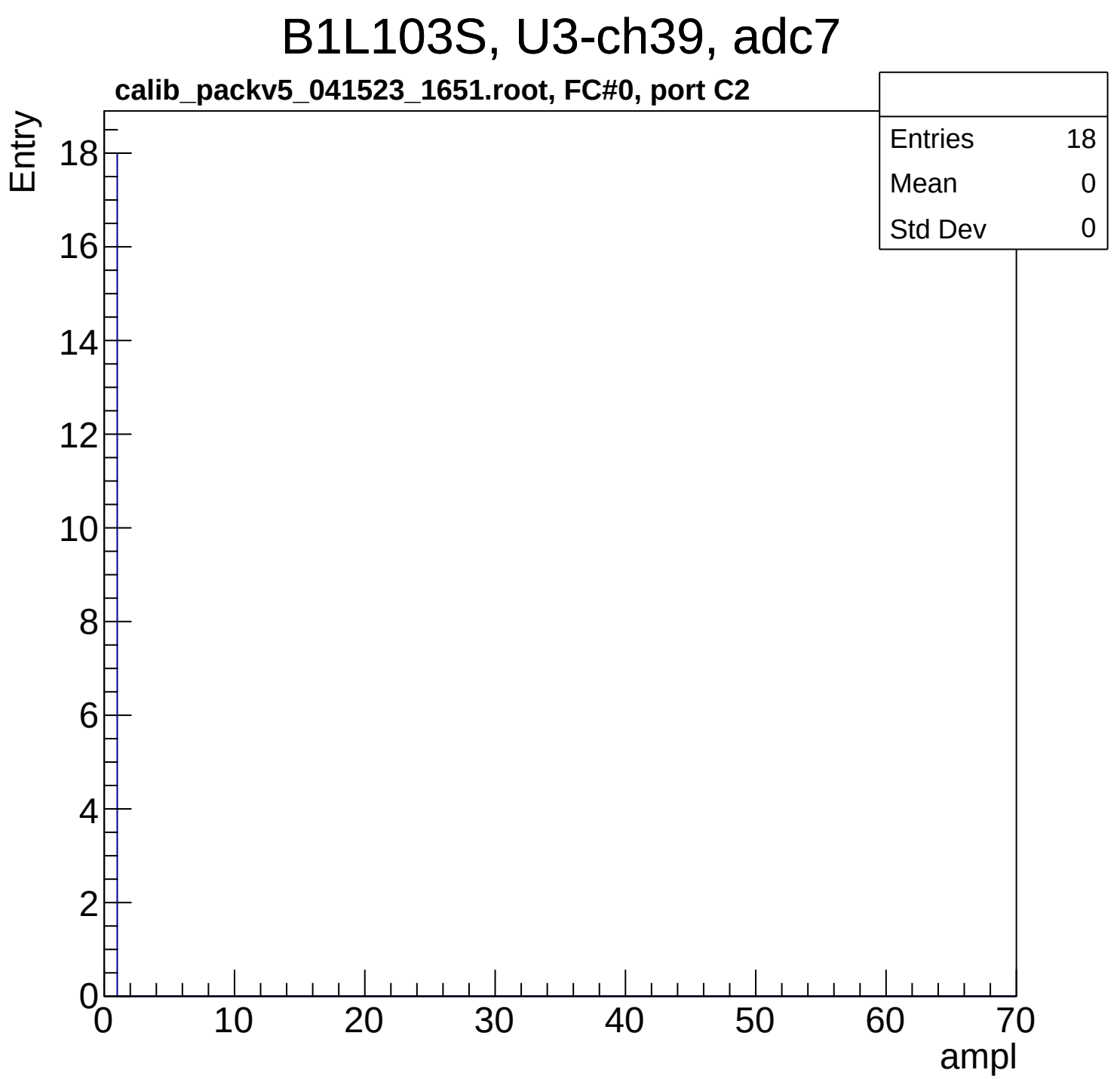
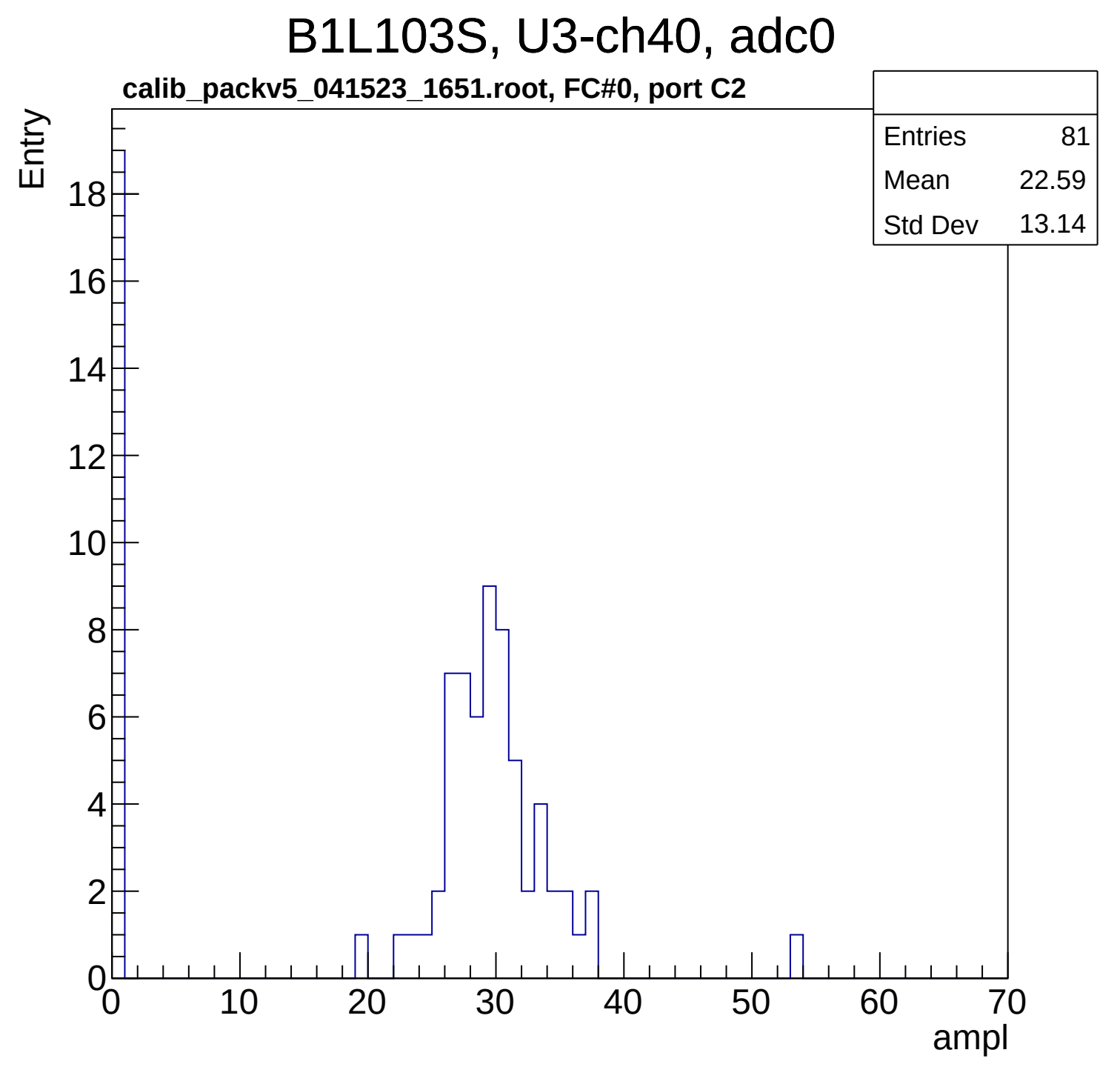
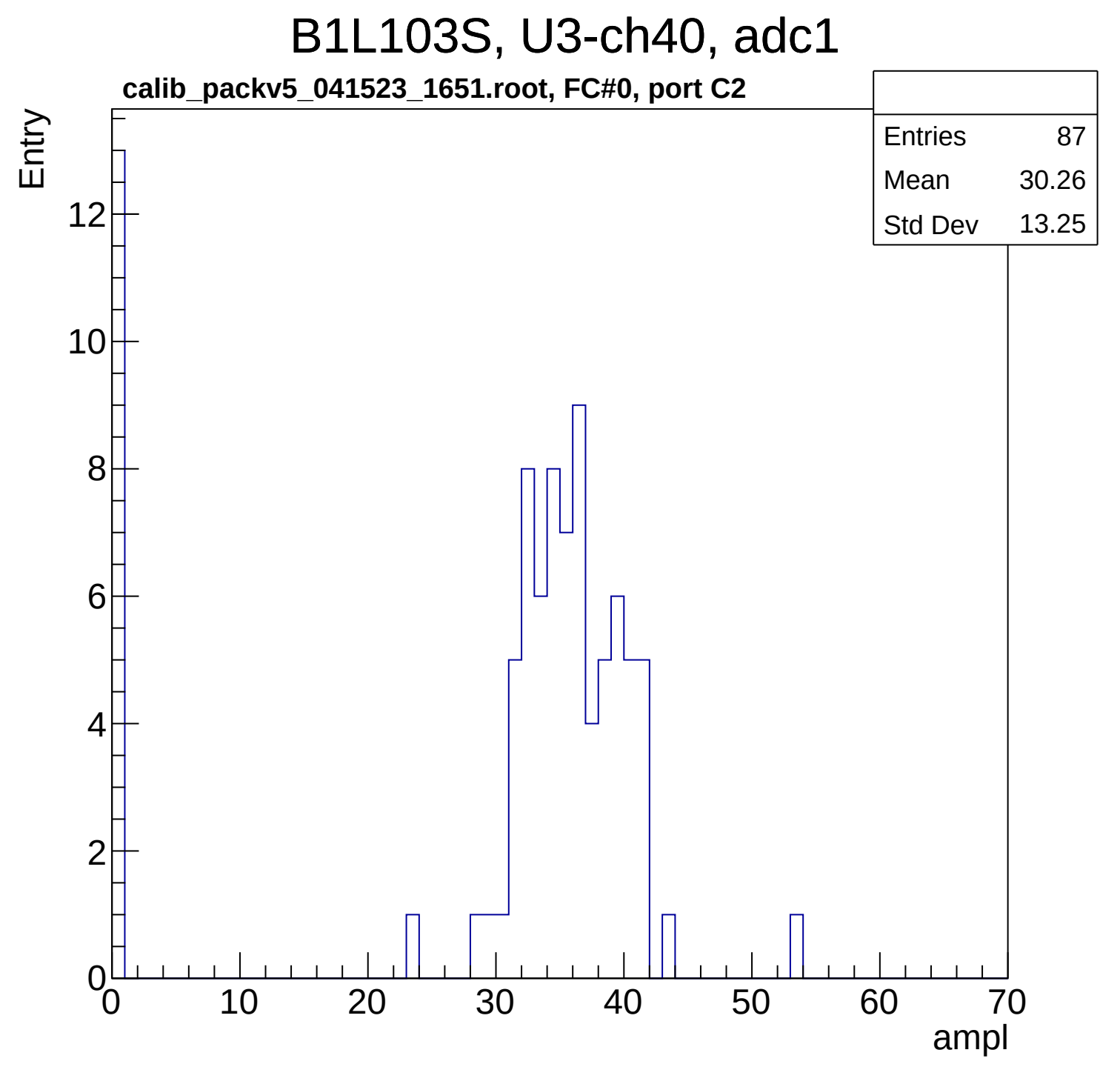
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U3-ch39, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch40, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 22.59
Std Dev 13.14
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch40, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 30.26
Std Dev 13.25
Entry
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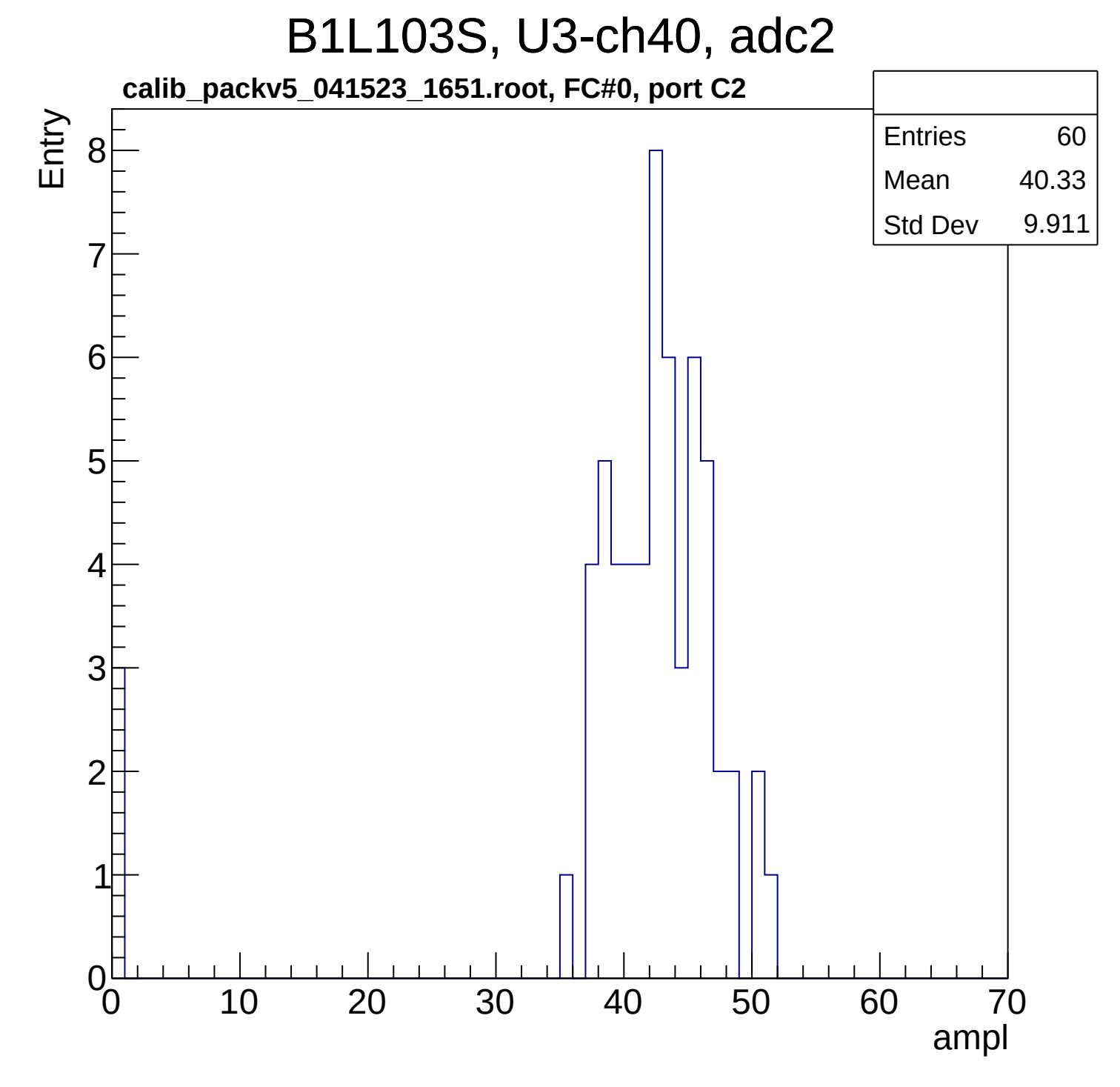
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch40, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 40.33
Std Dev 9.911
Entry
ampl
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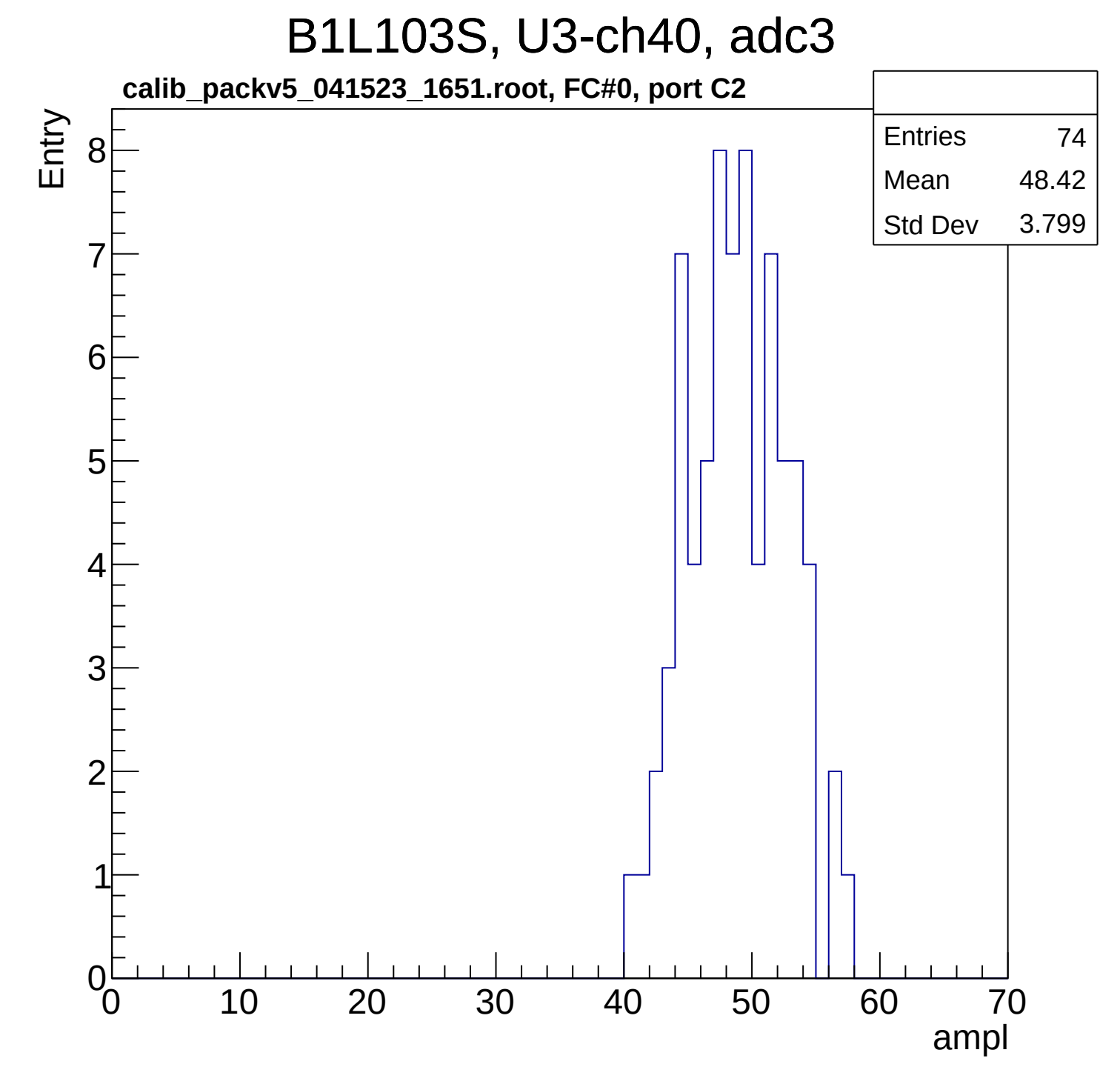
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch40, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 48.42
Std Dev 3.799
Entry
ampl
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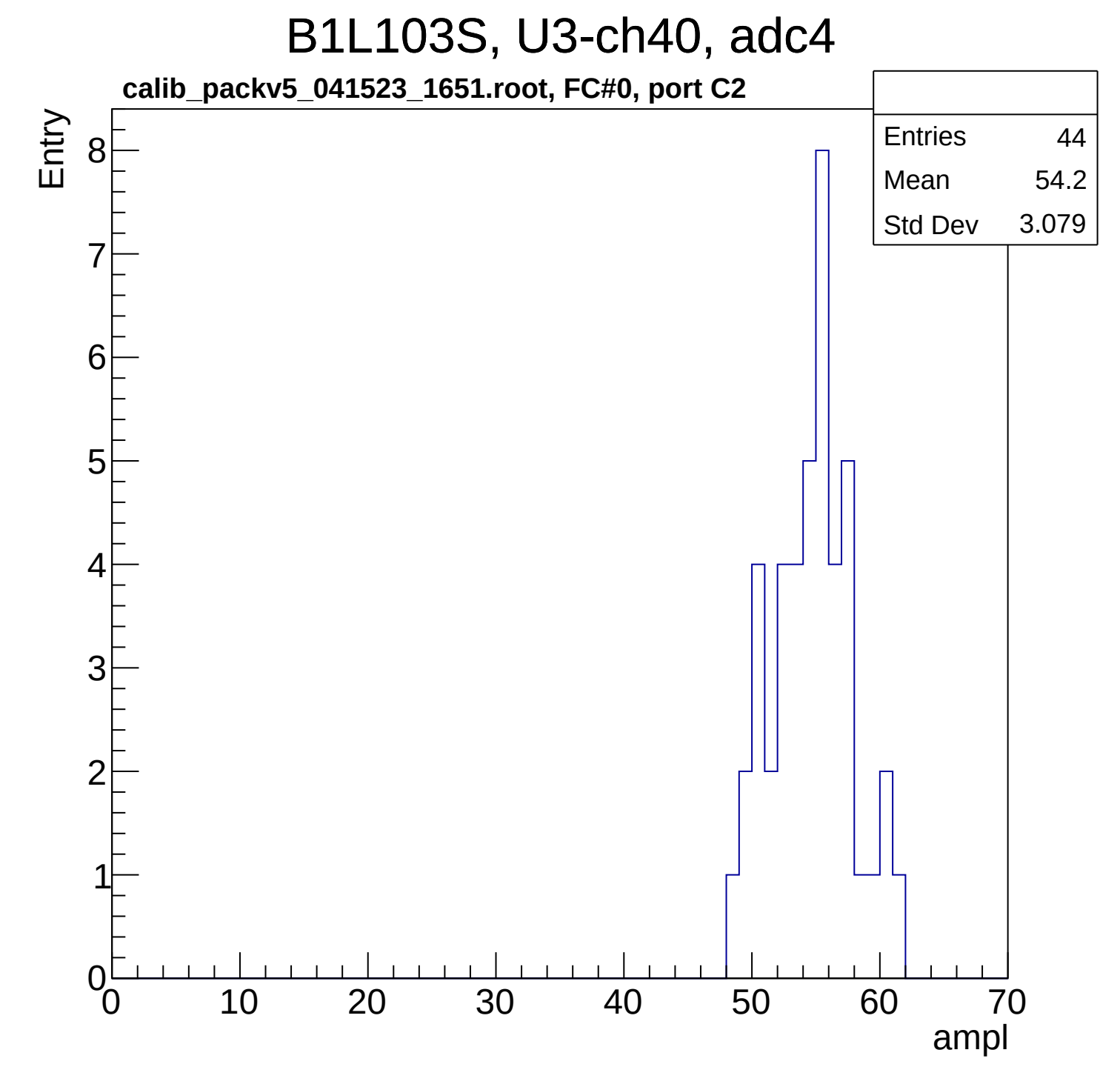
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch40, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 54.2
Std Dev 3.079
Entry
ampl
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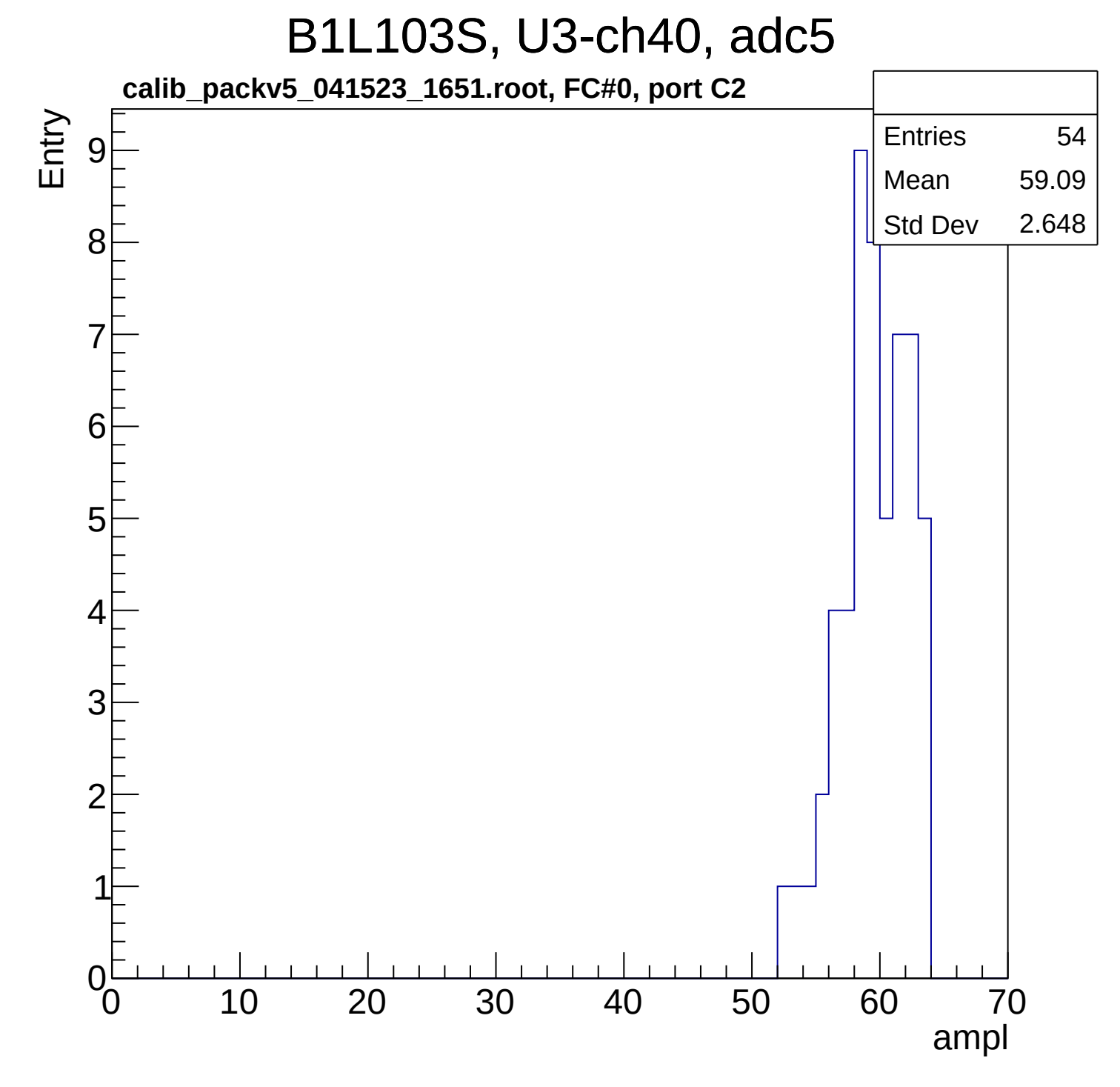
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch40, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 59.09
Std Dev 2.648
Entry
ampl
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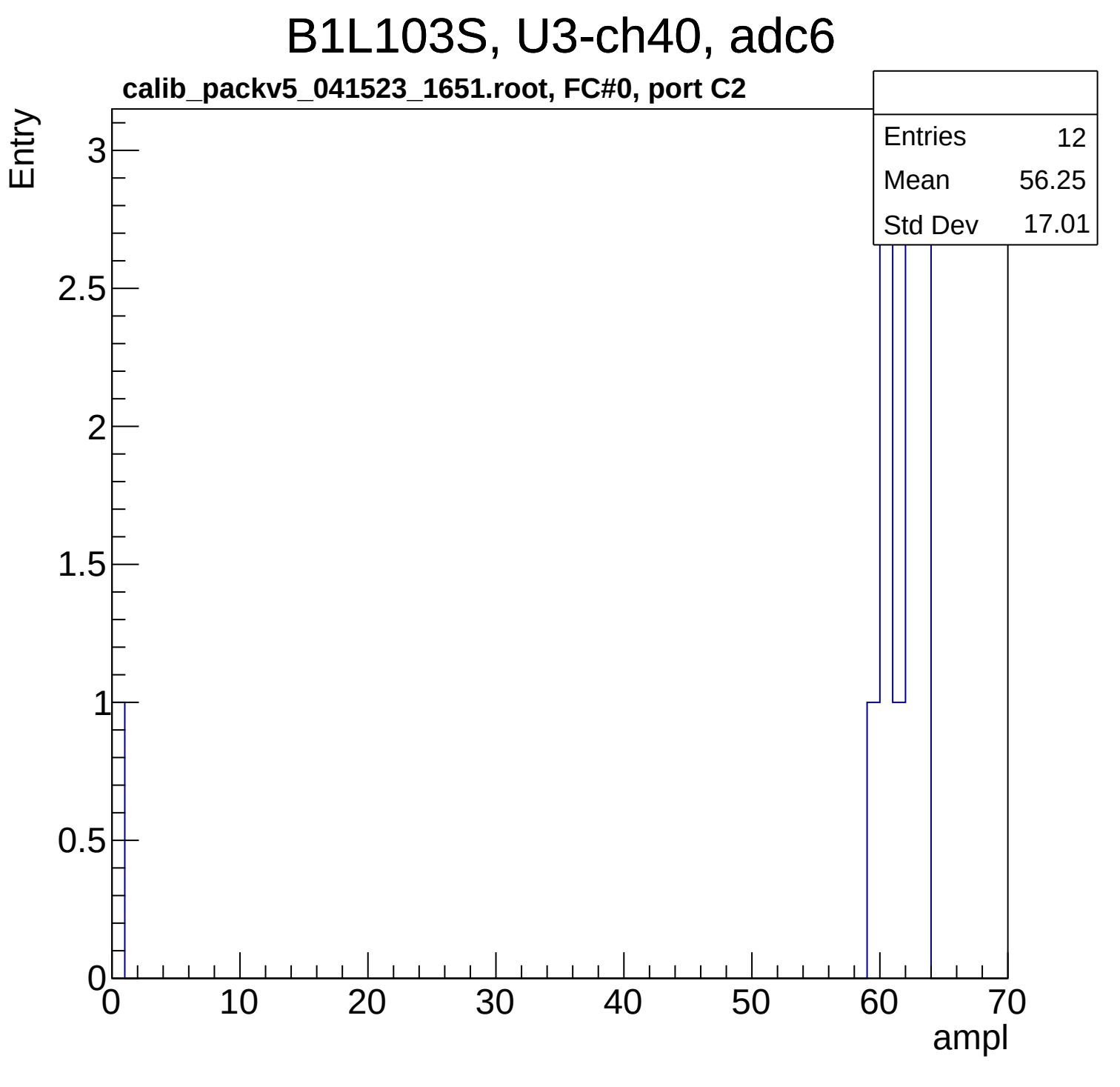
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch40, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 56.25
Std Dev 17.01
Entry
ampl
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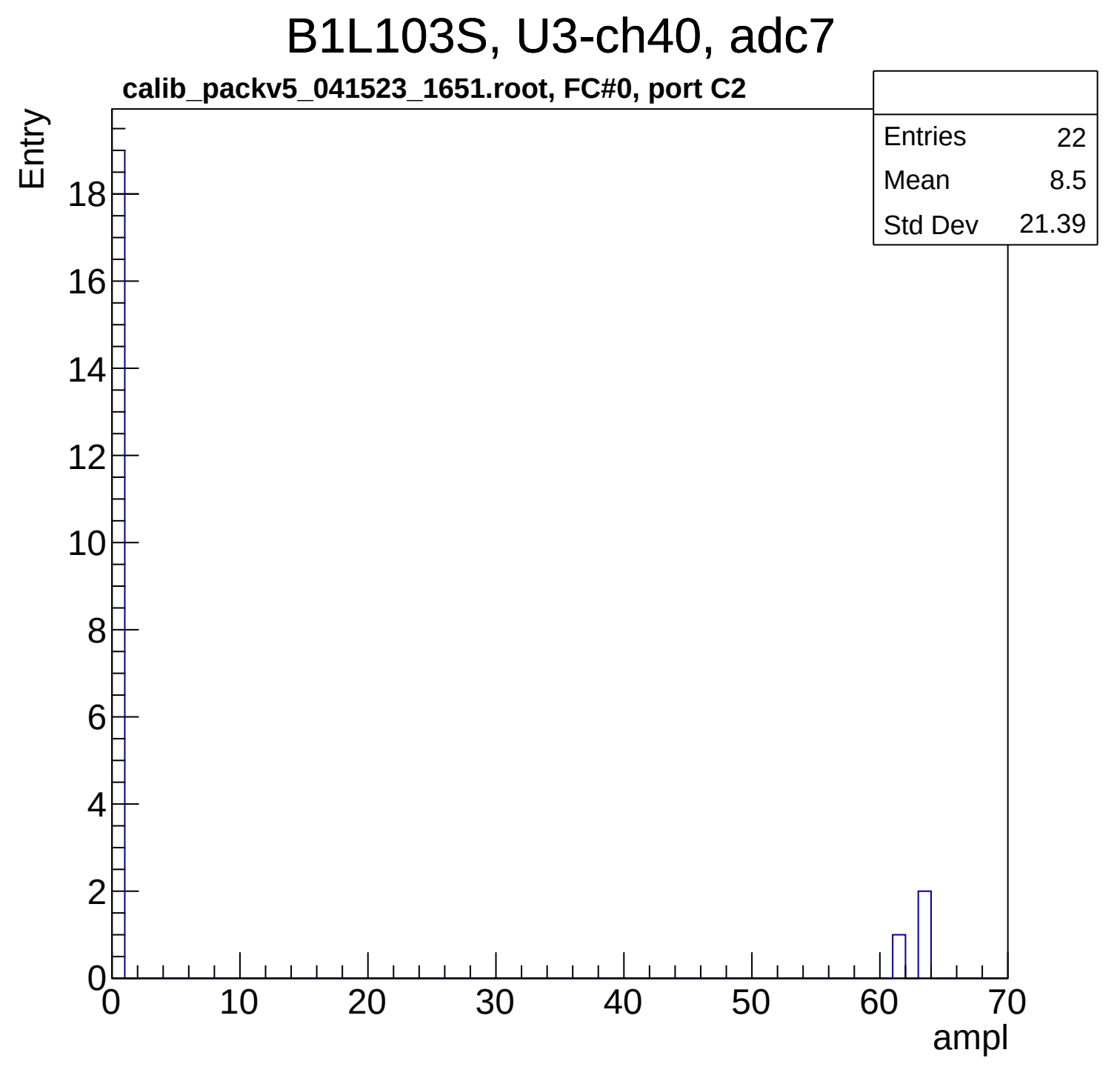
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U3-ch40, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.5
Std Dev 21.39
Entry
0
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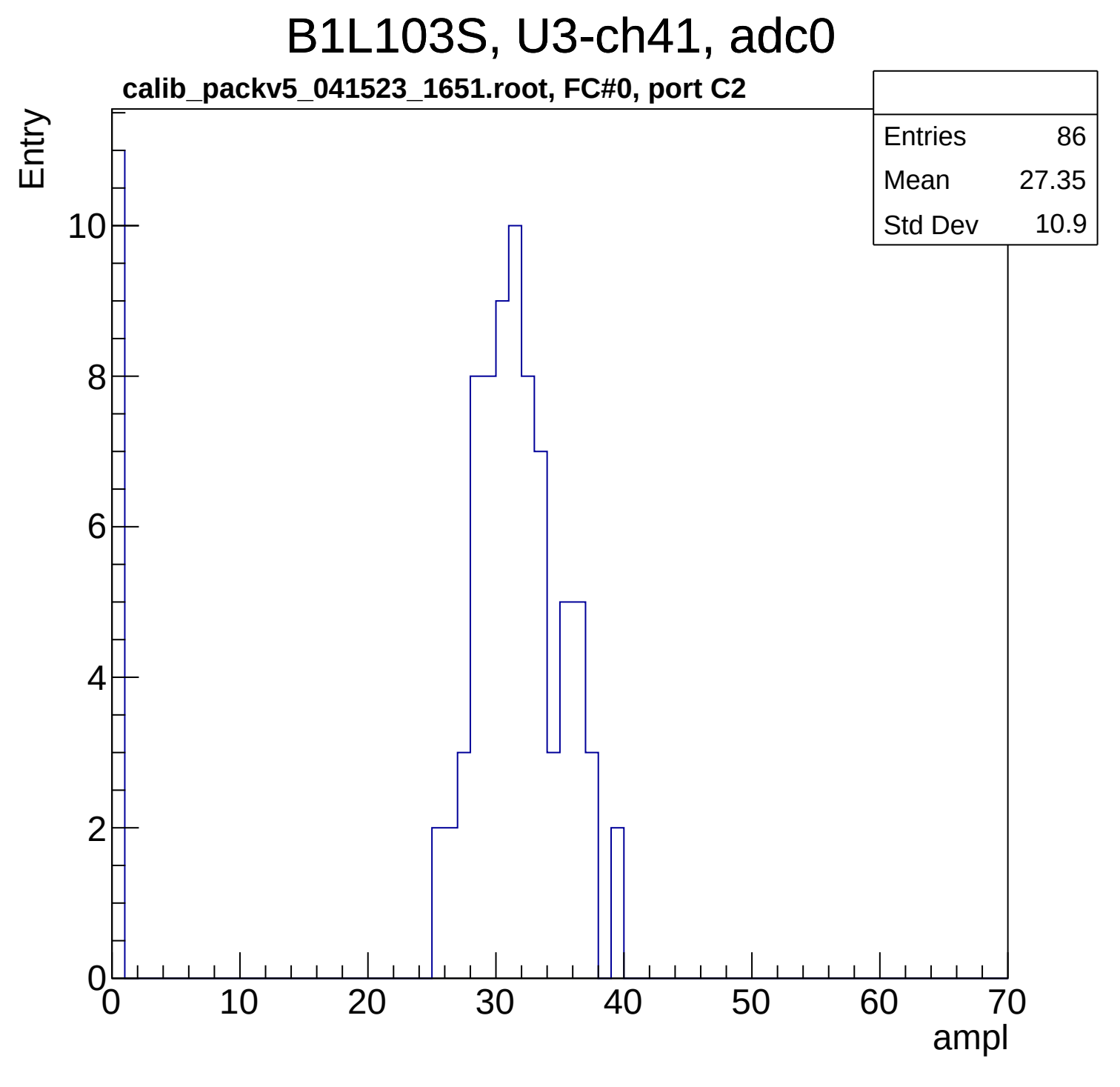
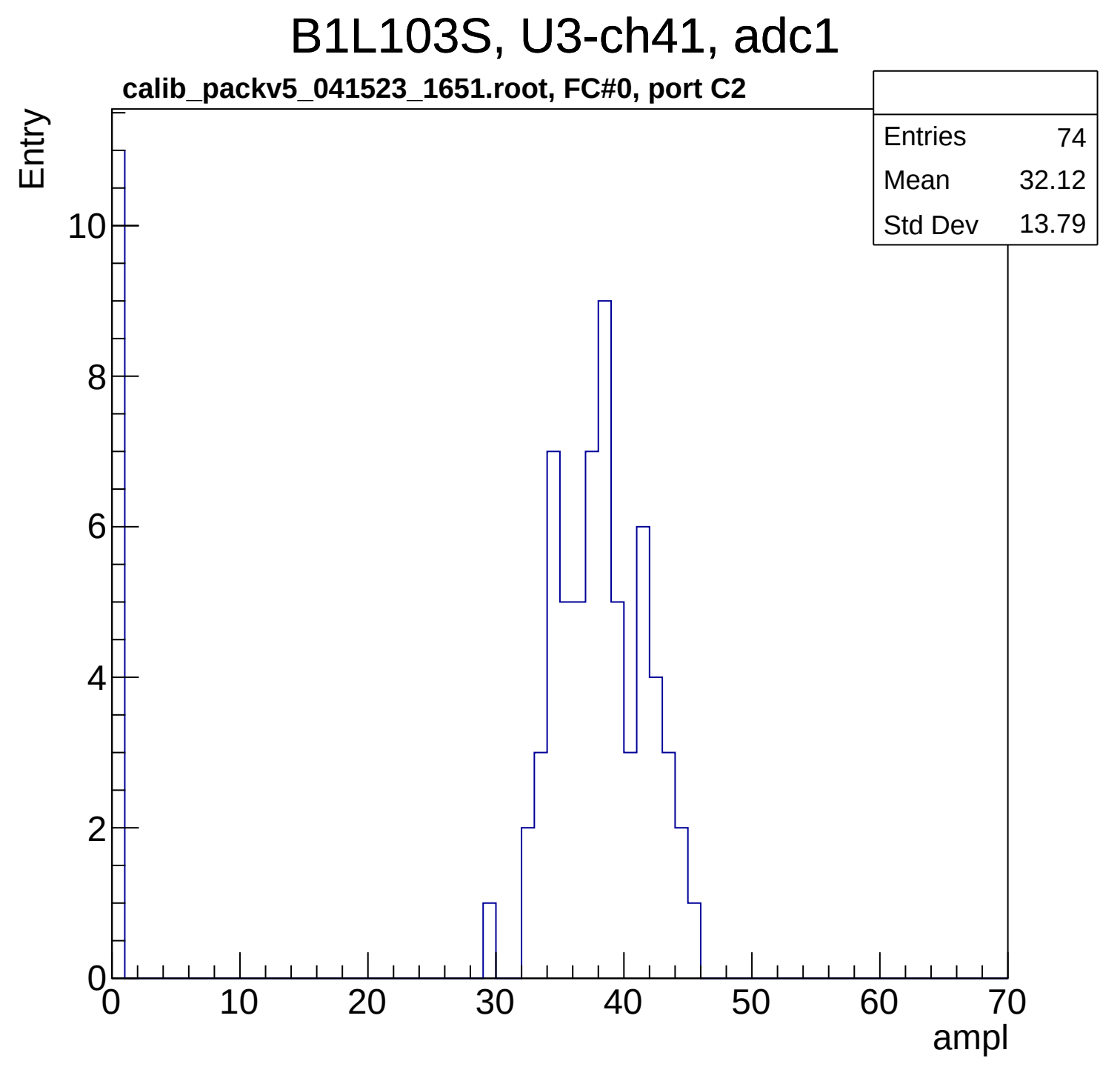
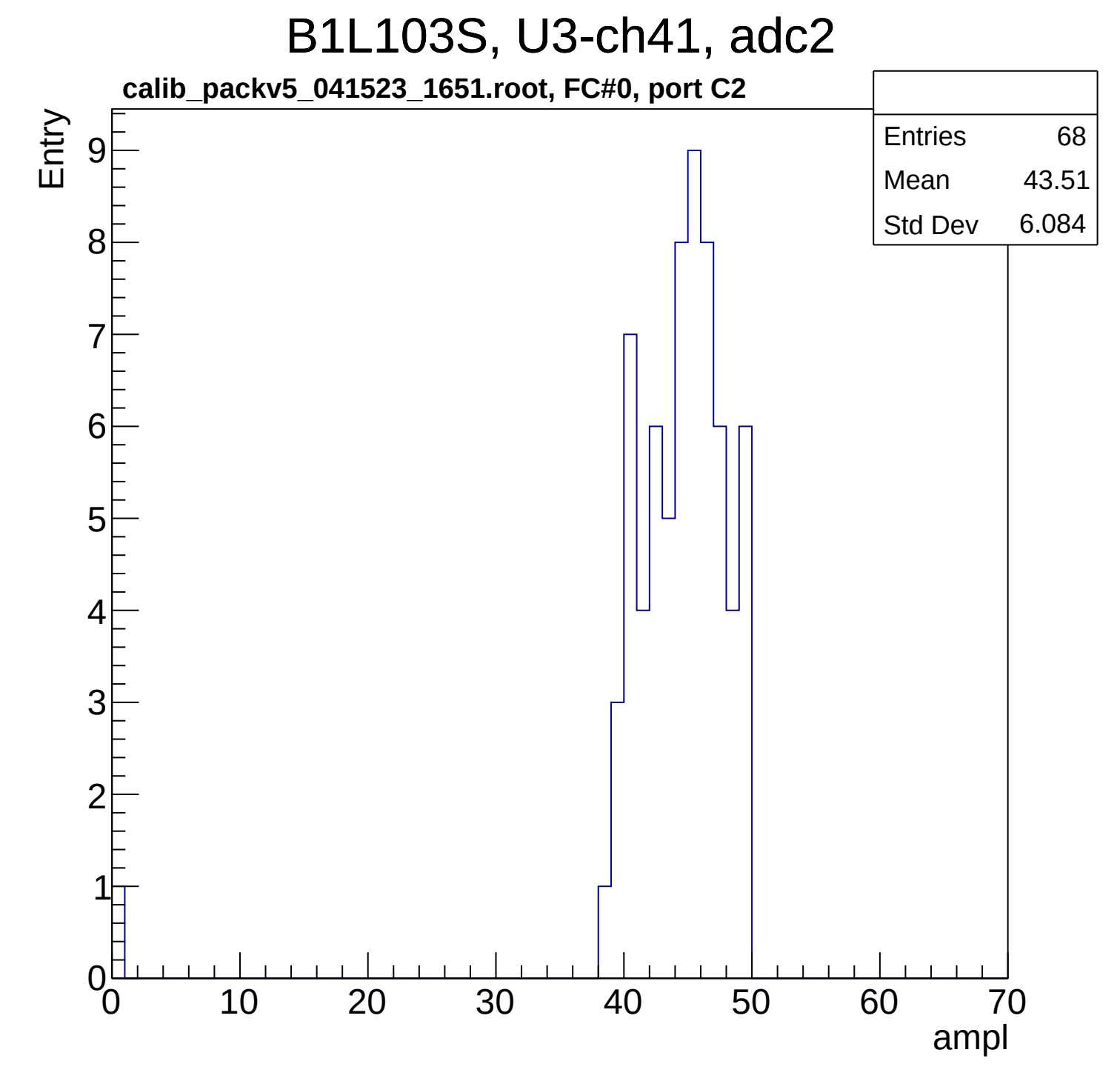
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch41, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 27.35
Std Dev 10.9
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch41, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 32.12
Std Dev 13.79
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch41, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 43.51
Std Dev 6.084
Entry
ampl
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2
3
4
5
6
7
8
9
0
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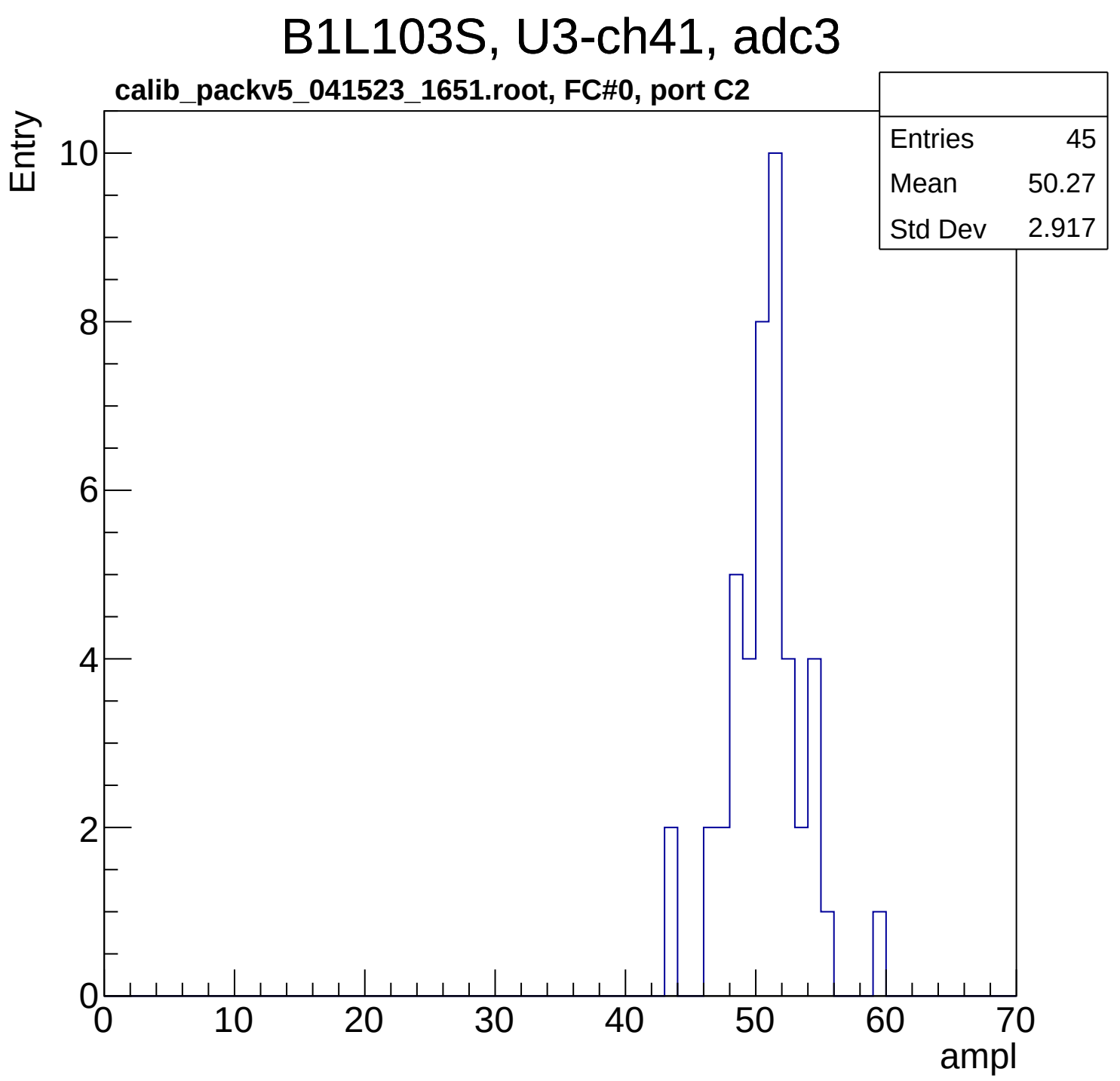
B1L103S, U3-ch41, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 50.27
Std Dev 2.917
Entry
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2
4
6
8
10
0
10
20
30
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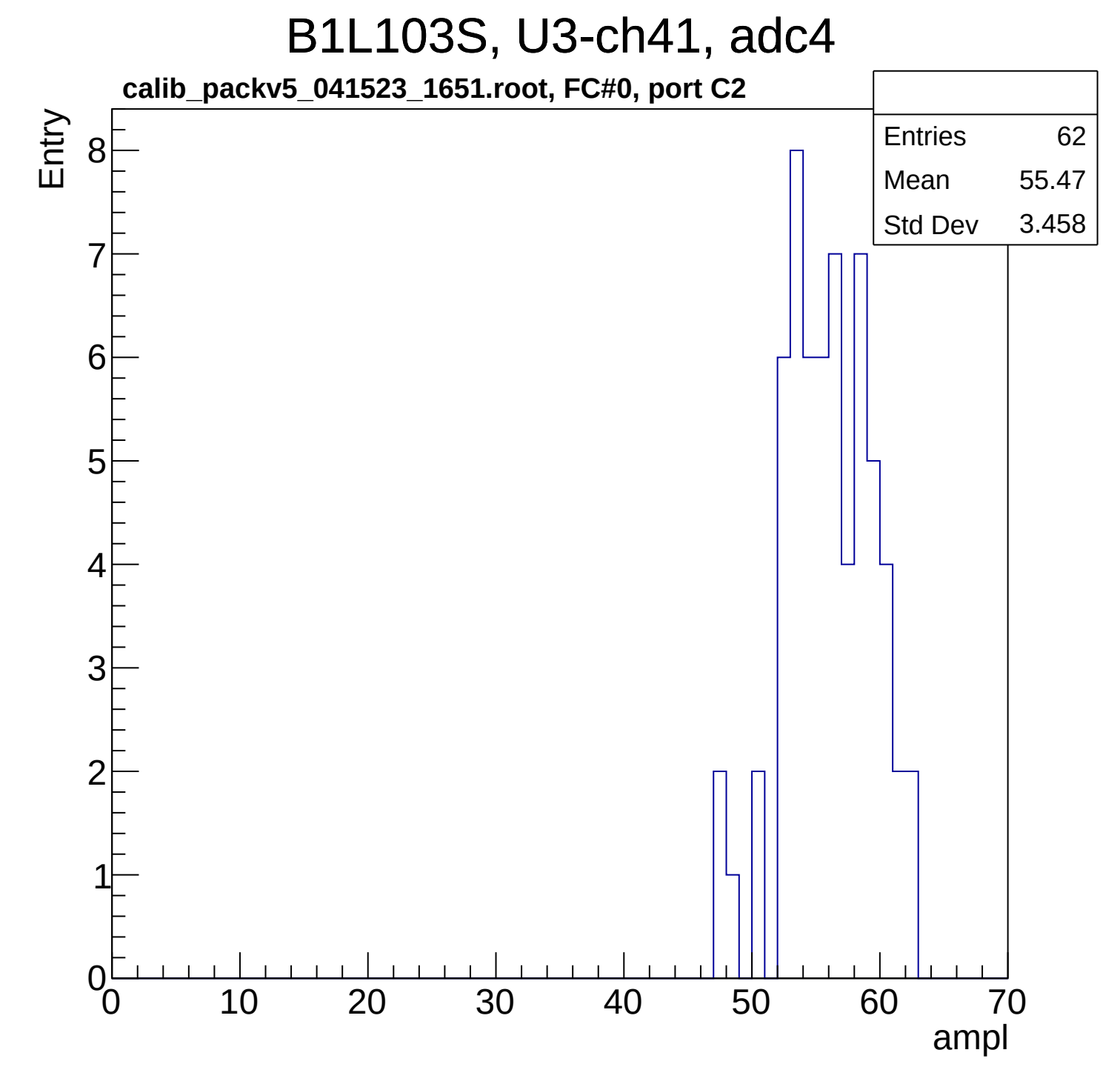
50
60
70
ampl


B1L103S, U3-ch41, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 55.47
Std Dev 3.458
Entry
ampl
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1
2
3
4
5
6
7
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0
10
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60
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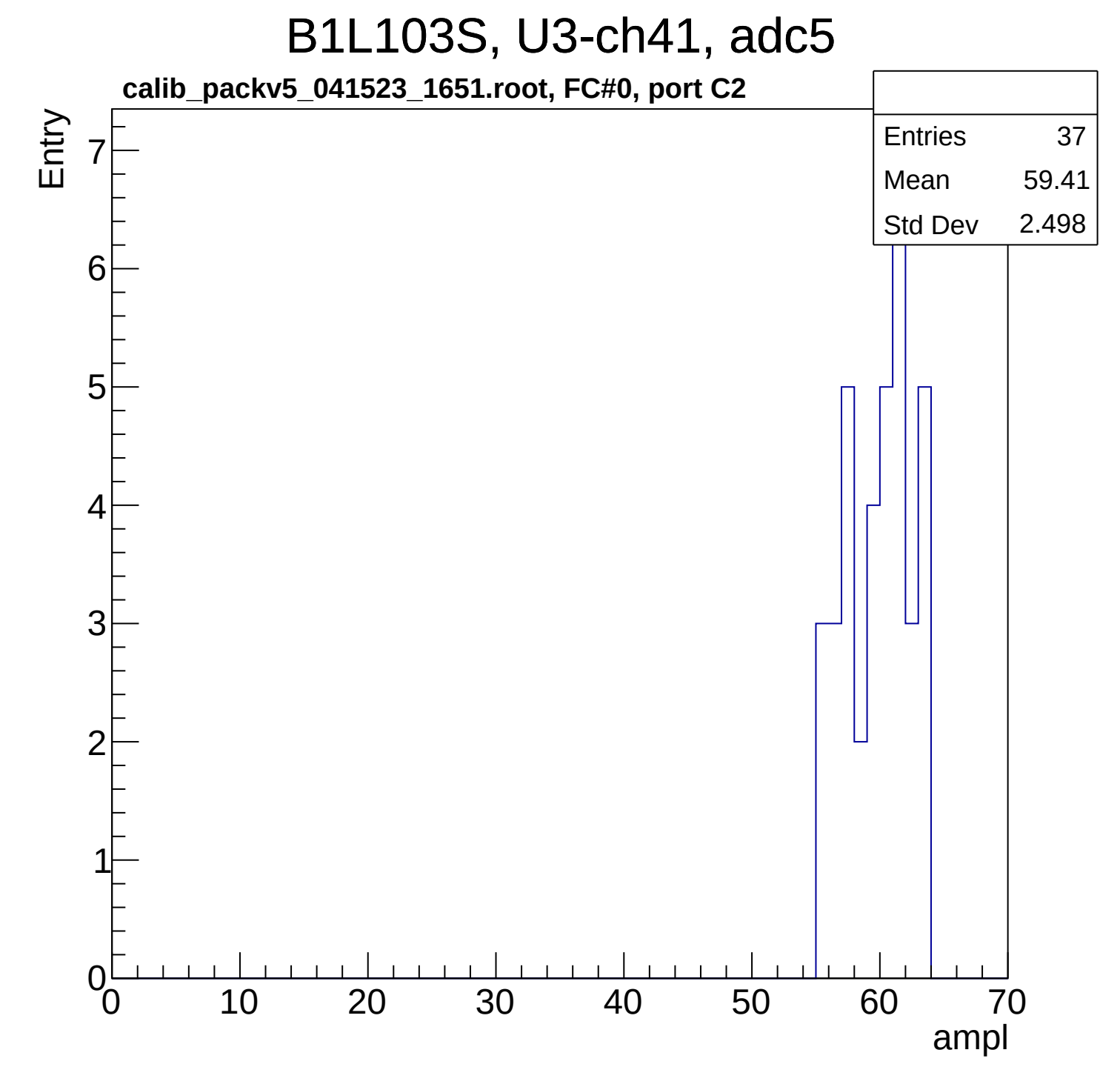
B1L103S, U3-ch41, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 59.41
Std Dev 2.498
Entry
ampl
0
1
2
3
4
5
6
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0
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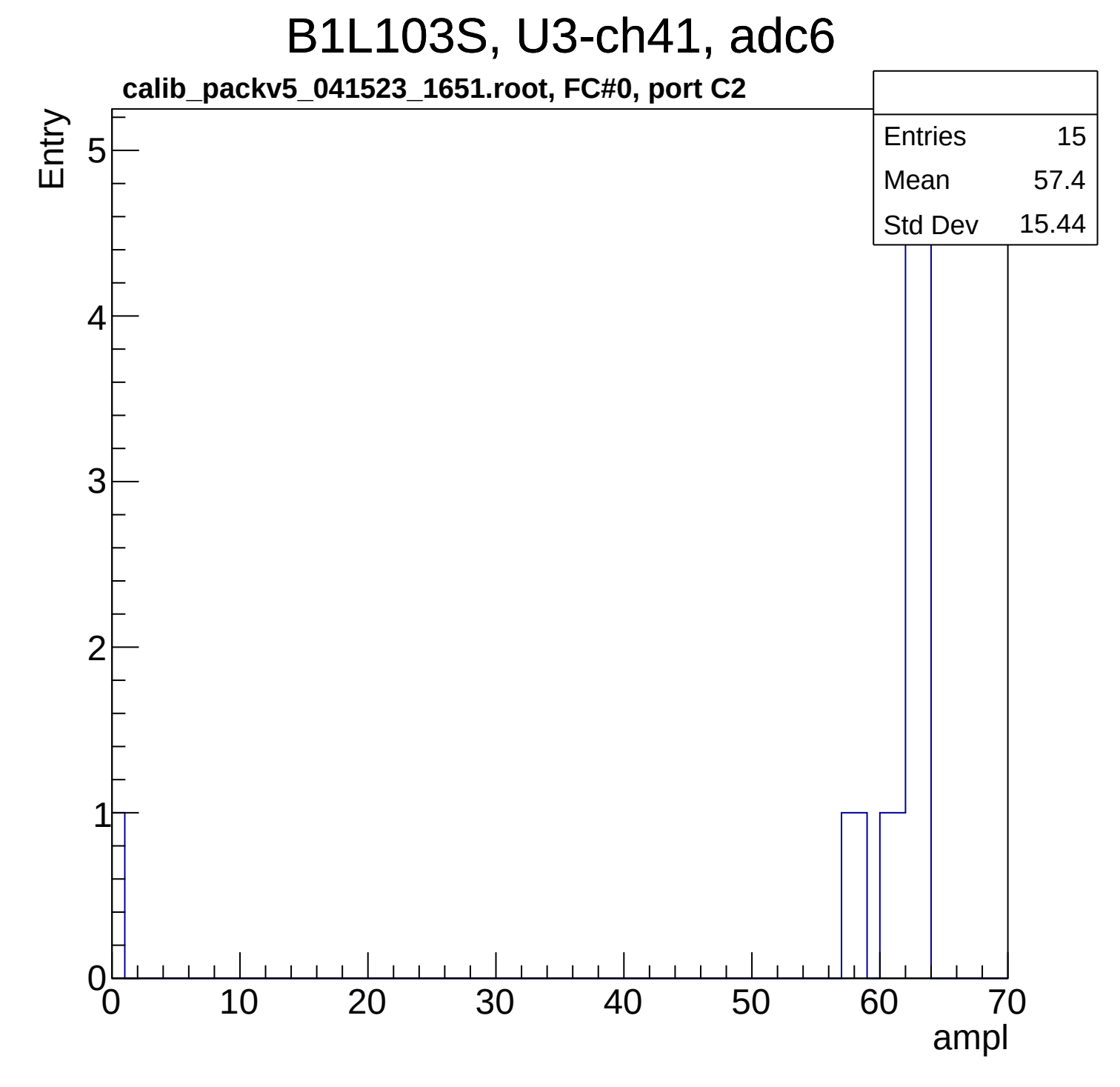
B1L103S, U3-ch41, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 57.4
Std Dev 15.44
Entry
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3
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20
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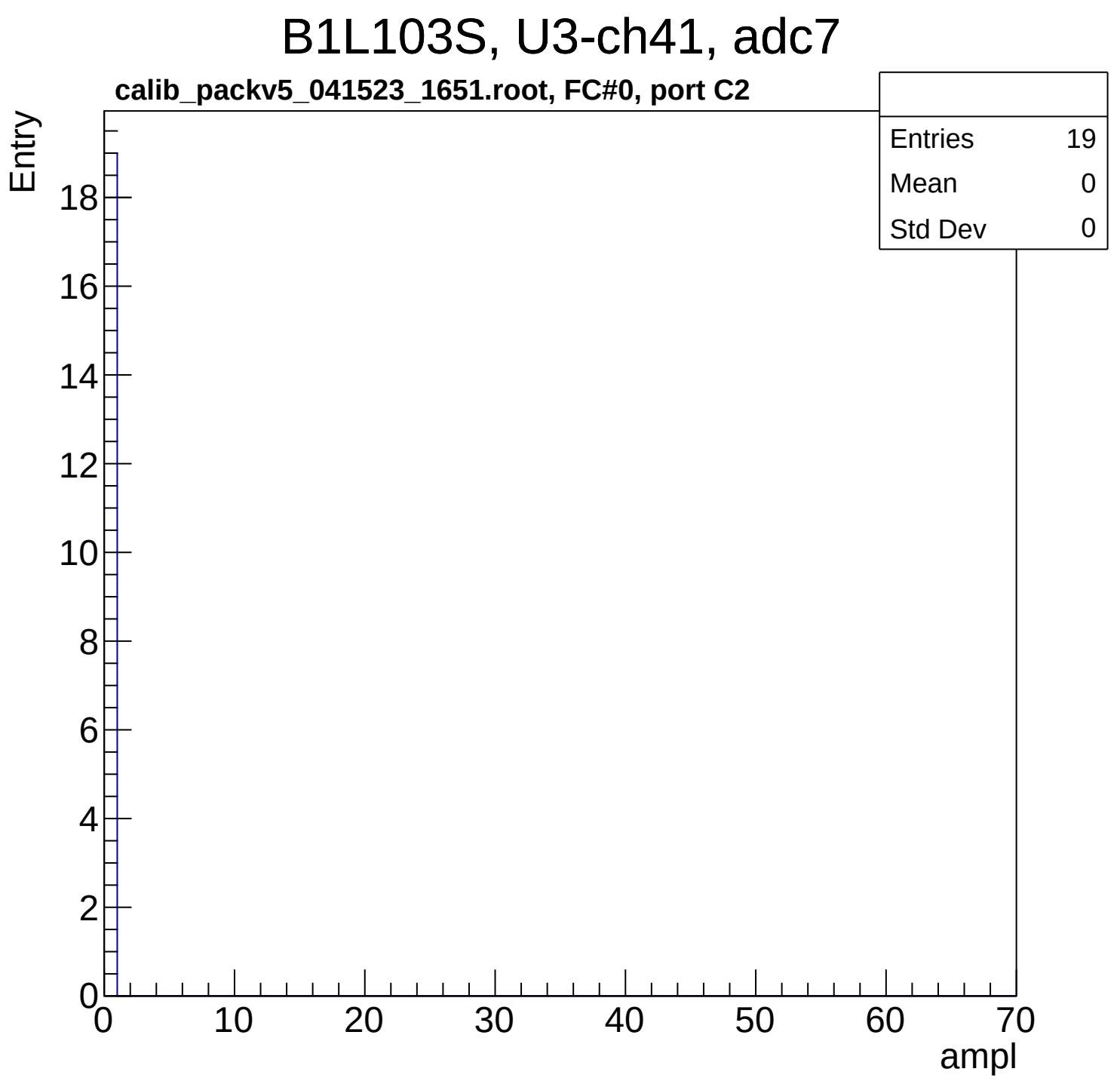
50
60
70
ampl


B1L103S, U3-ch41, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
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6
8
10
12
14
16
18
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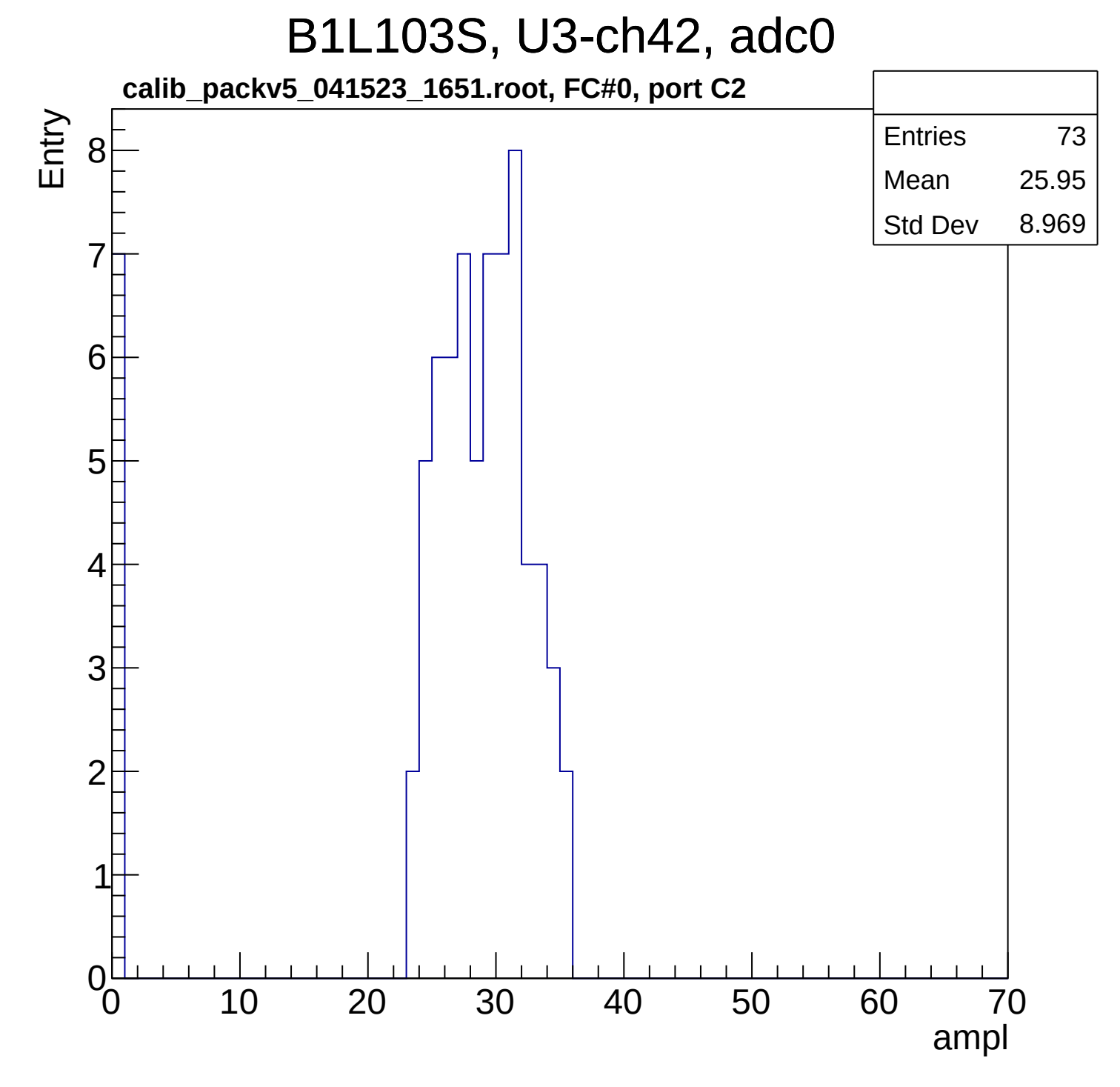
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch42, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 25.95
Std Dev 8.969
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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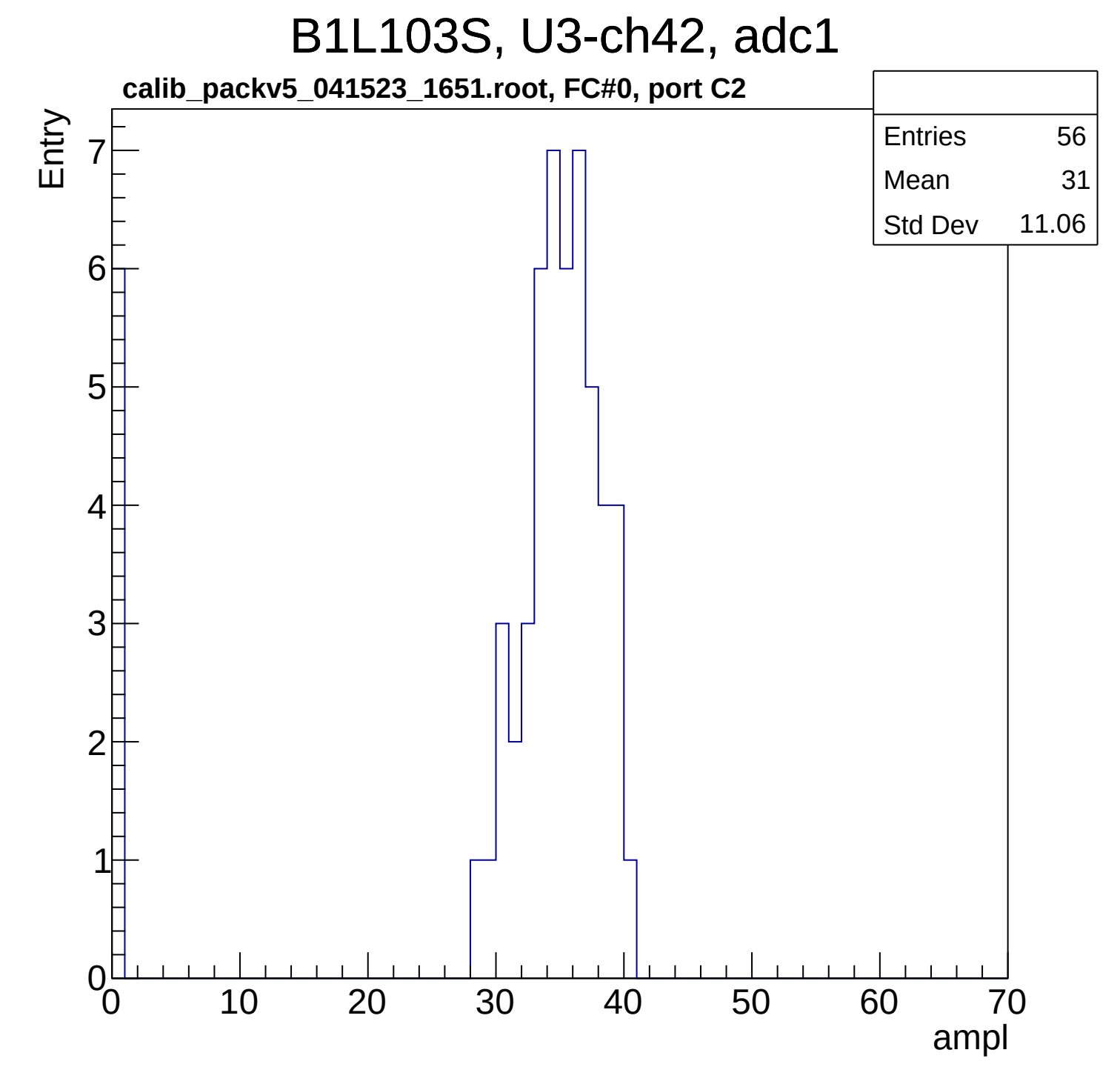
40
50
60
70


B1L103S, U3-ch42, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 31
Std Dev 11.06
Entry
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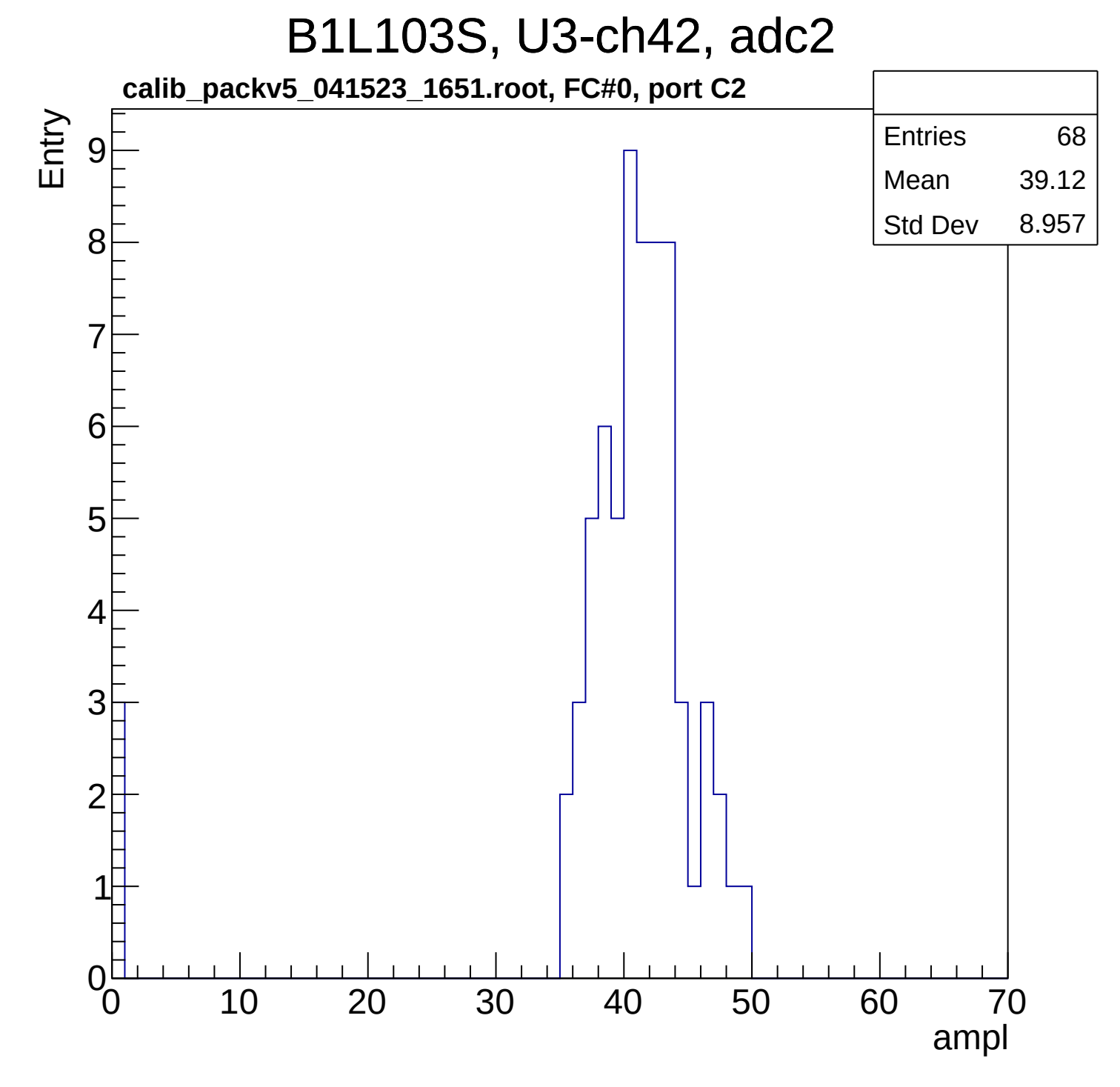
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch42, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 39.12
Std Dev 8.957
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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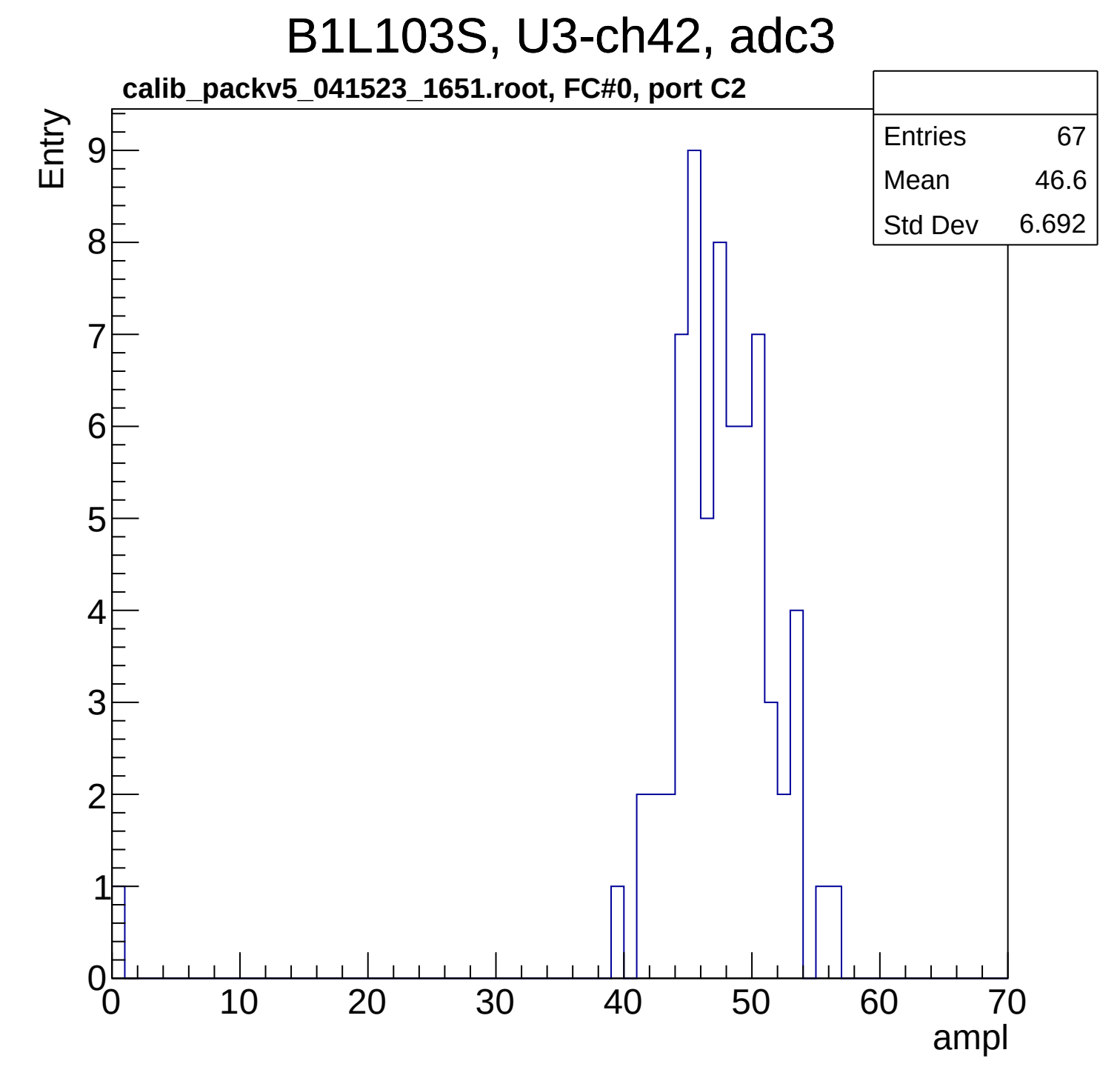
B1L103S, U3-ch42, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 46.6
Std Dev 6.692
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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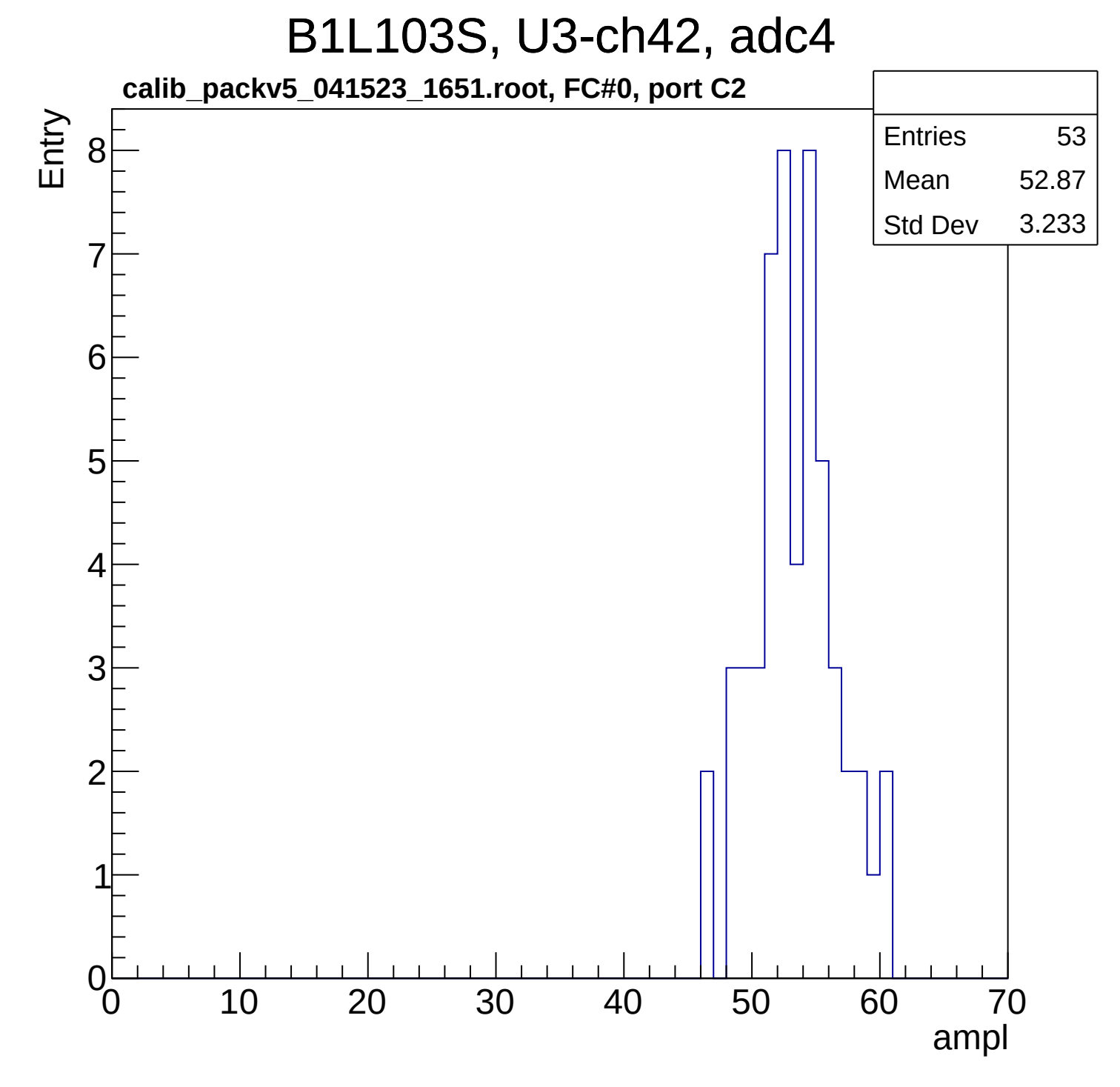
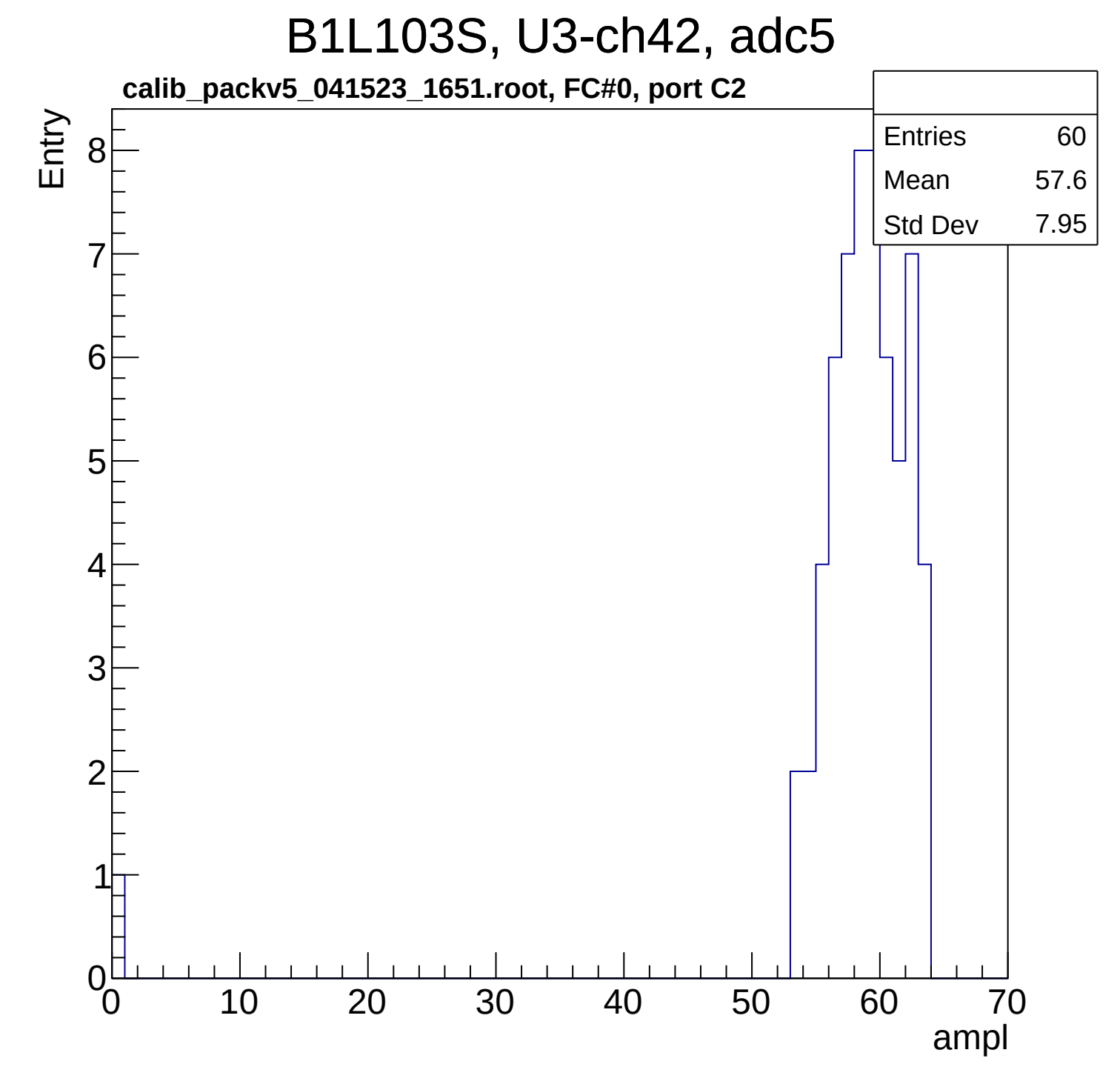
60
70


B1L103S, U3-ch42, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 52.87
Std Dev 3.233
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch42, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 57.6
Std Dev 7.95
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
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60
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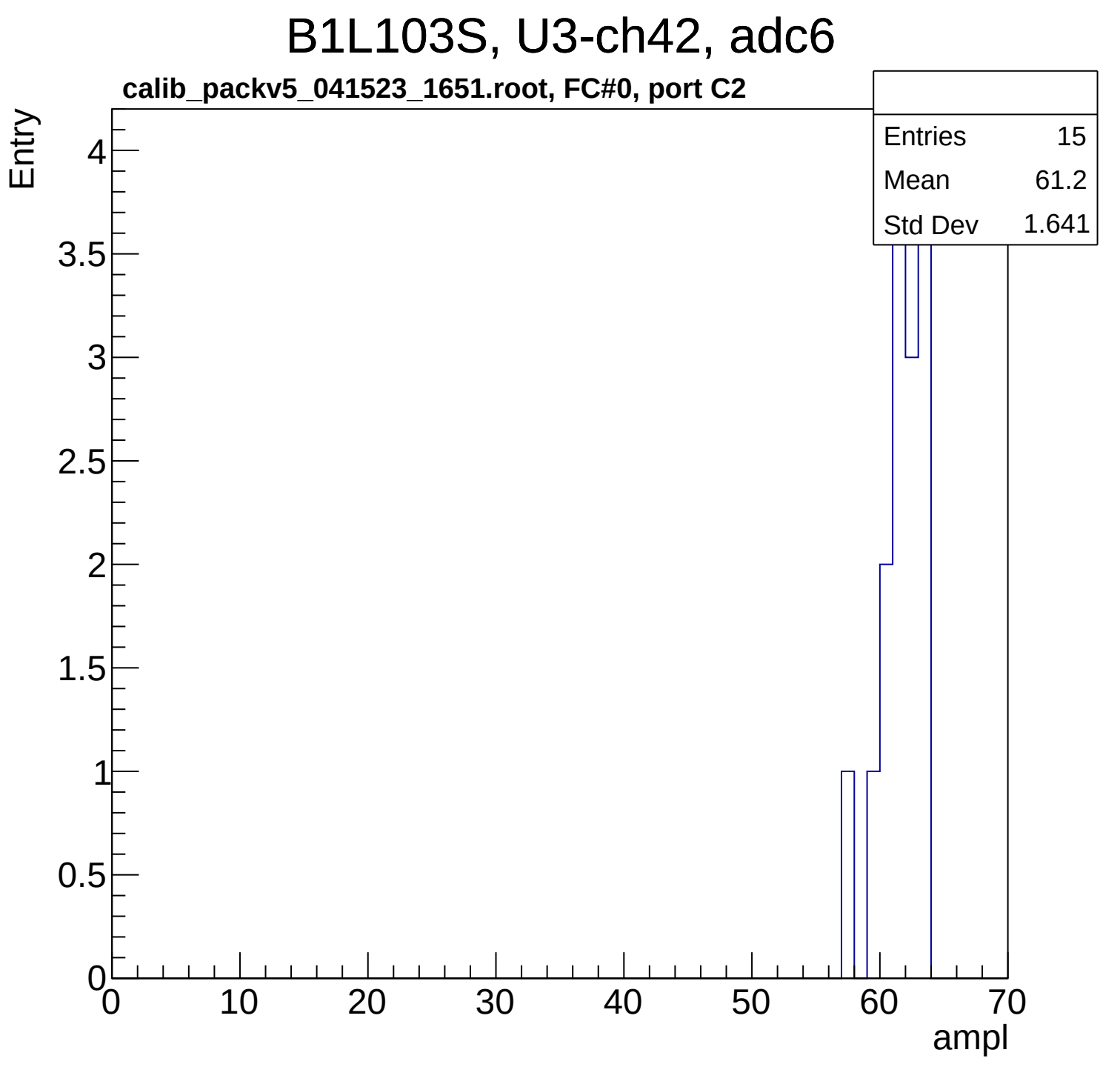
B1L103S, U3-ch42, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 61.2
Std Dev 1.641
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
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20
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40
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60
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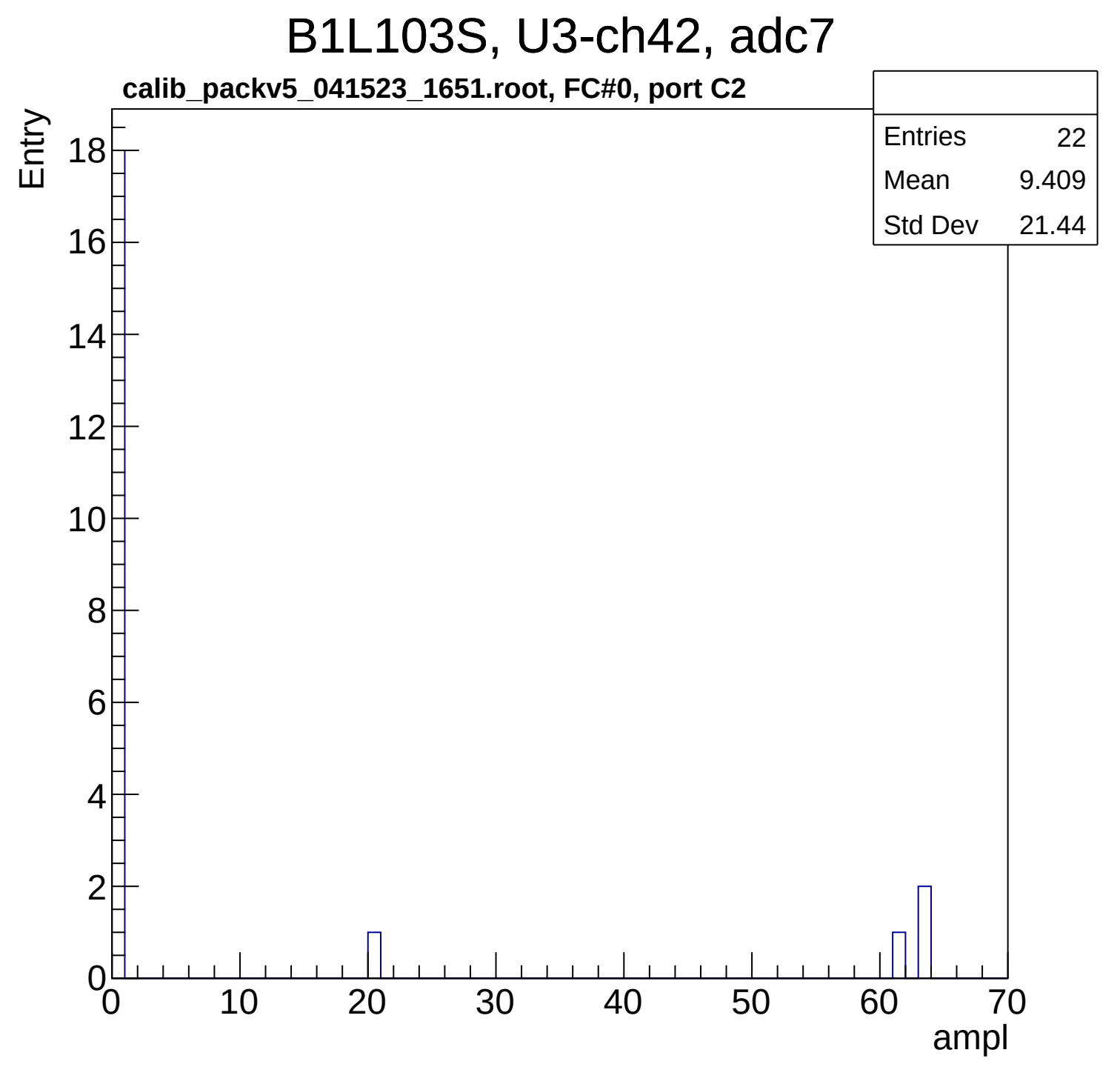
B1L103S, U3-ch42, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 9.409
Std Dev 21.44
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
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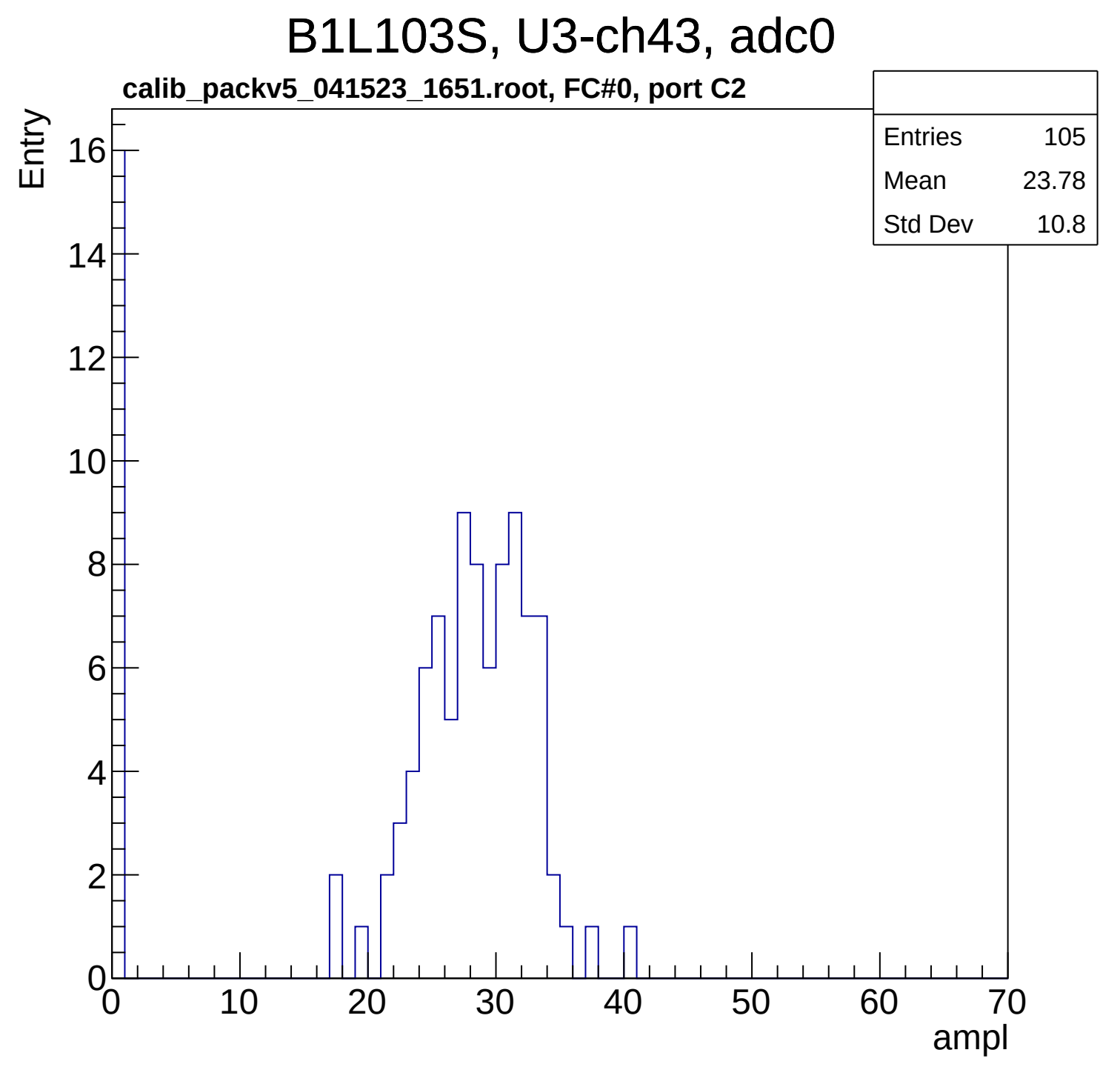
40
50
60
70
ampl


B1L103S, U3-ch43, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 105
Mean 23.78
Std Dev 10.8
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
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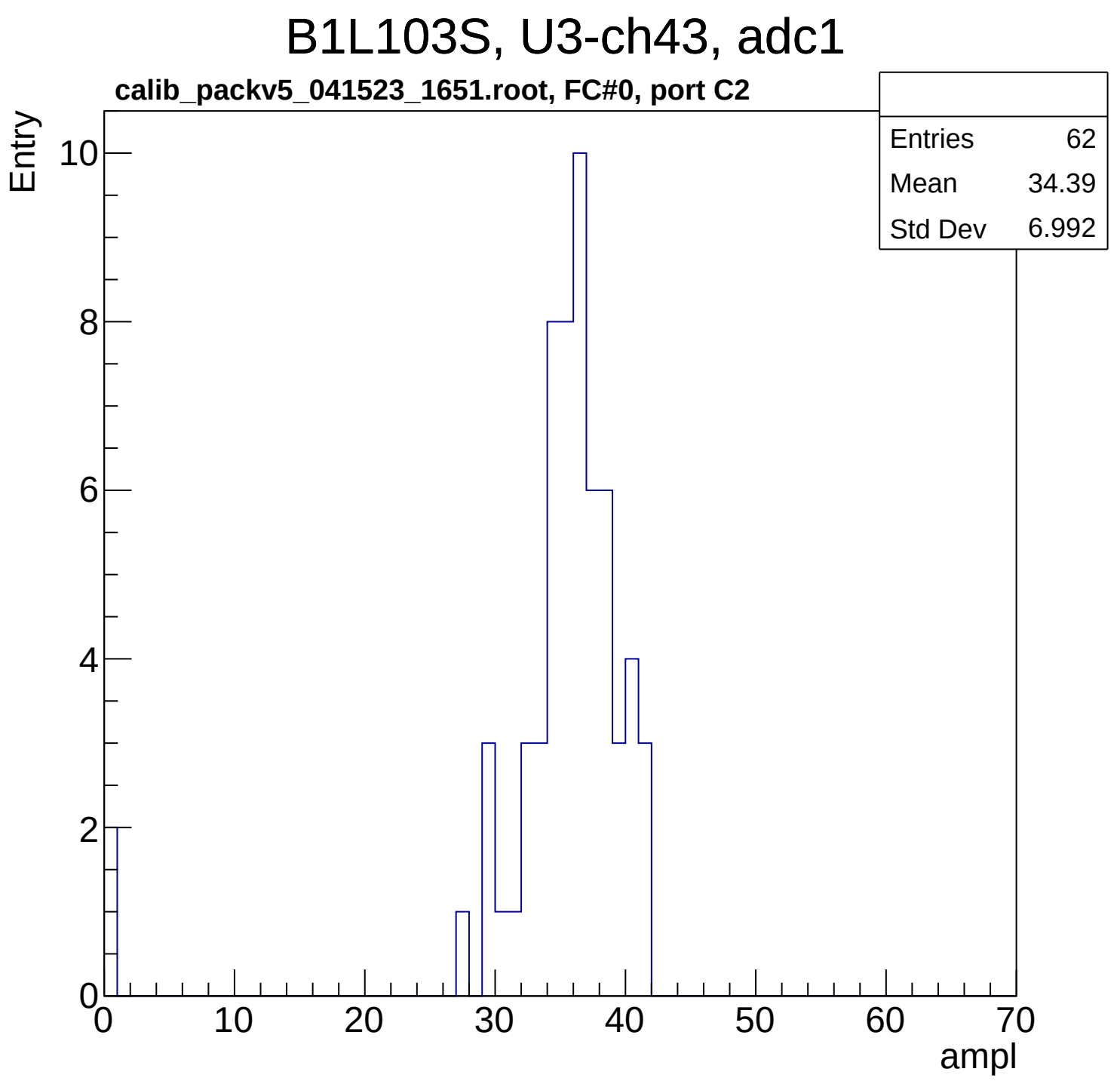
B1L103S, U3-ch43, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 34.39
Std Dev 6.992
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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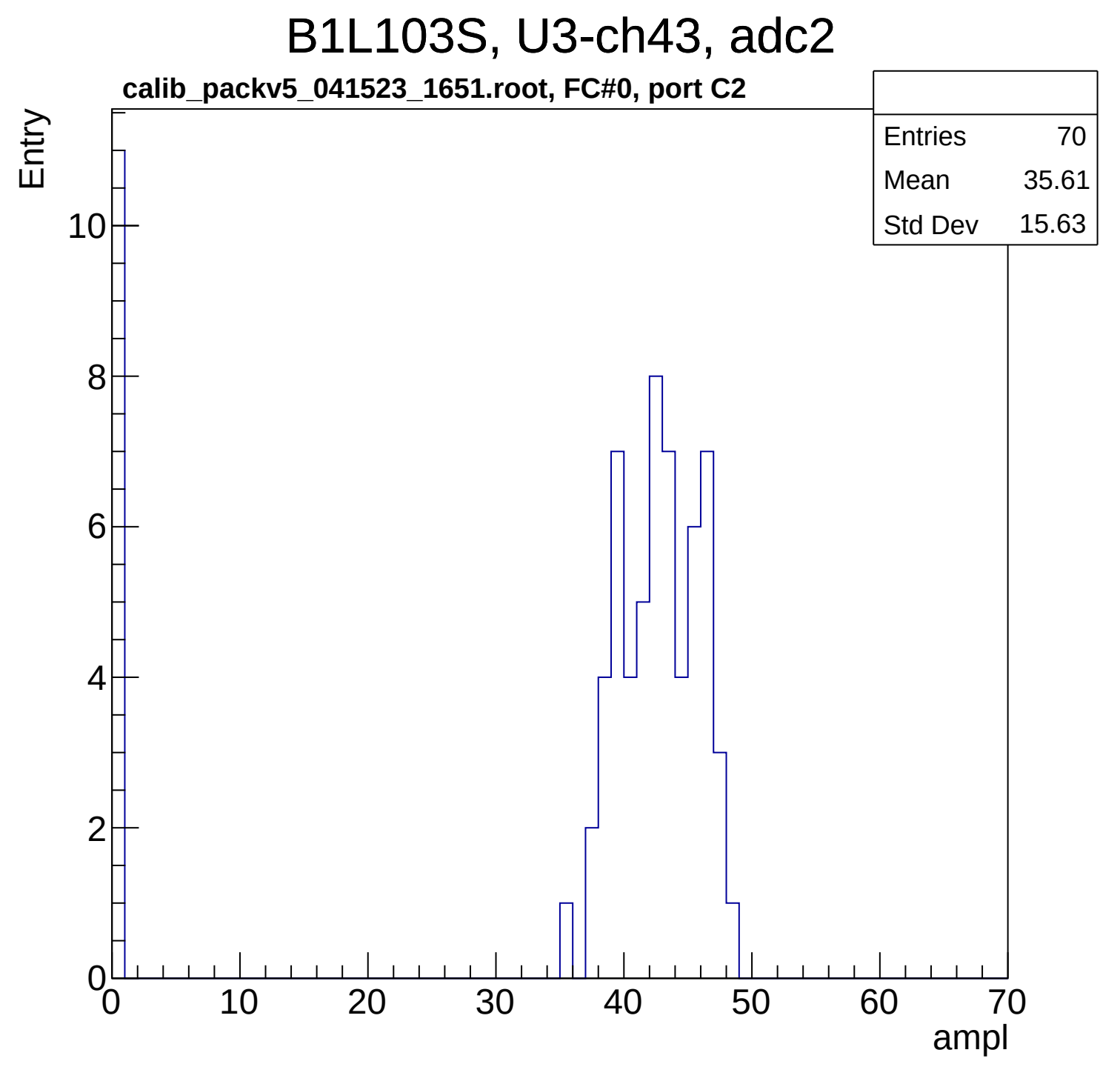
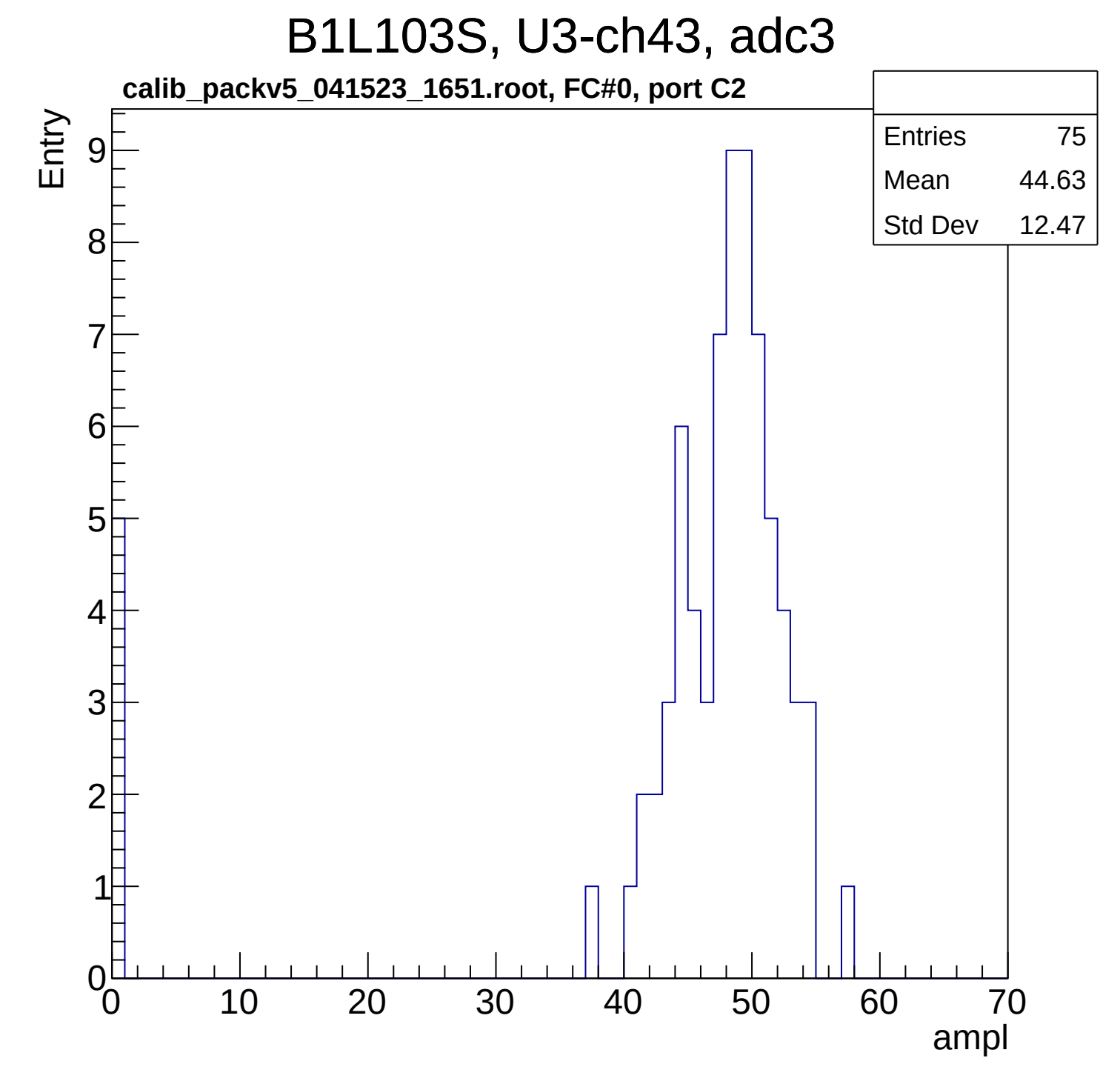
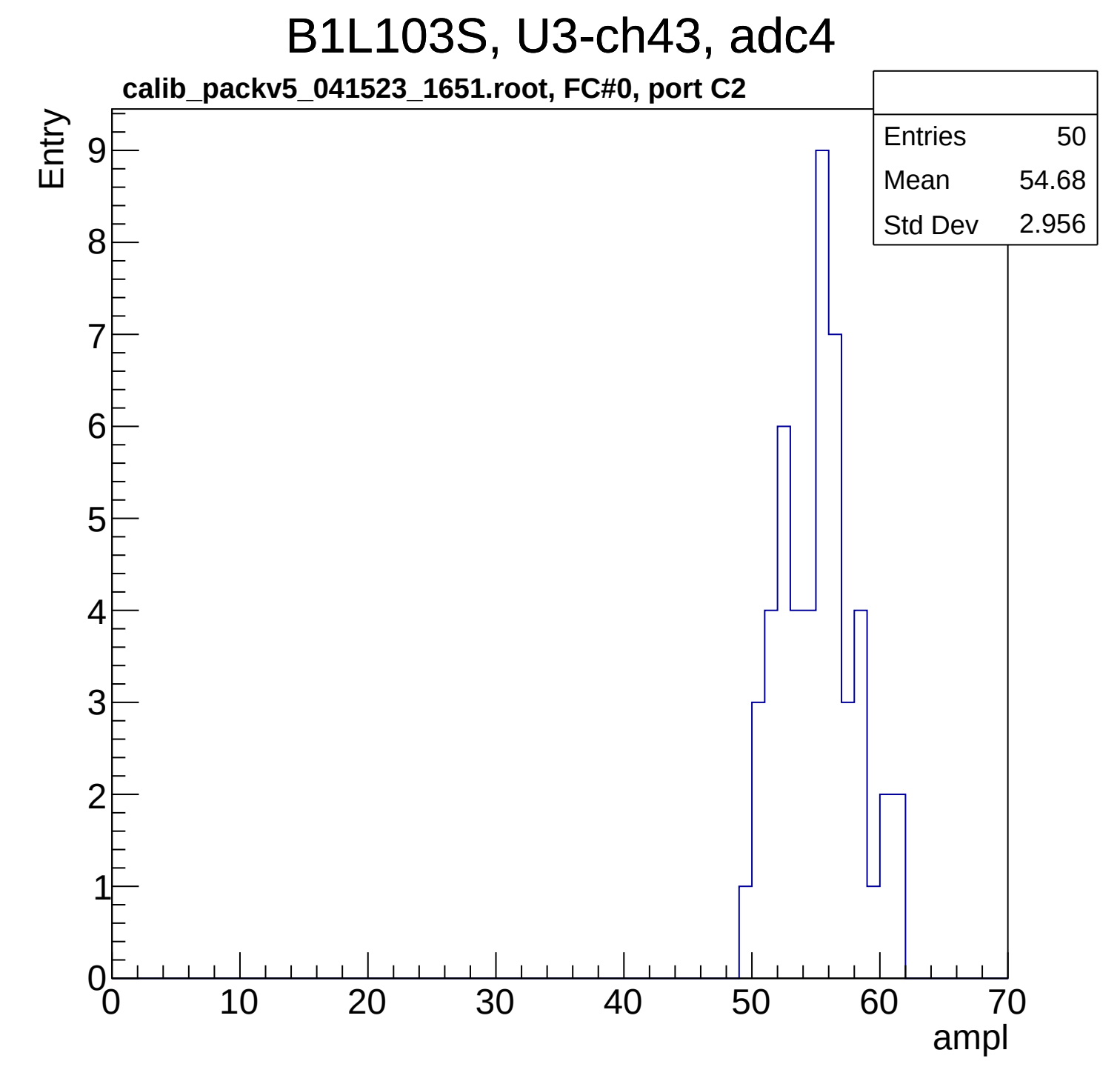

B1L103S, U3-ch43, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 35.61
Std Dev 15.63
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch43, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 44.63
Std Dev 12.47
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch43, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 54.68
Std Dev 2.956
Entry
ampl
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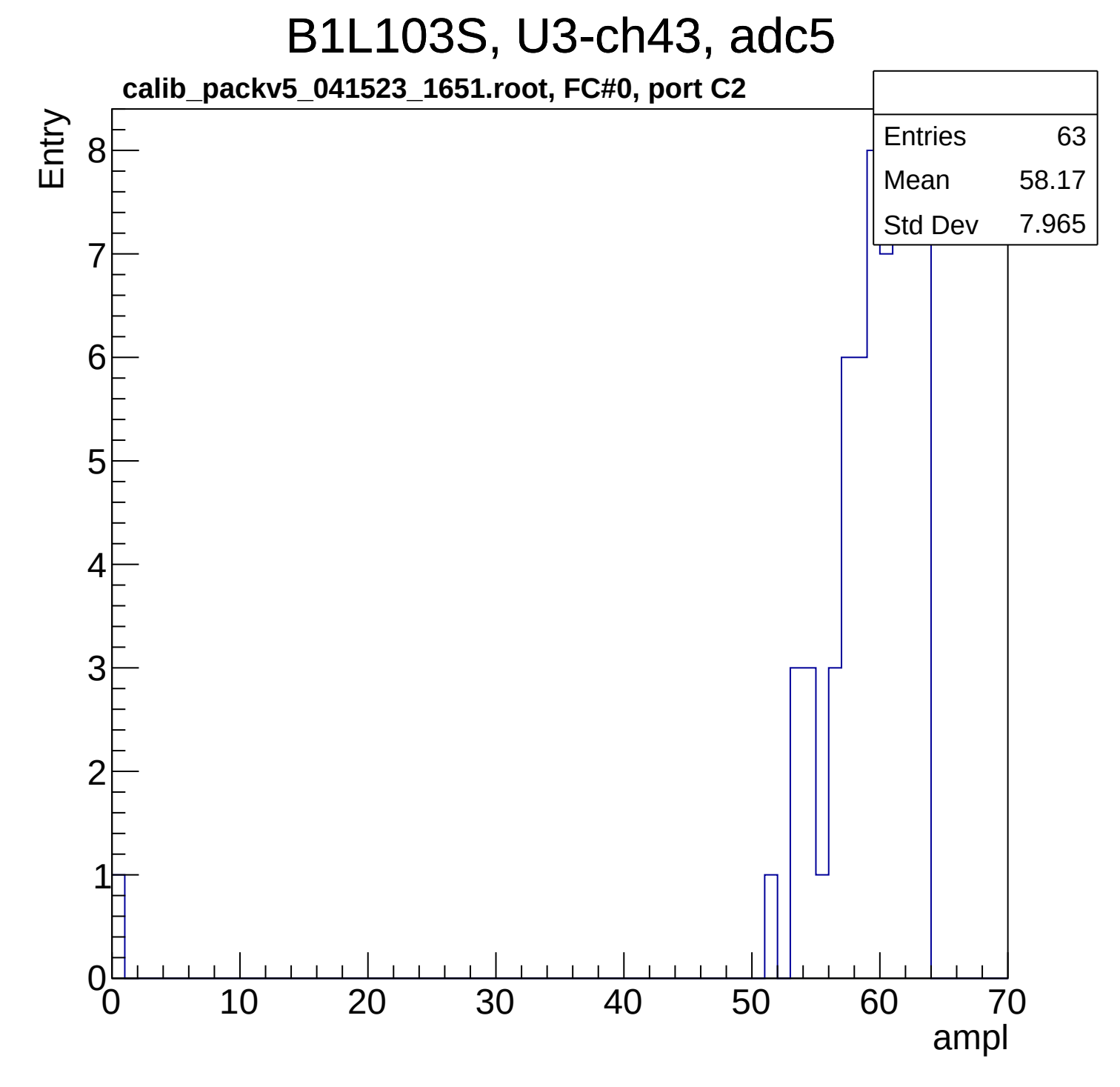
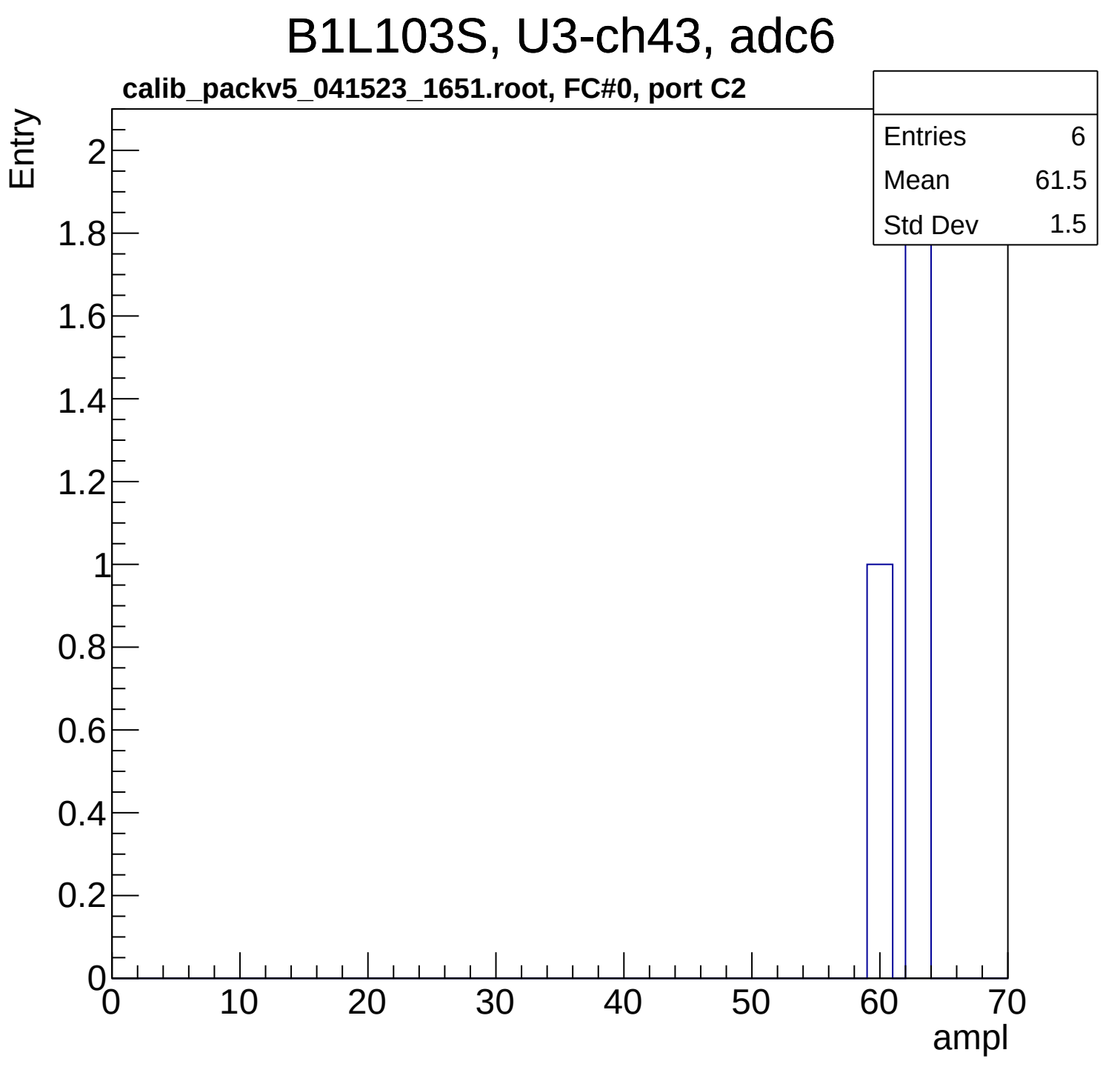
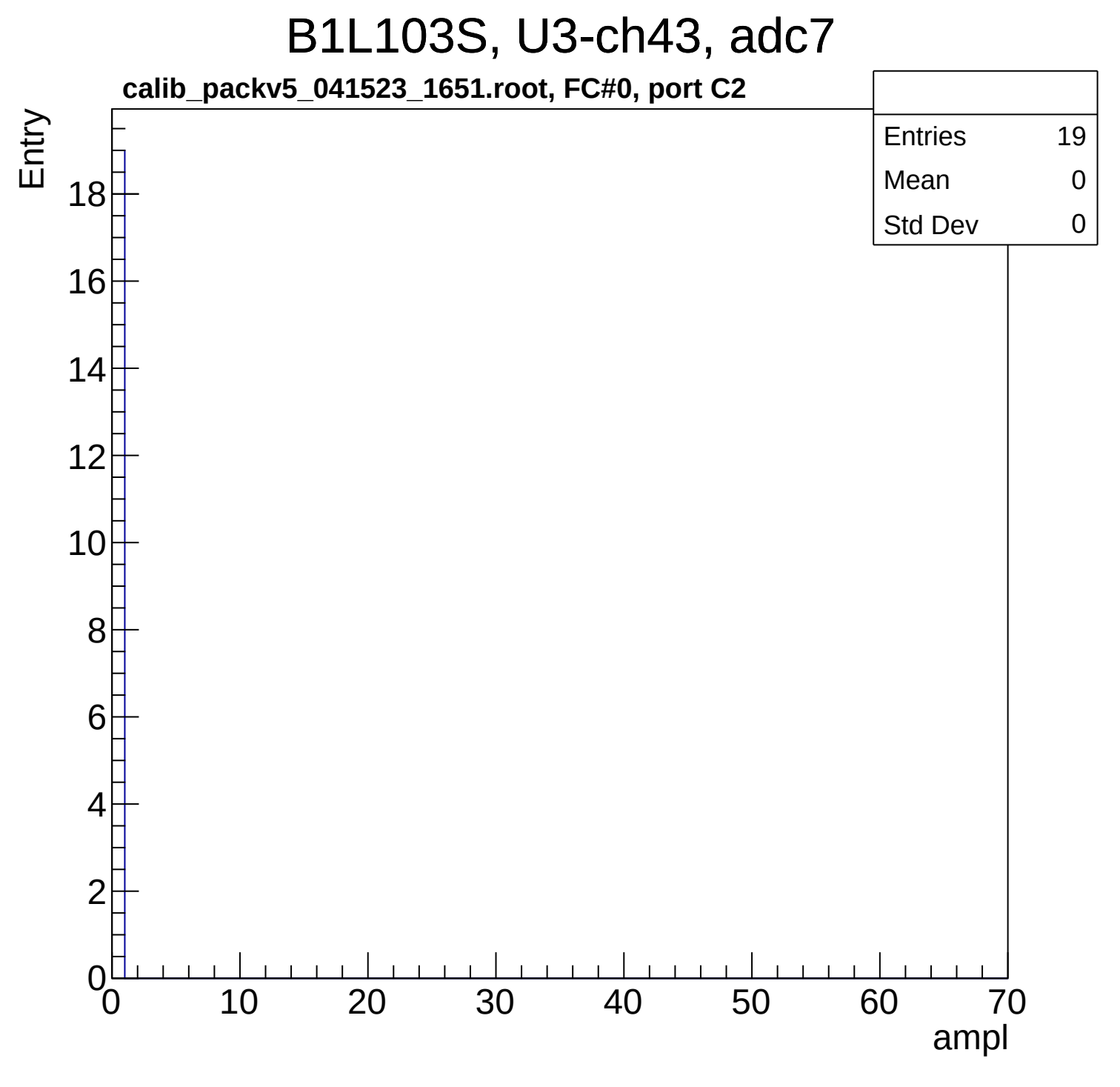
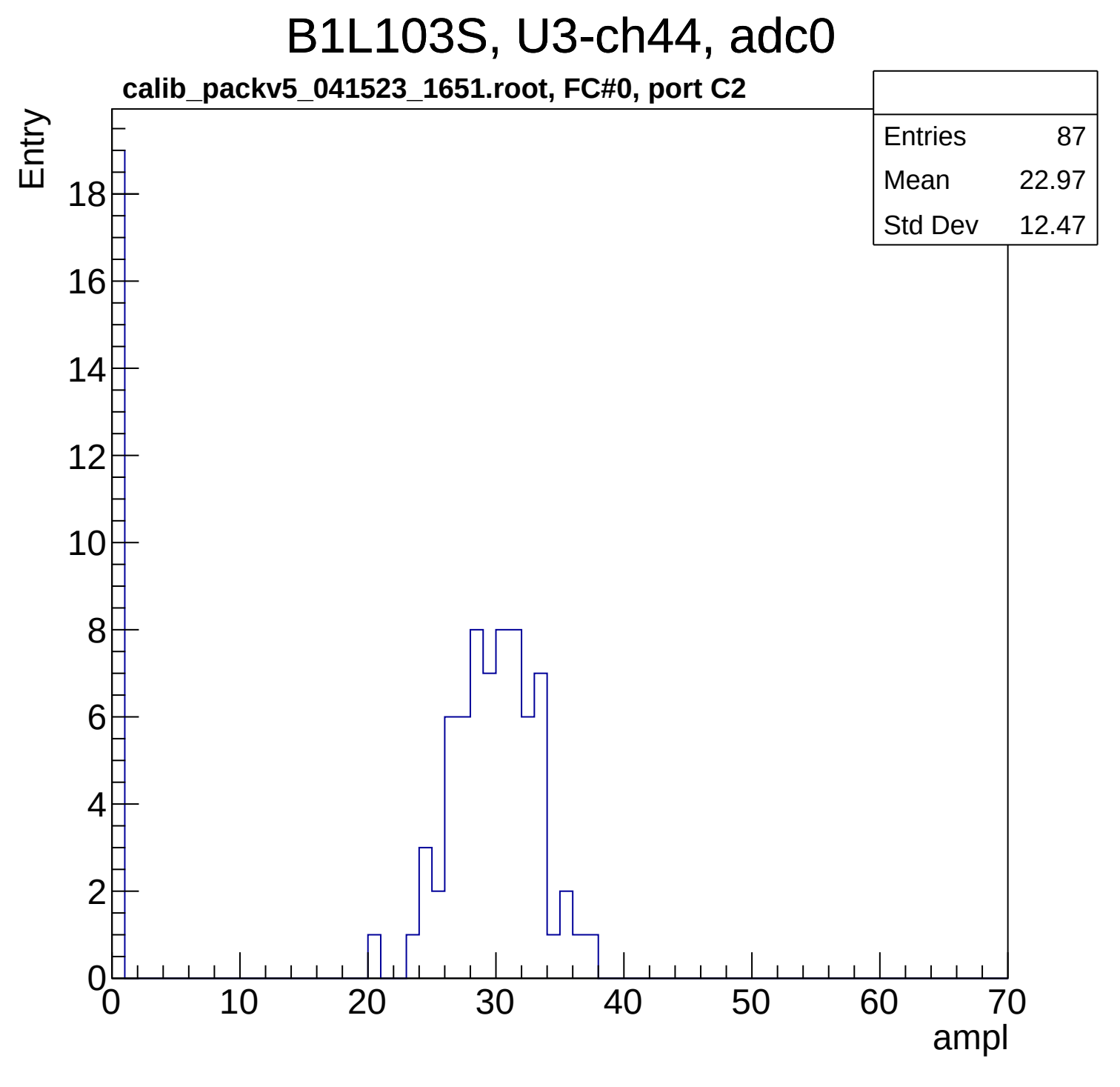
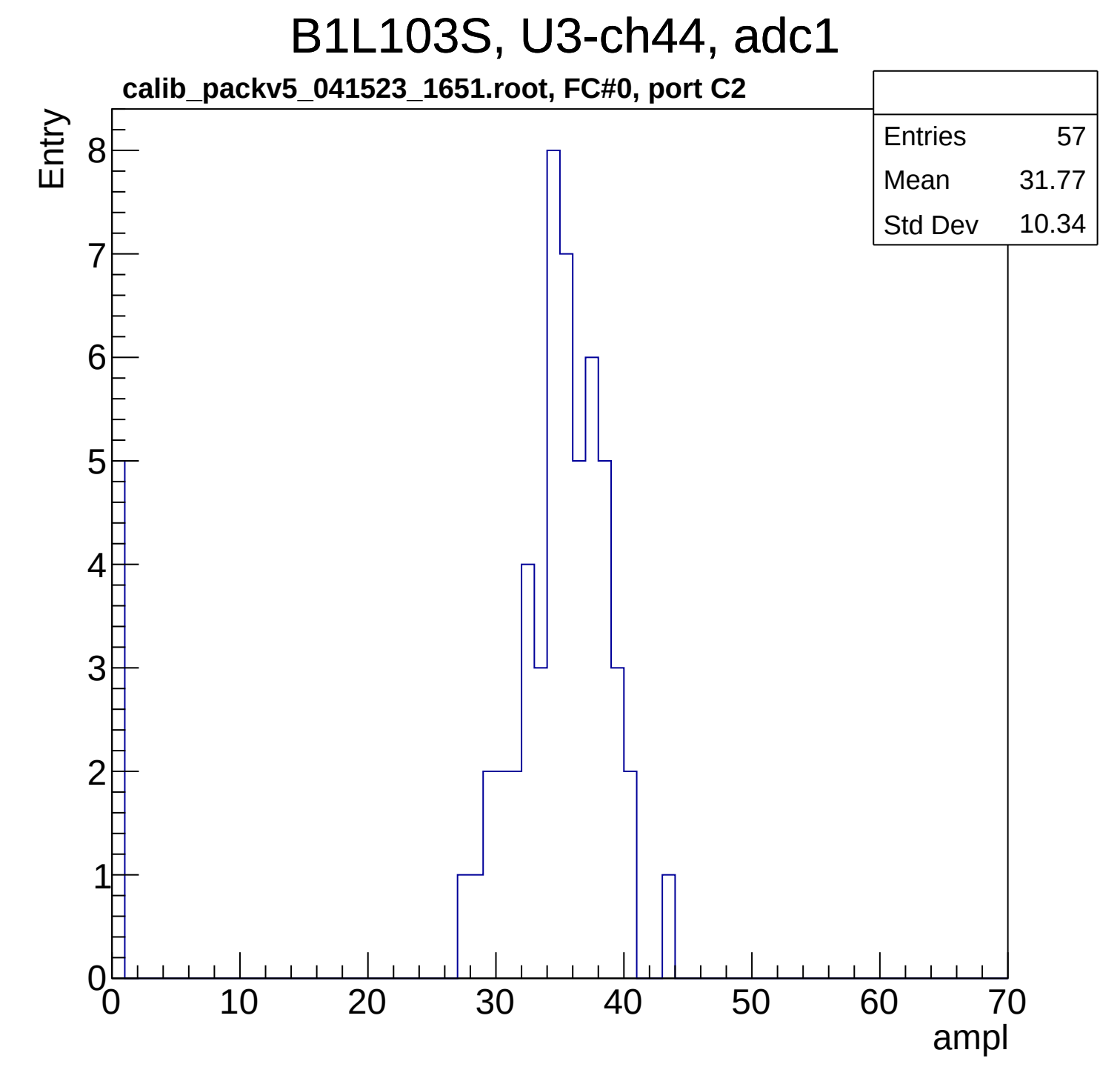
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

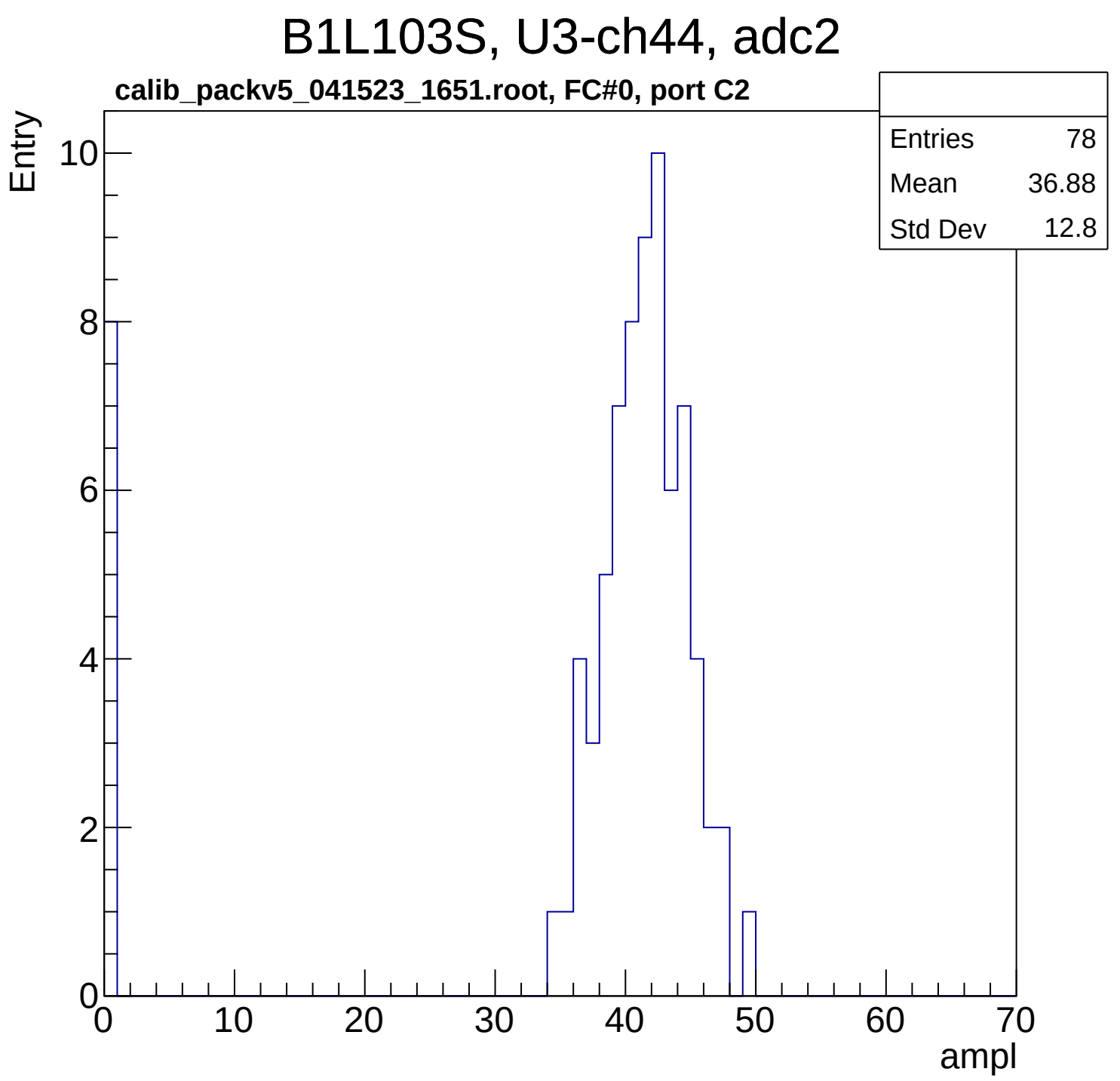

B1L103S, U3-ch43, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 58.17
Std Dev 7.965
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

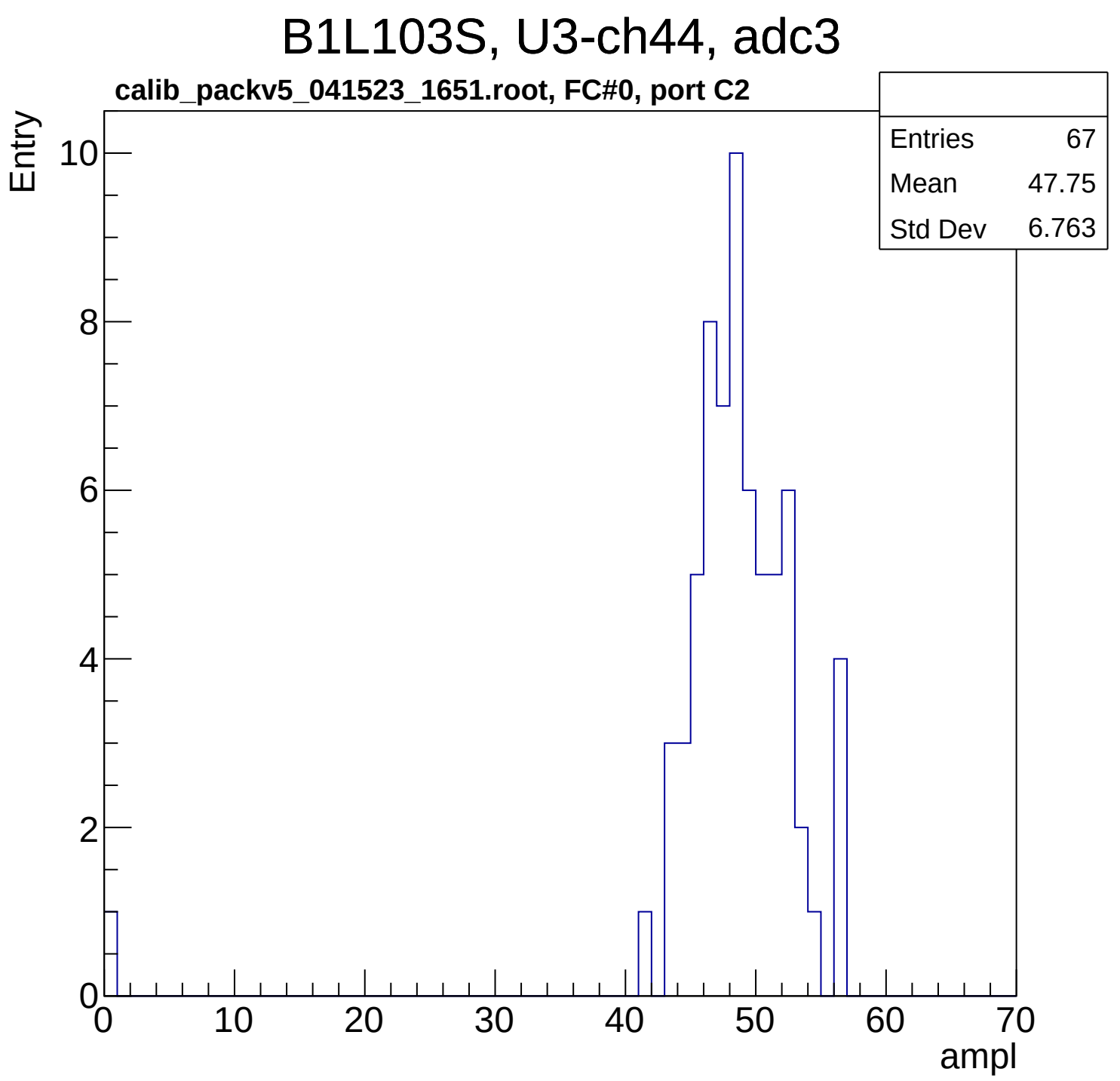

B1L103S, U3-ch43, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 61.5
Std Dev 1.5
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

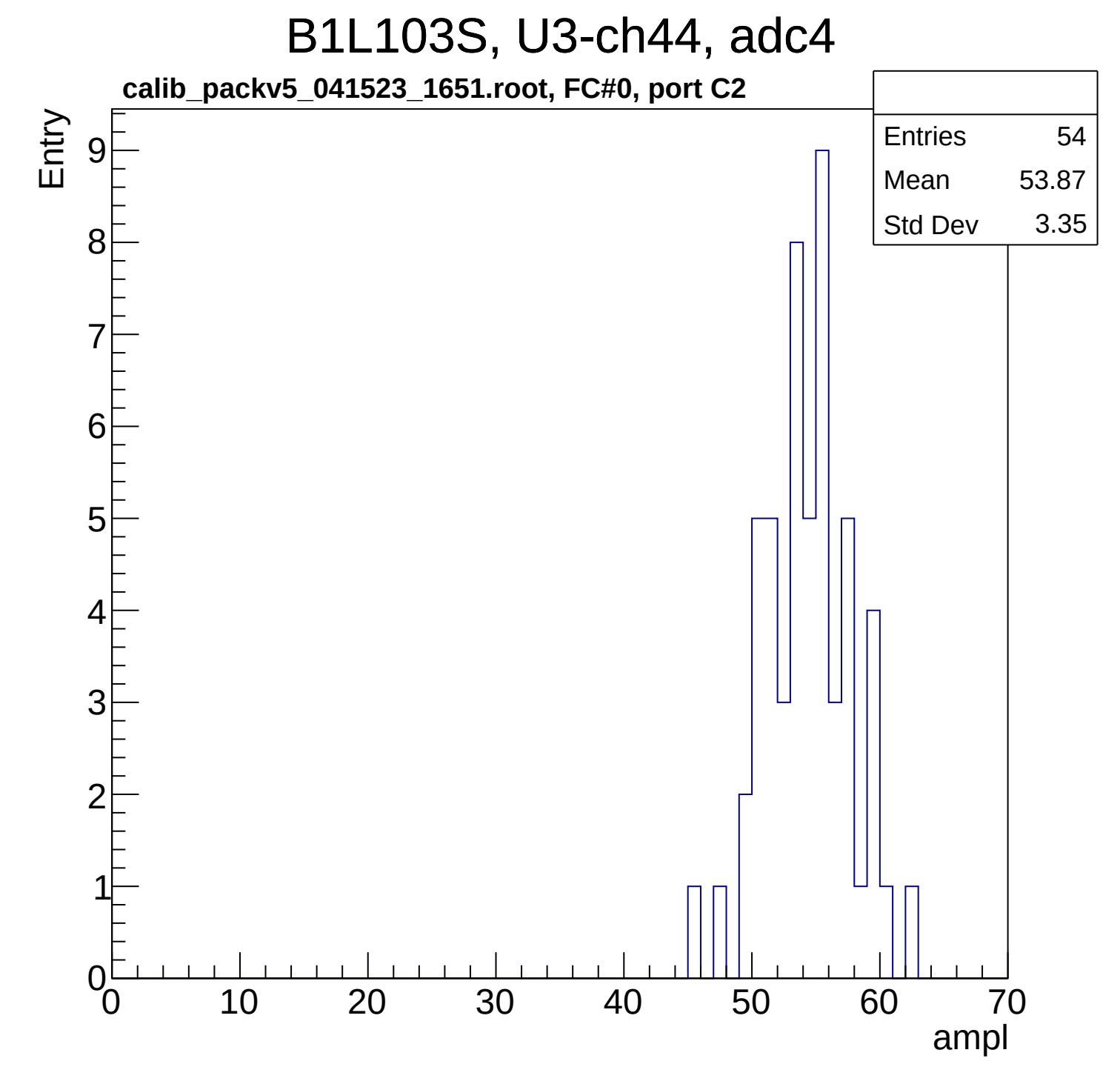

B1L103S, U3-ch43, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch44, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 22.97
Std Dev 12.47
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch44, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 31.77
Std Dev 10.34
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch44, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 36.88
Std Dev 12.8
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch44, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 47.75
Std Dev 6.763
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch44, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 53.87
Std Dev 3.35
Entry
ampl
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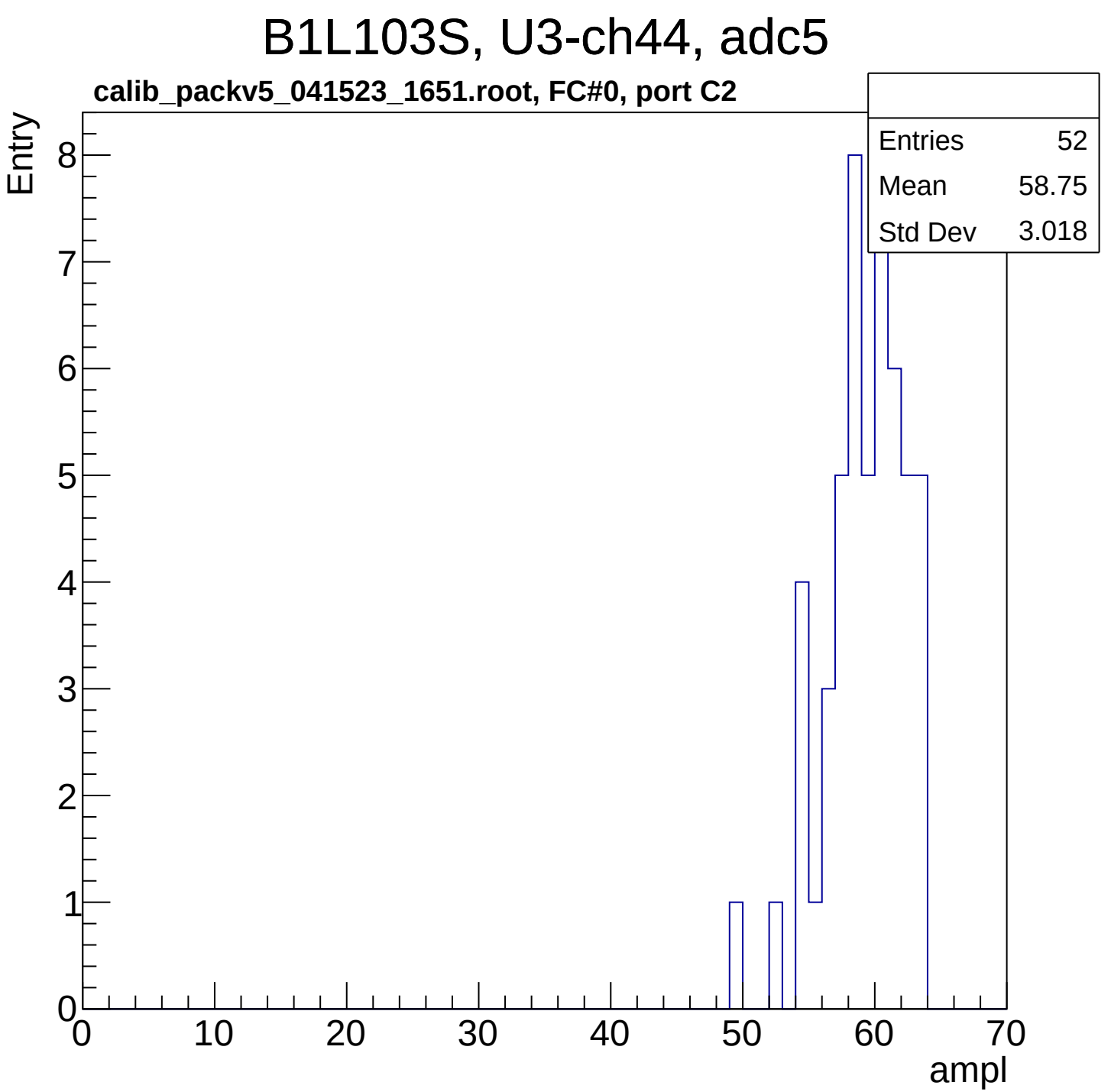
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch44, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 58.75
Std Dev 3.018
Entry
ampl
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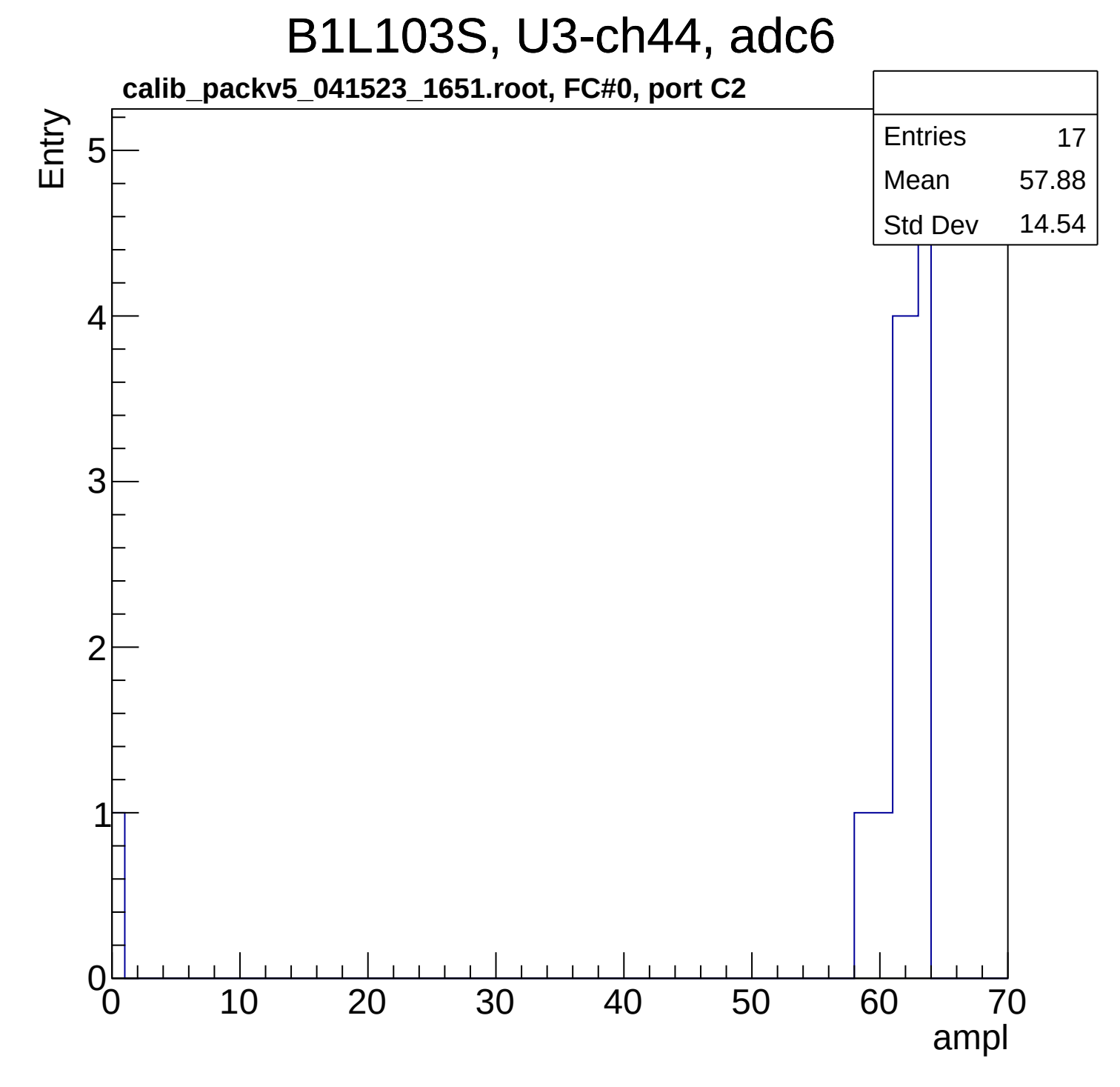
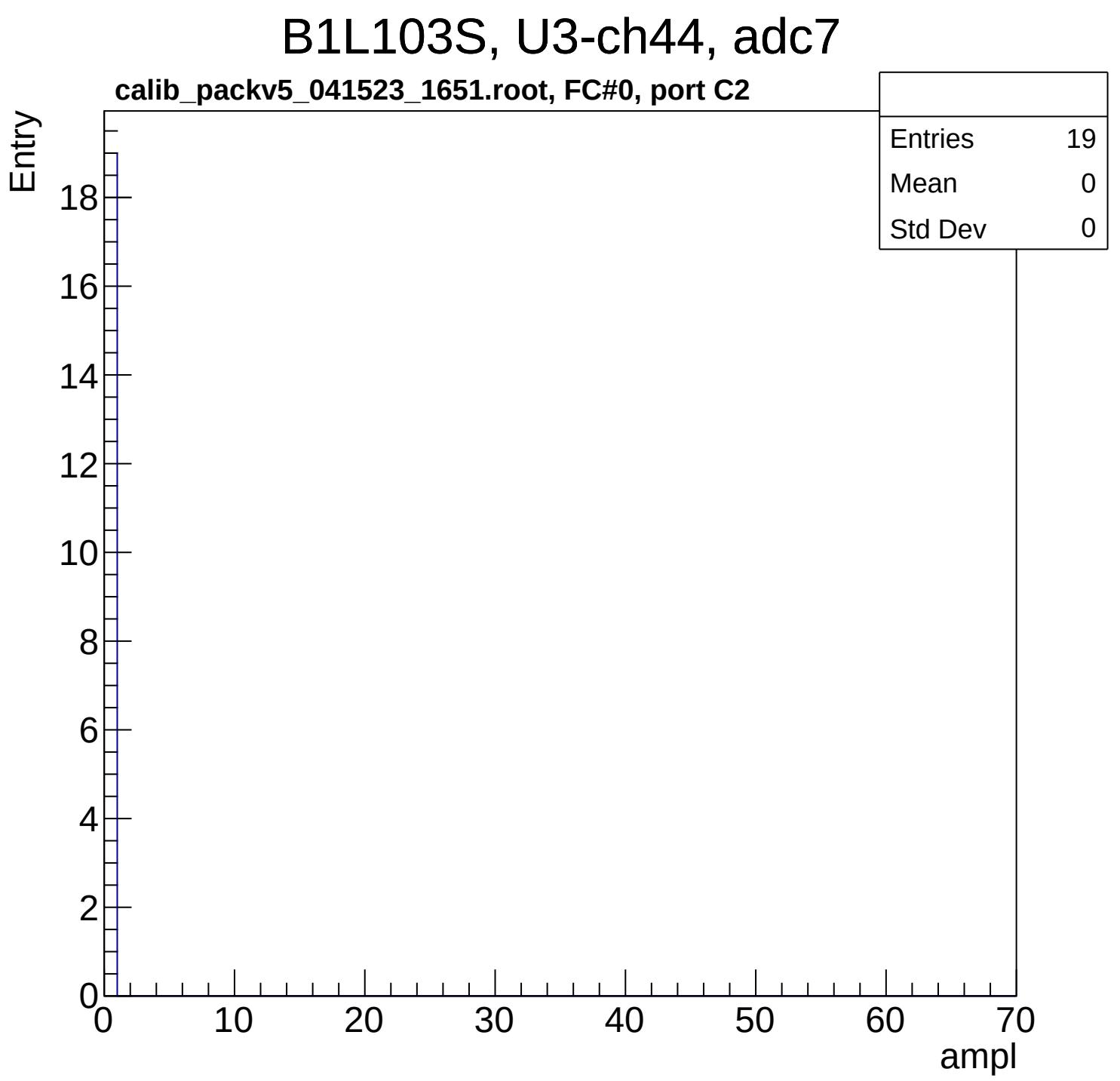
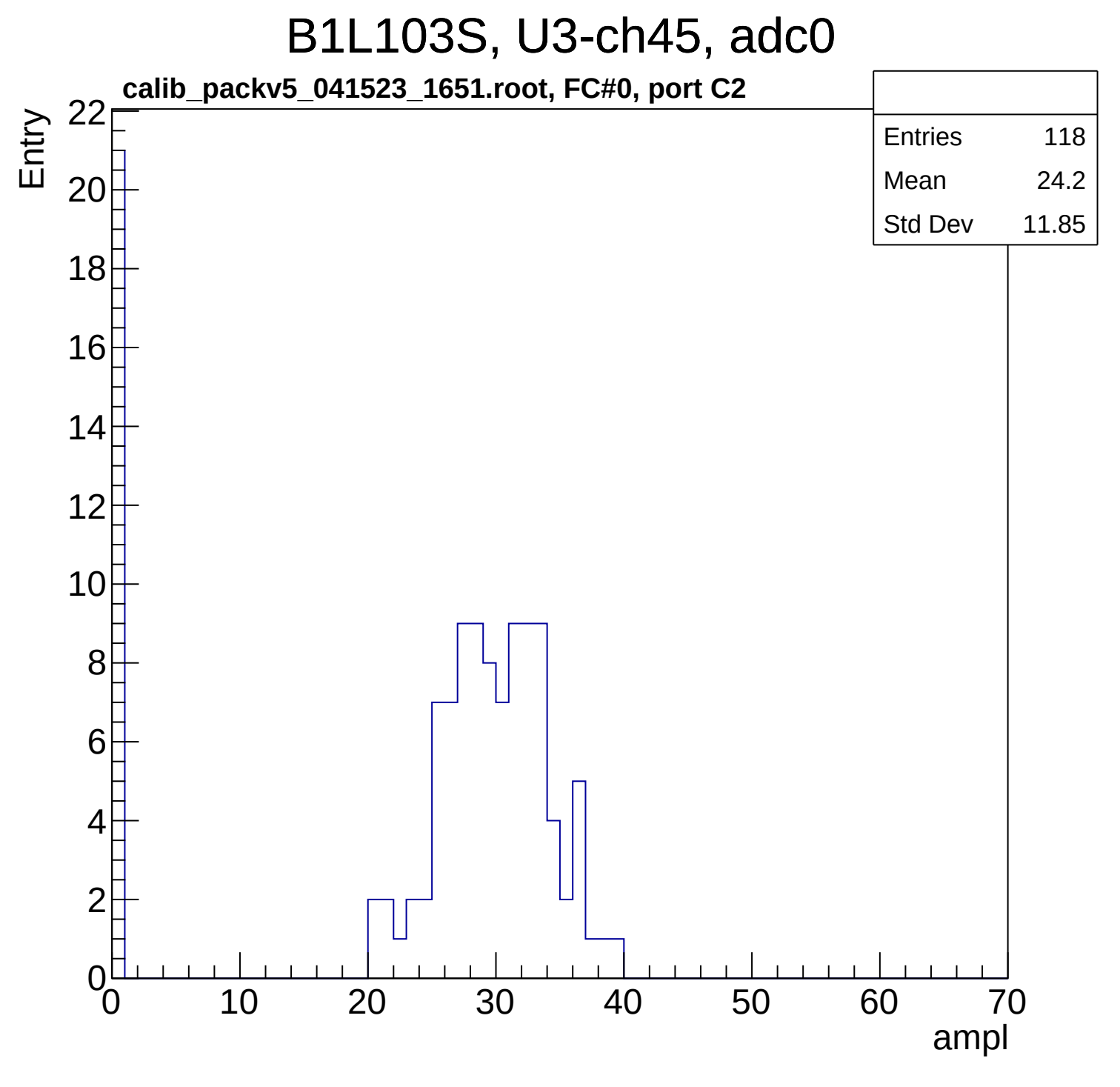
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch44, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 57.88
Std Dev 14.54
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U3-ch44, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch45, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 118
Mean 24.2
Std Dev 11.85
Entry
ampl
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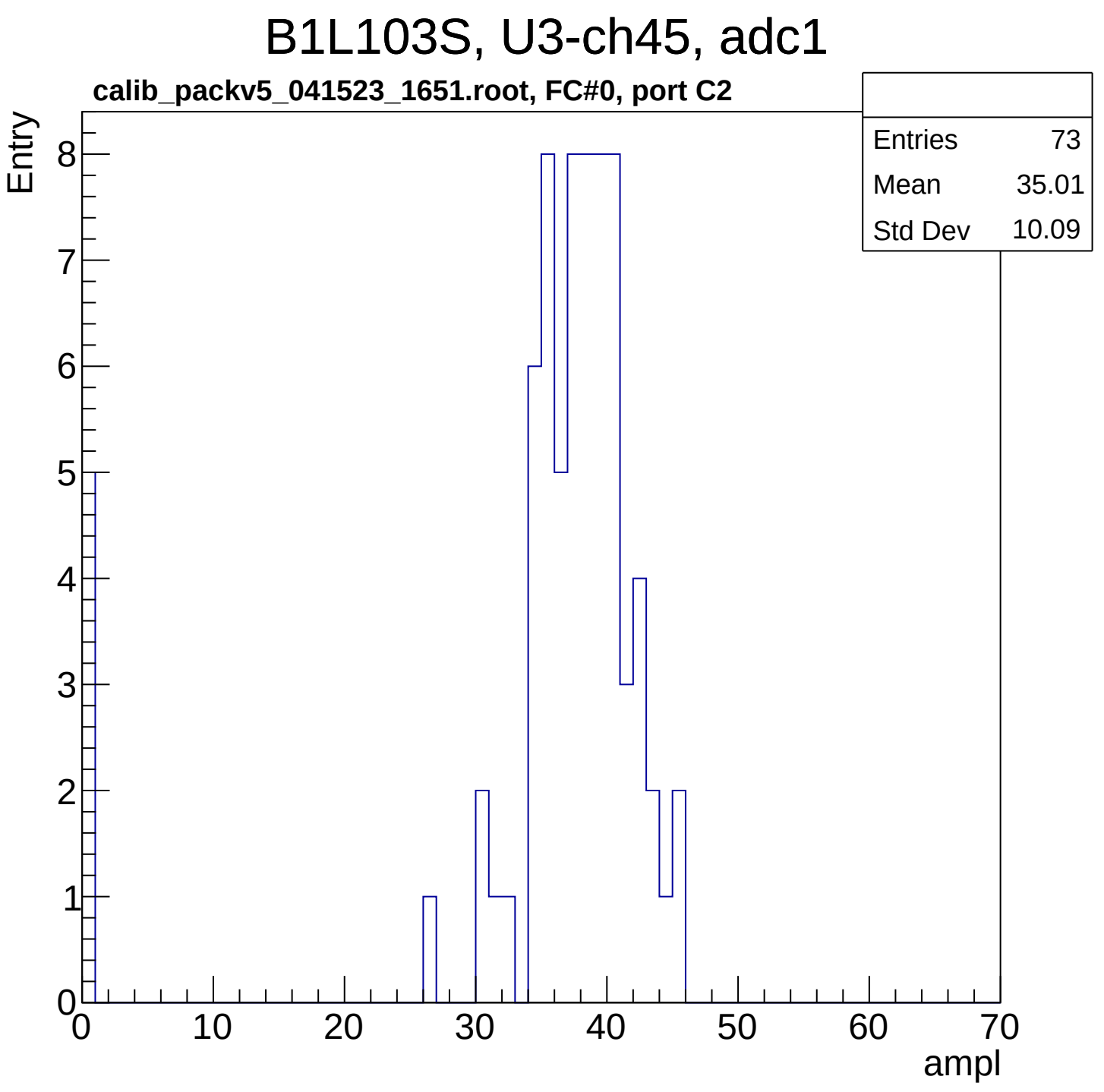
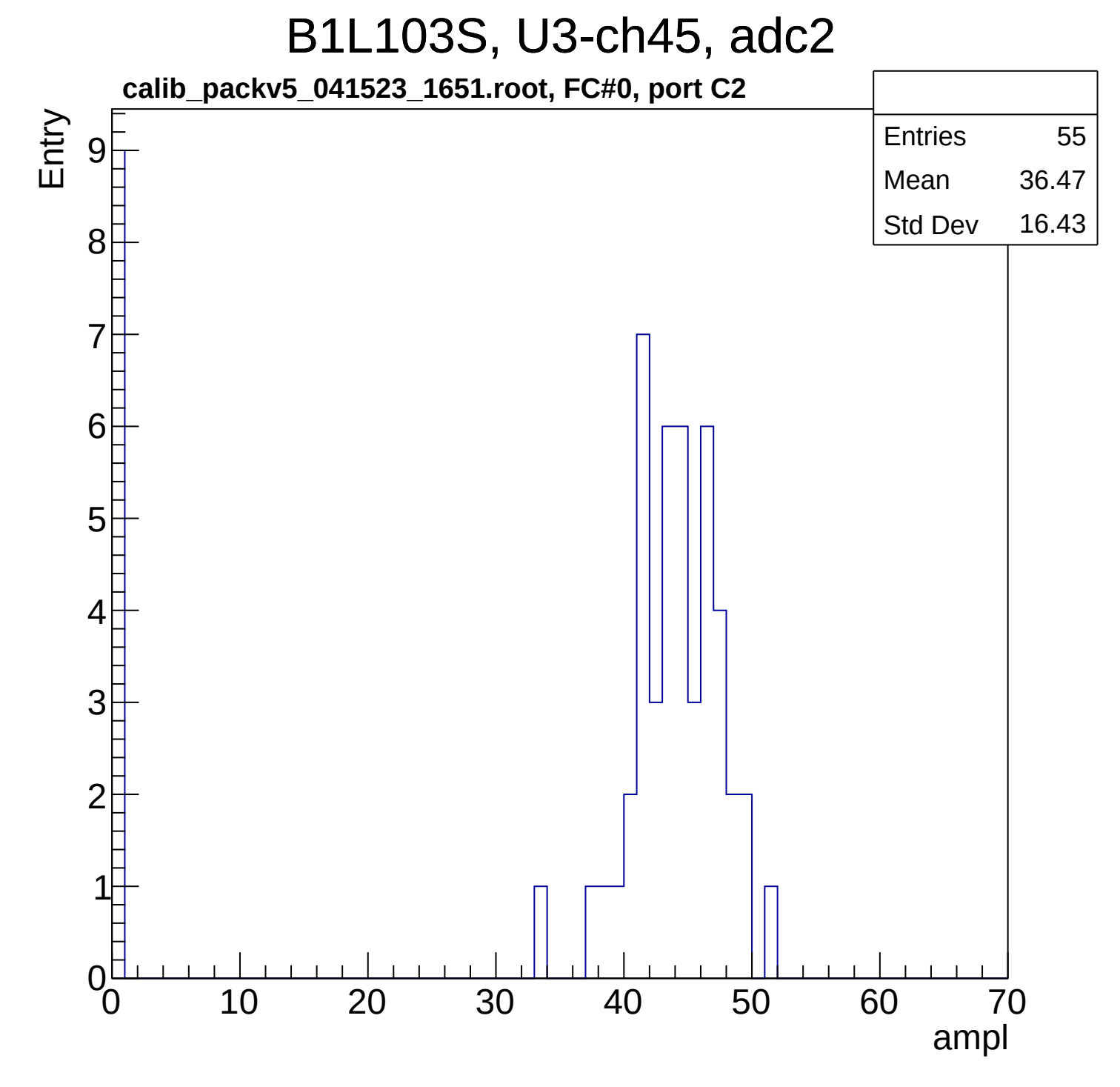
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70


B1L103S, U3-ch45, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 35.01
Std Dev 10.09
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch45, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 36.47
Std Dev 16.43
Entry
ampl
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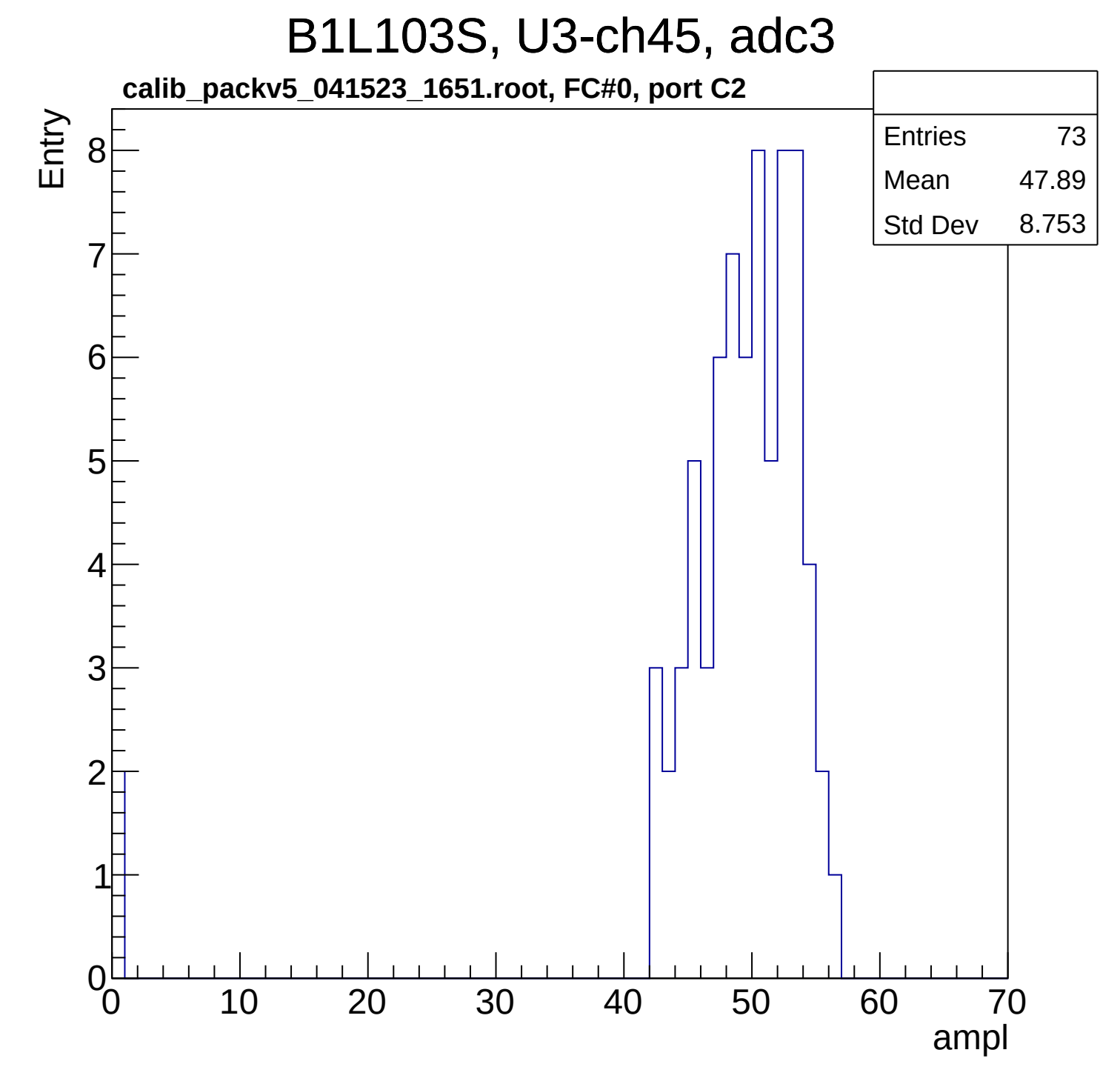
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch45, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 47.89
Std Dev 8.753
Entry
ampl
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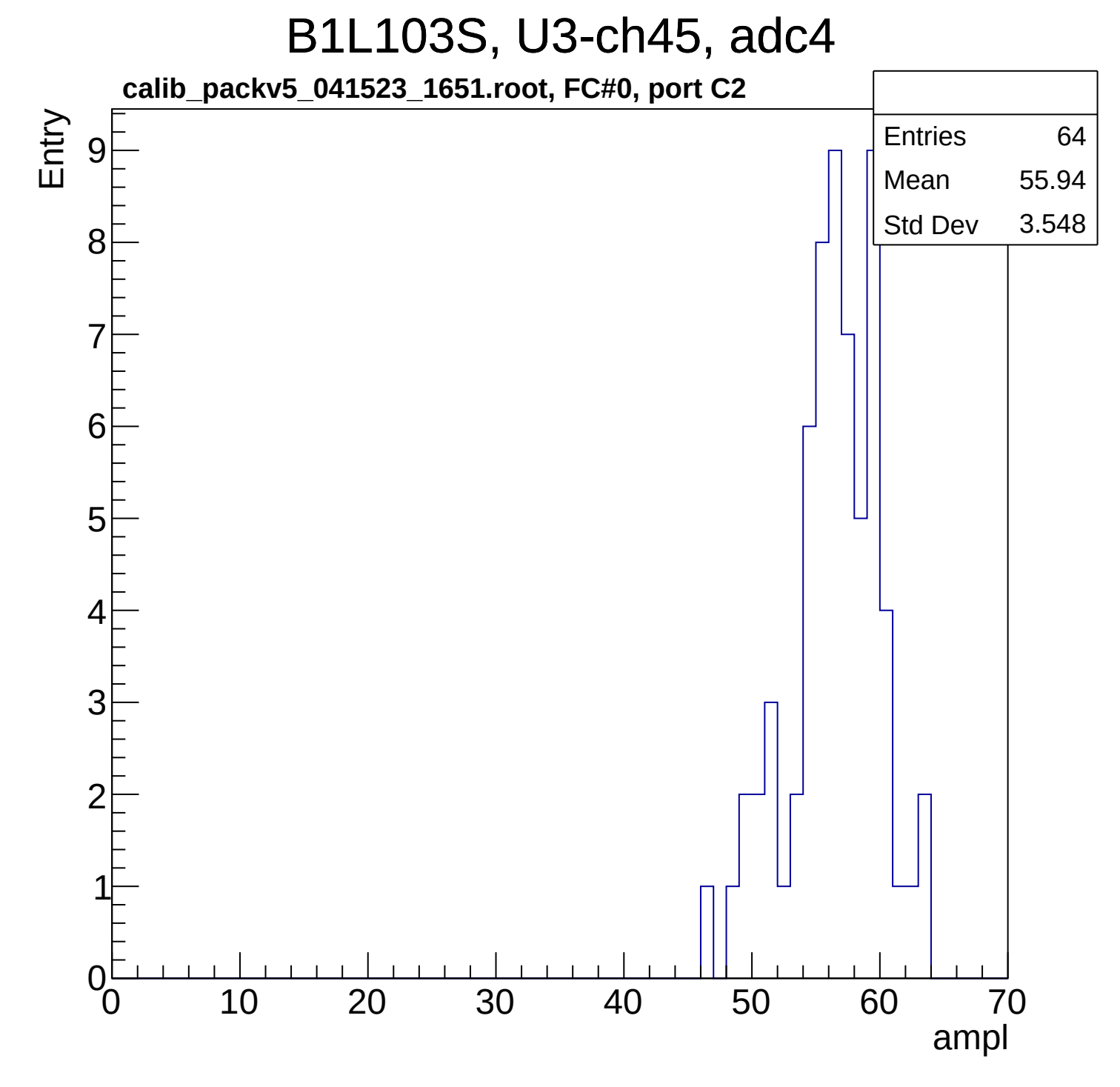
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch45, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 55.94
Std Dev 3.548
Entry
ampl
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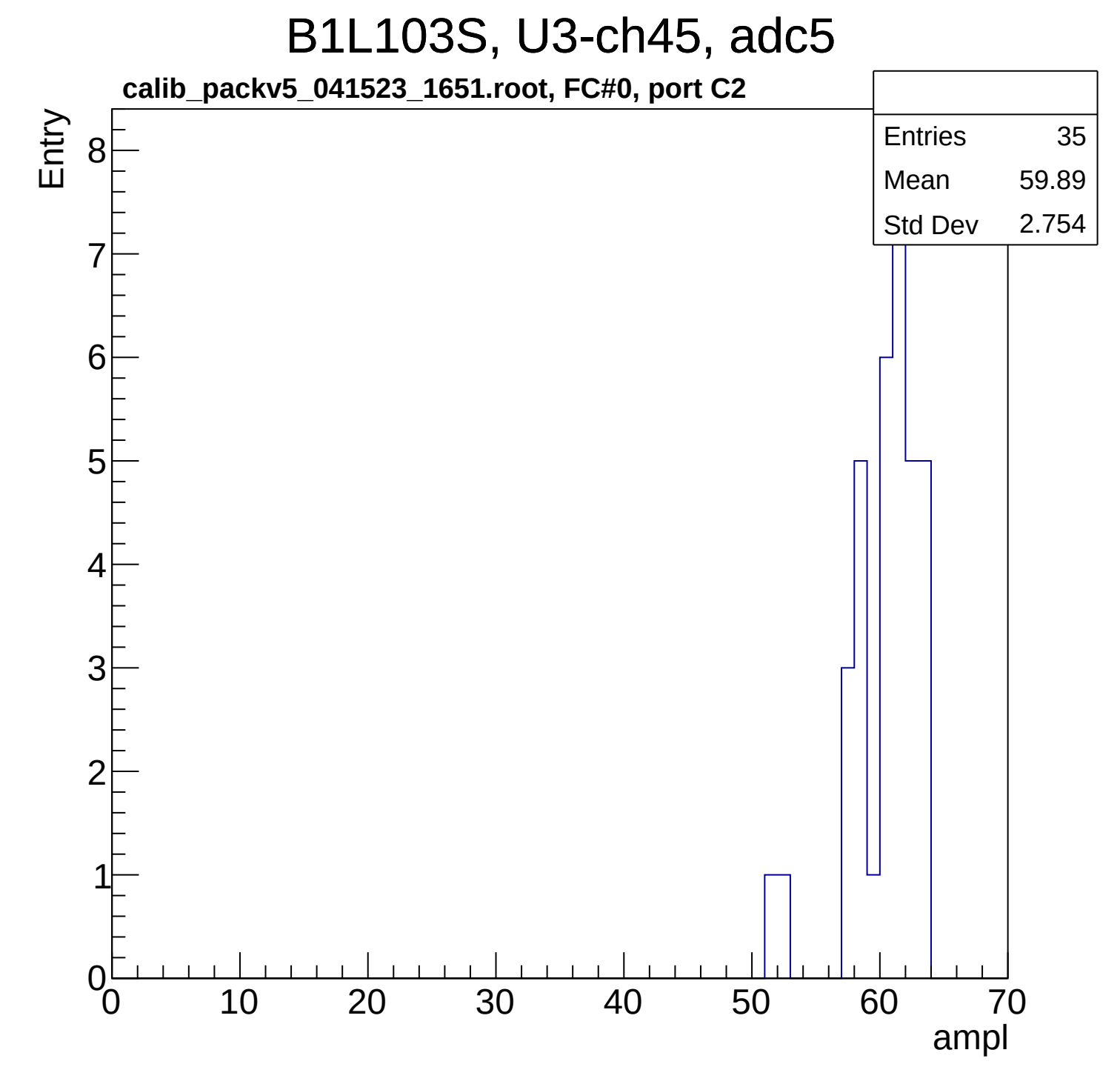
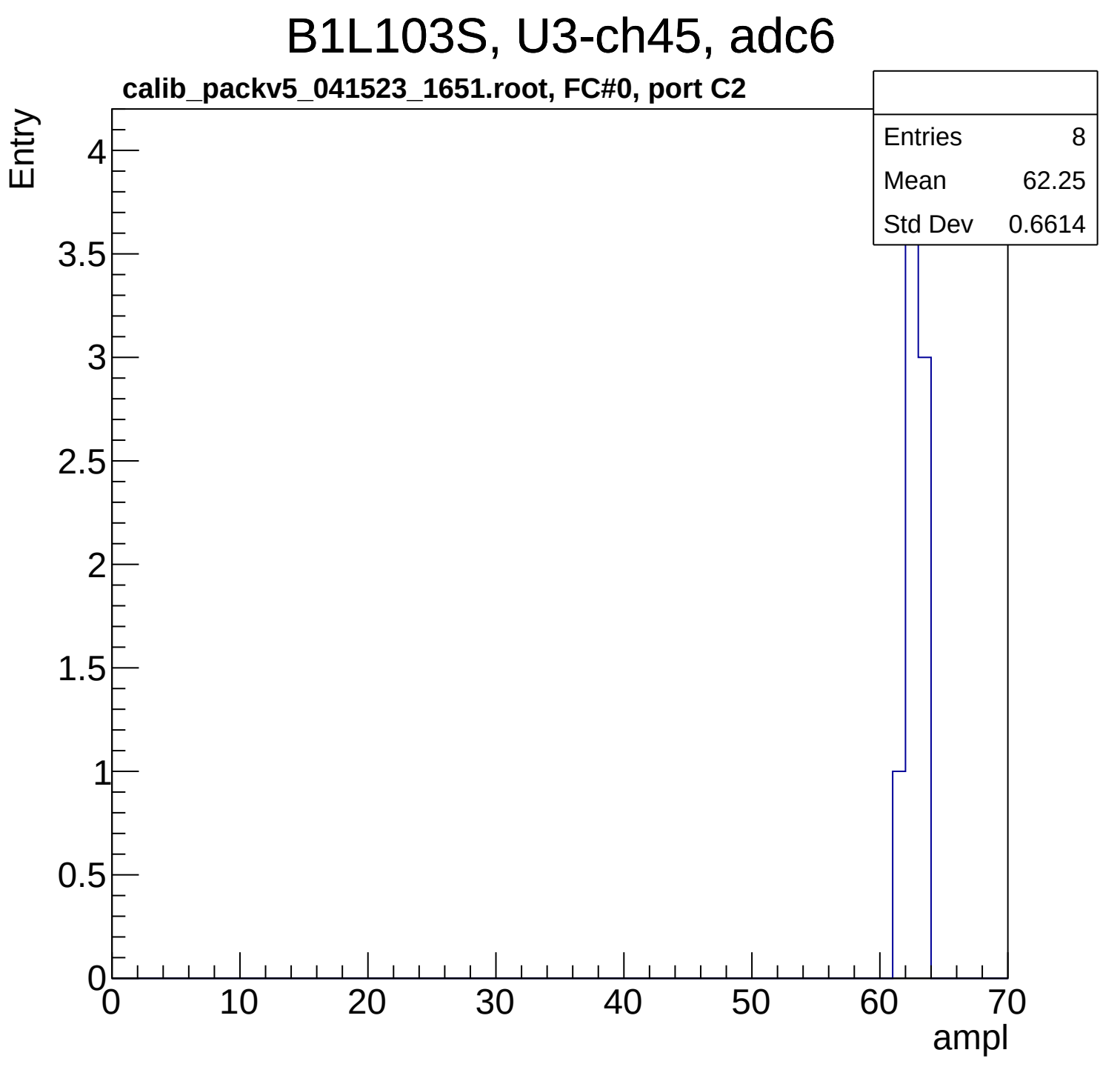
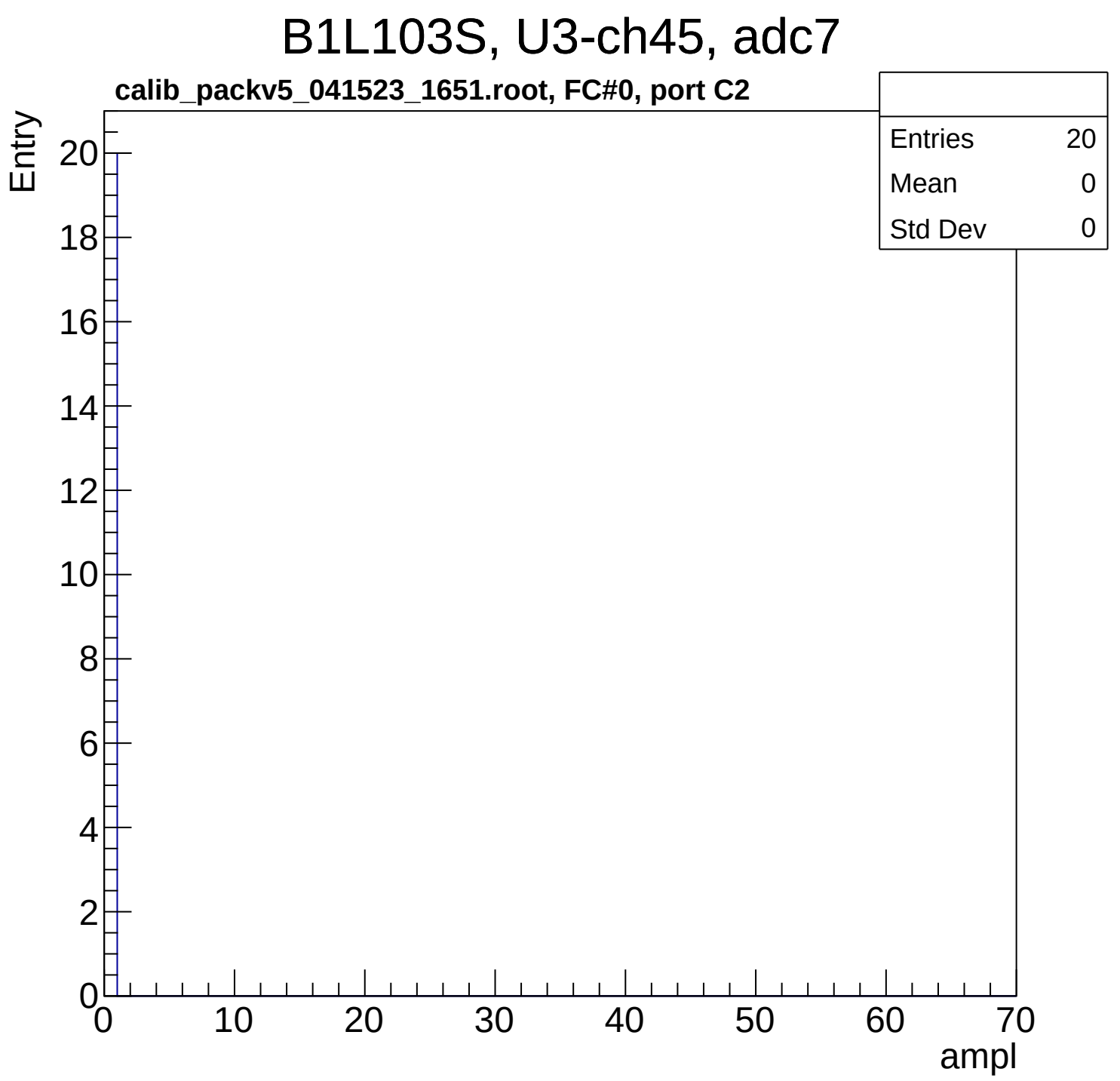
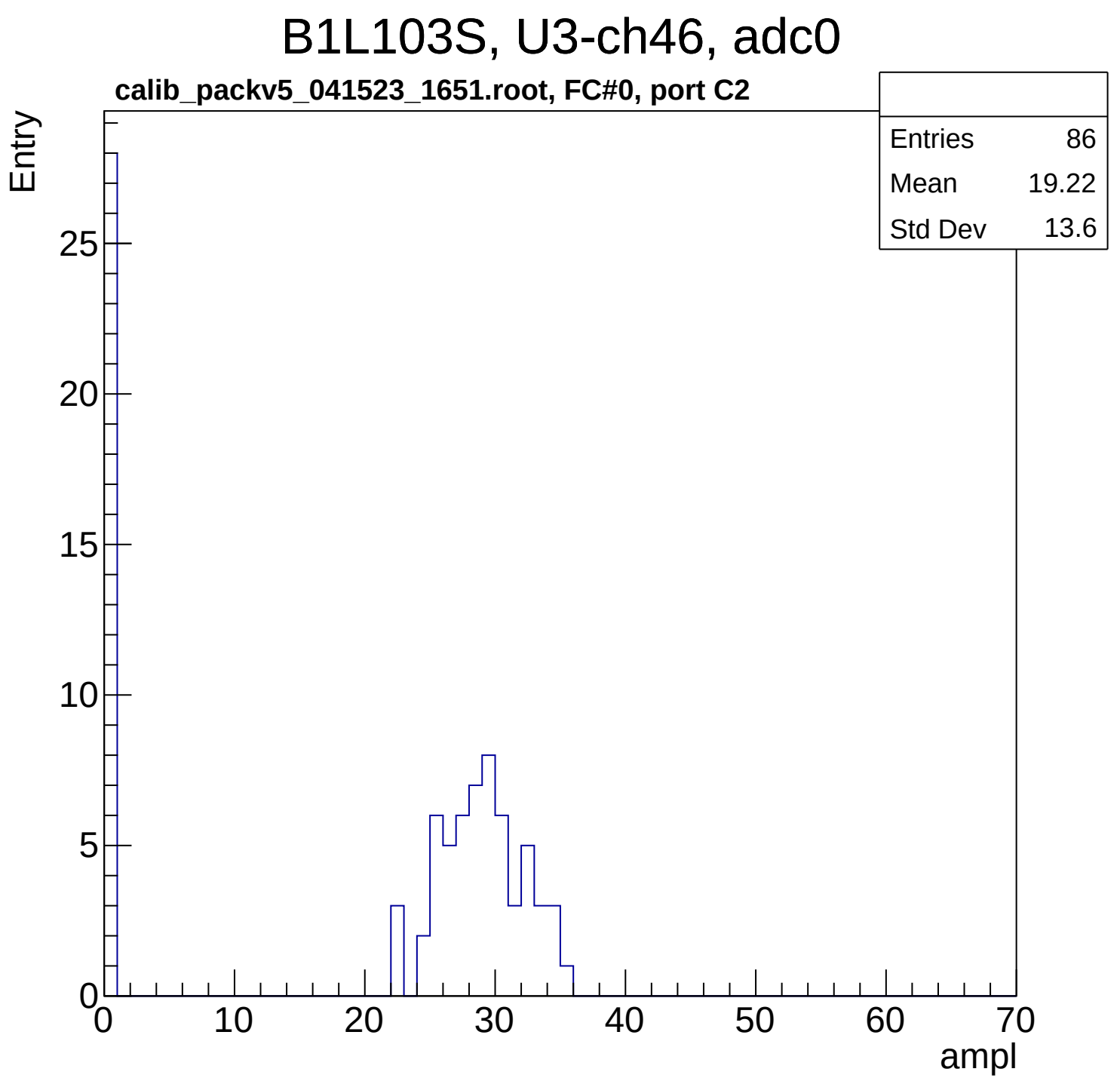
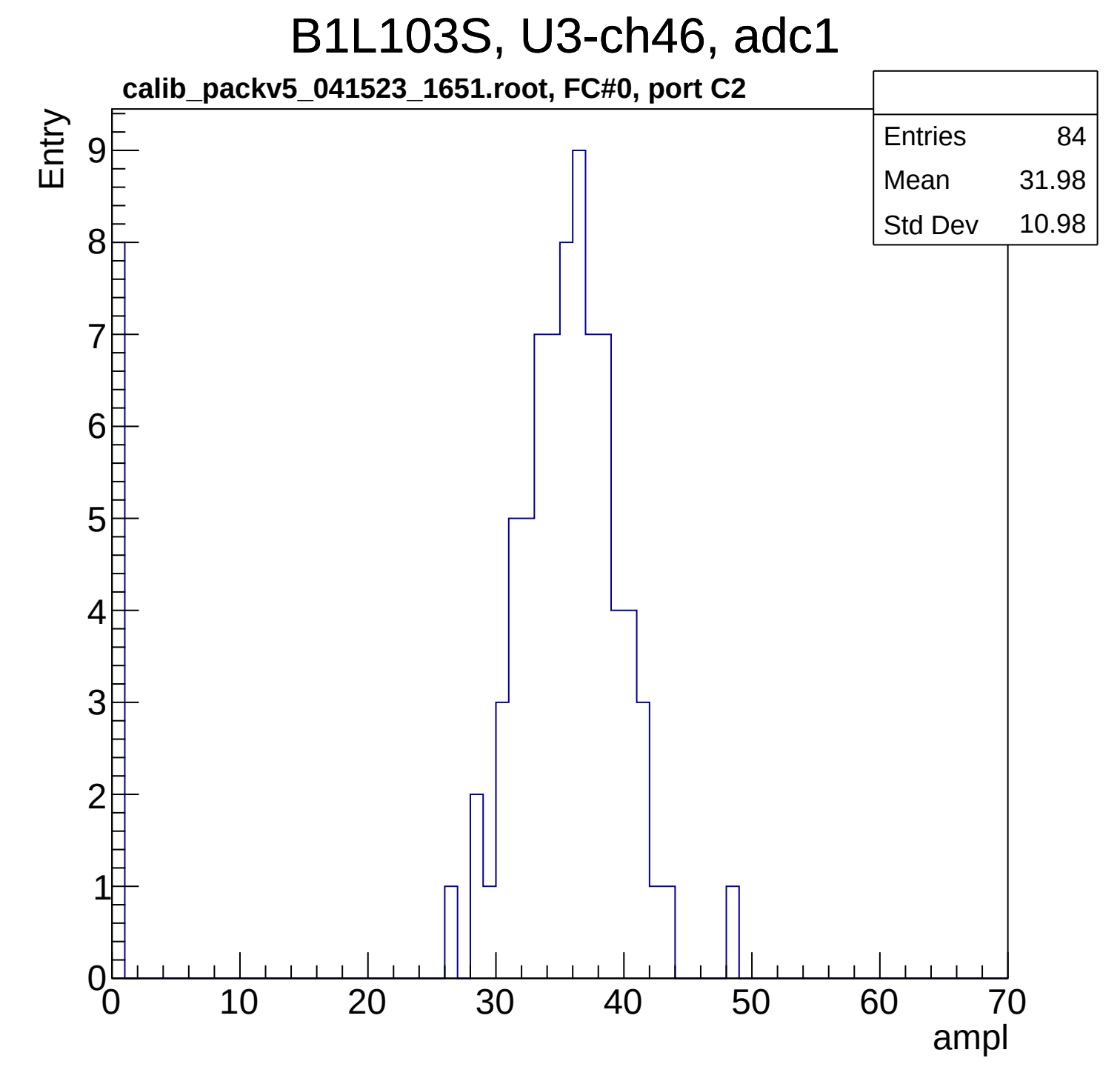
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

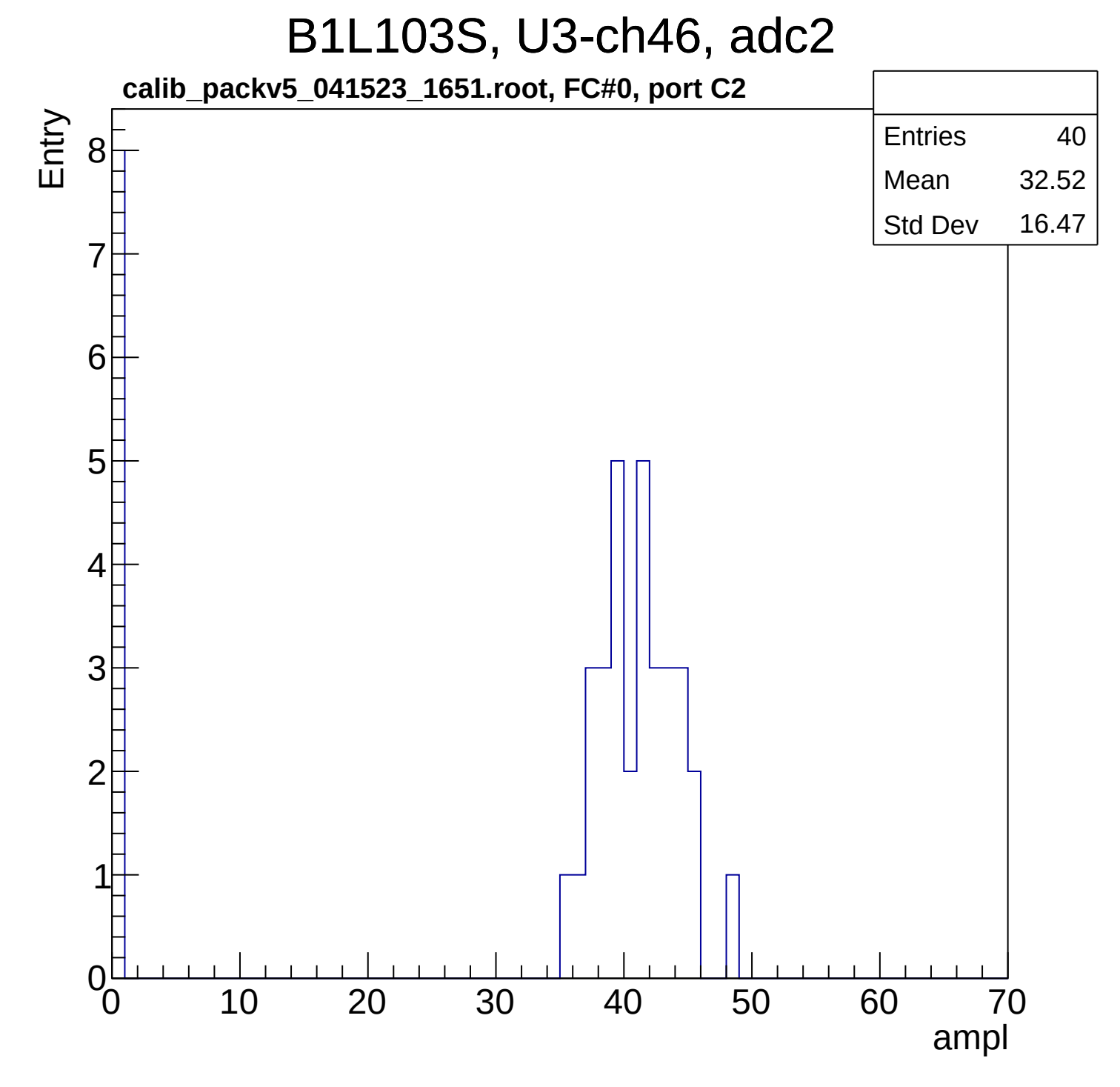

B1L103S, U3-ch45, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 59.89
Std Dev 2.754
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch45, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 62.25
Std Dev 0.6614
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U3-ch45, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch46, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 19.22
Std Dev 13.6
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch46, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 31.98
Std Dev 10.98
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch46, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 32.52
Std Dev 16.47
Entry
ampl
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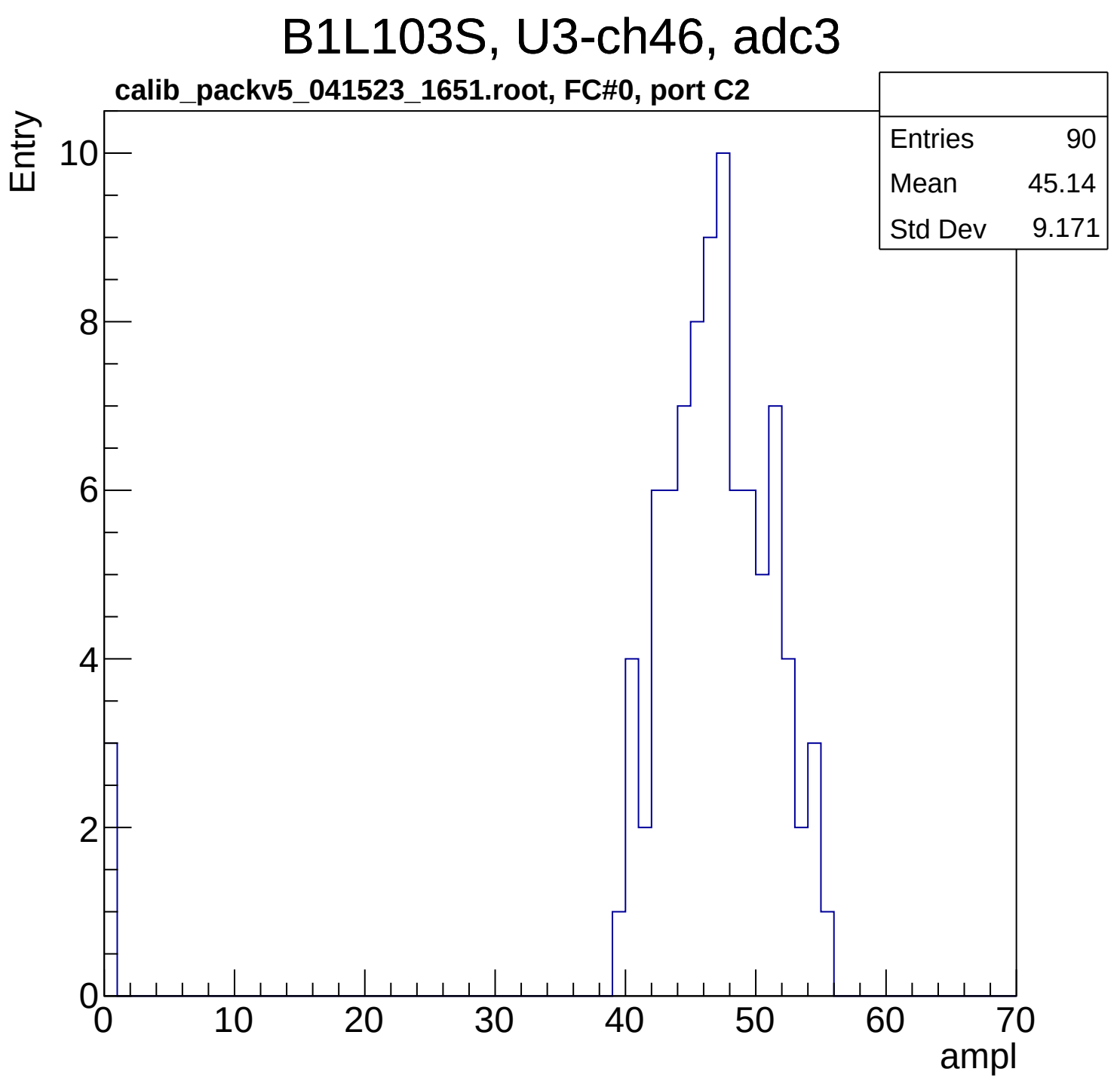
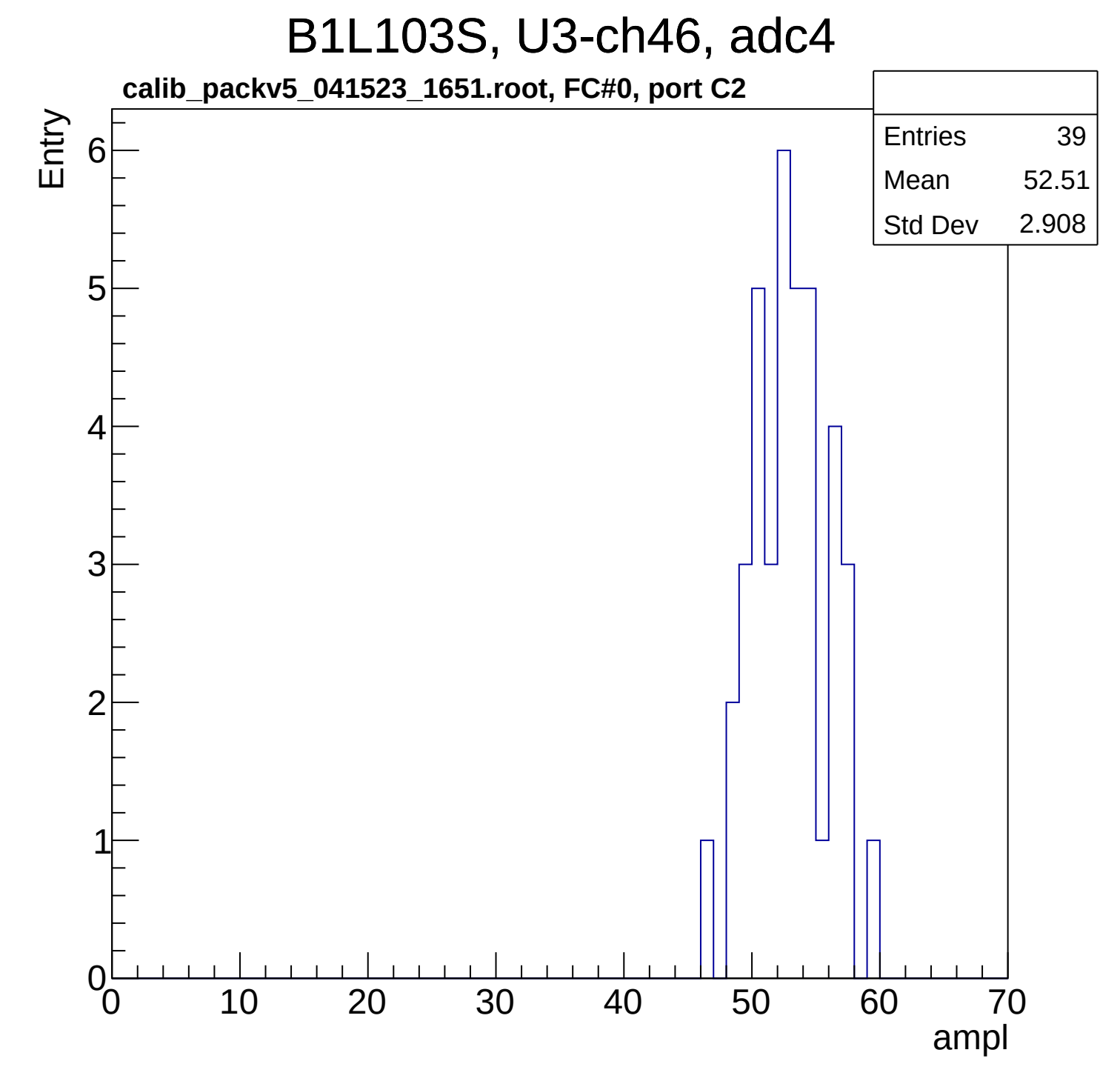
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch46, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 45.14
Std Dev 9.171
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U3-ch46, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 52.51
Std Dev 2.908
Entry
ampl
0
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3
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0
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40
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60
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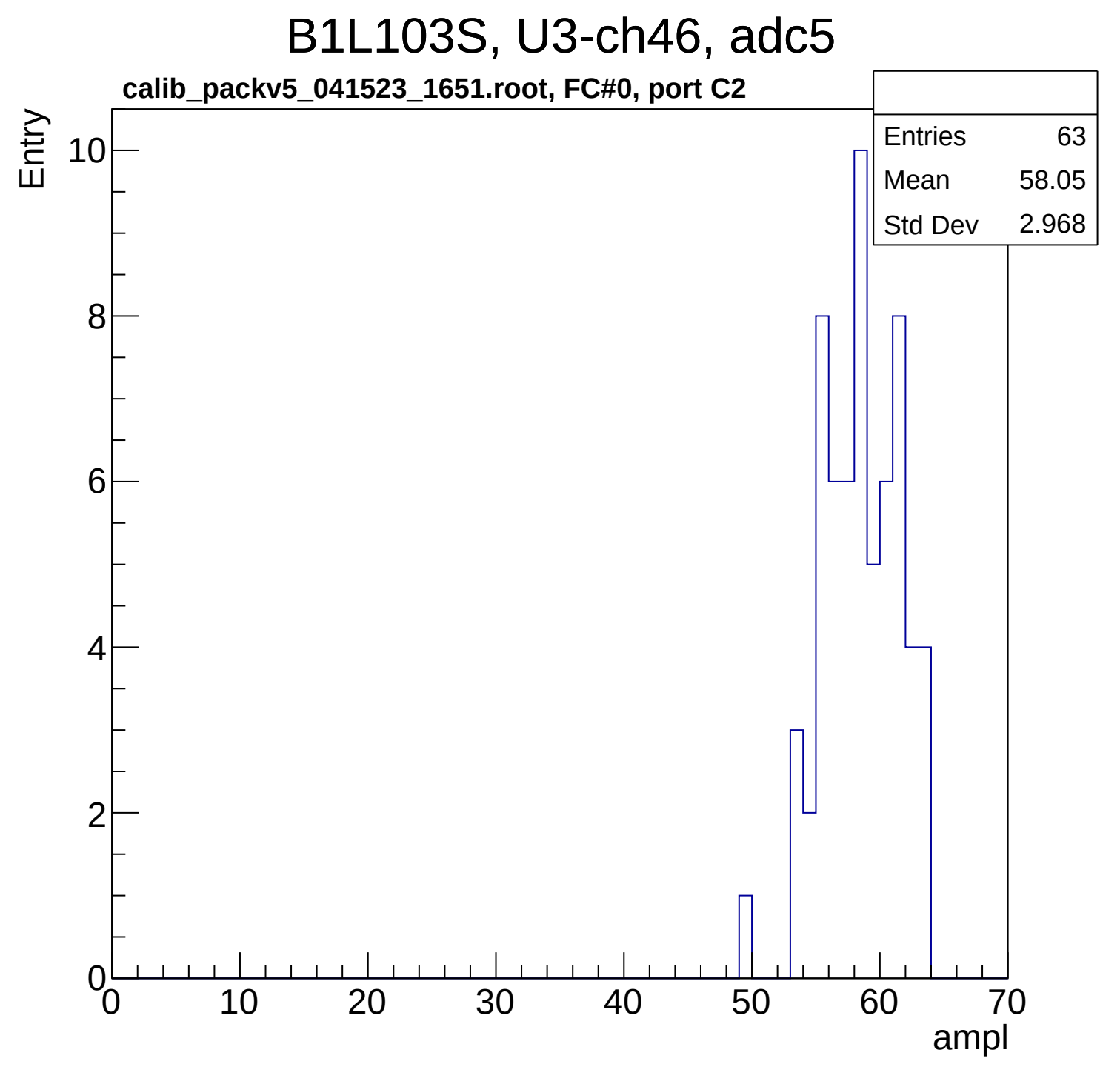
B1L103S, U3-ch46, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 58.05
Std Dev 2.968
Entry
ampl
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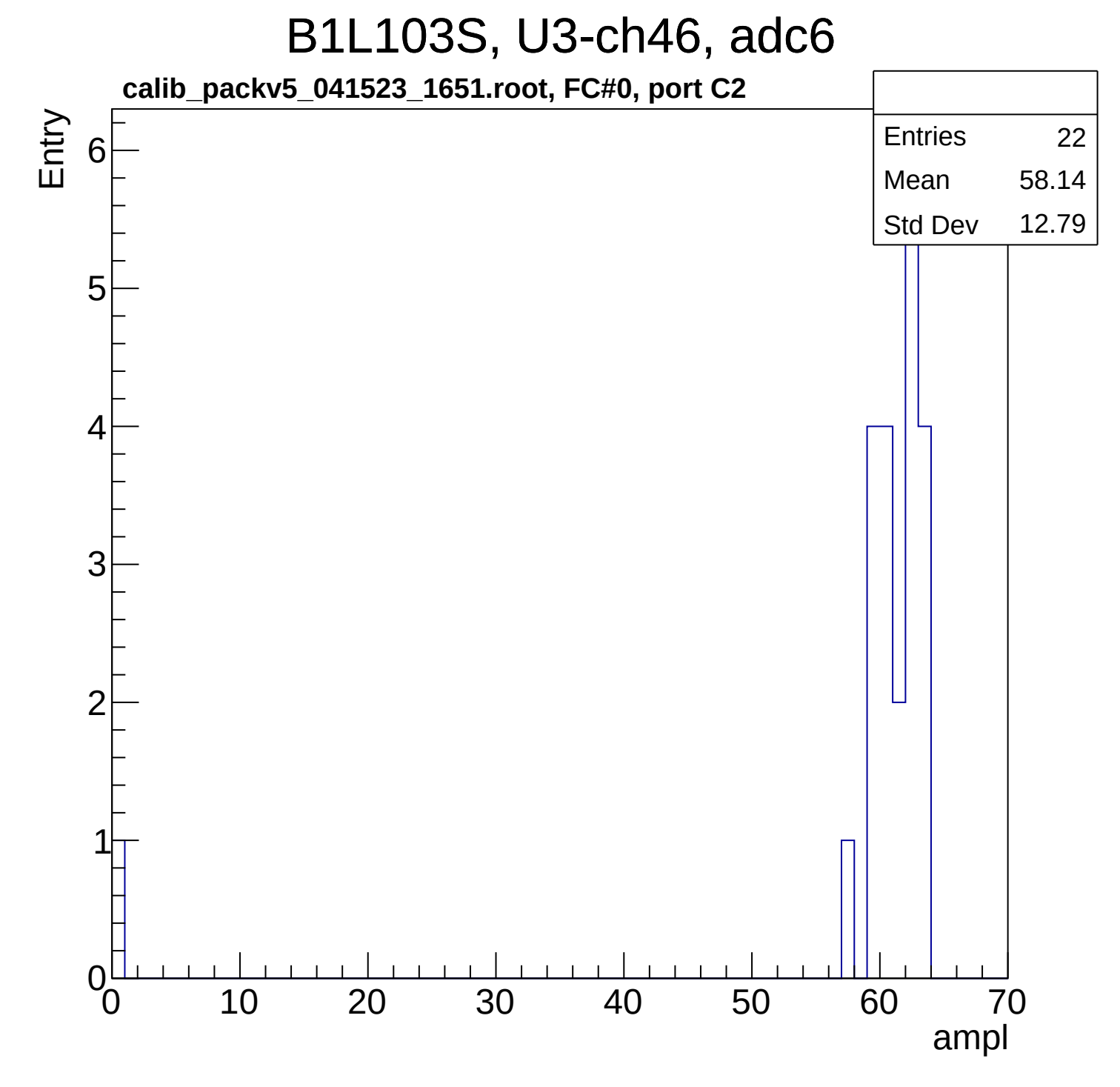
B1L103S, U3-ch46, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 58.14
Std Dev 12.79
Entry
ampl
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2
3
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0
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20
30
40
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60
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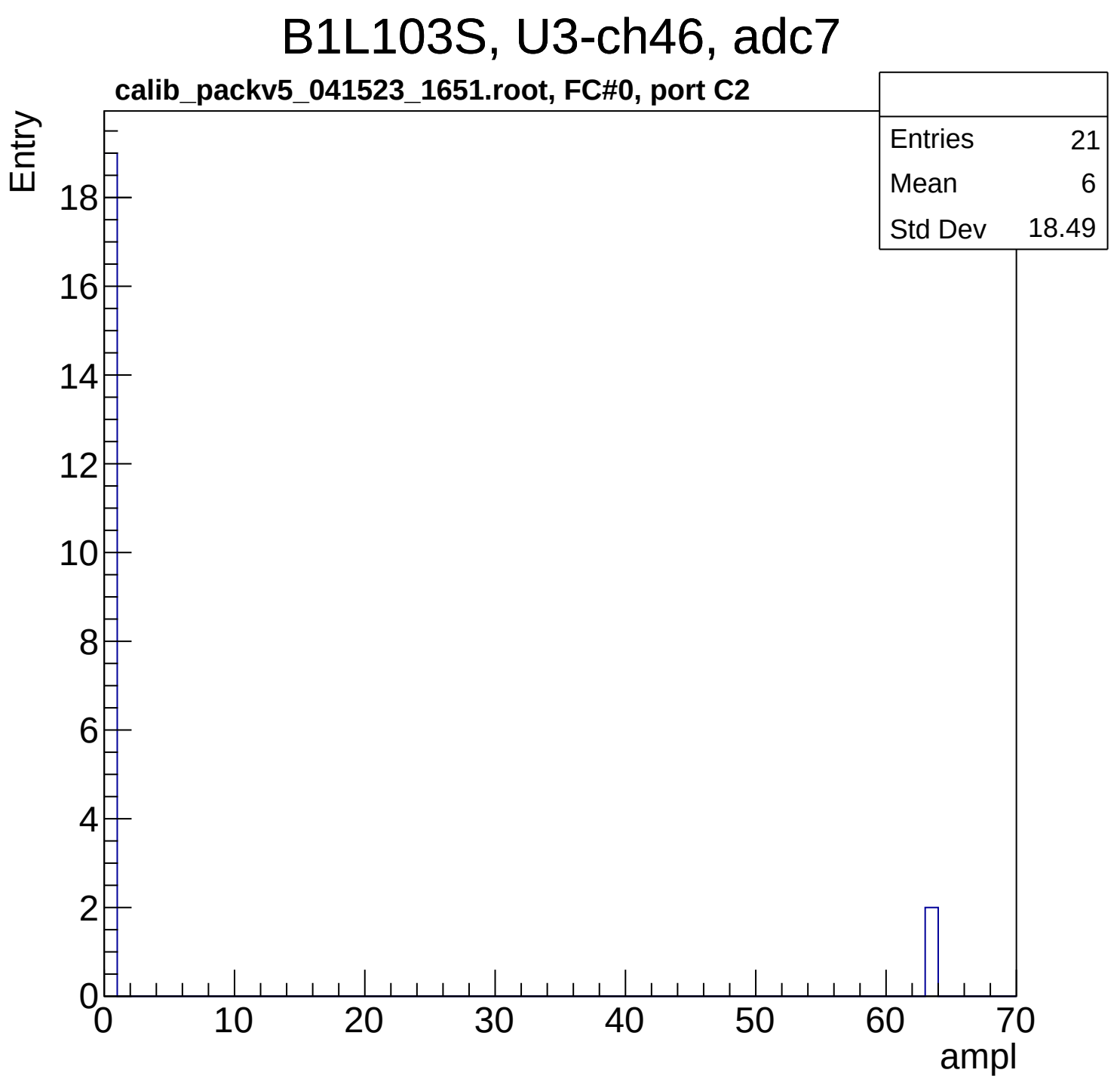
B1L103S, U3-ch46, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 6
Std Dev 18.49
Entry
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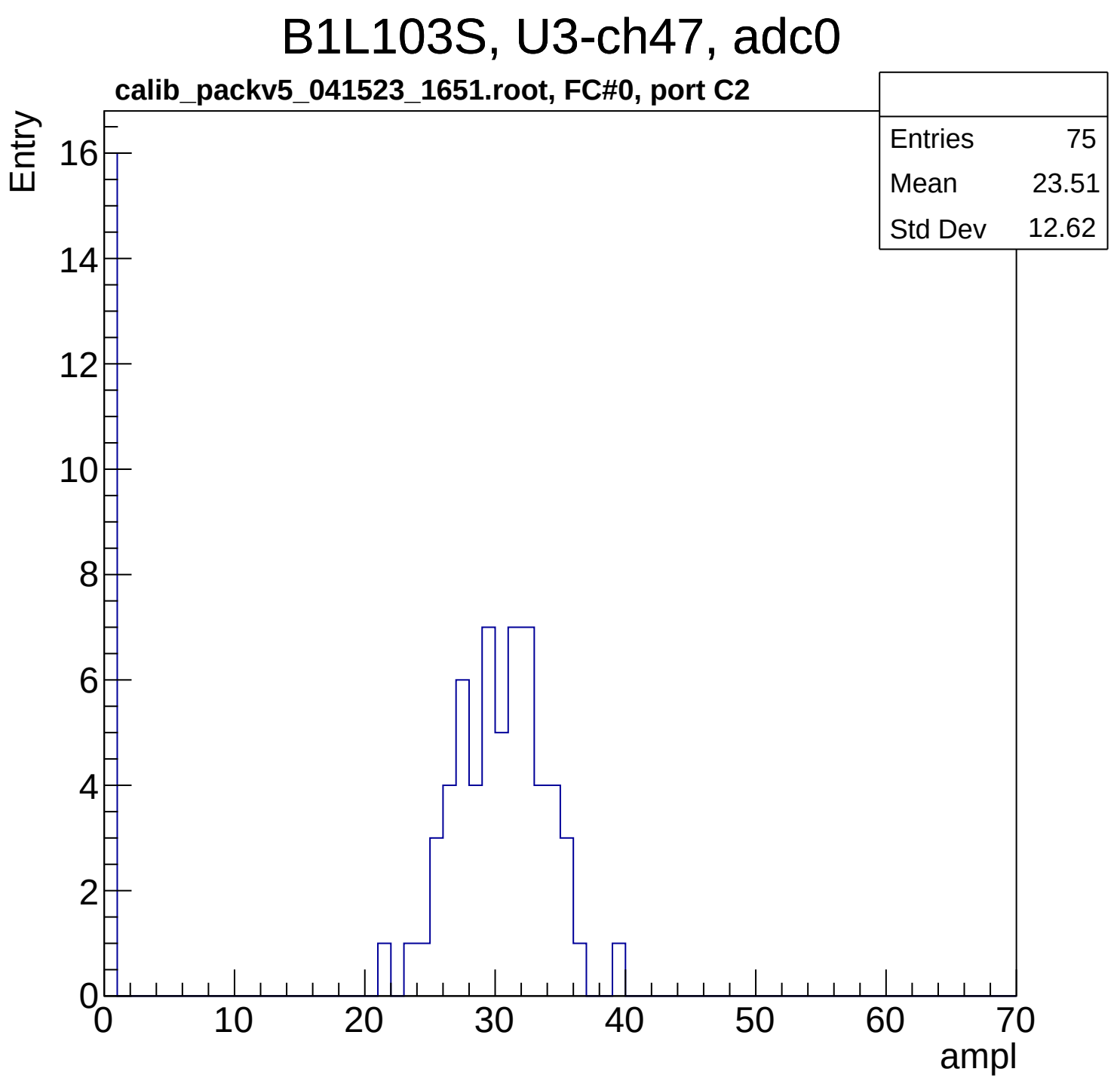
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch47, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 23.51
Std Dev 12.62
Entry
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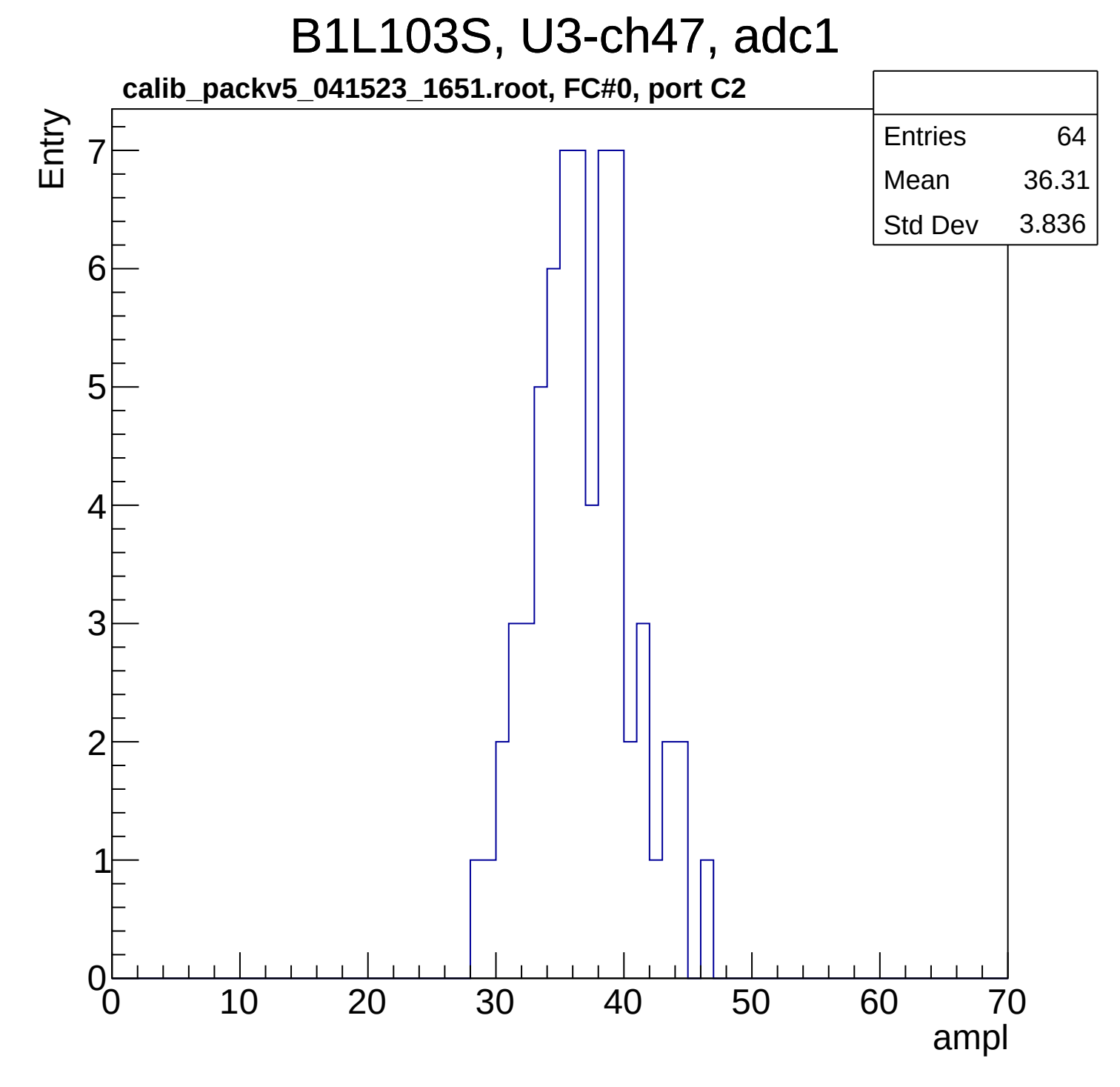
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch47, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 36.31
Std Dev 3.836
Entry
ampl
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2
3
4
5
6
7
0
10
20
30
40
50
60
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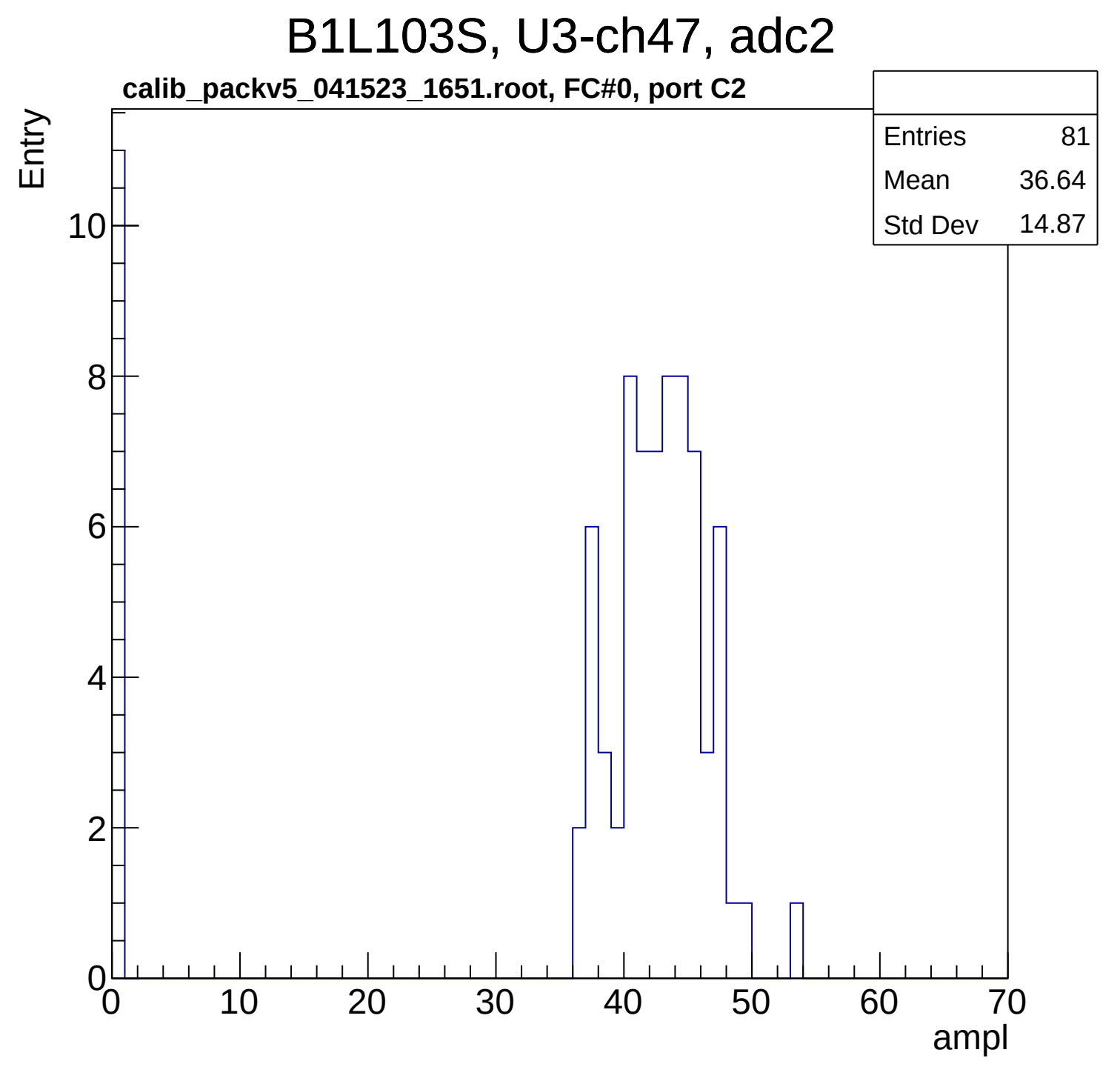
B1L103S, U3-ch47, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 36.64
Std Dev 14.87
Entry
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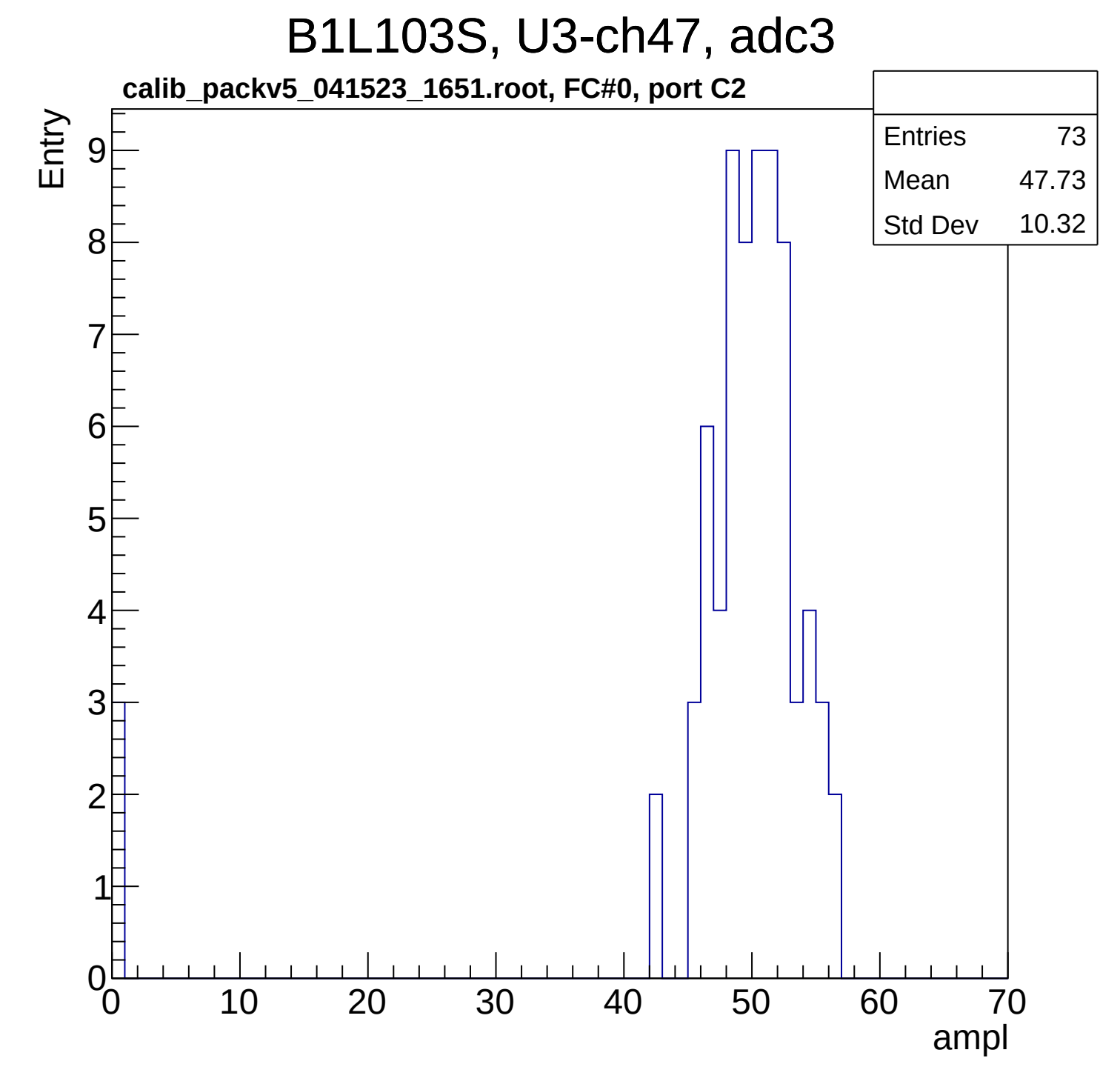
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch47, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 47.73
Std Dev 10.32
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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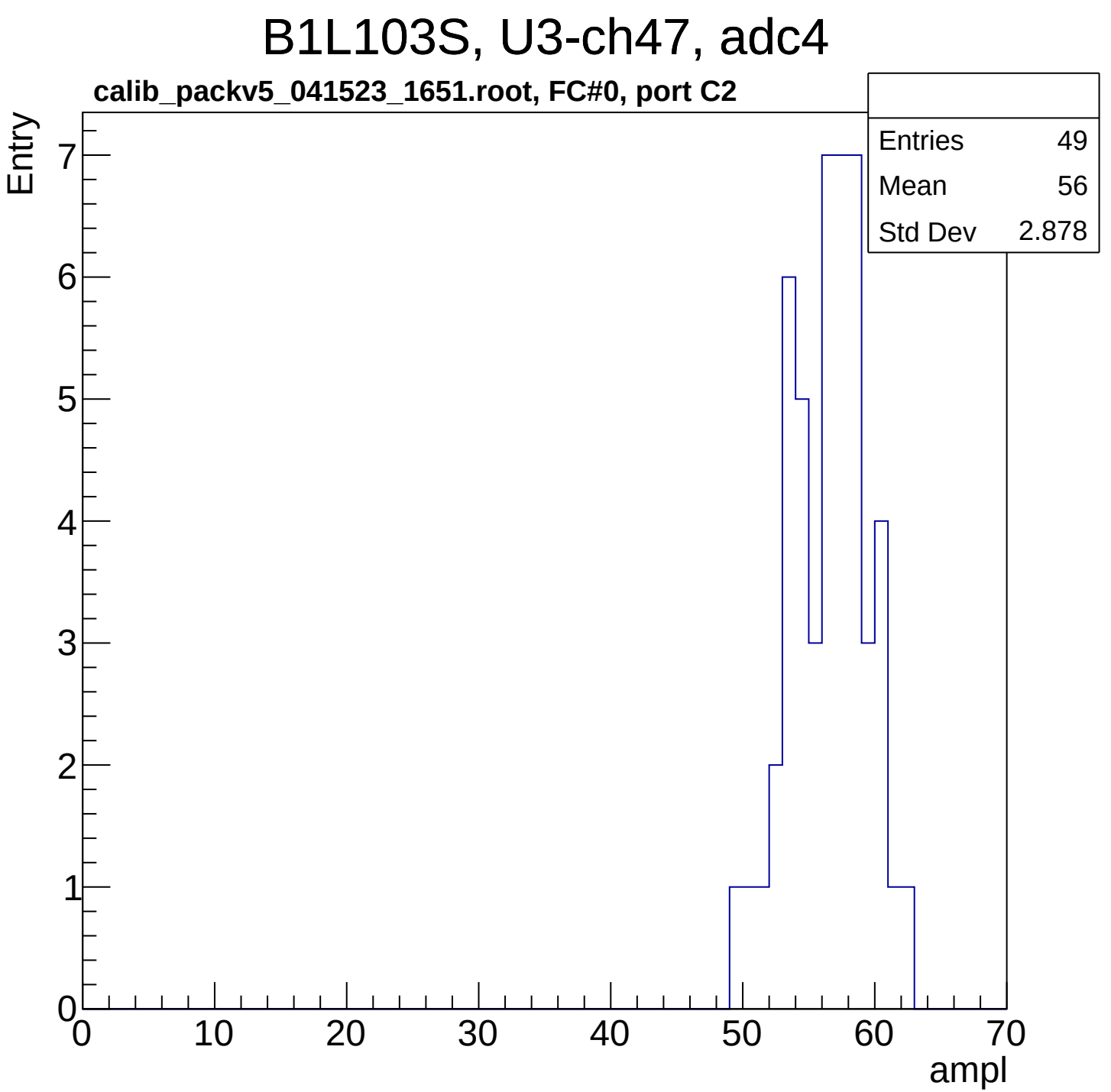
B1L103S, U3-ch47, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 56
Std Dev 2.878
Entry
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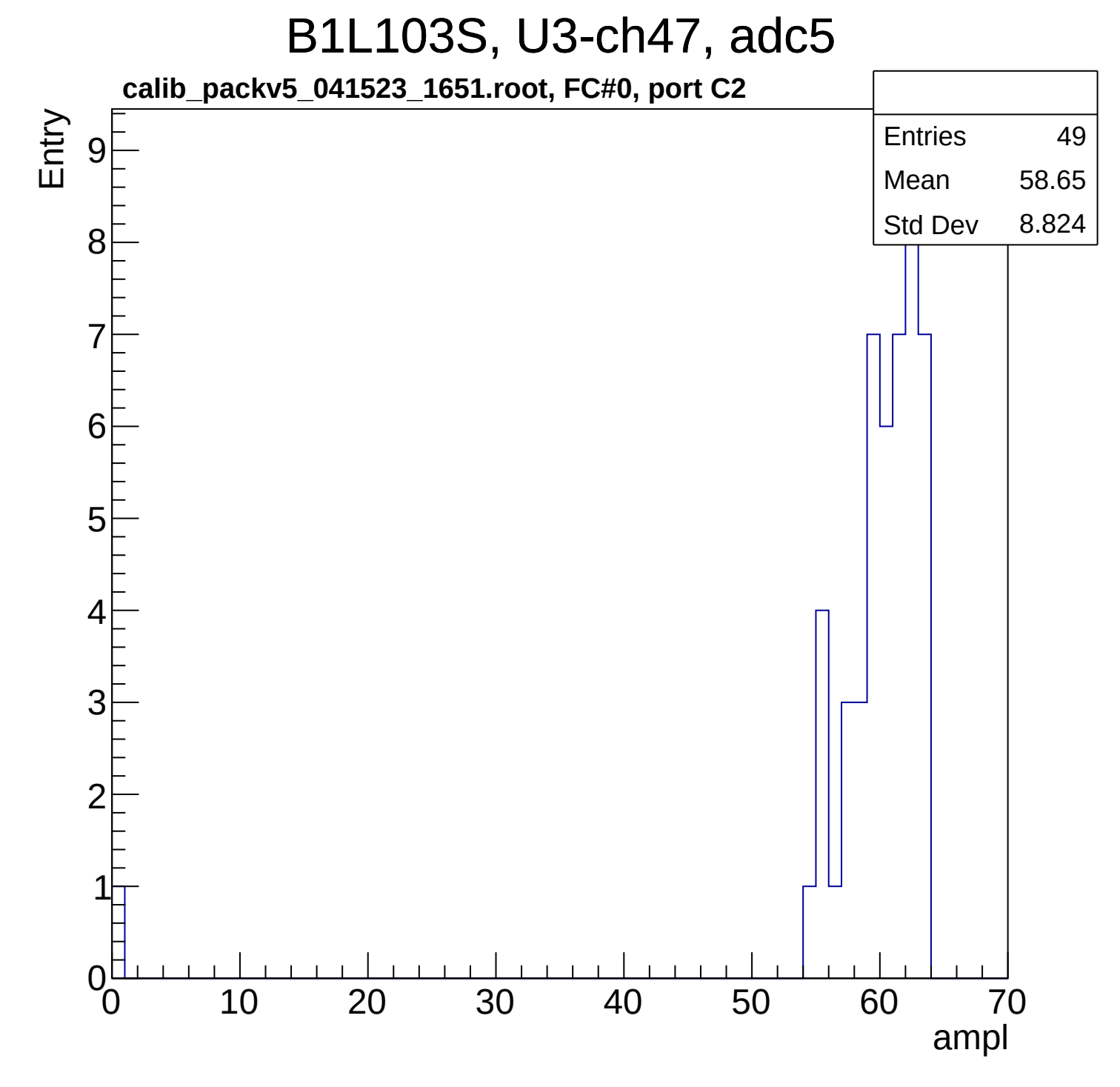
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch47, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 58.65
Std Dev 8.824
Entry
ampl
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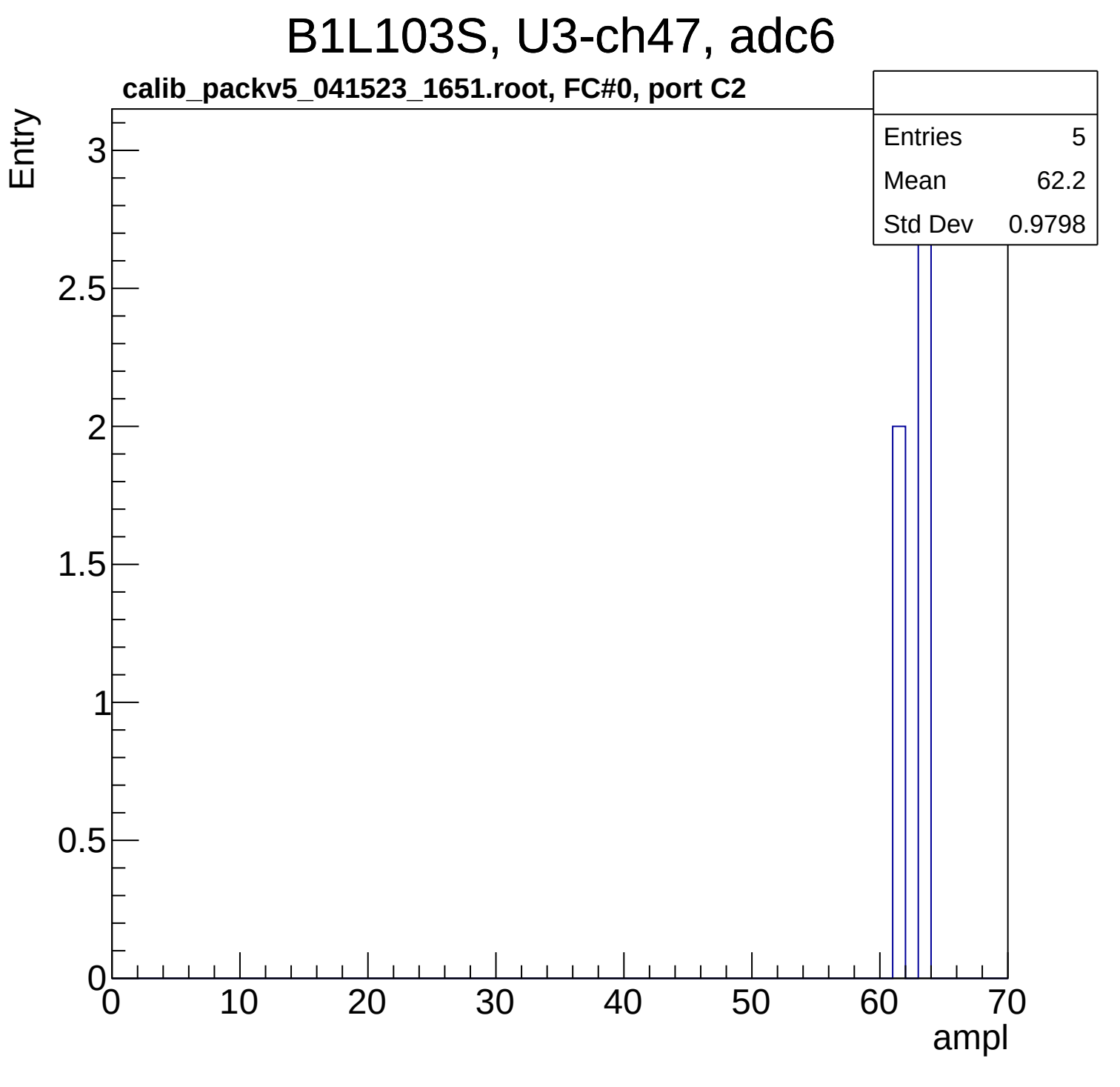
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch47, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 62.2
Std Dev 0.9798
Entry
ampl
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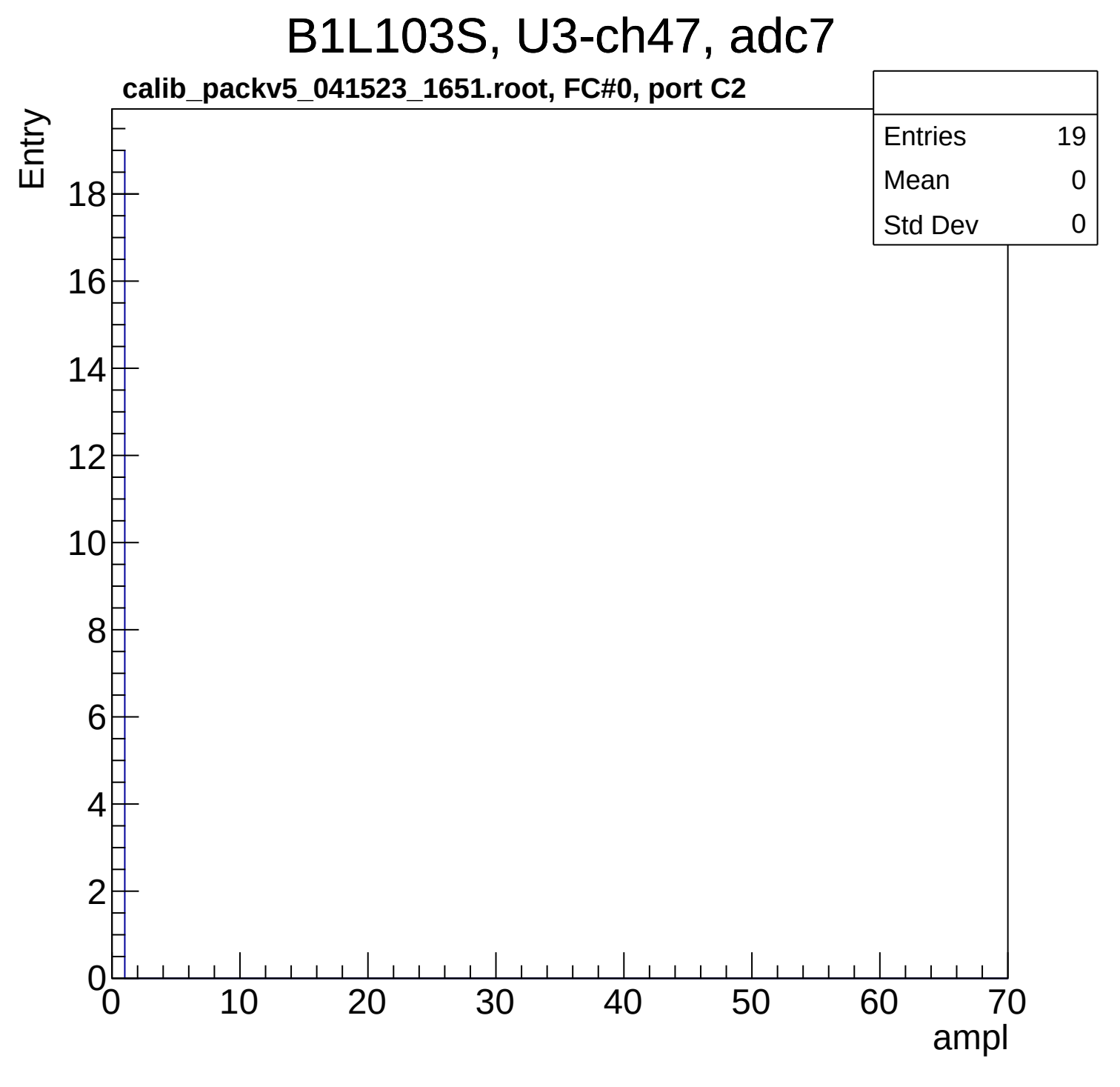
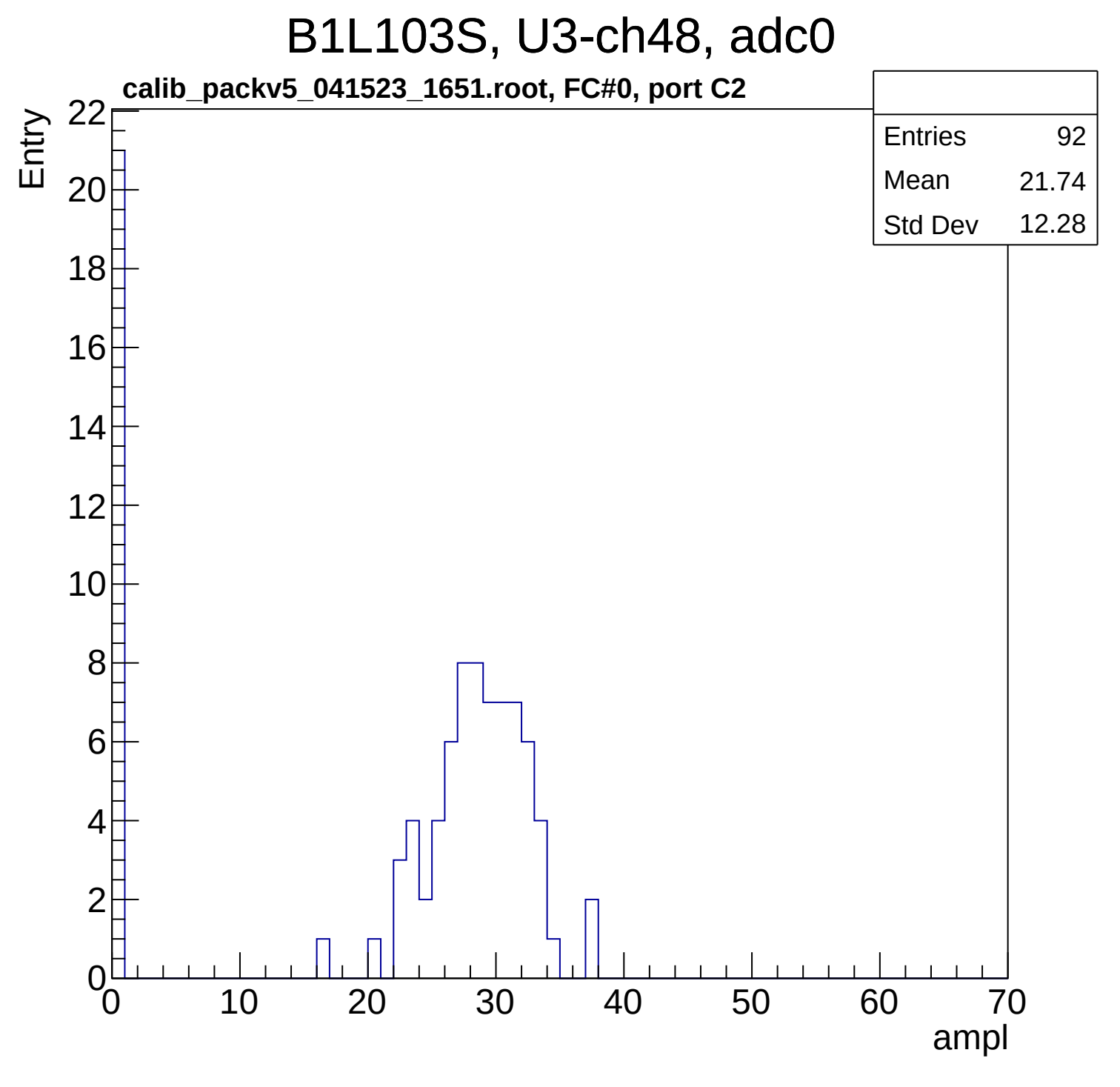
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U3-ch47, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch48, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 21.74
Std Dev 12.28
Entry
ampl
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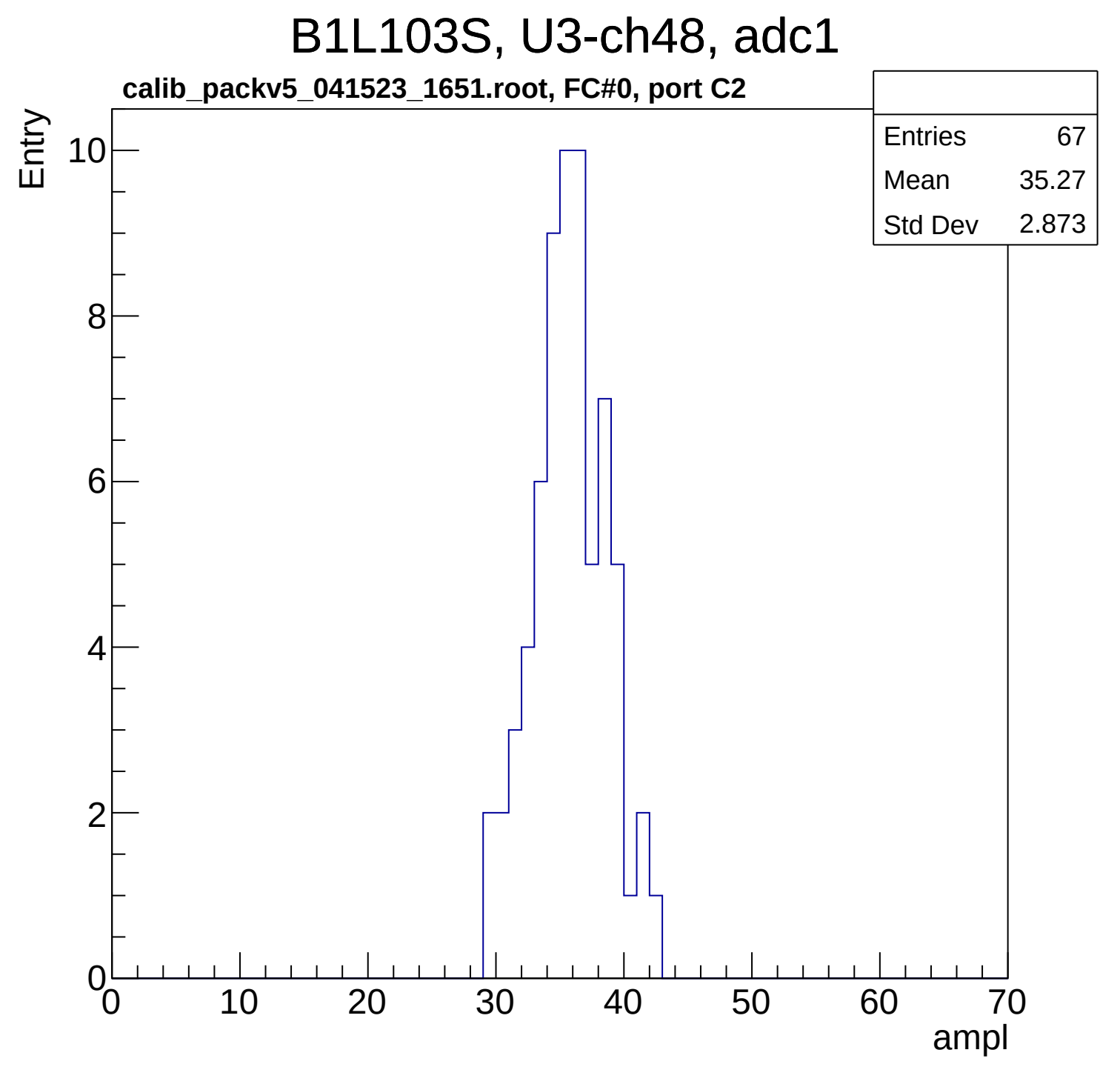
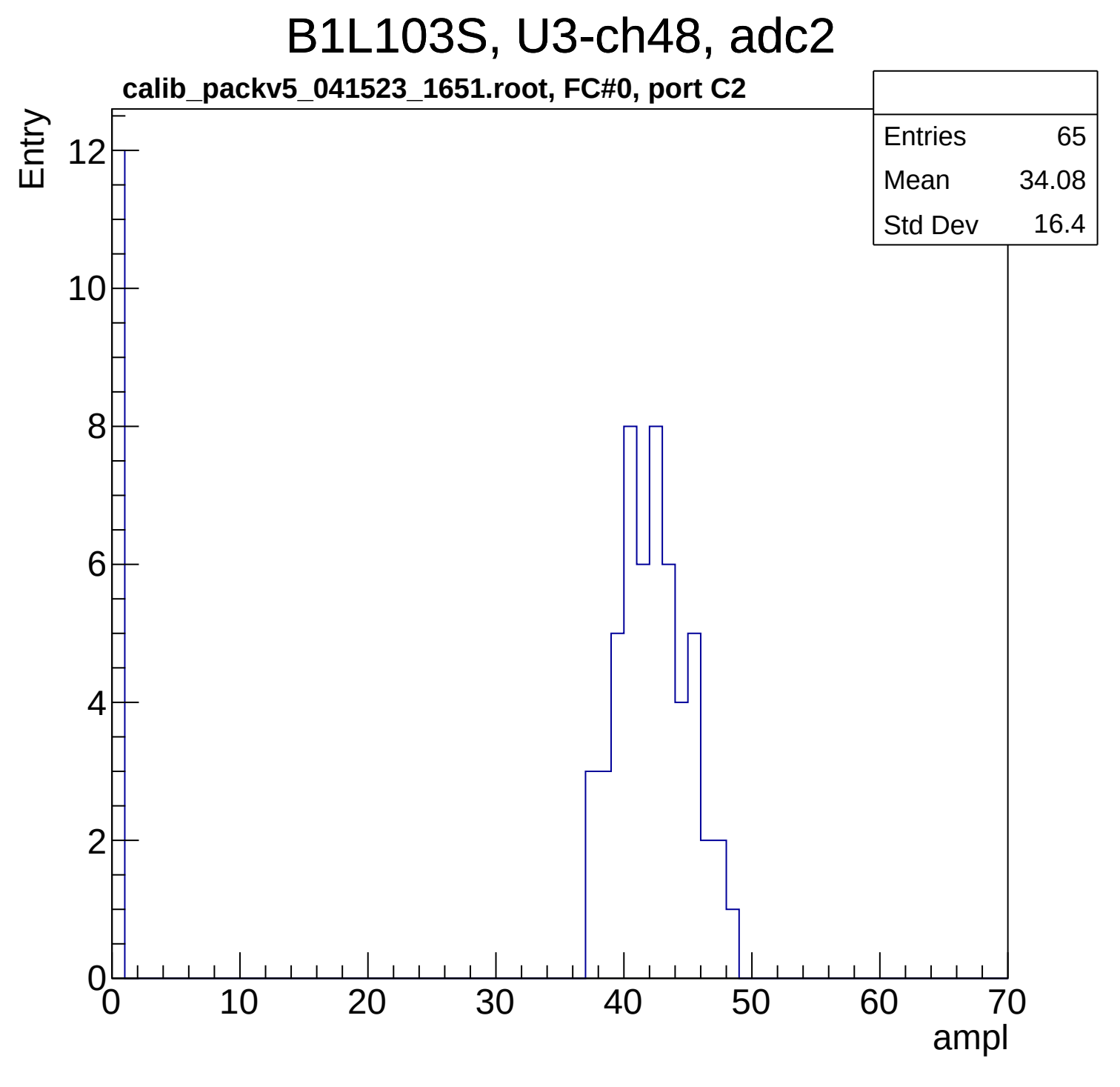
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70


B1L103S, U3-ch48, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 35.27
Std Dev 2.873
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U3-ch48, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 34.08
Std Dev 16.4
Entry
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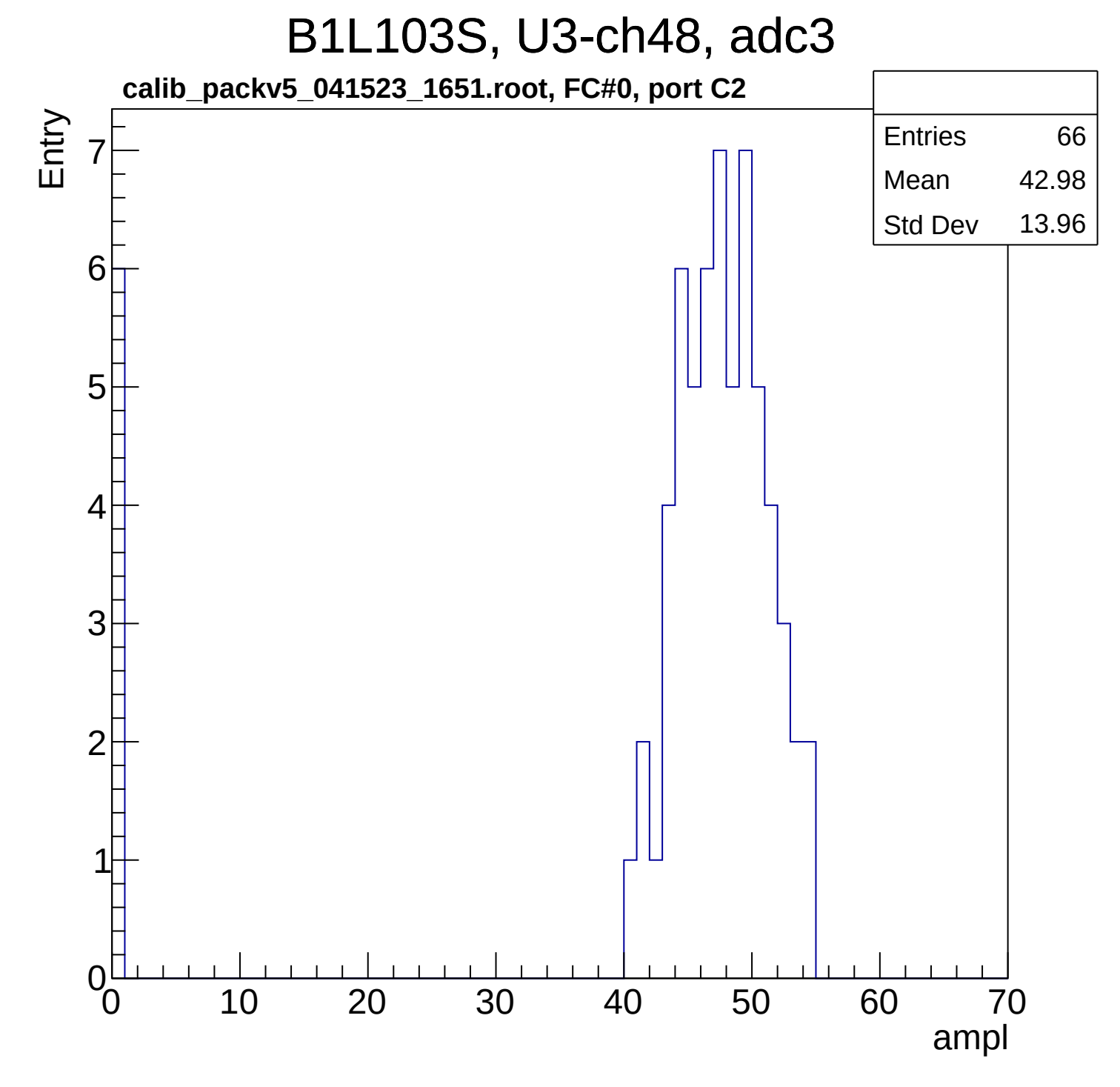
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch48, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 42.98
Std Dev 13.96
Entry
ampl
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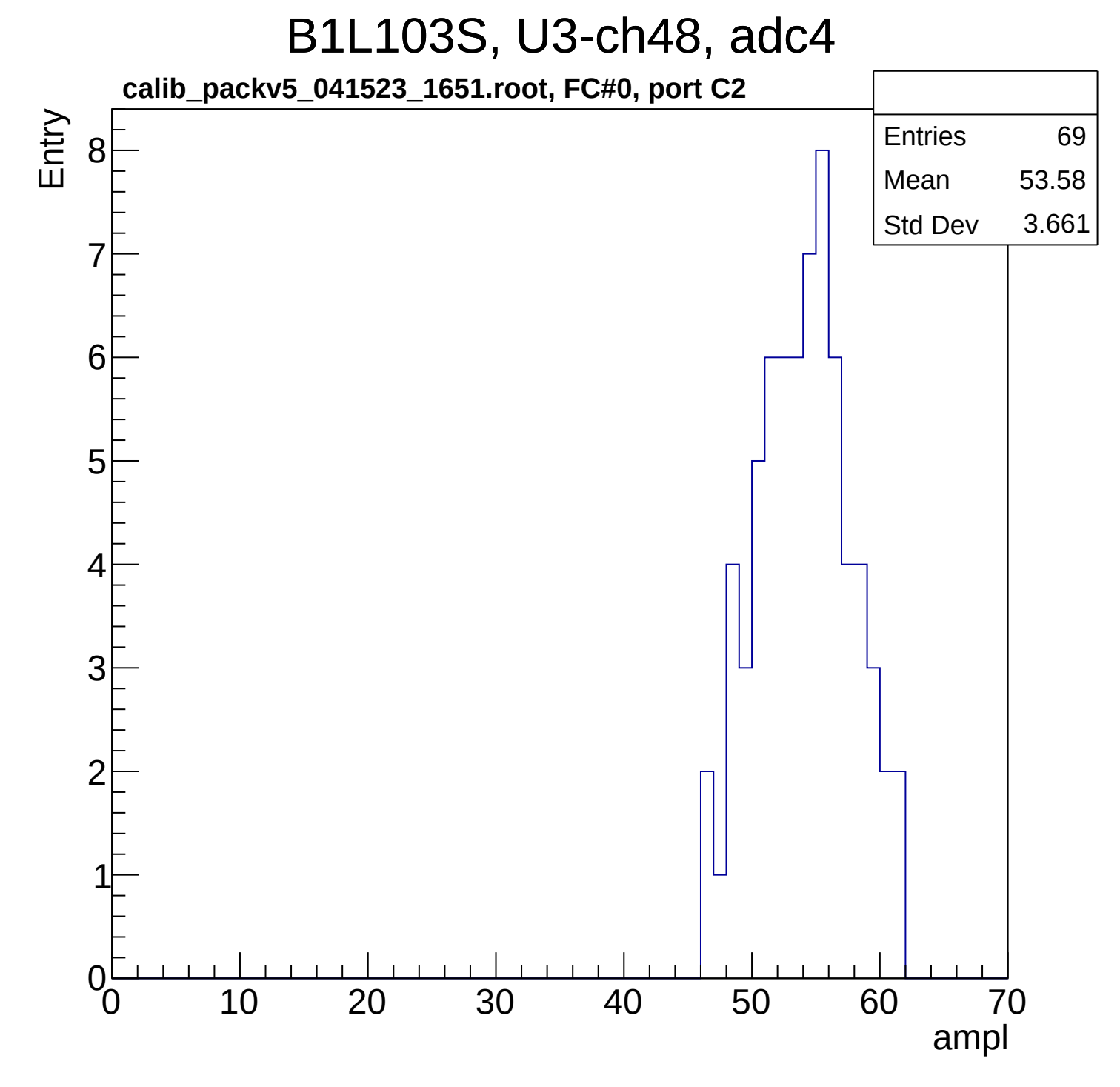
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch48, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 53.58
Std Dev 3.661
Entry
ampl
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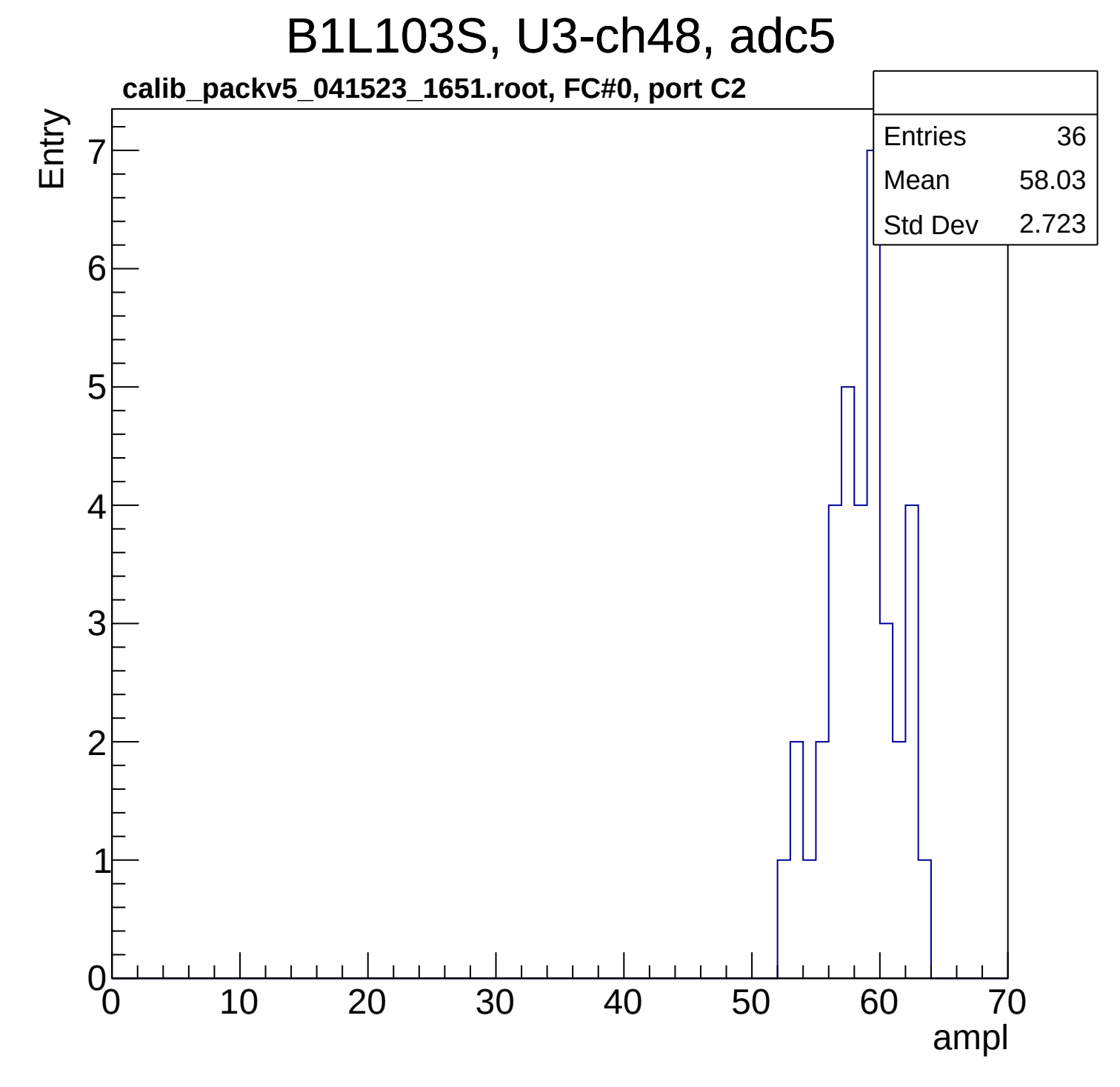
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch48, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 58.03
Std Dev 2.723
Entry
ampl
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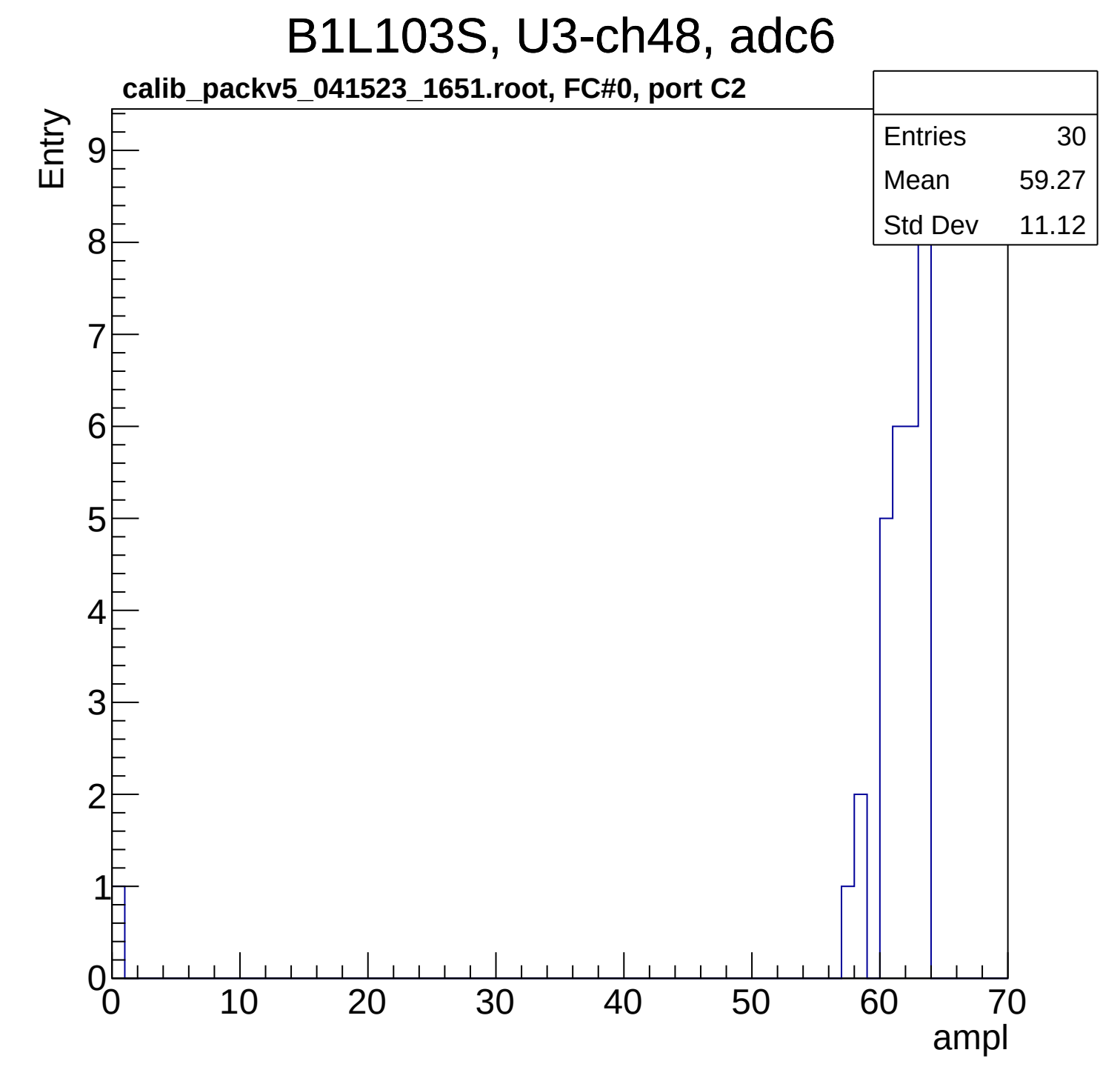
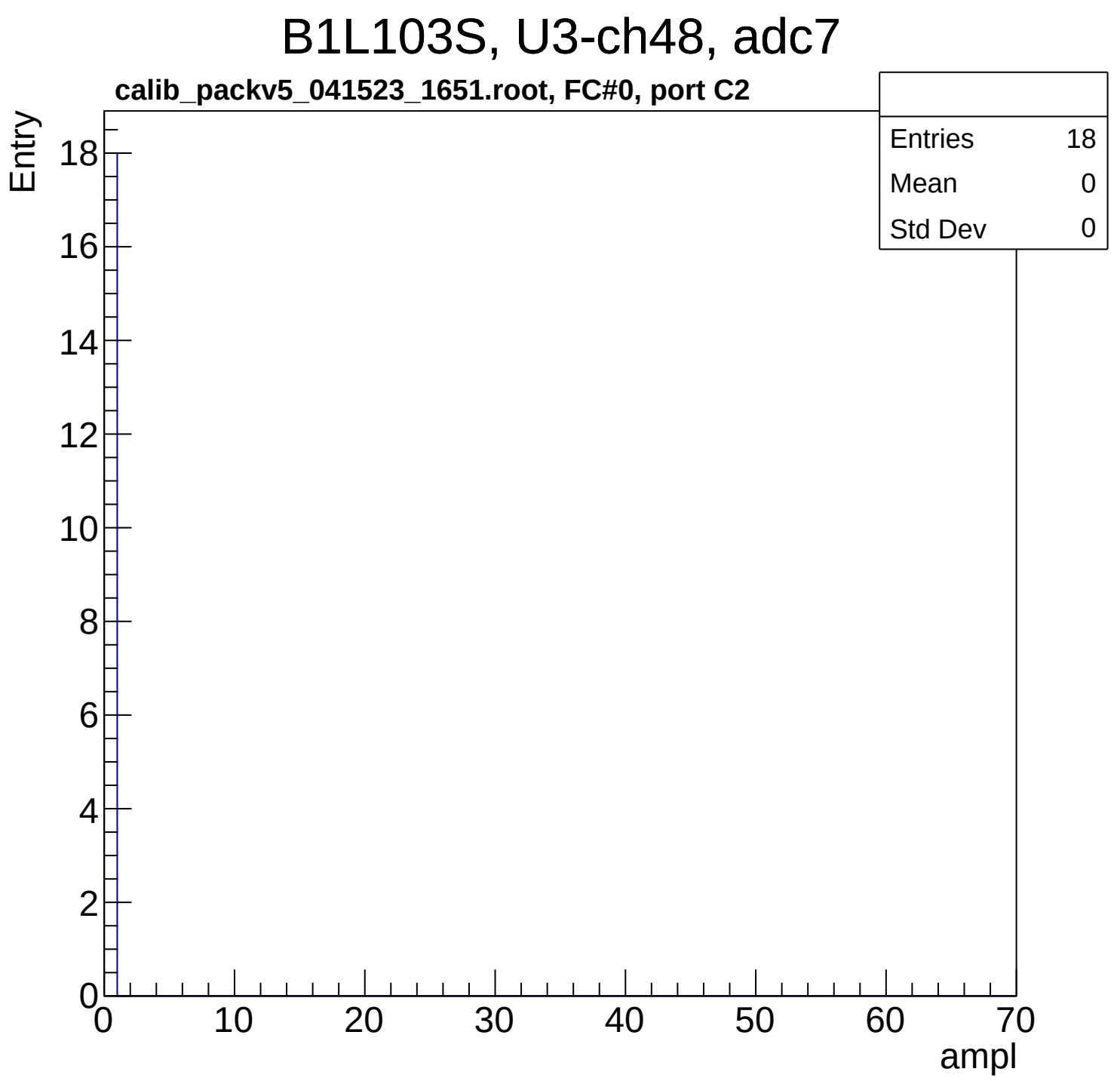
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch48, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 59.27
Std Dev 11.12
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch48, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
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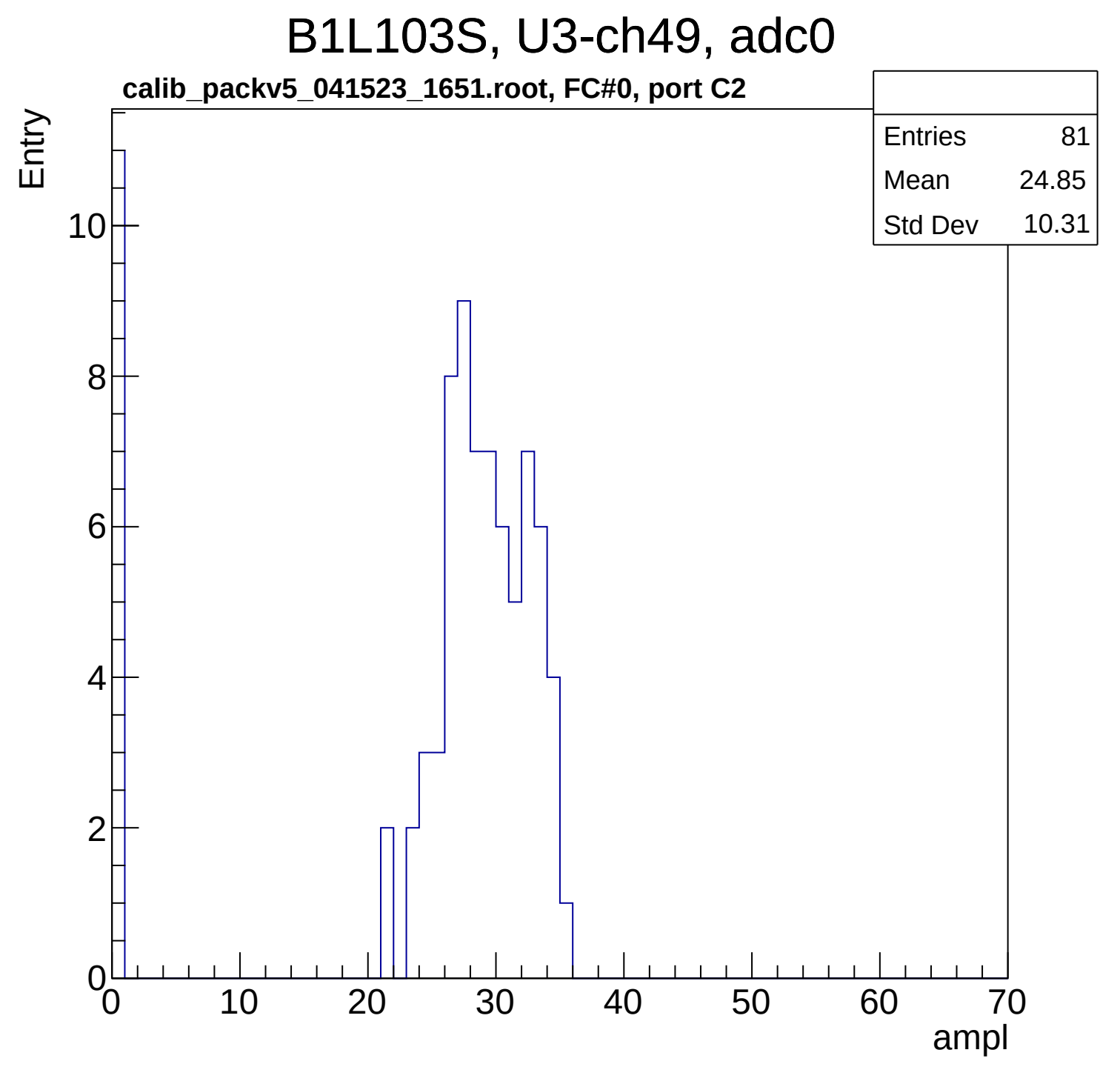
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch49, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 24.85
Std Dev 10.31
Entry
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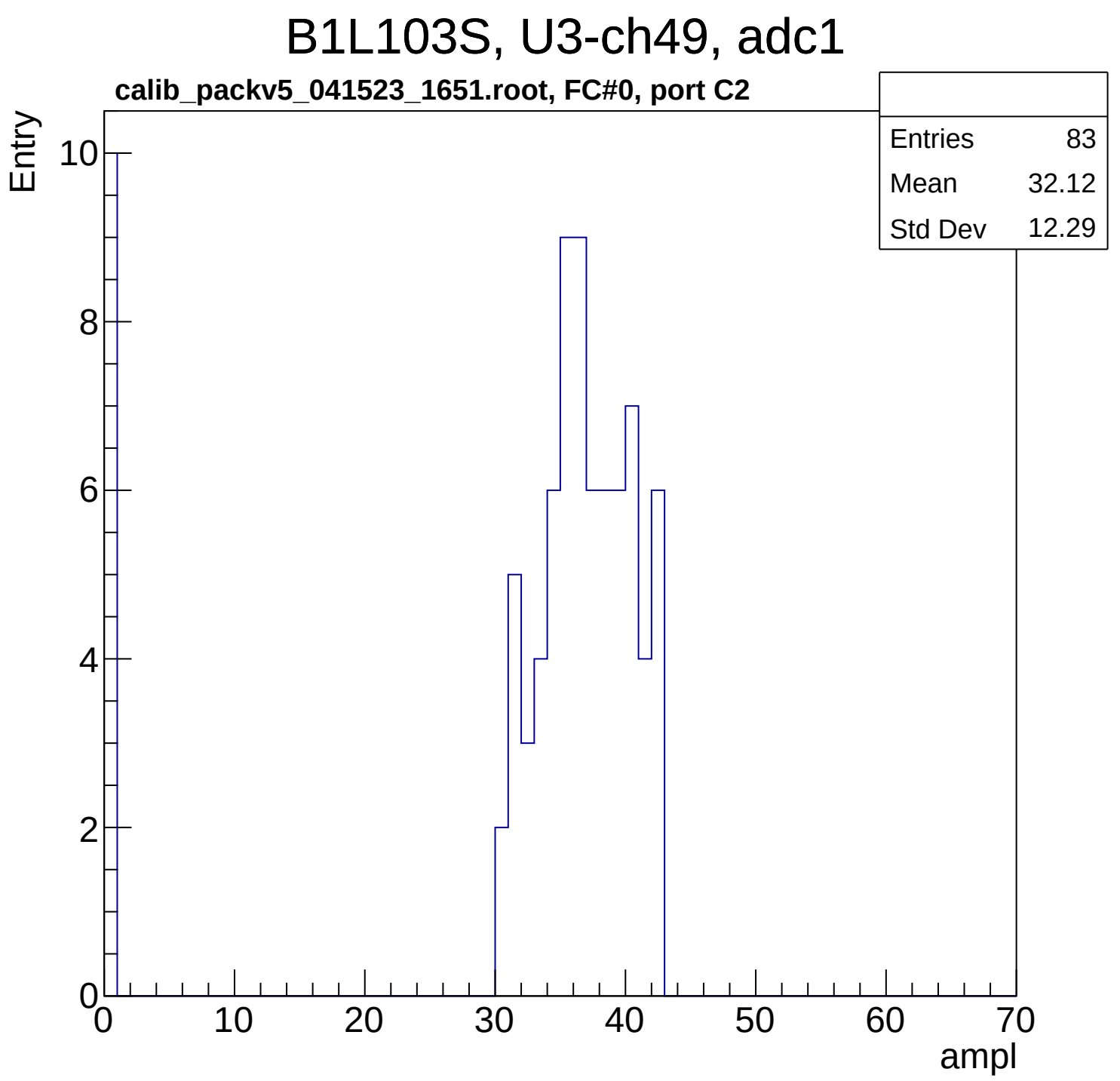
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch49, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 32.12
Std Dev 12.29
Entry
ampl
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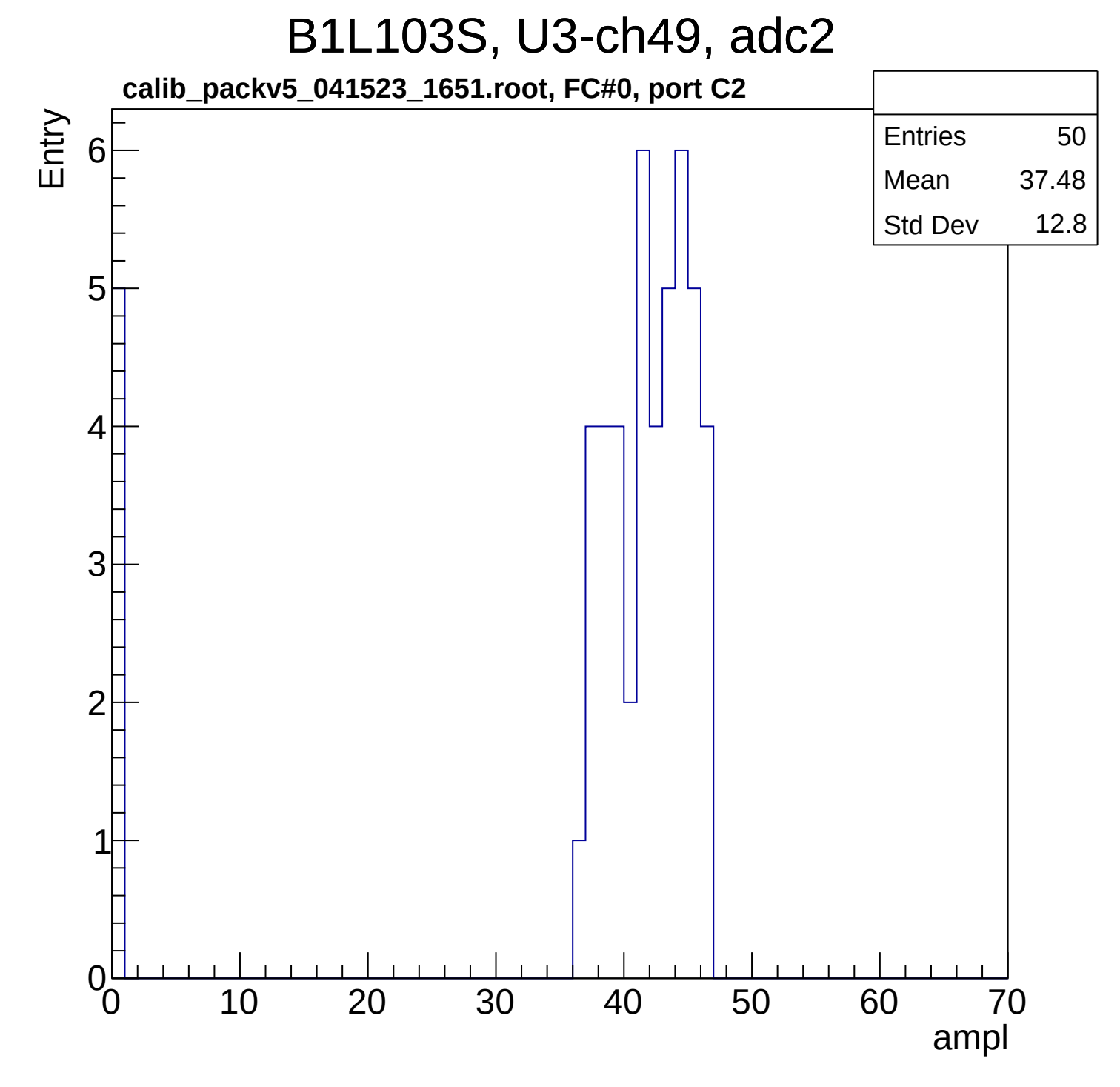
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U3-ch49, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 37.48
Std Dev 12.8
Entry
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2
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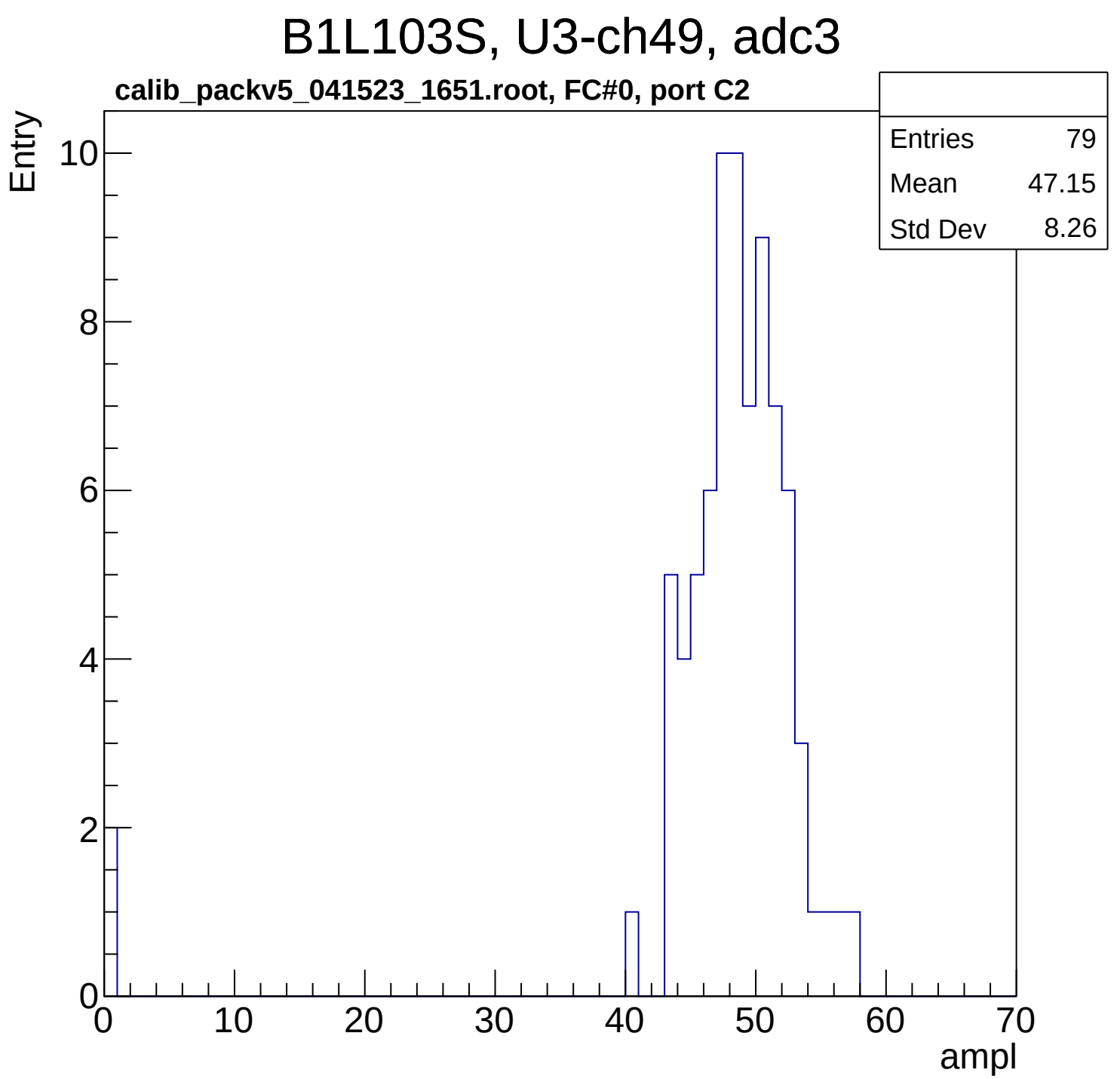
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch49, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 47.15
Std Dev 8.26
Entry
ampl
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4
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8
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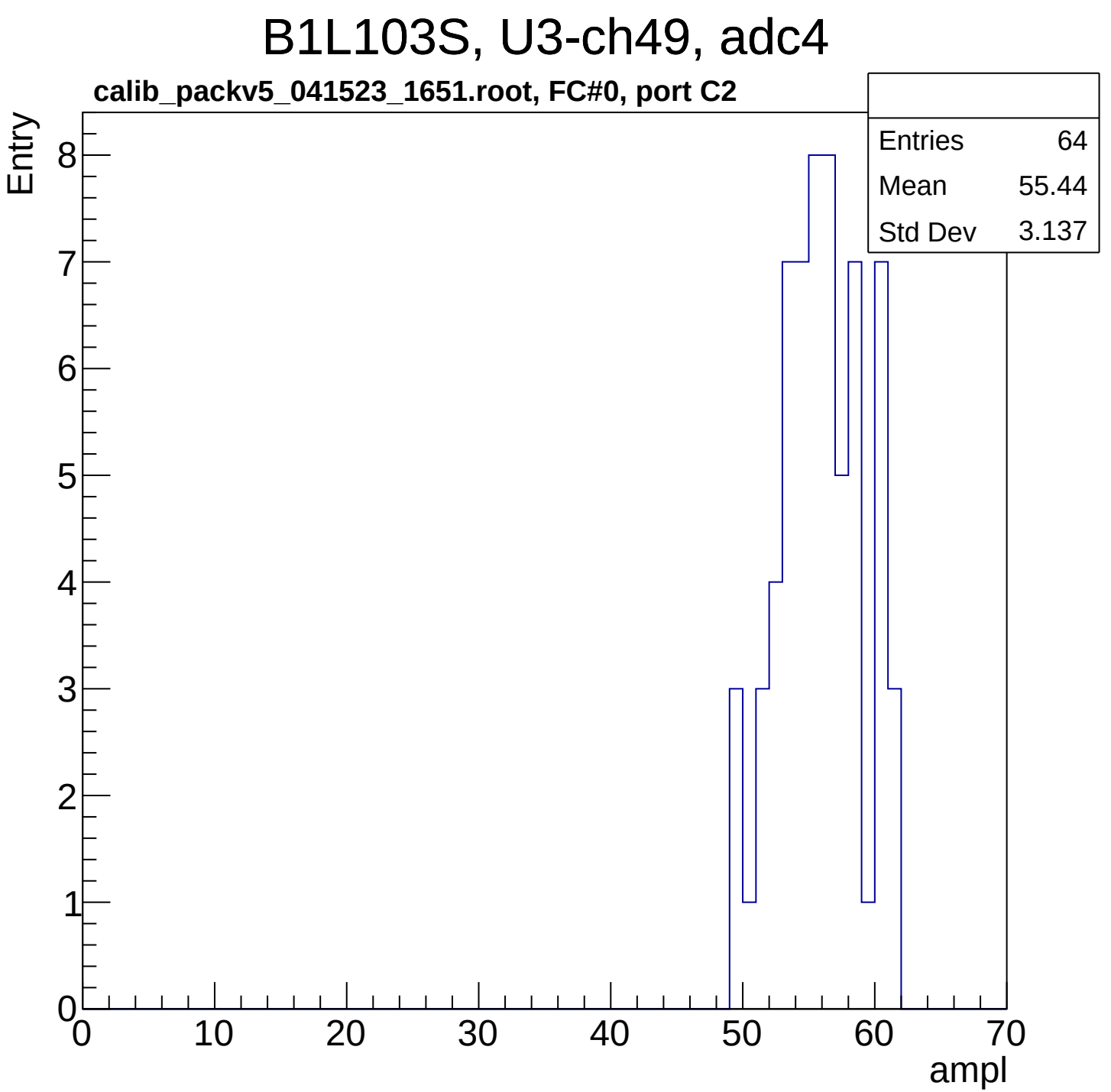
0
10
20
30
40
50
60
70


B1L103S, U3-ch49, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 55.44
Std Dev 3.137
Entry
ampl
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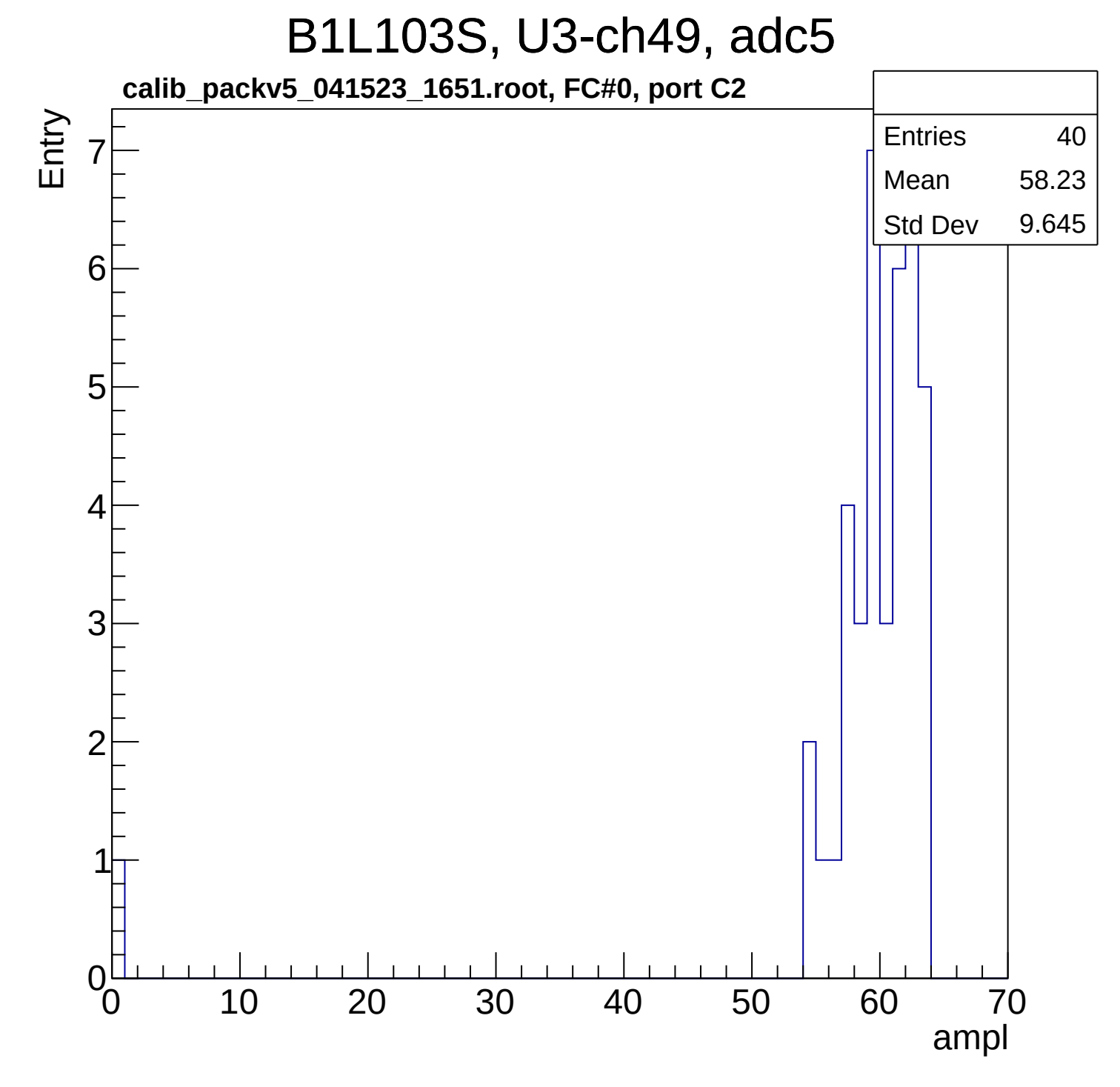
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch49, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 58.23
Std Dev 9.645
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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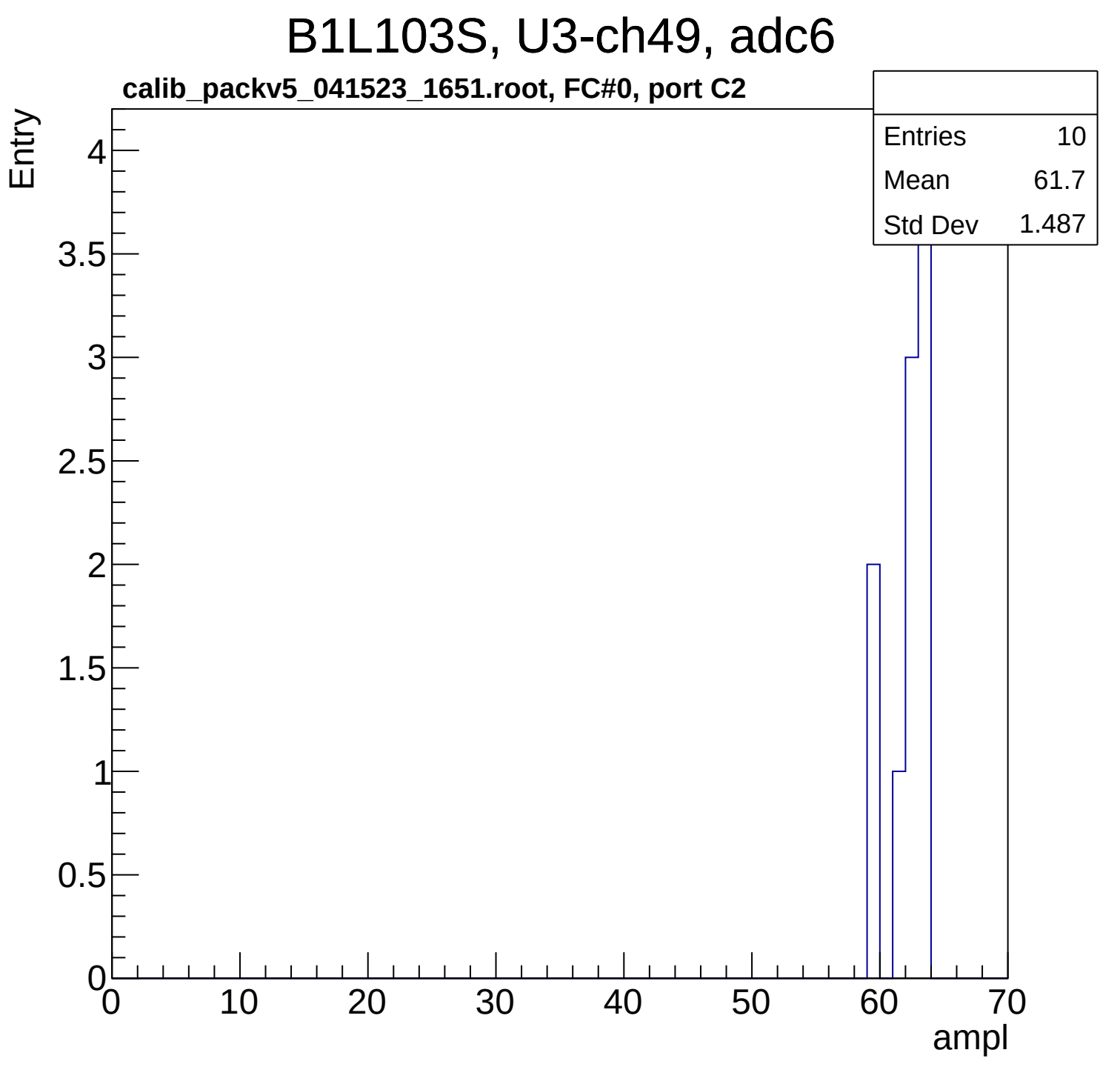
B1L103S, U3-ch49, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61.7
Std Dev 1.487
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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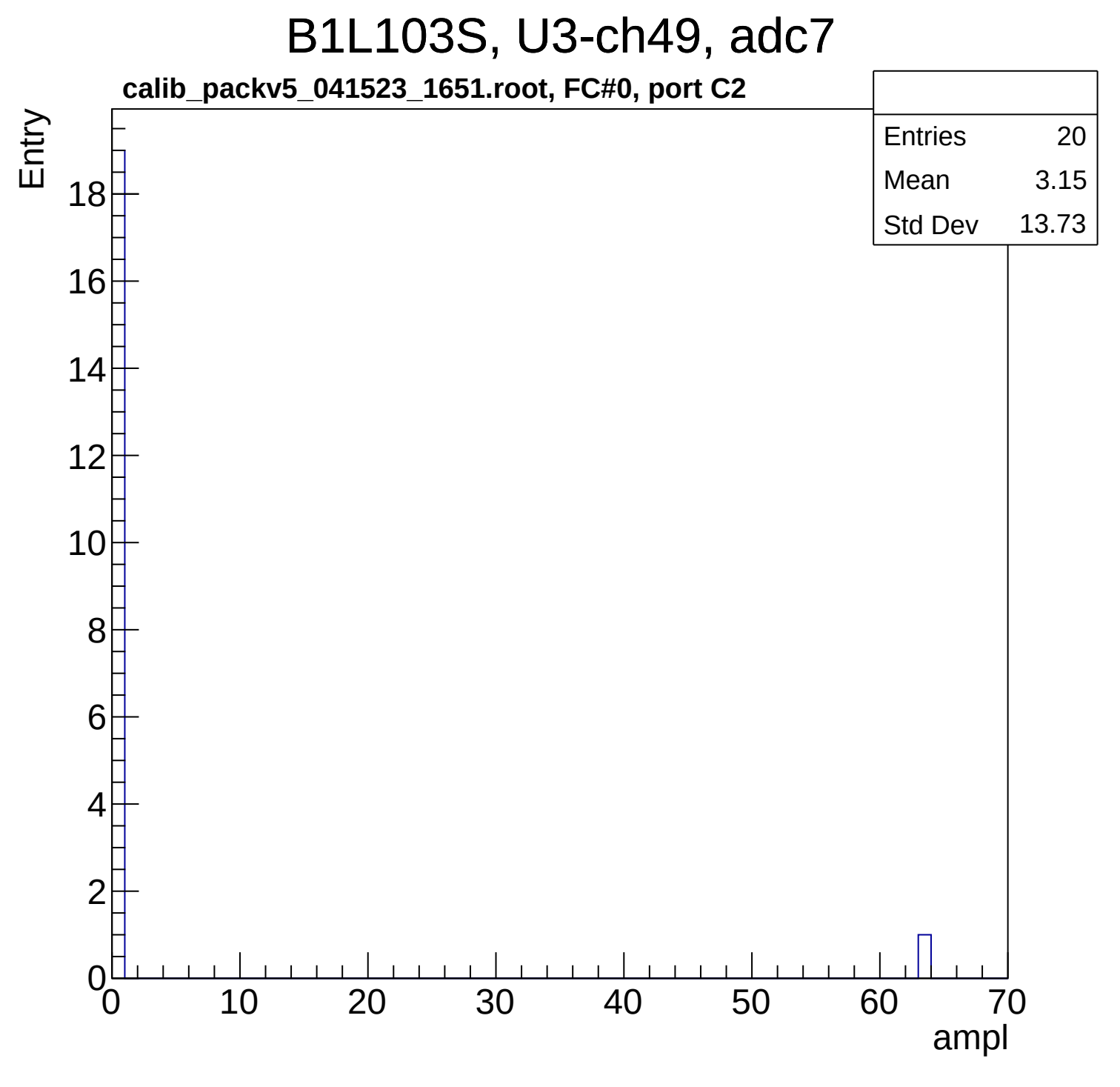
40
50
60
70


B1L103S, U3-ch49, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
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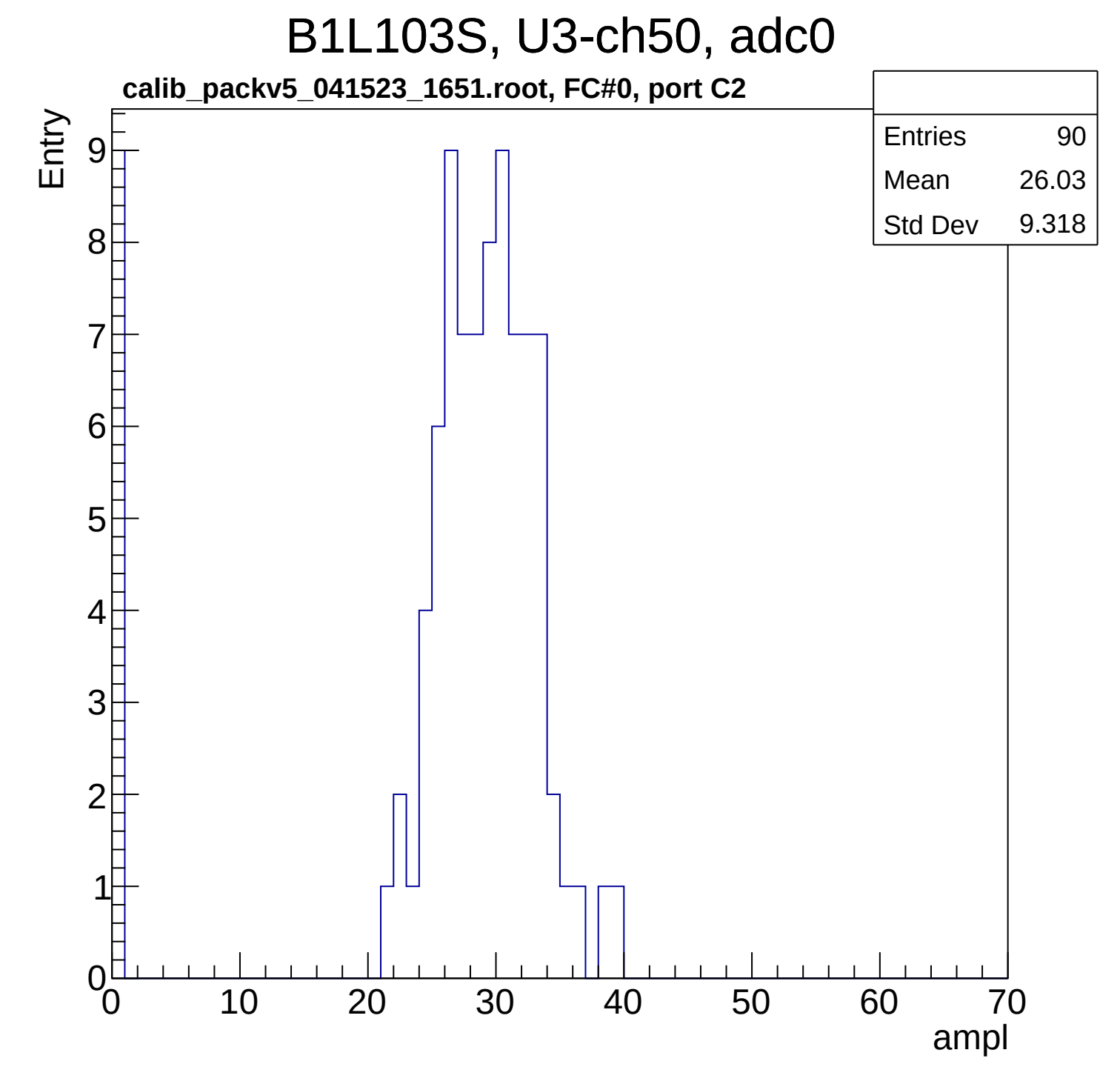
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch50, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 26.03
Std Dev 9.318
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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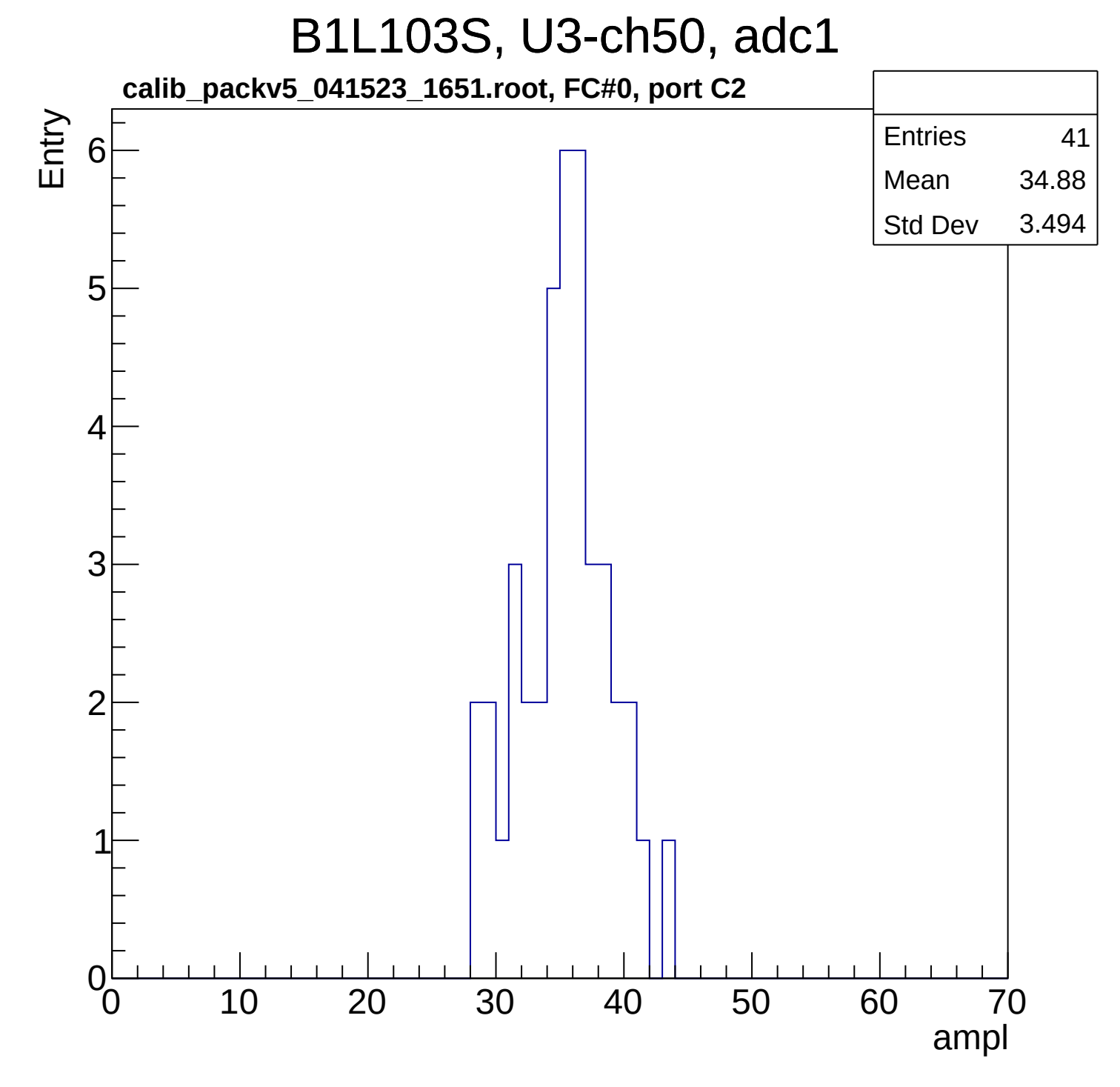
B1L103S, U3-ch50, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 34.88
Std Dev 3.494
Entry
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2
3
4
5
6
0
10
20
30
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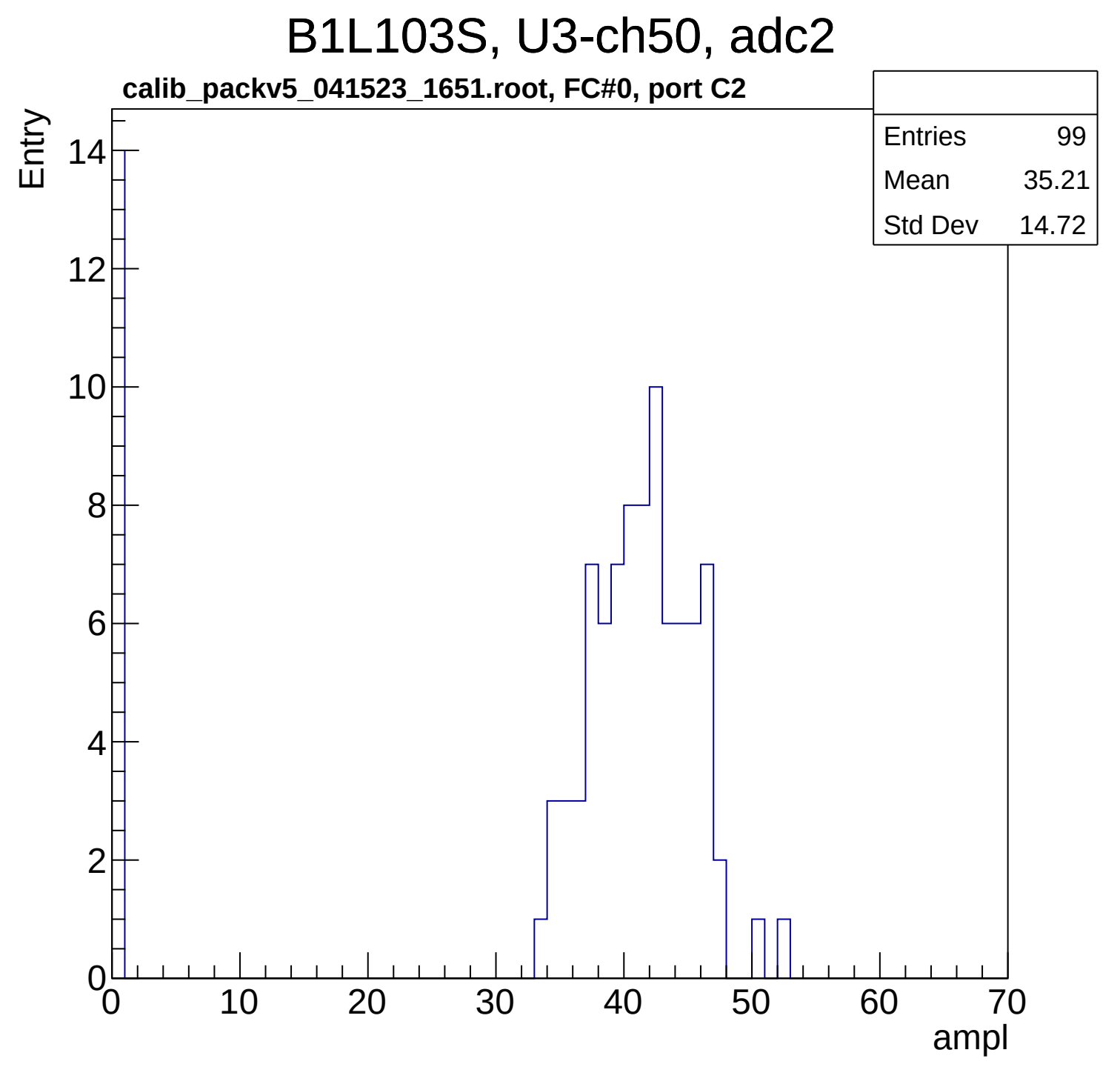
50
60
70
ampl


B1L103S, U3-ch50, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 35.21
Std Dev 14.72
Entry
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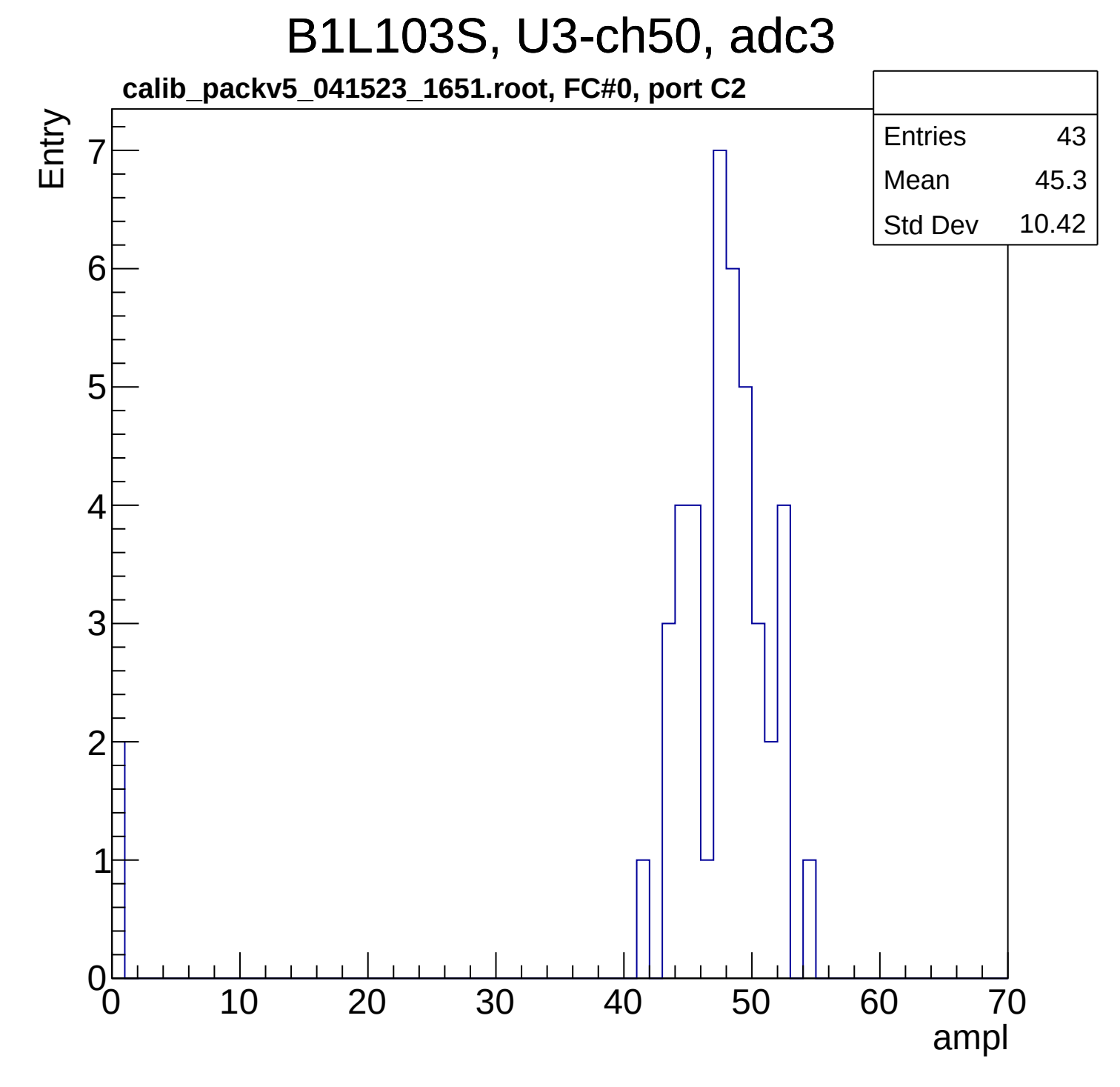
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch50, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 45.3
Std Dev 10.42
Entry
ampl
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4
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0
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60
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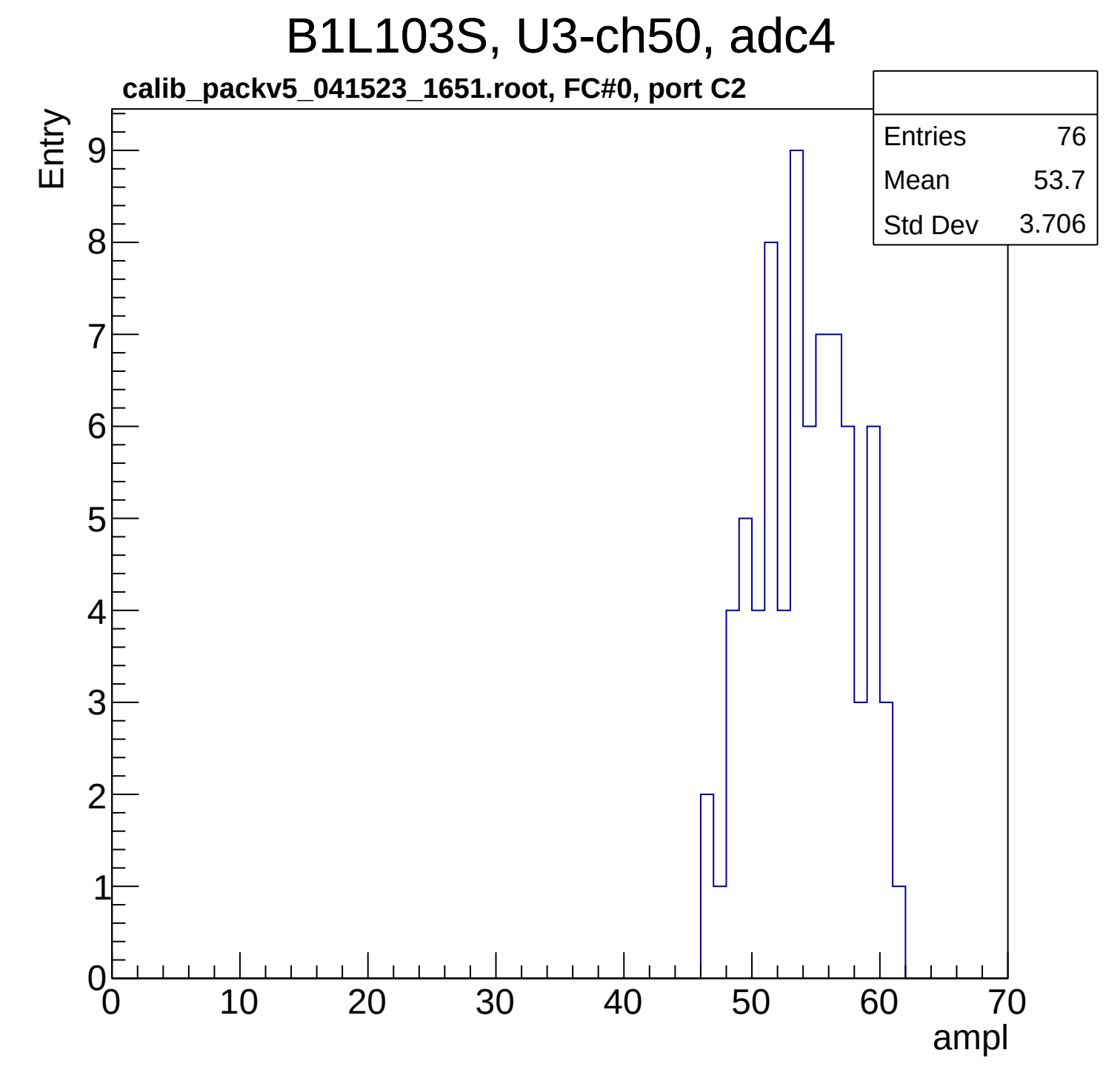
B1L103S, U3-ch50, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 53.7
Std Dev 3.706
Entry
ampl
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2
3
4
5
6
7
8
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0
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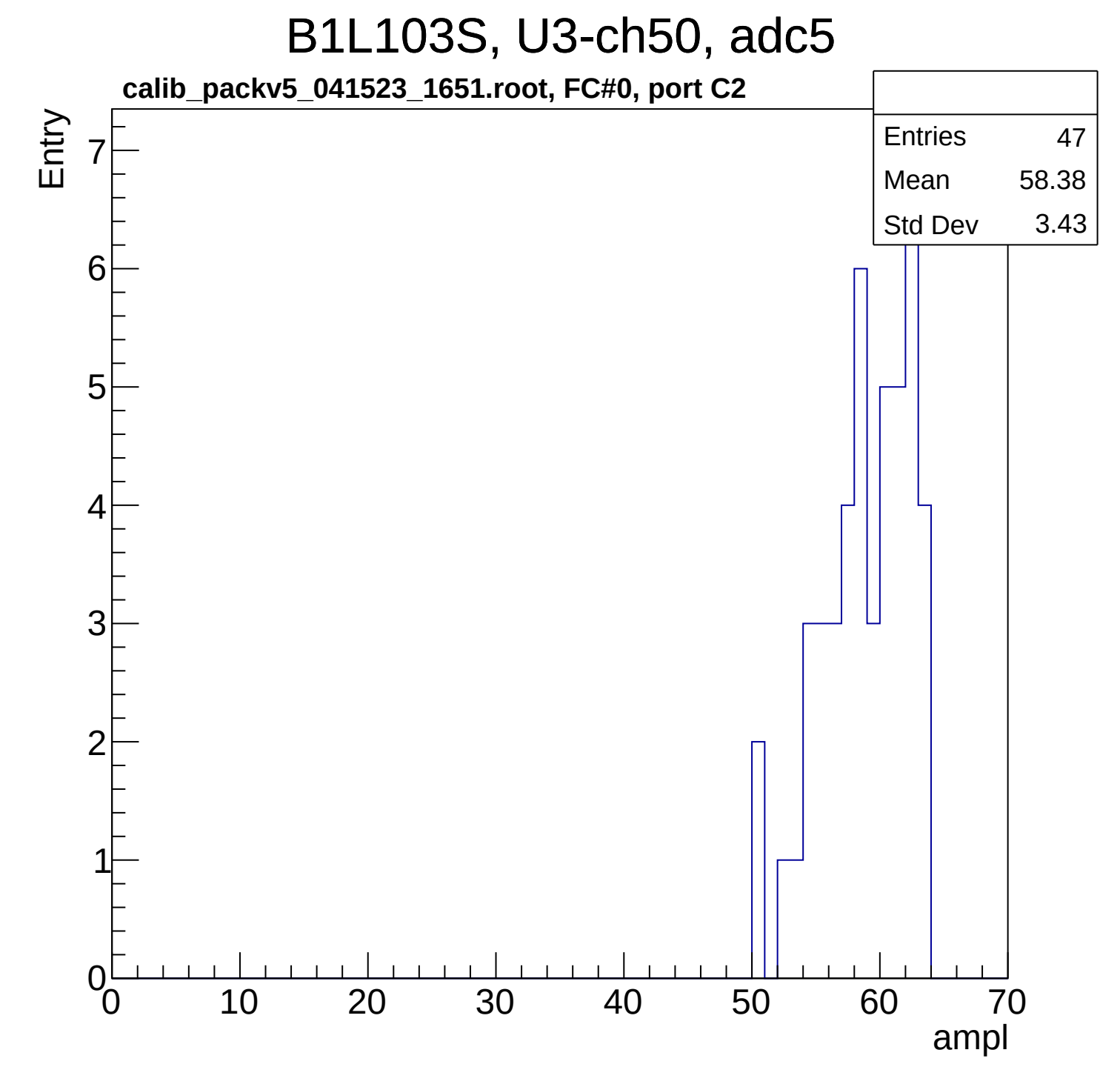
B1L103S, U3-ch50, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 58.38
Std Dev 3.43
Entry
ampl
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0
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60
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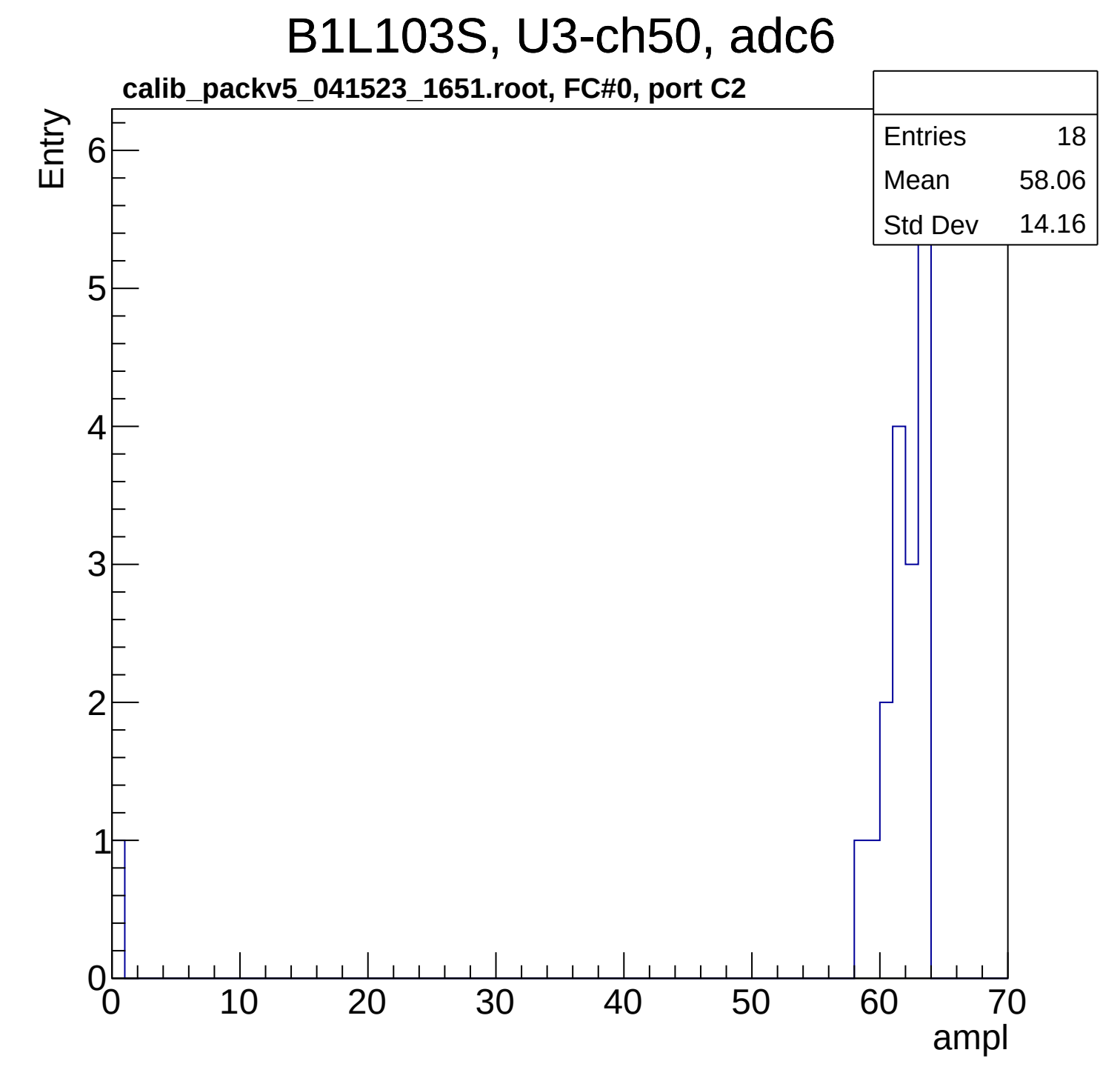
B1L103S, U3-ch50, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 58.06
Std Dev 14.16
Entry
0
1
2
3
4
5
6
0
10
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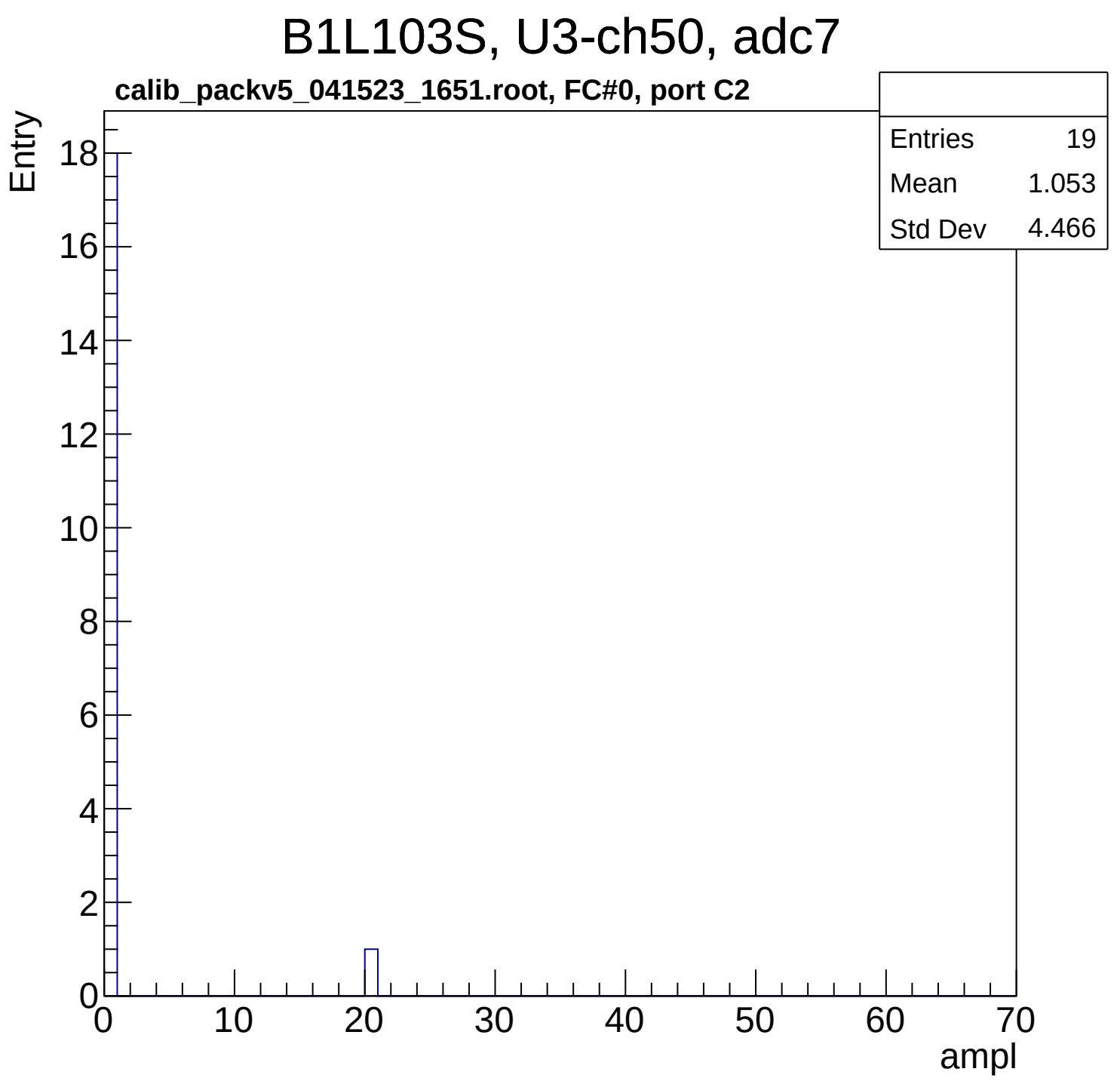
70
ampl


B1L103S, U3-ch50, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.053
Std Dev 4.466
Entry
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6
8
10
12
14
16
18
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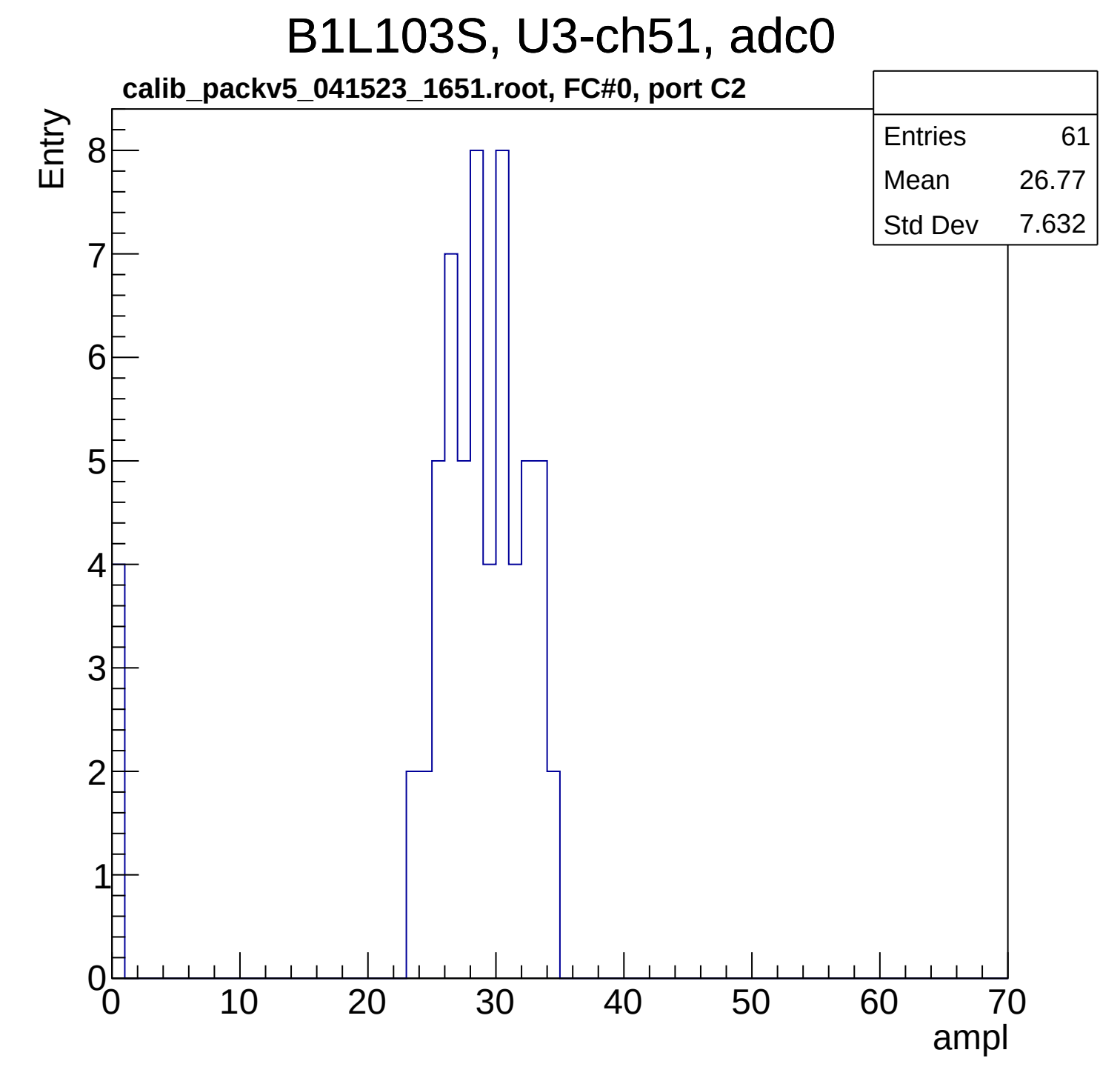
70
ampl


B1L103S, U3-ch51, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 26.77
Std Dev 7.632
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
50
60
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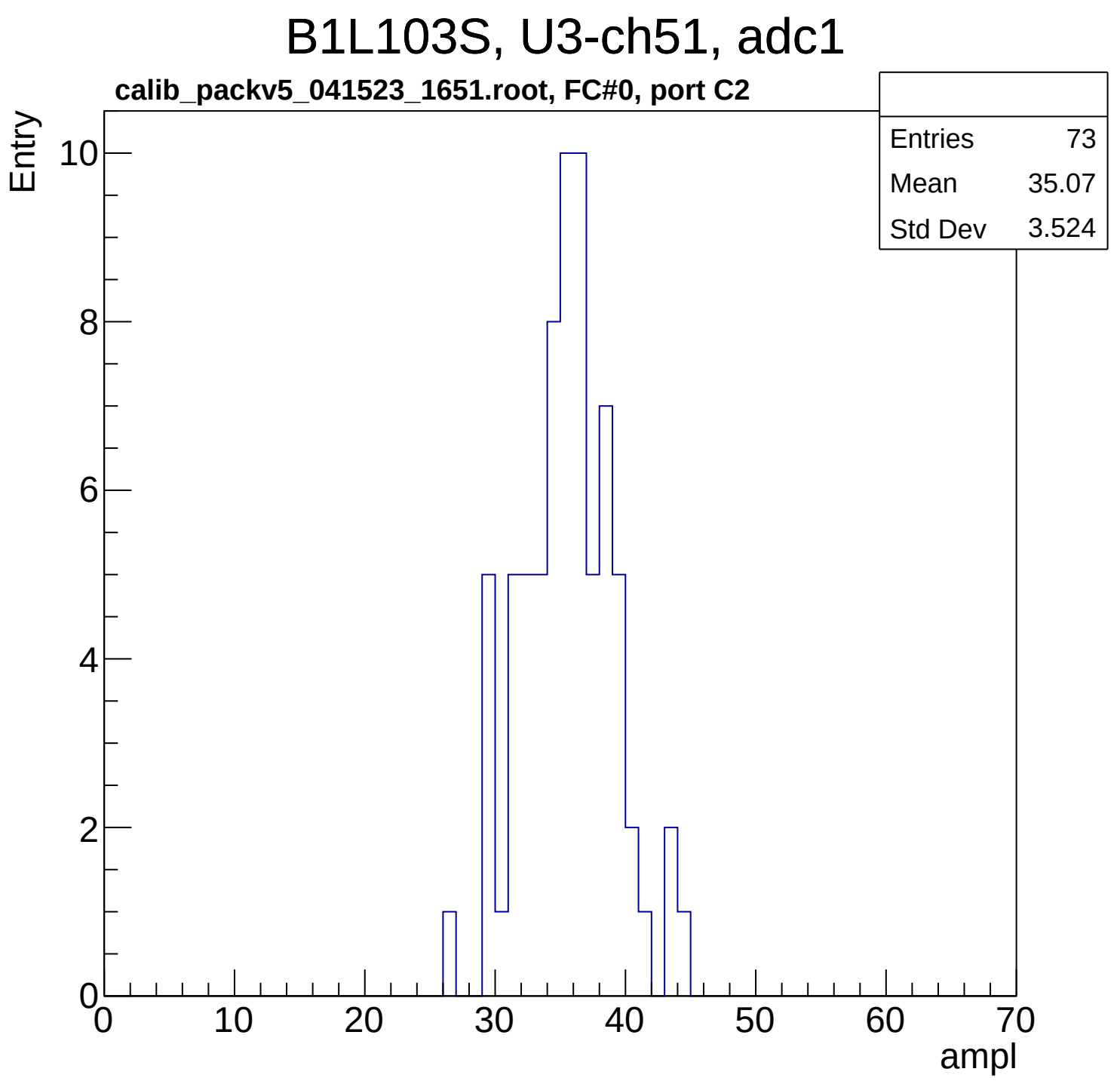
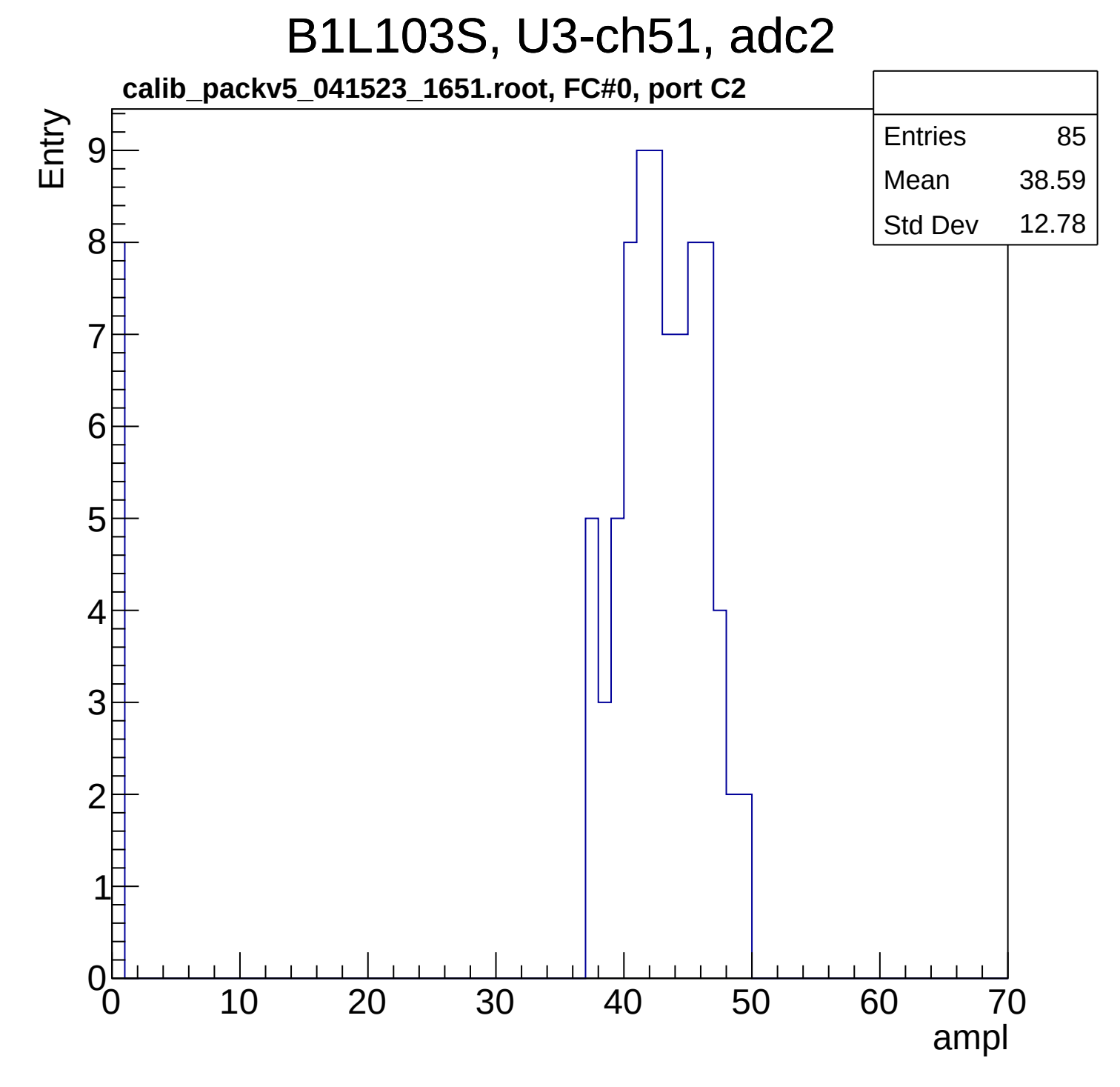

B1L103S, U3-ch51, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 35.07
Std Dev 3.524
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U3-ch51, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 38.59
Std Dev 12.78
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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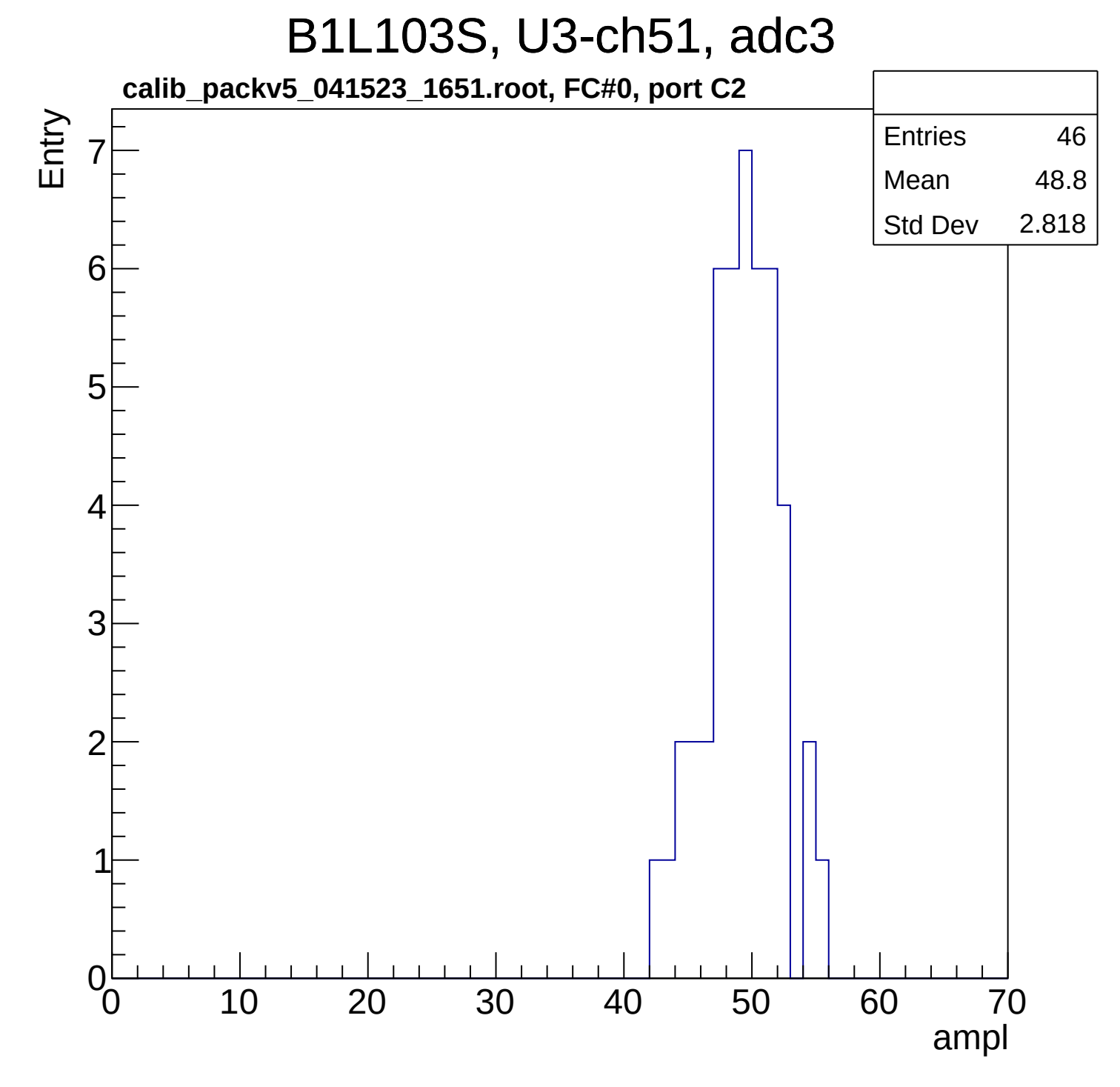
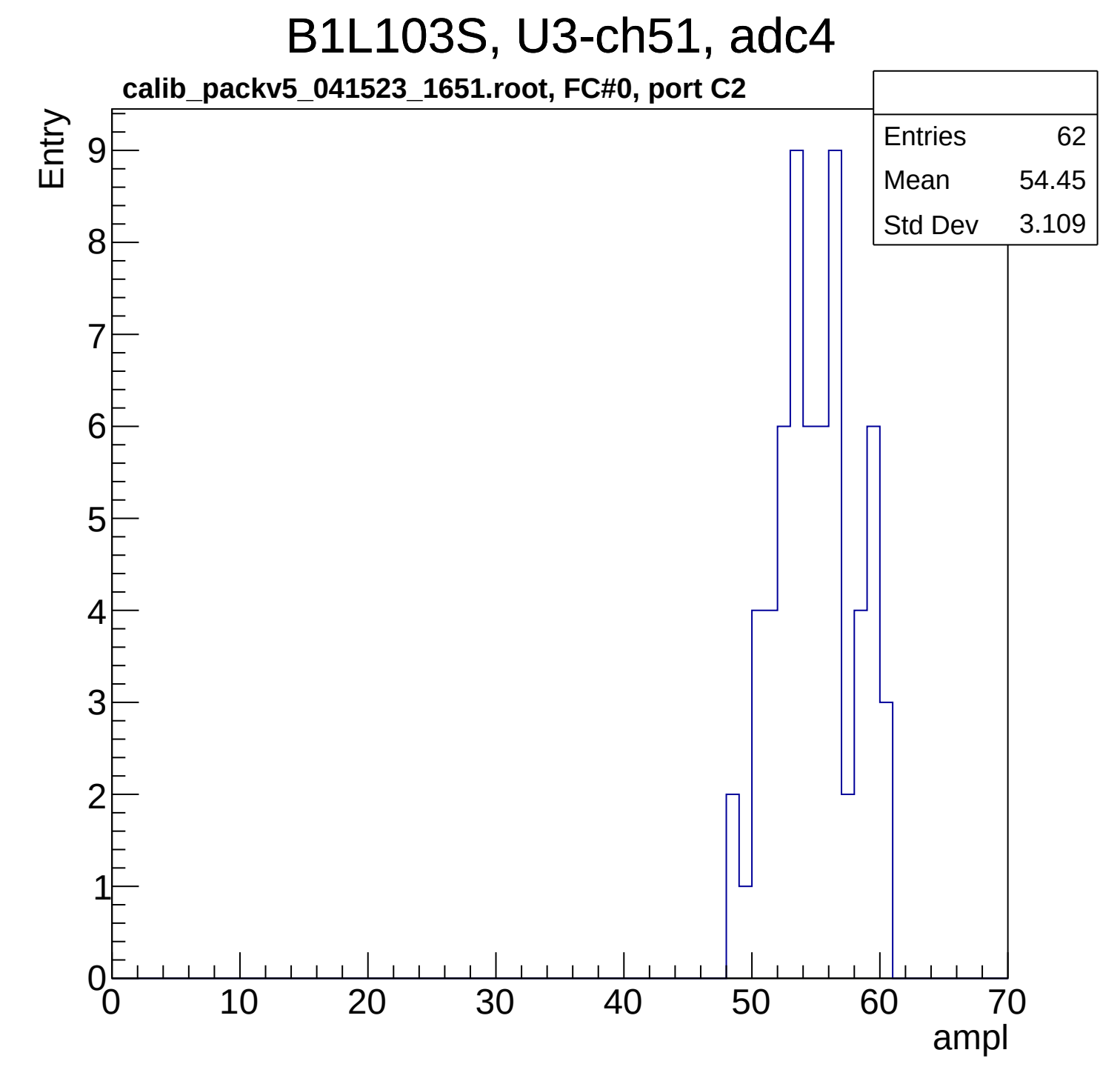

B1L103S, U3-ch51, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 48.8
Std Dev 2.818
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch51, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 54.45
Std Dev 3.109
Entry
ampl
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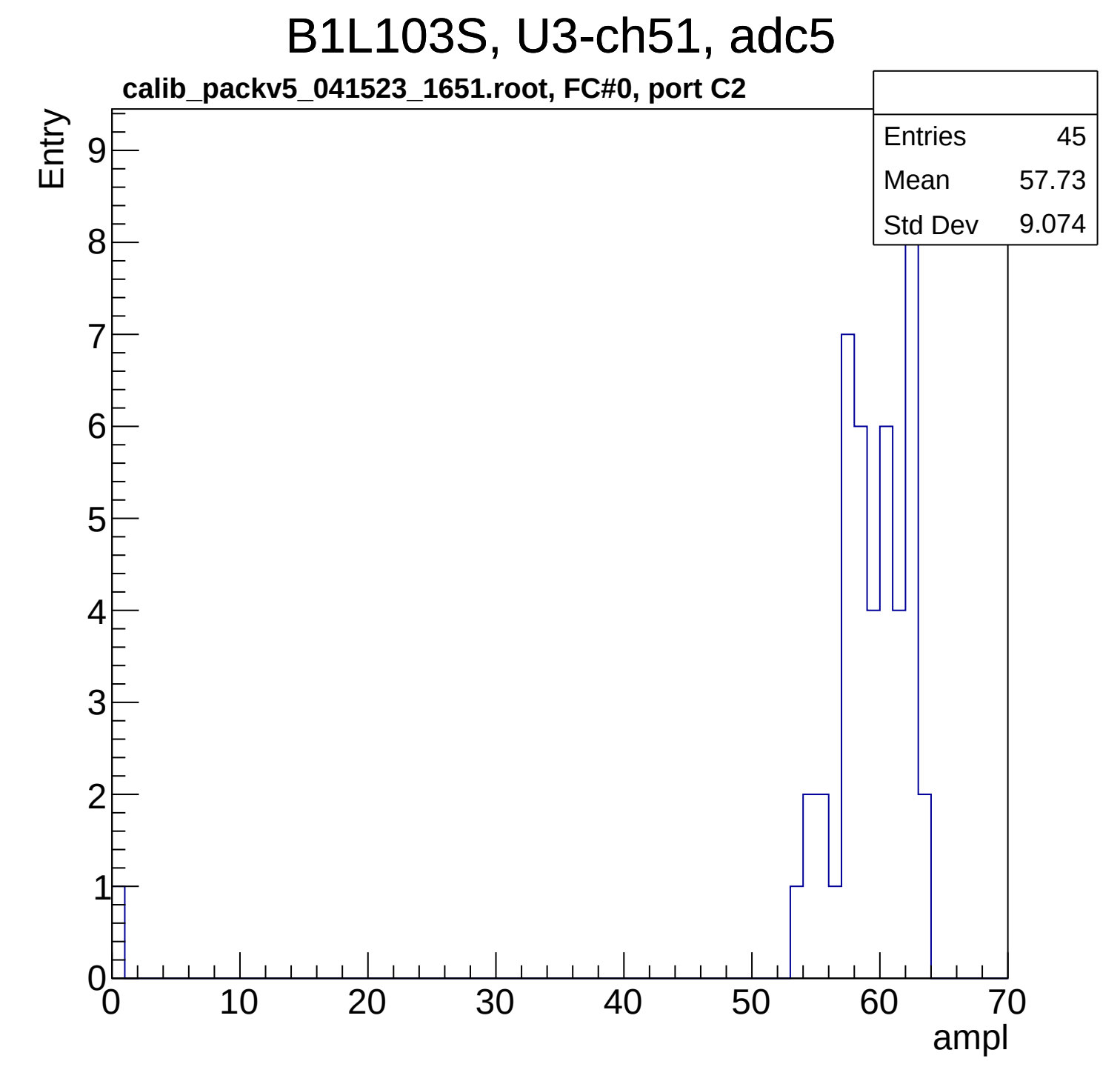
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch51, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 57.73
Std Dev 9.074
Entry
ampl
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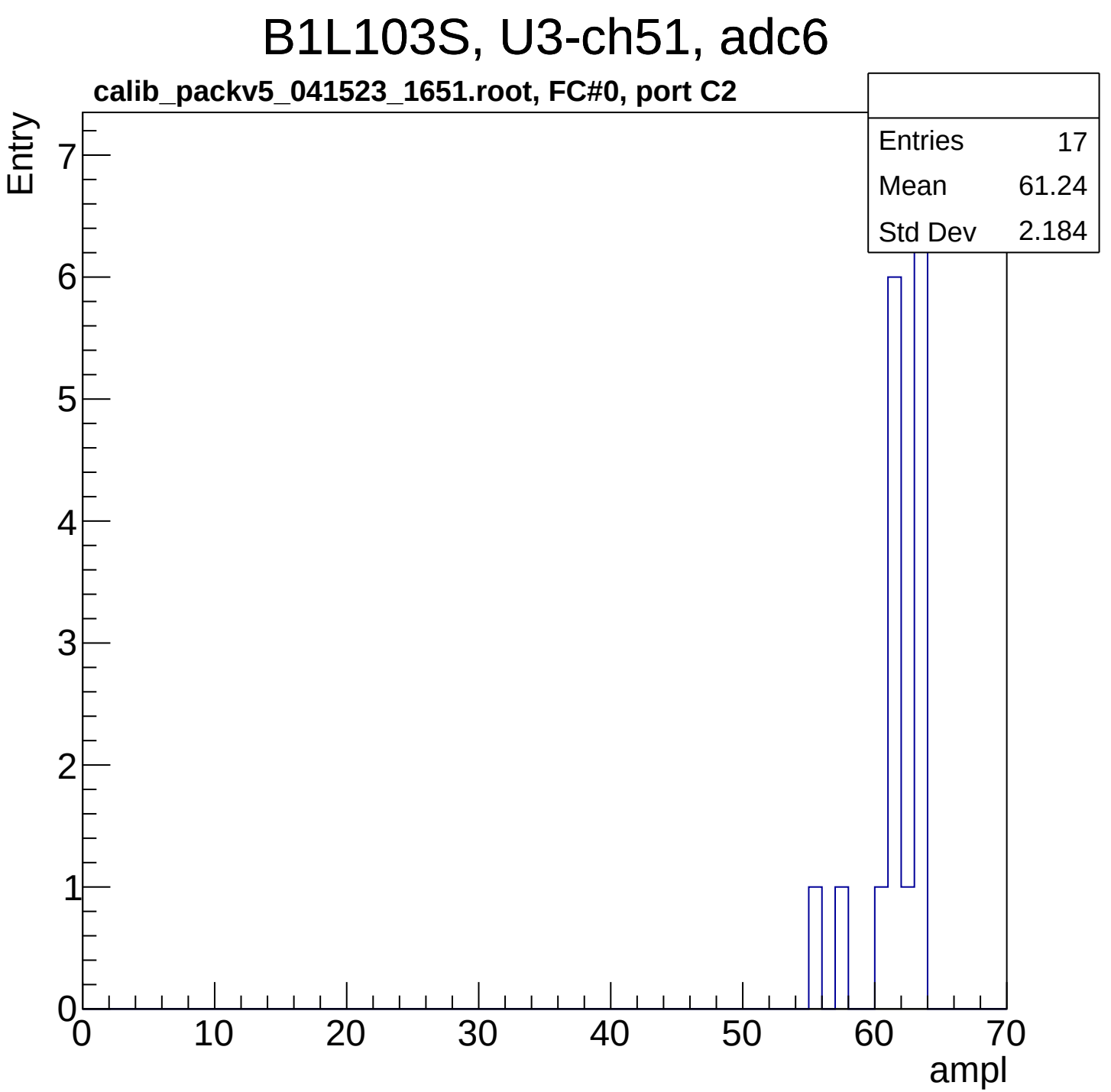
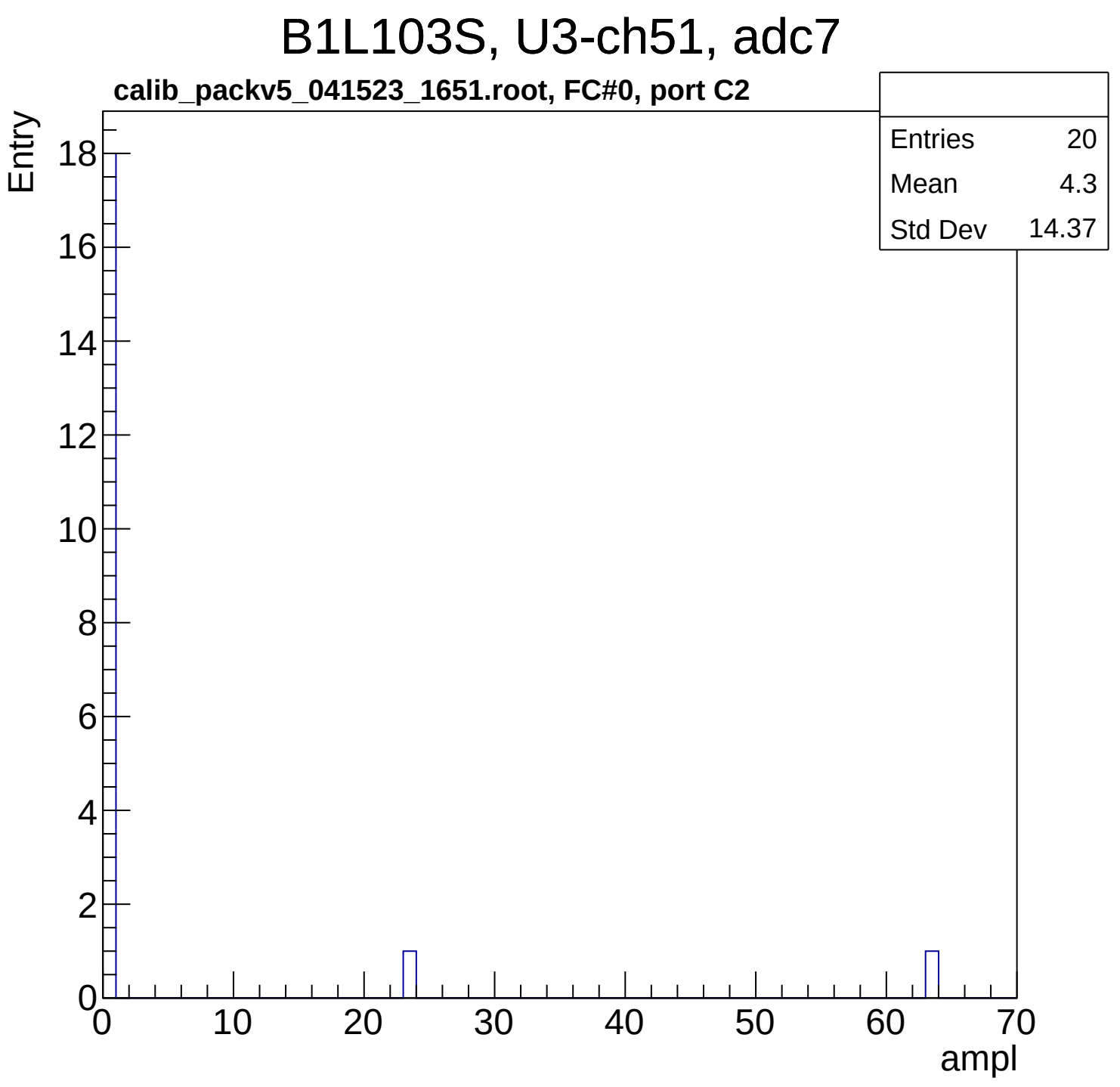
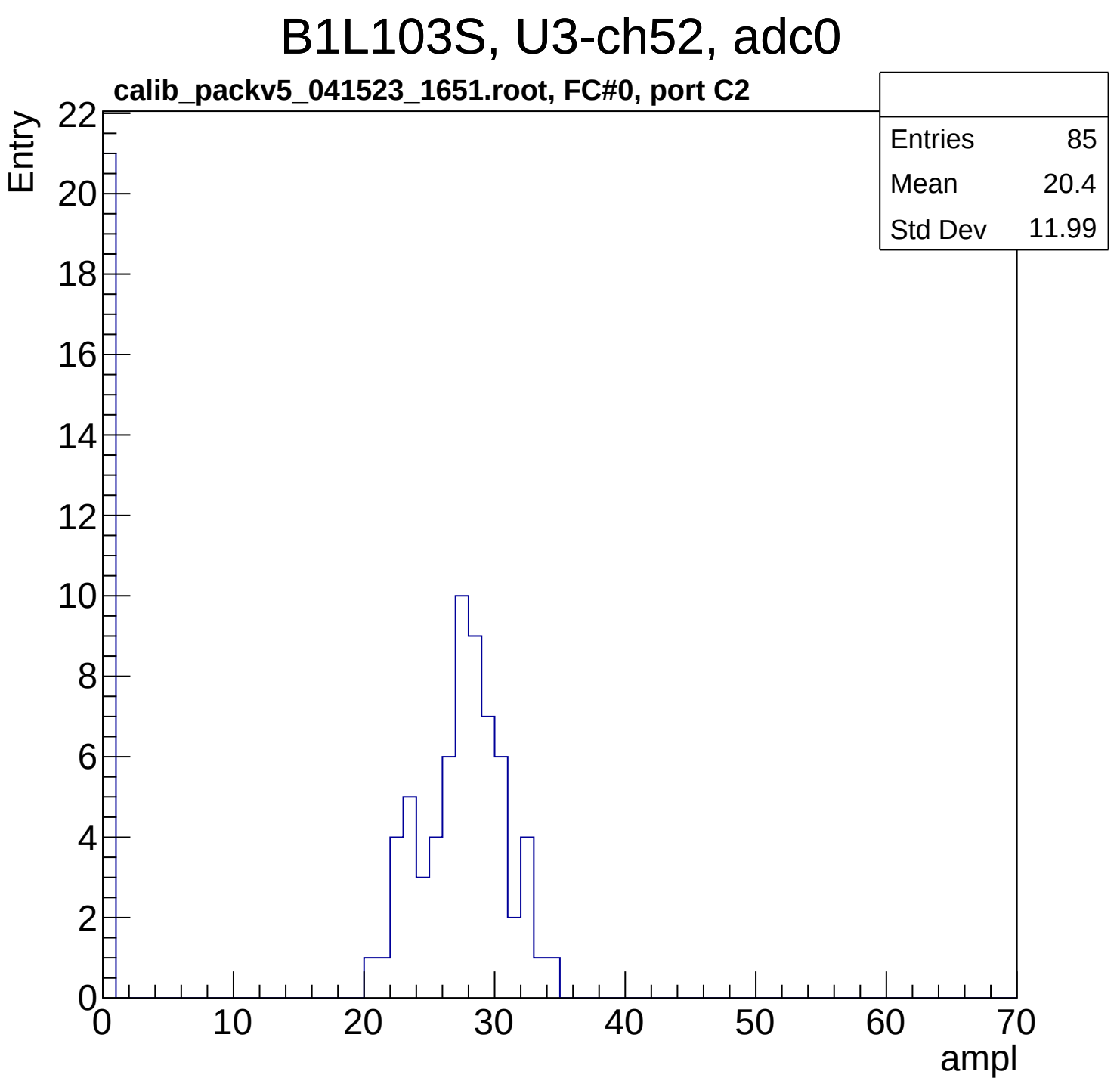
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch51, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 61.24
Std Dev 2.184
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch51, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4.3
Std Dev 14.37
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch52, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 20.4
Std Dev 11.99
Entry
ampl
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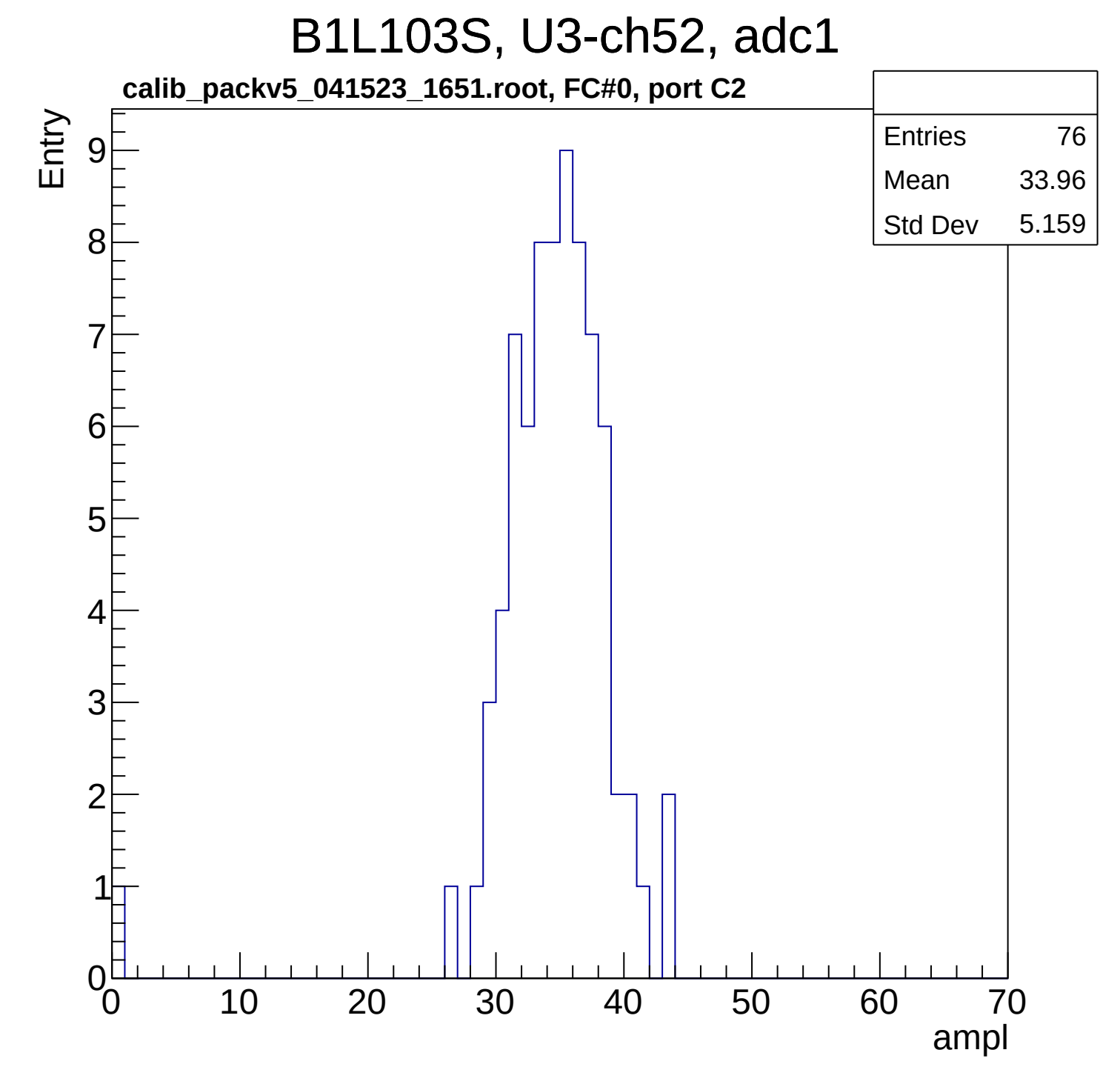
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70


B1L103S, U3-ch52, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 33.96
Std Dev 5.159
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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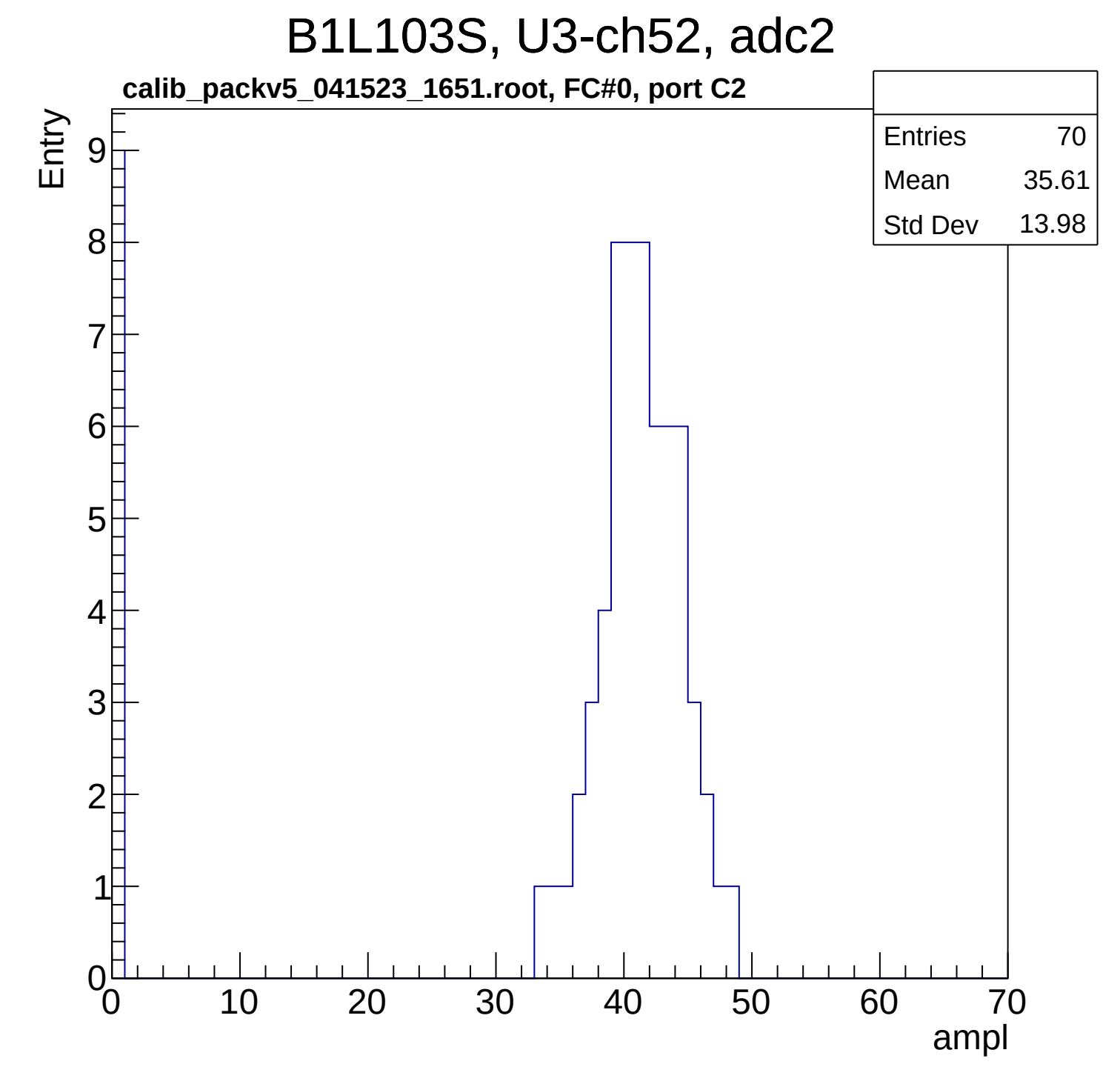
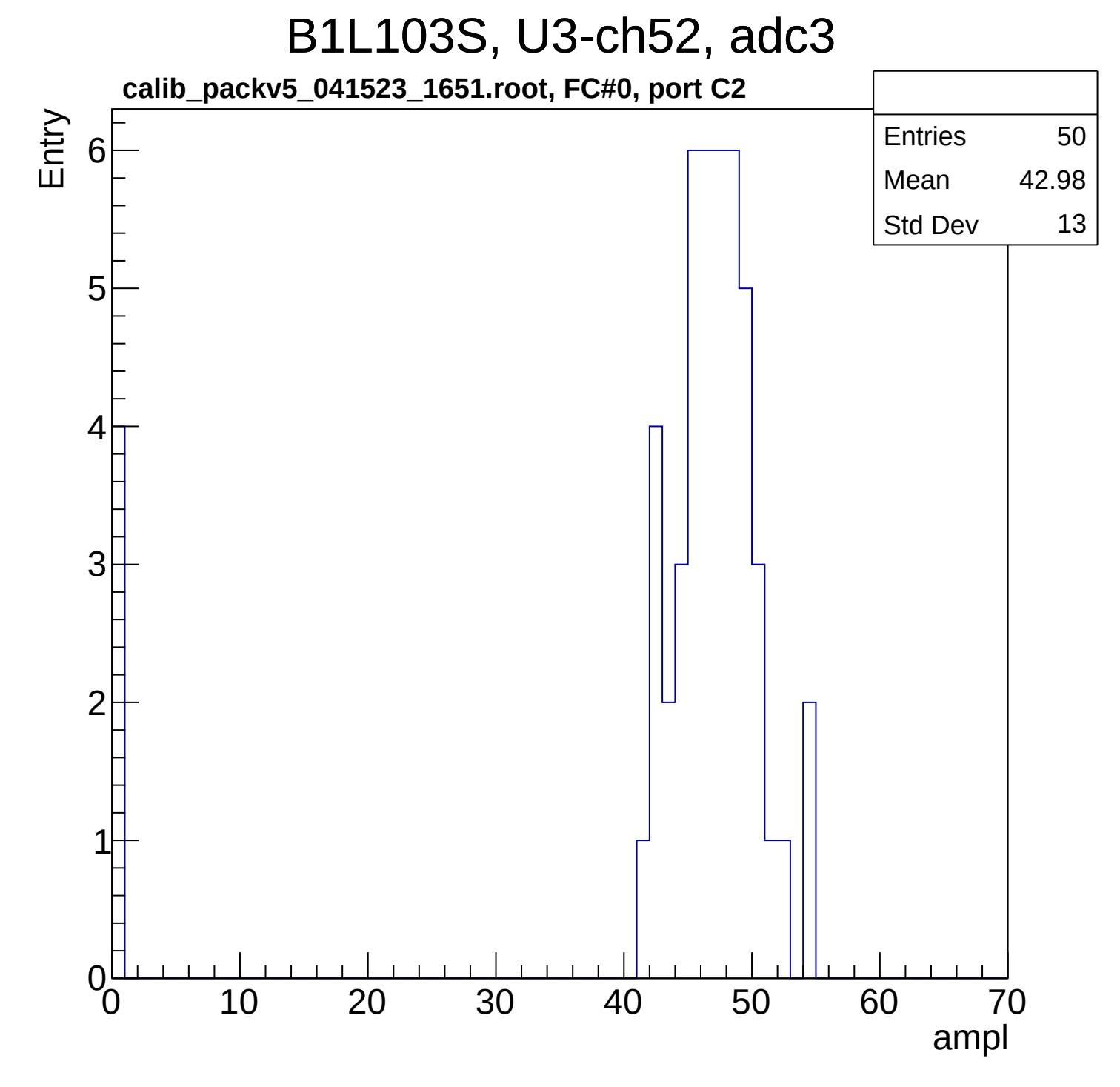

B1L103S, U3-ch52, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 35.61
Std Dev 13.98
Entry
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch52, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 42.98
Std Dev 13
Entry
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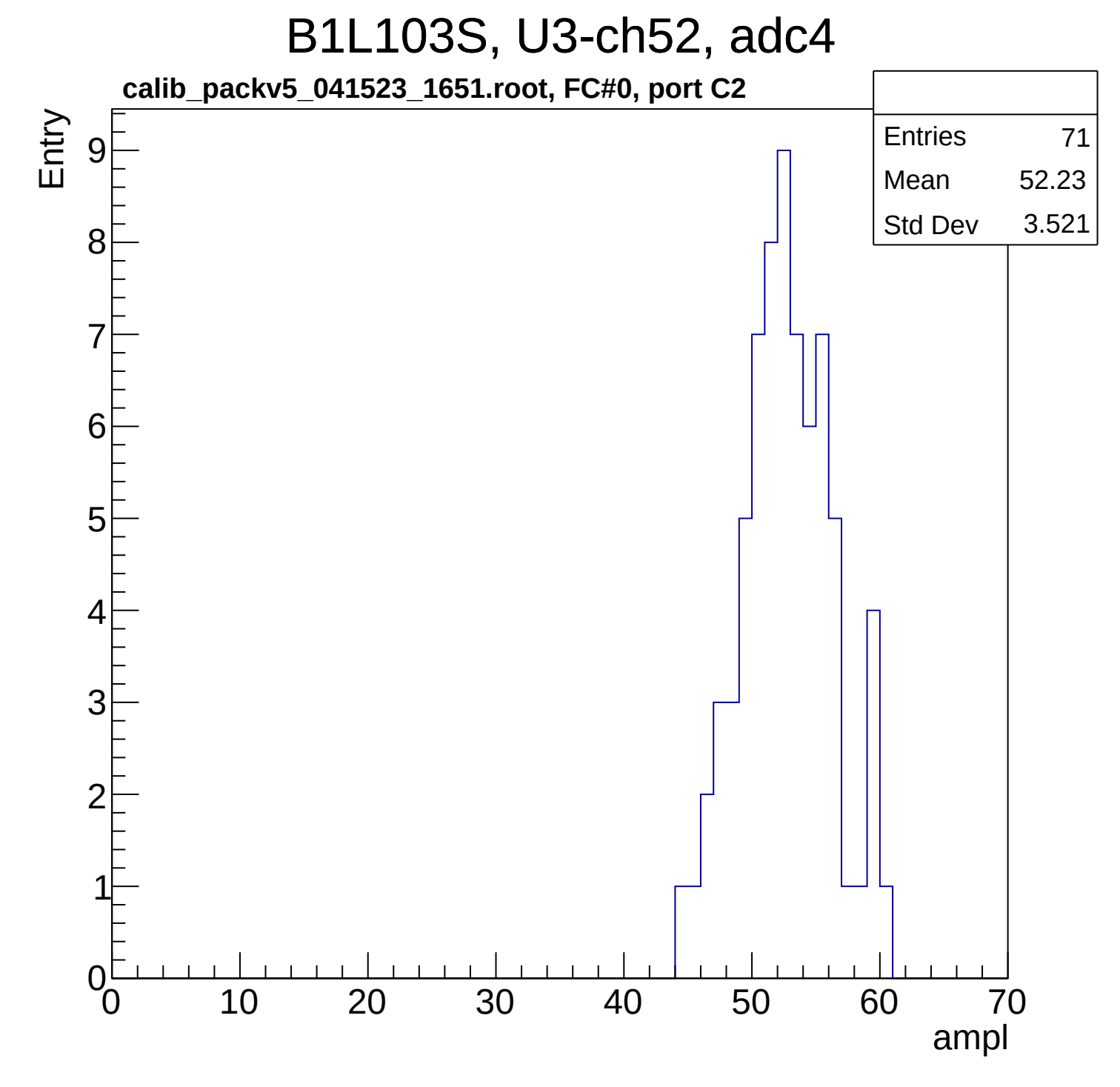
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch52, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 52.23
Std Dev 3.521
Entry
ampl
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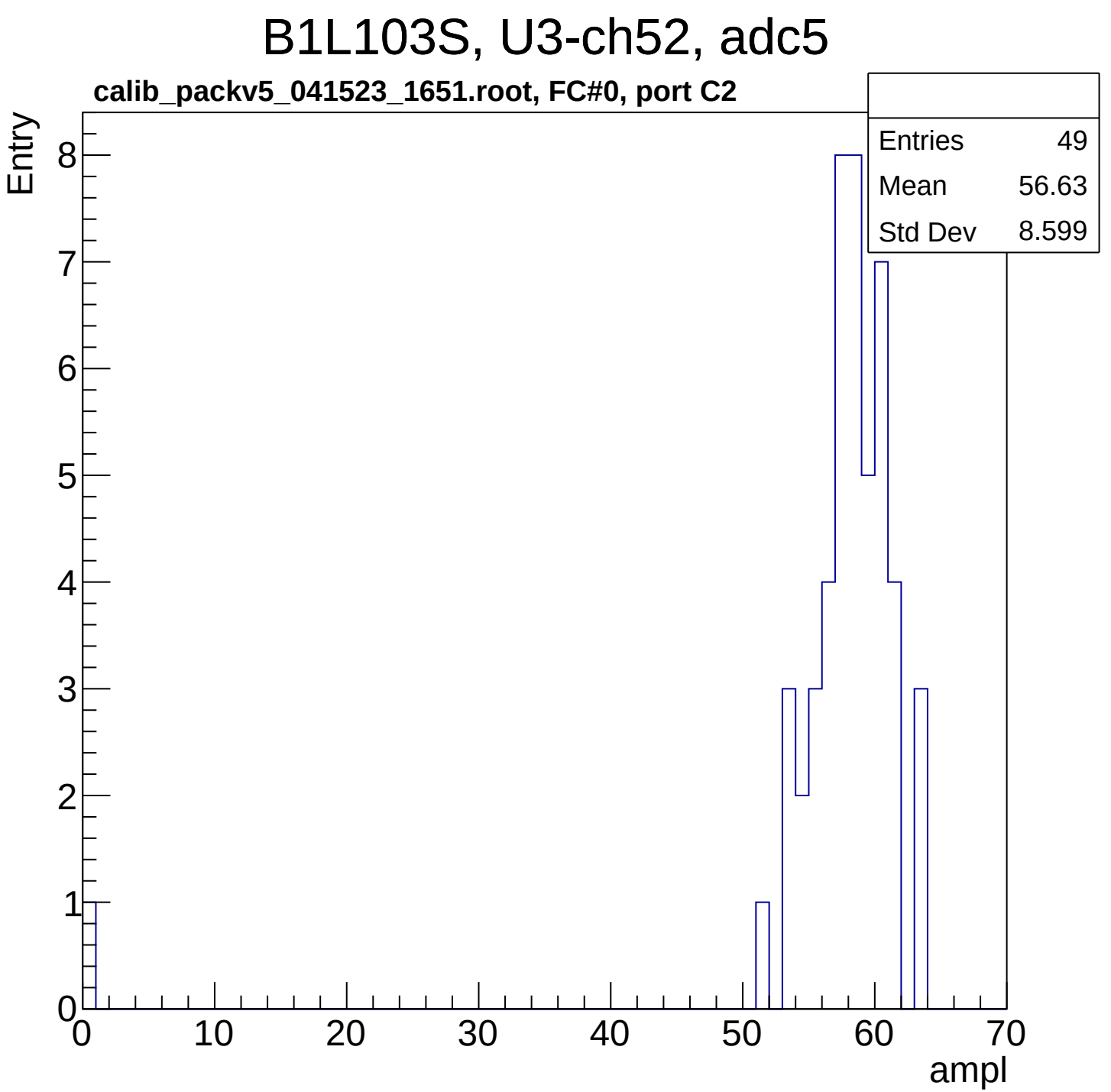
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch52, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 56.63
Std Dev 8.599
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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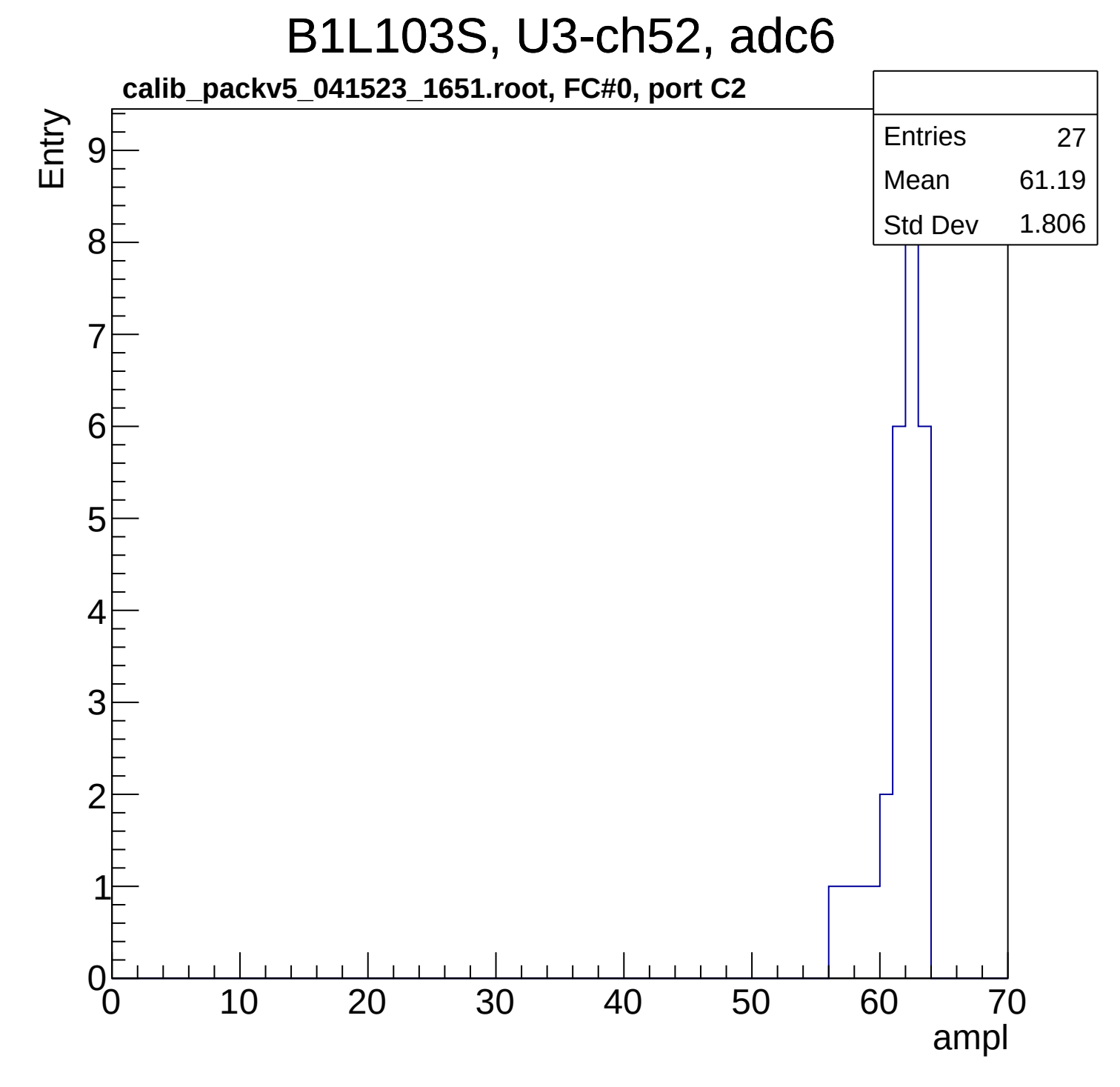
40
50
60
70


B1L103S, U3-ch52, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 61.19
Std Dev 1.806
Entry
ampl
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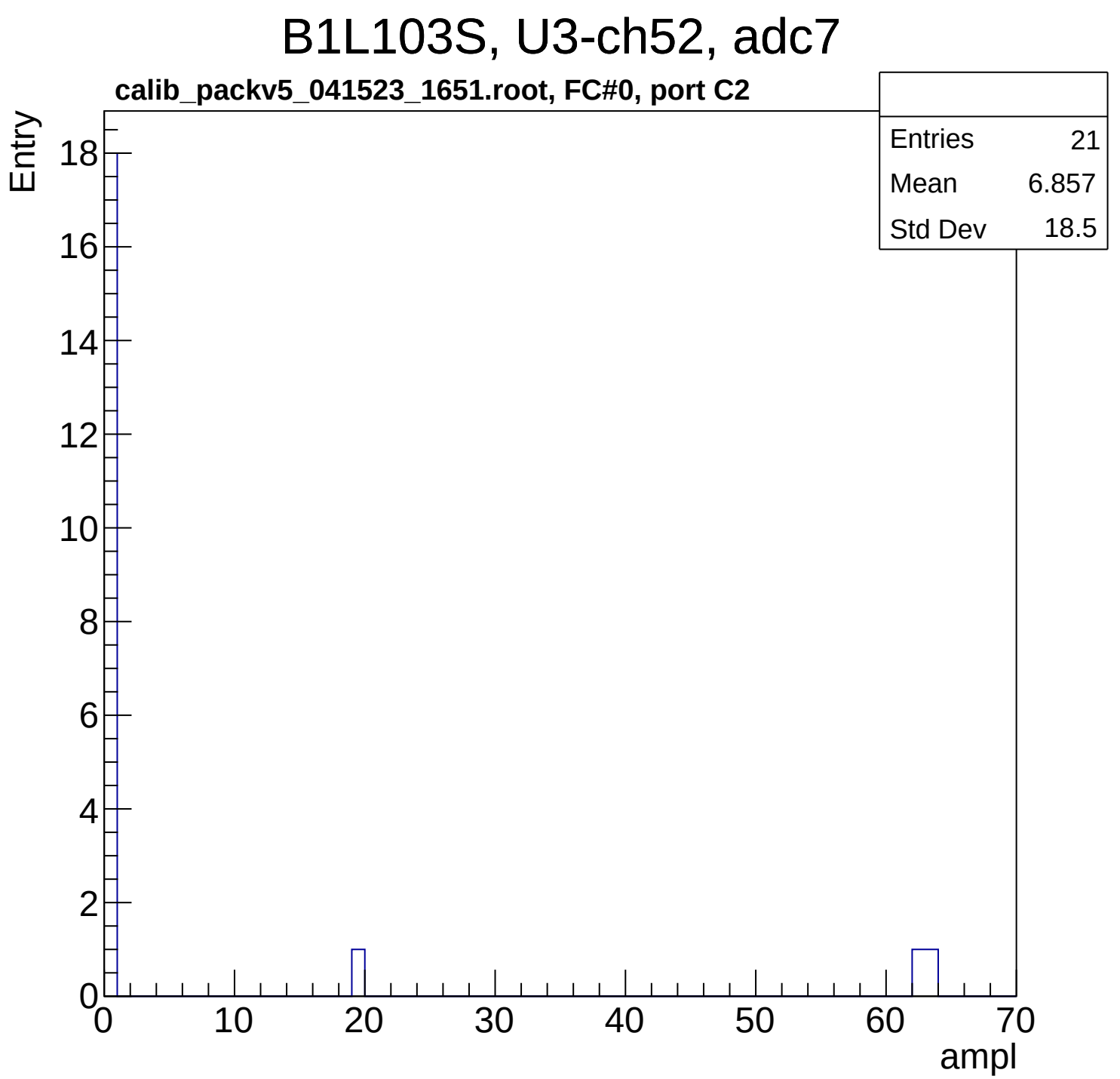
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch52, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 6.857
Std Dev 18.5
Entry
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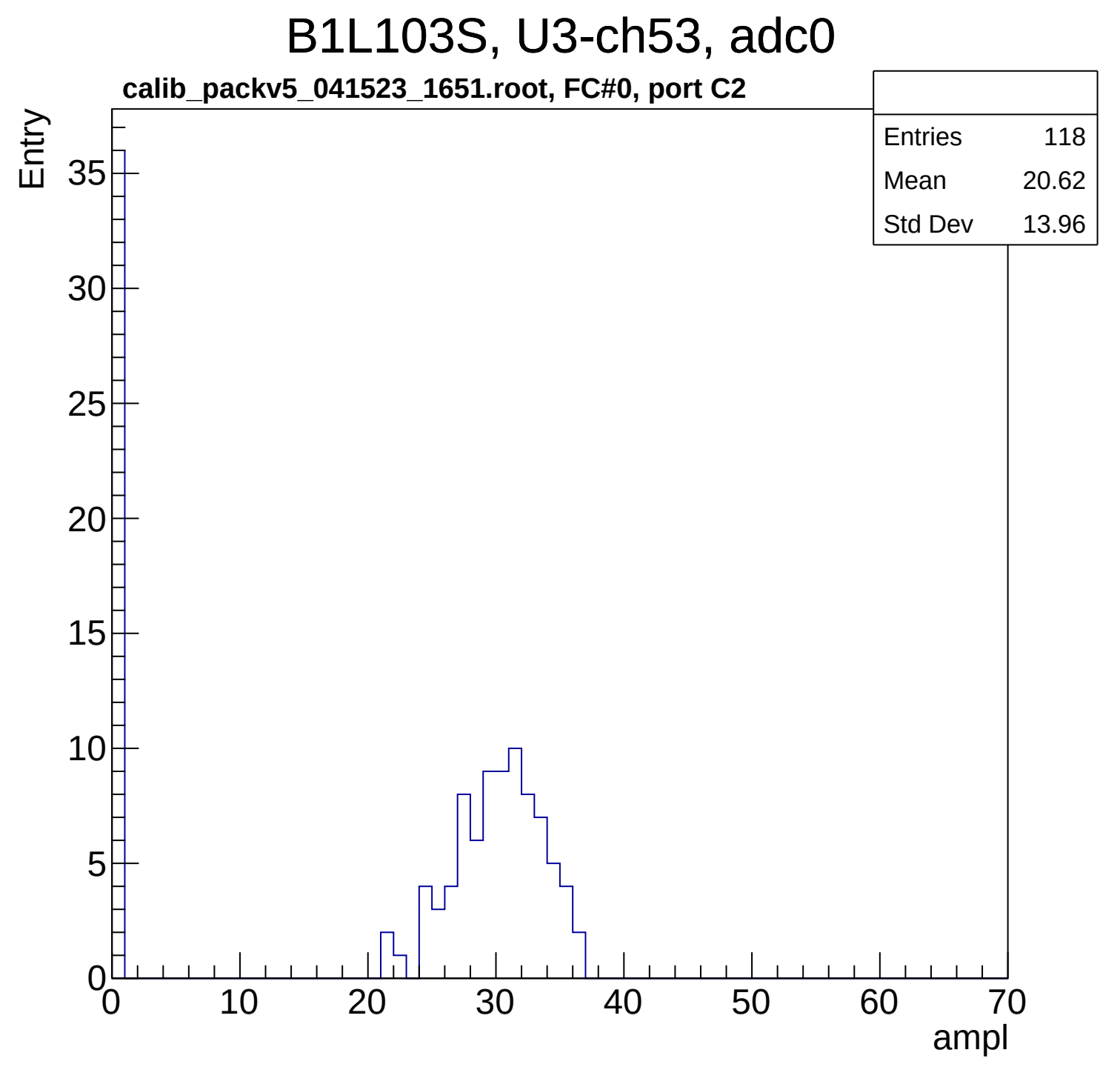
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch53, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 118
Mean 20.62
Std Dev 13.96
Entry
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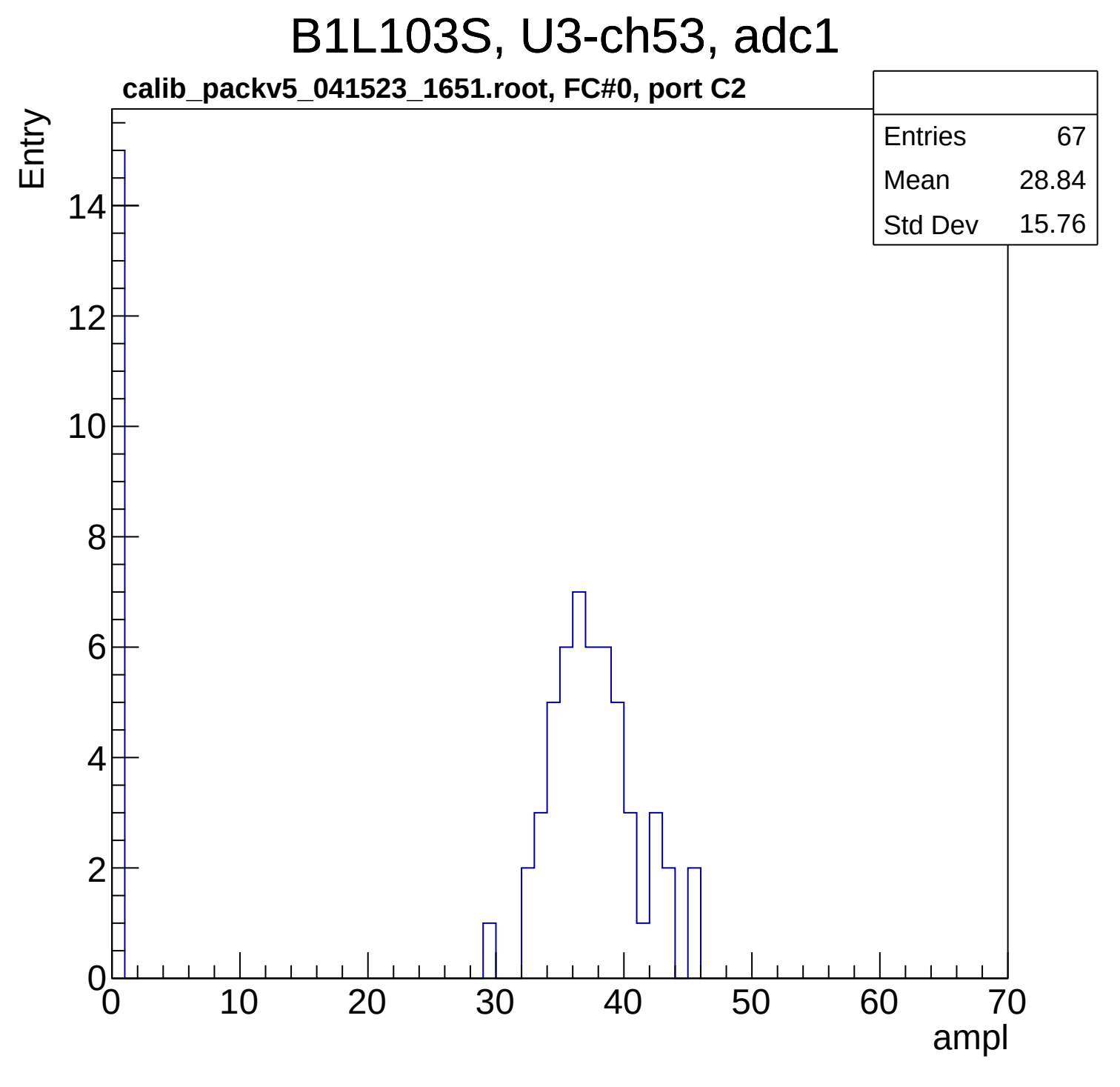
5
10
15
20
25
30
35
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch53, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 28.84
Std Dev 15.76
Entry
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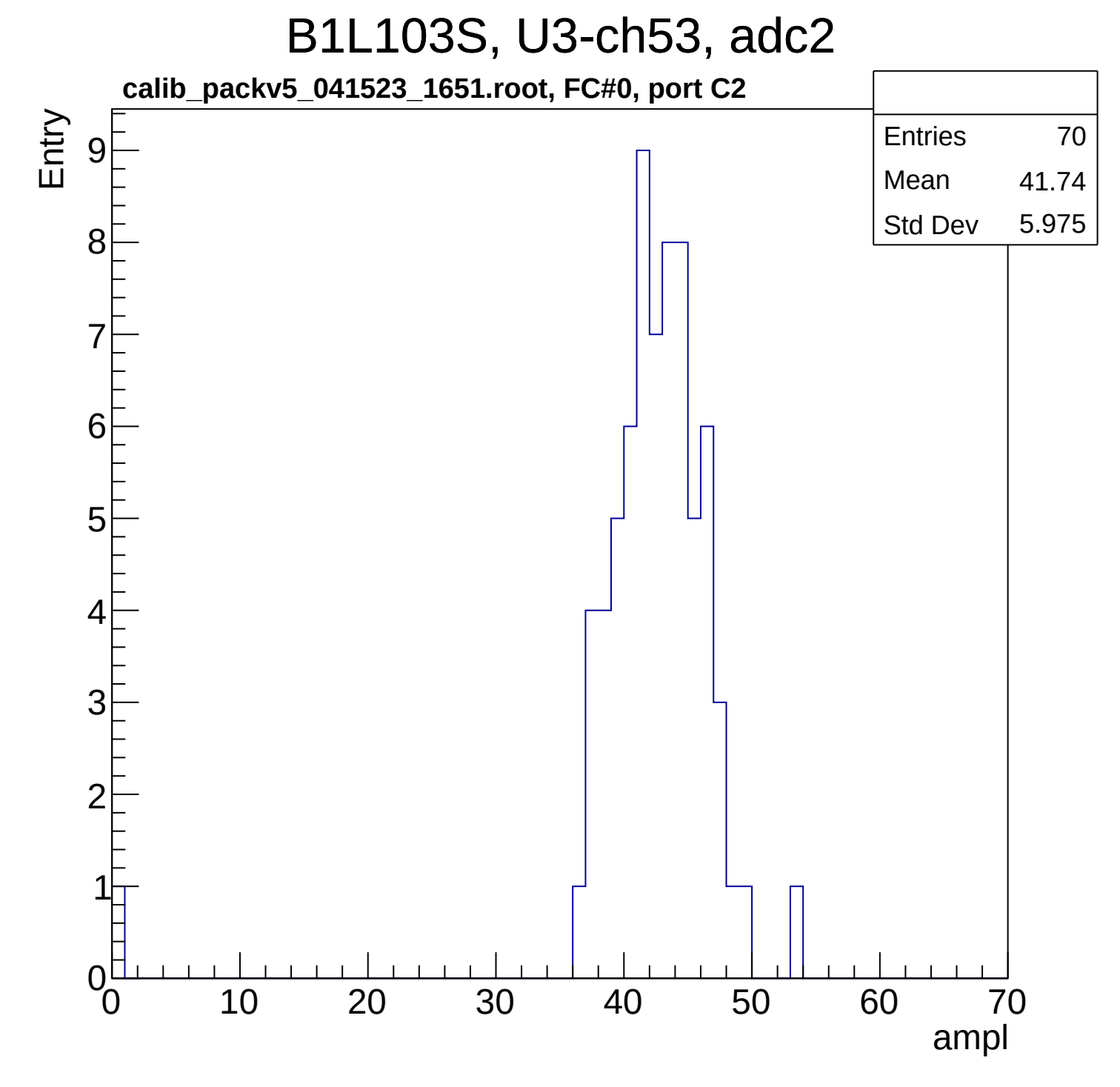
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch53, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 41.74
Std Dev 5.975
Entry
ampl
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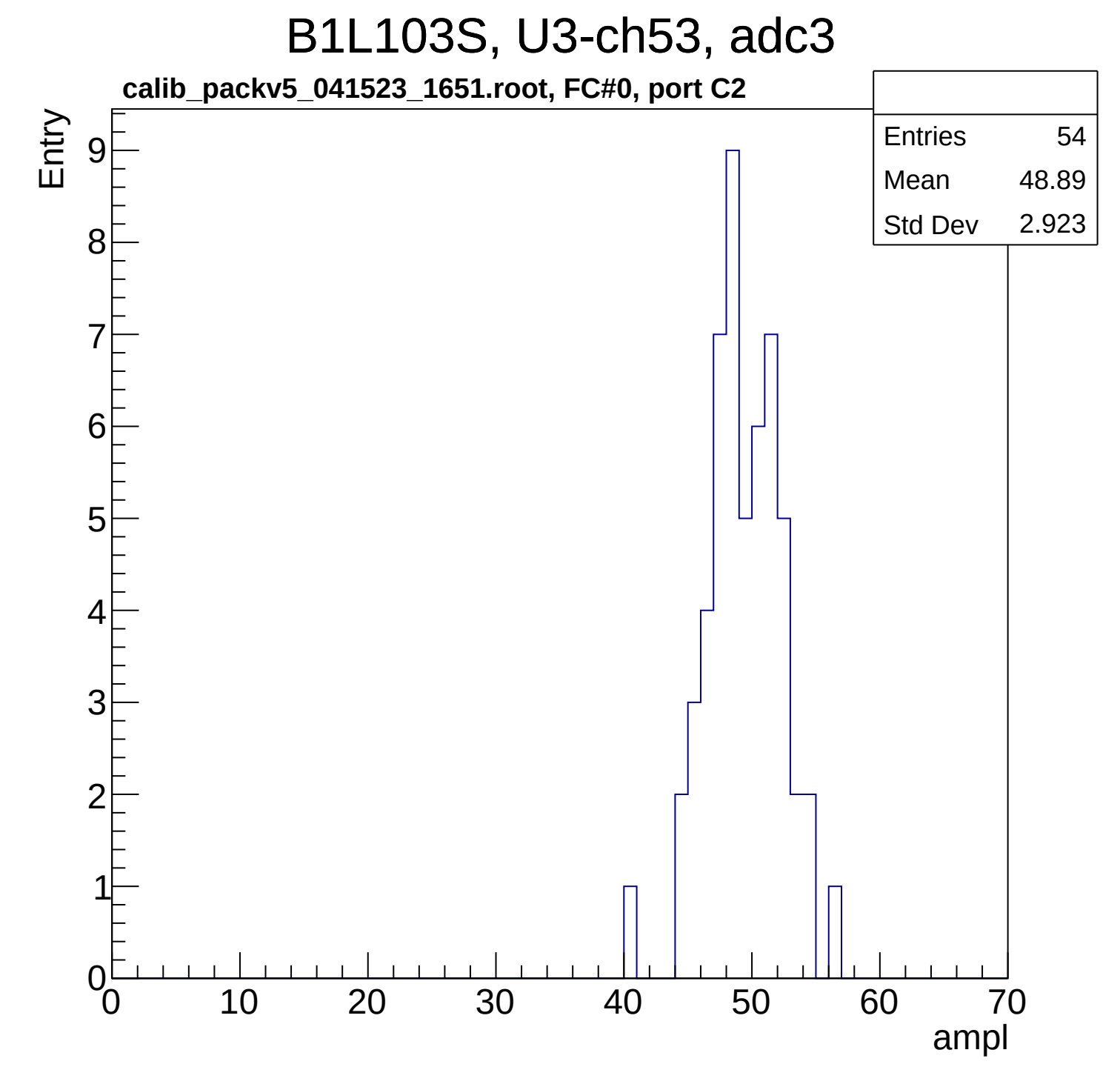
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch53, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 48.89
Std Dev 2.923
Entry
ampl
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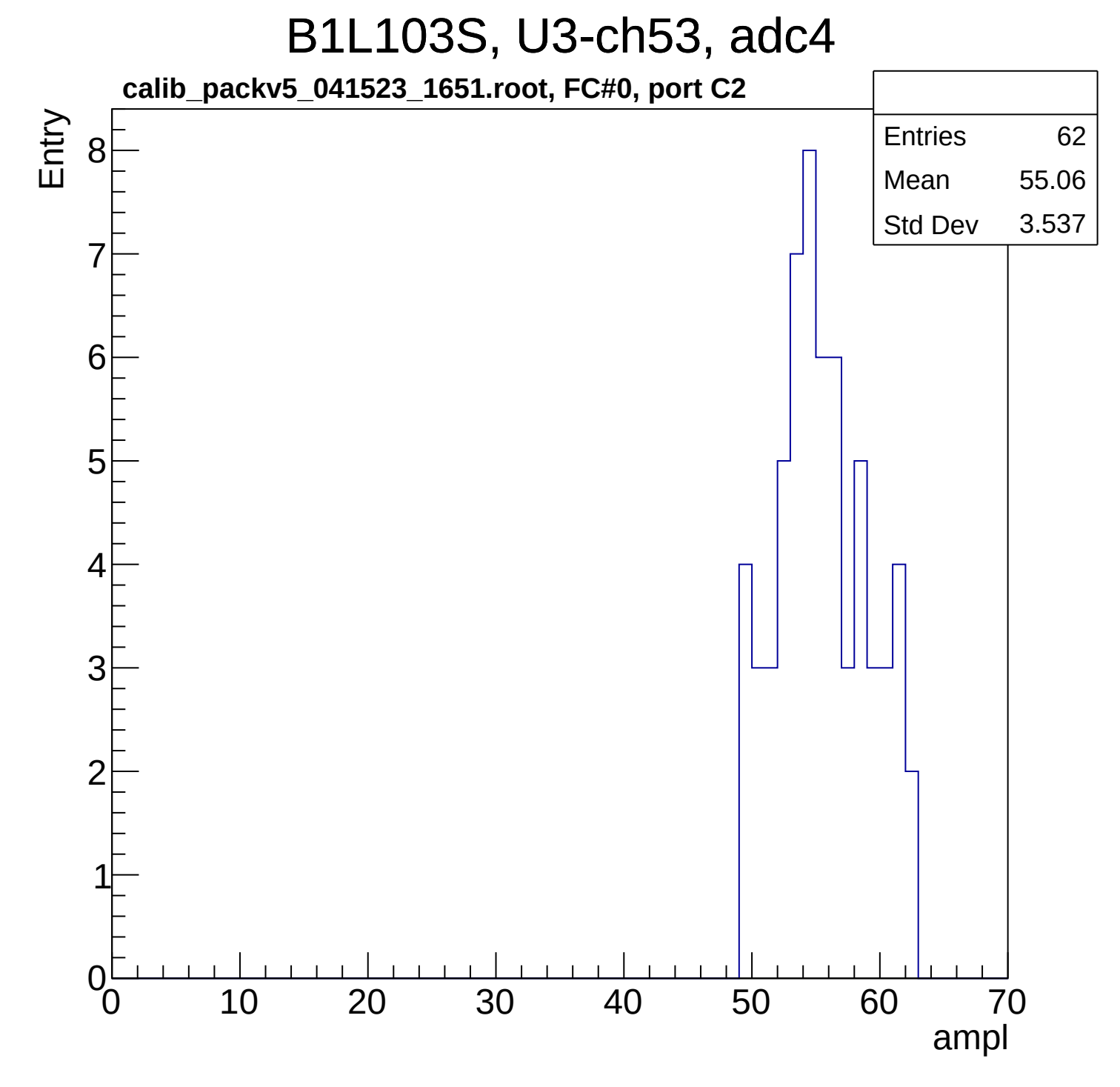
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch53, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 55.06
Std Dev 3.537
Entry
ampl
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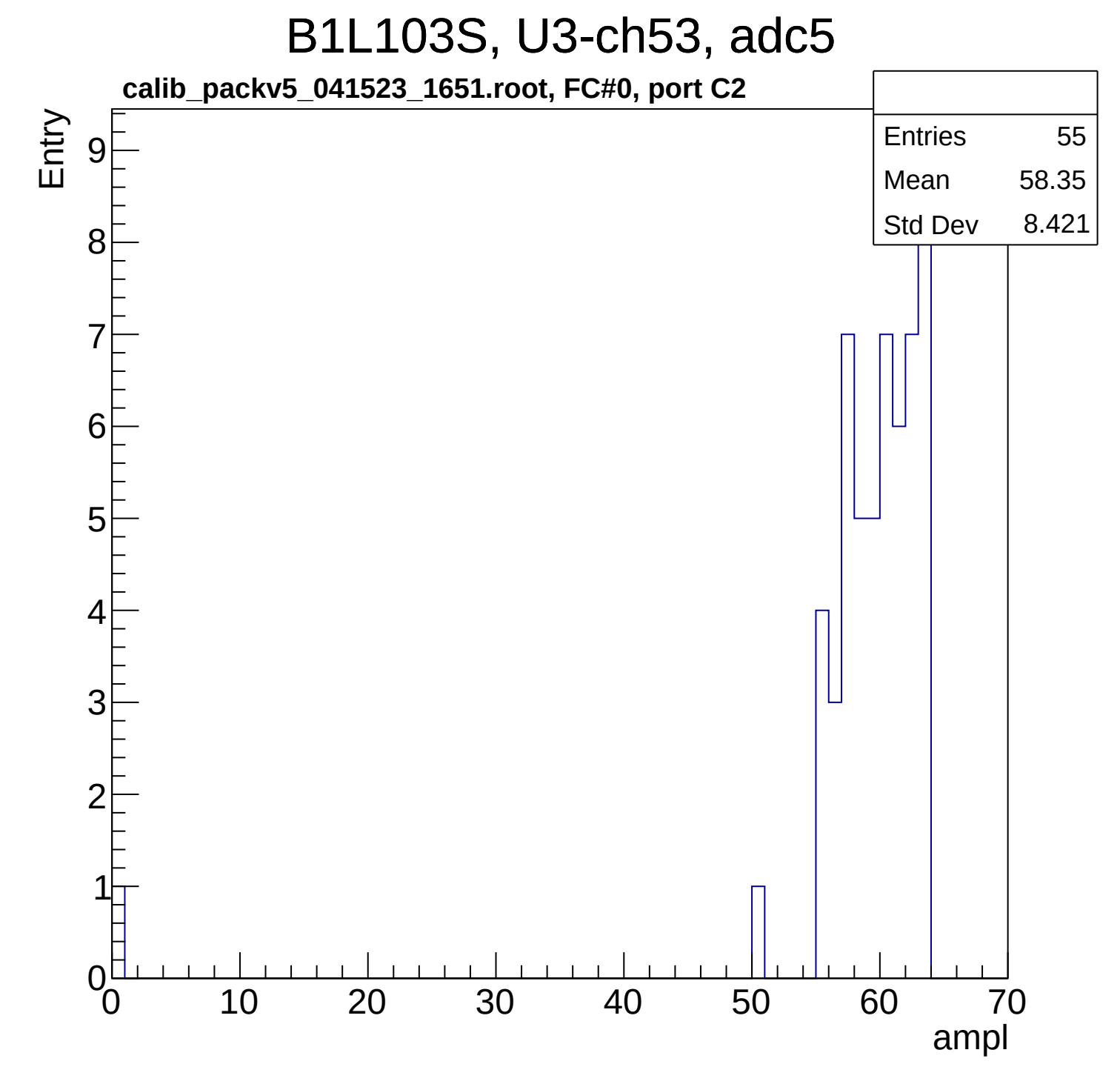
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch53, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 58.35
Std Dev 8.421
Entry
ampl
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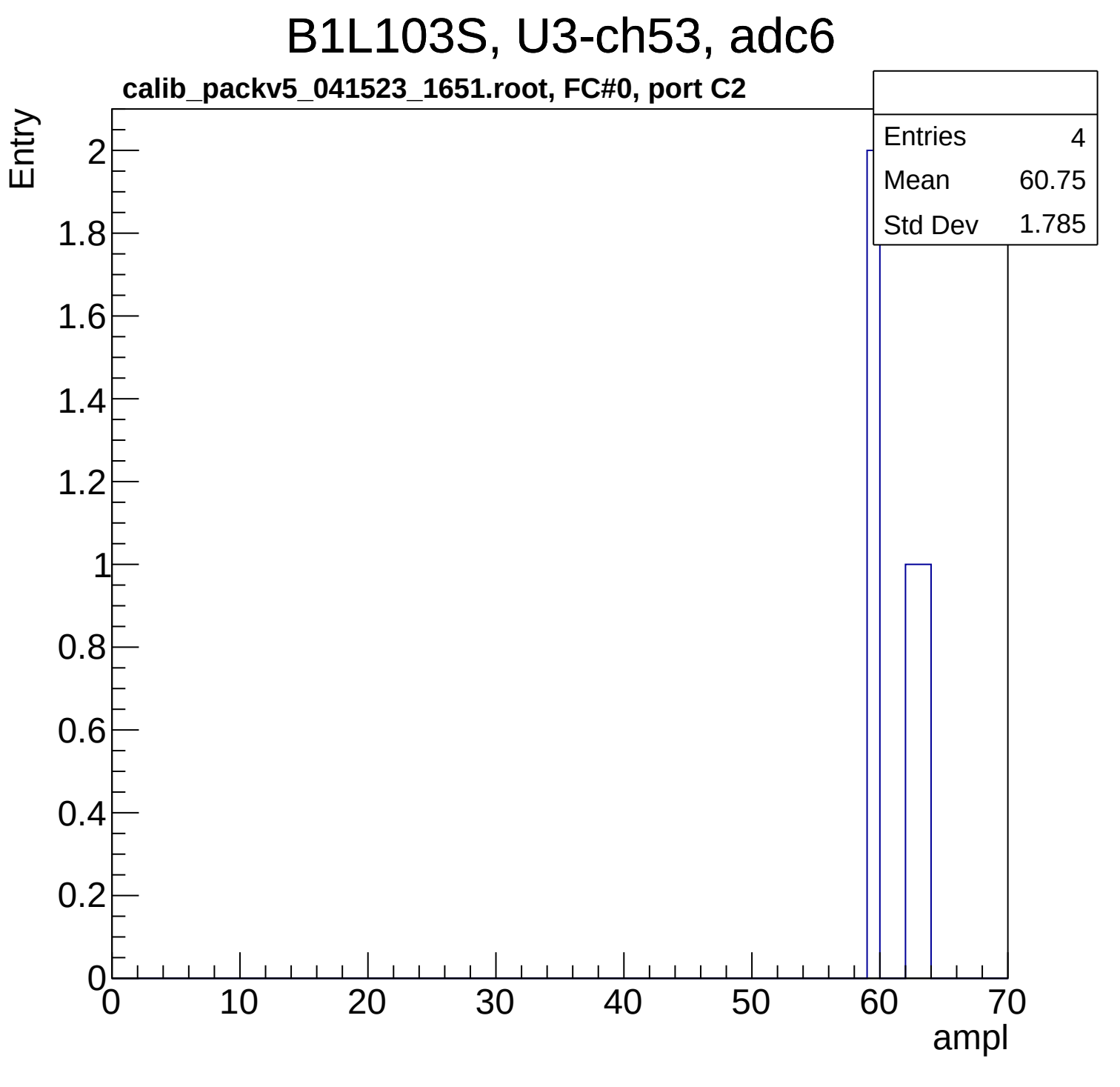
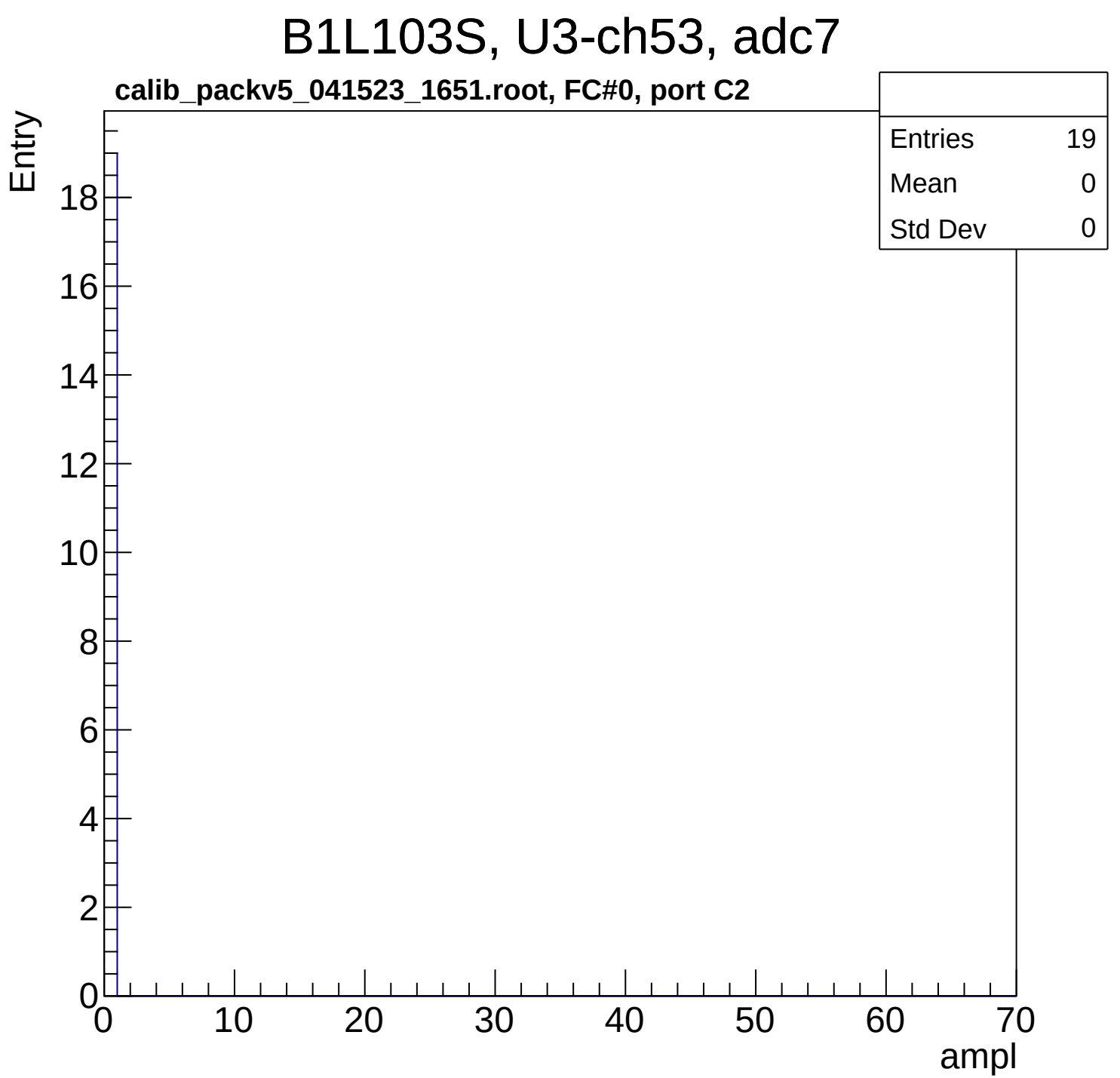
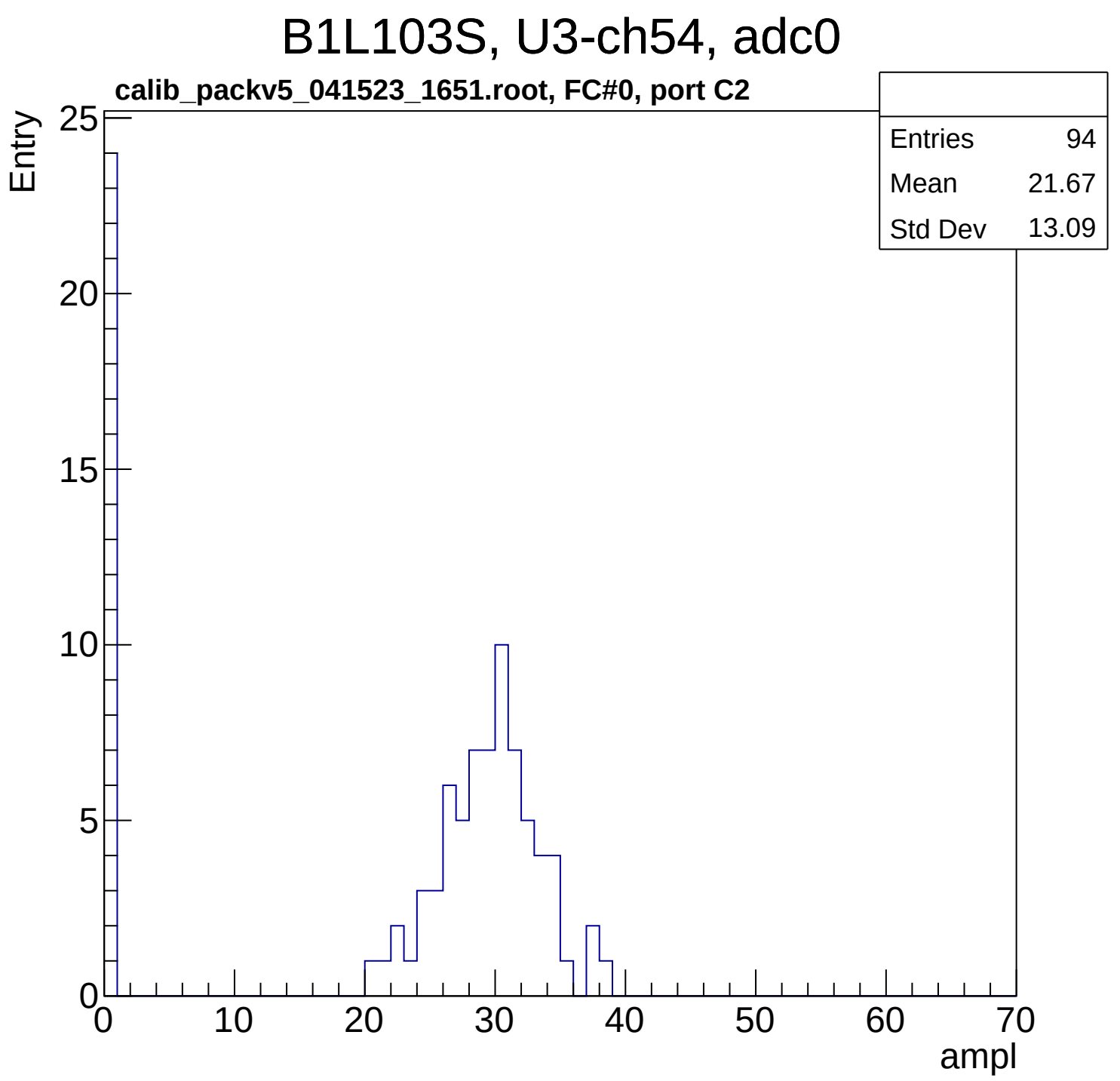
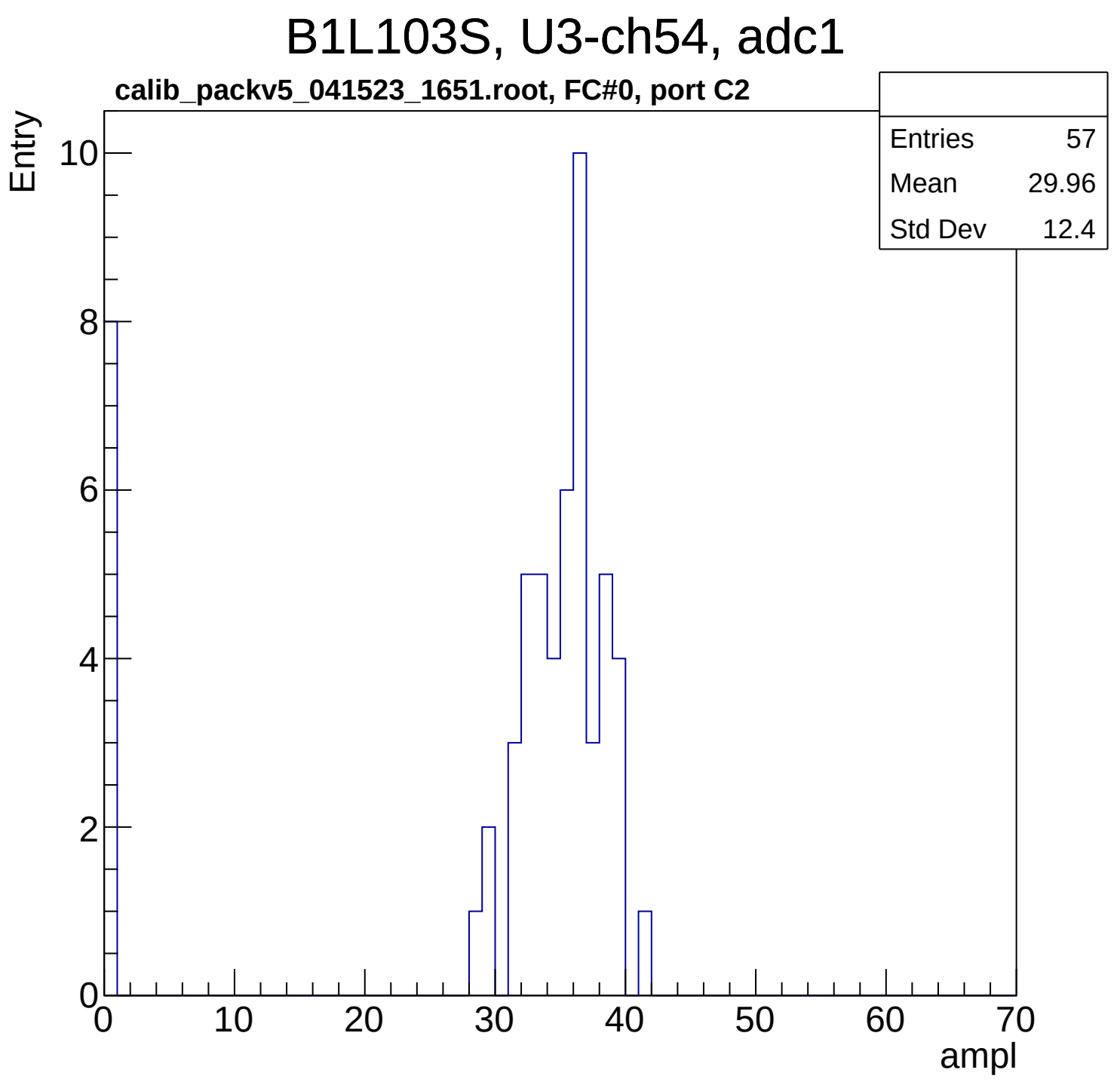
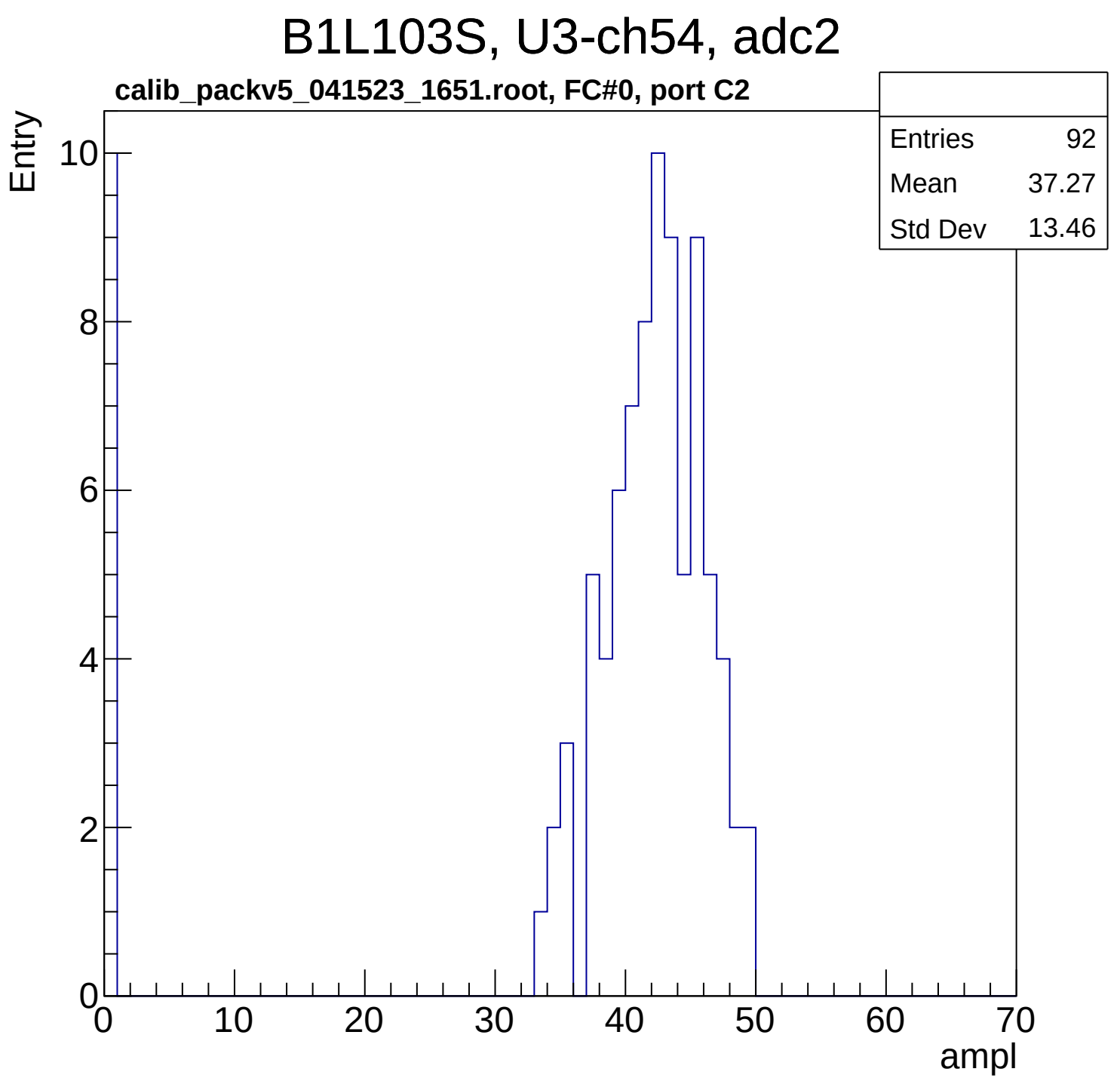
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch53, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 60.75
Std Dev 1.785
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U3-ch53, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch54, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 21.67
Std Dev 13.09
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch54, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 29.96
Std Dev 12.4
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch54, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 37.27
Std Dev 13.46
Entry
0
2
4
6
8
10
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10
20
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50
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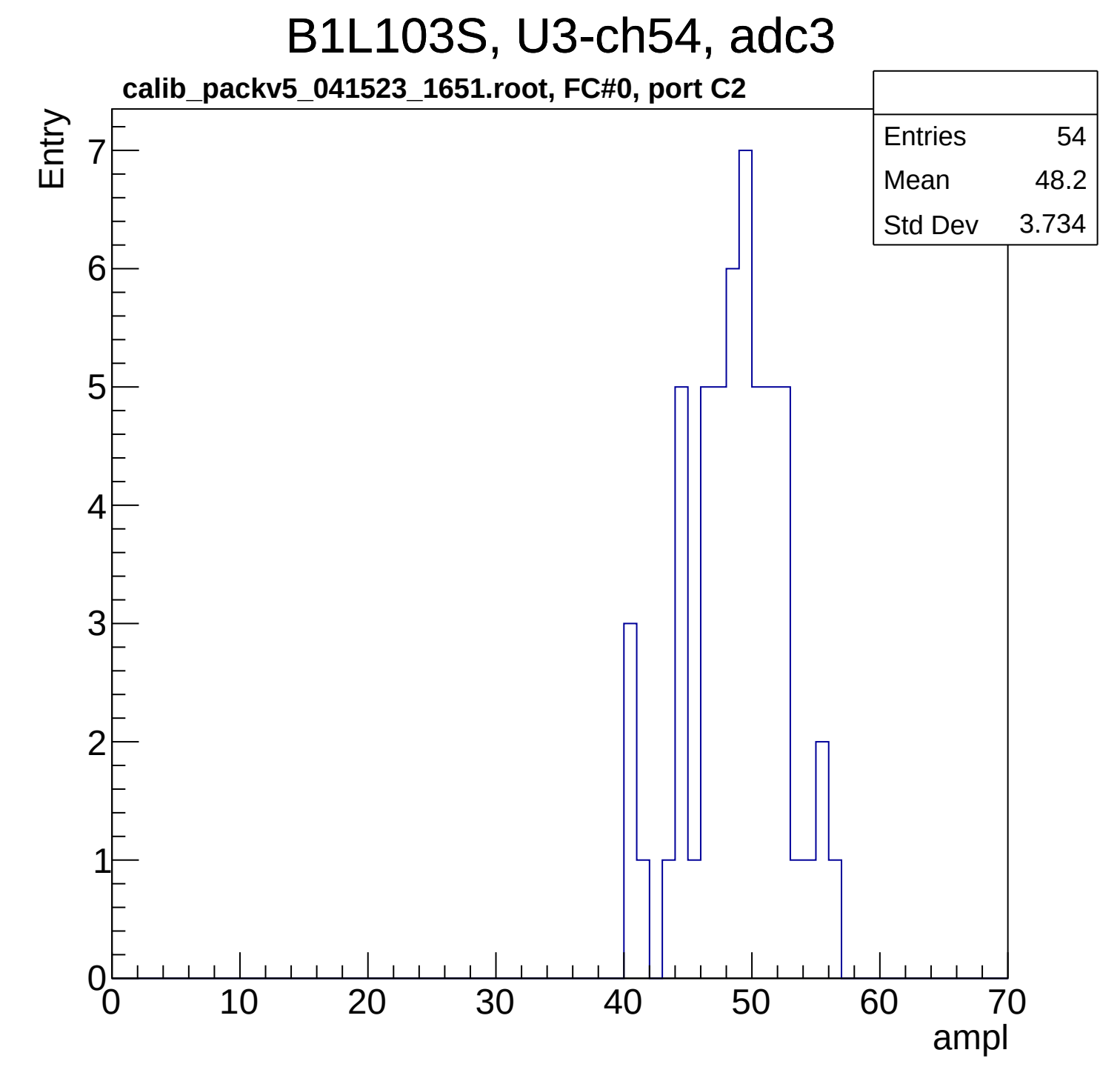
70
ampl


B1L103S, U3-ch54, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 48.2
Std Dev 3.734
Entry
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5
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7
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10
20
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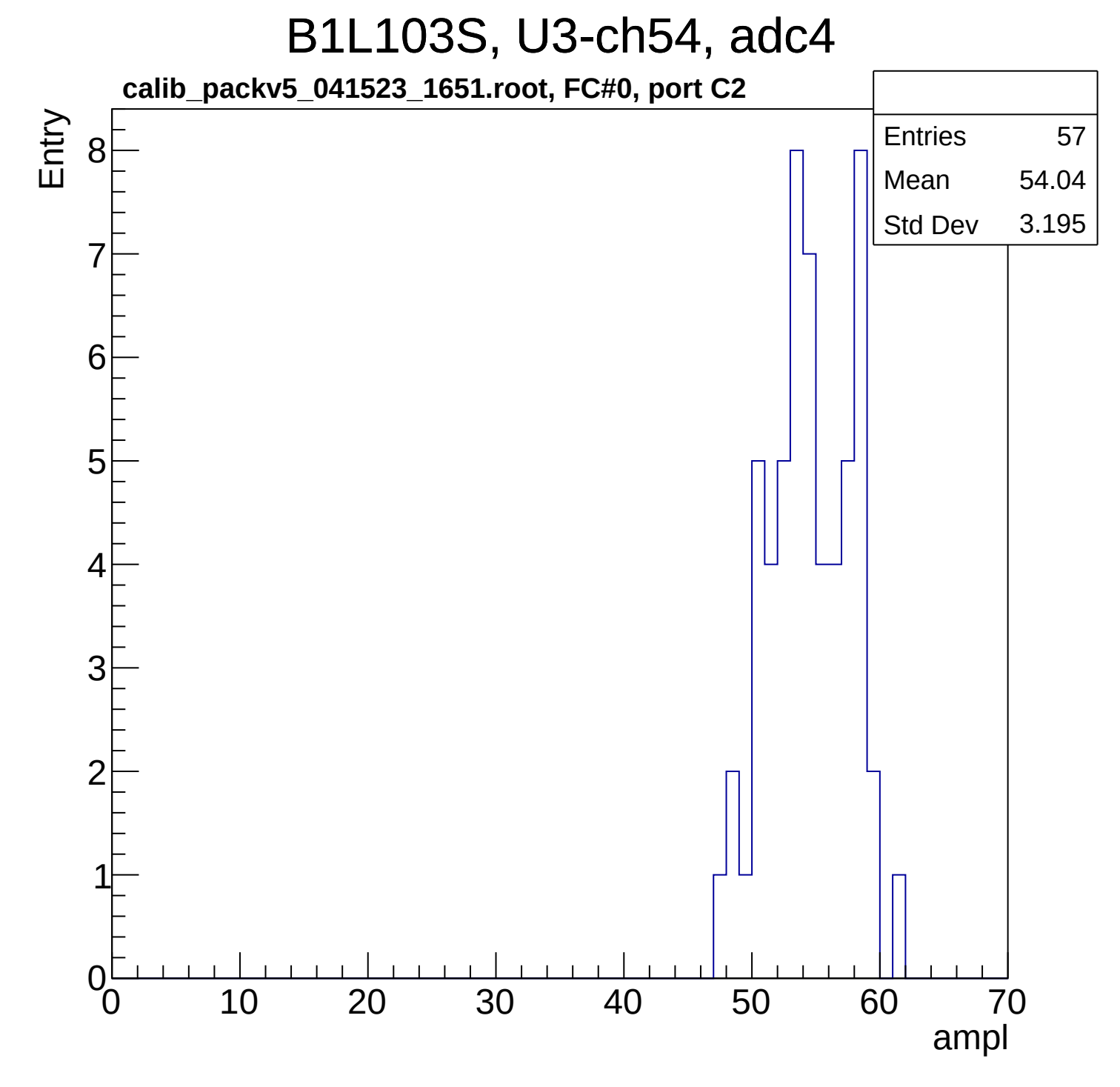
50
60
70
ampl


B1L103S, U3-ch54, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 54.04
Std Dev 3.195
Entry
ampl
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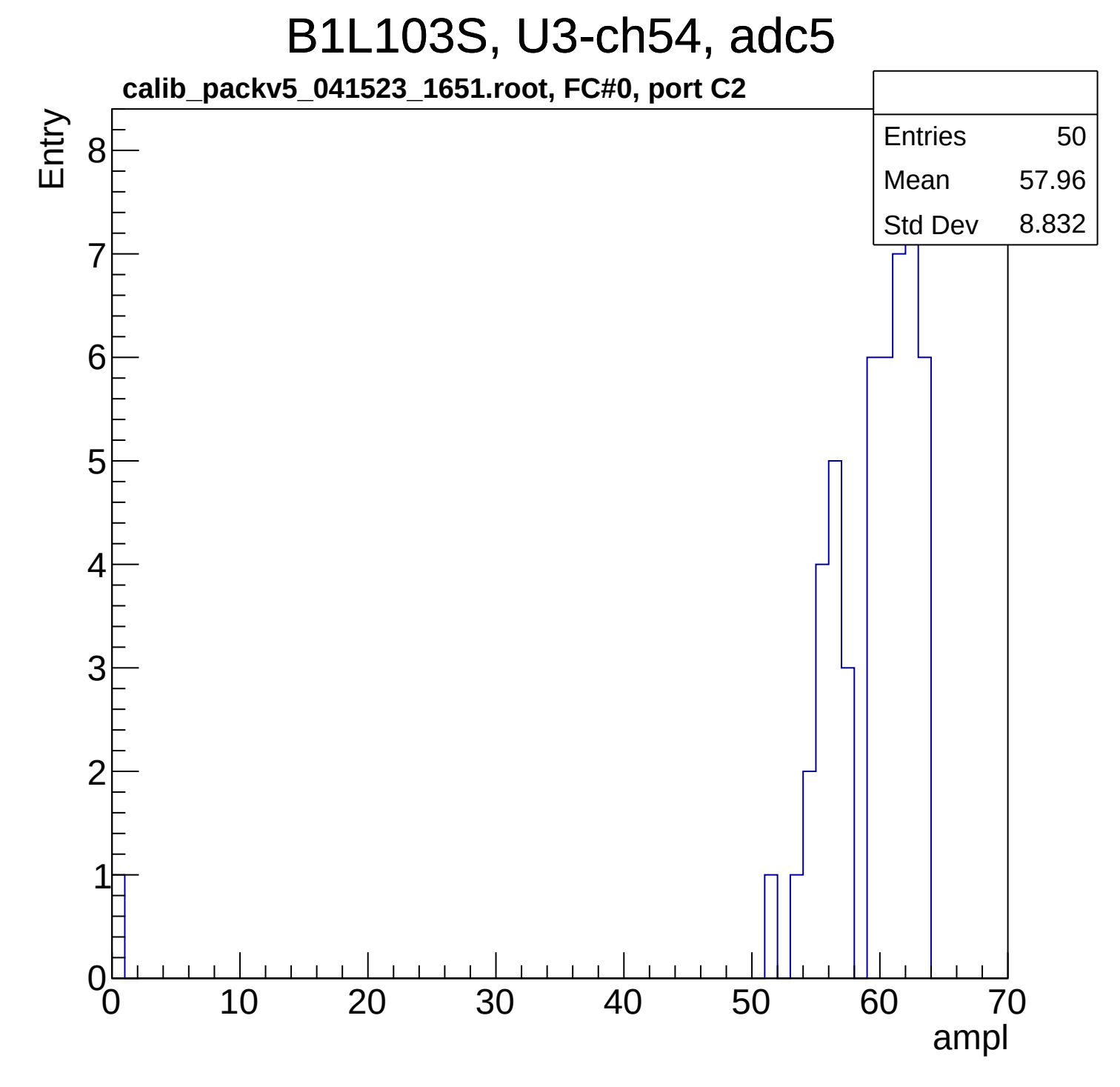
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch54, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 57.96
Std Dev 8.832
Entry
ampl
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1
2
3
4
5
6
7
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0
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40
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60
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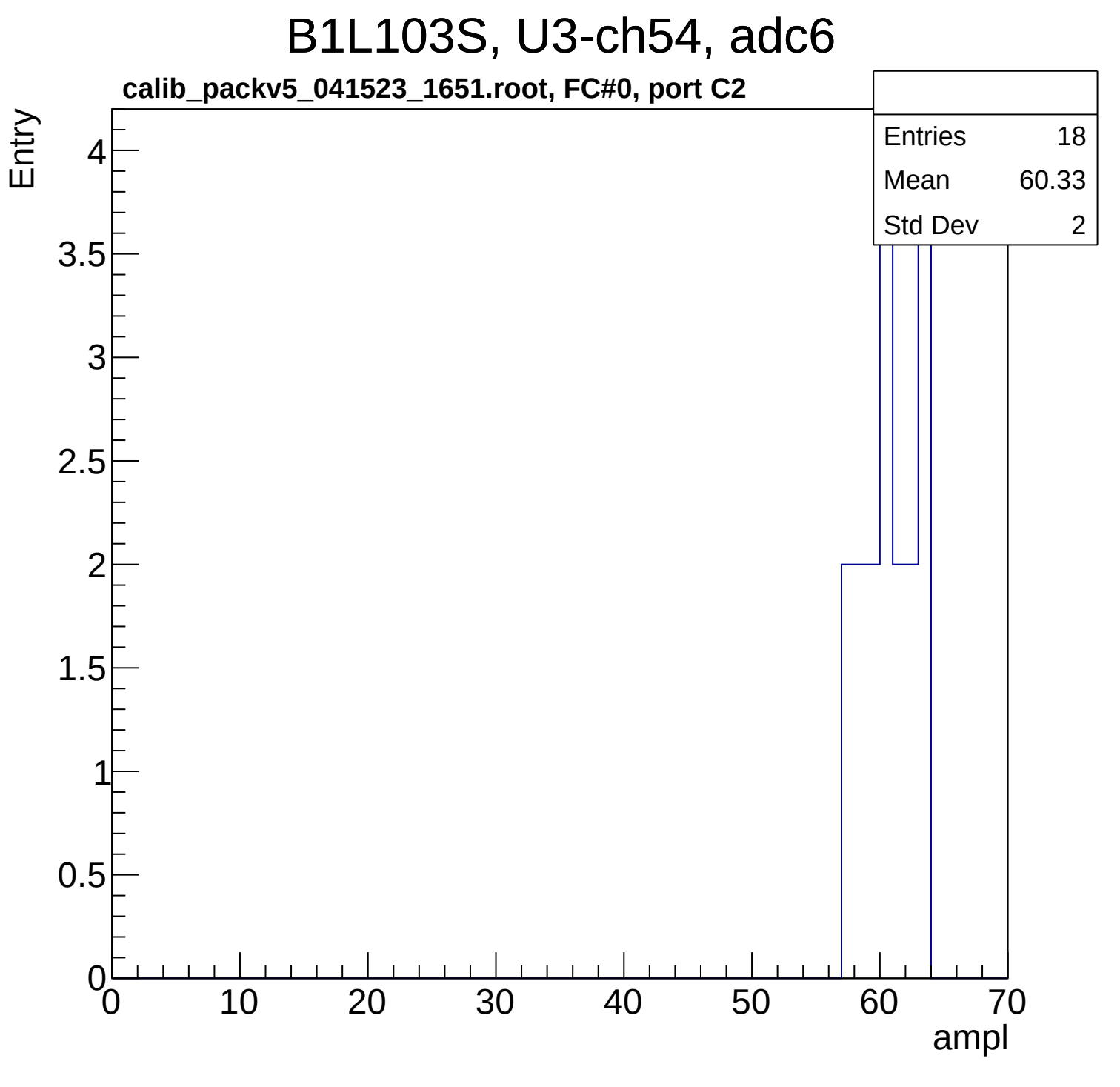
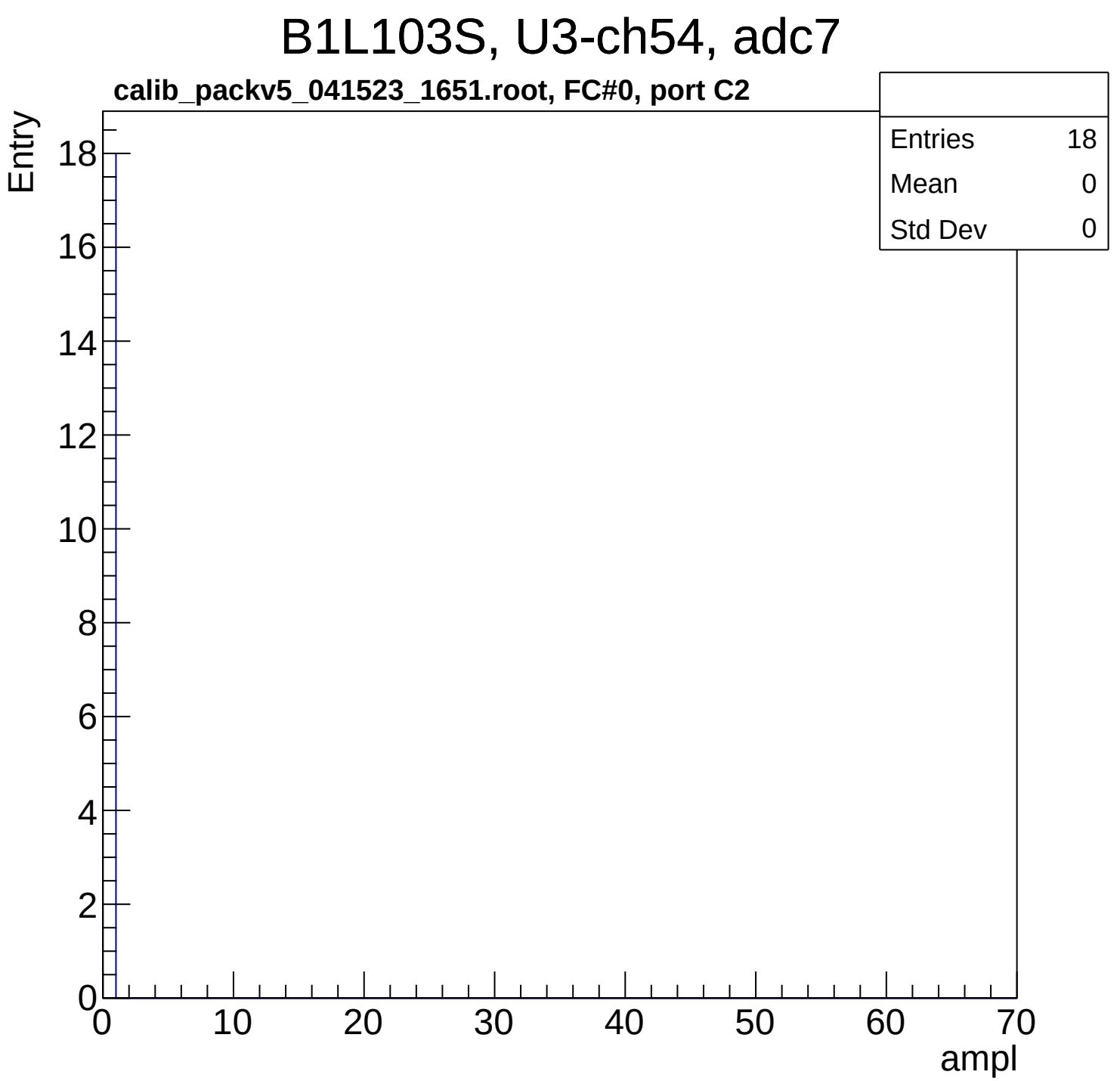
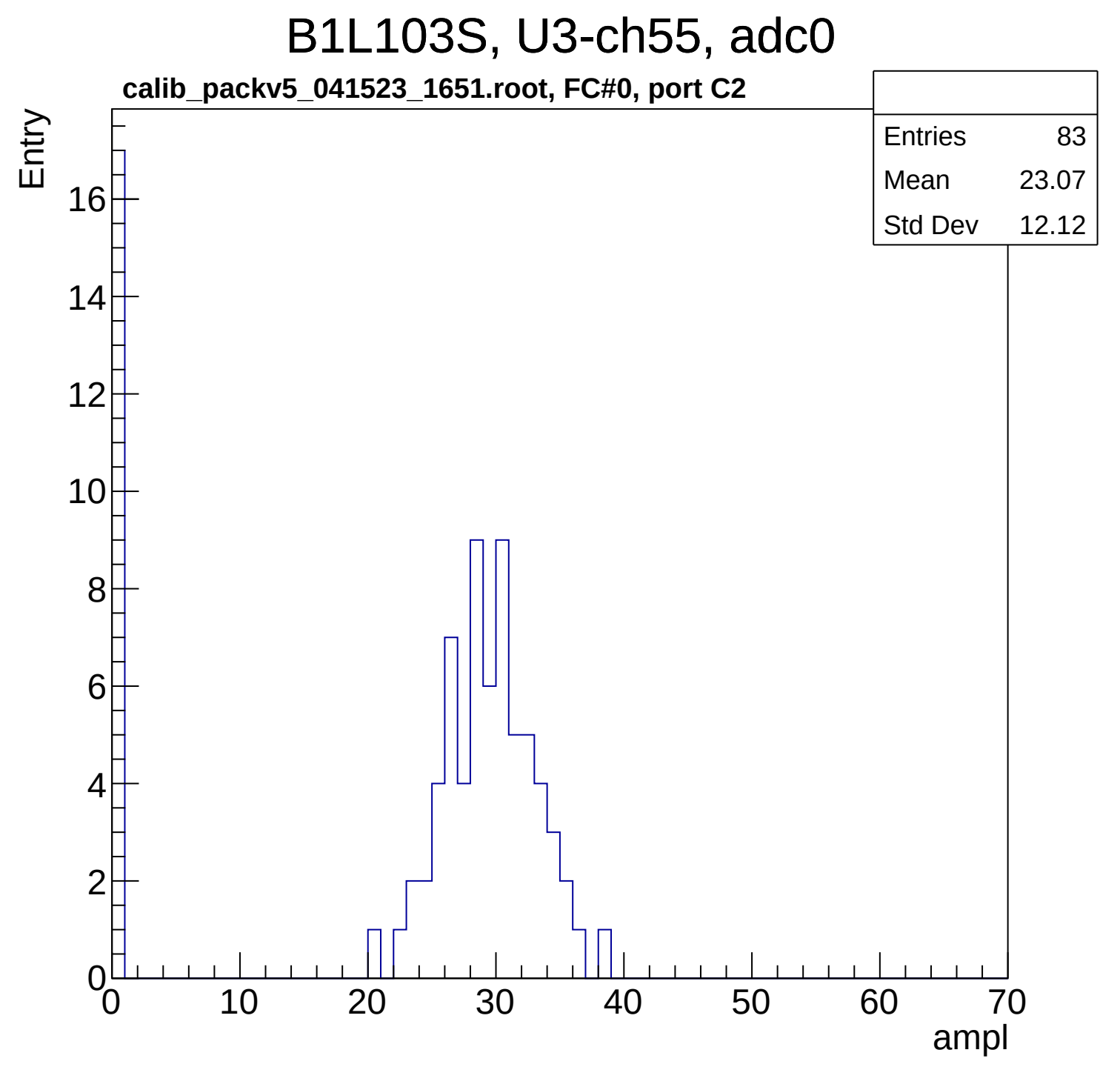

B1L103S, U3-ch54, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 60.33
Std Dev 2
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U3-ch54, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch55, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 23.07
Std Dev 12.12
Entry
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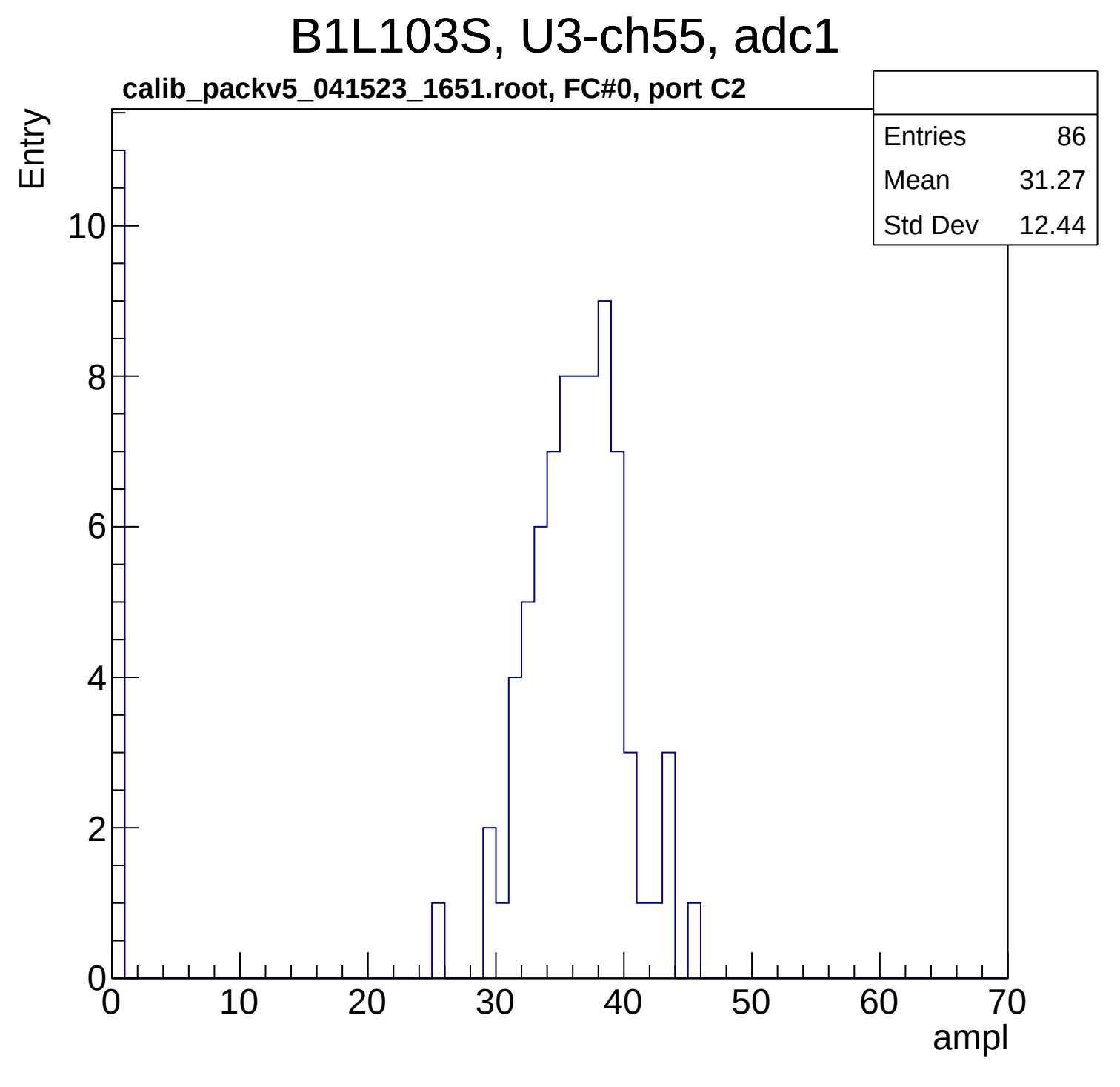
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch55, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 31.27
Std Dev 12.44
Entry
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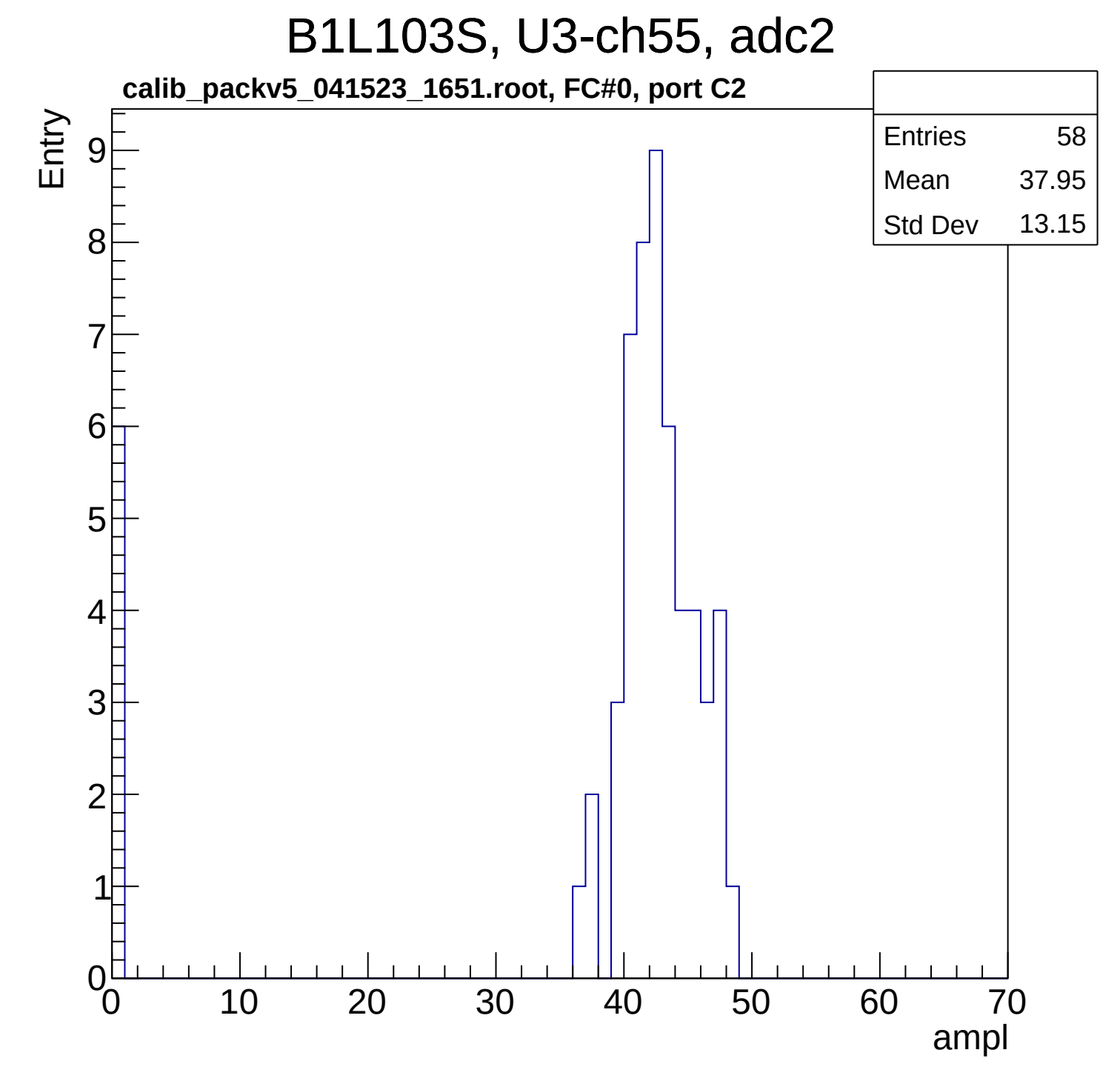
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch55, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 37.95
Std Dev 13.15
Entry
ampl
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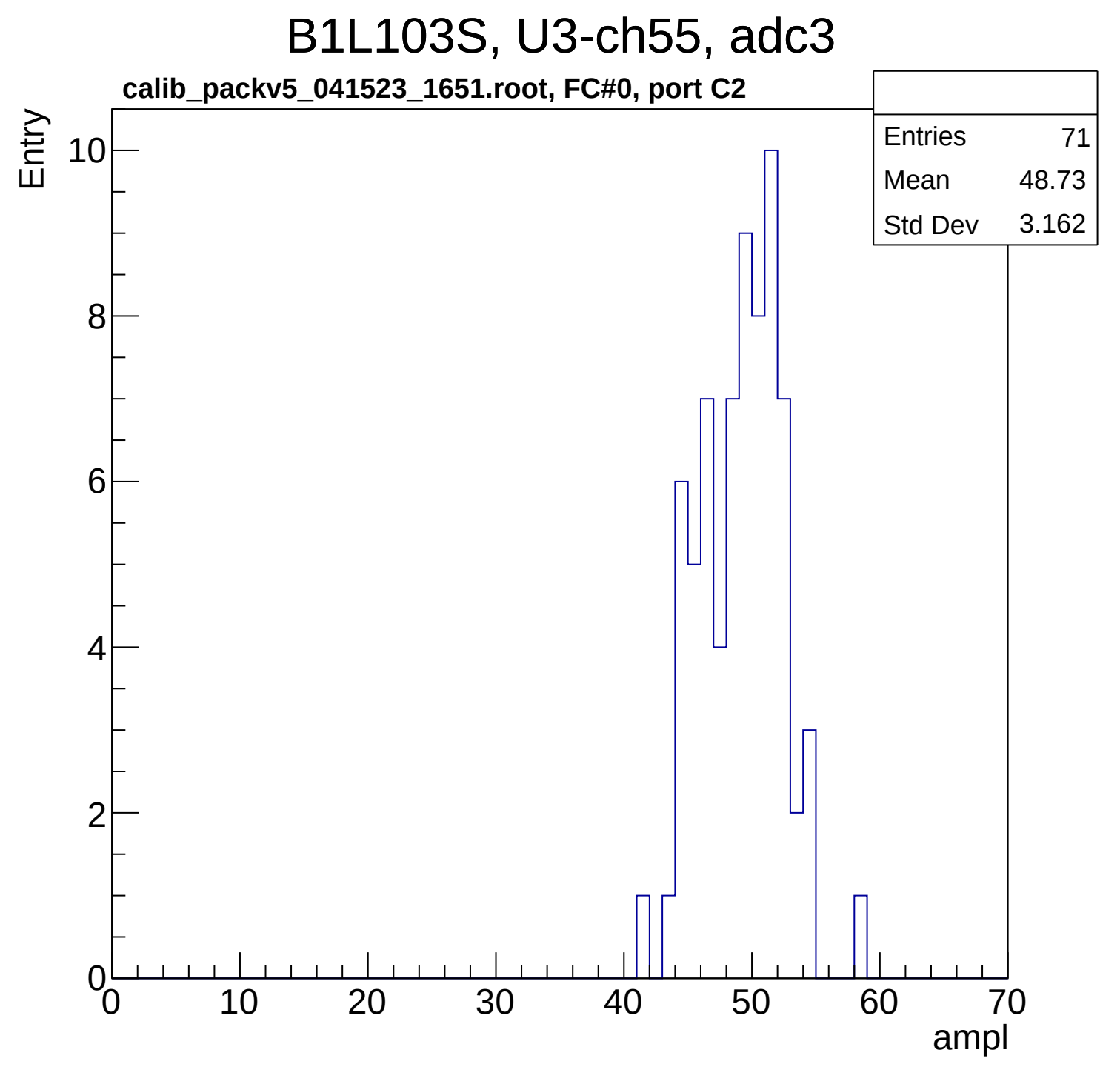
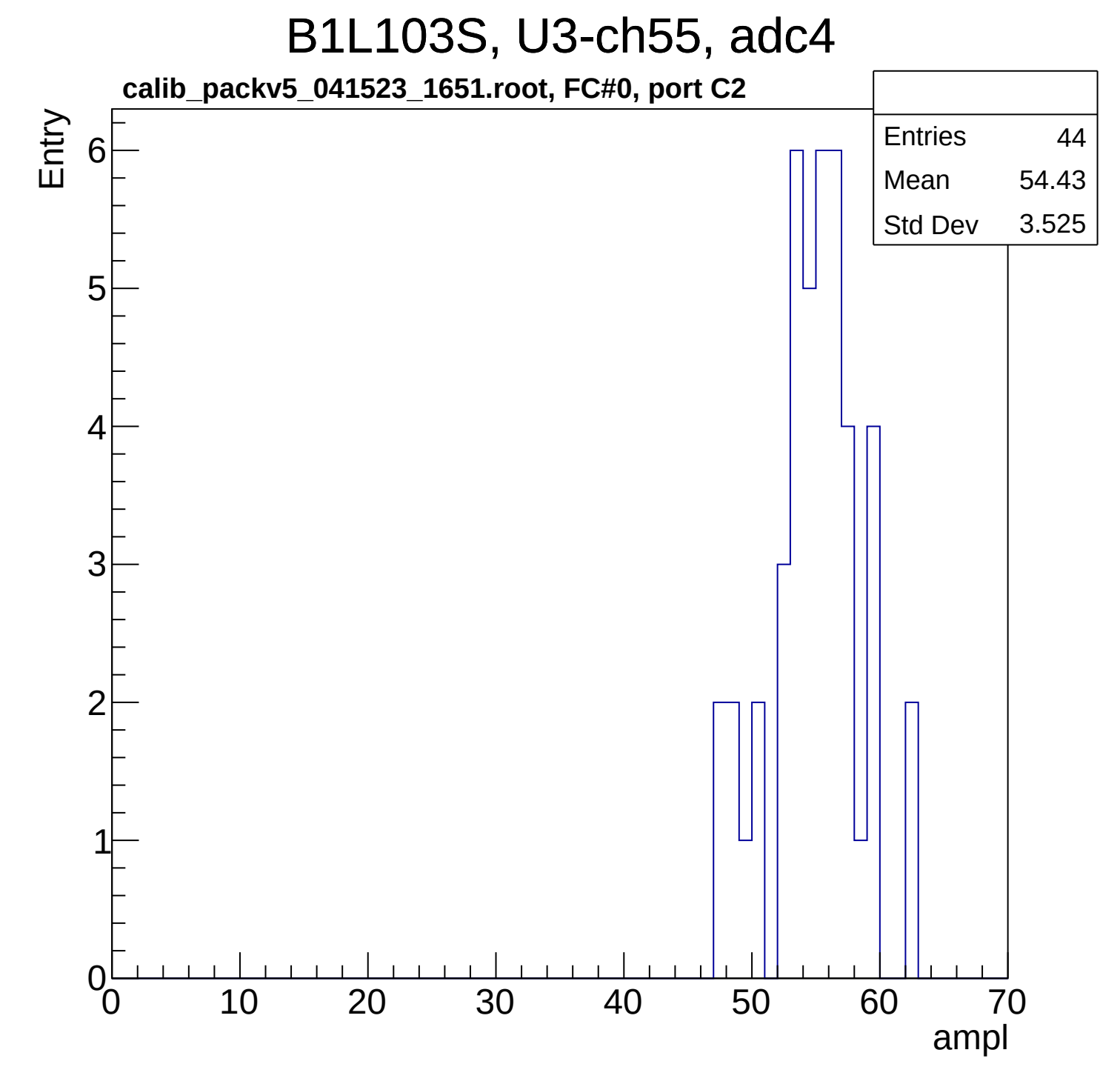
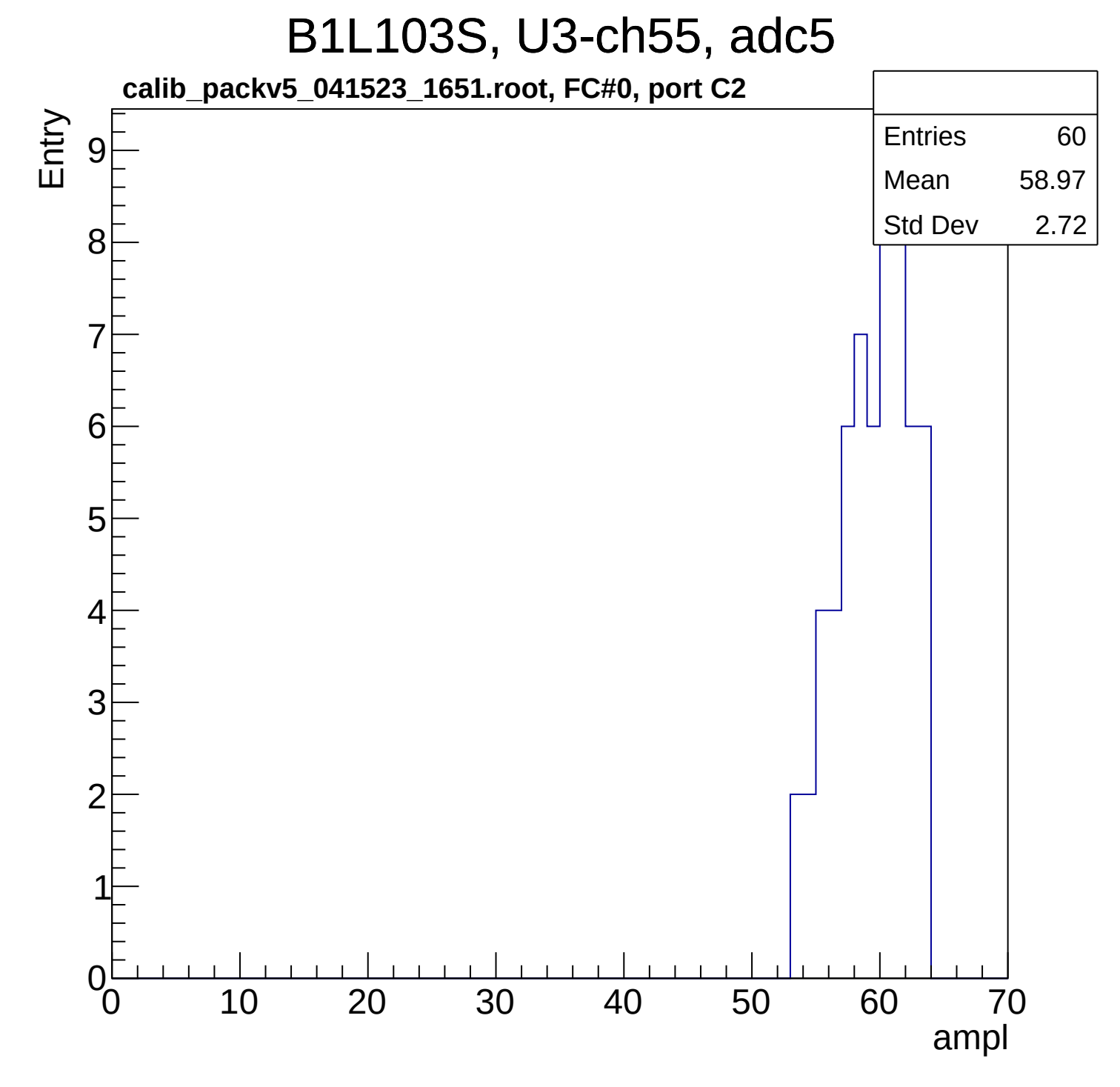
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch55, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 48.73
Std Dev 3.162
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U3-ch55, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 54.43
Std Dev 3.525
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U3-ch55, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 58.97
Std Dev 2.72
Entry
ampl
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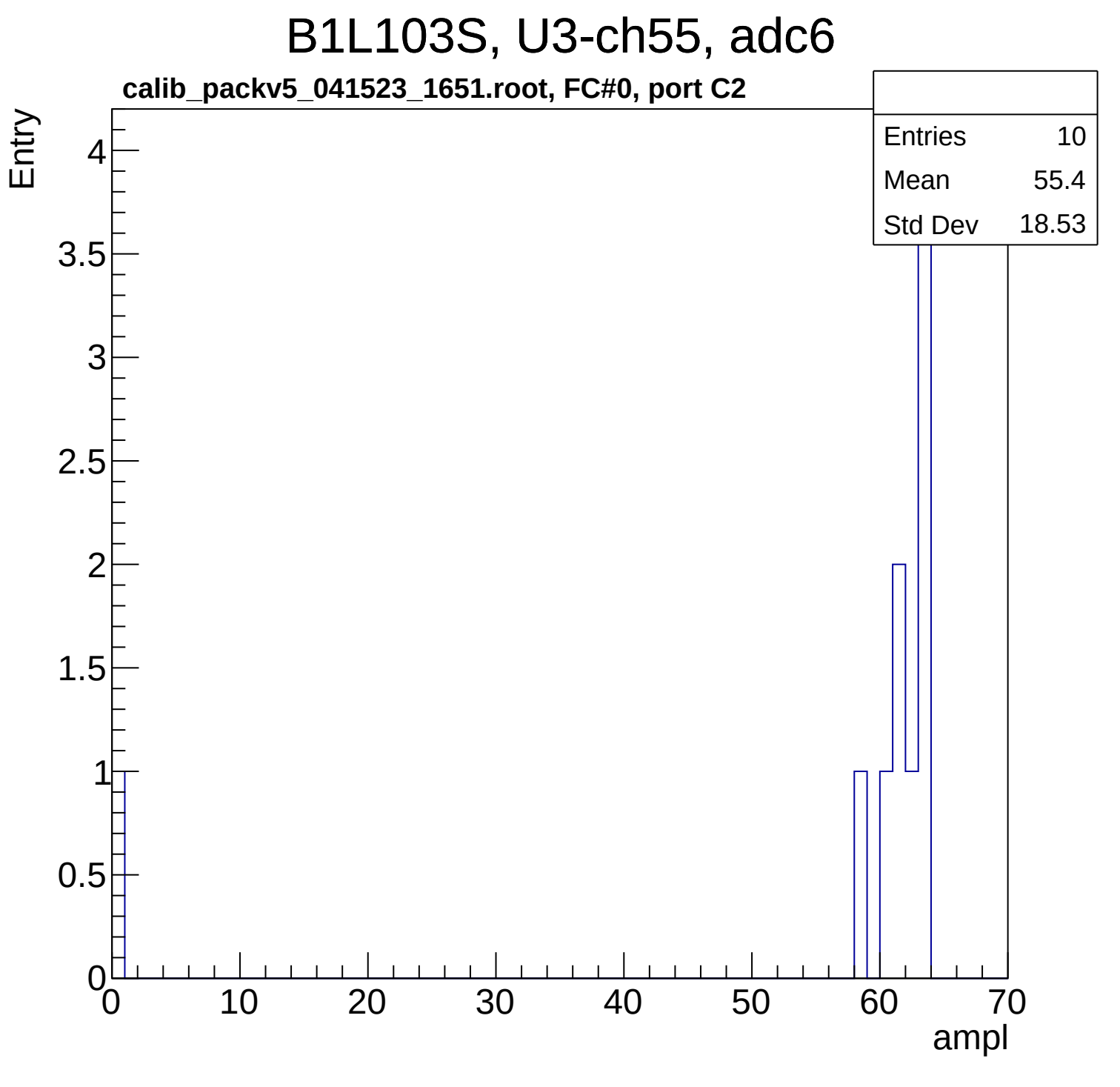
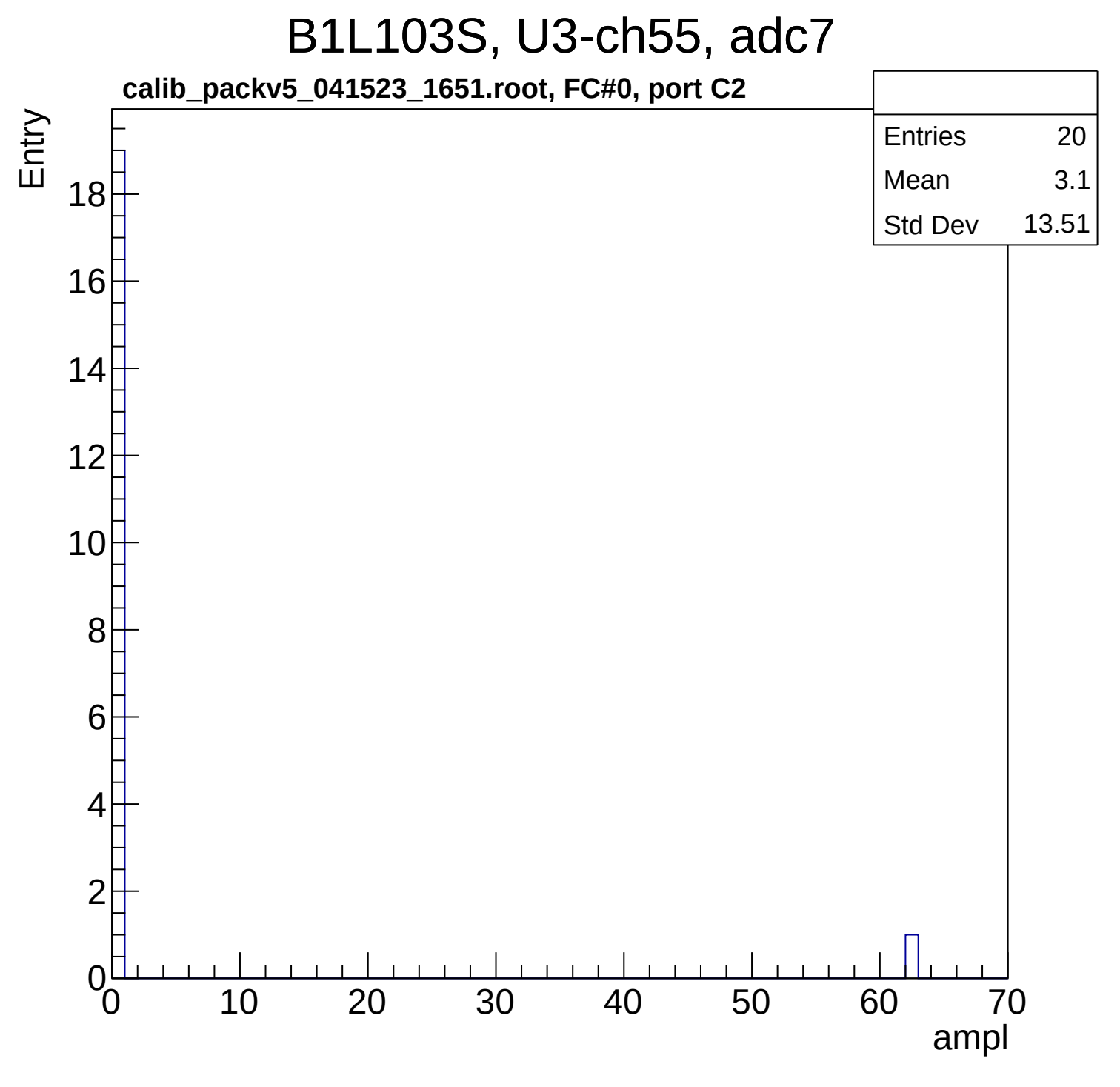
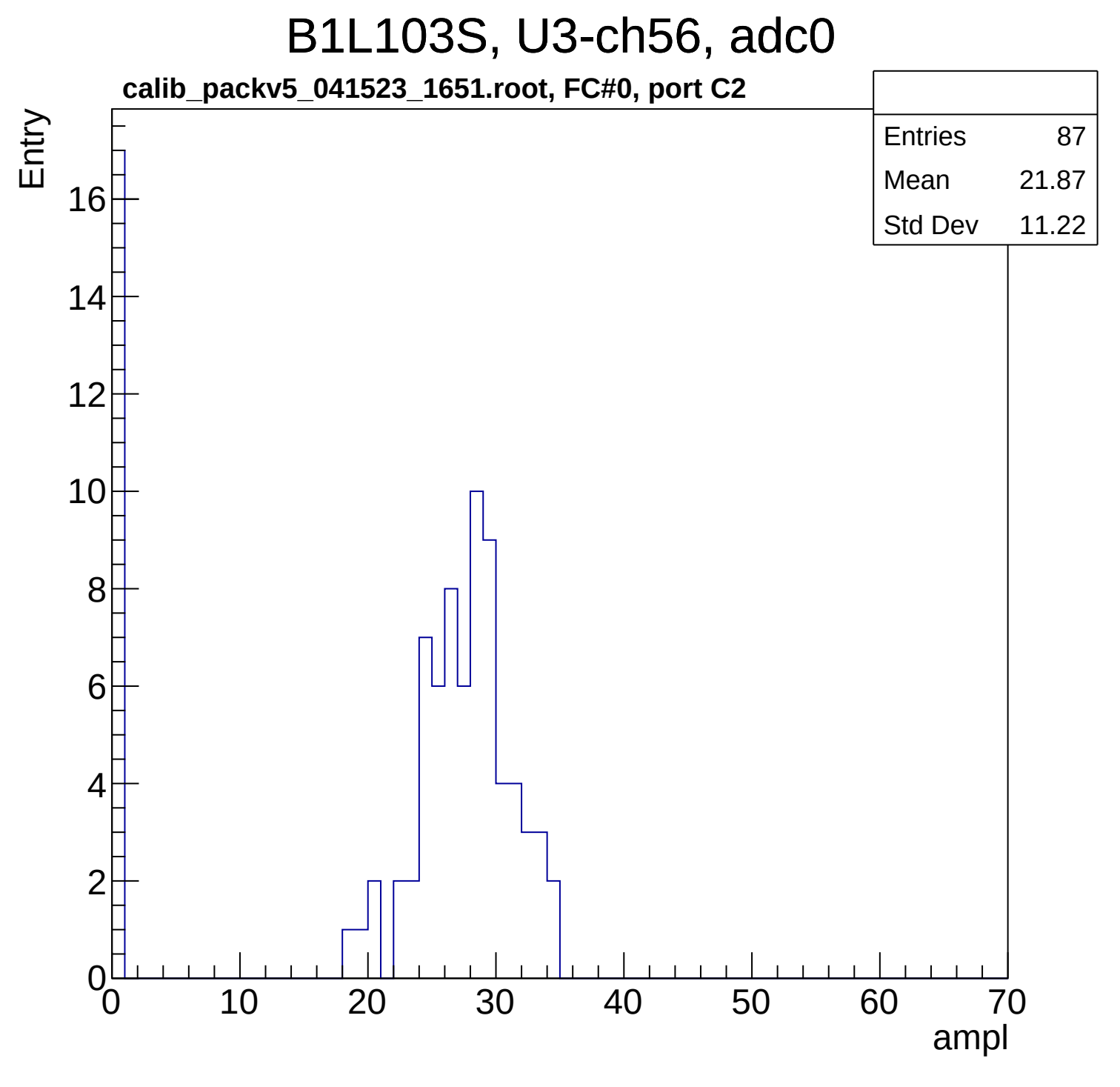
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch55, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 55.4
Std Dev 18.53
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U3-ch55, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch56, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 21.87
Std Dev 11.22
Entry
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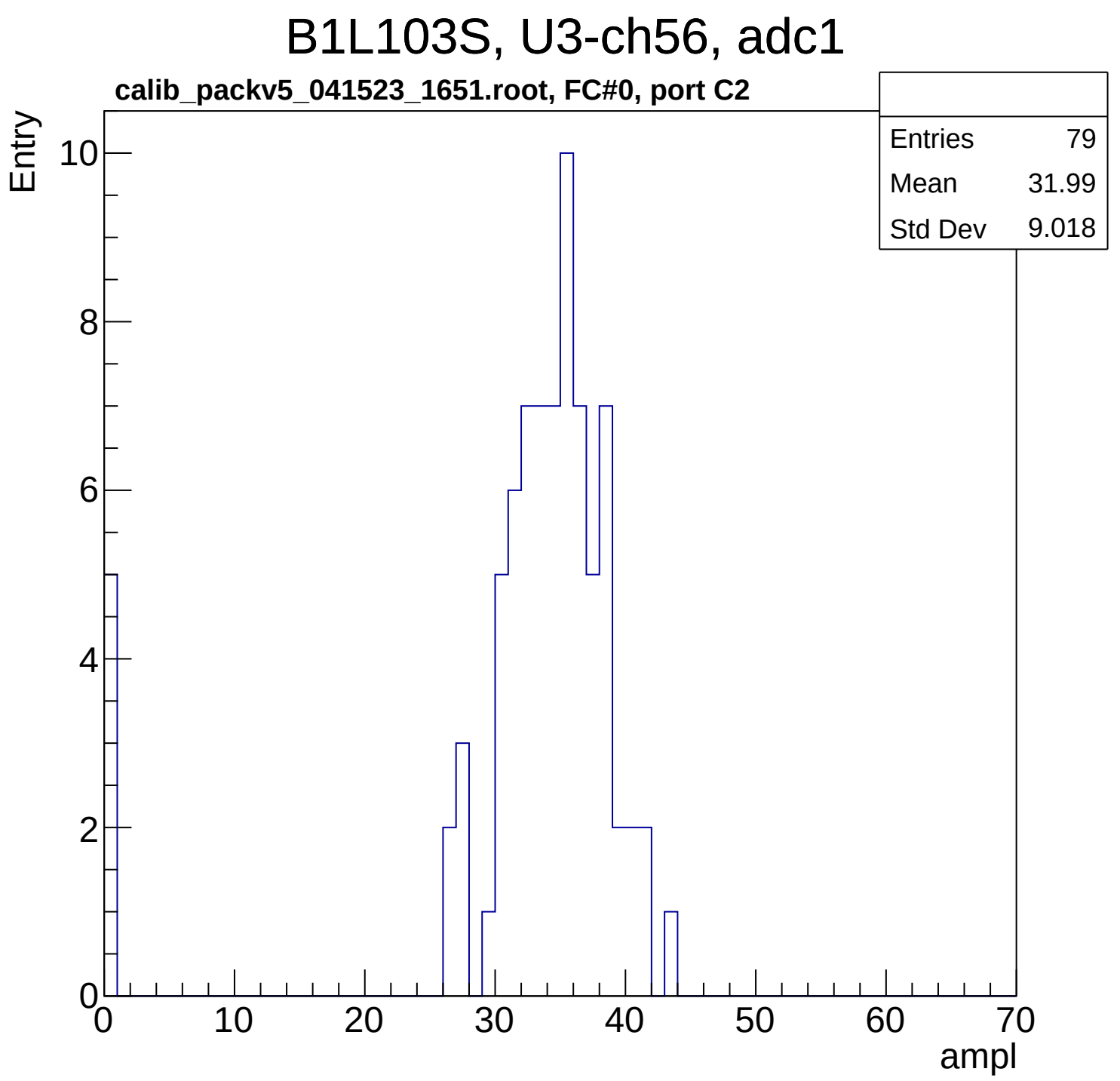
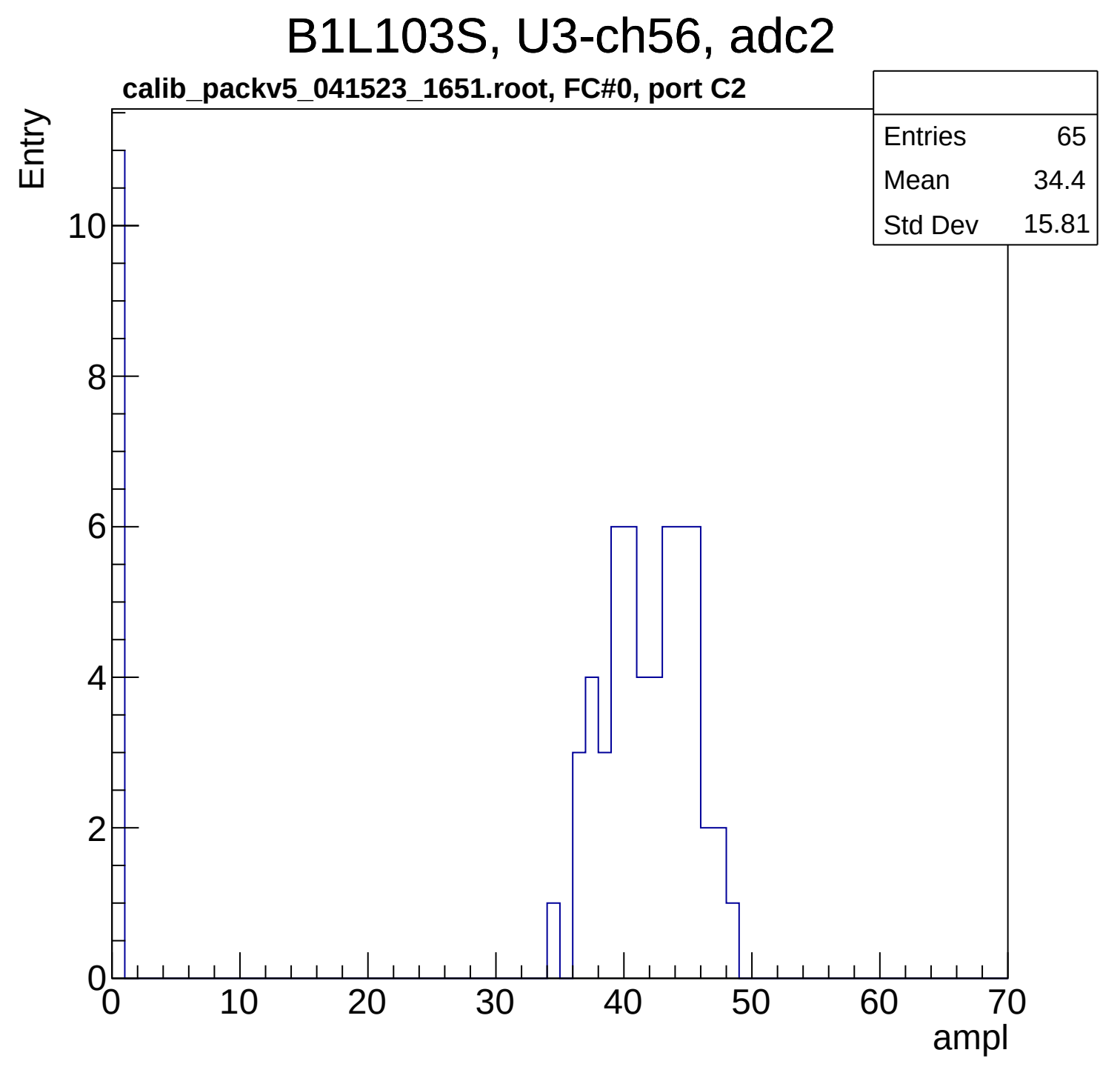
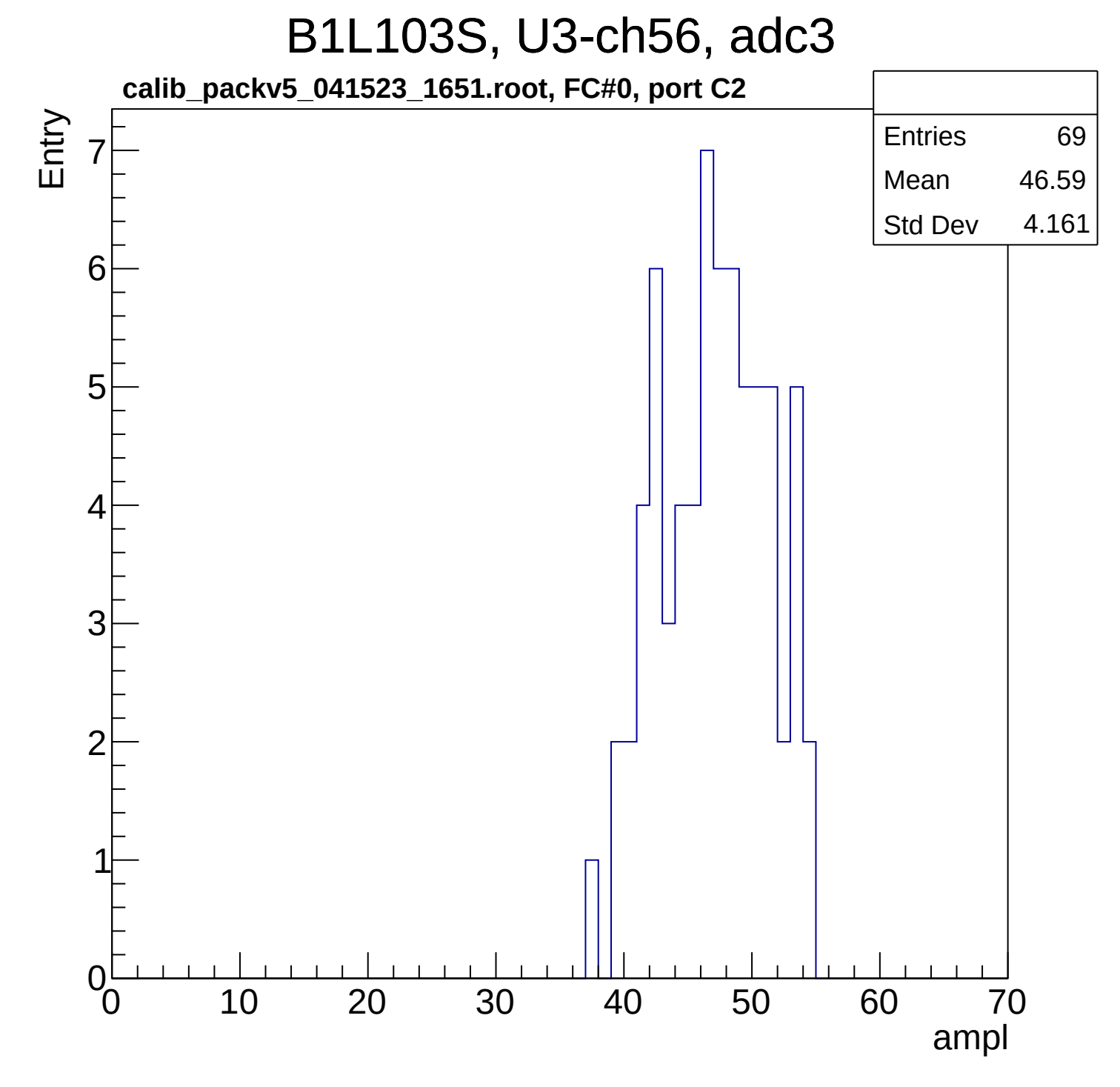
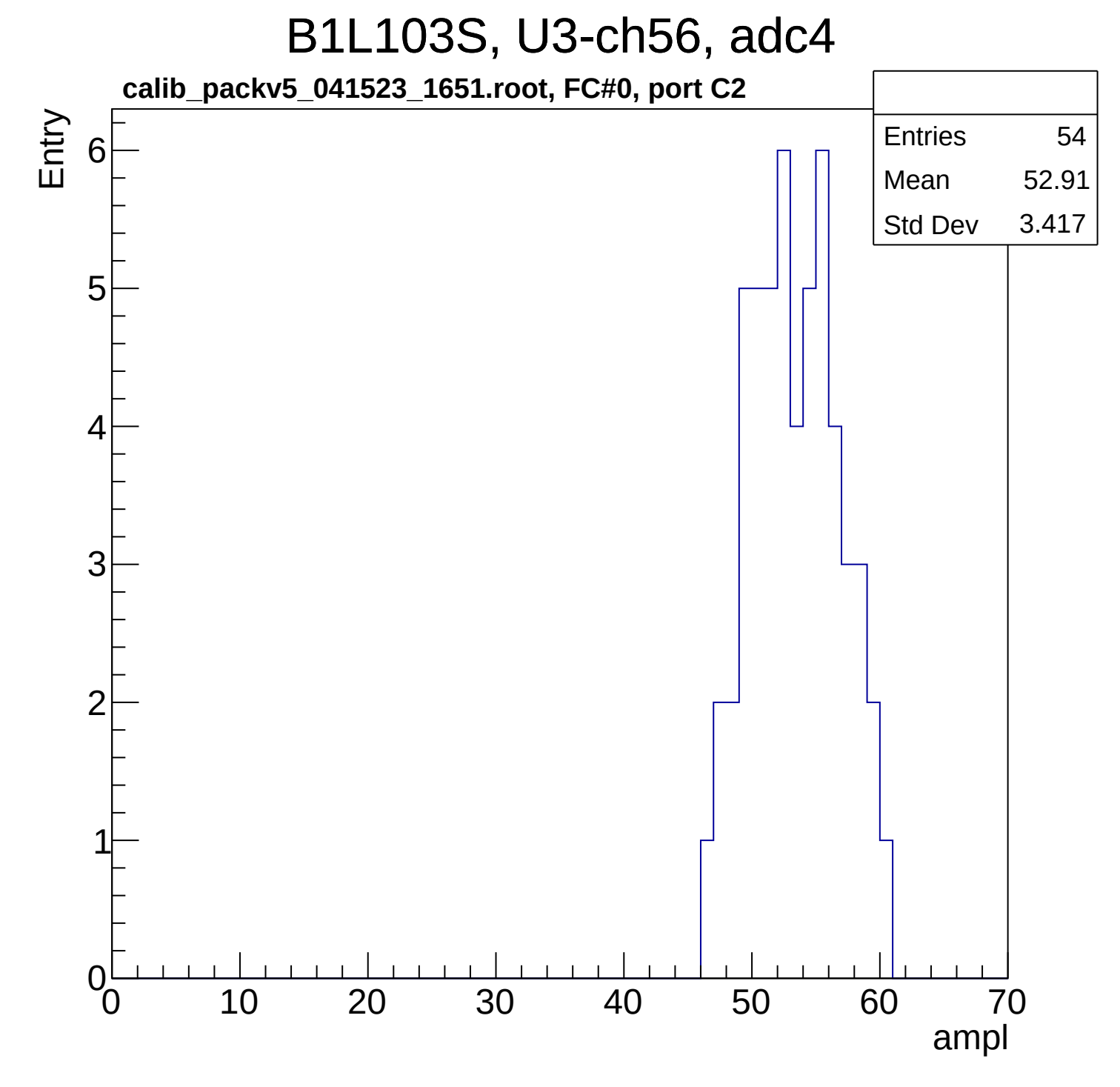
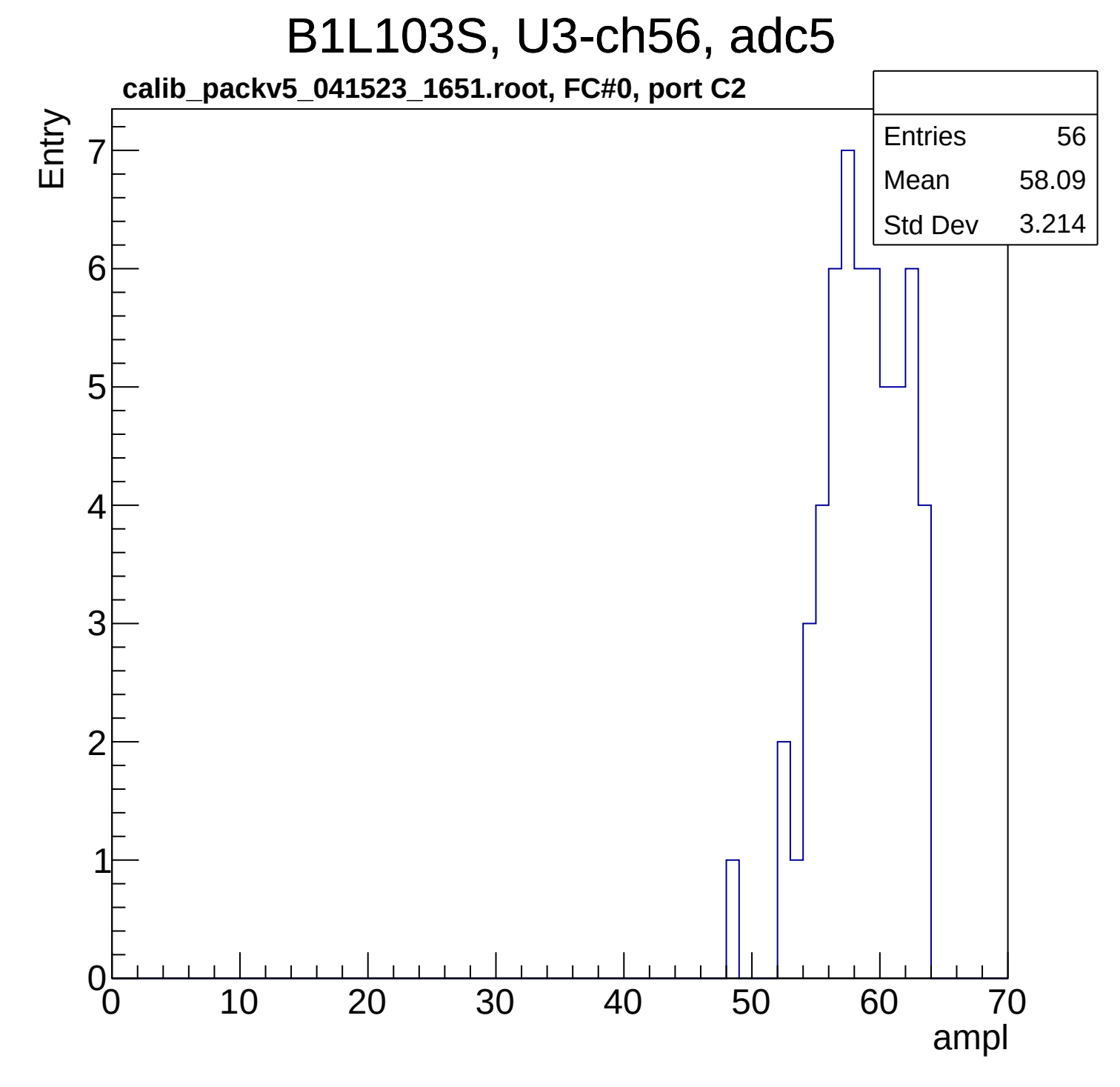
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch56, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 31.99
Std Dev 9.018
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U3-ch56, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 34.4
Std Dev 15.81
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch56, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 46.59
Std Dev 4.161
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch56, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 52.91
Std Dev 3.417
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch56, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 58.09
Std Dev 3.214
Entry
ampl
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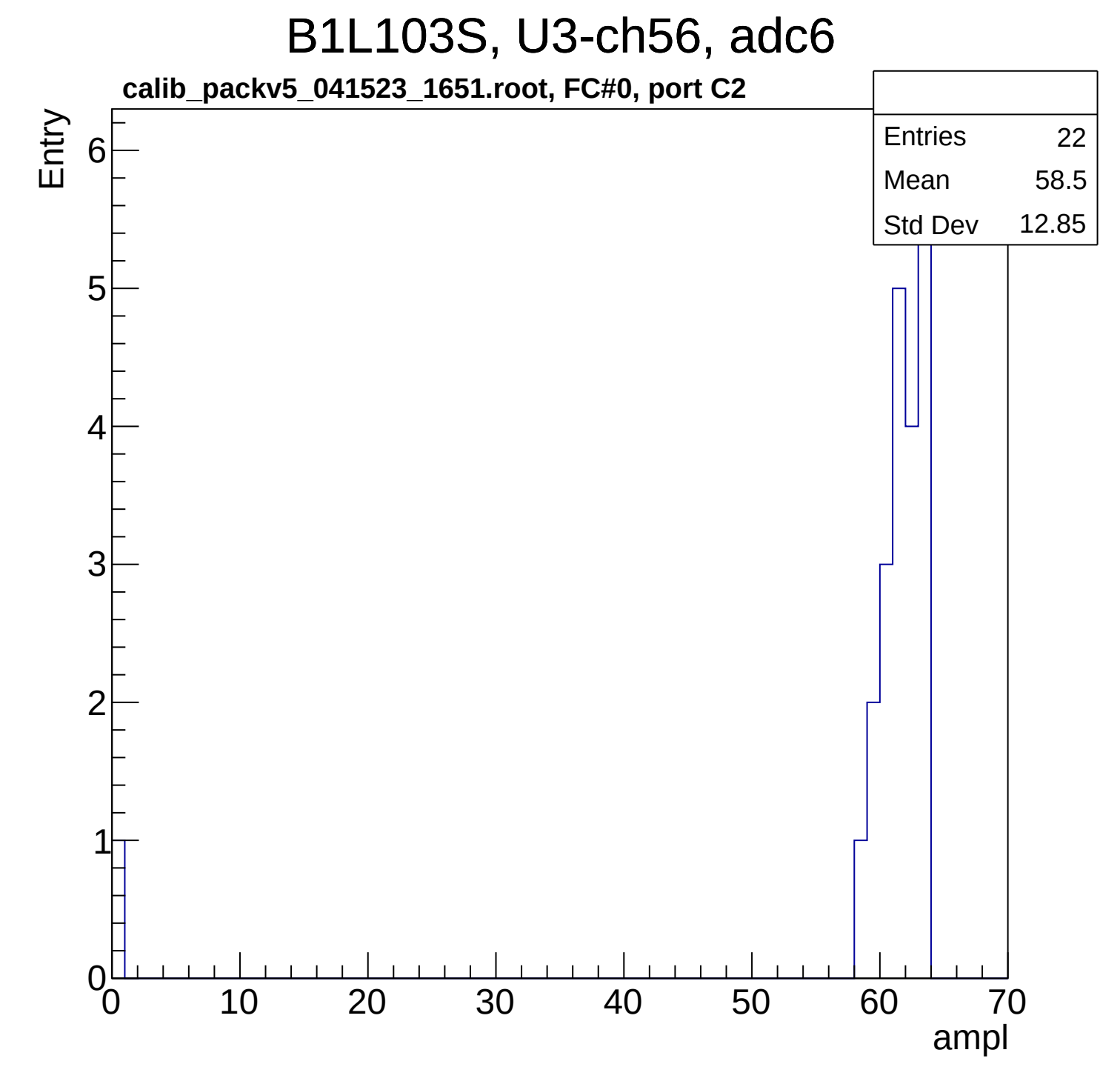
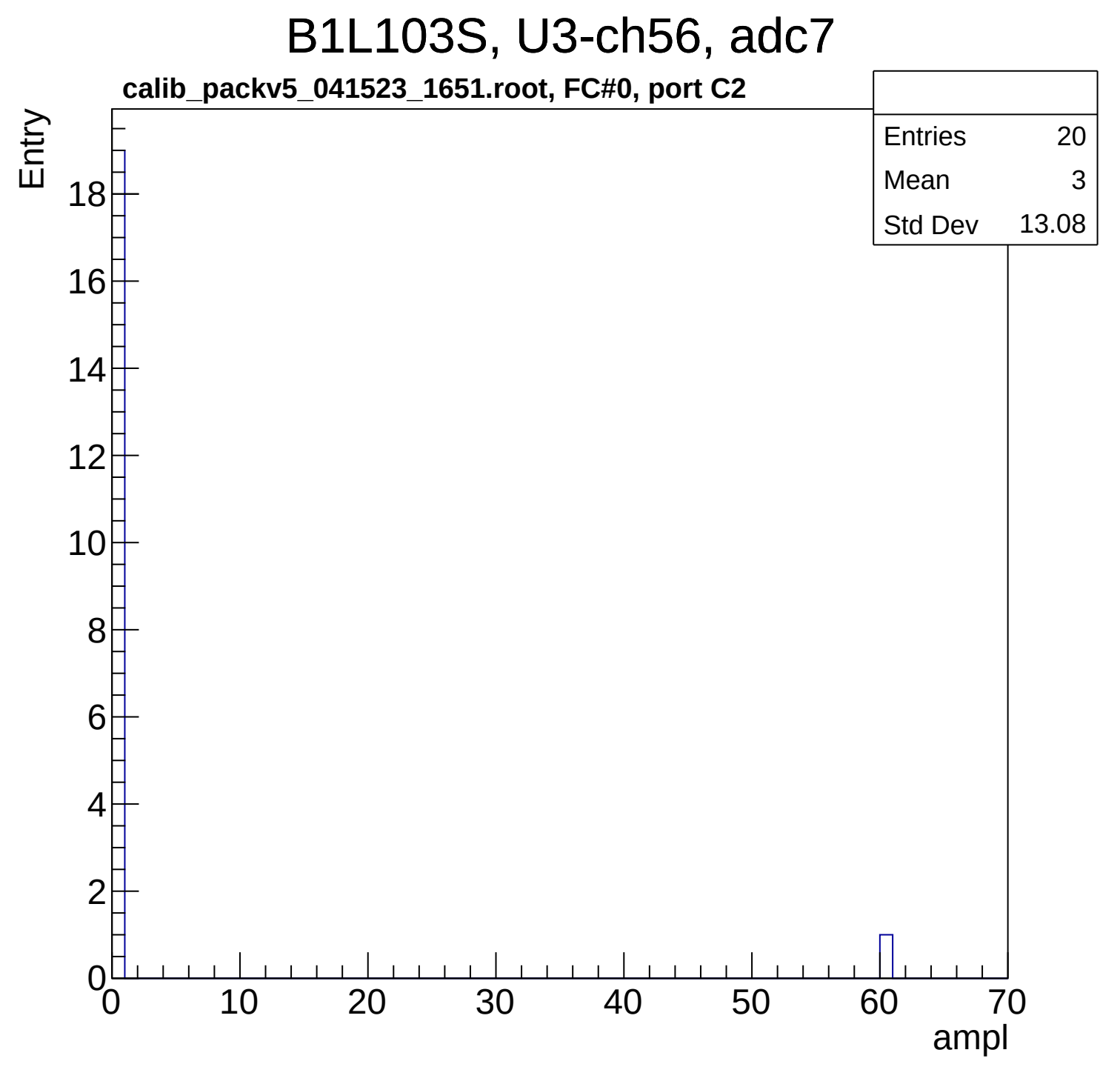
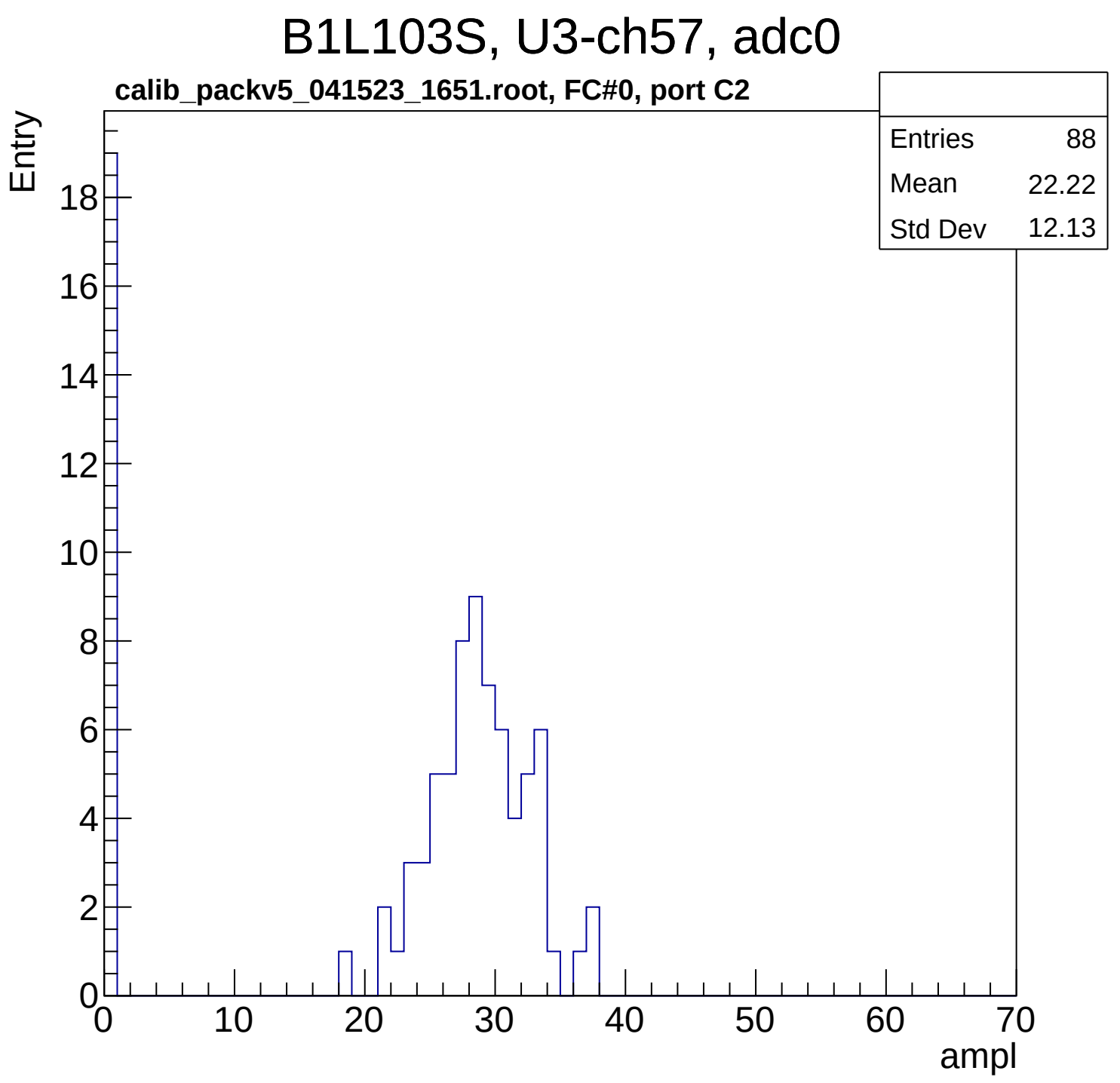
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch56, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 58.5
Std Dev 12.85
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch56, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3
Std Dev 13.08
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch57, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 22.22
Std Dev 12.13
Entry
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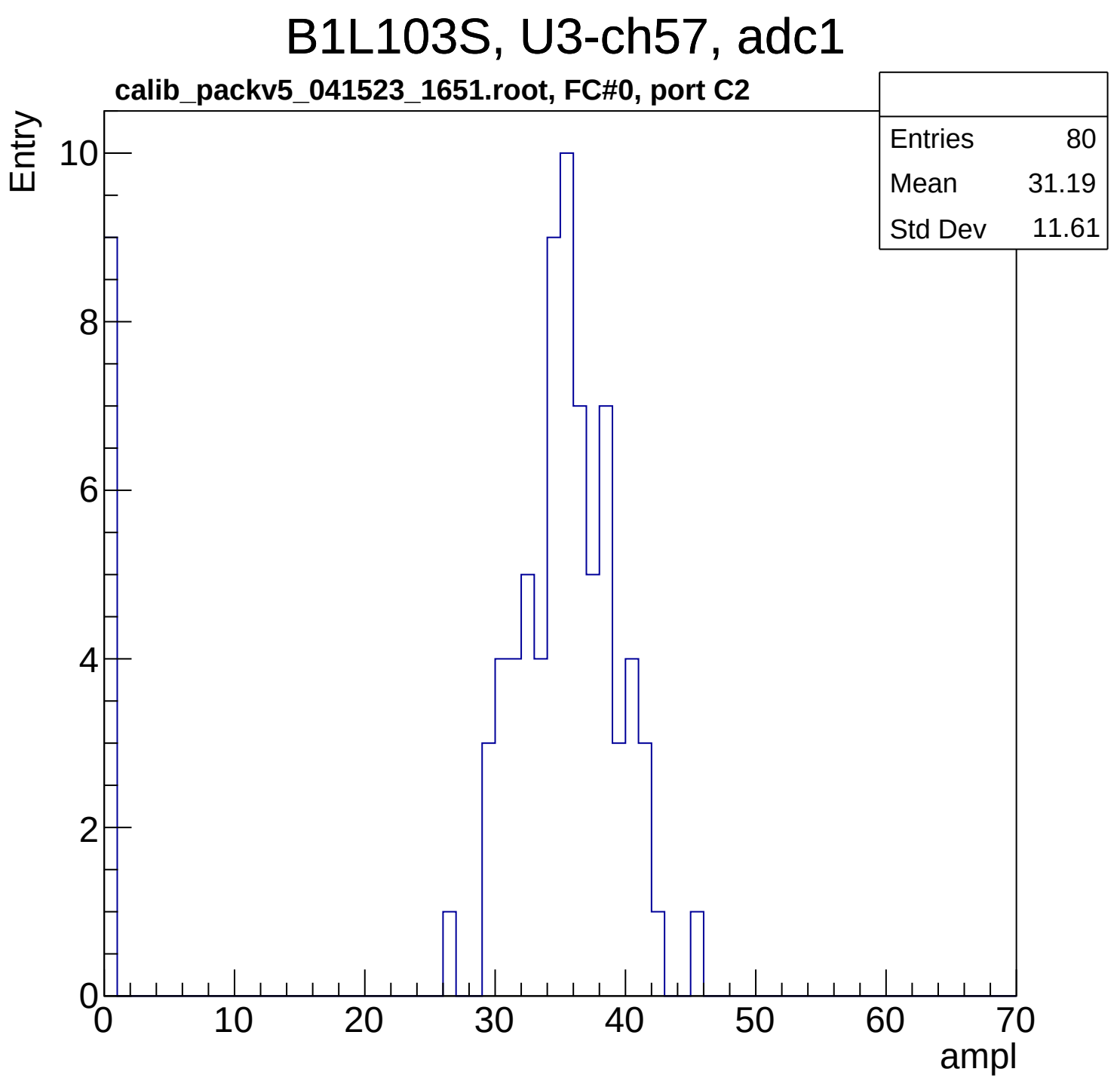
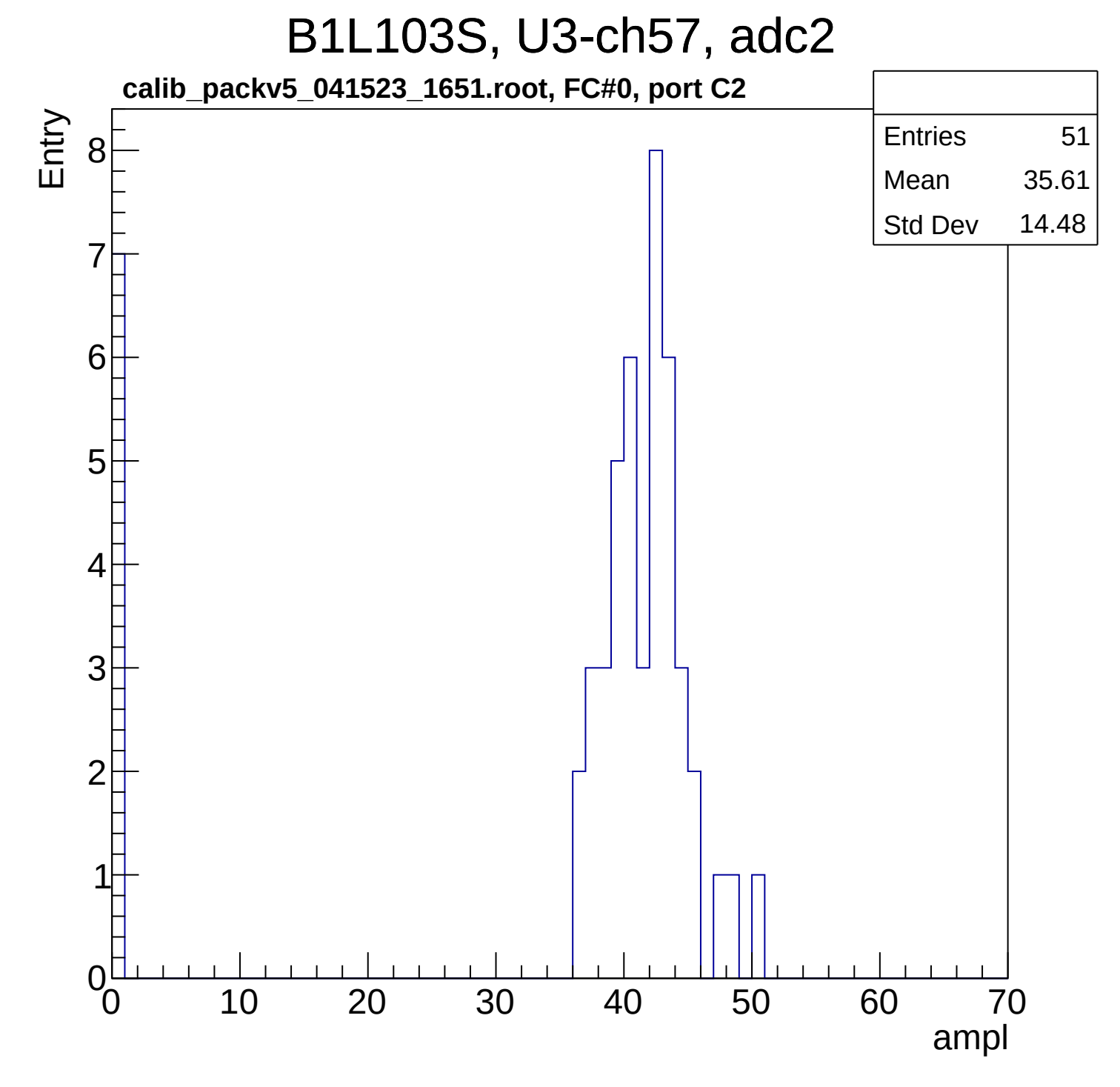
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch57, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 31.19
Std Dev 11.61
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U3-ch57, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 35.61
Std Dev 14.48
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
50
60
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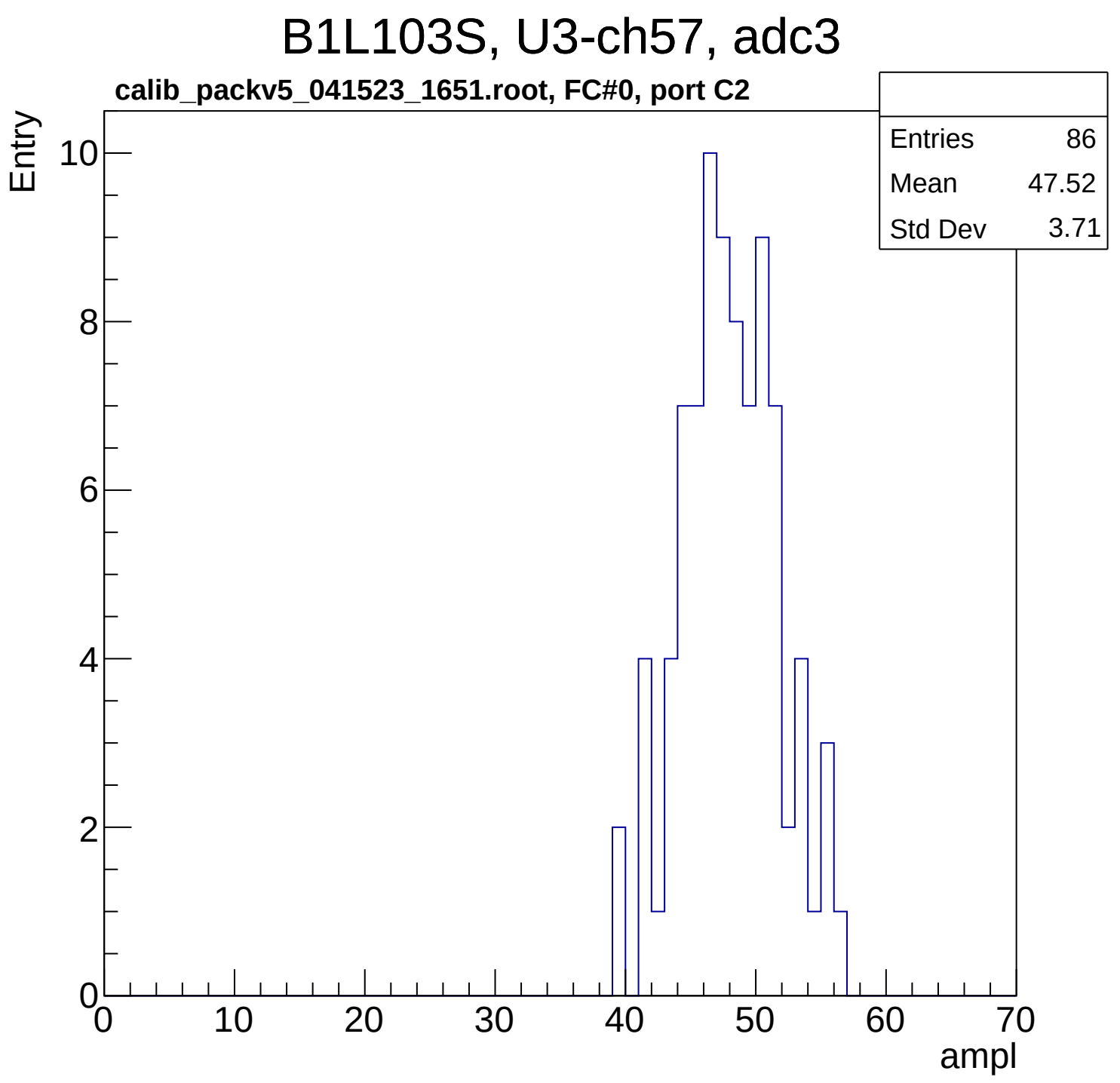
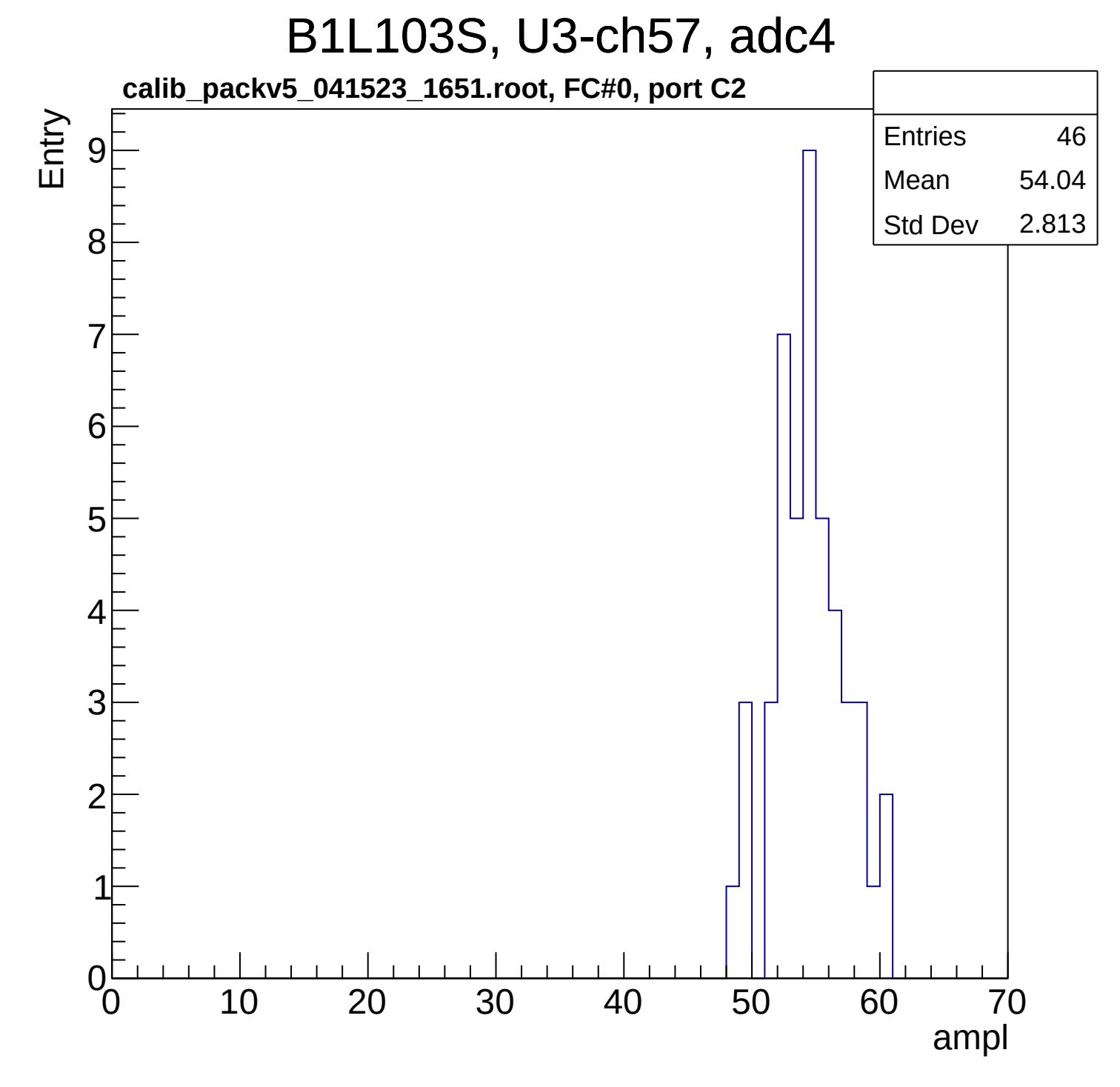

B1L103S, U3-ch57, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 47.52
Std Dev 3.71
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U3-ch57, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 54.04
Std Dev 2.813
Entry
ampl
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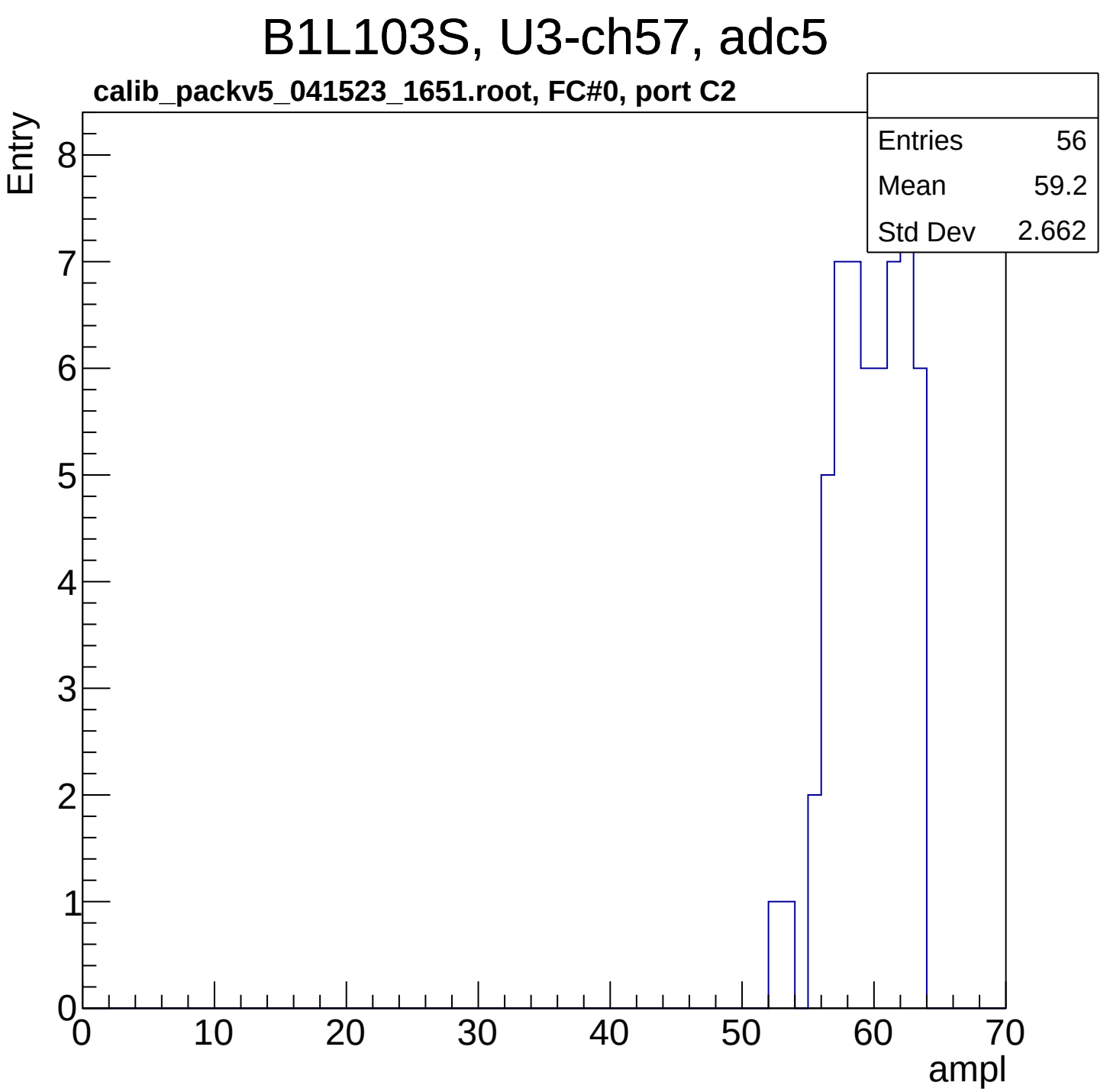
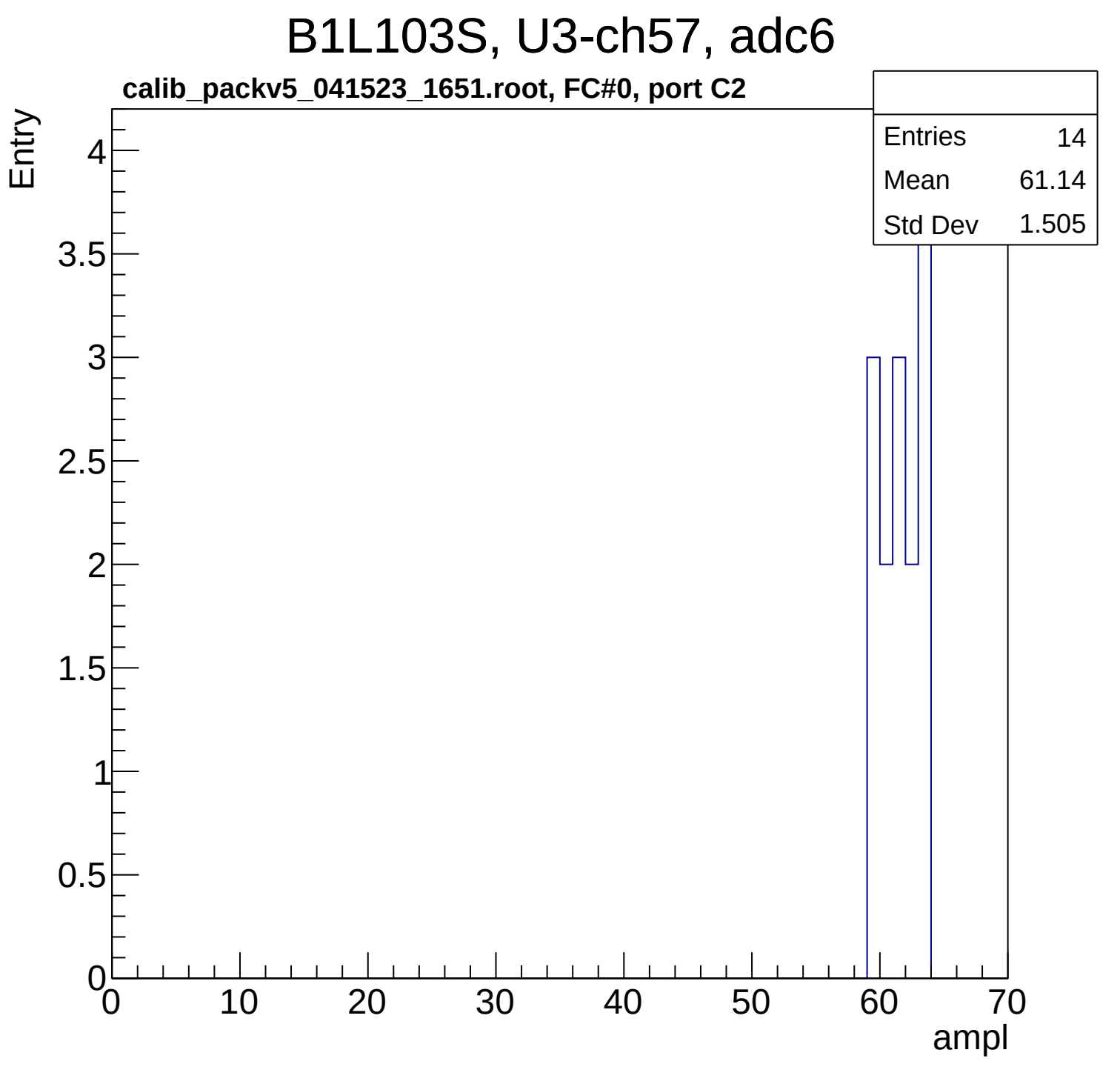
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch57, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 59.2
Std Dev 2.662
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch57, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 61.14
Std Dev 1.505
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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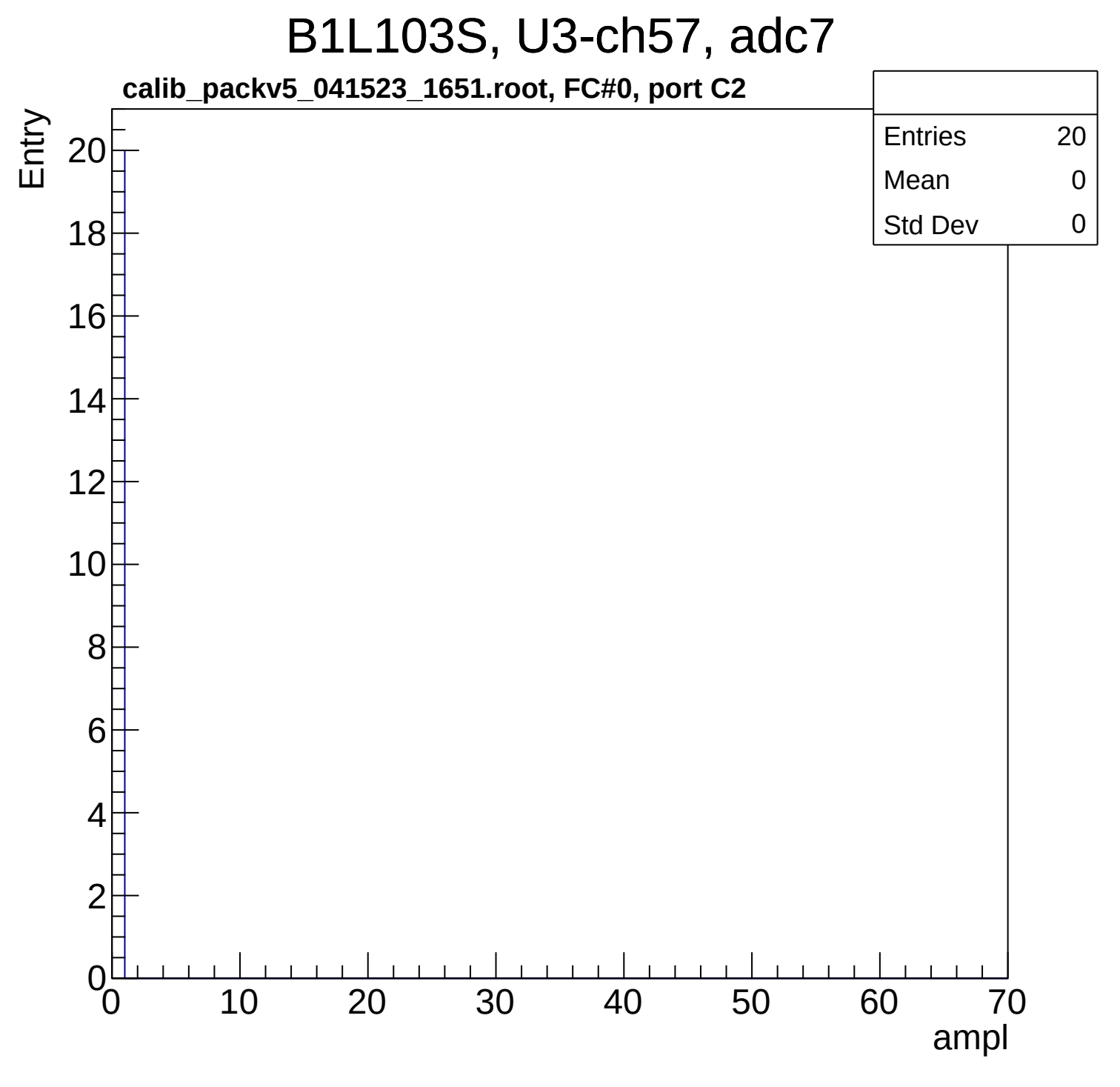
B1L103S, U3-ch57, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 0
Std Dev 0
Entry
0
2
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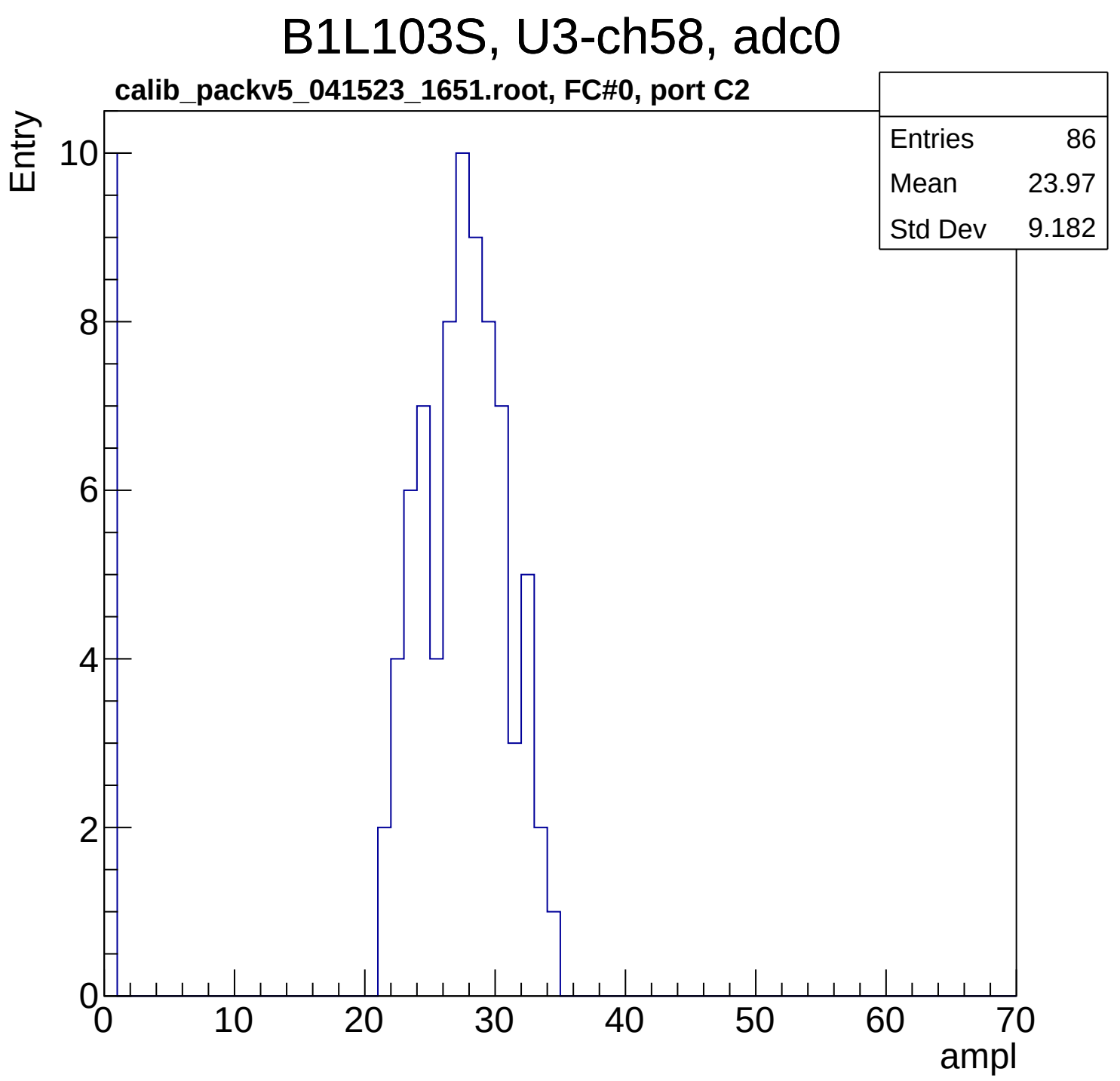
10
12
14
16
18
20
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch58, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 23.97
Std Dev 9.182
Entry
ampl
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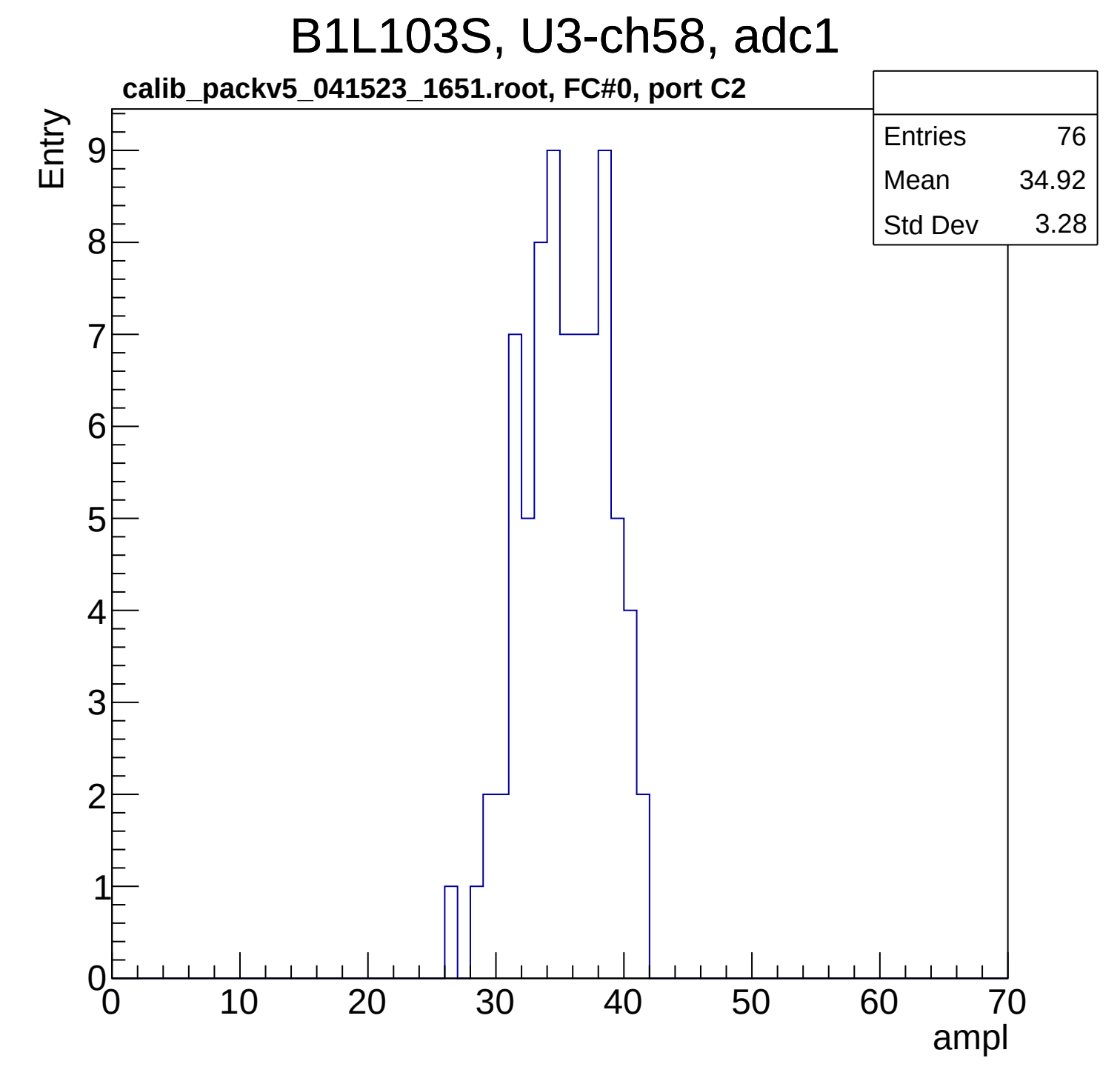
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U3-ch58, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 34.92
Std Dev 3.28
Entry
ampl
0
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2
3
4
5
6
7
8
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0
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40
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60
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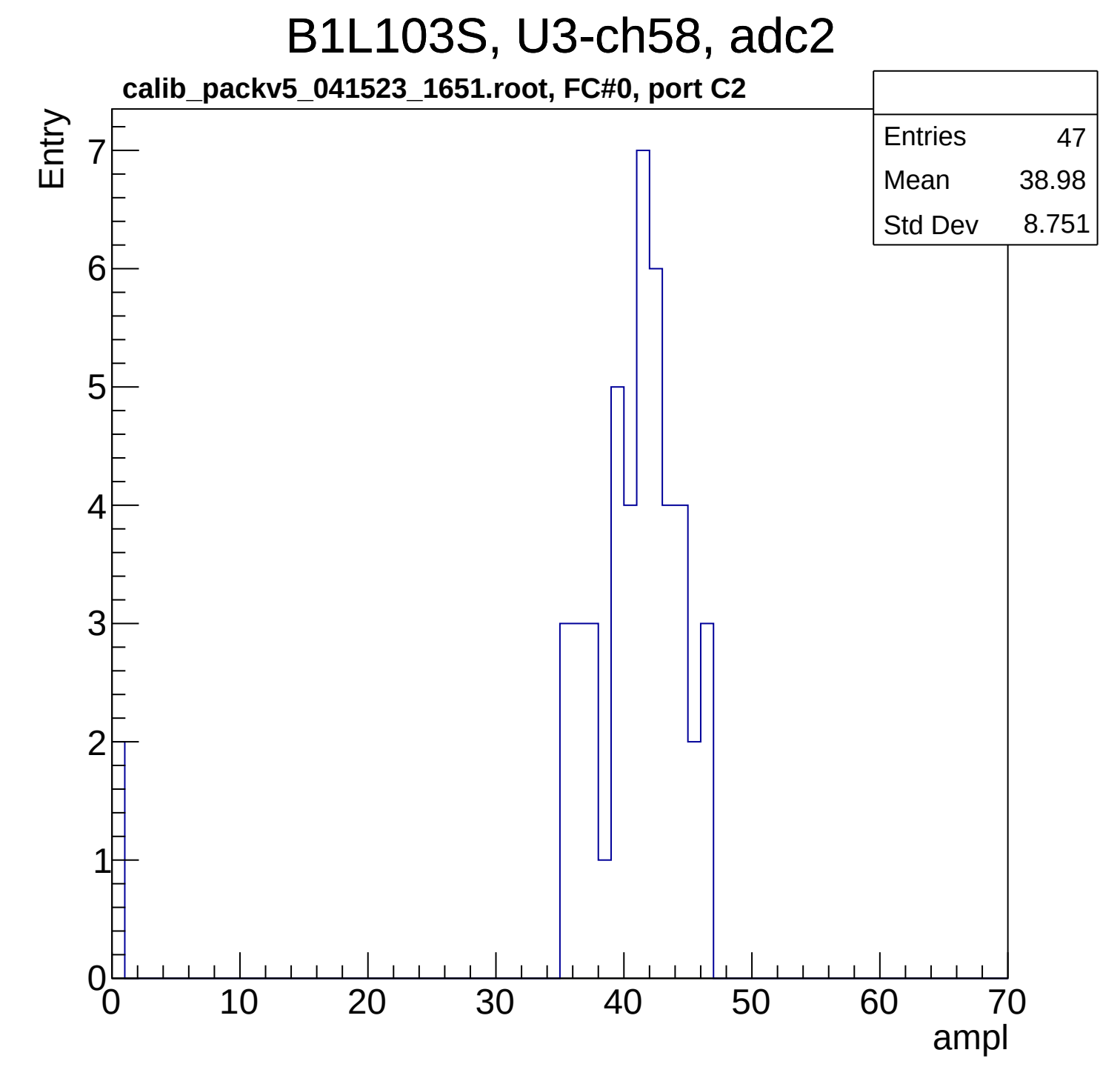
B1L103S, U3-ch58, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 38.98
Std Dev 8.751
Entry
ampl
0
1
2
3
4
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6
7
0
10
20
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40
50
60
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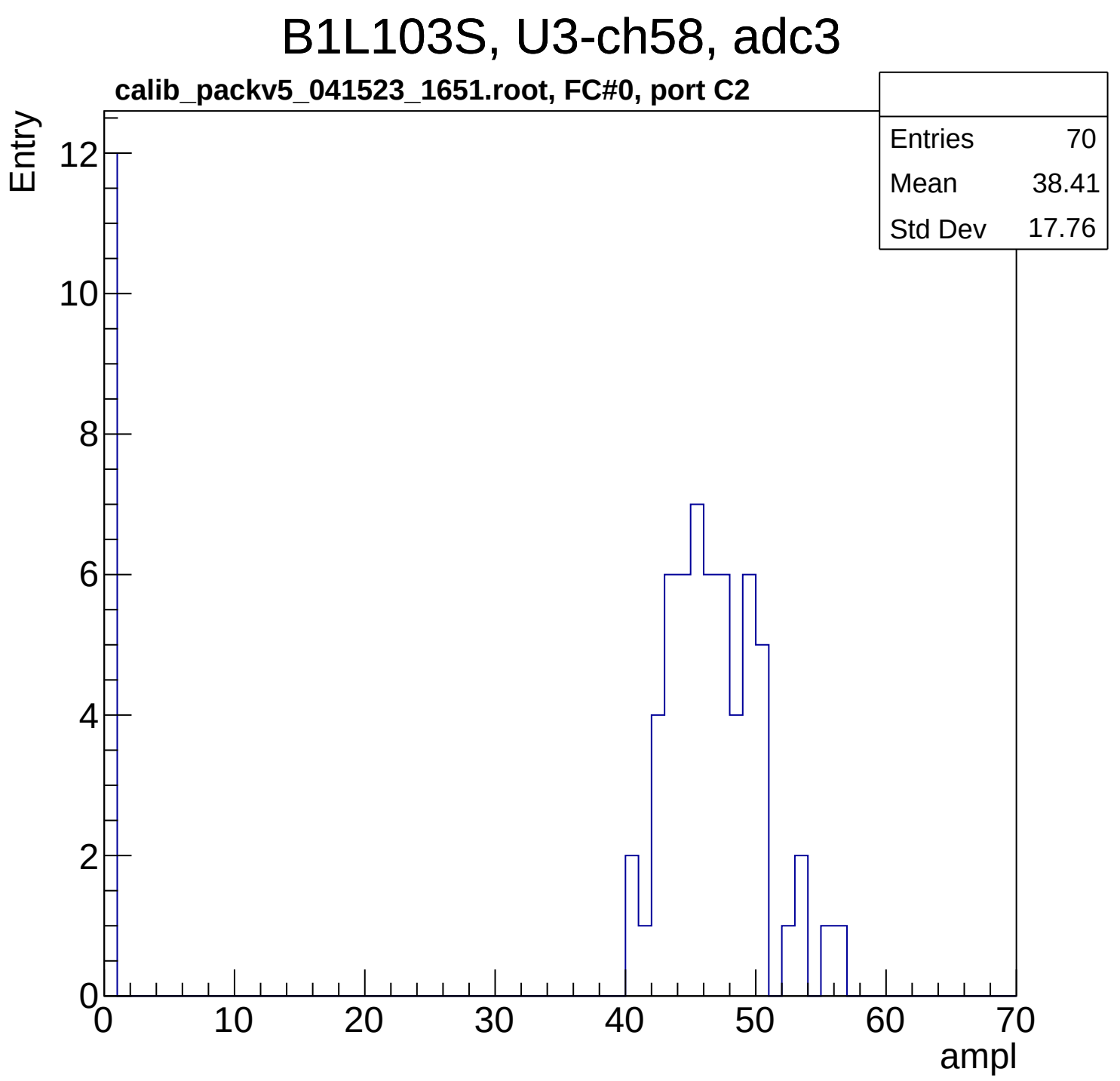
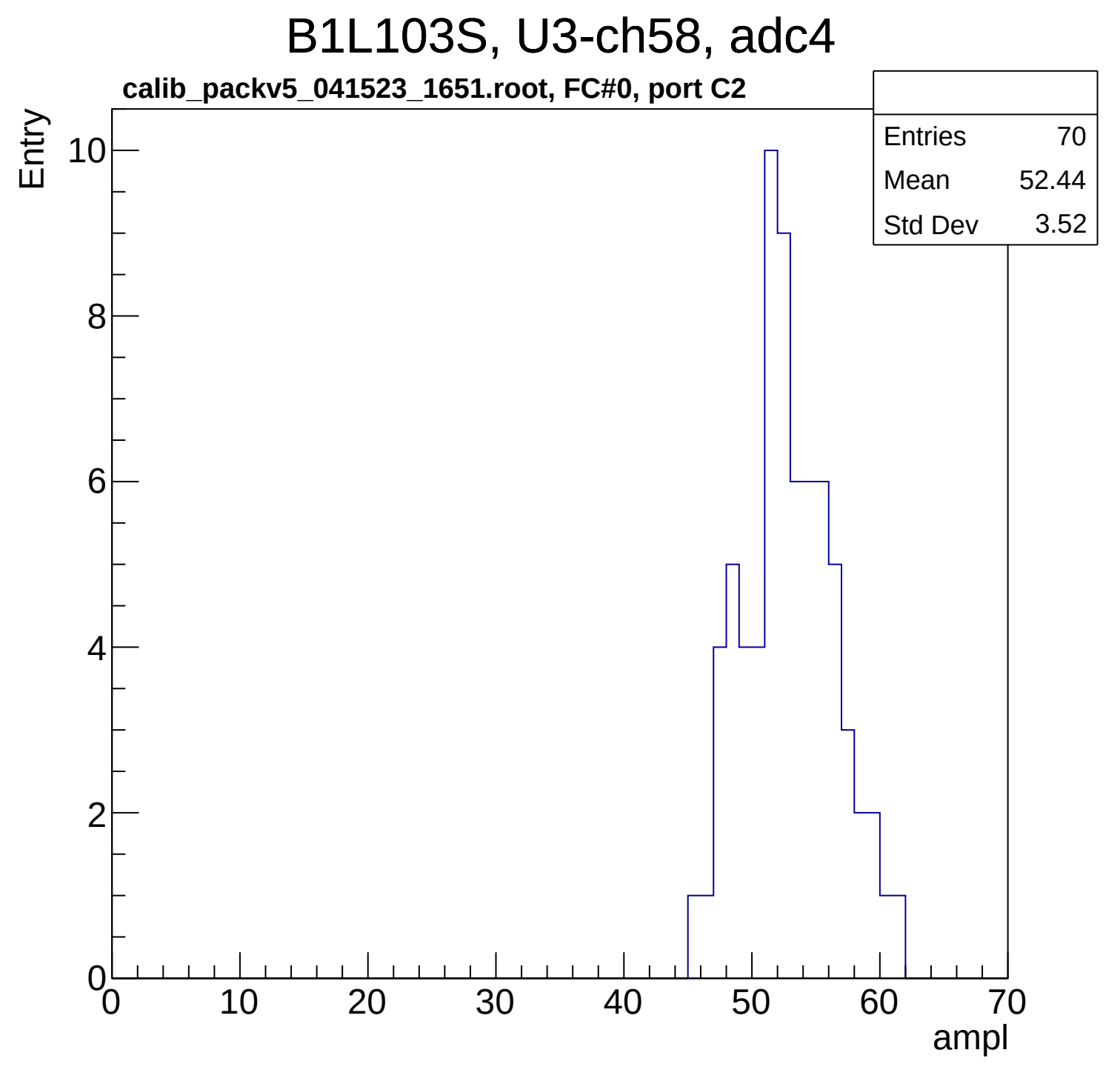
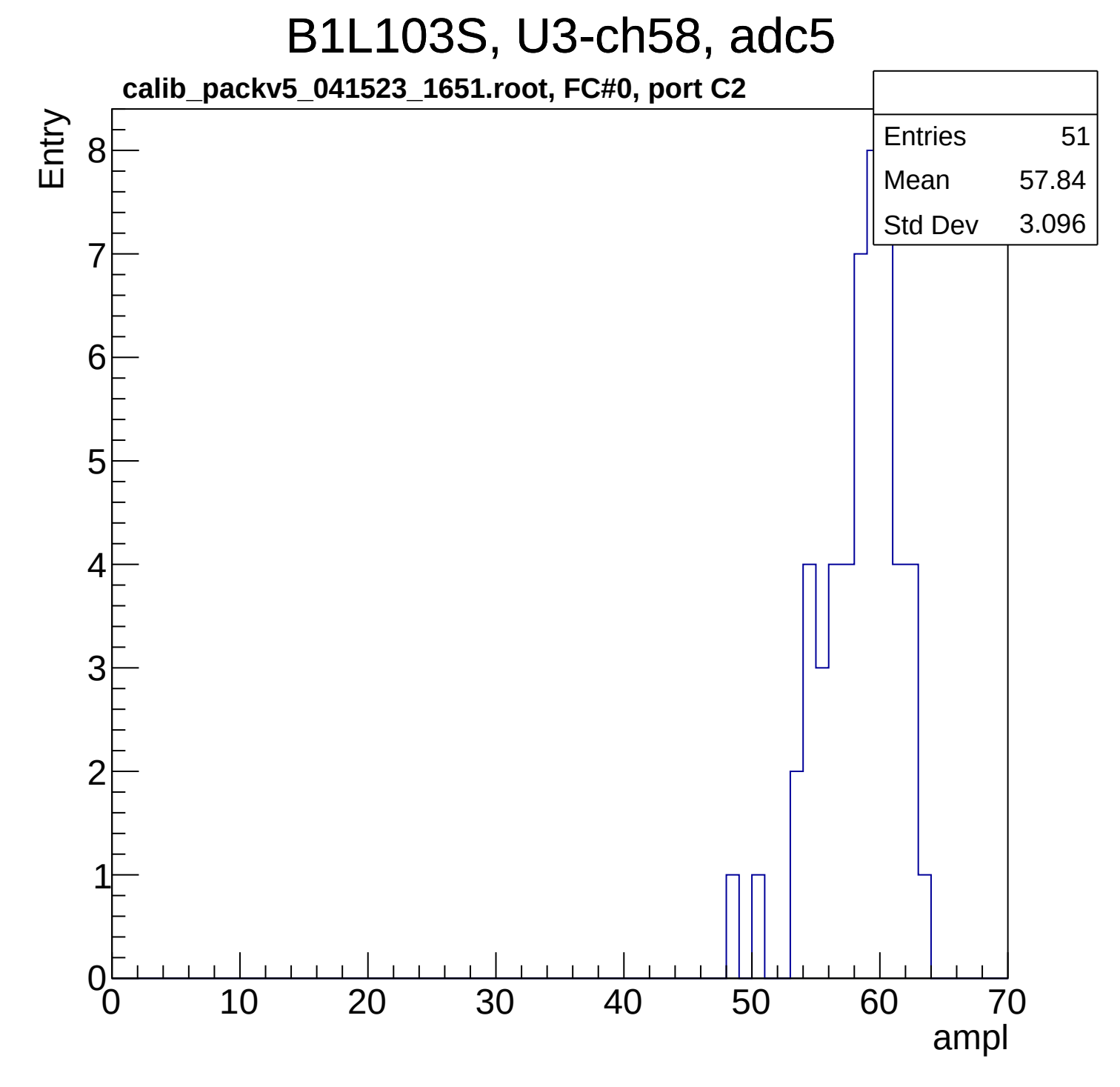

B1L103S, U3-ch58, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 38.41
Std Dev 17.76
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch58, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 52.44
Std Dev 3.52
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch58, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 57.84
Std Dev 3.096
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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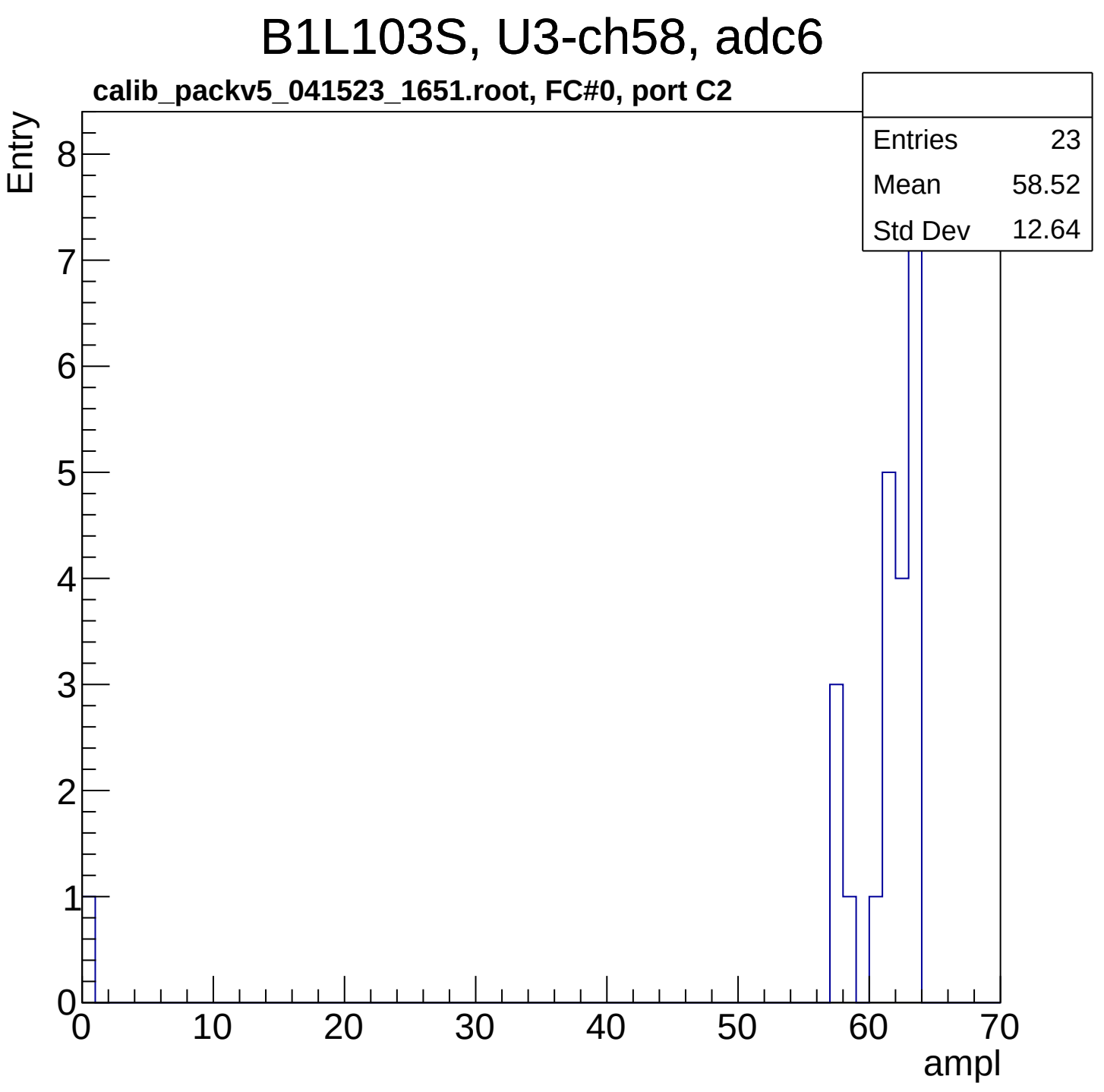
B1L103S, U3-ch58, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 58.52
Std Dev 12.64
Entry
ampl
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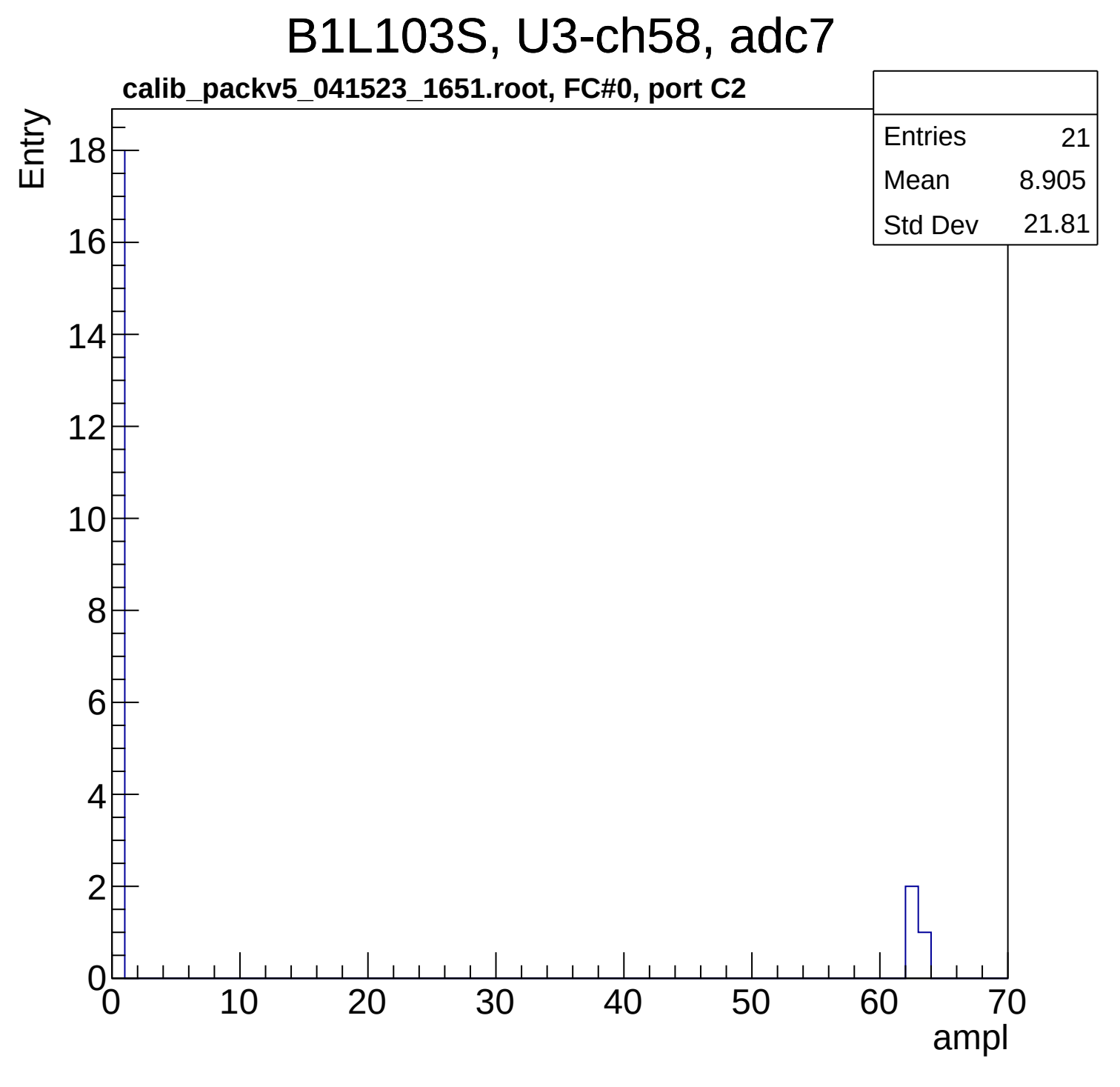
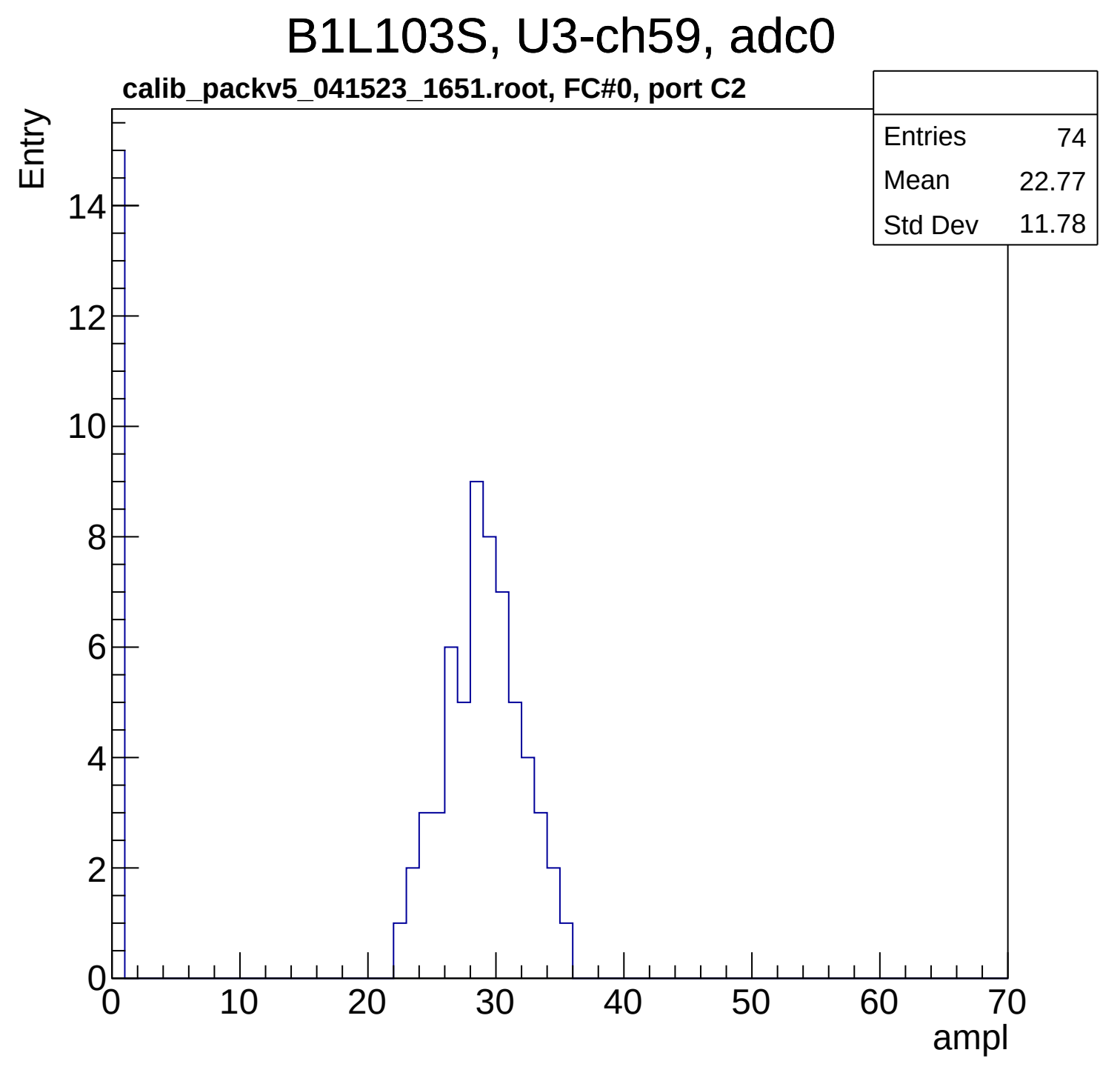
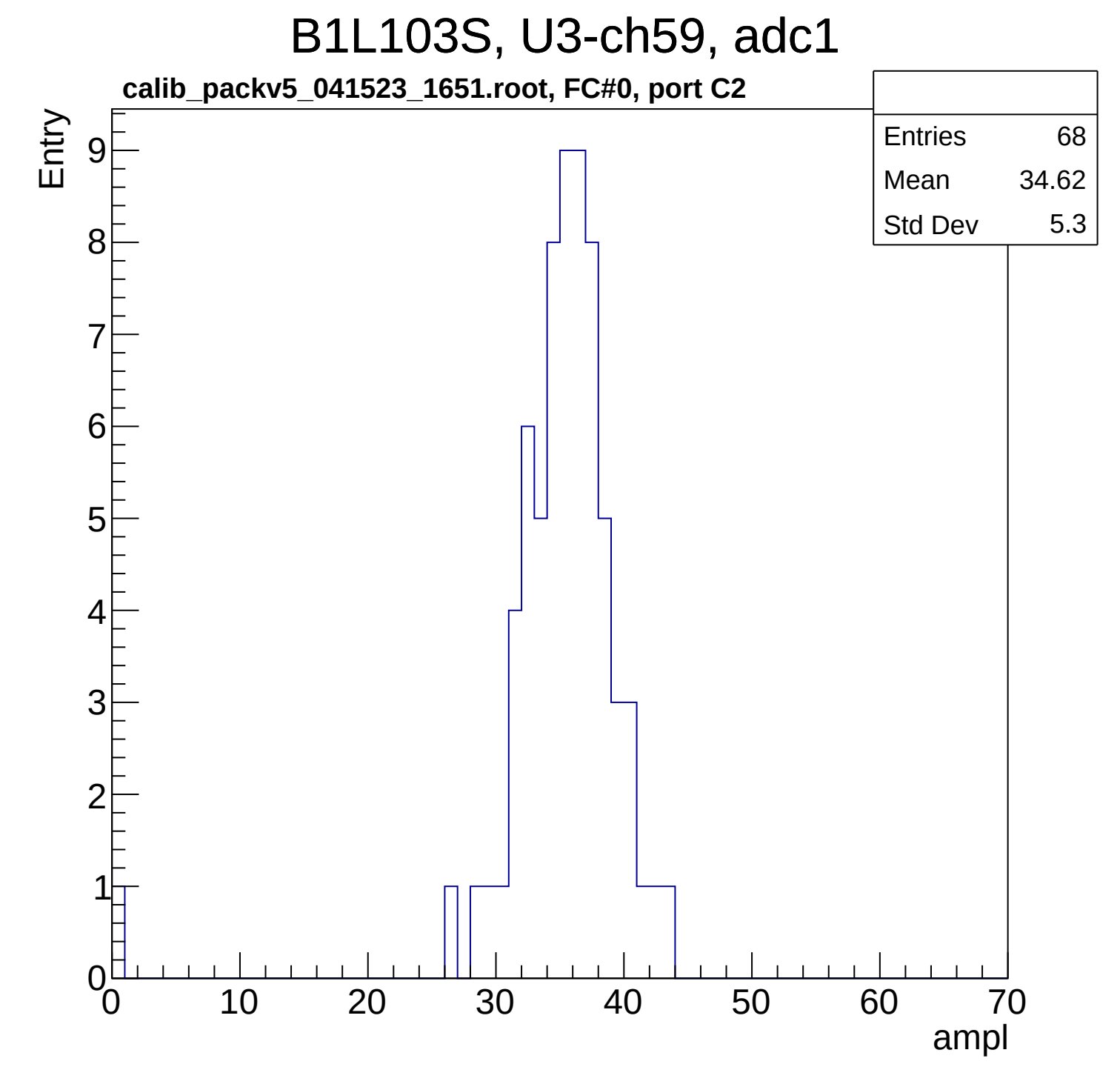
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch58, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 8.905
Std Dev 21.81
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch59, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 22.77
Std Dev 11.78
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch59, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 34.62
Std Dev 5.3
Entry
ampl
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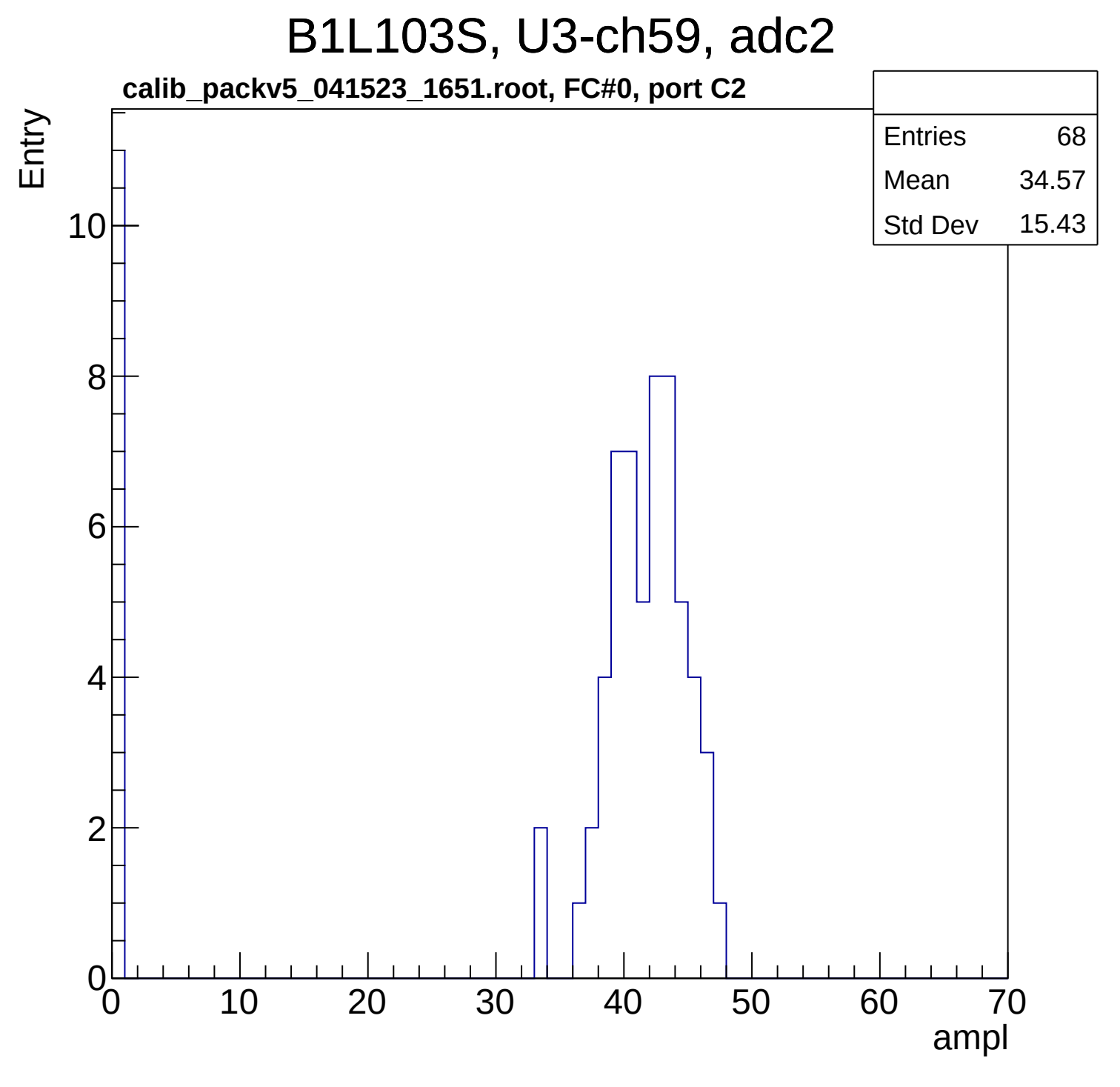
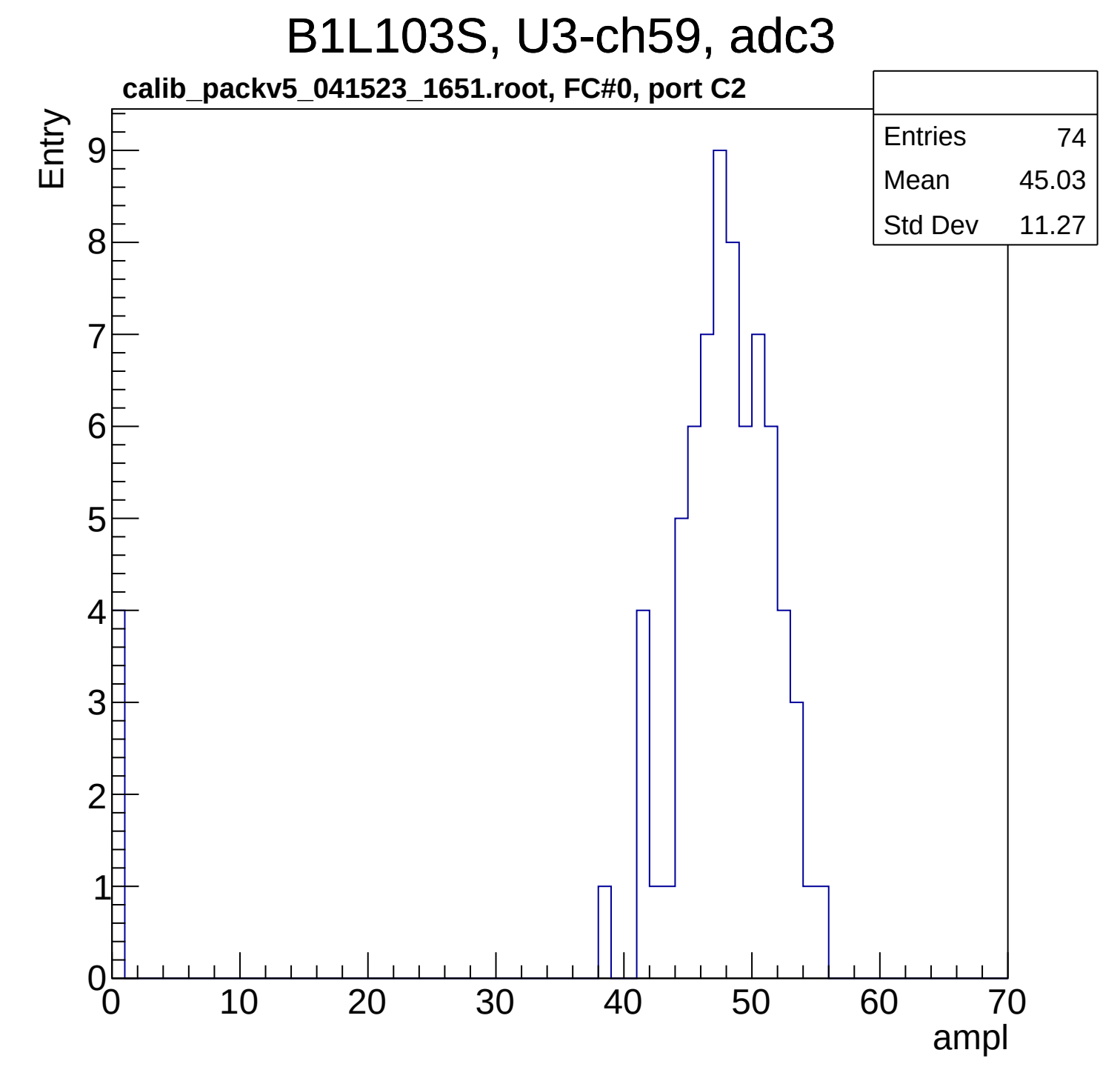
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch59, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 34.57
Std Dev 15.43
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch59, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 45.03
Std Dev 11.27
Entry
ampl
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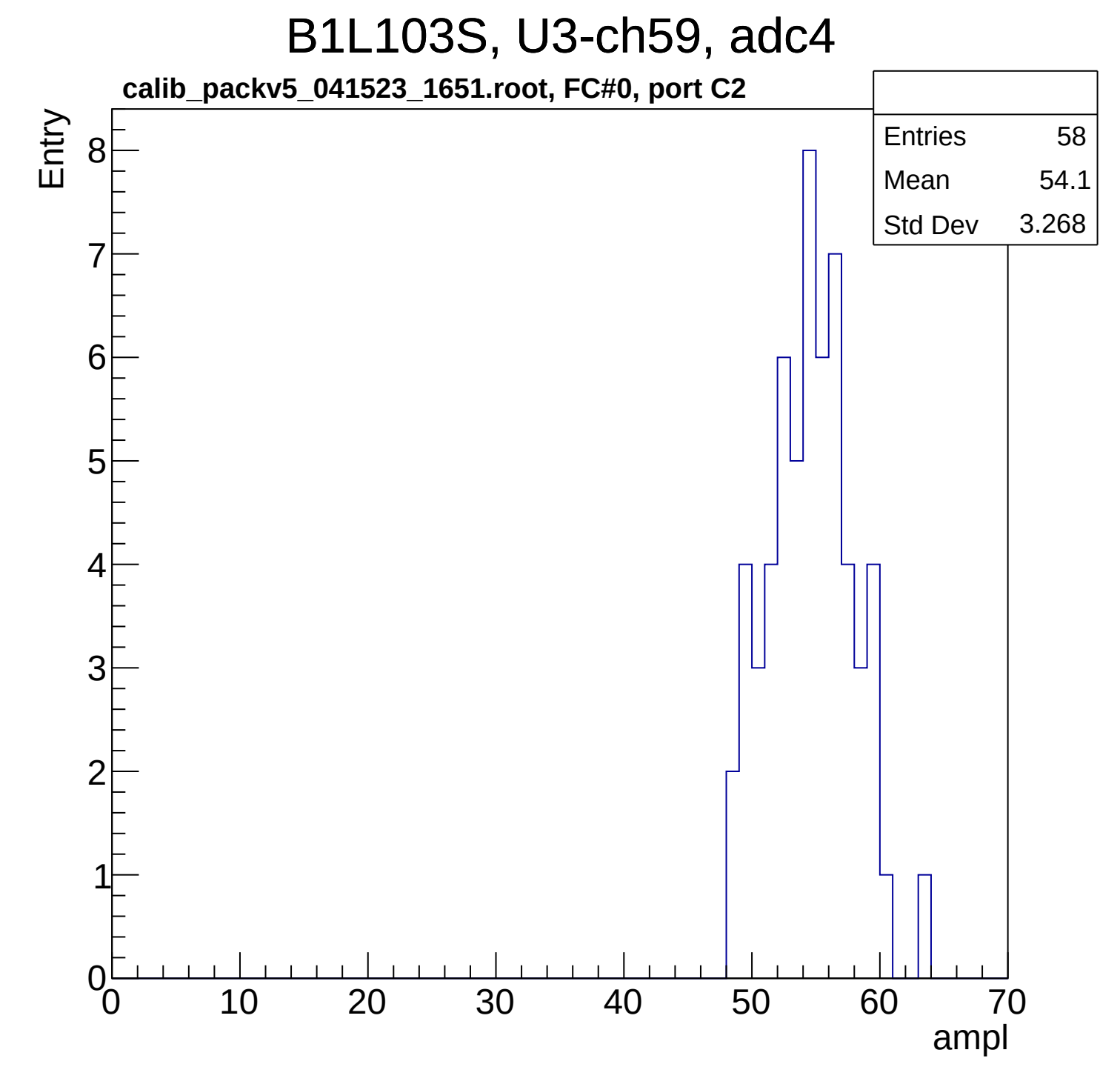
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch59, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 54.1
Std Dev 3.268
Entry
ampl
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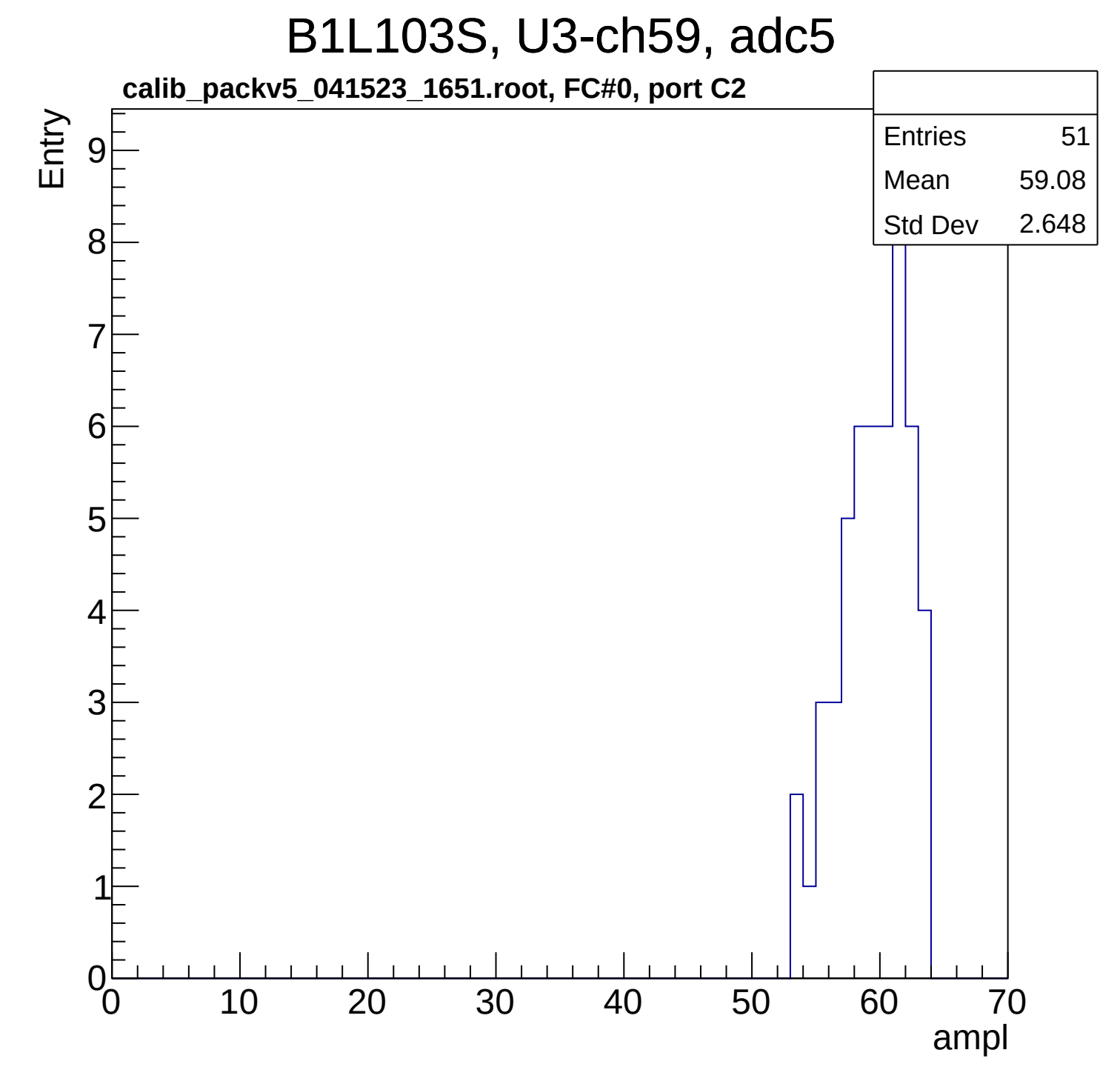
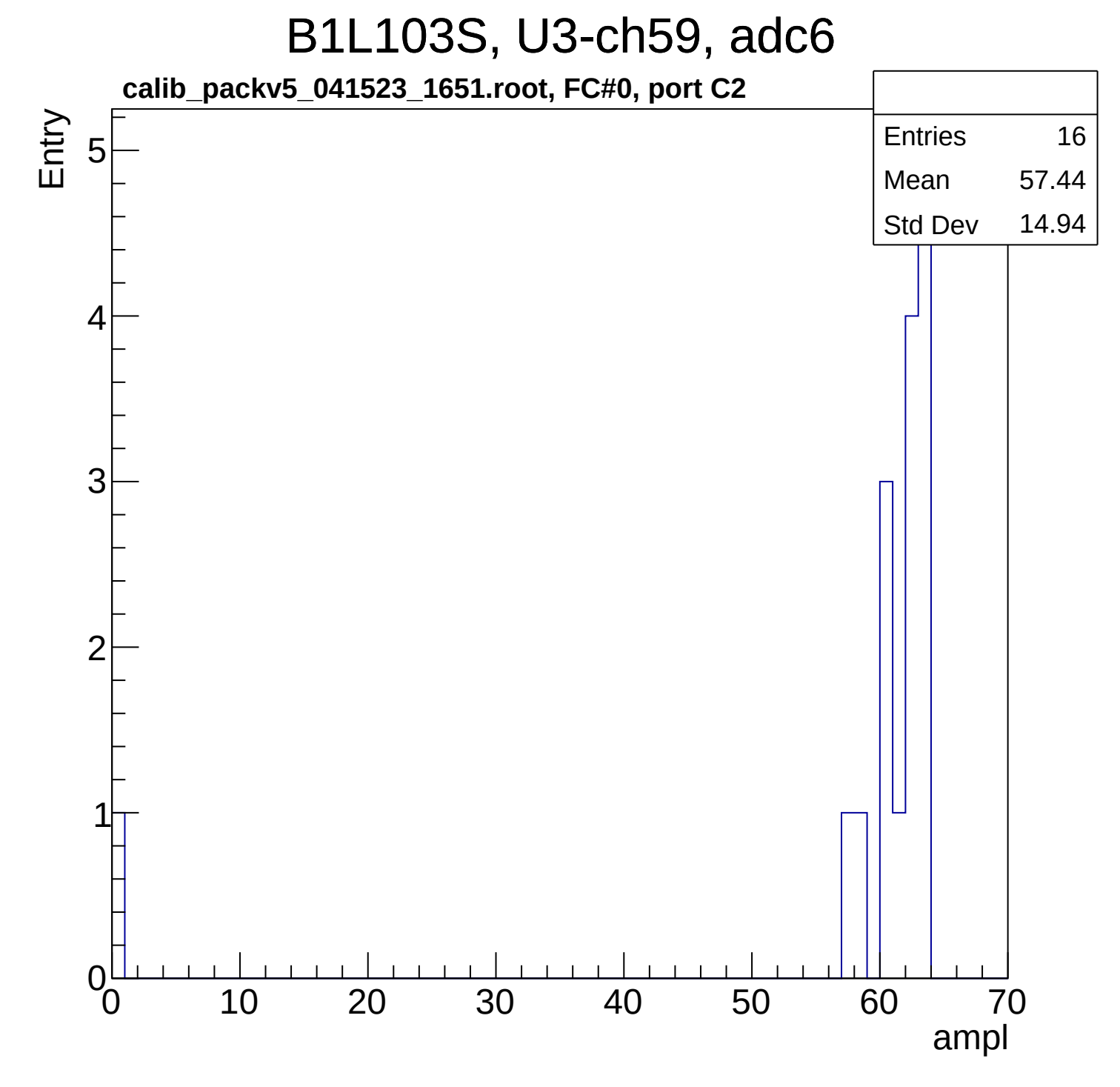
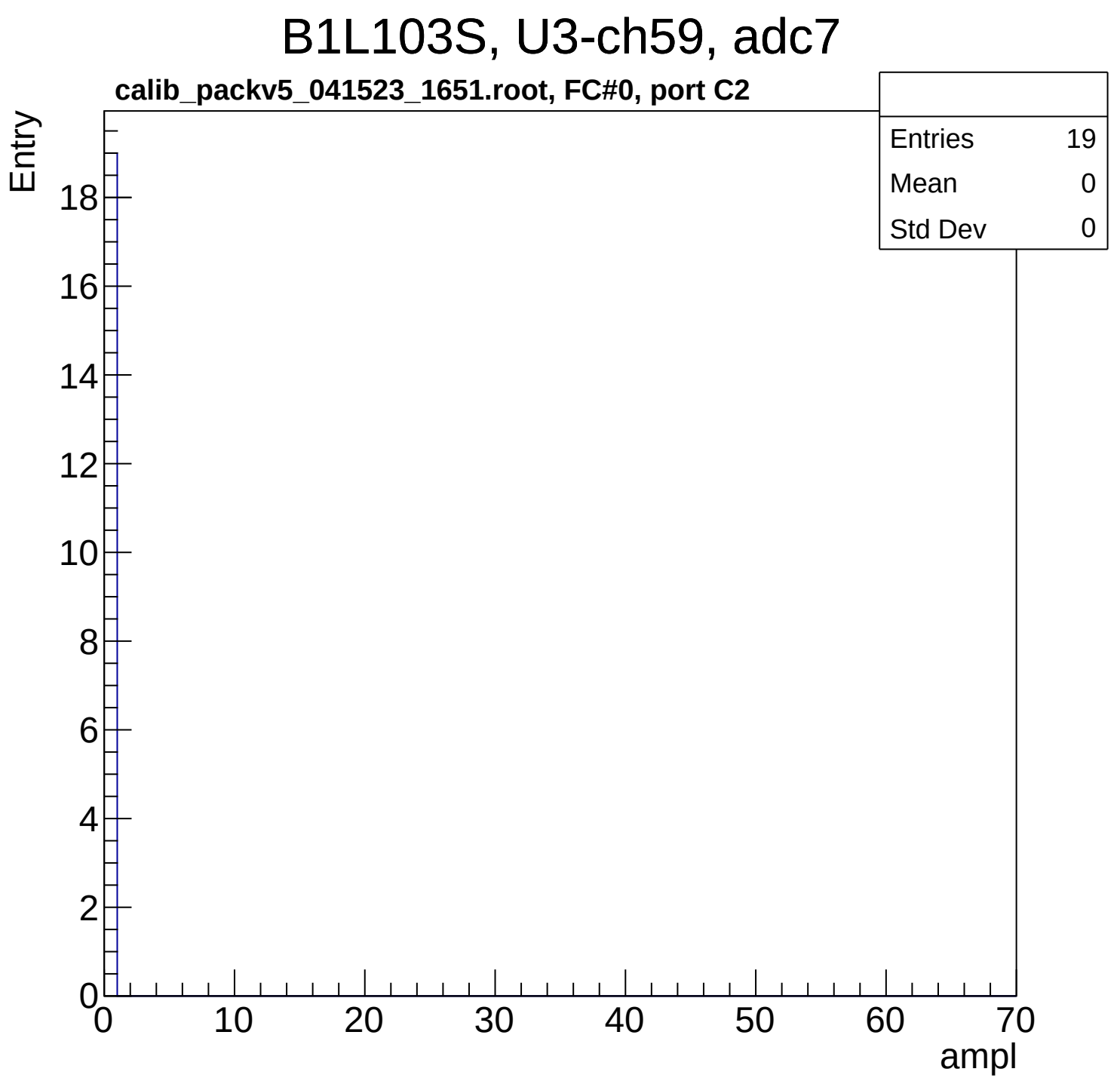
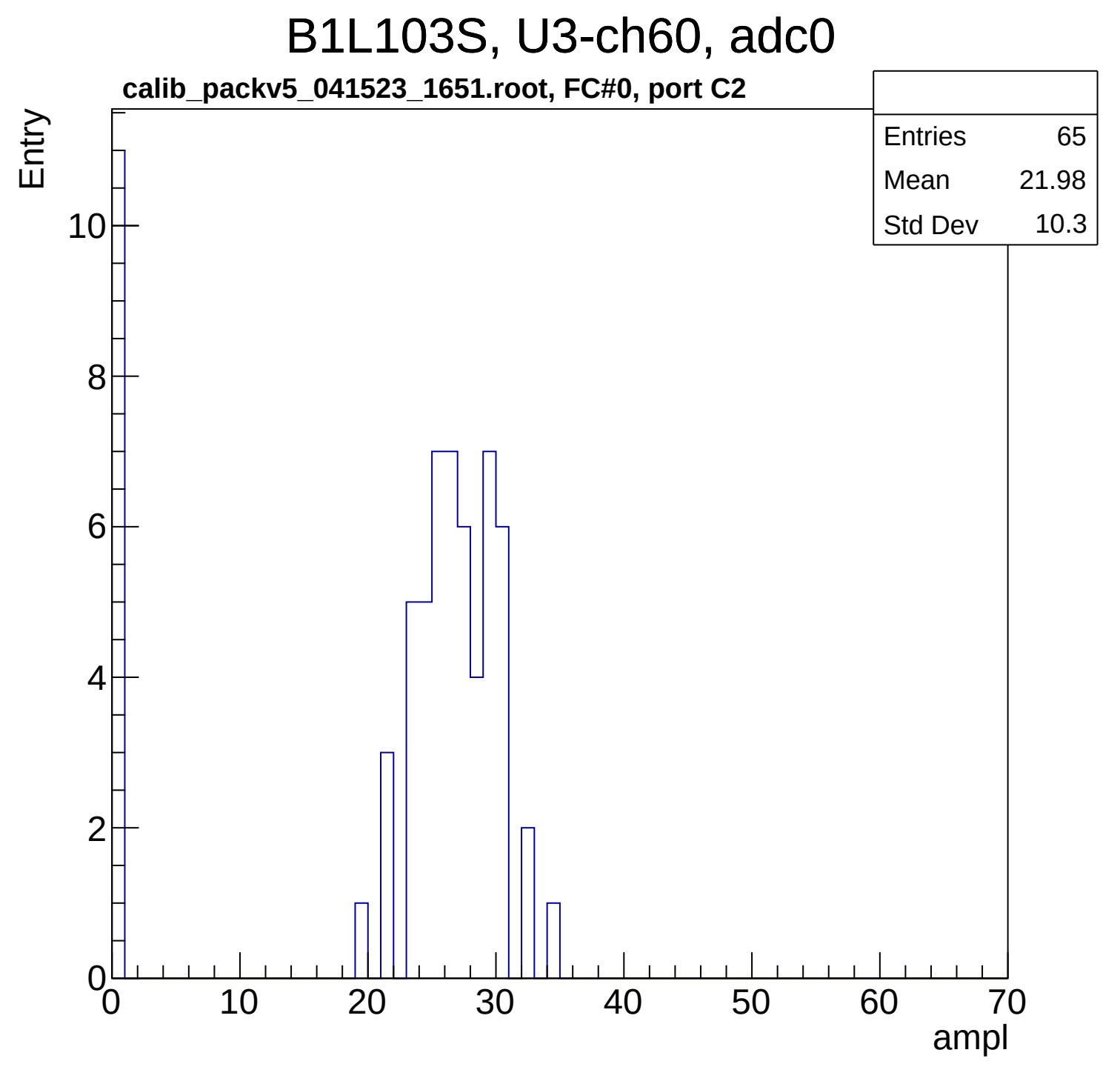
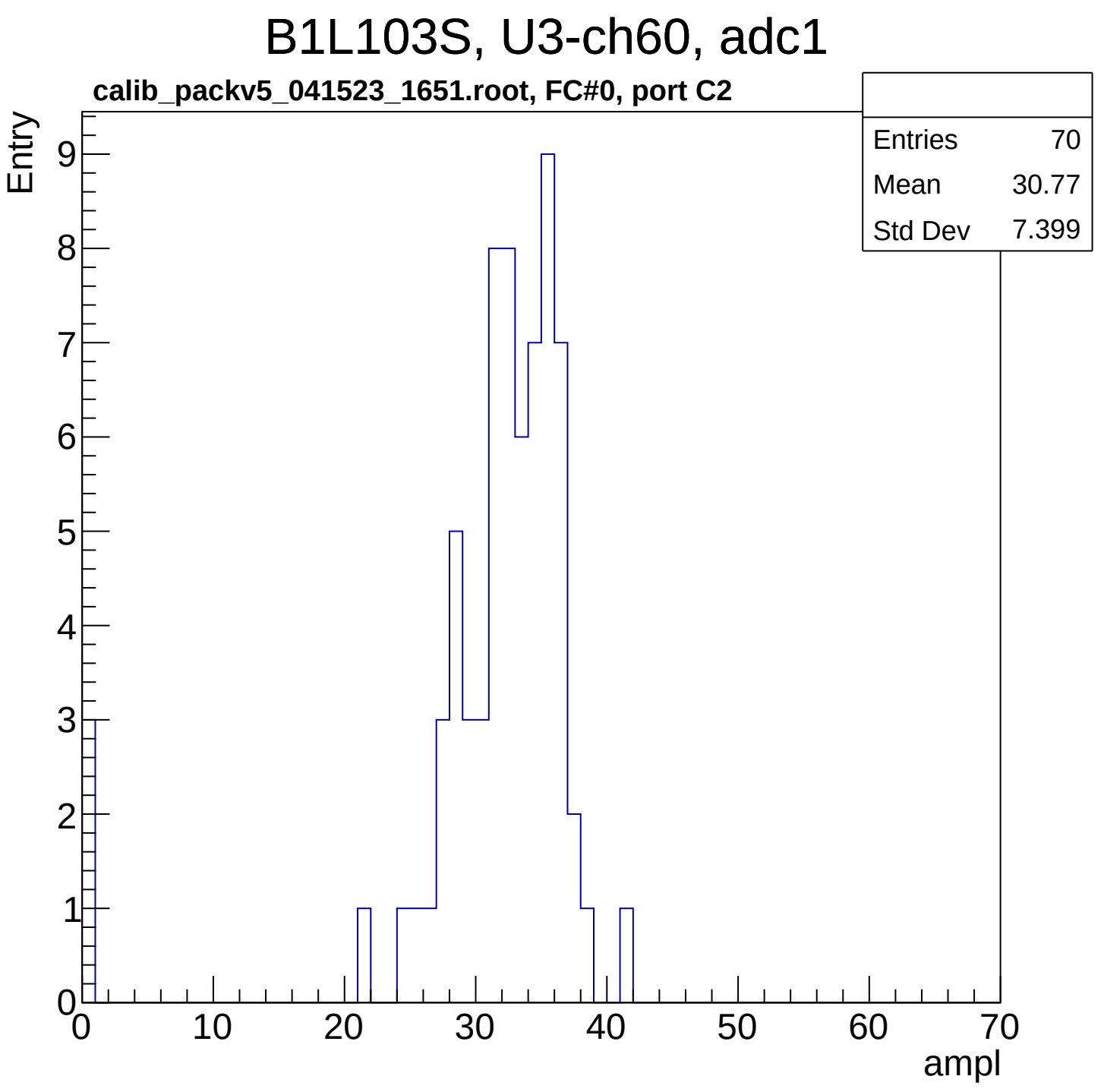
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch59, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 59.08
Std Dev 2.648
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch59, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 57.44
Std Dev 14.94
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch59, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch60, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 21.98
Std Dev 10.3
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch60, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 30.77
Std Dev 7.399
Entry
ampl
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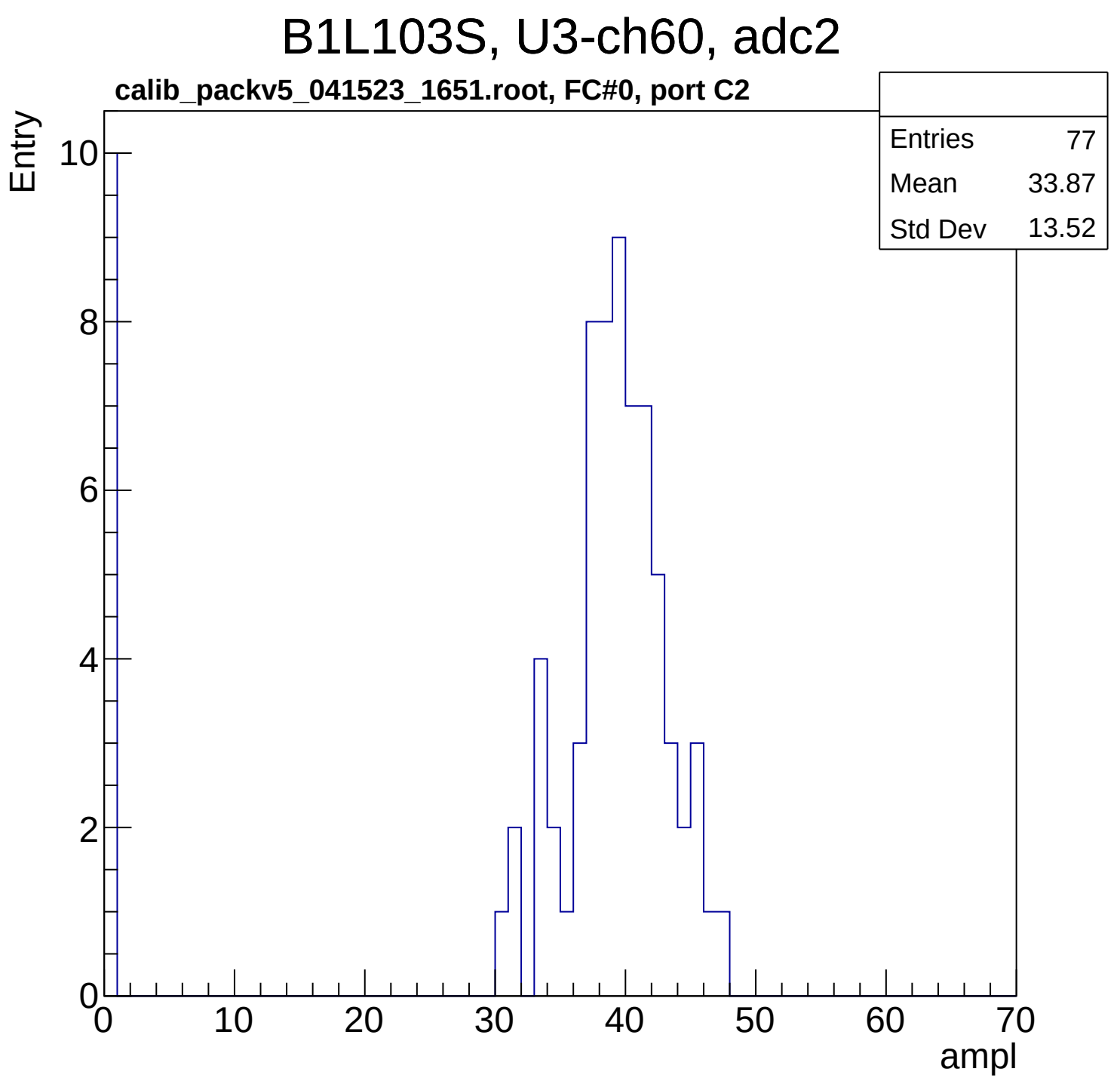
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch60, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 33.87
Std Dev 13.52
Entry
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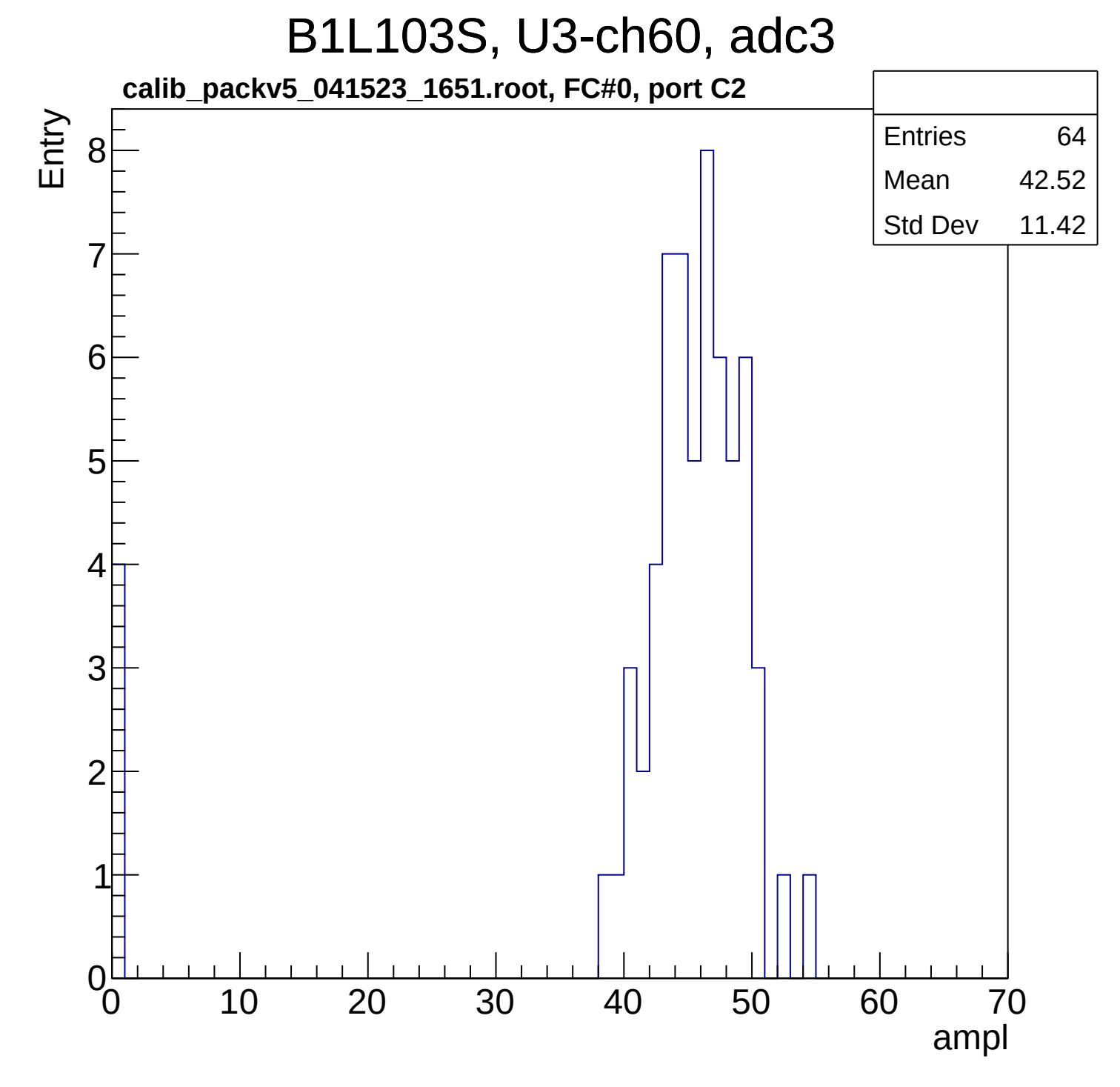
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch60, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 42.52
Std Dev 11.42
Entry
ampl
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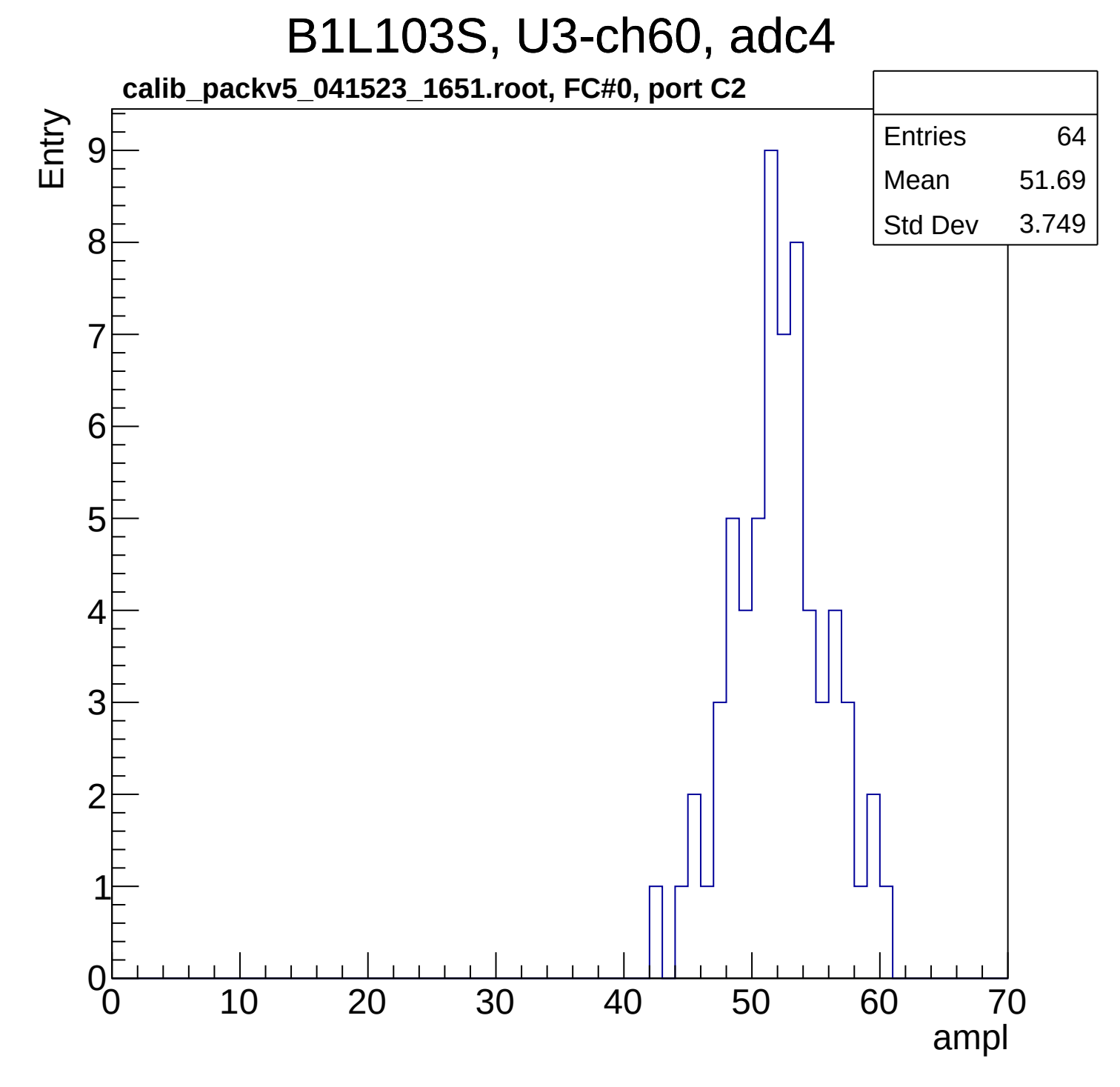
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch60, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 51.69
Std Dev 3.749
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
30
40
50
60
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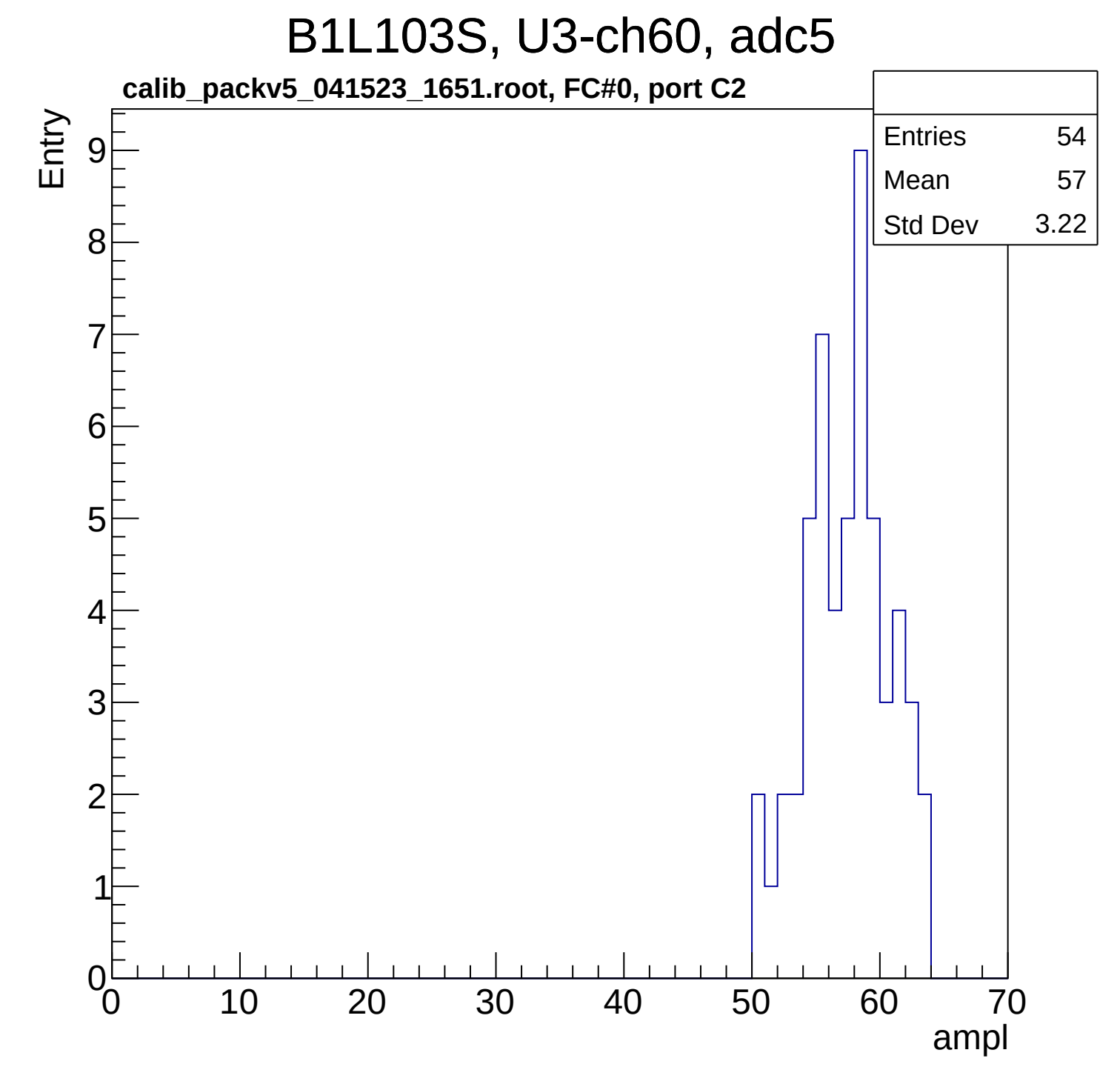
B1L103S, U3-ch60, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 57
Std Dev 3.22
Entry
ampl
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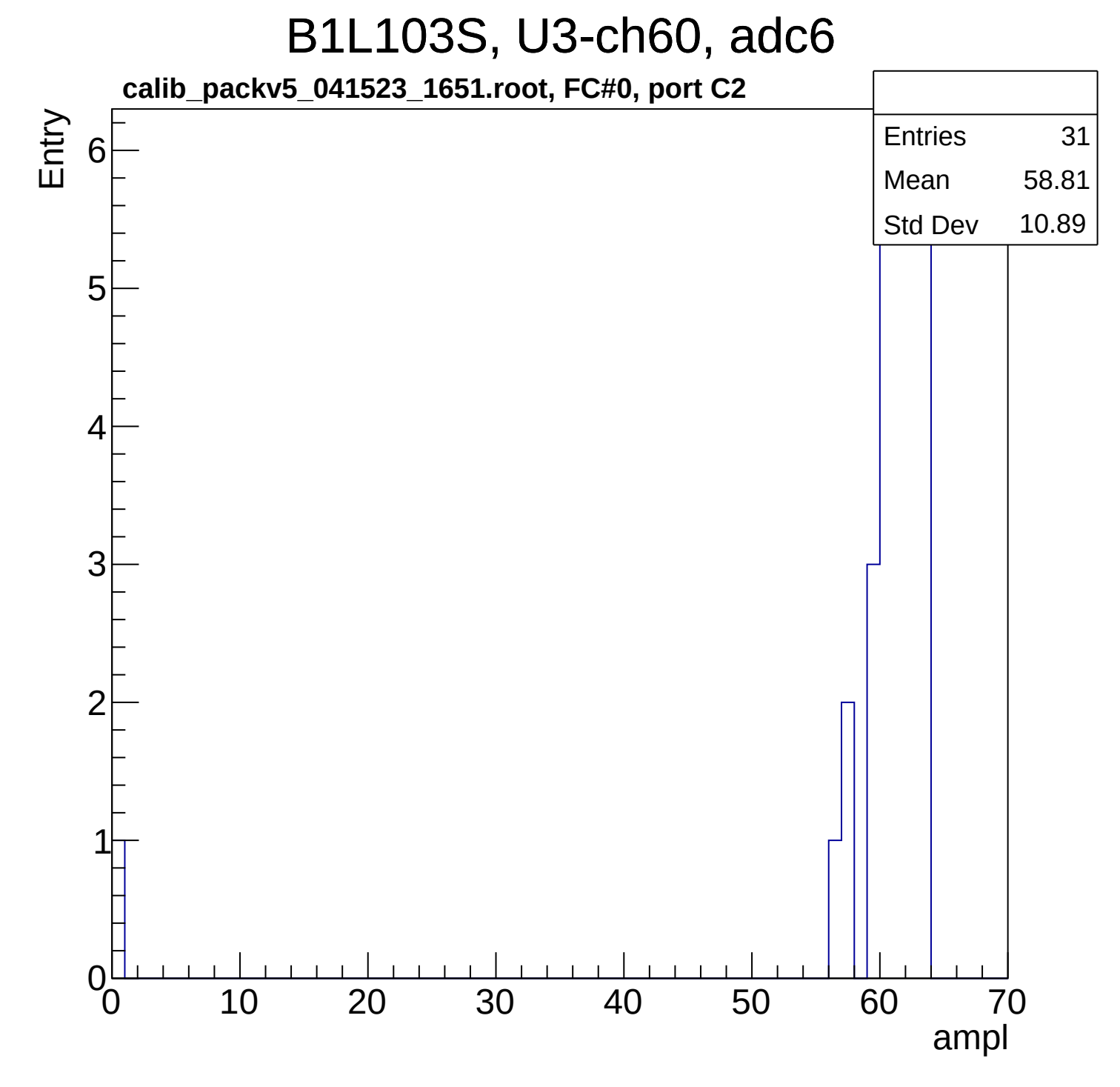
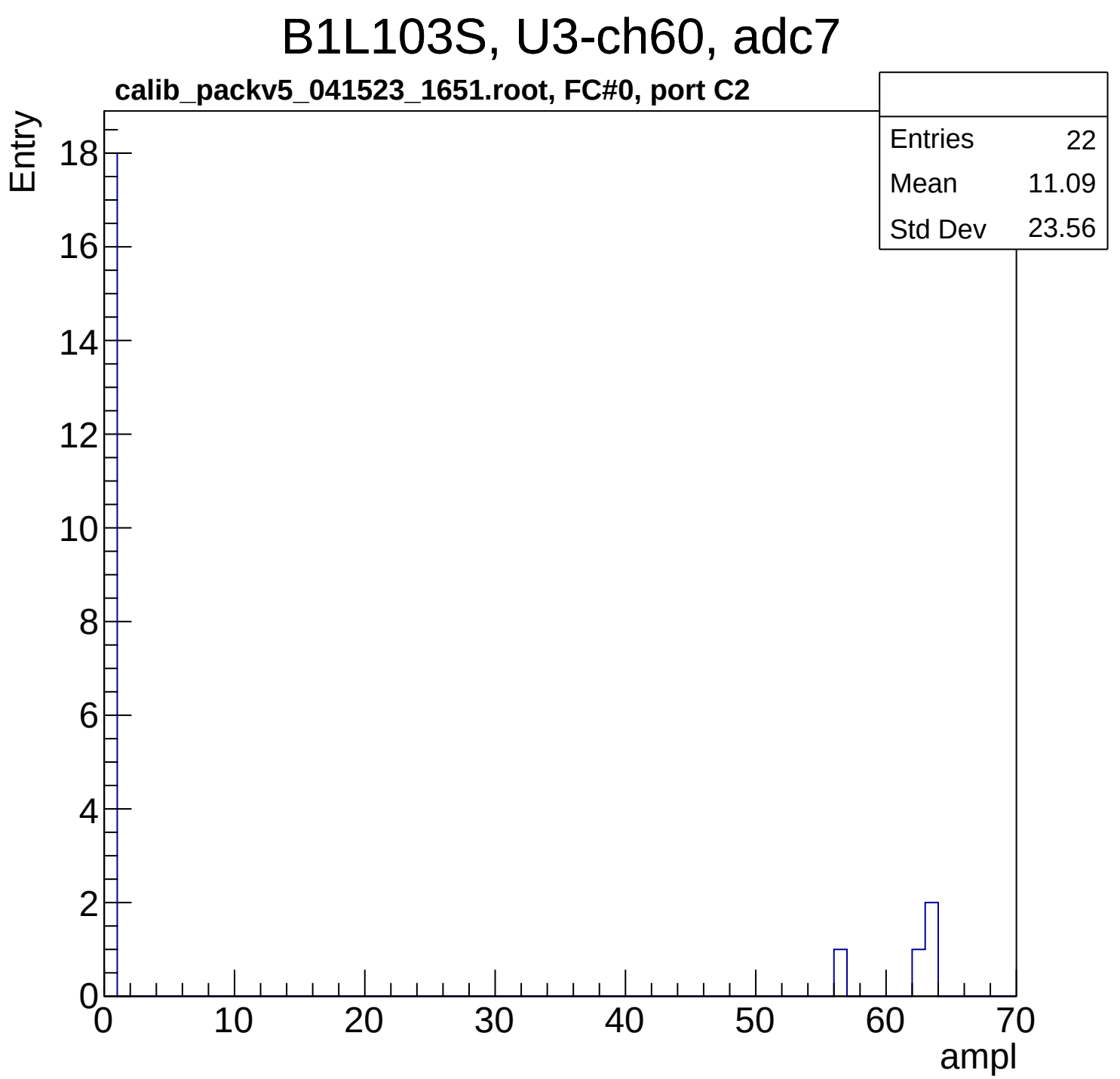
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch60, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 58.81
Std Dev 10.89
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U3-ch60, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 11.09
Std Dev 23.56
Entry
0
2
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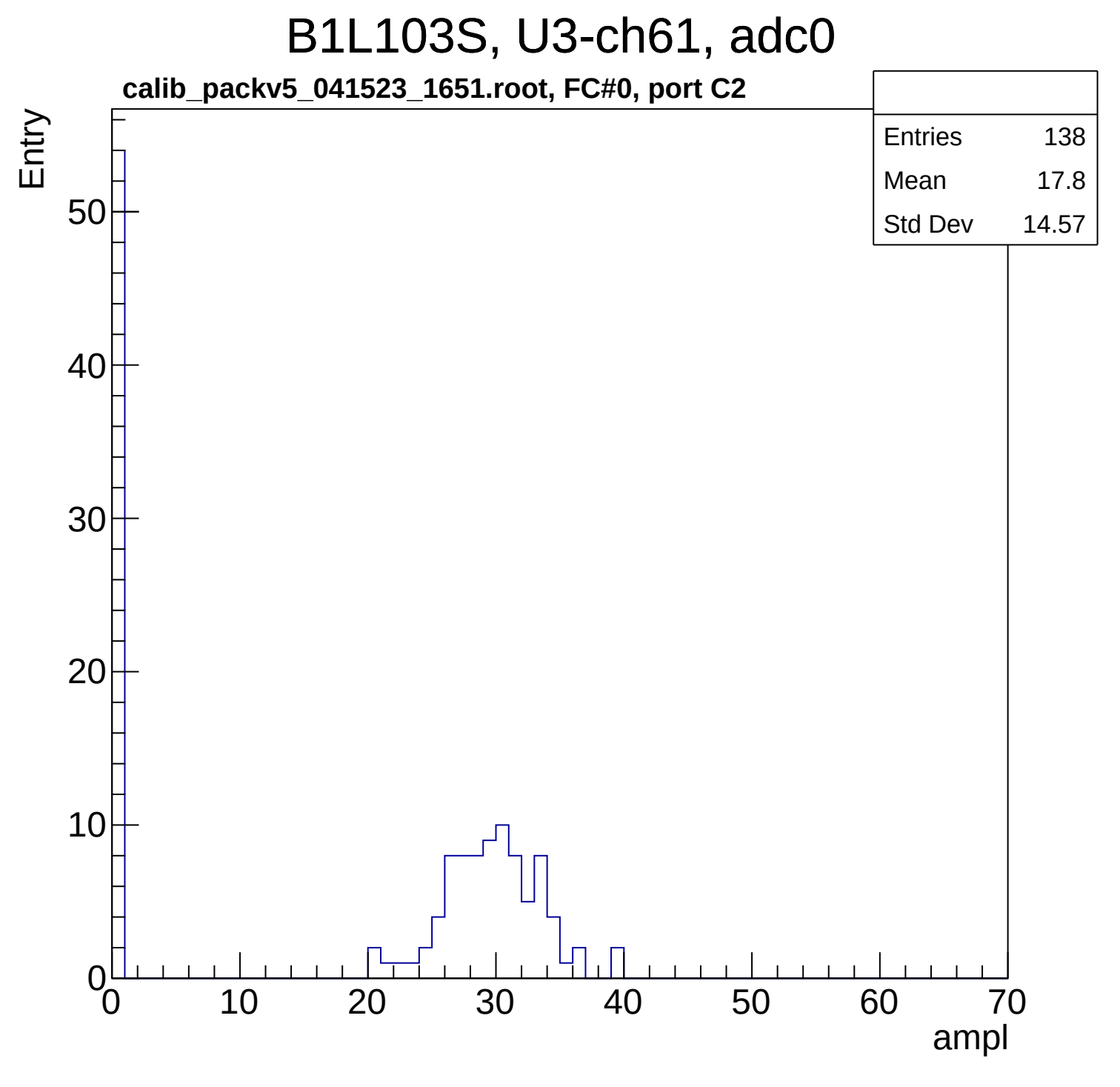
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch61, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 138
Mean 17.8
Std Dev 14.57
Entry
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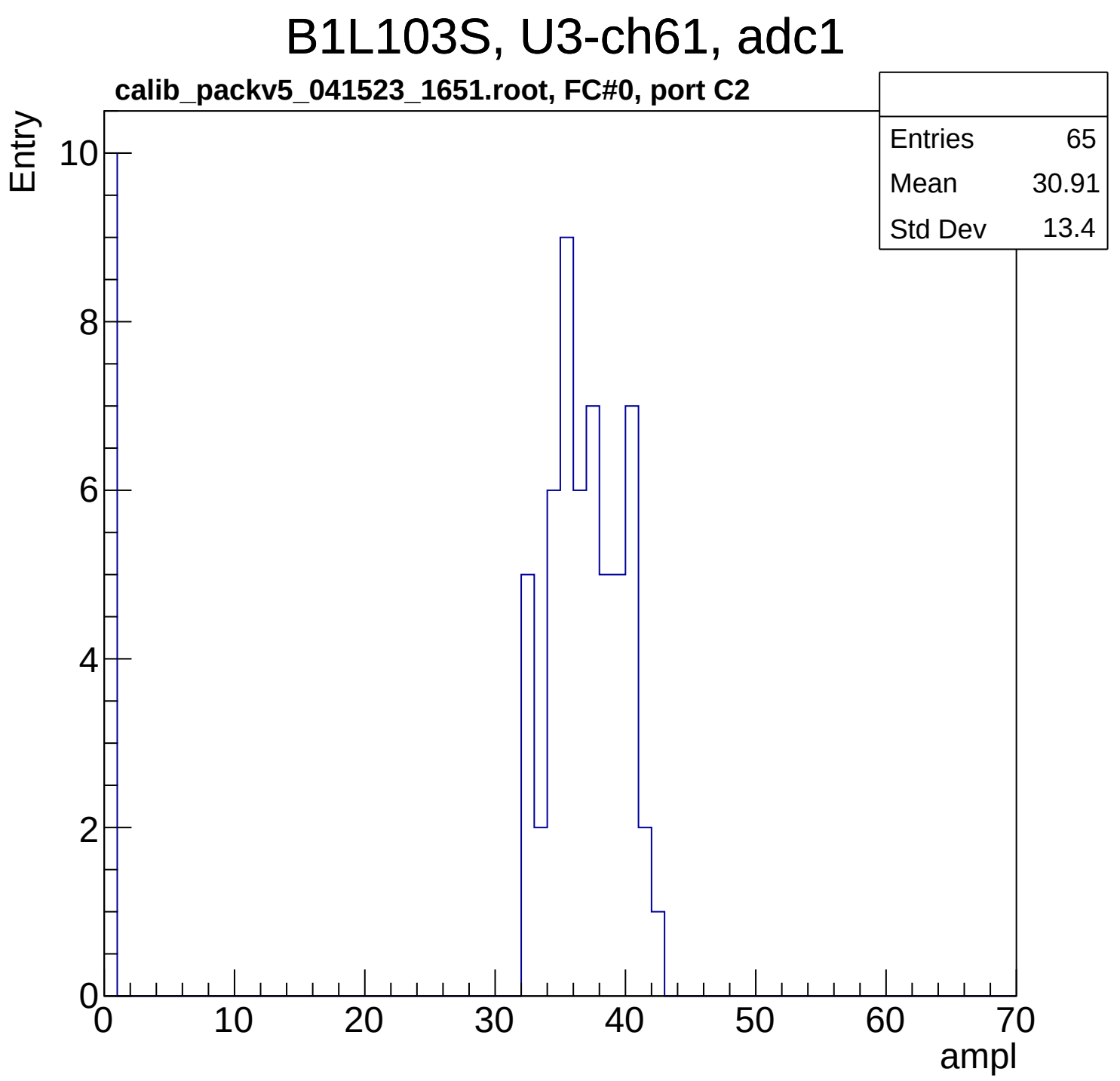
30
40
50
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch61, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 30.91
Std Dev 13.4
Entry
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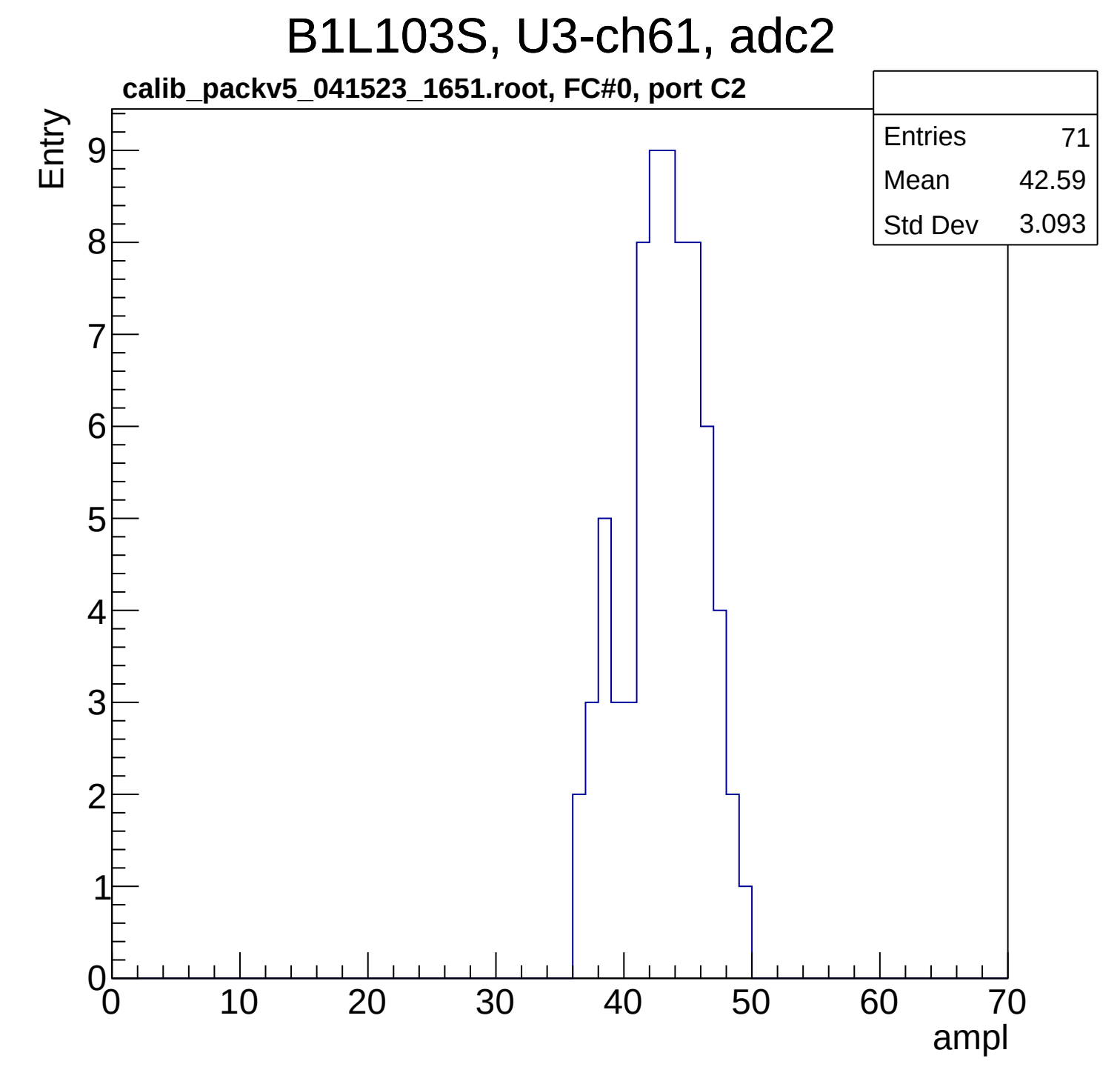
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch61, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 42.59
Std Dev 3.093
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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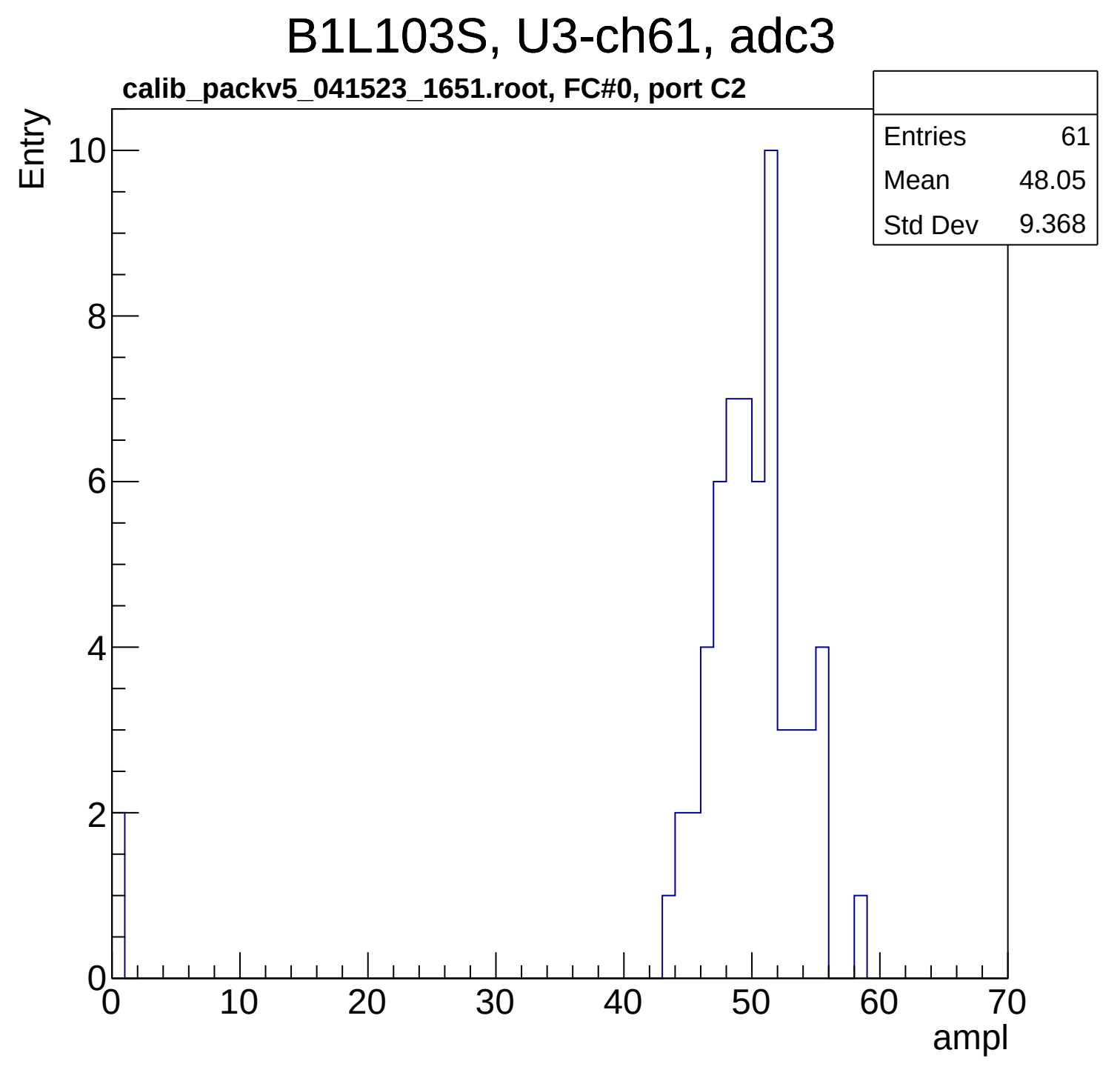
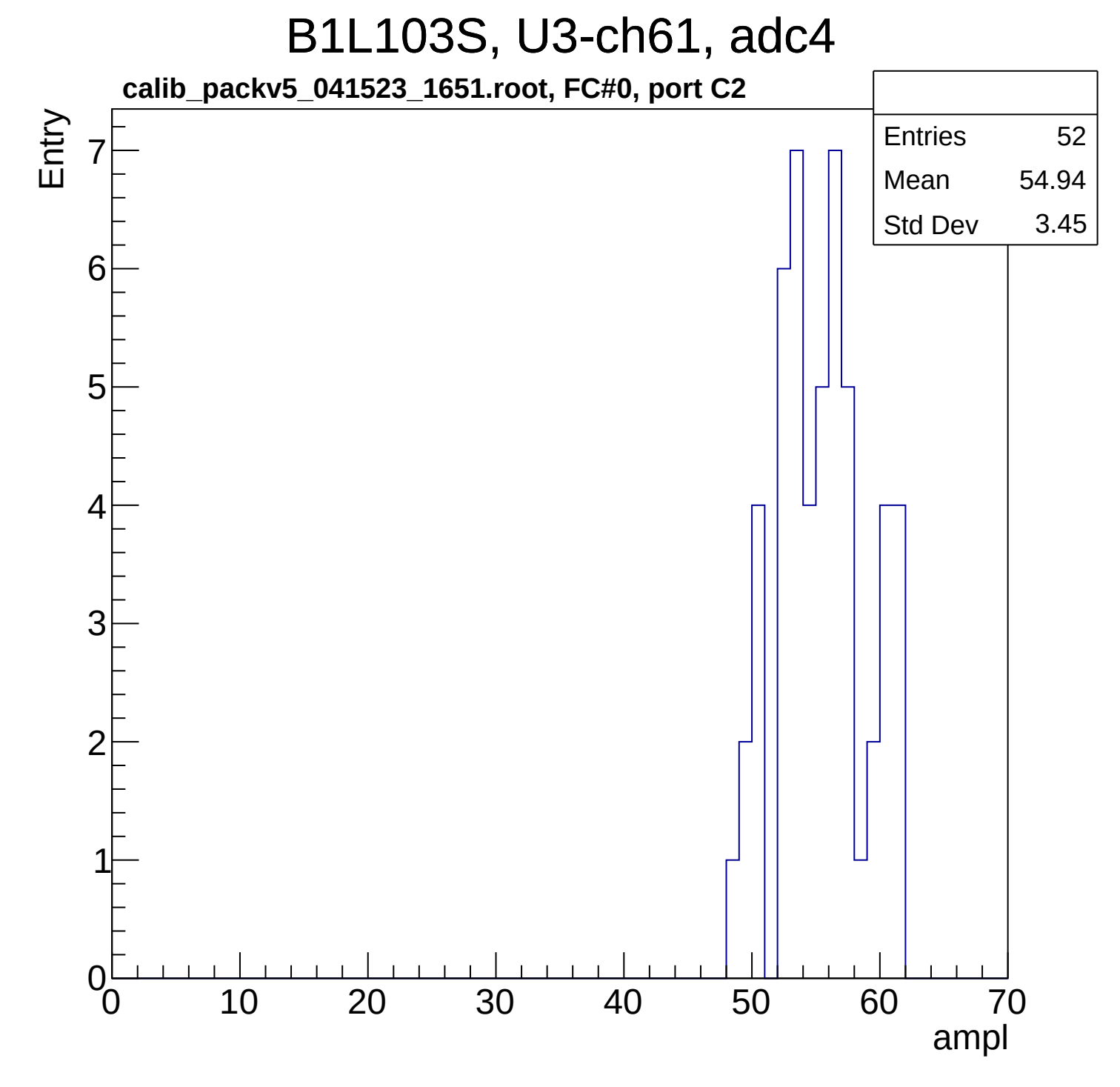
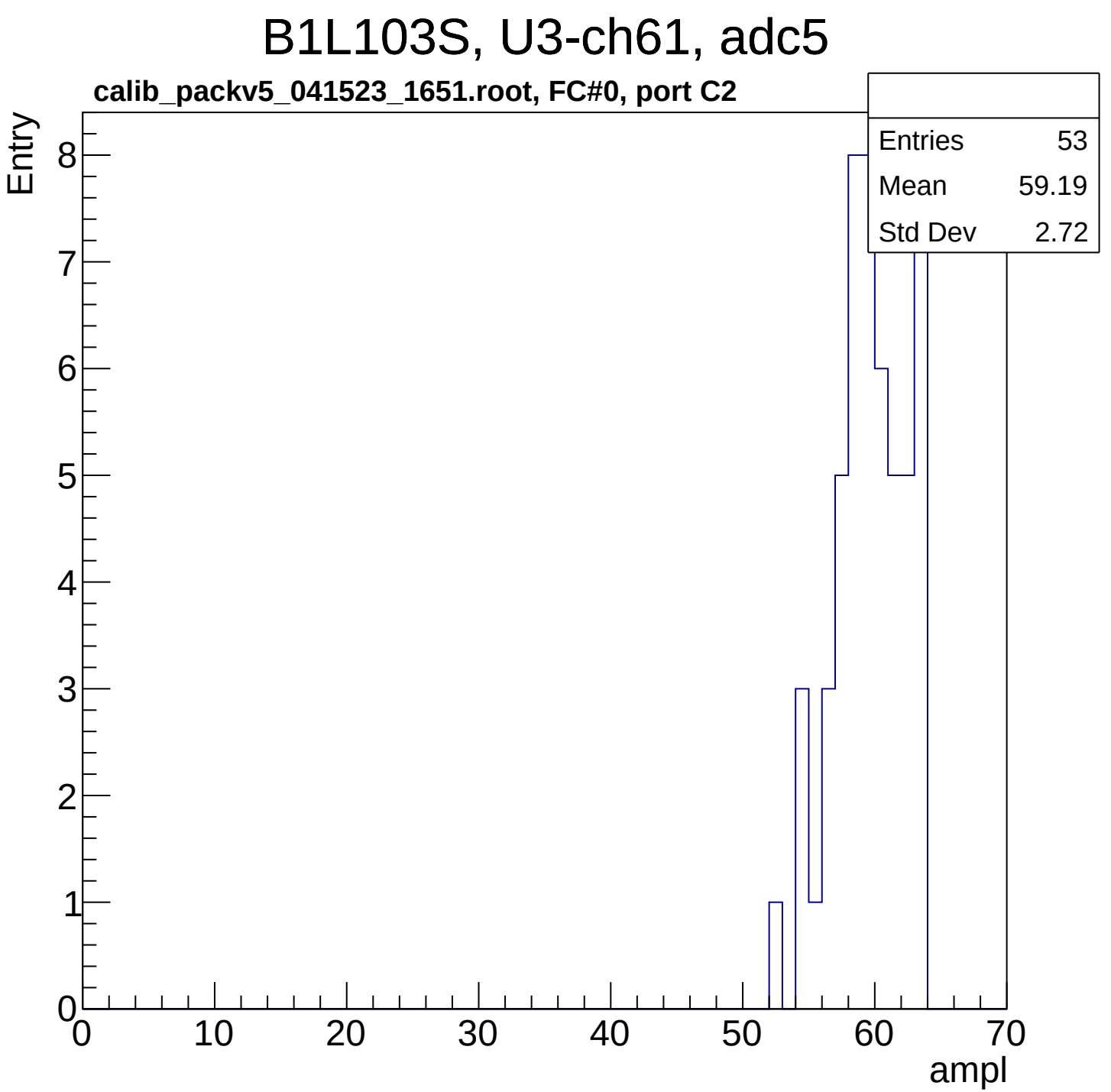
60
70


B1L103S, U3-ch61, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 48.05
Std Dev 9.368
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U3-ch61, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 54.94
Std Dev 3.45
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch61, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 59.19
Std Dev 2.72
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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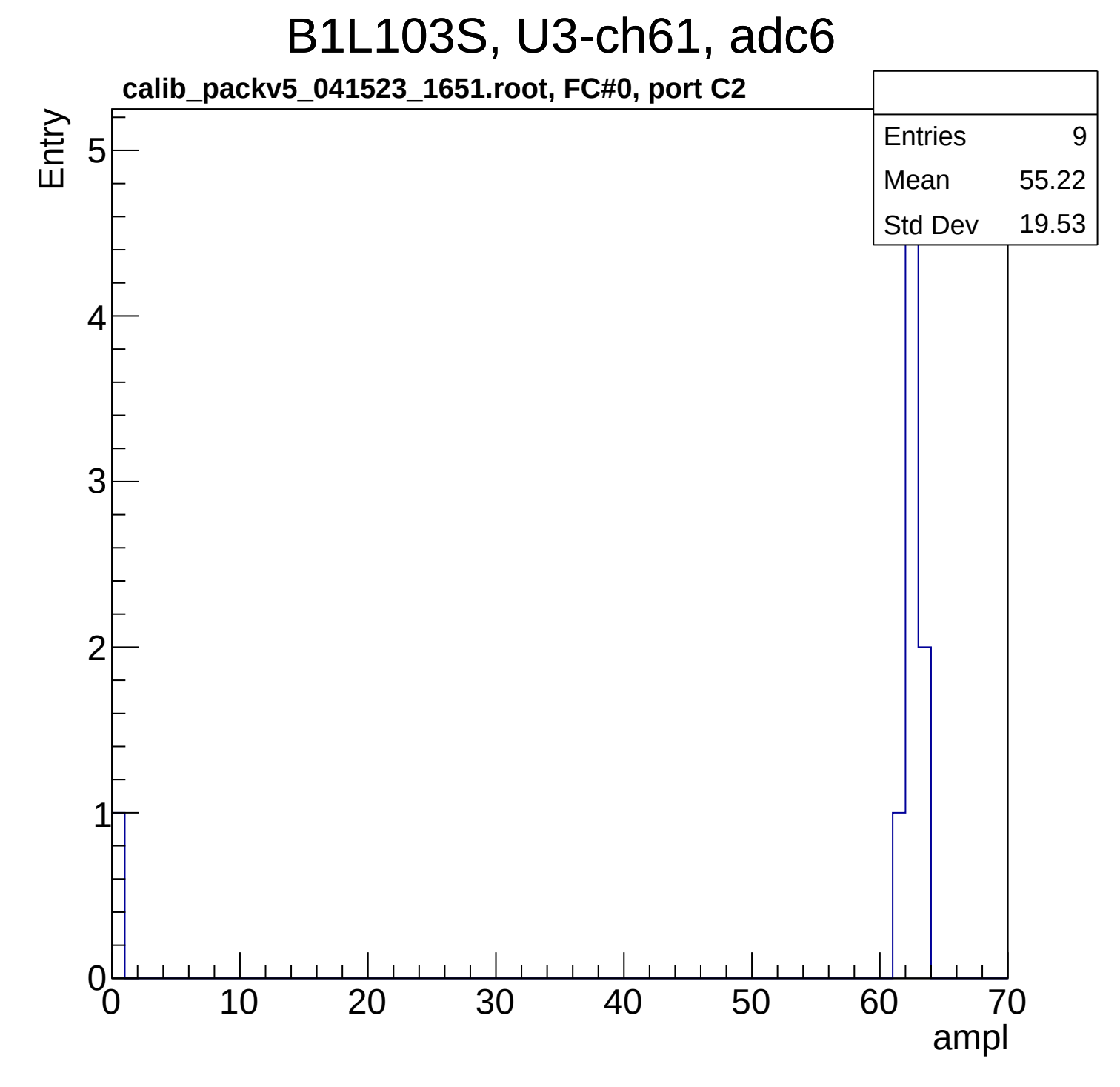
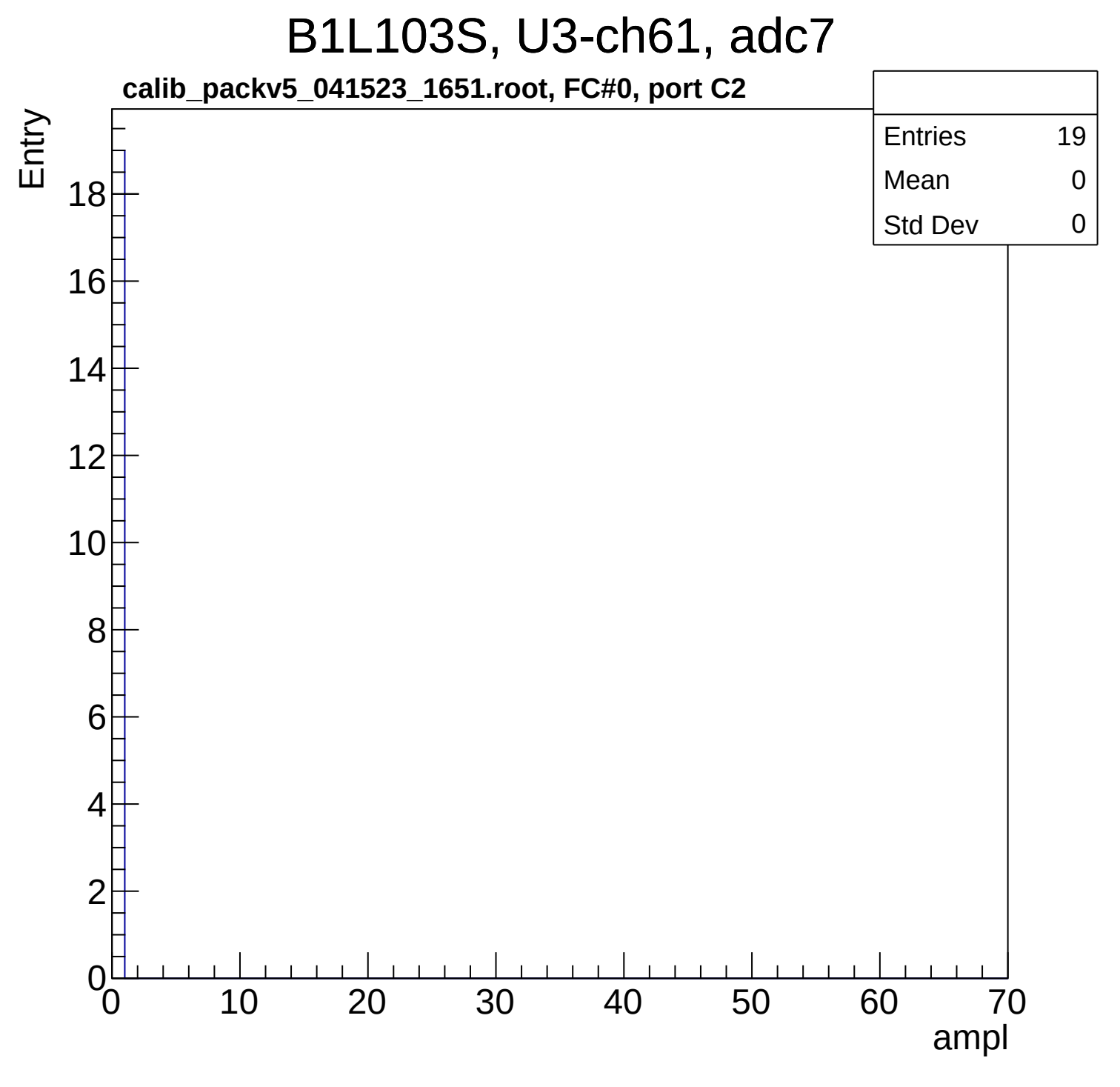
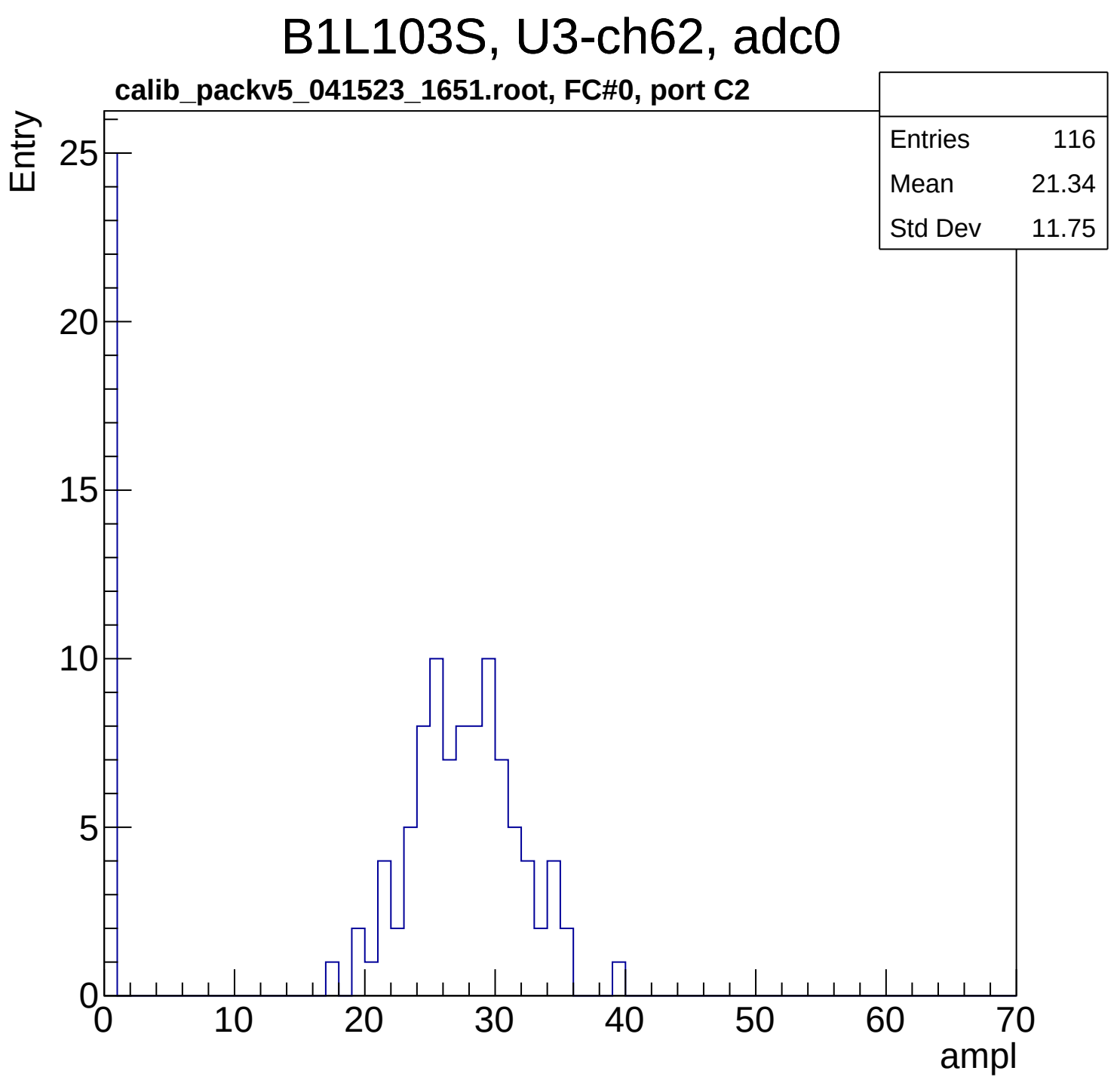
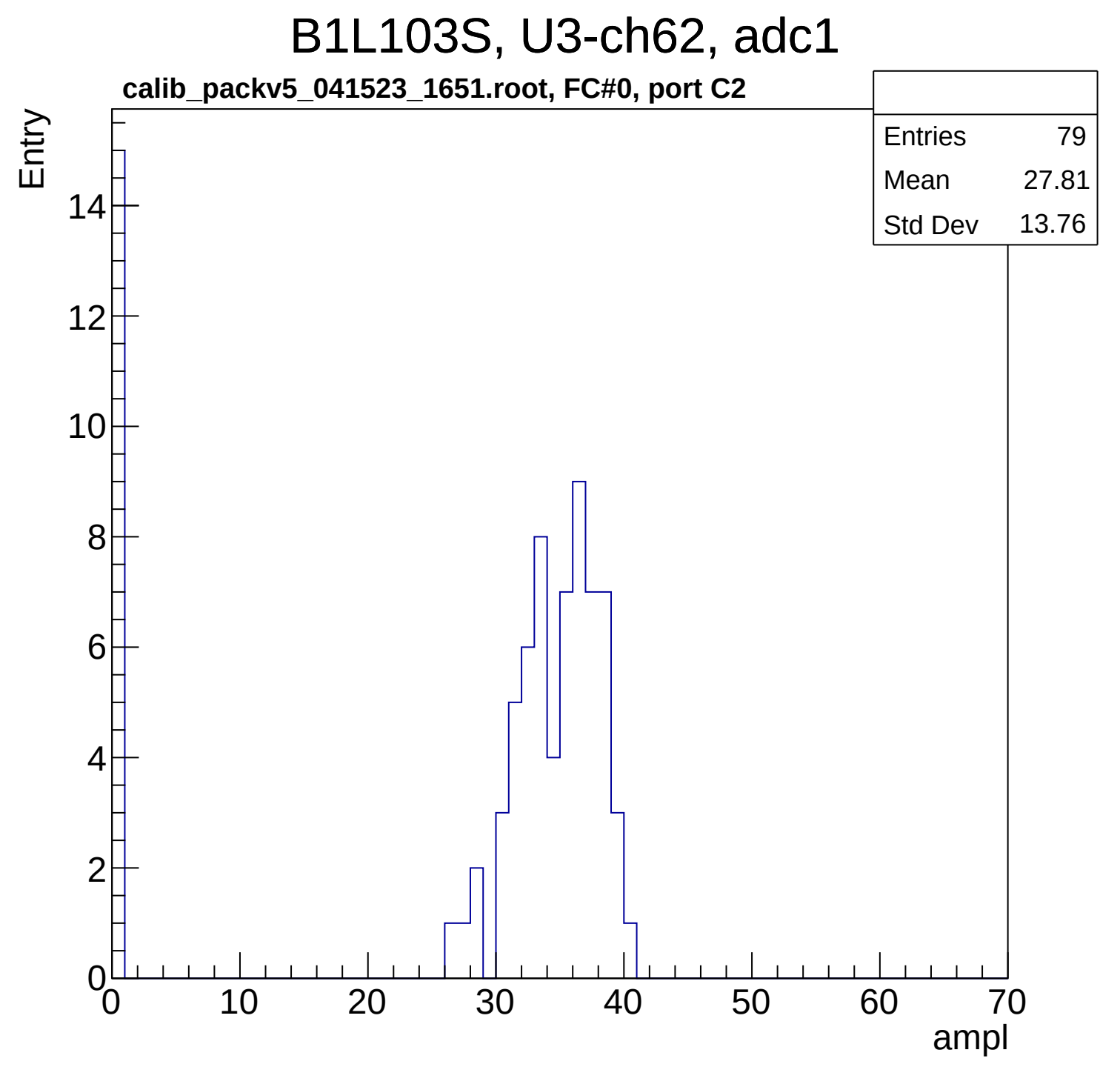
40
50
60
70


B1L103S, U3-ch61, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 55.22
Std Dev 19.53
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U3-ch61, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch62, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 116
Mean 21.34
Std Dev 11.75
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch62, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 27.81
Std Dev 13.76
Entry
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2
4
6
8
10
12
14
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10
20
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50
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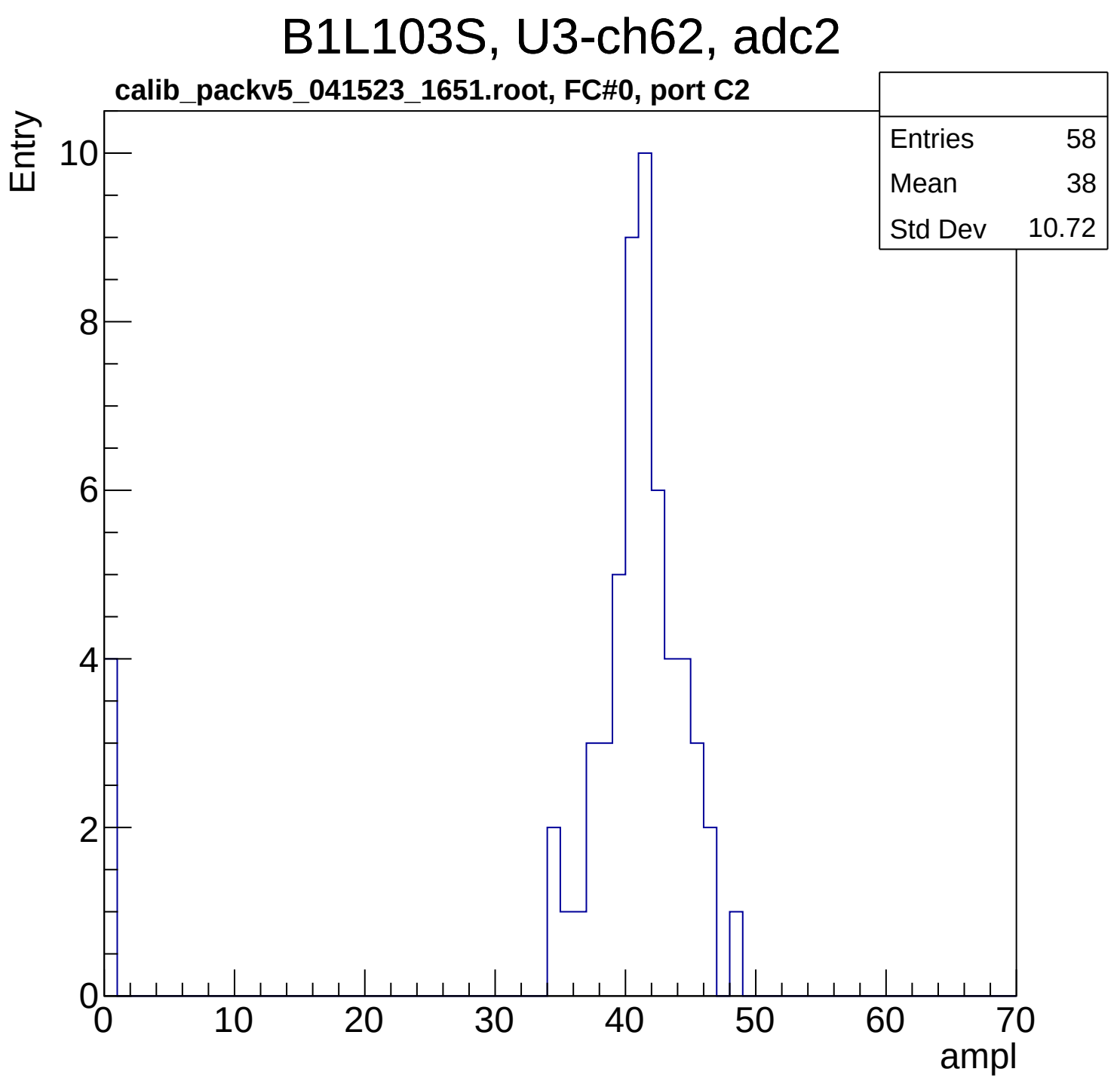
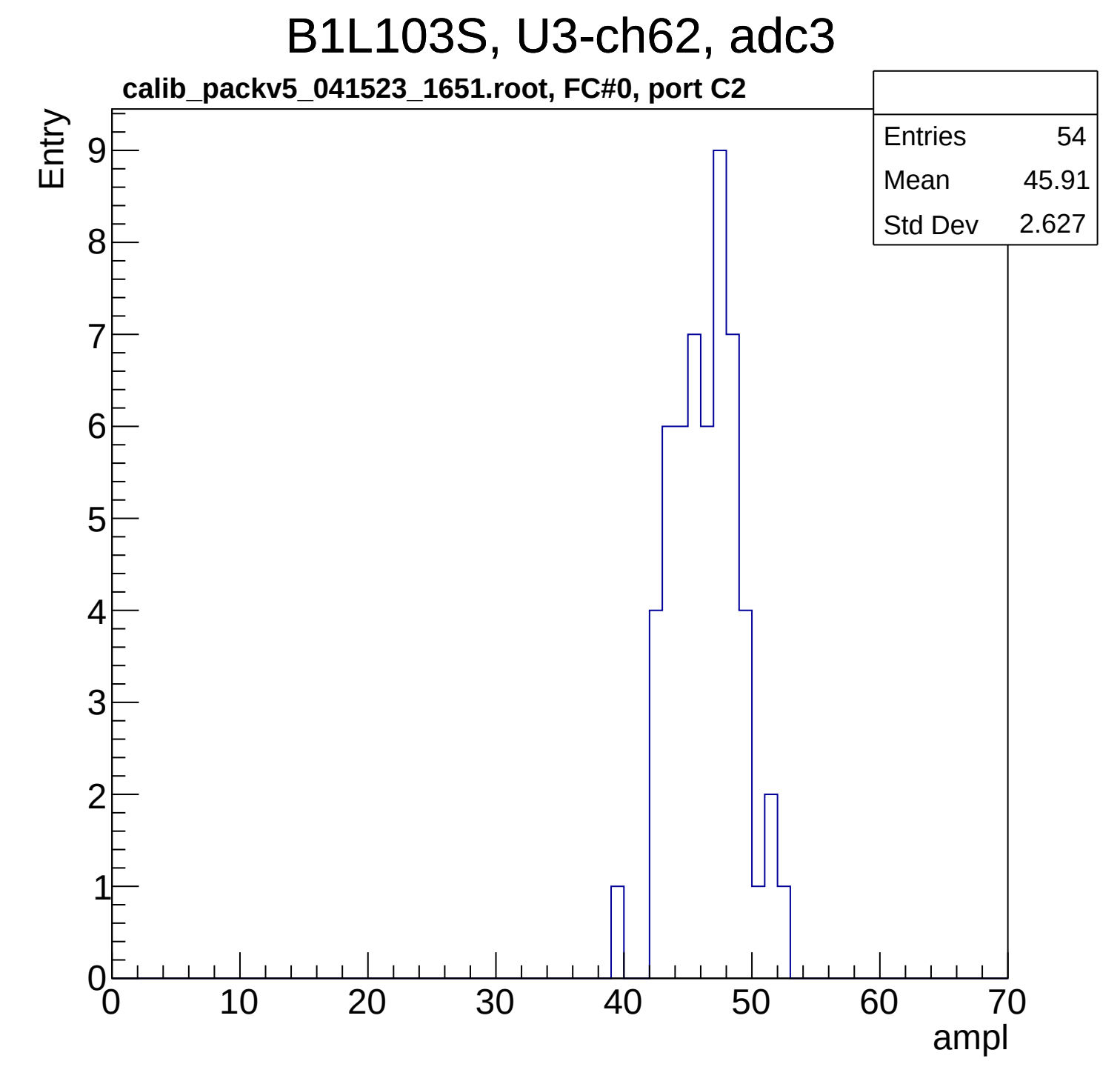
70
ampl


B1L103S, U3-ch62, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 38
Std Dev 10.72
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch62, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 45.91
Std Dev 2.627
Entry
ampl
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3
4
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6
7
8
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0
10
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60
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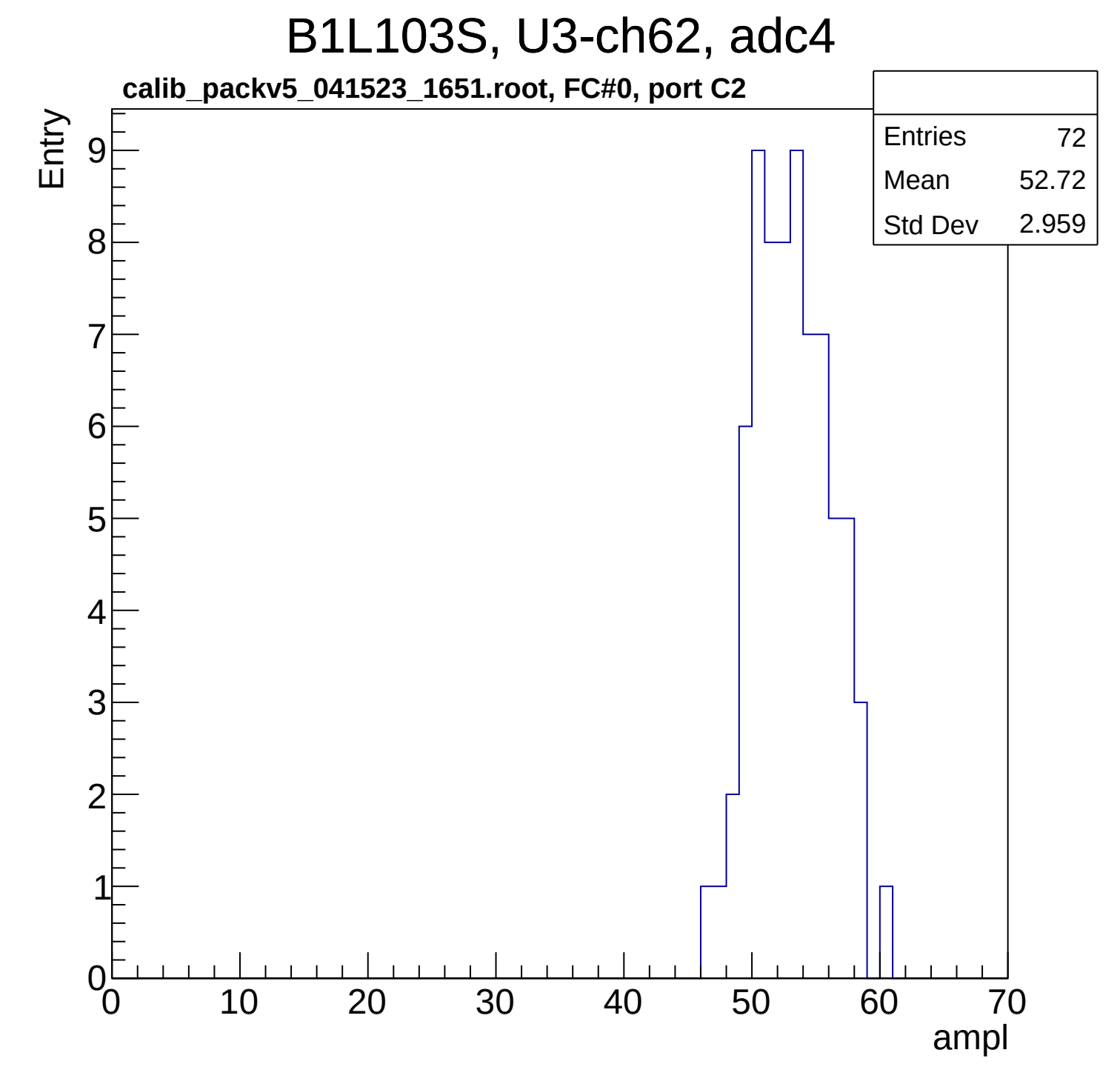
B1L103S, U3-ch62, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 52.72
Std Dev 2.959
Entry
ampl
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2
3
4
5
6
7
8
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0
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60
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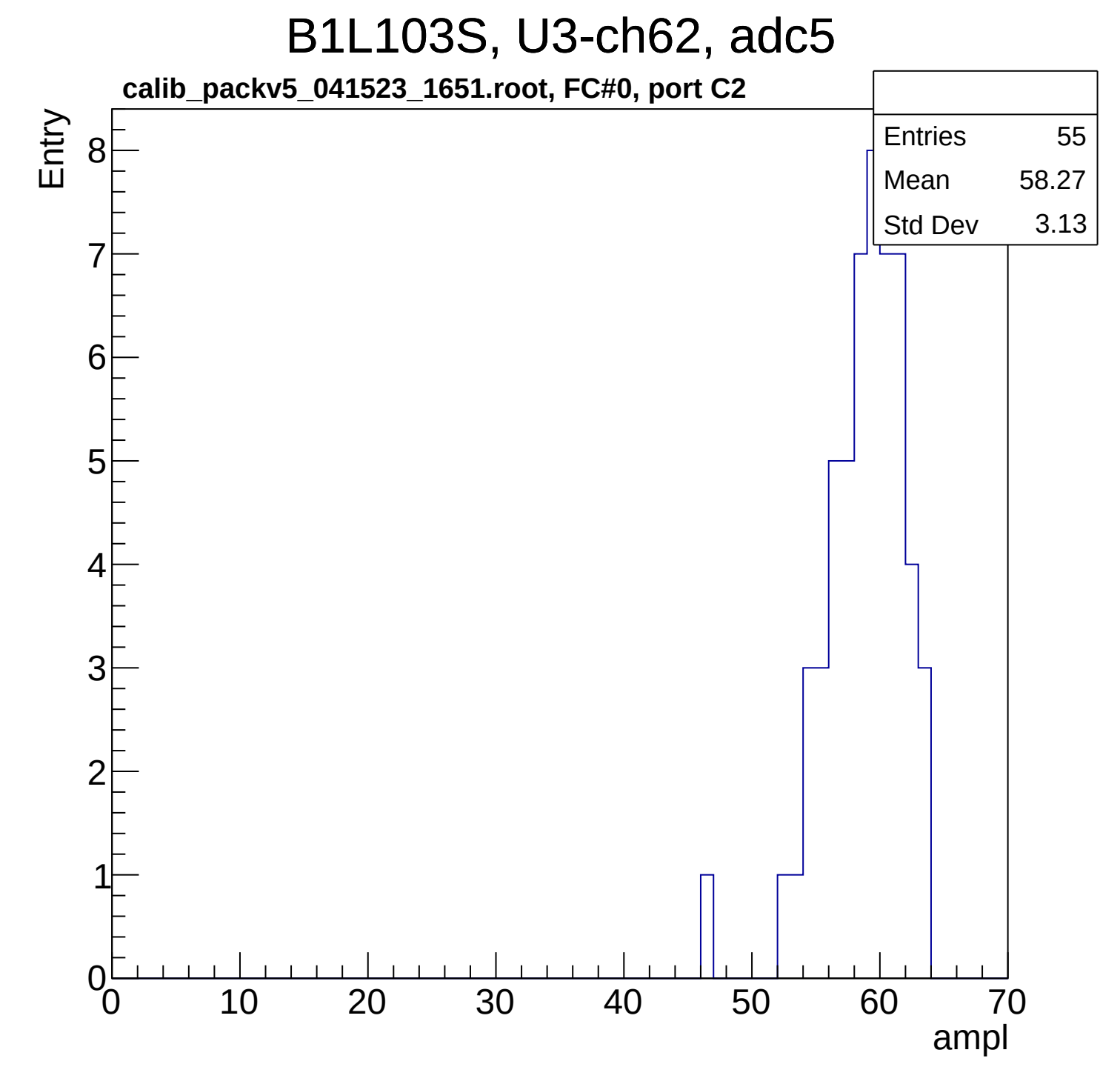
B1L103S, U3-ch62, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 58.27
Std Dev 3.13
Entry
ampl
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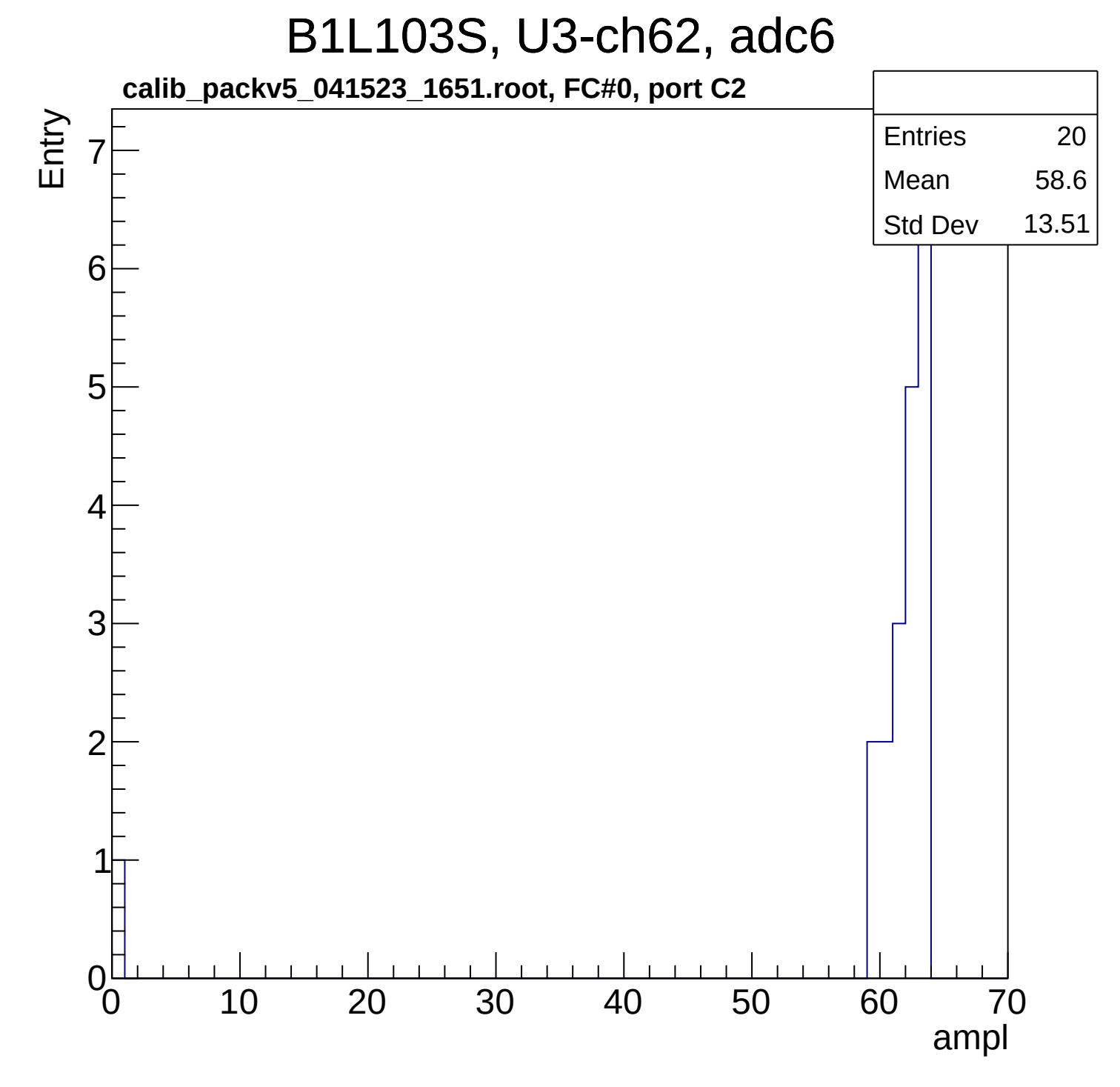
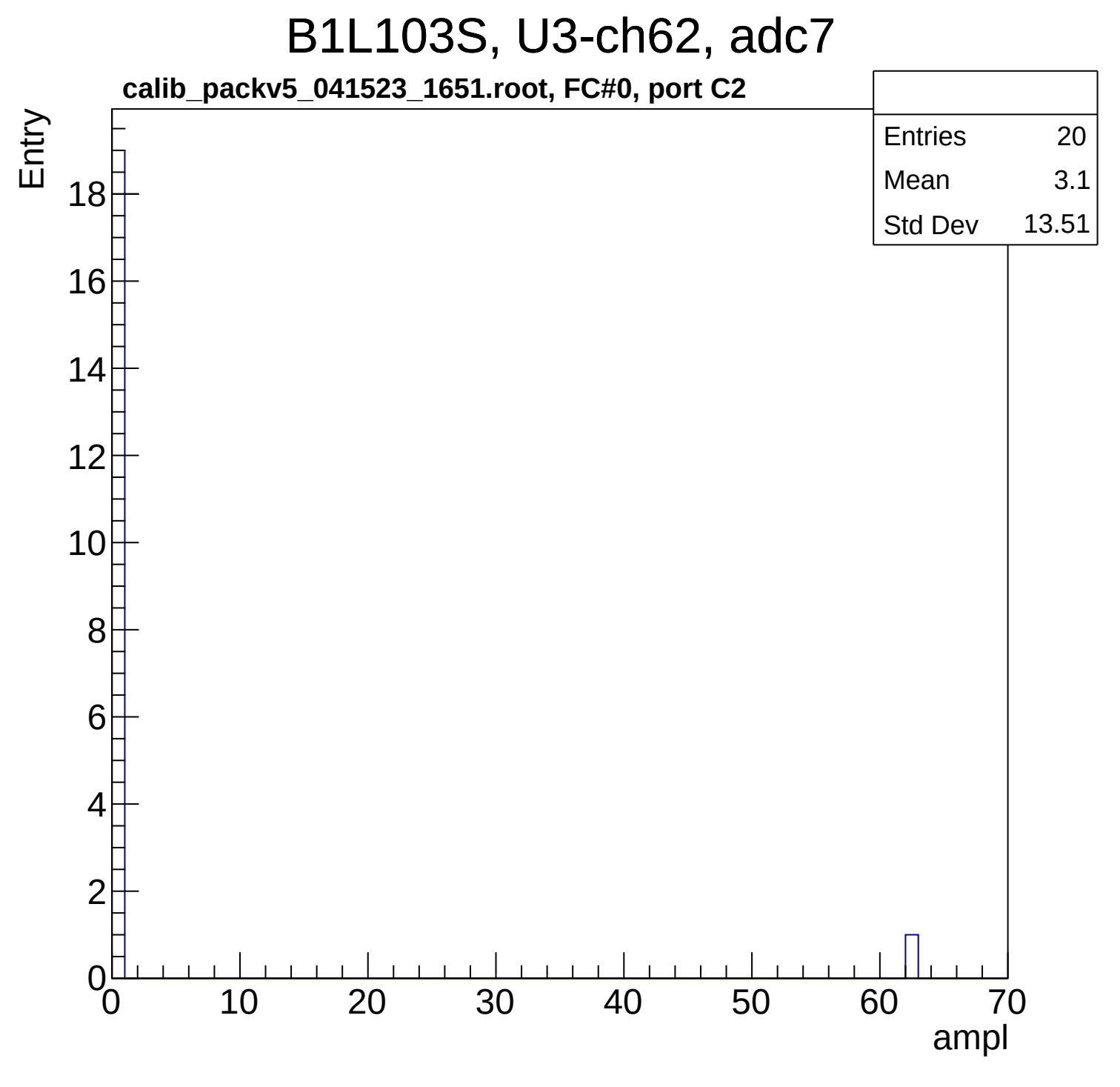
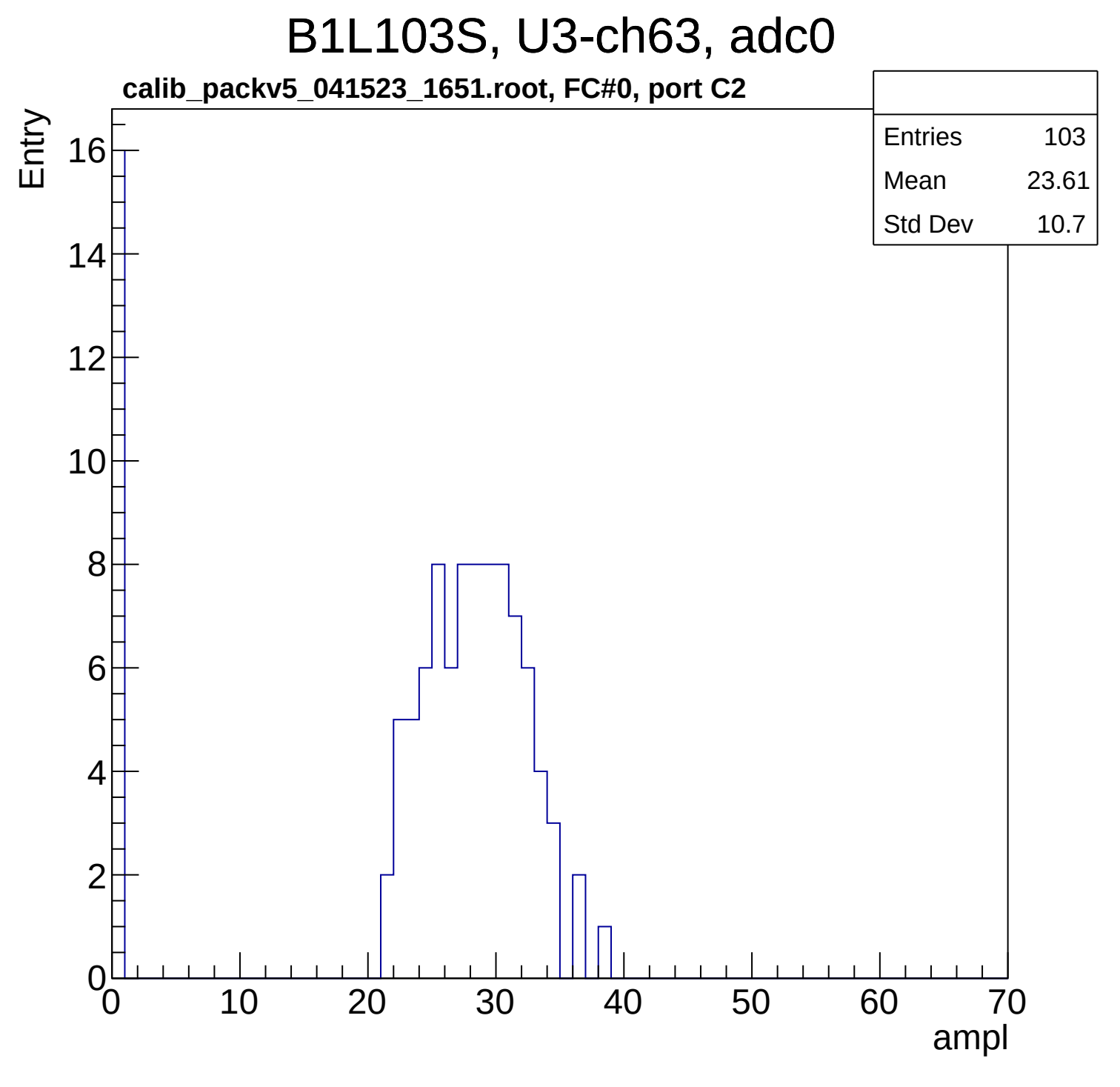
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch62, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 58.6
Std Dev 13.51
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch62, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch63, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 103
Mean 23.61
Std Dev 10.7
Entry
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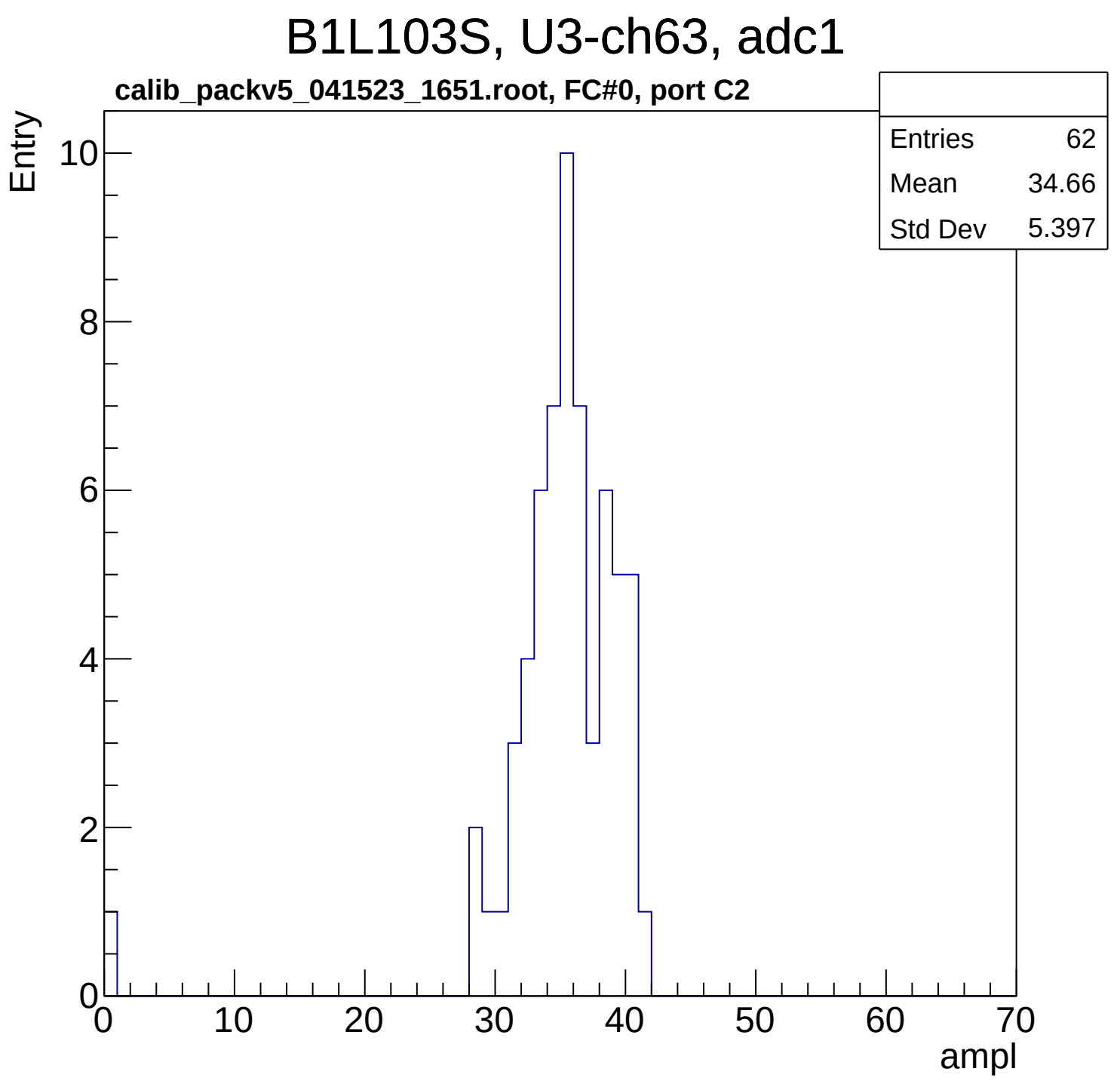
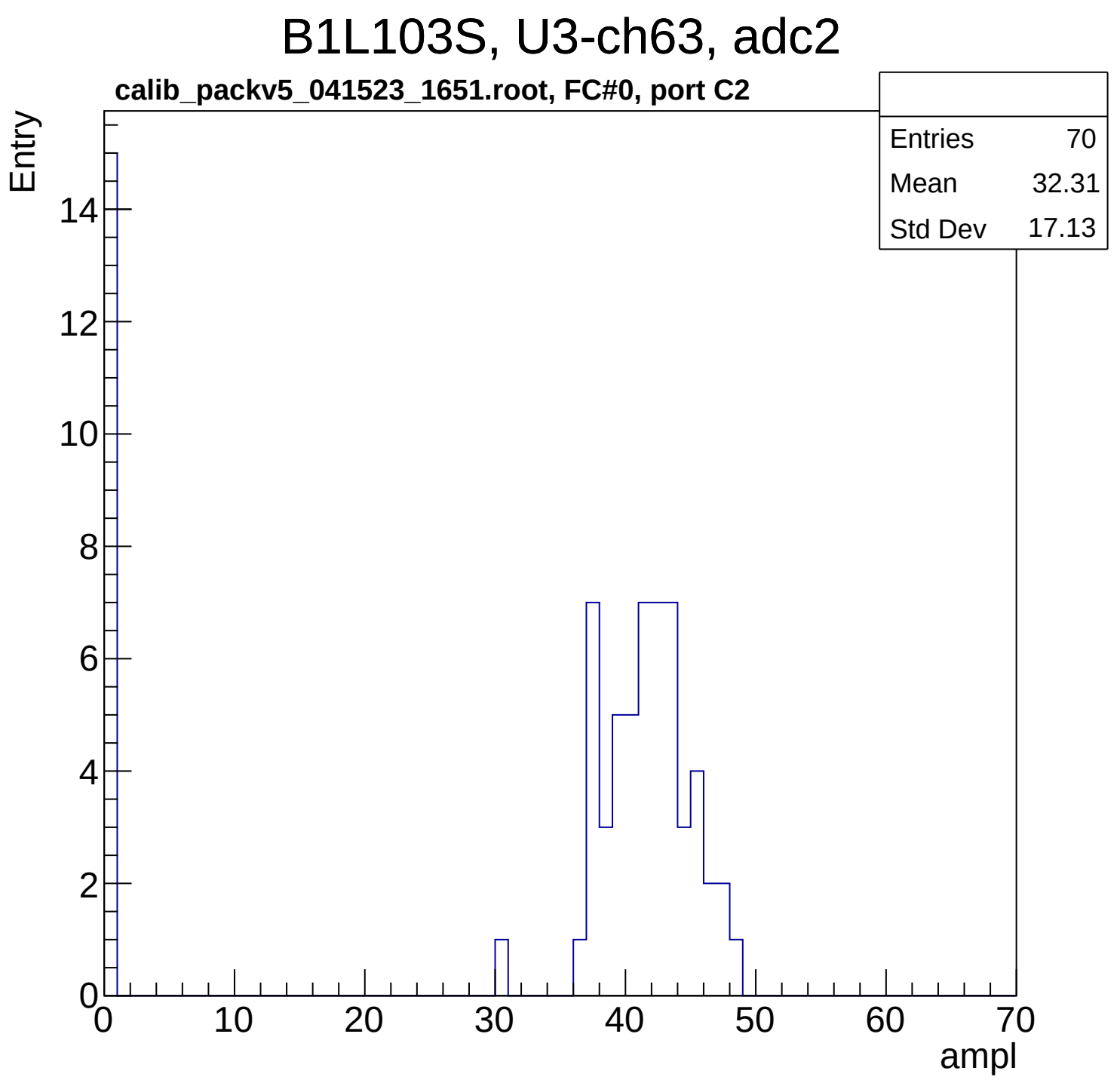
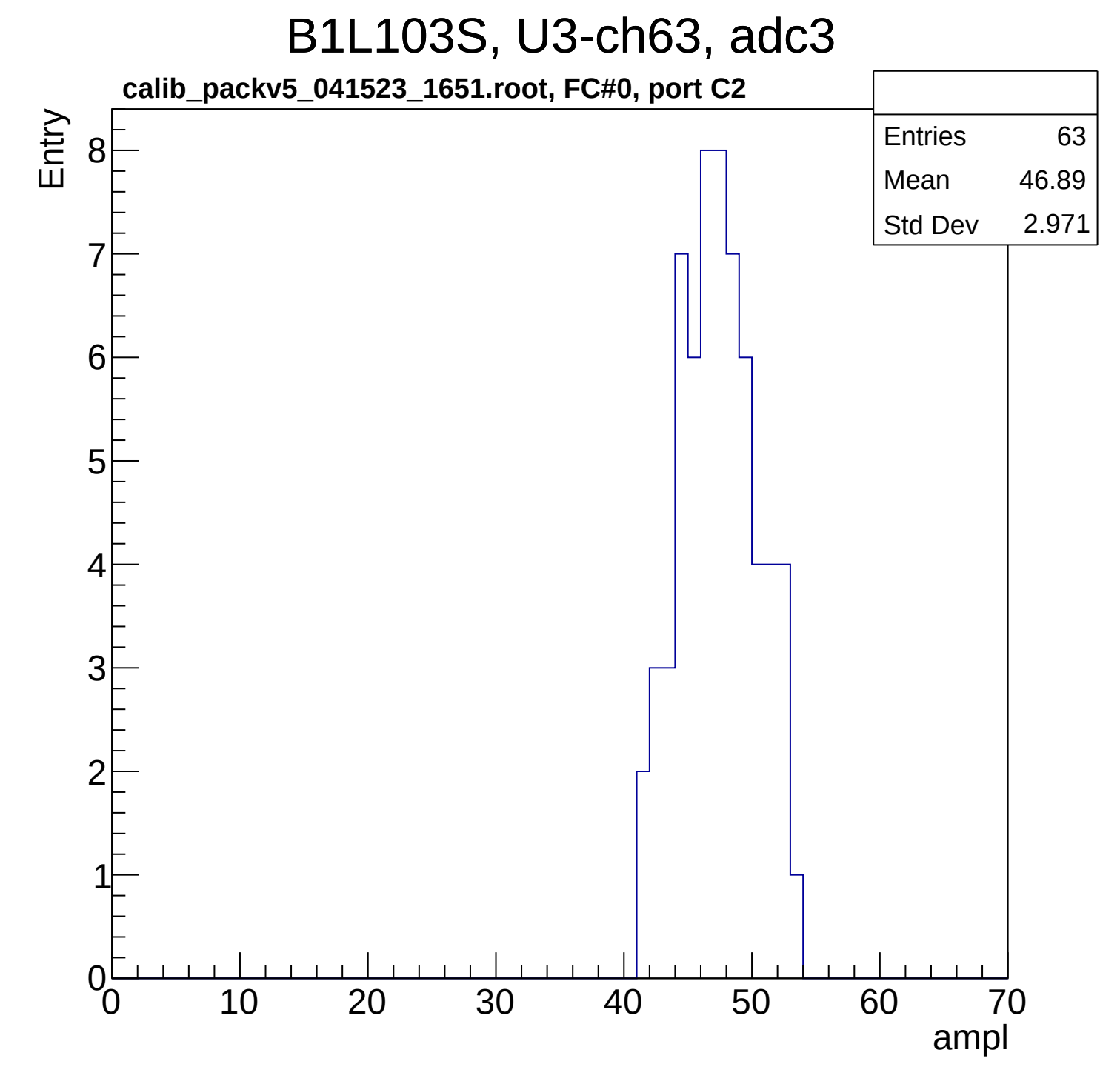
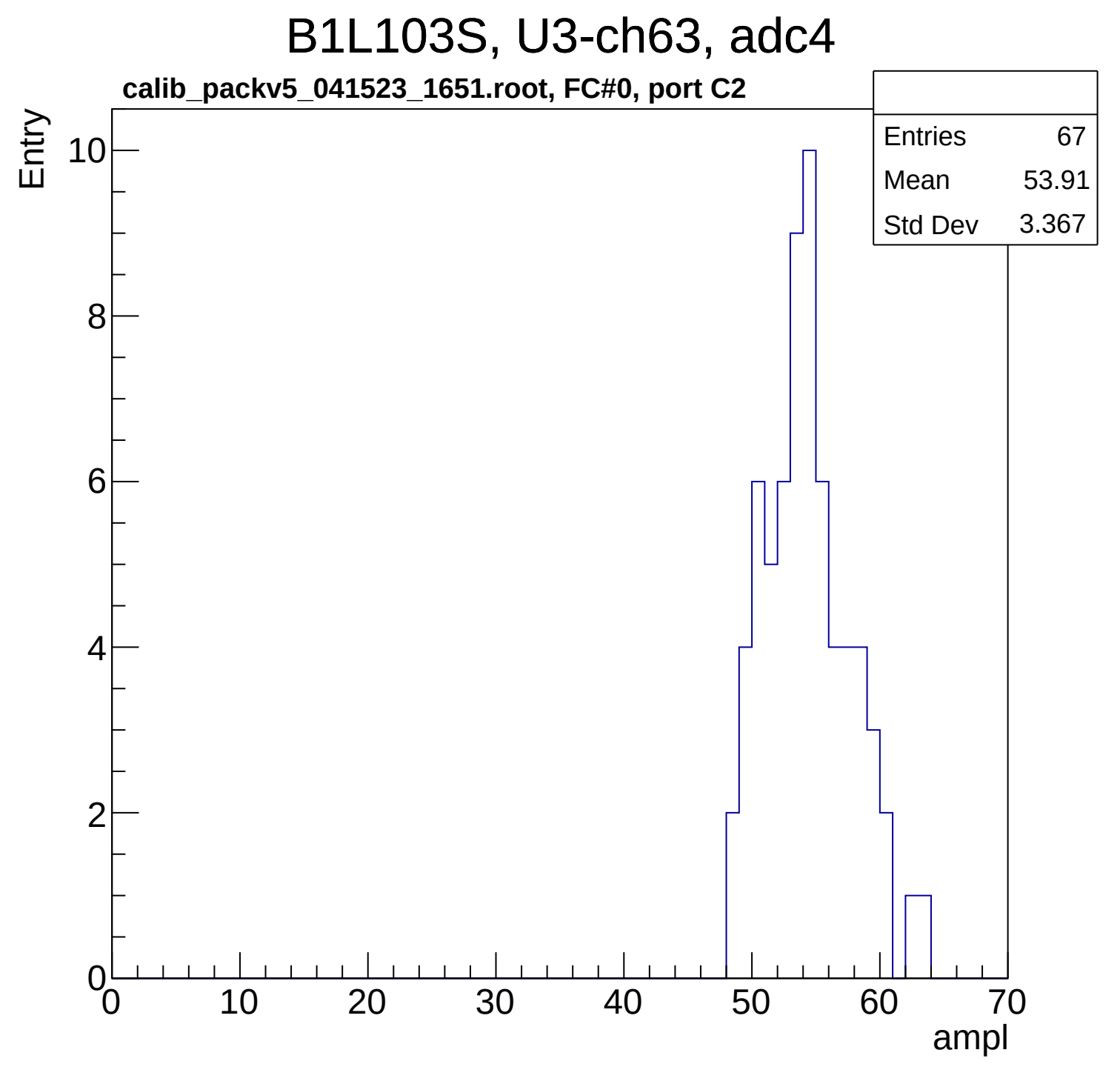
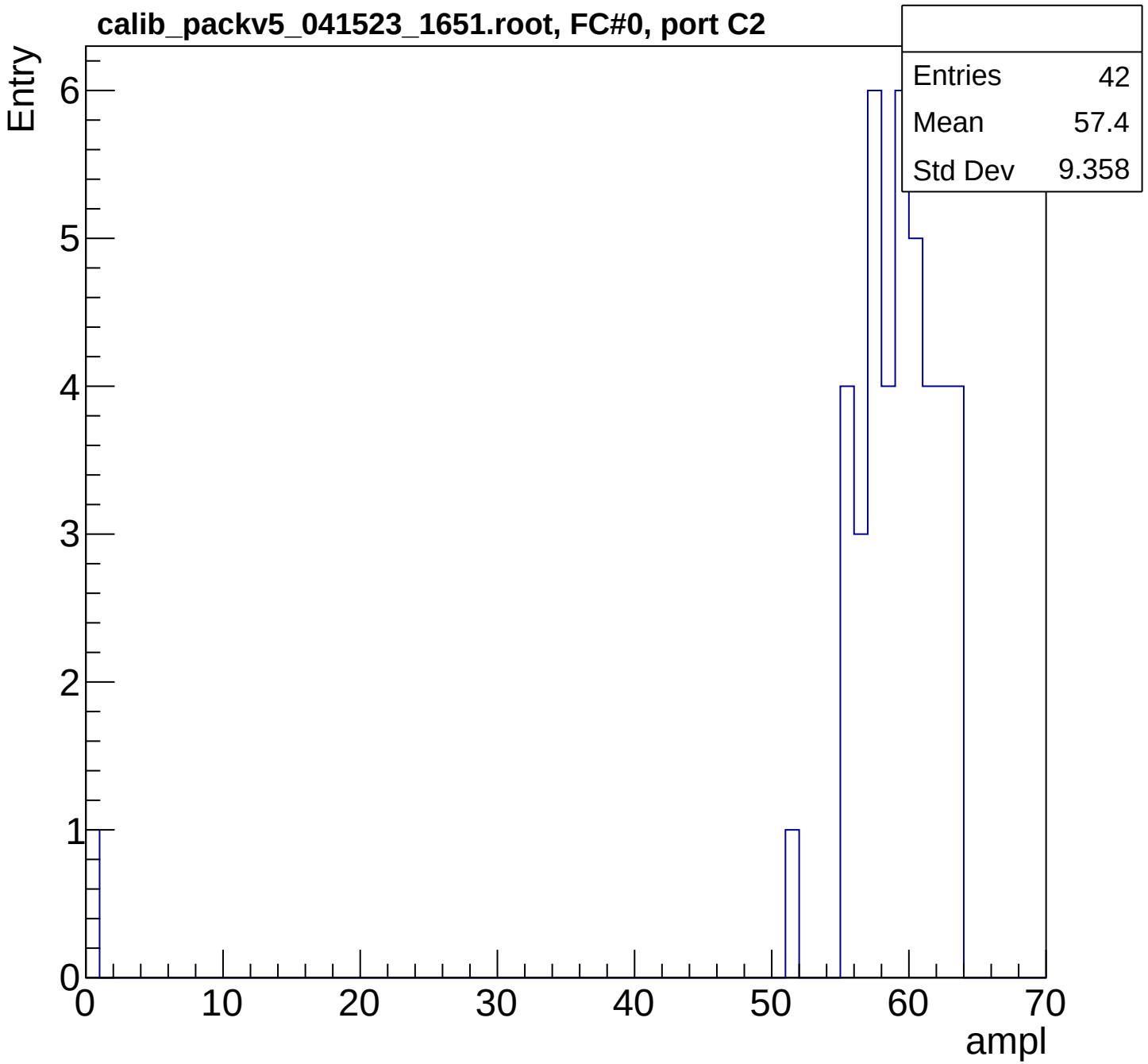
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

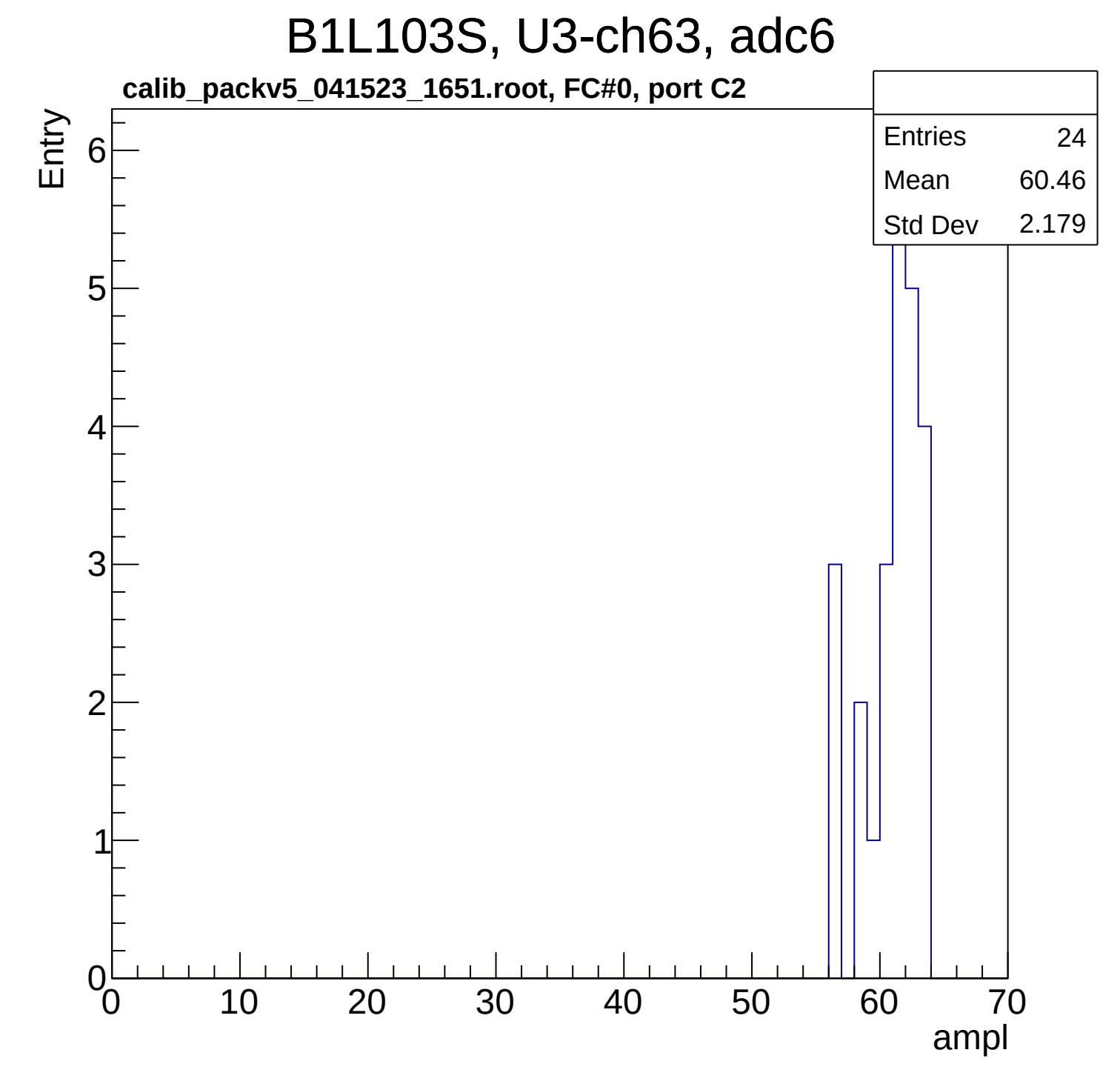

B1L103S, U3-ch63, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 34.66
Std Dev 5.397
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

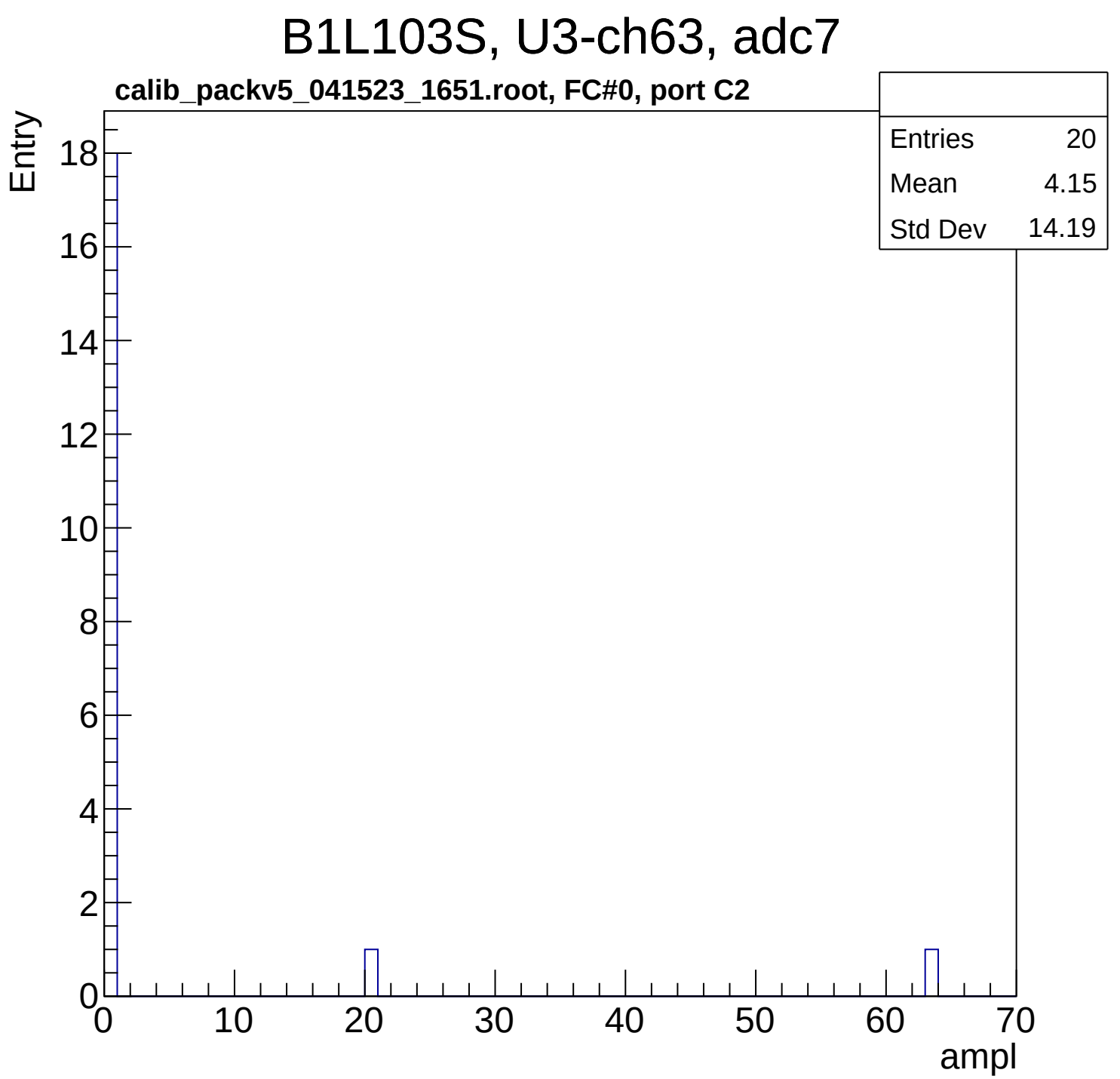

B1L103S, U3-ch63, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 32.31
Std Dev 17.13
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

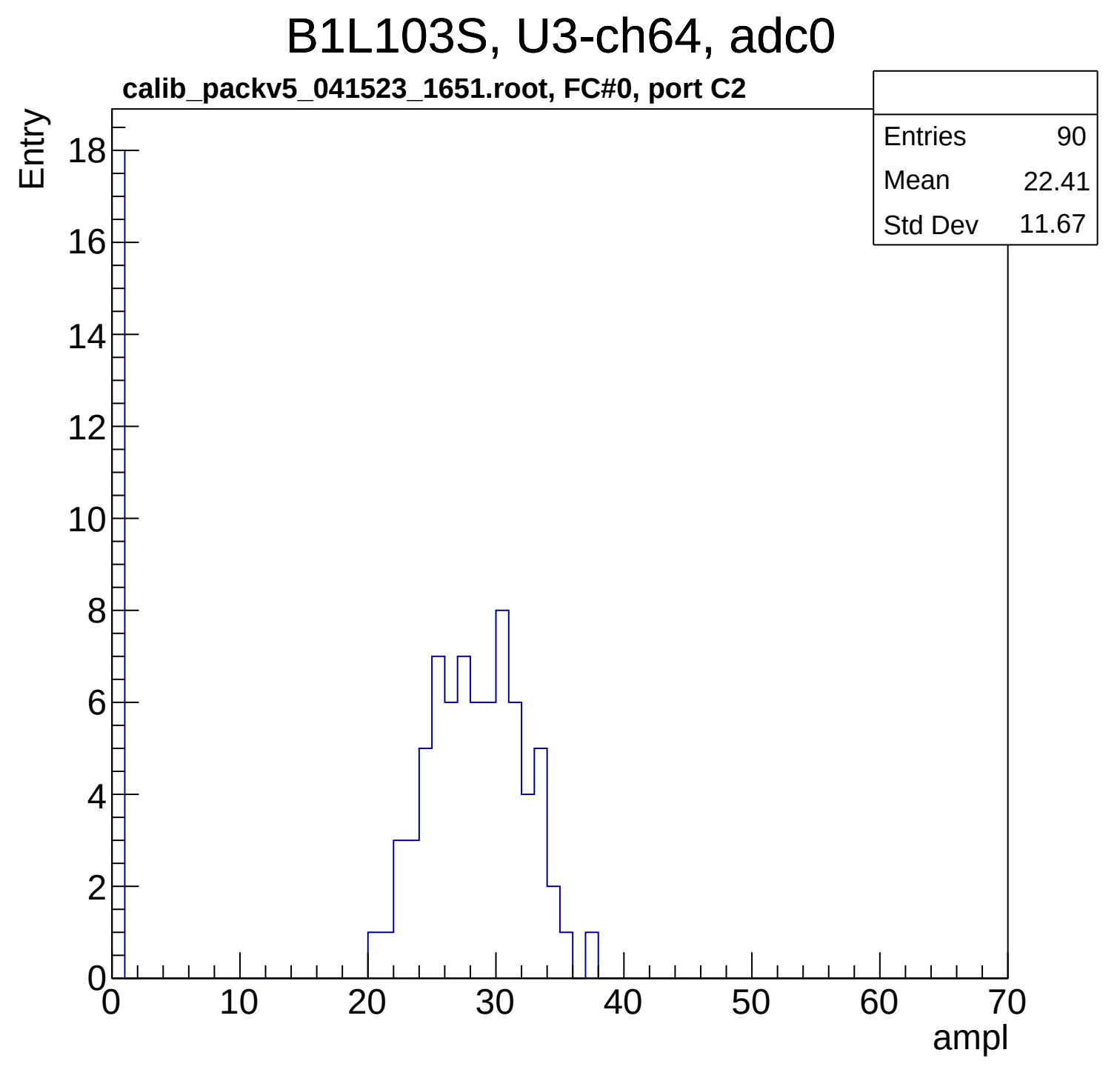

B1L103S, U3-ch63, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 46.89
Std Dev 2.971
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch63, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 53.91
Std Dev 3.367
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U3-ch63, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 57.4
Std Dev 9.358
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U3-ch63, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 60.46
Std Dev 2.179
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U3-ch63, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4.15
Std Dev 14.19
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch64, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 22.41
Std Dev 11.67
Entry
ampl
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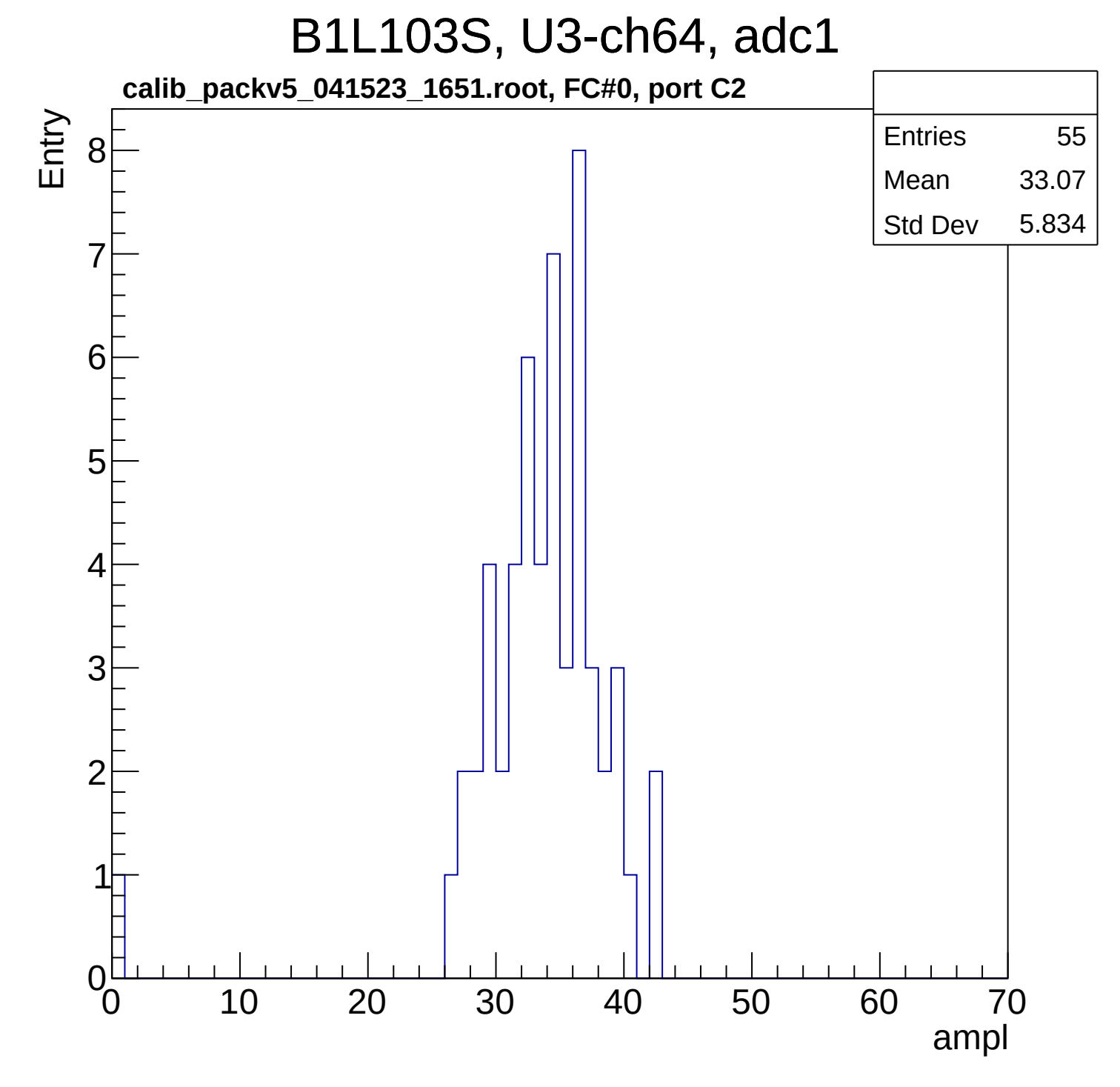
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L103S, U3-ch64, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 33.07
Std Dev 5.834
Entry
ampl
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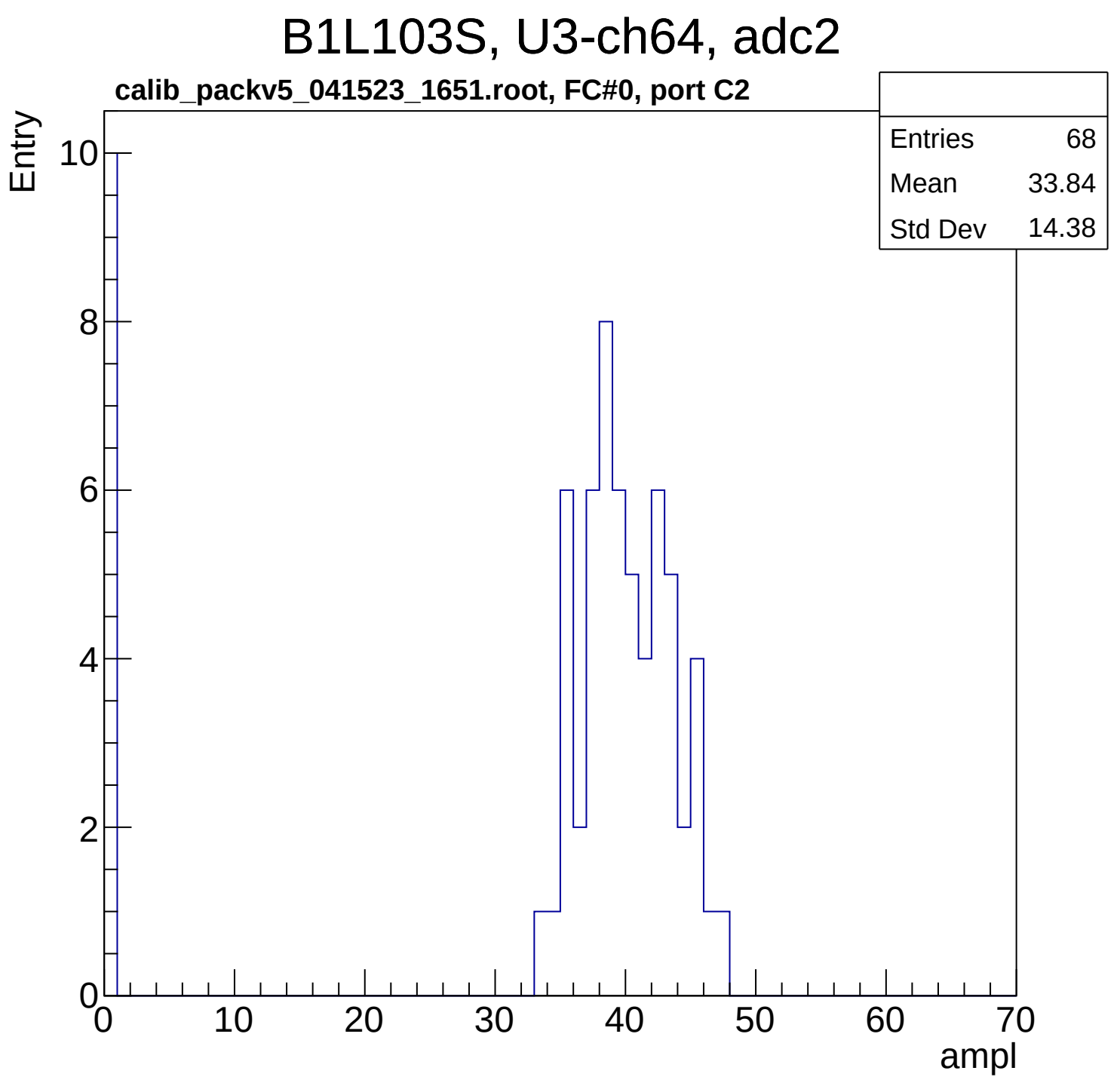
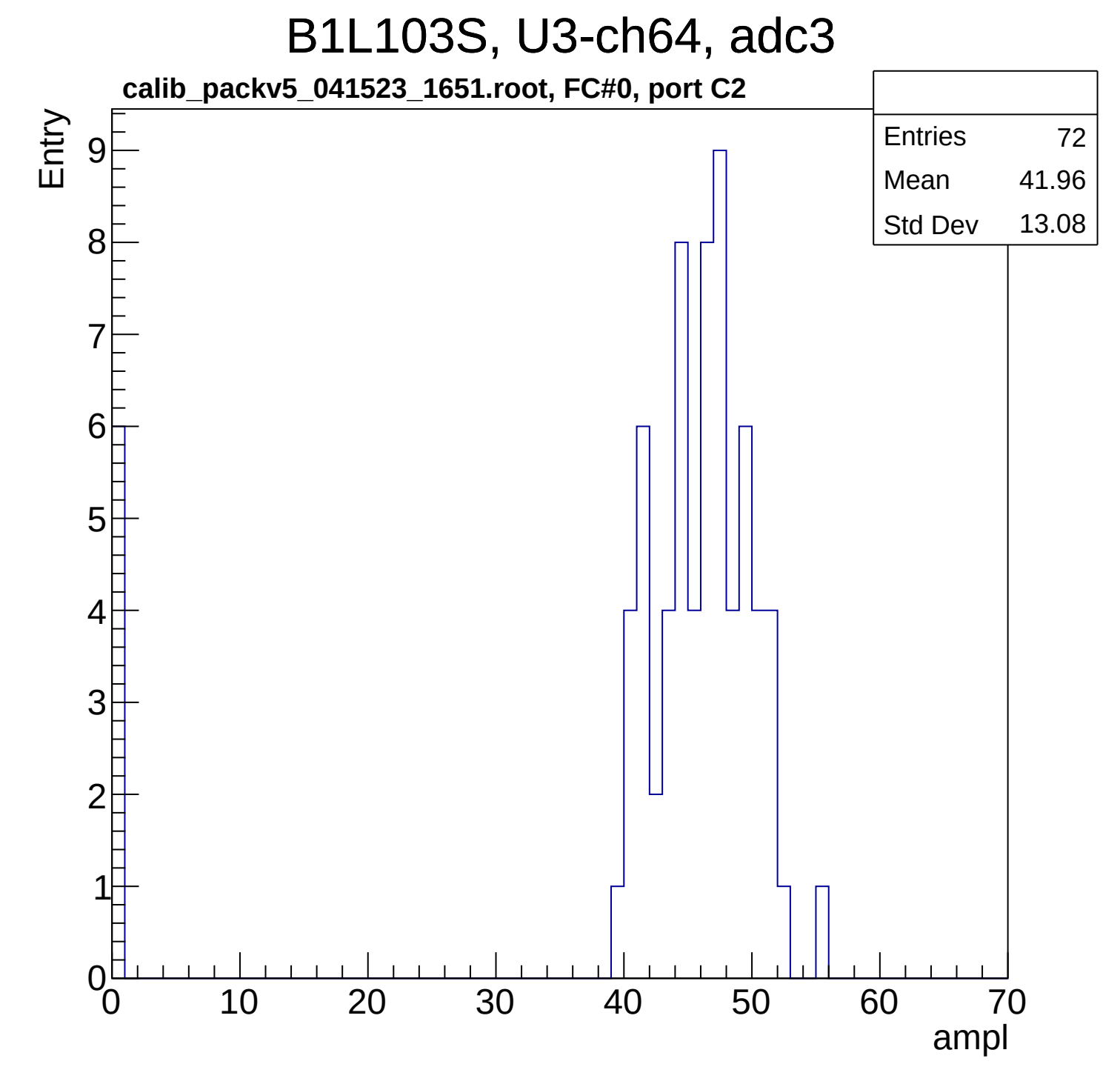
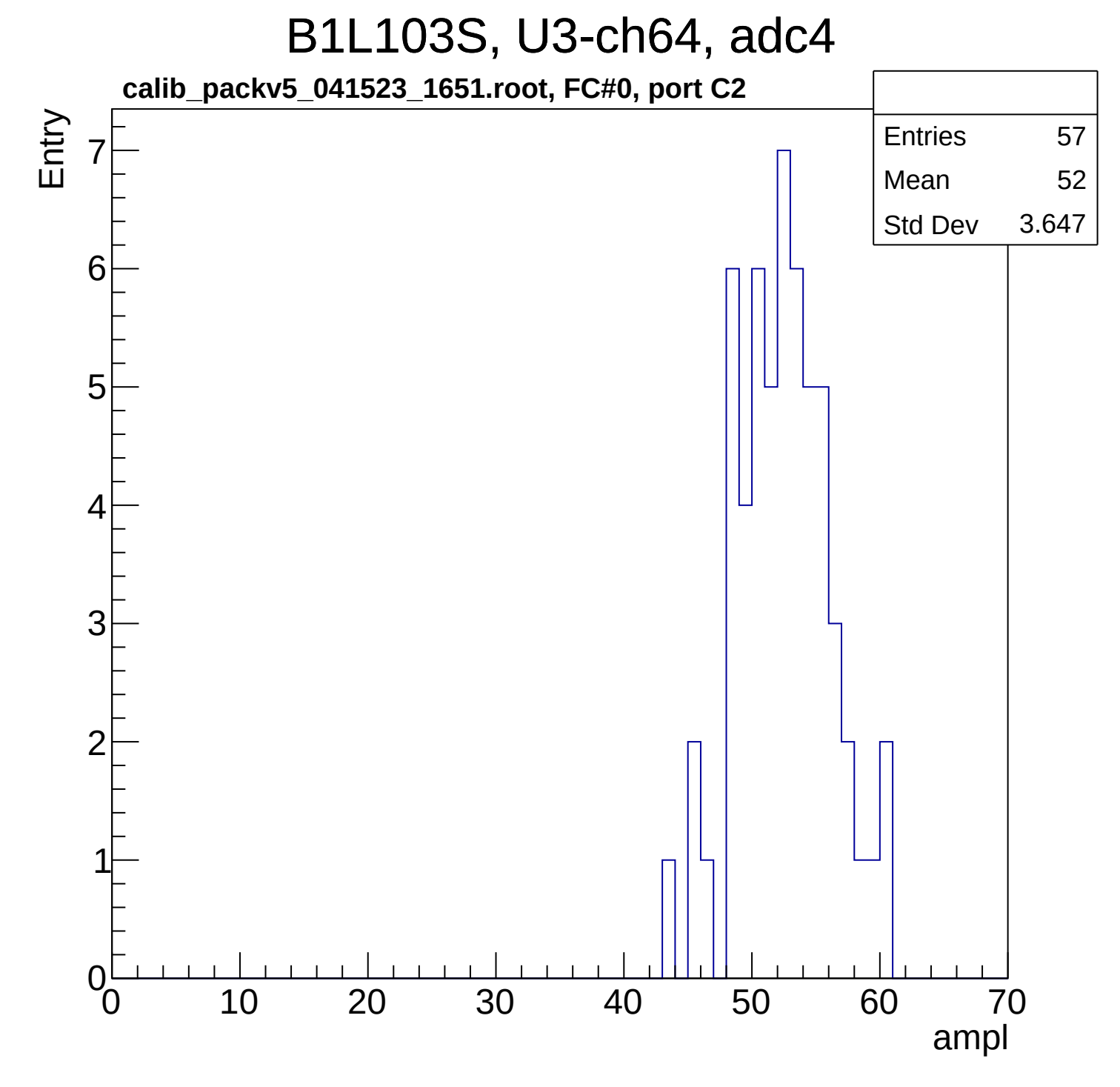
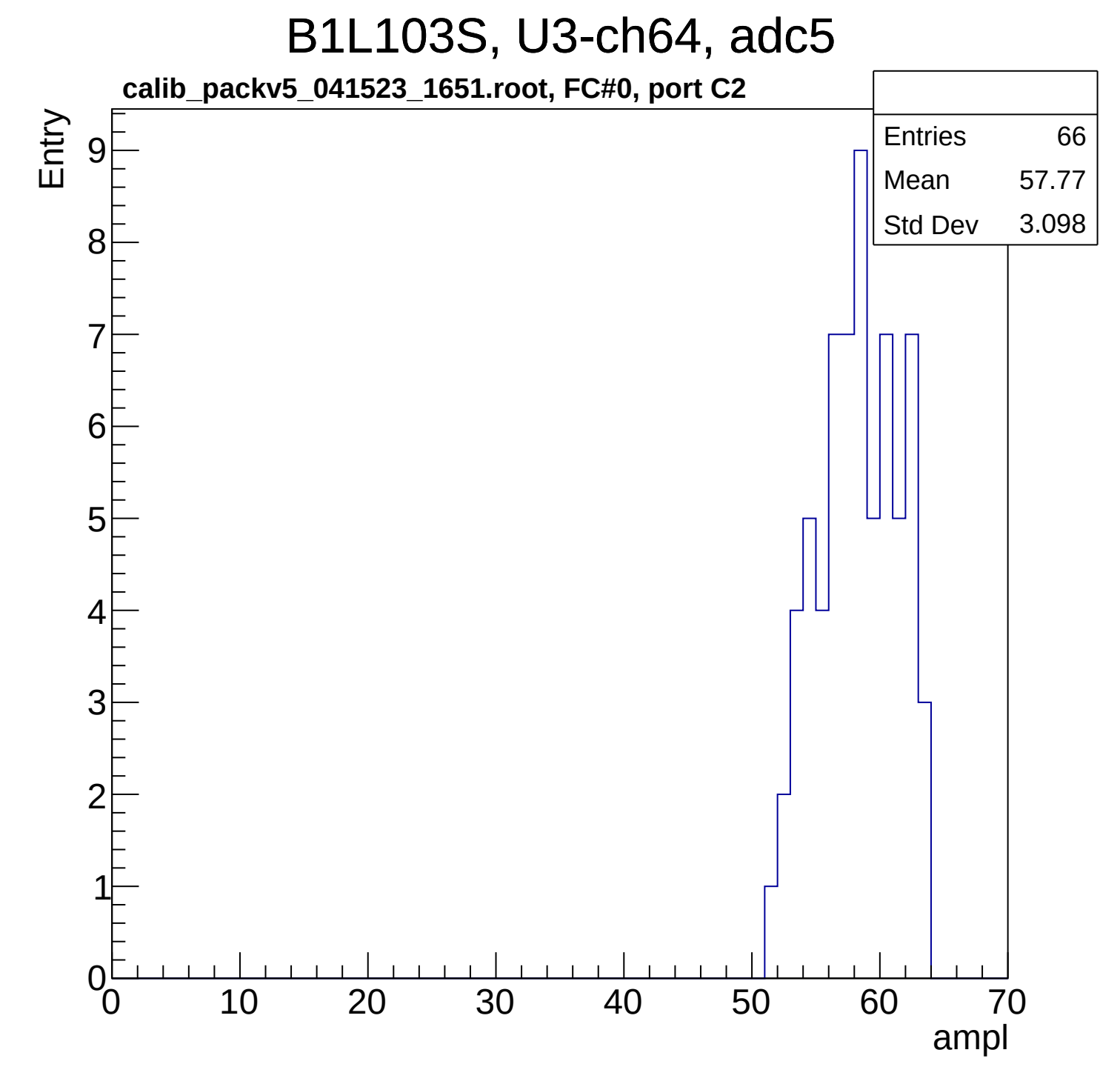
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch64, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 33.84
Std Dev 14.38
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch64, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 41.96
Std Dev 13.08
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch64, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 52
Std Dev 3.647
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch64, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 57.77
Std Dev 3.098
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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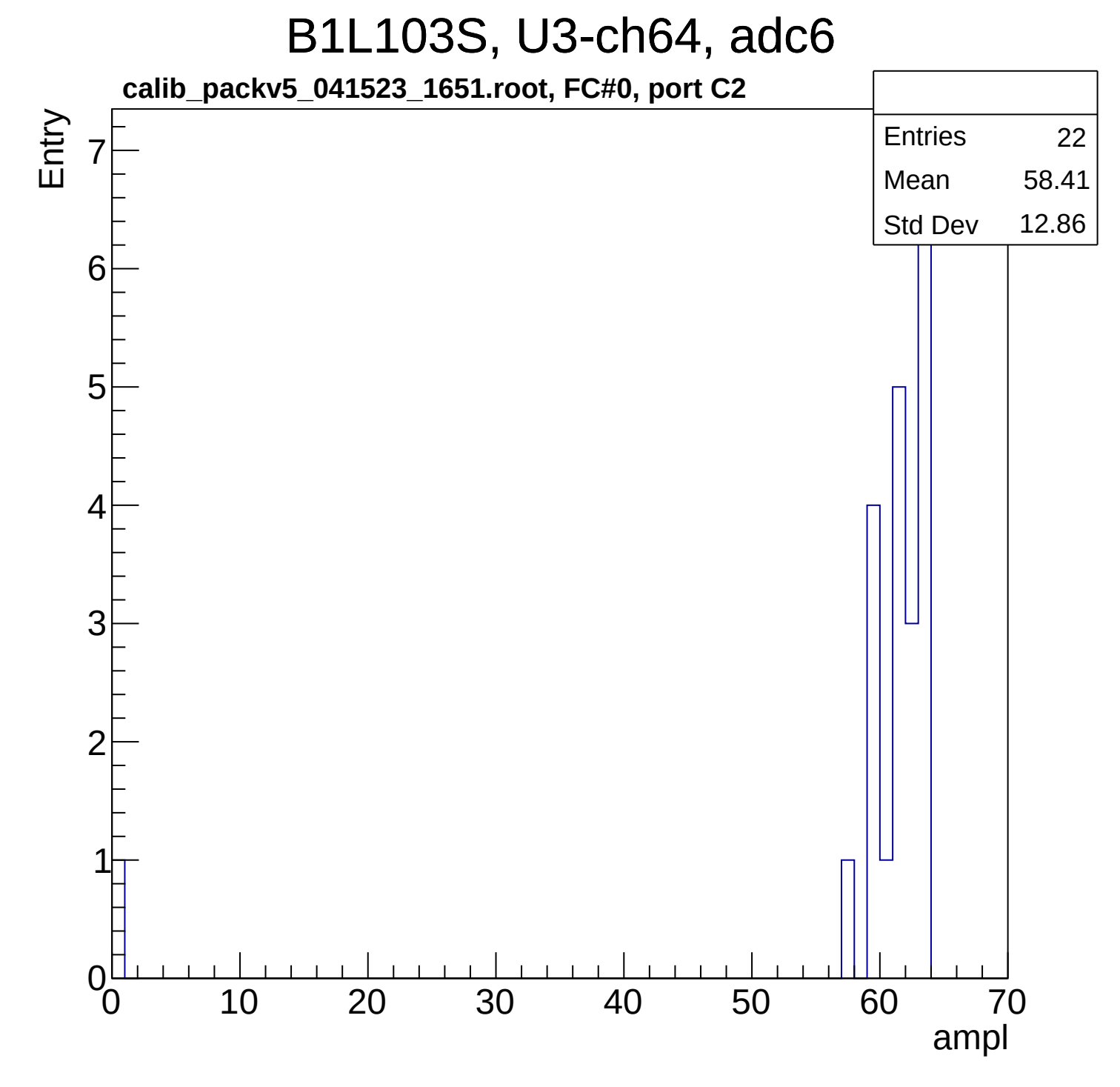
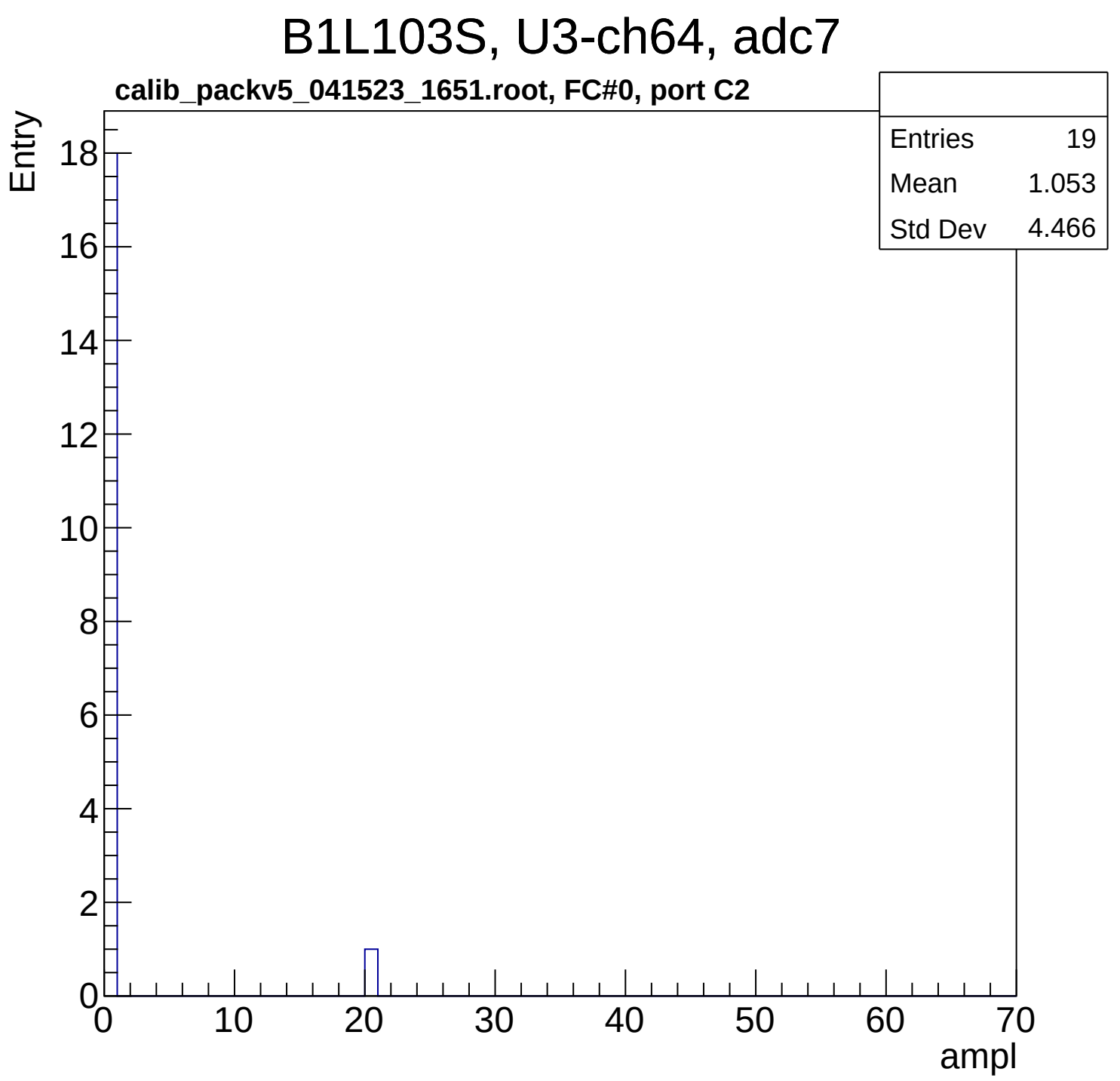

B1L103S, U3-ch64, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 58.41
Std Dev 12.86
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch64, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.053
Std Dev 4.466
Entry
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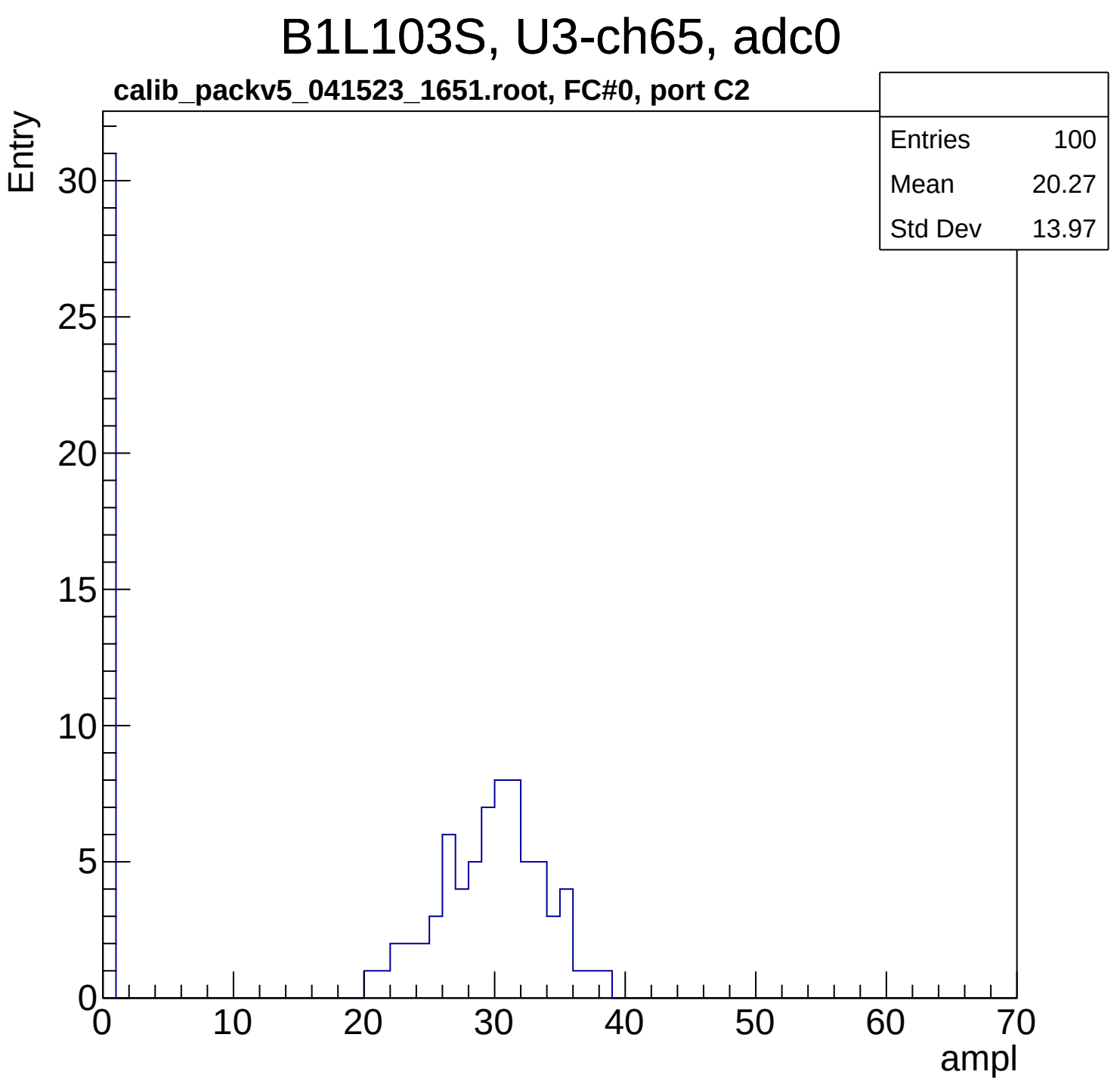
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch65, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 100
Mean 20.27
Std Dev 13.97
Entry
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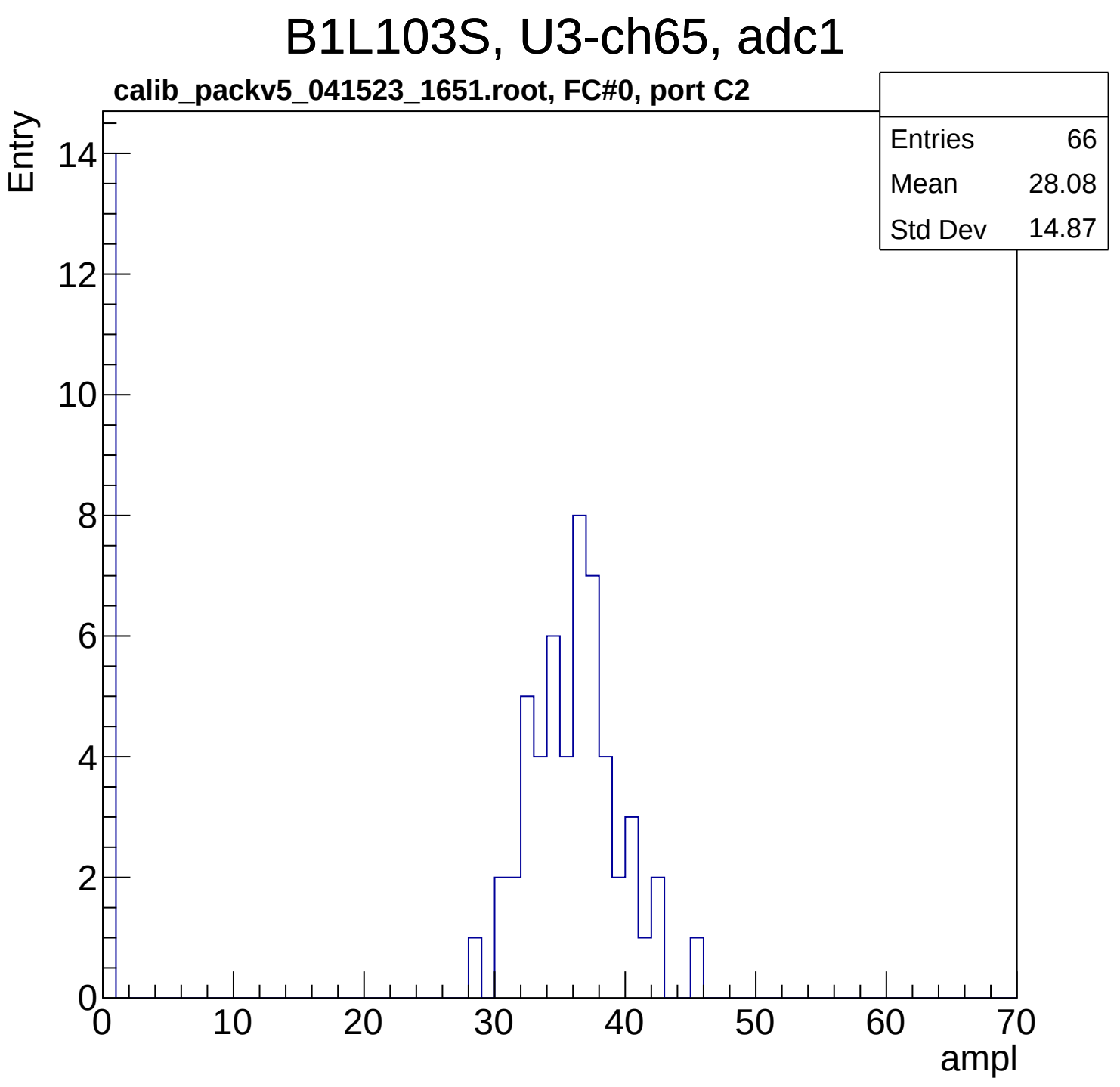
10
15
20
25
30
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch65, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 28.08
Std Dev 14.87
Entry
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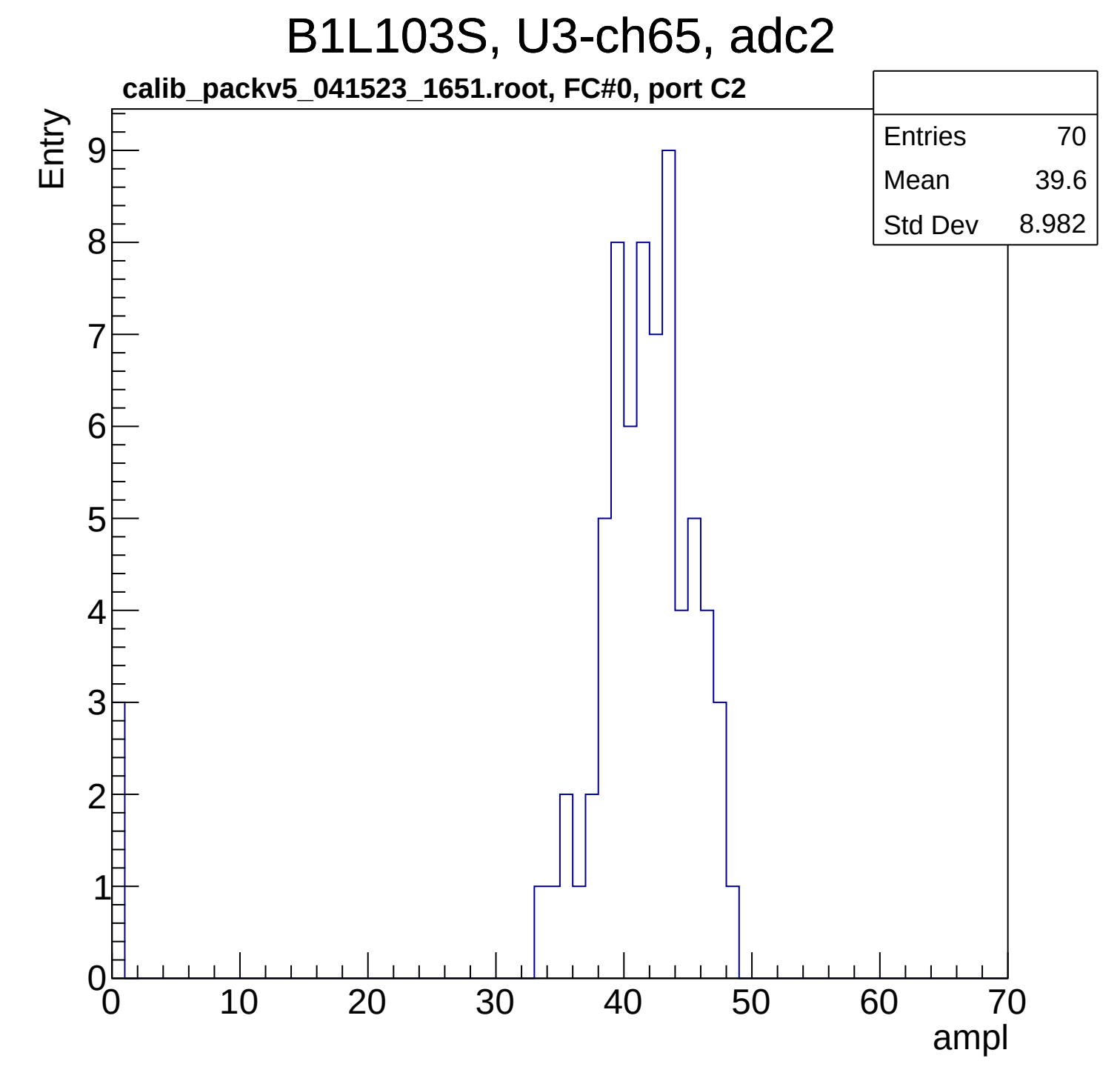
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch65, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 39.6
Std Dev 8.982
Entry
ampl
0
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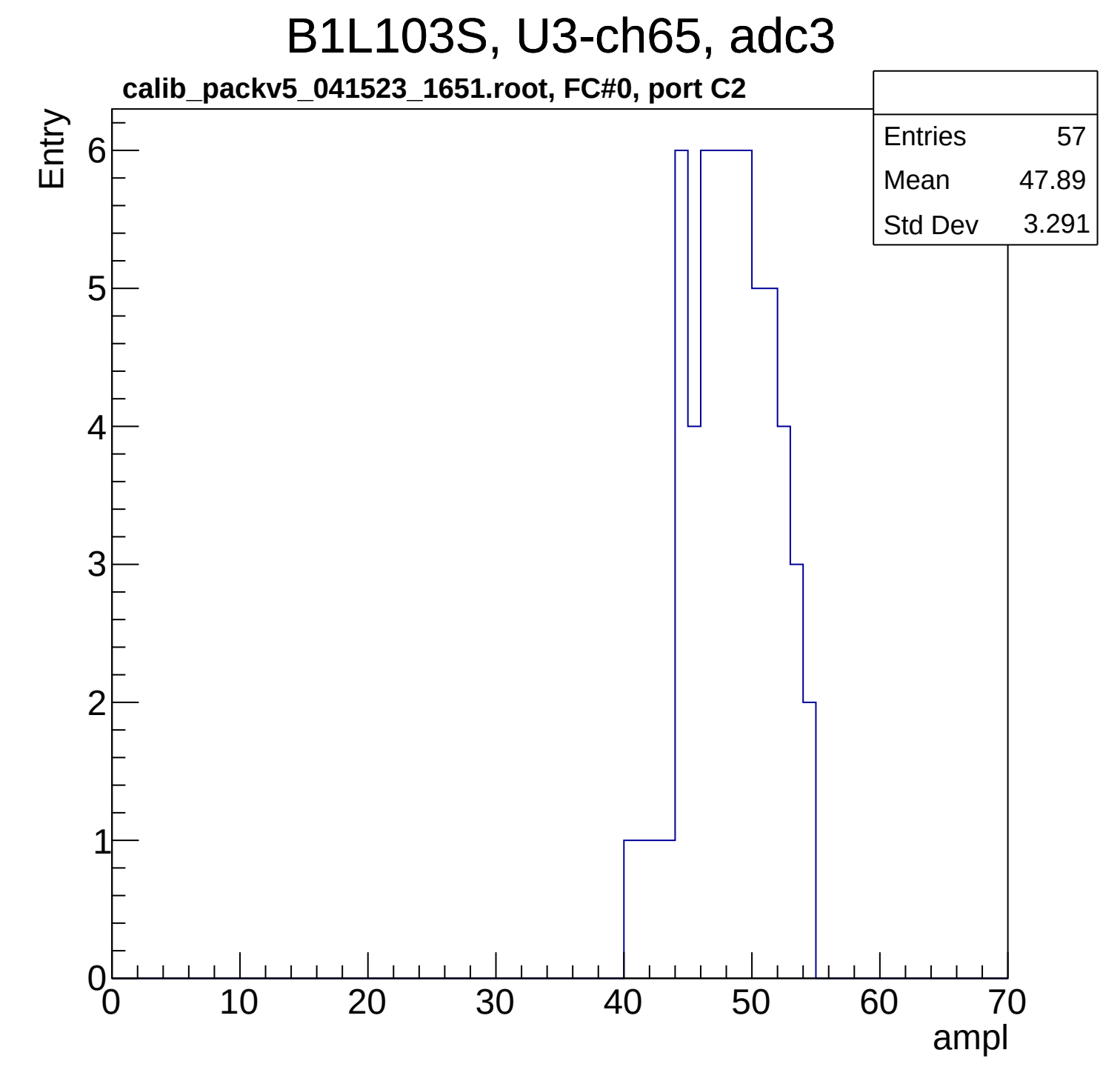
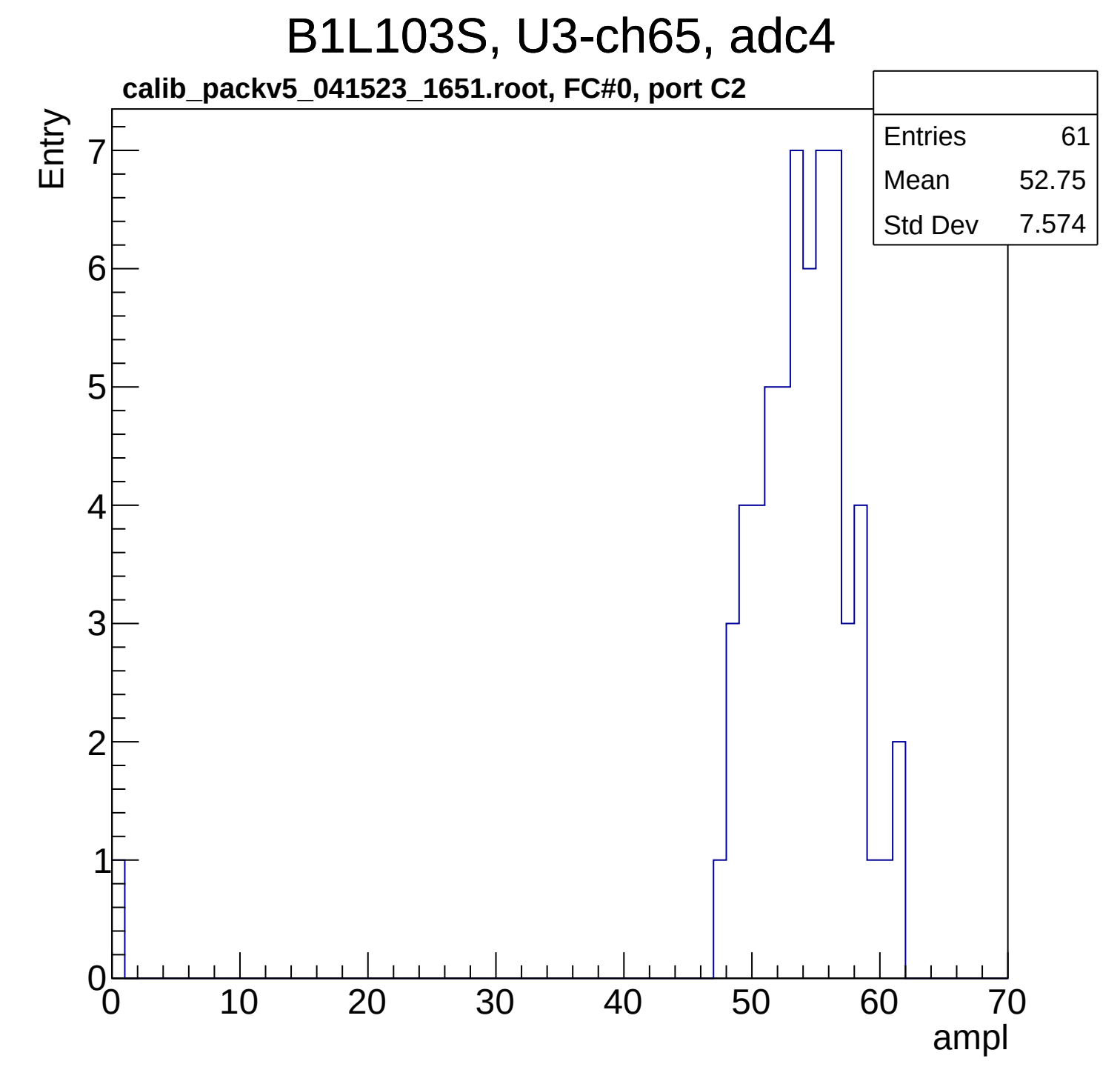
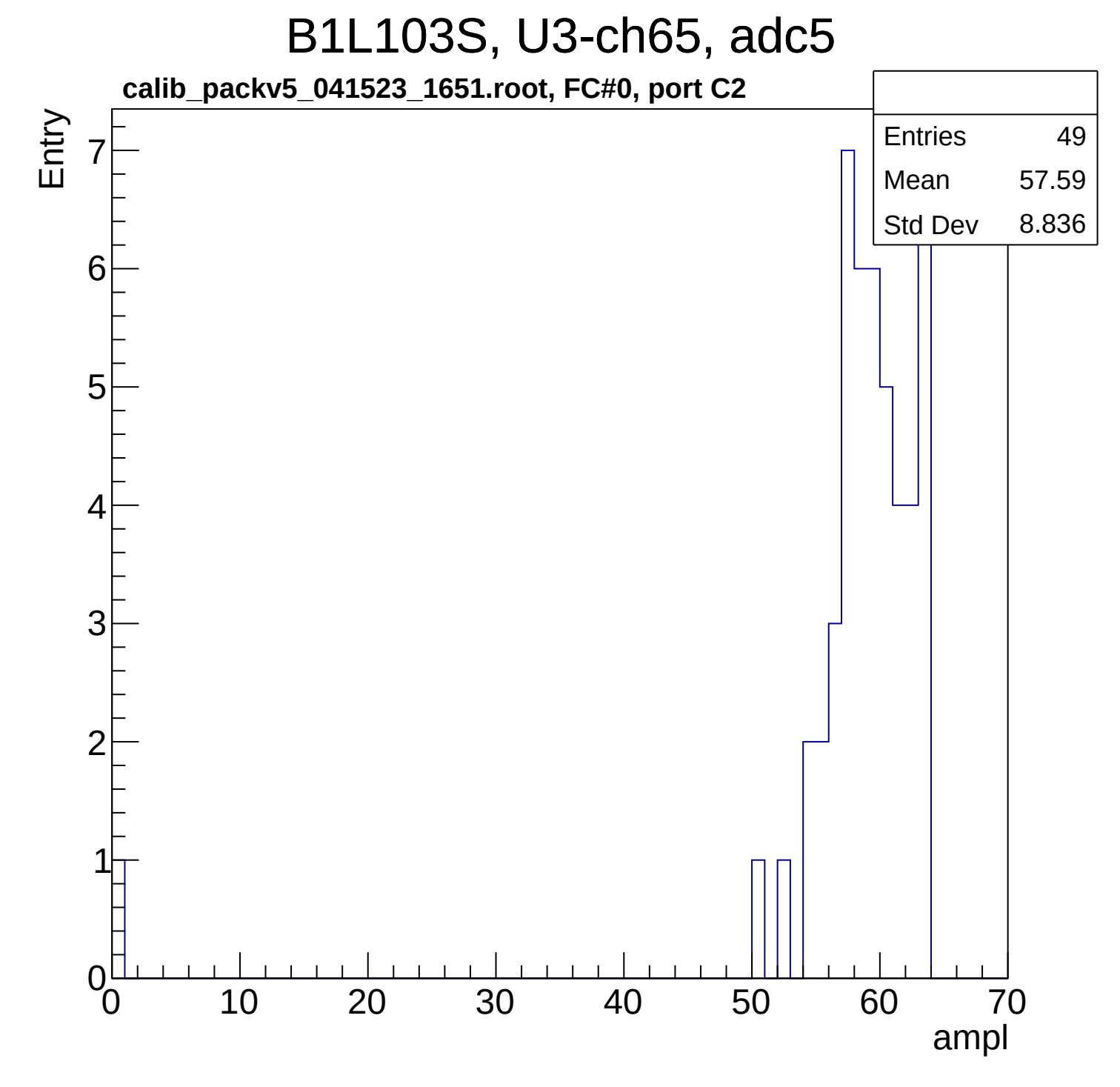
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch65, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 47.89
Std Dev 3.291
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch65, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 52.75
Std Dev 7.574
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch65, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 57.59
Std Dev 8.836
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
50
60
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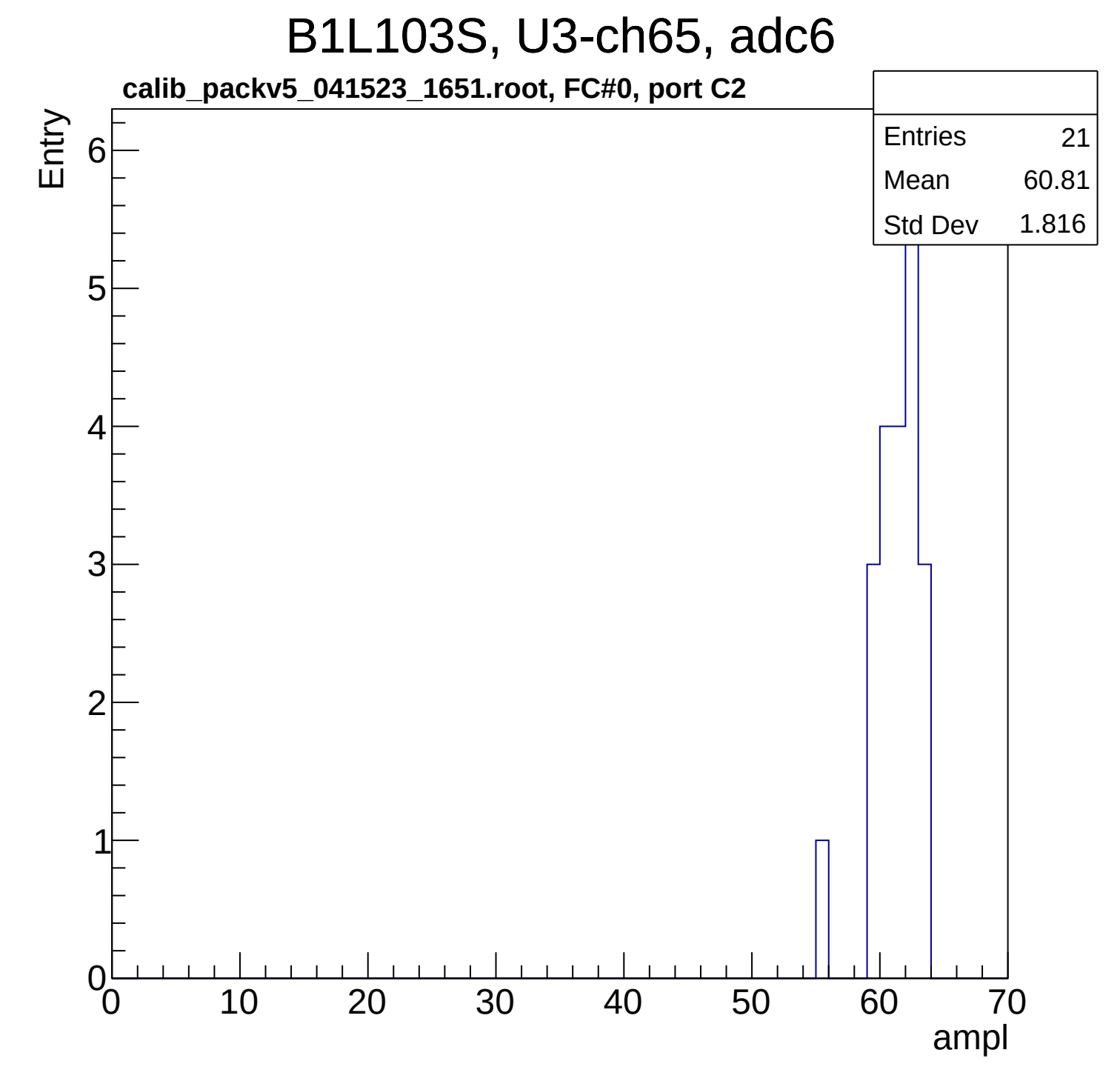
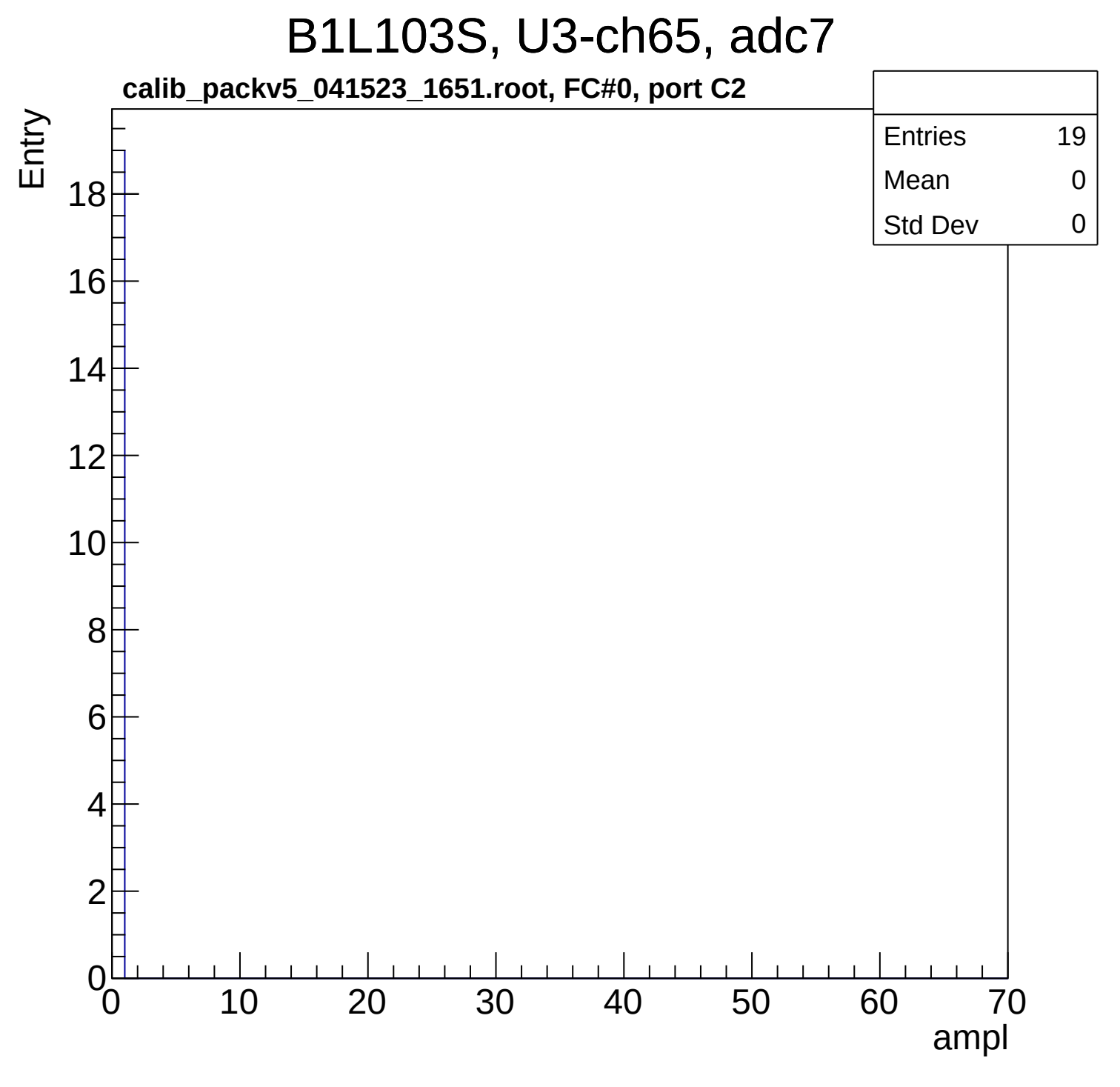
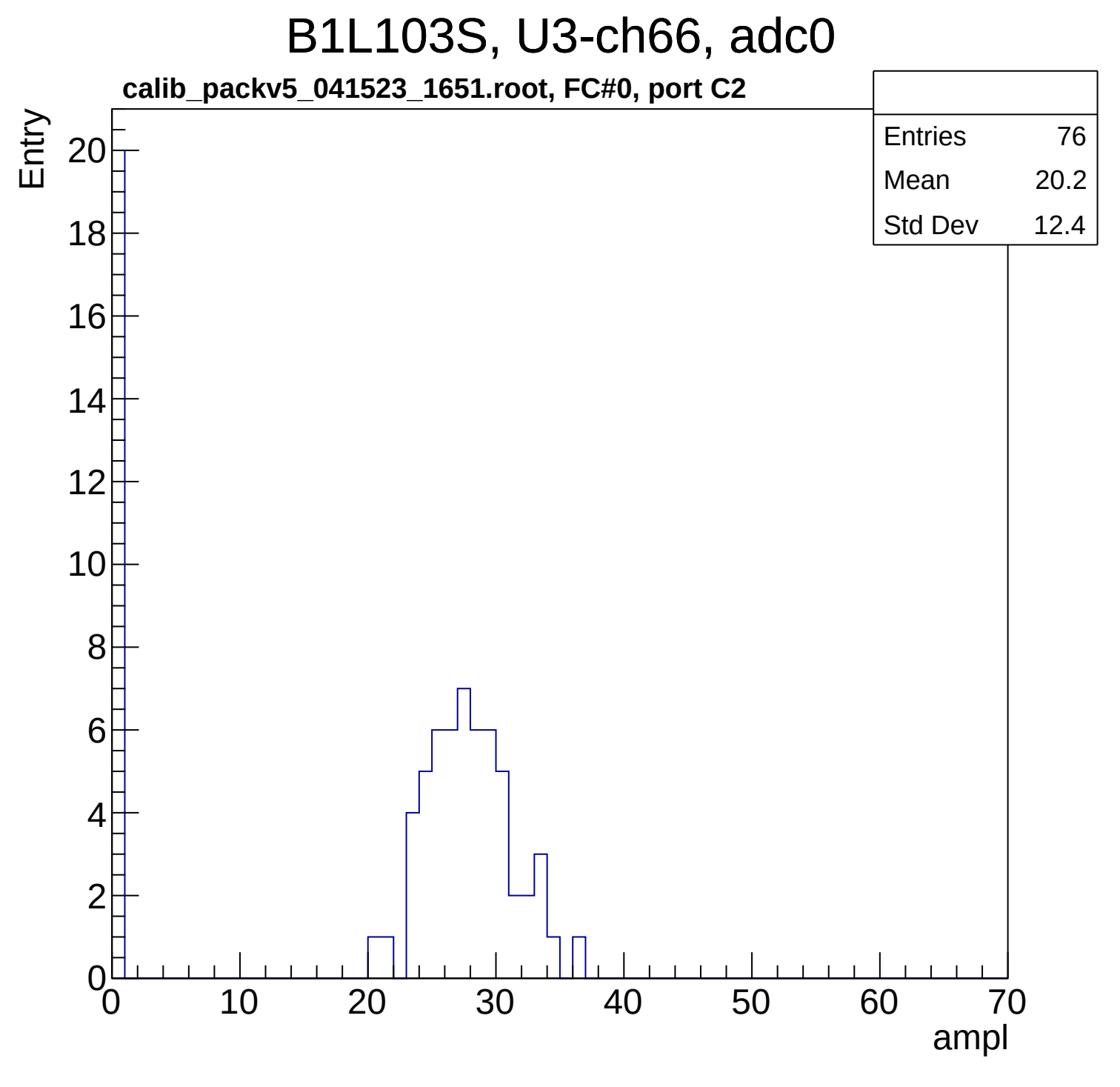

B1L103S, U3-ch65, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 60.81
Std Dev 1.816
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U3-ch65, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch66, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 20.2
Std Dev 12.4
Entry
ampl
0
2
4
6
8
10
12
14
16
18
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60
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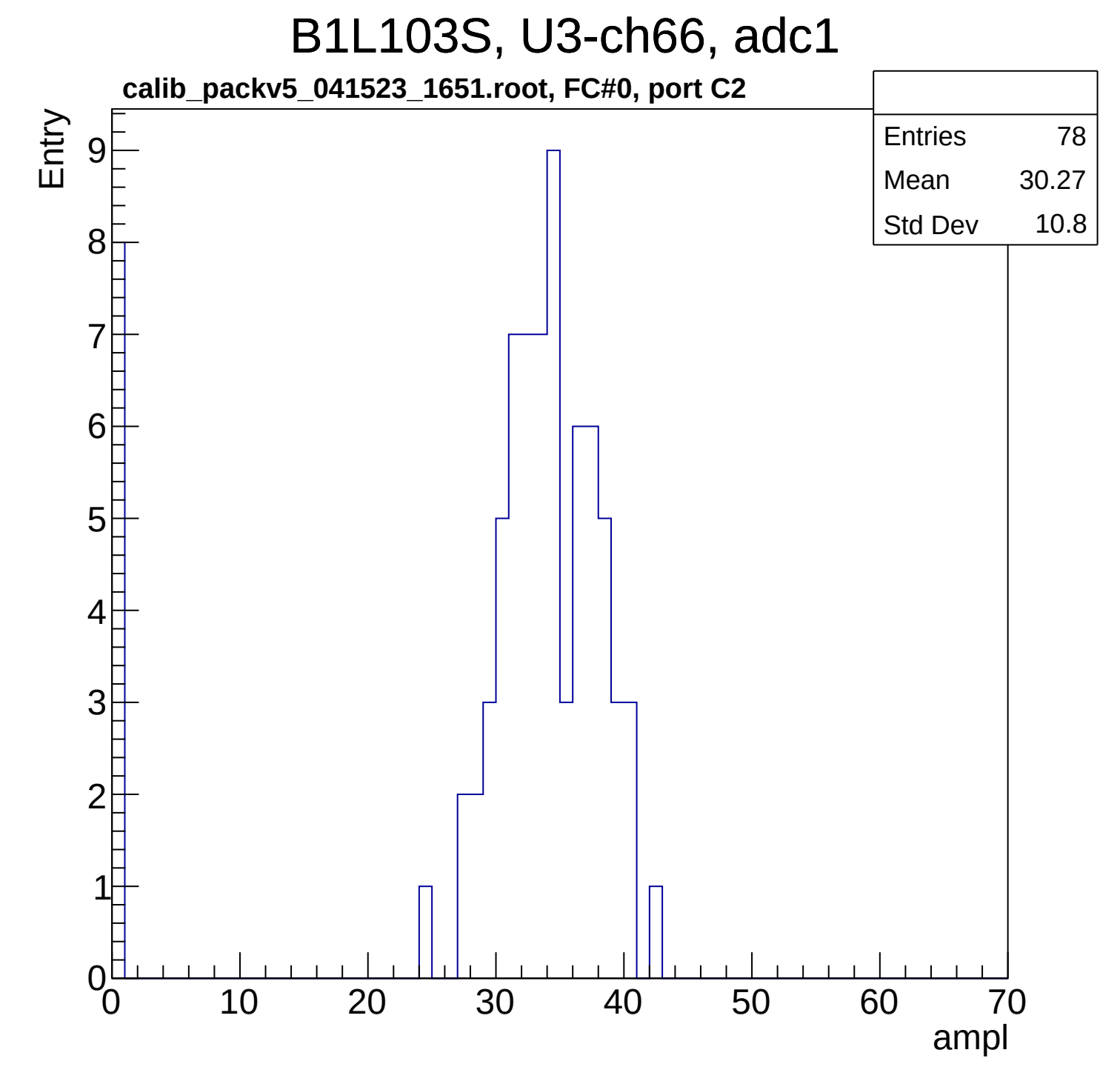
B1L103S, U3-ch66, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 30.27
Std Dev 10.8
Entry
ampl
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2
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5
6
7
8
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0
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40
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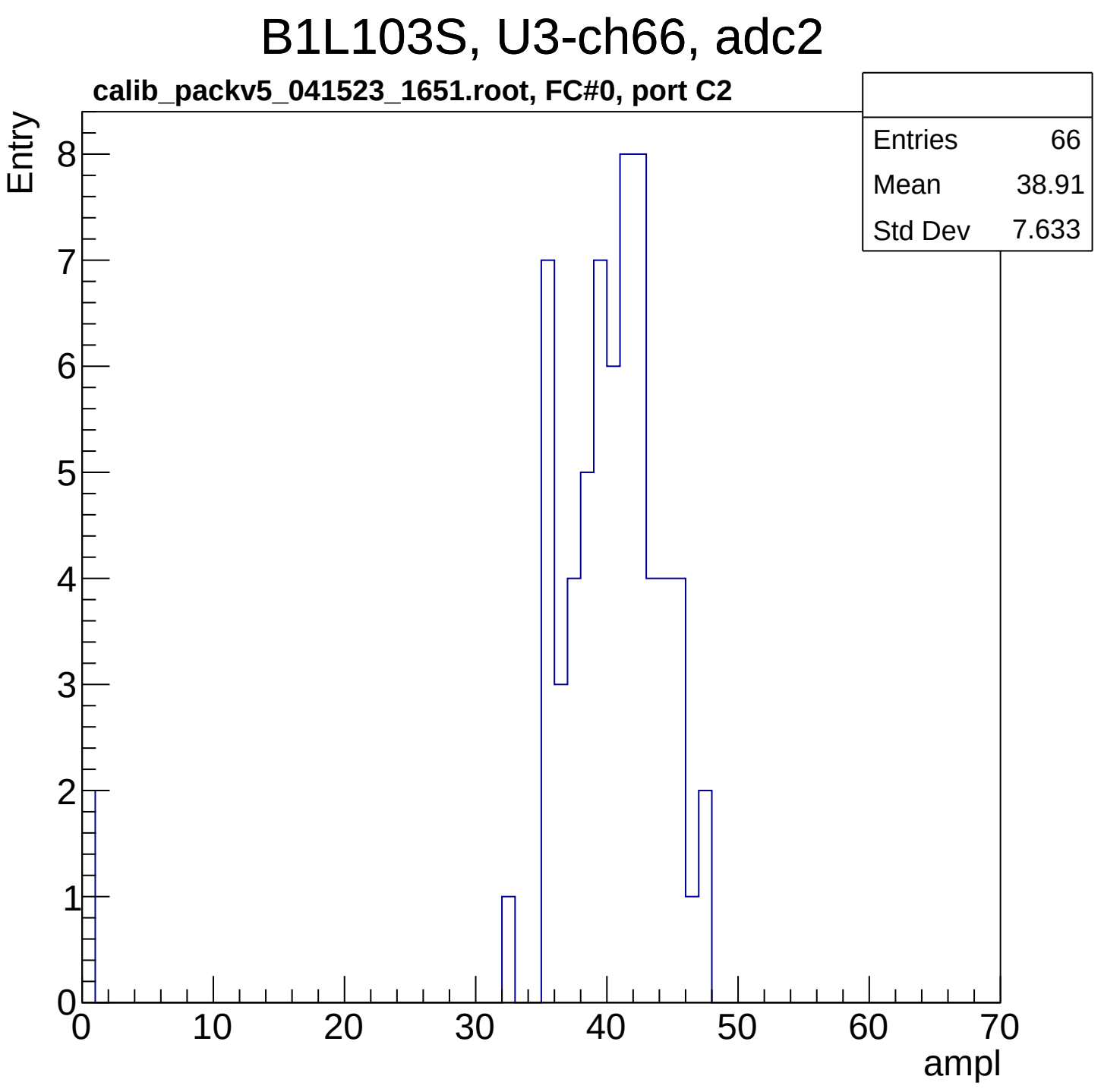
B1L103S, U3-ch66, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 38.91
Std Dev 7.633
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
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60
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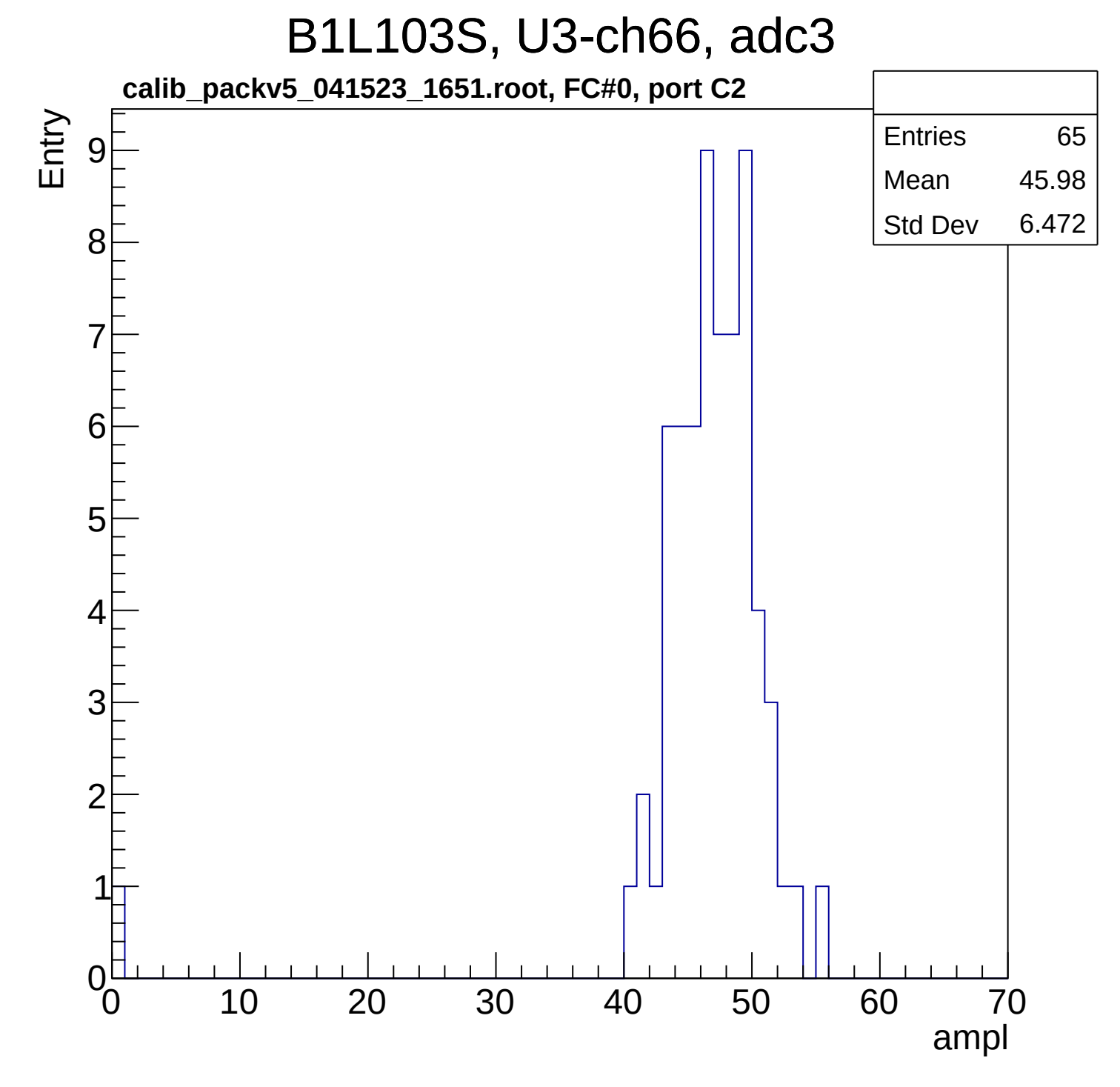
B1L103S, U3-ch66, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 45.98
Std Dev 6.472
Entry
ampl
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10
20
30
40
50
60
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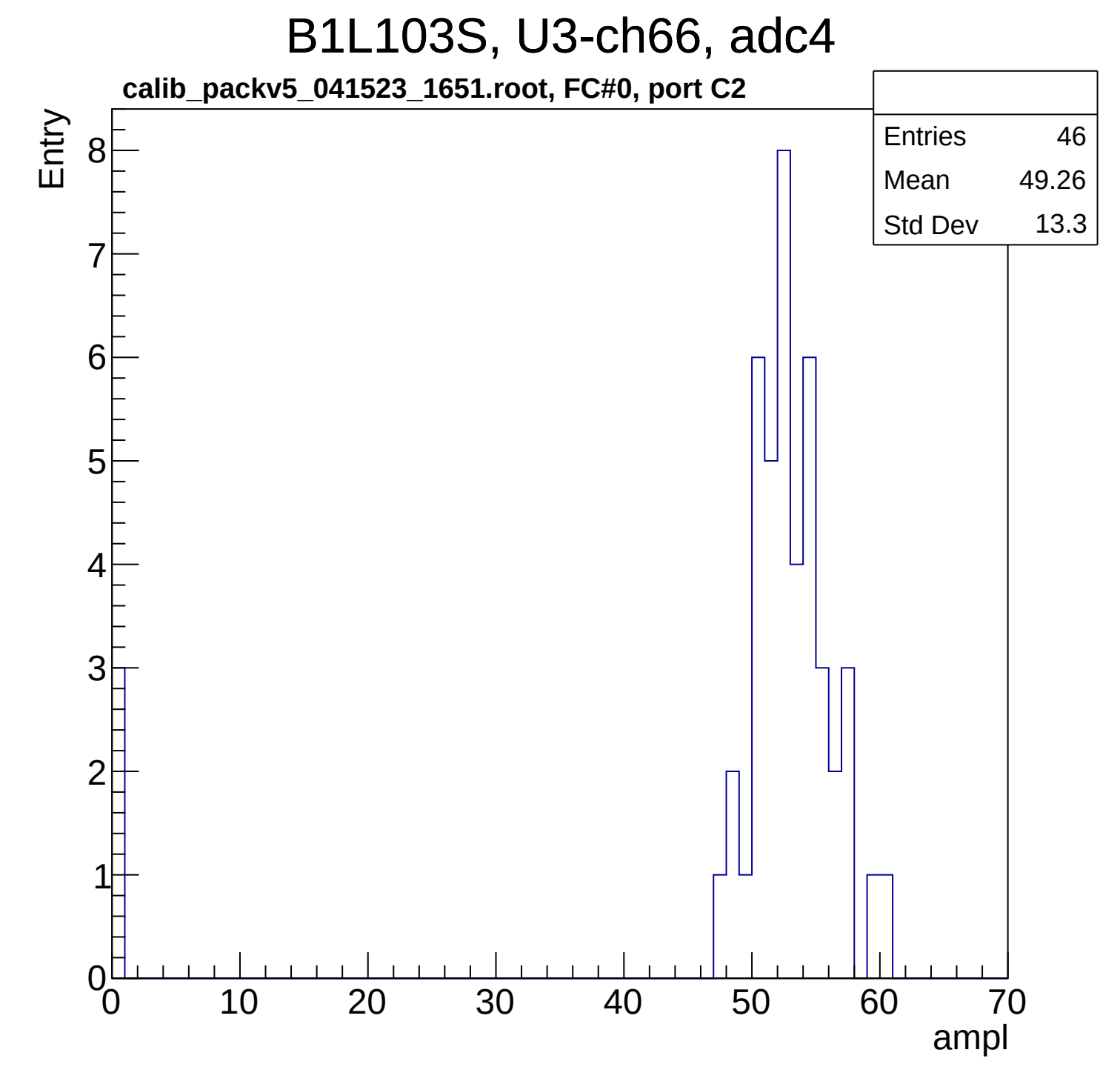
1
2
3
4
5
6
7
8
9


B1L103S, U3-ch66, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 49.26
Std Dev 13.3
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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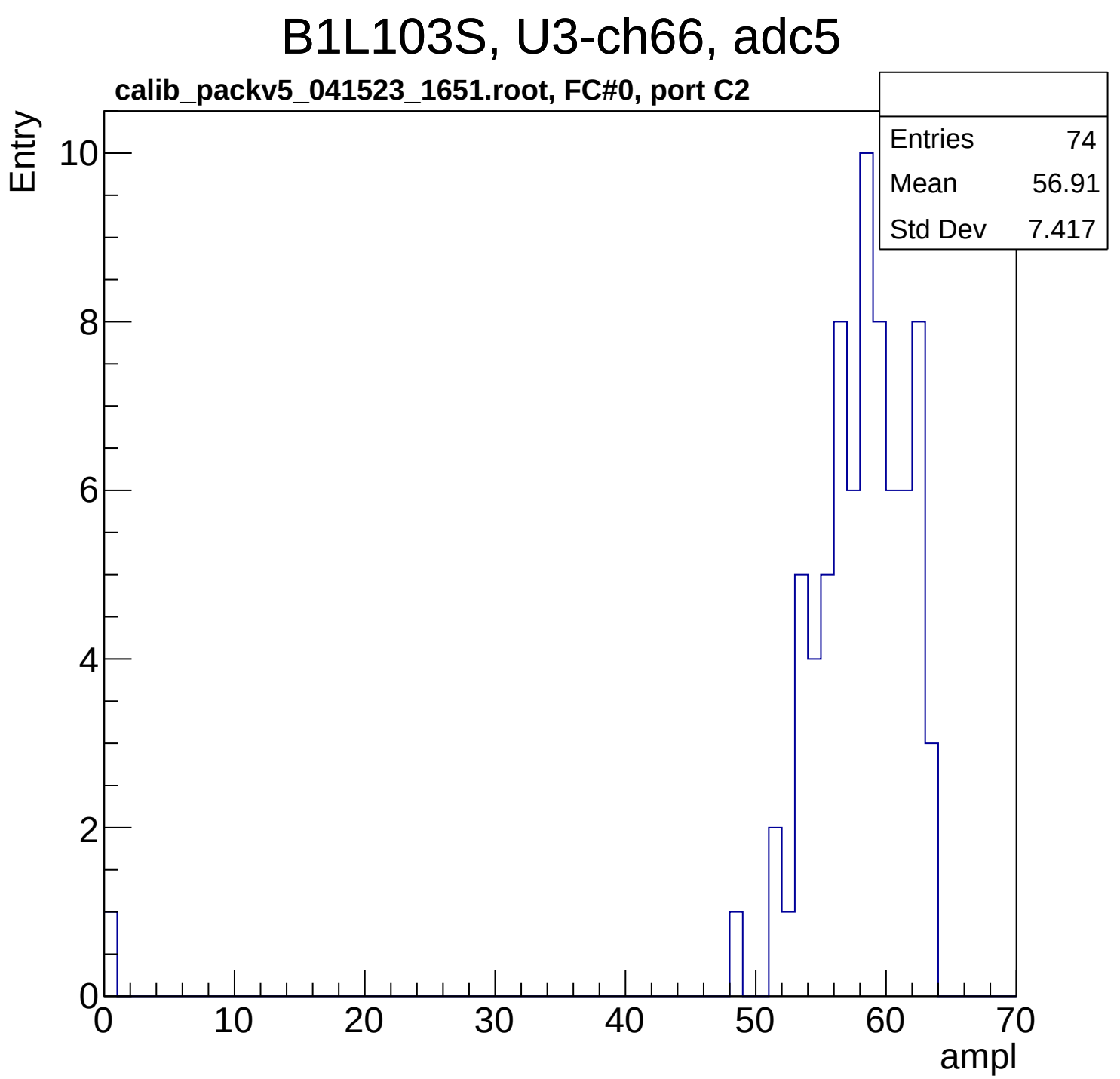
B1L103S, U3-ch66, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 56.91
Std Dev 7.417
Entry
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2
4
6
8
10
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10
20
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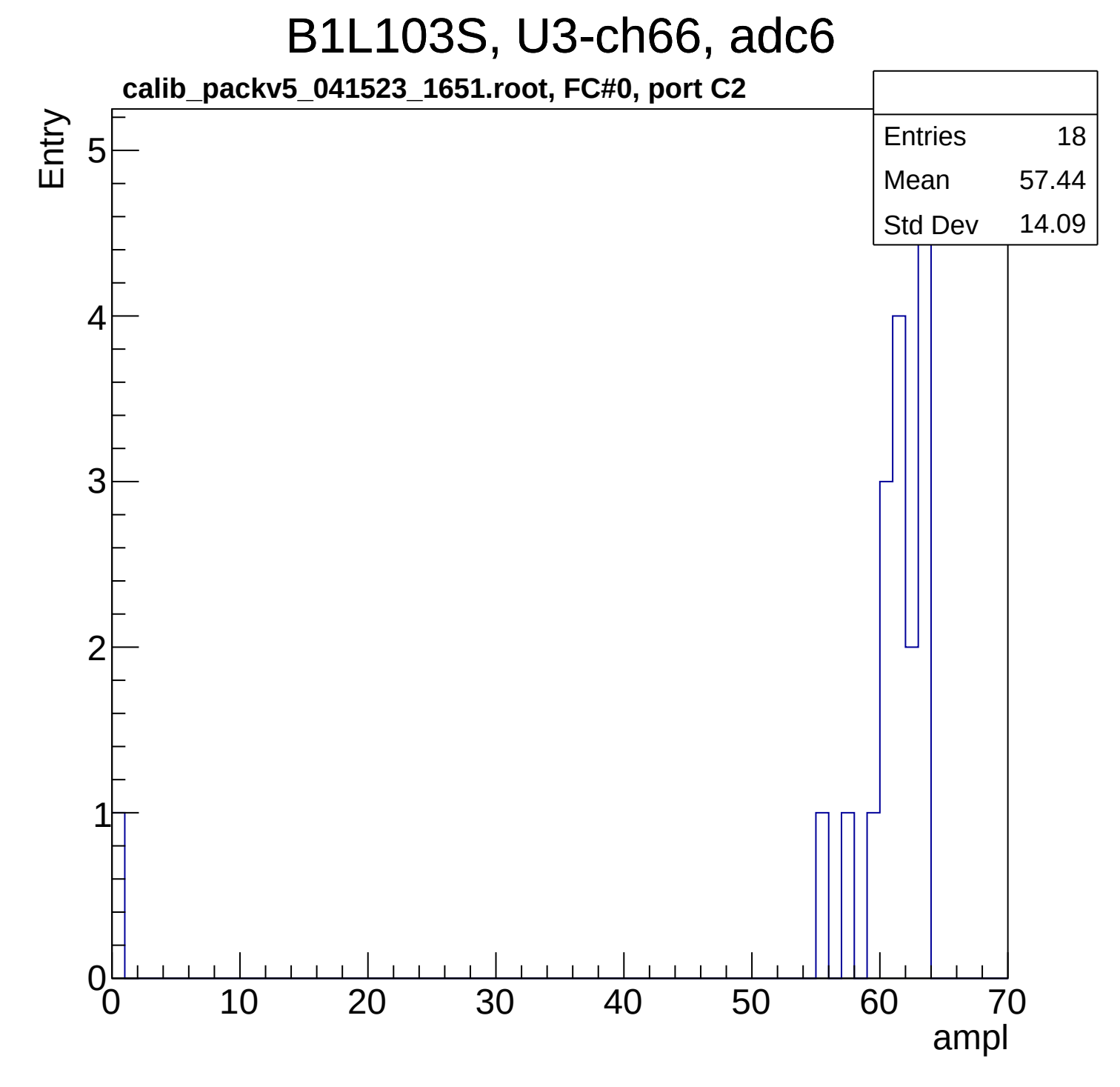
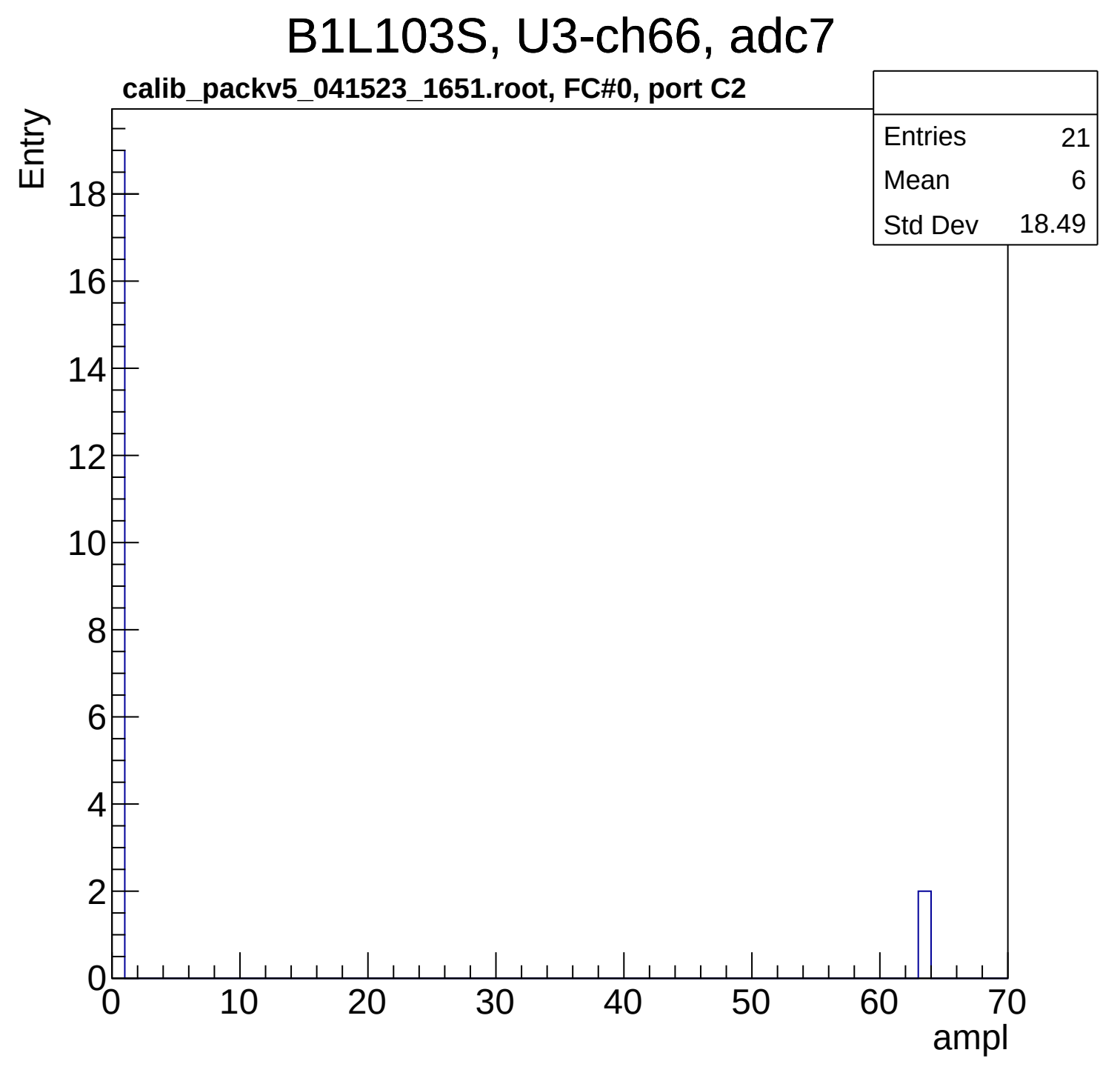
50
60
70
ampl


B1L103S, U3-ch66, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 57.44
Std Dev 14.09
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U3-ch66, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 6
Std Dev 18.49
Entry
0
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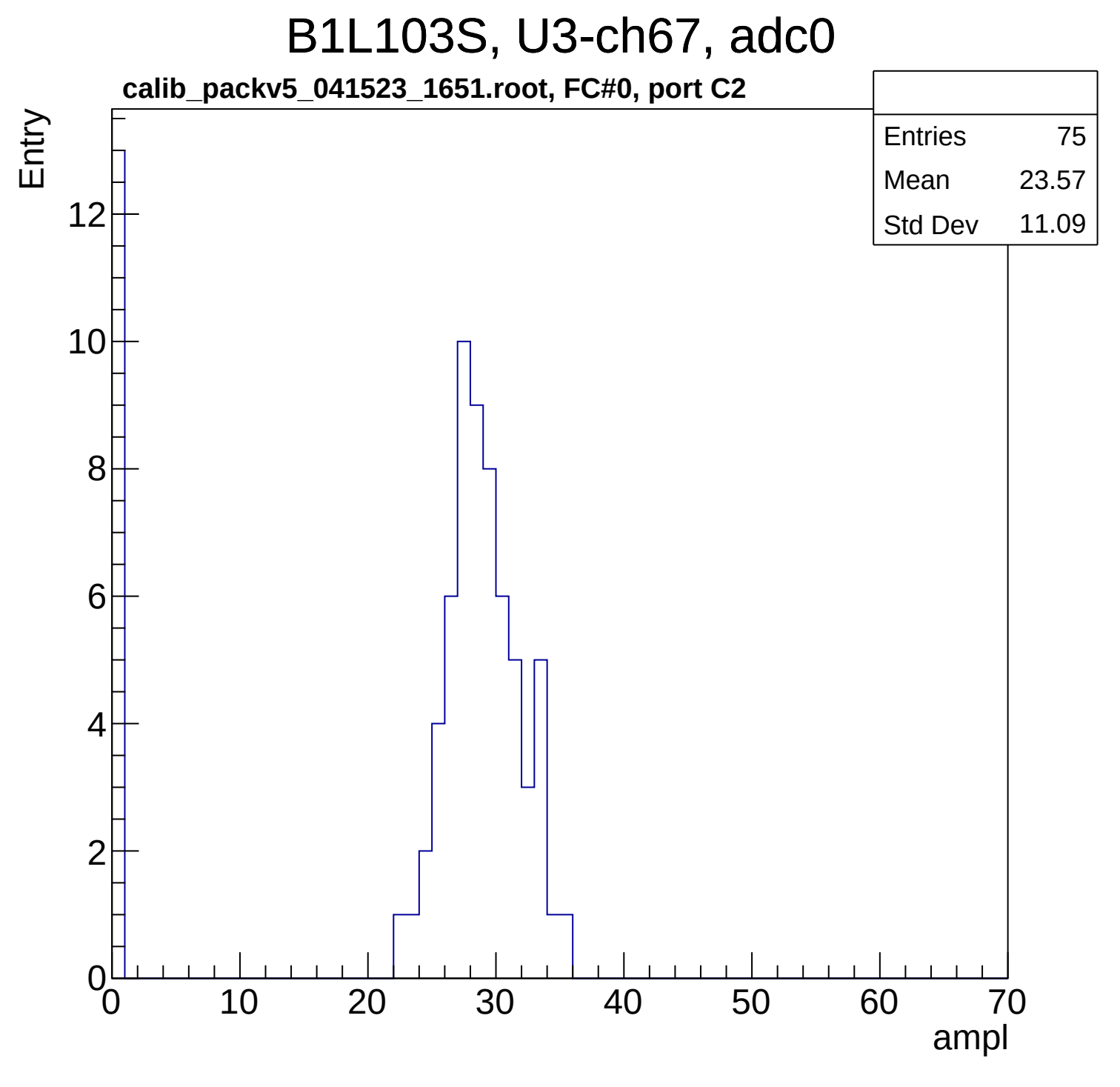
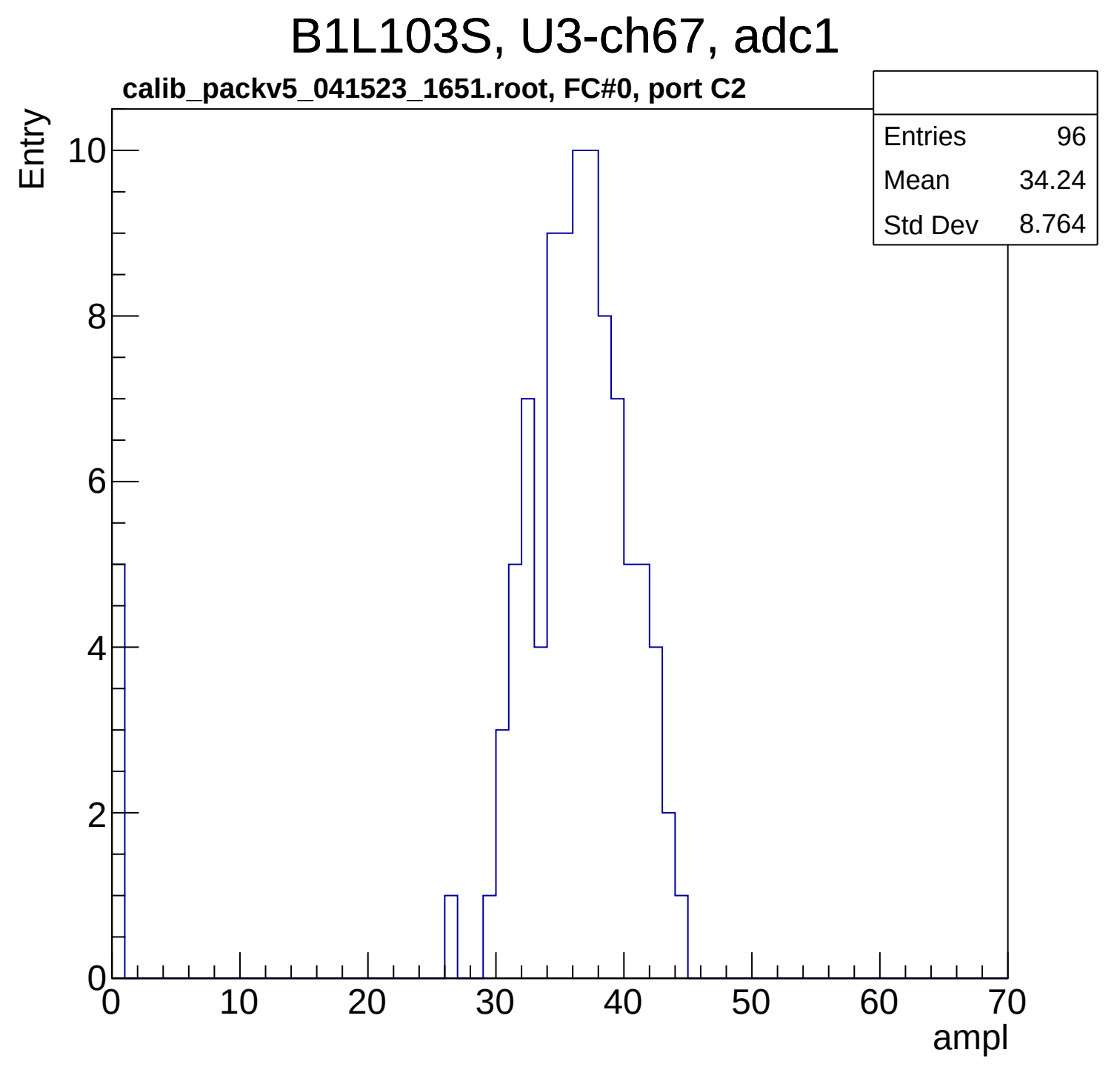
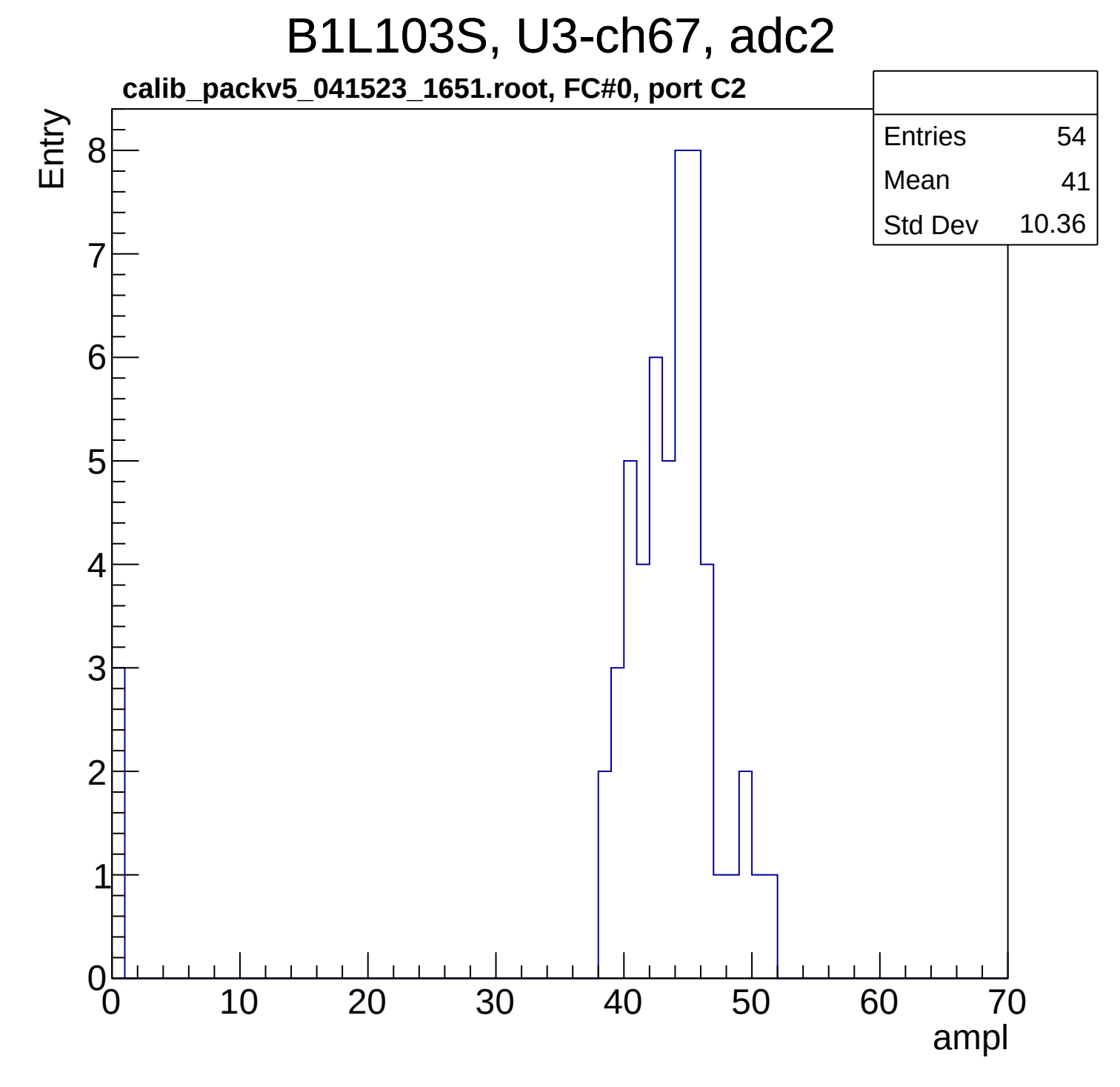
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch67, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 23.57
Std Dev 11.09
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch67, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 96
Mean 34.24
Std Dev 8.764
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U3-ch67, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 41
Std Dev 10.36
Entry
ampl
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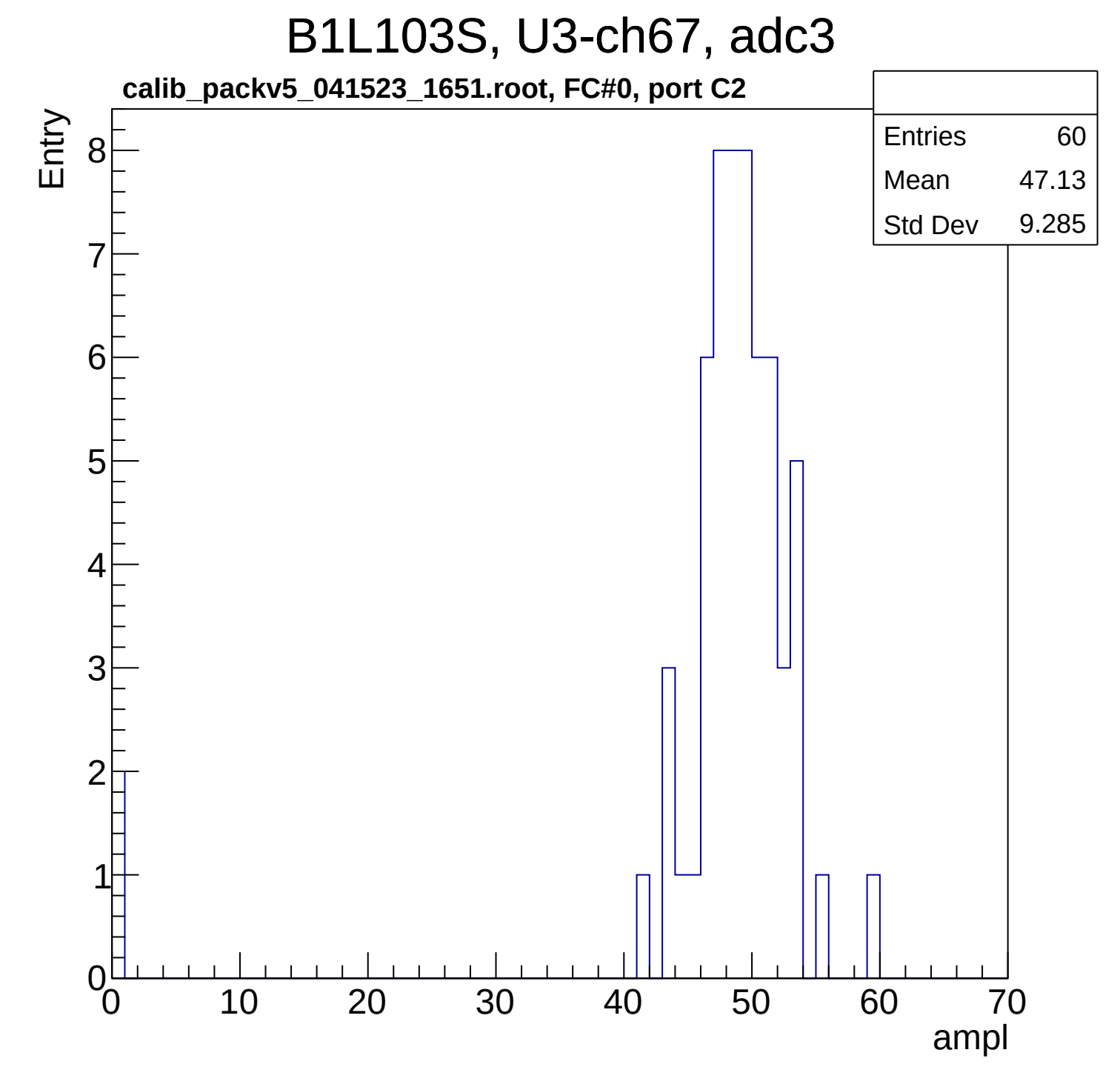
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch67, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 47.13
Std Dev 9.285
Entry
ampl
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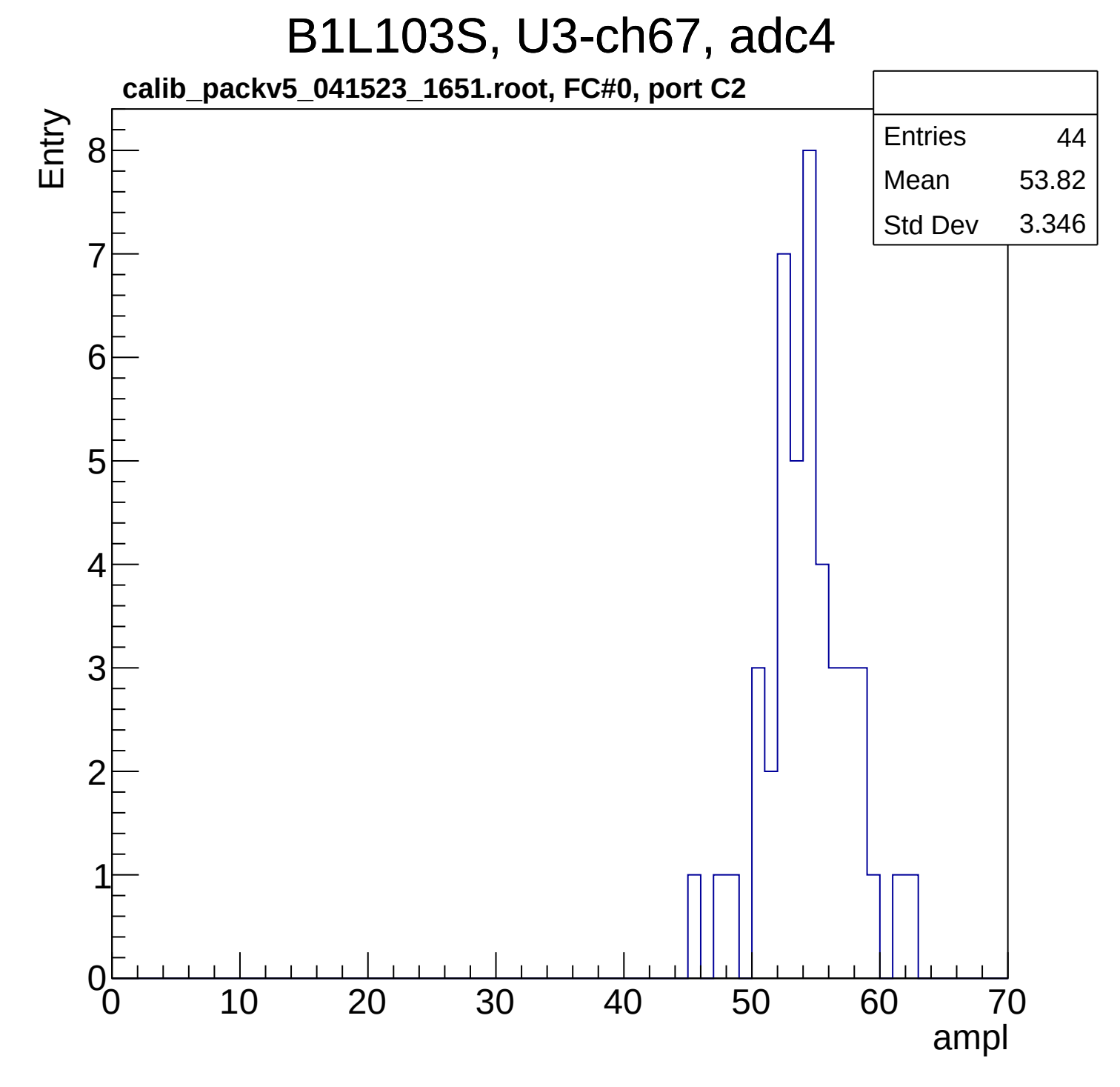
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch67, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 53.82
Std Dev 3.346
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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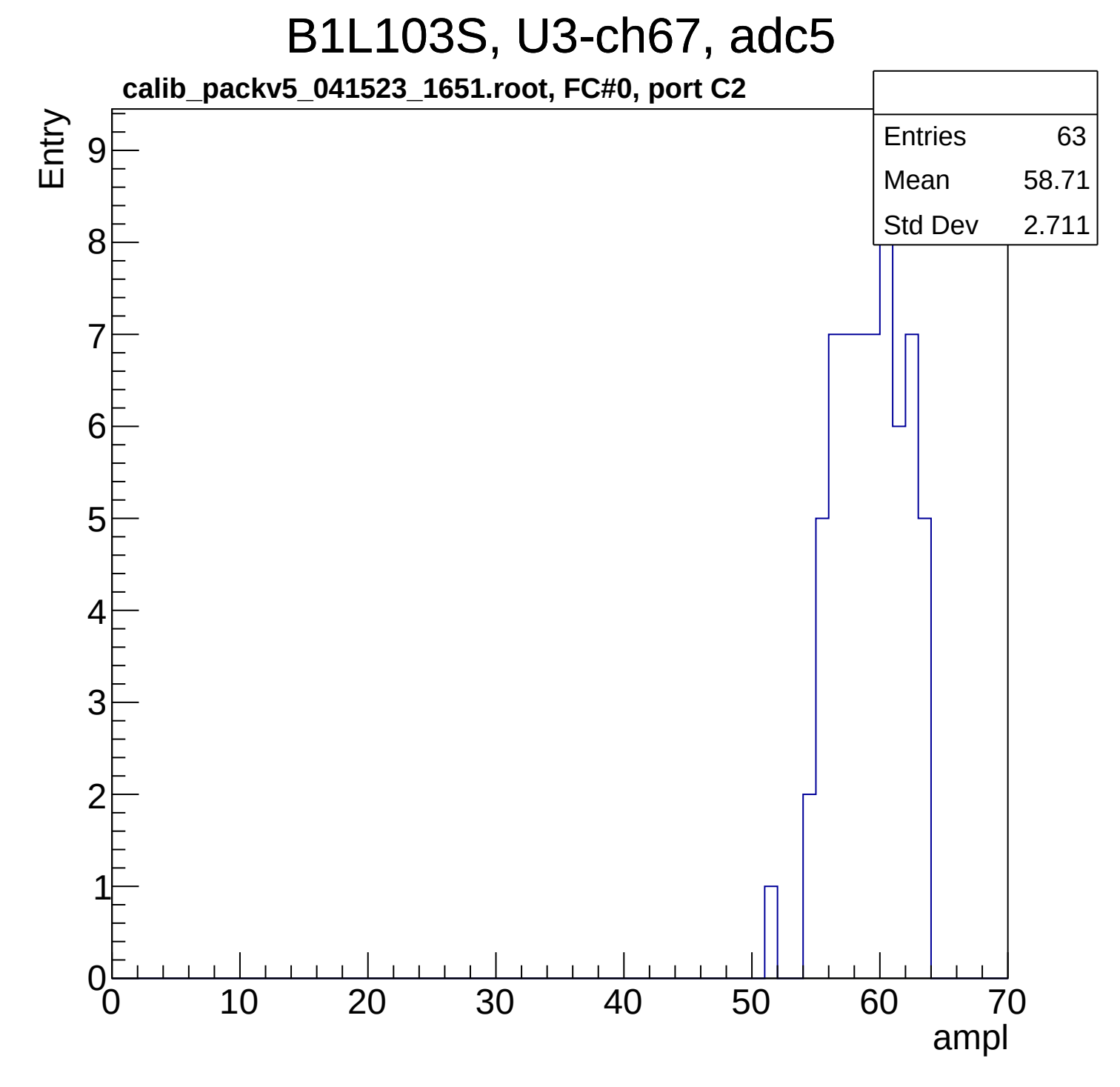
B1L103S, U3-ch67, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 58.71
Std Dev 2.711
Entry
ampl
0
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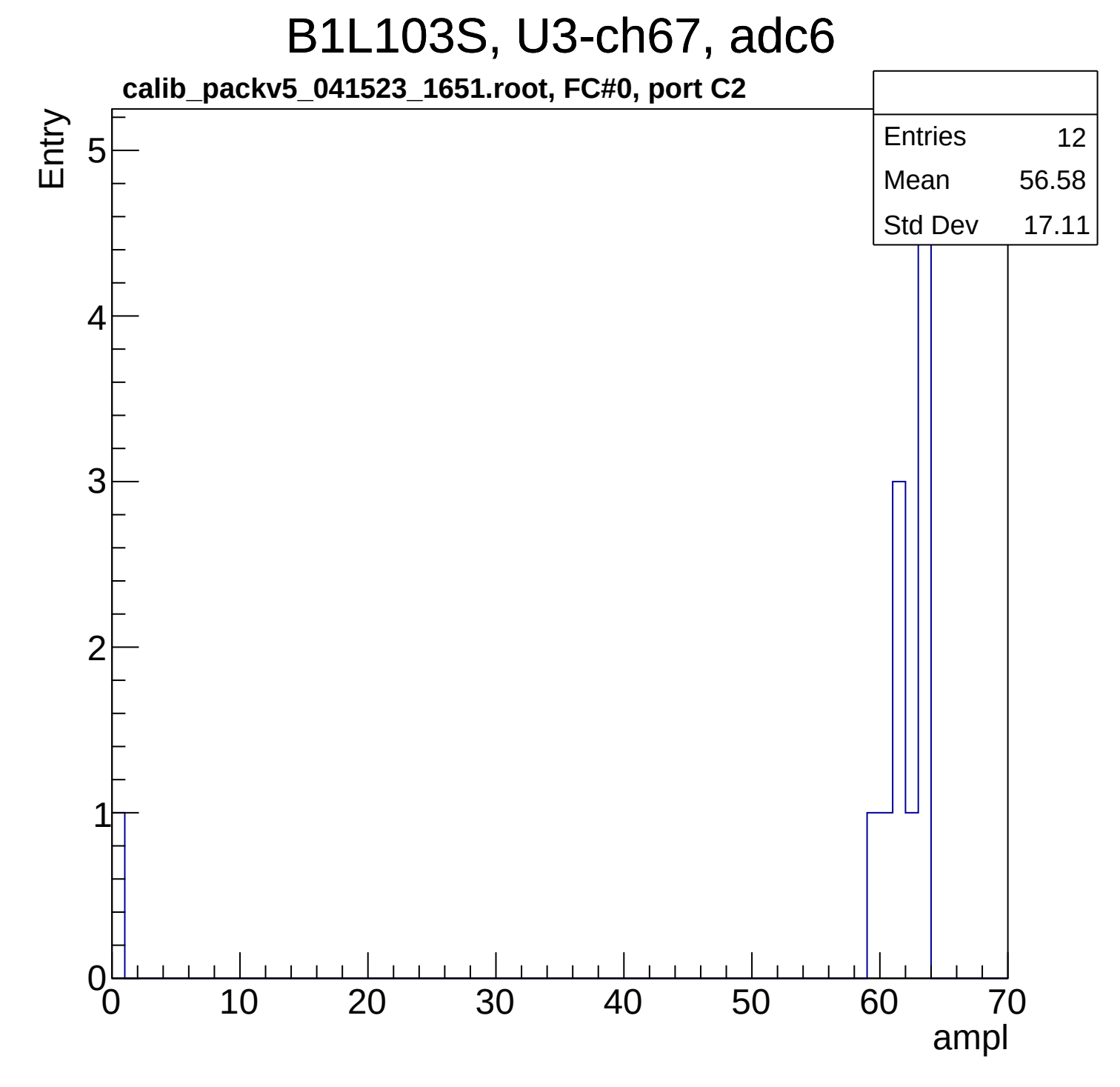
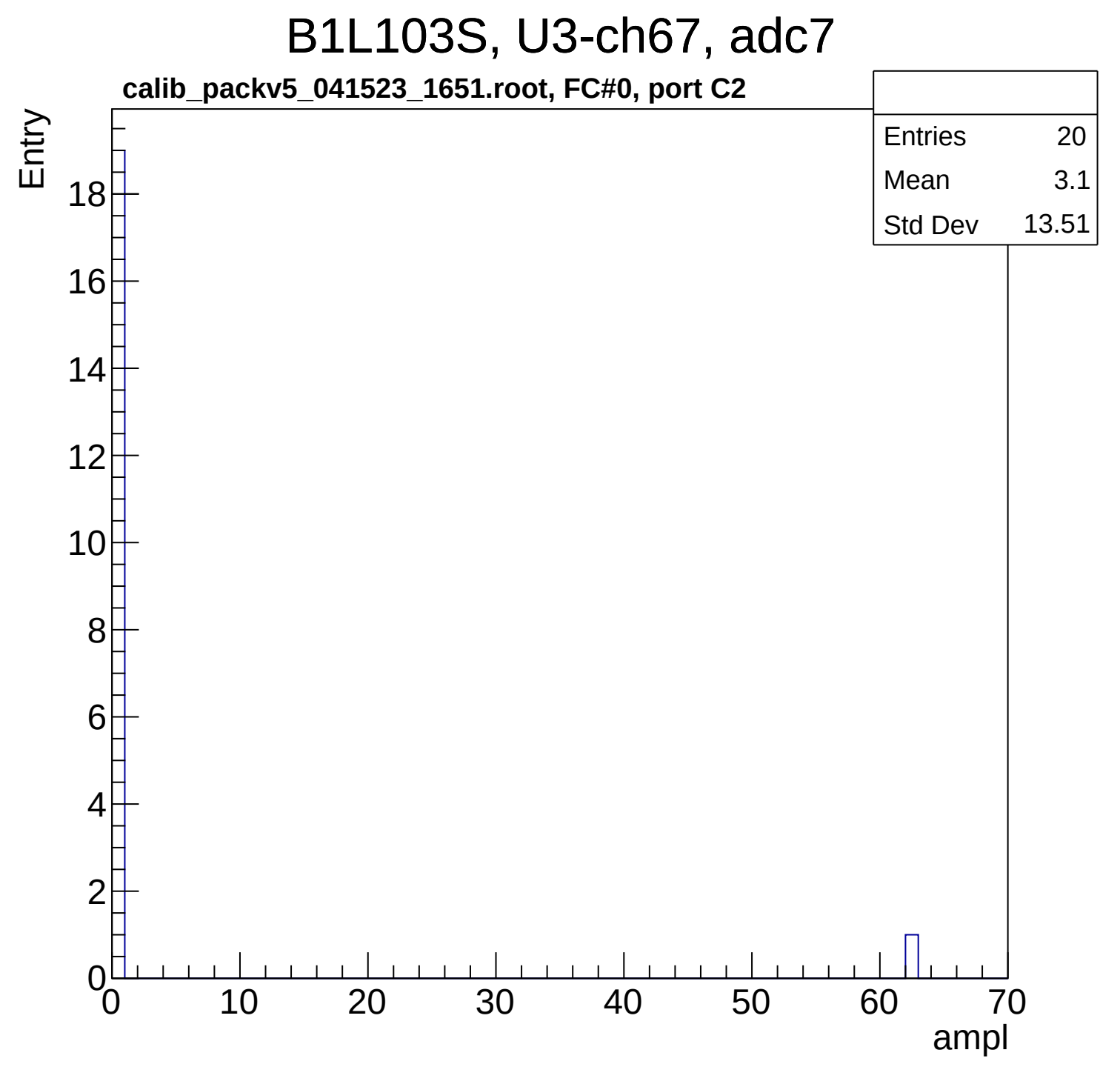
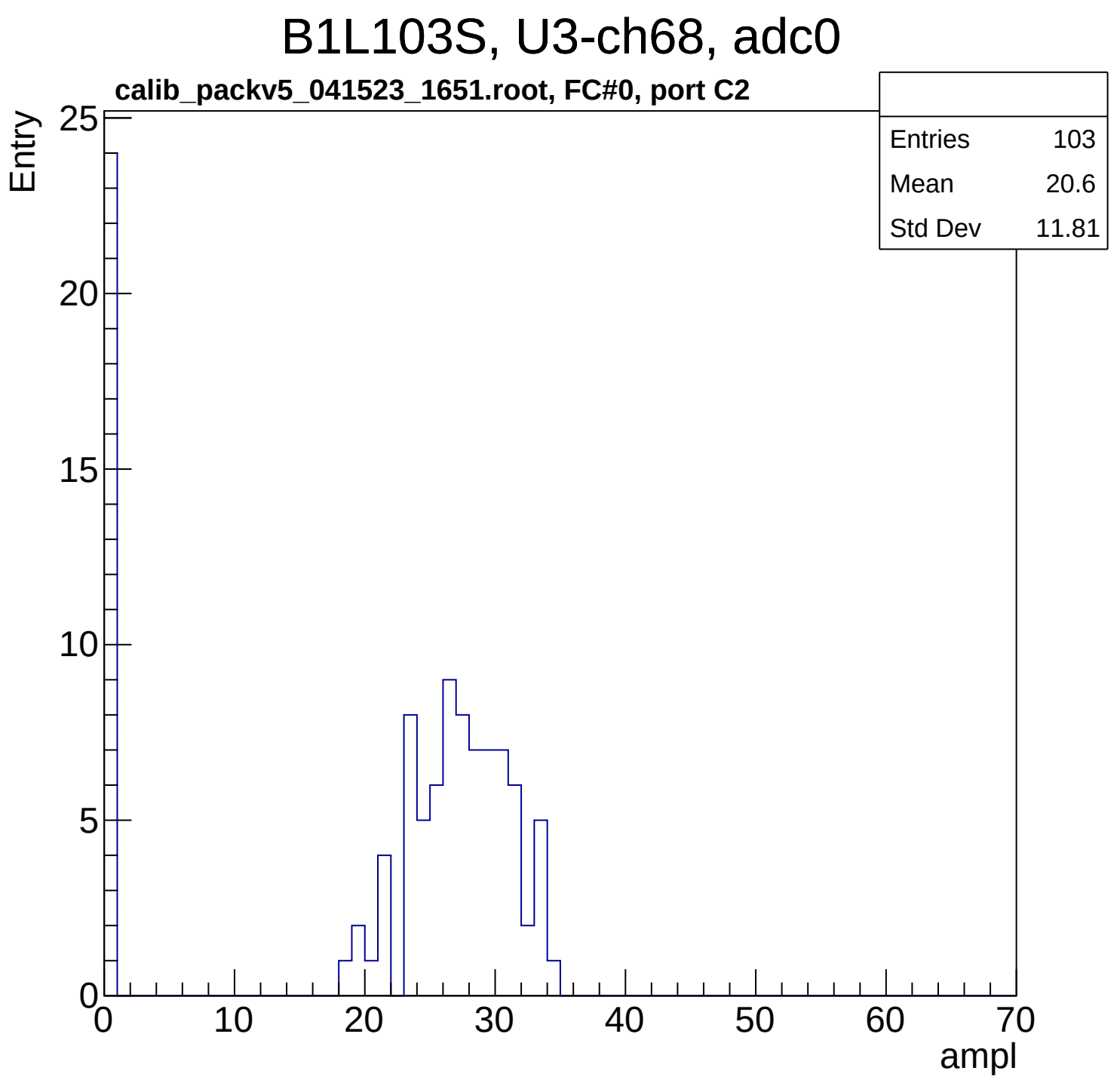
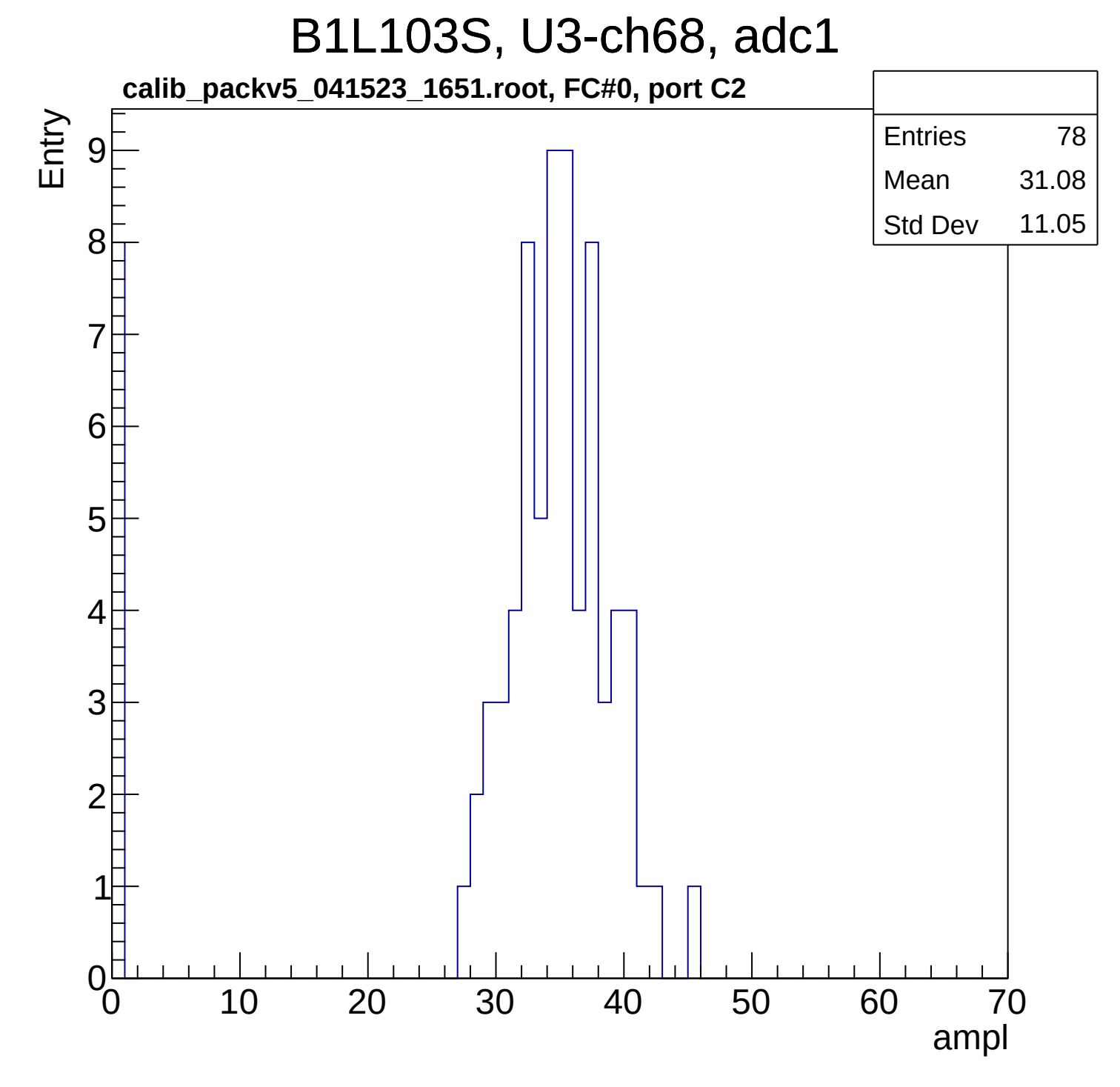
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch67, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 56.58
Std Dev 17.11
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch67, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch68, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 103
Mean 20.6
Std Dev 11.81
Entry
ampl
0
5
10
15
20
25
0
10
20
30
40
50
60
70


B1L103S, U3-ch68, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 31.08
Std Dev 11.05
Entry
ampl
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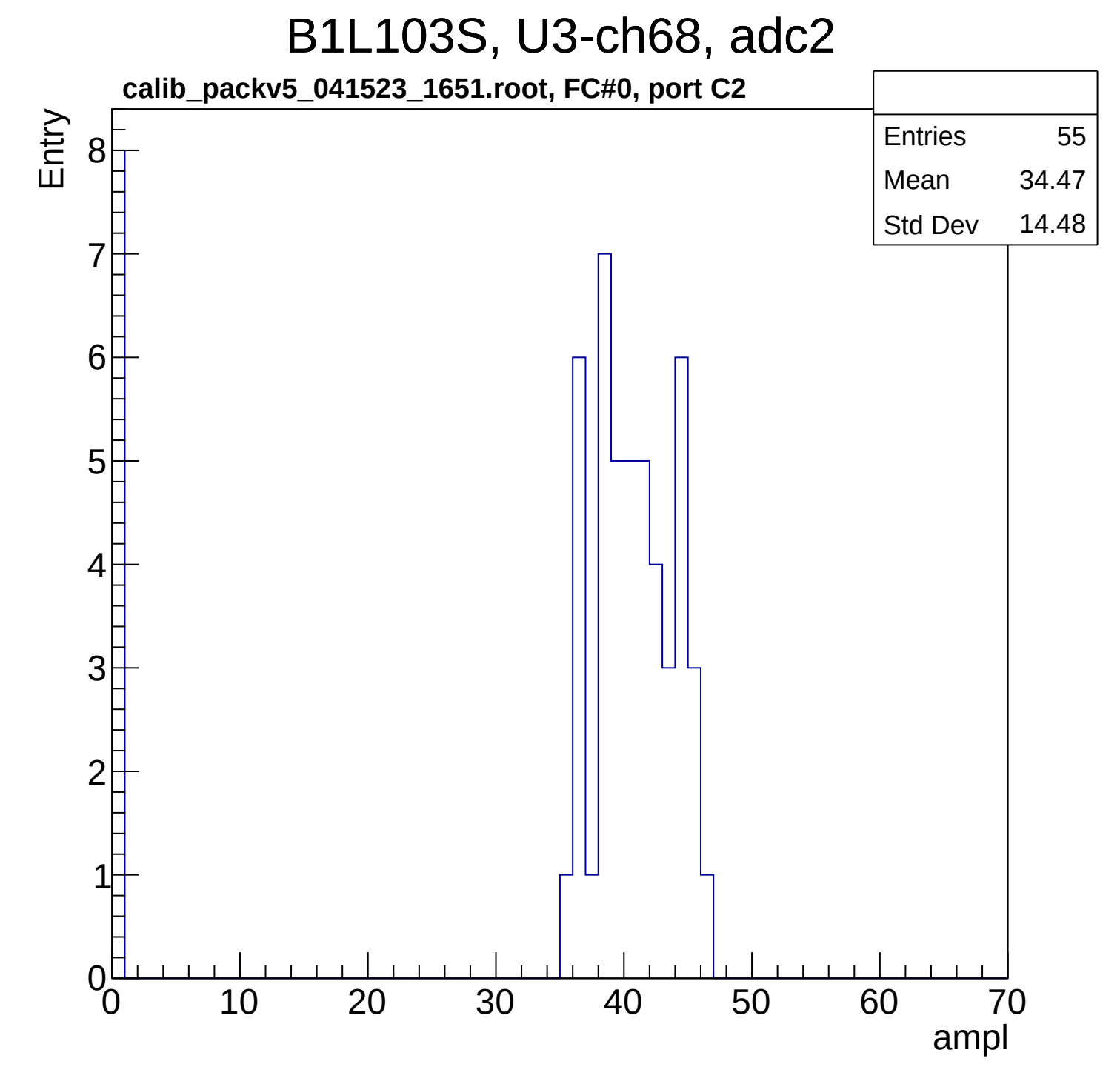
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch68, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 34.47
Std Dev 14.48
Entry
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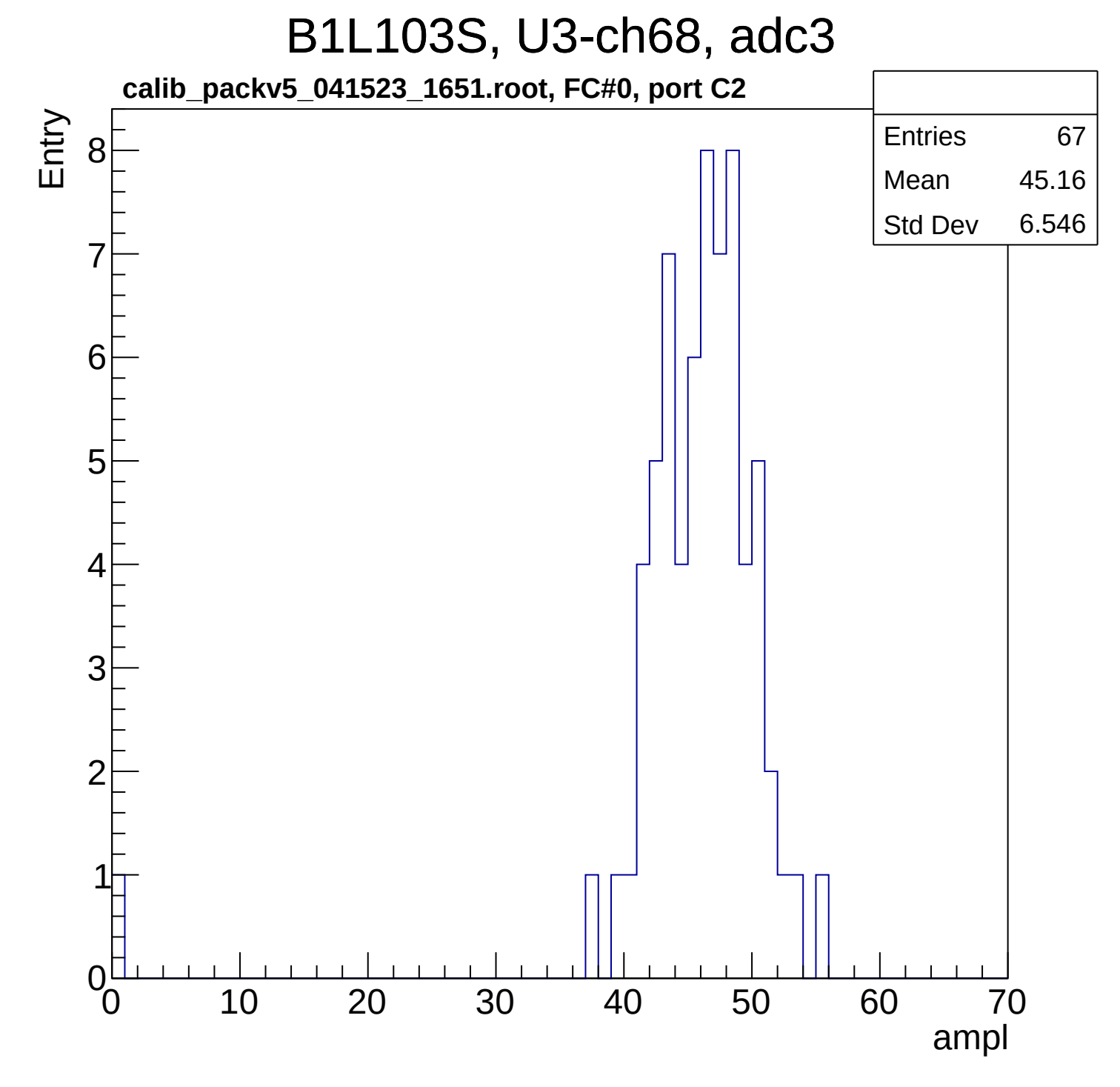
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch68, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 45.16
Std Dev 6.546
Entry
ampl
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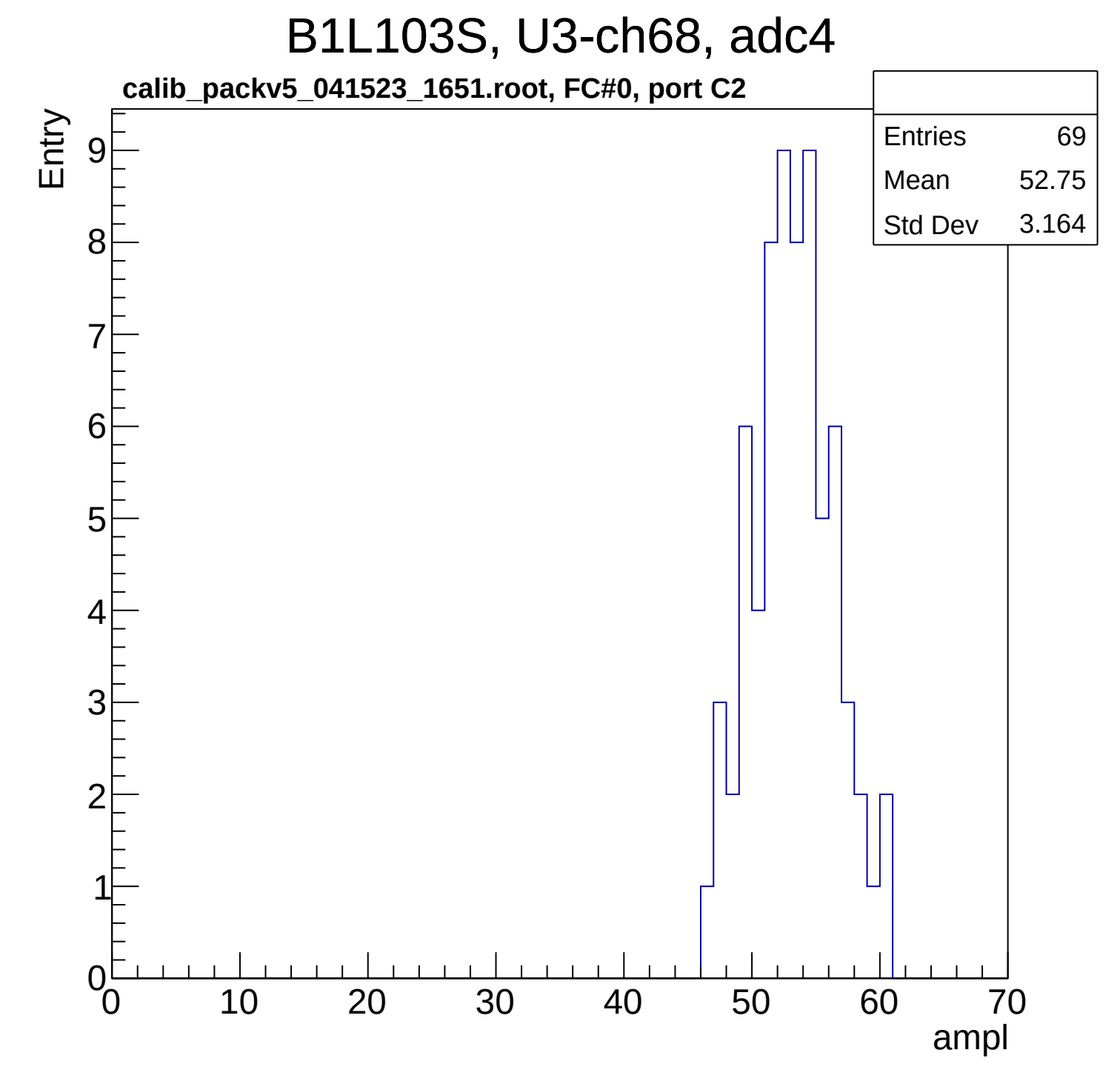
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch68, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 52.75
Std Dev 3.164
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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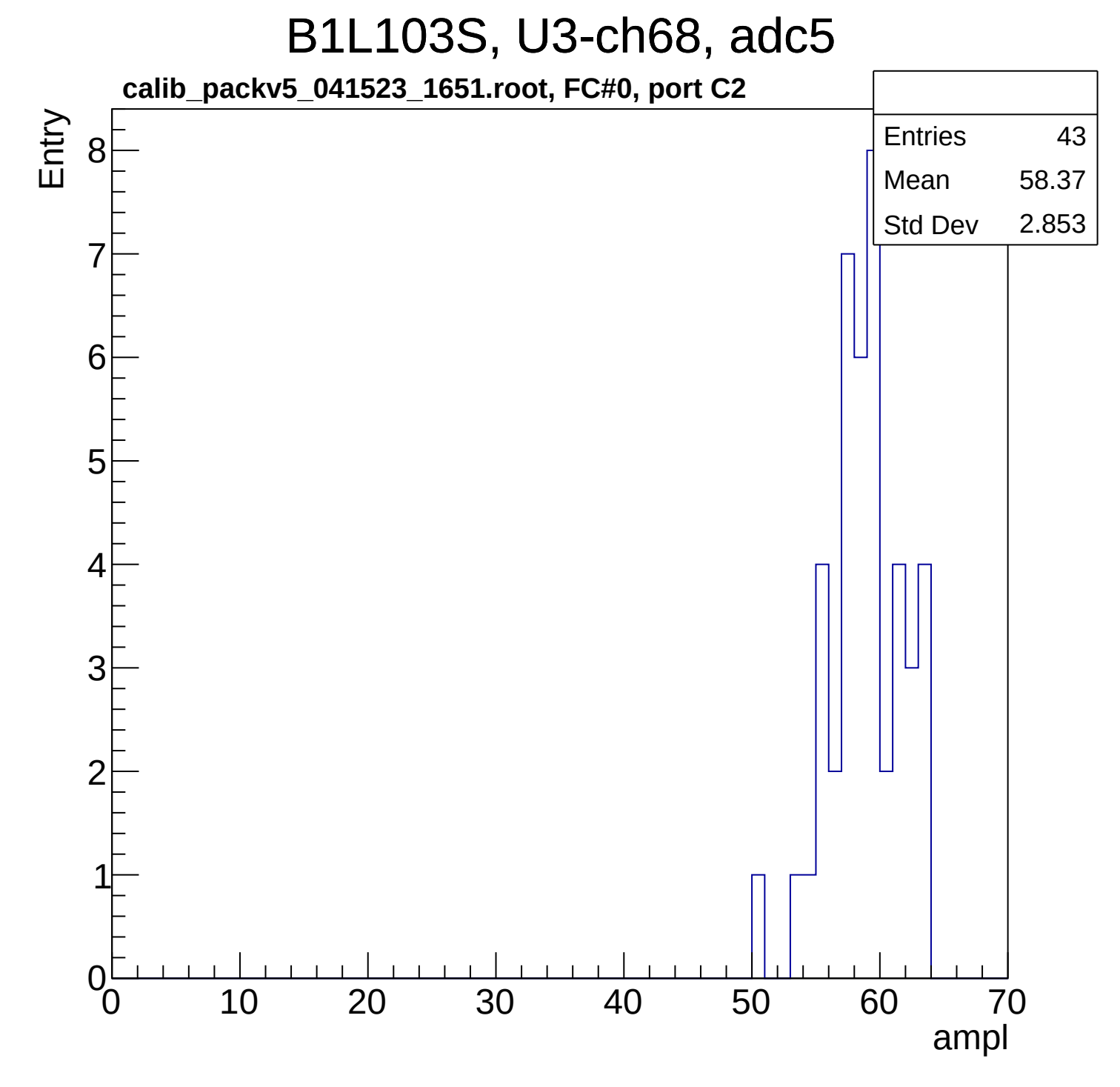
B1L103S, U3-ch68, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 58.37
Std Dev 2.853
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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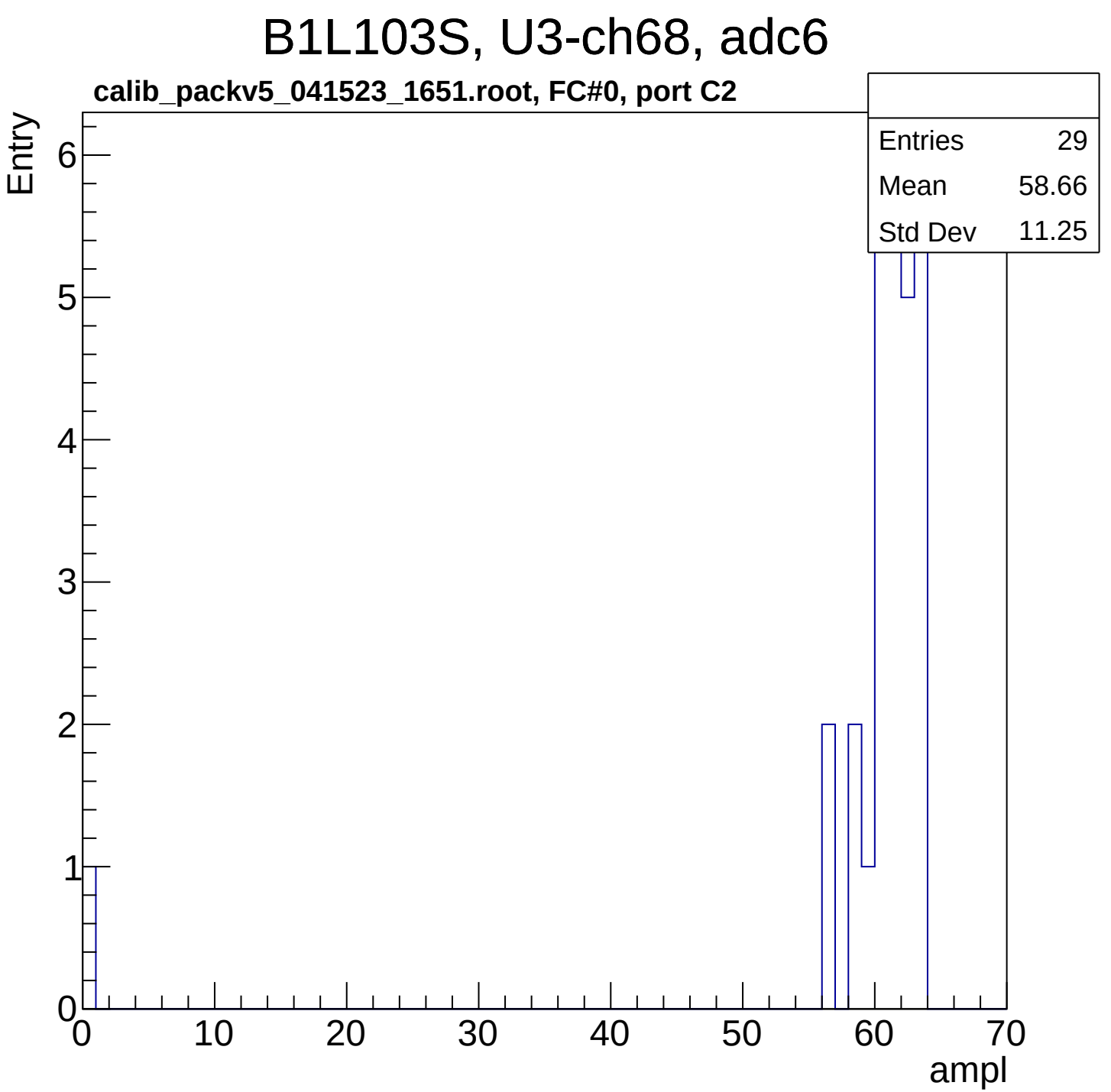
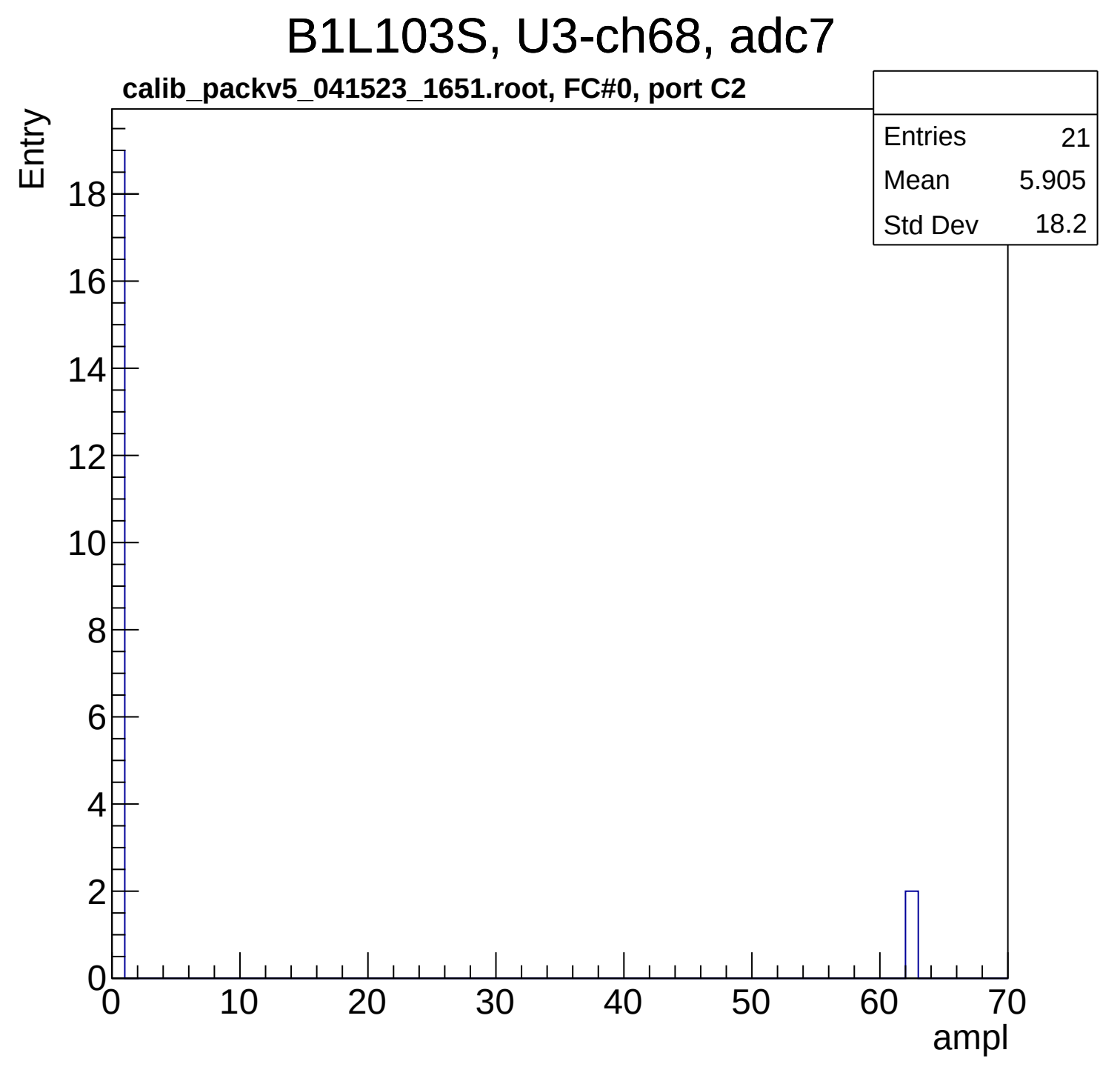
40
50
60
70


B1L103S, U3-ch68, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 58.66
Std Dev 11.25
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch68, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.905
Std Dev 18.2
Entry
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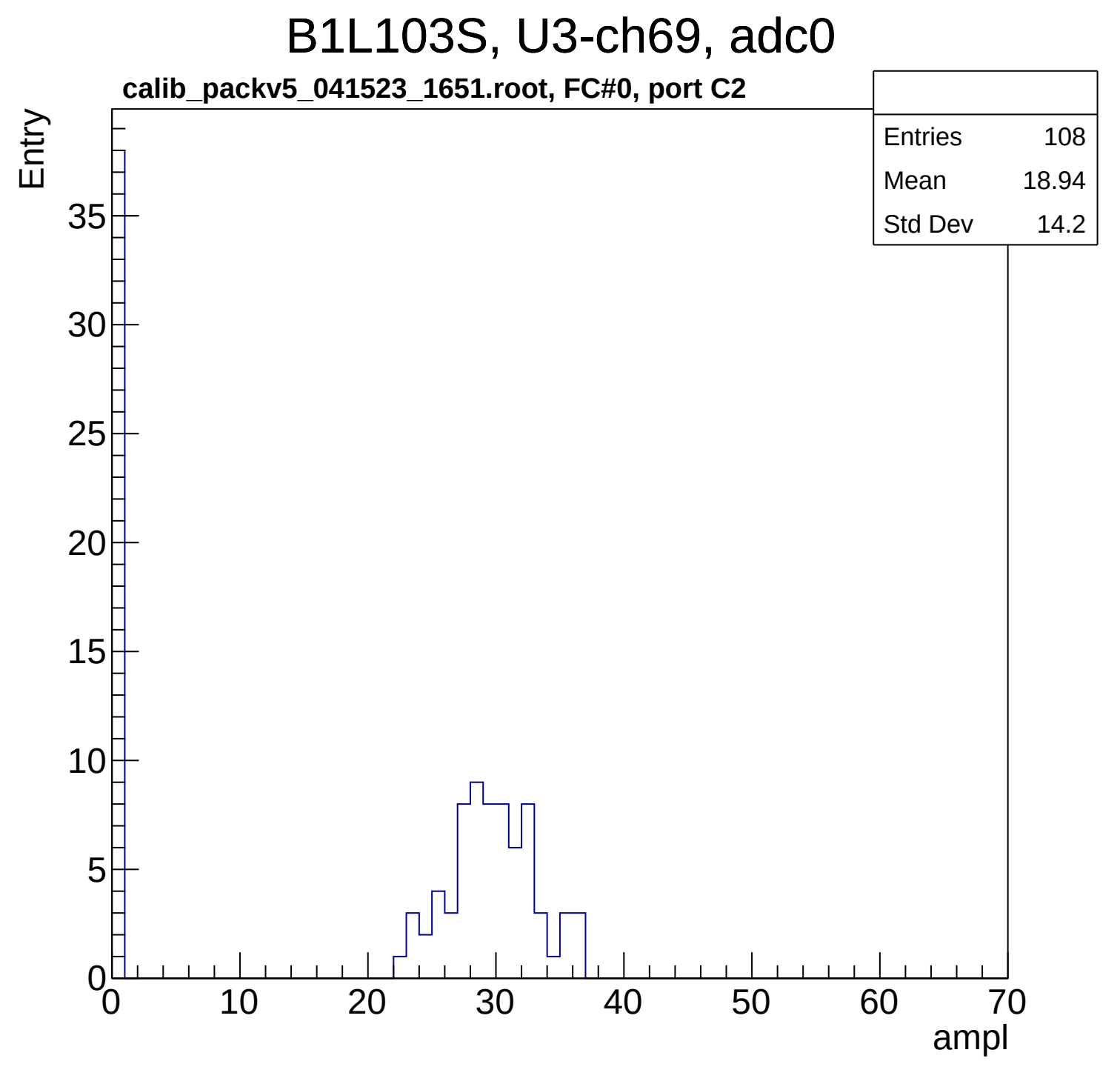
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch69, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 108
Mean 18.94
Std Dev 14.2
Entry
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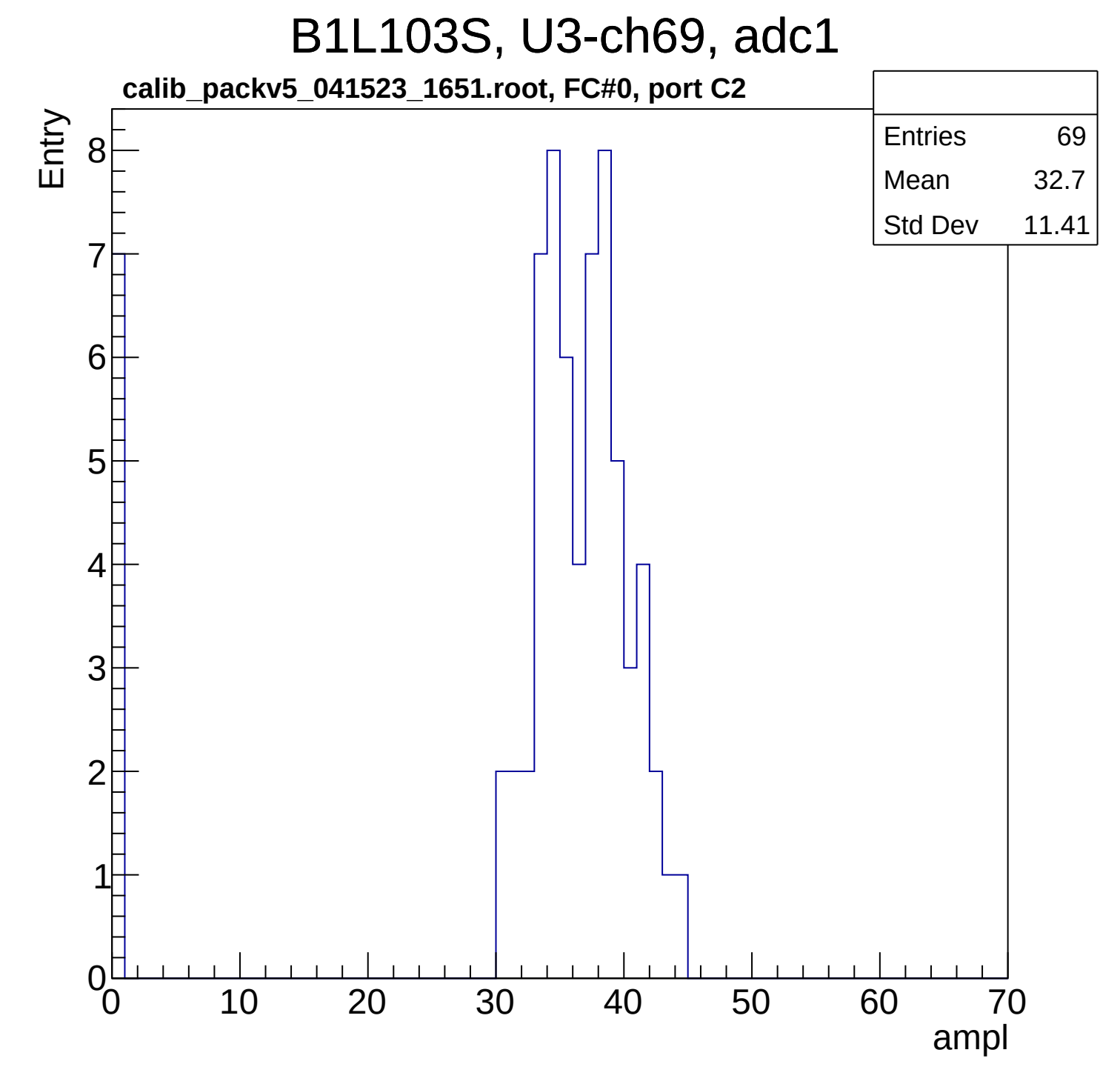
5
10
15
20
25
30
35
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch69, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 32.7
Std Dev 11.41
Entry
ampl
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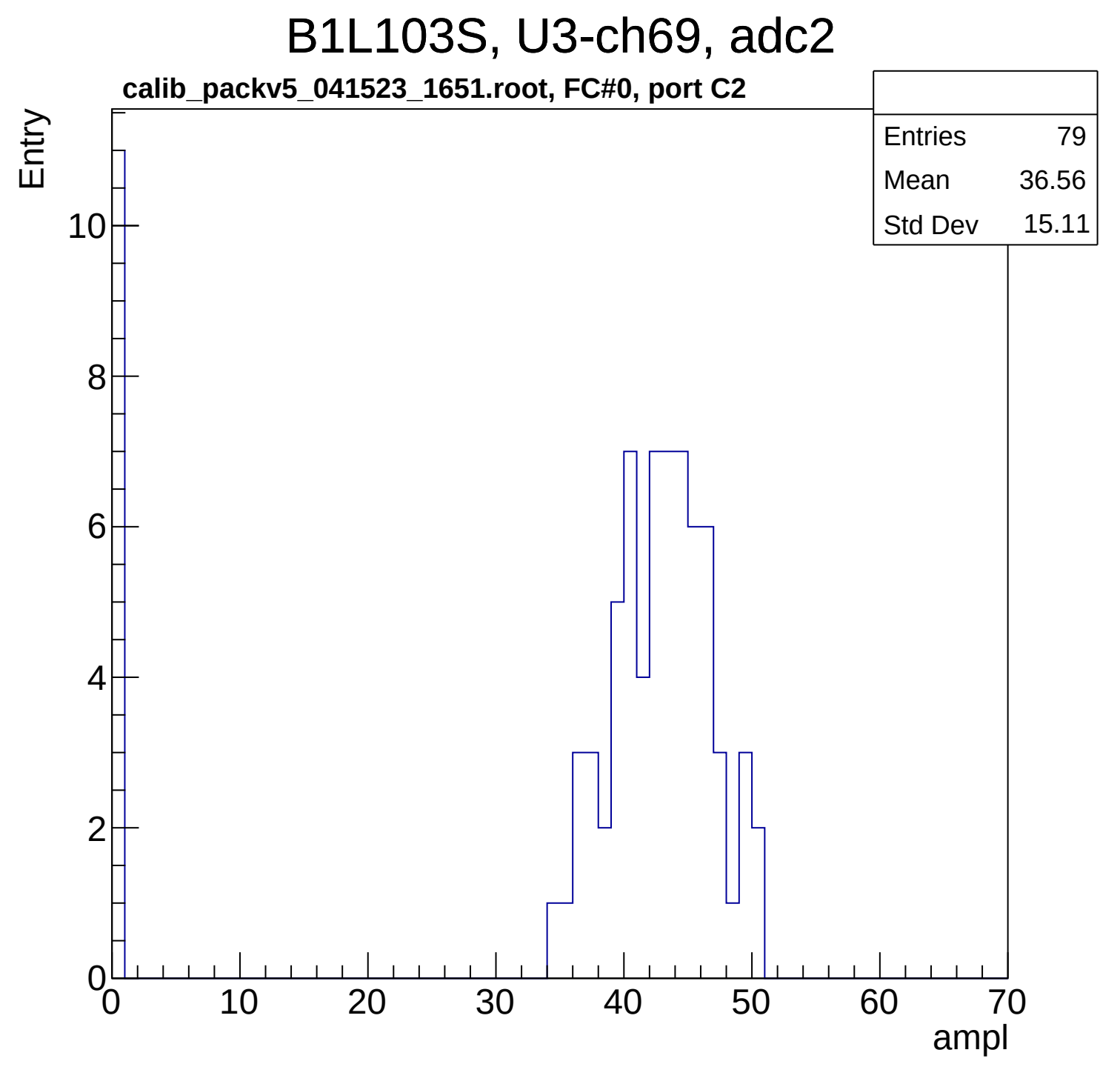
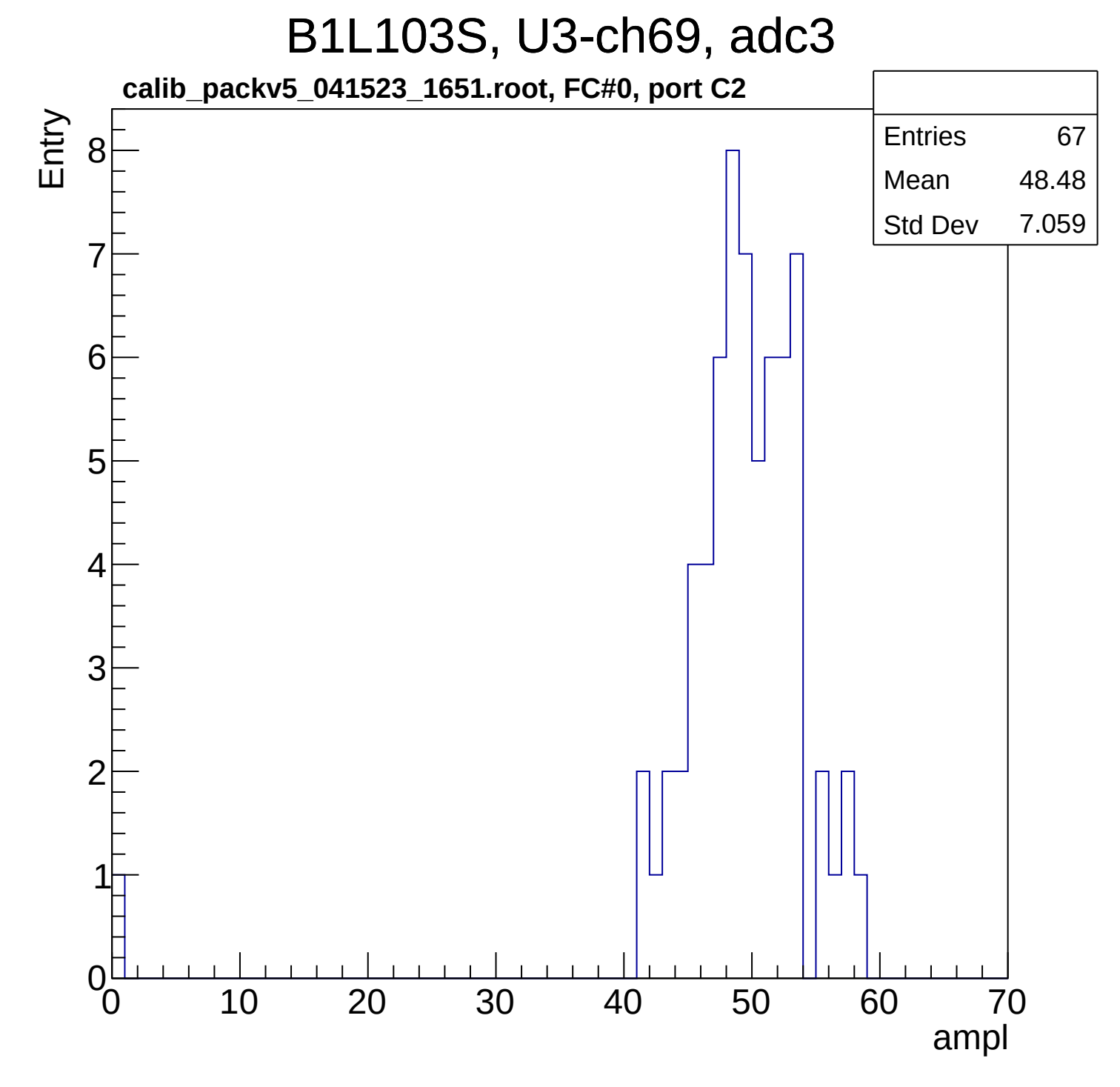
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch69, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 36.56
Std Dev 15.11
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch69, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 48.48
Std Dev 7.059
Entry
ampl
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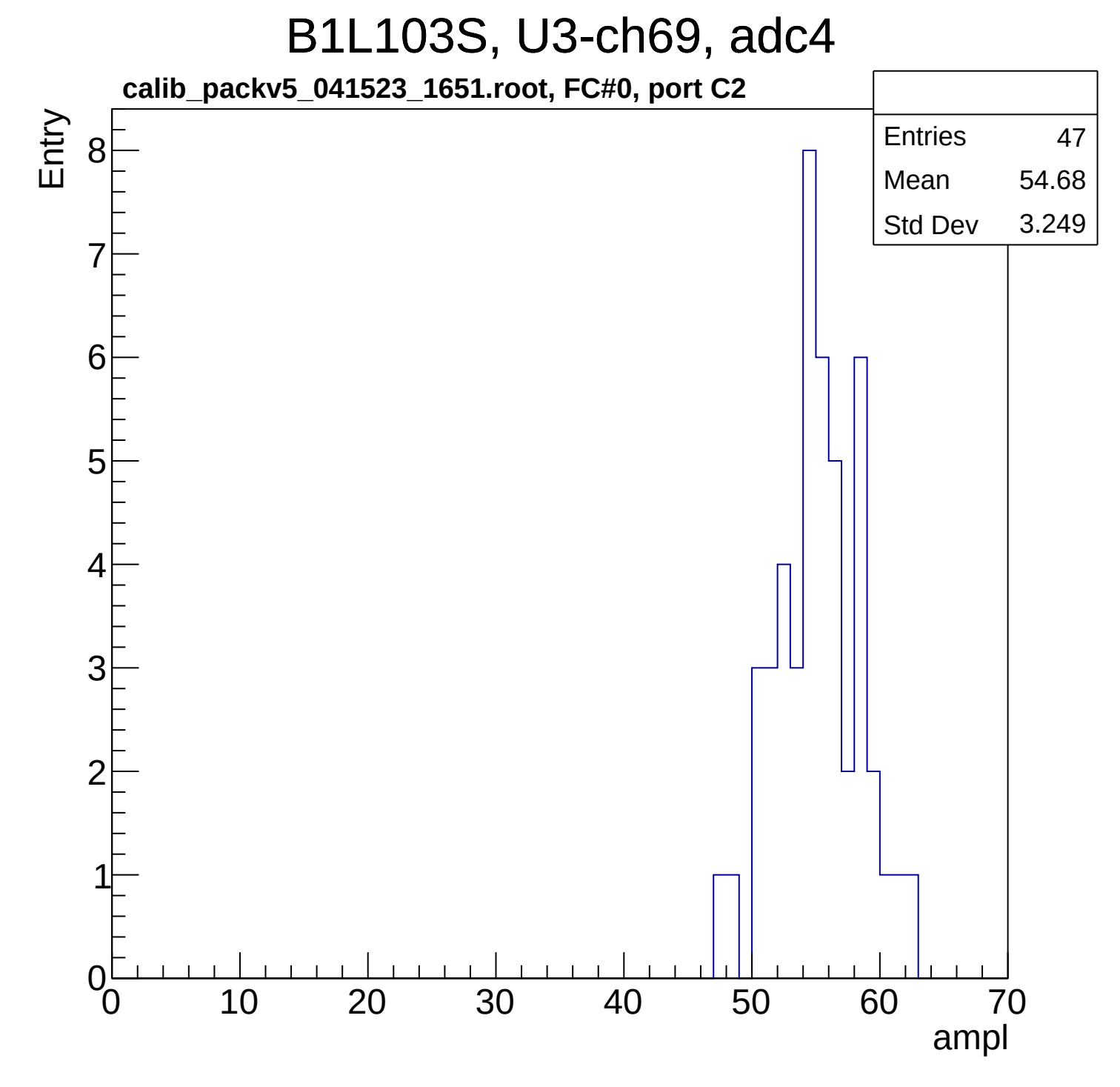
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch69, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 54.68
Std Dev 3.249
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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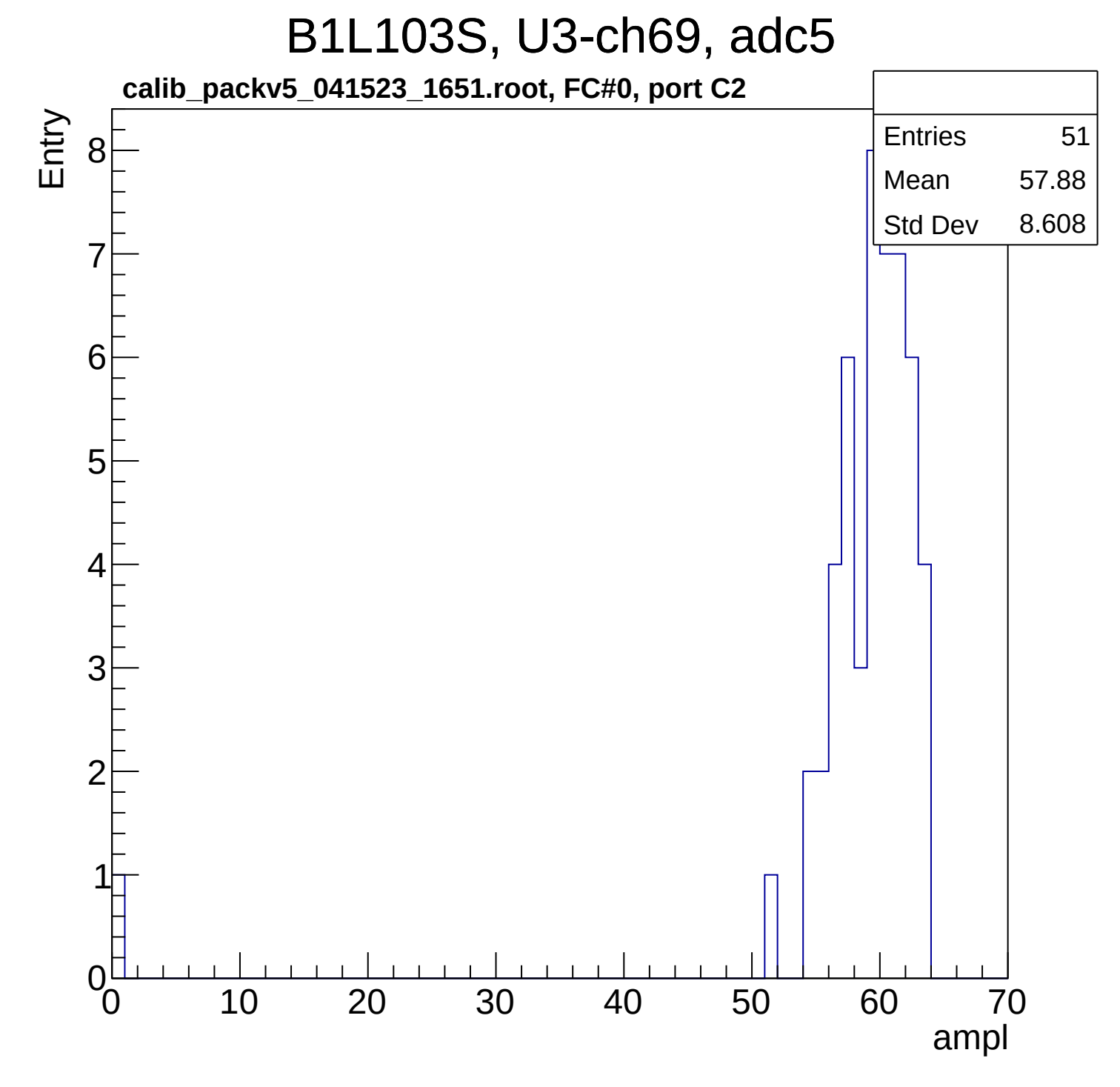
B1L103S, U3-ch69, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 57.88
Std Dev 8.608
Entry
ampl
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2
3
4
5
6
7
8
0
10
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30
40
50
60
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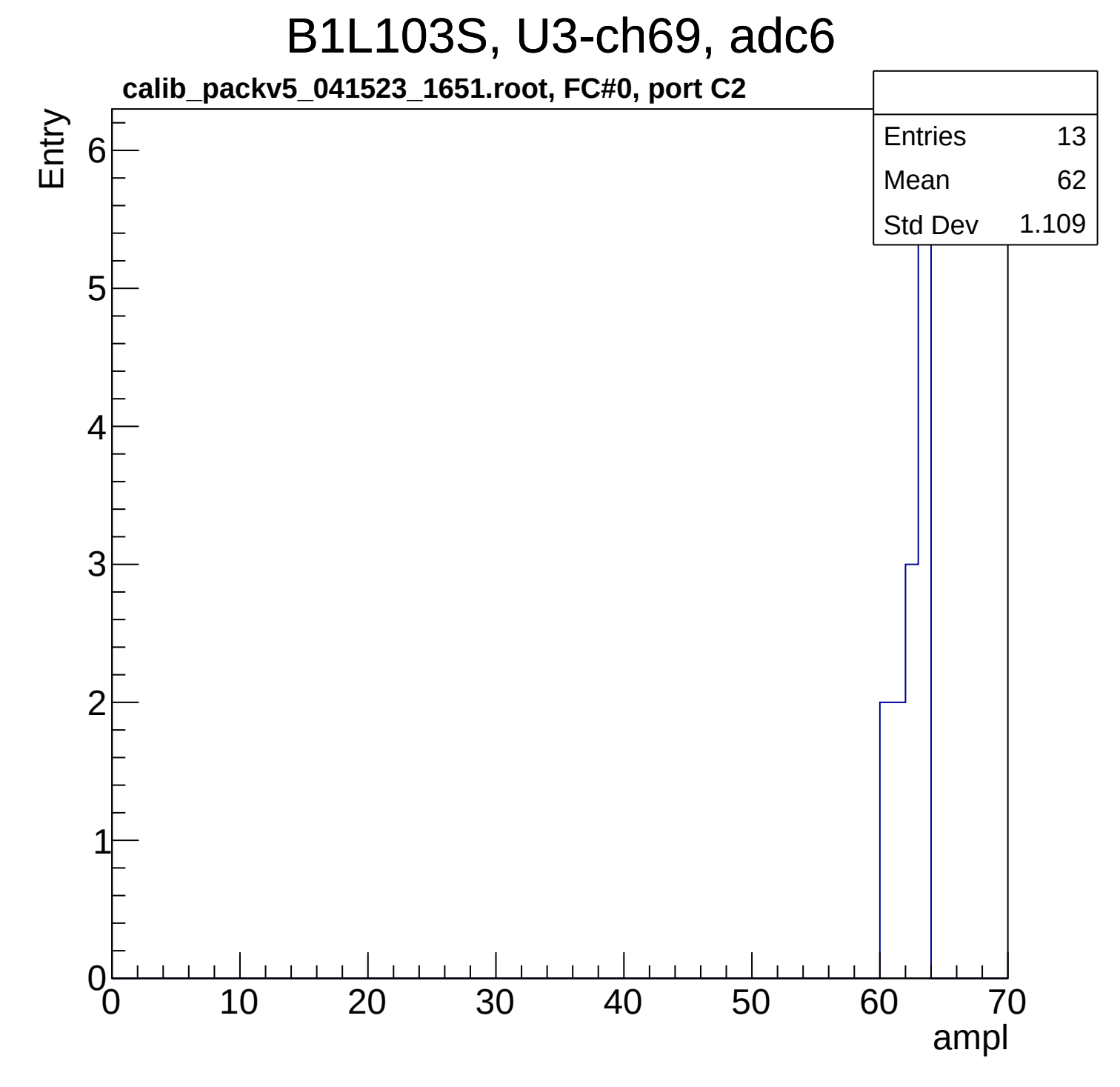
B1L103S, U3-ch69, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 62
Std Dev 1.109
Entry
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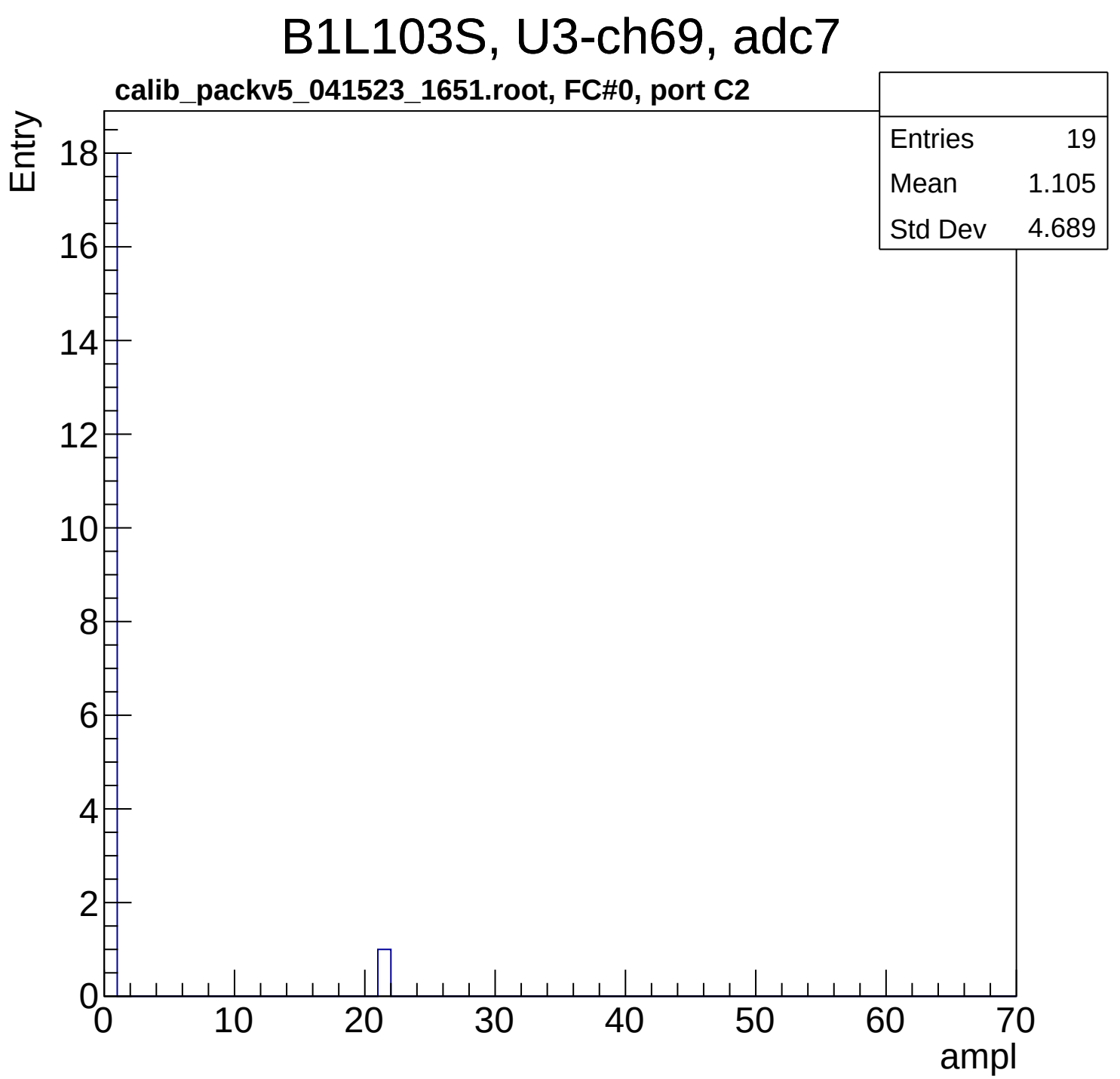
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch69, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.105
Std Dev 4.689
Entry
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6
8
10
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14
16
18
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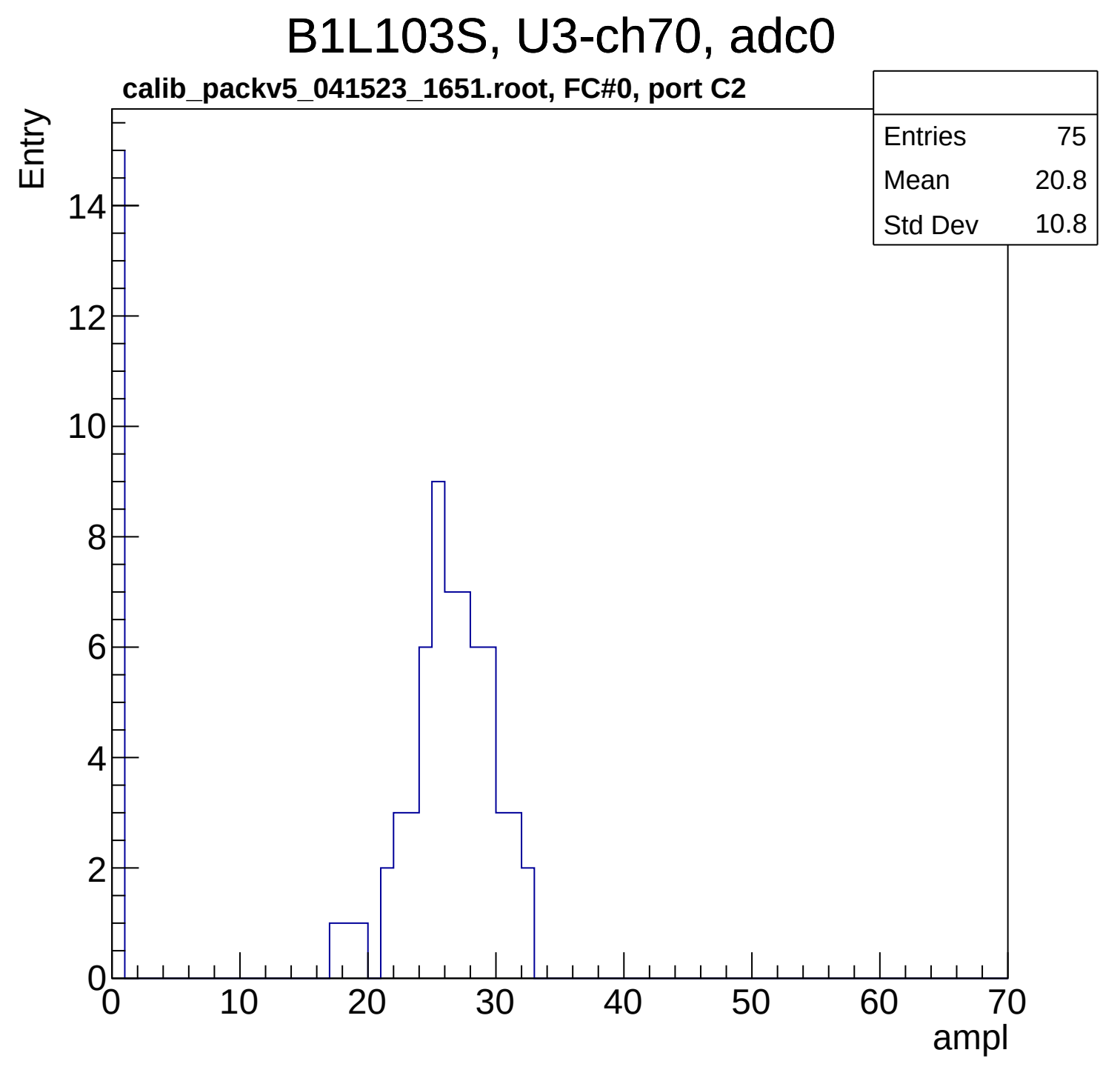
70
ampl


B1L103S, U3-ch70, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 20.8
Std Dev 10.8
Entry
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6
8
10
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14
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10
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50
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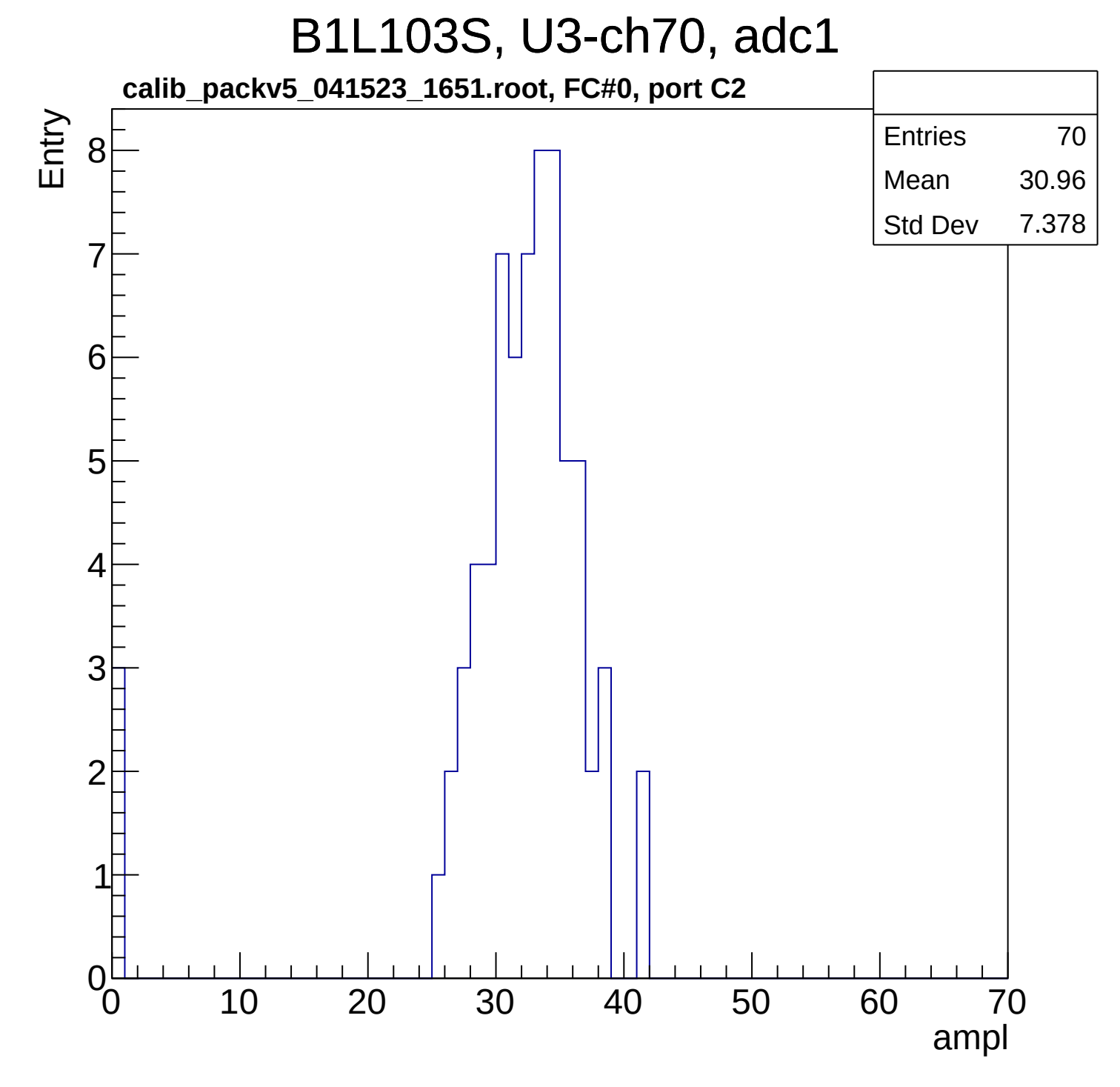
70
ampl


B1L103S, U3-ch70, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 30.96
Std Dev 7.378
Entry
ampl
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7
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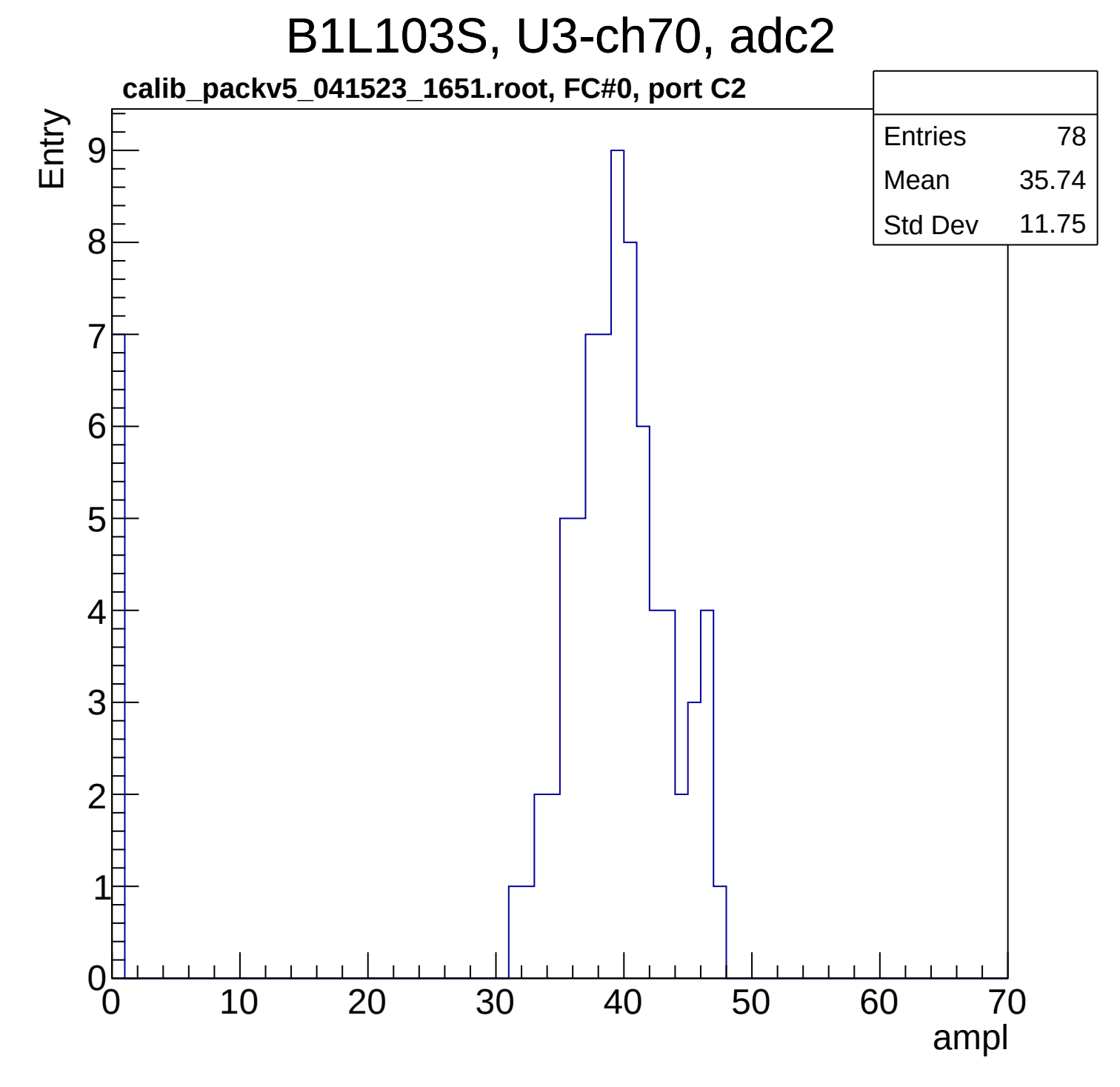
B1L103S, U3-ch70, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 35.74
Std Dev 11.75
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
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60
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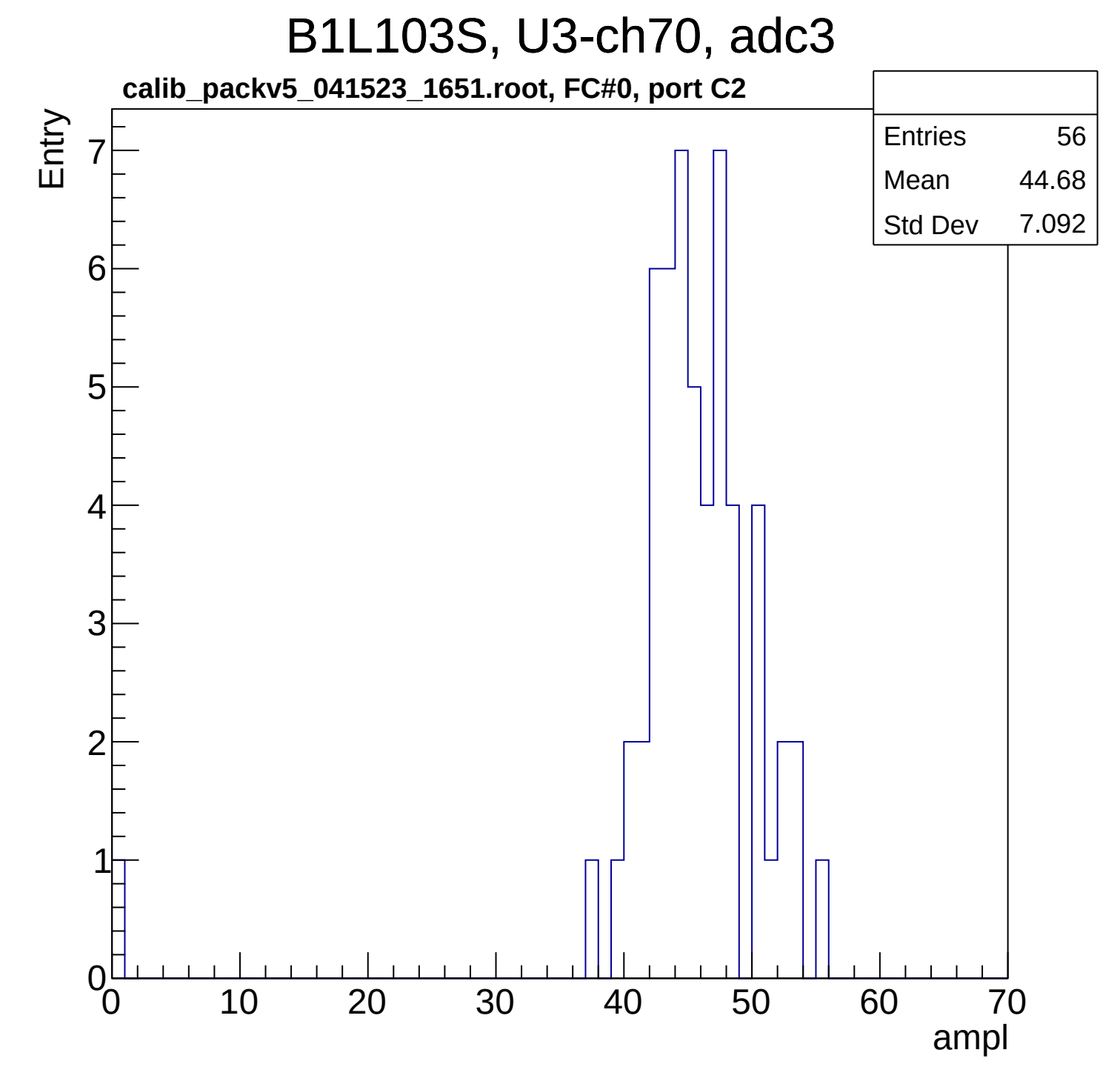
B1L103S, U3-ch70, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 44.68
Std Dev 7.092
Entry
ampl
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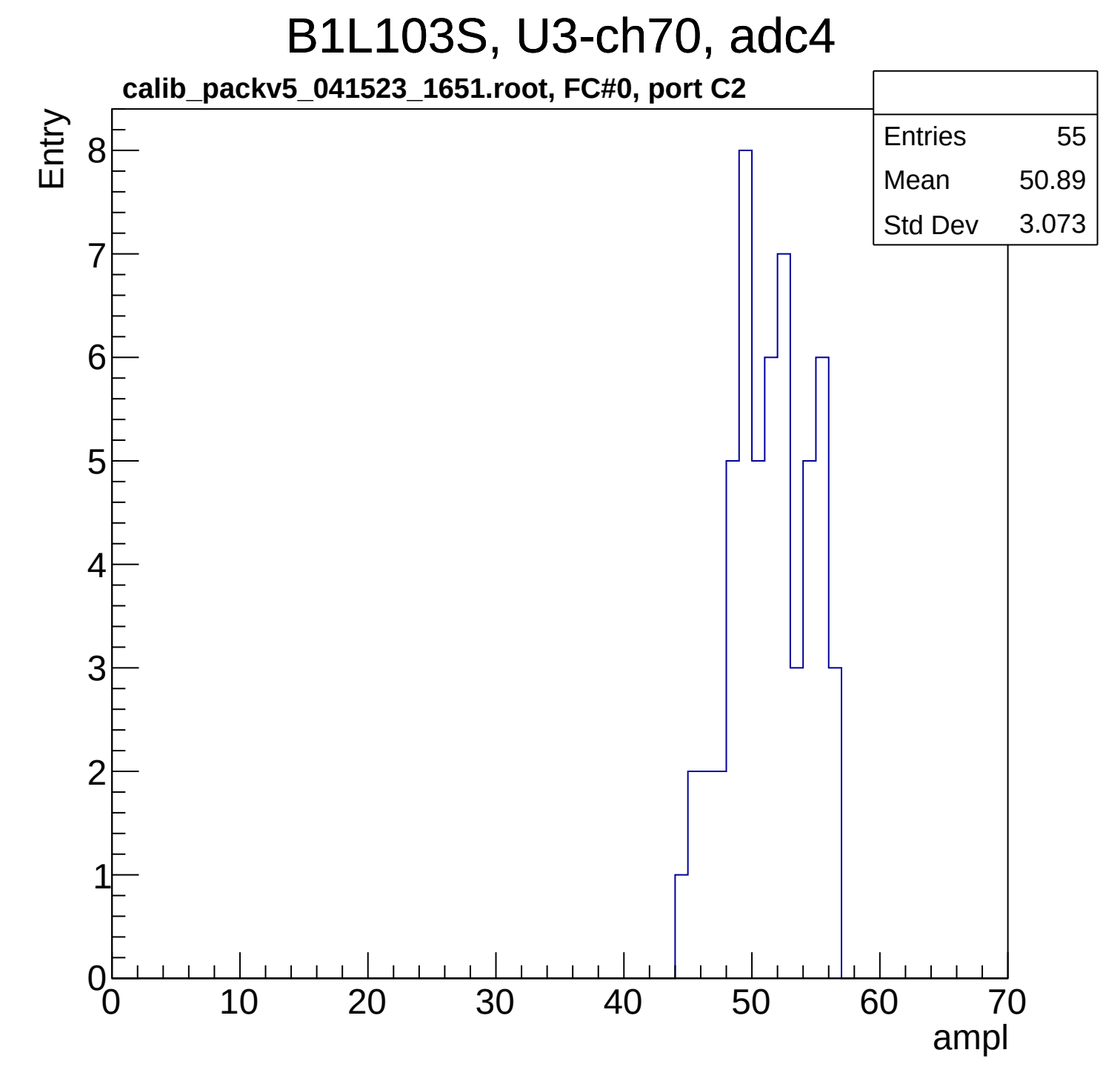
B1L103S, U3-ch70, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 50.89
Std Dev 3.073
Entry
ampl
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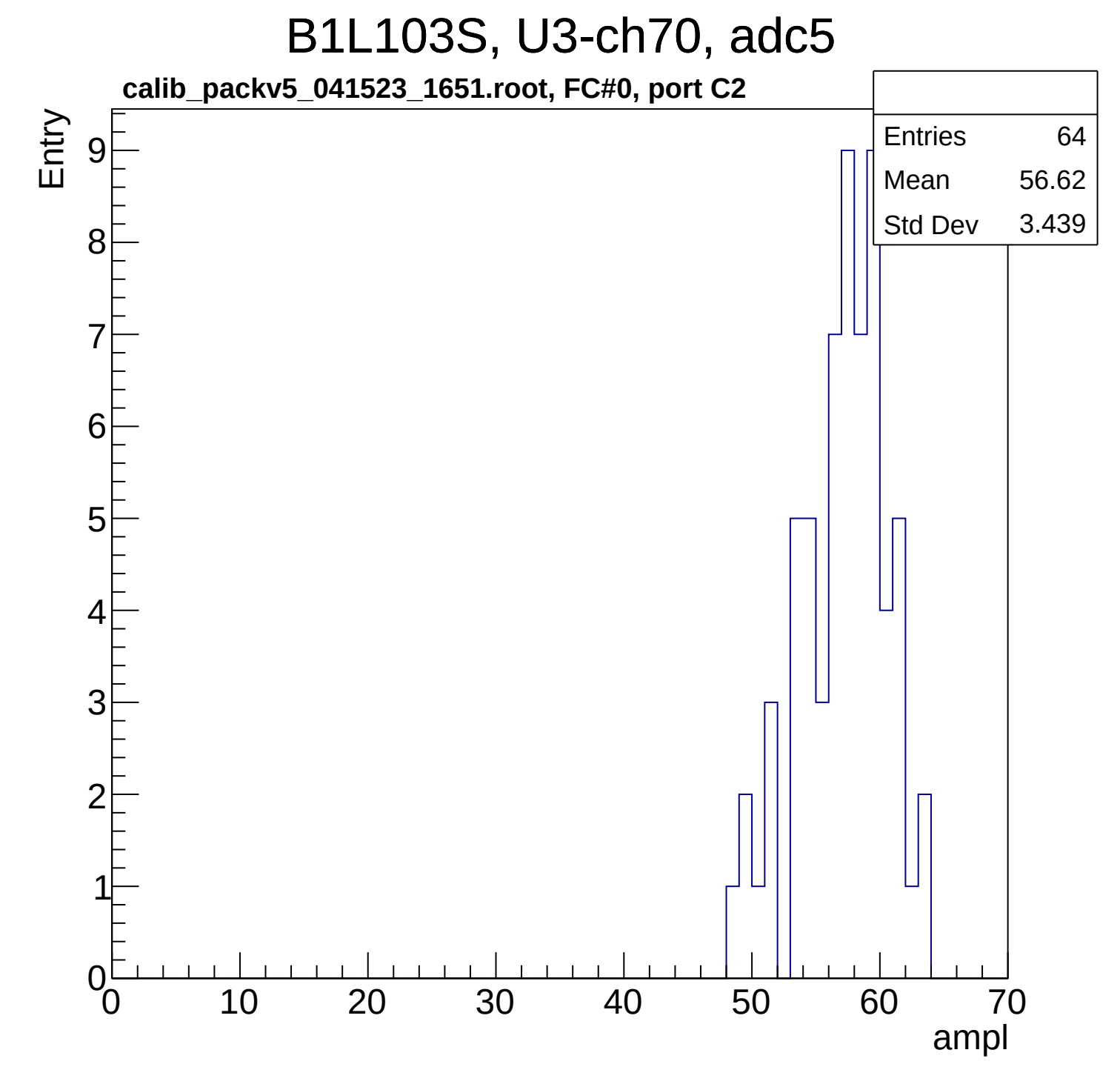
B1L103S, U3-ch70, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 56.62
Std Dev 3.439
Entry
ampl
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3
4
5
6
7
8
9
0
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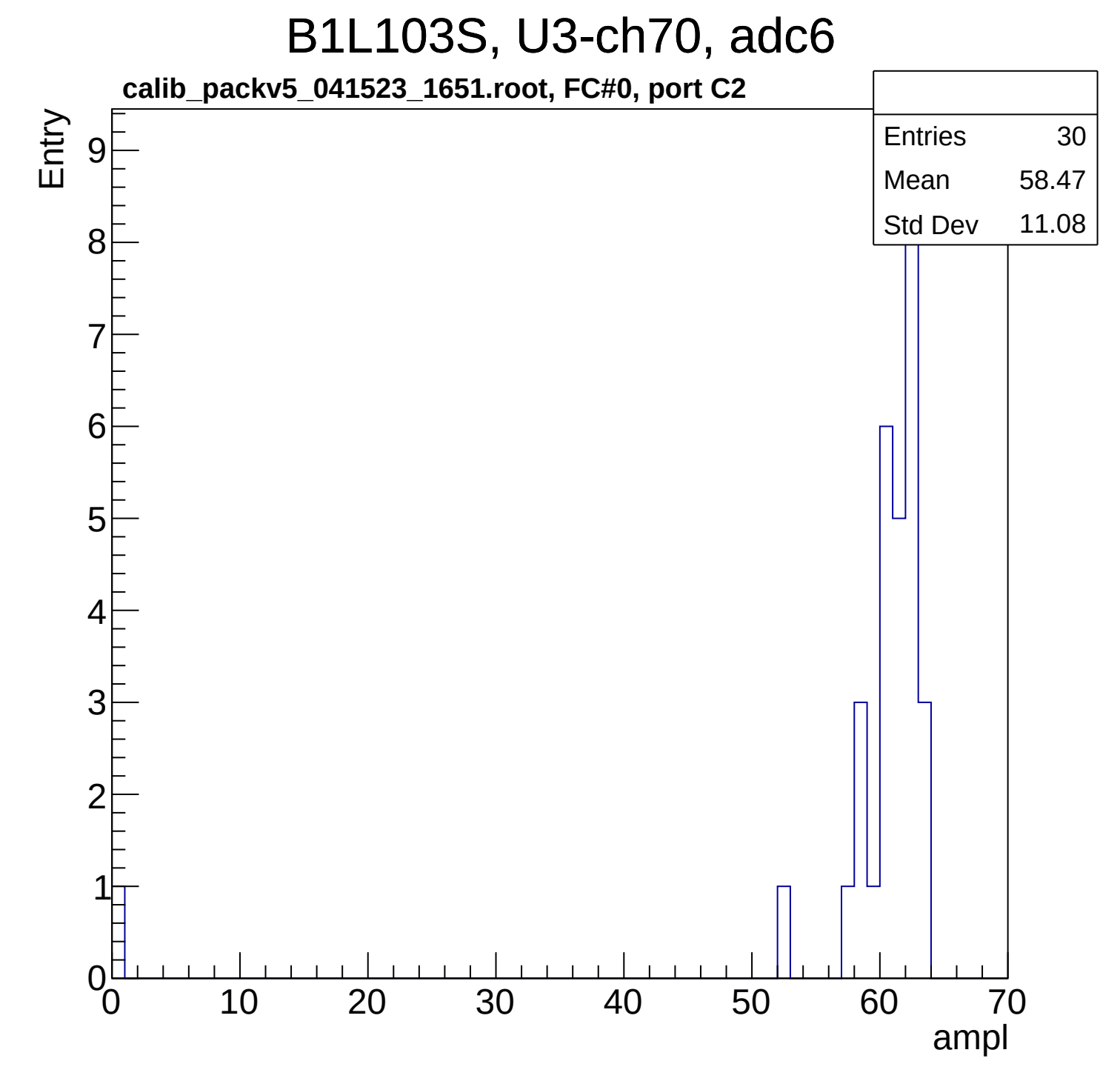
B1L103S, U3-ch70, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 58.47
Std Dev 11.08
Entry
ampl
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2
3
4
5
6
7
8
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0
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40
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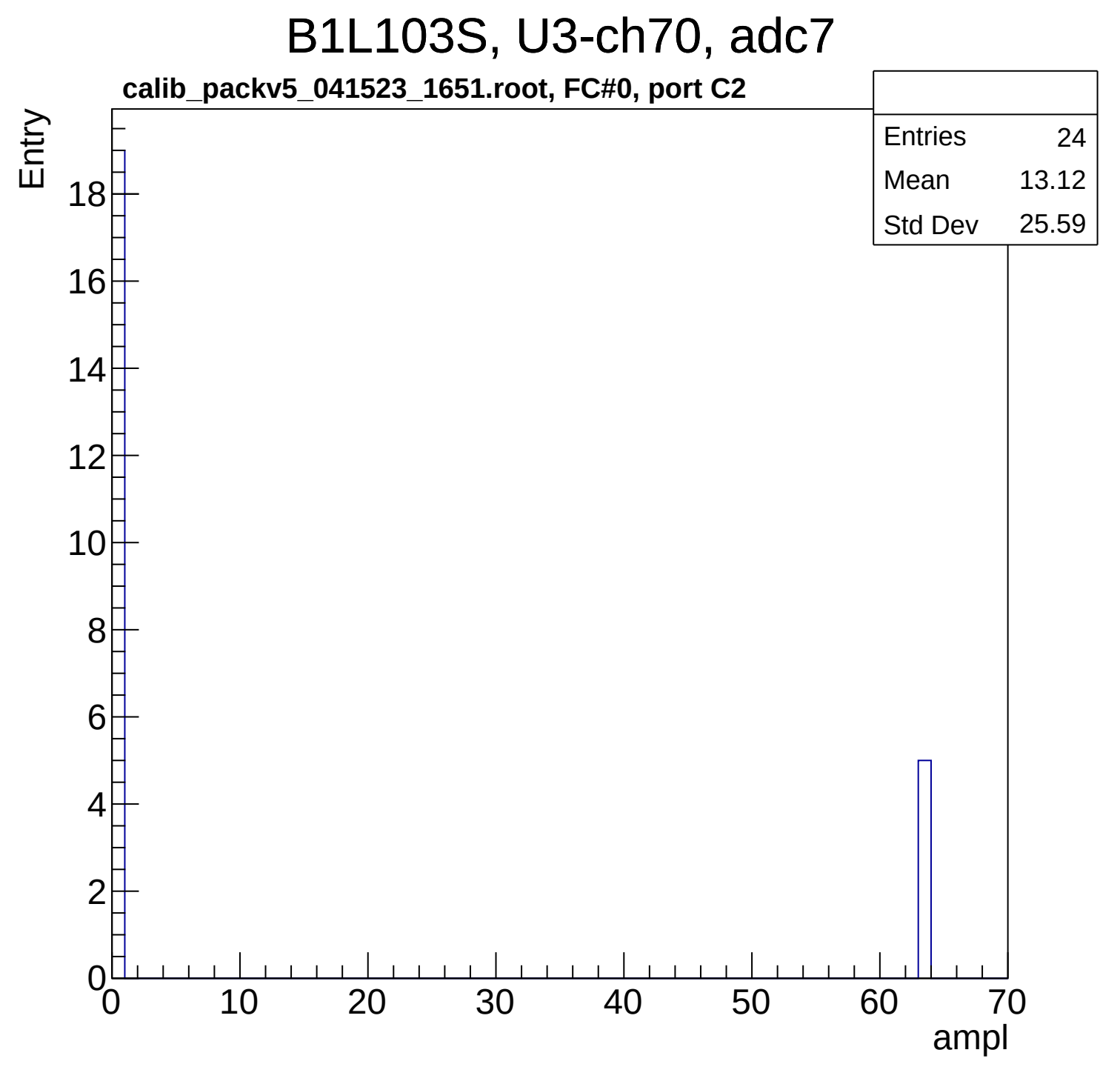
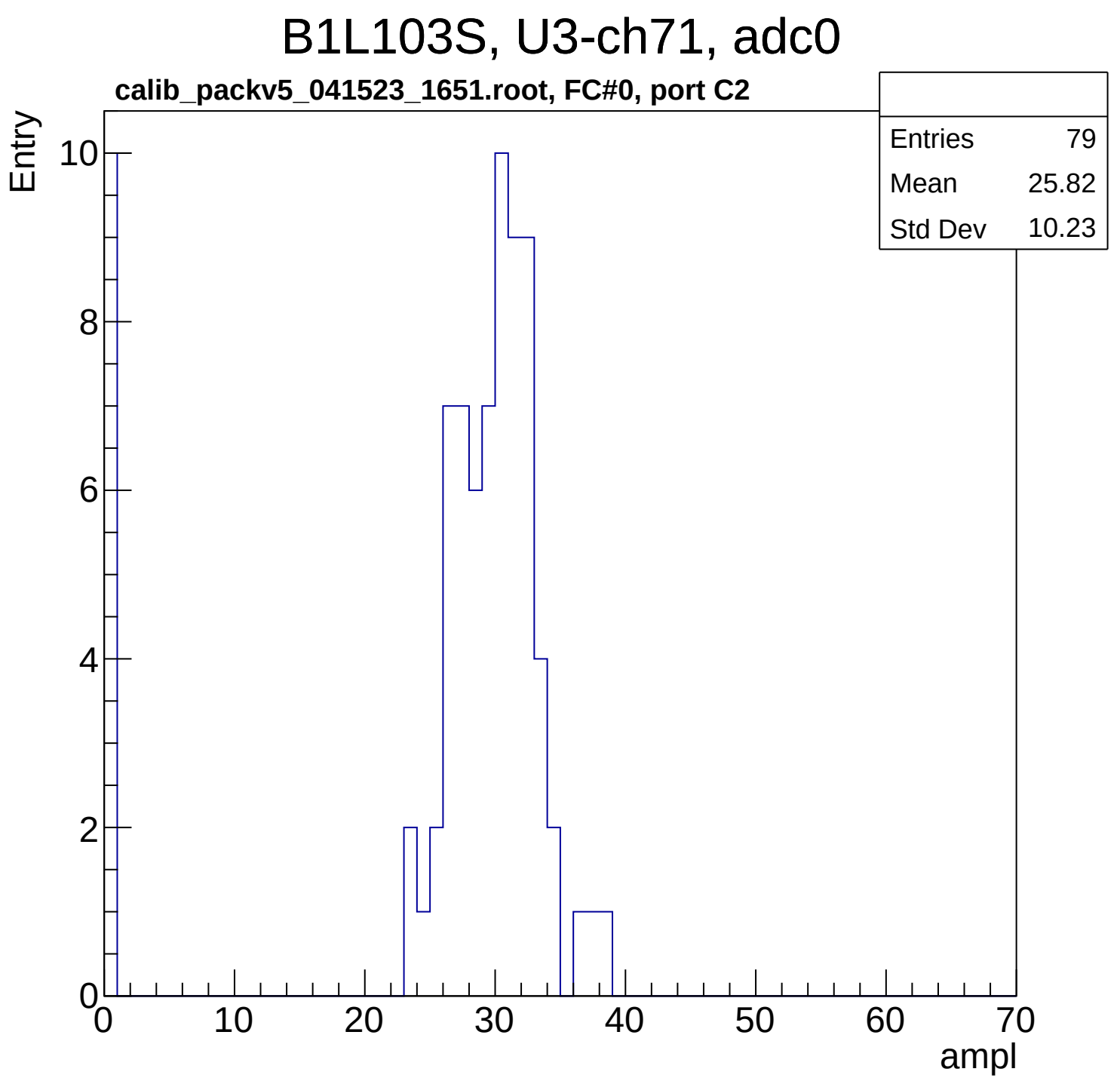
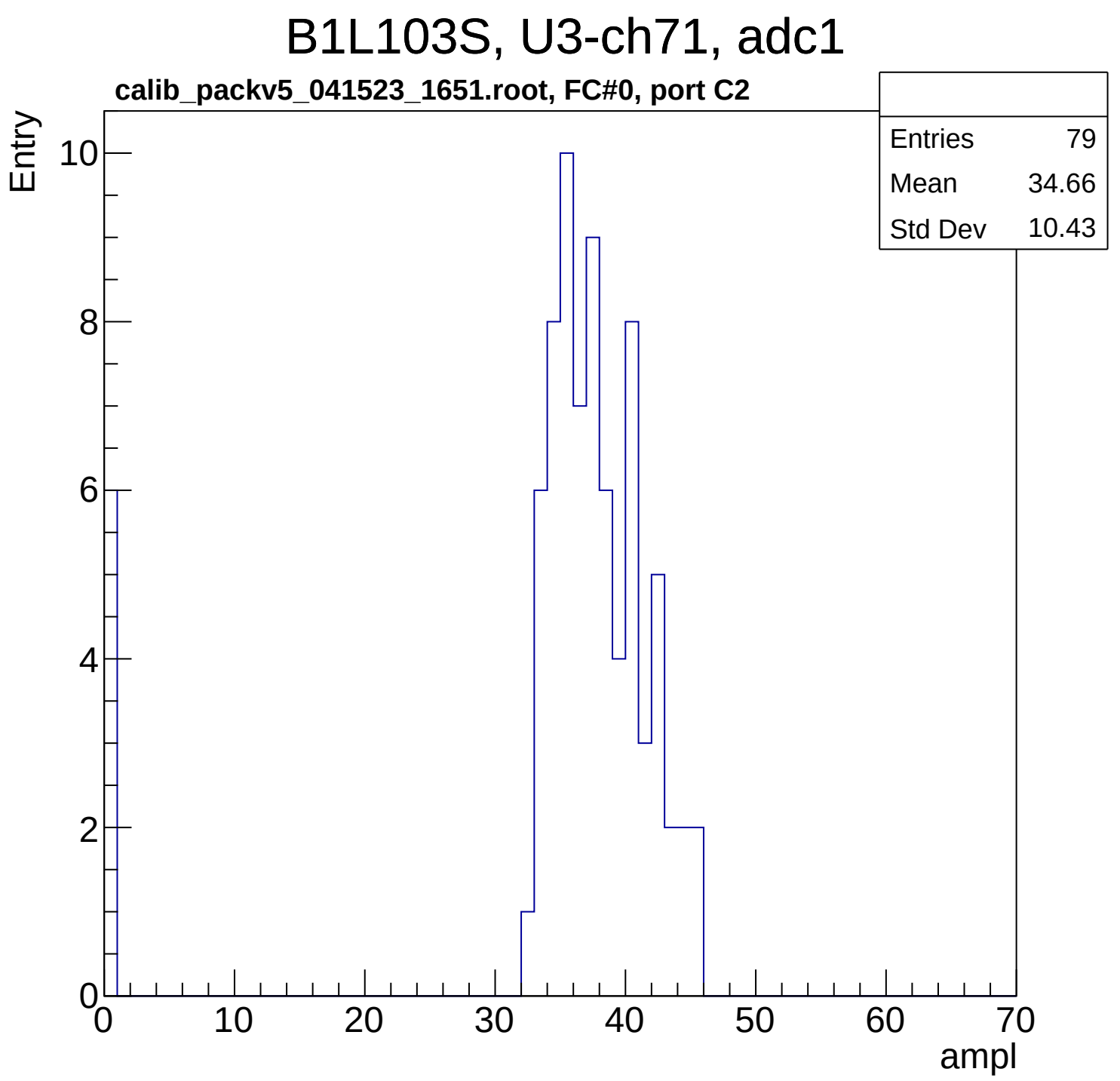
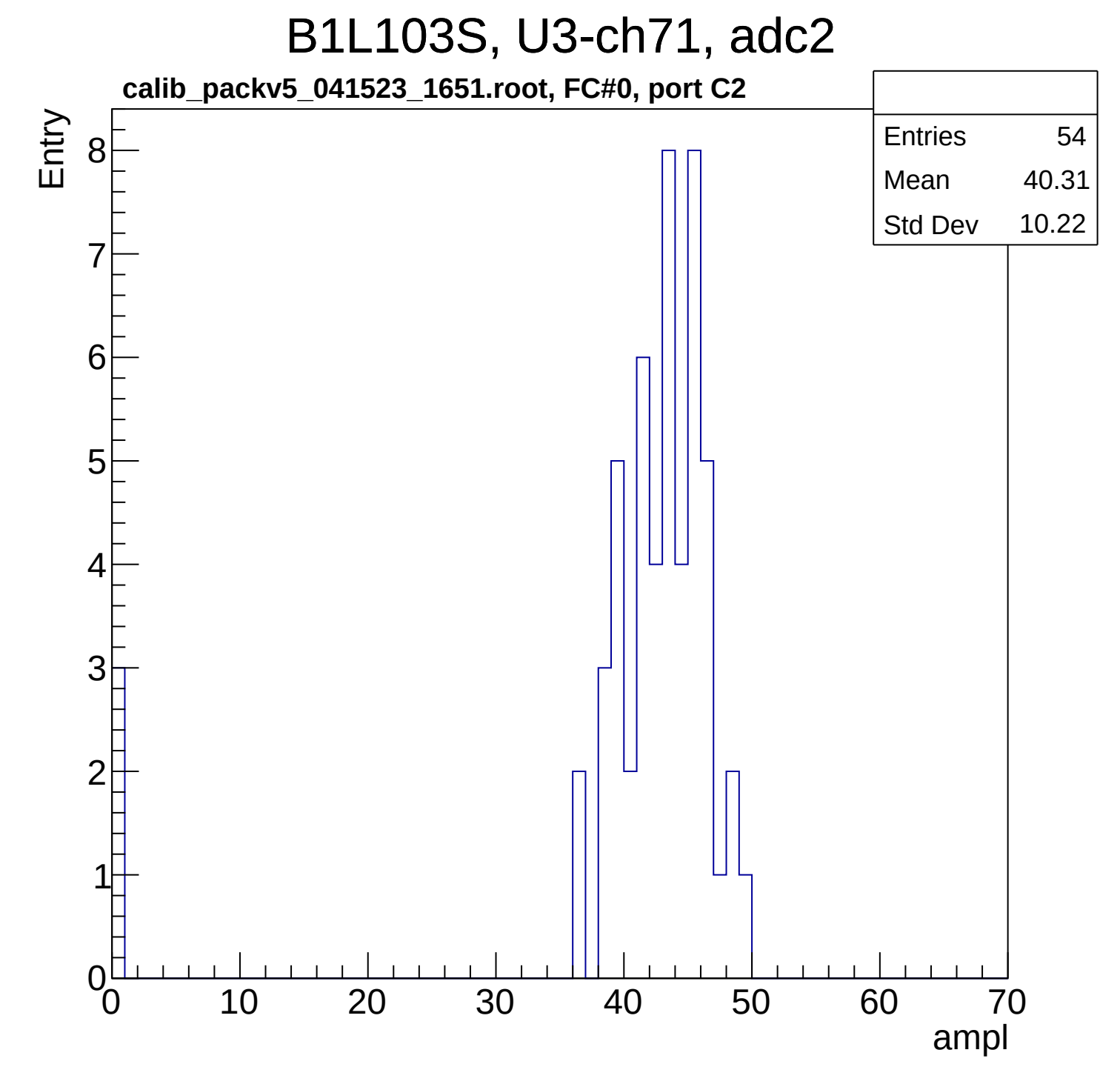

B1L103S, U3-ch70, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 13.12
Std Dev 25.59
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch71, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 25.82
Std Dev 10.23
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch71, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 34.66
Std Dev 10.43
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch71, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 40.31
Std Dev 10.22
Entry
ampl
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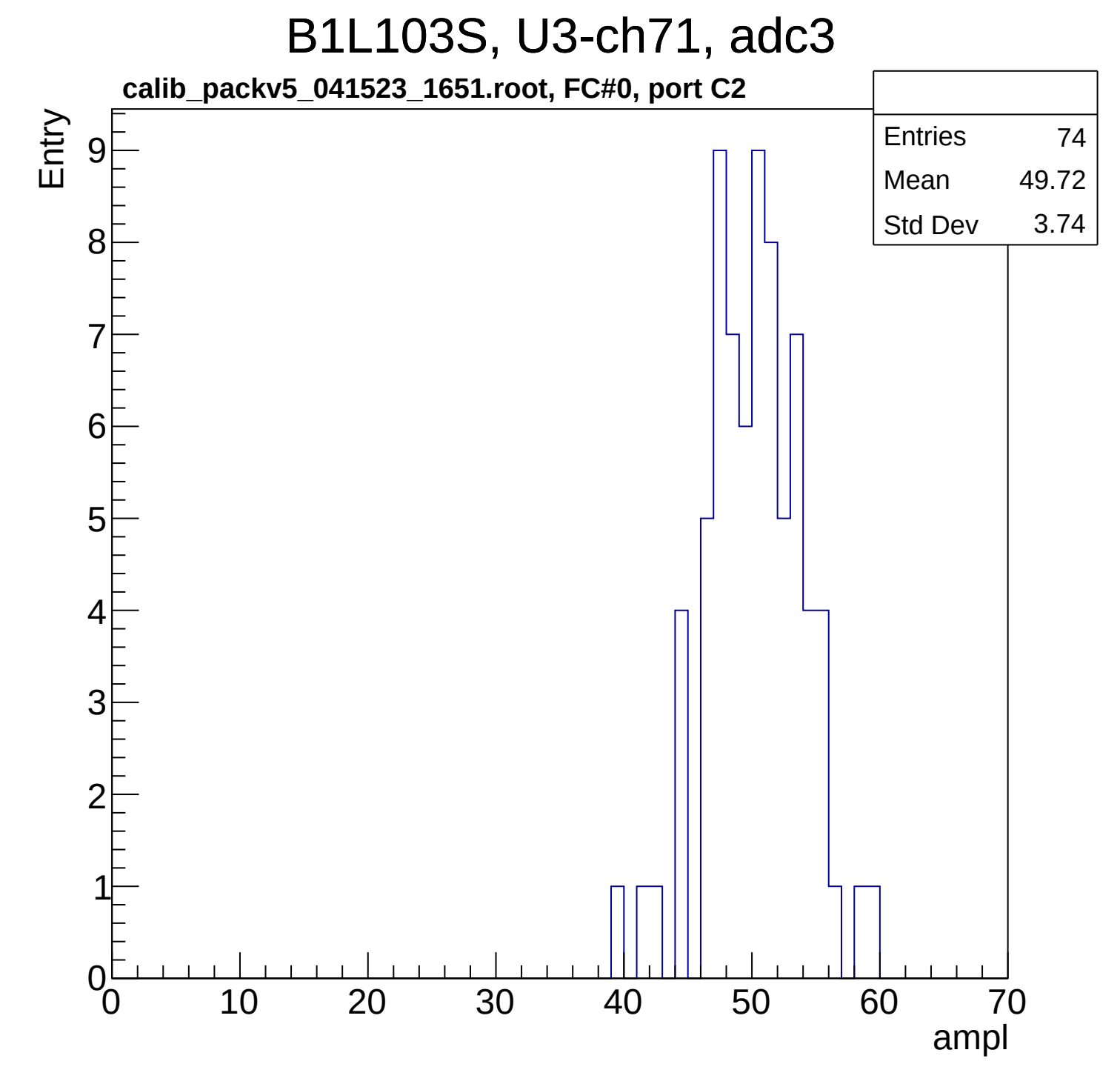
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch71, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 49.72
Std Dev 3.74
Entry
ampl
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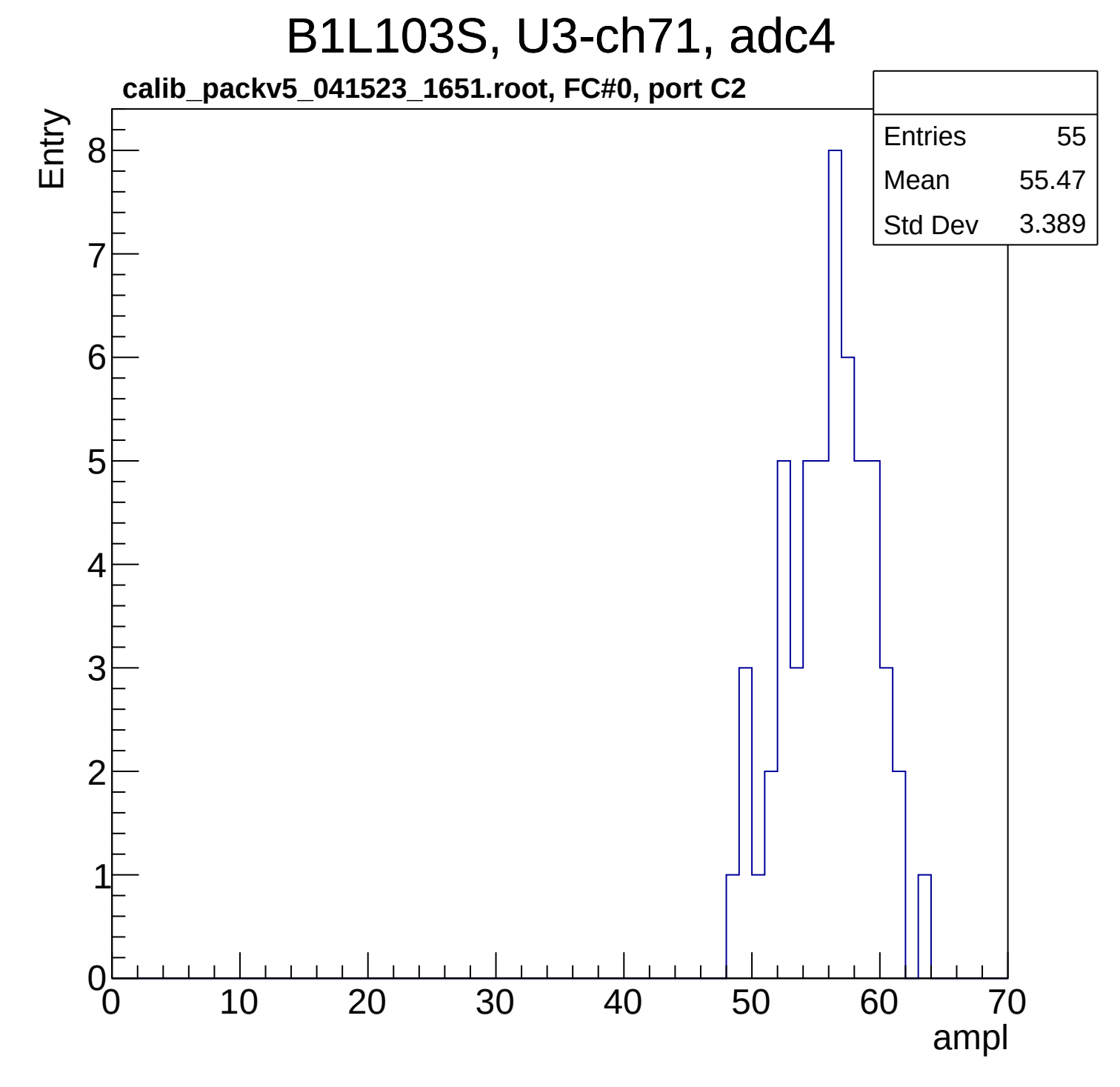
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch71, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 55.47
Std Dev 3.389
Entry
ampl
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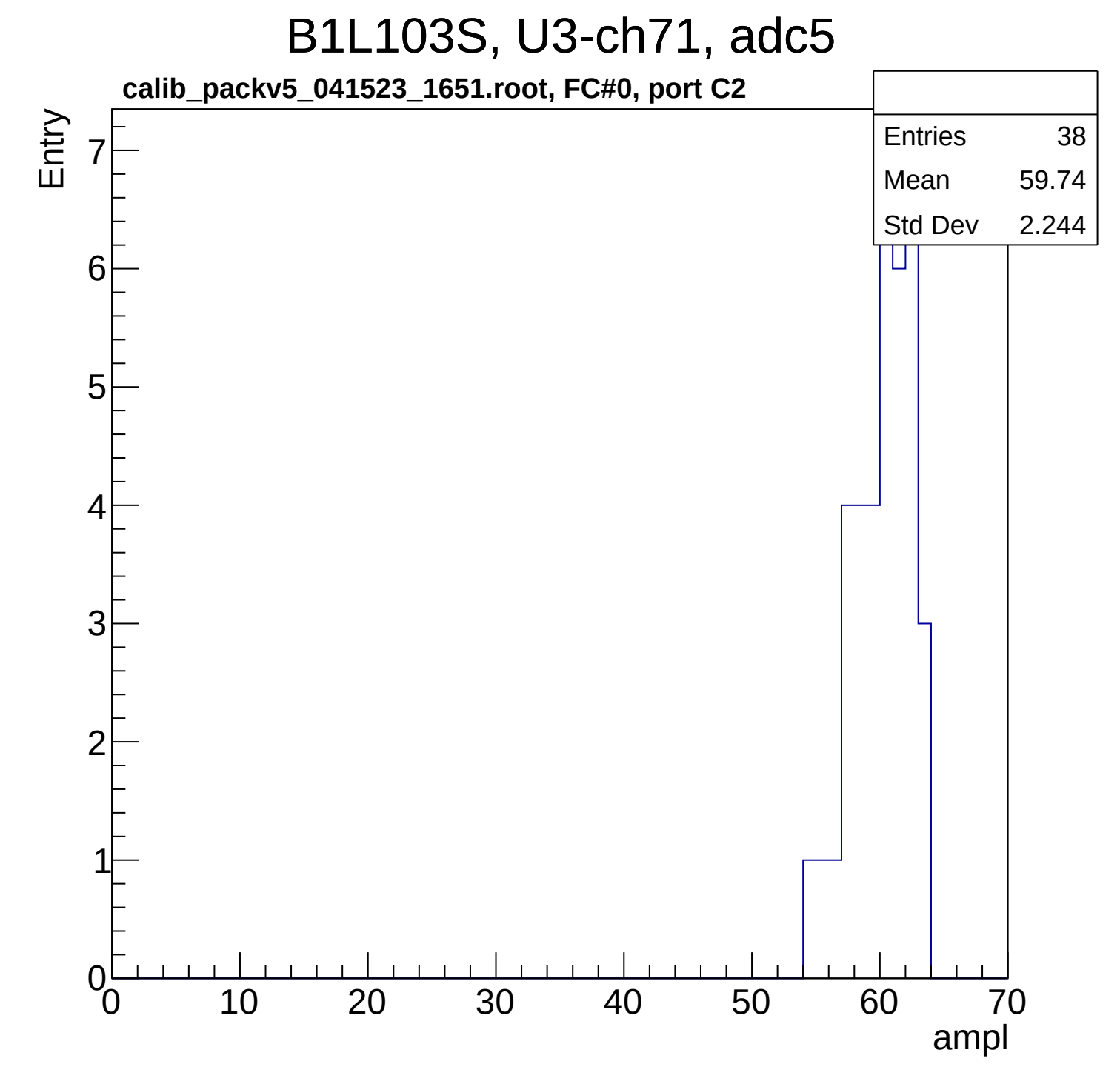
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch71, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 59.74
Std Dev 2.244
Entry
ampl
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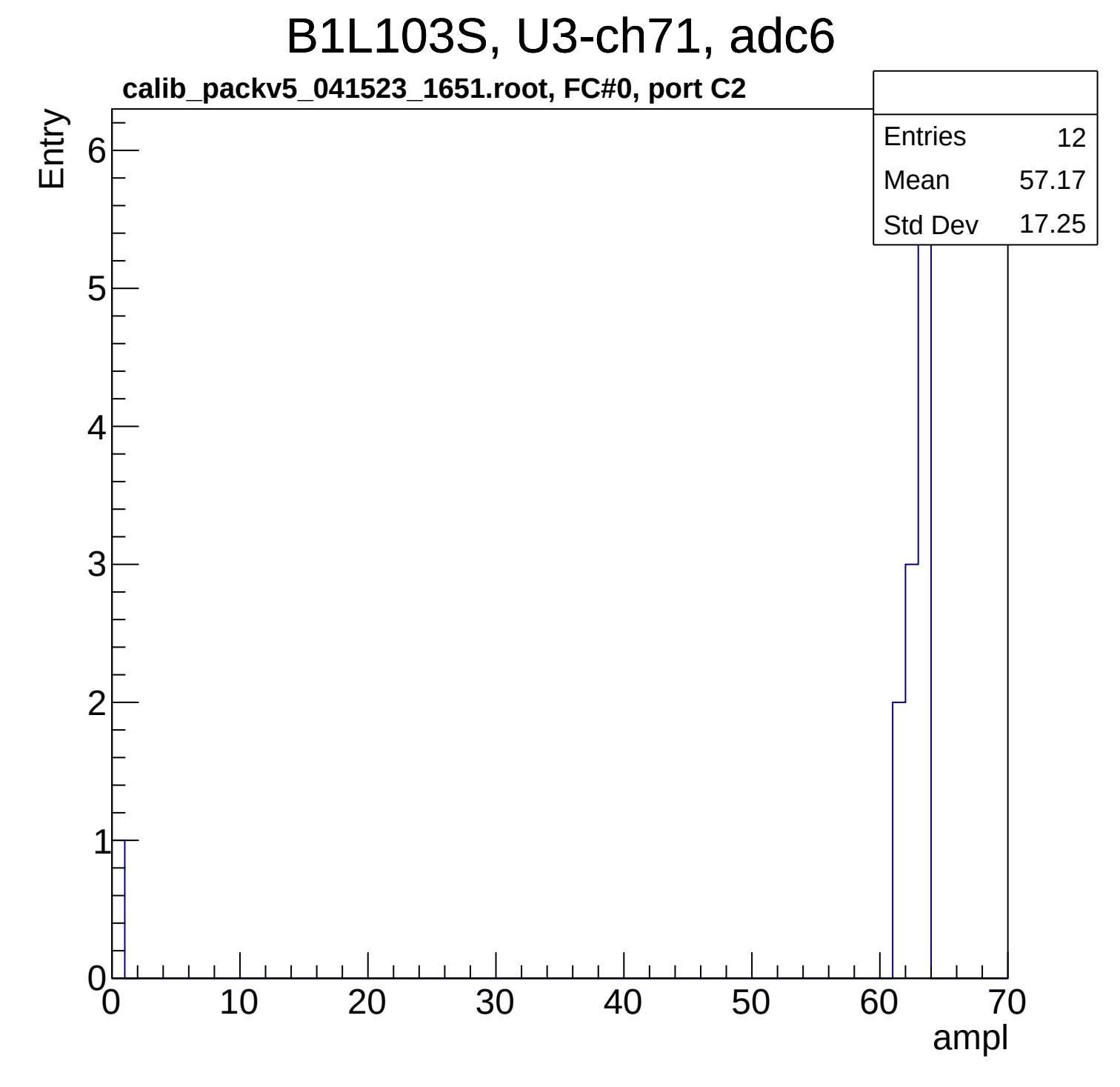
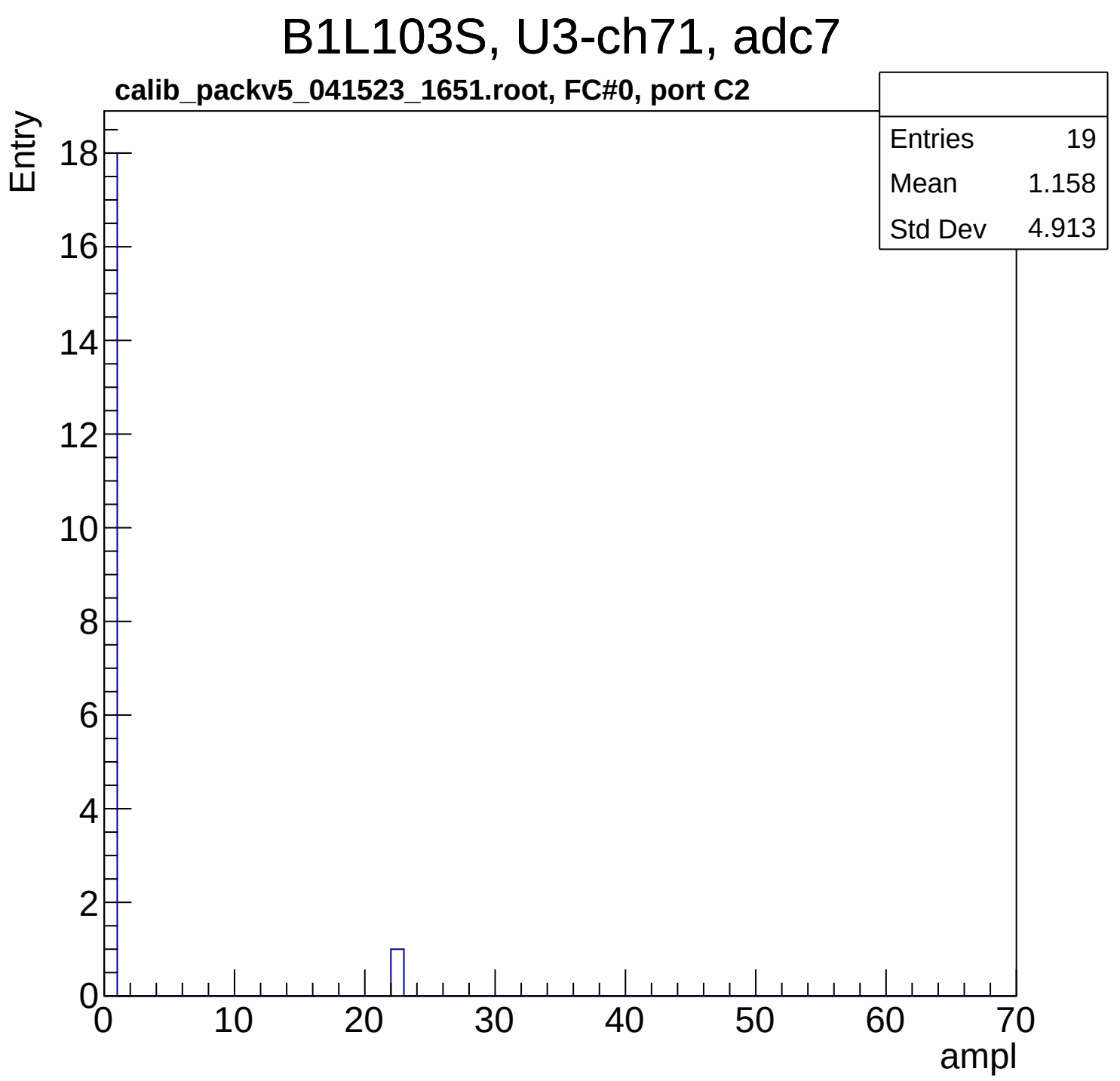
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch71, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 57.17
Std Dev 17.25
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U3-ch71, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.158
Std Dev 4.913
Entry
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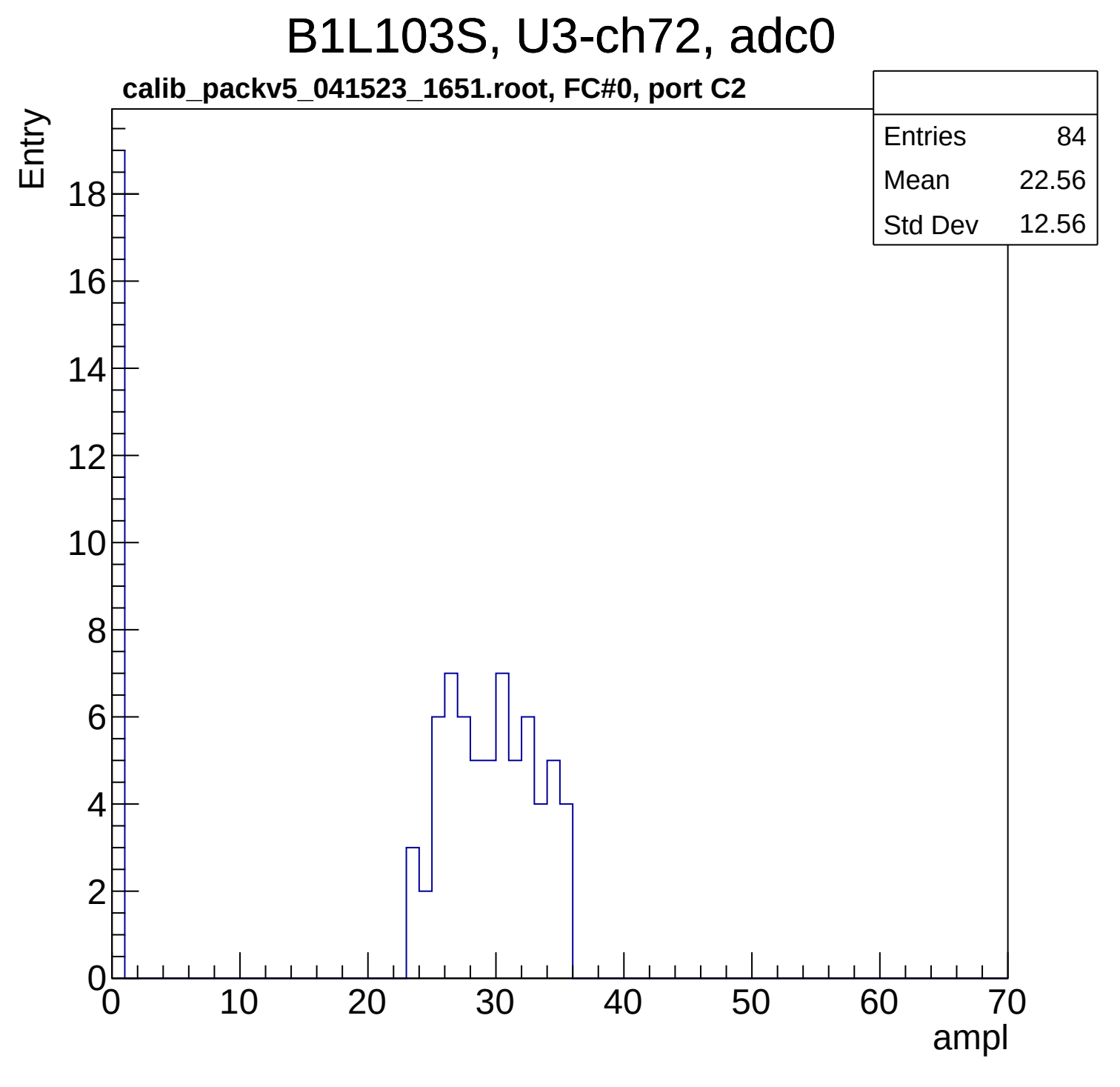
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch72, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 22.56
Std Dev 12.56
Entry
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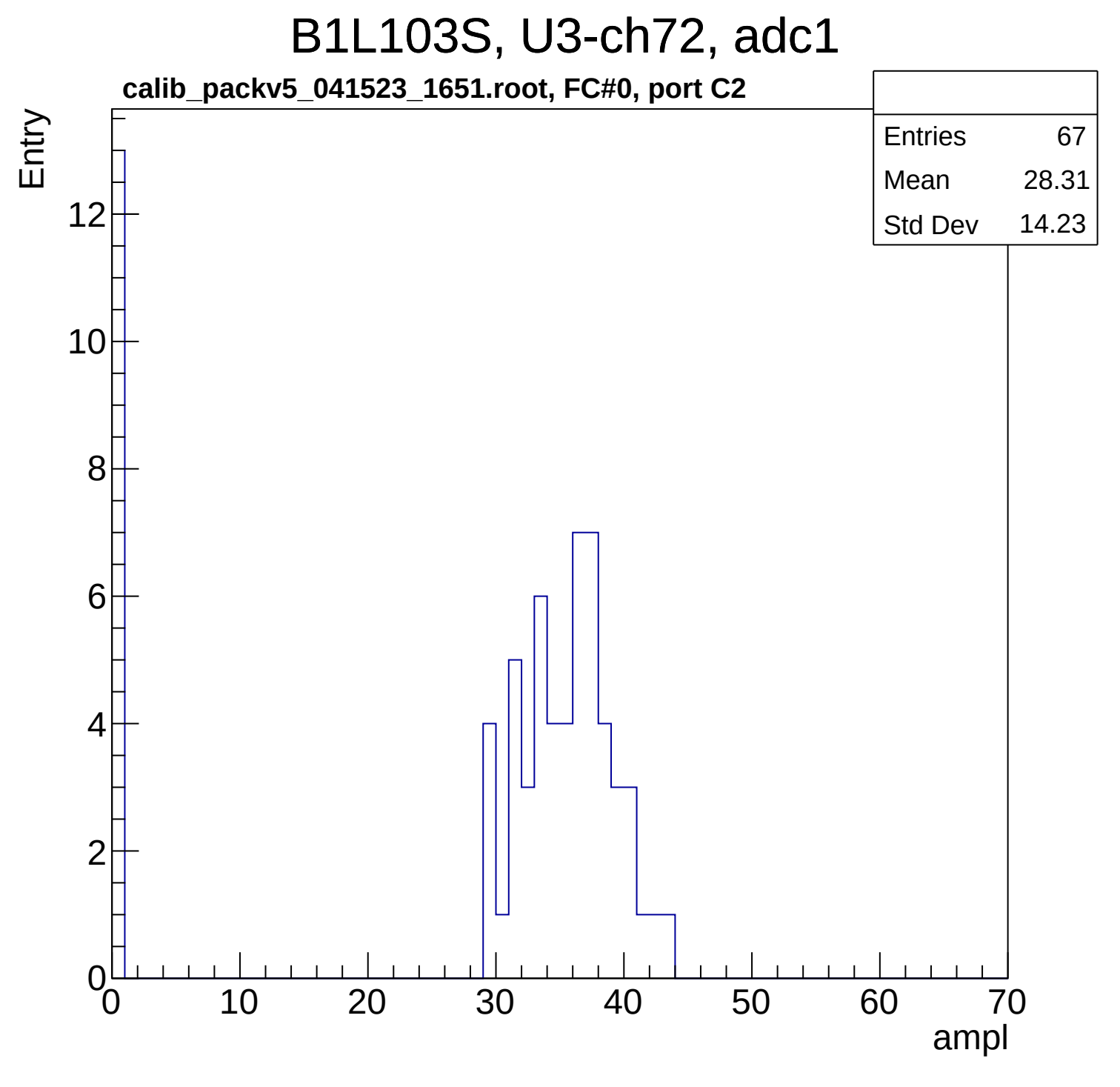
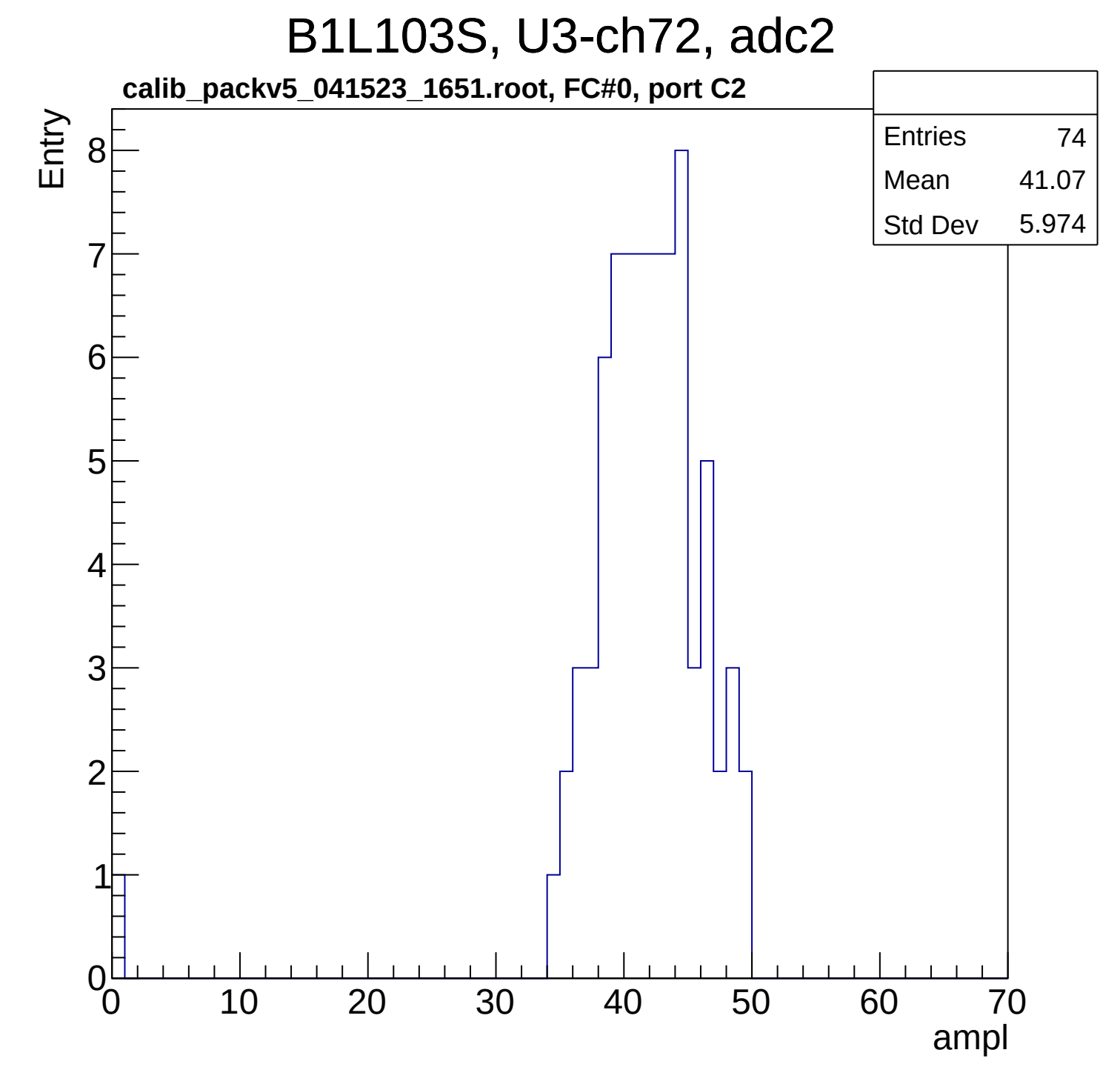
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch72, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 28.31
Std Dev 14.23
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch72, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 41.07
Std Dev 5.974
Entry
ampl
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2
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4
5
6
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0
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60
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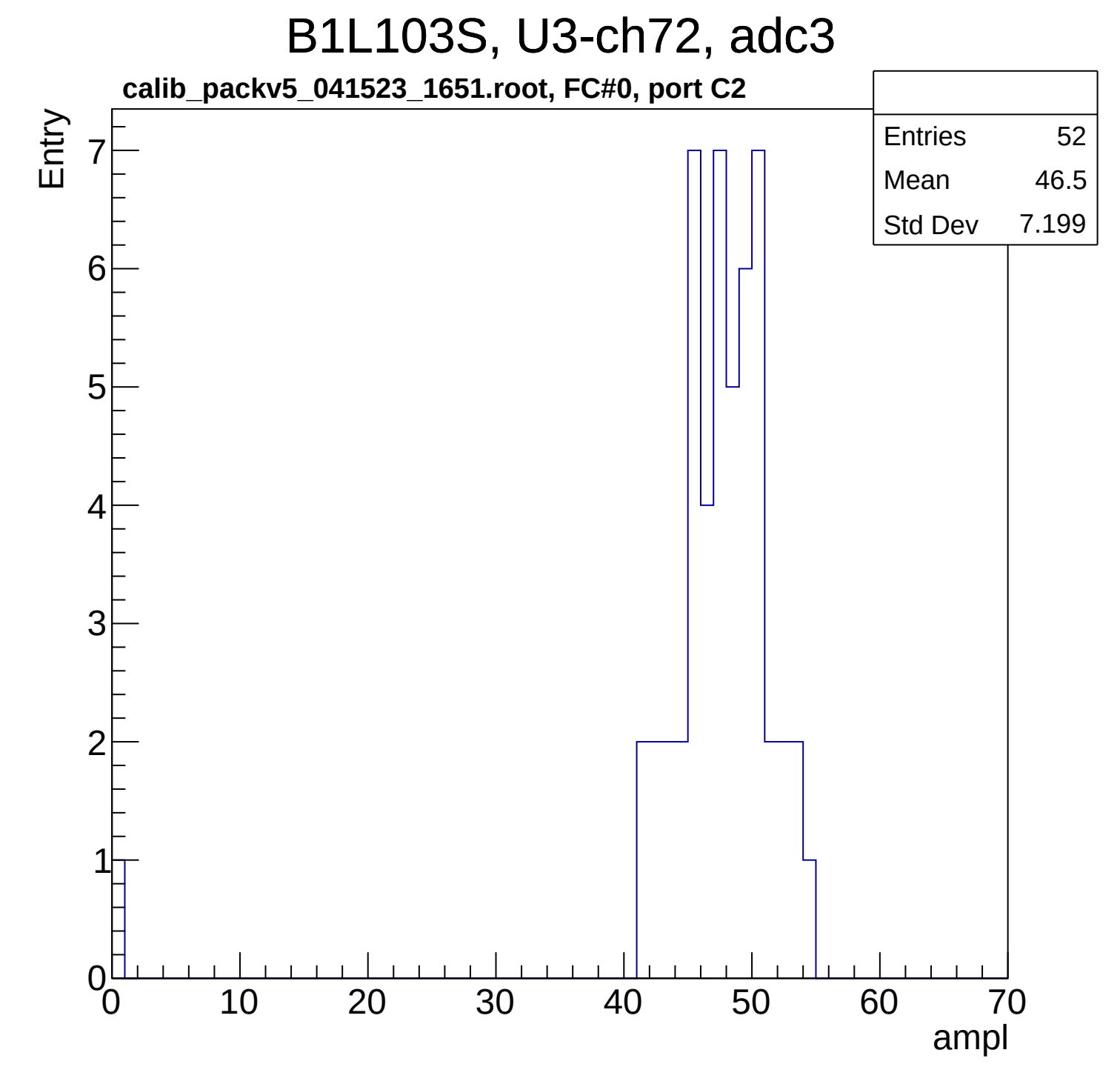
B1L103S, U3-ch72, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 46.5
Std Dev 7.199
Entry
ampl
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1
2
3
4
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6
7
0
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20
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40
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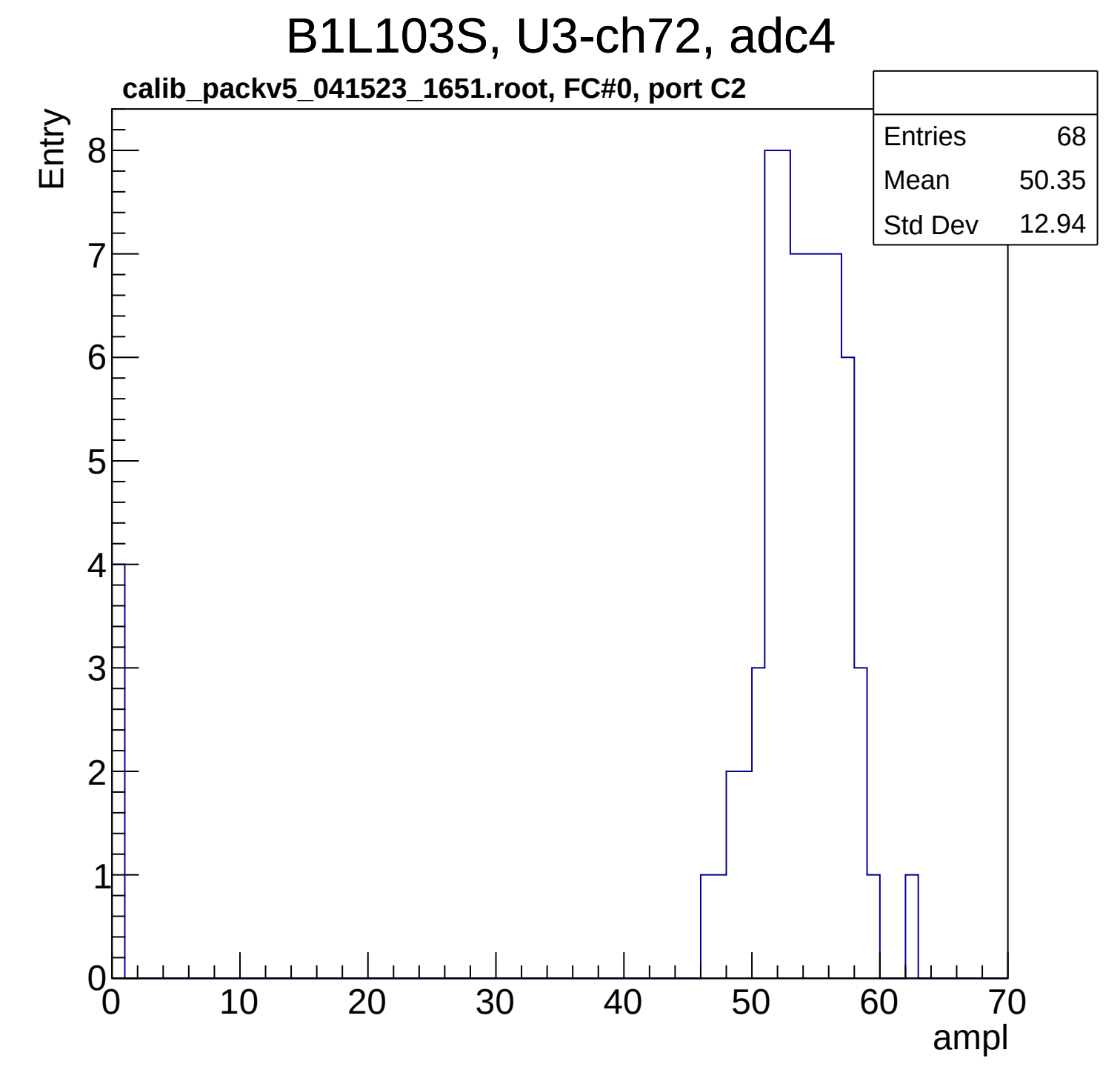
60
70


B1L103S, U3-ch72, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 50.35
Std Dev 12.94
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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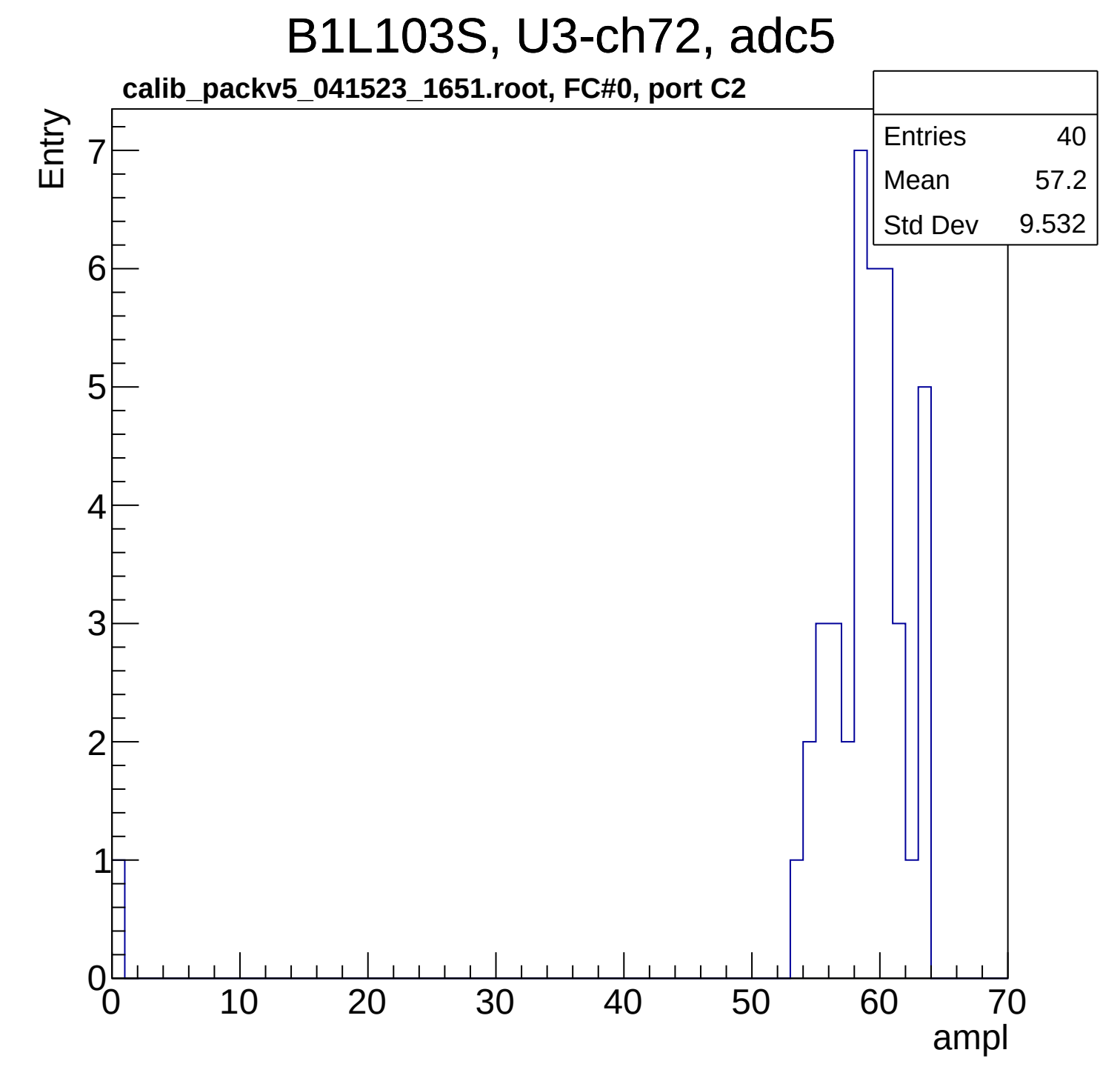
B1L103S, U3-ch72, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 57.2
Std Dev 9.532
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
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60
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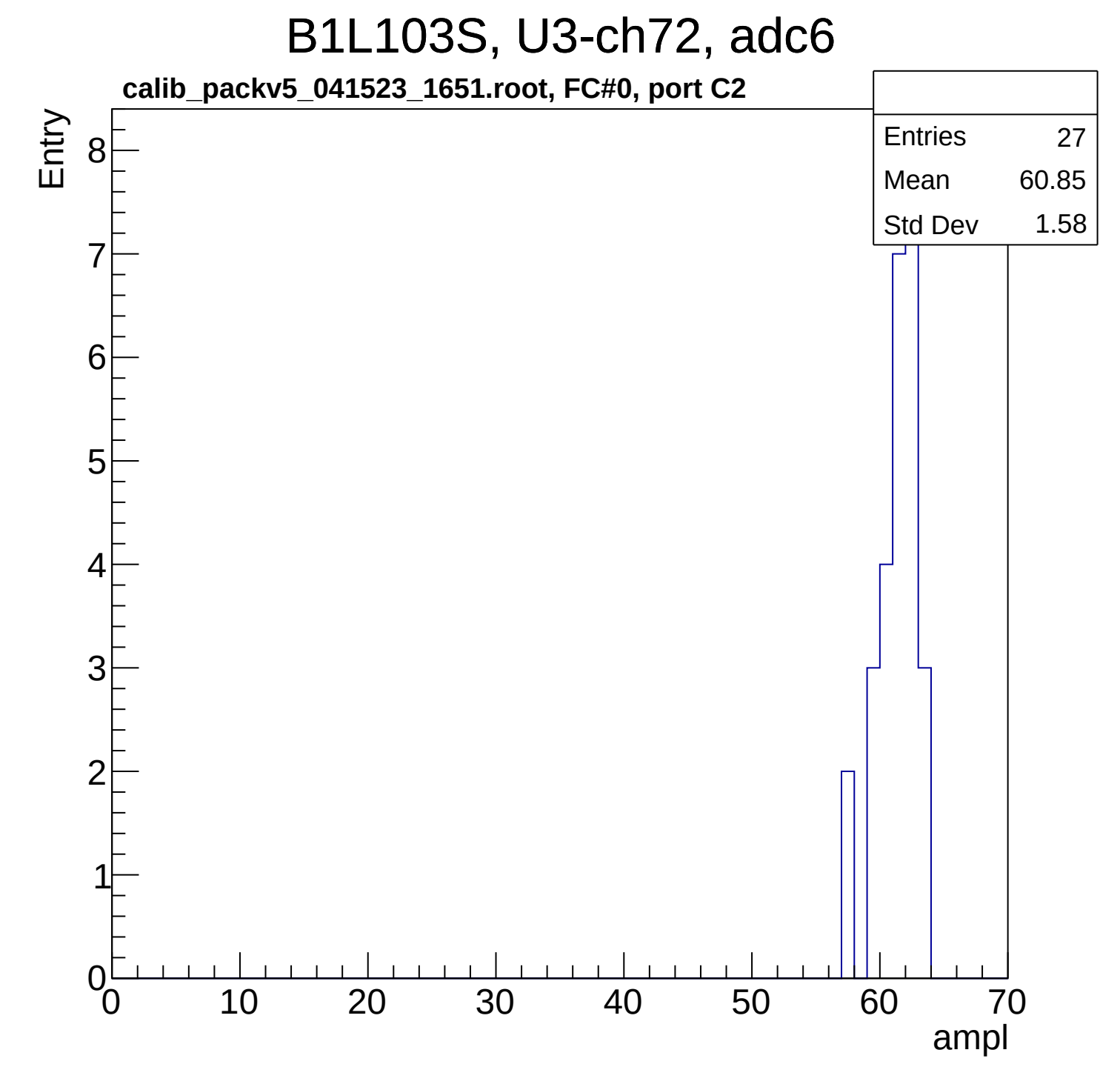
B1L103S, U3-ch72, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 60.85
Std Dev 1.58
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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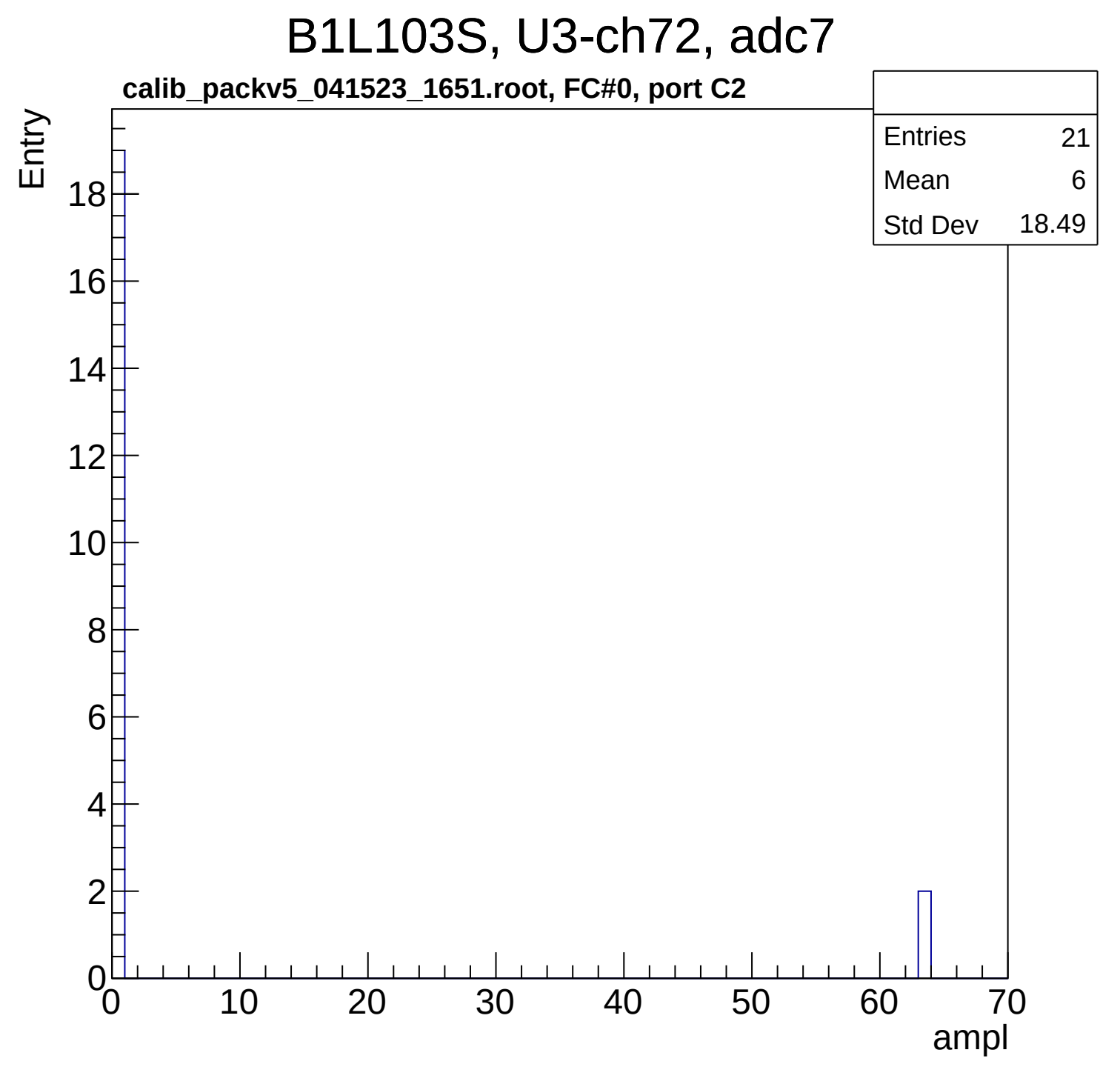
B1L103S, U3-ch72, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 6
Std Dev 18.49
Entry
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6
8
10
12
14
16
18
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10
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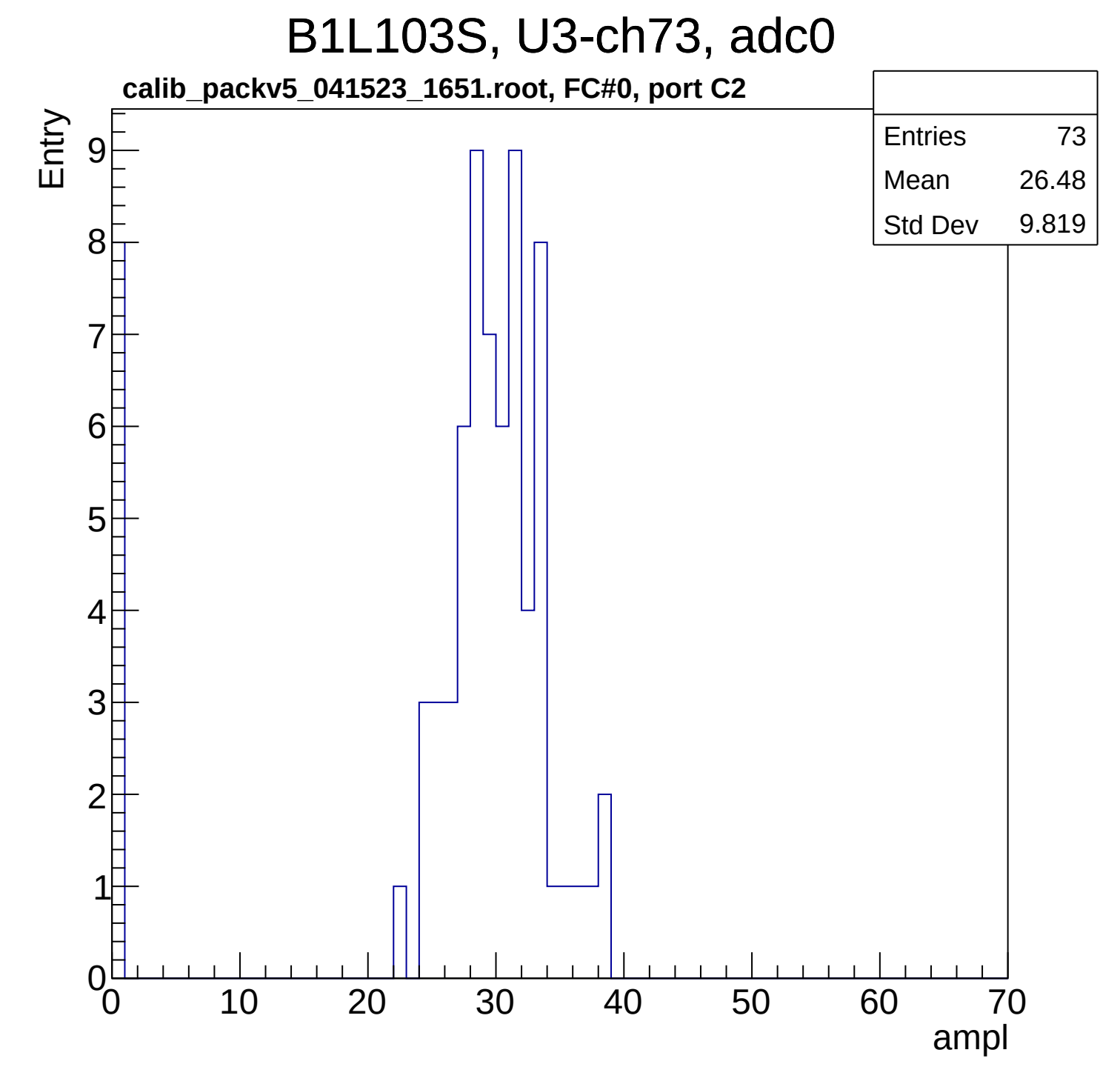
60
70
ampl


B1L103S, U3-ch73, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 26.48
Std Dev 9.819
Entry
ampl
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2
3
4
5
6
7
8
9
0
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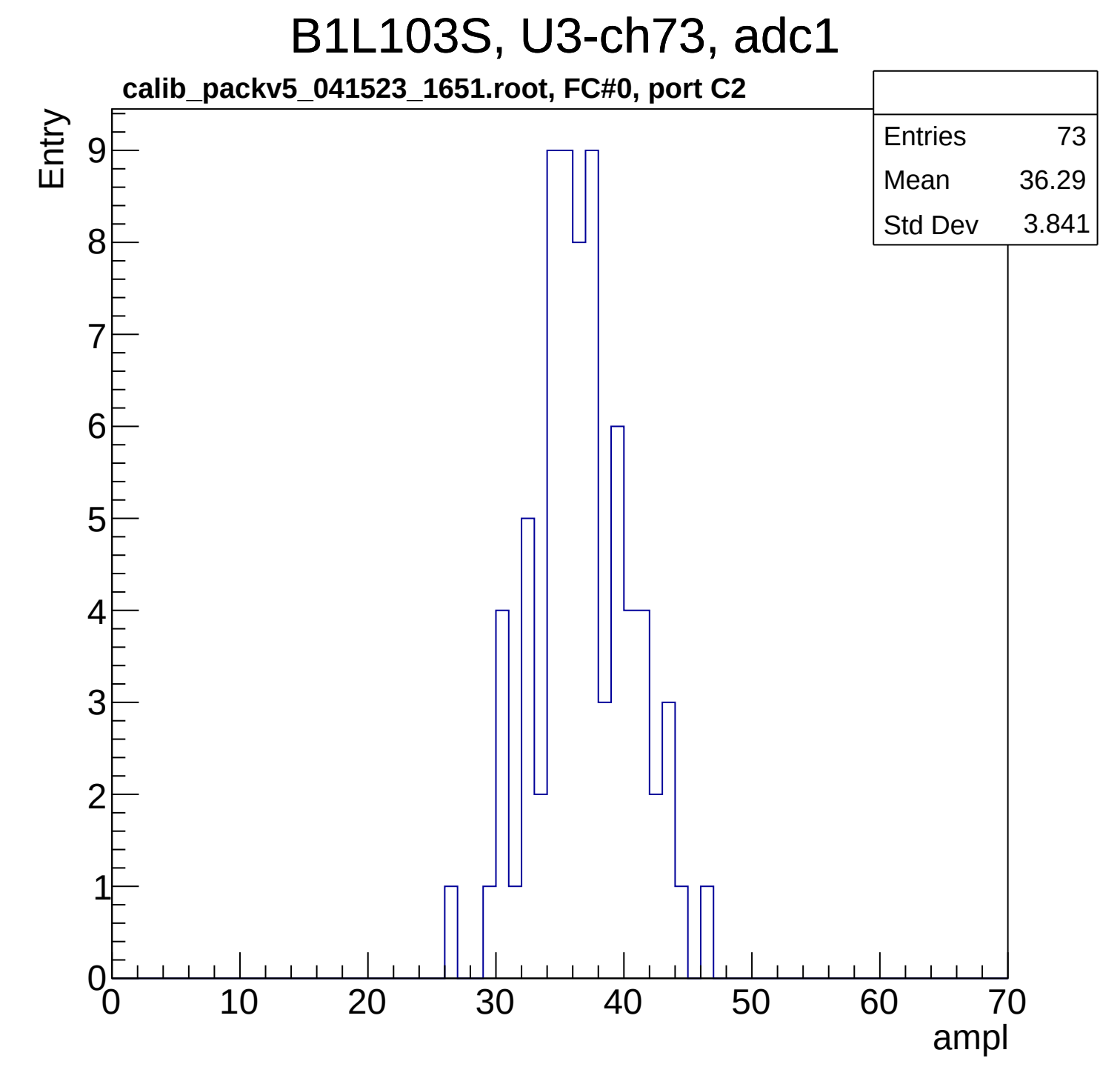
B1L103S, U3-ch73, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 36.29
Std Dev 3.841
Entry
ampl
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2
3
4
5
6
7
8
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0
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40
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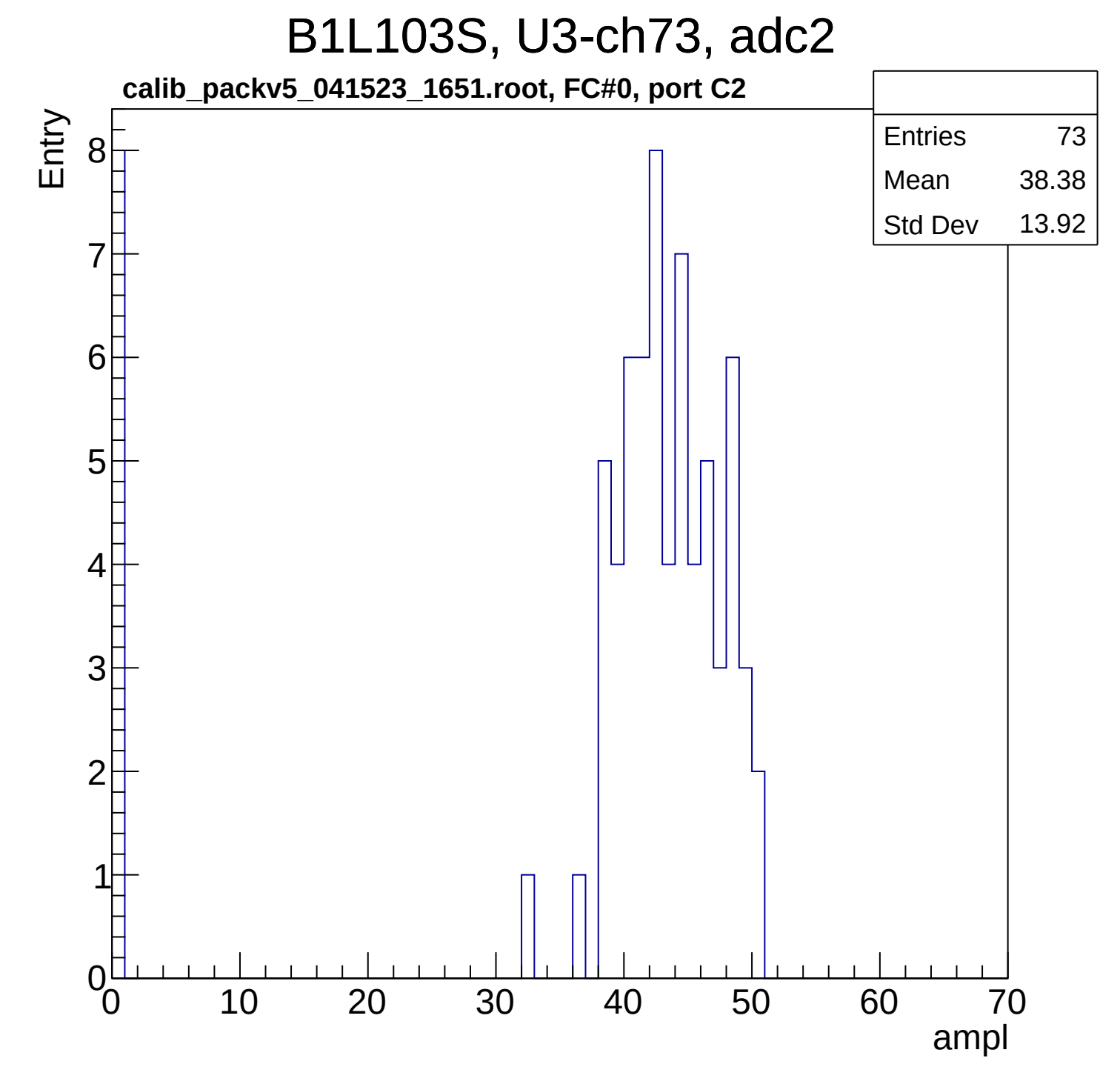
60
70


B1L103S, U3-ch73, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 38.38
Std Dev 13.92
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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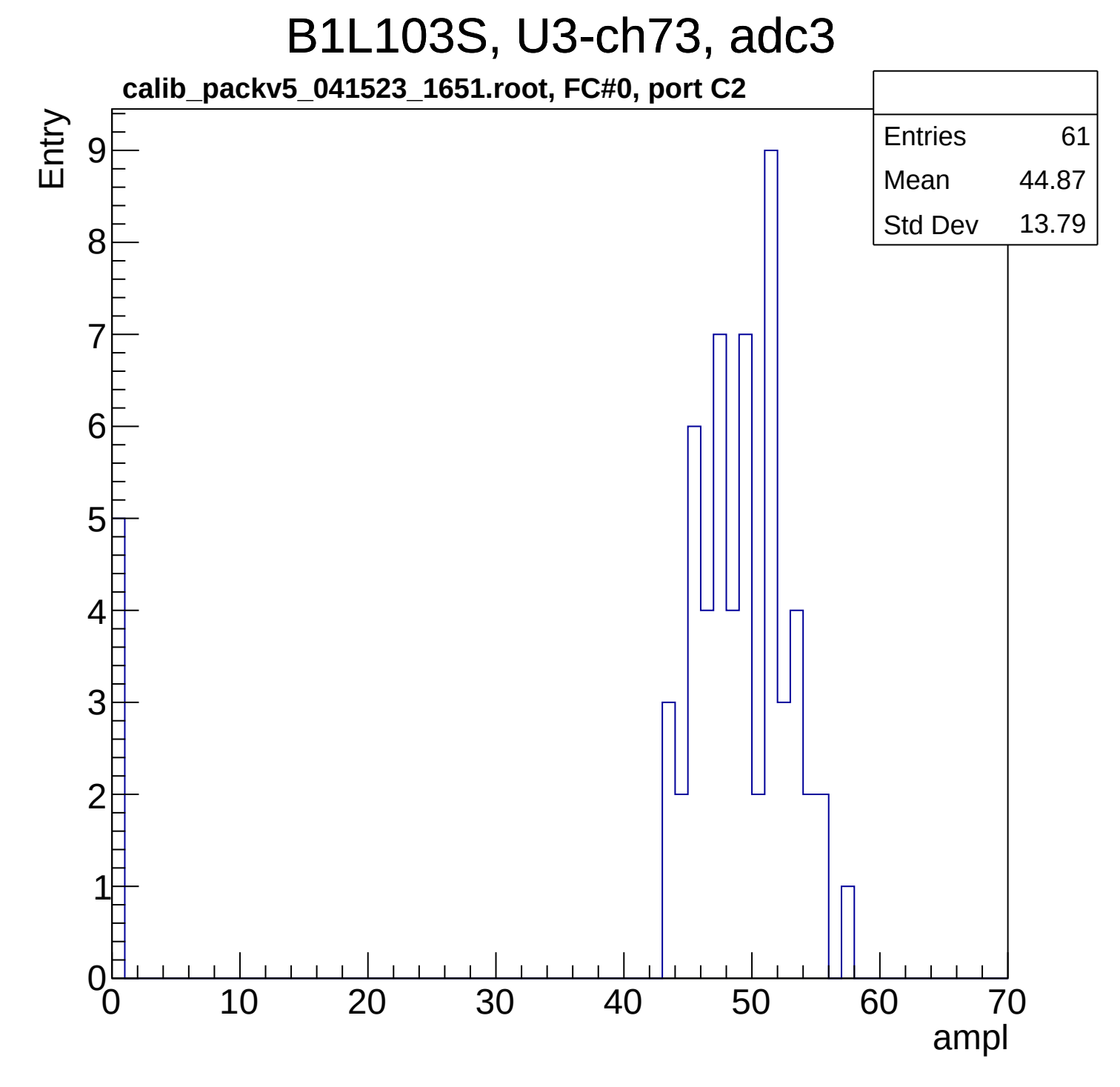
40
50
60
70


B1L103S, U3-ch73, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 44.87
Std Dev 13.79
Entry
ampl
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2
3
4
5
6
7
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0
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40
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60
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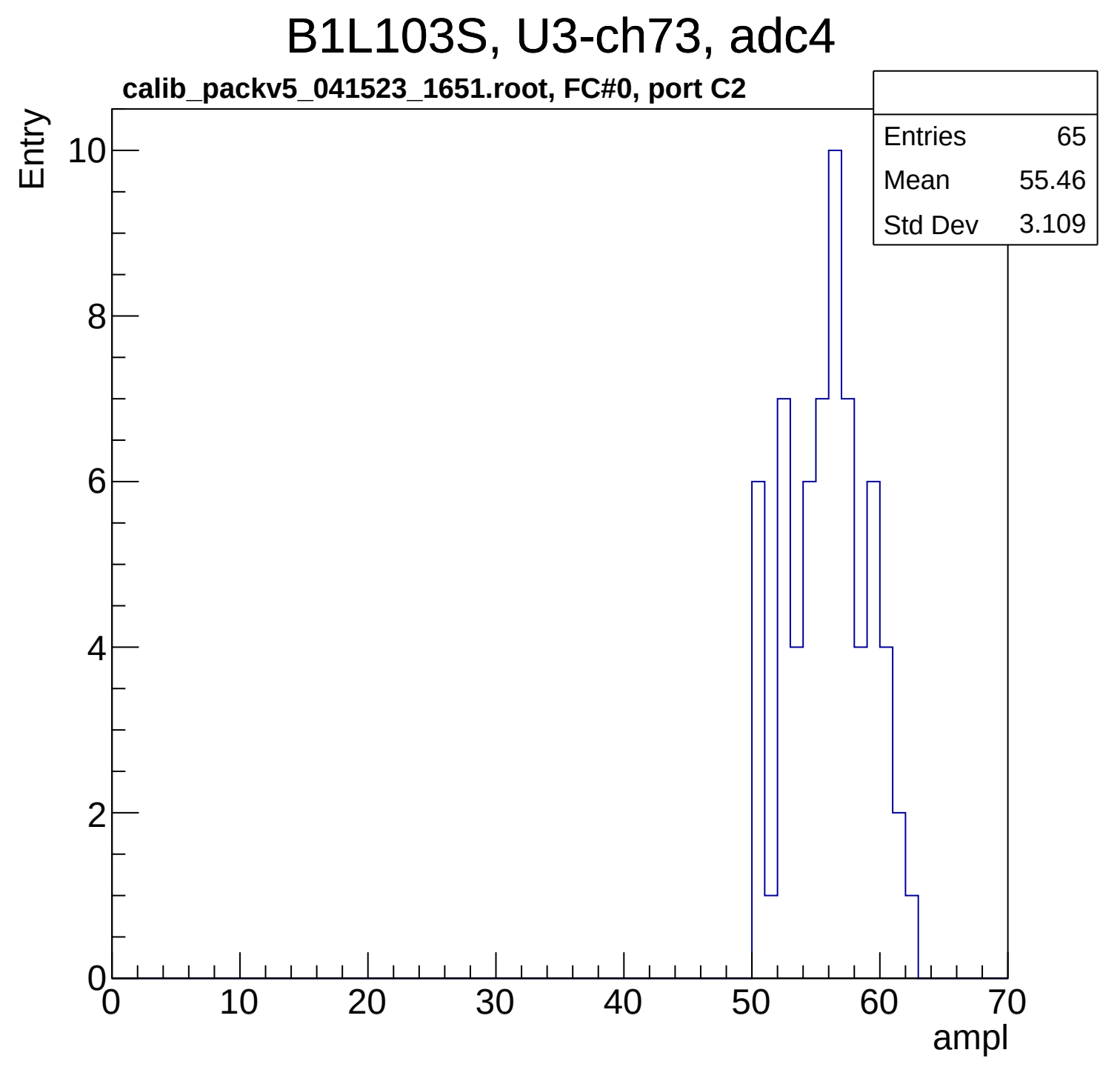
B1L103S, U3-ch73, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 55.46
Std Dev 3.109
Entry
ampl
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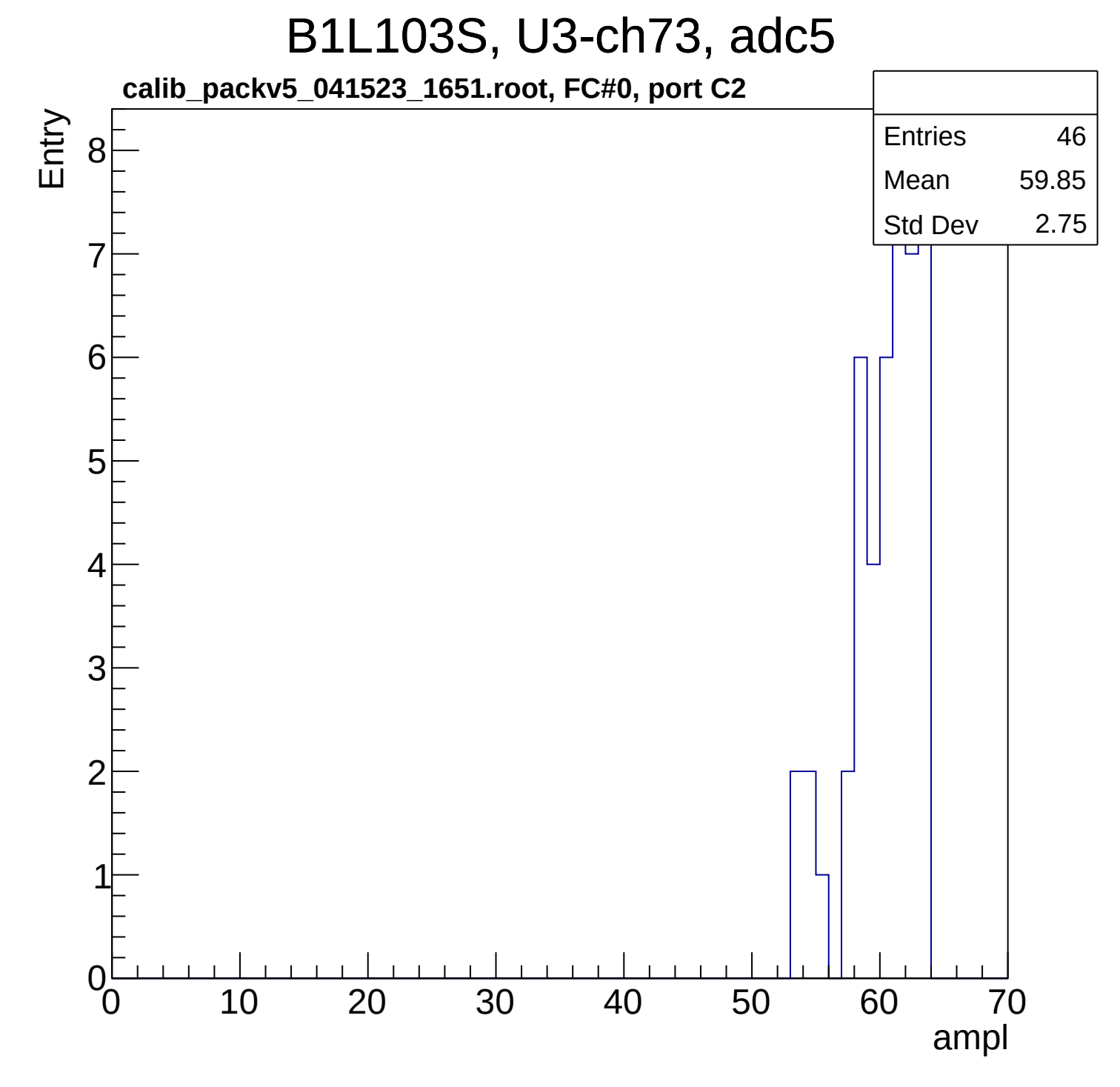
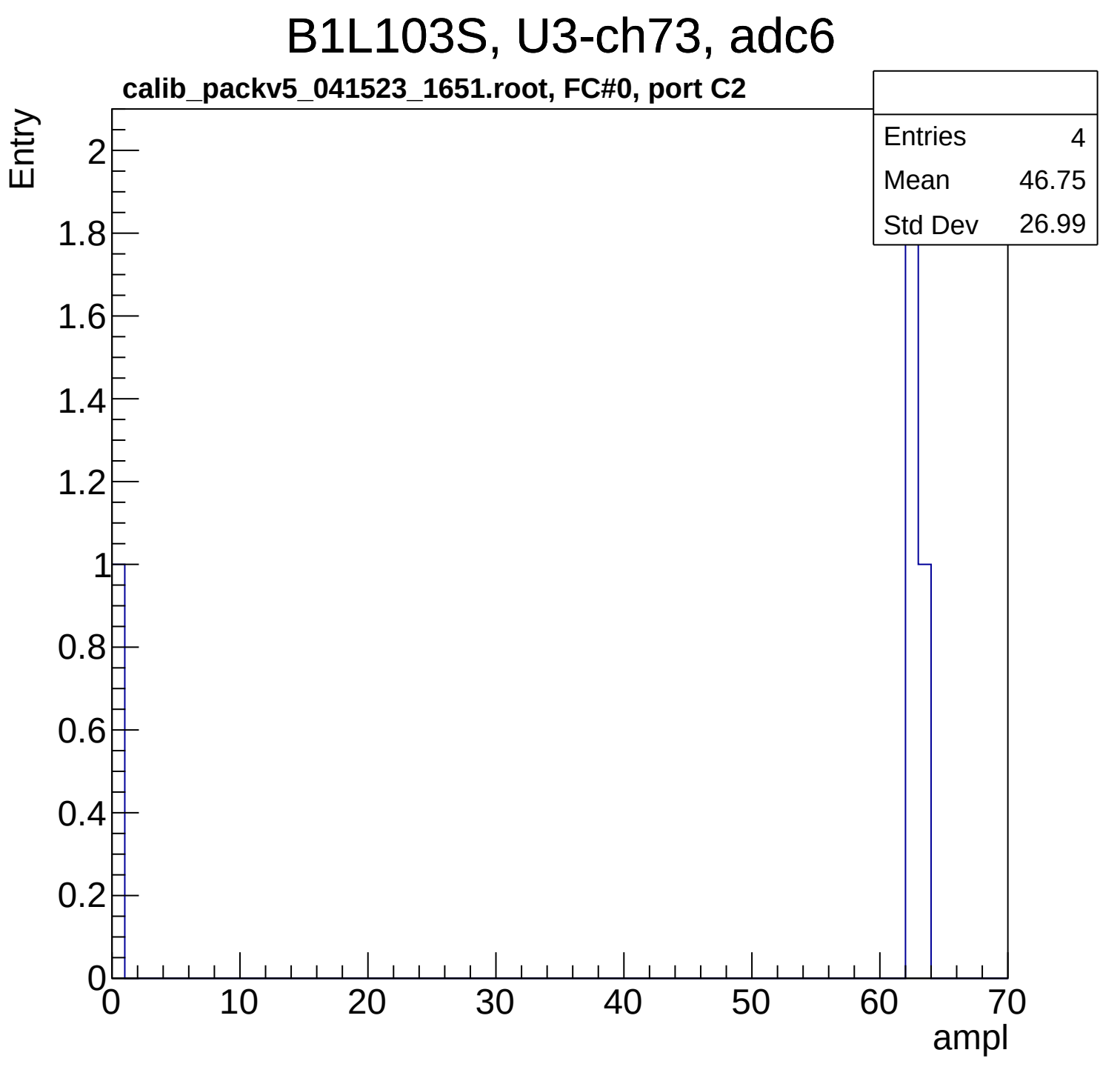
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U3-ch73, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 59.85
Std Dev 2.75
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch73, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 46.75
Std Dev 26.99
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
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40
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60
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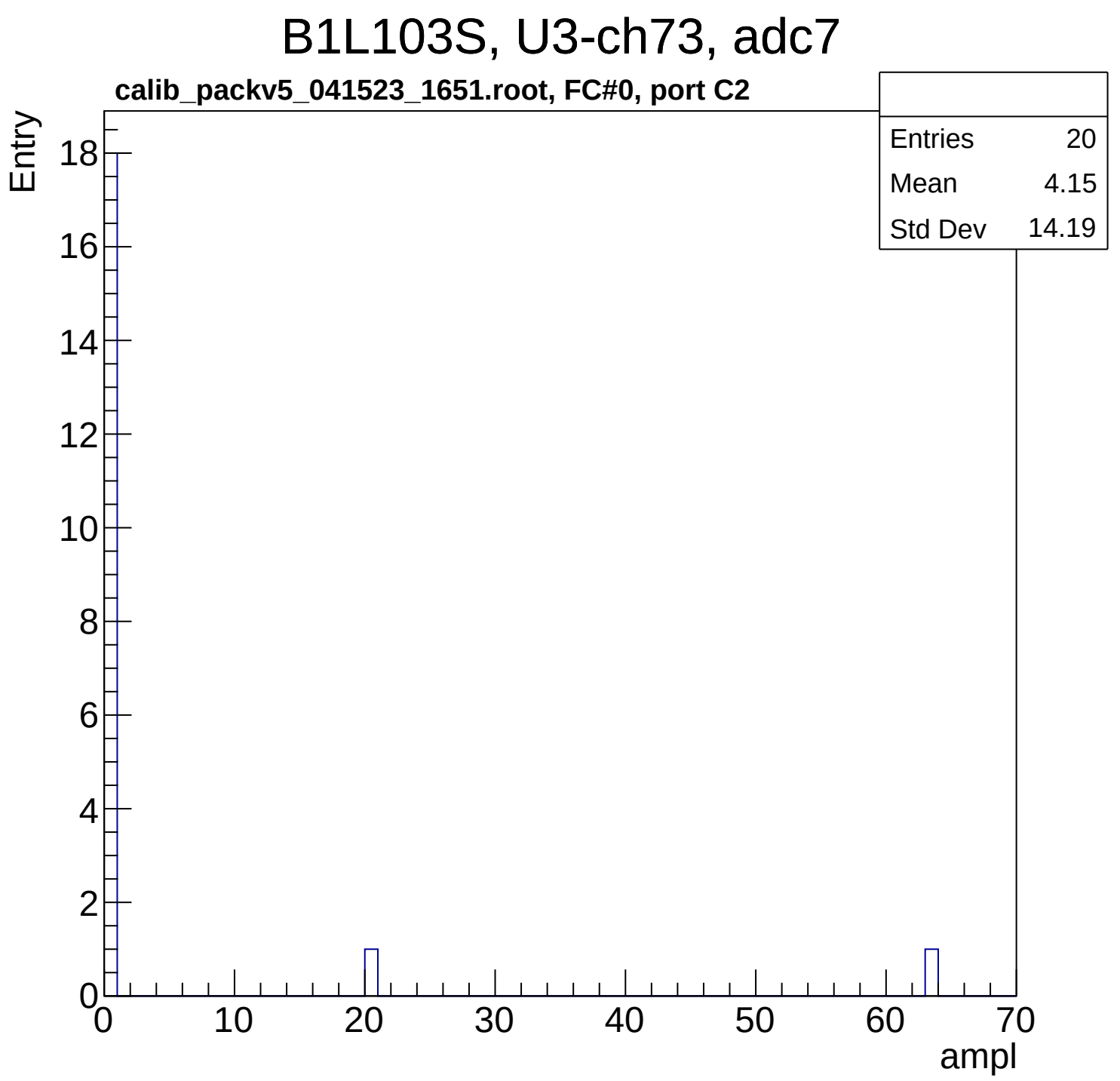
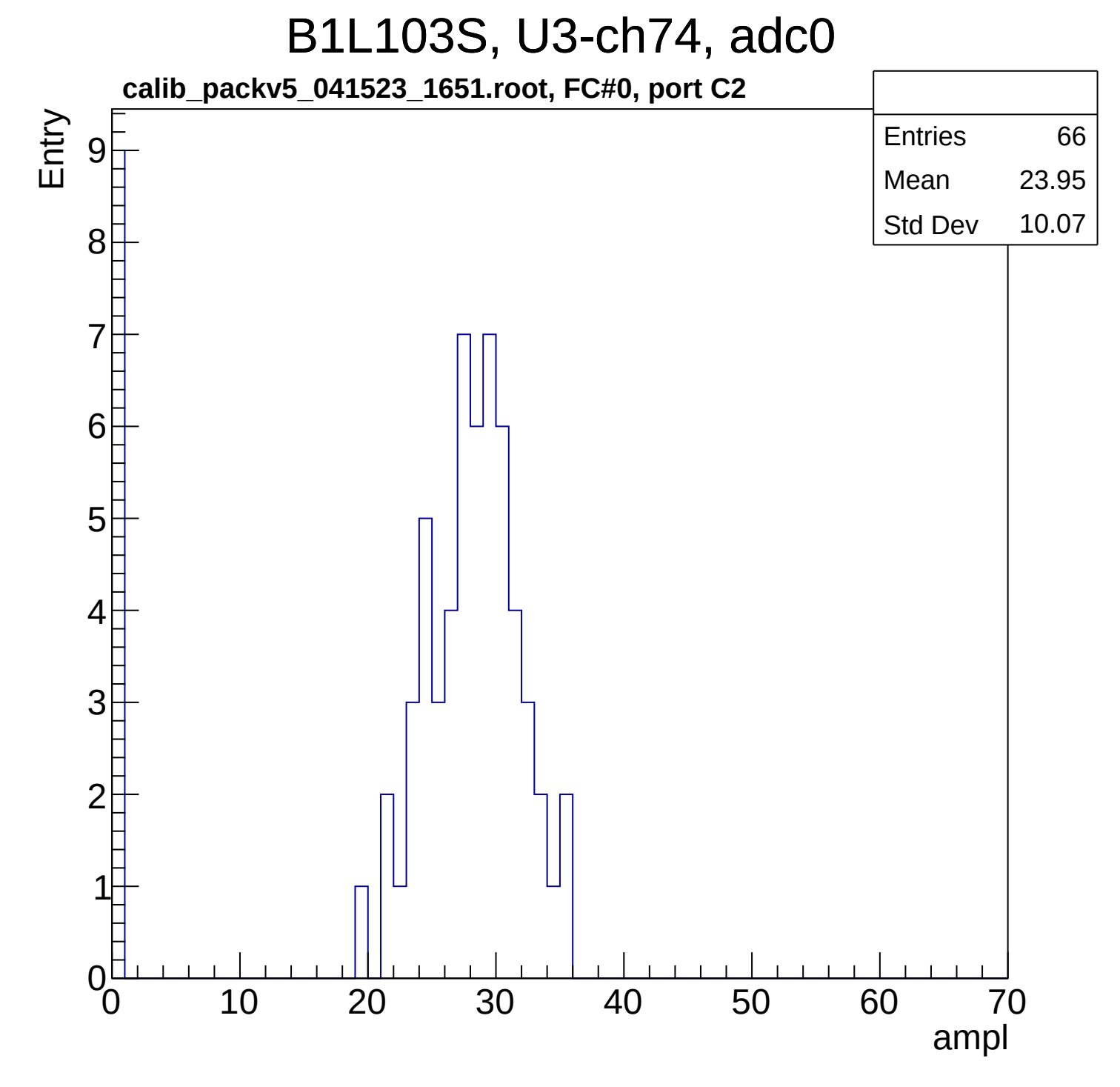

B1L103S, U3-ch73, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4.15
Std Dev 14.19
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch74, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 23.95
Std Dev 10.07
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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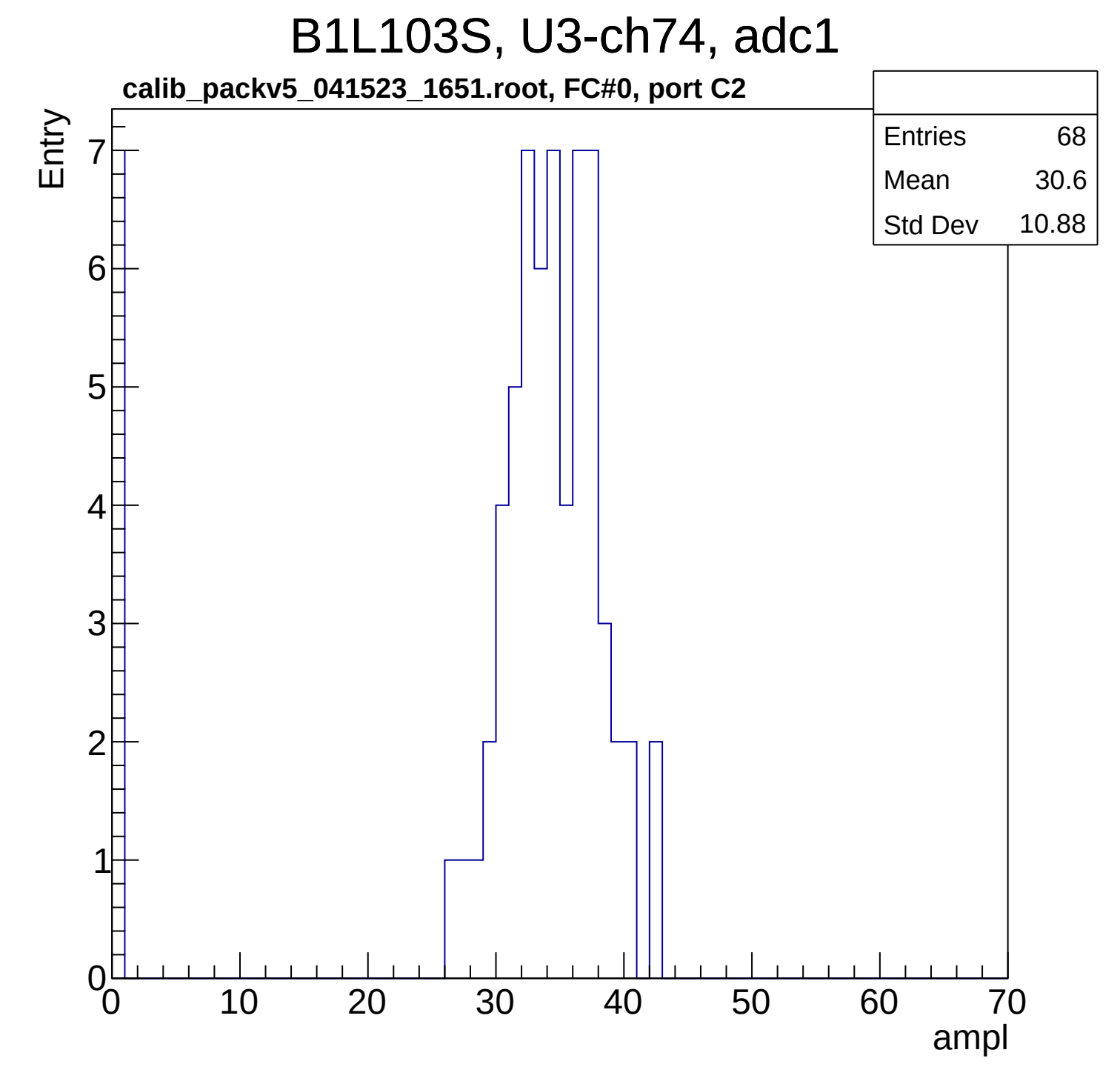
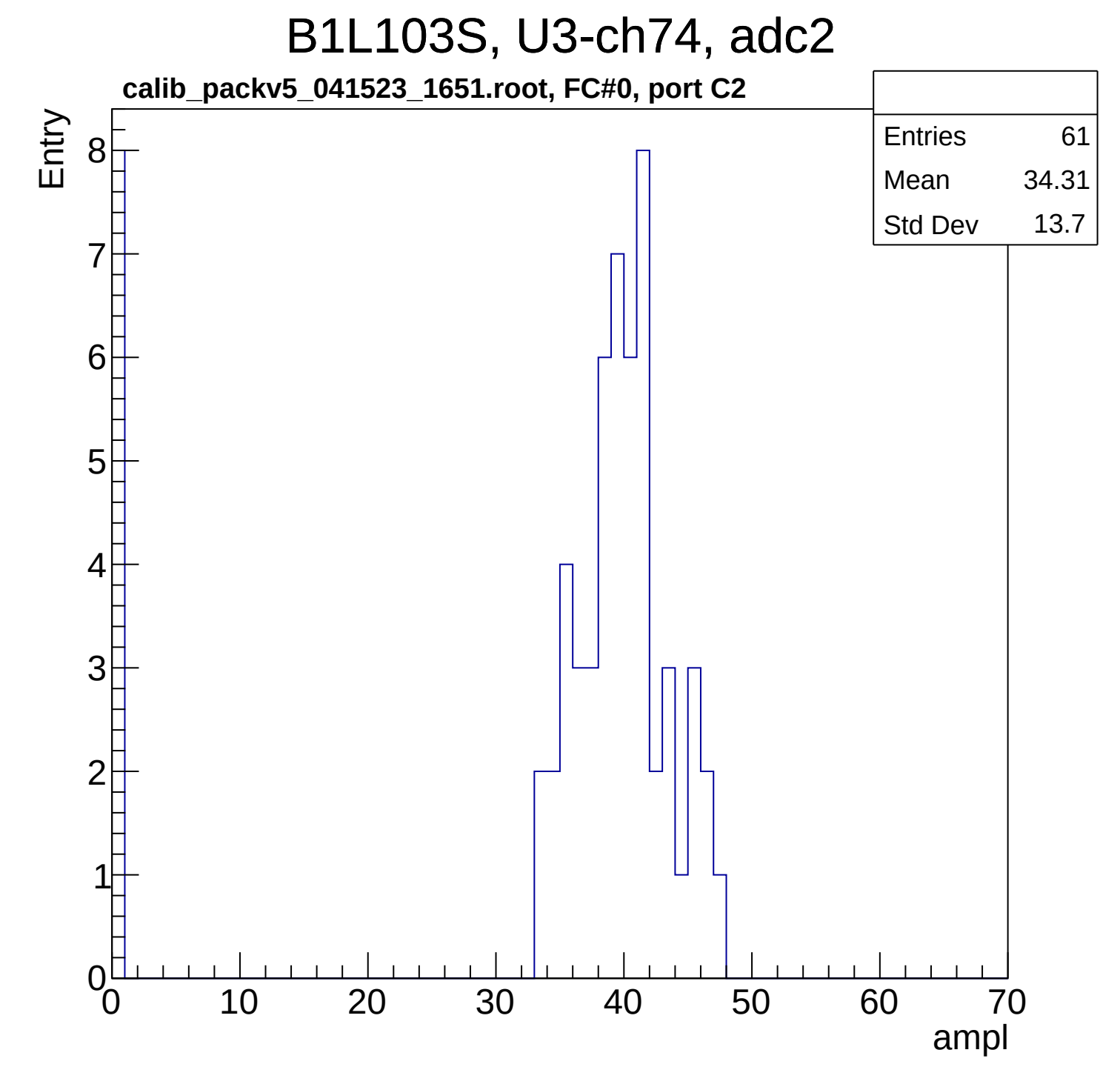

B1L103S, U3-ch74, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 30.6
Std Dev 10.88
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch74, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 34.31
Std Dev 13.7
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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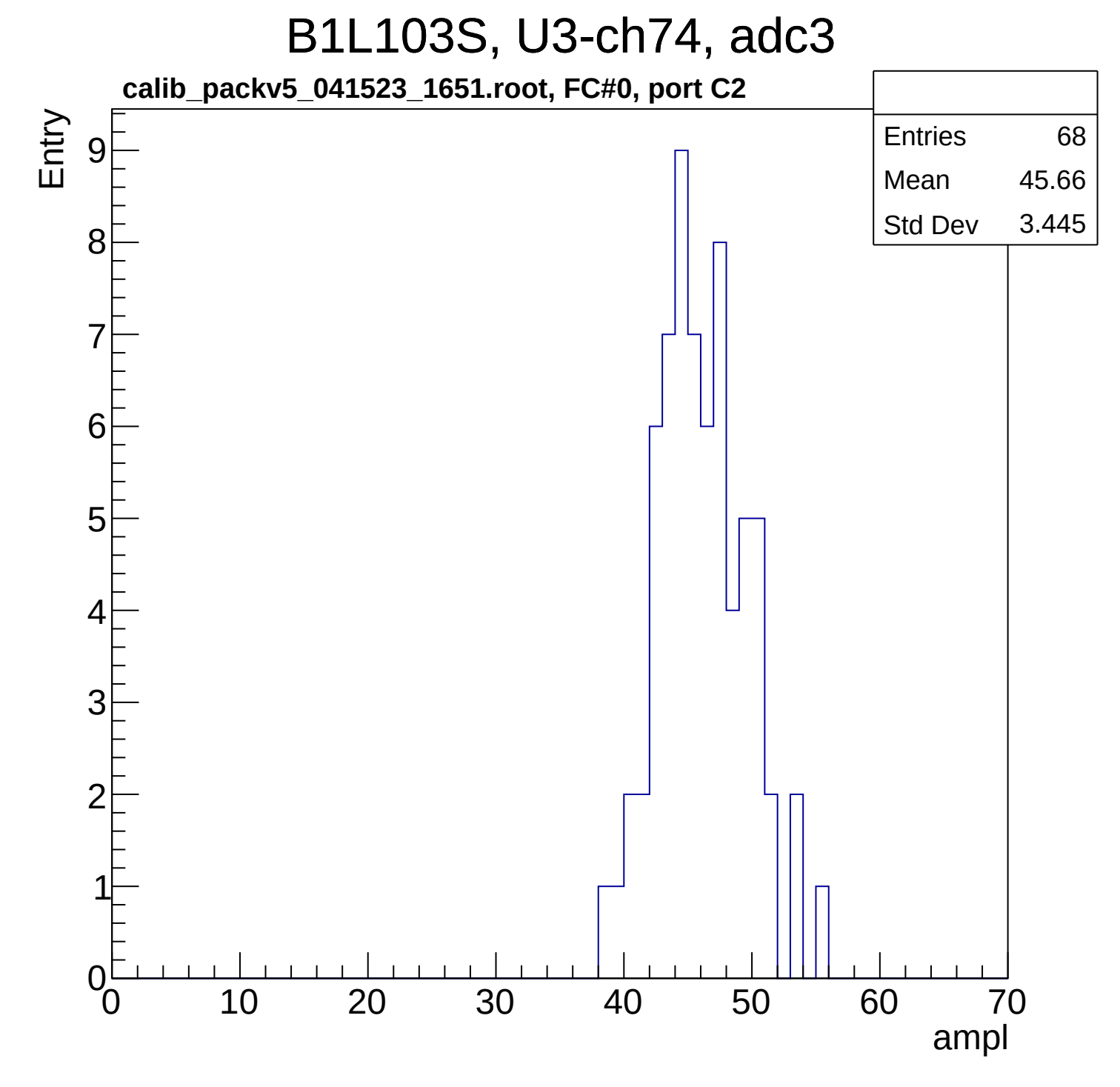
B1L103S, U3-ch74, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 45.66
Std Dev 3.445
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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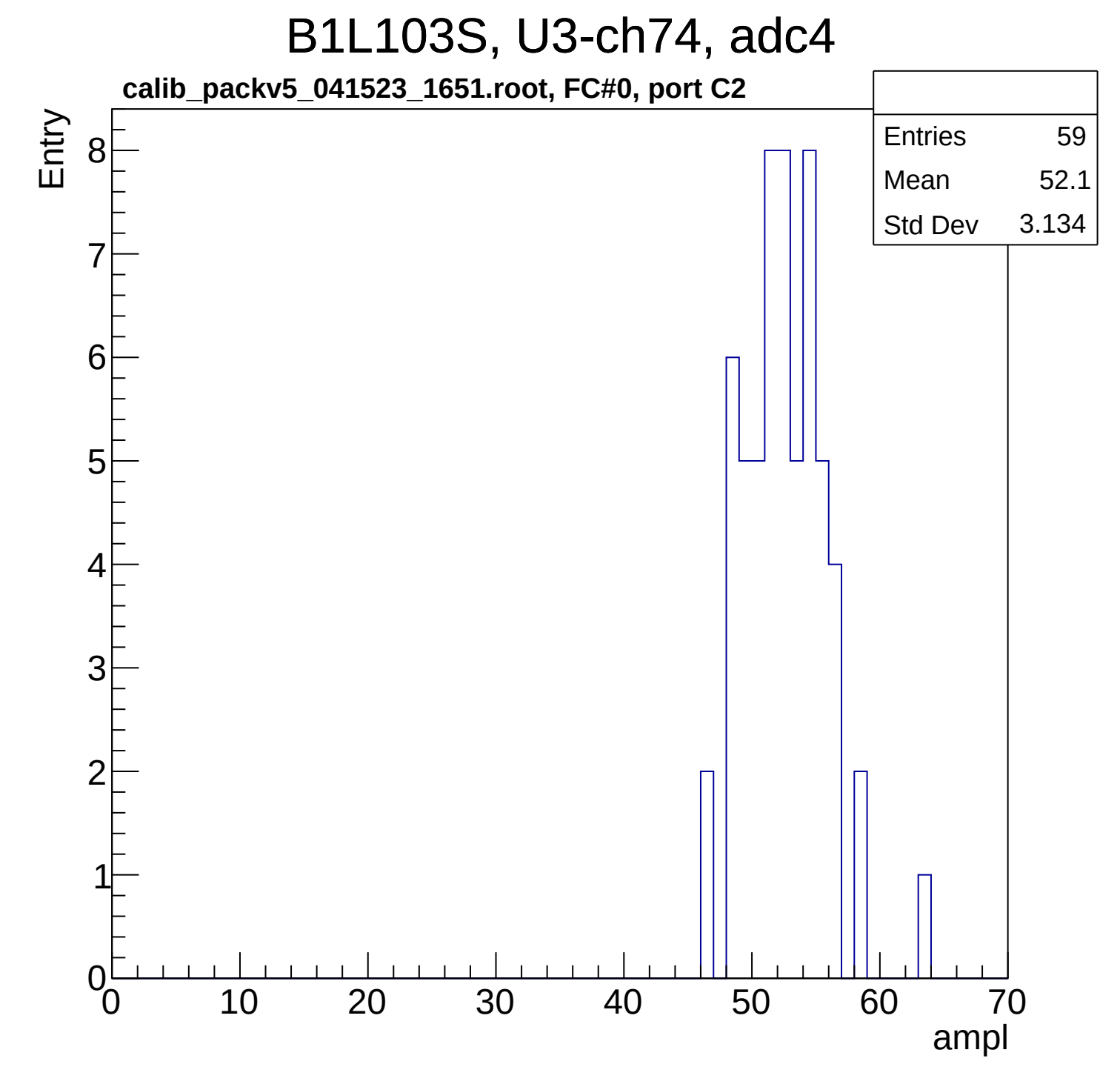
B1L103S, U3-ch74, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 52.1
Std Dev 3.134
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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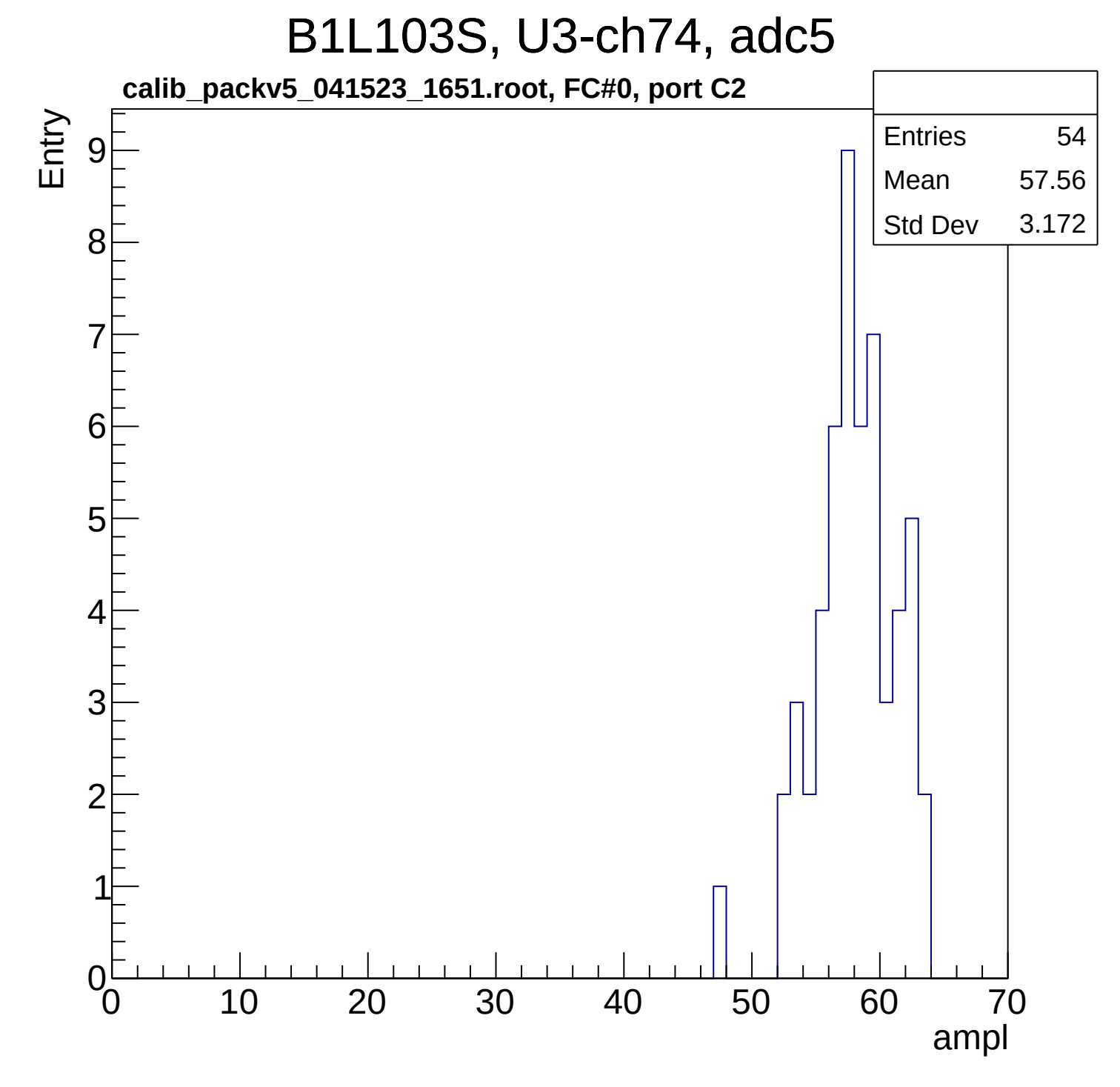
B1L103S, U3-ch74, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 57.56
Std Dev 3.172
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
50
60
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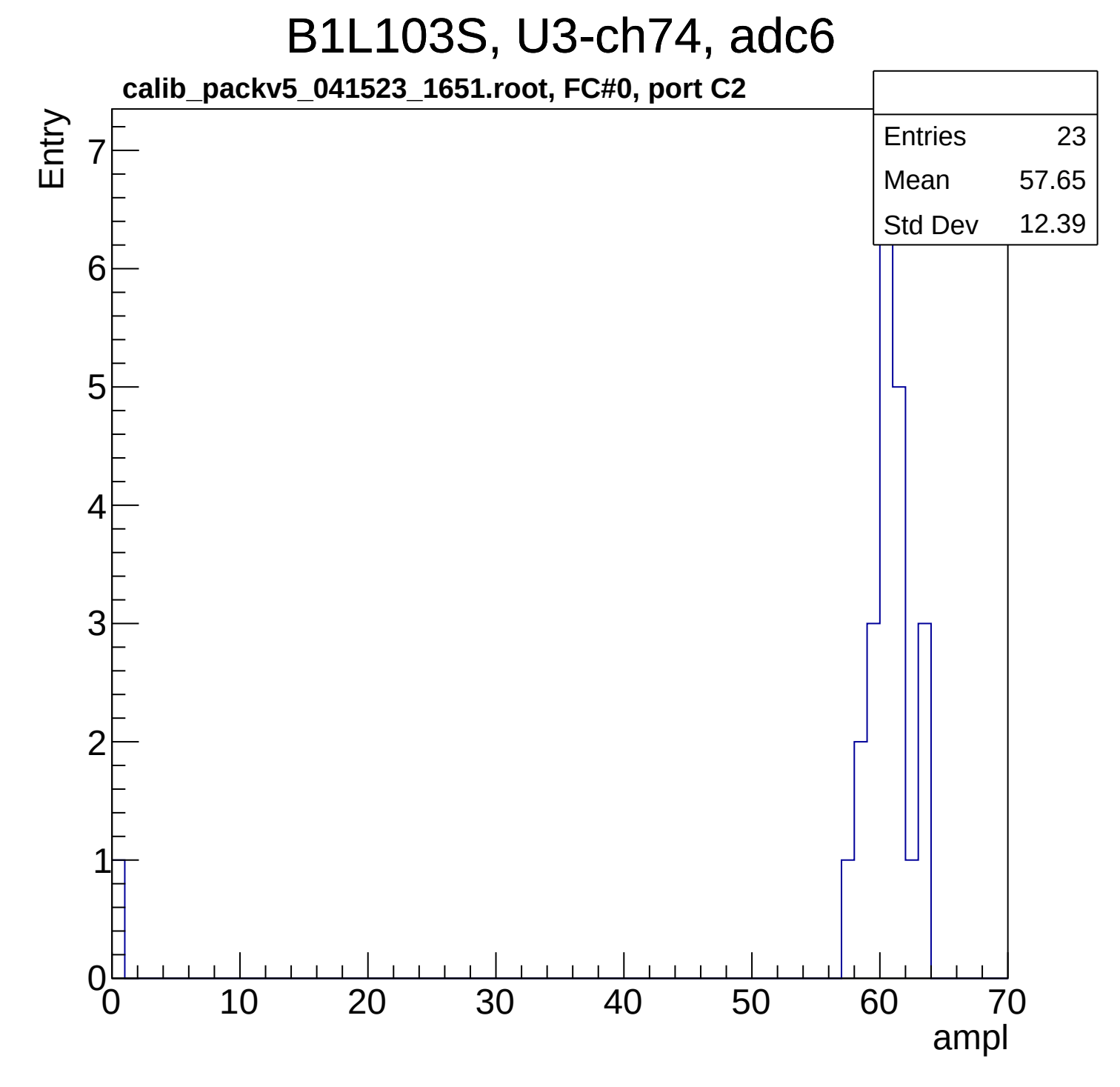
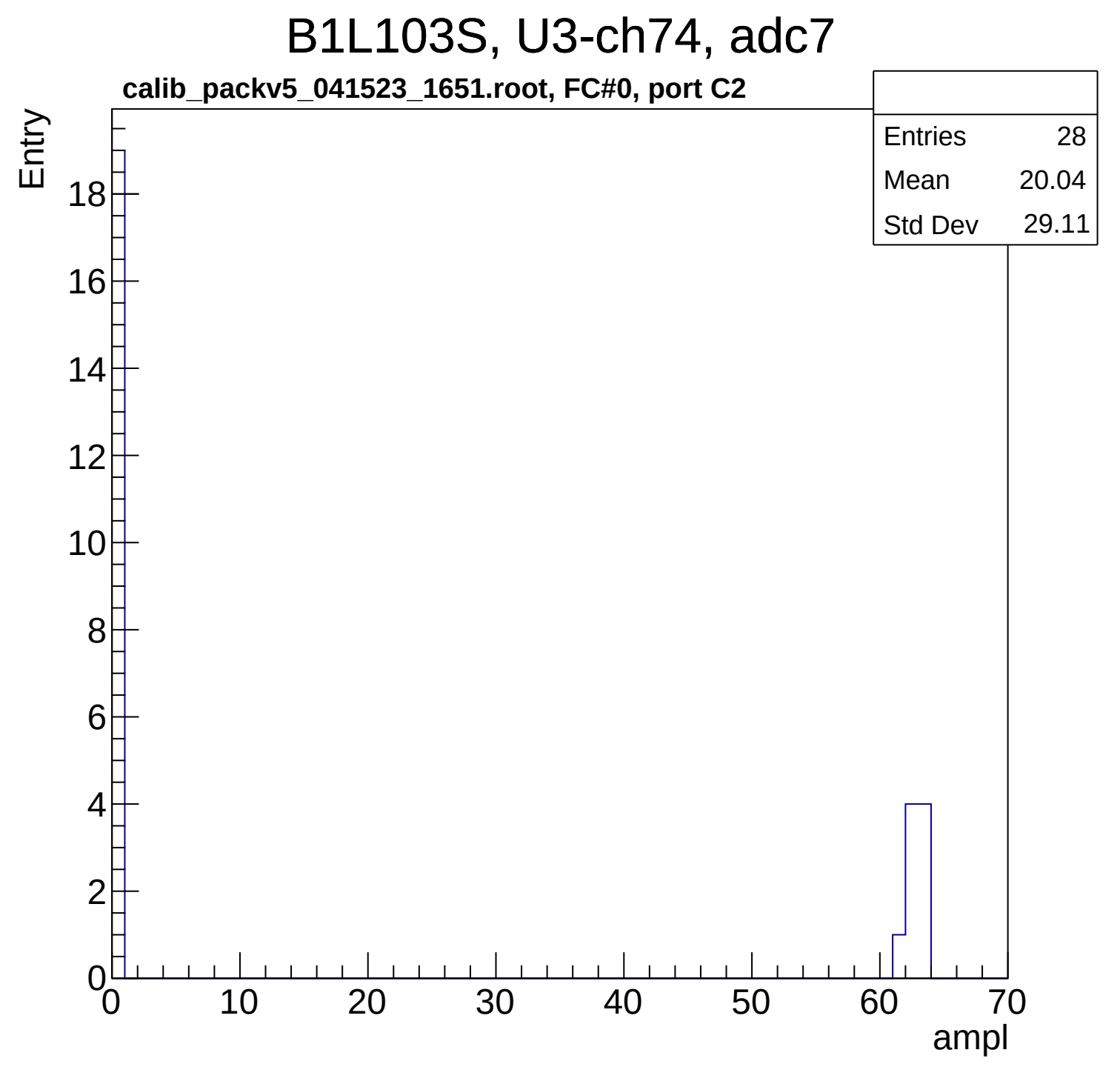
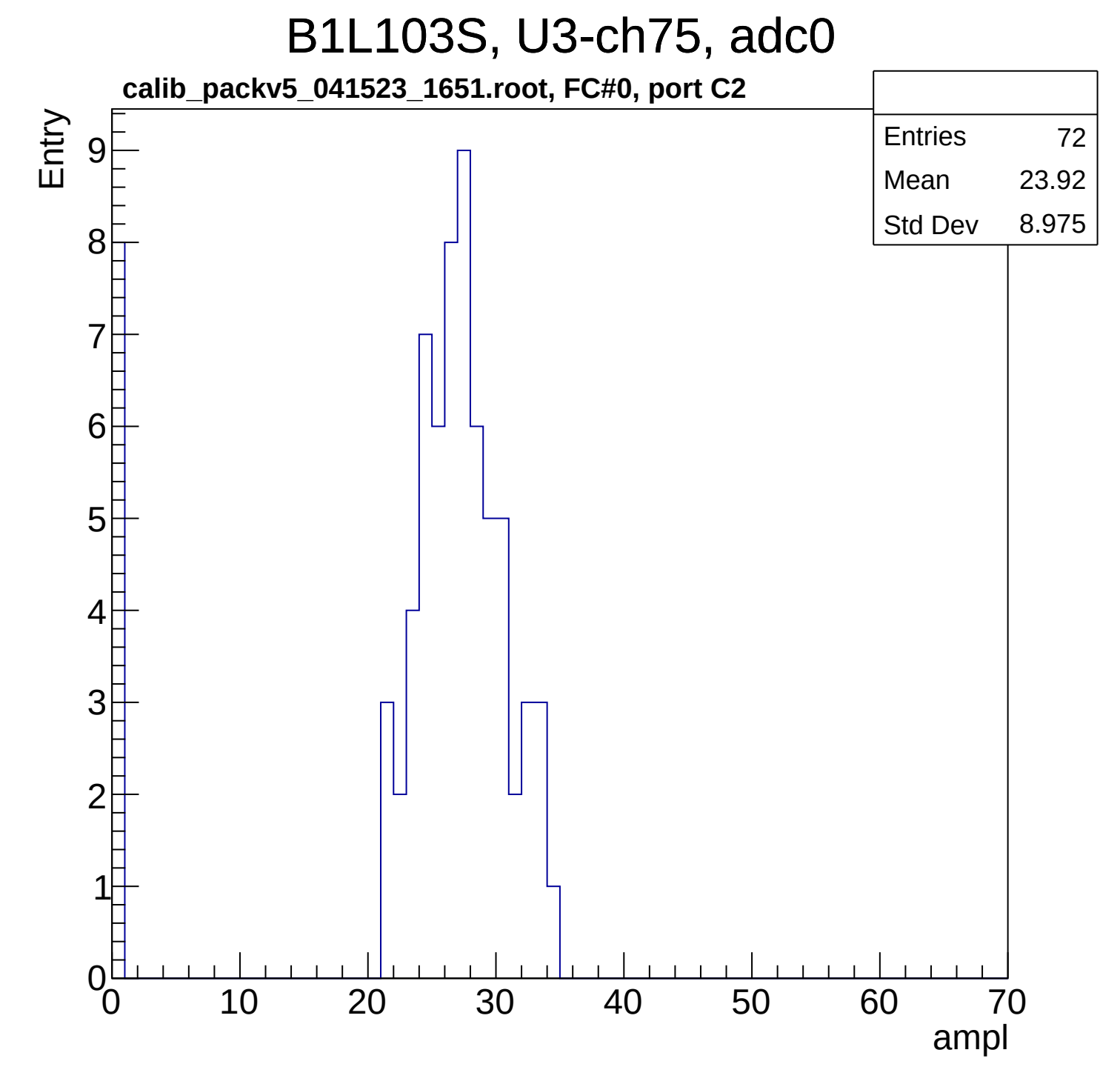
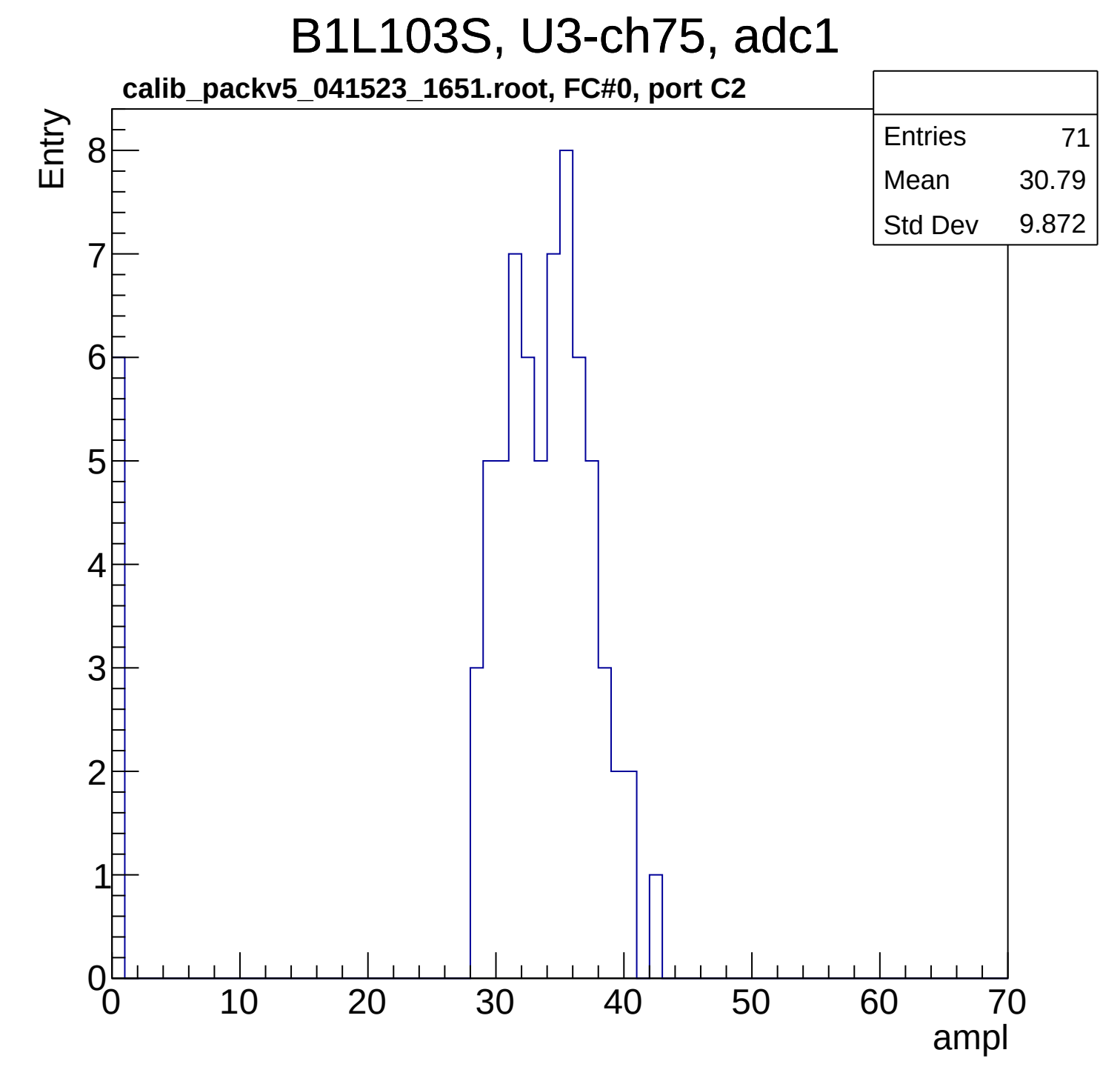

B1L103S, U3-ch74, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 57.65
Std Dev 12.39
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch74, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 20.04
Std Dev 29.11
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch75, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 23.92
Std Dev 8.975
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch75, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 30.79
Std Dev 9.872
Entry
ampl
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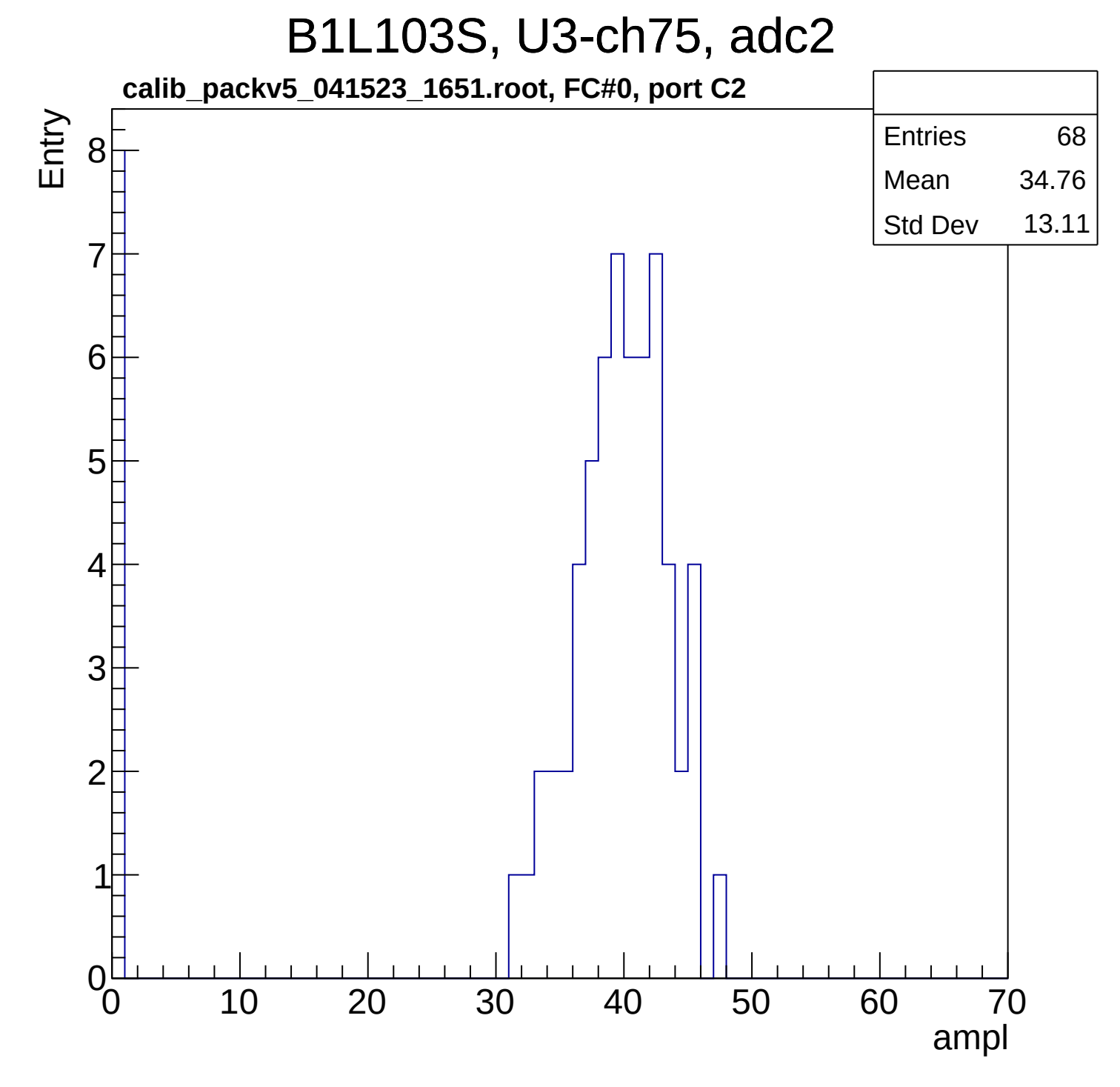
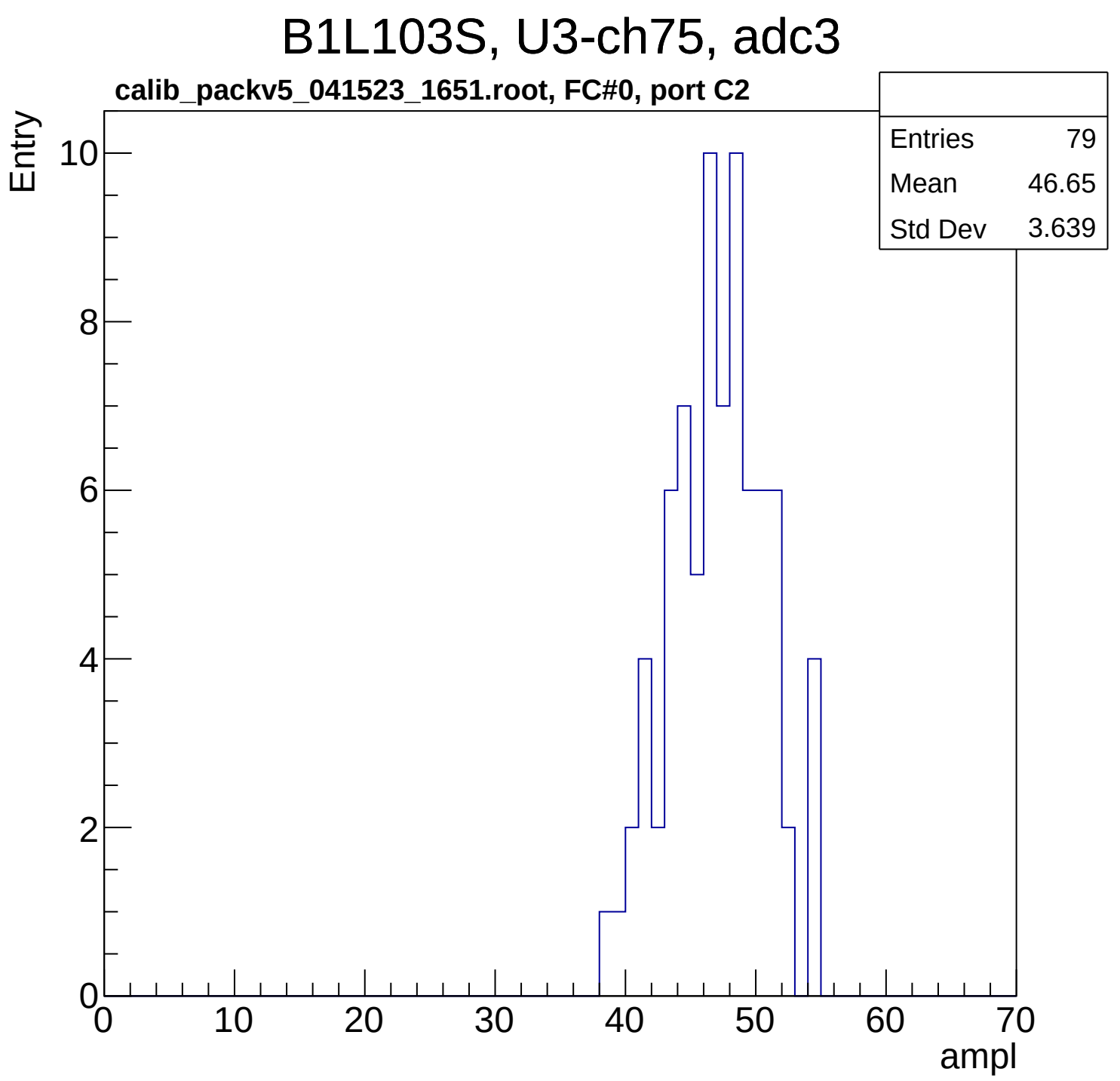
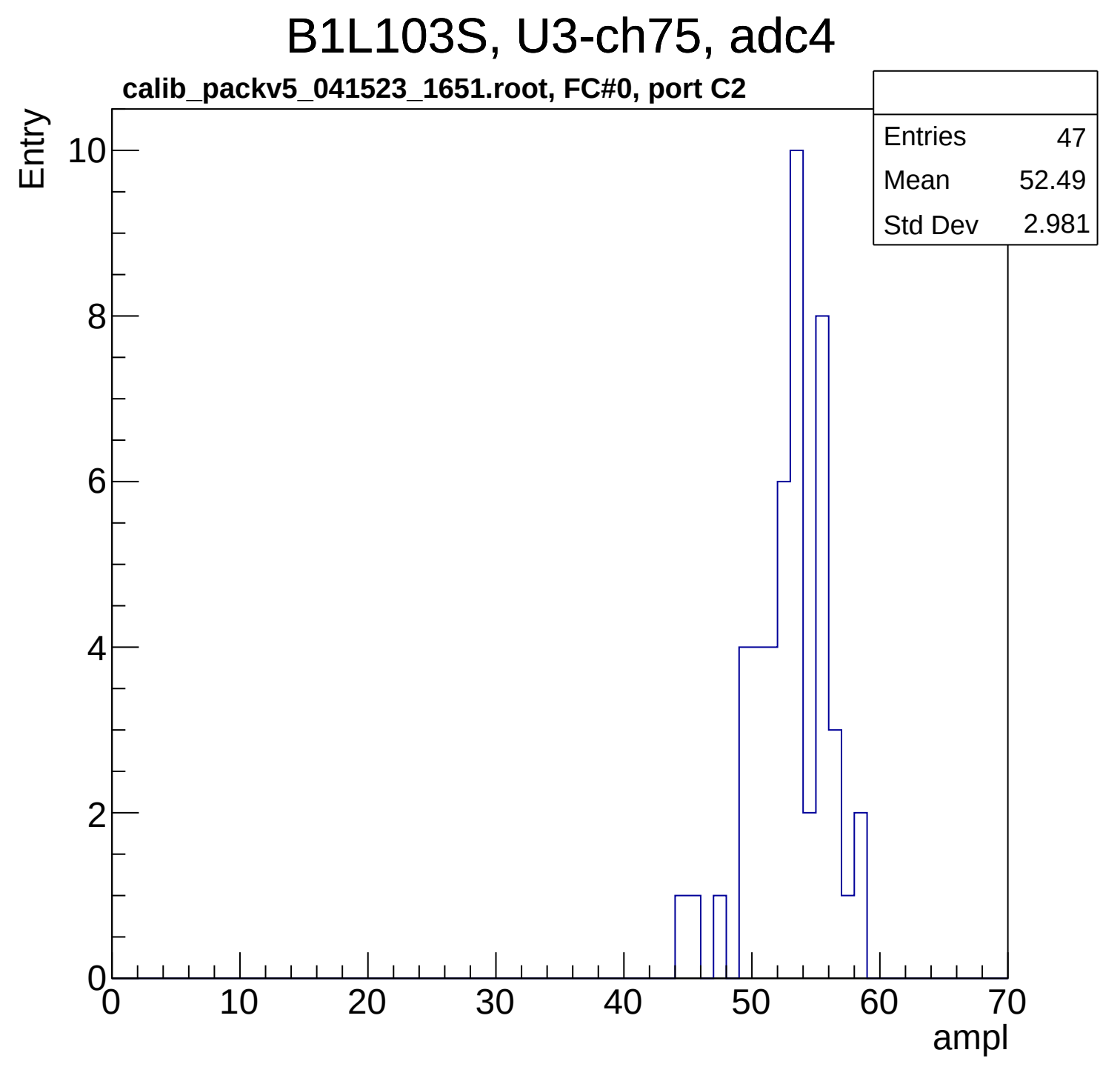
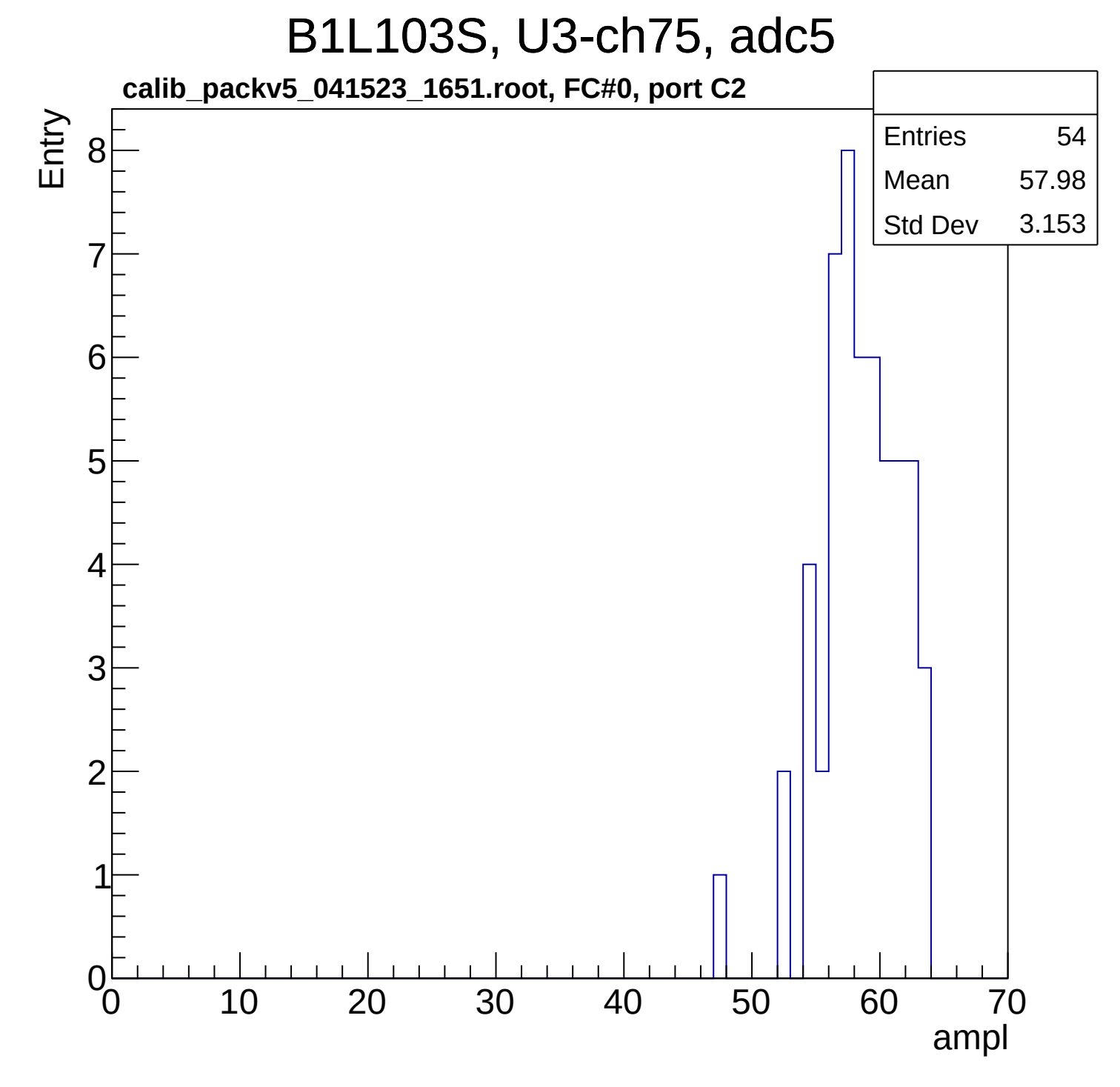
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch75, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 34.76
Std Dev 13.11
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch75, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 46.65
Std Dev 3.639
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U3-ch75, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 52.49
Std Dev 2.981
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U3-ch75, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 57.98
Std Dev 3.153
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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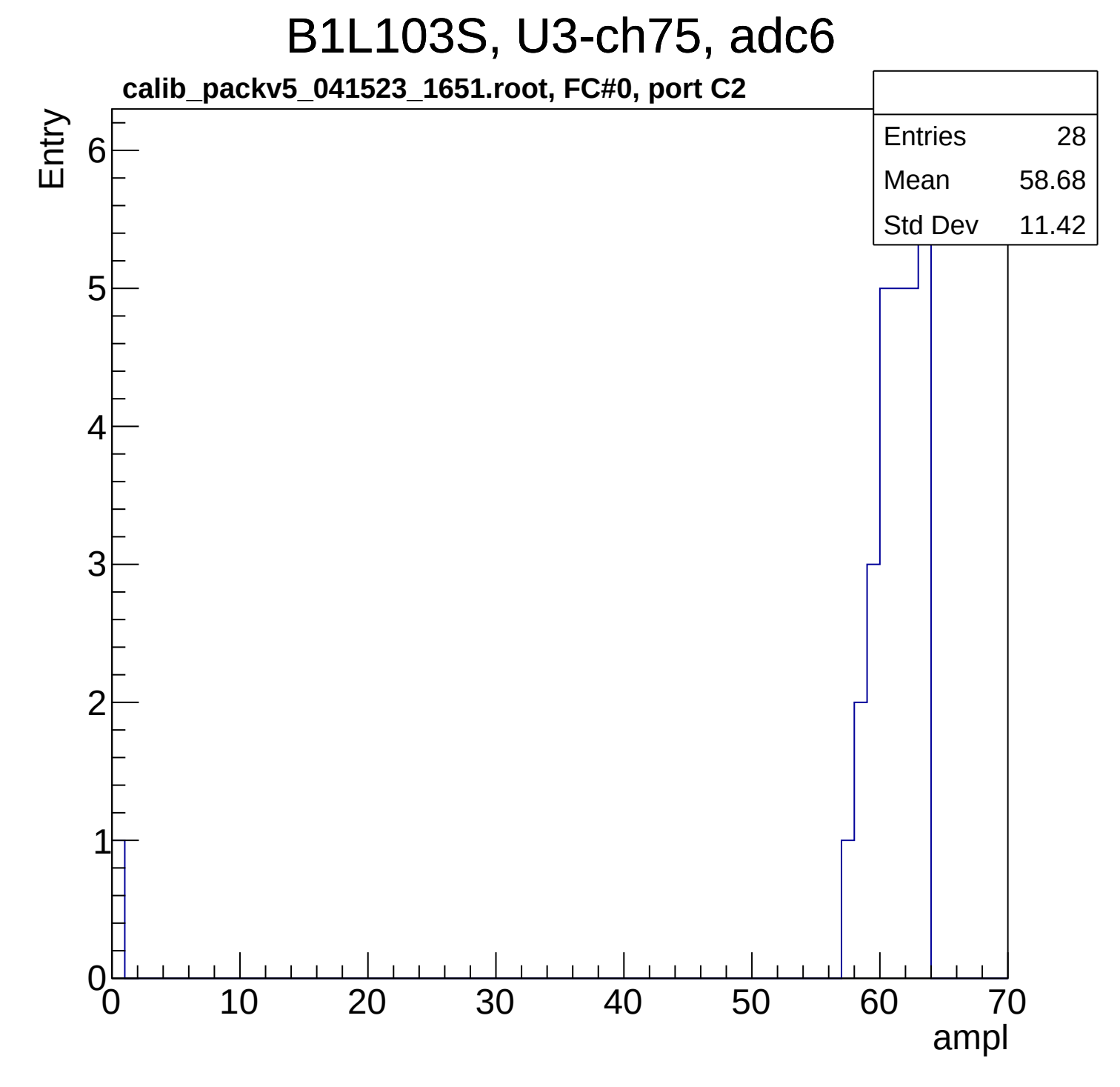
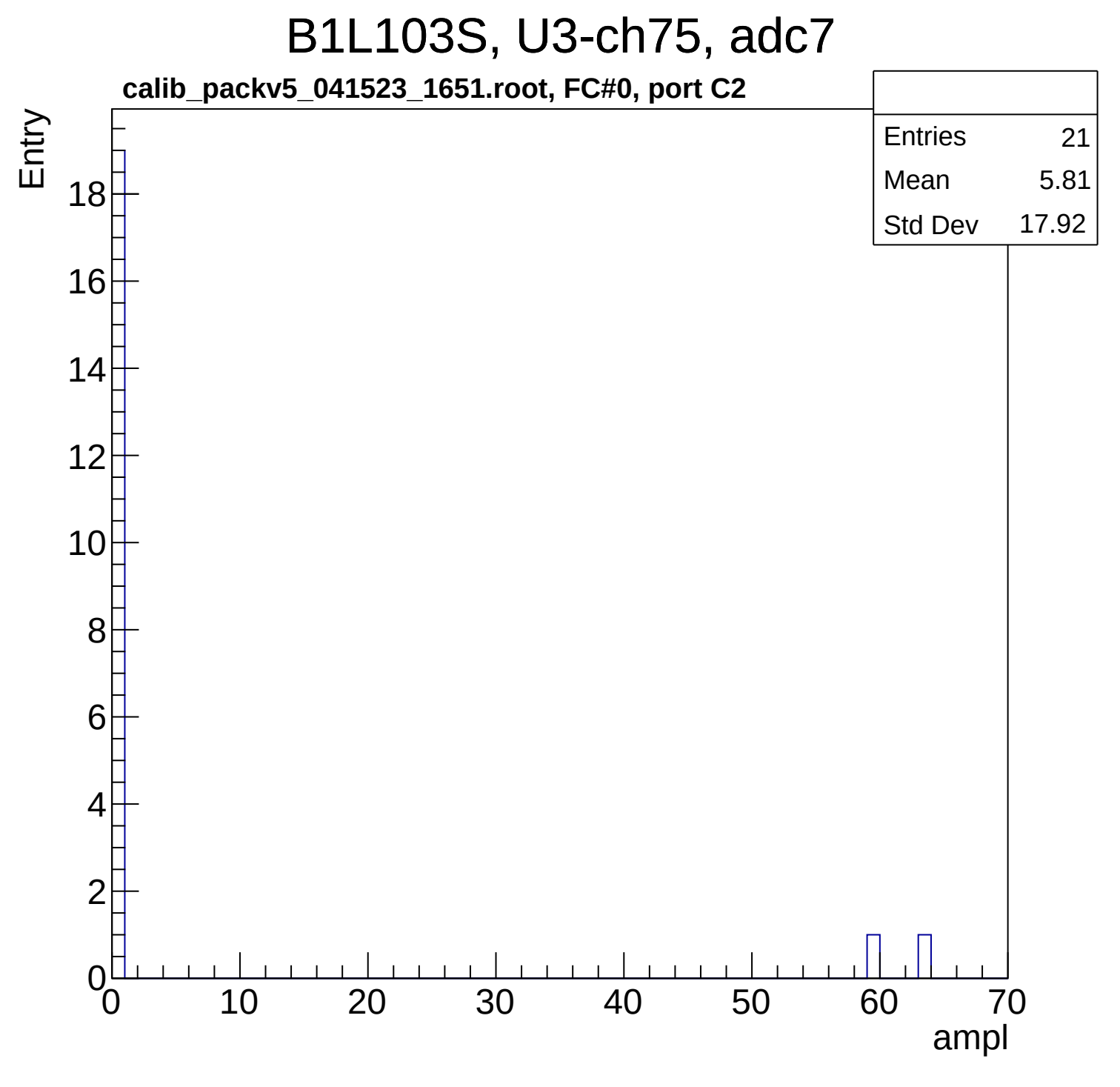
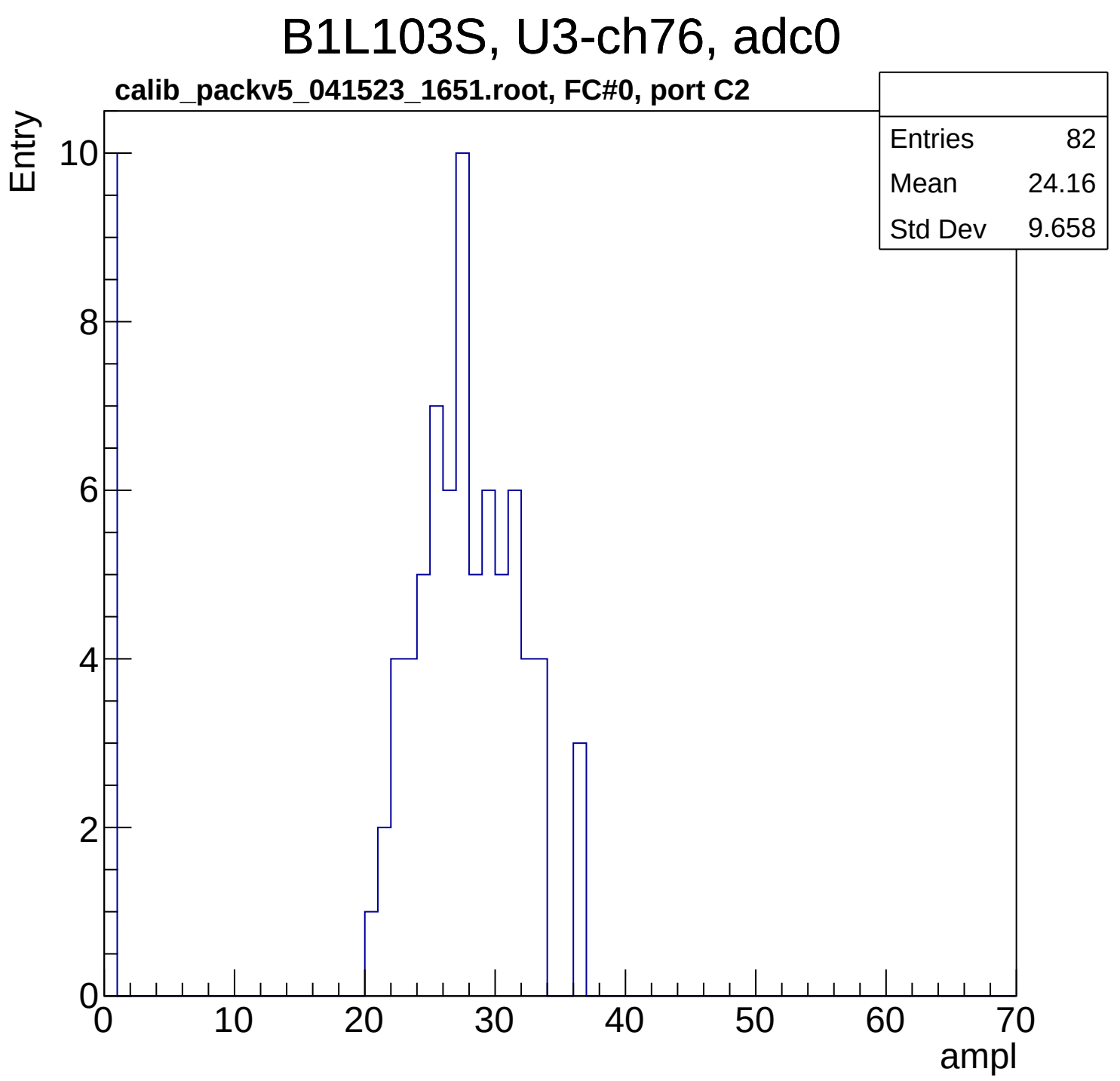
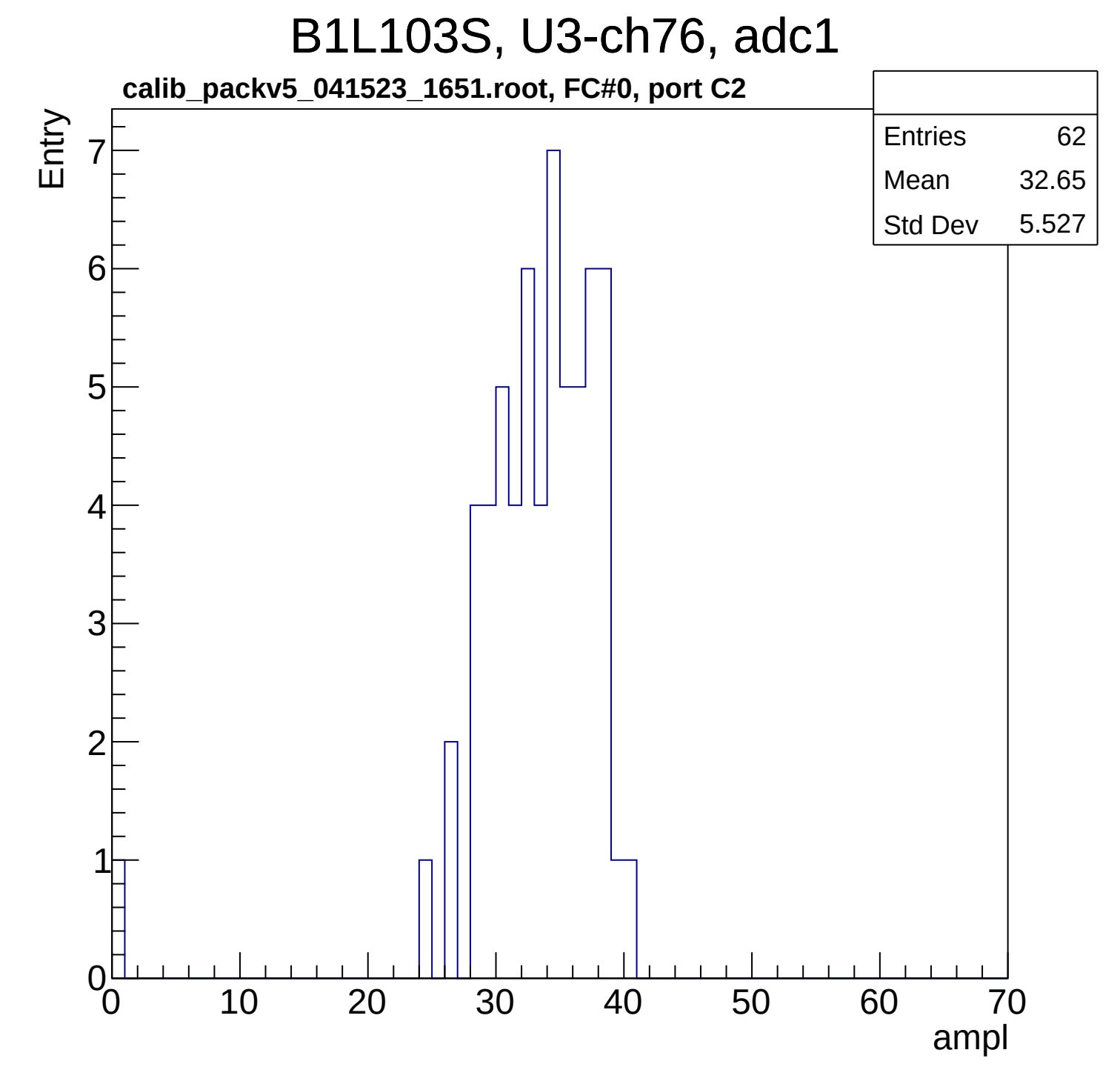
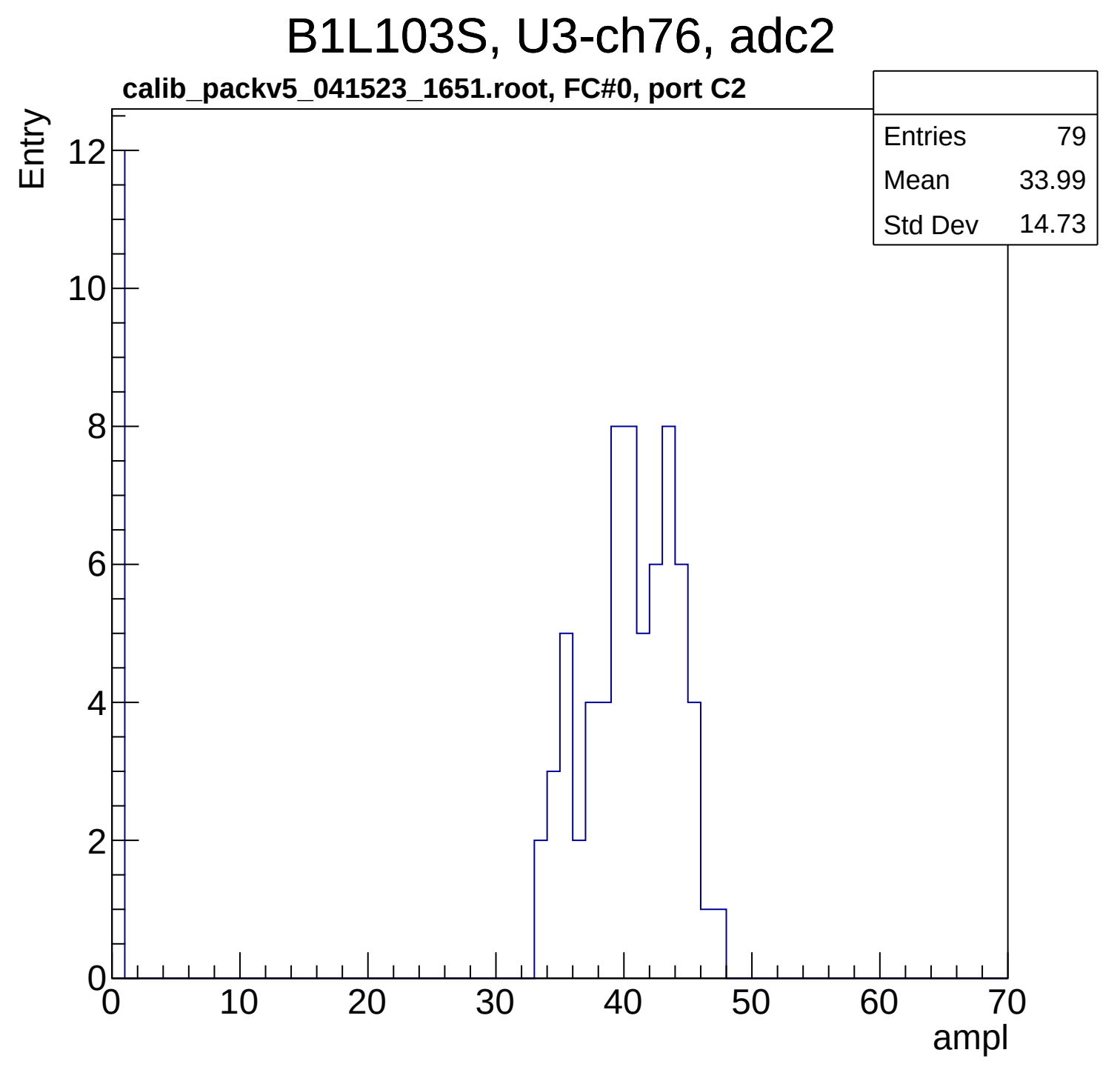
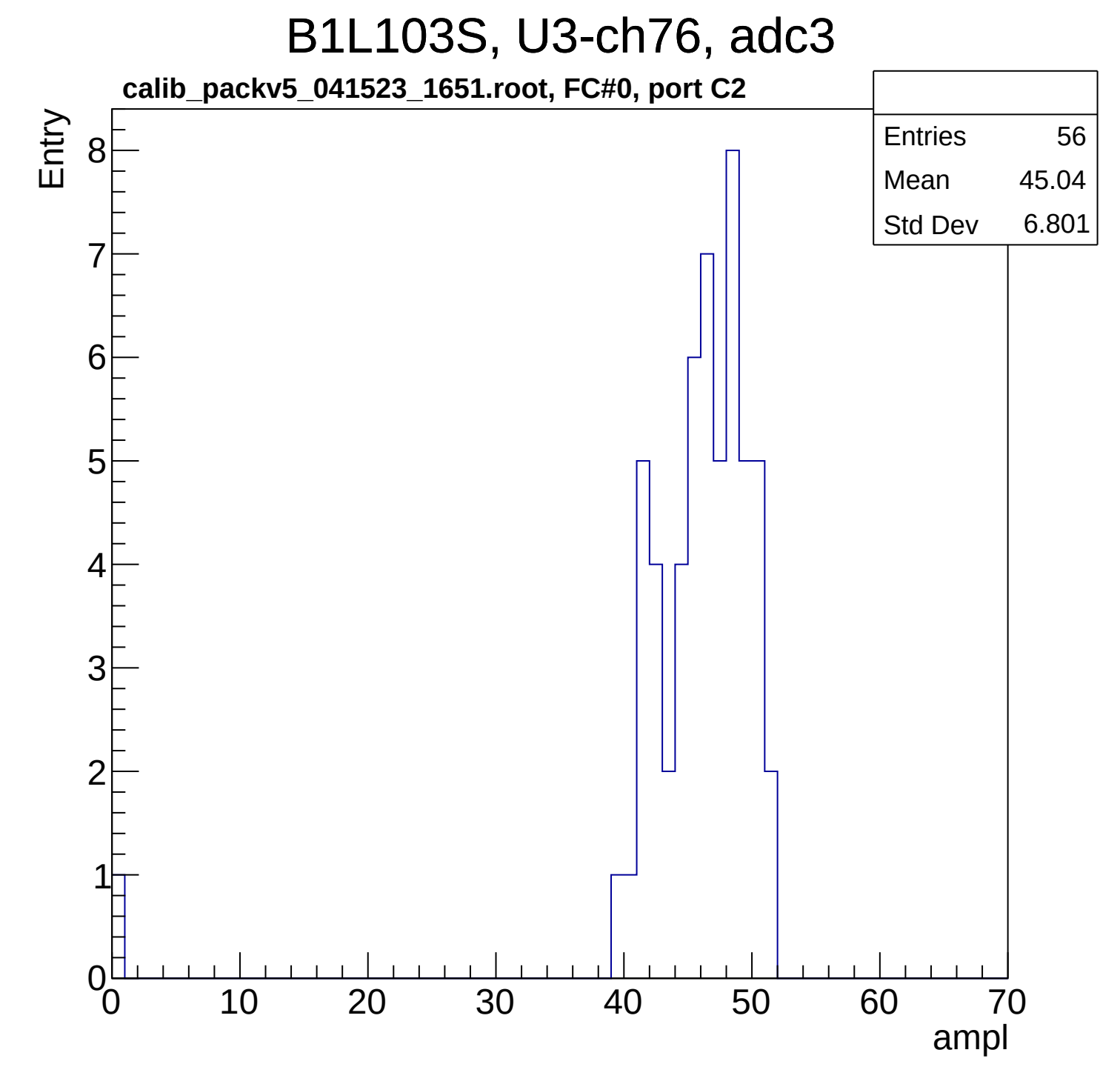

B1L103S, U3-ch75, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 58.68
Std Dev 11.42
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch75, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.81
Std Dev 17.92
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch76, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 24.16
Std Dev 9.658
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch76, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 32.65
Std Dev 5.527
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch76, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 33.99
Std Dev 14.73
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch76, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 45.04
Std Dev 6.801
Entry
ampl
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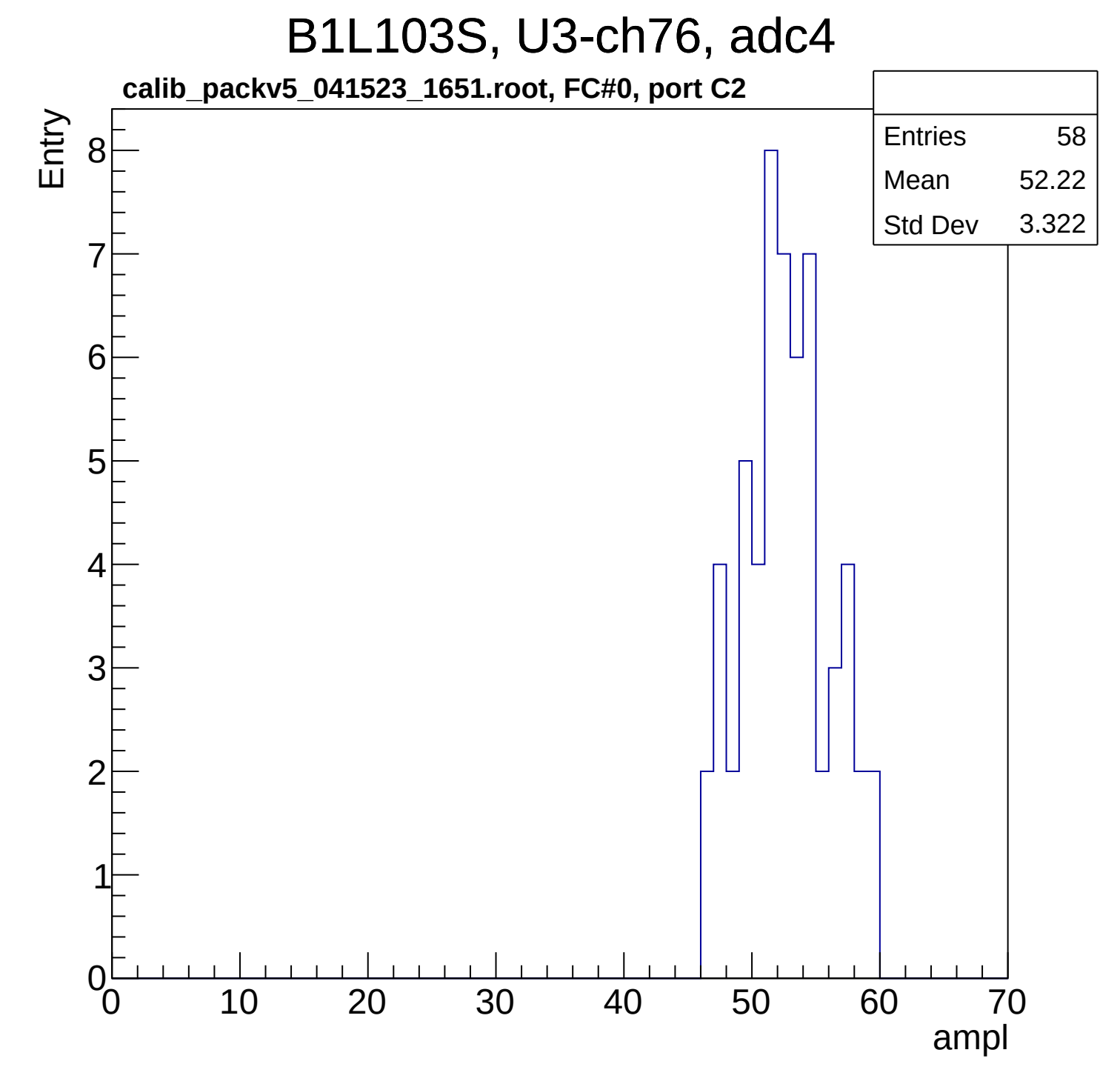
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch76, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 52.22
Std Dev 3.322
Entry
ampl
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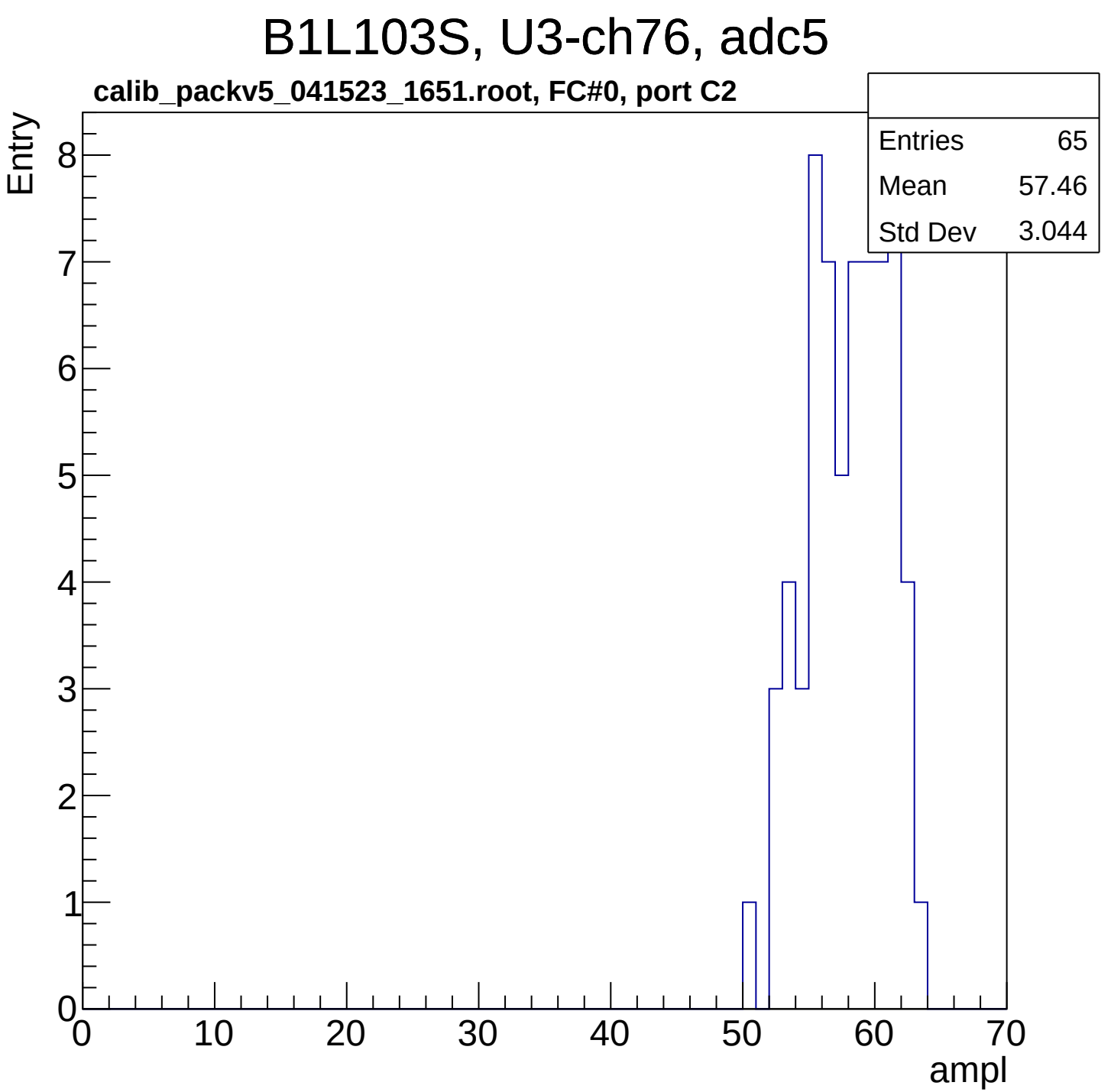
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch76, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 57.46
Std Dev 3.044
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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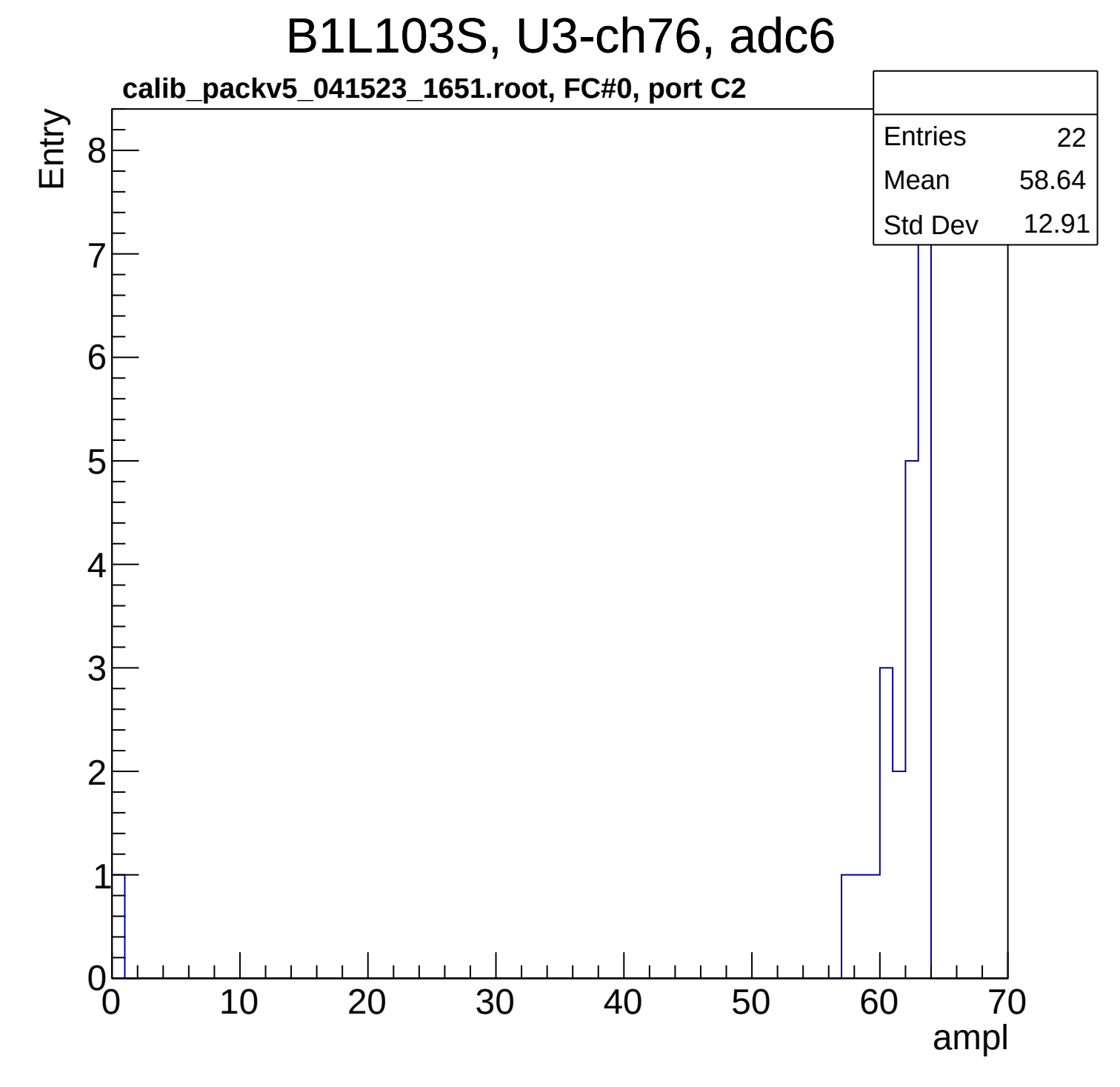
40
50
60
70


B1L103S, U3-ch76, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 58.64
Std Dev 12.91
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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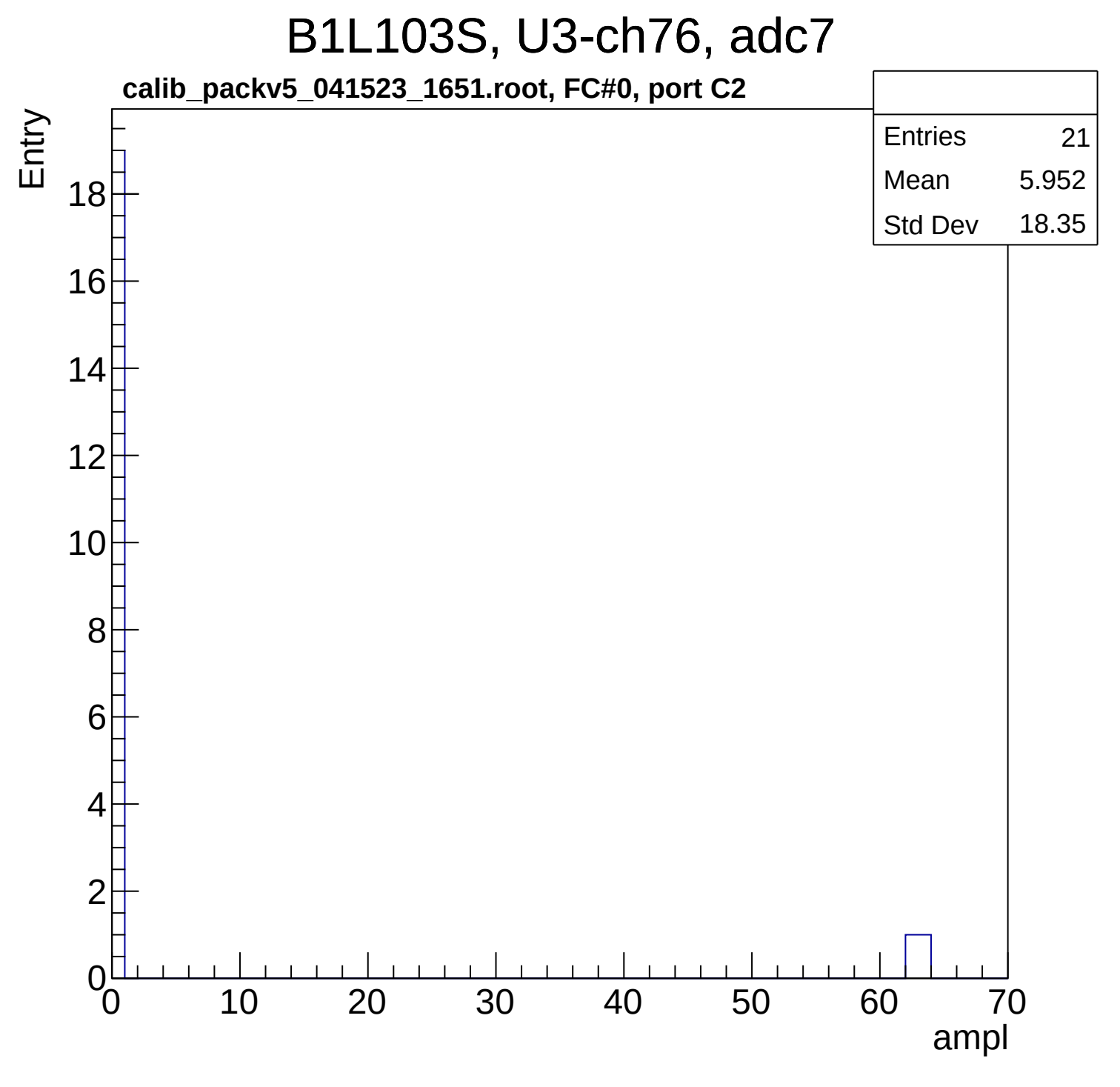
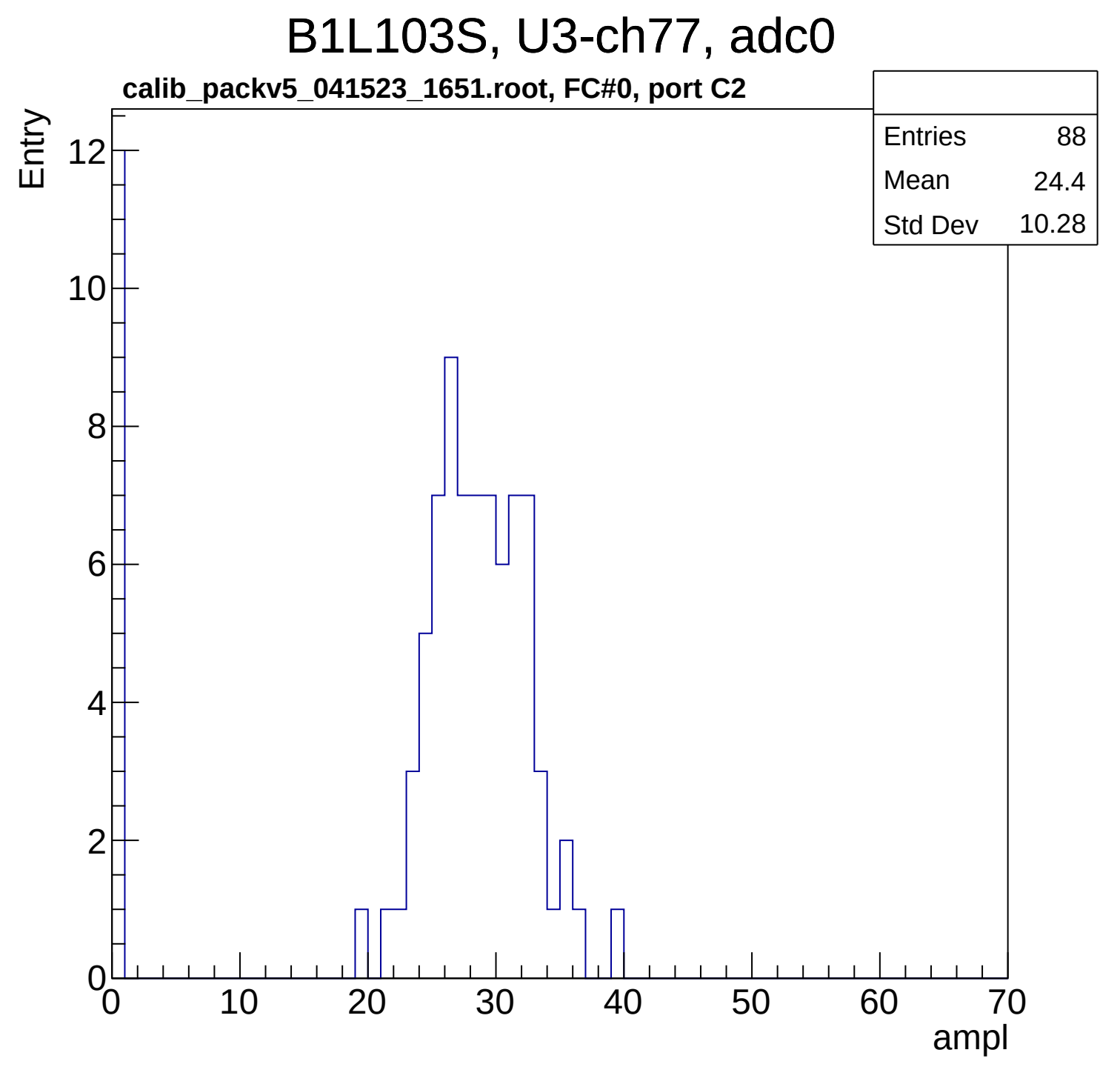
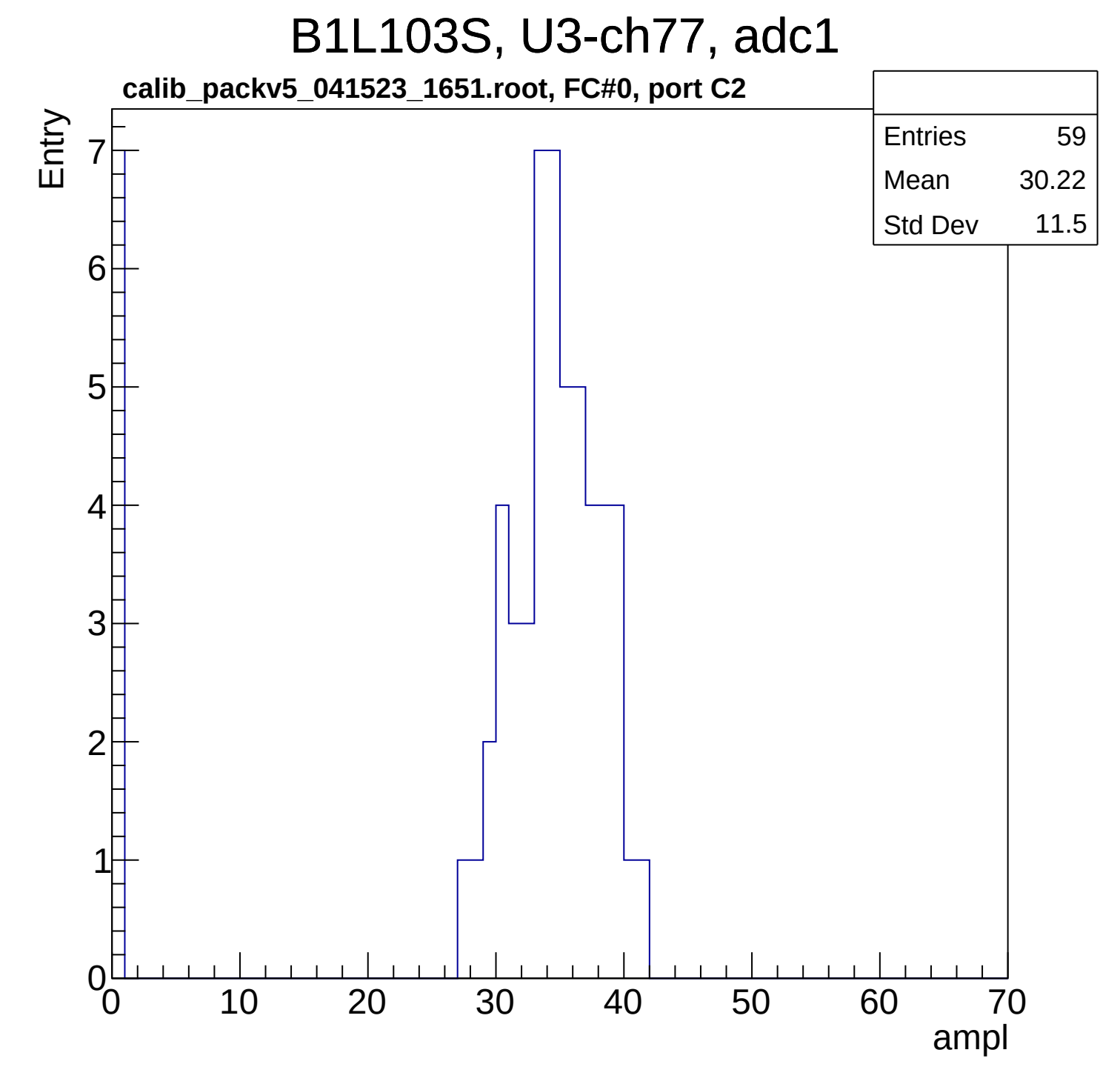
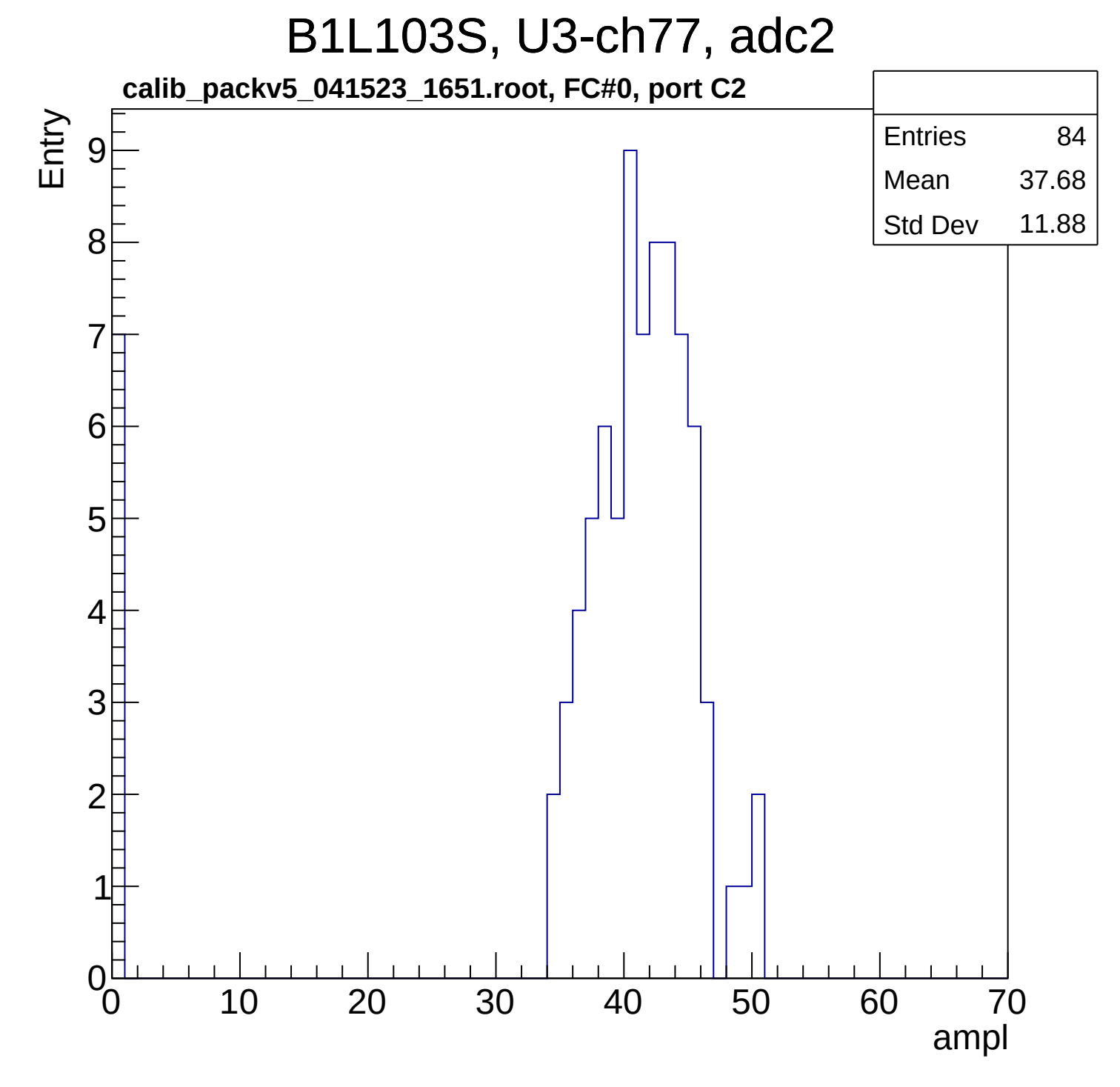
40
50
60
70


B1L103S, U3-ch76, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.952
Std Dev 18.35
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch77, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 24.4
Std Dev 10.28
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch77, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 30.22
Std Dev 11.5
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch77, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 37.68
Std Dev 11.88
Entry
ampl
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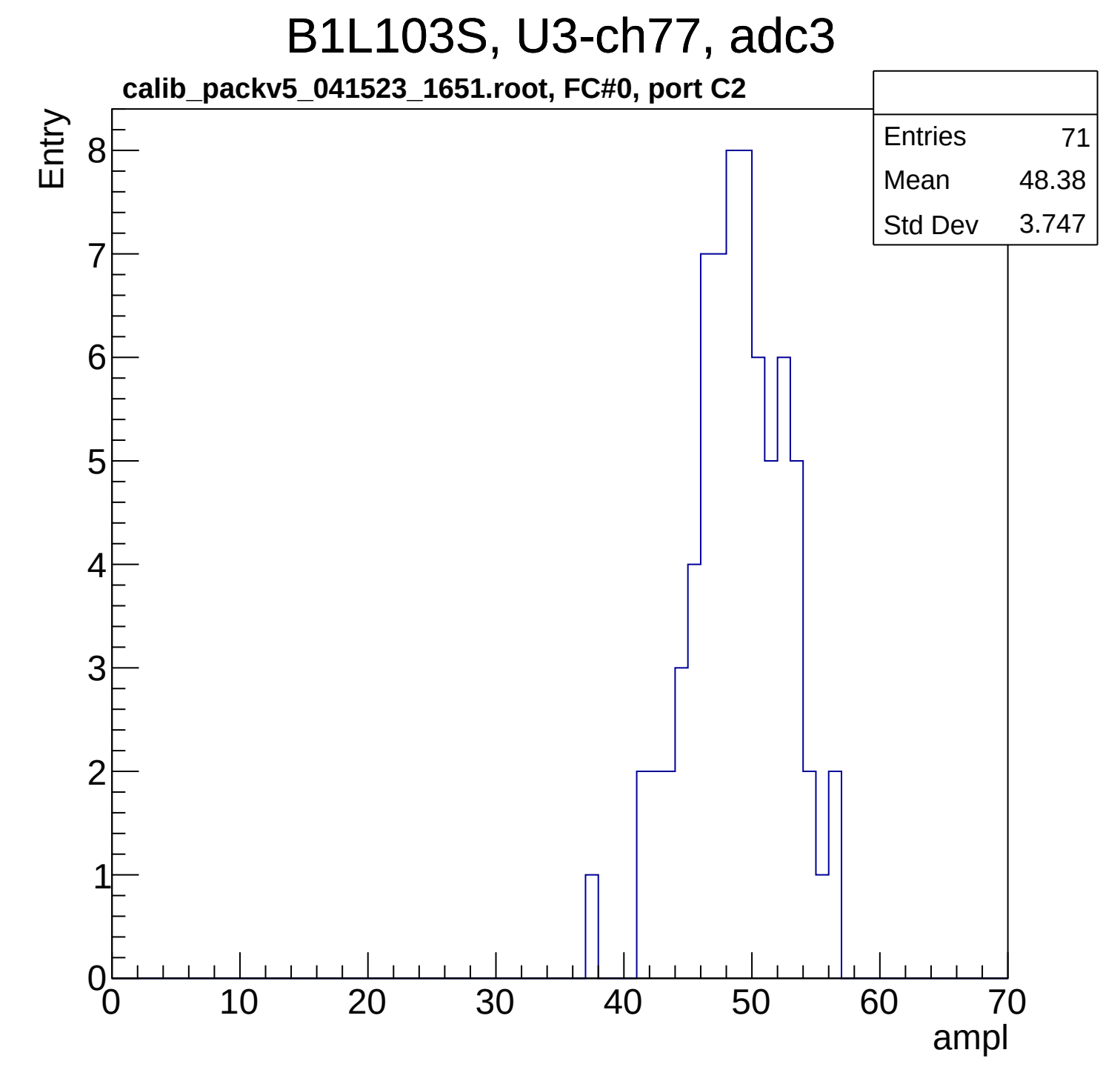
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch77, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 48.38
Std Dev 3.747
Entry
ampl
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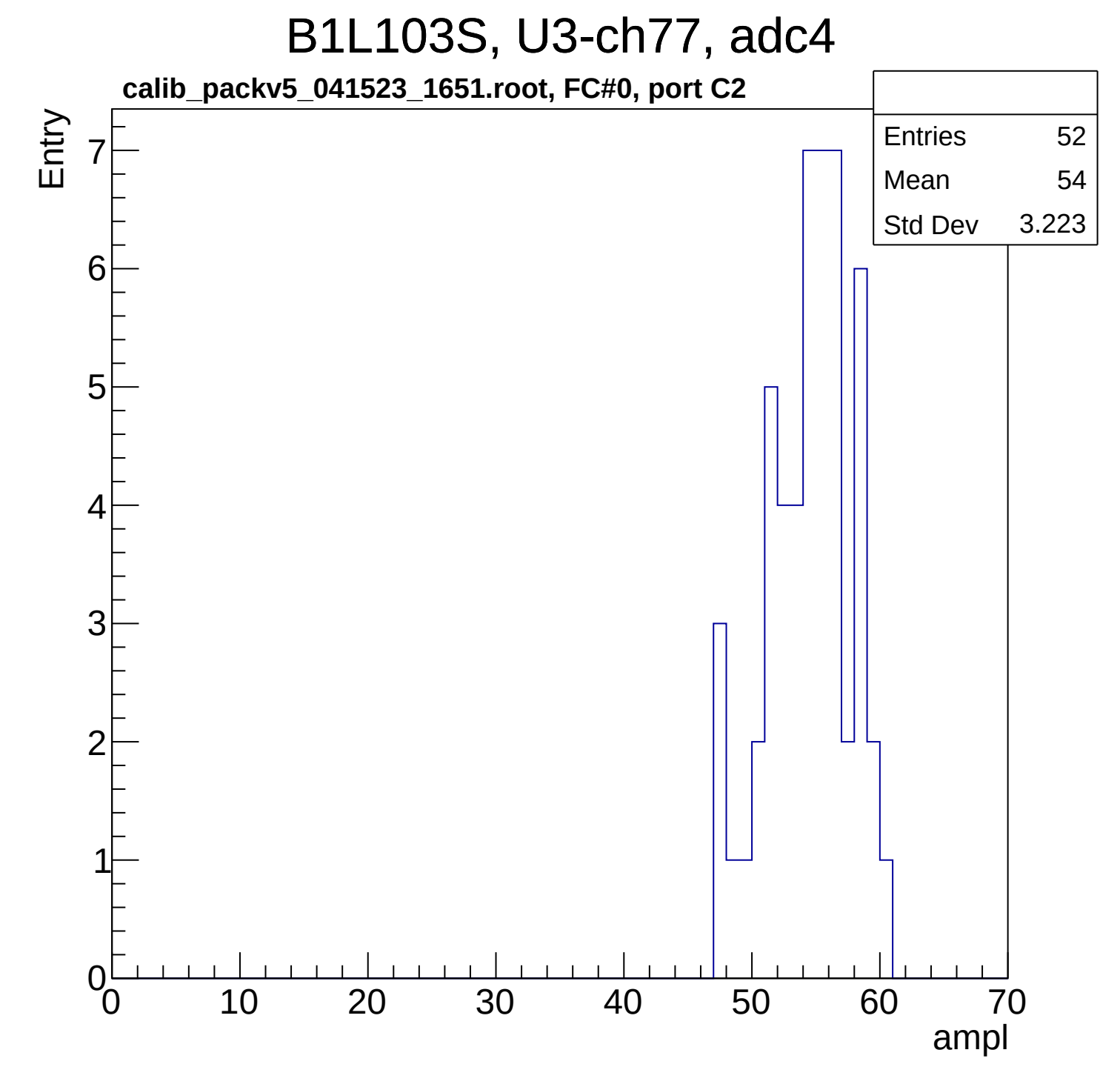
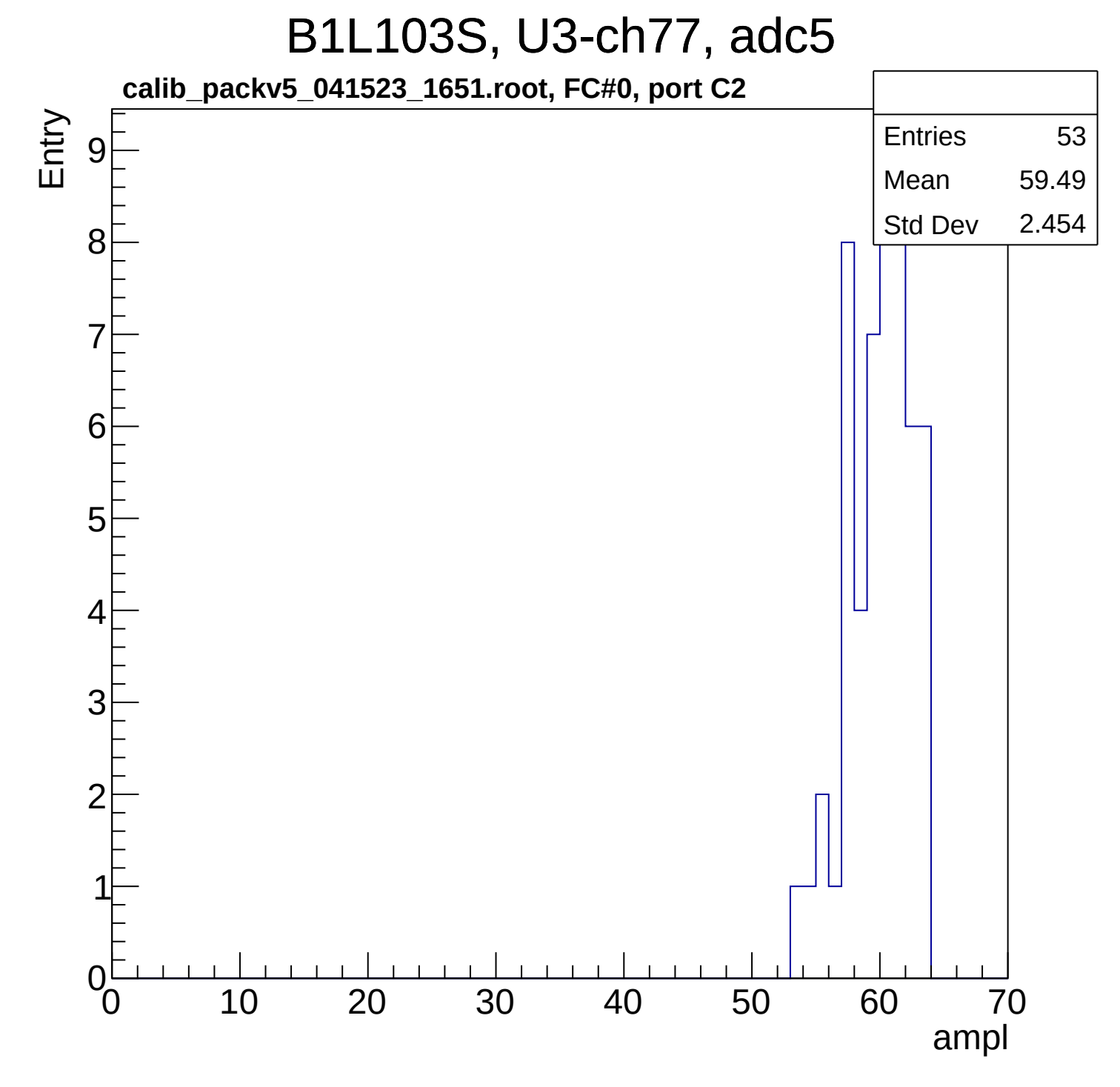
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch77, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 54
Std Dev 3.223
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch77, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 59.49
Std Dev 2.454
Entry
ampl
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2
3
4
5
6
7
8
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0
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20
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60
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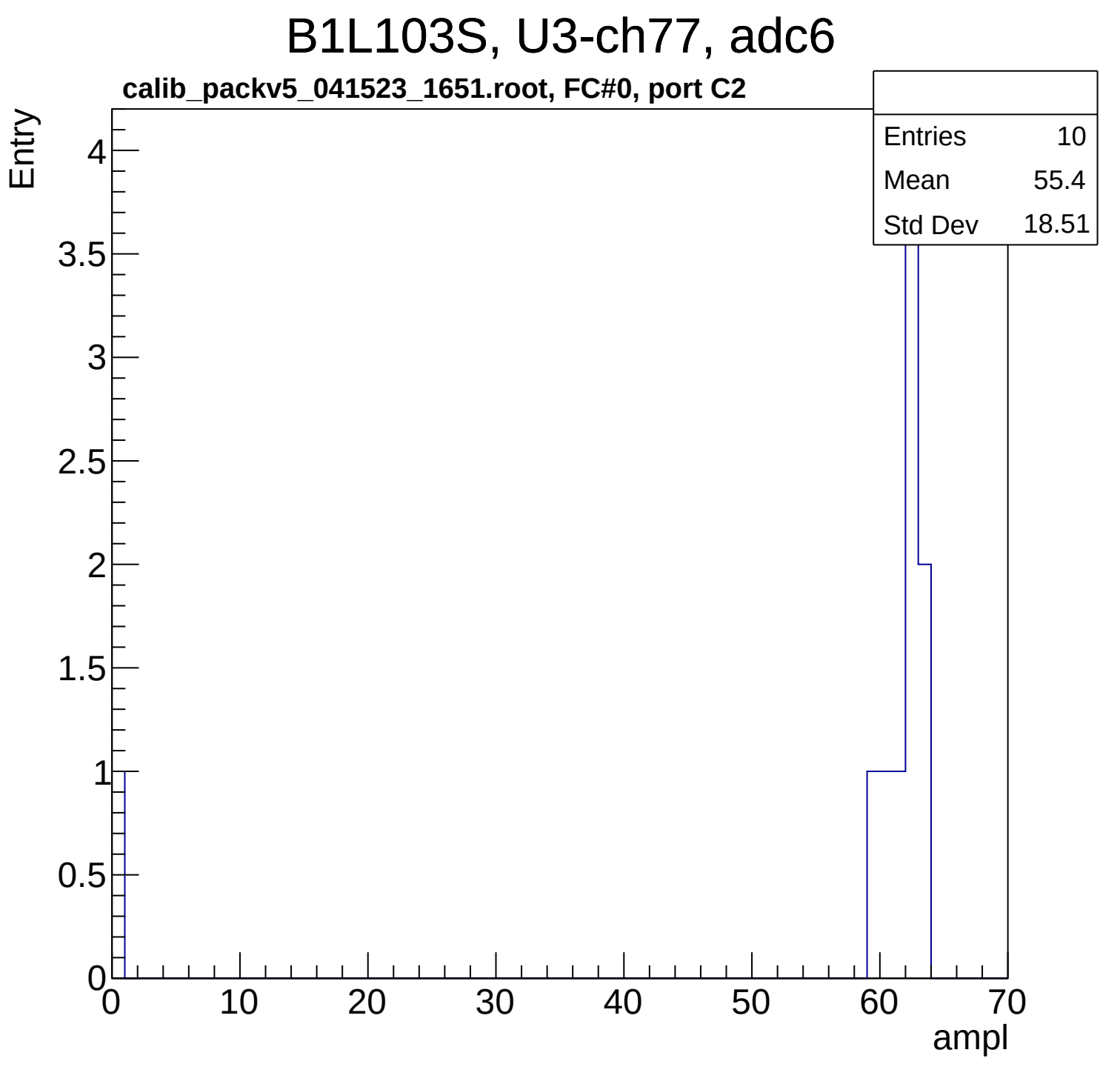
B1L103S, U3-ch77, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 55.4
Std Dev 18.51
Entry
ampl
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0.5
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1.5
2
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3
3.5
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0
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40
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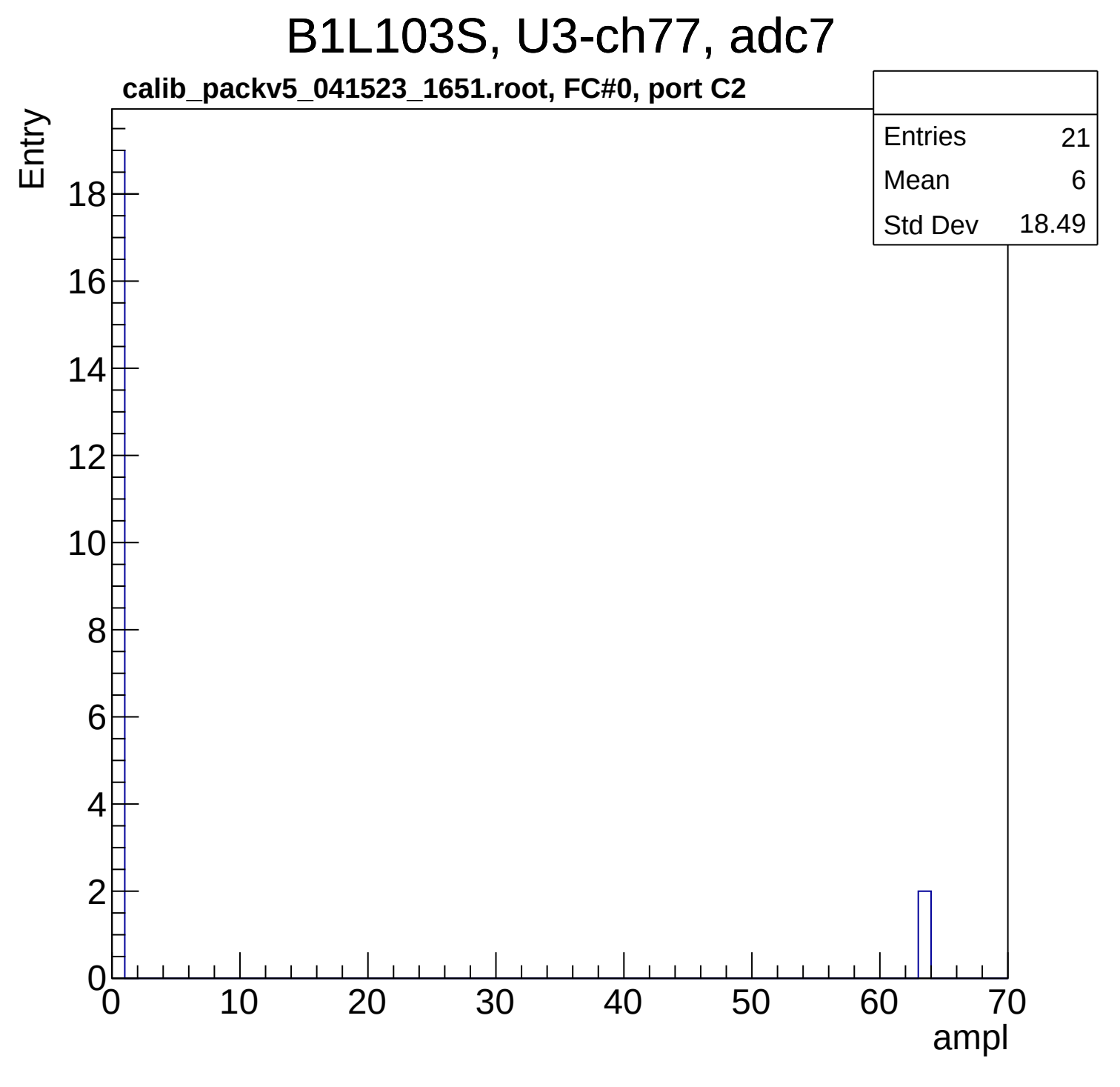
B1L103S, U3-ch77, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 6
Std Dev 18.49
Entry
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6
8
10
12
14
16
18
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10
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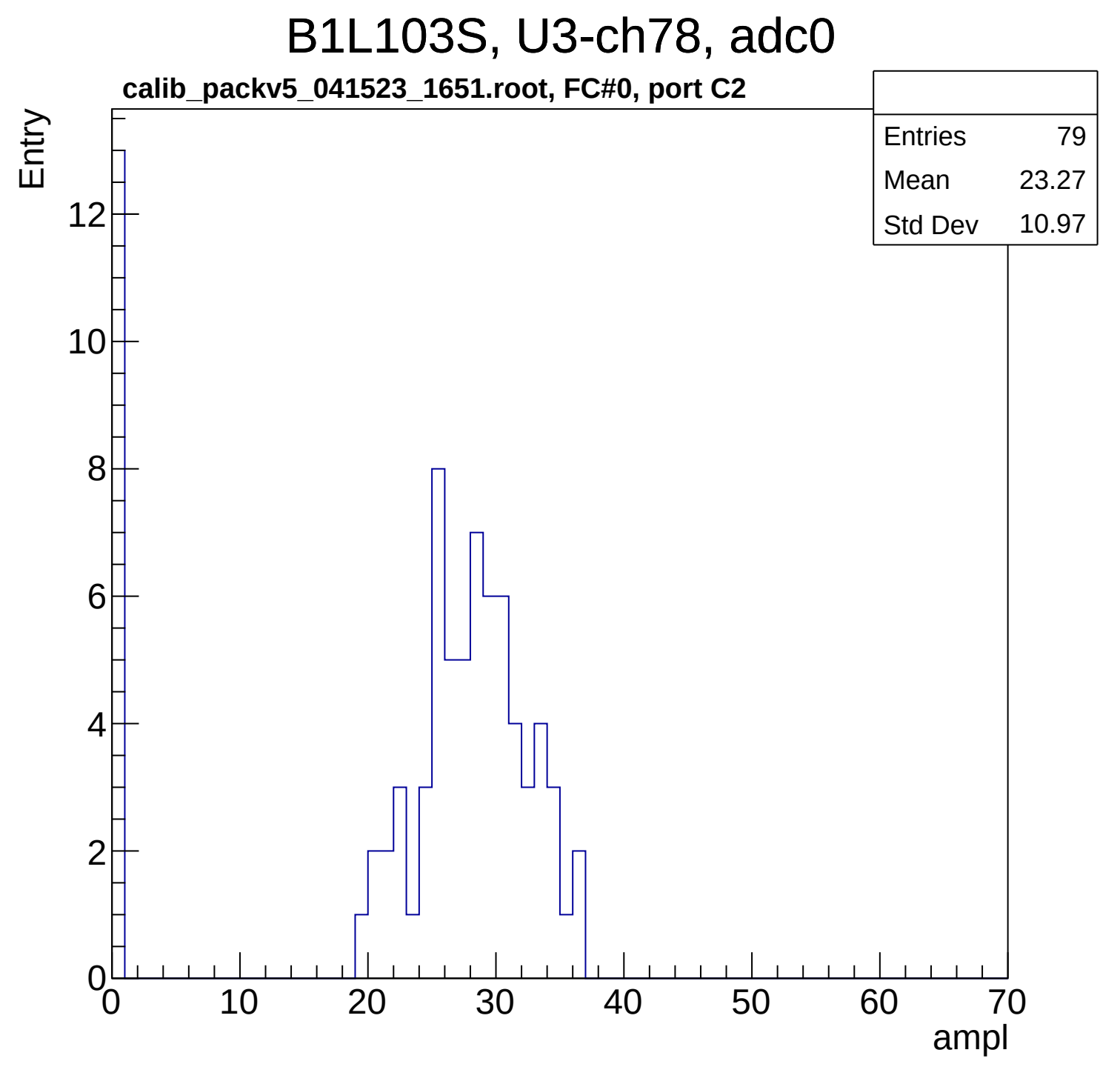
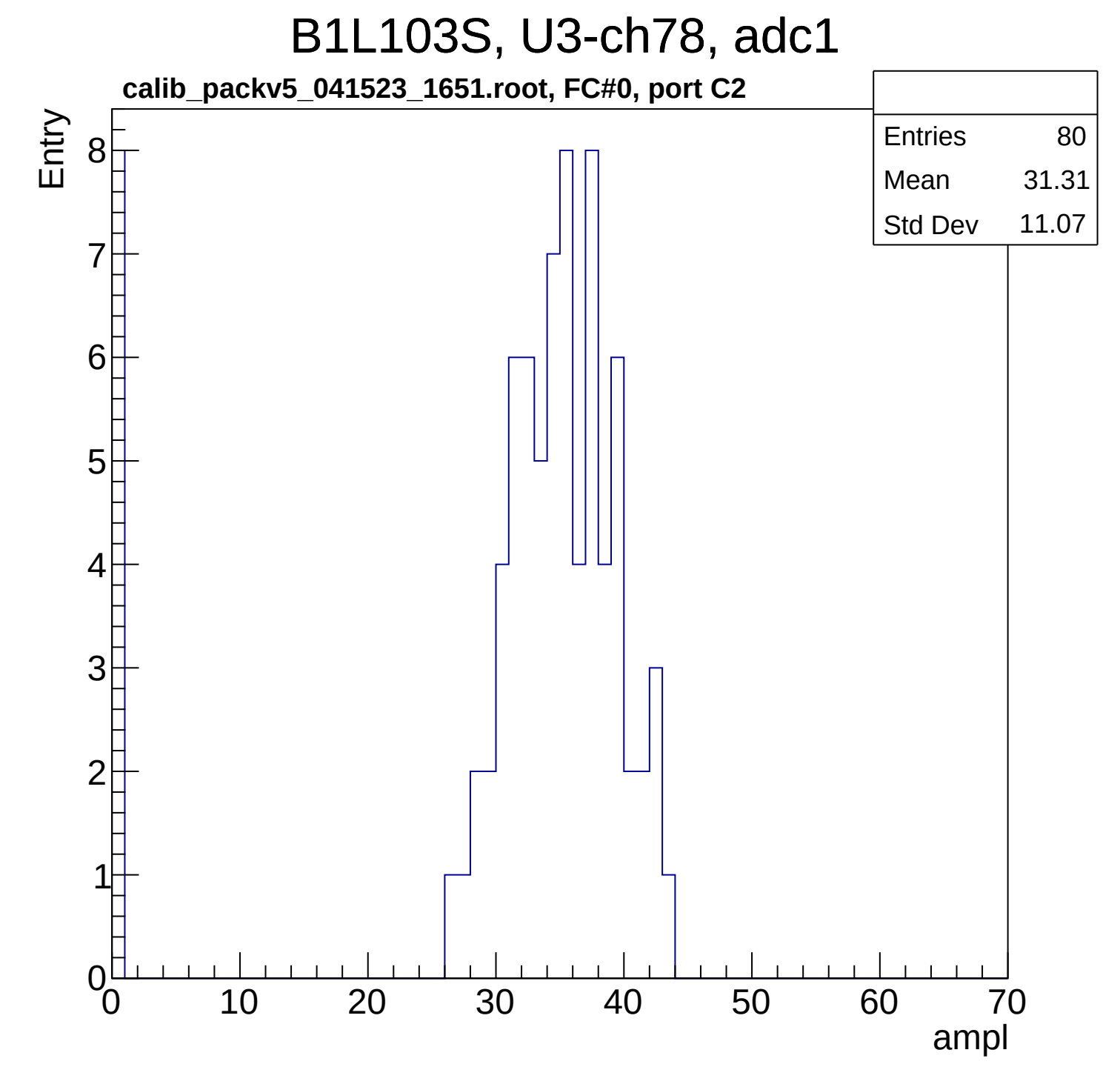
70
ampl


B1L103S, U3-ch78, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 23.27
Std Dev 10.97
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch78, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 31.31
Std Dev 11.07
Entry
ampl
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2
3
4
5
6
7
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0
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60
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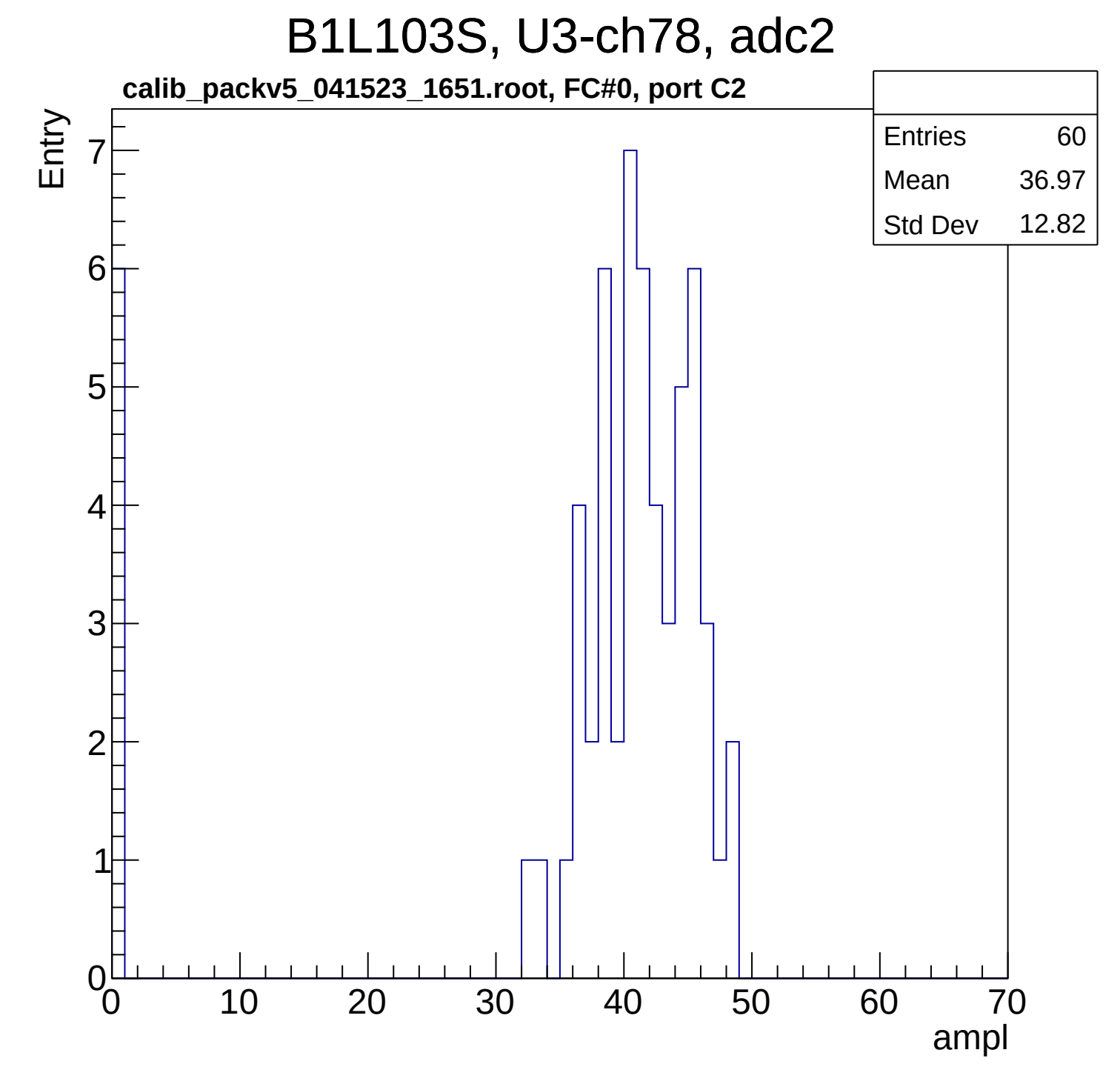
B1L103S, U3-ch78, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 36.97
Std Dev 12.82
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
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60
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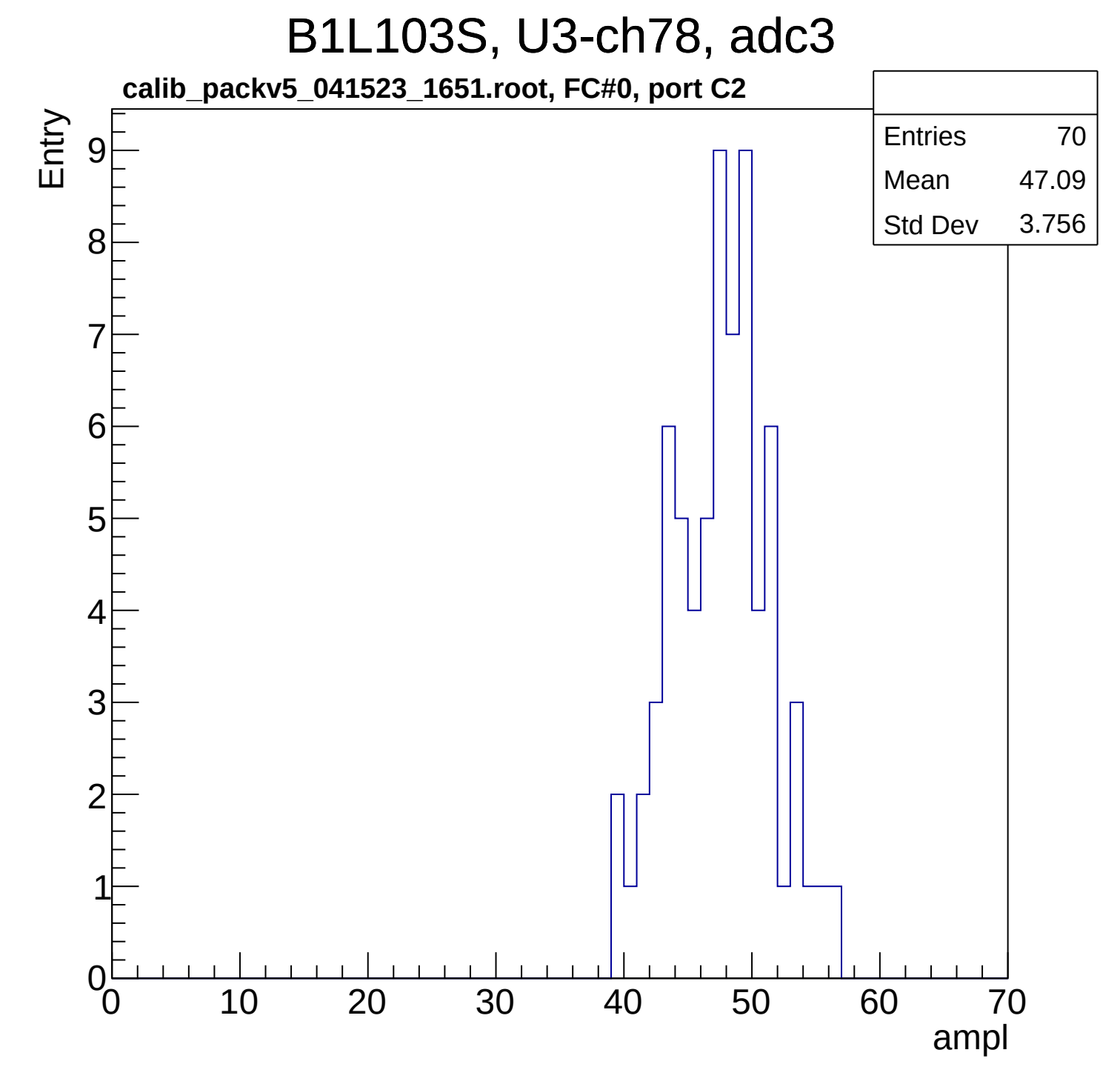
B1L103S, U3-ch78, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 47.09
Std Dev 3.756
Entry
ampl
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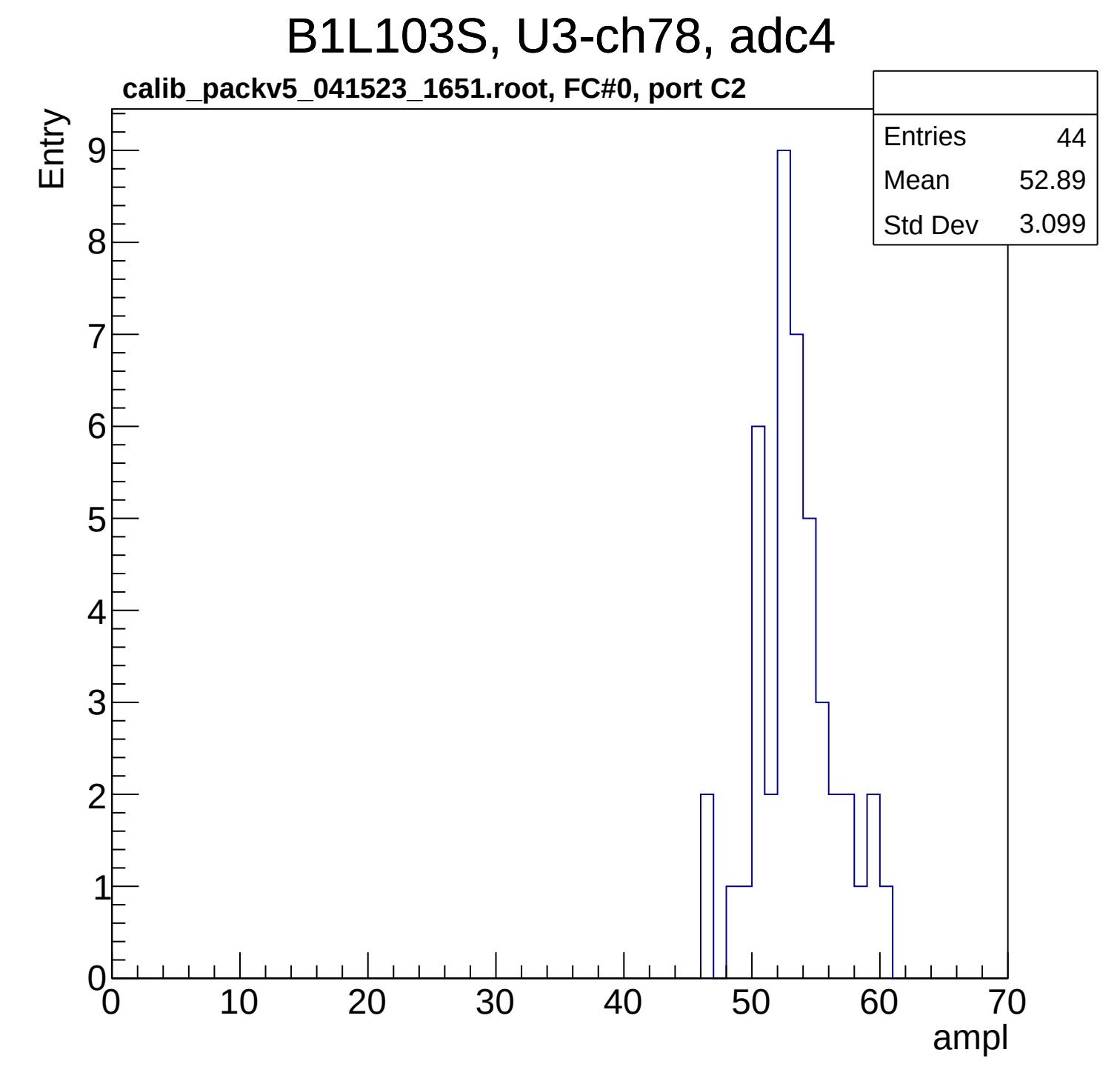
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch78, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 52.89
Std Dev 3.099
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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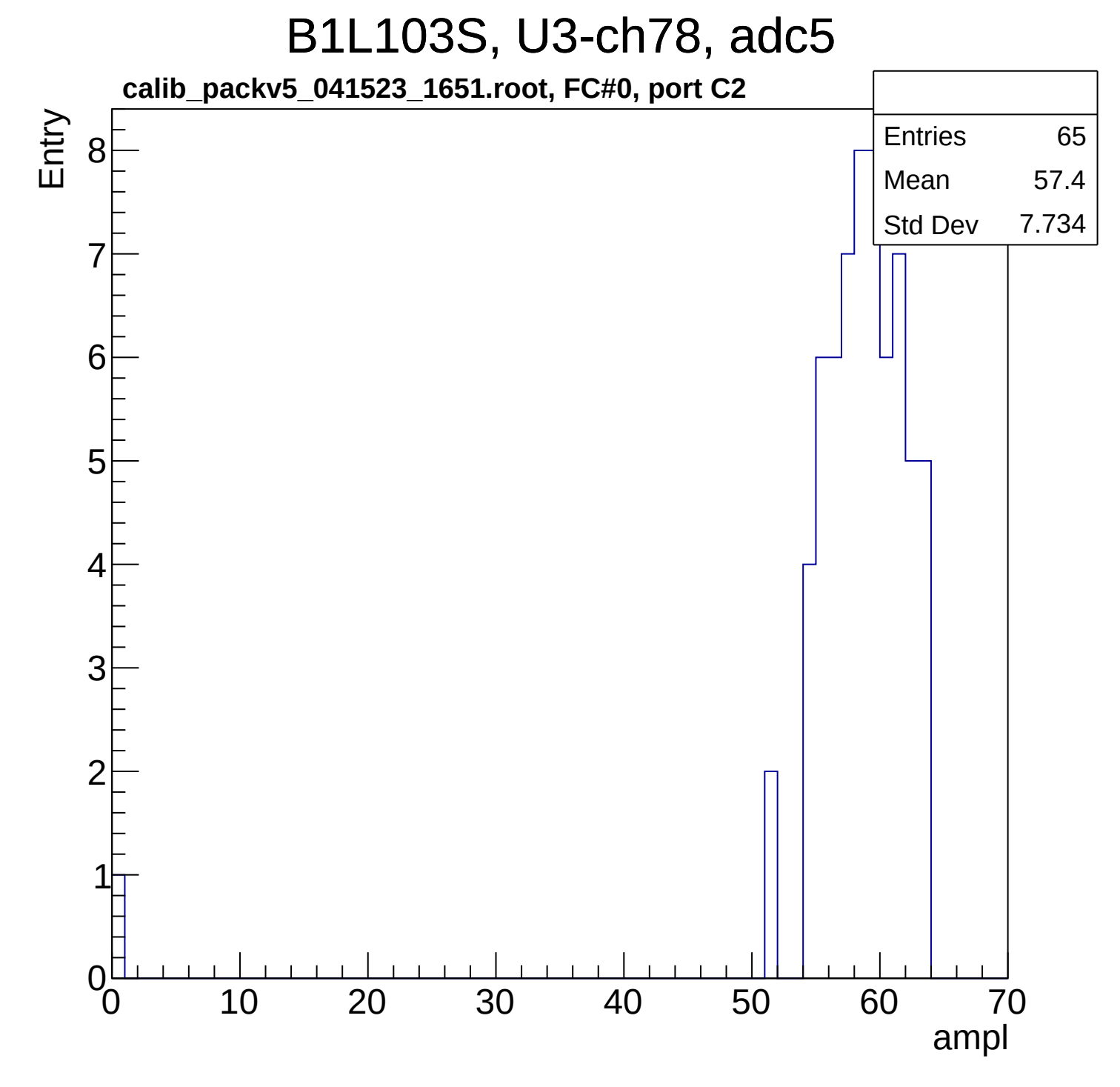
B1L103S, U3-ch78, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 57.4
Std Dev 7.734
Entry
ampl
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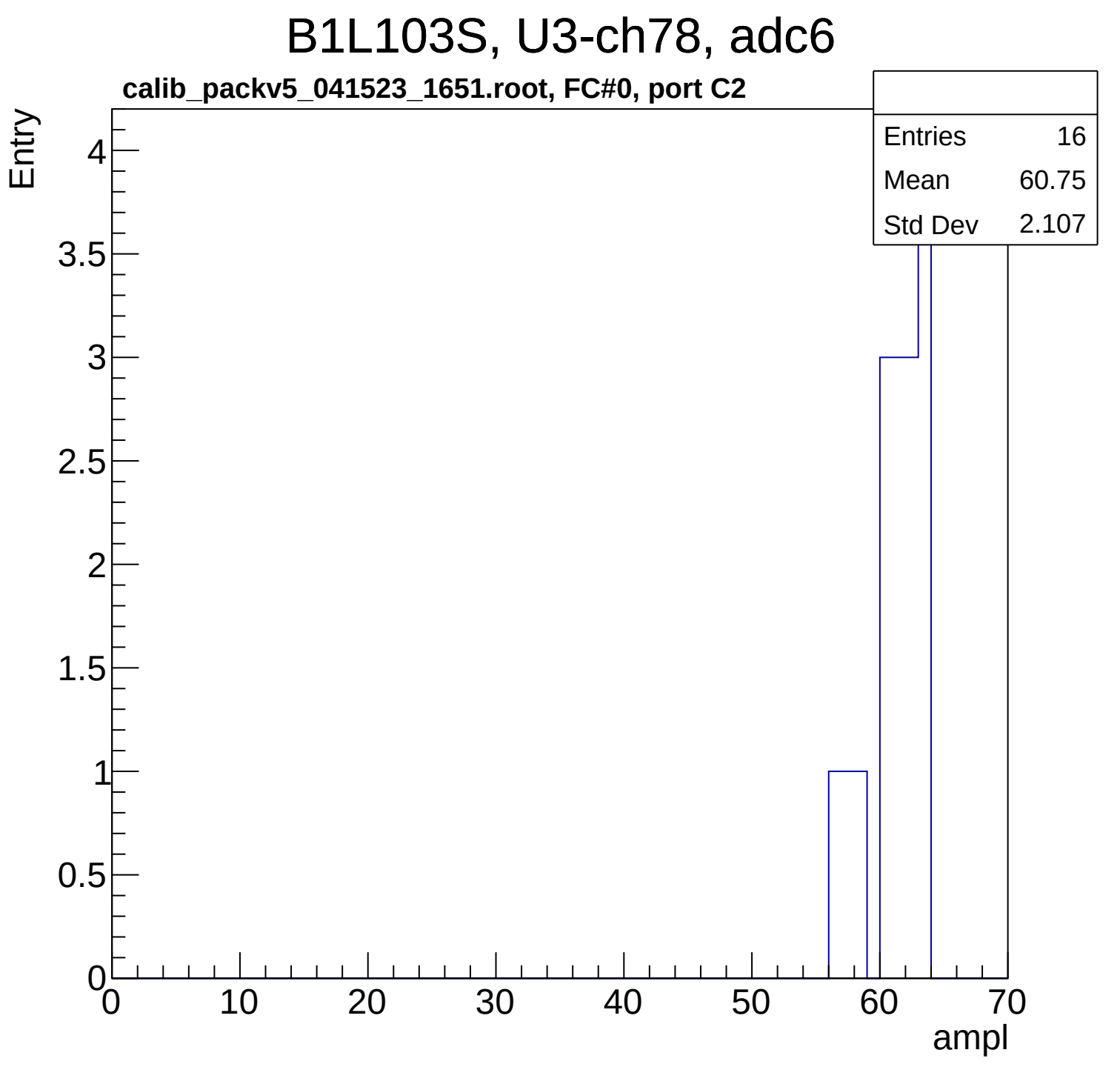
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch78, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 60.75
Std Dev 2.107
Entry
ampl
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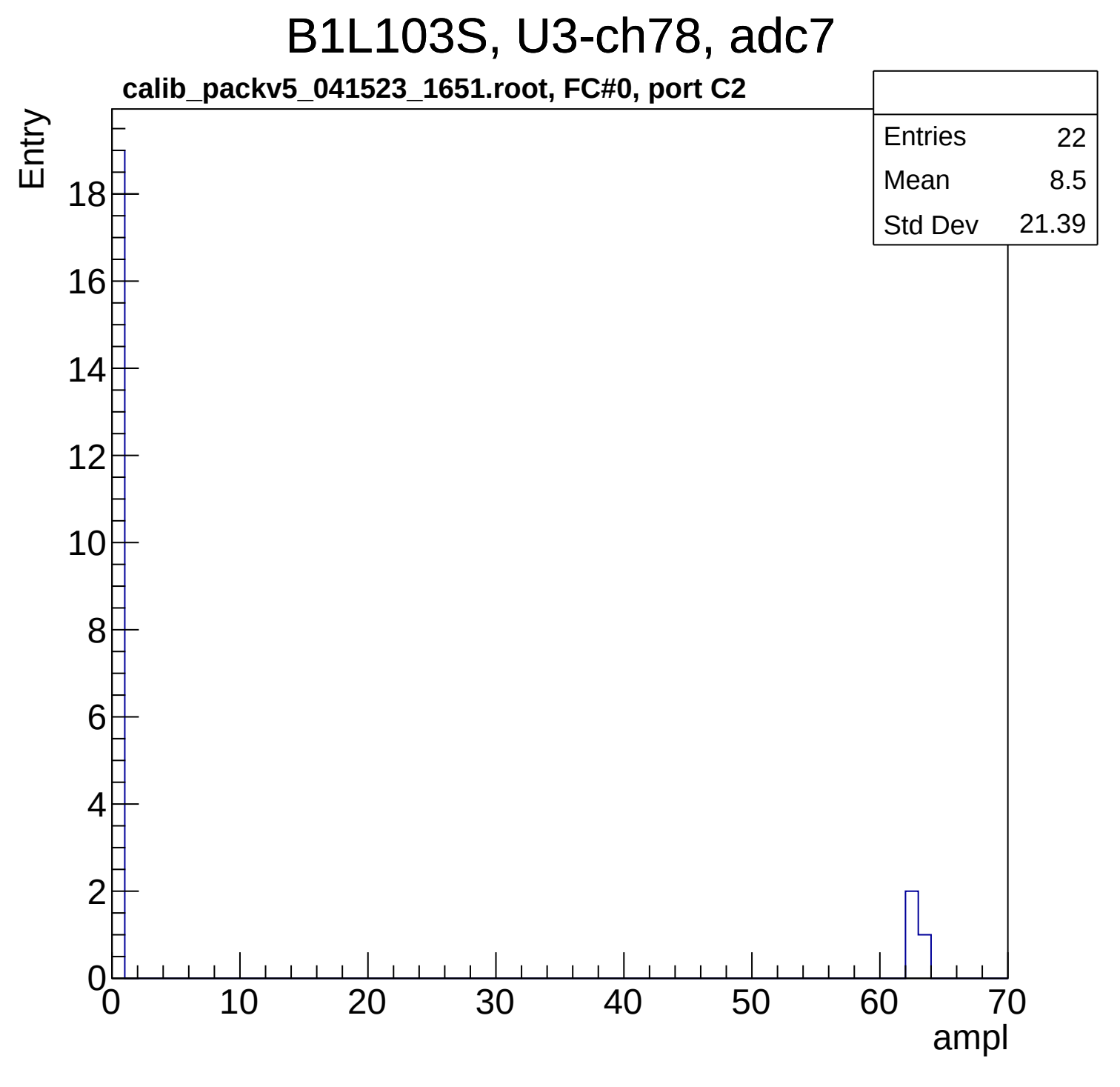
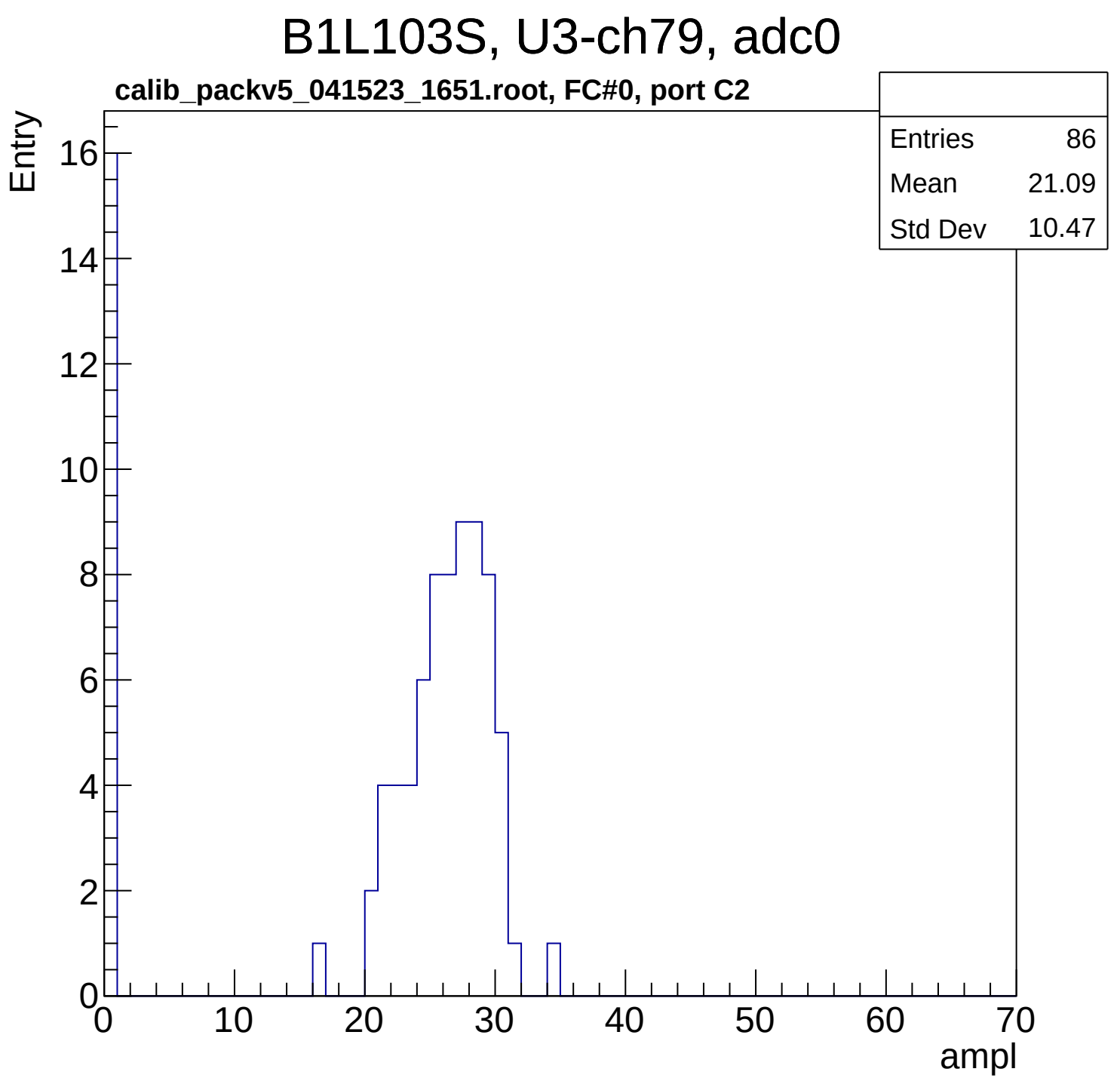
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U3-ch78, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.5
Std Dev 21.39
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch79, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 21.09
Std Dev 10.47
Entry
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4
6
8
10
12
14
16
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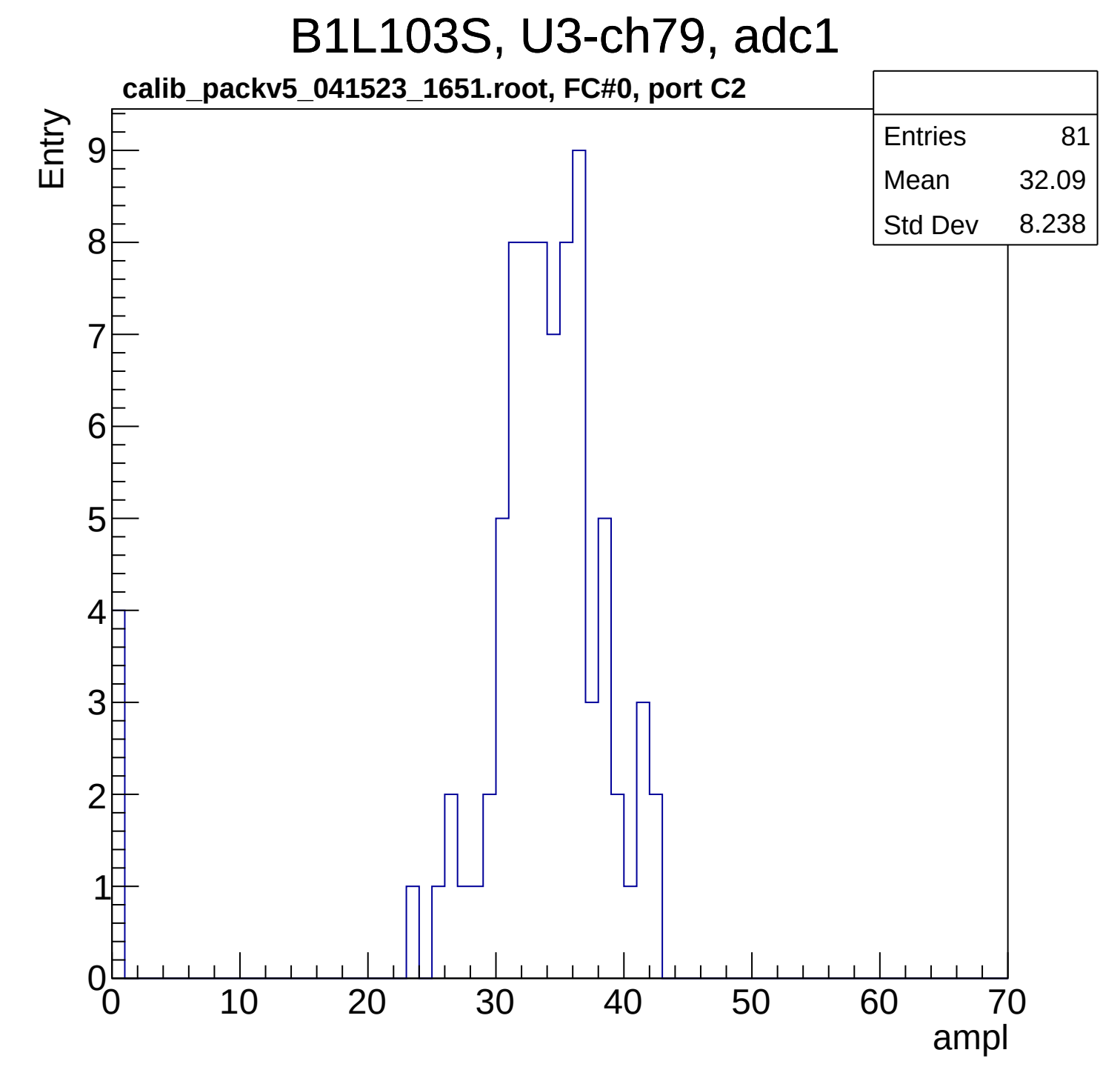
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch79, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 32.09
Std Dev 8.238
Entry
ampl
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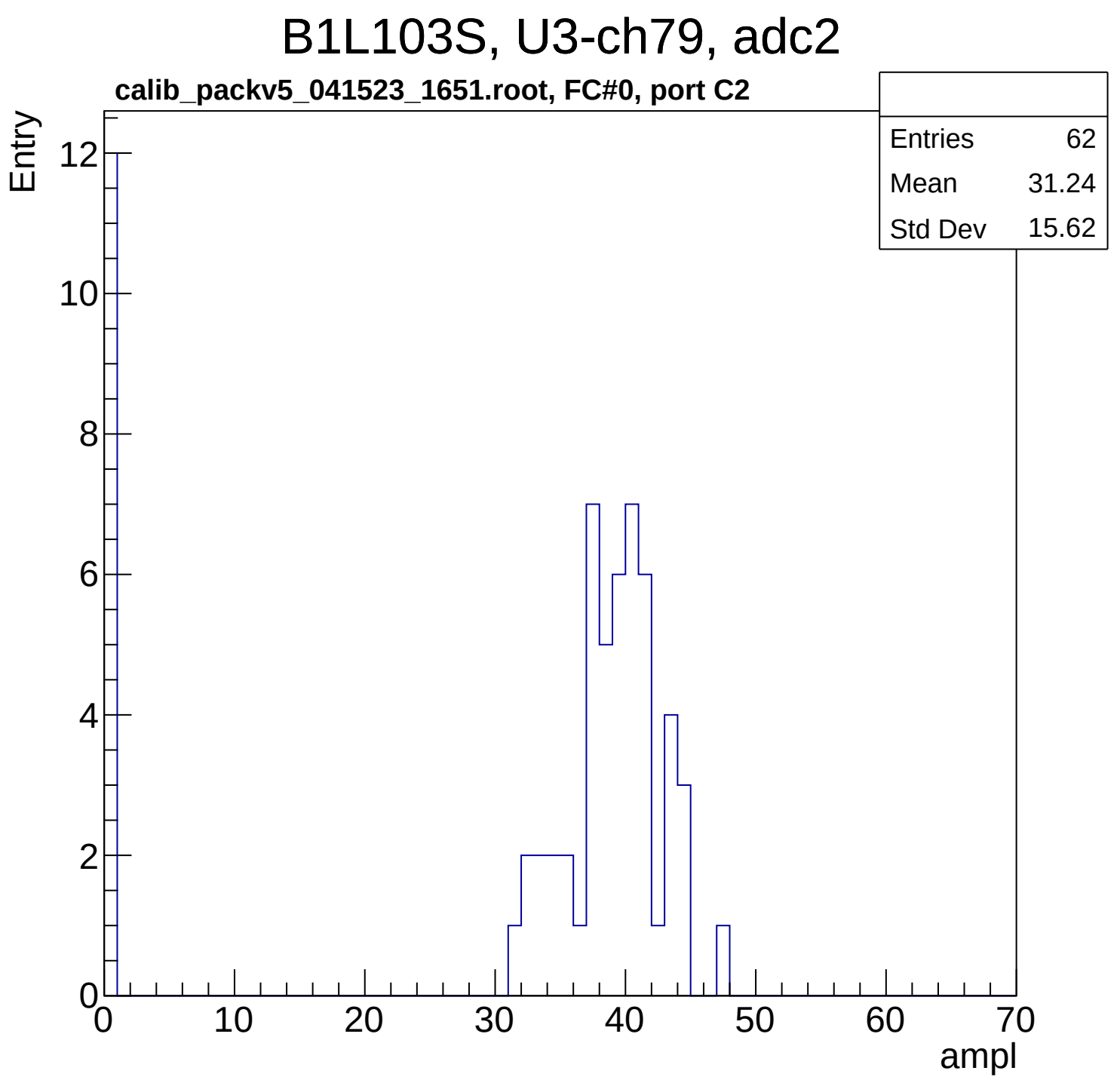
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch79, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 31.24
Std Dev 15.62
Entry
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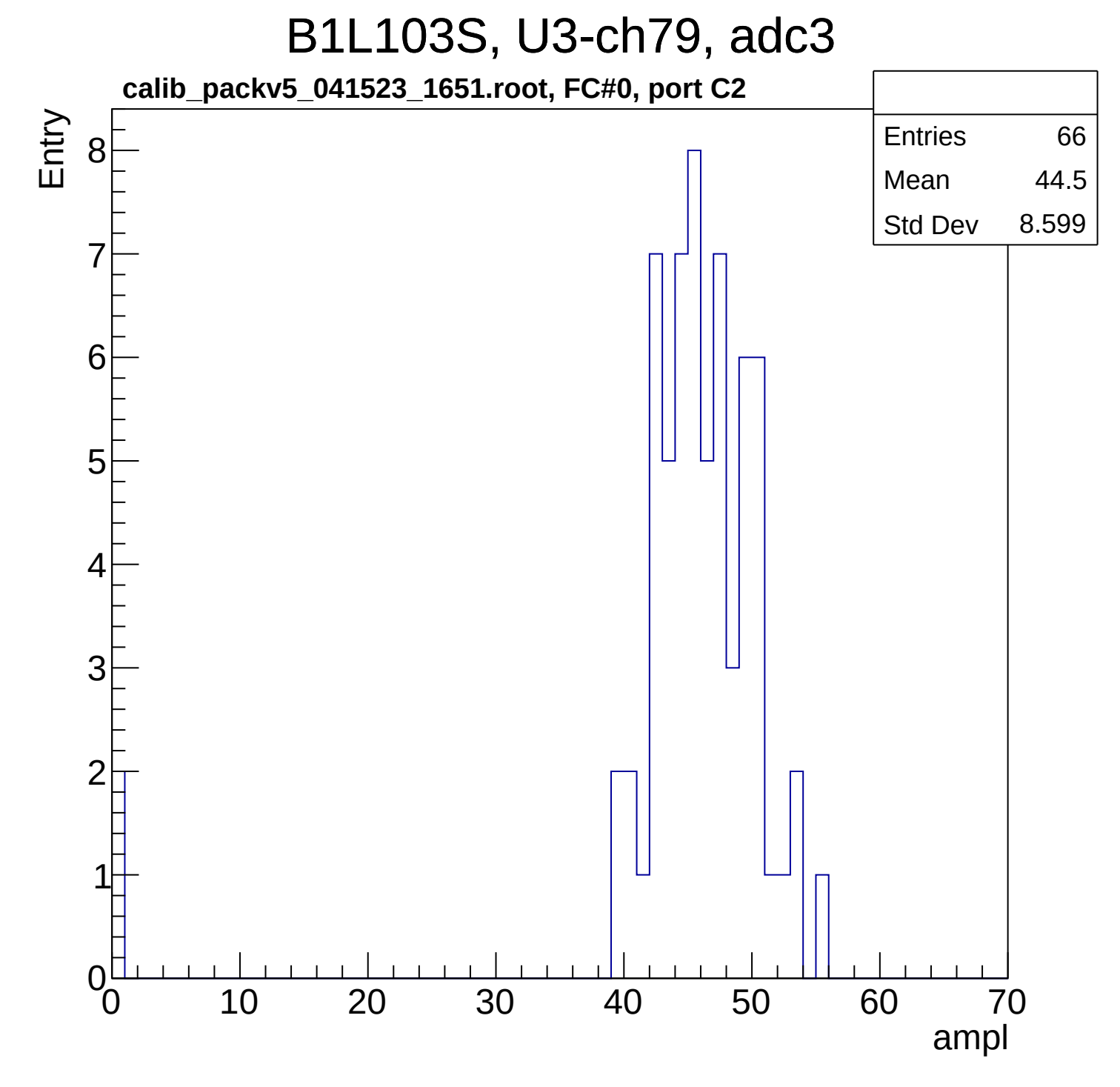
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch79, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 44.5
Std Dev 8.599
Entry
ampl
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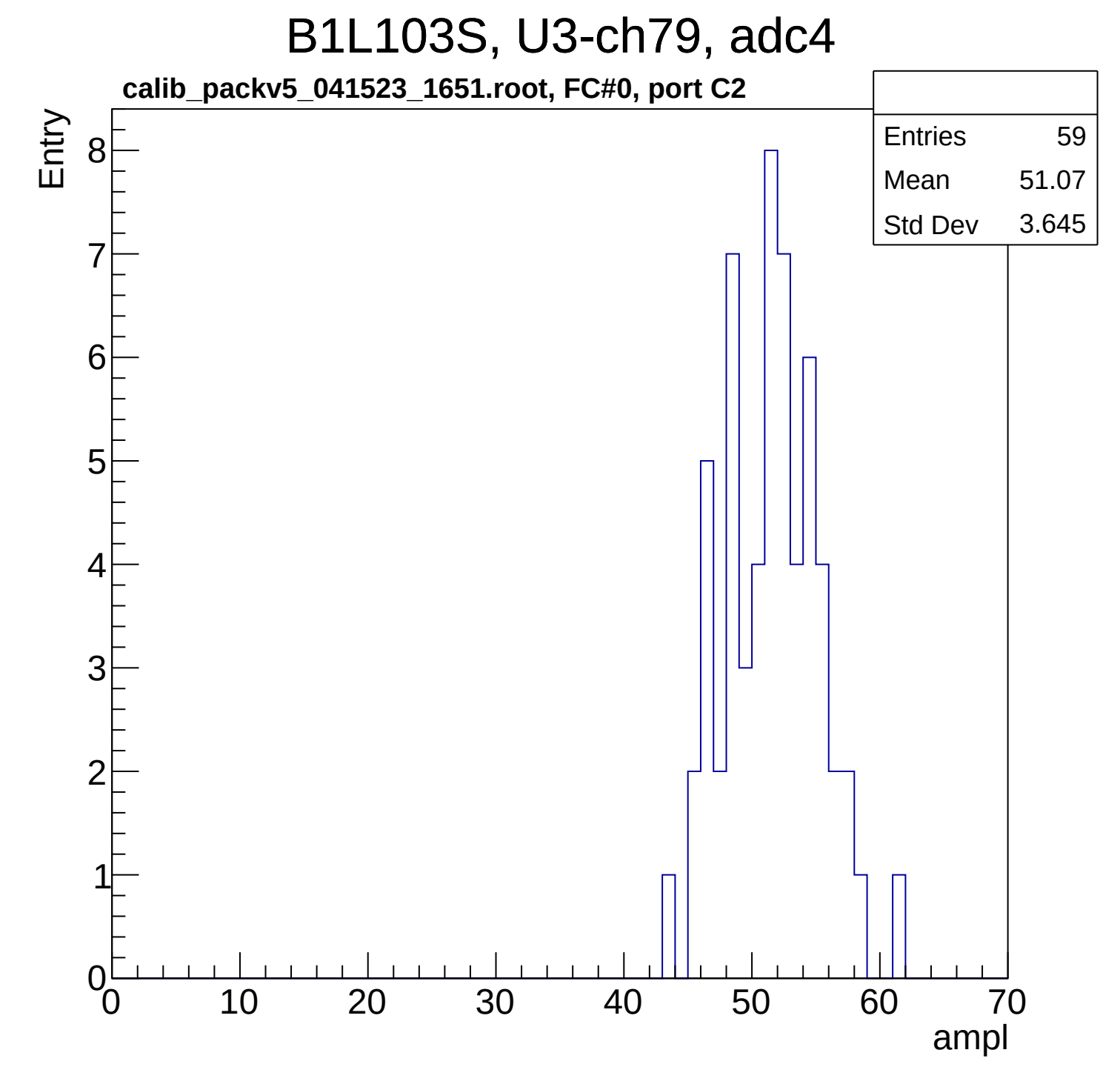
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch79, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 51.07
Std Dev 3.645
Entry
ampl
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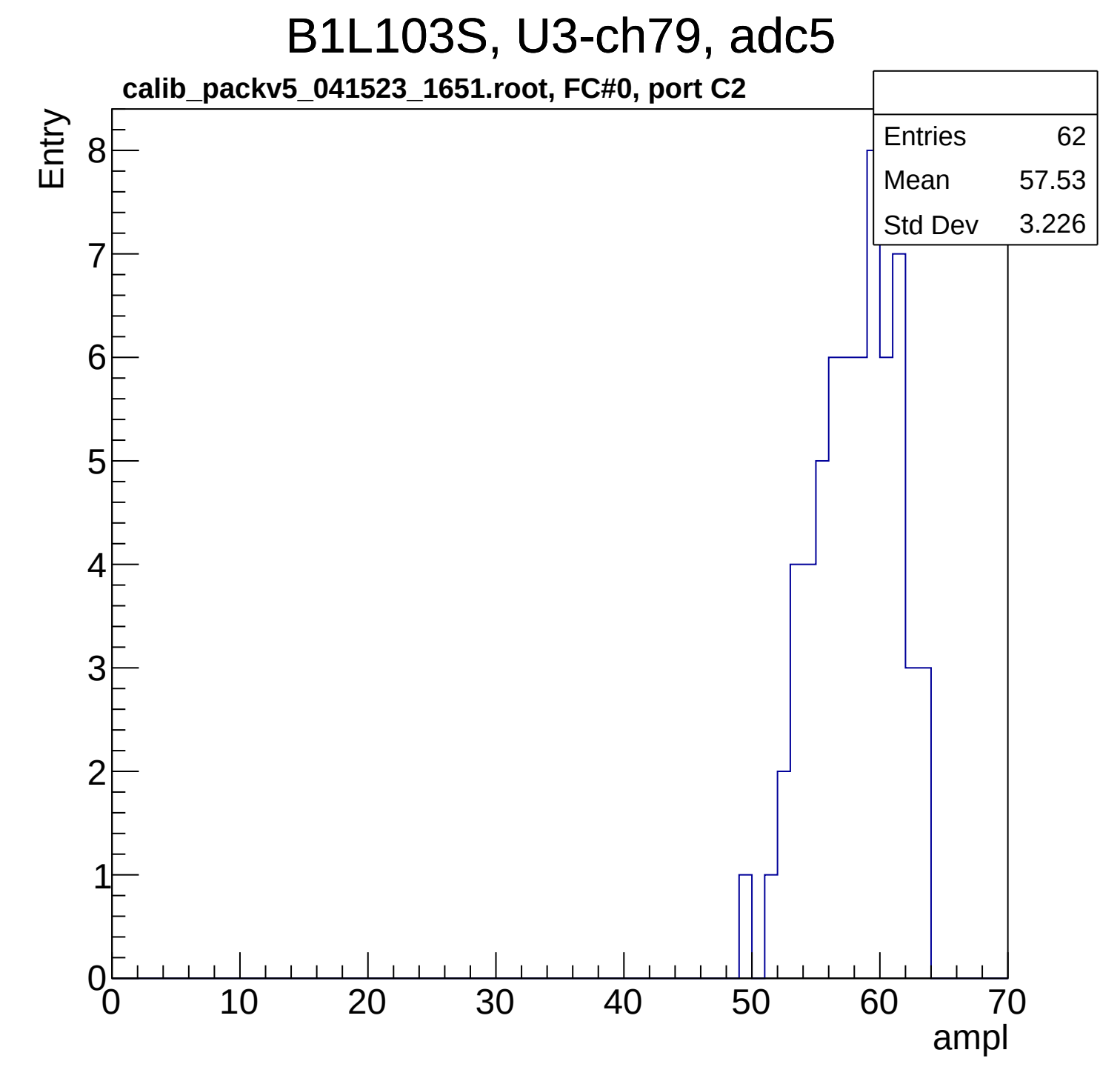
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch79, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 57.53
Std Dev 3.226
Entry
ampl
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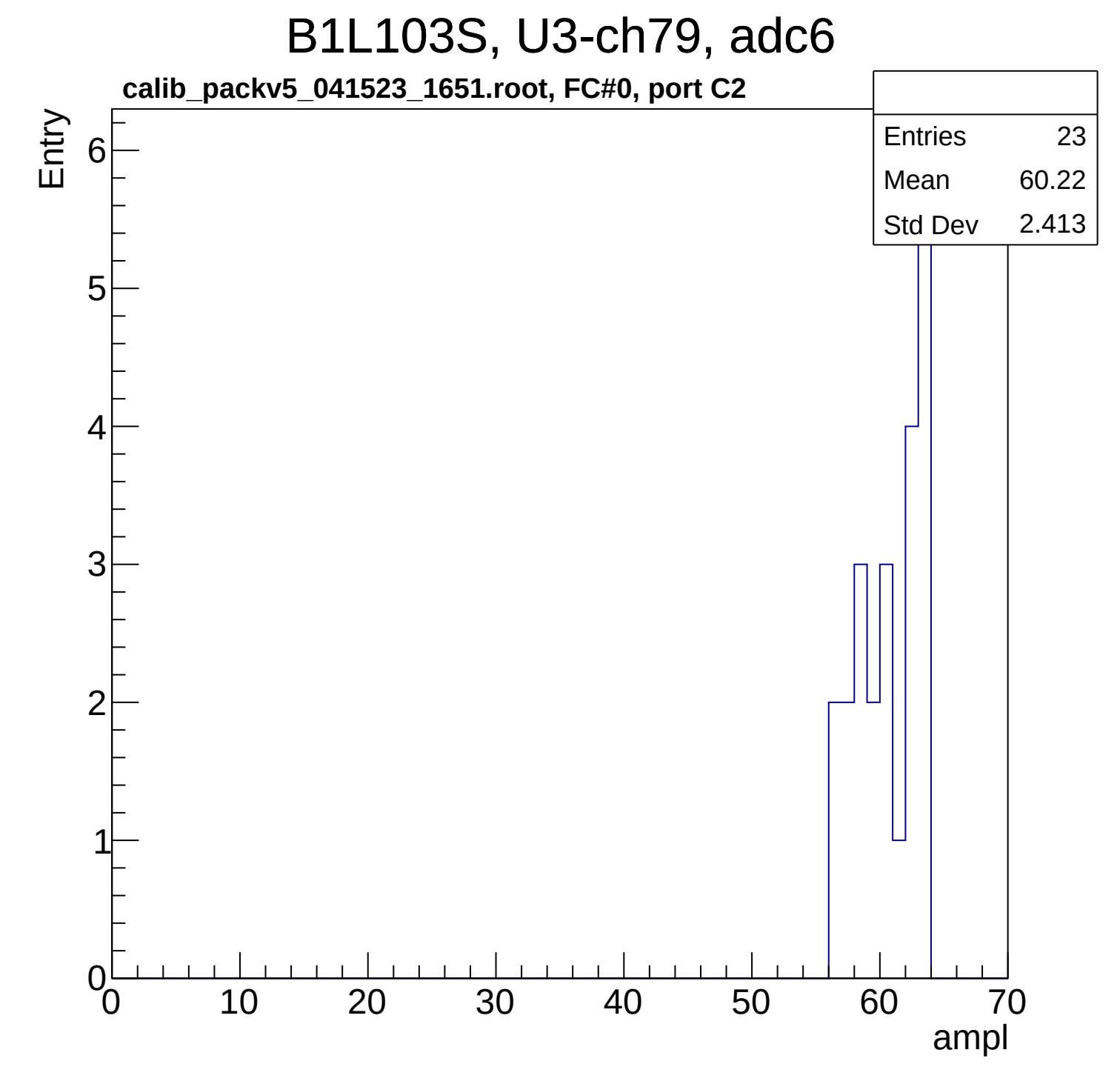
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch79, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 60.22
Std Dev 2.413
Entry
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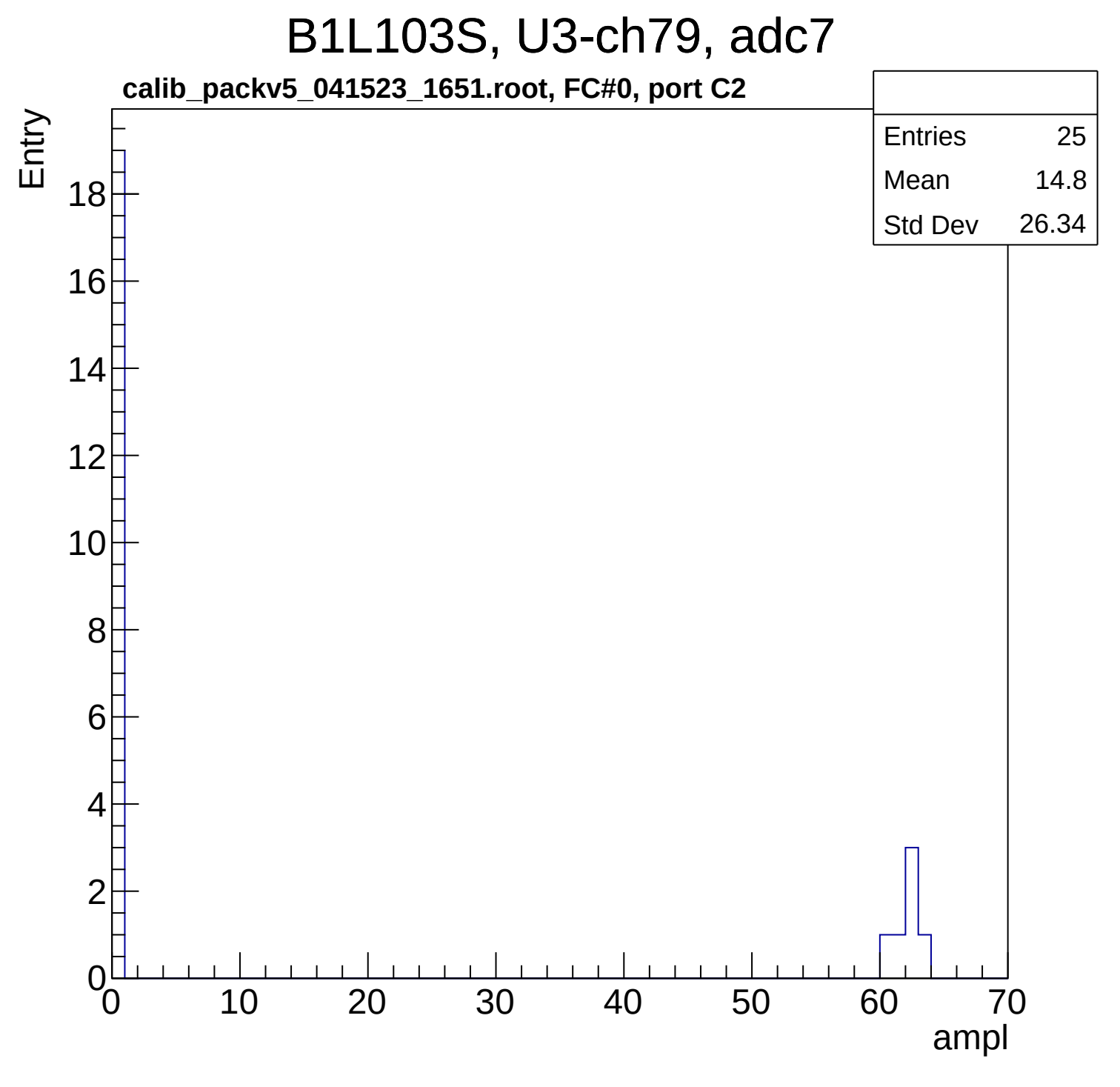
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch79, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 14.8
Std Dev 26.34
Entry
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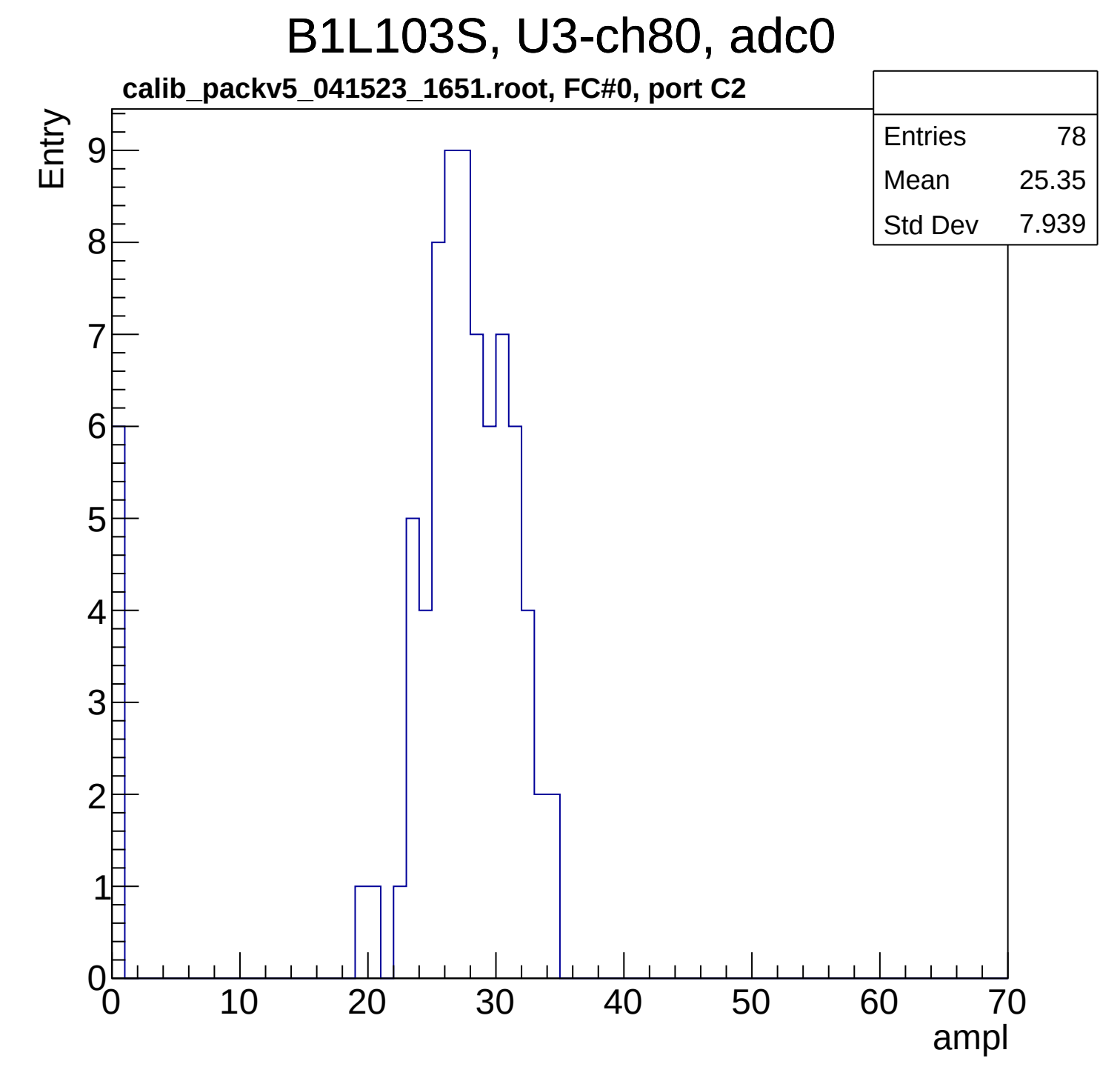
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch80, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 25.35
Std Dev 7.939
Entry
ampl
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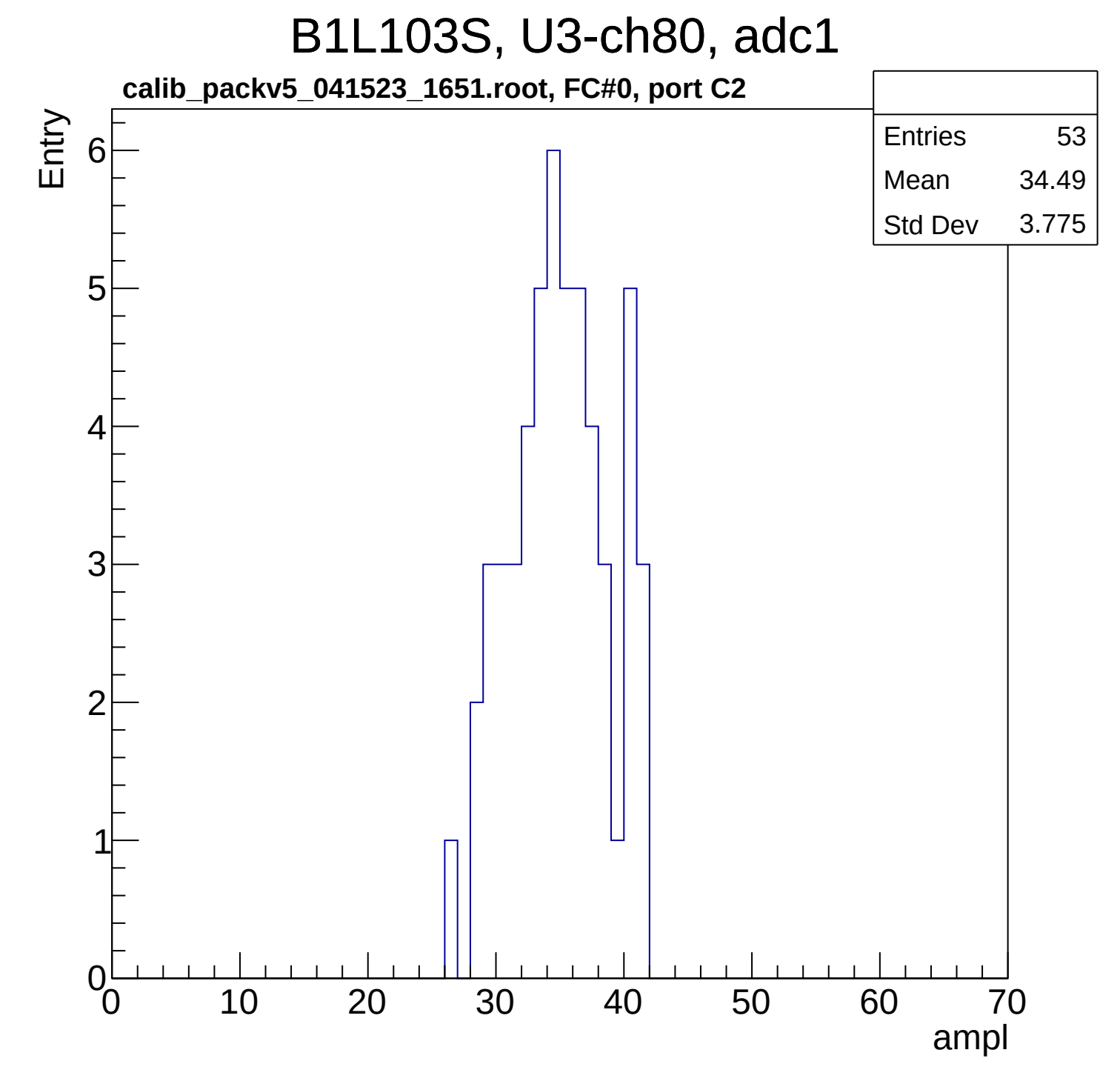
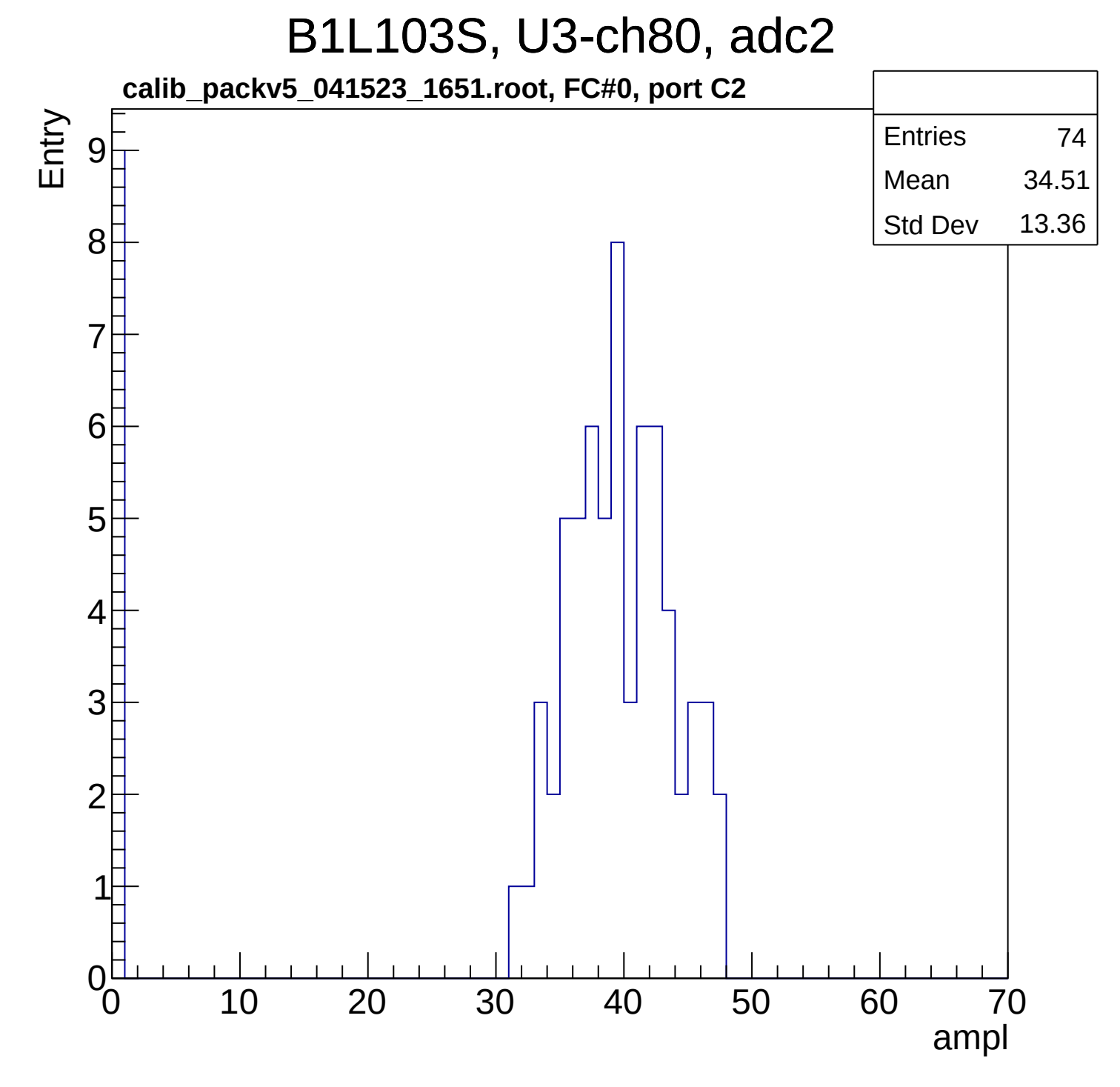
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch80, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 34.49
Std Dev 3.775
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U3-ch80, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 34.51
Std Dev 13.36
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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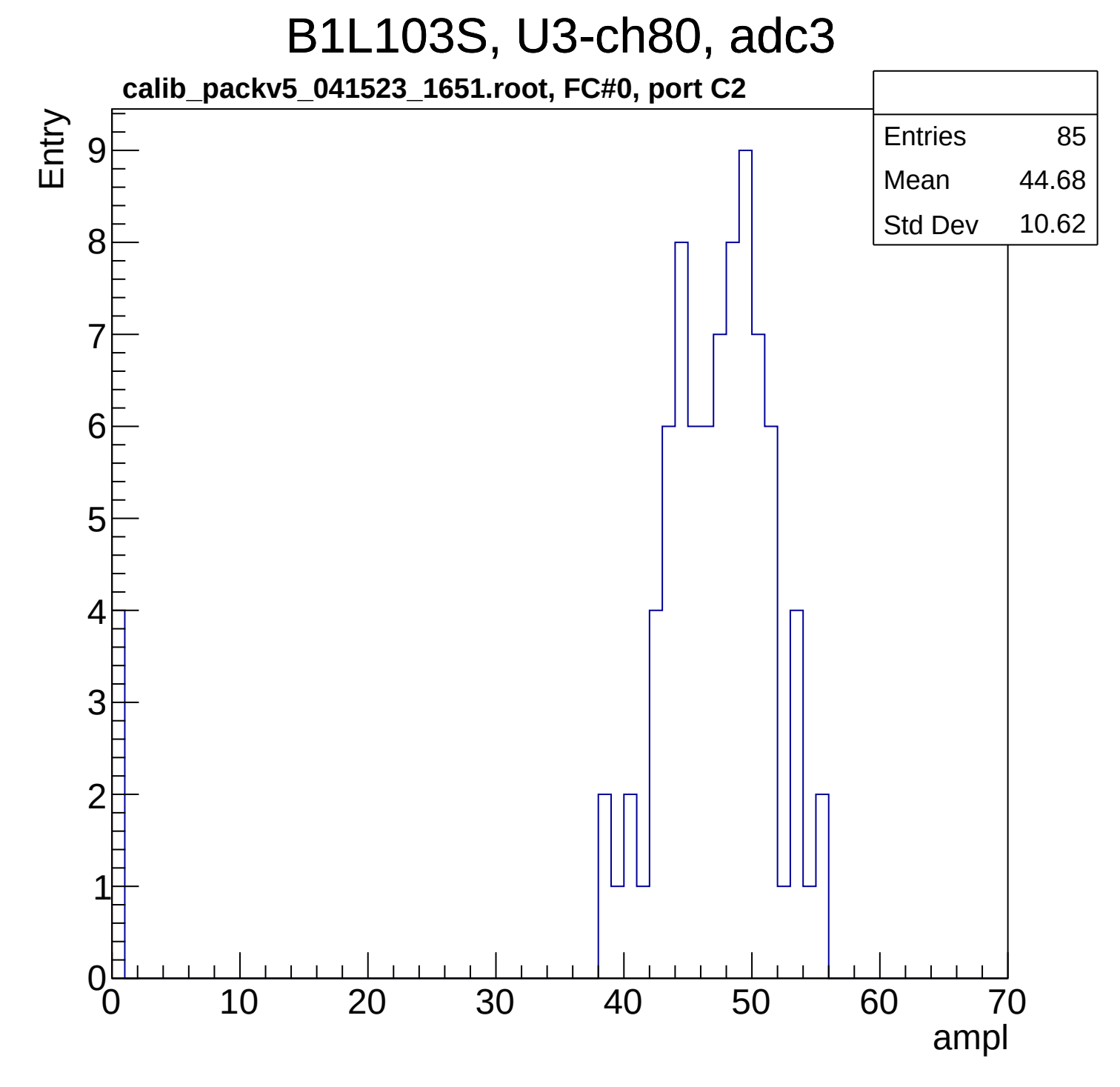
40
50
60
70


B1L103S, U3-ch80, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 44.68
Std Dev 10.62
Entry
ampl
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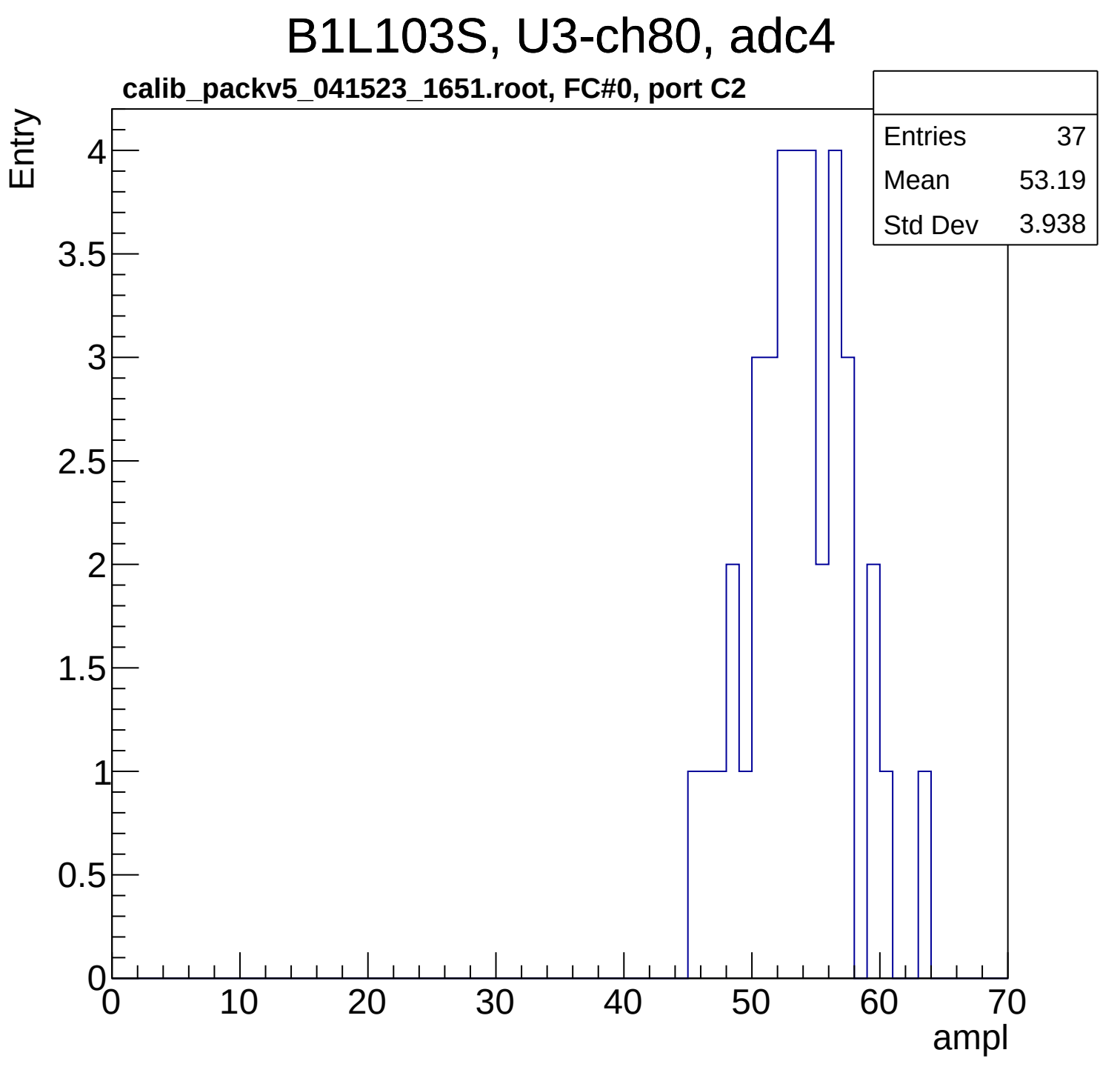
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch80, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 53.19
Std Dev 3.938
Entry
ampl
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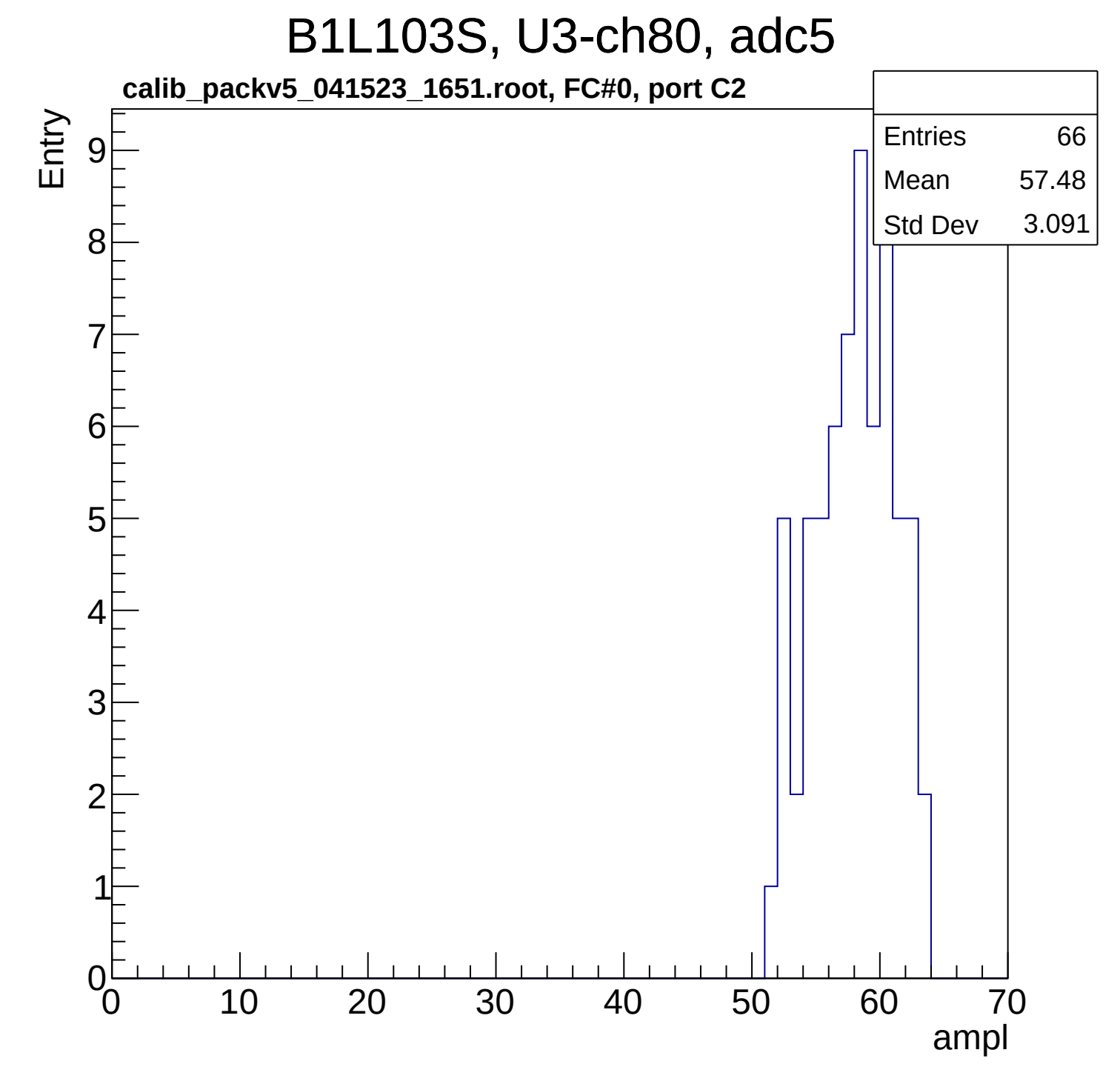
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U3-ch80, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 57.48
Std Dev 3.091
Entry
ampl
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2
3
4
5
6
7
8
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0
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40
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60
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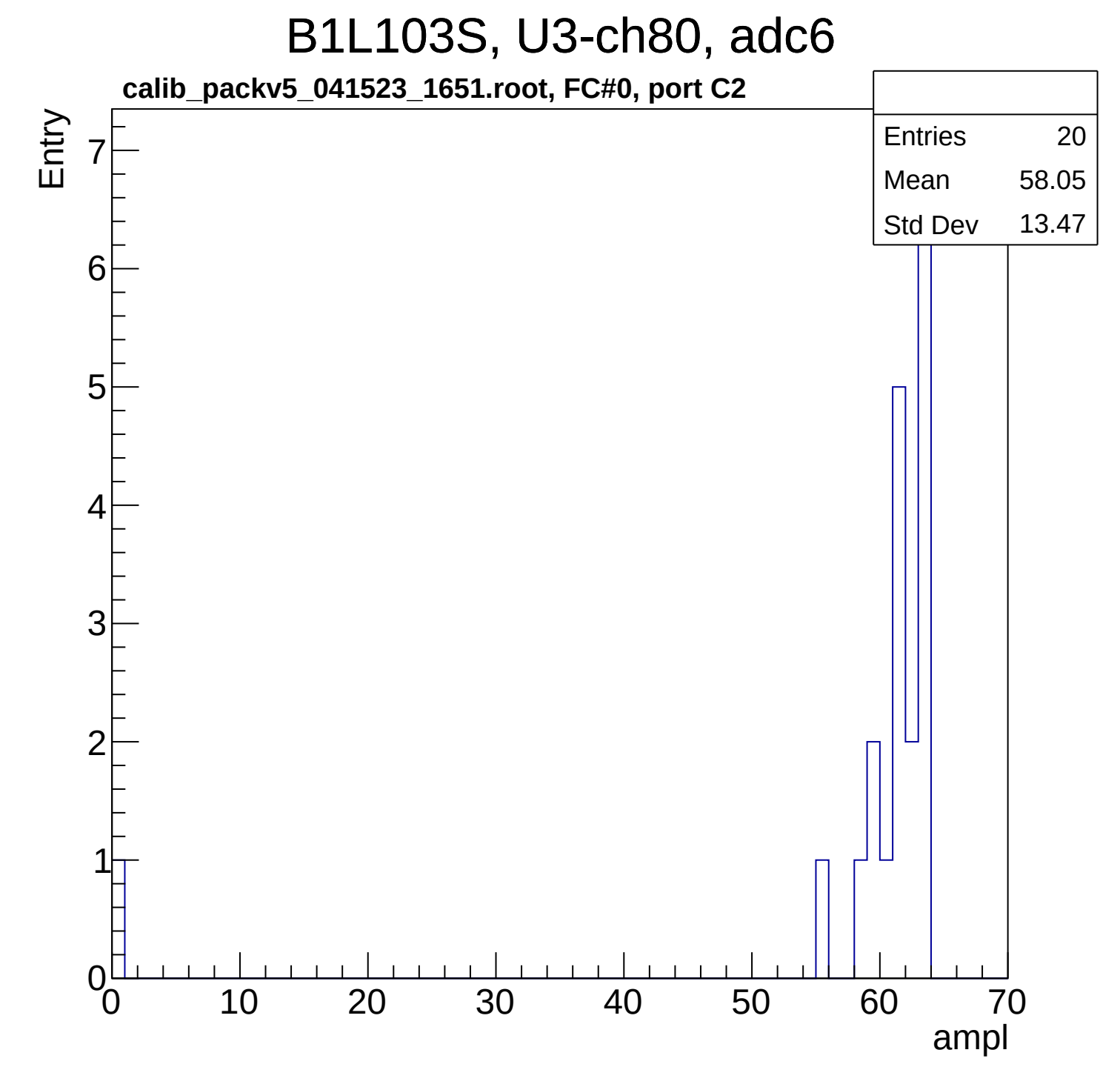
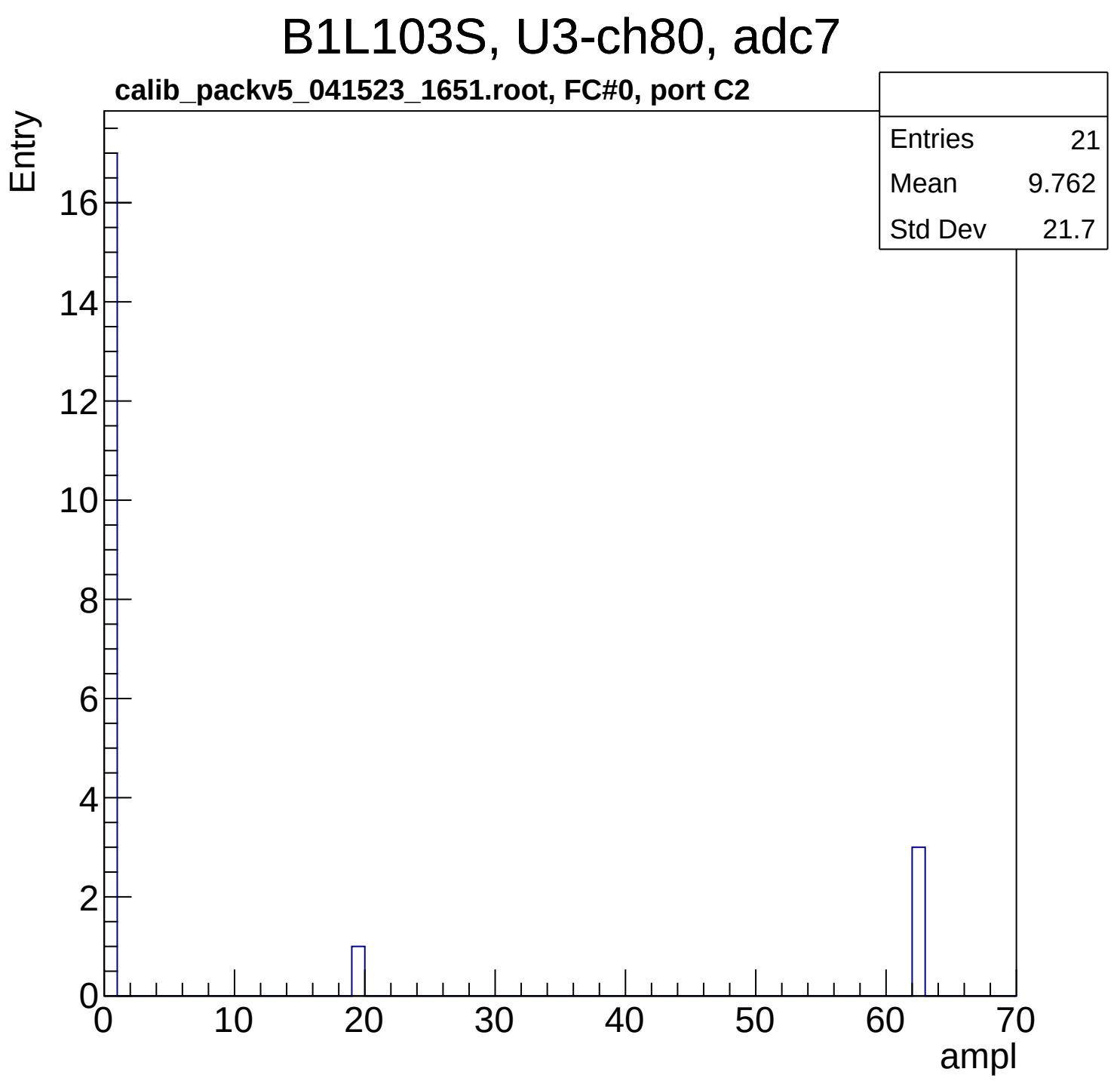

B1L103S, U3-ch80, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 58.05
Std Dev 13.47
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch80, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 9.762
Std Dev 21.7
Entry
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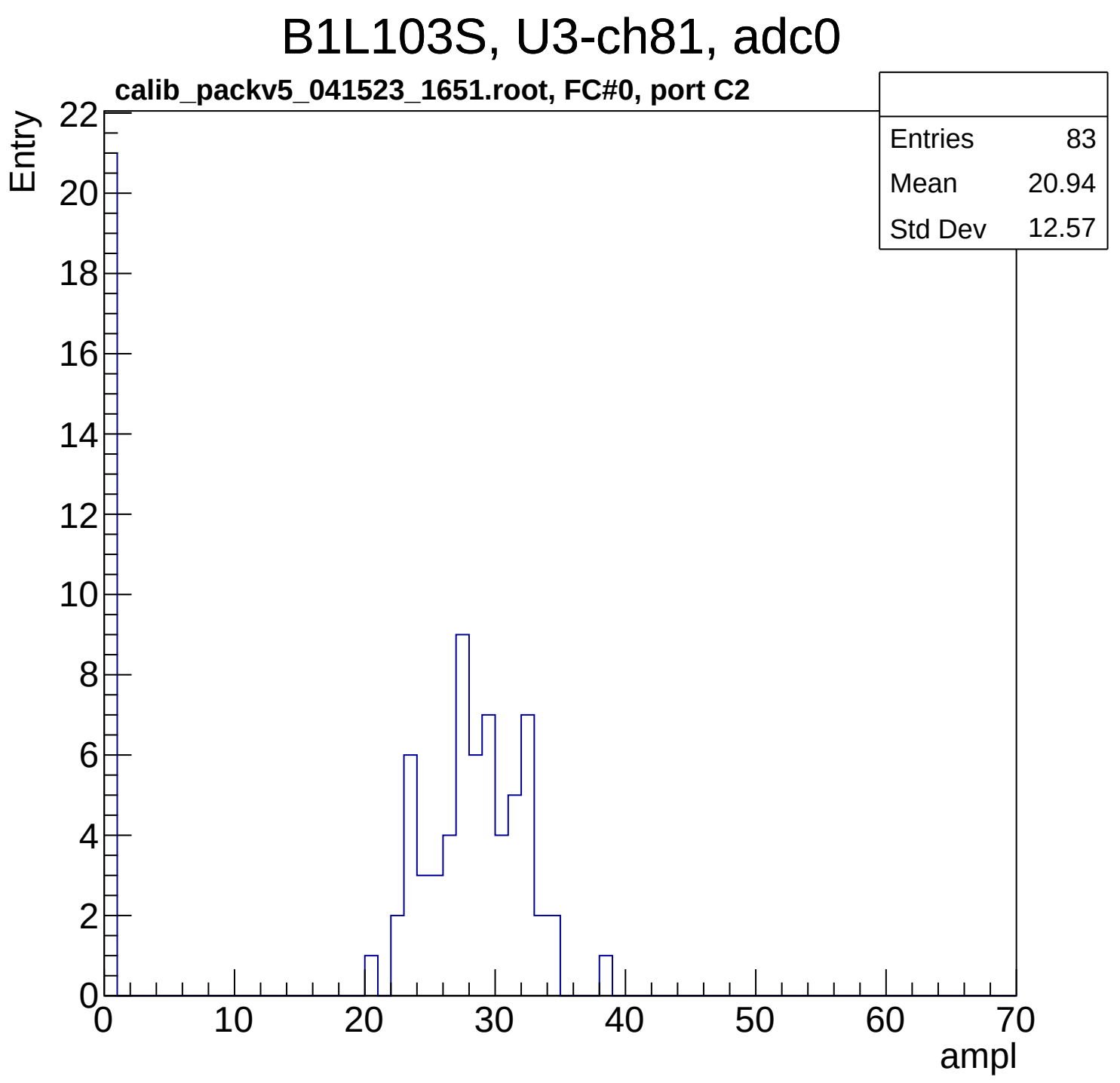
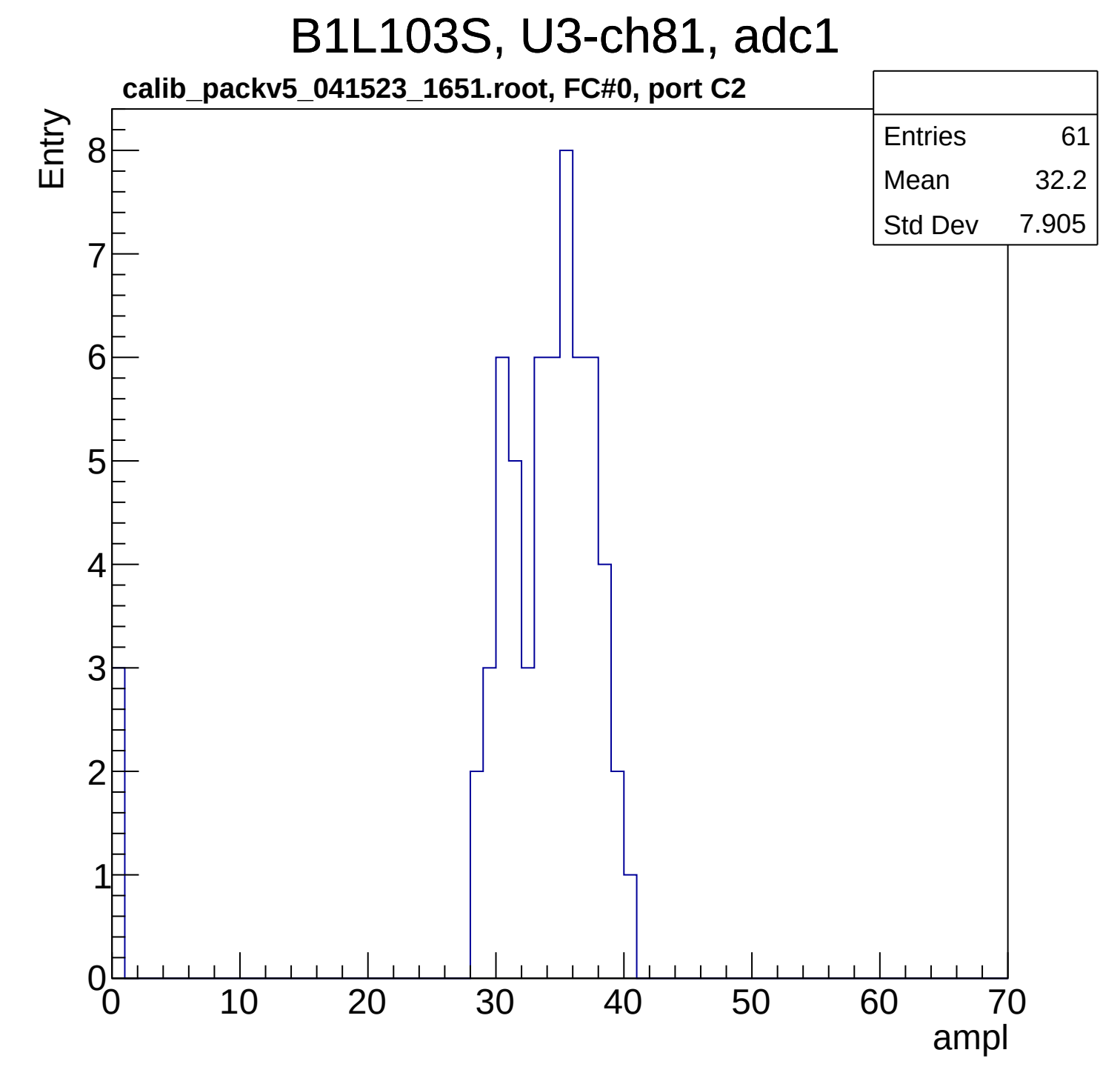
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch81, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 20.94
Std Dev 12.57
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70


B1L103S, U3-ch81, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 32.2
Std Dev 7.905
Entry
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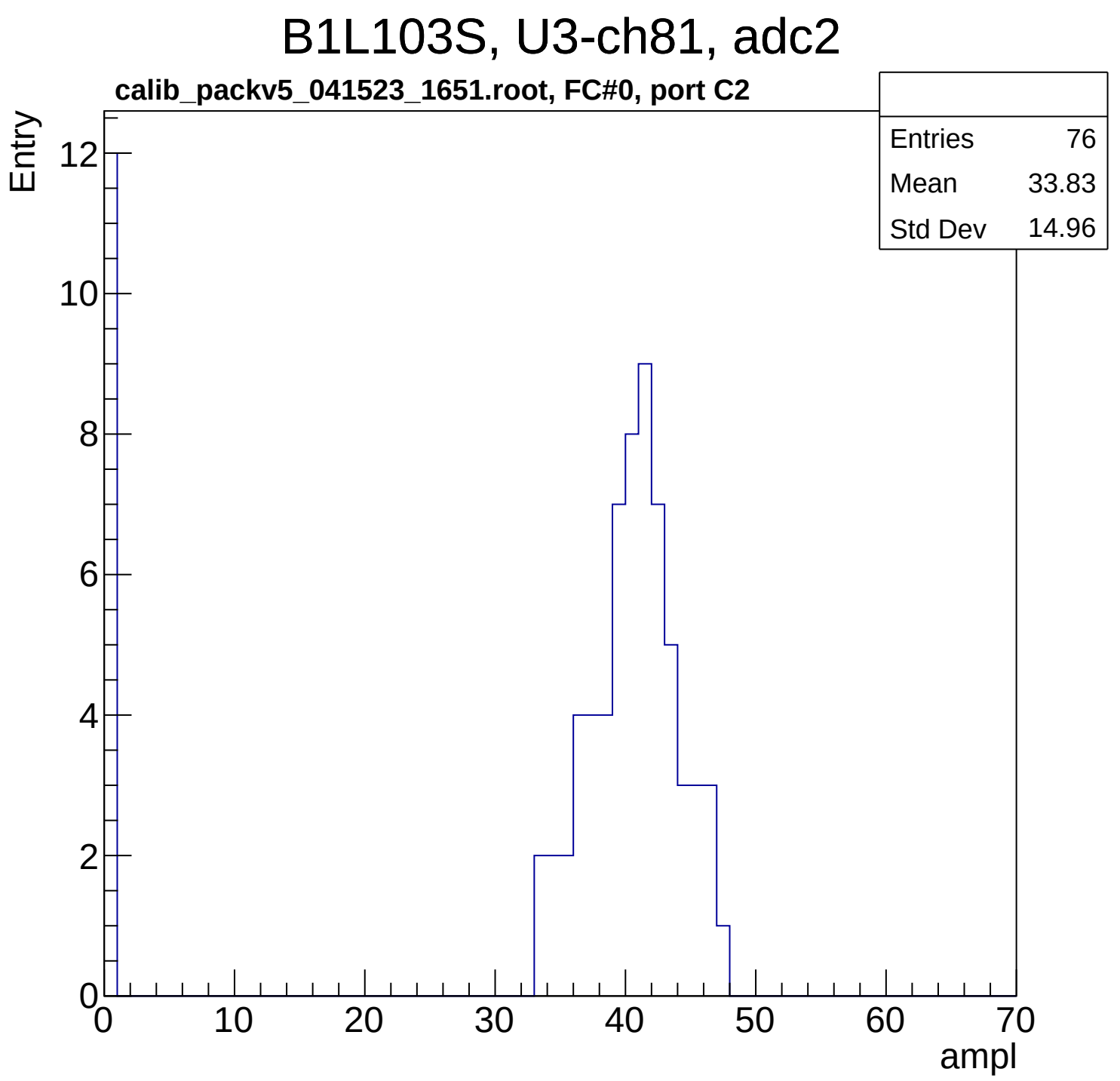
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch81, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 33.83
Std Dev 14.96
Entry
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4
6
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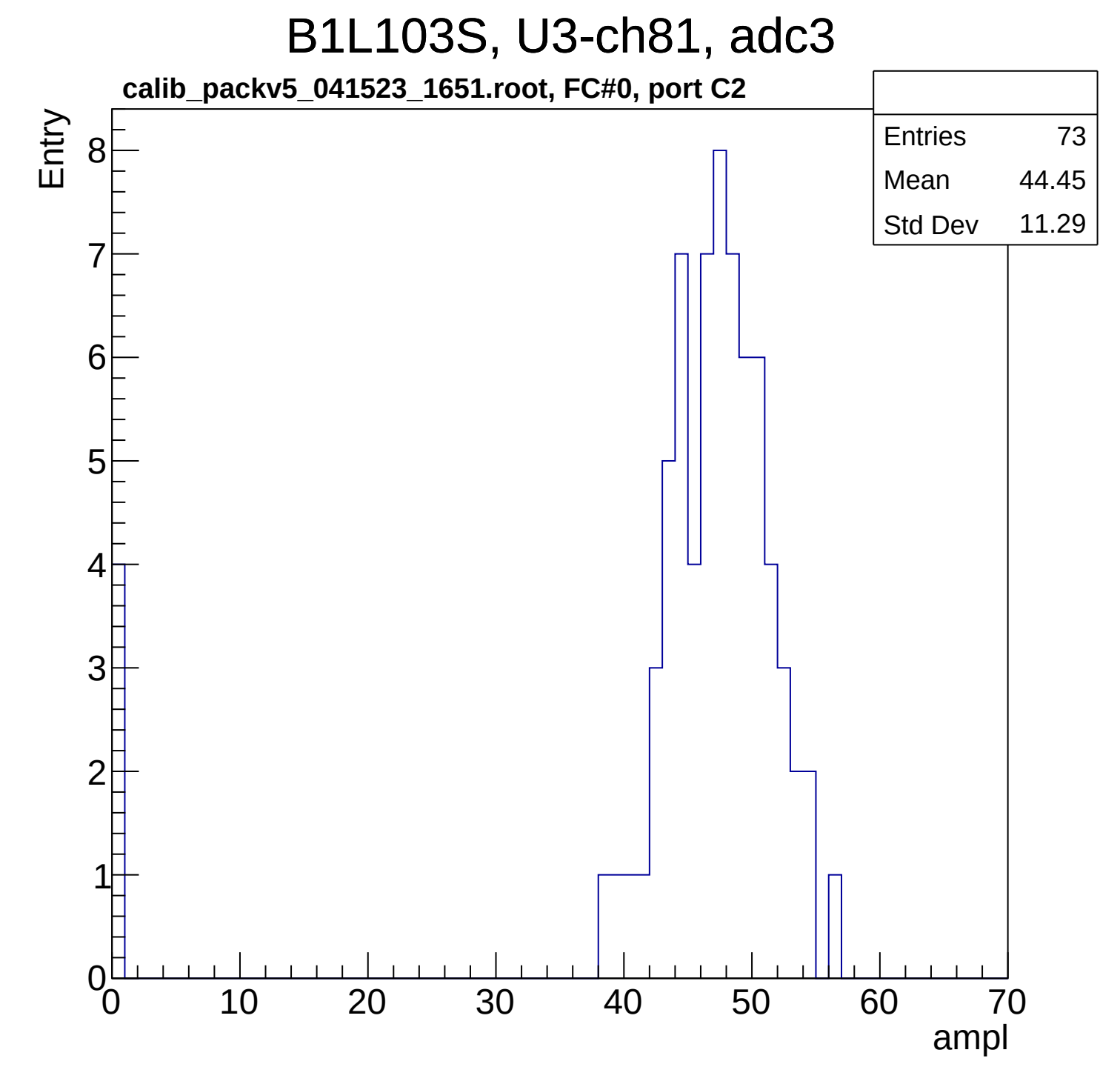
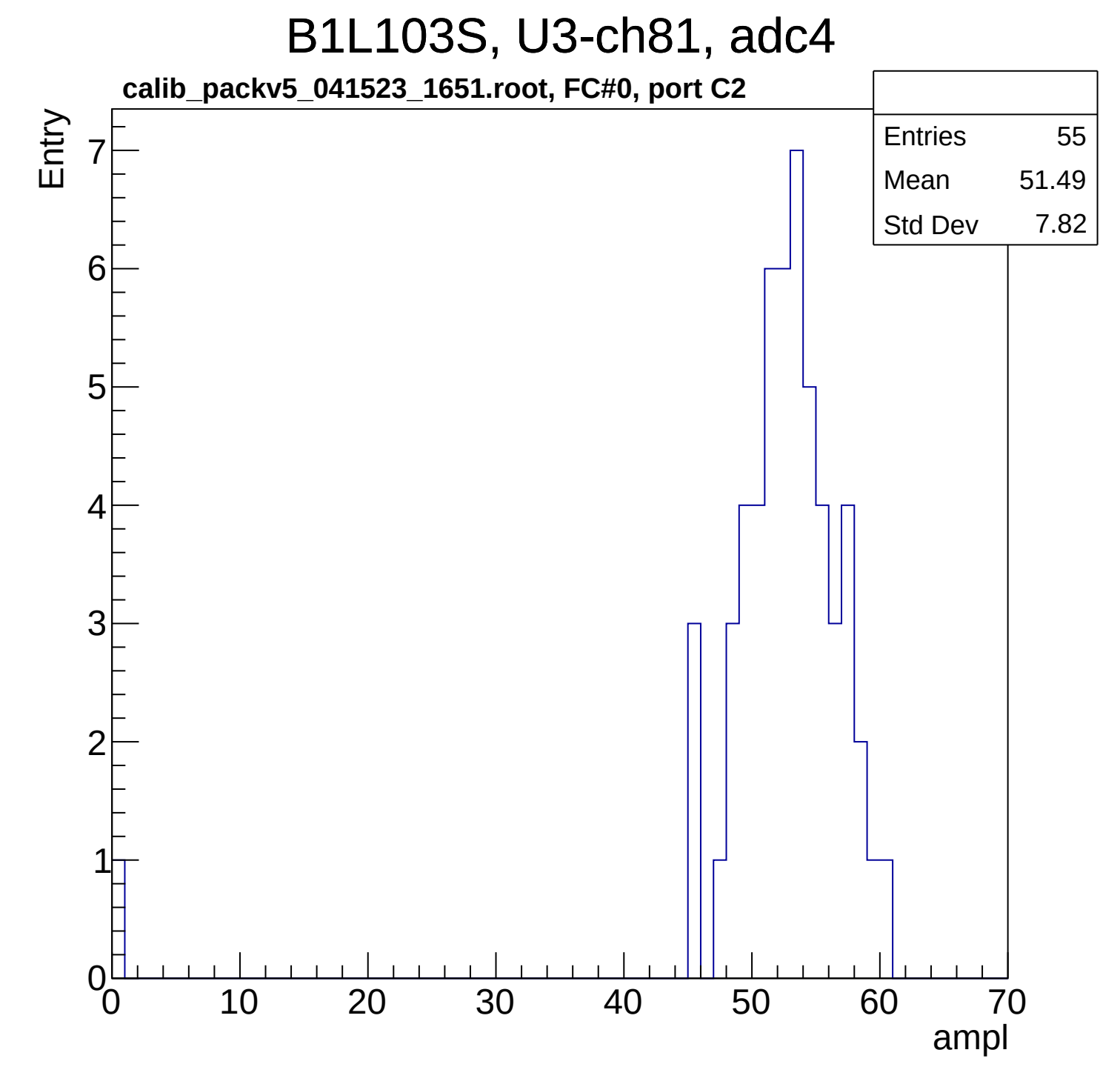
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch81, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 44.45
Std Dev 11.29
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch81, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 51.49
Std Dev 7.82
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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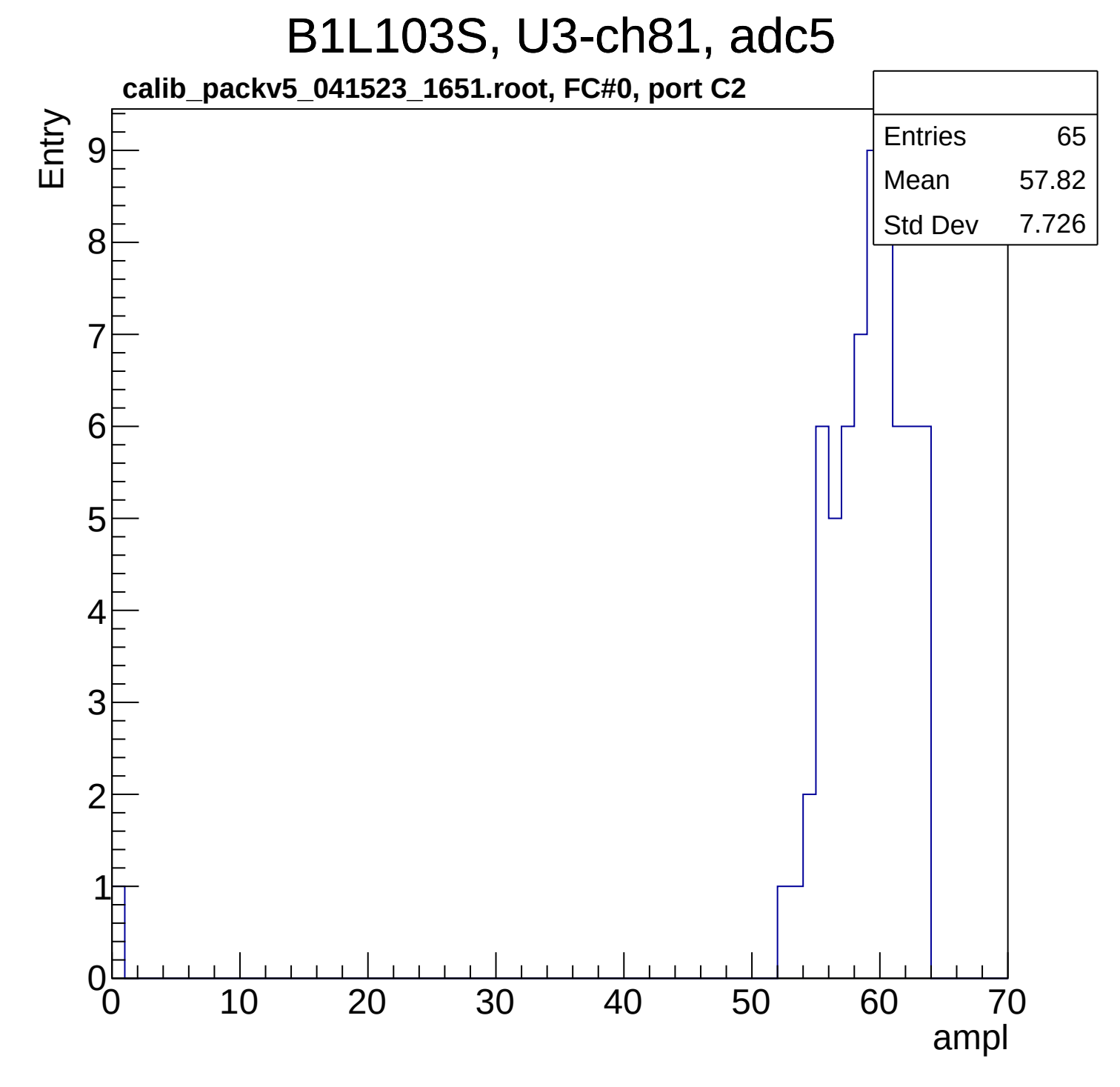
B1L103S, U3-ch81, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 57.82
Std Dev 7.726
Entry
ampl
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2
3
4
5
6
7
8
9
0
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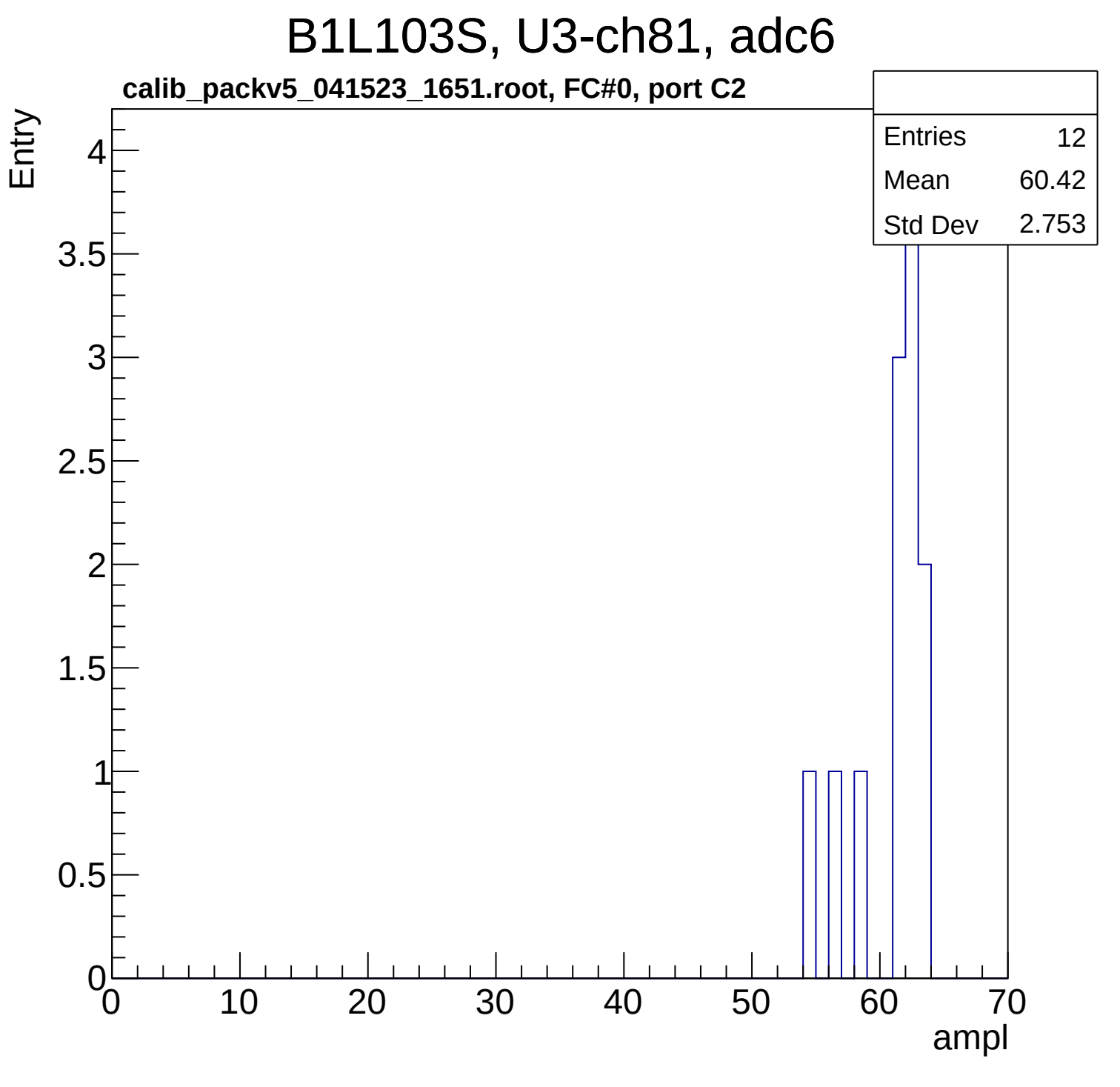
B1L103S, U3-ch81, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 60.42
Std Dev 2.753
Entry
ampl
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0.5
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1.5
2
2.5
3
3.5
4
0
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20
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40
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60
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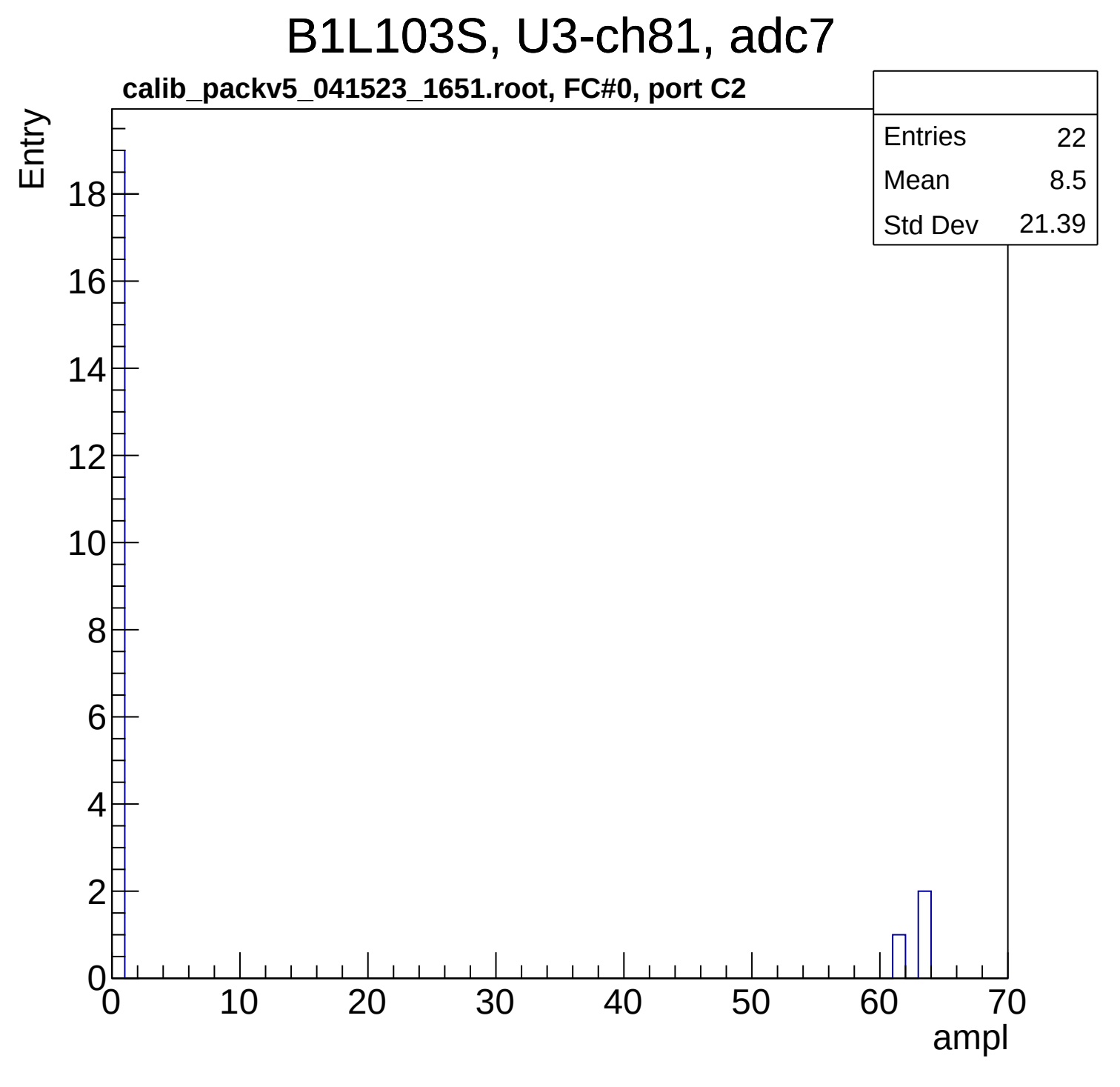
B1L103S, U3-ch81, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.5
Std Dev 21.39
Entry
0
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4
6
8
10
12
14
16
18
0
10
20
30
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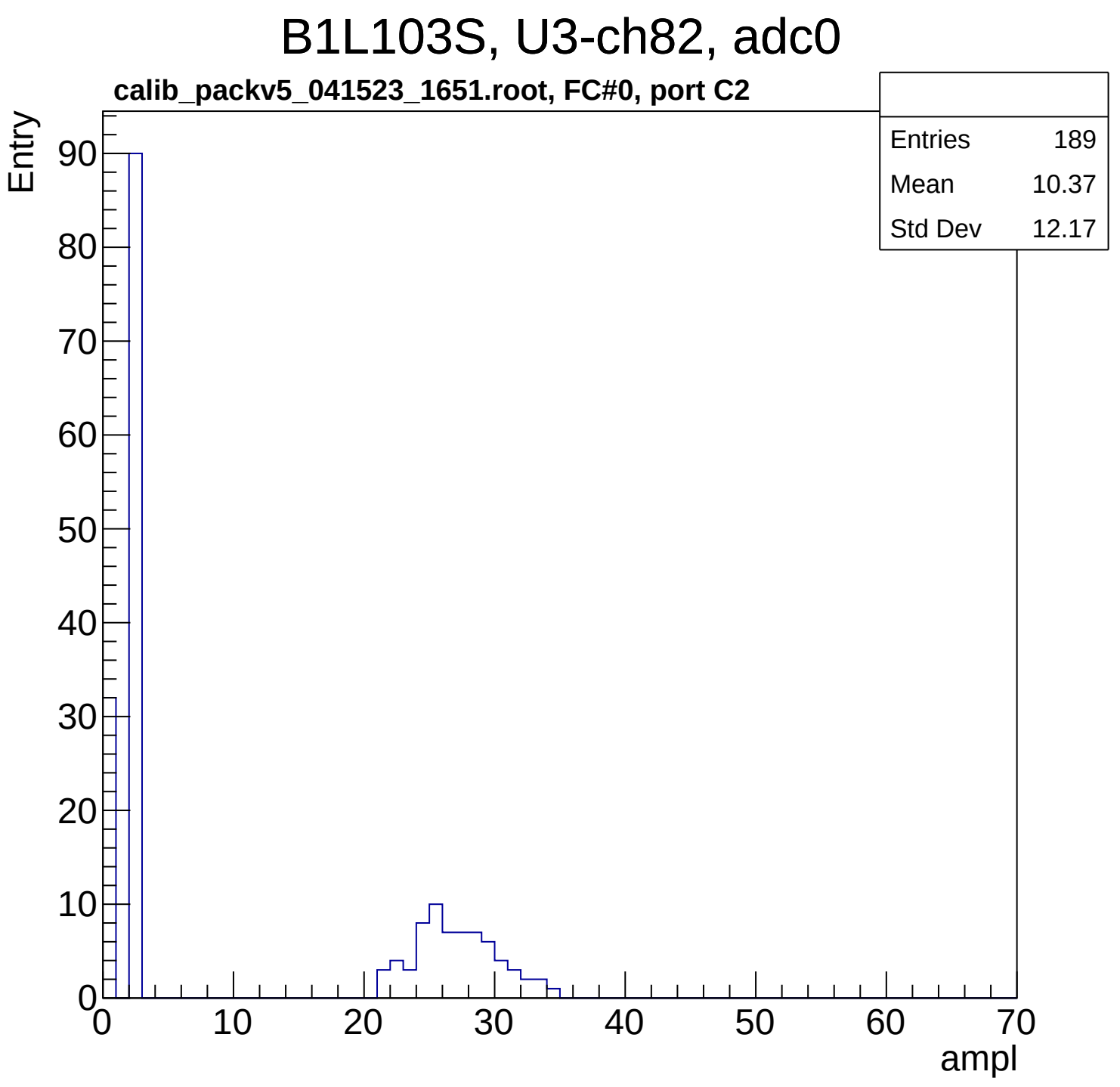
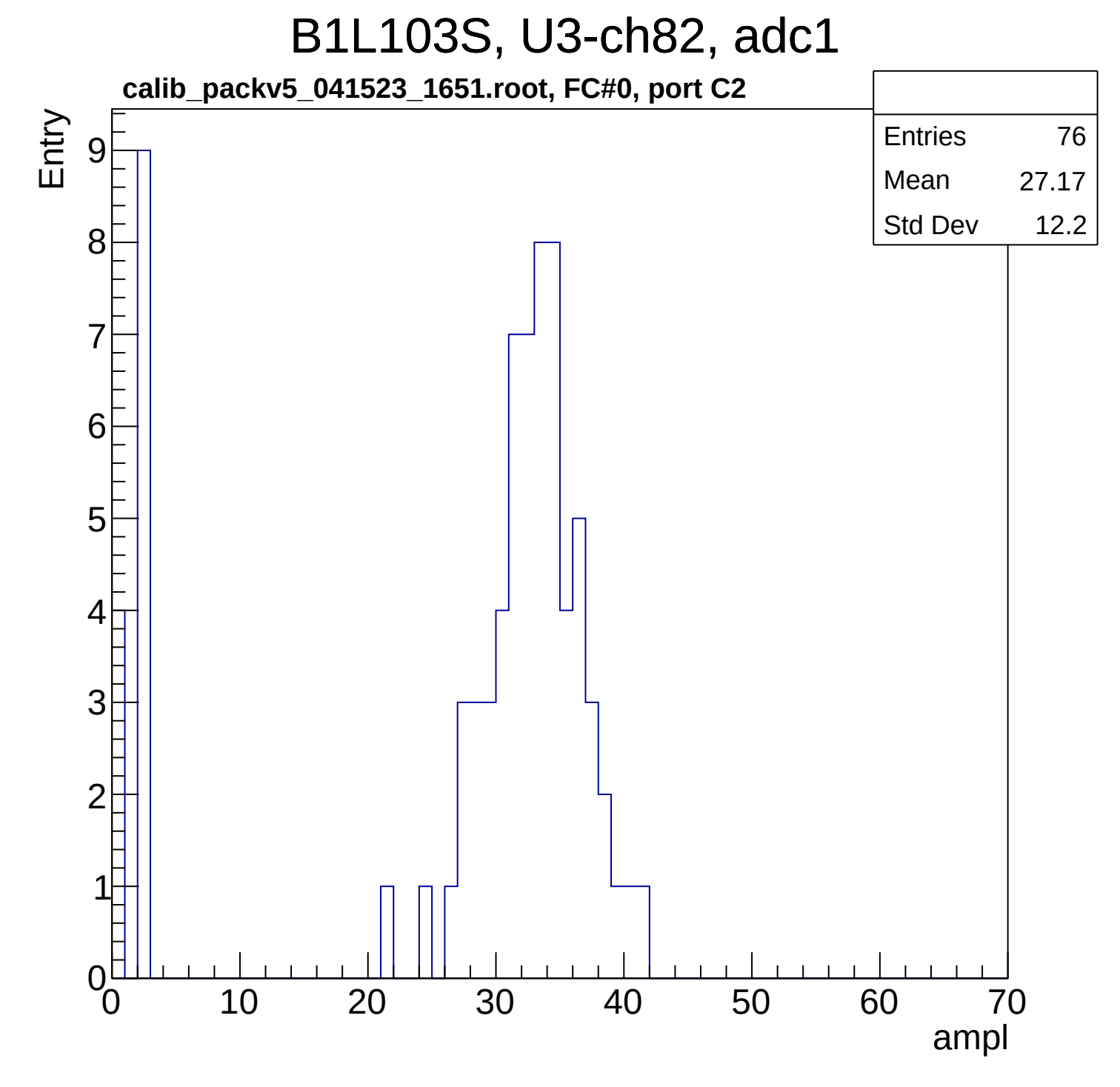
50
60
70
ampl


B1L103S, U3-ch82, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 189
Mean 10.37
Std Dev 12.17
Entry
ampl
0
10
20
30
40
50
60
70
80
90


B1L103S, U3-ch82, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 27.17
Std Dev 12.2
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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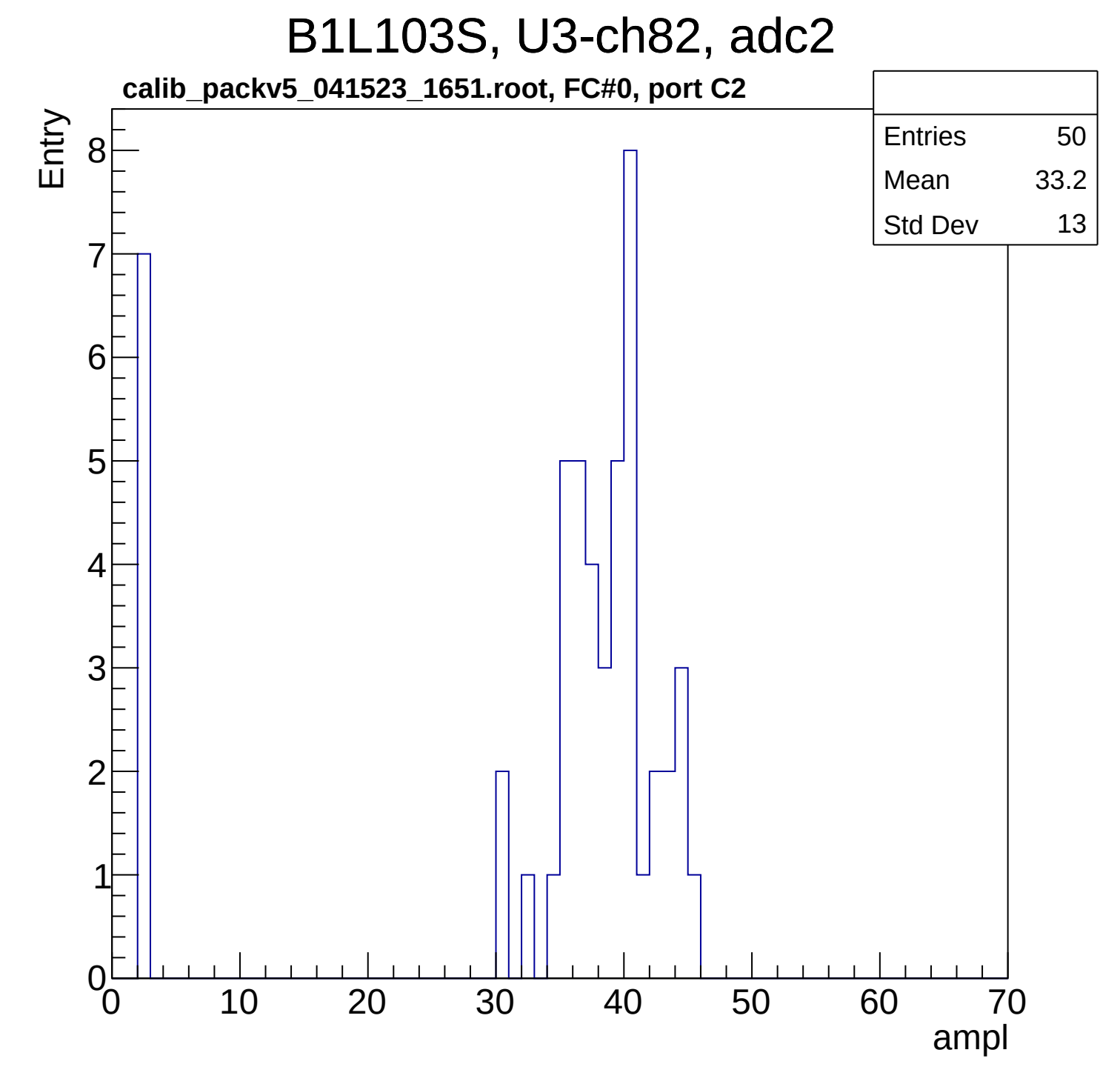
B1L103S, U3-ch82, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 33.2
Std Dev 13
Entry
ampl
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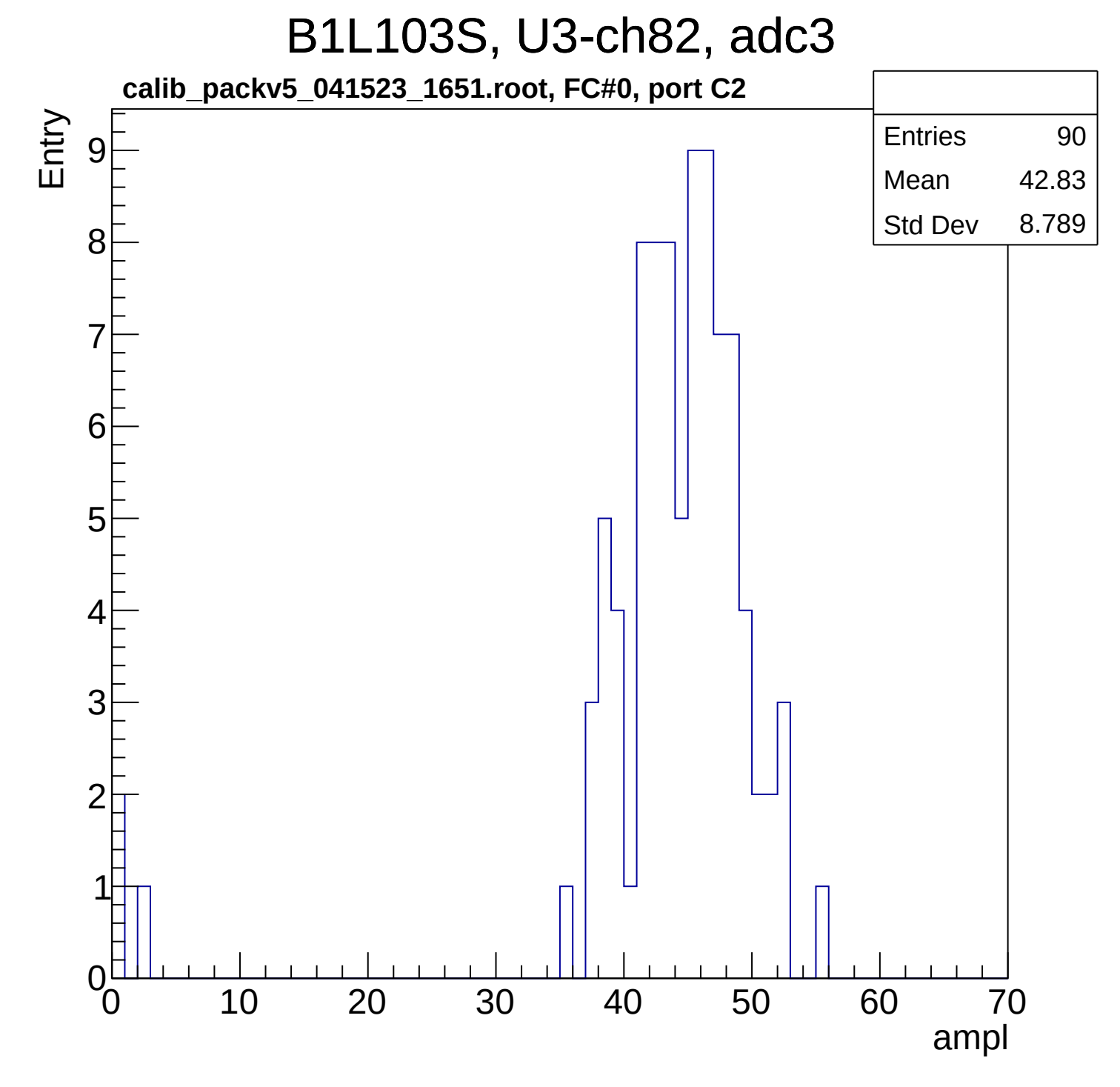
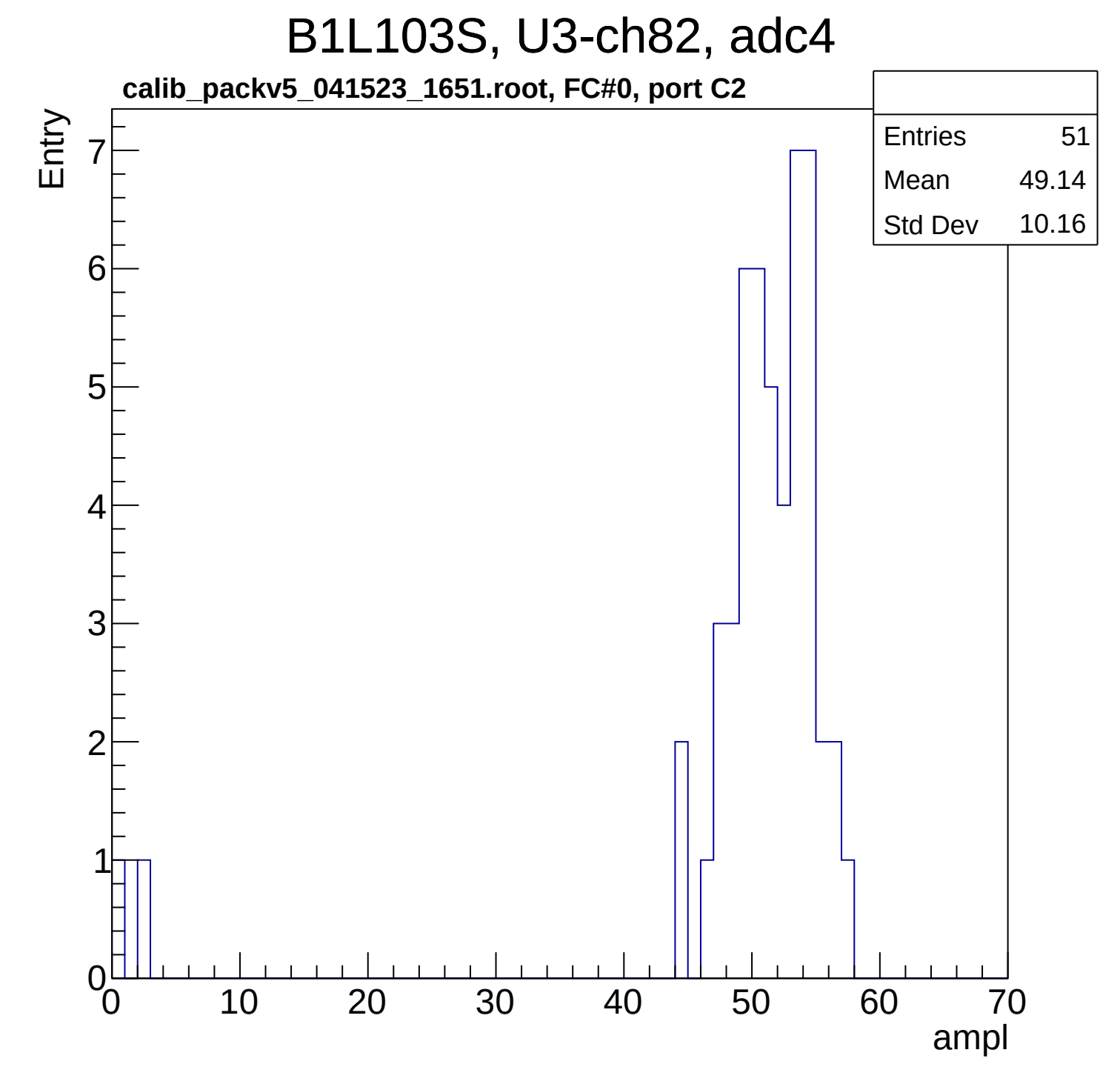
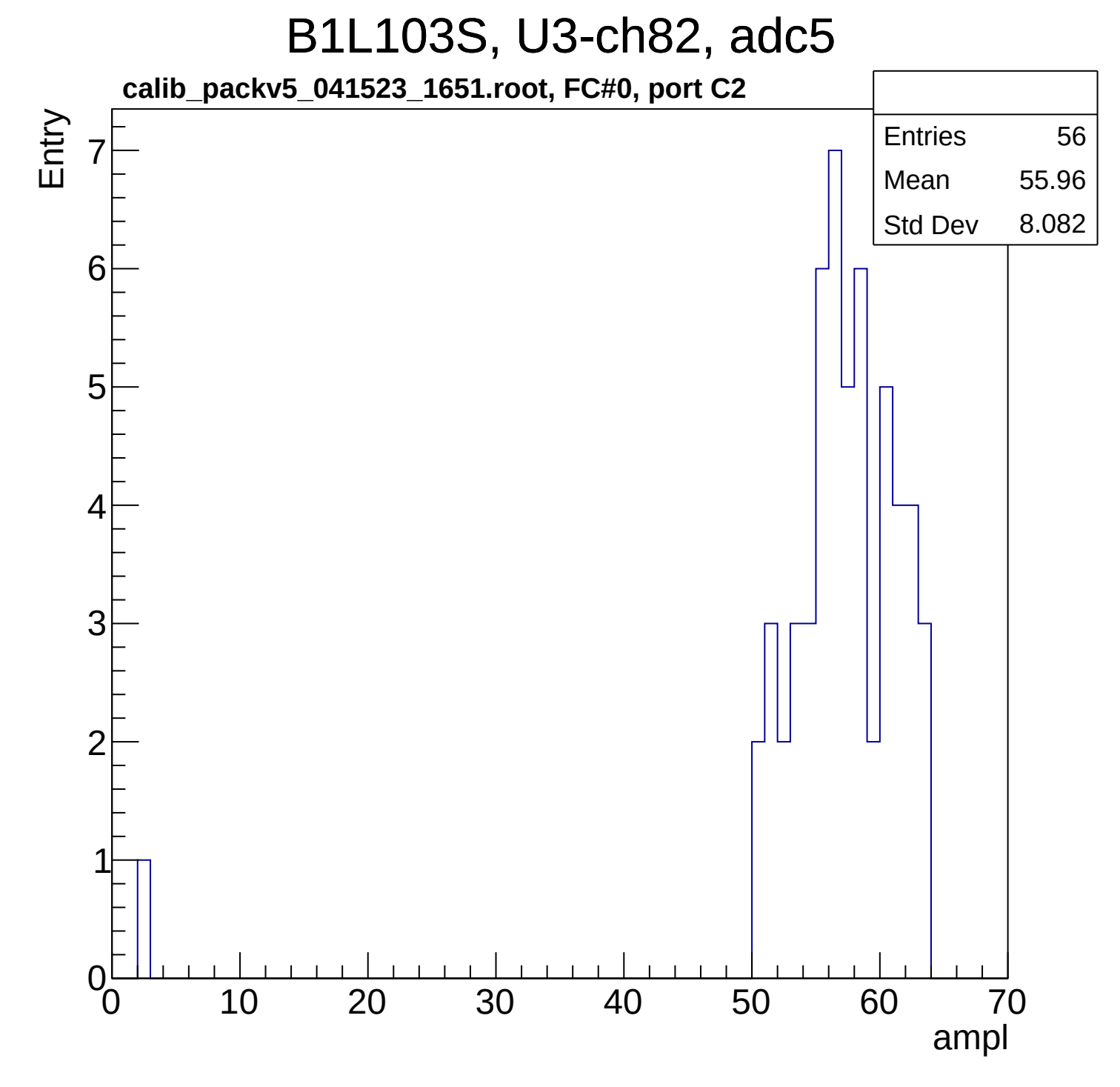
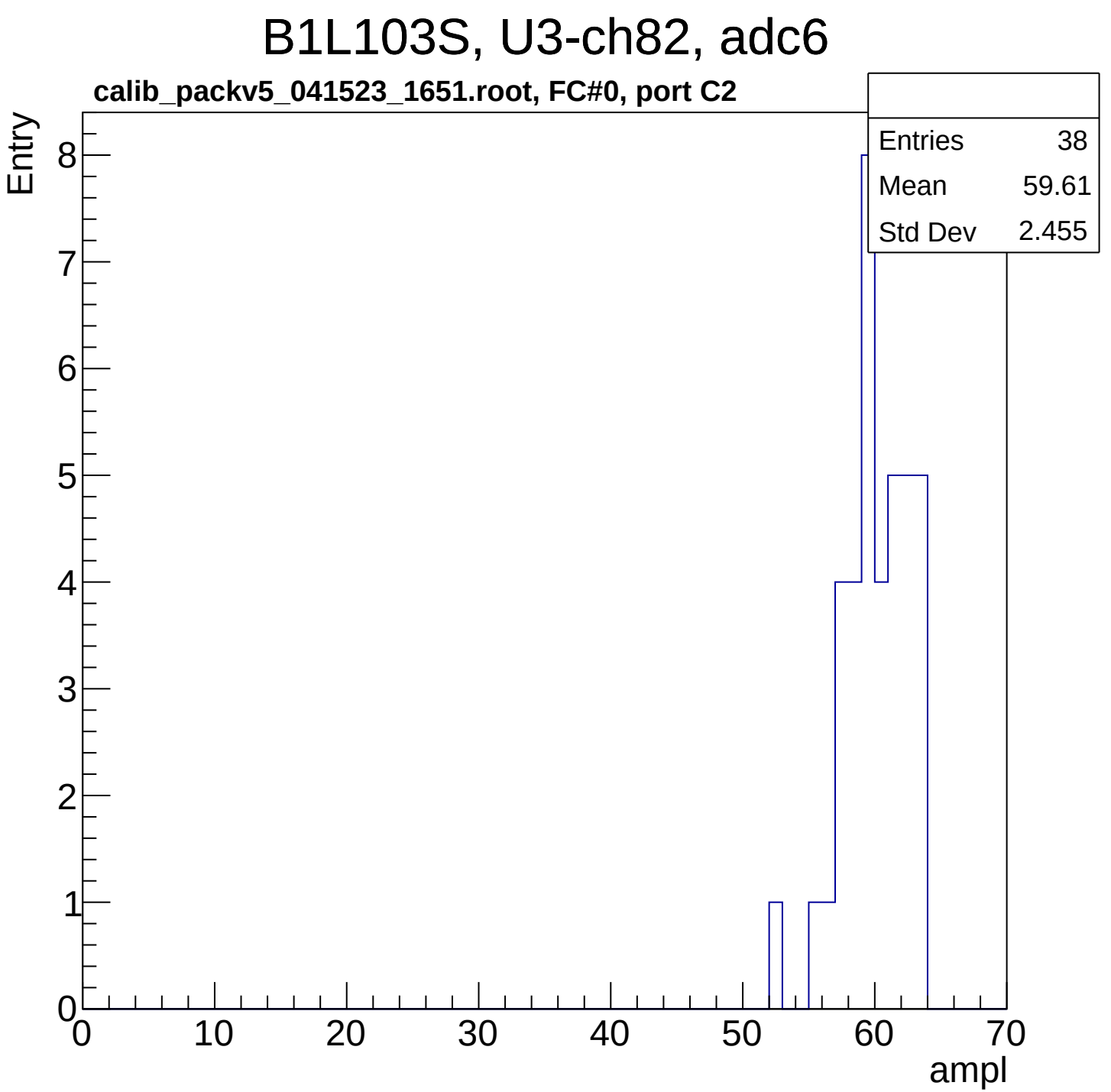
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch82, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 42.83
Std Dev 8.789
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch82, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 49.14
Std Dev 10.16
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch82, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 55.96
Std Dev 8.082
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch82, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 59.61
Std Dev 2.455
Entry
ampl
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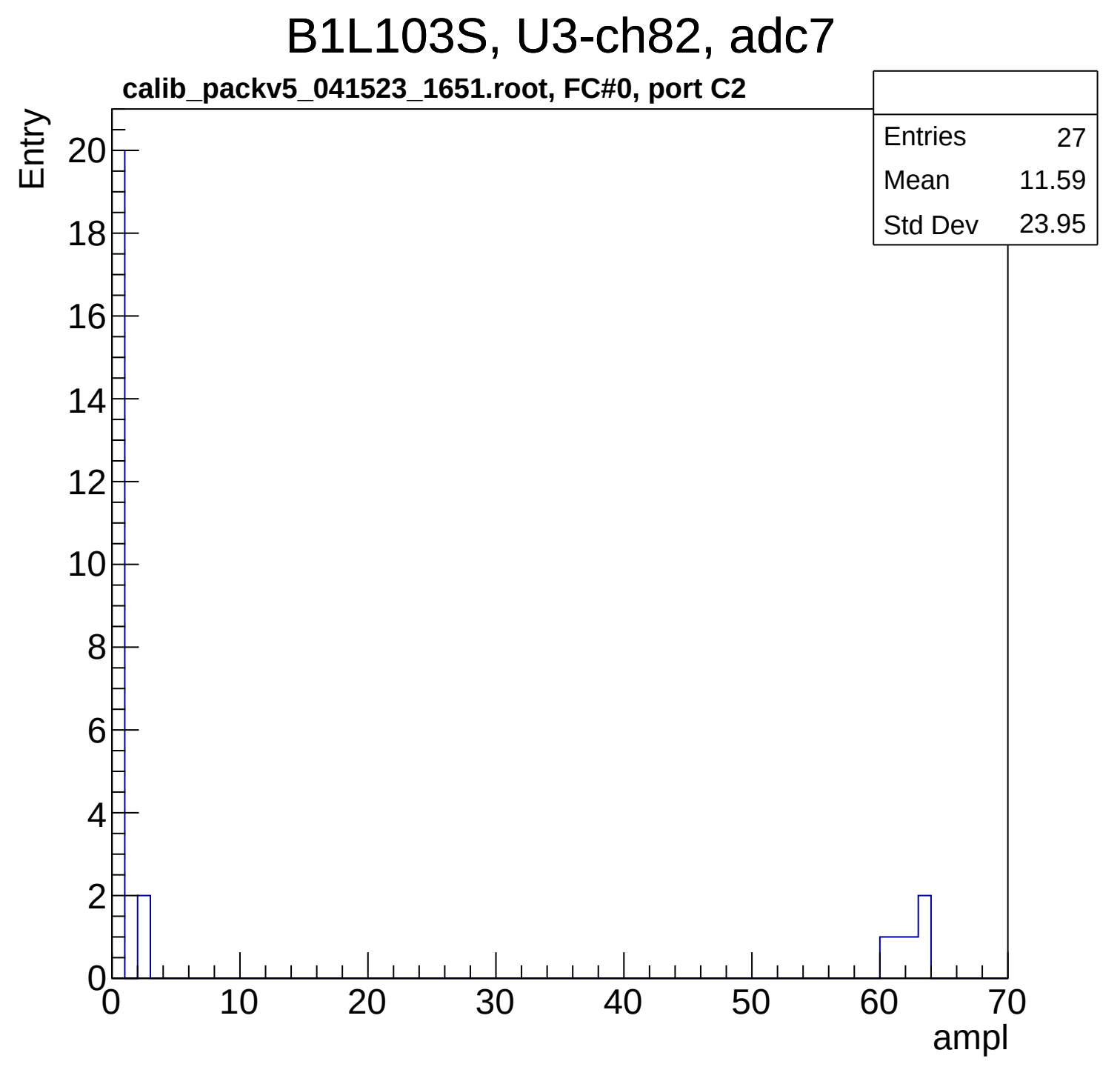
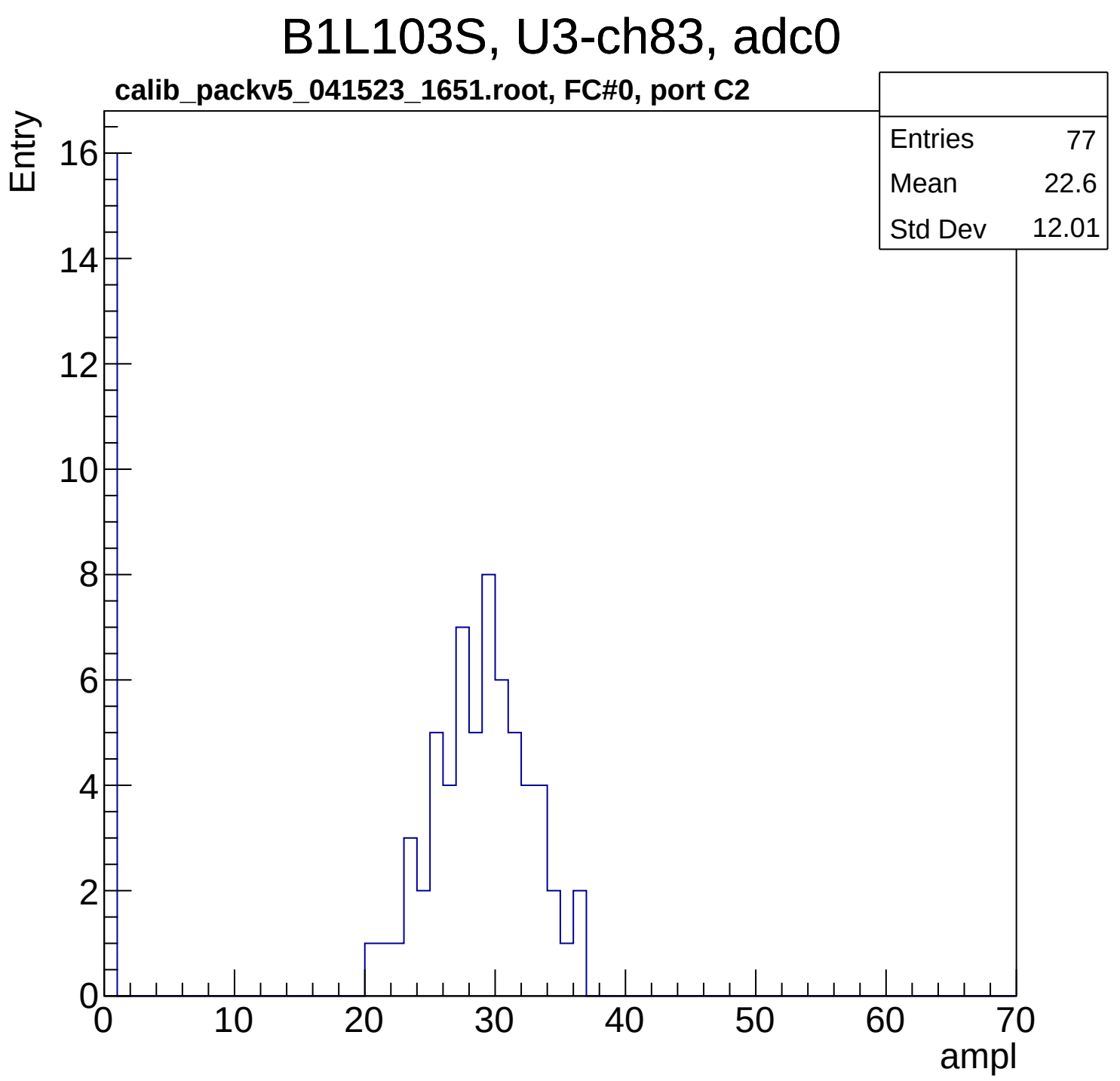
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch82, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 11.59
Std Dev 23.95
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70


B1L103S, U3-ch83, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 22.6
Std Dev 12.01
Entry
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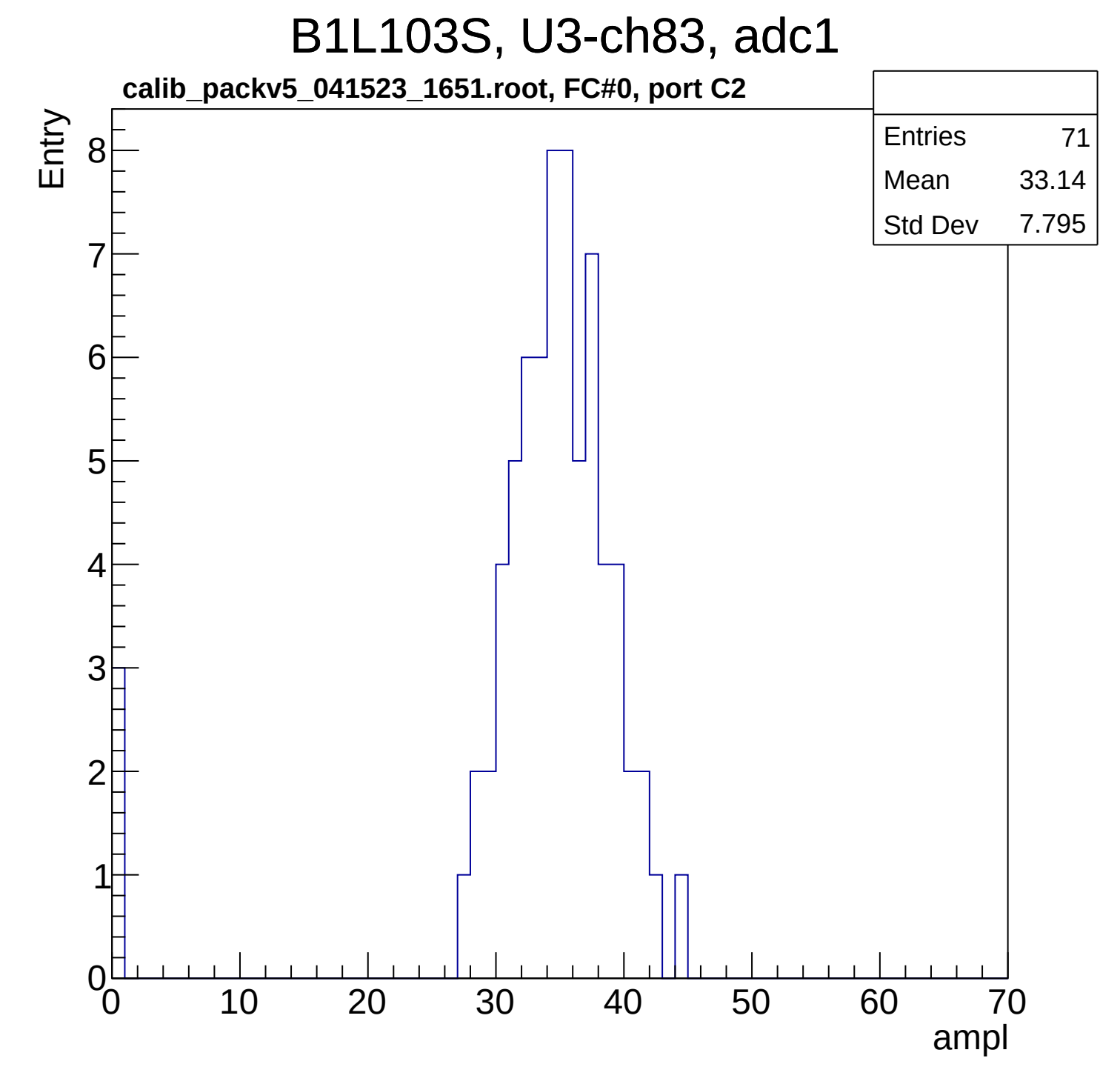
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch83, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 33.14
Std Dev 7.795
Entry
ampl
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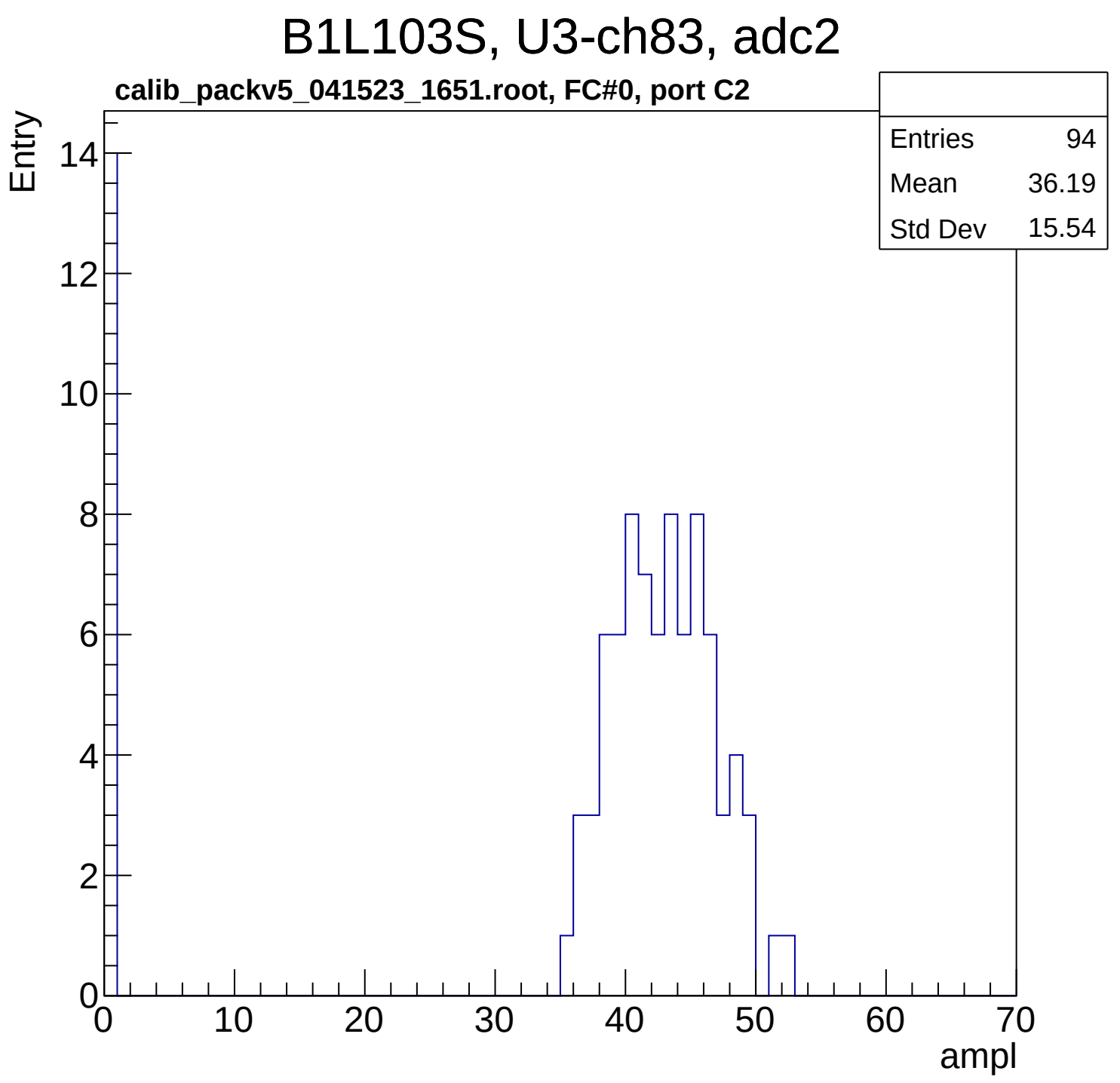
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch83, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 36.19
Std Dev 15.54
Entry
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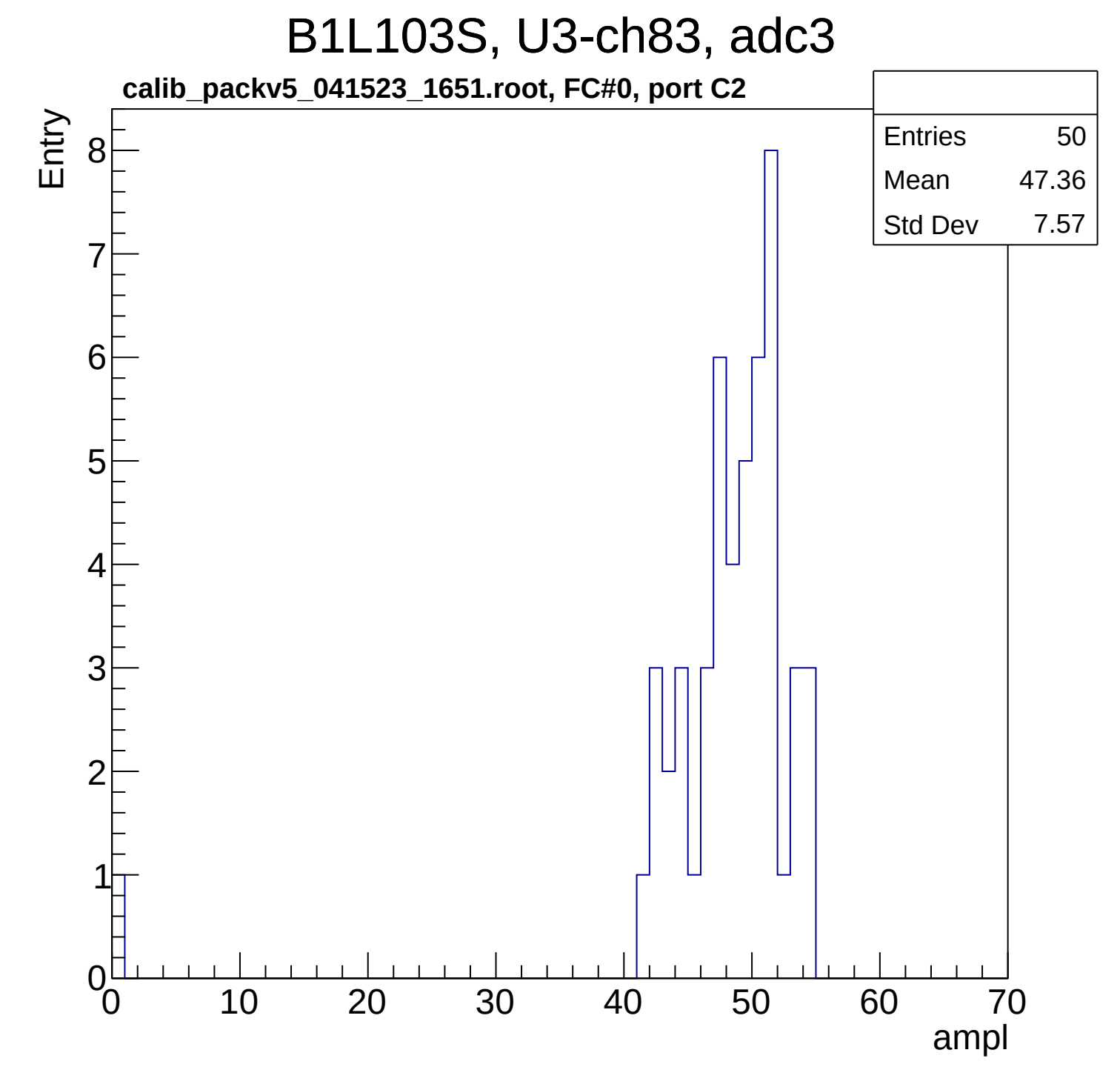
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch83, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 47.36
Std Dev 7.57
Entry
ampl
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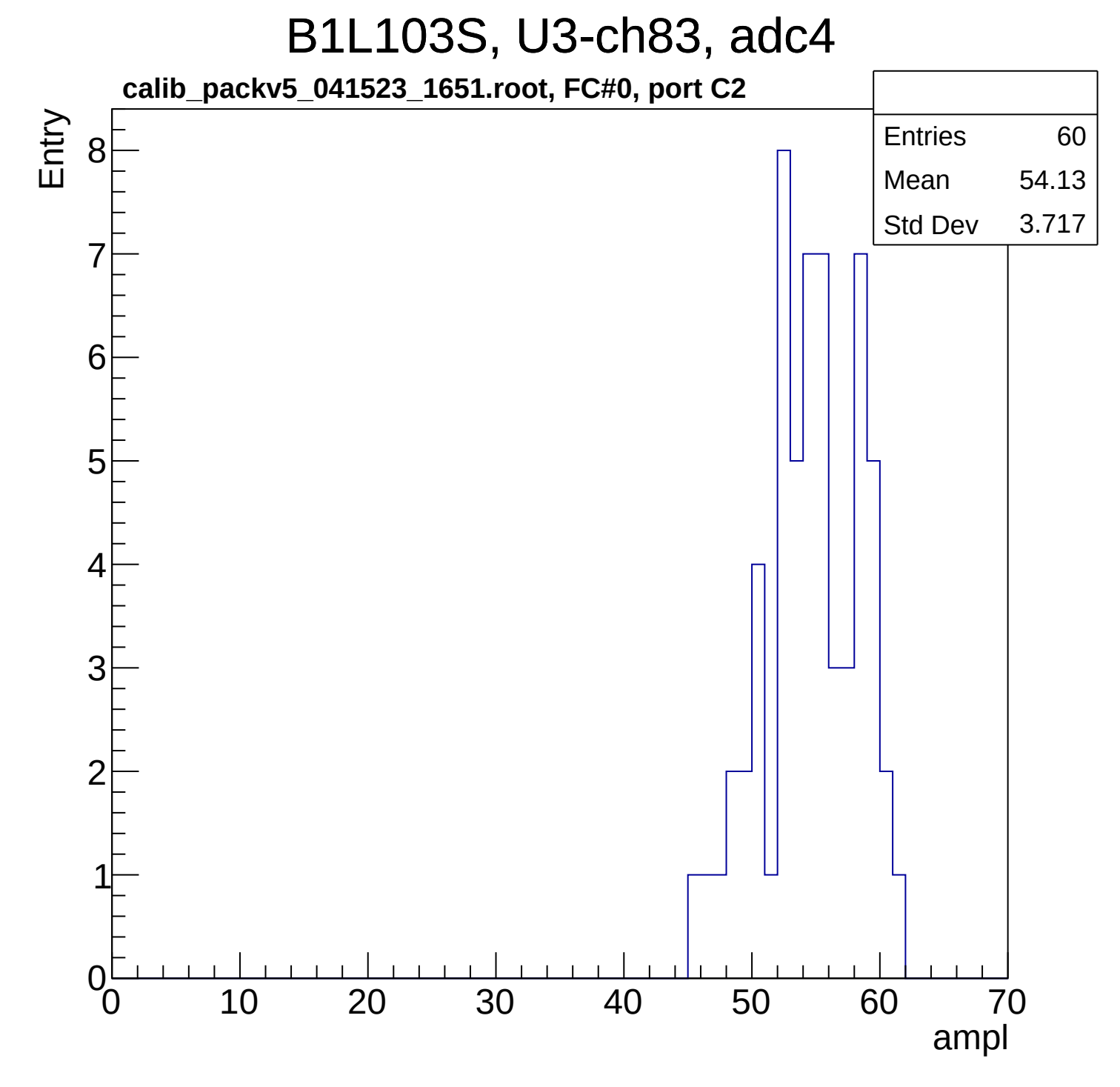
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch83, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 54.13
Std Dev 3.717
Entry
ampl
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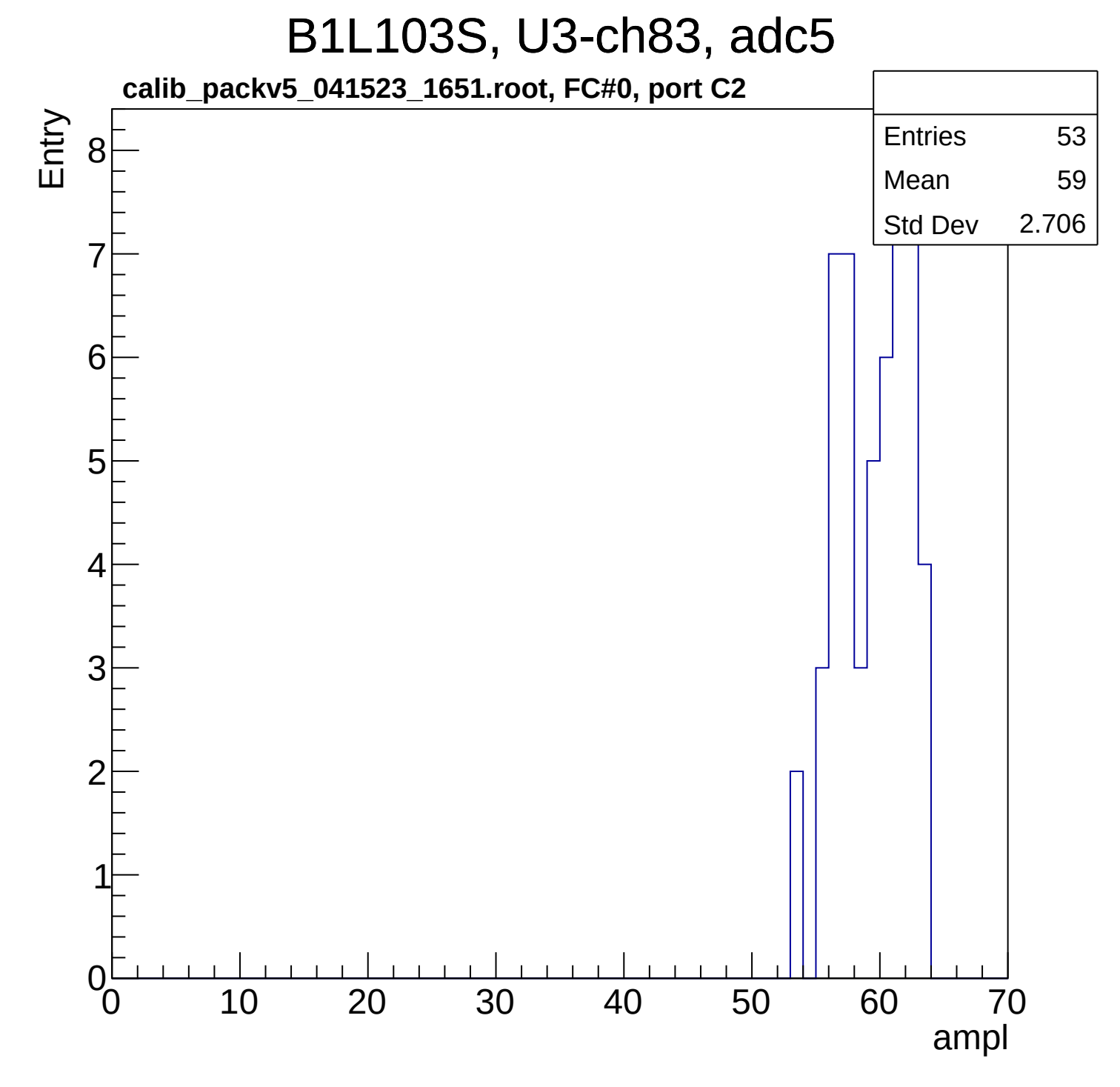
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch83, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 59
Std Dev 2.706
Entry
ampl
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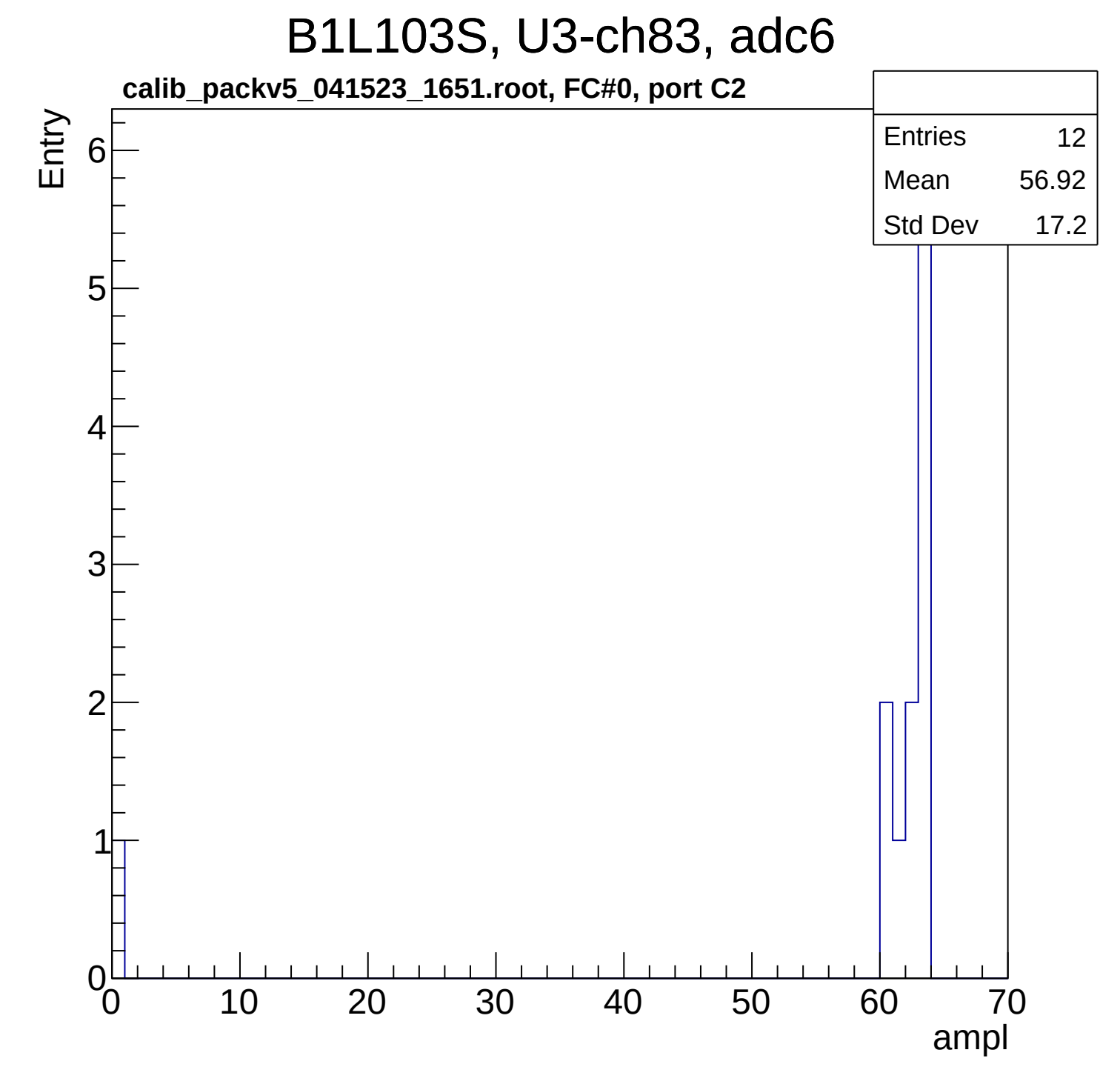
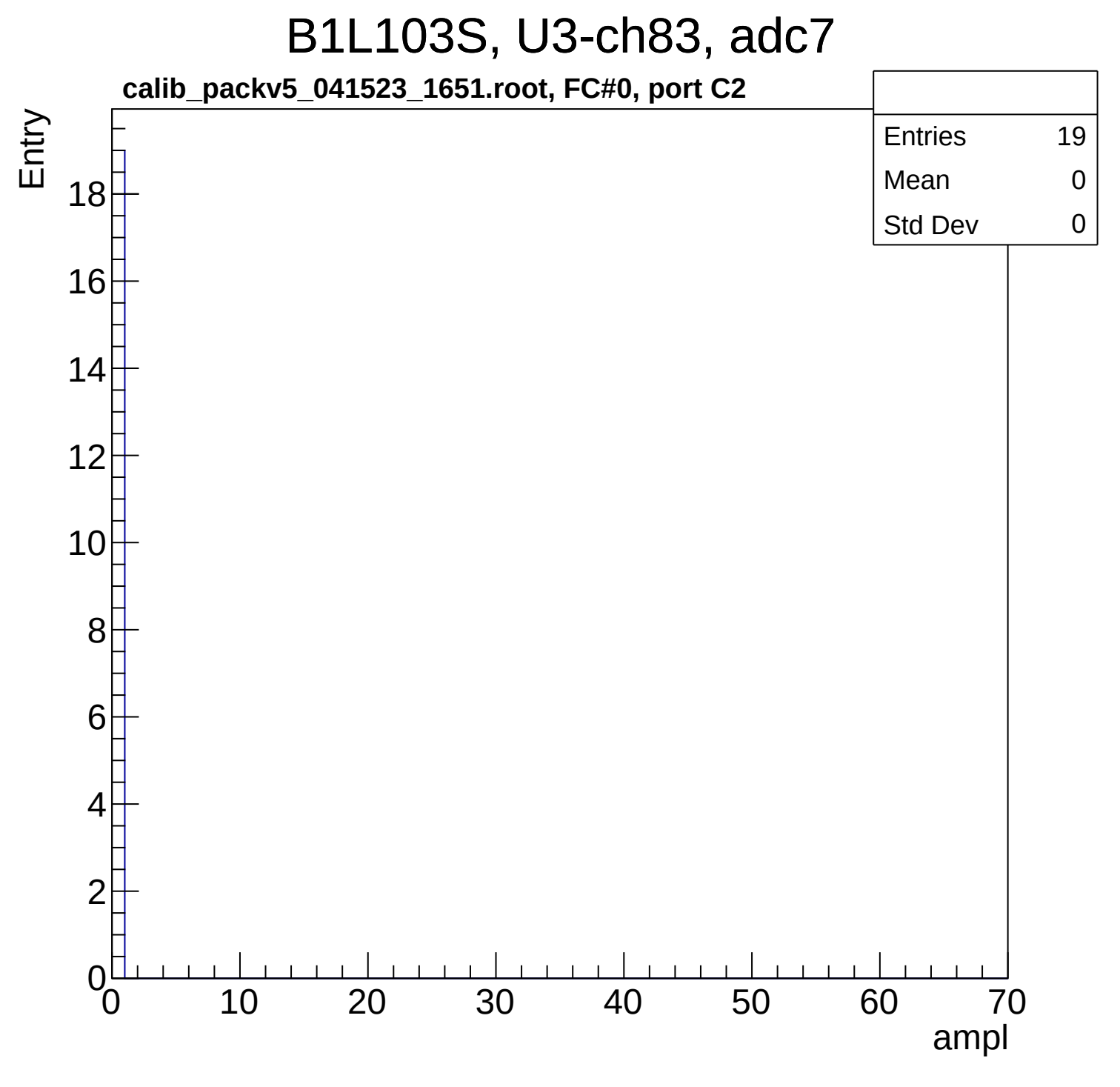
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch83, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 56.92
Std Dev 17.2
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch83, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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4
6
8
10
12
14
16
18
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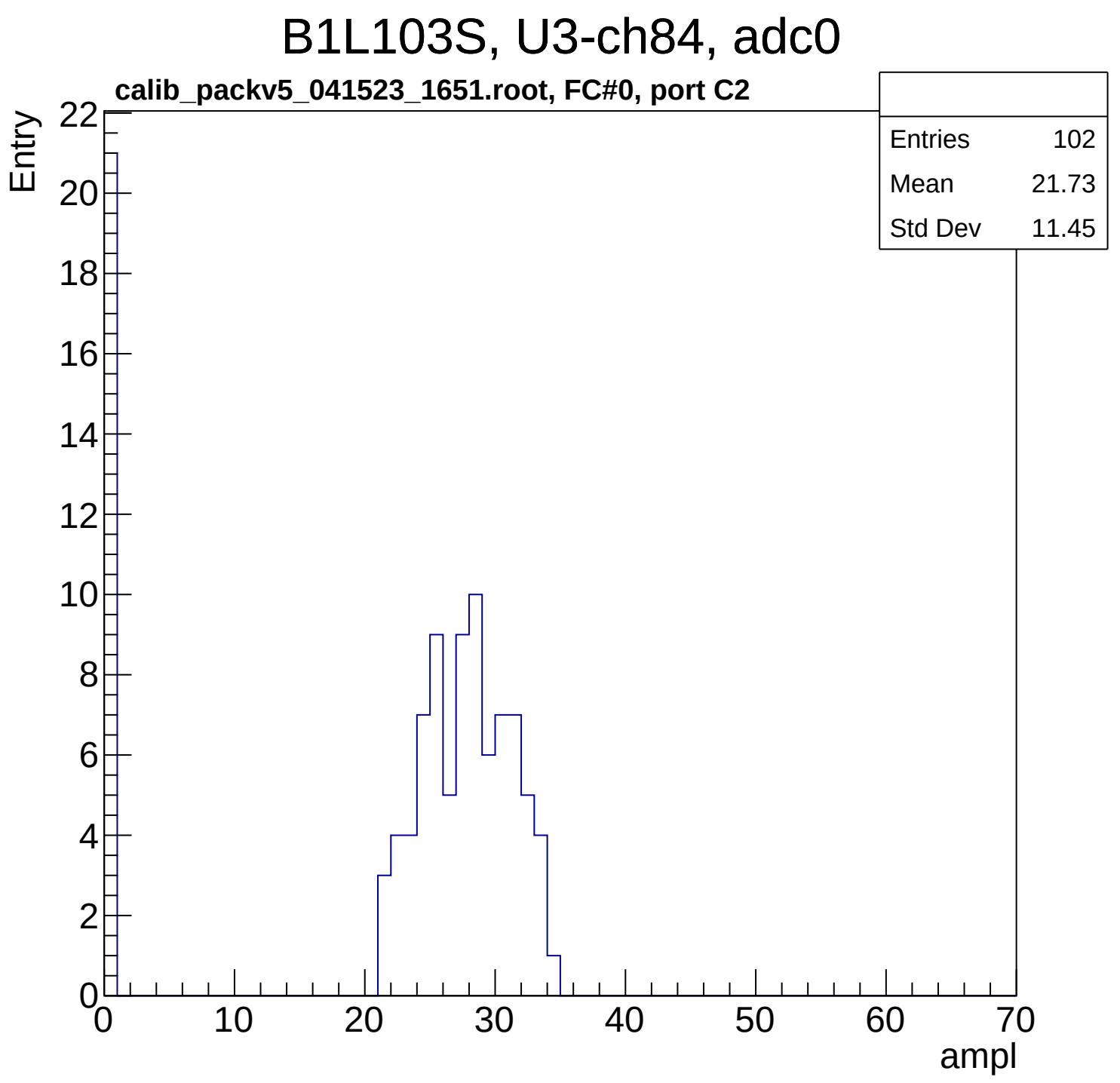
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch84, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 102
Mean 21.73
Std Dev 11.45
Entry
ampl
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2
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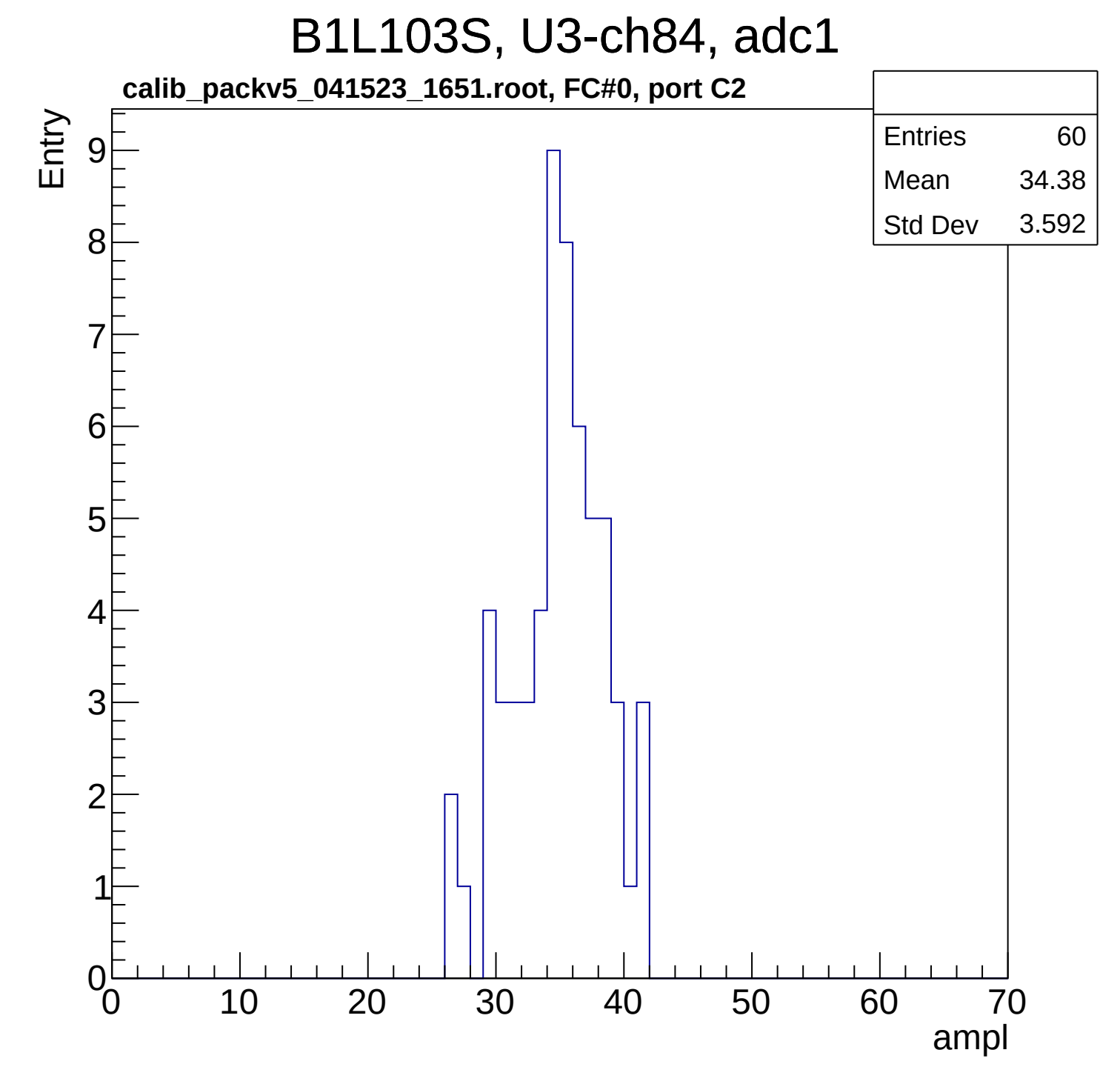
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70


B1L103S, U3-ch84, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 34.38
Std Dev 3.592
Entry
ampl
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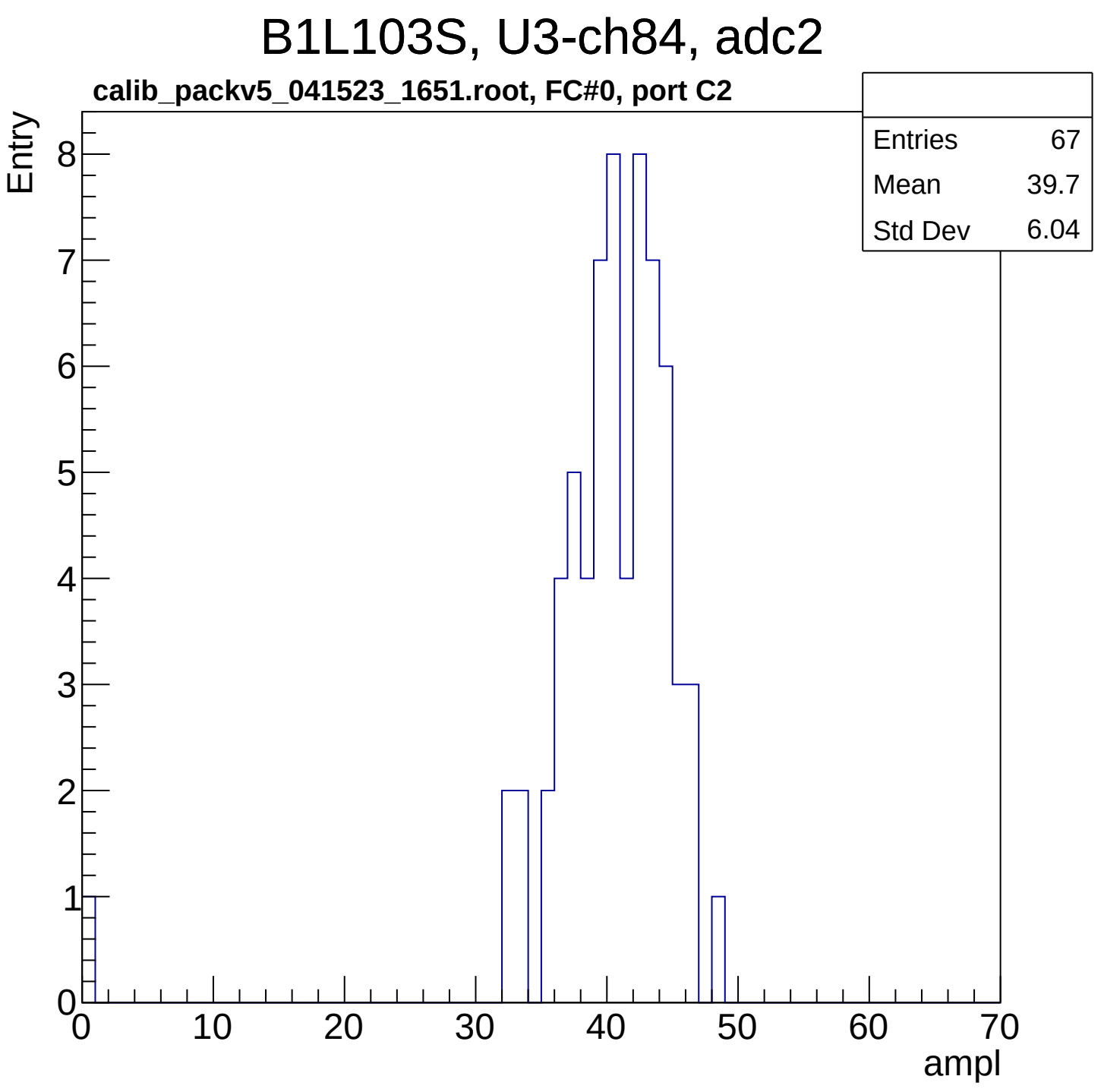
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch84, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 39.7
Std Dev 6.04
Entry
ampl
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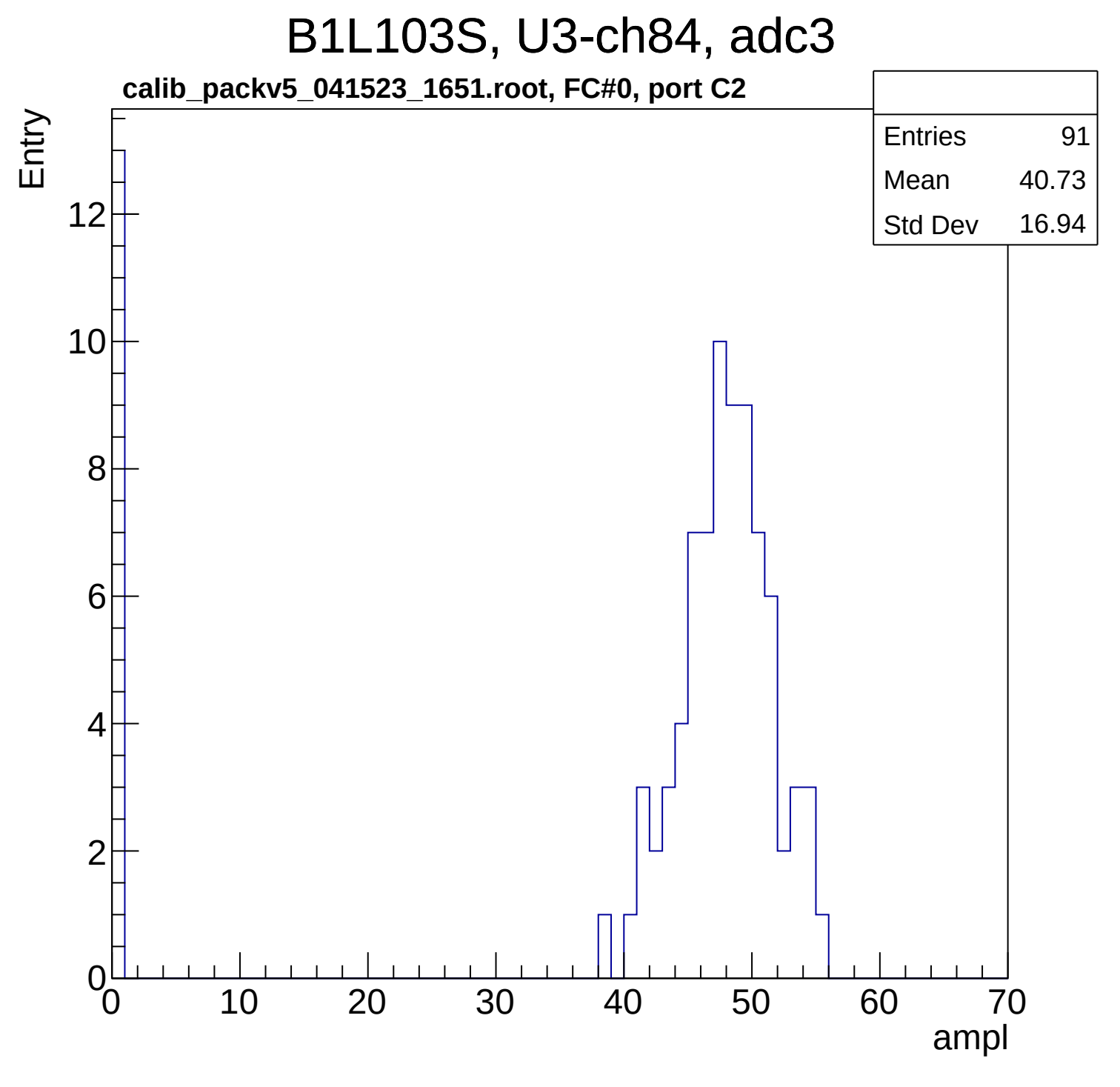
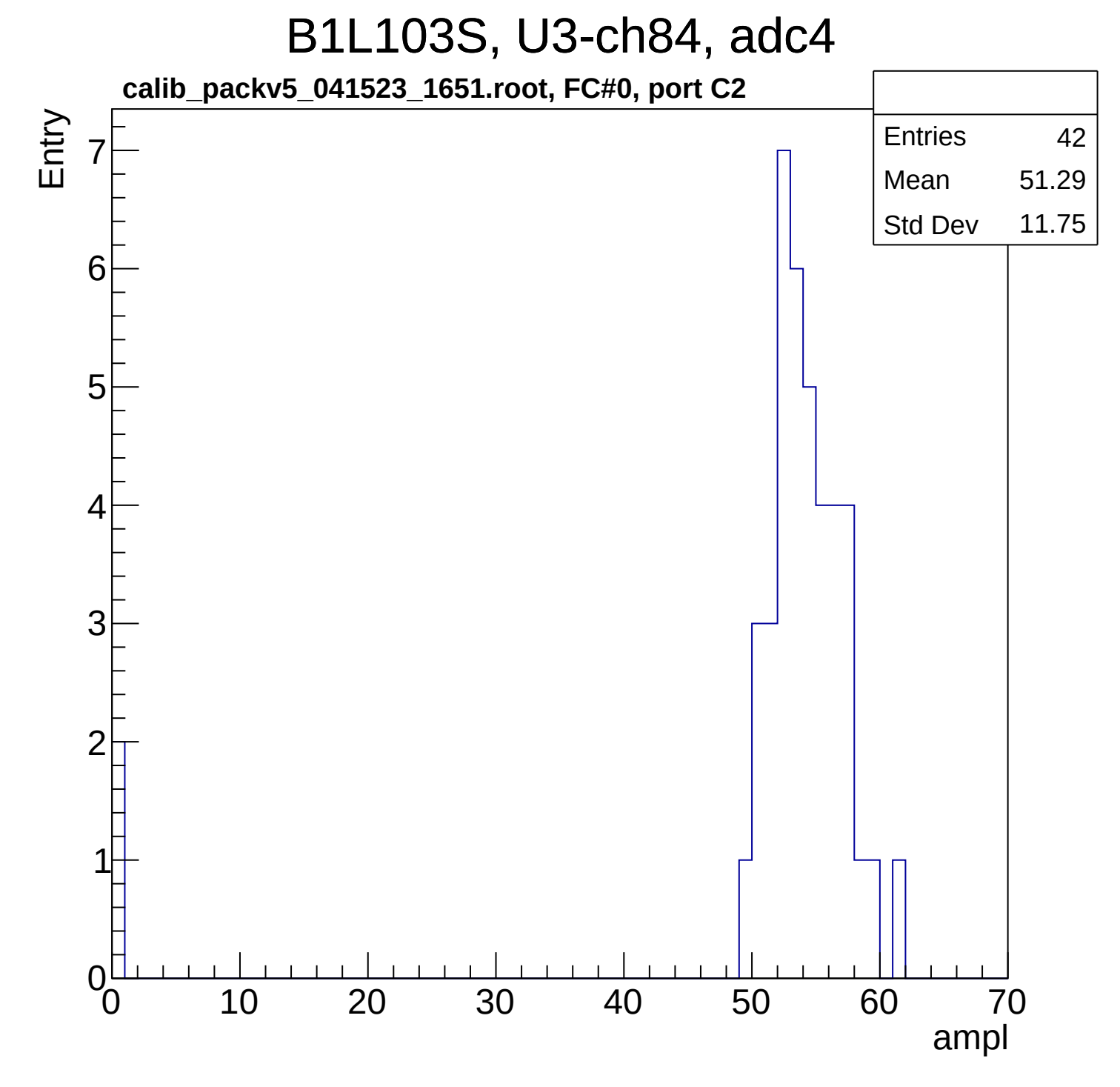
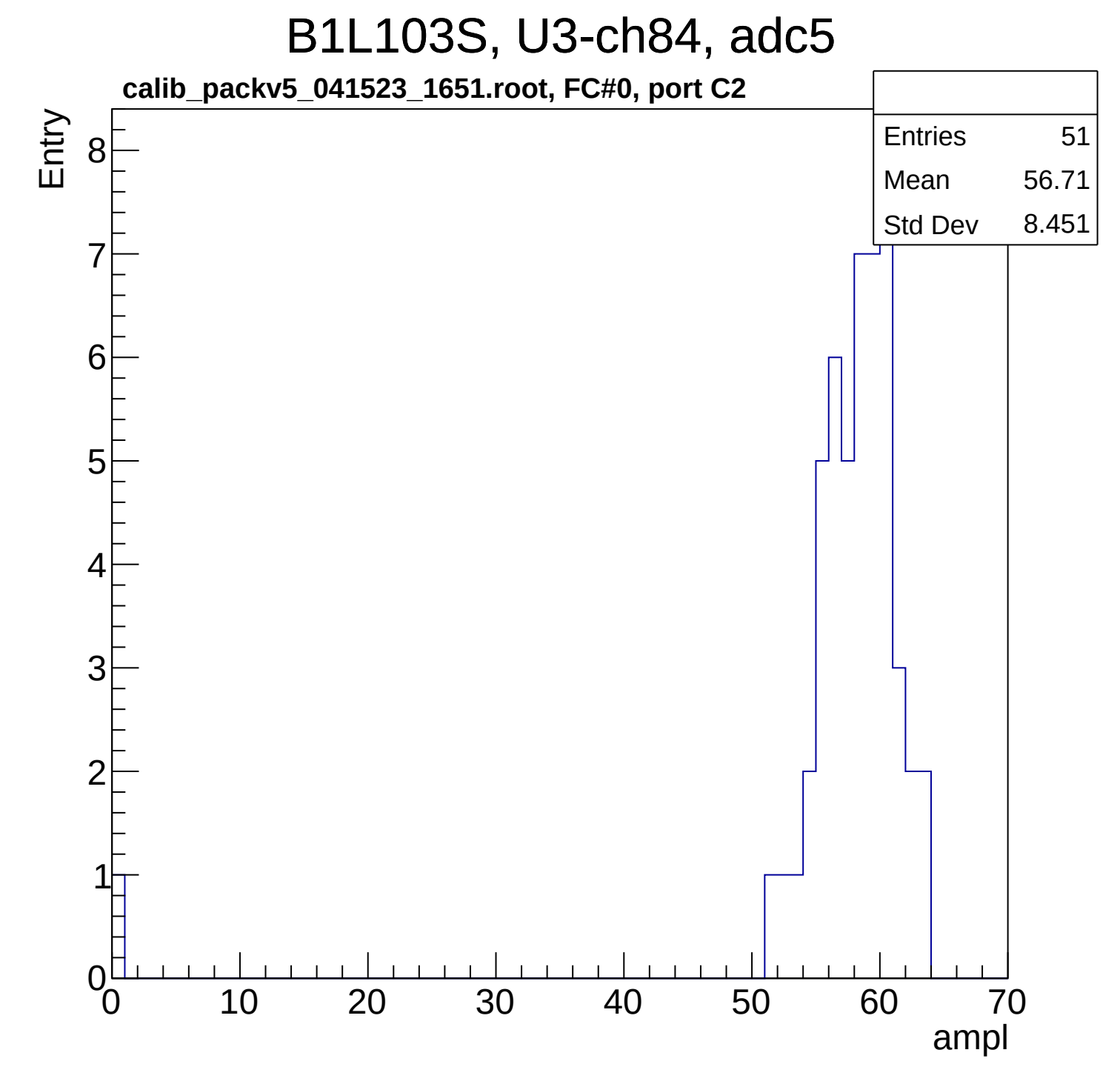
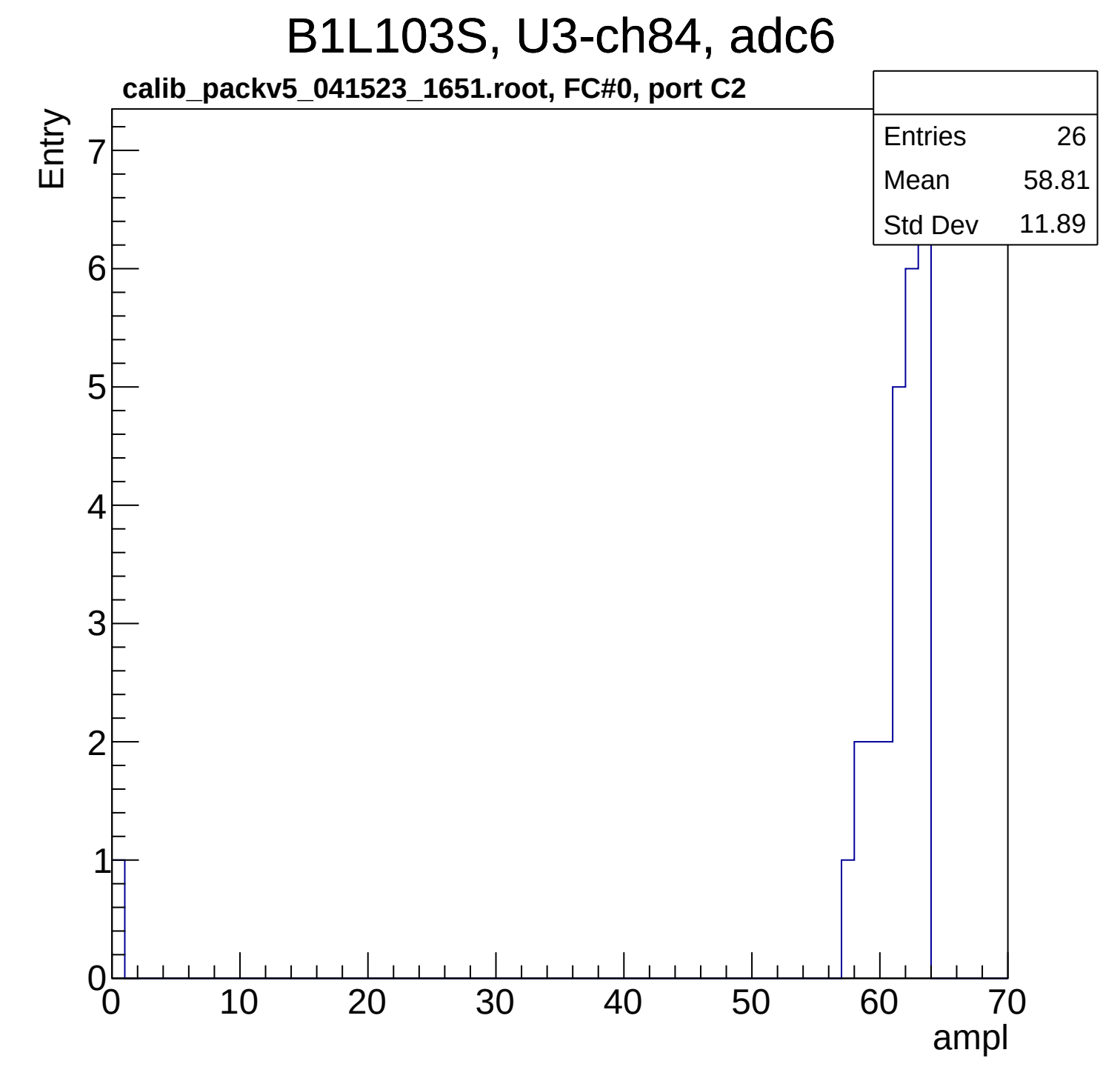
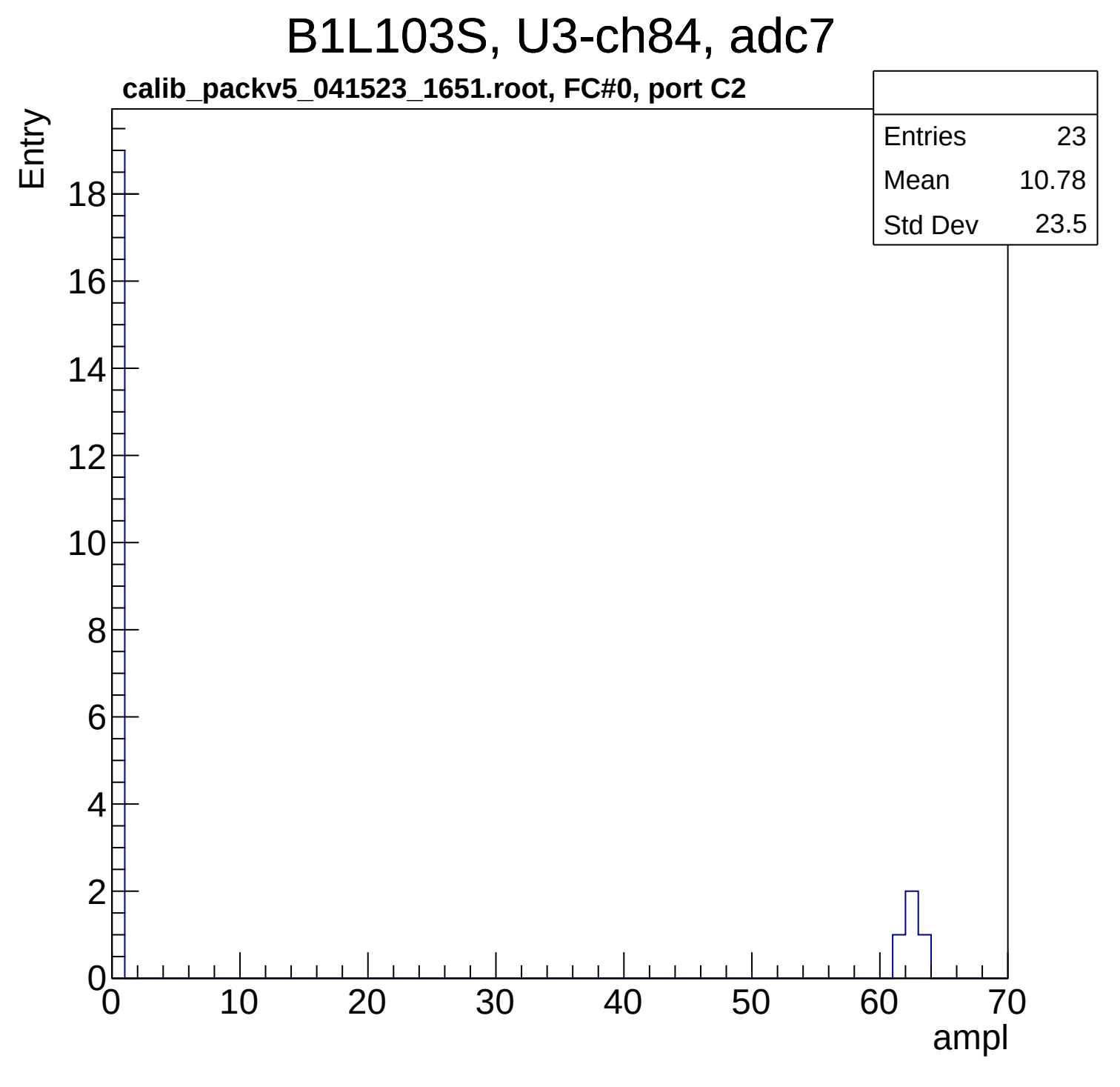
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

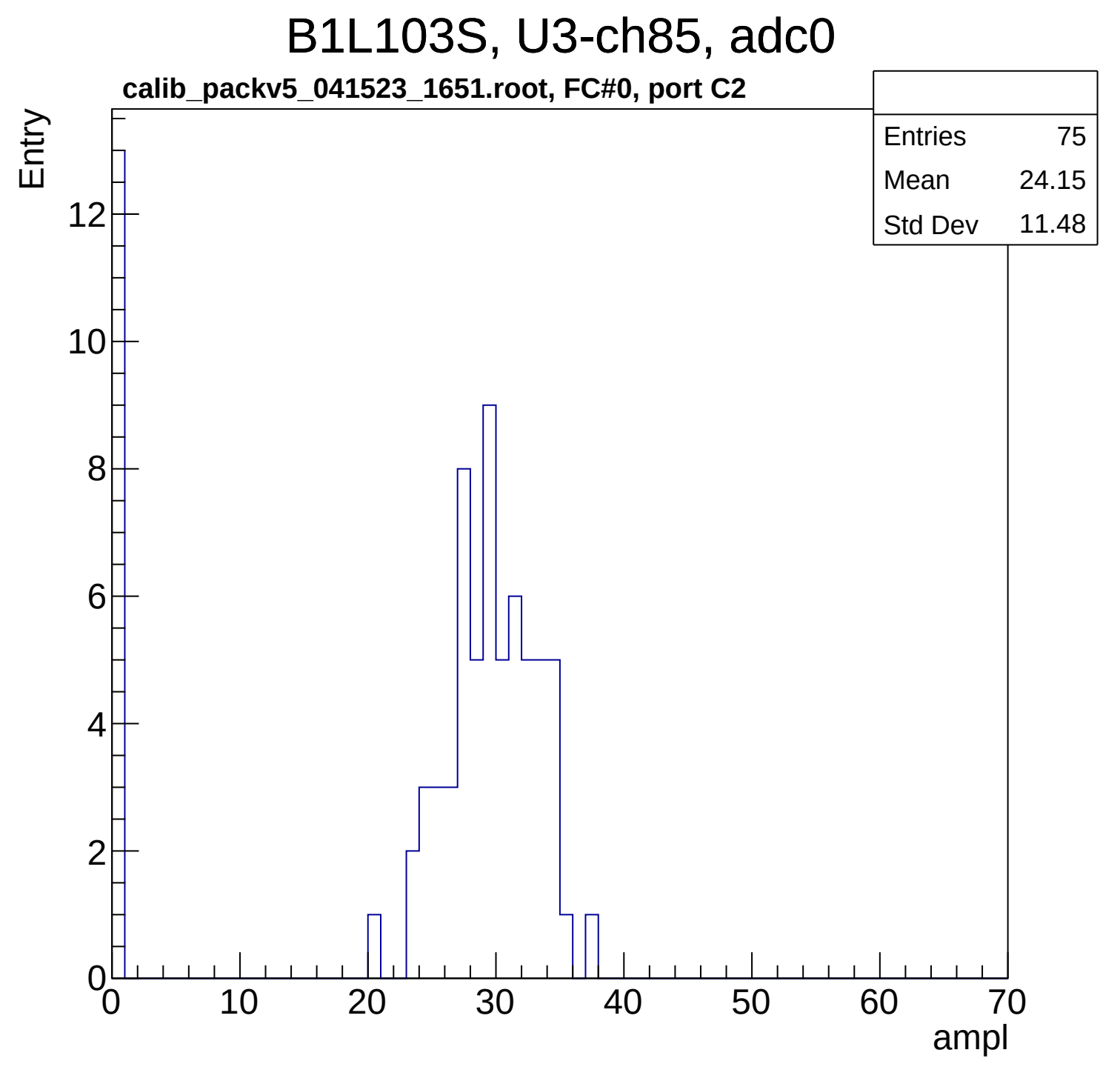

B1L103S, U3-ch84, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 40.73
Std Dev 16.94
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

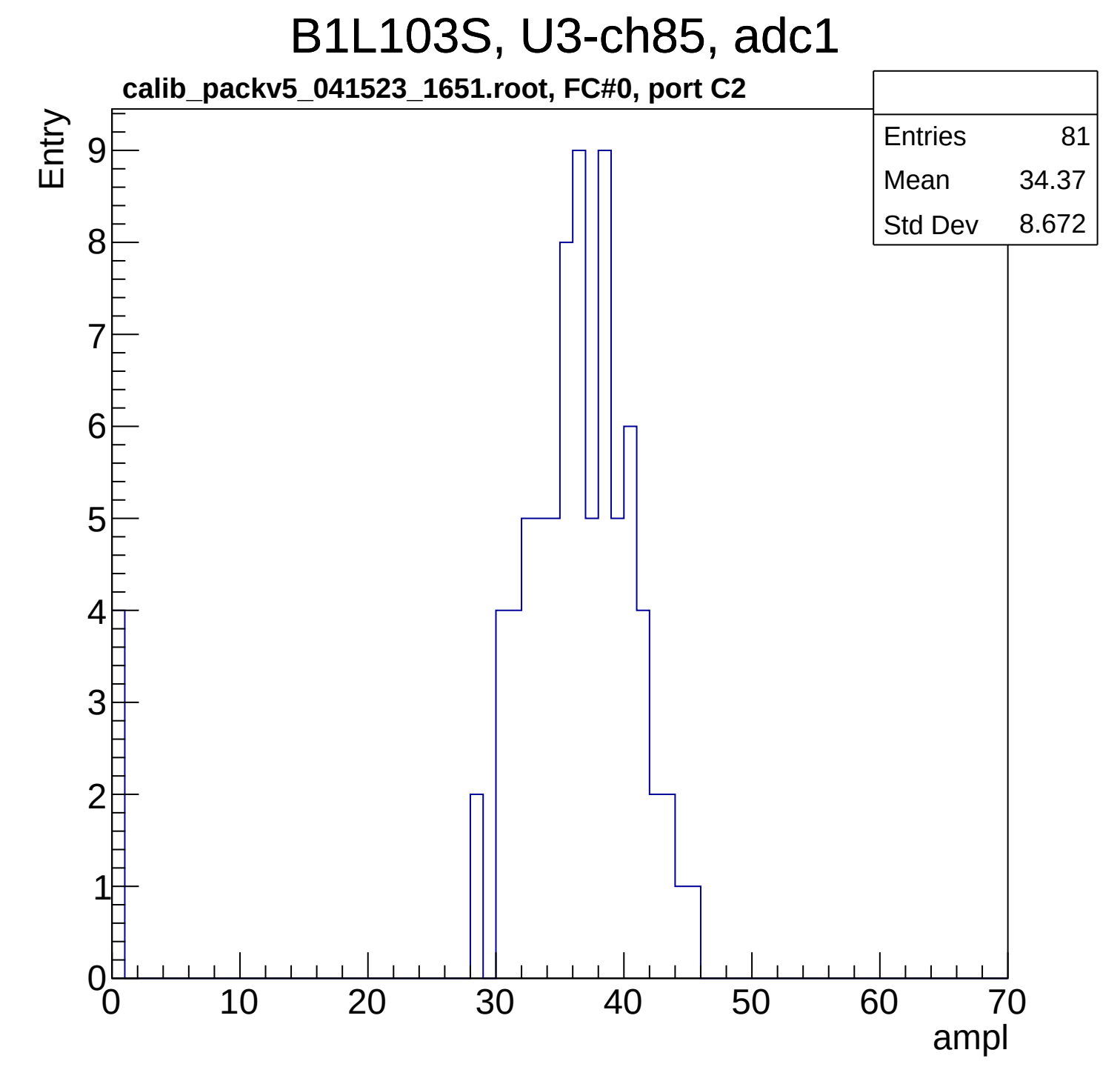

B1L103S, U3-ch84, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 51.29
Std Dev 11.75
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch84, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 56.71
Std Dev 8.451
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch84, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 58.81
Std Dev 11.89
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch84, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 10.78
Std Dev 23.5
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch85, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 24.15
Std Dev 11.48
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch85, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 34.37
Std Dev 8.672
Entry
ampl
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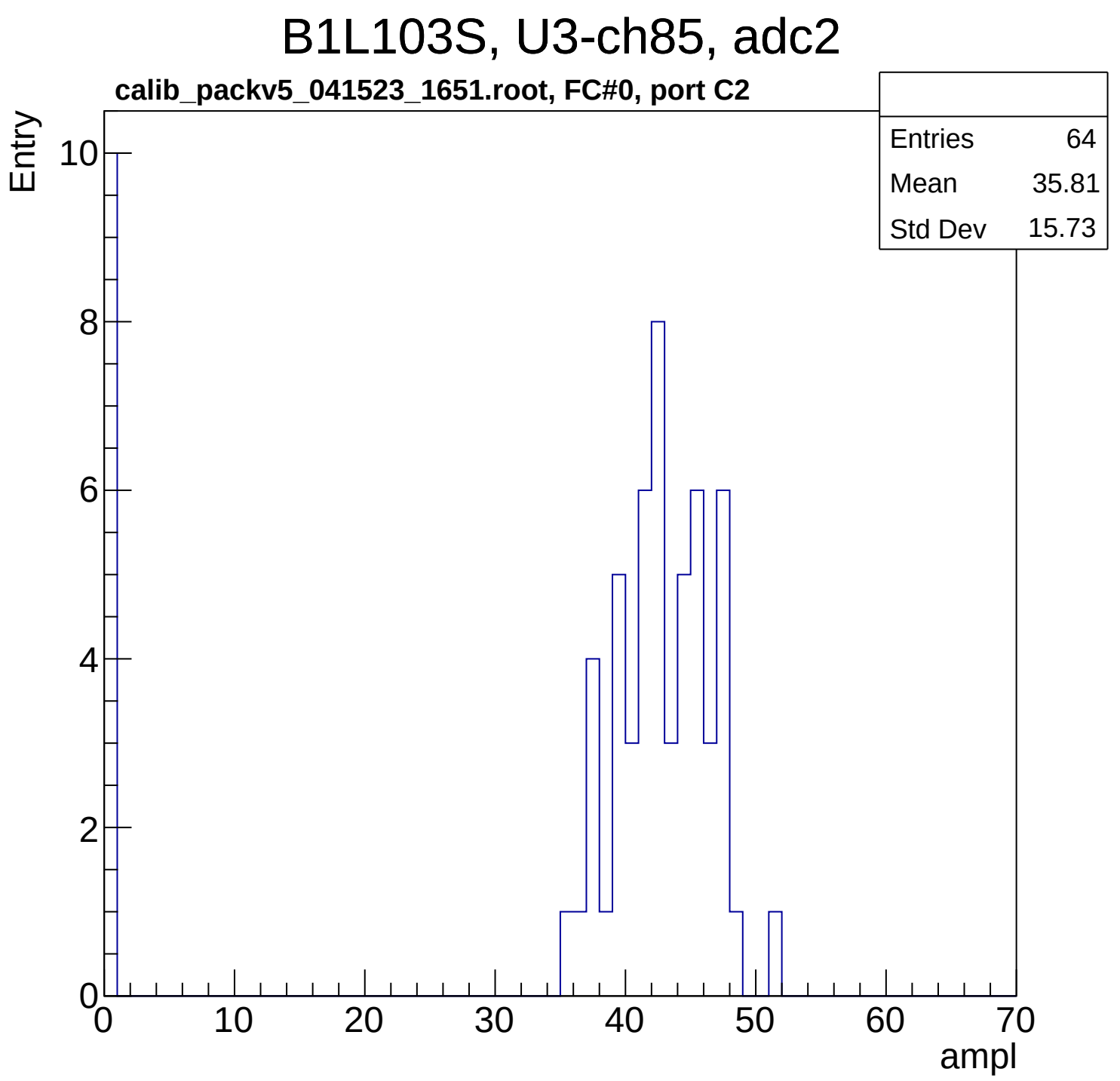
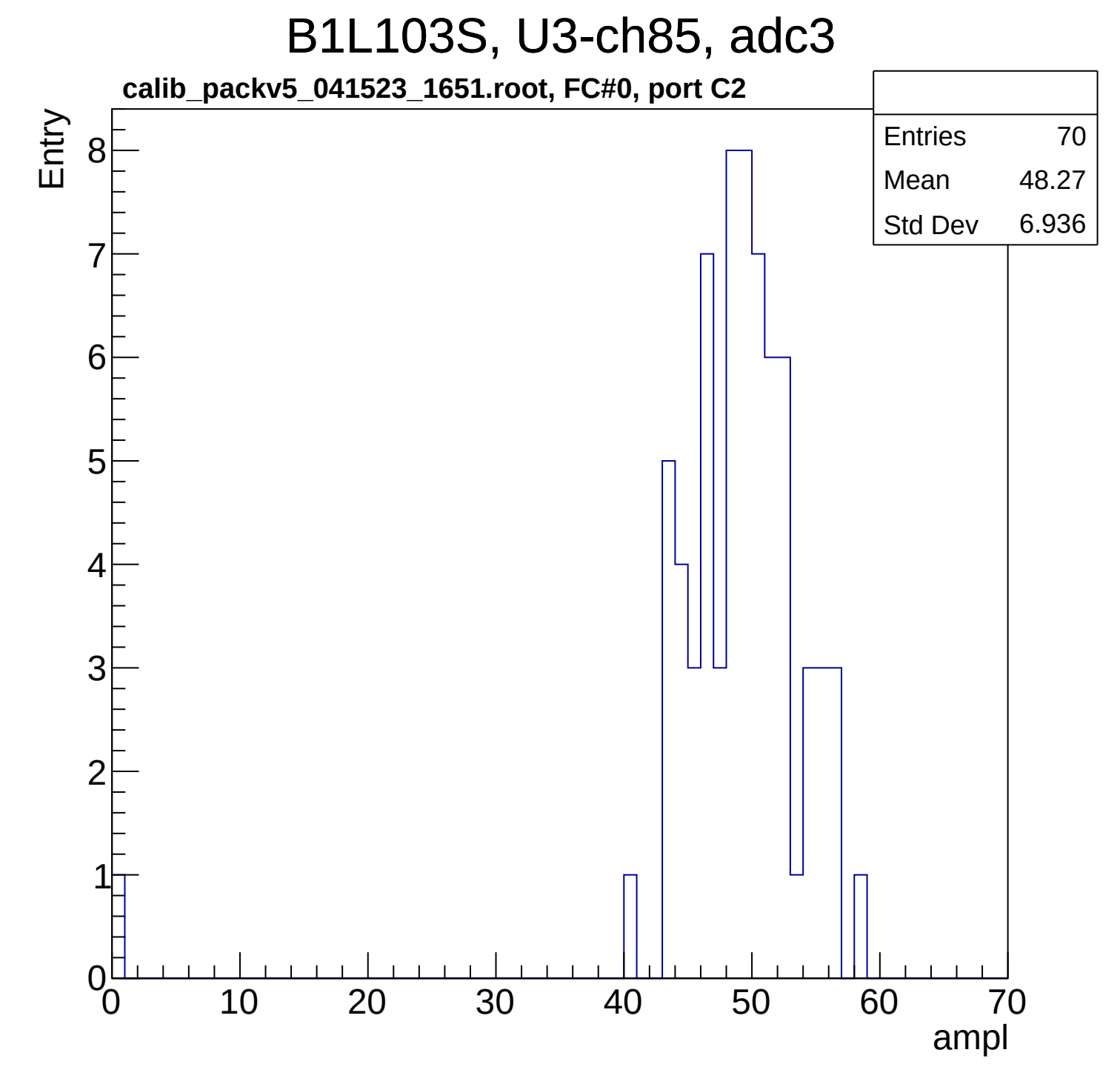
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch85, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 35.81
Std Dev 15.73
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch85, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 48.27
Std Dev 6.936
Entry
ampl
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2
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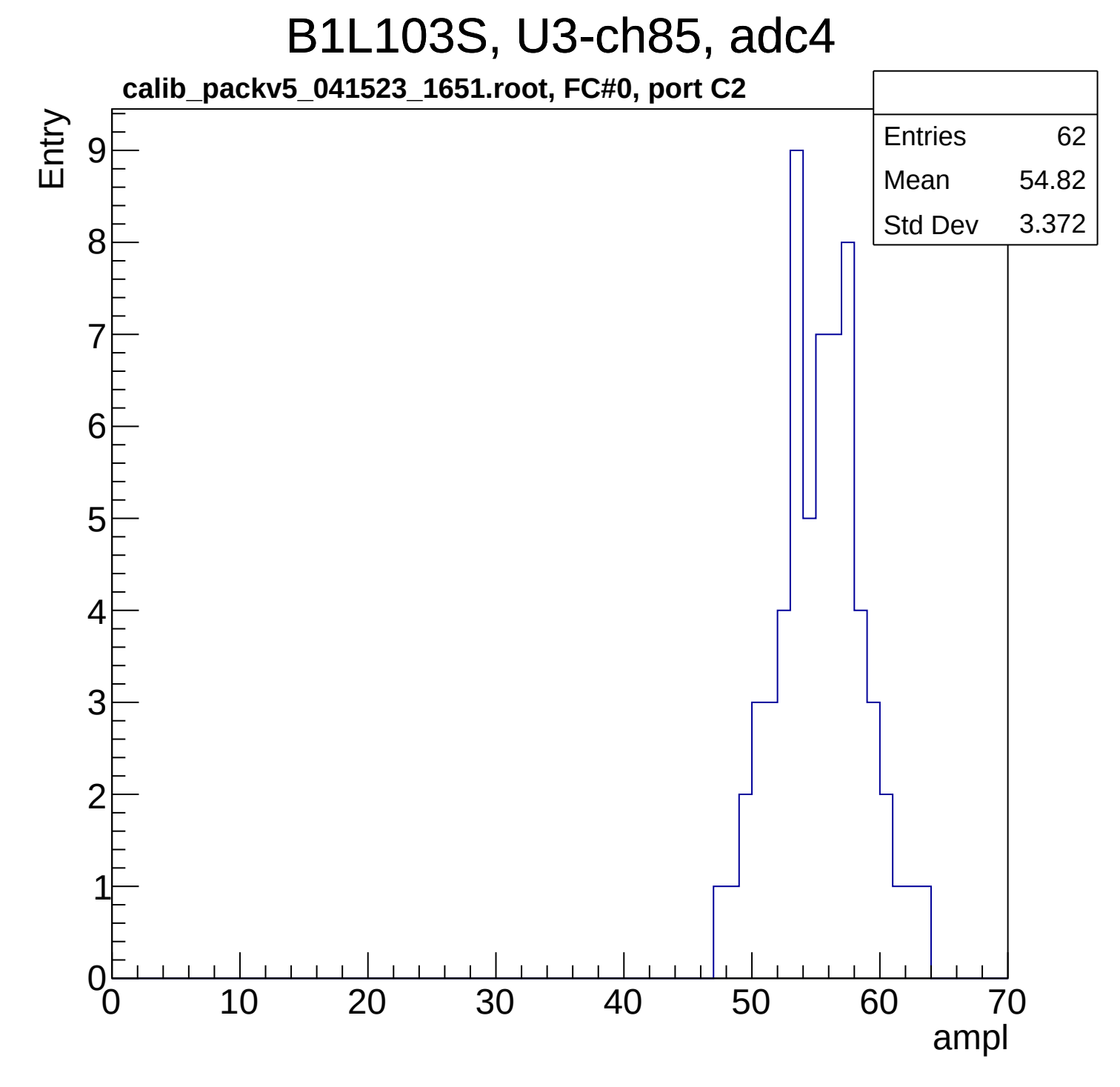
B1L103S, U3-ch85, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 54.82
Std Dev 3.372
Entry
ampl
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6
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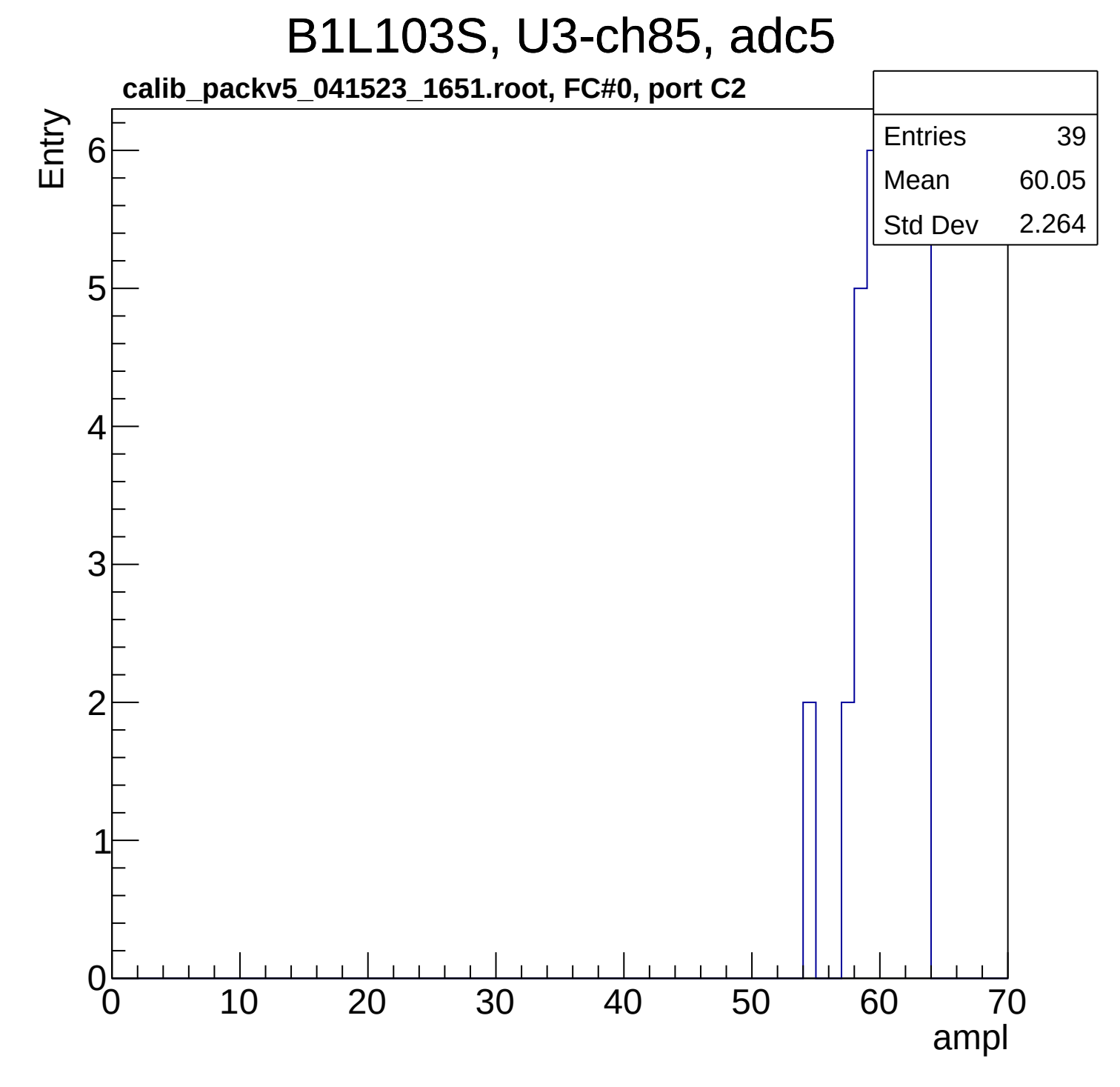
B1L103S, U3-ch85, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 60.05
Std Dev 2.264
Entry
ampl
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3
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0
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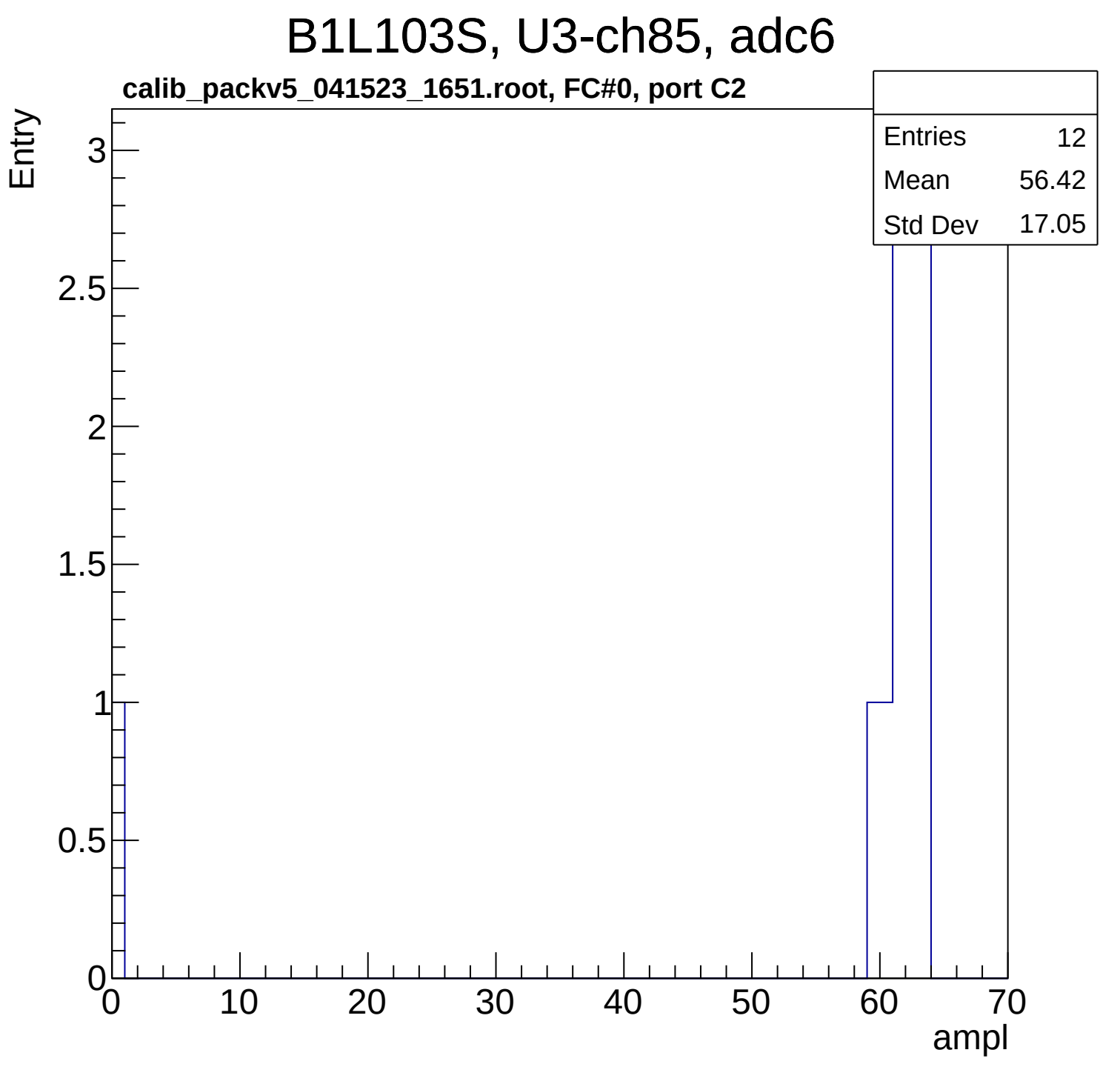
B1L103S, U3-ch85, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 56.42
Std Dev 17.05
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
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40
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60
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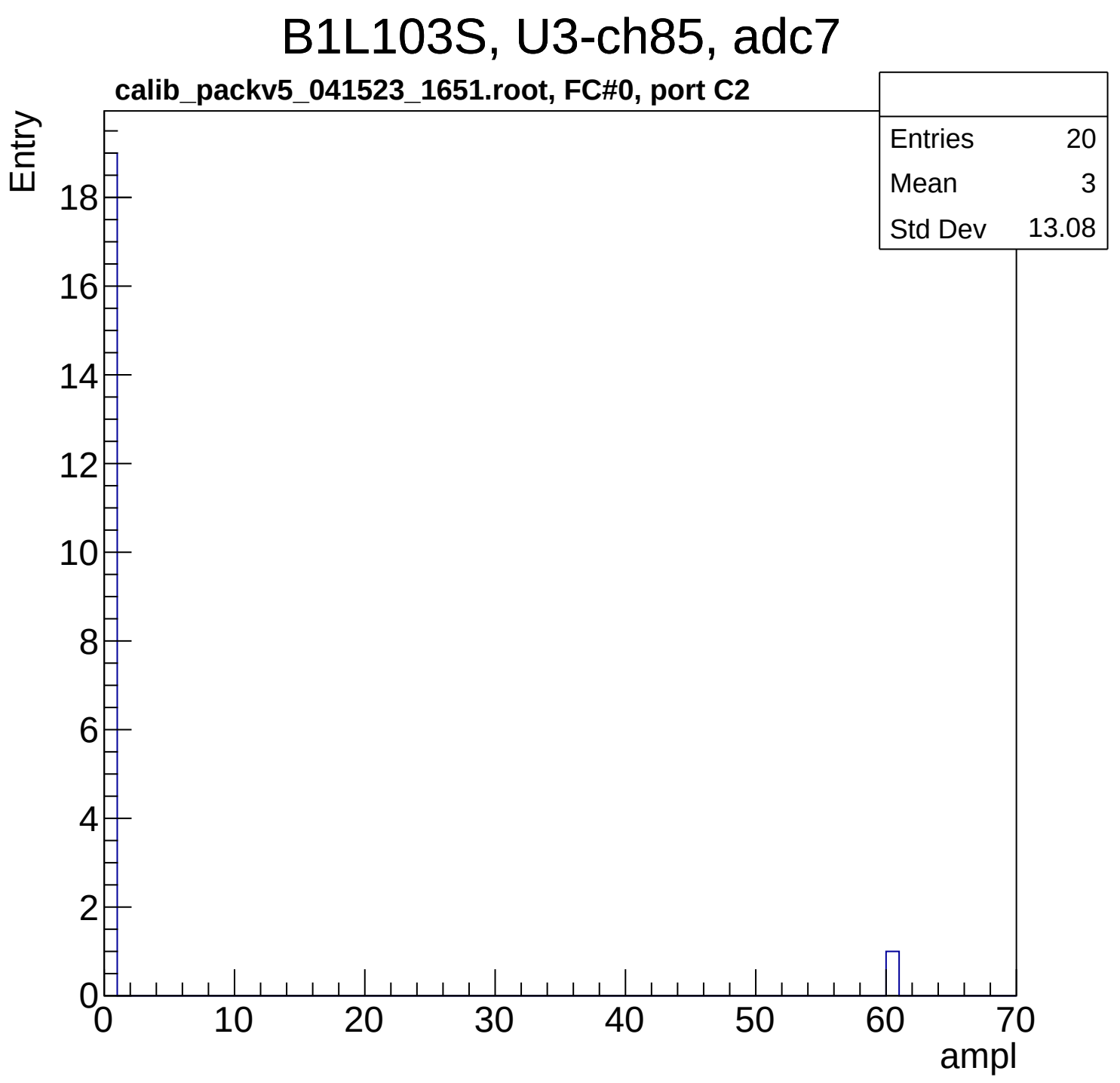
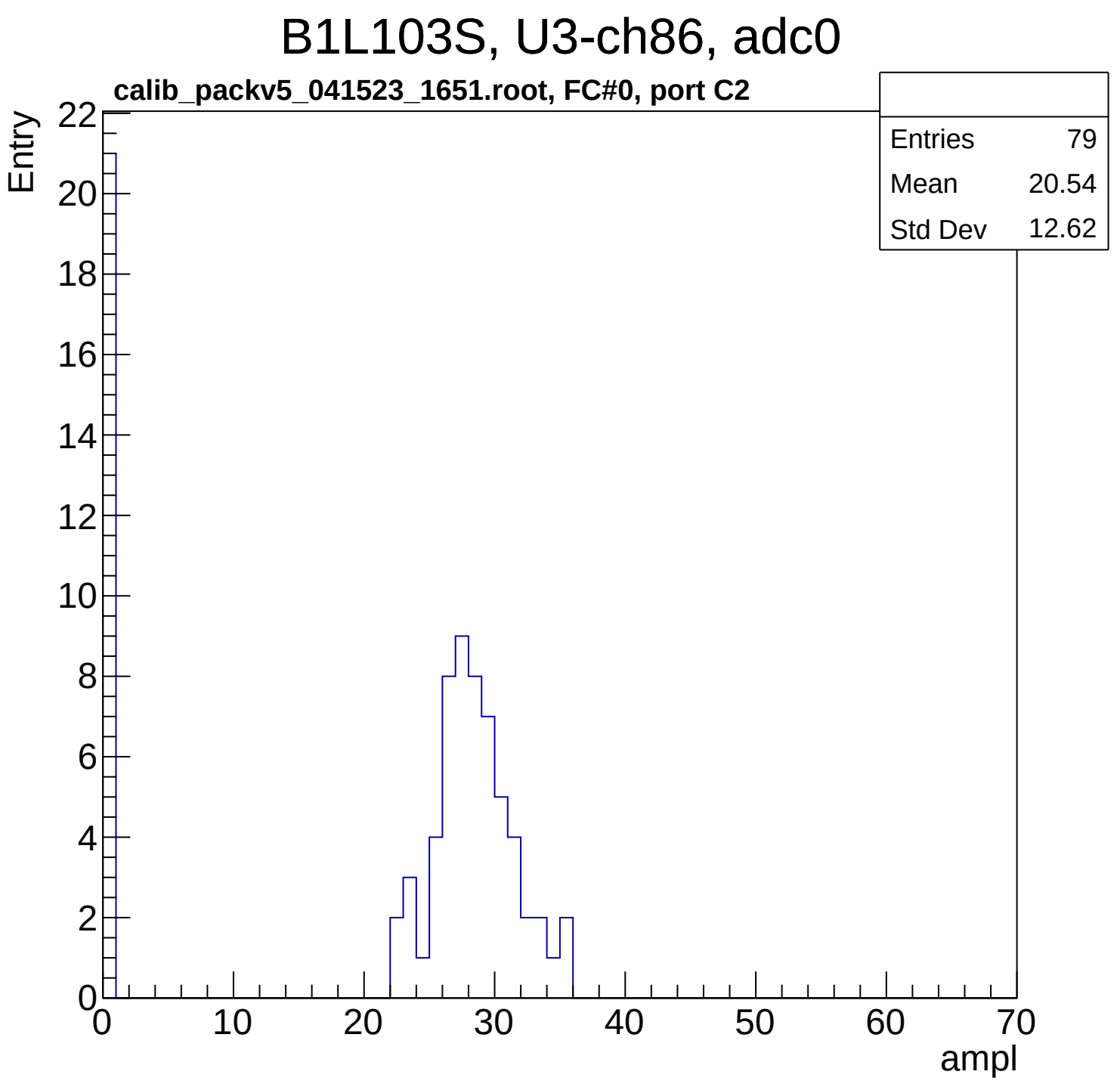

B1L103S, U3-ch85, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3
Std Dev 13.08
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch86, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 20.54
Std Dev 12.62
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
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40
50
60
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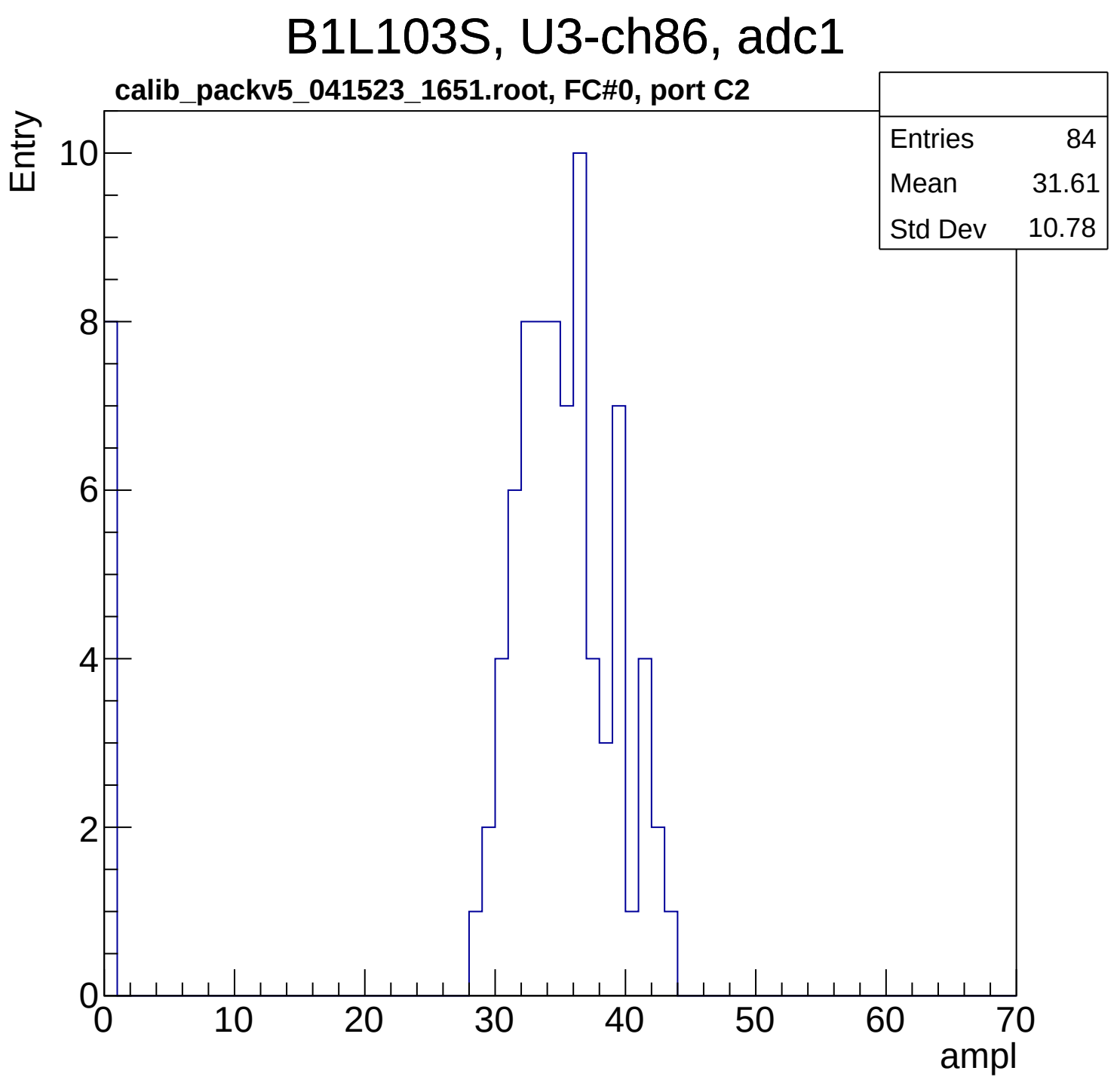
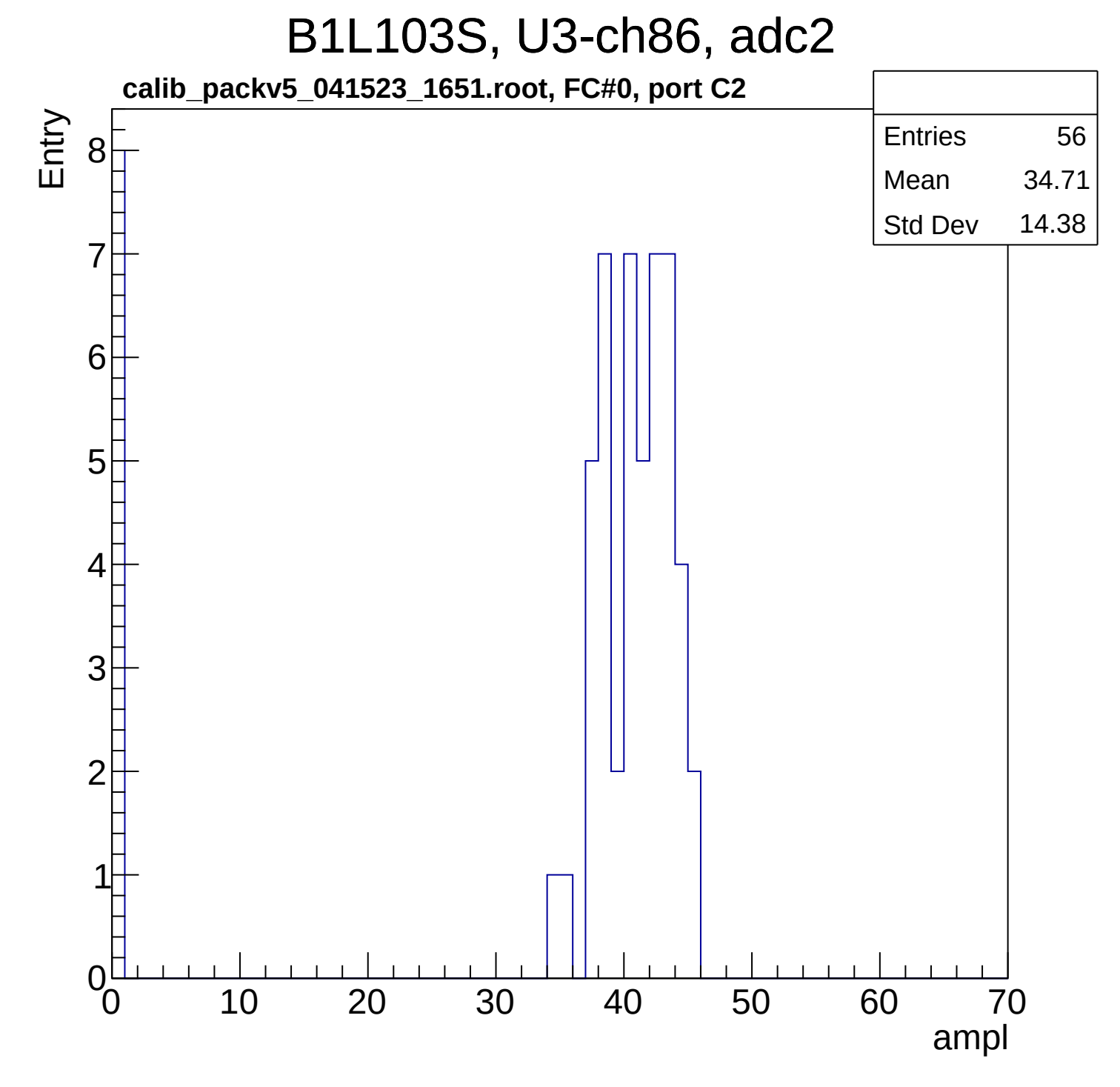

B1L103S, U3-ch86, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 31.61
Std Dev 10.78
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch86, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 34.71
Std Dev 14.38
Entry
0
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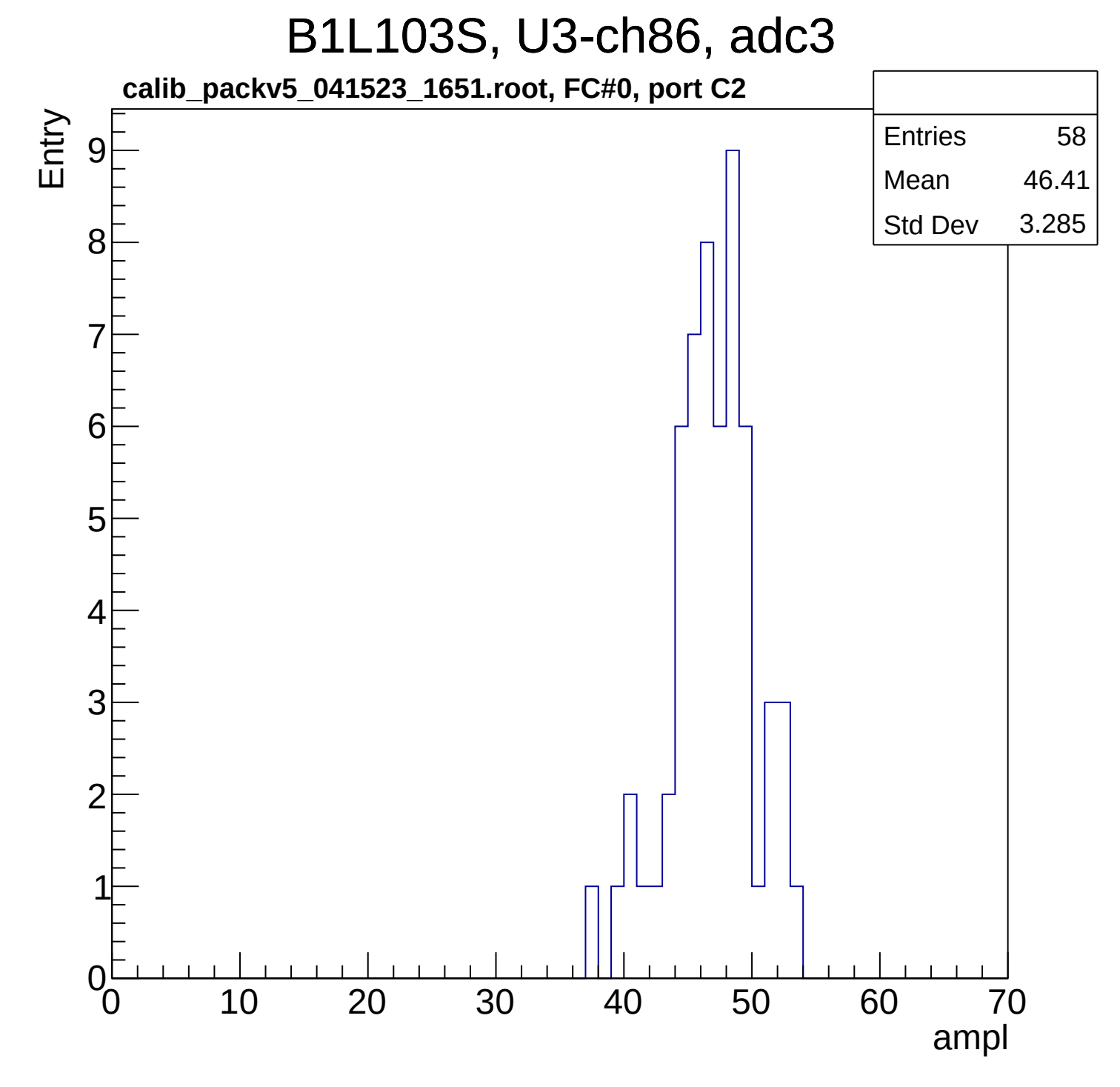
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch86, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 46.41
Std Dev 3.285
Entry
ampl
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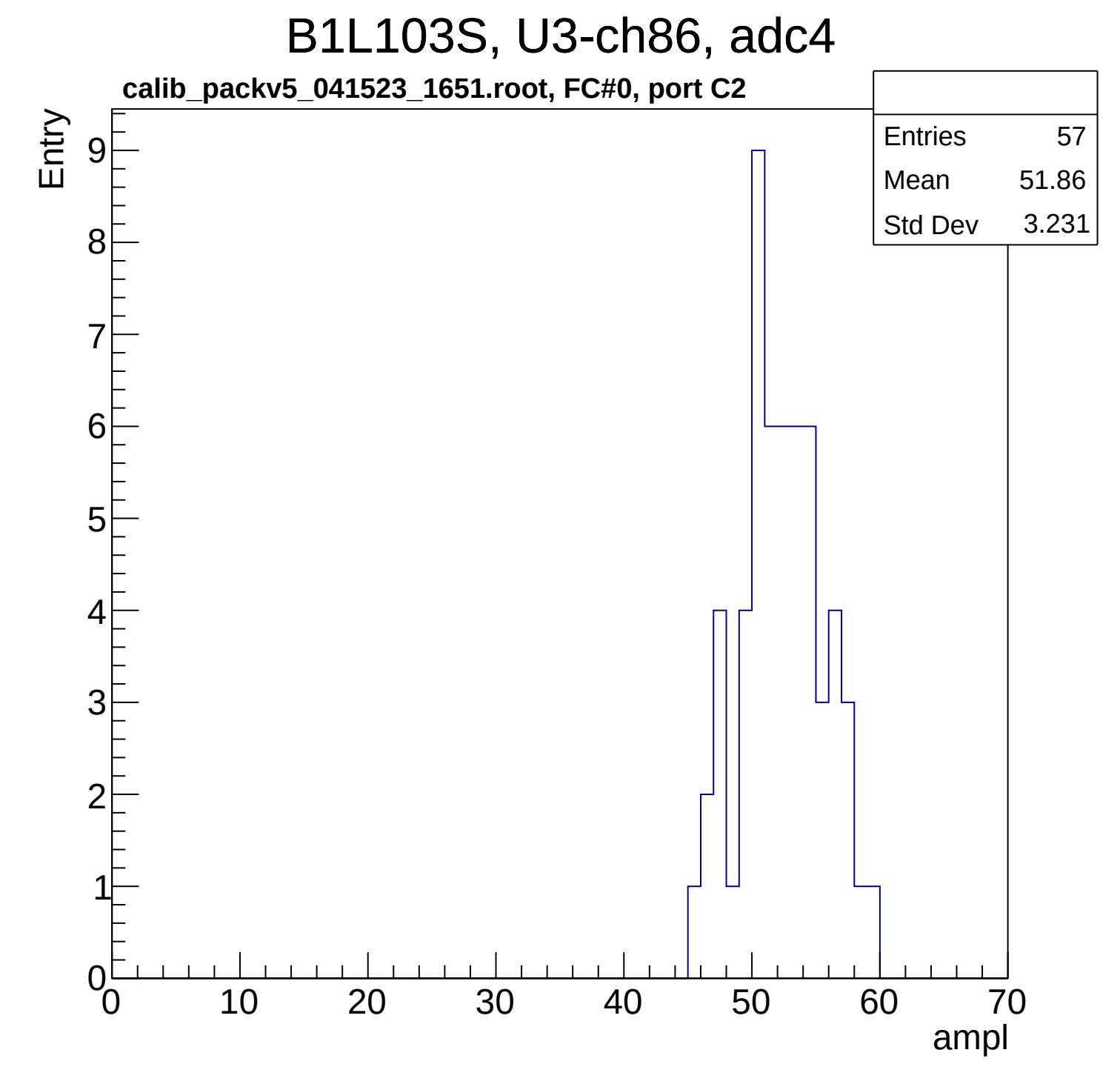
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch86, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 51.86
Std Dev 3.231
Entry
ampl
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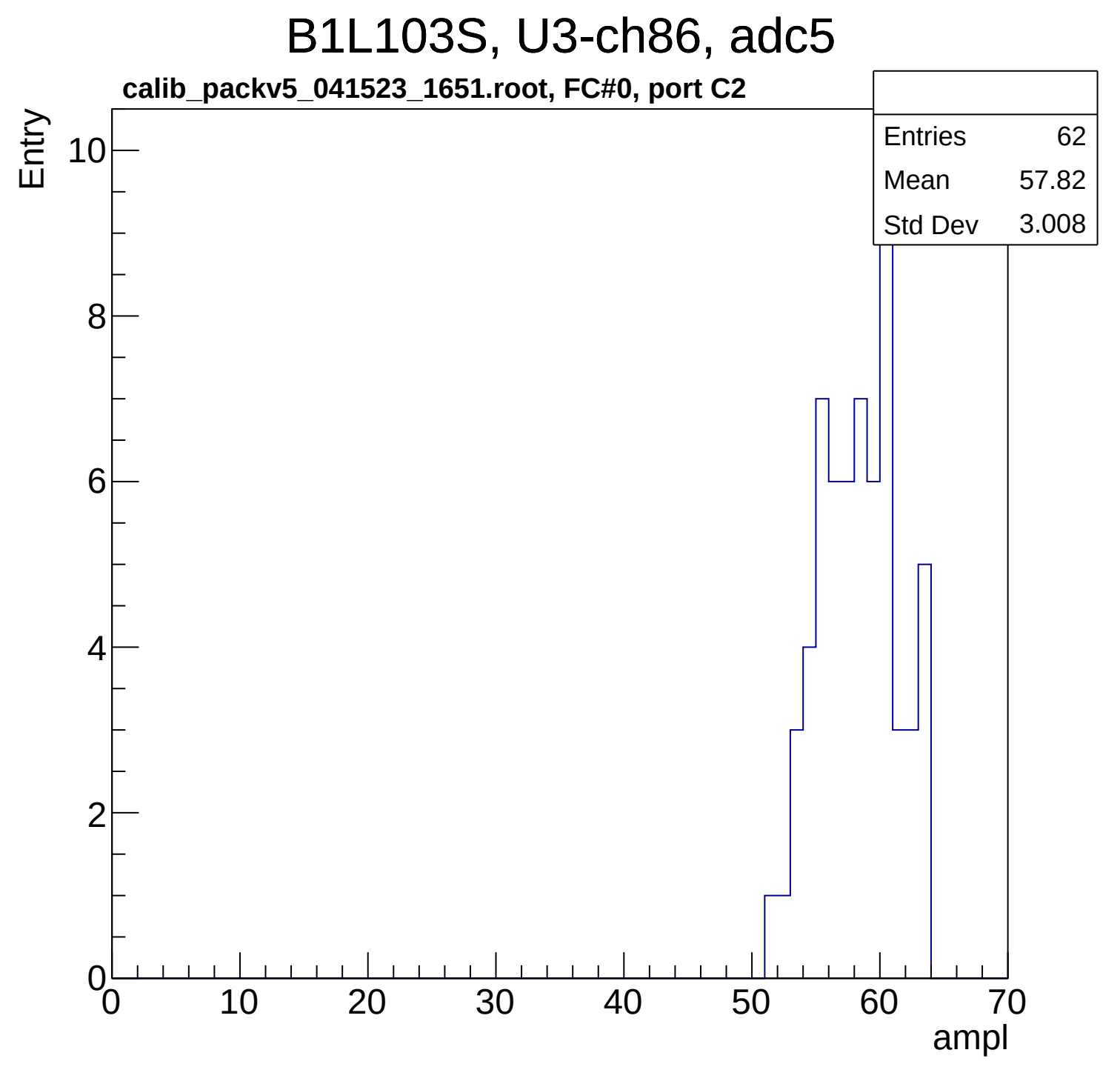
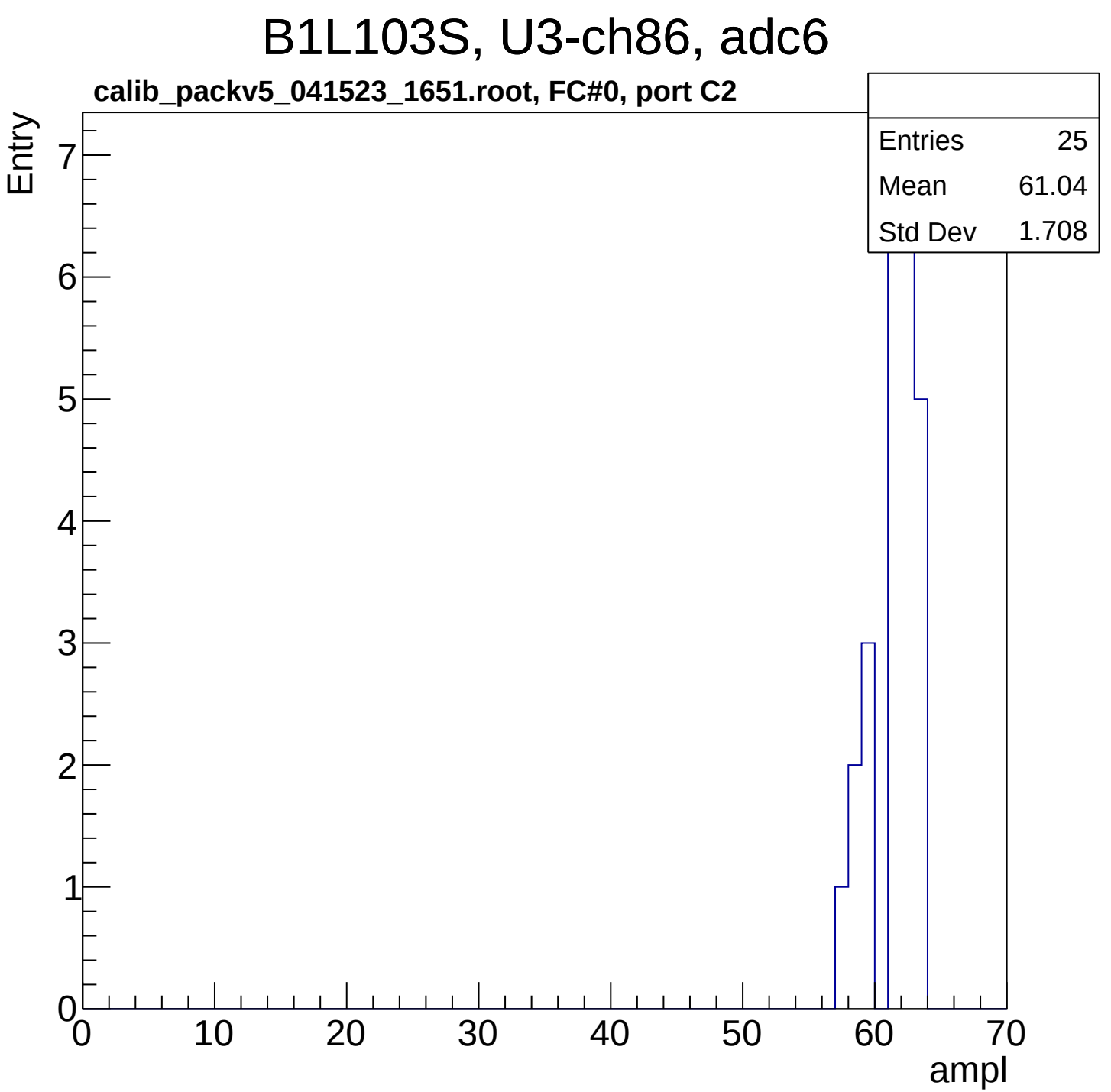
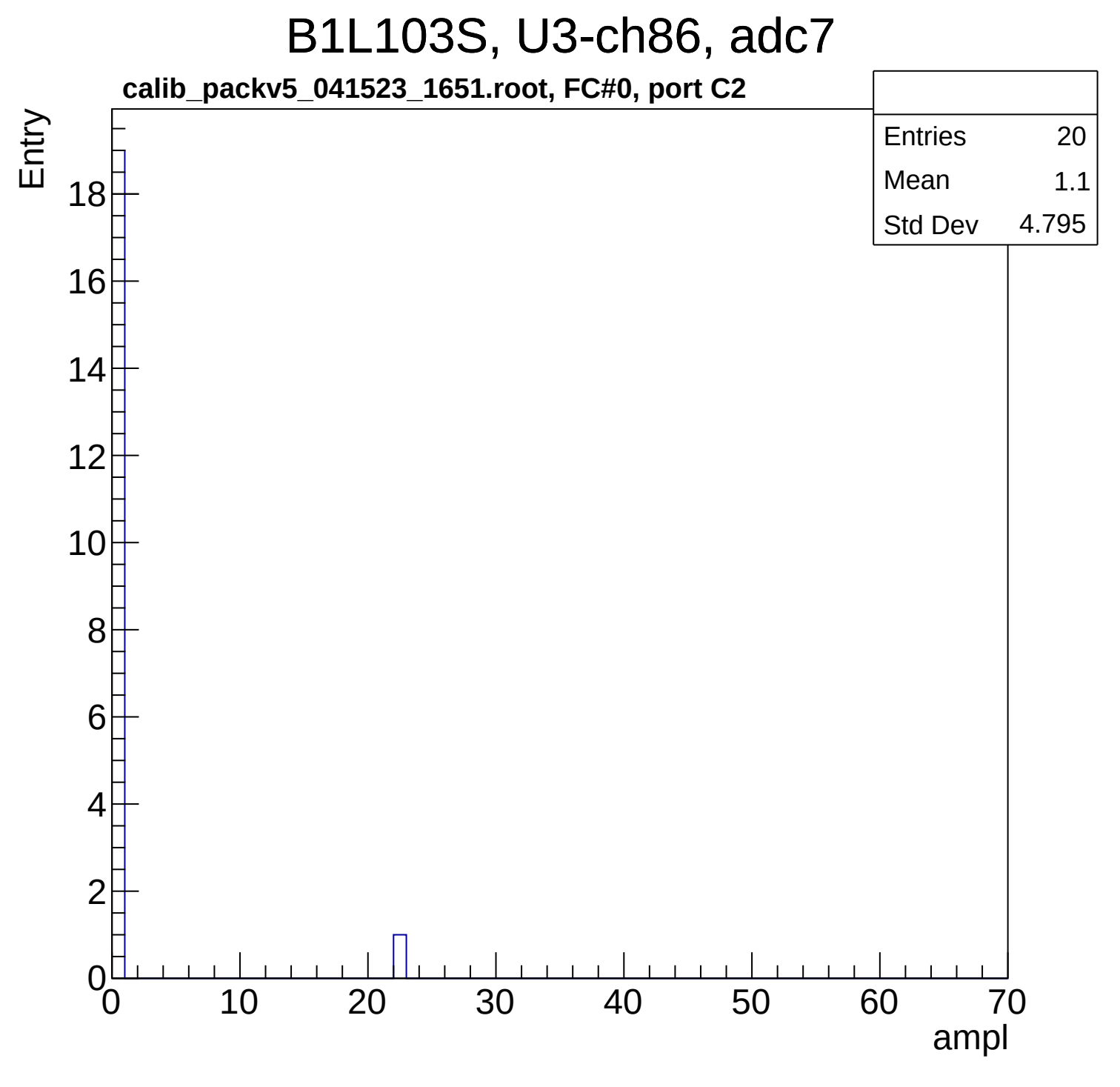
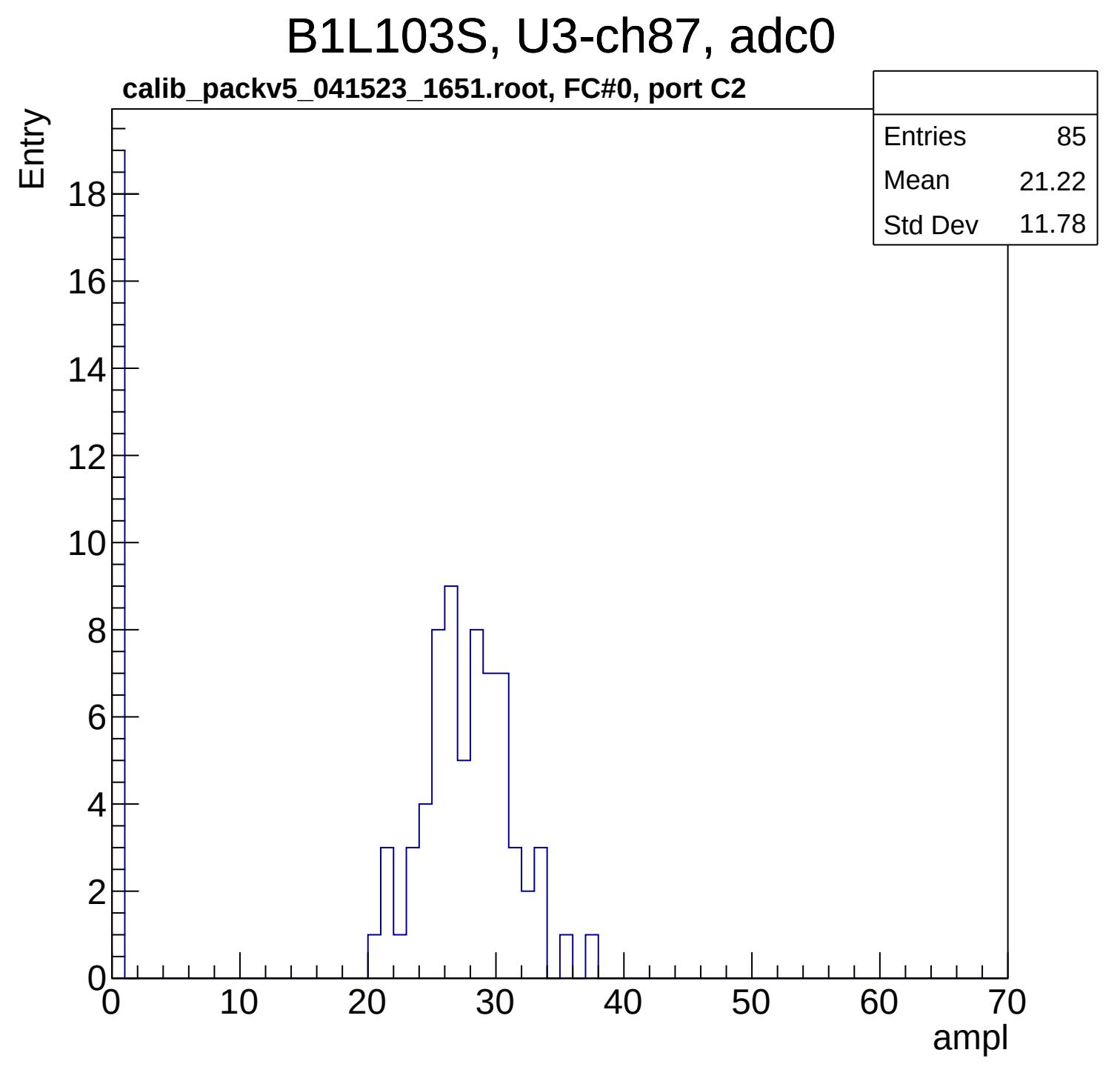
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch86, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 57.82
Std Dev 3.008
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U3-ch86, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 61.04
Std Dev 1.708
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch86, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 1.1
Std Dev 4.795
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch87, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 21.22
Std Dev 11.78
Entry
ampl
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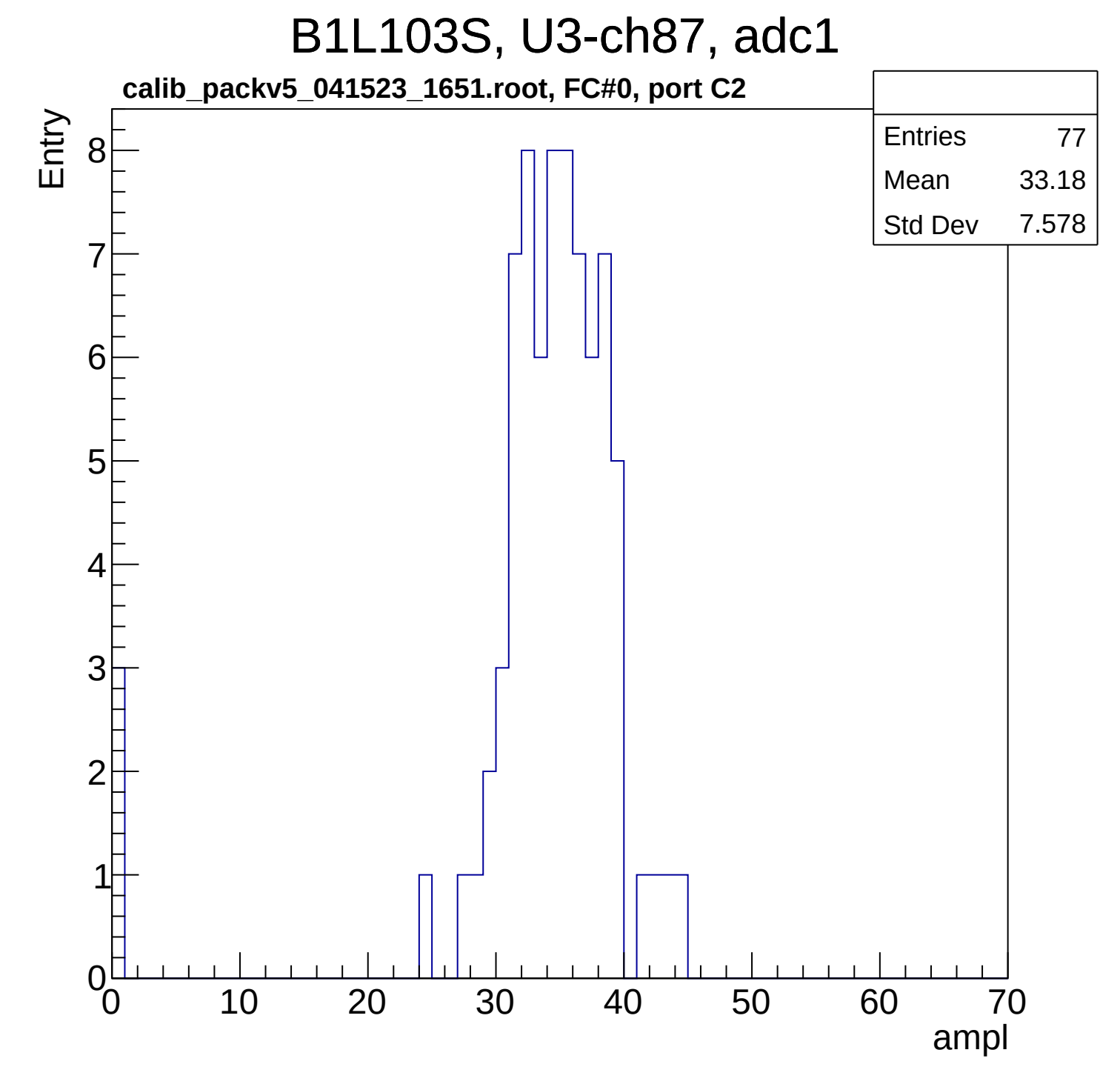
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L103S, U3-ch87, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 33.18
Std Dev 7.578
Entry
ampl
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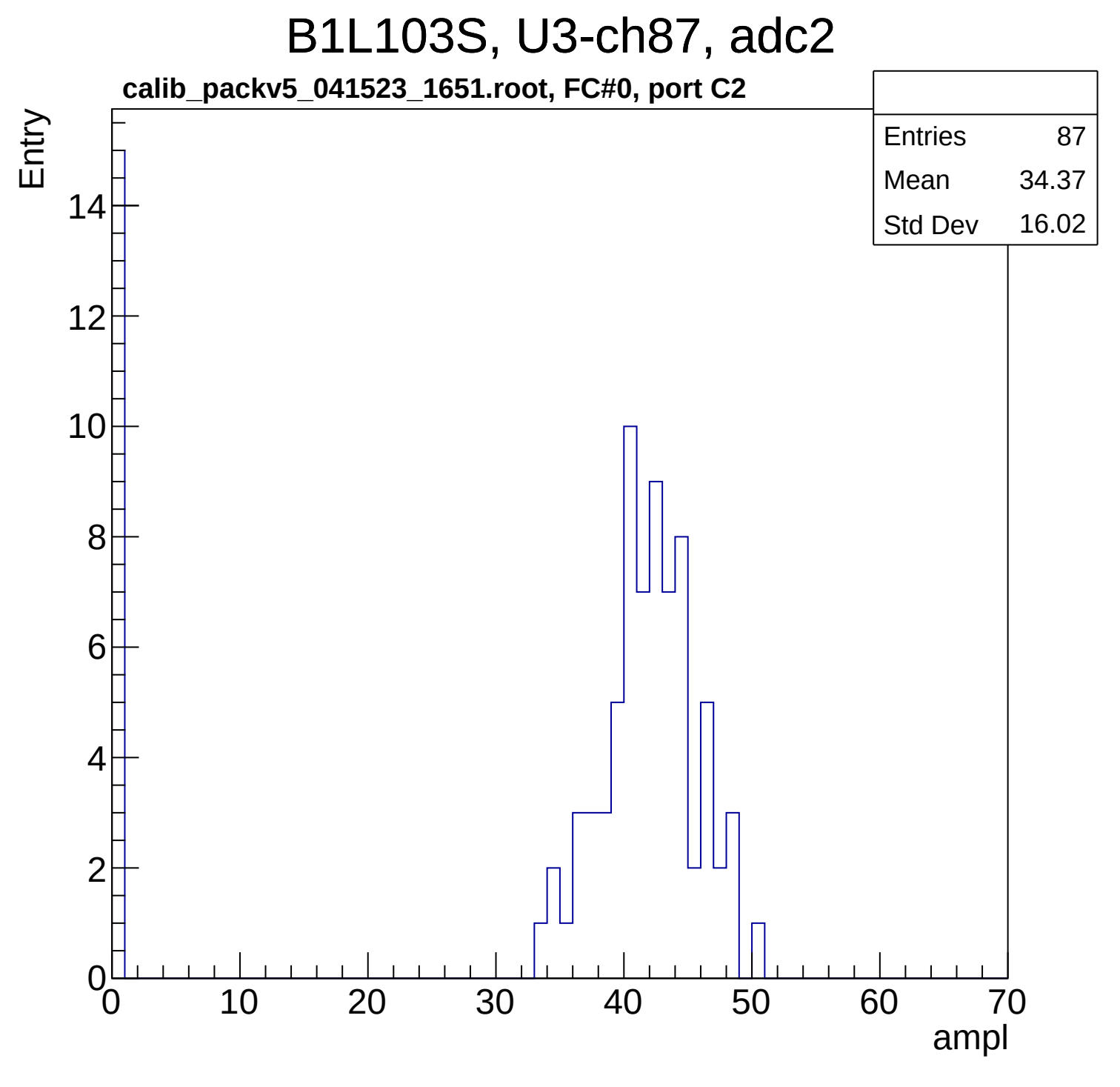
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch87, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 34.37
Std Dev 16.02
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
30
40
50
60
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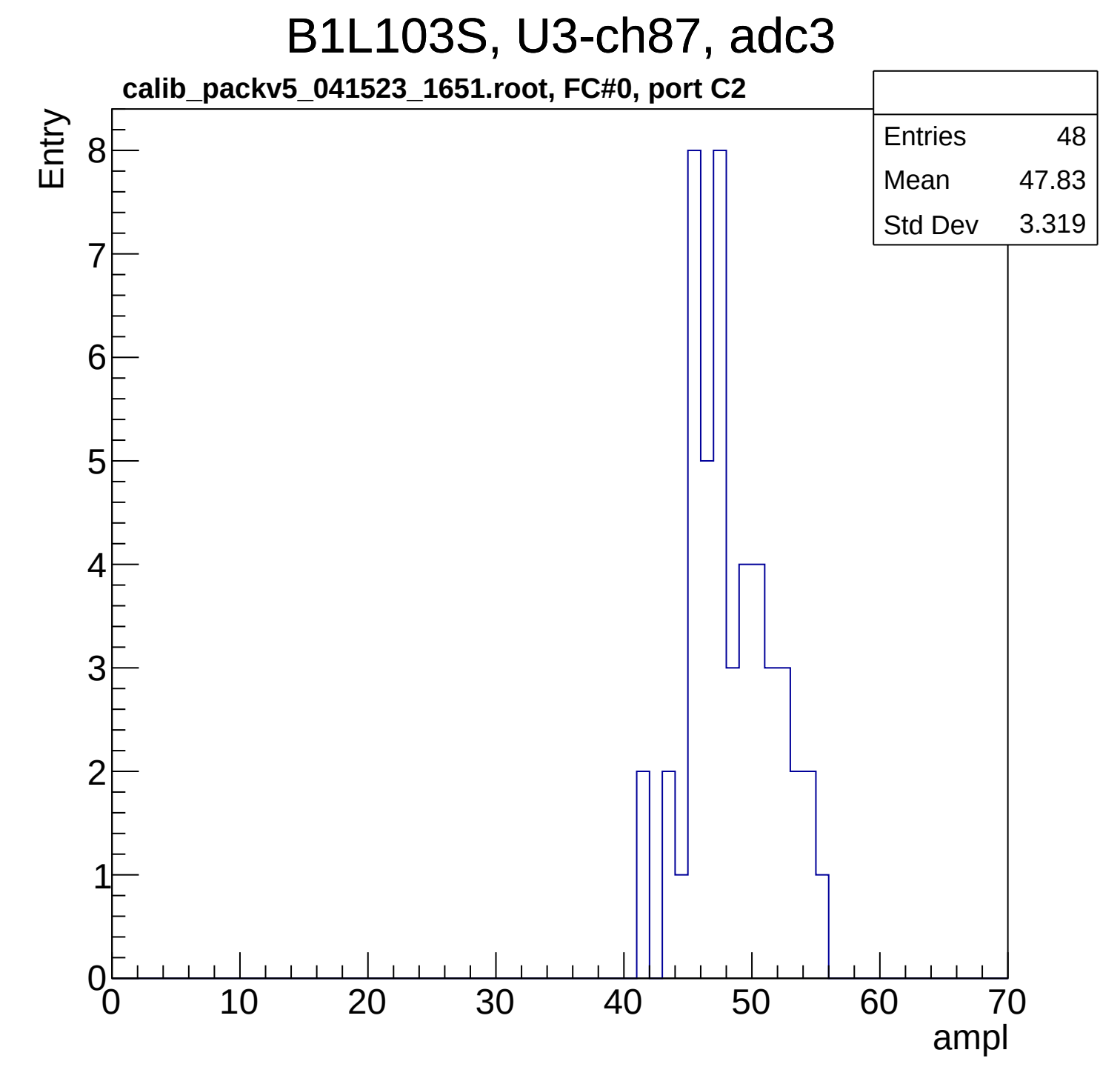
B1L103S, U3-ch87, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 47.83
Std Dev 3.319
Entry
ampl
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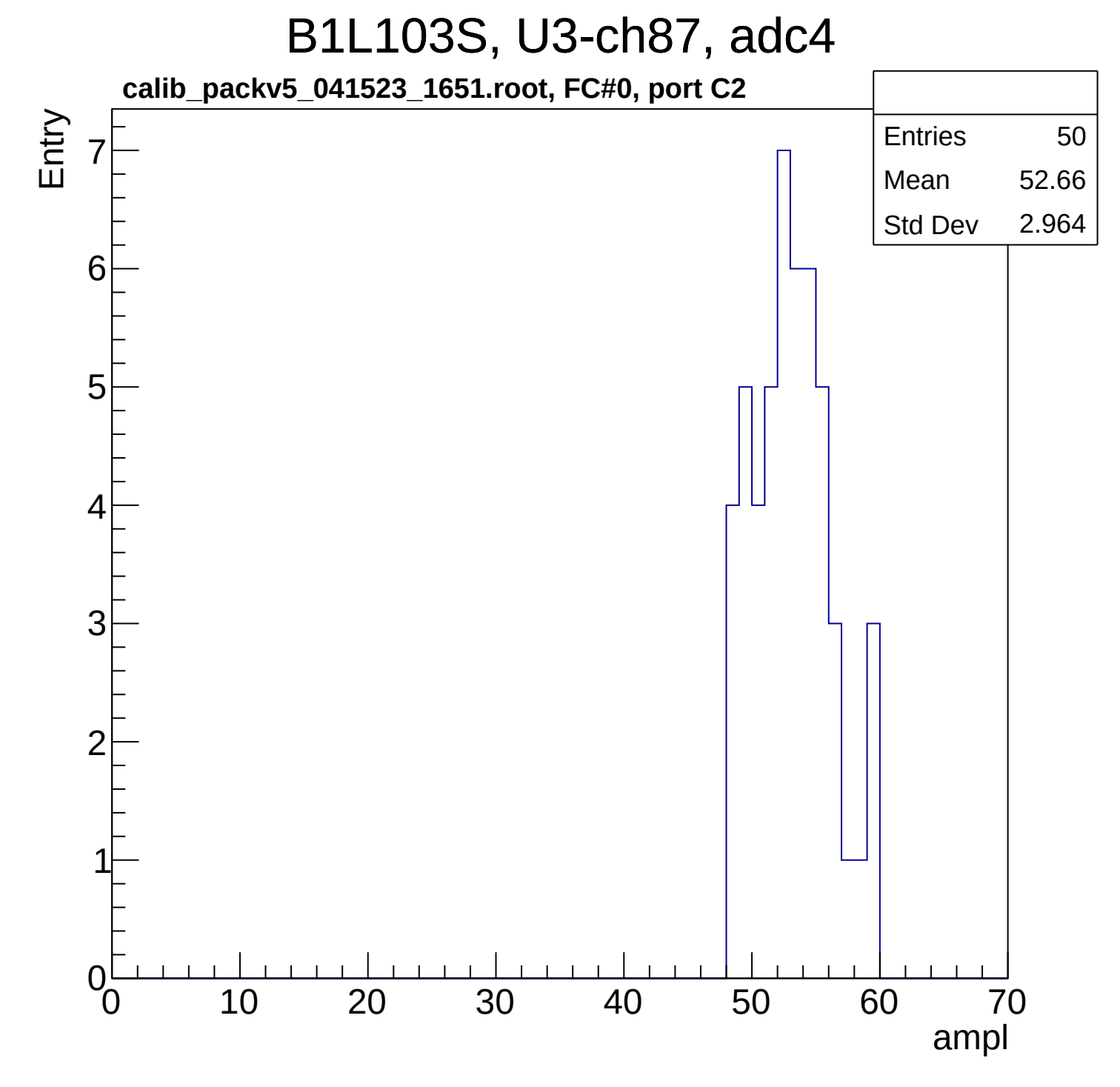
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch87, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 52.66
Std Dev 2.964
Entry
ampl
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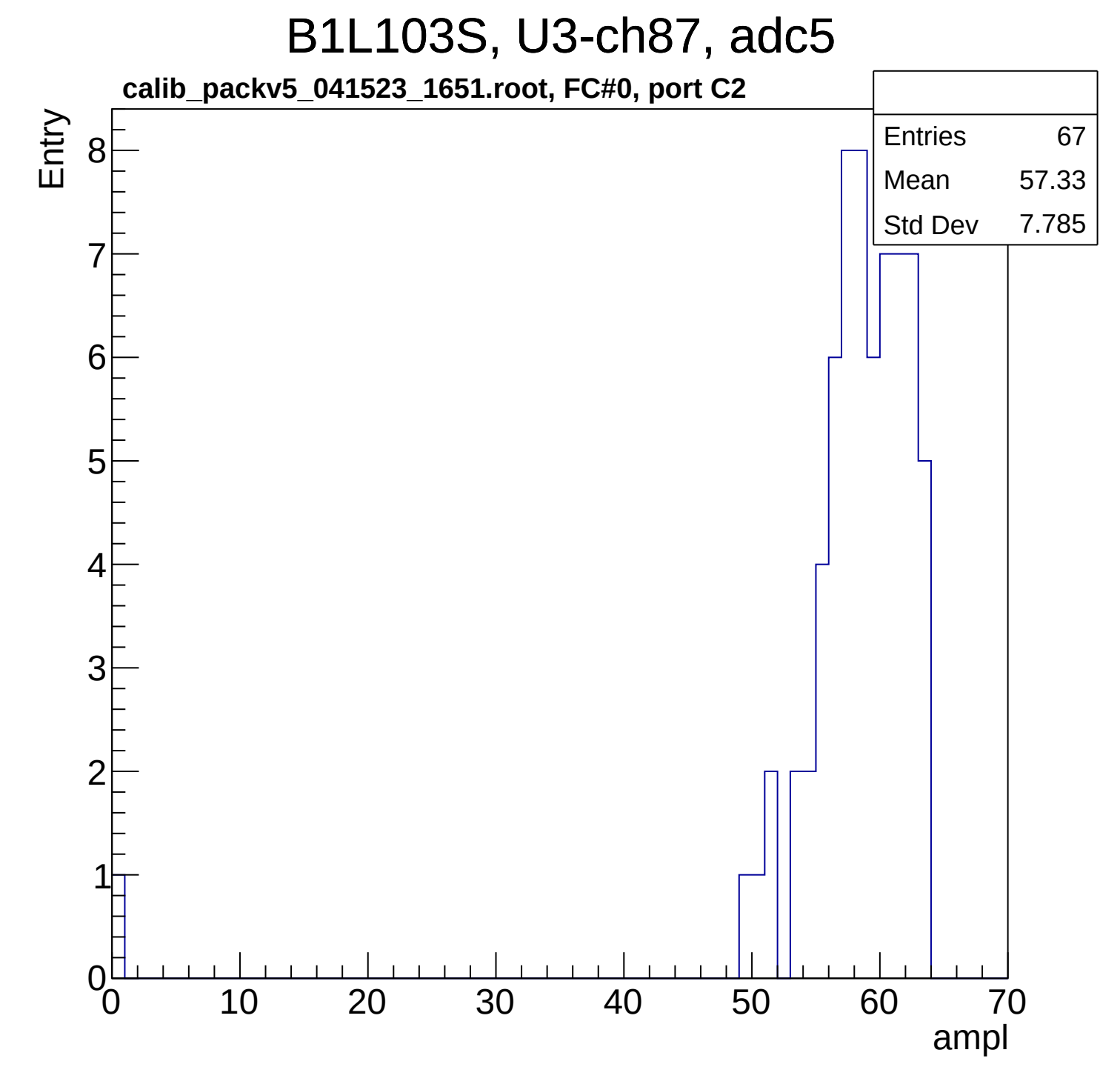
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch87, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 57.33
Std Dev 7.785
Entry
ampl
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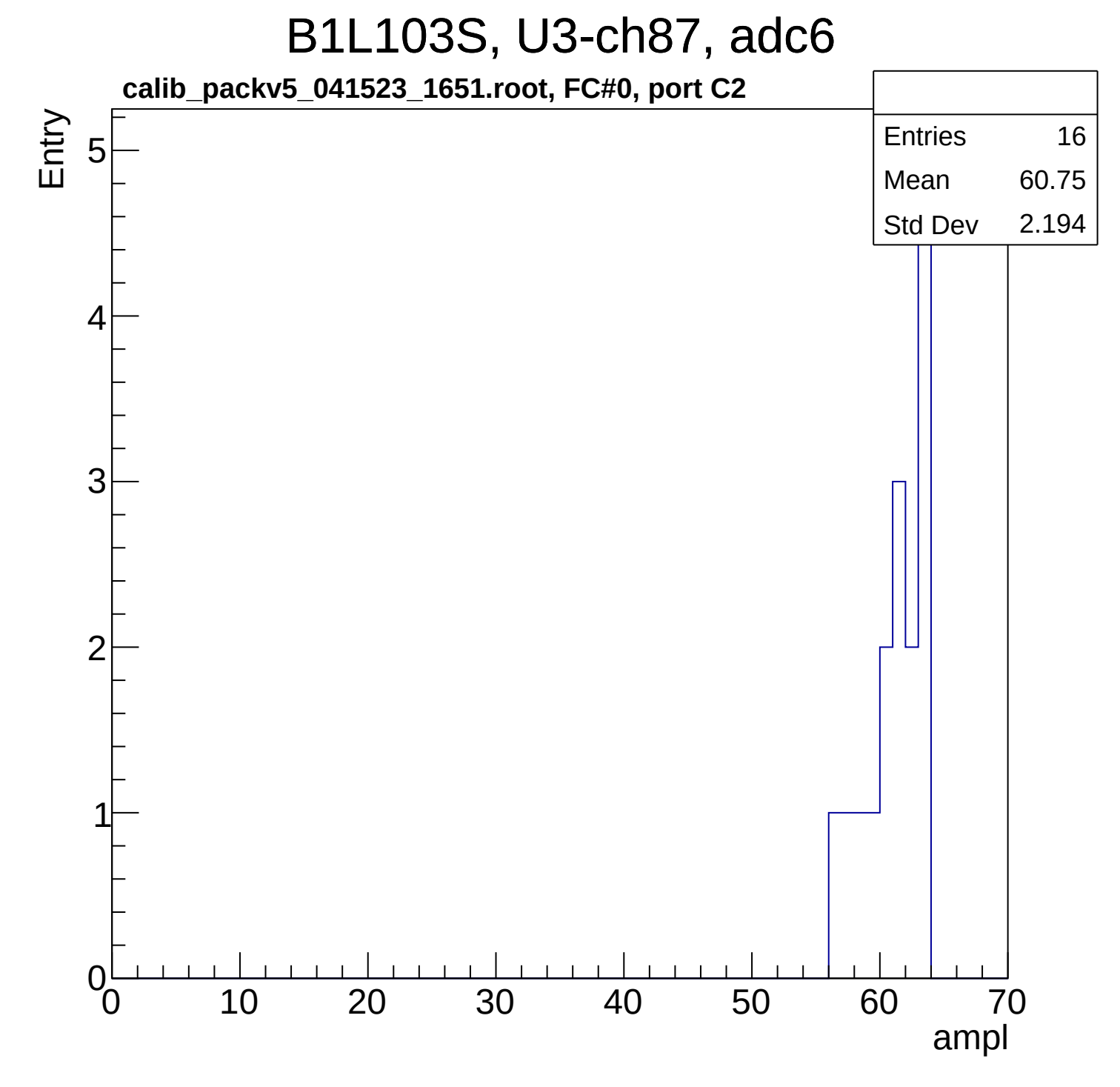
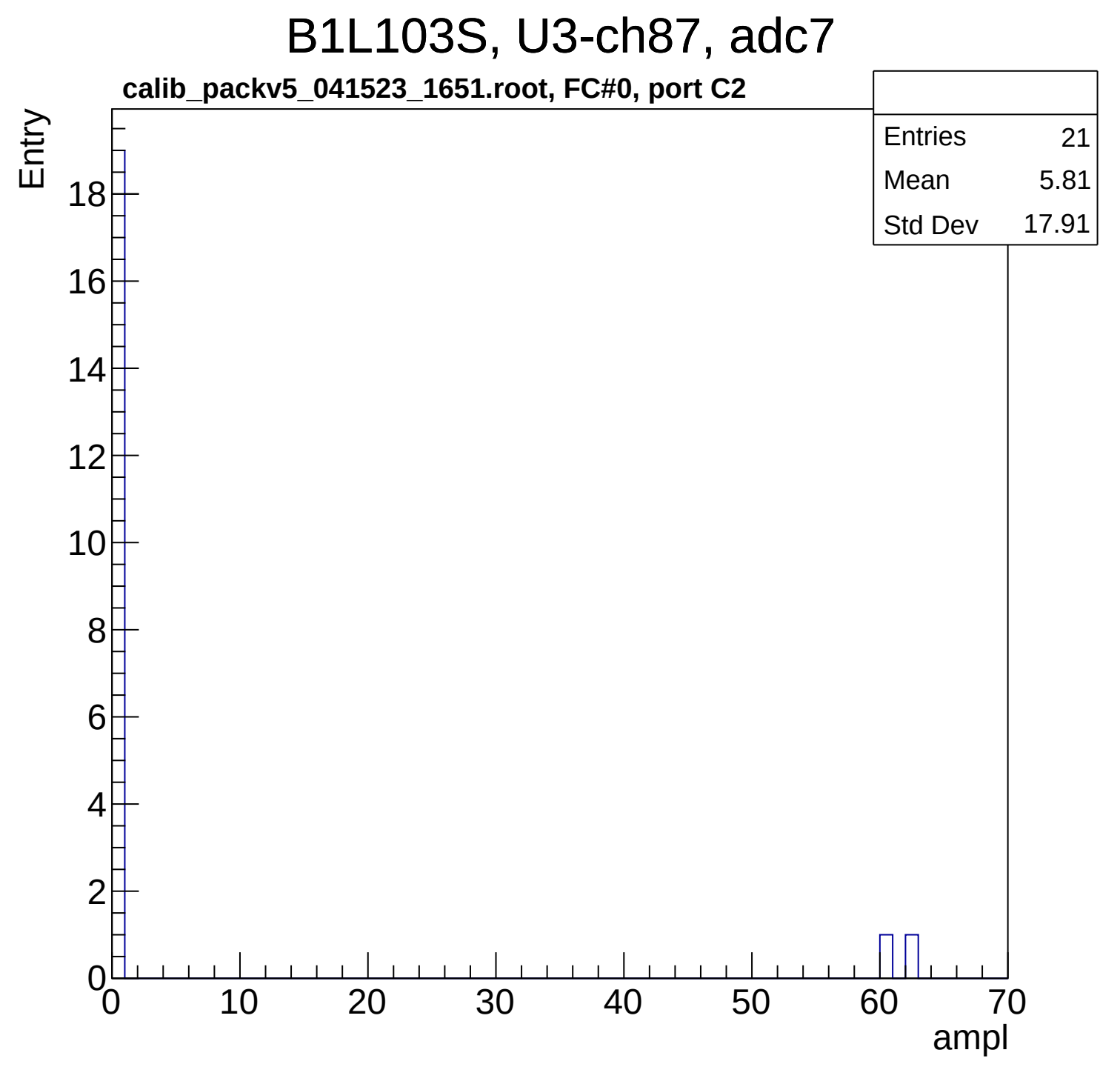
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch87, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 60.75
Std Dev 2.194
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch87, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.81
Std Dev 17.91
Entry
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2
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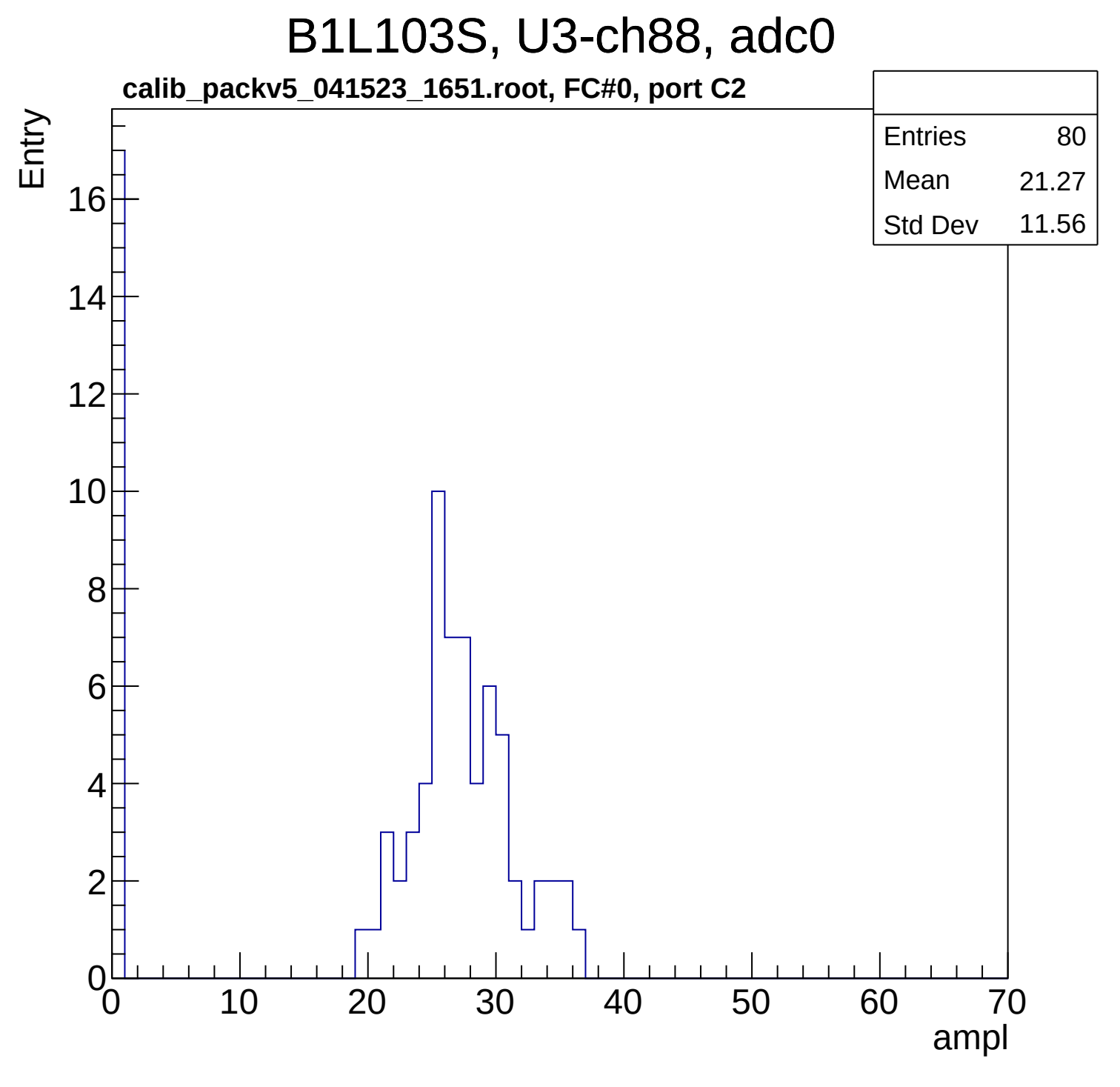
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch88, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 21.27
Std Dev 11.56
Entry
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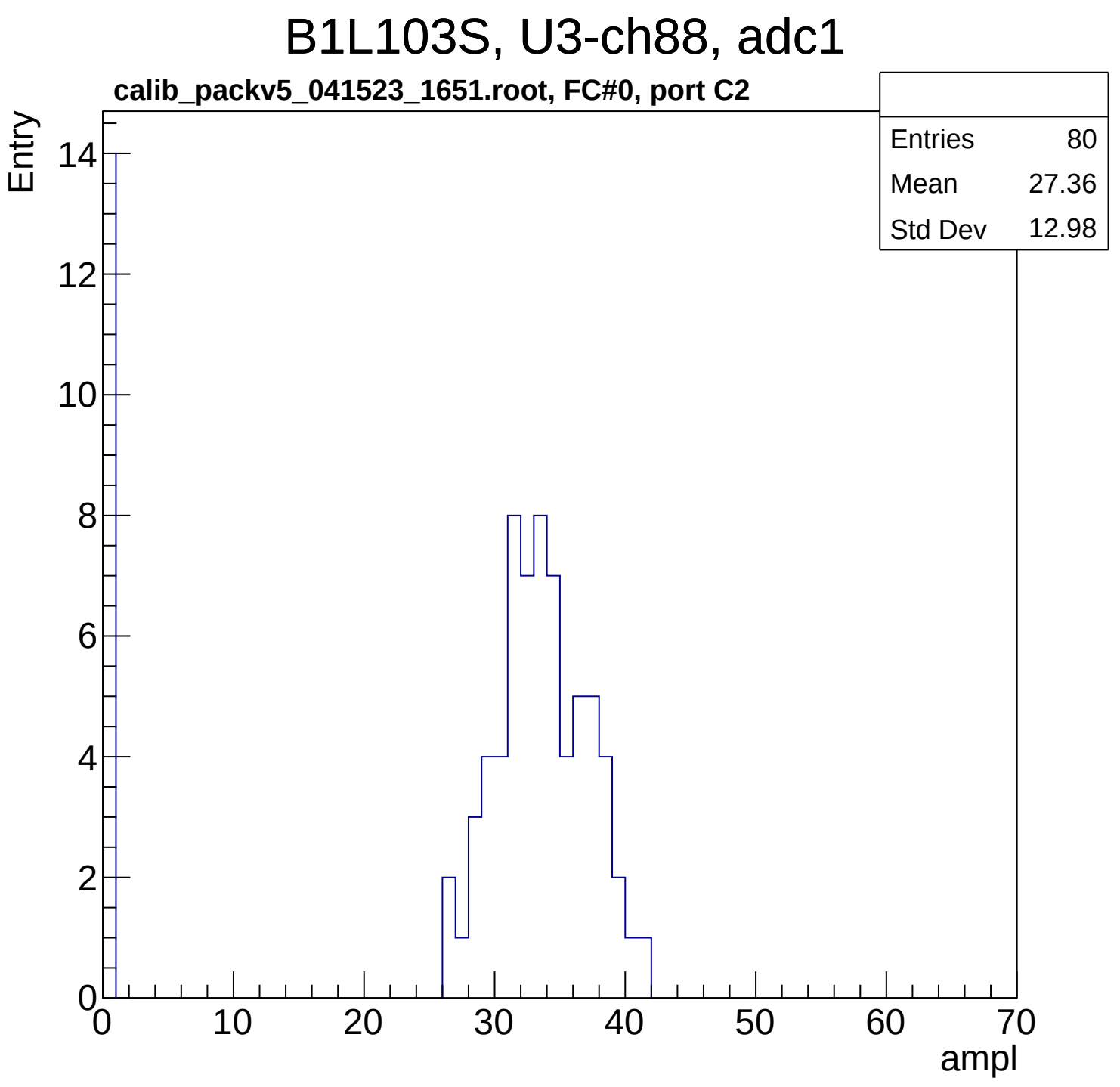
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch88, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 27.36
Std Dev 12.98
Entry
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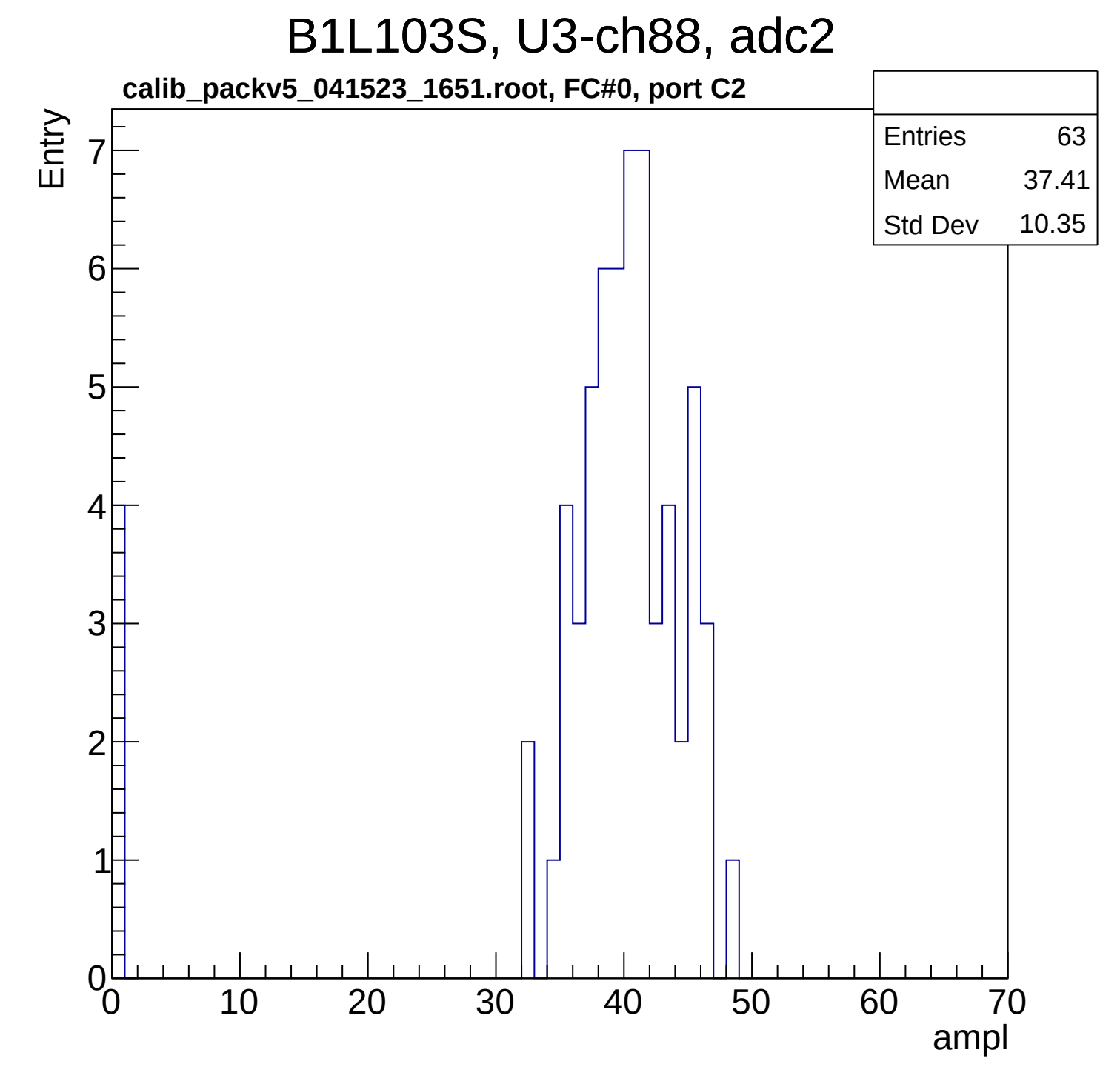
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch88, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 37.41
Std Dev 10.35
Entry
ampl
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2
3
4
5
6
7
0
10
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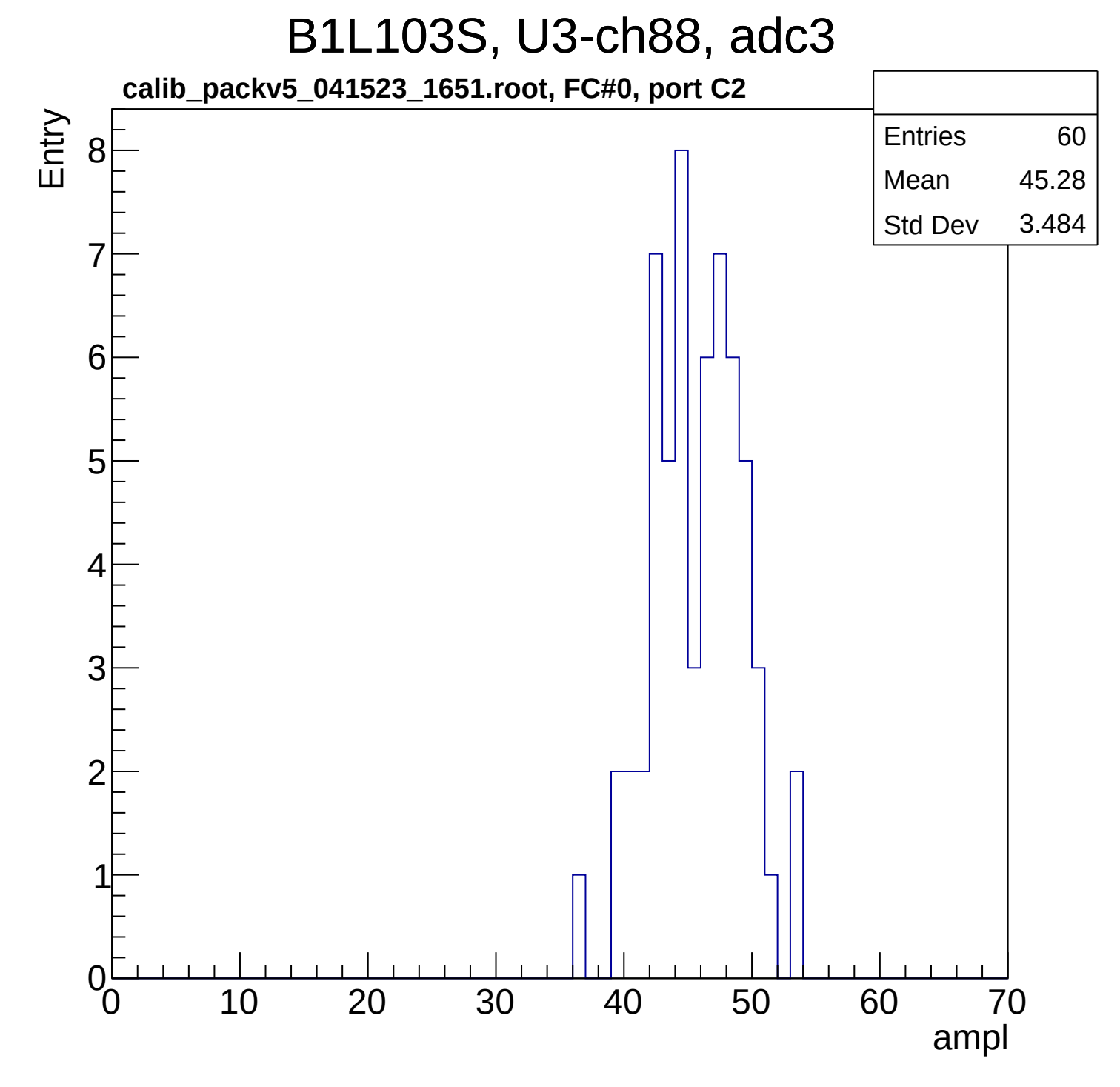
30
40
50
60
70


B1L103S, U3-ch88, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 45.28
Std Dev 3.484
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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60
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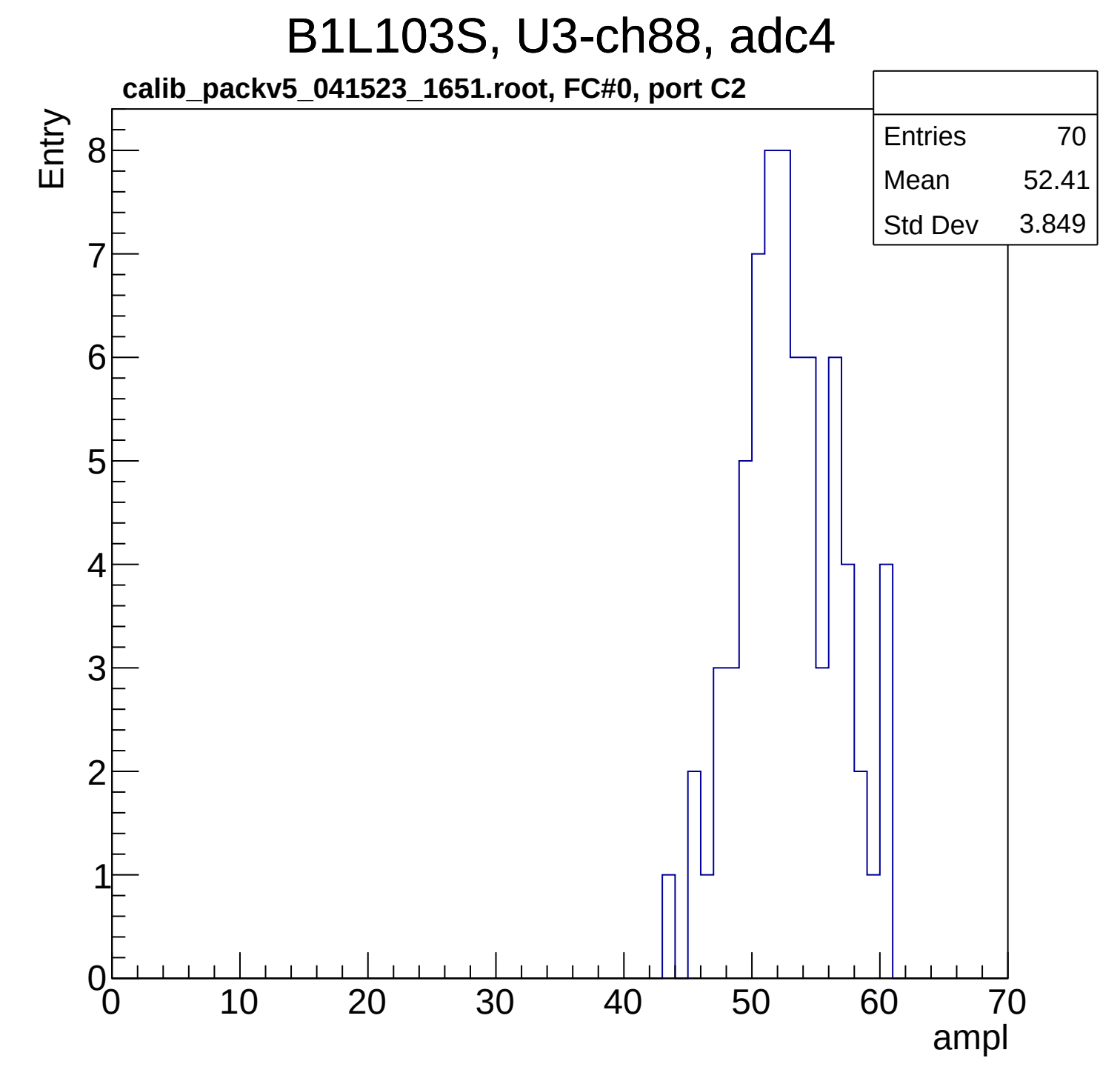
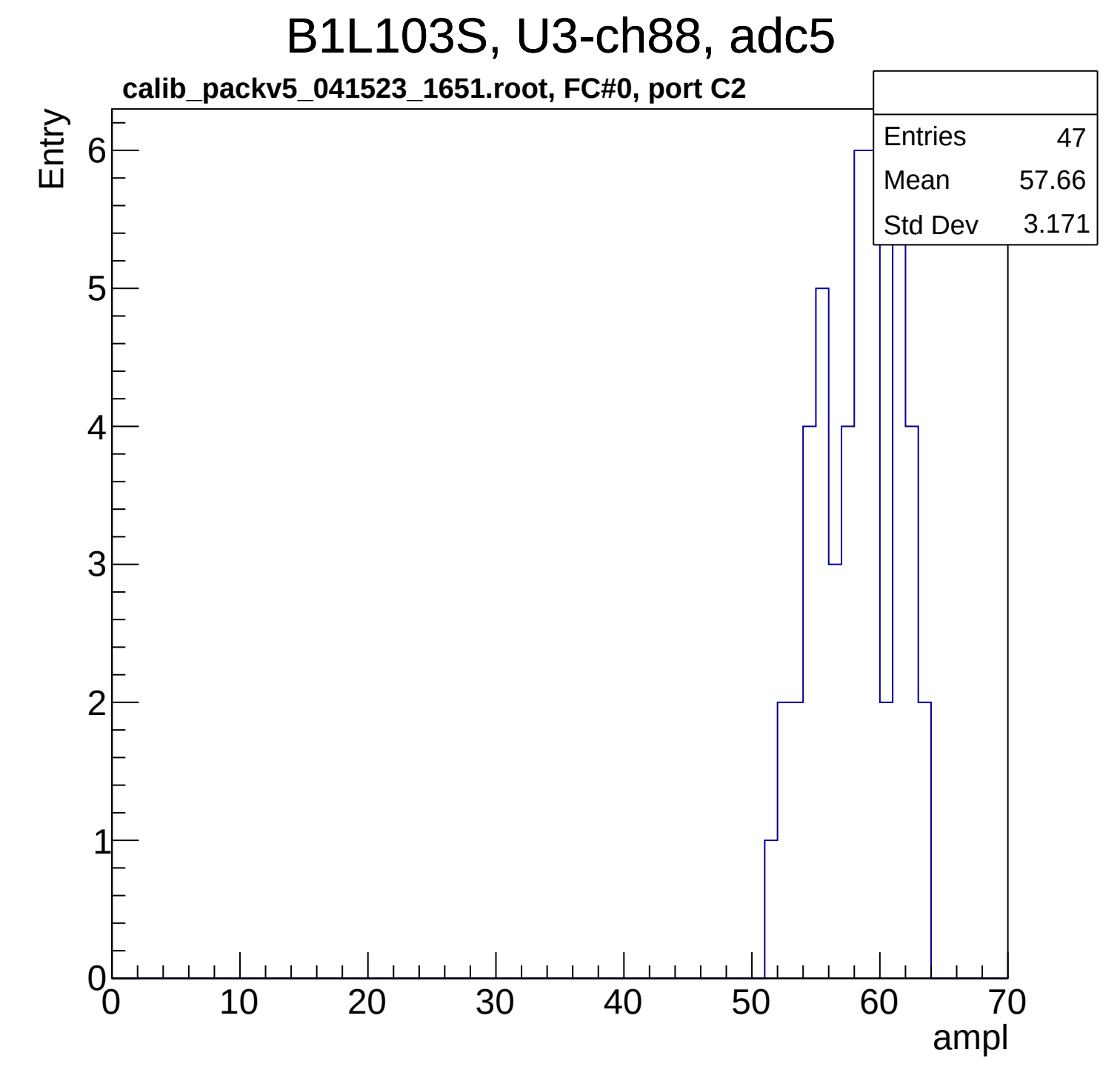
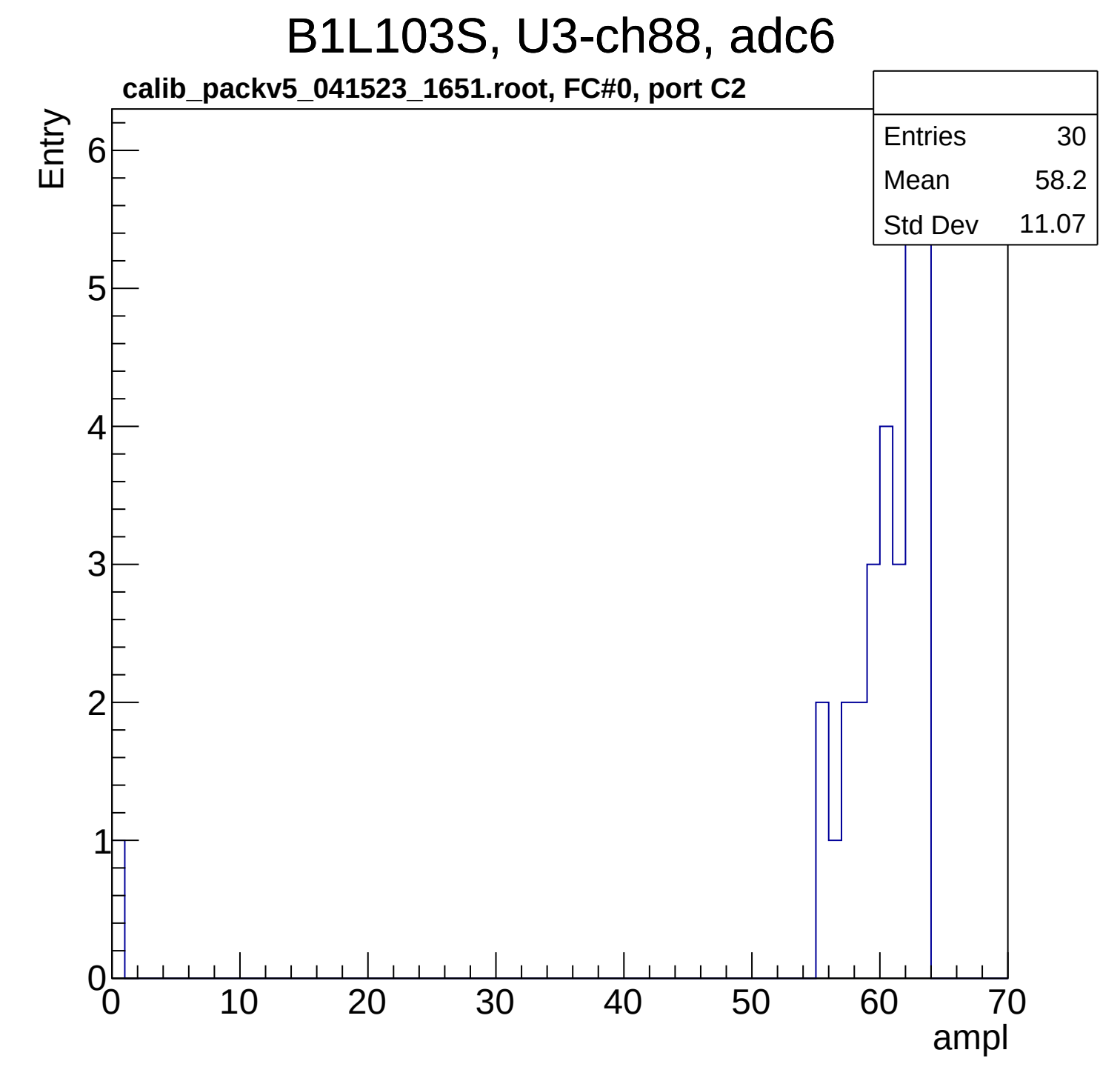
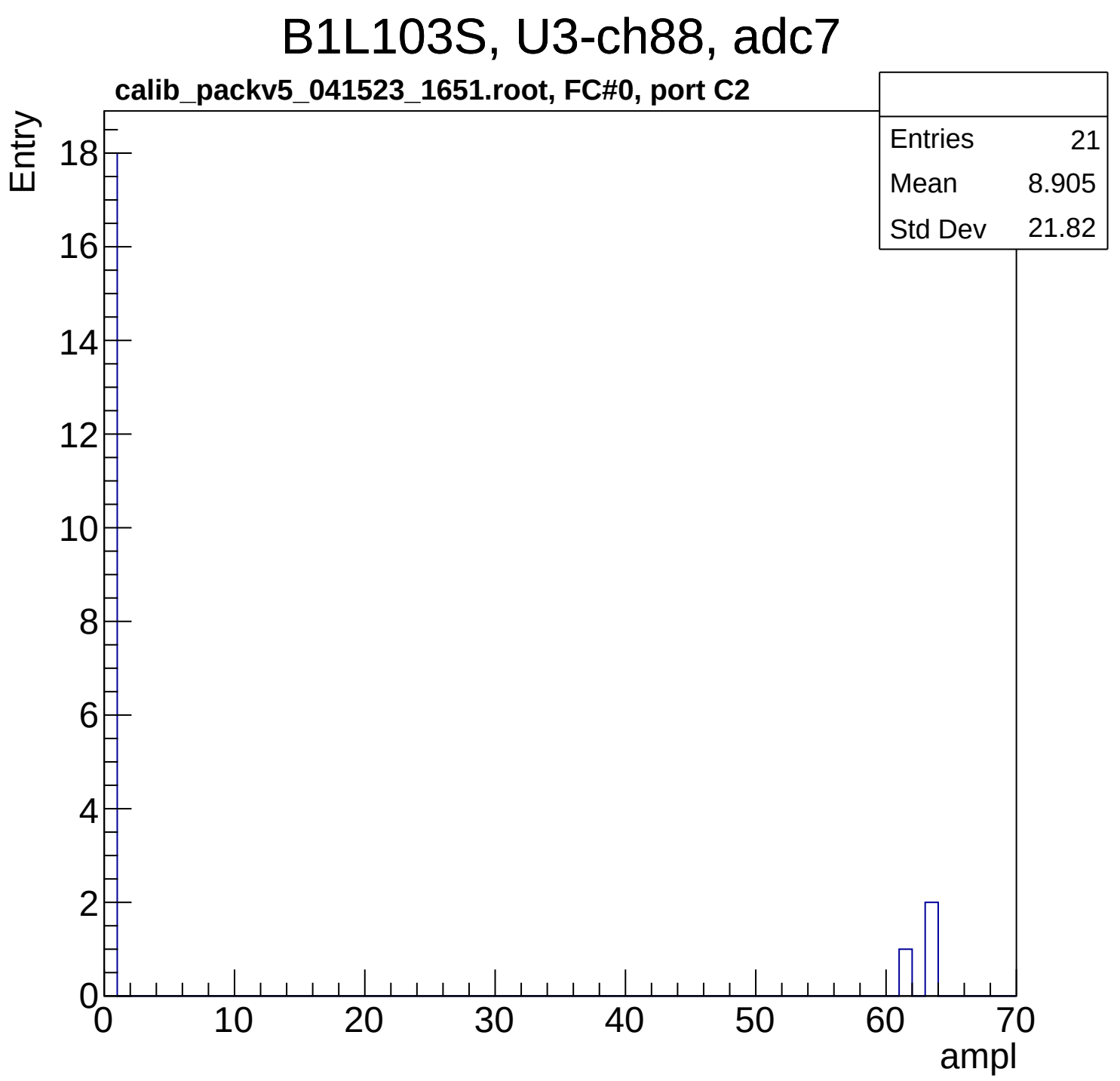

B1L103S, U3-ch88, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 52.41
Std Dev 3.849
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch88, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 57.66
Std Dev 3.171
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U3-ch88, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 58.2
Std Dev 11.07
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch88, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 8.905
Std Dev 21.82
Entry
0
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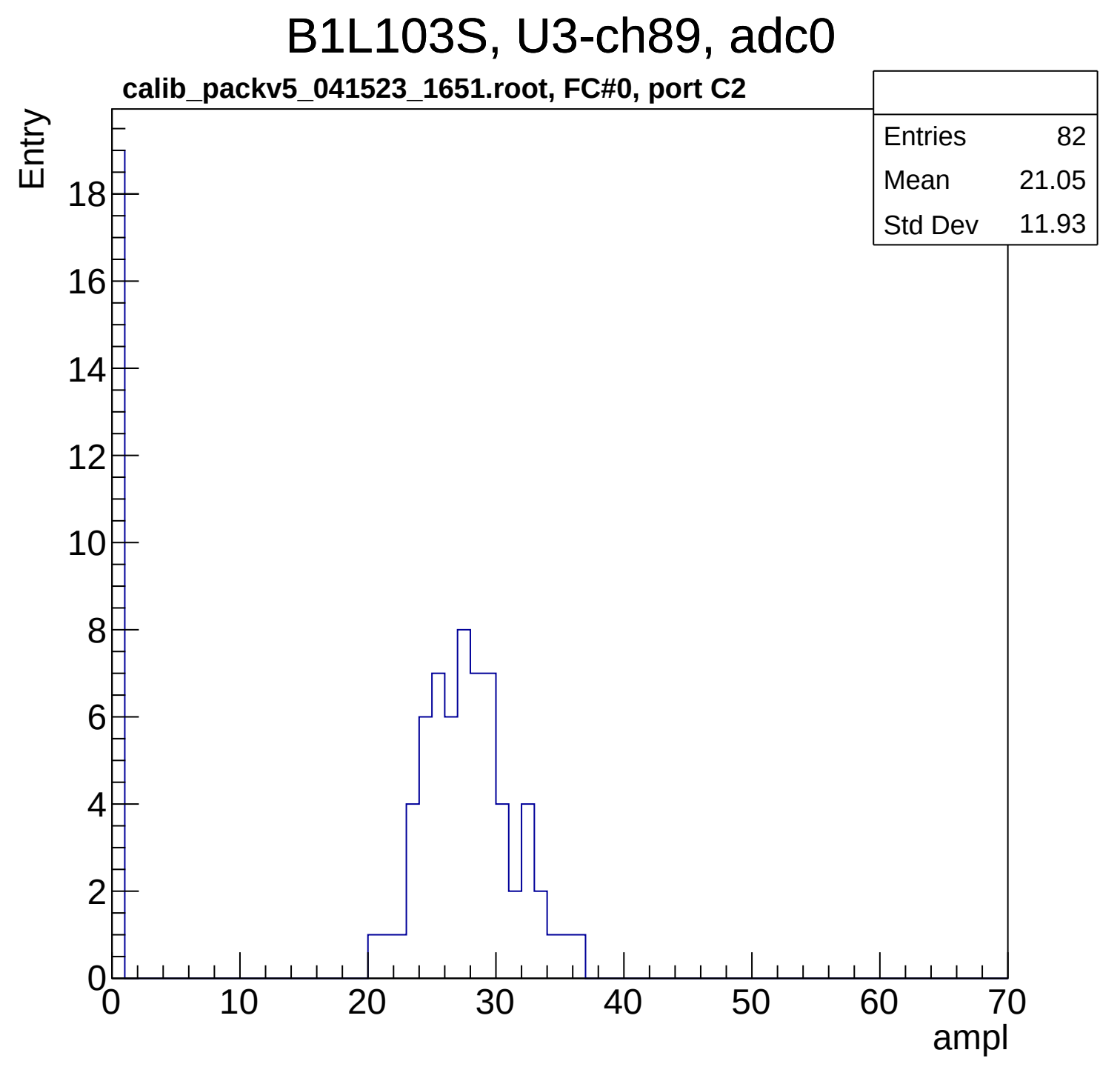
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch89, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 21.05
Std Dev 11.93
Entry
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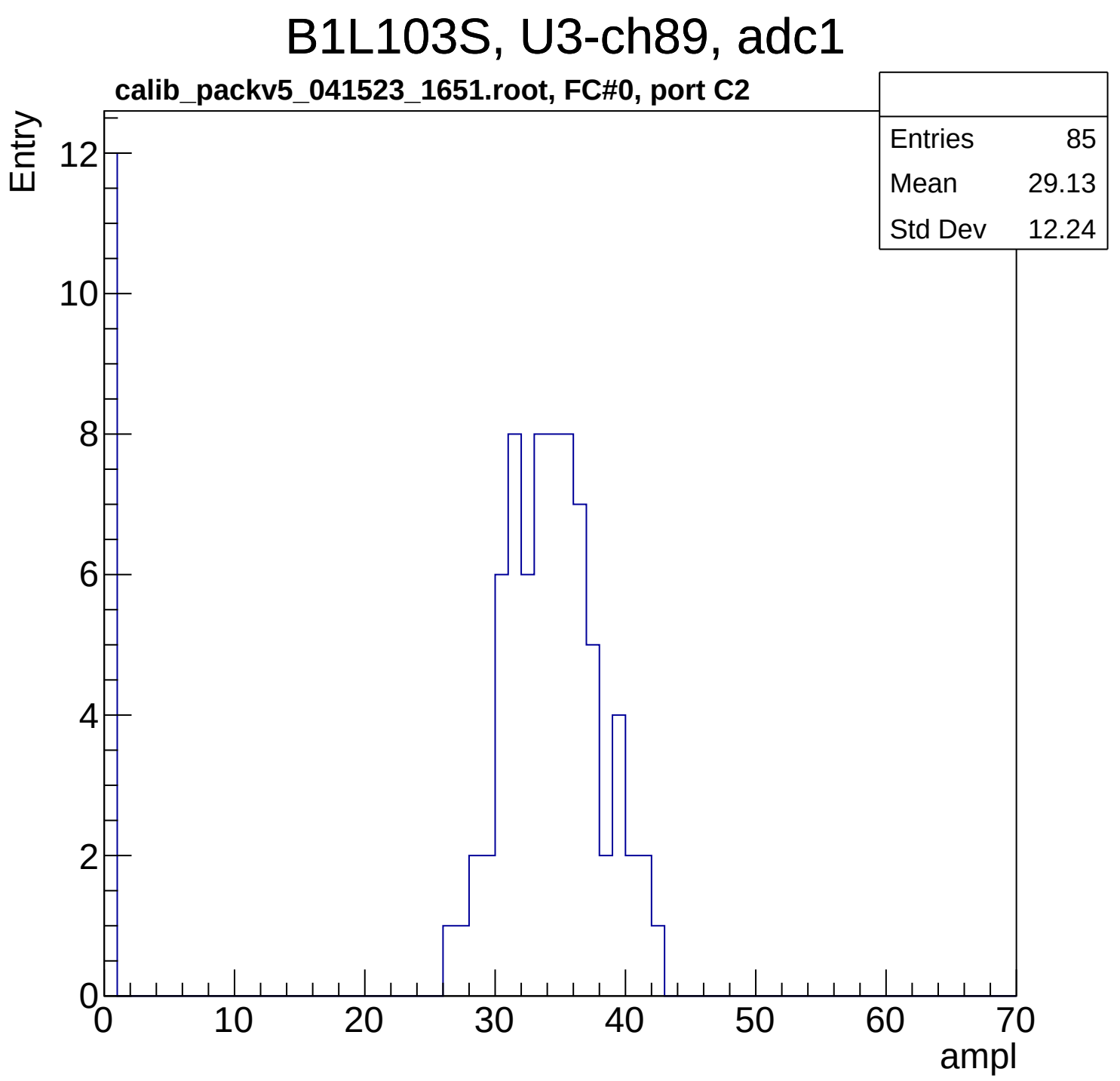
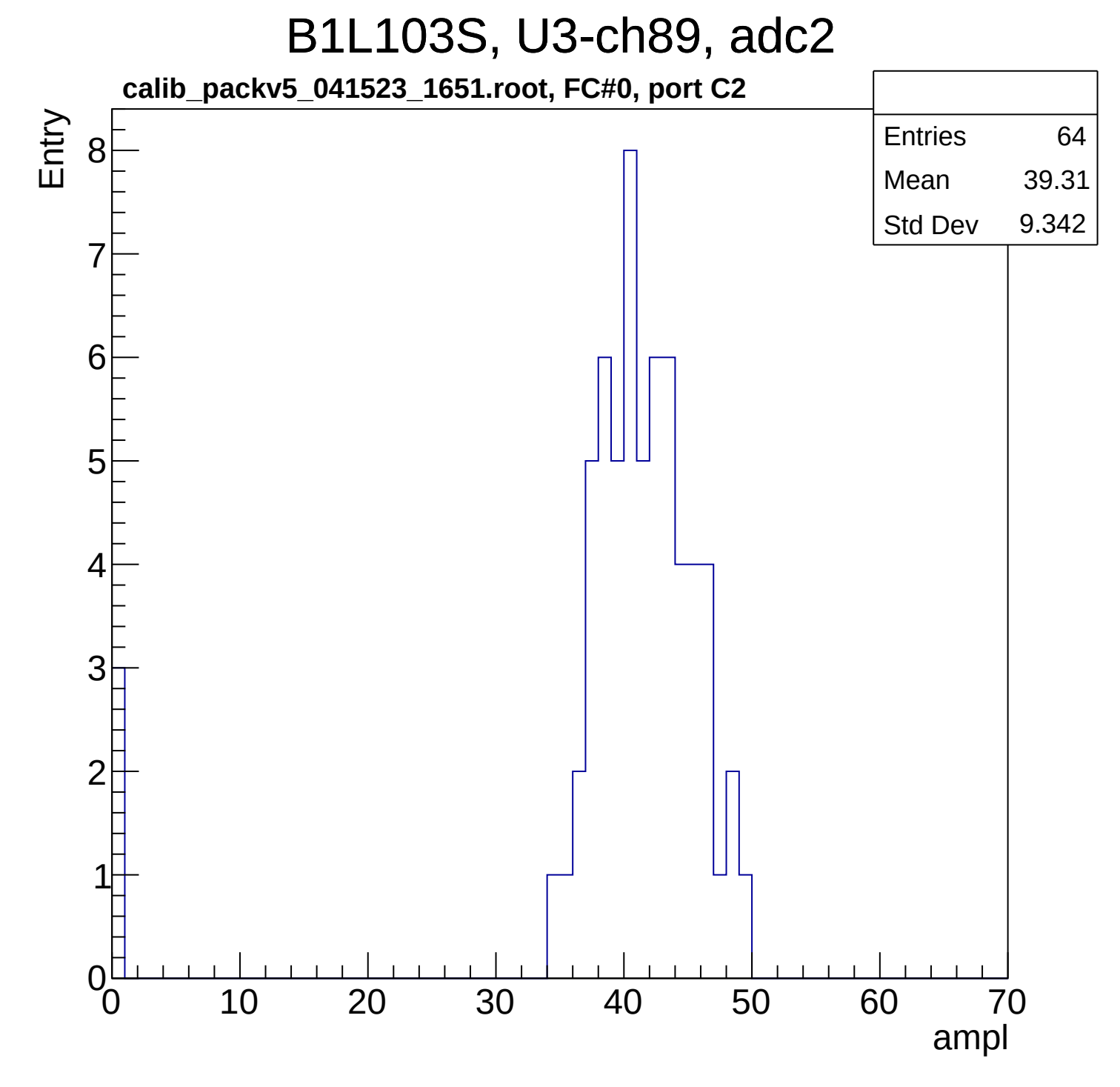
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch89, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 29.13
Std Dev 12.24
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch89, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 39.31
Std Dev 9.342
Entry
ampl
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1
2
3
4
5
6
7
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0
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20
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40
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60
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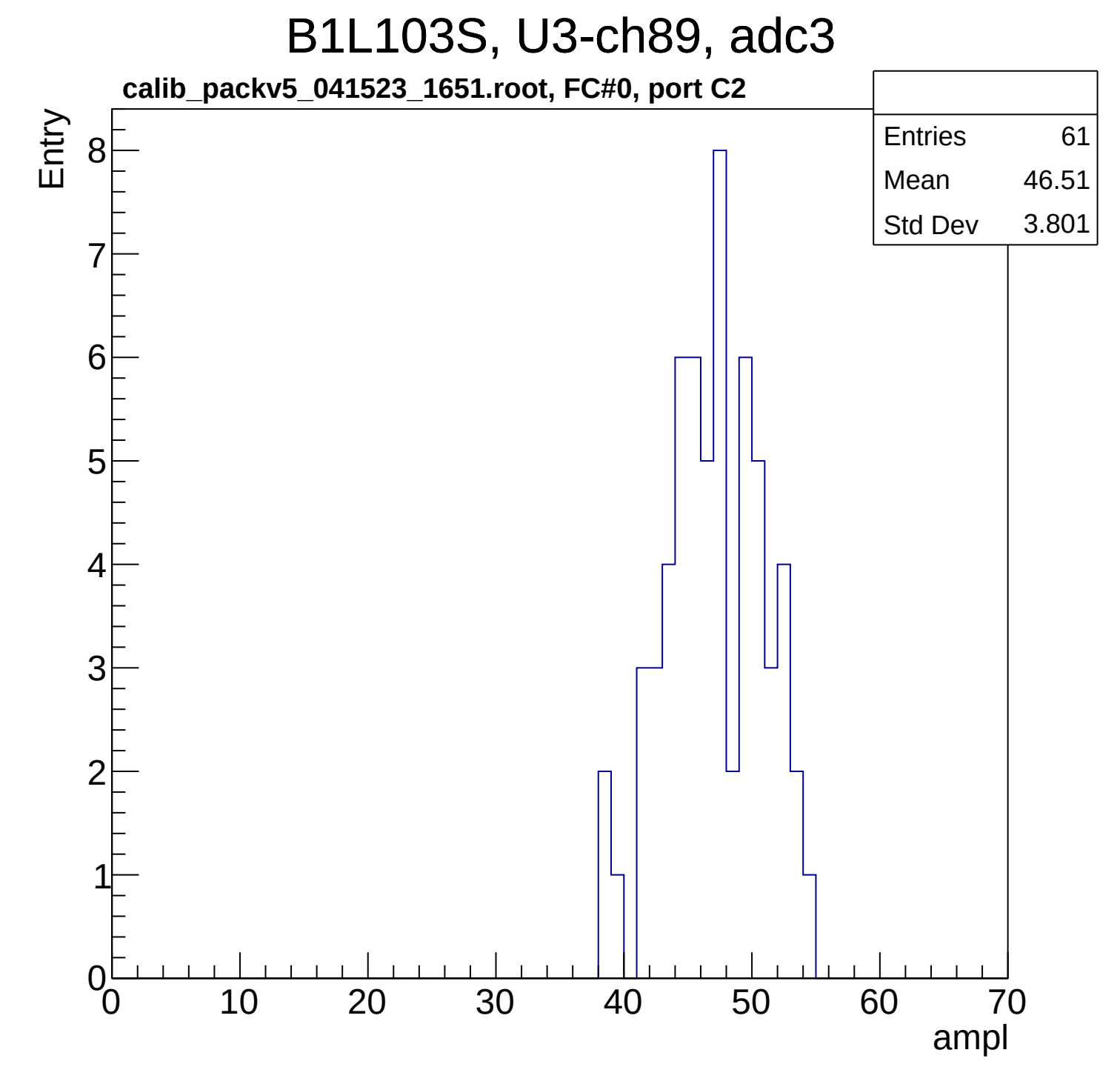
B1L103S, U3-ch89, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 46.51
Std Dev 3.801
Entry
ampl
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2
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7
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40
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60
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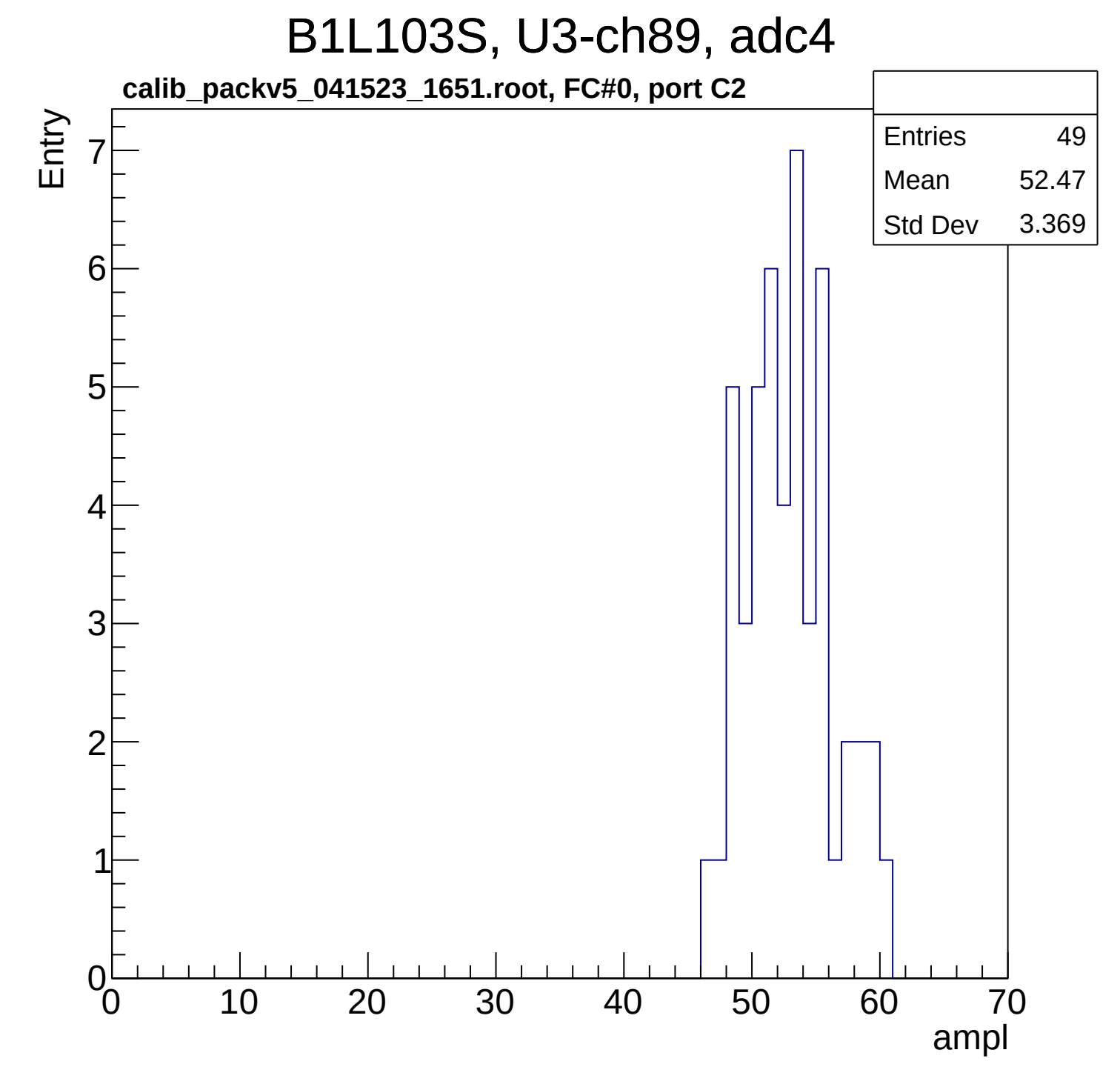
B1L103S, U3-ch89, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 52.47
Std Dev 3.369
Entry
ampl
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1
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4
5
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0
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20
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40
50
60
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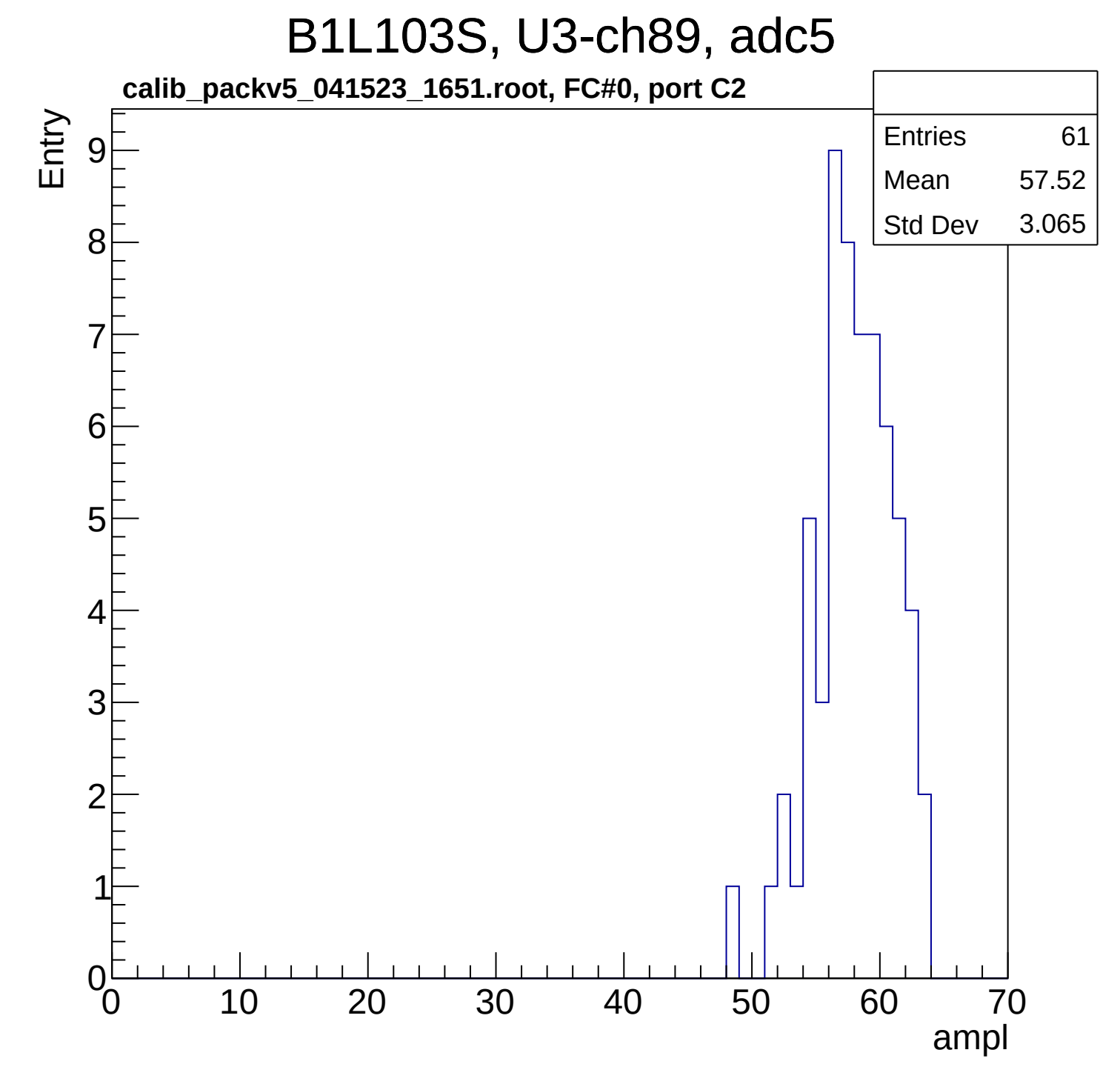
B1L103S, U3-ch89, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 57.52
Std Dev 3.065
Entry
ampl
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2
3
4
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6
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8
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0
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40
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60
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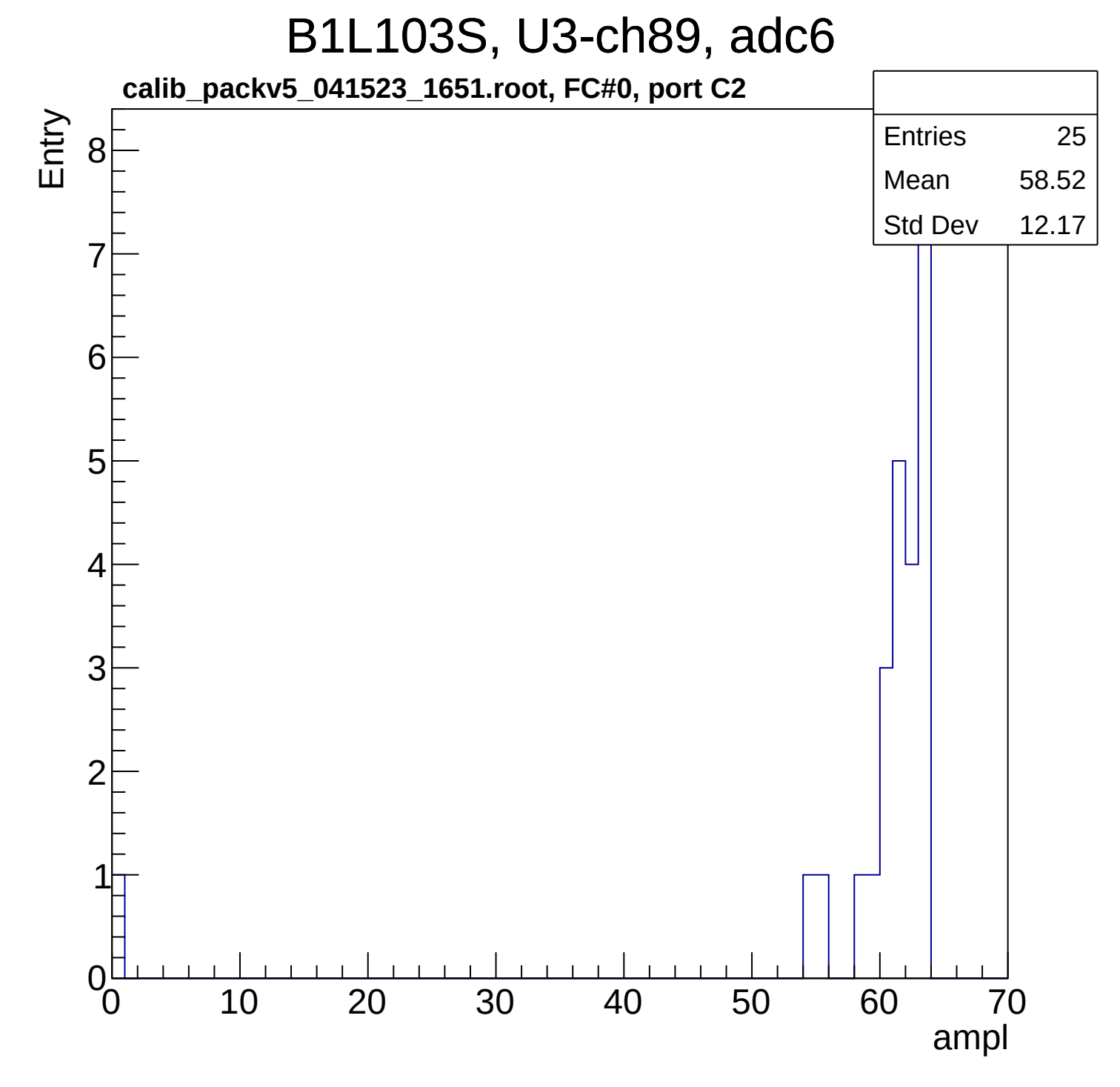
B1L103S, U3-ch89, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 58.52
Std Dev 12.17
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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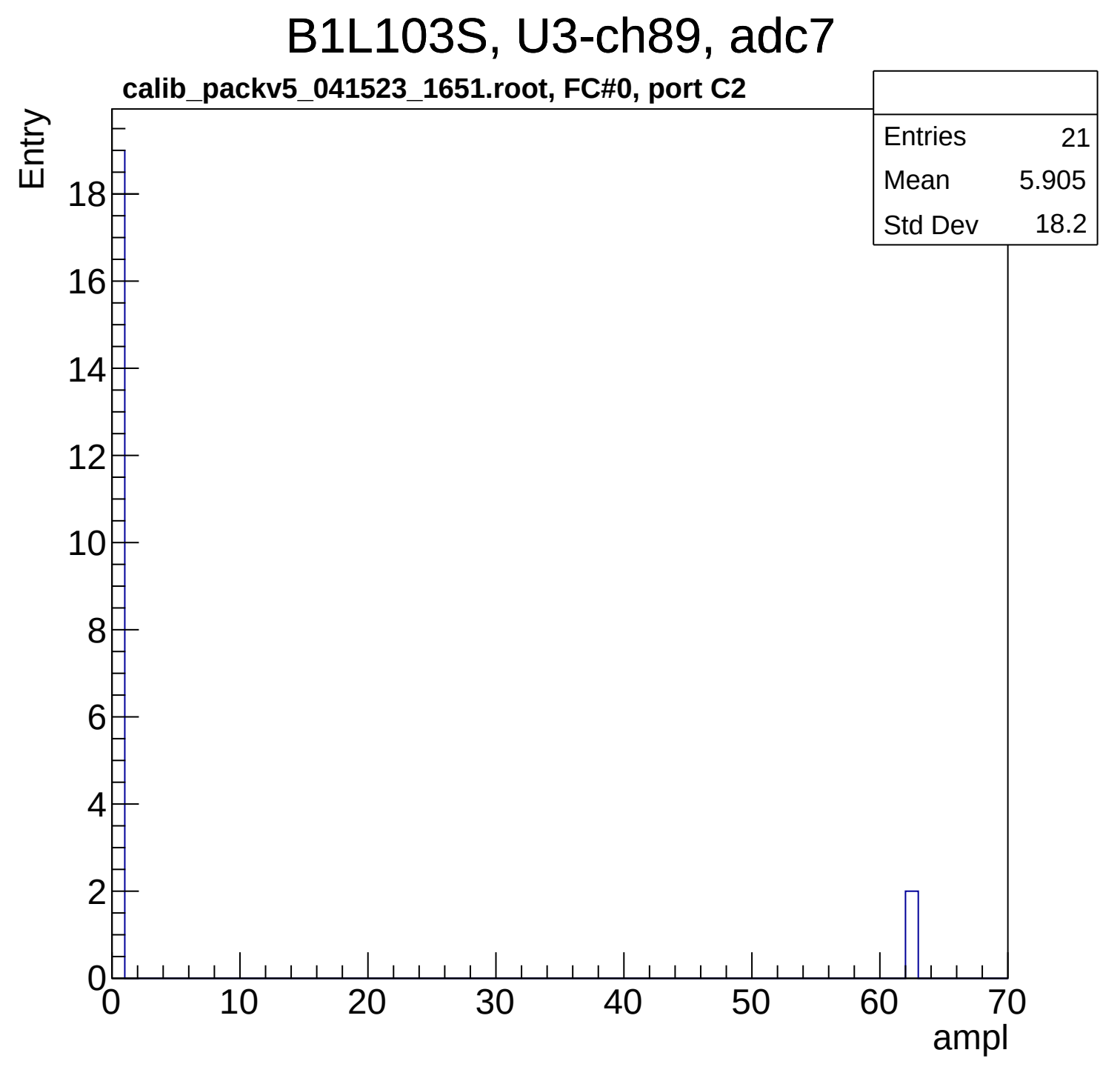
B1L103S, U3-ch89, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.905
Std Dev 18.2
Entry
0
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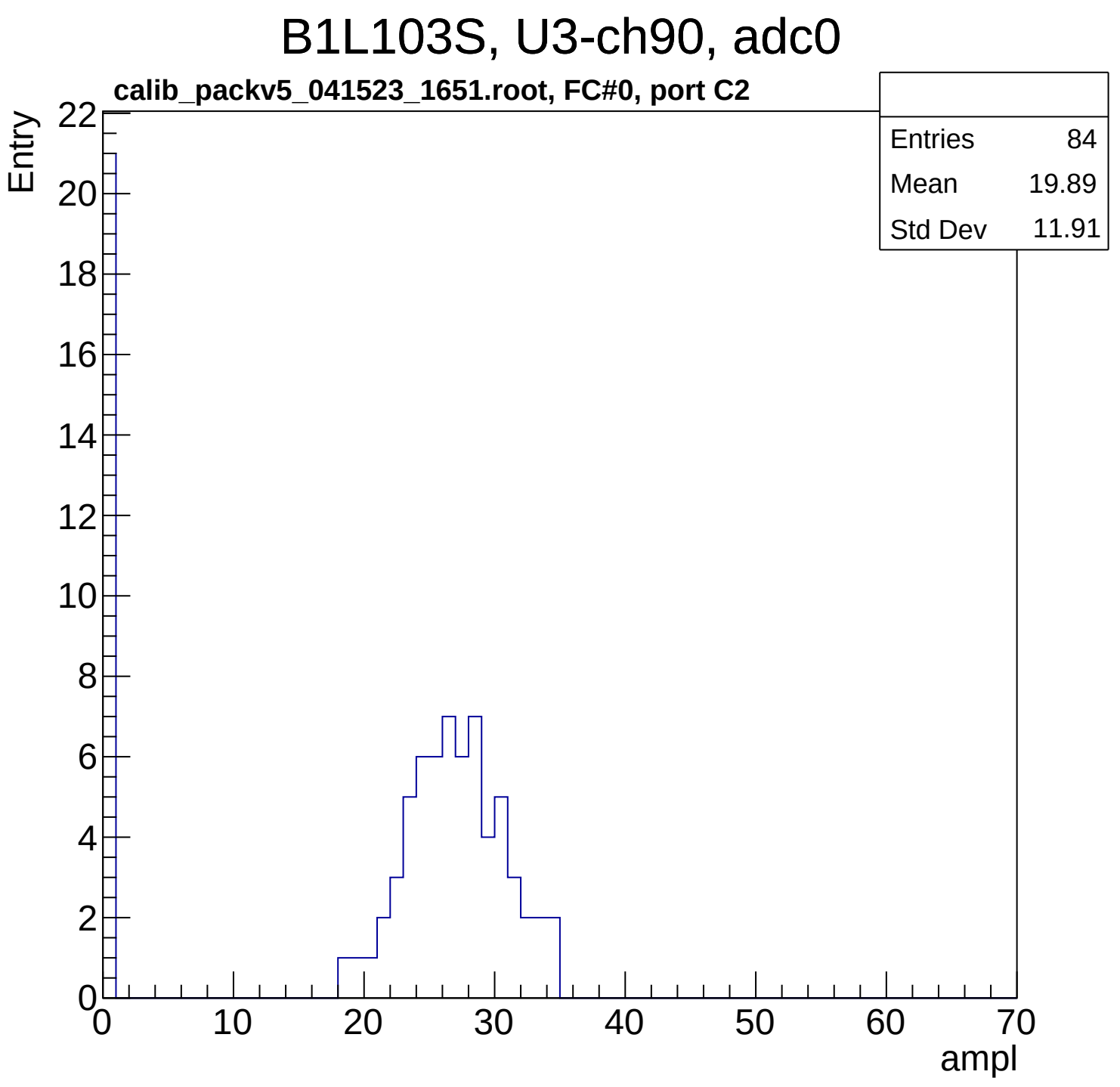
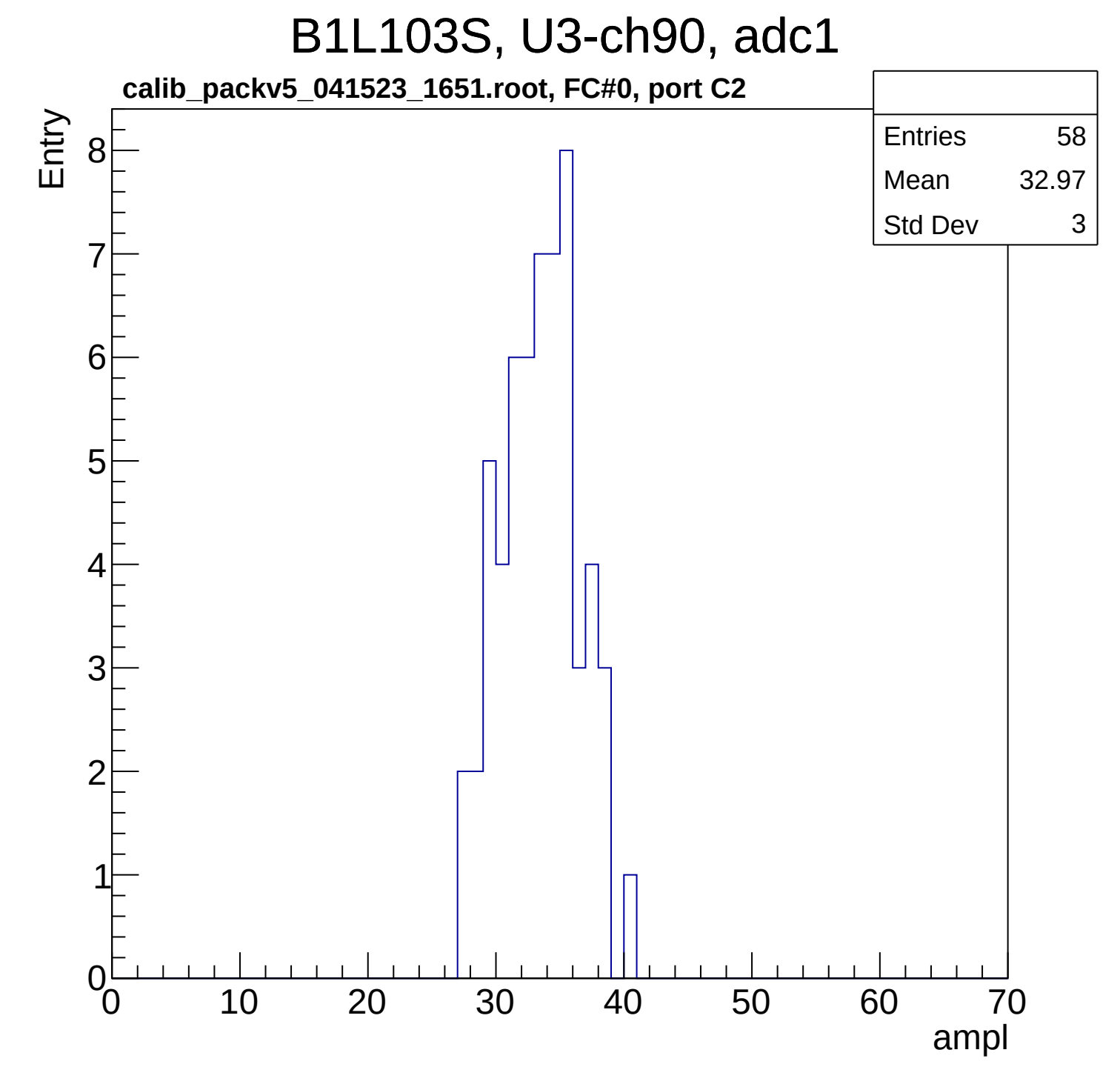
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch90, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 19.89
Std Dev 11.91
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70


B1L103S, U3-ch90, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 32.97
Std Dev 3
Entry
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2
3
4
5
6
7
8
0
10
20
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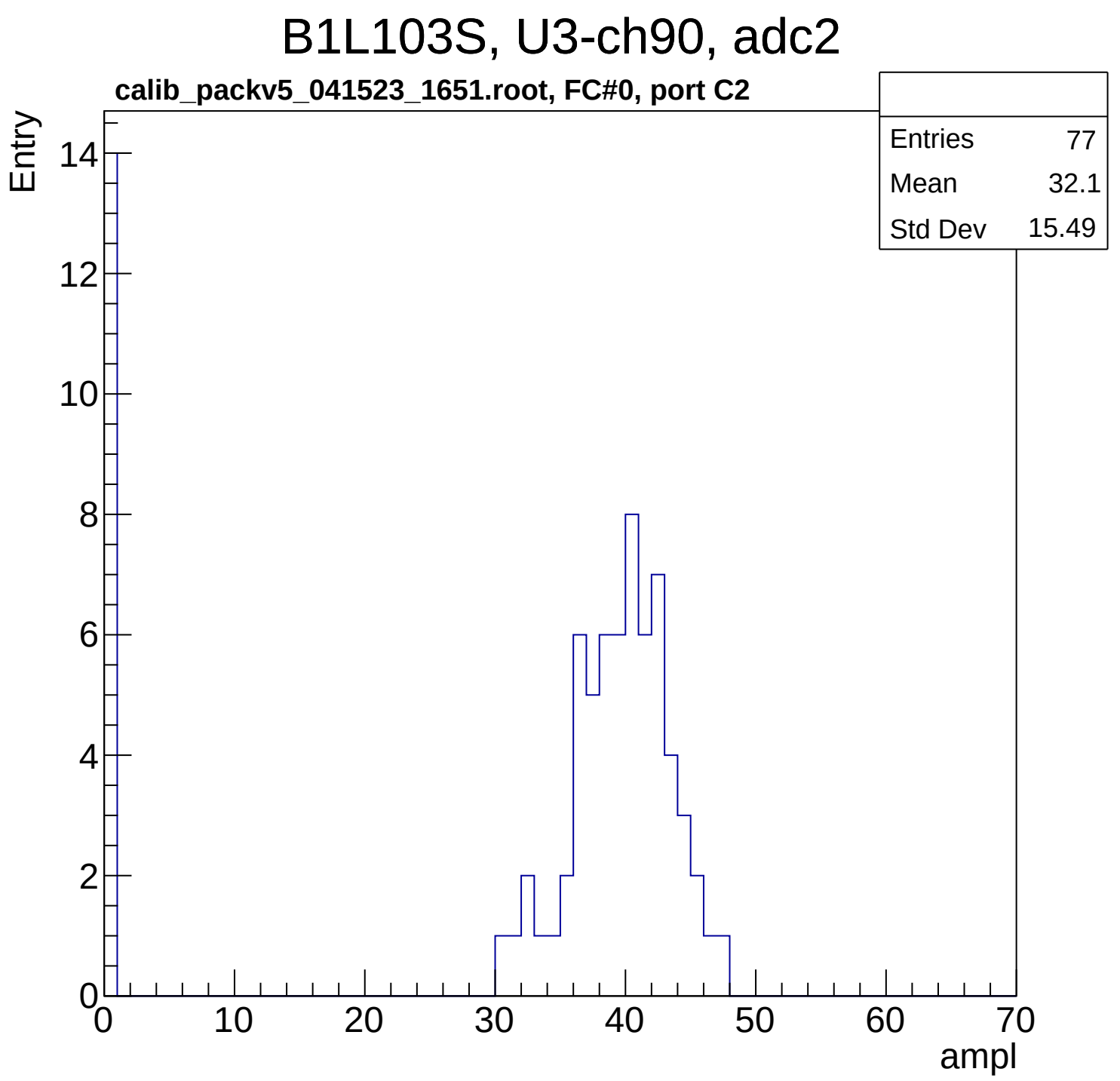
50
60
70
ampl


B1L103S, U3-ch90, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 32.1
Std Dev 15.49
Entry
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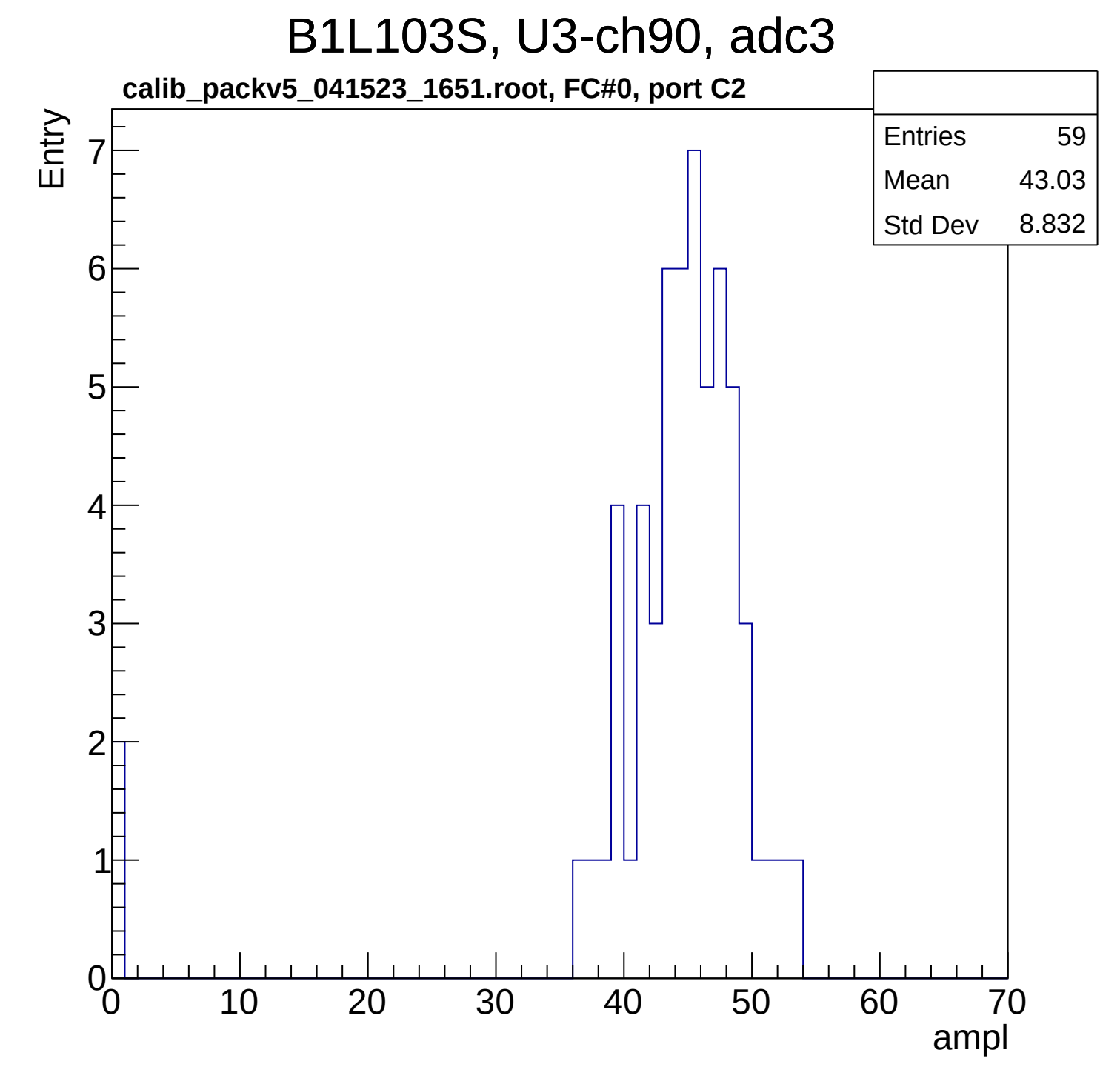
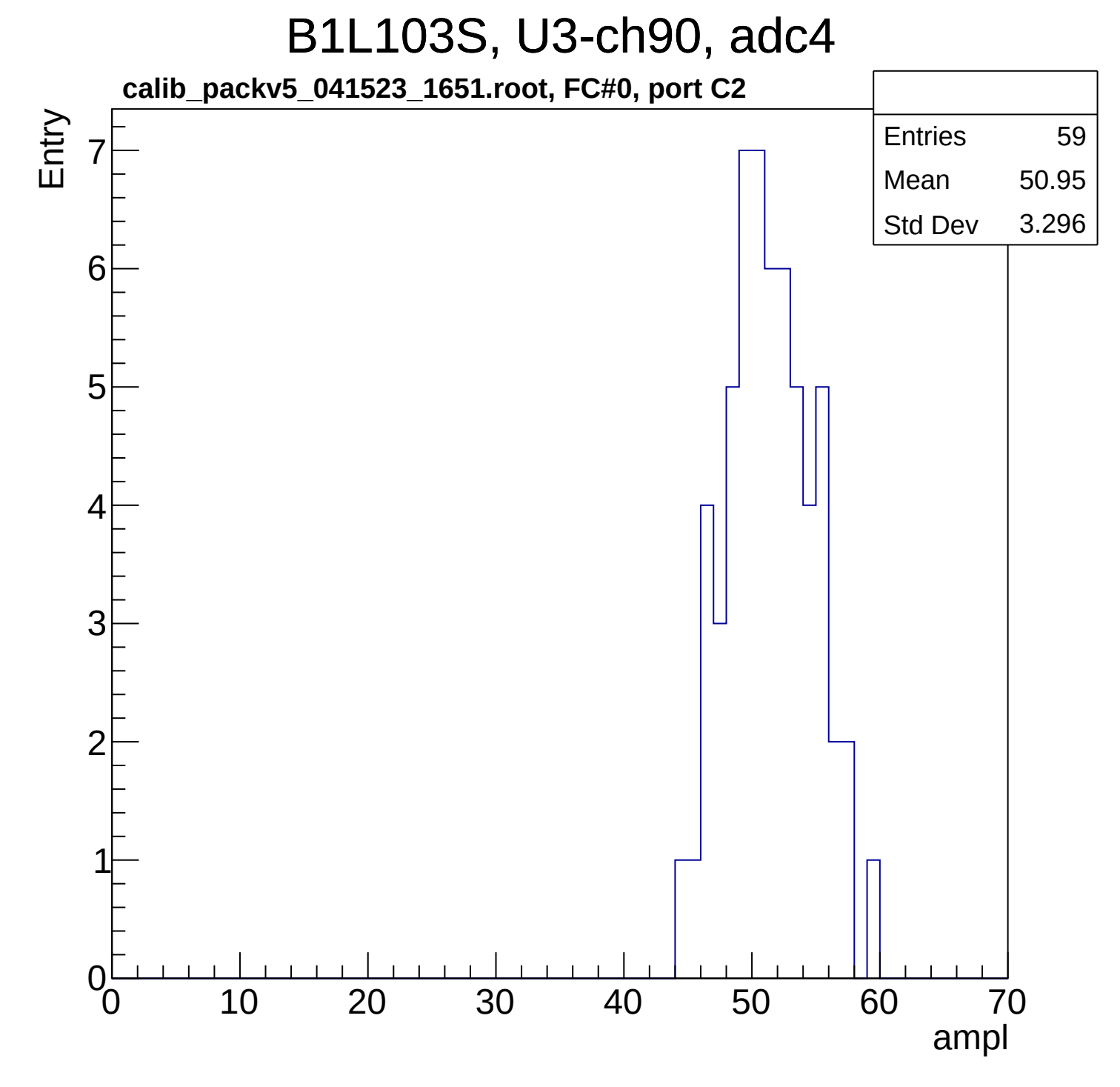
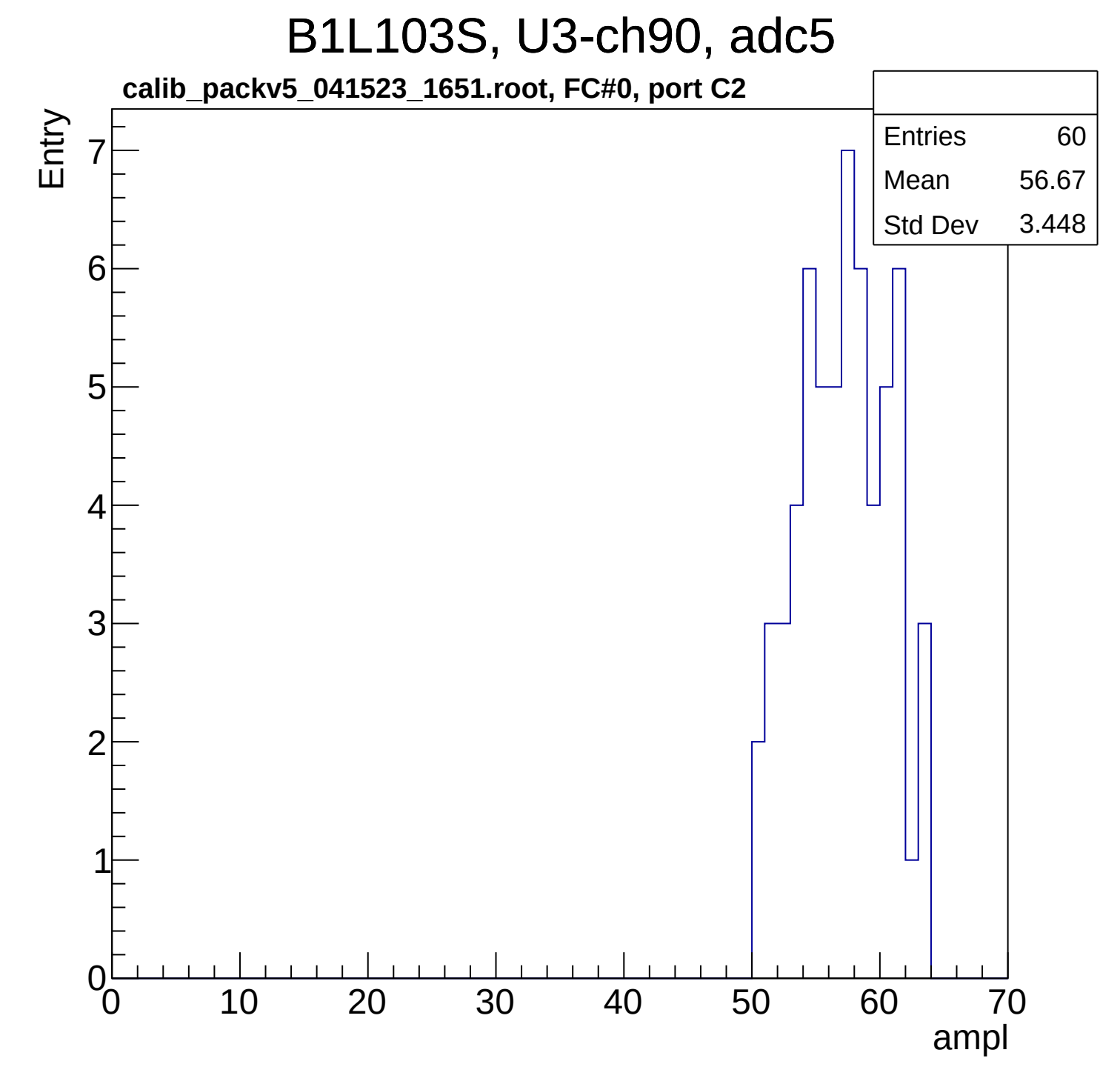
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch90, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 43.03
Std Dev 8.832
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch90, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 50.95
Std Dev 3.296
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch90, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 56.67
Std Dev 3.448
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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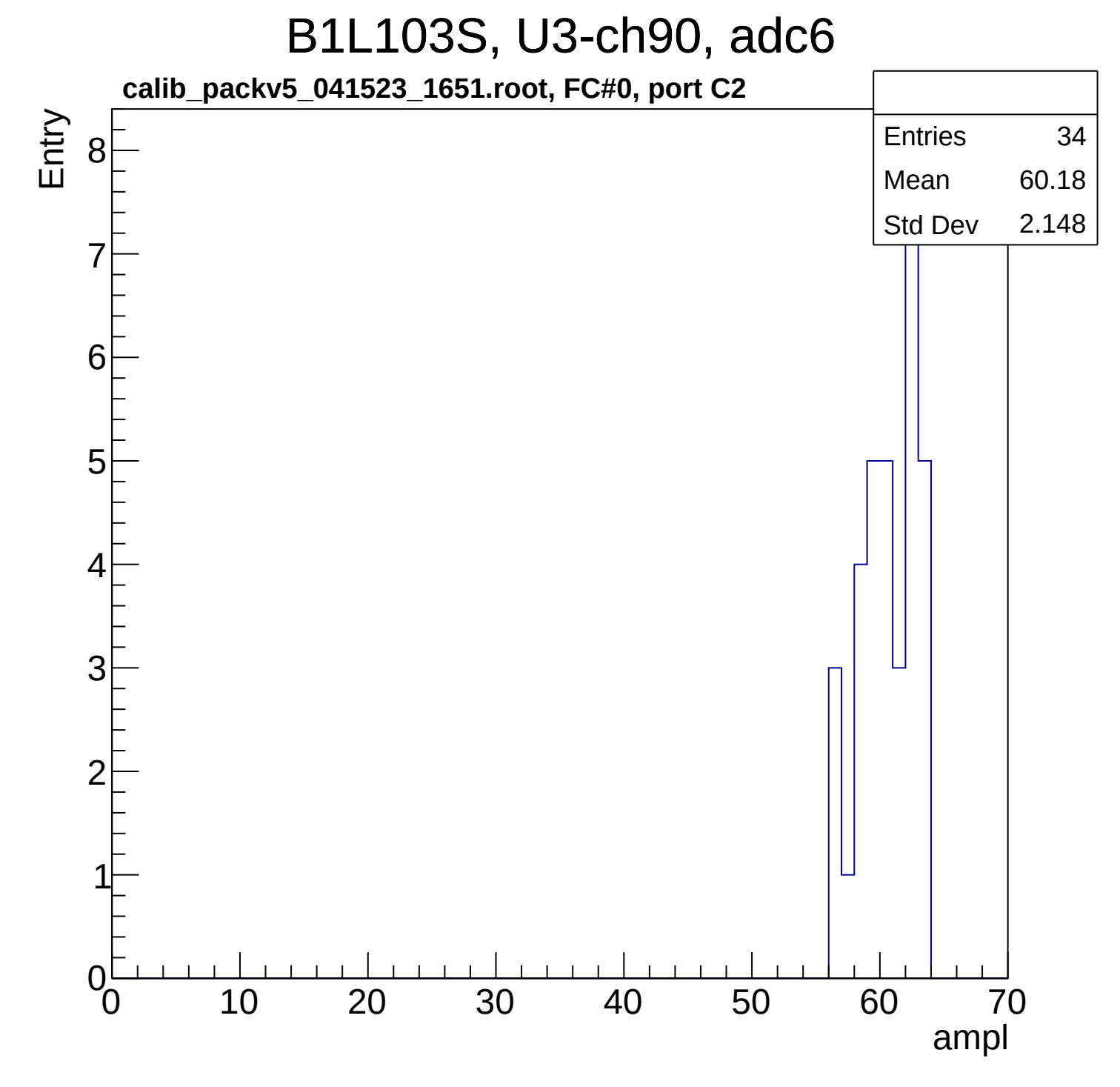
B1L103S, U3-ch90, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 60.18
Std Dev 2.148
Entry
ampl
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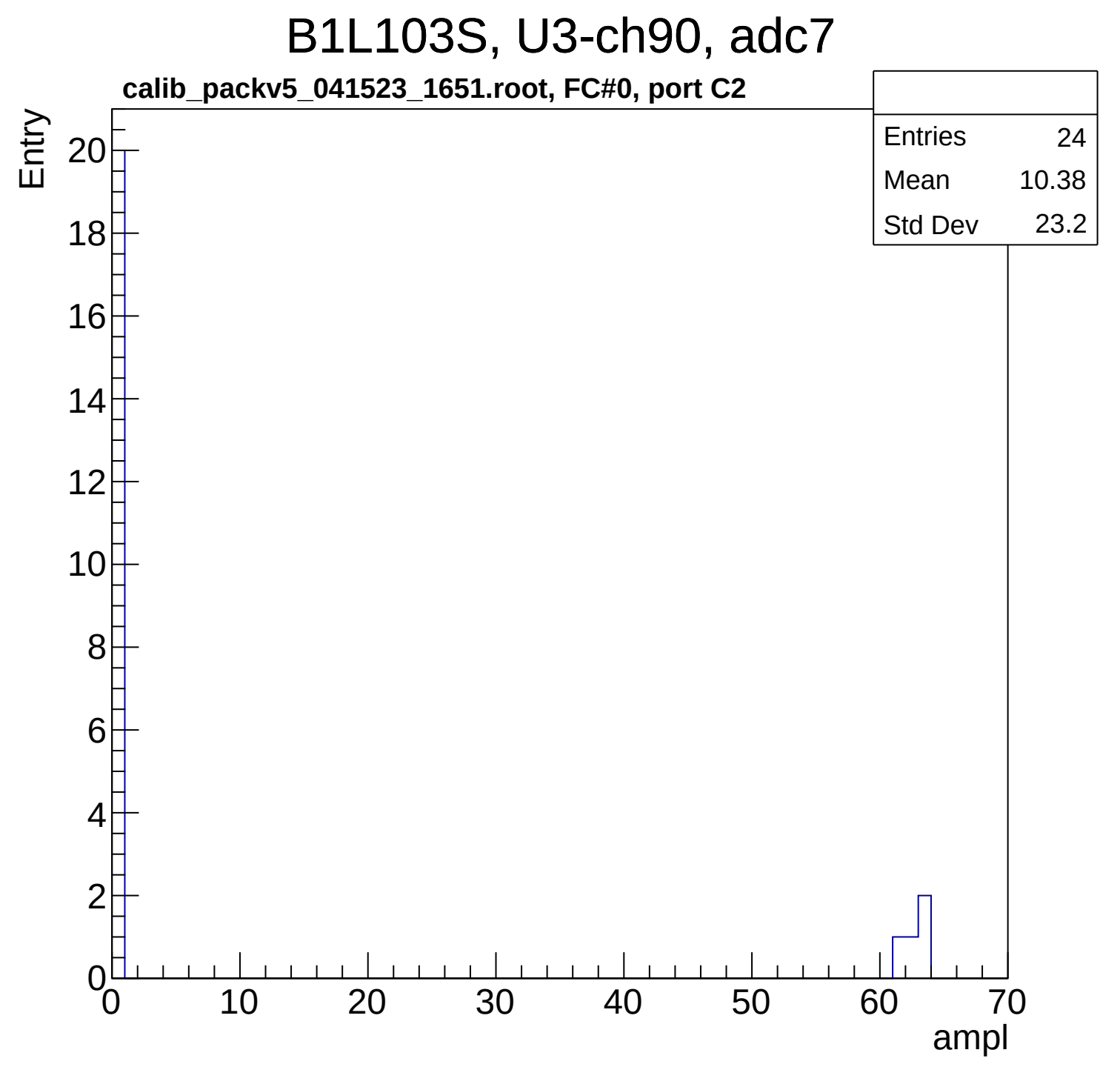
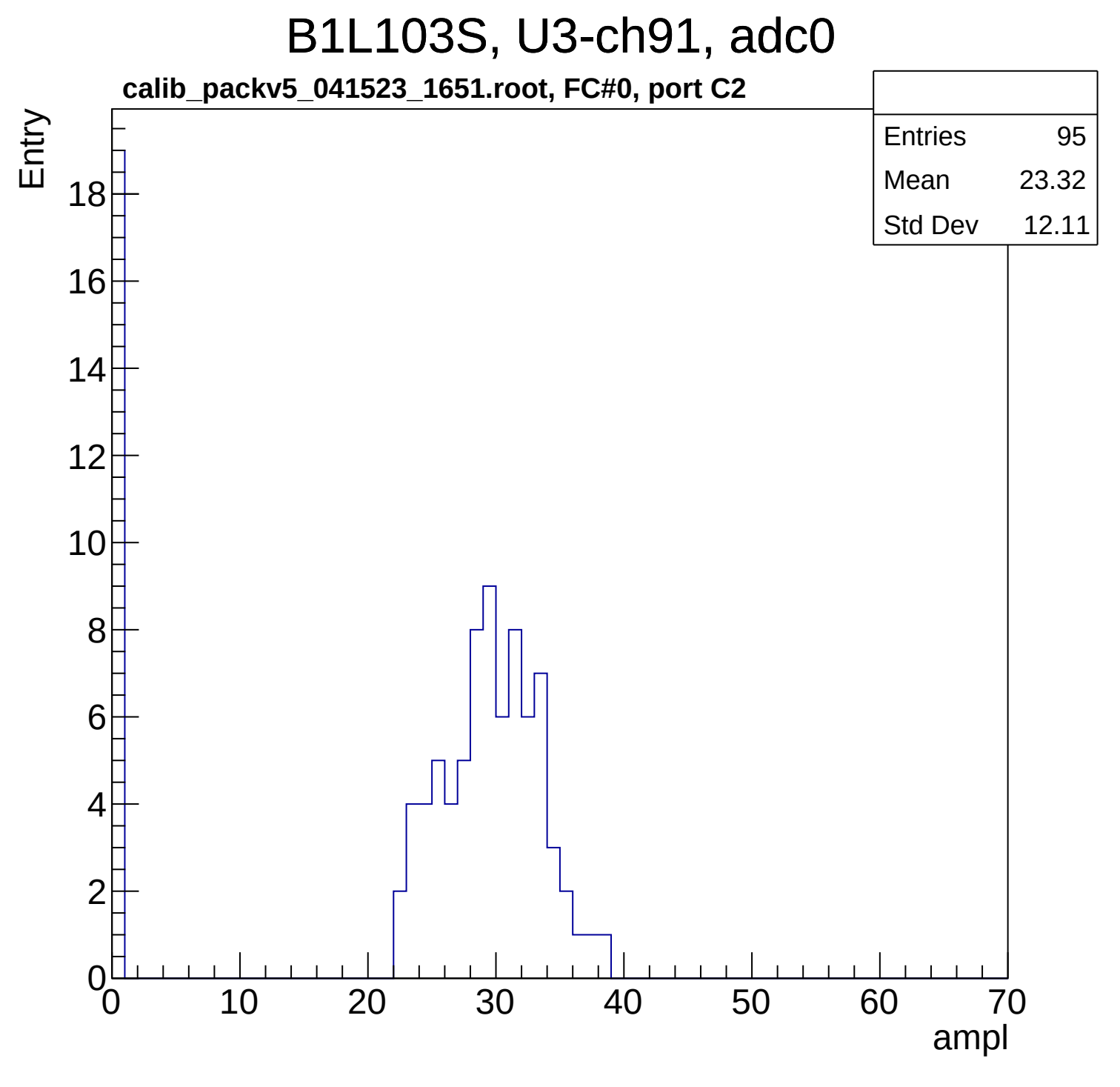
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch90, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 10.38
Std Dev 23.2
Entry
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch91, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 23.32
Std Dev 12.11
Entry
0
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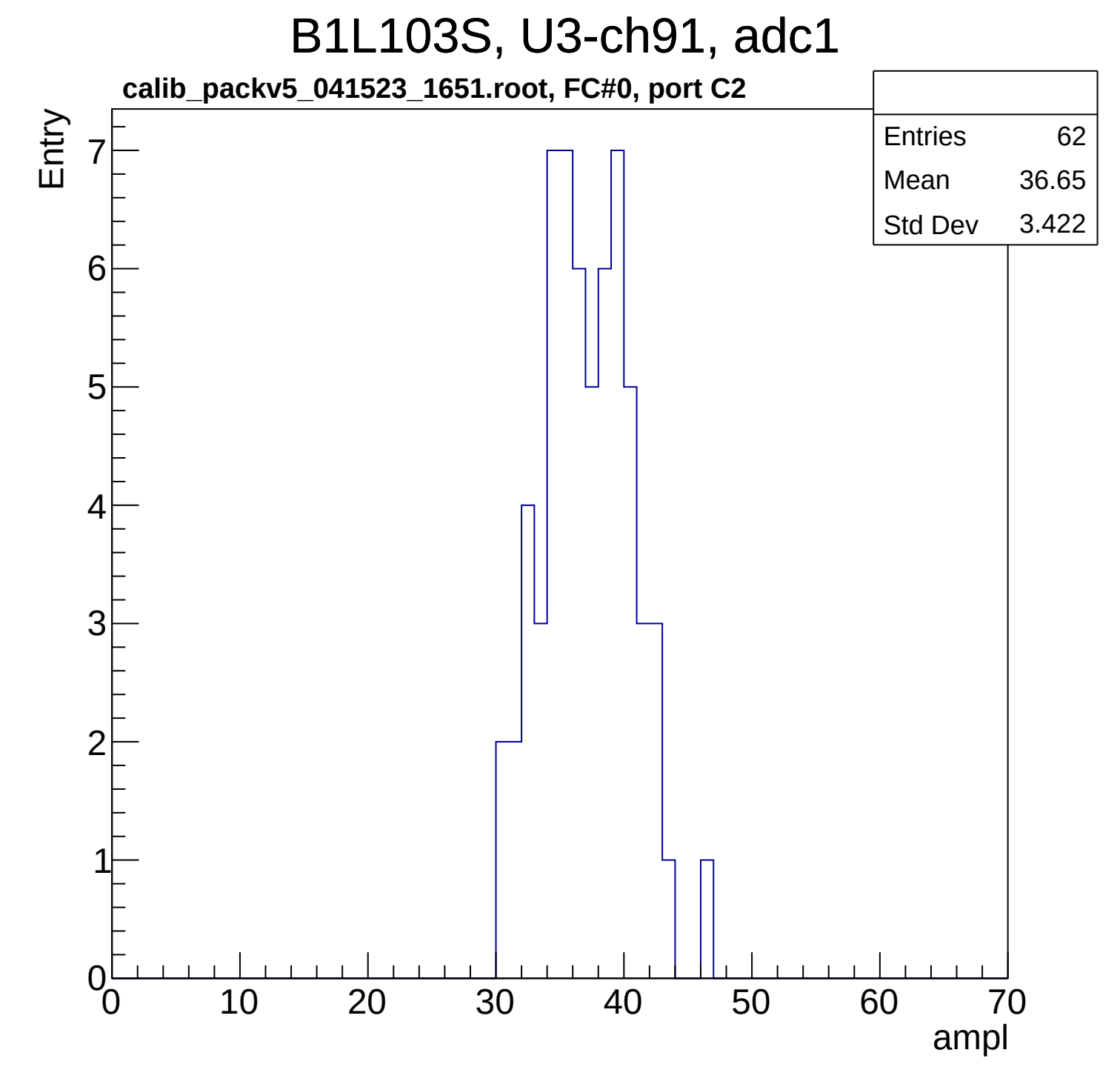
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch91, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 36.65
Std Dev 3.422
Entry
ampl
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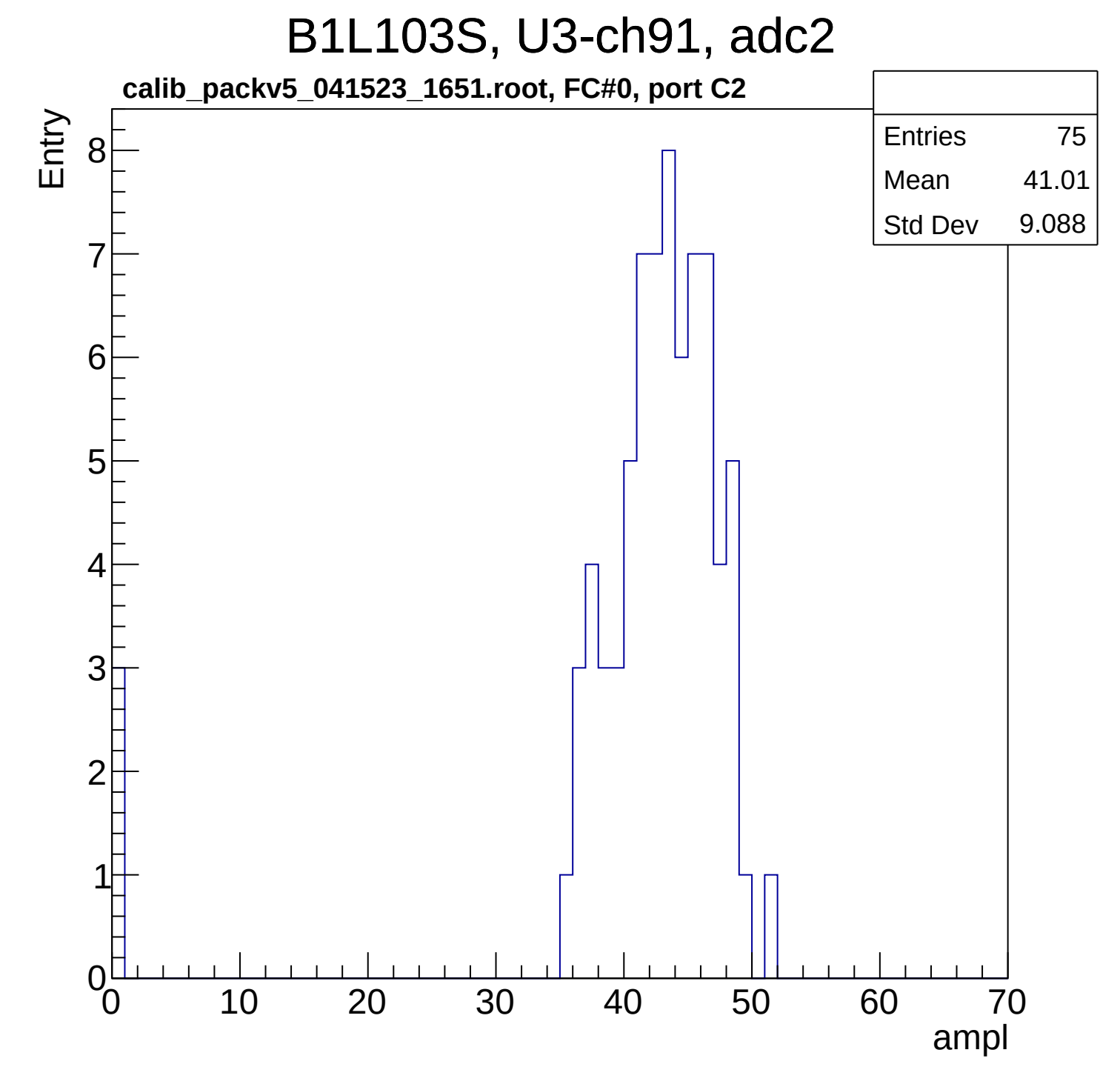
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch91, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 41.01
Std Dev 9.088
Entry
ampl
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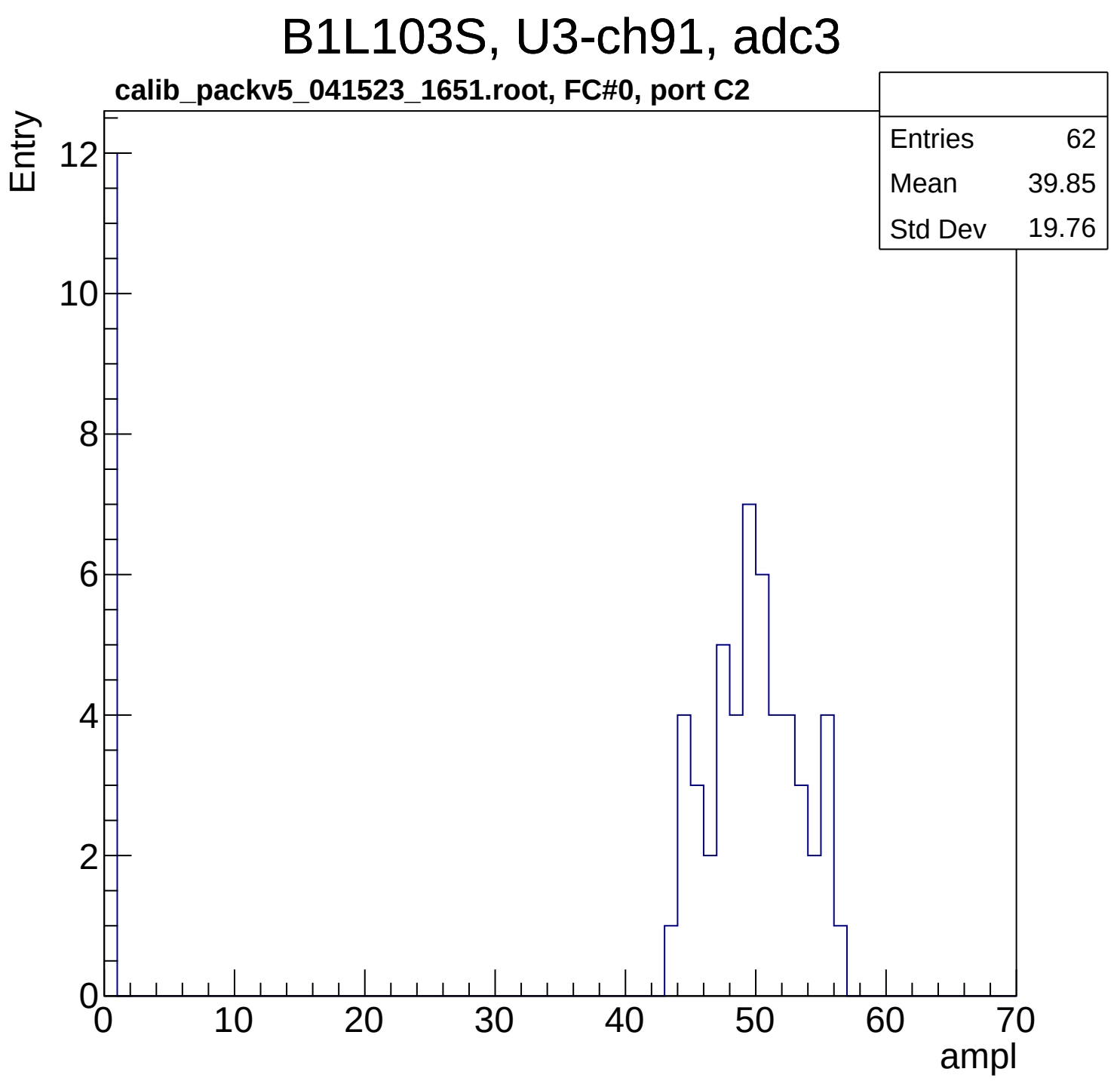
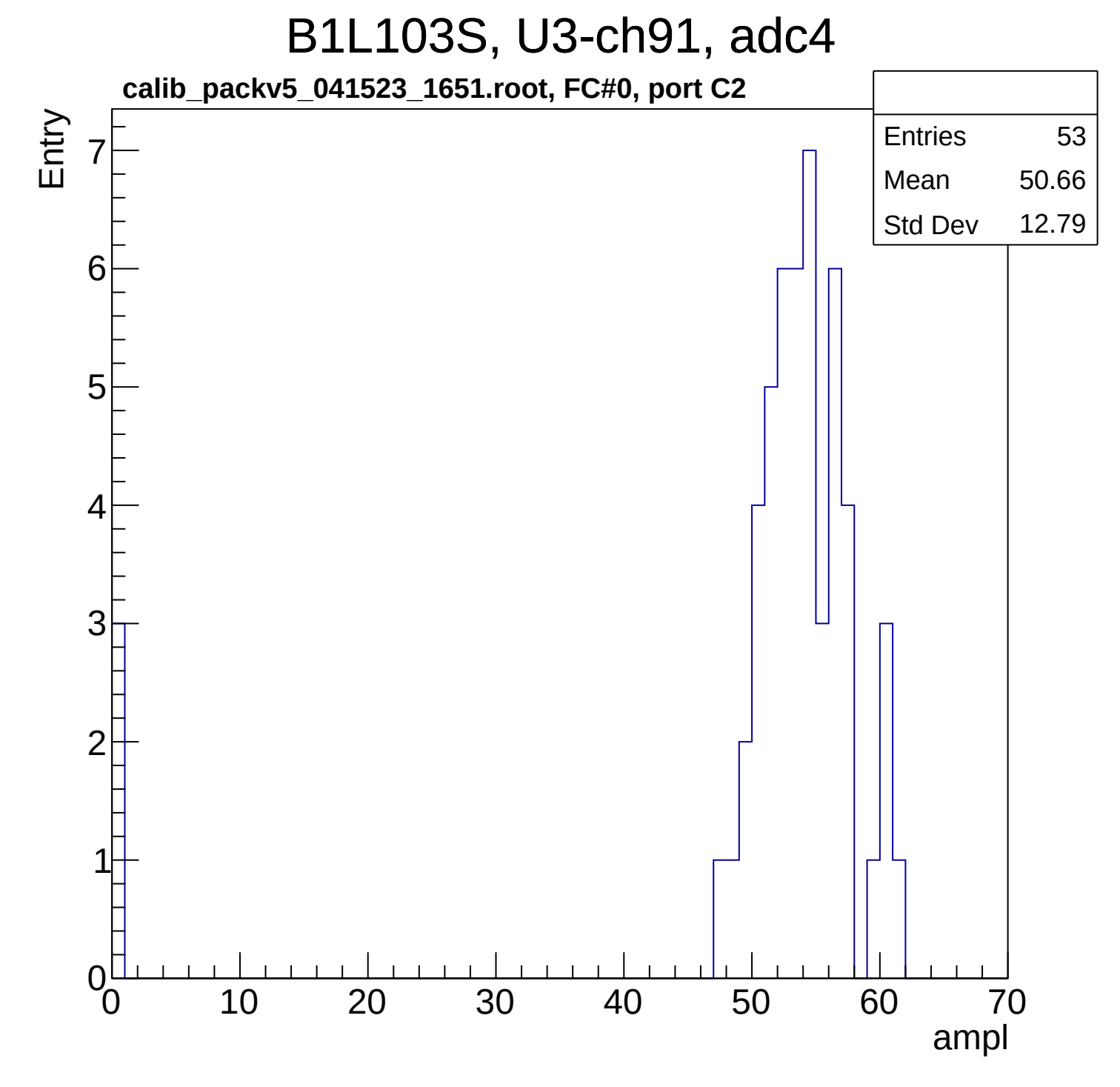
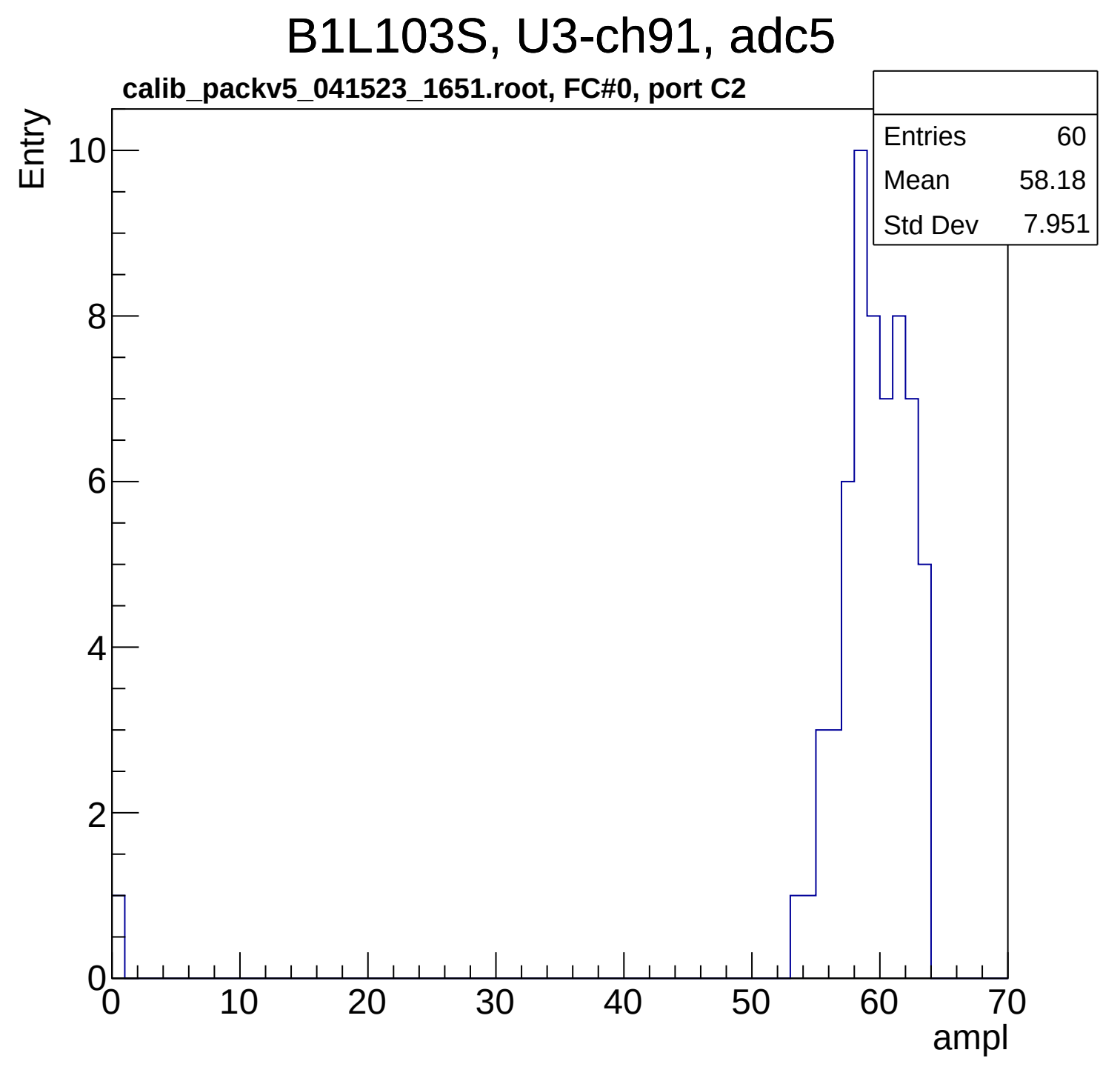
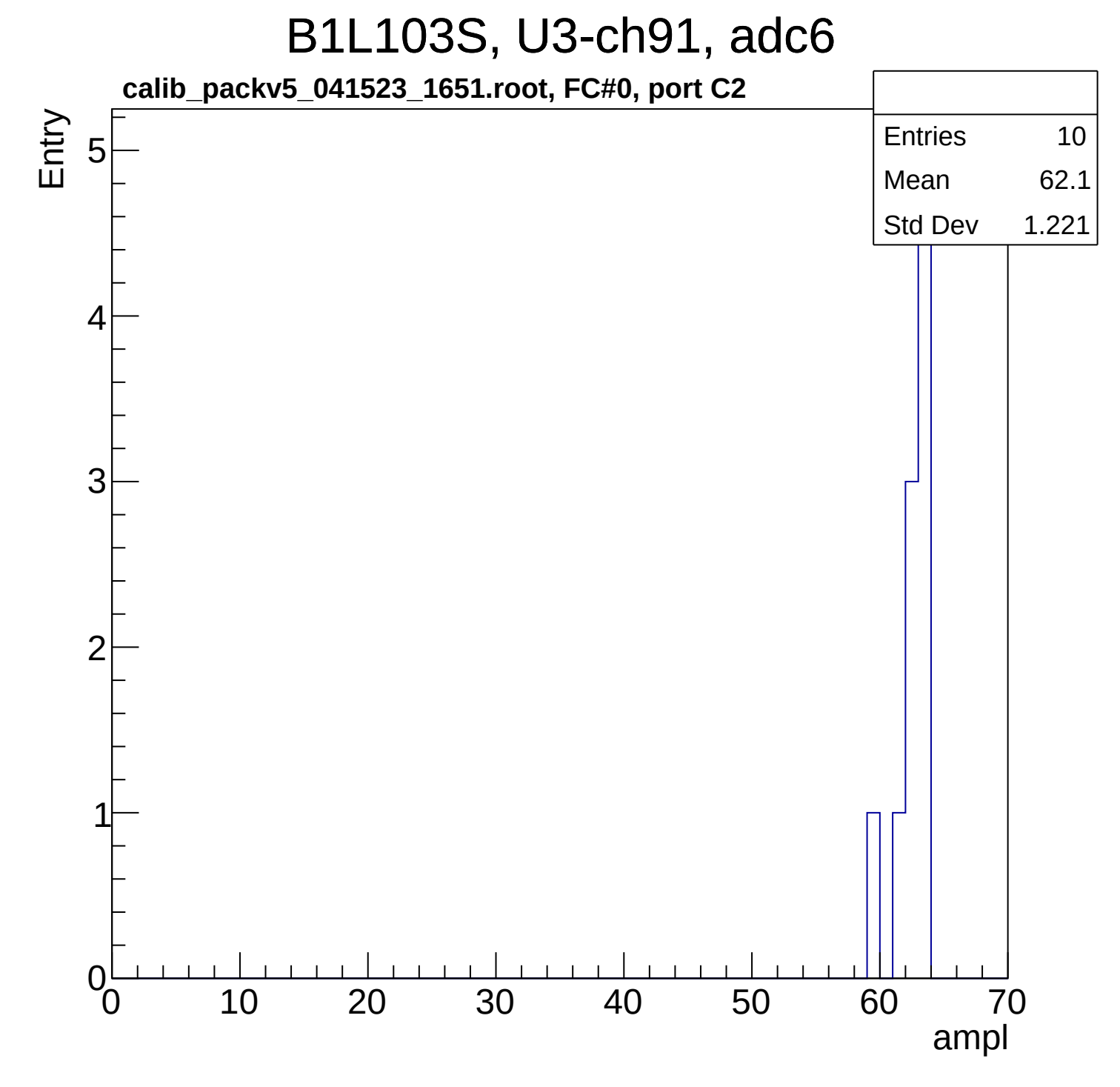
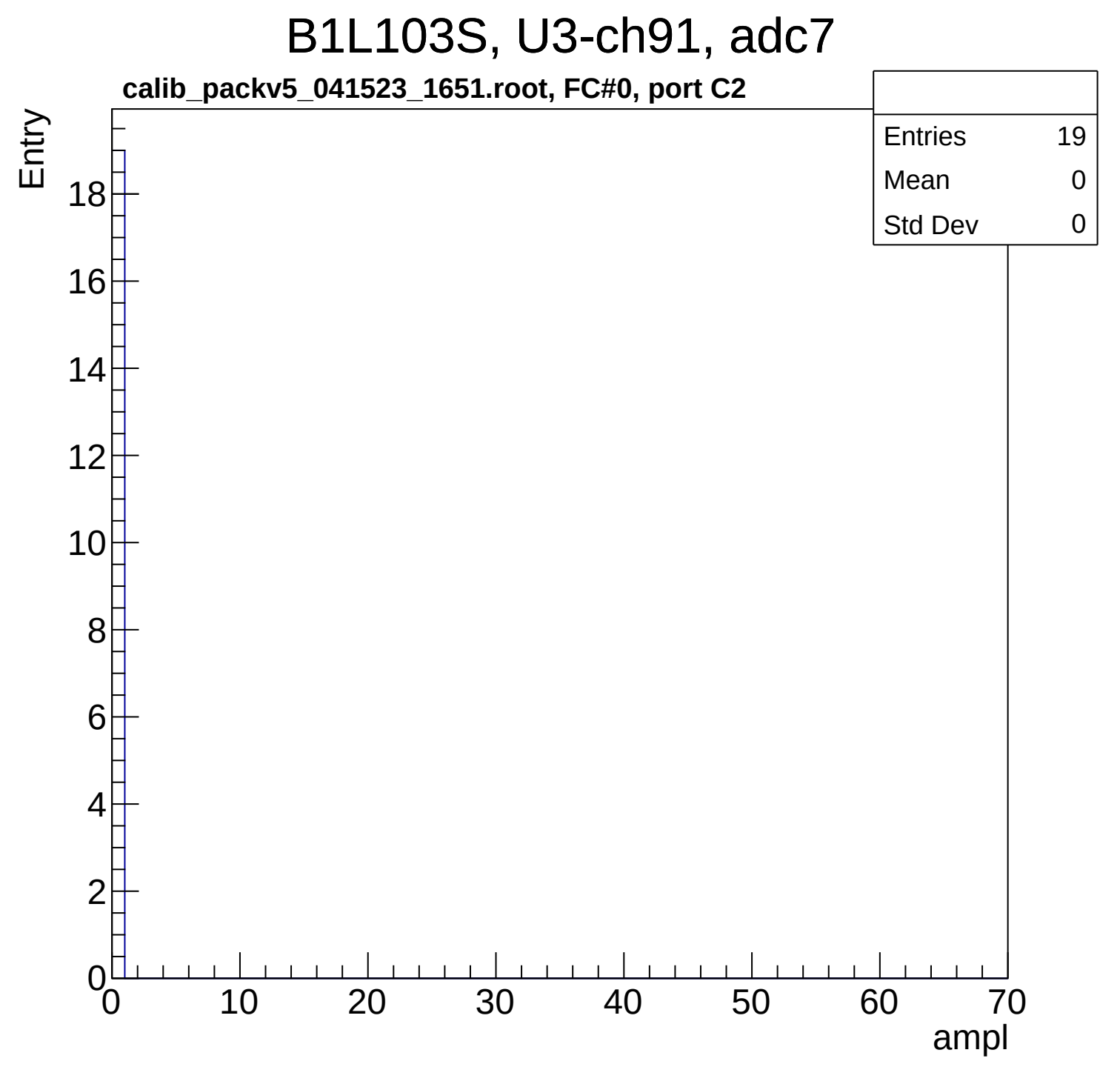
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

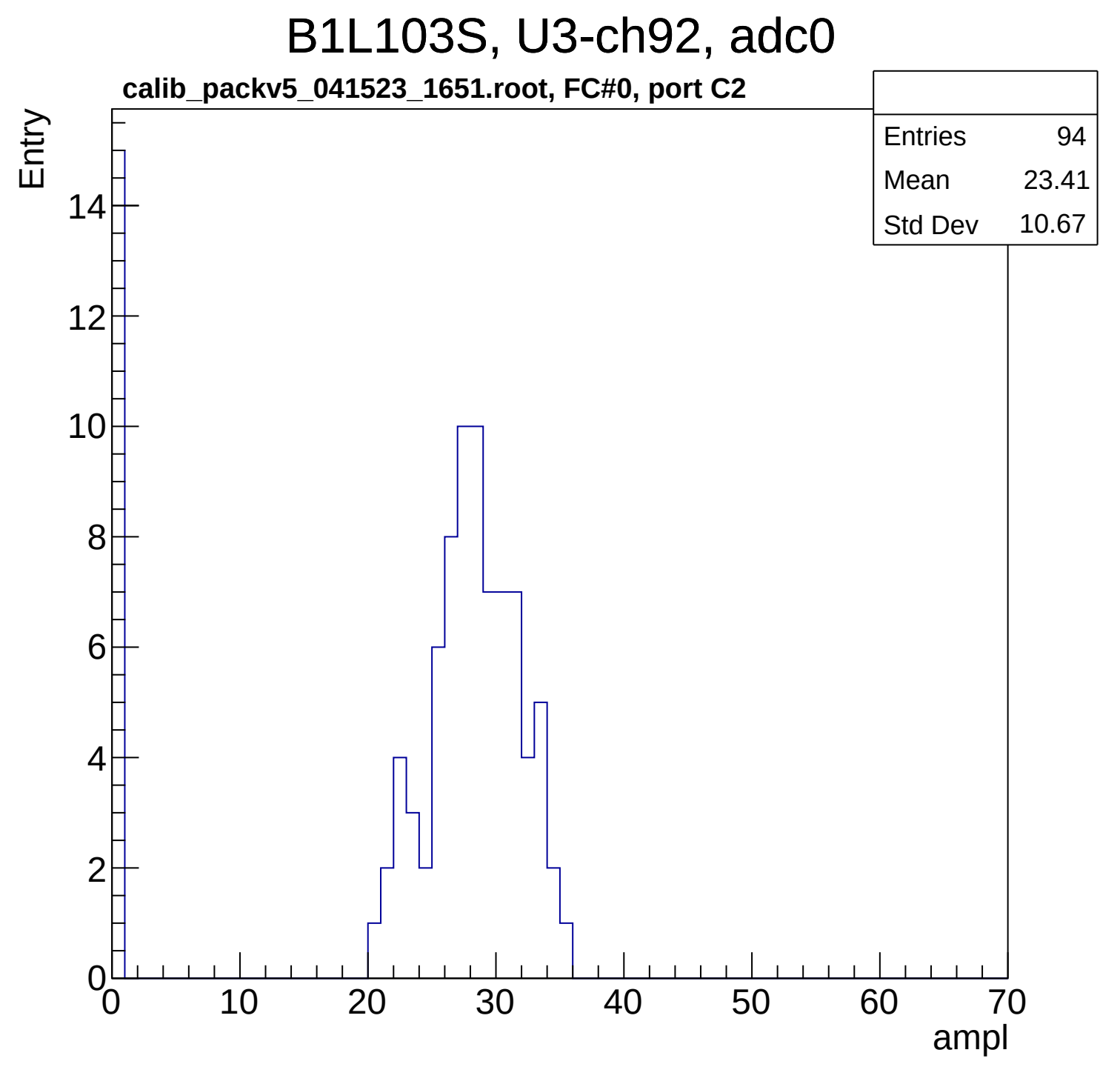

B1L103S, U3-ch91, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 39.85
Std Dev 19.76
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch91, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 50.66
Std Dev 12.79
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch91, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 58.18
Std Dev 7.951
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U3-ch91, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 62.1
Std Dev 1.221
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U3-ch91, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch92, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 23.41
Std Dev 10.67
Entry
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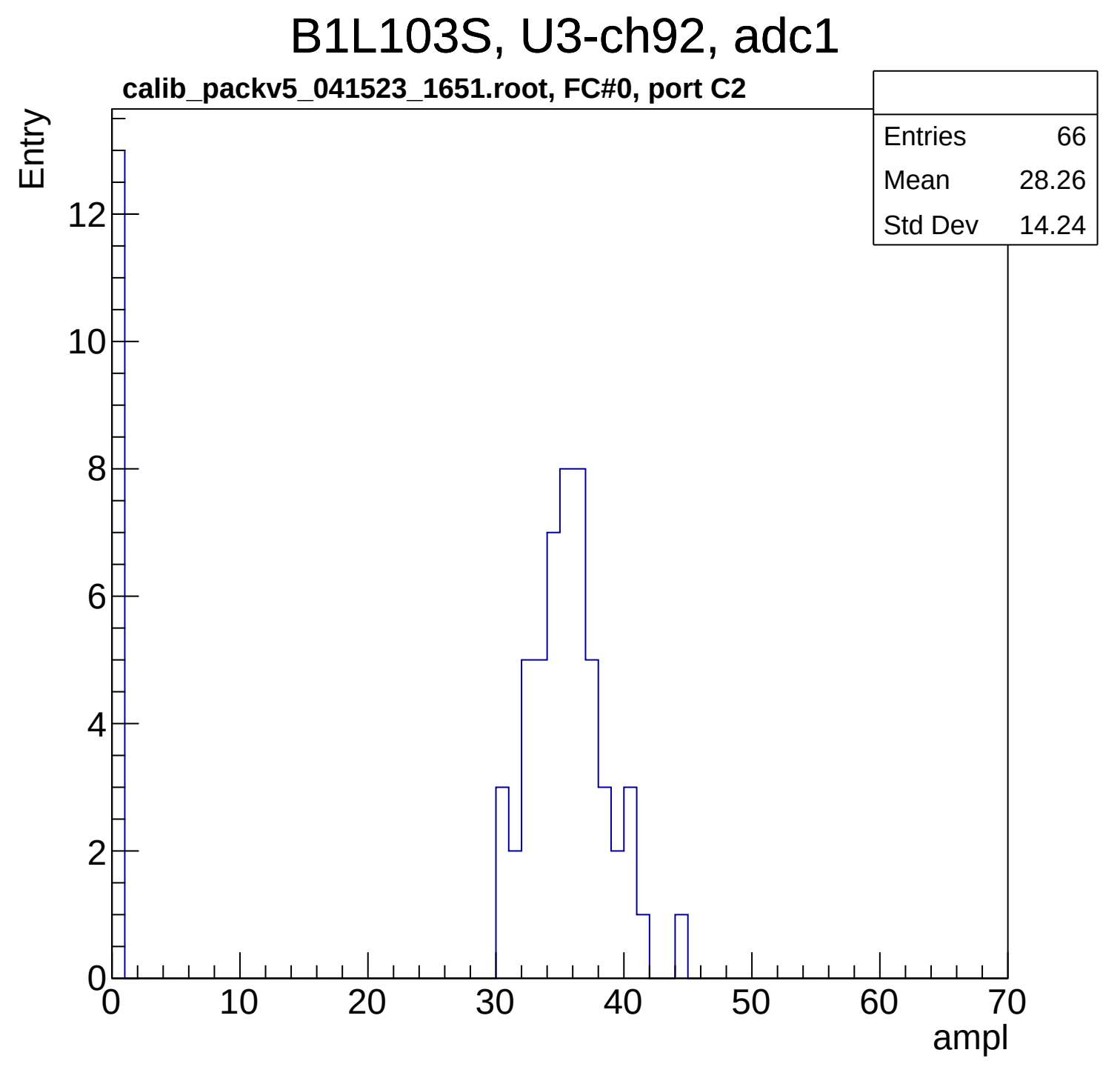
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch92, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 28.26
Std Dev 14.24
Entry
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4
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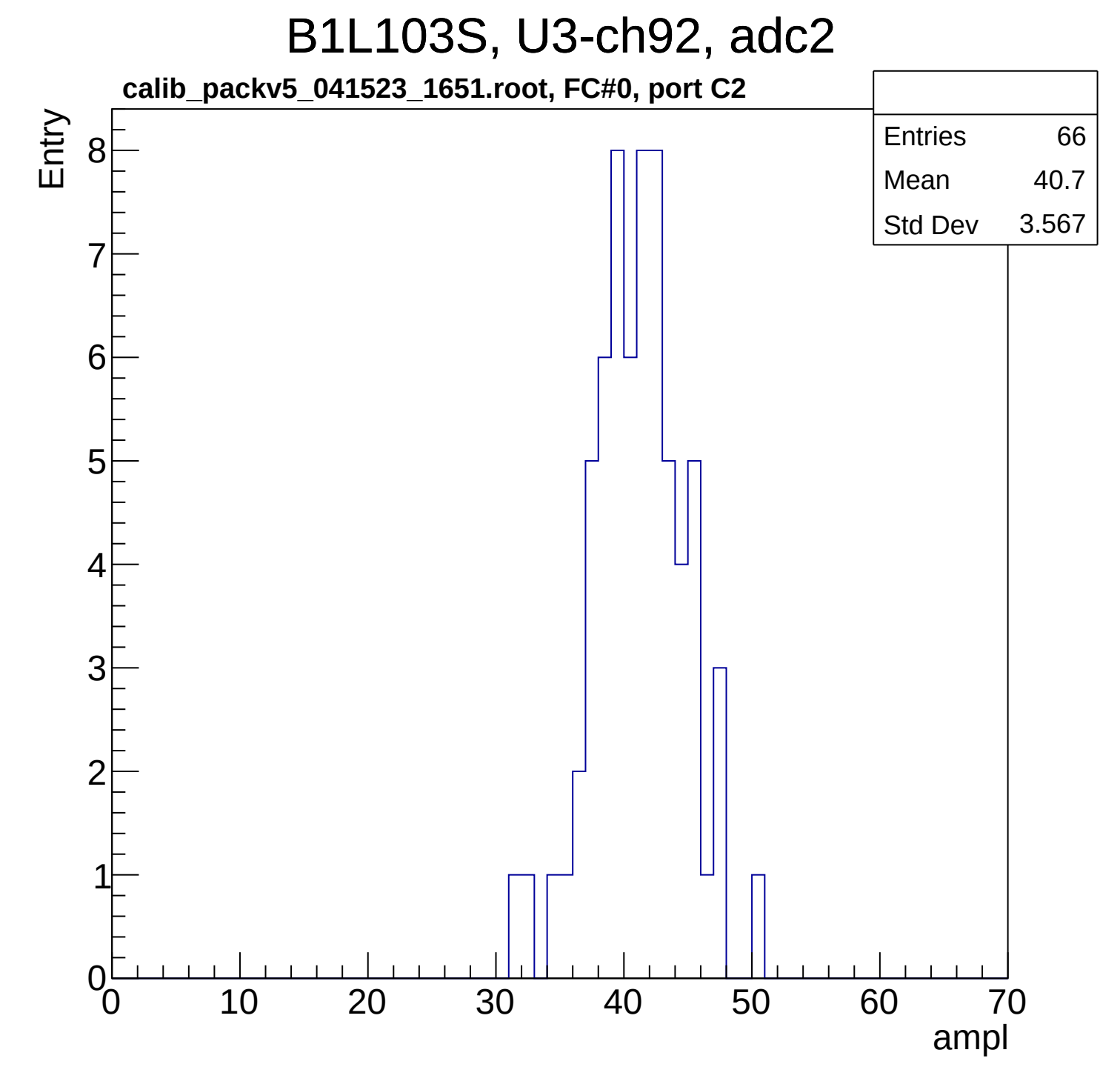
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch92, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 40.7
Std Dev 3.567
Entry
ampl
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1
2
3
4
5
6
7
8
0
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60
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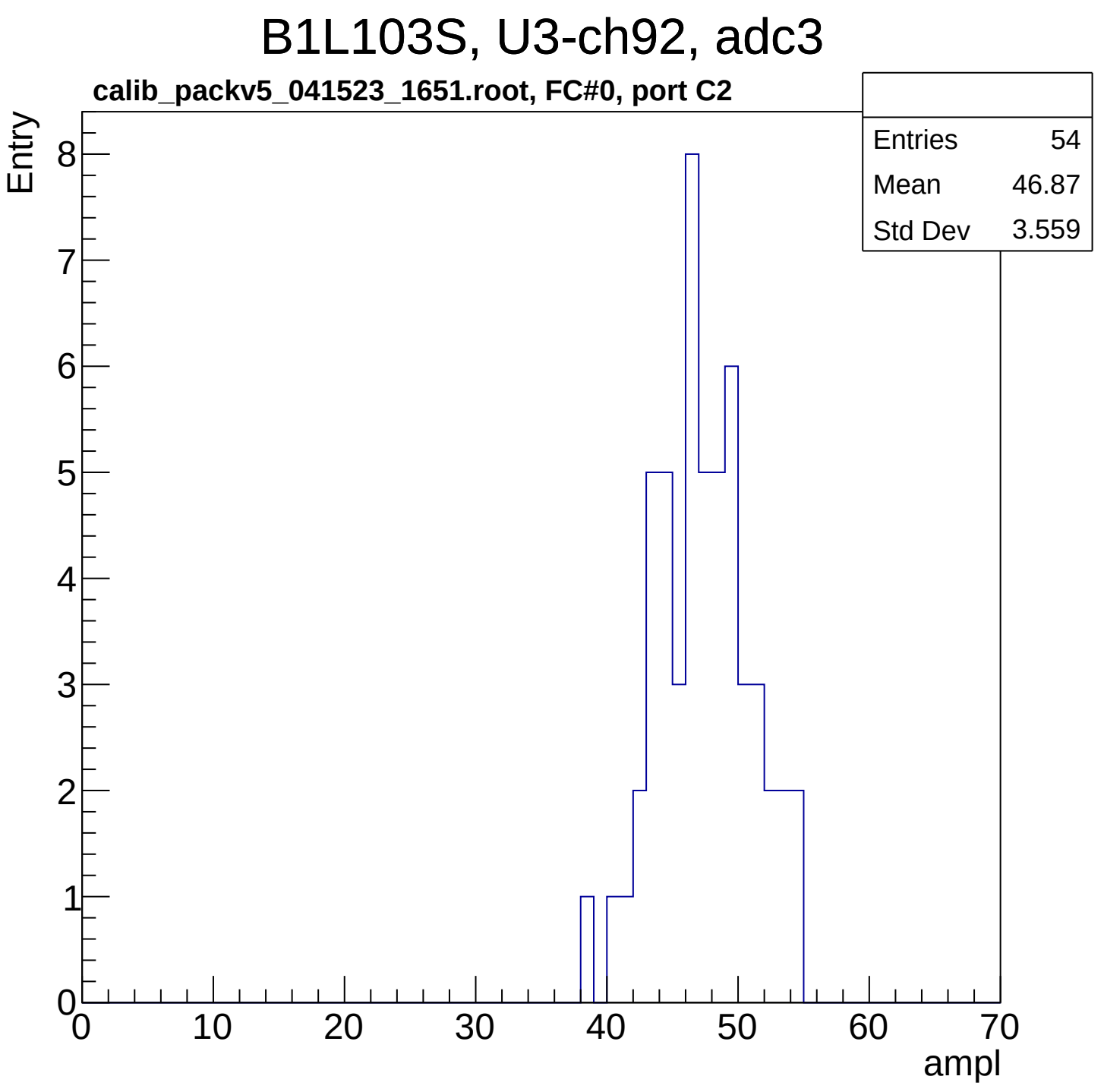
B1L103S, U3-ch92, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 46.87
Std Dev 3.559
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
50
60
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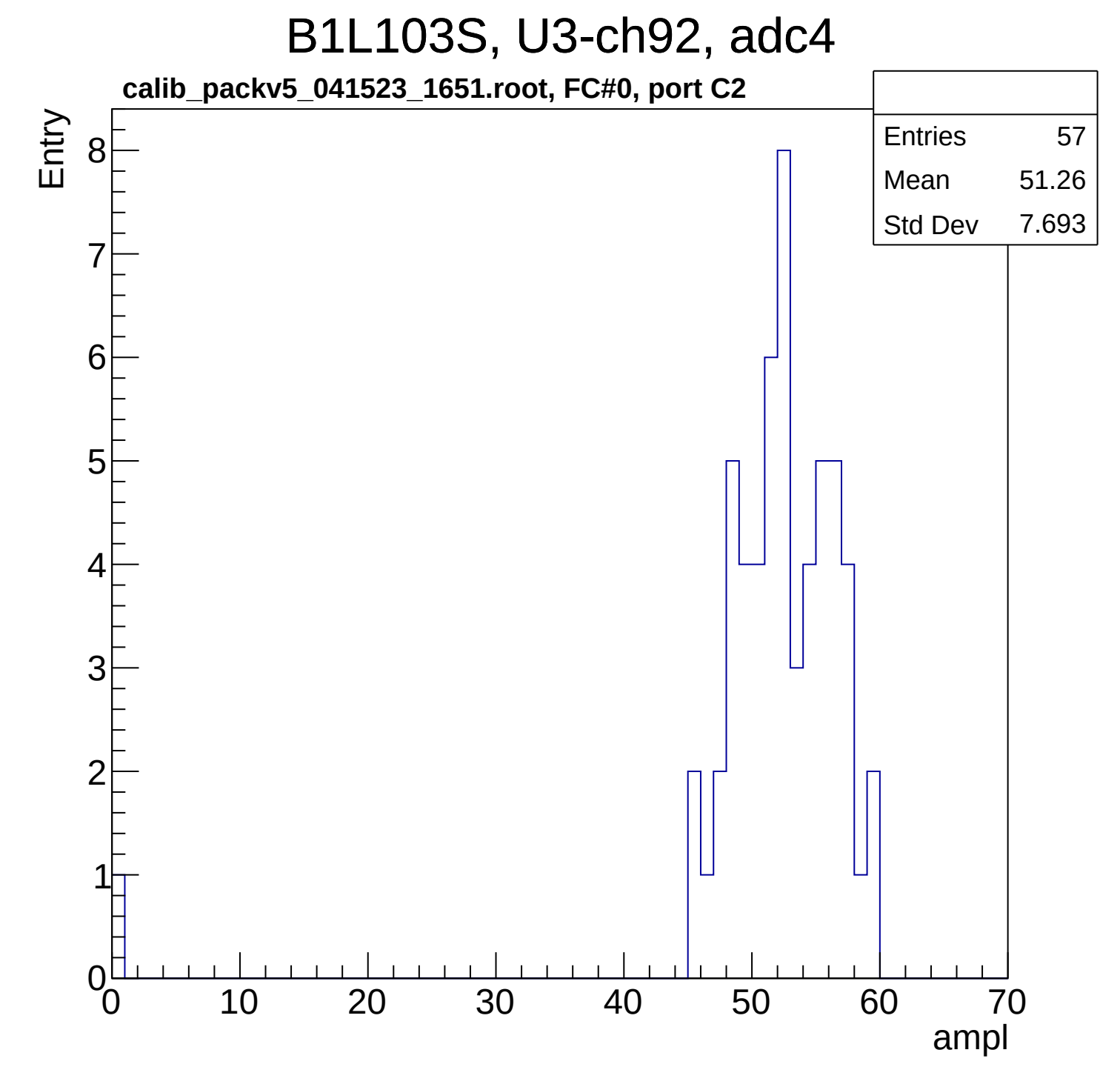
B1L103S, U3-ch92, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 51.26
Std Dev 7.693
Entry
ampl
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2
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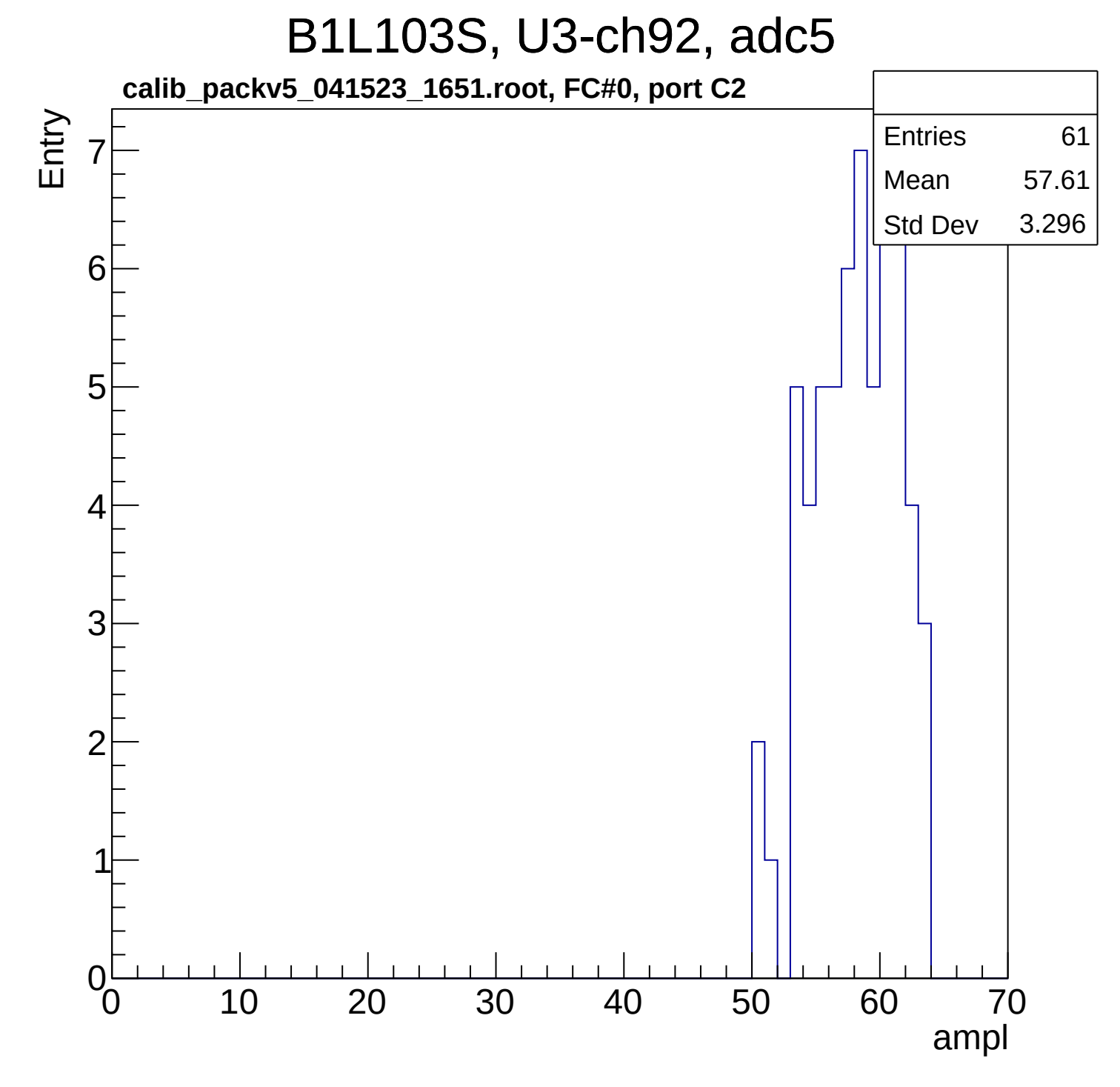
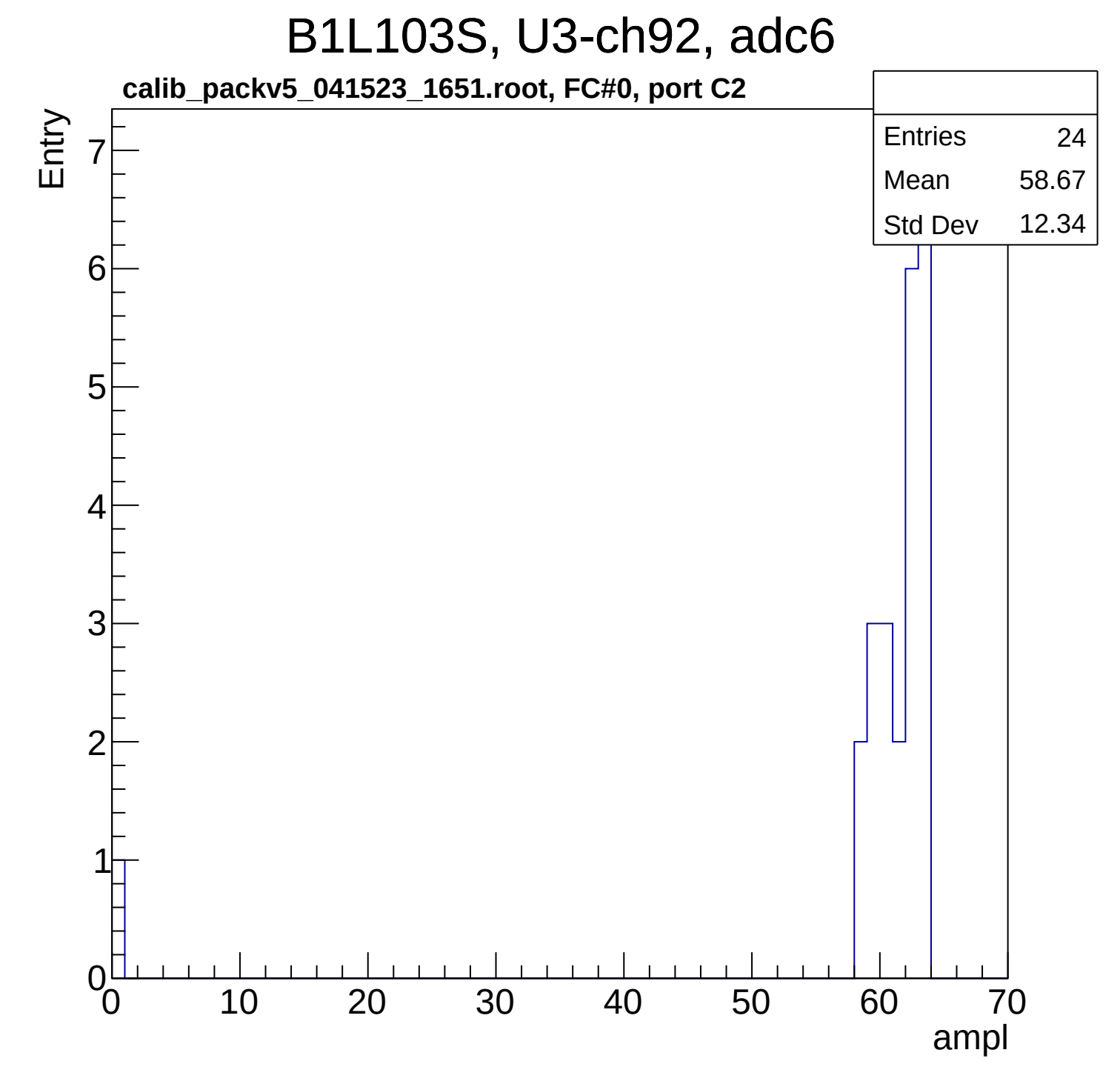
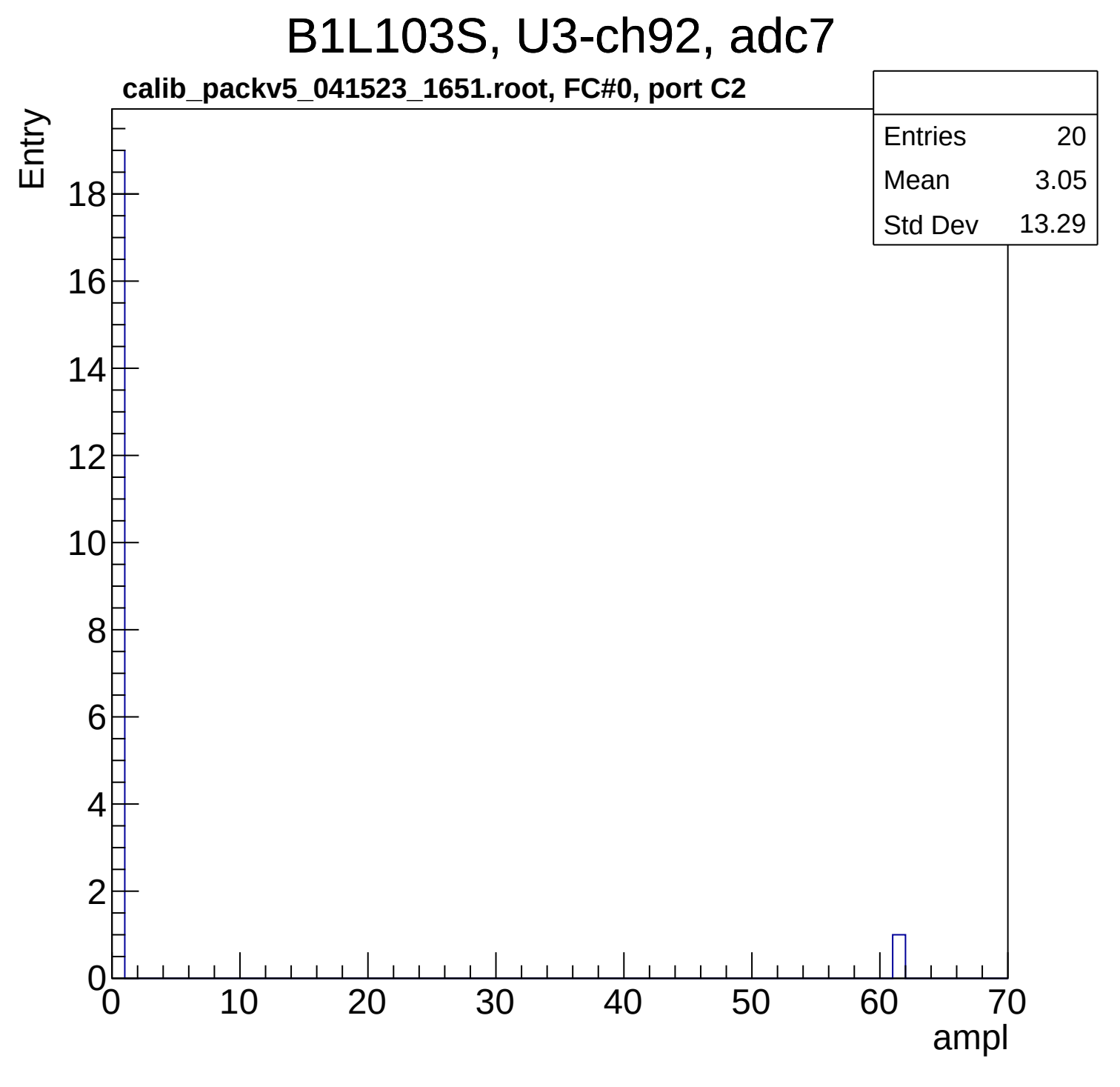
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch92, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 57.61
Std Dev 3.296
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch92, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 58.67
Std Dev 12.34
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch92, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.05
Std Dev 13.29
Entry
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6
8
10
12
14
16
18
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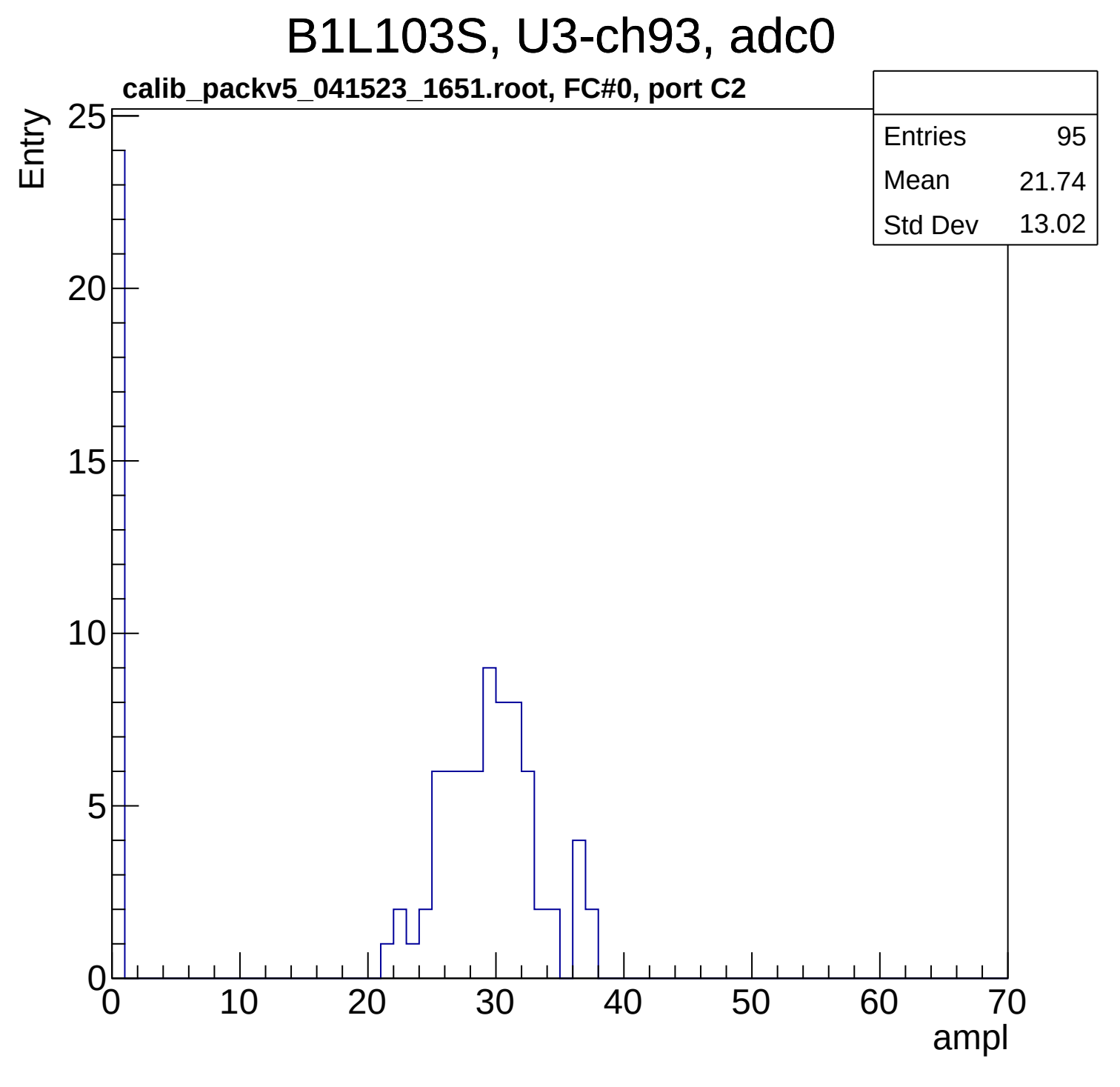
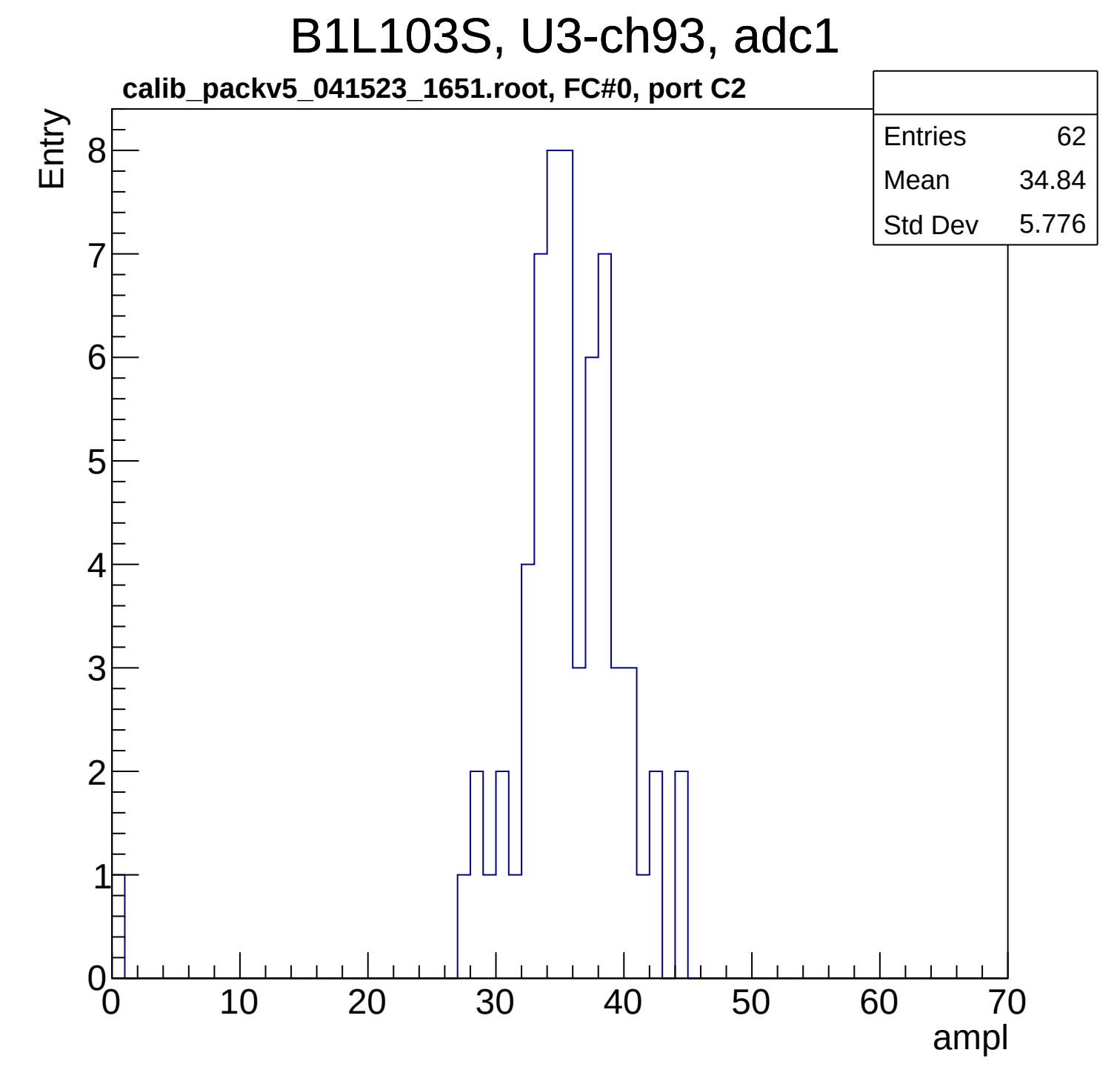
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch93, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 21.74
Std Dev 13.02
Entry
ampl
0
5
10
15
20
25
0
10
20
30
40
50
60
70


B1L103S, U3-ch93, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 34.84
Std Dev 5.776
Entry
ampl
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2
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4
5
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7
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0
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60
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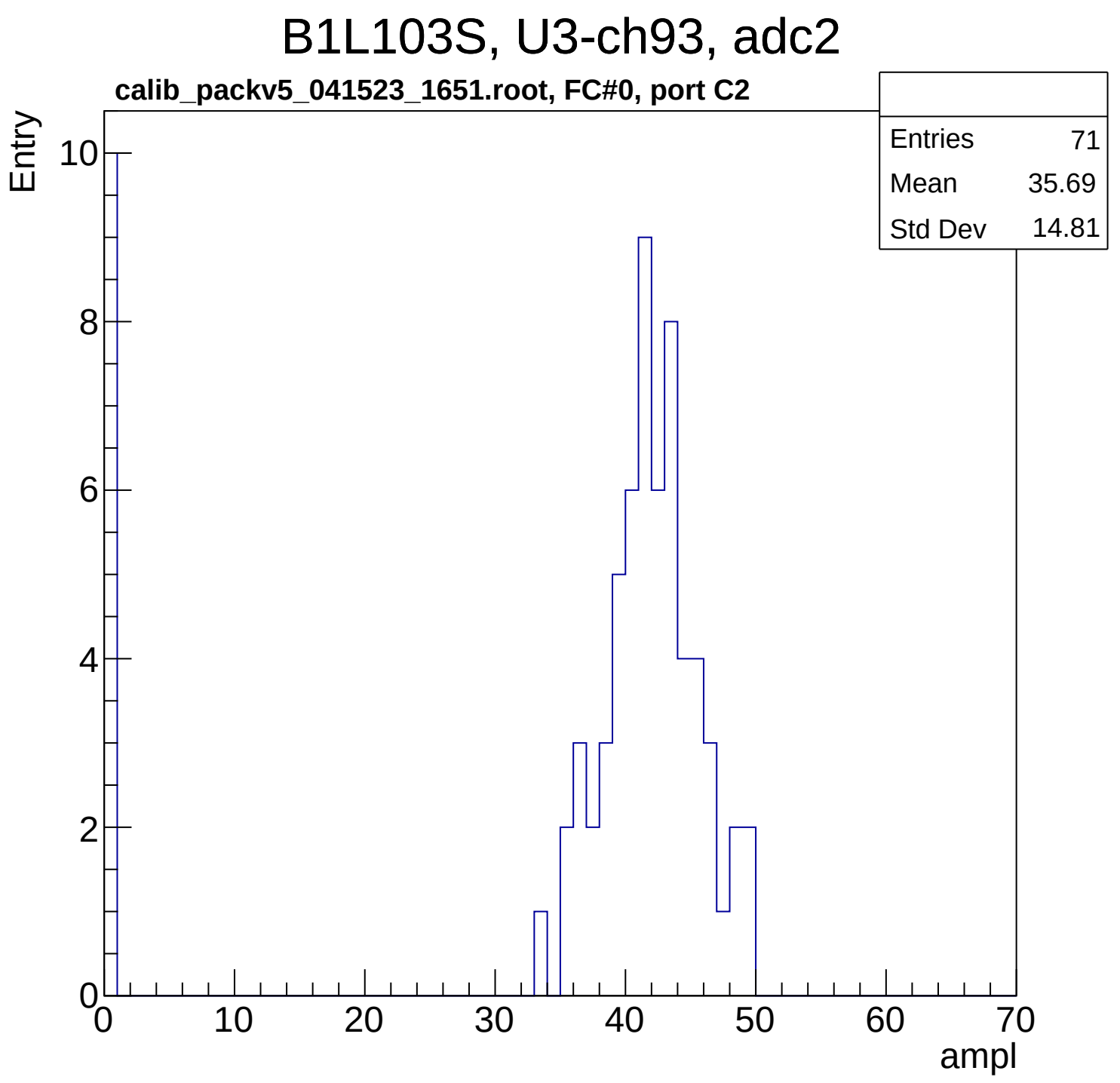
B1L103S, U3-ch93, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 35.69
Std Dev 14.81
Entry
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2
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6
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10
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10
20
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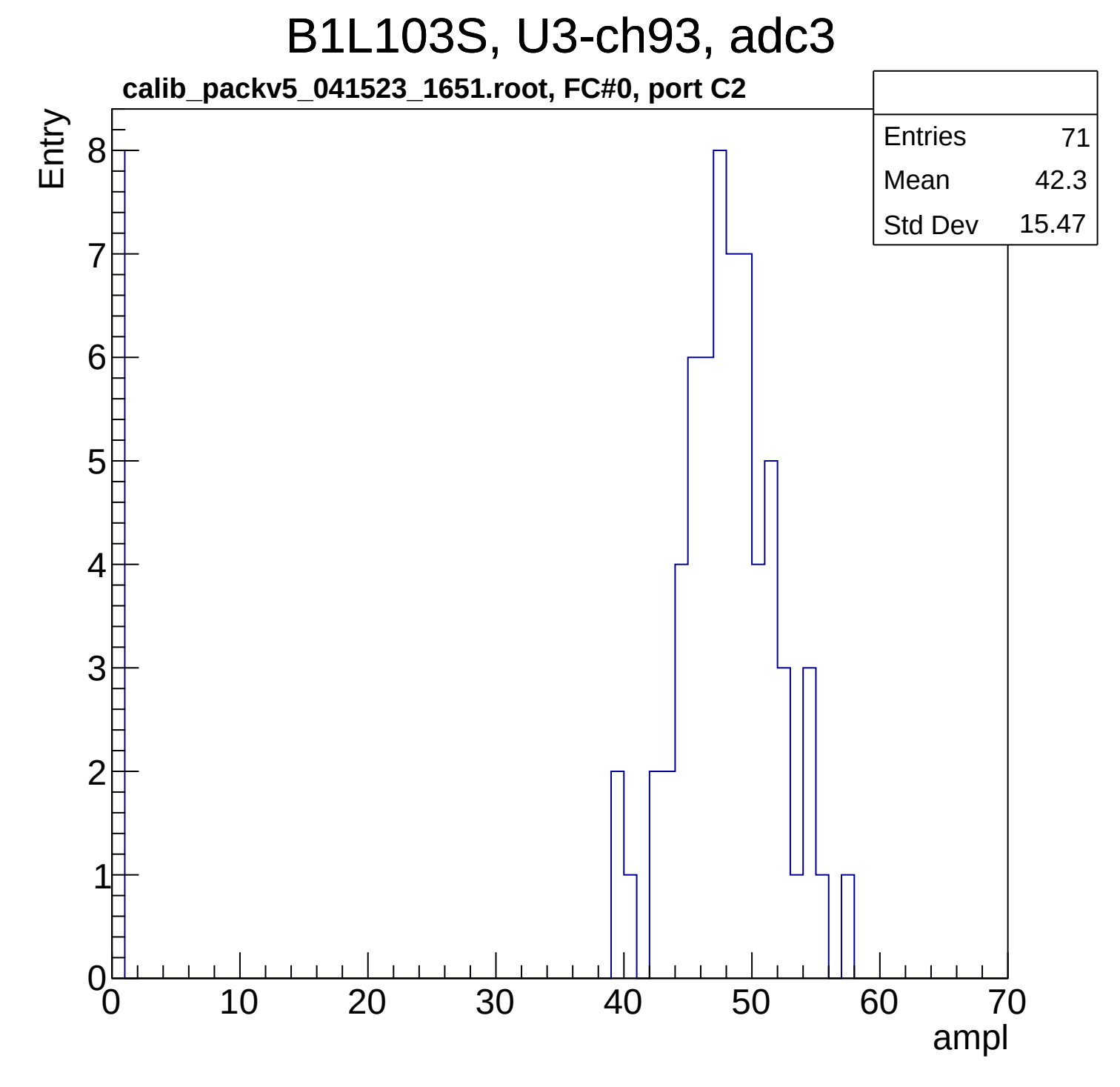
50
60
70
ampl


B1L103S, U3-ch93, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 42.3
Std Dev 15.47
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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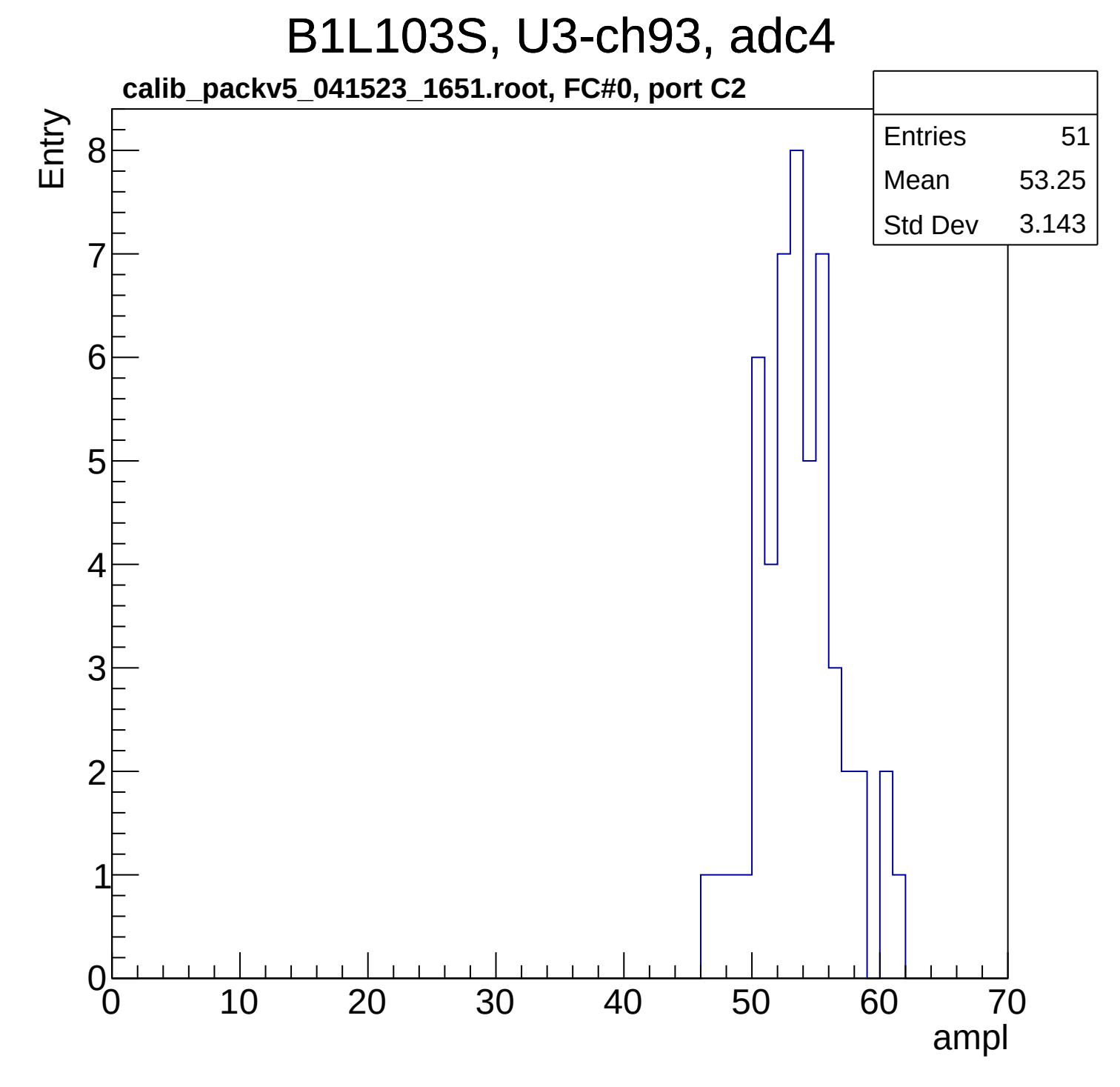
B1L103S, U3-ch93, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 53.25
Std Dev 3.143
Entry
ampl
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2
3
4
5
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7
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0
10
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60
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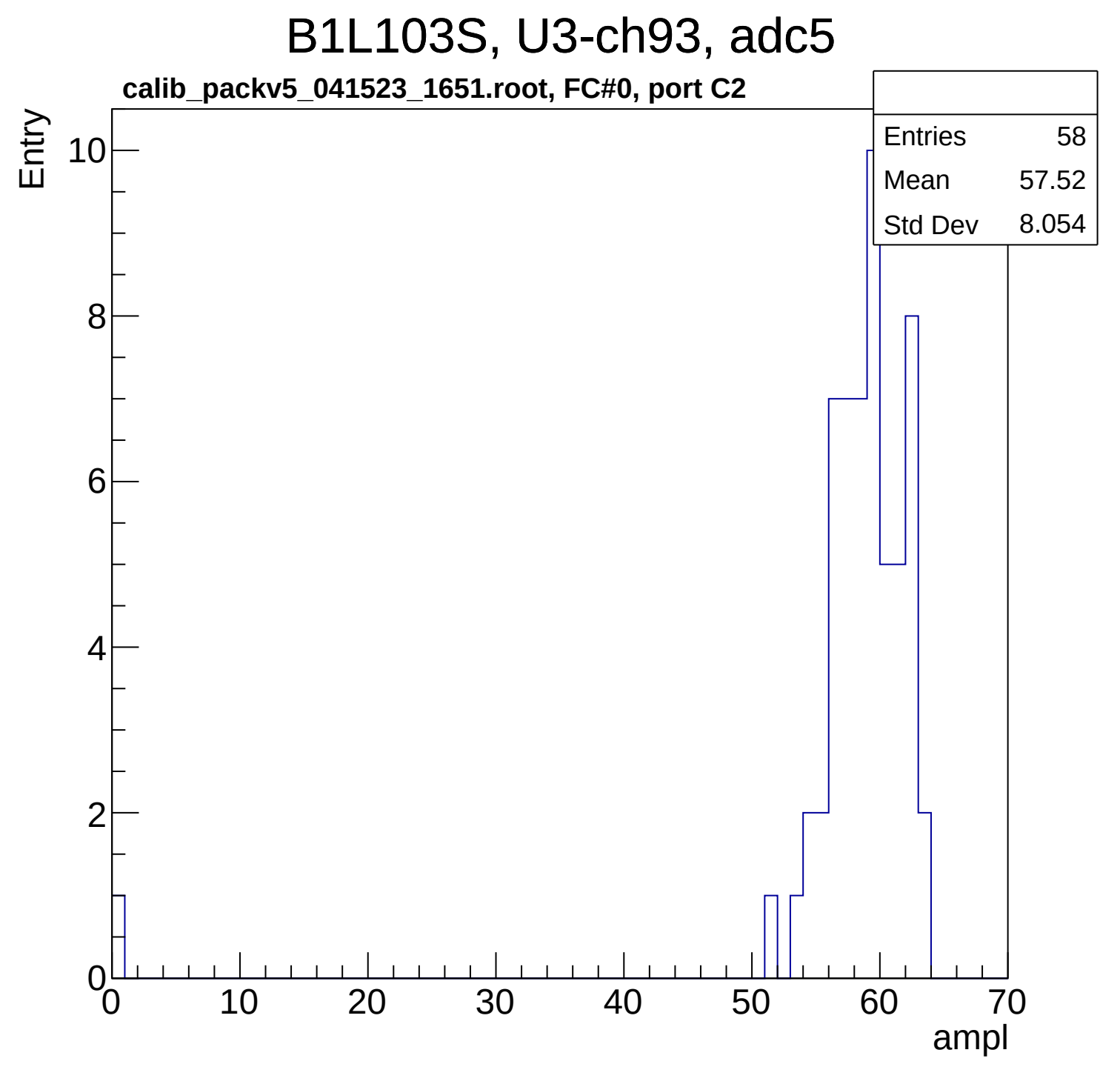
B1L103S, U3-ch93, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 57.52
Std Dev 8.054
Entry
ampl
0
2
4
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8
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0
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40
50
60
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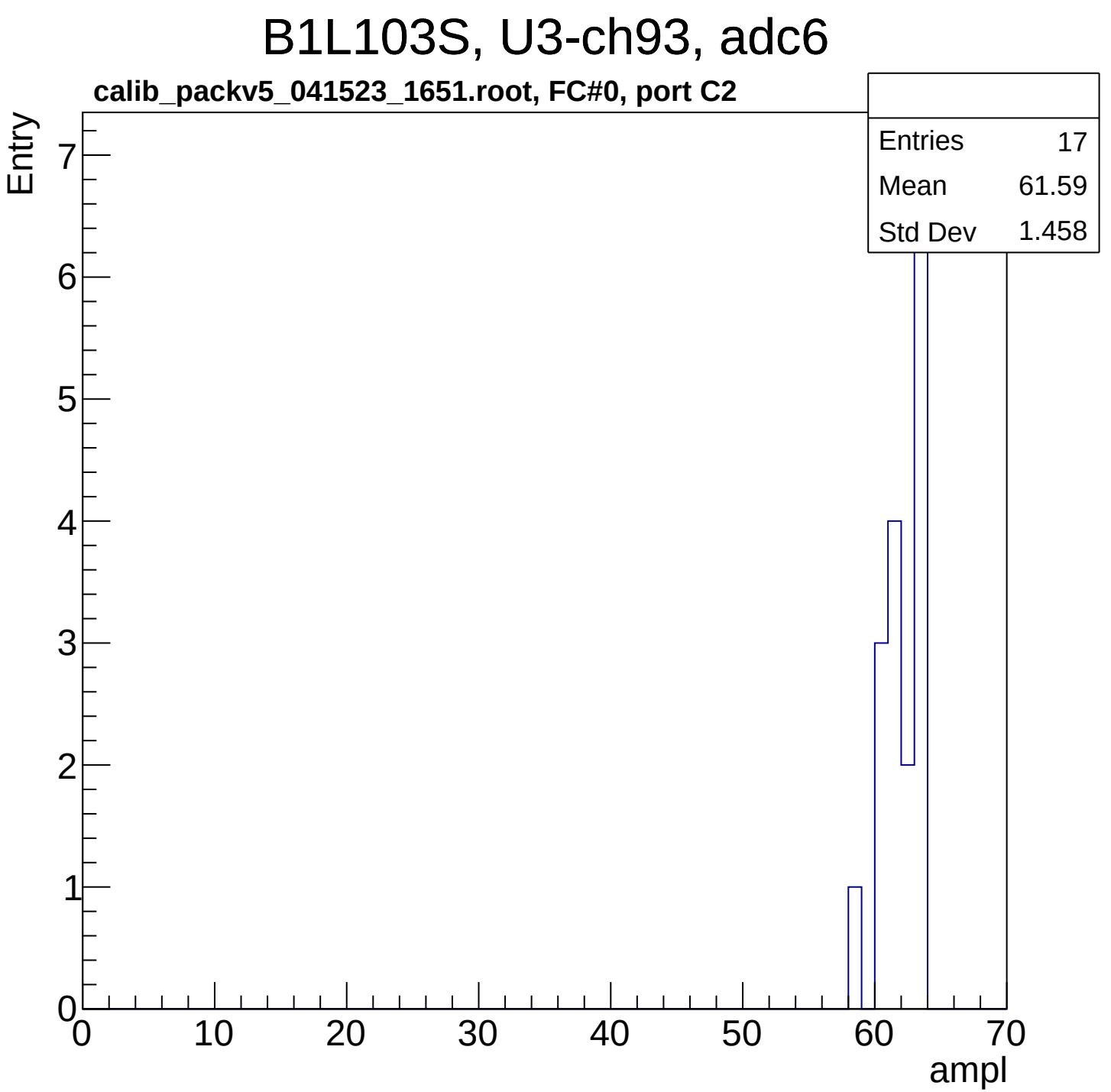
B1L103S, U3-ch93, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 61.59
Std Dev 1.458
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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40
50
60
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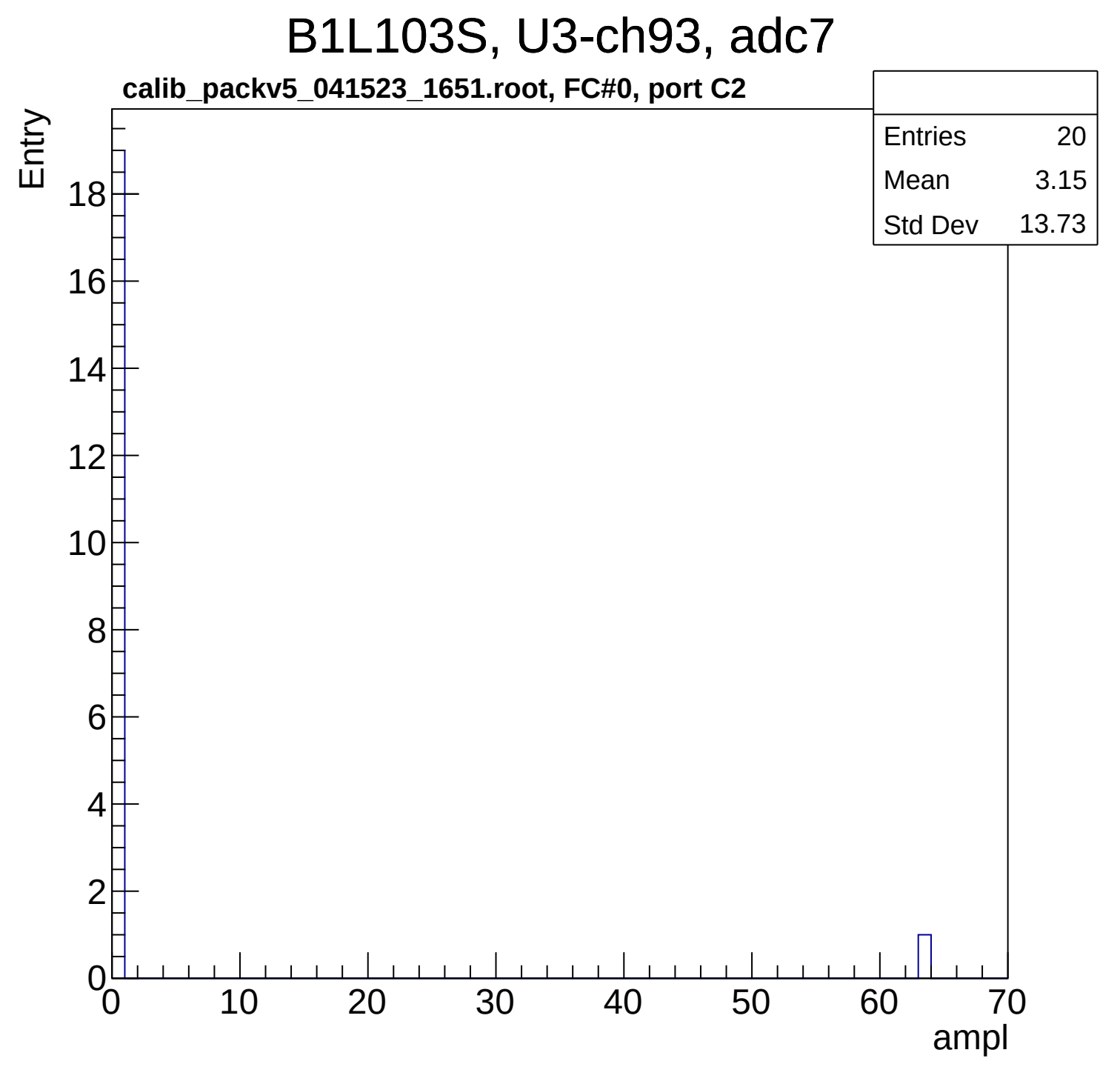
B1L103S, U3-ch93, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
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8
10
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14
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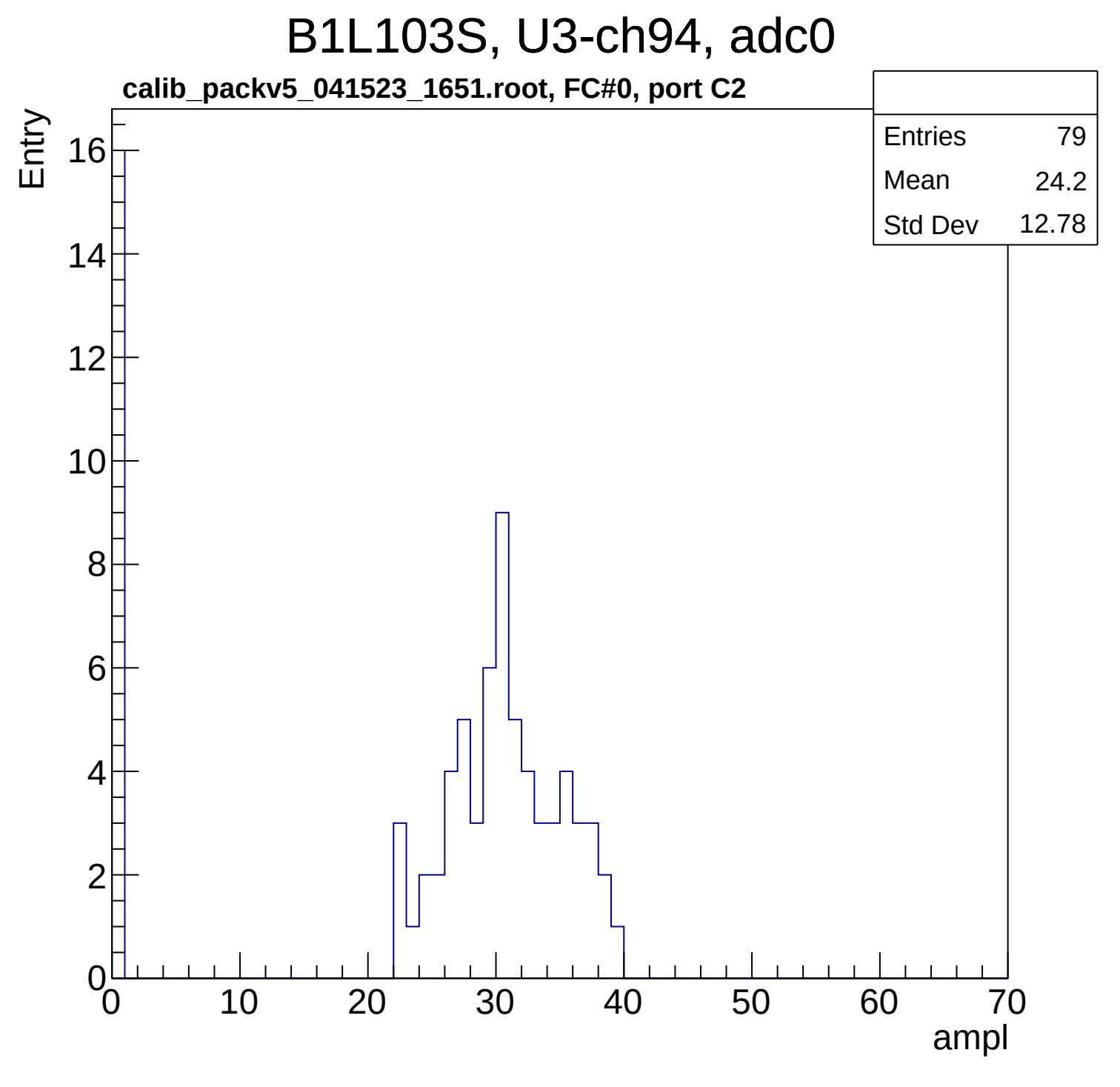
70
ampl


B1L103S, U3-ch94, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 24.2
Std Dev 12.78
Entry
ampl
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2
4
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10
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14
16
0
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40
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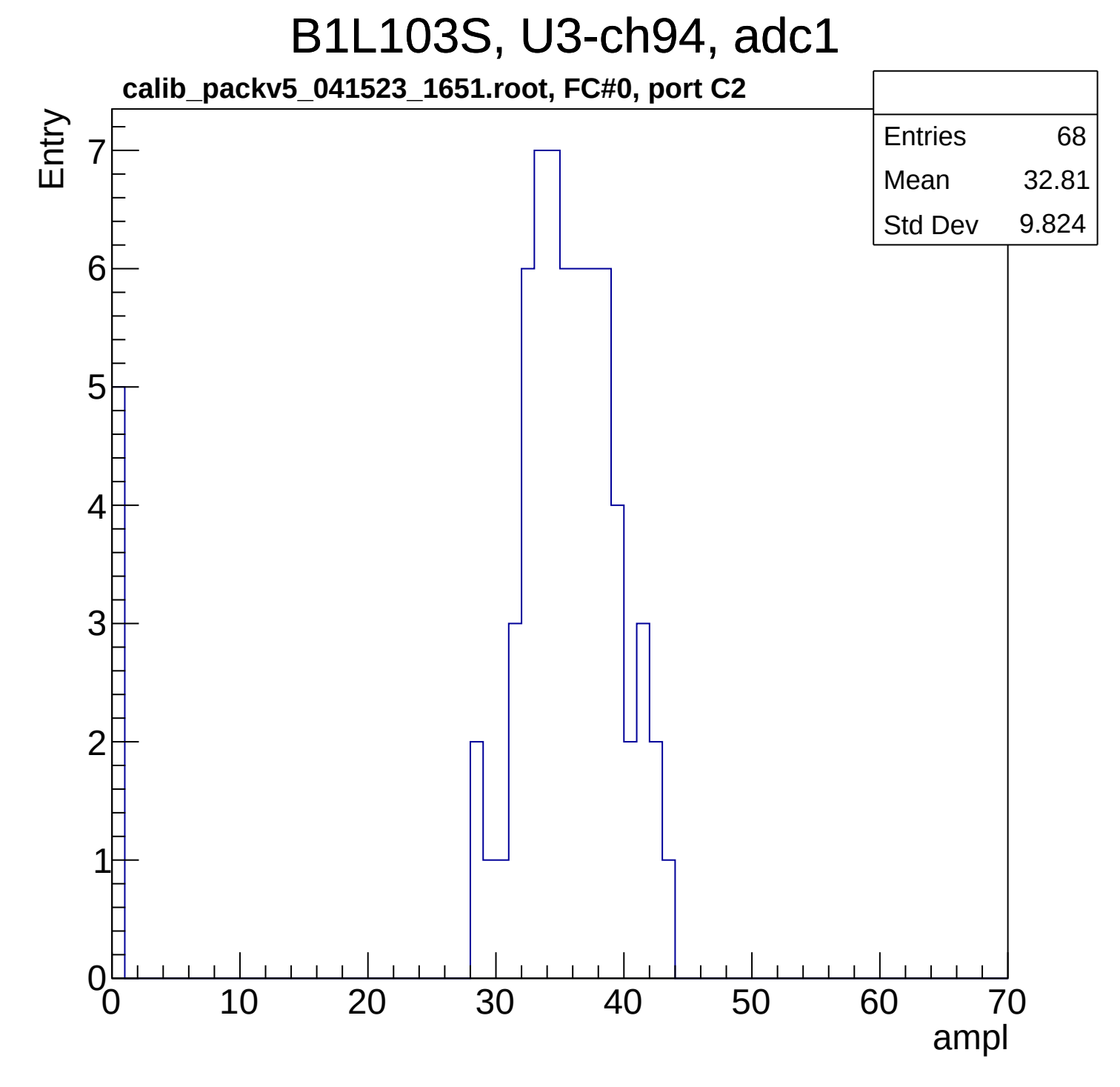
B1L103S, U3-ch94, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 32.81
Std Dev 9.824
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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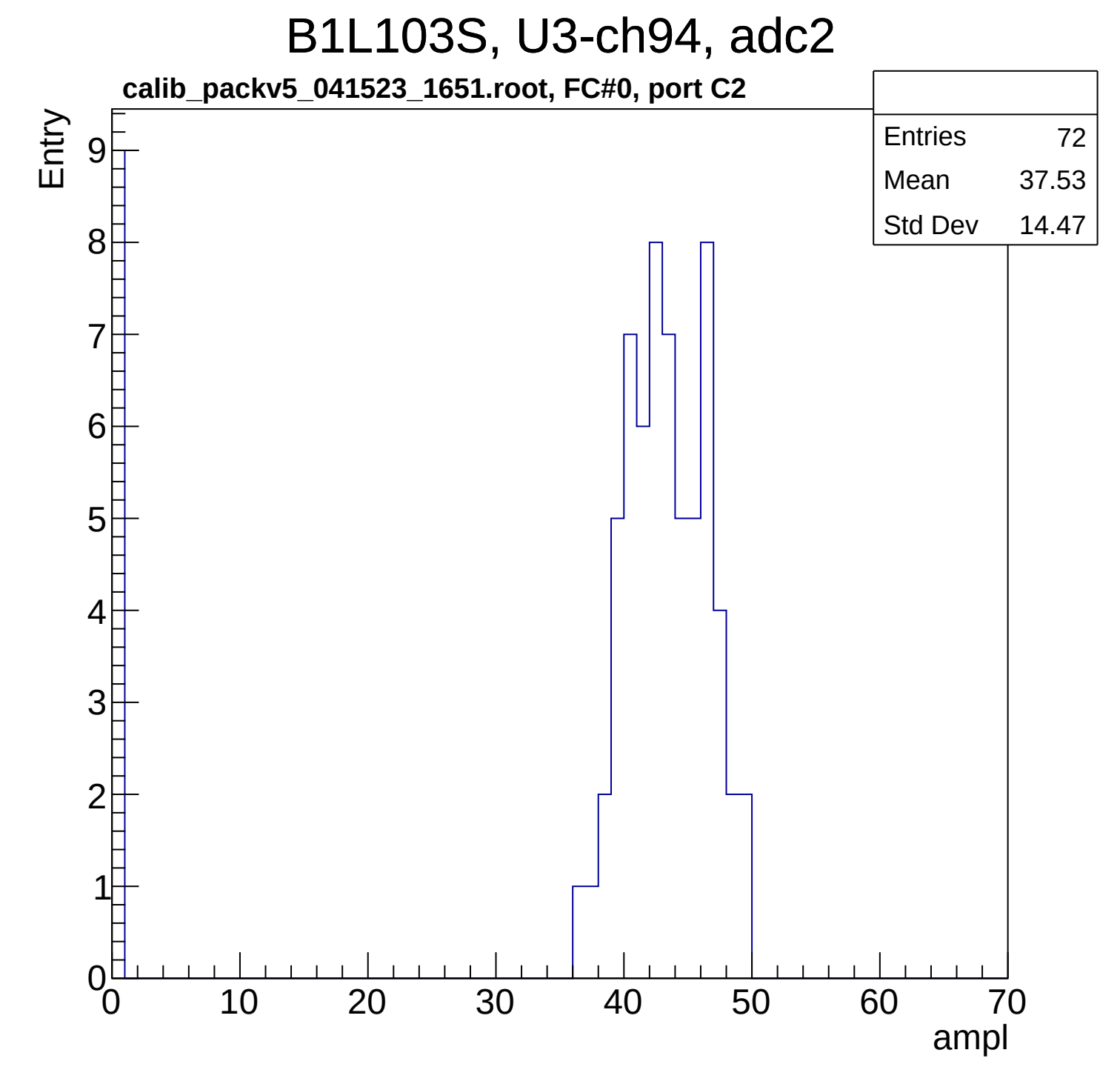
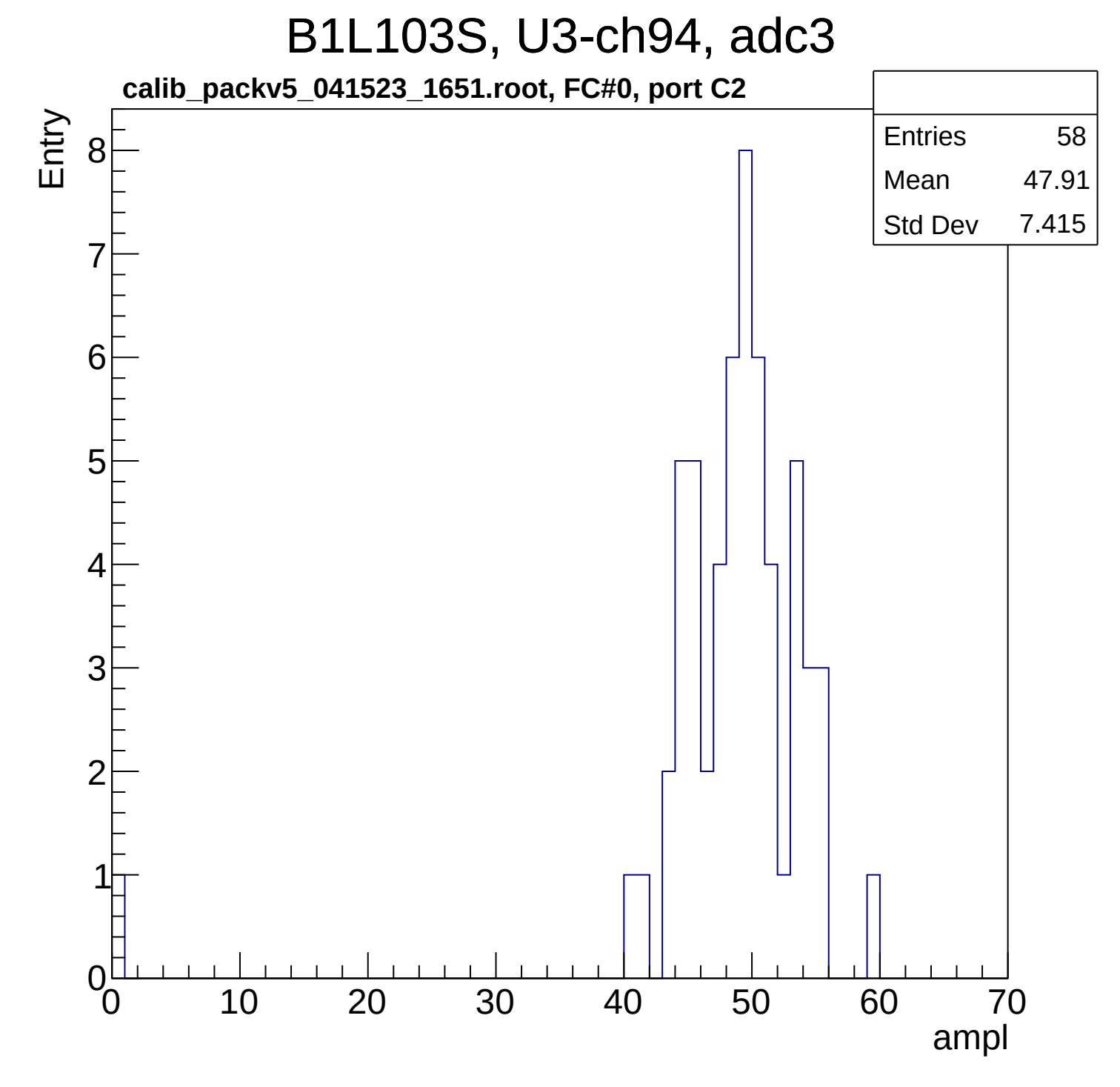
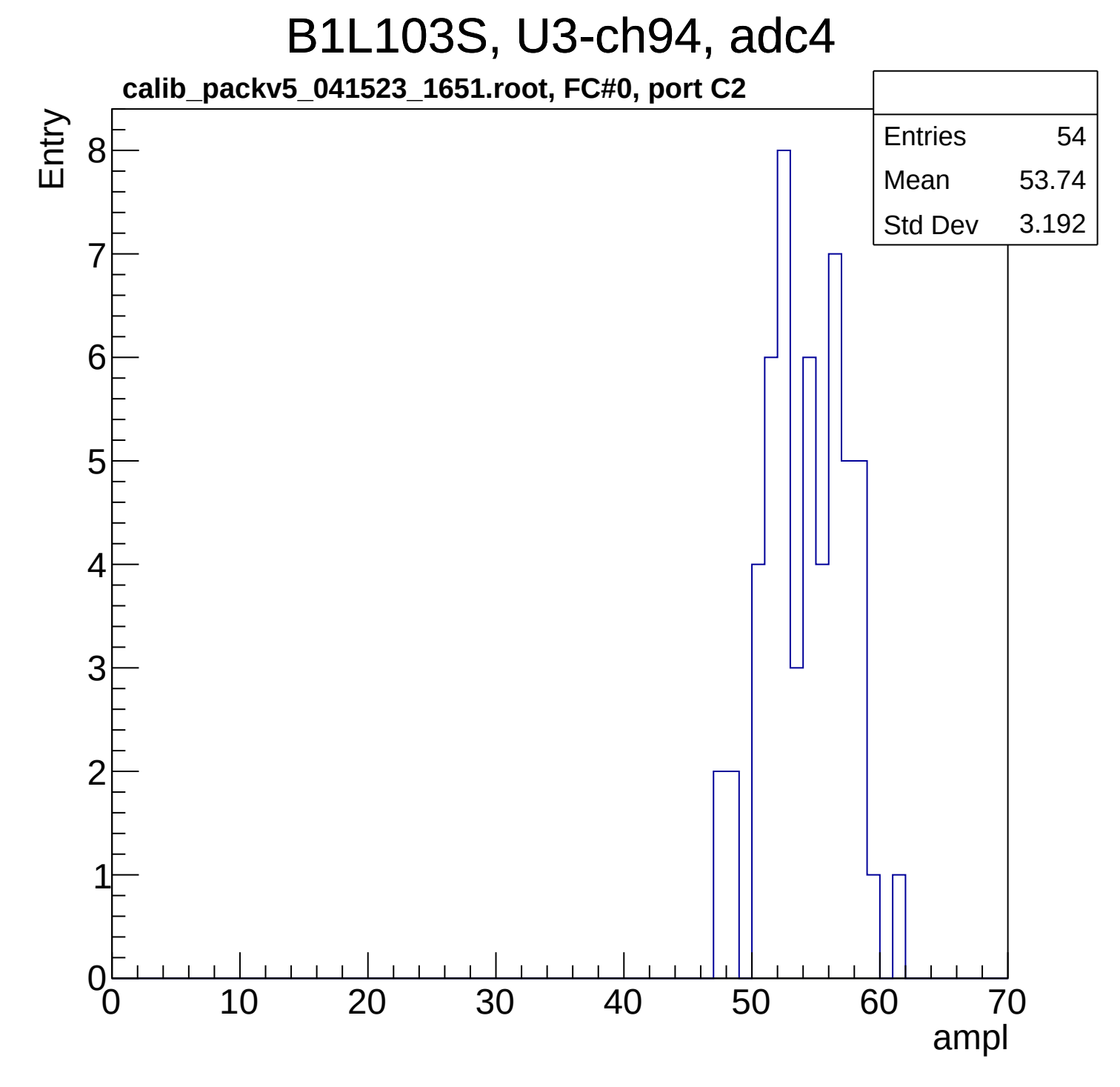

B1L103S, U3-ch94, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 37.53
Std Dev 14.47
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch94, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 47.91
Std Dev 7.415
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch94, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 53.74
Std Dev 3.192
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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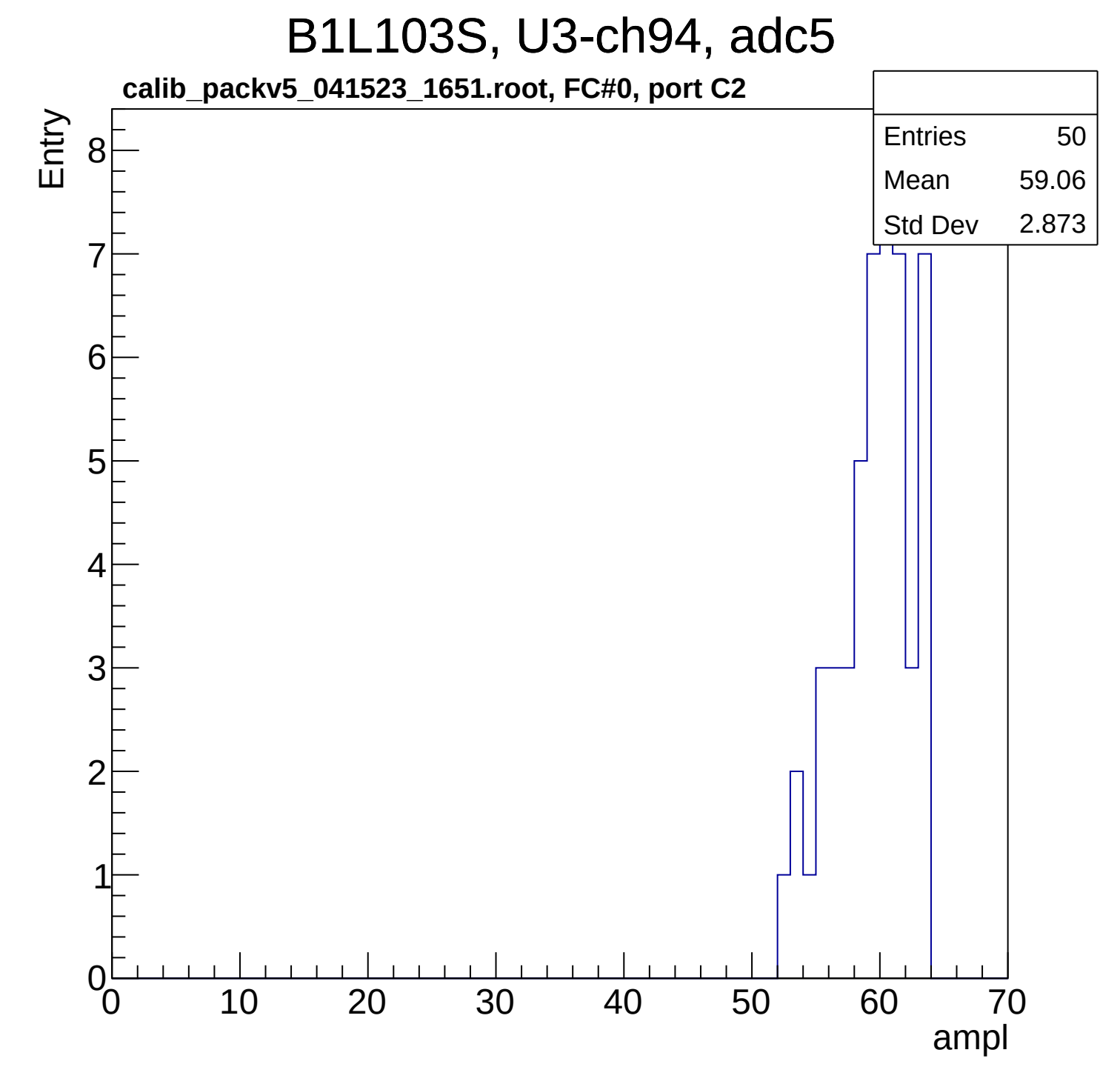
B1L103S, U3-ch94, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 59.06
Std Dev 2.873
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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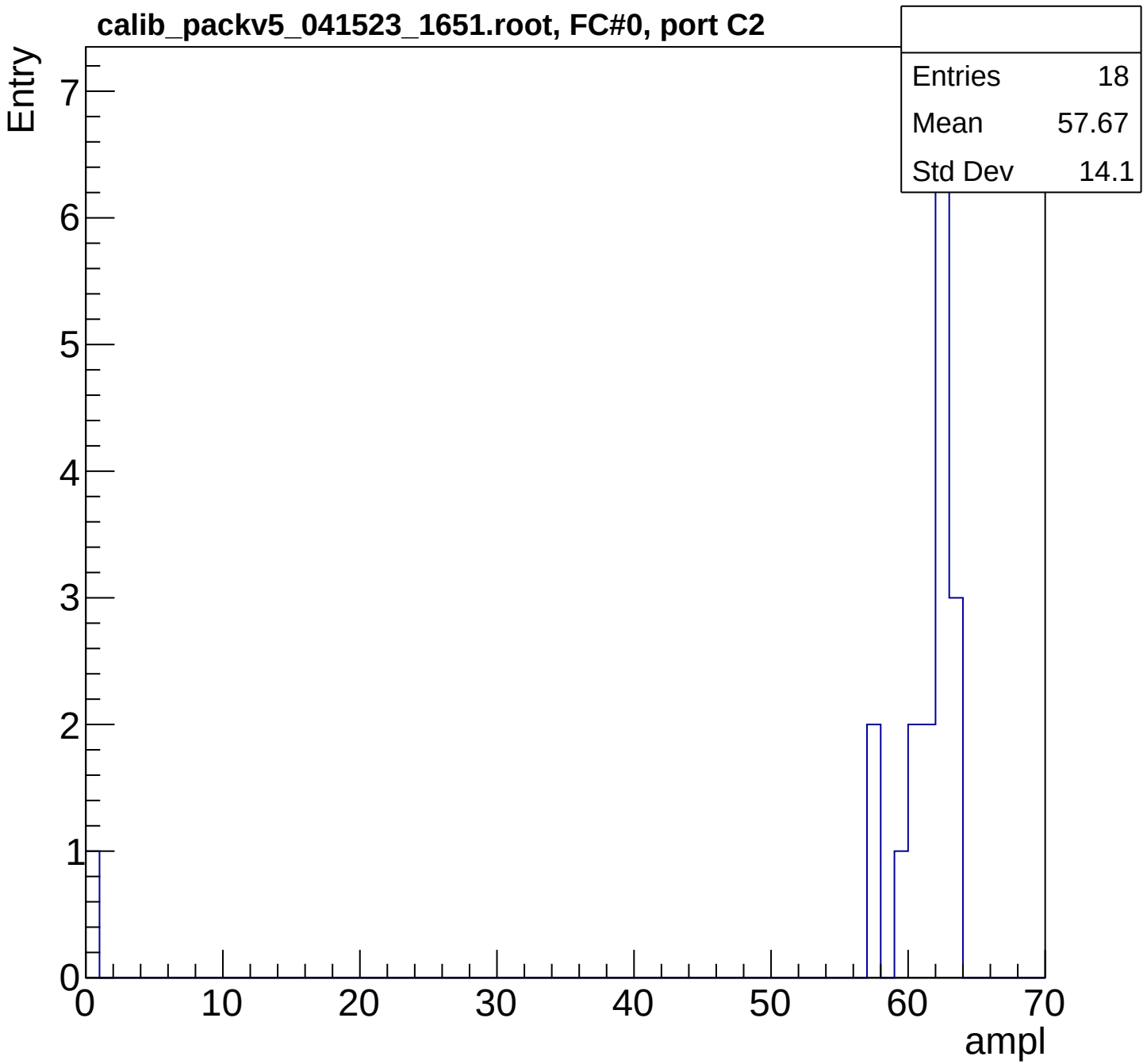
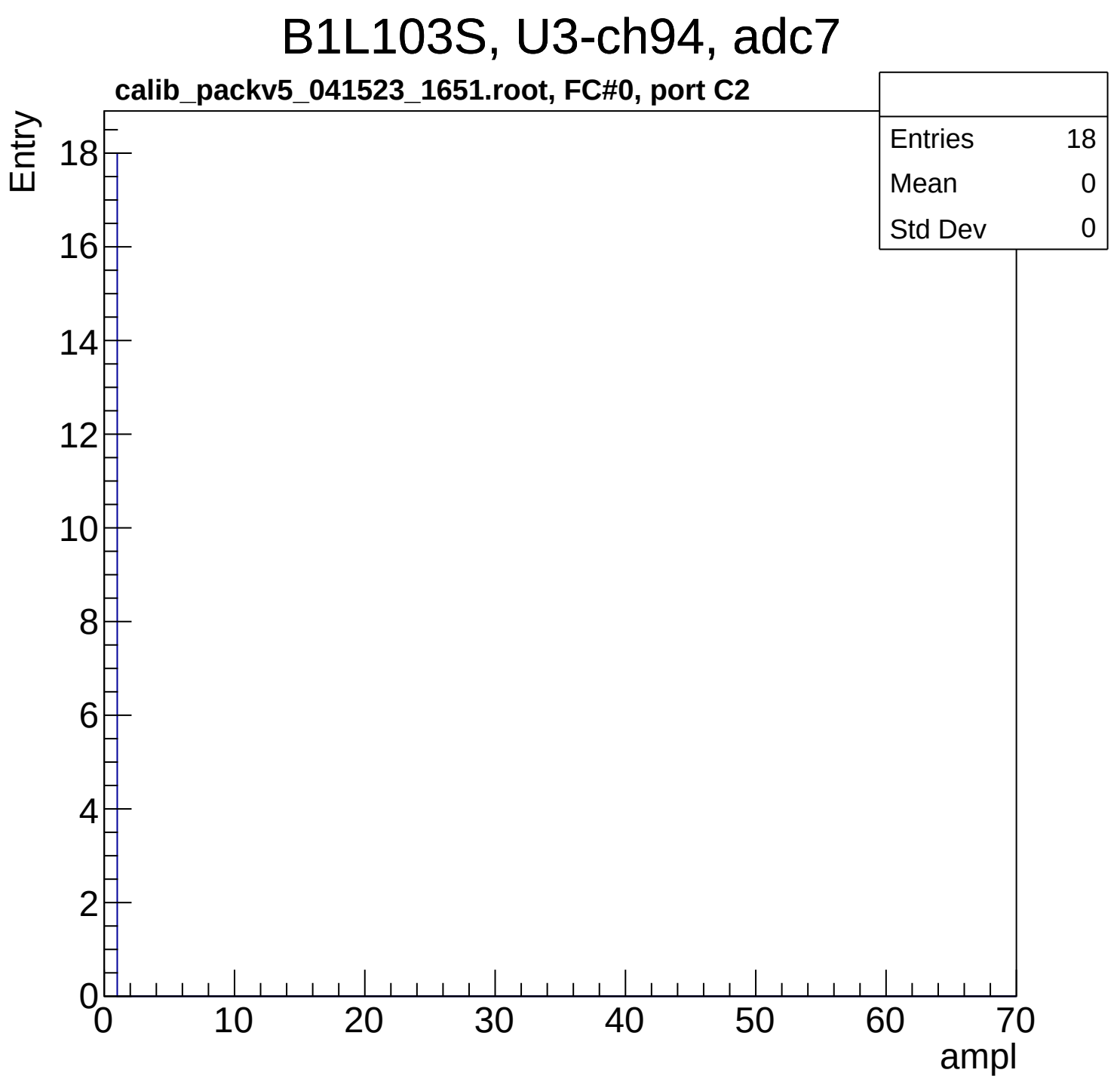
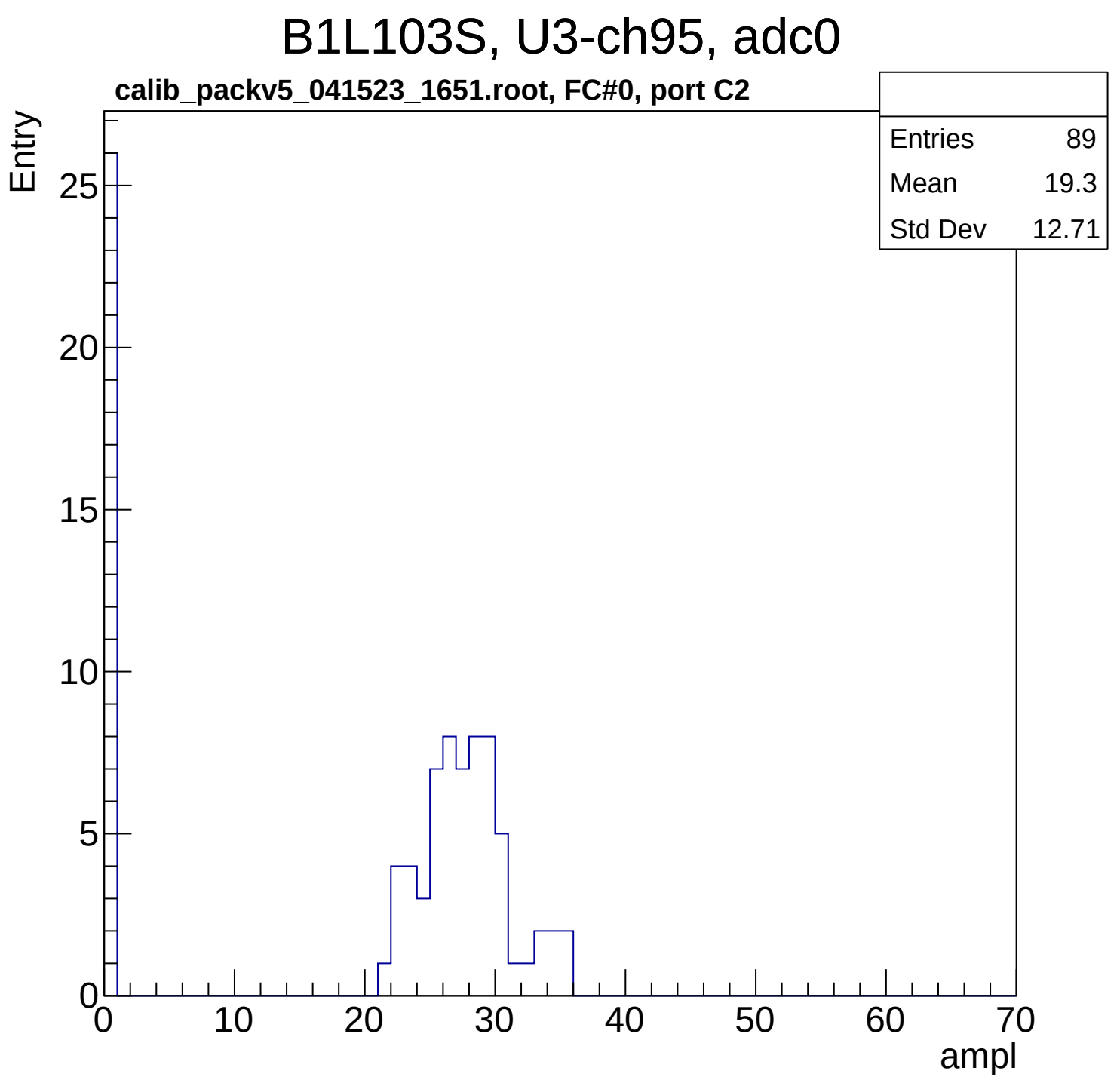

B1L103S, U3-ch94, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 57.67
Std Dev 14.1
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch94, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch95, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 19.3
Std Dev 12.71
Entry
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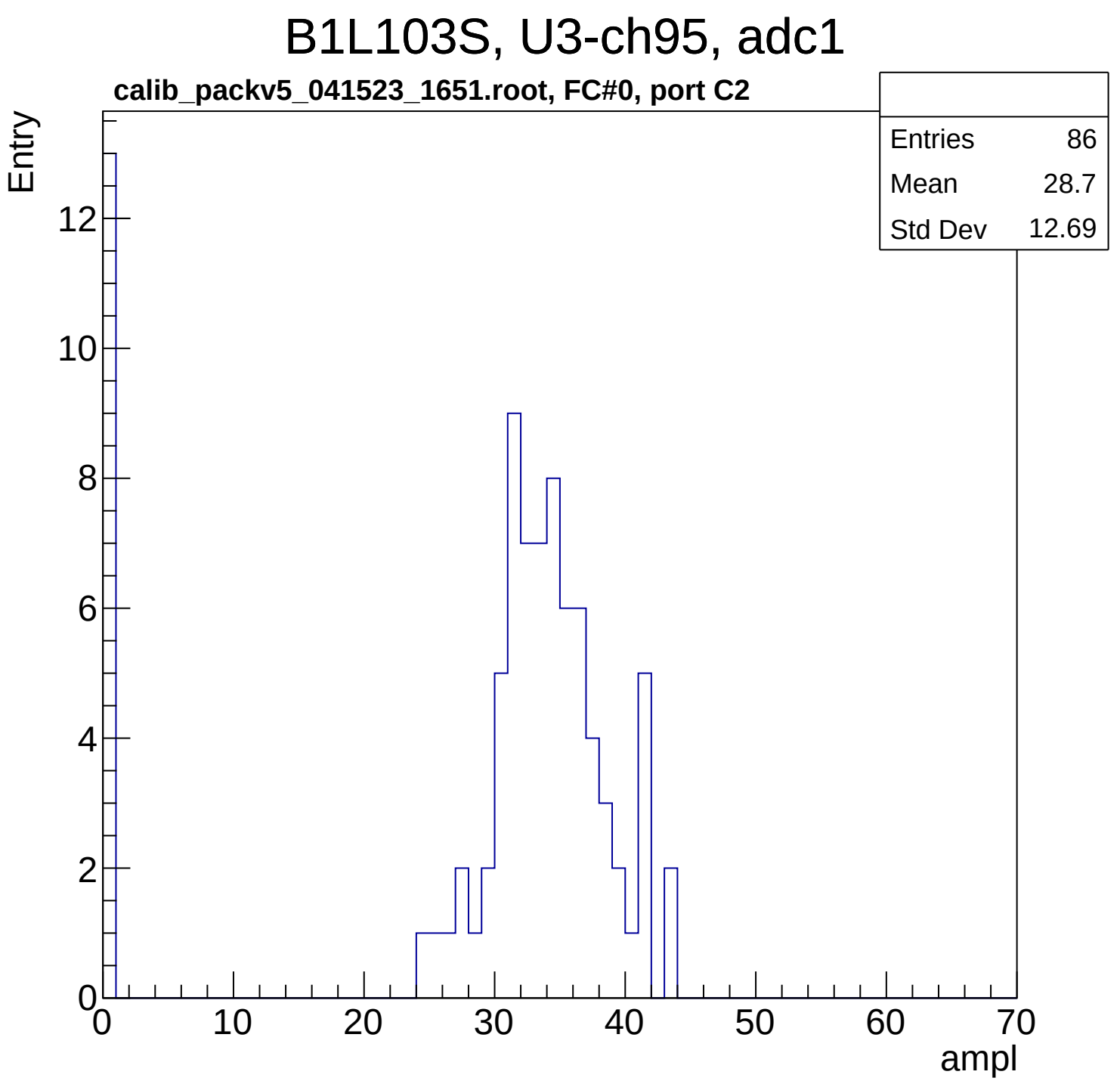
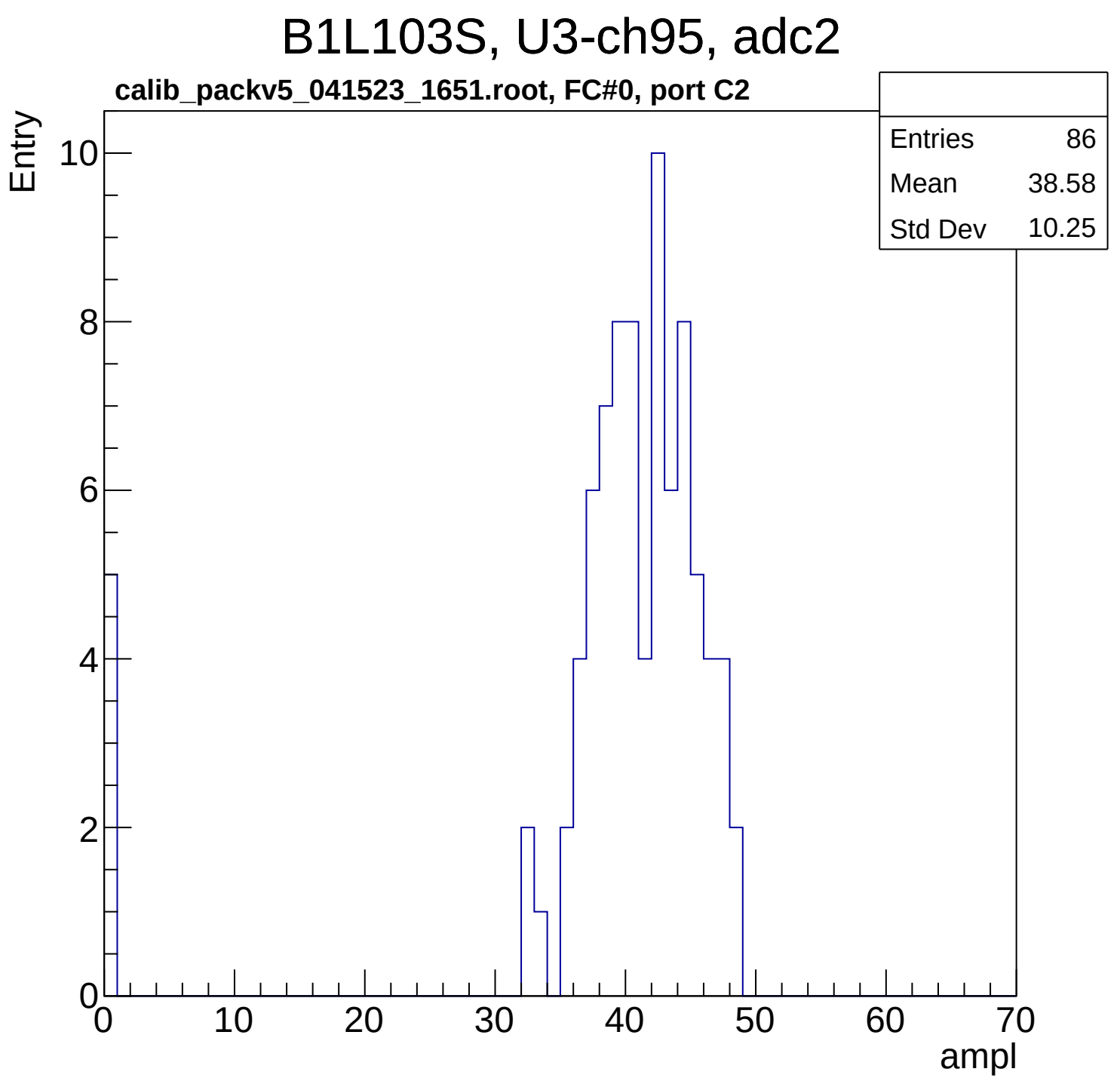
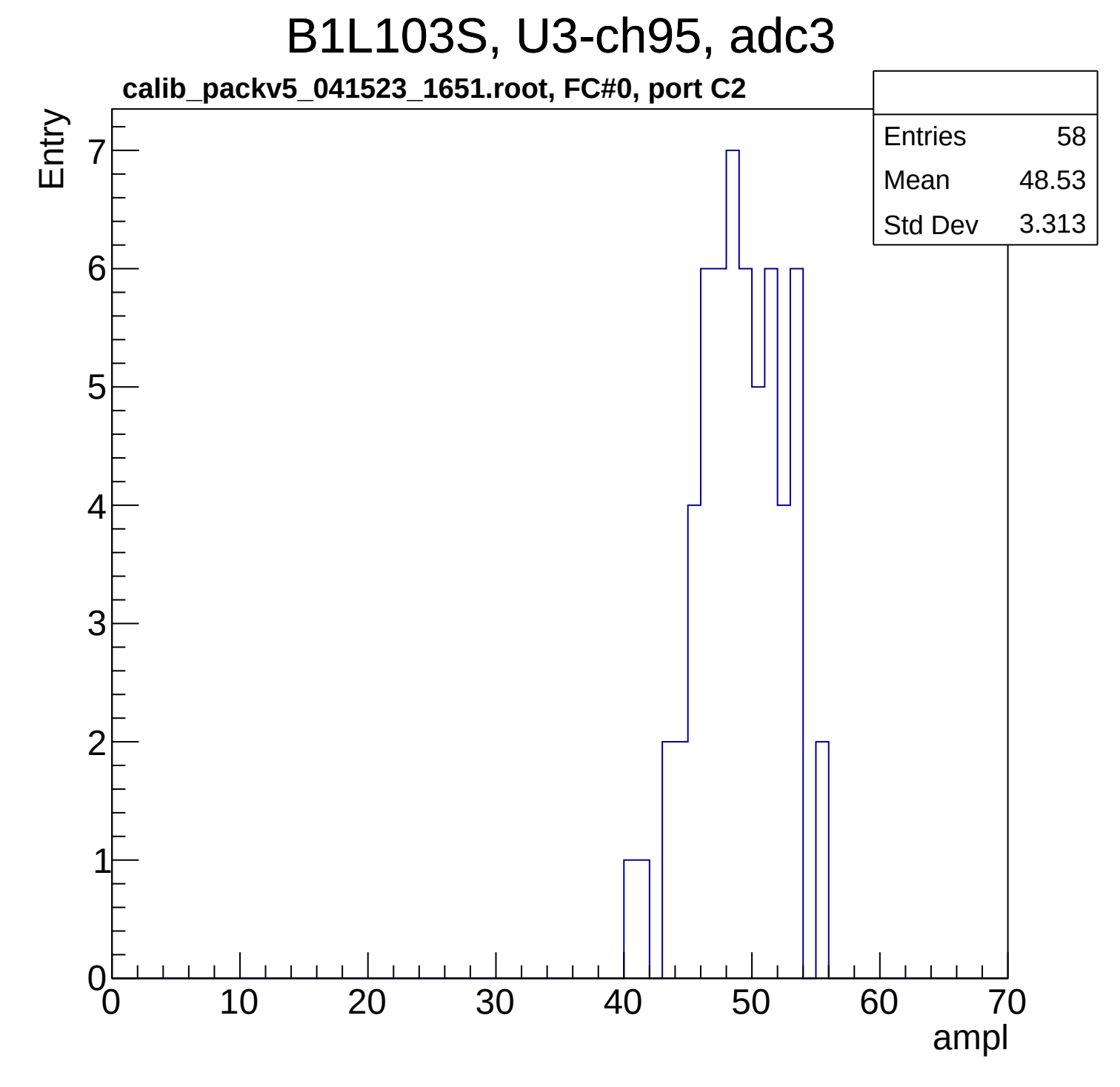
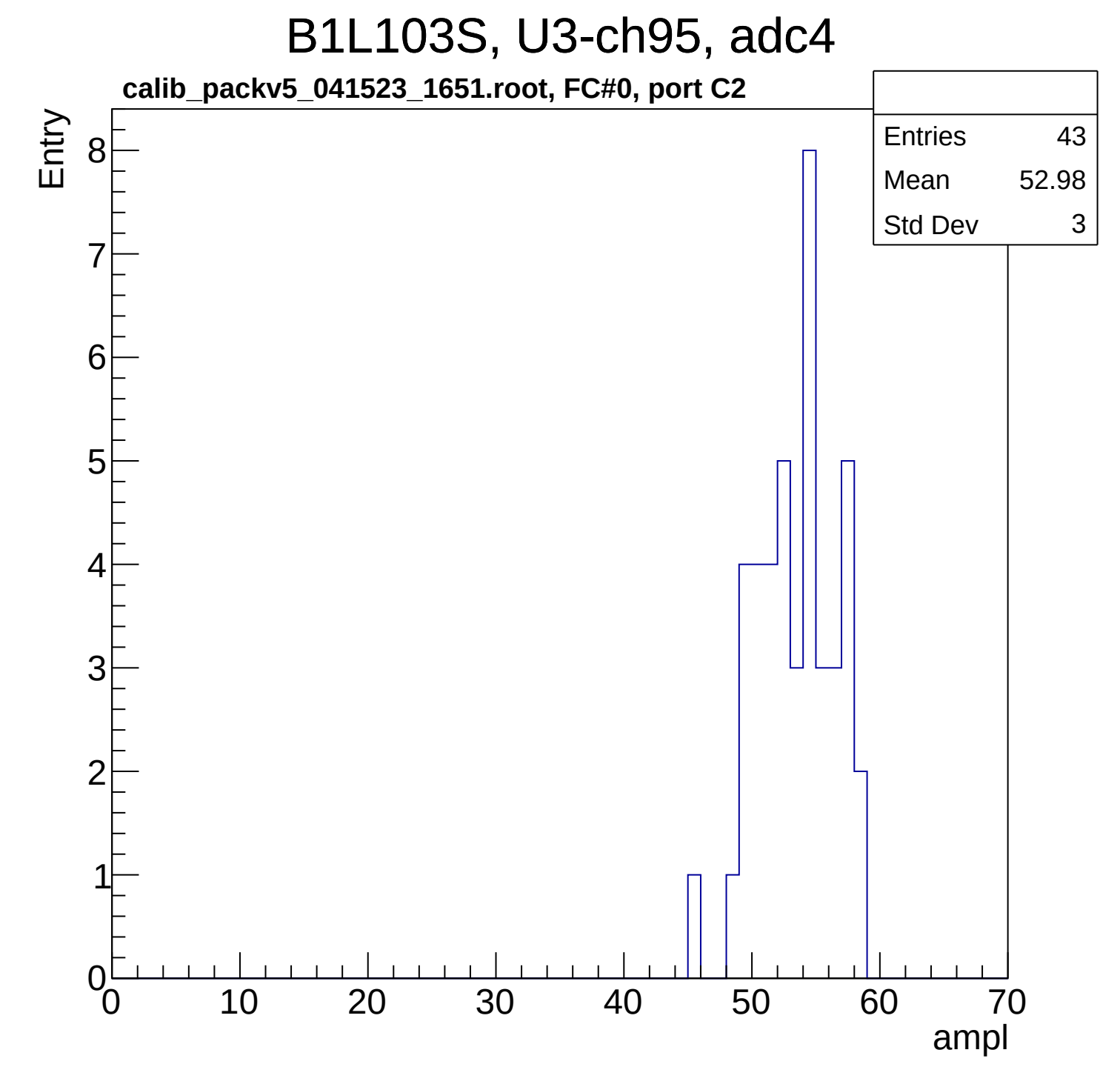
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch95, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 28.7
Std Dev 12.69
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch95, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 38.58
Std Dev 10.25
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U3-ch95, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 48.53
Std Dev 3.313
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch95, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 52.98
Std Dev 3
Entry
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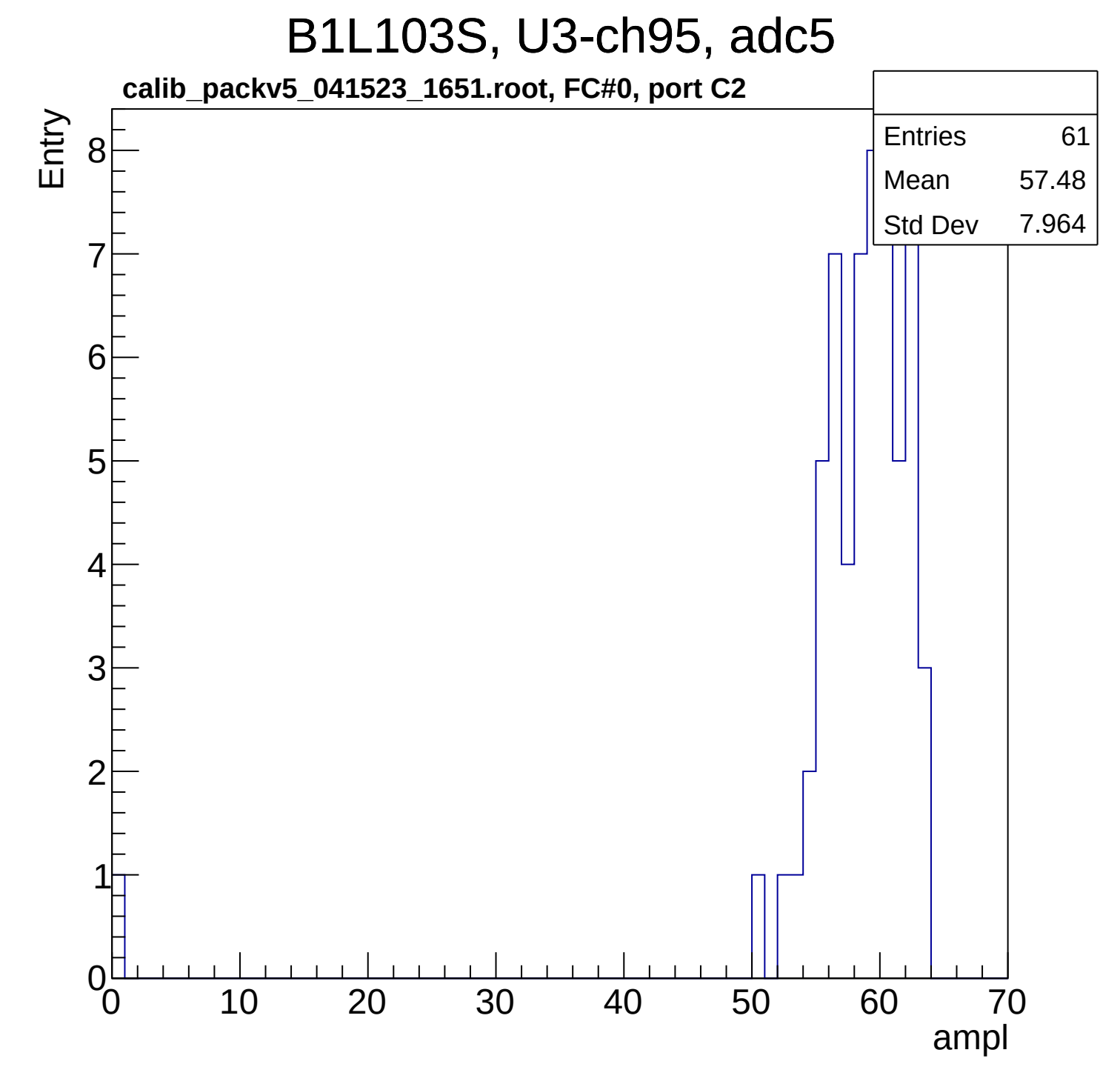
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch95, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 57.48
Std Dev 7.964
Entry
ampl
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2
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4
5
6
7
8
0
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20
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40
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60
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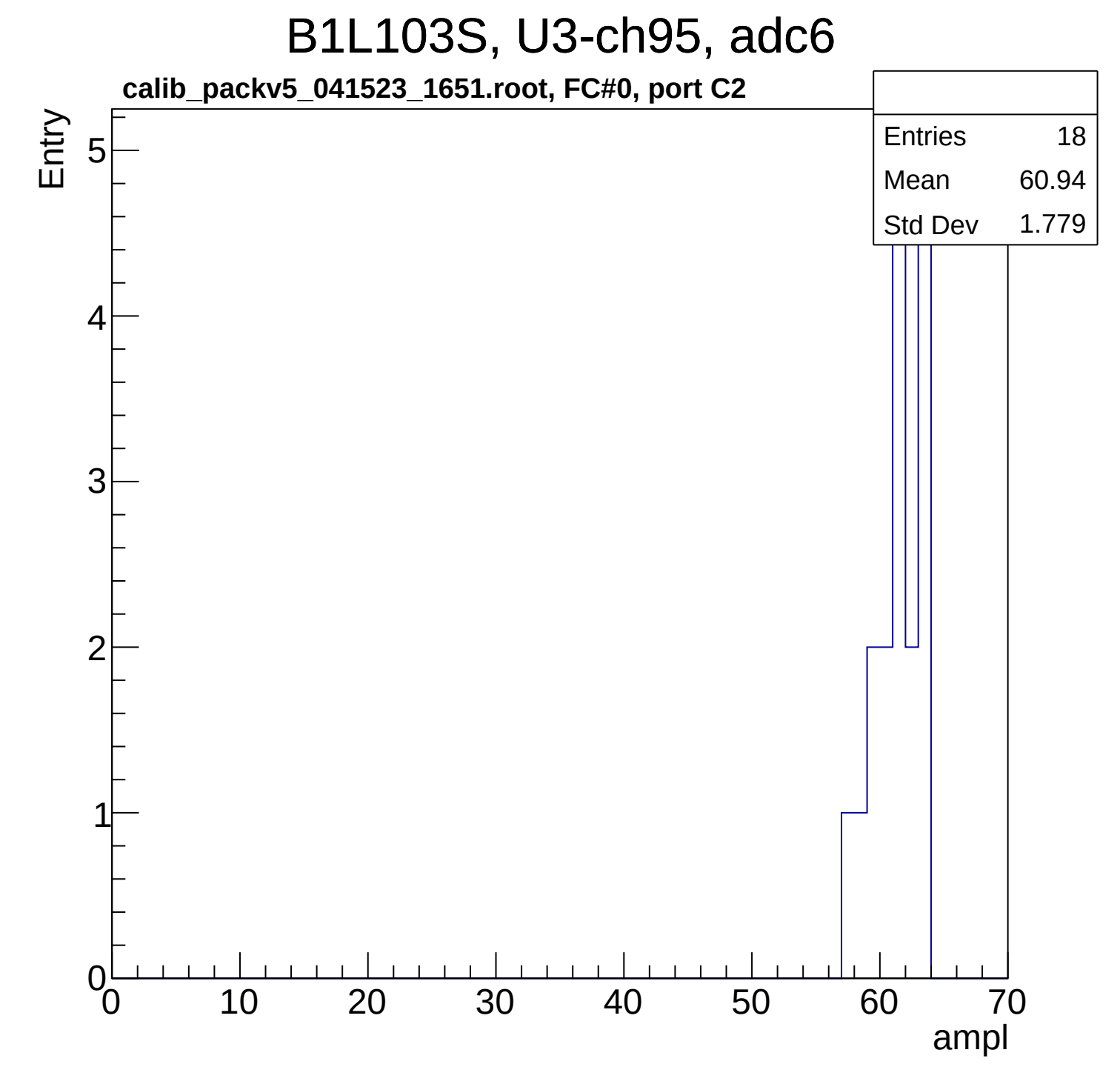
B1L103S, U3-ch95, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 60.94
Std Dev 1.779
Entry
ampl
0
1
2
3
4
5
0
10
20
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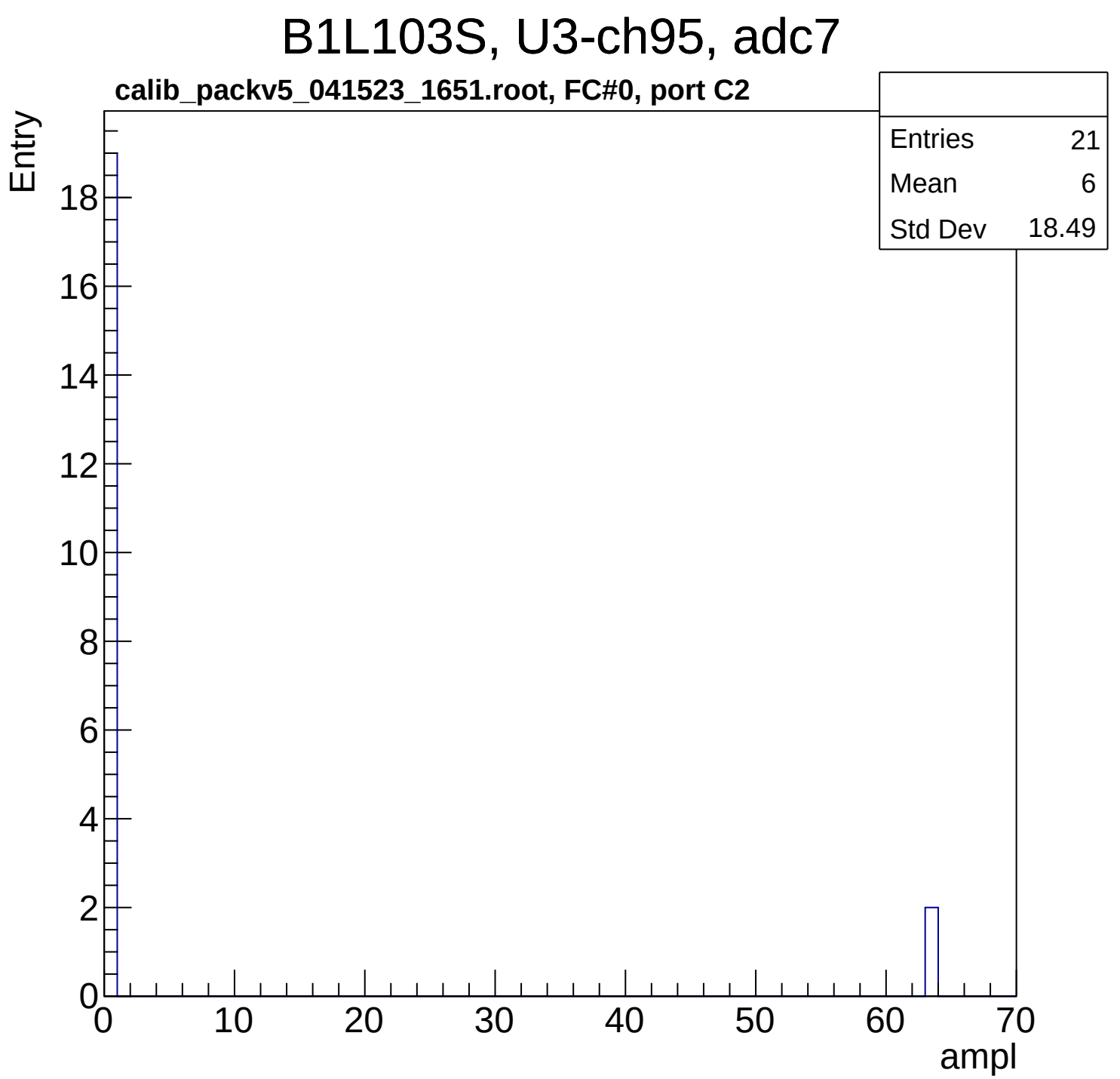
40
50
60
70


B1L103S, U3-ch95, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 6
Std Dev 18.49
Entry
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6
8
10
12
14
16
18
0
10
20
30
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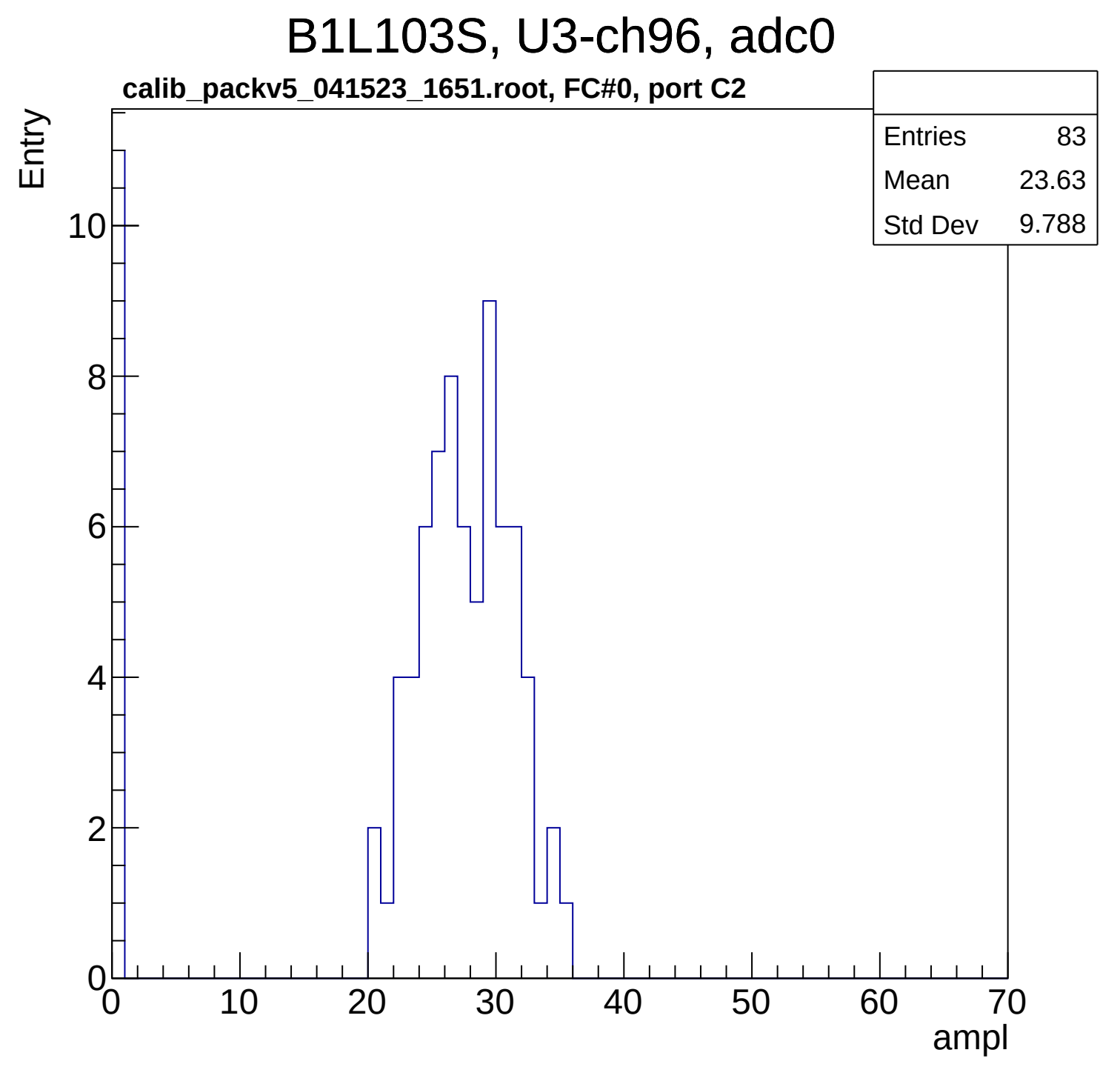
50
60
70
ampl


B1L103S, U3-ch96, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 23.63
Std Dev 9.788
Entry
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6
8
10
0
10
20
30
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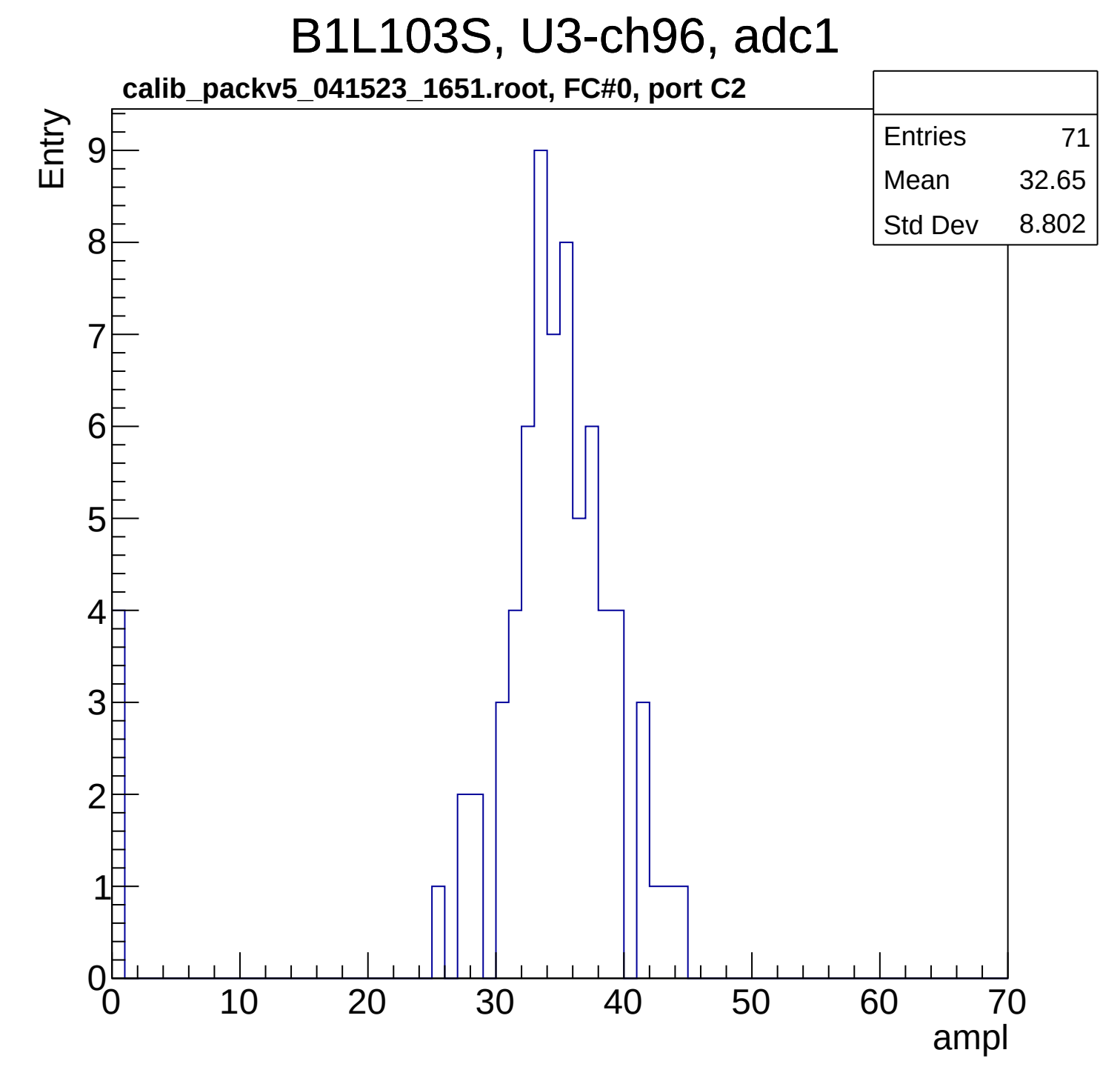
50
60
70
ampl


B1L103S, U3-ch96, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 32.65
Std Dev 8.802
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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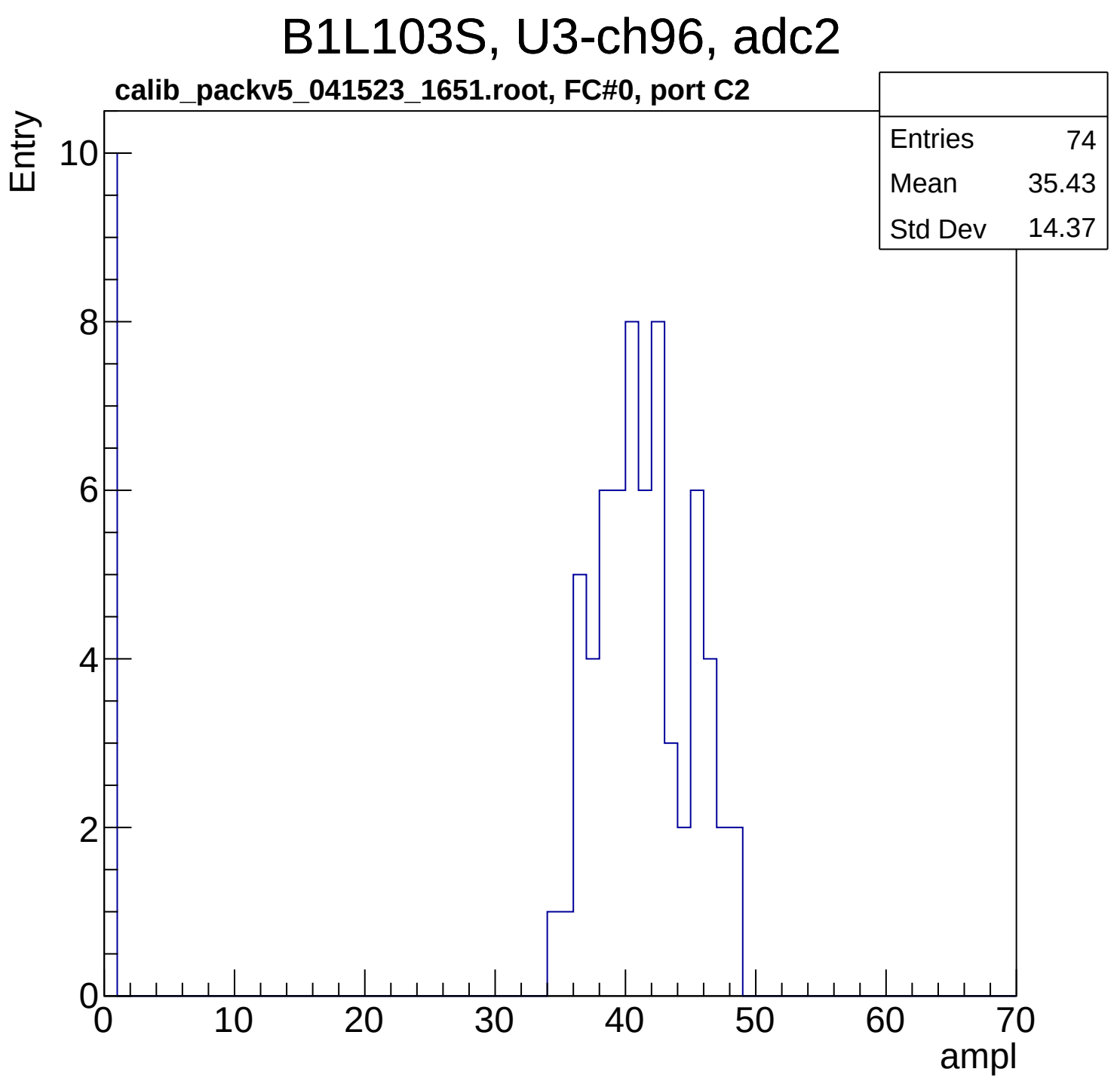
B1L103S, U3-ch96, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 35.43
Std Dev 14.37
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
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60
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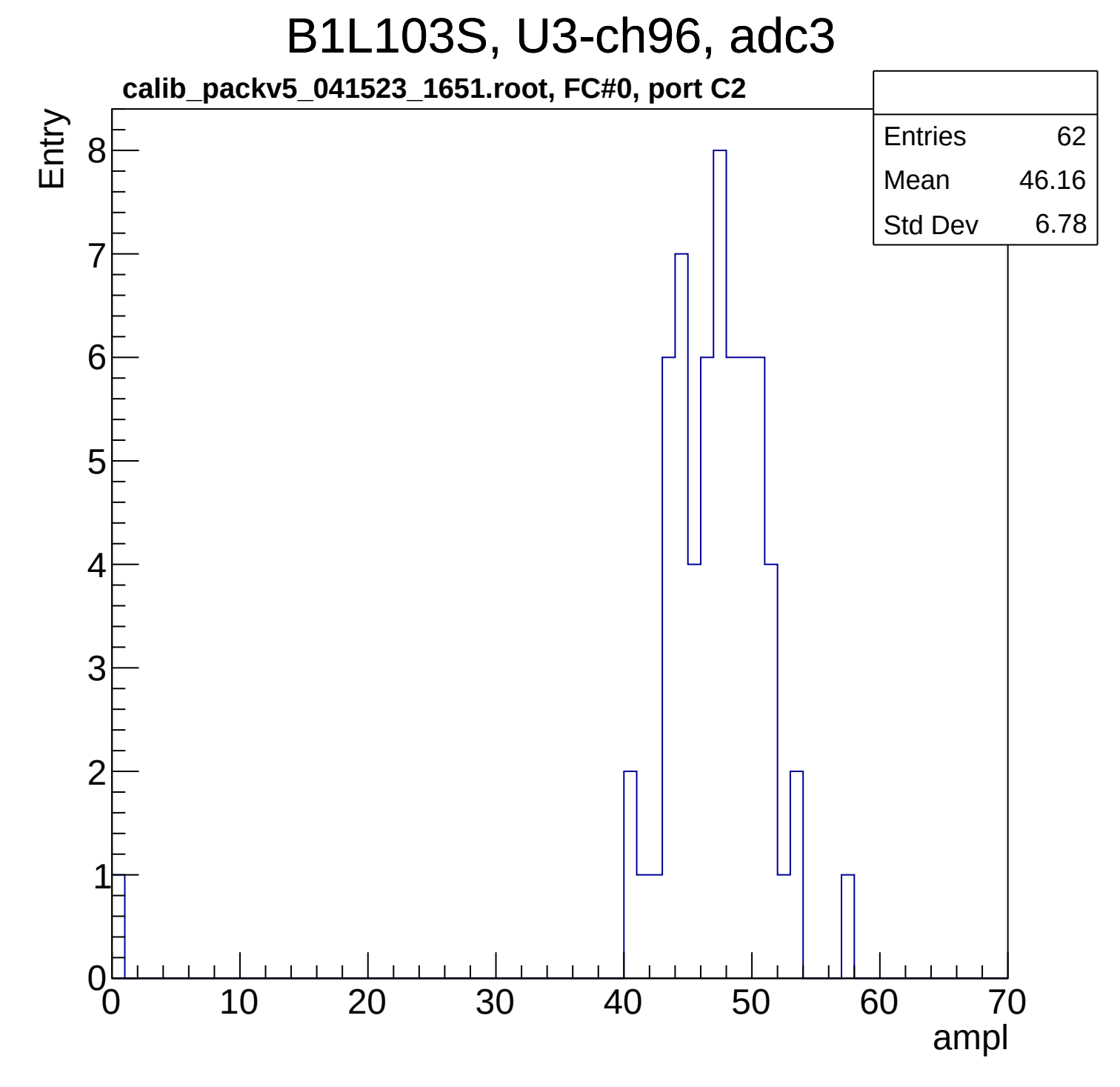
B1L103S, U3-ch96, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 46.16
Std Dev 6.78
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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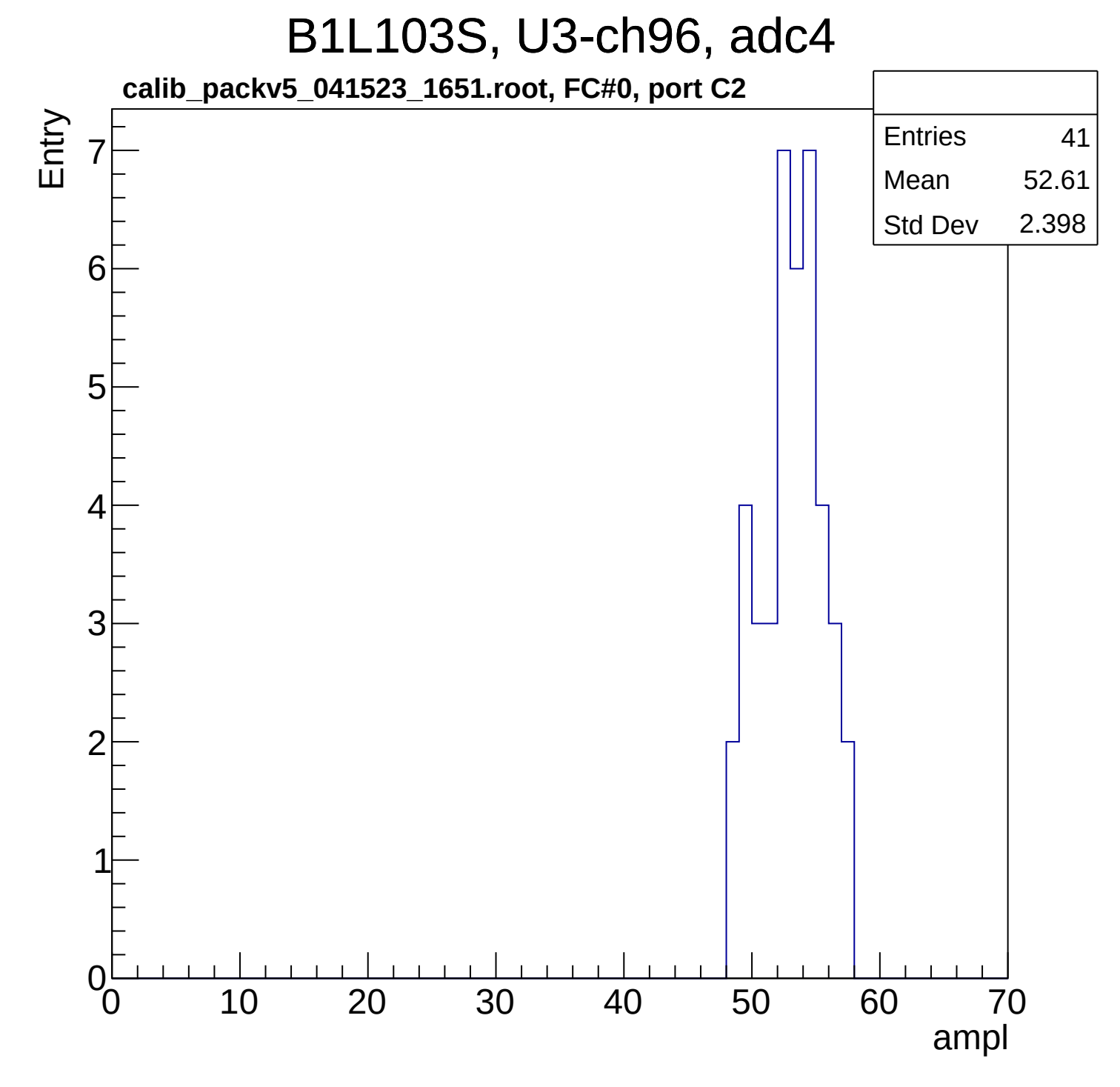
B1L103S, U3-ch96, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 52.61
Std Dev 2.398
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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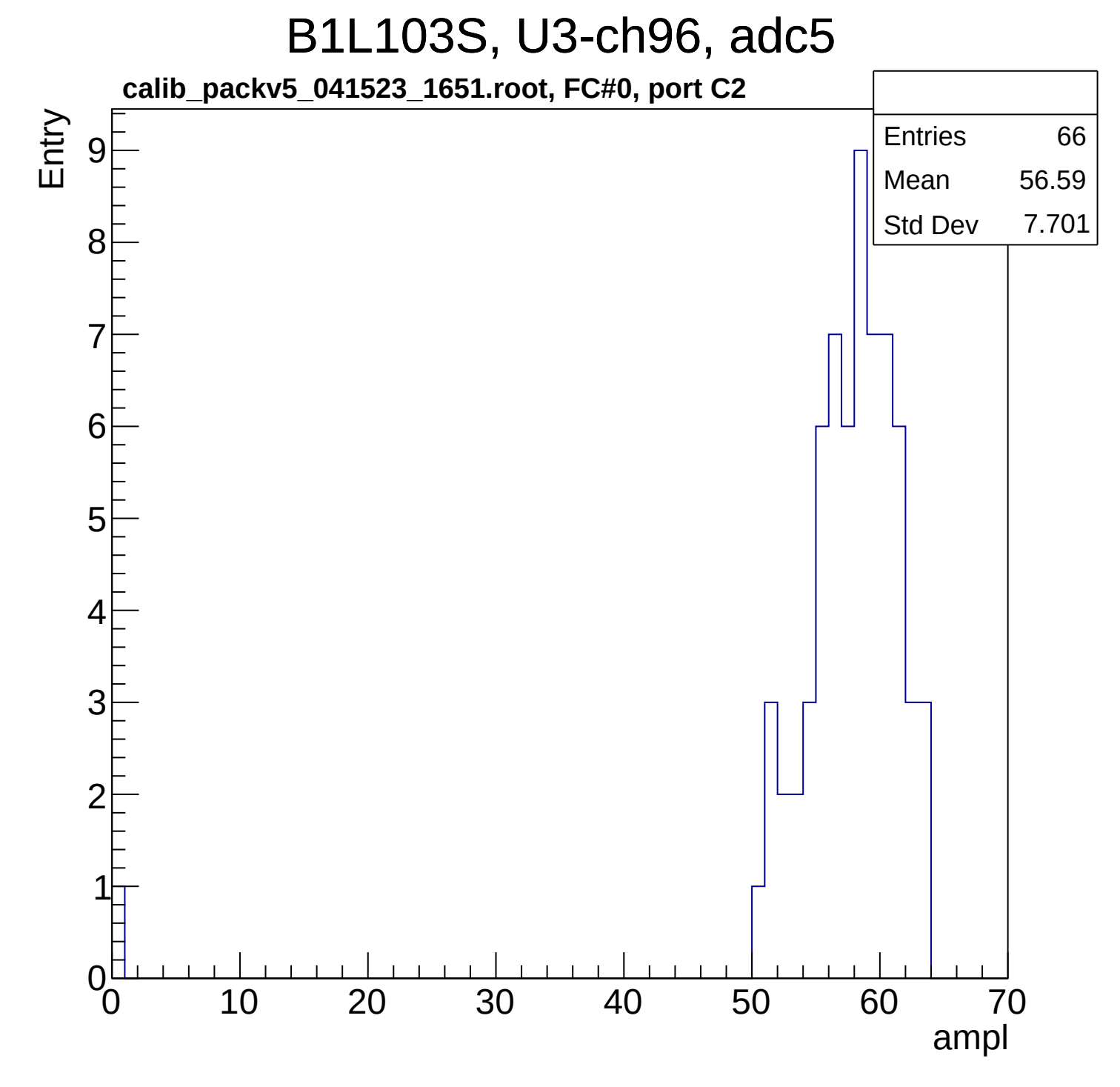
B1L103S, U3-ch96, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 56.59
Std Dev 7.701
Entry
ampl
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2
3
4
5
6
7
8
9
0
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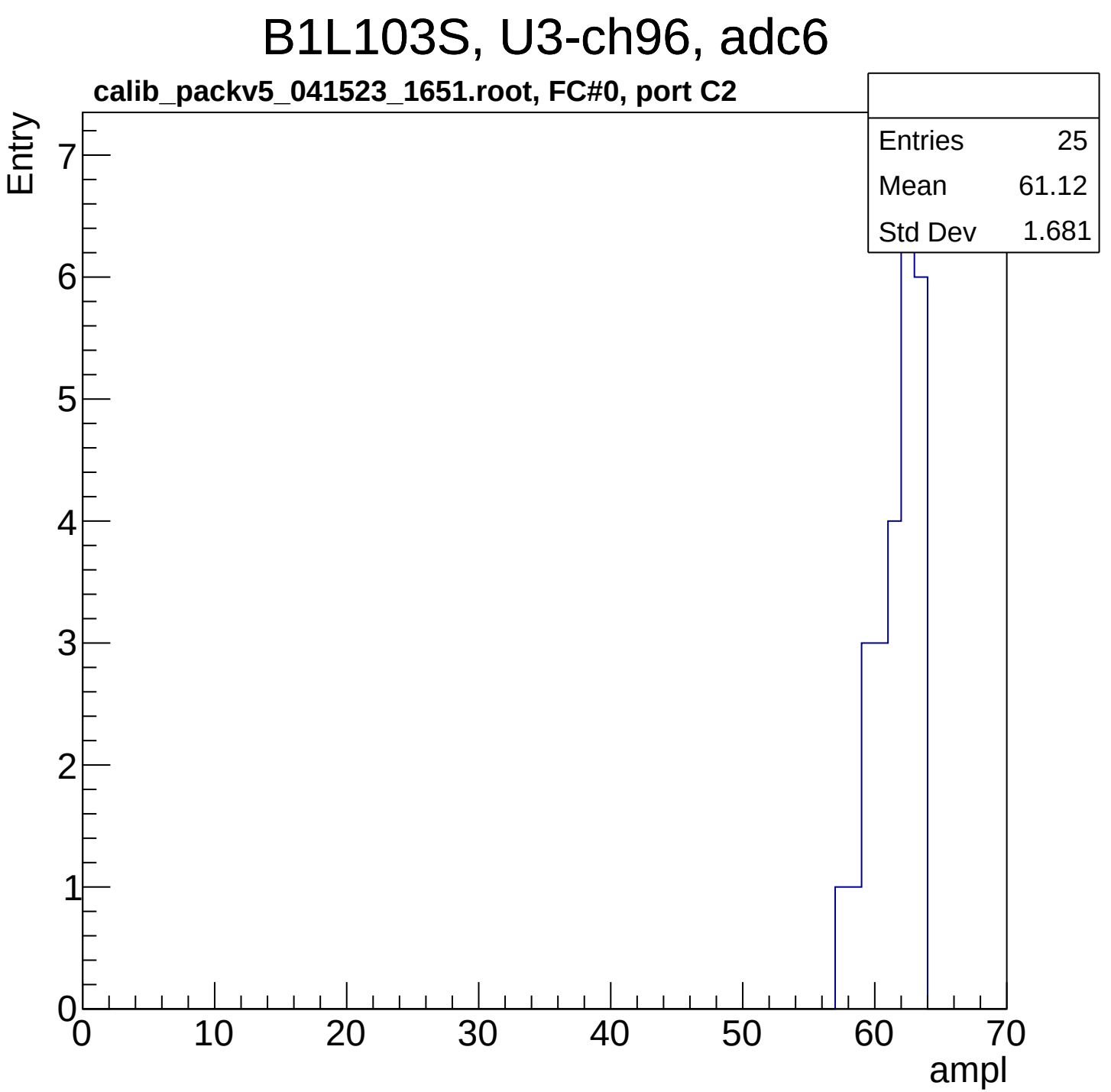
B1L103S, U3-ch96, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 61.12
Std Dev 1.681
Entry
ampl
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1
2
3
4
5
6
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0
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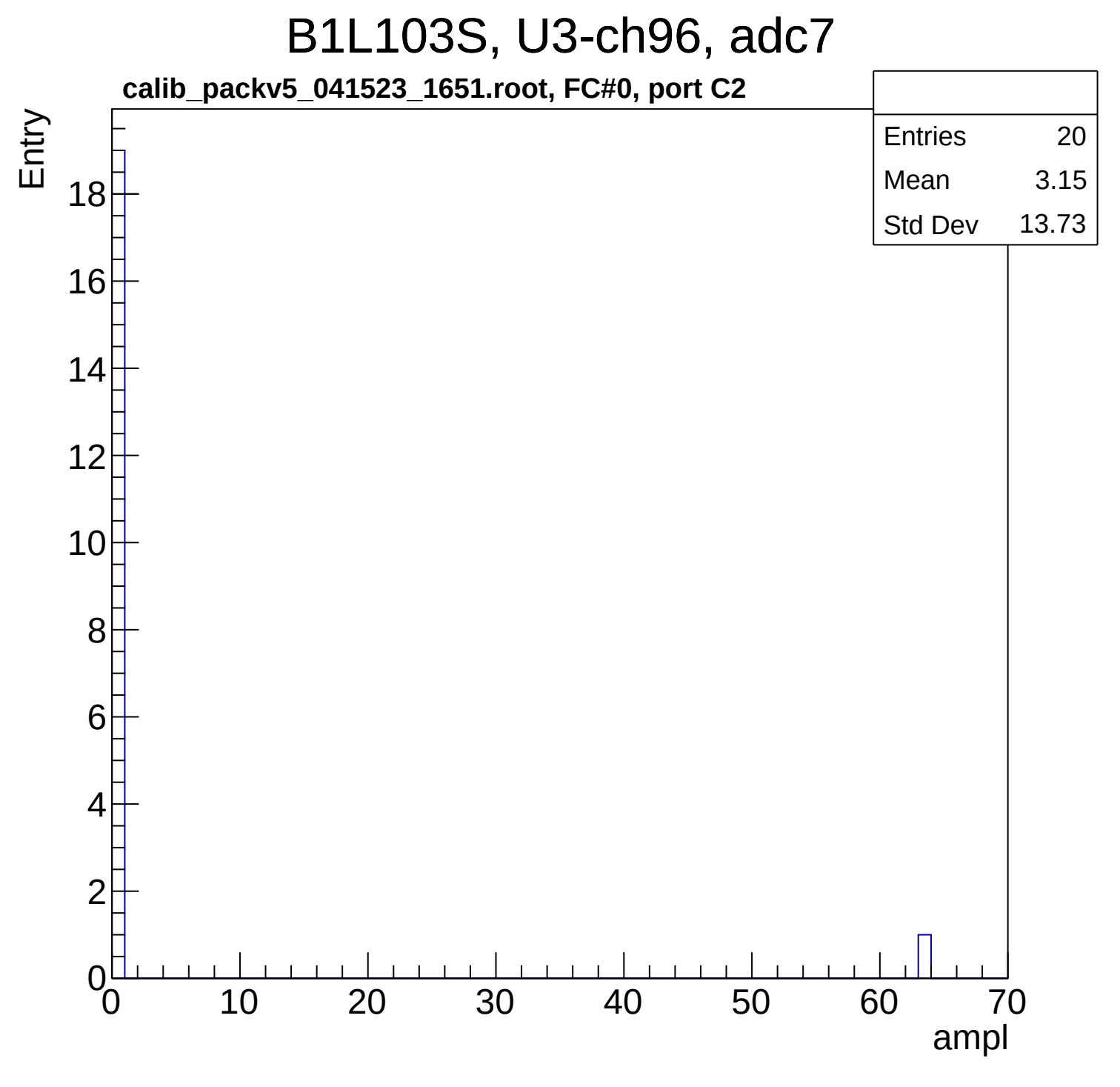
20
30
40
50
60
70


B1L103S, U3-ch96, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
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8
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14
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10
20
30
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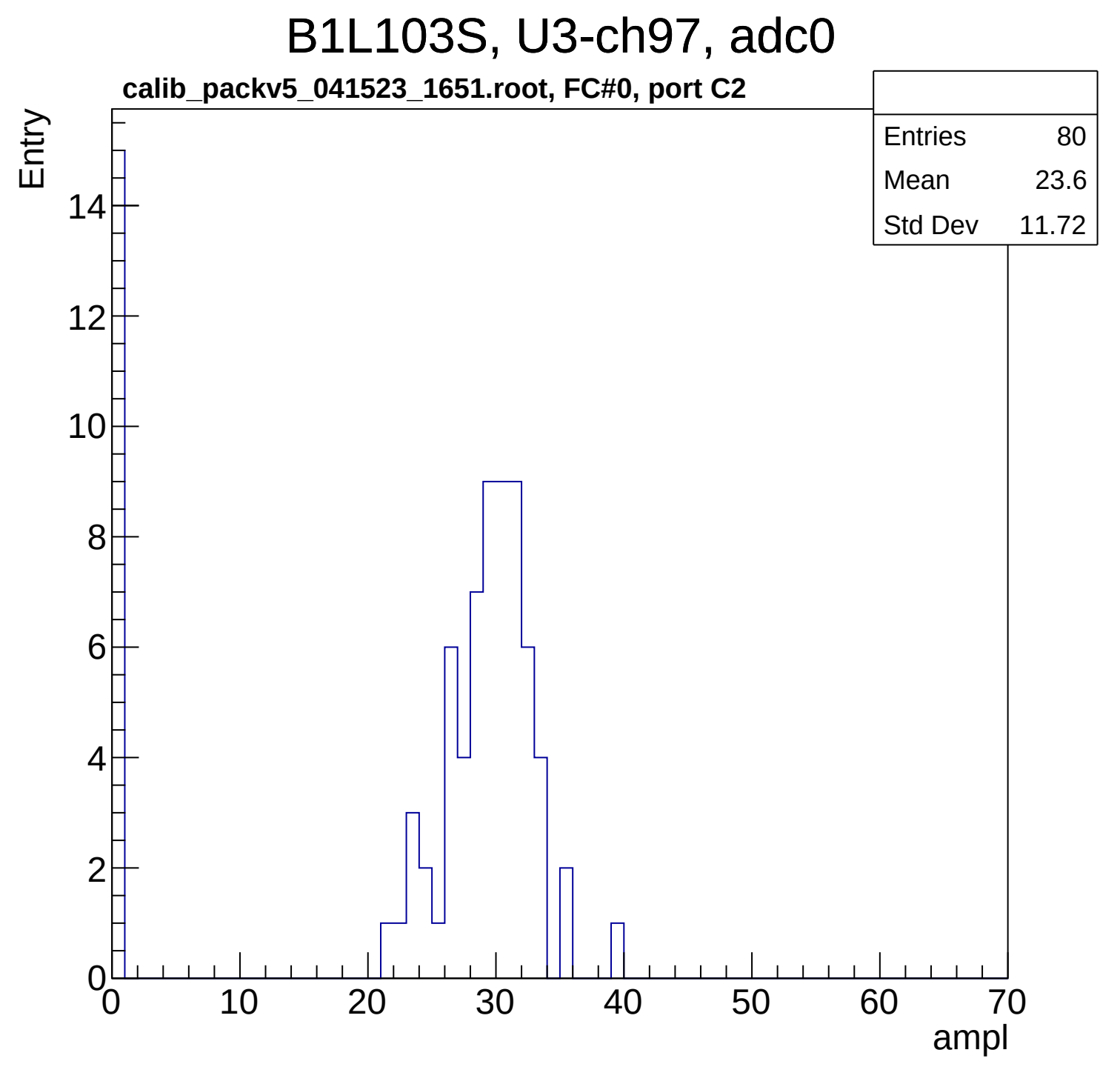
50
60
70
ampl


B1L103S, U3-ch97, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 23.6
Std Dev 11.72
Entry
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2
4
6
8
10
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14
0
10
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50
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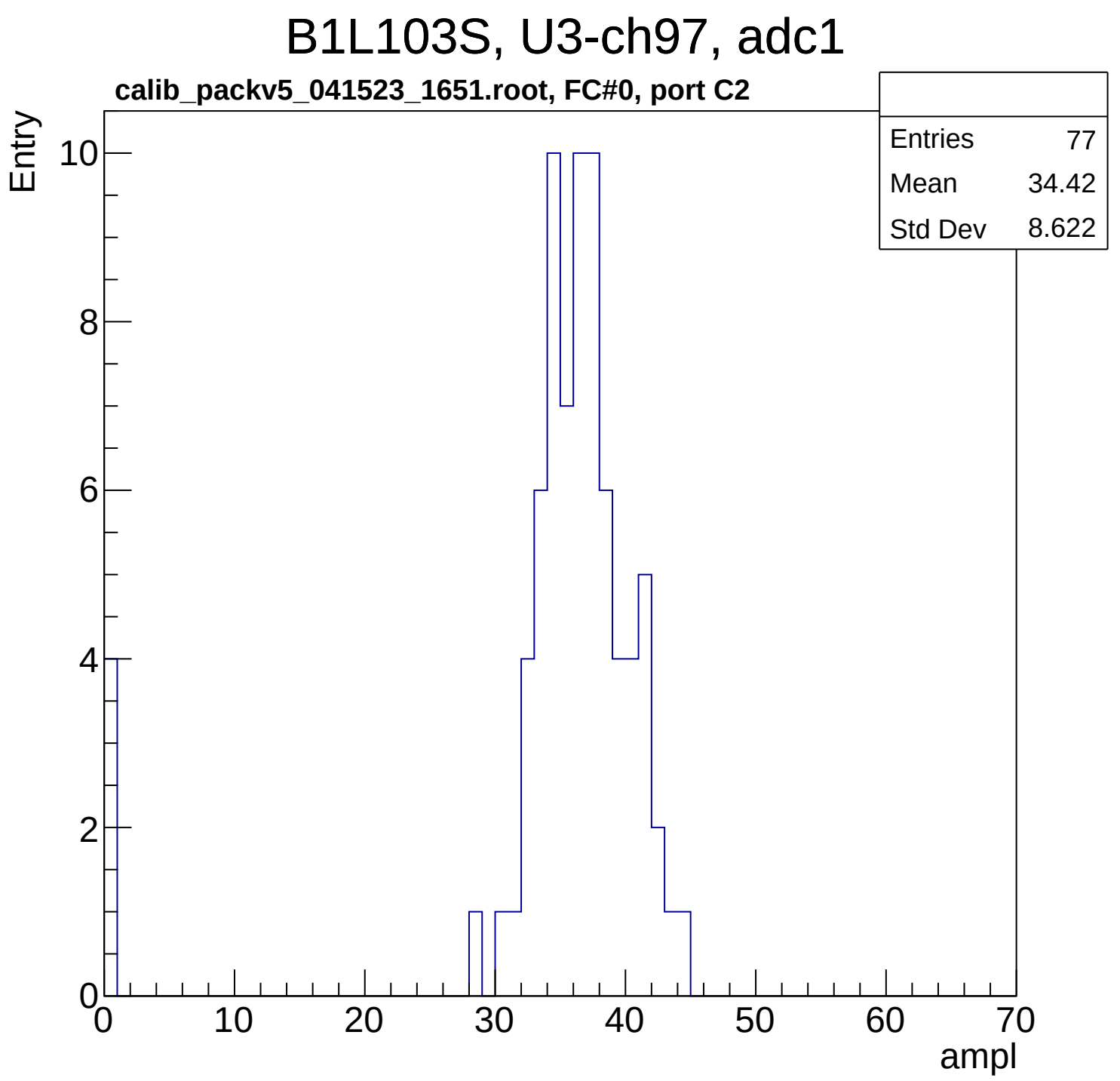
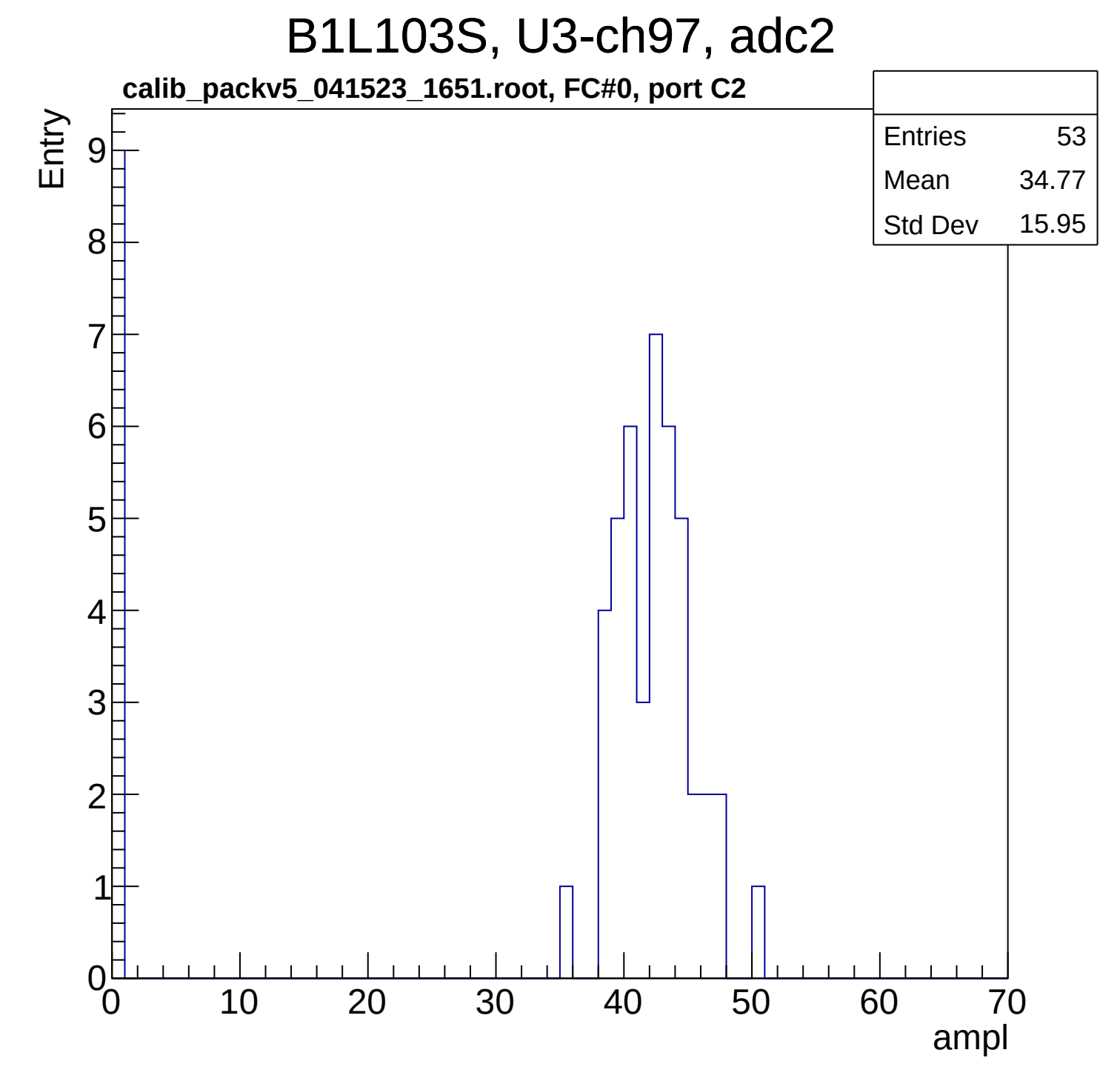
70
ampl


B1L103S, U3-ch97, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 34.42
Std Dev 8.622
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch97, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 34.77
Std Dev 15.95
Entry
ampl
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5
6
7
8
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0
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40
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60
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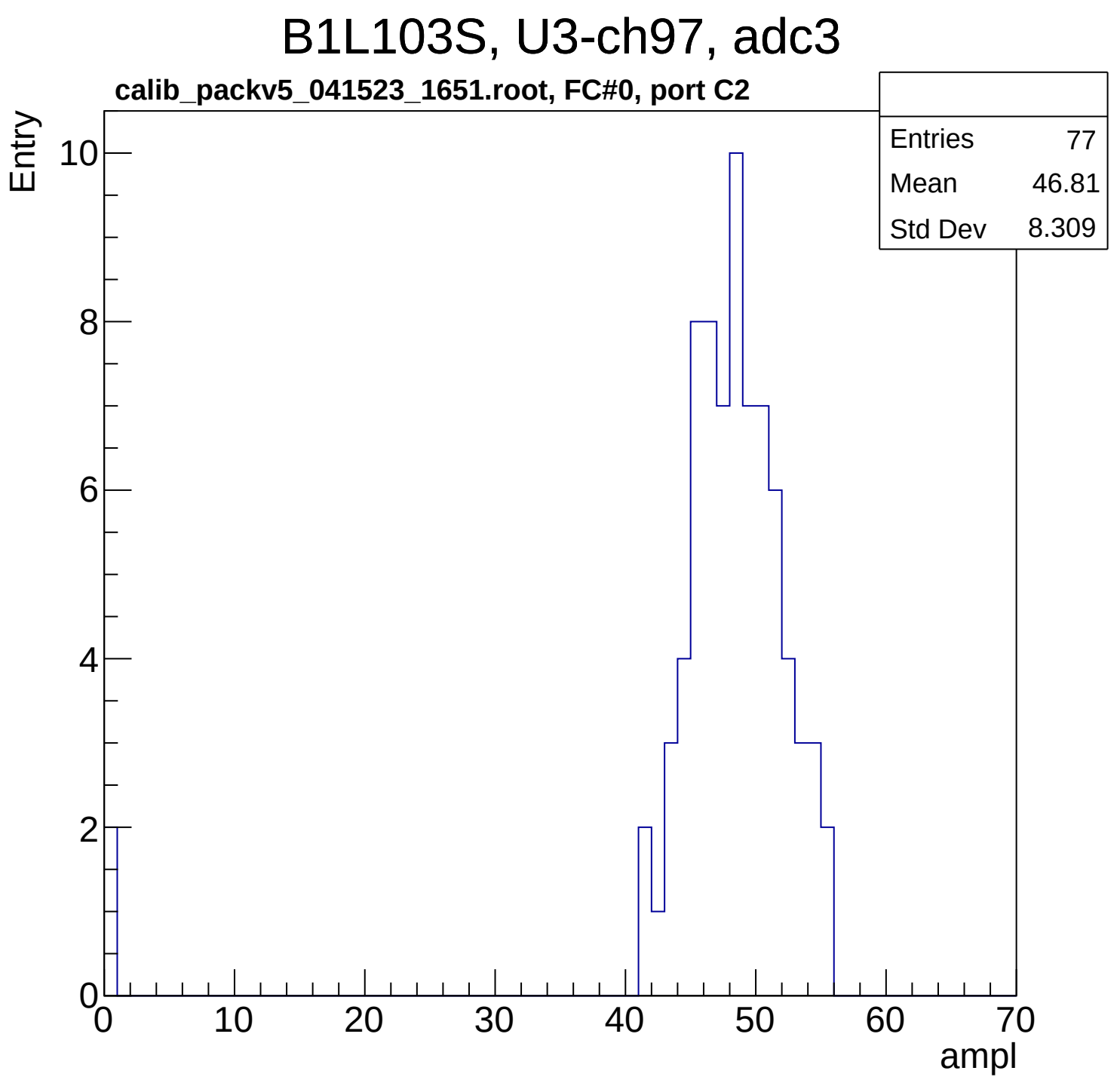
B1L103S, U3-ch97, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 46.81
Std Dev 8.309
Entry
ampl
0
2
4
6
8
10
0
10
20
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40
50
60
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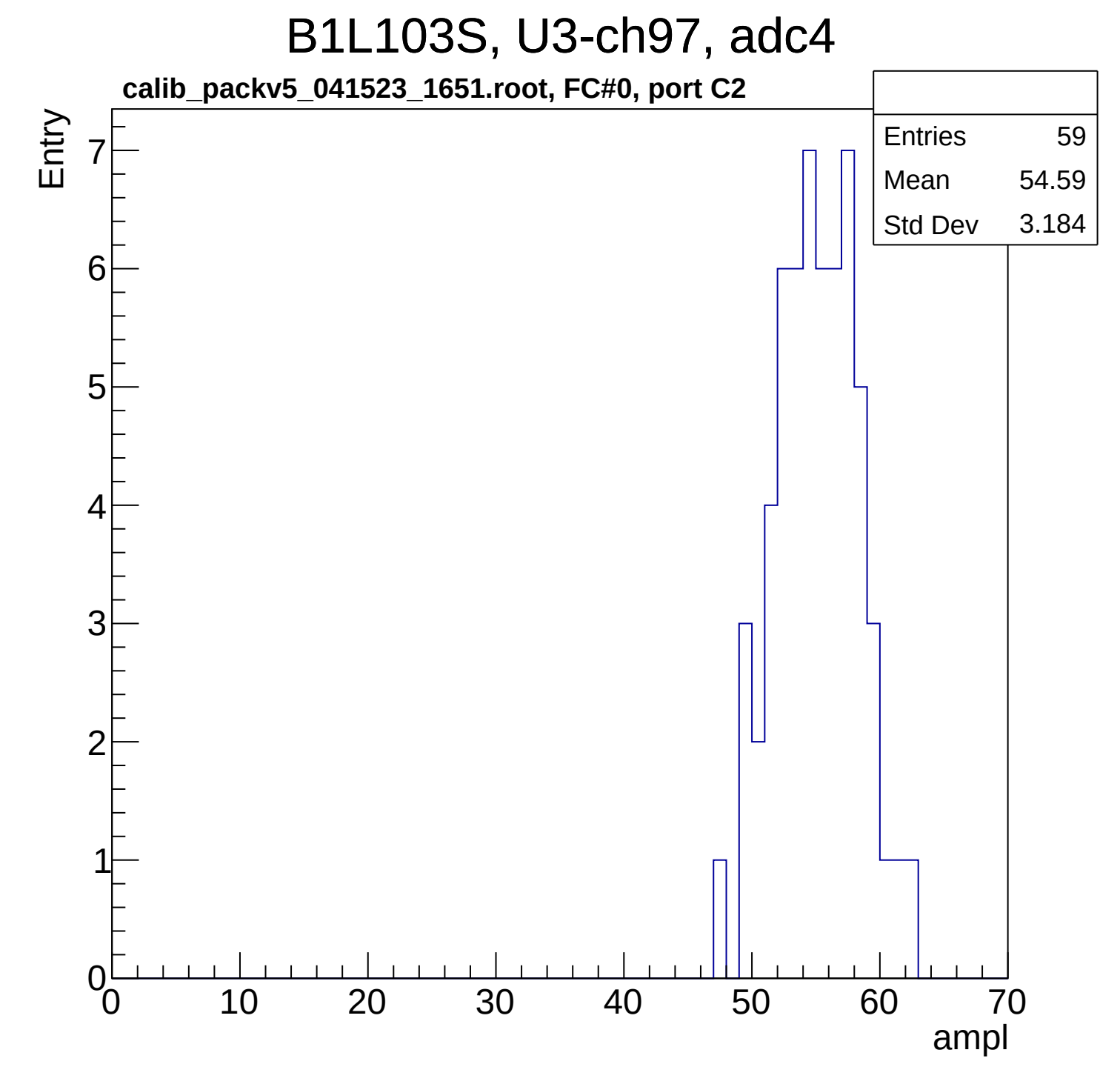
B1L103S, U3-ch97, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 54.59
Std Dev 3.184
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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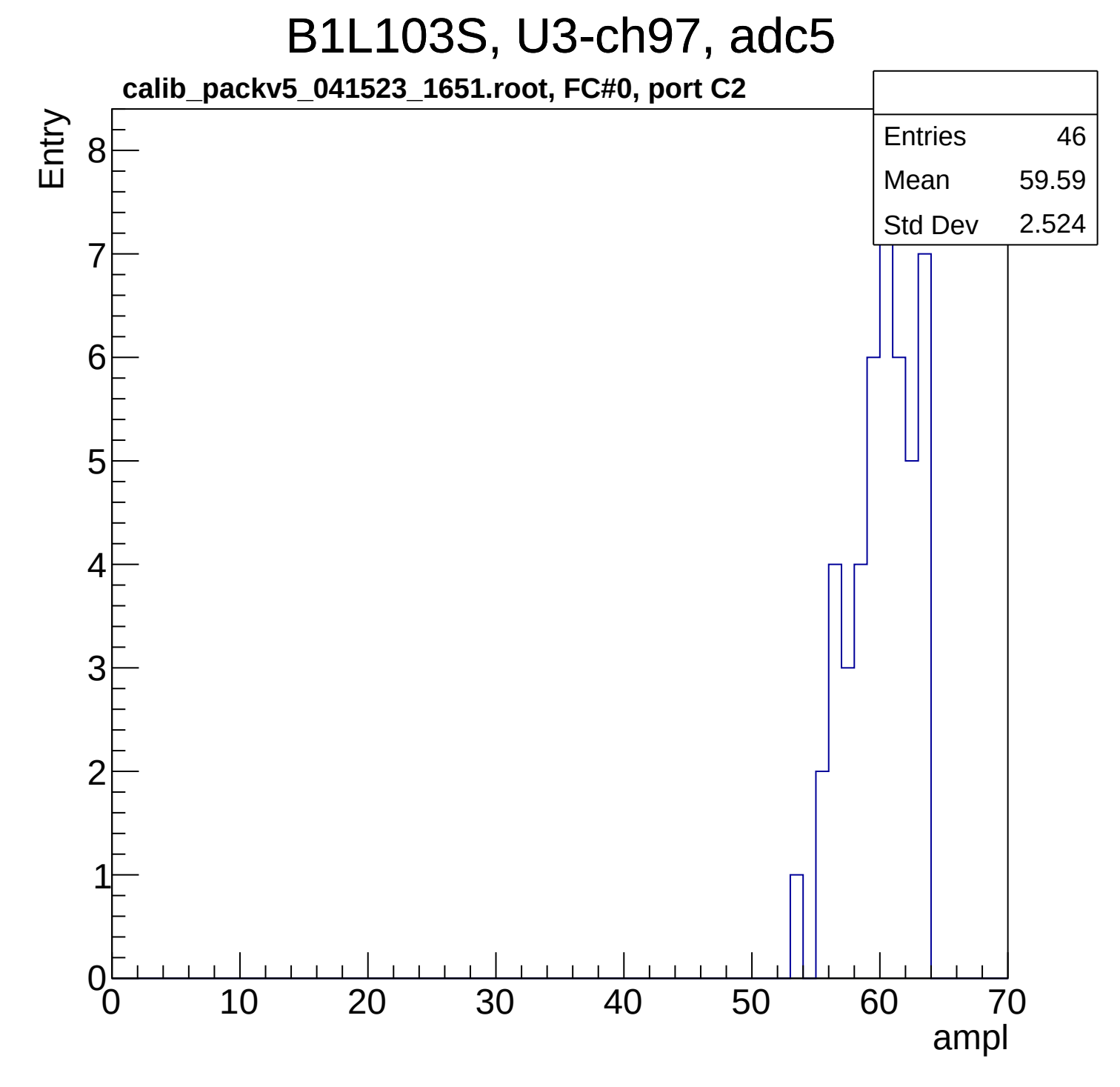
B1L103S, U3-ch97, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 59.59
Std Dev 2.524
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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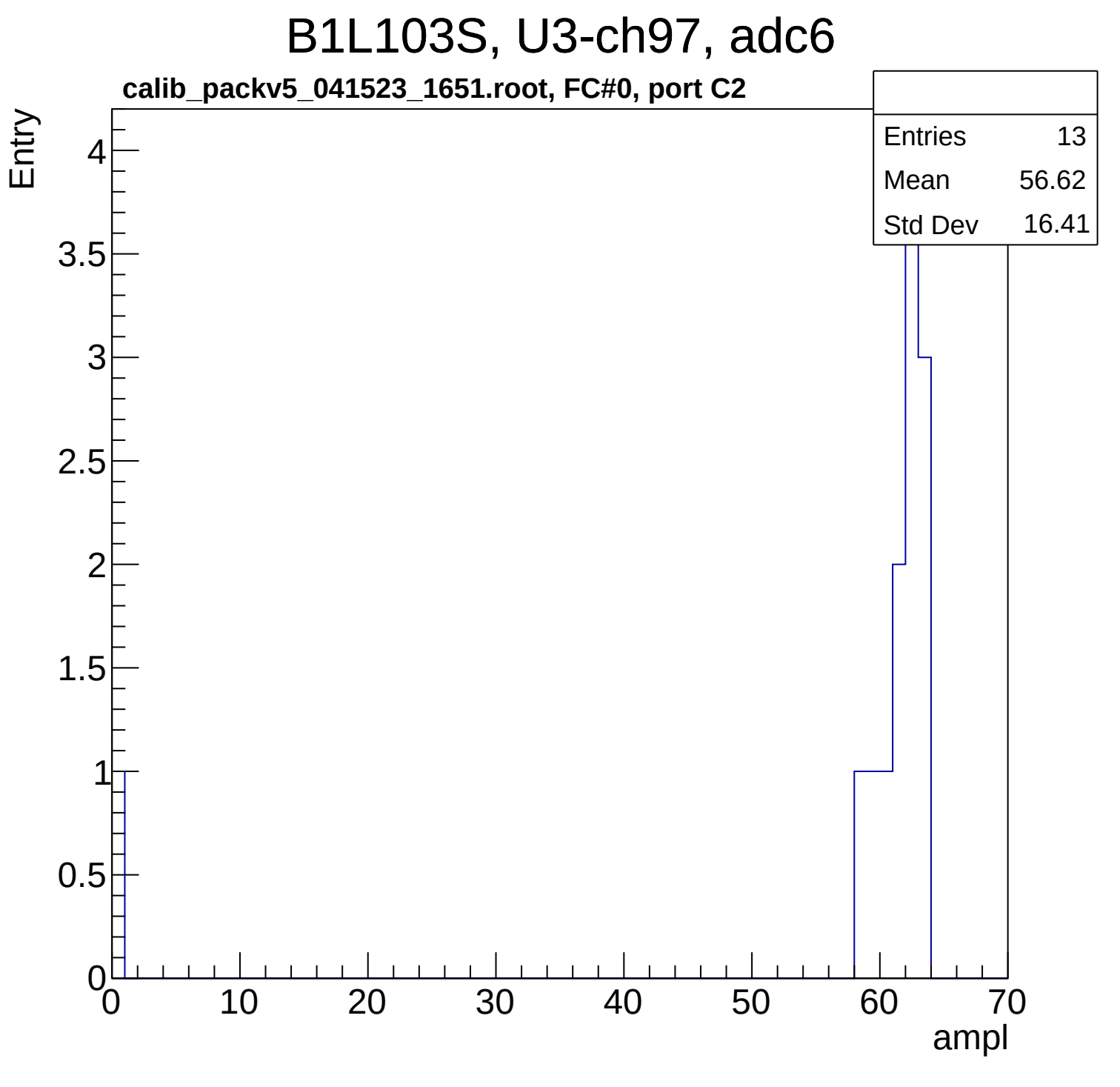
B1L103S, U3-ch97, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 56.62
Std Dev 16.41
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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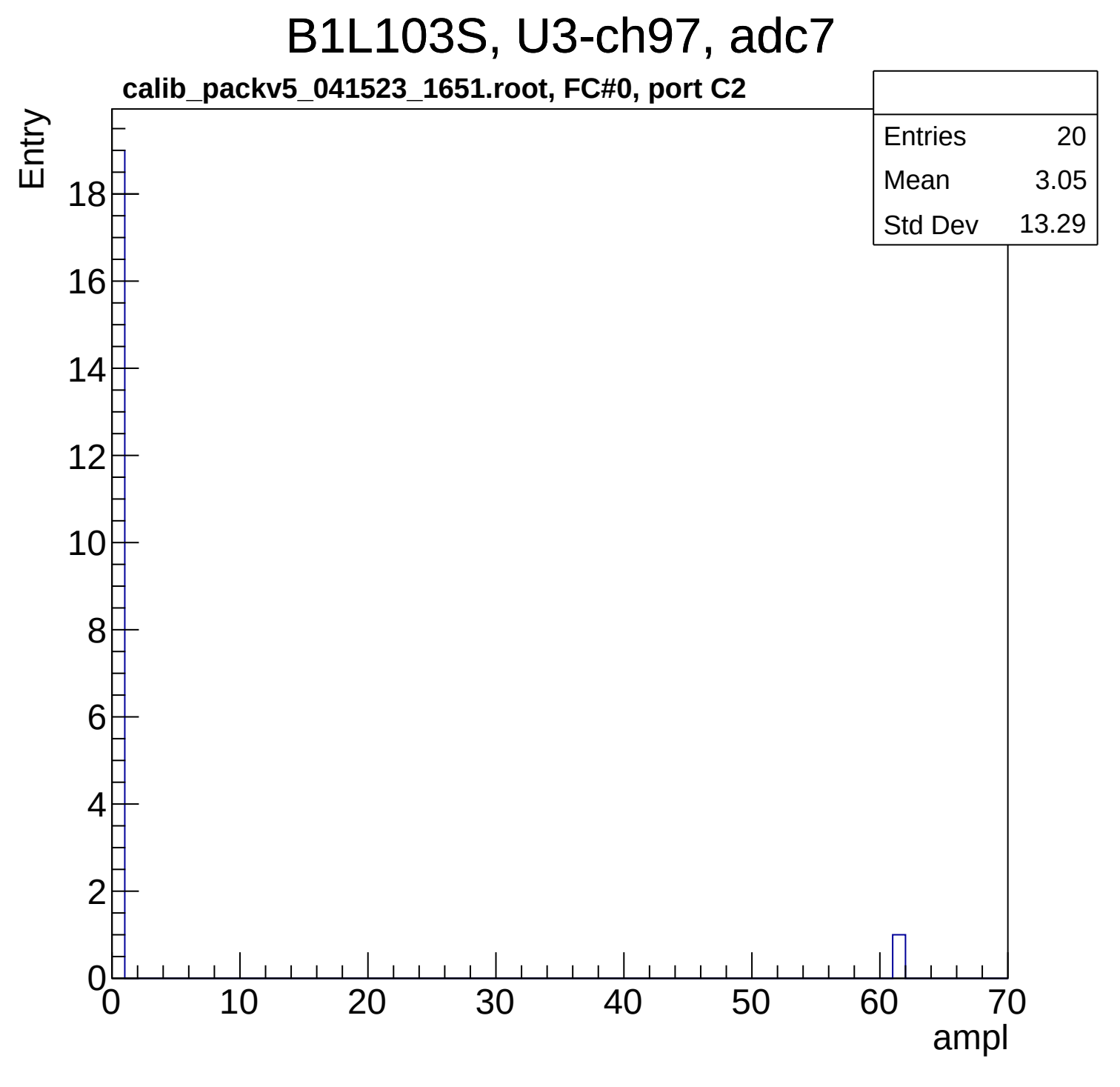
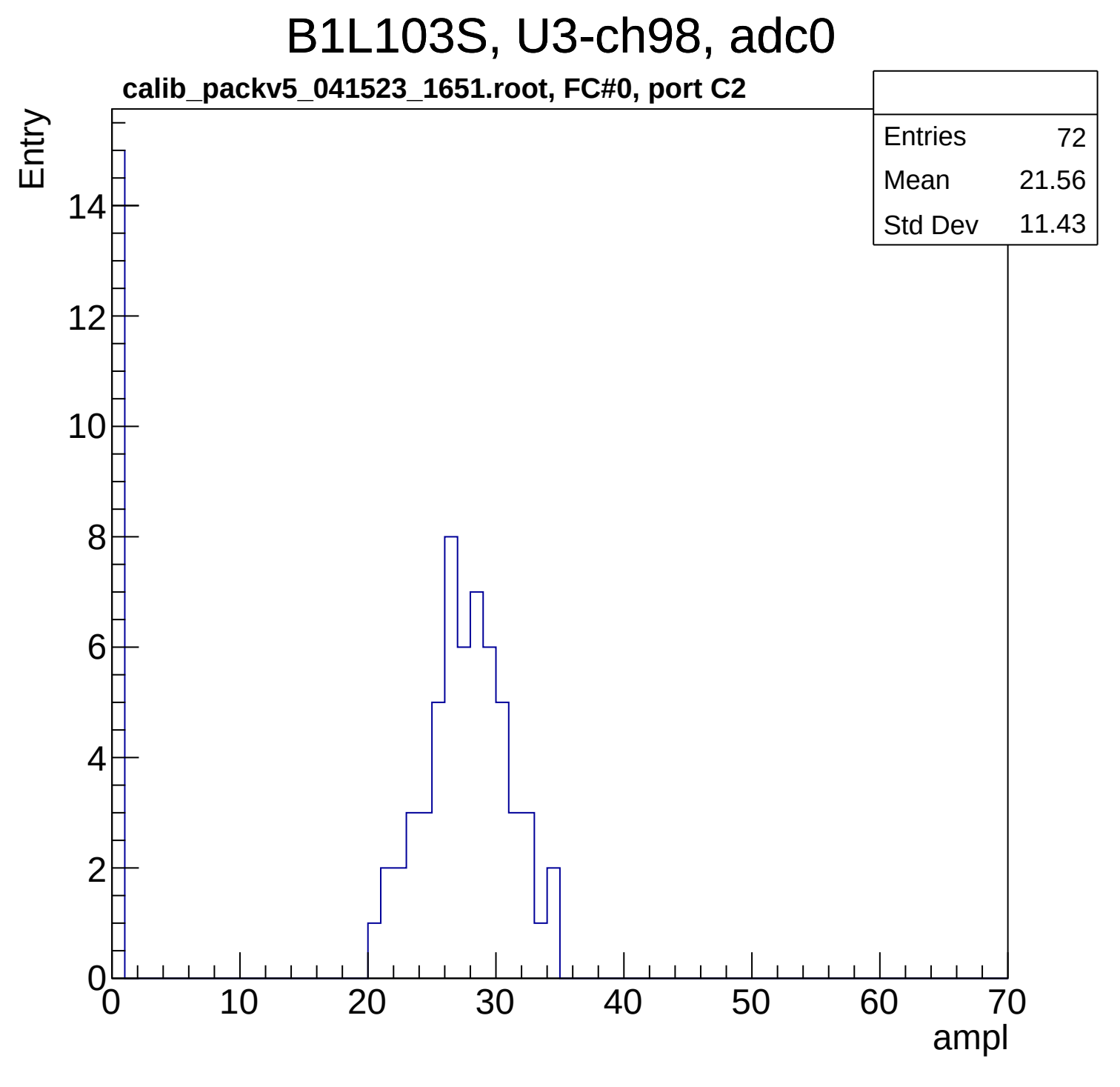
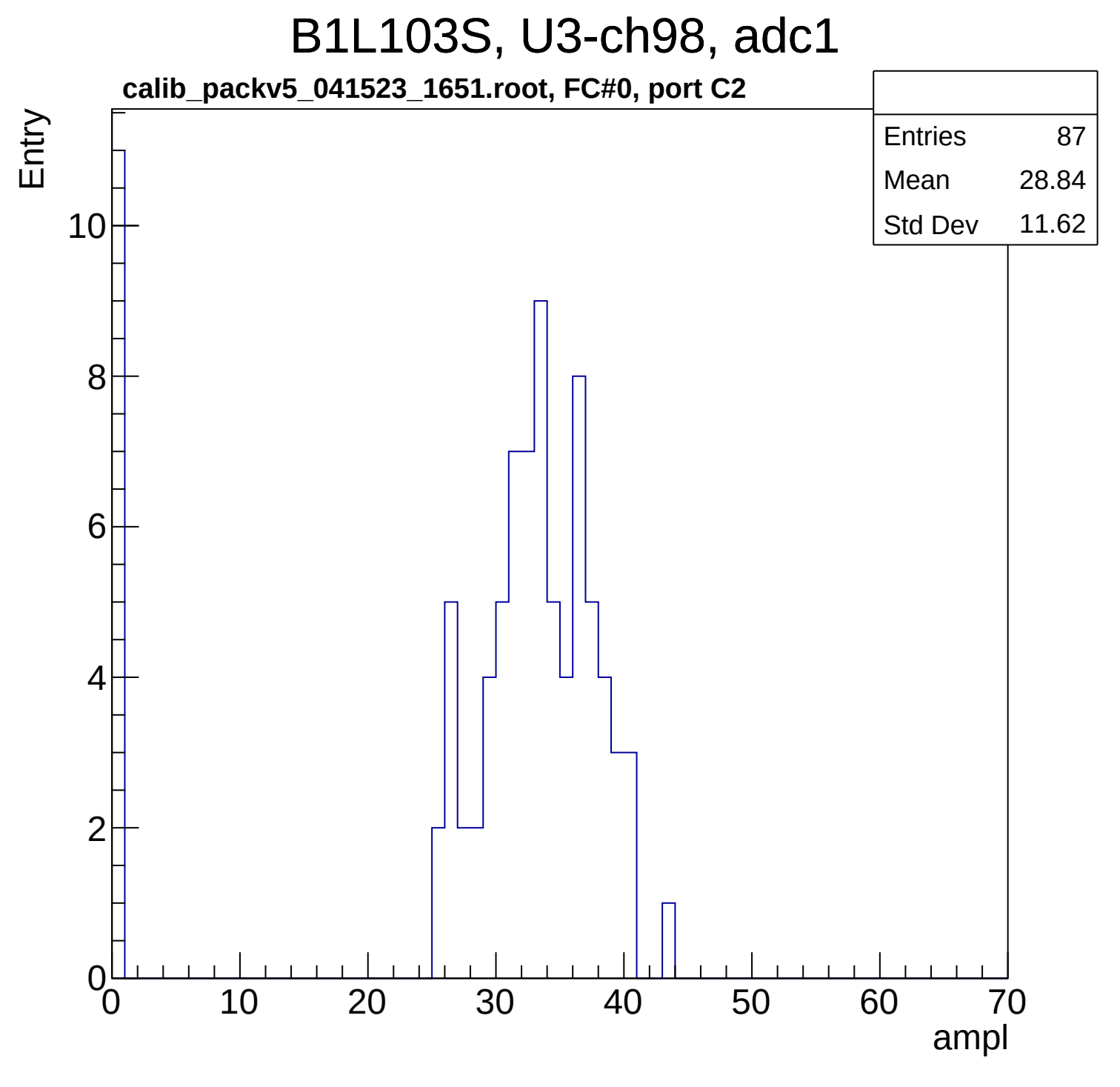
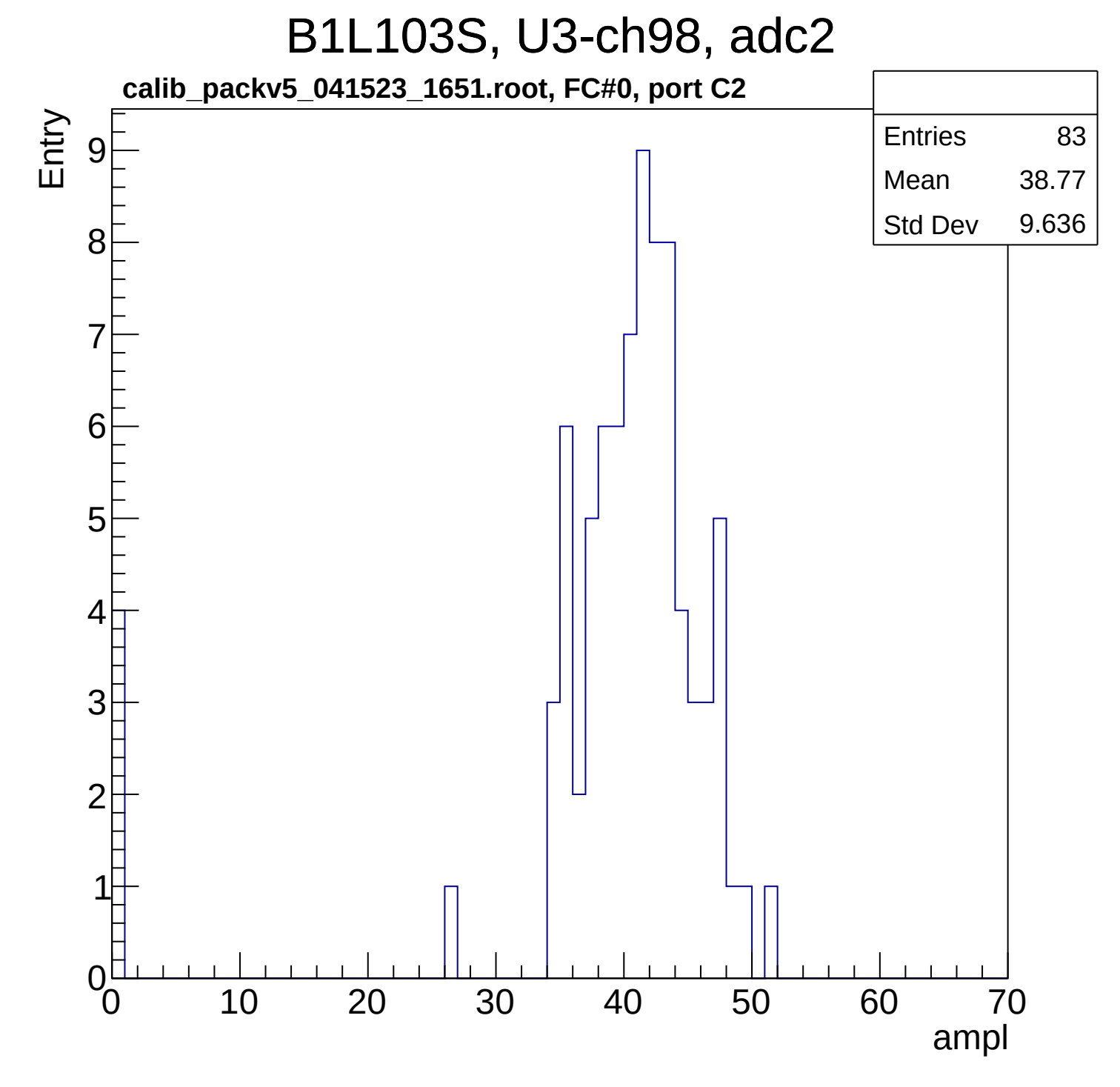
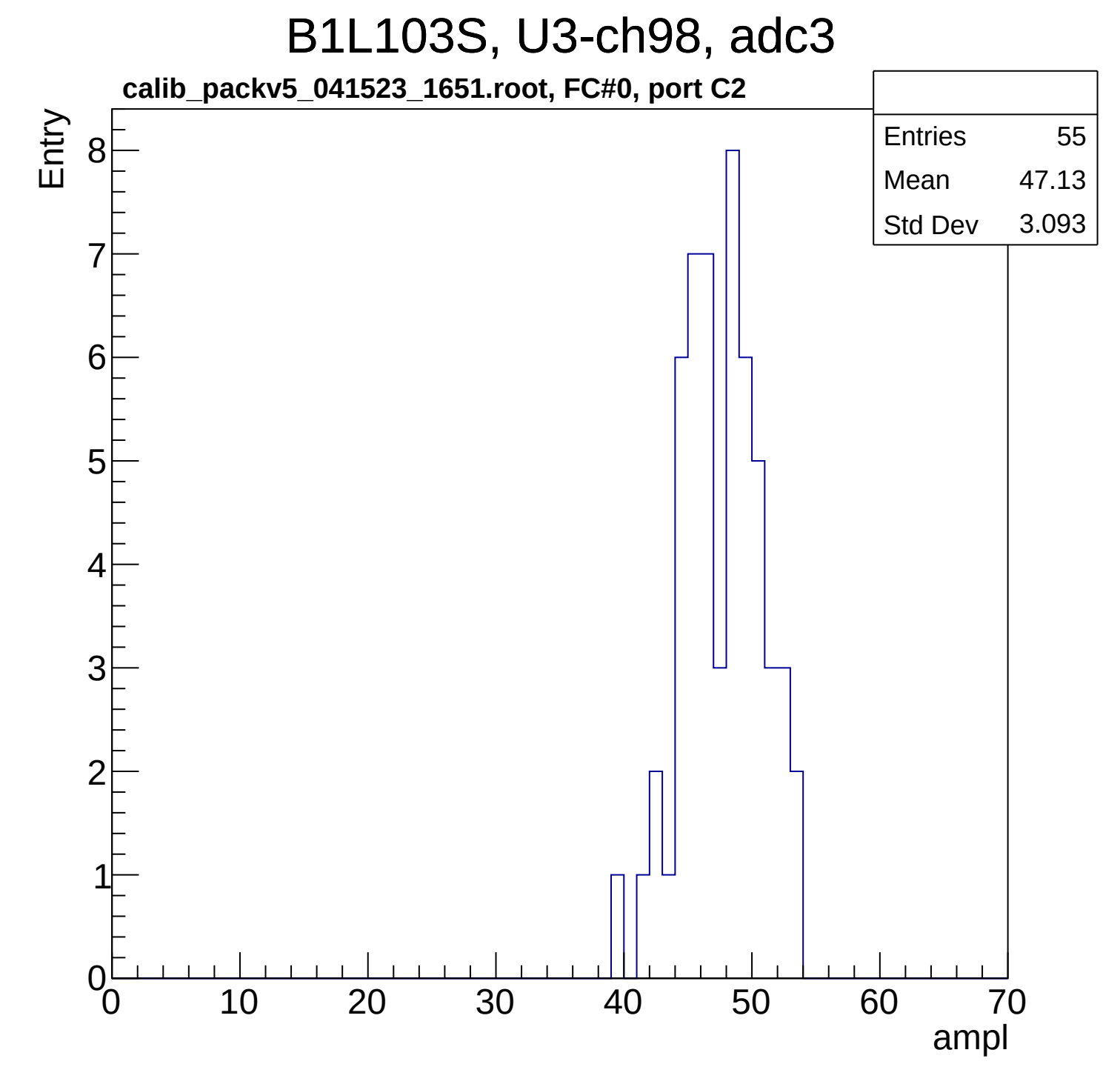
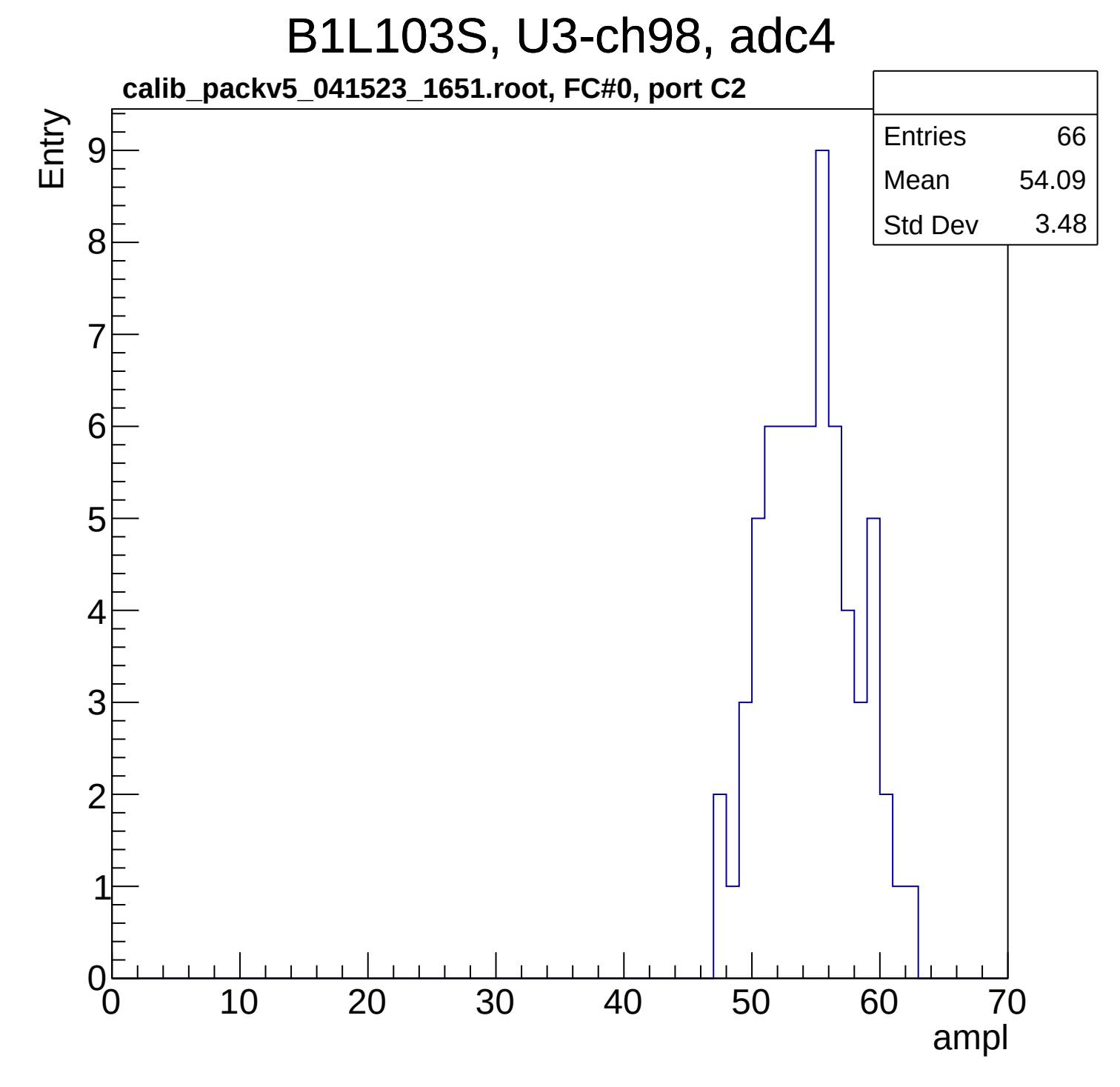

B1L103S, U3-ch97, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.05
Std Dev 13.29
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

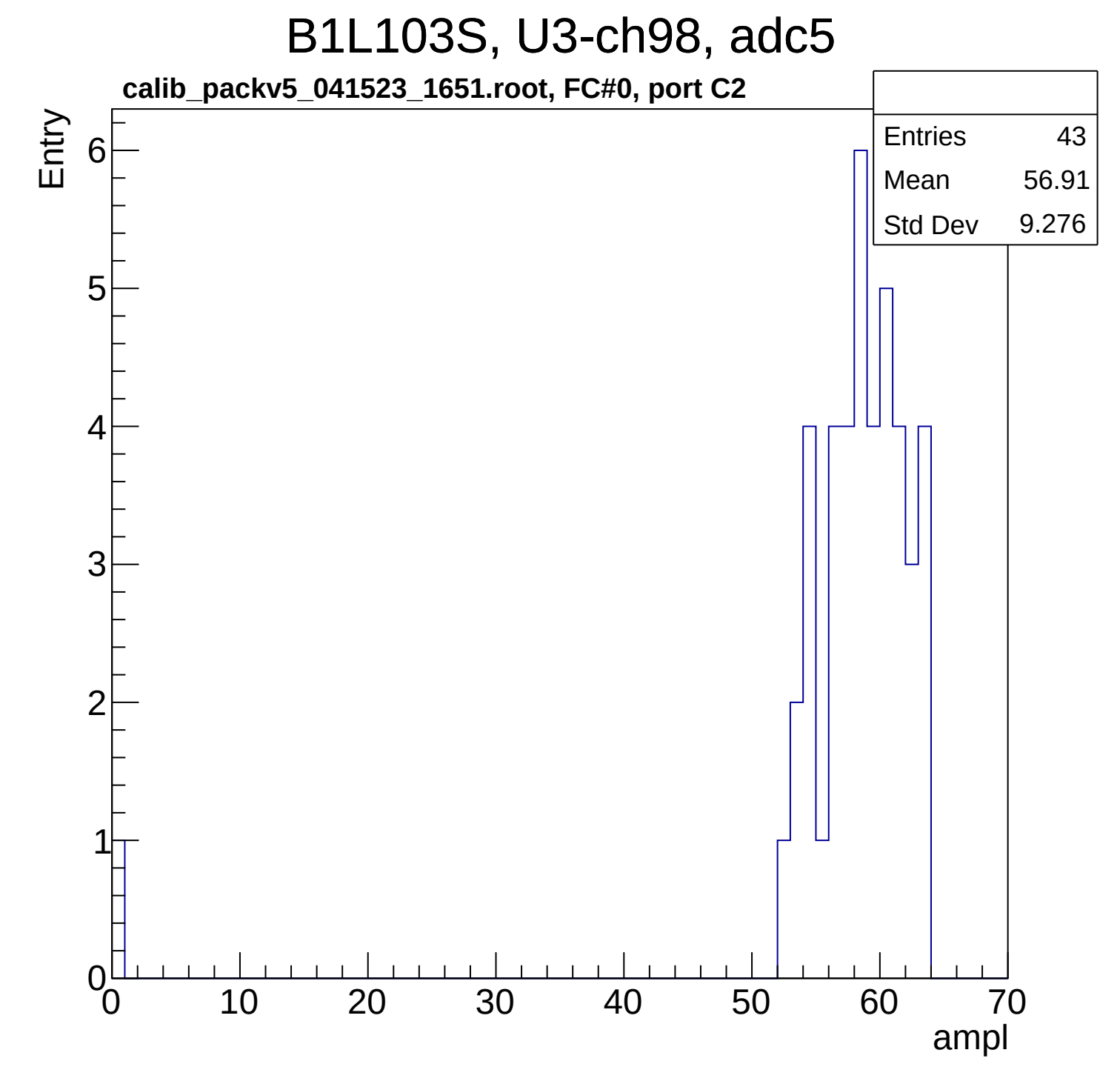

B1L103S, U3-ch98, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 21.56
Std Dev 11.43
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

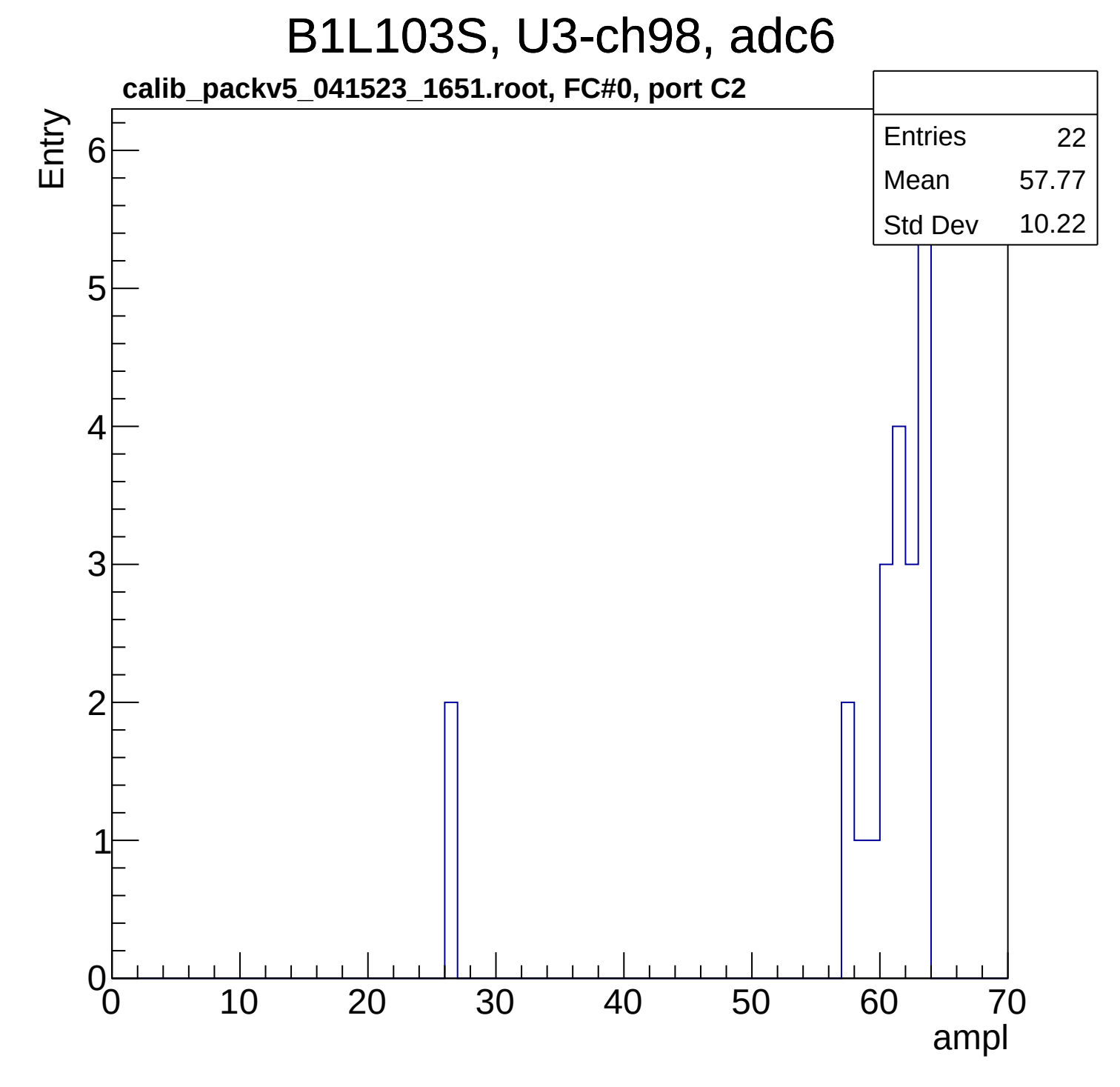

B1L103S, U3-ch98, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 28.84
Std Dev 11.62
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

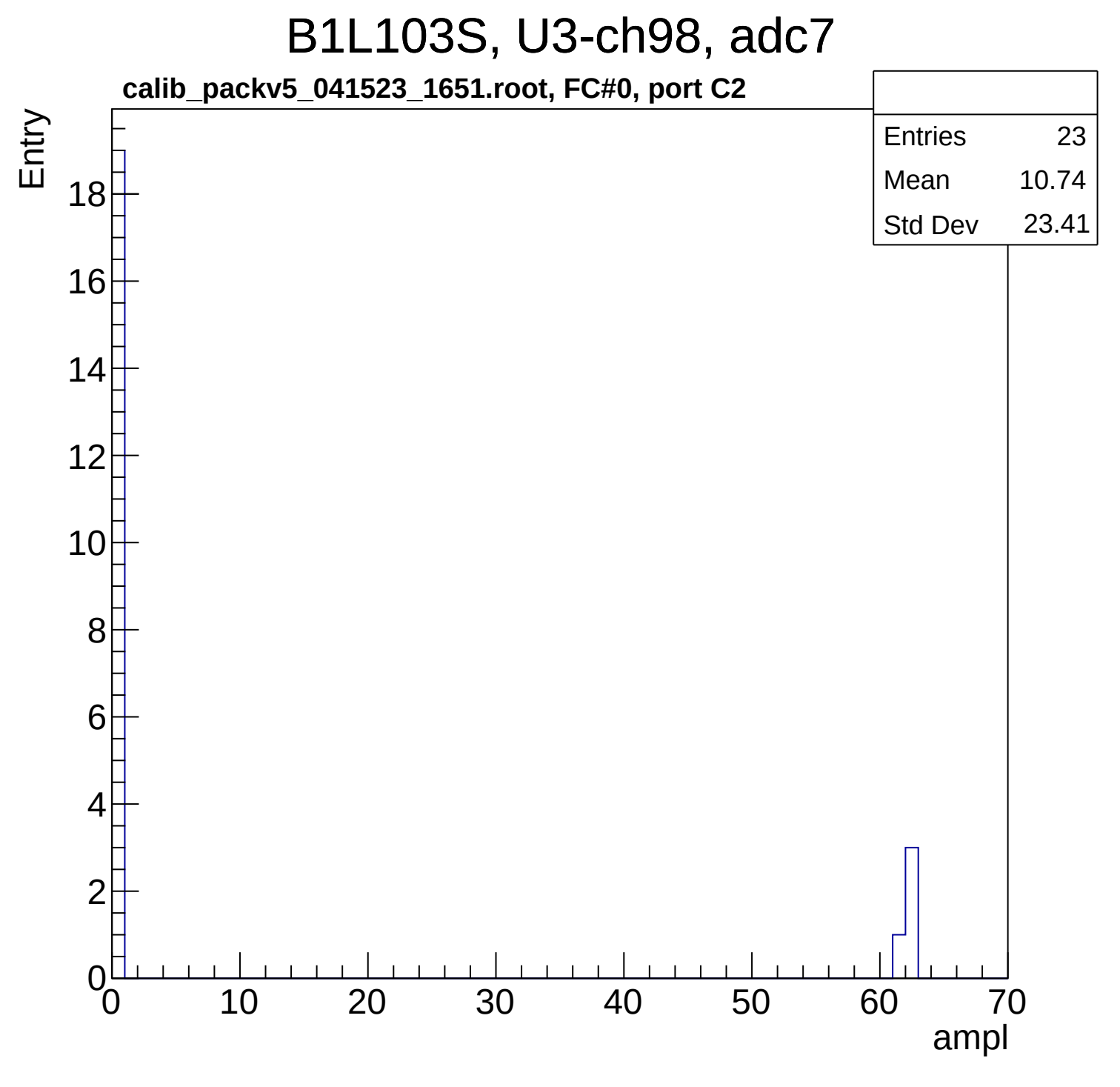

B1L103S, U3-ch98, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 38.77
Std Dev 9.636
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

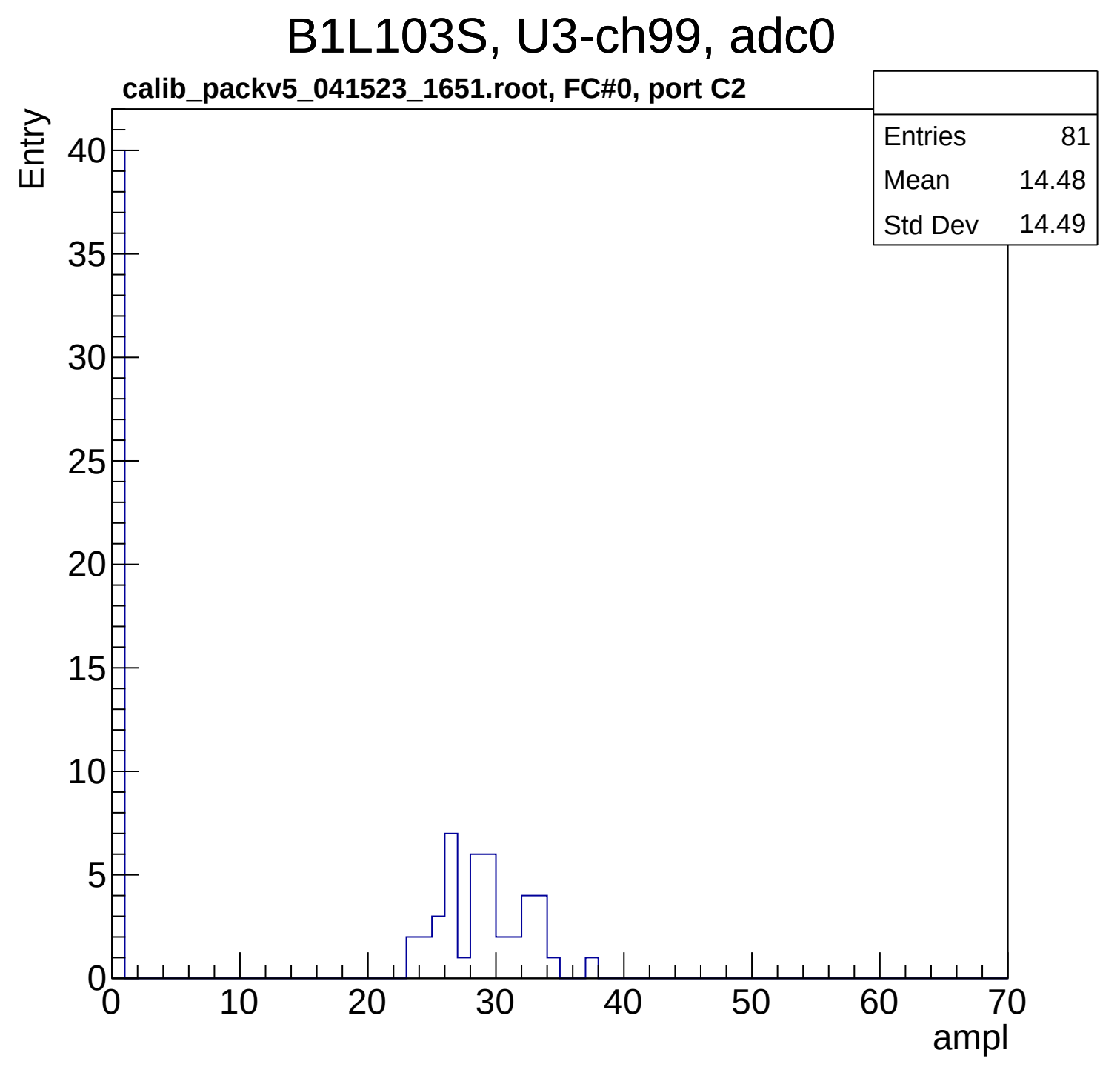

B1L103S, U3-ch98, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 47.13
Std Dev 3.093
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch98, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 54.09
Std Dev 3.48
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch98, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 56.91
Std Dev 9.276
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U3-ch98, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 57.77
Std Dev 10.22
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U3-ch98, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 10.74
Std Dev 23.41
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch99, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 14.48
Std Dev 14.49
Entry
ampl
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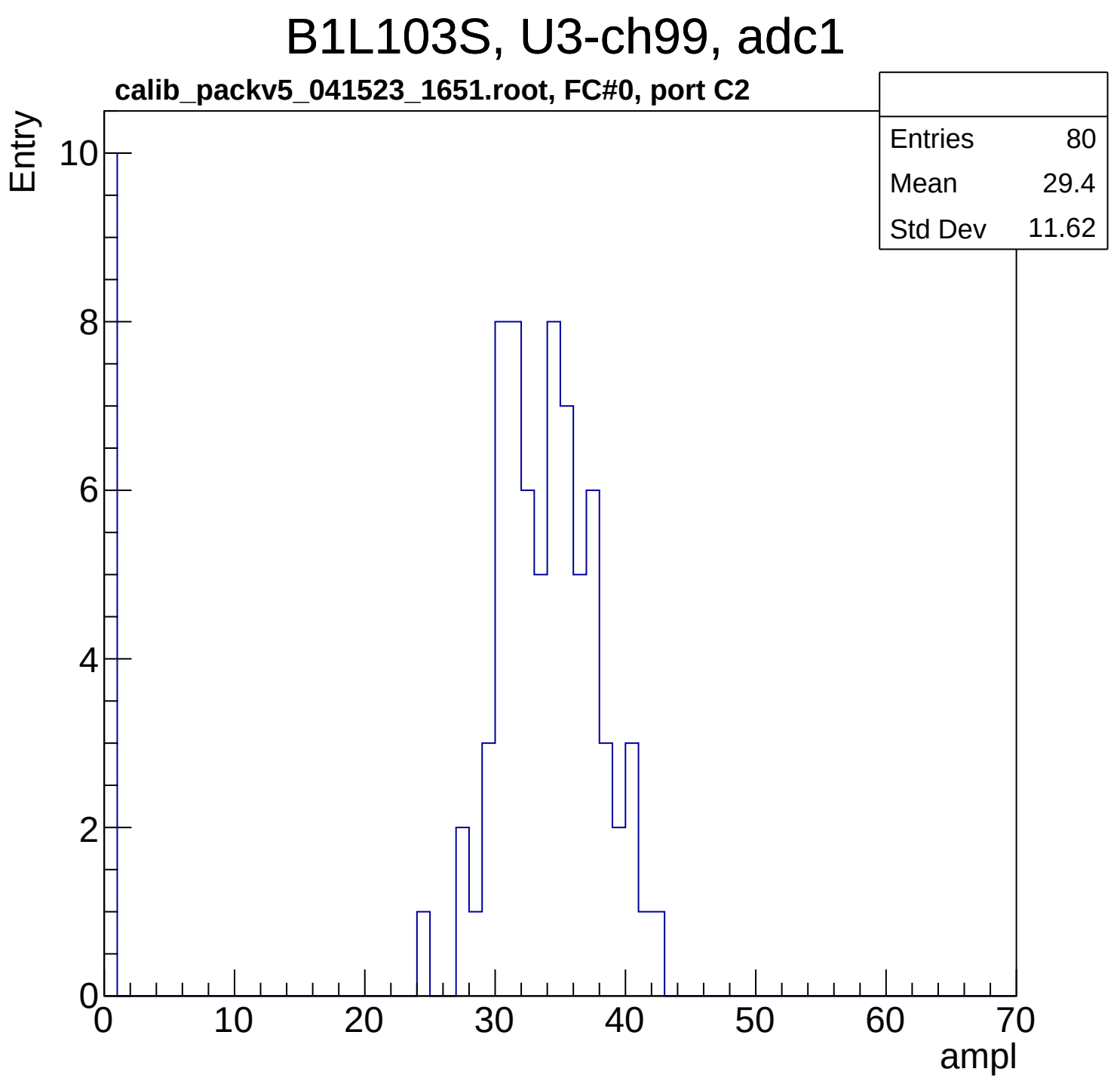
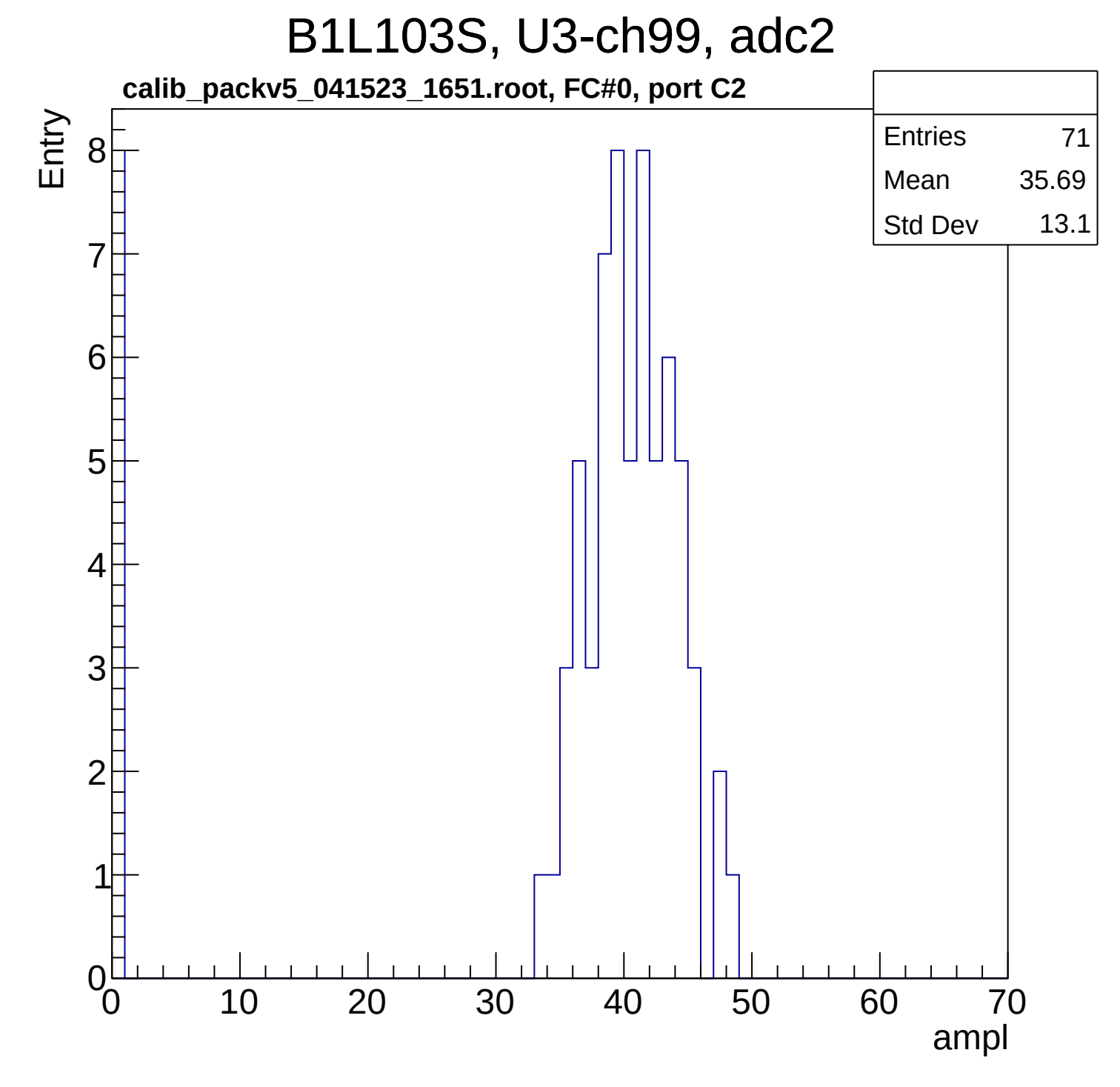
5
10
15
20
25
30
35
40
0
10
20
30
40
50
60
70


B1L103S, U3-ch99, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 29.4
Std Dev 11.62
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch99, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 35.69
Std Dev 13.1
Entry
ampl
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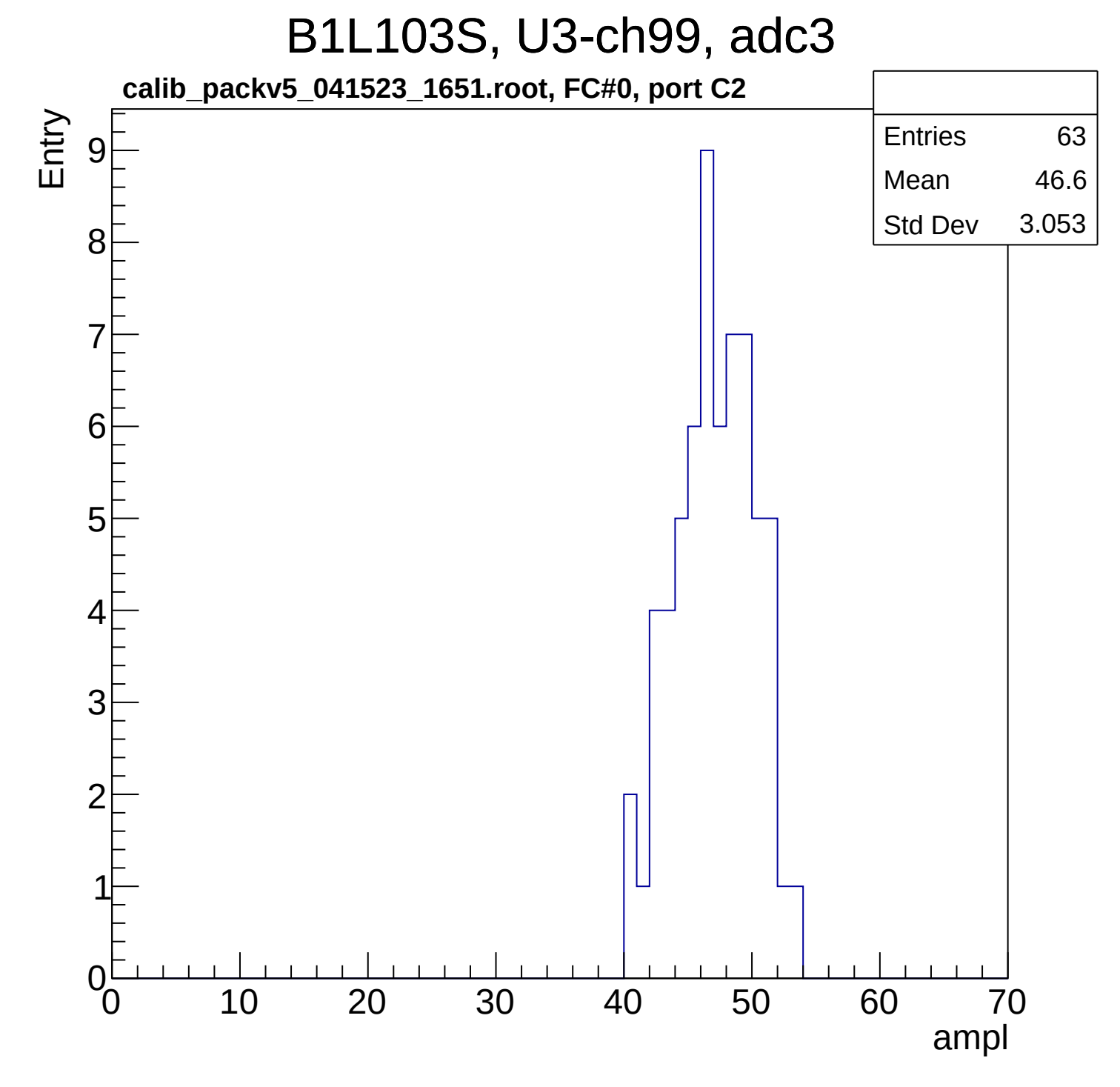
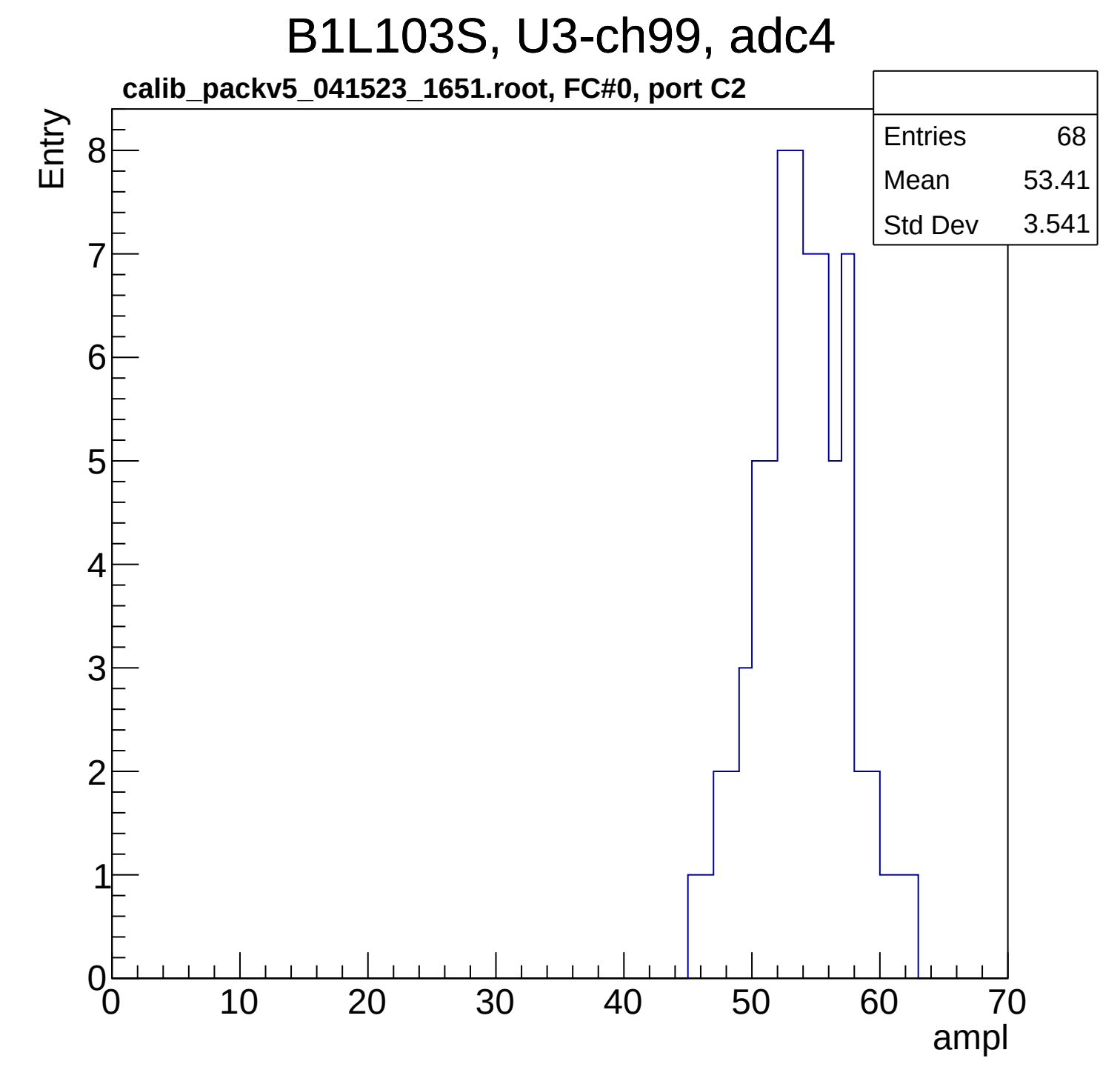
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch99, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 46.6
Std Dev 3.053
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch99, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 53.41
Std Dev 3.541
Entry
ampl
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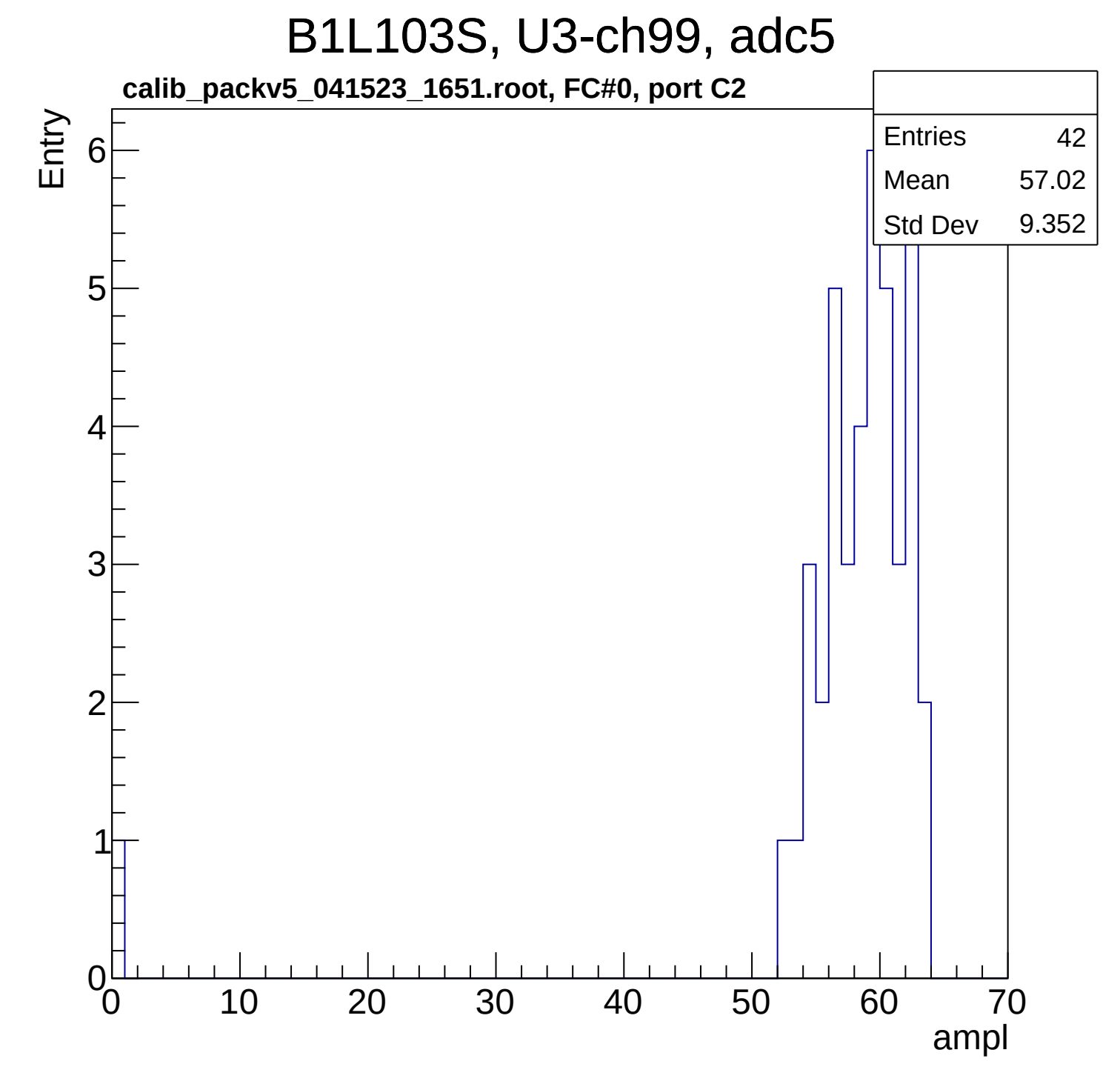
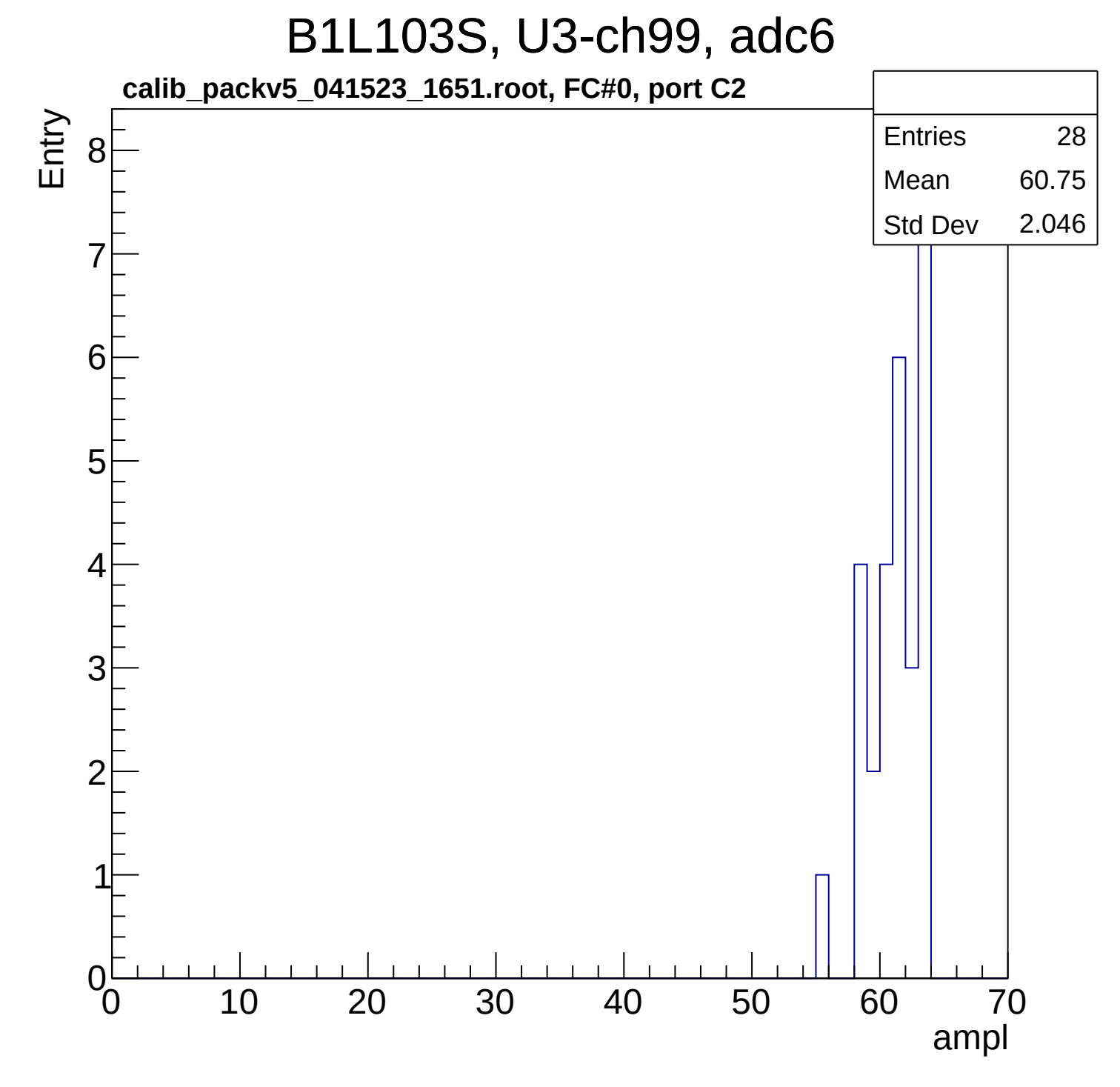
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch99, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 57.02
Std Dev 9.352
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U3-ch99, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 60.75
Std Dev 2.046
Entry
ampl
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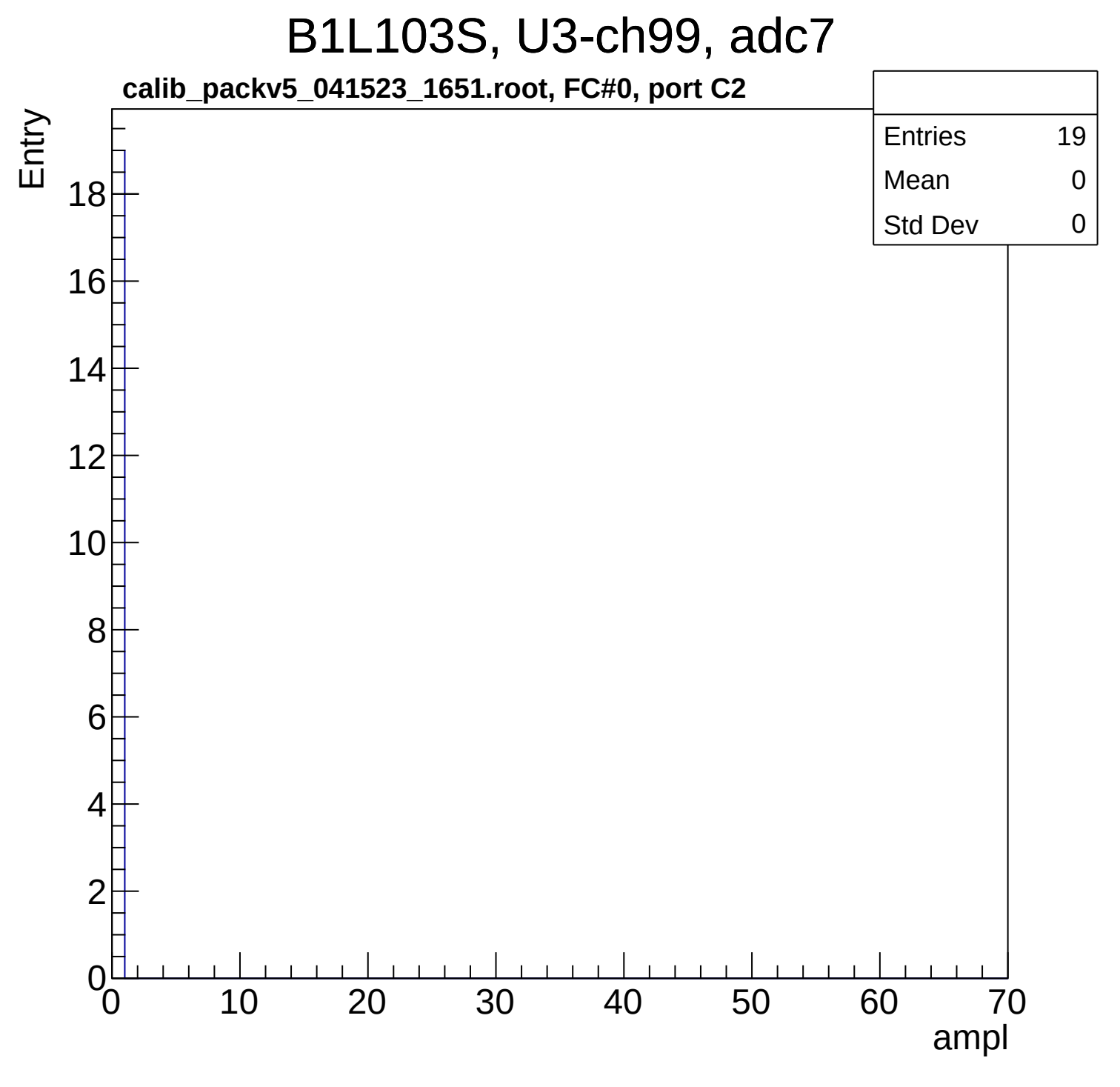
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch99, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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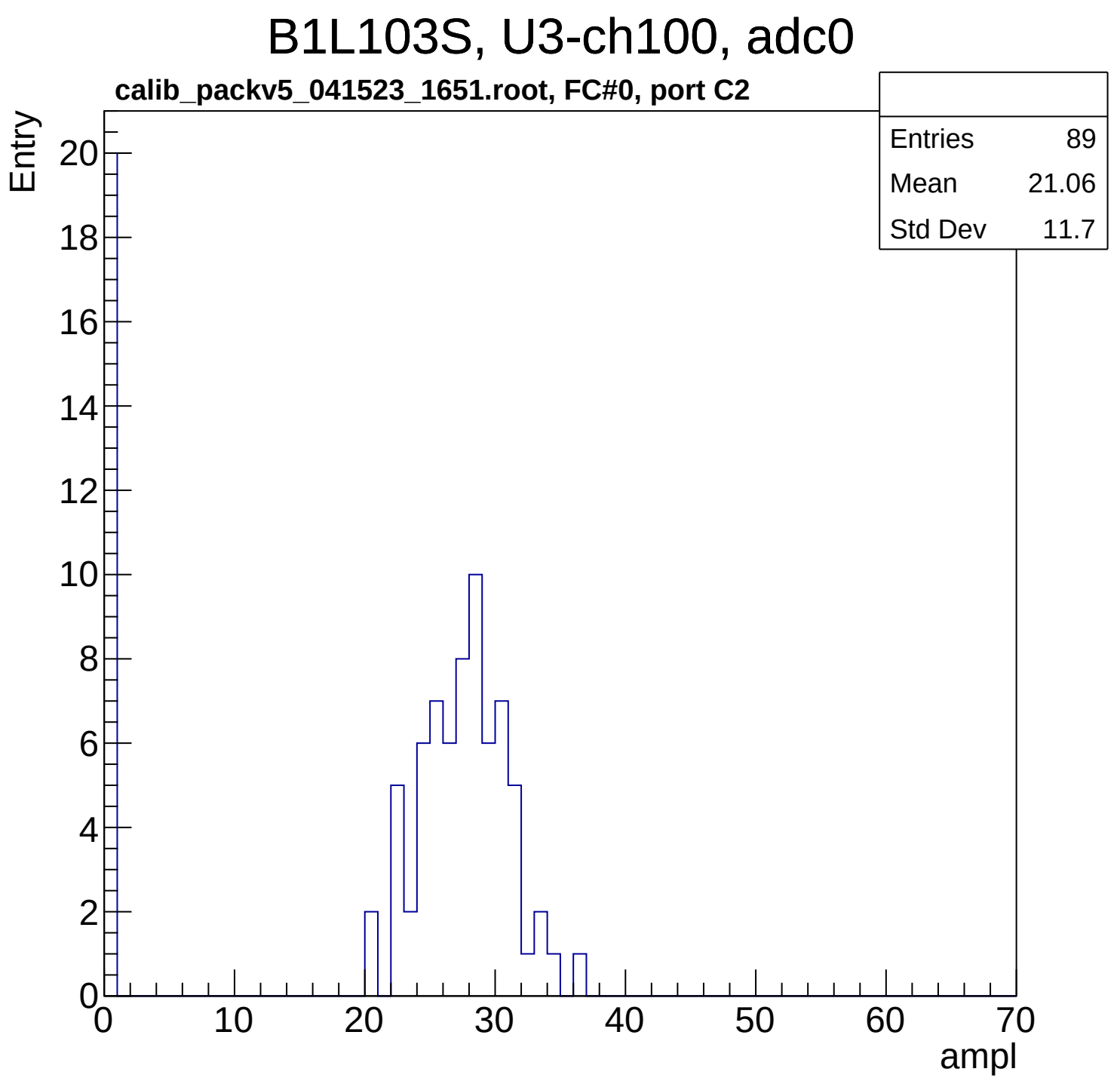
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch100, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 21.06
Std Dev 11.7
Entry
0
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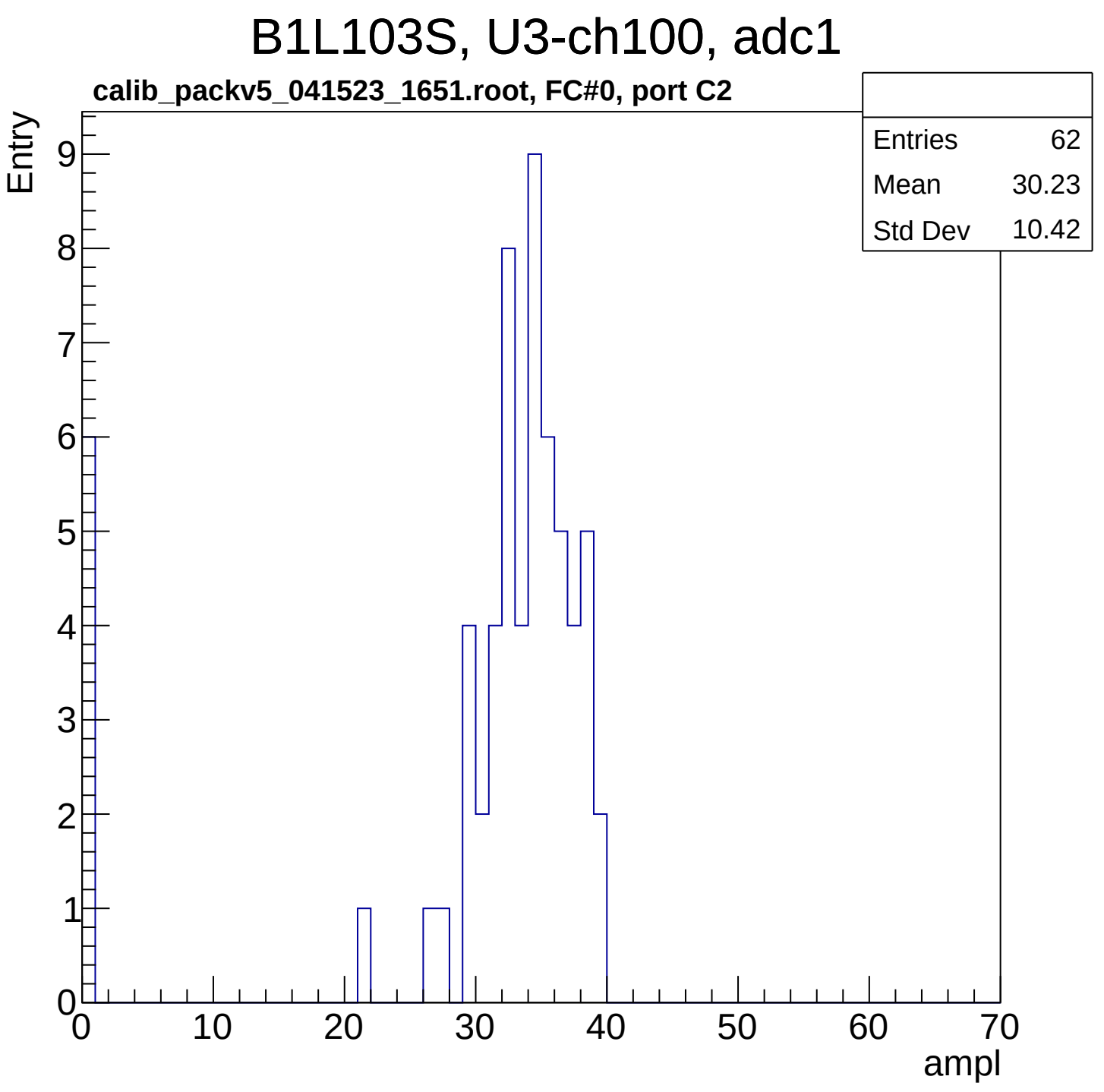
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch100, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 30.23
Std Dev 10.42
Entry
ampl
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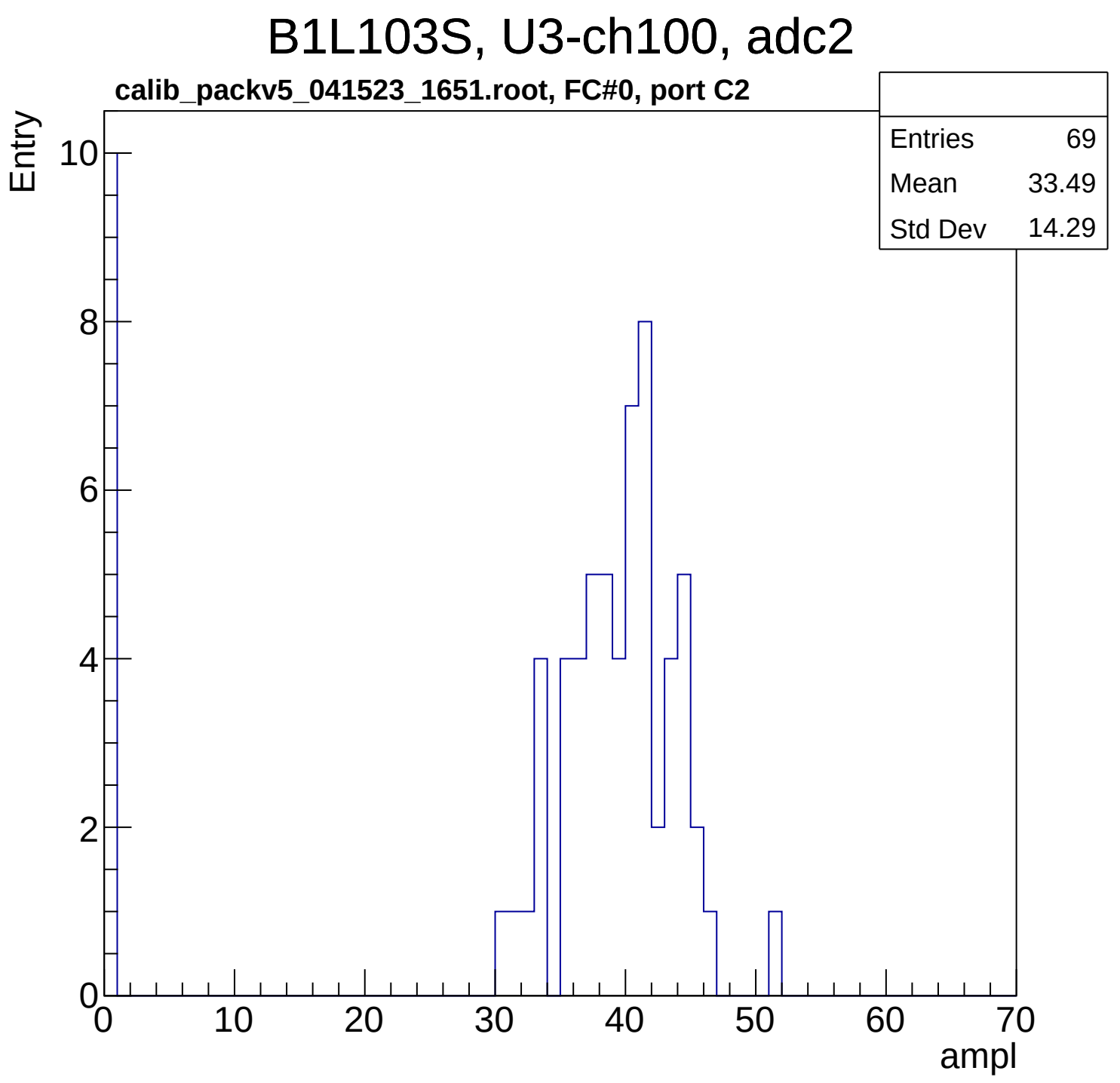
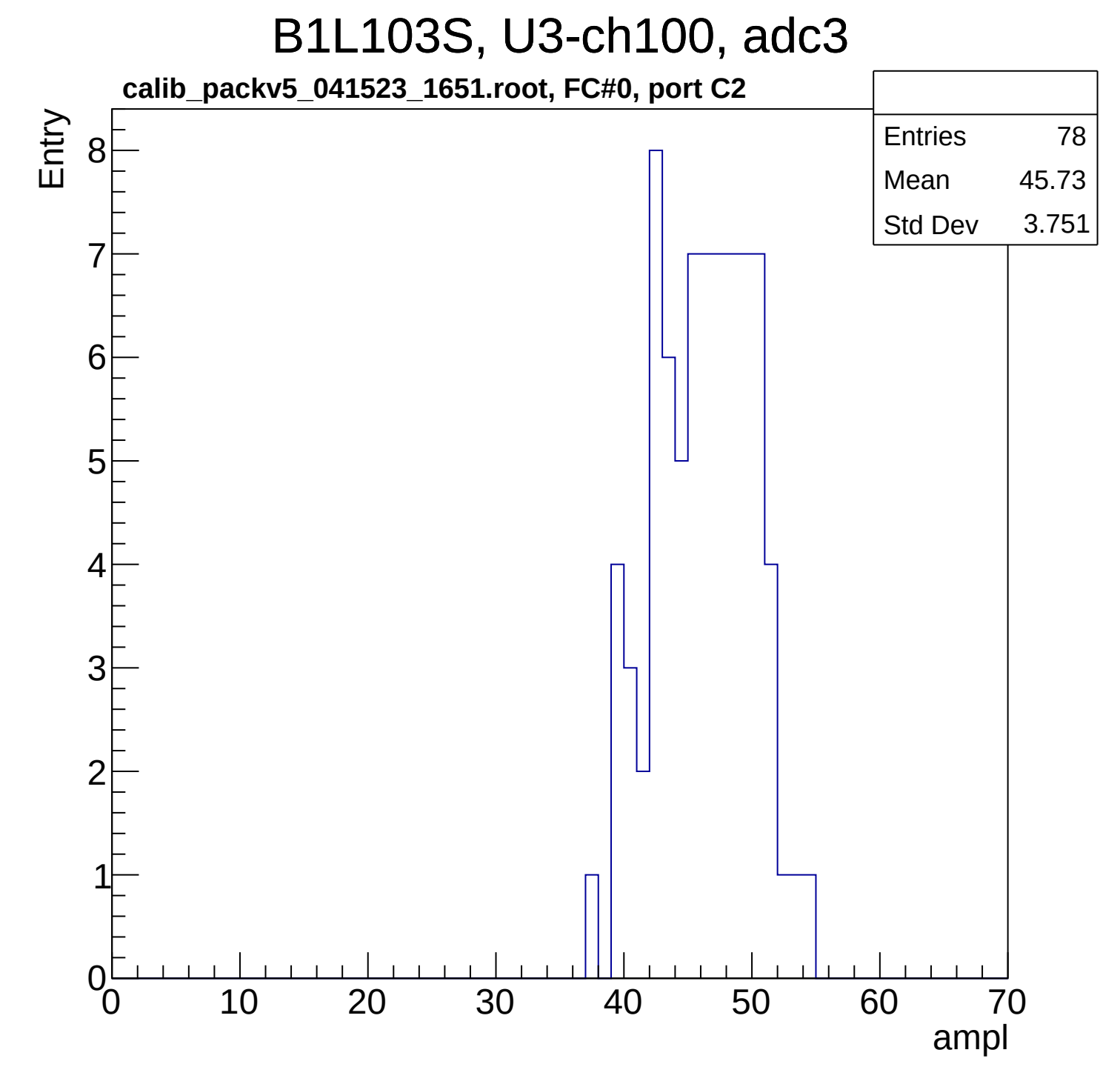
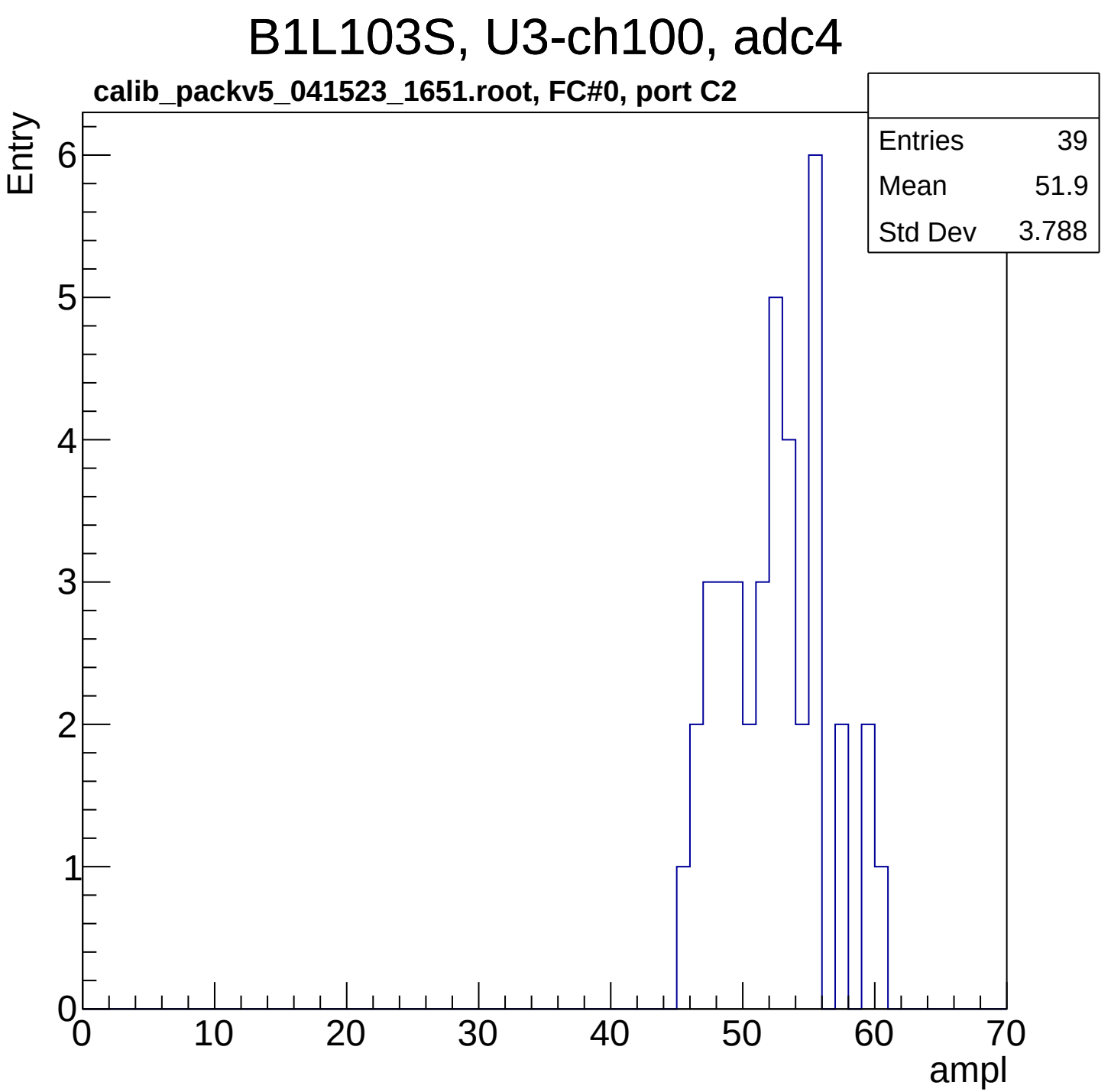
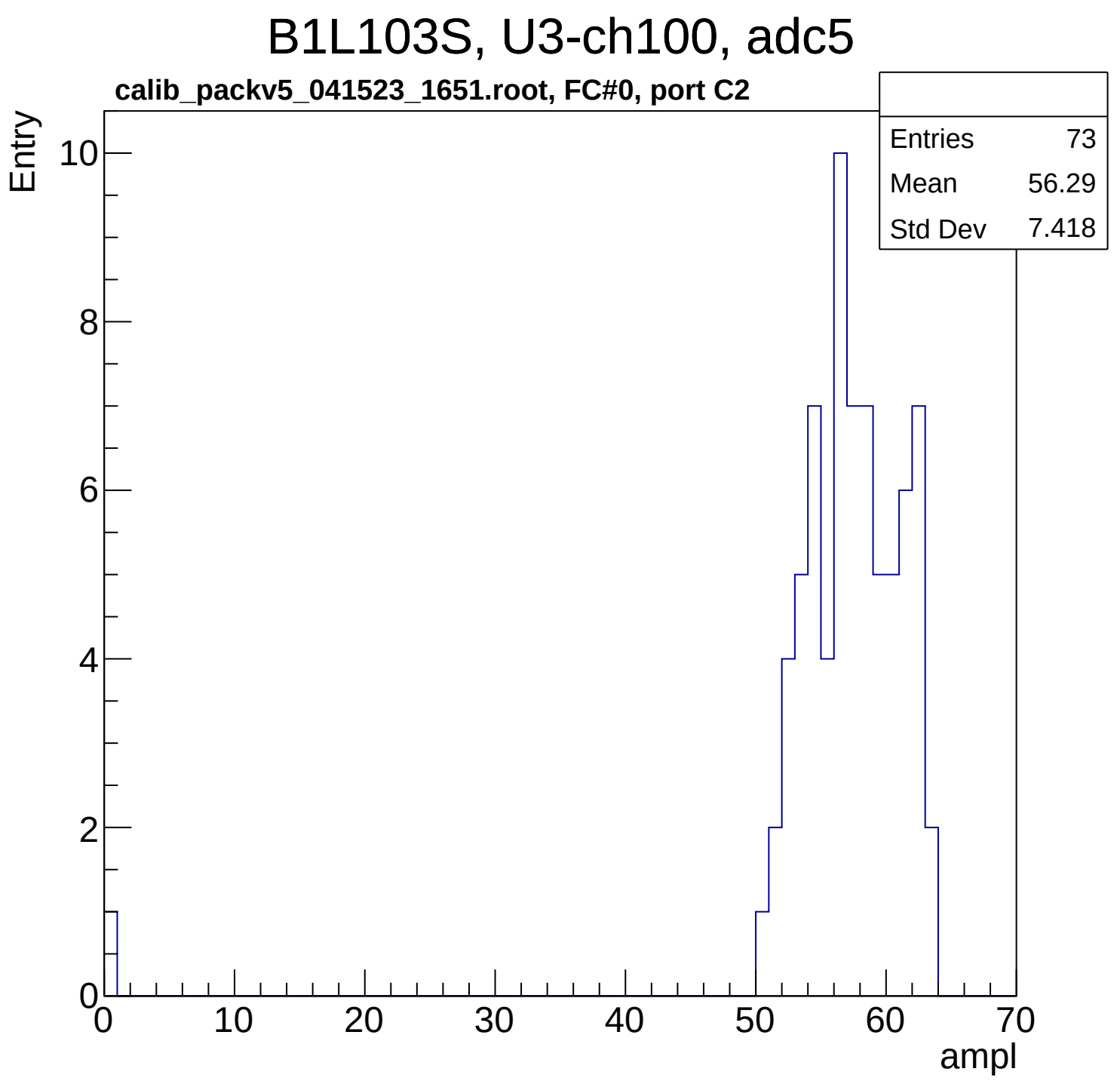
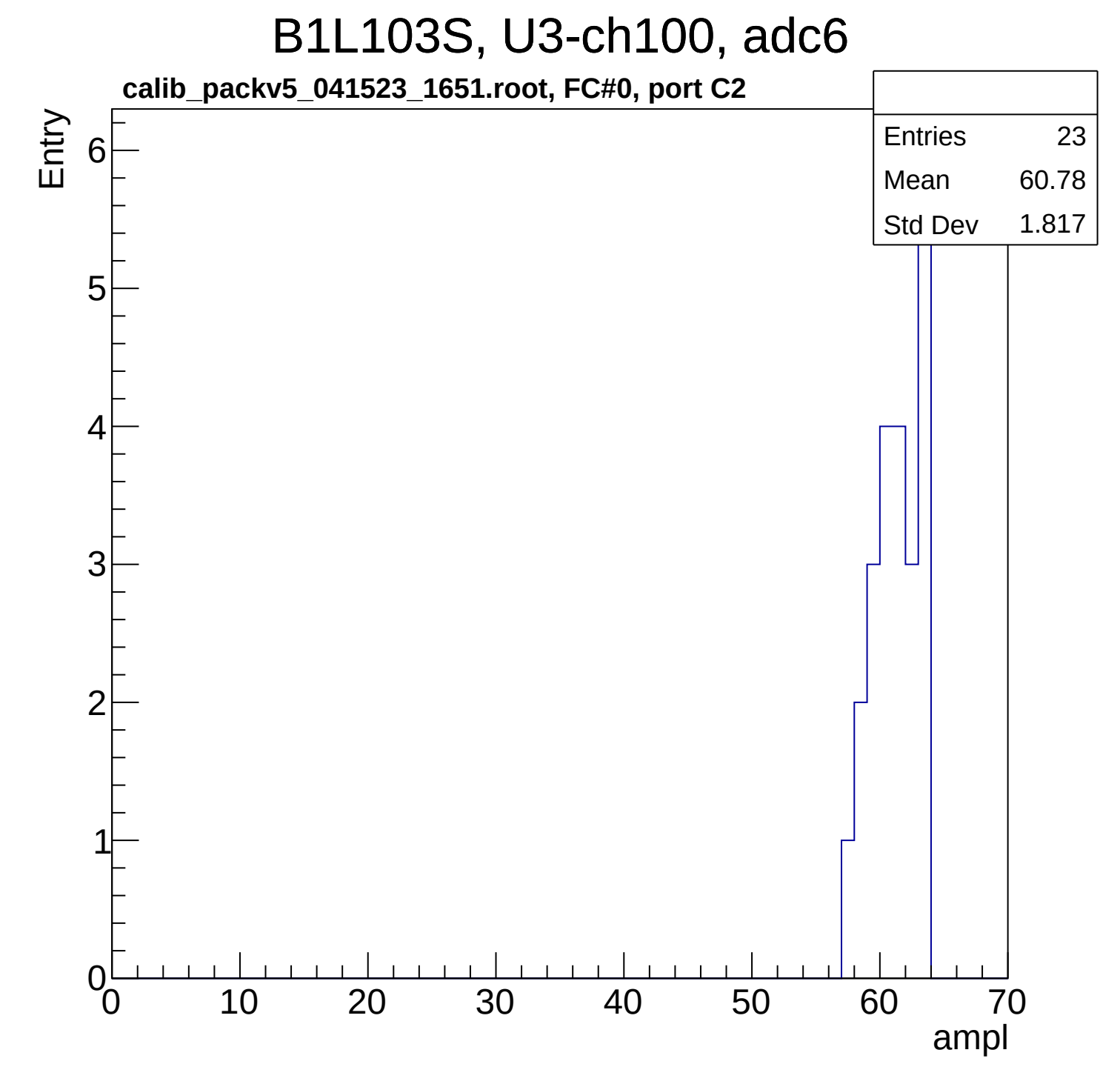
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

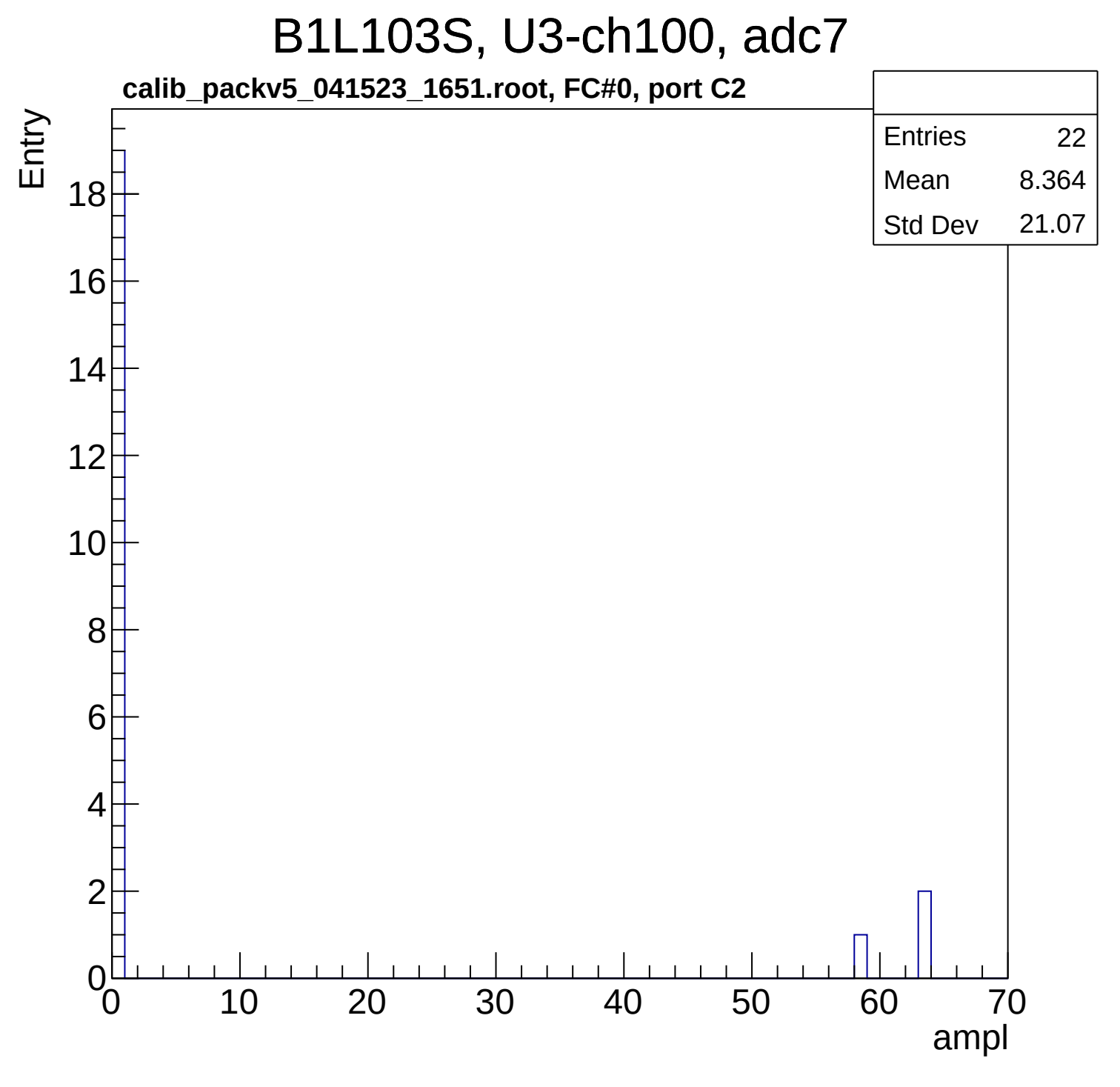

B1L103S, U3-ch100, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 33.49
Std Dev 14.29
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U3-ch100, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 45.73
Std Dev 3.751
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch100, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 51.9
Std Dev 3.788
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch100, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 56.29
Std Dev 7.418
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U3-ch100, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 60.78
Std Dev 1.817
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U3-ch100, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.364
Std Dev 21.07
Entry
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6
8
10
12
14
16
18
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10
20
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50
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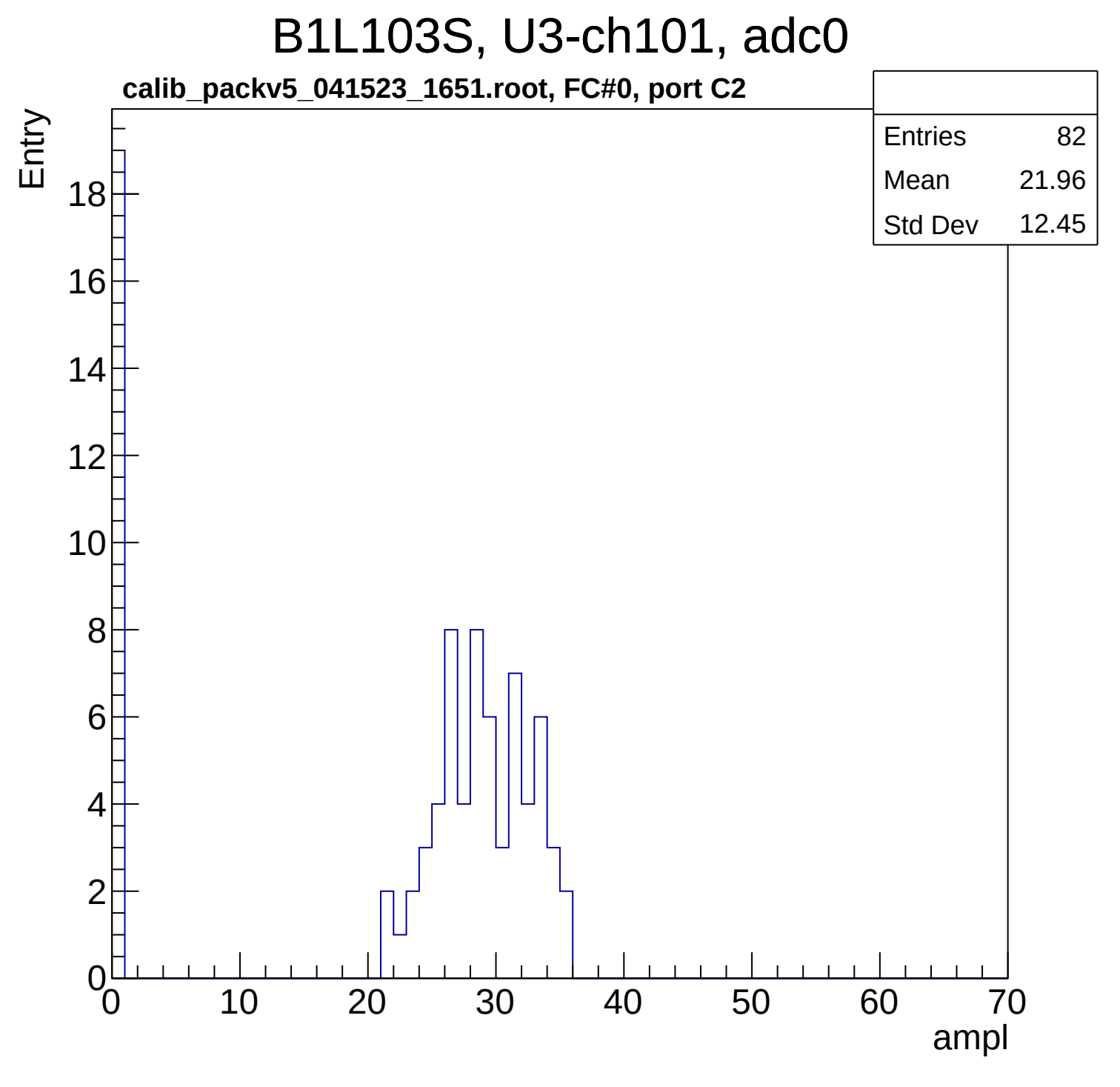
70
ampl


B1L103S, U3-ch101, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 21.96
Std Dev 12.45
Entry
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8
10
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14
16
18
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10
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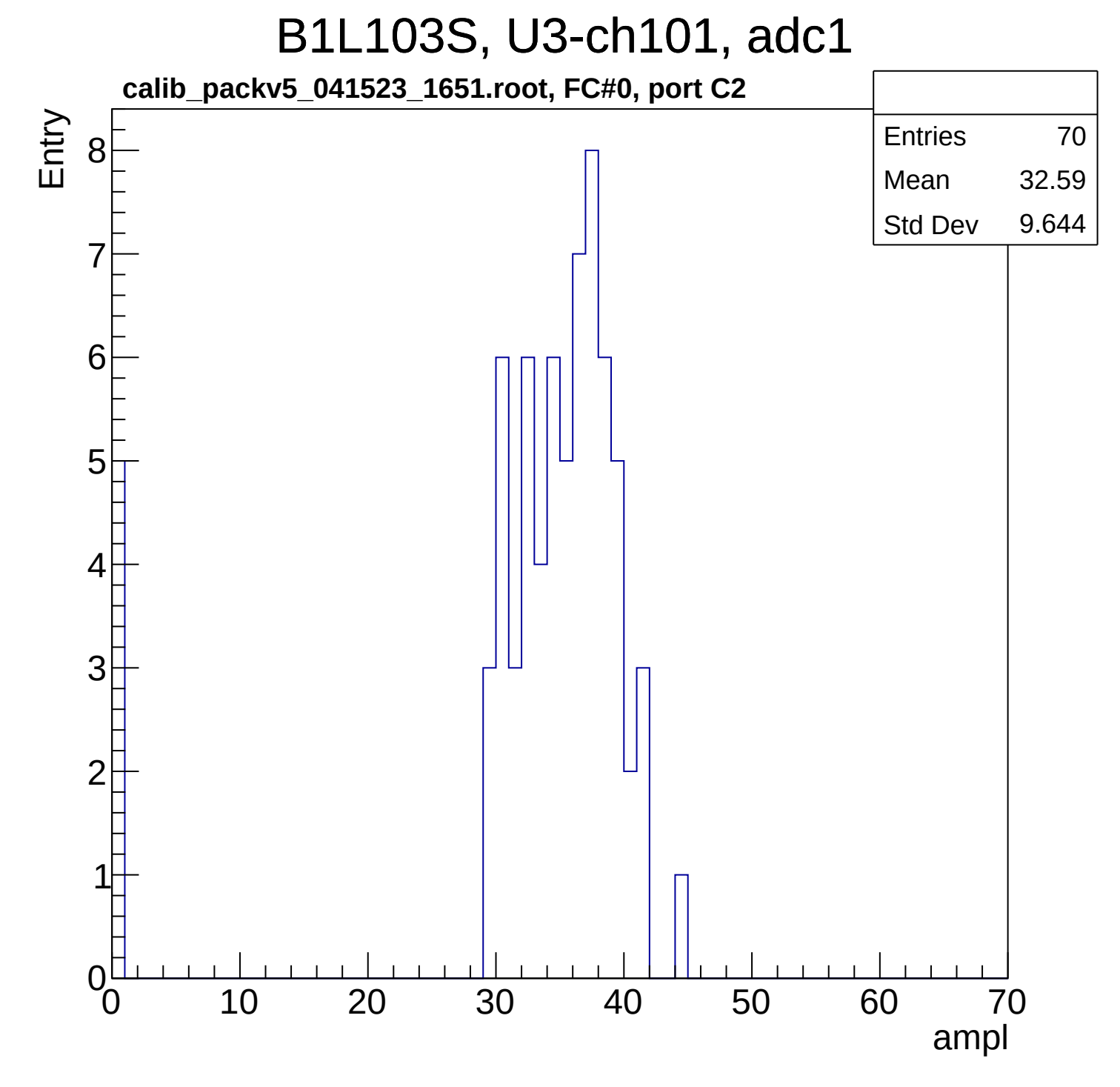
70
ampl


B1L103S, U3-ch101, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 32.59
Std Dev 9.644
Entry
ampl
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2
3
4
5
6
7
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0
10
20
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40
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60
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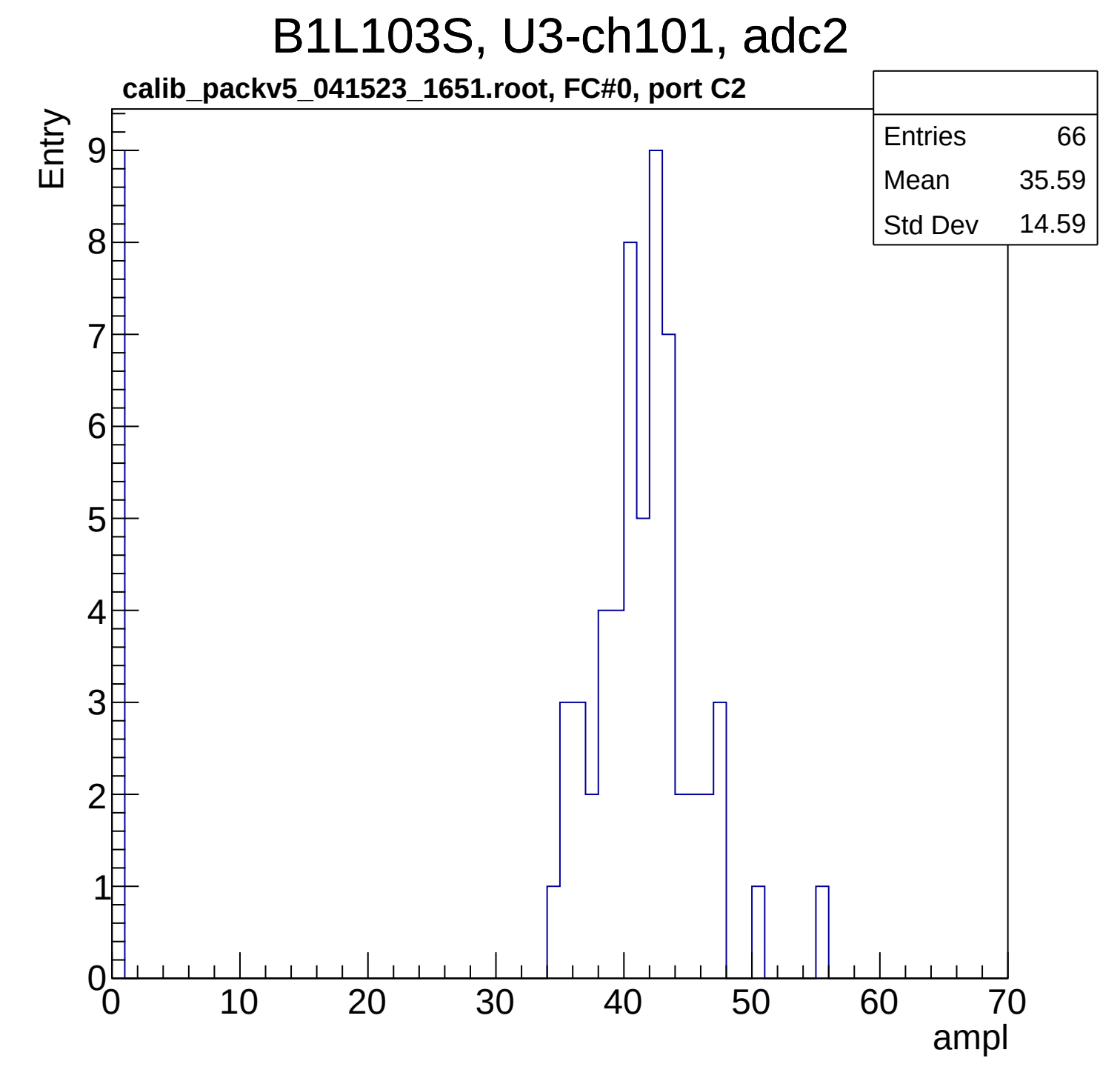
B1L103S, U3-ch101, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 35.59
Std Dev 14.59
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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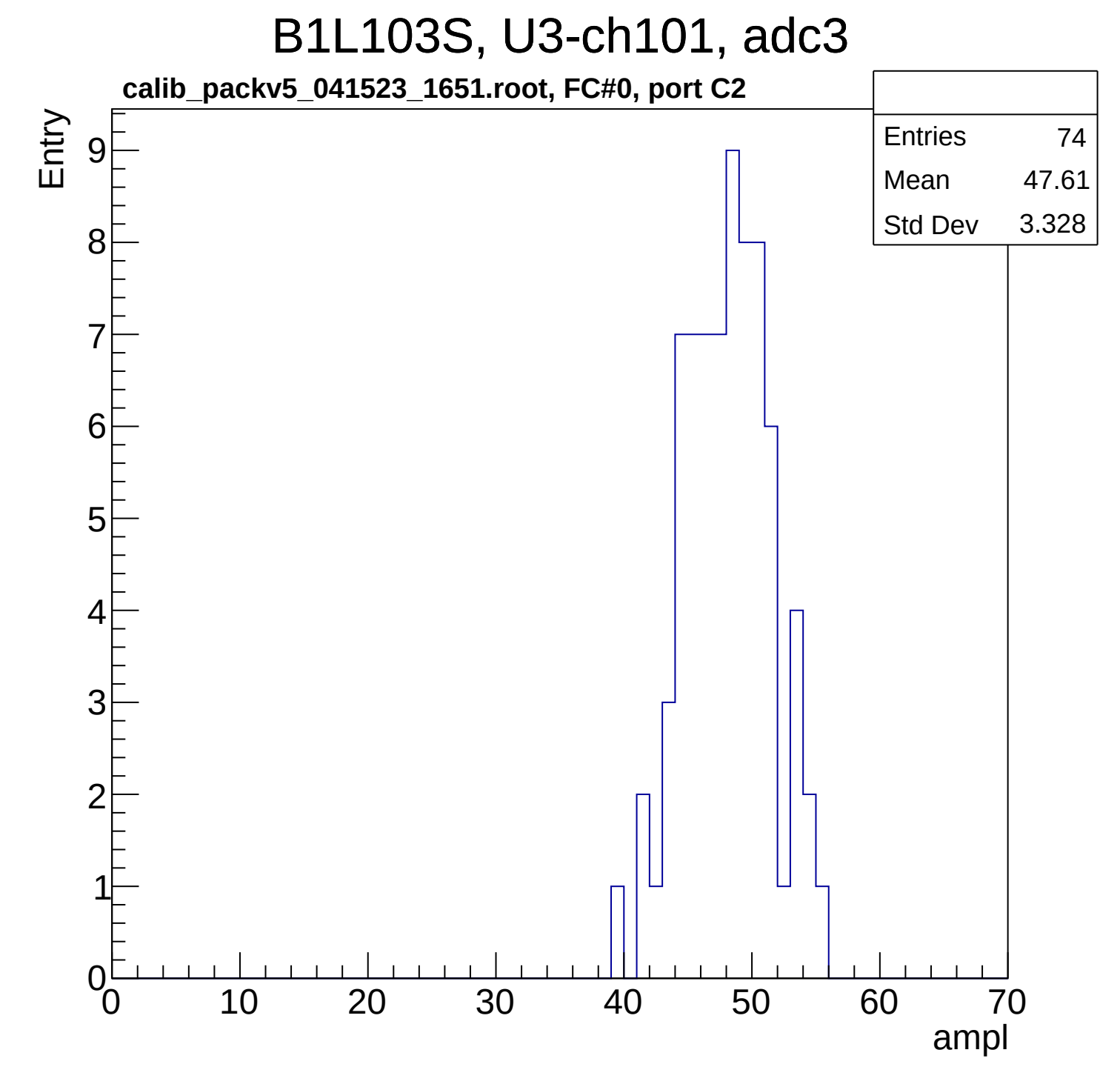
B1L103S, U3-ch101, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 47.61
Std Dev 3.328
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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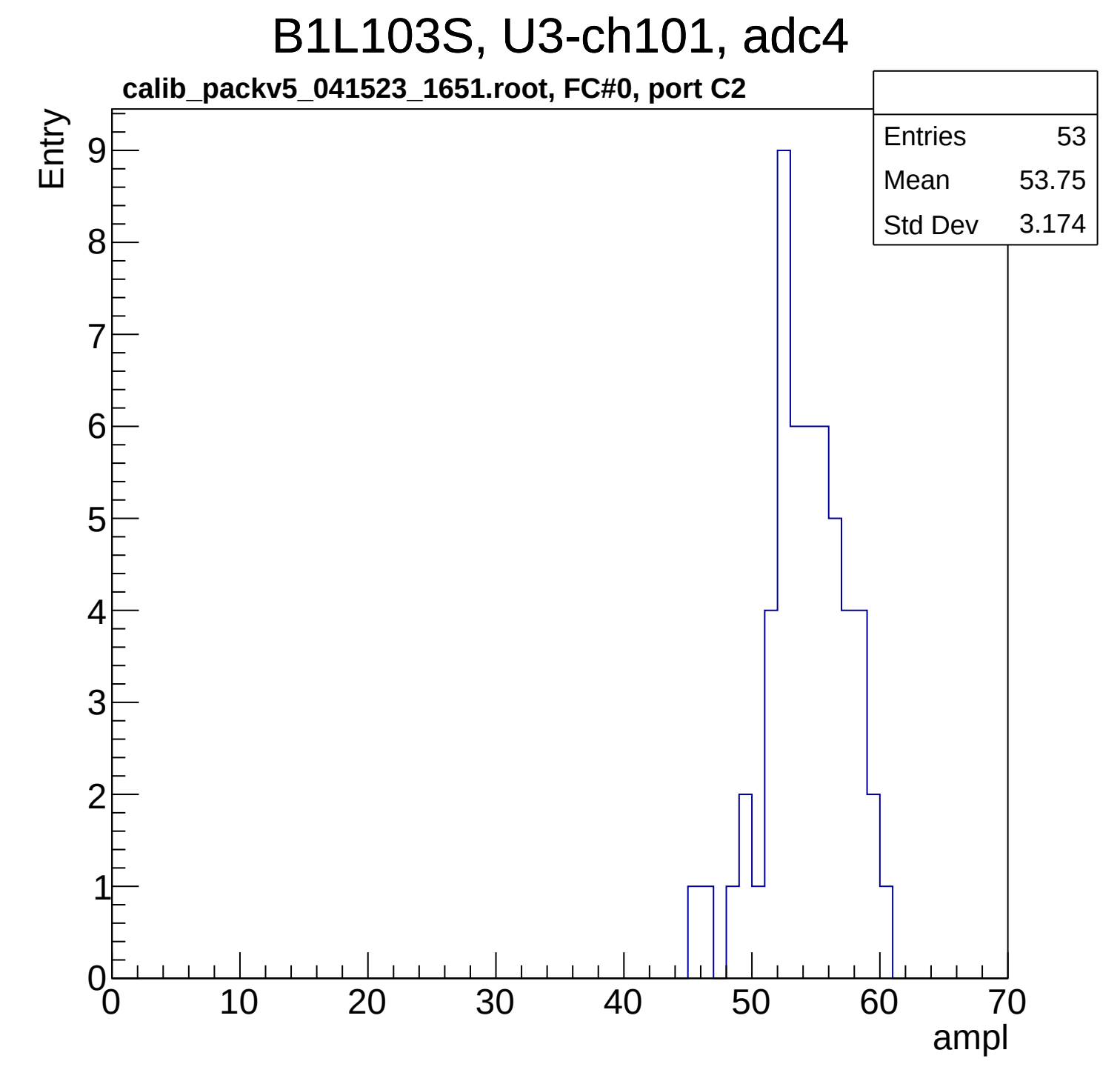
B1L103S, U3-ch101, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 53.75
Std Dev 3.174
Entry
ampl
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4
5
6
7
8
9
0
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40
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60
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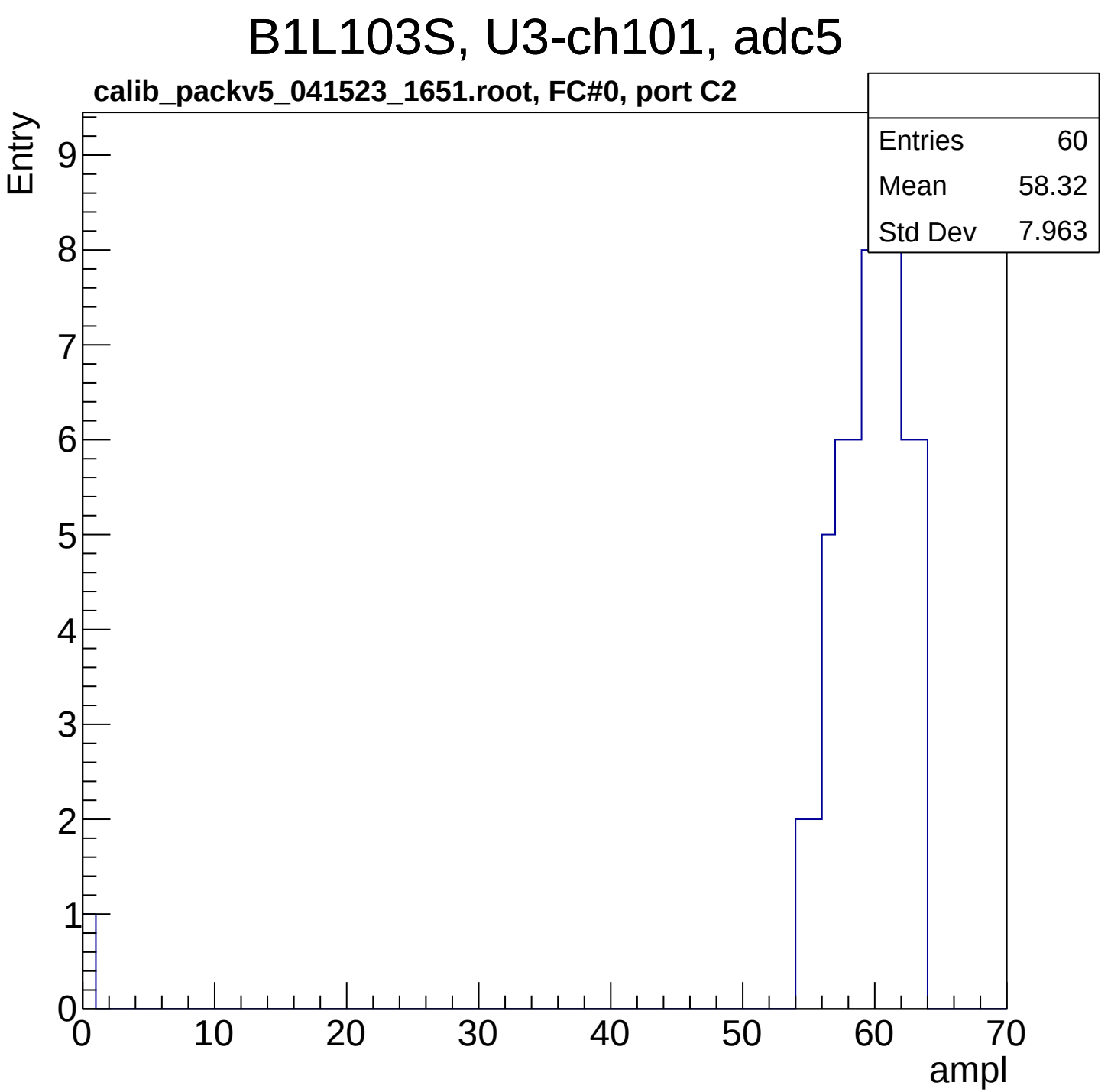
B1L103S, U3-ch101, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 58.32
Std Dev 7.963
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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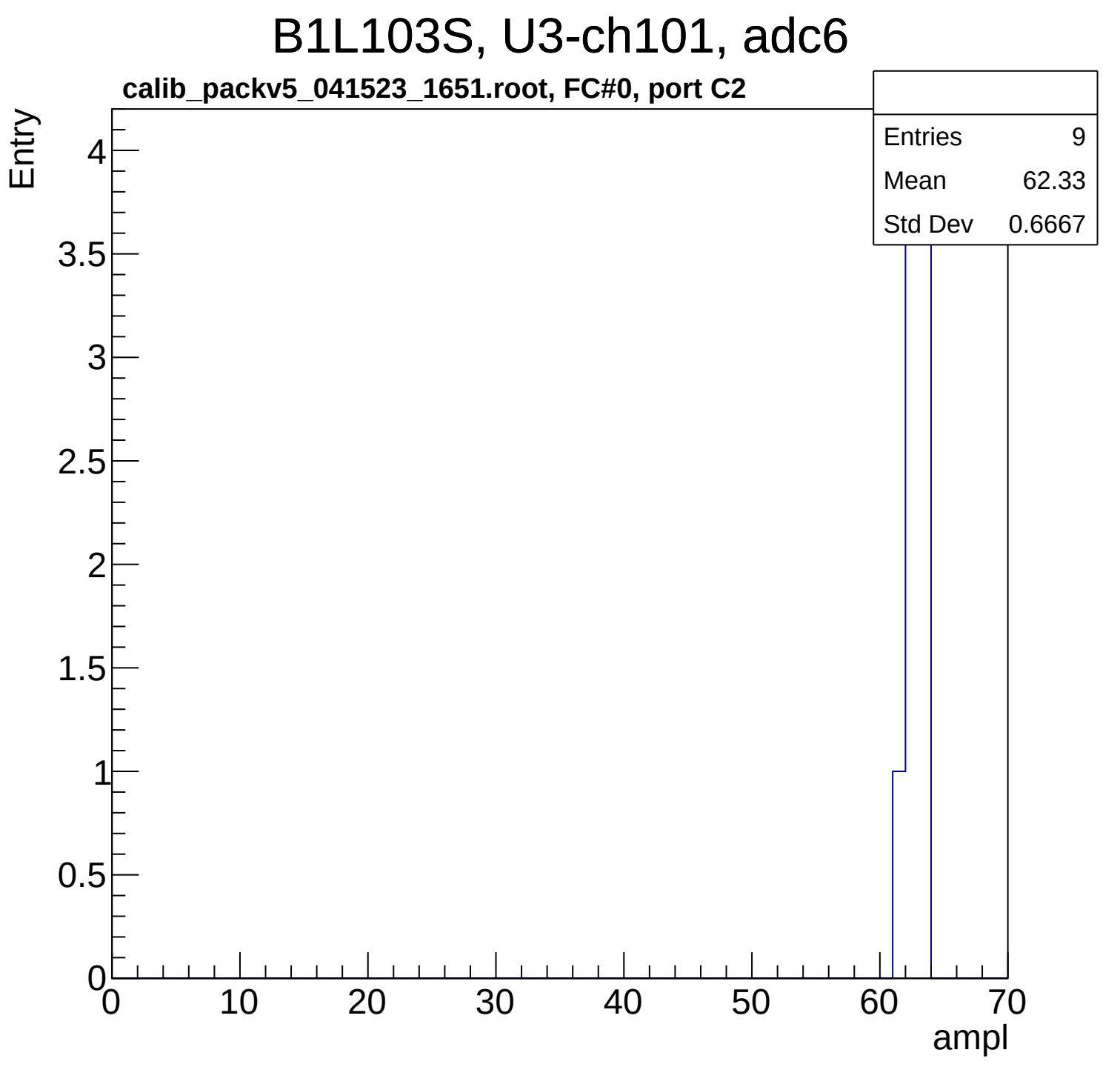
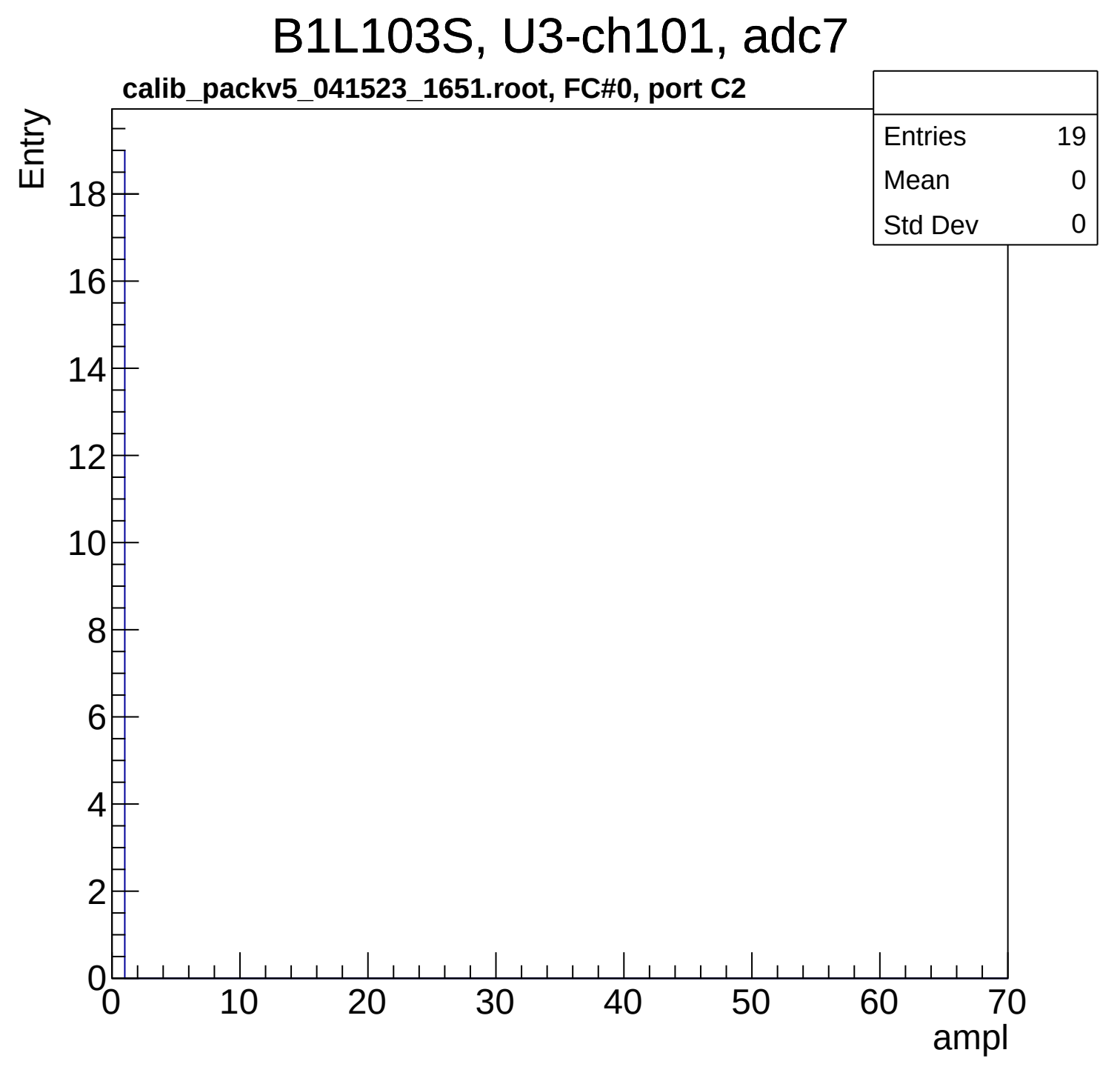
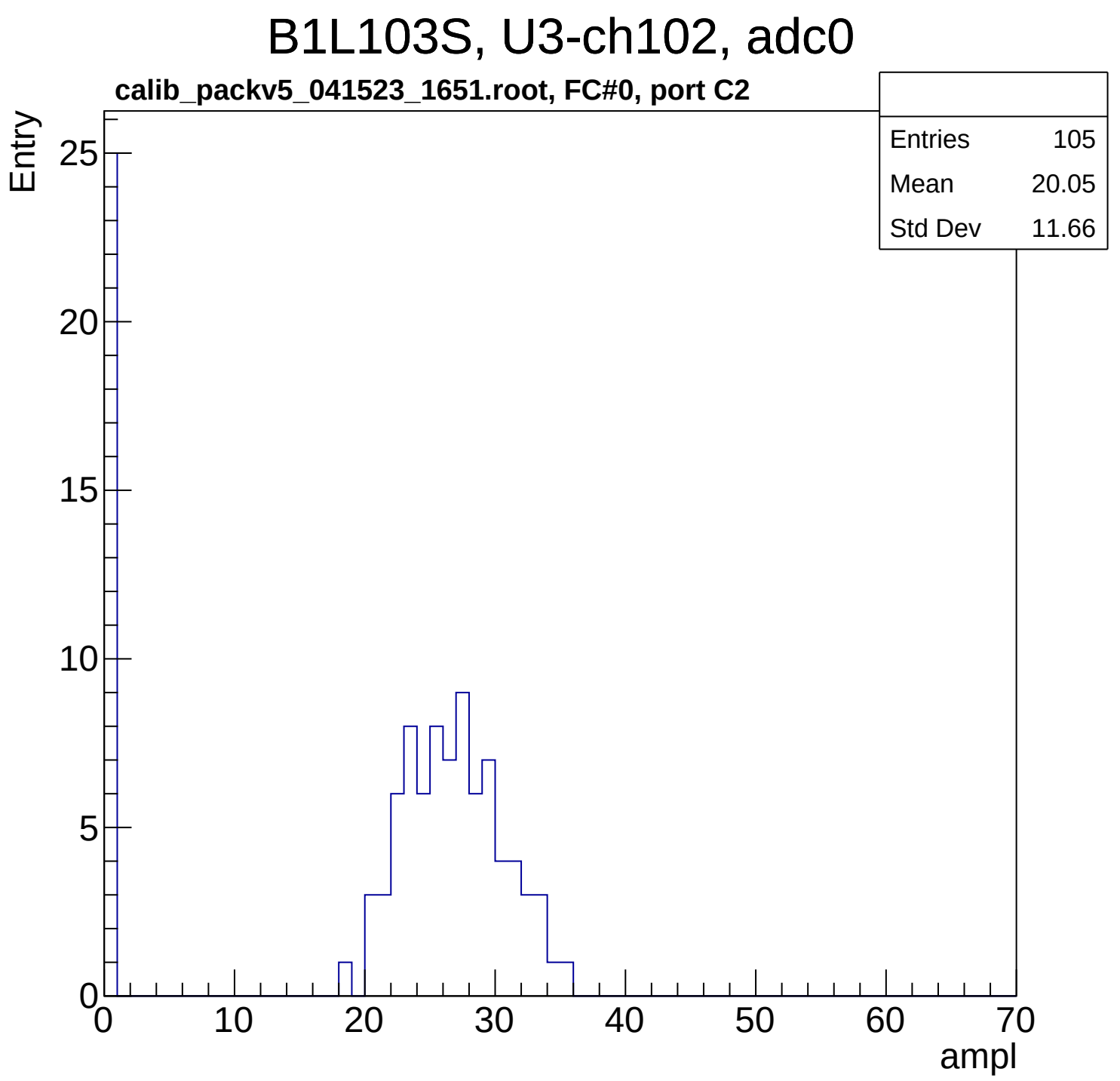
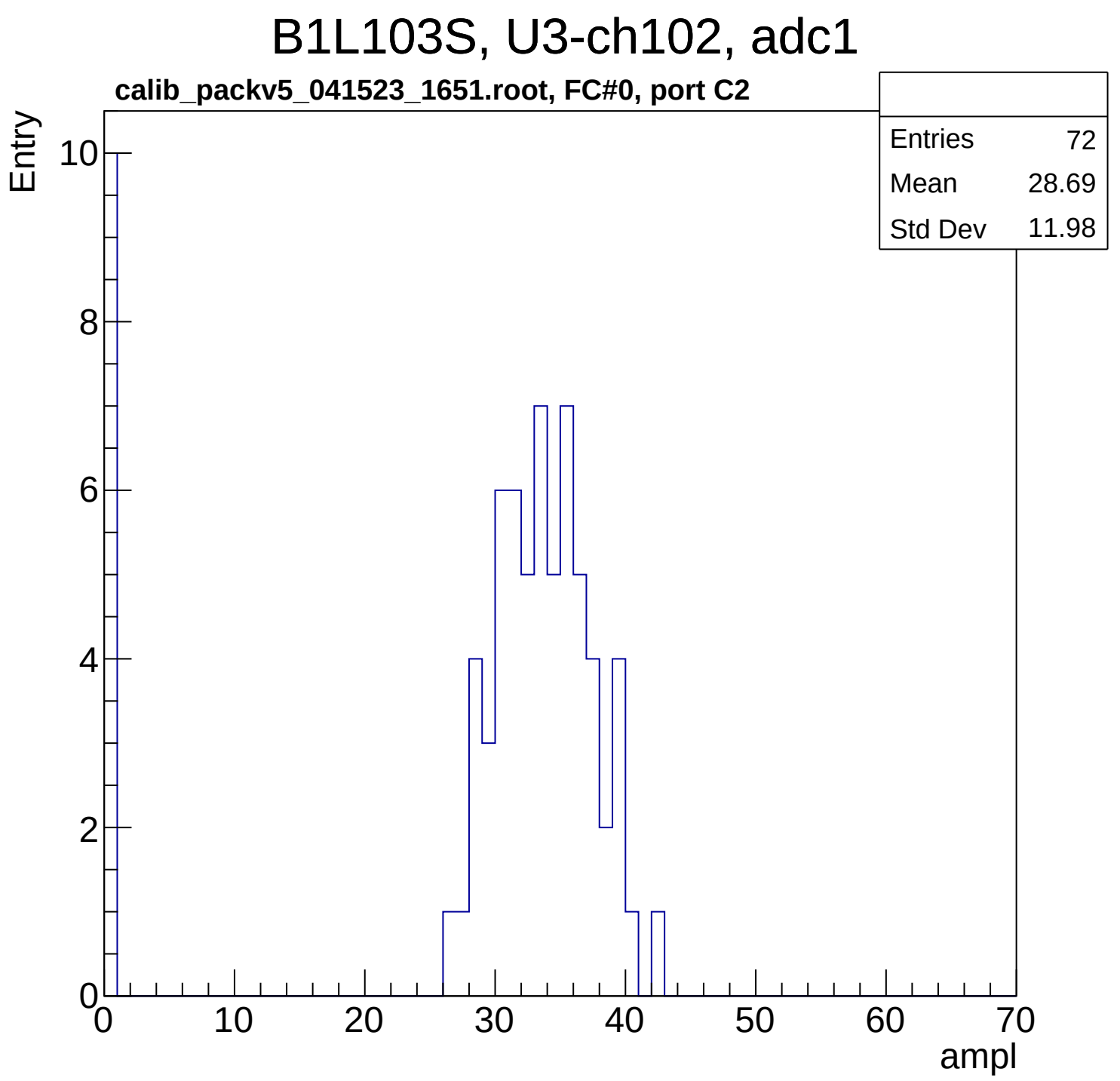
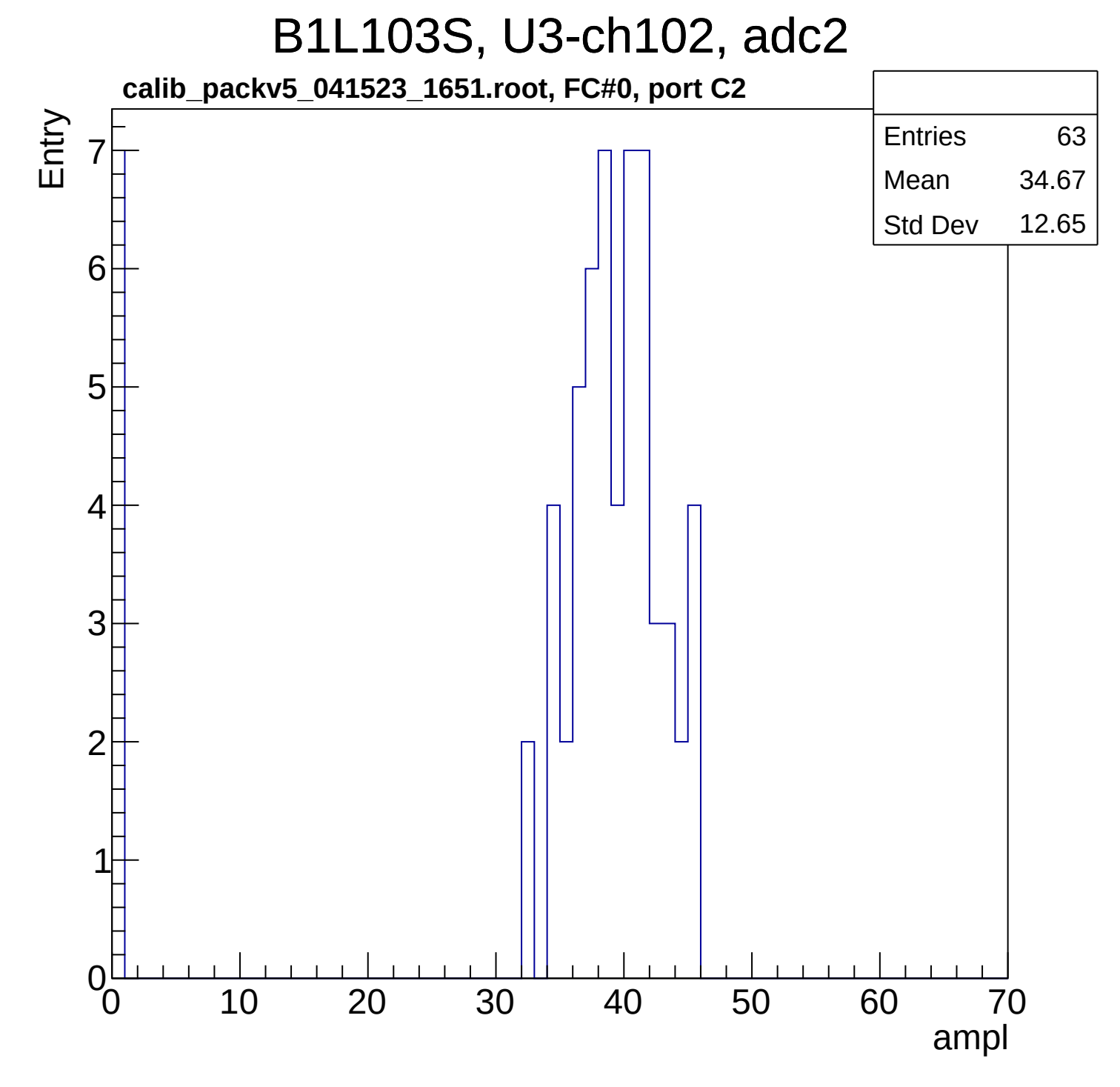
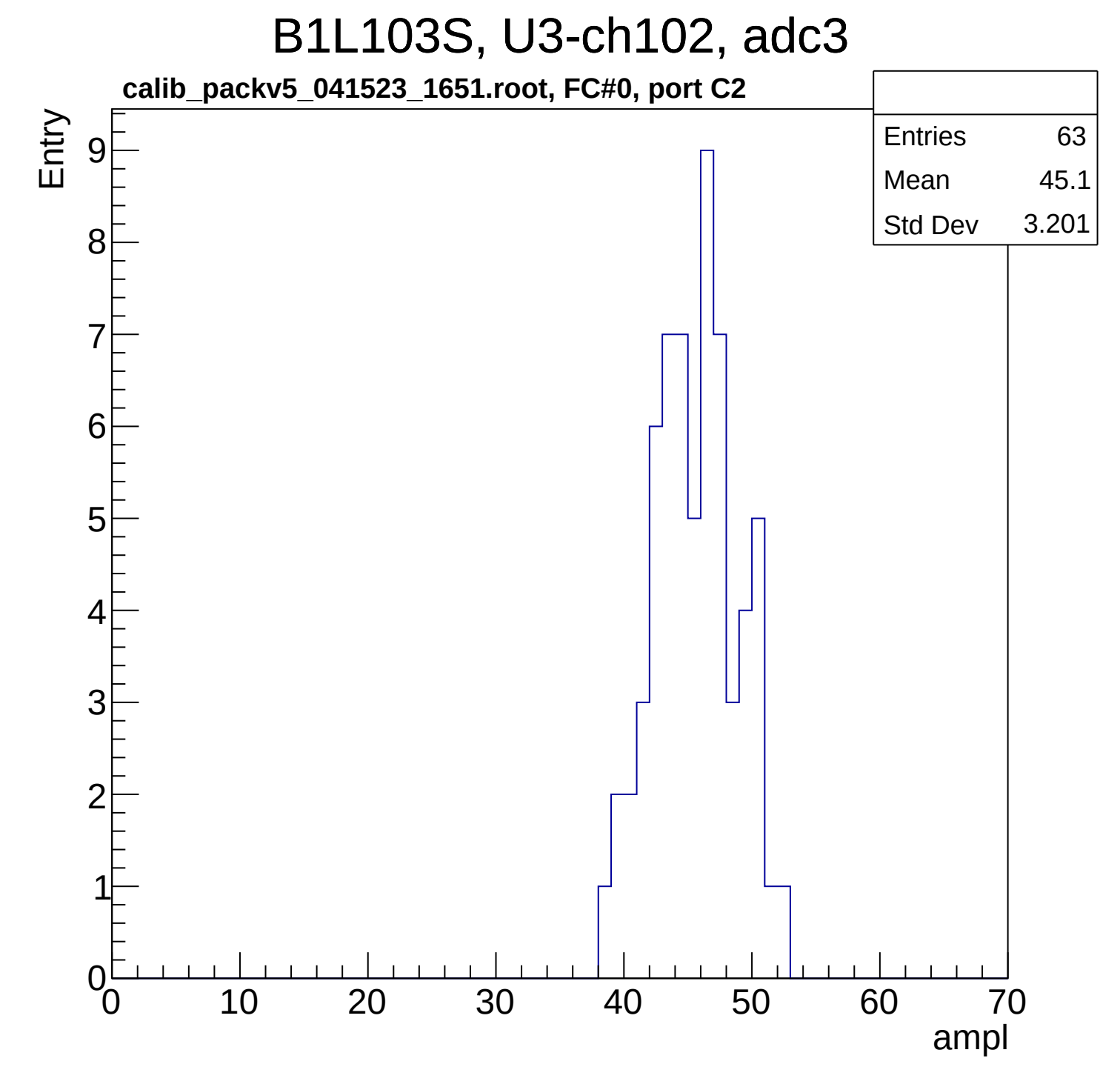

B1L103S, U3-ch101, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 62.33
Std Dev 0.6667
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

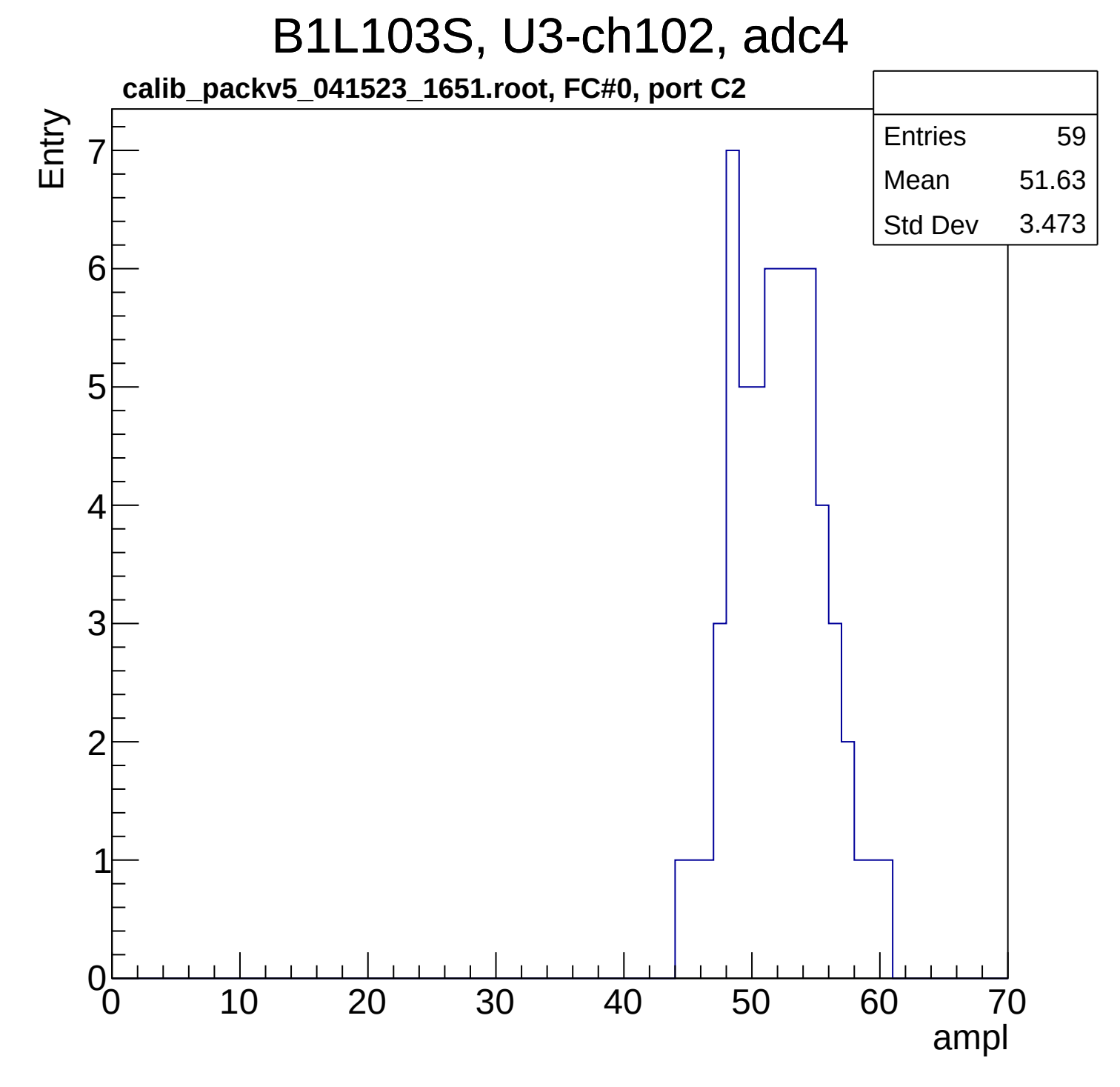

B1L103S, U3-ch101, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

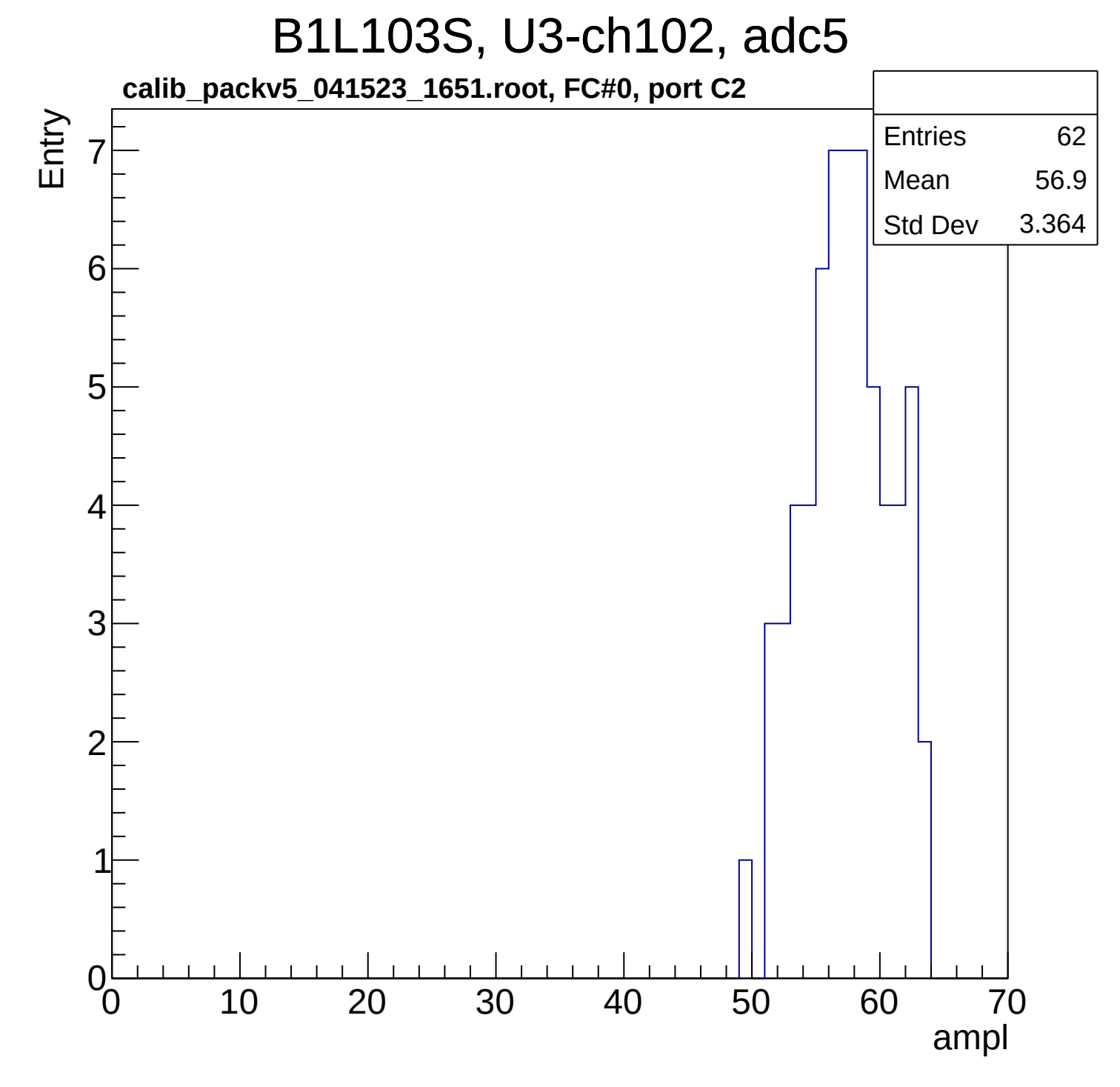

B1L103S, U3-ch102, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 105
Mean 20.05
Std Dev 11.66
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl

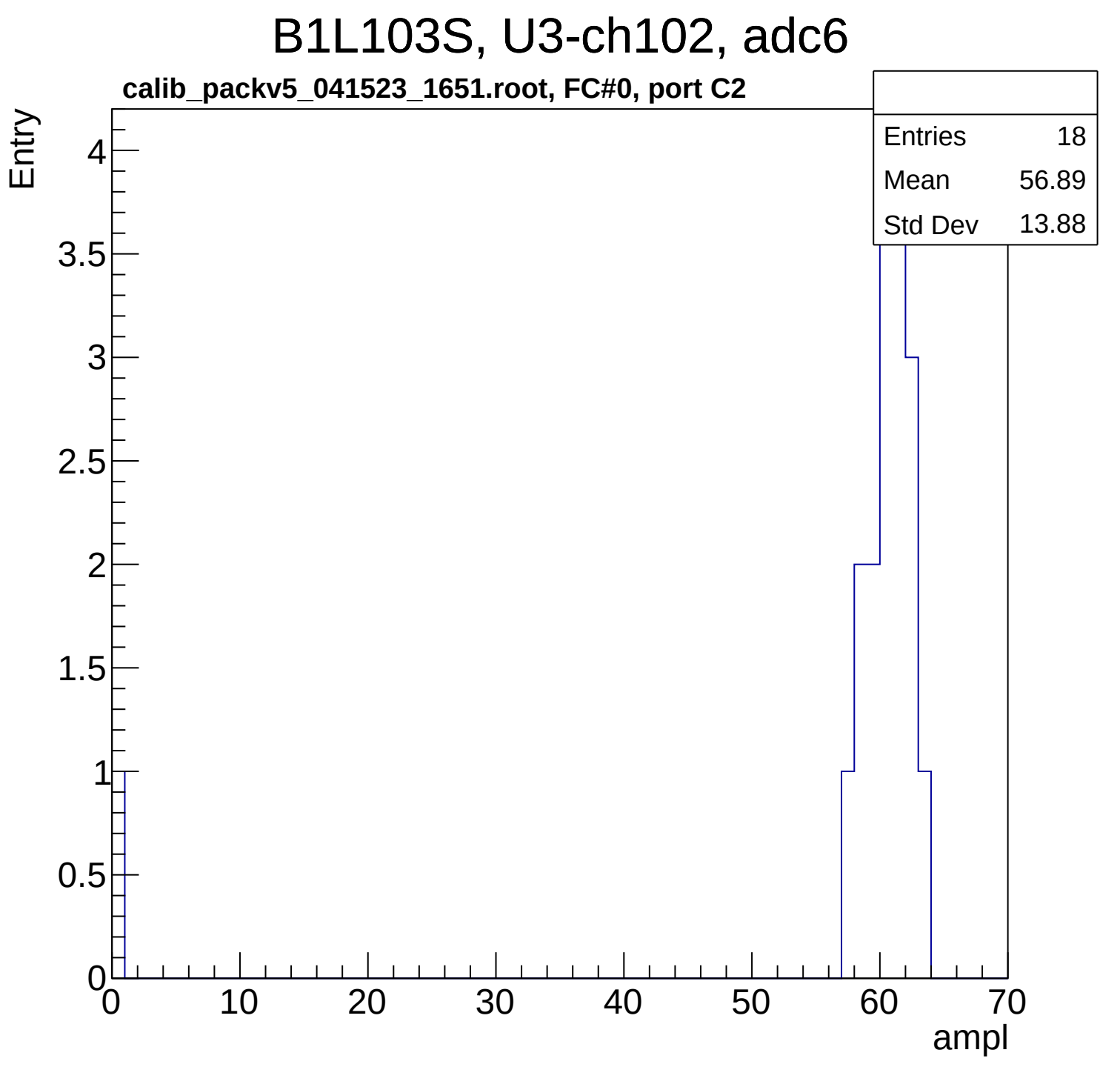

B1L103S, U3-ch102, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 28.69
Std Dev 11.98
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch102, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 34.67
Std Dev 12.65
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch102, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 45.1
Std Dev 3.201
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch102, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 51.63
Std Dev 3.473
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch102, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 56.9
Std Dev 3.364
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch102, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 56.89
Std Dev 13.88
Entry
ampl
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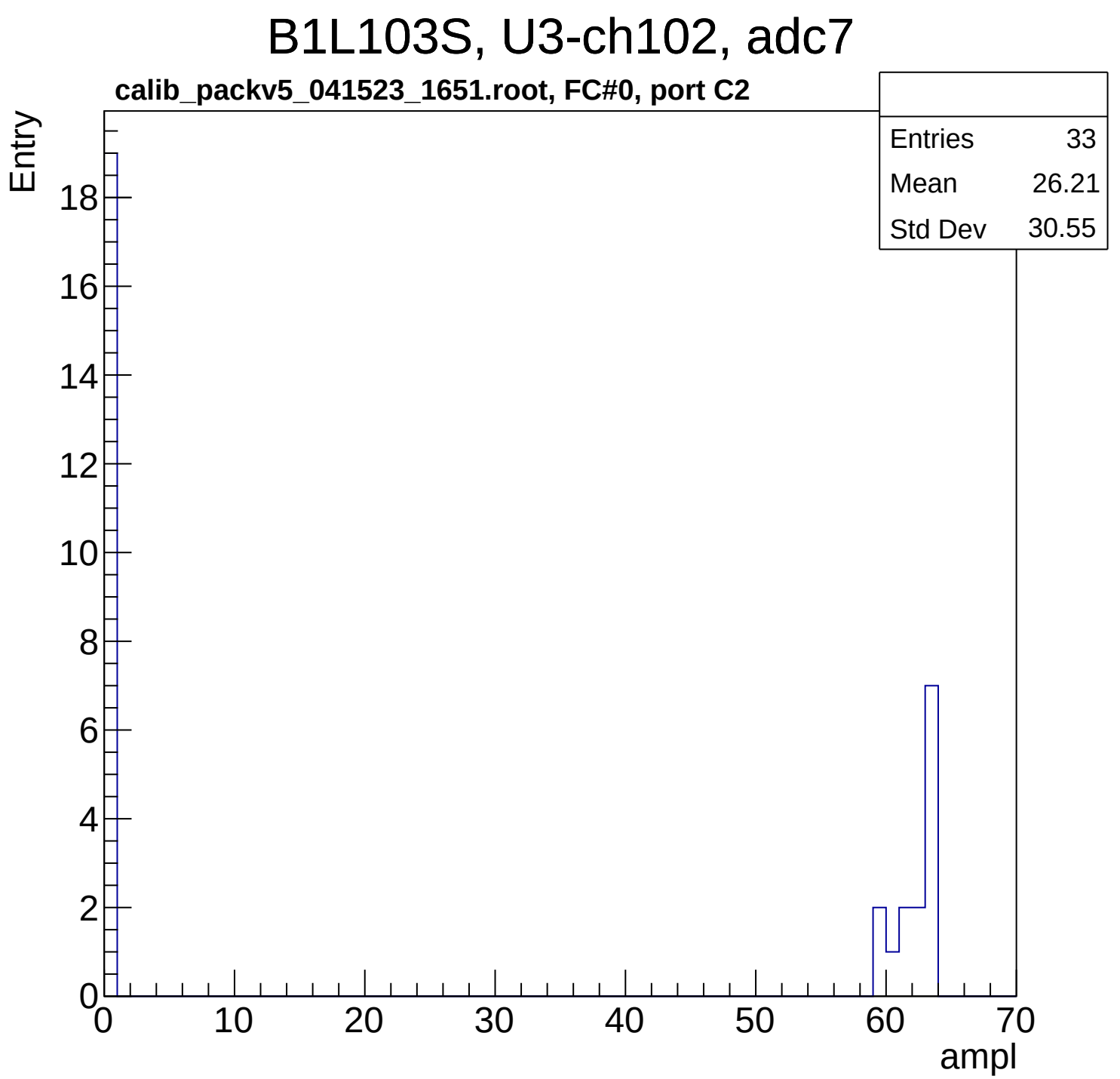
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U3-ch102, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 26.21
Std Dev 30.55
Entry
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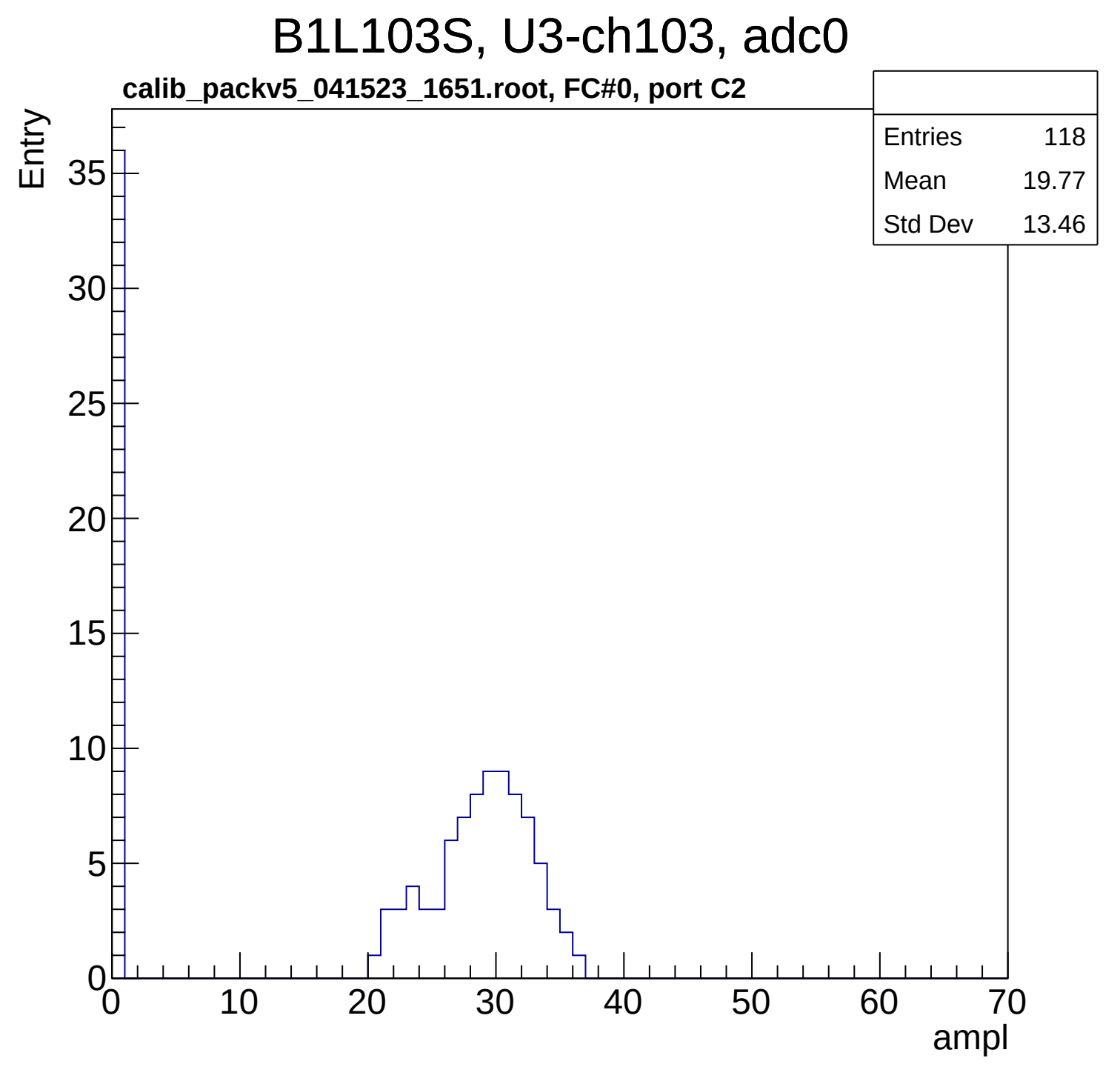
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch103, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 118
Mean 19.77
Std Dev 13.46
Entry
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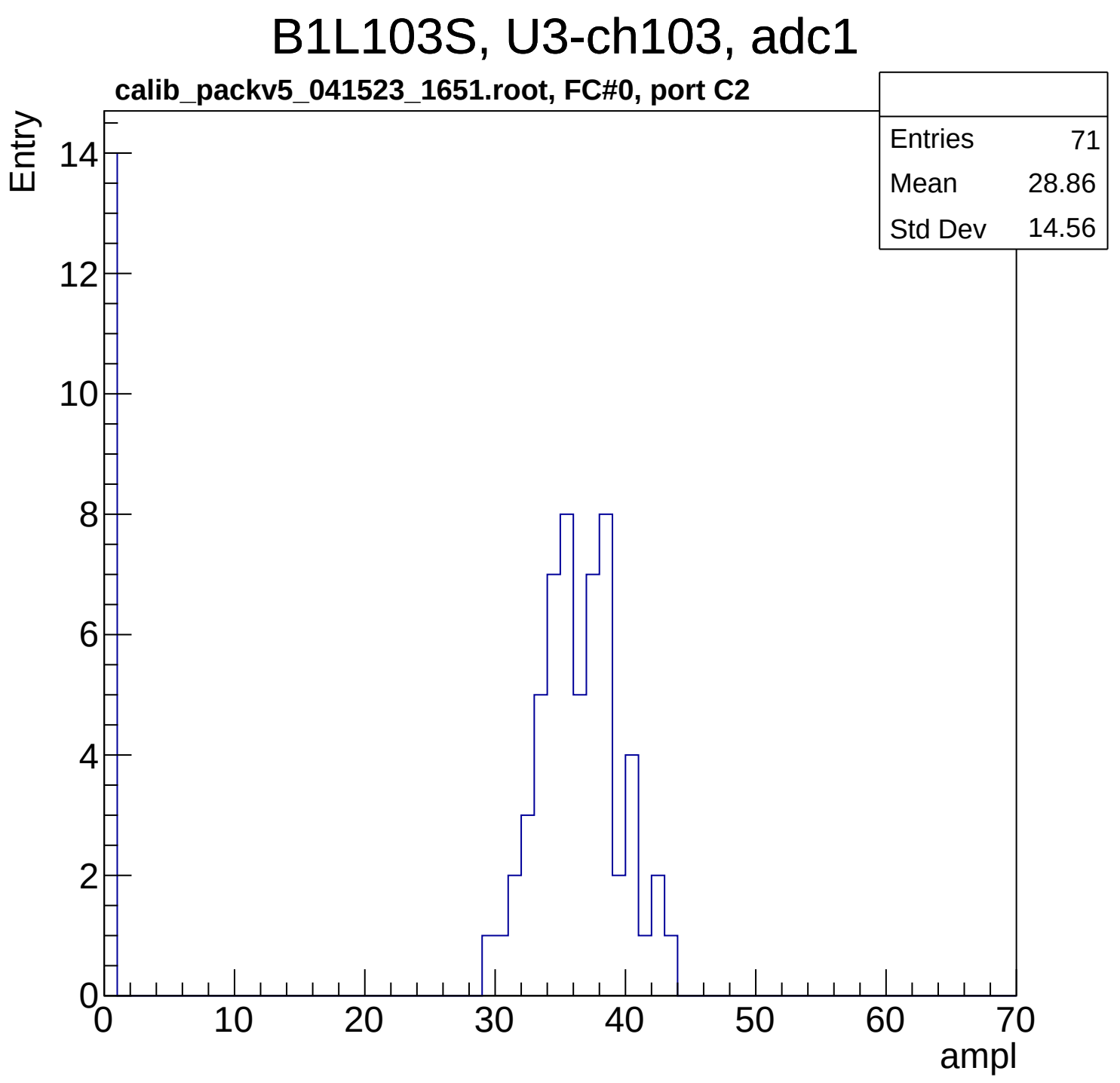
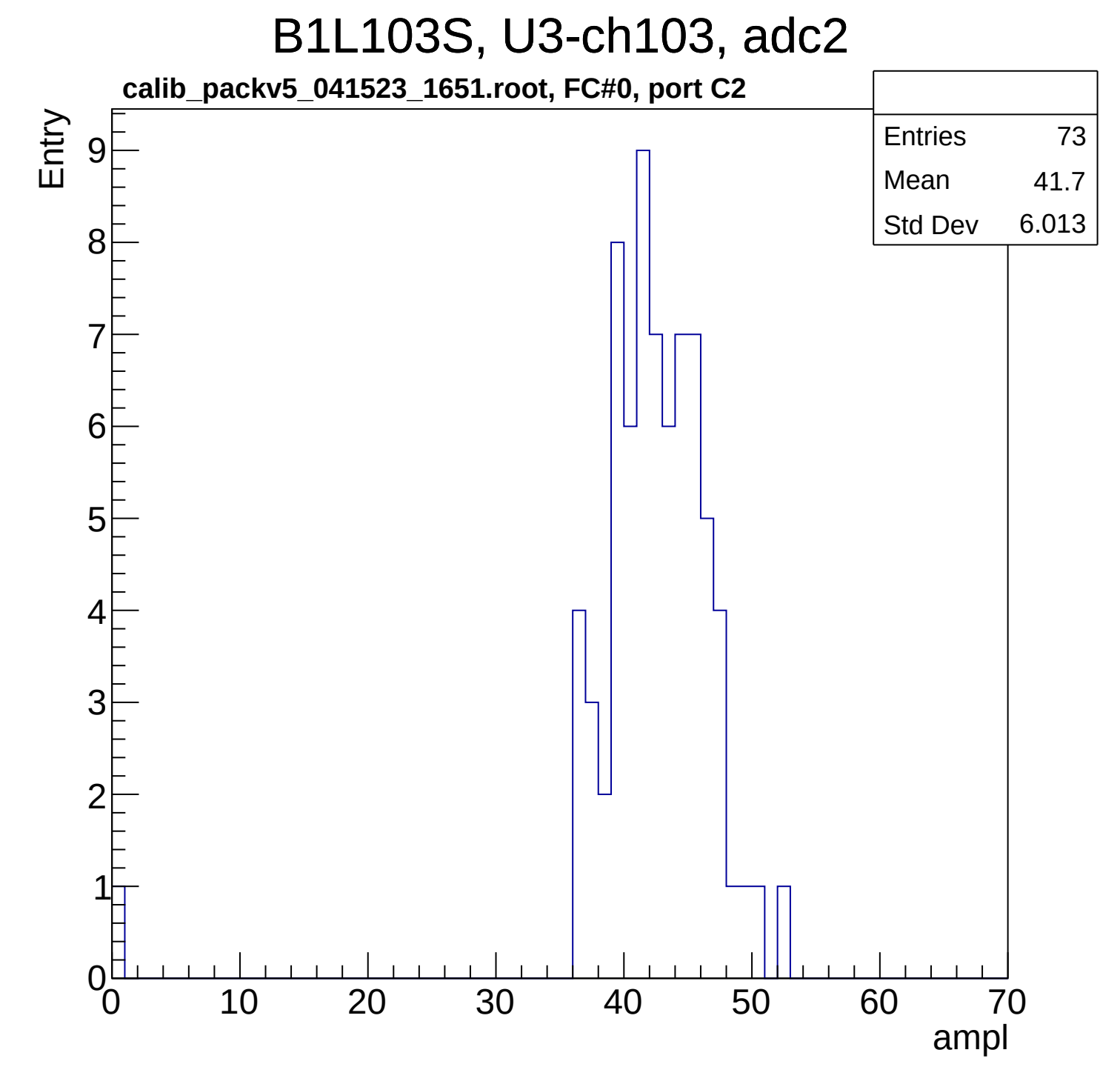
5
10
15
20
25
30
35
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch103, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 28.86
Std Dev 14.56
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch103, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 41.7
Std Dev 6.013
Entry
ampl
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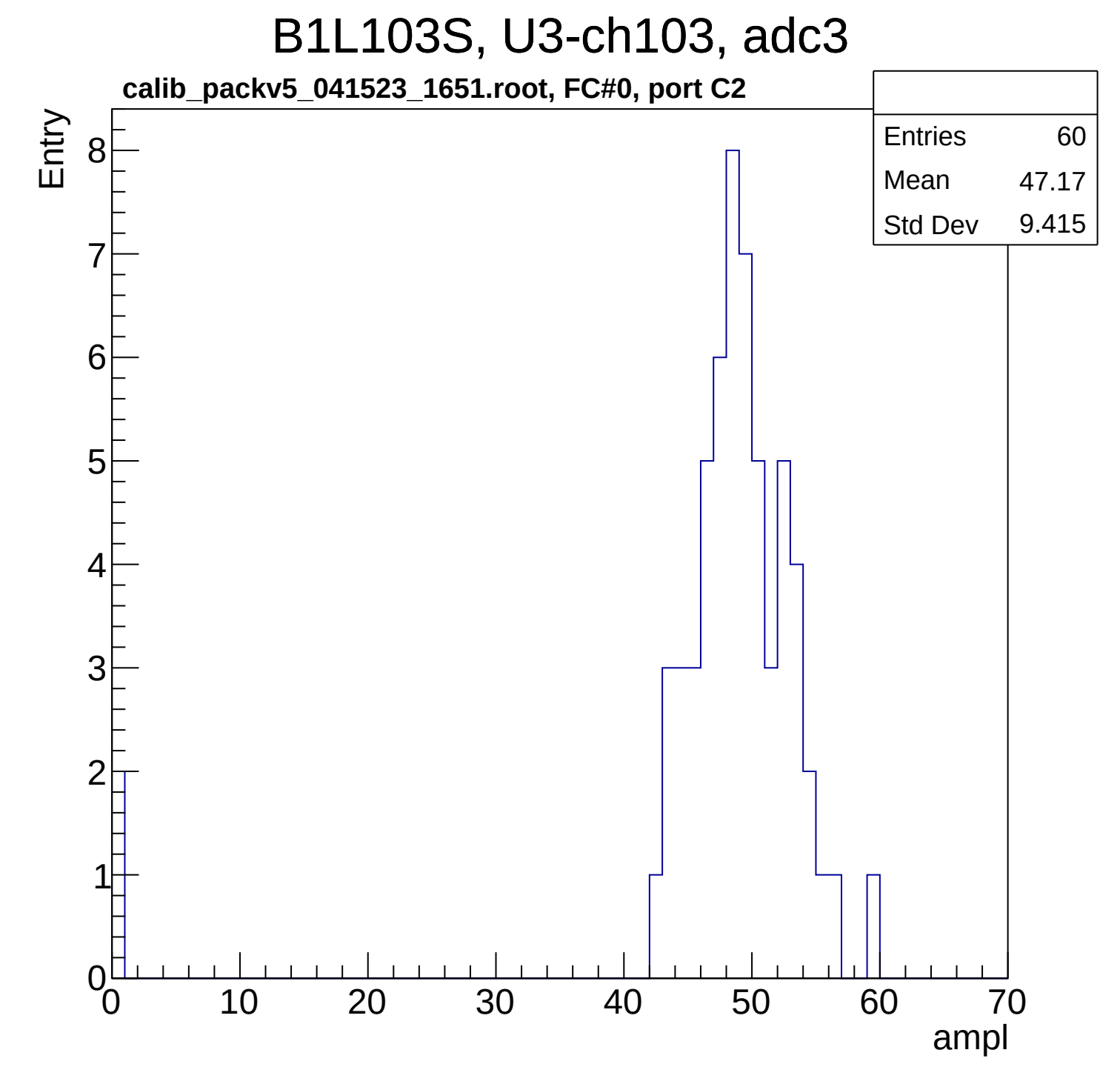
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch103, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 47.17
Std Dev 9.415
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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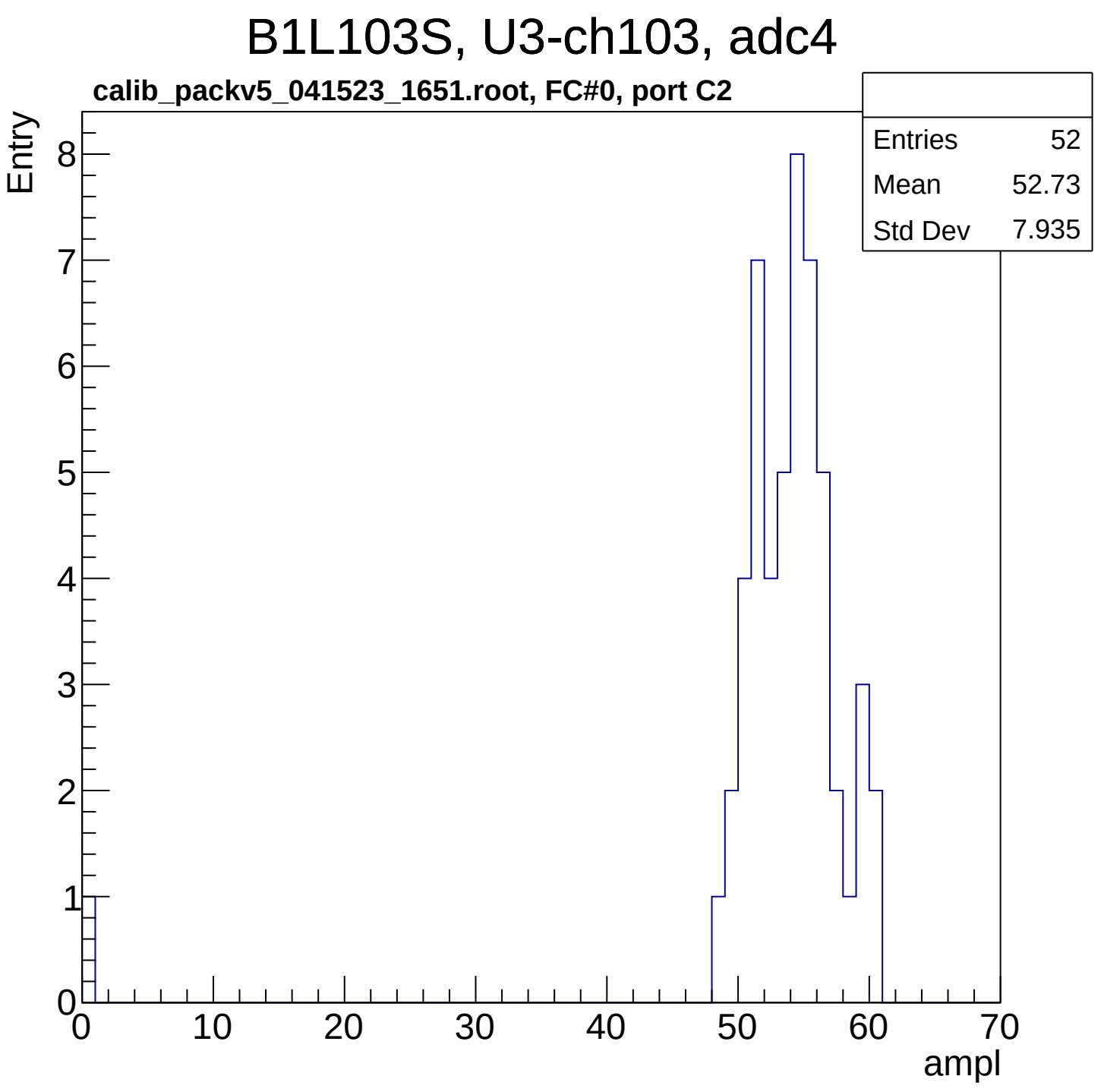
40
50
60
70


B1L103S, U3-ch103, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 52.73
Std Dev 7.935
Entry
ampl
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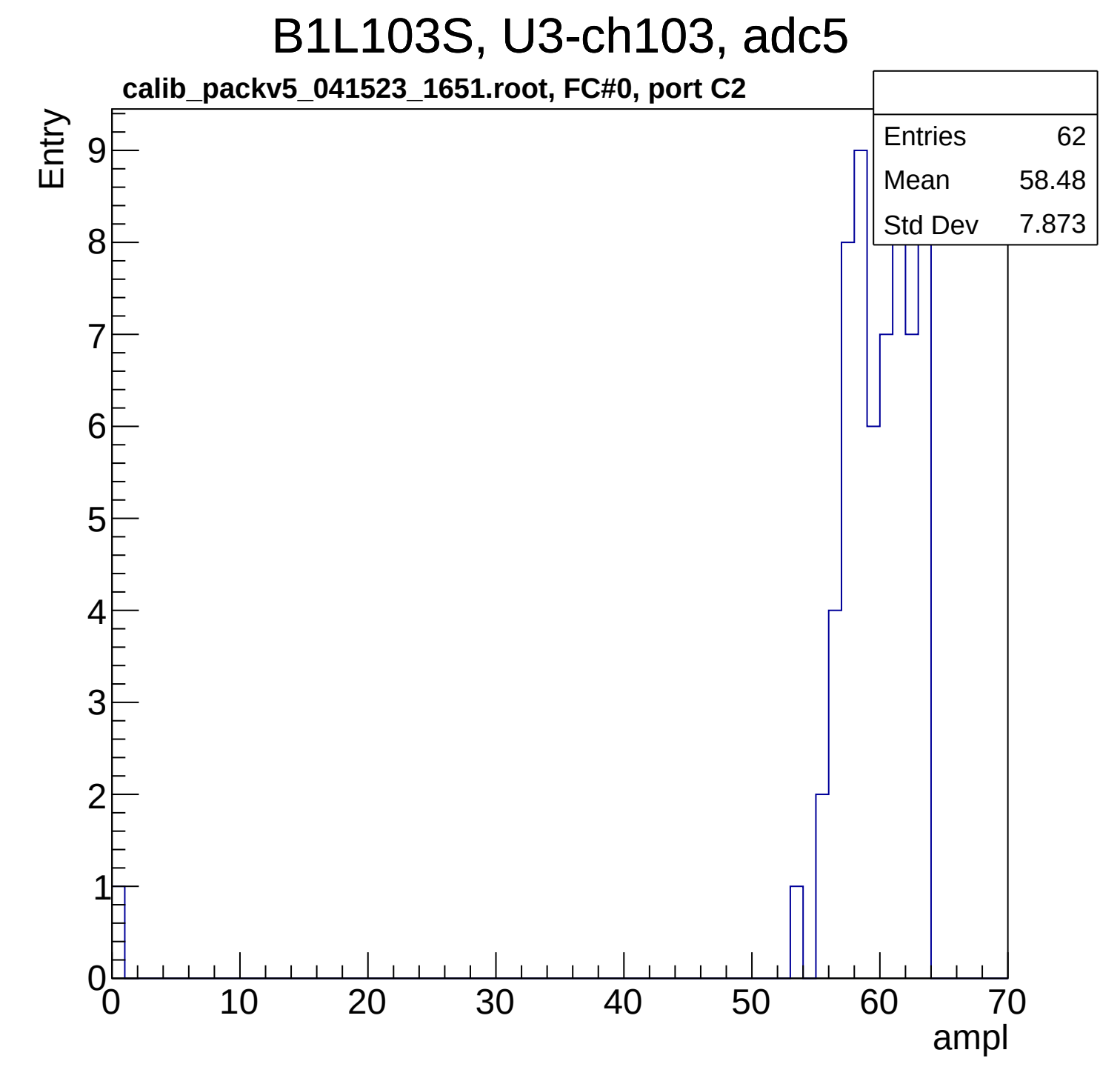
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch103, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 58.48
Std Dev 7.873
Entry
ampl
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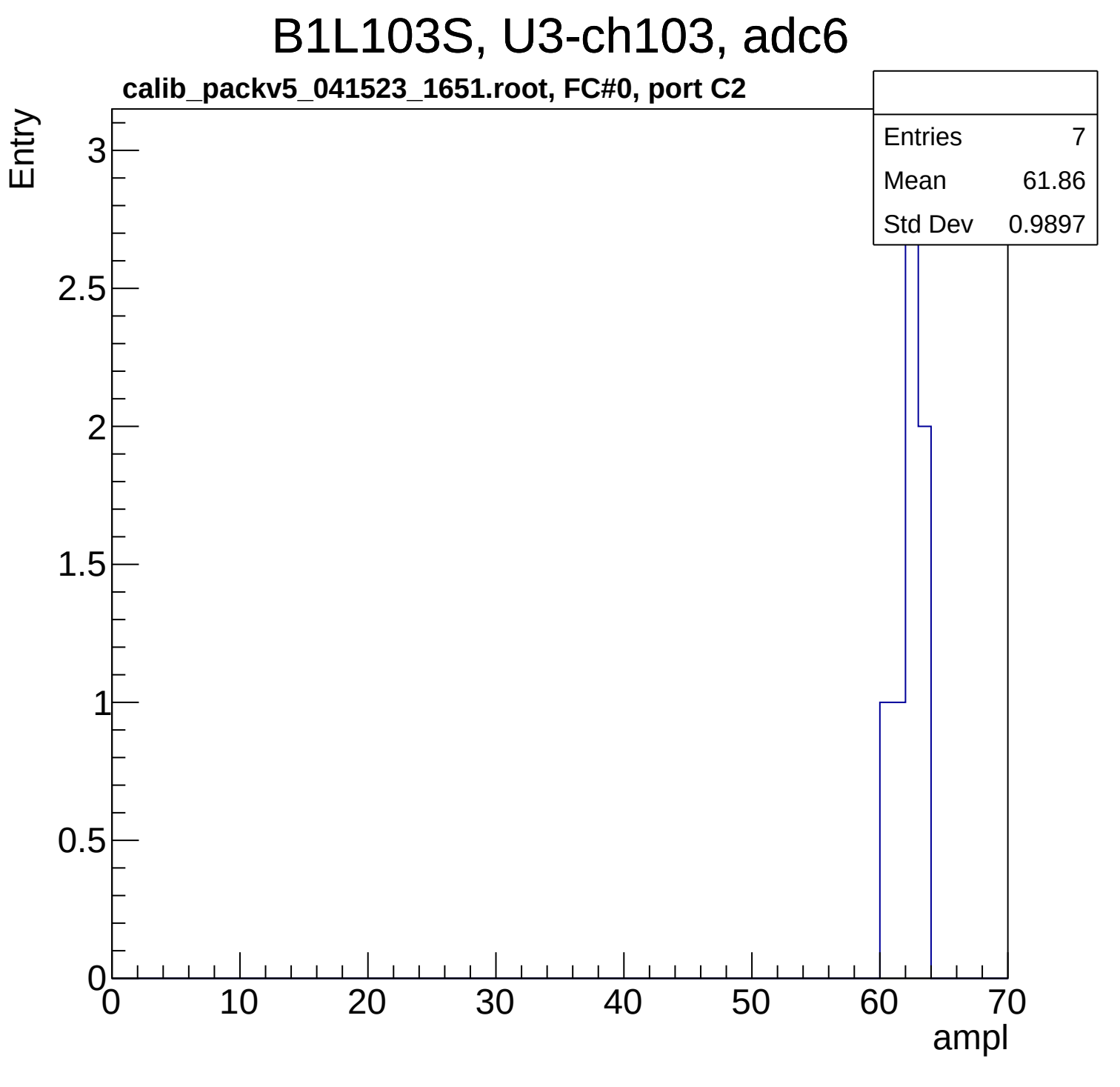
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch103, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 61.86
Std Dev 0.9897
Entry
ampl
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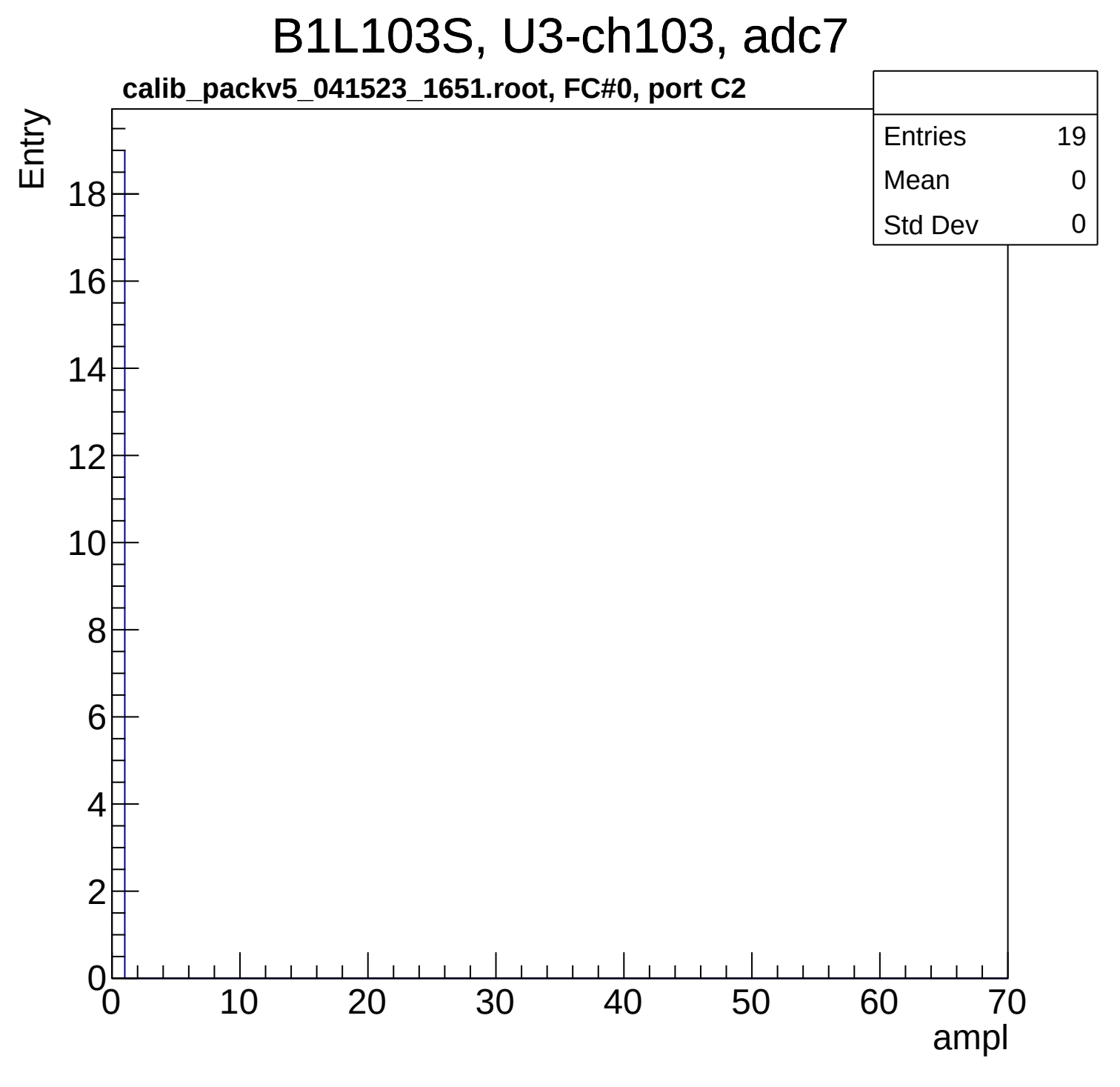
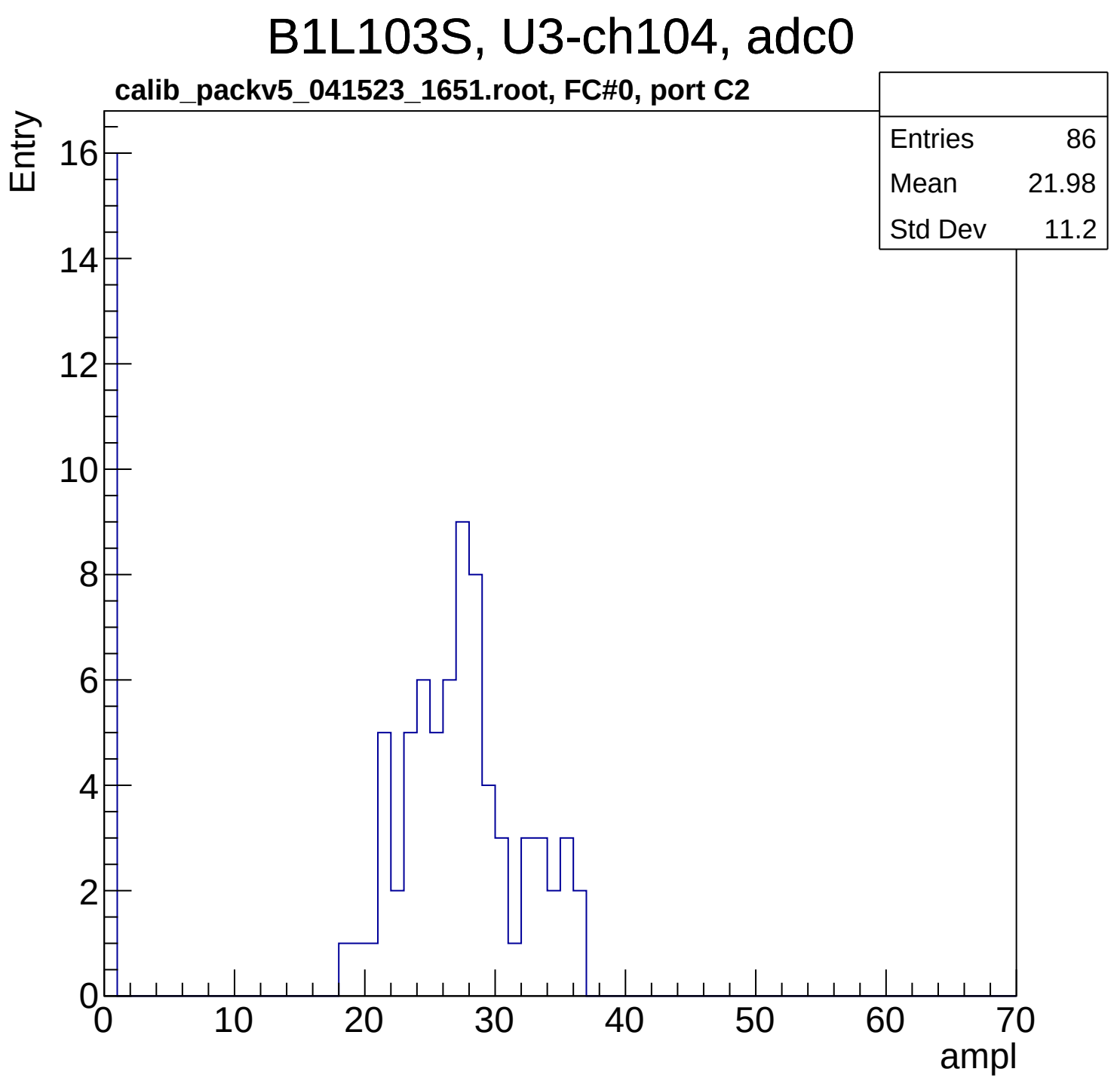
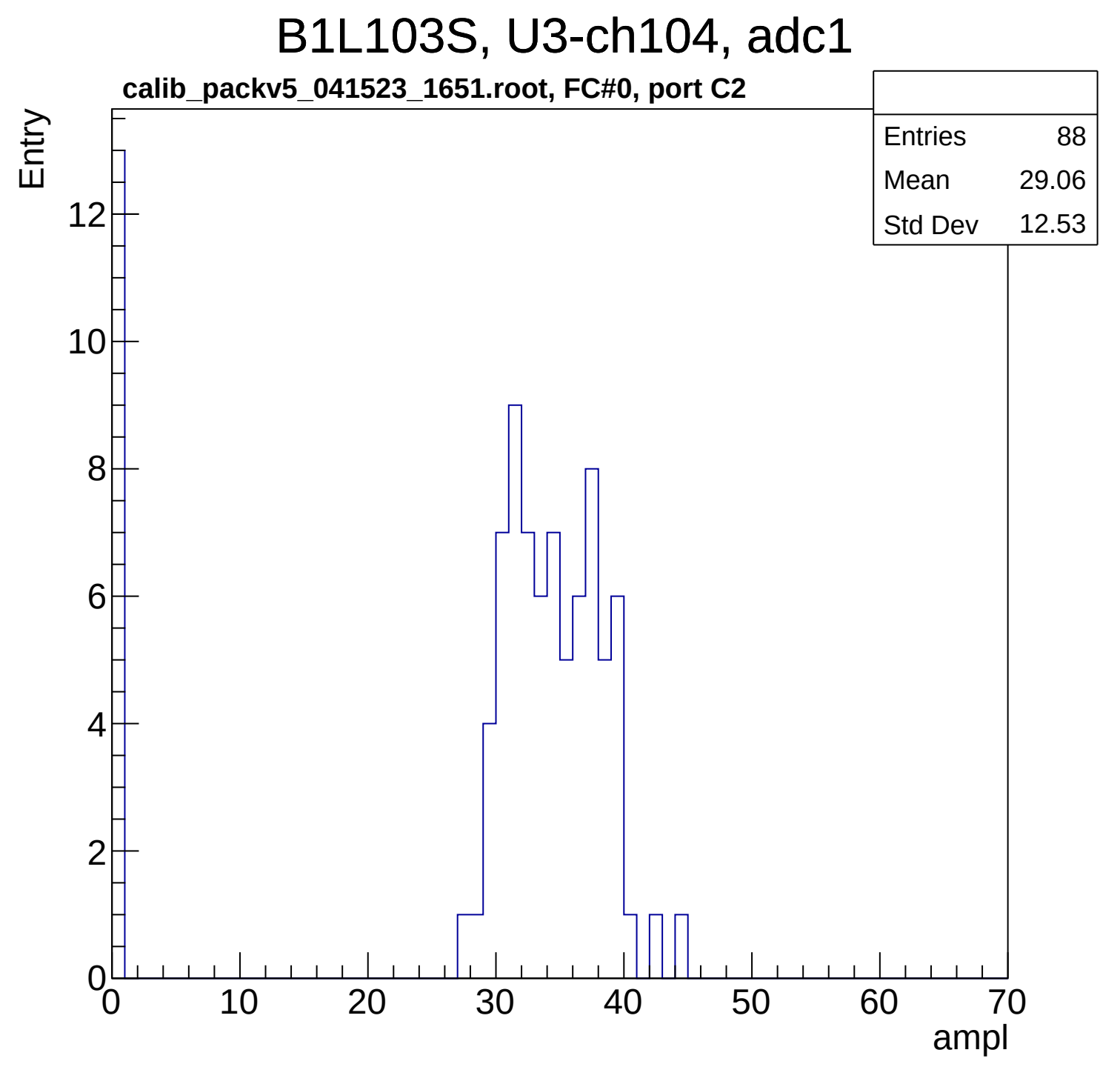
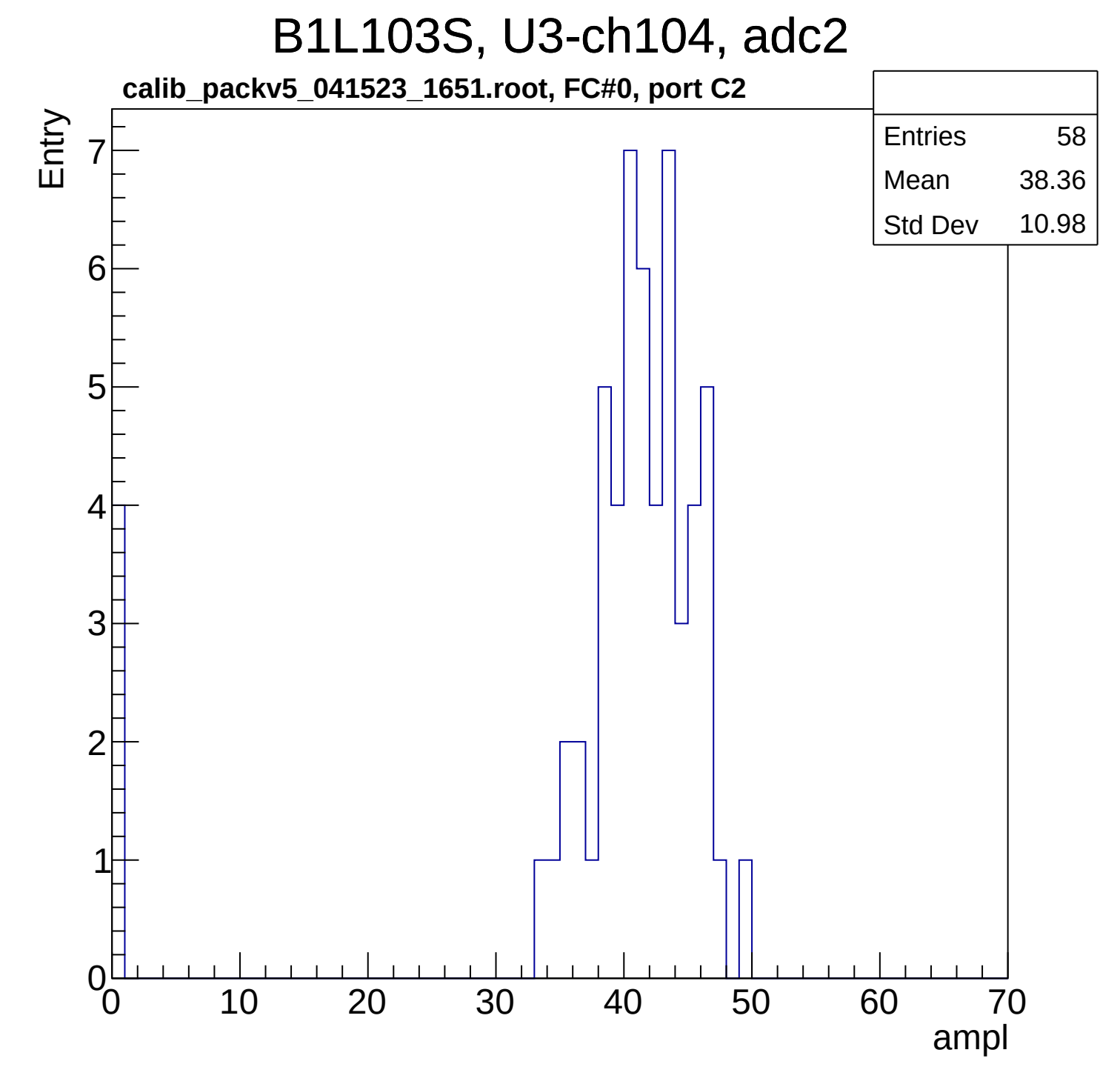
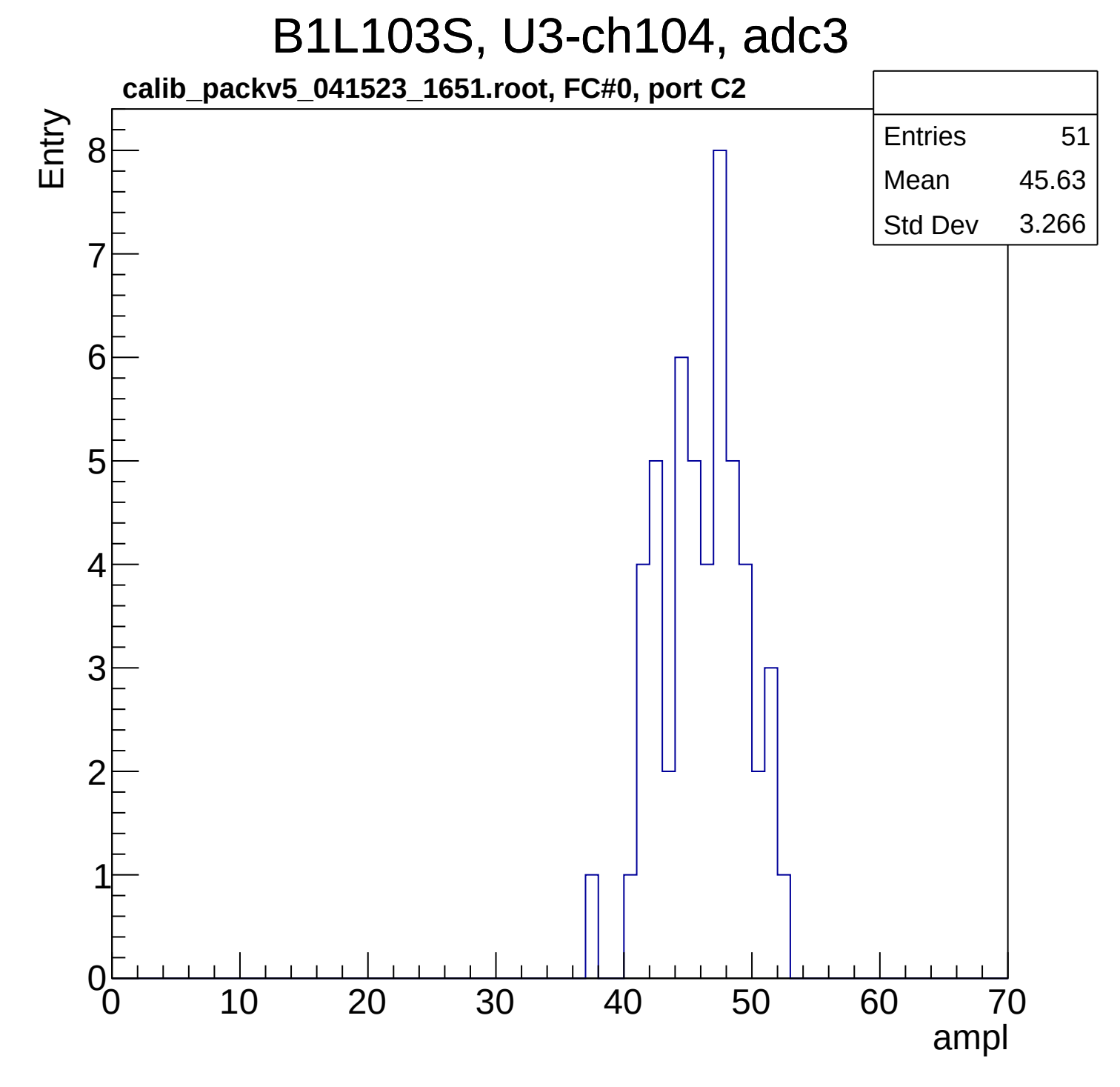
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

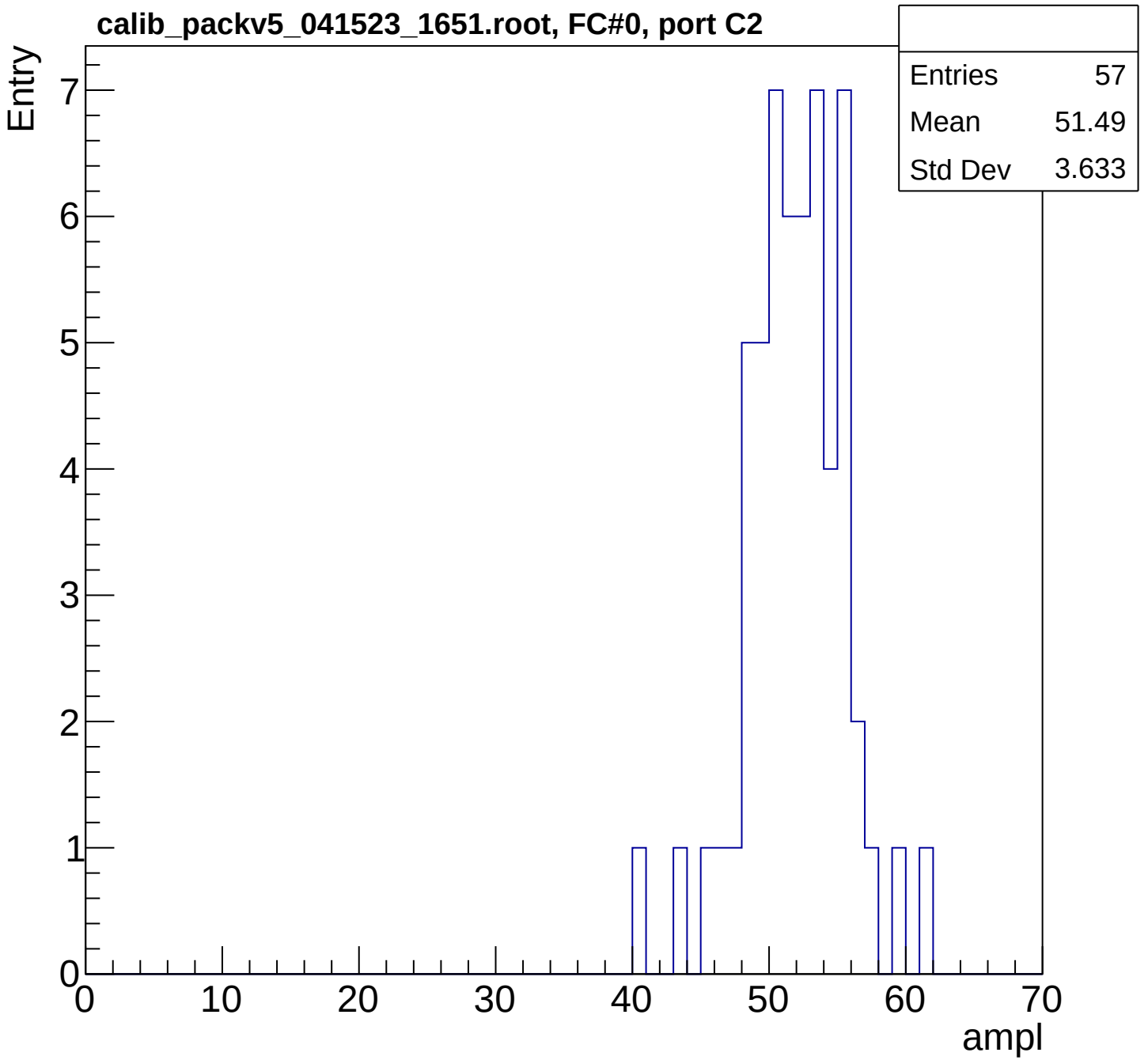

B1L103S, U3-ch103, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch104, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 21.98
Std Dev 11.2
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch104, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 29.06
Std Dev 12.53
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch104, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 38.36
Std Dev 10.98
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch104, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 45.63
Std Dev 3.266
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch104, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 51.49
Std Dev 3.633
Entry
ampl
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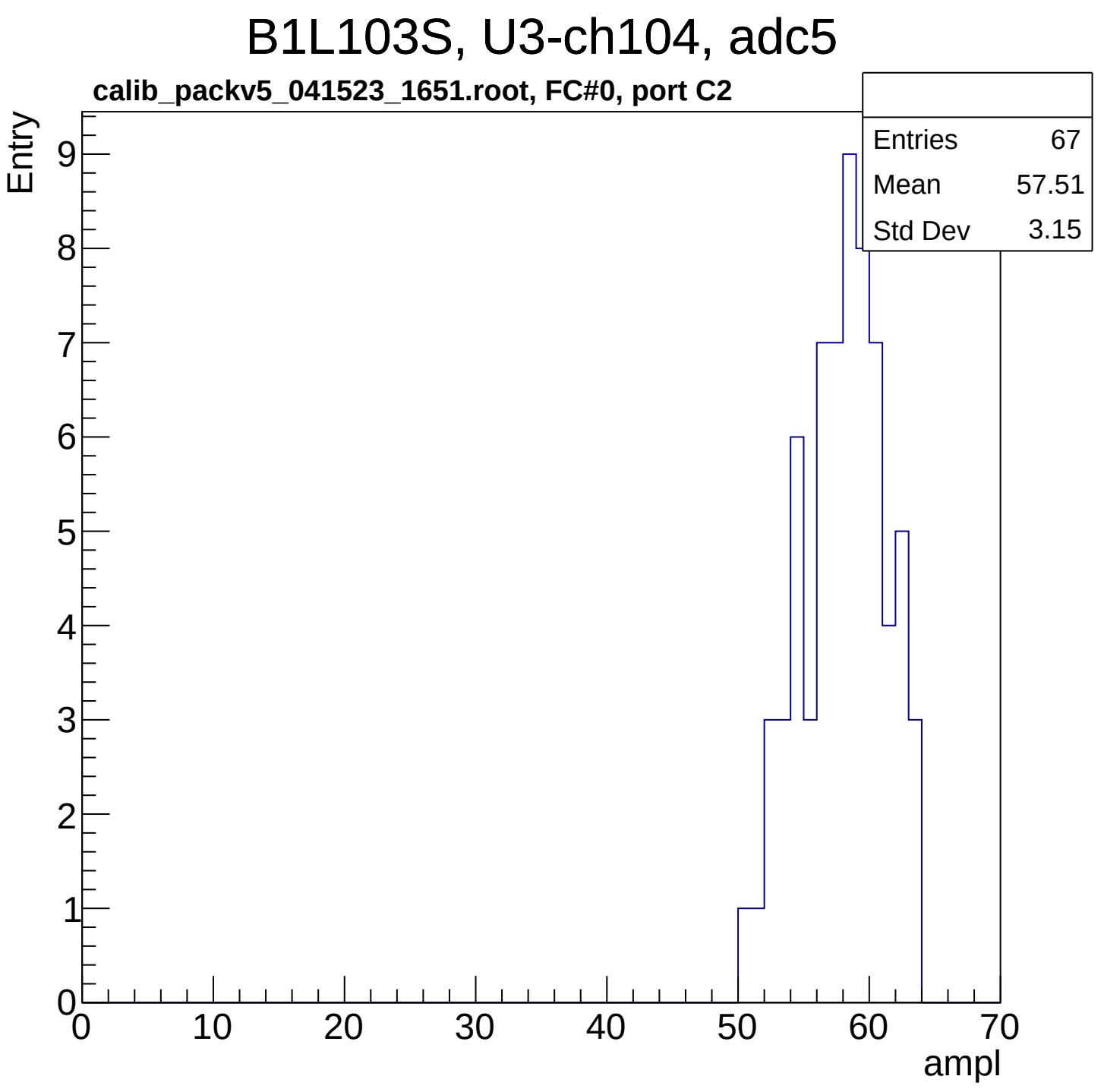
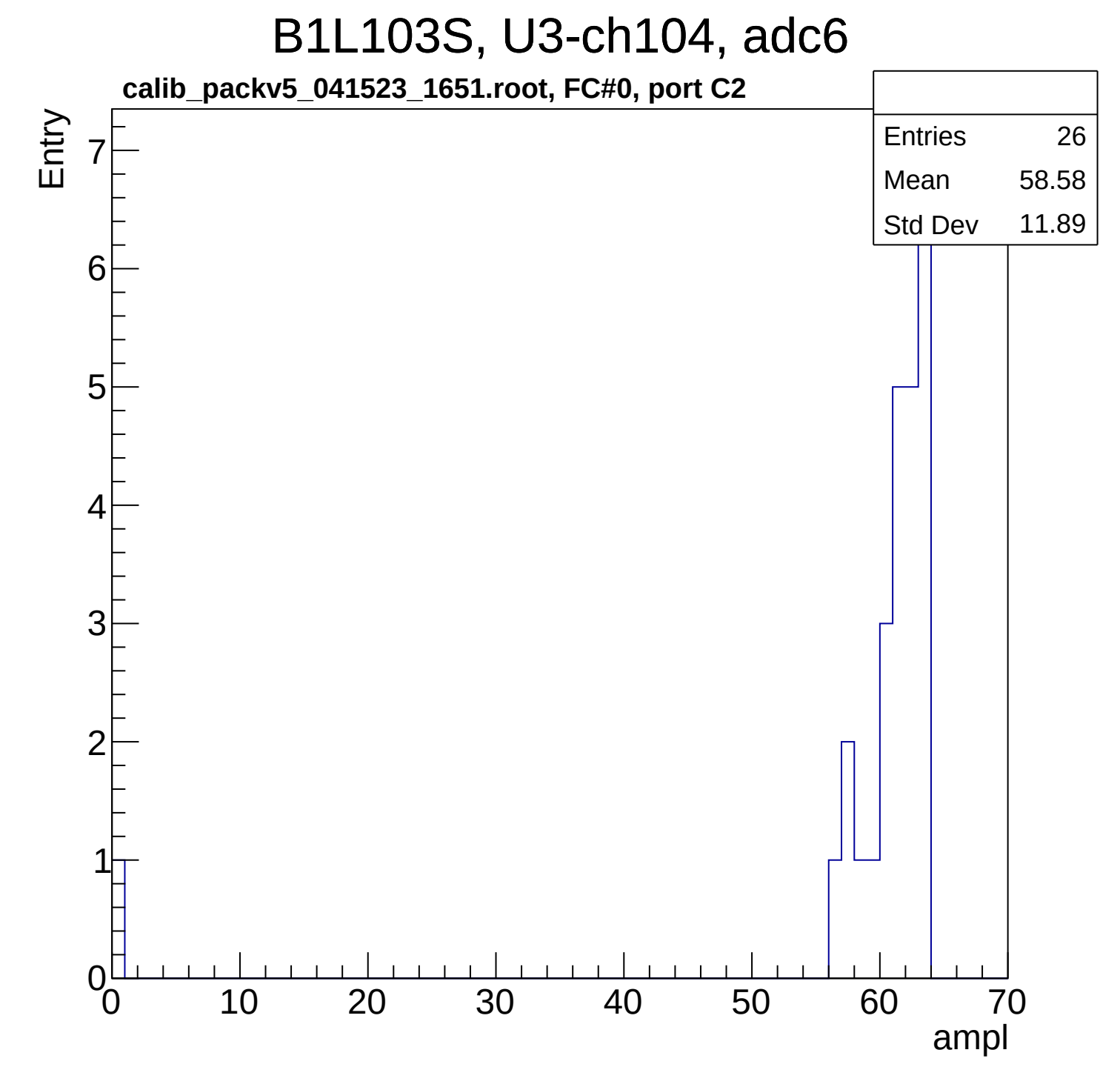
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch104, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 57.51
Std Dev 3.15
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch104, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 58.58
Std Dev 11.89
Entry
ampl
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2
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4
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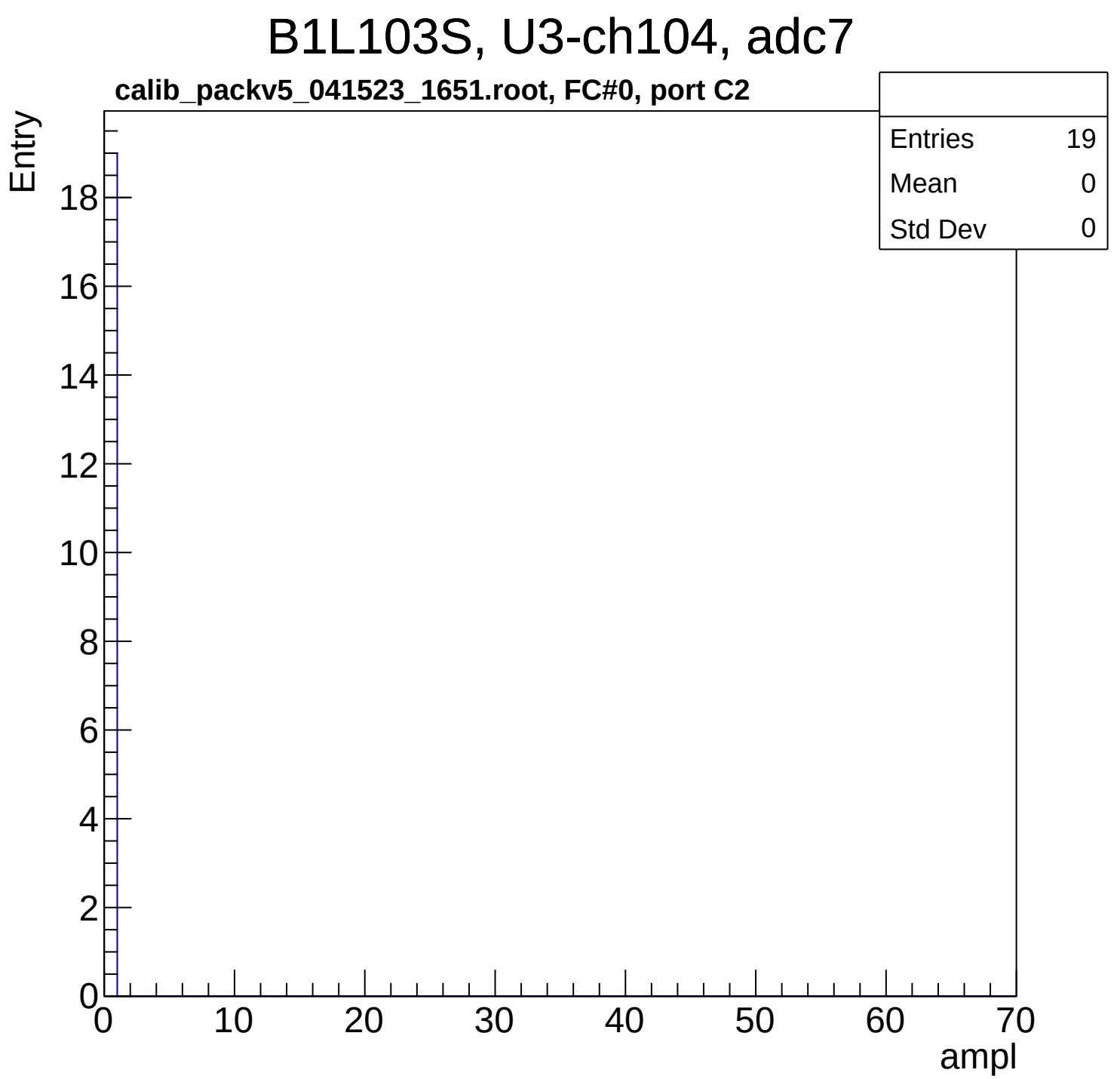
B1L103S, U3-ch104, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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6
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10
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14
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18
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50
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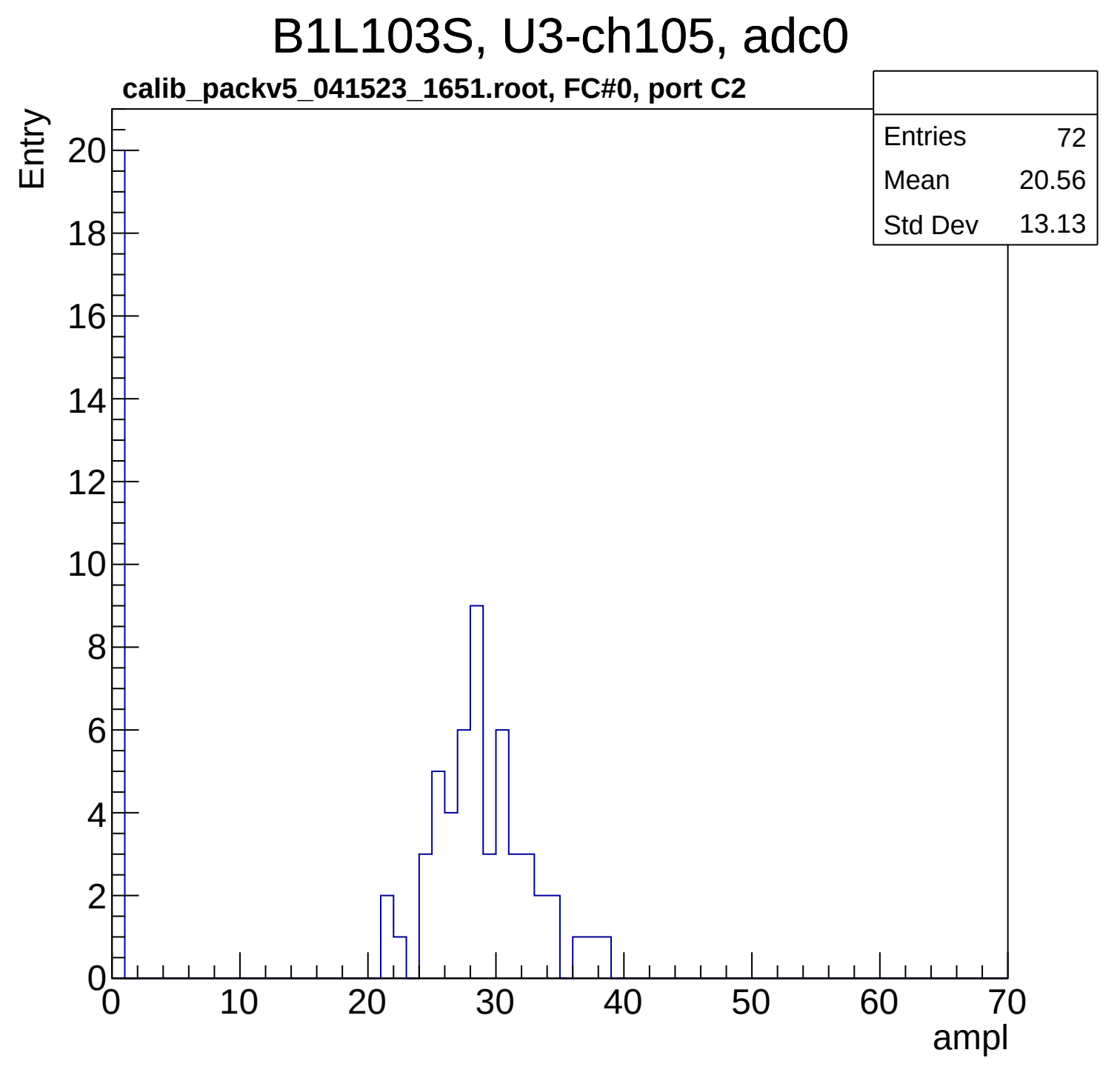
70
ampl


B1L103S, U3-ch105, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 20.56
Std Dev 13.13
Entry
ampl
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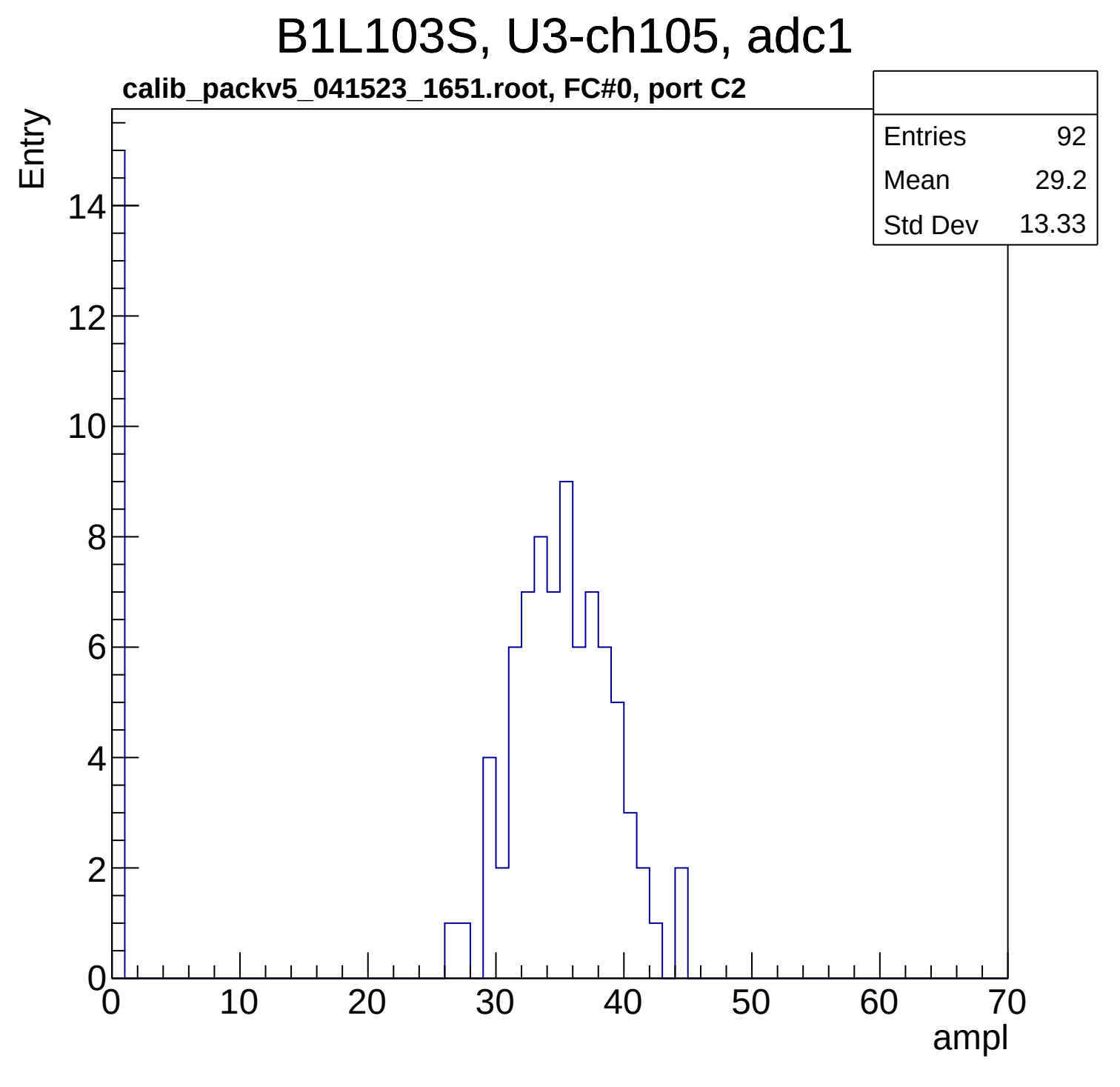
B1L103S, U3-ch105, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 29.2
Std Dev 13.33
Entry
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10
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50
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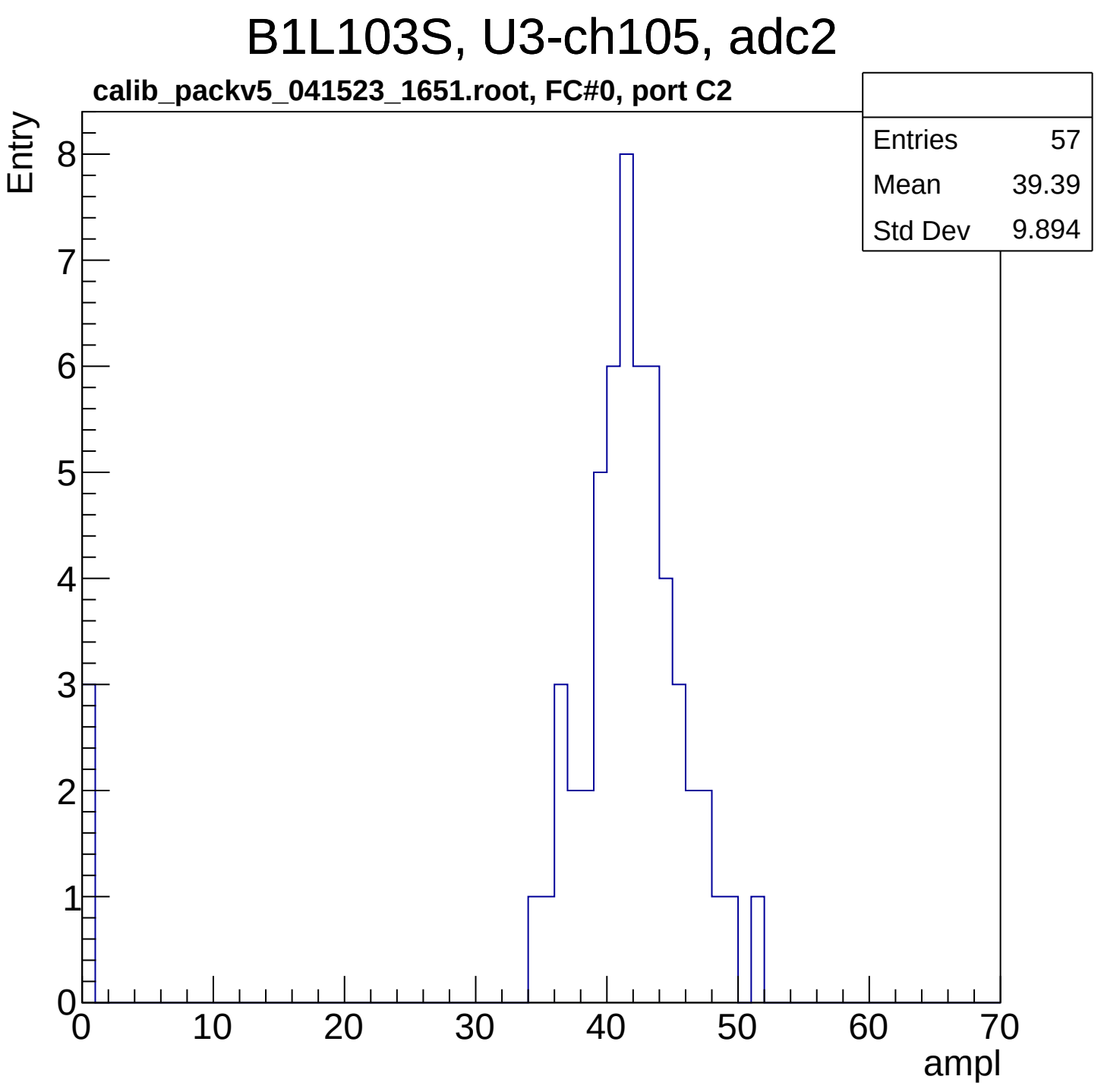
70
ampl


B1L103S, U3-ch105, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 39.39
Std Dev 9.894
Entry
ampl
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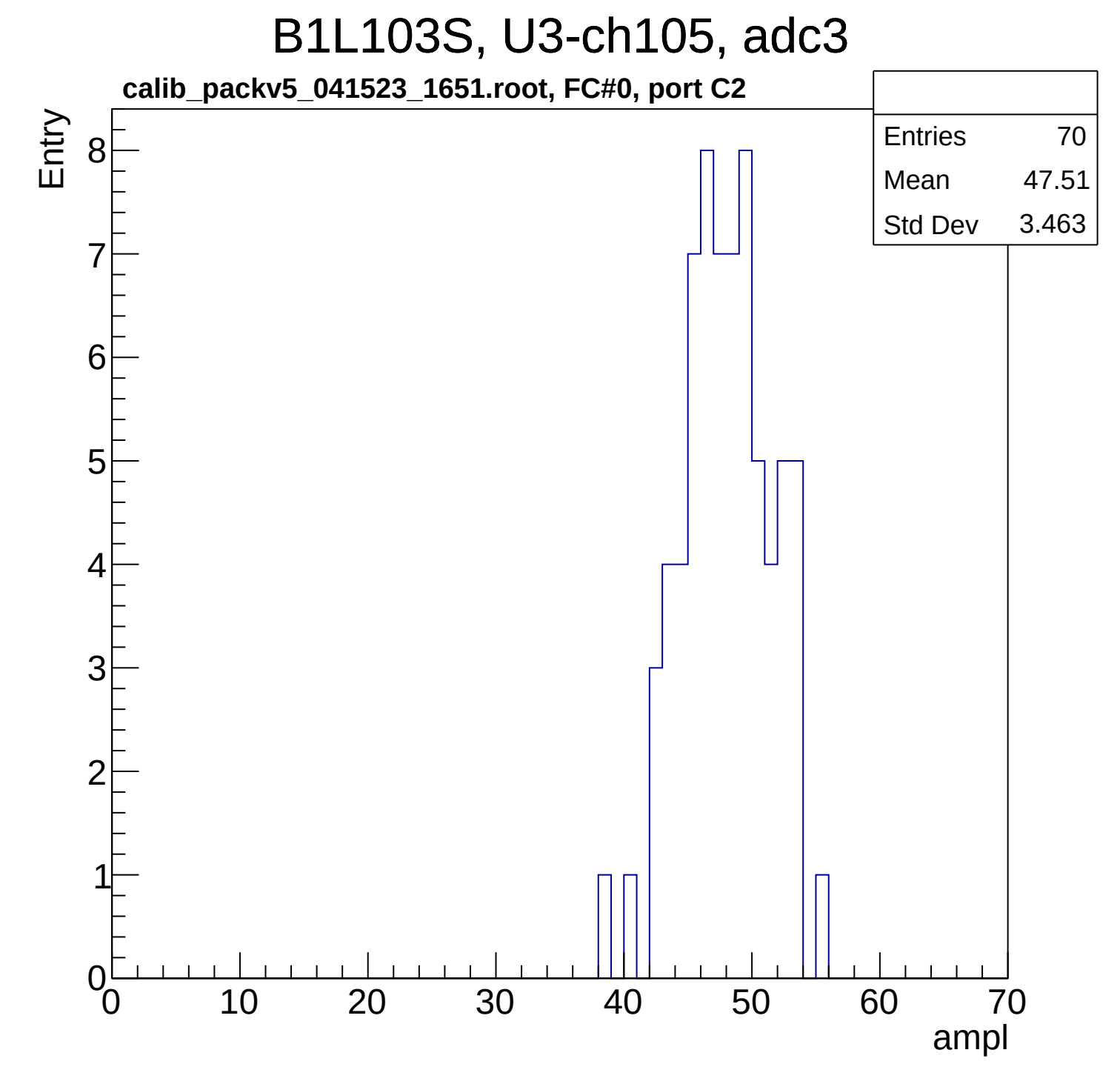
B1L103S, U3-ch105, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 47.51
Std Dev 3.463
Entry
ampl
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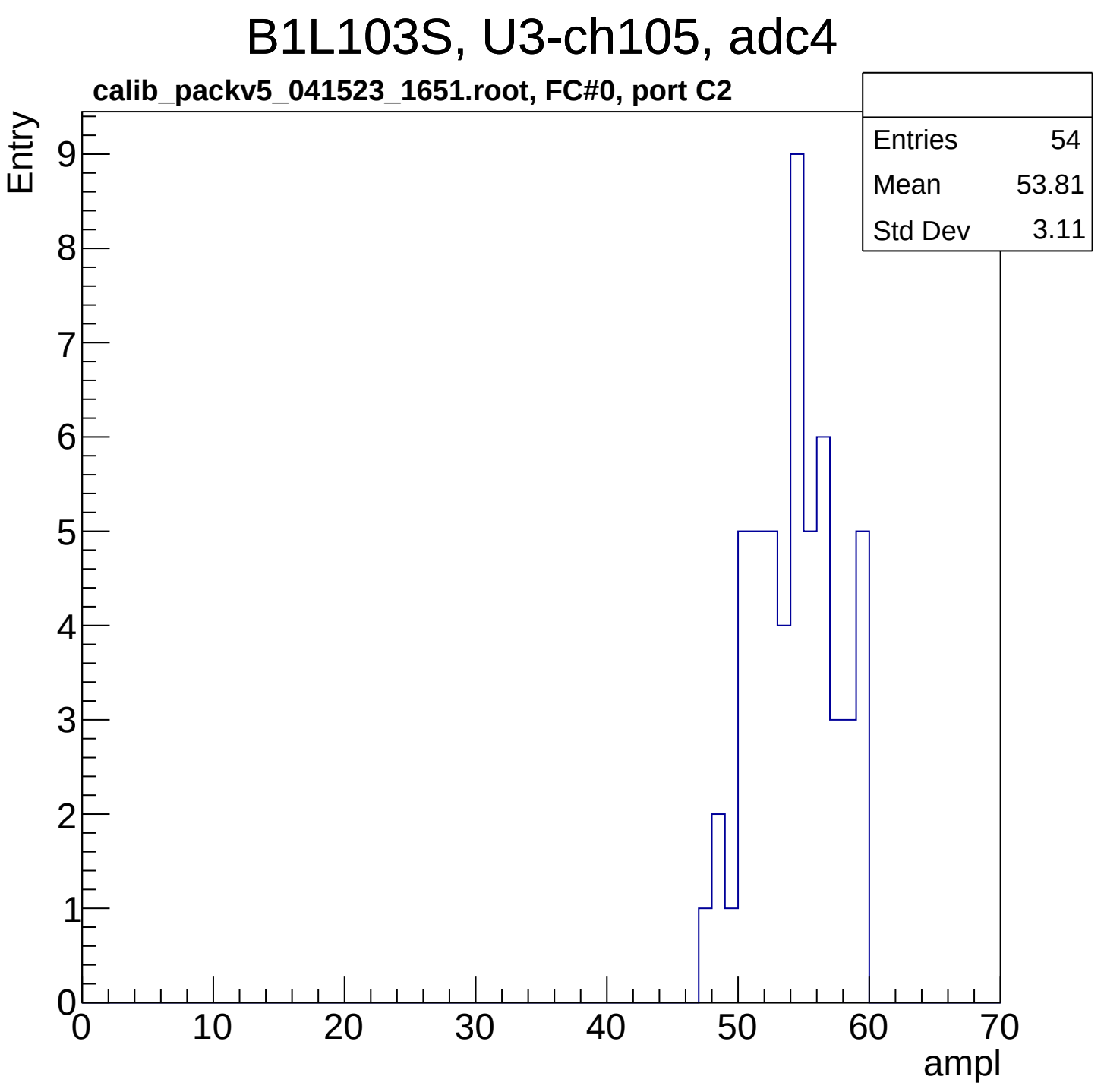
B1L103S, U3-ch105, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 53.81
Std Dev 3.11
Entry
ampl
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4
5
6
7
8
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0
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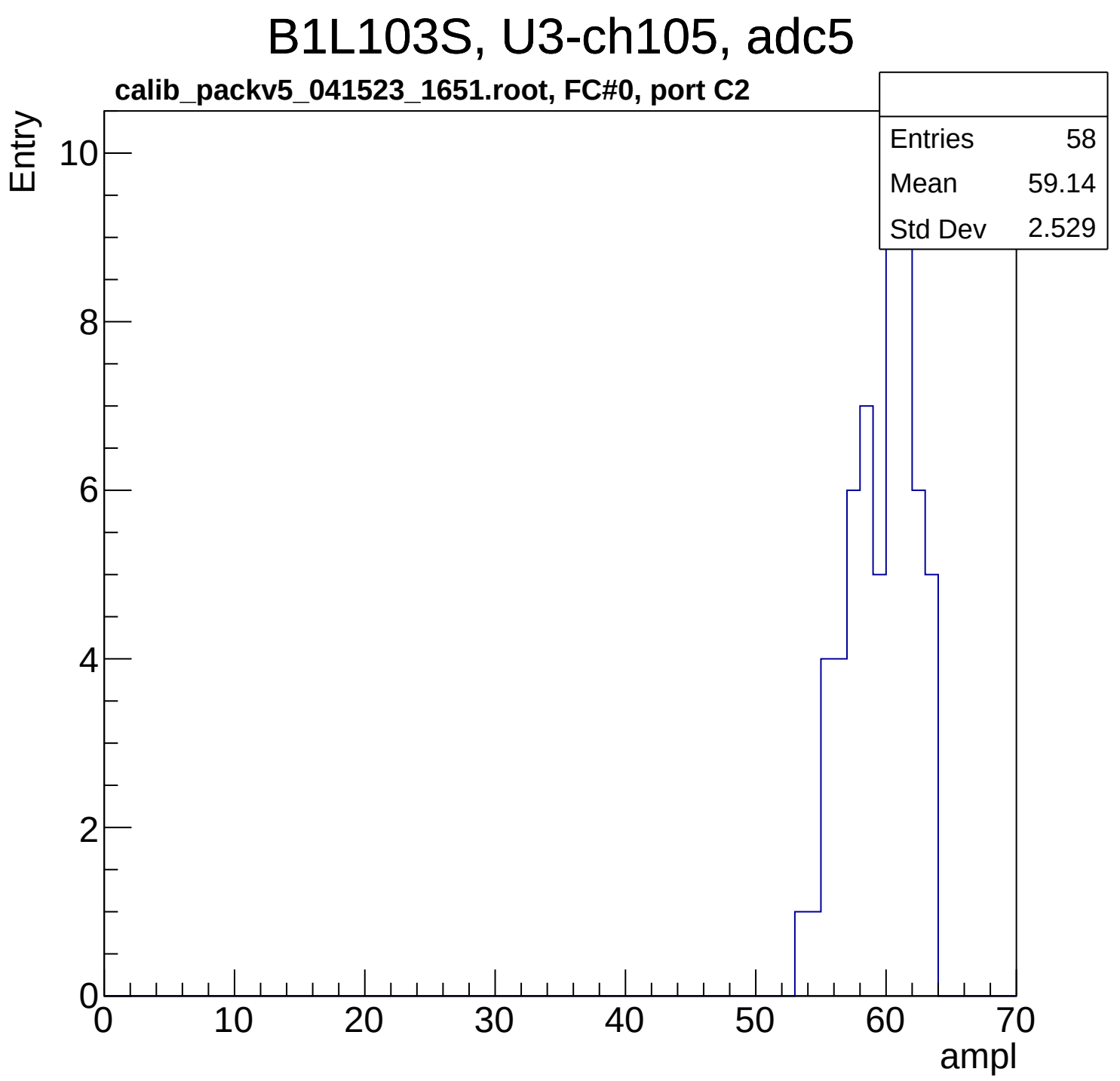
B1L103S, U3-ch105, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 59.14
Std Dev 2.529
Entry
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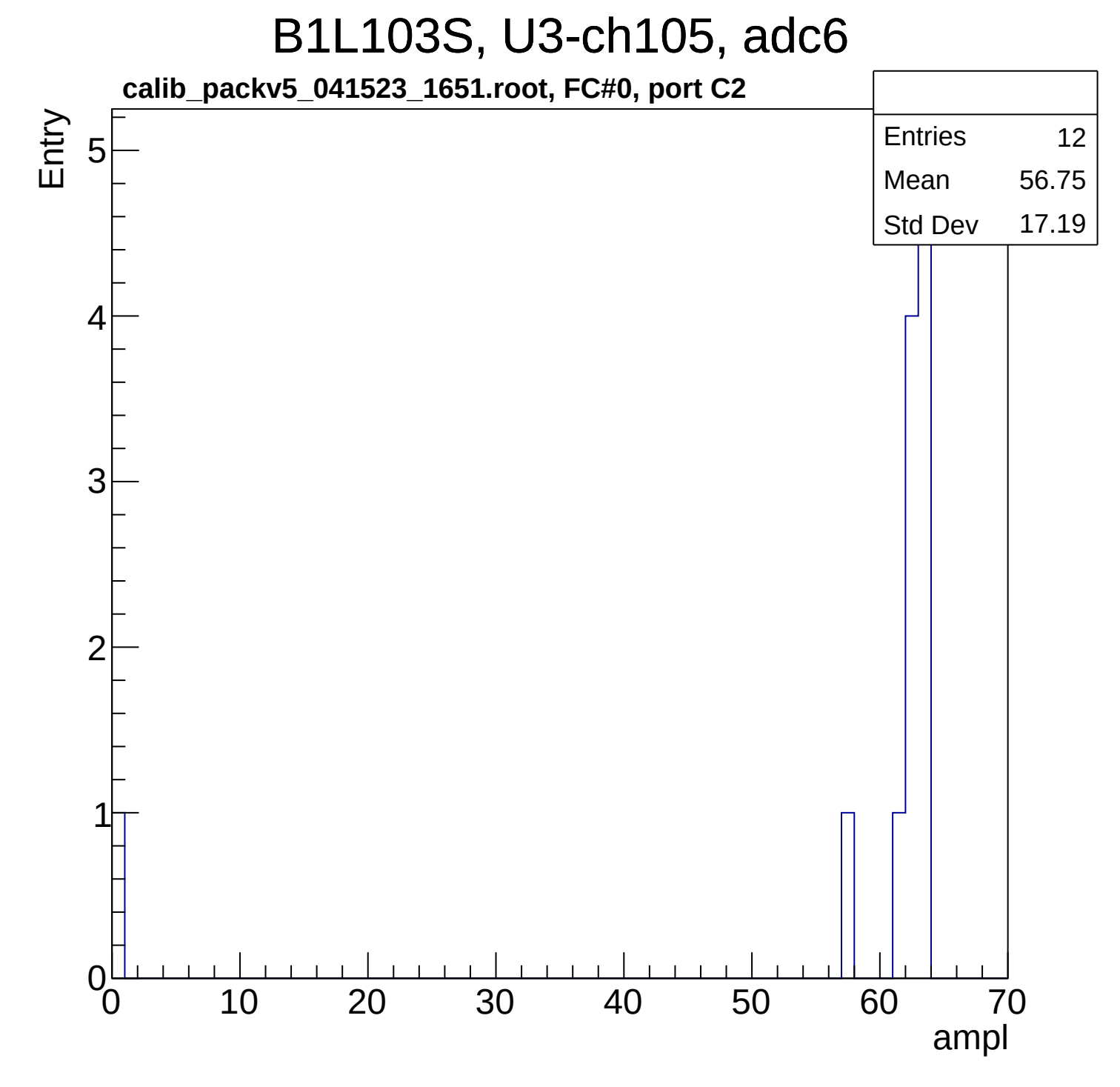
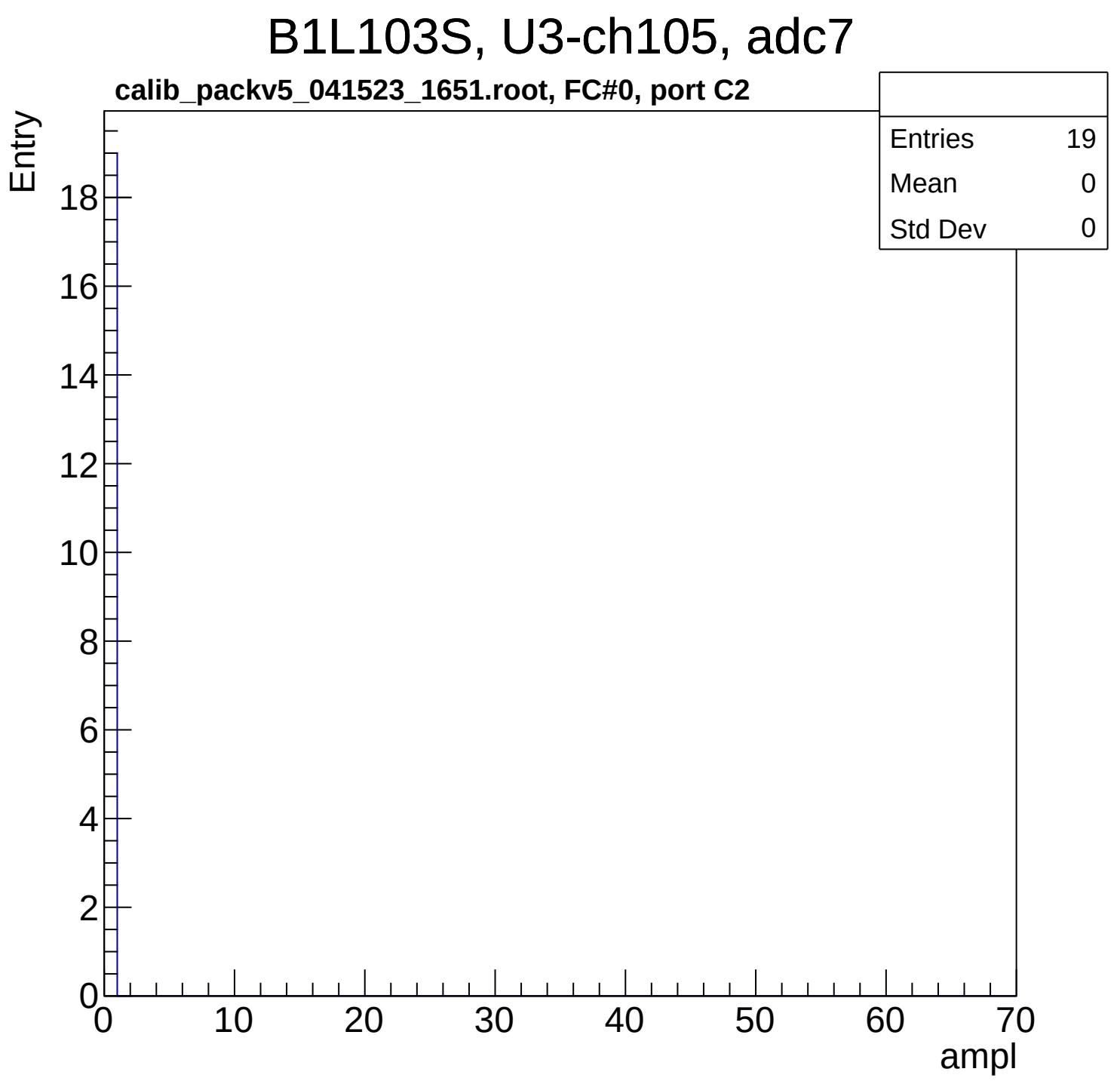
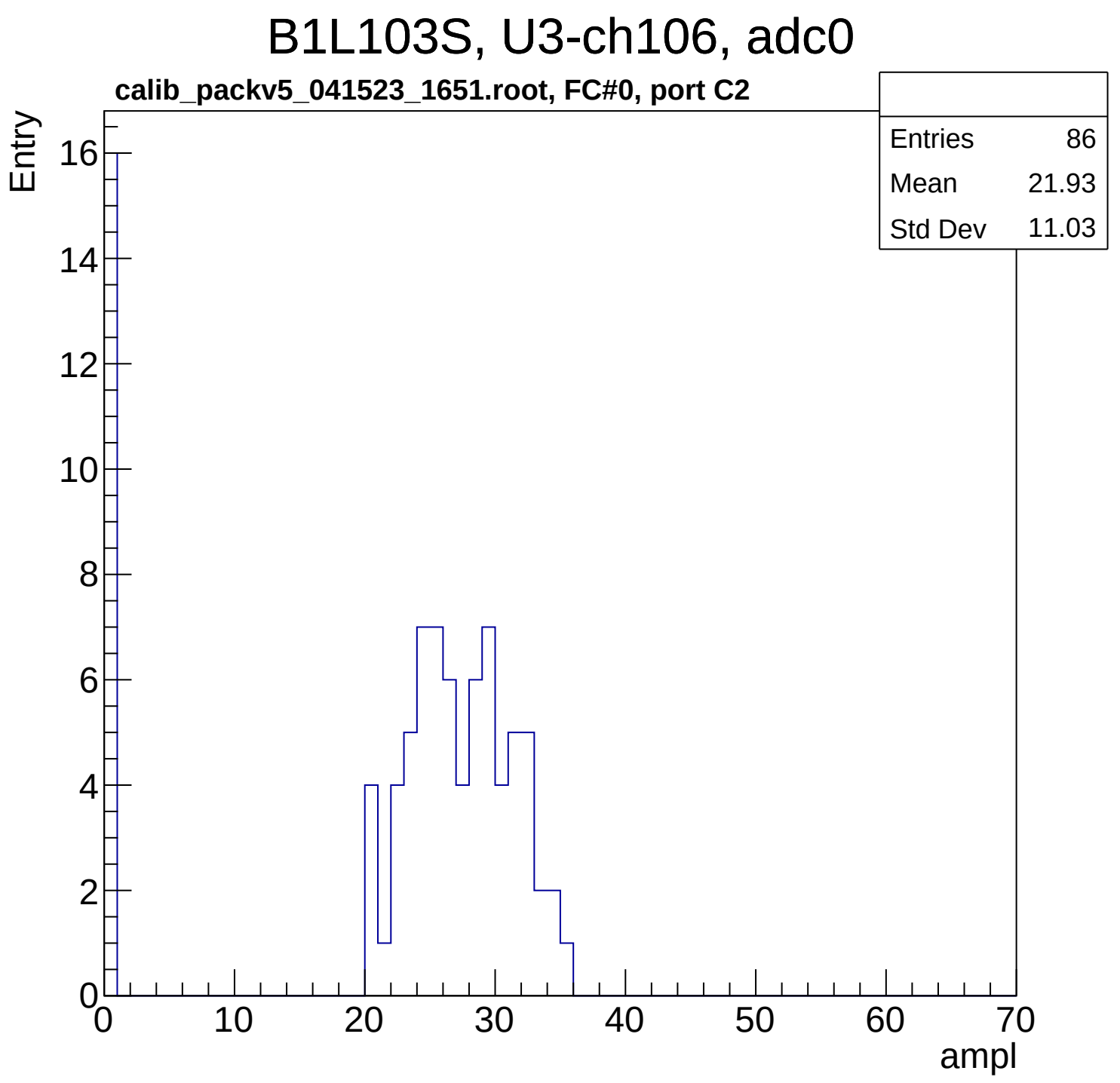
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch105, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 56.75
Std Dev 17.19
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U3-ch105, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch106, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 21.93
Std Dev 11.03
Entry
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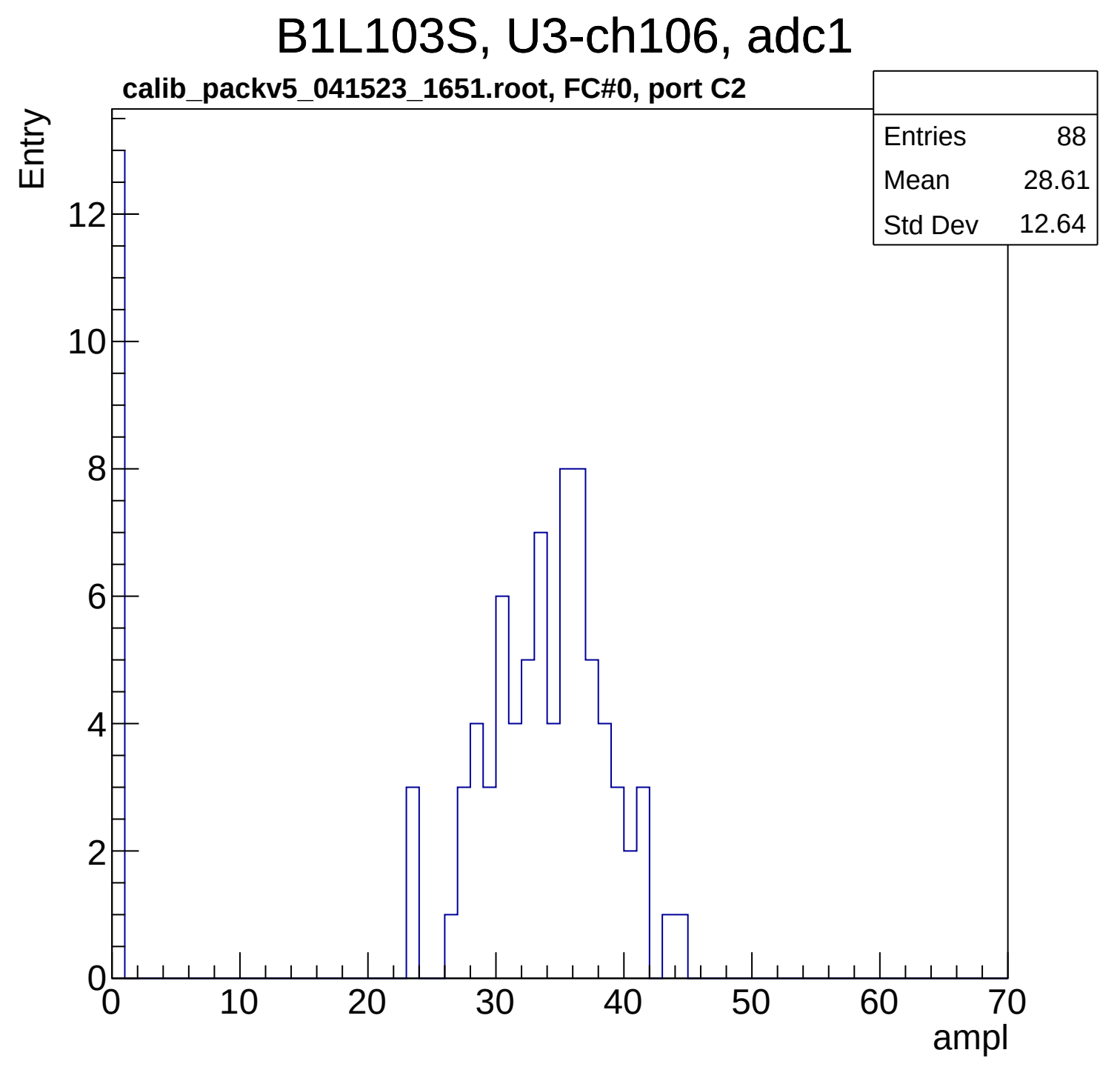
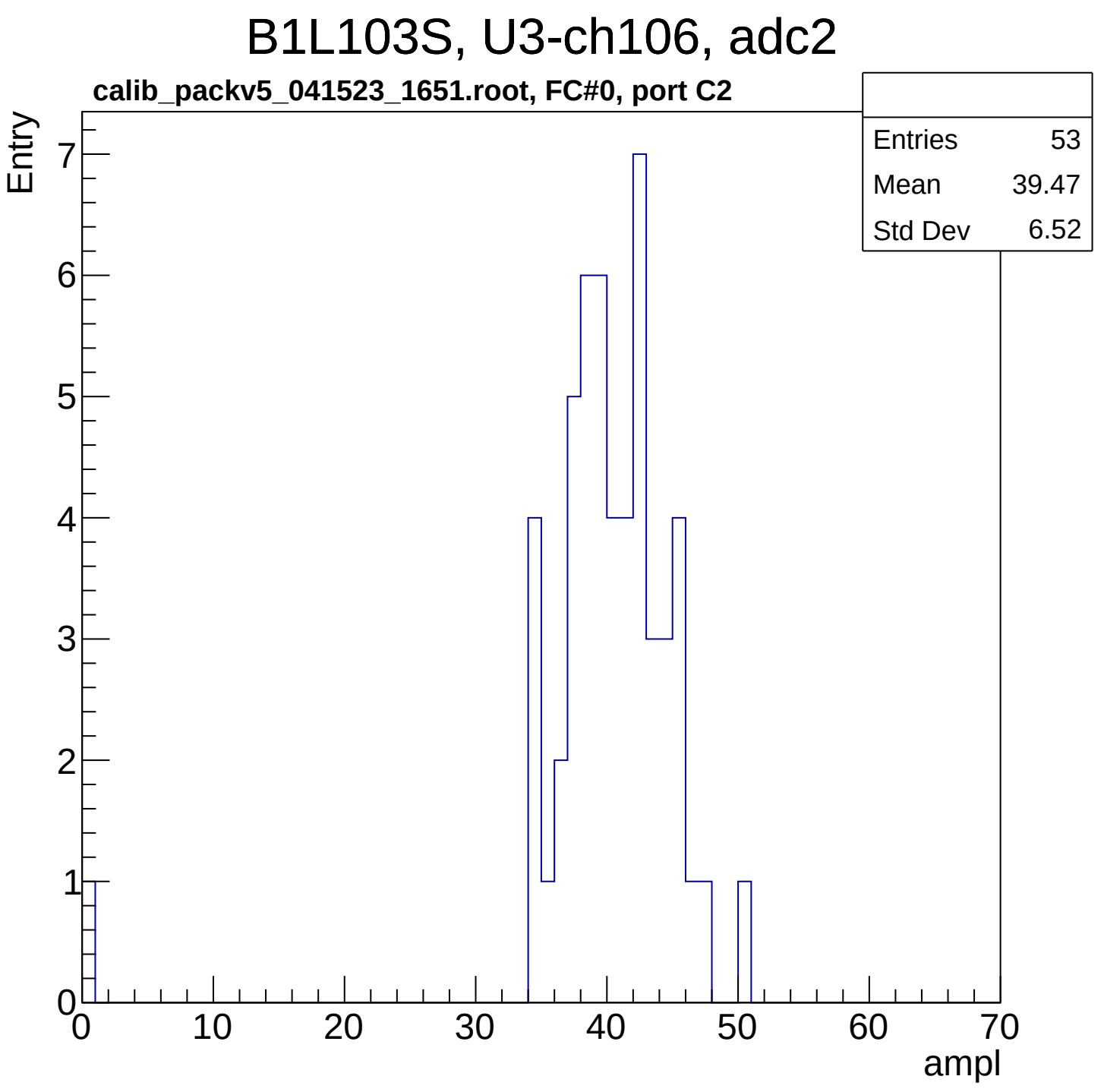
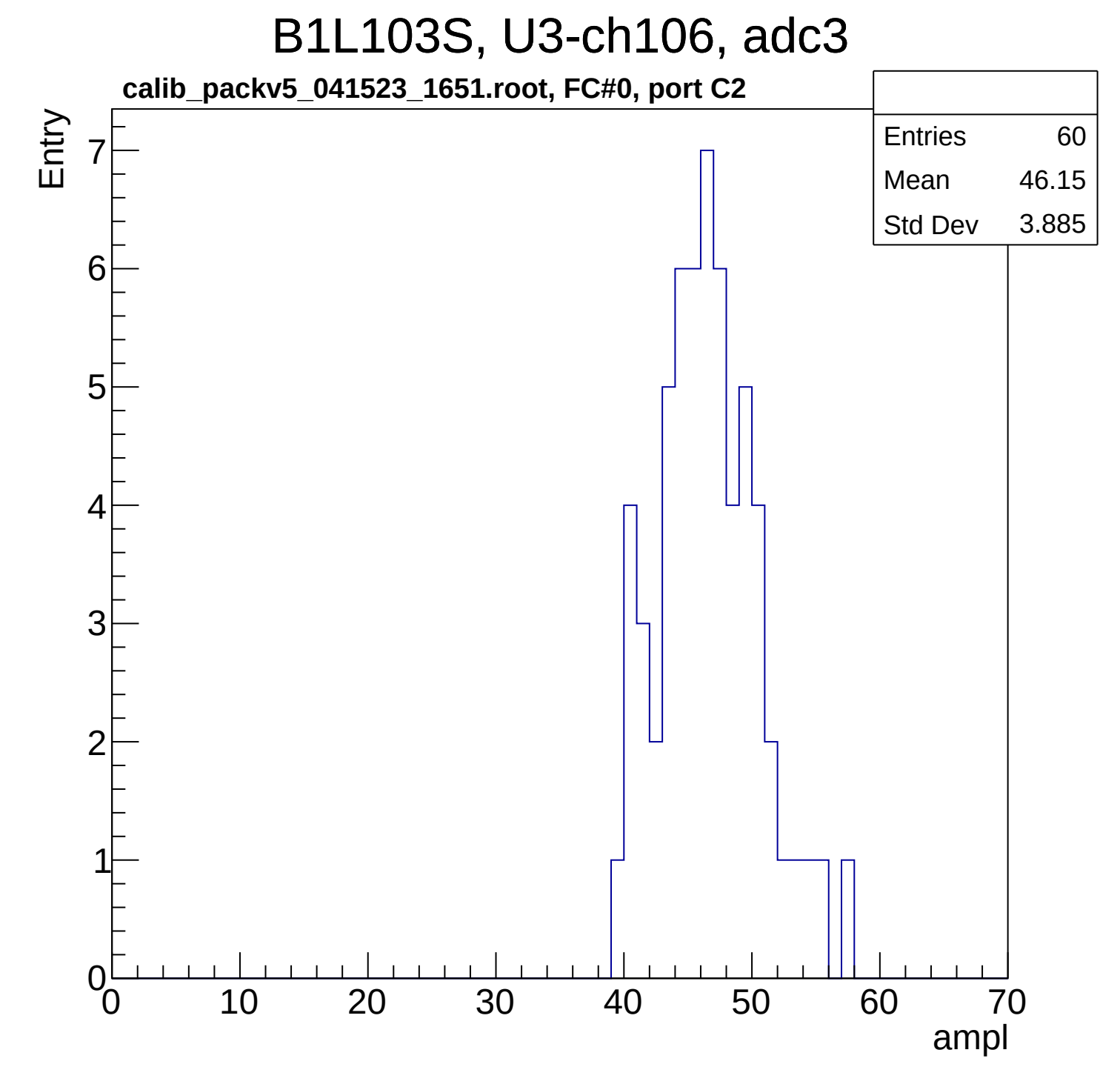
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch106, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 28.61
Std Dev 12.64
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch106, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 39.47
Std Dev 6.52
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch106, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 46.15
Std Dev 3.885
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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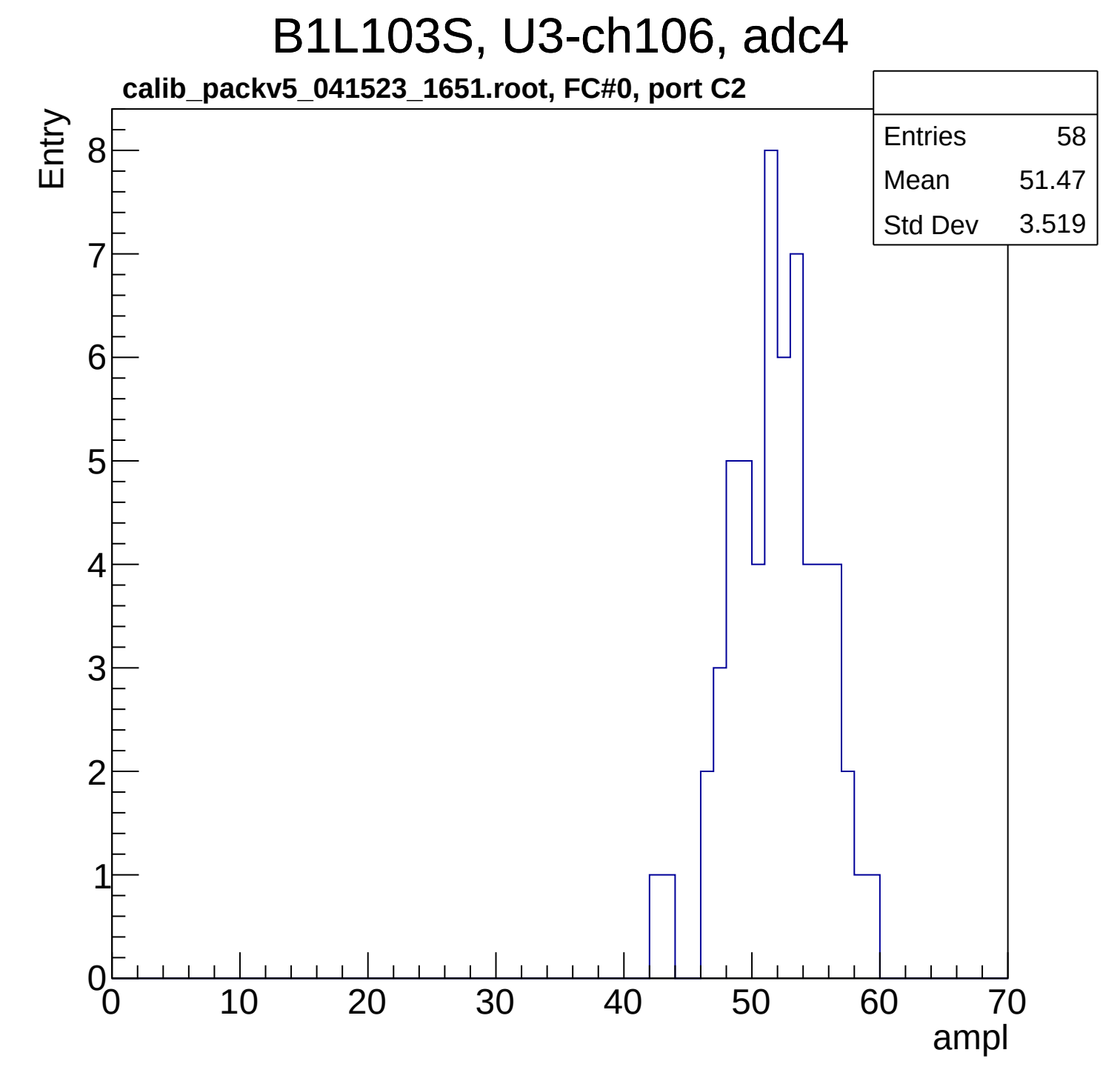
40
50
60
70


B1L103S, U3-ch106, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 51.47
Std Dev 3.519
Entry
ampl
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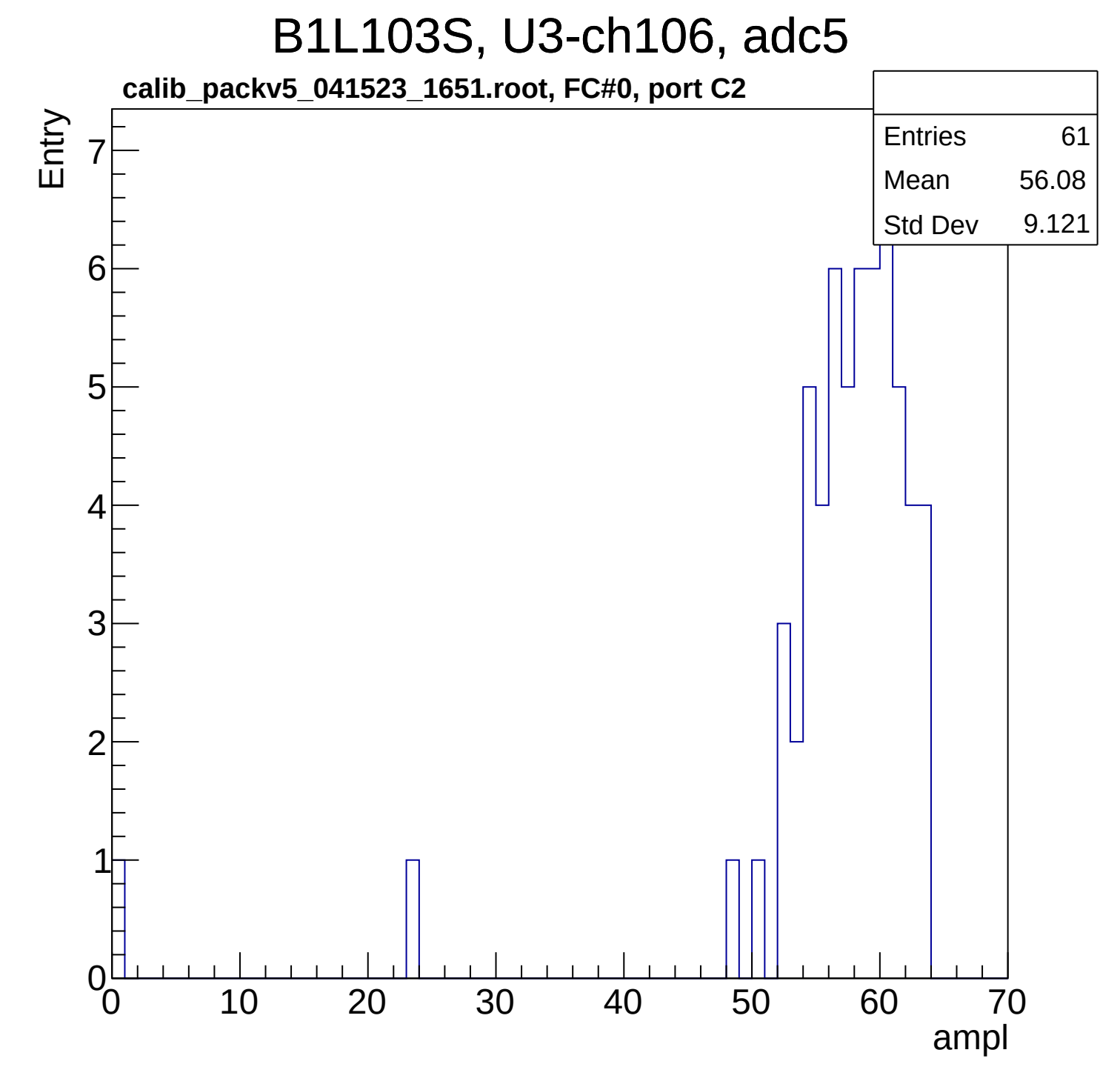
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch106, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 56.08
Std Dev 9.121
Entry
ampl
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4
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0
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40
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60
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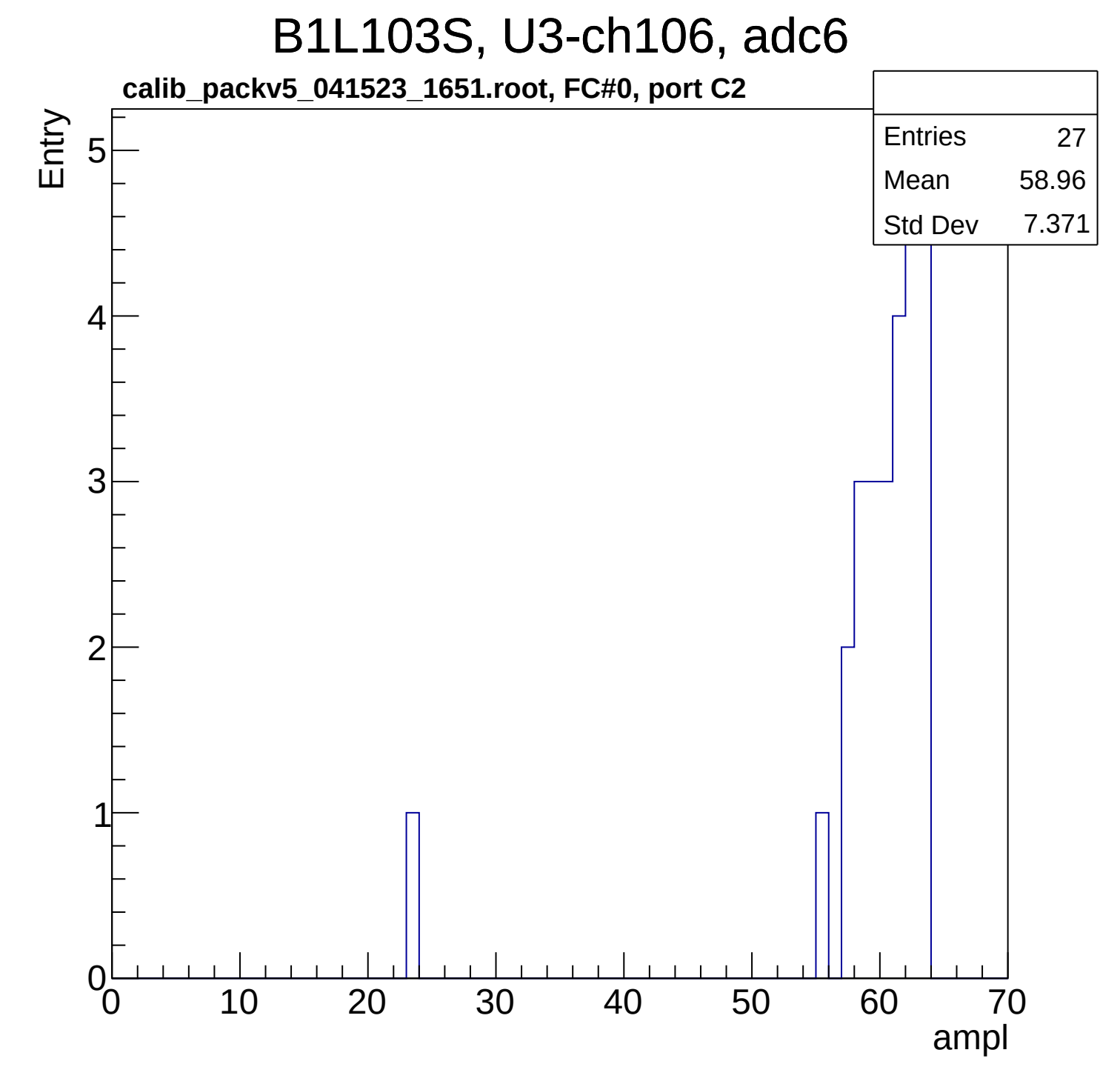
B1L103S, U3-ch106, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 58.96
Std Dev 7.371
Entry
ampl
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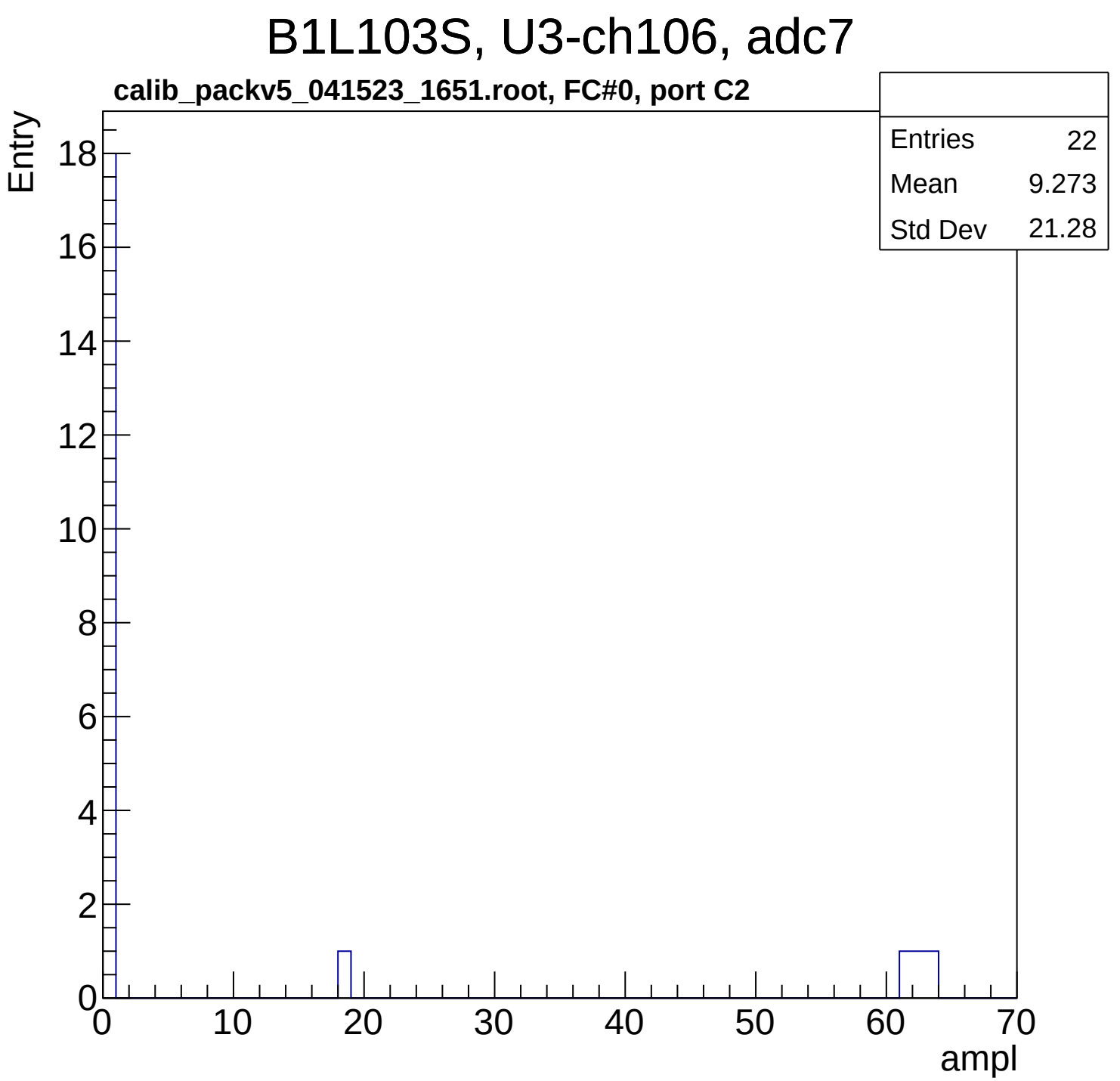
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U3-ch106, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 9.273
Std Dev 21.28
Entry
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8
10
12
14
16
18
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10
20
30
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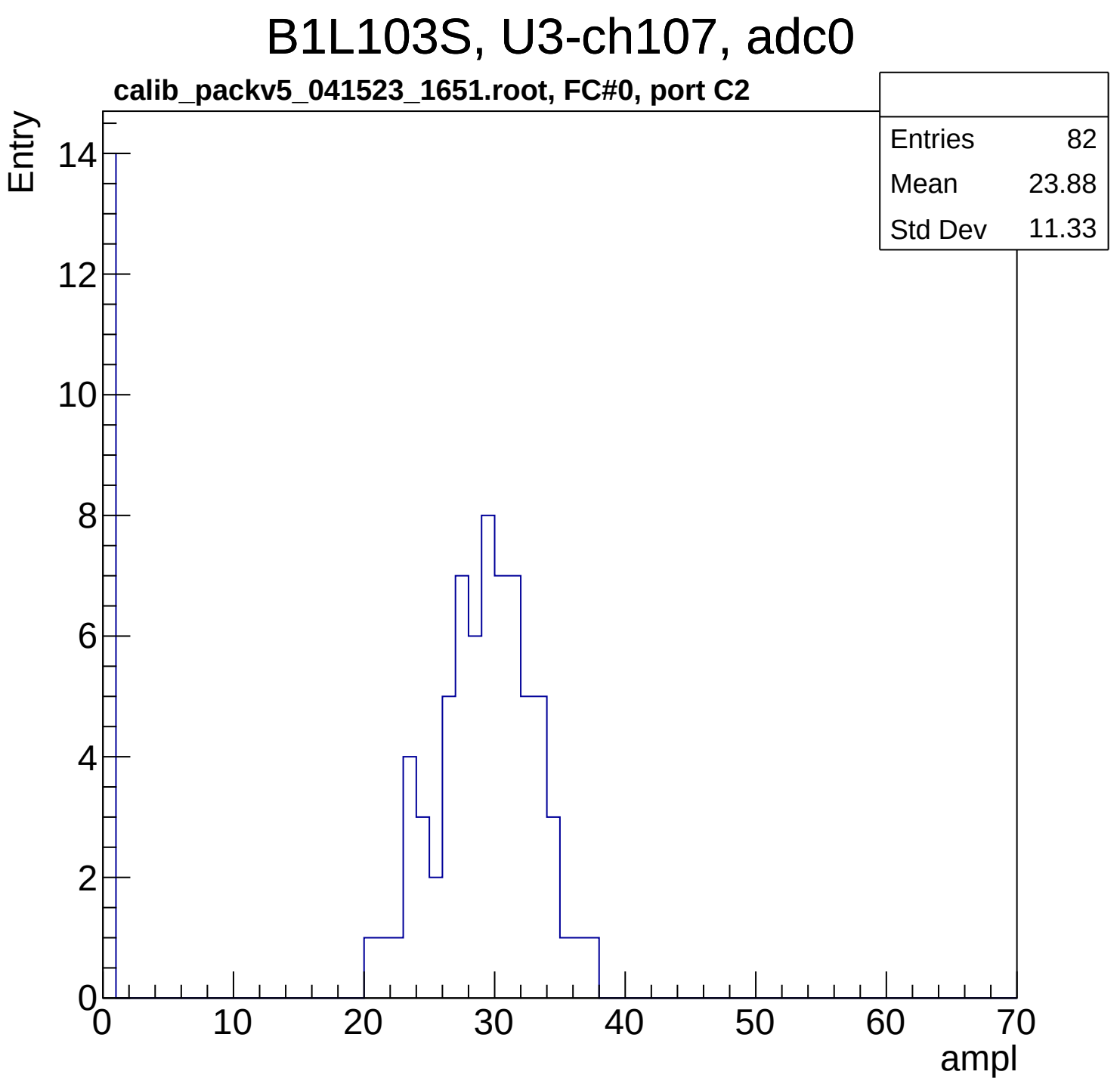
50
60
70
ampl


B1L103S, U3-ch107, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 23.88
Std Dev 11.33
Entry
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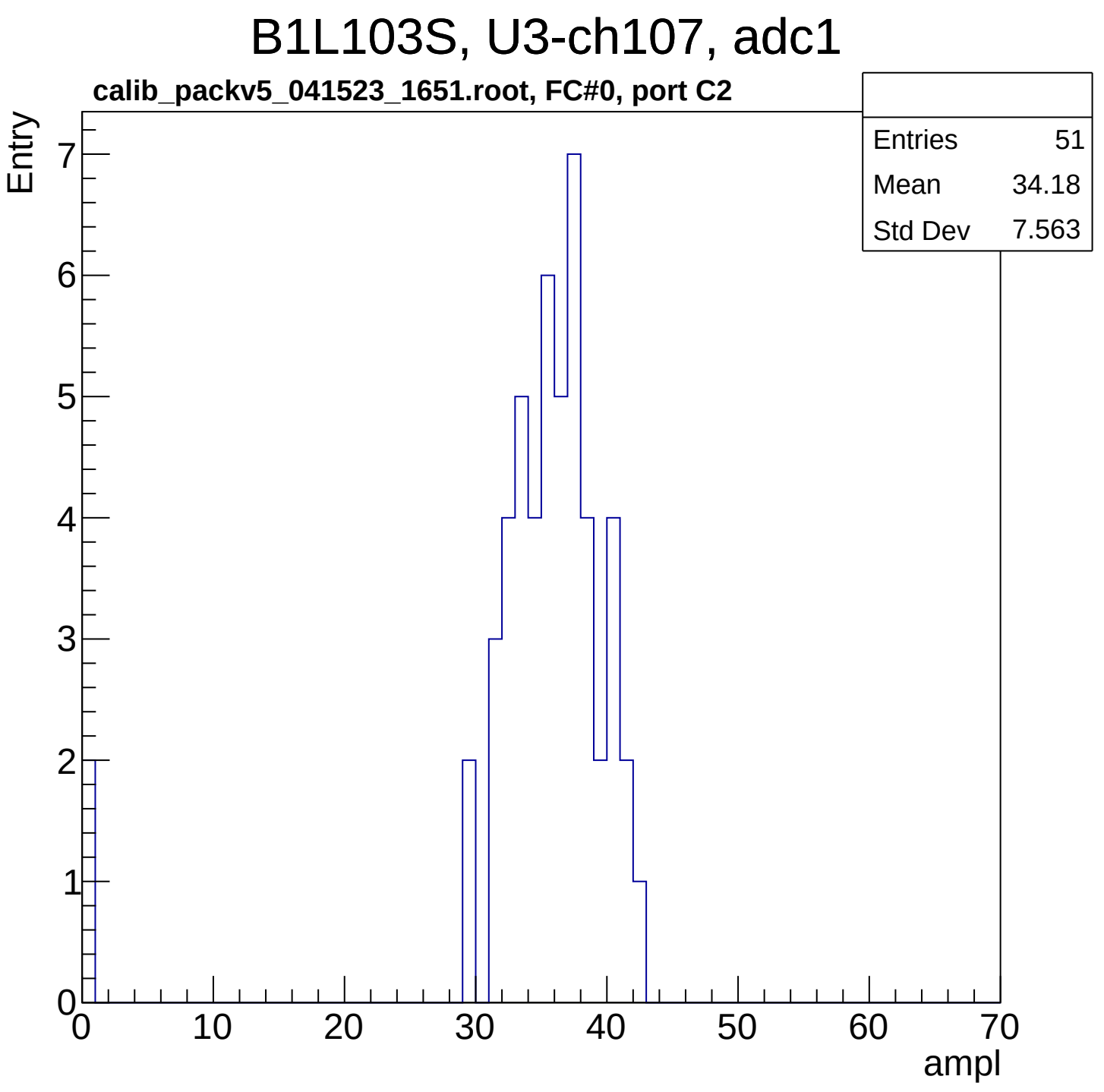
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch107, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 34.18
Std Dev 7.563
Entry
ampl
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2
3
4
5
6
7
0
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20
30
40
50
60
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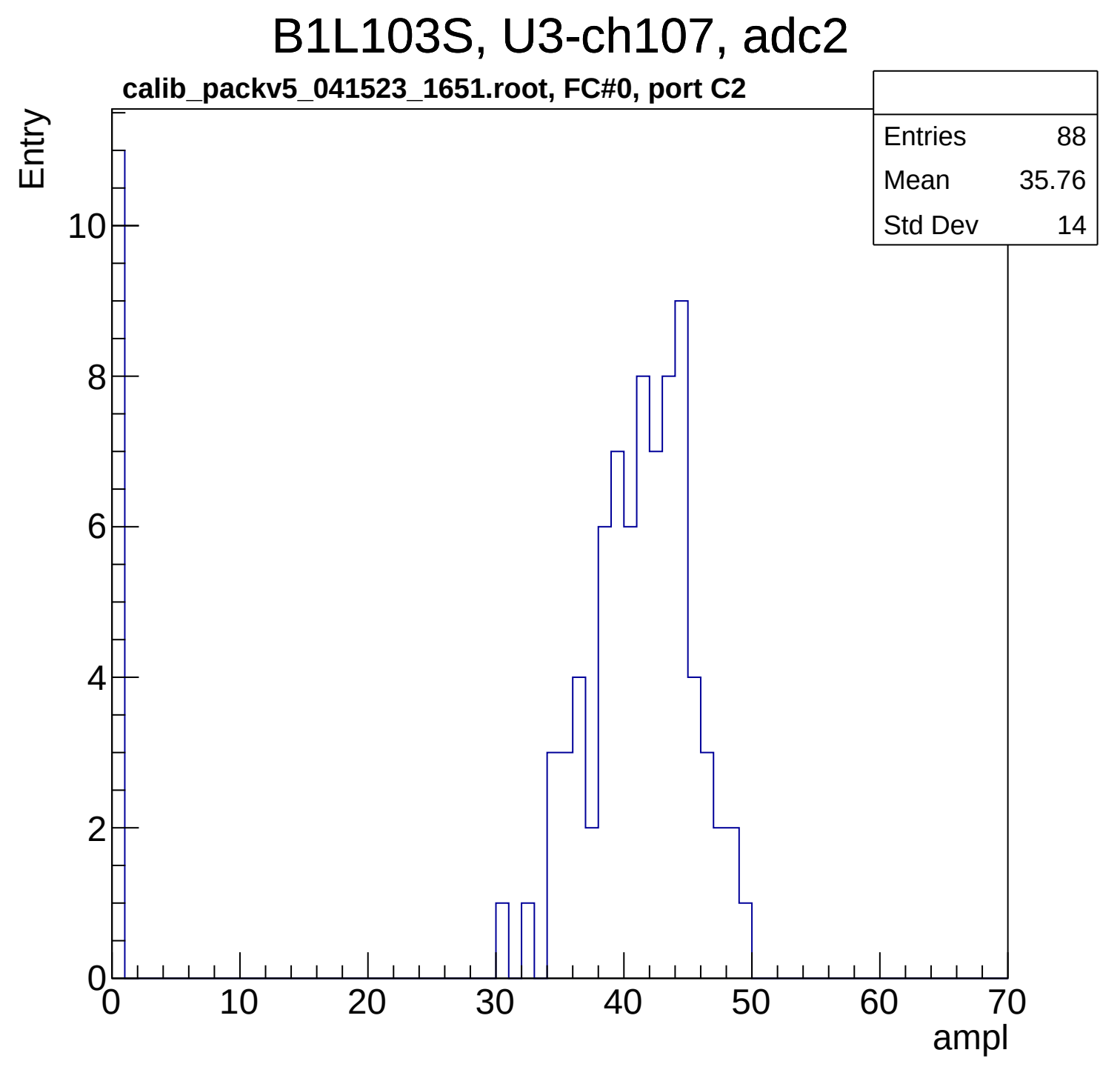
B1L103S, U3-ch107, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 35.76
Std Dev 14
Entry
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6
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10
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10
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50
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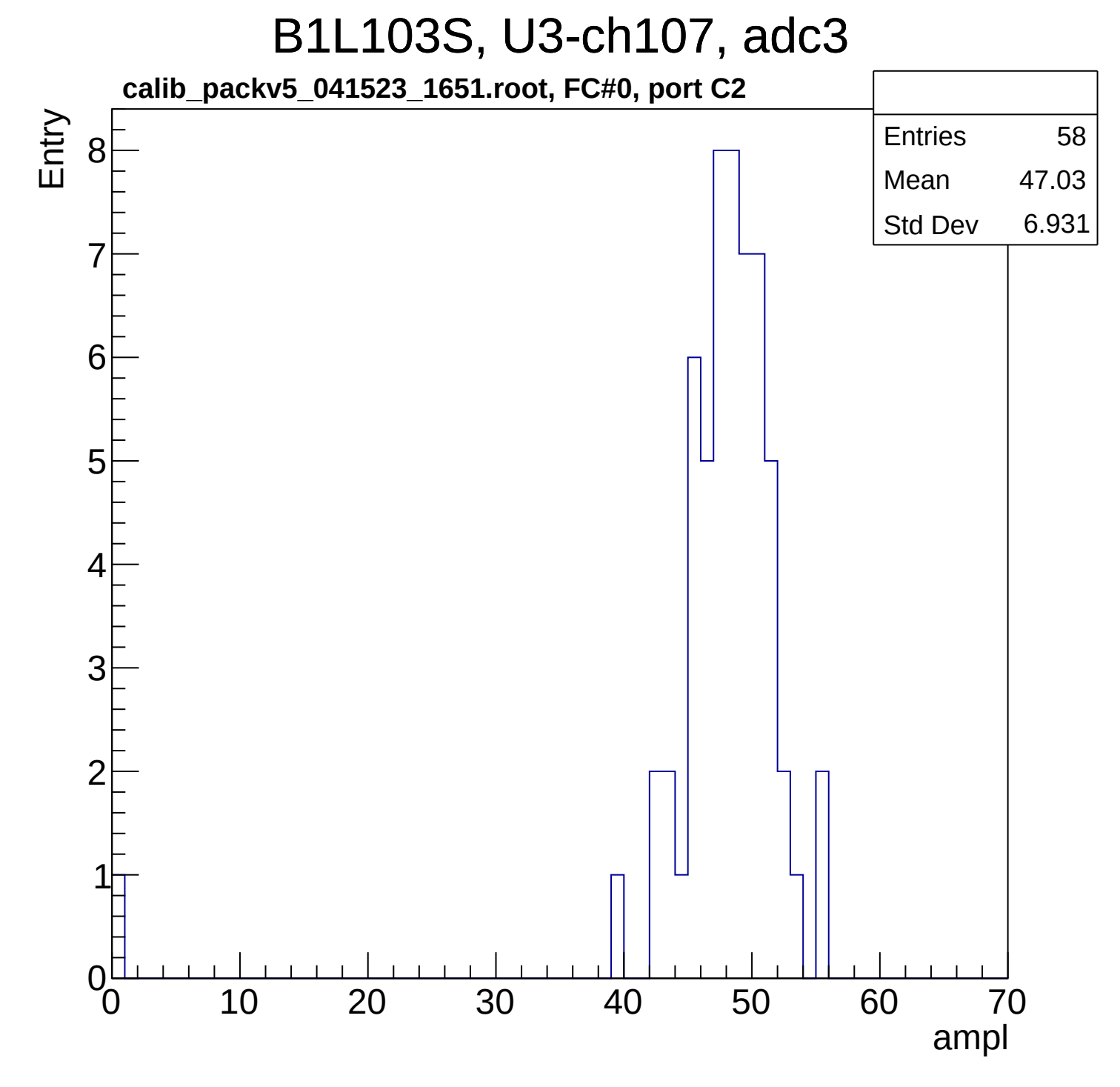
70
ampl


B1L103S, U3-ch107, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 47.03
Std Dev 6.931
Entry
ampl
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4
5
6
7
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0
10
20
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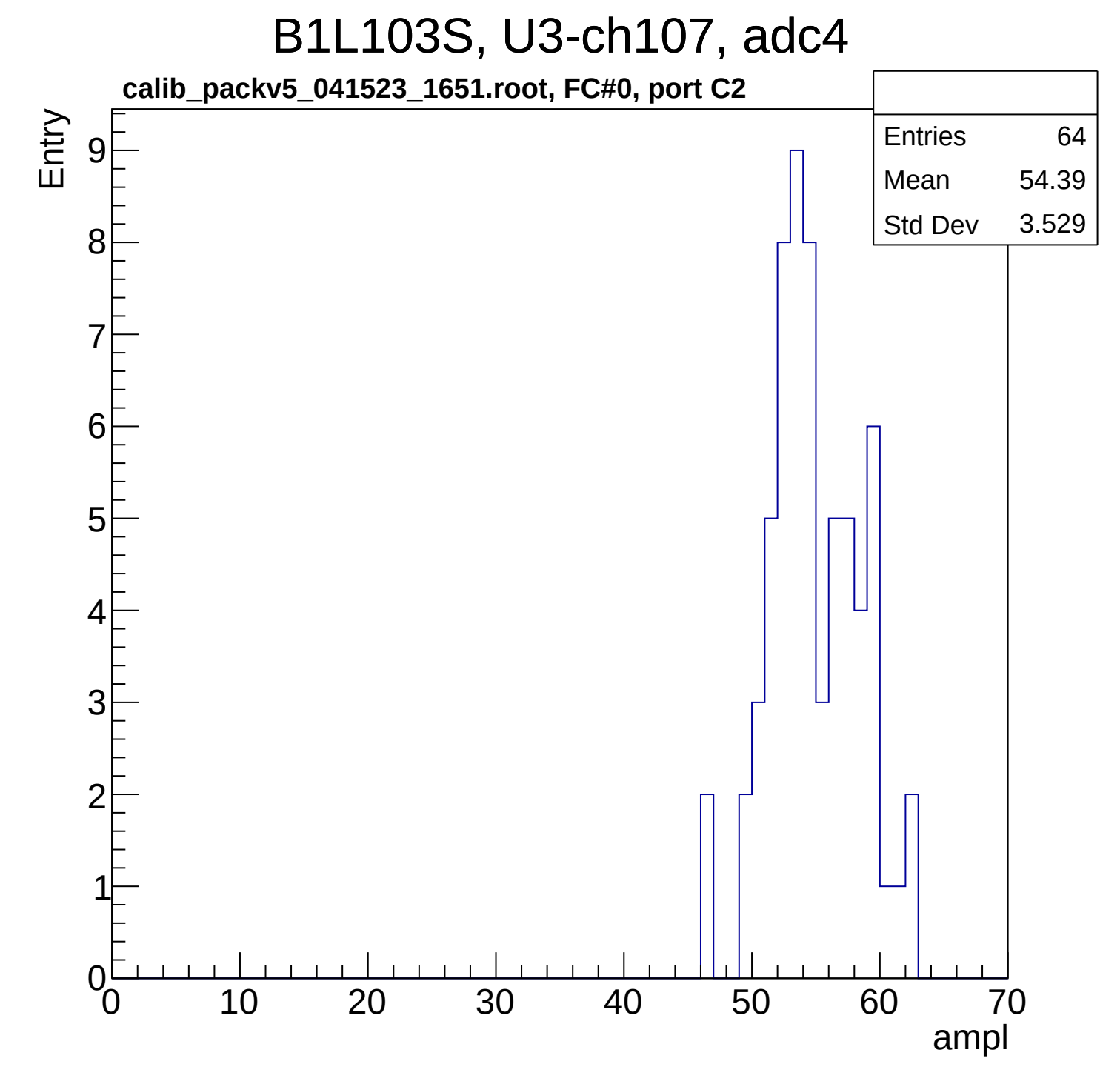
60
70


B1L103S, U3-ch107, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 54.39
Std Dev 3.529
Entry
ampl
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4
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6
7
8
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0
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60
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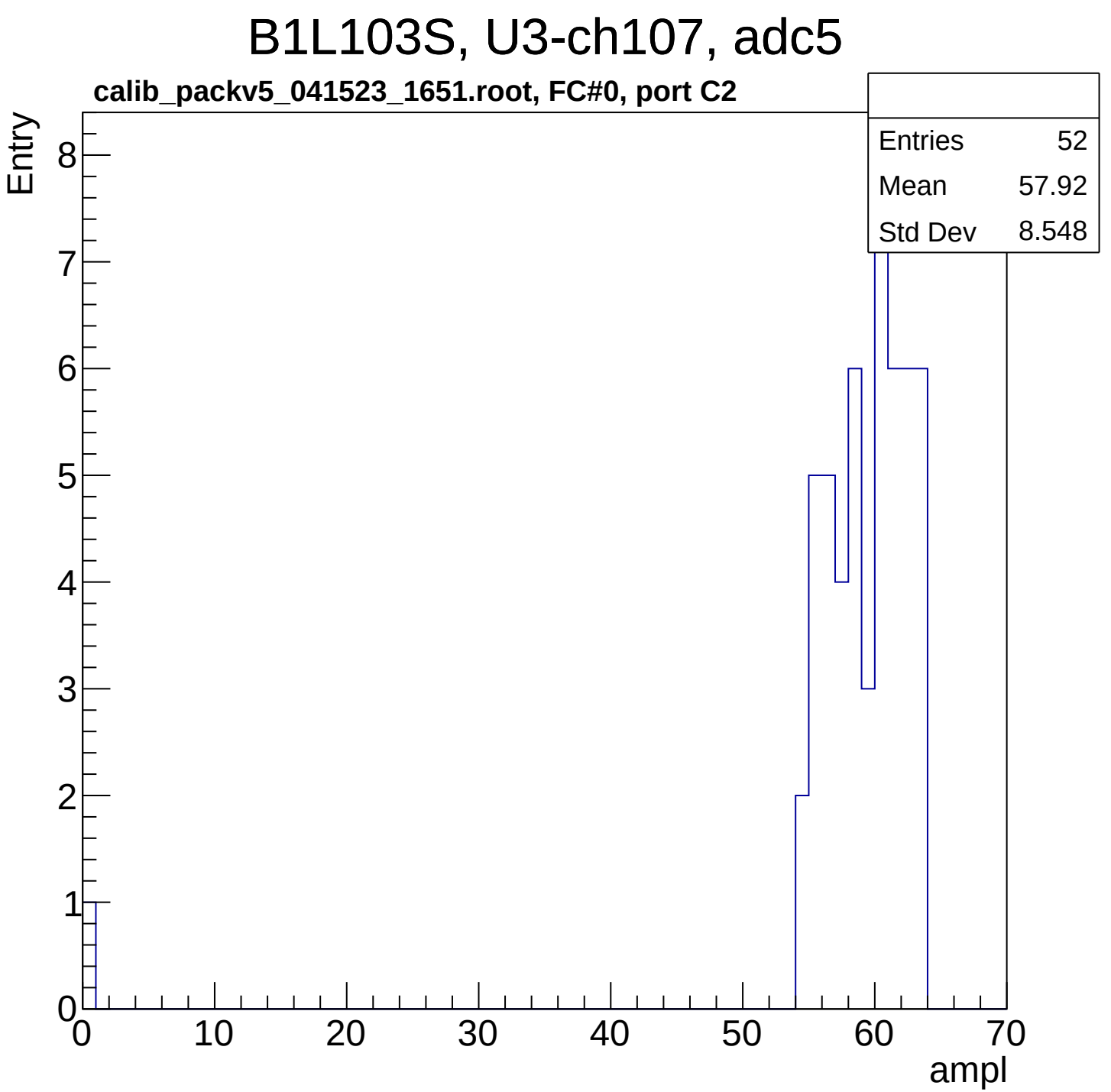
B1L103S, U3-ch107, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 57.92
Std Dev 8.548
Entry
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6
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0
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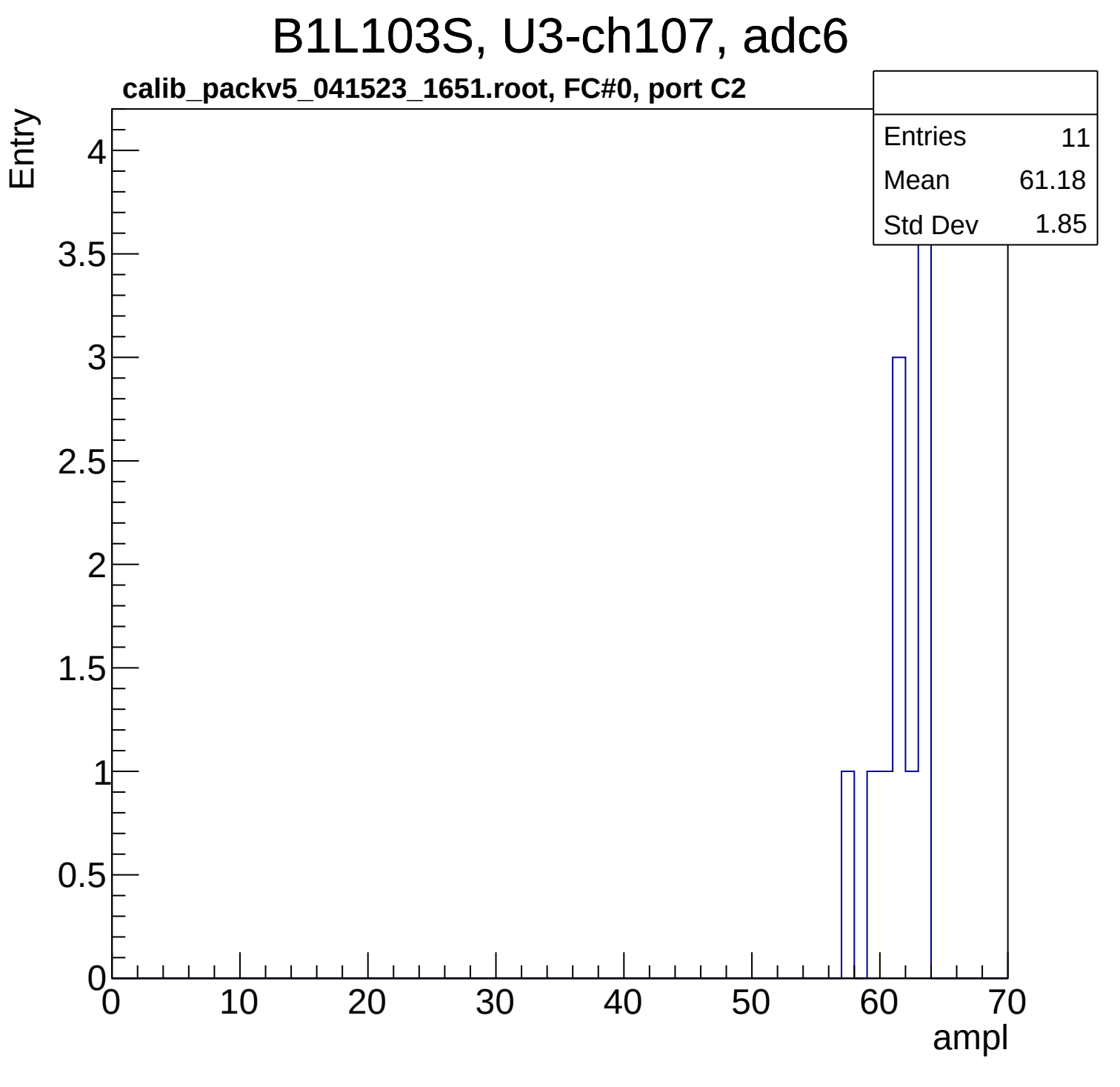
B1L103S, U3-ch107, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 61.18
Std Dev 1.85
Entry
ampl
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1.5
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3
3.5
4
0
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20
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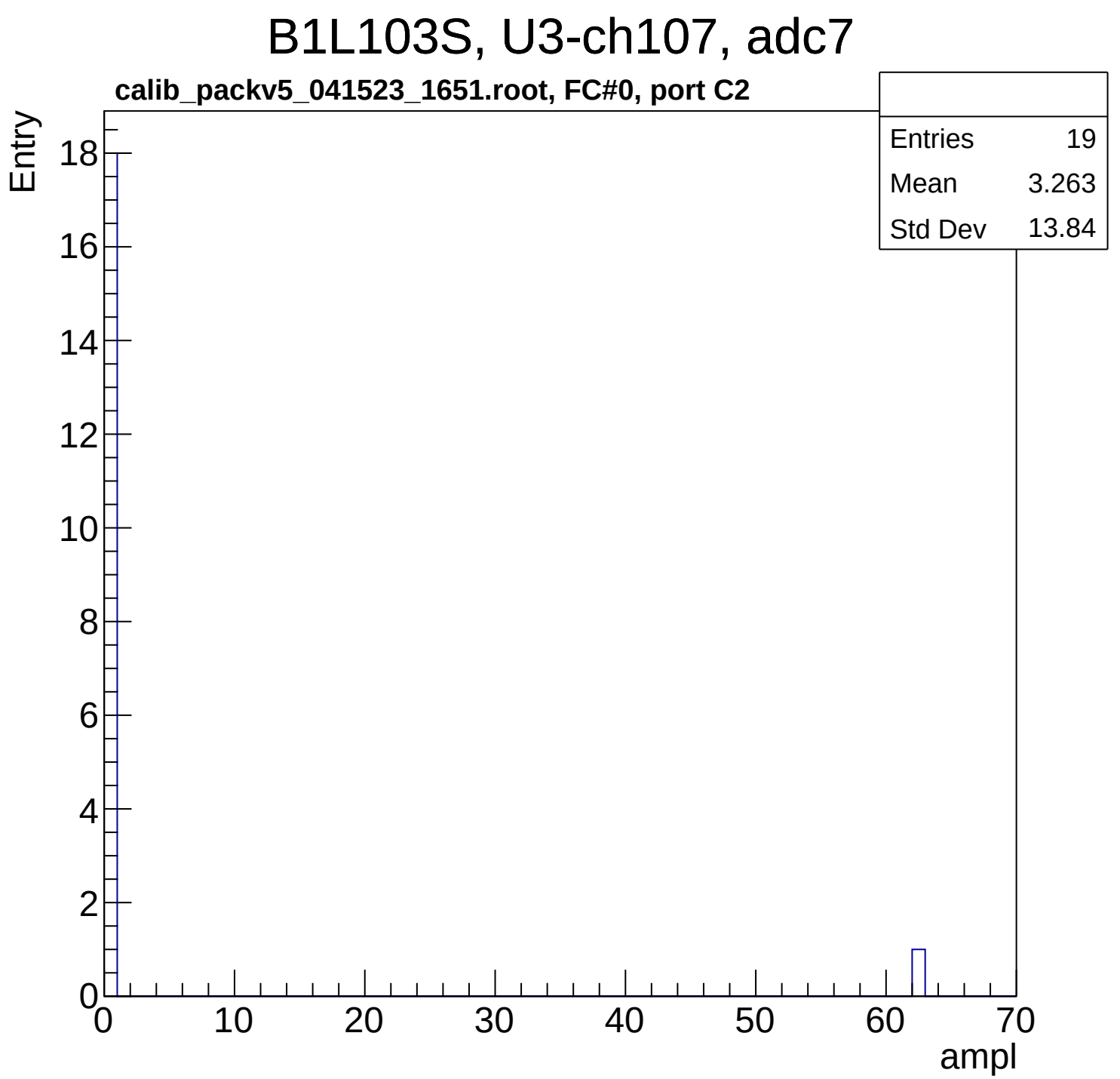
B1L103S, U3-ch107, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.263
Std Dev 13.84
Entry
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14
16
18
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10
20
30
40
50
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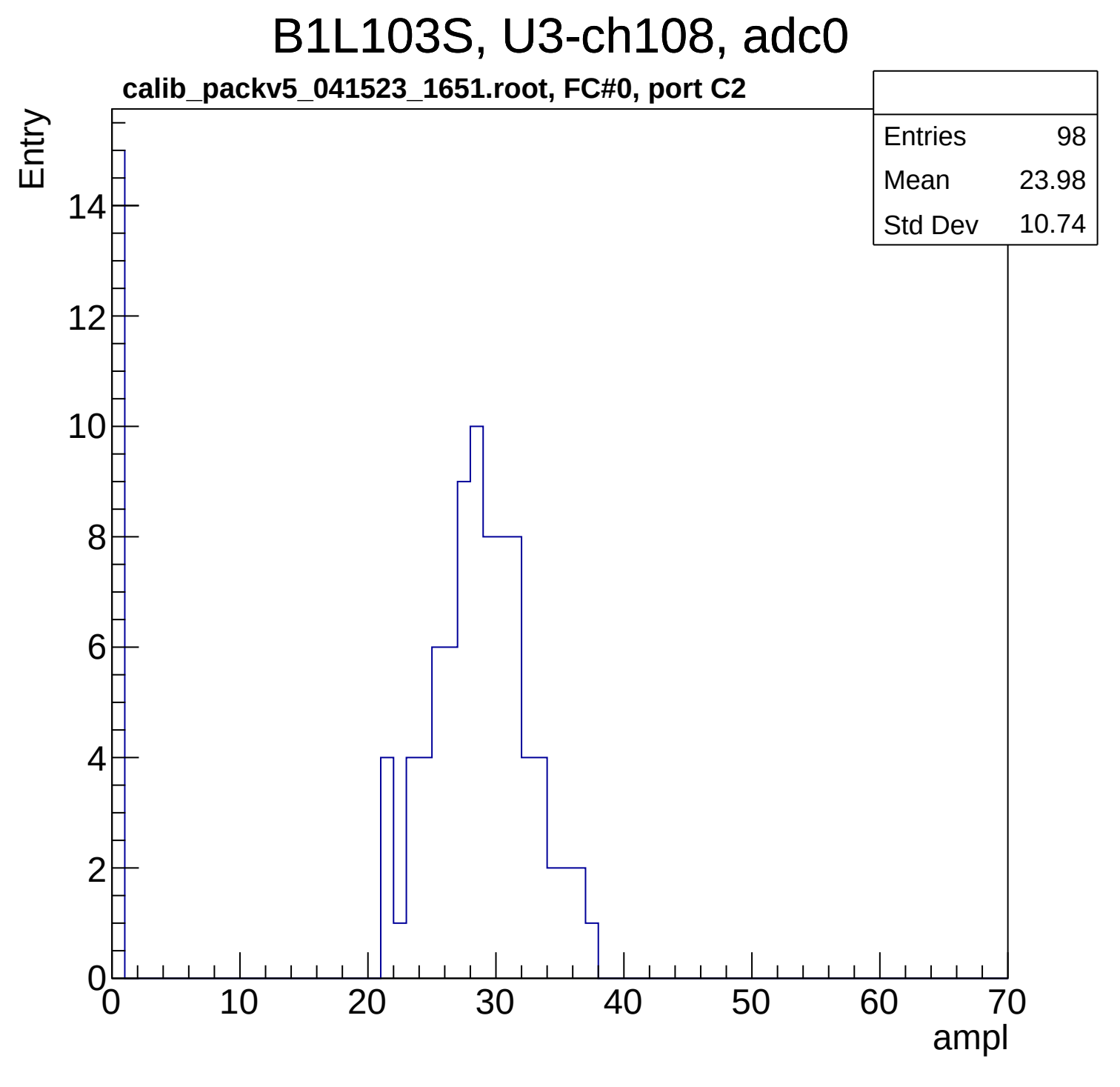
70
ampl


B1L103S, U3-ch108, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 98
Mean 23.98
Std Dev 10.74
Entry
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6
8
10
12
14
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10
20
30
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50
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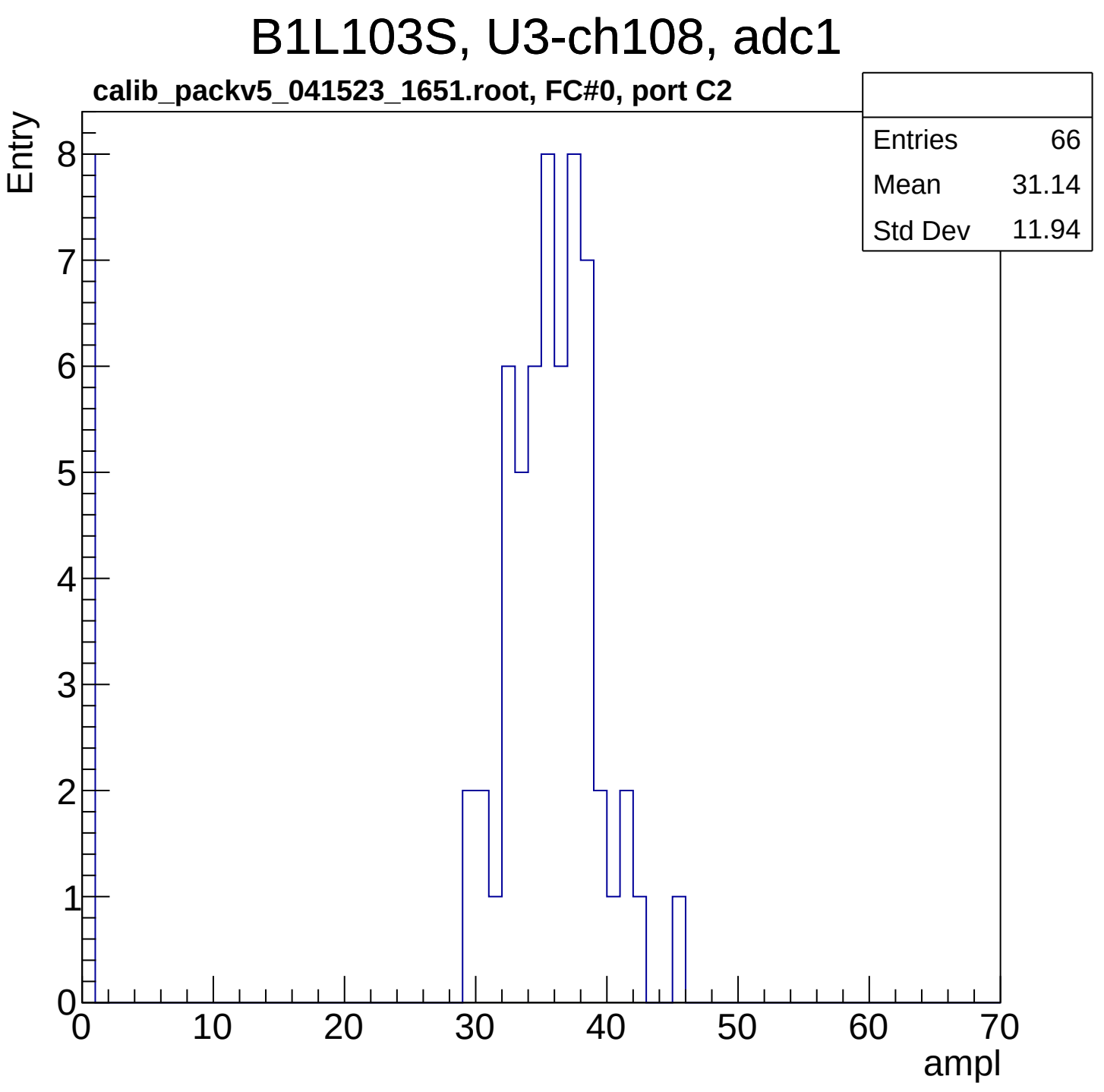
70
ampl


B1L103S, U3-ch108, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 31.14
Std Dev 11.94
Entry
ampl
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5
6
7
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0
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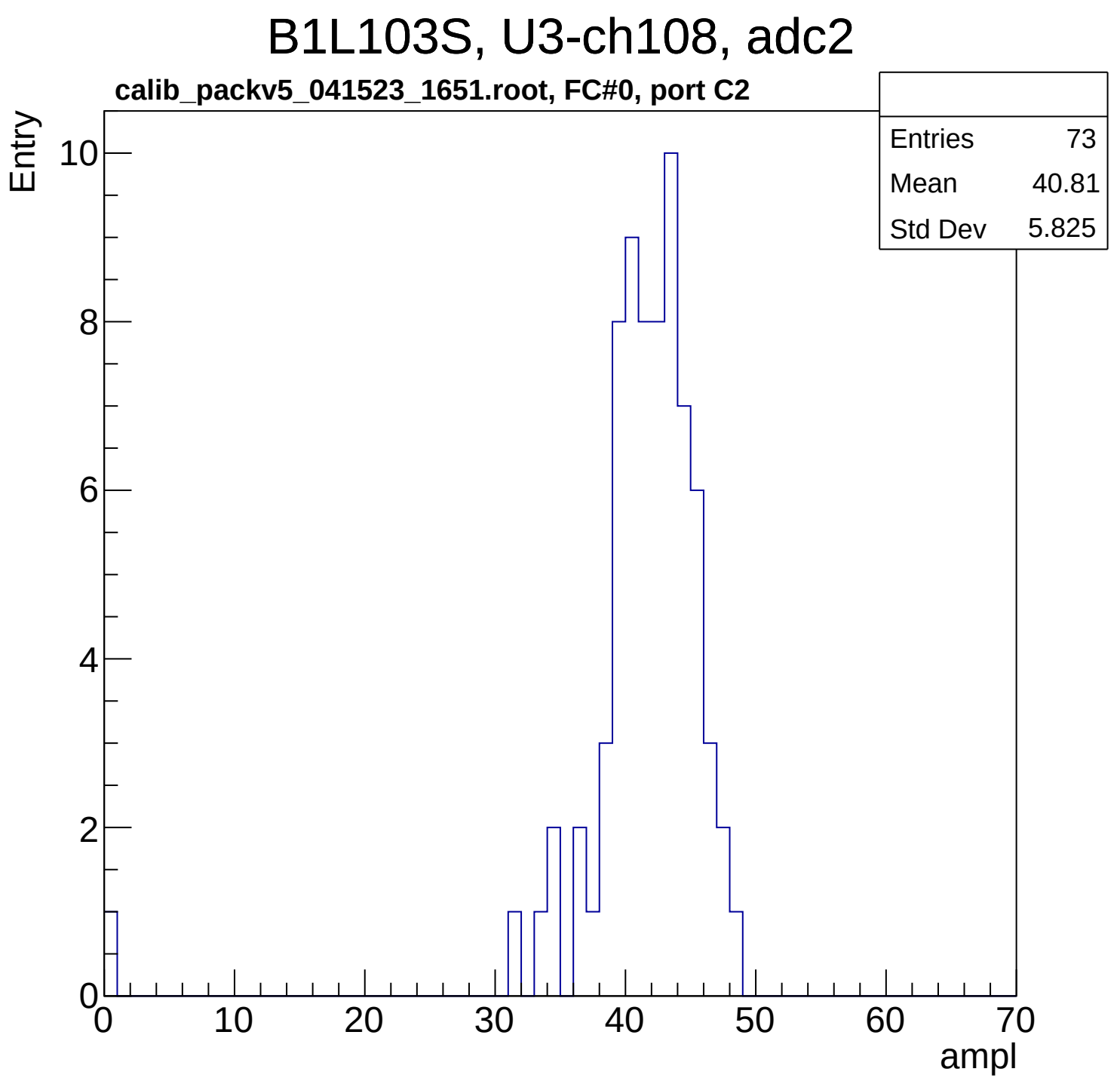
60
70


B1L103S, U3-ch108, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 40.81
Std Dev 5.825
Entry
ampl
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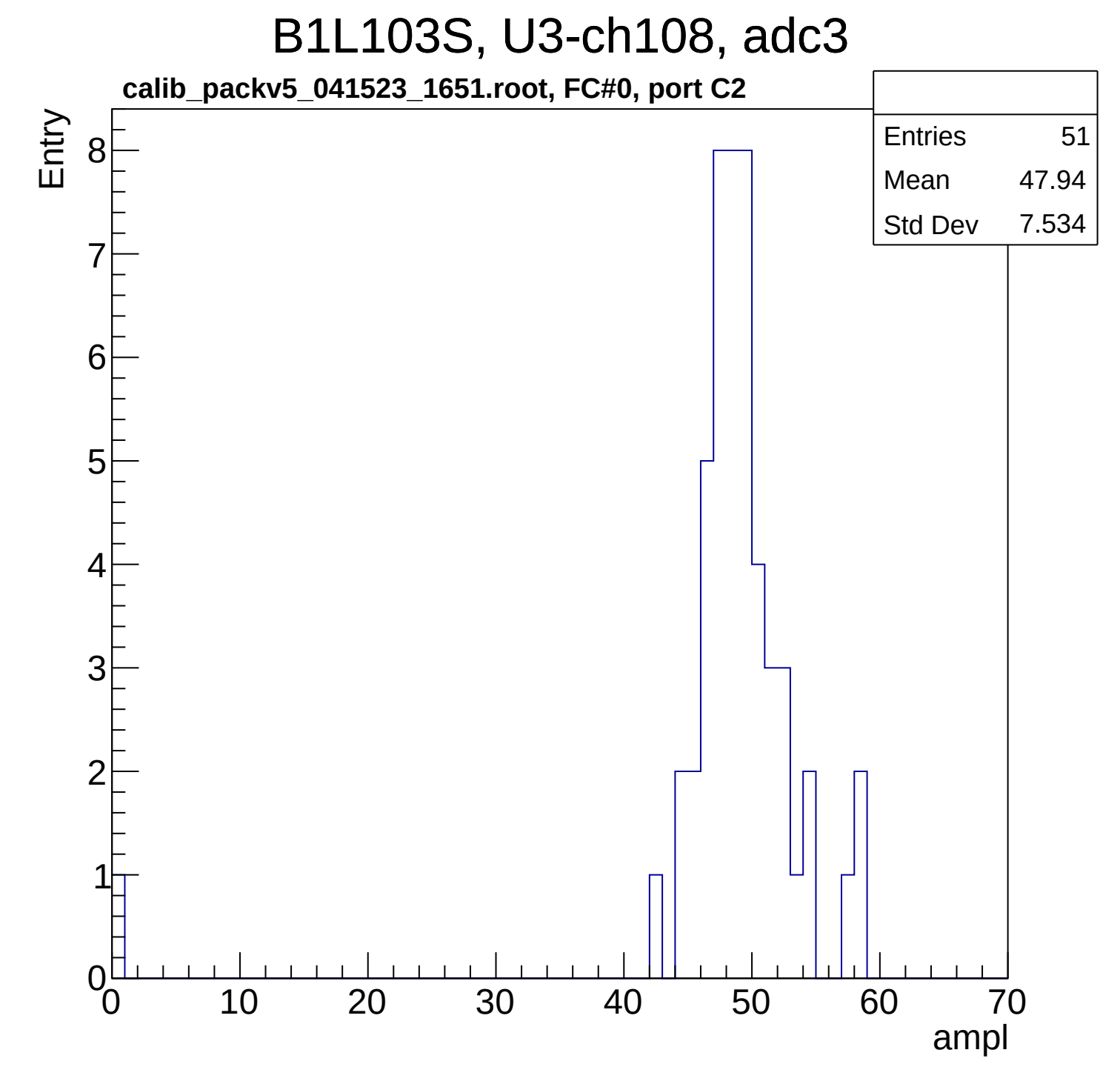
B1L103S, U3-ch108, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 47.94
Std Dev 7.534
Entry
ampl
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4
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6
7
8
0
10
20
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40
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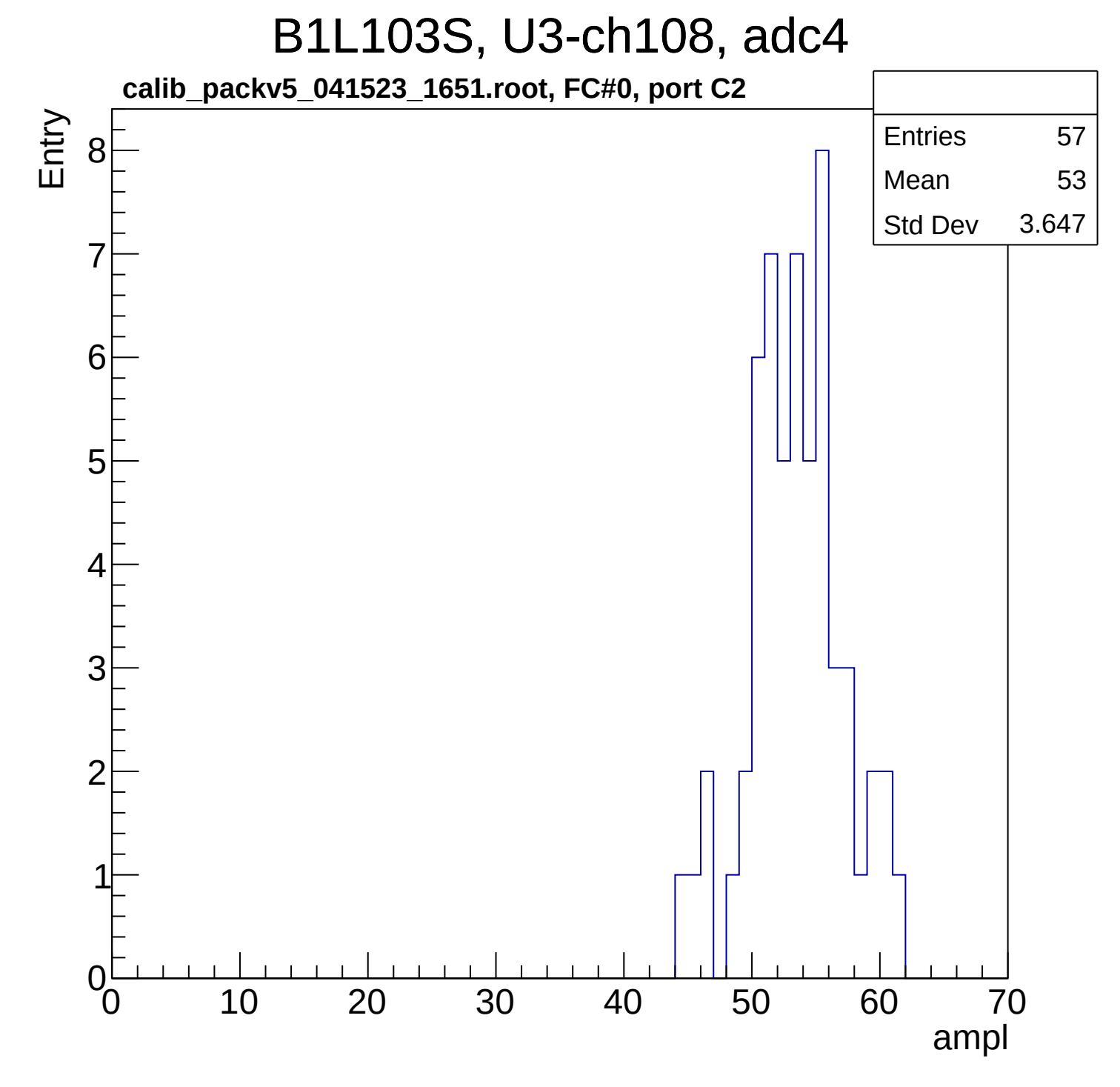
B1L103S, U3-ch108, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 53
Std Dev 3.647
Entry
ampl
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3
4
5
6
7
8
0
10
20
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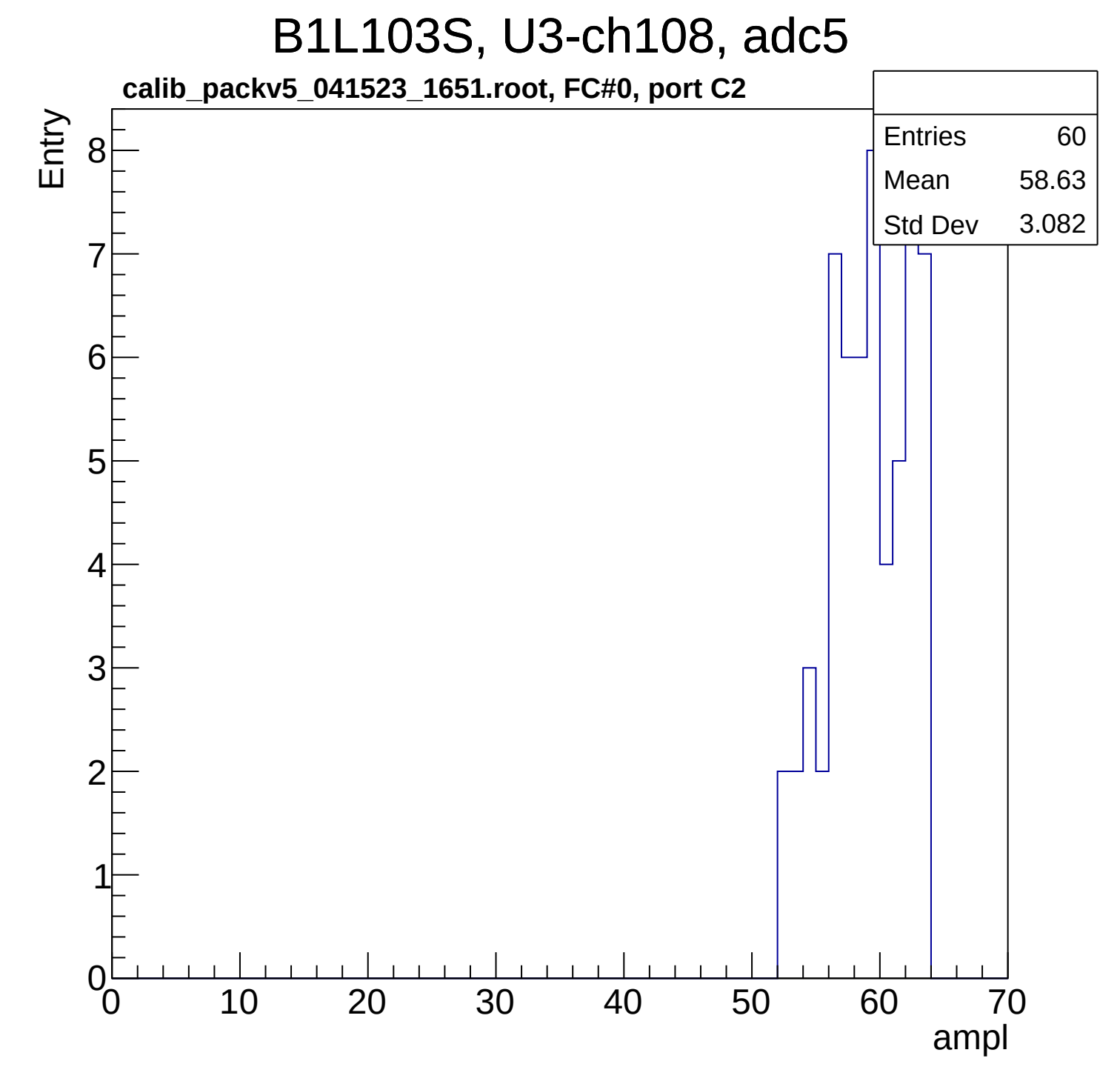
40
50
60
70


B1L103S, U3-ch108, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 58.63
Std Dev 3.082
Entry
ampl
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2
3
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5
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7
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0
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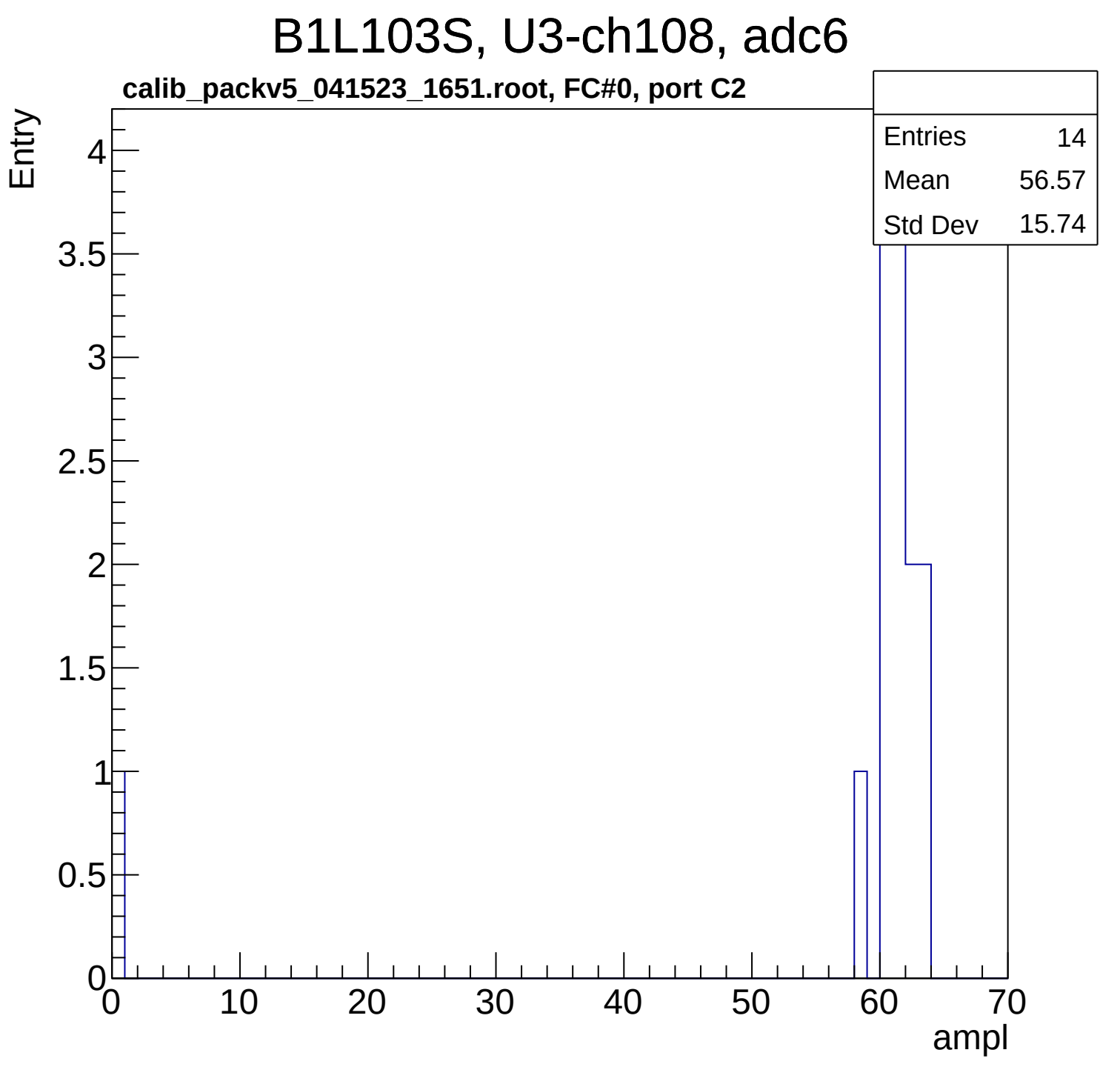
B1L103S, U3-ch108, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 56.57
Std Dev 15.74
Entry
ampl
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1.5
2
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3
3.5
4
0
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40
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60
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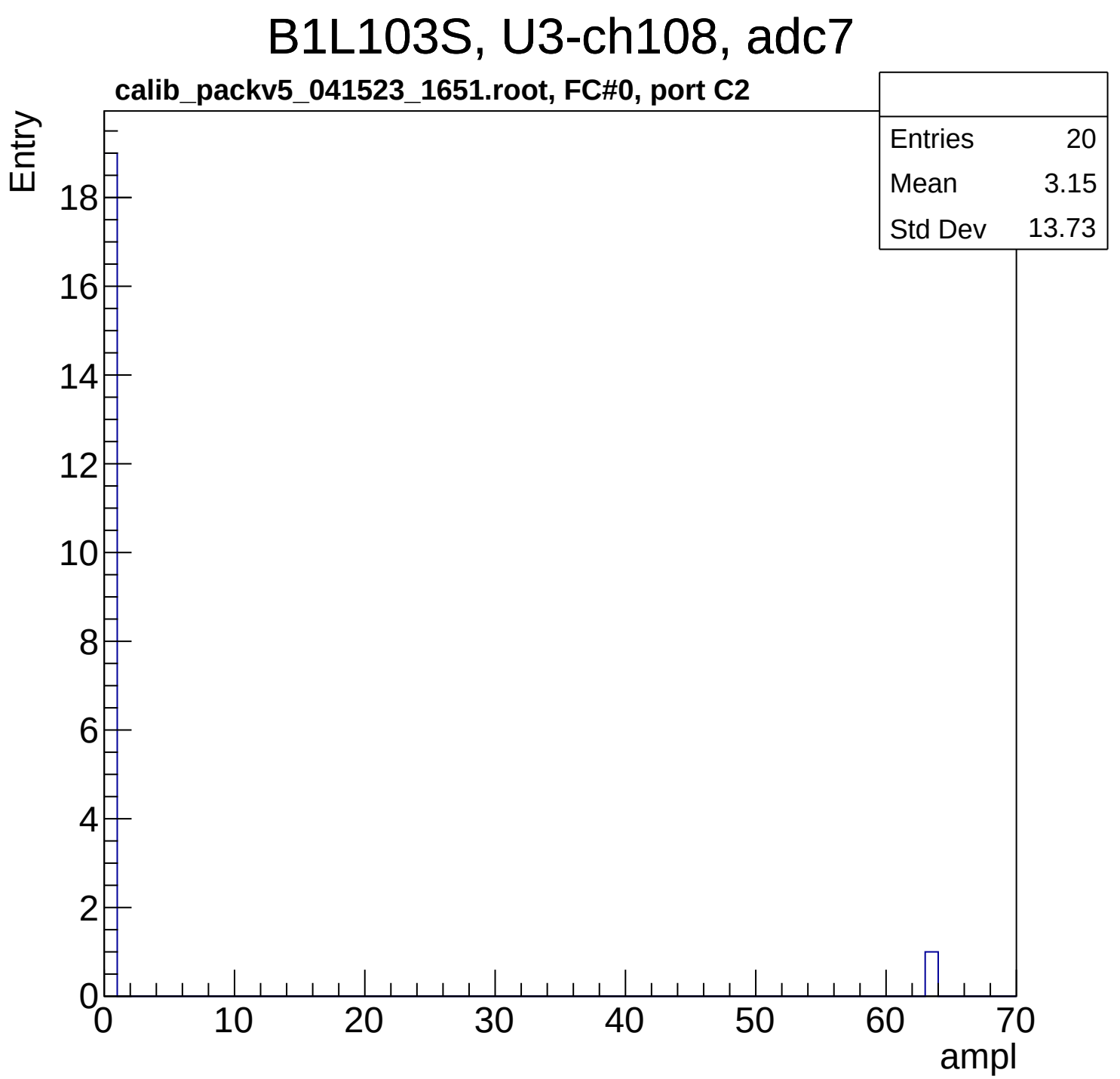
B1L103S, U3-ch108, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
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6
8
10
12
14
16
18
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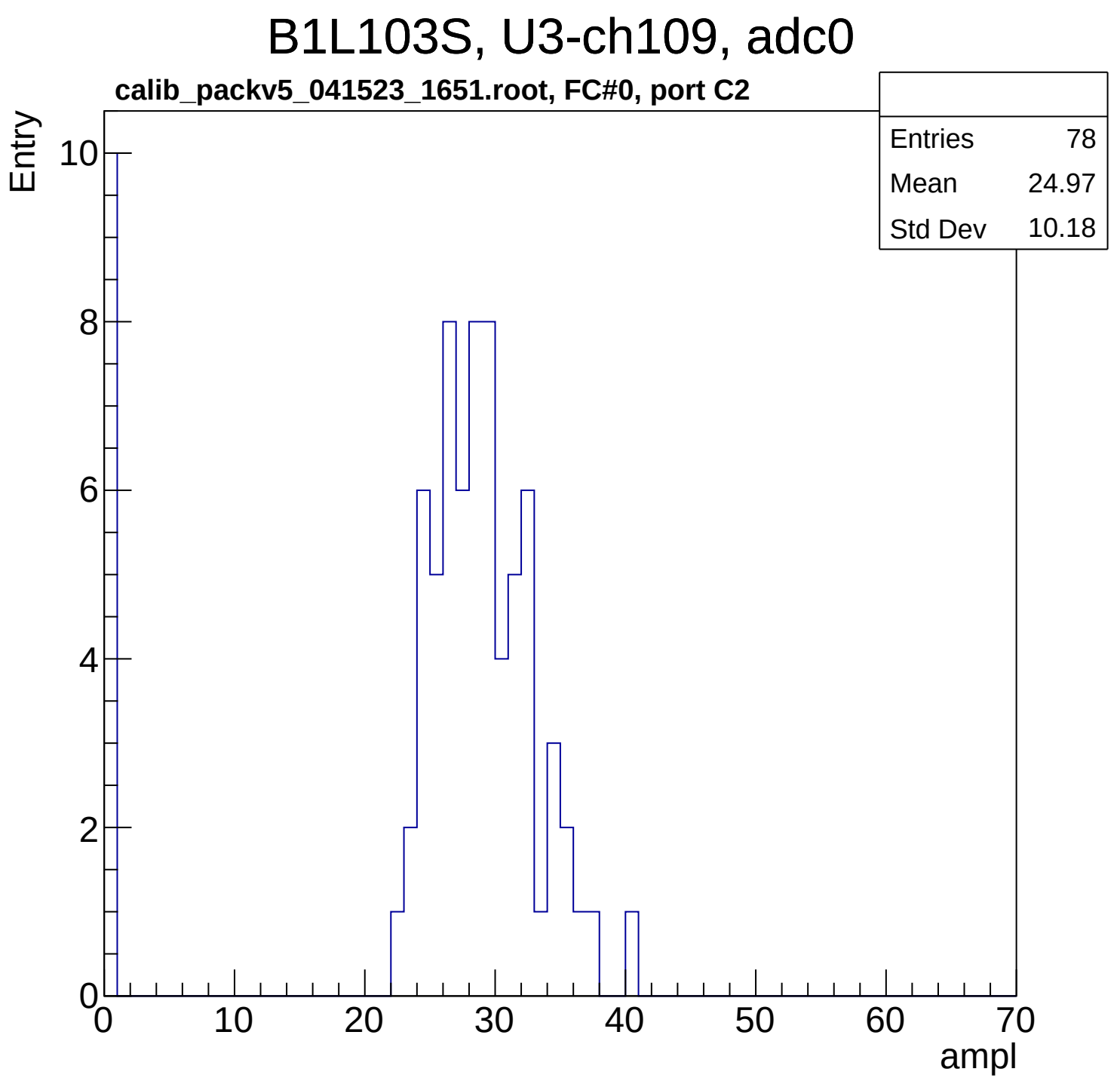
50
60
70
ampl


B1L103S, U3-ch109, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 24.97
Std Dev 10.18
Entry
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8
10
0
10
20
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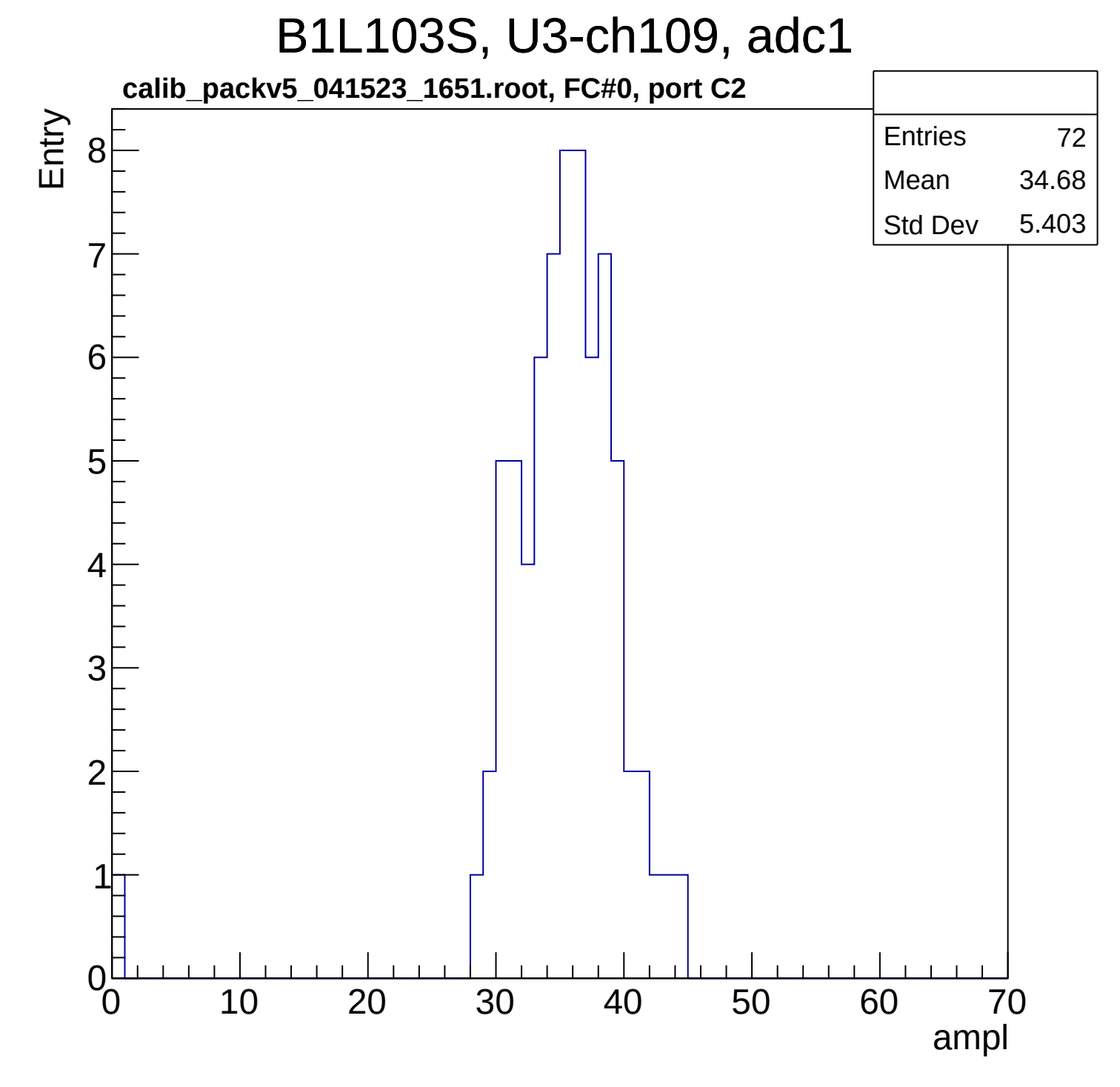
50
60
70
ampl


B1L103S, U3-ch109, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 34.68
Std Dev 5.403
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
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60
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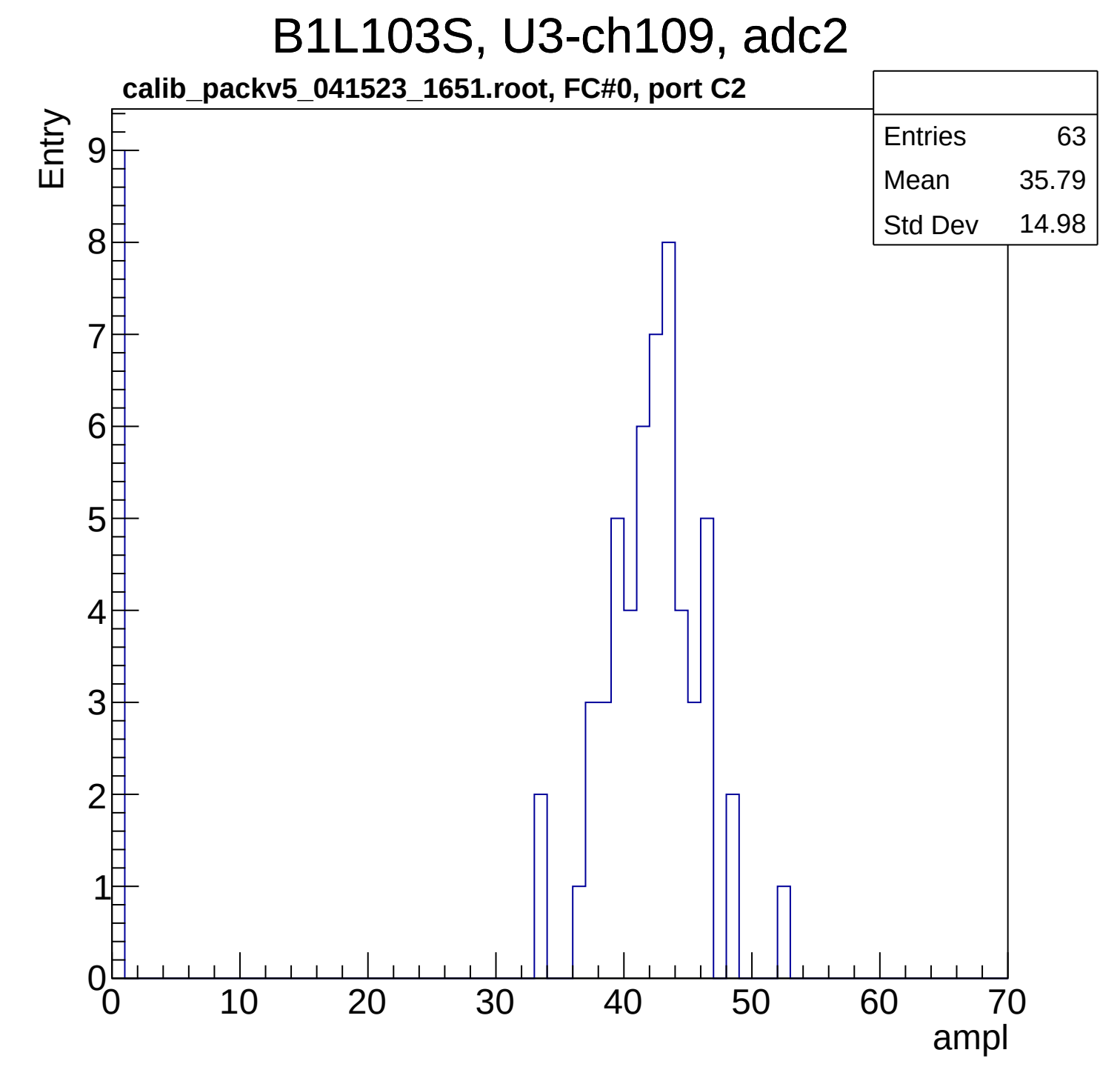
B1L103S, U3-ch109, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 35.79
Std Dev 14.98
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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40
50
60
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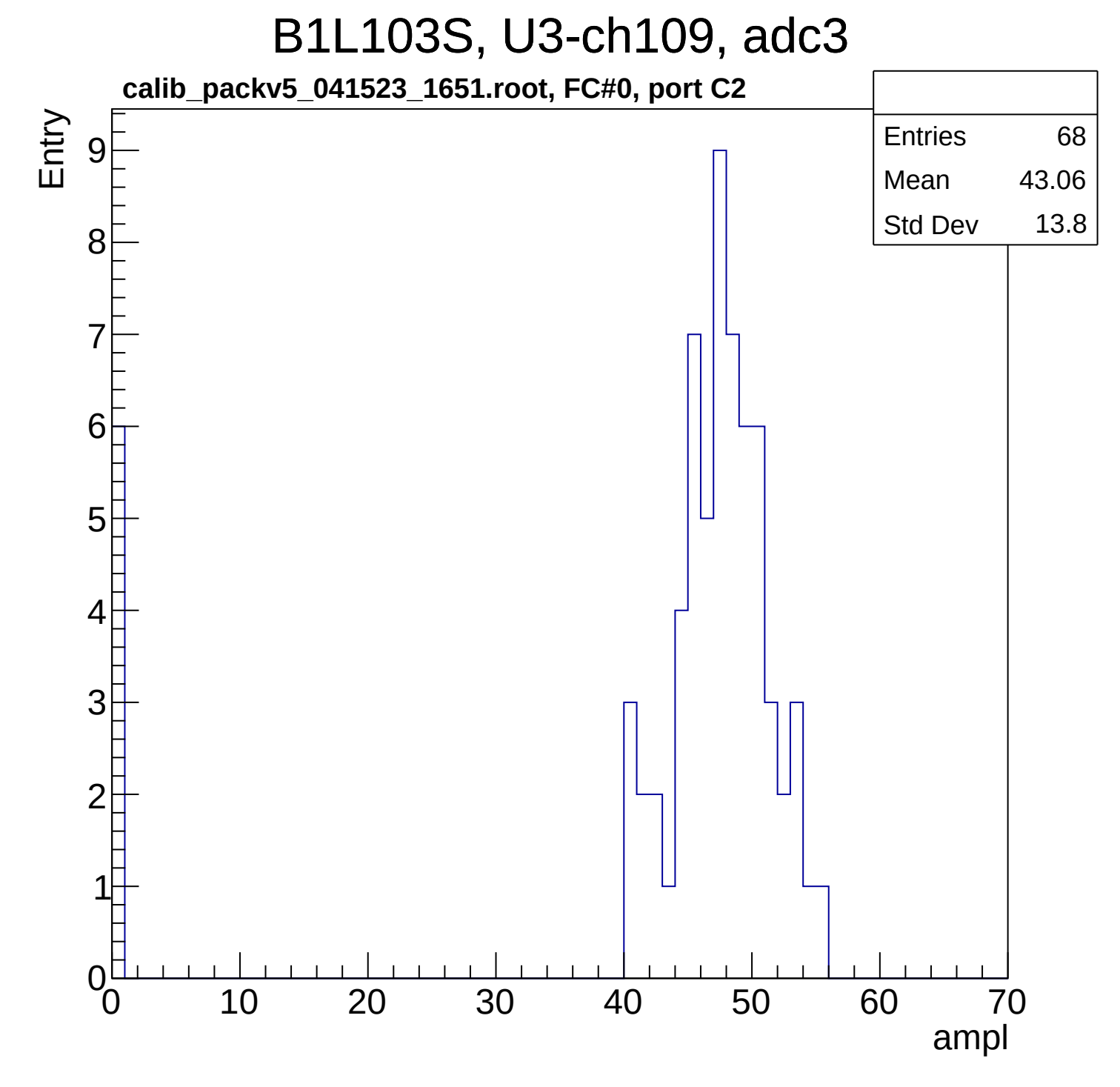
B1L103S, U3-ch109, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 43.06
Std Dev 13.8
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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40
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60
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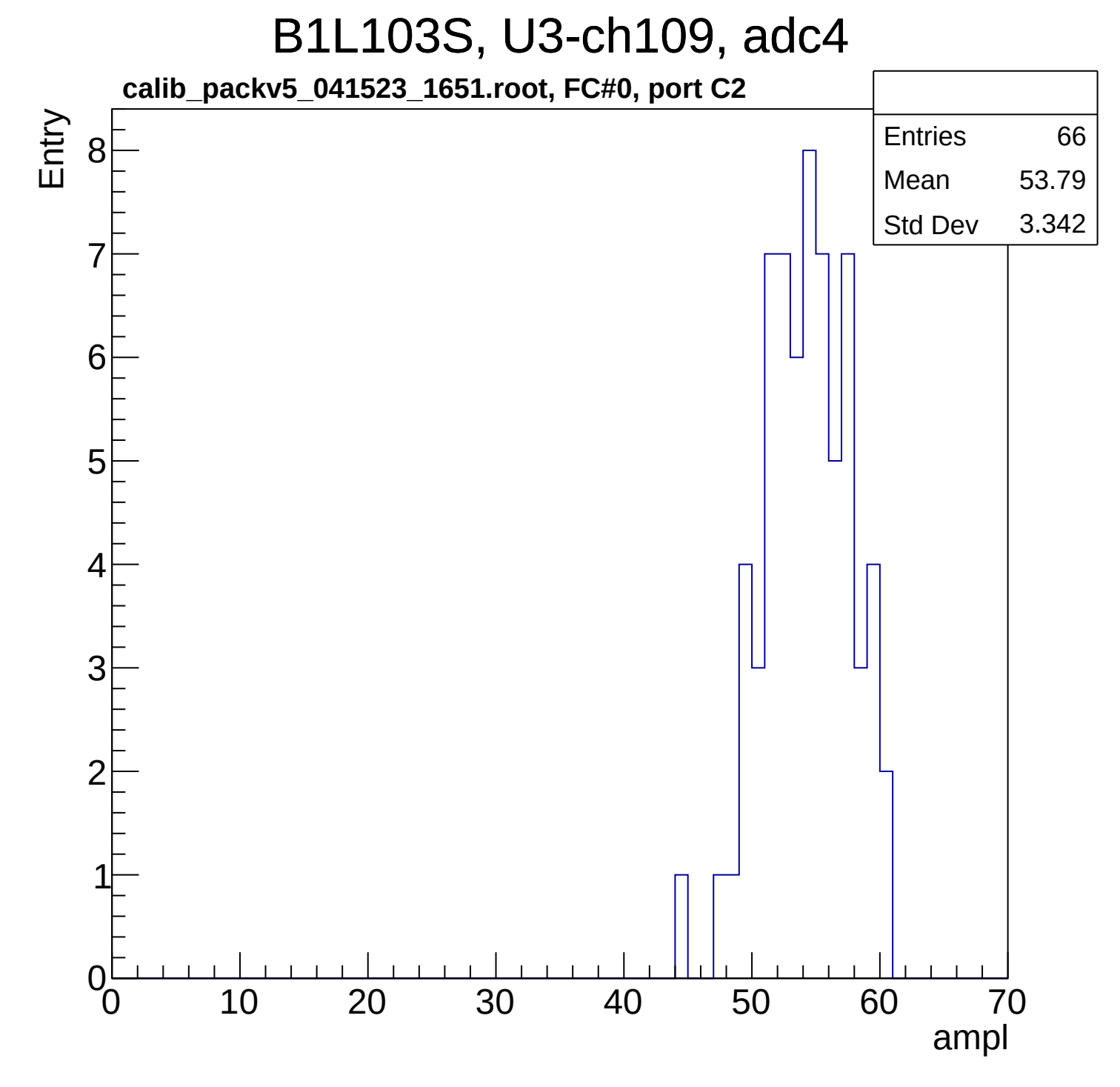
B1L103S, U3-ch109, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 53.79
Std Dev 3.342
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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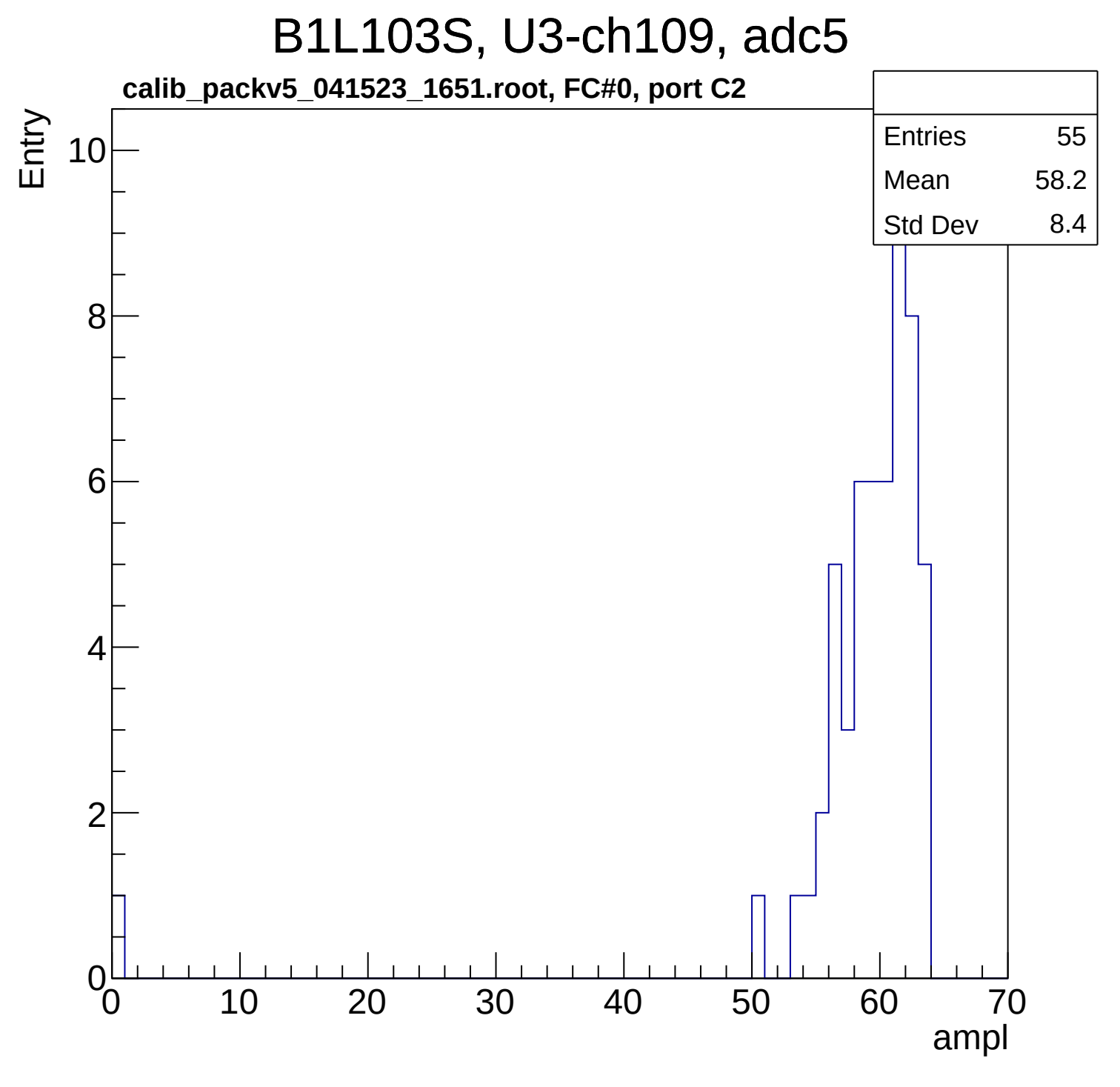
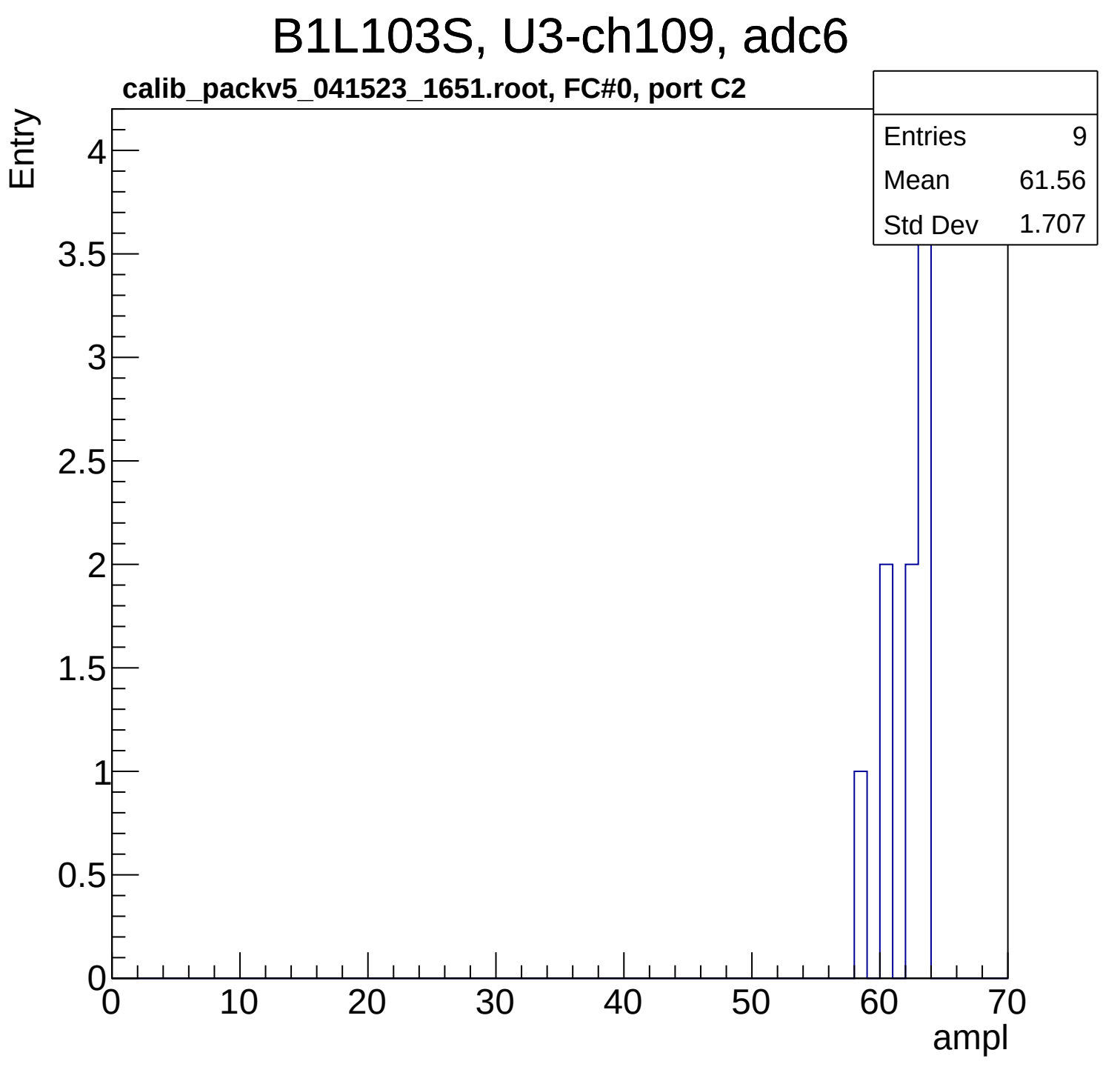

B1L103S, U3-ch109, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 58.2
Std Dev 8.4
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch109, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 61.56
Std Dev 1.707
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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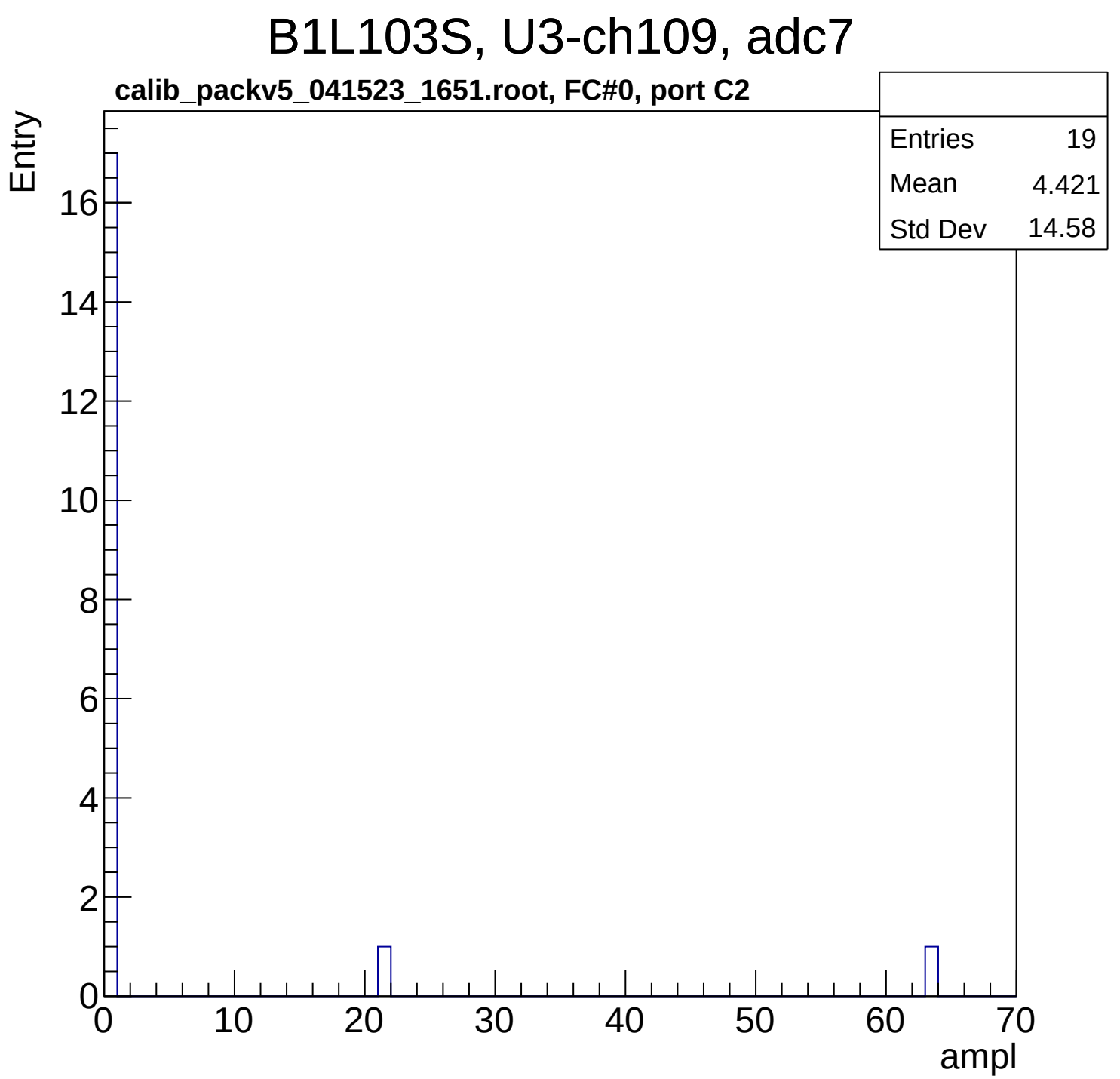
B1L103S, U3-ch109, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 4.421
Std Dev 14.58
Entry
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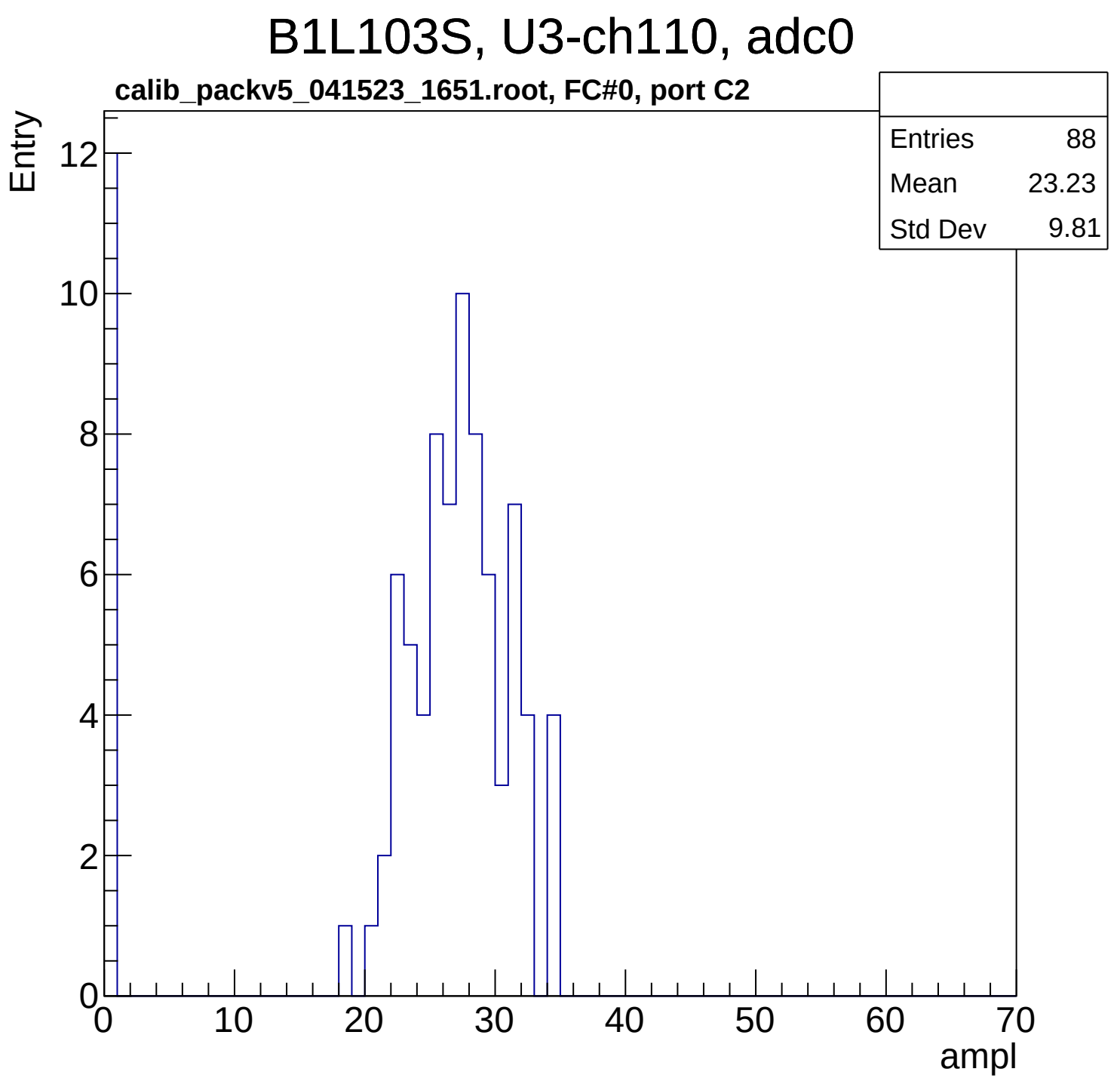
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch110, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 23.23
Std Dev 9.81
Entry
ampl
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2
4
6
8
10
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0
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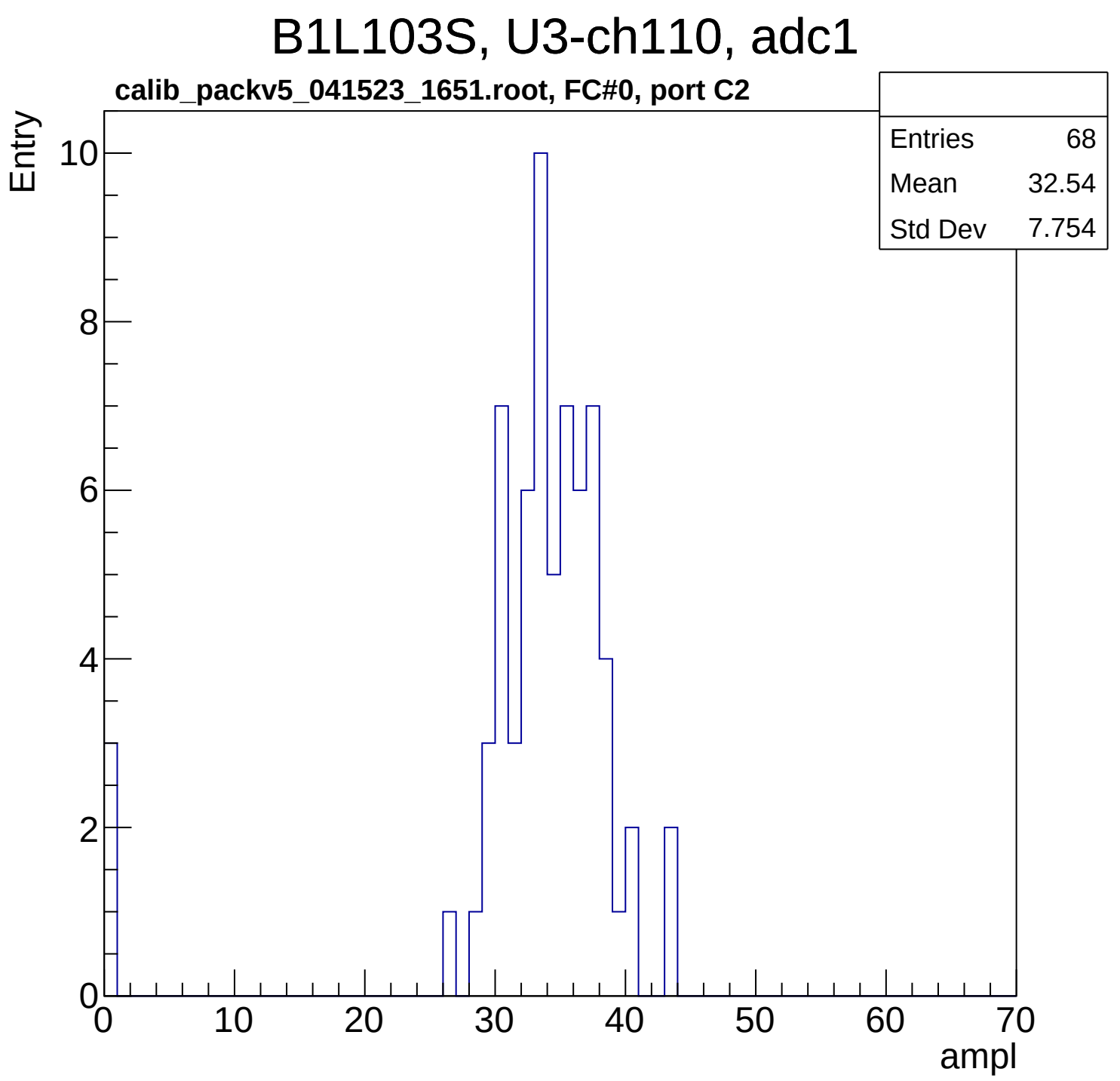
20
30
40
50
60
70


B1L103S, U3-ch110, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 32.54
Std Dev 7.754
Entry
ampl
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2
4
6
8
10
0
10
20
30
40
50
60
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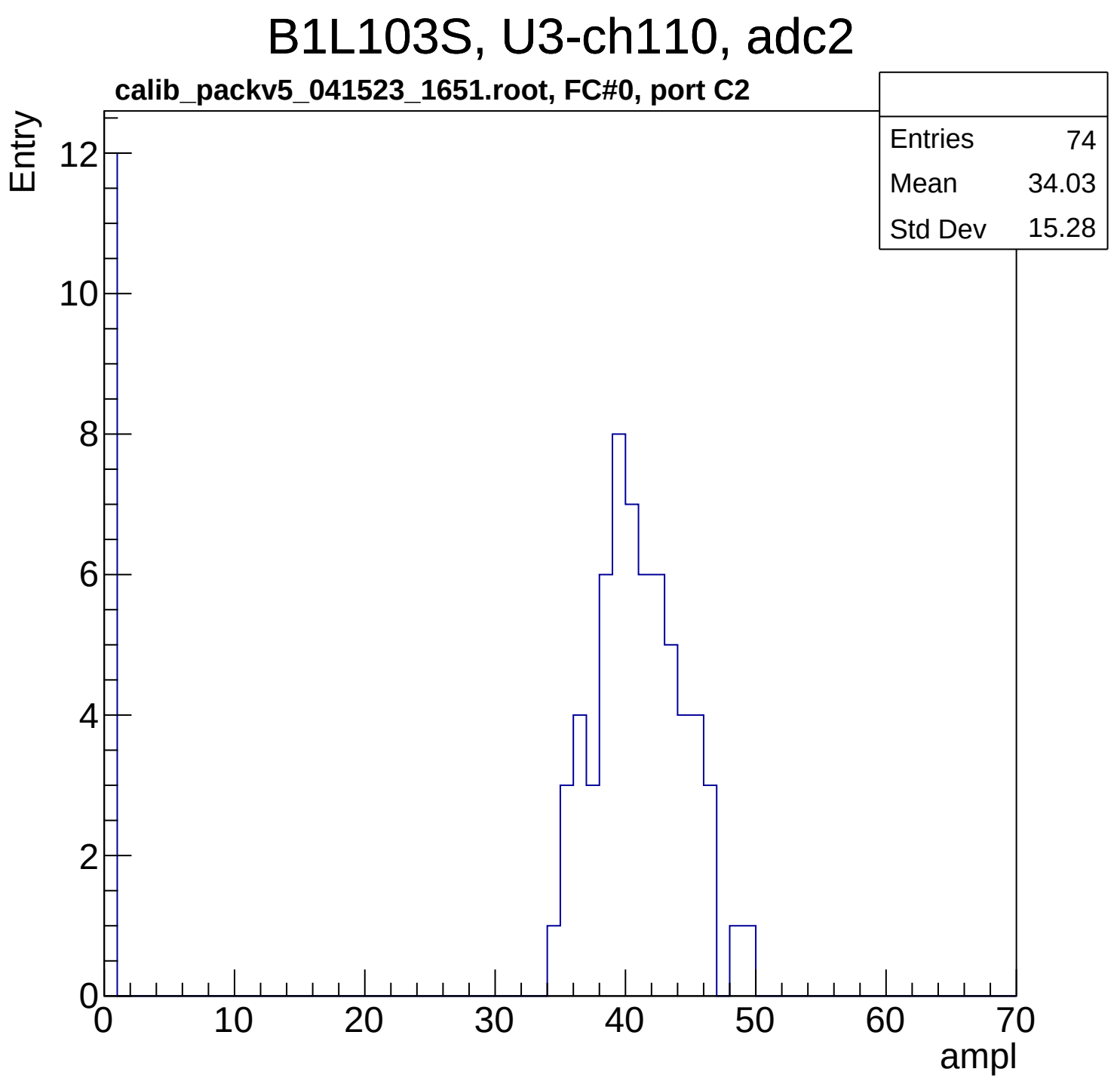
B1L103S, U3-ch110, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 34.03
Std Dev 15.28
Entry
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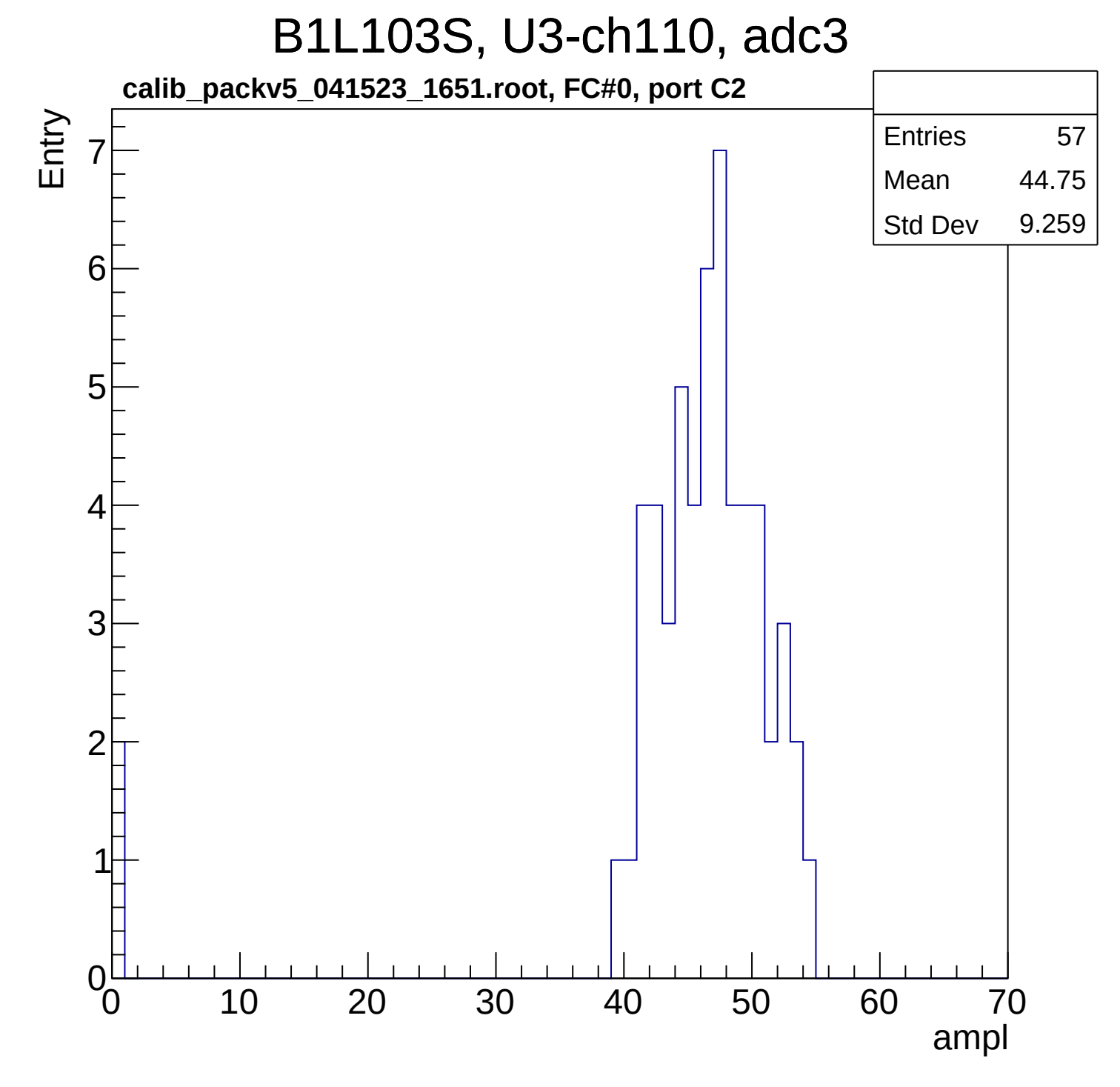
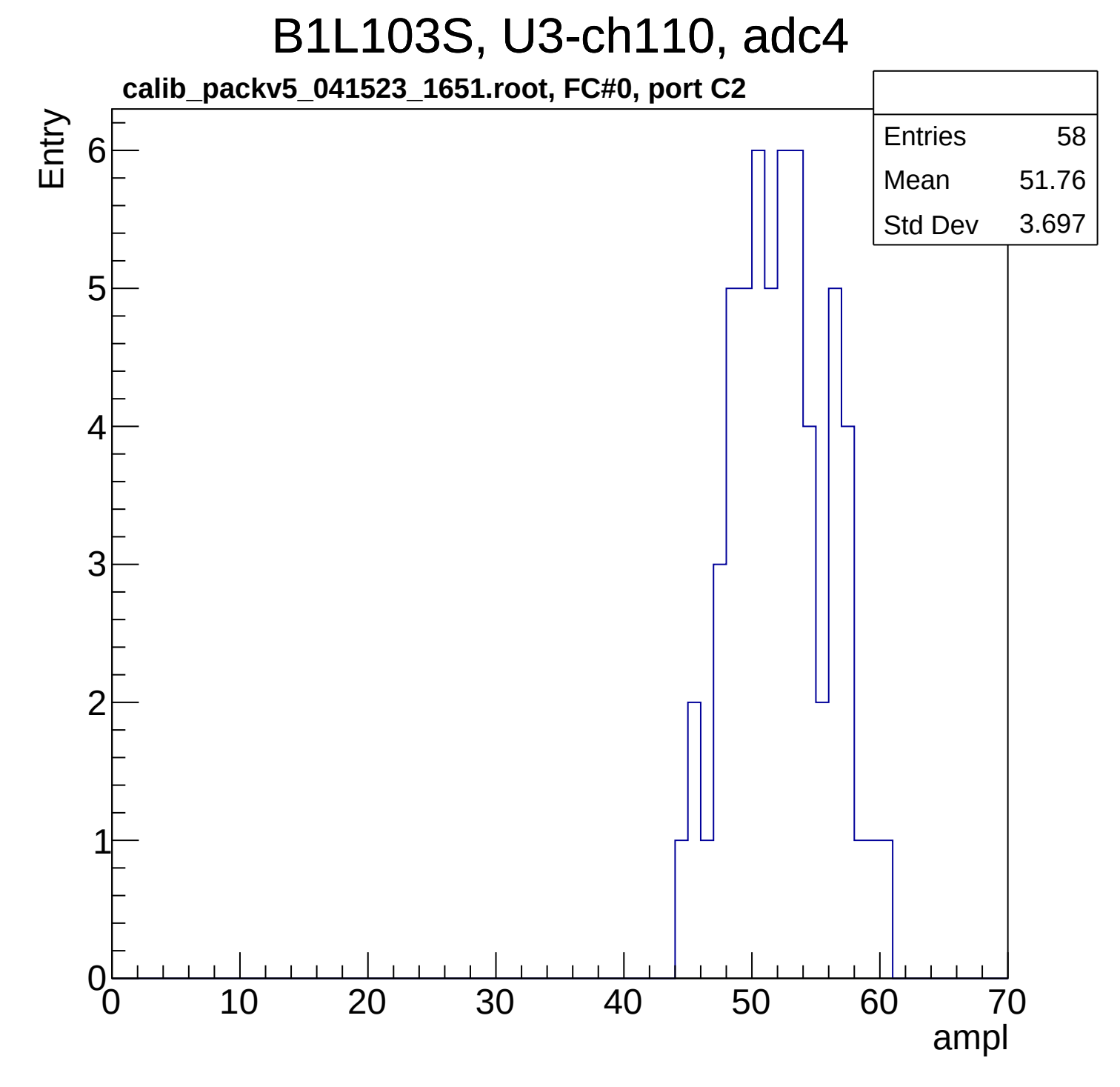
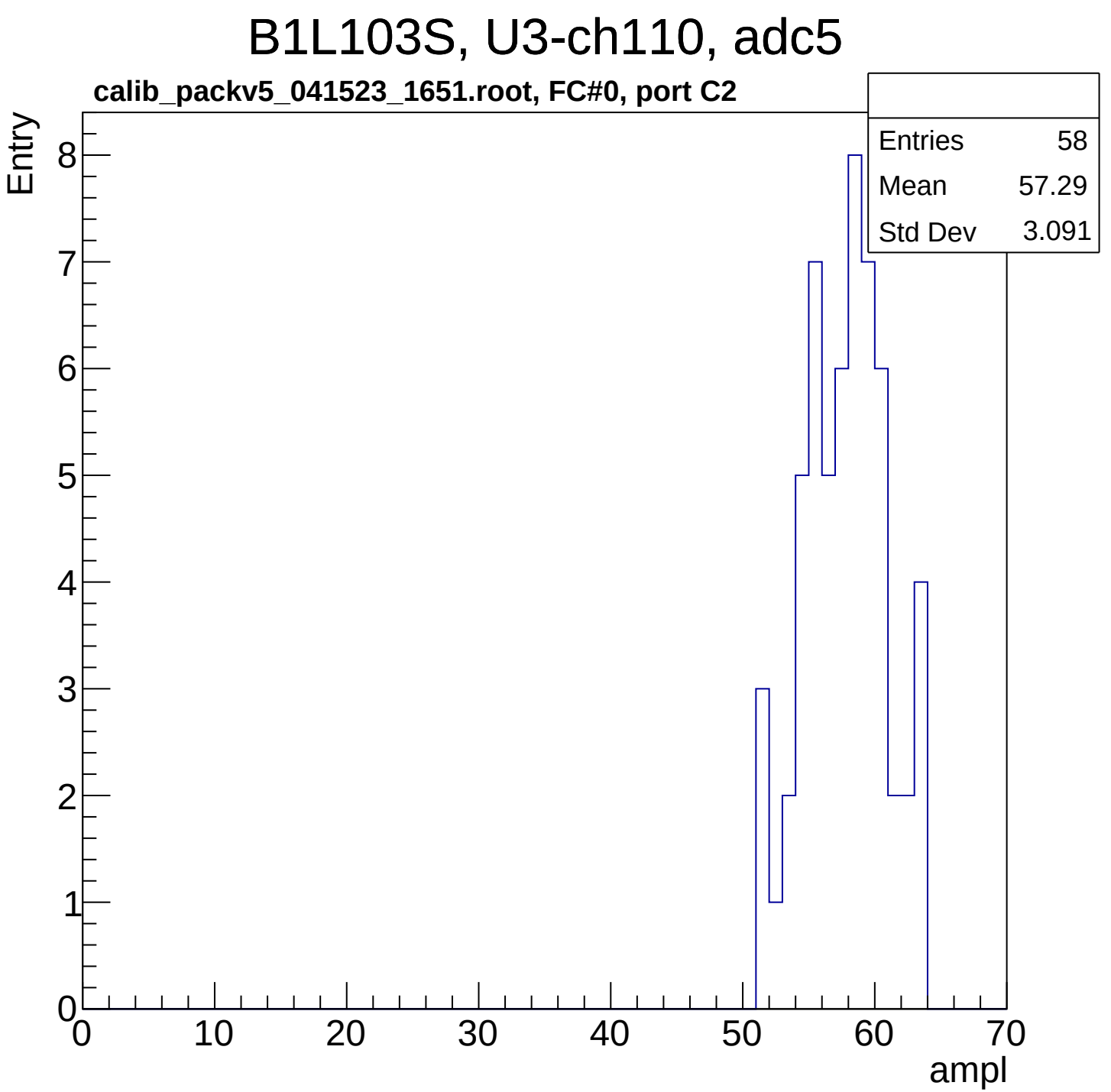
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch110, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 44.75
Std Dev 9.259
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch110, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 51.76
Std Dev 3.697
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U3-ch110, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 57.29
Std Dev 3.091
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
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60
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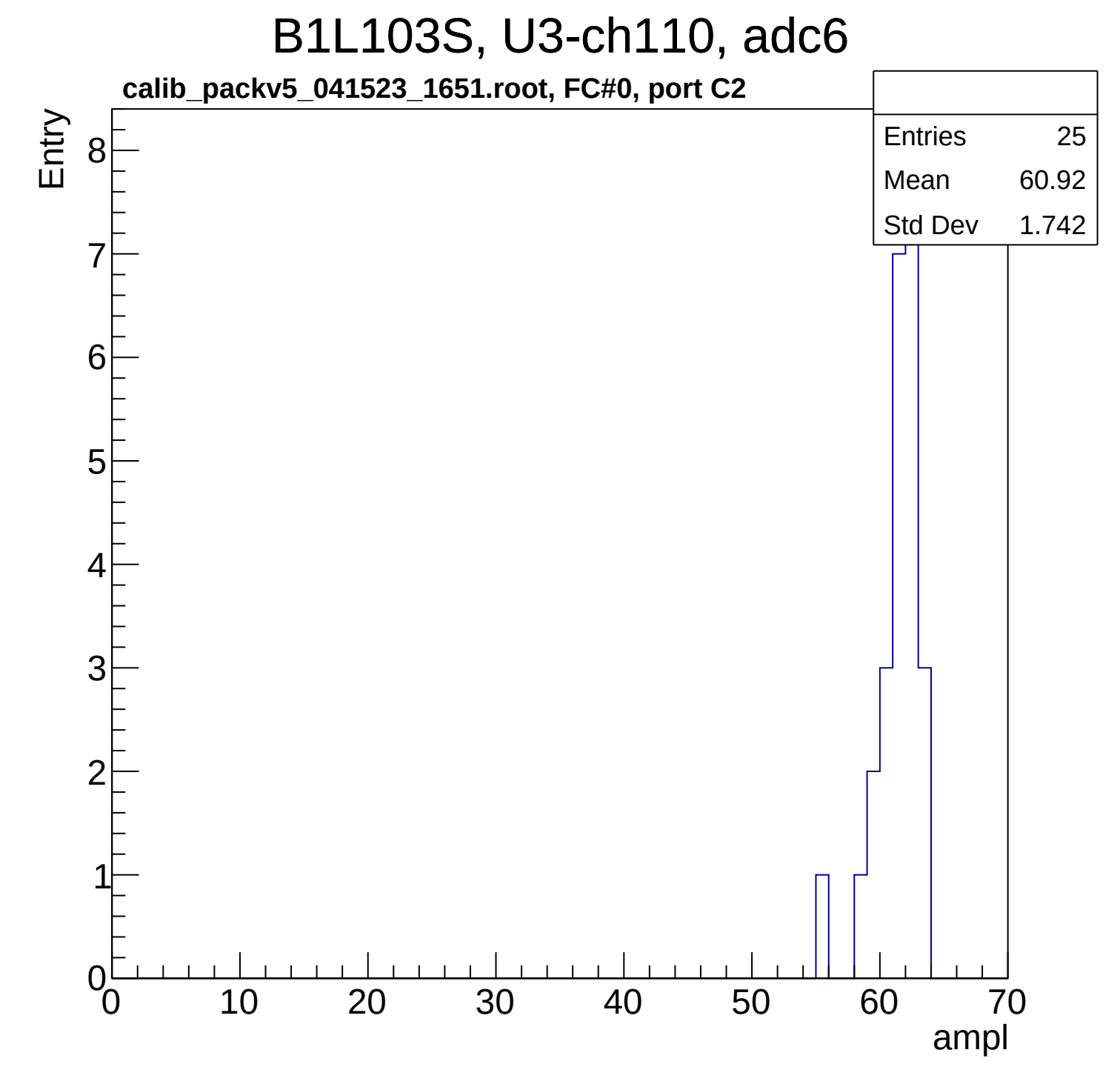
B1L103S, U3-ch110, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 60.92
Std Dev 1.742
Entry
ampl
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4
5
6
7
8
0
10
20
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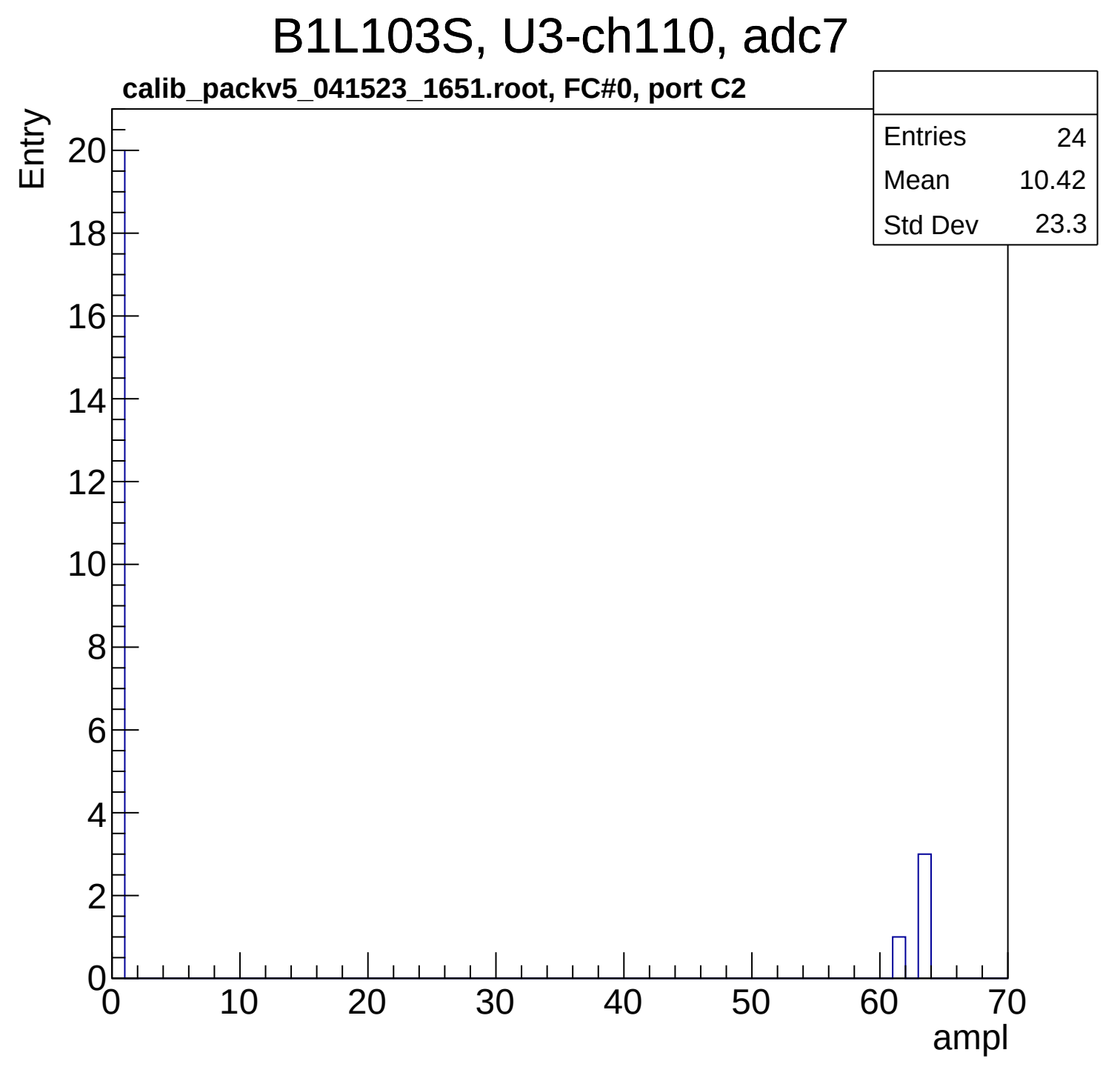
40
50
60
70


B1L103S, U3-ch110, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 10.42
Std Dev 23.3
Entry
ampl
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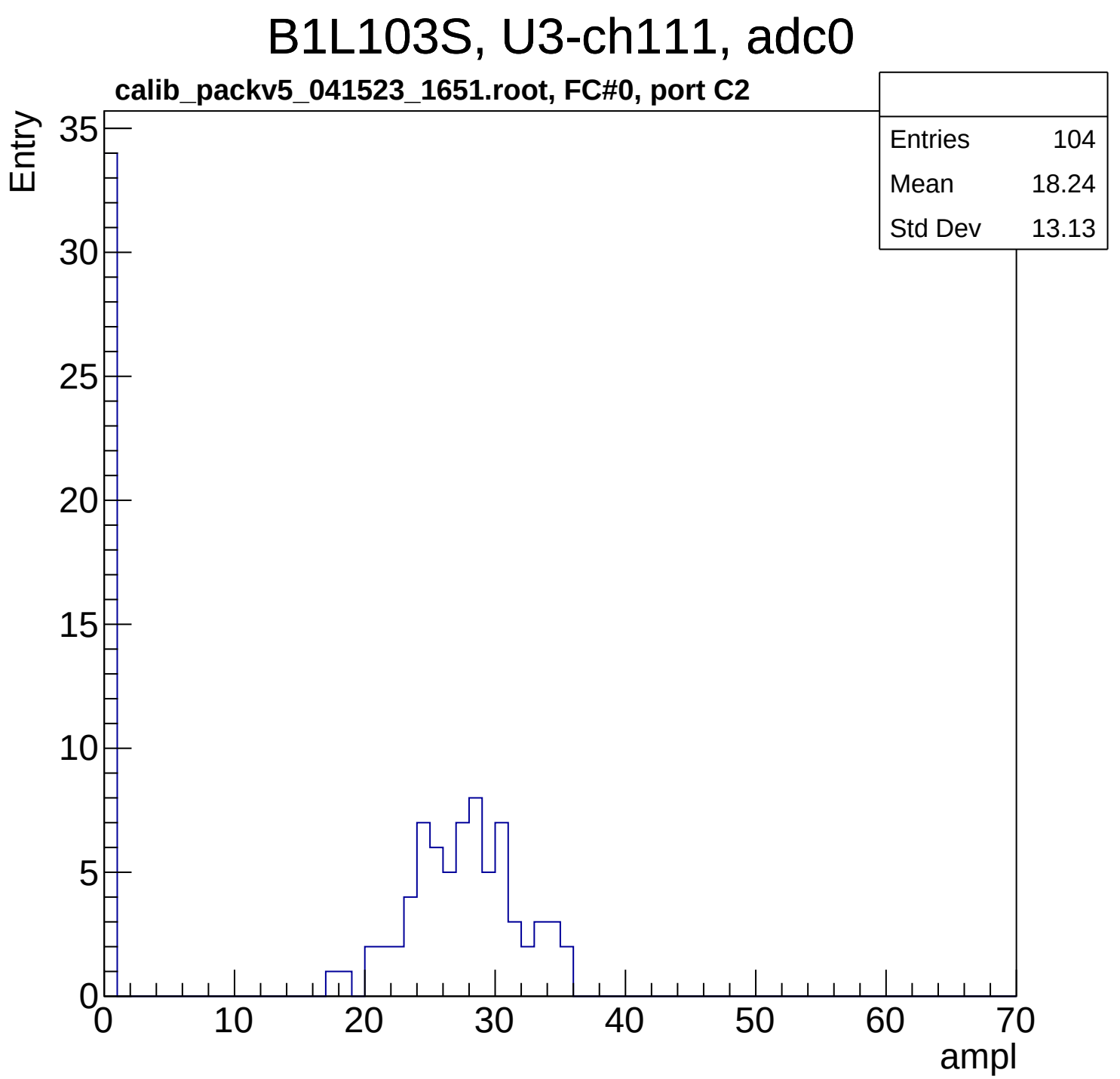
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70


B1L103S, U3-ch111, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 104
Mean 18.24
Std Dev 13.13
Entry
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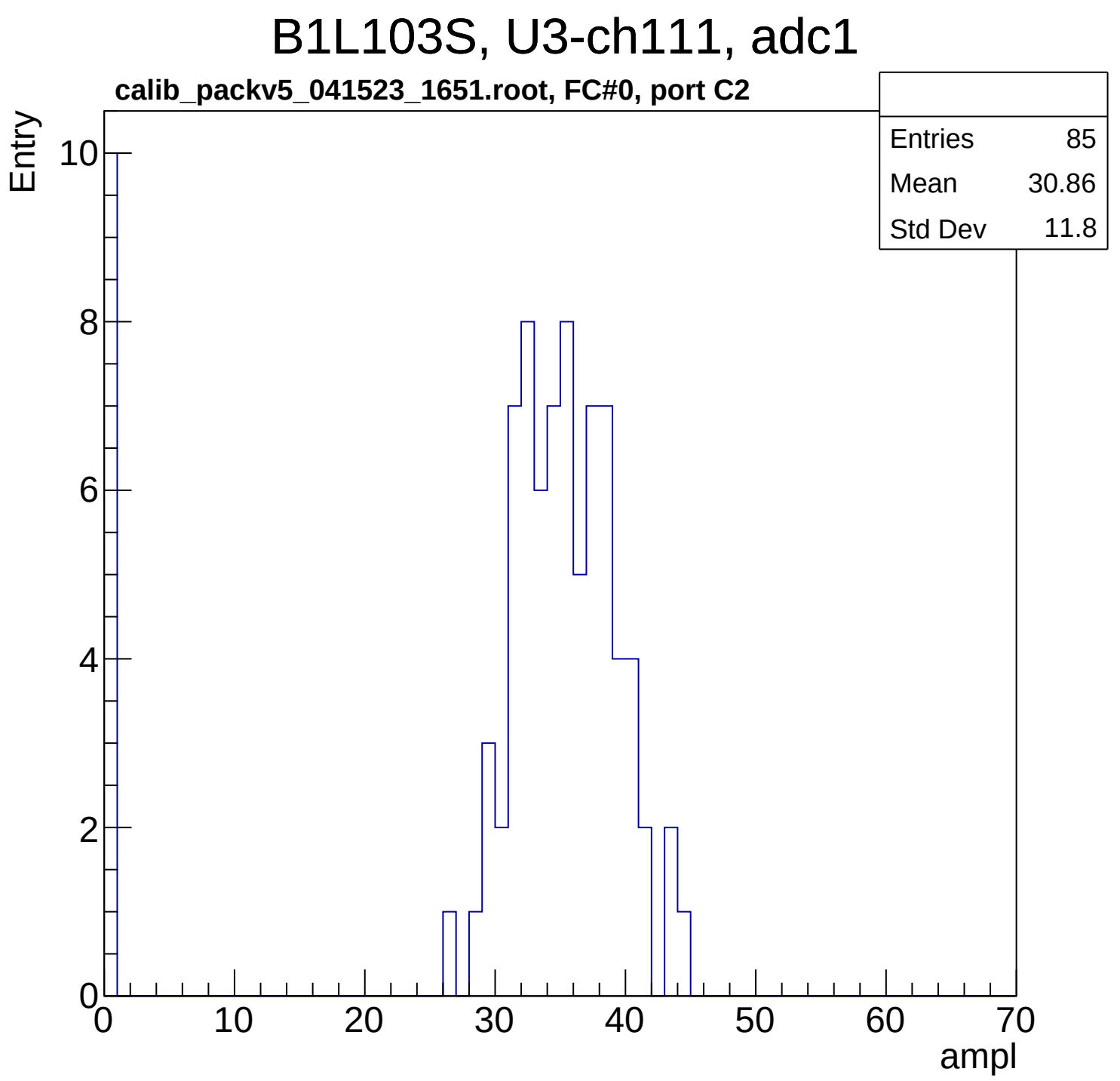
5
10
15
20
25
30
35
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch111, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 30.86
Std Dev 11.8
Entry
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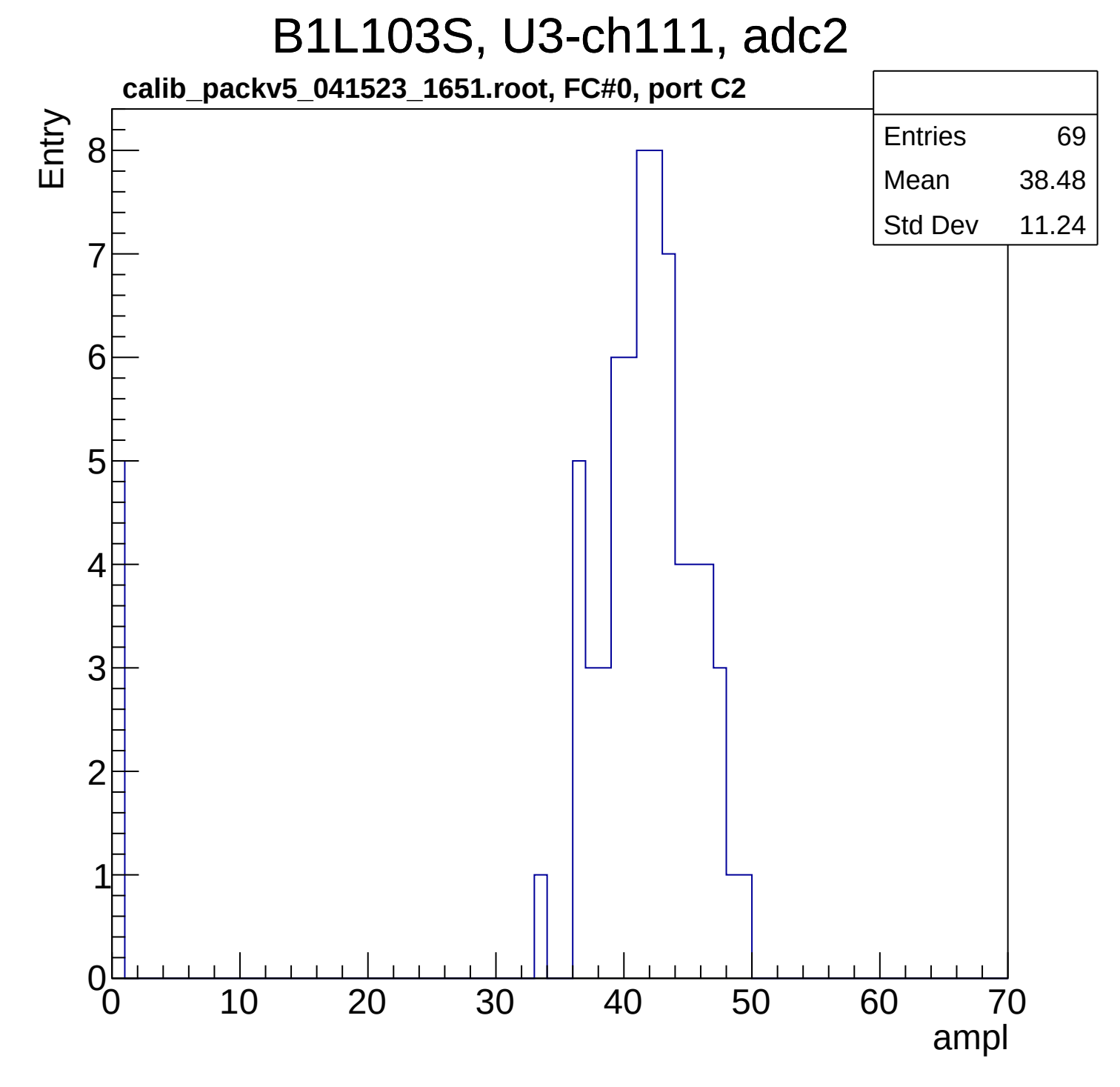
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch111, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 38.48
Std Dev 11.24
Entry
ampl
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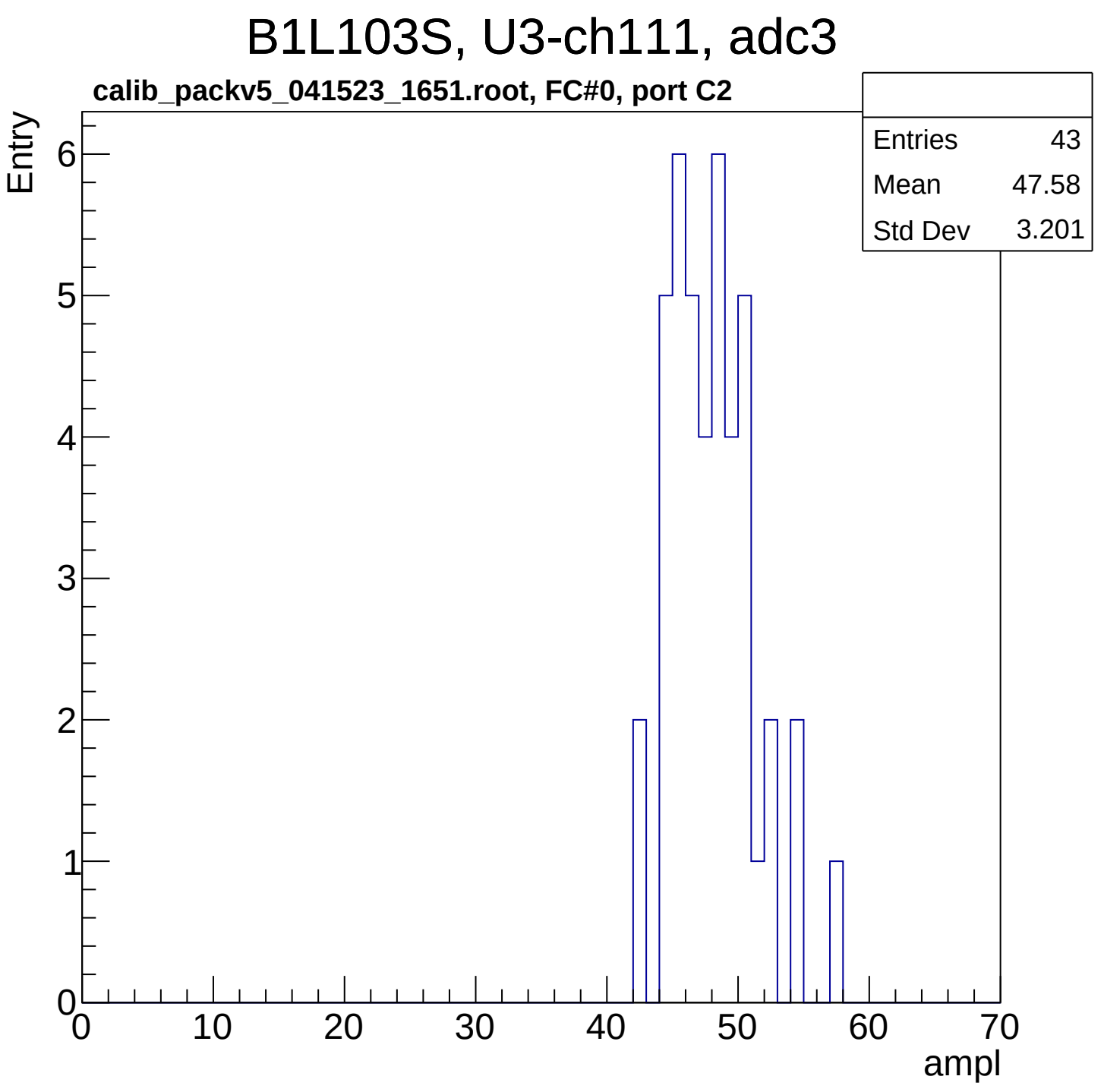
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch111, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 47.58
Std Dev 3.201
Entry
ampl
0
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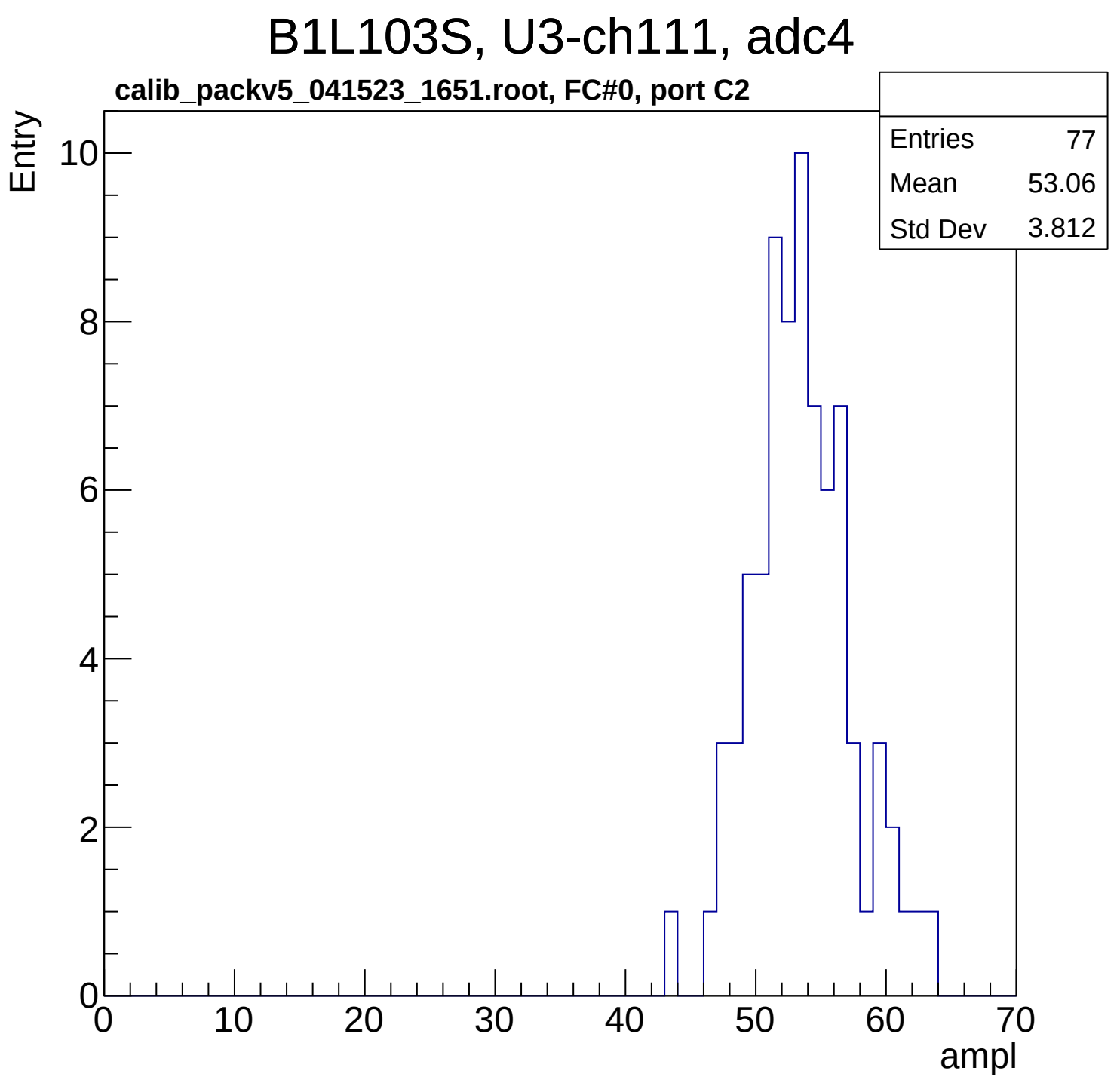
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U3-ch111, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 53.06
Std Dev 3.812
Entry
ampl
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4
6
8
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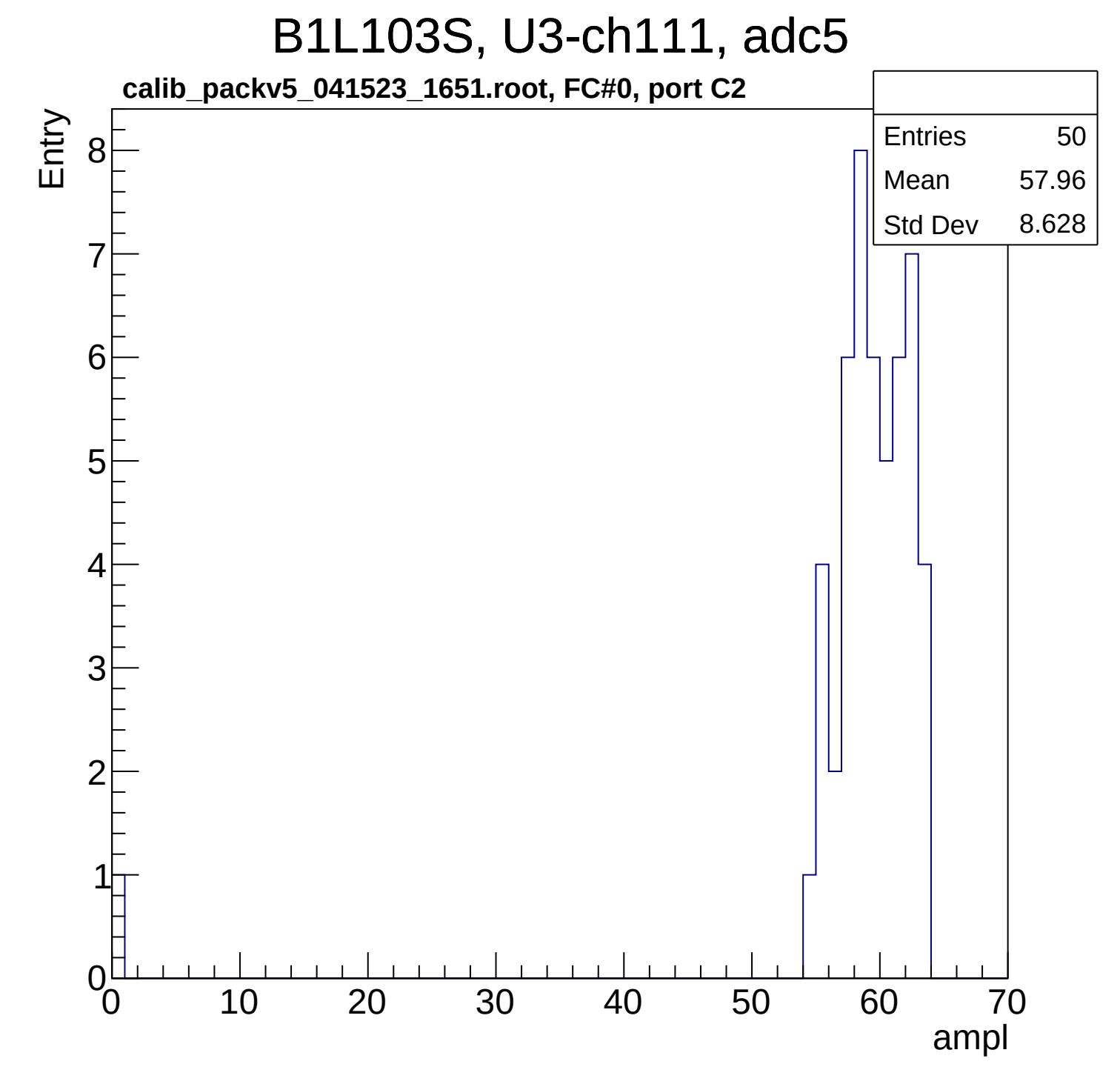
0
10
20
30
40
50
60
70


B1L103S, U3-ch111, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 57.96
Std Dev 8.628
Entry
ampl
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2
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4
5
6
7
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0
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60
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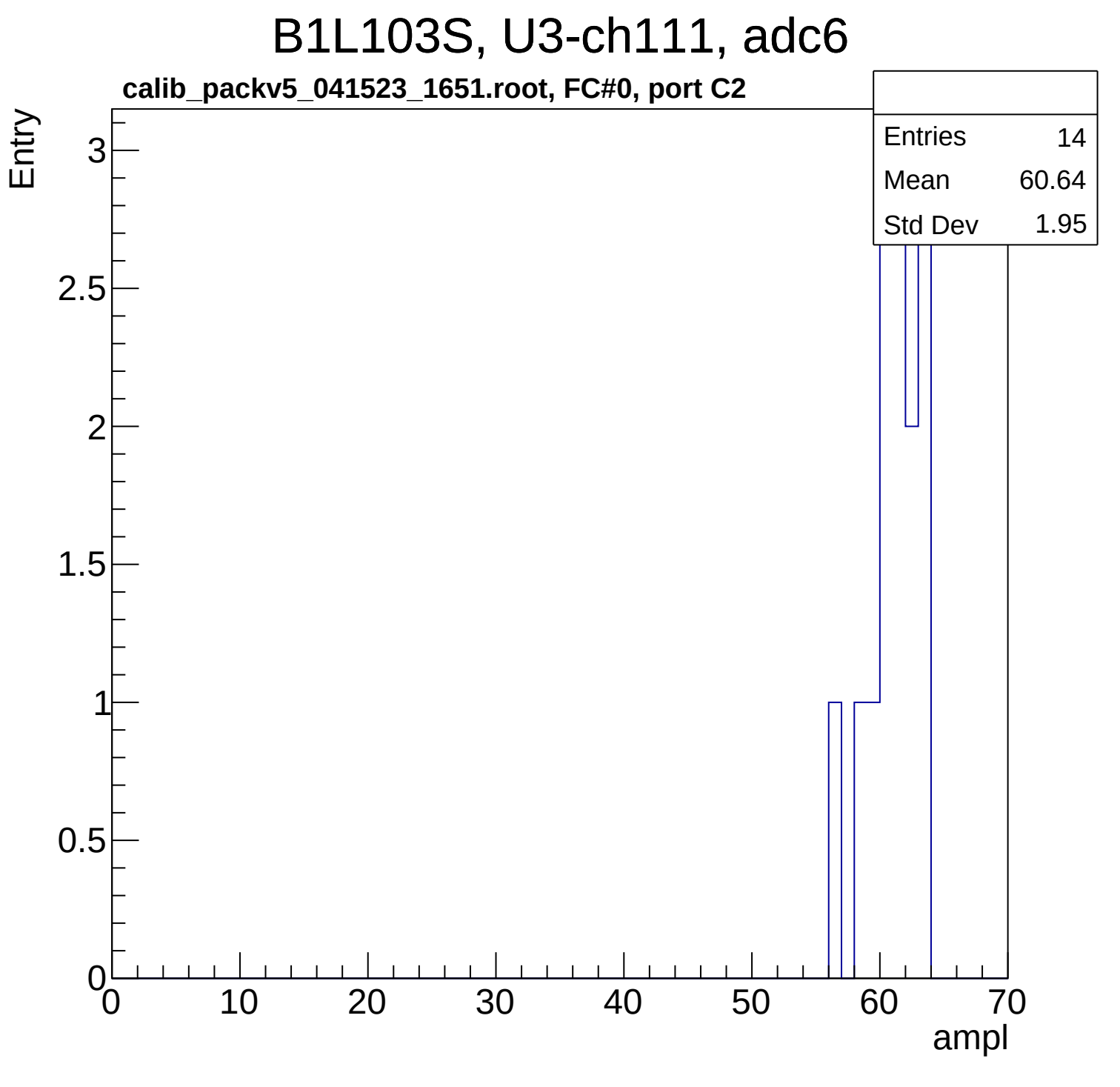
B1L103S, U3-ch111, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 60.64
Std Dev 1.95
Entry
ampl
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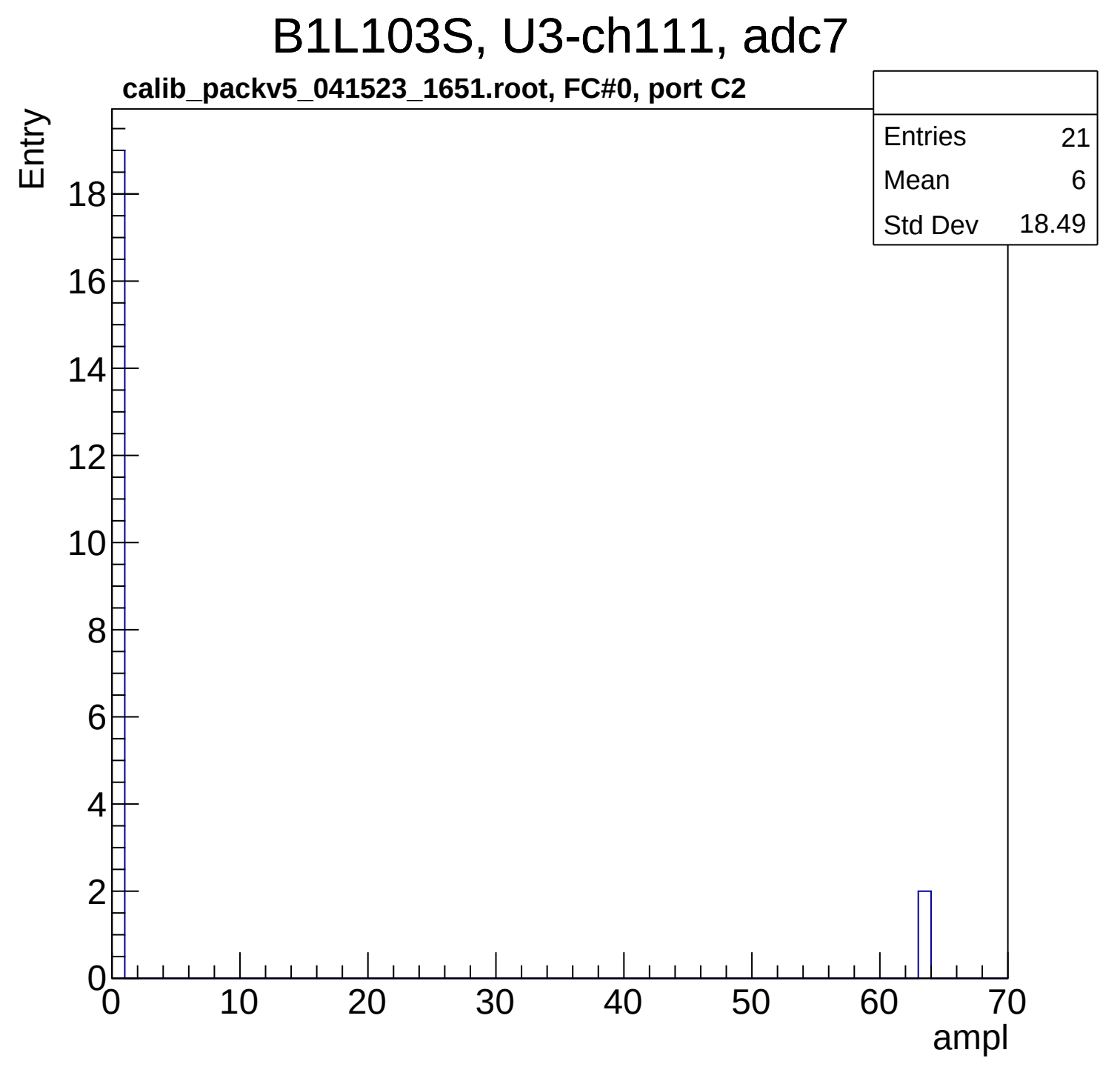
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U3-ch111, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 6
Std Dev 18.49
Entry
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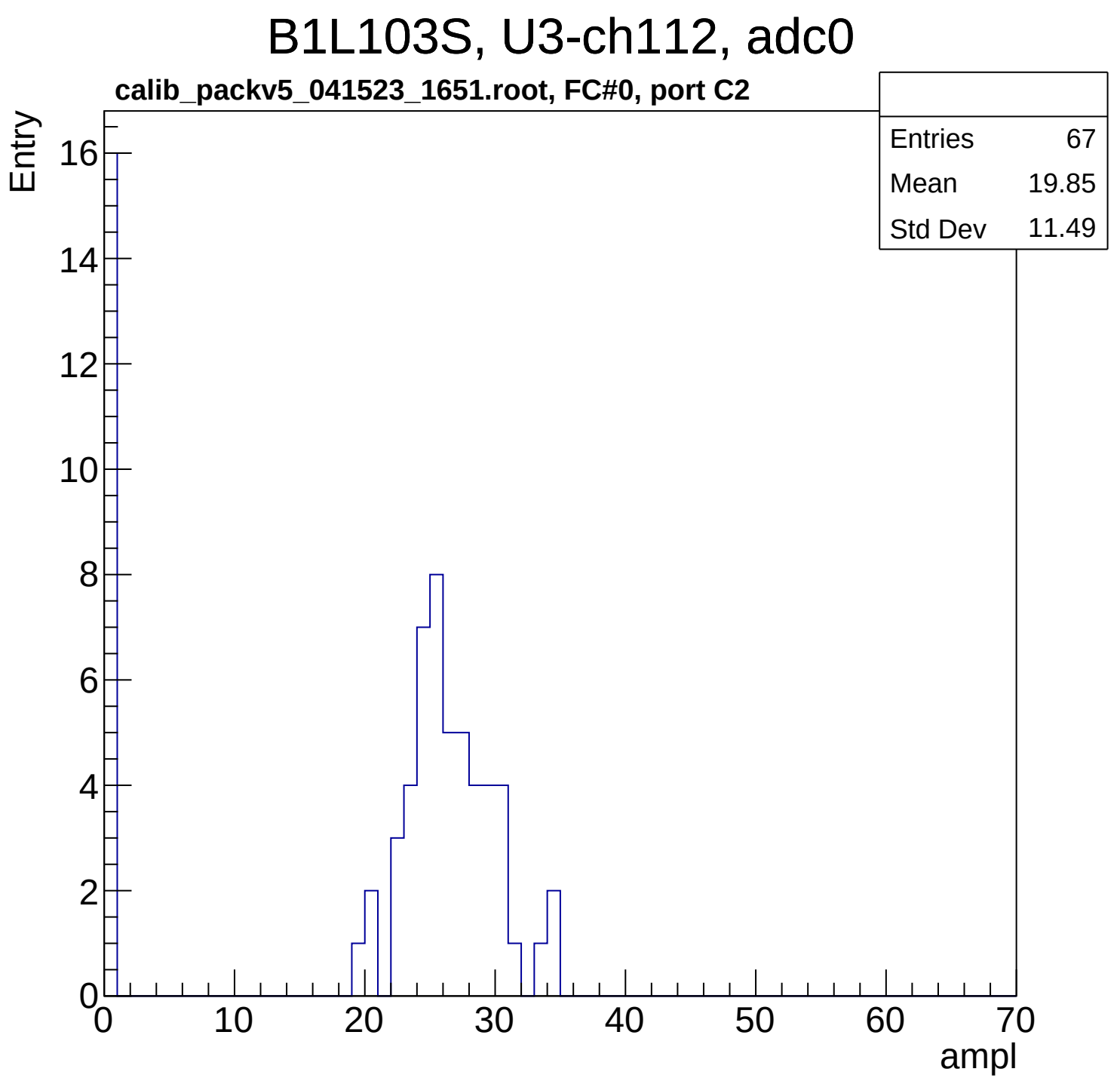
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch112, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 19.85
Std Dev 11.49
Entry
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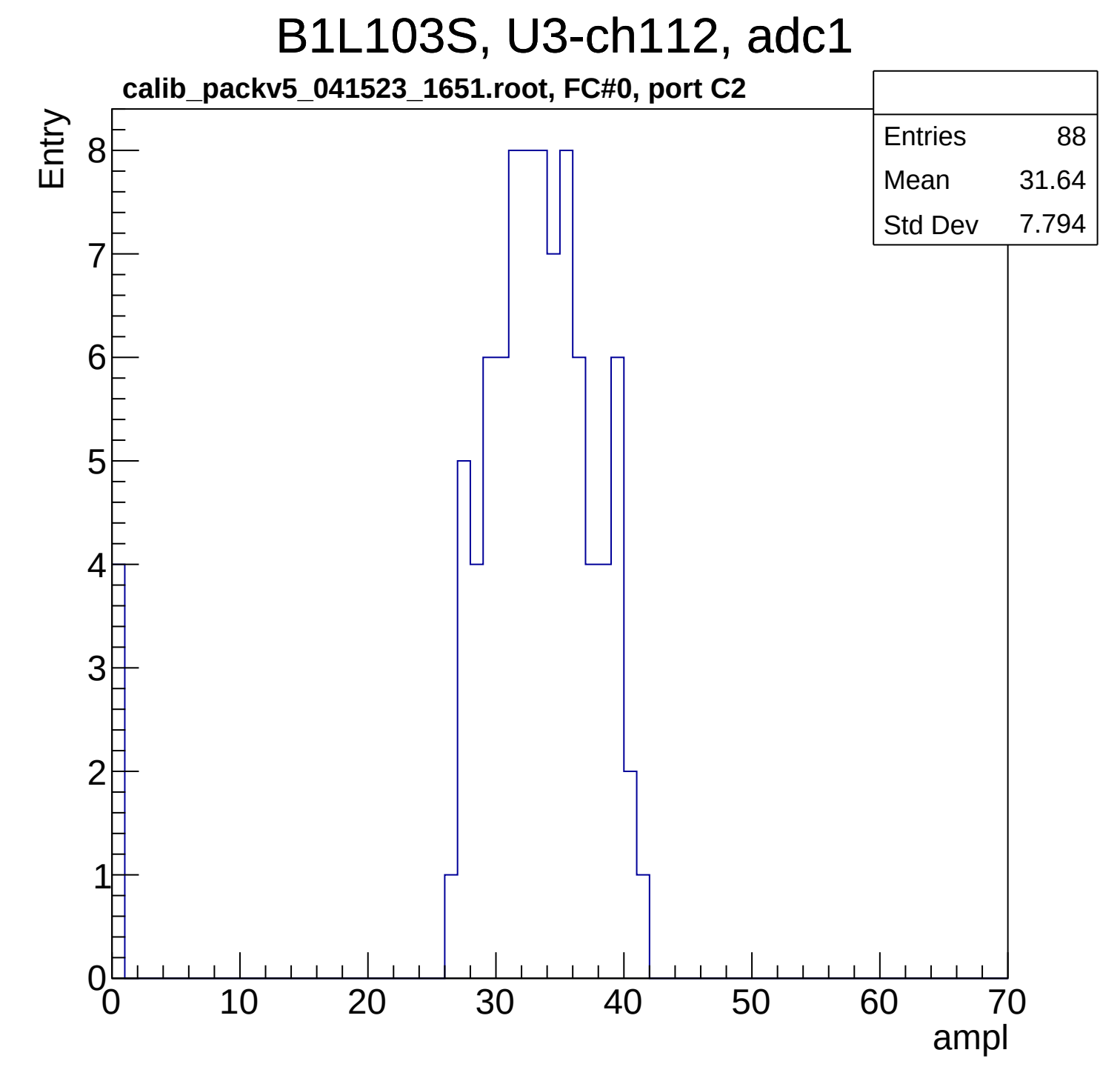
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch112, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 31.64
Std Dev 7.794
Entry
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2
3
4
5
6
7
8
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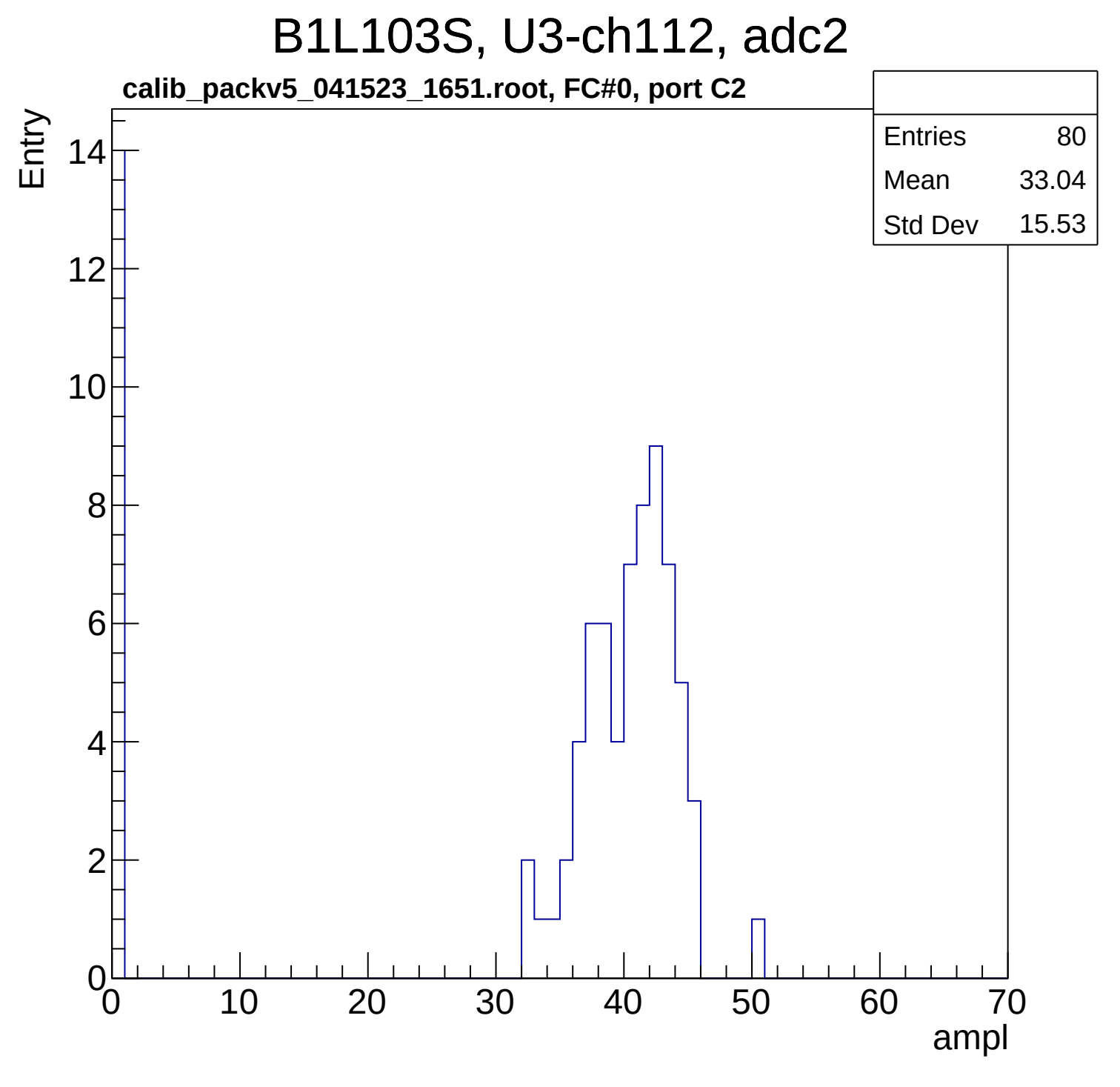
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch112, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 33.04
Std Dev 15.53
Entry
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0
10
20
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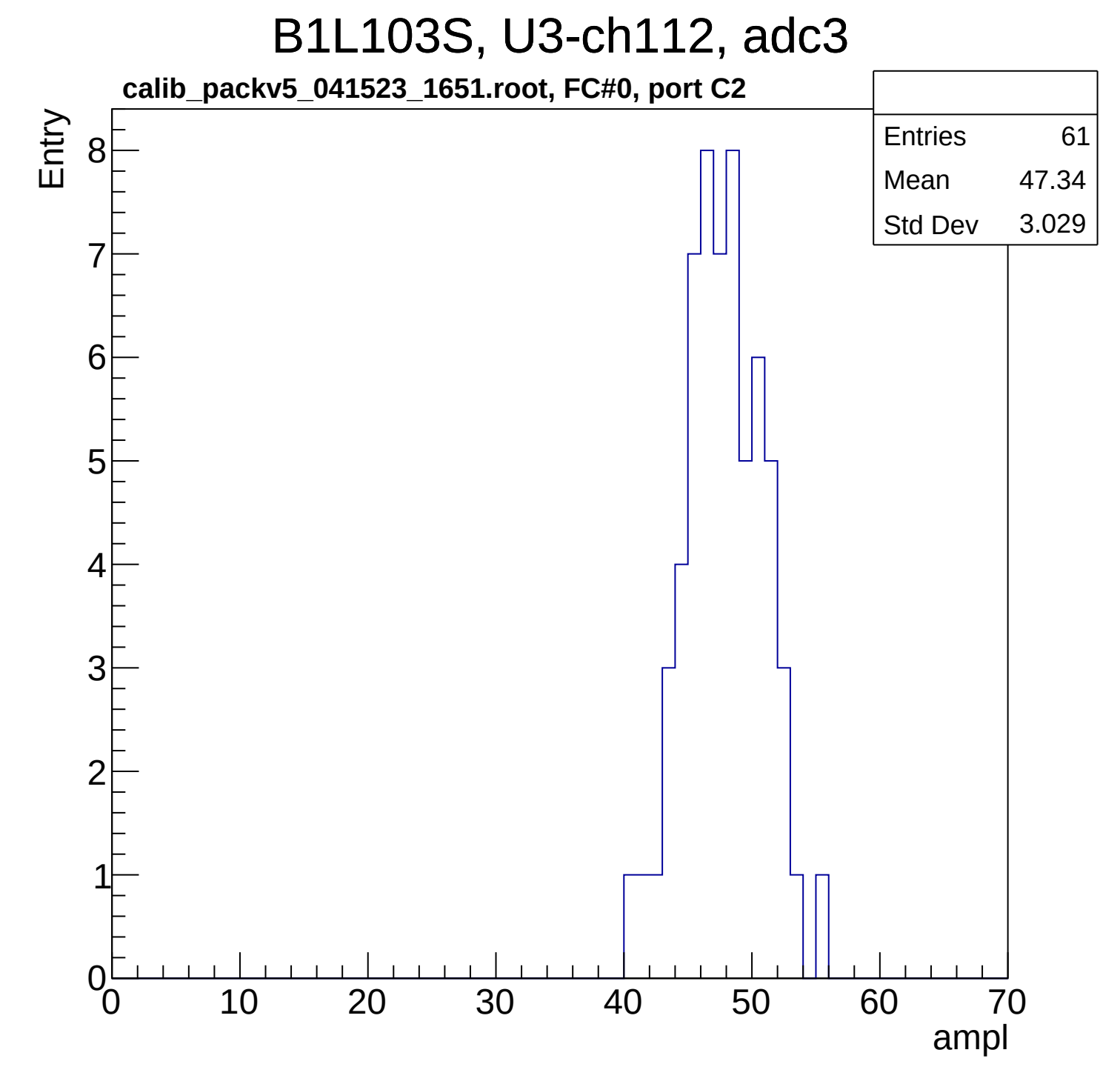
50
60
70
ampl


B1L103S, U3-ch112, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 47.34
Std Dev 3.029
Entry
ampl
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2
3
4
5
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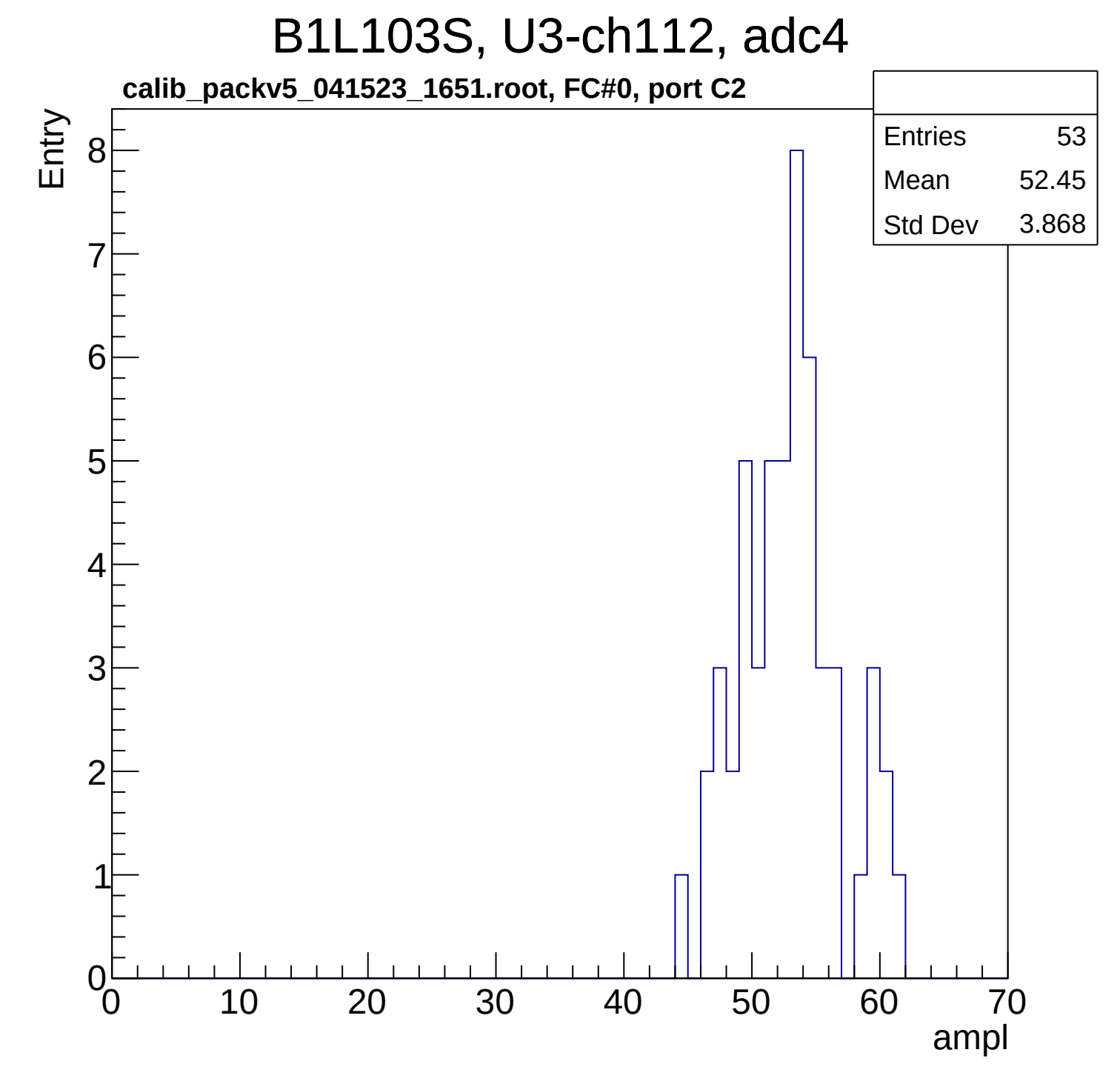
B1L103S, U3-ch112, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 52.45
Std Dev 3.868
Entry
ampl
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2
3
4
5
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7
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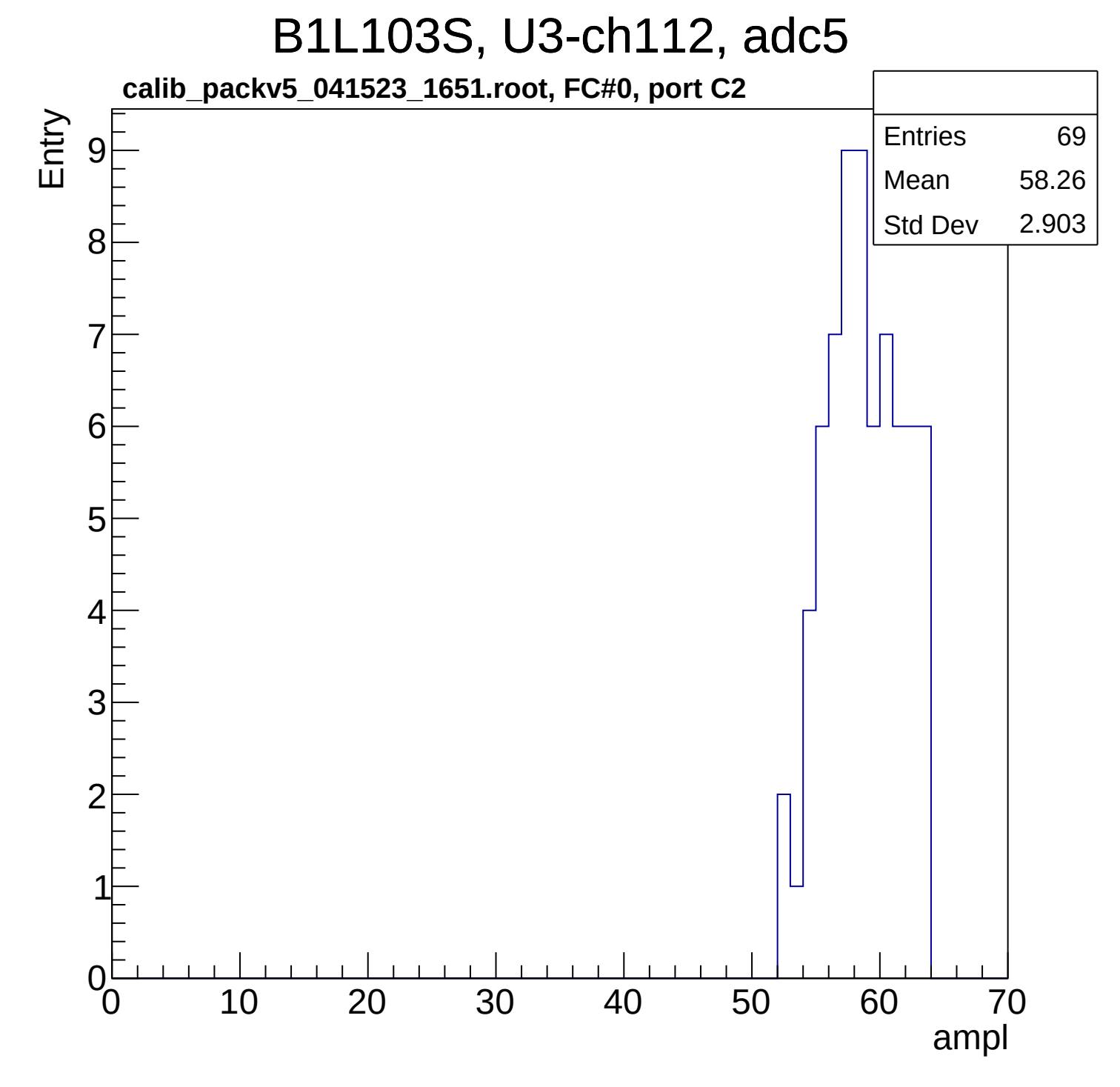
B1L103S, U3-ch112, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 58.26
Std Dev 2.903
Entry
ampl
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0
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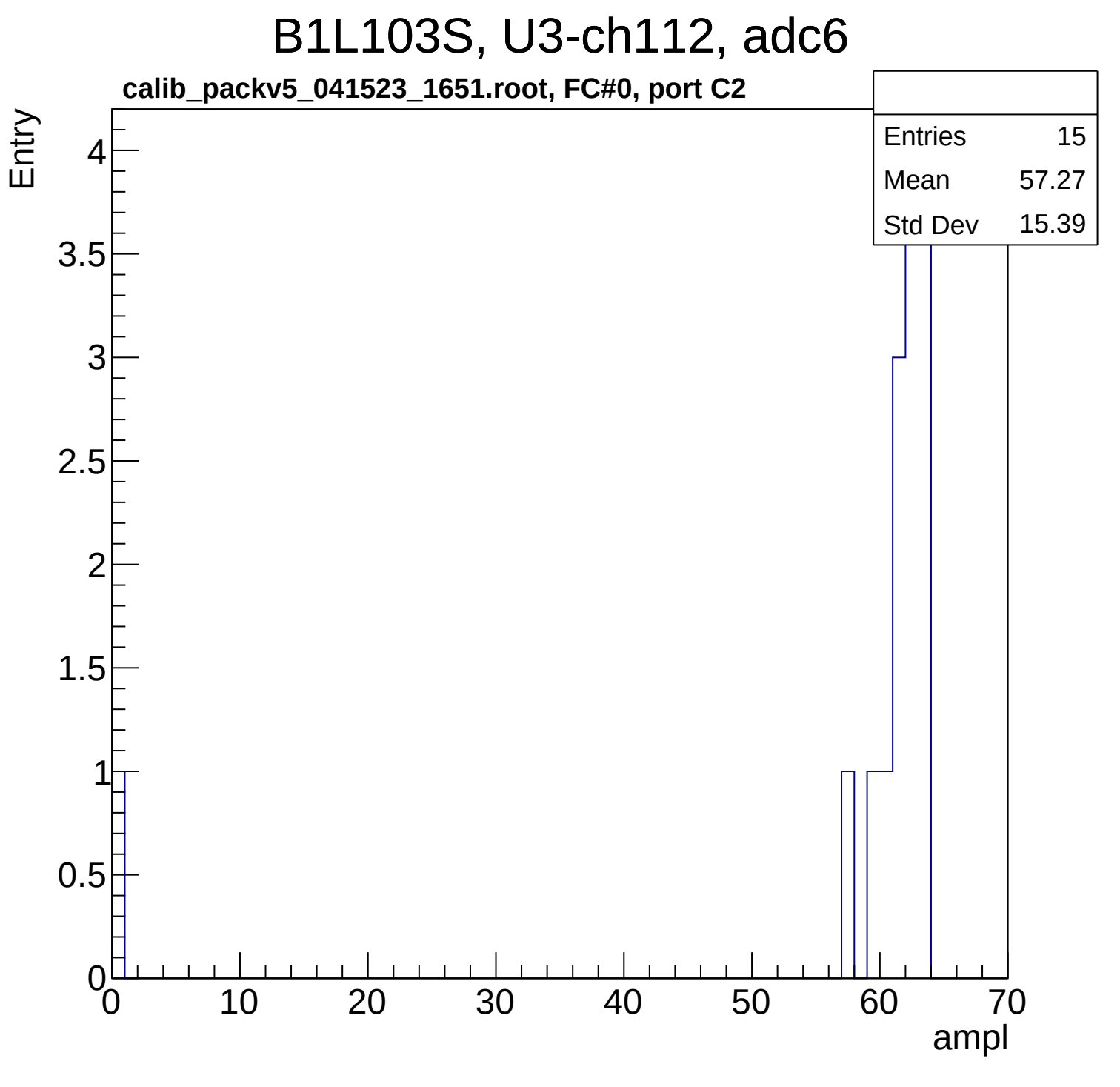
B1L103S, U3-ch112, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 57.27
Std Dev 15.39
Entry
ampl
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0.5
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1.5
2
2.5
3
3.5
4
0
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40
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60
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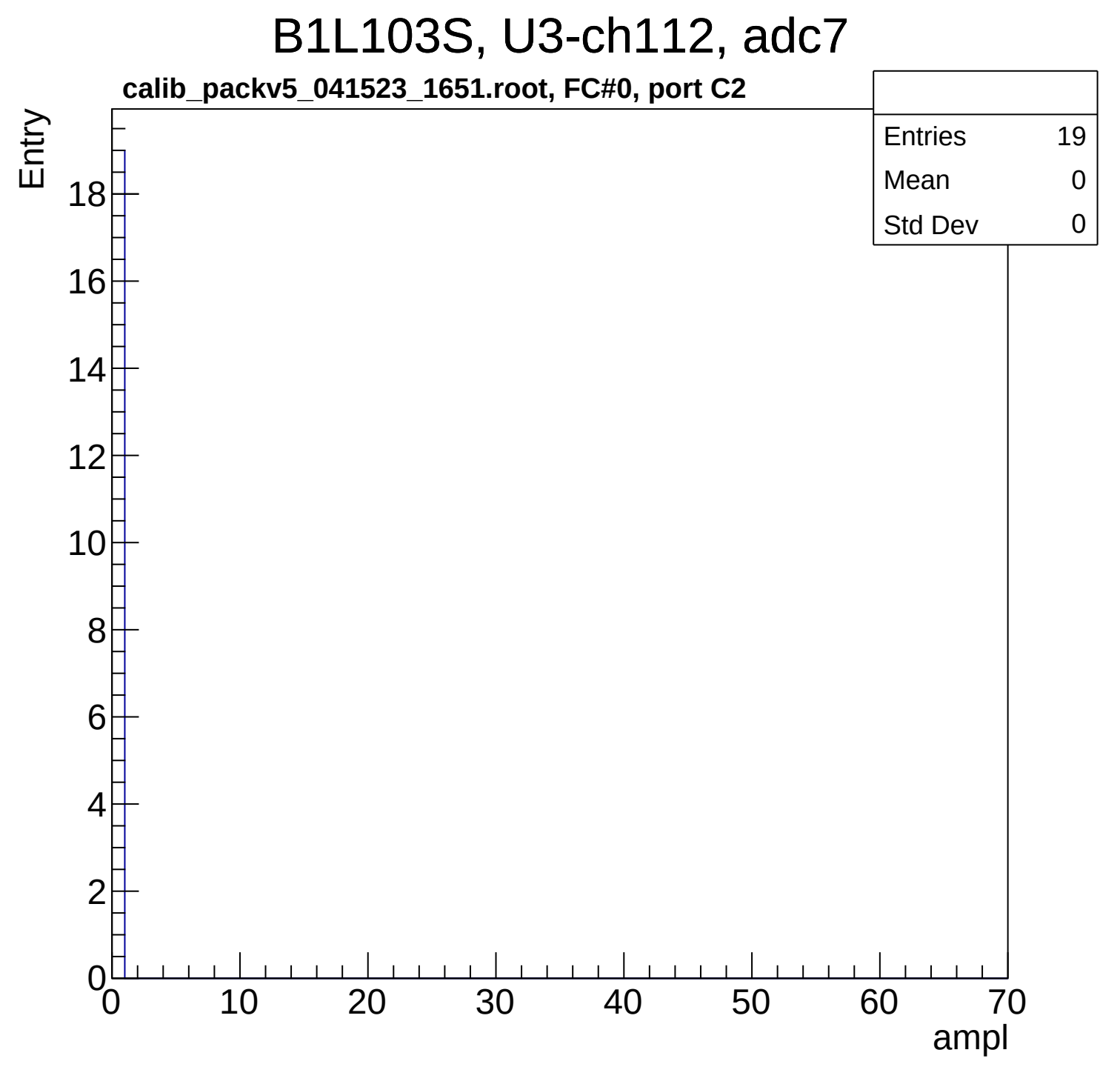
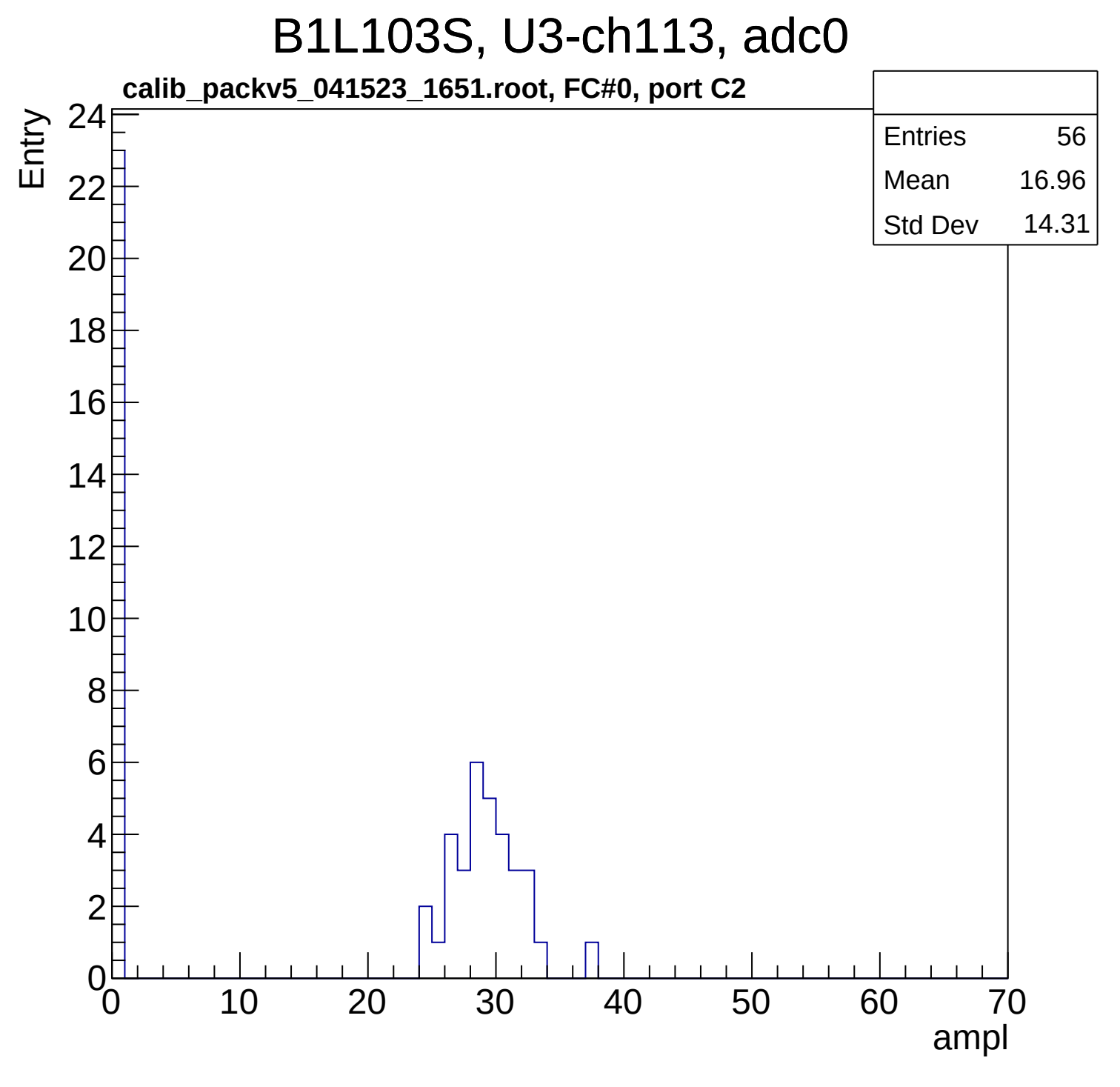

B1L103S, U3-ch112, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch113, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 16.96
Std Dev 14.31
Entry
ampl
0
2
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10
12
14
16
18
20
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40
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60
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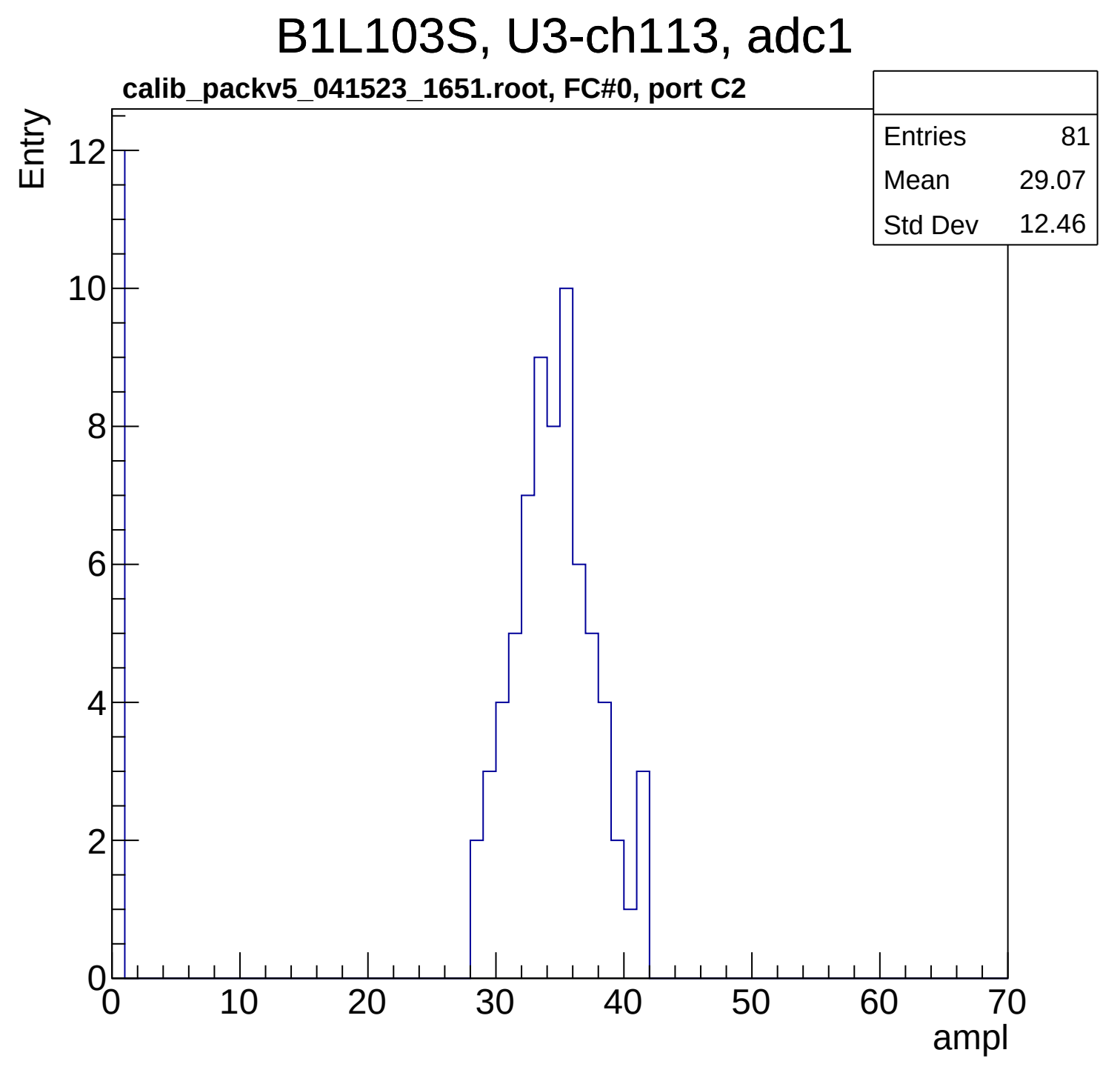
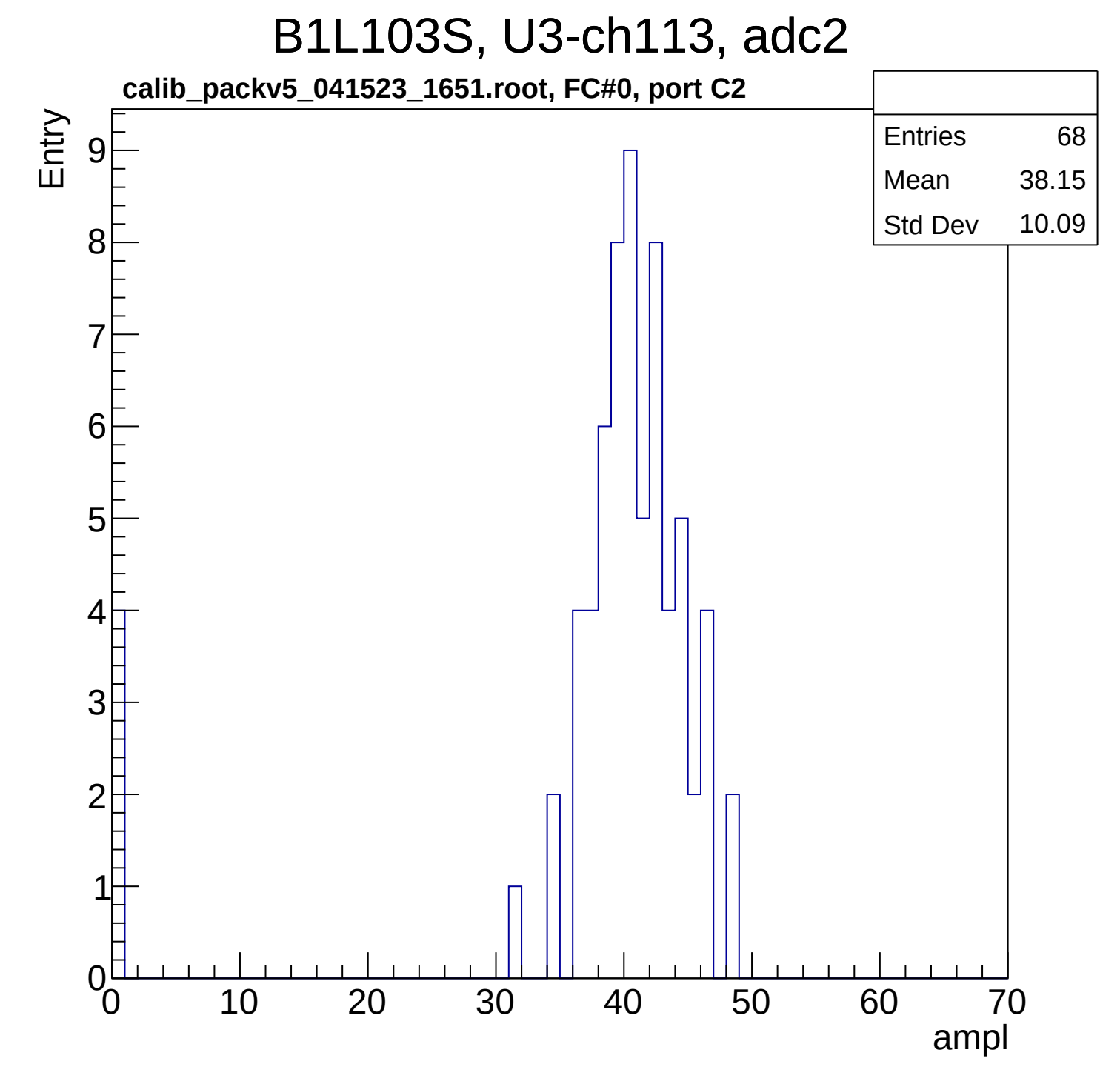

B1L103S, U3-ch113, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 29.07
Std Dev 12.46
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch113, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 38.15
Std Dev 10.09
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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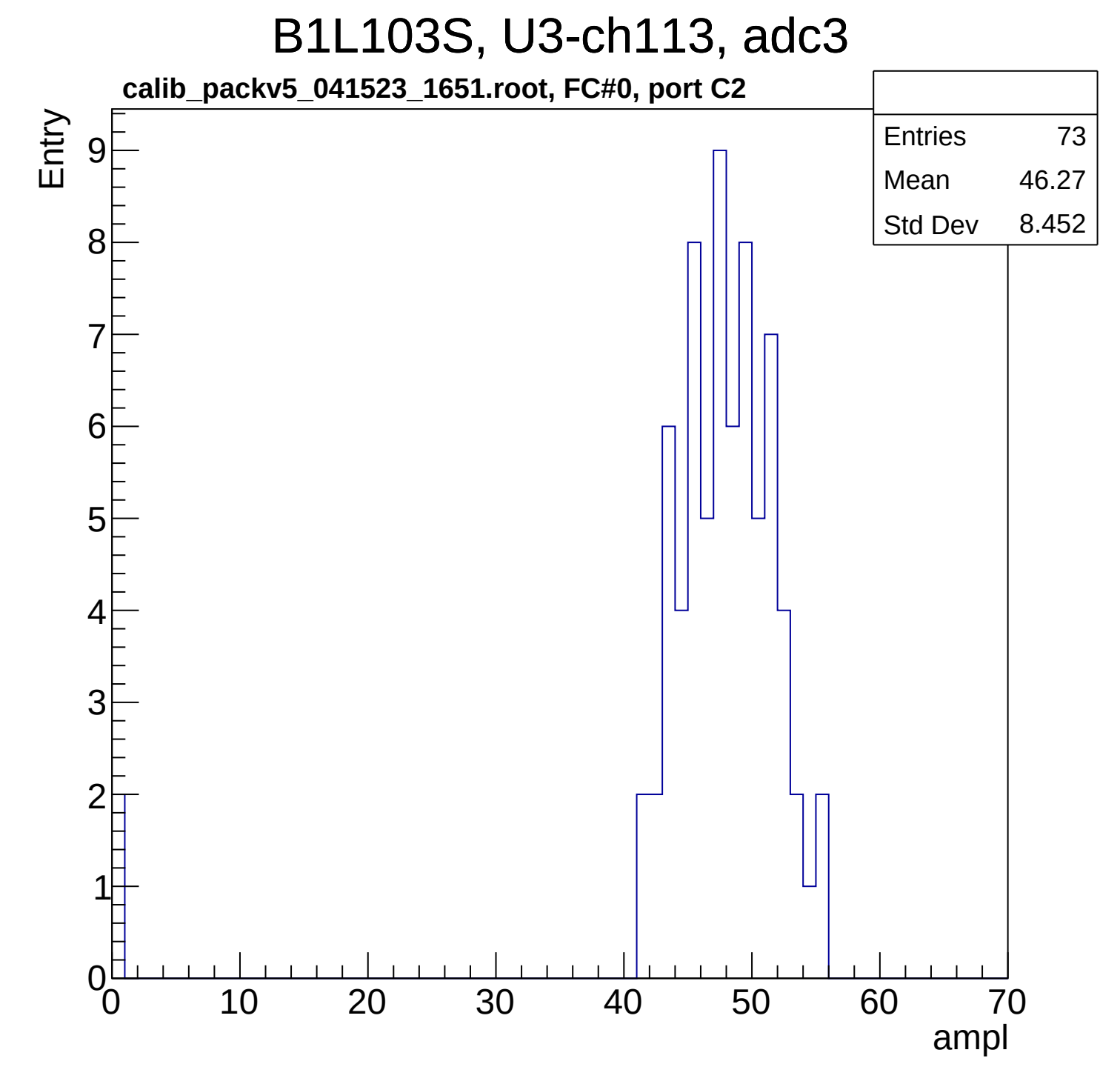
B1L103S, U3-ch113, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 46.27
Std Dev 8.452
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
30
40
50
60
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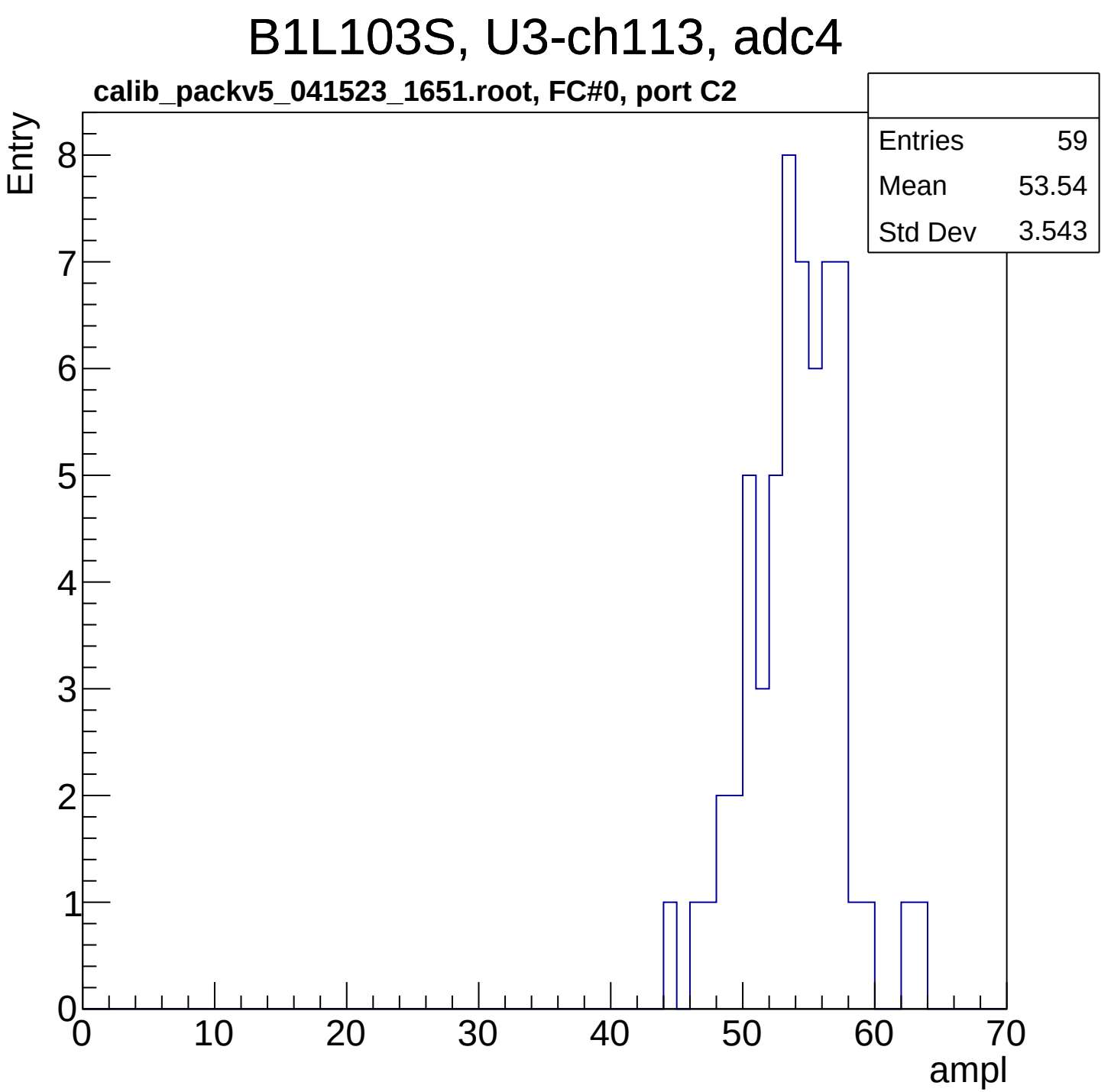
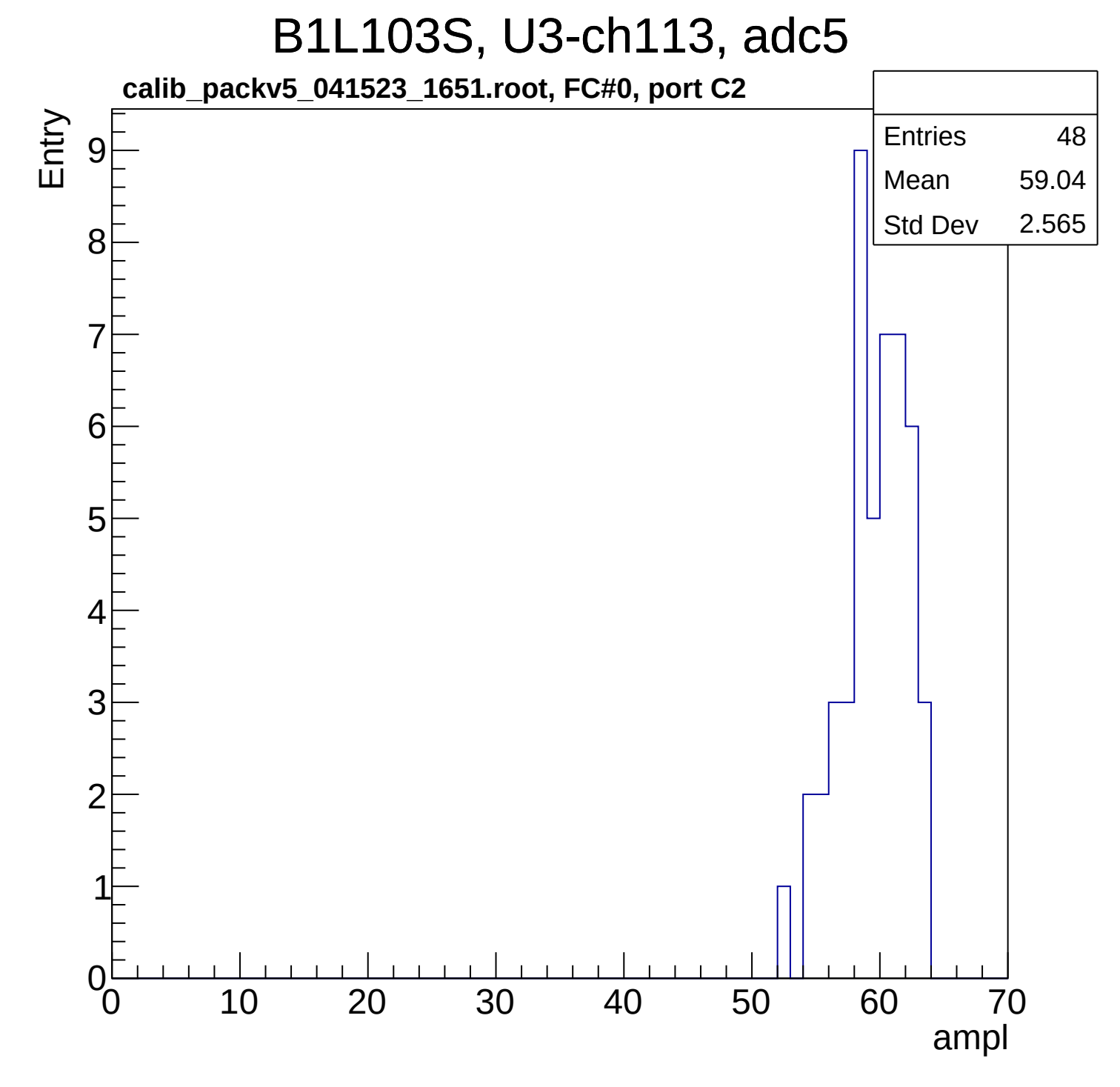

B1L103S, U3-ch113, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 53.54
Std Dev 3.543
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch113, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 59.04
Std Dev 2.565
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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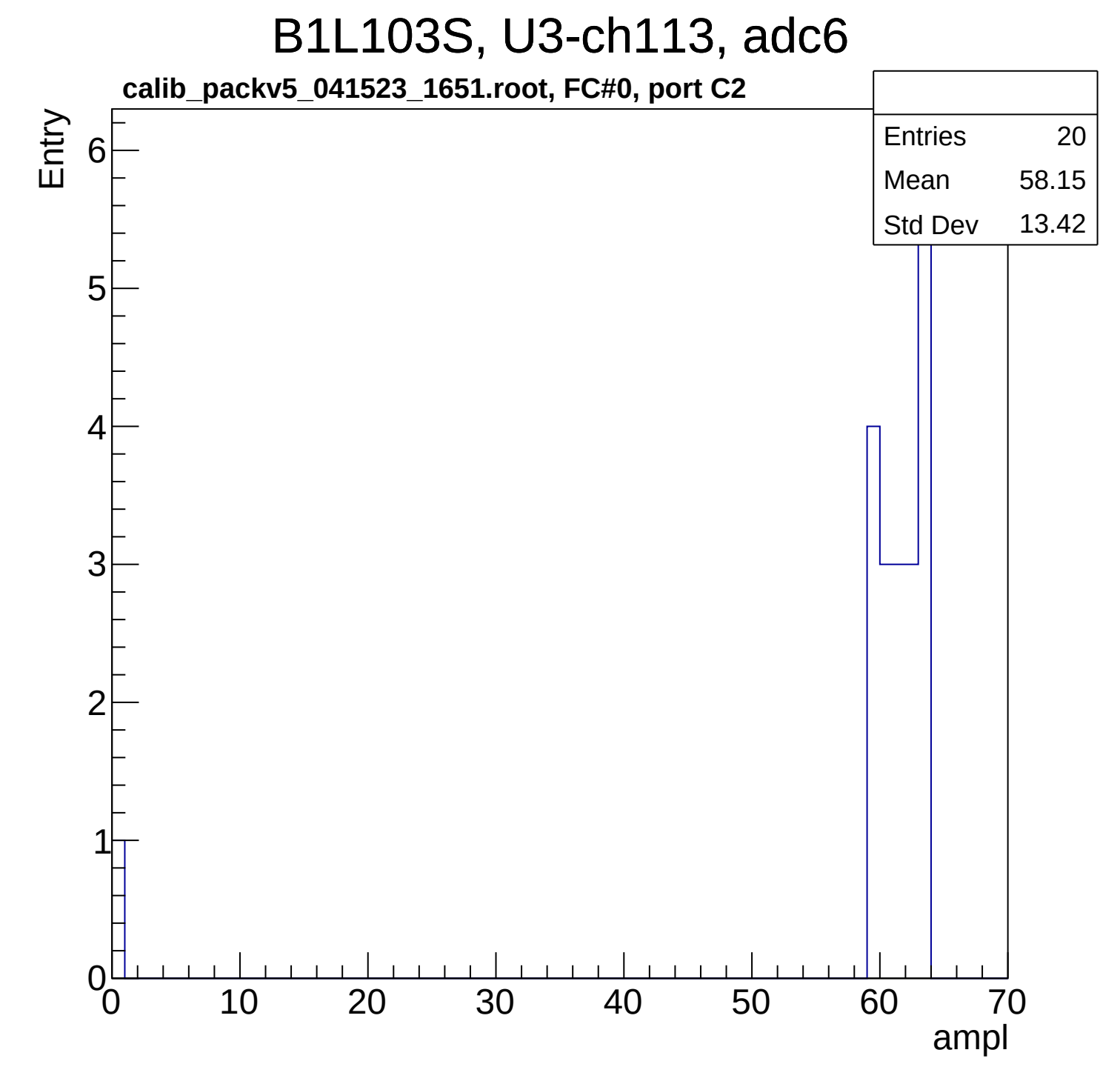
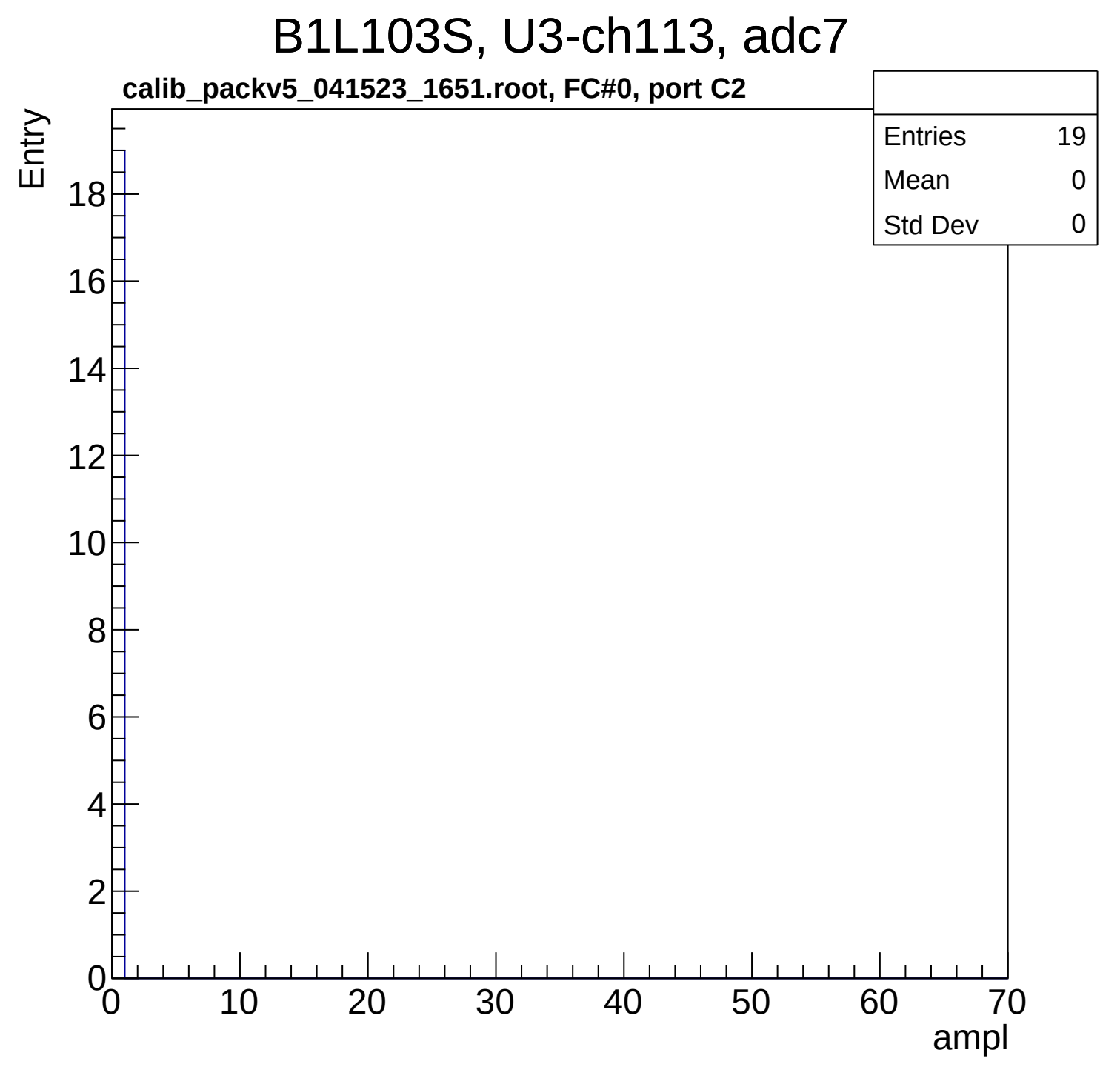
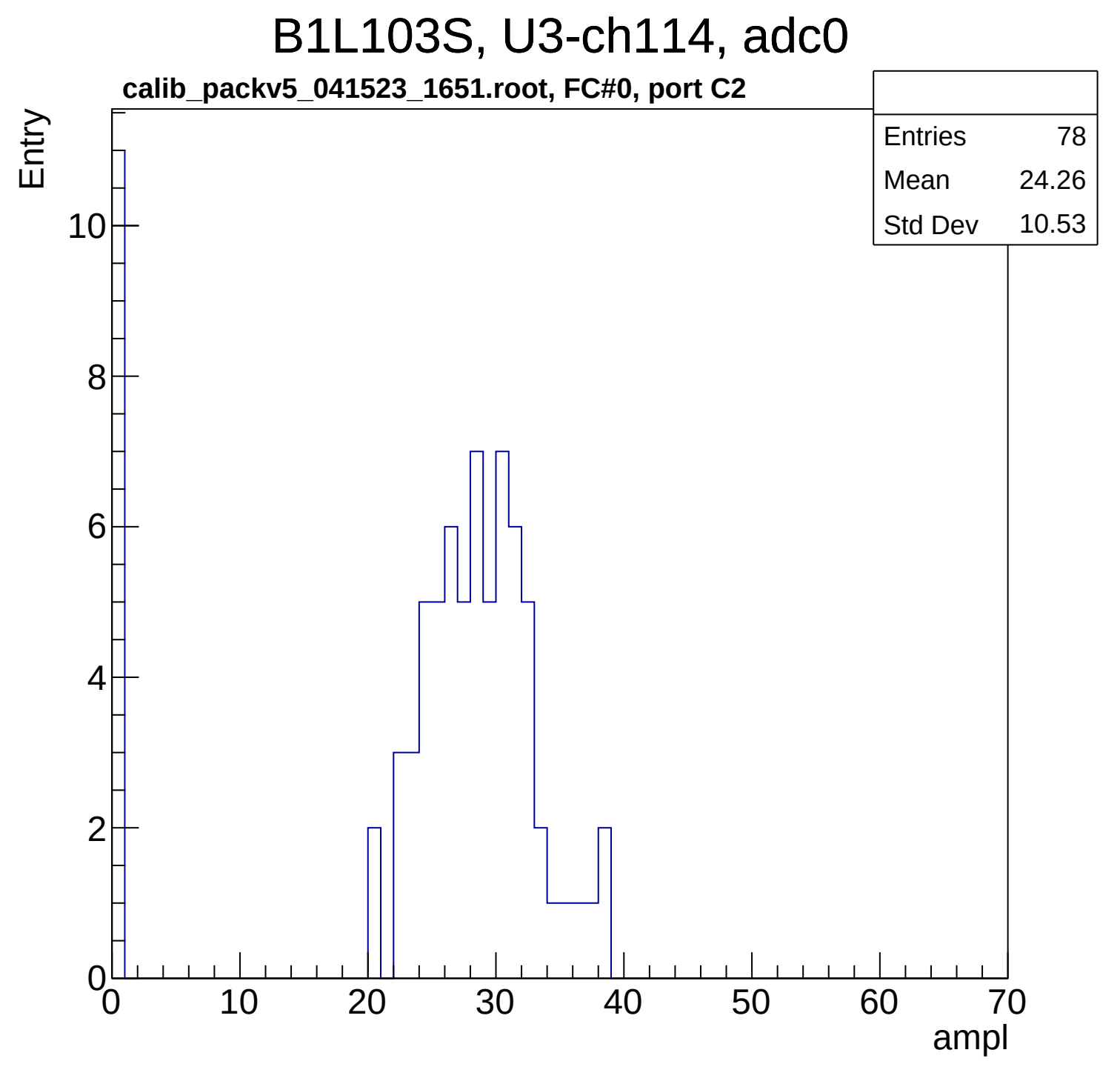
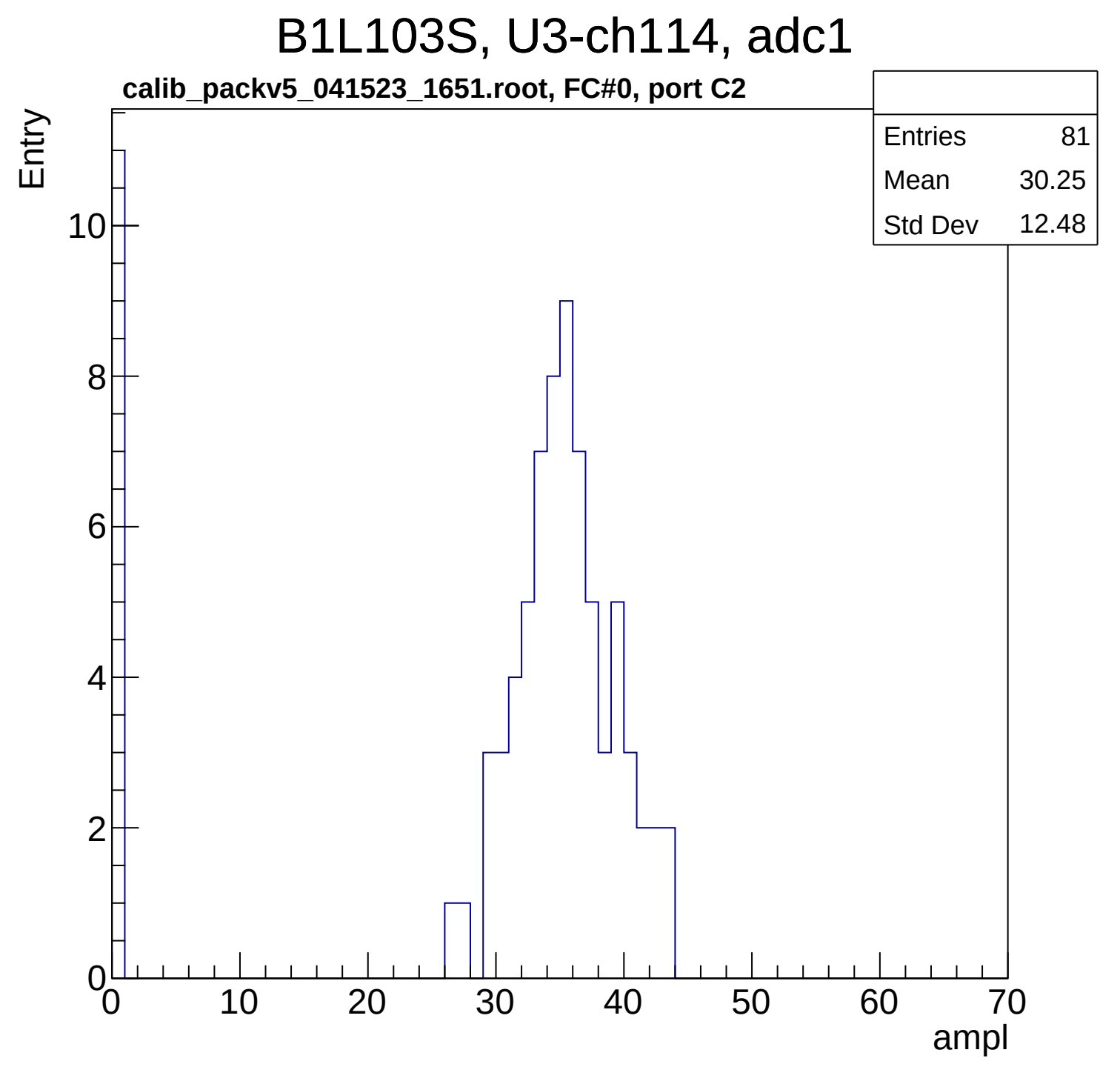
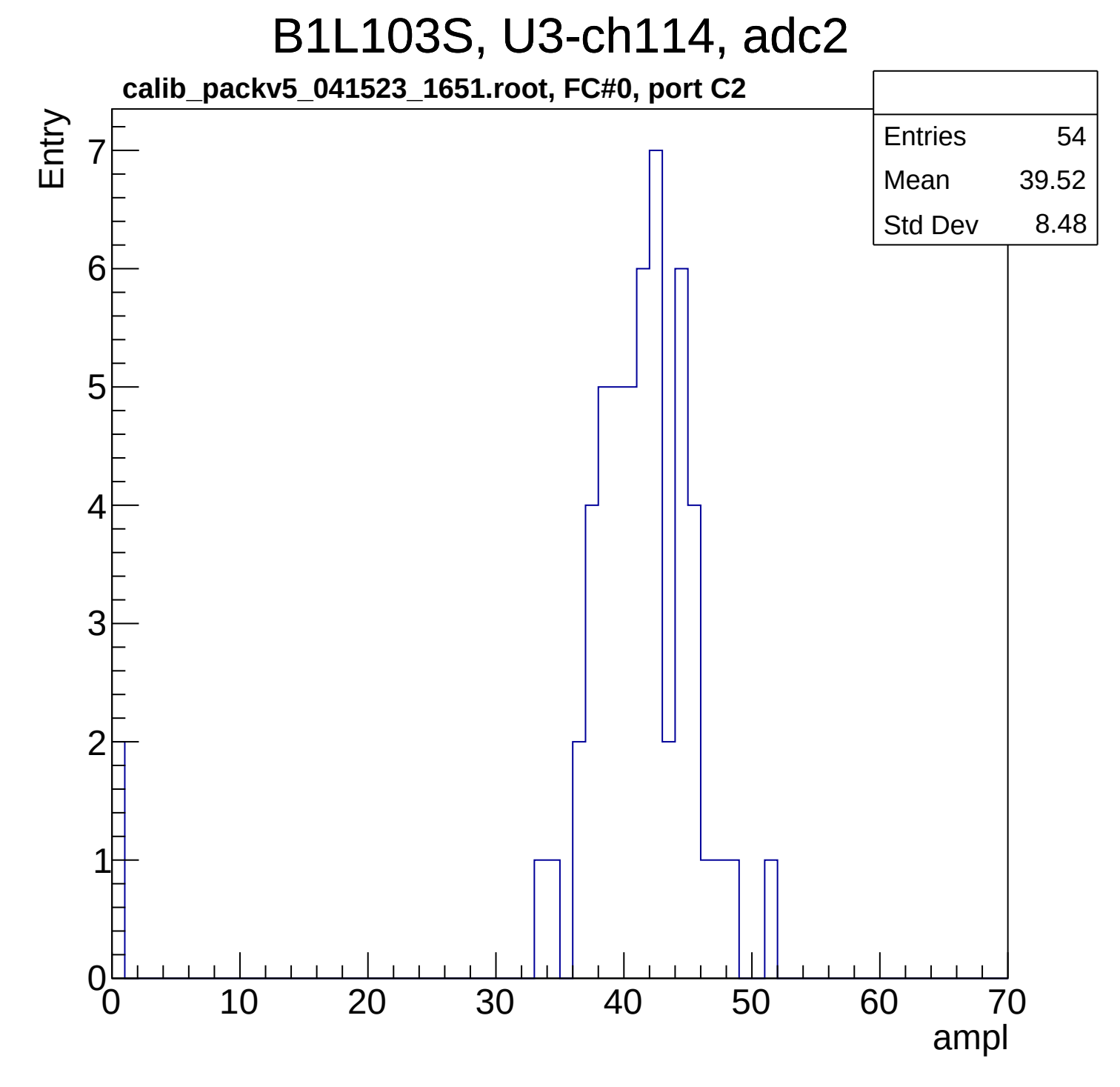
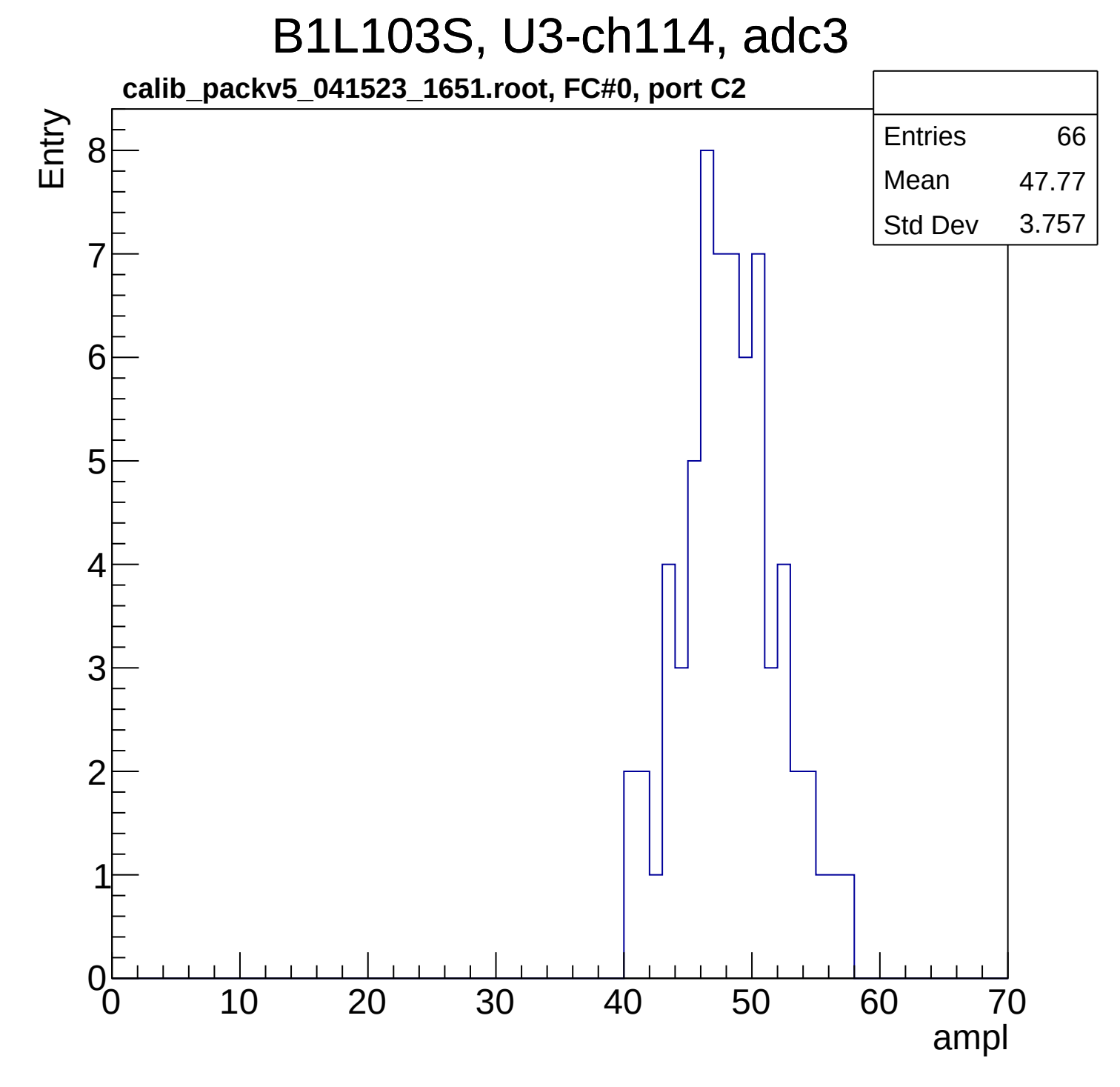

B1L103S, U3-ch113, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 58.15
Std Dev 13.42
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U3-ch113, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch114, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 24.26
Std Dev 10.53
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch114, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 30.25
Std Dev 12.48
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch114, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 39.52
Std Dev 8.48
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch114, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 47.77
Std Dev 3.757
Entry
ampl
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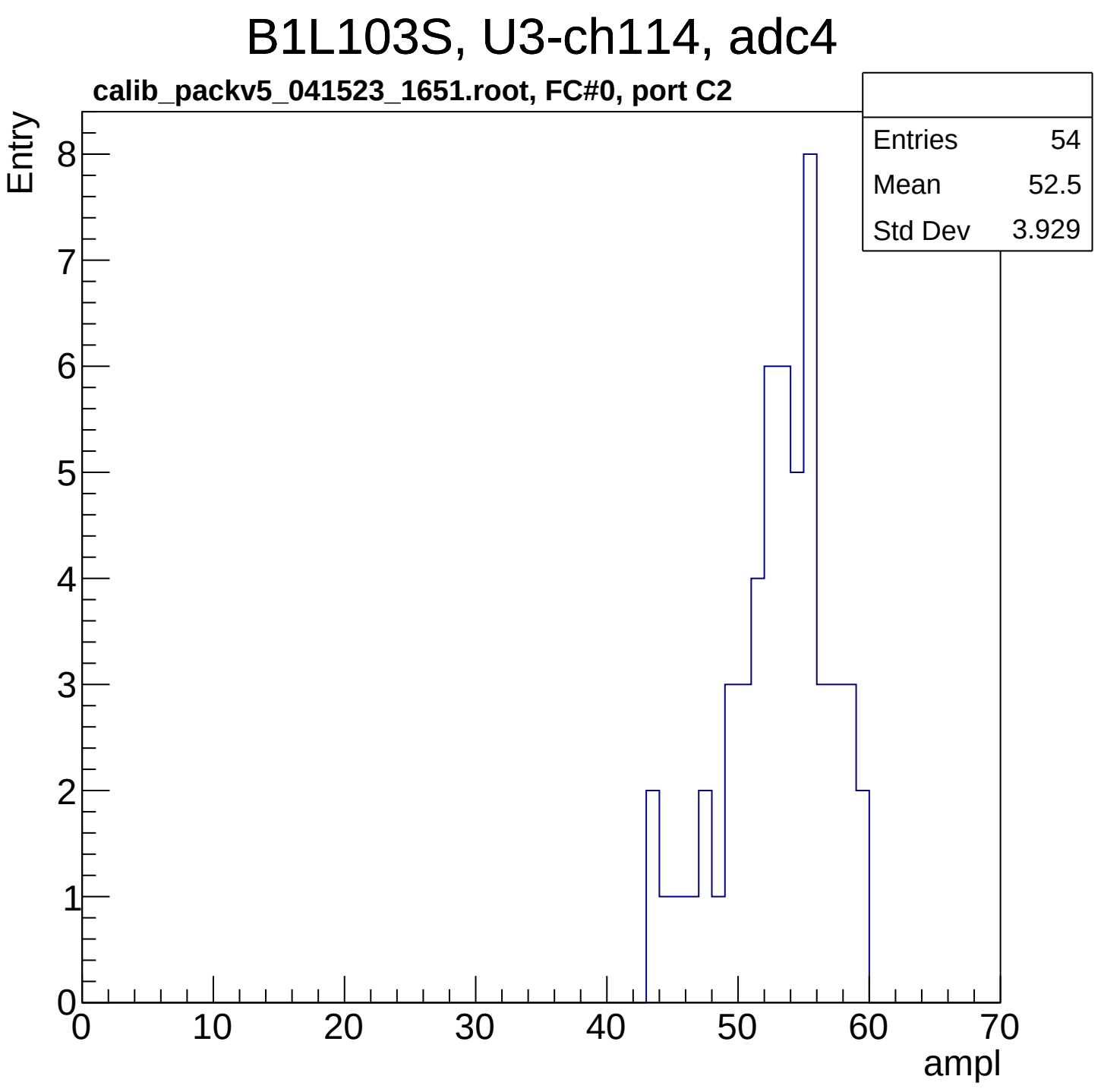
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch114, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 52.5
Std Dev 3.929
Entry
ampl
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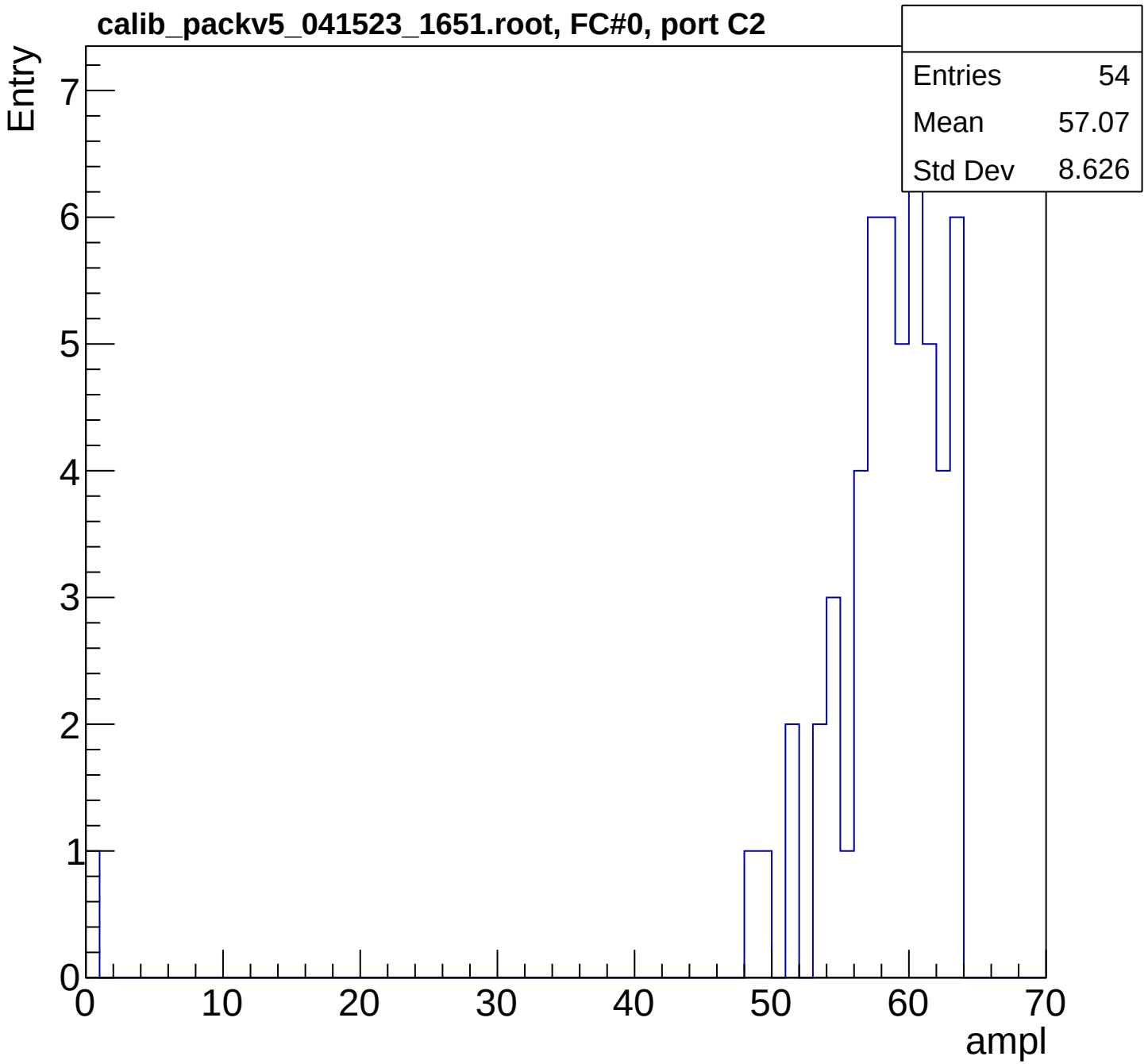
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch114, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 57.07
Std Dev 8.626
Entry
ampl
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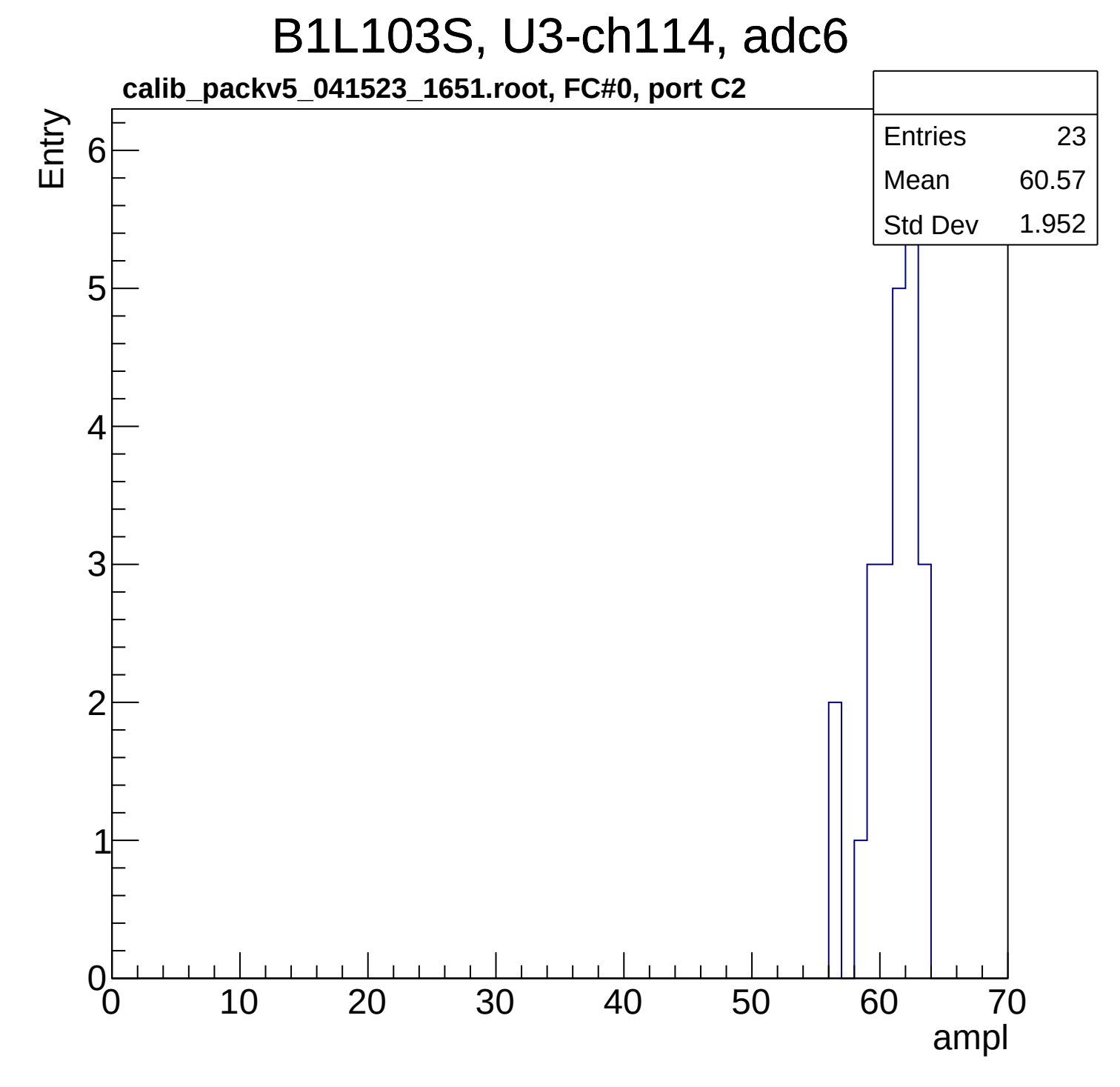
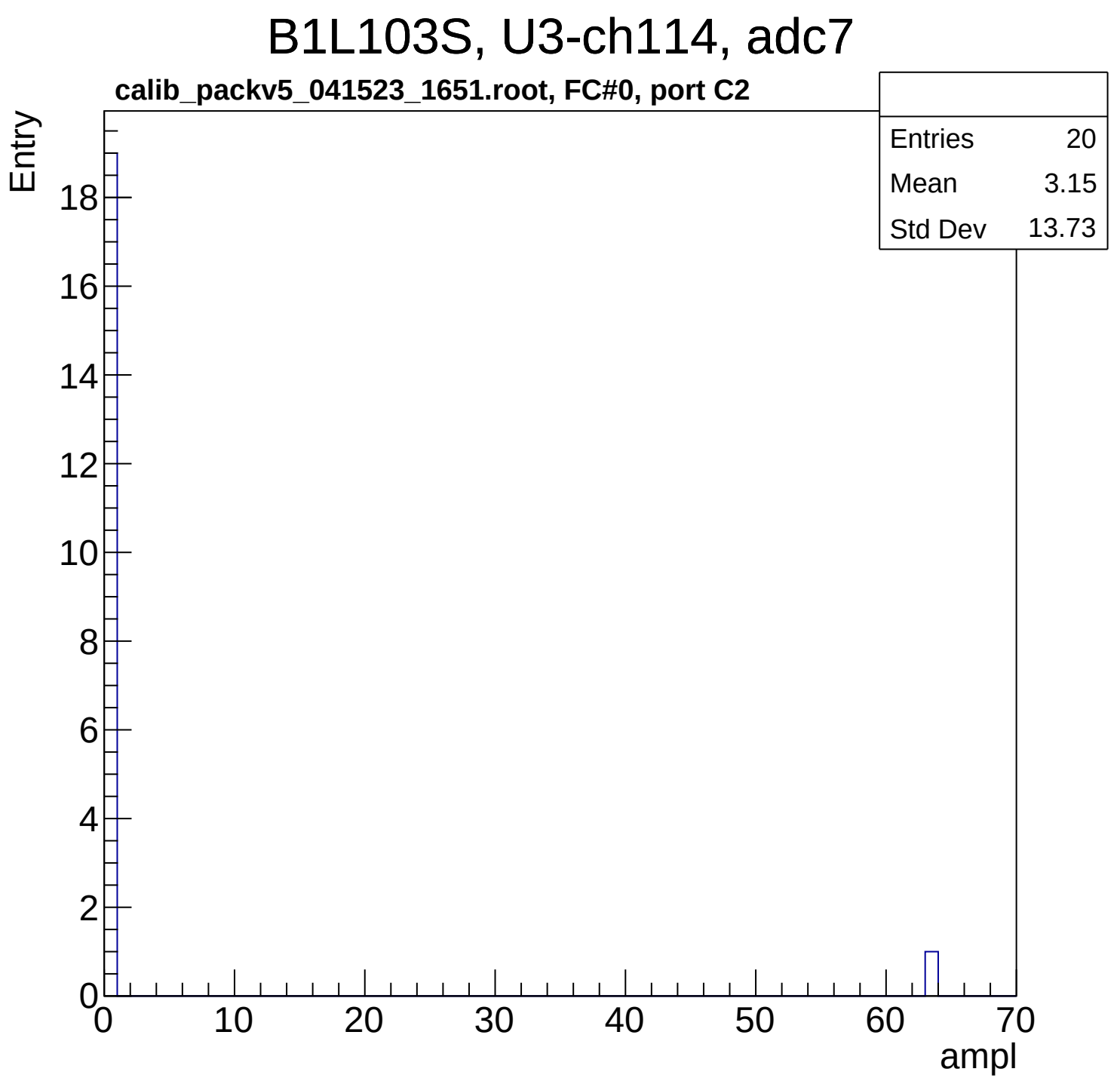
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch114, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 60.57
Std Dev 1.952
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U3-ch114, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
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6
8
10
12
14
16
18
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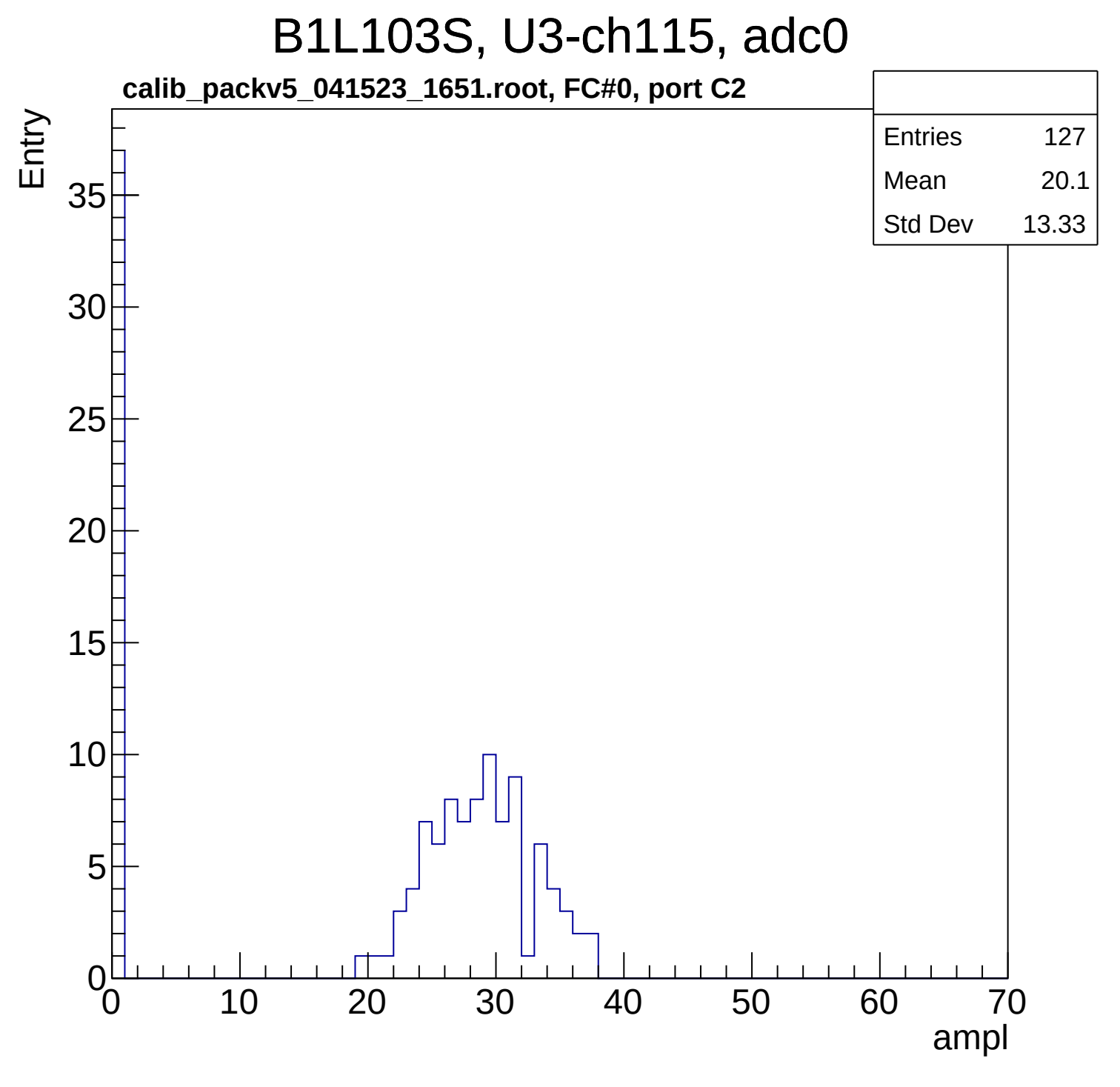
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch115, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 127
Mean 20.1
Std Dev 13.33
Entry
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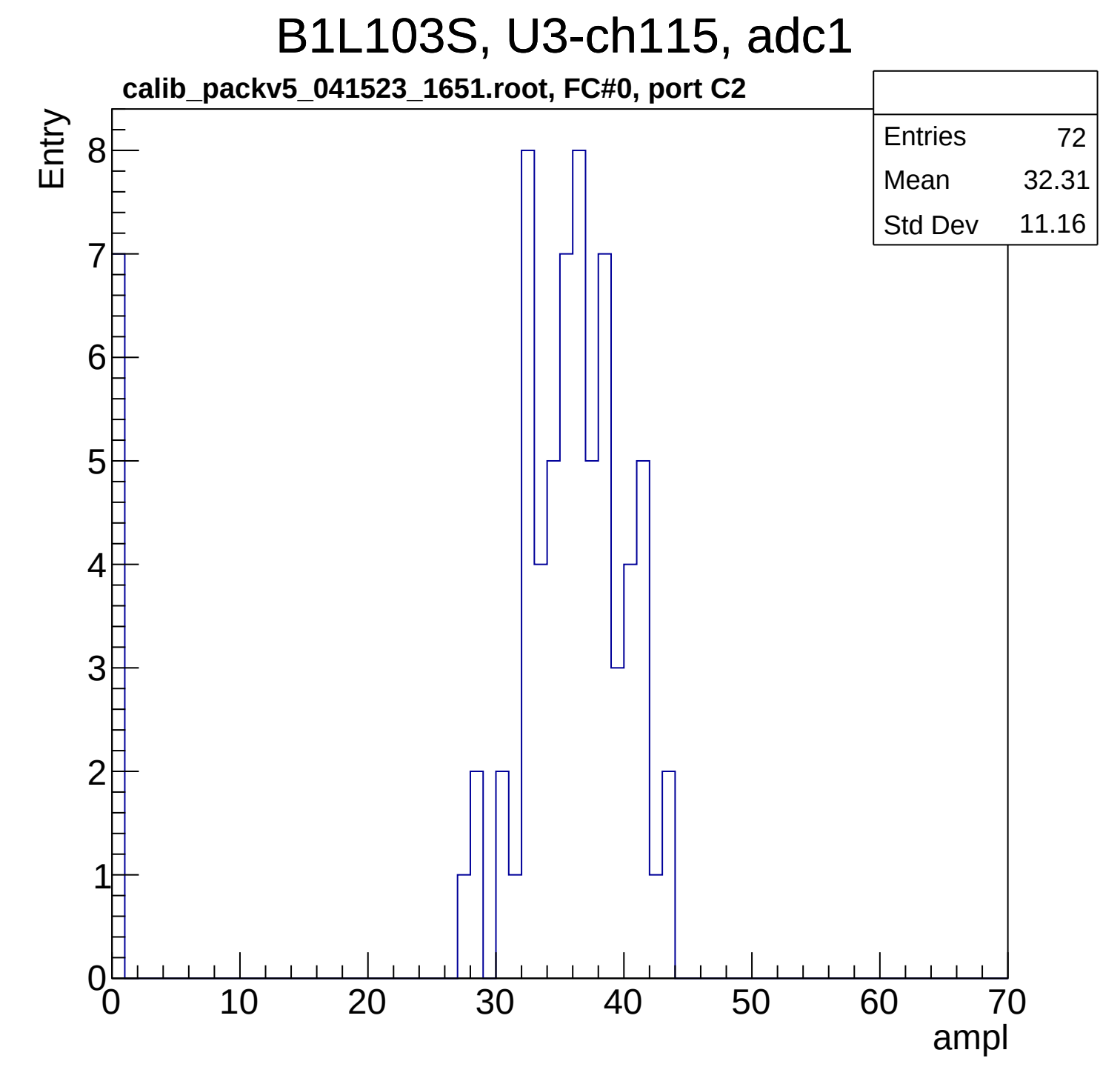
5
10
15
20
25
30
35
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch115, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 32.31
Std Dev 11.16
Entry
ampl
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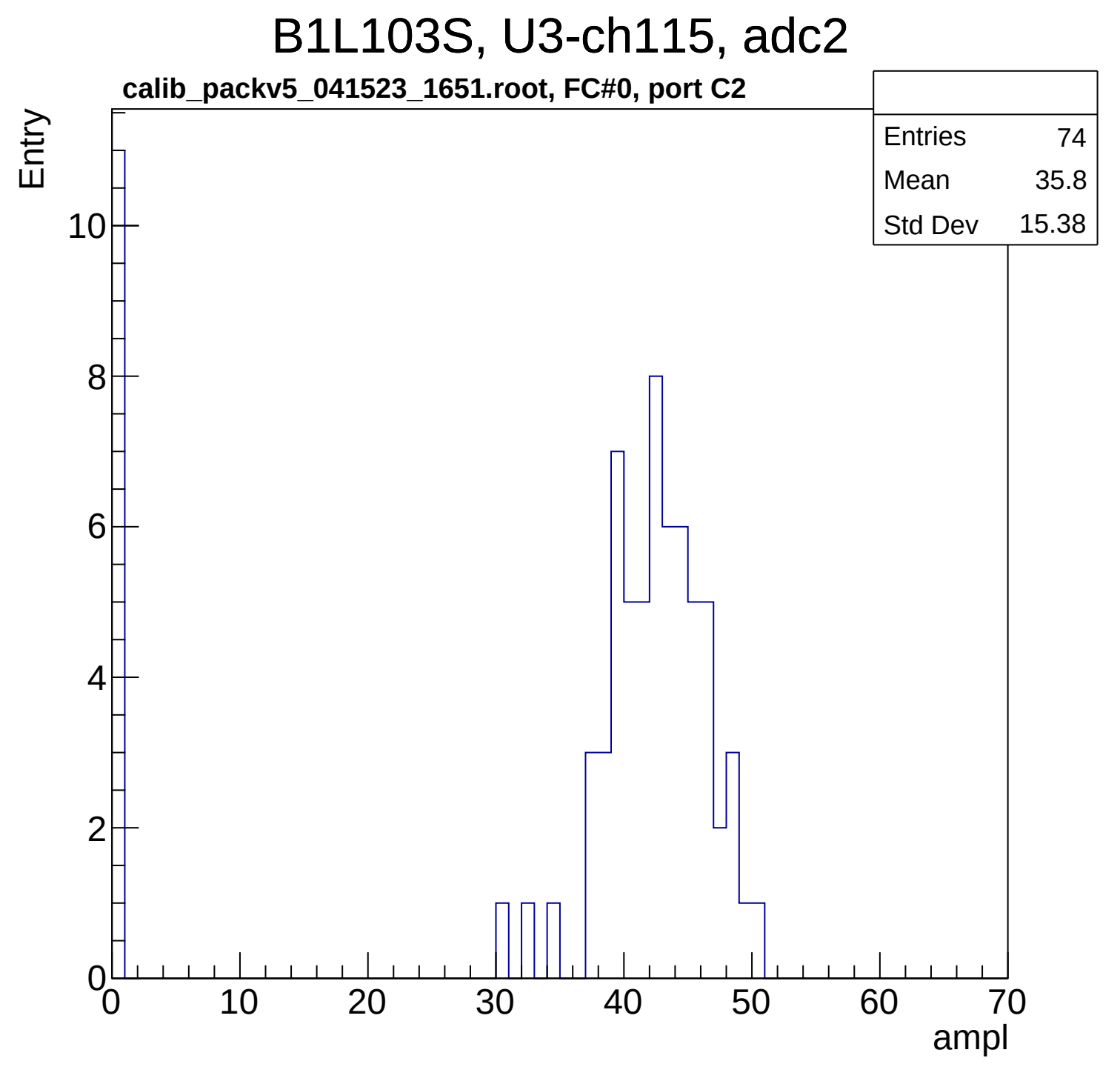
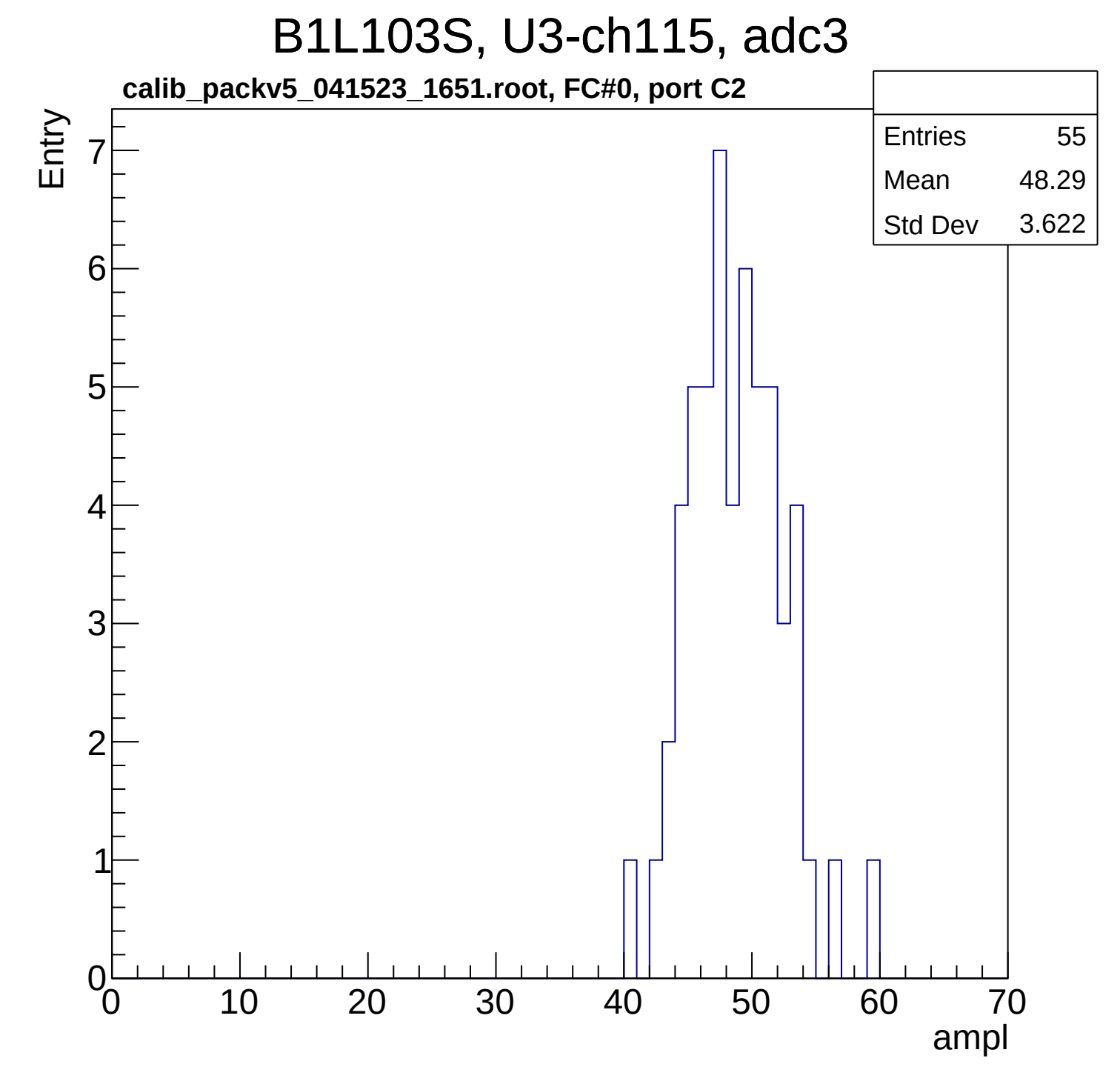
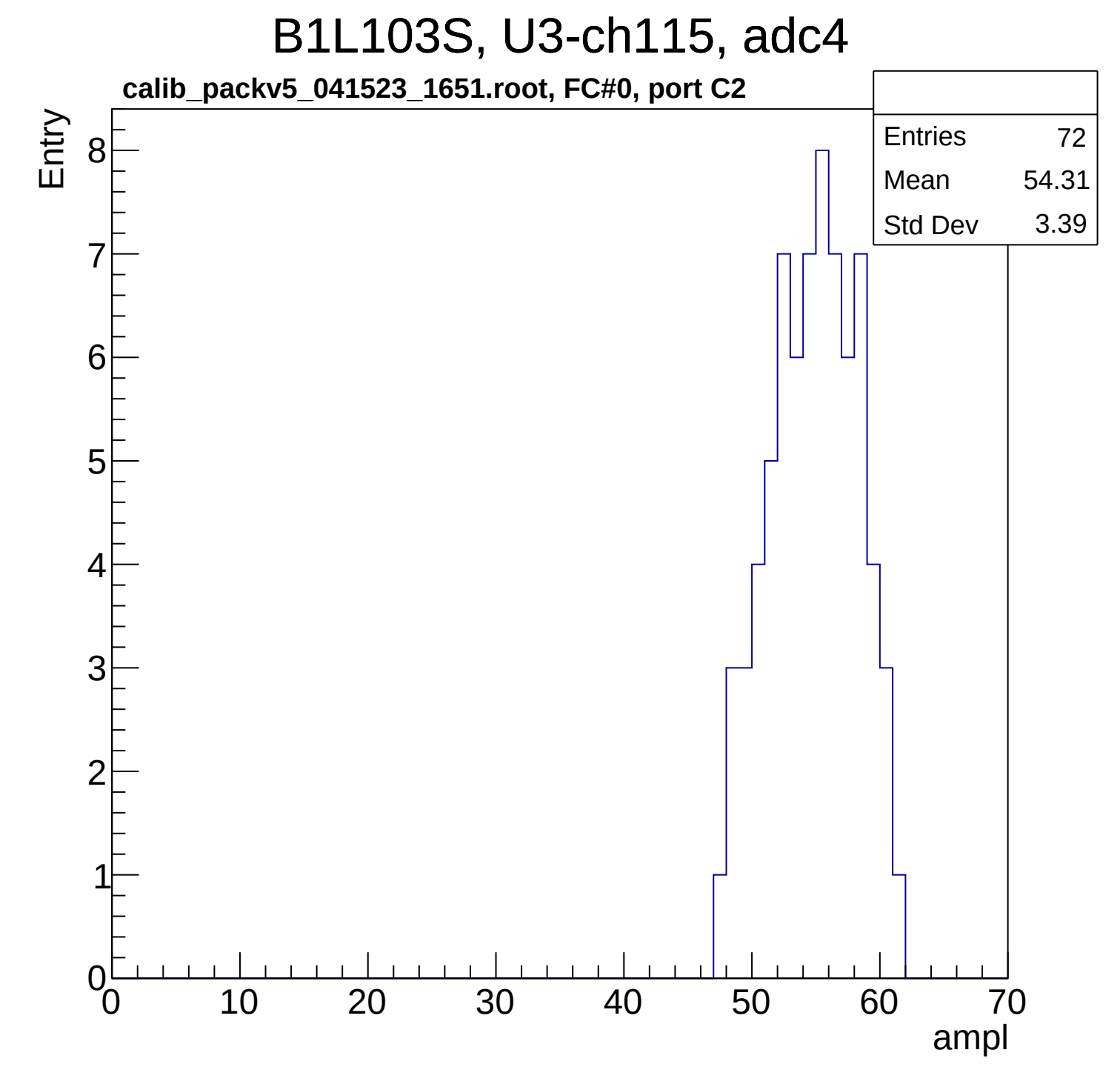
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch115, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 35.8
Std Dev 15.38
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch115, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 48.29
Std Dev 3.622
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch115, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 54.31
Std Dev 3.39
Entry
ampl
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1
2
3
4
5
6
7
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0
10
20
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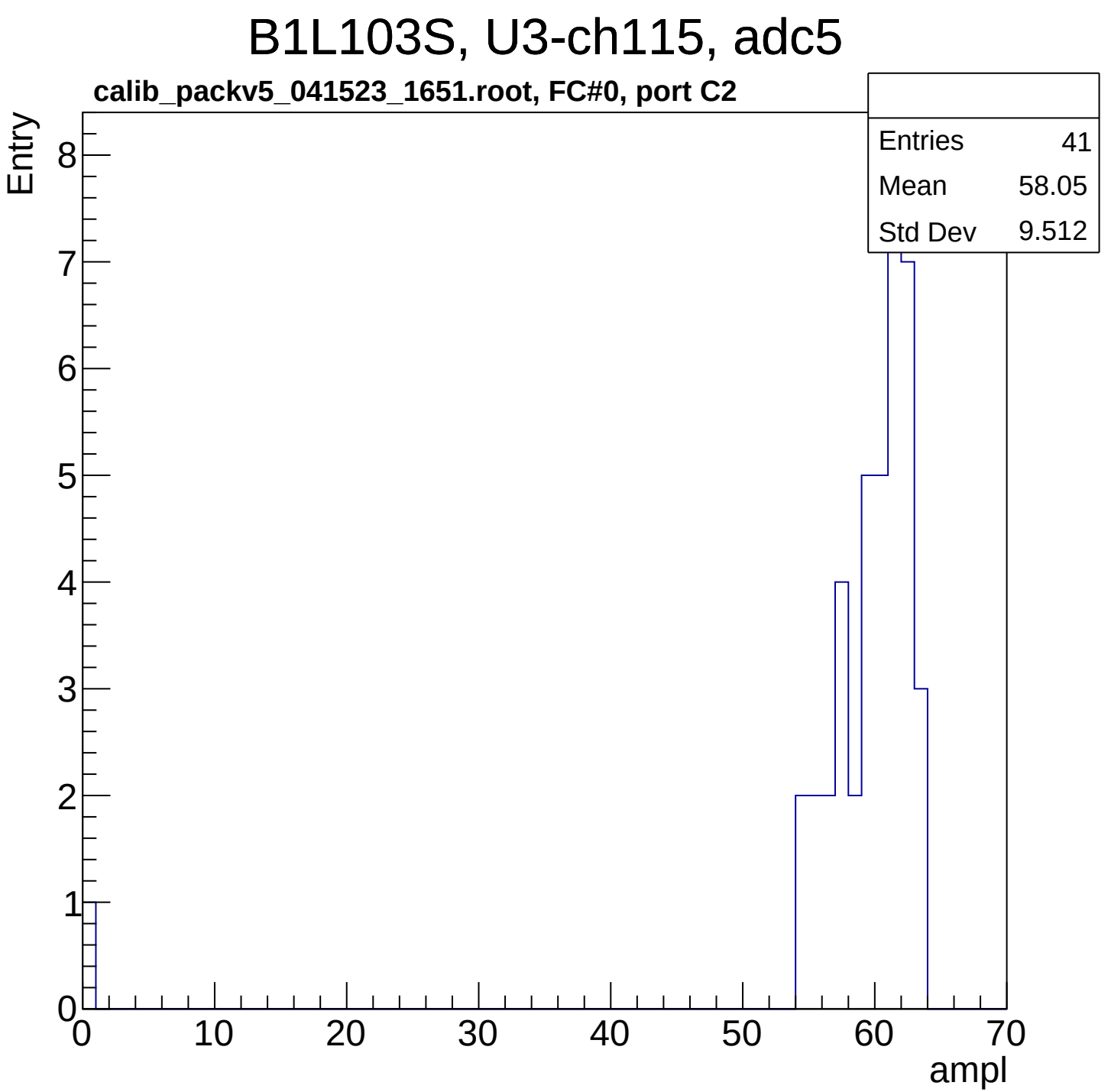
40
50
60
70


B1L103S, U3-ch115, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 58.05
Std Dev 9.512
Entry
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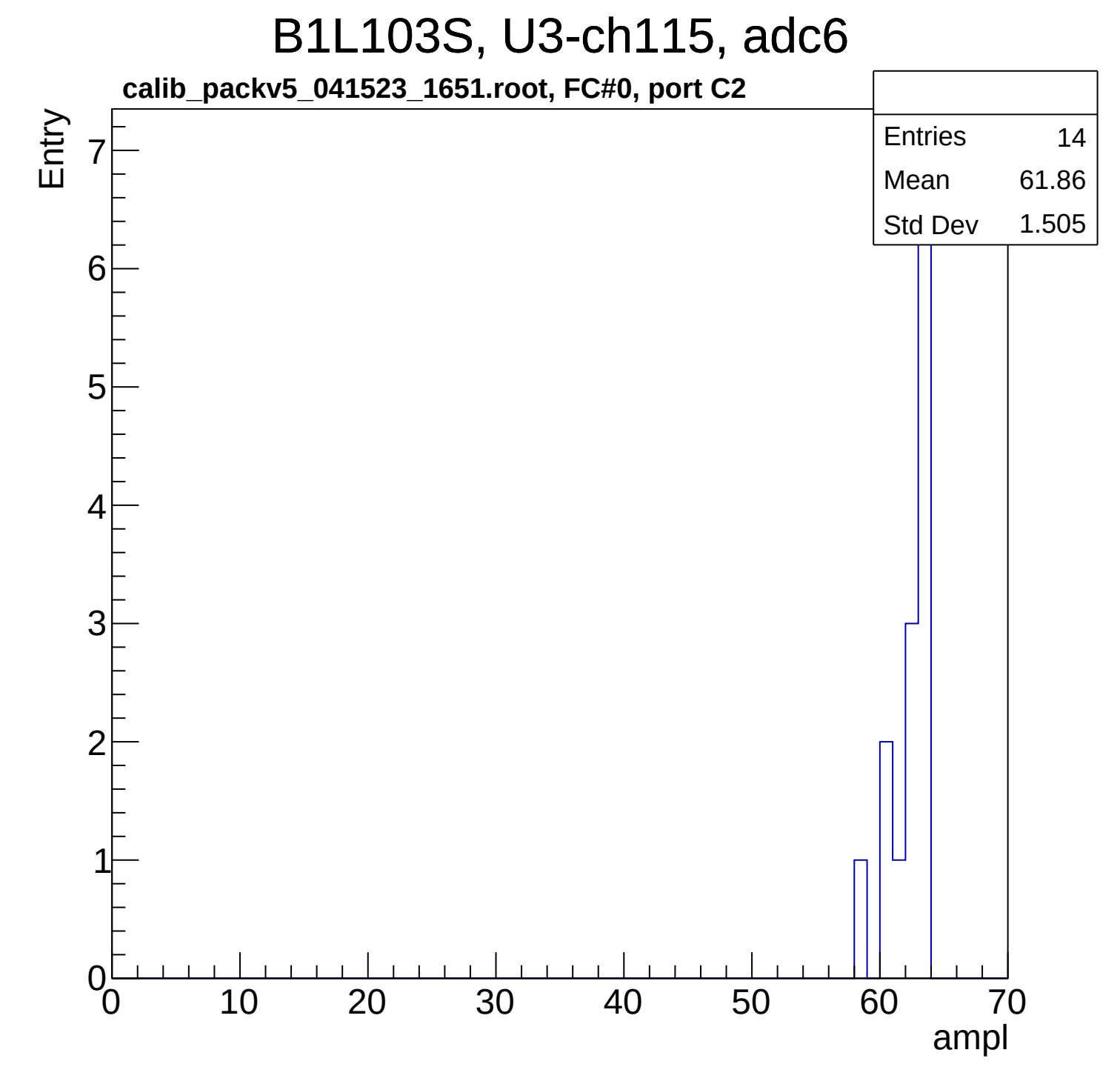
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch115, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 61.86
Std Dev 1.505
Entry
ampl
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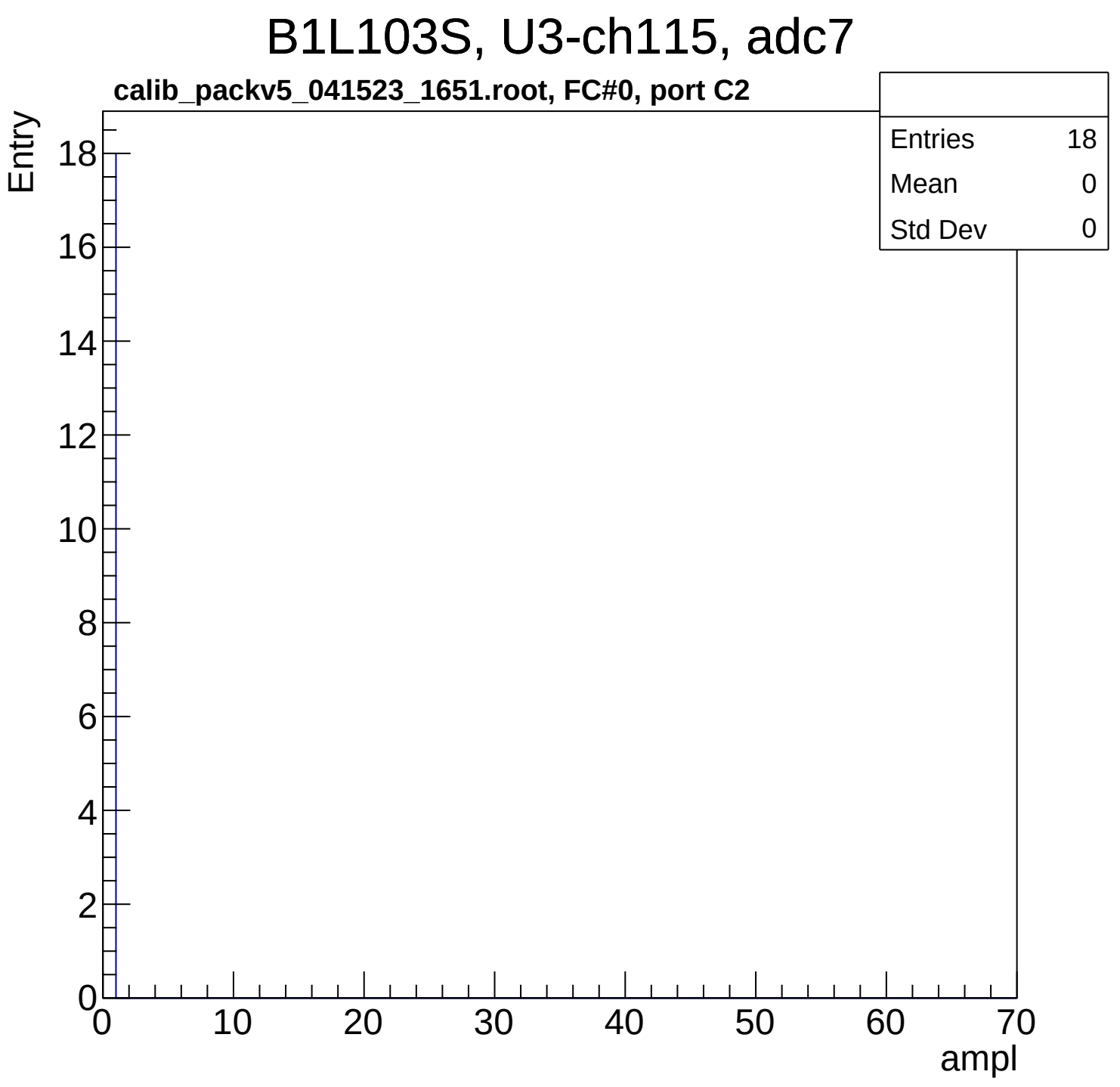
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch115, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
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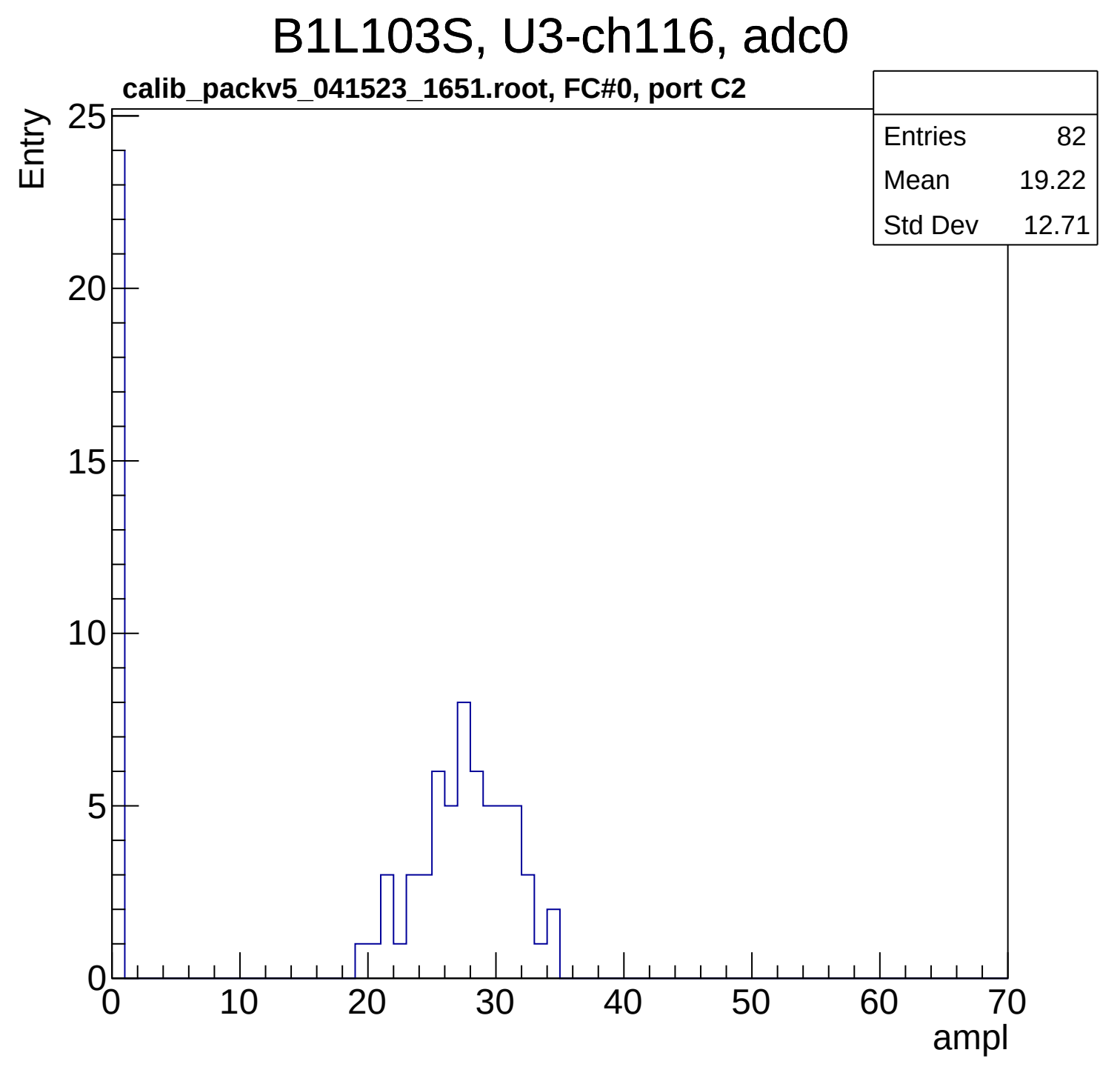
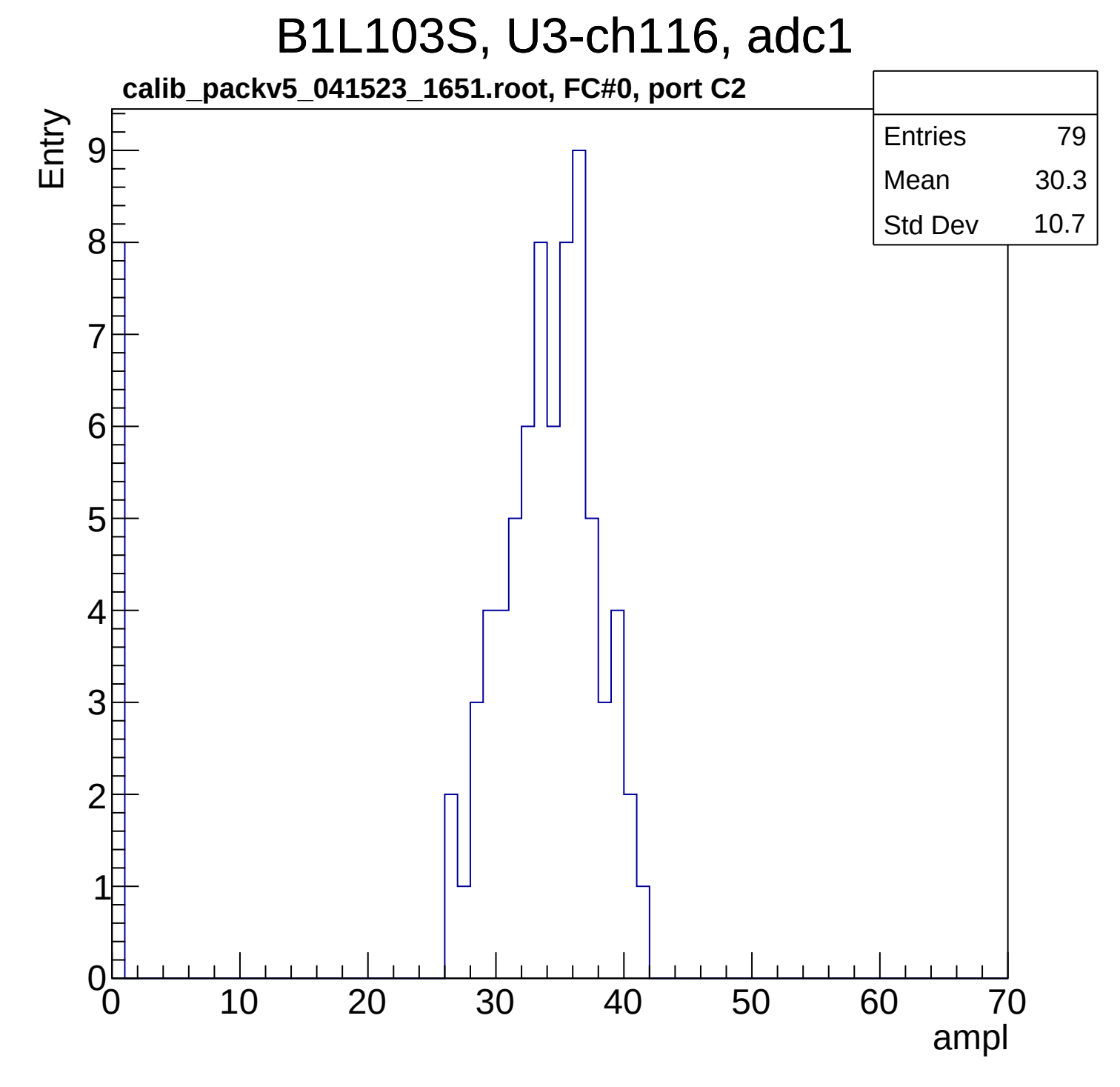
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch116, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 19.22
Std Dev 12.71
Entry
ampl
0
5
10
15
20
25
0
10
20
30
40
50
60
70


B1L103S, U3-ch116, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 30.3
Std Dev 10.7
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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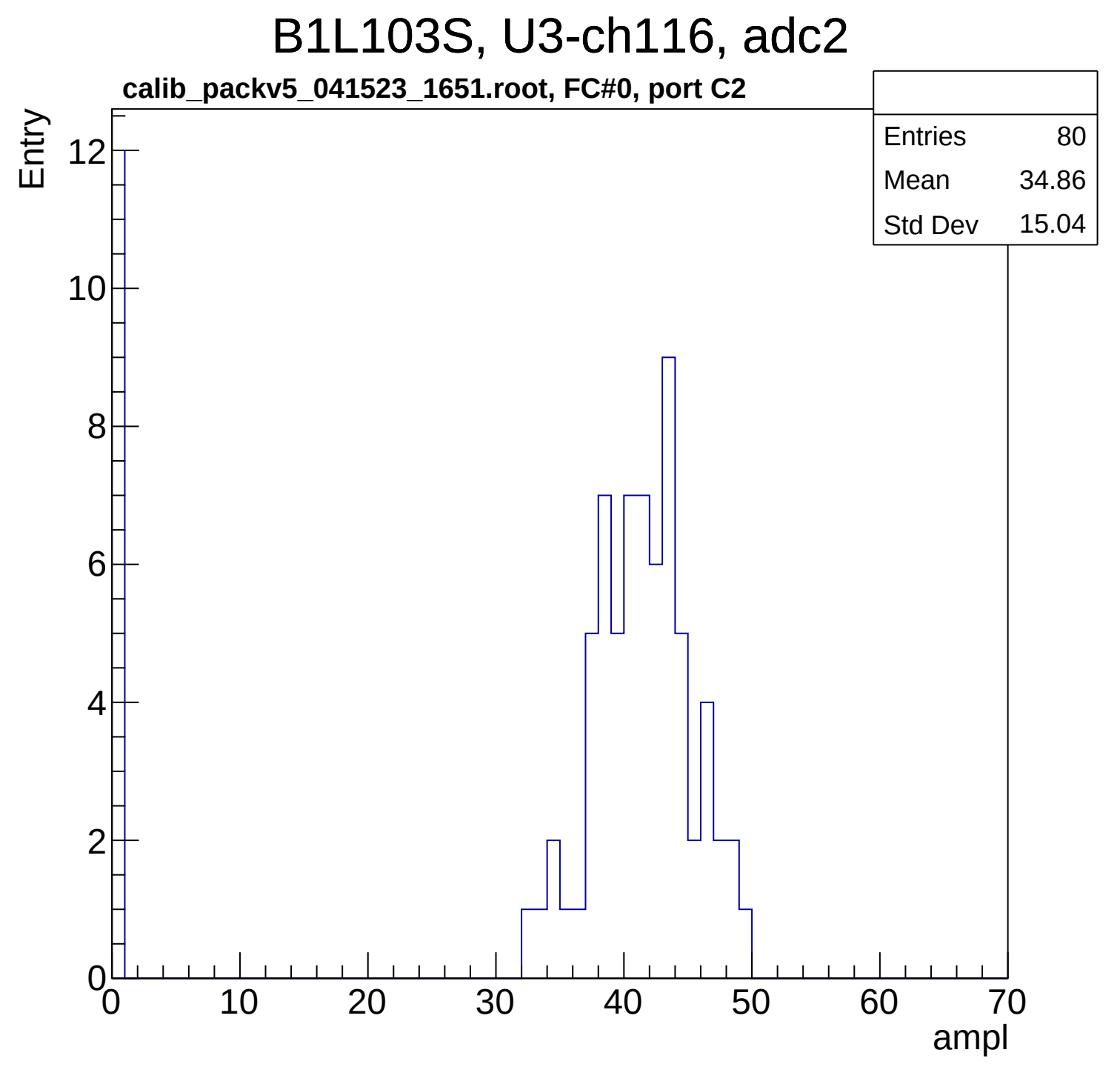
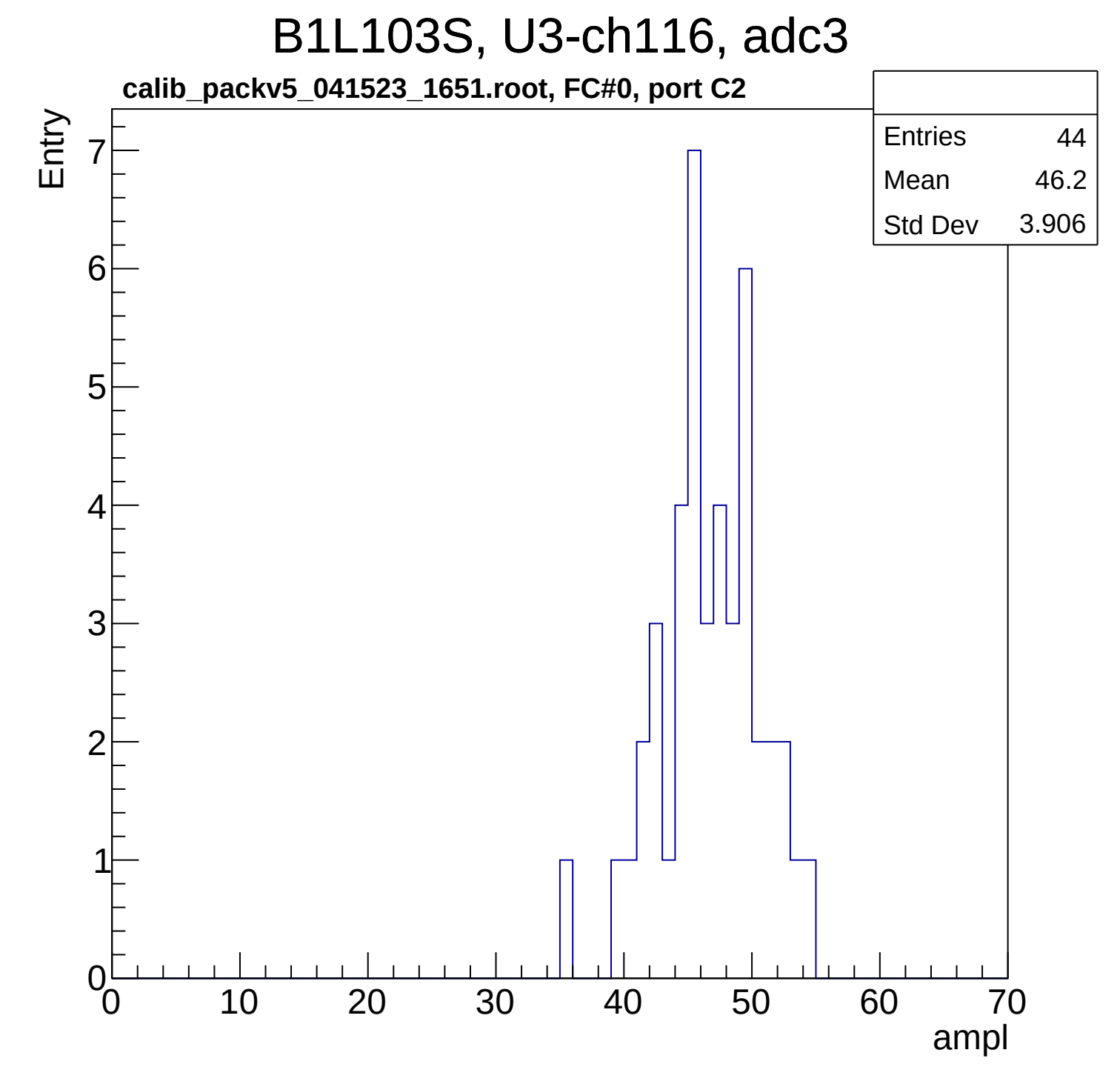

B1L103S, U3-ch116, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 34.86
Std Dev 15.04
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch116, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 46.2
Std Dev 3.906
Entry
ampl
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2
3
4
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0
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60
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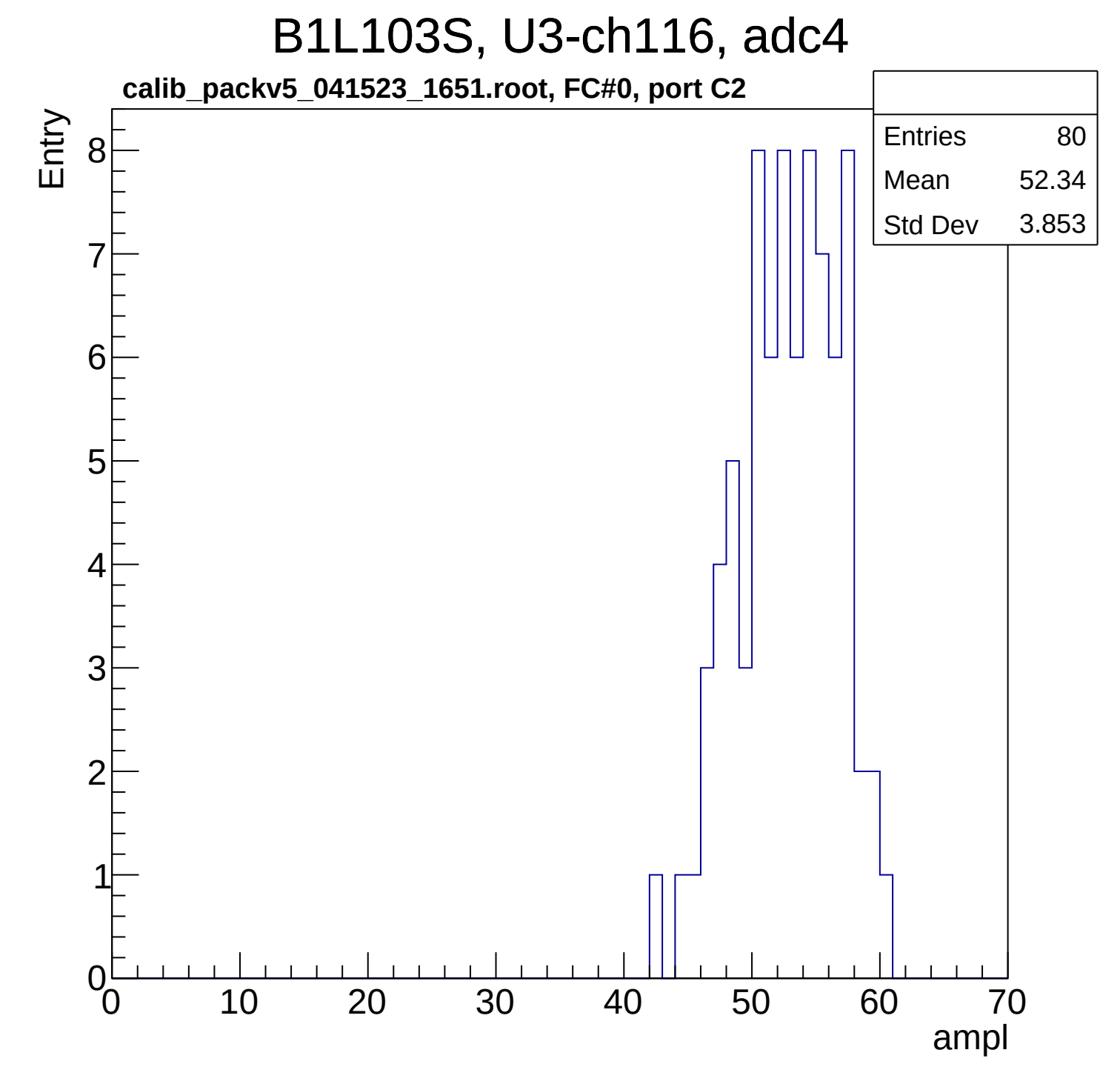
B1L103S, U3-ch116, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 52.34
Std Dev 3.853
Entry
ampl
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2
3
4
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7
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0
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40
50
60
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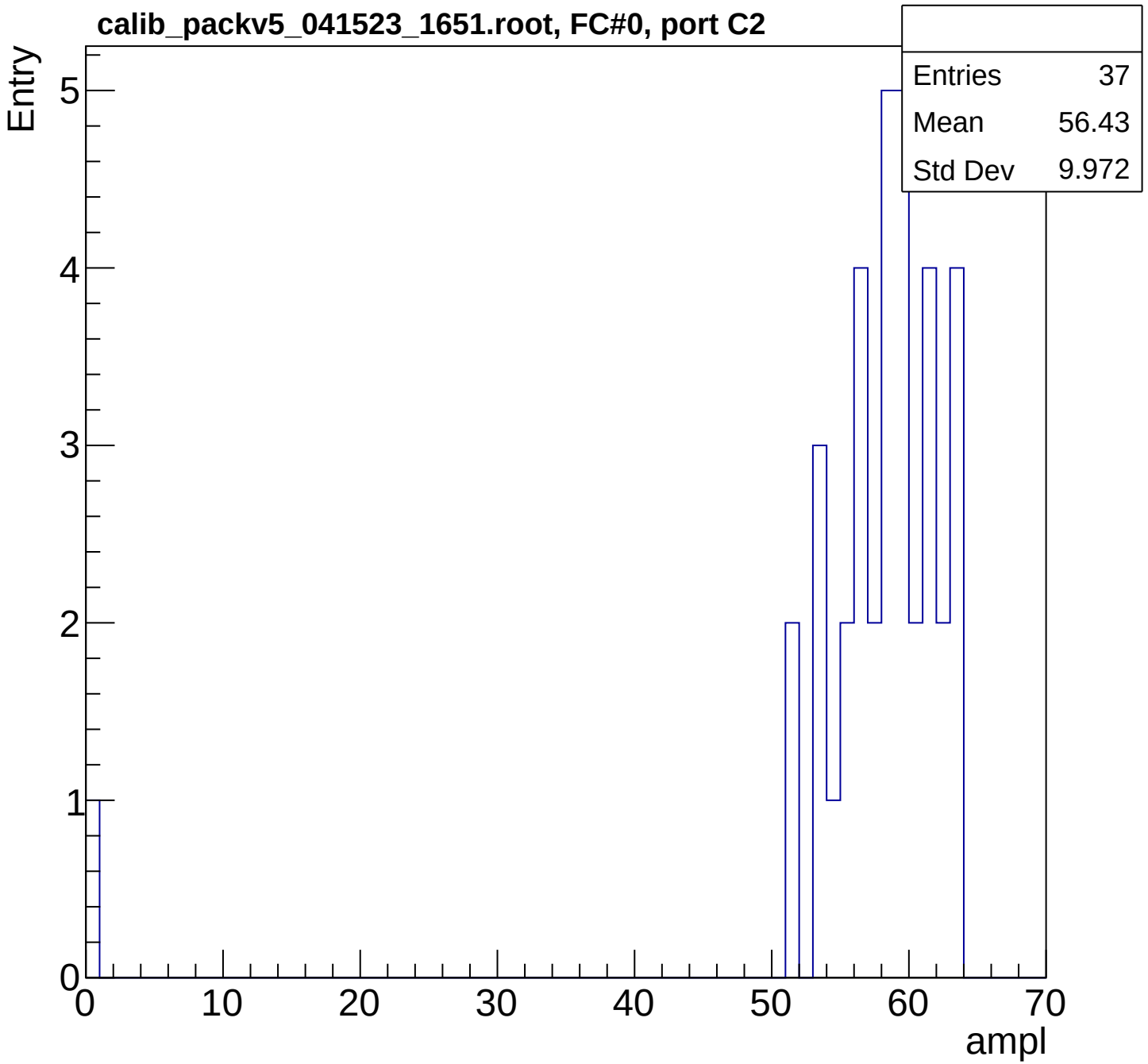
B1L103S, U3-ch116, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 56.43
Std Dev 9.972
Entry
ampl
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1
2
3
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0
10
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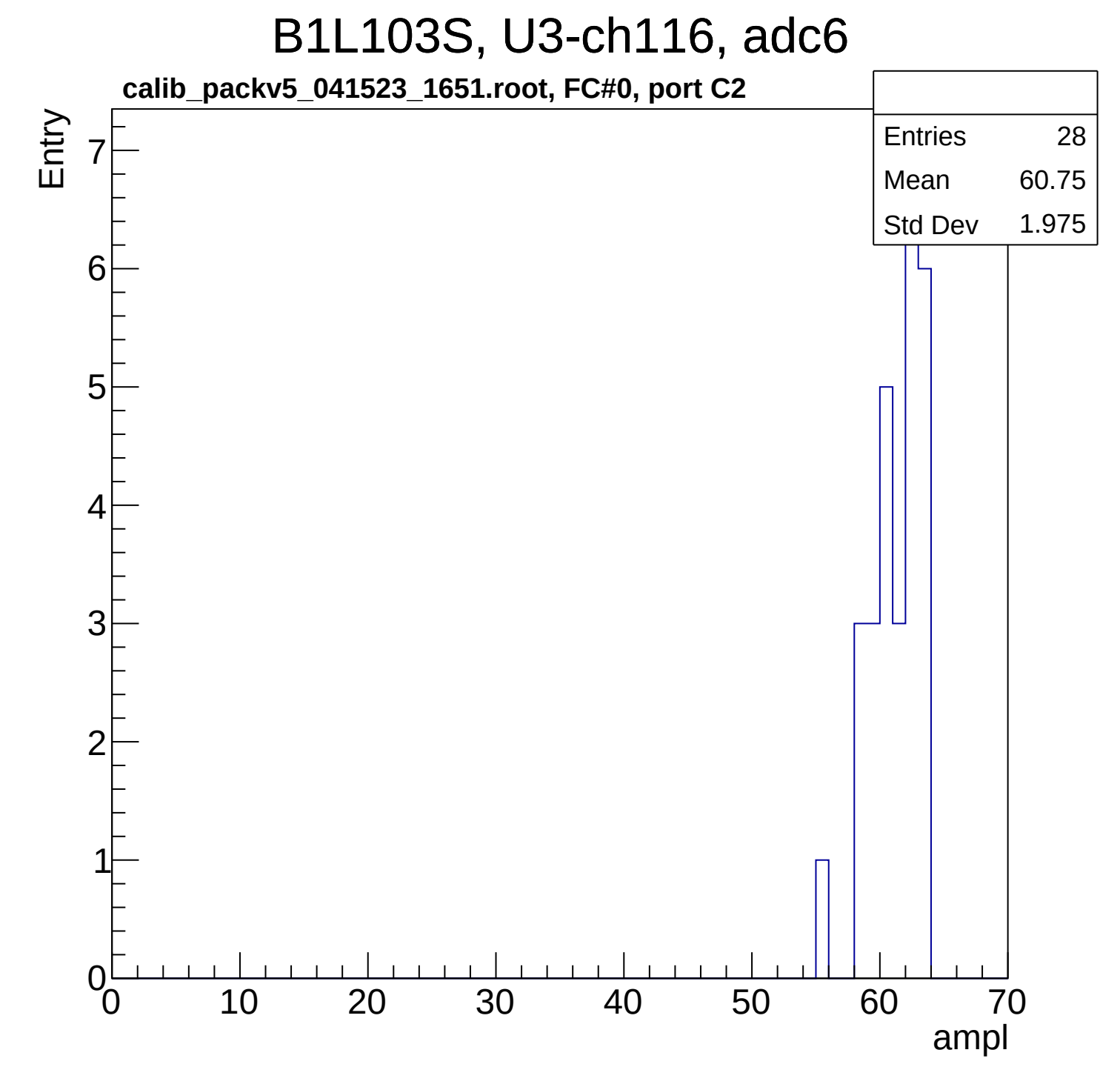
40
50
60
70


B1L103S, U3-ch116, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 60.75
Std Dev 1.975
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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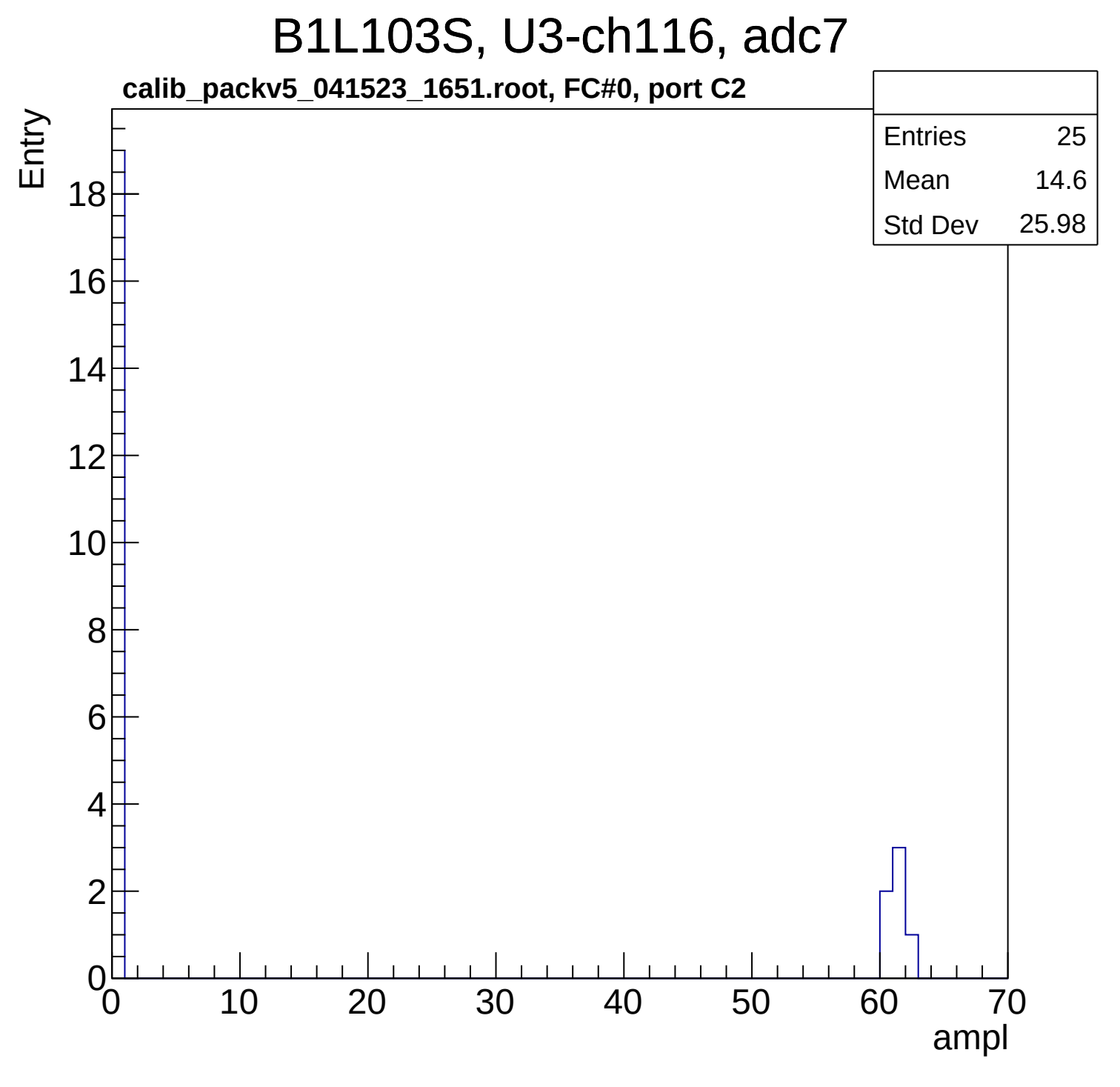
40
50
60
70


B1L103S, U3-ch116, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 14.6
Std Dev 25.98
Entry
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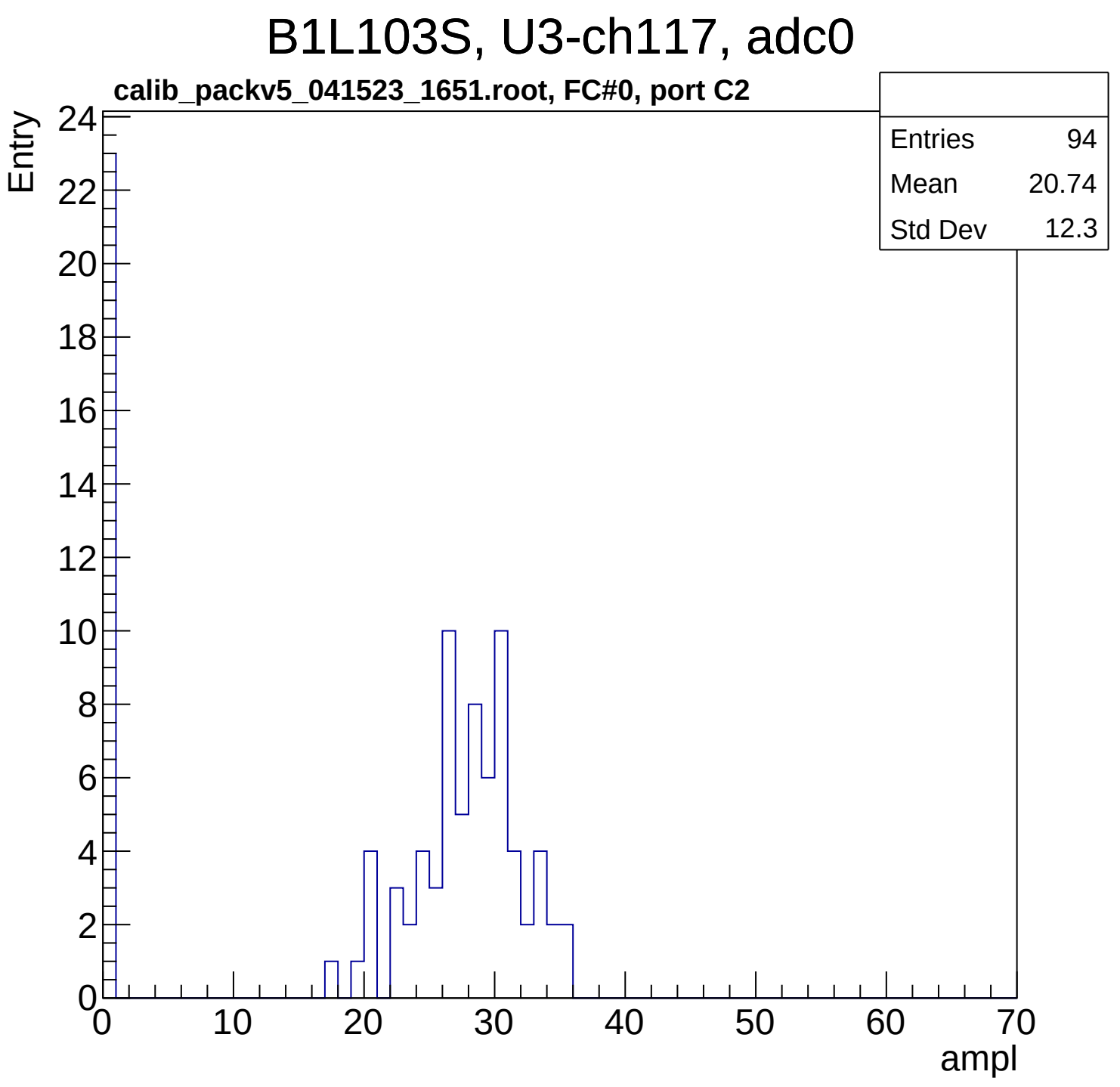
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch117, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 20.74
Std Dev 12.3
Entry
ampl
0
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4
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8
10
12
14
16
18
20
22
24
0
10
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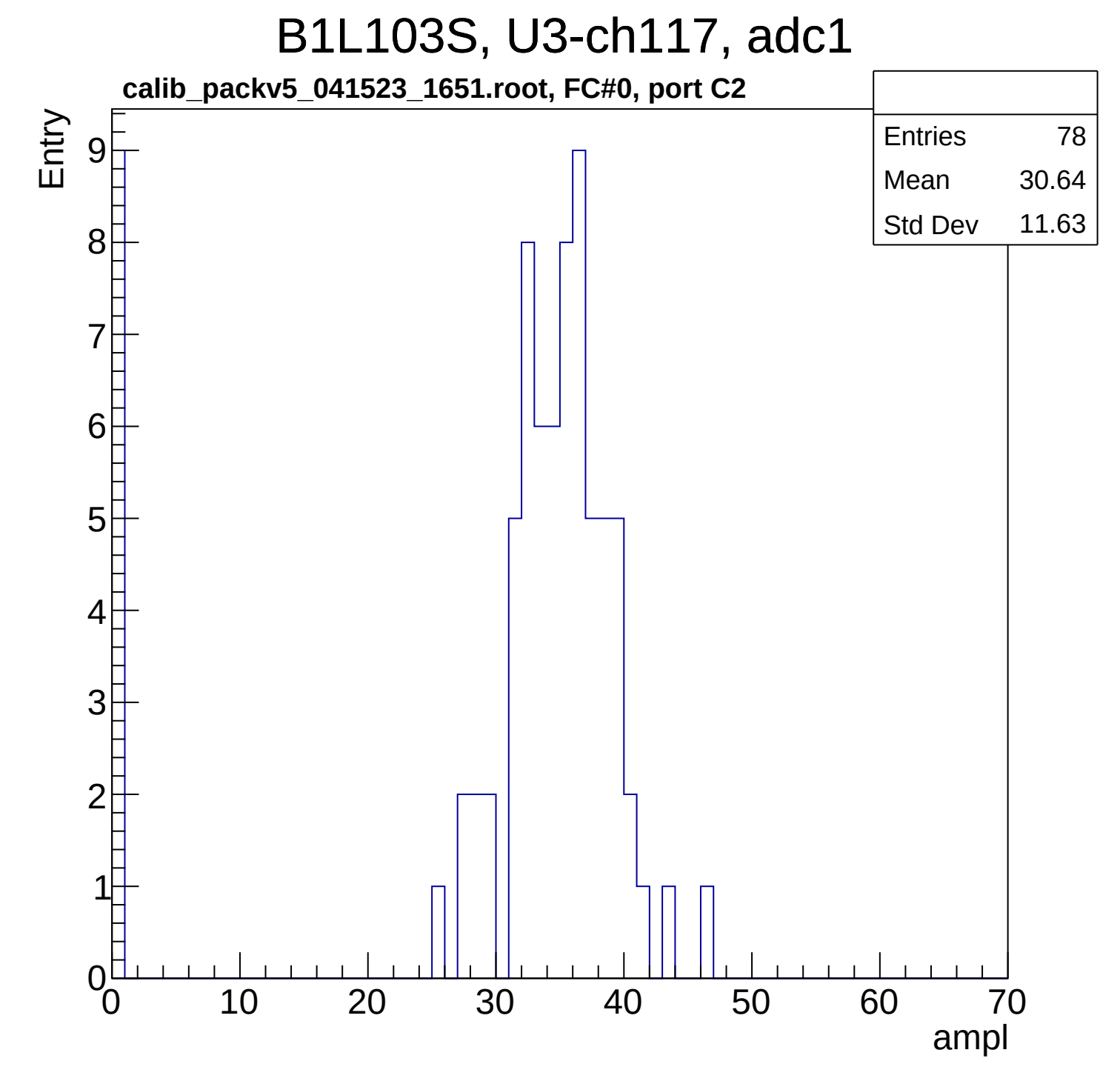
40
50
60
70


B1L103S, U3-ch117, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 30.64
Std Dev 11.63
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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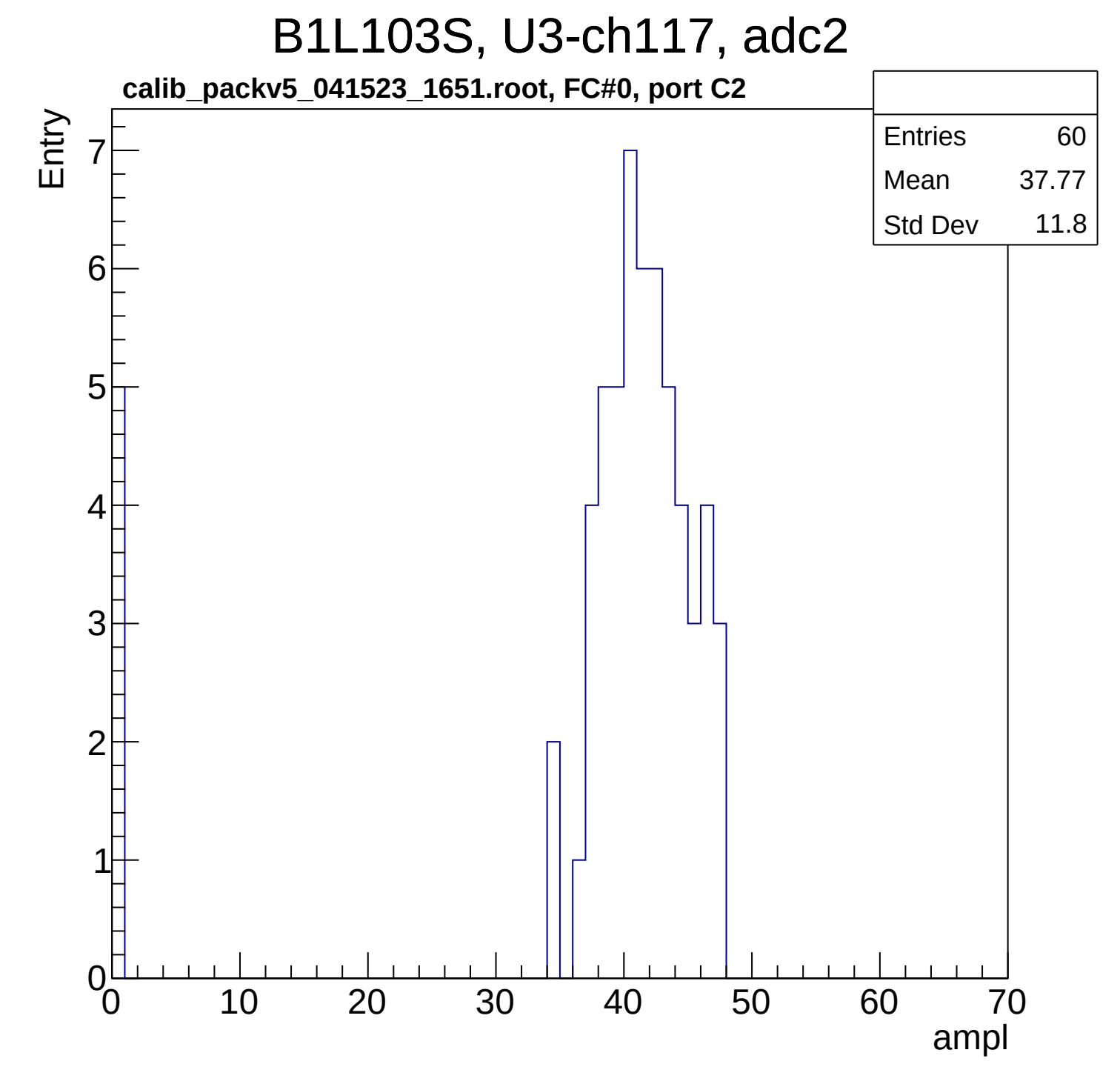
B1L103S, U3-ch117, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 37.77
Std Dev 11.8
Entry
ampl
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1
2
3
4
5
6
7
0
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20
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40
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60
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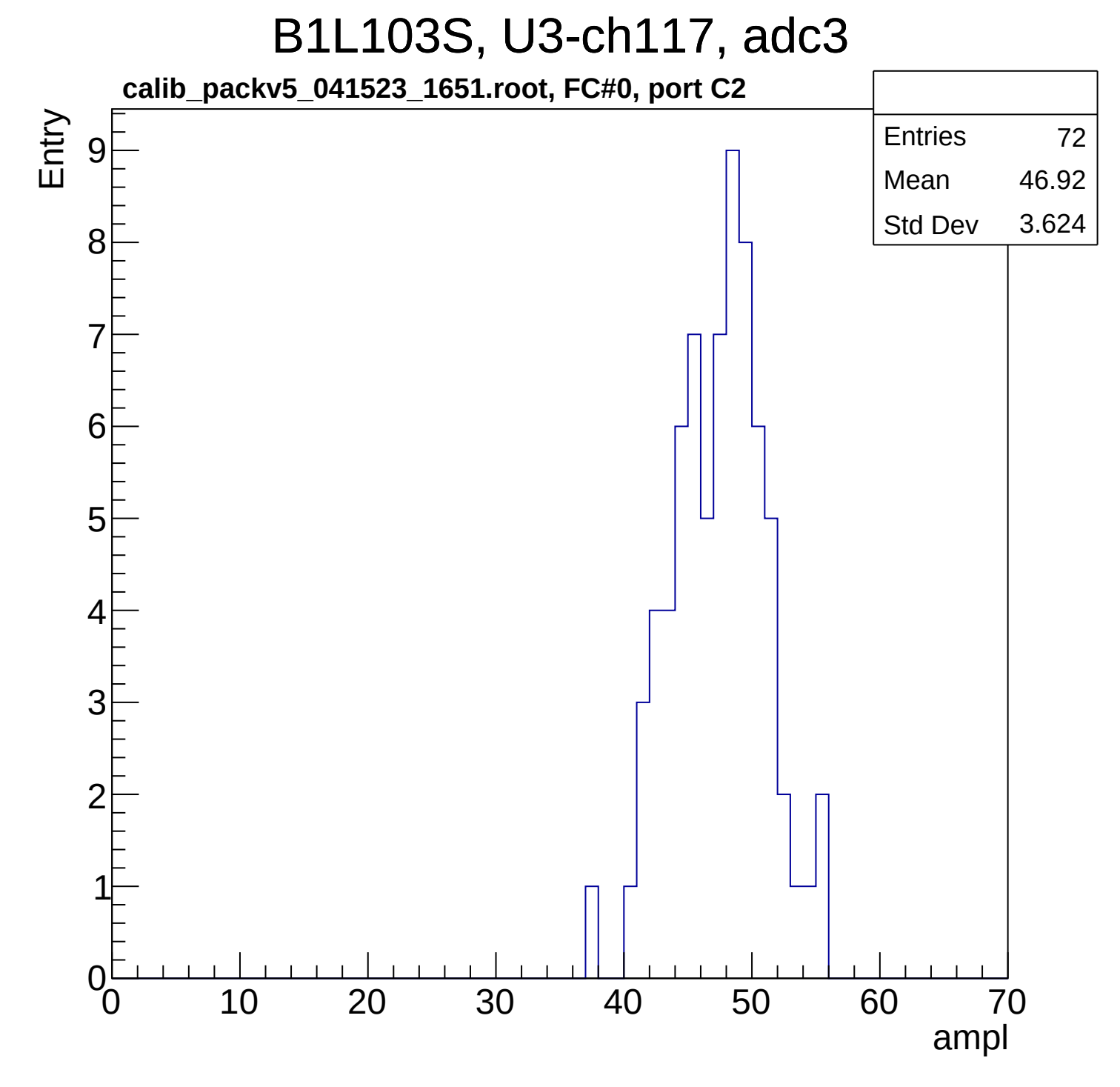
B1L103S, U3-ch117, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 46.92
Std Dev 3.624
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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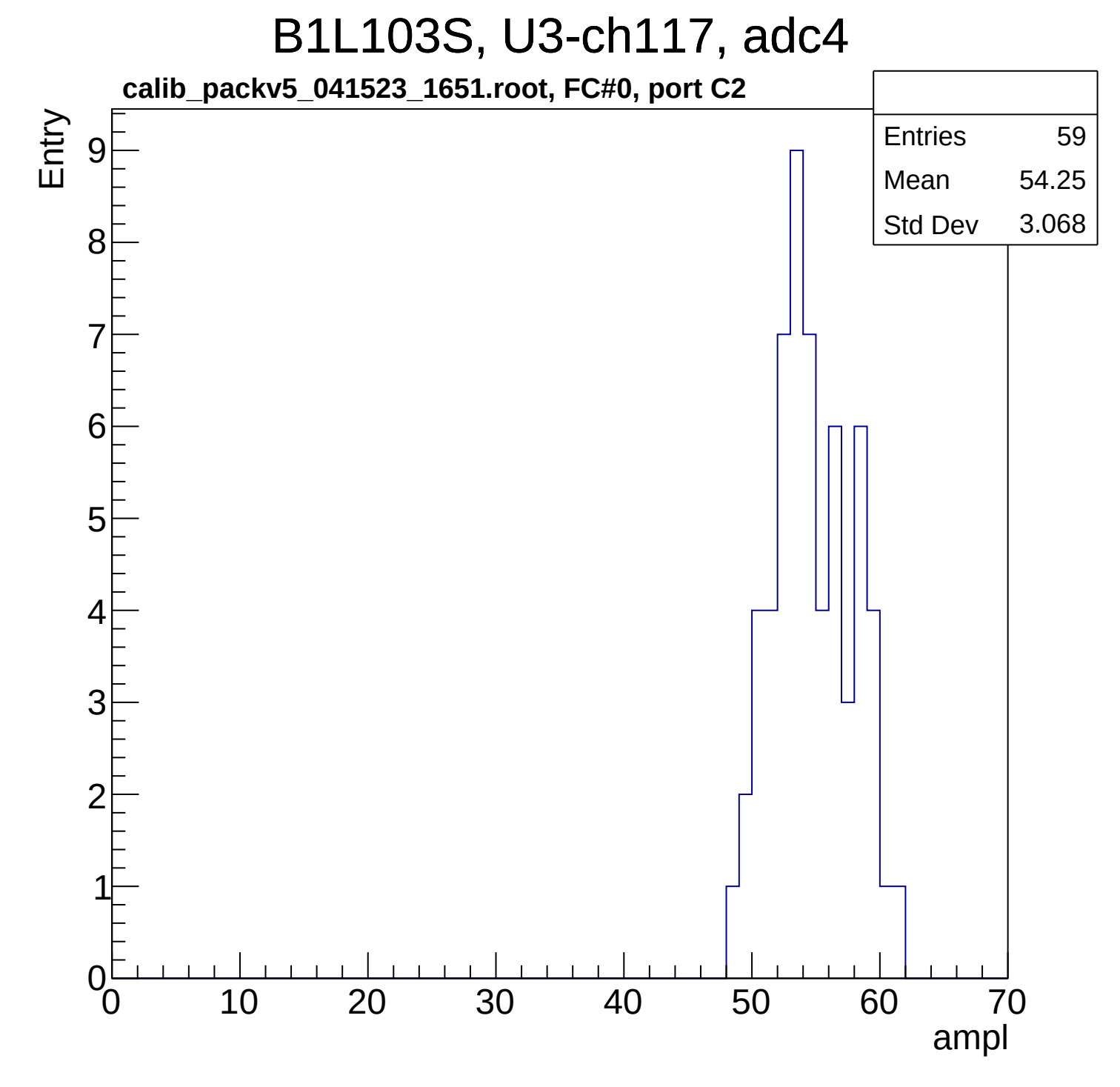
B1L103S, U3-ch117, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 54.25
Std Dev 3.068
Entry
ampl
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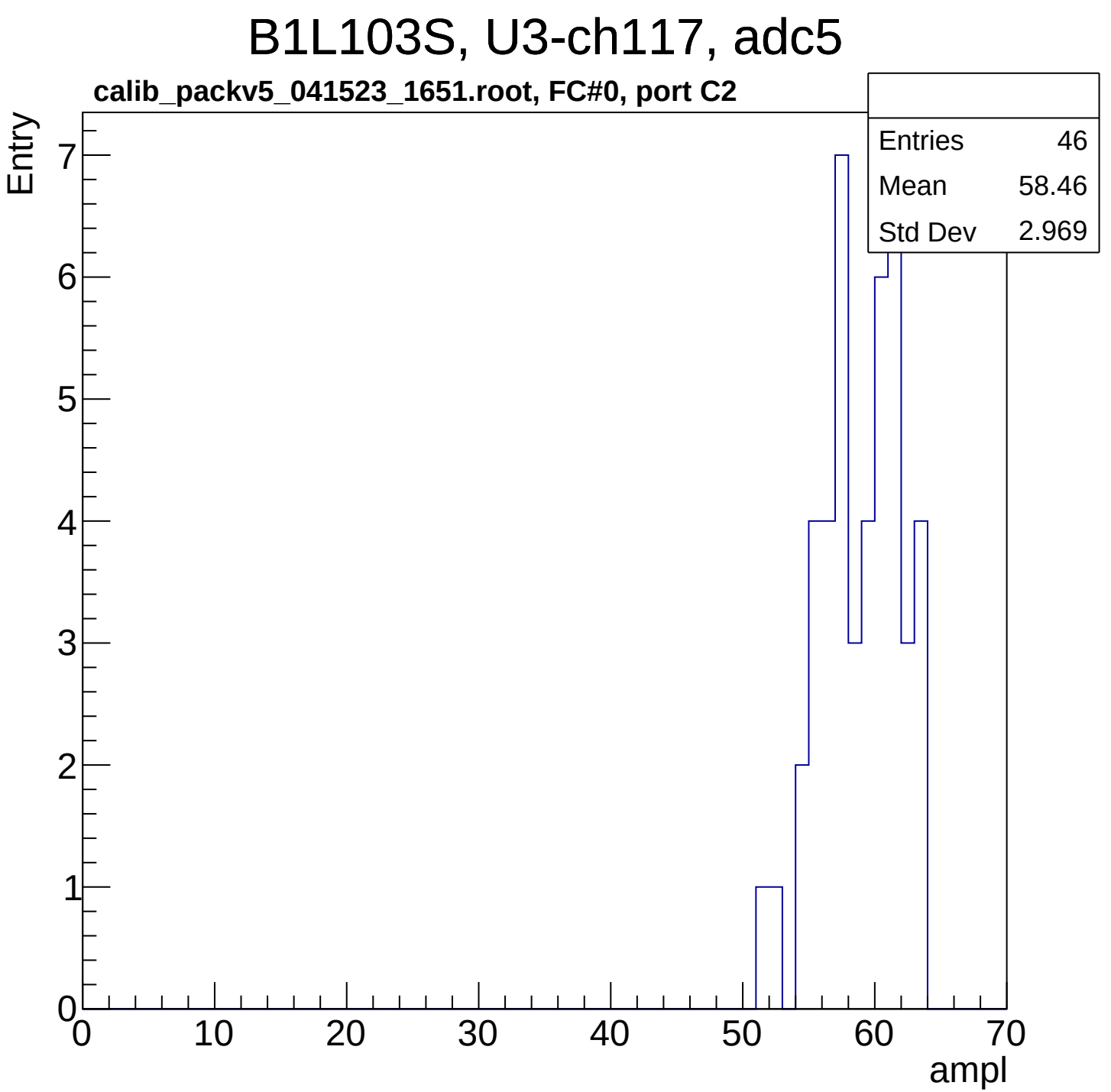
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch117, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 58.46
Std Dev 2.969
Entry
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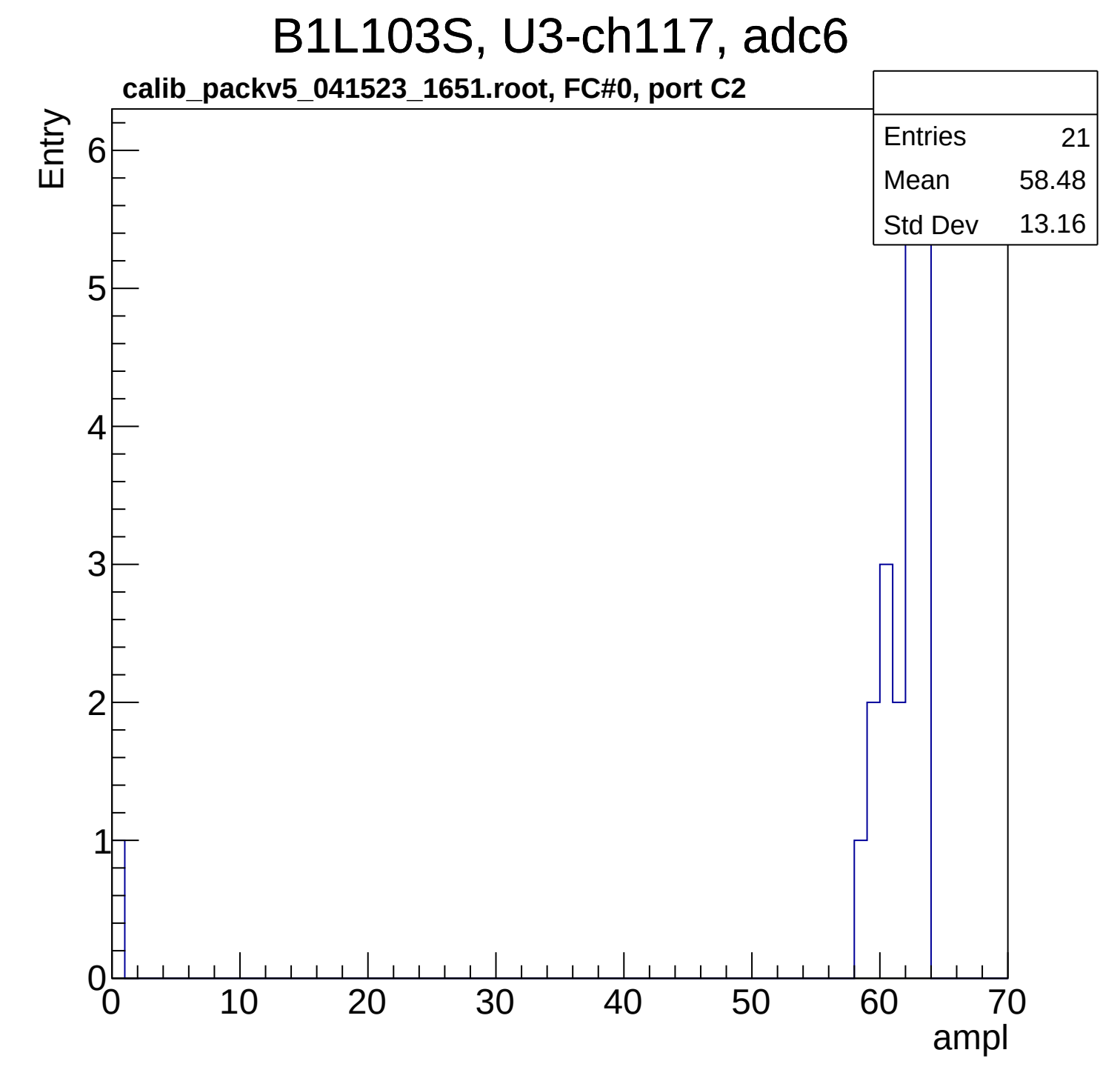
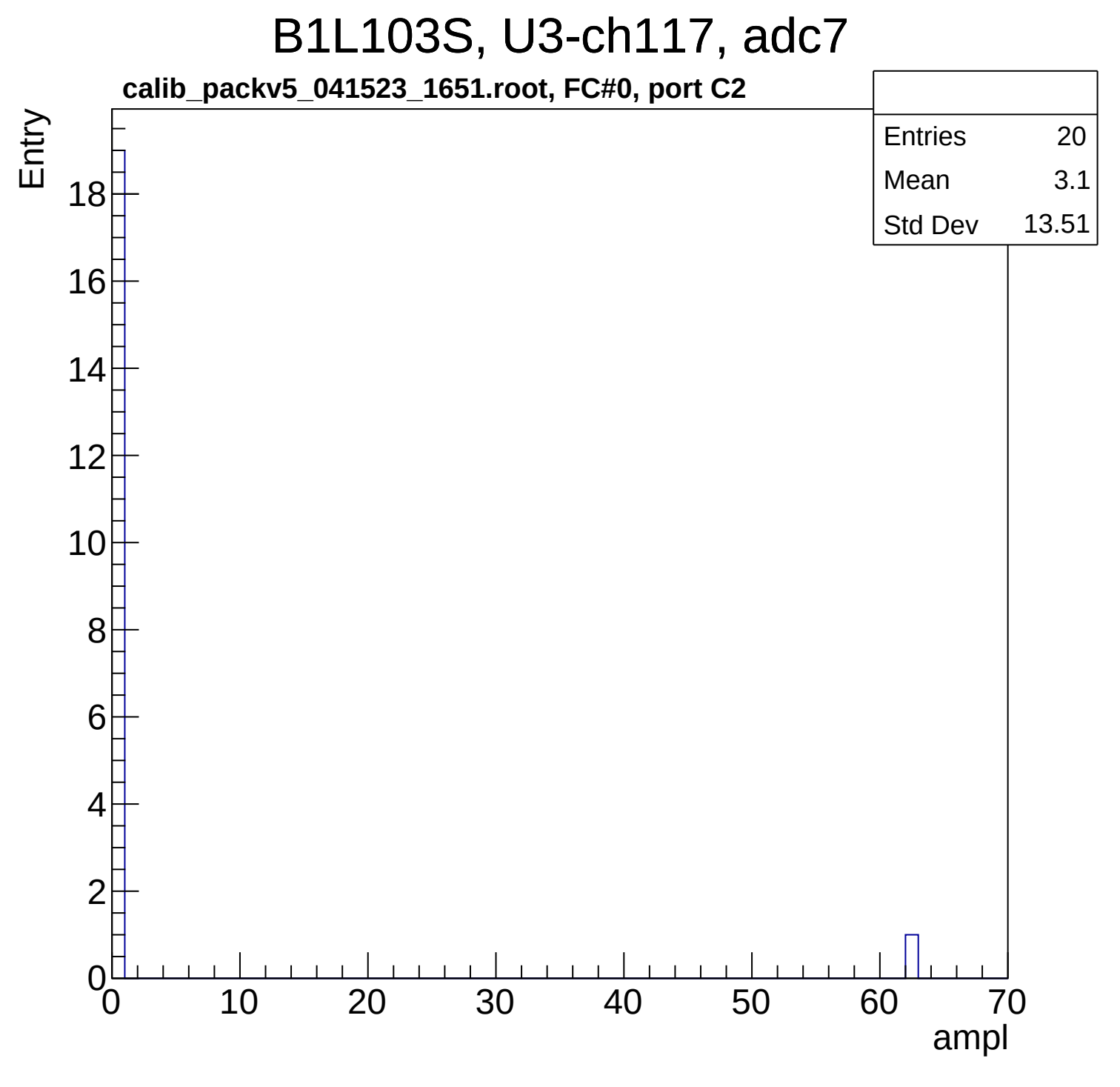
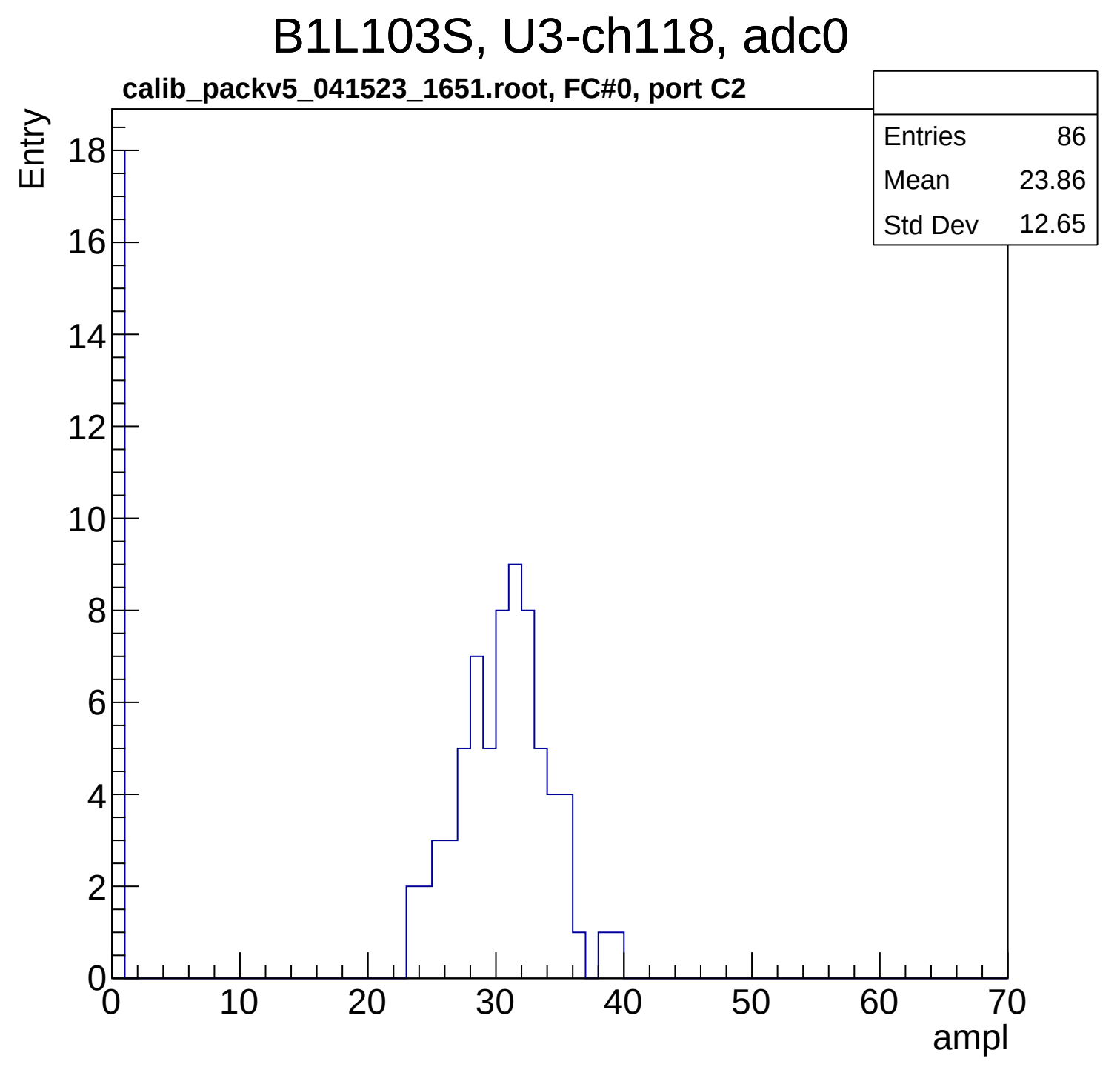
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch117, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 58.48
Std Dev 13.16
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch117, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch118, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 23.86
Std Dev 12.65
Entry
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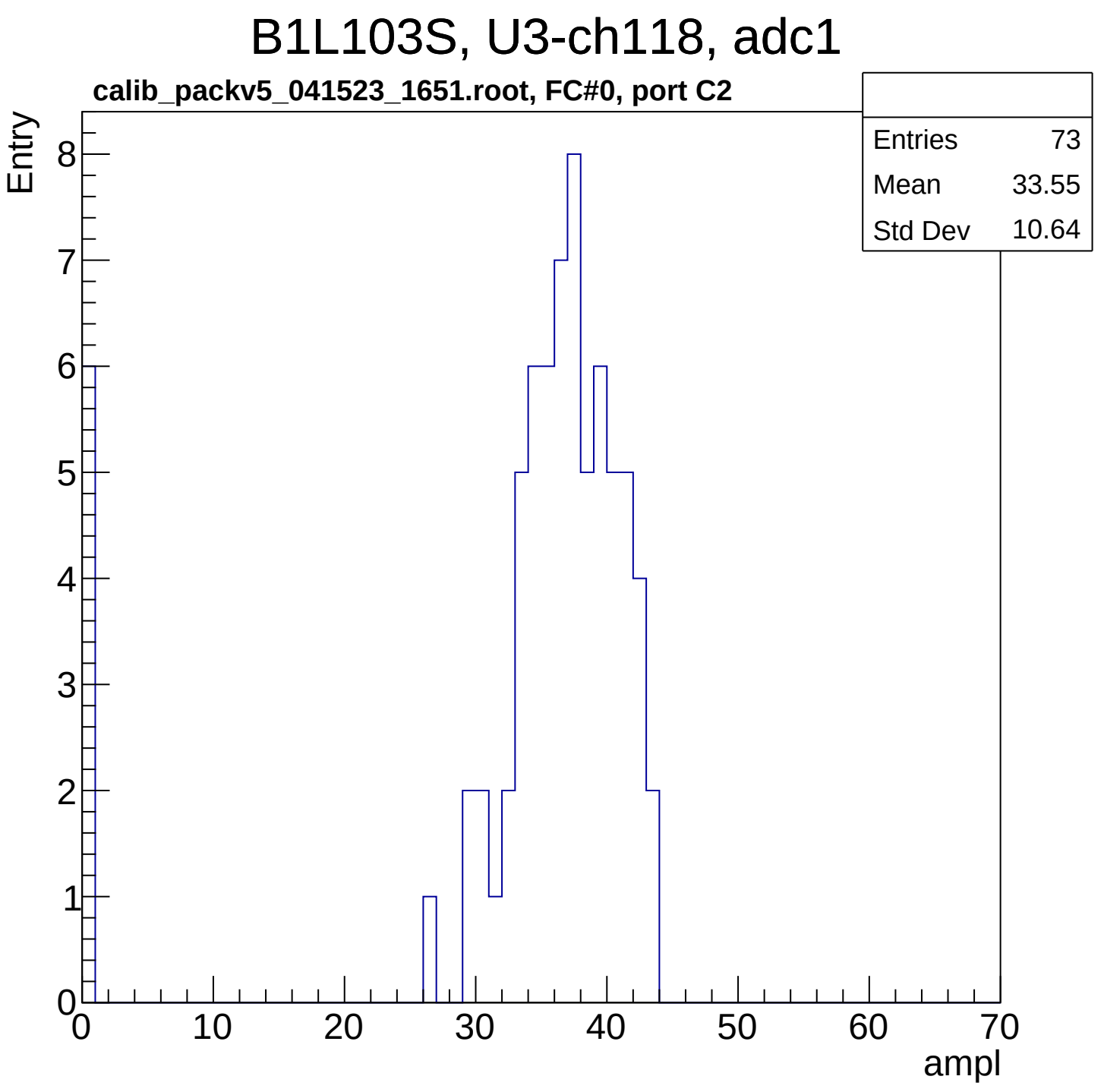
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch118, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 33.55
Std Dev 10.64
Entry
ampl
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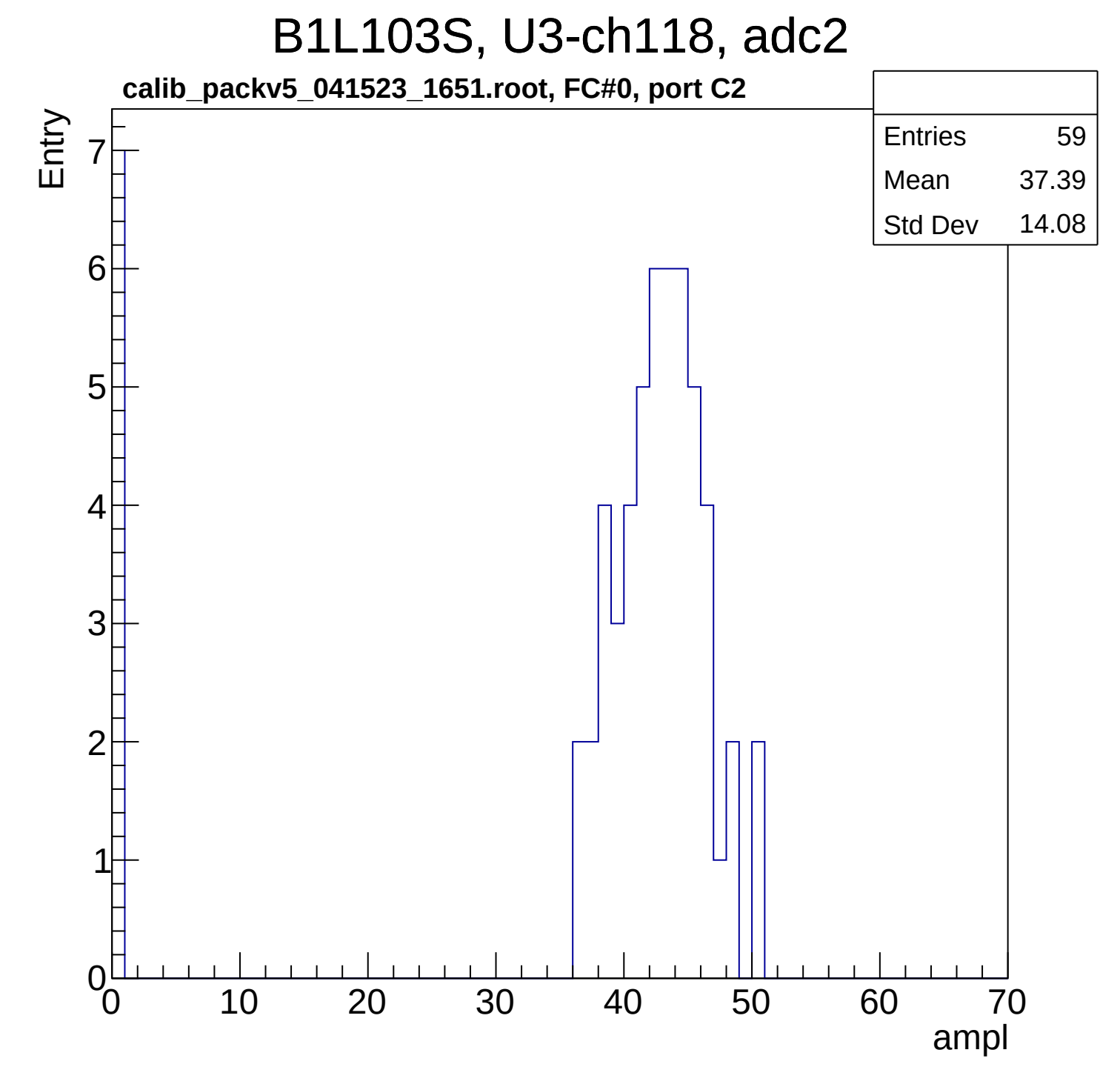
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch118, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 37.39
Std Dev 14.08
Entry
ampl
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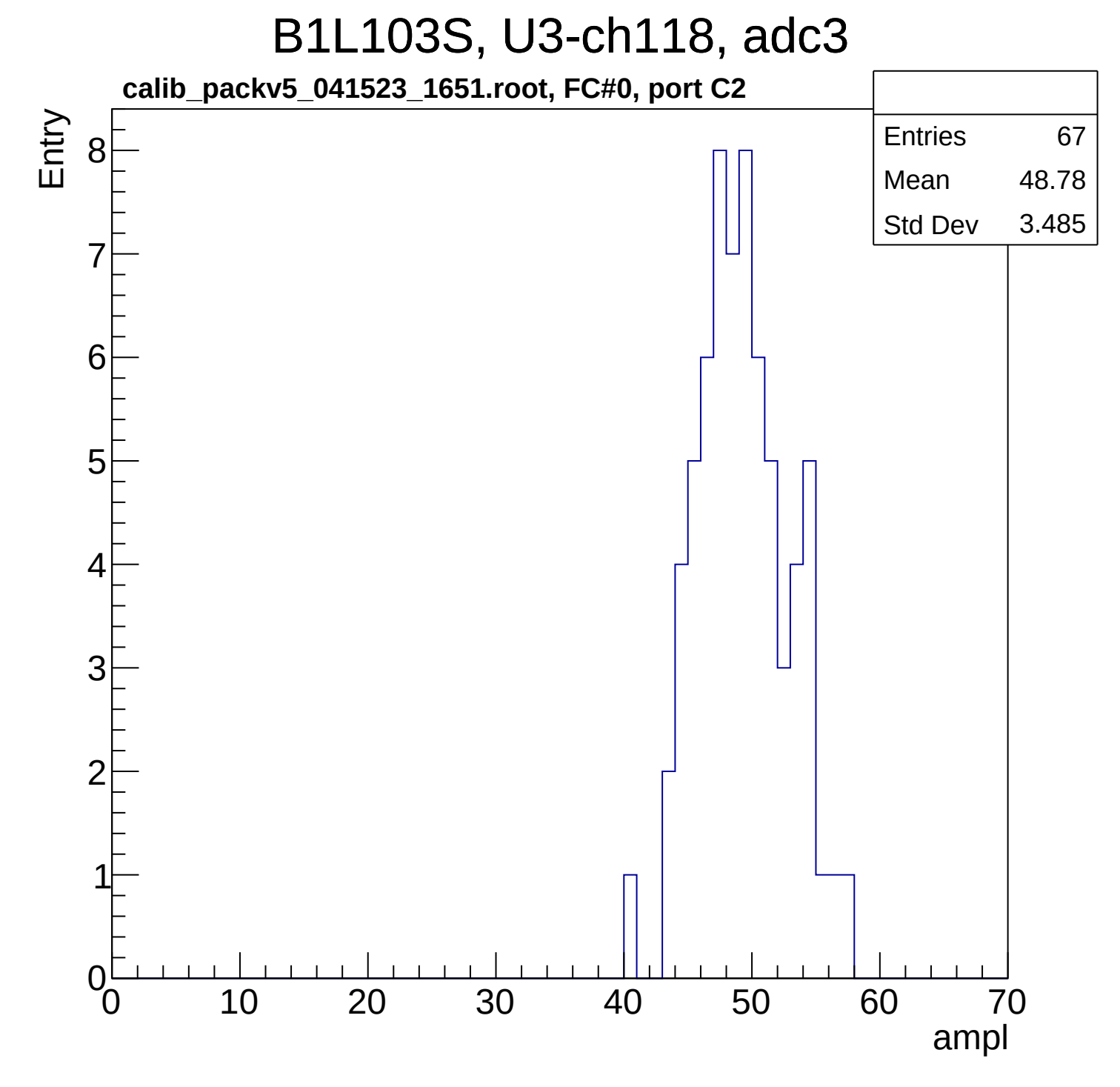
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch118, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 48.78
Std Dev 3.485
Entry
ampl
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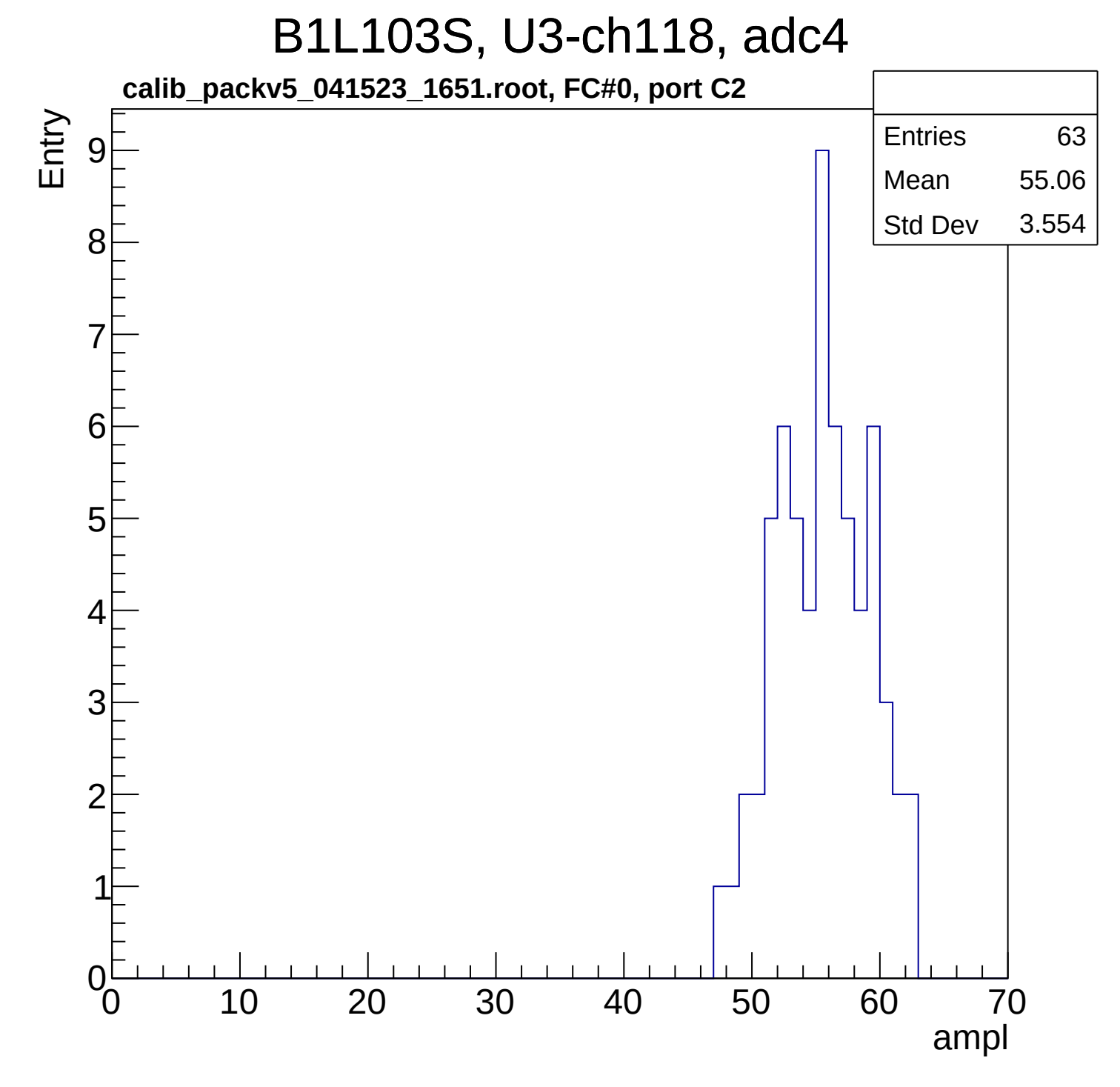
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch118, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 55.06
Std Dev 3.554
Entry
ampl
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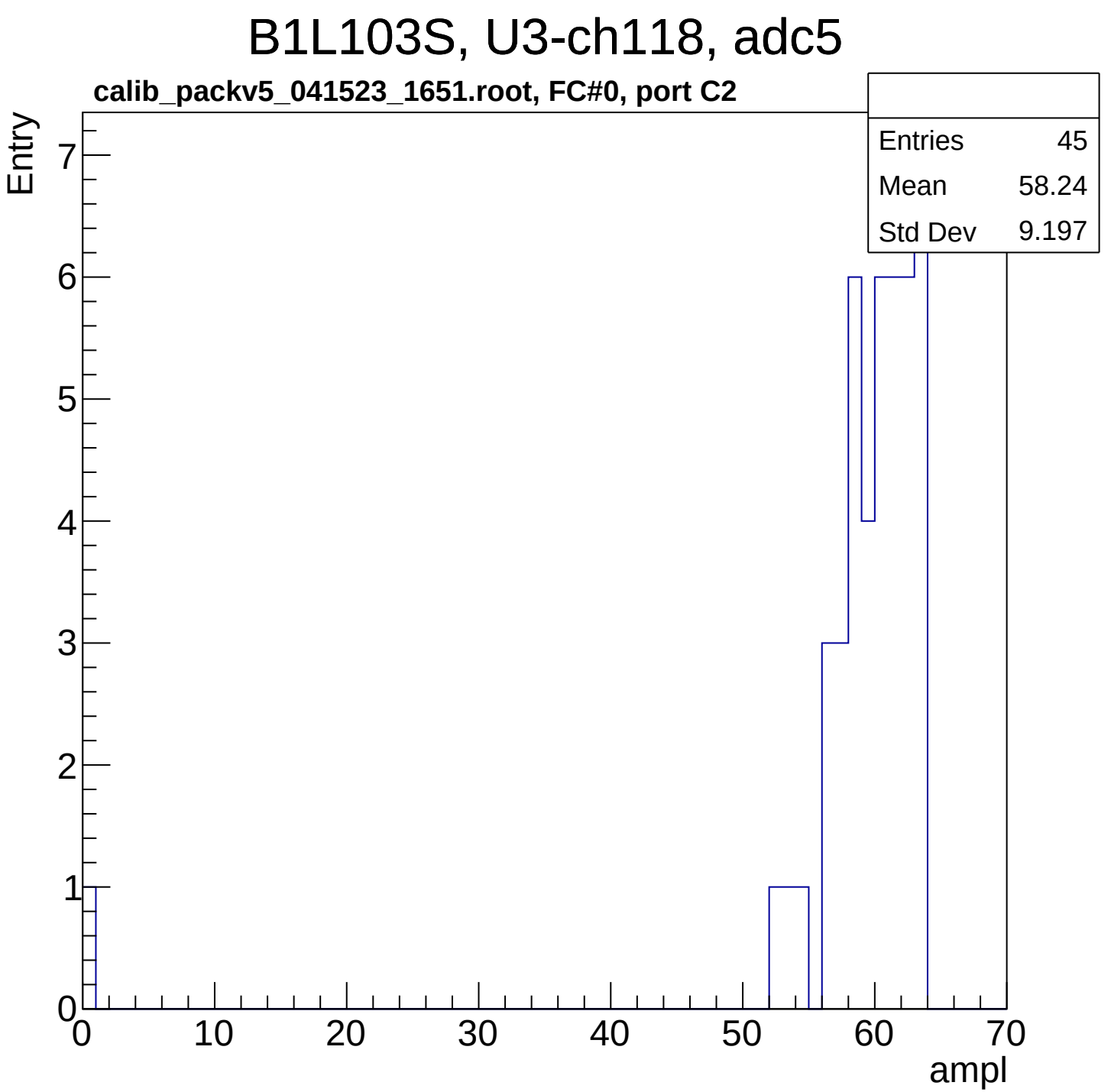
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch118, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 58.24
Std Dev 9.197
Entry
ampl
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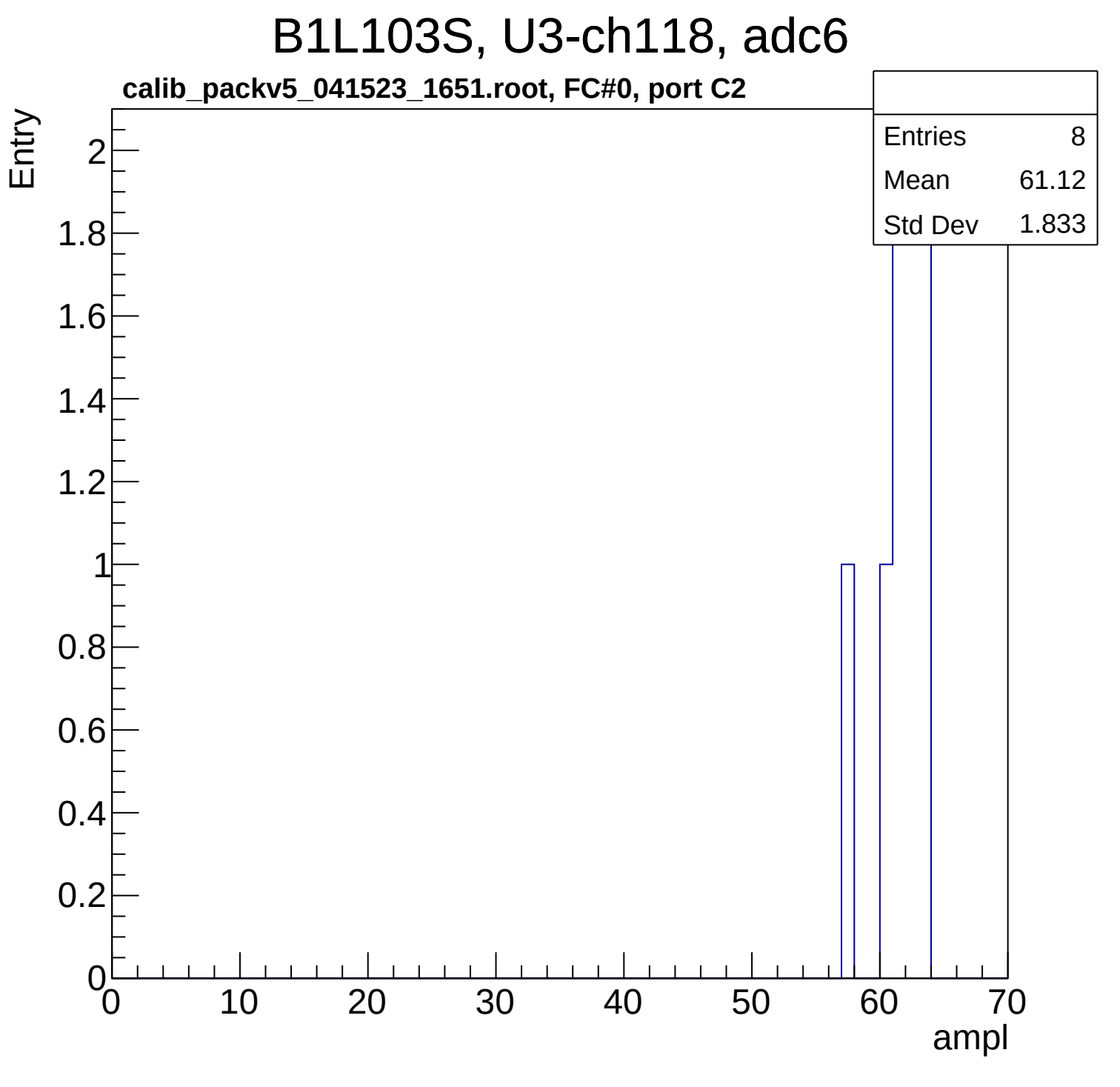
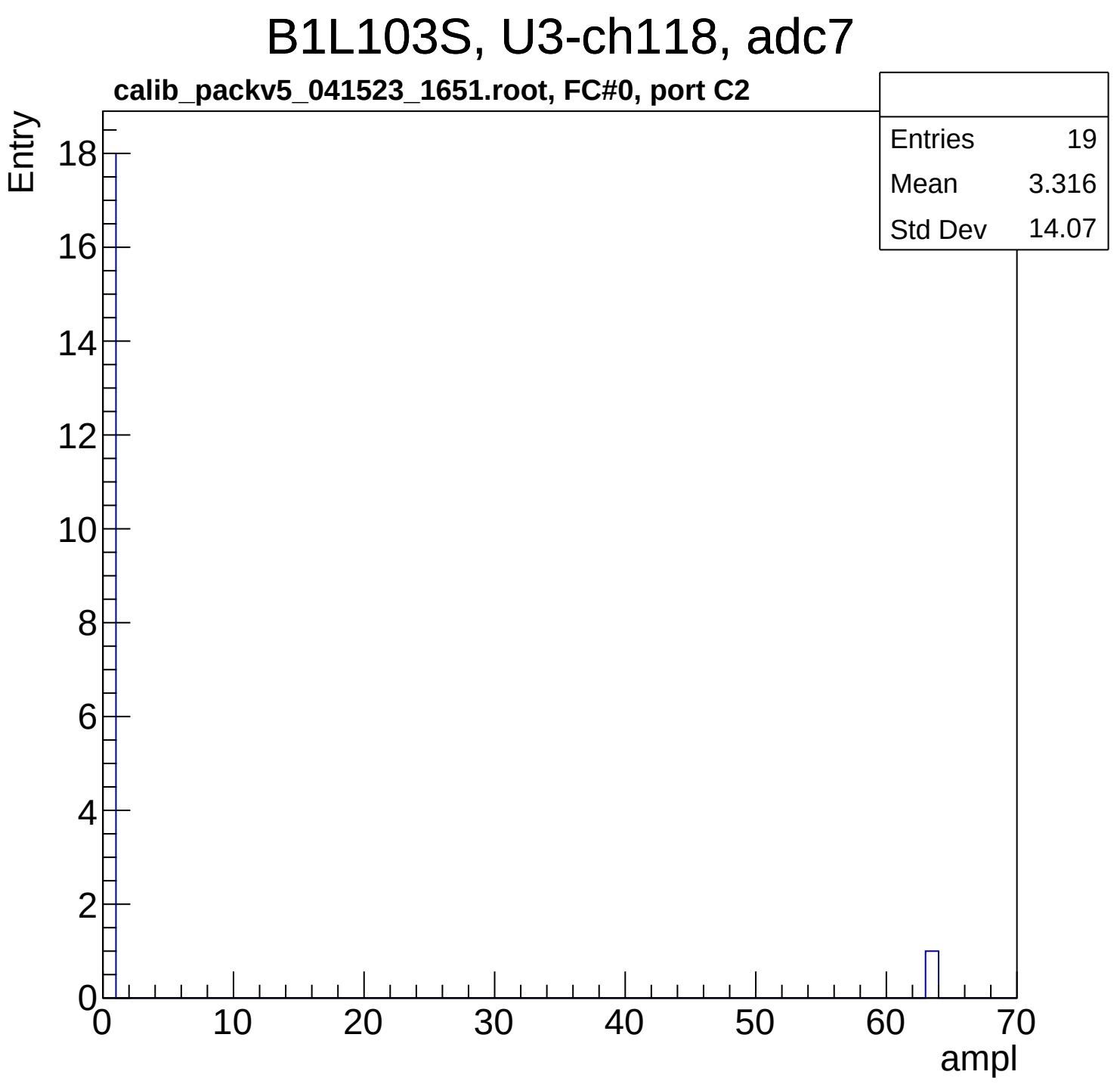
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch118, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 61.12
Std Dev 1.833
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U3-ch118, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.316
Std Dev 14.07
Entry
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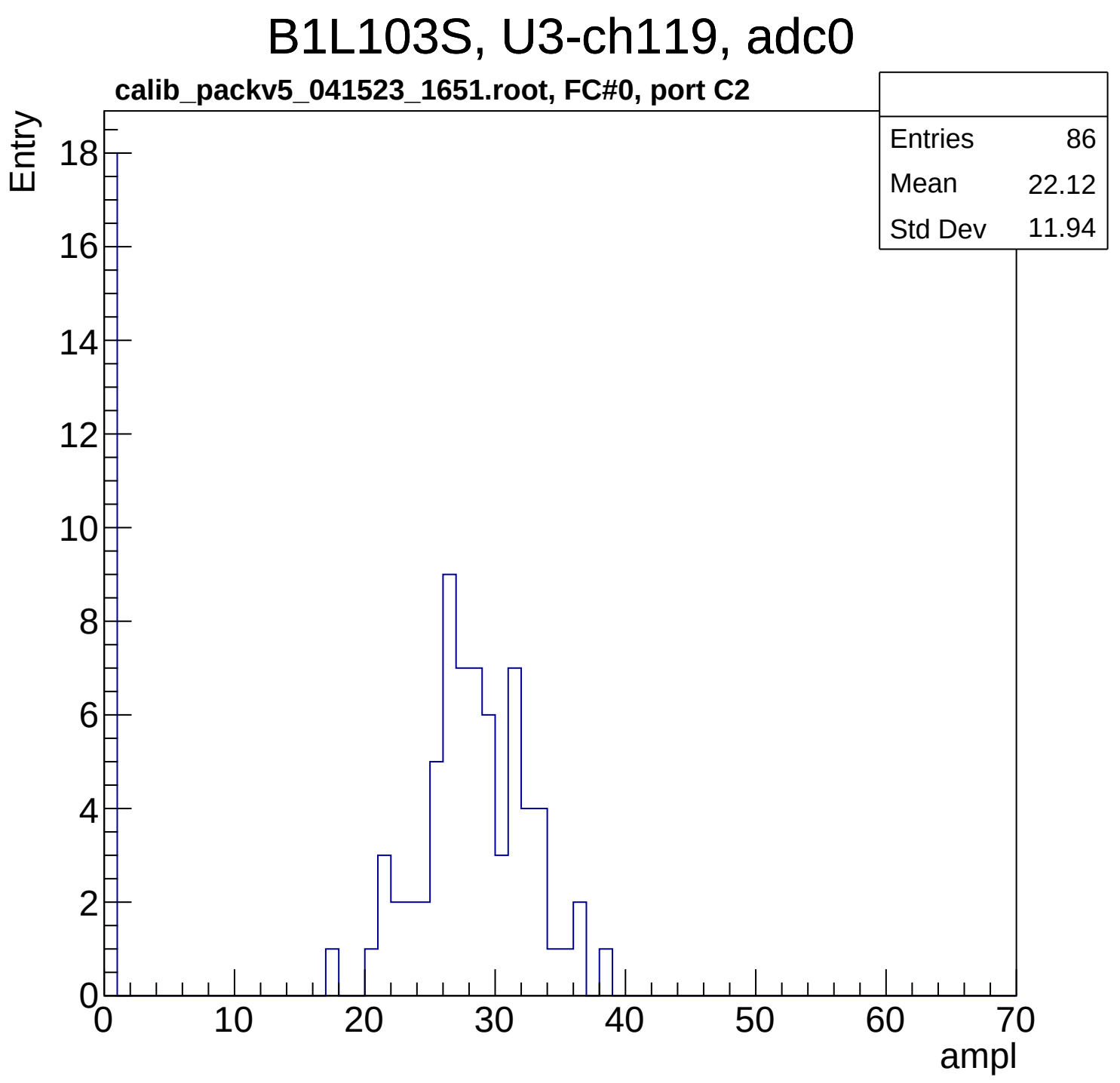
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch119, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 22.12
Std Dev 11.94
Entry
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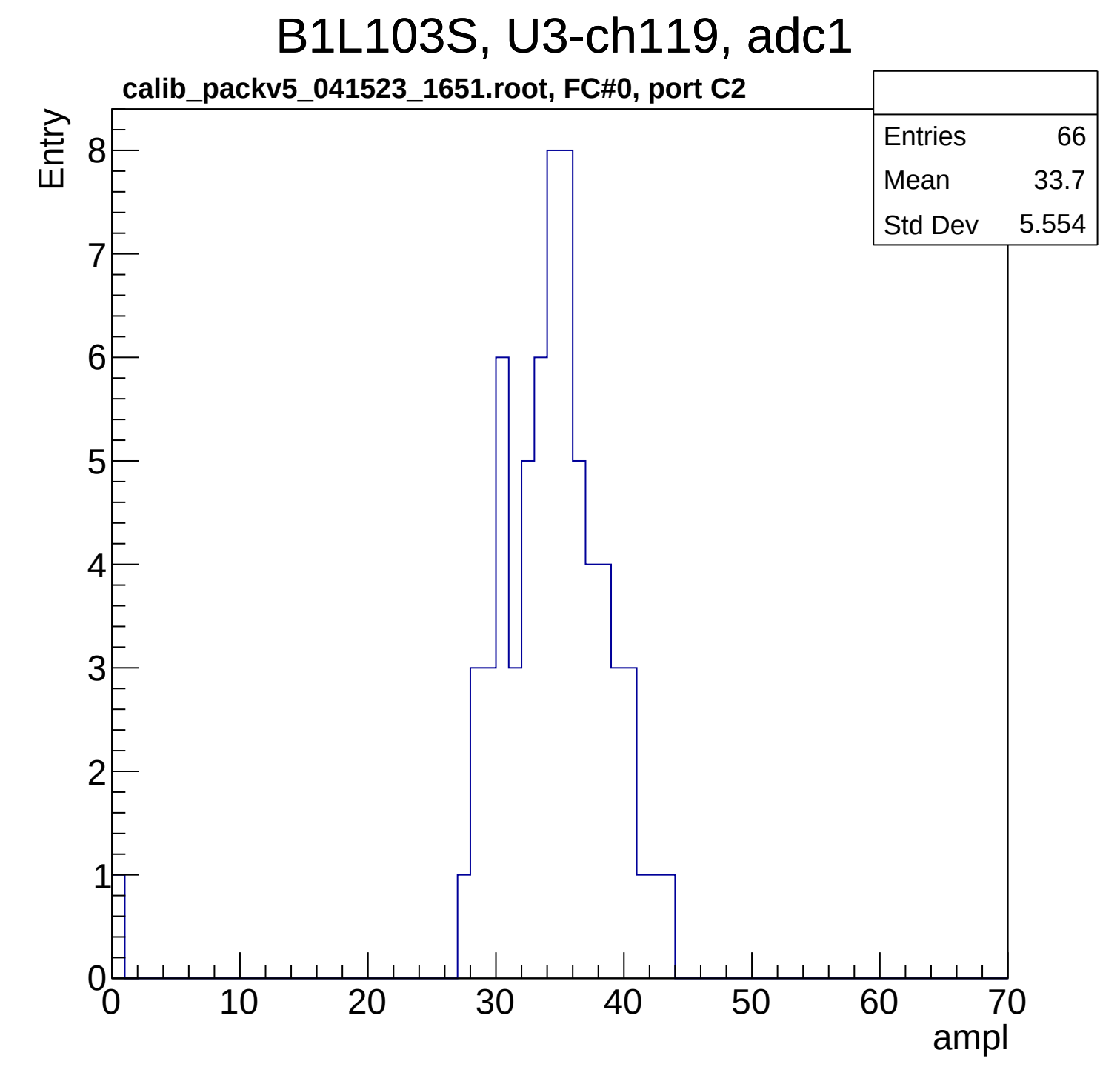
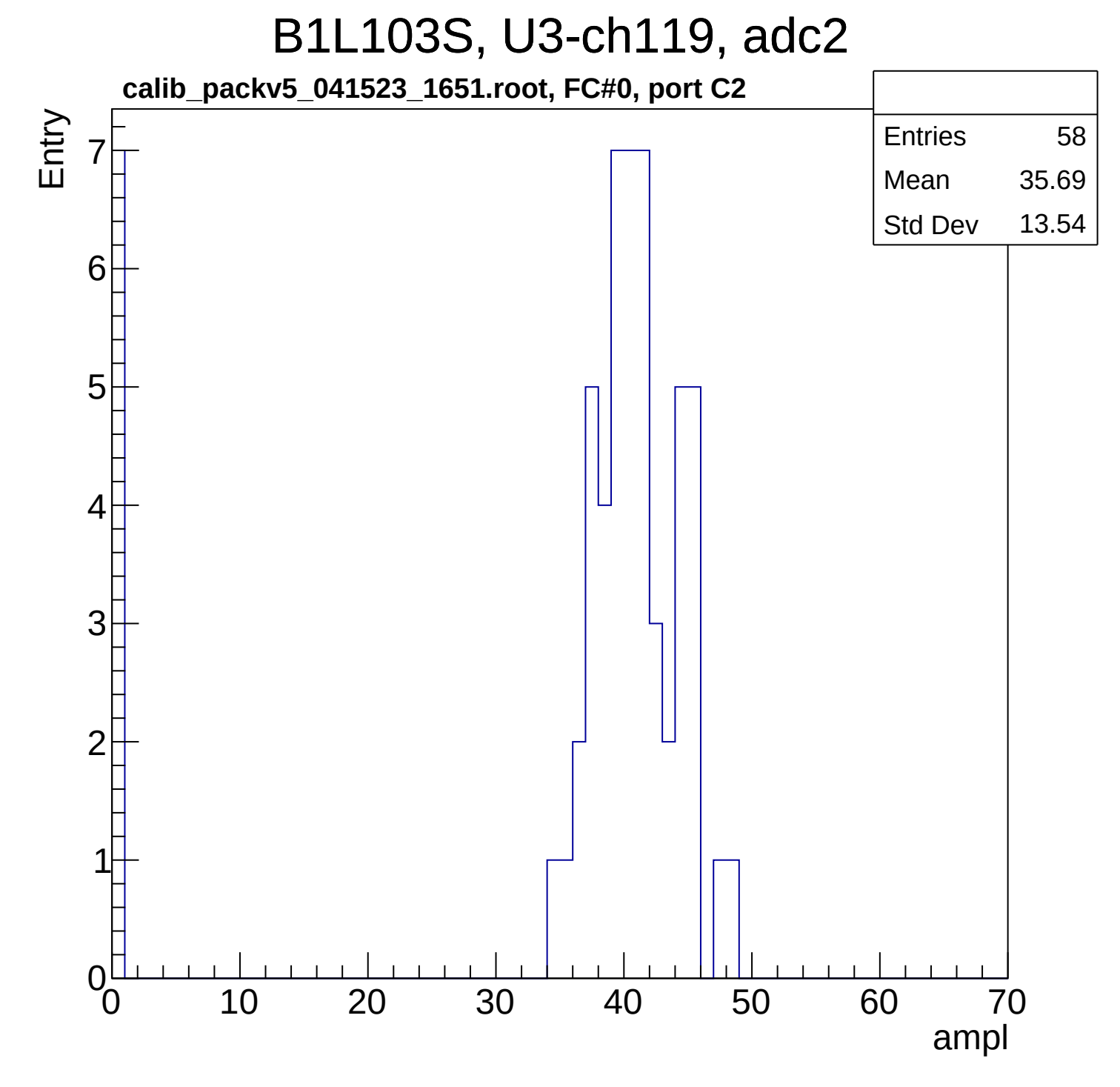
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch119, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 33.7
Std Dev 5.554
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch119, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 35.69
Std Dev 13.54
Entry
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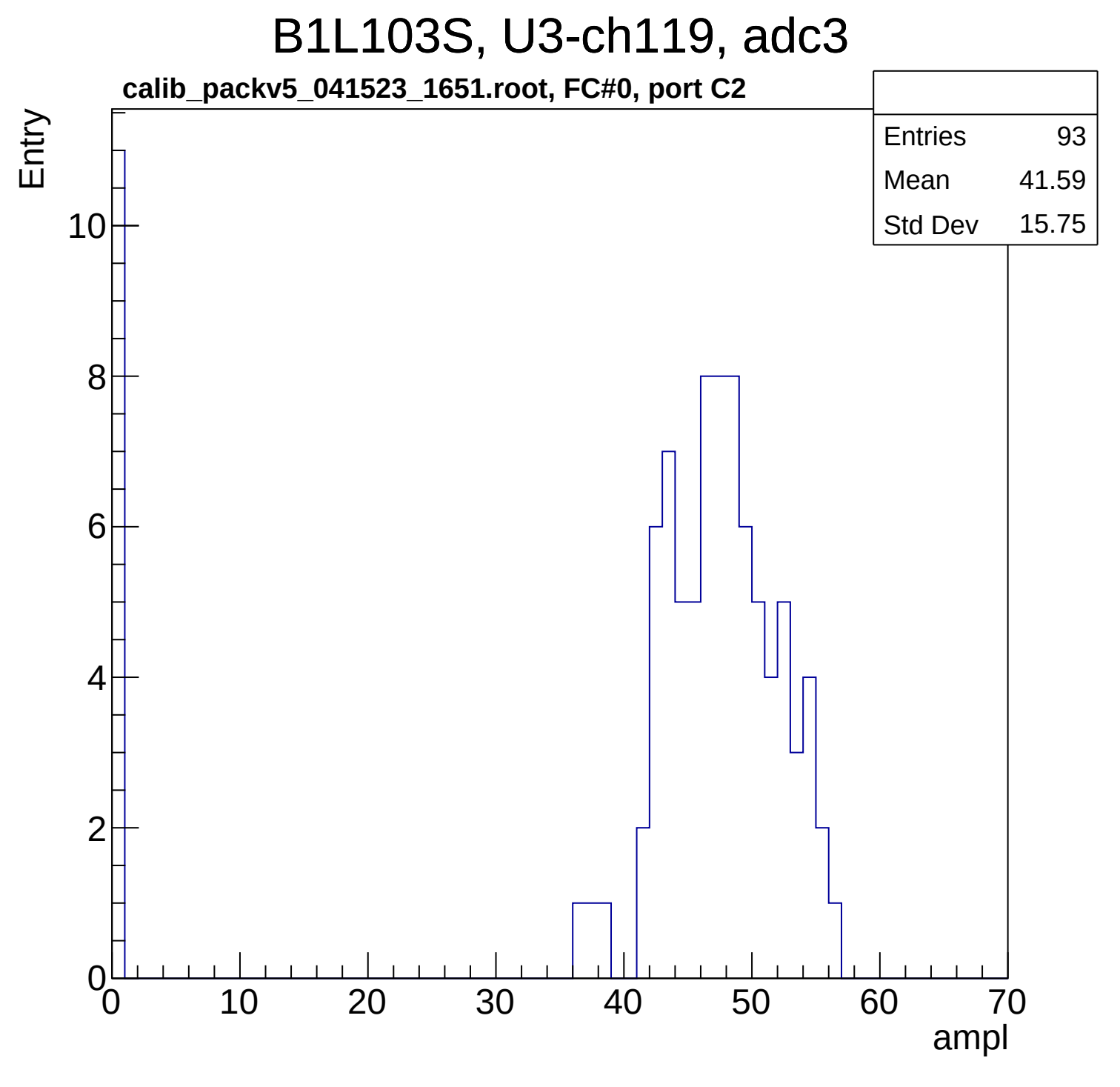
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch119, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 41.59
Std Dev 15.75
Entry
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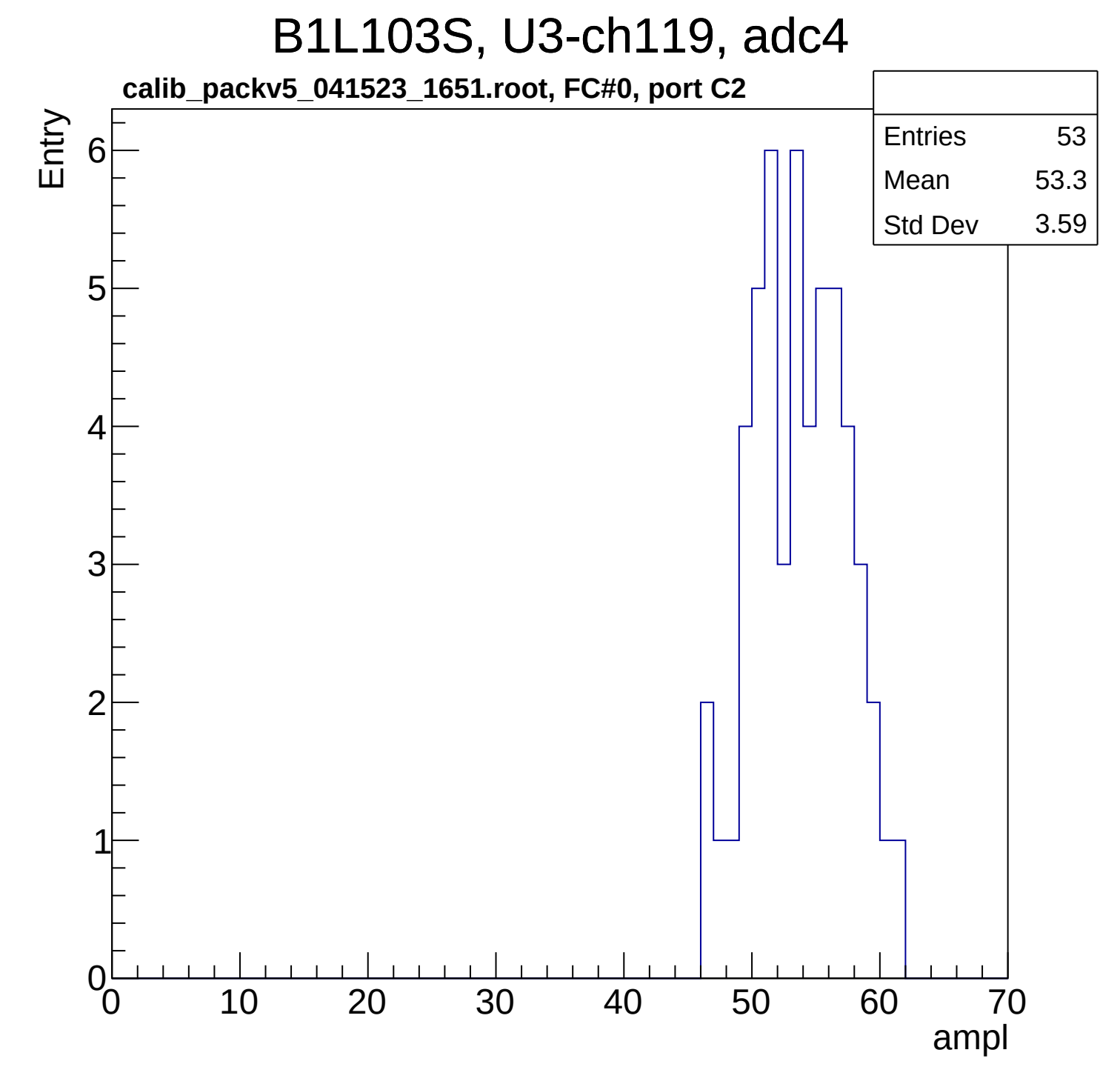
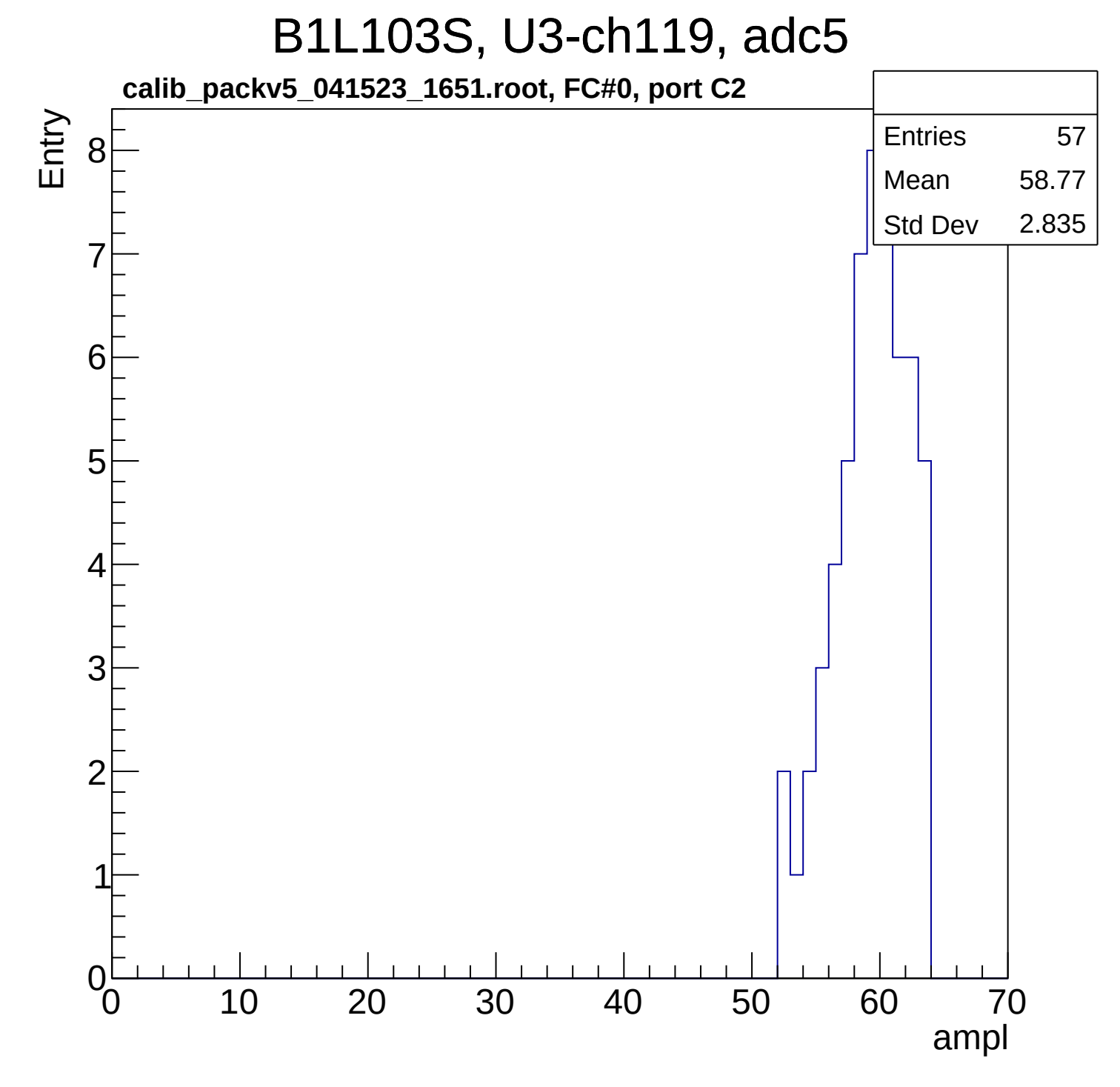
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch119, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 53.3
Std Dev 3.59
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch119, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 58.77
Std Dev 2.835
Entry
ampl
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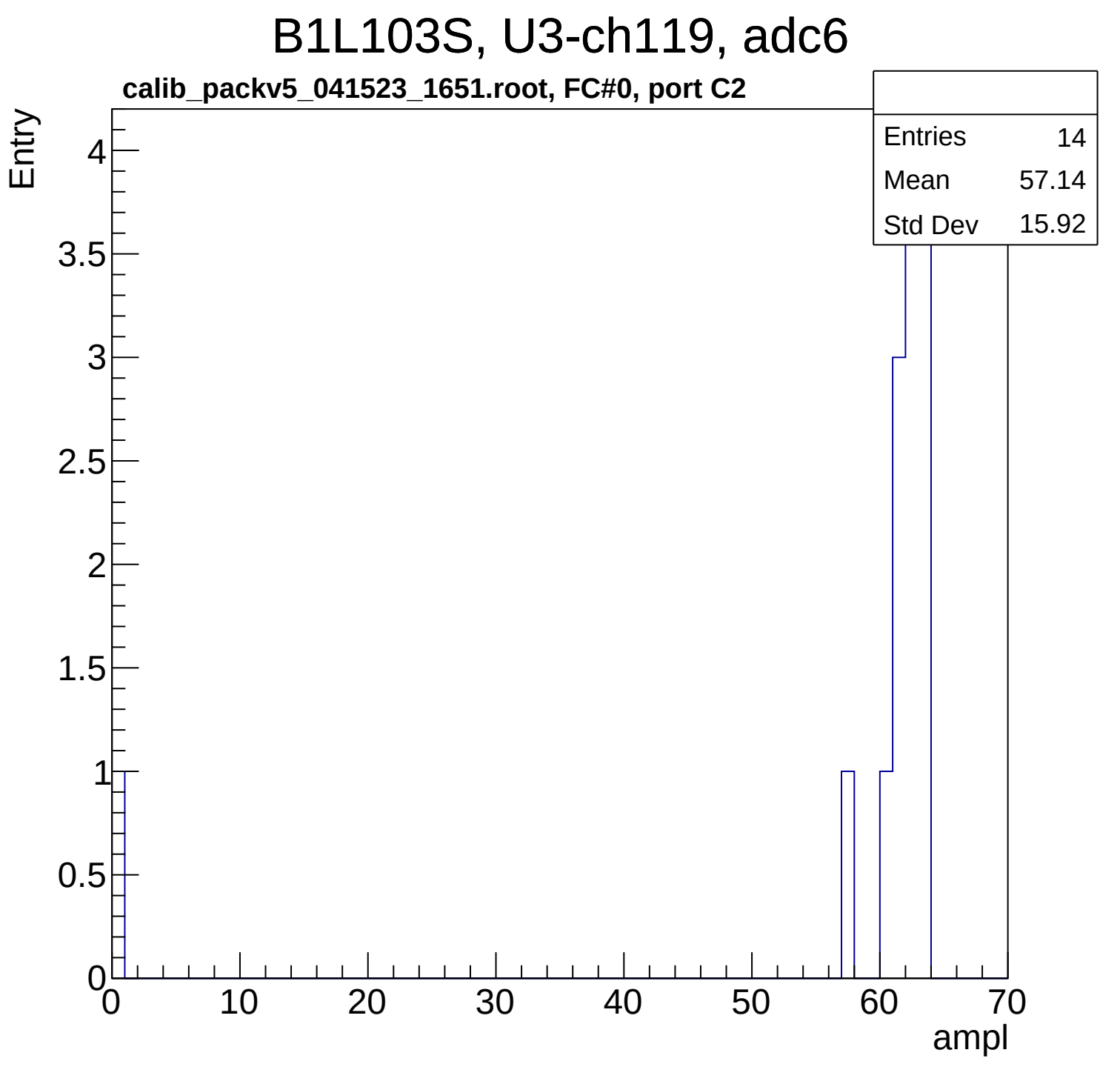
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch119, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 57.14
Std Dev 15.92
Entry
ampl
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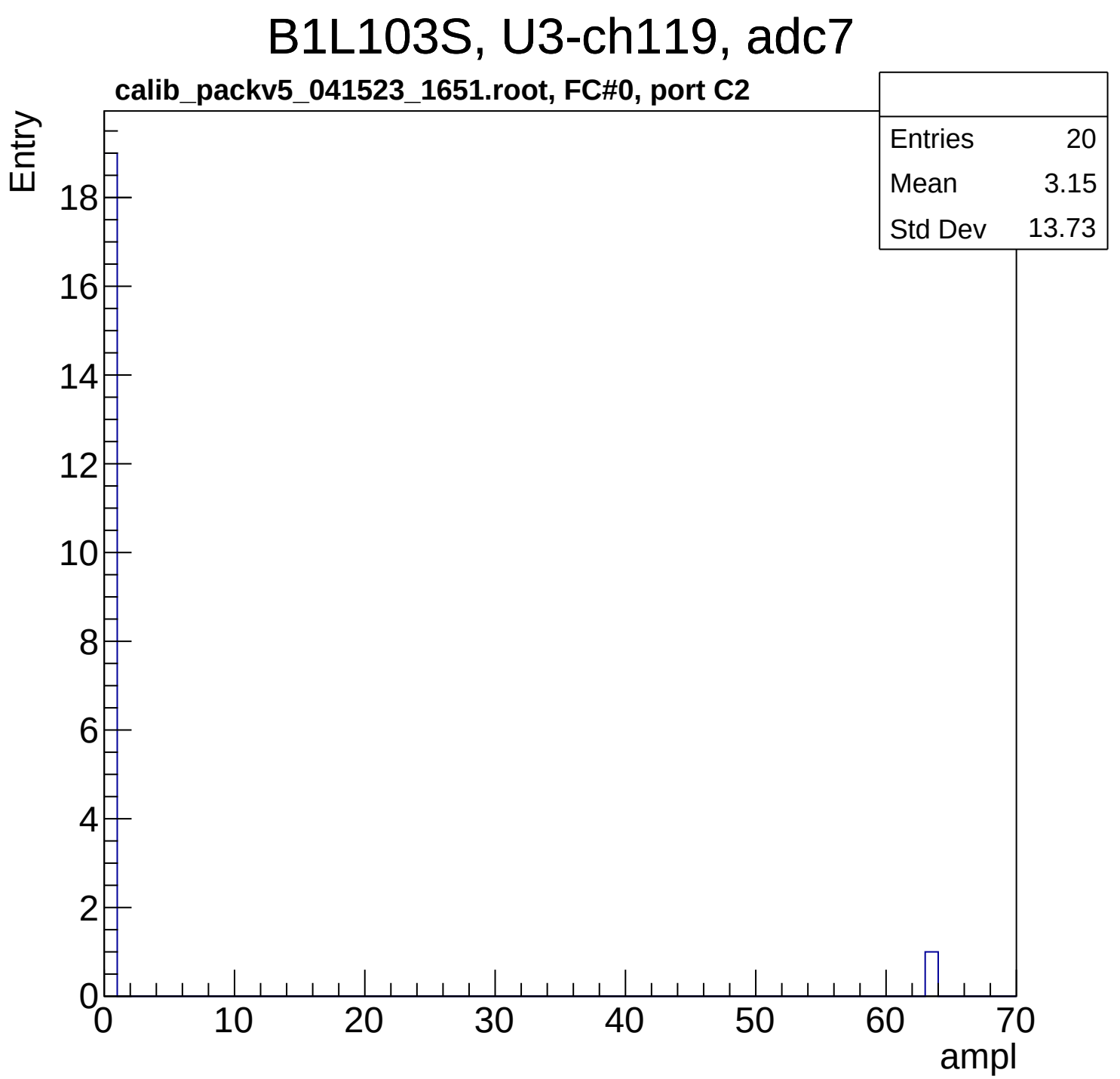
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U3-ch119, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
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6
8
10
12
14
16
18
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10
20
30
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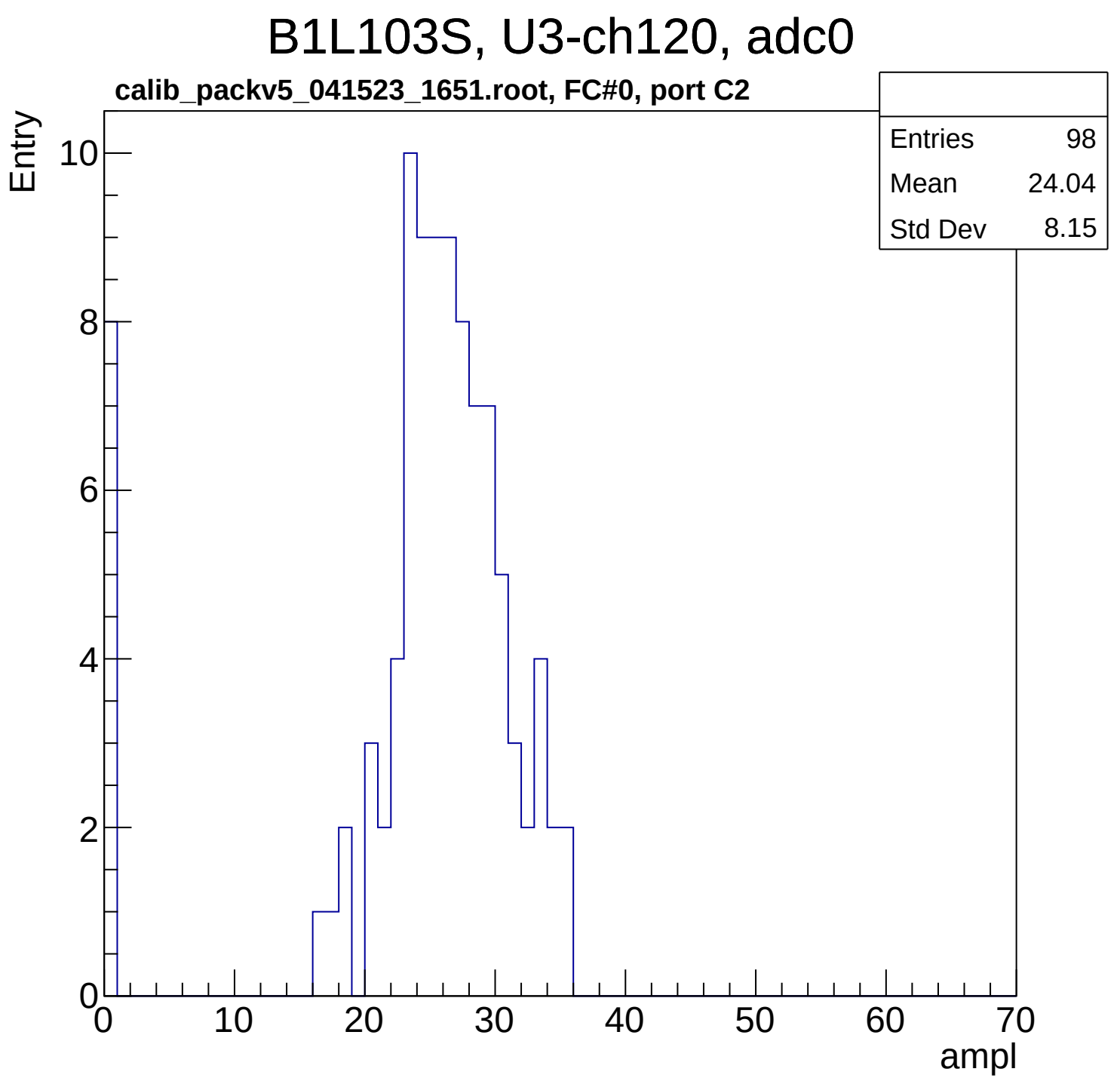
50
60
70
ampl


B1L103S, U3-ch120, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 98
Mean 24.04
Std Dev 8.15
Entry
ampl
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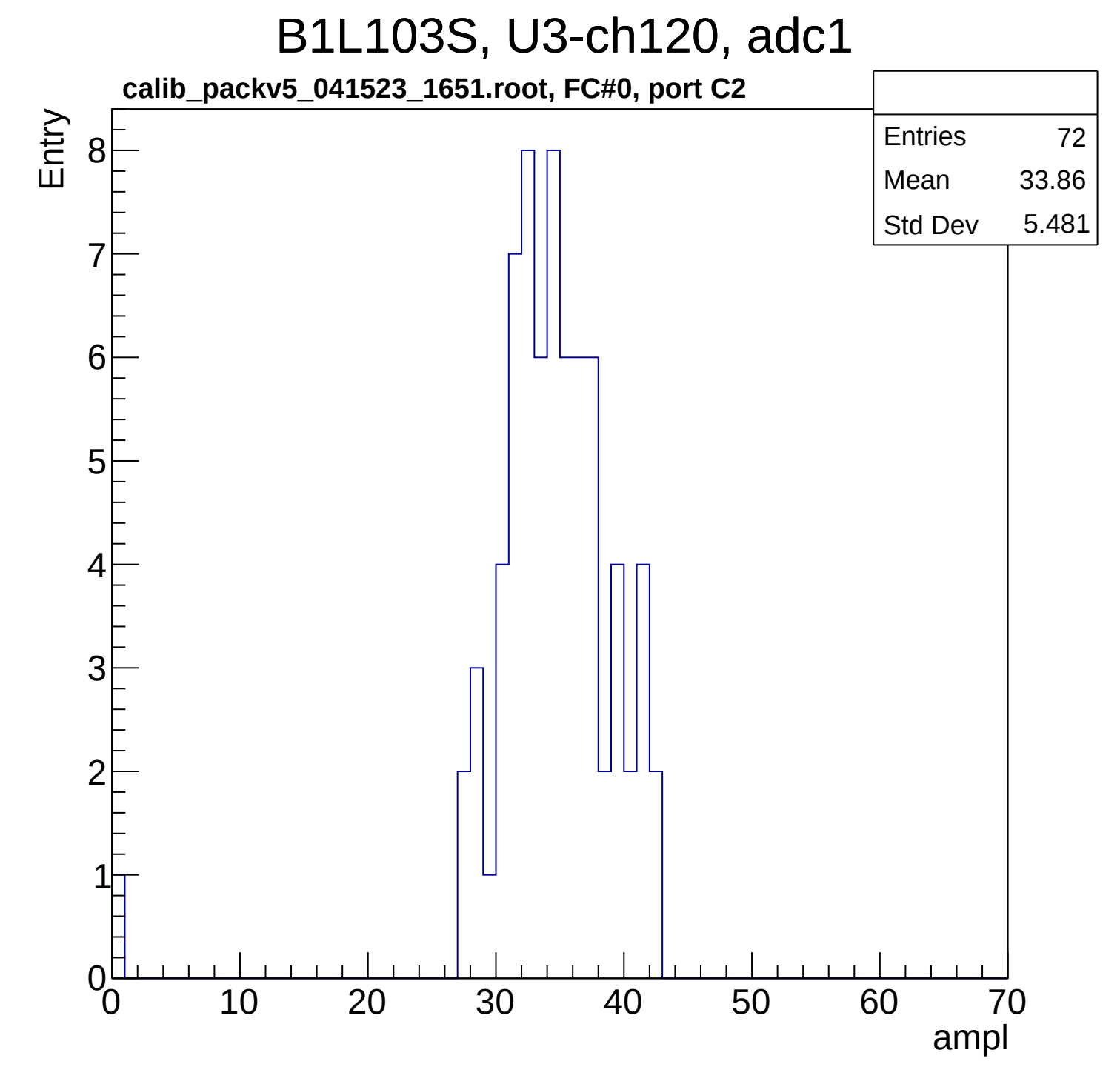
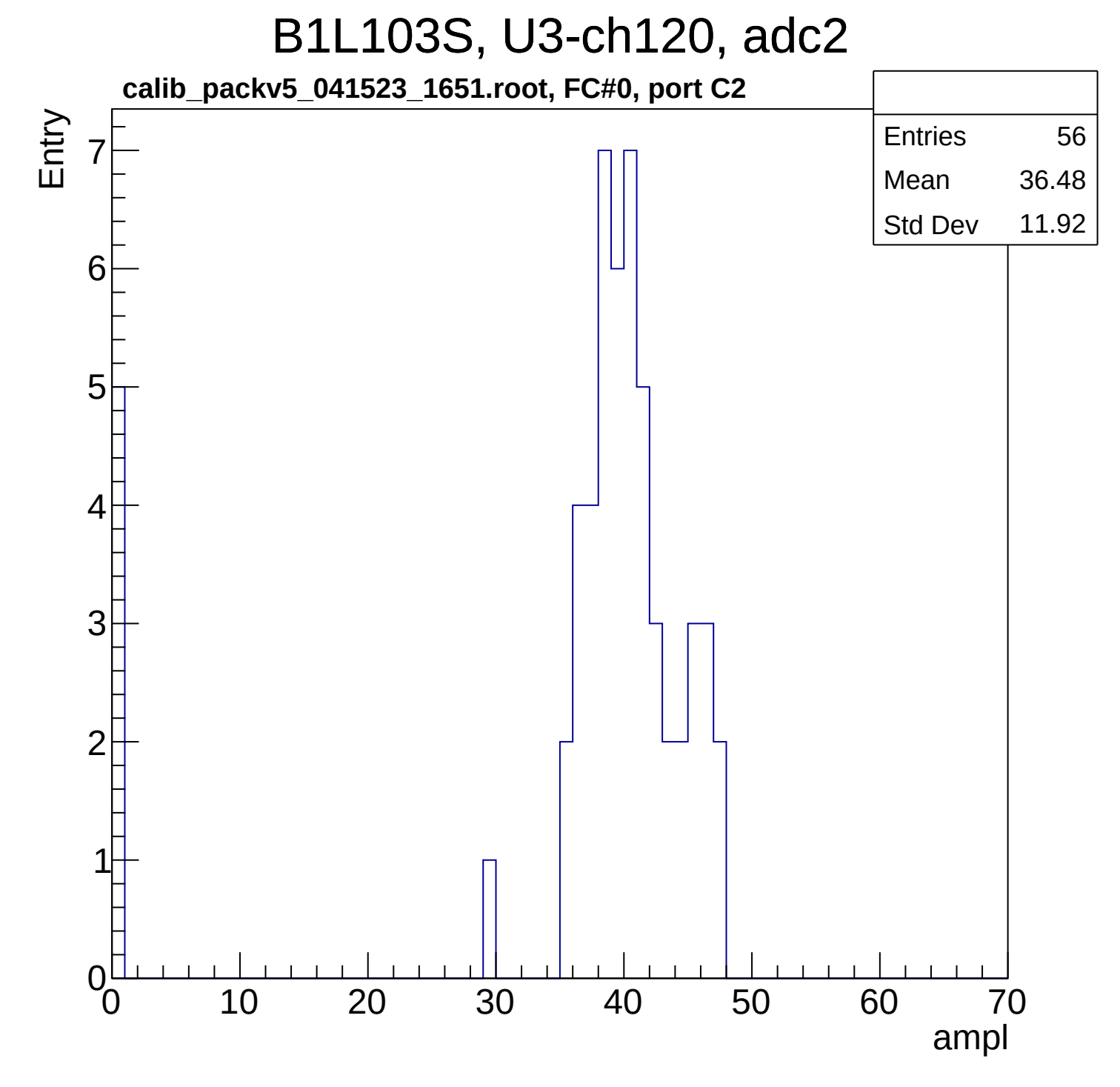
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U3-ch120, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 33.86
Std Dev 5.481
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch120, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 36.48
Std Dev 11.92
Entry
ampl
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3
4
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6
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0
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40
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60
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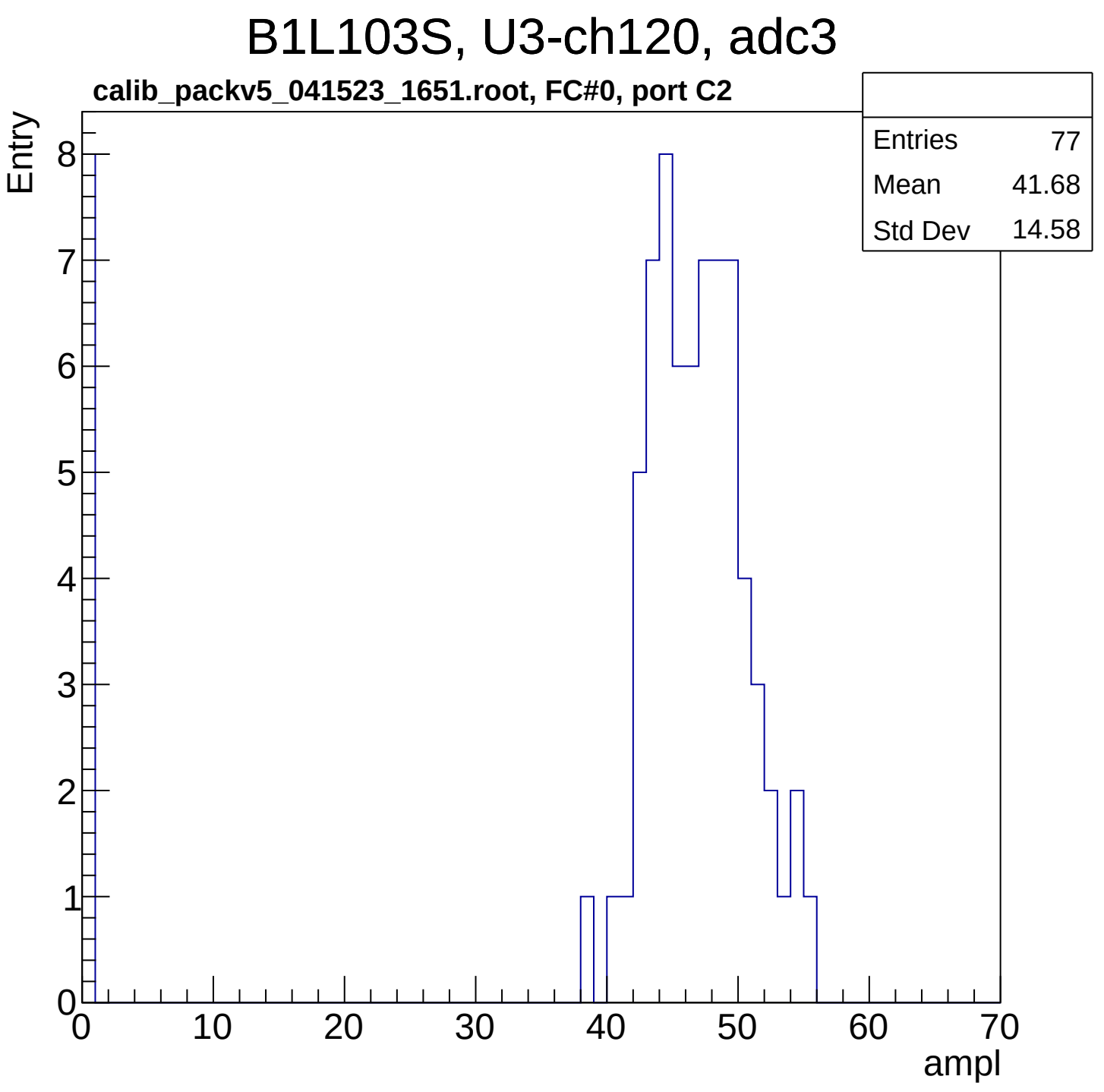
B1L103S, U3-ch120, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 41.68
Std Dev 14.58
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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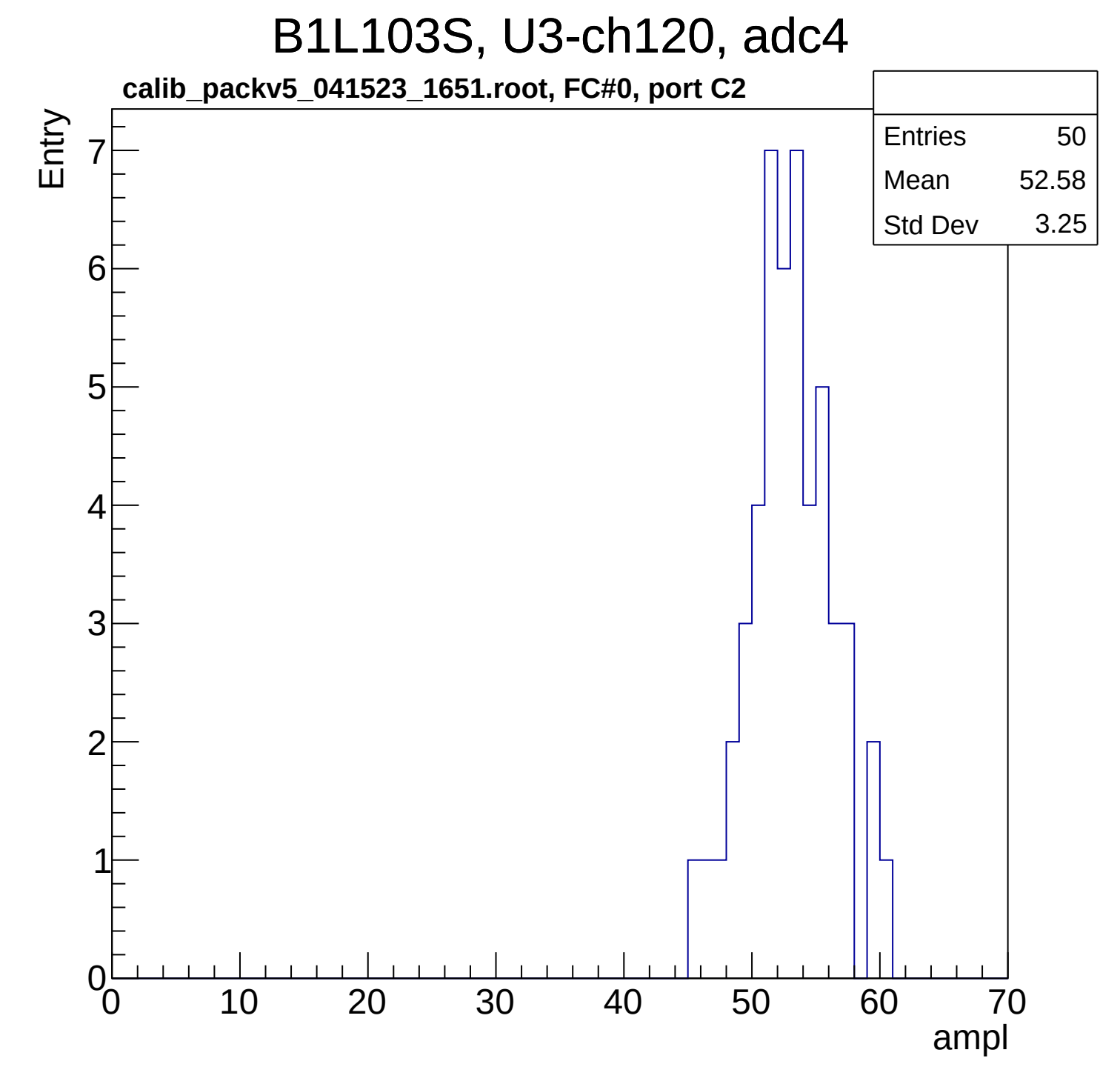
B1L103S, U3-ch120, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 52.58
Std Dev 3.25
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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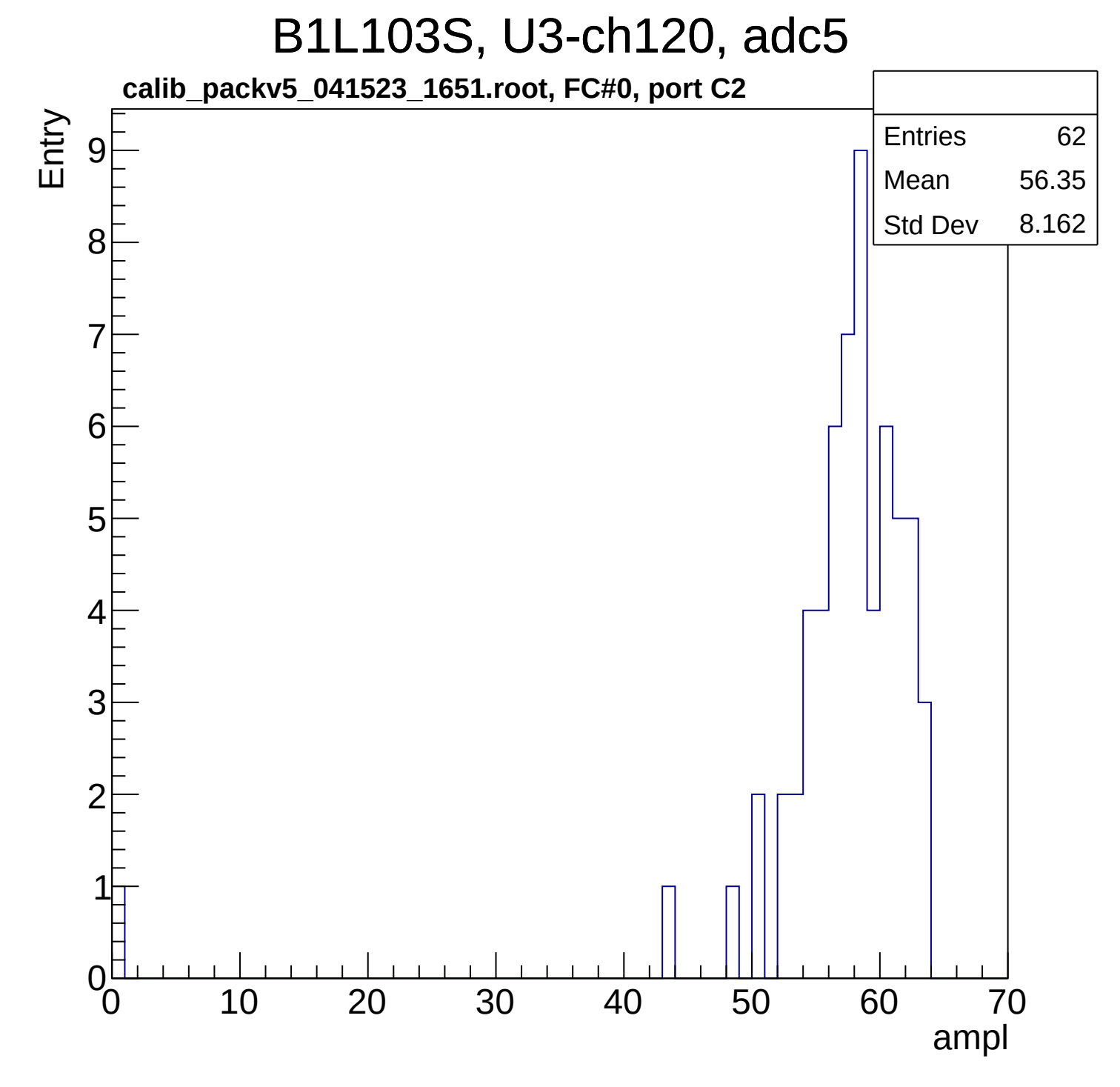
B1L103S, U3-ch120, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 56.35
Std Dev 8.162
Entry
ampl
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2
3
4
5
6
7
8
9
0
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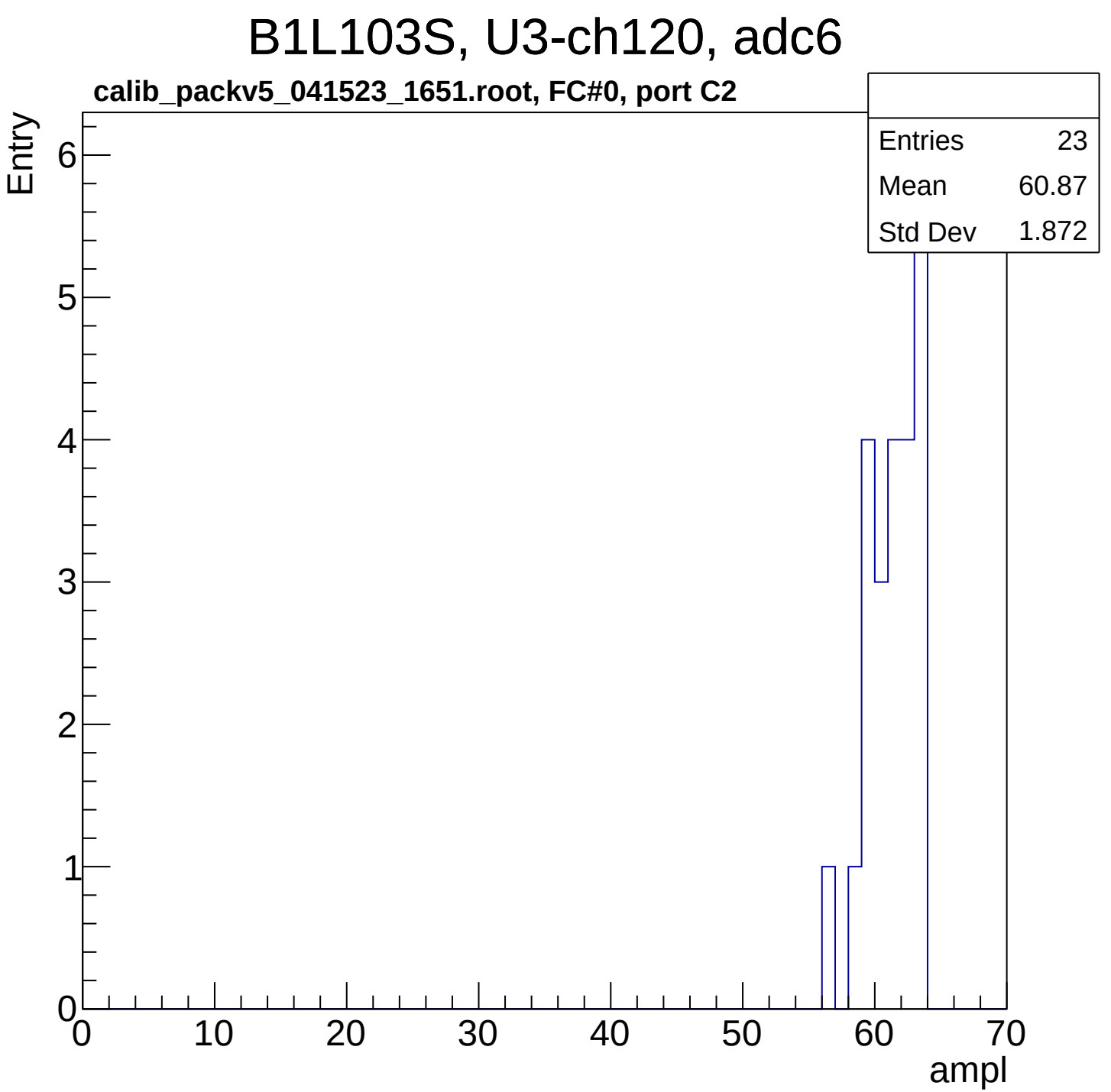
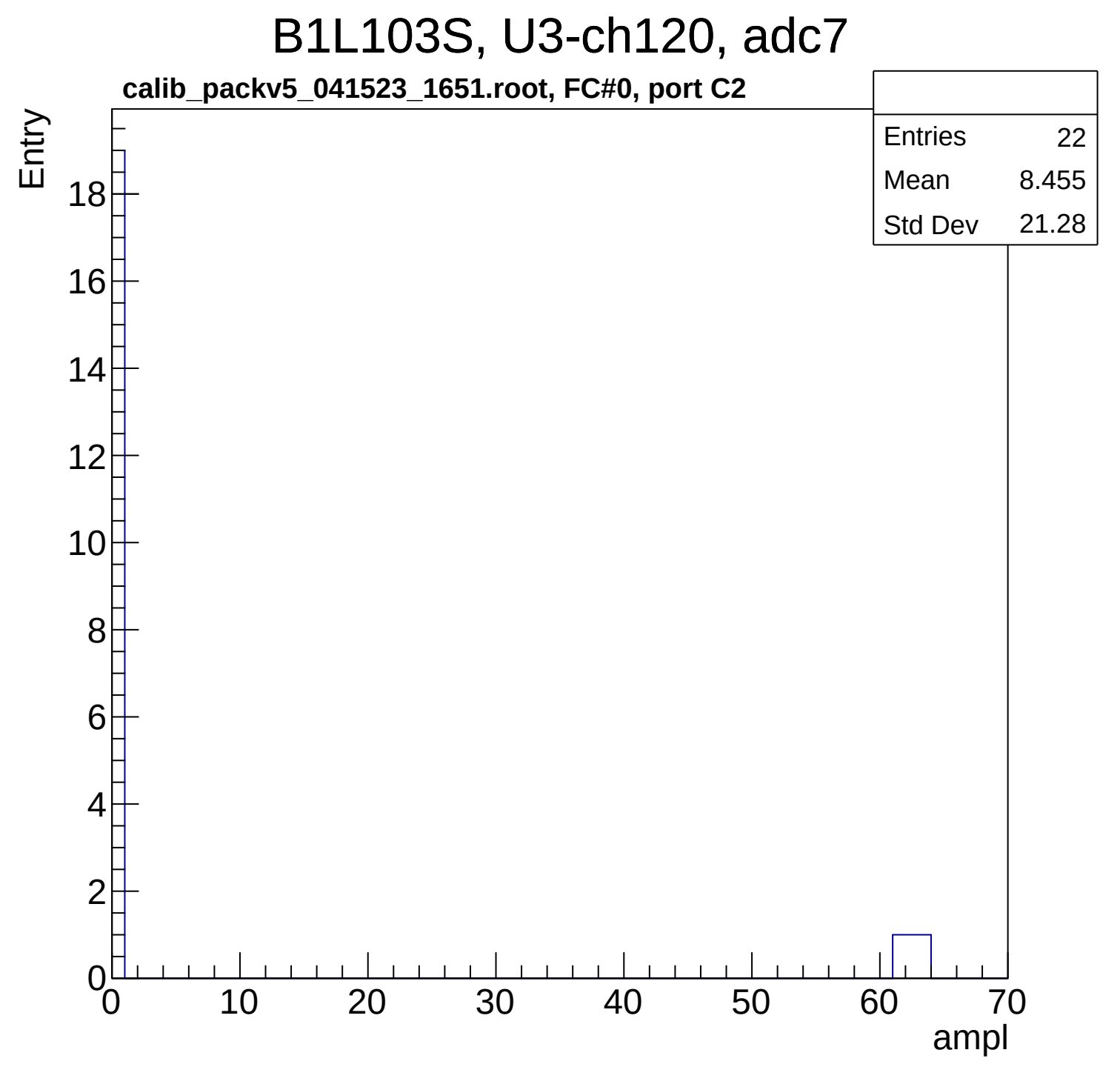
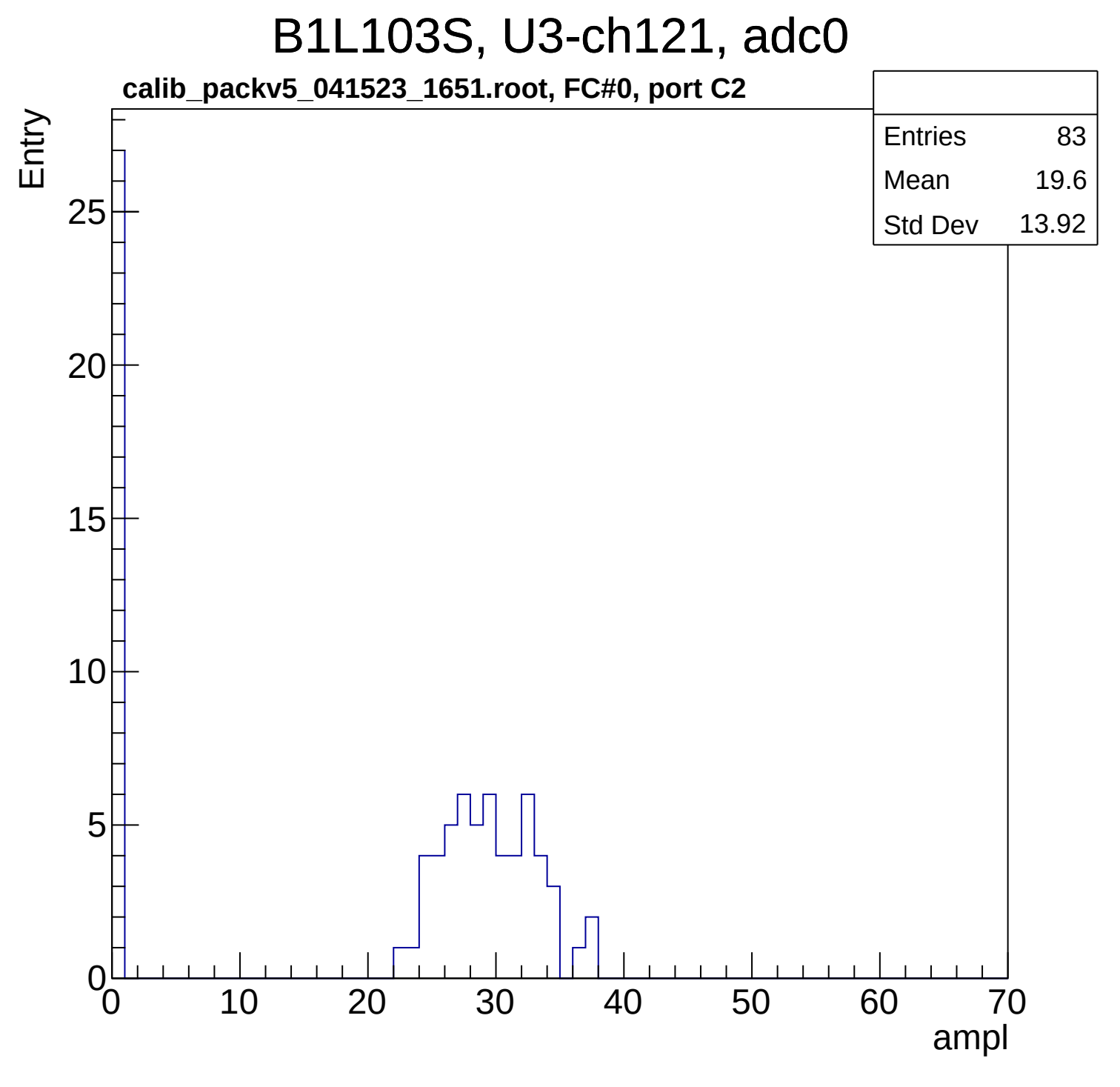
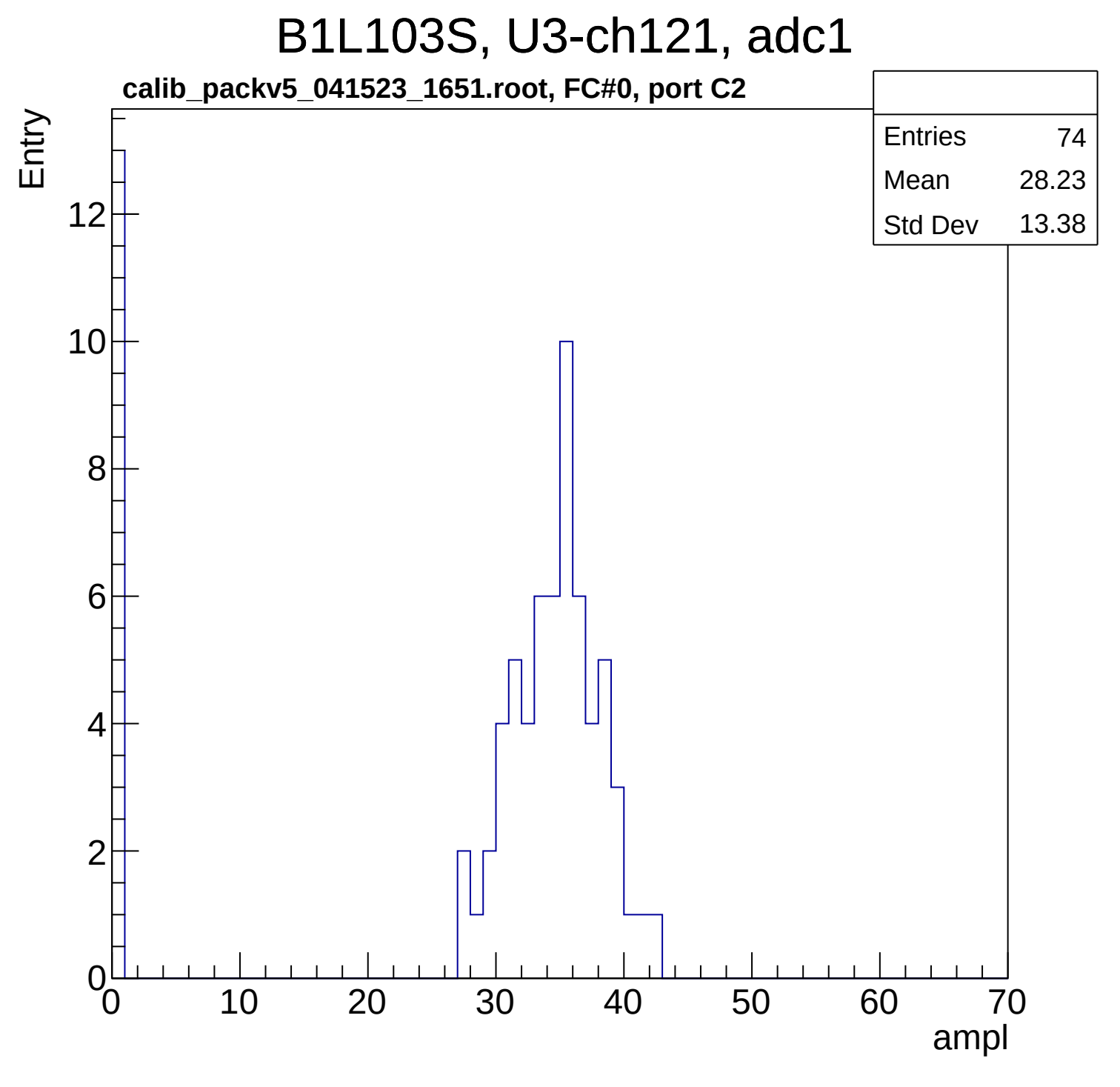
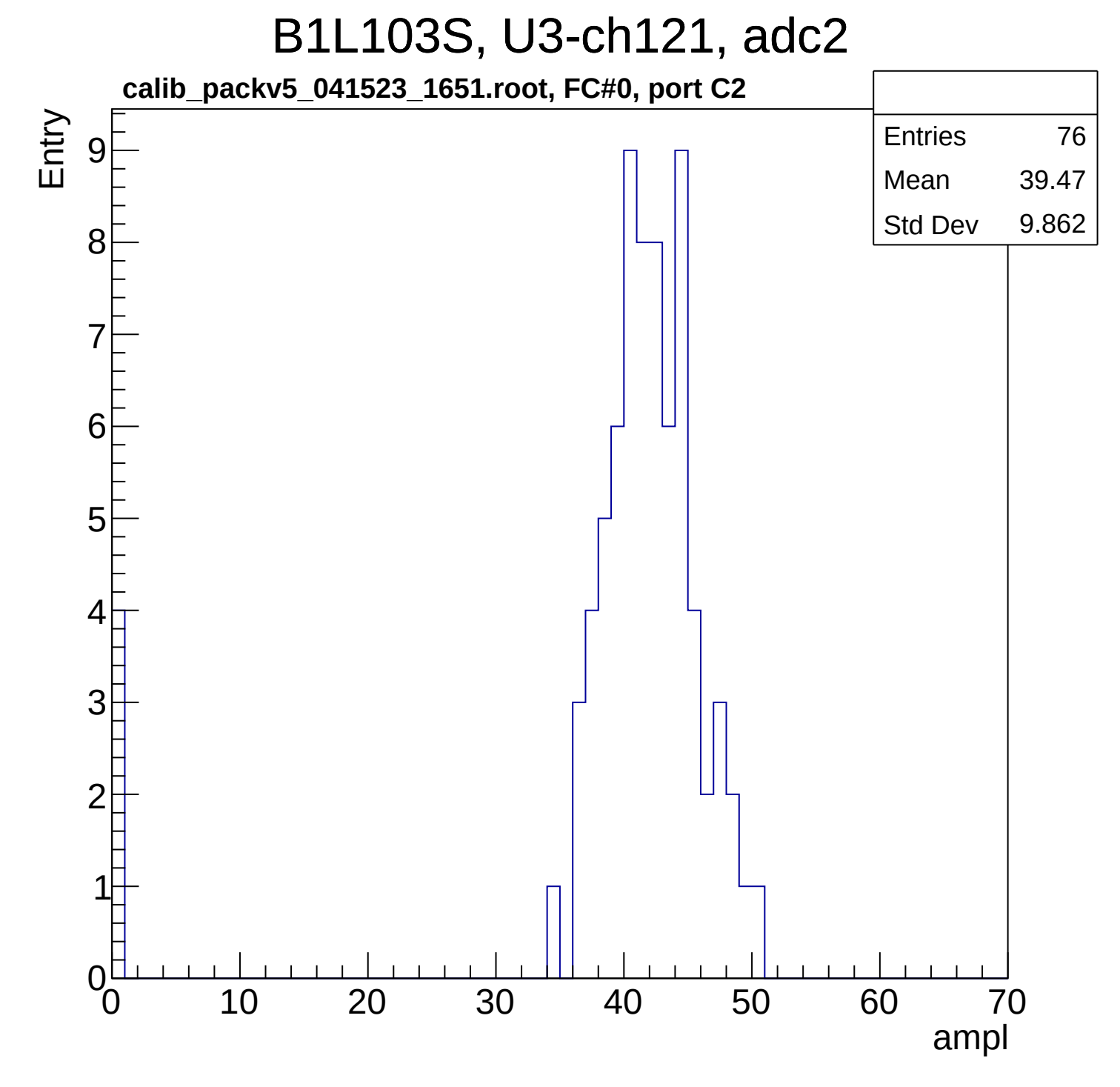
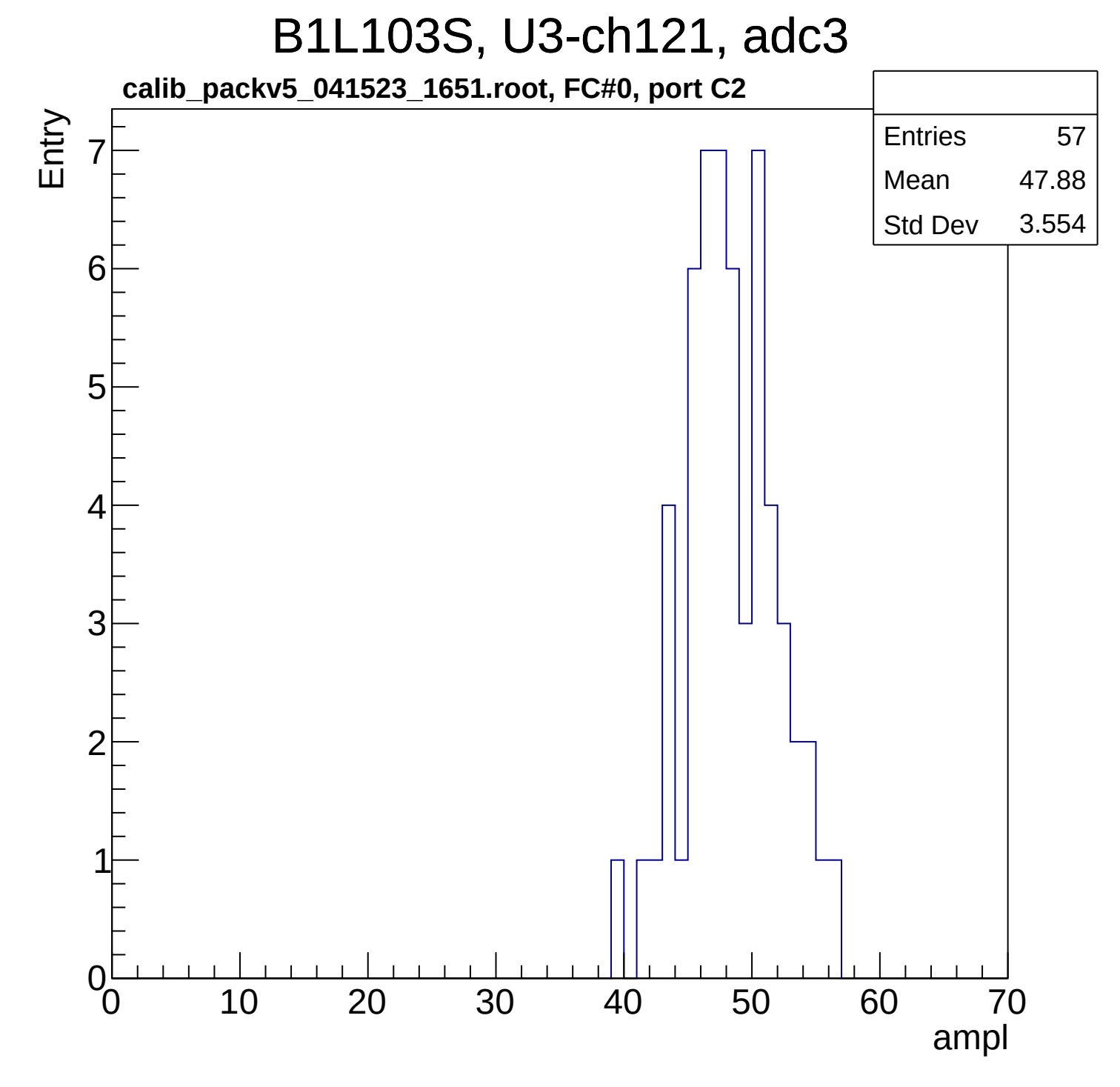

B1L103S, U3-ch120, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 60.87
Std Dev 1.872
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

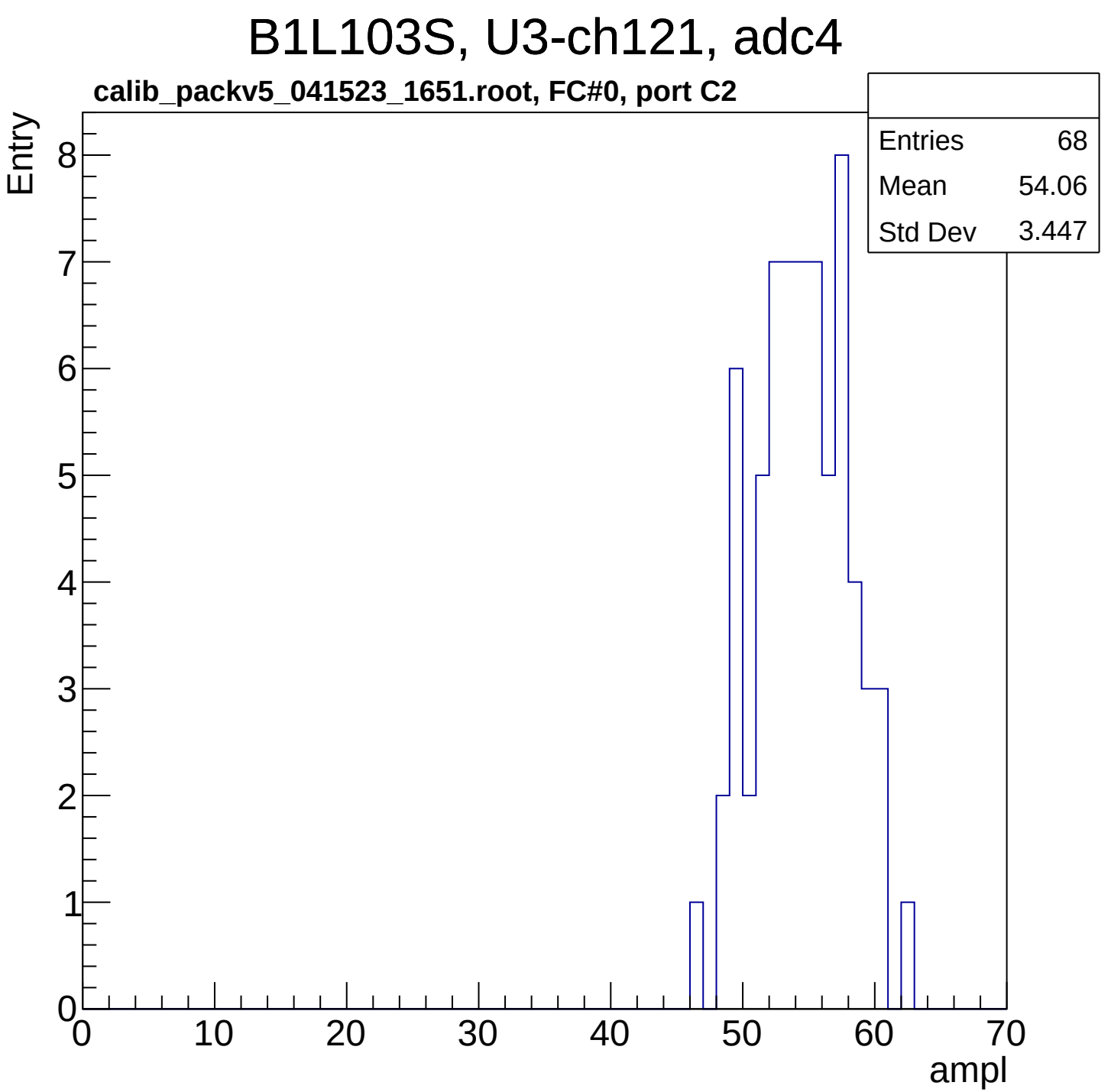

B1L103S, U3-ch120, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.455
Std Dev 21.28
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

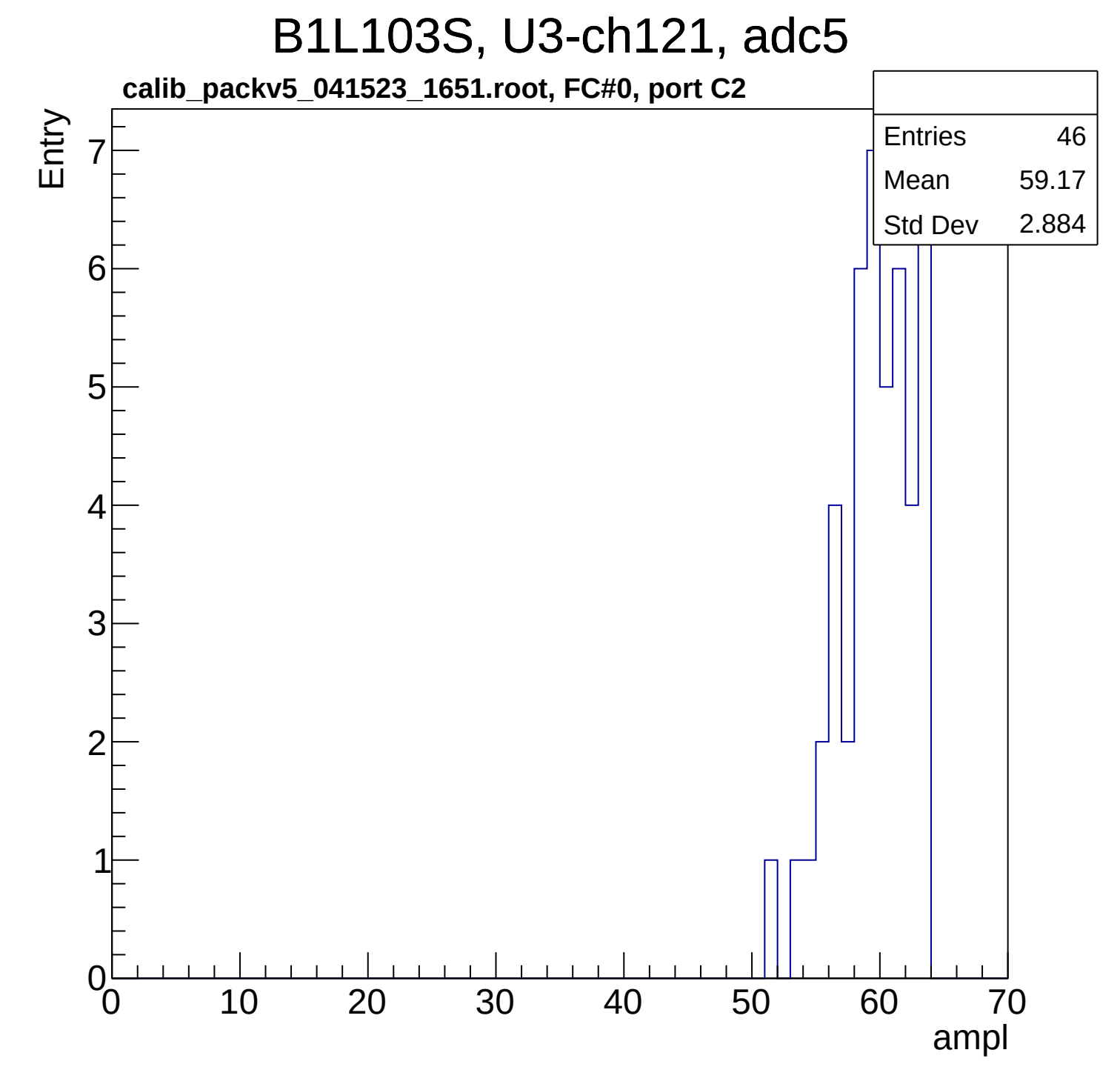

B1L103S, U3-ch121, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 19.6
Std Dev 13.92
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl

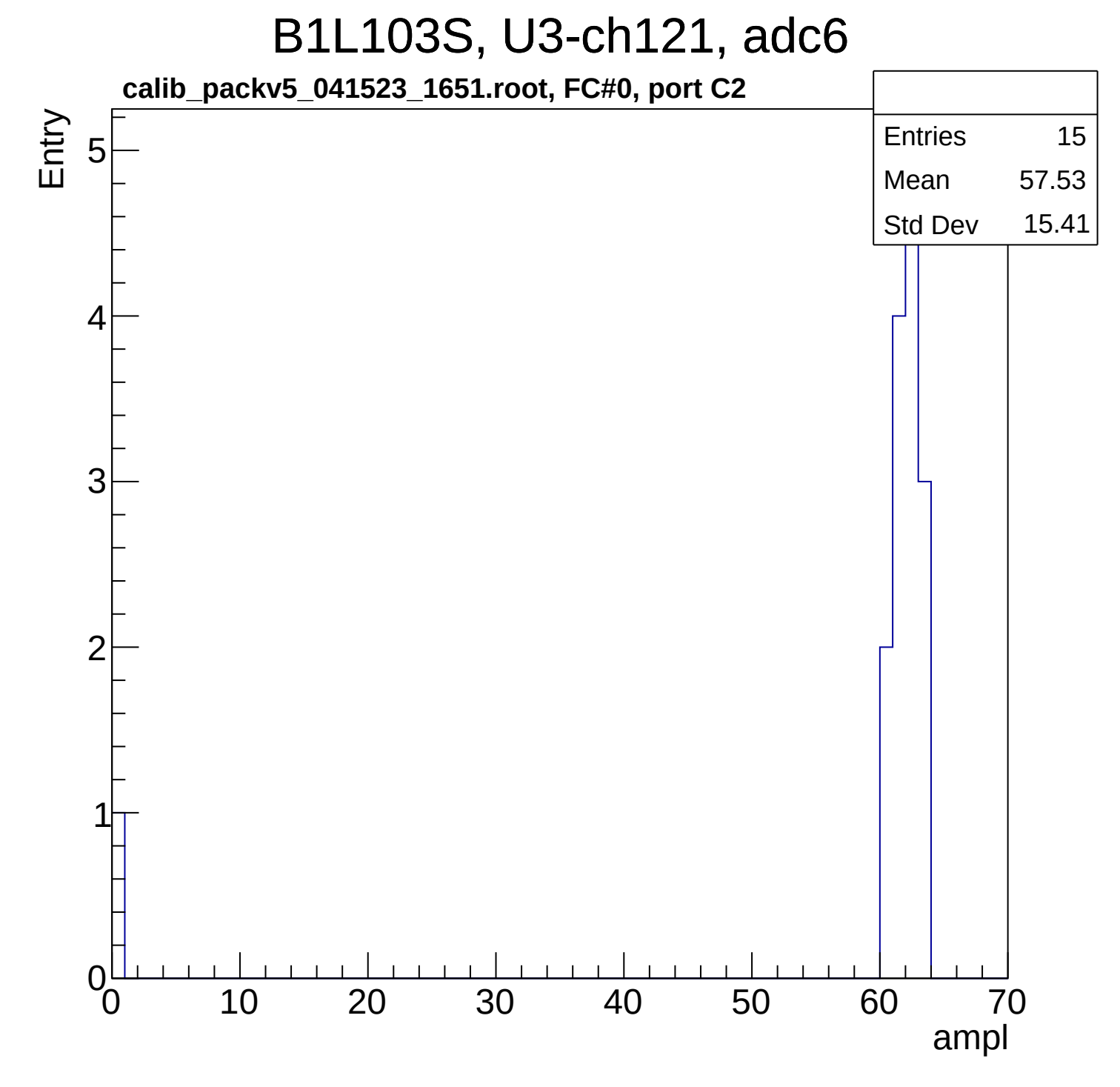

B1L103S, U3-ch121, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 28.23
Std Dev 13.38
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

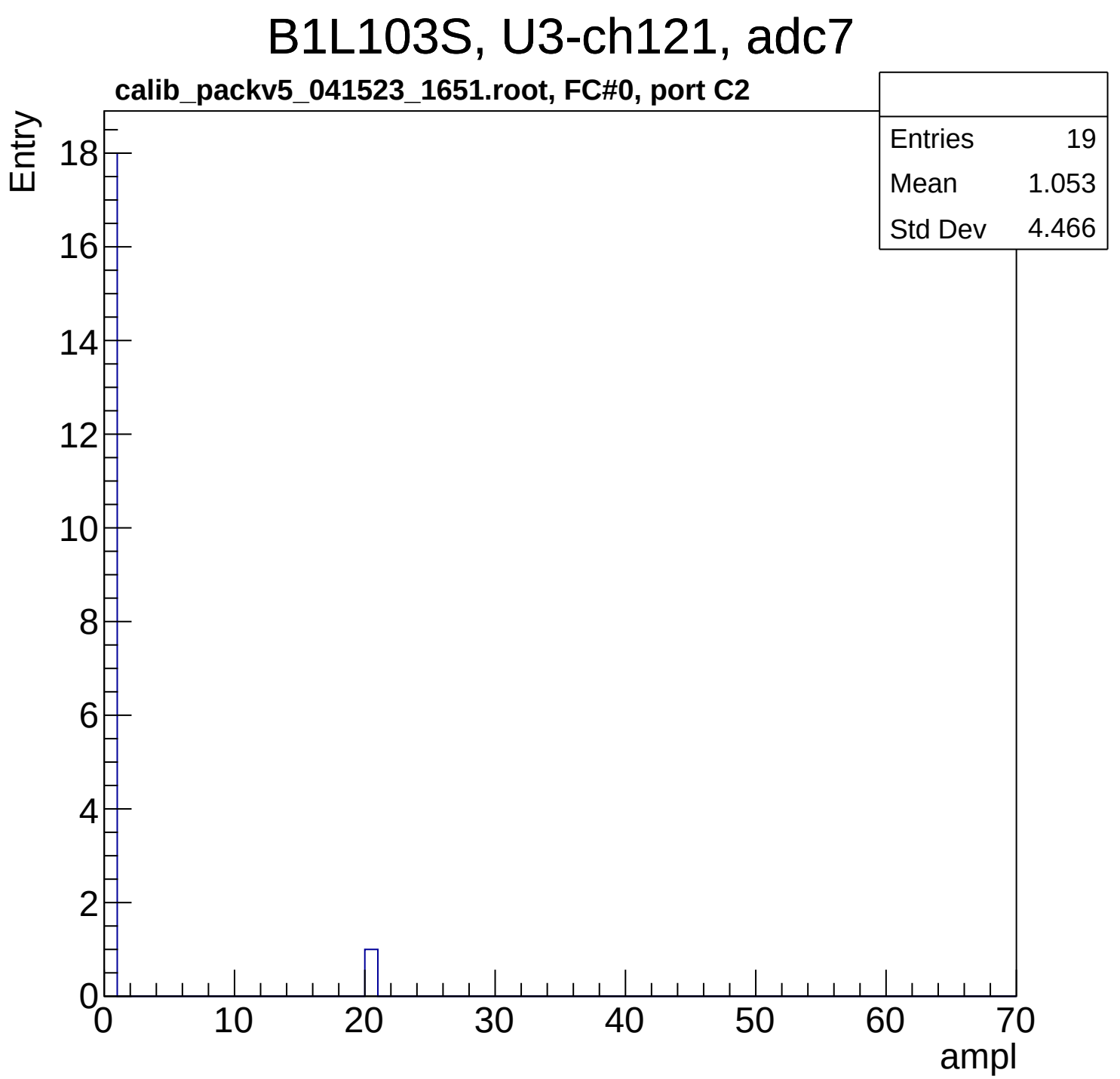

B1L103S, U3-ch121, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 39.47
Std Dev 9.862
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

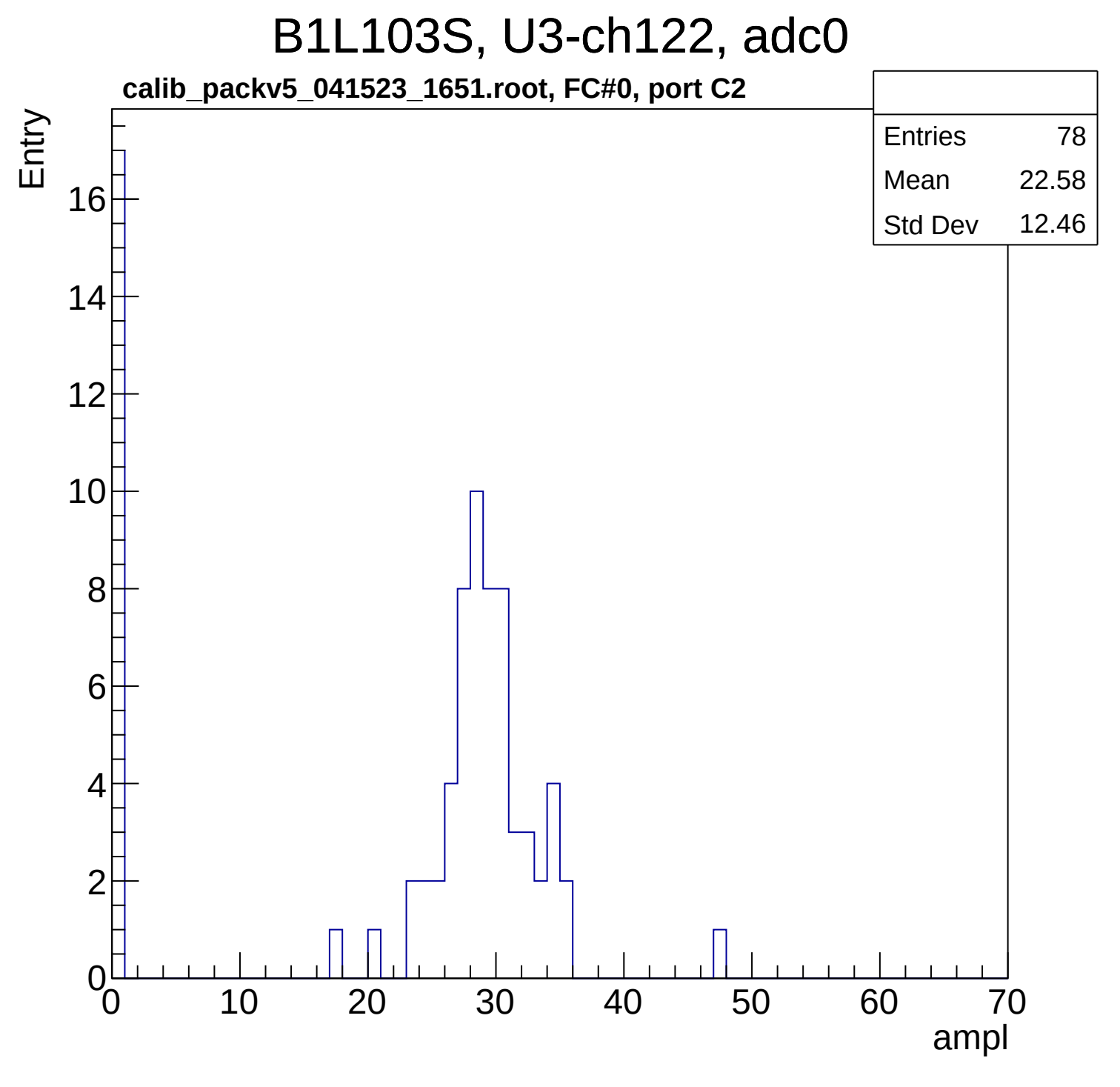

B1L103S, U3-ch121, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 47.88
Std Dev 3.554
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch121, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 54.06
Std Dev 3.447
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch121, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 59.17
Std Dev 2.884
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch121, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 57.53
Std Dev 15.41
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch121, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.053
Std Dev 4.466
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch122, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 22.58
Std Dev 12.46
Entry
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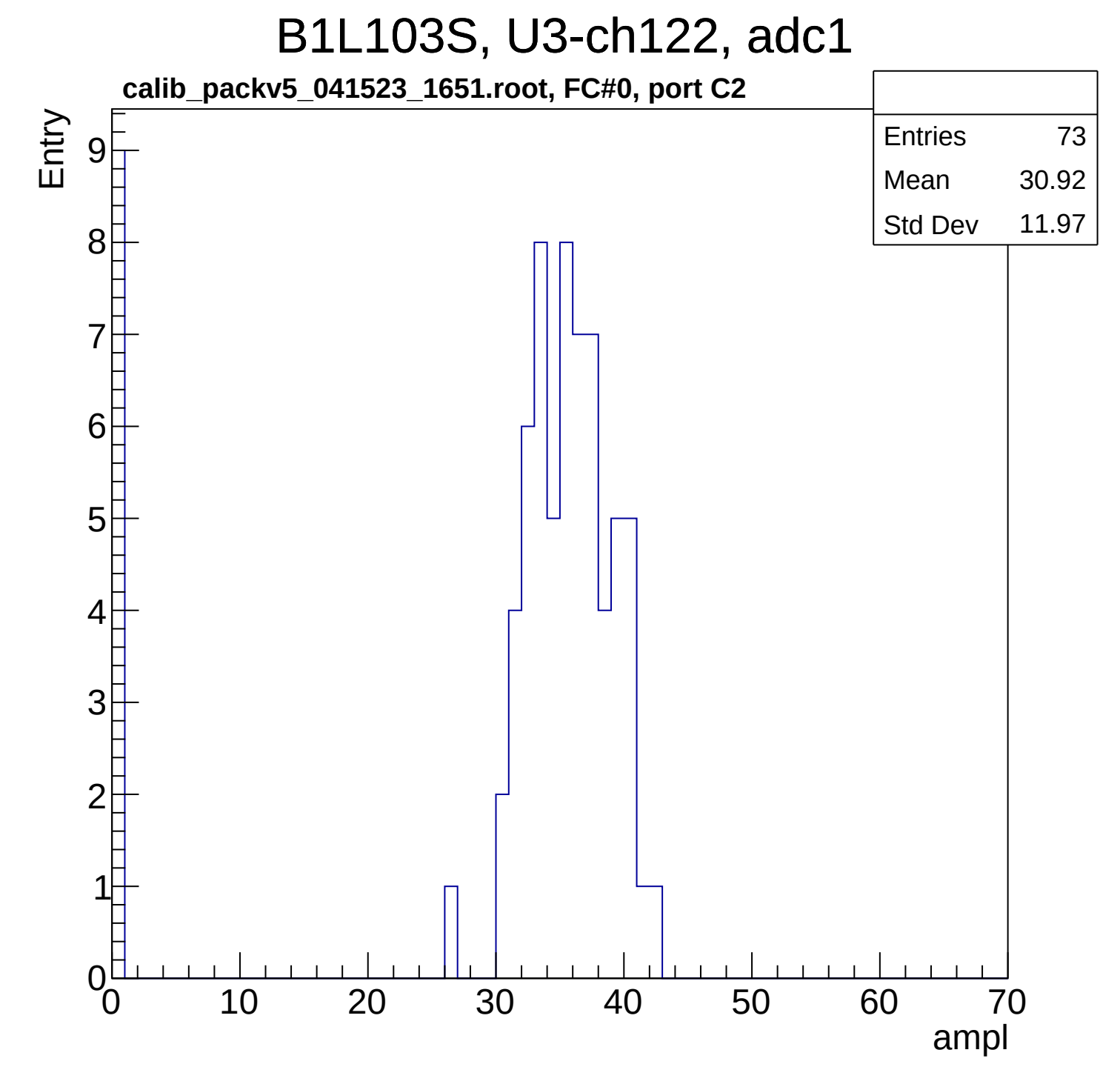
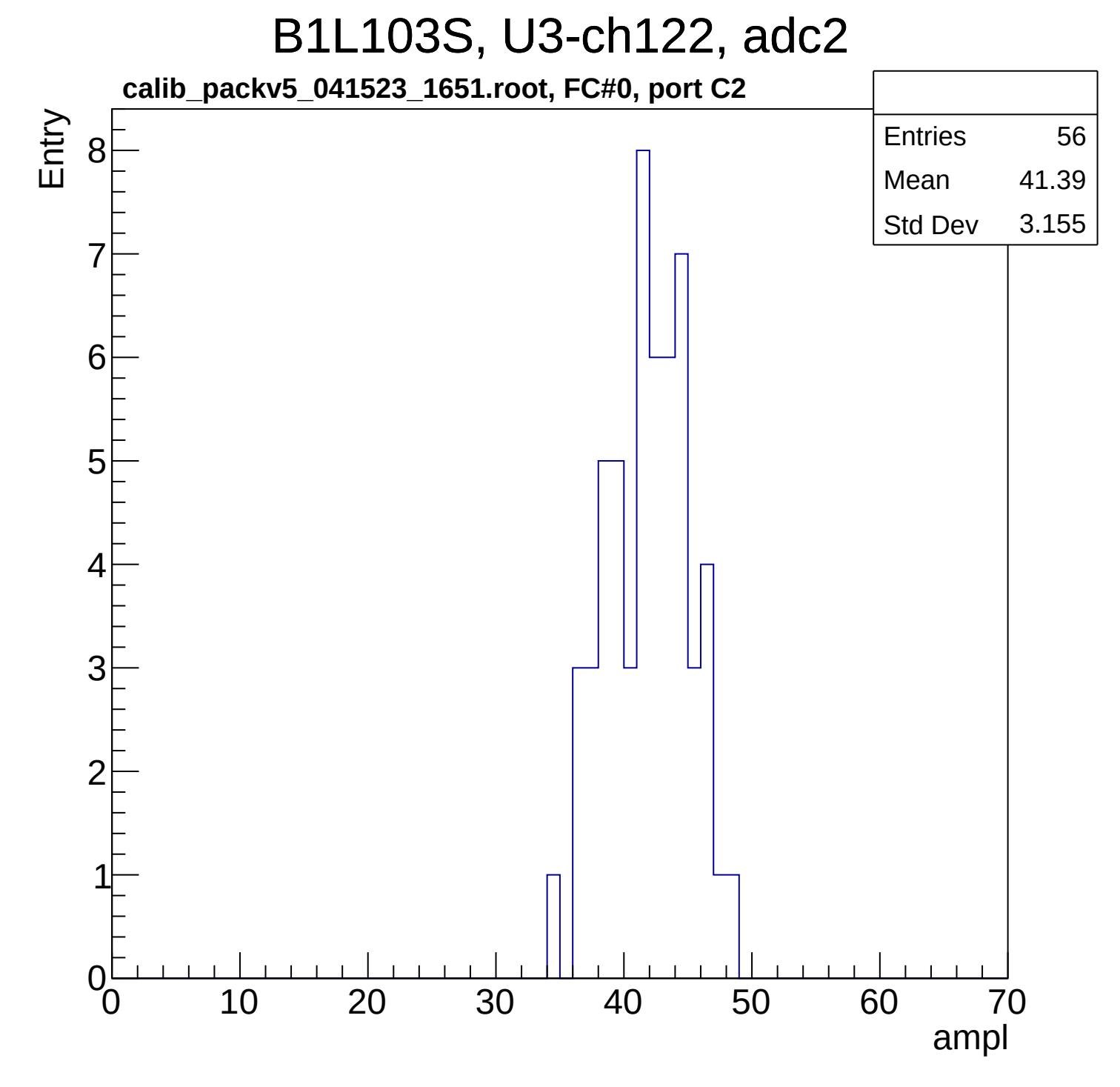
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch122, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 30.92
Std Dev 11.97
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch122, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 41.39
Std Dev 3.155
Entry
ampl
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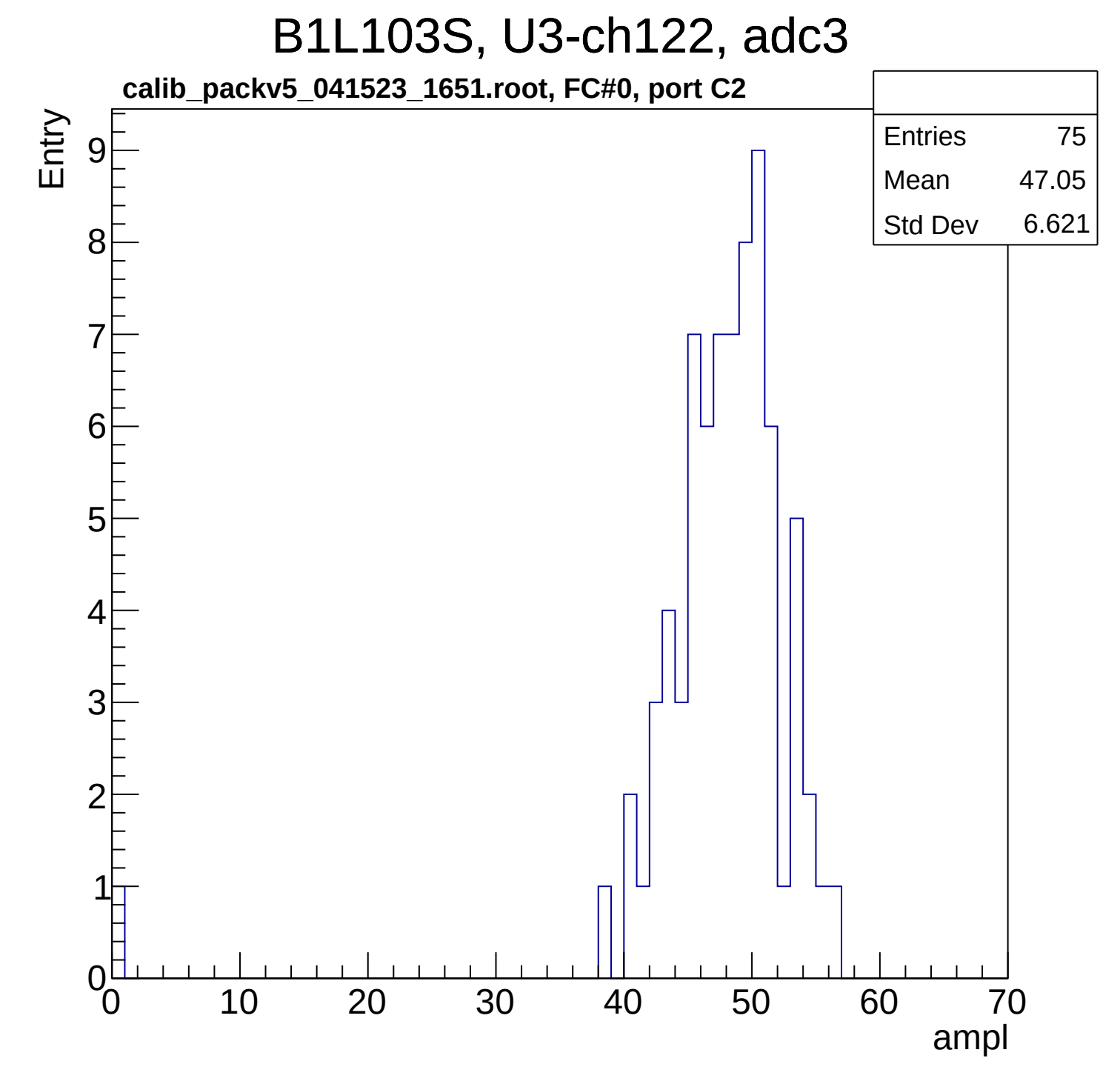
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch122, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 47.05
Std Dev 6.621
Entry
ampl
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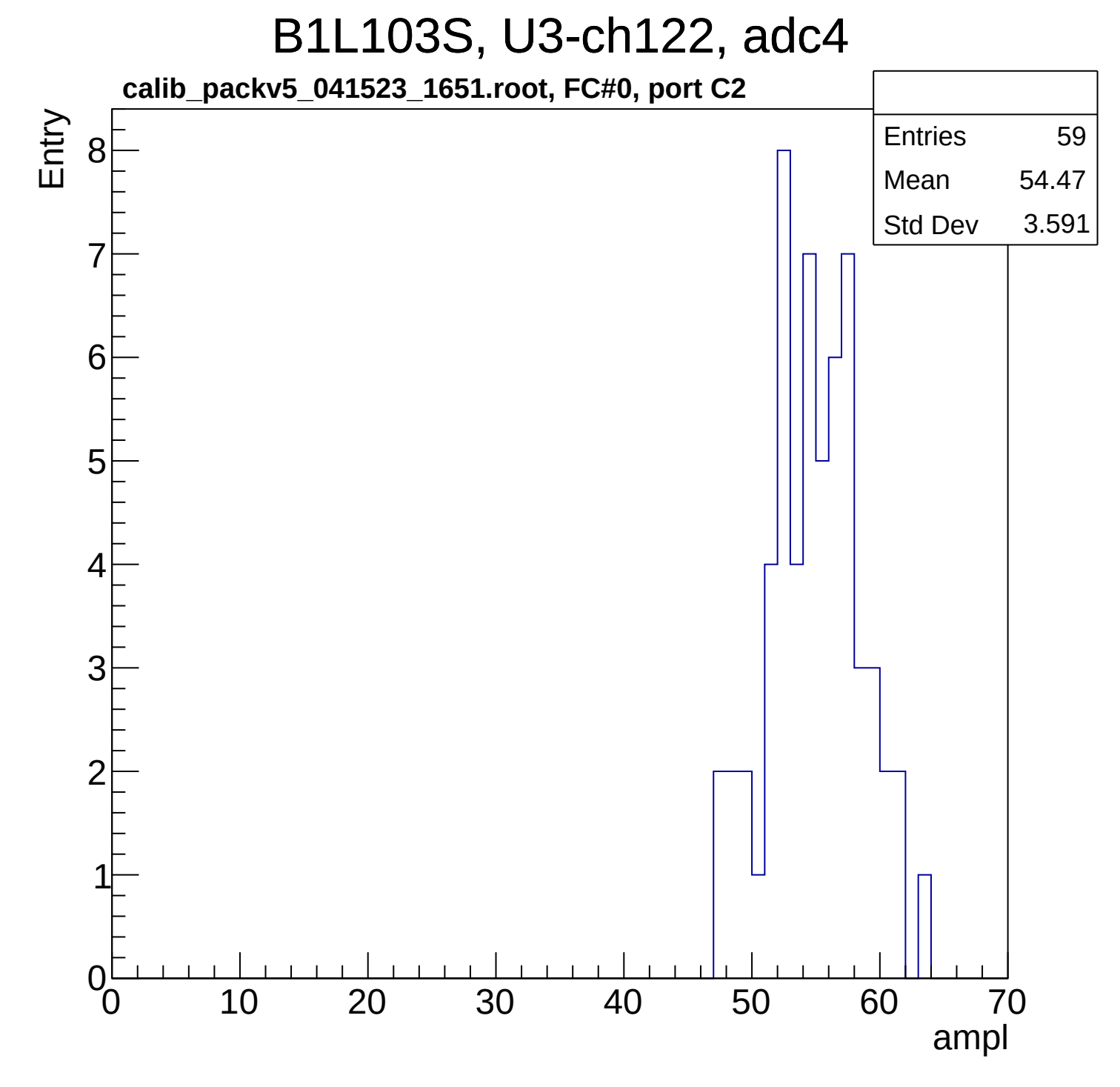
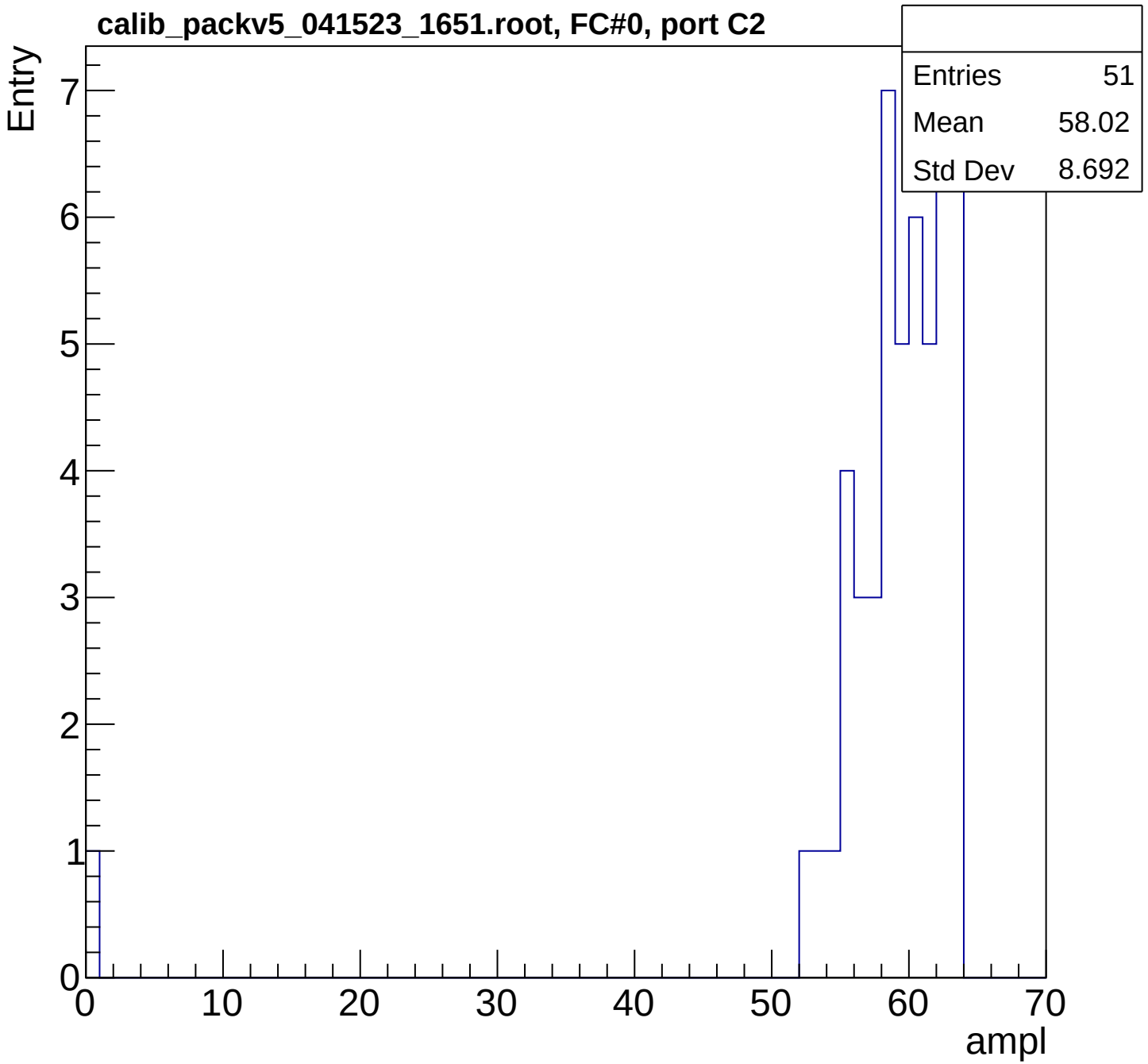
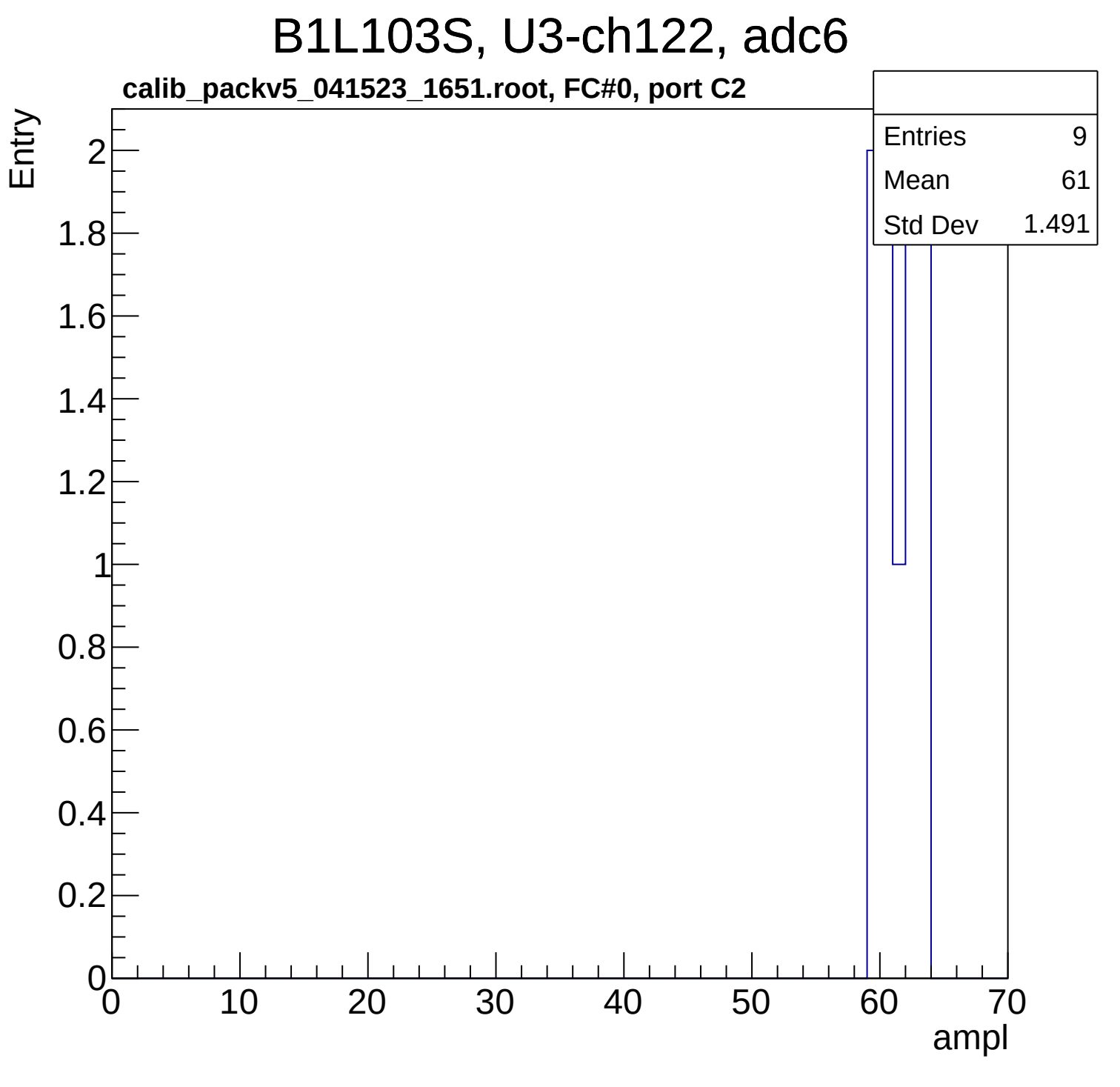
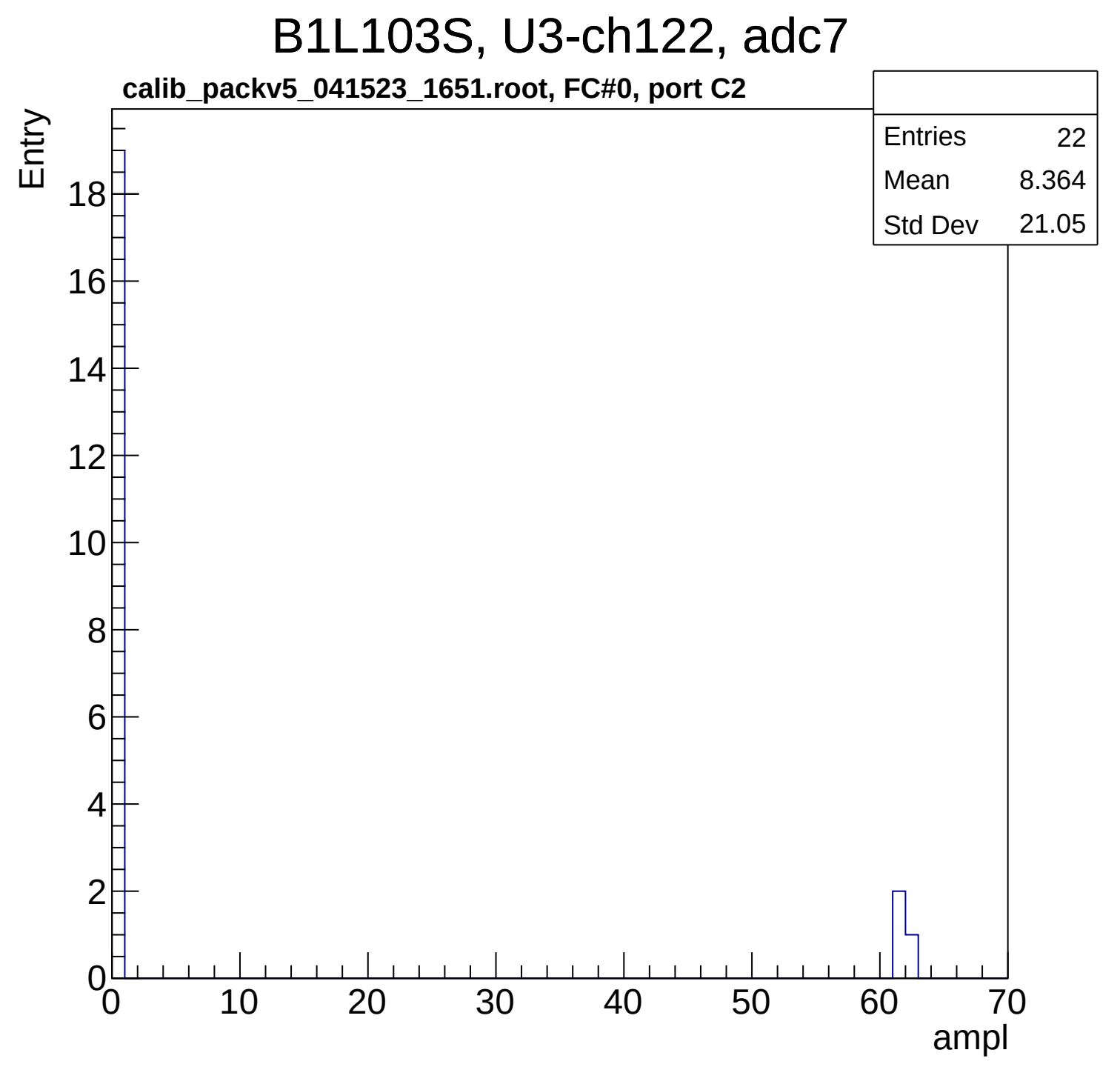
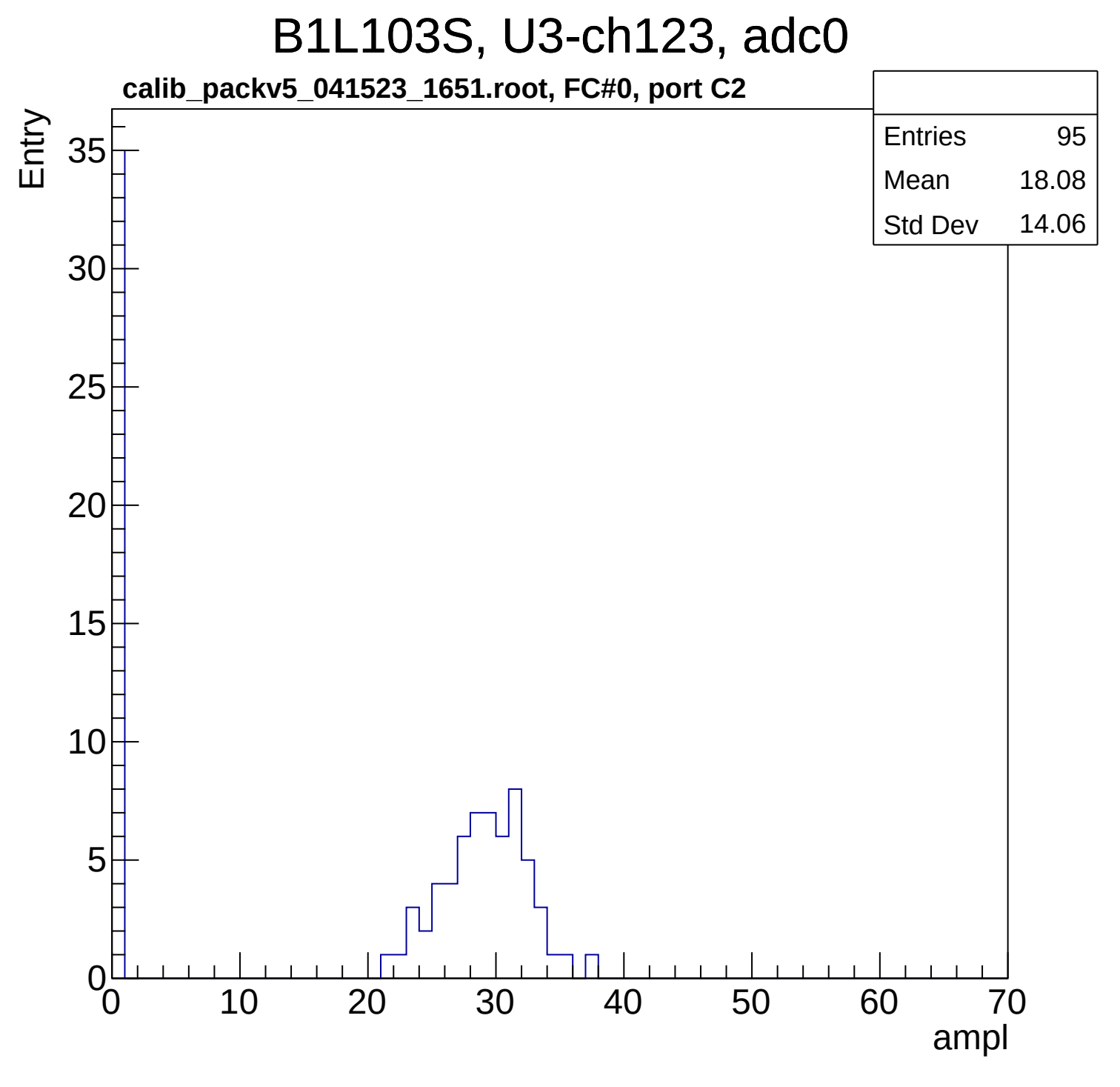
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

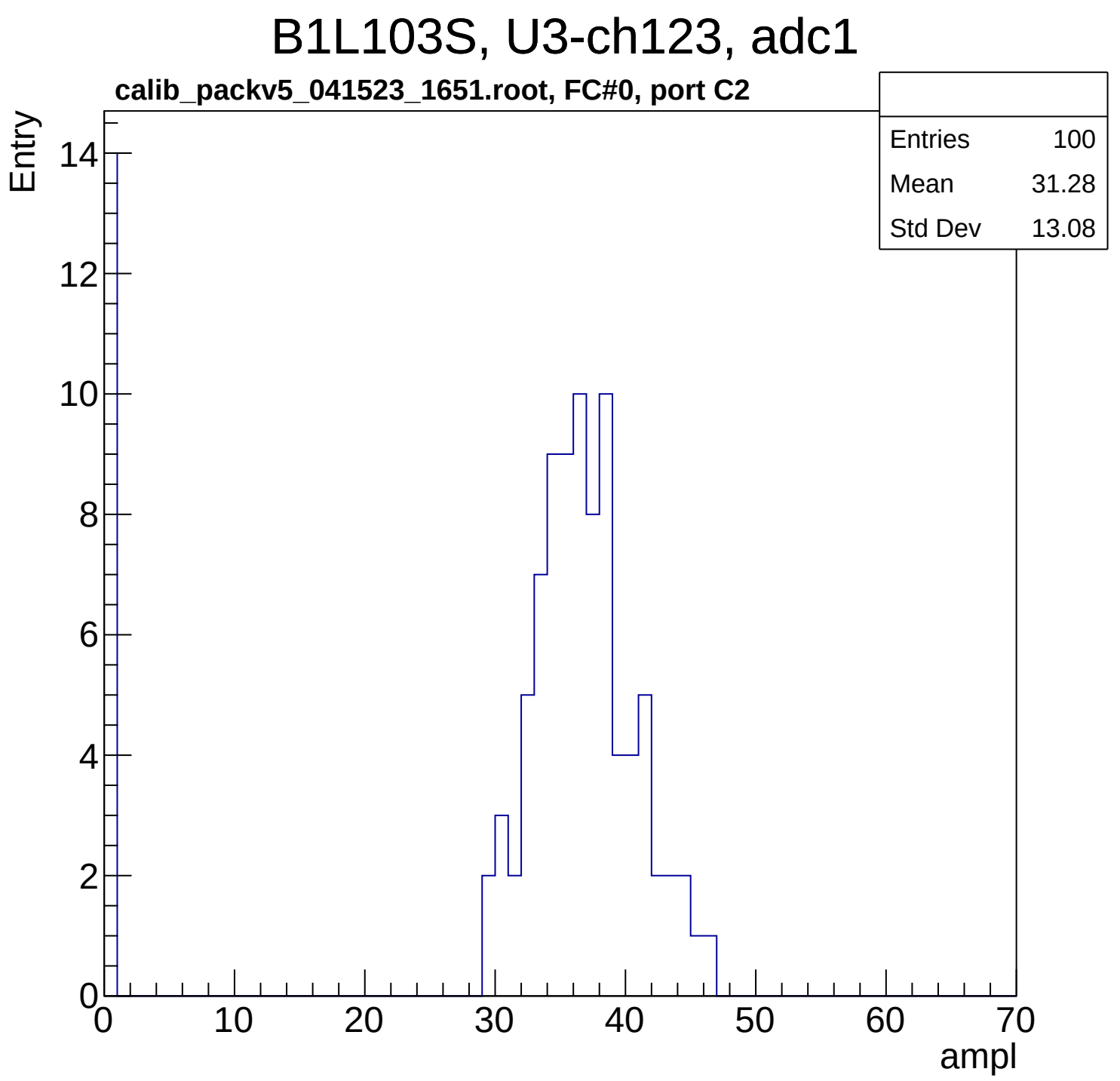

B1L103S, U3-ch122, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 54.47
Std Dev 3.591
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch122, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 58.02
Std Dev 8.692
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch122, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 61
Std Dev 1.491
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U3-ch122, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.364
Std Dev 21.05
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch123, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 18.08
Std Dev 14.06
Entry
ampl
0
5
10
15
20
25
30
35
0
10
20
30
40
50
60
70


B1L103S, U3-ch123, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 100
Mean 31.28
Std Dev 13.08
Entry
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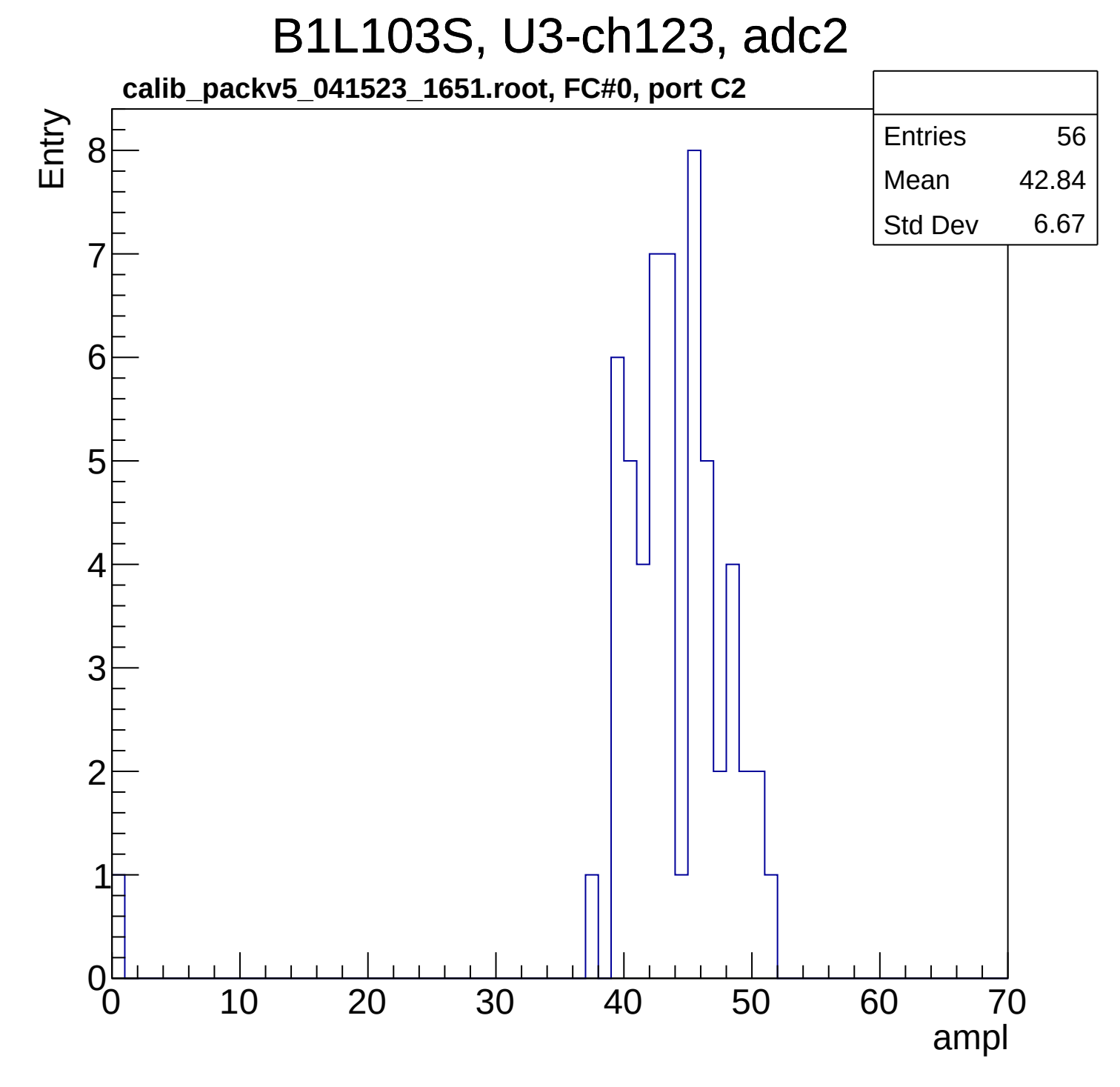
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch123, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 42.84
Std Dev 6.67
Entry
ampl
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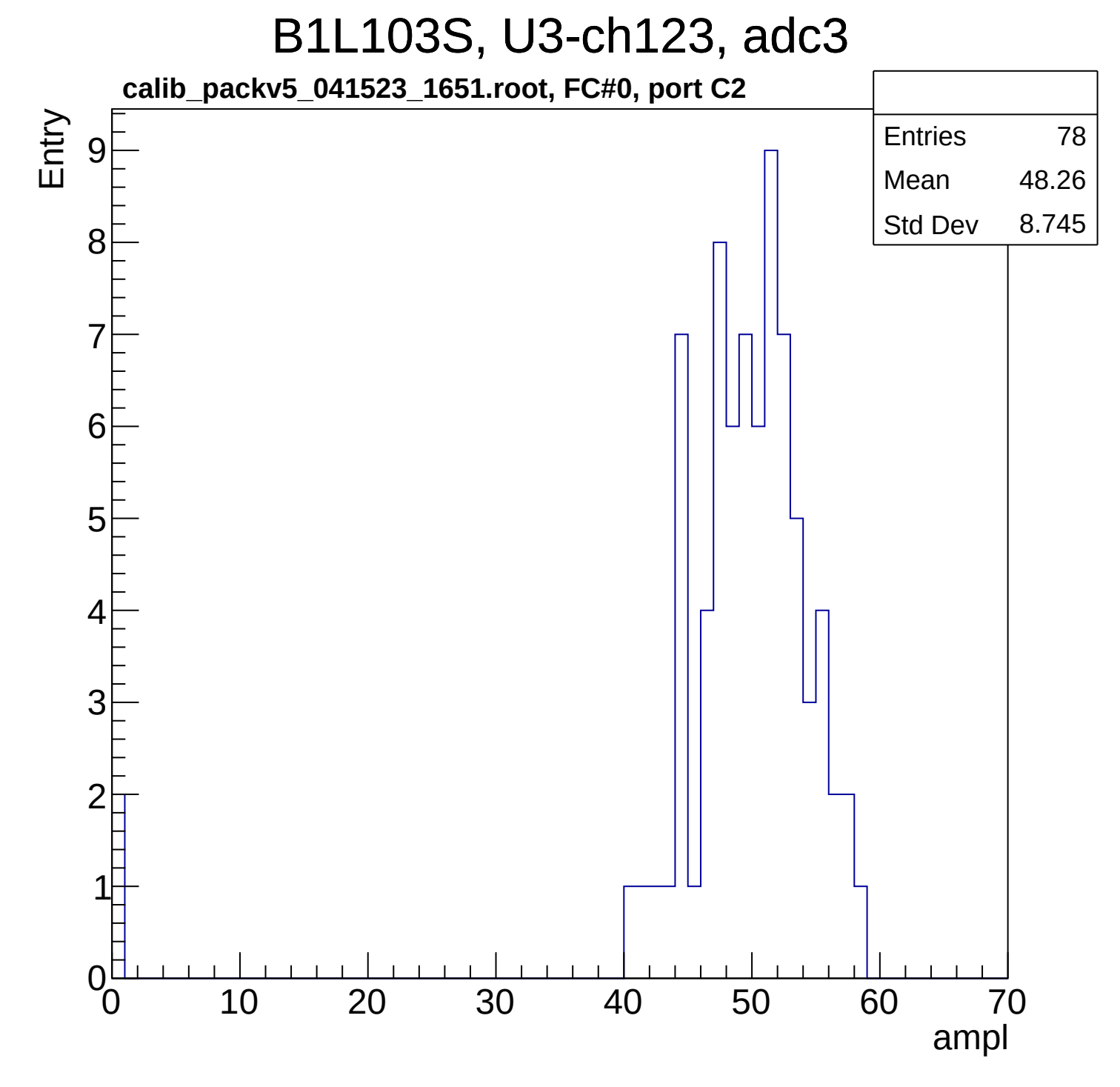
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch123, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 48.26
Std Dev 8.745
Entry
ampl
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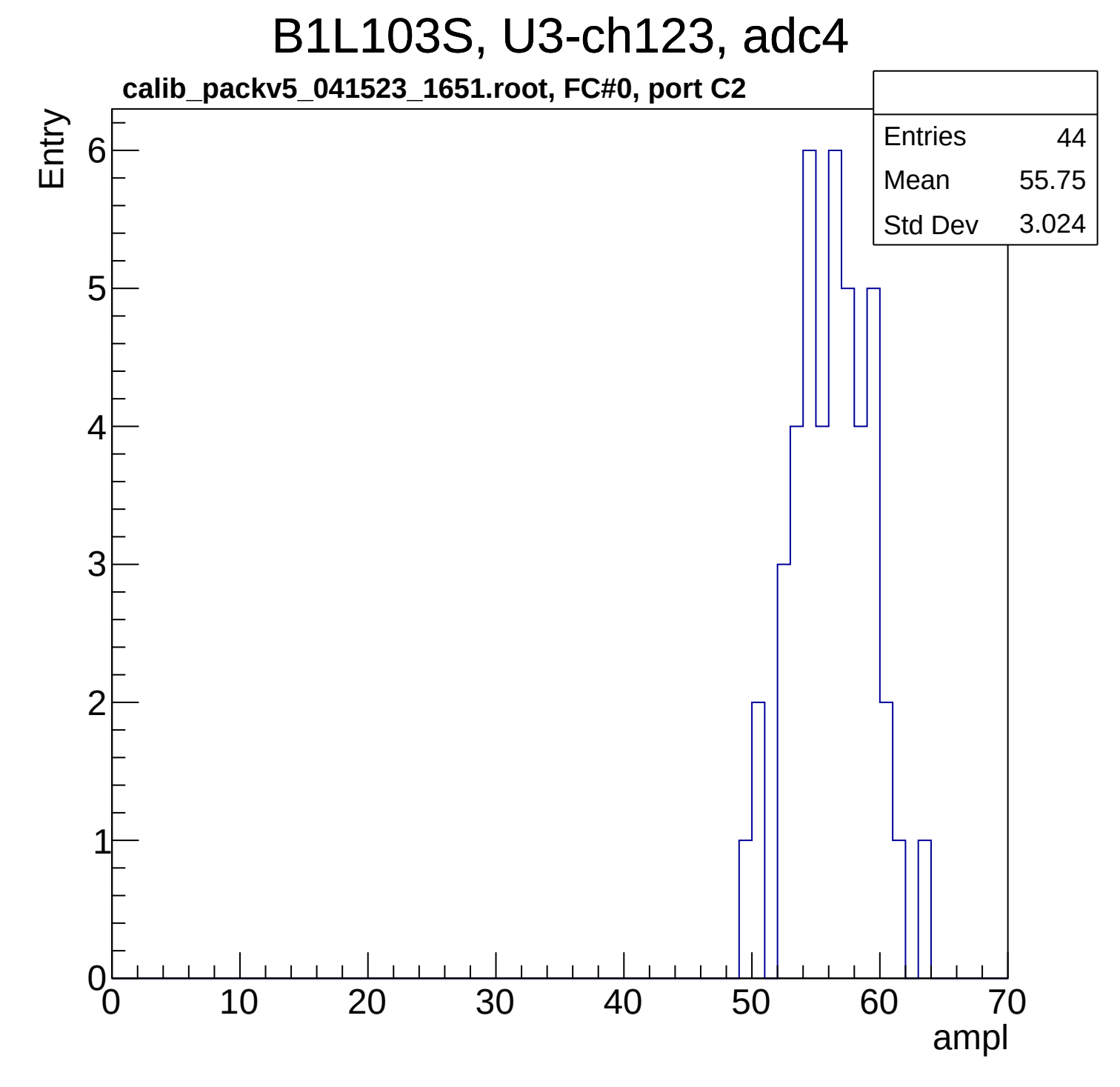
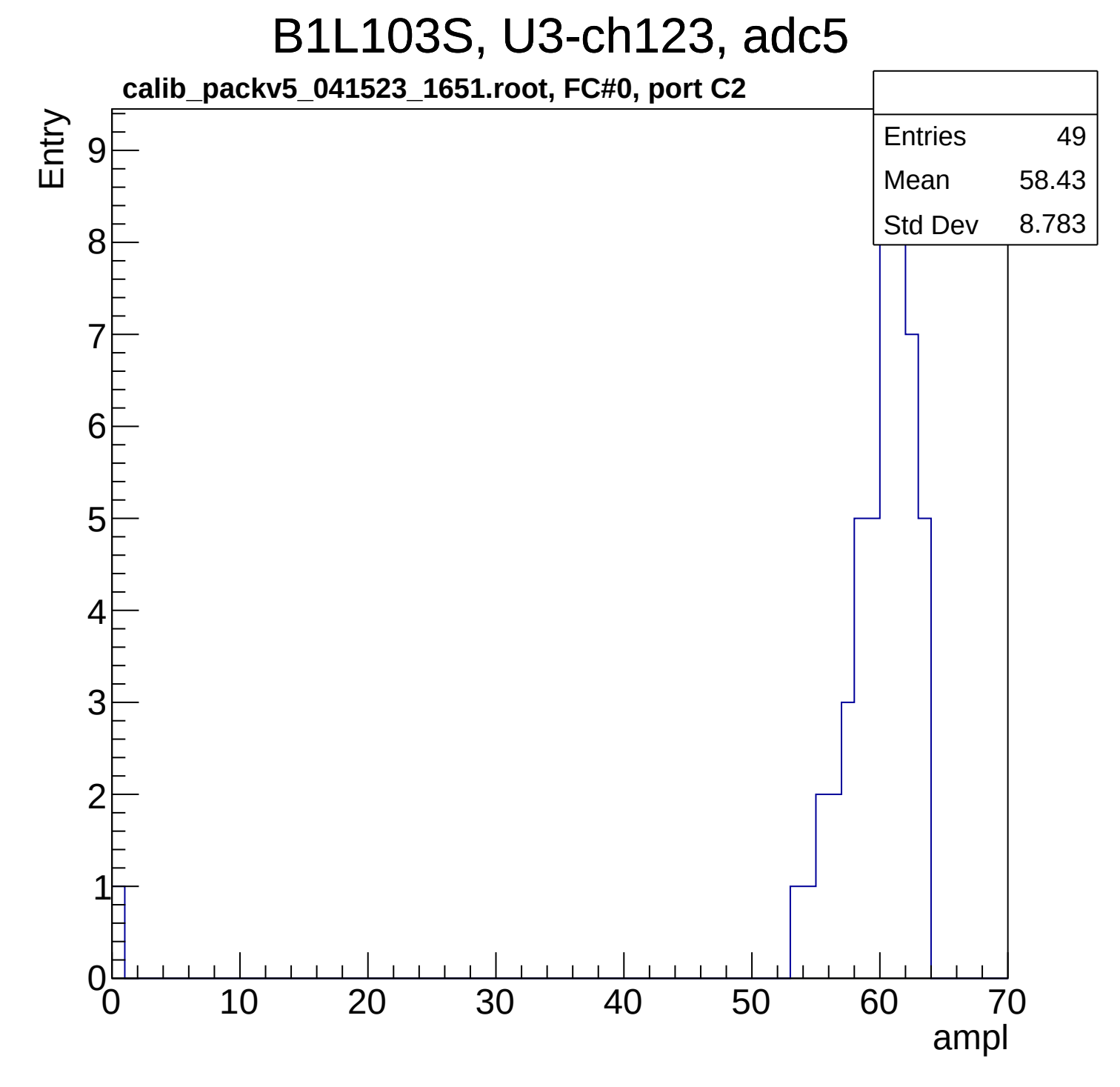
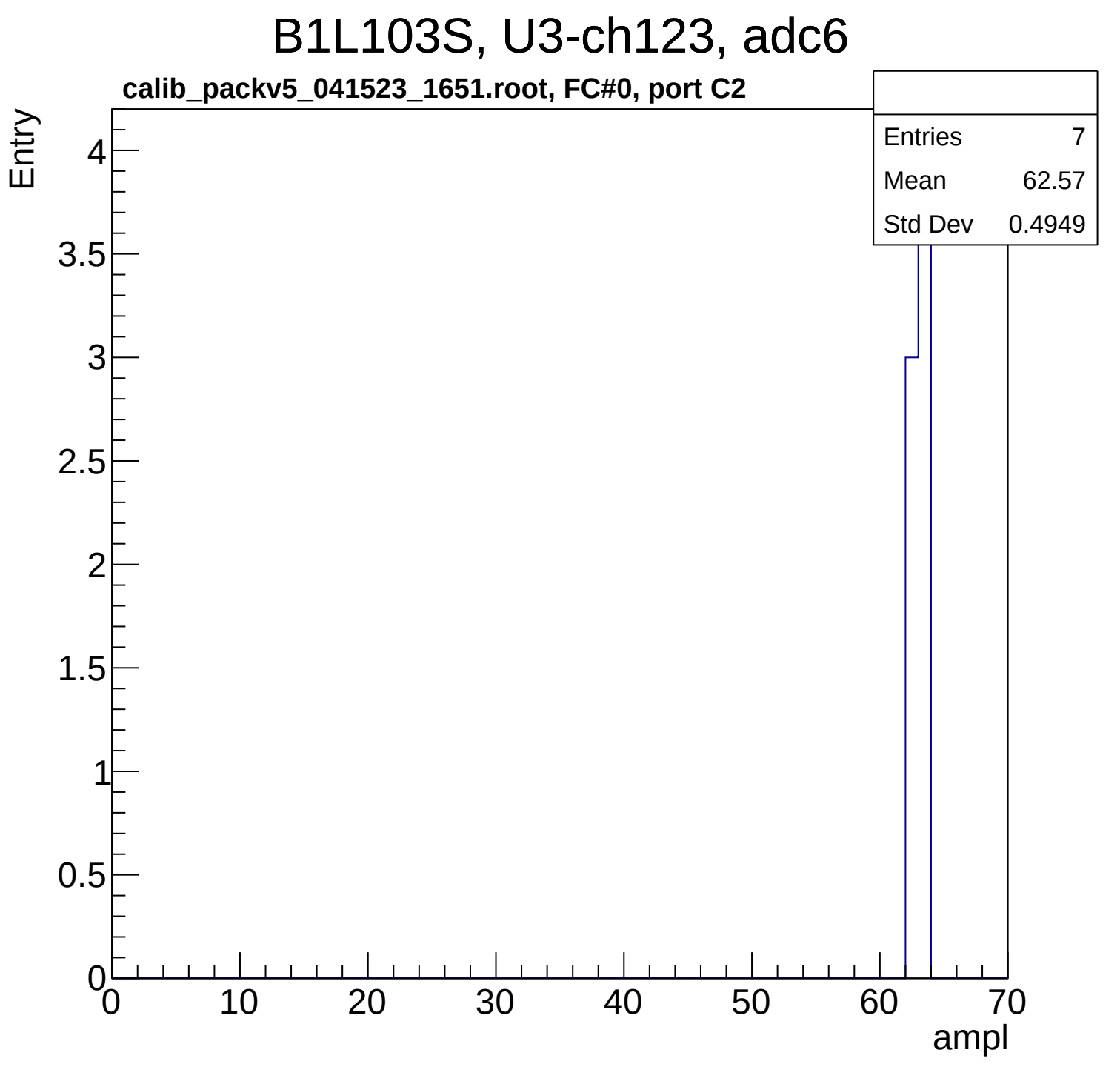
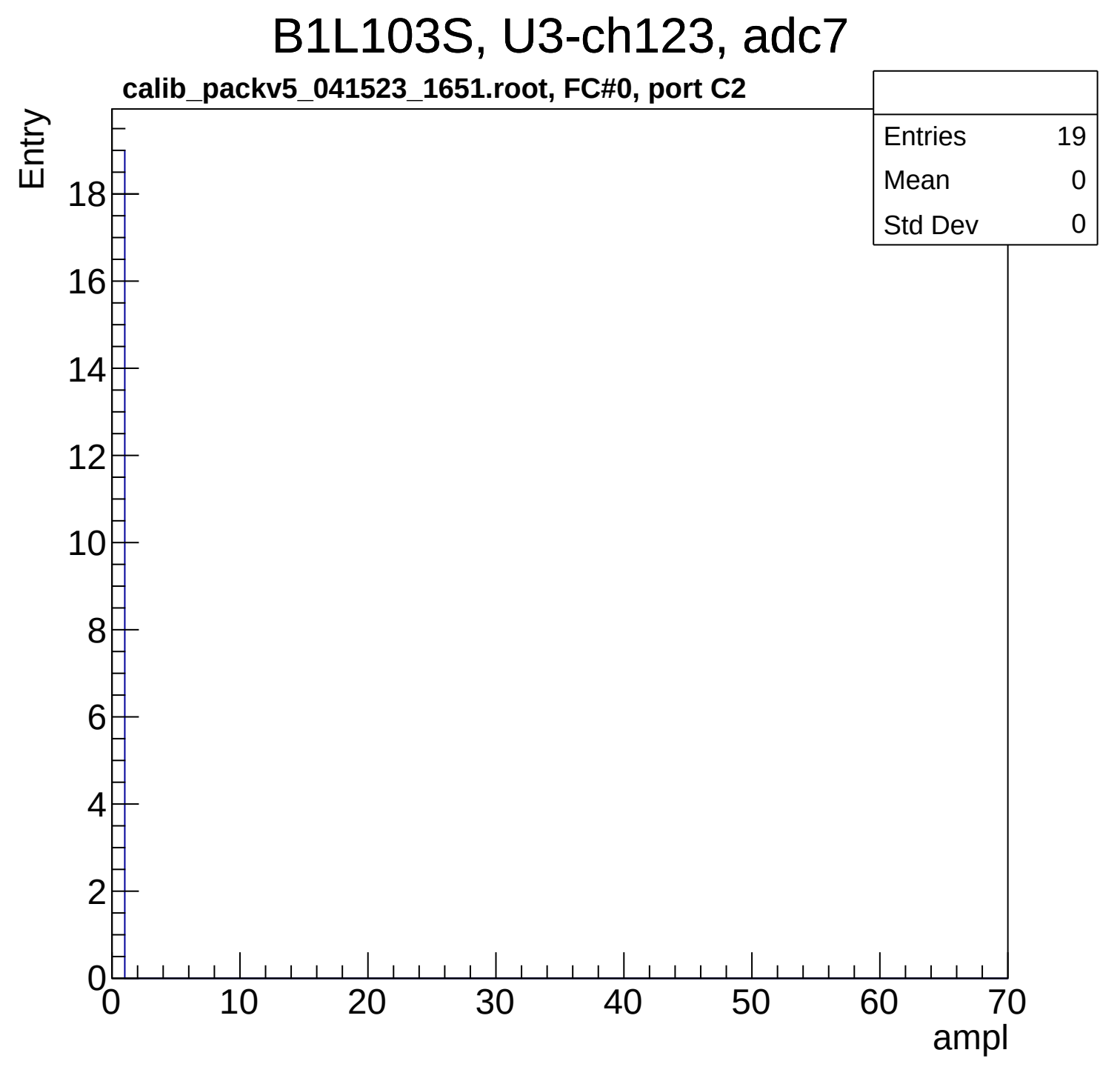
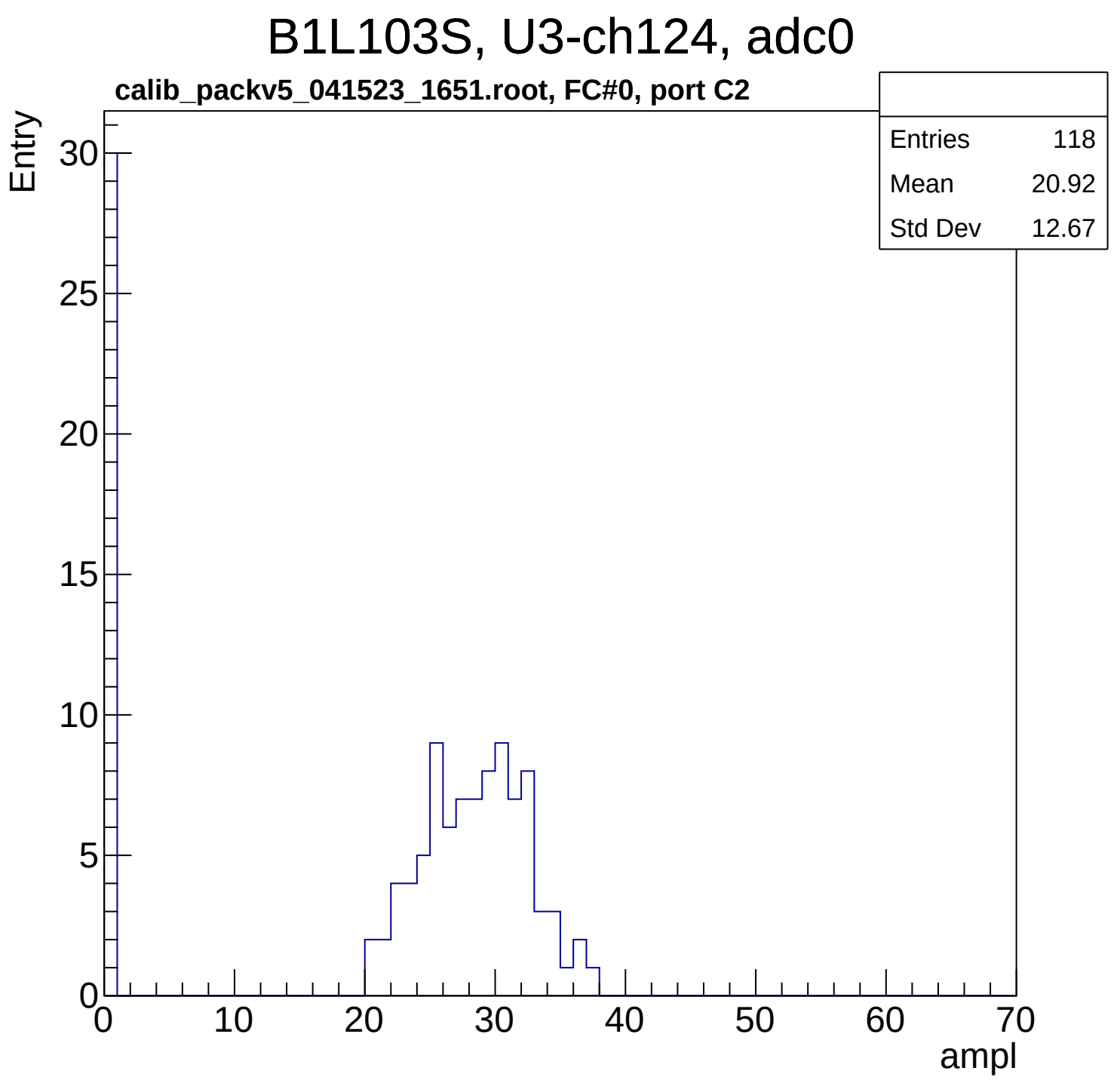
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

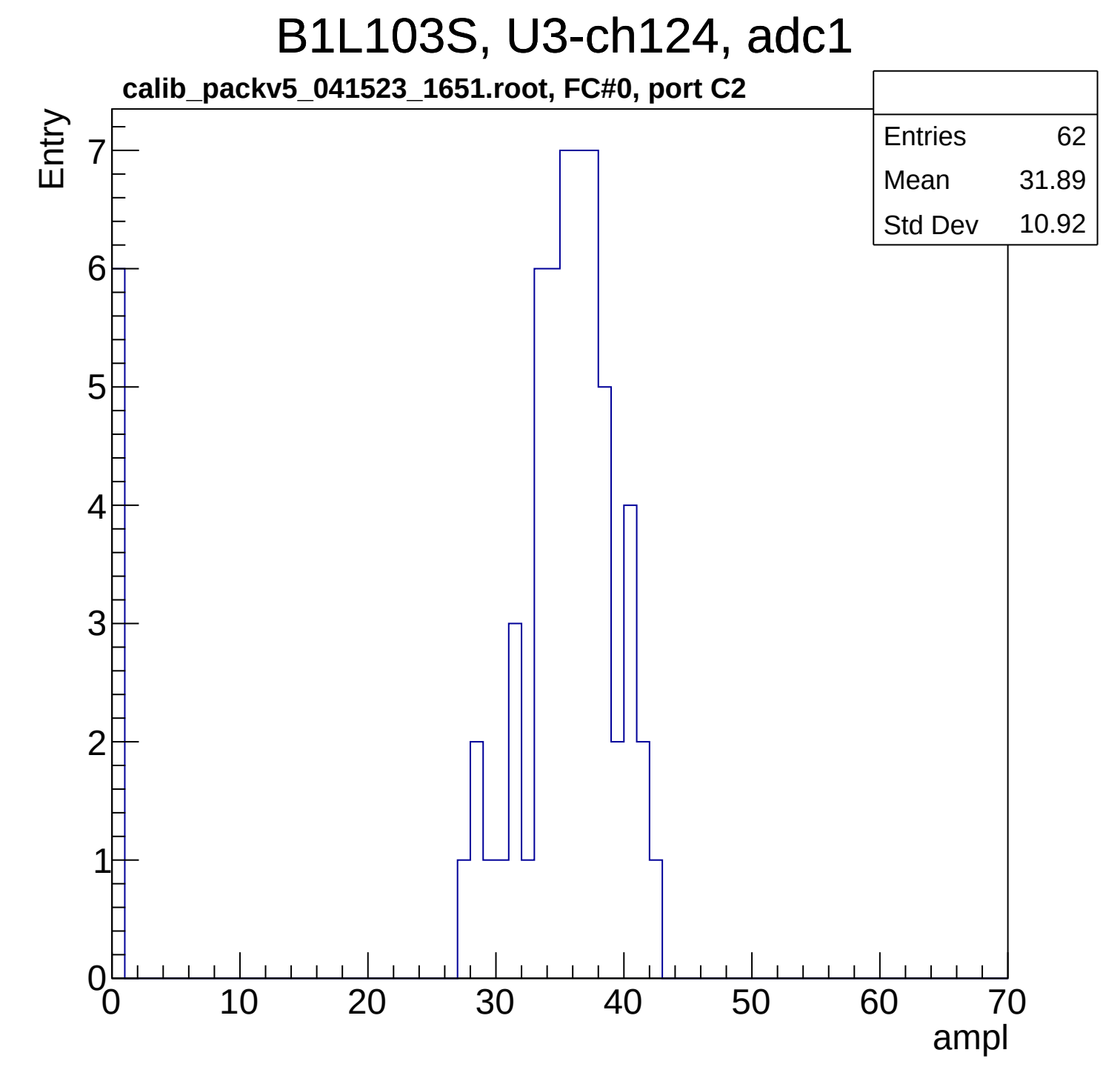

B1L103S, U3-ch123, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 55.75
Std Dev 3.024
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch123, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 58.43
Std Dev 8.783
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch123, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 62.57
Std Dev 0.4949
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U3-ch123, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch124, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 118
Mean 20.92
Std Dev 12.67
Entry
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch124, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 31.89
Std Dev 10.92
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
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60
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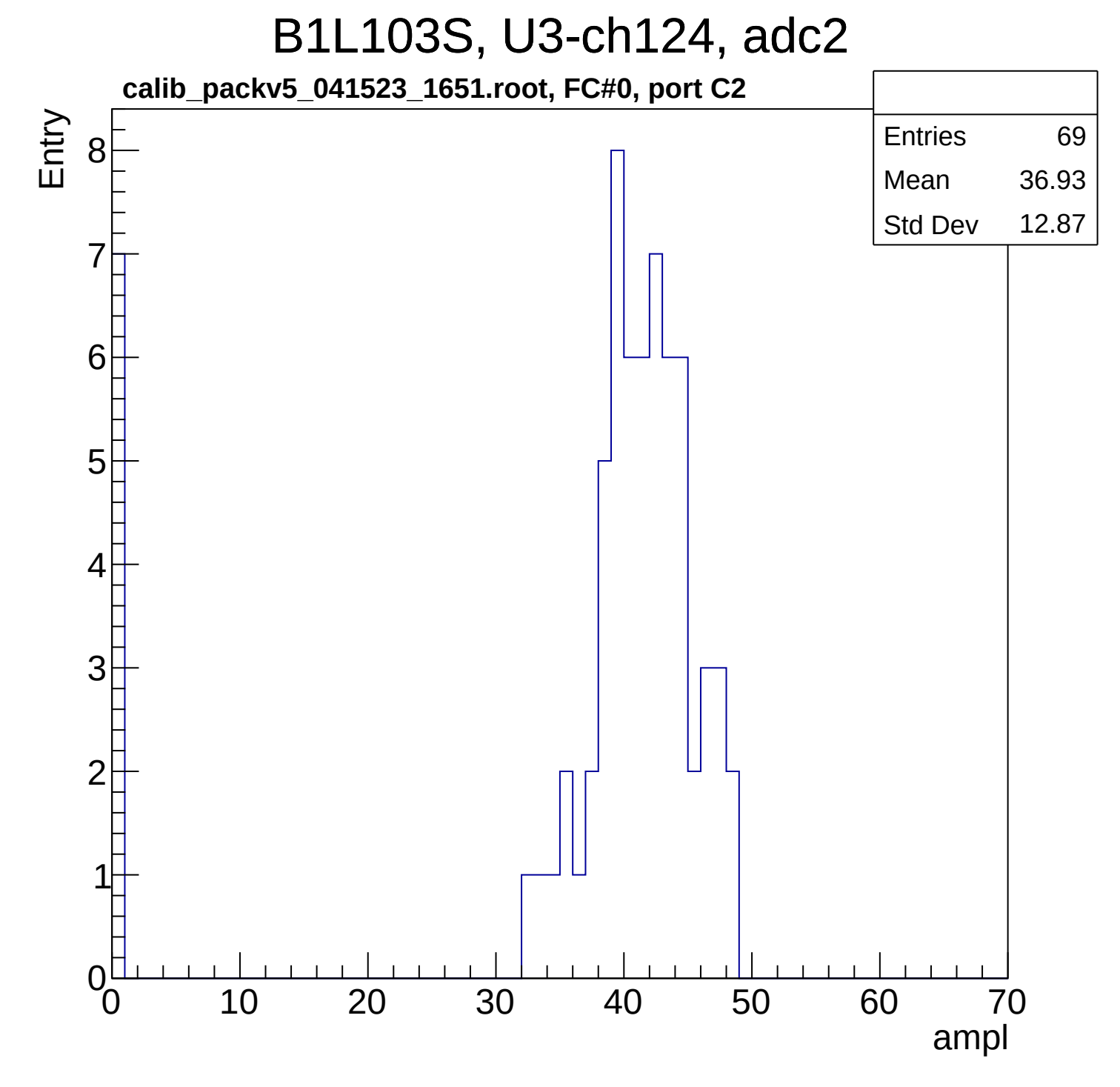
B1L103S, U3-ch124, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 36.93
Std Dev 12.87
Entry
ampl
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2
3
4
5
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7
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0
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40
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60
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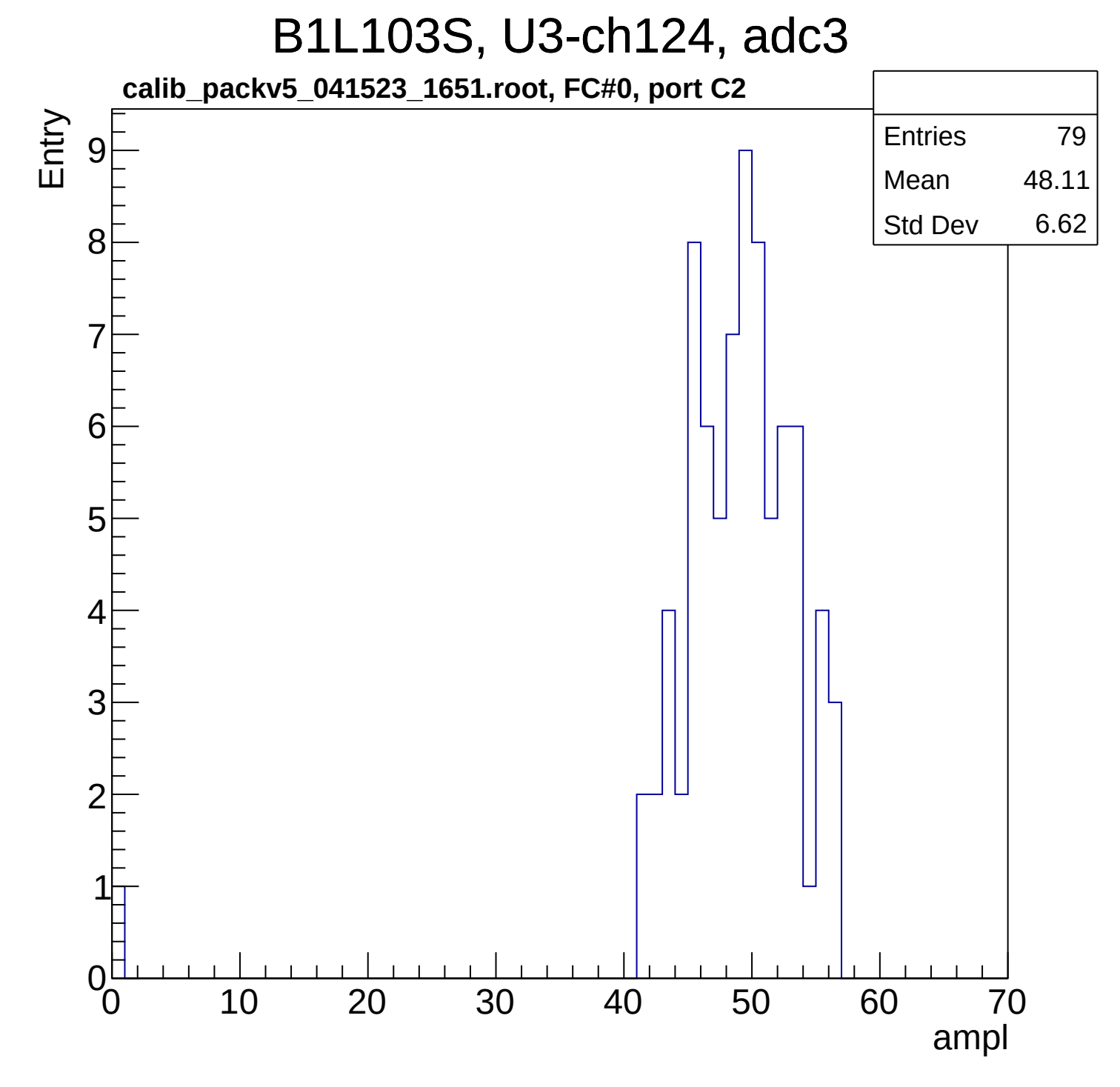
B1L103S, U3-ch124, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 48.11
Std Dev 6.62
Entry
ampl
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2
3
4
5
6
7
8
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0
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60
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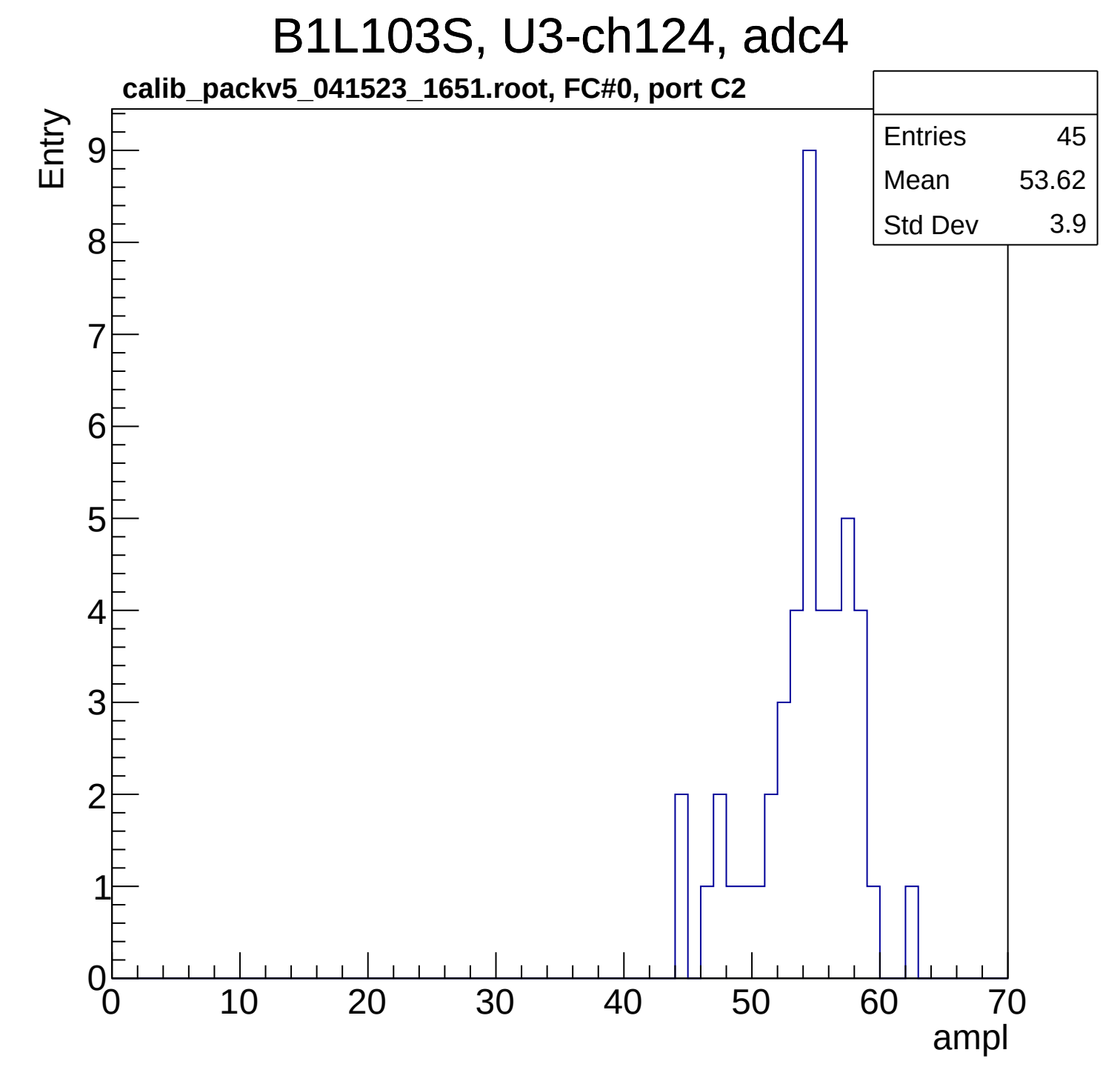
B1L103S, U3-ch124, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 53.62
Std Dev 3.9
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
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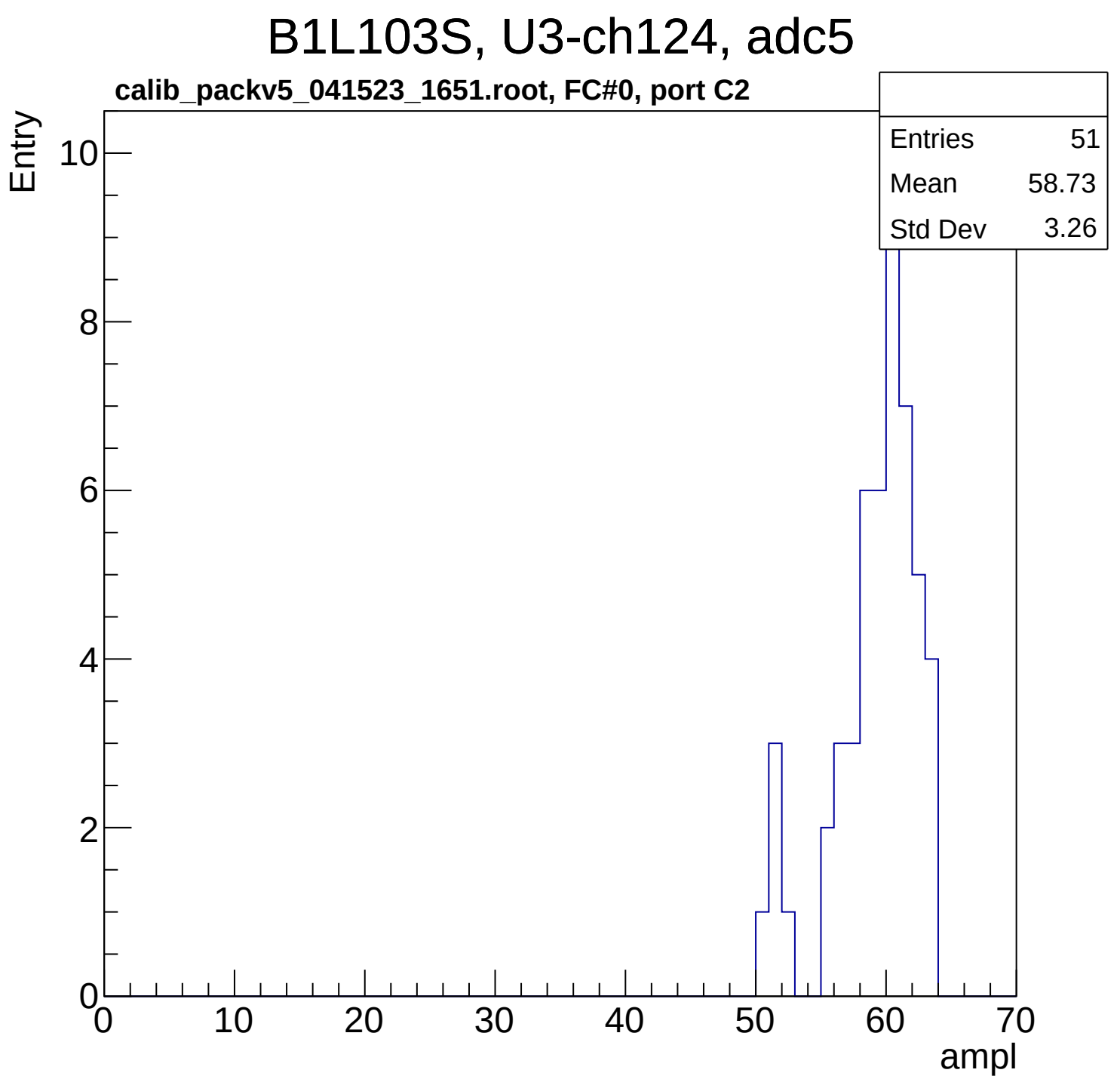
60
70


B1L103S, U3-ch124, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 58.73
Std Dev 3.26
Entry
0
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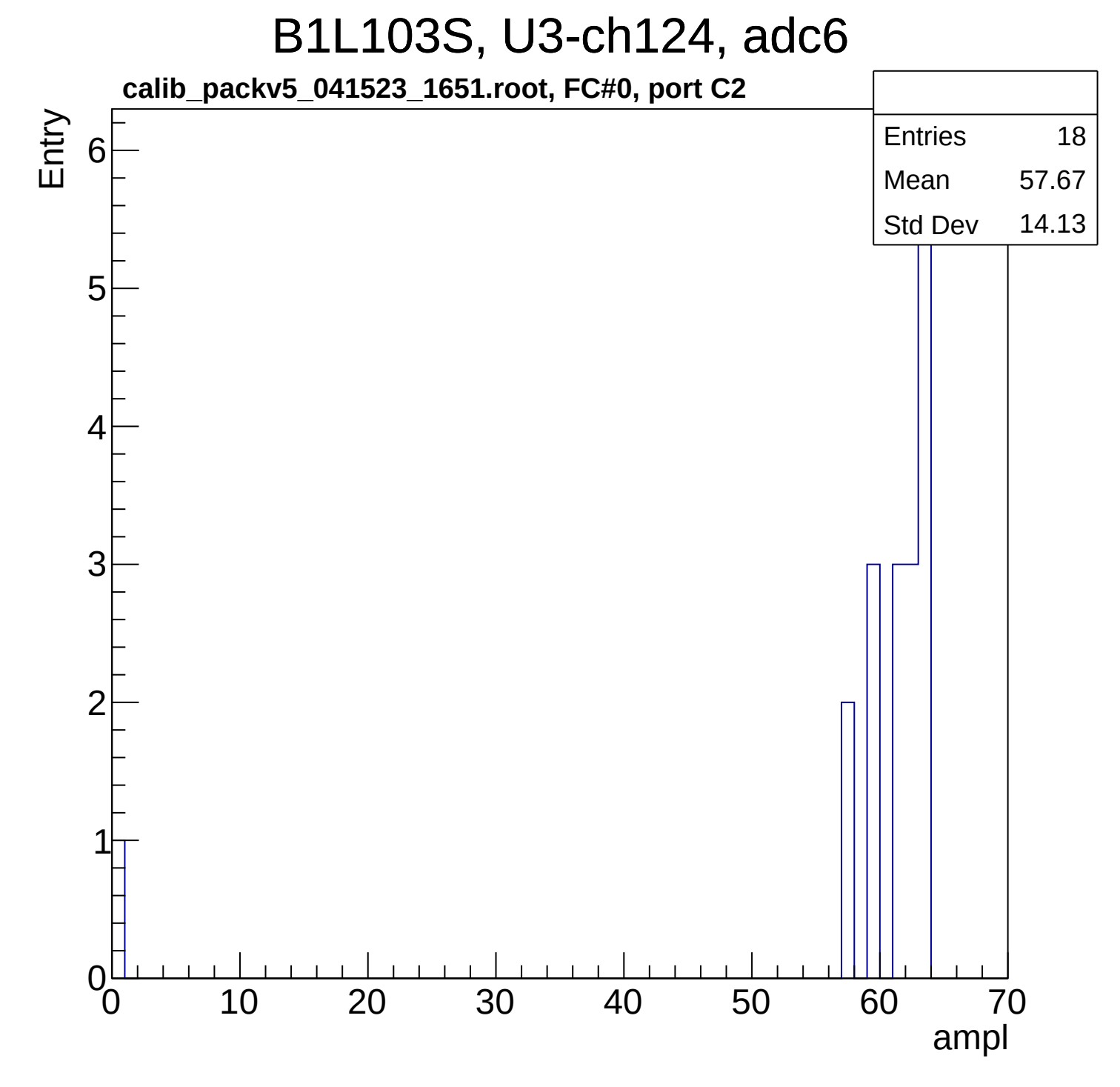
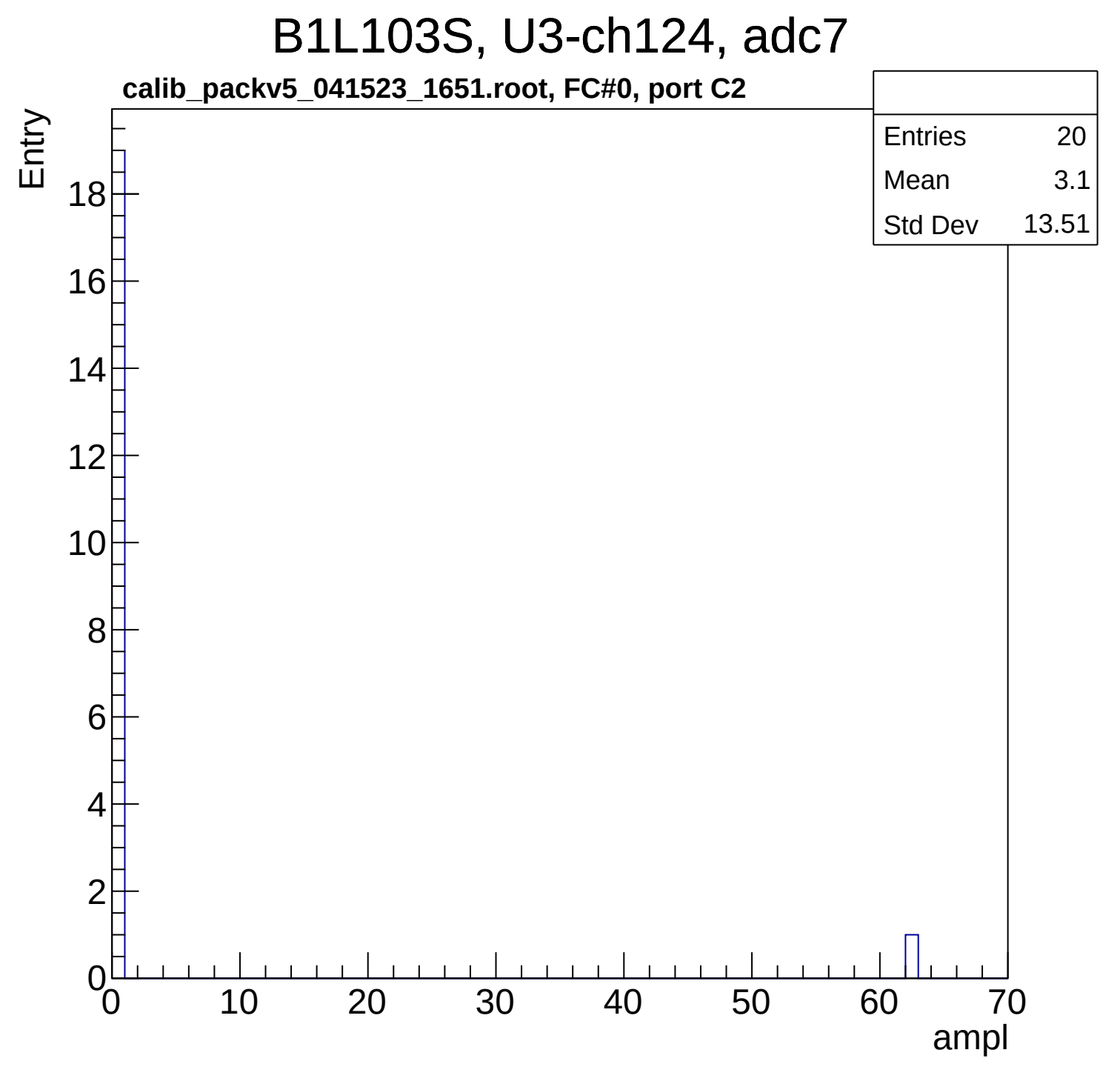
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch124, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 57.67
Std Dev 14.13
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch124, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
2
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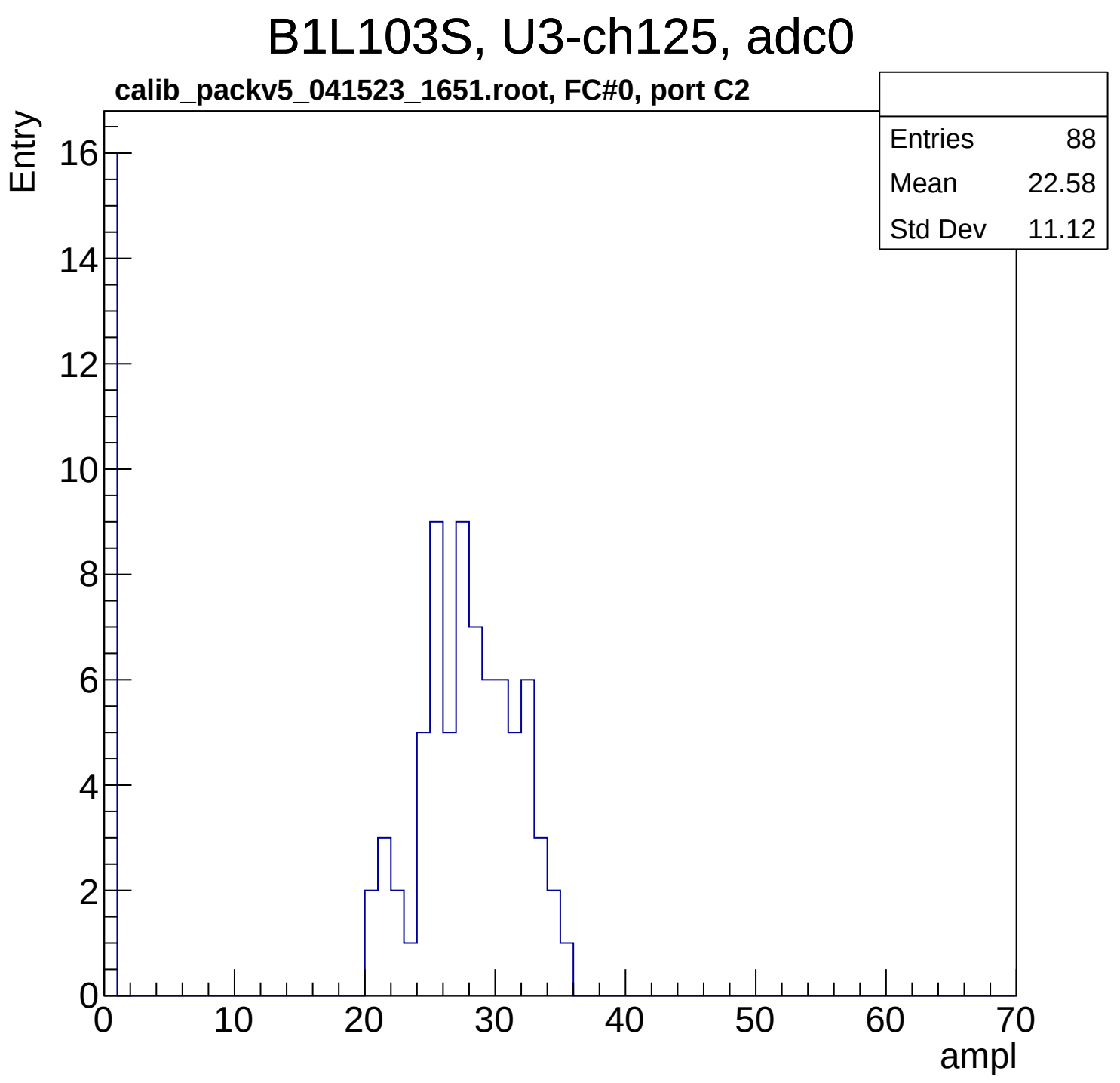
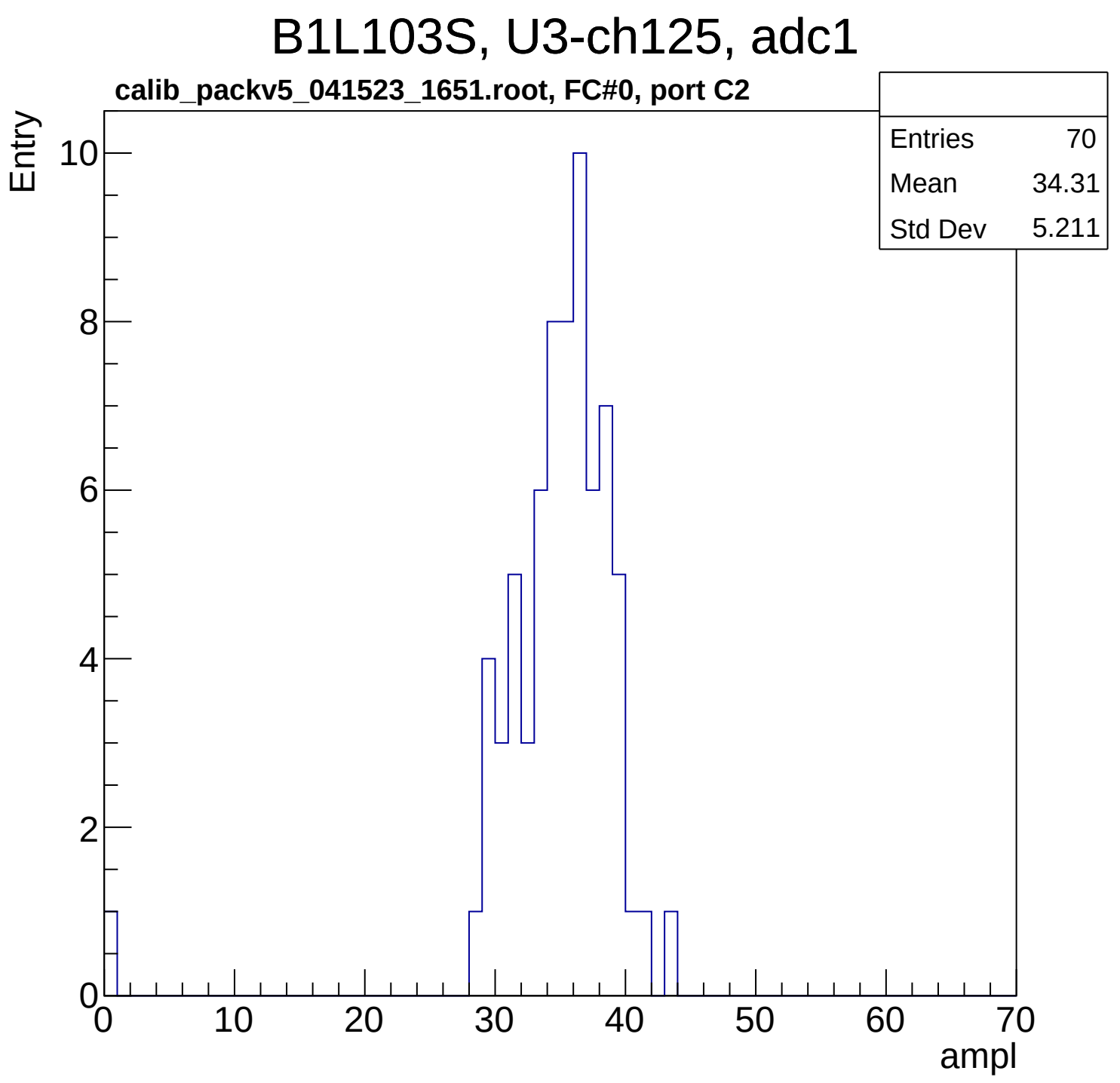
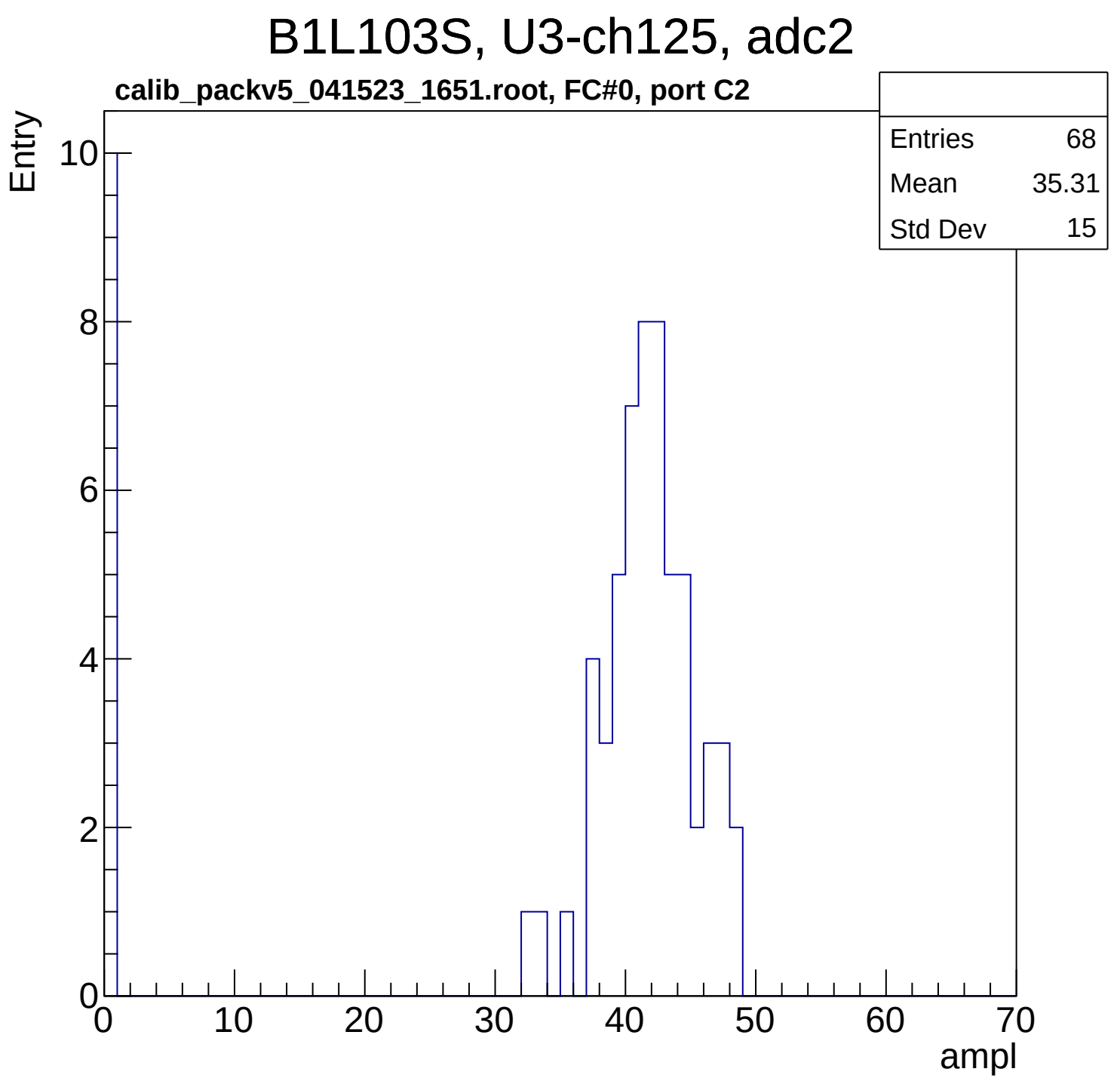
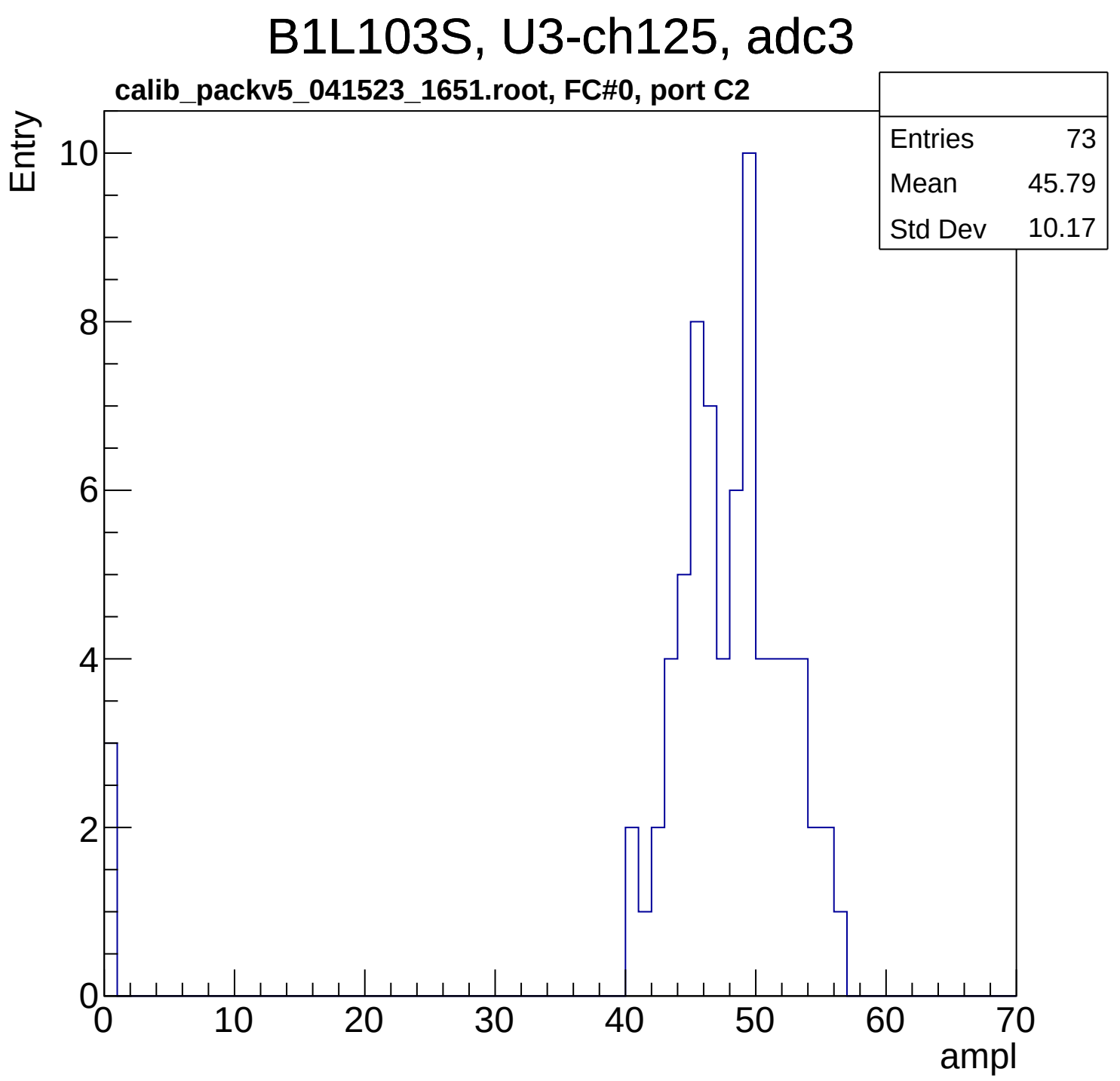
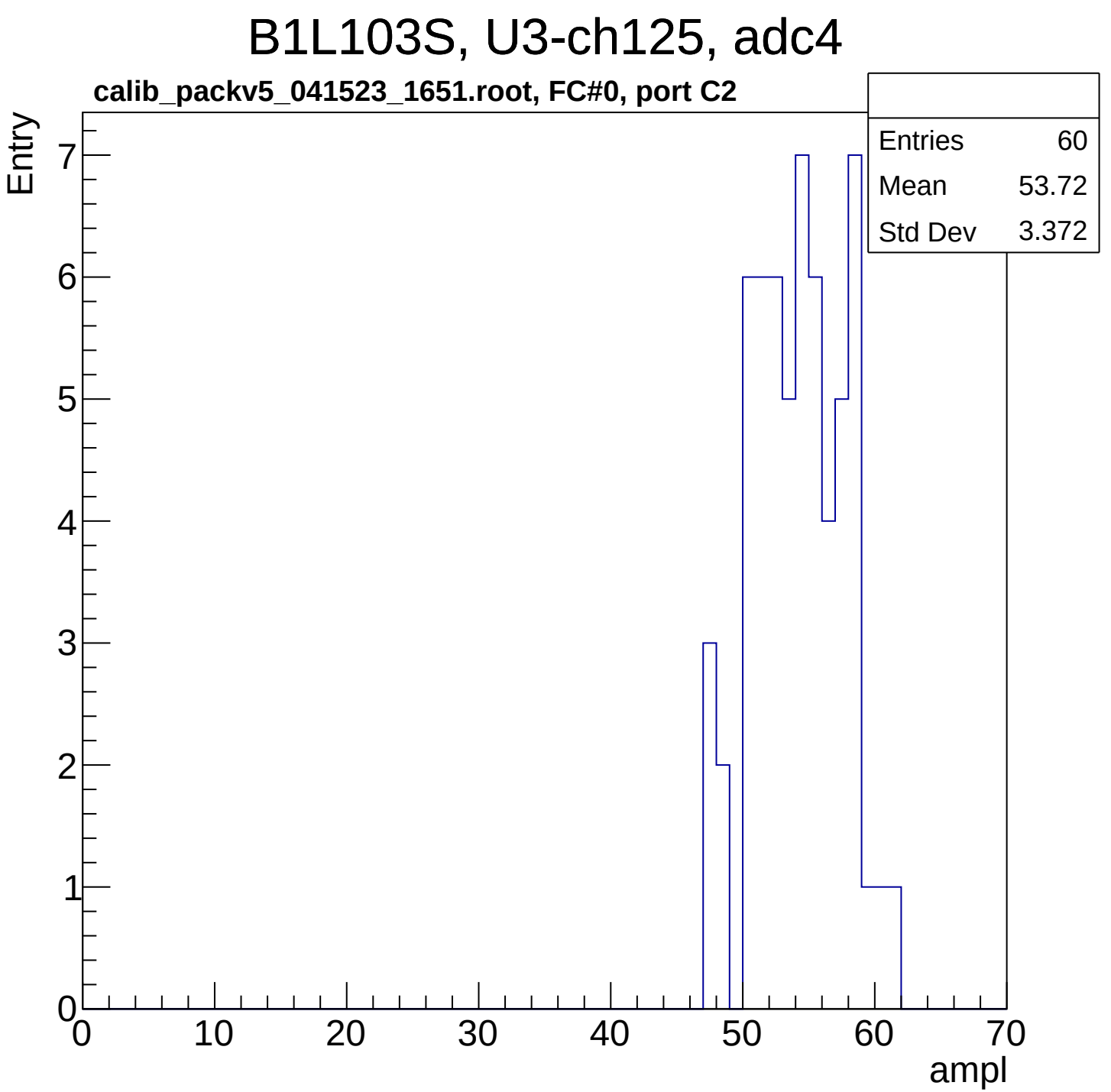
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

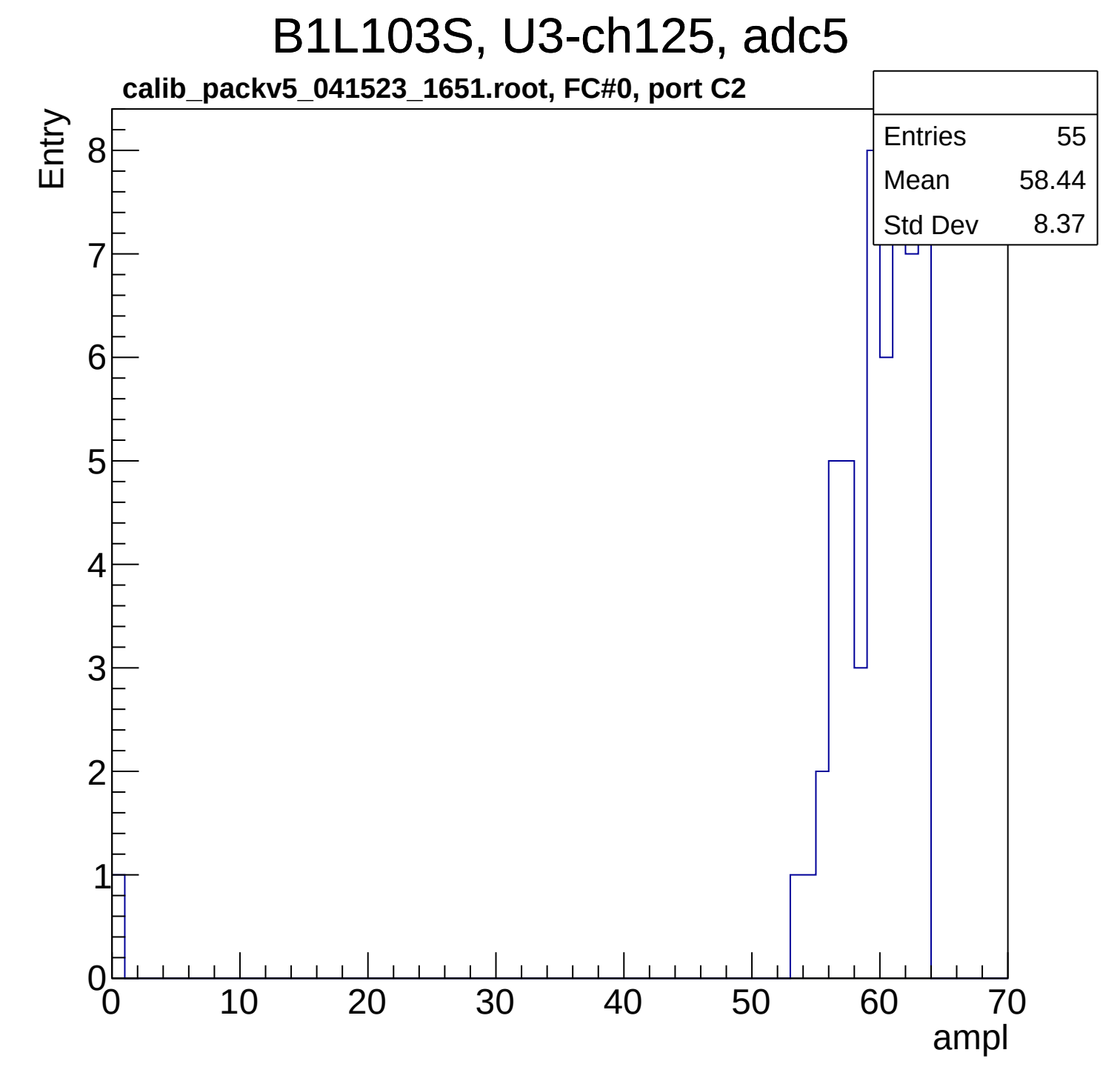

B1L103S, U3-ch125, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 22.58
Std Dev 11.12
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L103S, U3-ch125, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 34.31
Std Dev 5.211
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch125, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 35.31
Std Dev 15
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch125, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 45.79
Std Dev 10.17
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U3-ch125, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 53.72
Std Dev 3.372
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U3-ch125, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 58.44
Std Dev 8.37
Entry
ampl
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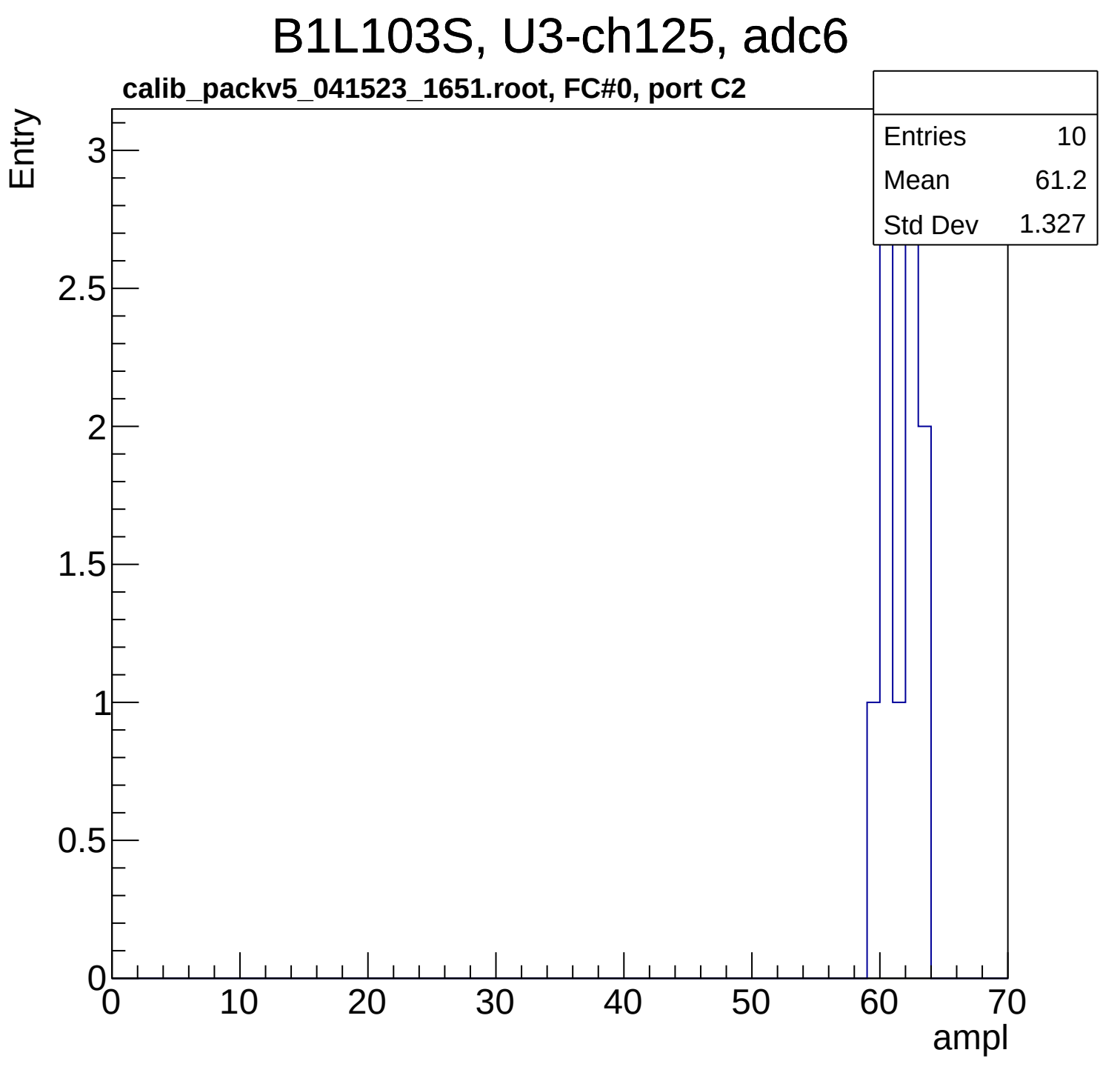
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch125, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61.2
Std Dev 1.327
Entry
ampl
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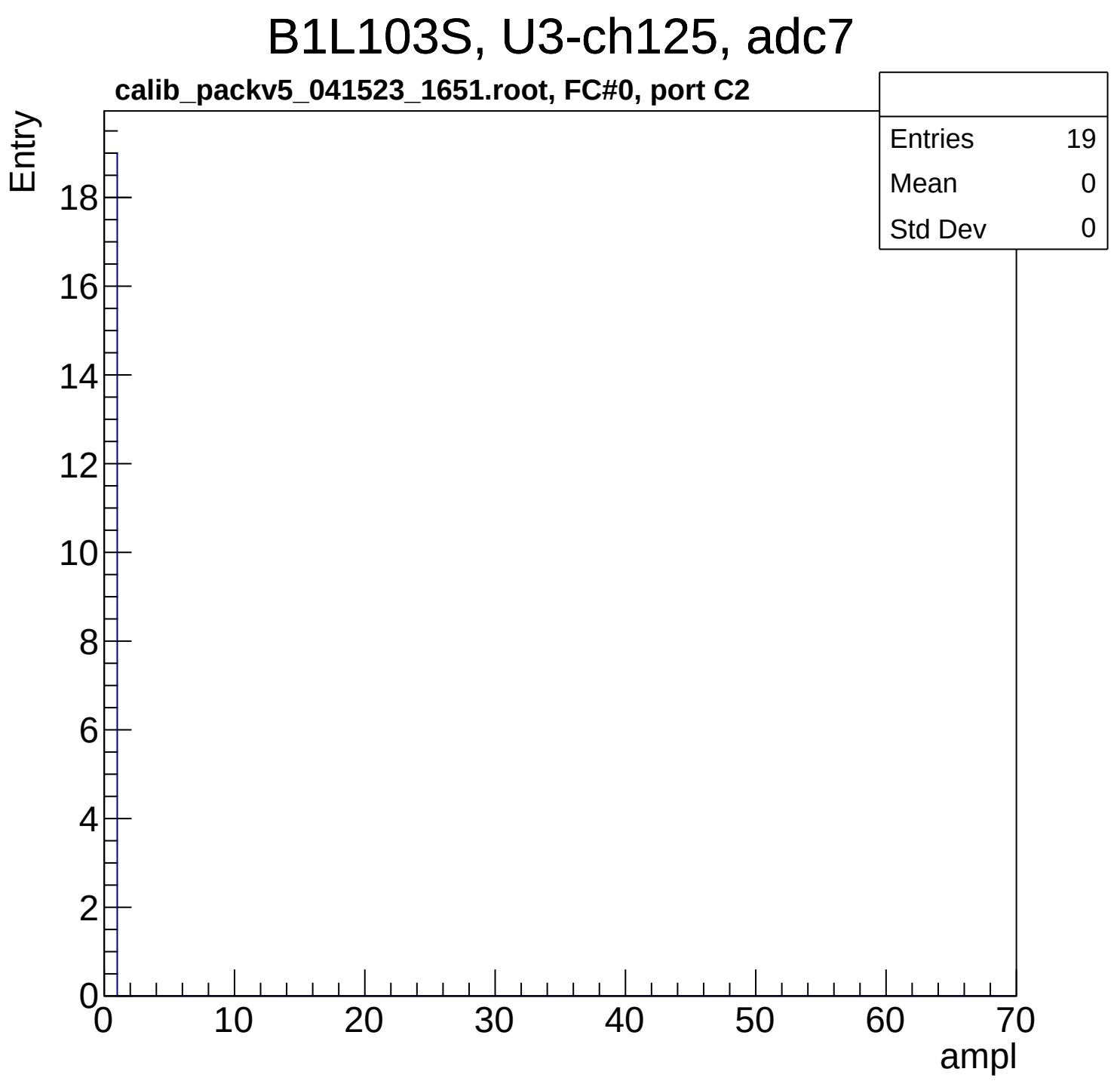
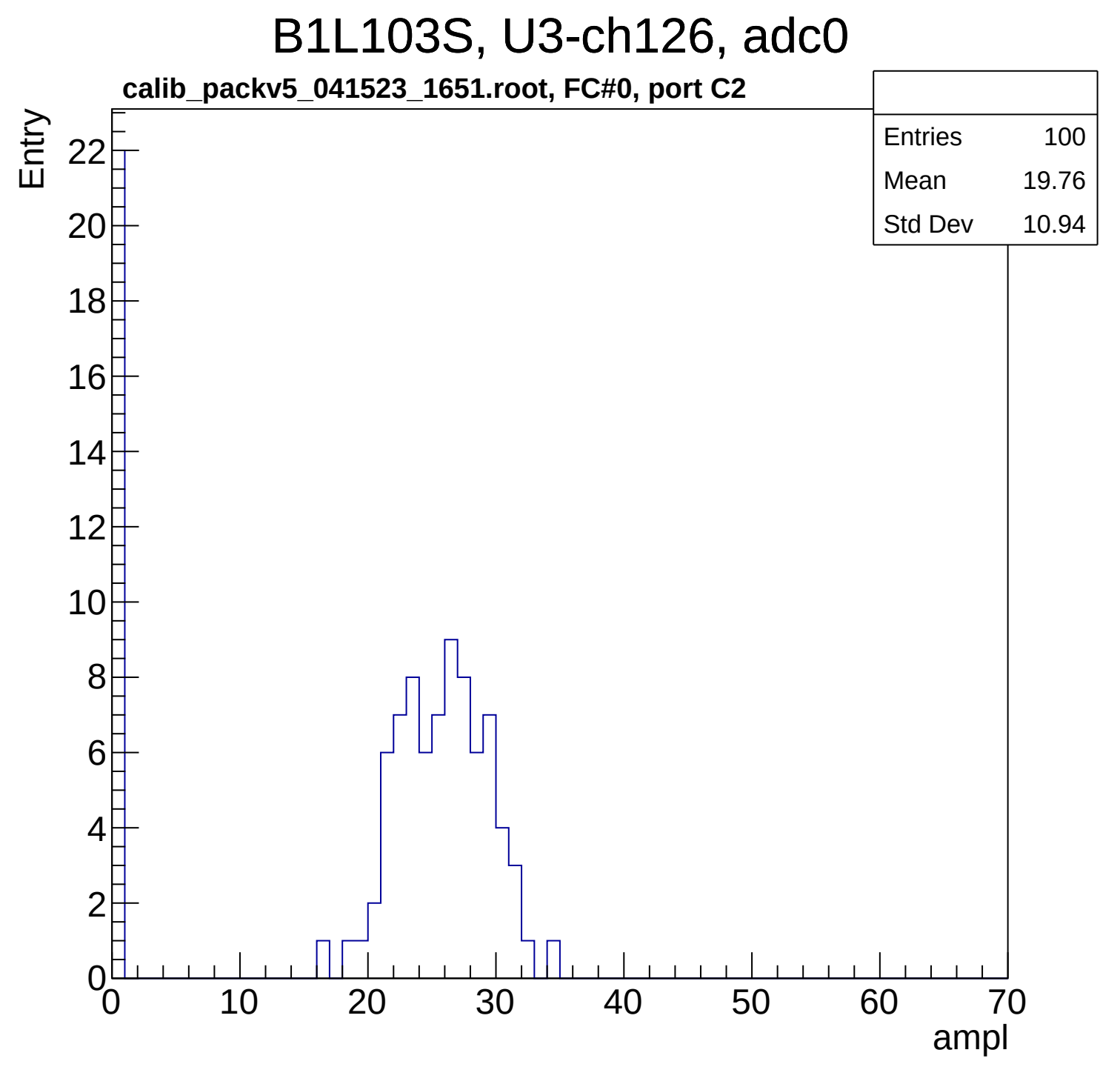
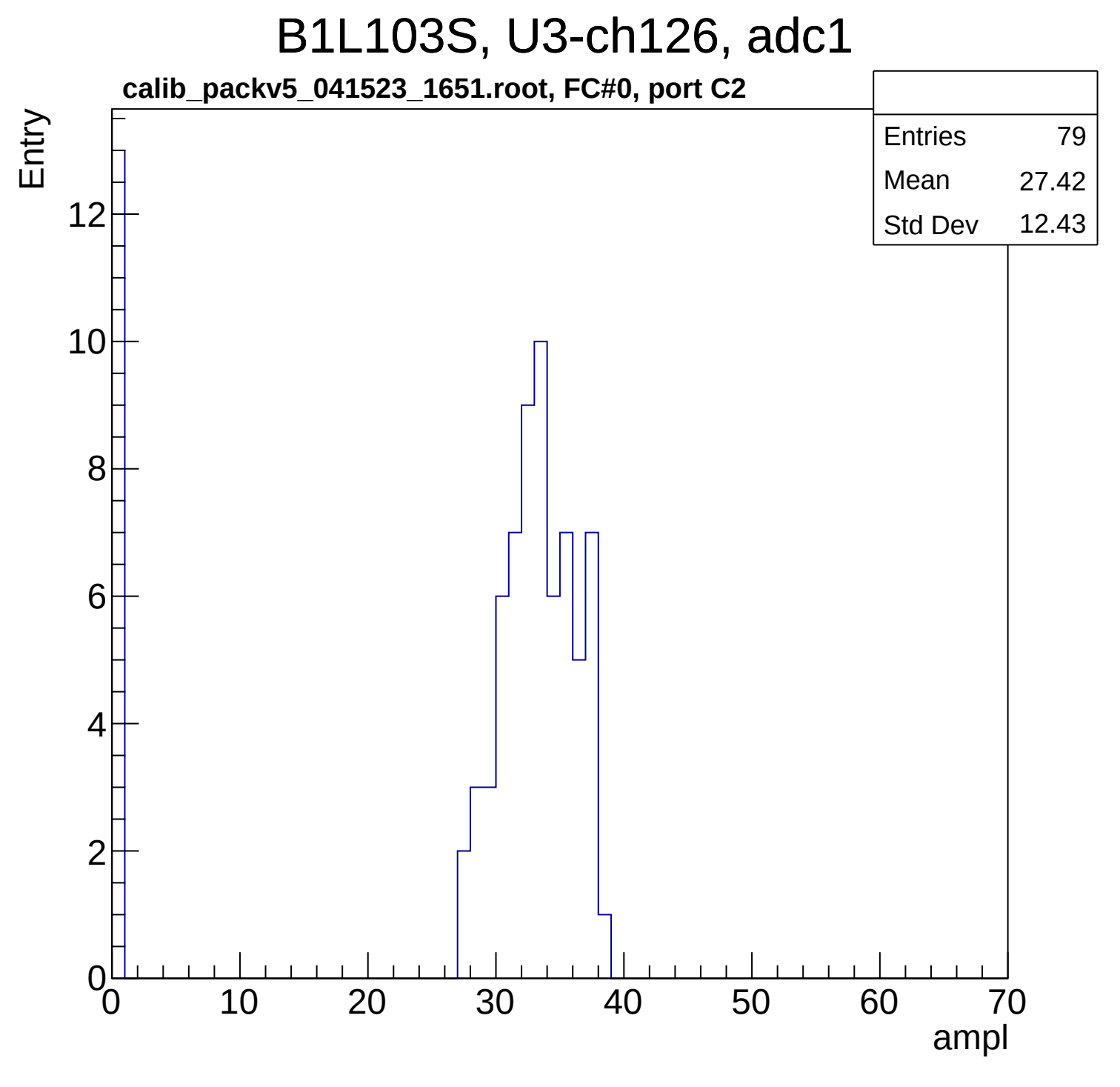
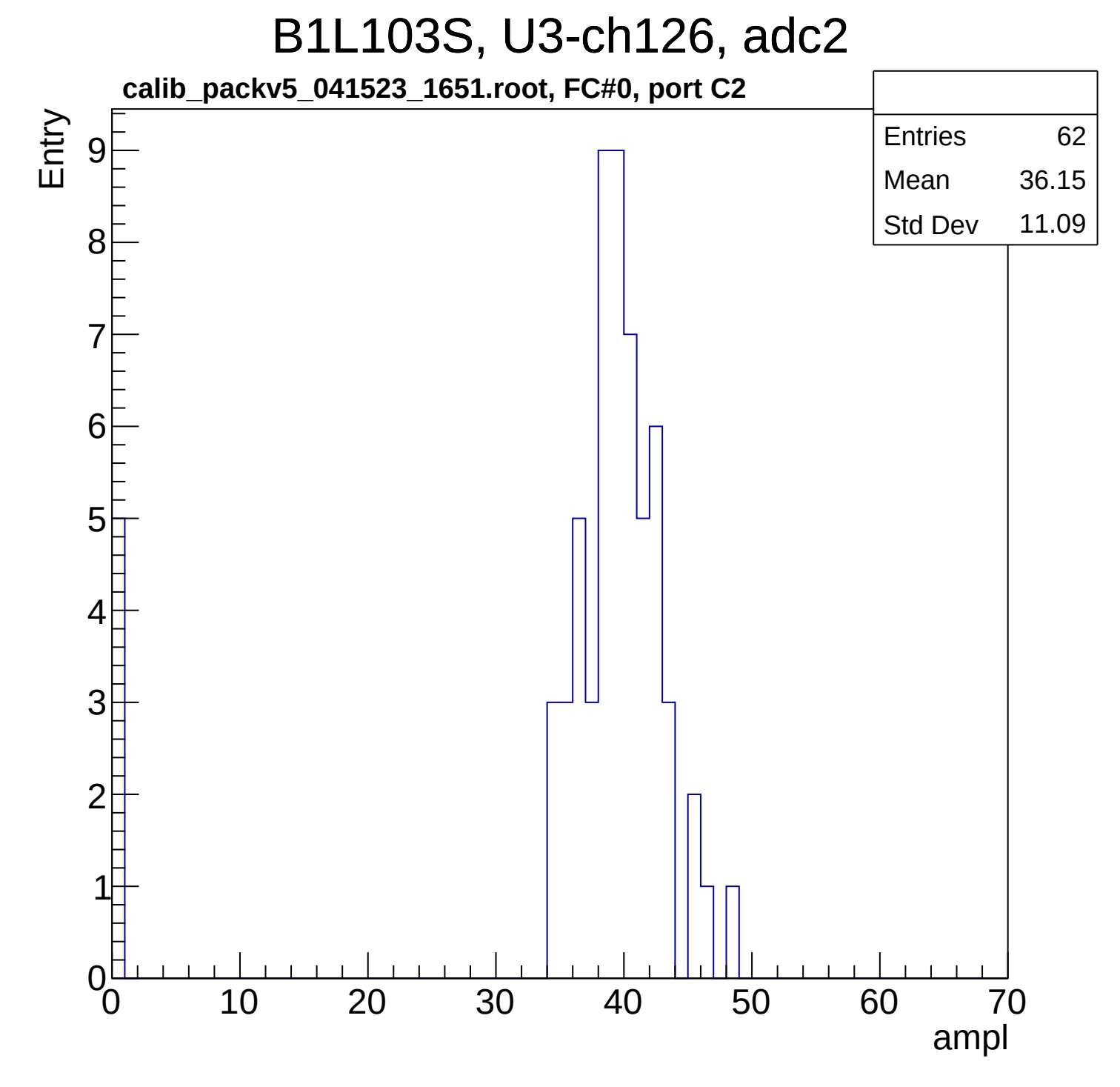
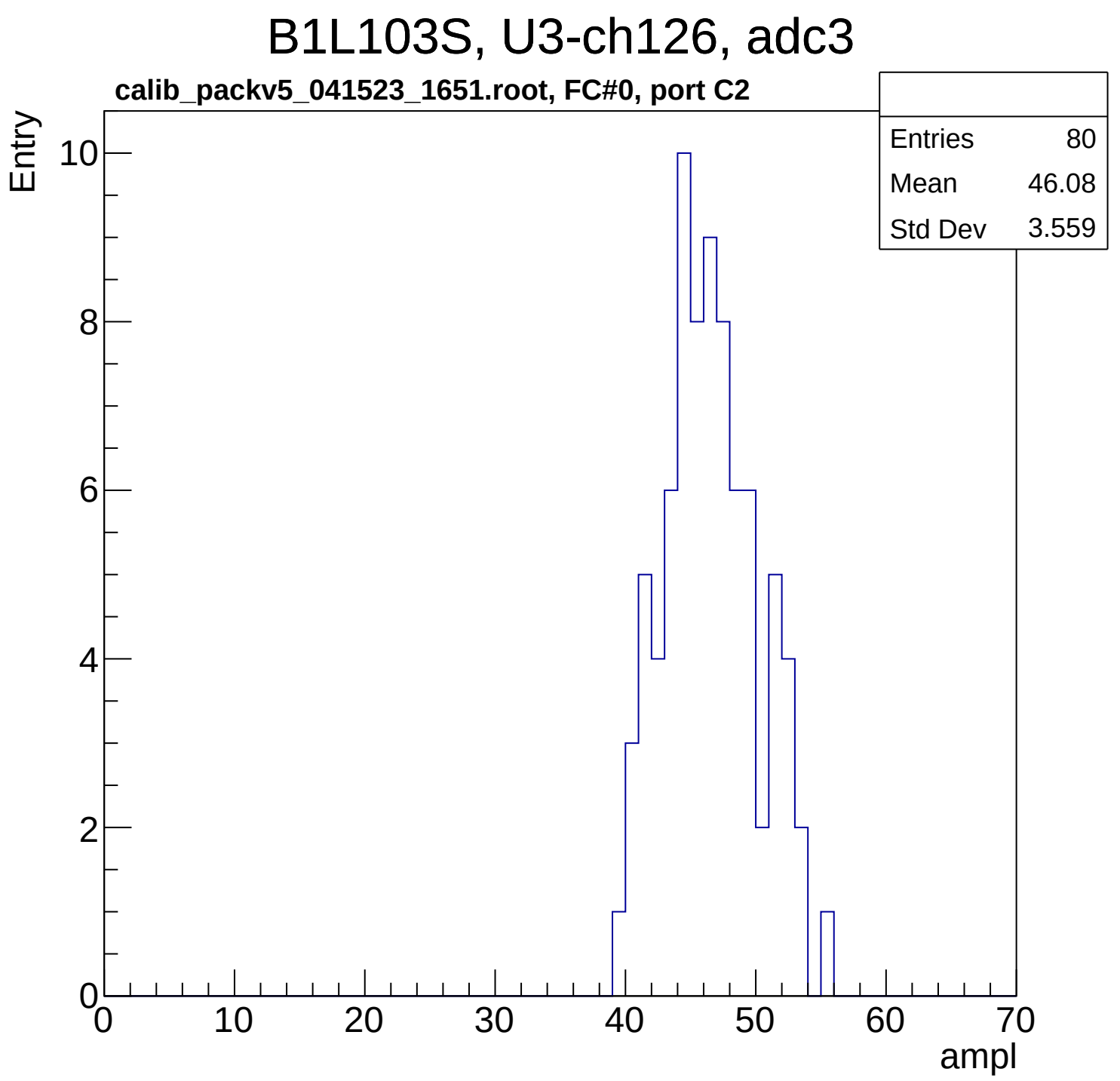
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

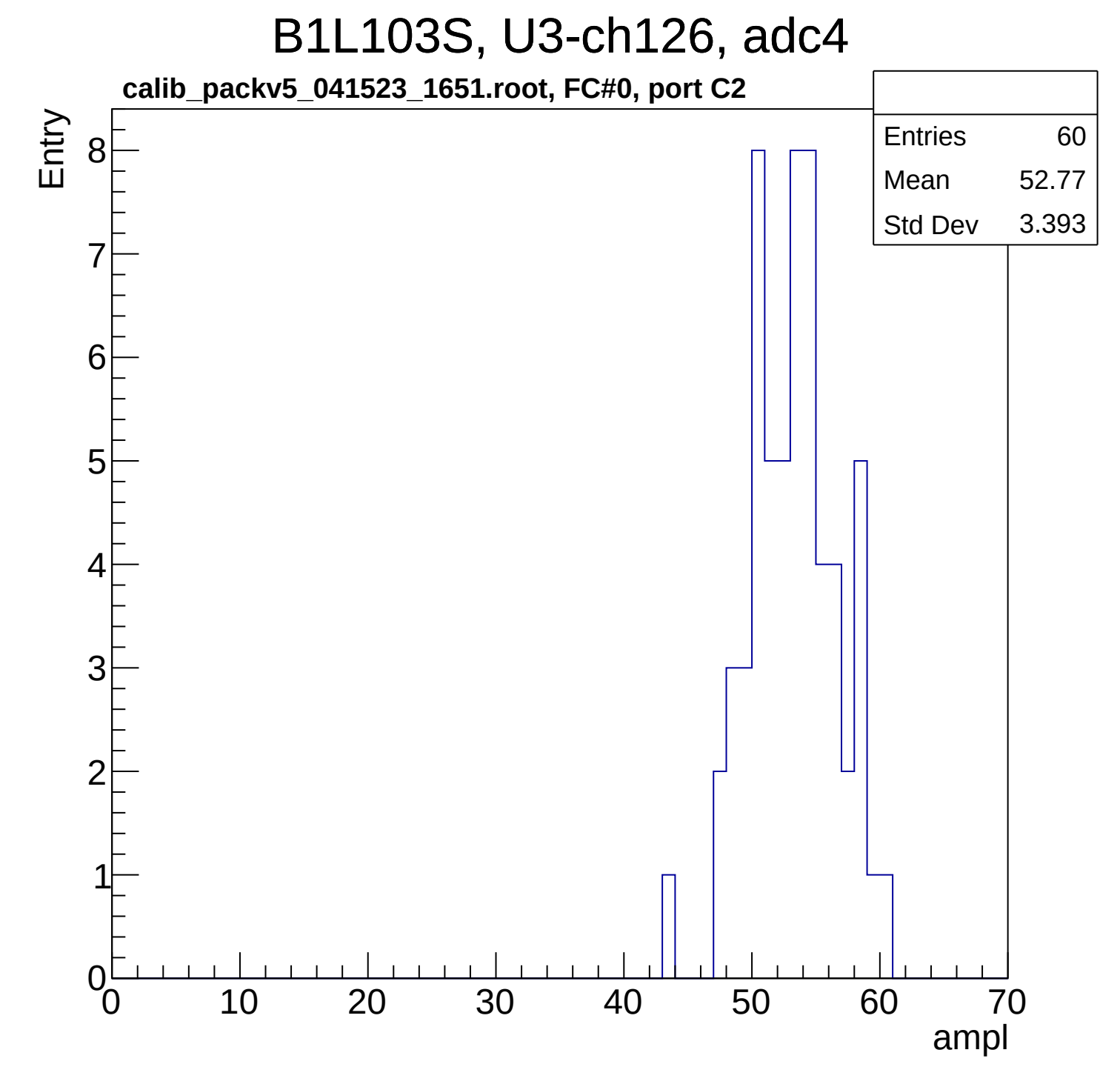

B1L103S, U3-ch125, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch126, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 100
Mean 19.76
Std Dev 10.94
Entry
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch126, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 27.42
Std Dev 12.43
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch126, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 36.15
Std Dev 11.09
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch126, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 46.08
Std Dev 3.559
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch126, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 52.77
Std Dev 3.393
Entry
ampl
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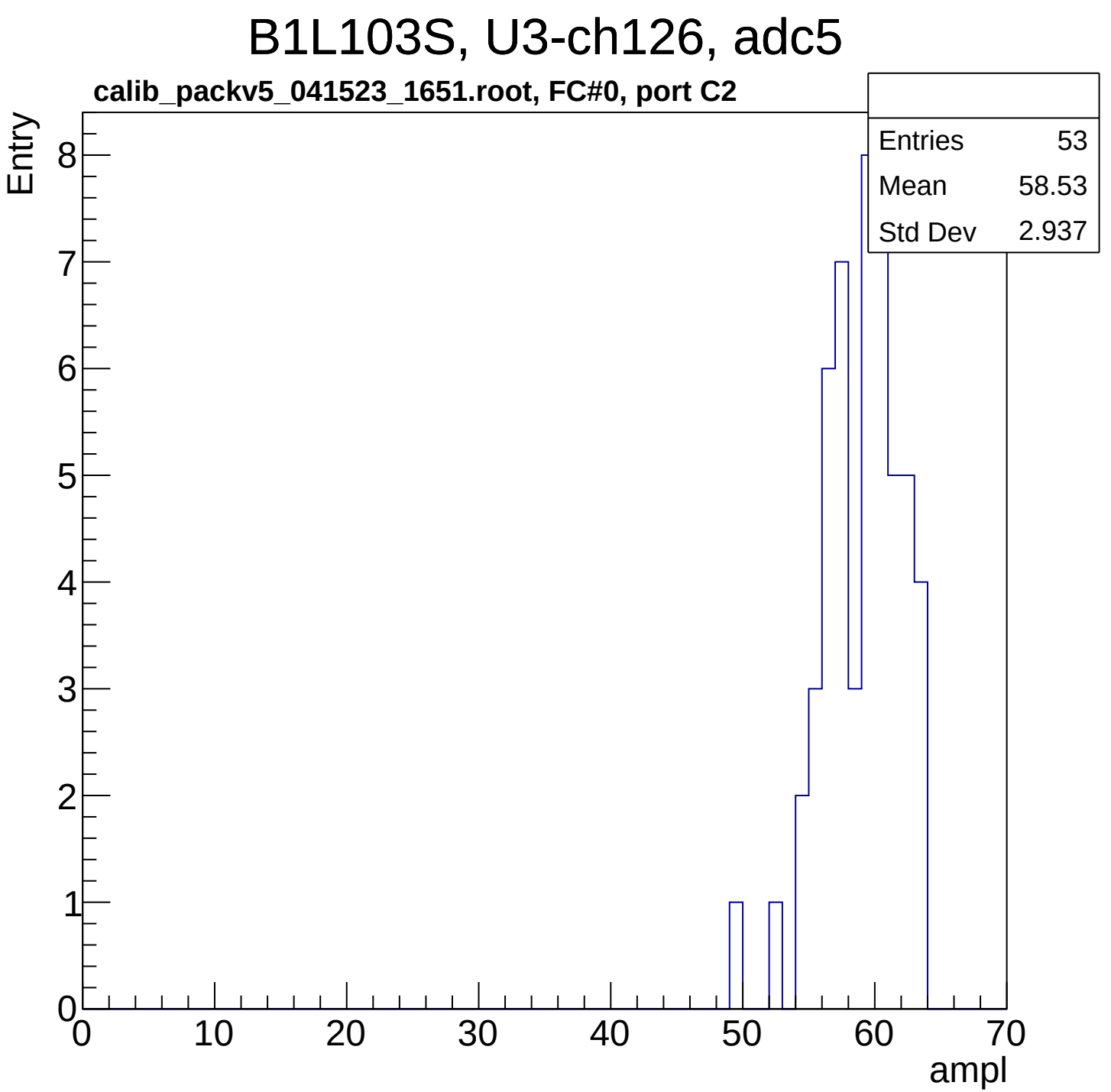
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch126, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 58.53
Std Dev 2.937
Entry
ampl
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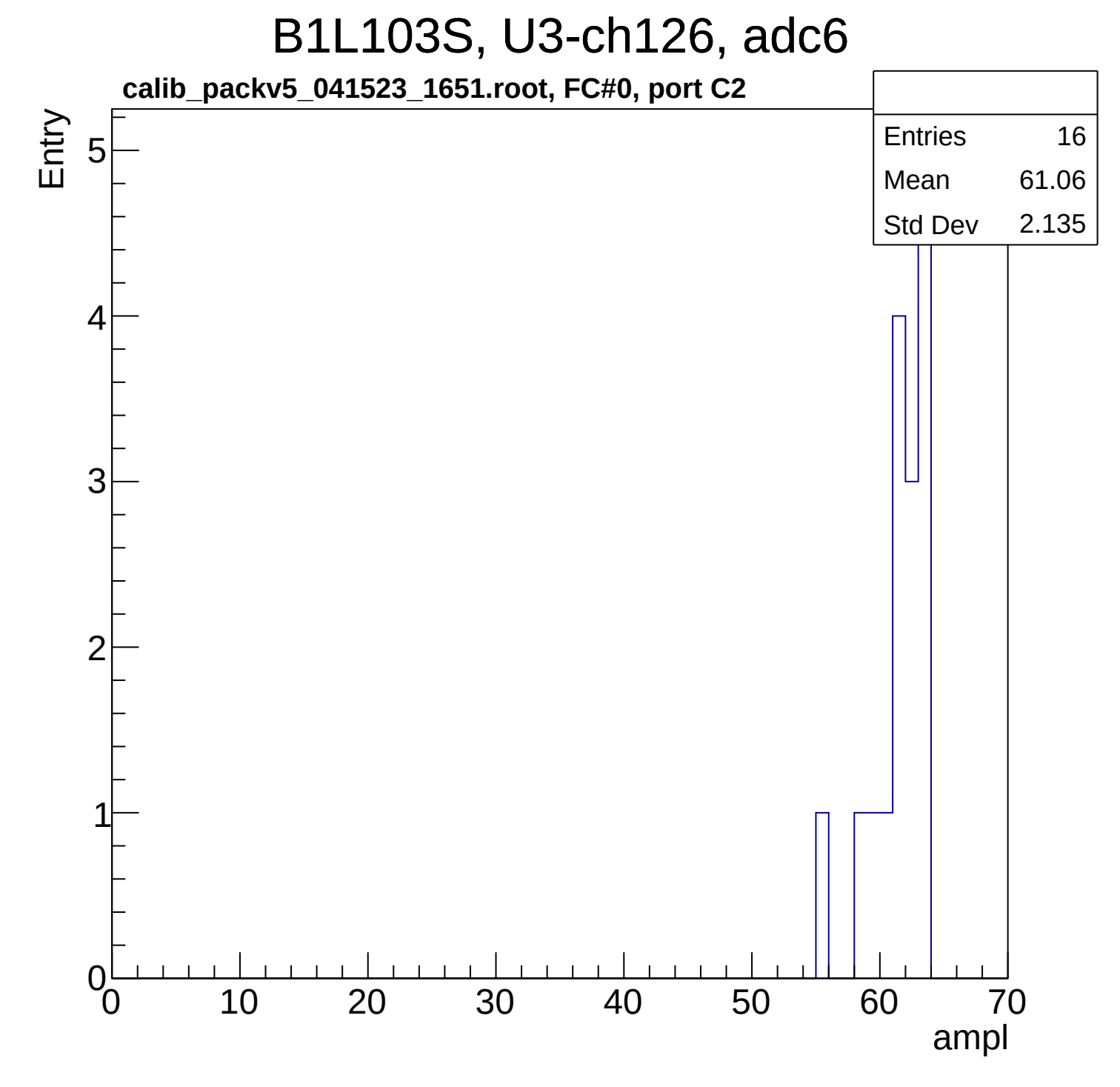
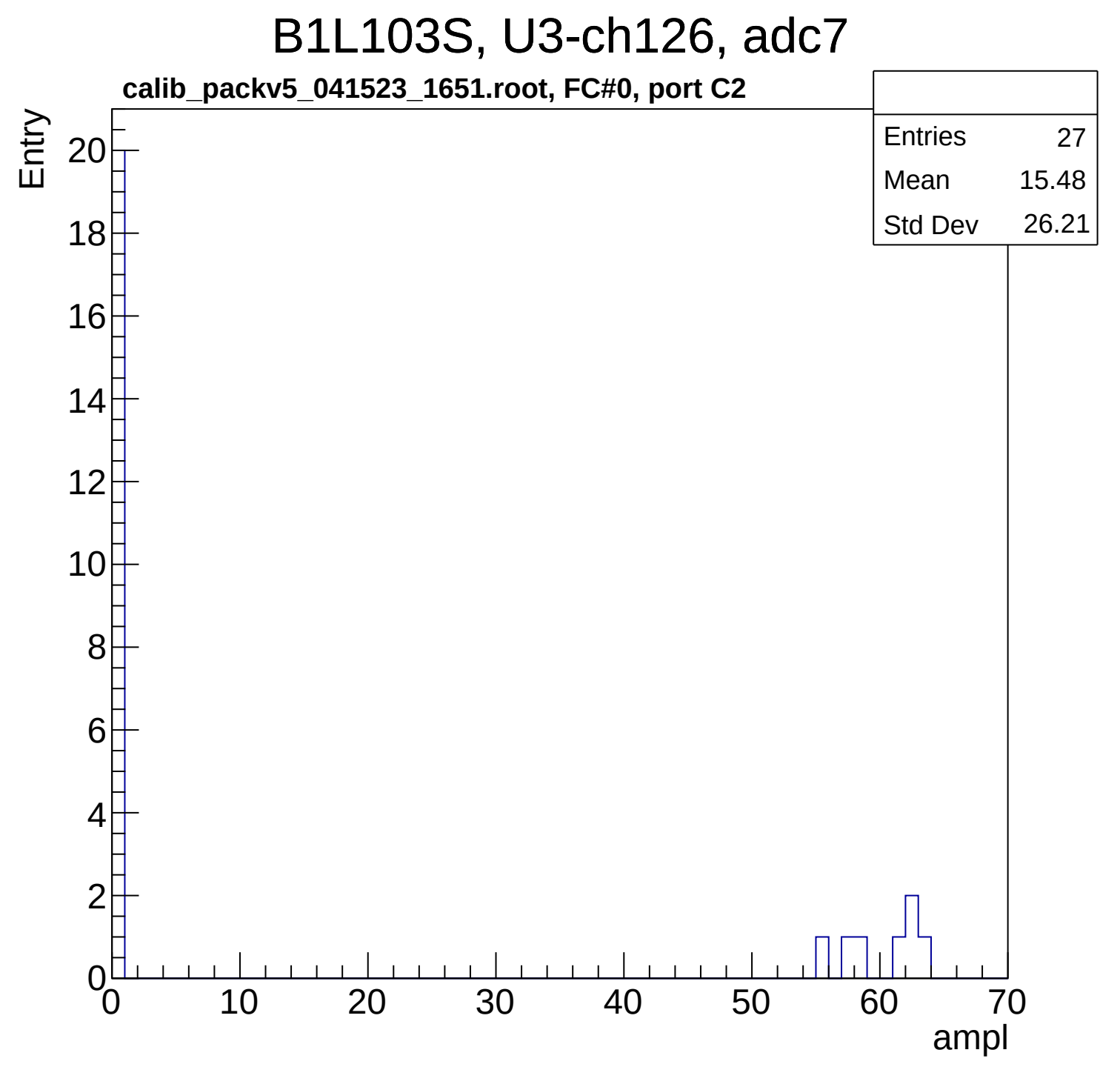
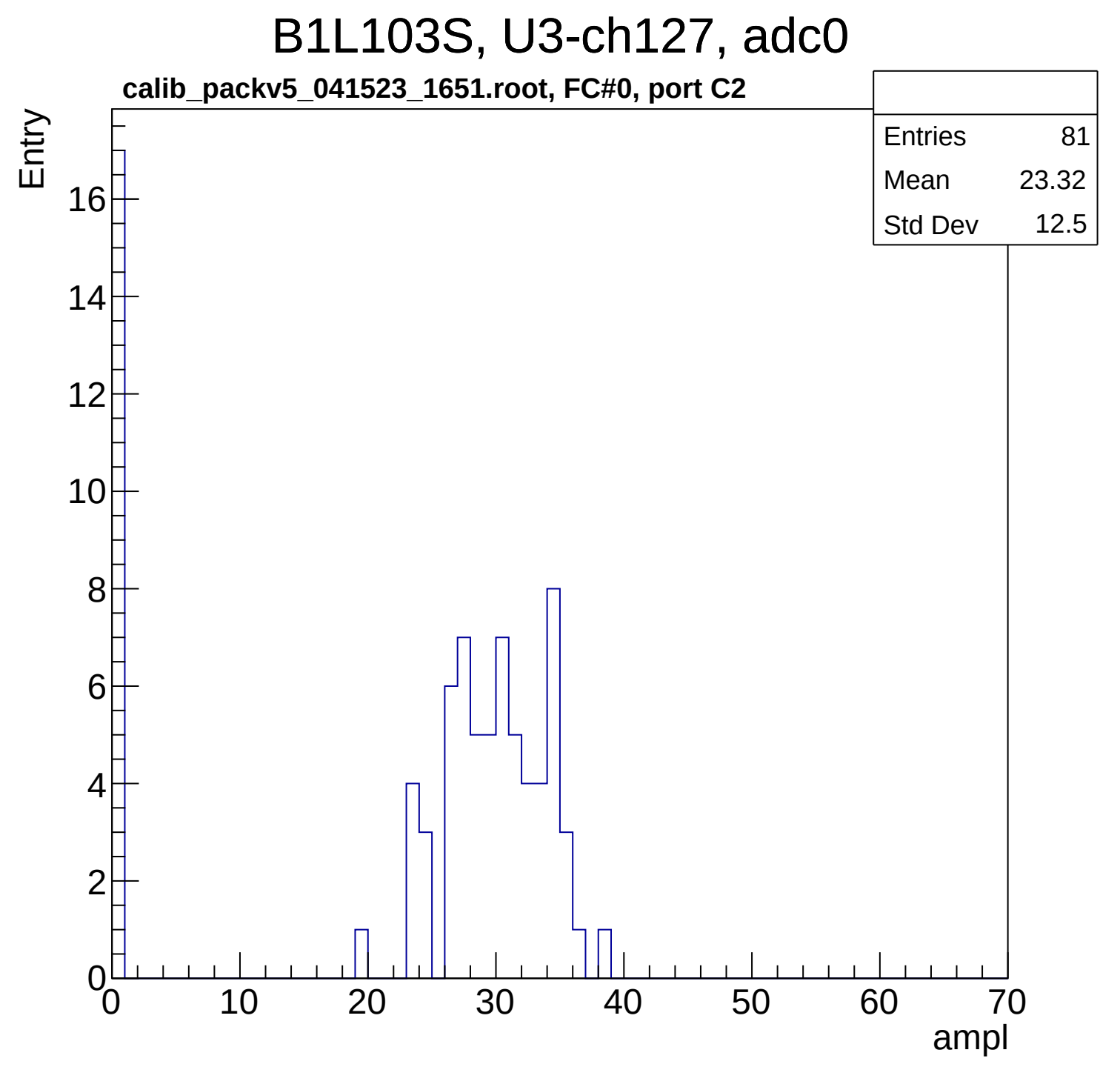
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch126, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 61.06
Std Dev 2.135
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U3-ch126, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 15.48
Std Dev 26.21
Entry
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch127, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 23.32
Std Dev 12.5
Entry
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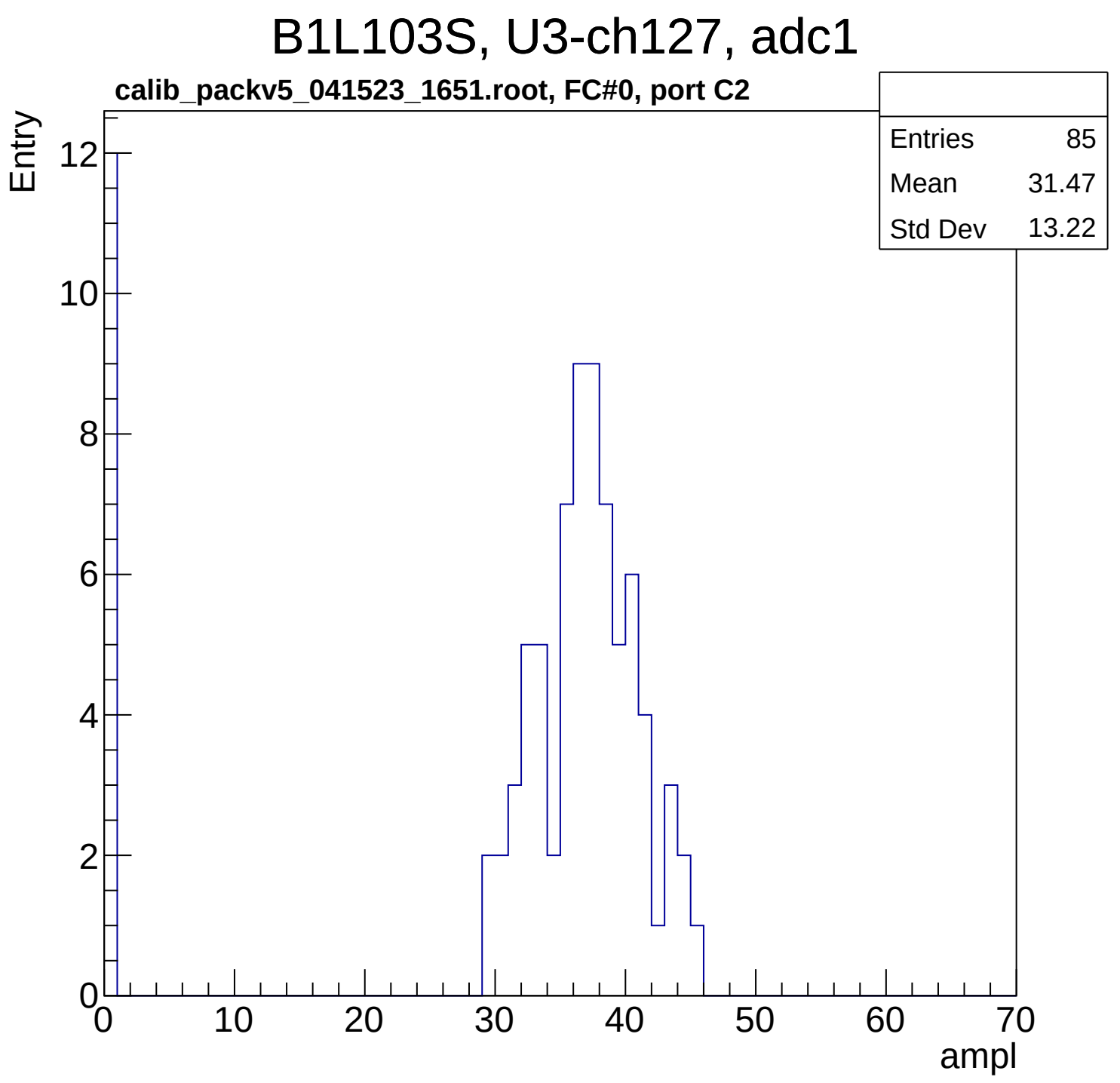
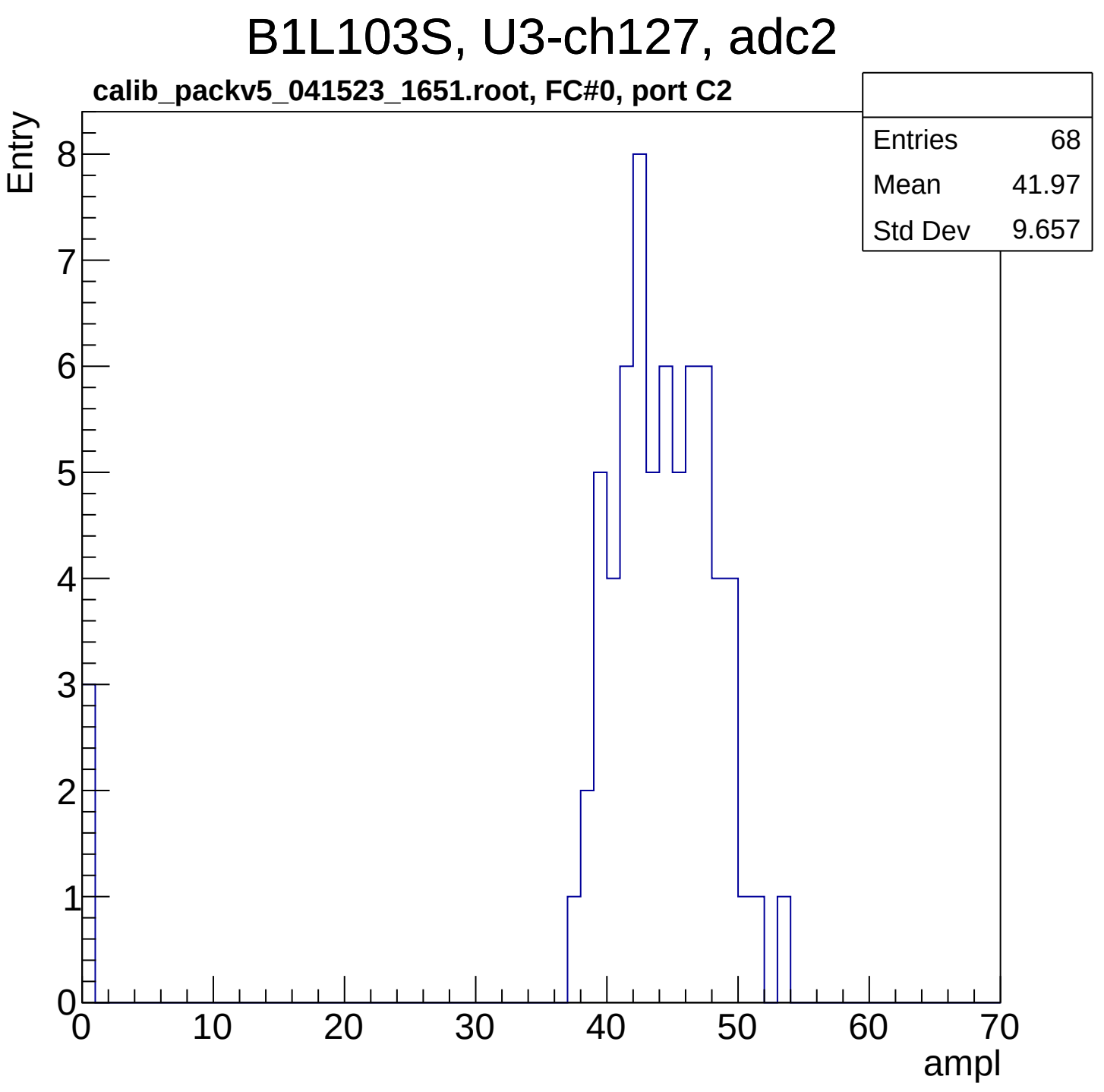
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch127, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 31.47
Std Dev 13.22
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U3-ch127, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 41.97
Std Dev 9.657
Entry
ampl
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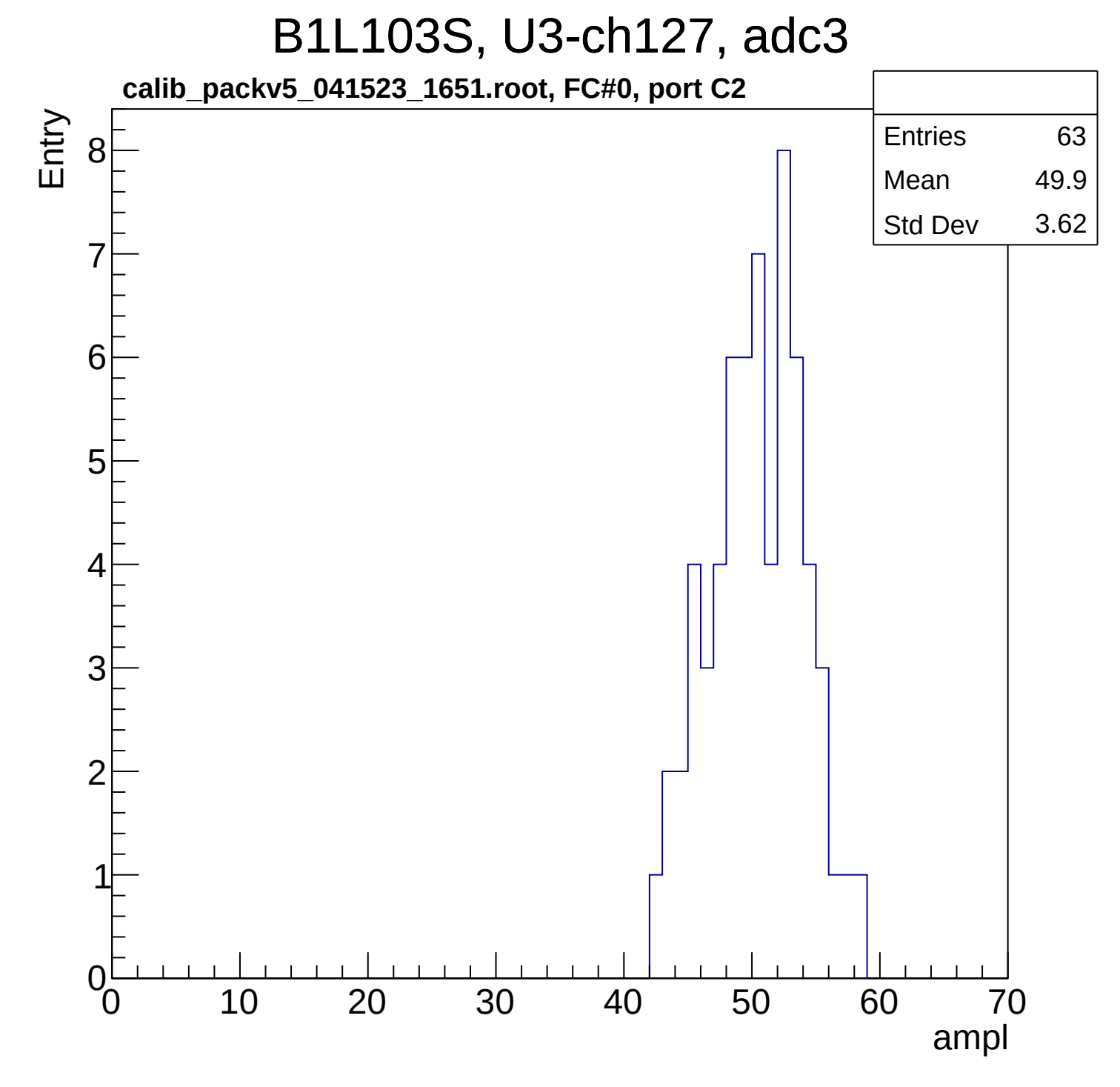
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch127, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 49.9
Std Dev 3.62
Entry
ampl
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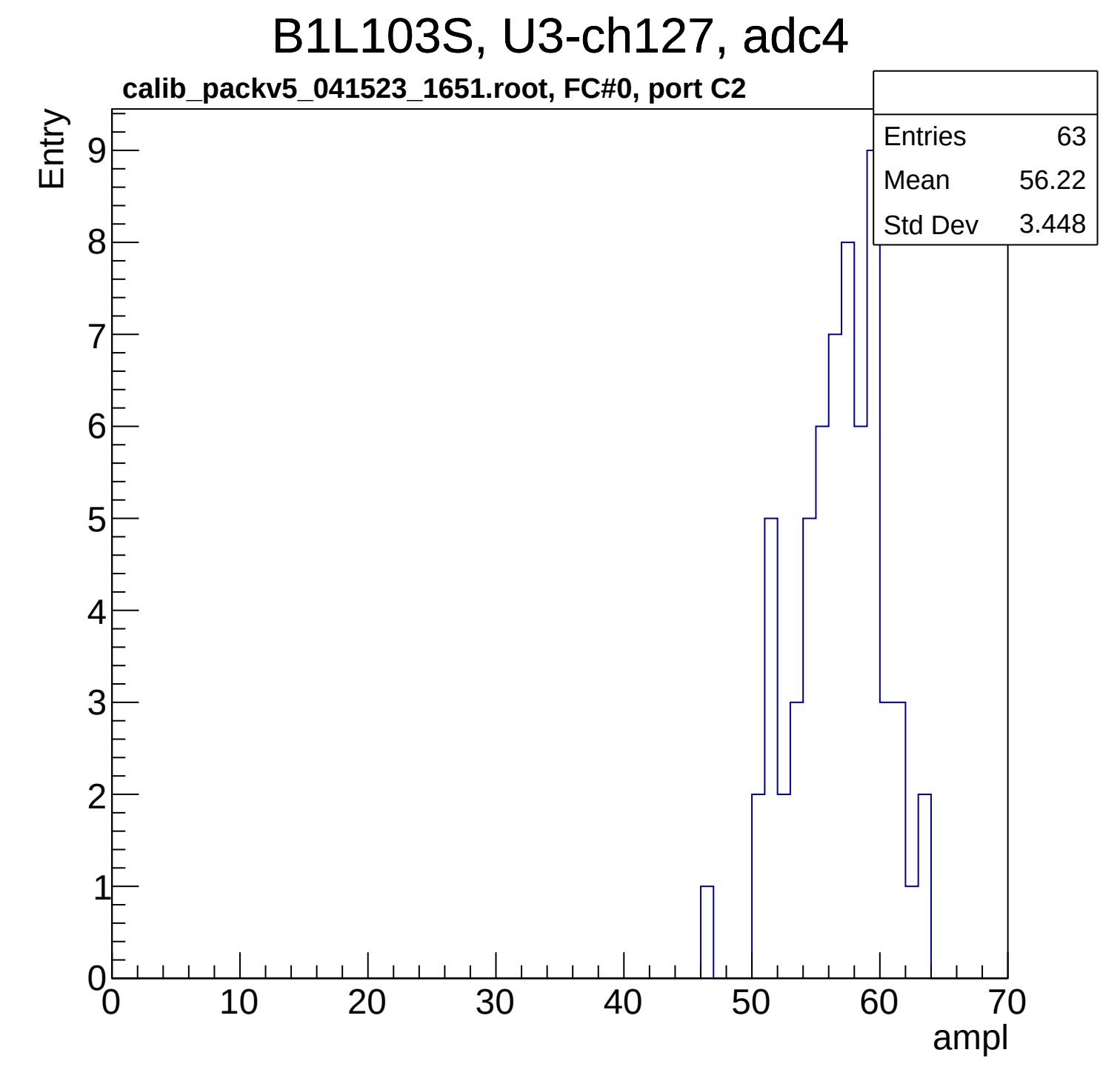
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch127, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 56.22
Std Dev 3.448
Entry
ampl
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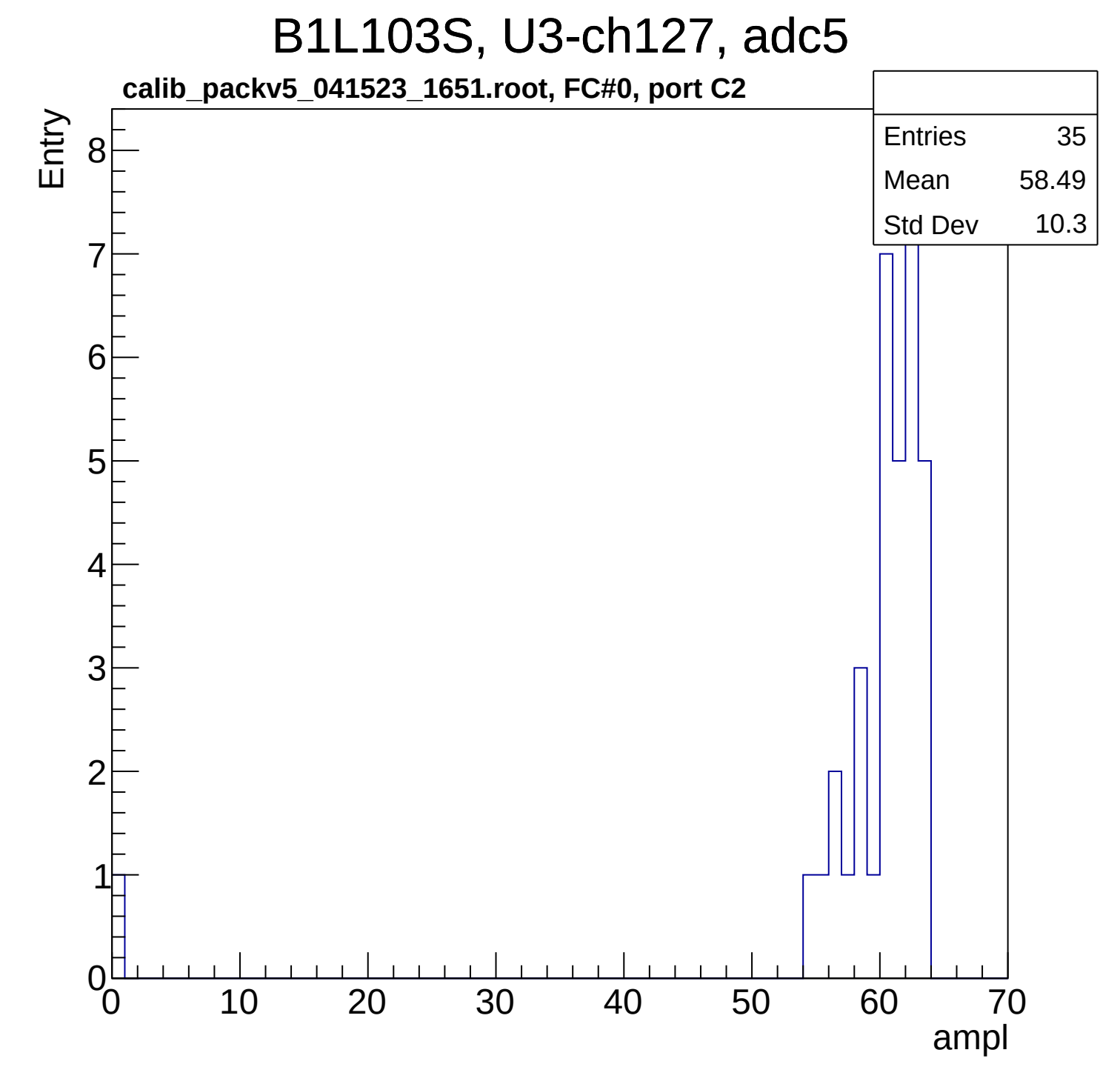
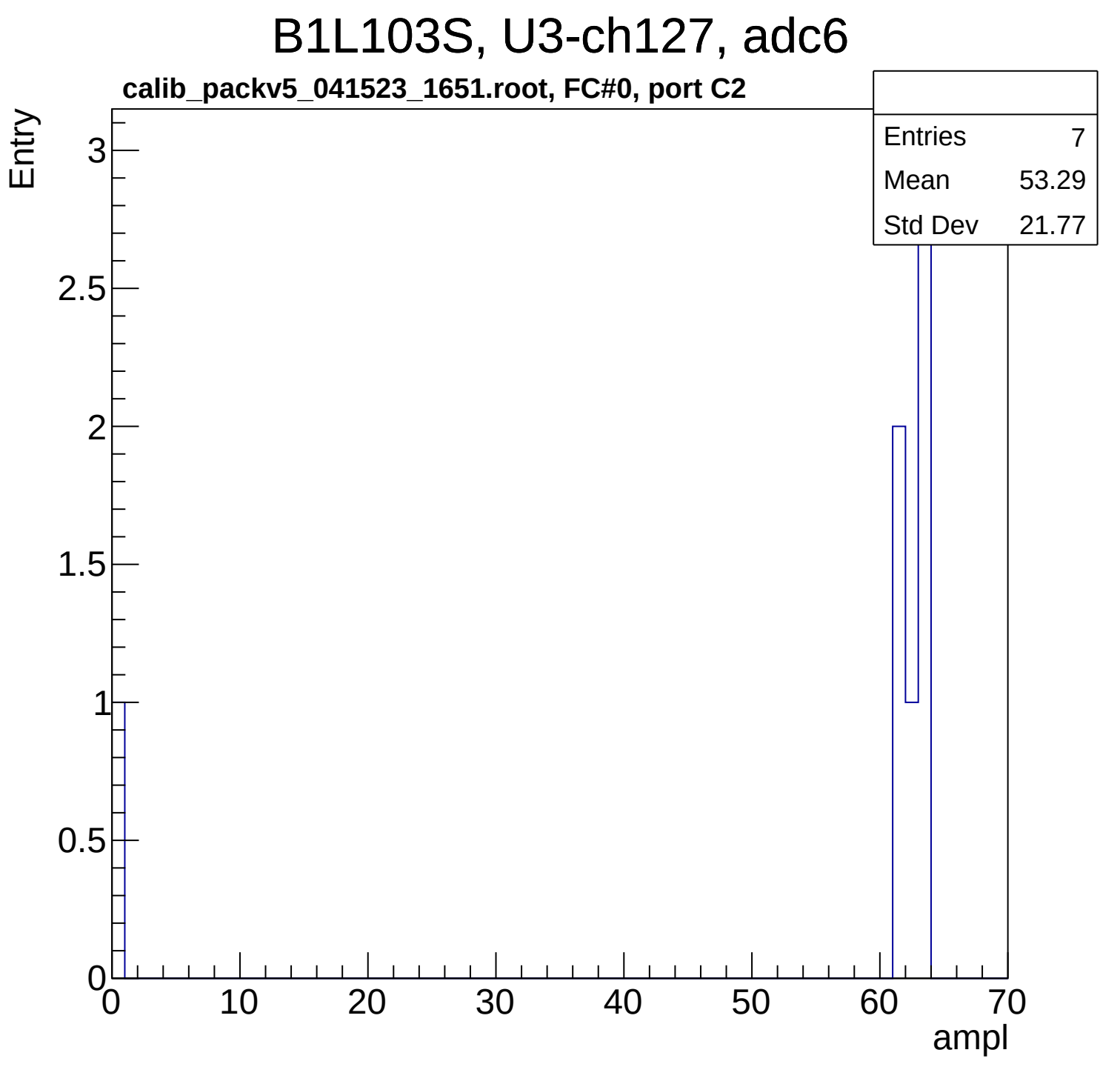
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U3-ch127, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 58.49
Std Dev 10.3
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U3-ch127, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 53.29
Std Dev 21.77
Entry
ampl
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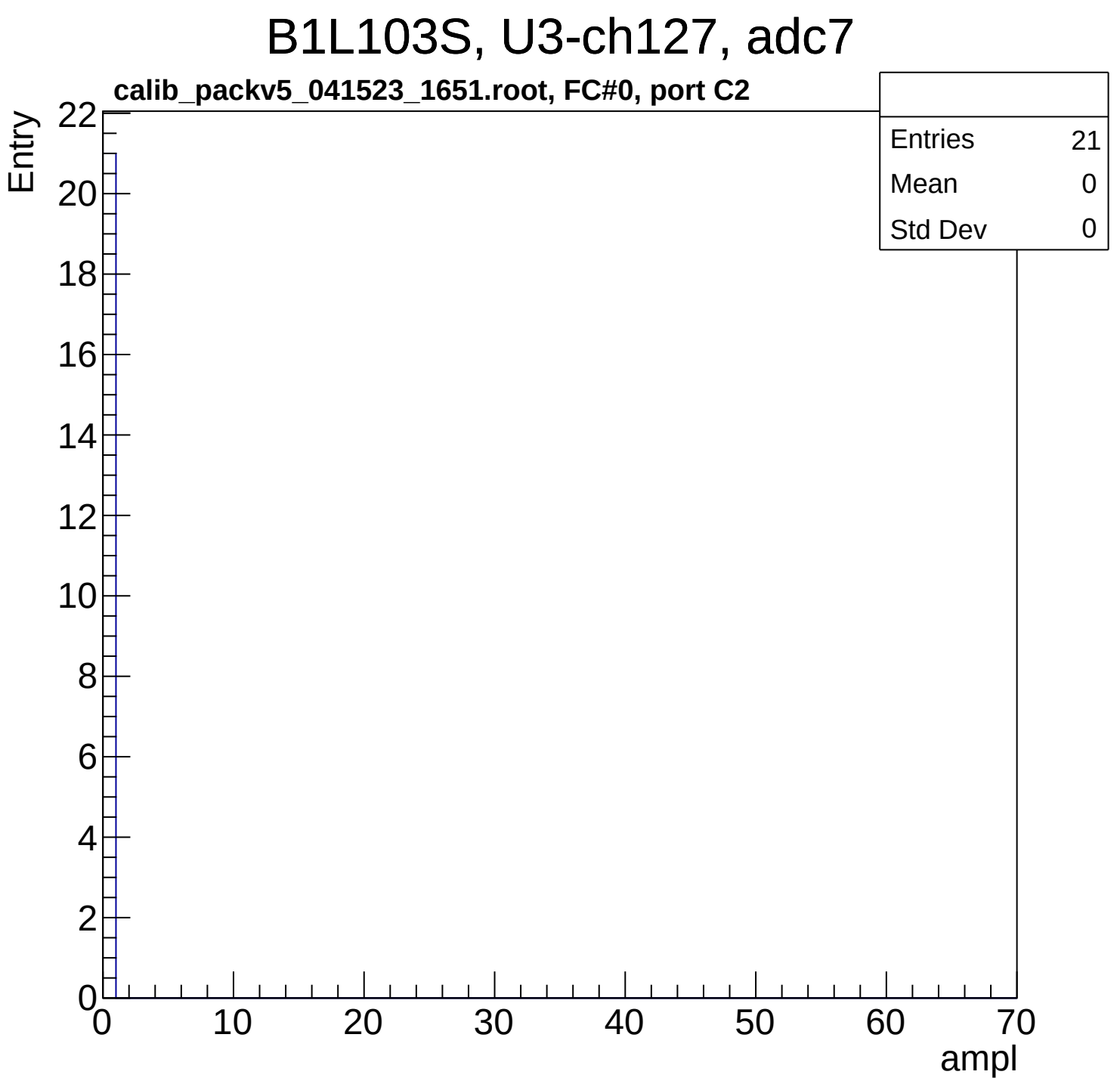
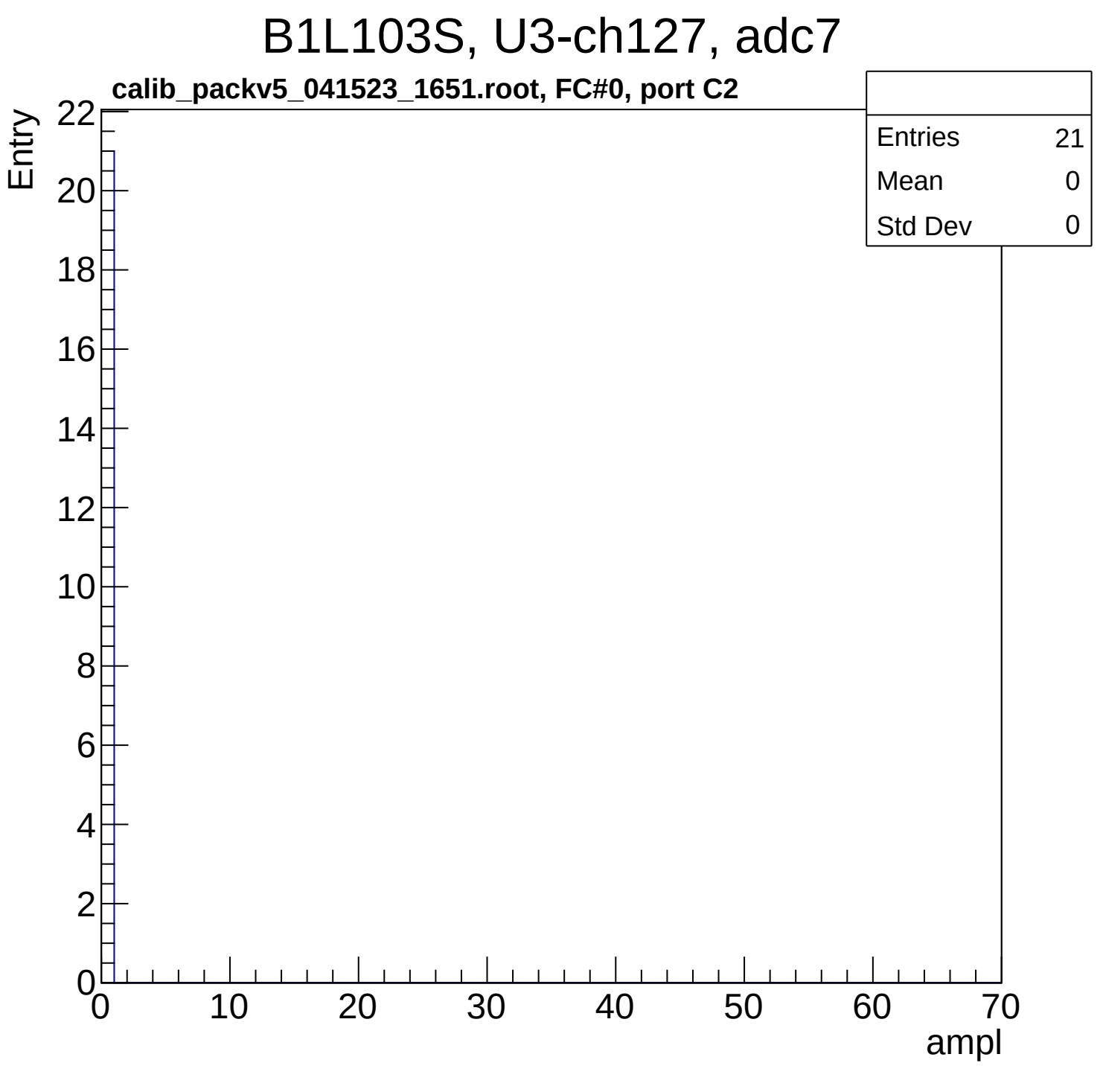
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U3-ch127, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 0
Std Dev 0
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70


B1L103S, U3-ch127, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 0
Std Dev 0
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70