



# B1L003S, U6-ch0, adc0

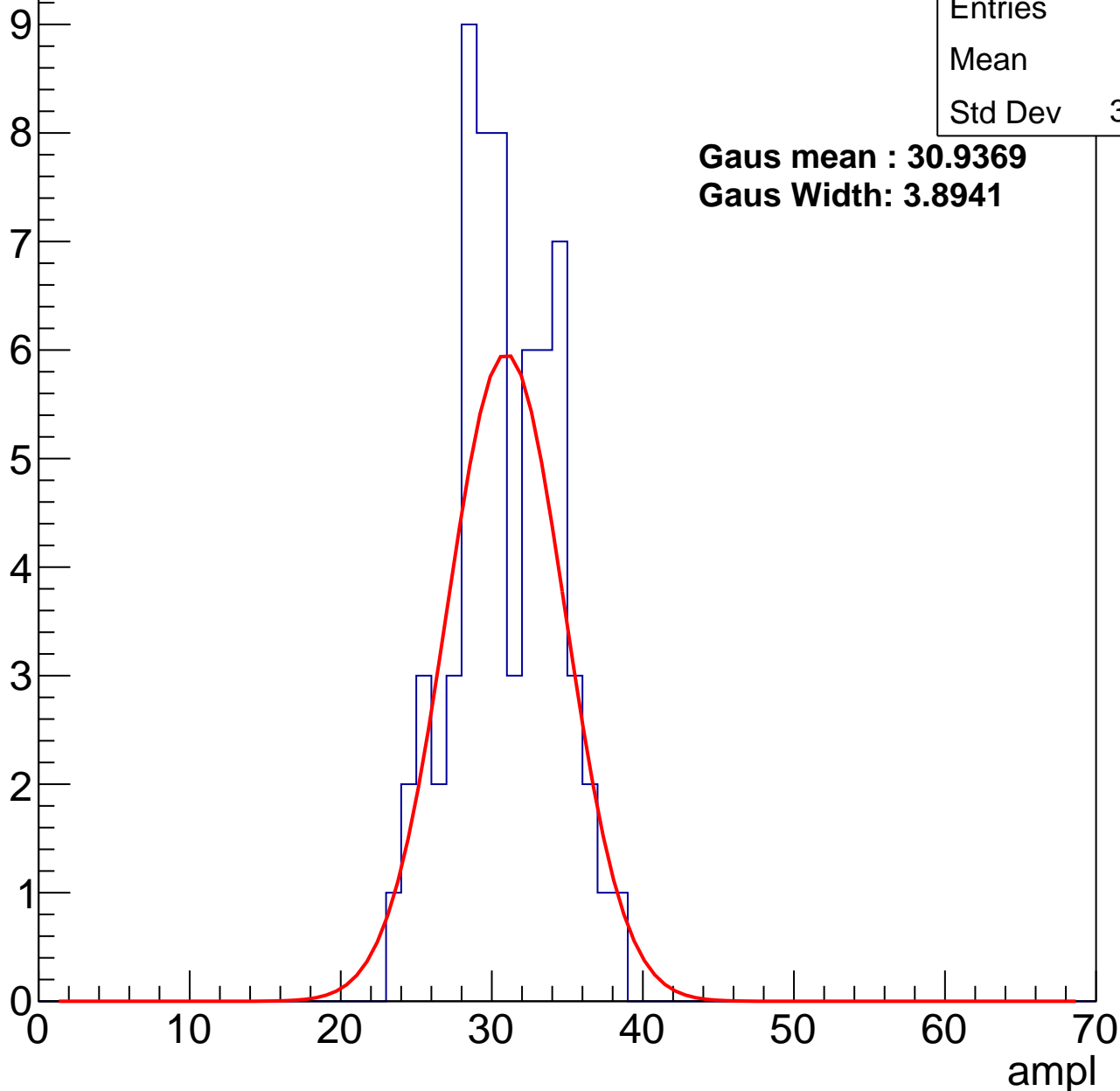
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	30.4
Std Dev	3.378

**Gaus mean : 30.9369**

**Gaus Width: 3.8941**



# B1L003S, U6-ch0, adc1

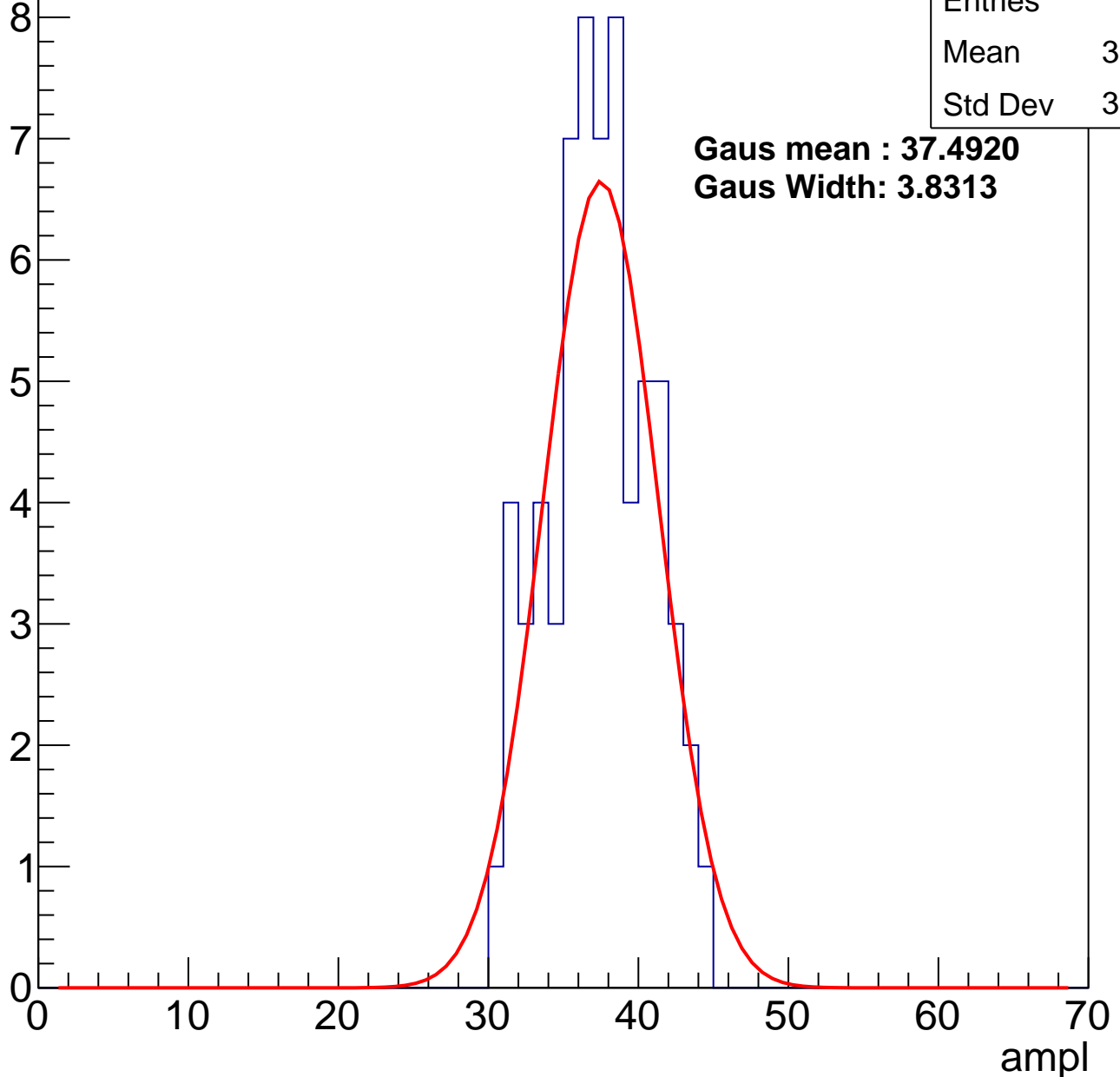
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	36.88
Std Dev	3.372

**Gaus mean : 37.4920**

**Gaus Width: 3.8313**



# B1L003S, U6-ch0, adc2

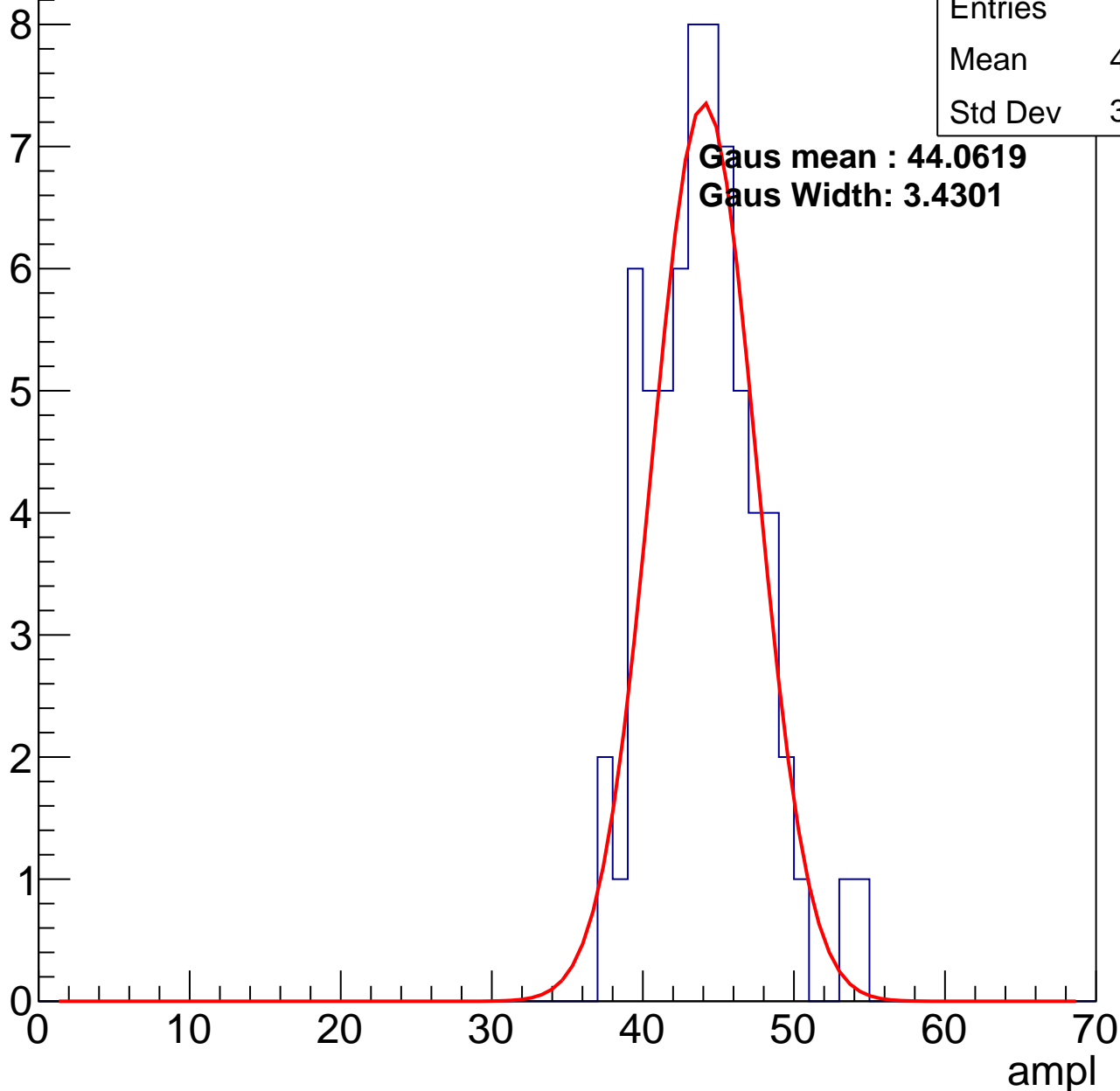
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	43.62
Std Dev	3.537

**Gaus mean : 44.0619**

**Gaus Width: 3.4301**

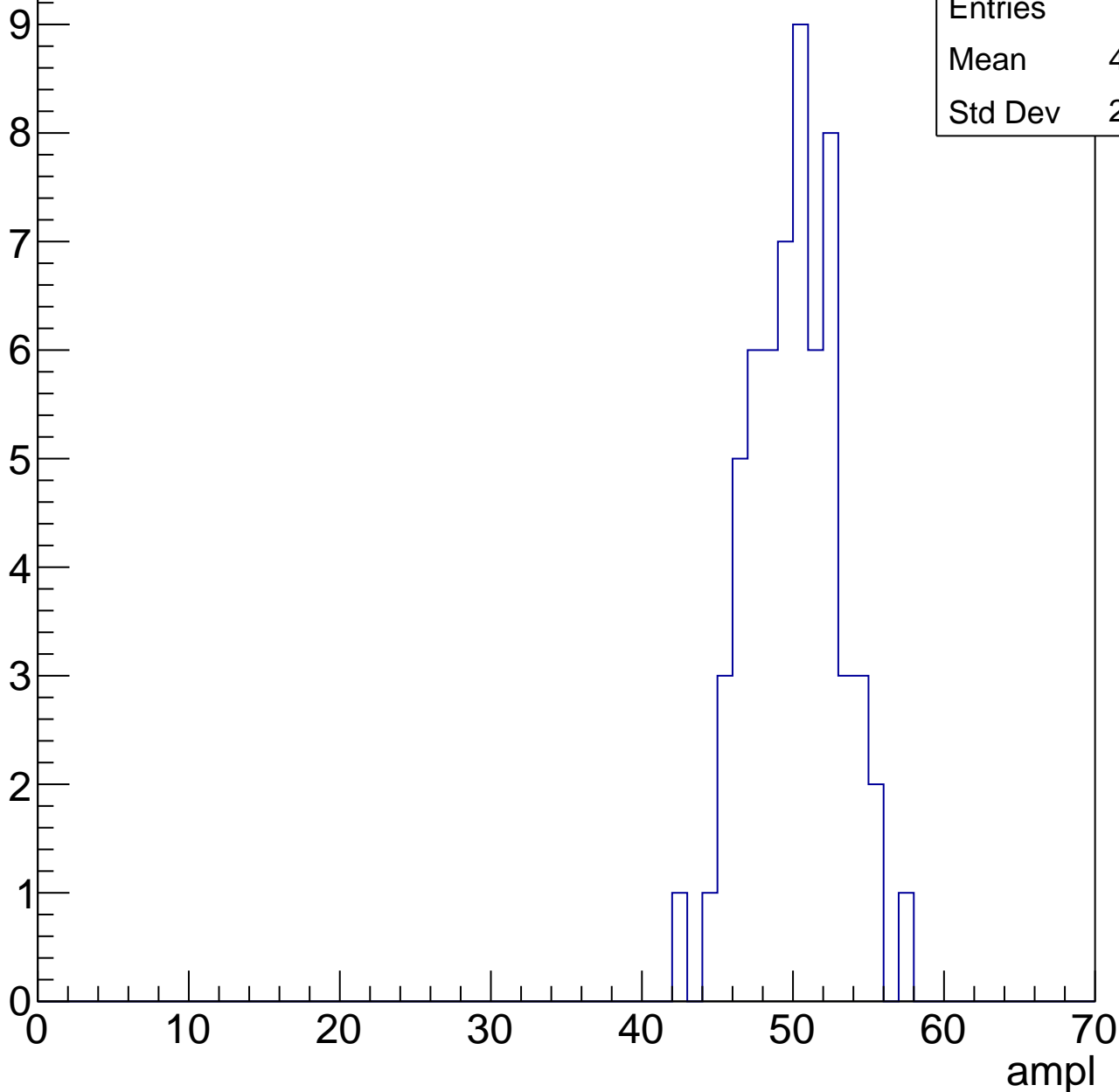


# B1L003S, U6-ch0, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	49.57
Std Dev	2.978



# B1L003S, U6-ch0, adc4

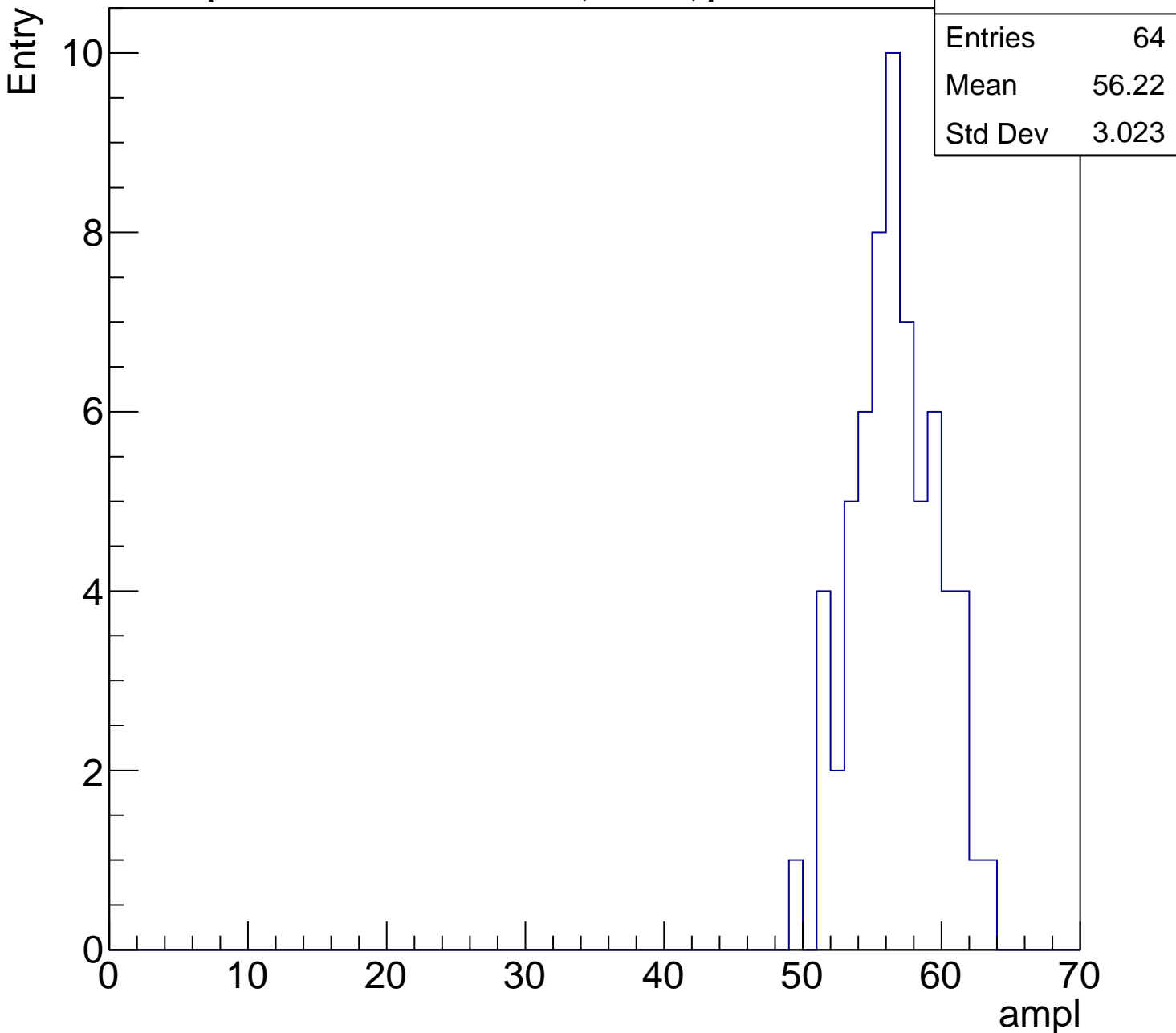
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	64
Mean	56.22
Std Dev	3.023

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70  
ampl

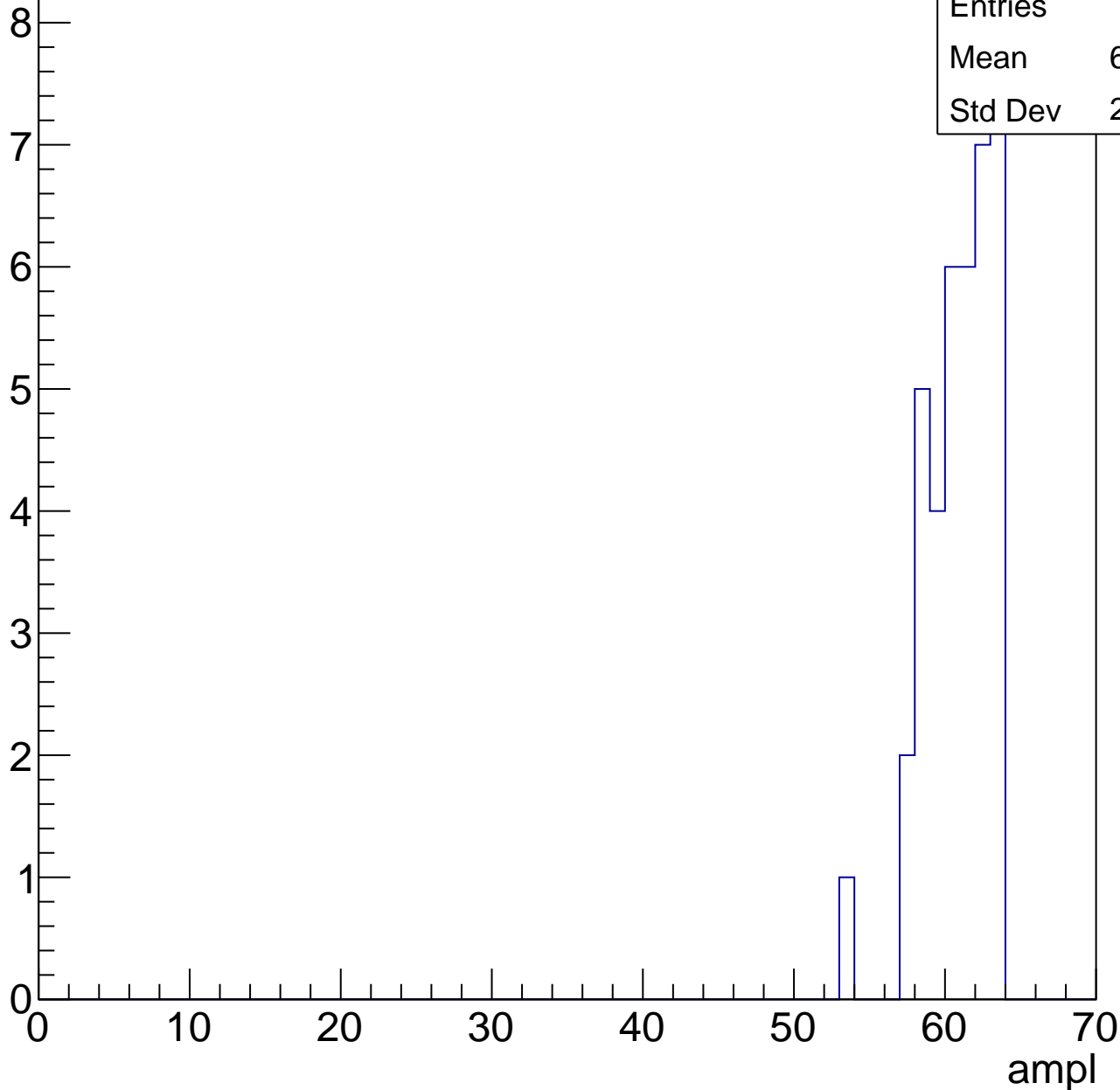


# B1L003S, U6-ch0, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	39
Mean	60.44
Std Dev	2.205



# B1L003S, U6-ch0, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

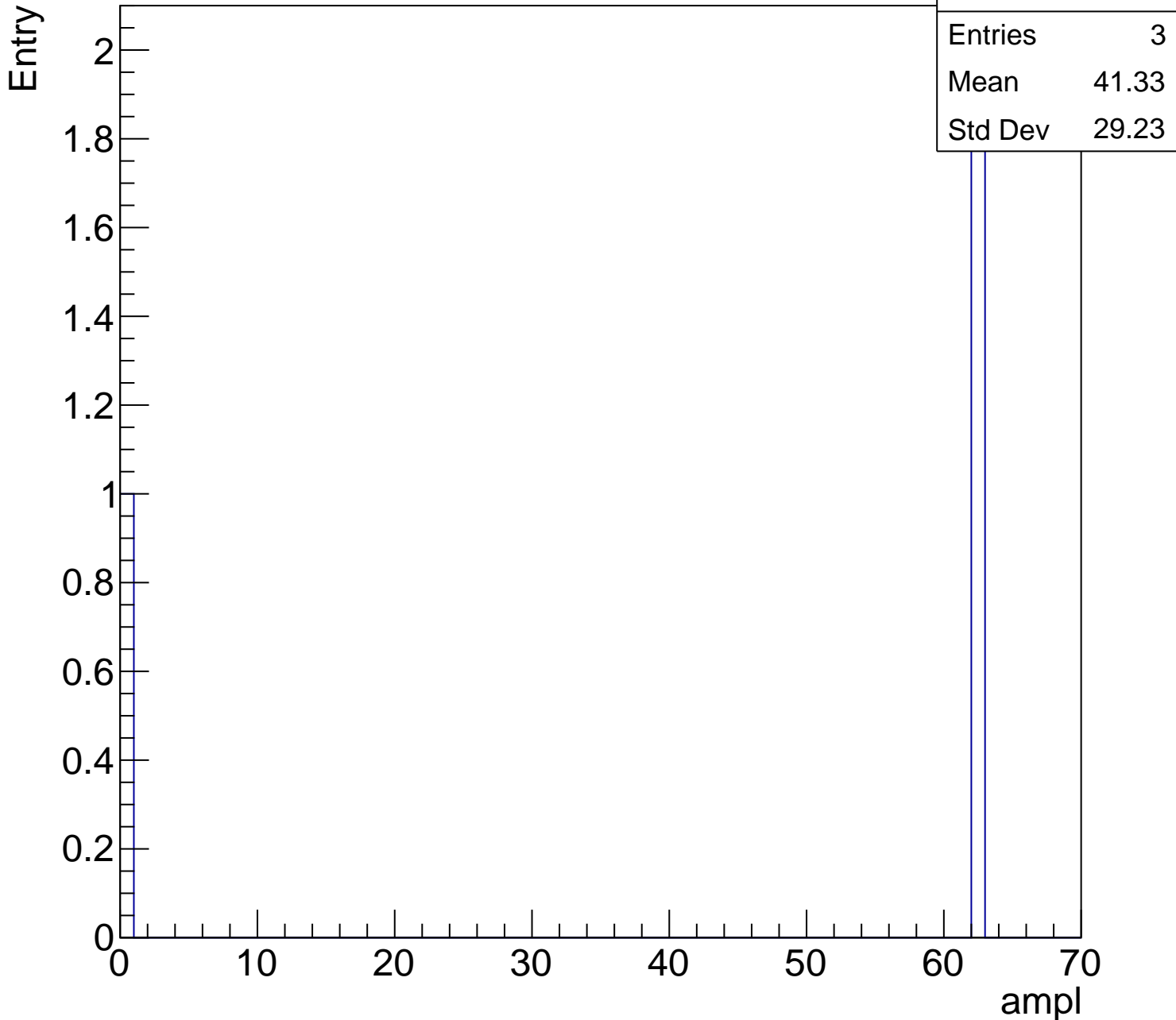
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	41.33
Std Dev	29.23

0 10 20 30 40 50 60 70

ampl

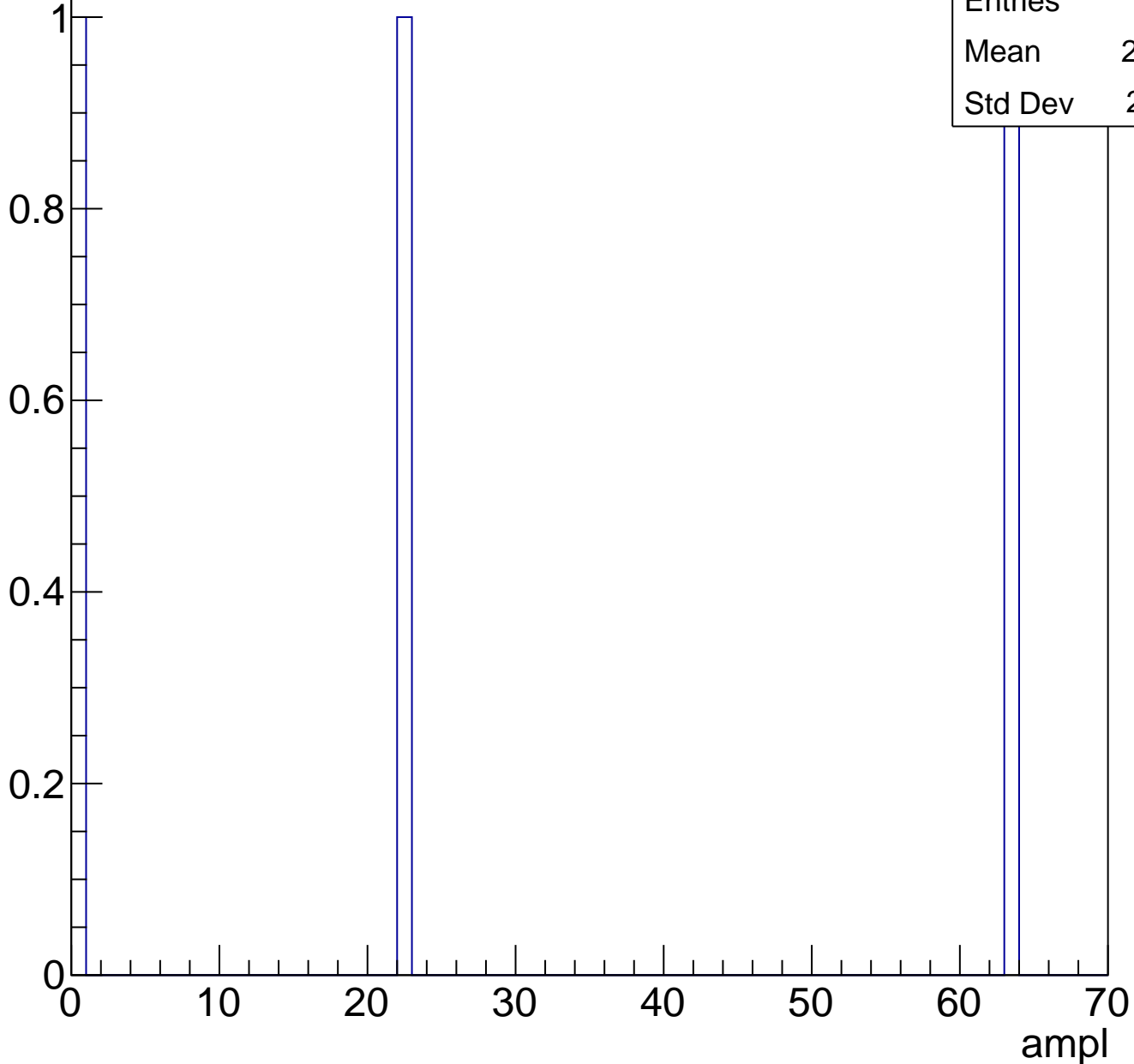




# B1L003S, U6-ch0, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	3
Mean	28.33
Std Dev	26.11

# B1L003S, U6-ch1, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	67
Mean	30.55
Std Dev	4.972

**Gaus mean : 31.0267**

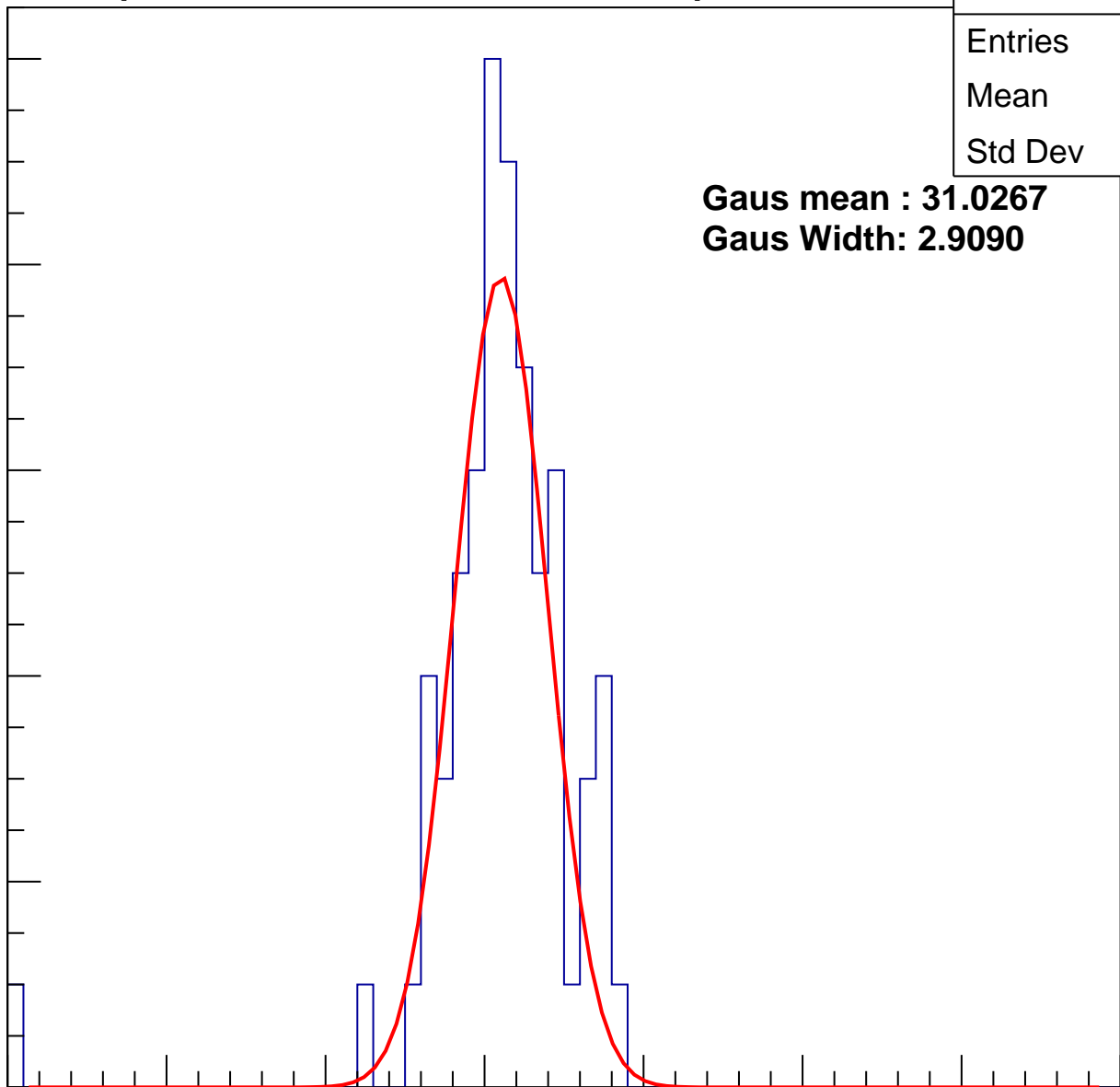
**Gaus Width: 2.9090**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U6-ch1, adc1

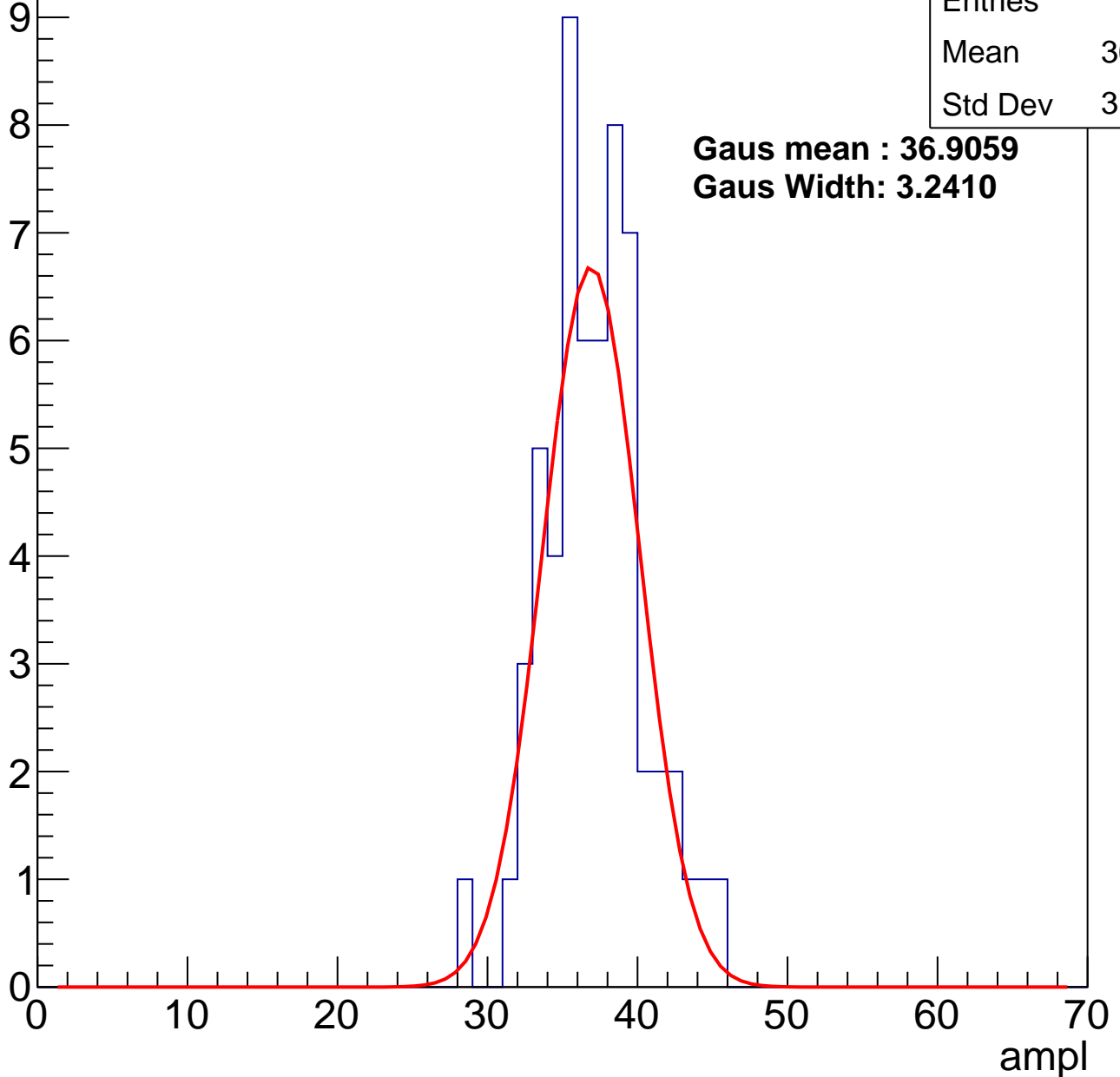
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	36.68
Std Dev	3.265

**Gaus mean : 36.9059**

**Gaus Width: 3.2410**



# B1L003S, U6-ch1, adc2

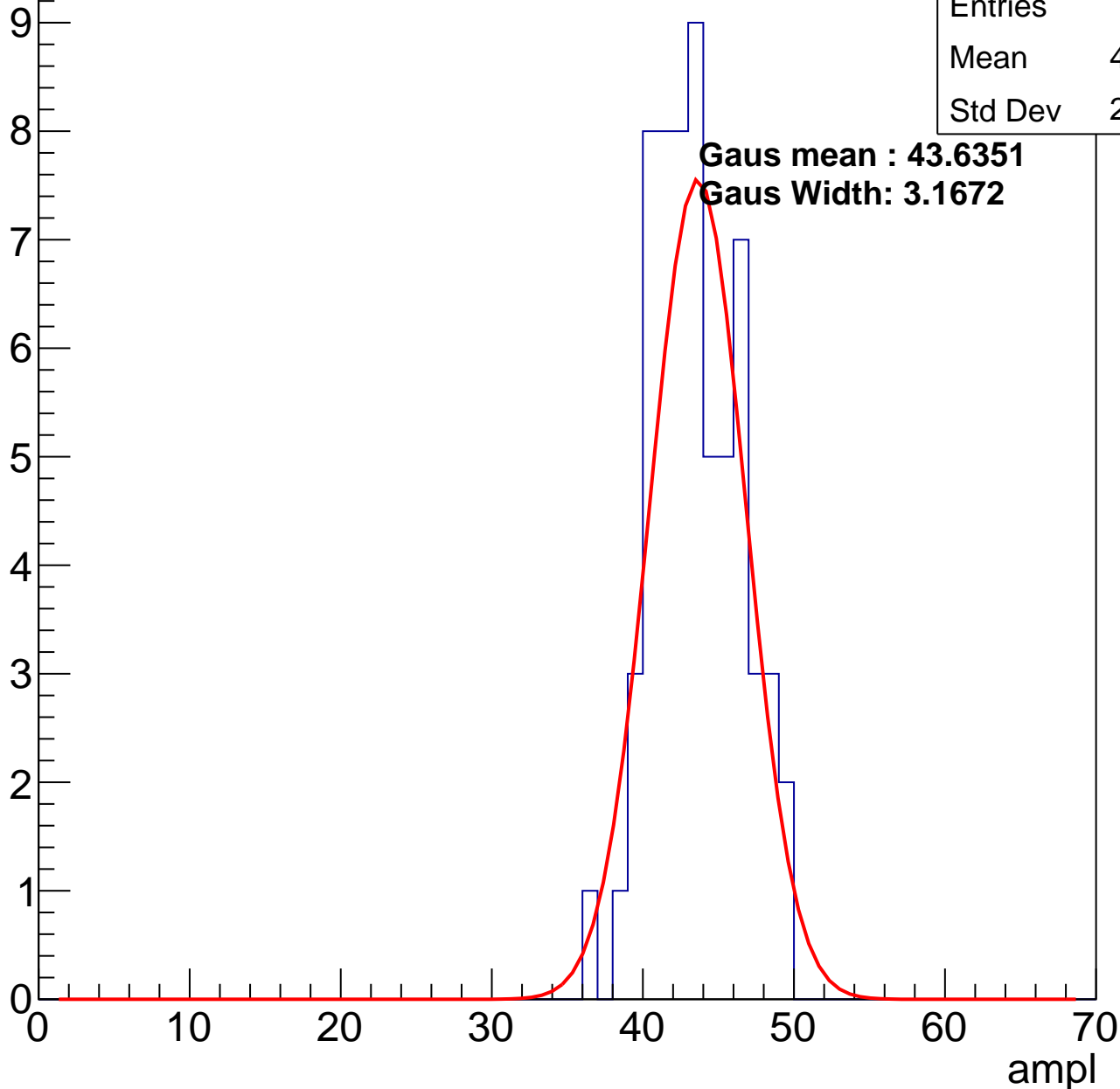
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	43.05
Std Dev	2.864

**Gaus mean : 43.6351**

**Gaus Width: 3.1672**



# B1L003S, U6-ch1, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	66
Mean	49.45
Std Dev	2.965

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

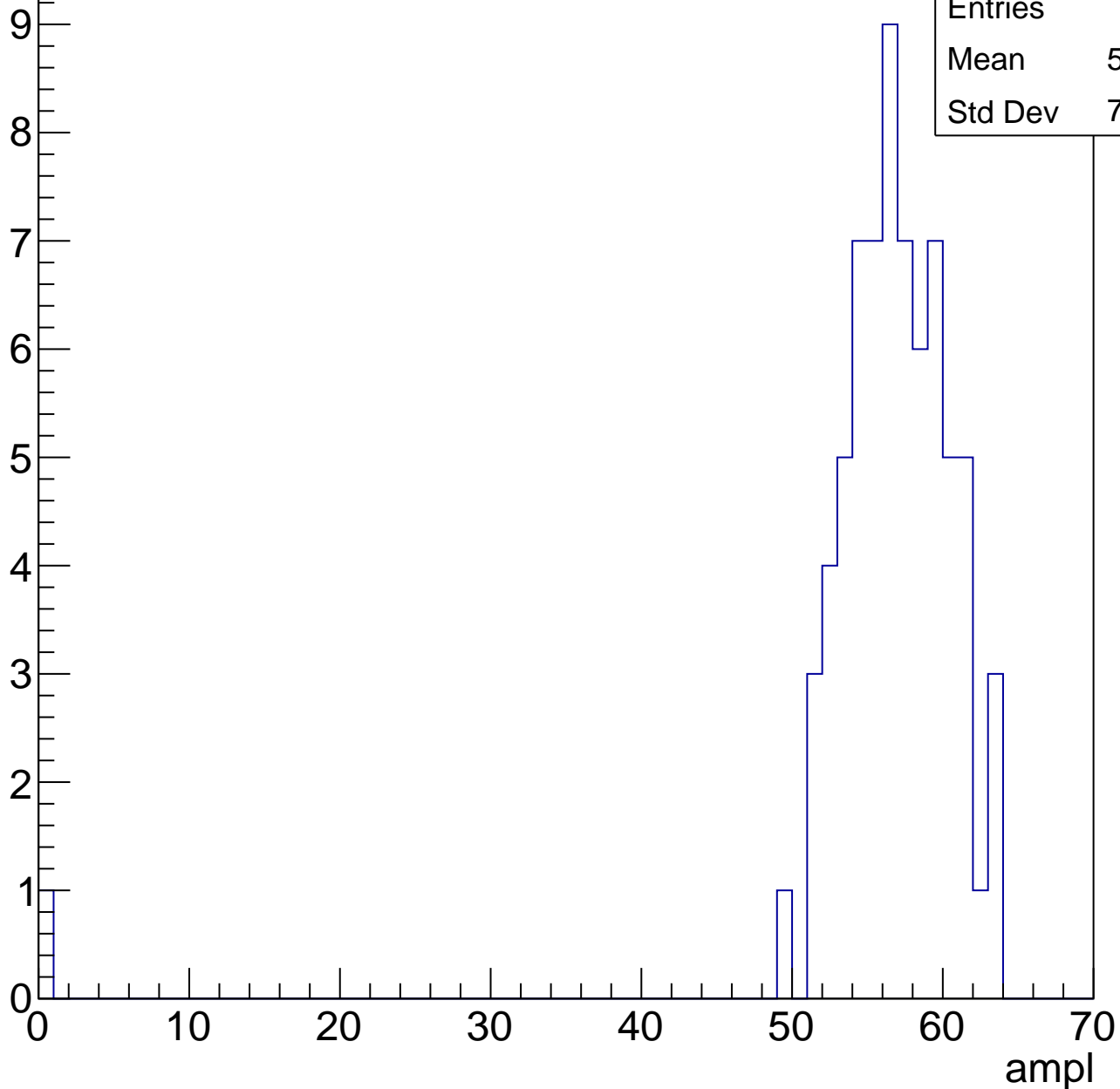


# B1L003S, U6-ch1, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	71
Mean	55.75
Std Dev	7.394

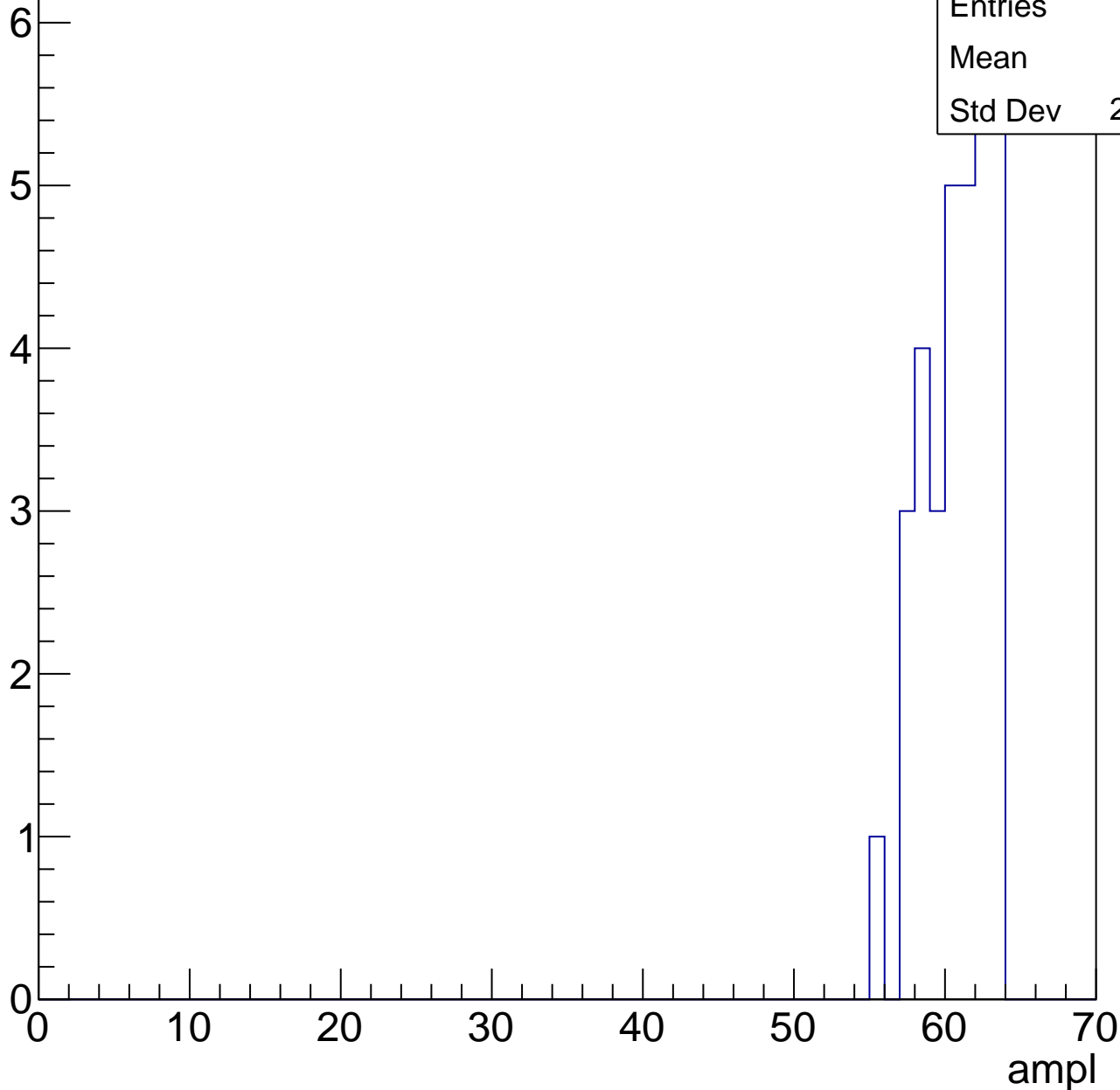


# B1L003S, U6-ch1, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

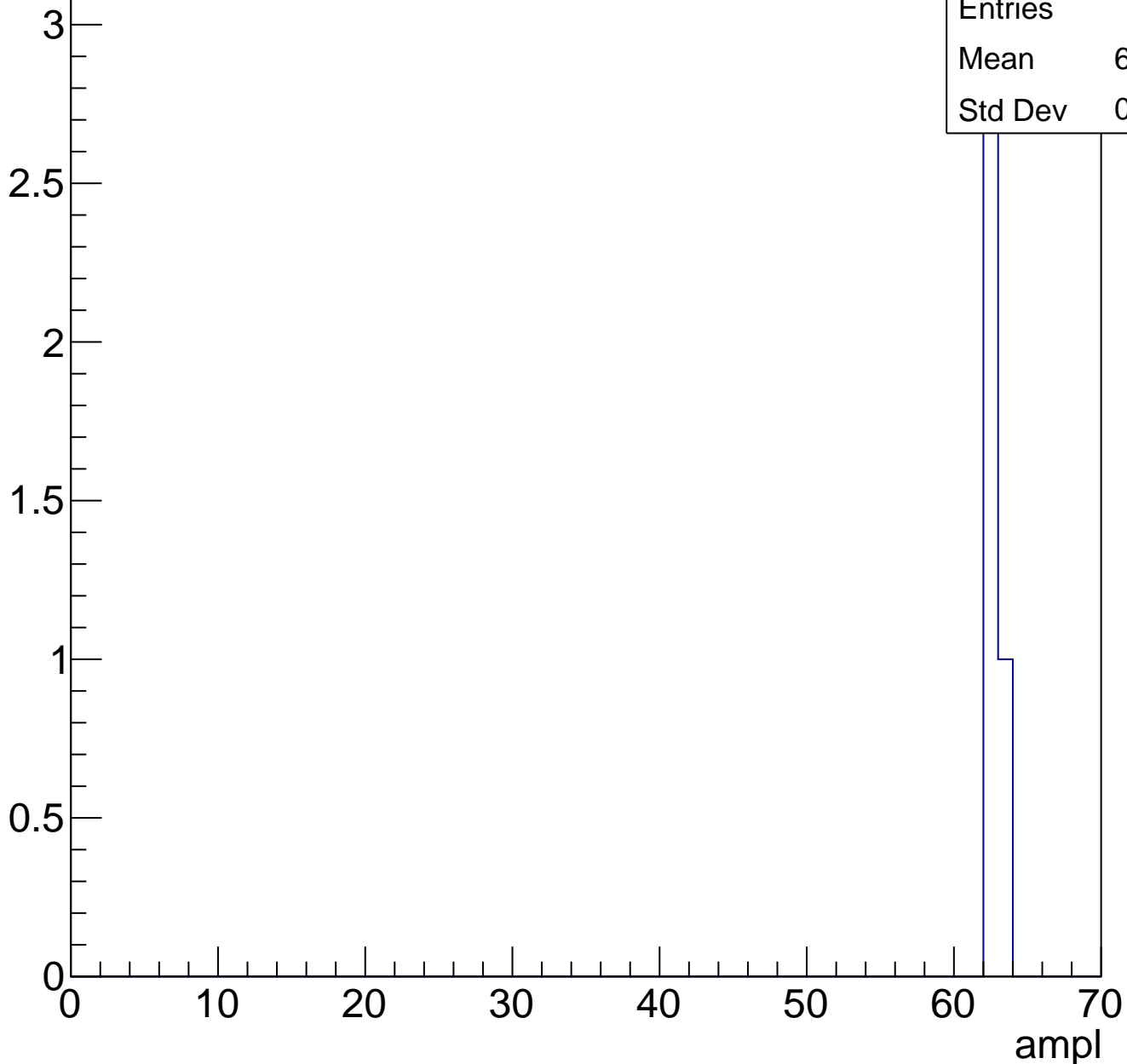
Entries	33
Mean	60.3
Std Dev	2.139



# B1L003S, U6-ch1, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch1, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U6-ch2, adc0

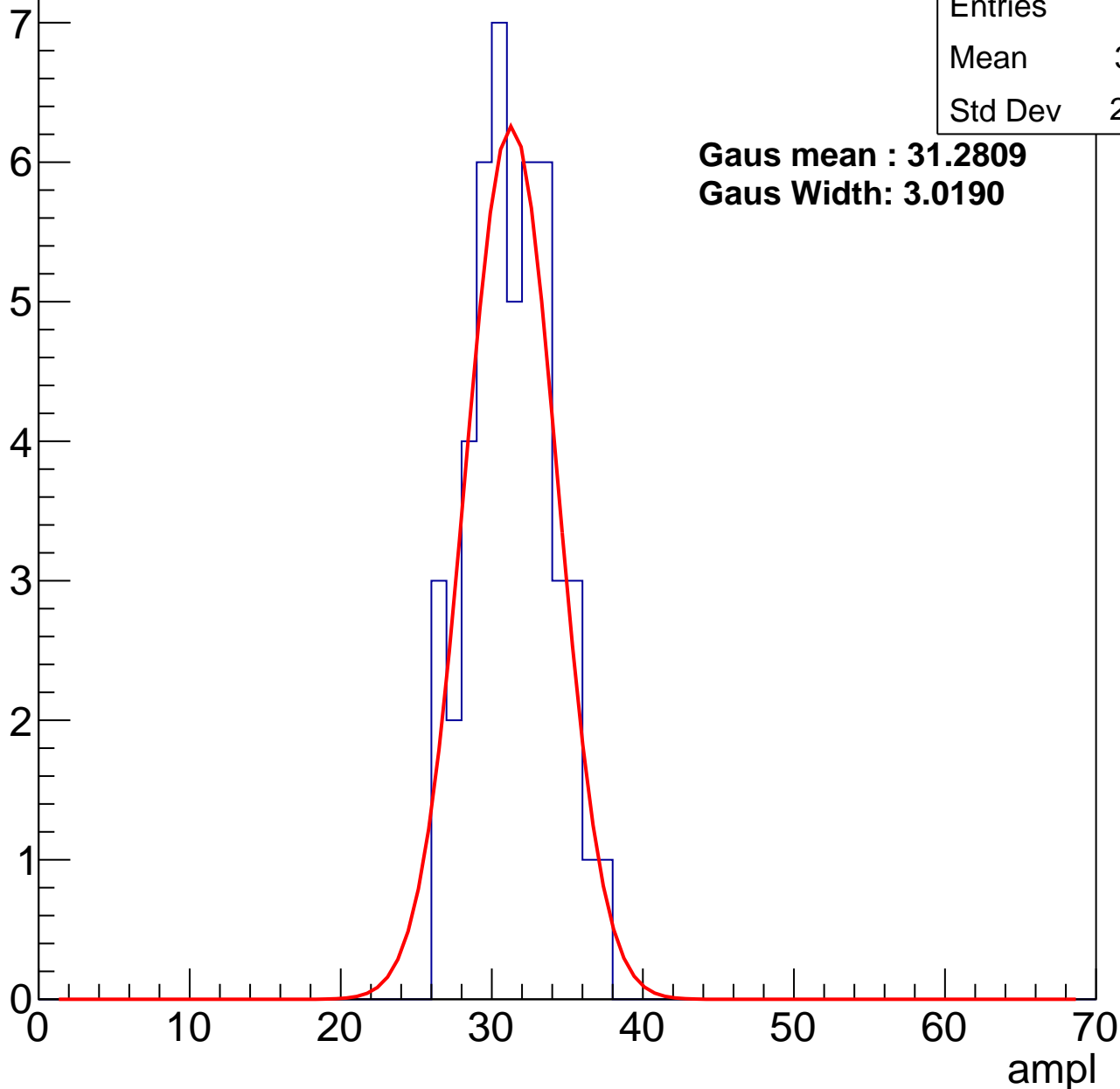
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	47
Mean	30.91
Std Dev	2.688

**Gaus mean : 31.2809**

**Gaus Width: 3.0190**



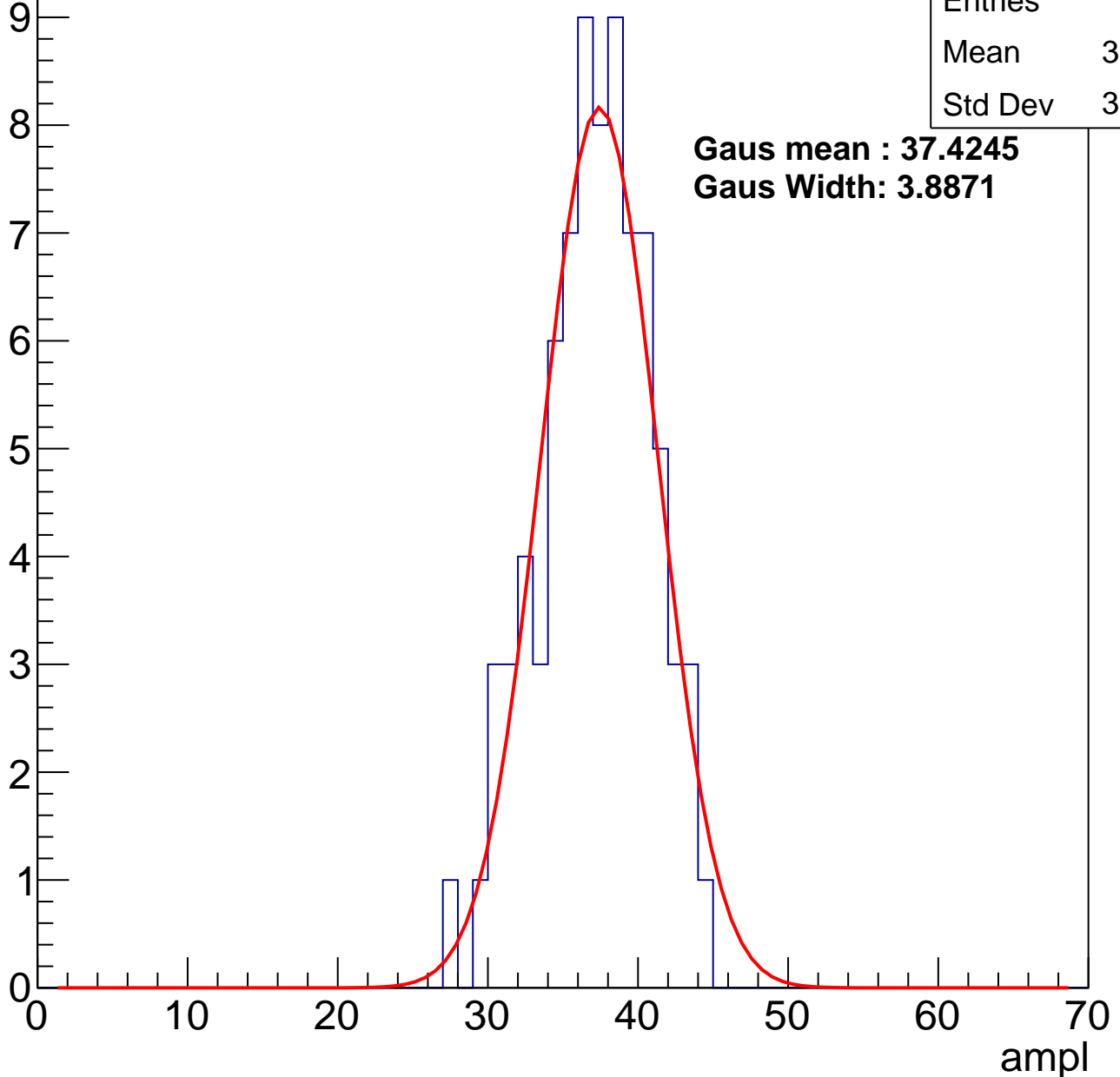
# B1L003S, U6-ch2, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	80
Mean	36.67
Std Dev	3.643

**Gaus mean : 37.4245**  
**Gaus Width: 3.8871**



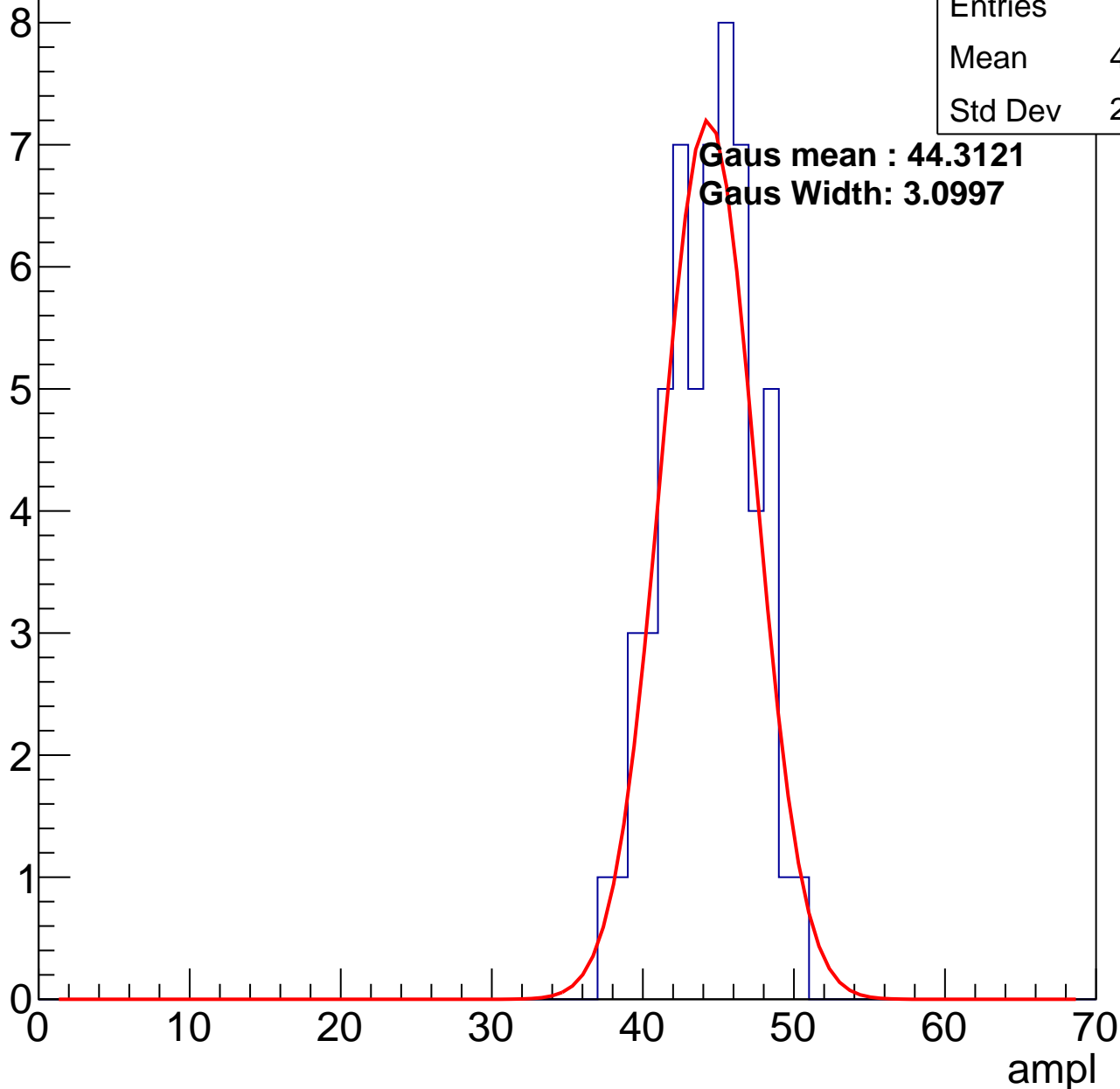
# B1L003S, U6-ch2, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	43.84
Std Dev	2.929

**Gaus mean : 44.3121**  
**Gaus Width: 3.0997**

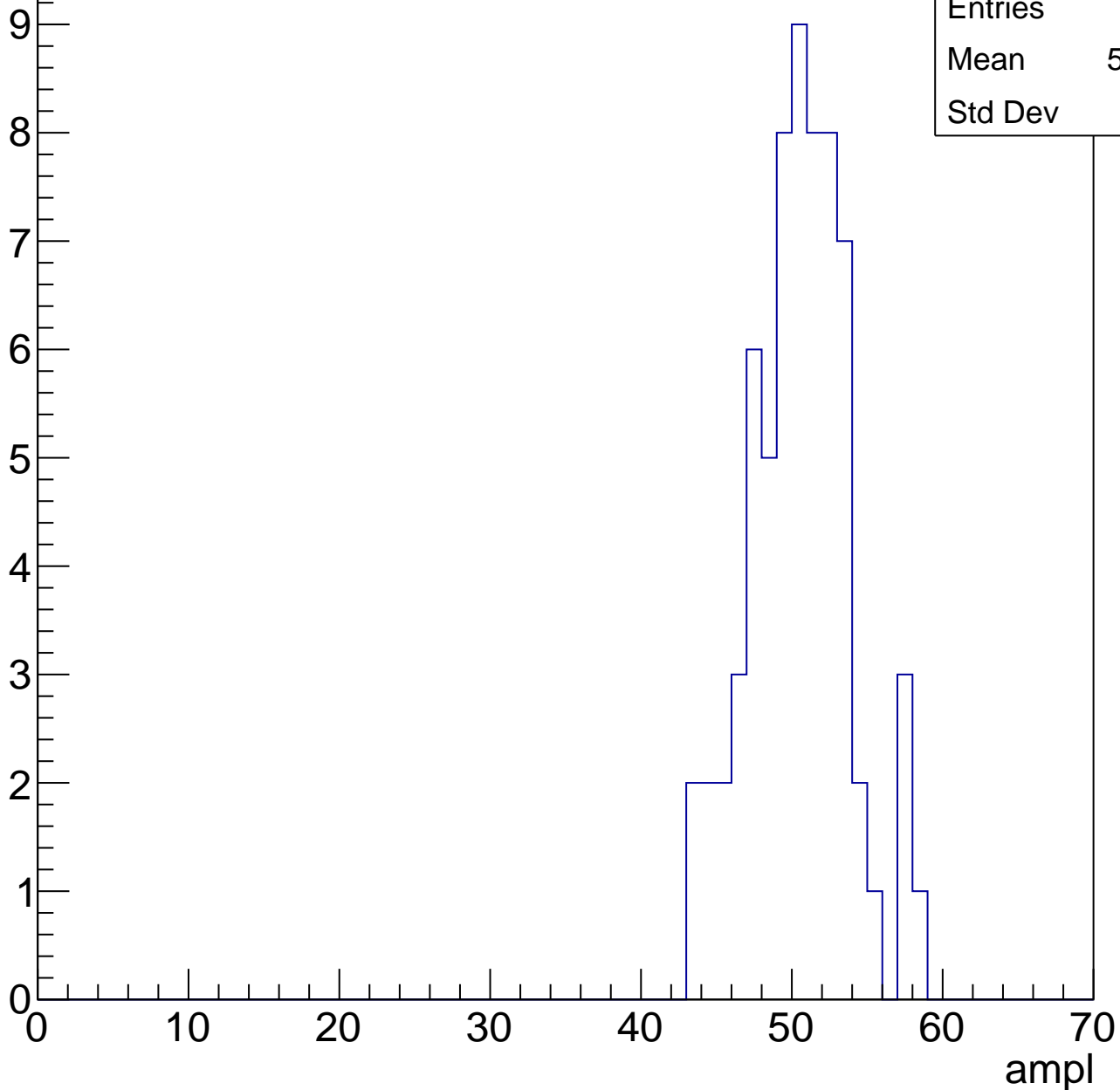


# B1L003S, U6-ch2, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	50.04
Std Dev	3.28

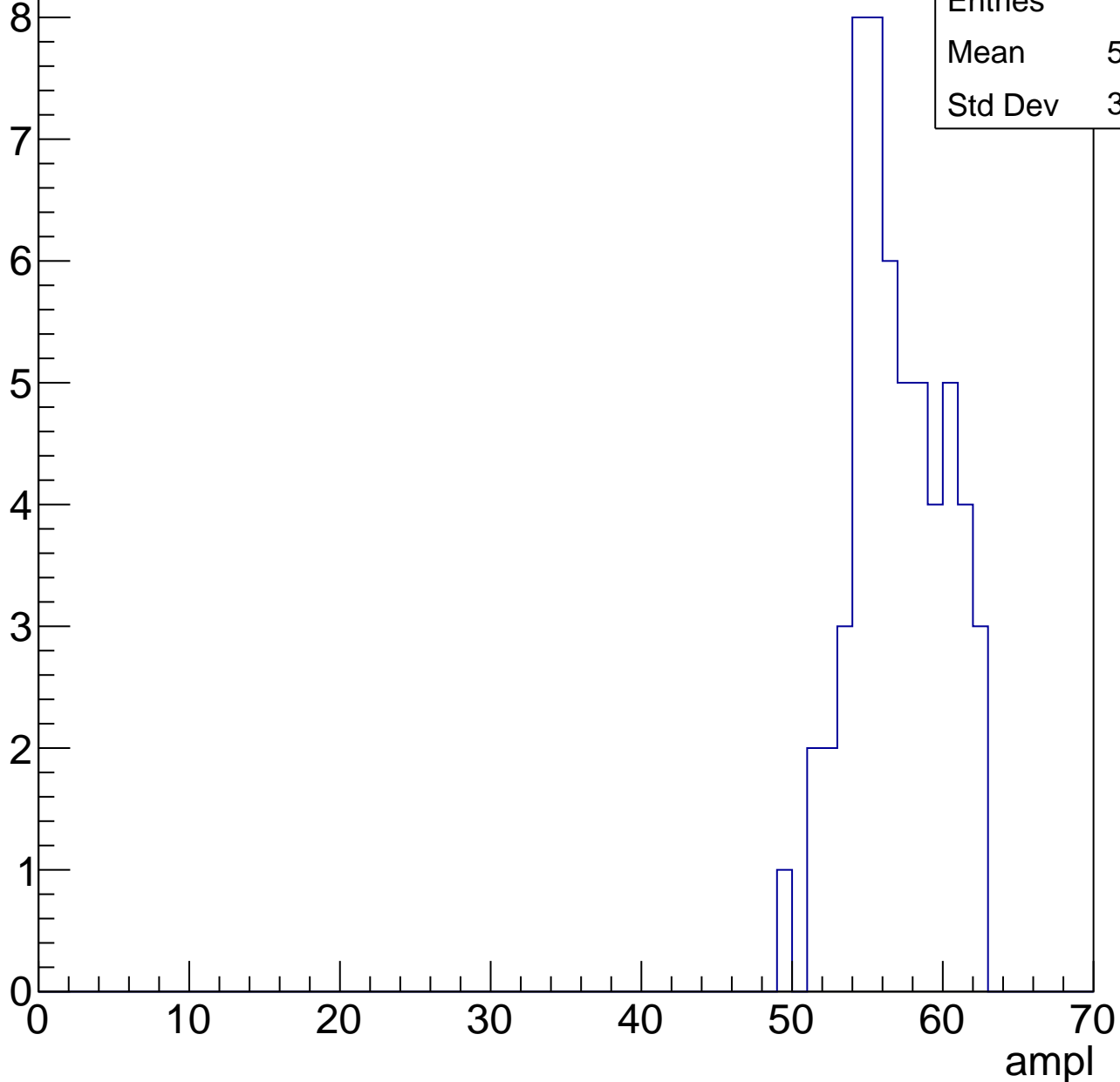


# B1L003S, U6-ch2, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	56.48
Std Dev	3.088

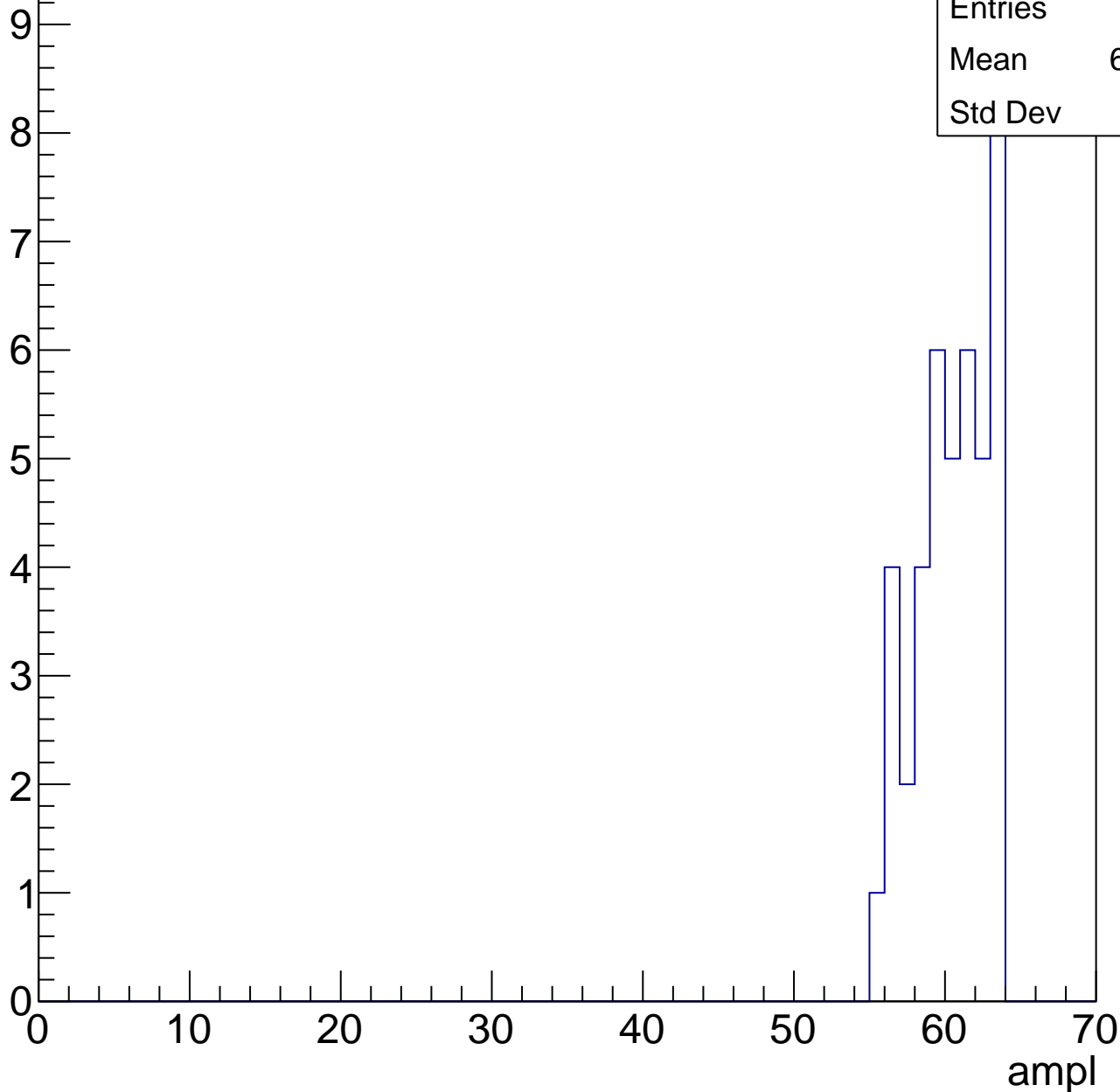


# B1L003S, U6-ch2, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

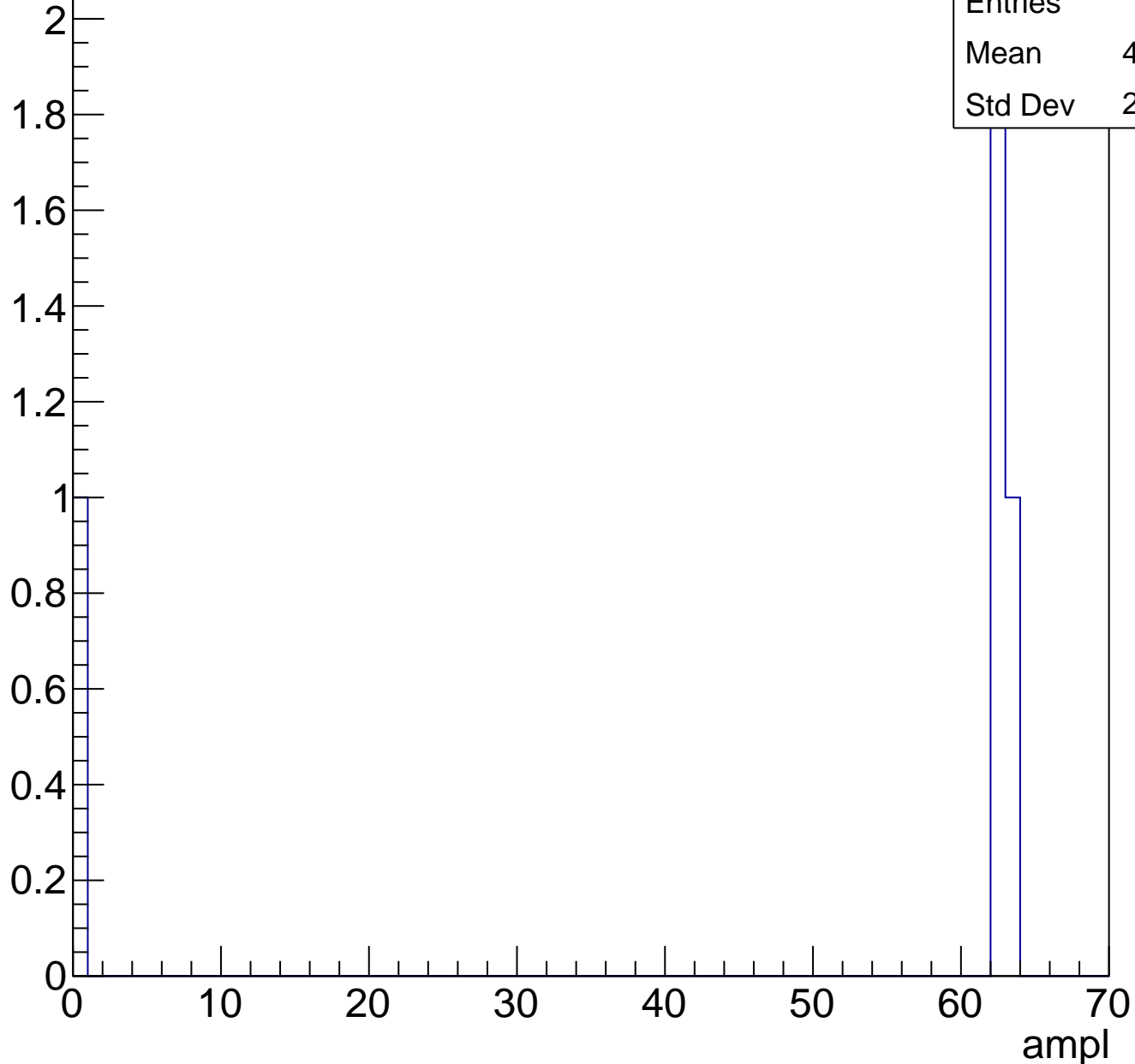
Entries	42
Mean	60.05
Std Dev	2.37



# B1L003S, U6-ch2, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch2, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	12.5
Std Dev	12.5

ampl

# B1L003S, U6-ch3, adc0

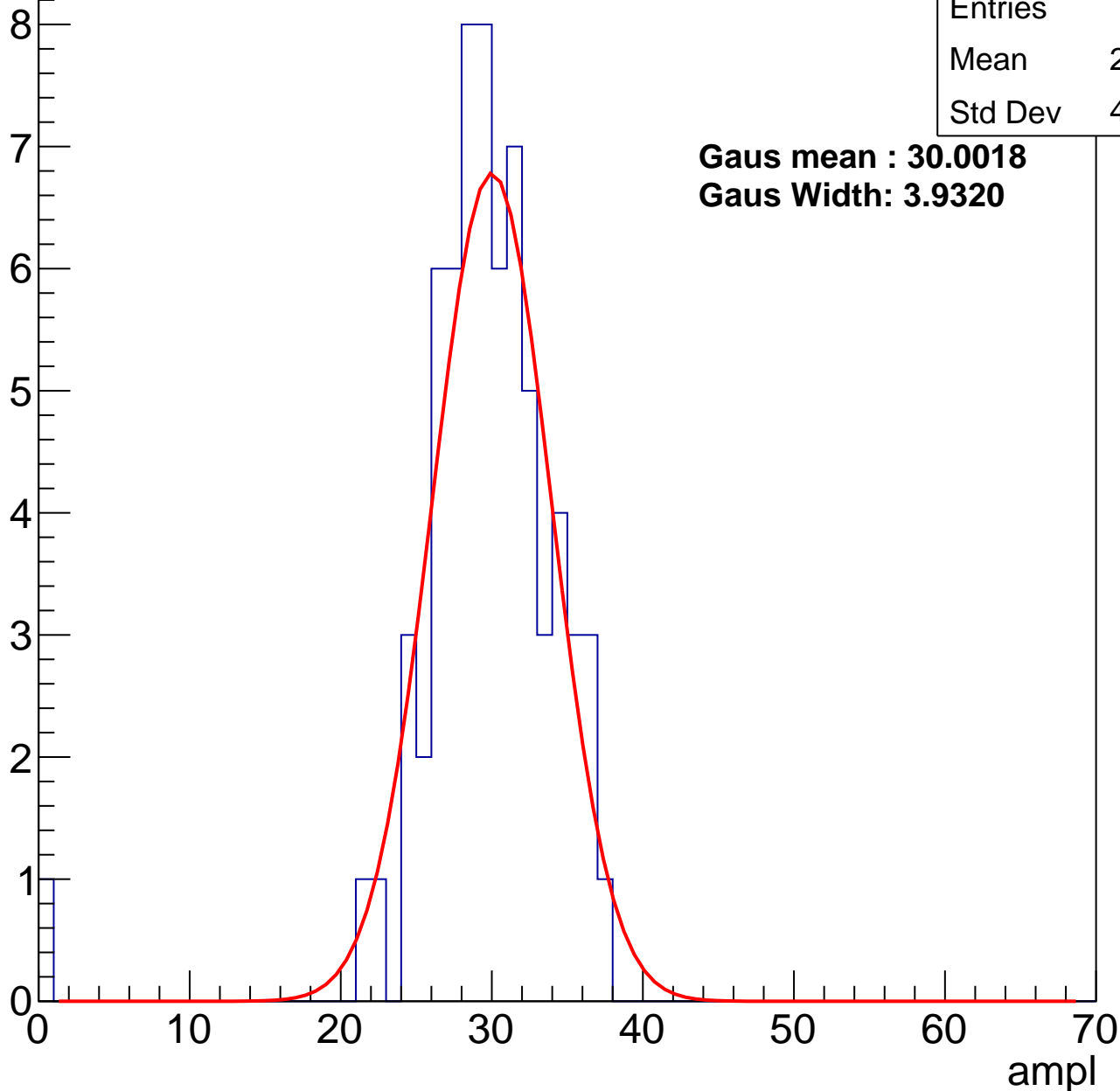
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	29.13
Std Dev	4.988

**Gaus mean : 30.0018**

**Gaus Width: 3.9320**



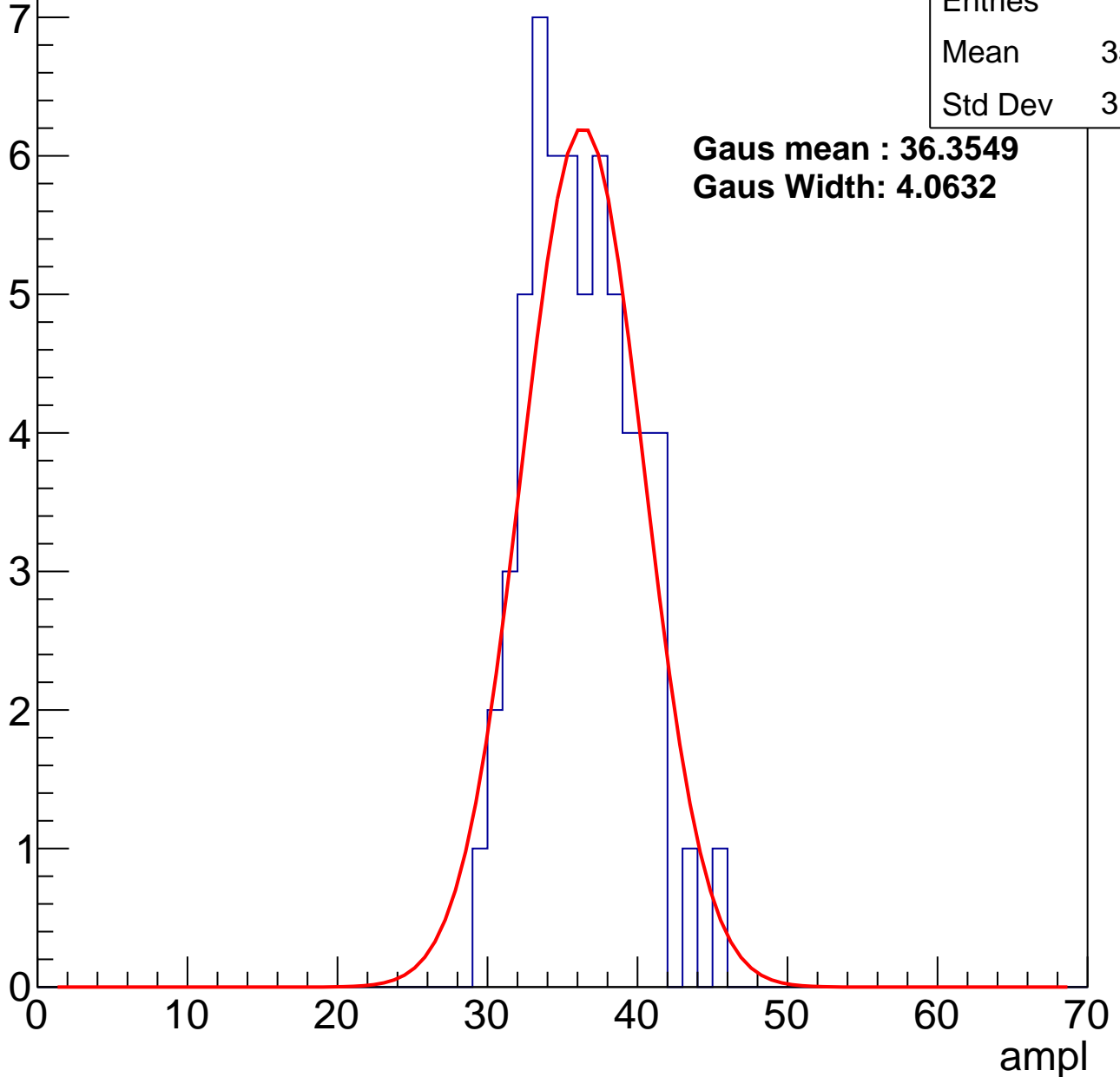
# B1L003S, U6-ch3, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	35.78
Std Dev	3.469

**Gaus mean : 36.3549**  
**Gaus Width: 4.0632**



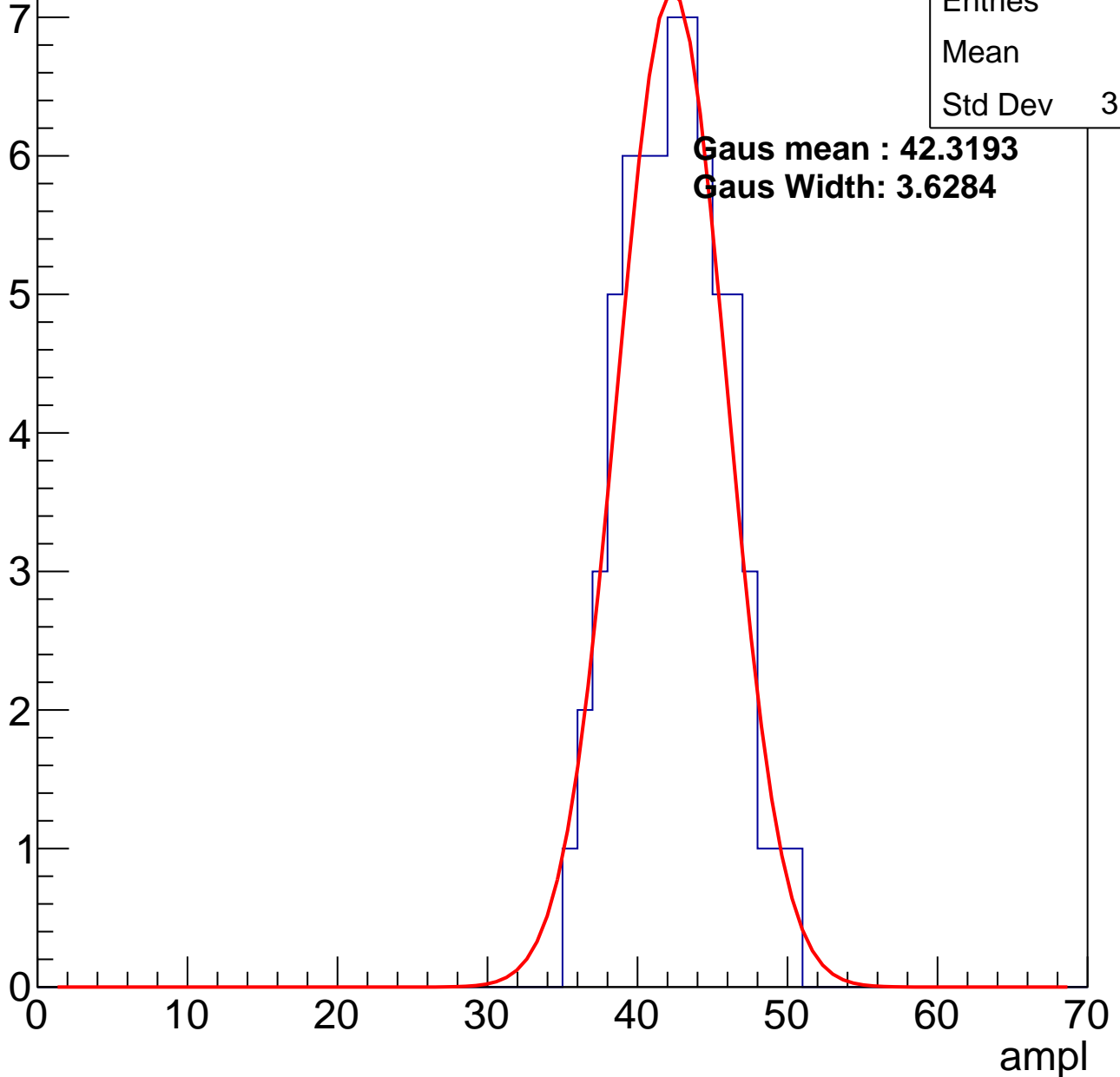
# B1L003S, U6-ch3, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	42
Std Dev	3.374

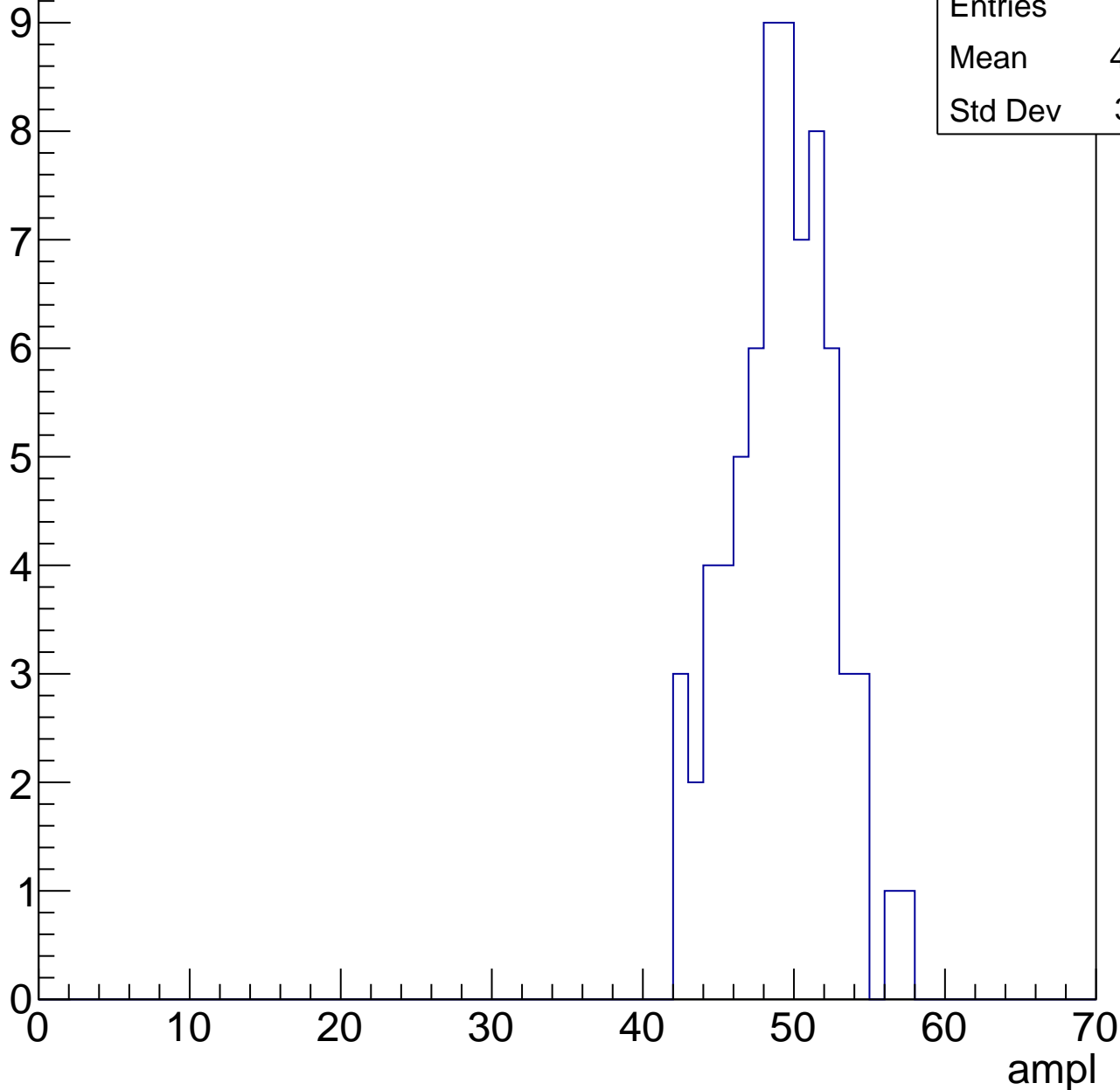
**Gaus mean : 42.3193**  
**Gaus Width: 3.6284**



# B1L003S, U6-ch3, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch3, adc4

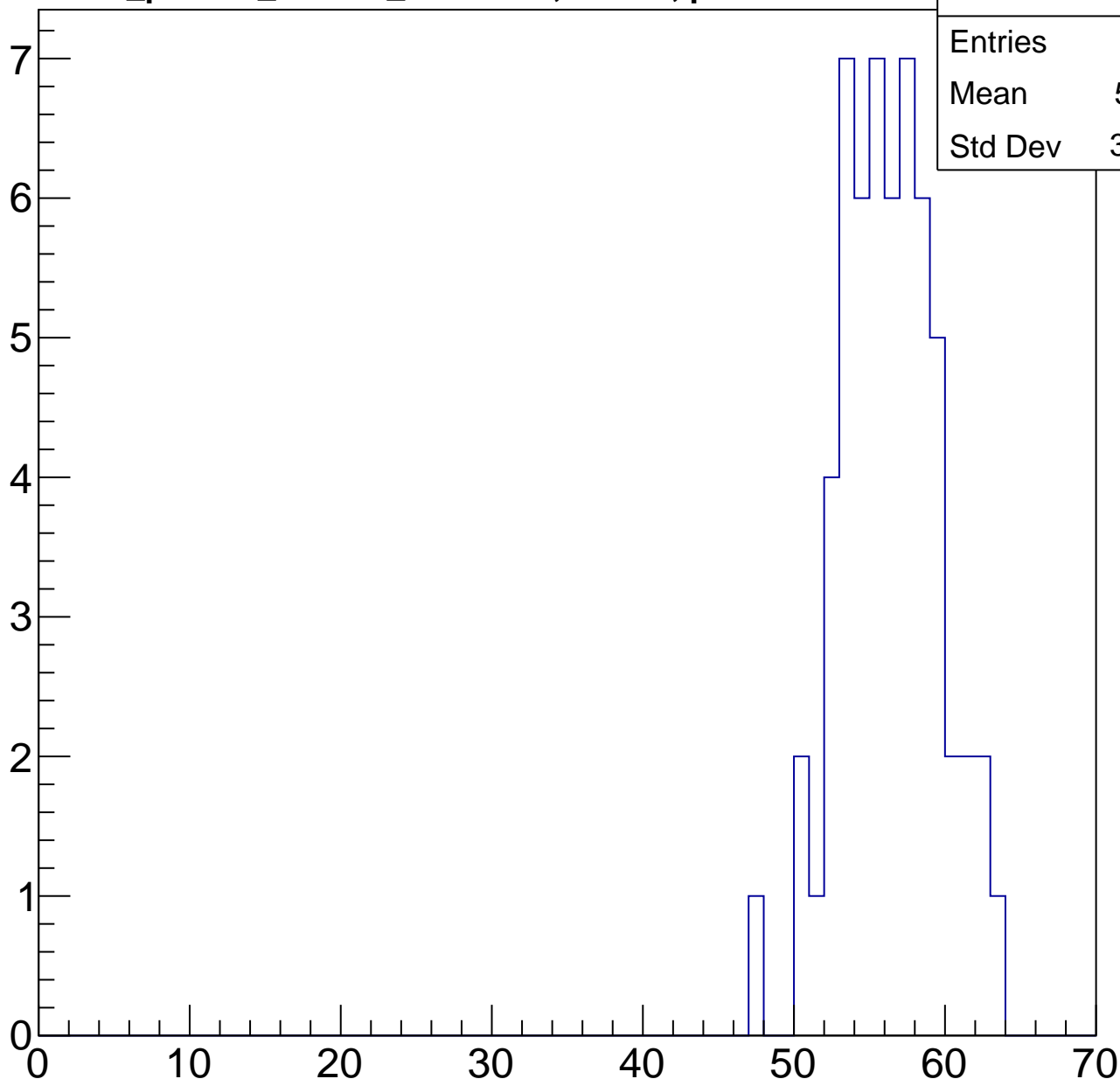
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

7  
6  
5  
4  
3  
2  
1  
0

Entries	59
Mean	55.81
Std Dev	3.223

ampl

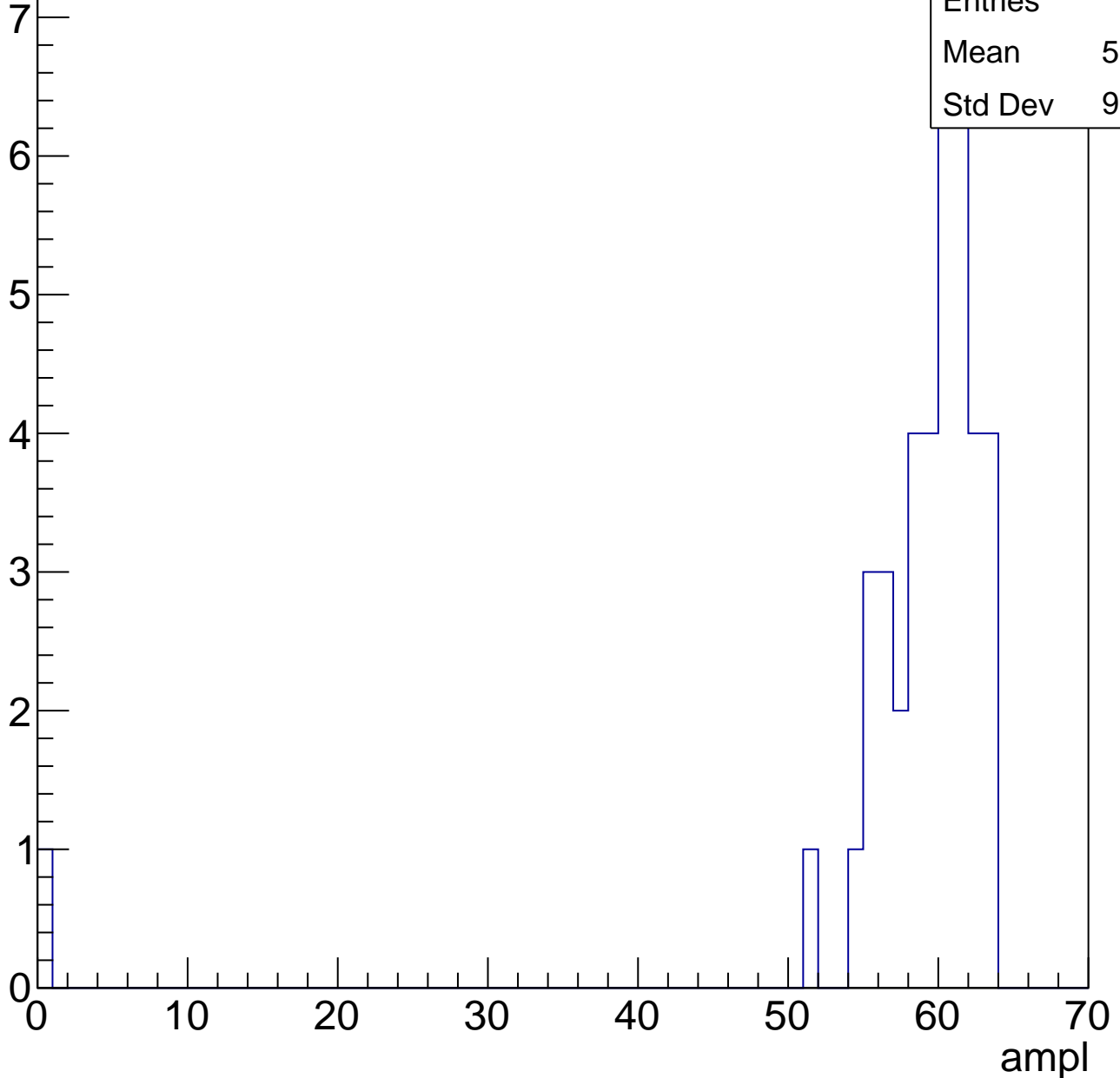


# B1L003S, U6-ch3, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	41
Mean	57.73
Std Dev	9.533

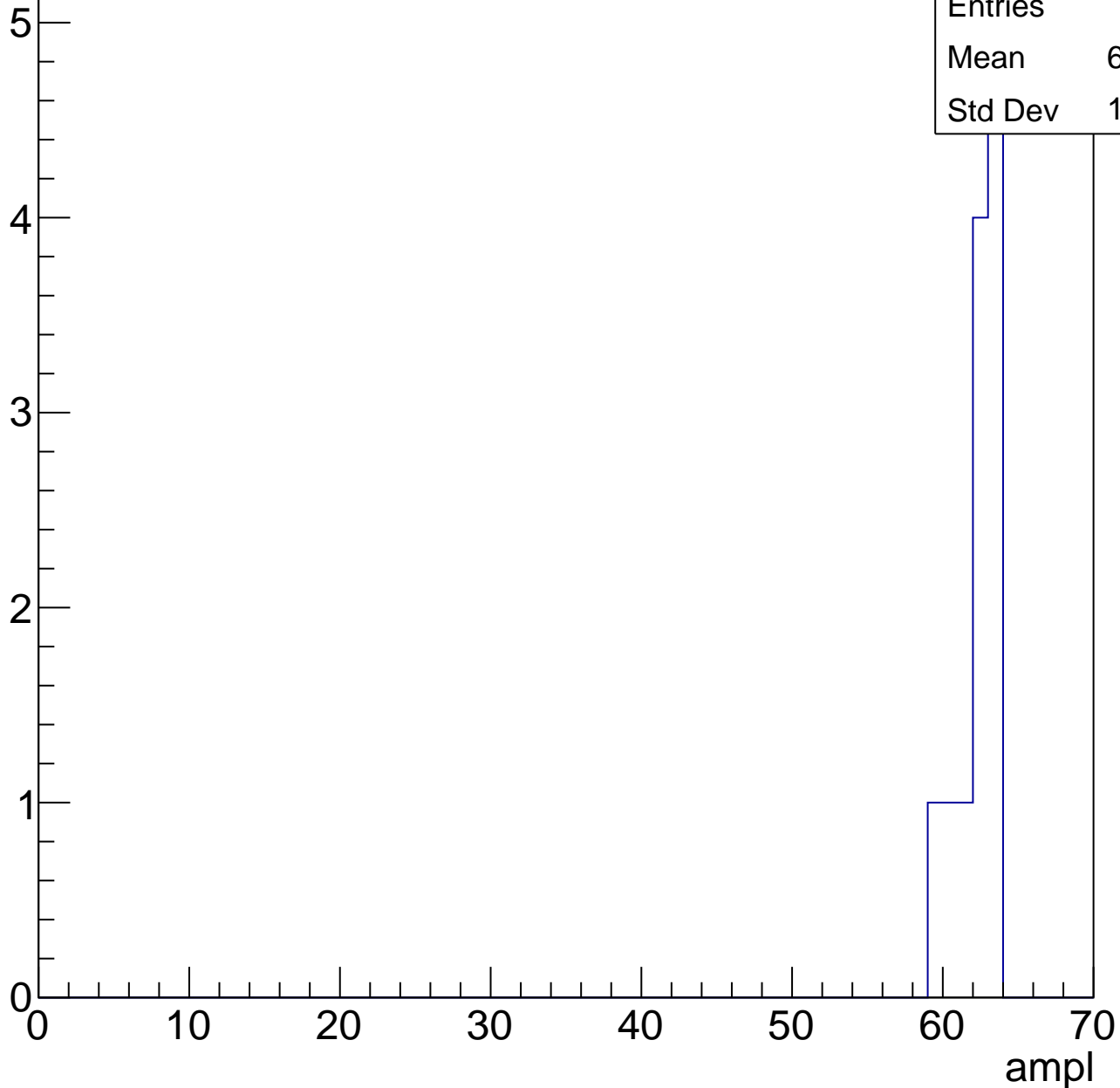


# B1L003S, U6-ch3, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	12
Mean	61.92
Std Dev	1.256





# B1L003S, U6-ch3, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U6-ch4, adc0

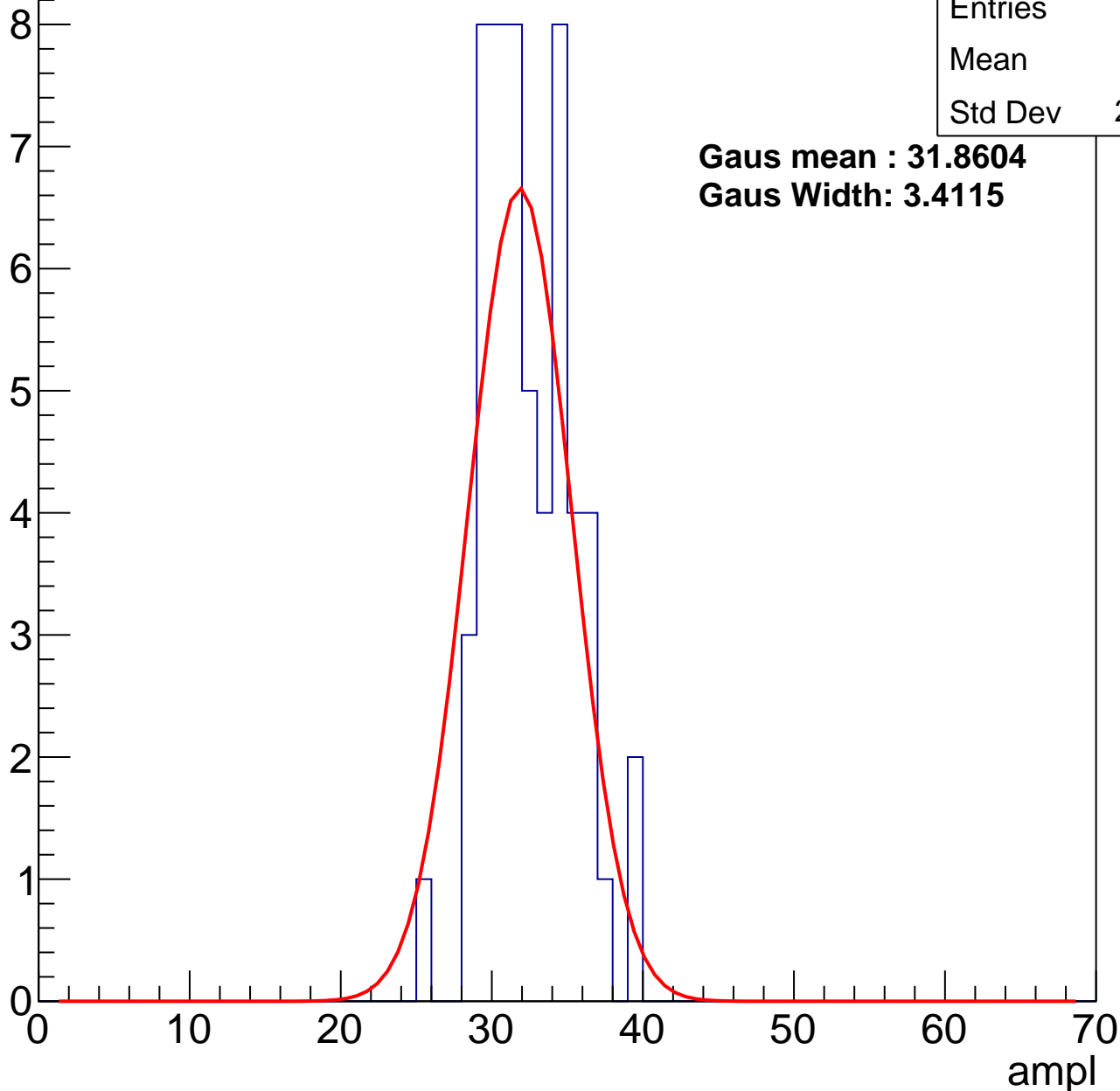
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	32
Std Dev	2.891

**Gaus mean : 31.8604**

**Gaus Width: 3.4115**



# B1L003S, U6-ch4, adc1

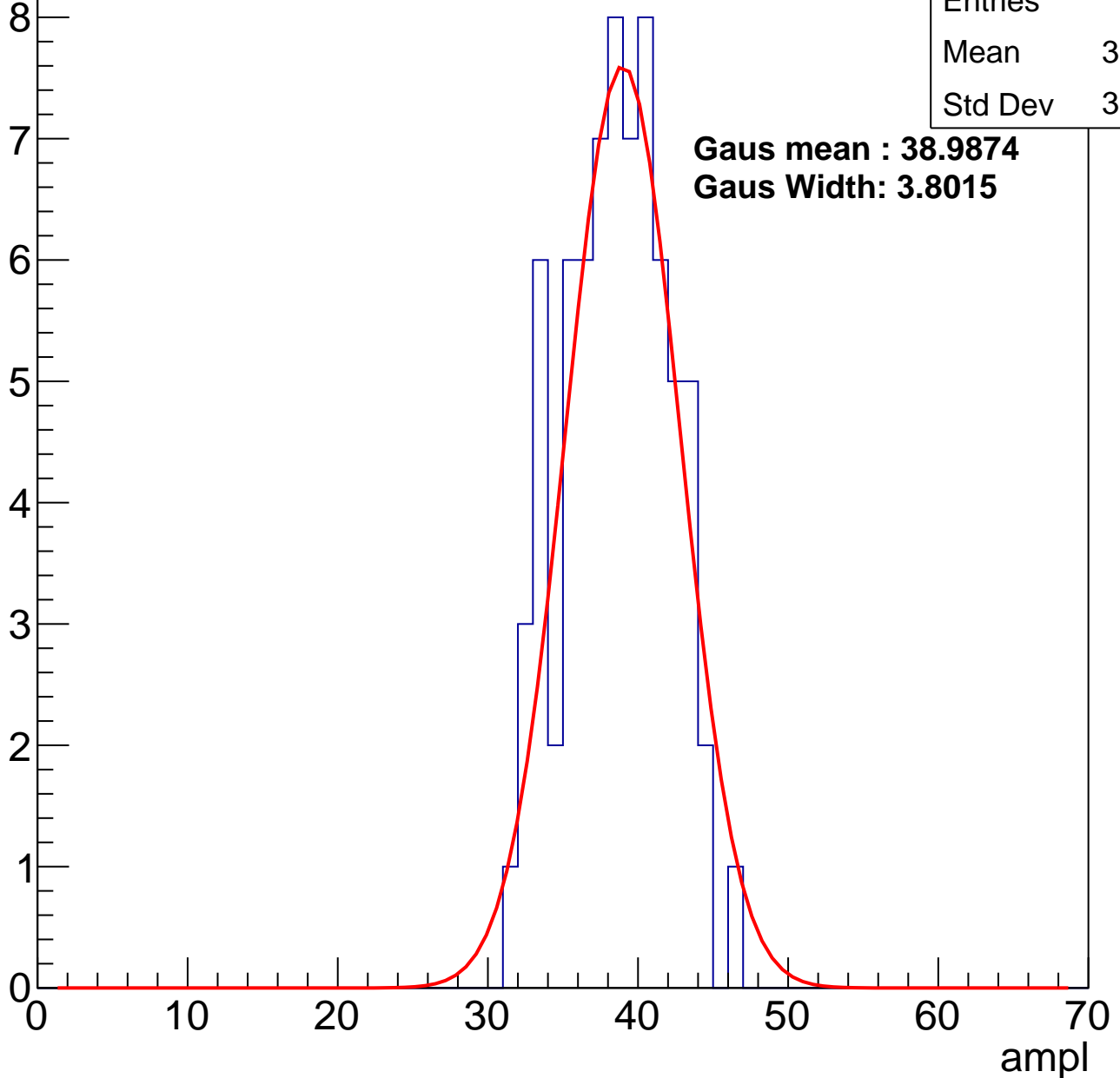
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	73
Mean	38.08
Std Dev	3.427

**Gaus mean : 38.9874**

**Gaus Width: 3.8015**



# B1L003S, U6-ch4, adc2

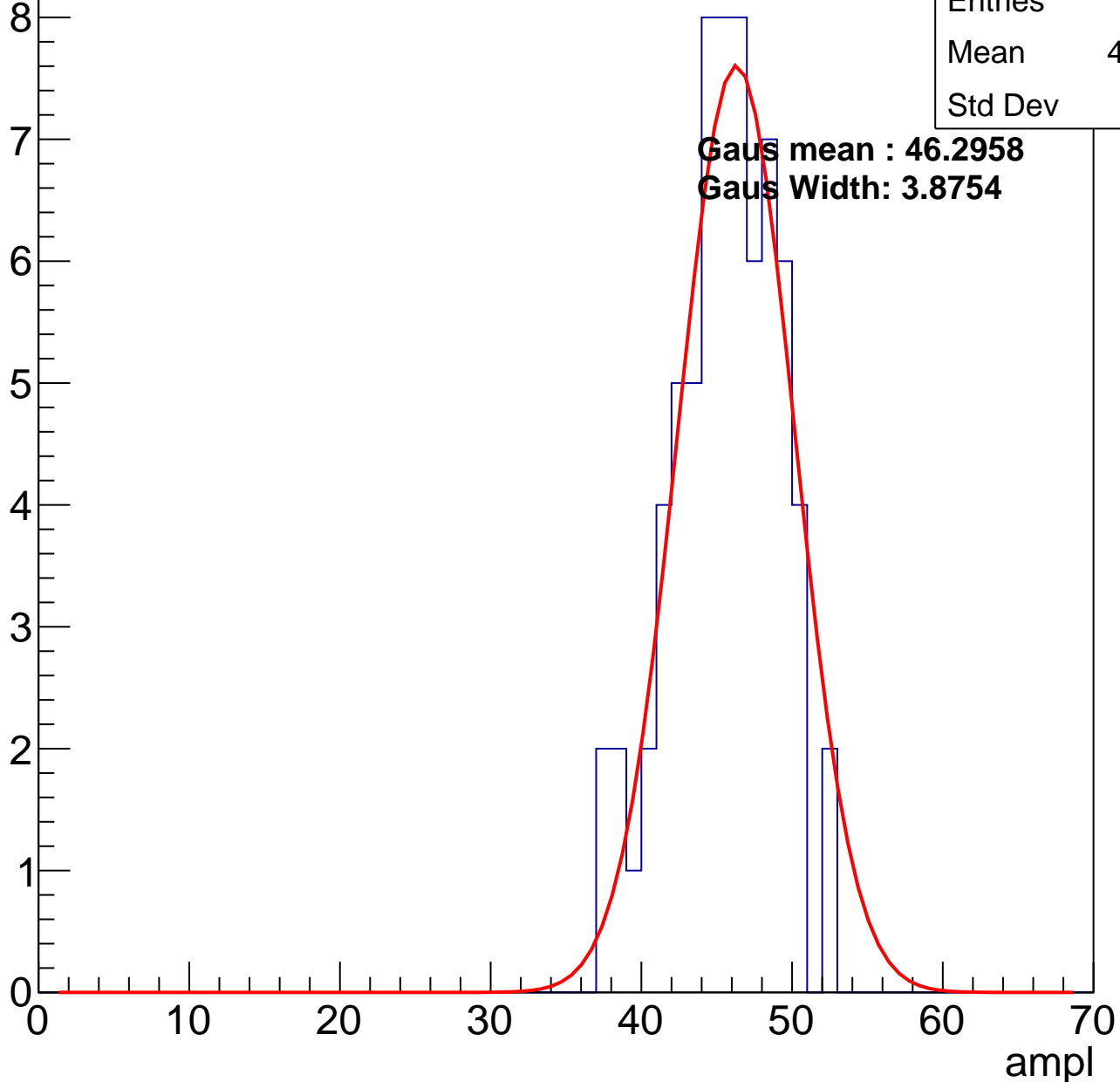
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	45.06
Std Dev	3.46

**Gaus mean : 46.2958**

**Gaus Width: 3.8754**



# B1L003S, U6-ch4, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

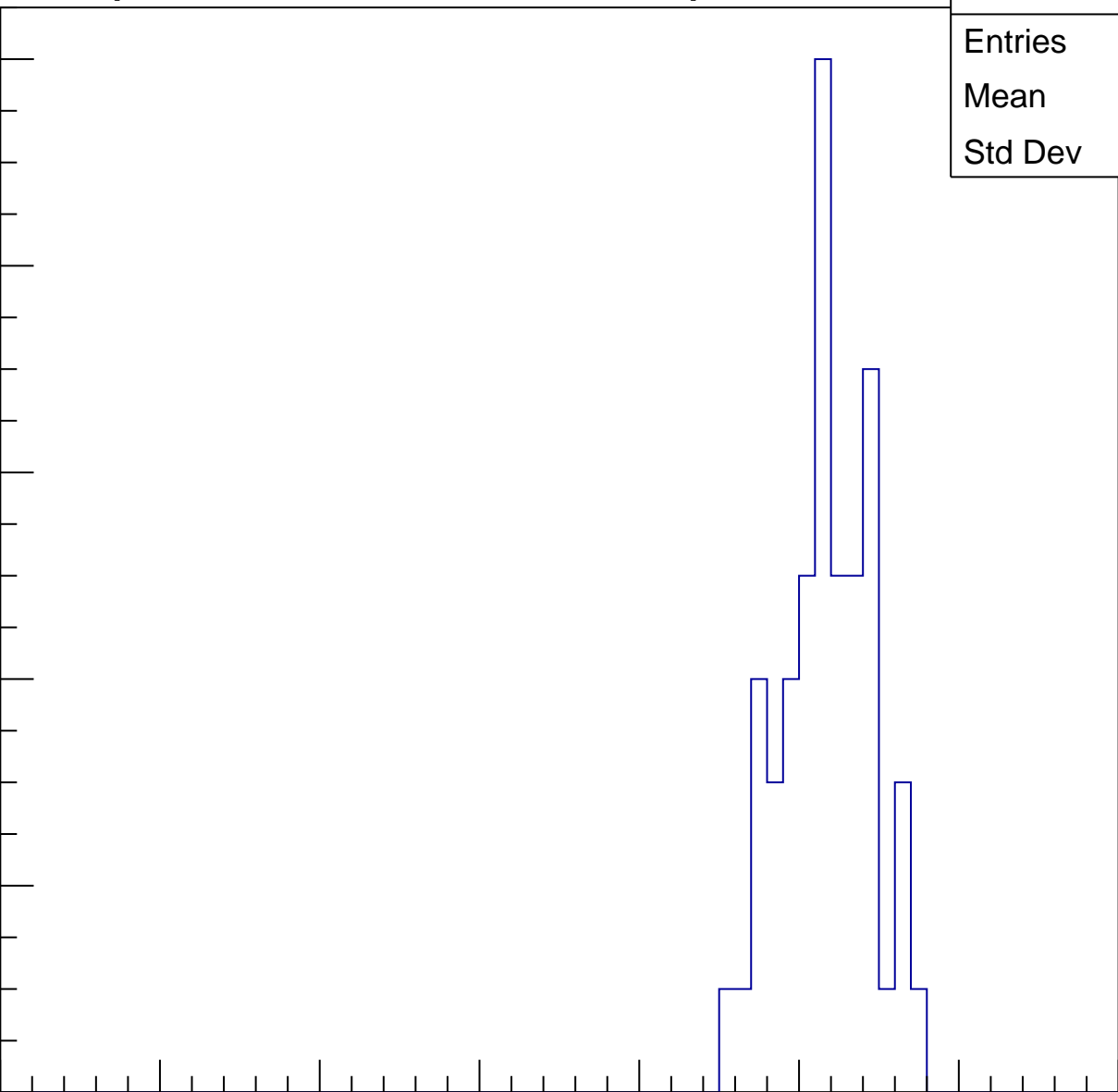
Entries	50
Mean	51.24
Std Dev	2.775

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

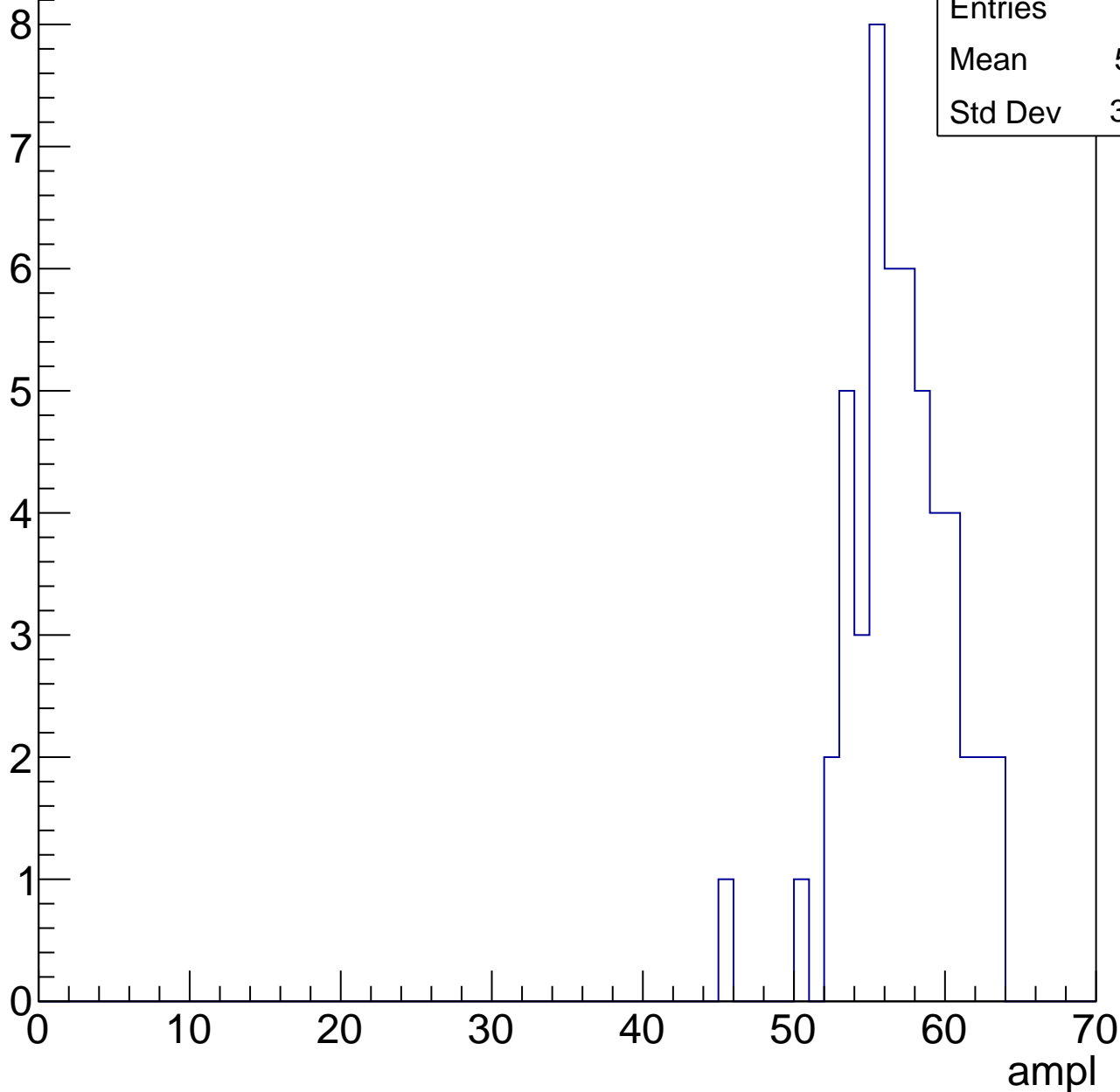


# B1L003S, U6-ch4, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	51
Mean	56.51
Std Dev	3.392

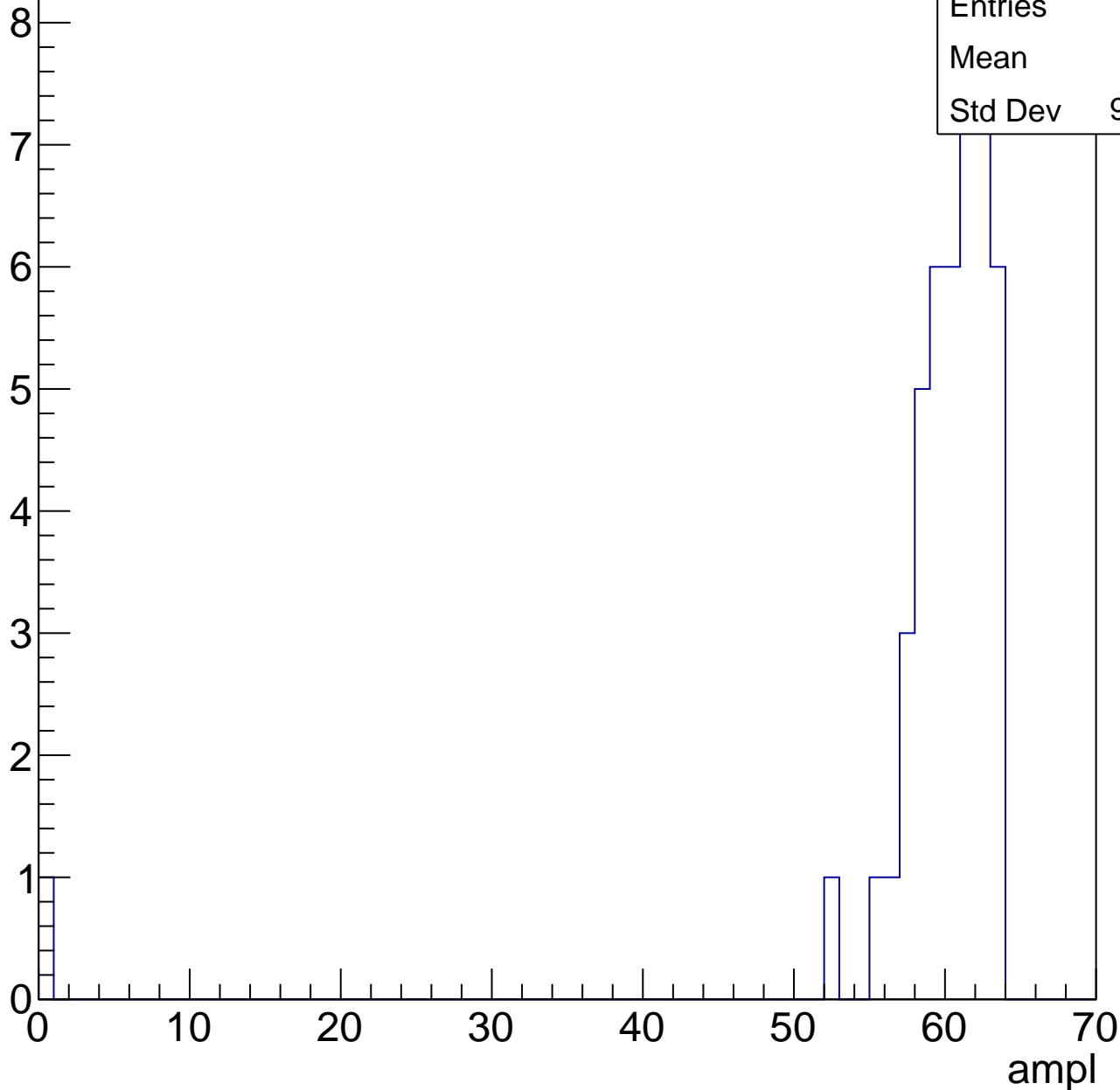


# B1L003S, U6-ch4, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	46
Mean	58.7
Std Dev	9.057



# B1L003S, U6-ch4, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	63
Std Dev	0

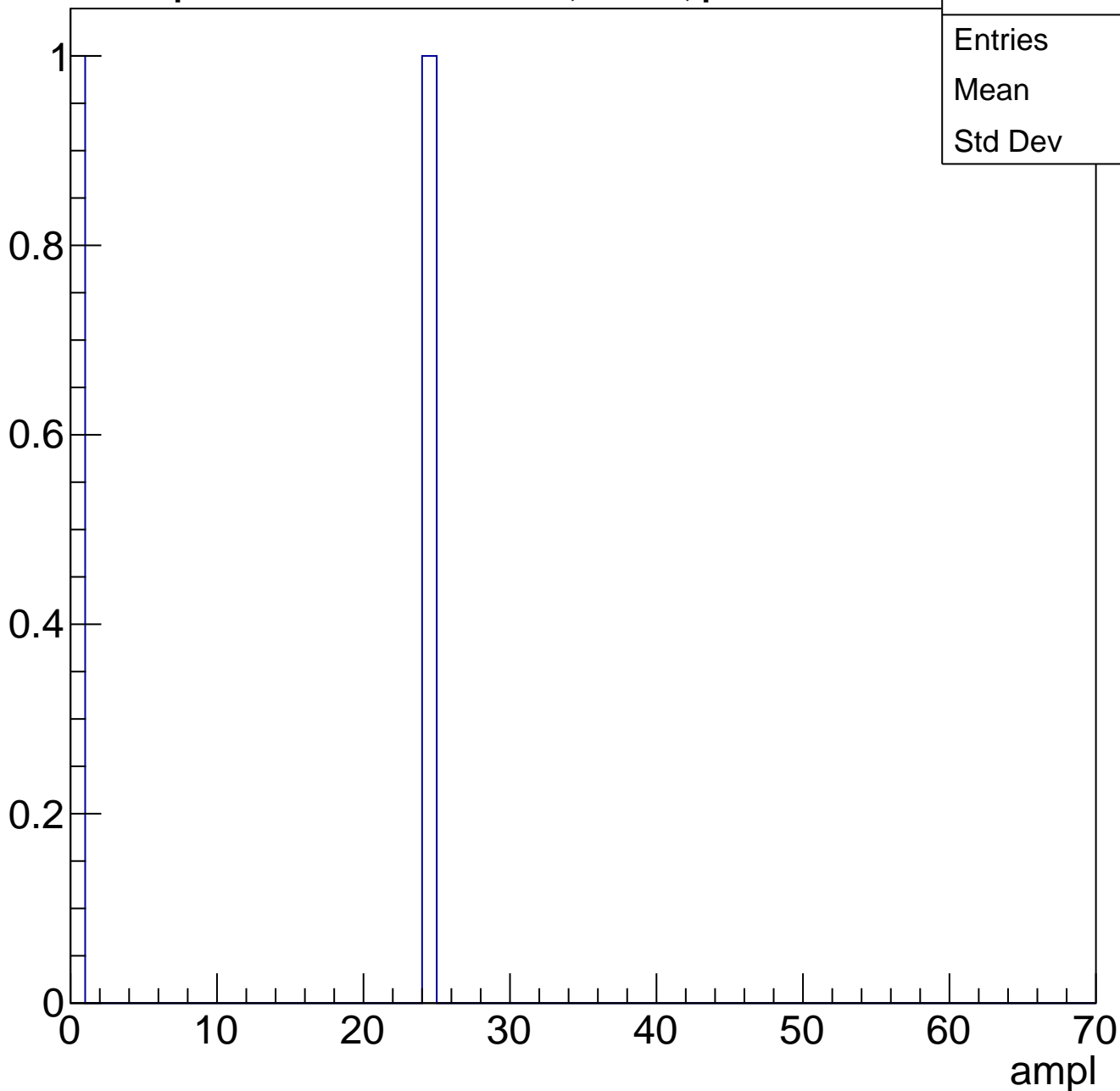
ampl



# B1L003S, U6-ch4, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch5, adc0

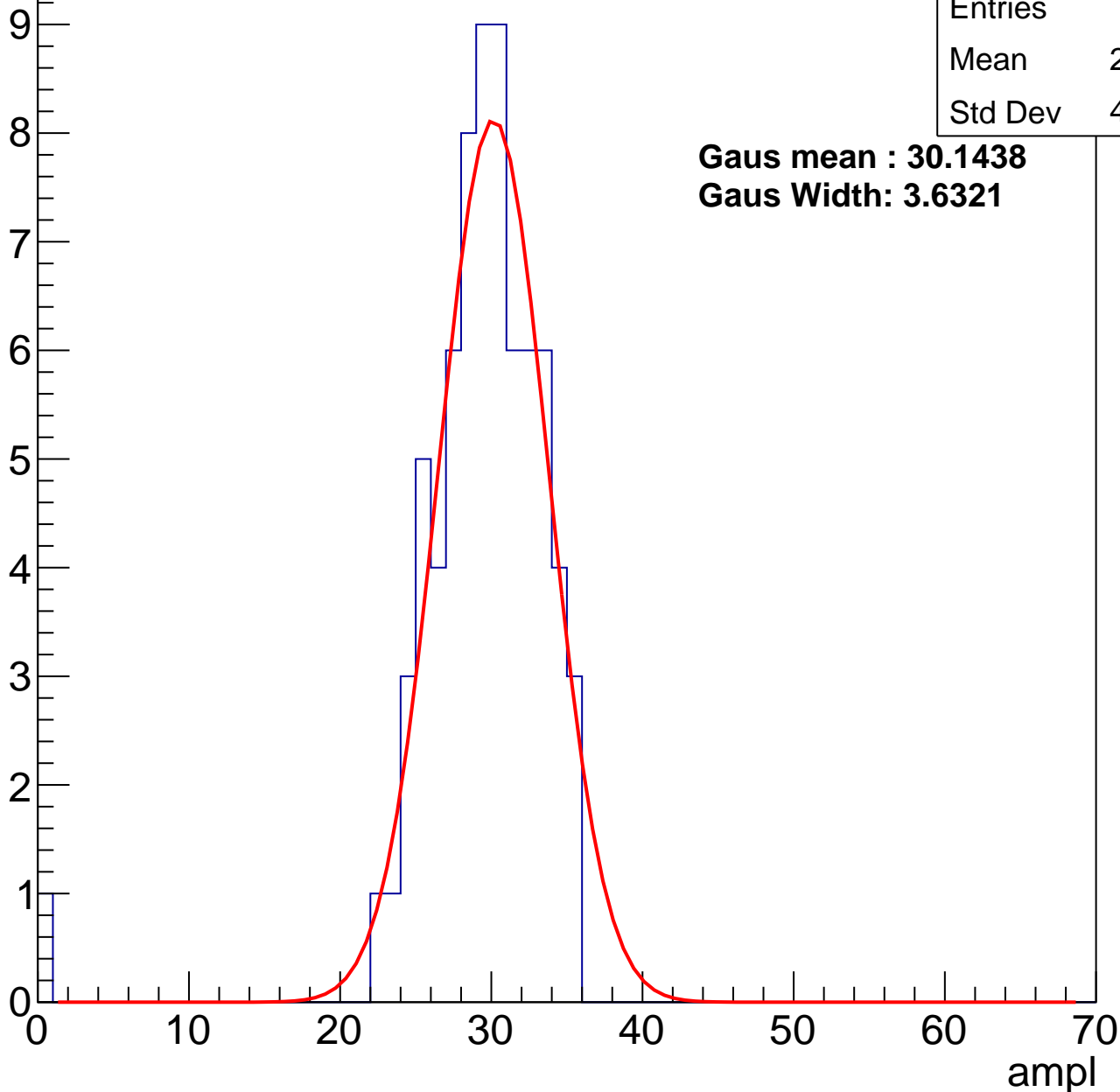
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	72
Mean	28.89
Std Dev	4.623

**Gaus mean : 30.1438**

**Gaus Width: 3.6321**

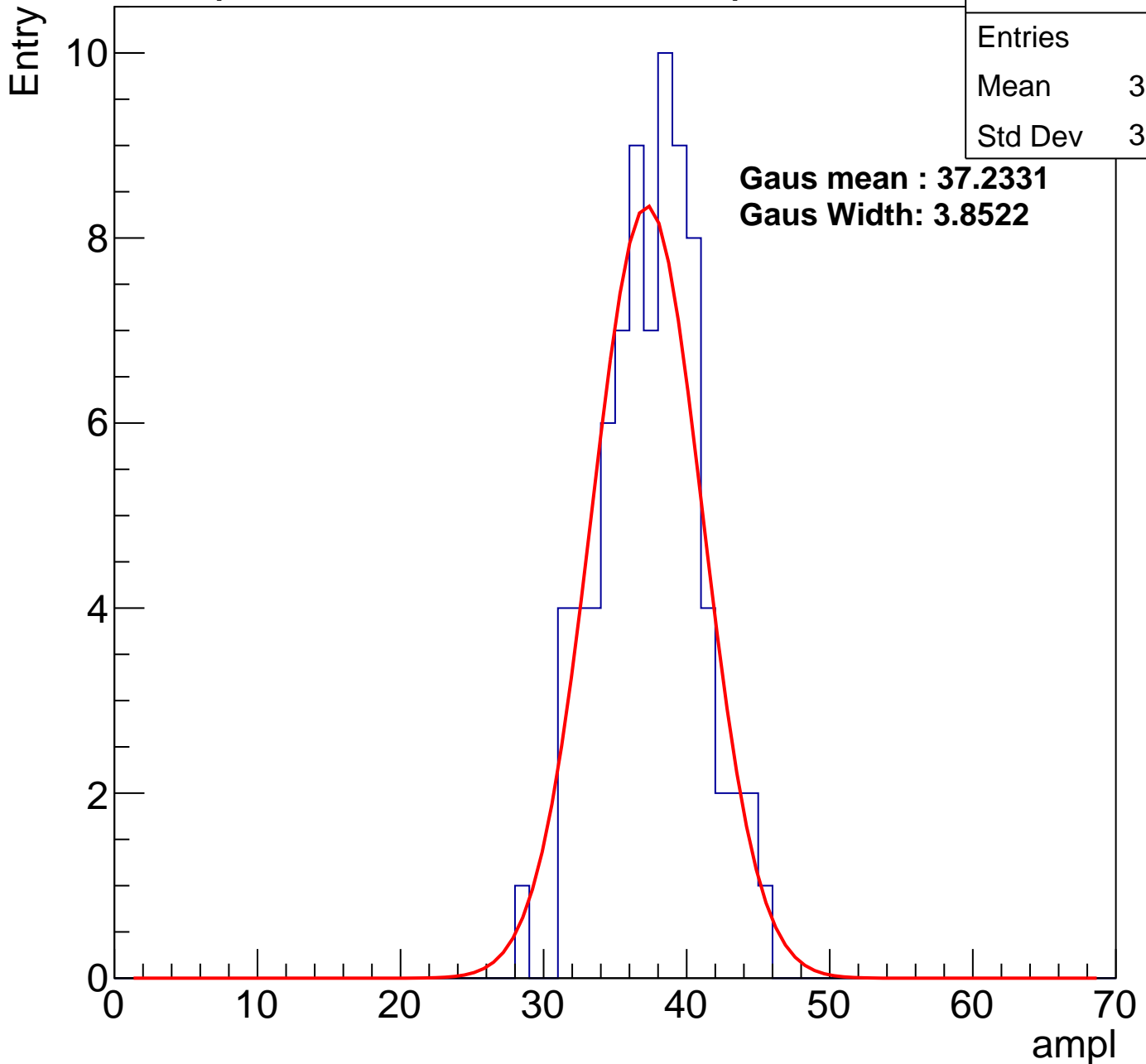


# B1L003S, U6-ch5, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	80
Mean	37.02
Std Dev	3.439

**Gaus mean : 37.2331**  
**Gaus Width: 3.8522**



# B1L003S, U6-ch5, adc2

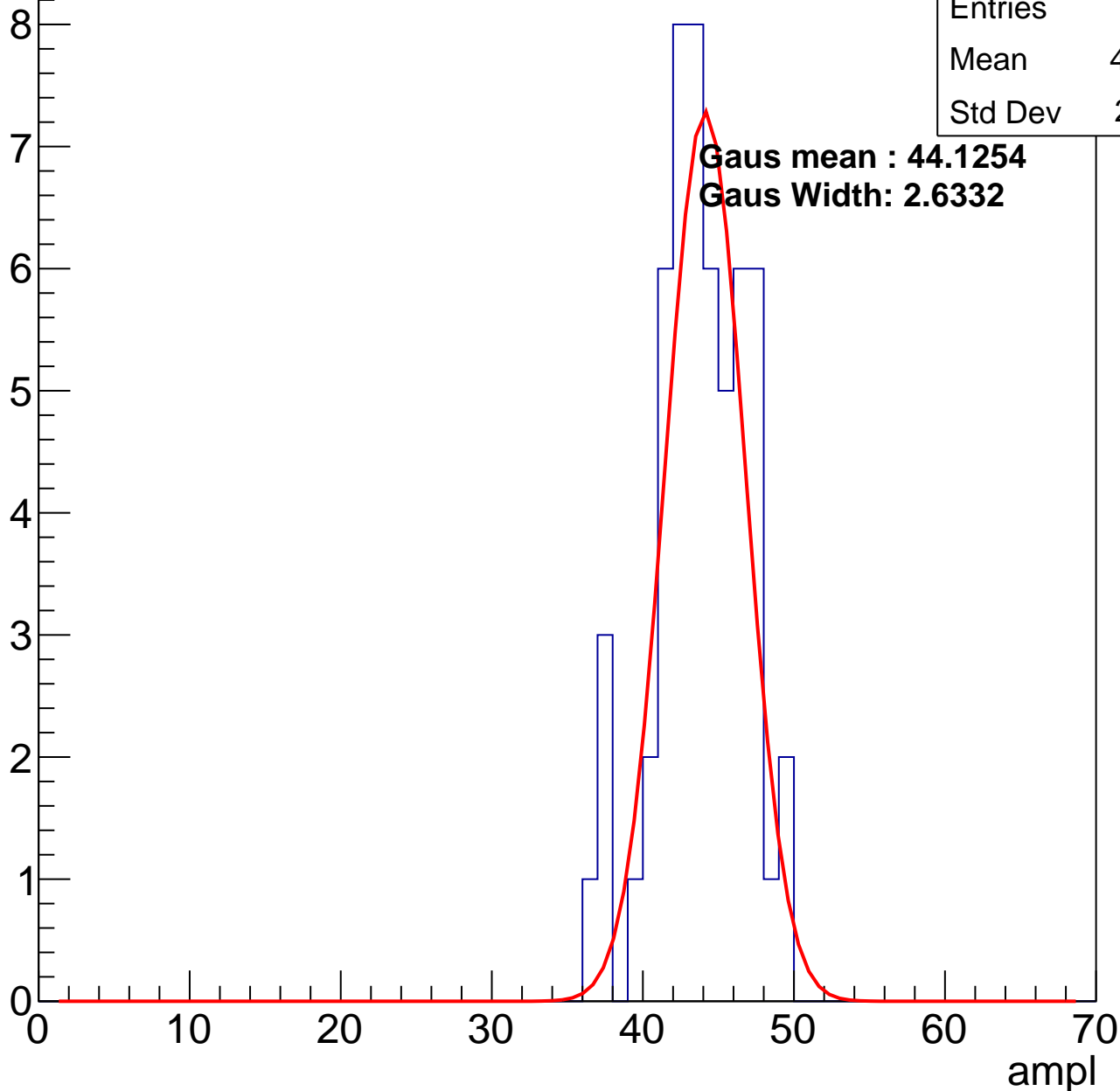
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	43.36
Std Dev	2.981

**Gaus mean : 44.1254**

**Gaus Width: 2.6332**

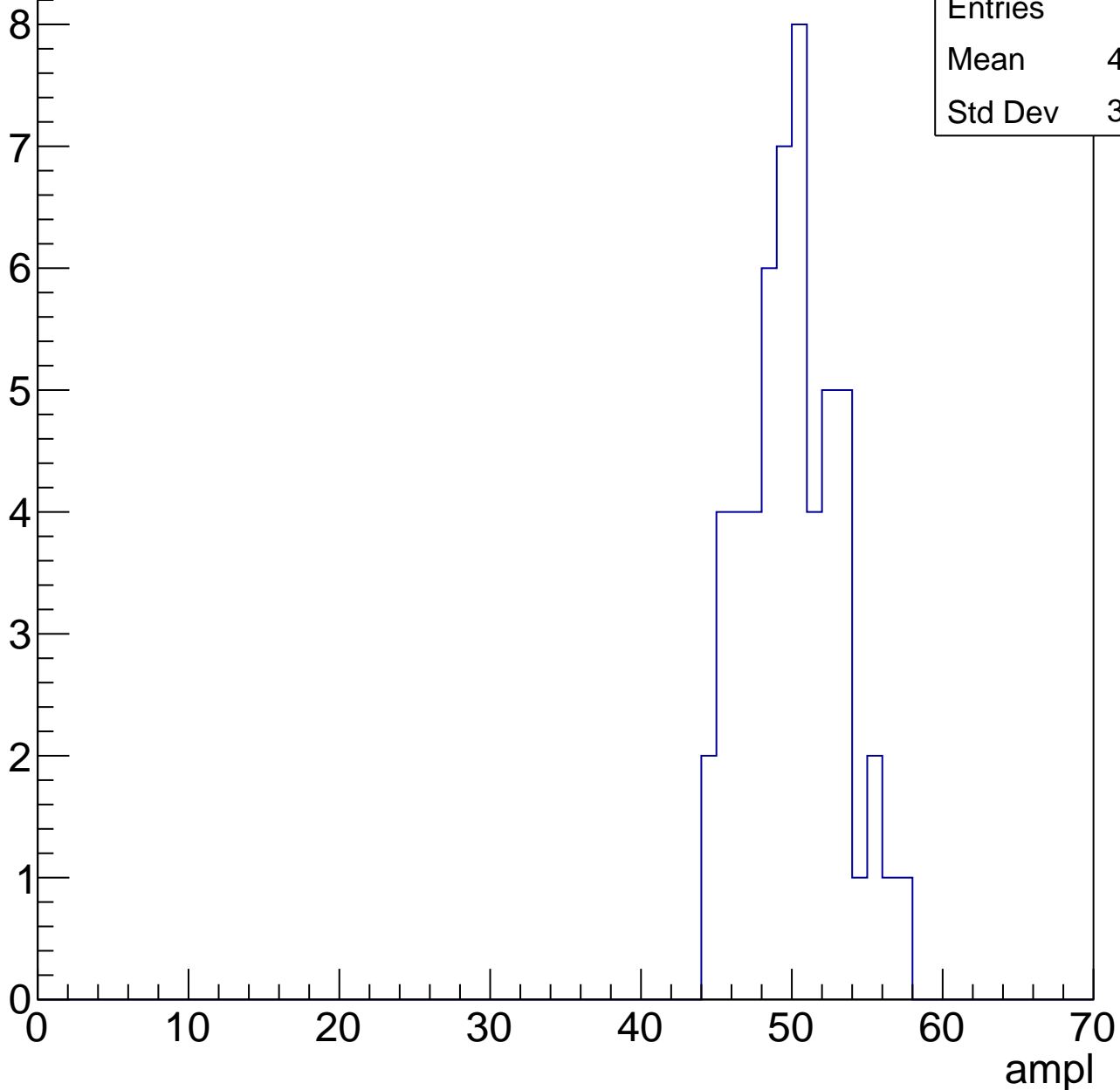


# B1L003S, U6-ch5, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

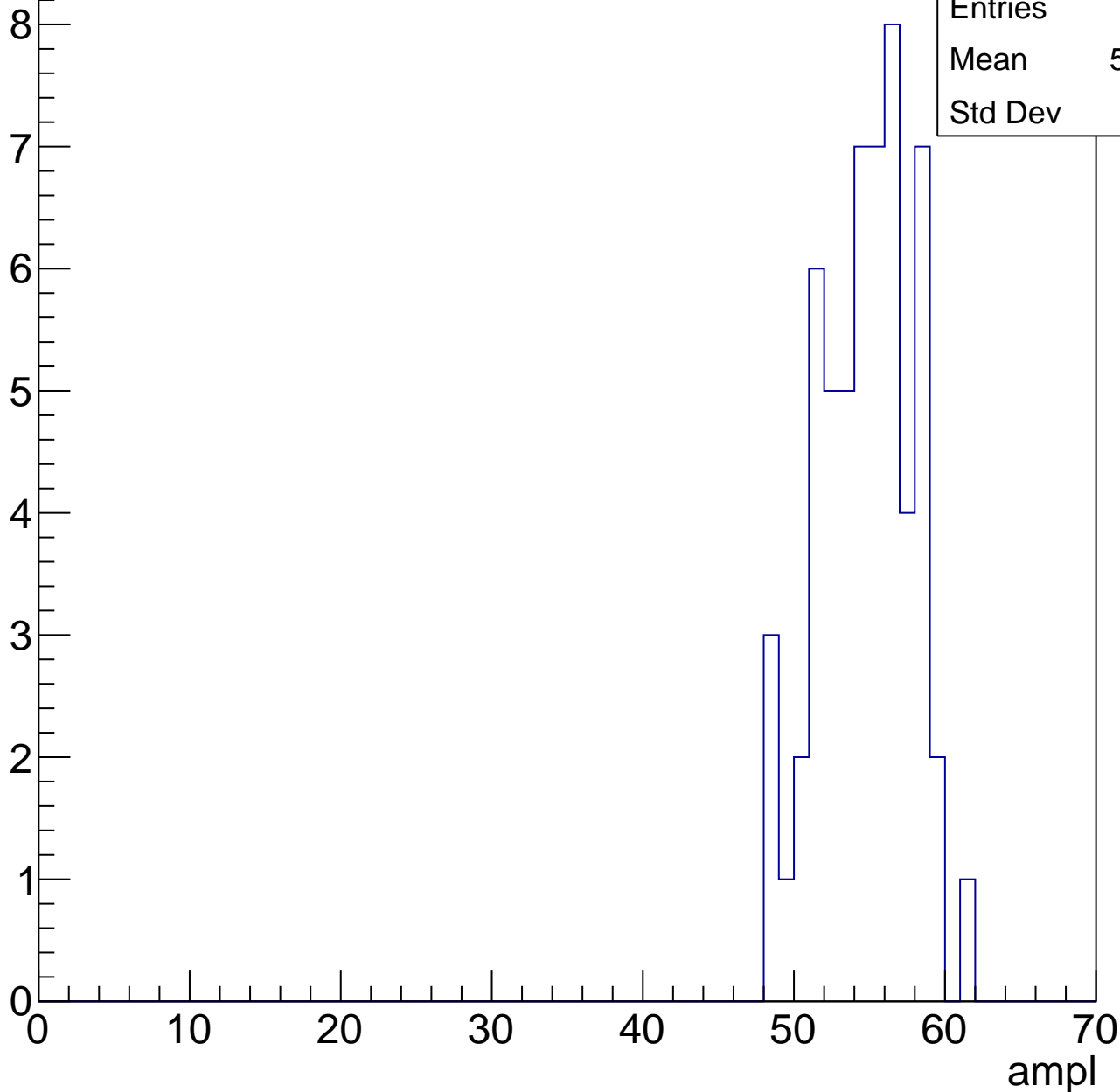
Entries	54
Mean	49.57
Std Dev	3.083



# B1L003S, U6-ch5, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

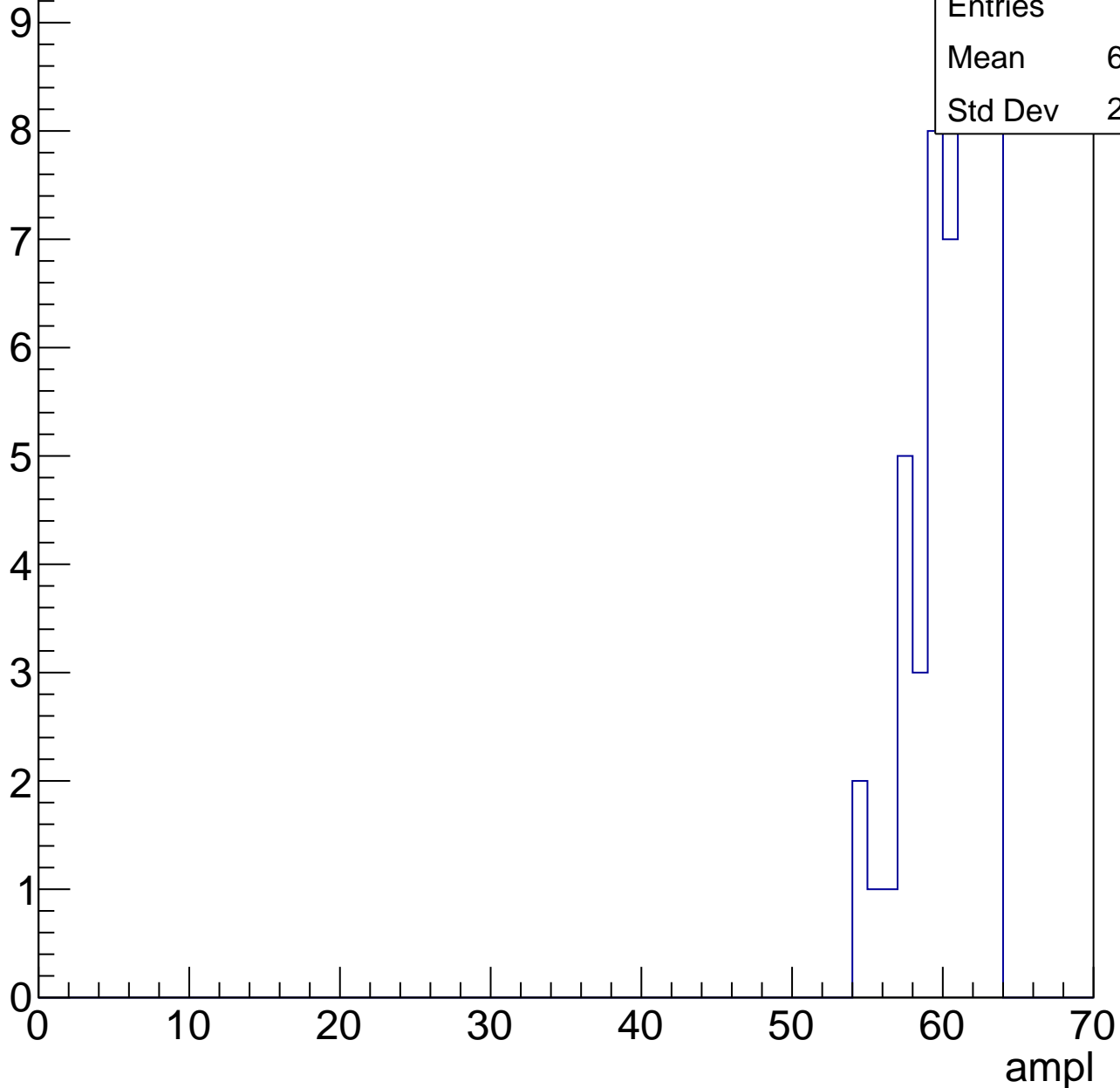


Entries	58
Mean	54.28
Std Dev	3.01

# B1L003S, U6-ch5, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

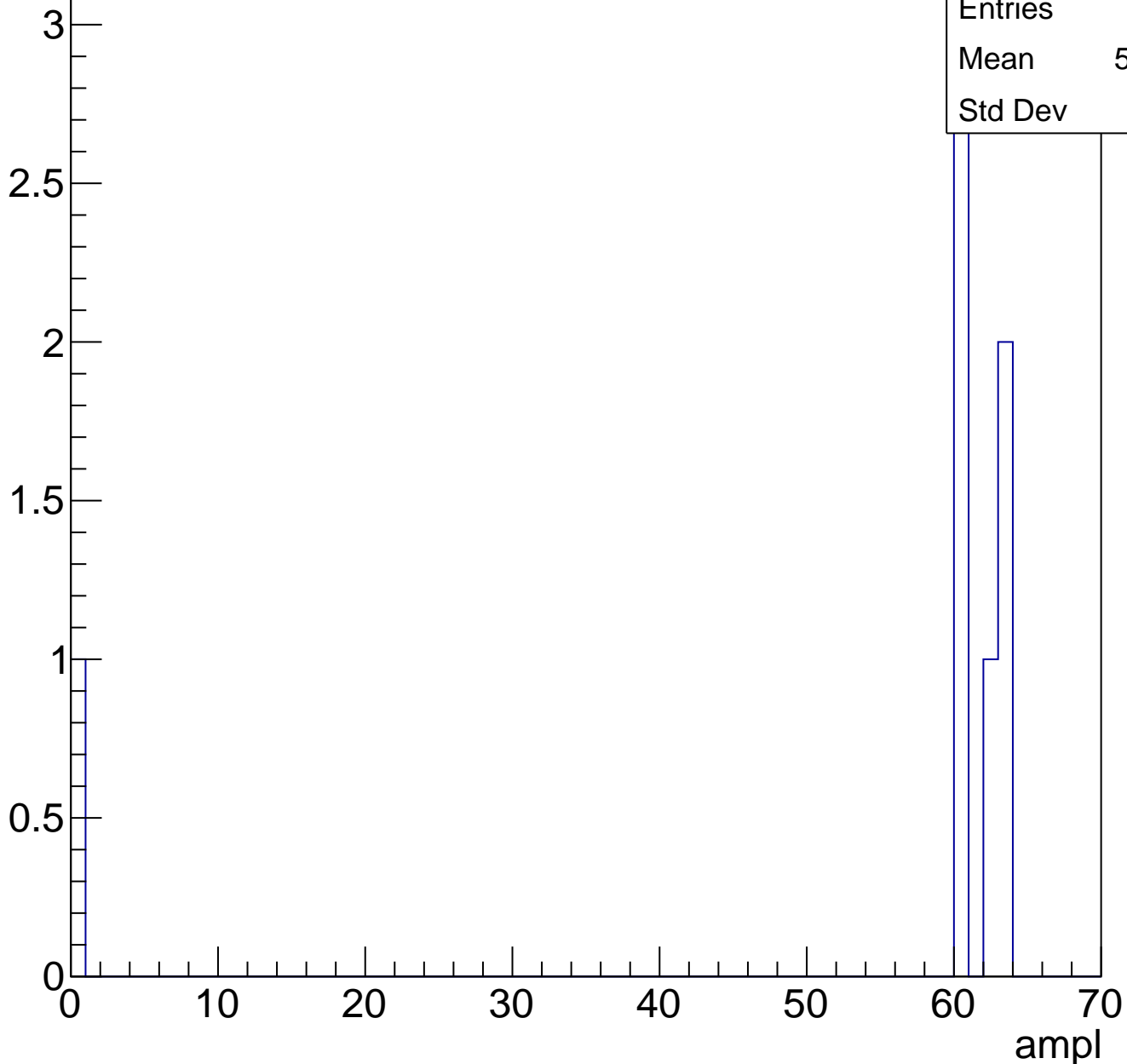
Entry



# B1L003S, U6-ch5, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



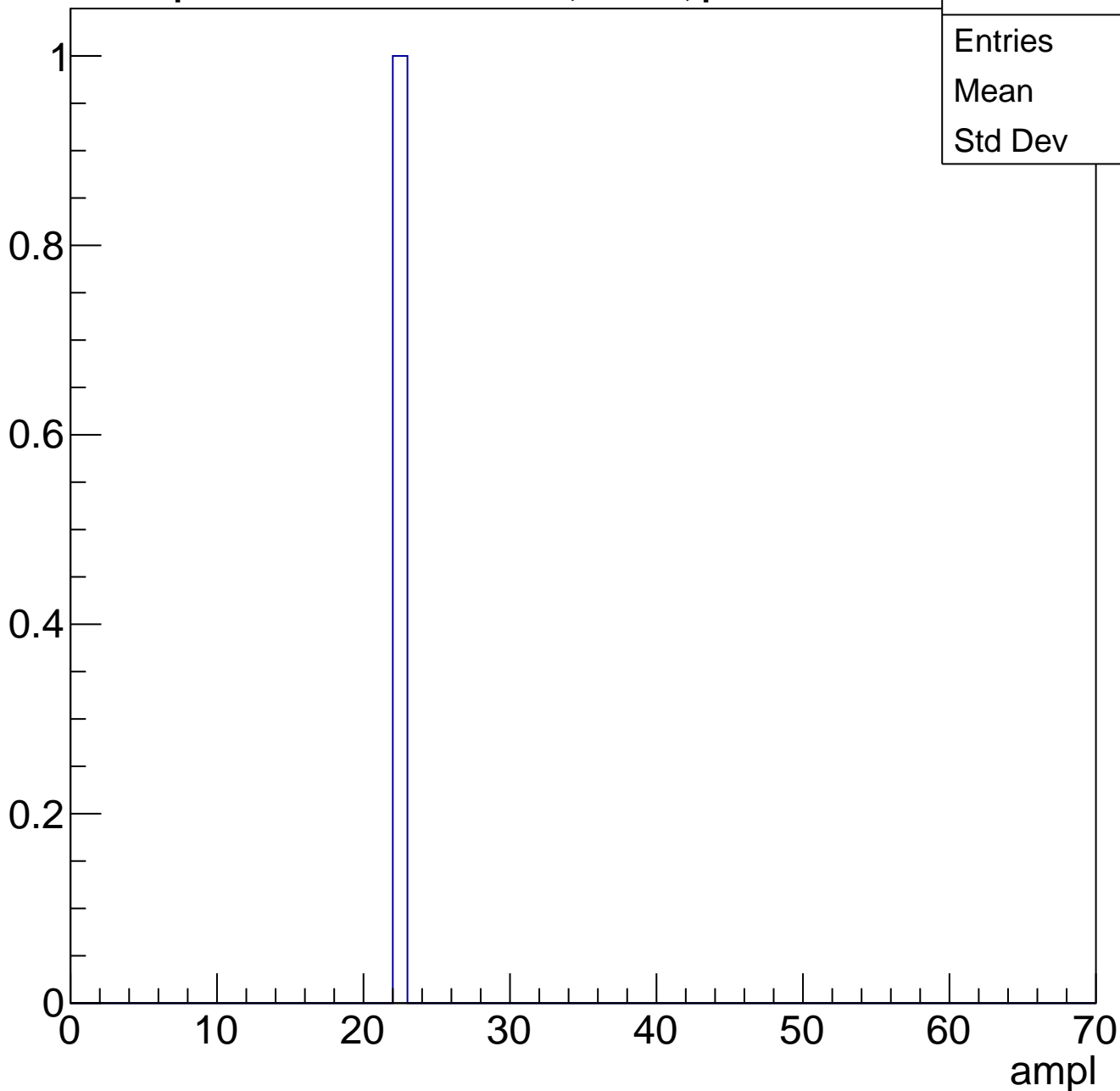
Entries	7
Mean	52.57
Std Dev	21.5



# B1L003S, U6-ch5, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch6, adc0

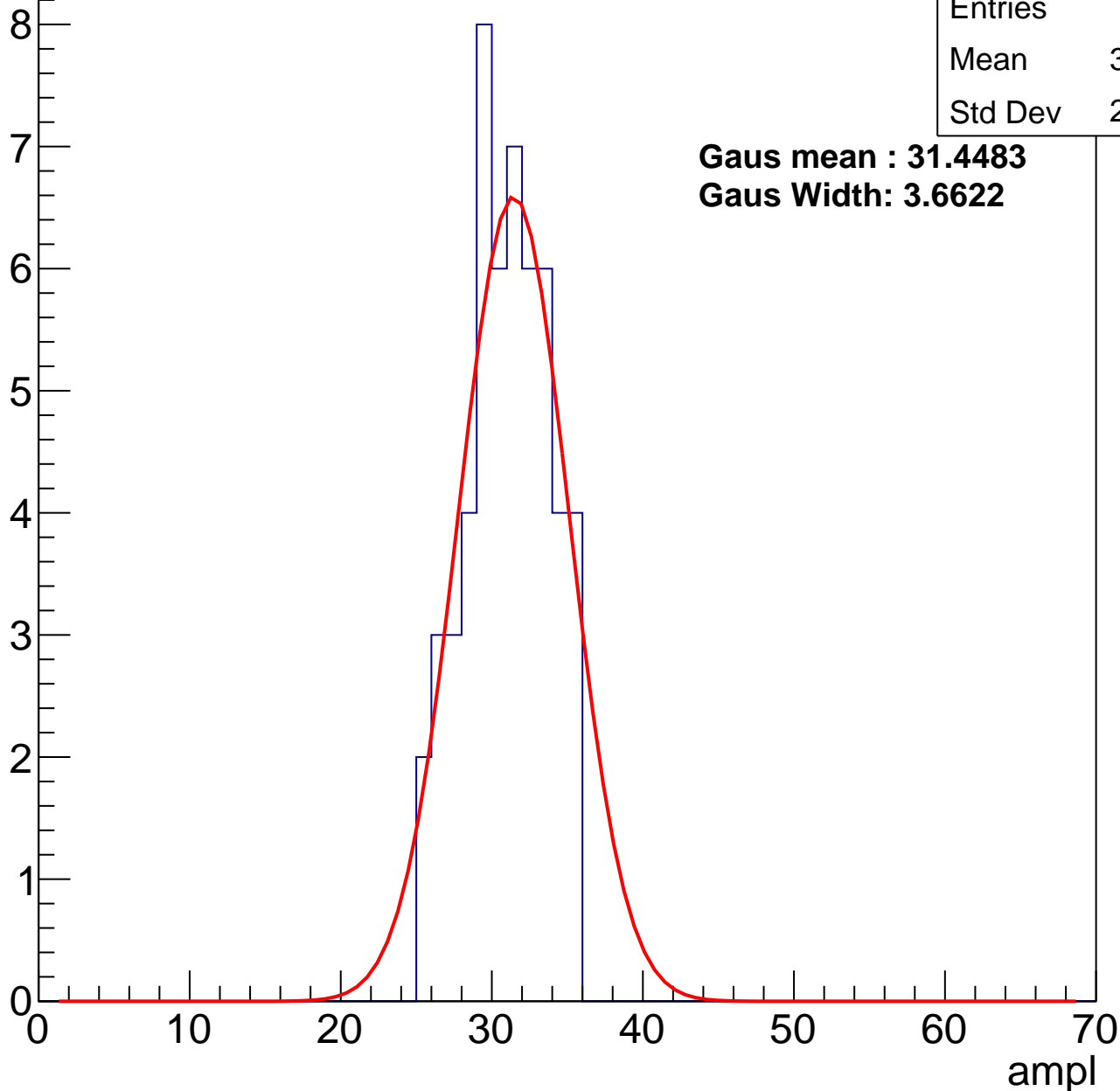
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	30.49
Std Dev	2.696

**Gaus mean : 31.4483**

**Gaus Width: 3.6622**



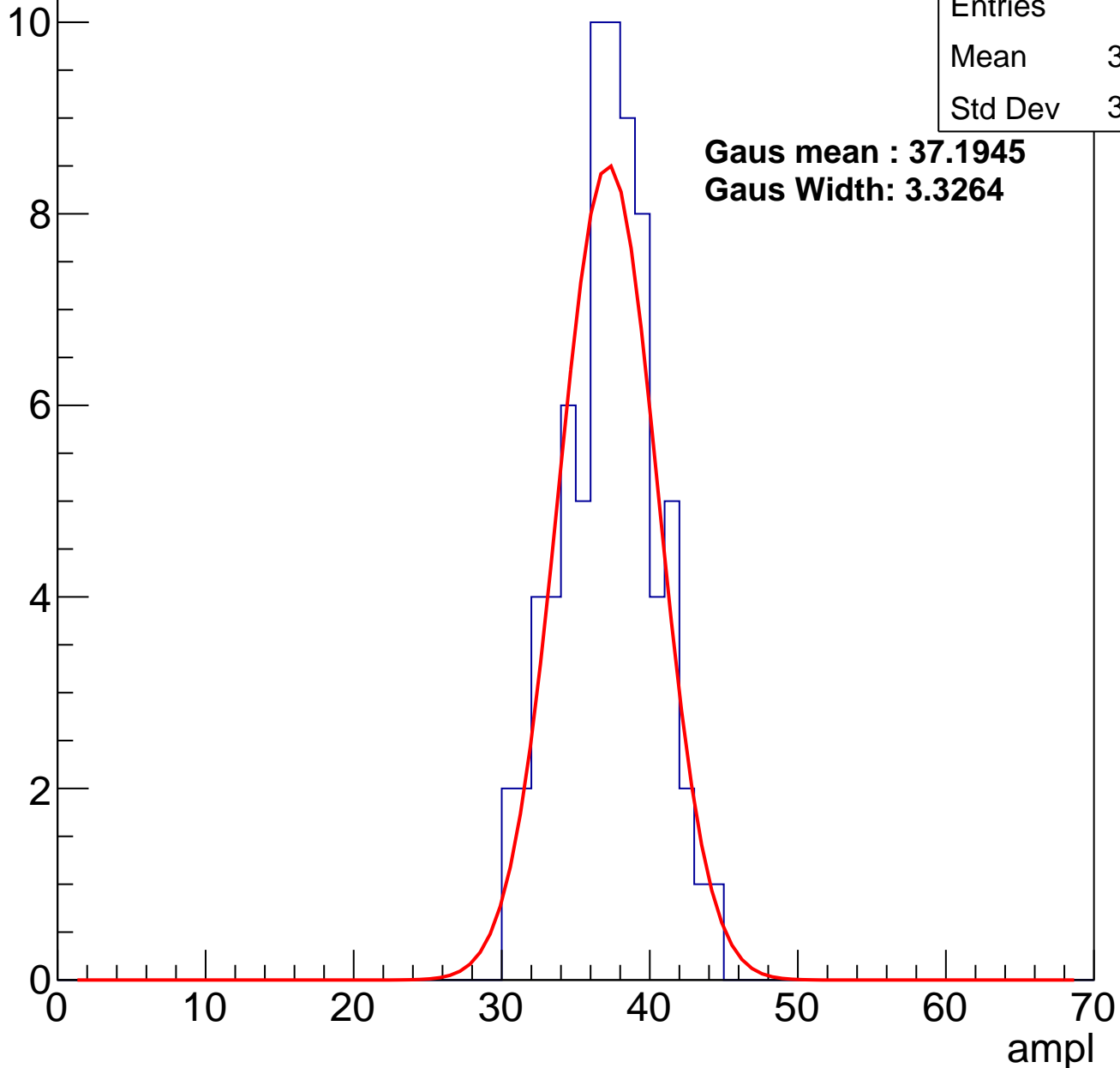
# B1L003S, U6-ch6, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	73
Mean	36.73
Std Dev	3.107

**Gaus mean : 37.1945**  
**Gaus Width: 3.3264**

Entry



# B1L003S, U6-ch6, adc2

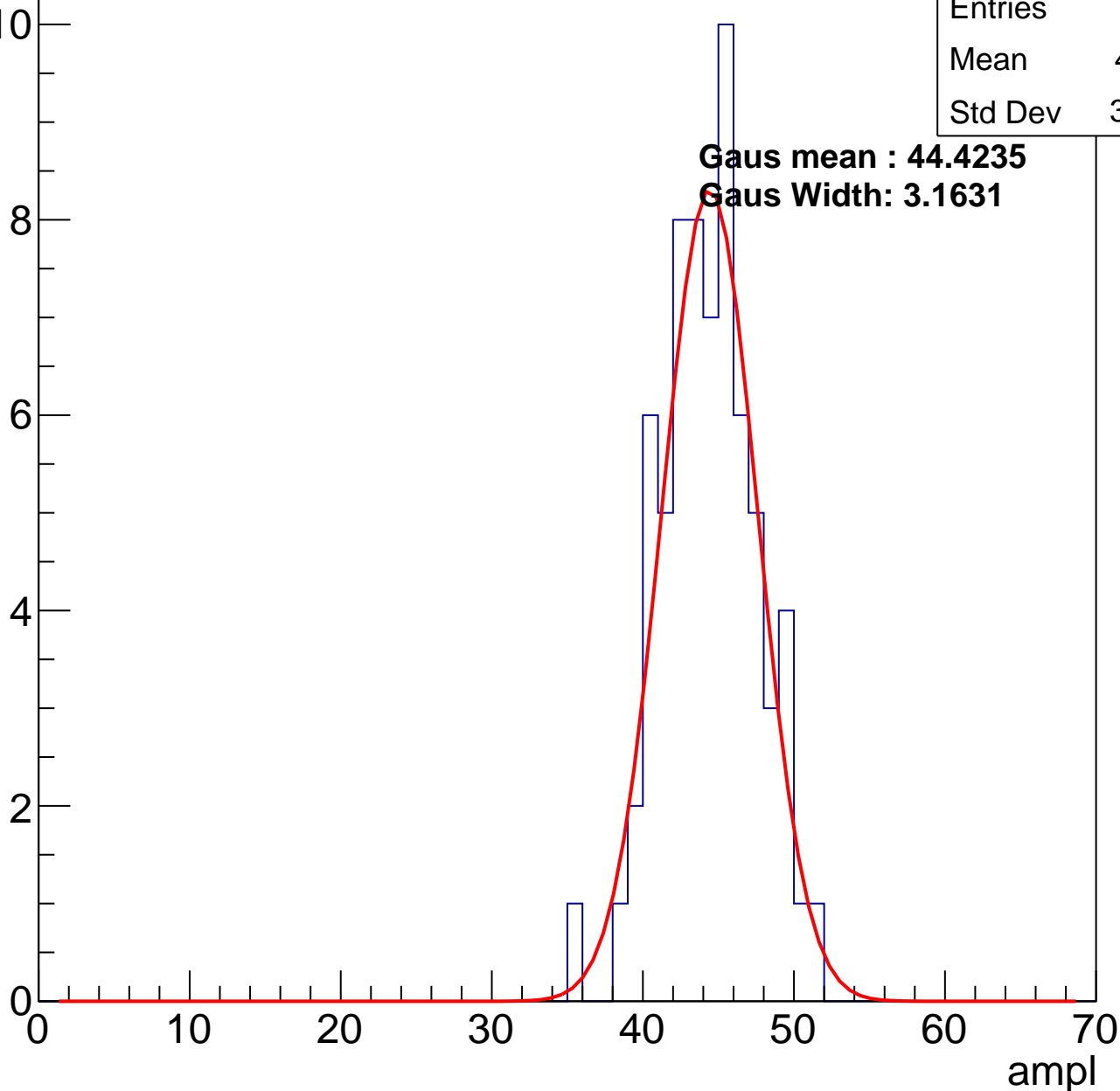
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	68
Mean	43.91
Std Dev	3.114

**Gaus mean : 44.4235**

**Gaus Width: 3.1631**

Entry

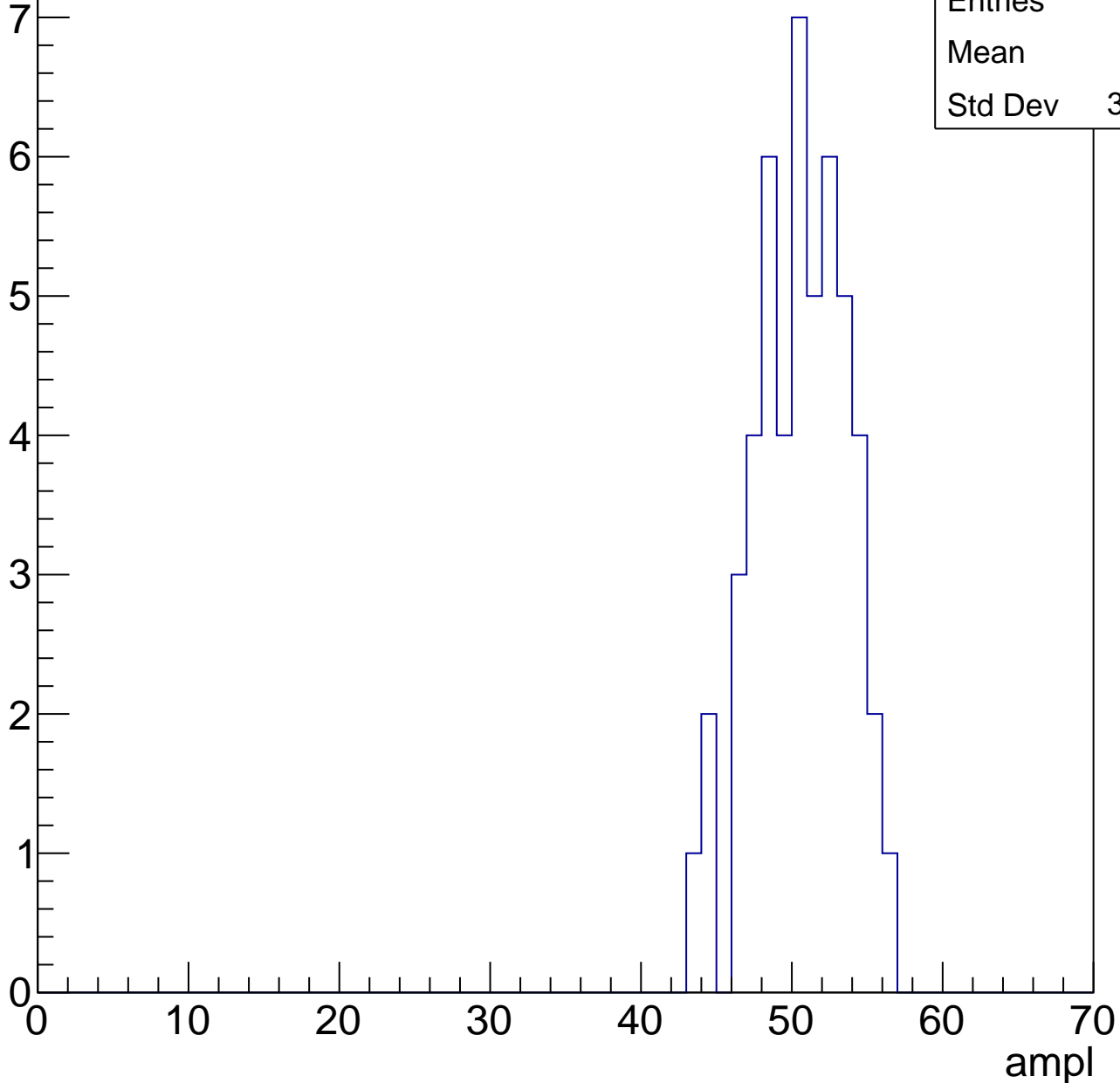


# B1L003S, U6-ch6, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	50
Mean	50.1
Std Dev	3.022

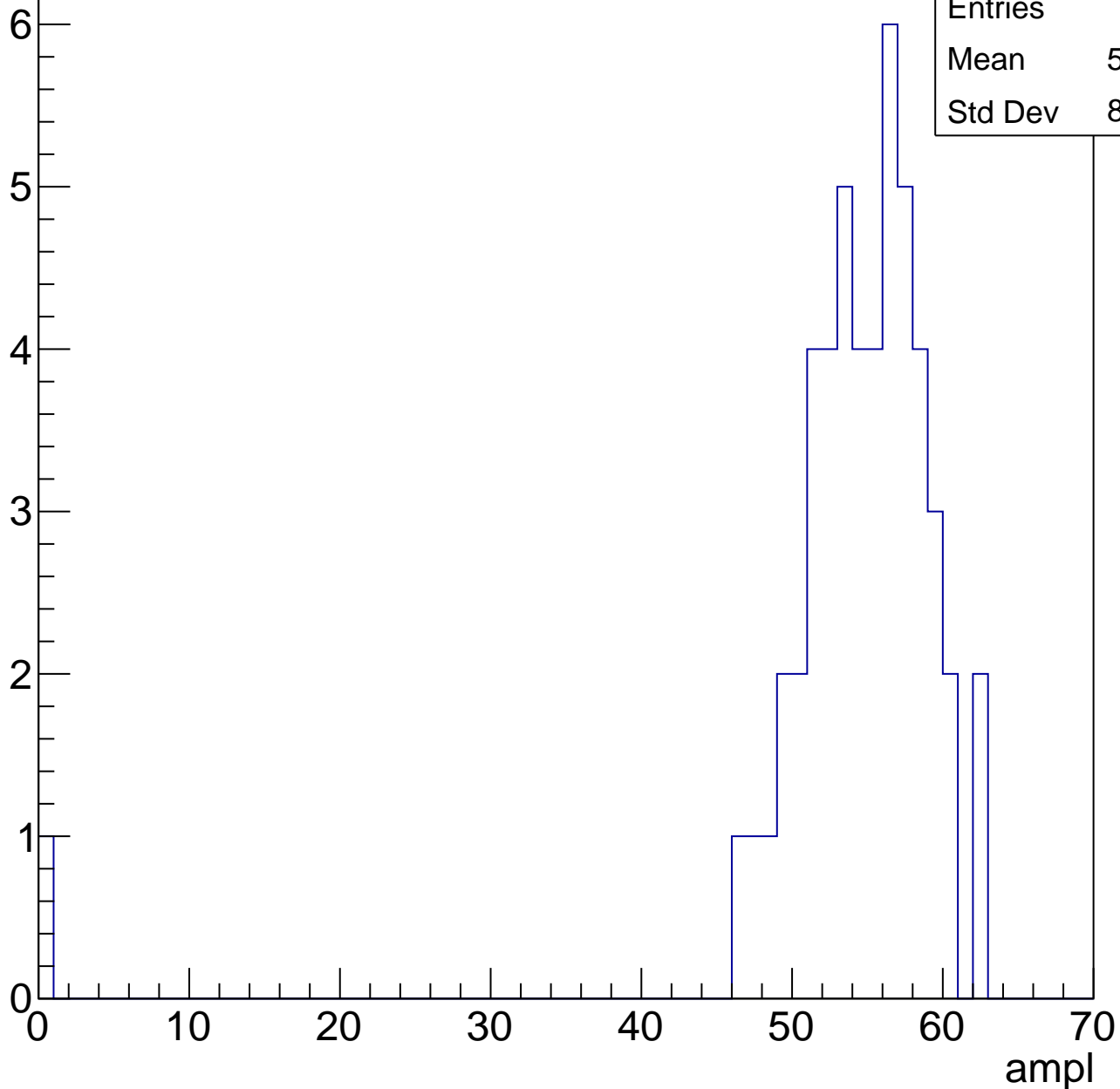


# B1L003S, U6-ch6, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

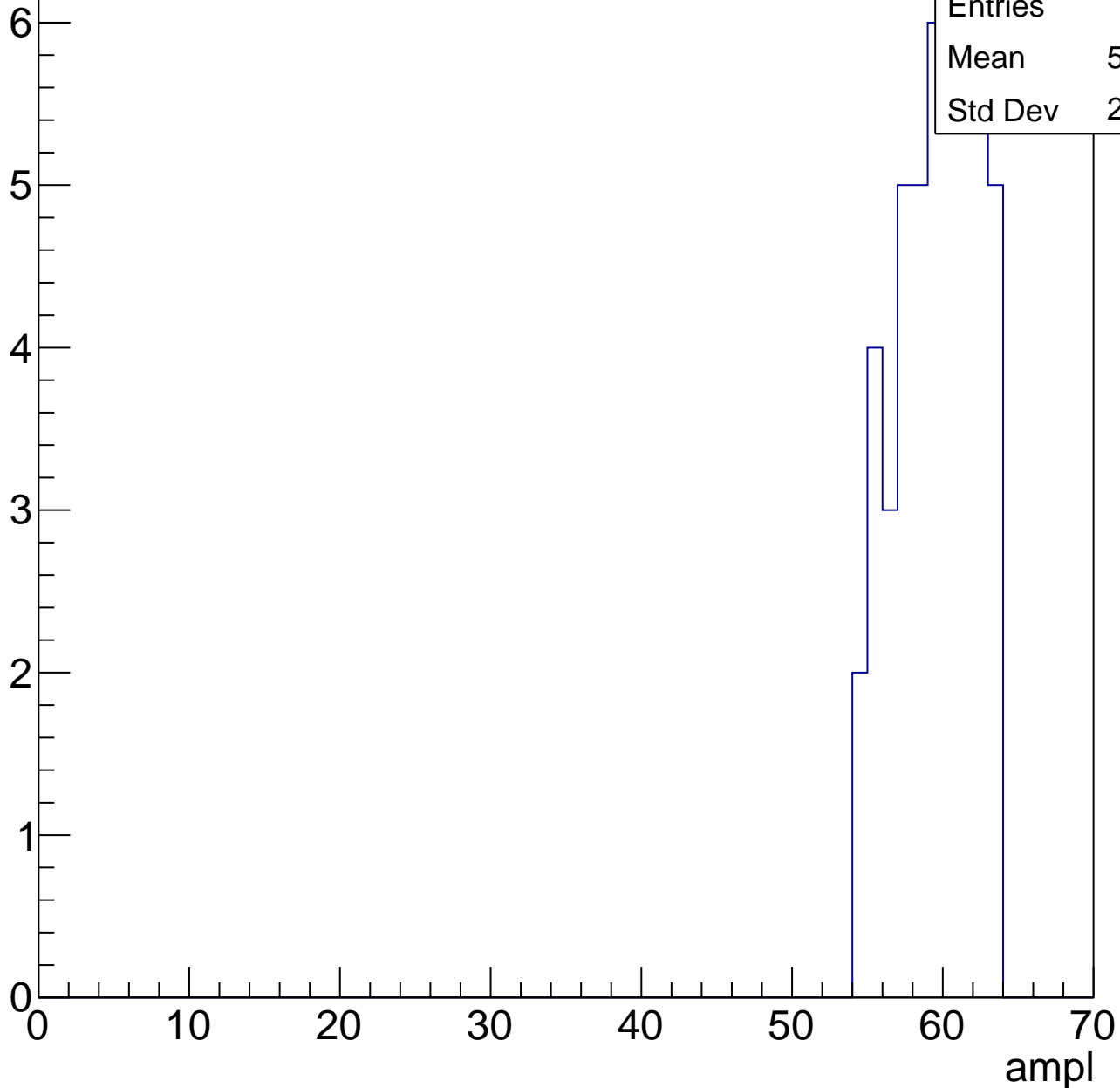
Entries	51
Mean	53.45
Std Dev	8.402



# B1L003S, U6-ch6, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



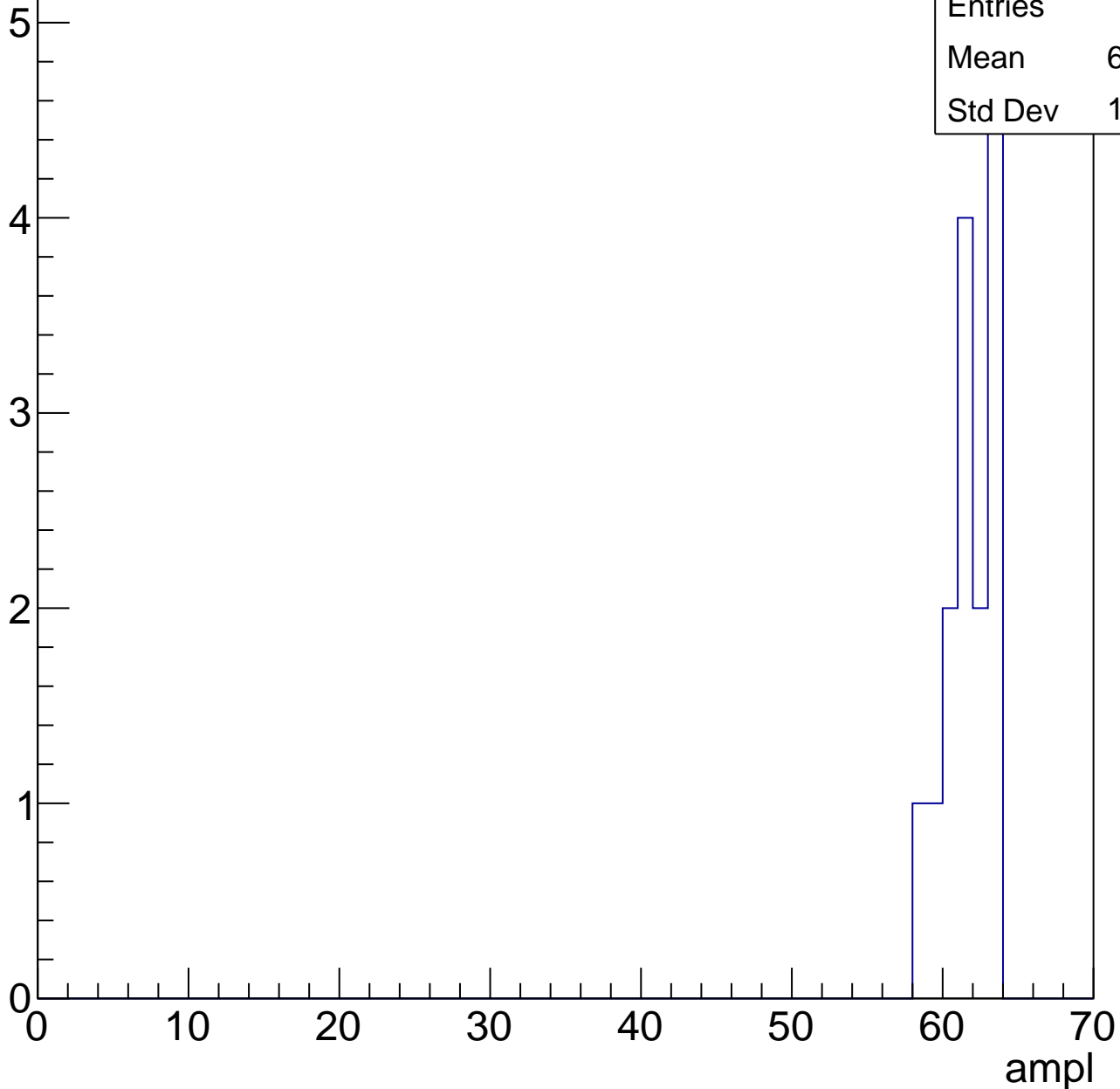
Entries	48
Mean	59.12
Std Dev	2.619

# B1L003S, U6-ch6, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	15
Mean	61.33
Std Dev	1.535





# B1L003S, U6-ch6, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U6-ch7, adc0

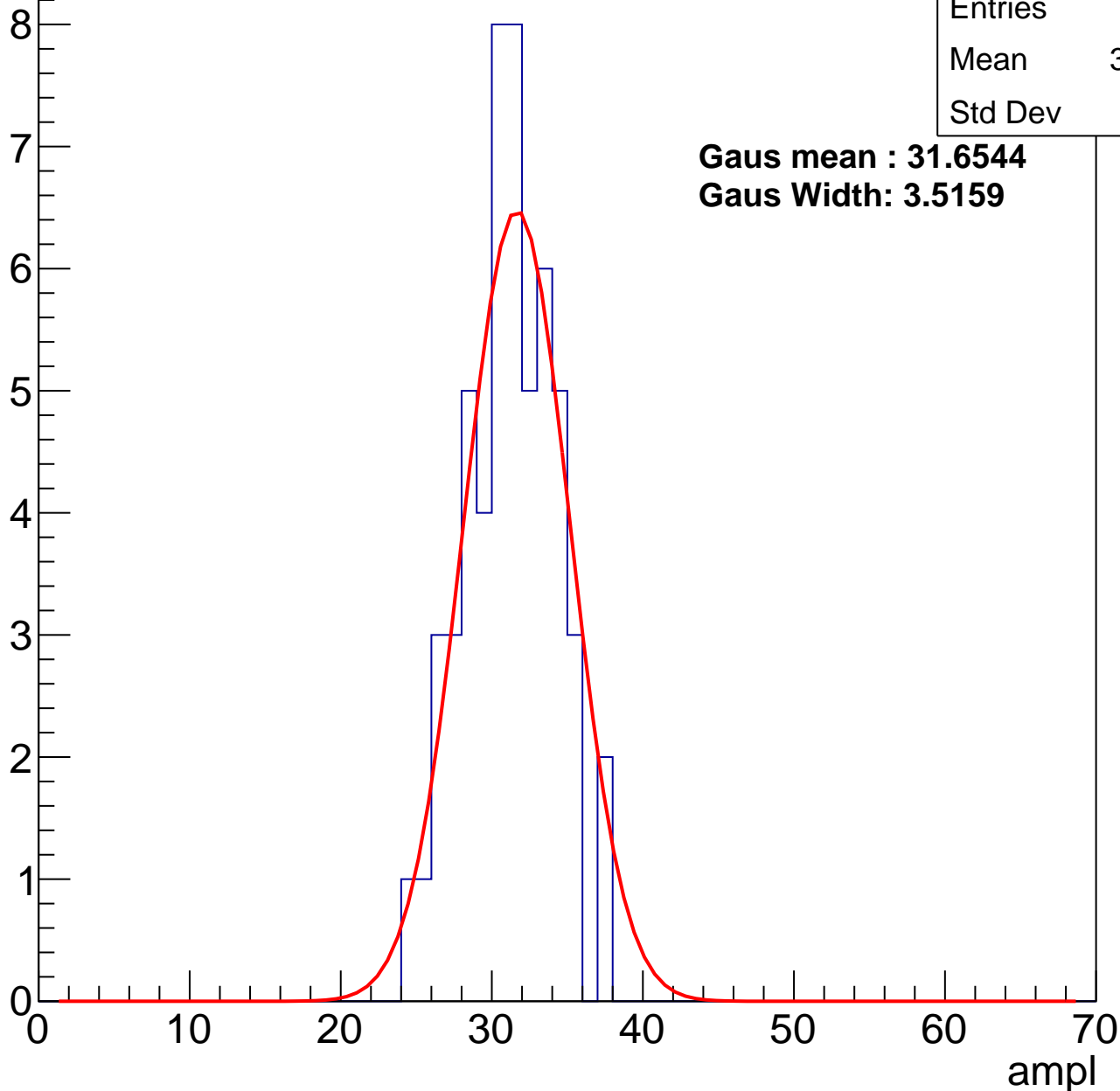
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	54
Mean	30.72
Std Dev	2.94

**Gaus mean : 31.6544**

**Gaus Width: 3.5159**



# B1L003S, U6-ch7, adc1

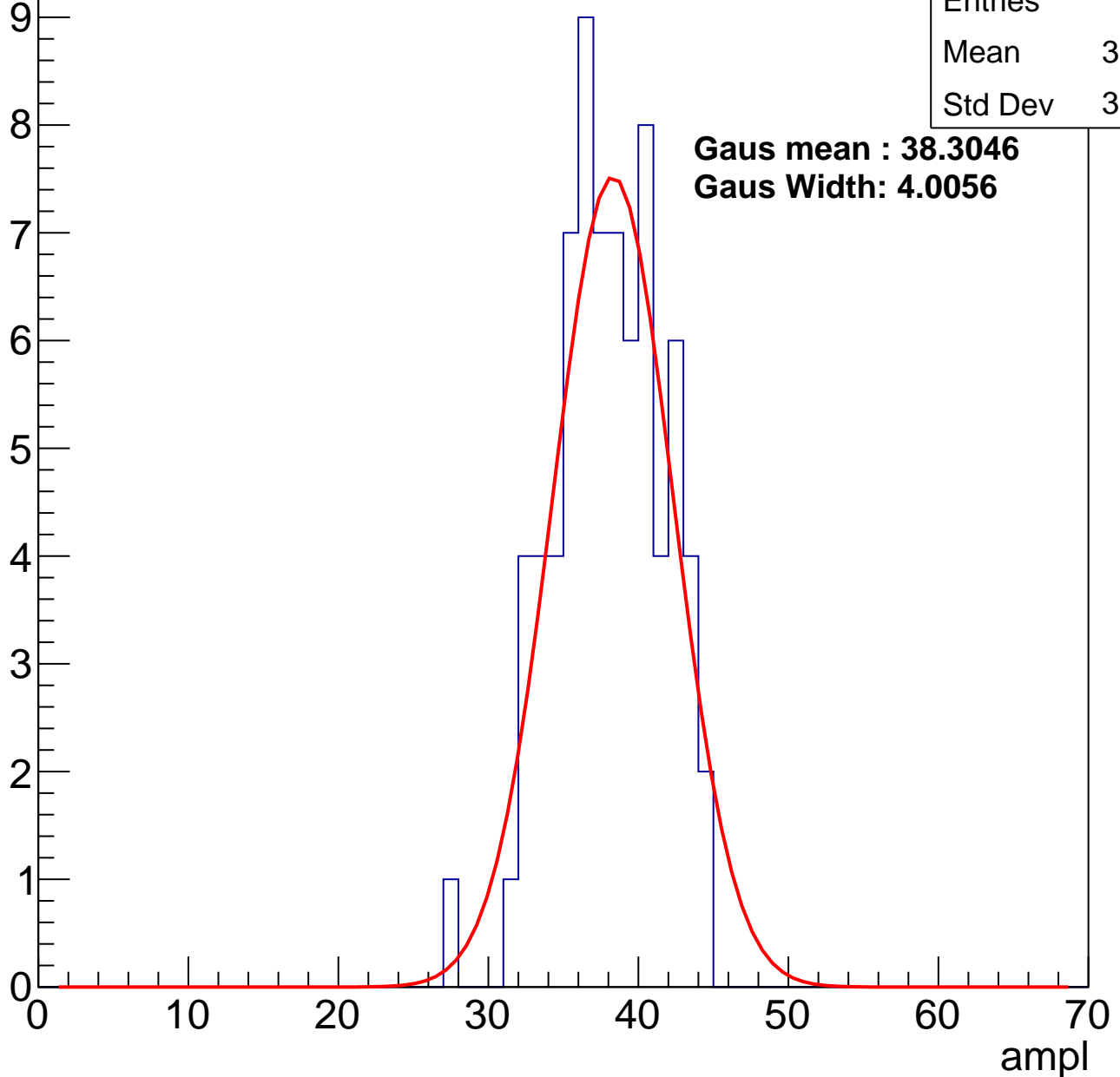
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	74
Mean	37.54
Std Dev	3.507

**Gaus mean : 38.3046**

**Gaus Width: 4.0056**



# B1L003S, U6-ch7, adc2

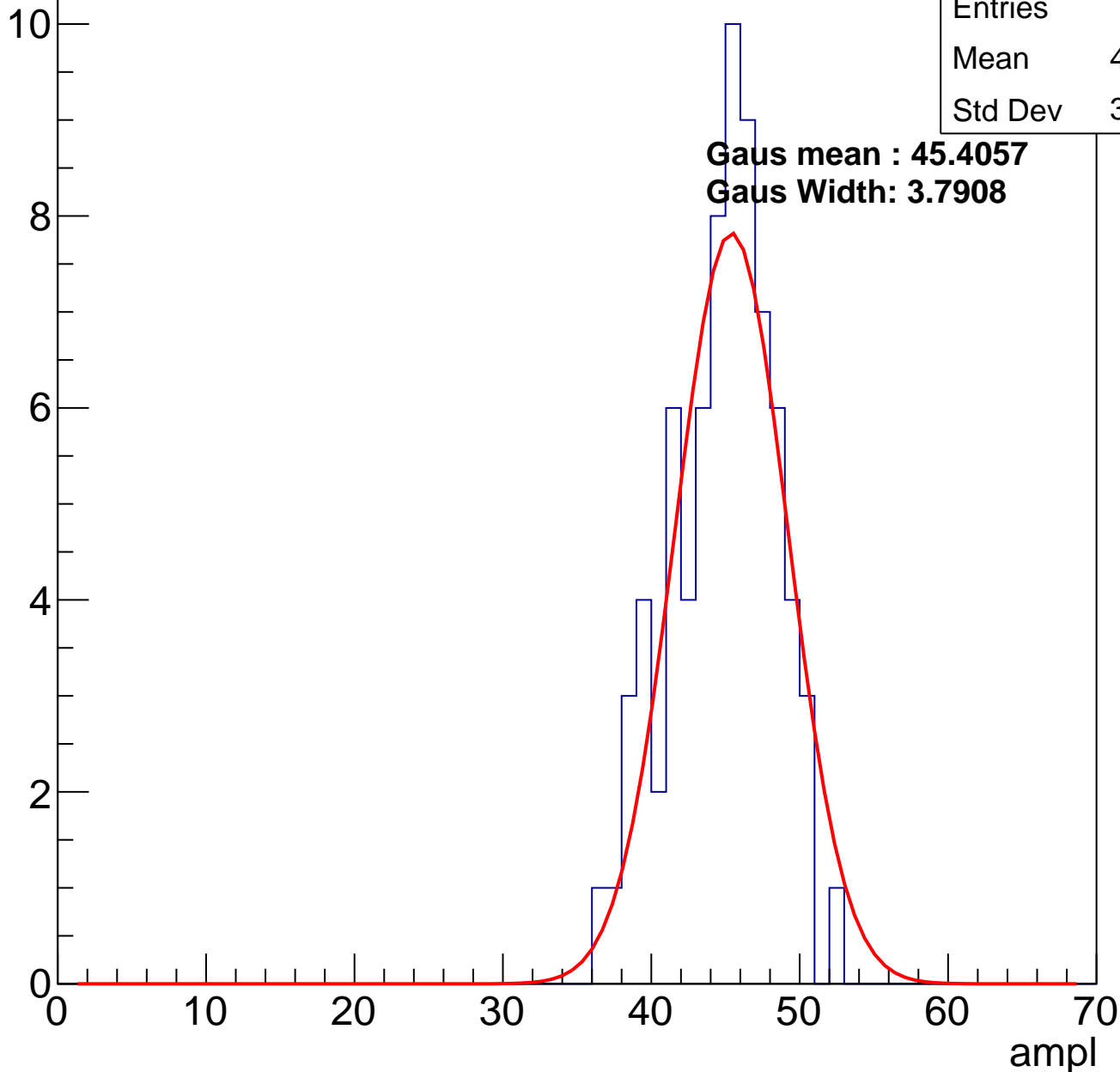
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	75
Mean	44.35
Std Dev	3.458

**Gaus mean : 45.4057**

**Gaus Width: 3.7908**

Entry

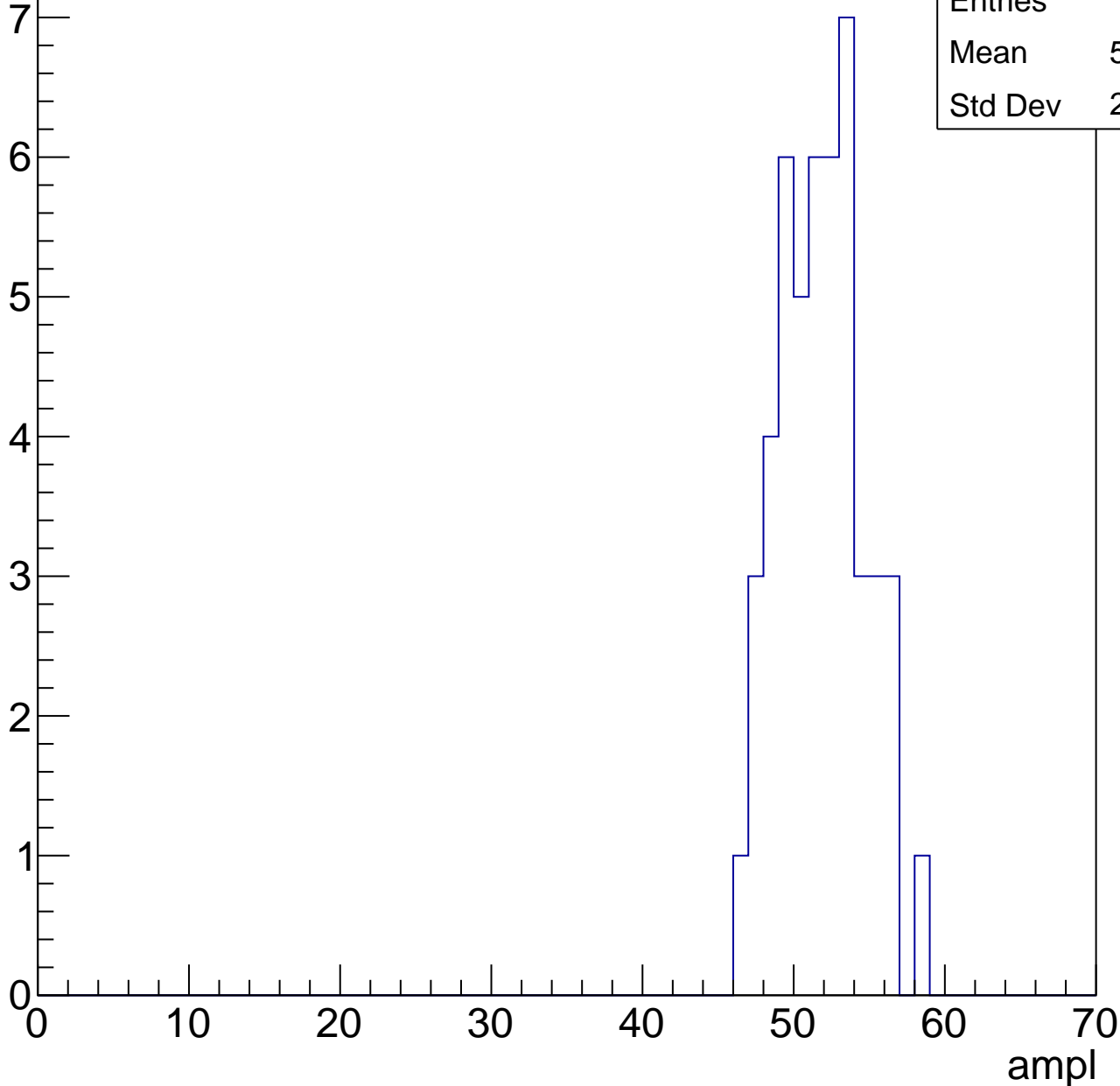


# B1L003S, U6-ch7, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

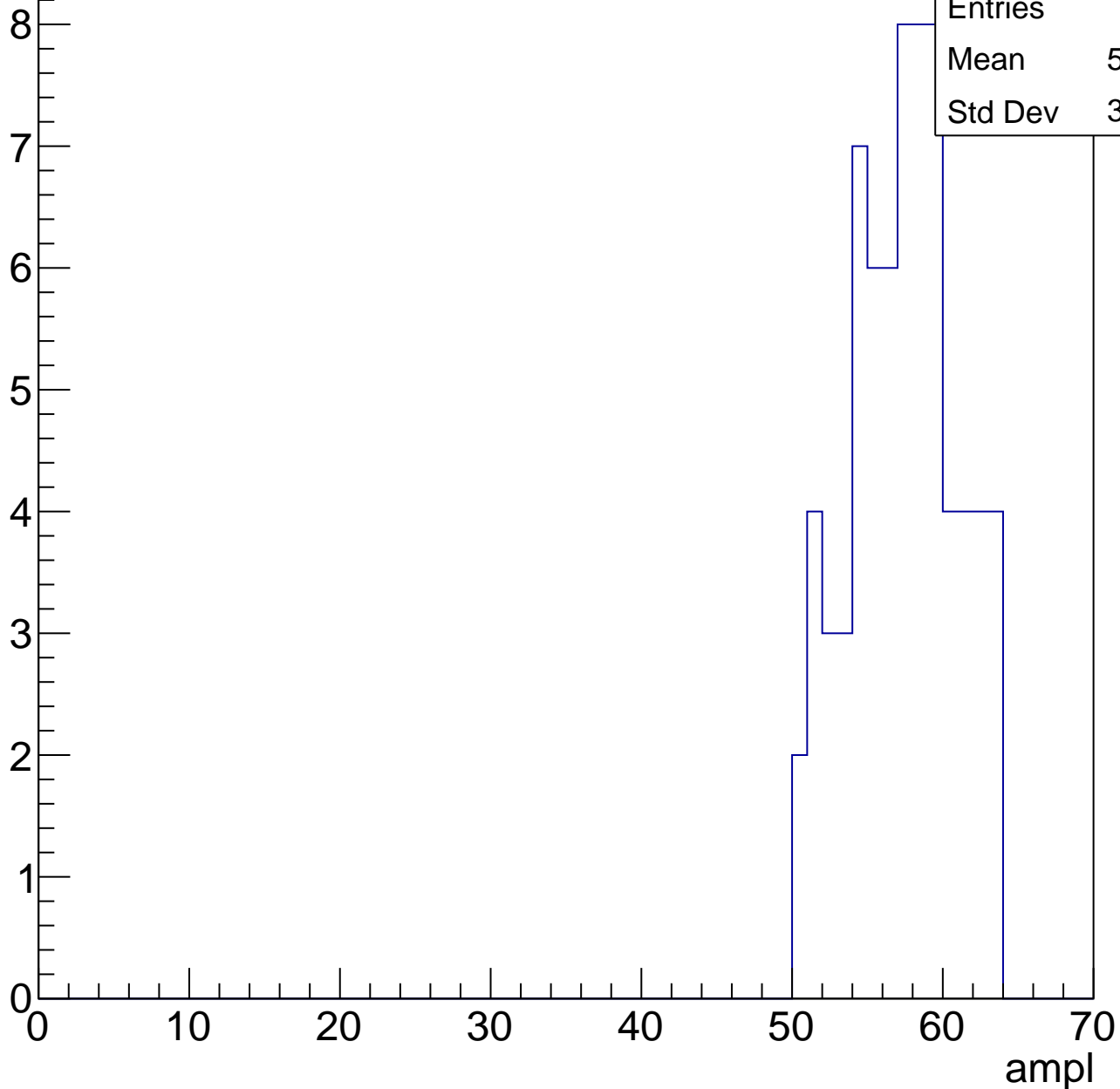
Entries	48
Mean	51.35
Std Dev	2.757



# B1L003S, U6-ch7, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

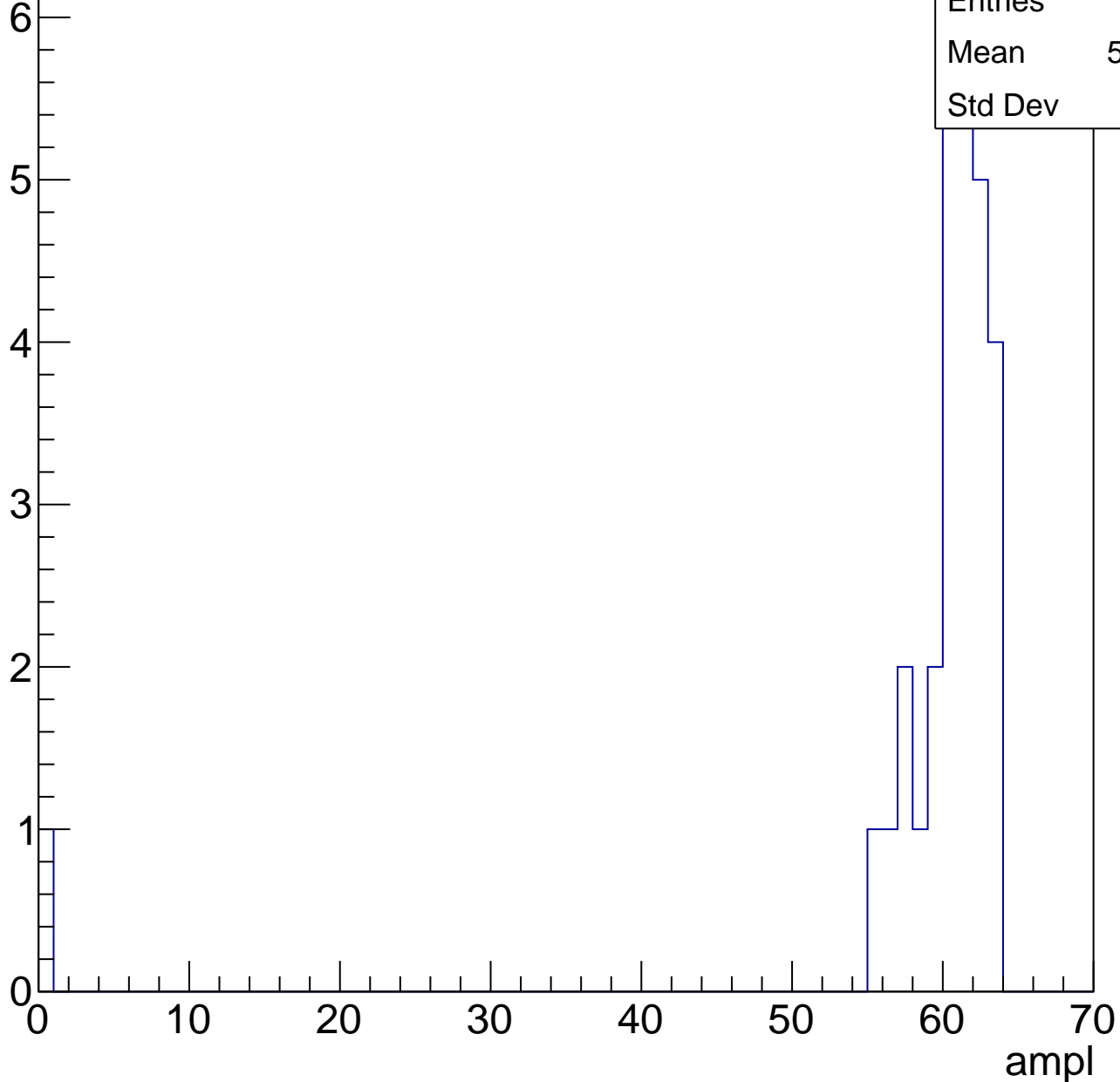
Entry



# B1L003S, U6-ch7, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch7, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

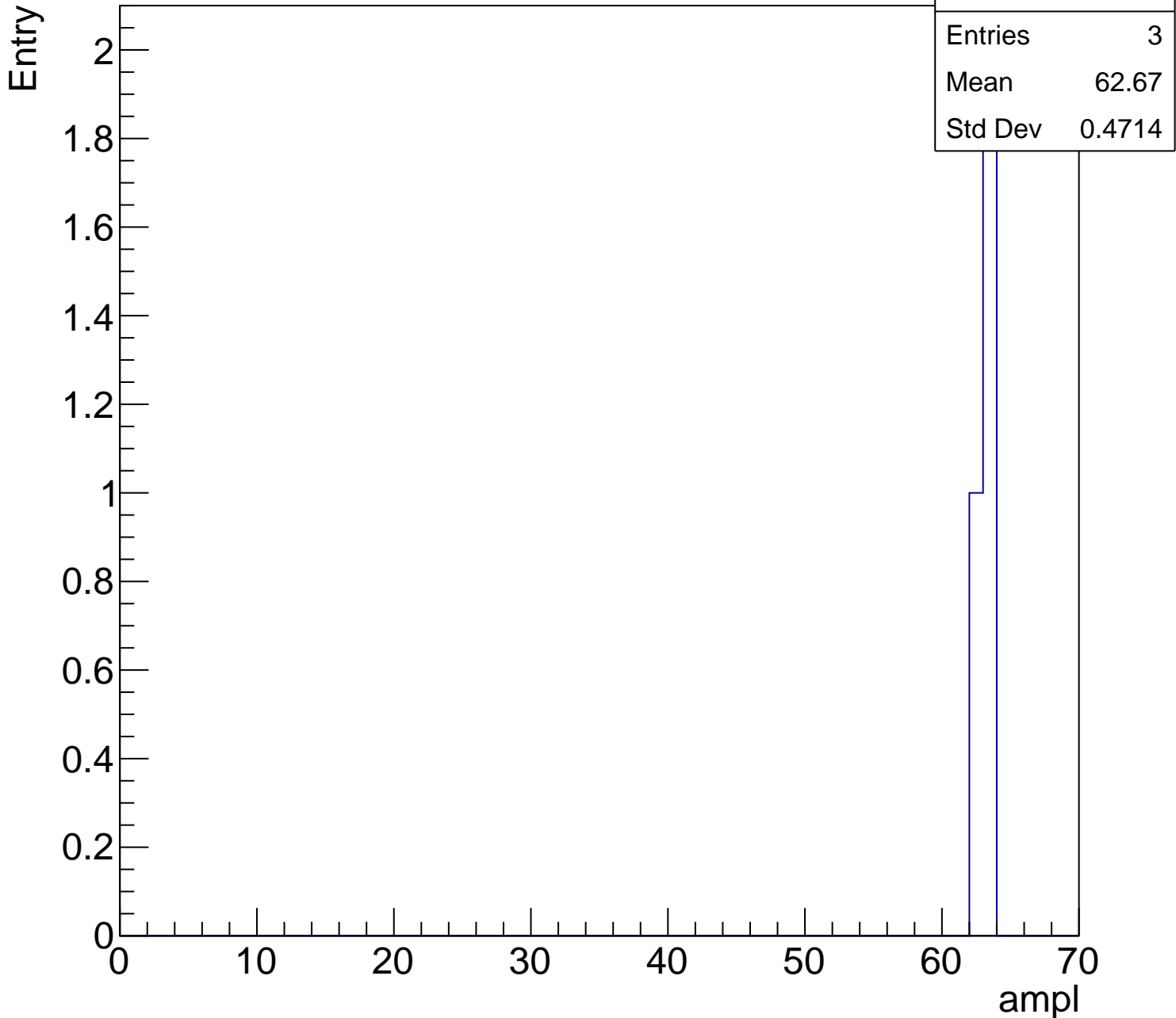
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.67
Std Dev	0.4714

0 10 20 30 40 50 60 70

ampl





# B1L003S, U6-ch7, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch8, adc0

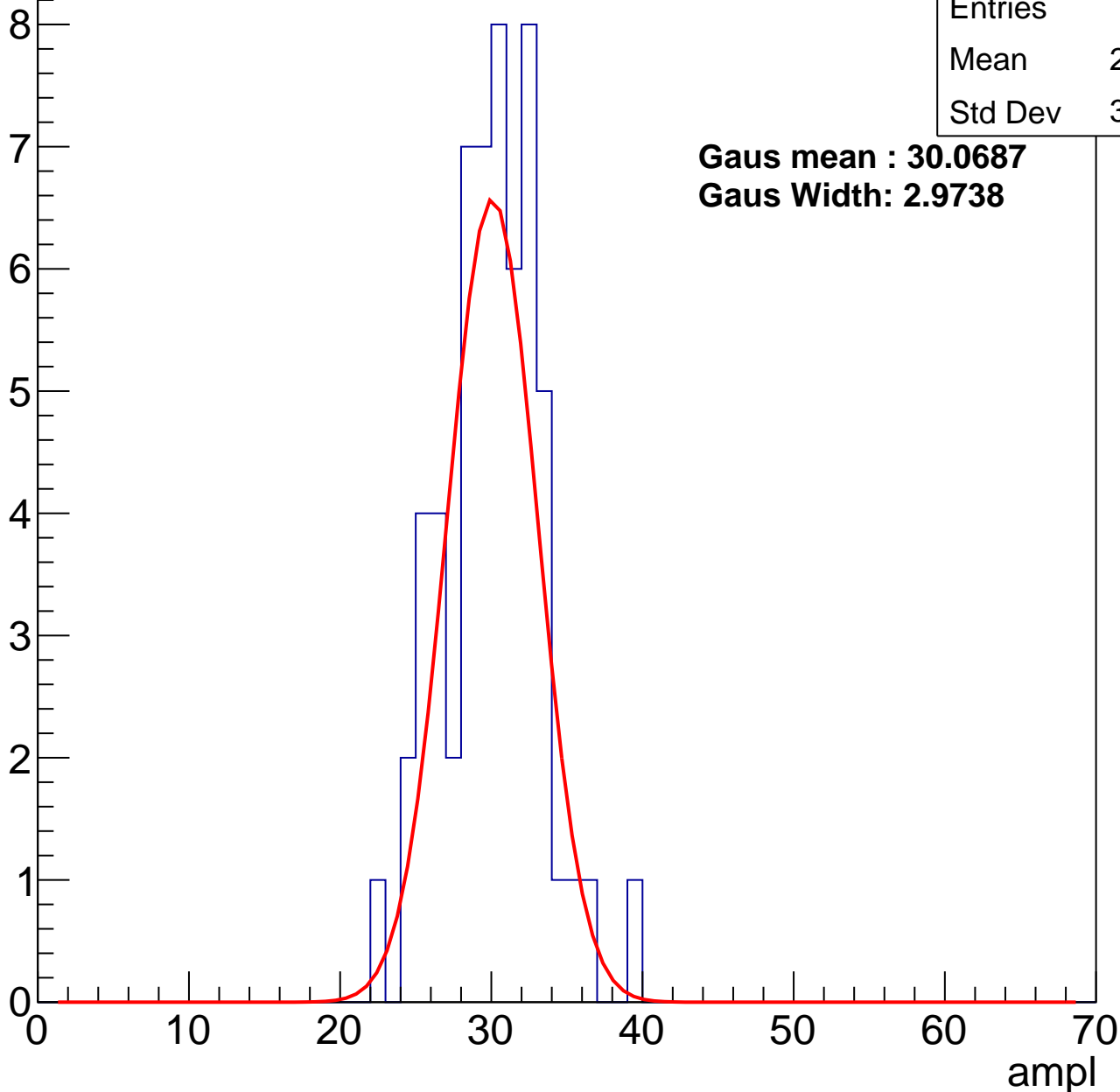
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	29.62
Std Dev	3.178

**Gaus mean : 30.0687**

**Gaus Width: 2.9738**



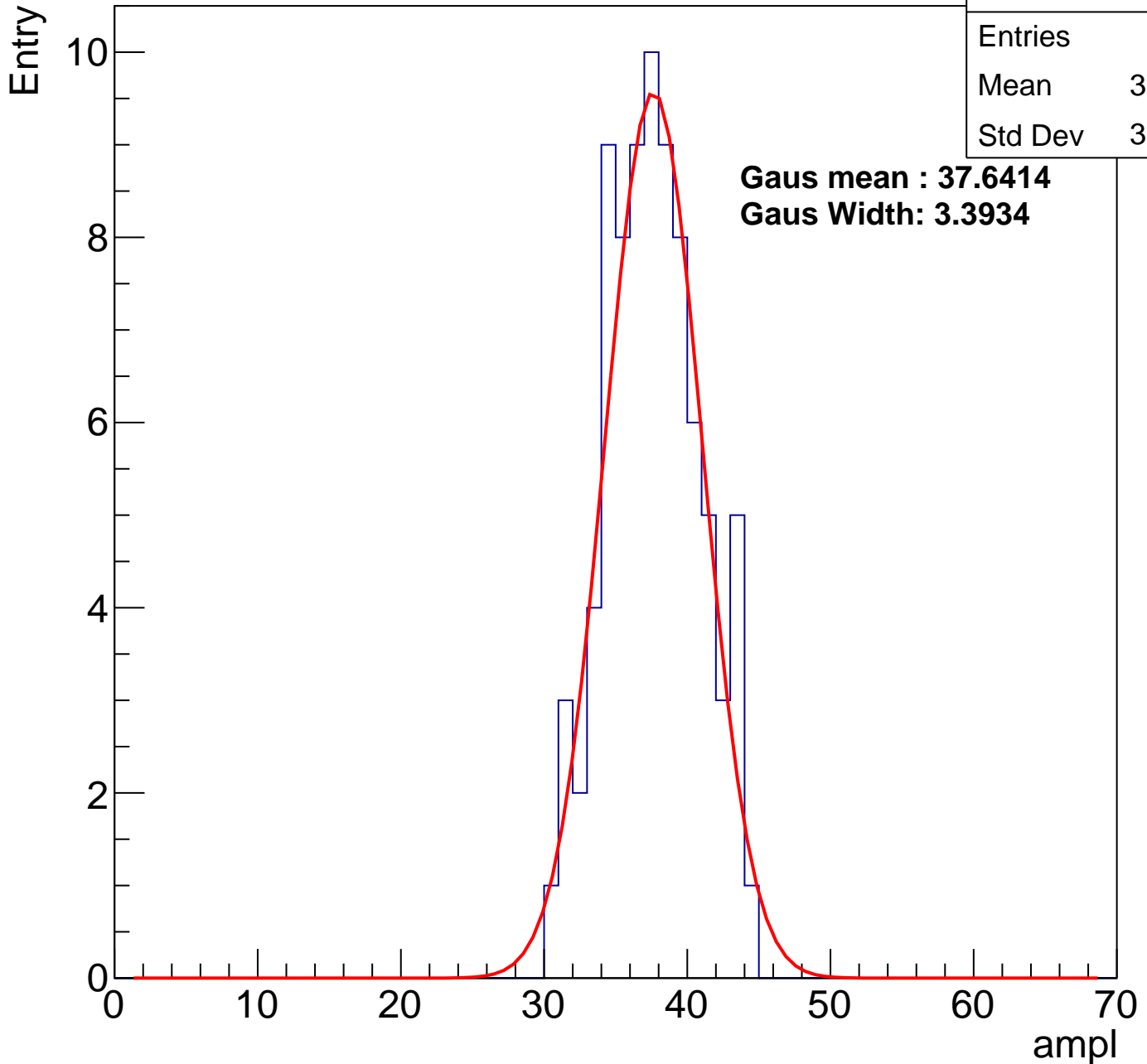
# B1L003S, U6-ch8, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	83
Mean	37.14
Std Dev	3.238

**Gaus mean : 37.6414**

**Gaus Width: 3.3934**



# B1L003S, U6-ch8, adc2

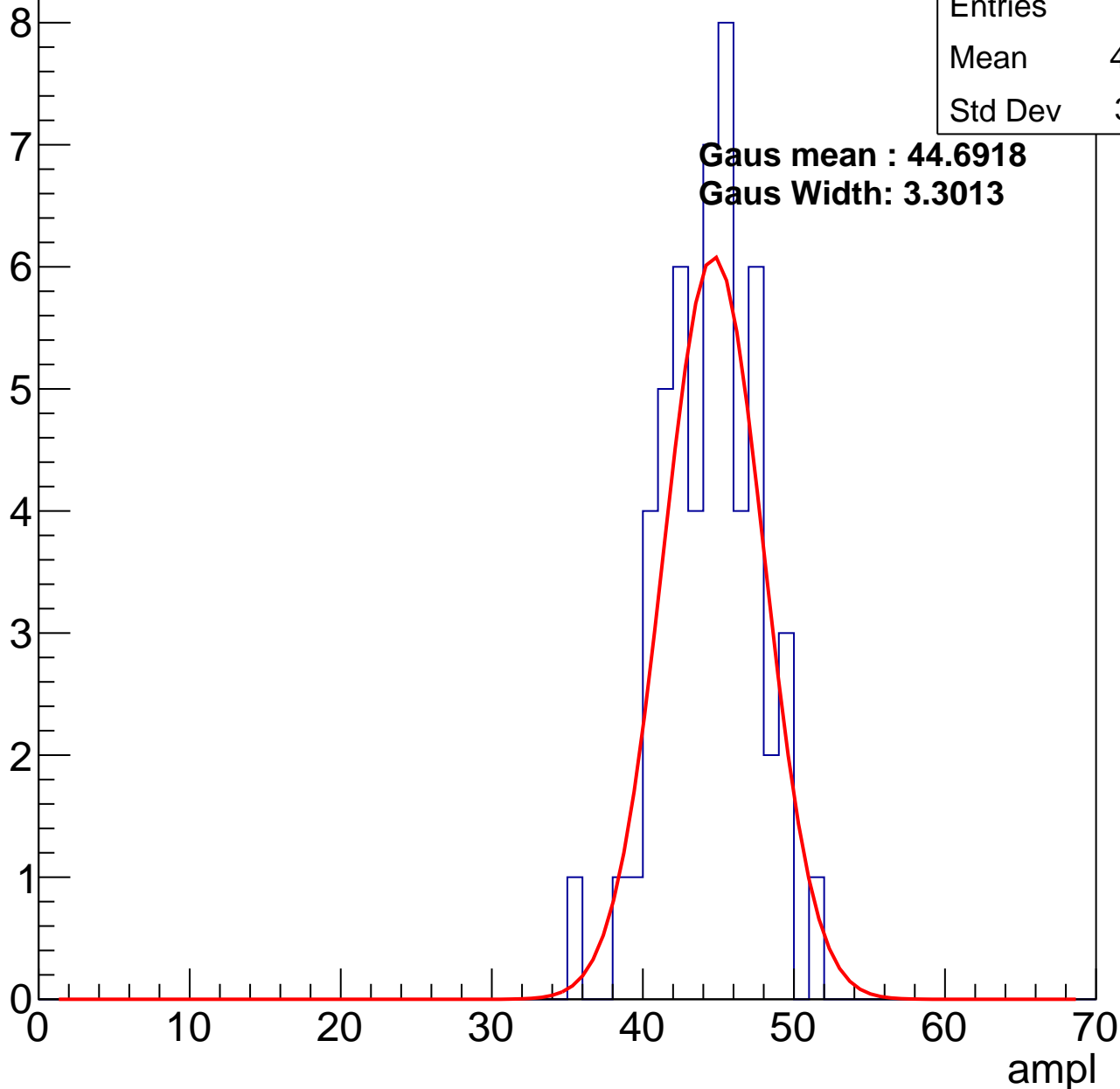
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	43.94
Std Dev	3.111

**Gaus mean : 44.6918**

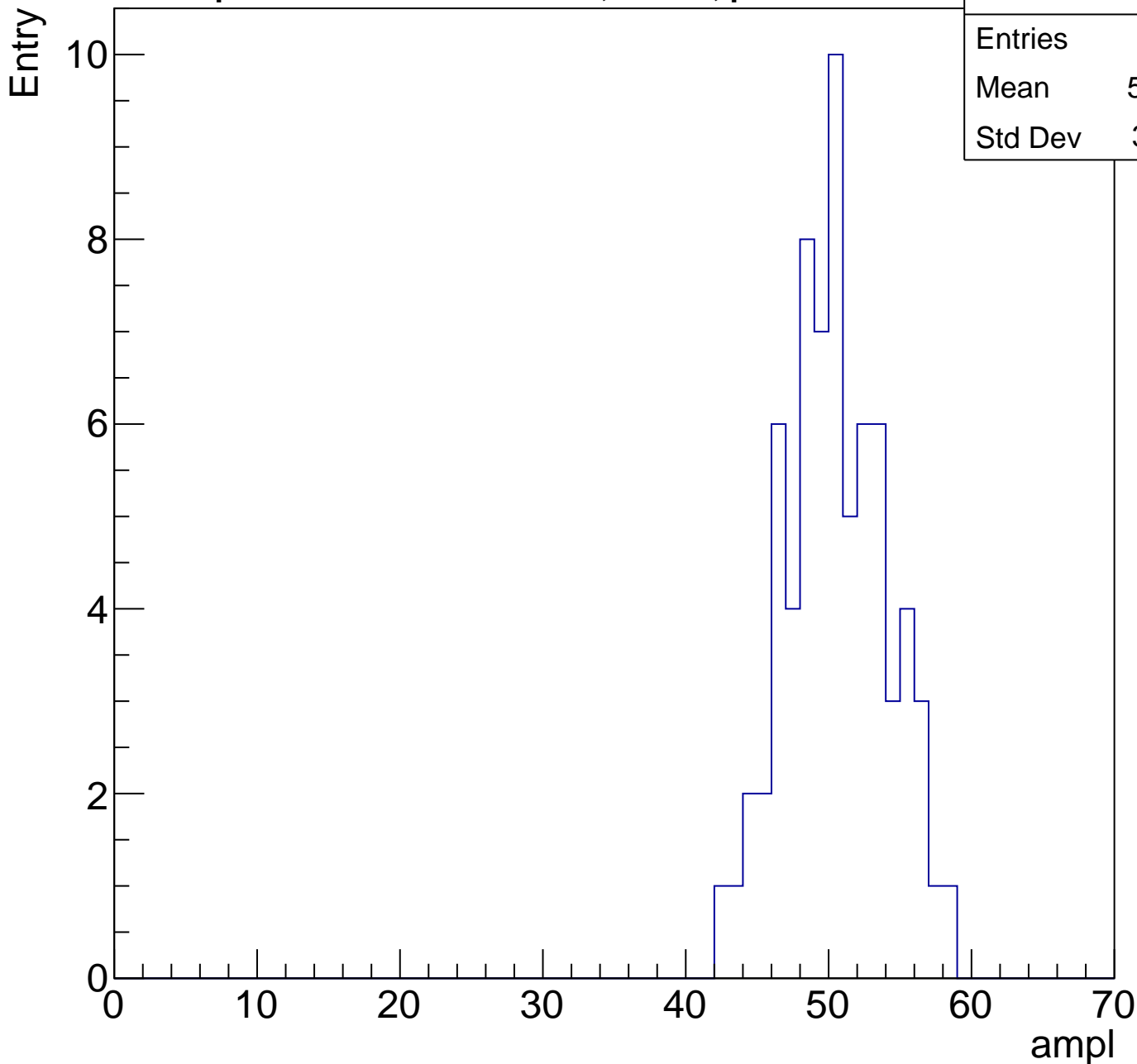
**Gaus Width: 3.3013**



# B1L003S, U6-ch8, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	70
Mean	50.06
Std Dev	3.501

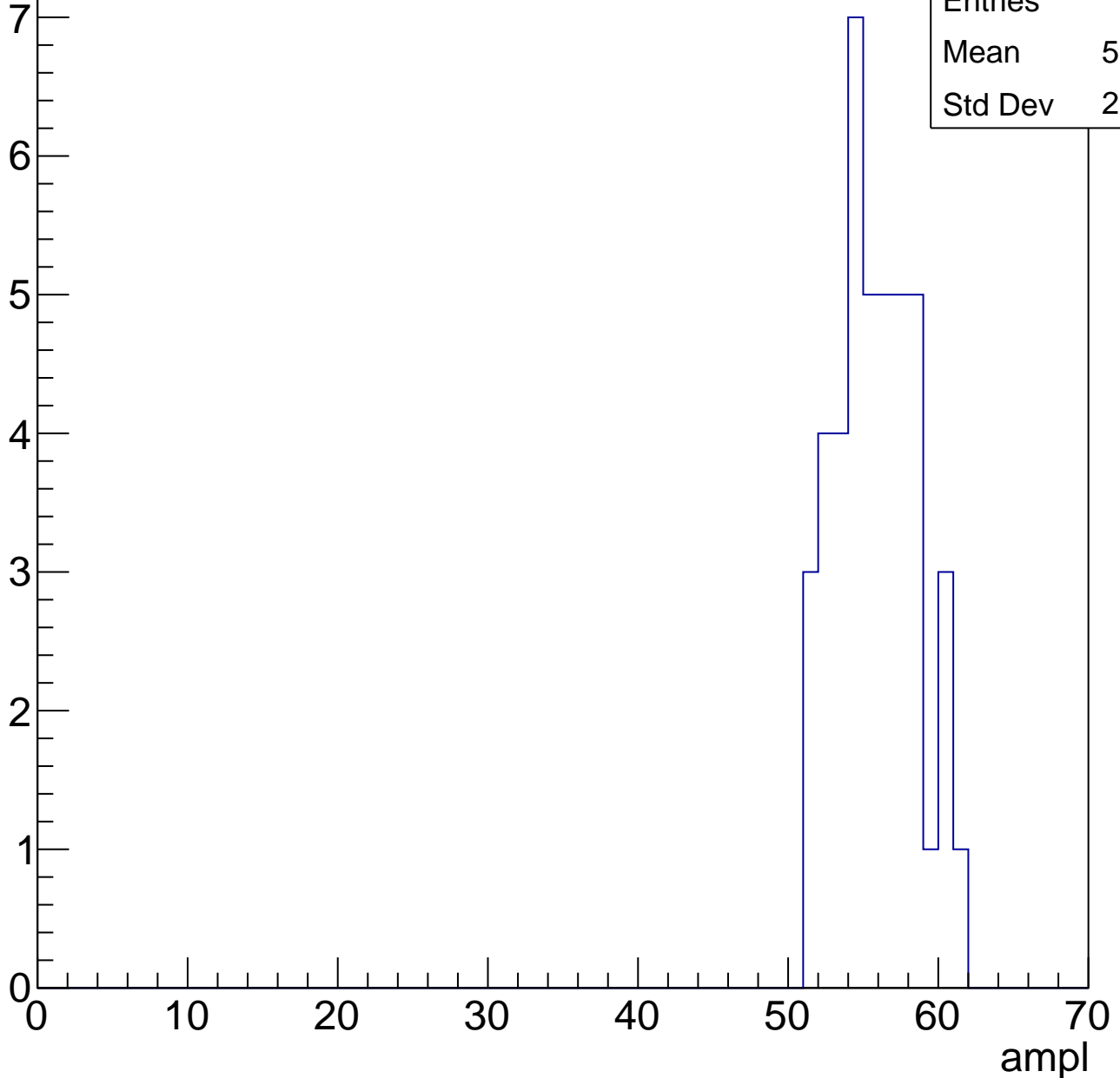


# B1L003S, U6-ch8, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

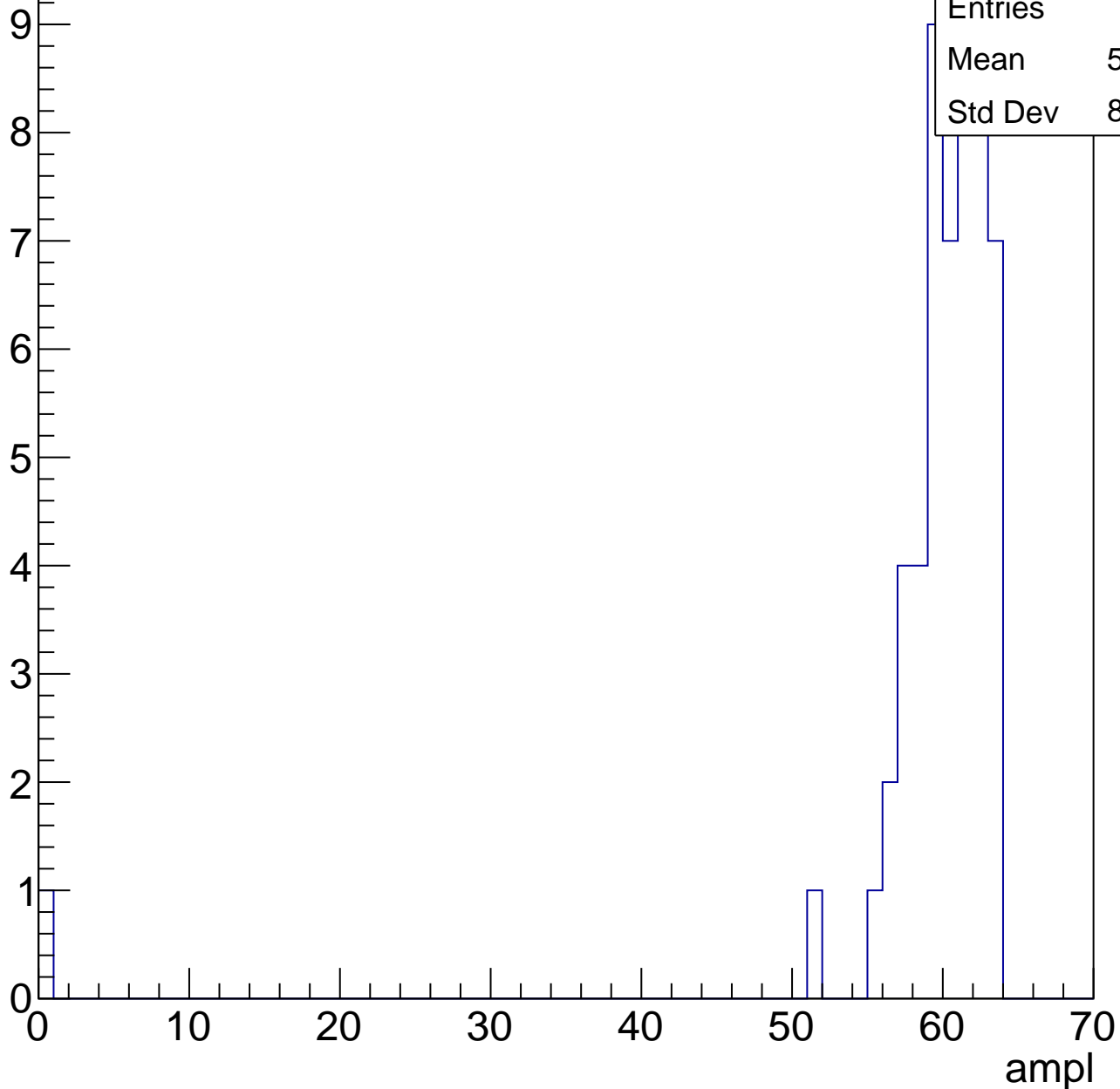
Entries	43
Mean	55.37
Std Dev	2.633



# B1L003S, U6-ch8, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch8, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch8, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch9, adc0

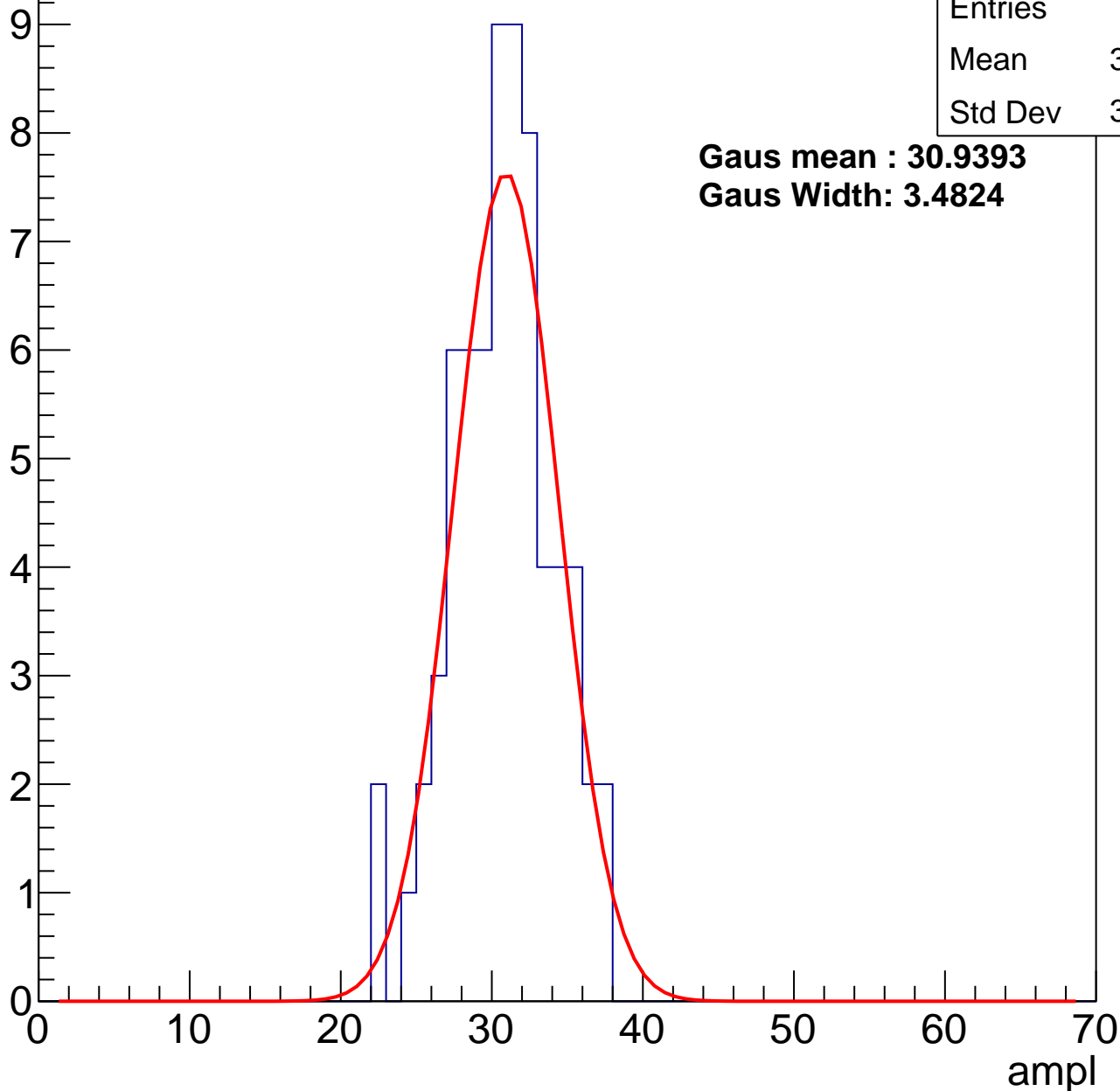
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	30.28
Std Dev	3.325

**Gaus mean : 30.9393**

**Gaus Width: 3.4824**



# B1L003S, U6-ch9, adc1

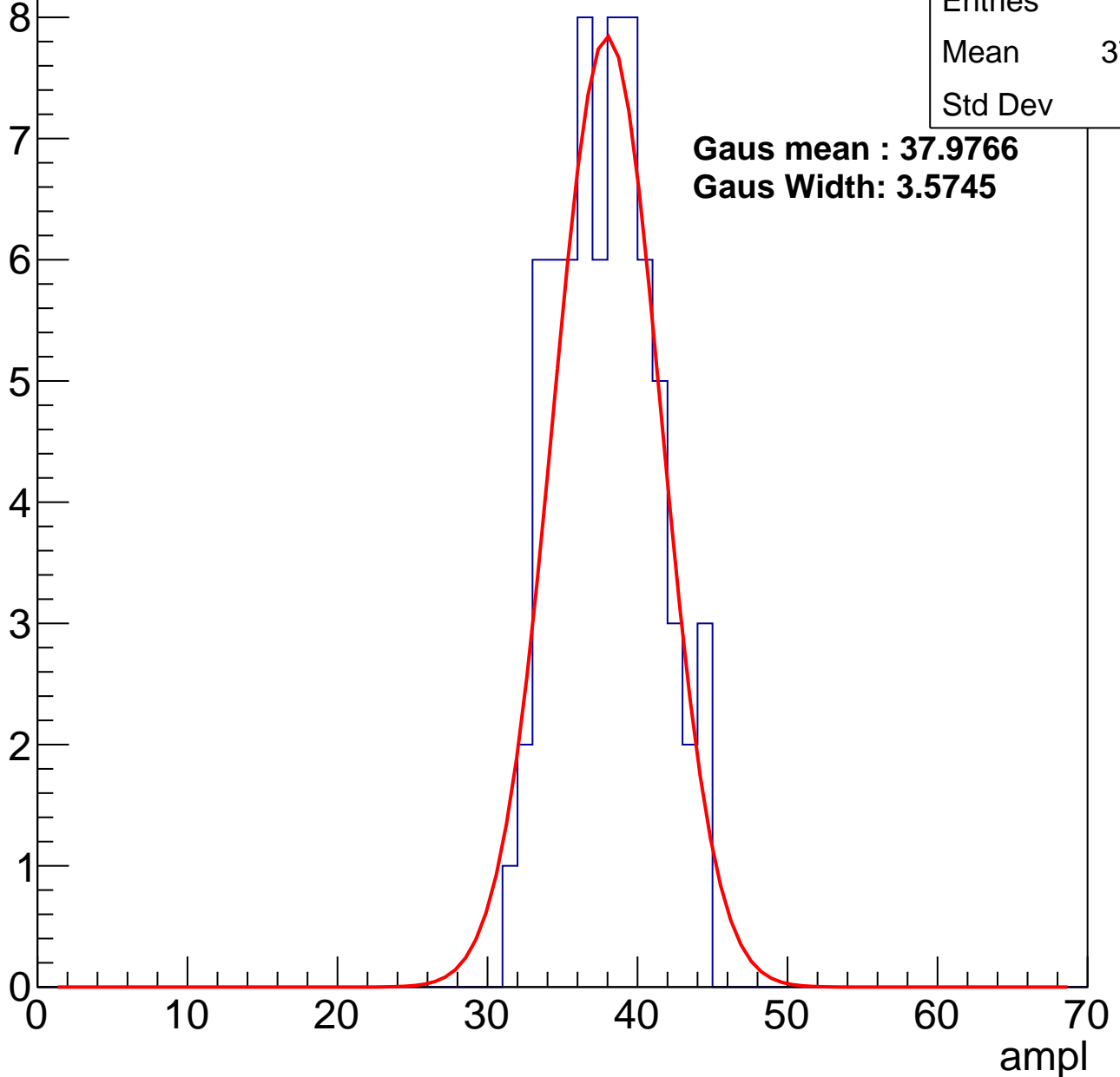
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	37.46
Std Dev	3.21

**Gaus mean : 37.9766**

**Gaus Width: 3.5745**



# B1L003S, U6-ch9, adc2

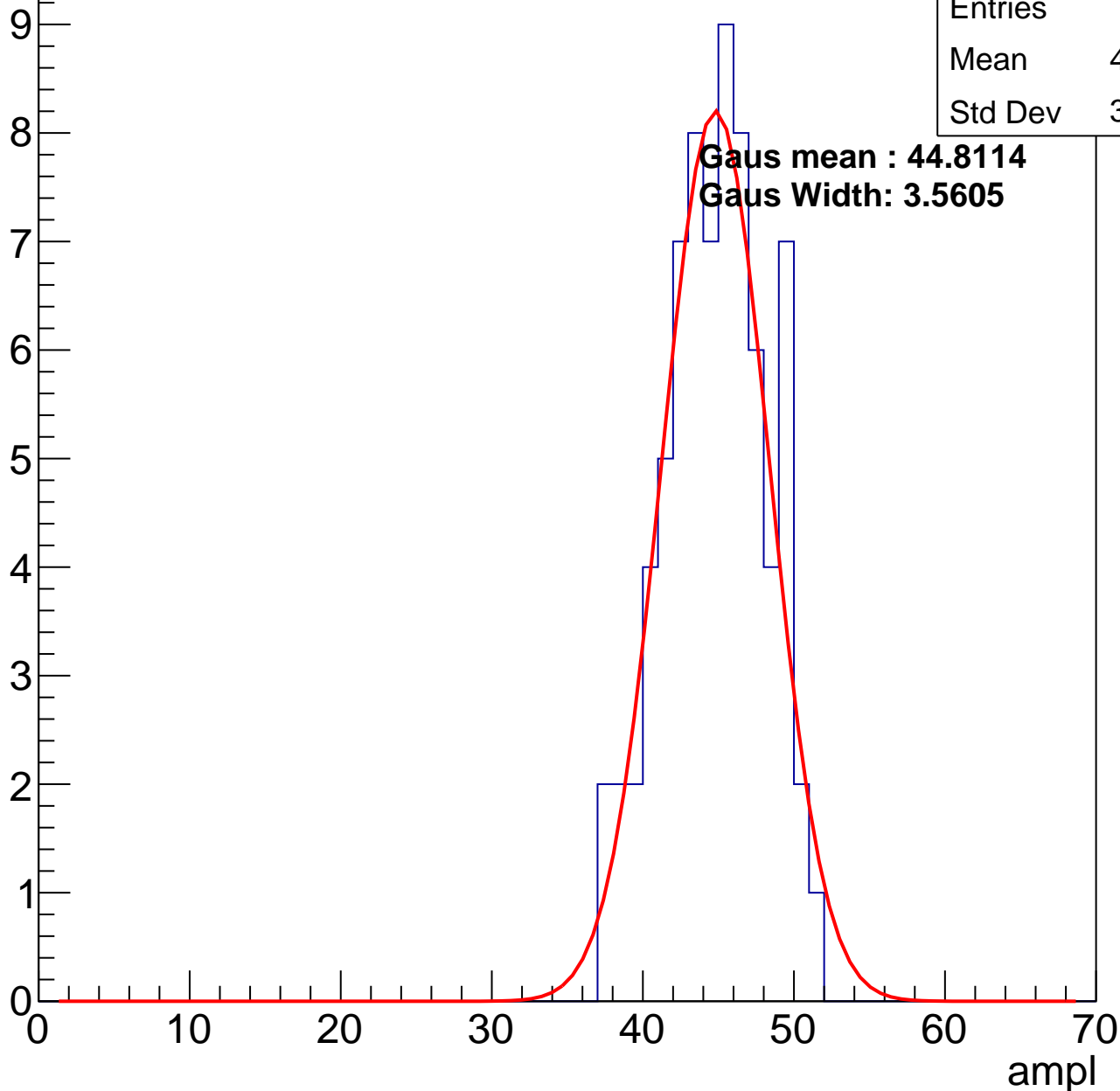
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	74
Mean	44.32
Std Dev	3.313

**Gaus mean : 44.8114**

**Gaus Width: 3.5605**

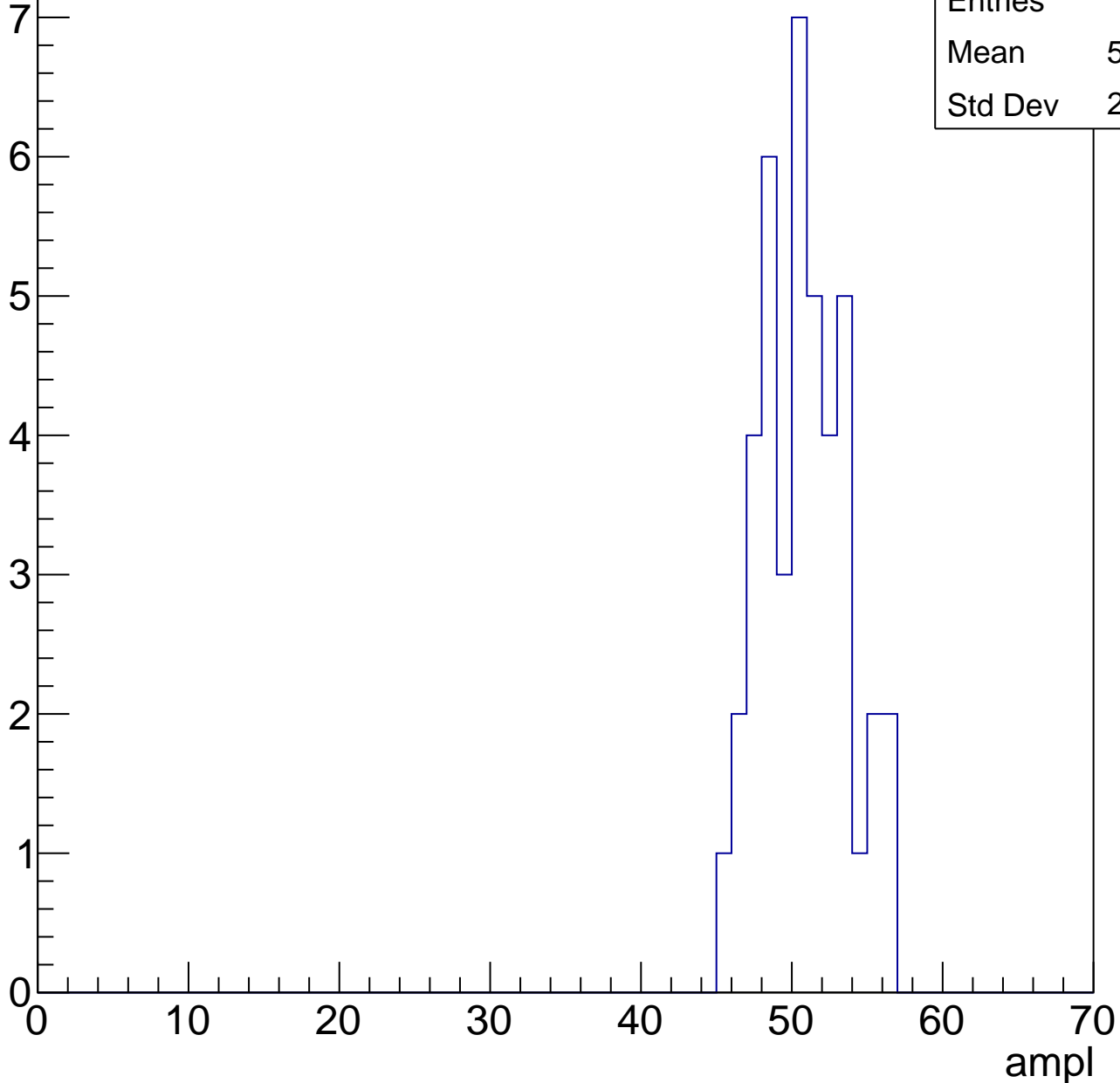


# B1L003S, U6-ch9, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

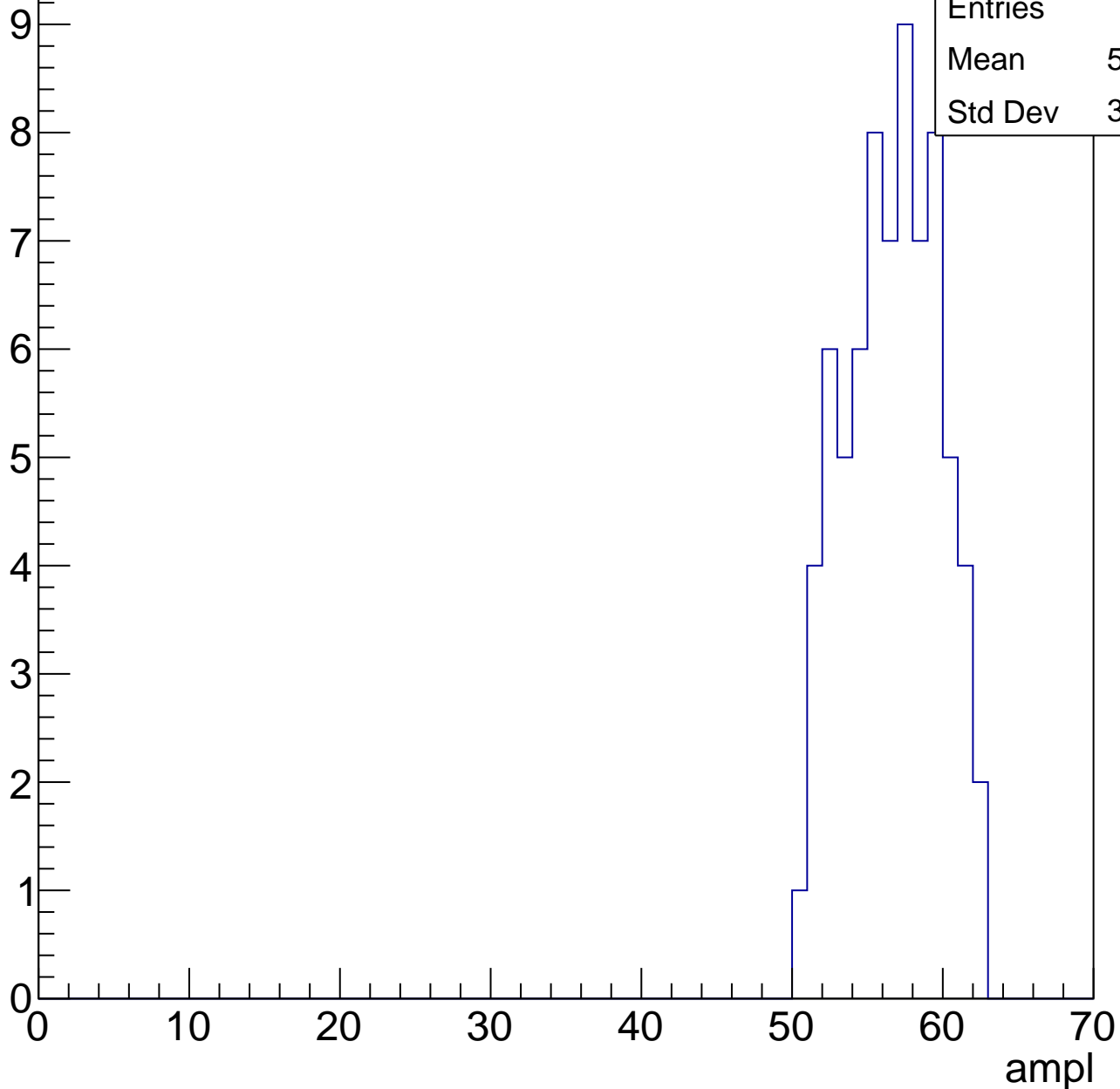
Entries	42
Mean	50.33
Std Dev	2.757



# B1L003S, U6-ch9, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



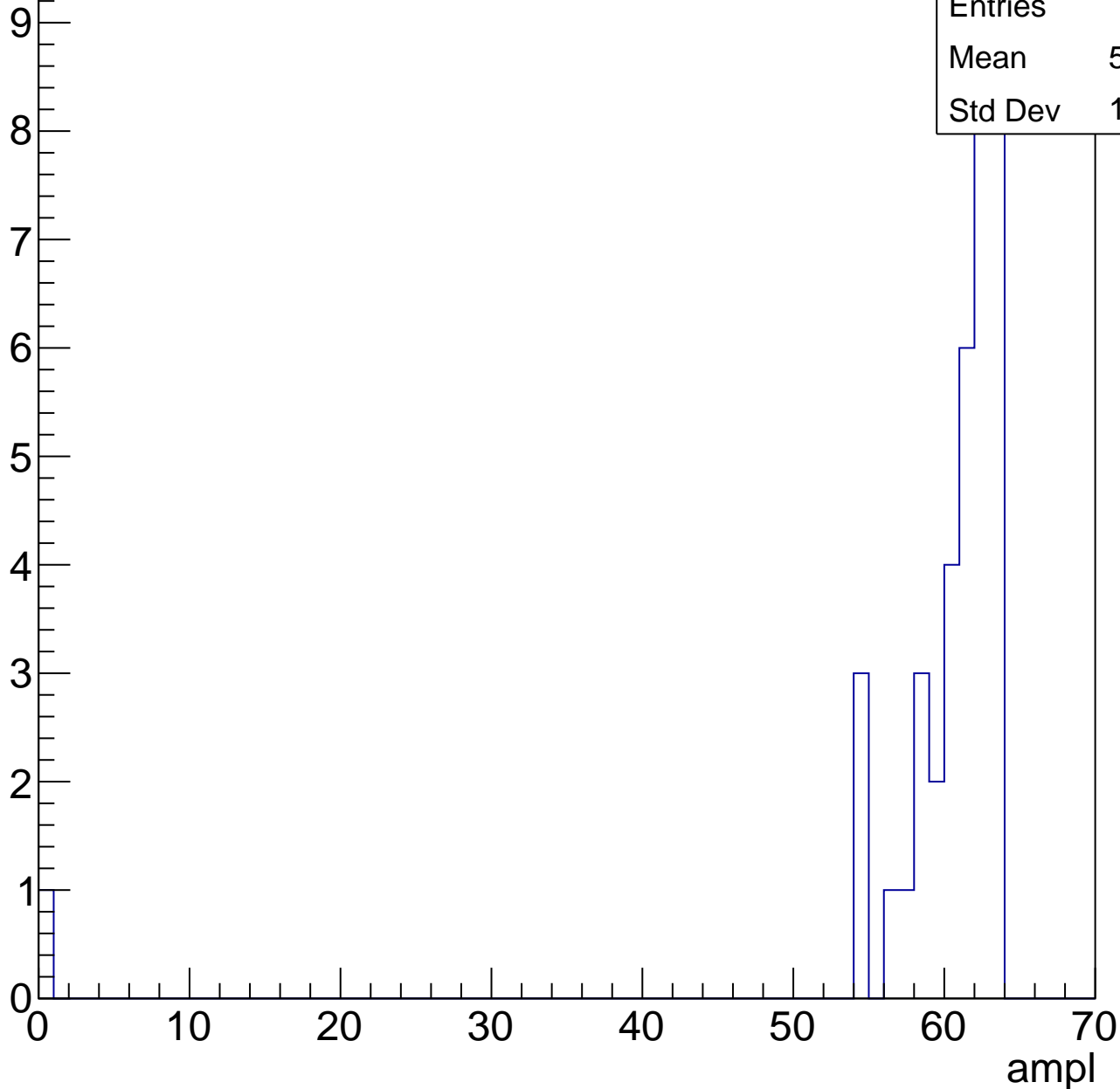
Entries	72
Mean	56.19
Std Dev	3.044

# B1L003S, U6-ch9, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	38
Mean	58.84
Std Dev	10.02



# B1L003S, U6-ch9, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch9, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch10, adc0

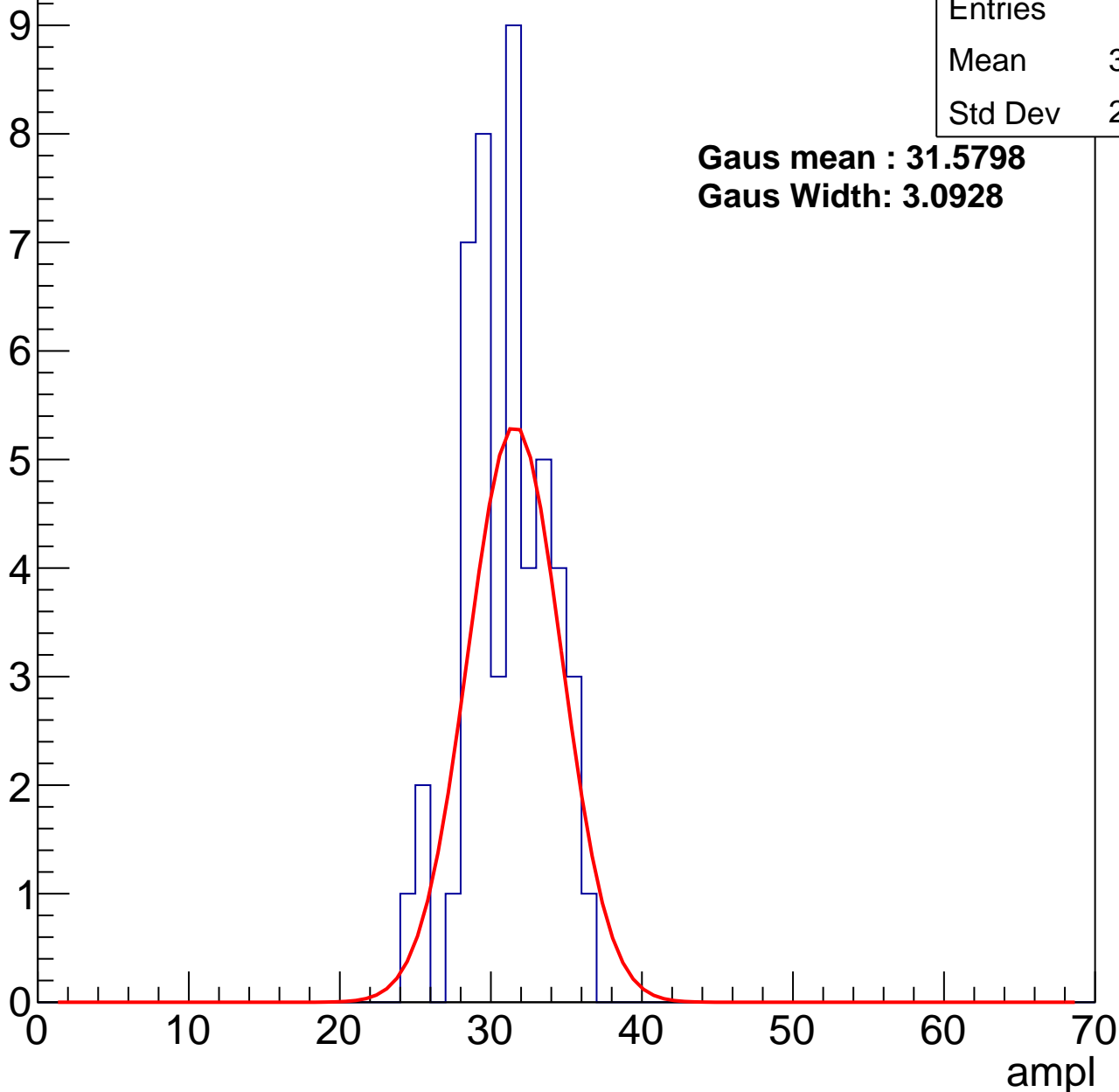
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	48
Mean	30.58
Std Dev	2.737

**Gaus mean : 31.5798**

**Gaus Width: 3.0928**



# B1L003S, U6-ch10, adc1

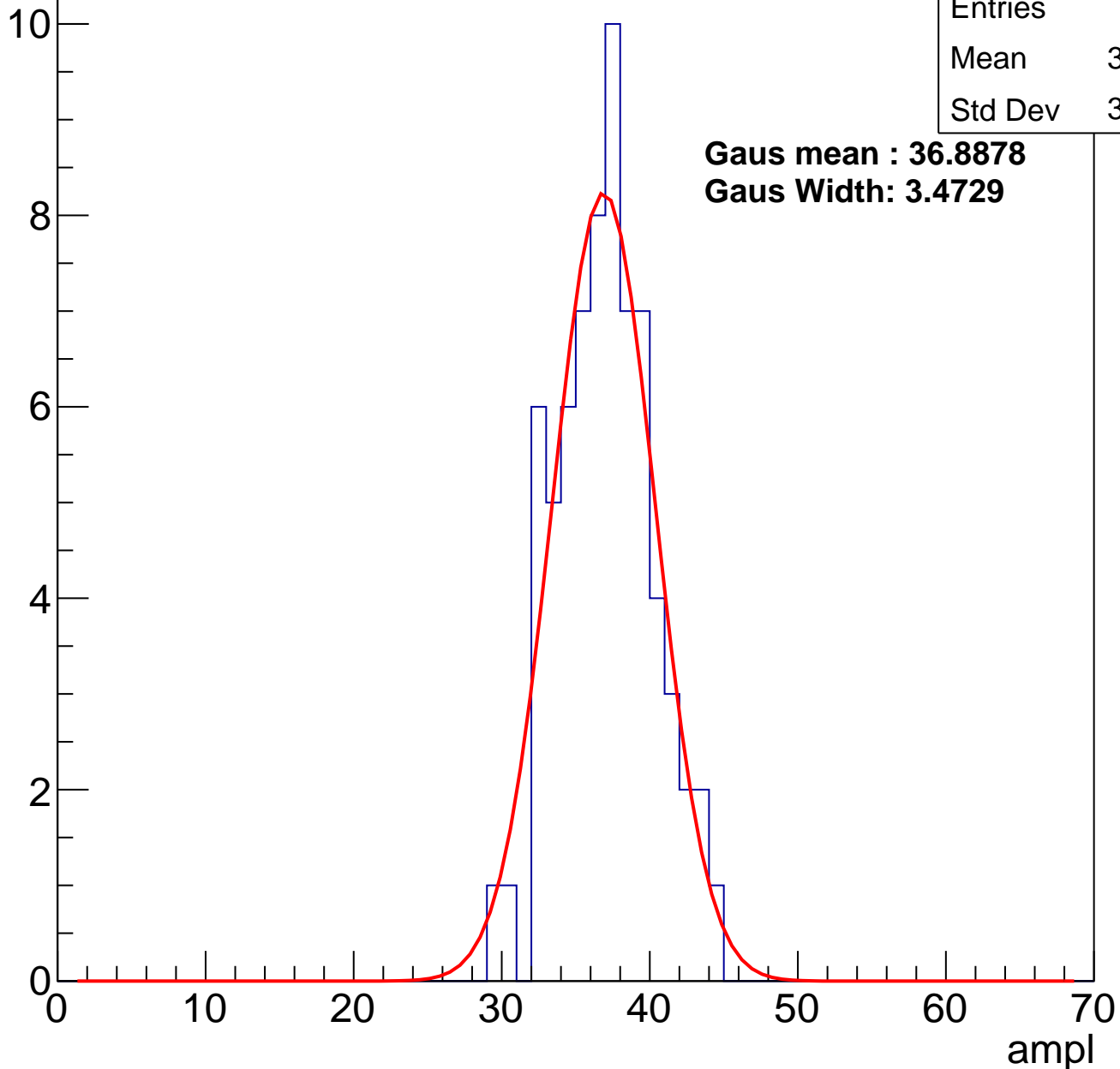
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	70
Mean	36.56
Std Dev	3.183

**Gaus mean : 36.8878**

**Gaus Width: 3.4729**

Entry



# B1L003S, U6-ch10, adc2

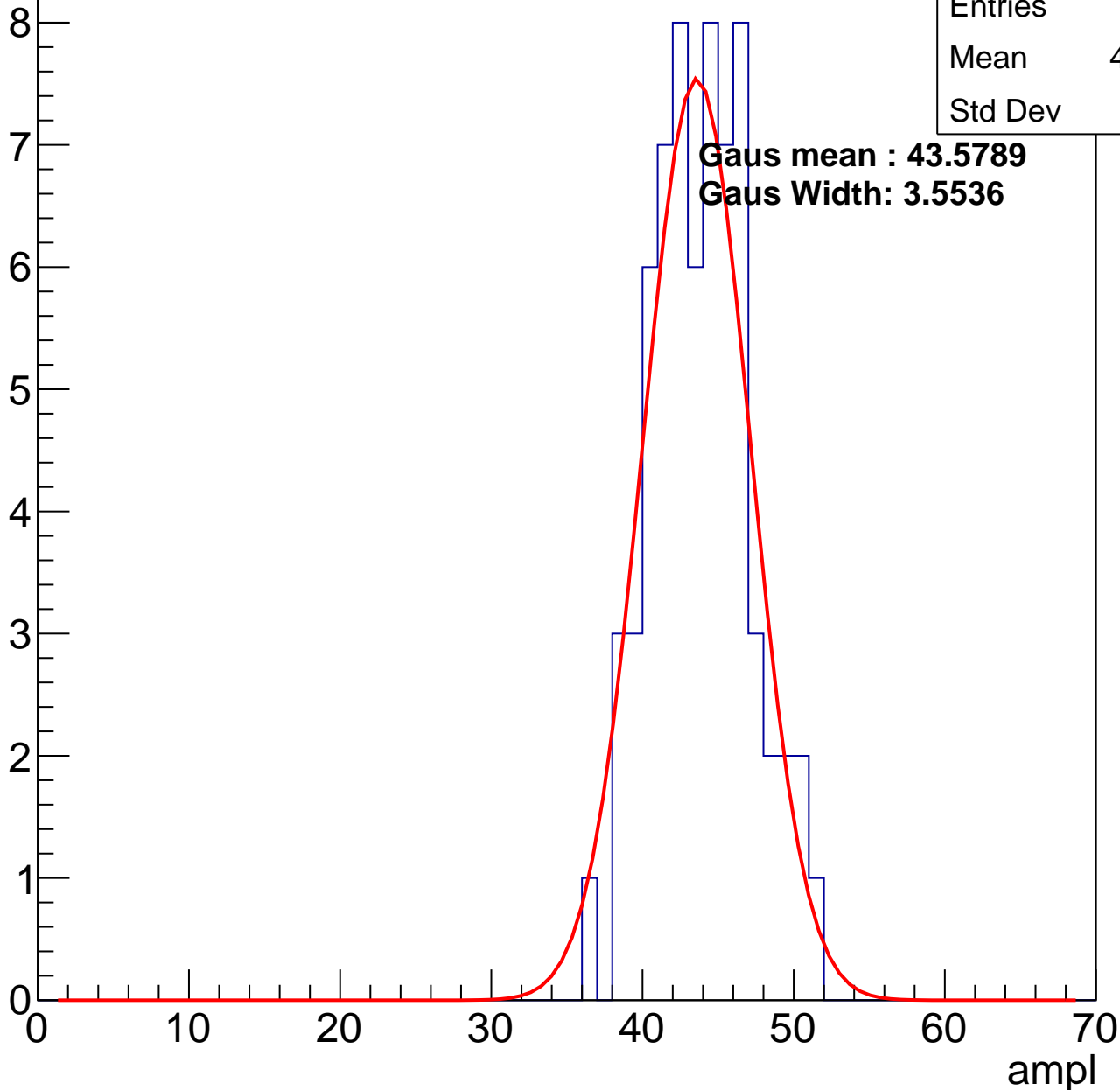
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	43.42
Std Dev	3.21

**Gaus mean : 43.5789**

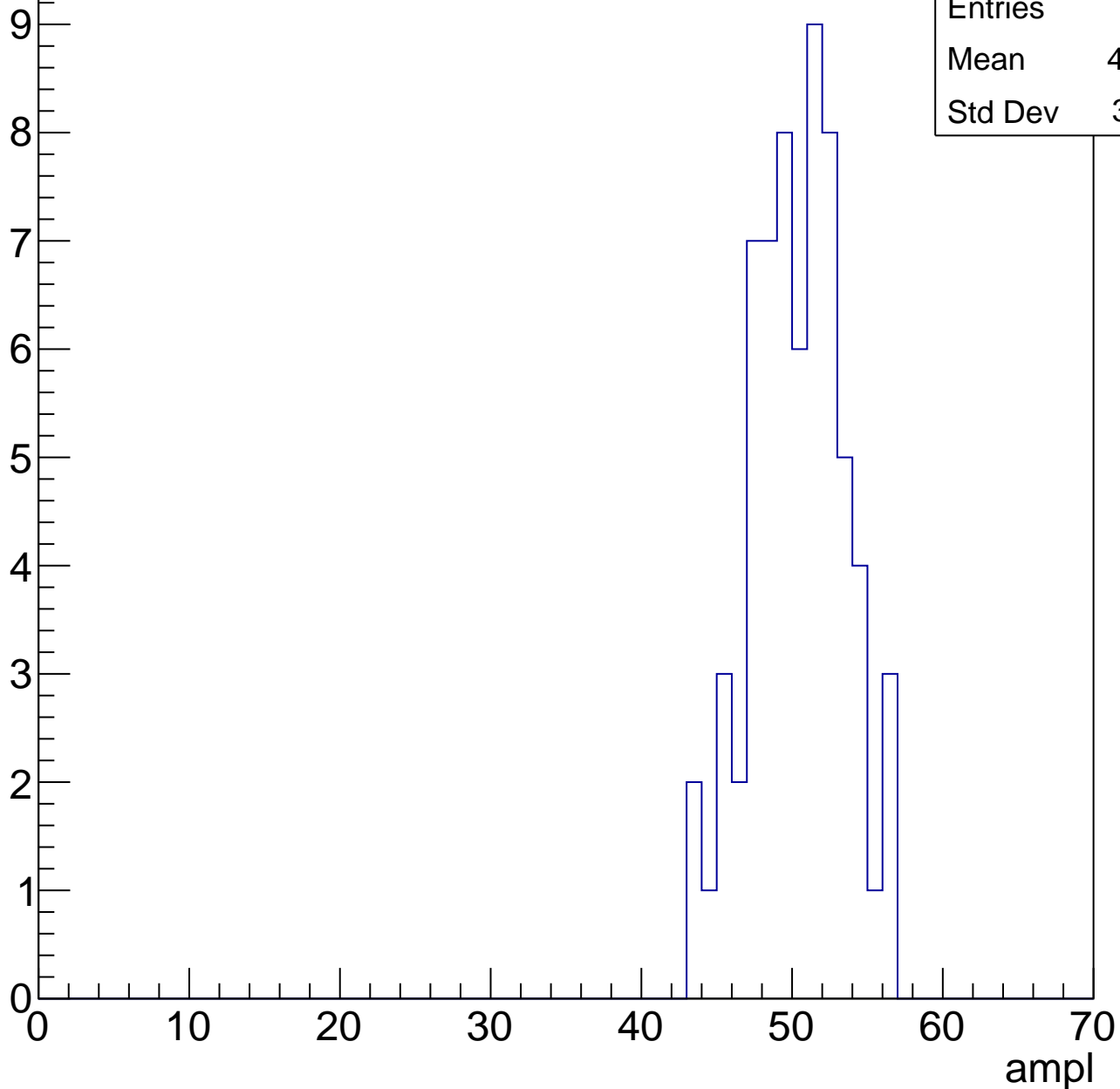
**Gaus Width: 3.5536**



# B1L003S, U6-ch10, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

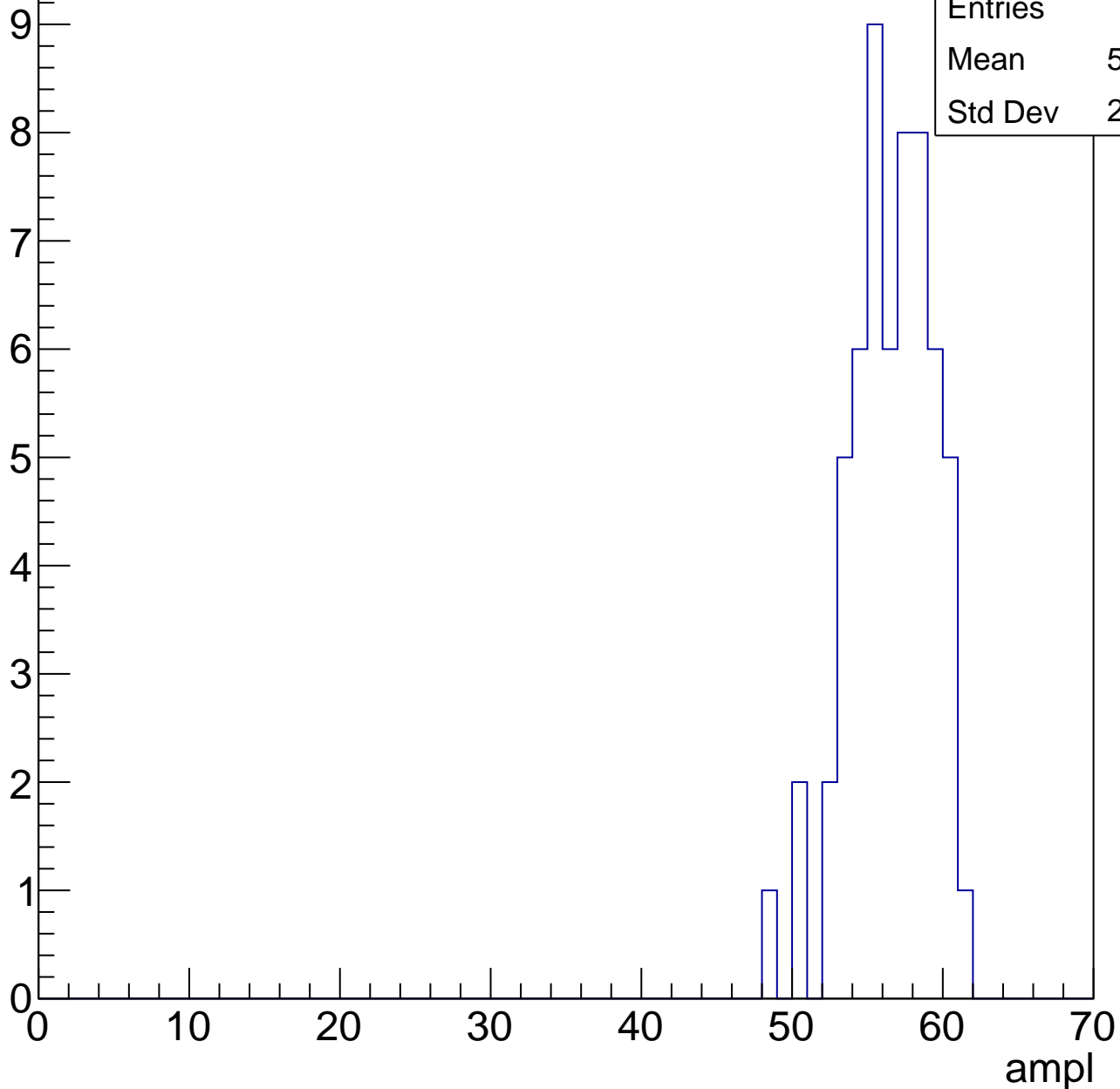


Entries	66
Mean	49.89
Std Dev	3.071

# B1L003S, U6-ch10, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



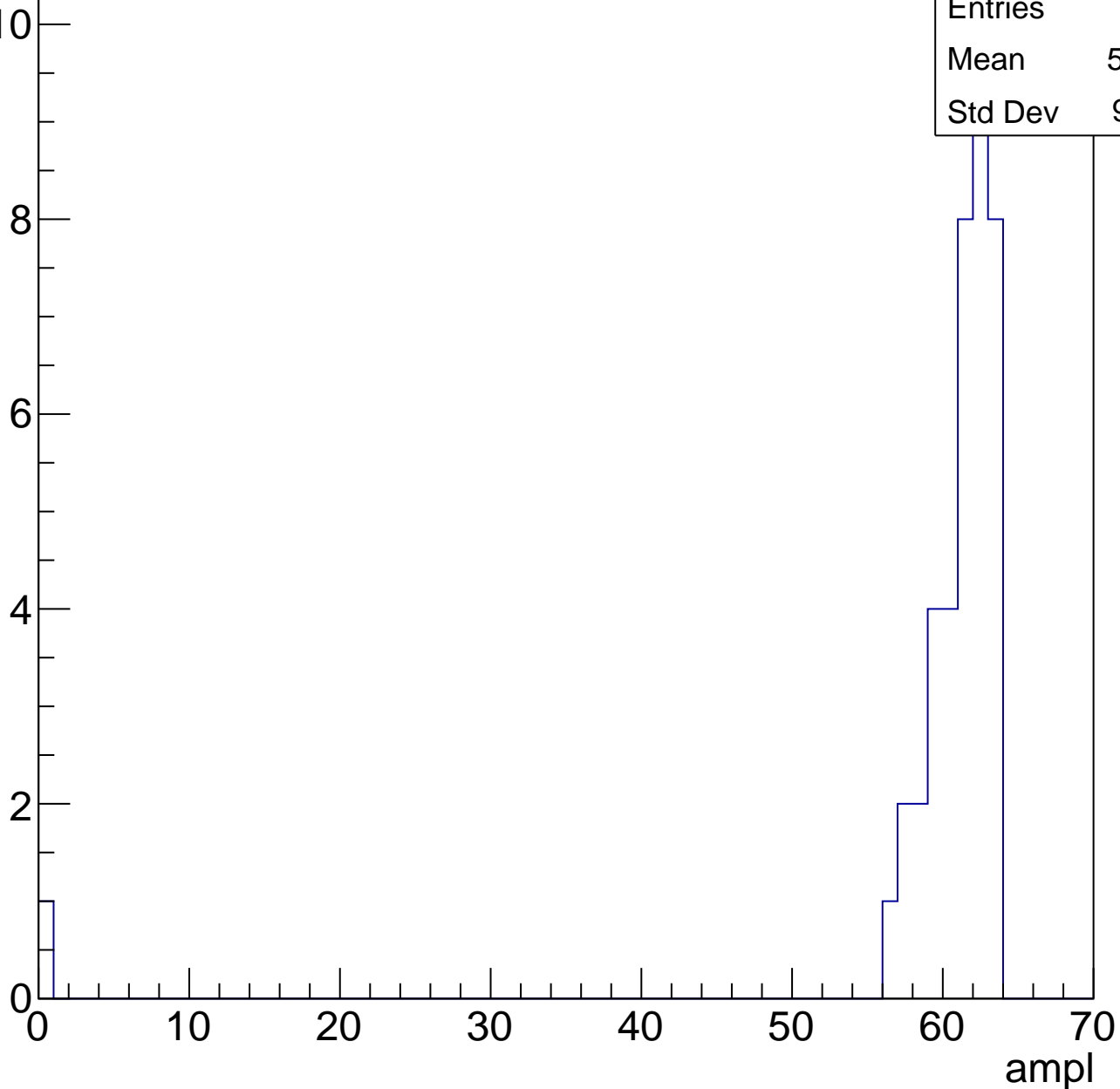
Entries	59
Mean	56.05
Std Dev	2.746

# B1L003S, U6-ch10, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	40
Mean	59.35
Std Dev	9.681



# B1L003S, U6-ch10, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

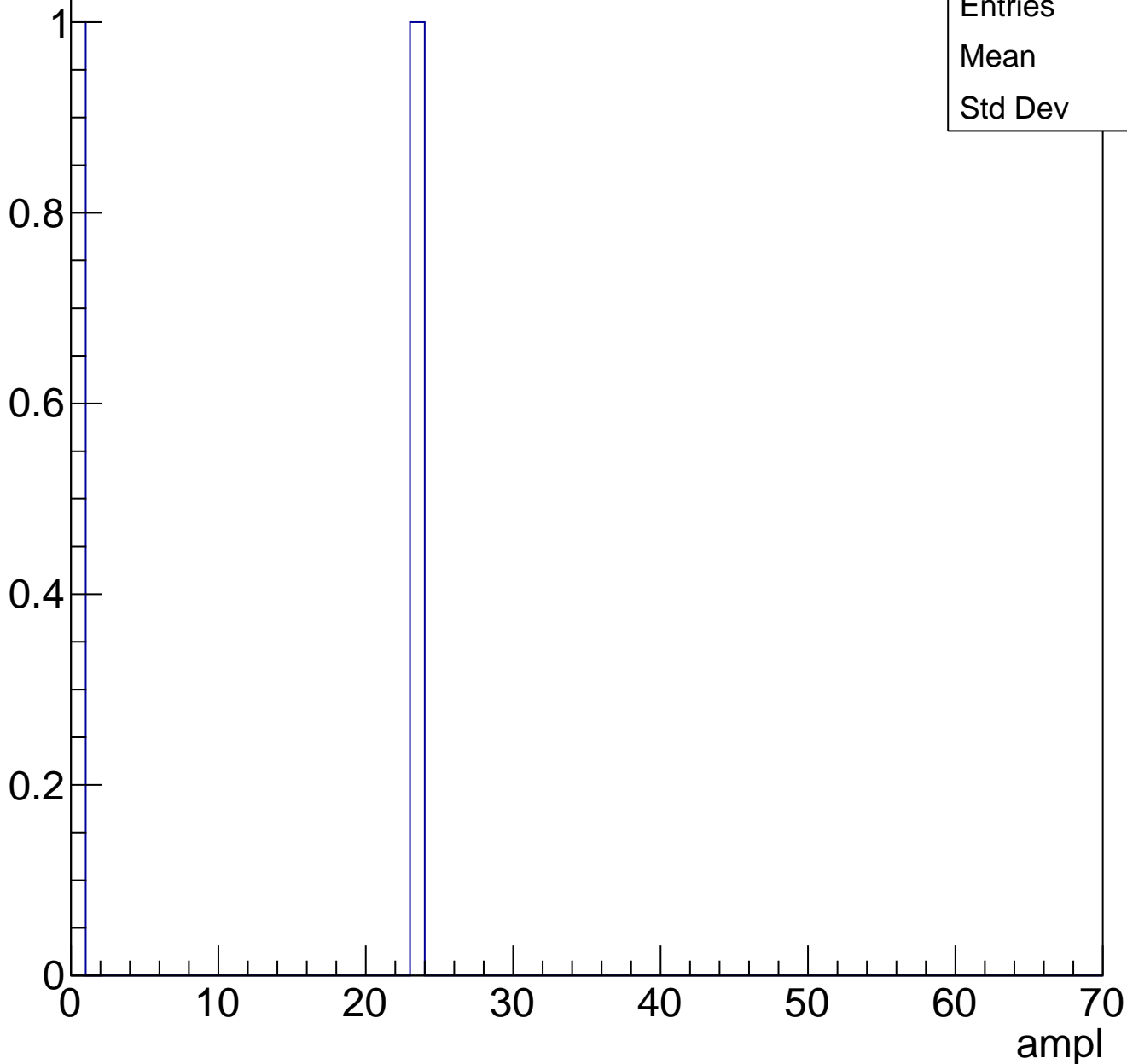




# B1L003S, U6-ch10, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch11, adc0

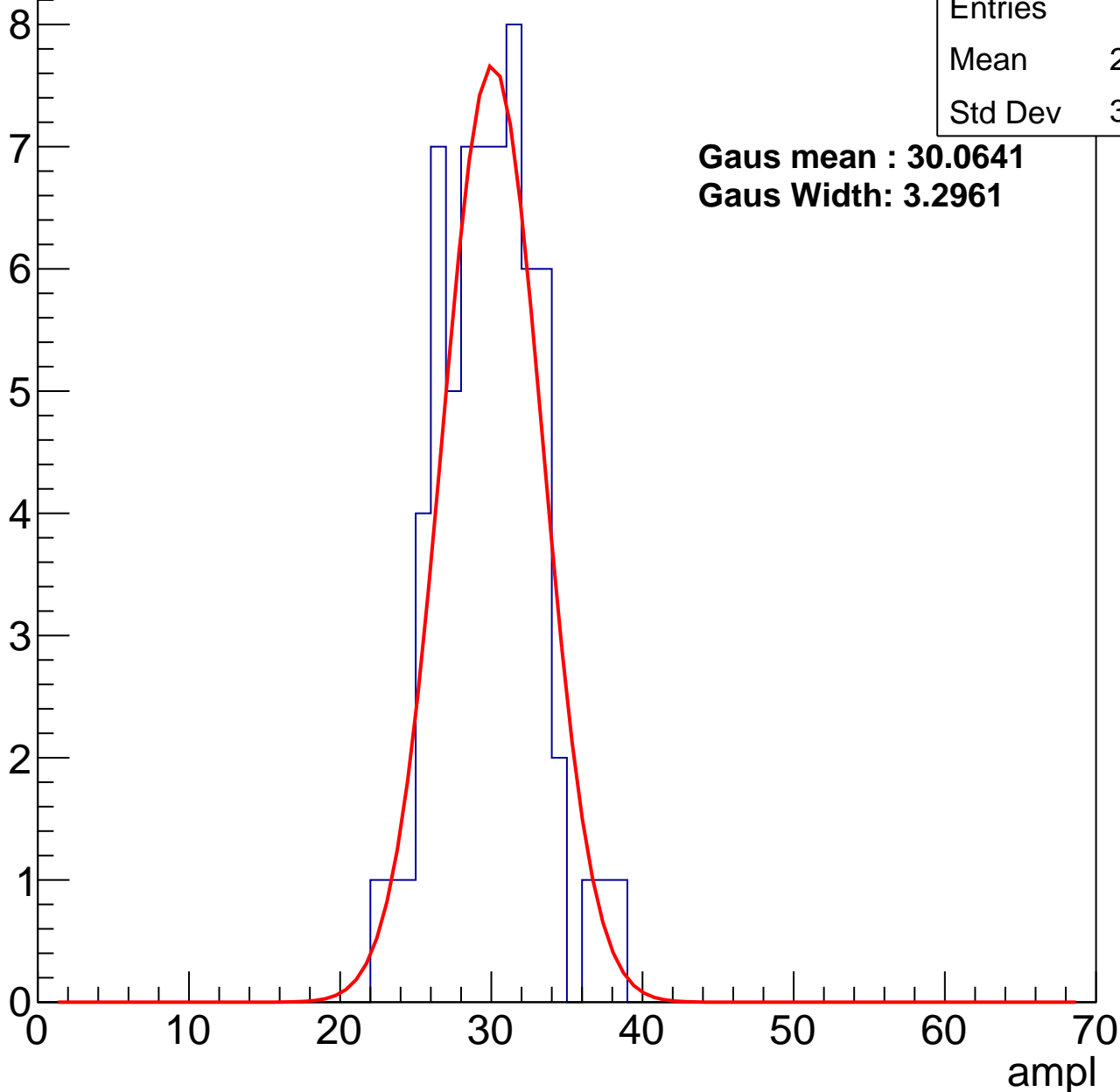
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	29.42
Std Dev	3.248

**Gaus mean : 30.0641**

**Gaus Width: 3.2961**



# B1L003S, U6-ch11, adc1

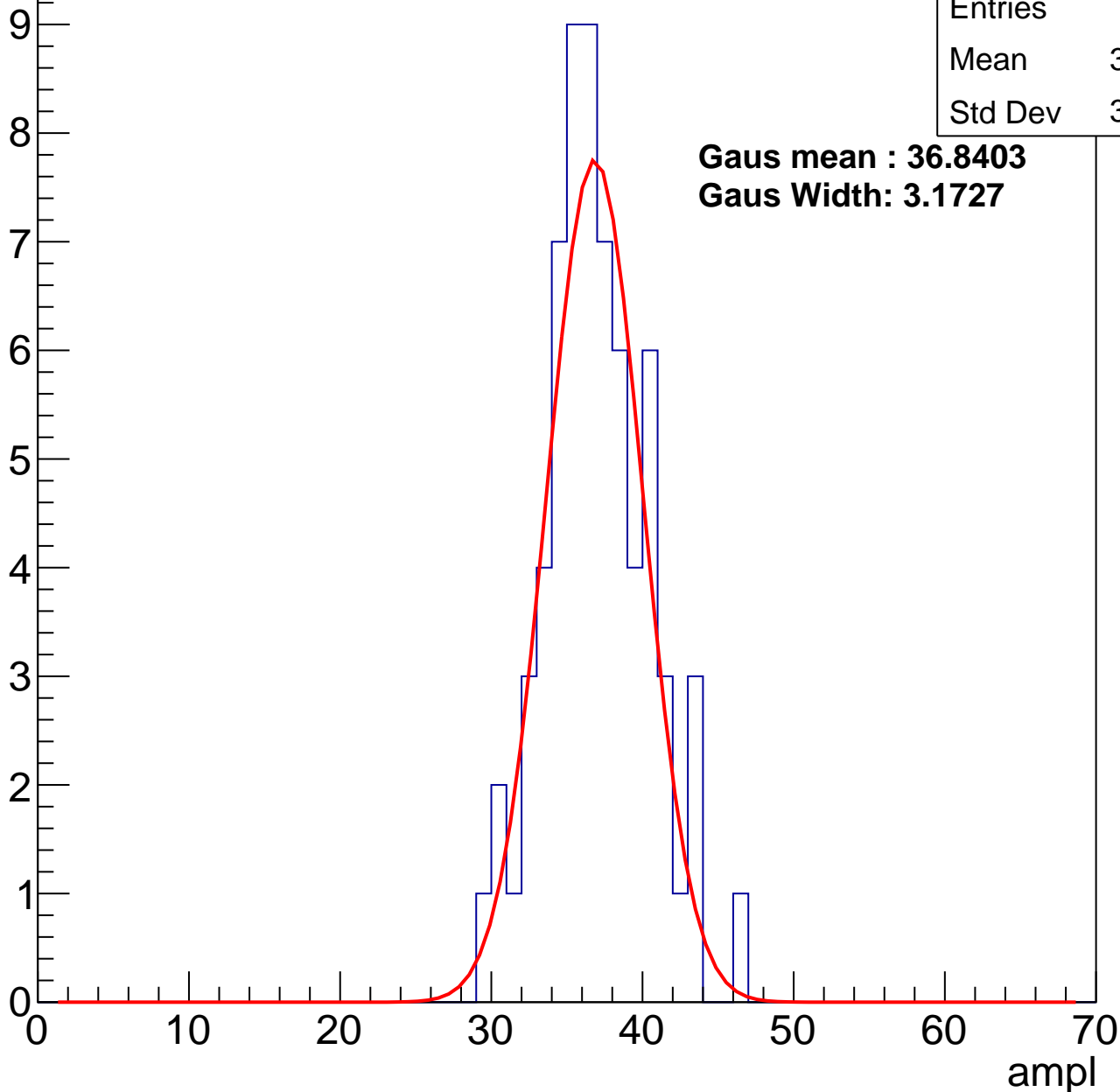
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	36.54
Std Dev	3.387

**Gaus mean : 36.8403**

**Gaus Width: 3.1727**



# B1L003S, U6-ch11, adc2

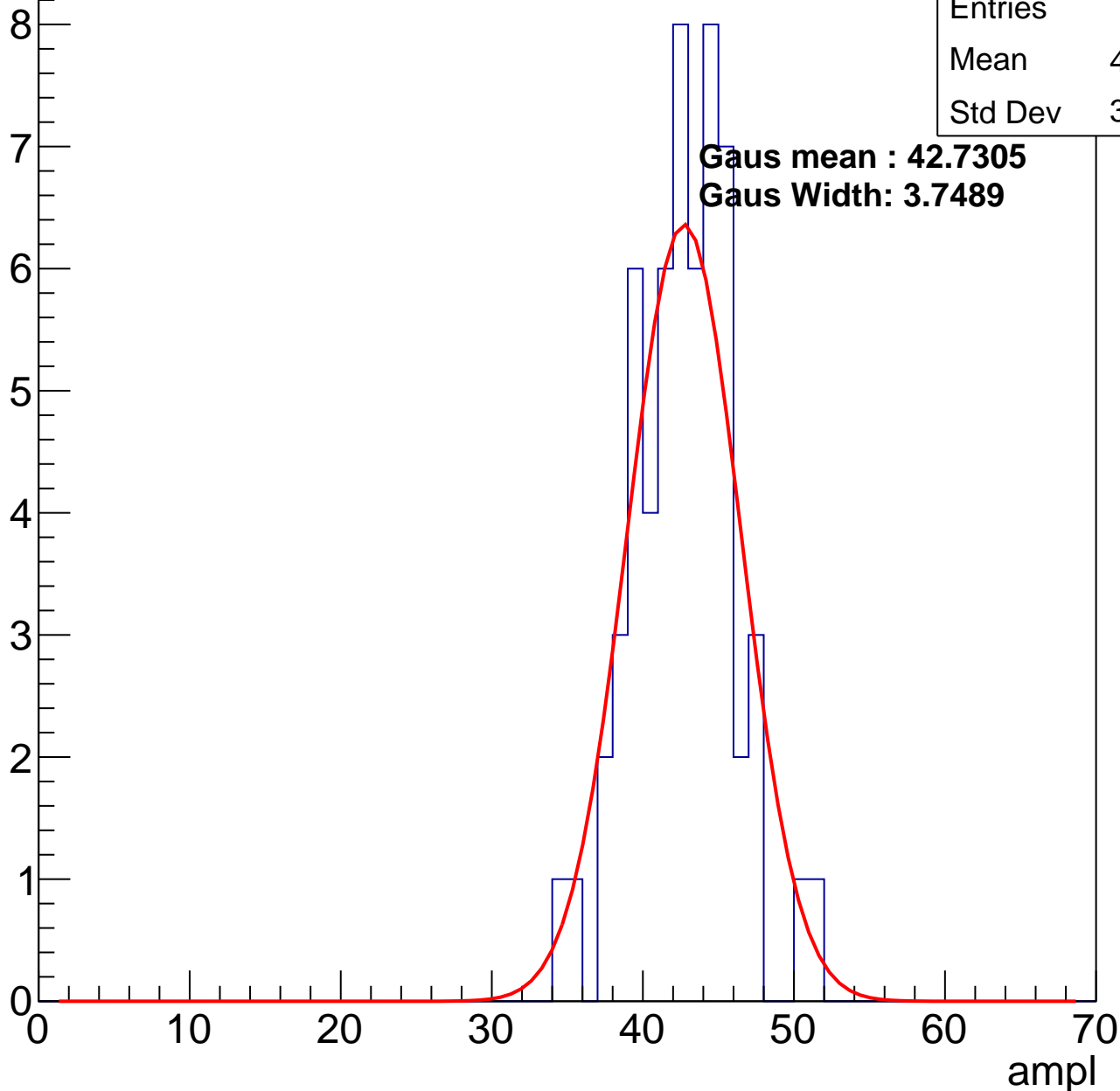
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	42.24
Std Dev	3.285

**Gaus mean : 42.7305**

**Gaus Width: 3.7489**

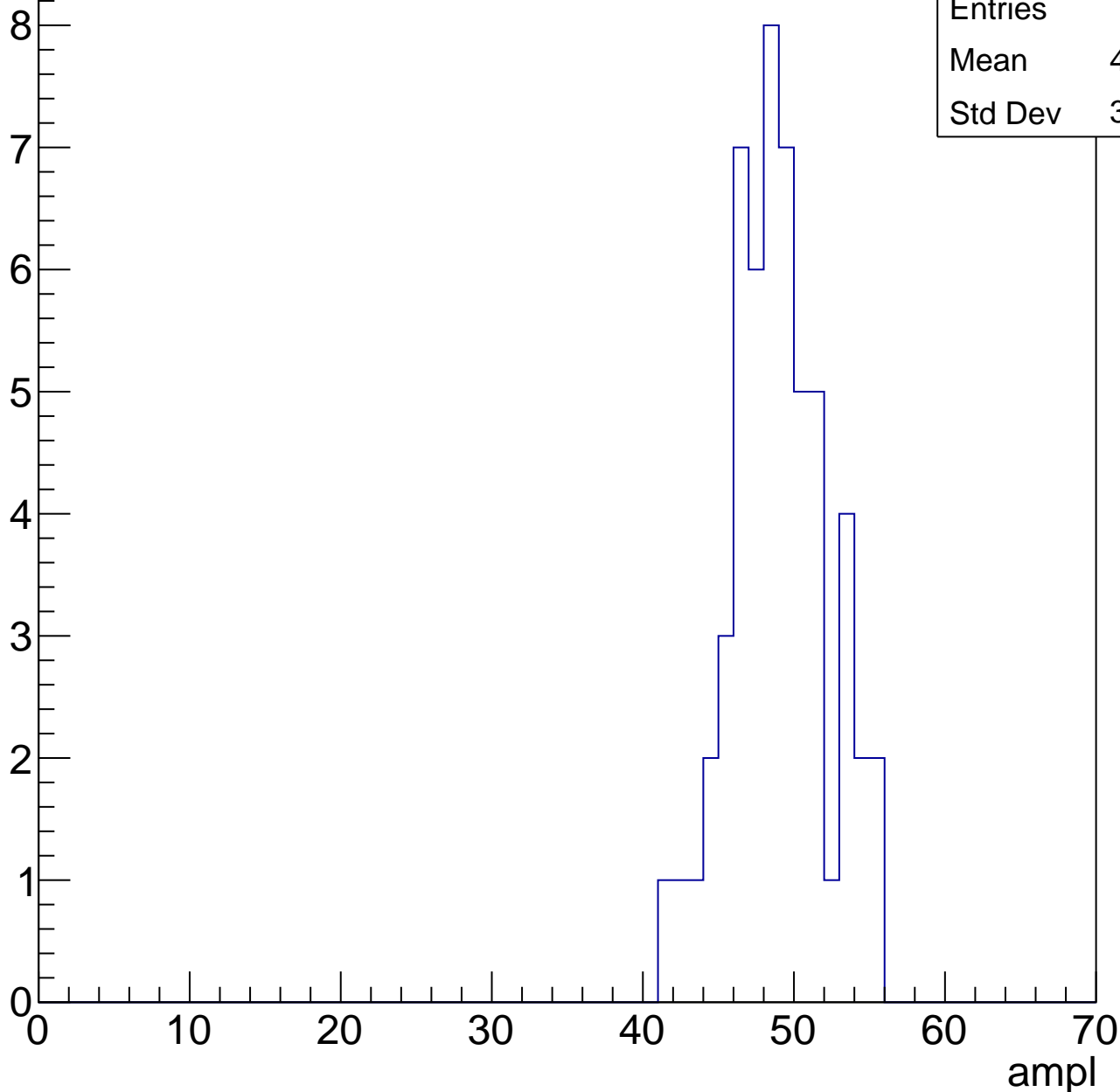


# B1L003S, U6-ch11, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	48.49
Std Dev	3.156

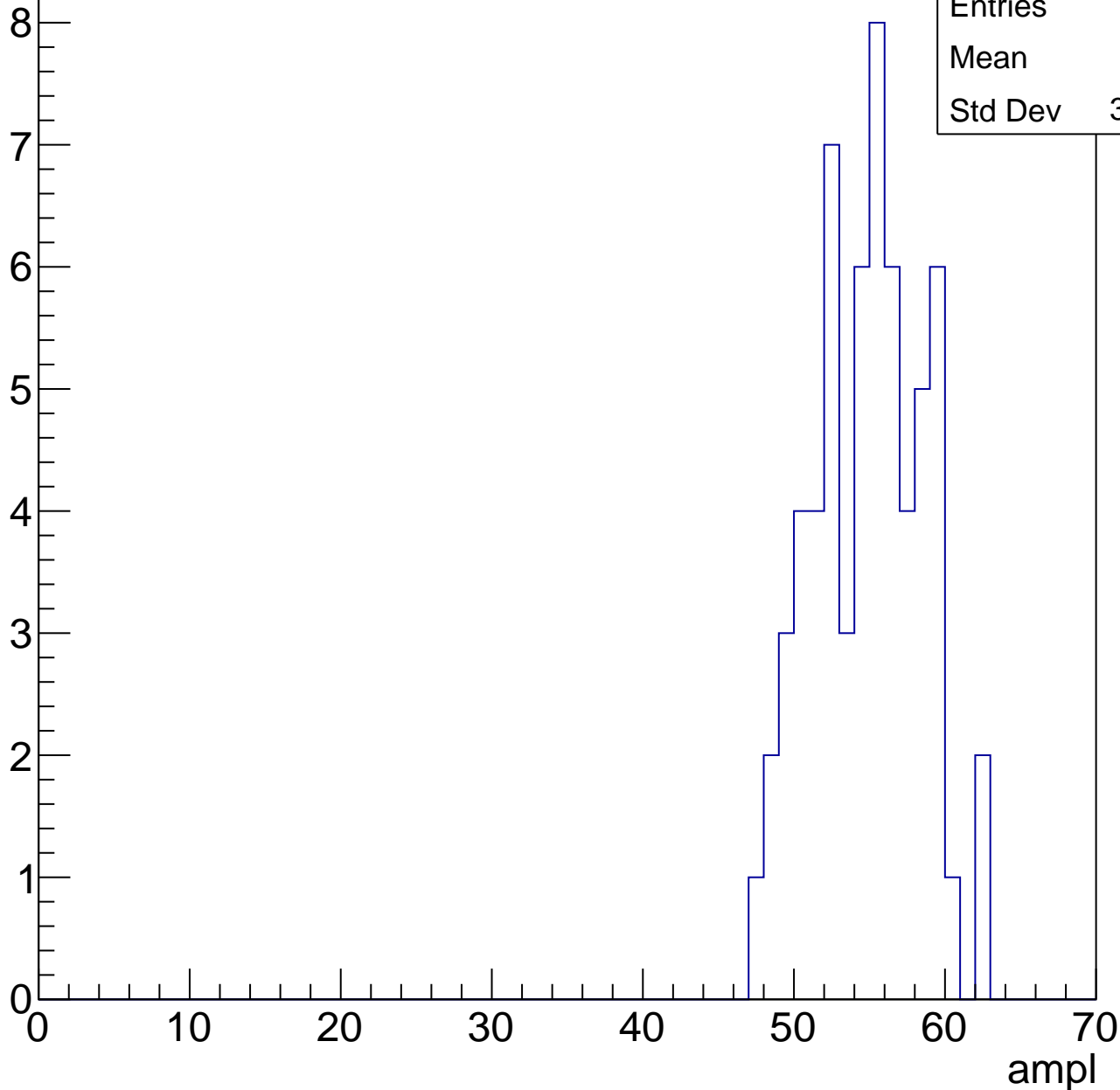


# B1L003S, U6-ch11, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	54.4
Std Dev	3.544

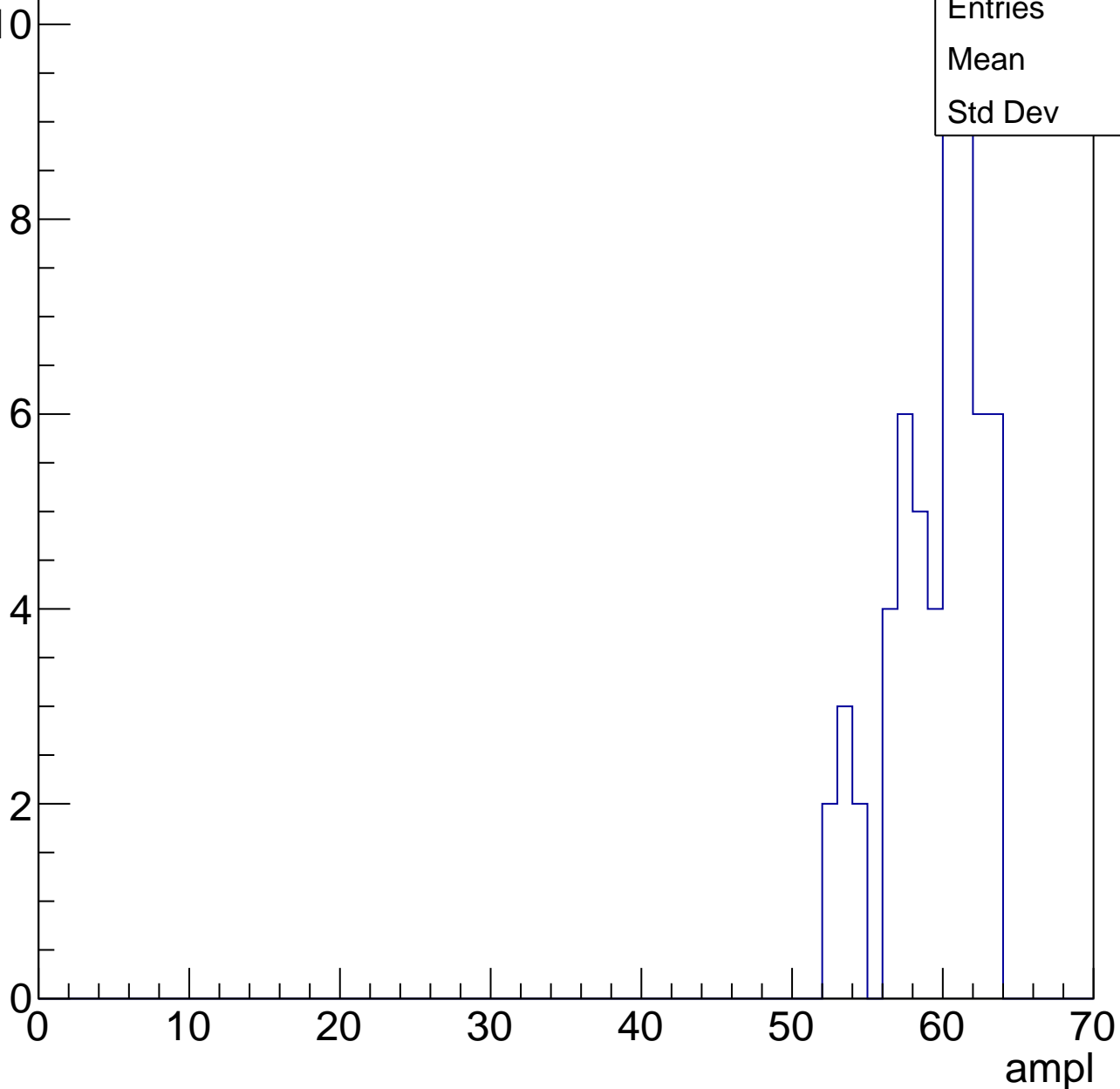


# B1L003S, U6-ch11, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

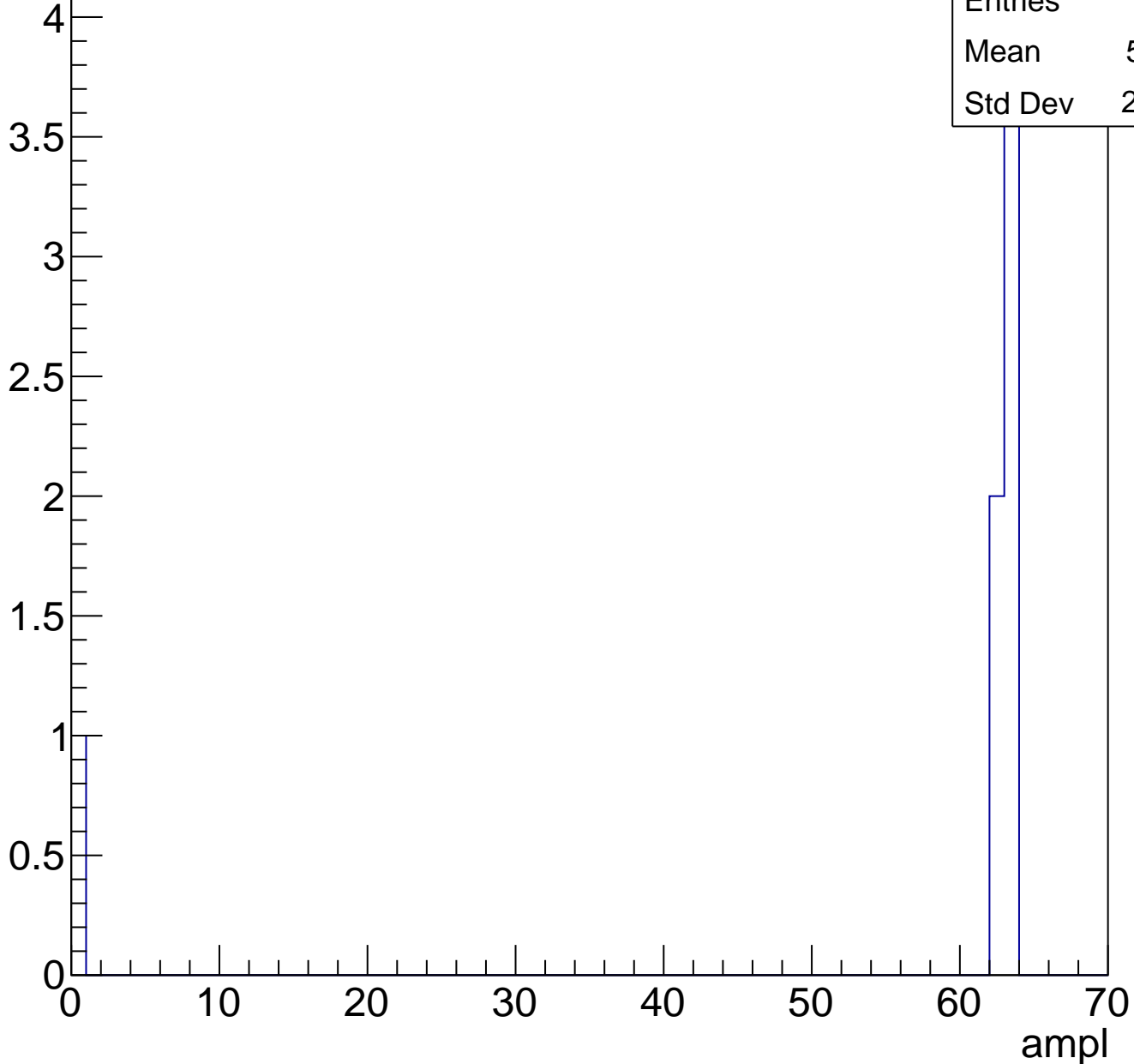
Entries	57
Mean	59
Std Dev	3.02



# B1L003S, U6-ch11, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch11, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L003S, U6-ch12, adc0

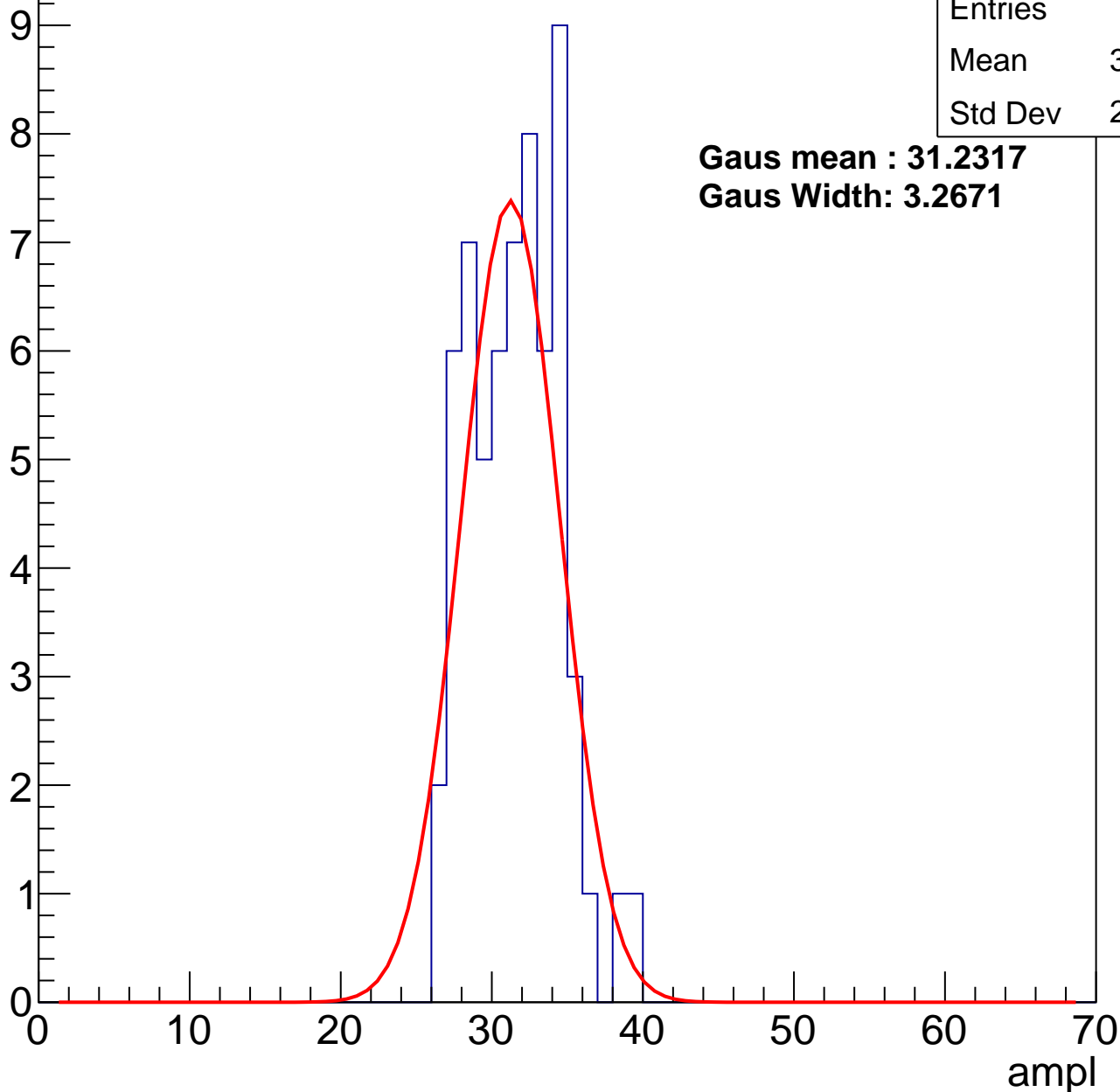
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	31.13
Std Dev	2.932

**Gaus mean : 31.2317**

**Gaus Width: 3.2671**



# B1L003S, U6-ch12, adc1

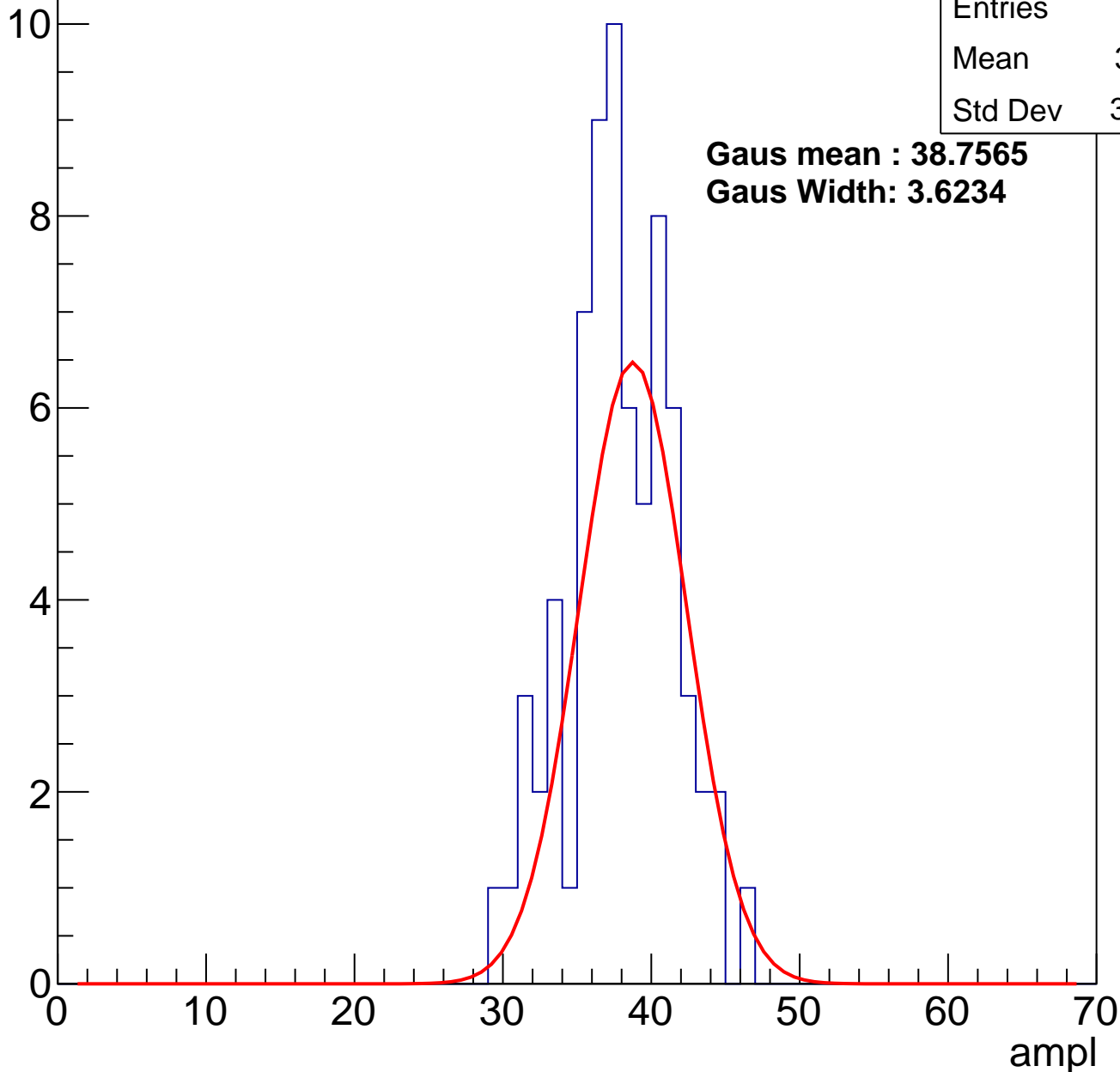
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	71
Mean	37.41
Std Dev	3.539

**Gaus mean : 38.7565**

**Gaus Width: 3.6234**

Entry



# B1L003S, U6-ch12, adc2

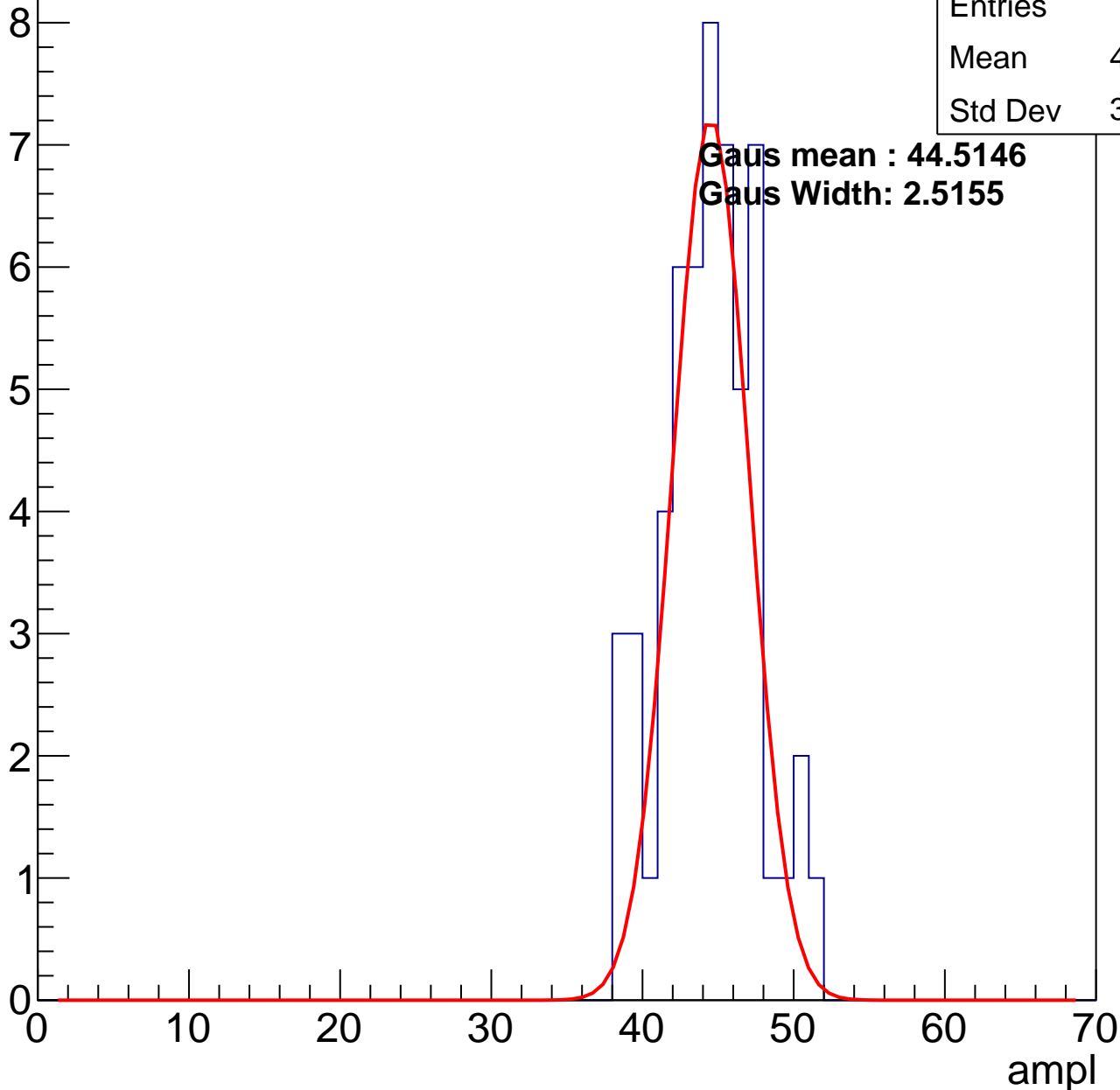
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	43.98
Std Dev	3.066

**Gaus mean : 44.5146**

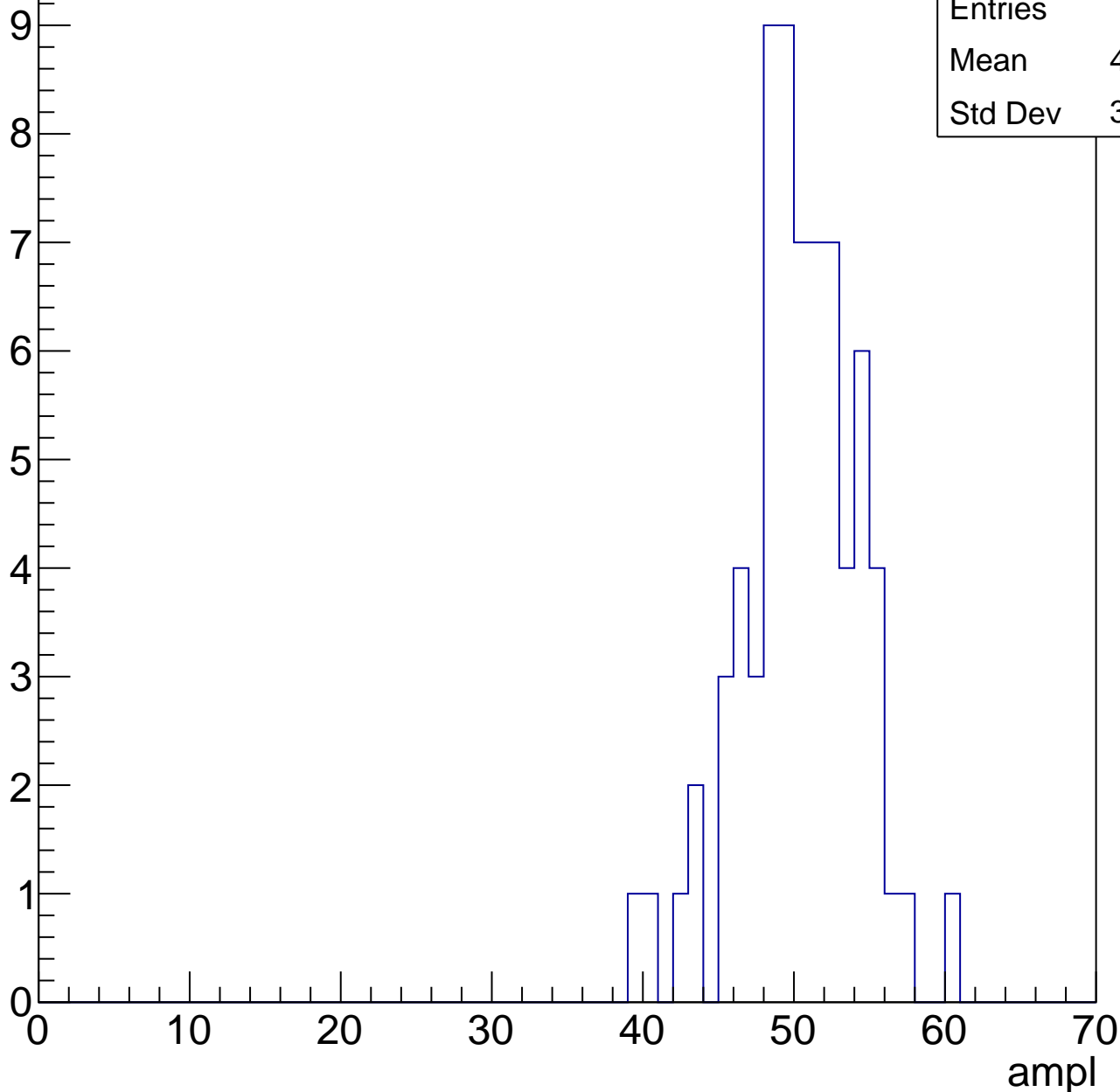
**Gaus Width: 2.5155**



# B1L003S, U6-ch12, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



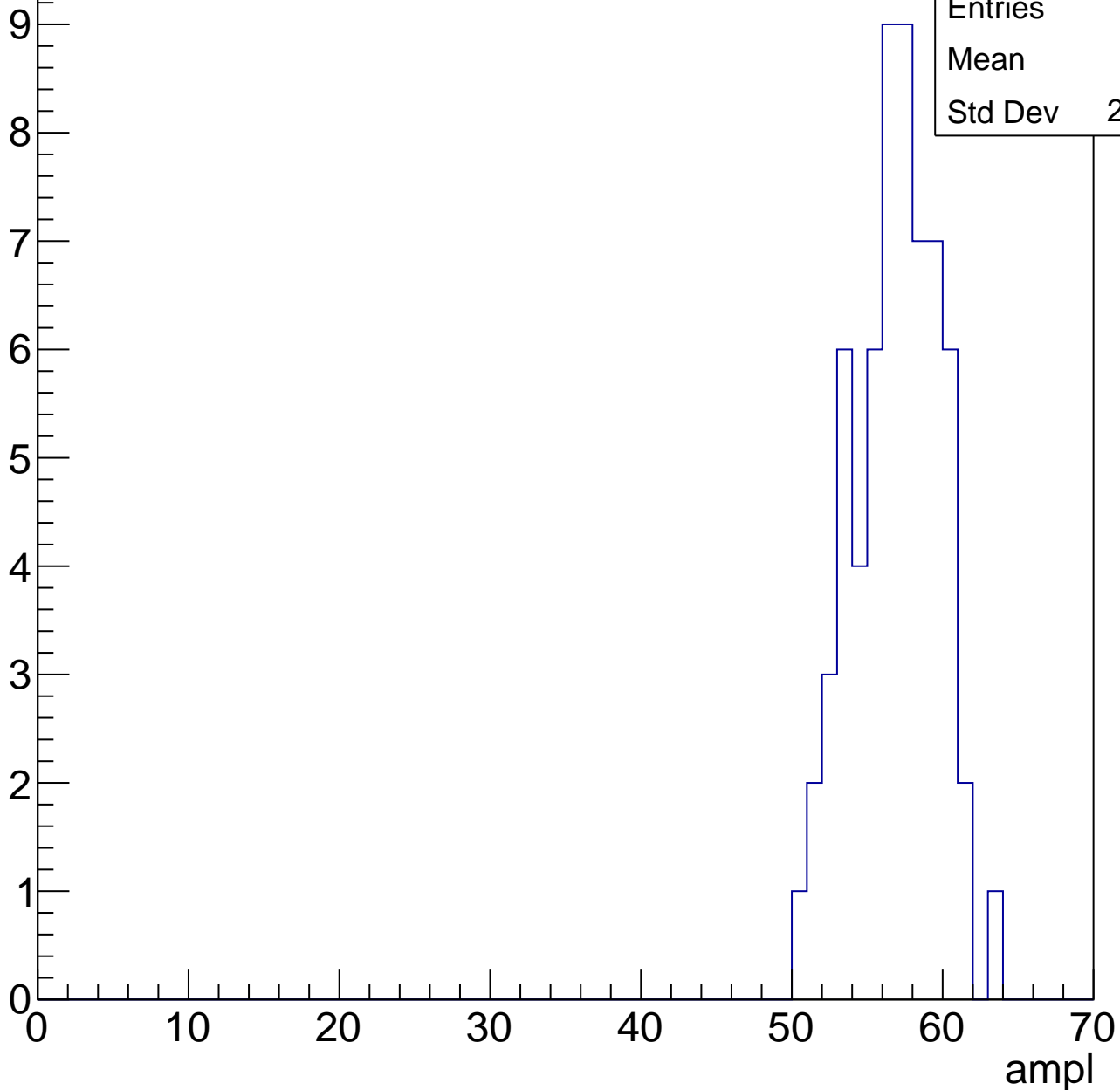
Entries	71
Mean	49.86
Std Dev	3.836

# B1L003S, U6-ch12, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

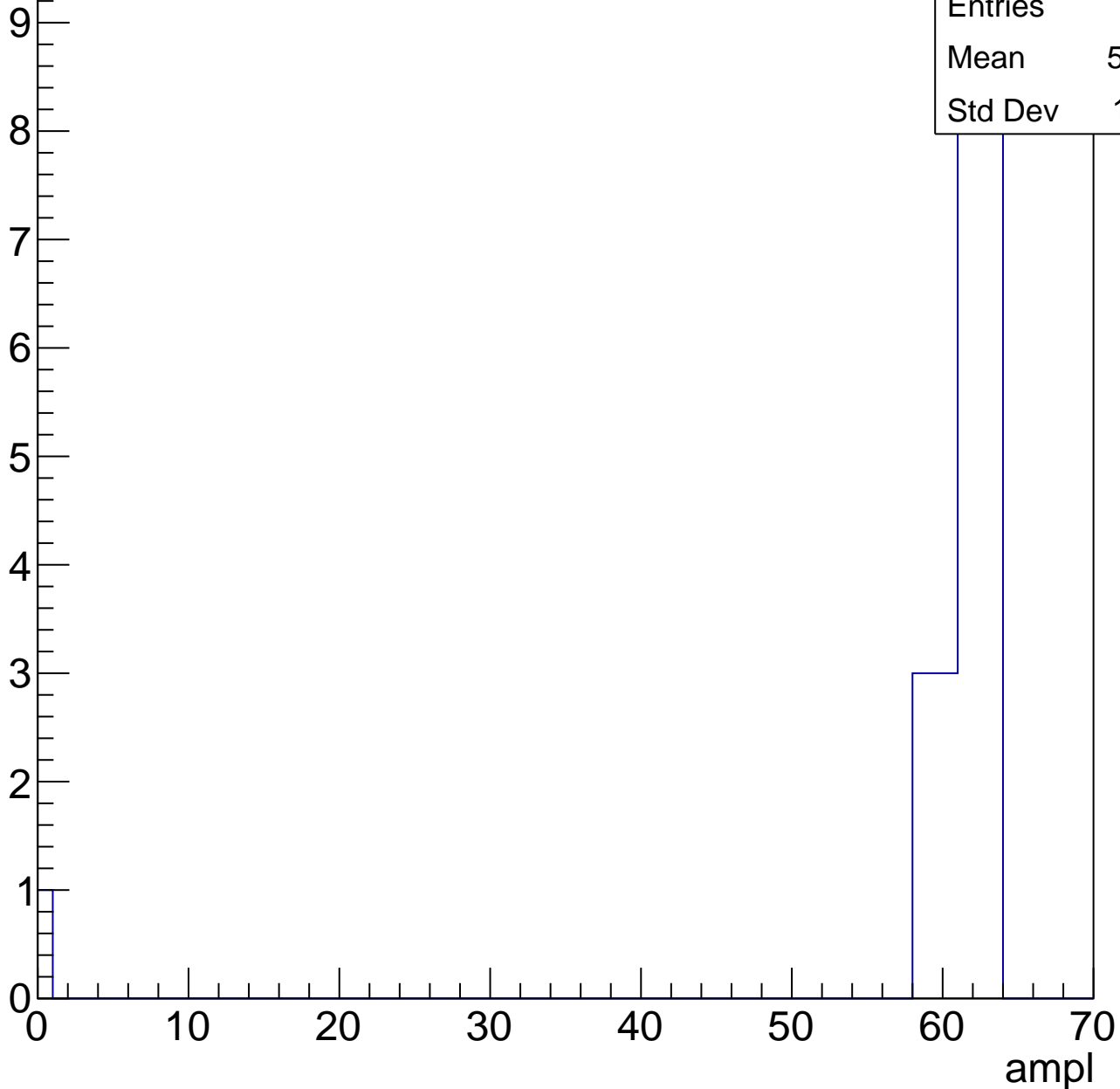
Entries	63
Mean	56.4
Std Dev	2.803



# B1L003S, U6-ch12, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch12, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

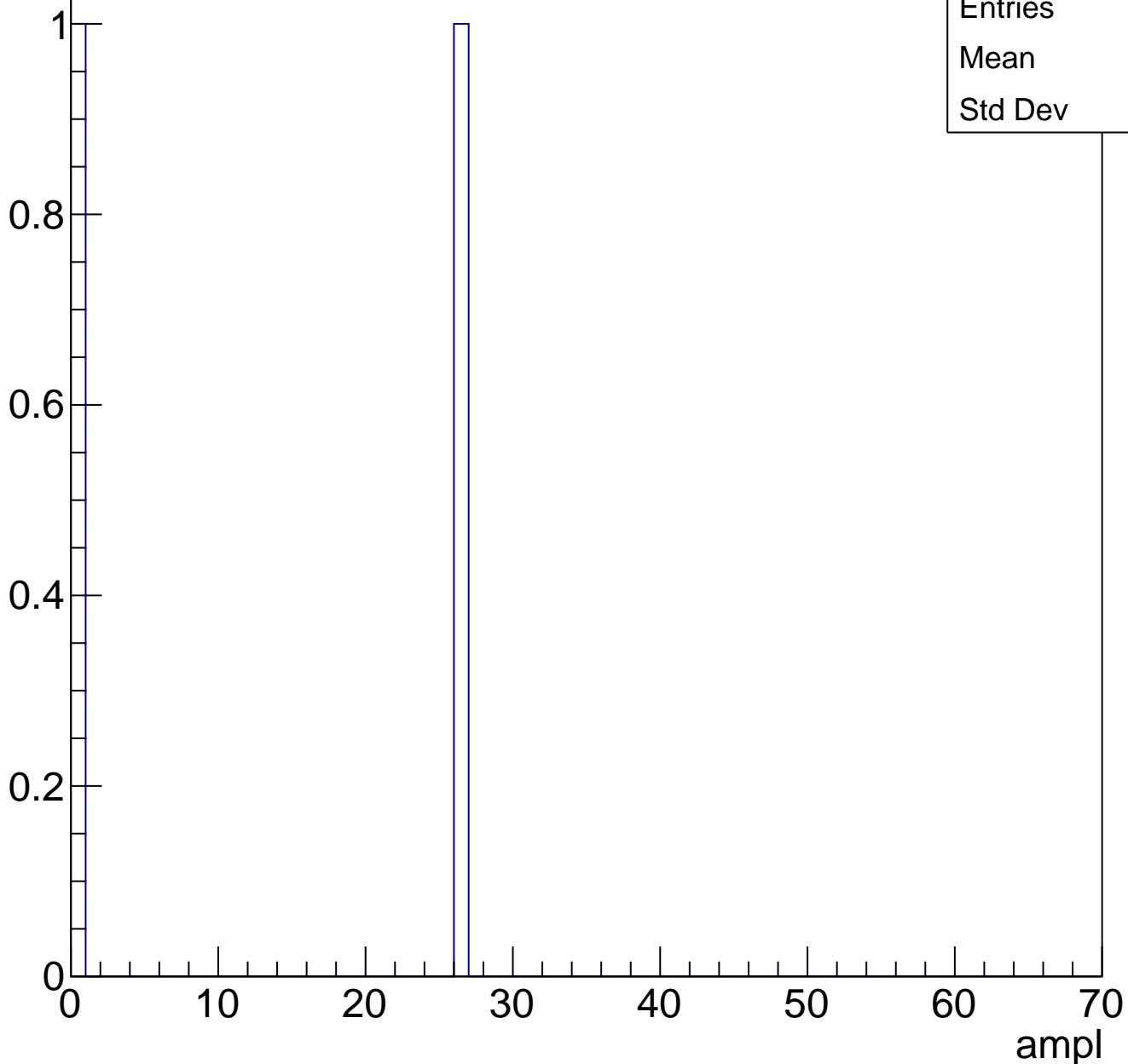




# B1L003S, U6-ch12, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	13
Std Dev	13

# B1L003S, U6-ch13, adc0

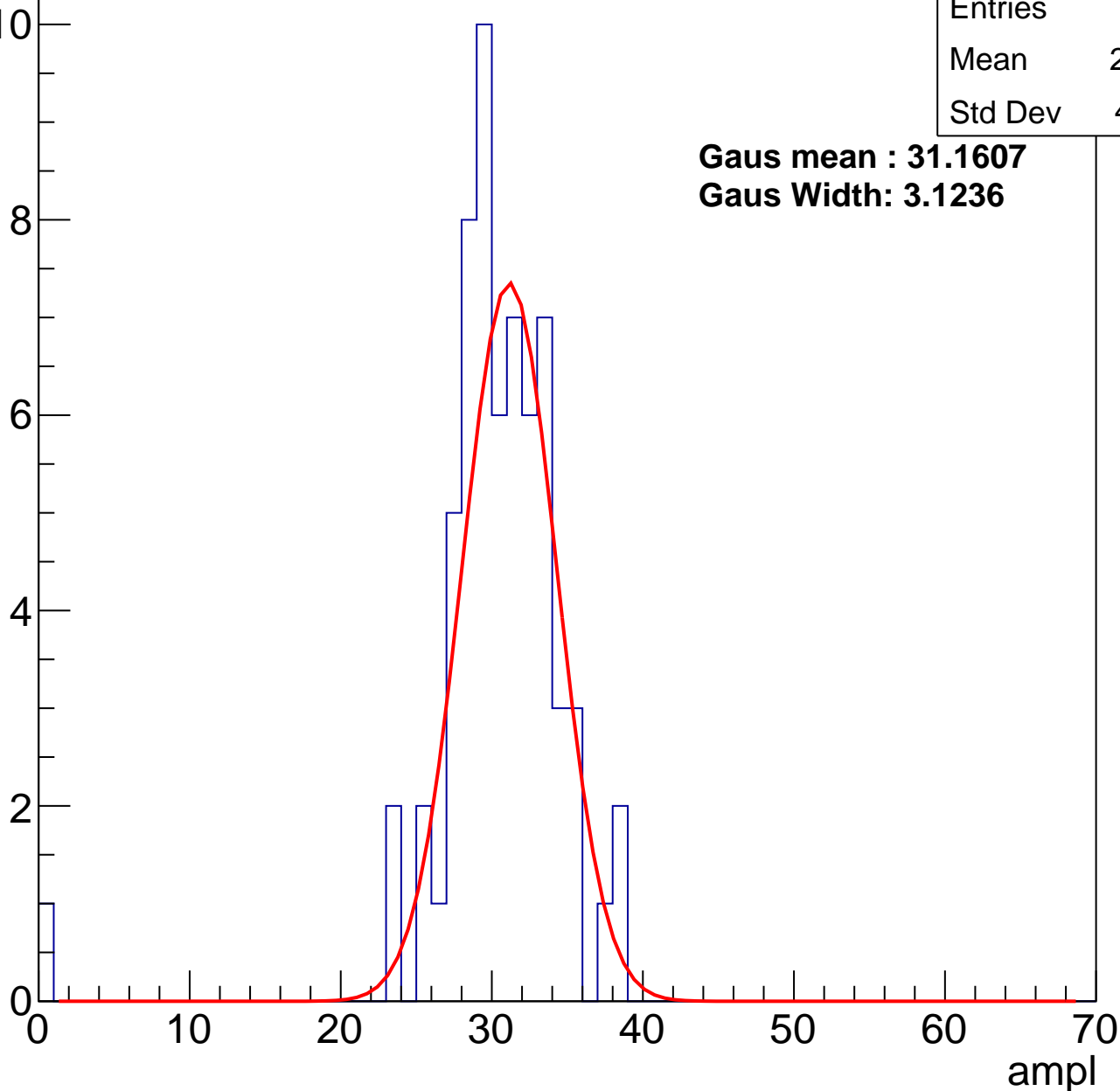
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	29.86
Std Dev	4.911

**Gaus mean : 31.1607**

**Gaus Width: 3.1236**



# B1L003S, U6-ch13, adc1

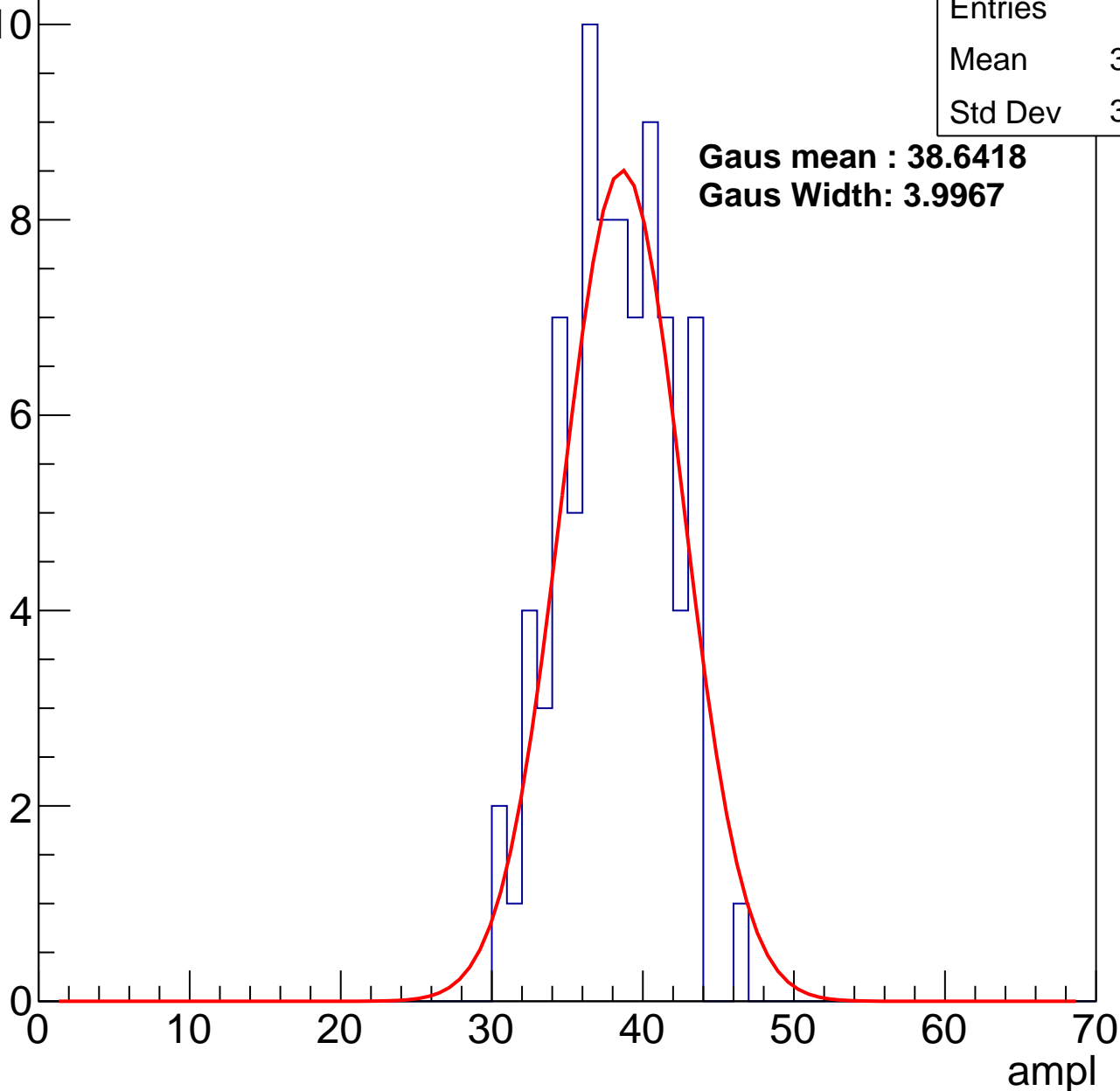
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	83
Mean	37.66
Std Dev	3.472

**Gaus mean : 38.6418**

**Gaus Width: 3.9967**



# B1L003S, U6-ch13, adc2

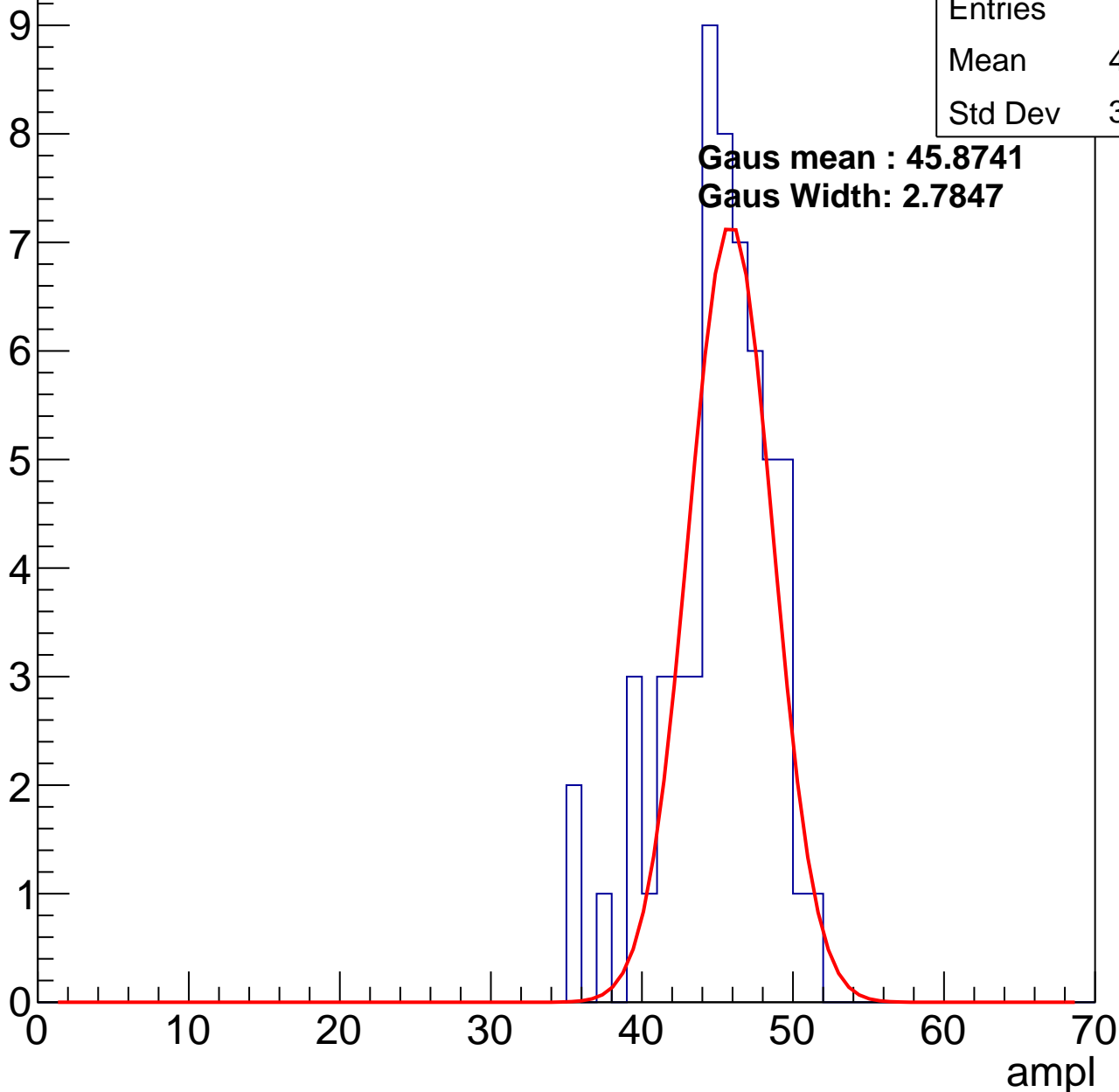
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	44.62
Std Dev	3.478

**Gaus mean : 45.8741**

**Gaus Width: 2.7847**

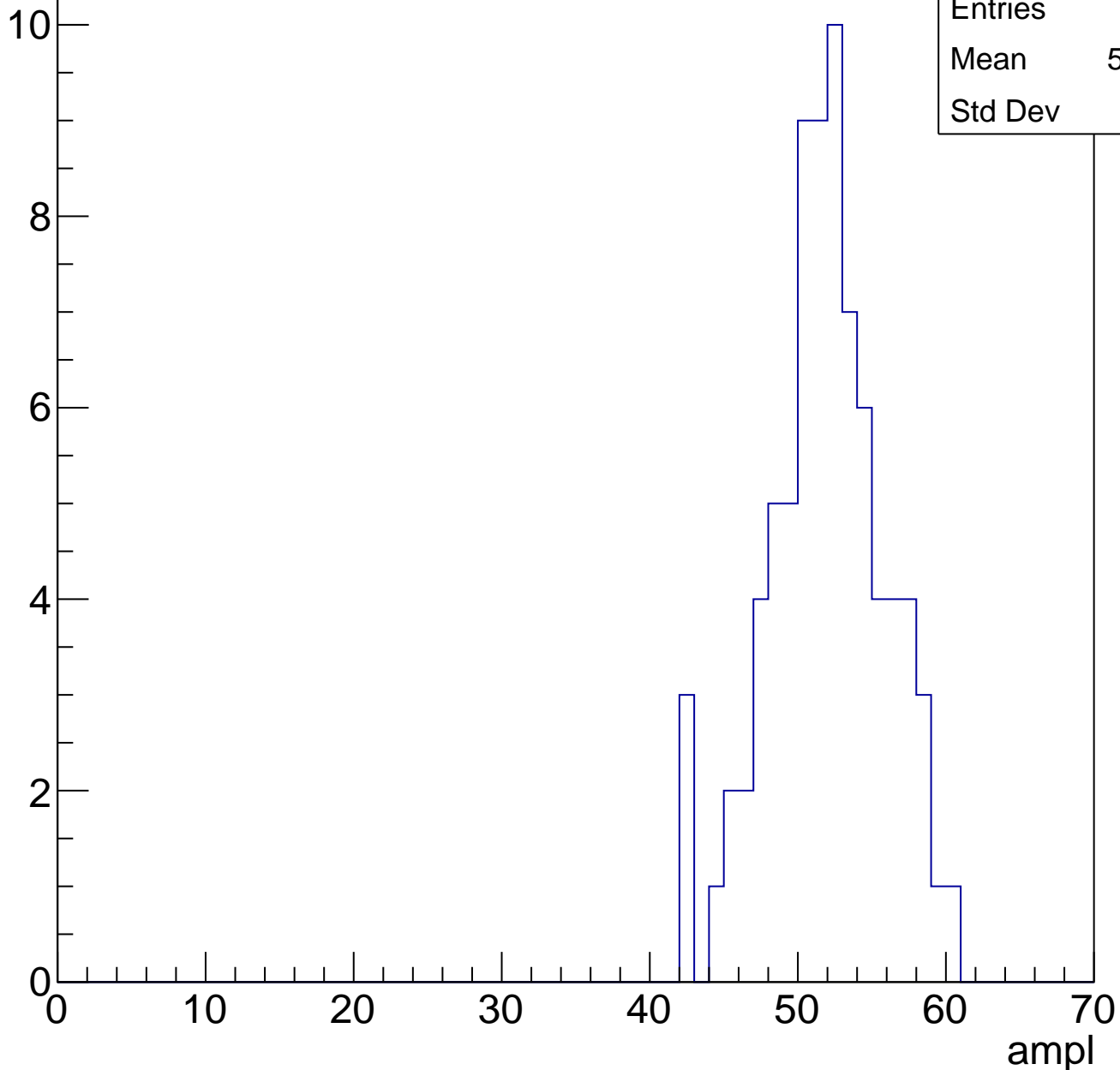


# B1L003S, U6-ch13, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	80
Mean	51.42
Std Dev	3.92

Entry

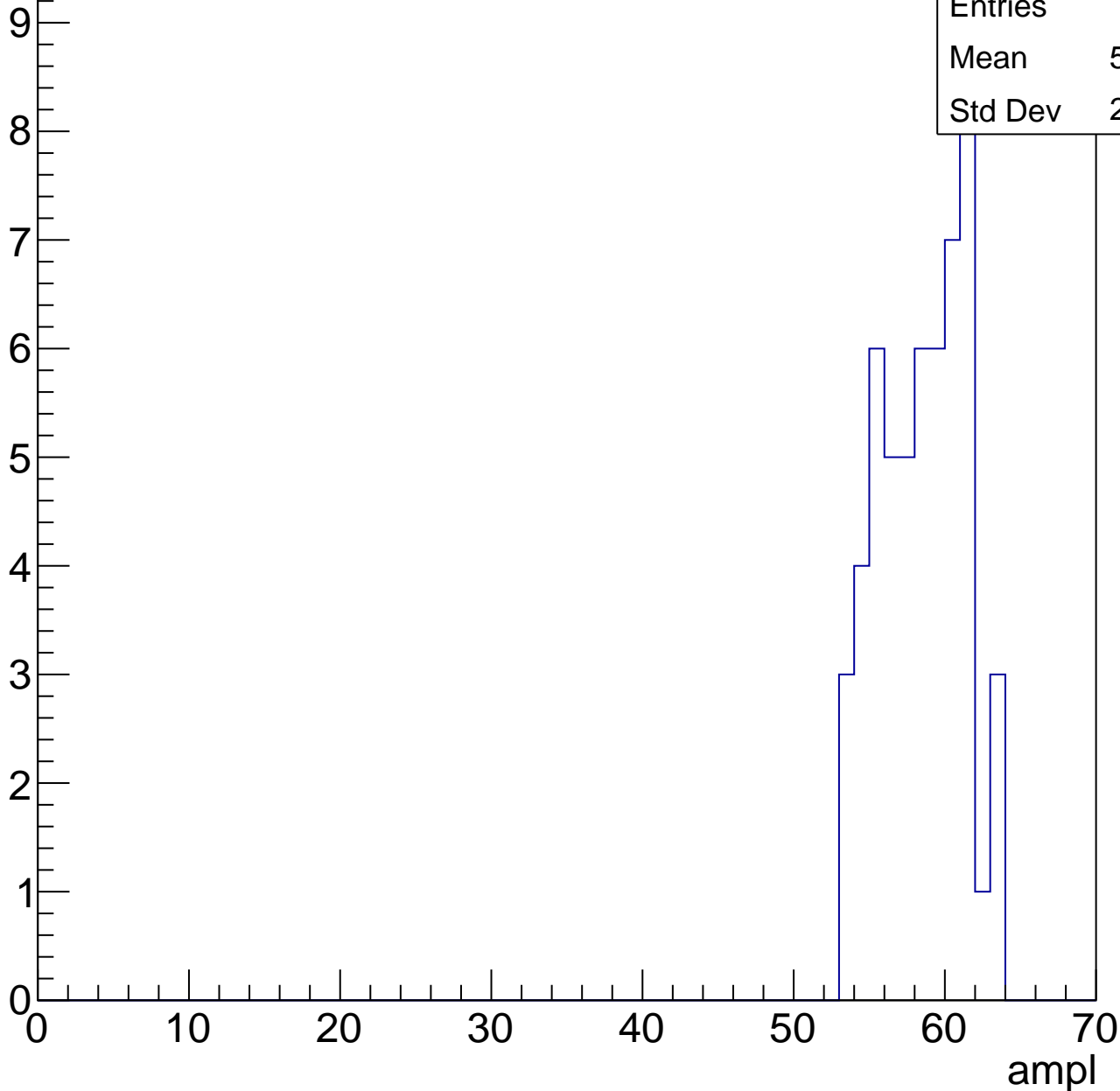


# B1L003S, U6-ch13, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	58.04
Std Dev	2.776

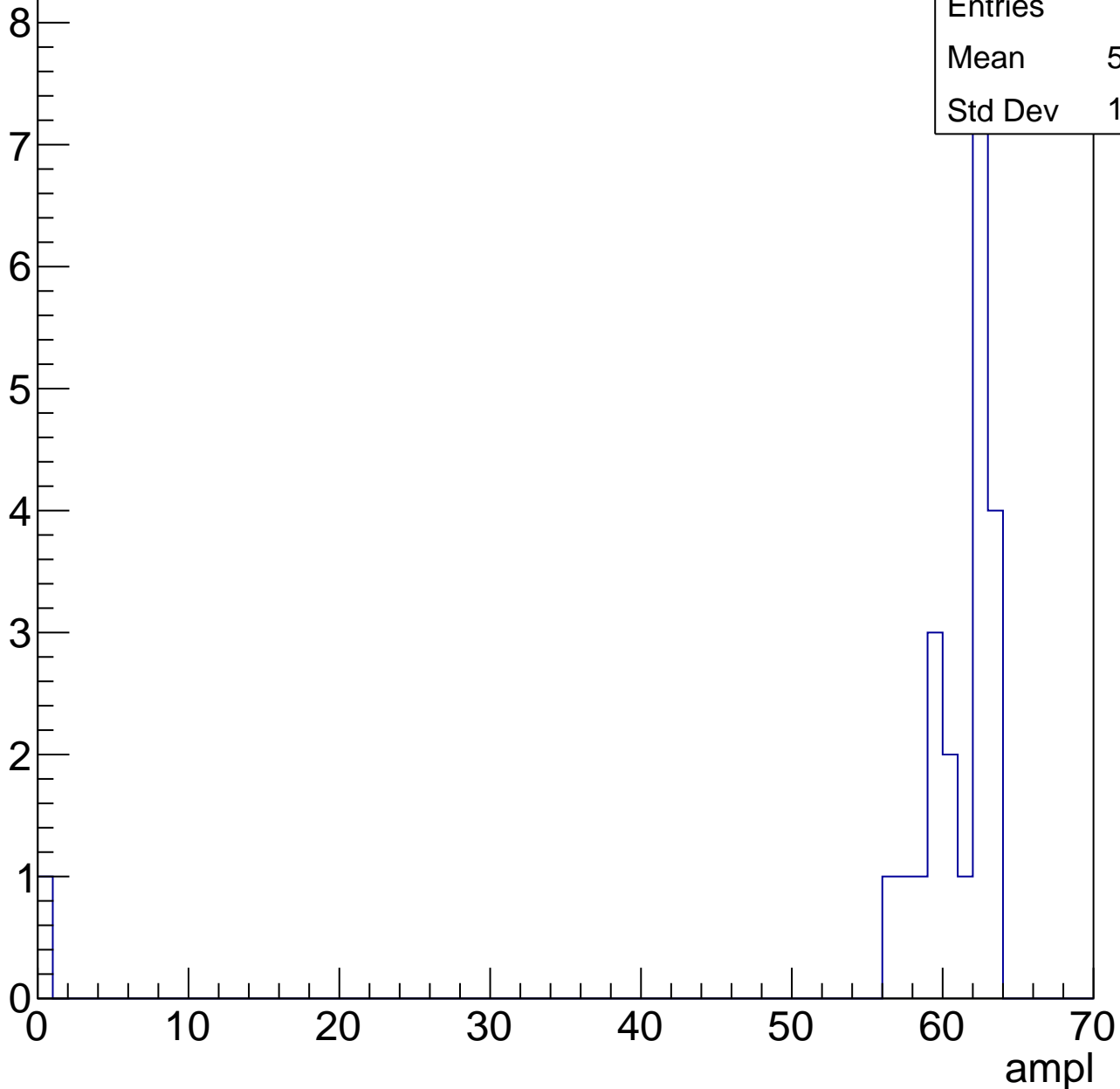


# B1L003S, U6-ch13, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

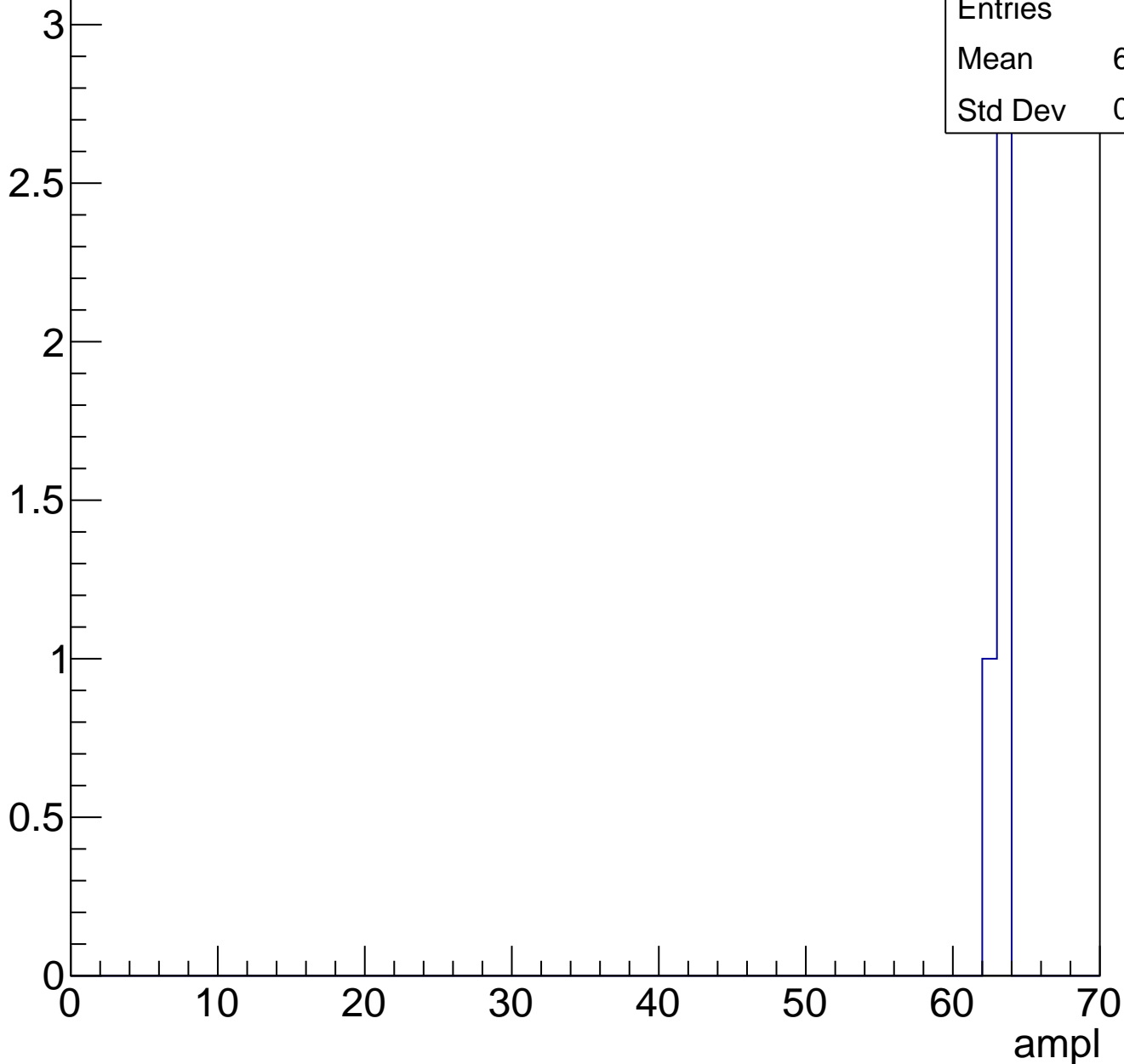
Entries	22
Mean	58.05
Std Dev	12.82



# B1L003S, U6-ch13, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch13, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

5

4

3

2

1

0

0

10

20

30

40

50

60

70

ampl

Entries

5

Mean

0

Std Dev

0

# B1L003S, U6-ch14, adc0

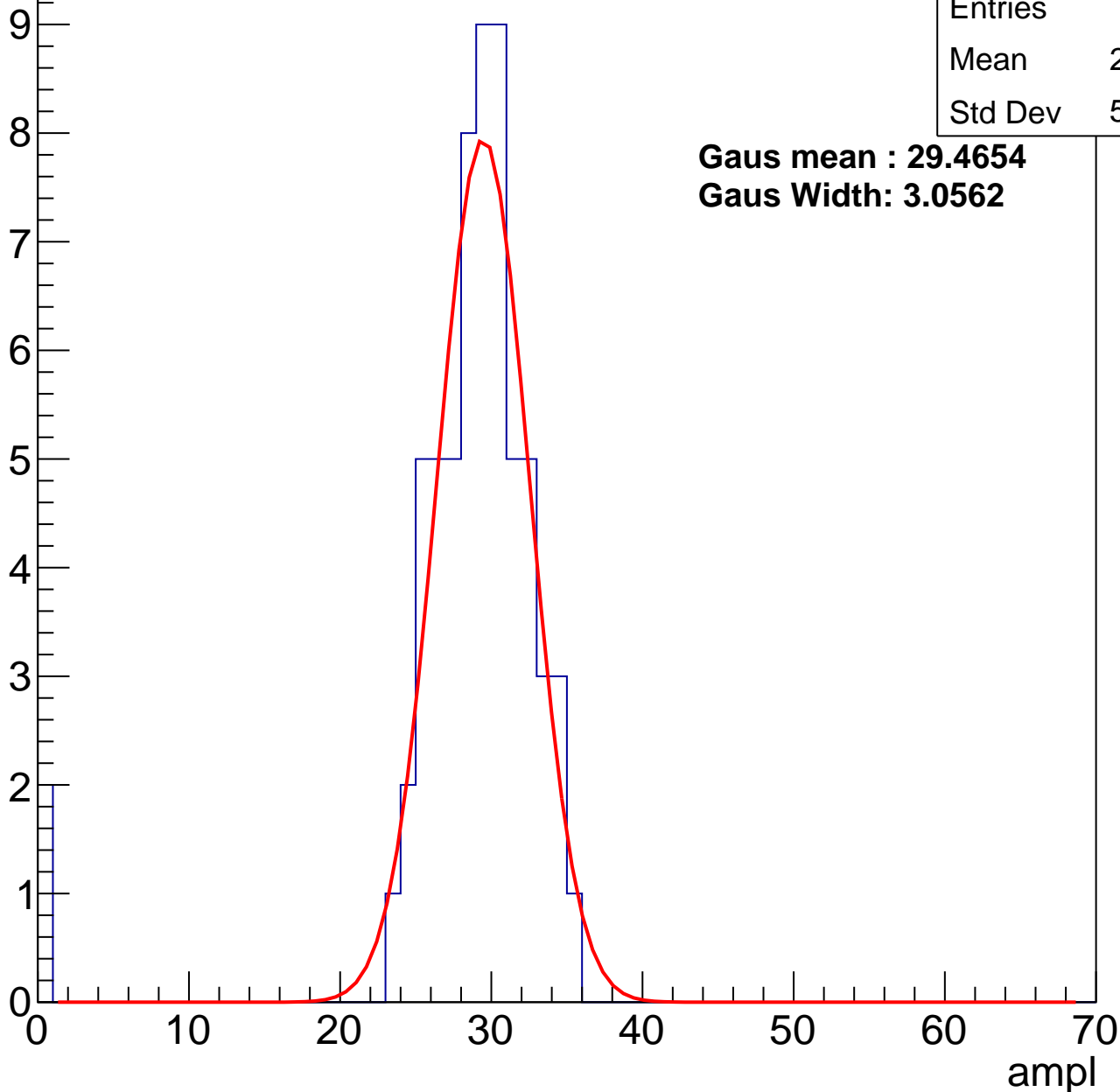
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	28.05
Std Dev	5.769

**Gaus mean : 29.4654**

**Gaus Width: 3.0562**



# B1L003S, U6-ch14, adc1

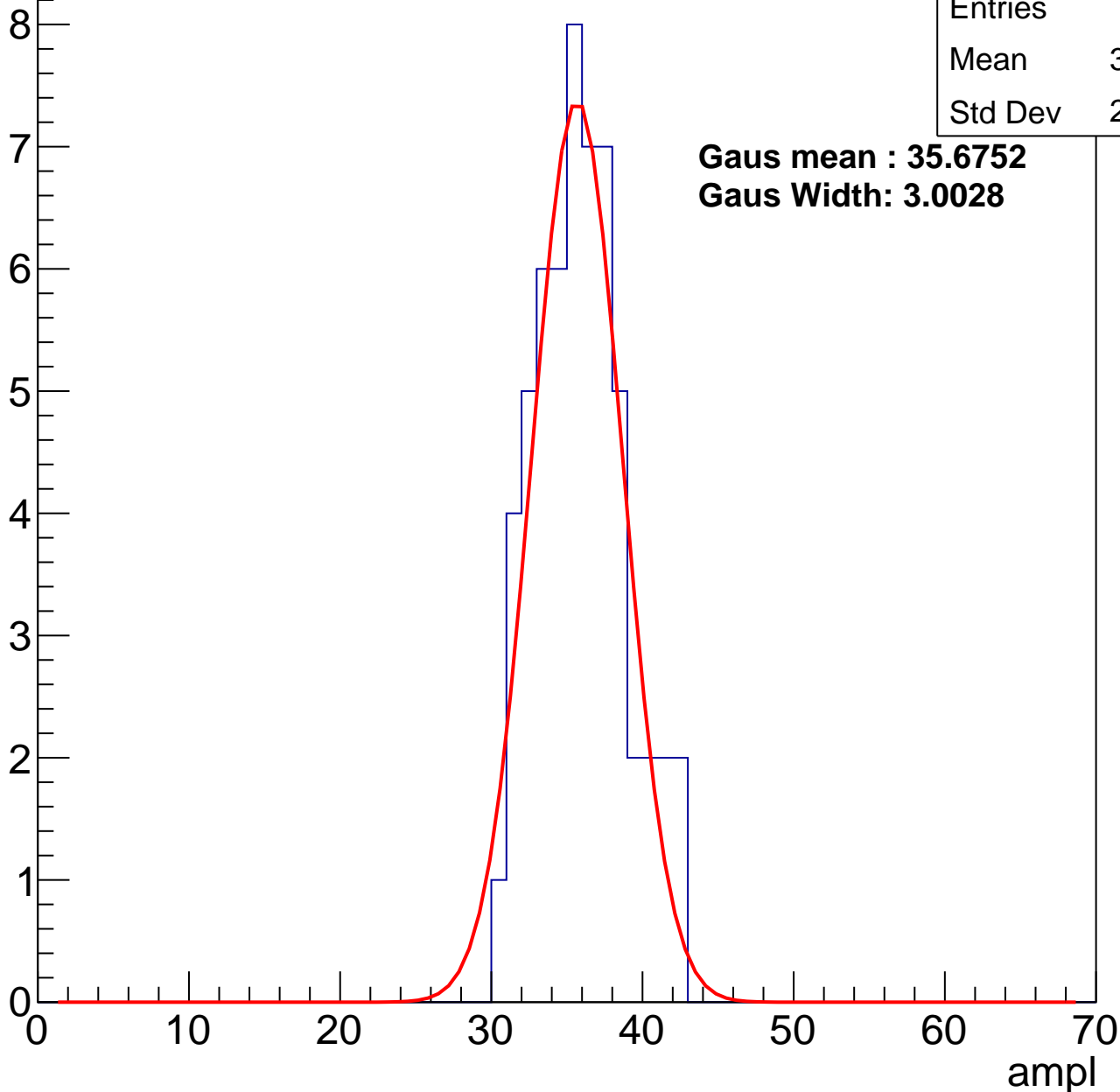
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	35.46
Std Dev	2.914

**Gaus mean : 35.6752**

**Gaus Width: 3.0028**



# B1L003S, U6-ch14, adc2

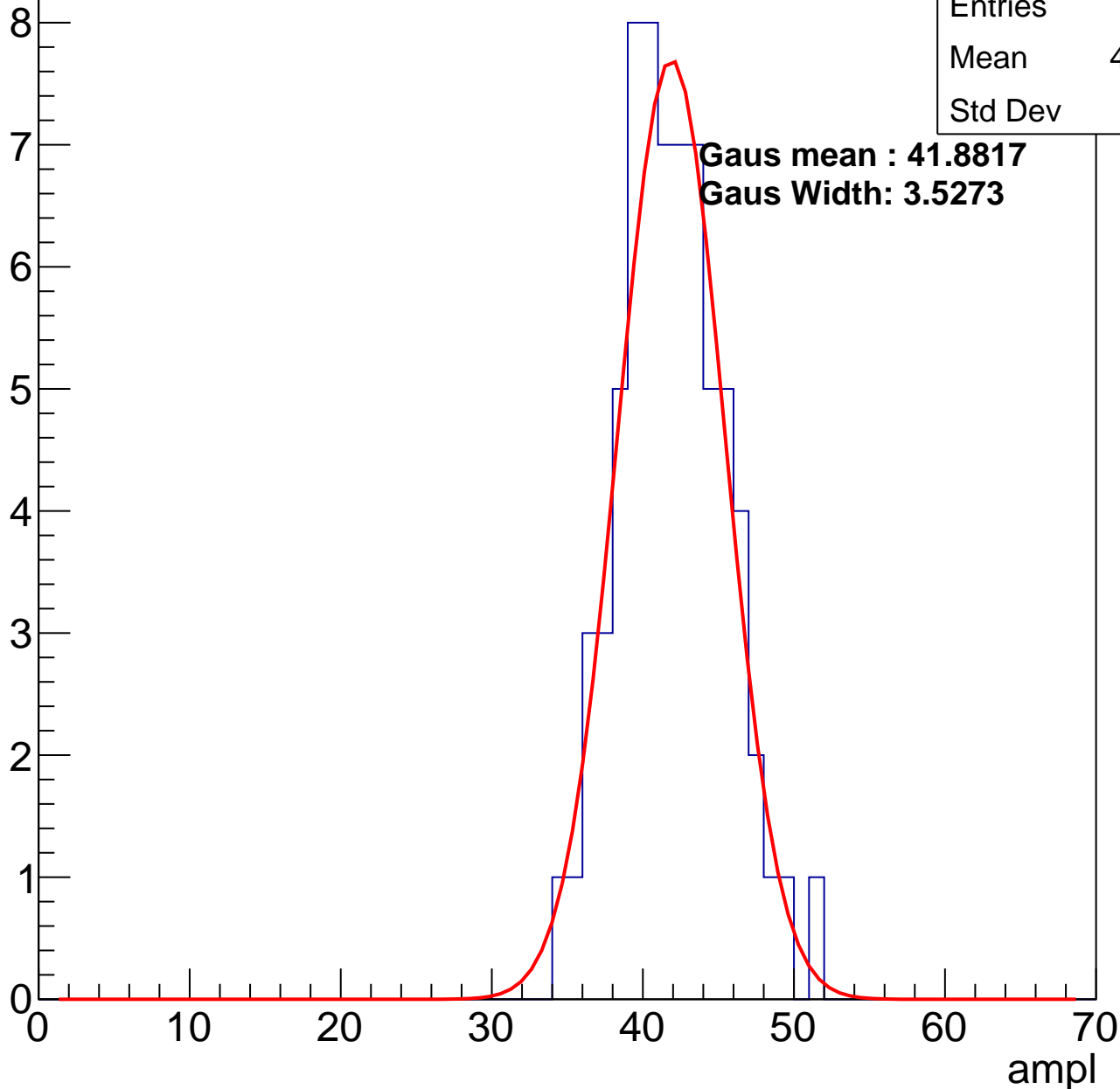
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	41.49
Std Dev	3.45

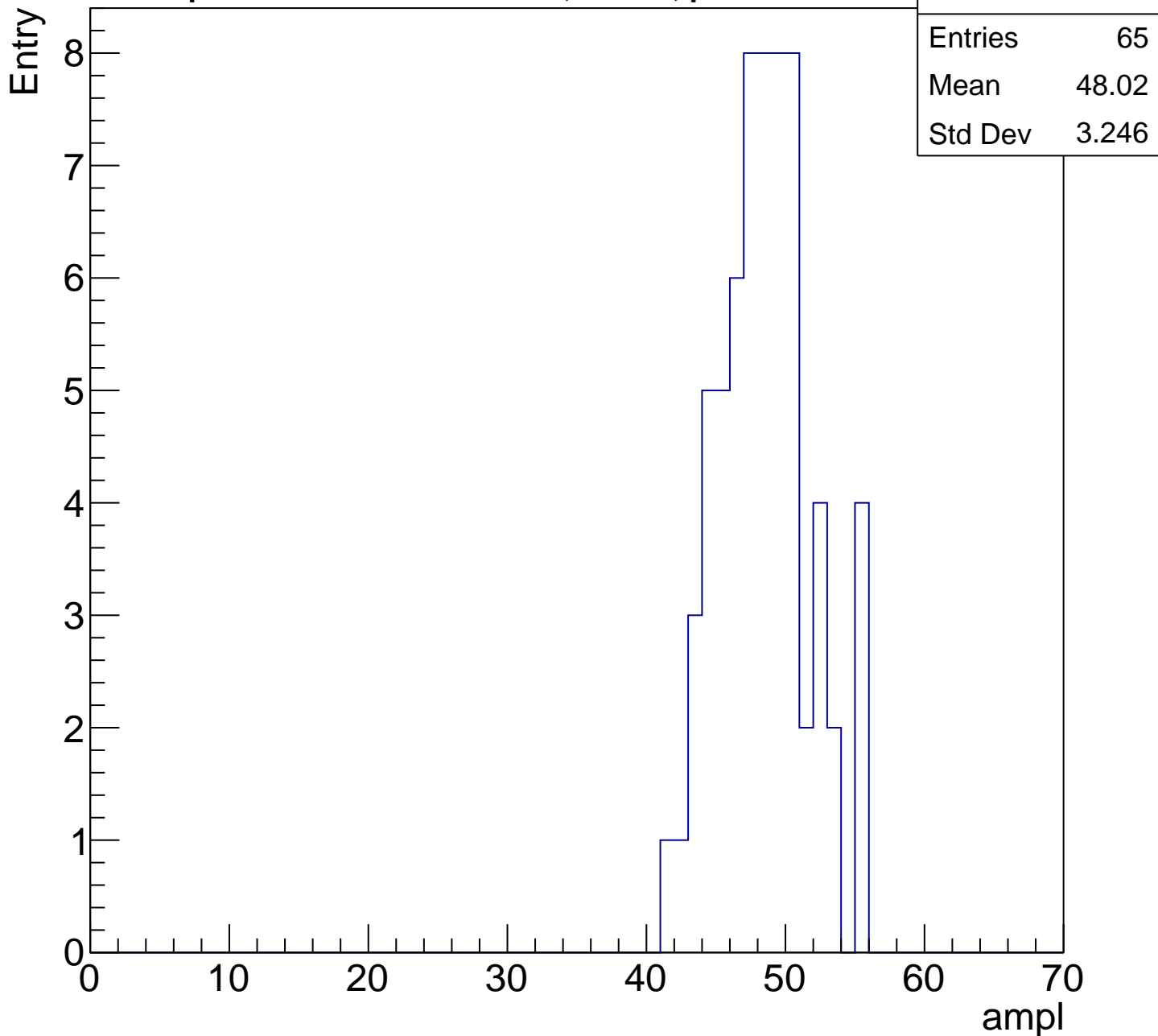
**Gaus mean : 41.8817**

**Gaus Width: 3.5273**



# B1L003S, U6-ch14, adc3

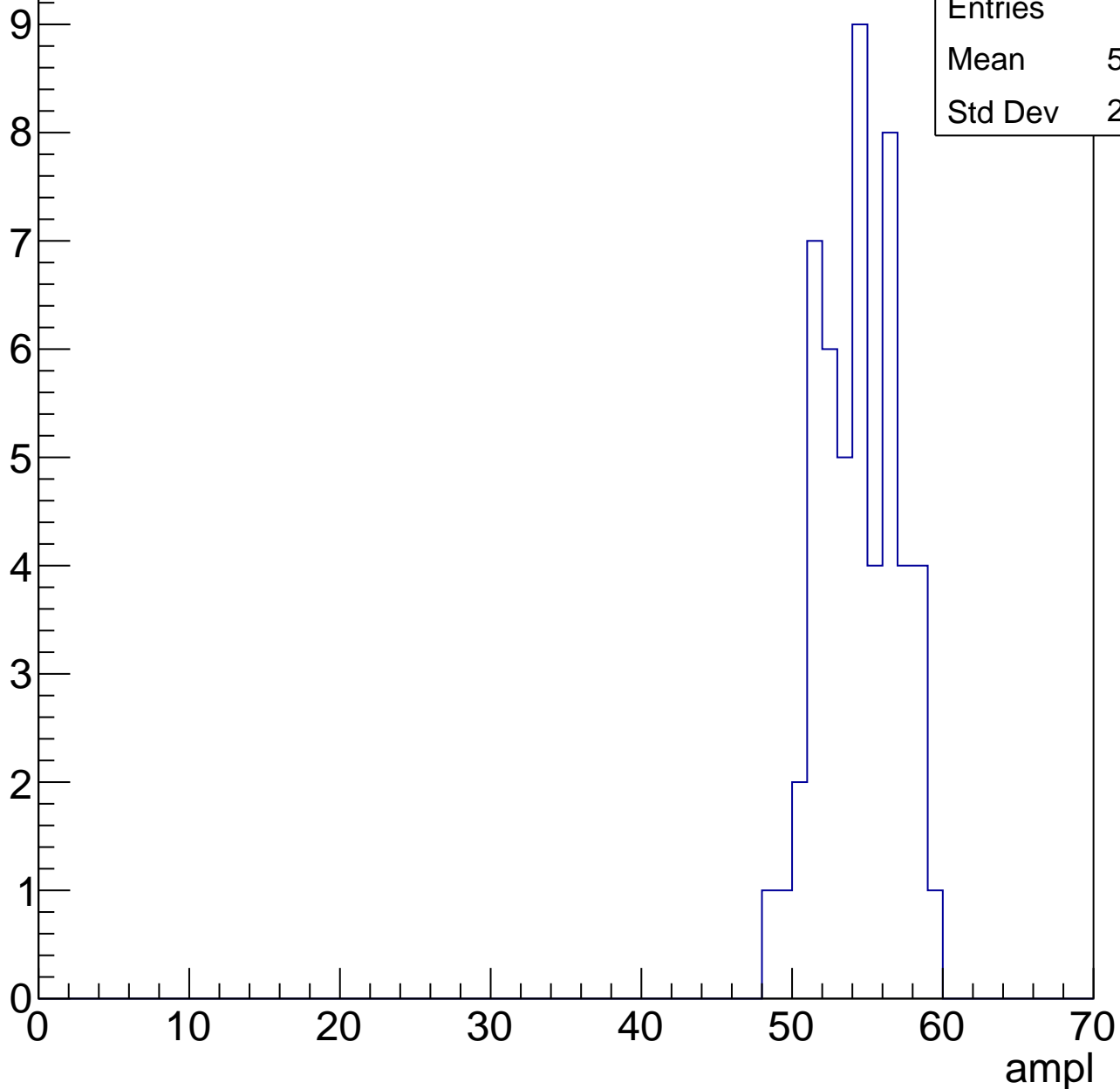
calib\_packv5\_042523\_0143.root, FC#13, port D2



# B1L003S, U6-ch14, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

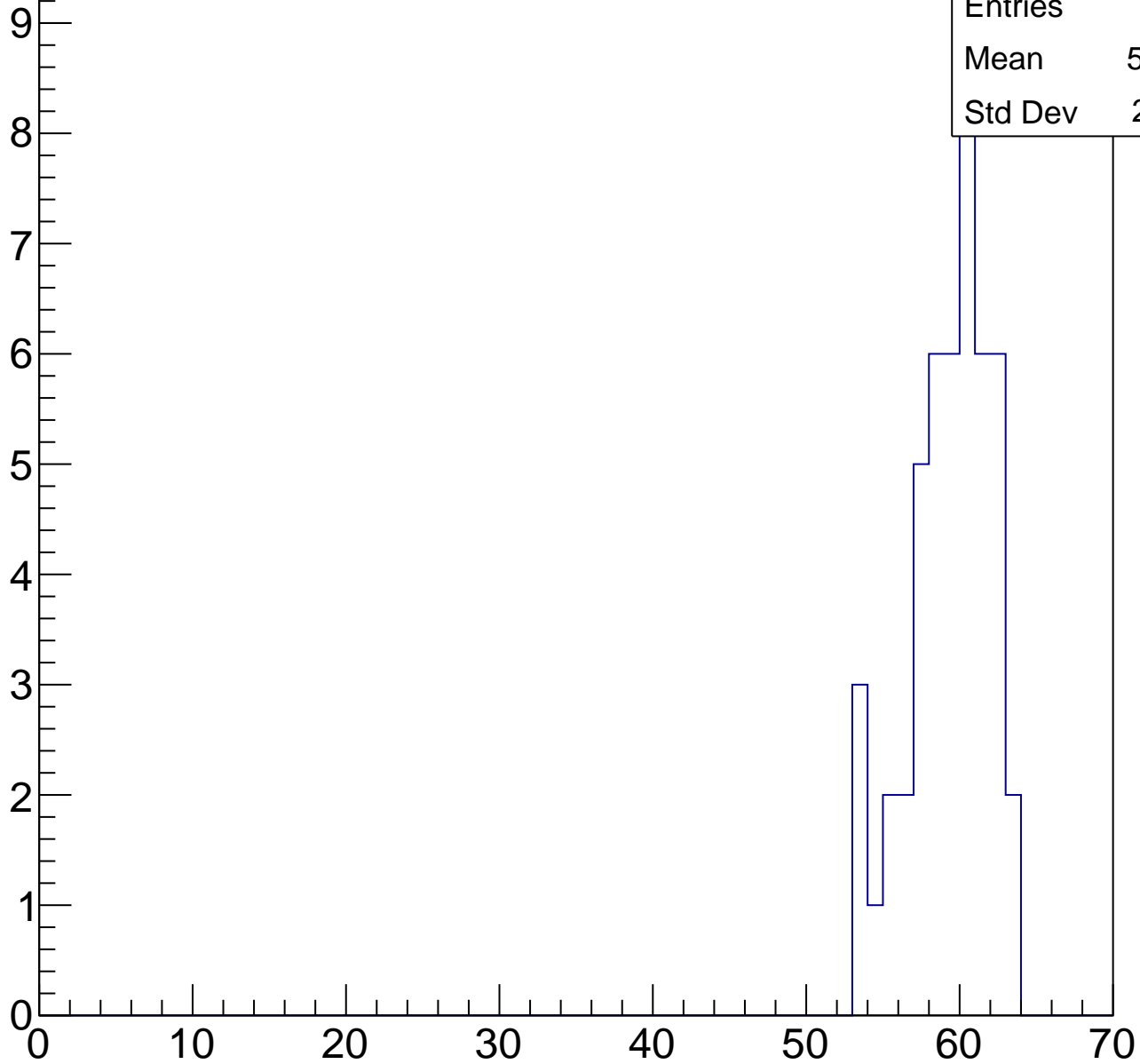


Entries	52
Mean	53.92
Std Dev	2.578

# B1L003S, U6-ch14, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	48
Mean	58.88
Std Dev	2.611

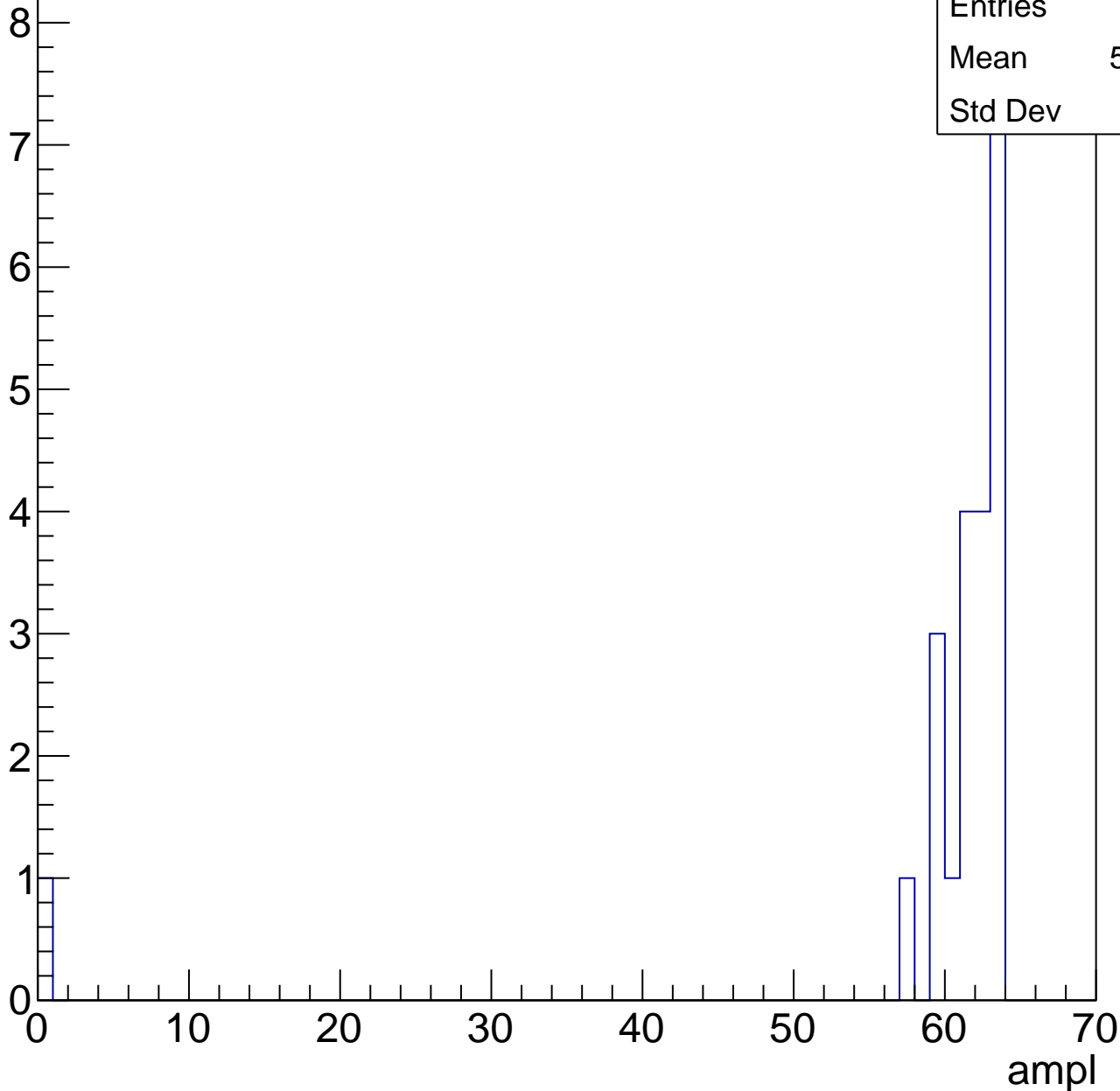
ampl

# B1L003S, U6-ch14, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	22
Mean	58.64
Std Dev	12.9





# B1L003S, U6-ch14, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U6-ch15, adc0

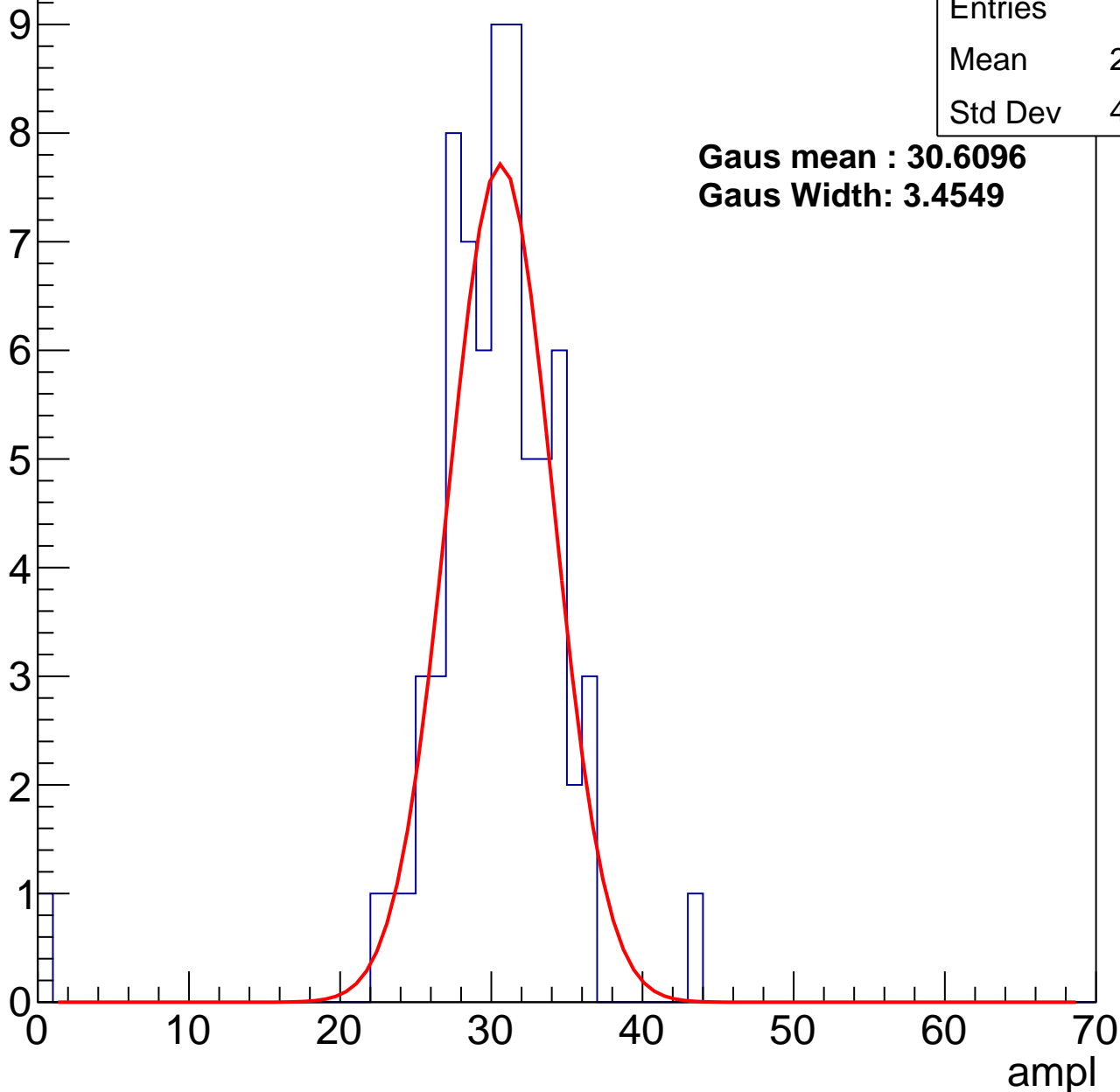
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	71
Mean	29.68
Std Dev	4.989

**Gaus mean : 30.6096**

**Gaus Width: 3.4549**



# B1L003S, U6-ch15, adc1

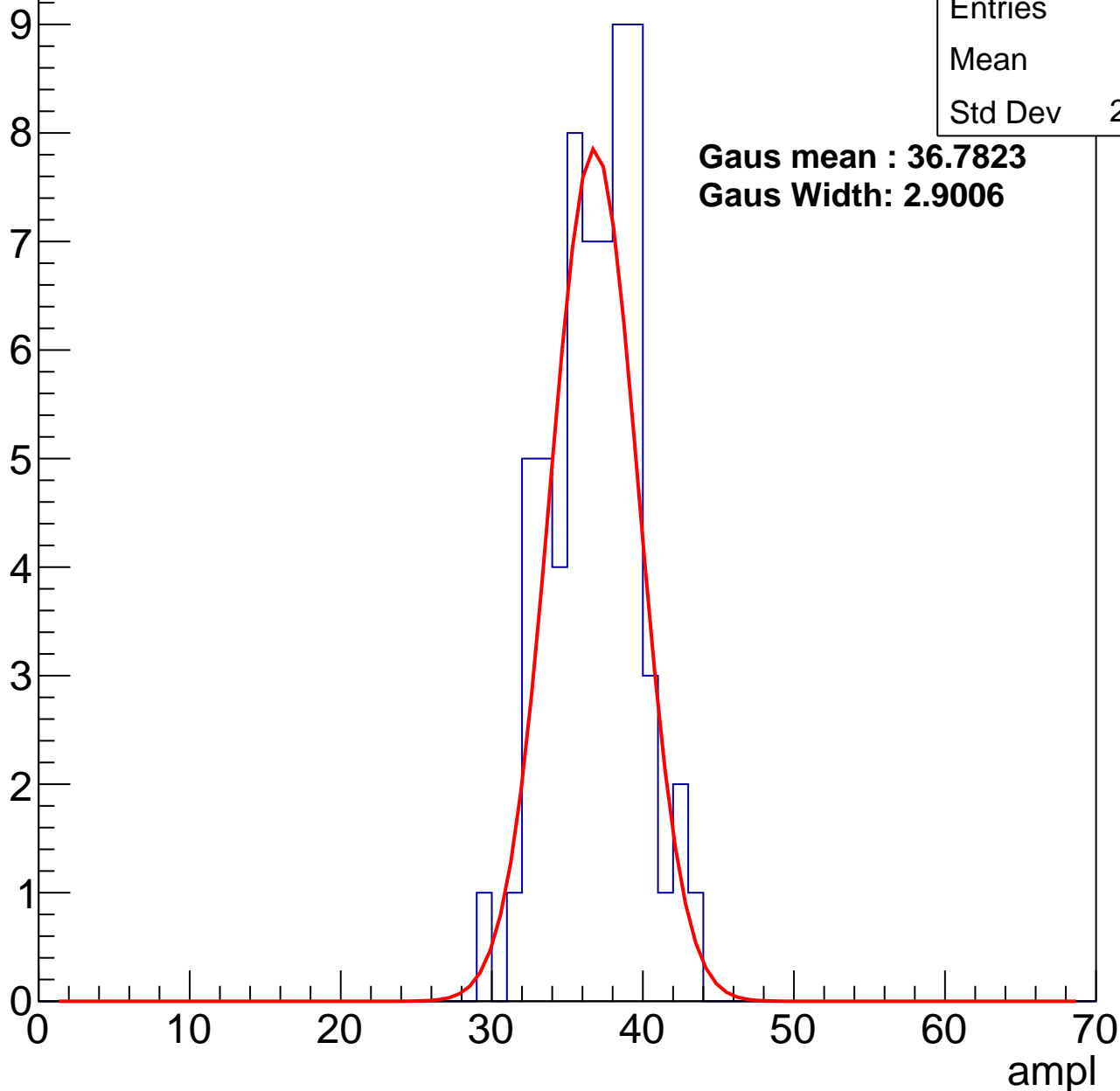
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	36.4
Std Dev	2.903

**Gaus mean : 36.7823**

**Gaus Width: 2.9006**



# B1L003S, U6-ch15, adc2

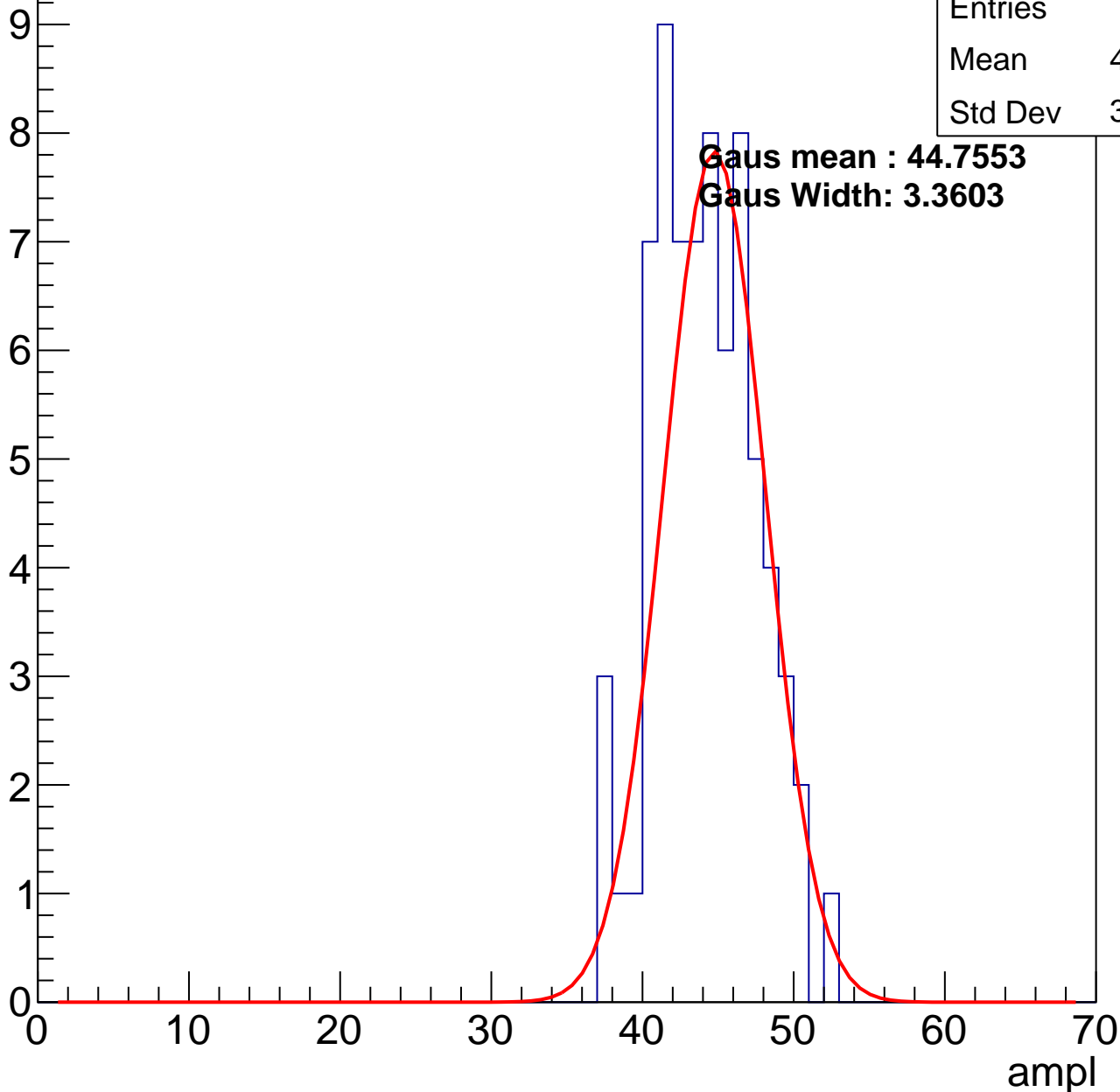
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	72
Mean	43.72
Std Dev	3.309

**Gaus mean : 44.7553**

**Gaus Width: 3.3603**

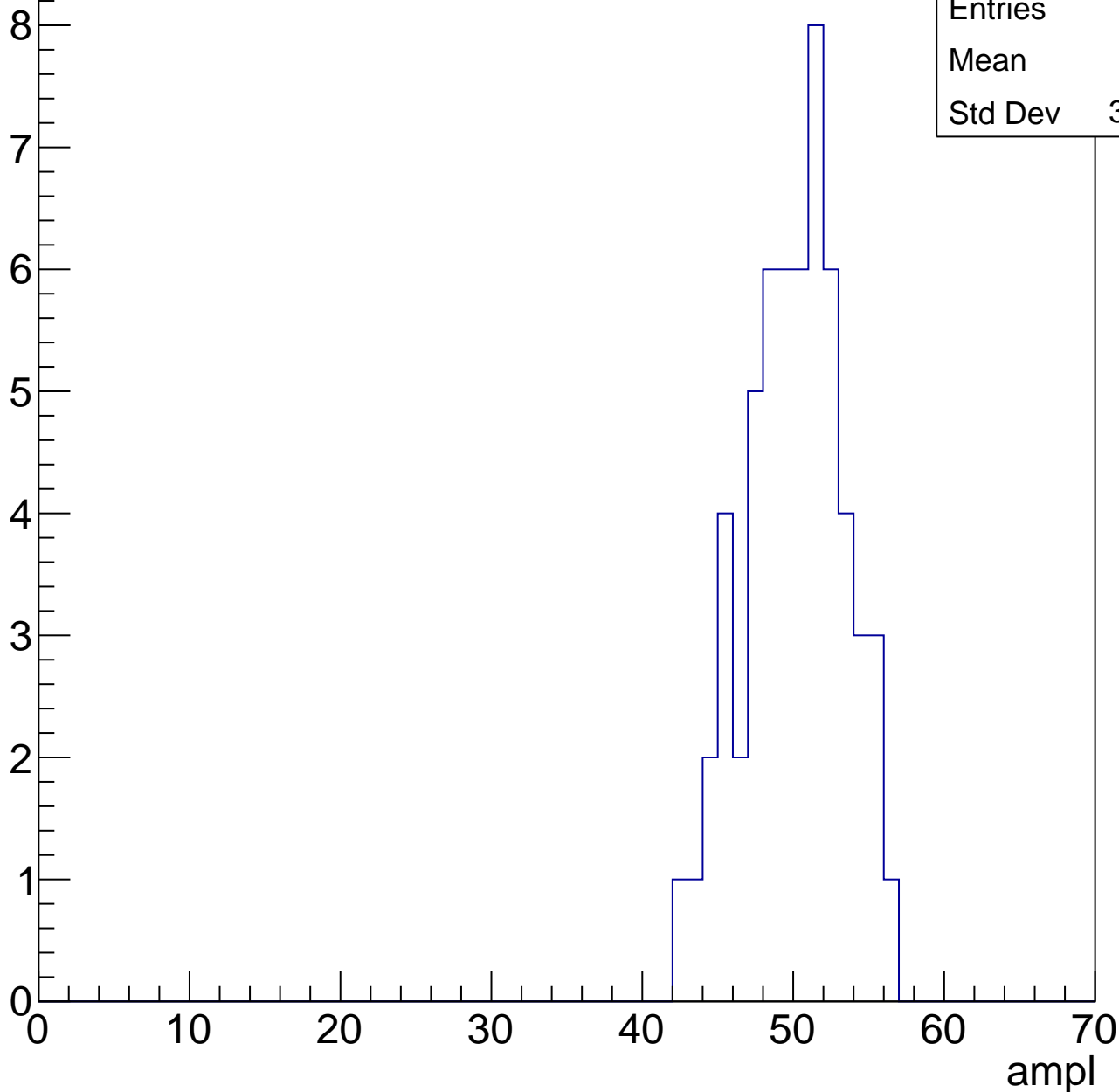


# B1L003S, U6-ch15, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	49.6
Std Dev	3.243



# B1L003S, U6-ch15, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

7

6

5

4

3

2

1

0

Entries 53

Mean 55.53

Std Dev 2.95

0

0

10

20

30

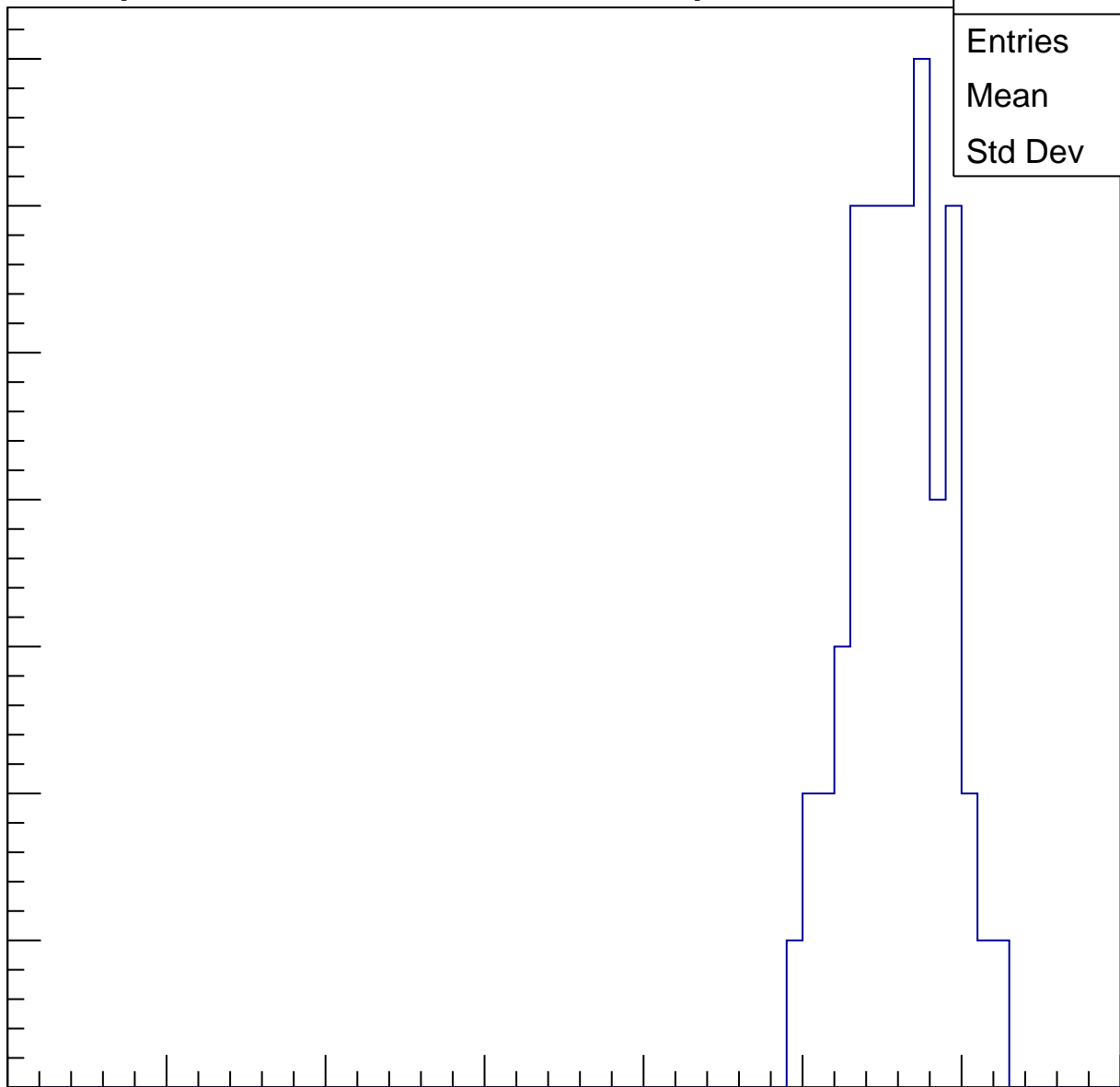
40

50

60

70

ampl

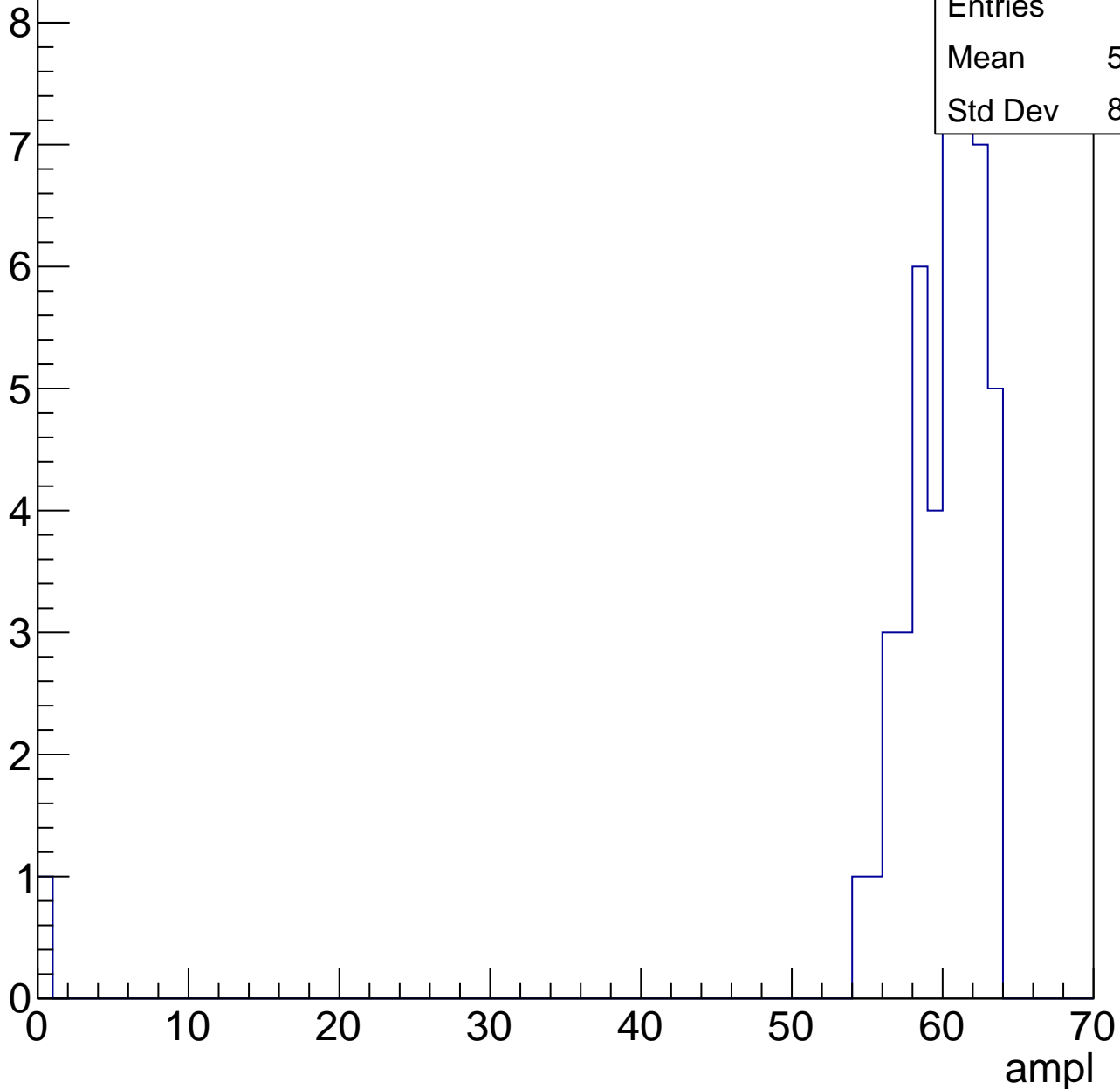


# B1L003S, U6-ch15, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	47
Mean	58.49
Std Dev	8.918

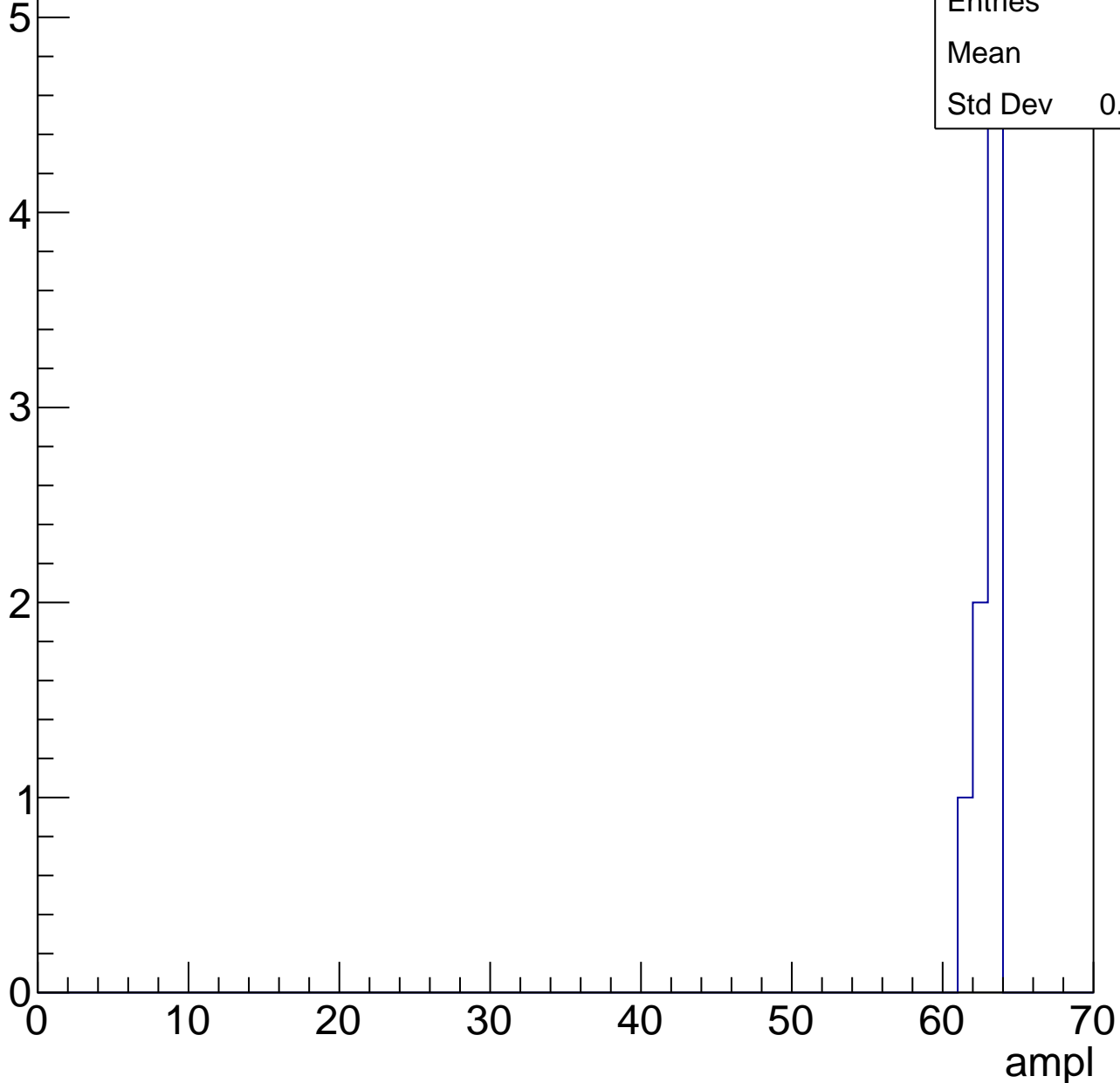


# B1L003S, U6-ch15, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	8
Mean	62.5
Std Dev	0.7071





# B1L003S, U6-ch15, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L003S, U6-ch16, adc0

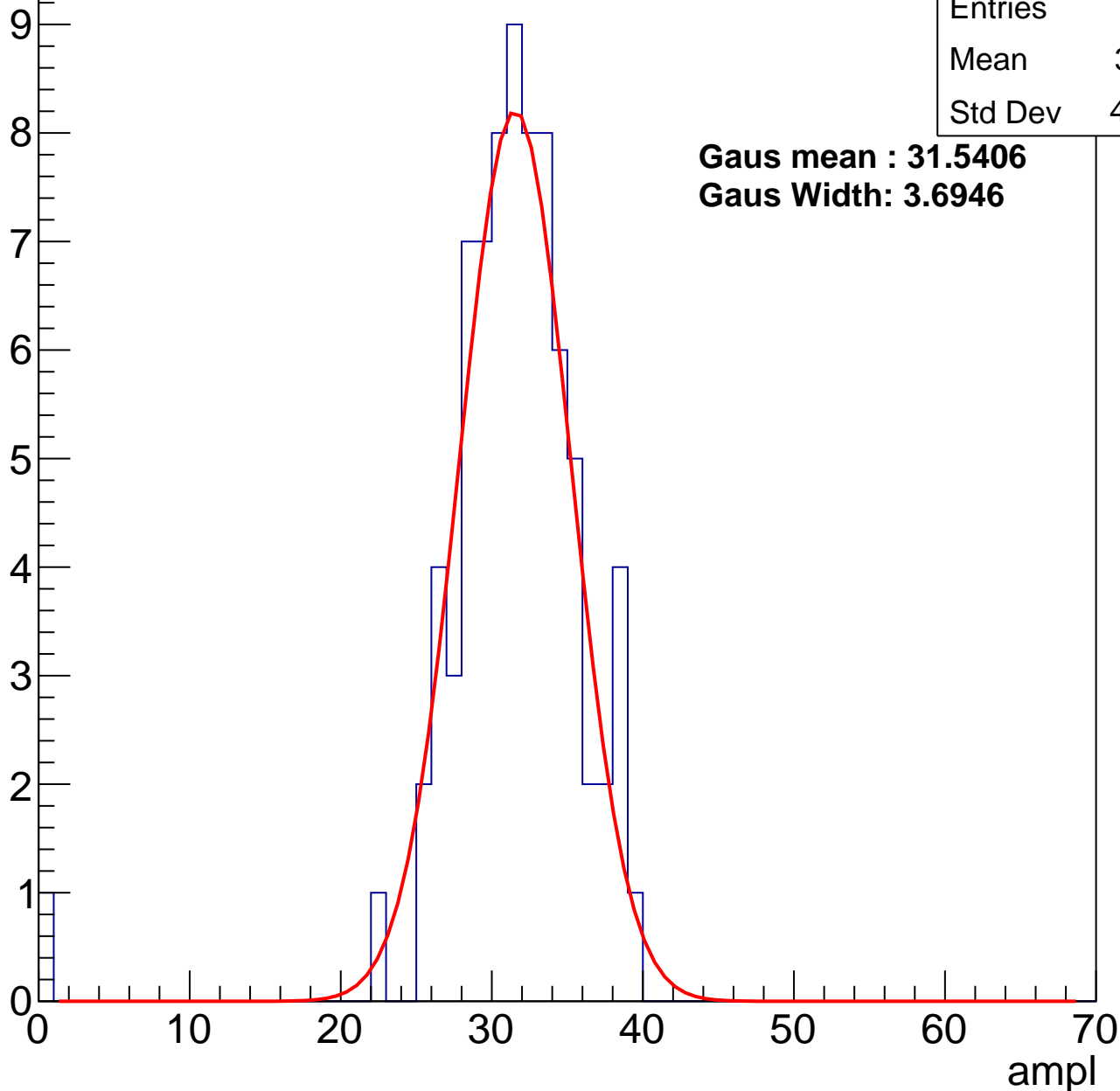
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	78
Mean	30.91
Std Dev	4.957

**Gaus mean : 31.5406**

**Gaus Width: 3.6946**



# B1L003S, U6-ch16, adc1

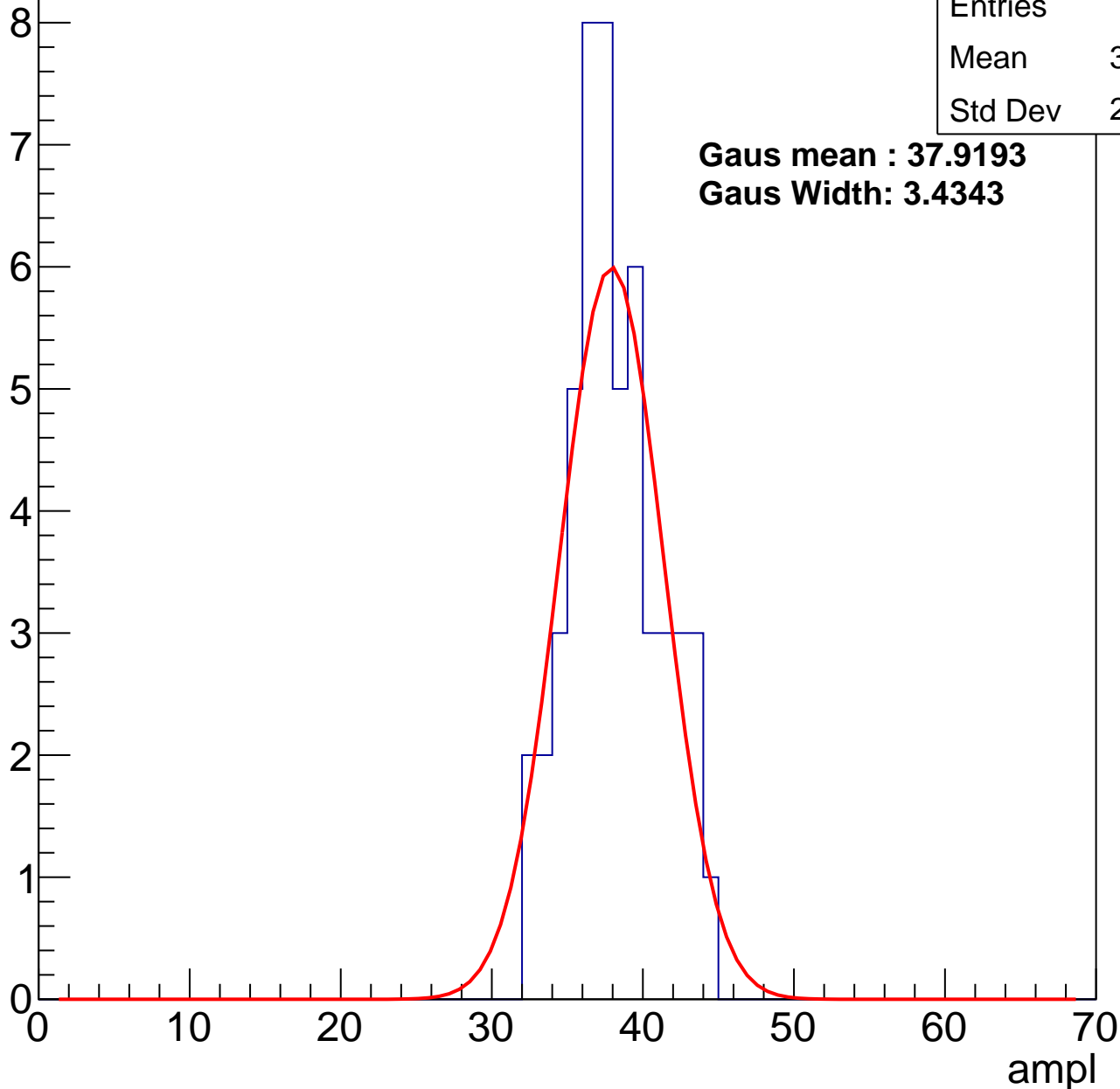
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	52
Mean	37.63
Std Dev	2.948

**Gaus mean : 37.9193**

**Gaus Width: 3.4343**

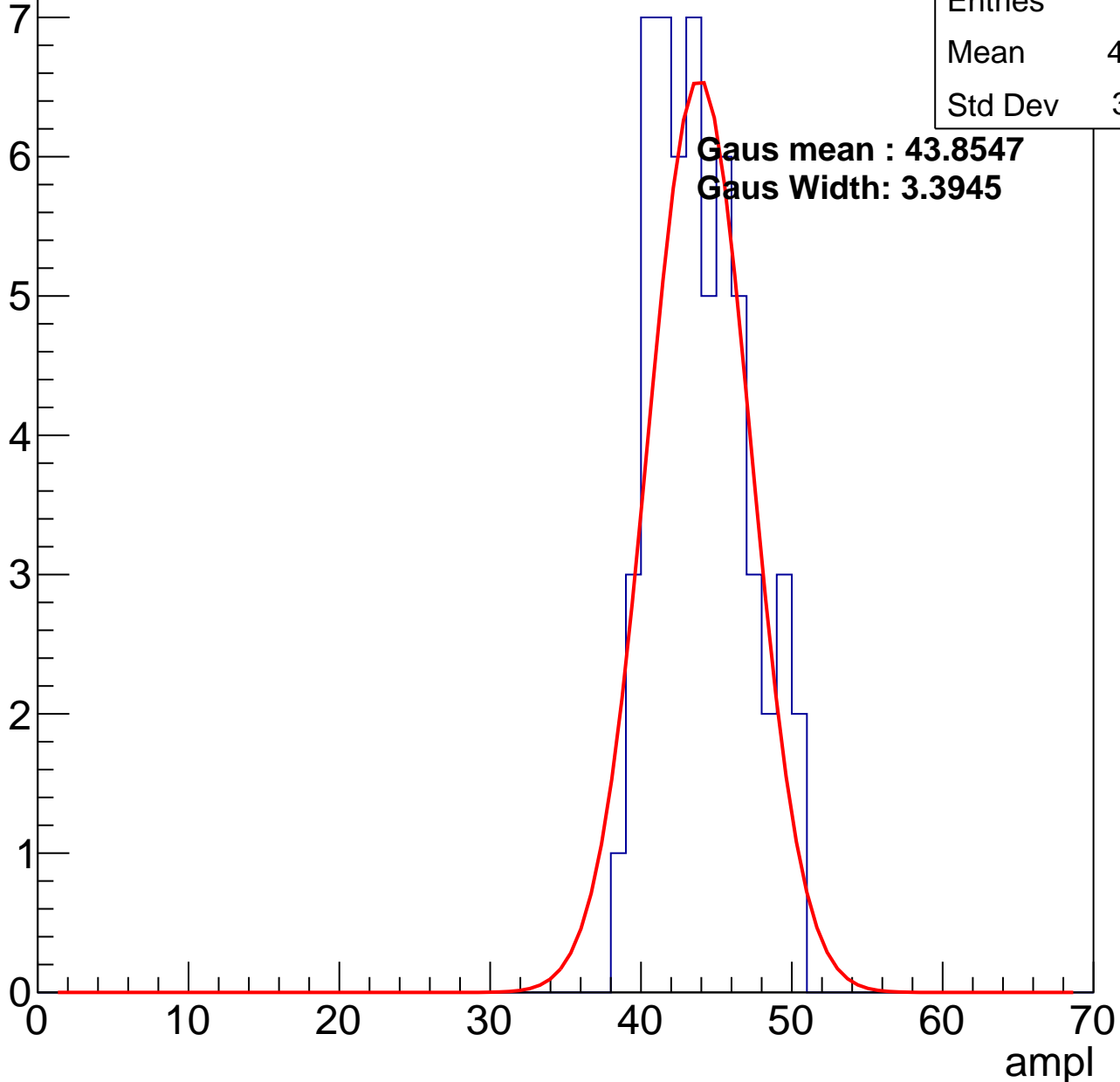


# B1L003S, U6-ch16, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

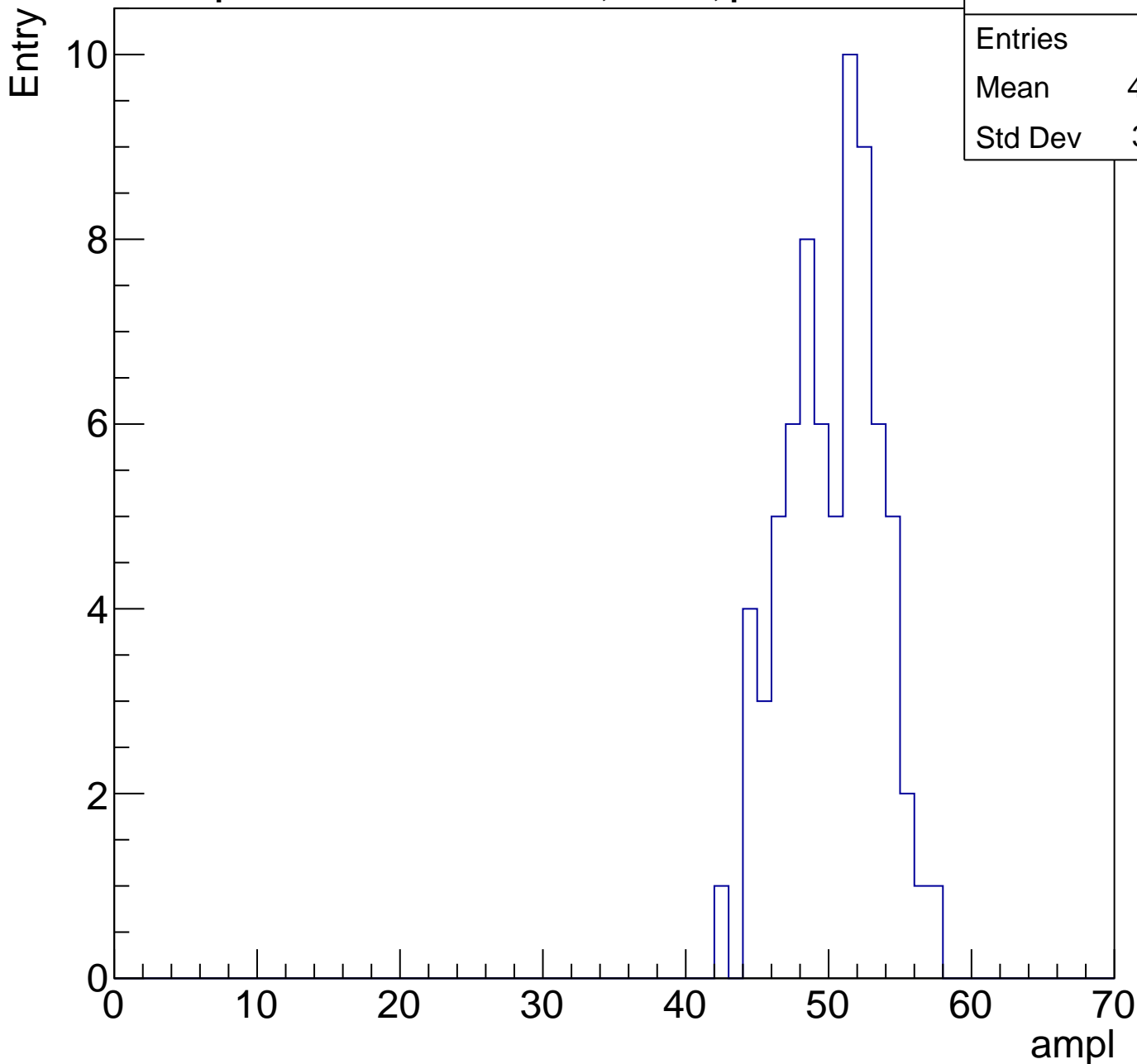
Entries	57
Mean	43.49
Std Dev	3.061



# B1L003S, U6-ch16, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	72
Mean	49.75
Std Dev	3.261

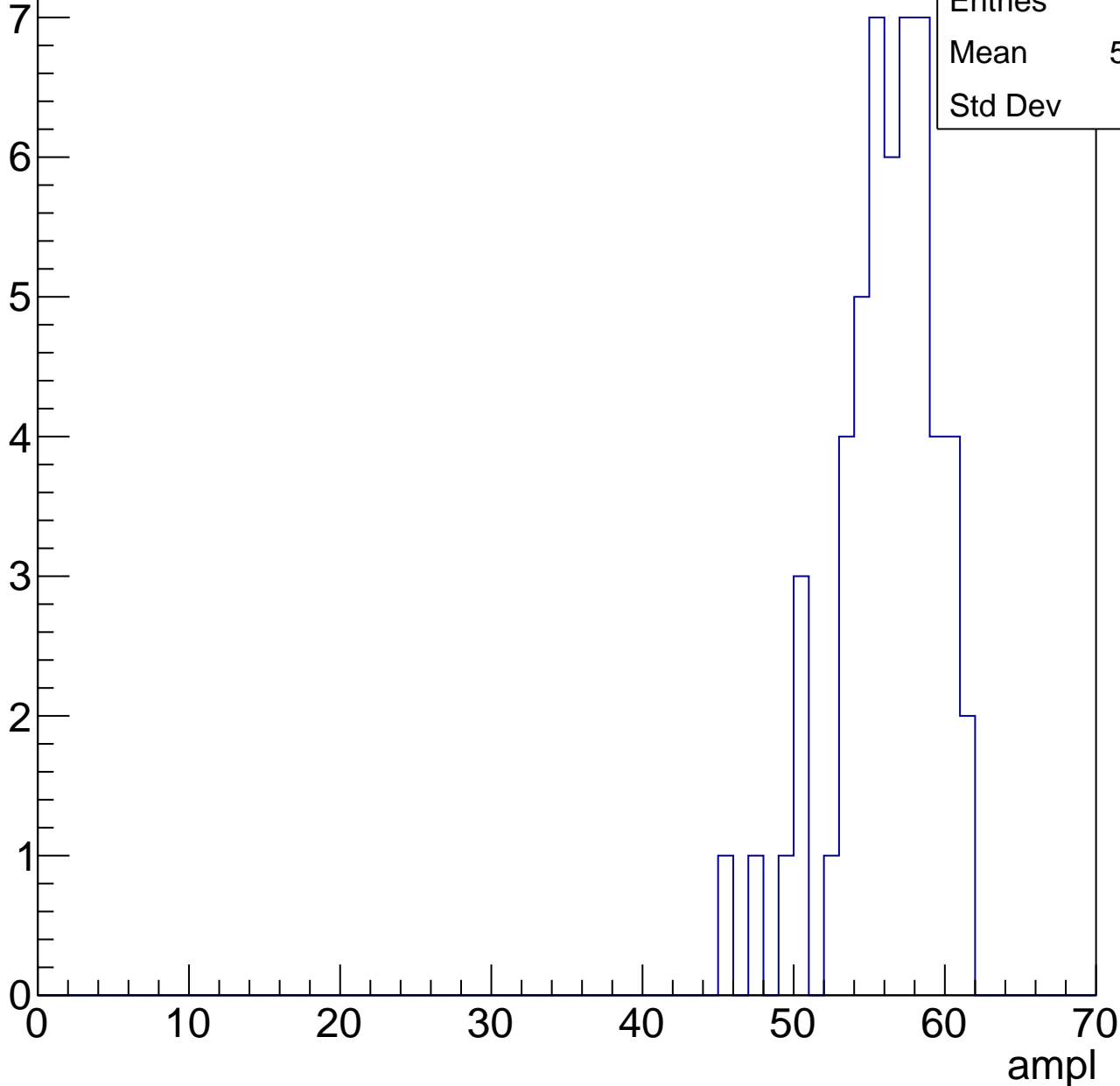


# B1L003S, U6-ch16, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	55.64
Std Dev	3.41

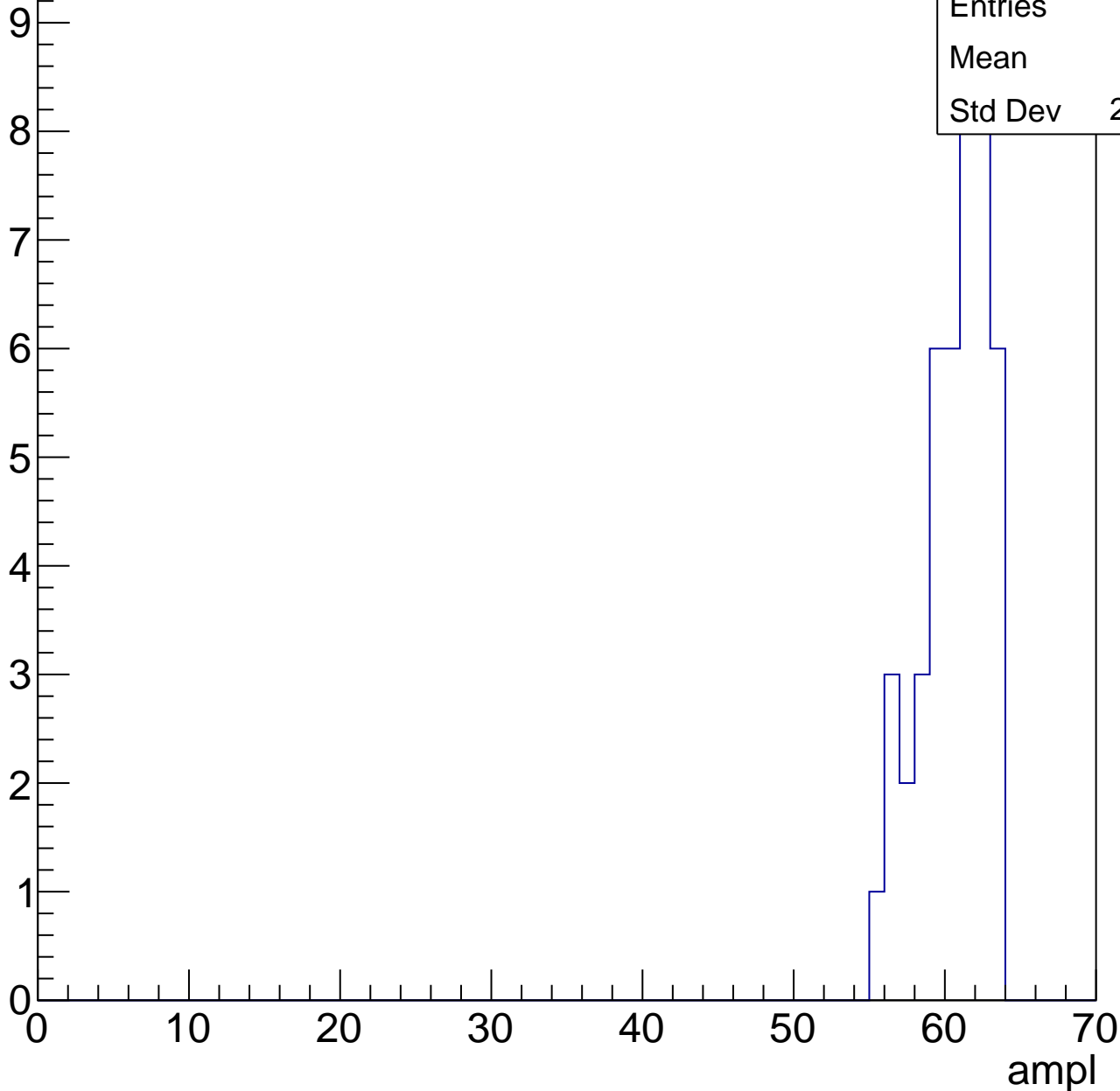


# B1L003S, U6-ch16, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

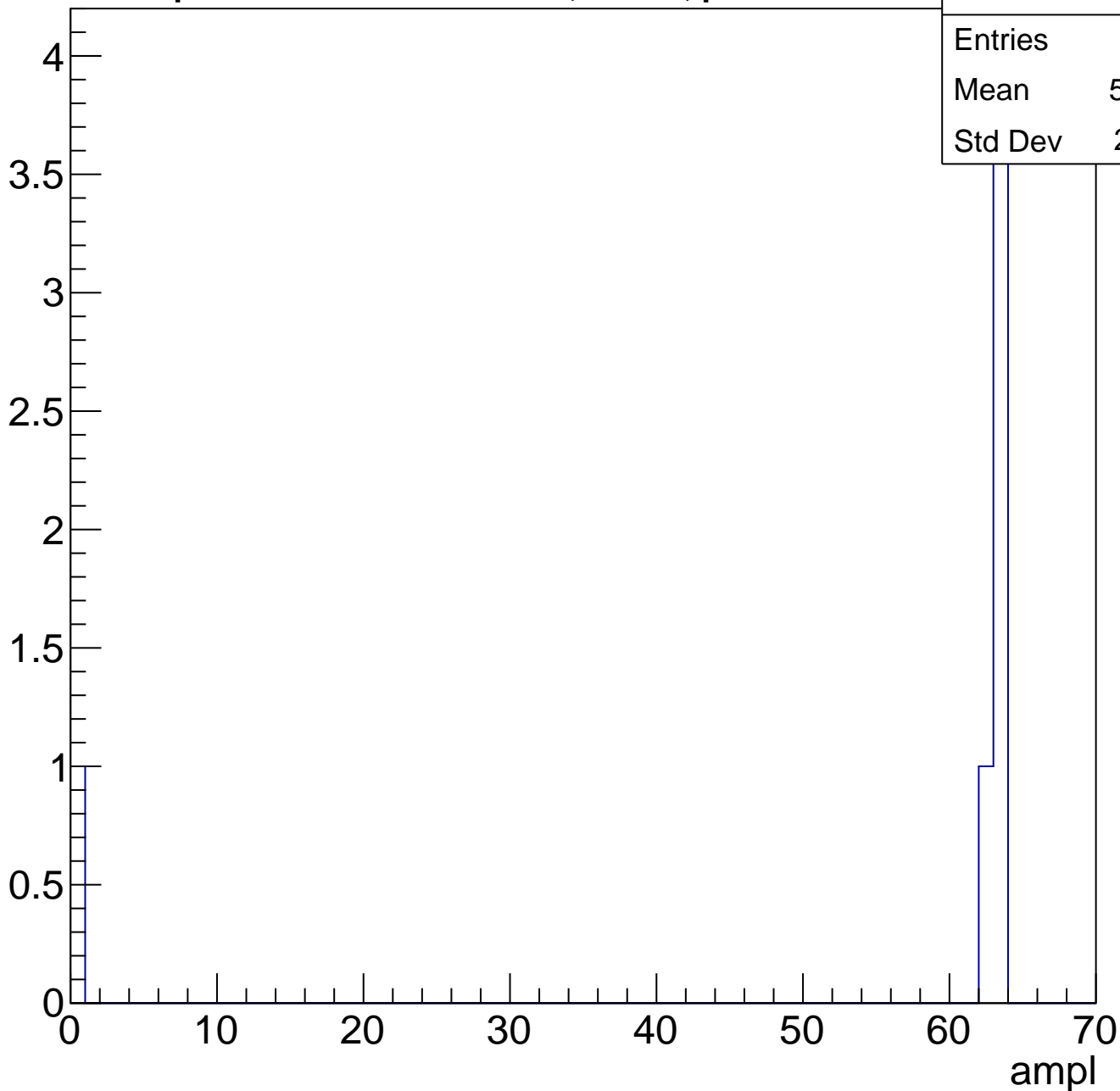
Entries	44
Mean	60.2
Std Dev	2.159



# B1L003S, U6-ch16, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch16, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L003S, U6-ch17, adc0

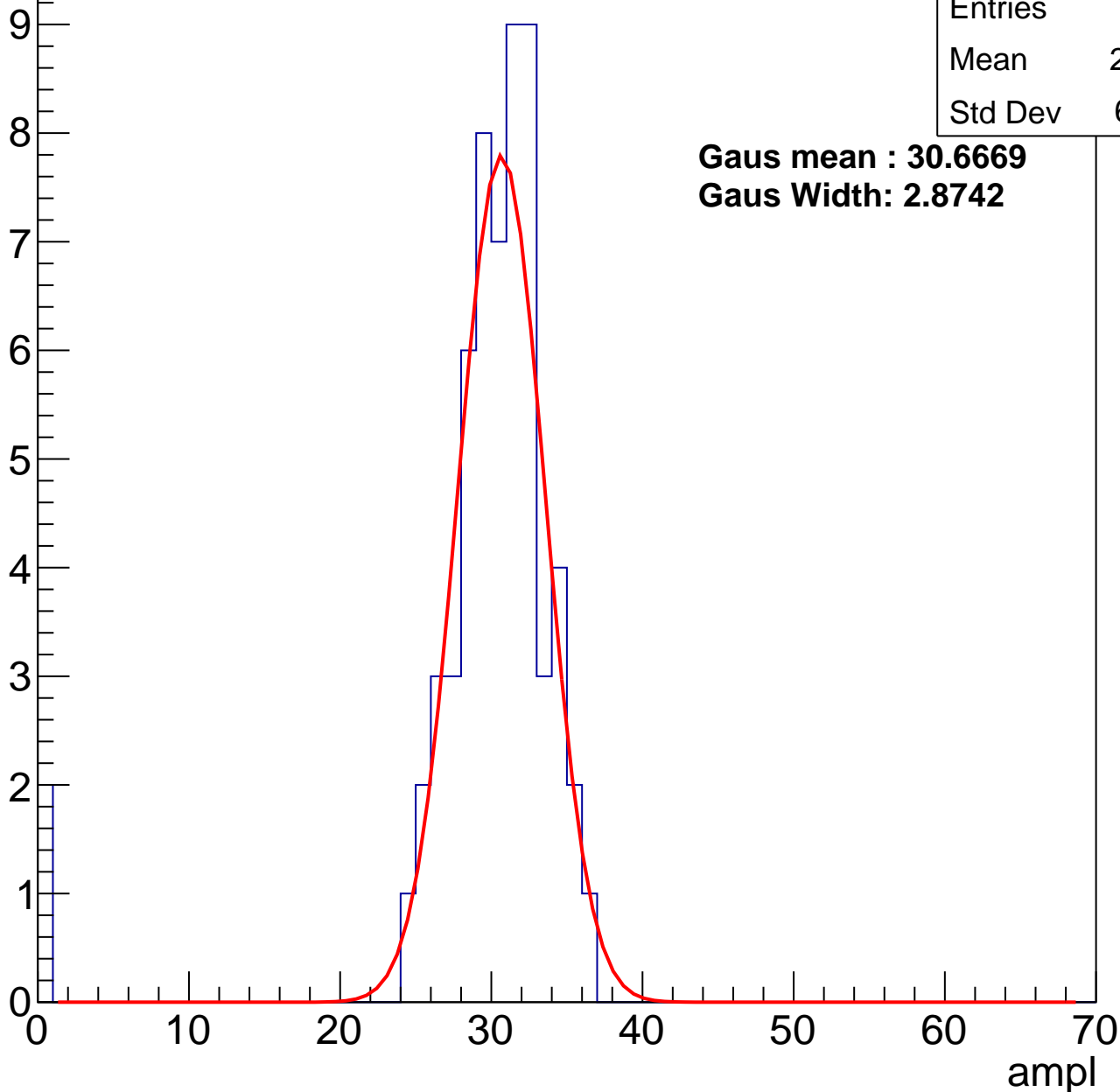
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	29.18
Std Dev	6.021

**Gaus mean : 30.6669**

**Gaus Width: 2.8742**



# B1L003S, U6-ch17, adc1

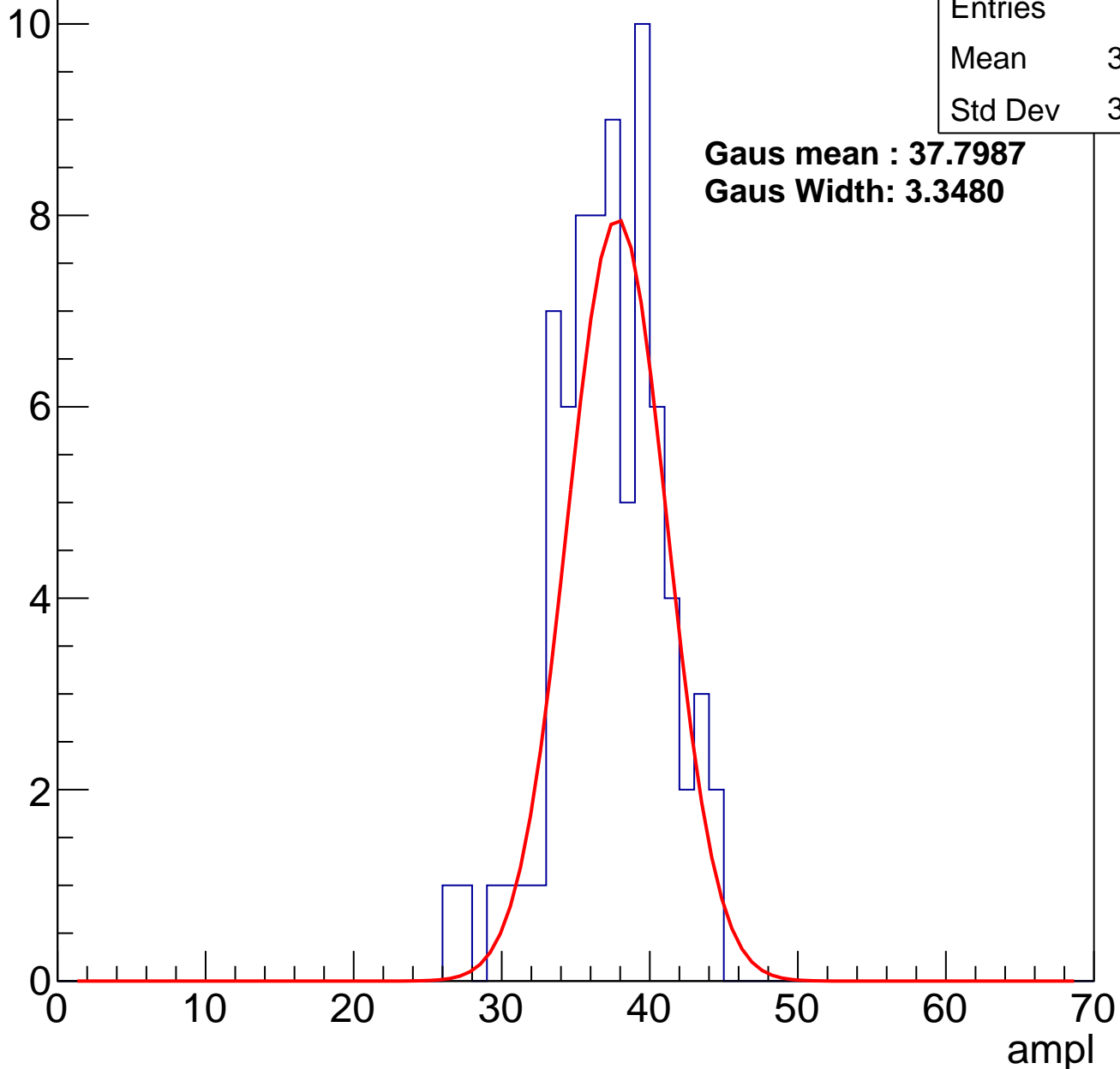
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	76
Mean	36.79
Std Dev	3.657

**Gaus mean : 37.7987**

**Gaus Width: 3.3480**

Entry



# B1L003S, U6-ch17, adc2

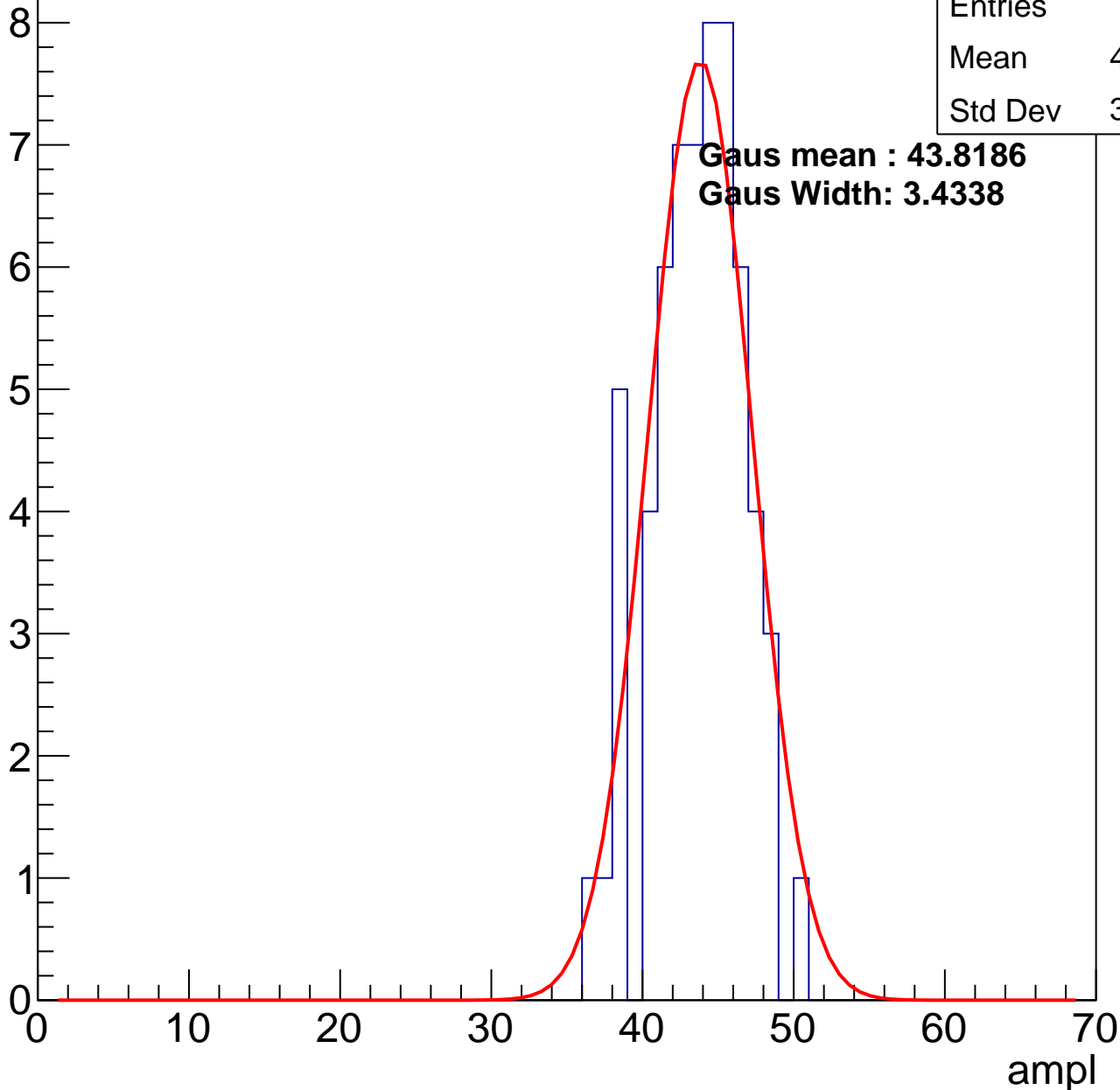
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	43.18
Std Dev	3.022

**Gaus mean : 43.8186**

**Gaus Width: 3.4338**

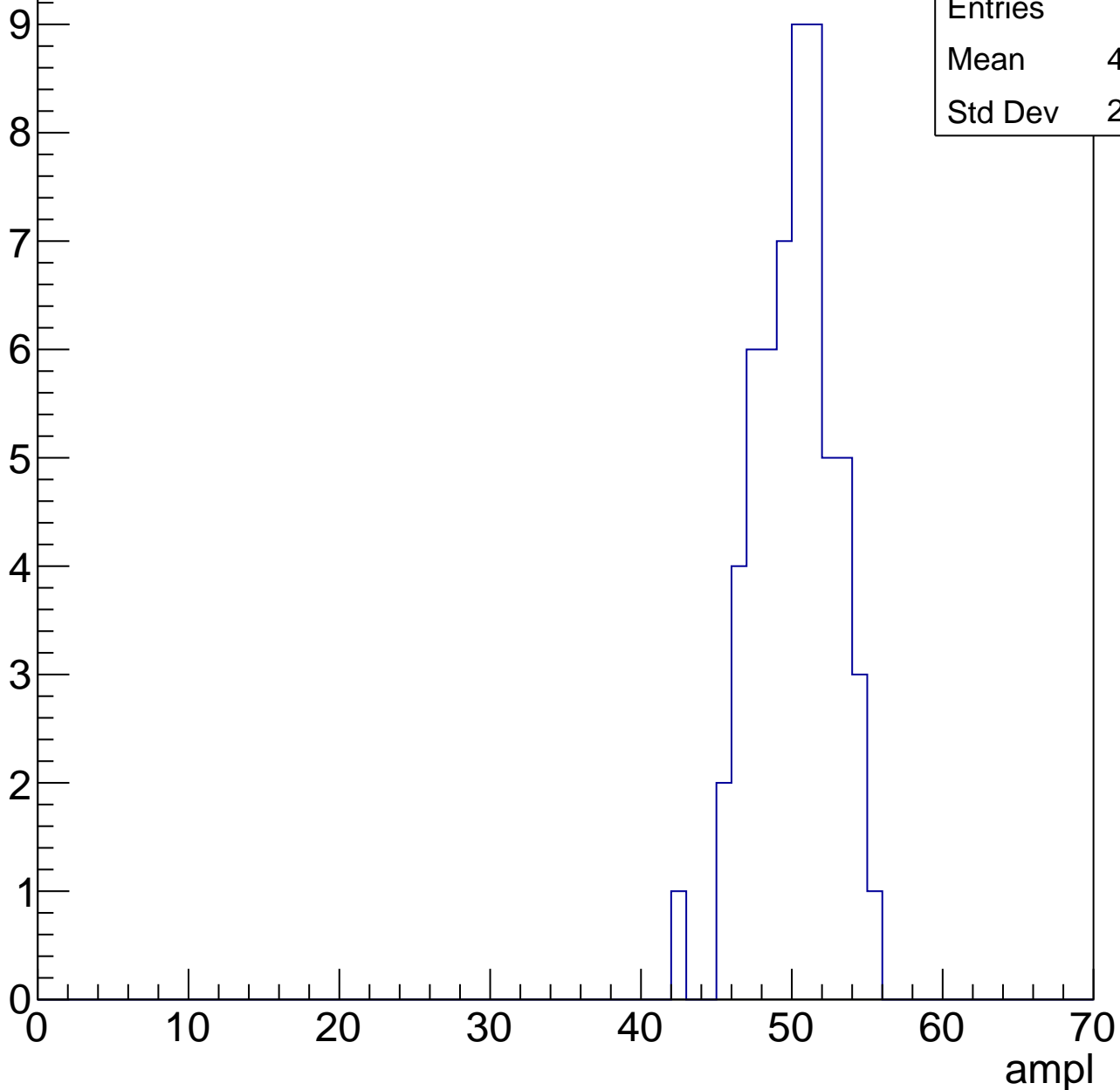


# B1L003S, U6-ch17, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	49.66
Std Dev	2.636

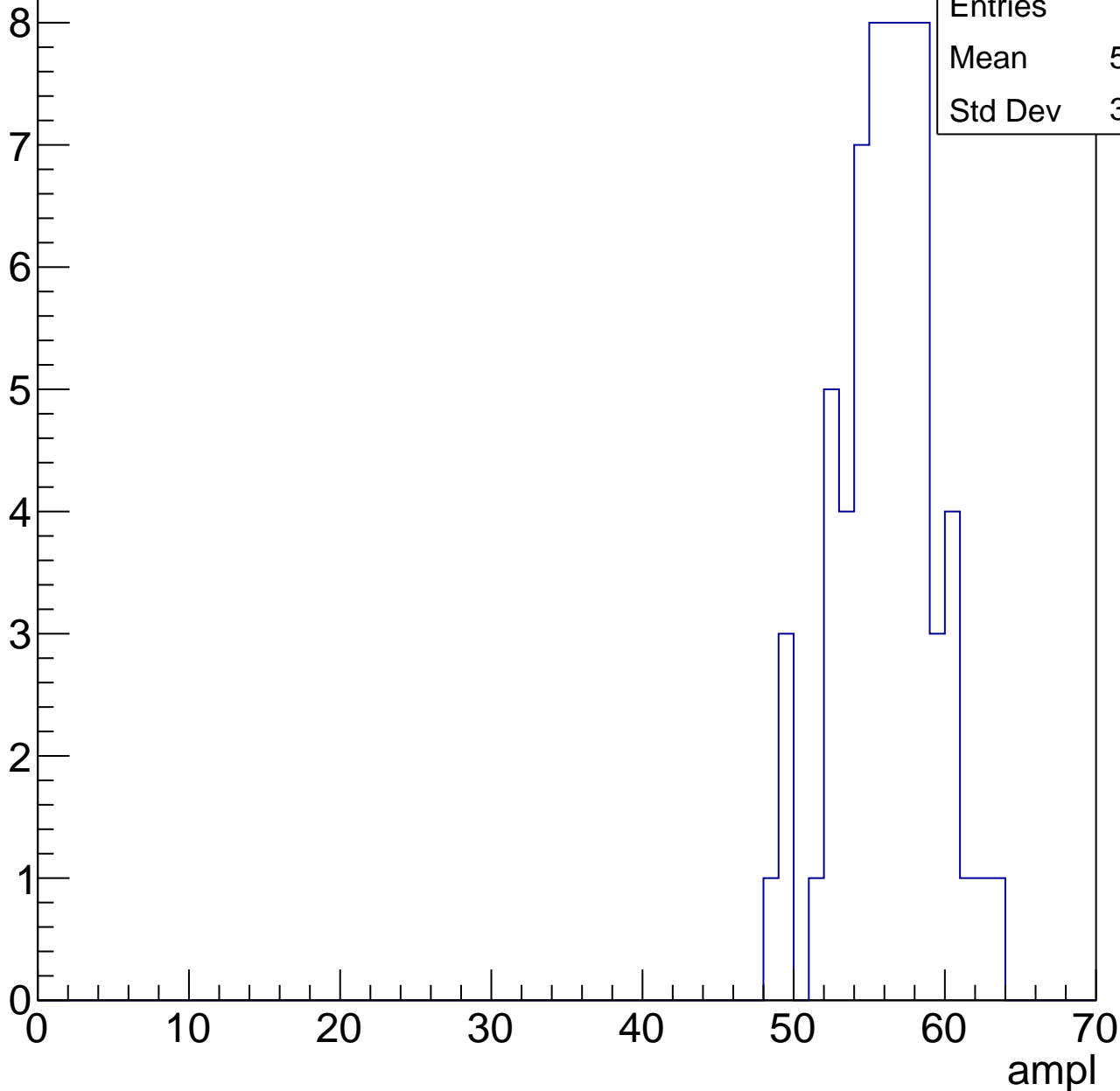


# B1L003S, U6-ch17, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	55.67
Std Dev	3.142

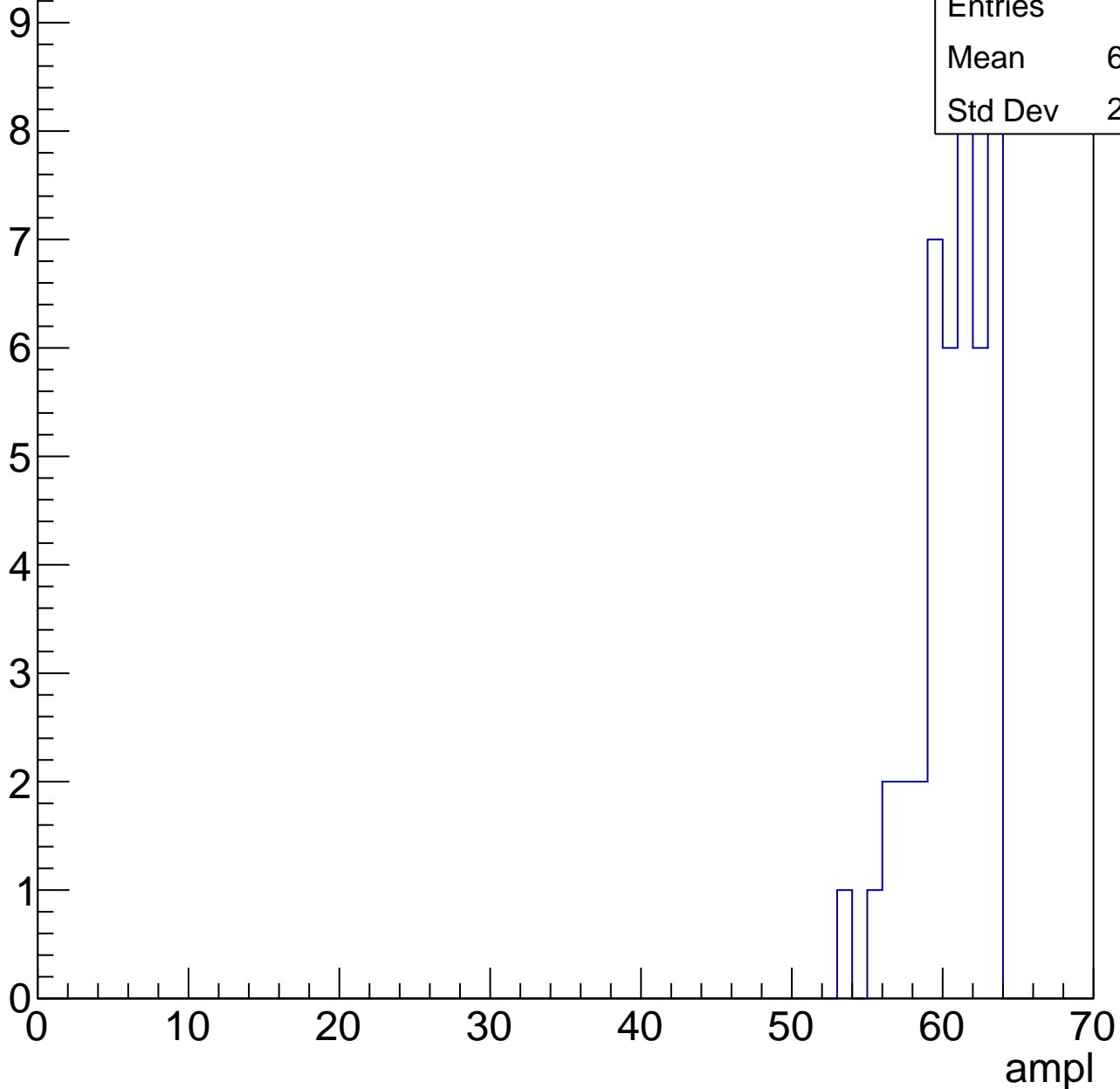


# B1L003S, U6-ch17, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

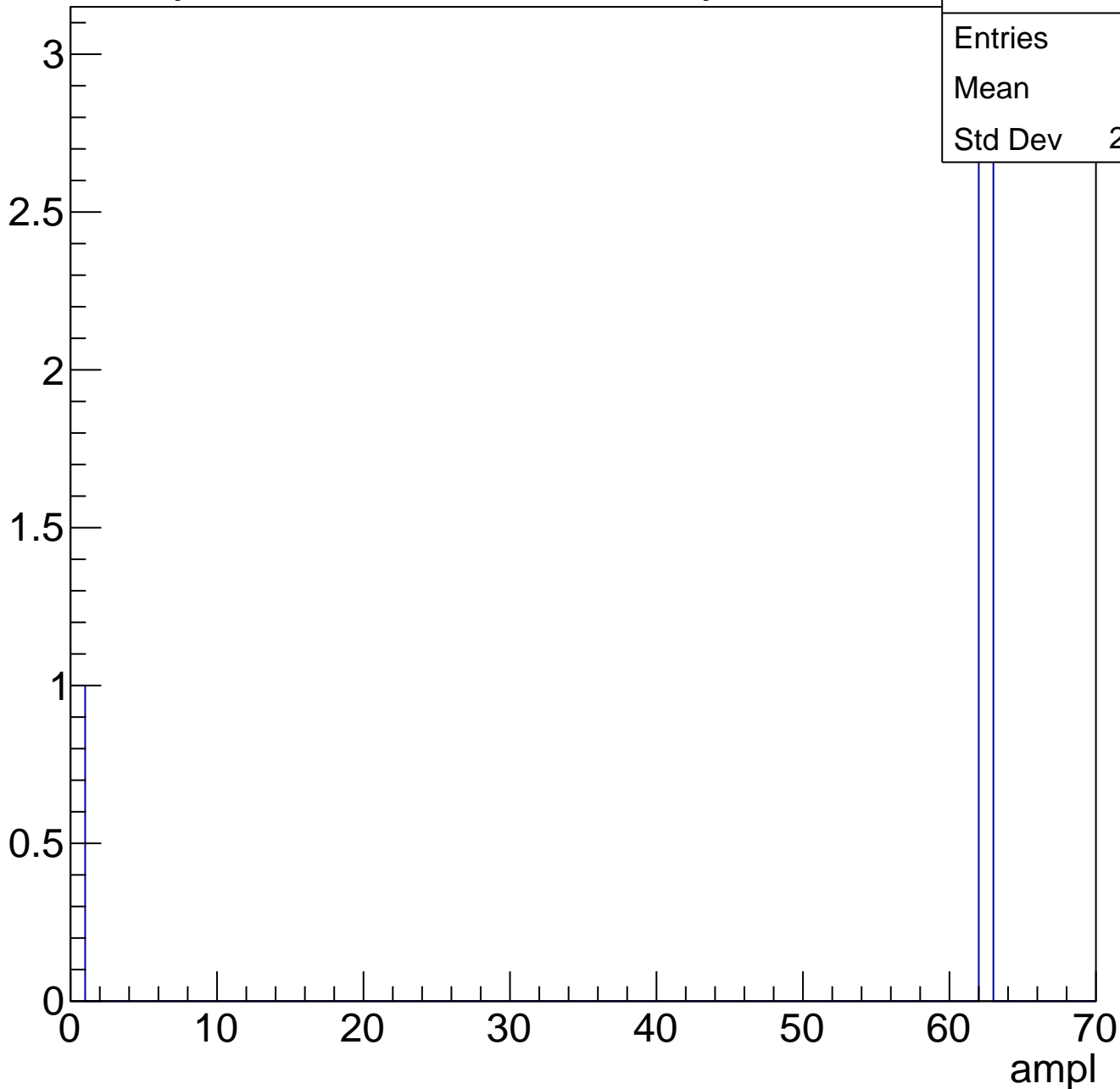
Entries	45
Mean	60.24
Std Dev	2.358



# B1L003S, U6-ch17, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch17, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U6-ch18, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	53
Mean	29.02
Std Dev	3.23

**Gaus mean : 29.7225**

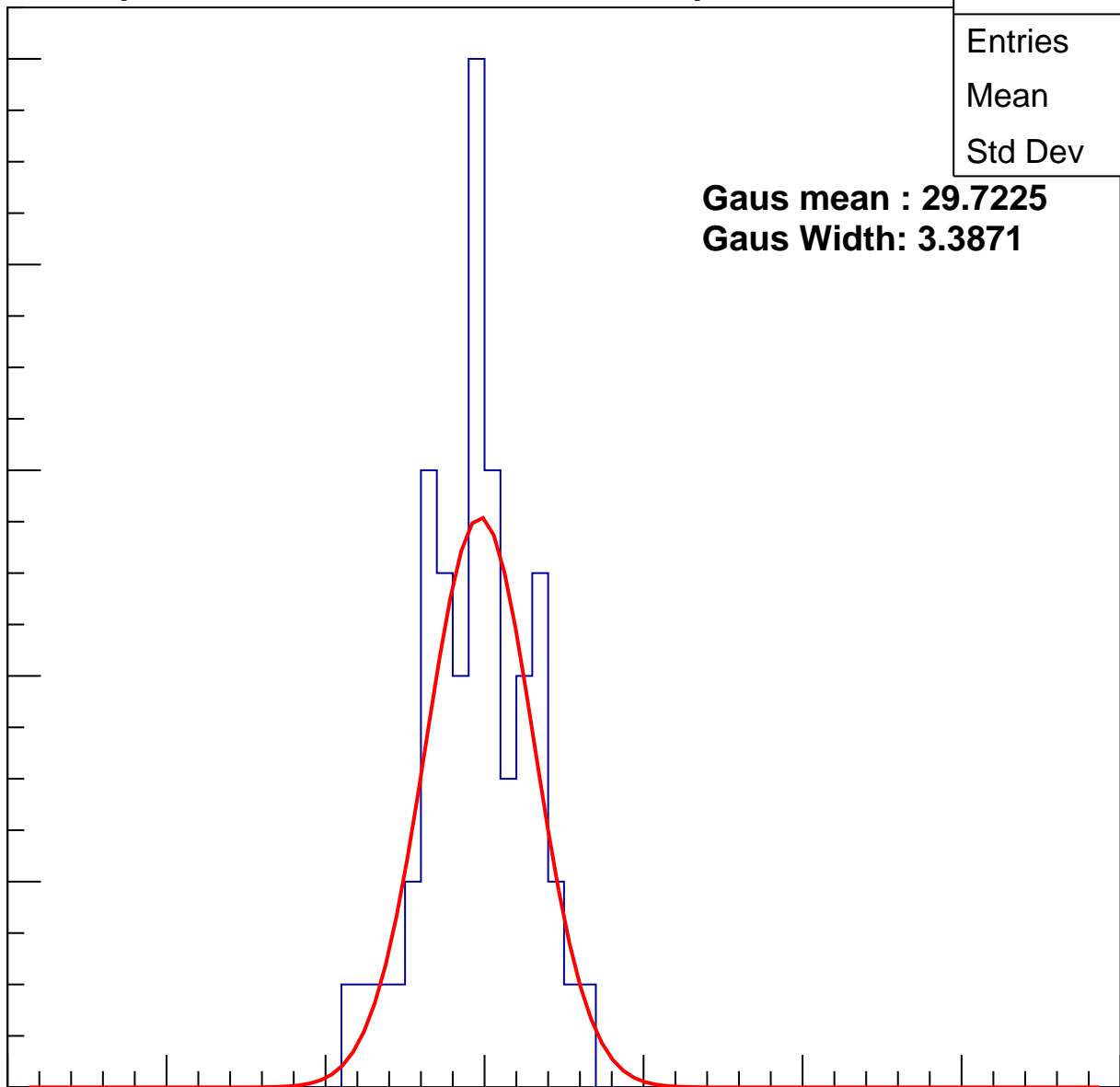
**Gaus Width: 3.3871**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U6-ch18, adc1

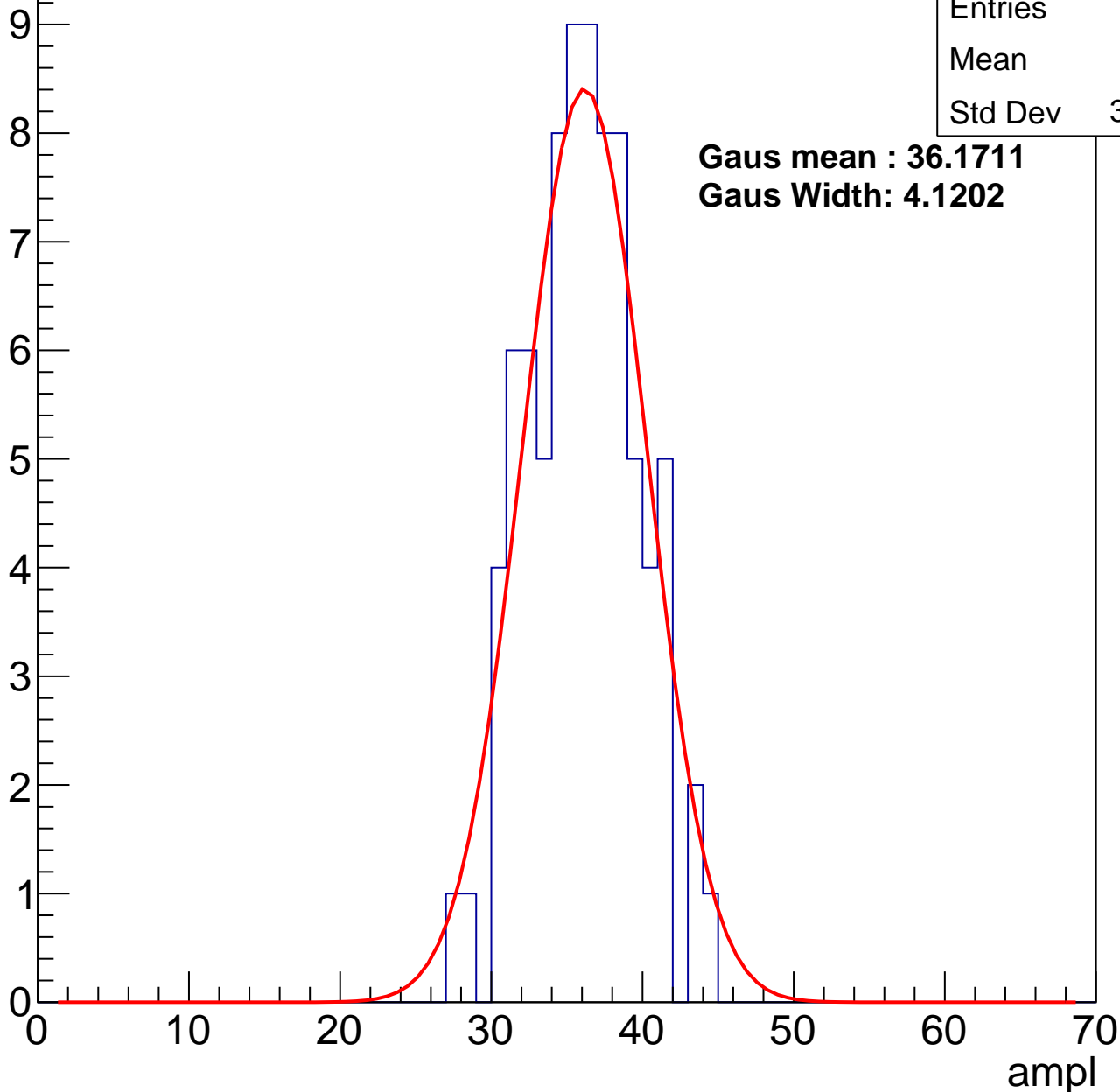
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	82
Mean	35.6
Std Dev	3.568

**Gaus mean : 36.1711**

**Gaus Width: 4.1202**



# B1L003S, U6-ch18, adc2

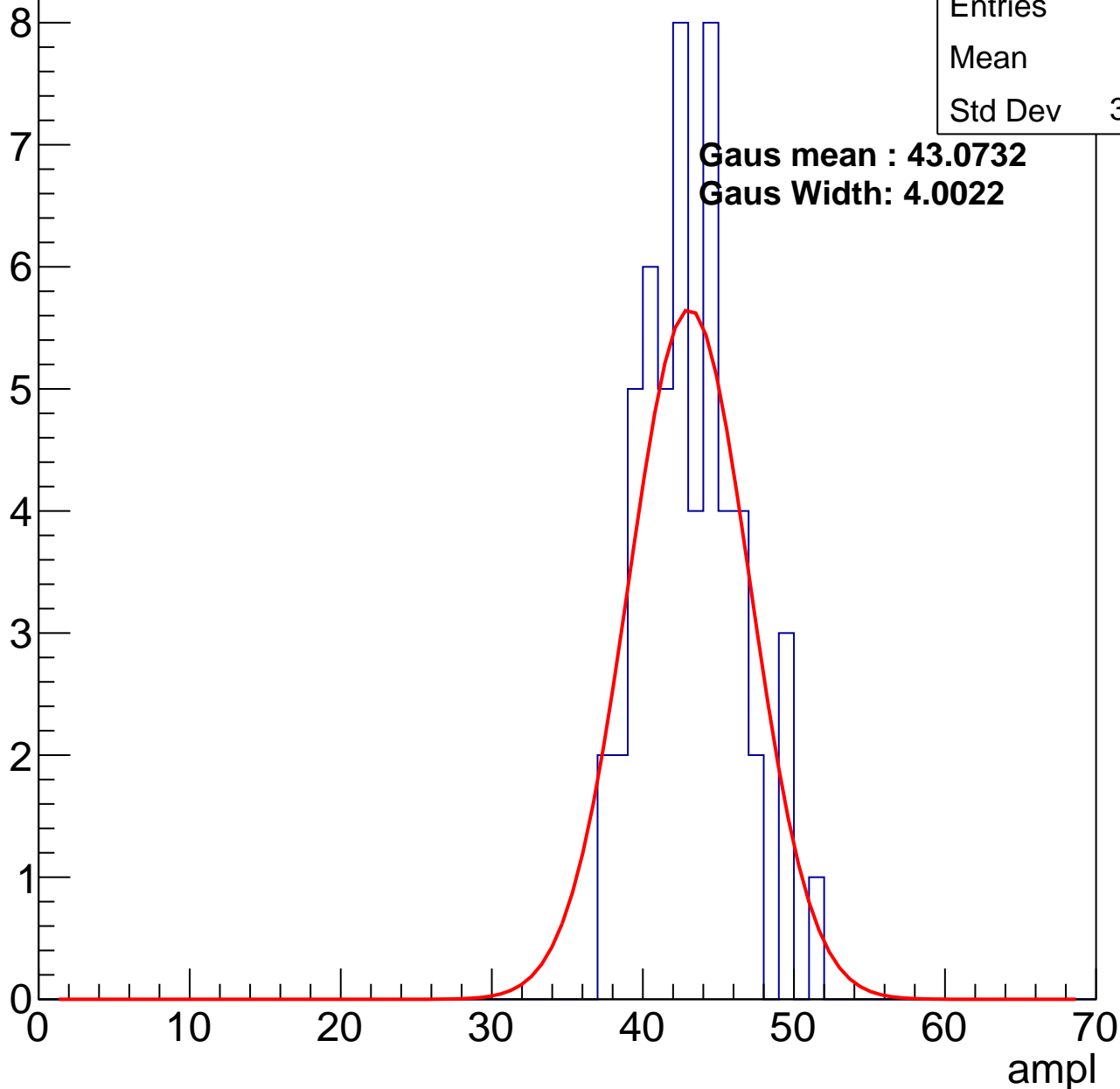
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	54
Mean	42.7
Std Dev	3.172

**Gaus mean : 43.0732**

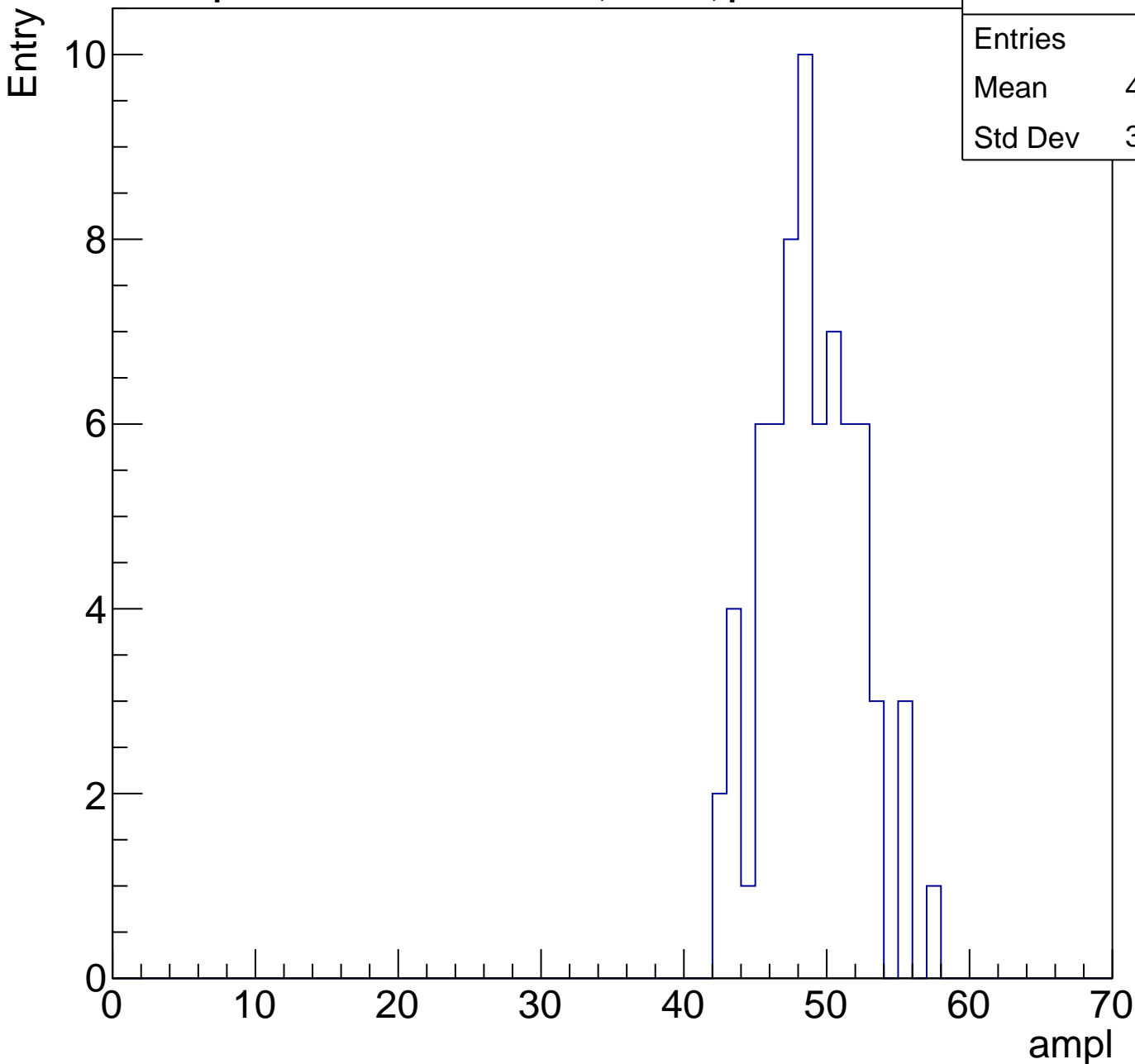
**Gaus Width: 4.0022**



# B1L003S, U6-ch18, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

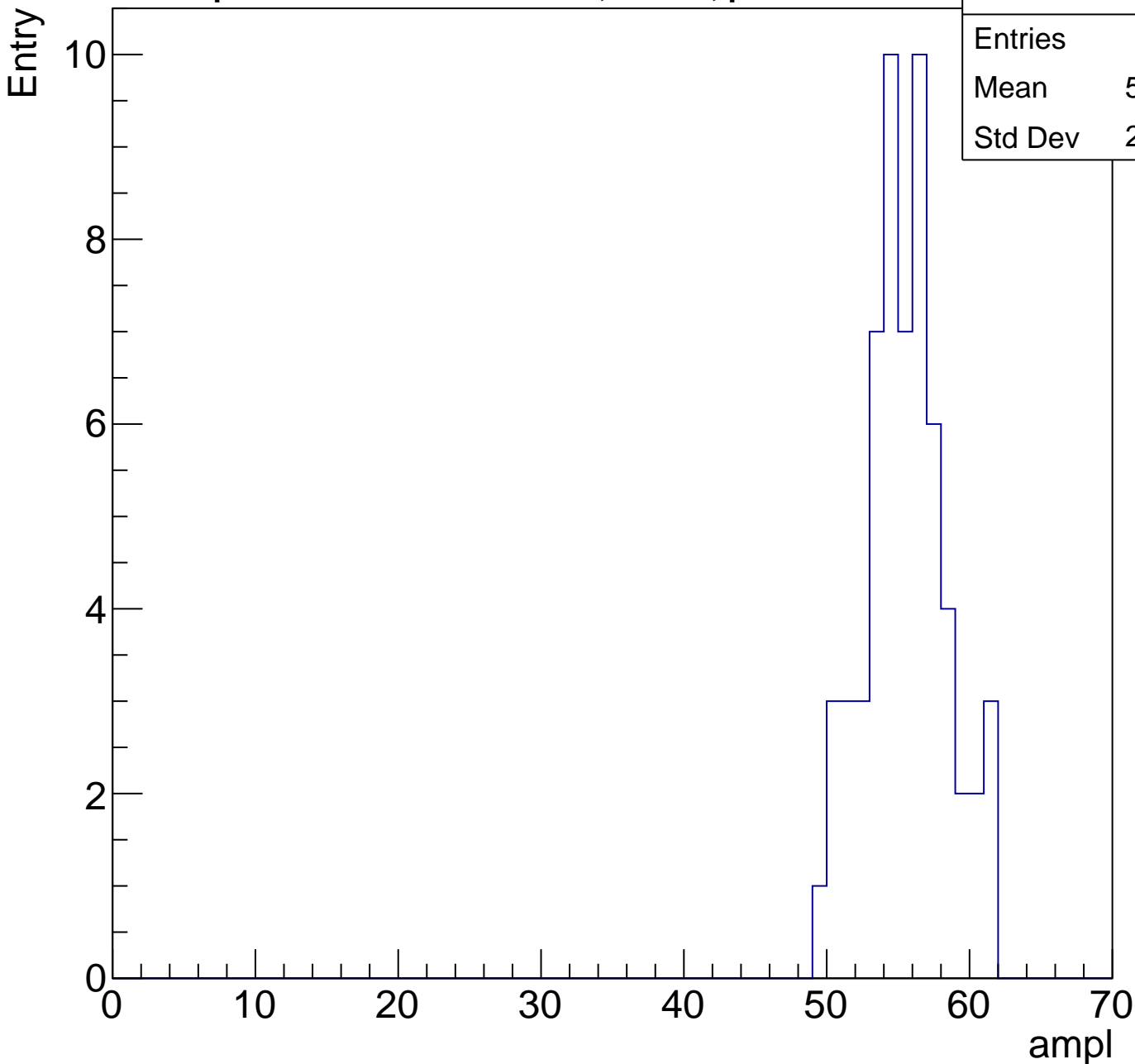
Entries	69
Mean	48.48
Std Dev	3.286



# B1L003S, U6-ch18, adc4

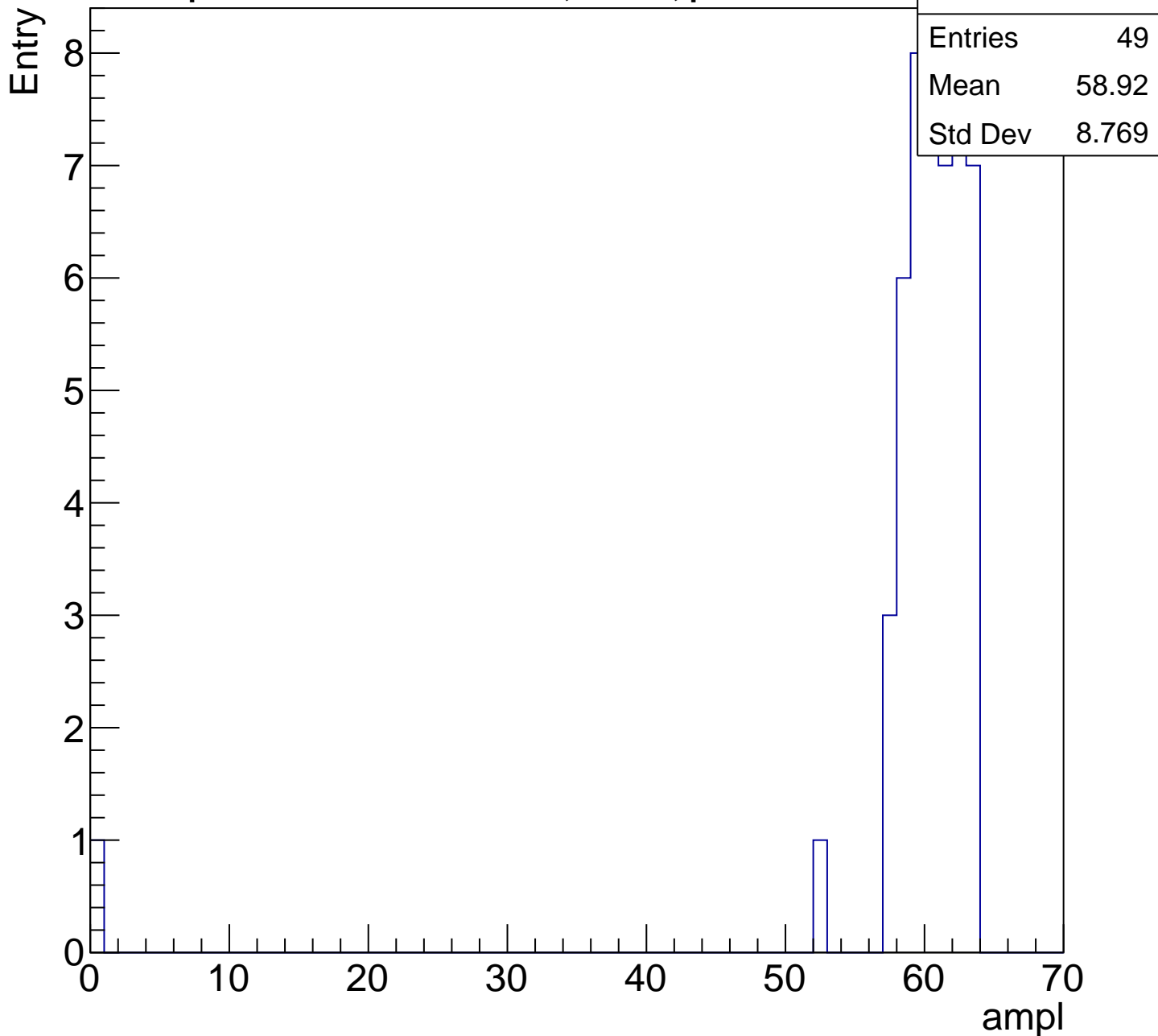
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	61
Mean	55.07
Std Dev	2.816



# B1L003S, U6-ch18, adc5

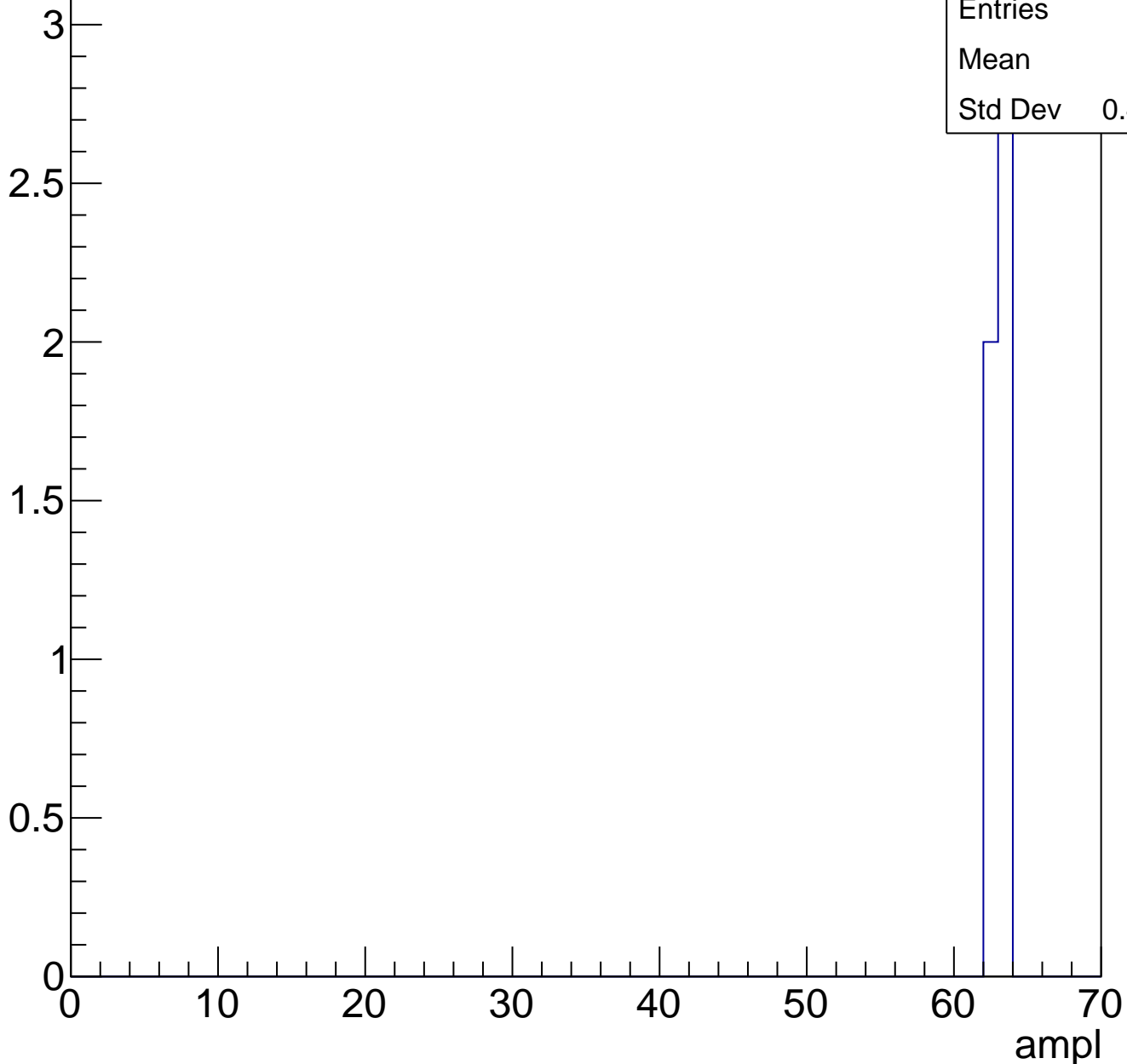
calib\_packv5\_042523\_0143.root, FC#13, port D2



# B1L003S, U6-ch18, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch18, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L003S, U6-ch19, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	55
Mean	30.22
Std Dev	2.801

**Gaus mean : 30.5124**

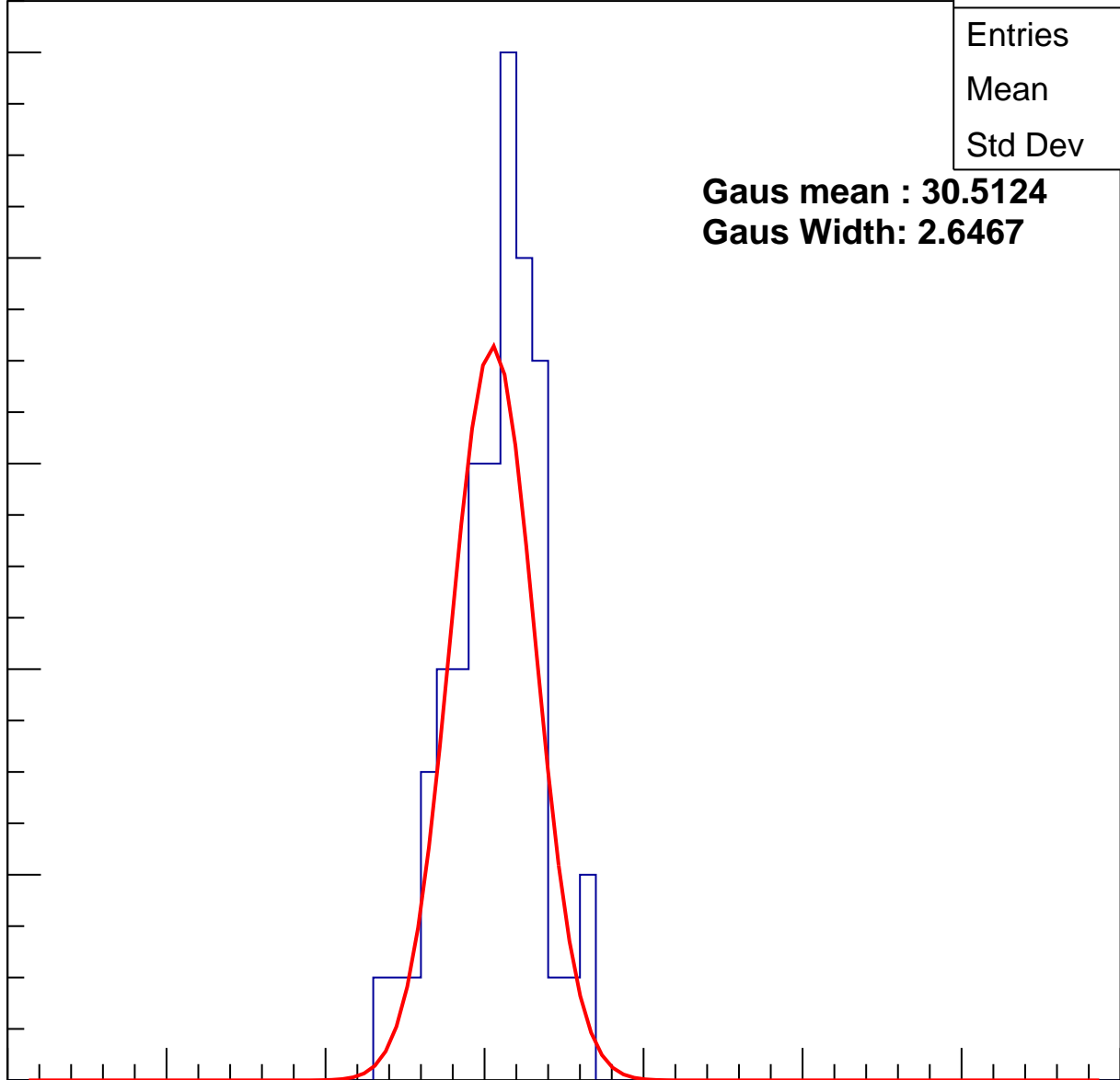
**Gaus Width: 2.6467**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U6-ch19, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	73
Mean	37.14
Std Dev	2.935

**Gaus mean : 37.8494**

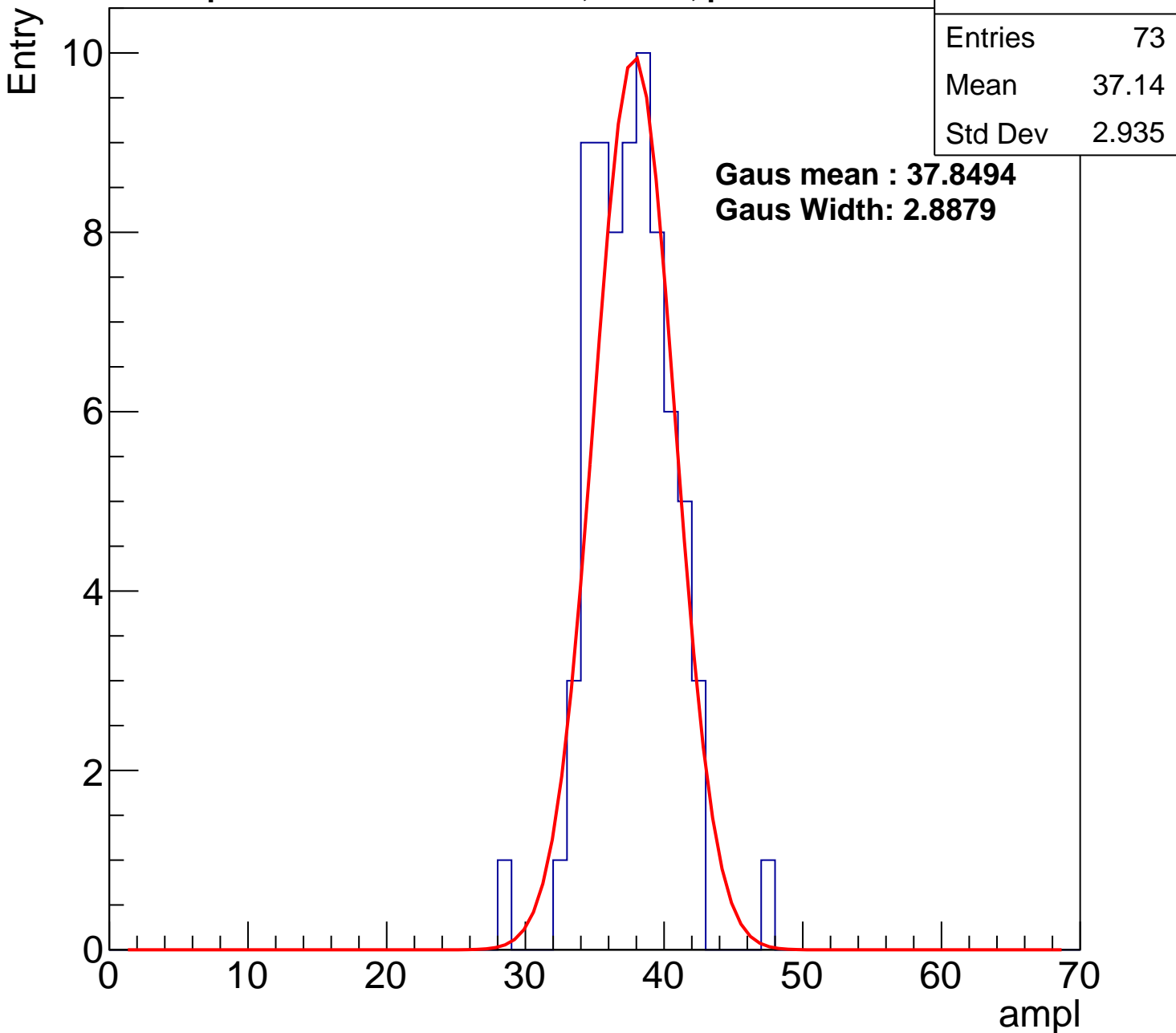
**Gaus Width: 2.8879**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L003S, U6-ch19, adc2

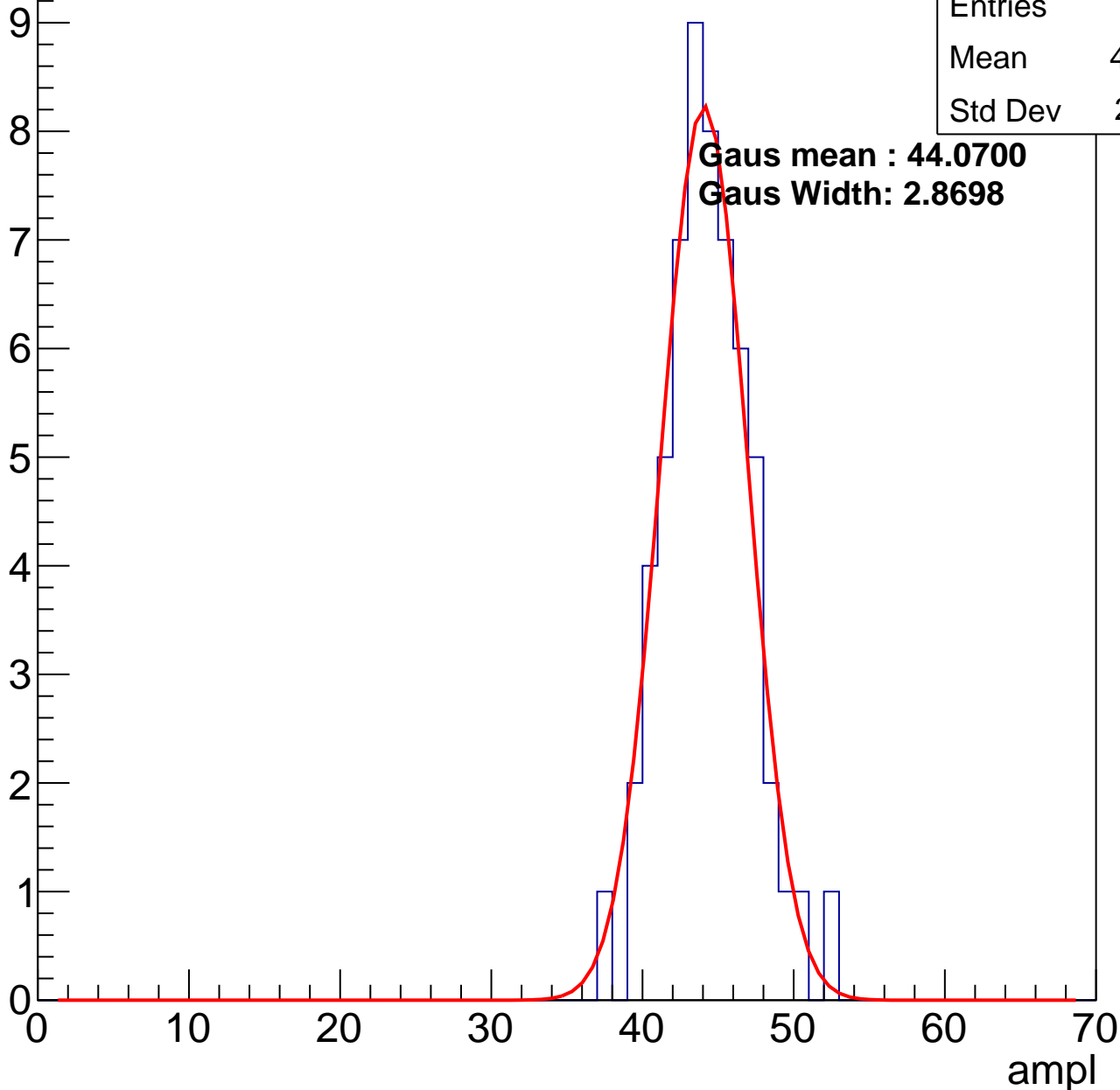
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	43.83
Std Dev	2.841

**Gaus mean : 44.0700**

**Gaus Width: 2.8698**

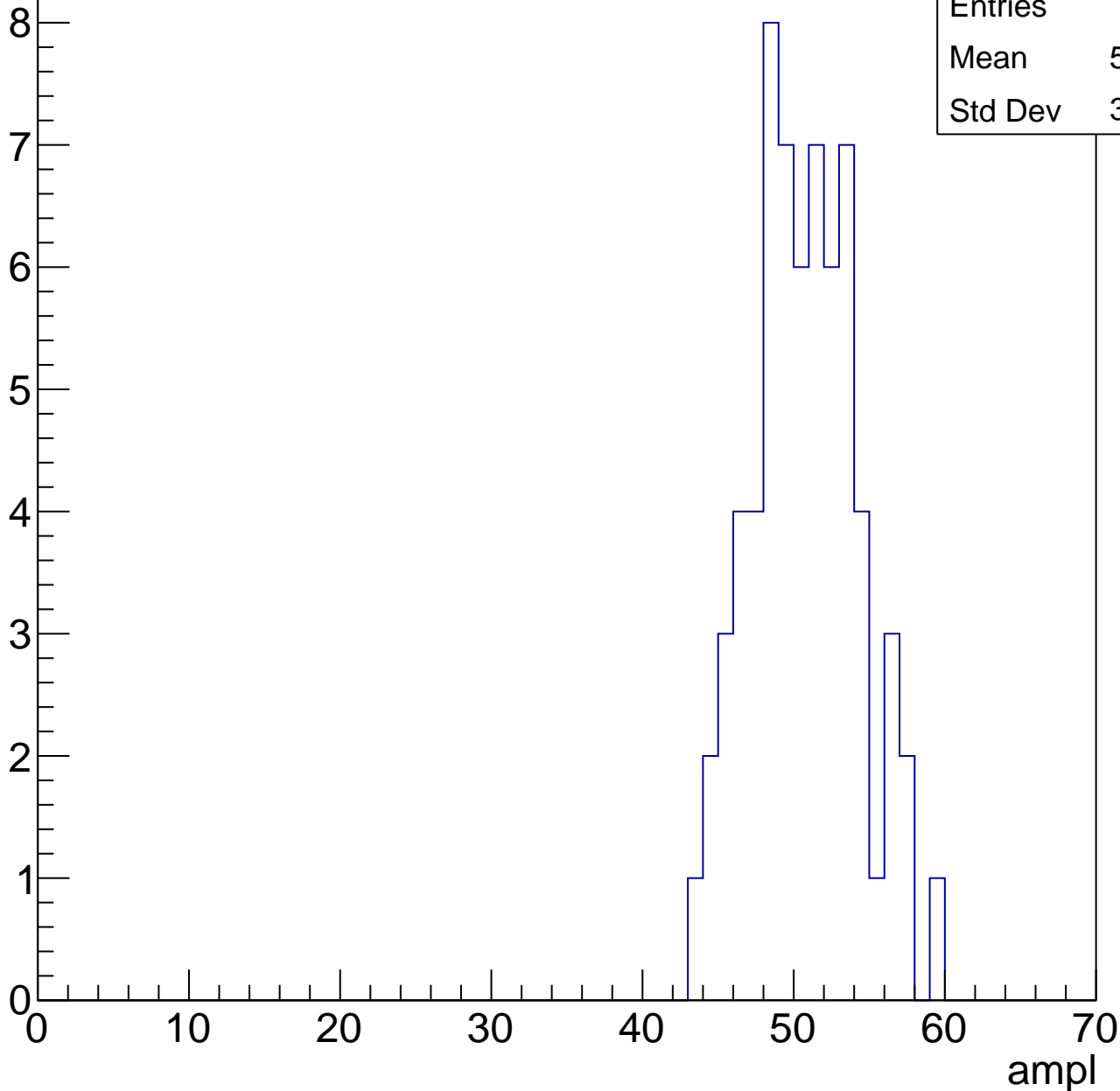


# B1L003S, U6-ch19, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	50.26
Std Dev	3.483

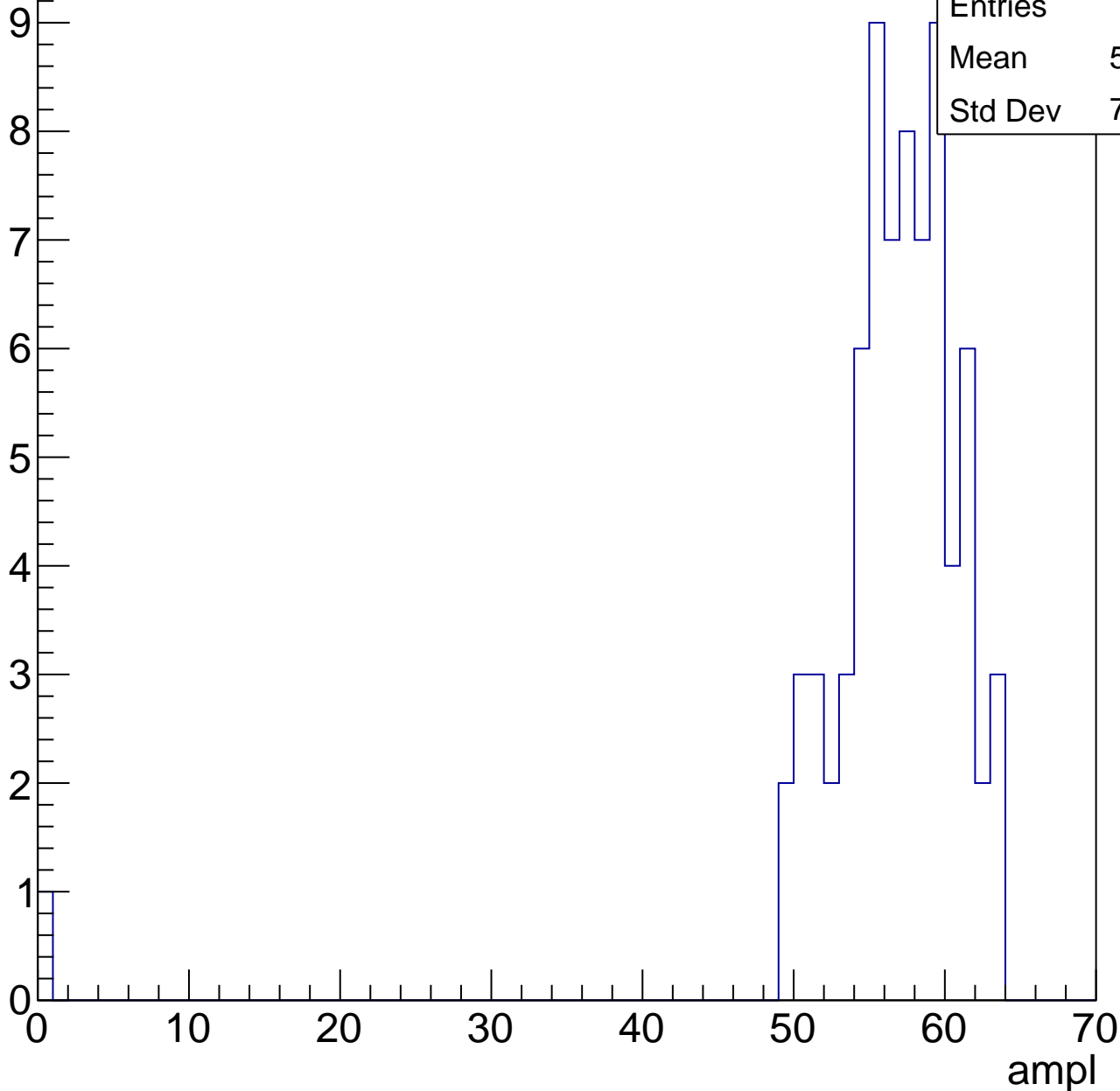


# B1L003S, U6-ch19, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	75
Mean	55.83
Std Dev	7.355

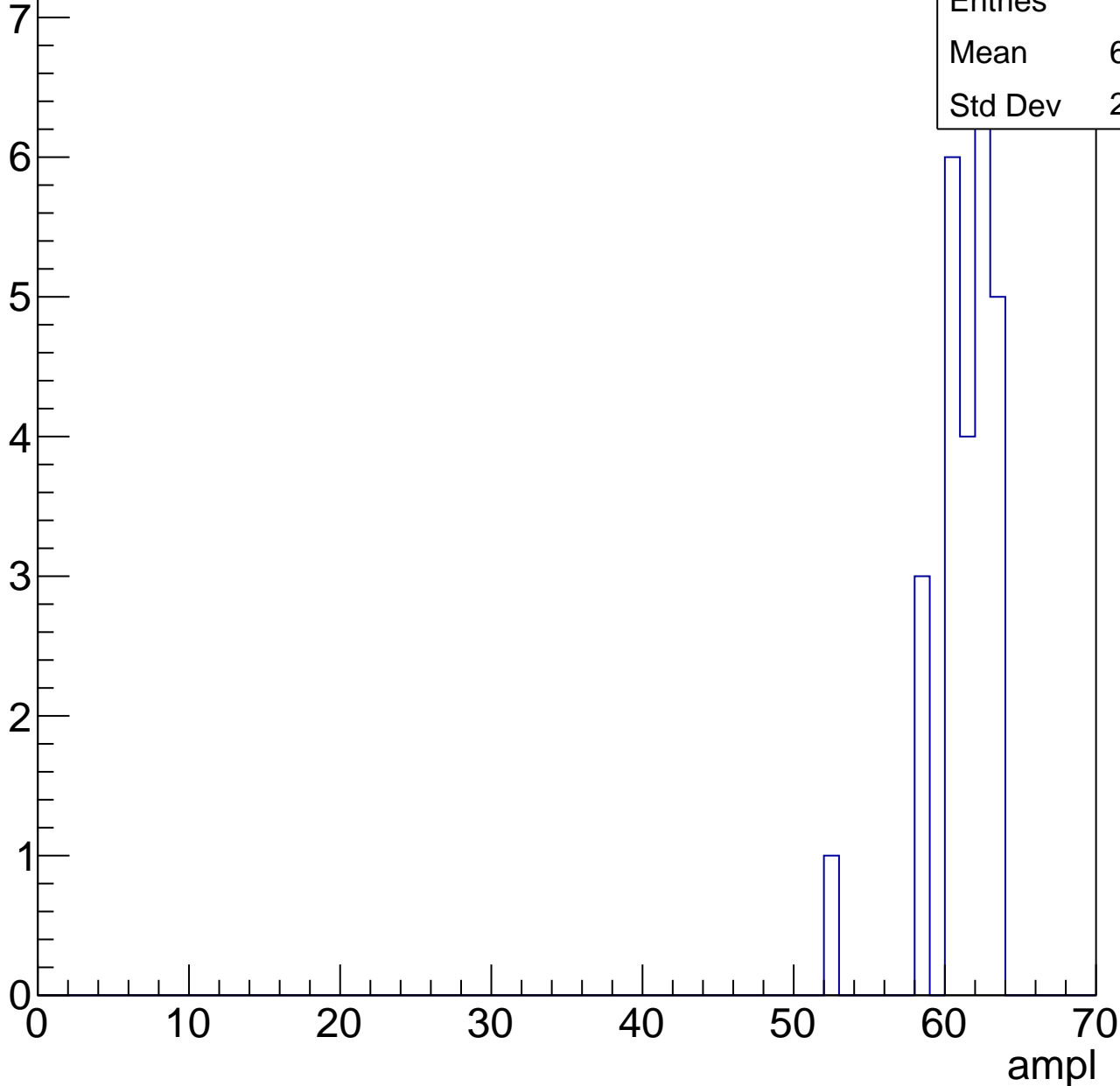


# B1L003S, U6-ch19, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	26
Mean	60.73
Std Dev	2.313



# B1L003S, U6-ch19, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch19, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U6-ch20, adc0

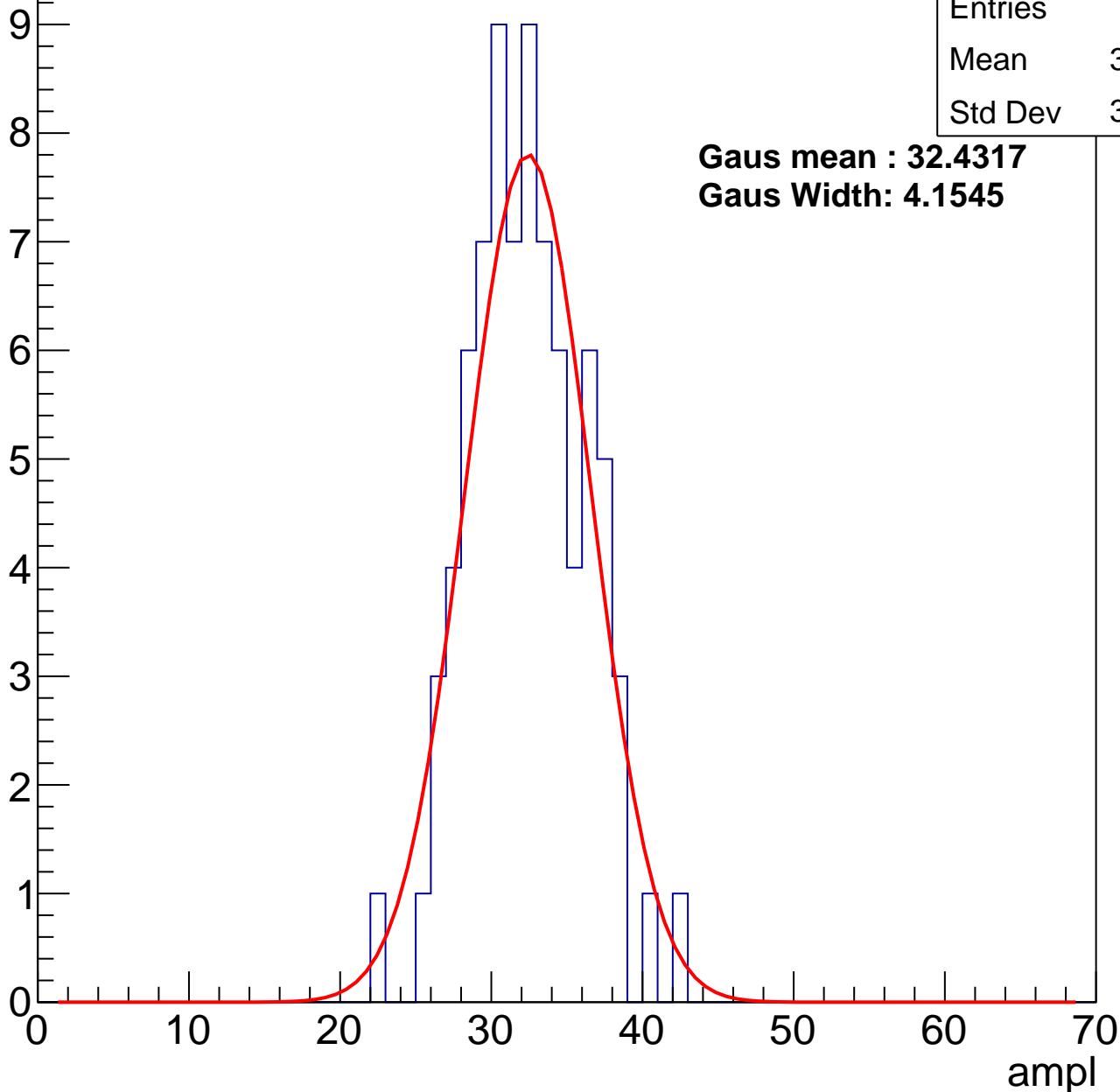
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	80
Mean	31.89
Std Dev	3.738

**Gaus mean : 32.4317**

**Gaus Width: 4.1545**



# B1L003S, U6-ch20, adc1

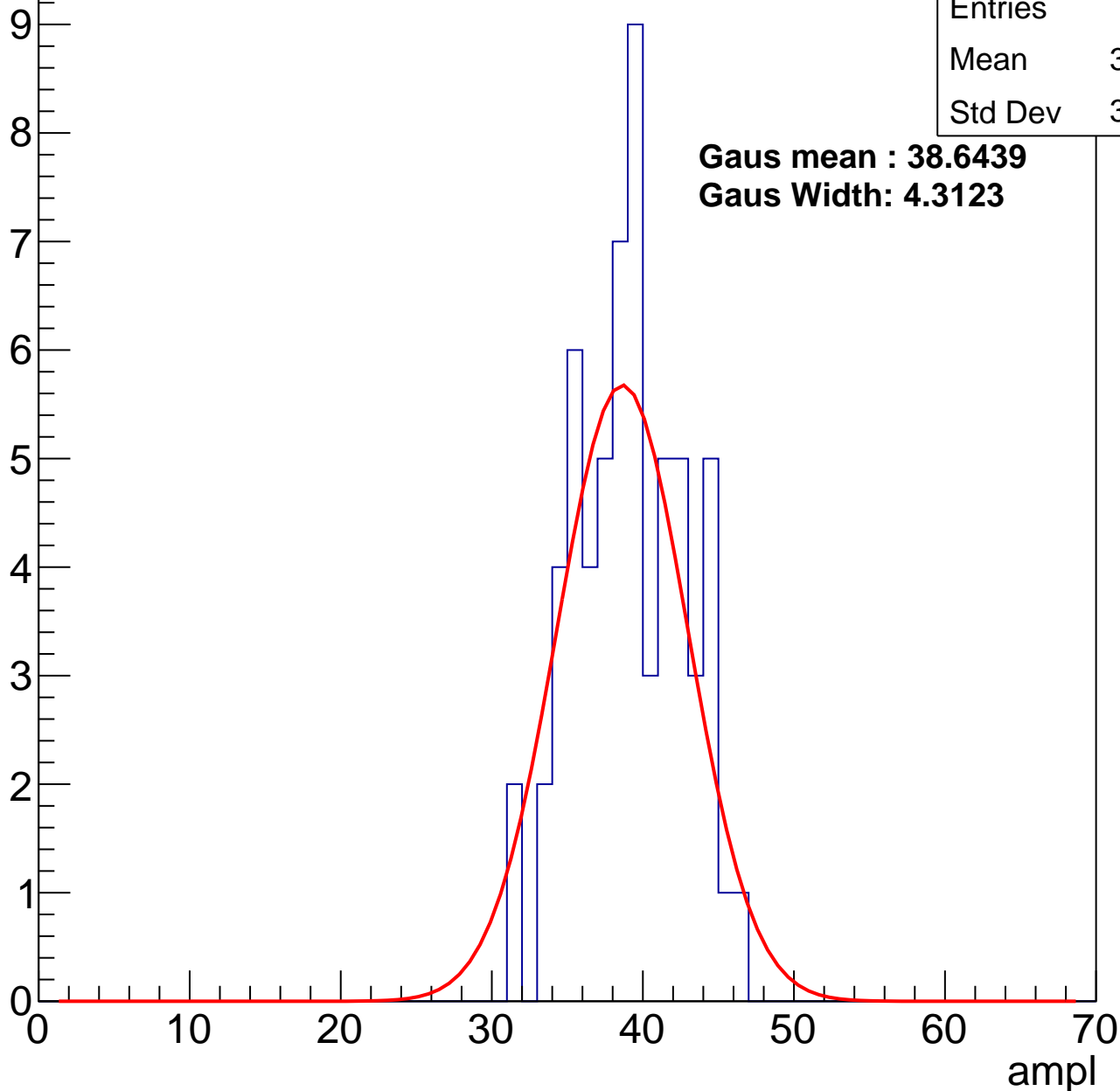
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	38.63
Std Dev	3.539

**Gaus mean : 38.6439**

**Gaus Width: 4.3123**



# B1L003S, U6-ch20, adc2

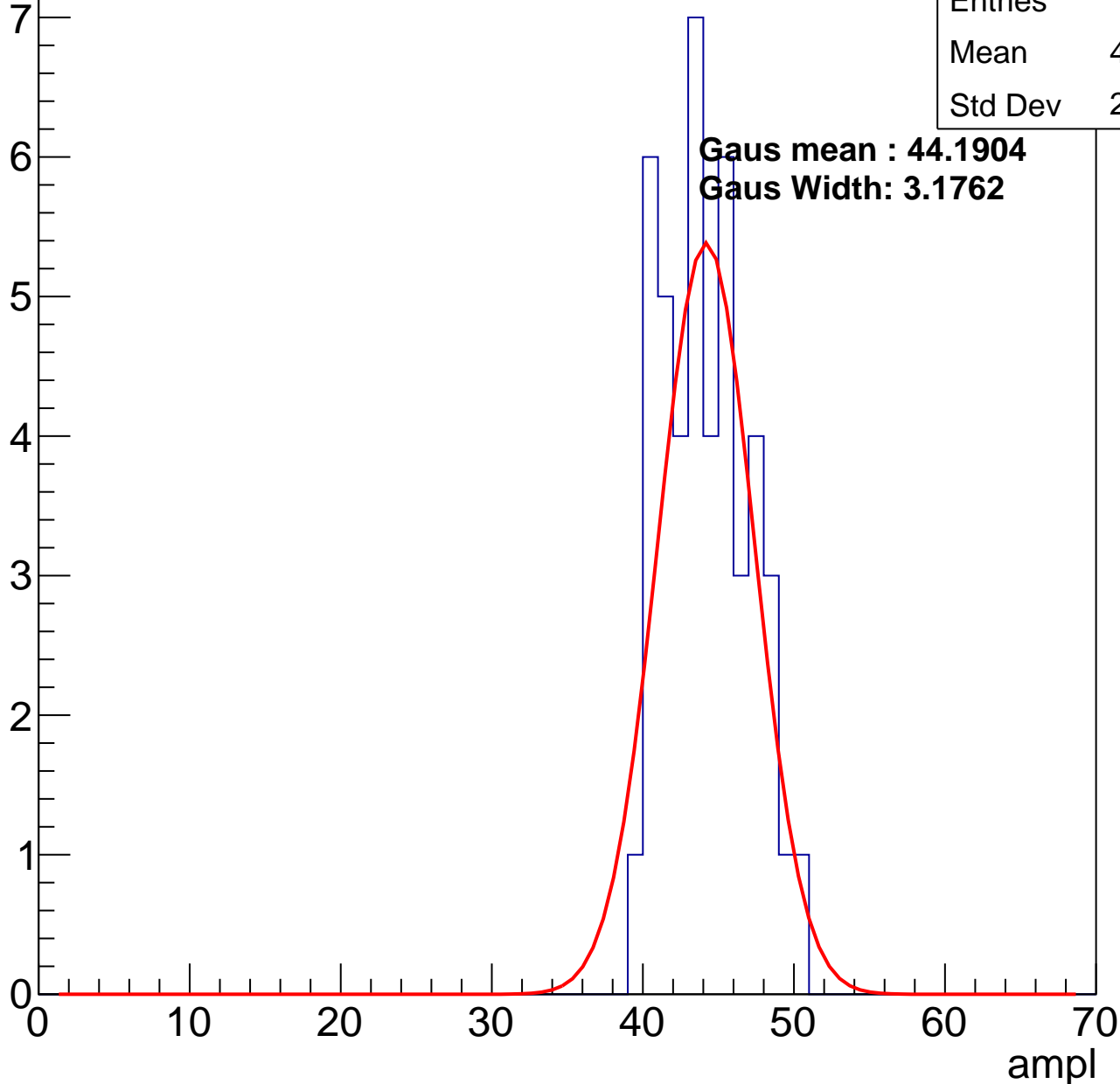
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	45
Mean	43.73
Std Dev	2.784

**Gaus mean : 44.1904**

**Gaus Width: 3.1762**

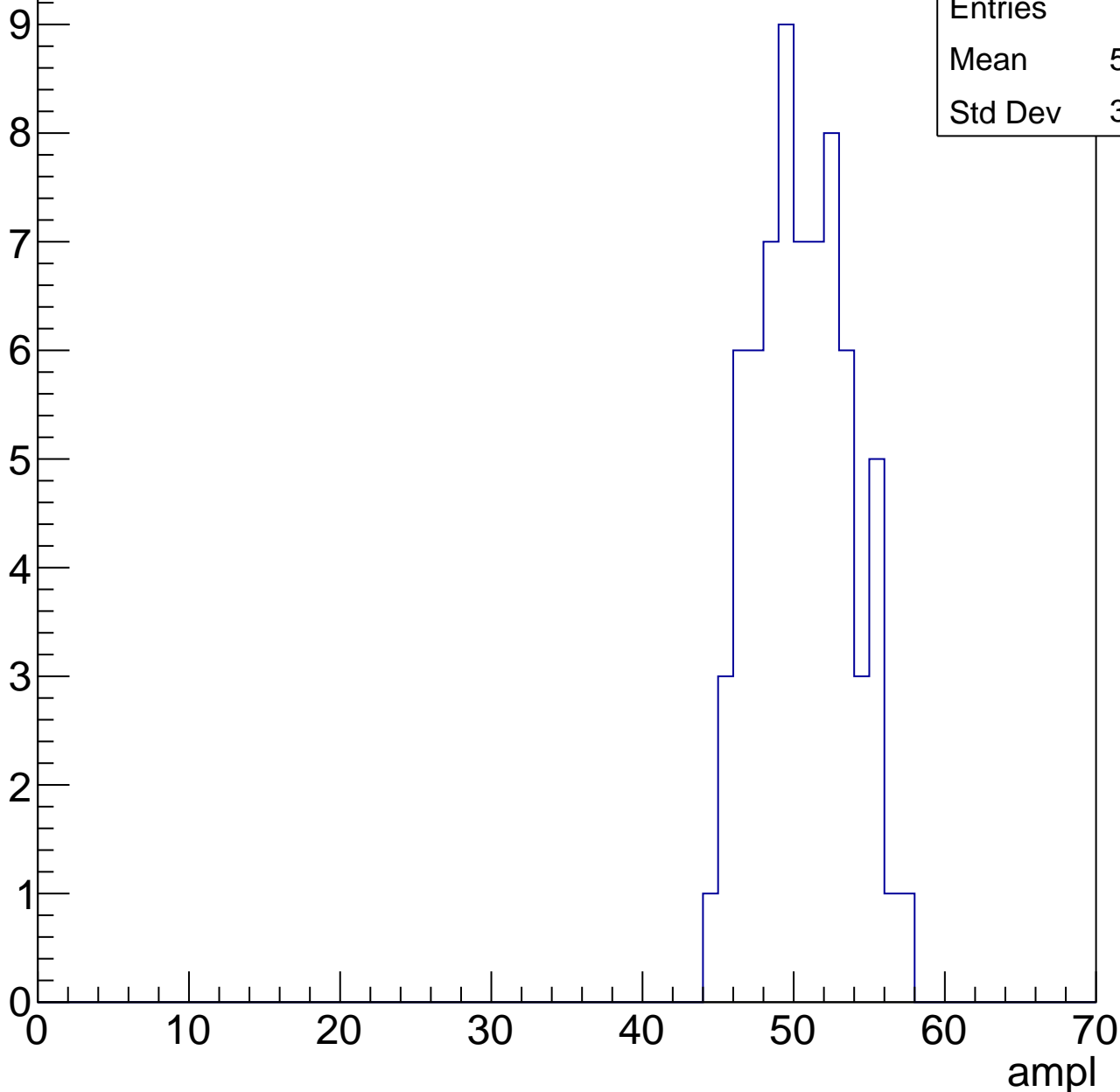


# B1L003S, U6-ch20, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	50.07
Std Dev	3.044

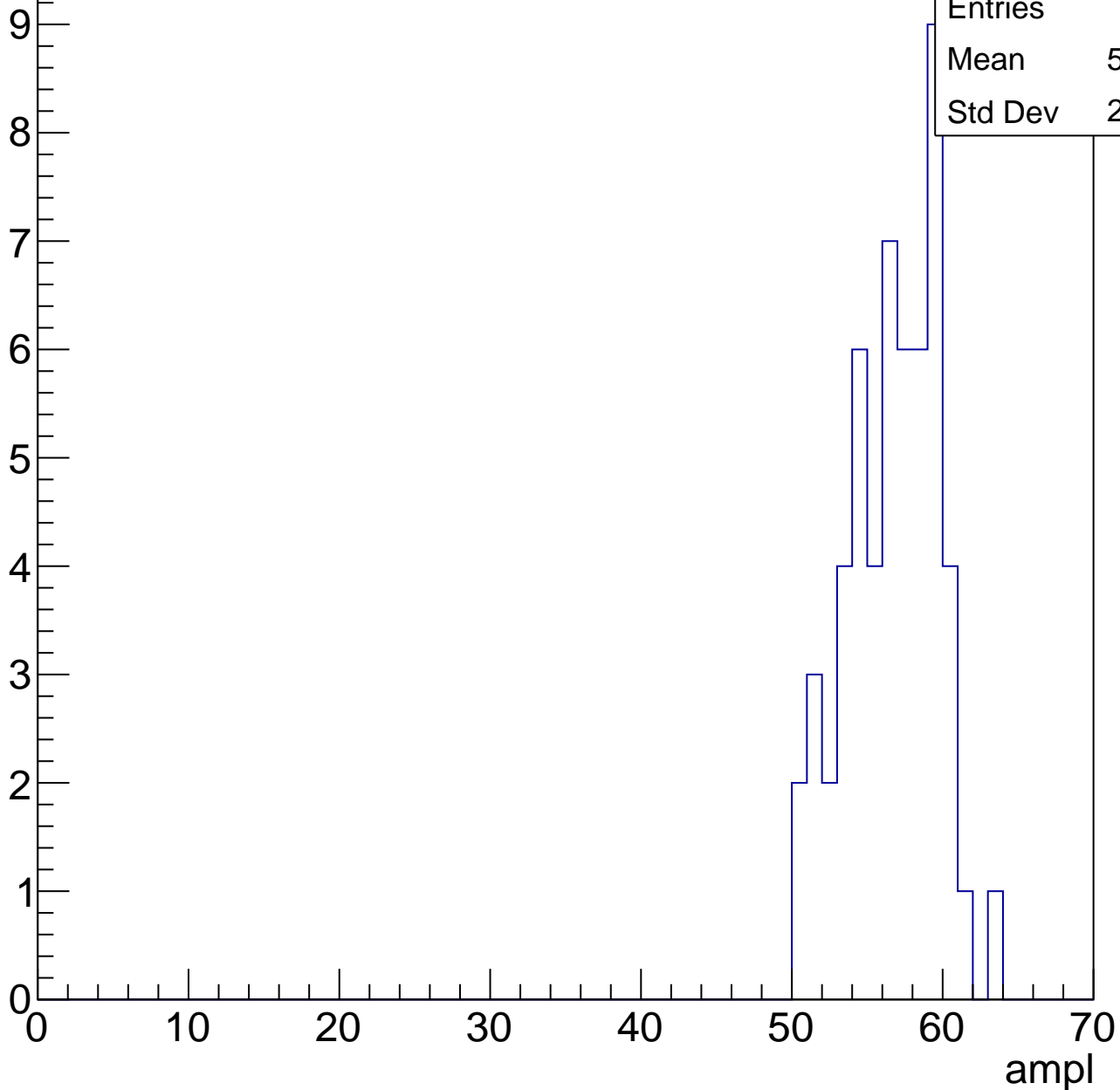


# B1L003S, U6-ch20, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	56.18
Std Dev	2.985

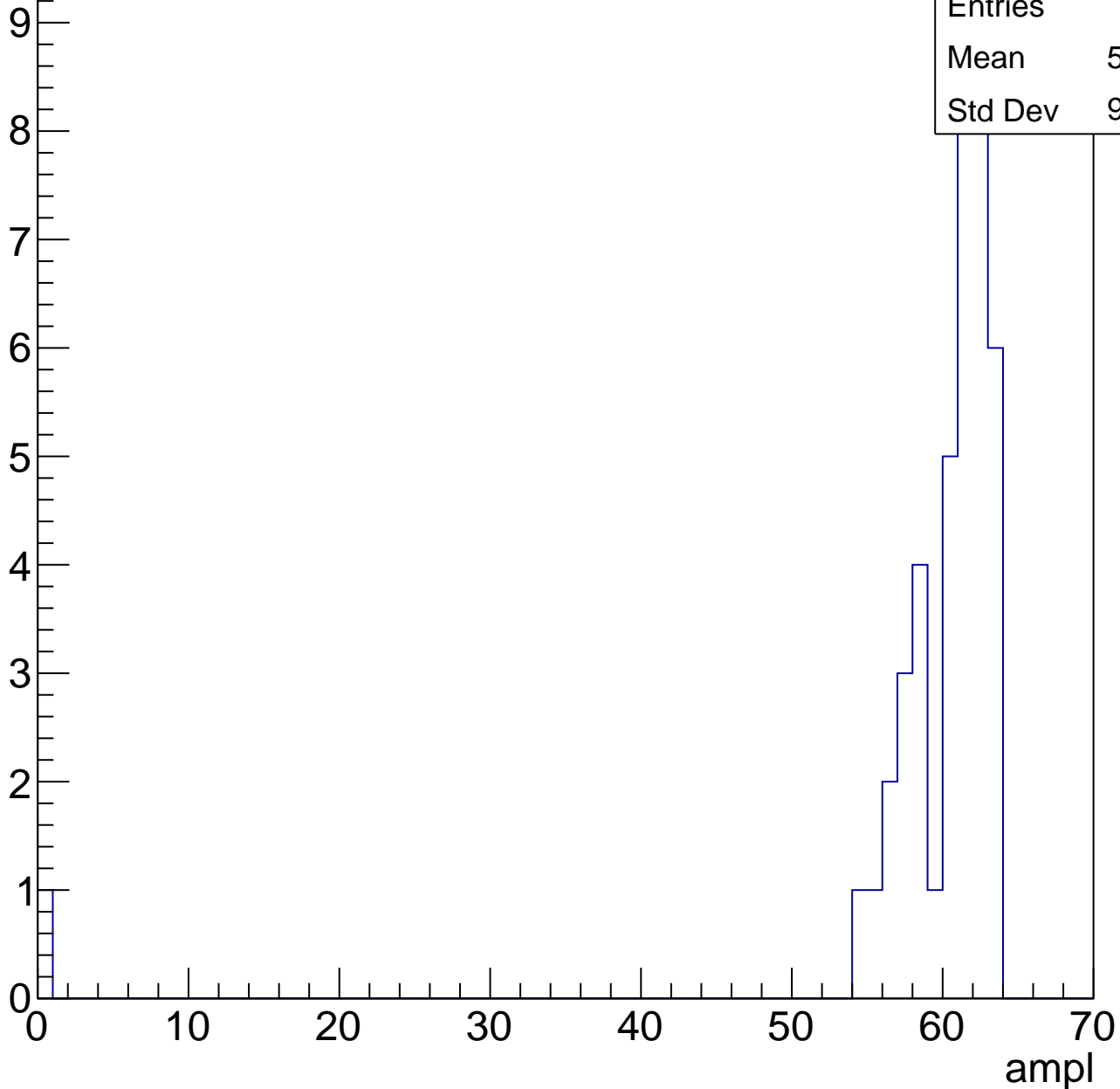


# B1L003S, U6-ch20, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

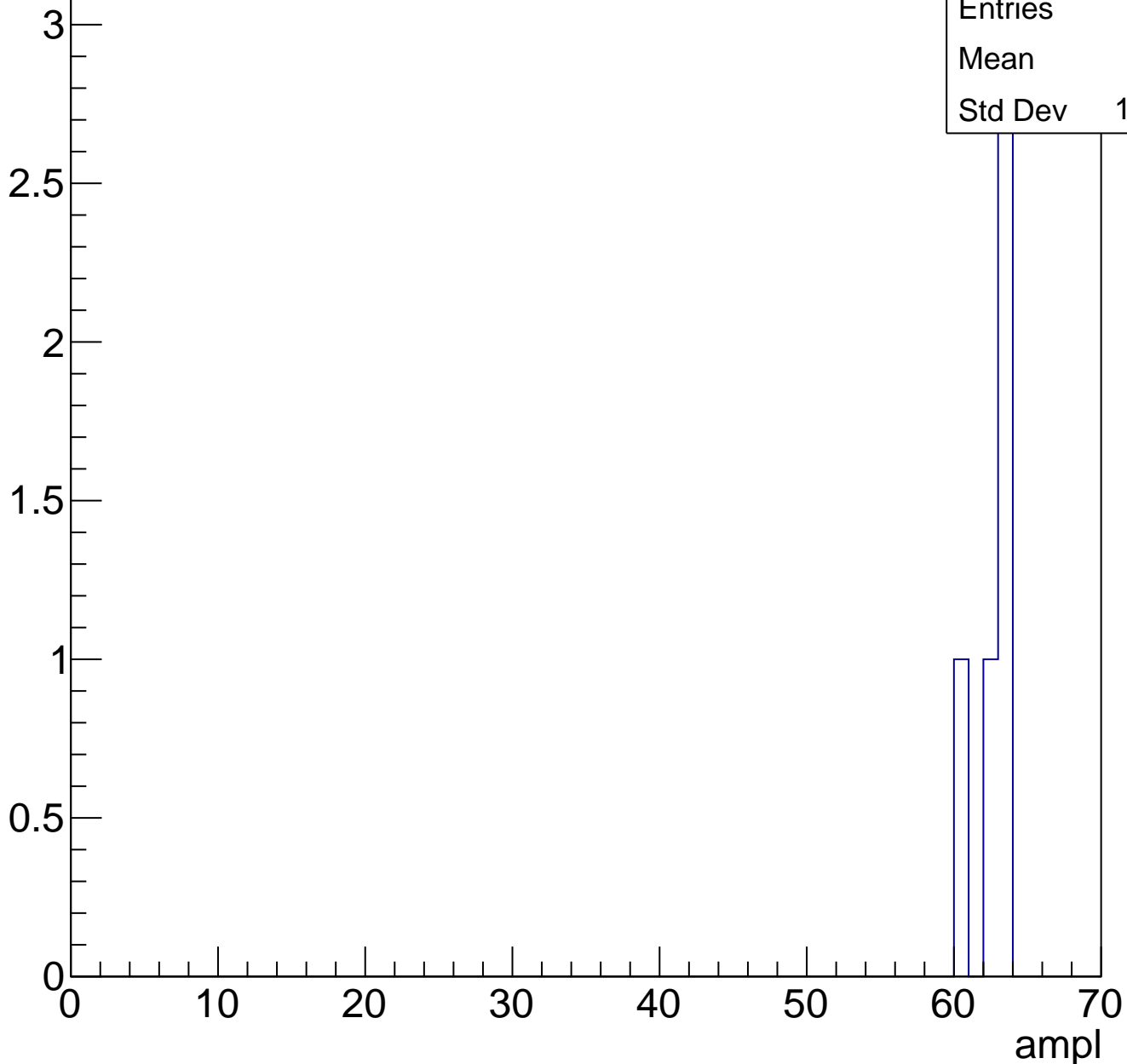
Entries	42
Mean	58.76
Std Dev	9.476



# B1L003S, U6-ch20, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch20, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U6-ch21, adc0

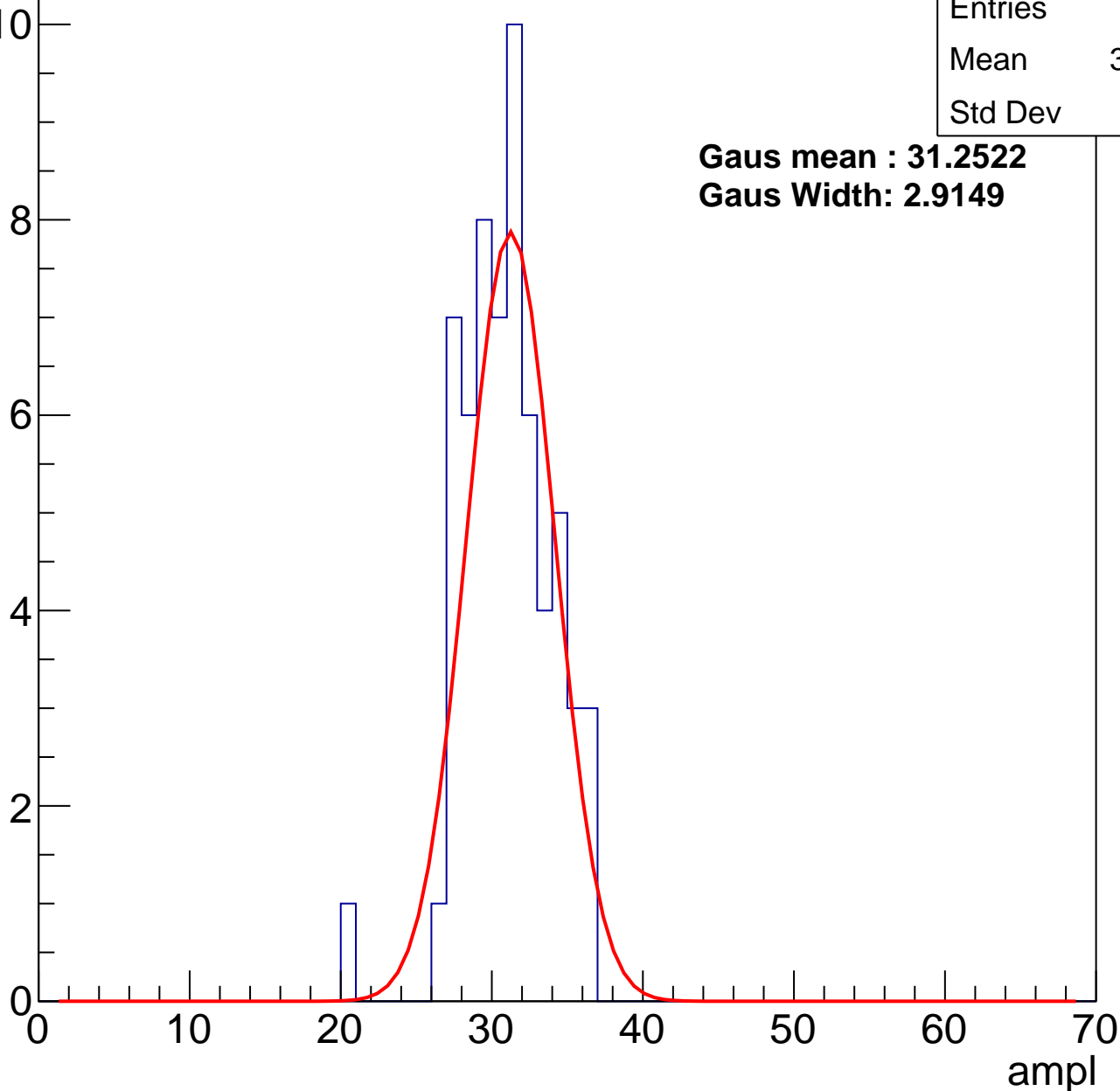
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	30.52
Std Dev	2.94

**Gaus mean : 31.2522**

**Gaus Width: 2.9149**

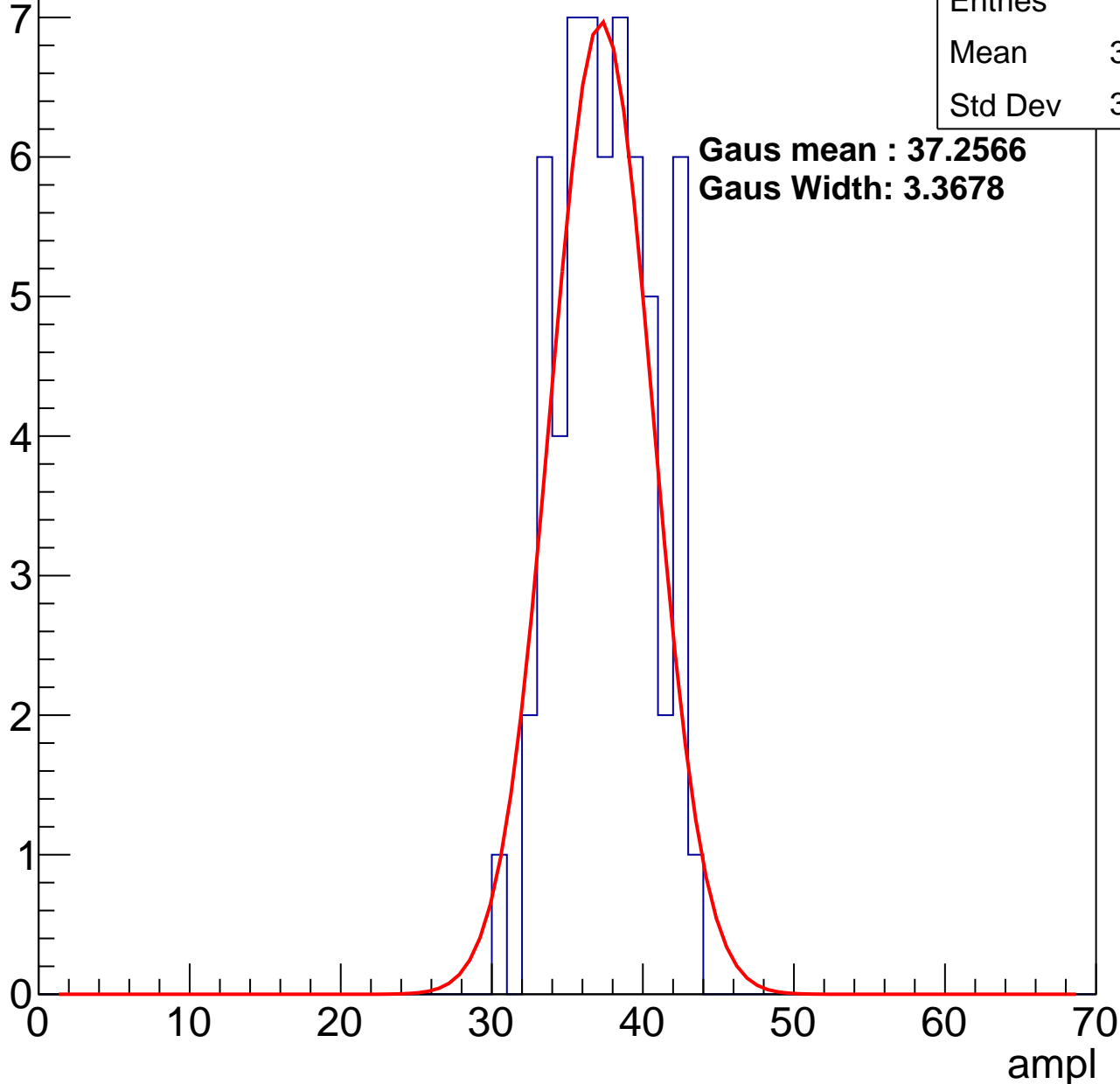


# B1L003S, U6-ch21, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	37.07
Std Dev	3.054



# B1L003S, U6-ch21, adc2

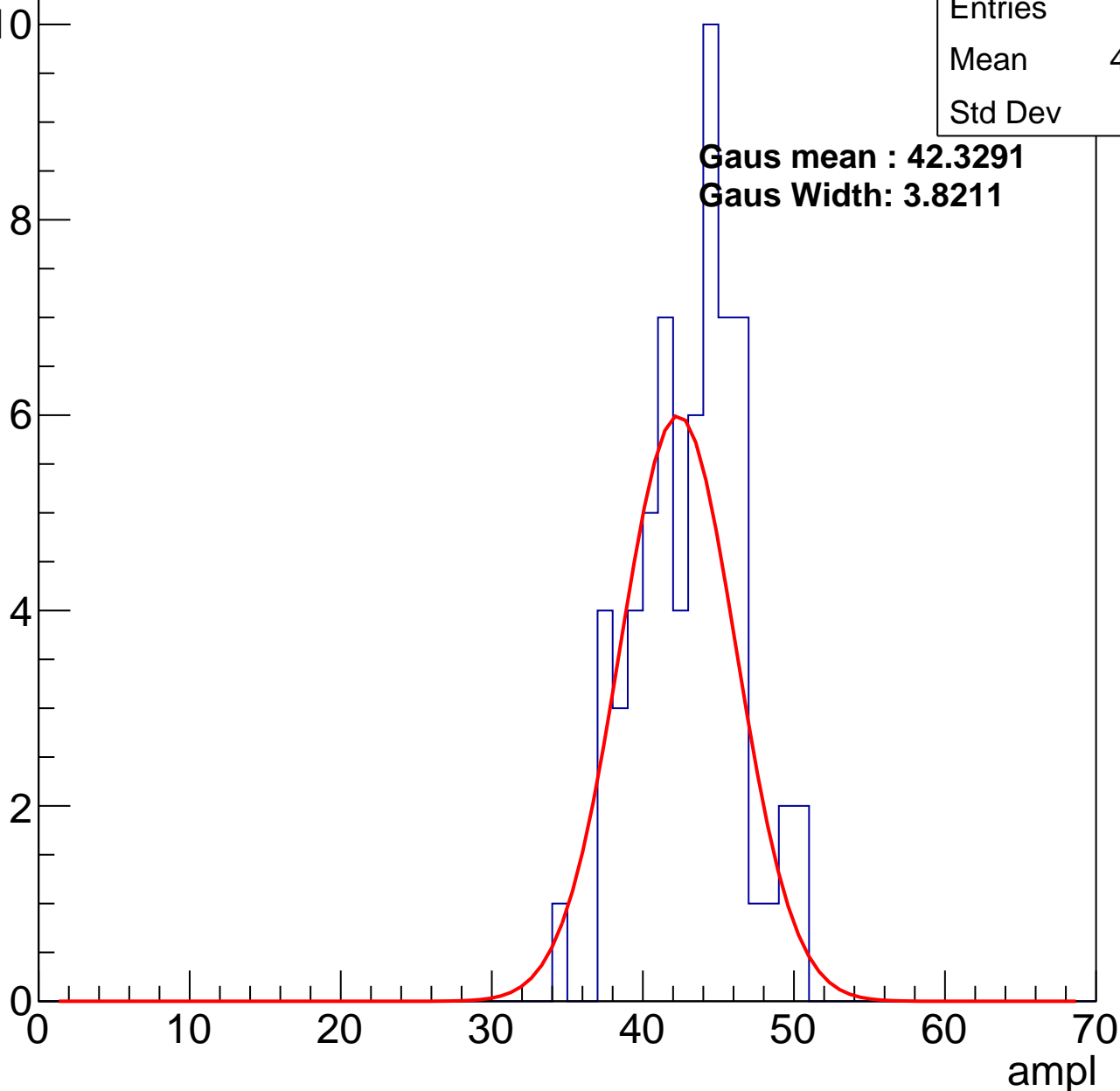
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	42.73
Std Dev	3.42

**Gaus mean : 42.3291**

**Gaus Width: 3.8211**

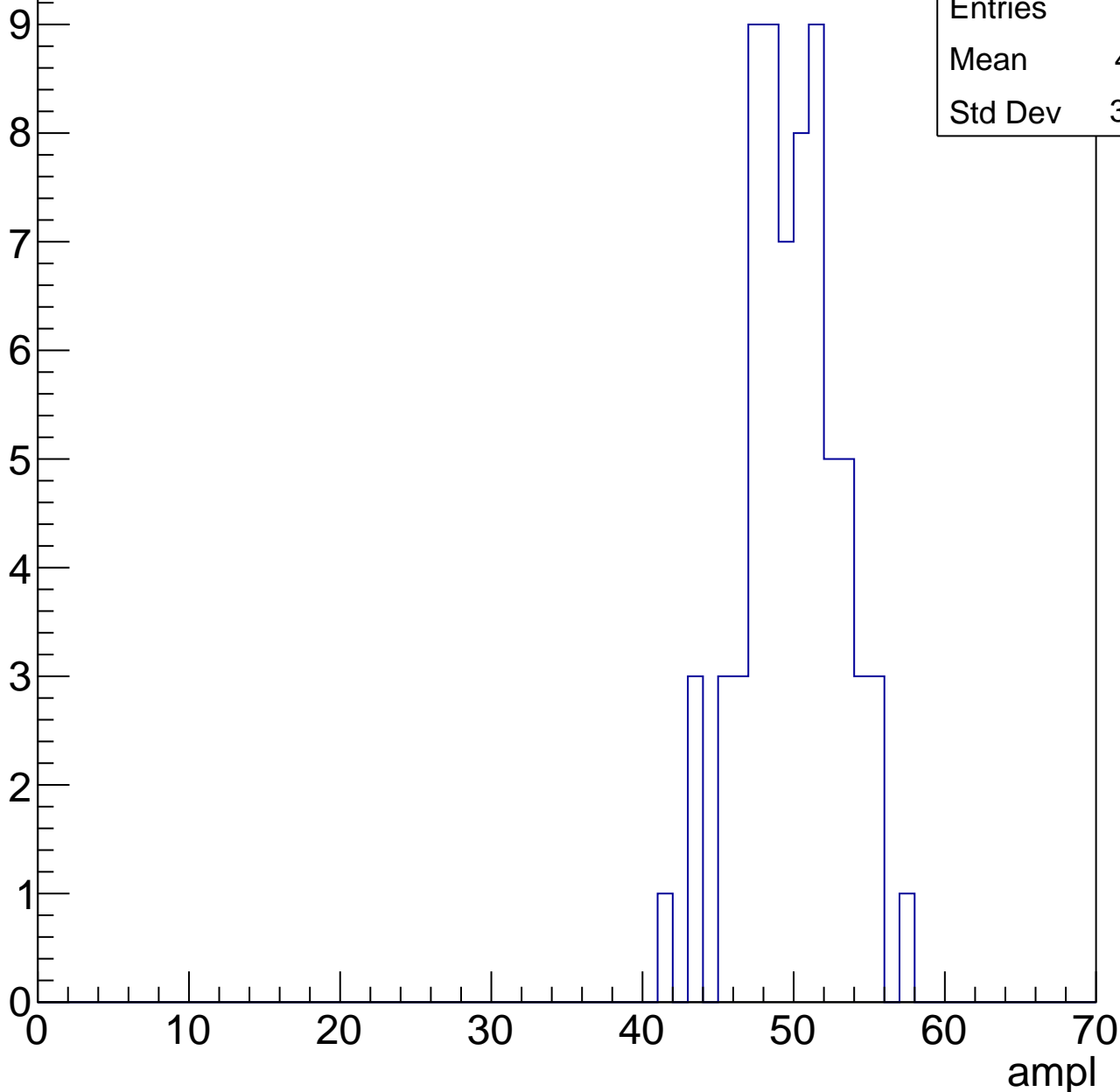


# B1L003S, U6-ch21, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	49.41
Std Dev	3.177

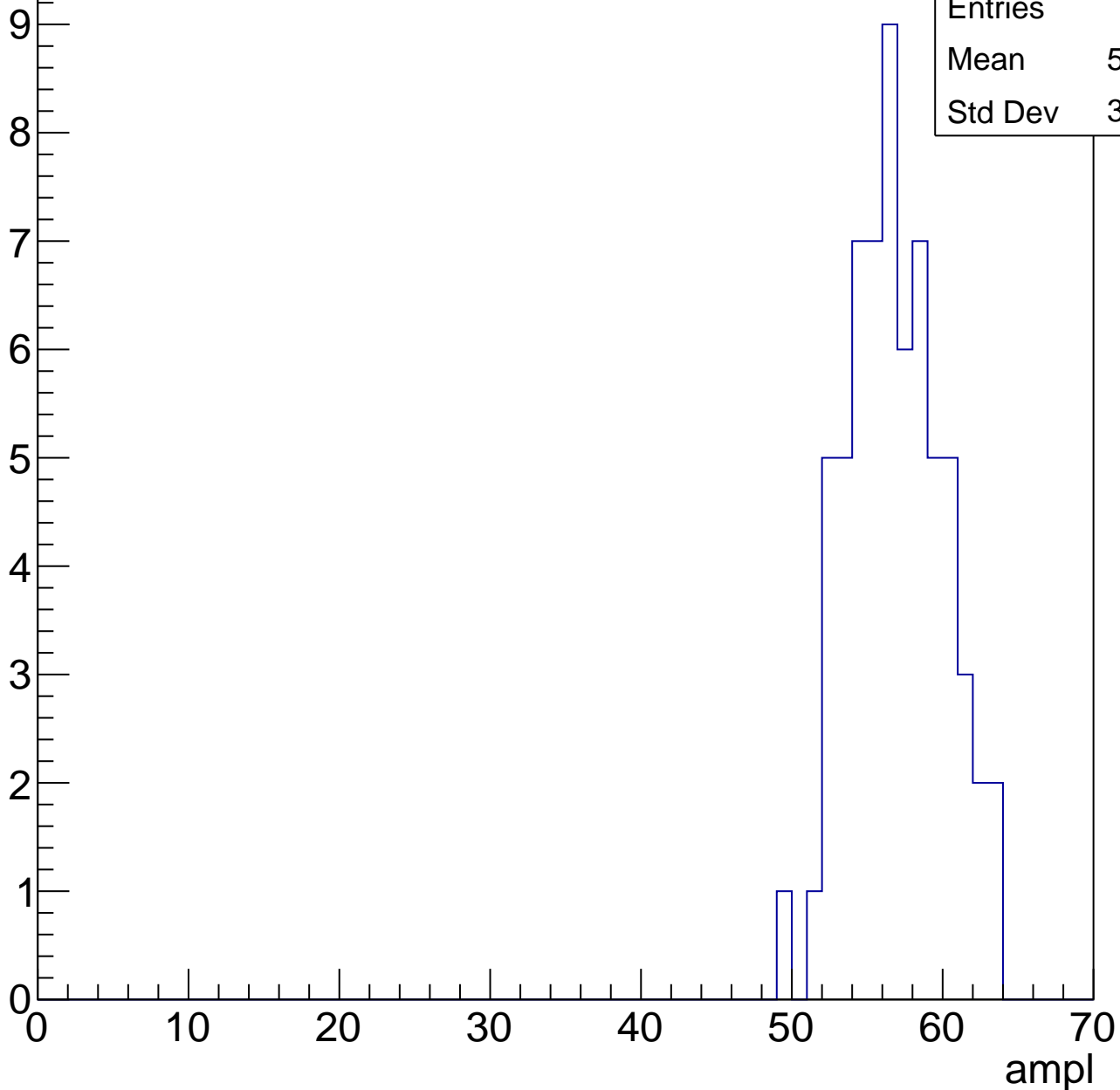


# B1L003S, U6-ch21, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	56.43
Std Dev	3.103

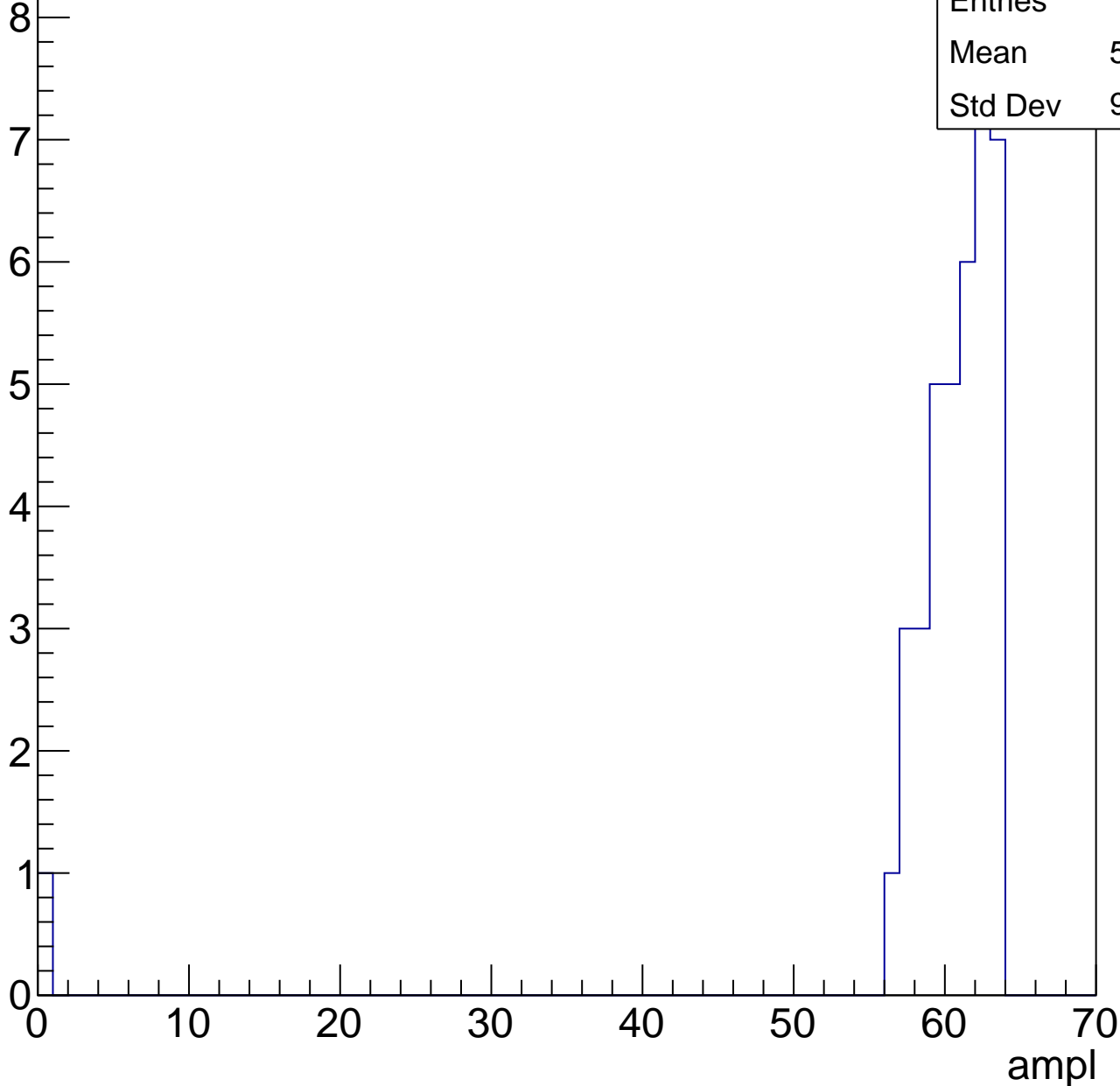


# B1L003S, U6-ch21, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

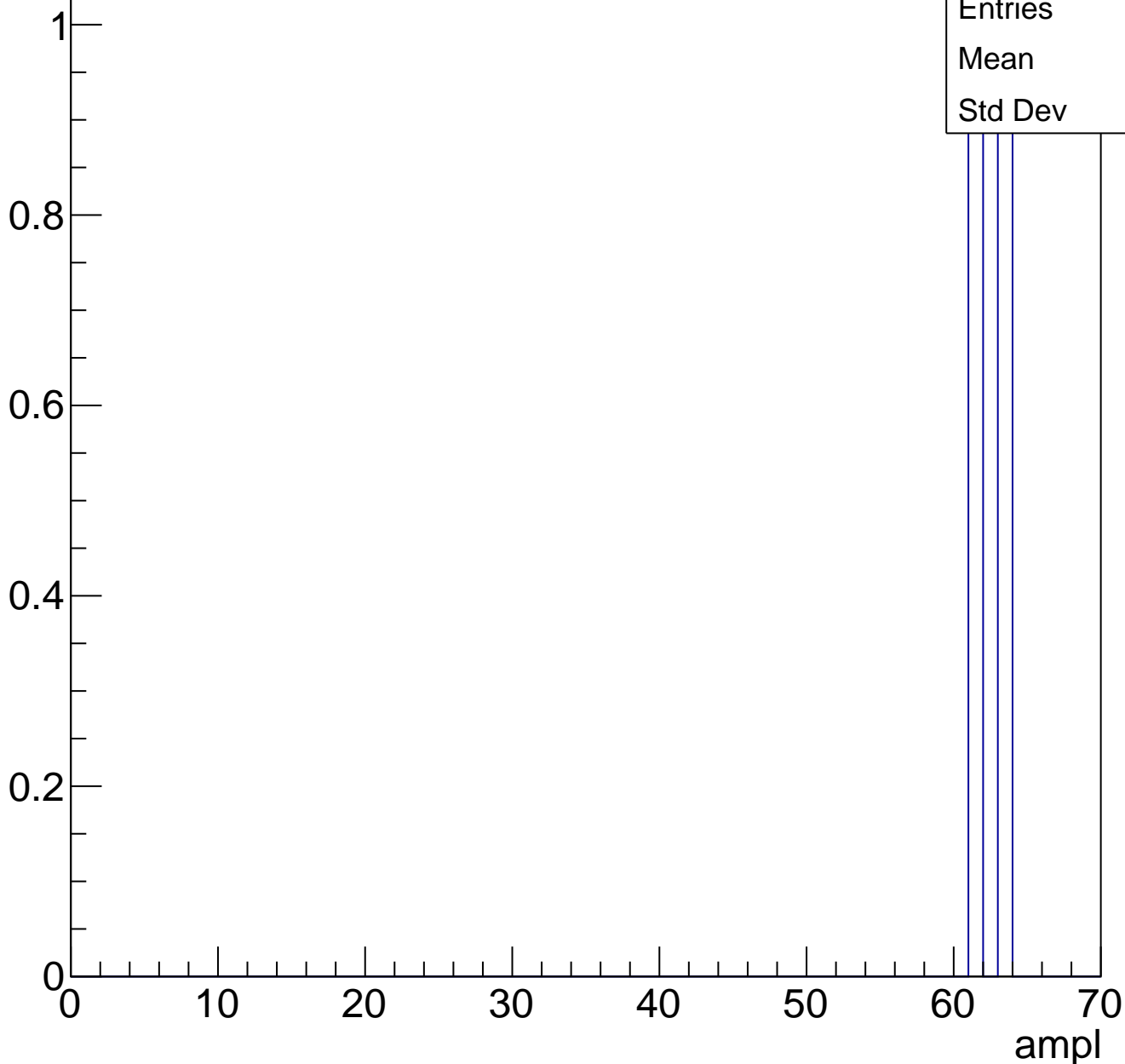
Entries	39
Mean	58.95
Std Dev	9.764



# B1L003S, U6-ch21, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch21, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch22, adc0

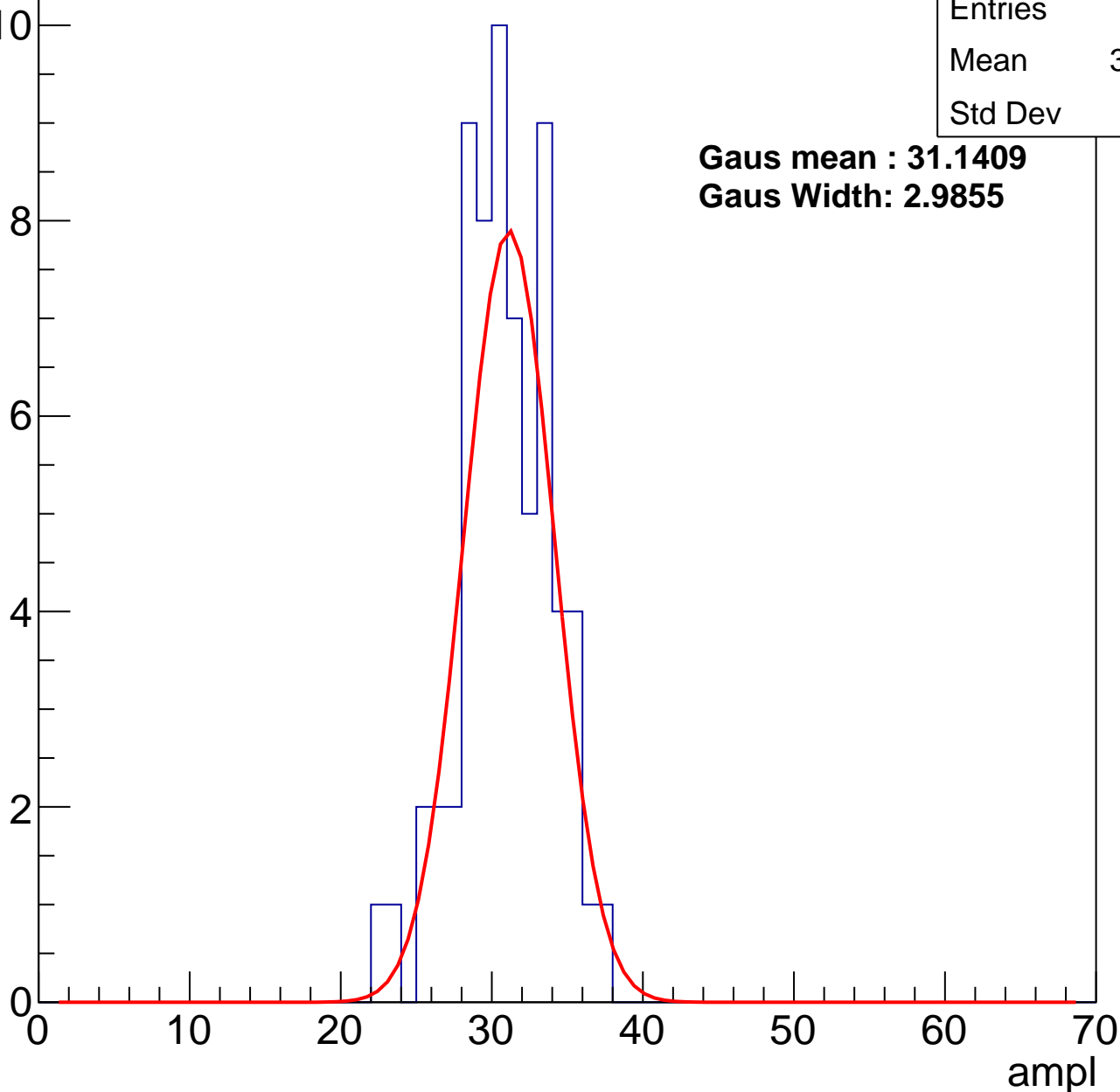
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	30.42
Std Dev	3.02

**Gaus mean : 31.1409**

**Gaus Width: 2.9855**



# B1L003S, U6-ch22, adc1

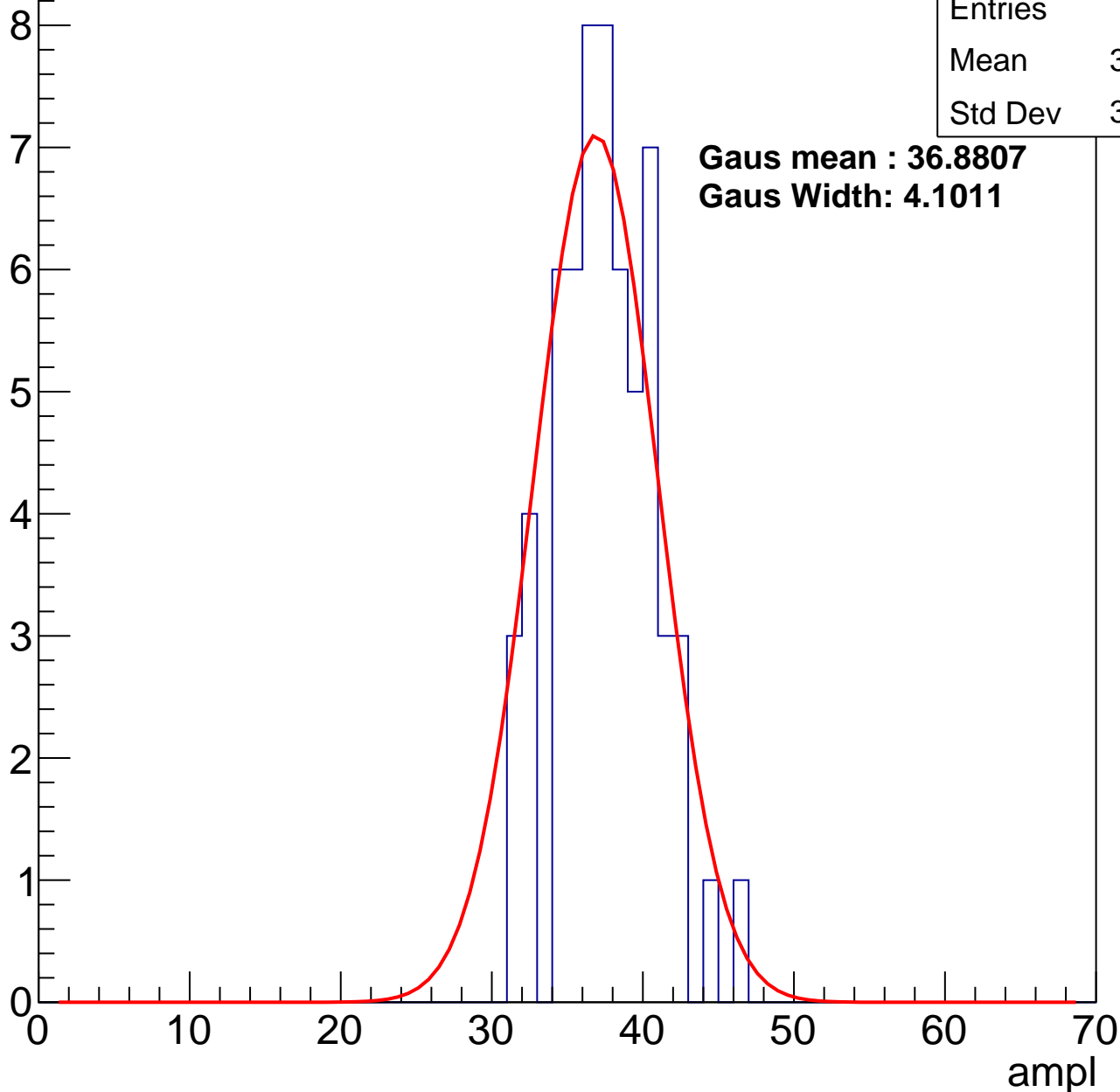
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	37.07
Std Dev	3.228

**Gaus mean : 36.8807**

**Gaus Width: 4.1011**



# B1L003S, U6-ch22, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	69
Mean	42.96
Std Dev	3.411

**Gaus mean : 43.8887**

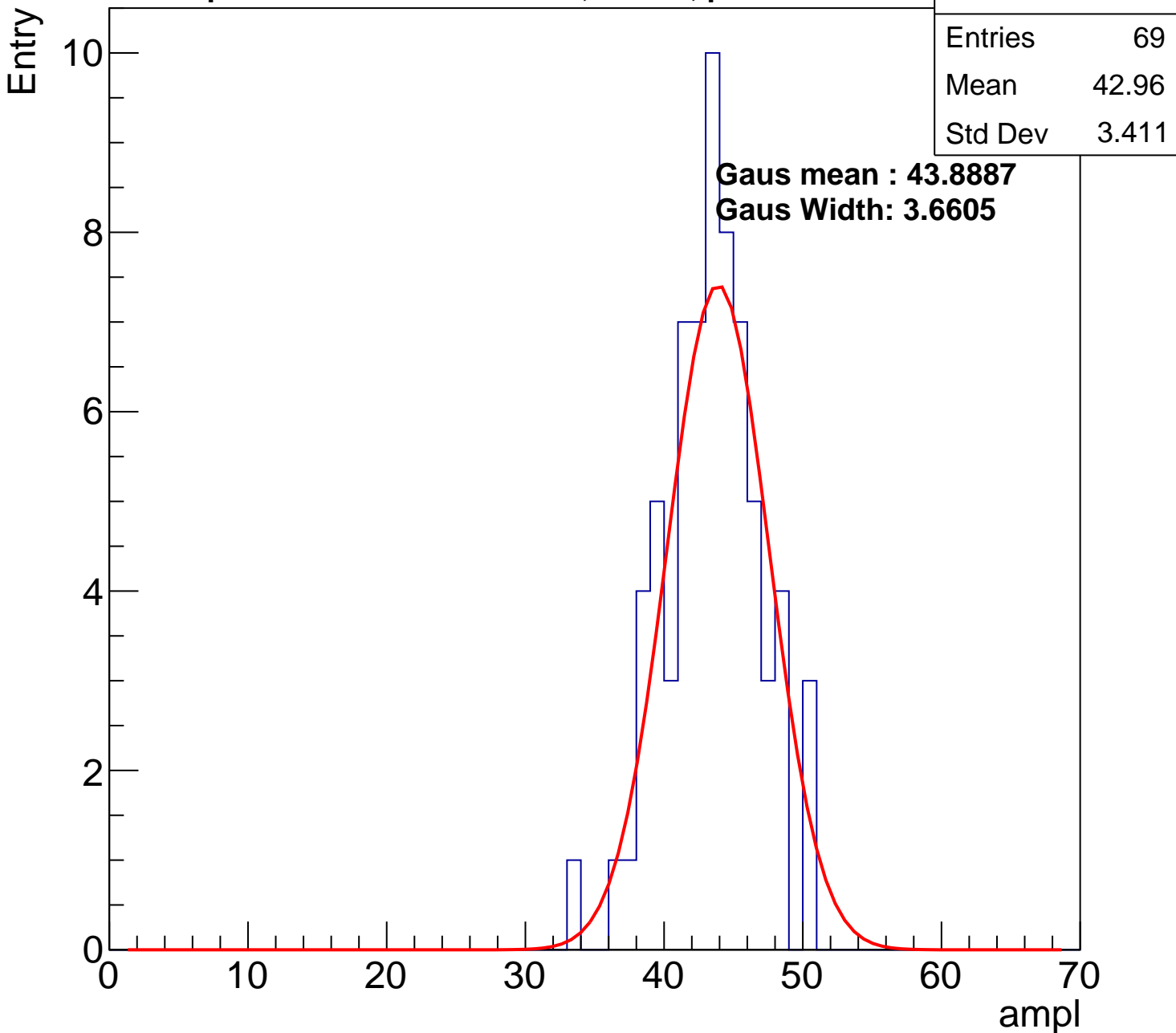
**Gaus Width: 3.6605**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

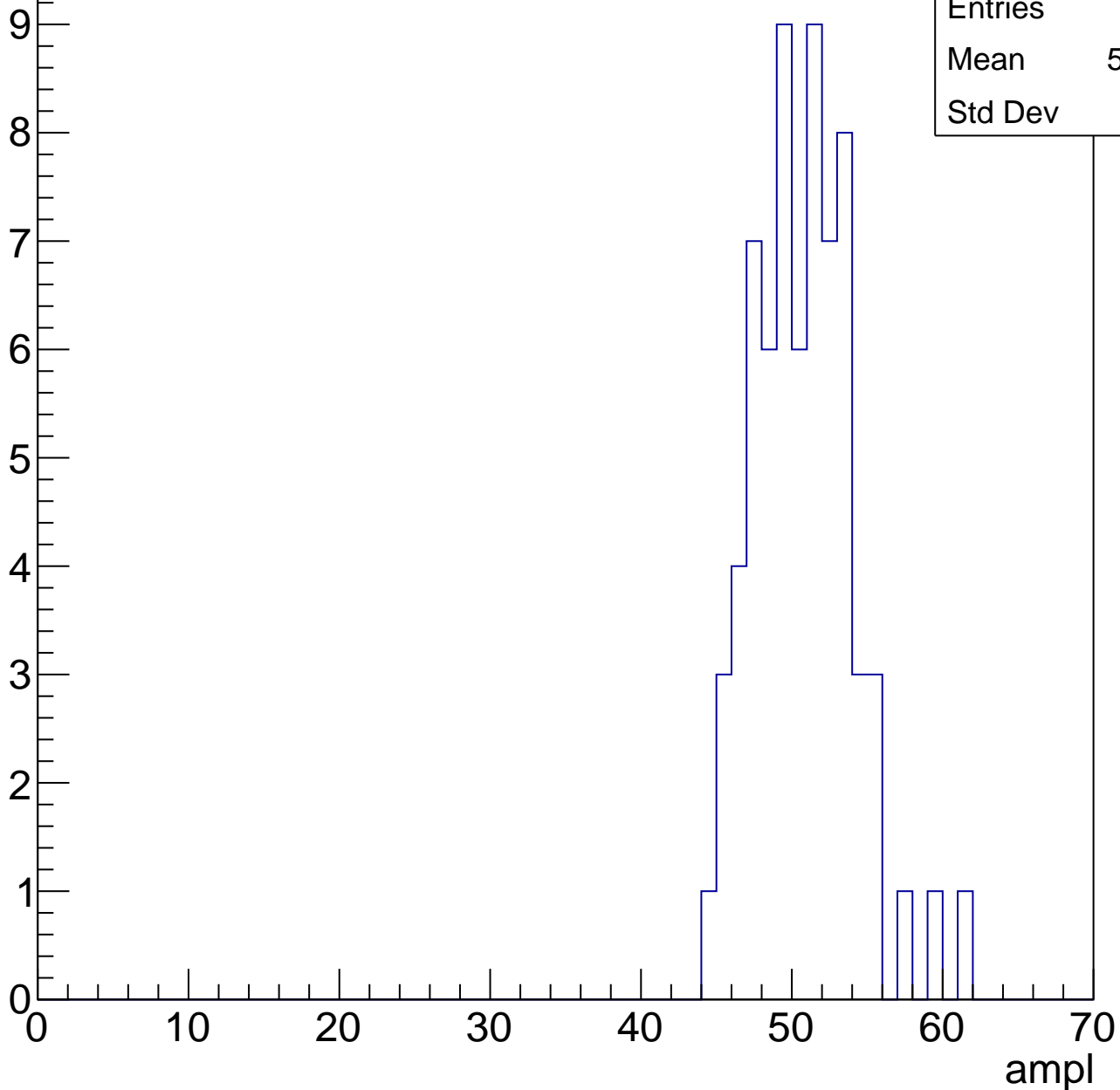


# B1L003S, U6-ch22, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

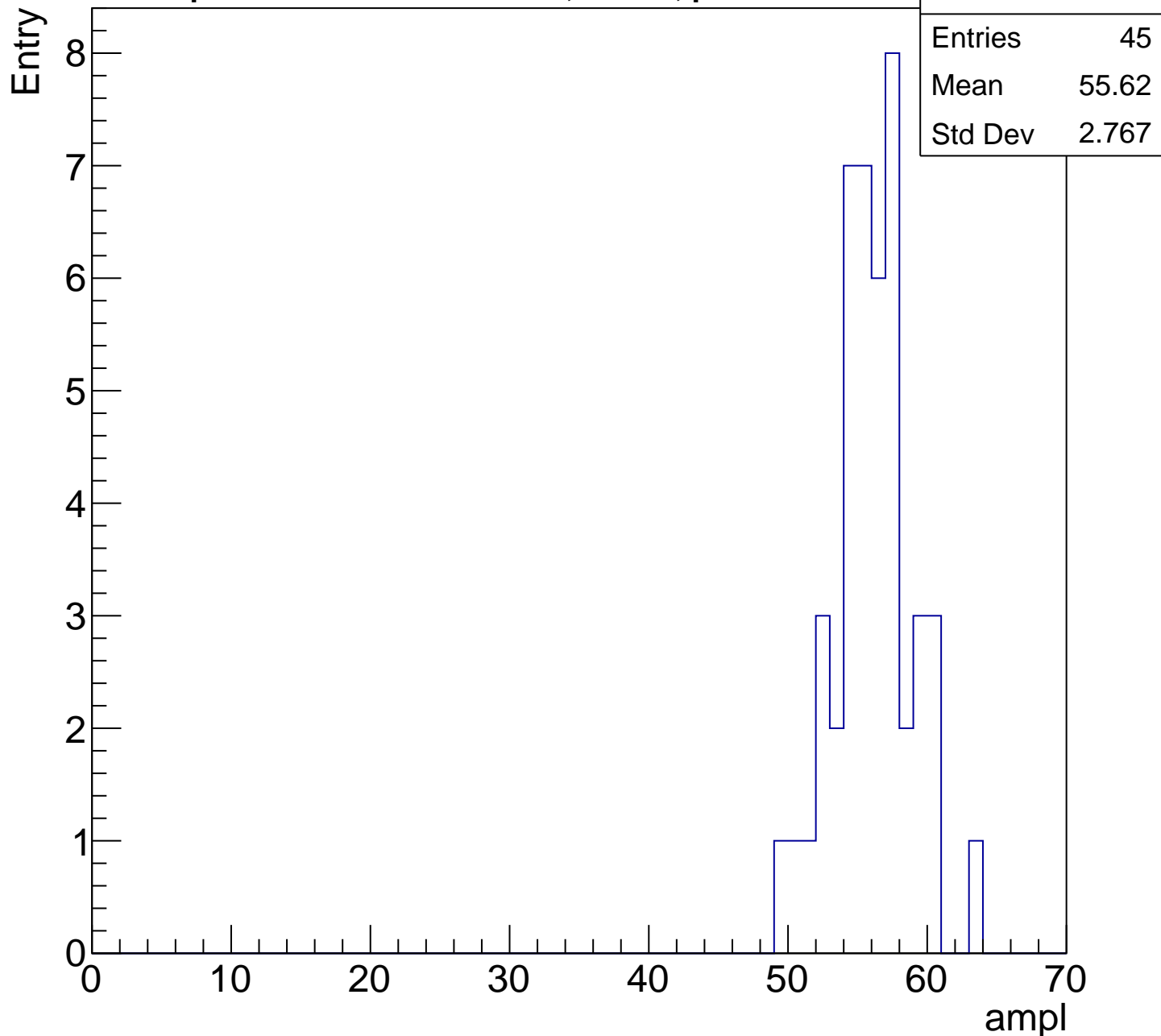
Entry

Entries	69
Mean	50.32
Std Dev	3.29



# B1L003S, U6-ch22, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2



# B1L003S, U6-ch22, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	51
Mean	58.94
Std Dev	8.587

ampl

0

10

20

30

40

50

60

70

# B1L003S, U6-ch22, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch22, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L003S, U6-ch23, adc0

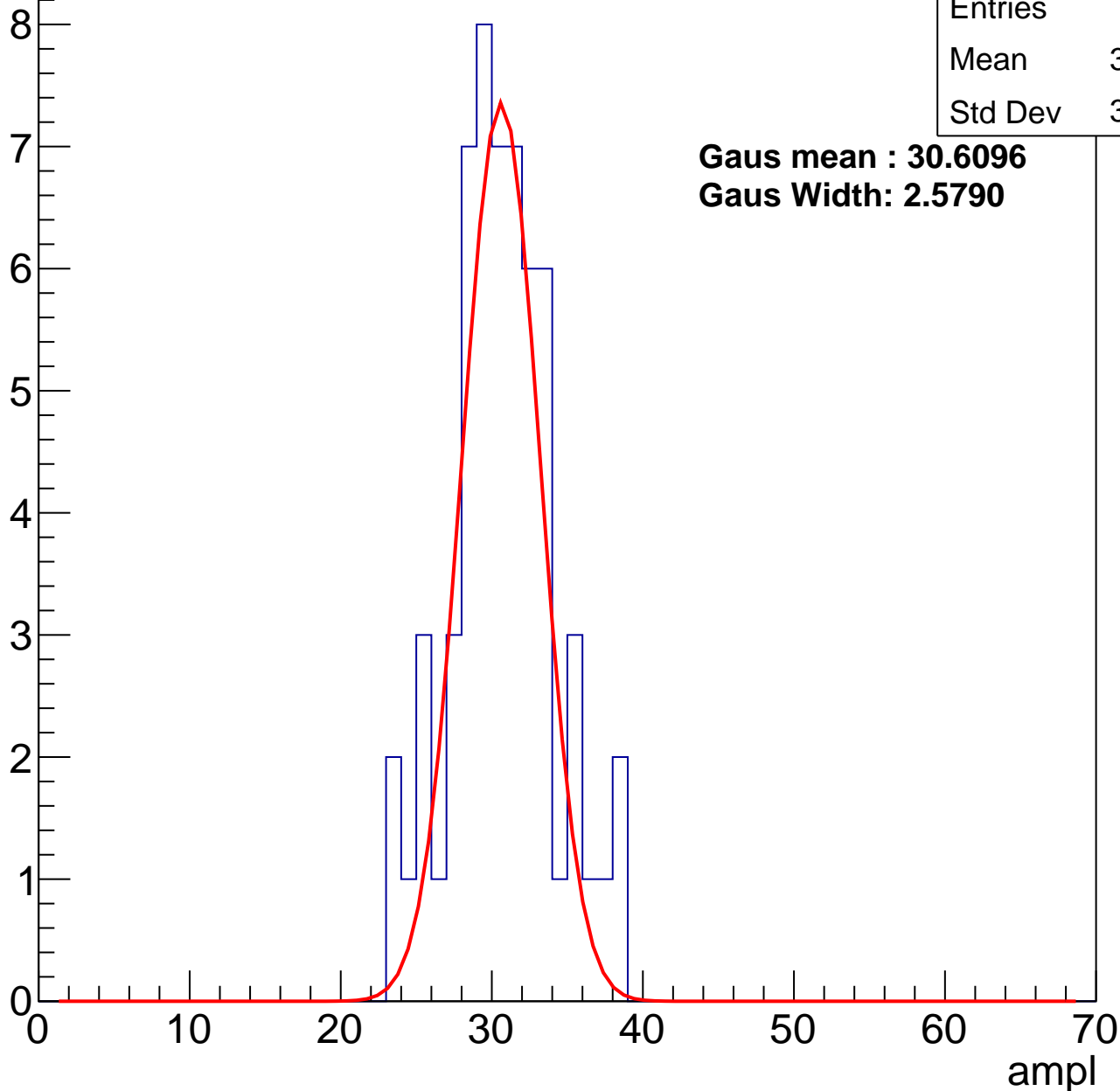
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	30.25
Std Dev	3.378

**Gaus mean : 30.6096**

**Gaus Width: 2.5790**



# B1L003S, U6-ch23, adc1

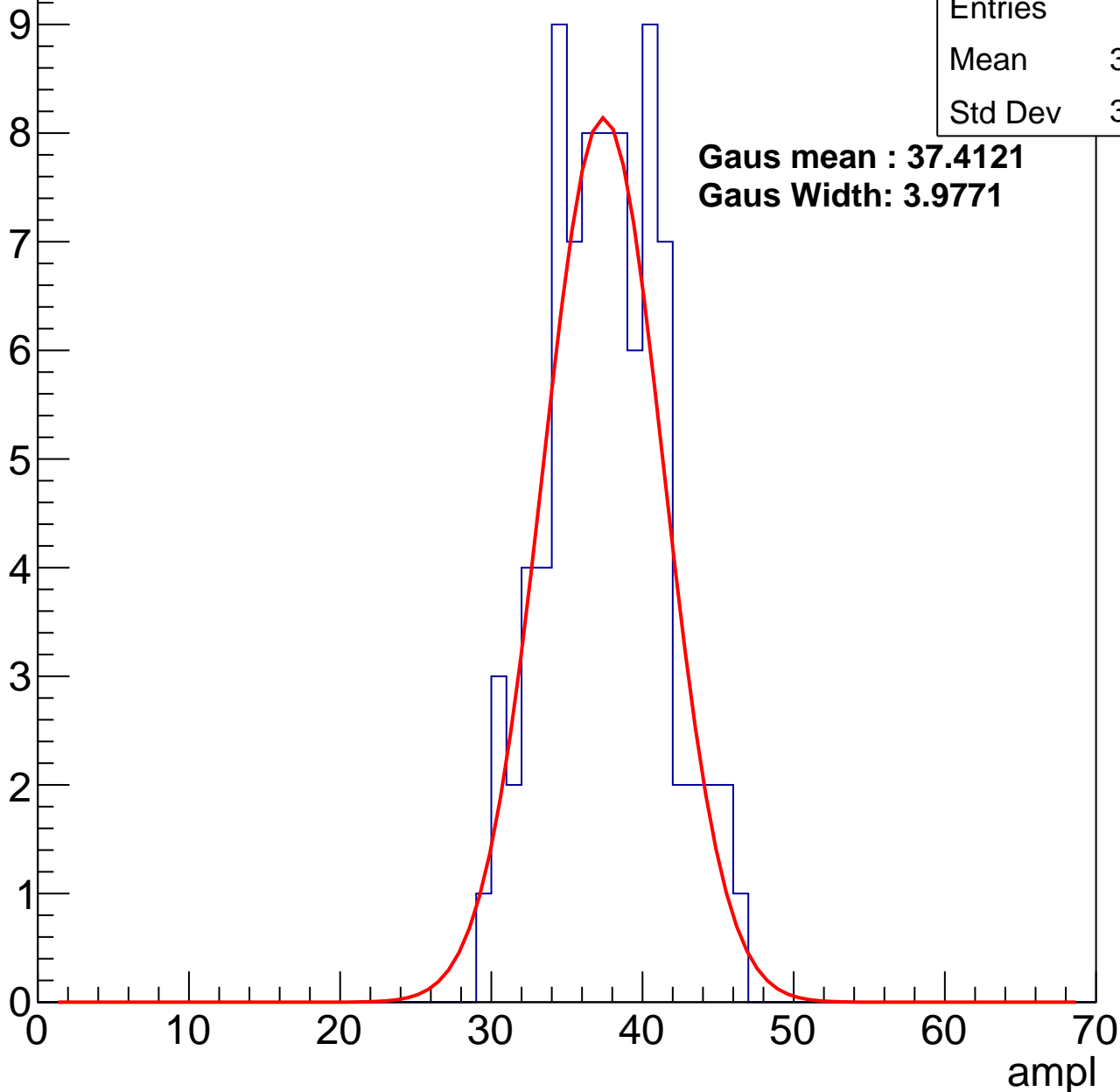
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	85
Mean	37.12
Std Dev	3.784

**Gaus mean : 37.4121**

**Gaus Width: 3.9771**



# B1L003S, U6-ch23, adc2

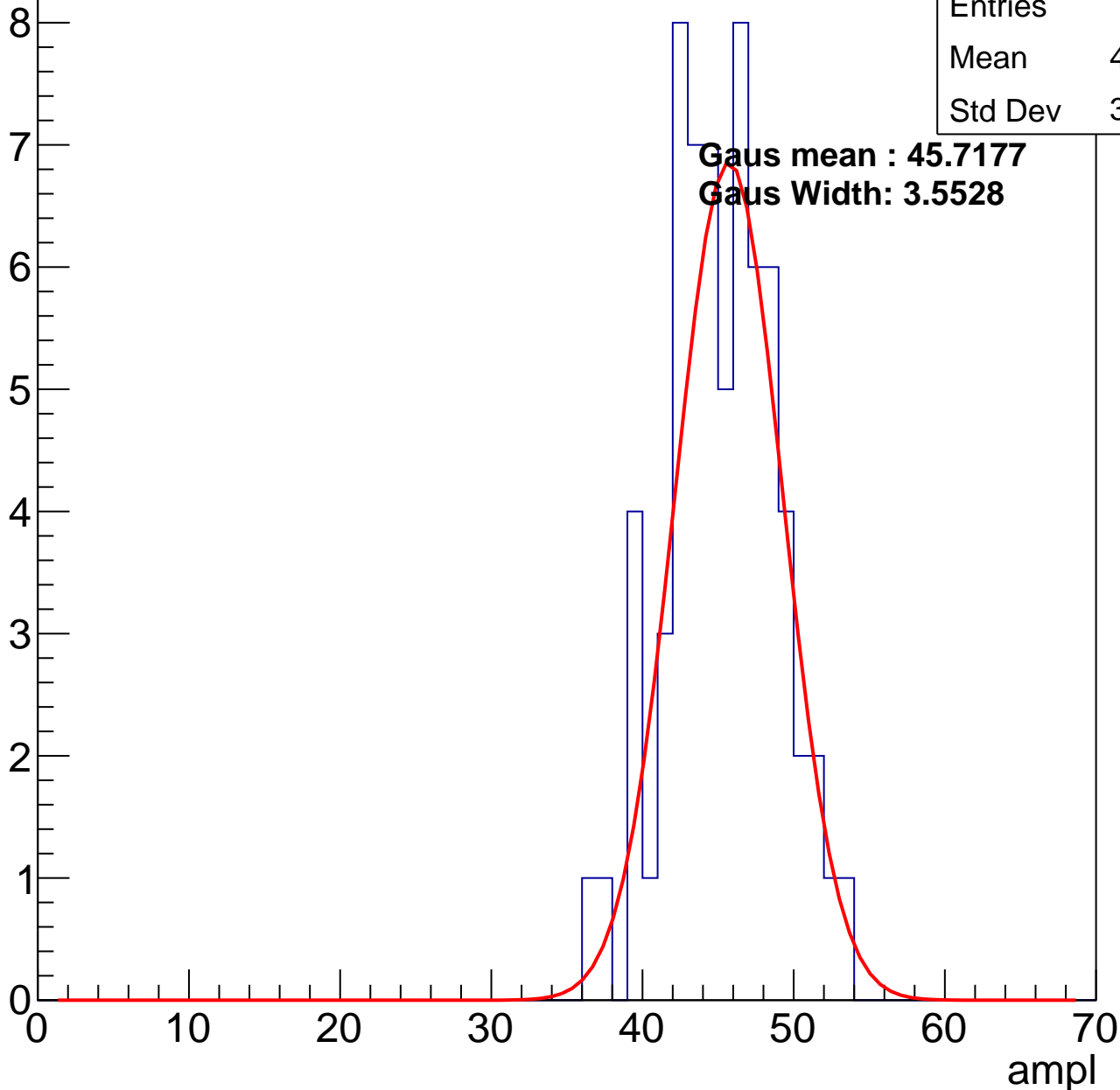
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	44.82
Std Dev	3.566

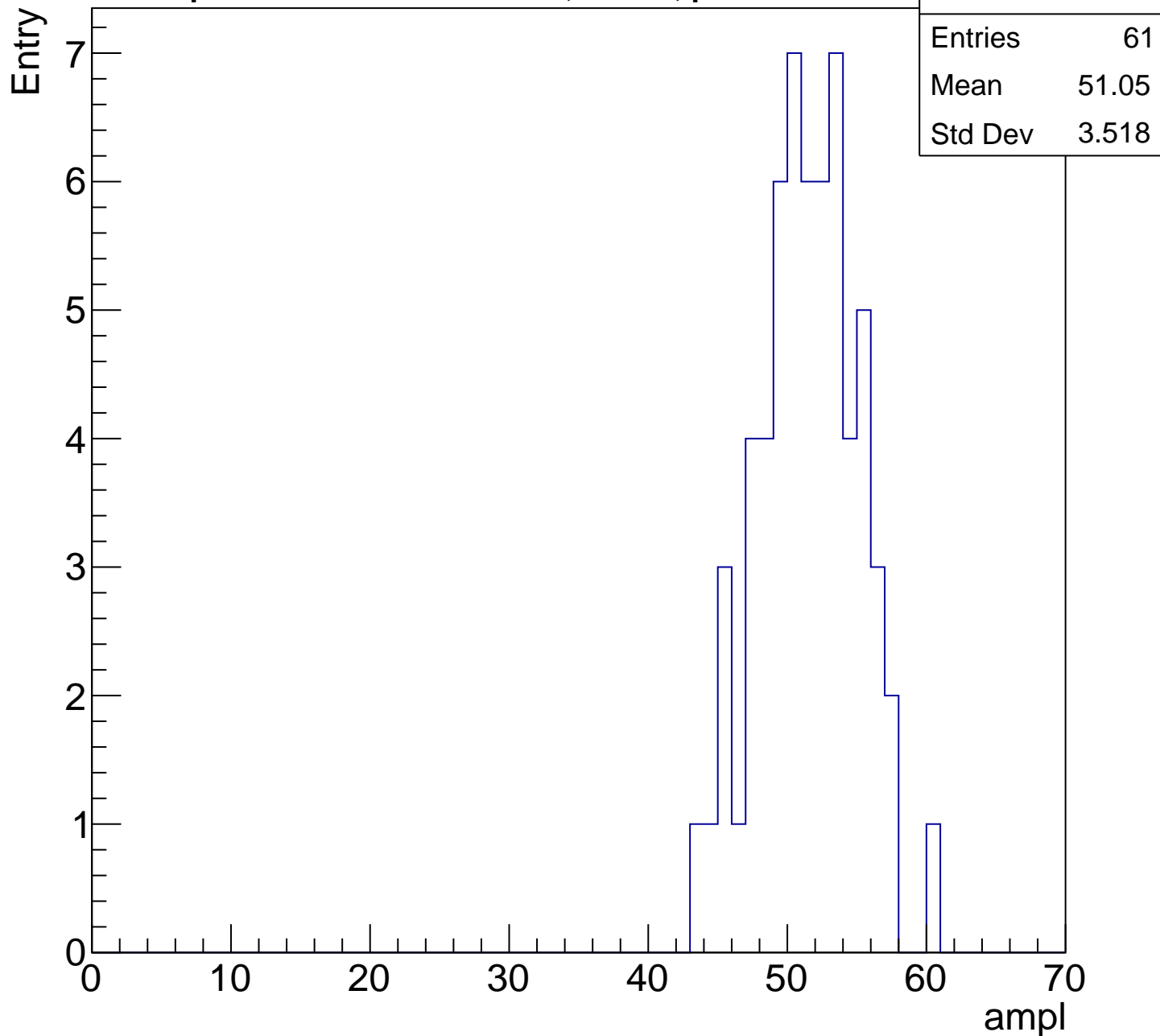
**Gaus mean : 45.7177**

**Gaus Width: 3.5528**



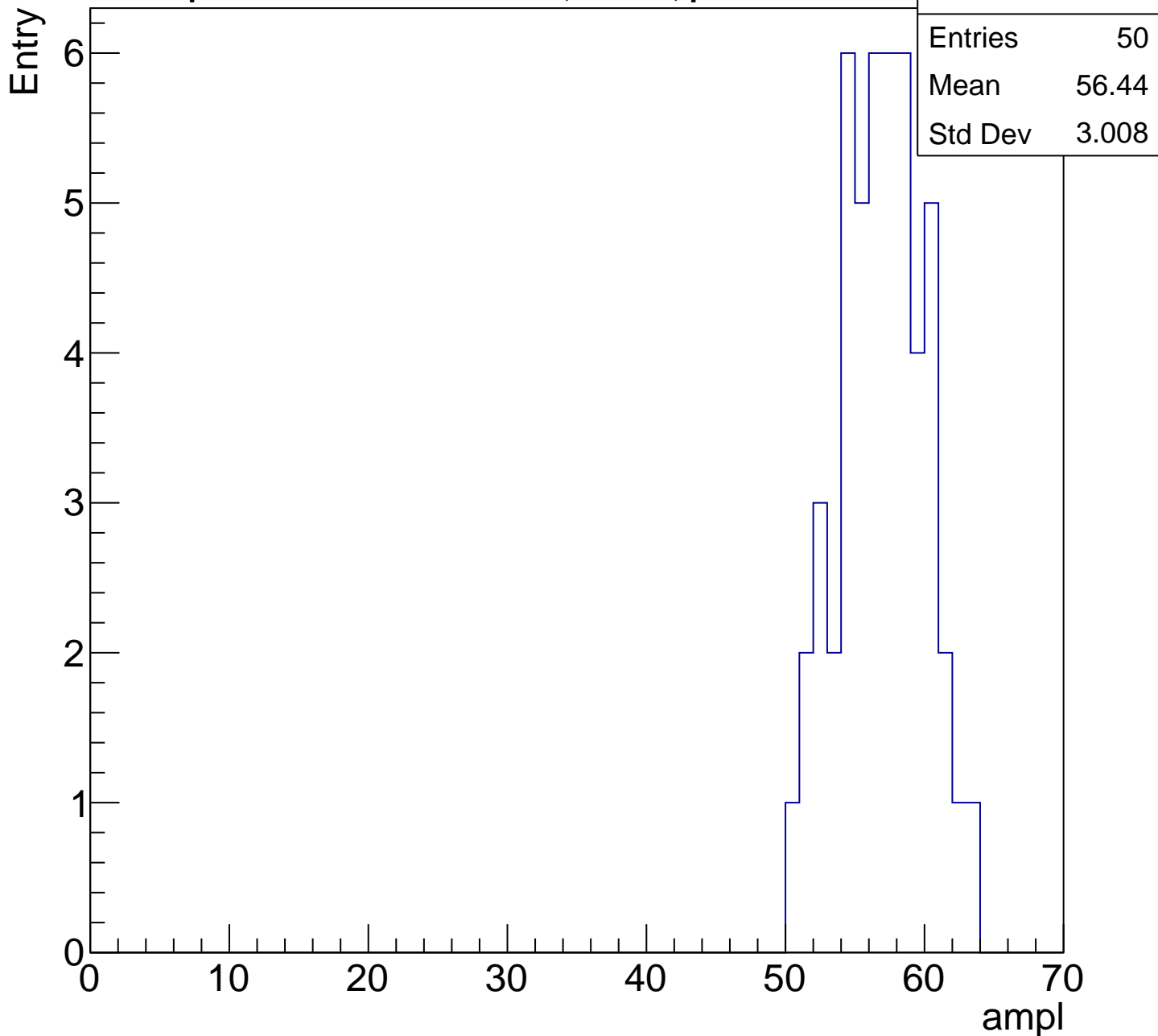
# B1L003S, U6-ch23, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2



# B1L003S, U6-ch23, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

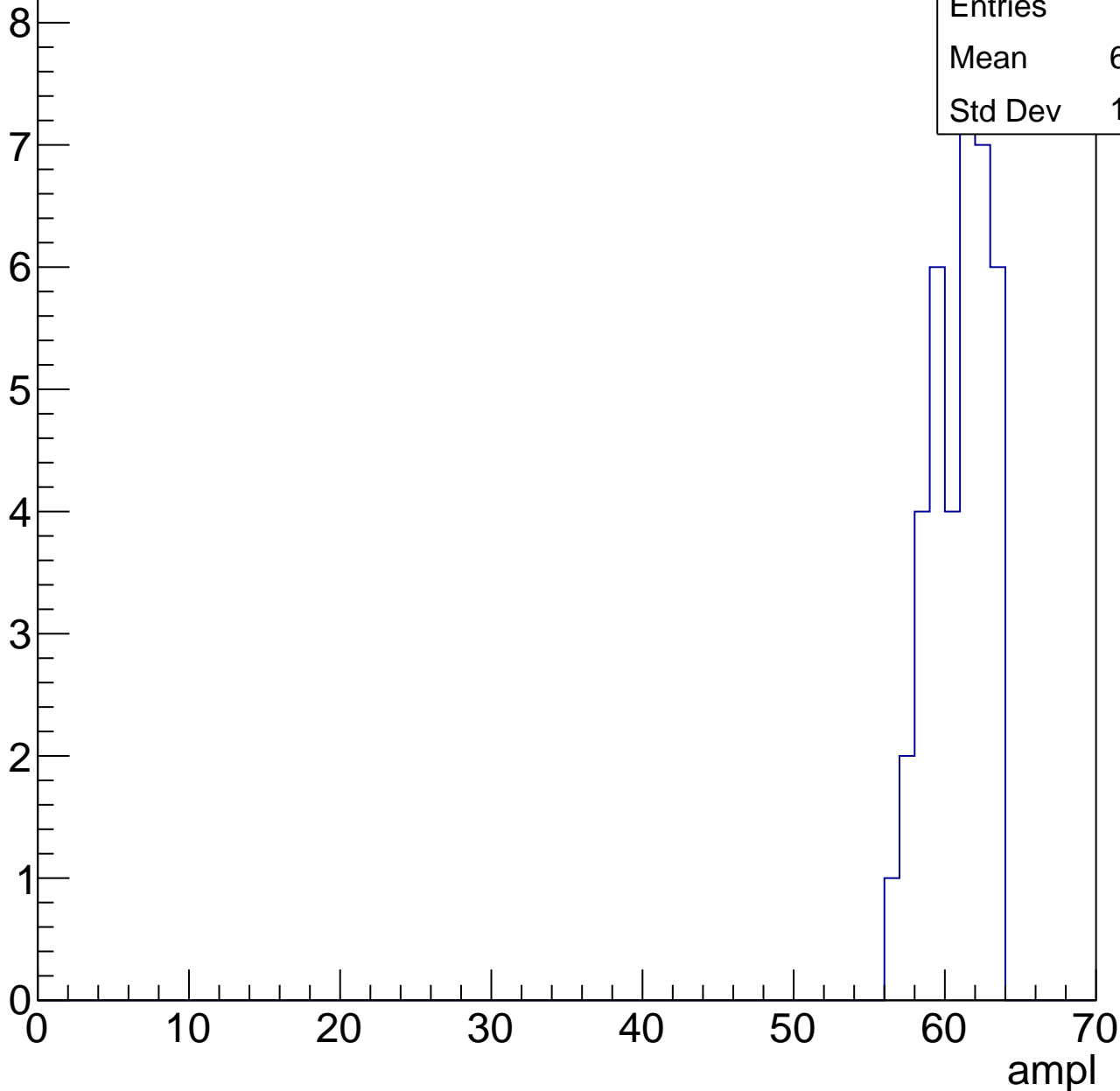


# B1L003S, U6-ch23, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	38
Mean	60.42
Std Dev	1.914



# B1L003S, U6-ch23, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch23, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U6-ch24, adc0

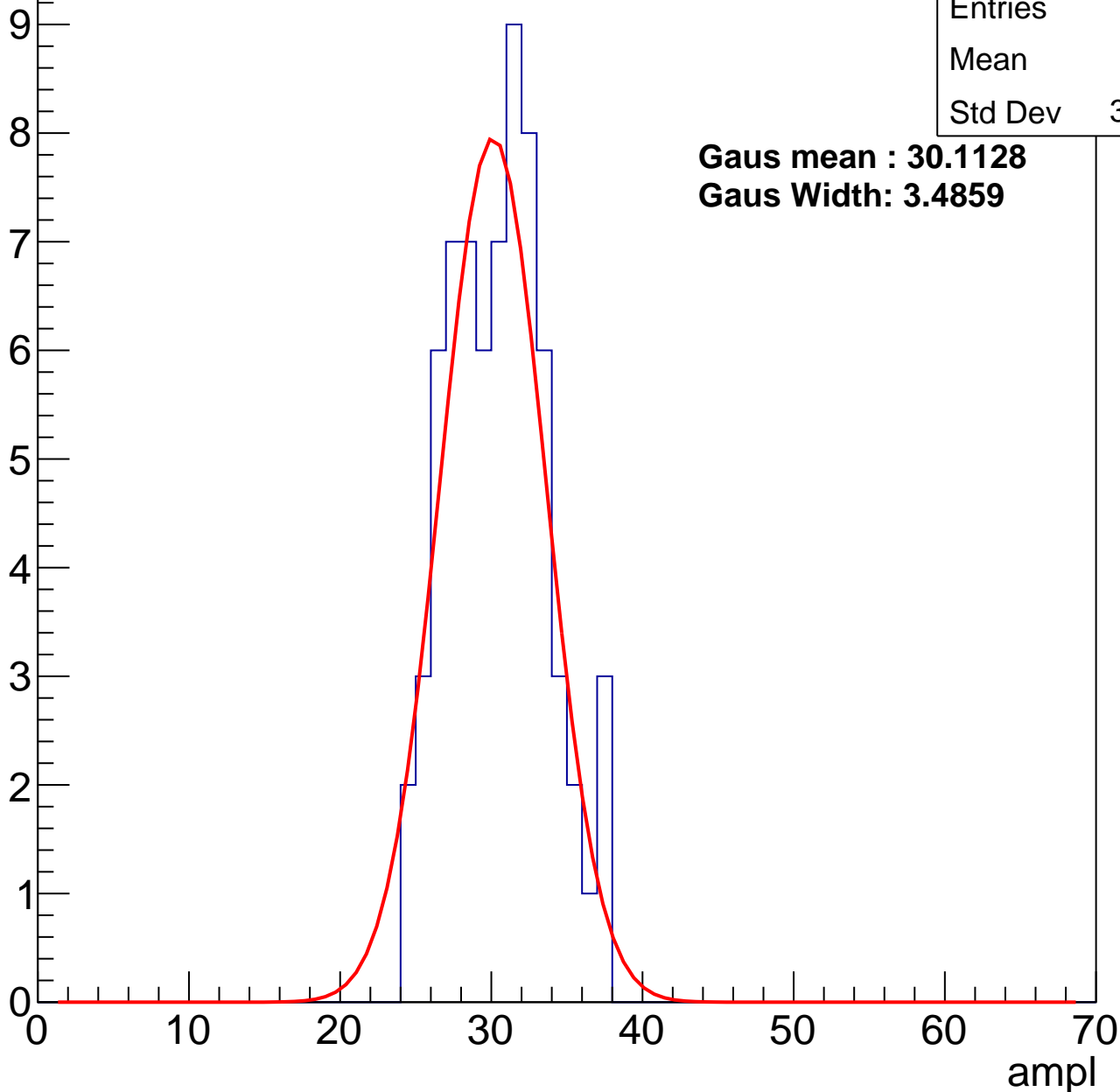
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	30
Std Dev	3.198

**Gaus mean : 30.1128**

**Gaus Width: 3.4859**



# B1L003S, U6-ch24, adc1

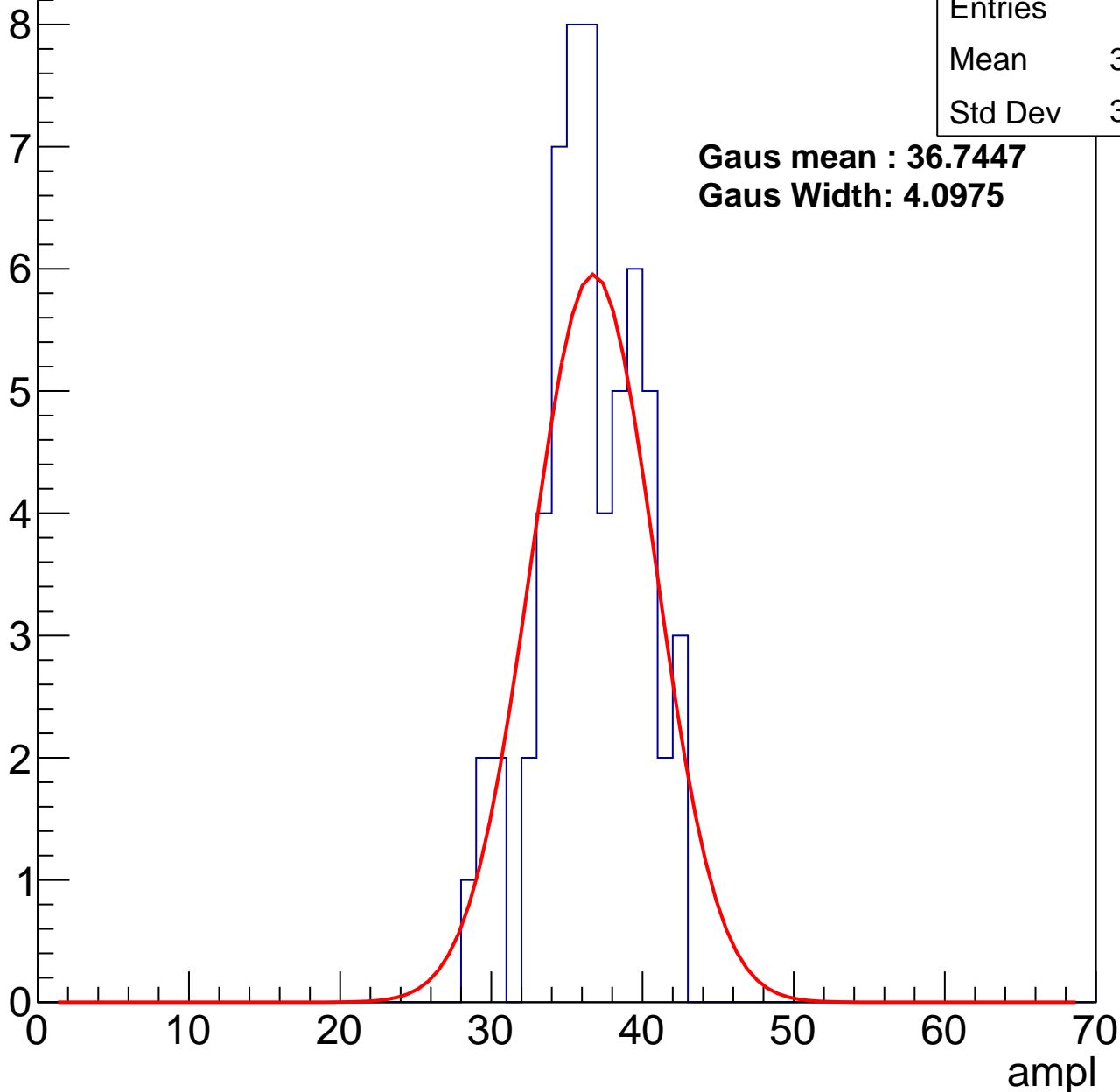
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	36.07
Std Dev	3.329

**Gaus mean : 36.7447**

**Gaus Width: 4.0975**



# B1L003S, U6-ch24, adc2

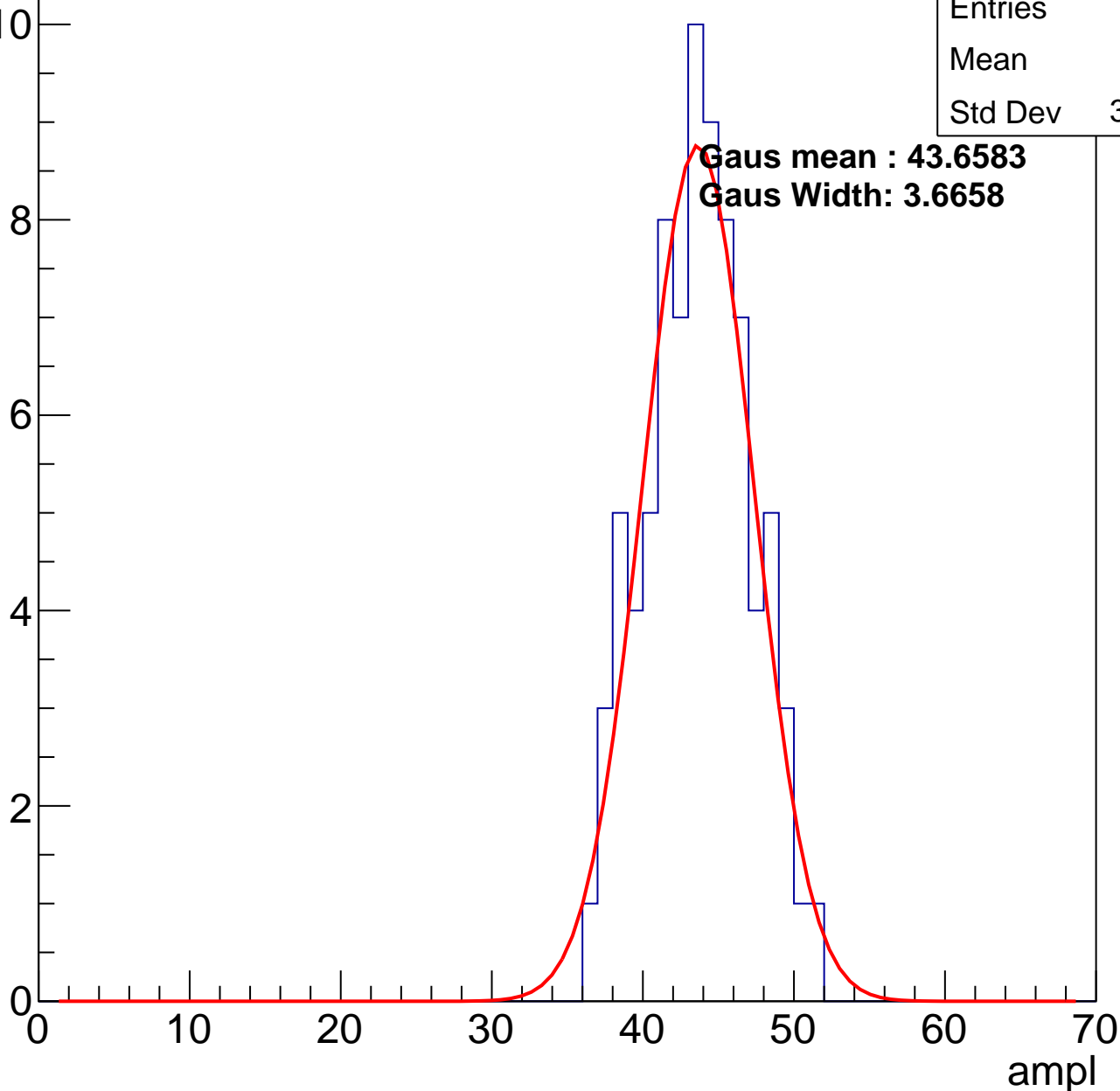
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	81
Mean	43.2
Std Dev	3.408

**Gaus mean : 43.6583**

**Gaus Width: 3.6658**

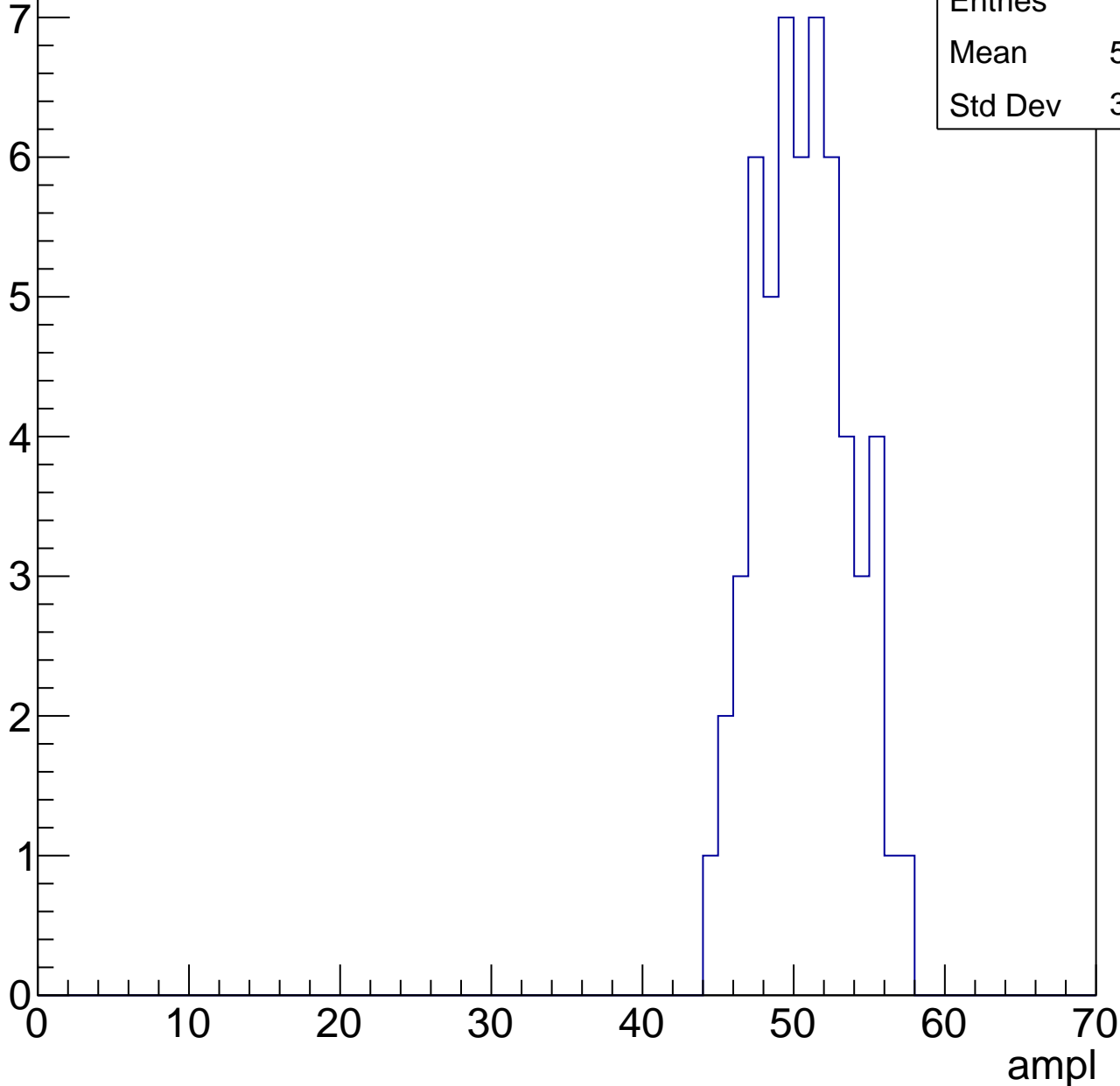


# B1L003S, U6-ch24, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

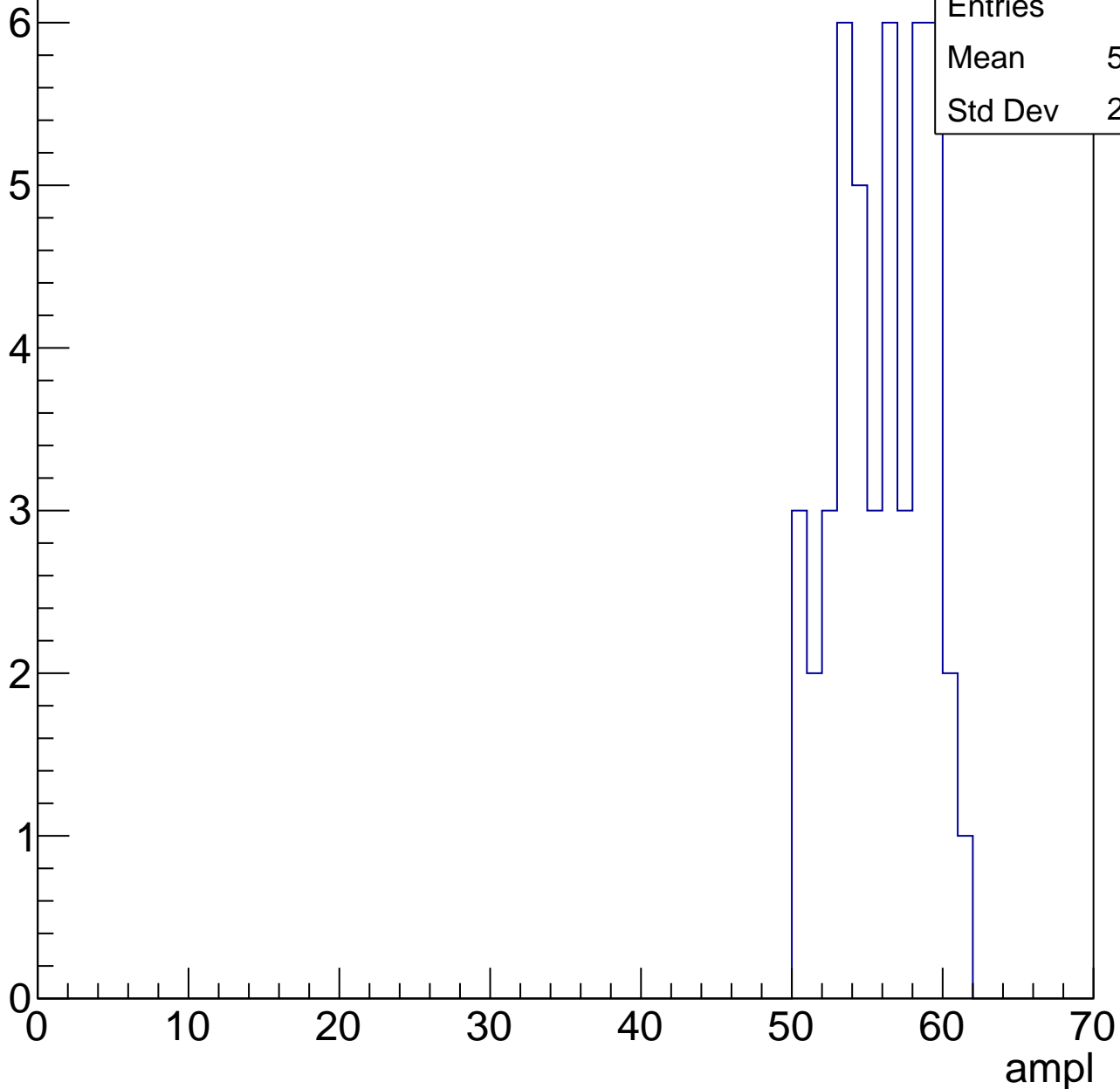
Entries	56
Mean	50.23
Std Dev	3.024



# B1L003S, U6-ch24, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



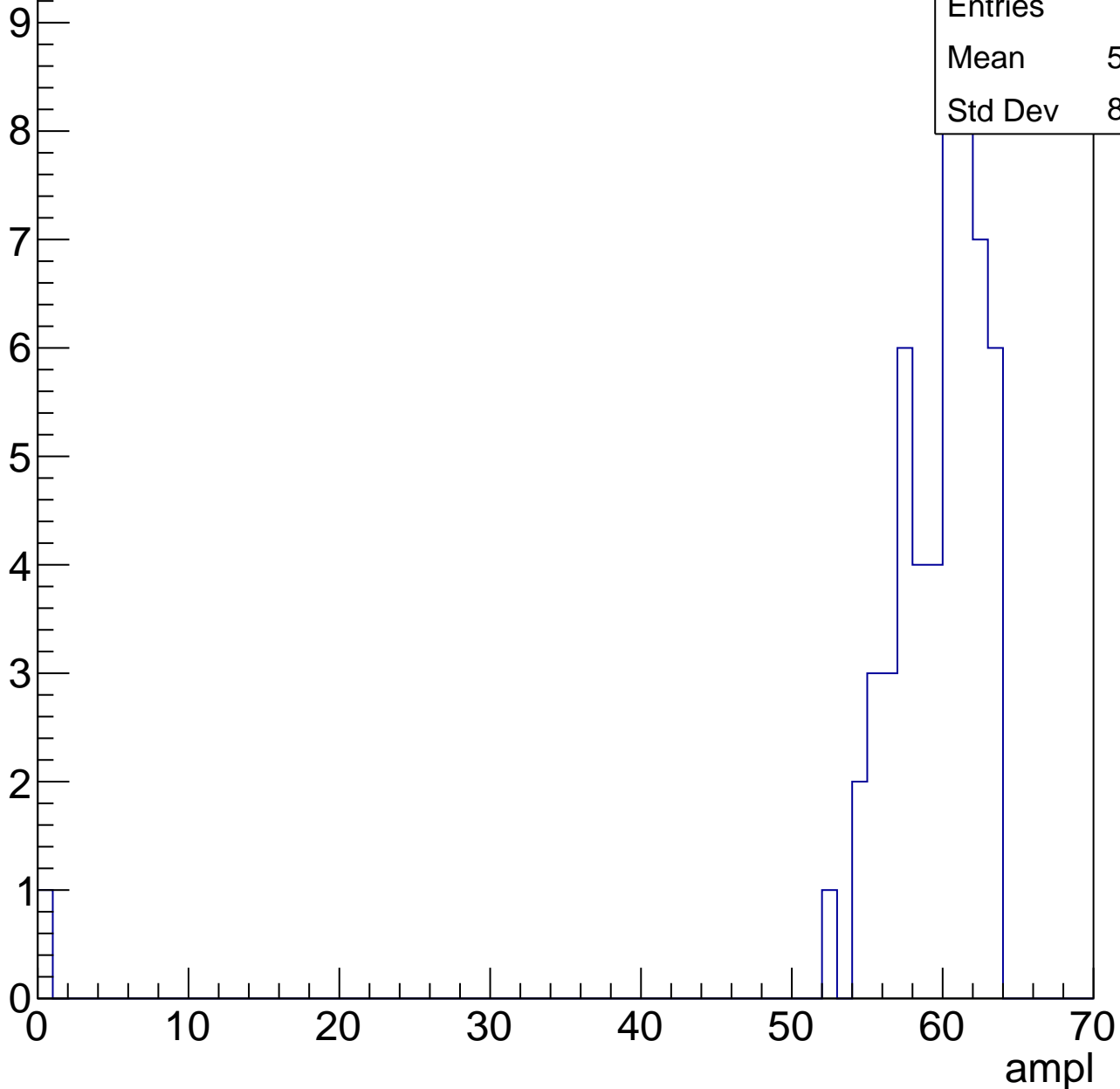
Entries	46
Mean	55.46
Std Dev	2.976

# B1L003S, U6-ch24, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

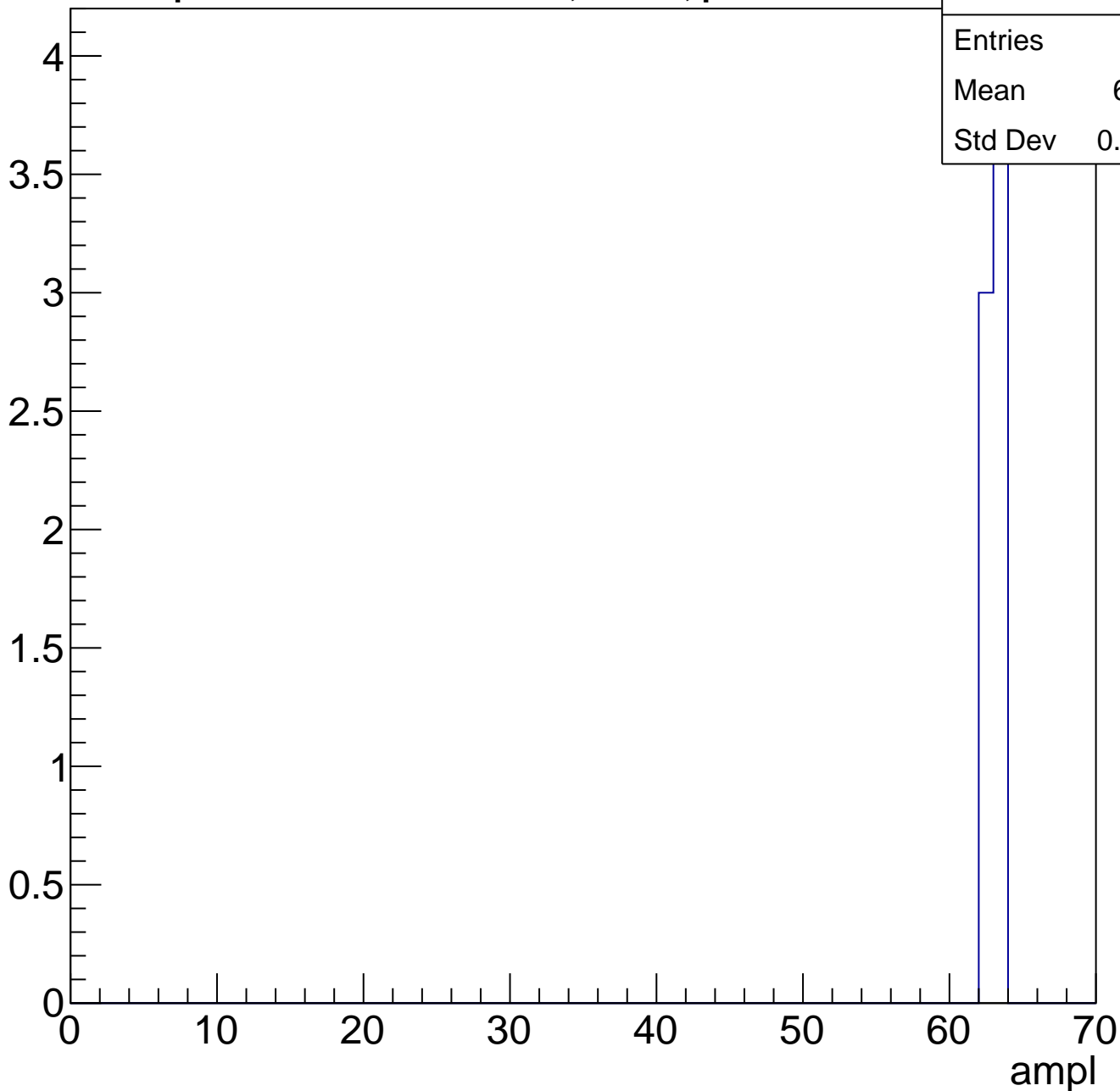
Entries	54
Mean	58.22
Std Dev	8.447



# B1L003S, U6-ch24, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

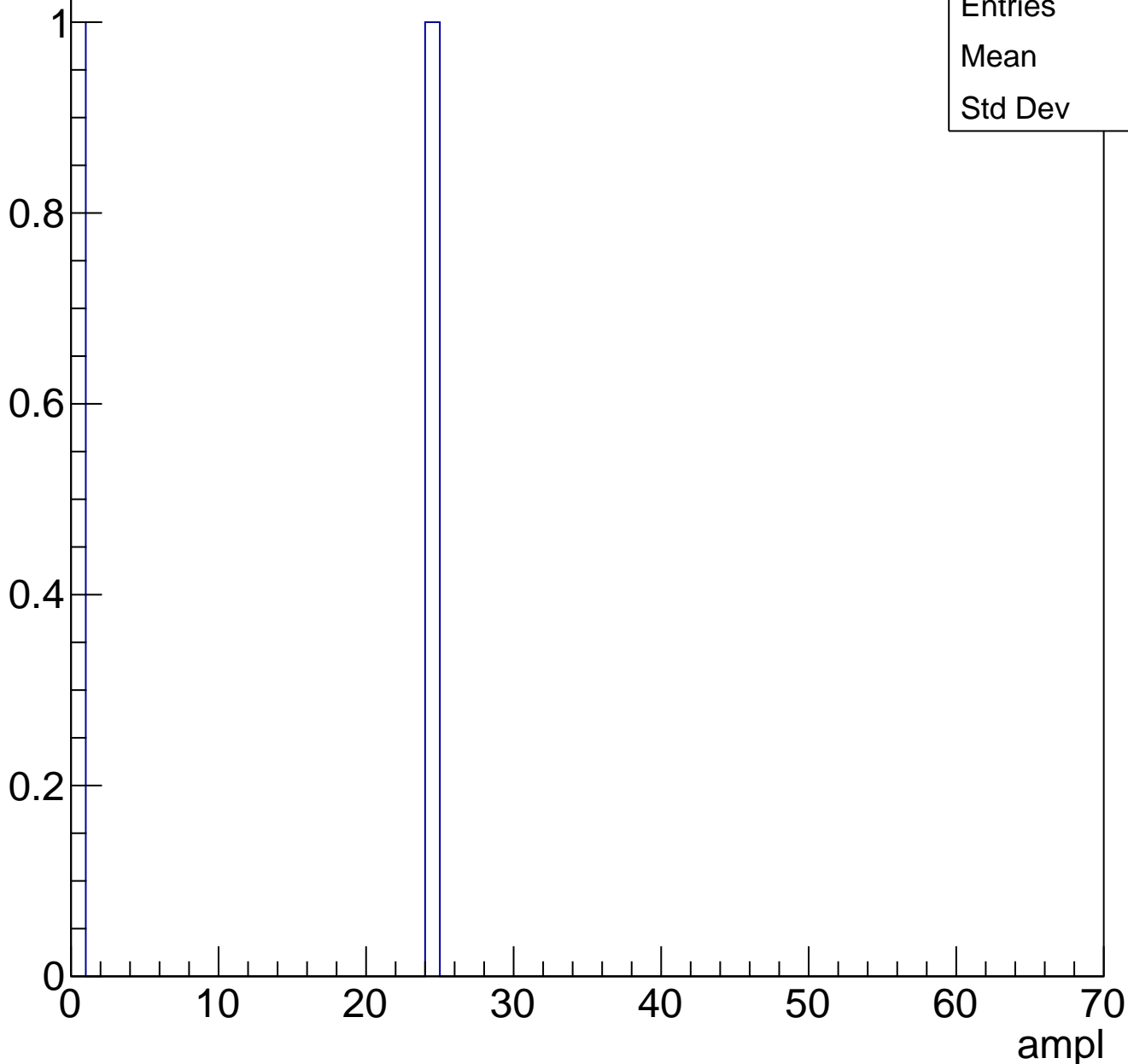




# B1L003S, U6-ch24, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch25, adc0

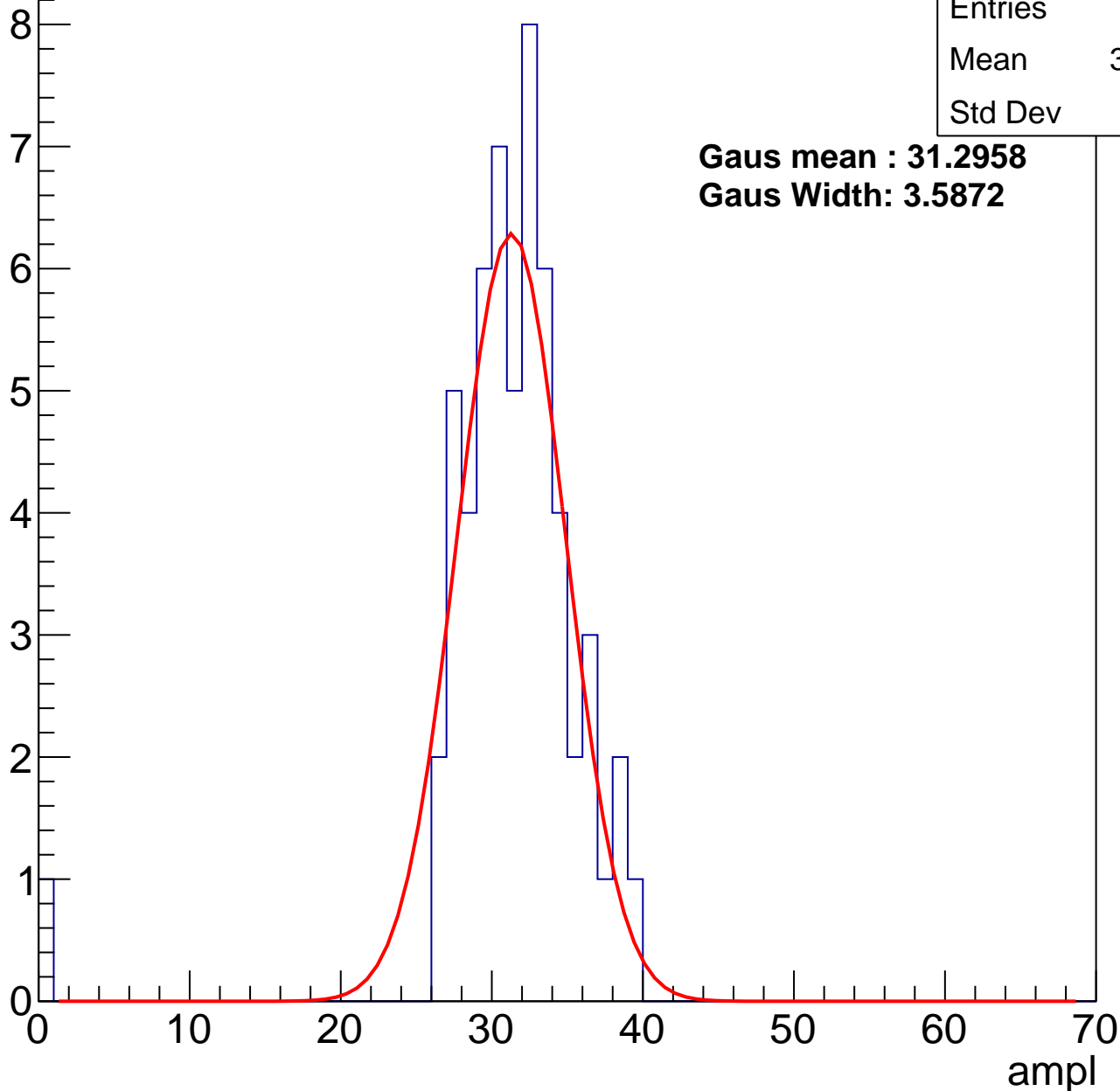
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	30.84
Std Dev	5.18

**Gaus mean : 31.2958**

**Gaus Width: 3.5872**



# B1L003S, U6-ch25, adc1

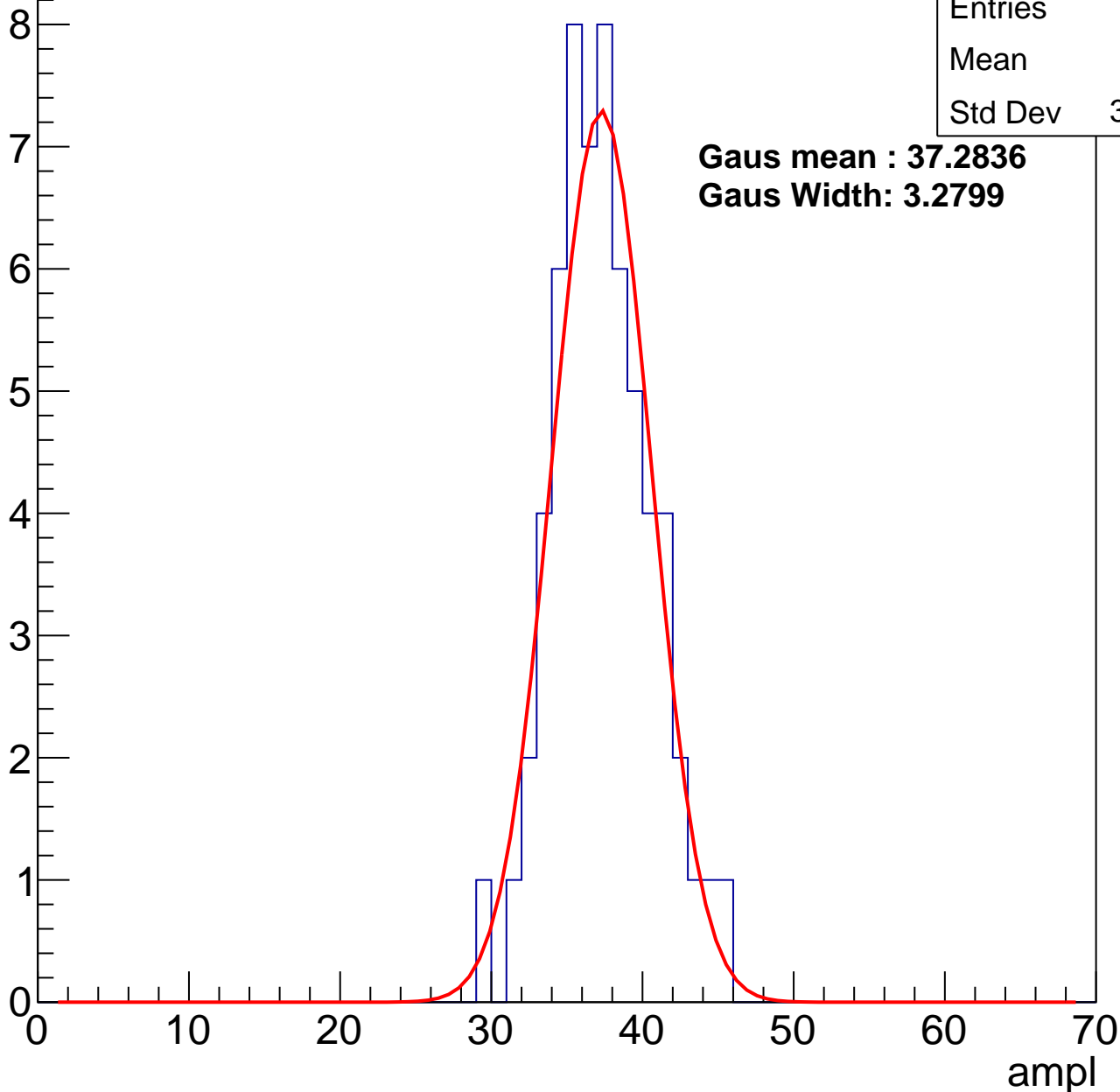
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	36.9
Std Dev	3.217

**Gaus mean : 37.2836**

**Gaus Width: 3.2799**



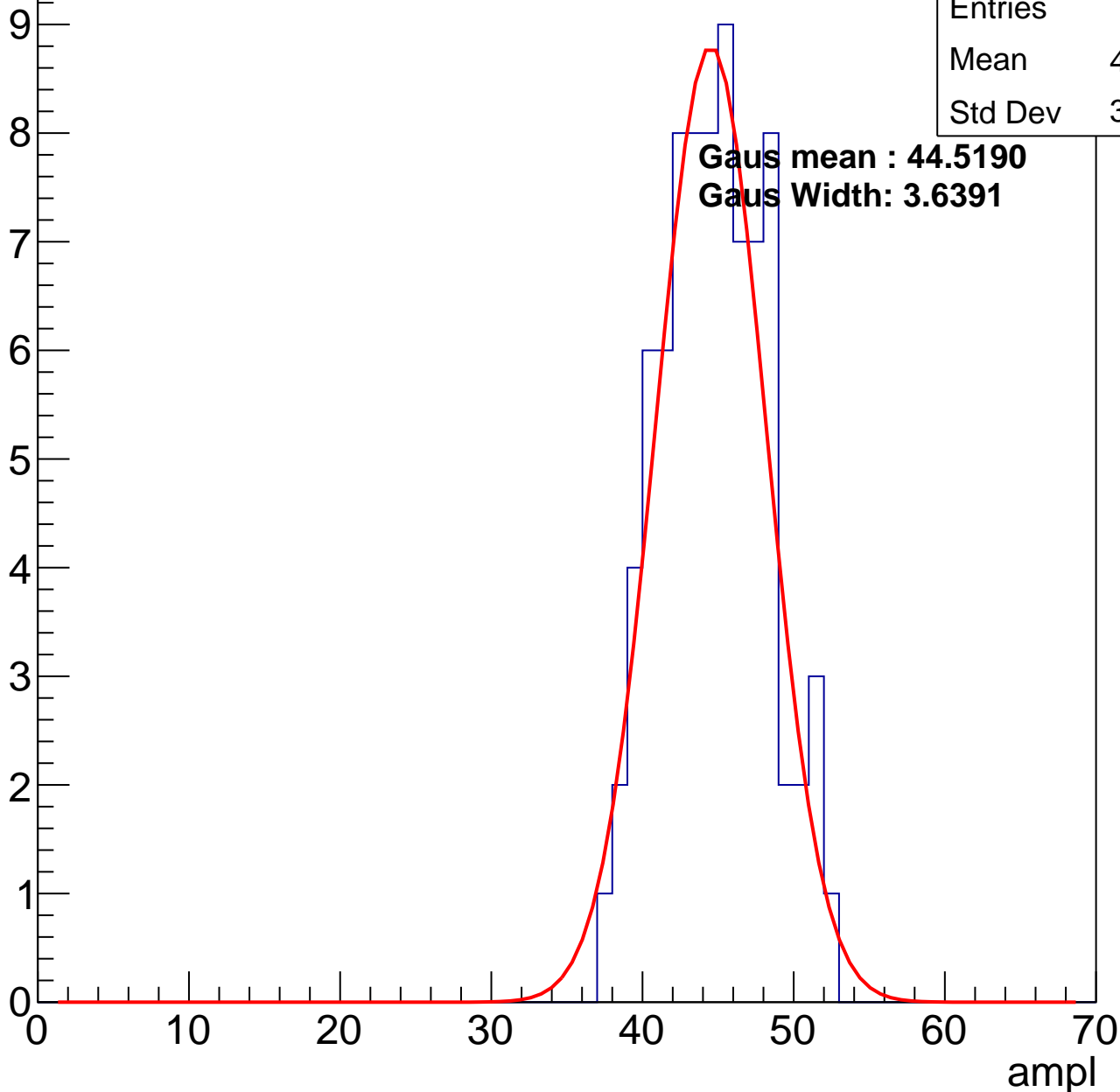
# B1L003S, U6-ch25, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

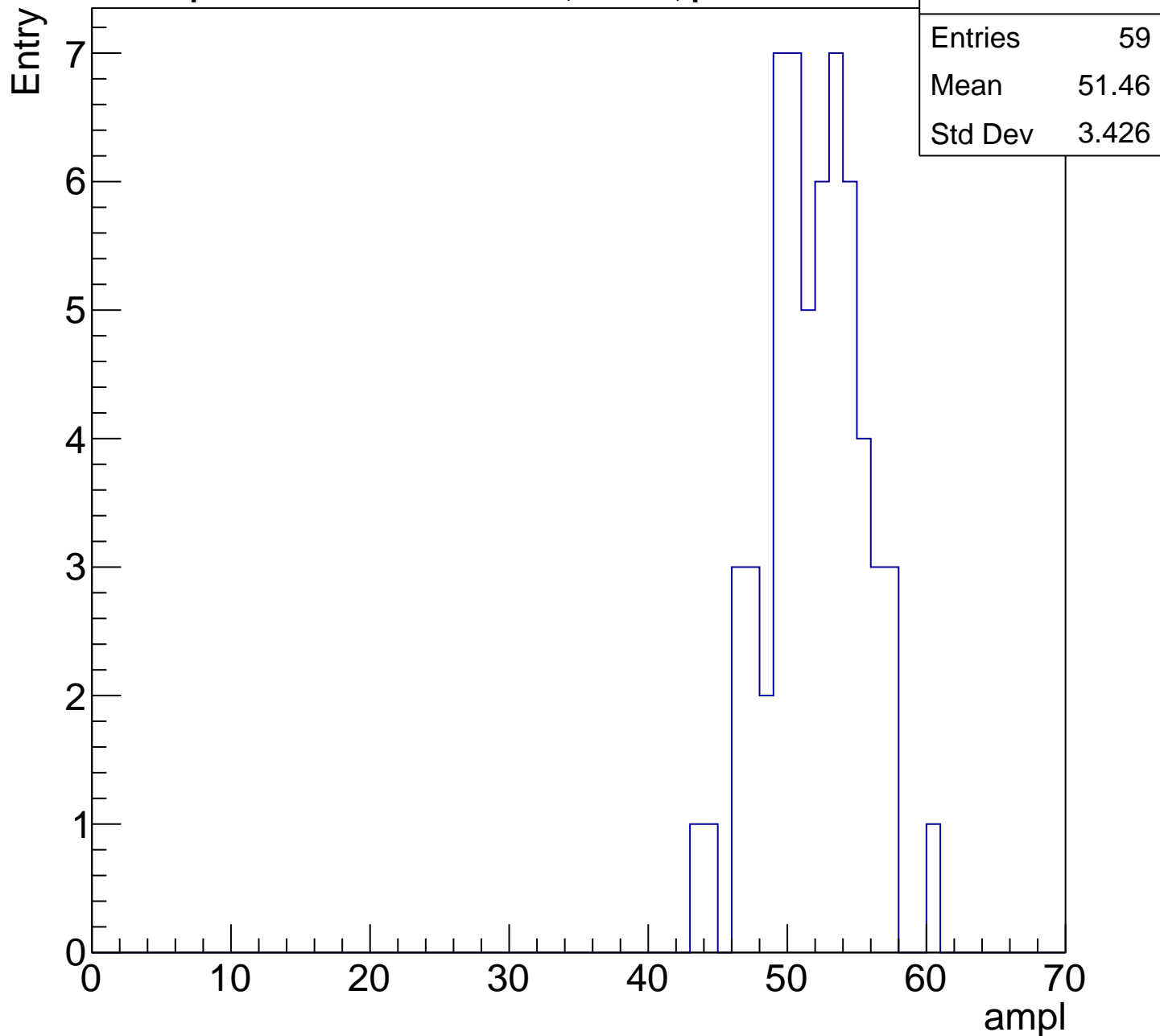
Entries	82
Mean	44.27
Std Dev	3.432

**Gaus mean : 44.5190**  
**Gaus Width: 3.6391**



# B1L003S, U6-ch25, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

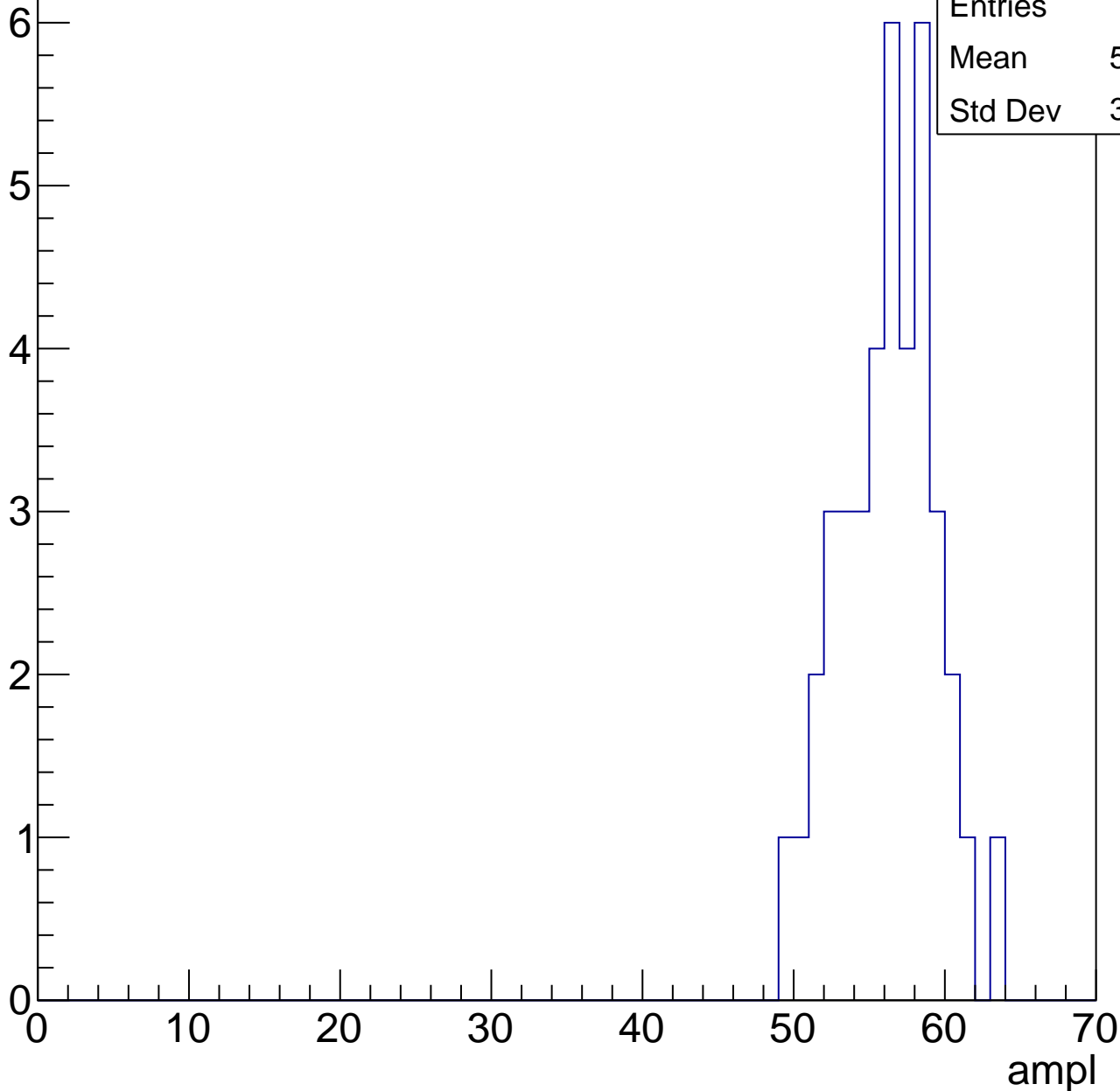


# B1L003S, U6-ch25, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	40
Mean	55.77
Std Dev	3.102

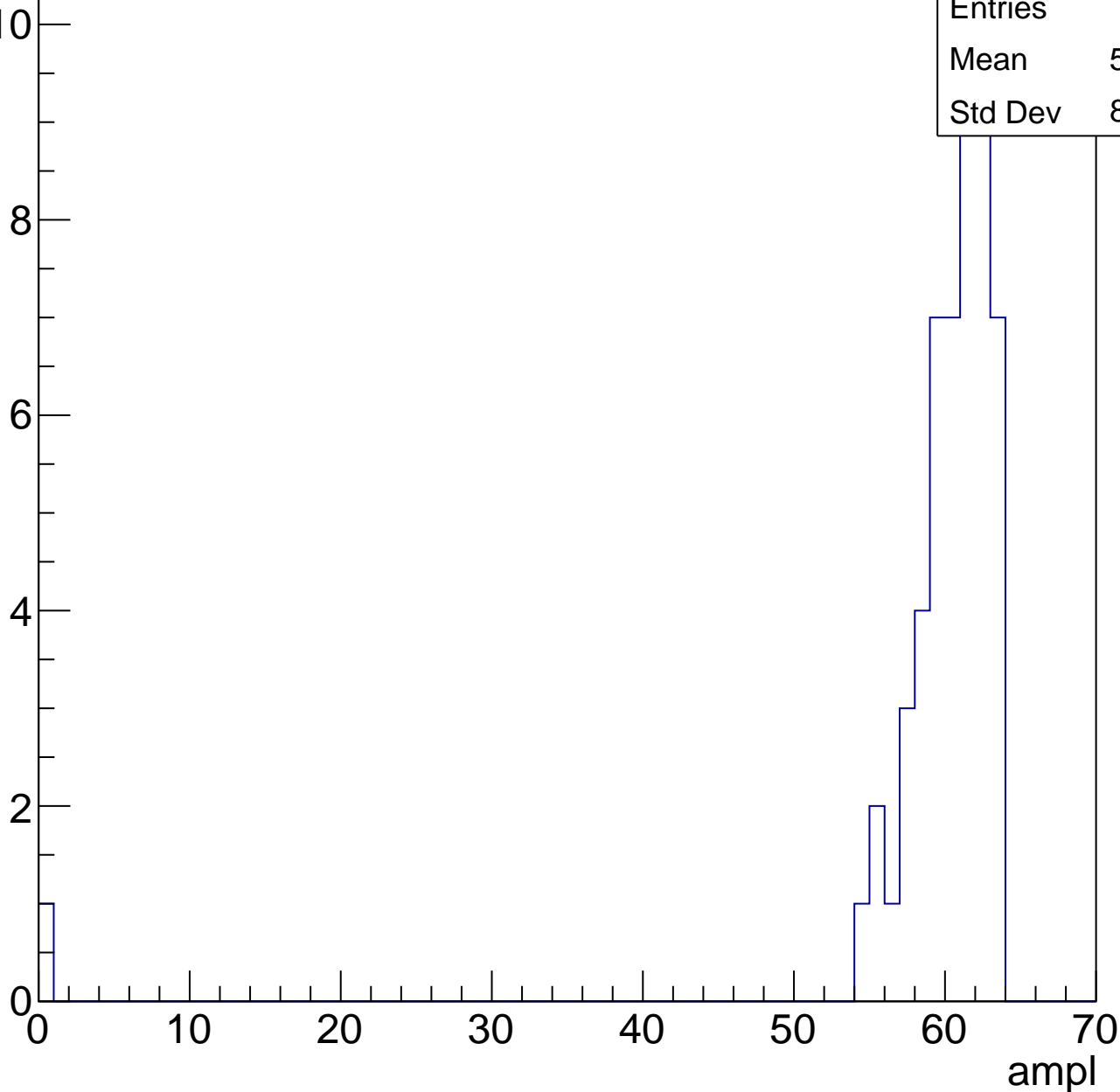


# B1L003S, U6-ch25, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	52
Mean	58.96
Std Dev	8.557



# B1L003S, U6-ch25, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch25, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U6-ch26, adc0

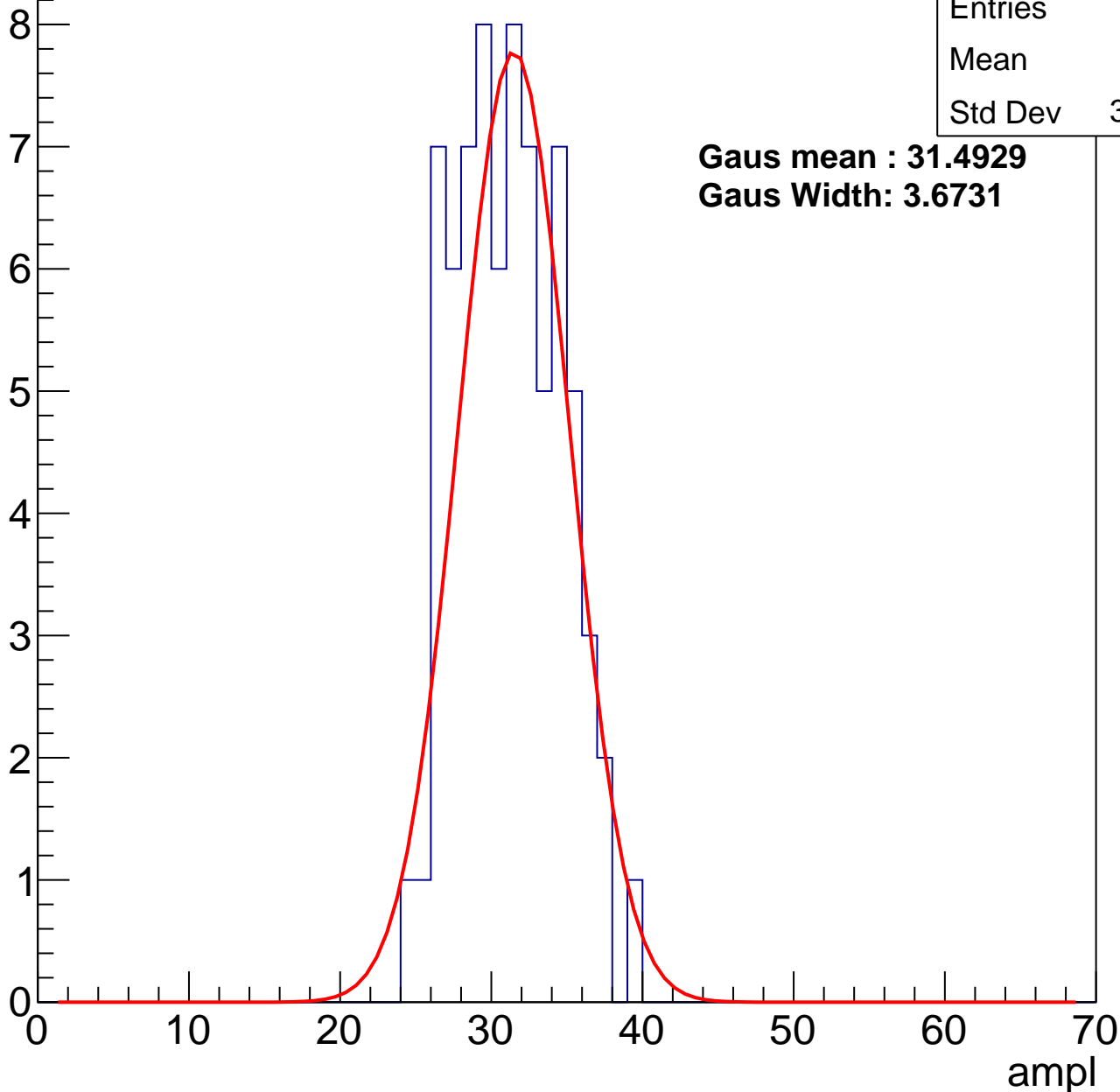
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	74
Mean	30.7
Std Dev	3.352

**Gaus mean : 31.4929**

**Gaus Width: 3.6731**



# B1L003S, U6-ch26, adc1

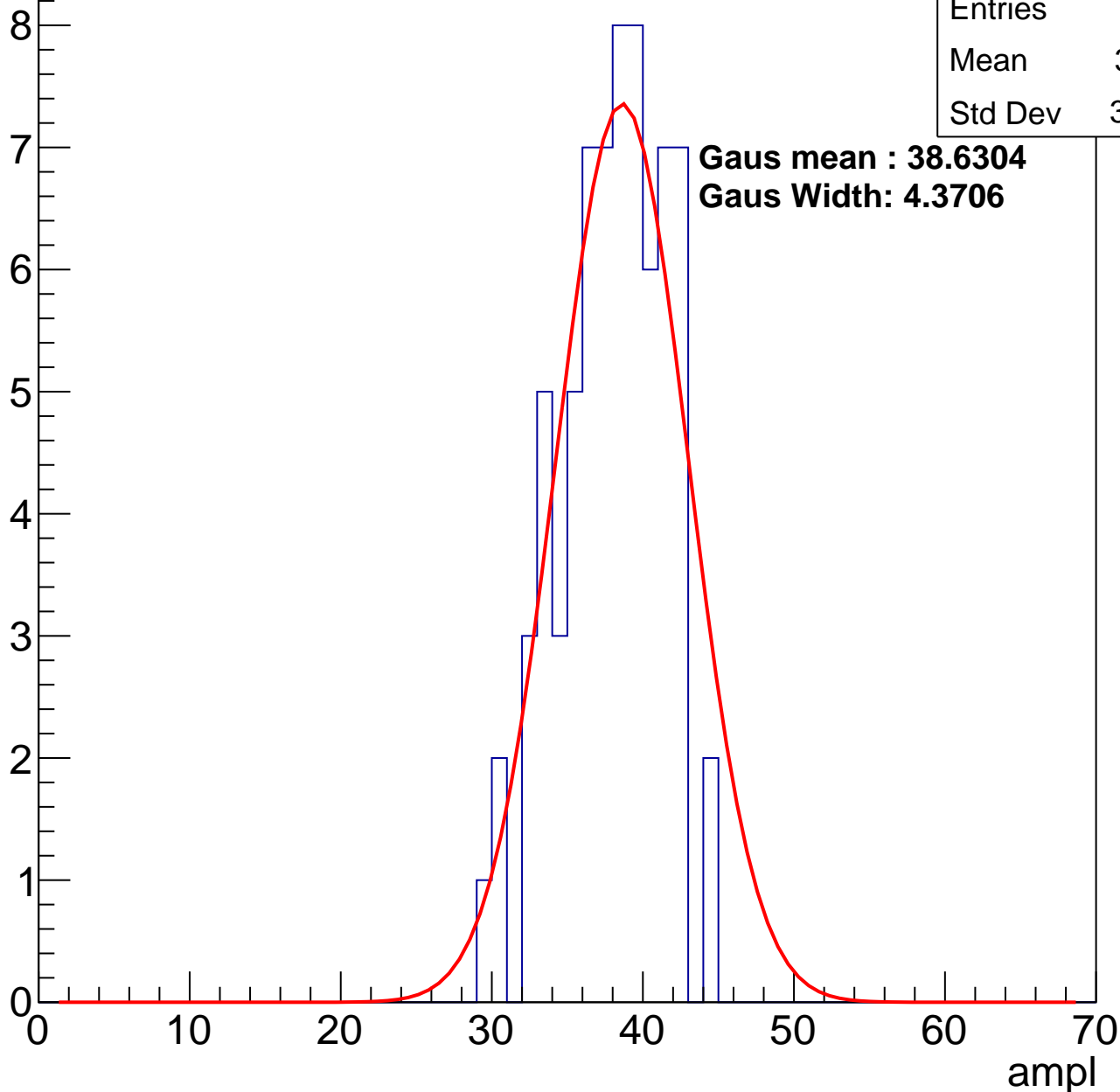
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	71
Mean	37.51
Std Dev	3.423

**Gaus mean : 38.6304**

**Gaus Width: 4.3706**



# B1L003S, U6-ch26, adc2

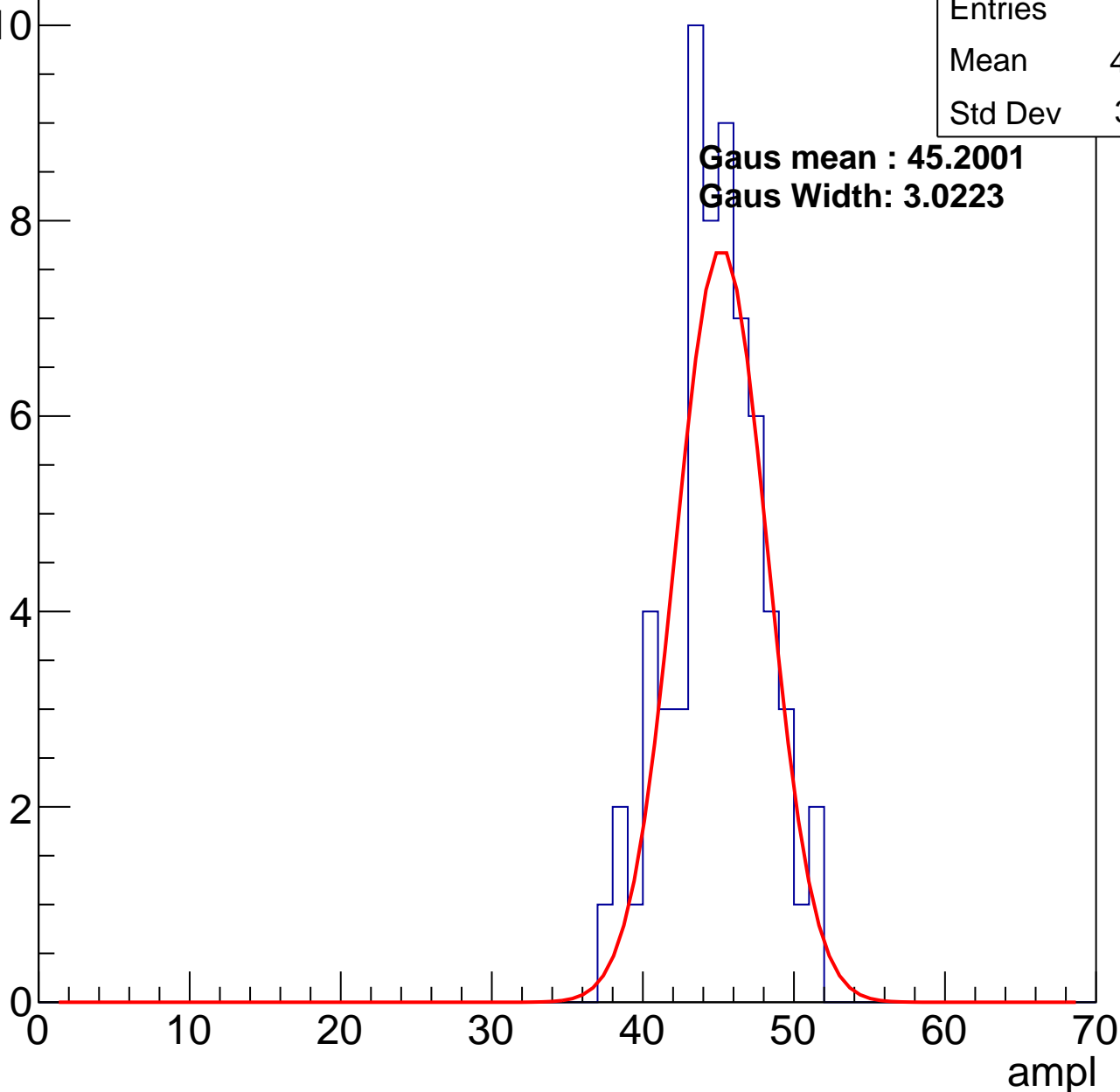
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	44.42
Std Dev	3.091

**Gaus mean : 45.2001**

**Gaus Width: 3.0223**

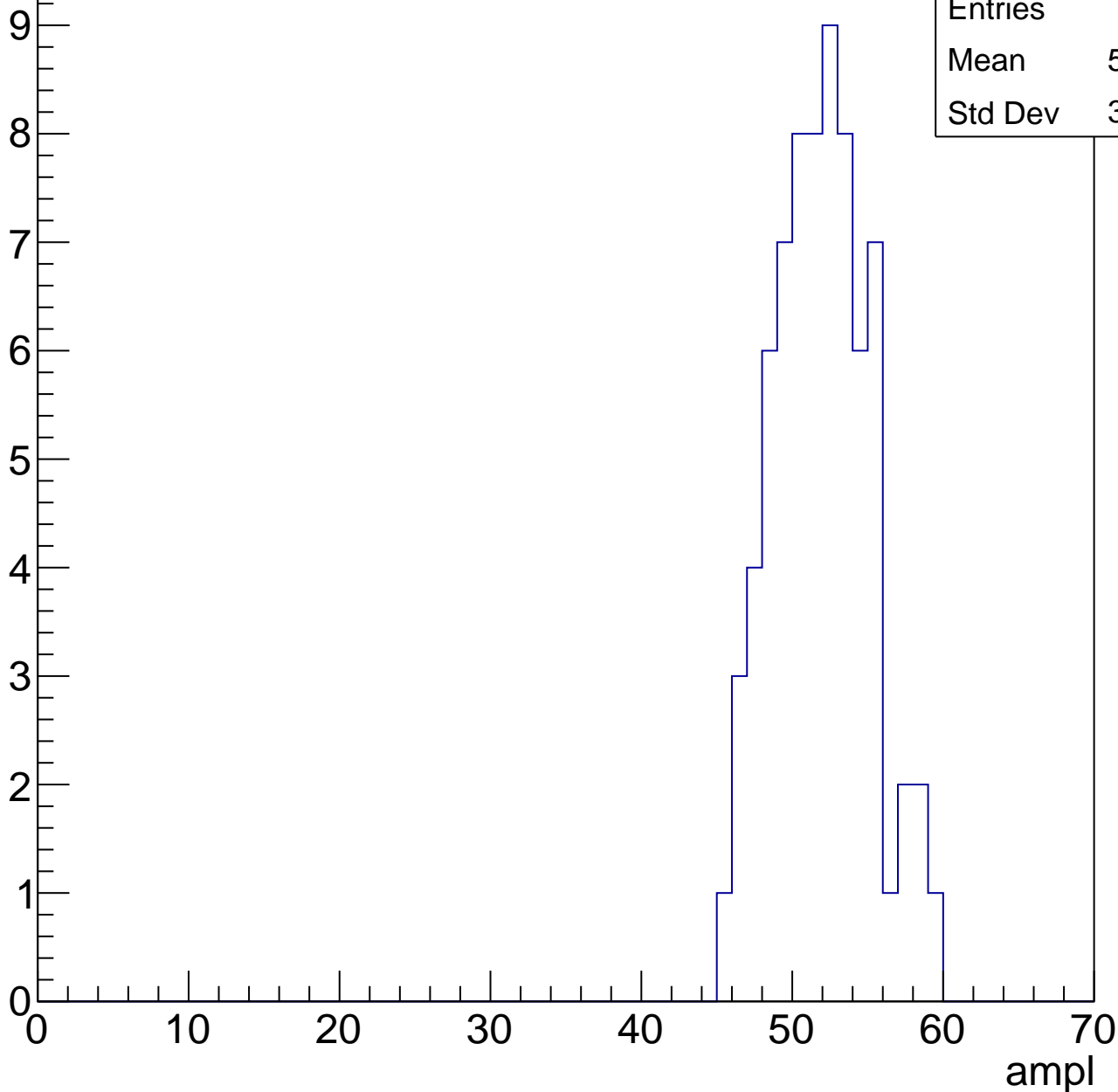


# B1L003S, U6-ch26, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	73
Mean	51.45
Std Dev	3.132

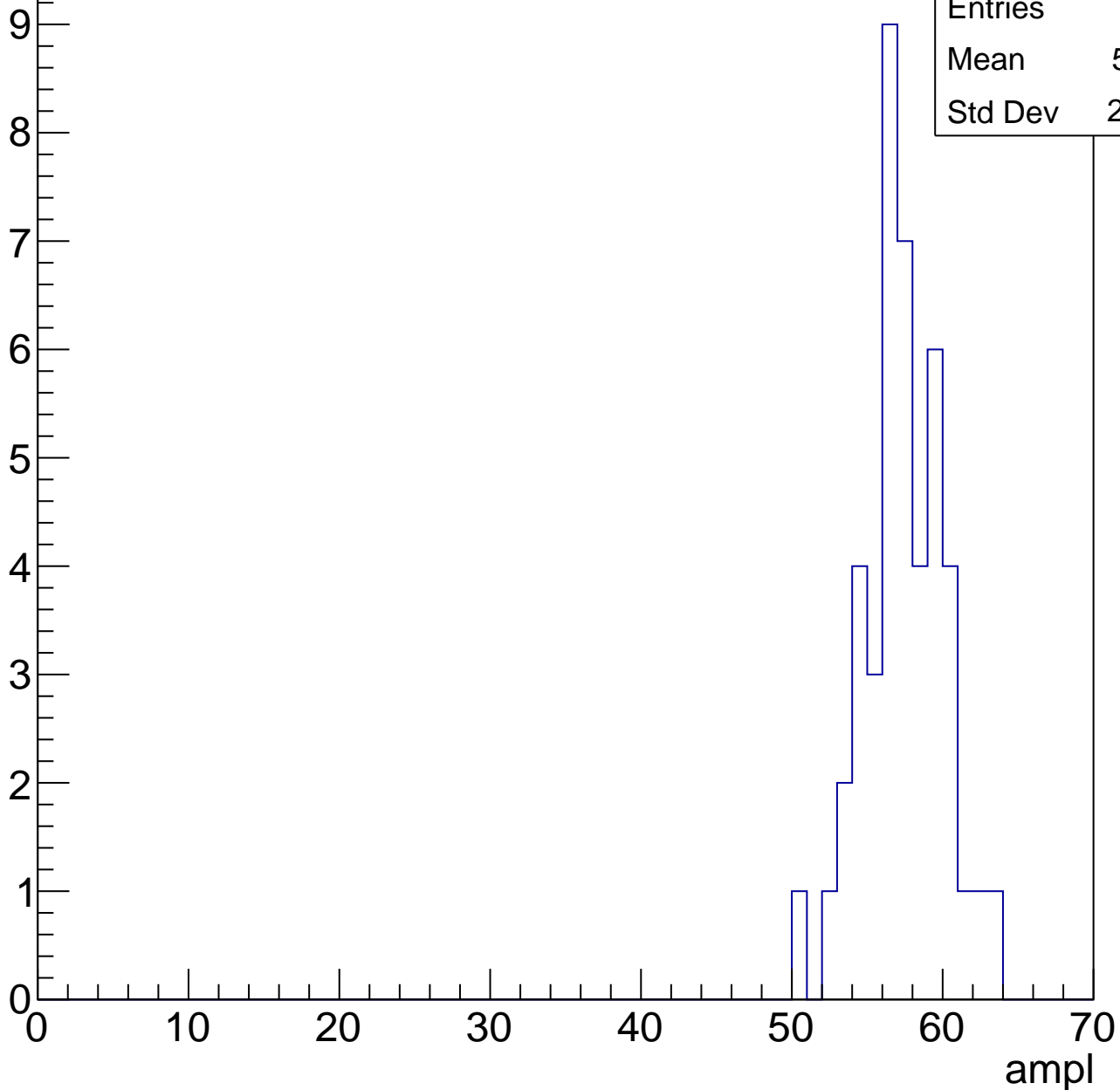


# B1L003S, U6-ch26, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	44
Mean	56.91
Std Dev	2.627

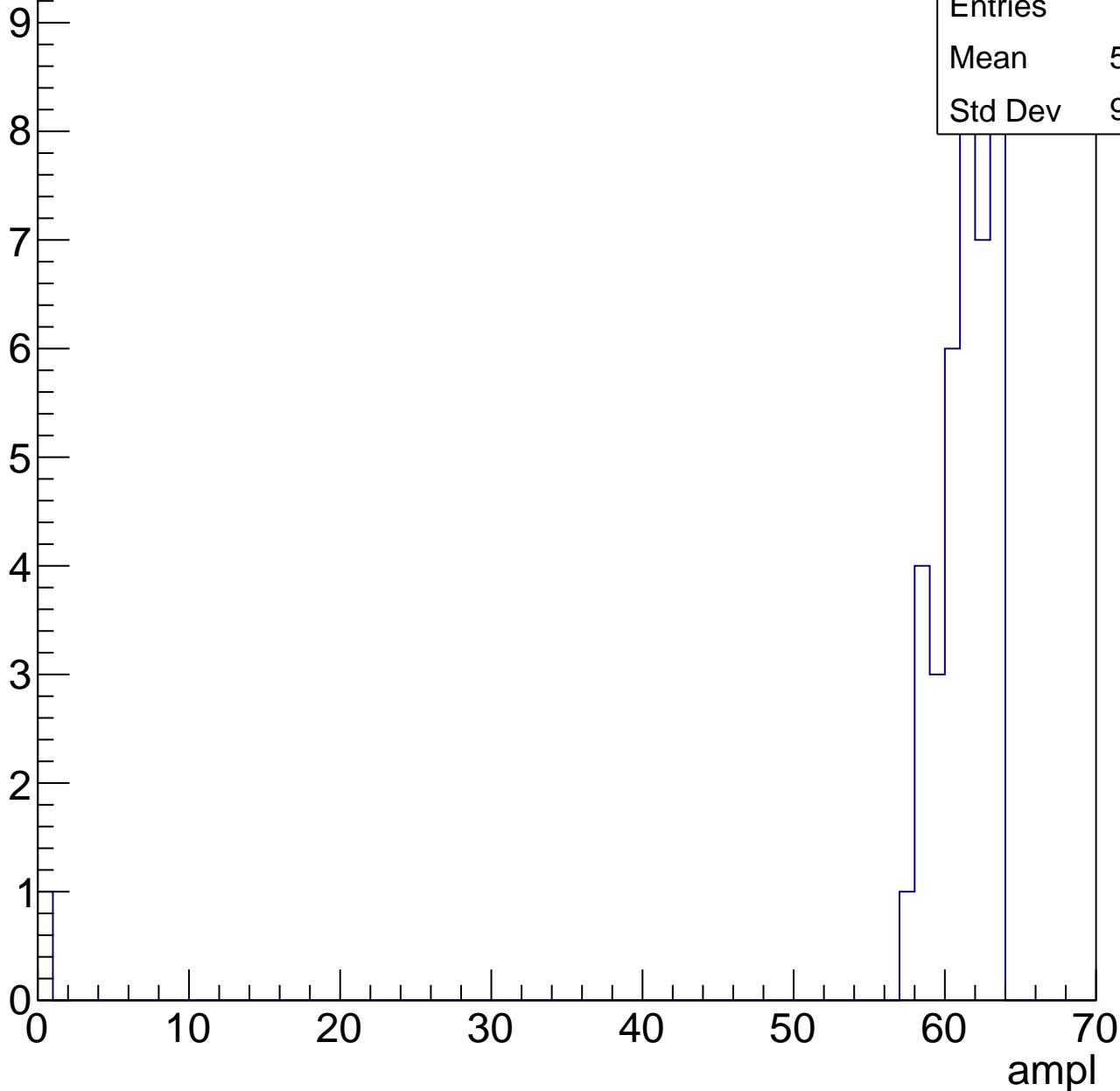


# B1L003S, U6-ch26, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

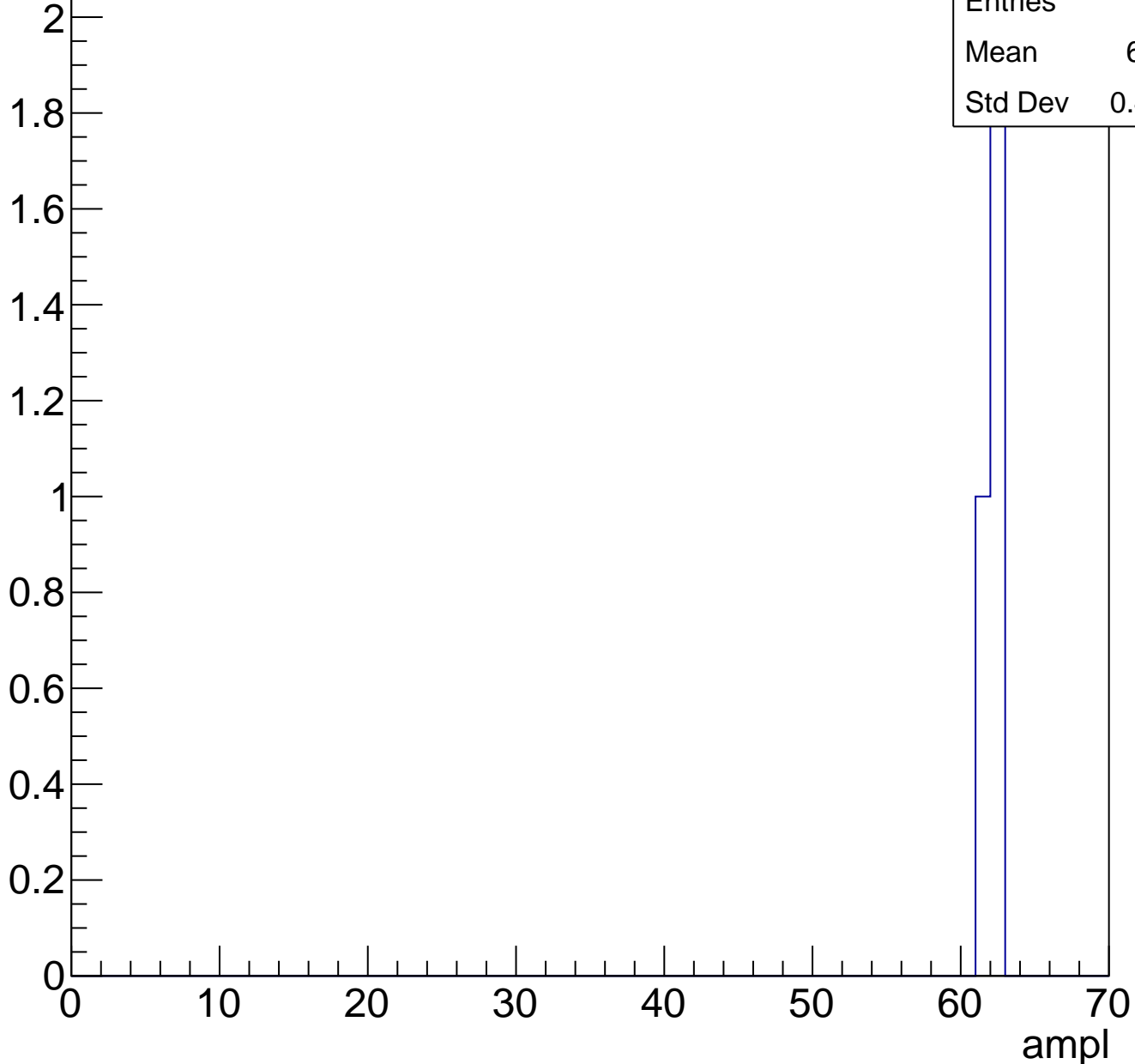
Entries	39
Mean	59.36
Std Dev	9.778



# B1L003S, U6-ch26, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch26, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch27, adc0

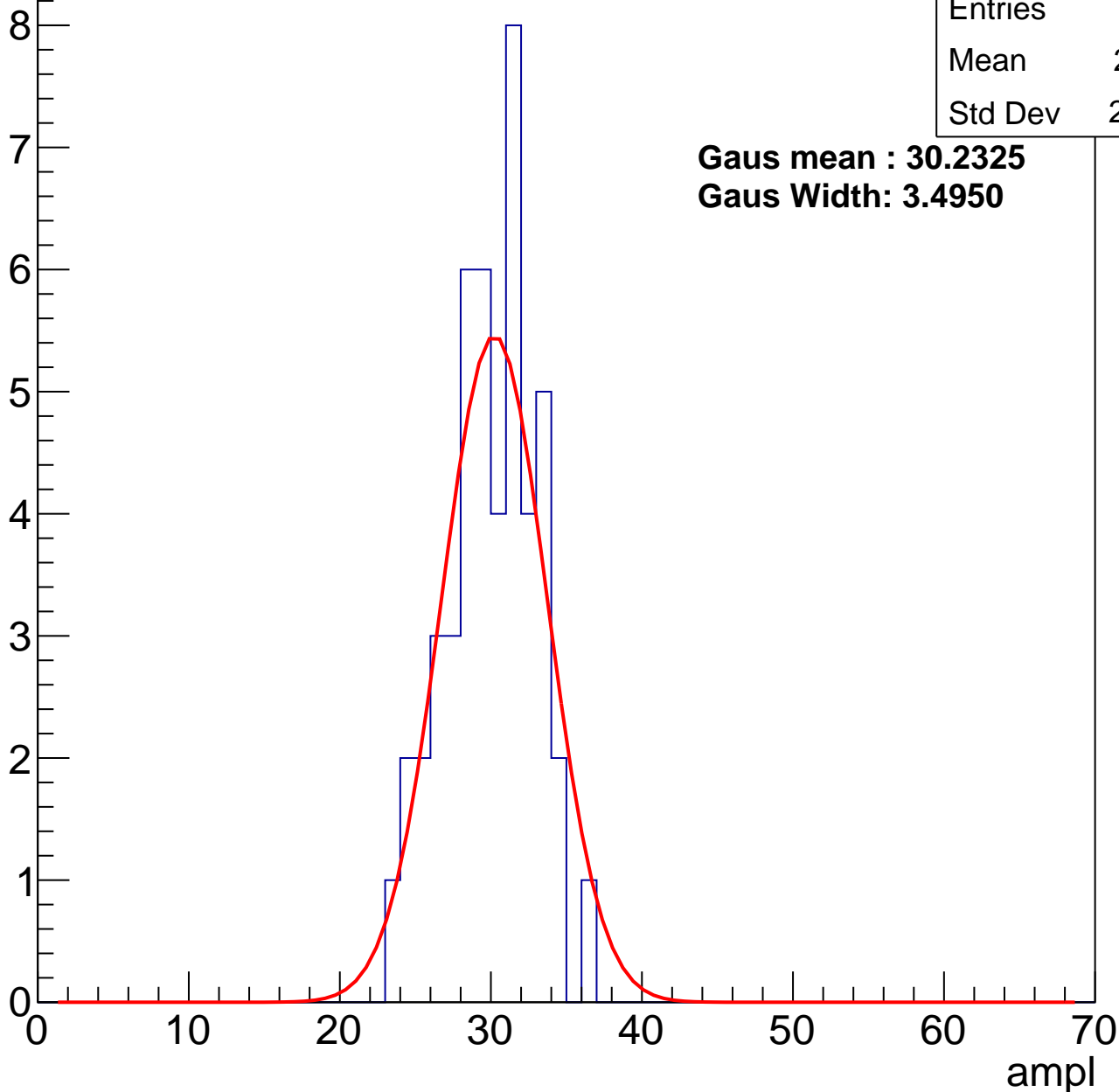
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	47
Mean	29.51
Std Dev	2.924

**Gaus mean : 30.2325**

**Gaus Width: 3.4950**



# B1L003S, U6-ch27, adc1

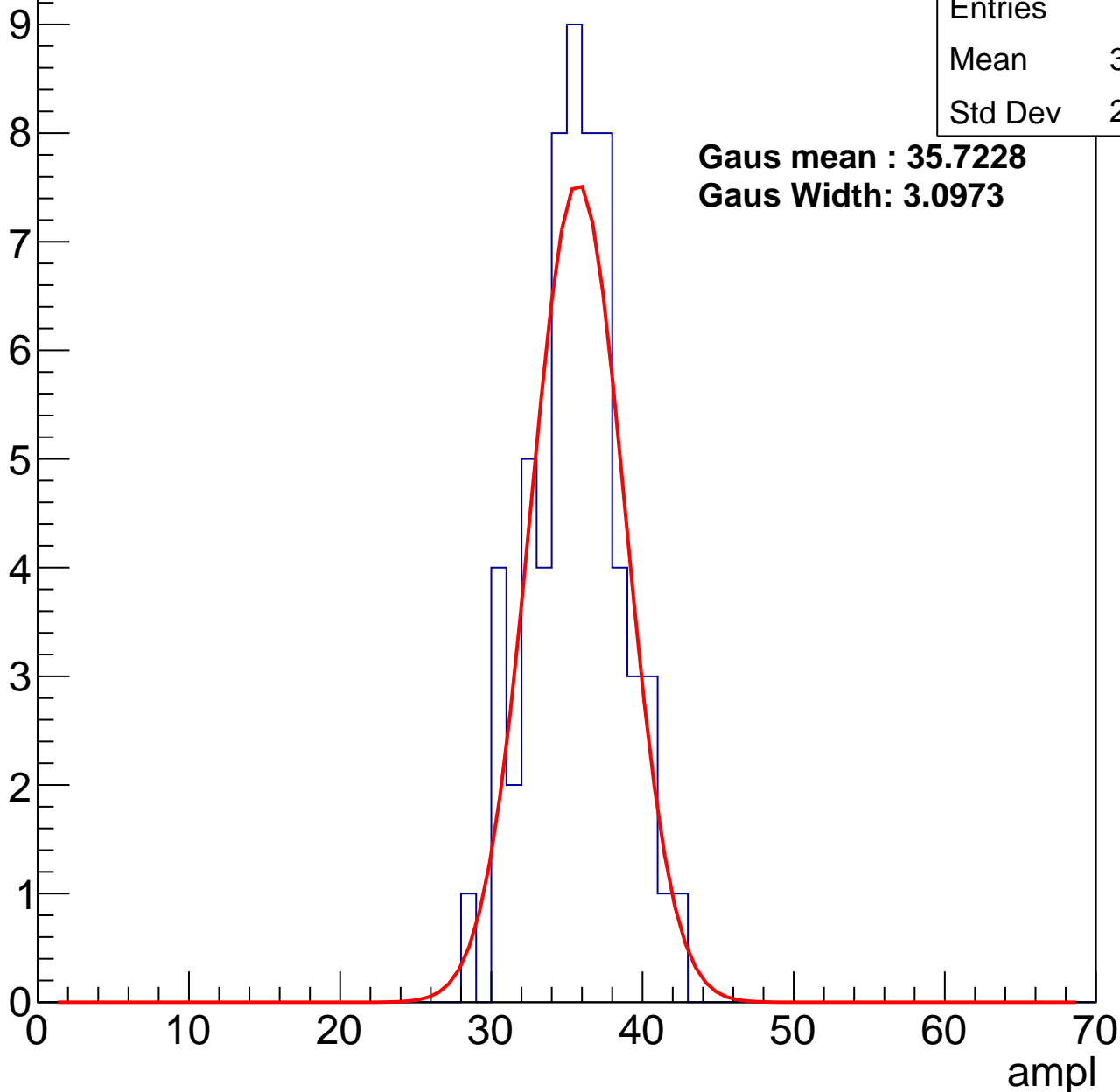
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	35.16
Std Dev	2.954

**Gaus mean : 35.7228**

**Gaus Width: 3.0973**



# B1L003S, U6-ch27, adc2

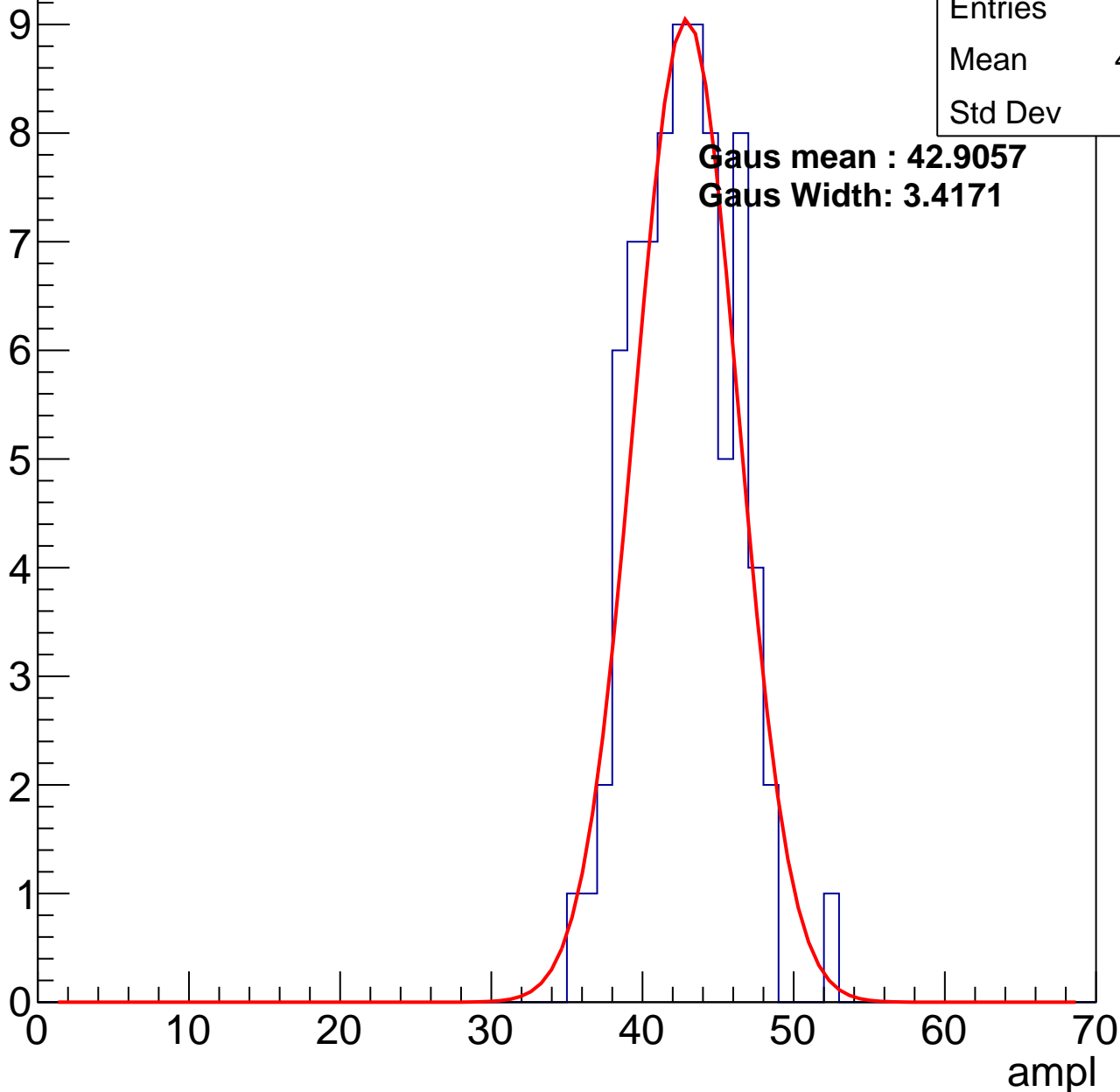
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	78
Mean	42.31
Std Dev	3.22

**Gaus mean : 42.9057**

**Gaus Width: 3.4171**

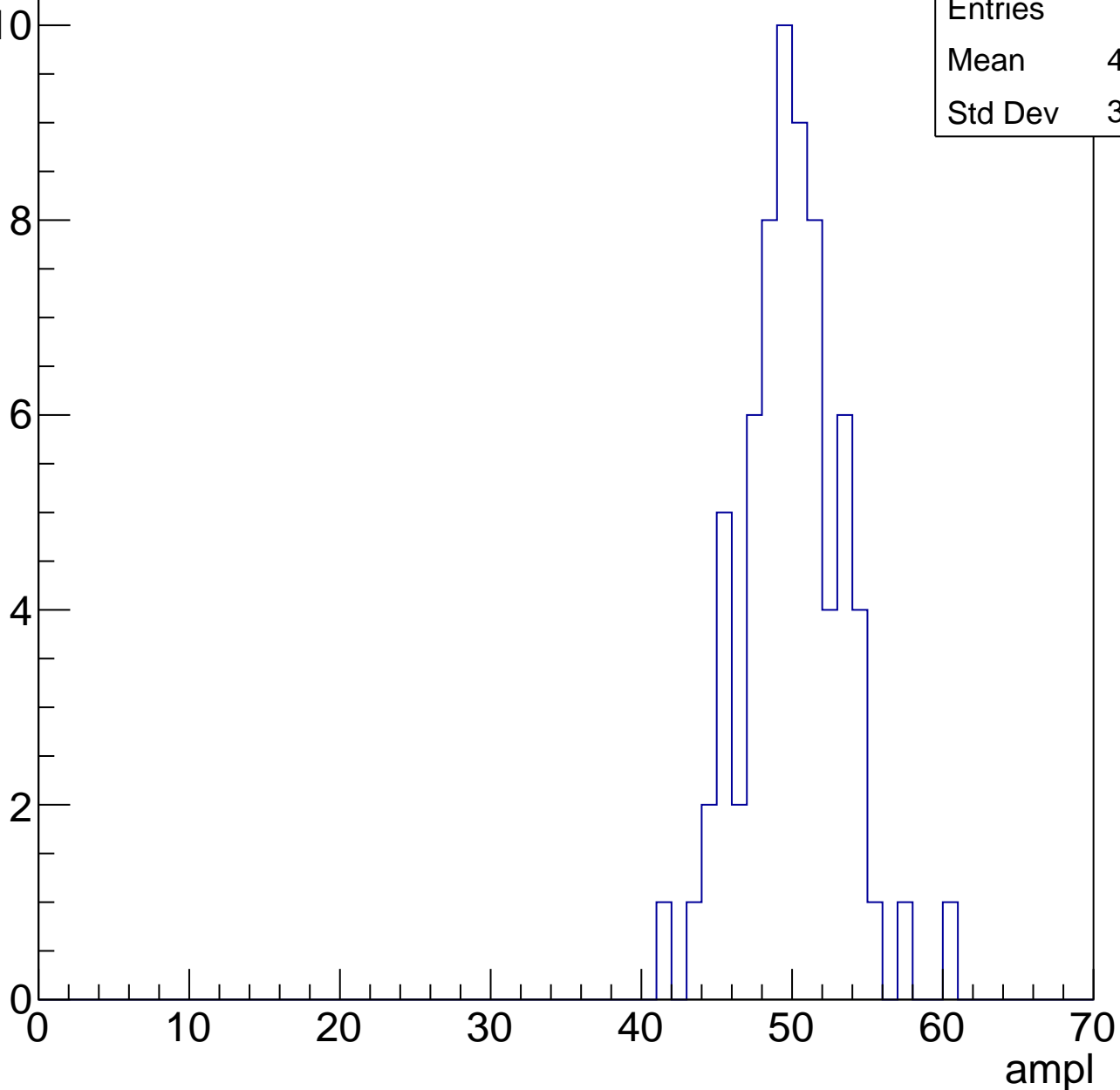


# B1L003S, U6-ch27, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

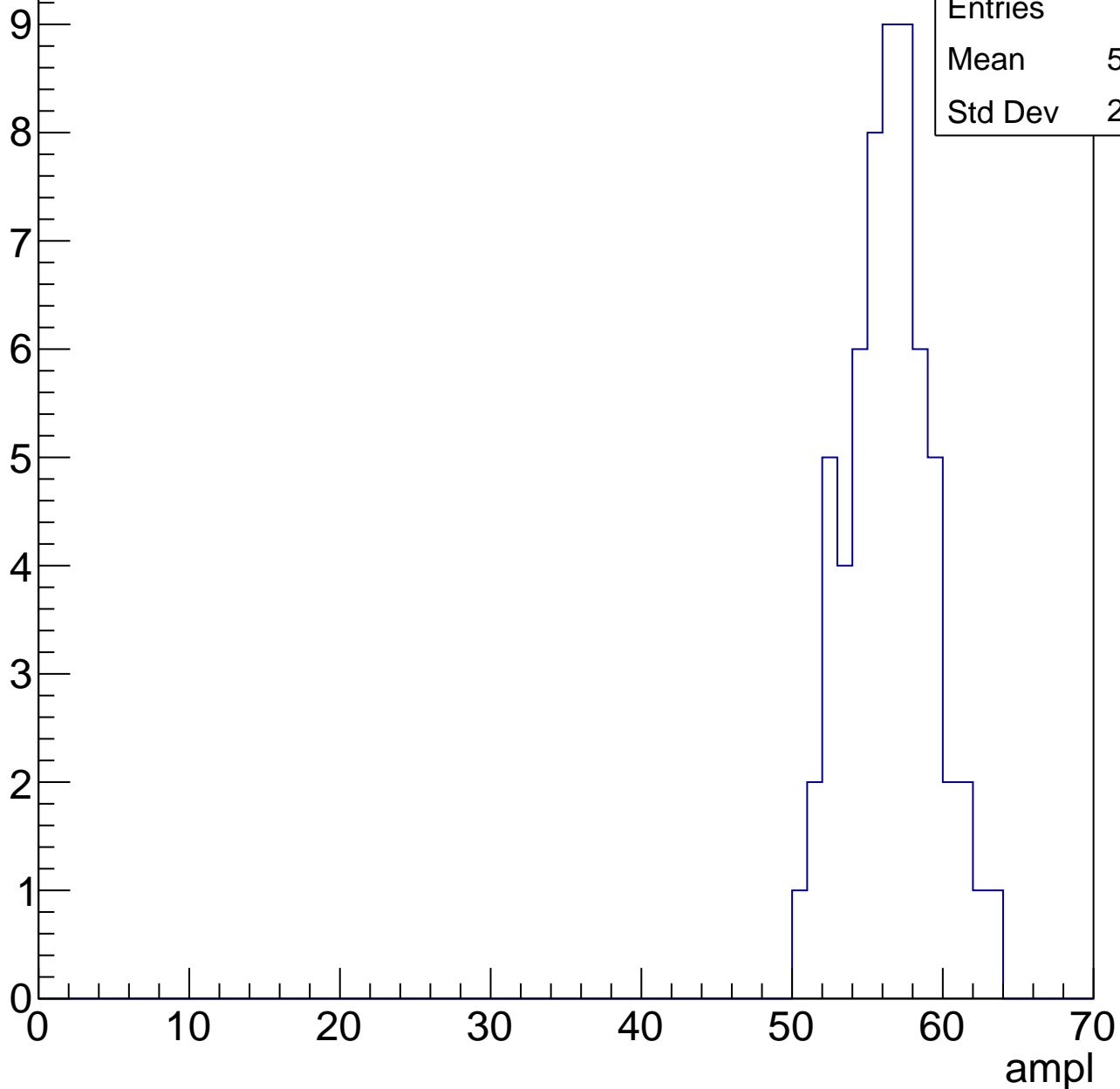
Entries	69
Mean	49.52
Std Dev	3.308



# B1L003S, U6-ch27, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



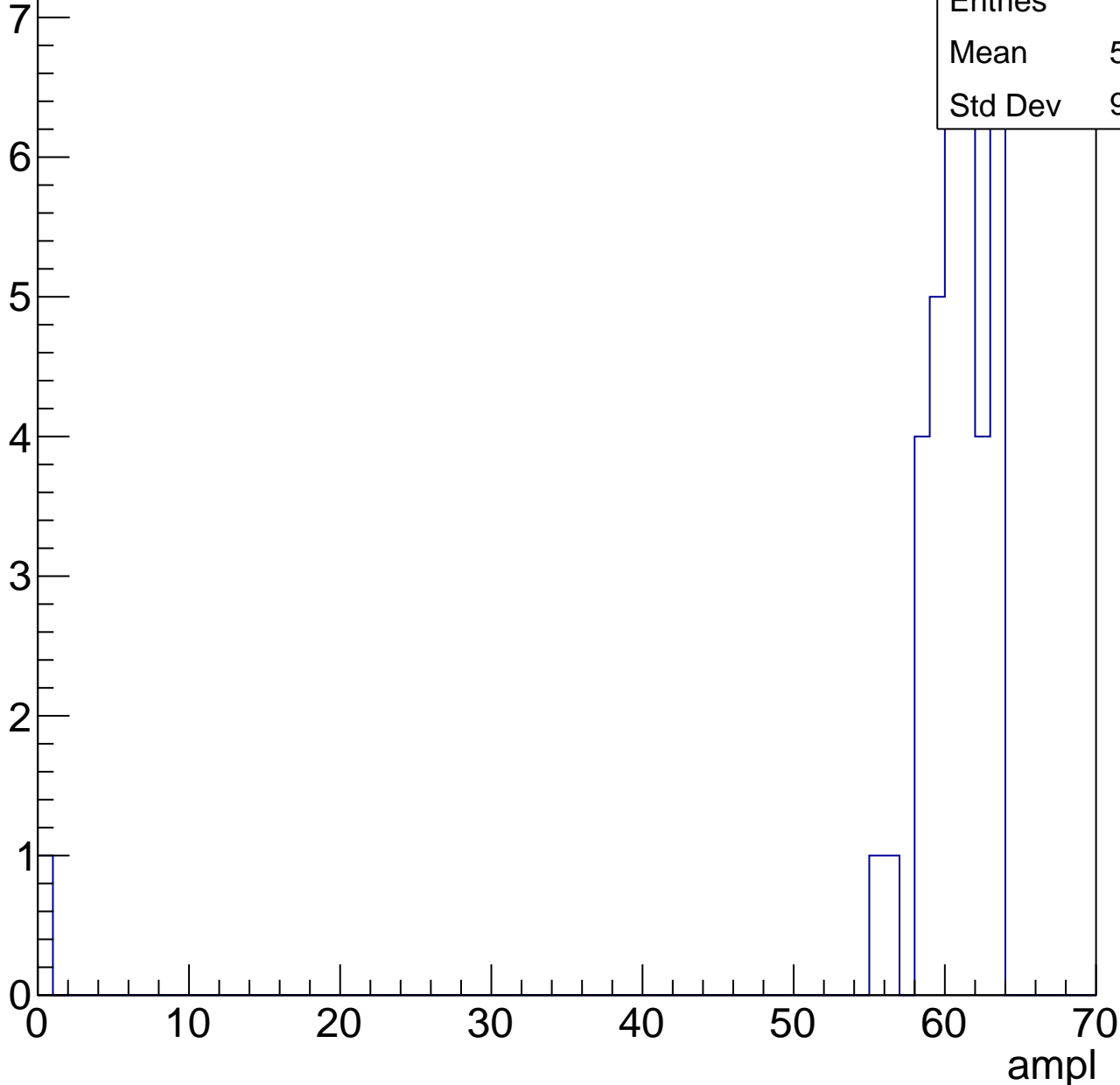
Entries	61
Mean	55.98
Std Dev	2.802

# B1L003S, U6-ch27, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	37
Mean	58.76
Std Dev	9.988

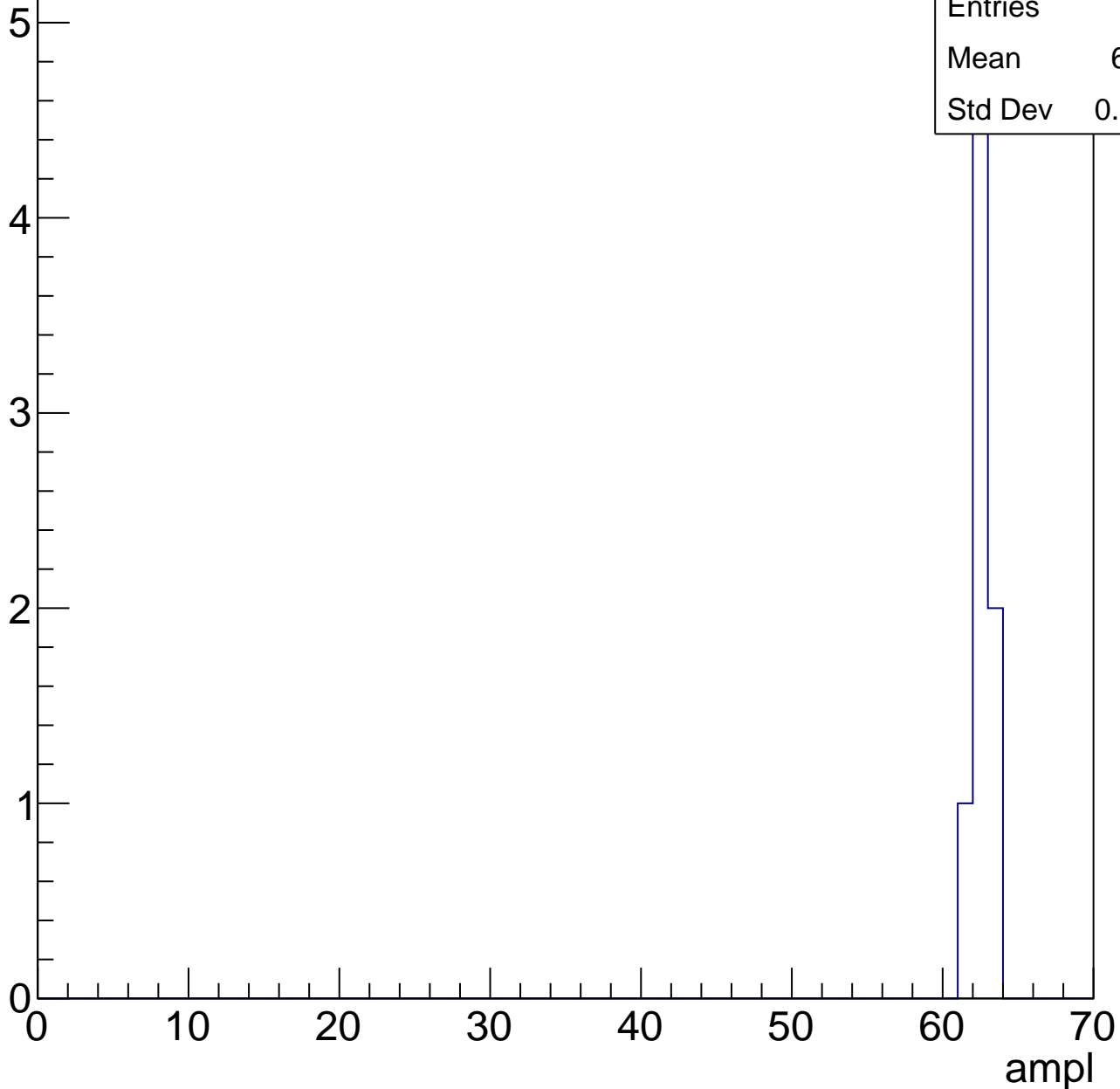


# B1L003S, U6-ch27, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	8
Mean	62.12
Std Dev	0.5995





# B1L003S, U6-ch27, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	22
Std Dev	0

# B1L003S, U6-ch28, adc0

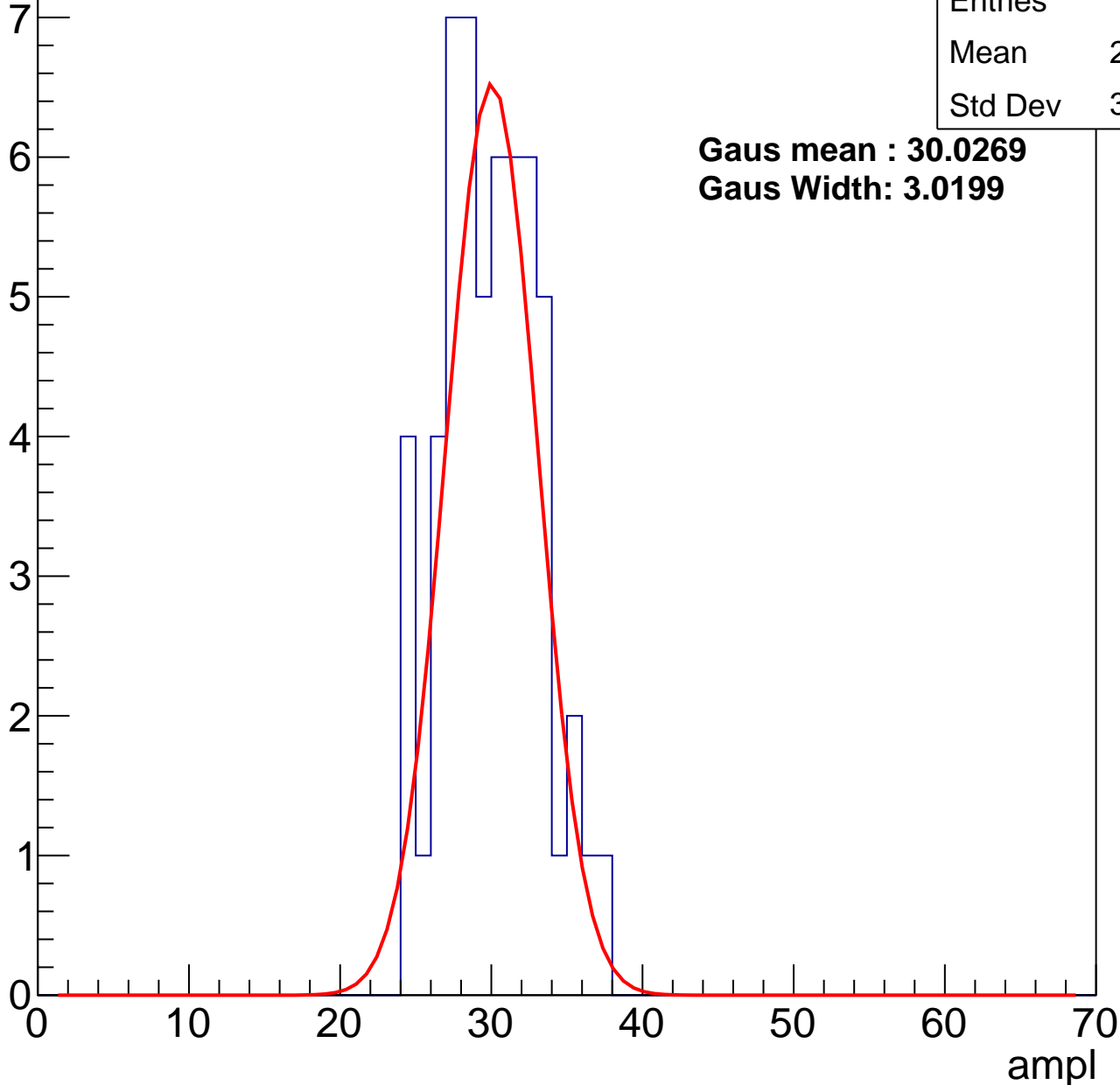
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	29.55
Std Dev	3.116

**Gaus mean : 30.0269**

**Gaus Width: 3.0199**



# B1L003S, U6-ch28, adc1

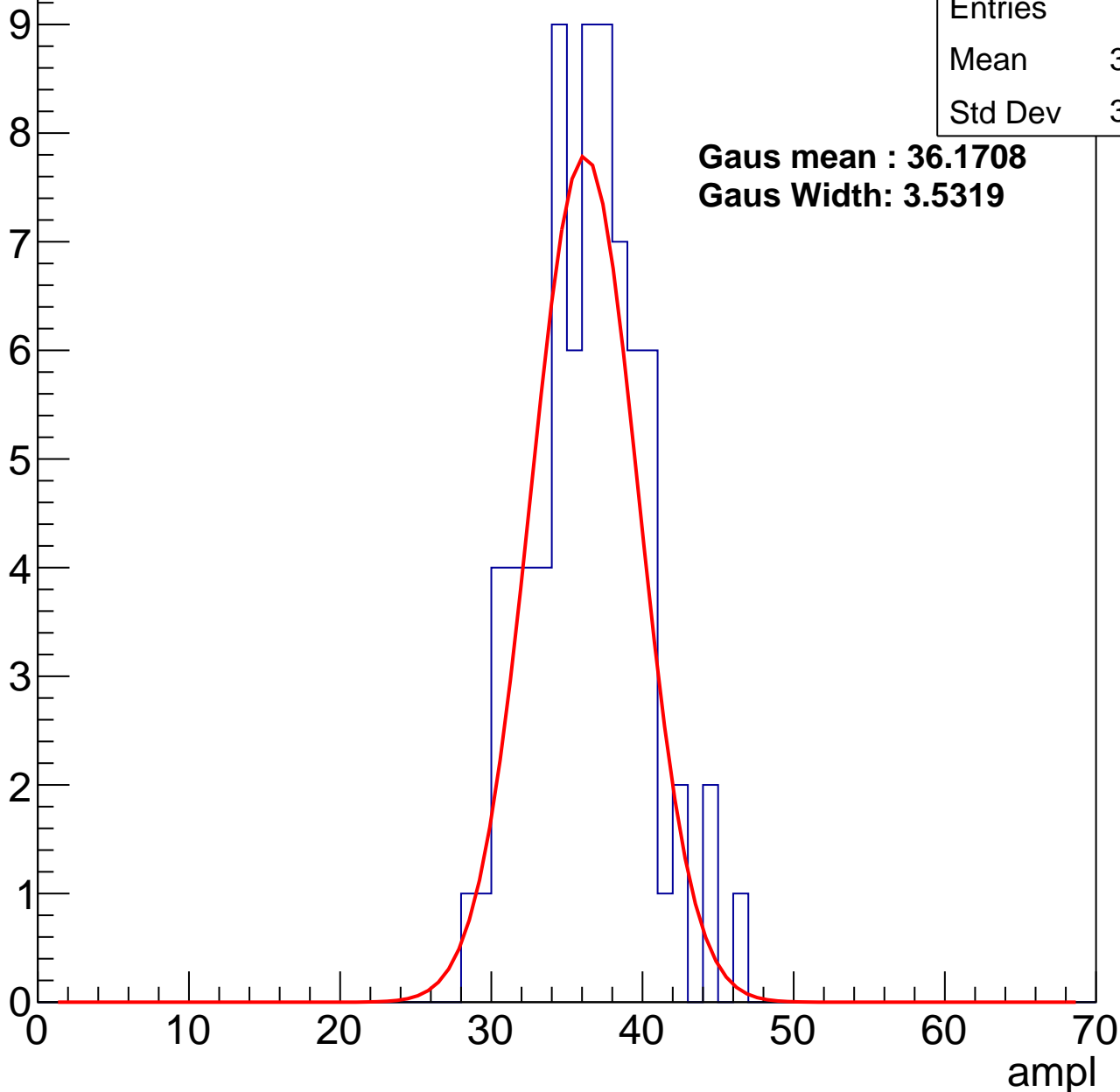
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	76
Mean	35.96
Std Dev	3.647

**Gaus mean : 36.1708**

**Gaus Width: 3.5319**



# B1L003S, U6-ch28, adc2

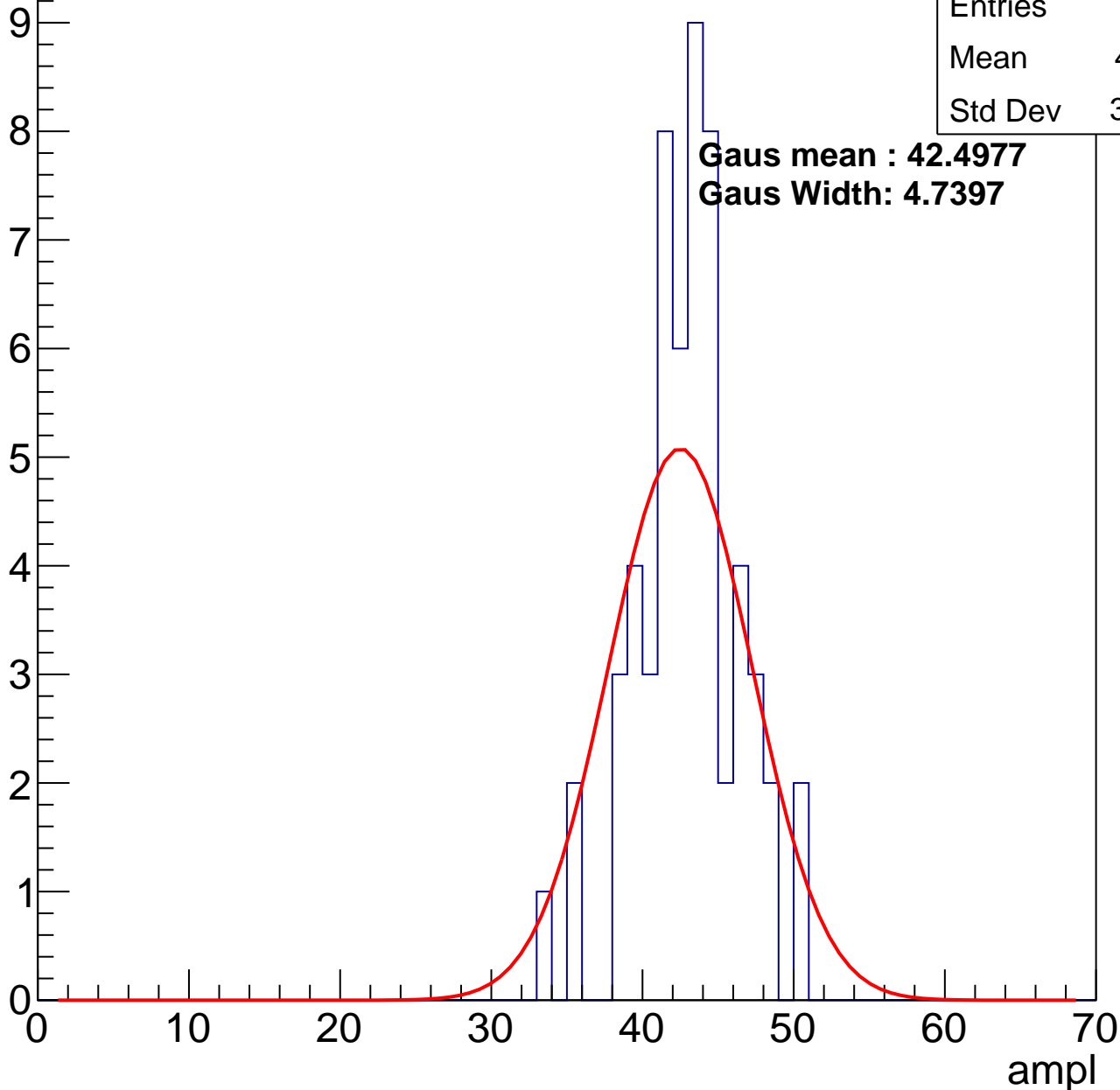
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	42.51
Std Dev	3.419

**Gaus mean : 42.4977**

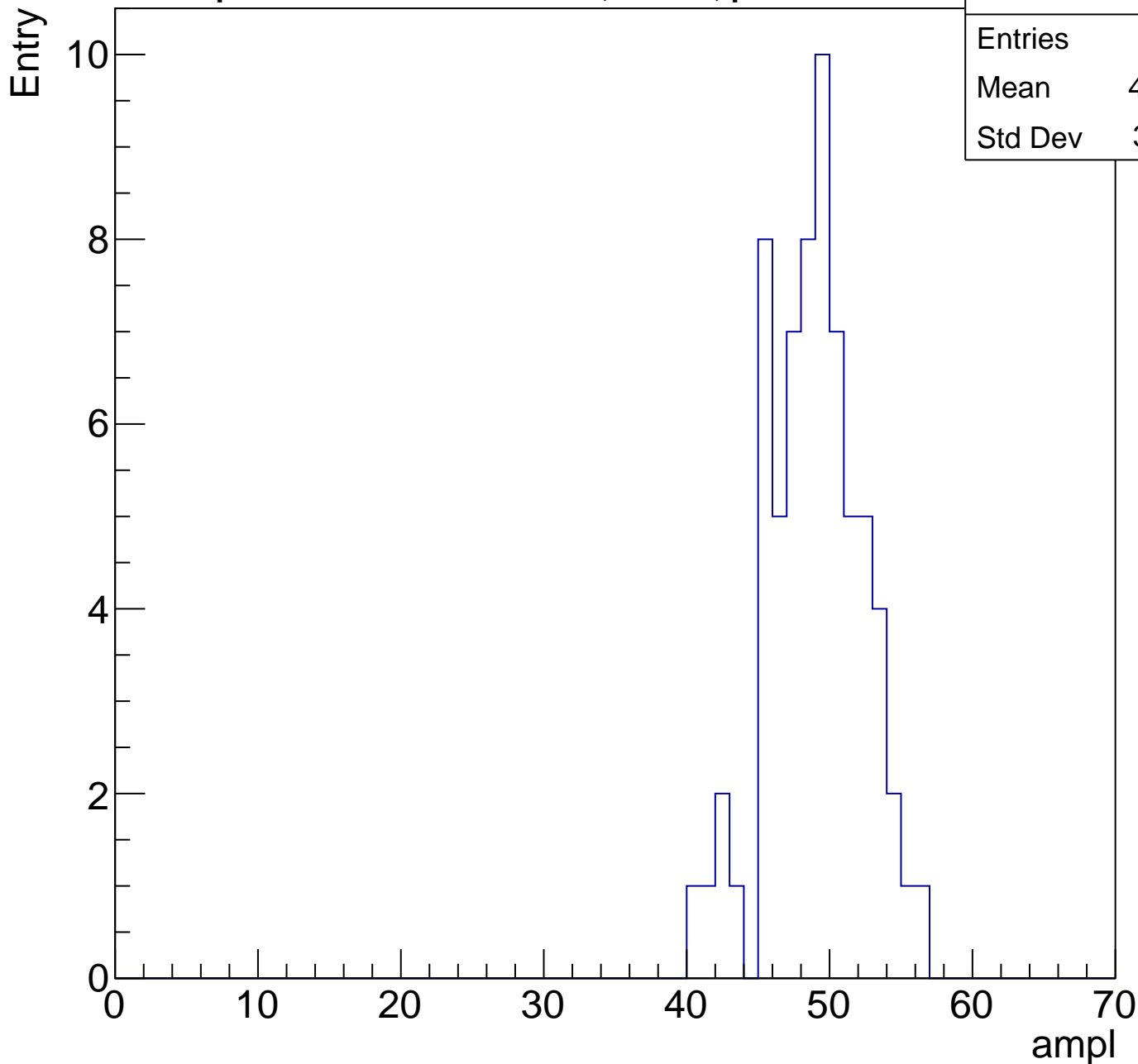
**Gaus Width: 4.7397**



# B1L003S, U6-ch28, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	68
Mean	48.49
Std Dev	3.301



# B1L003S, U6-ch28, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

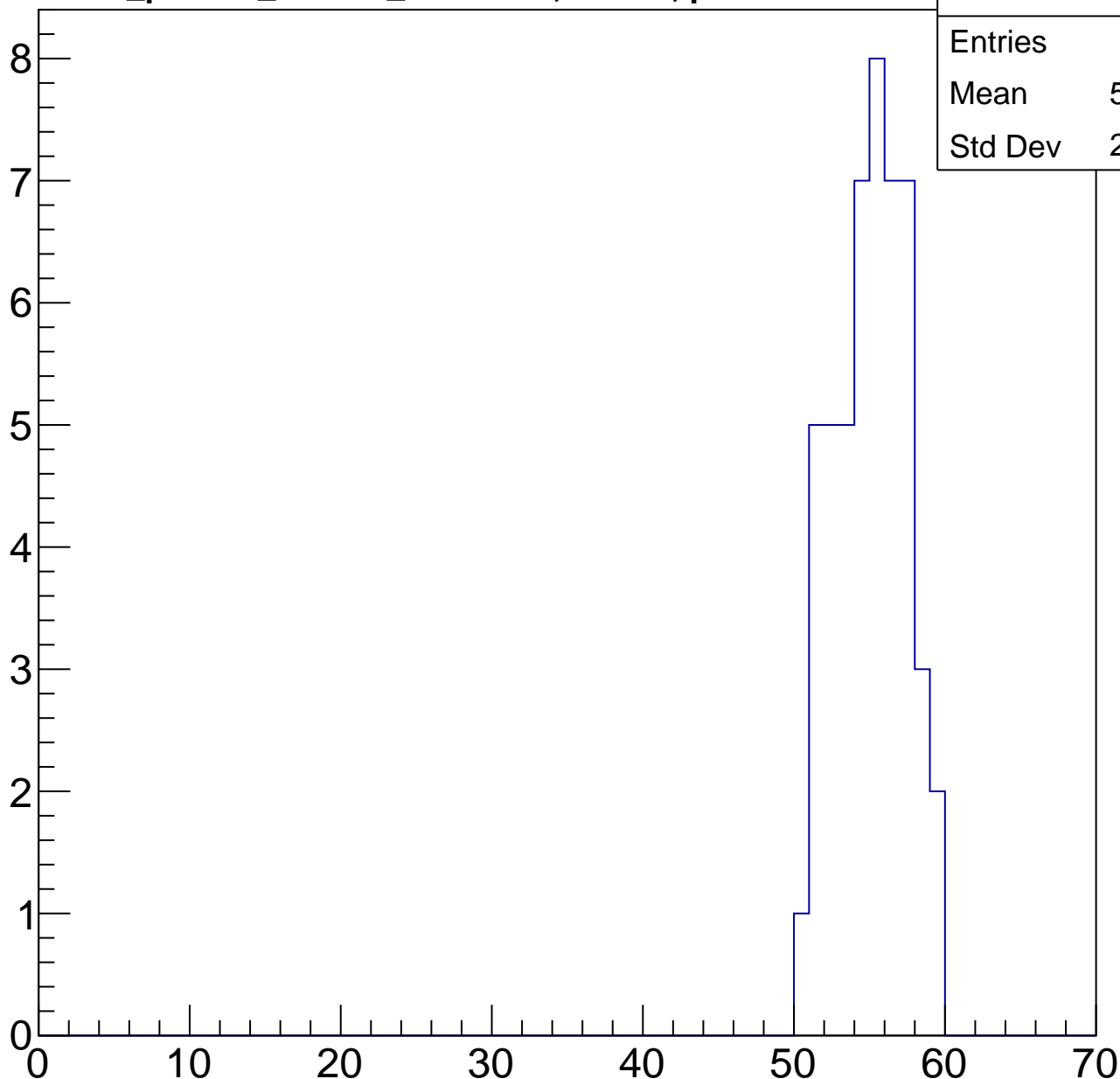
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	50
Mean	54.62
Std Dev	2.297

ampl

0 10 20 30 40 50 60 70

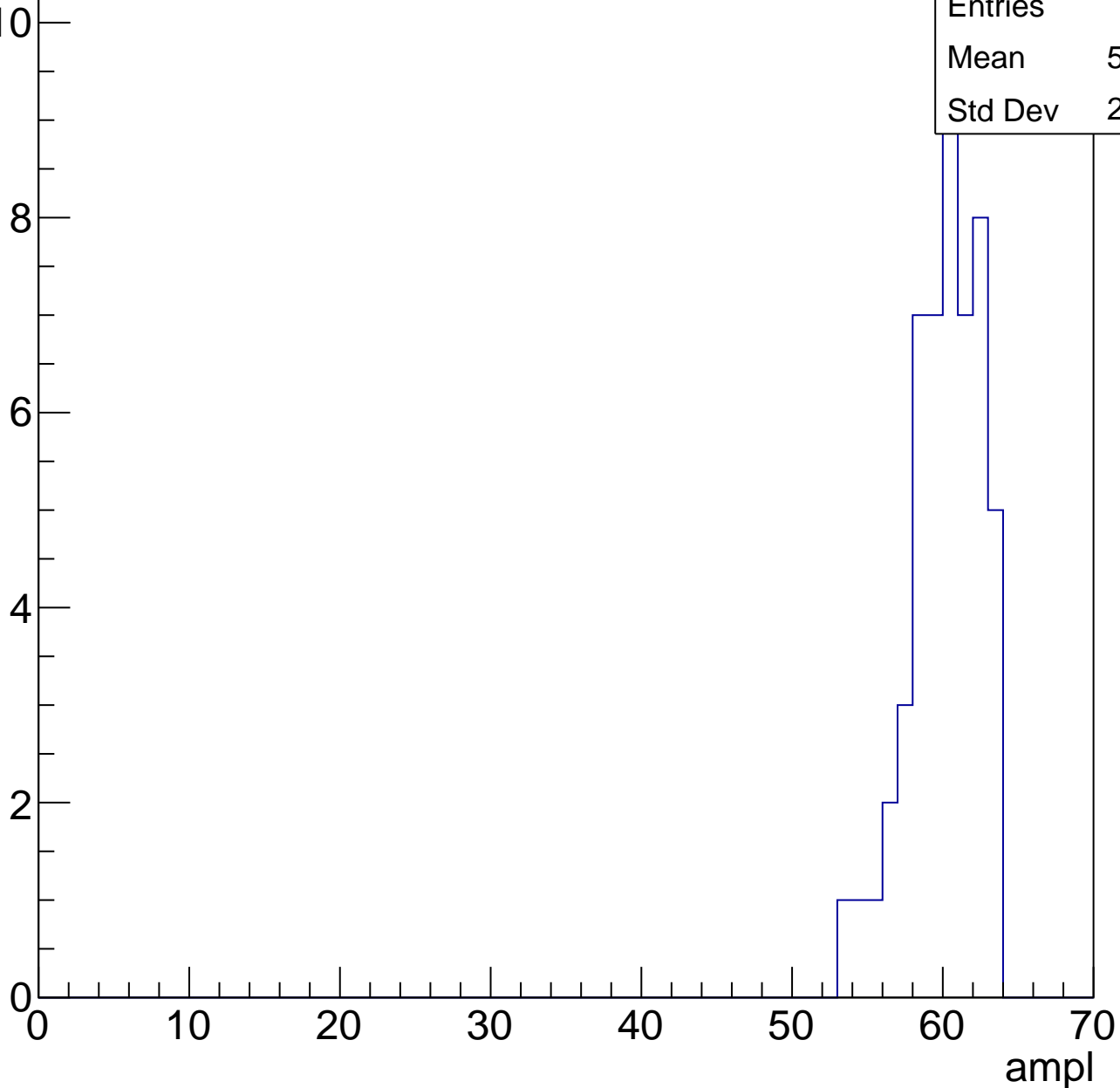


# B1L003S, U6-ch28, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	52
Mean	59.65
Std Dev	2.328

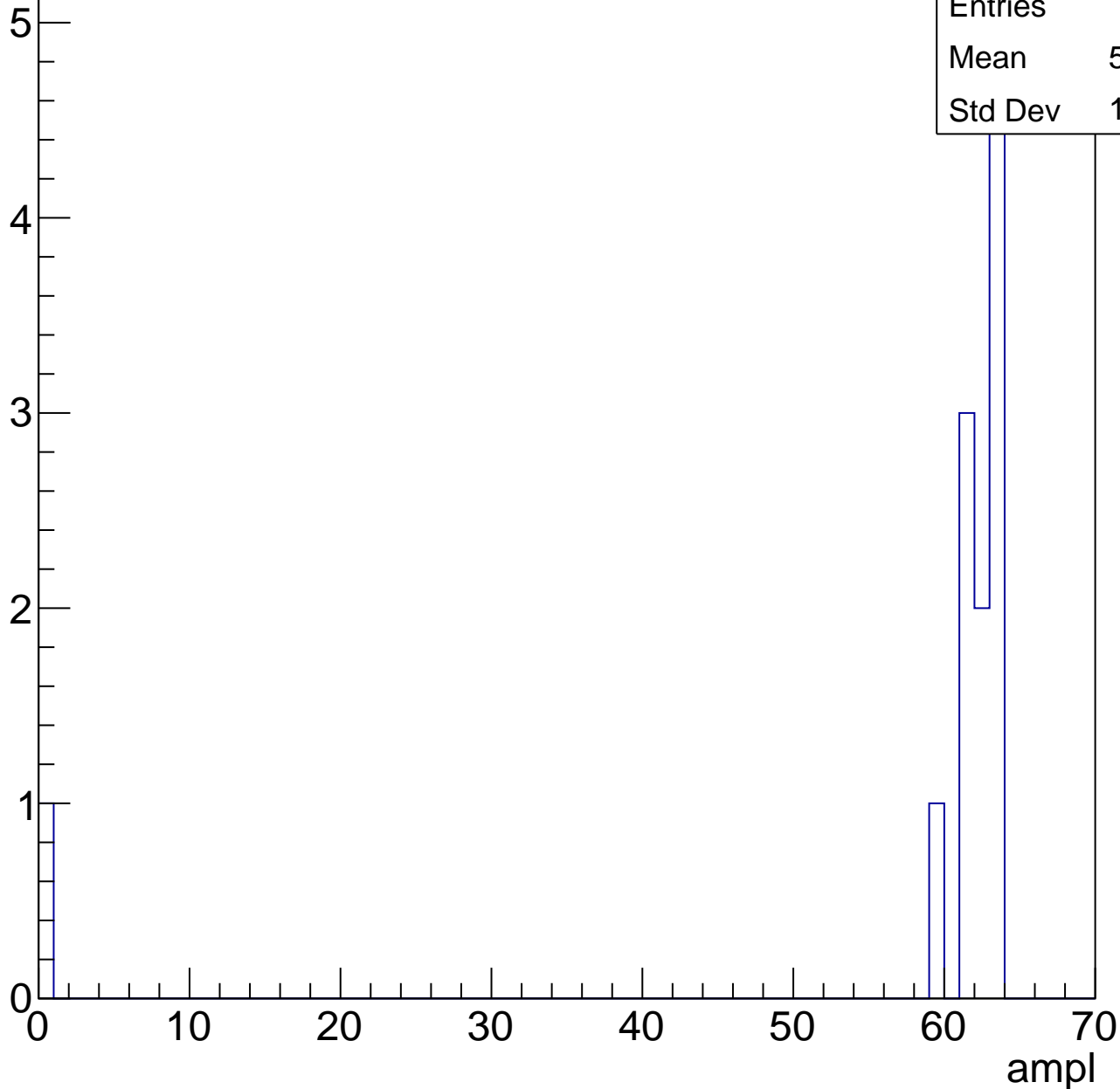


# B1L003S, U6-ch28, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	12
Mean	56.75
Std Dev	17.15





# B1L003S, U6-ch28, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch29, adc0

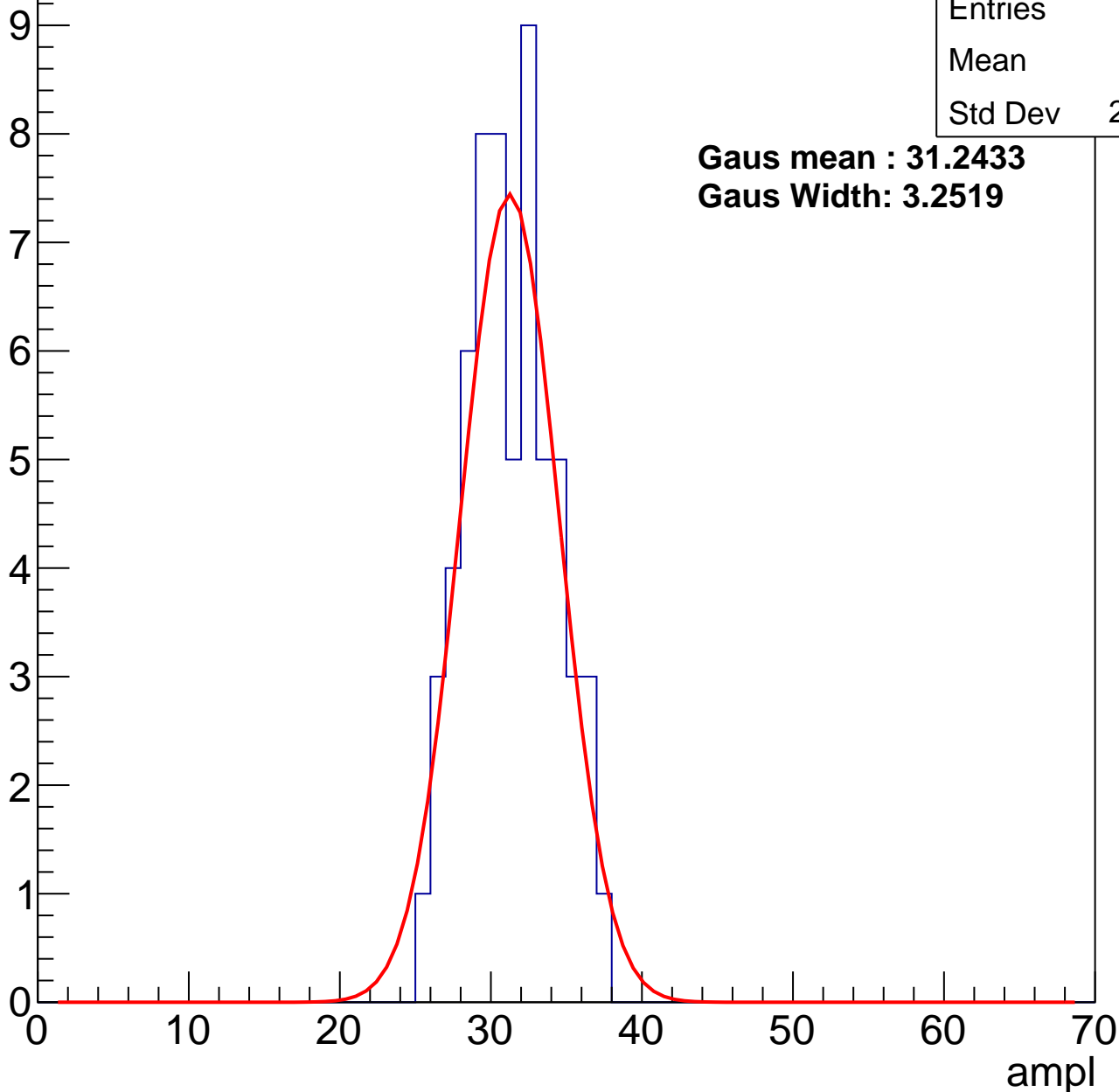
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	30.8
Std Dev	2.862

**Gaus mean : 31.2433**

**Gaus Width: 3.2519**



# B1L003S, U6-ch29, adc1

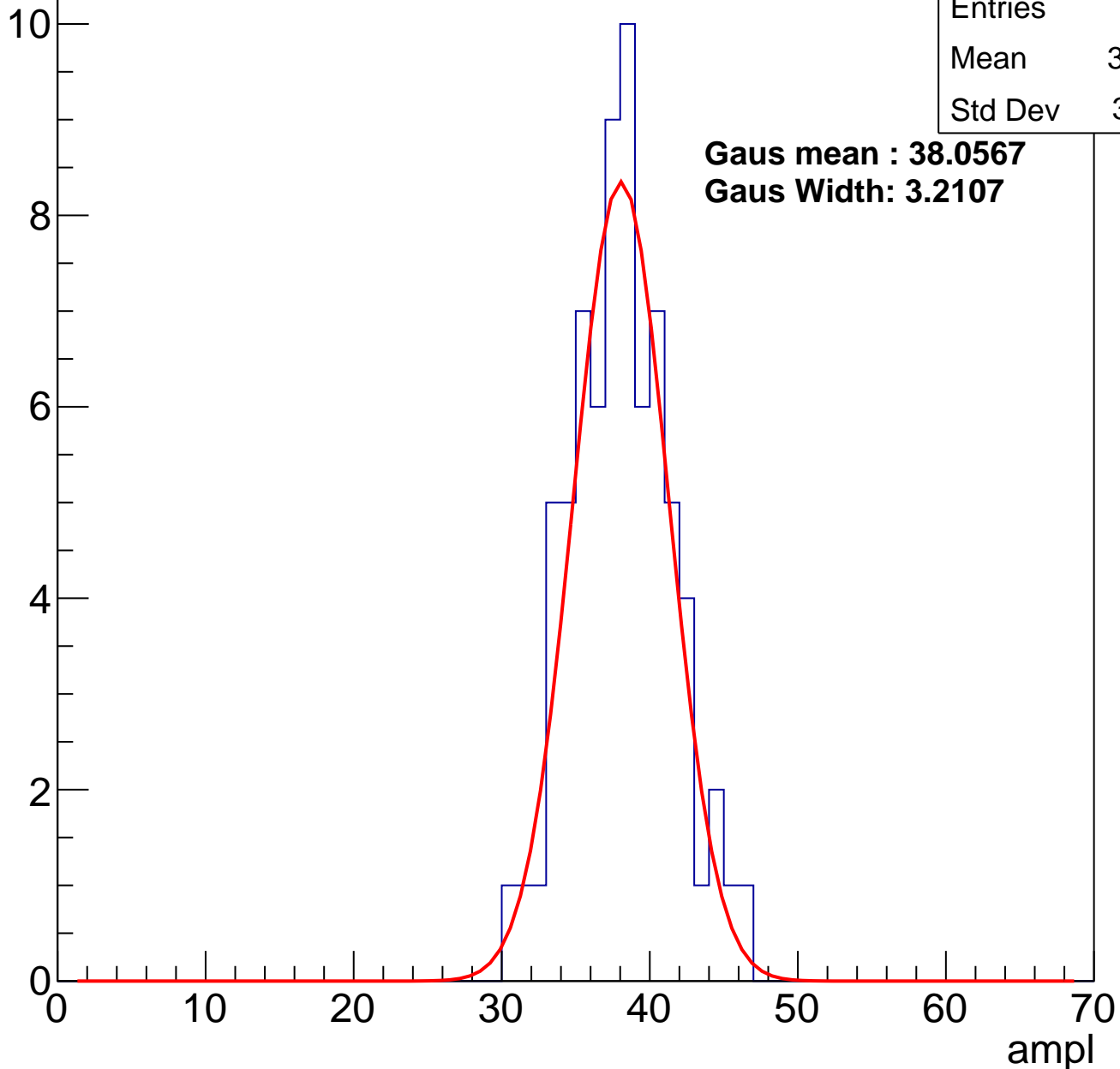
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	72
Mean	37.65
Std Dev	3.321

**Gaus mean : 38.0567**

**Gaus Width: 3.2107**

Entry



# B1L003S, U6-ch29, adc2

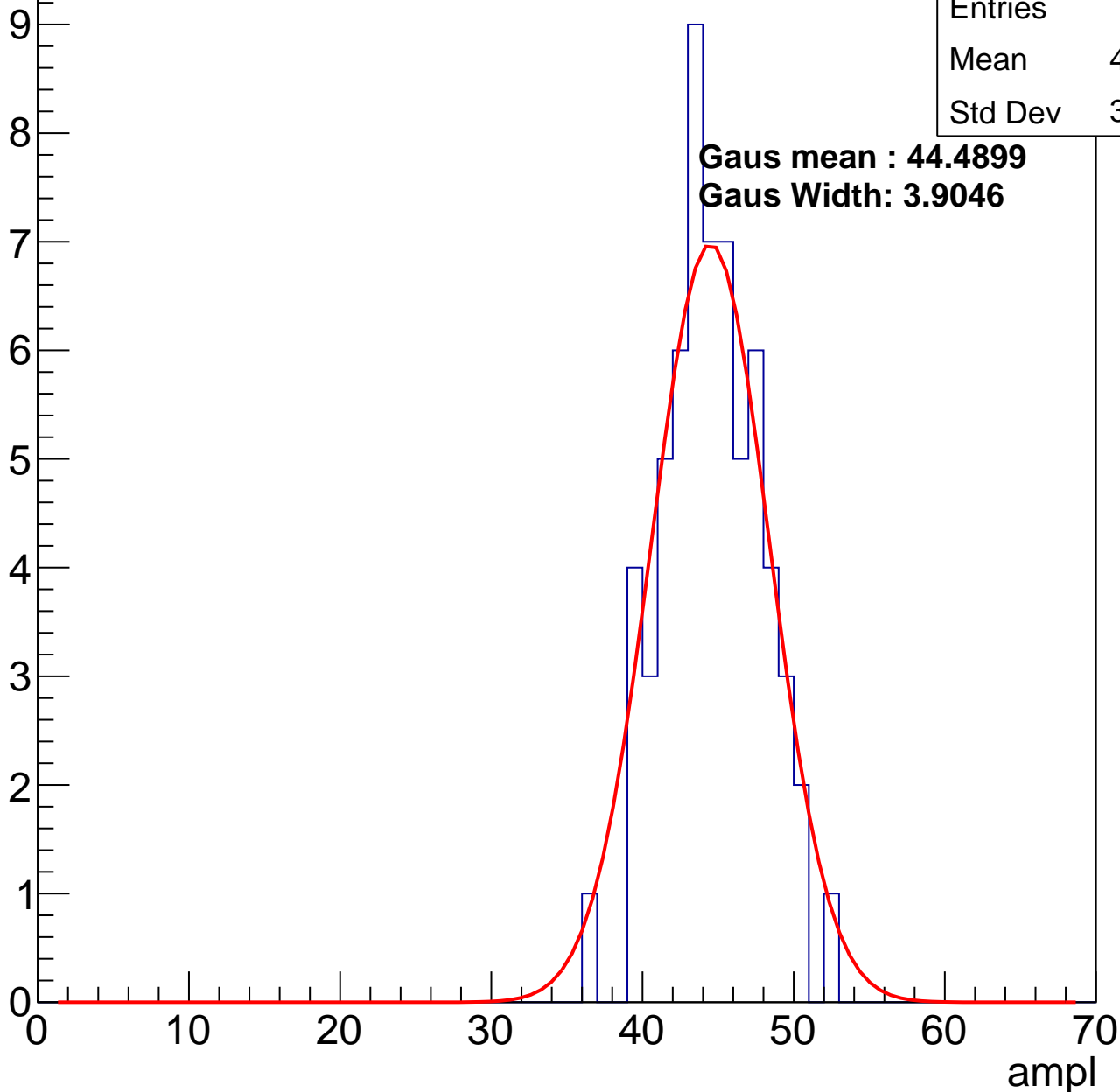
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	44.16
Std Dev	3.198

**Gaus mean : 44.4899**

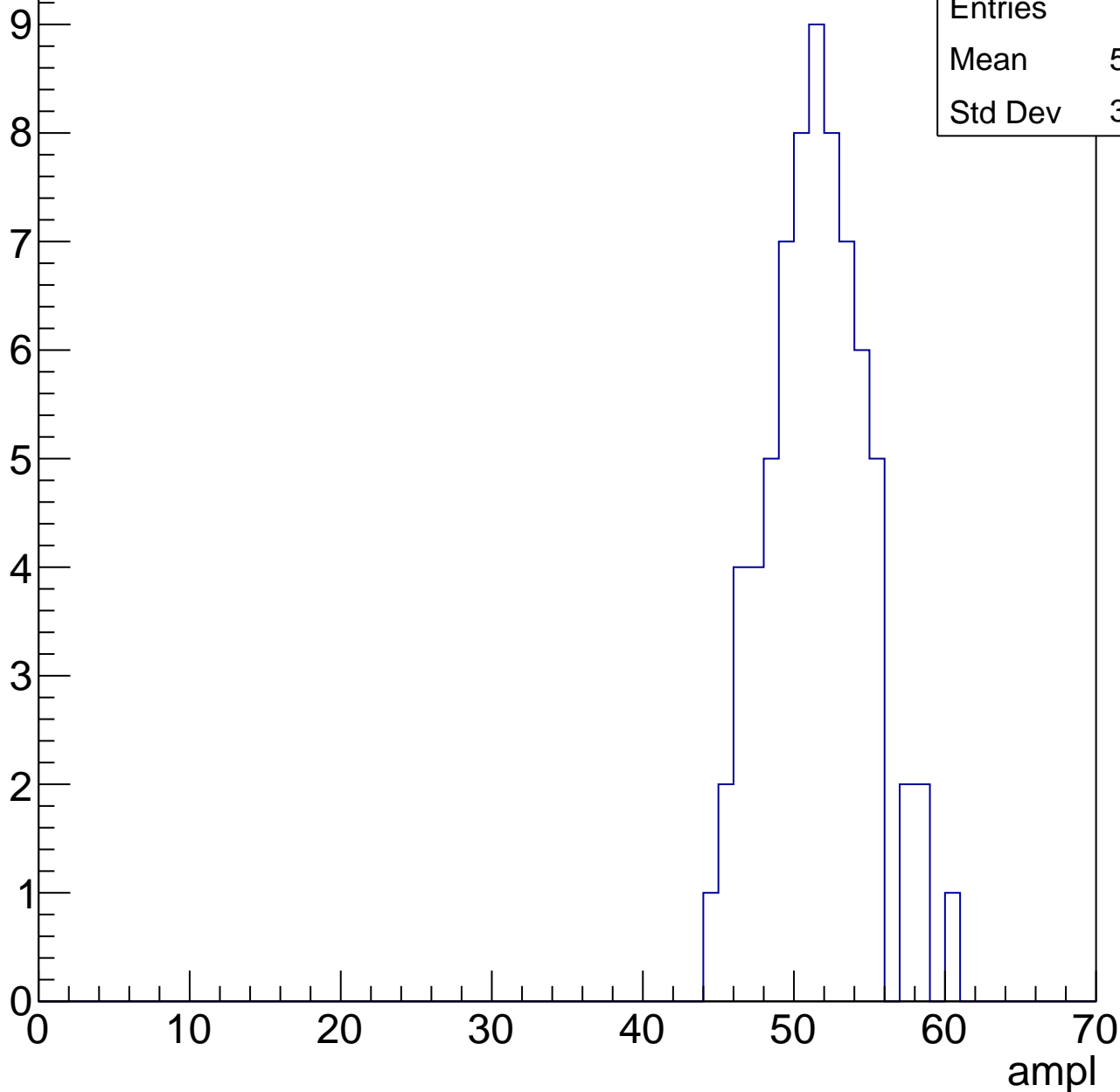
**Gaus Width: 3.9046**



# B1L003S, U6-ch29, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

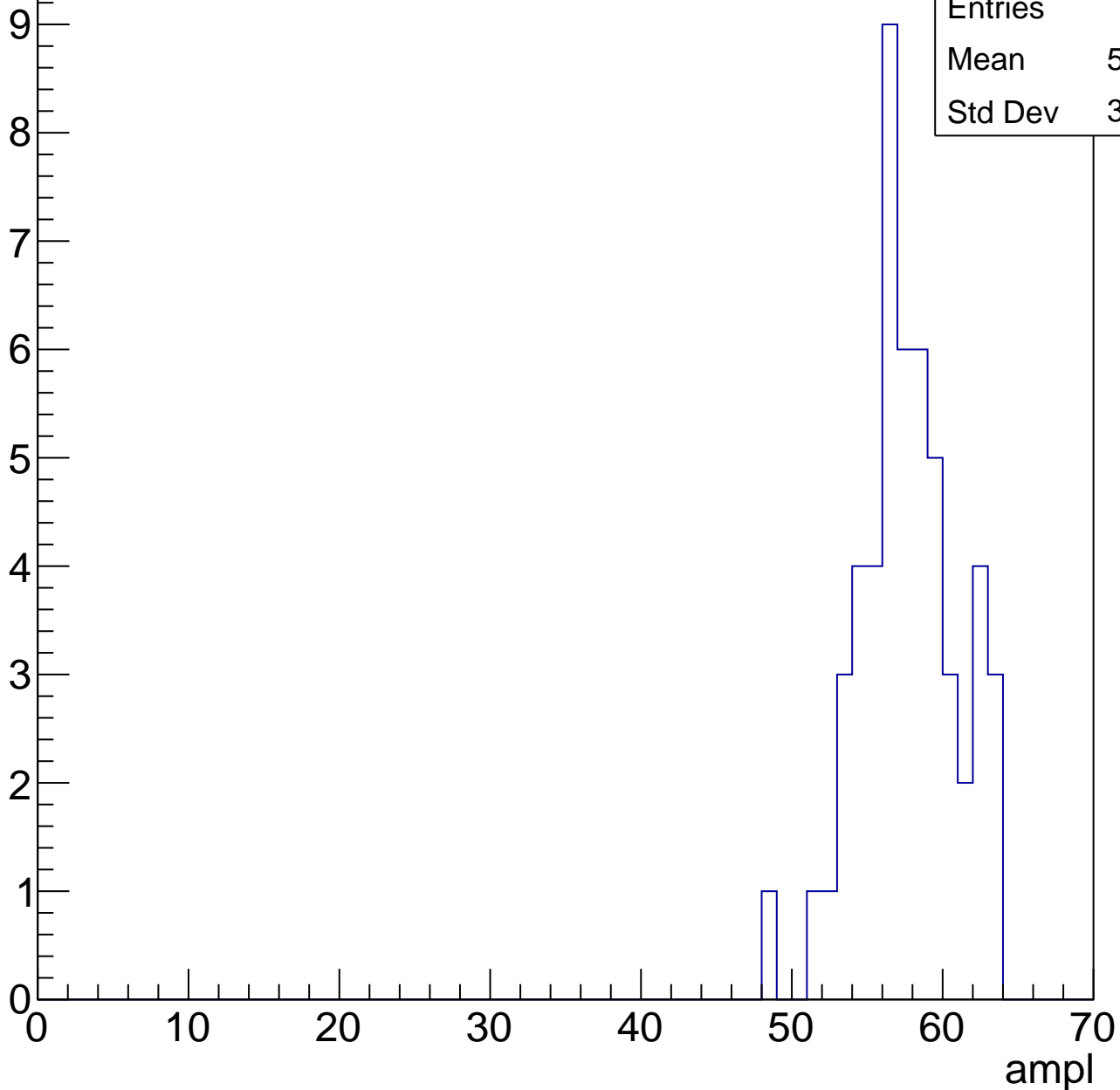


# B1L003S, U6-ch29, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	52
Mean	57.19
Std Dev	3.229

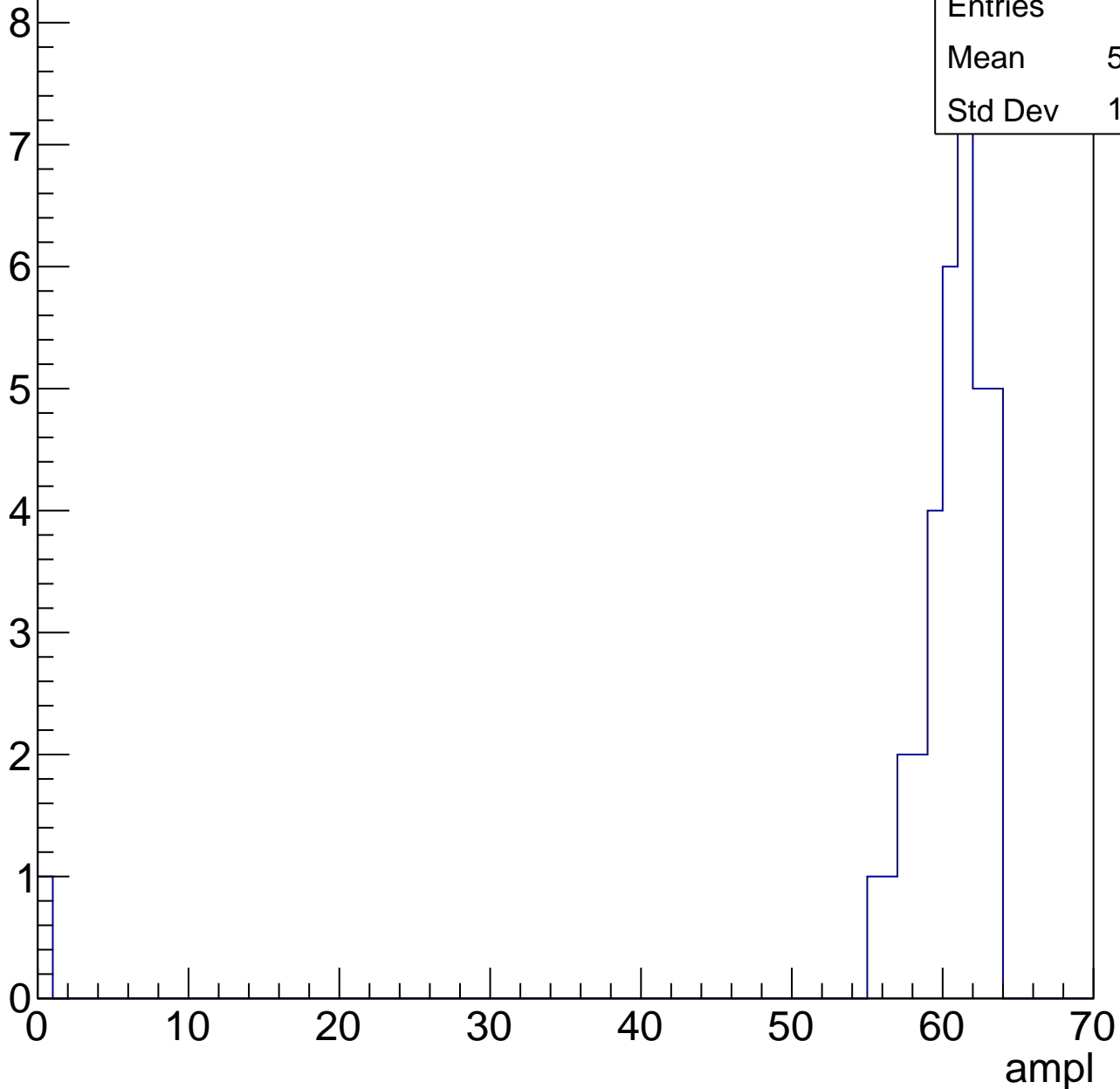


# B1L003S, U6-ch29, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	35
Mean	58.57
Std Dev	10.24



# B1L003S, U6-ch29, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch29, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U6-ch30, adc0

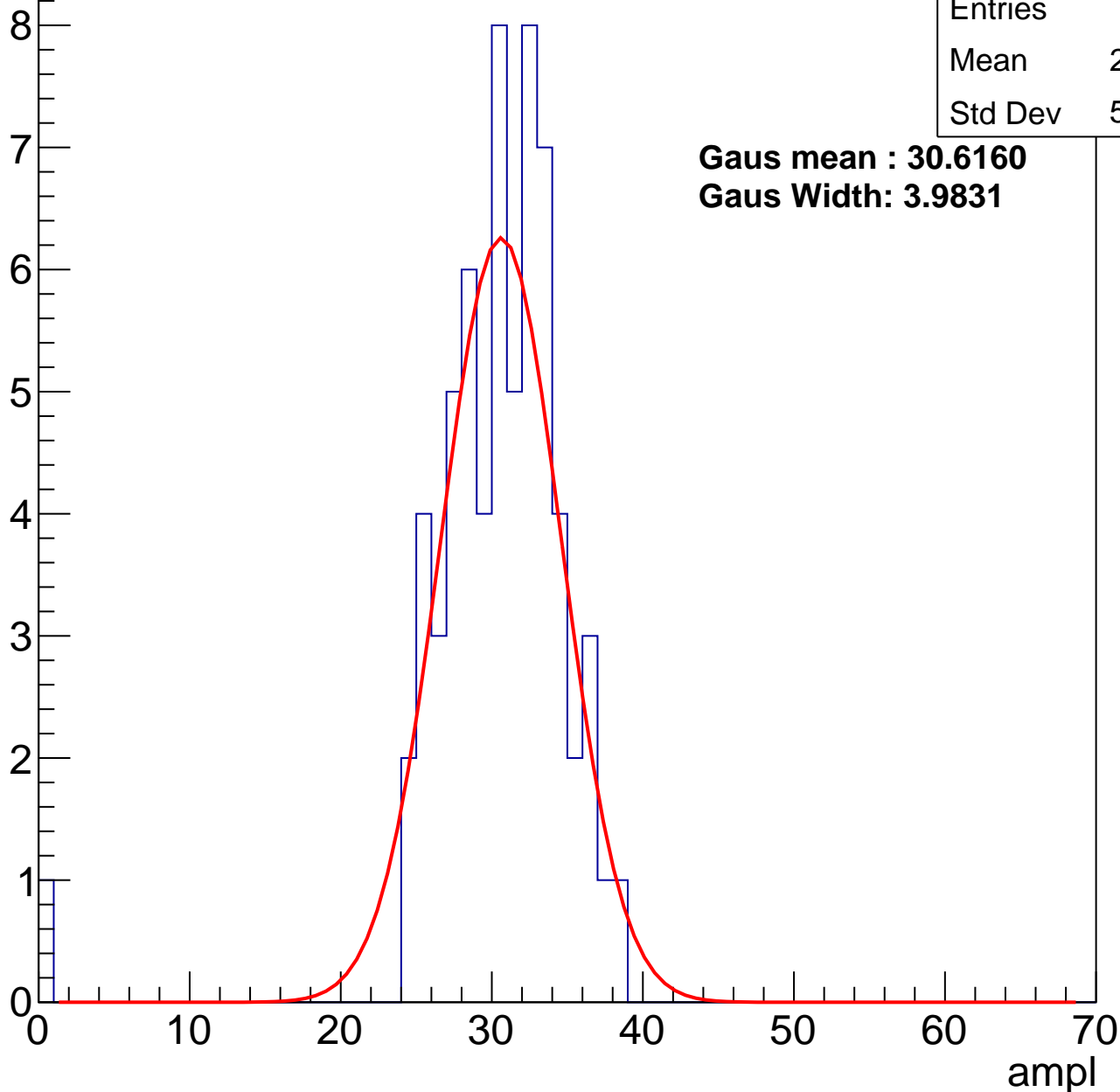
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	29.94
Std Dev	5.043

**Gaus mean : 30.6160**

**Gaus Width: 3.9831**



# B1L003S, U6-ch30, adc1

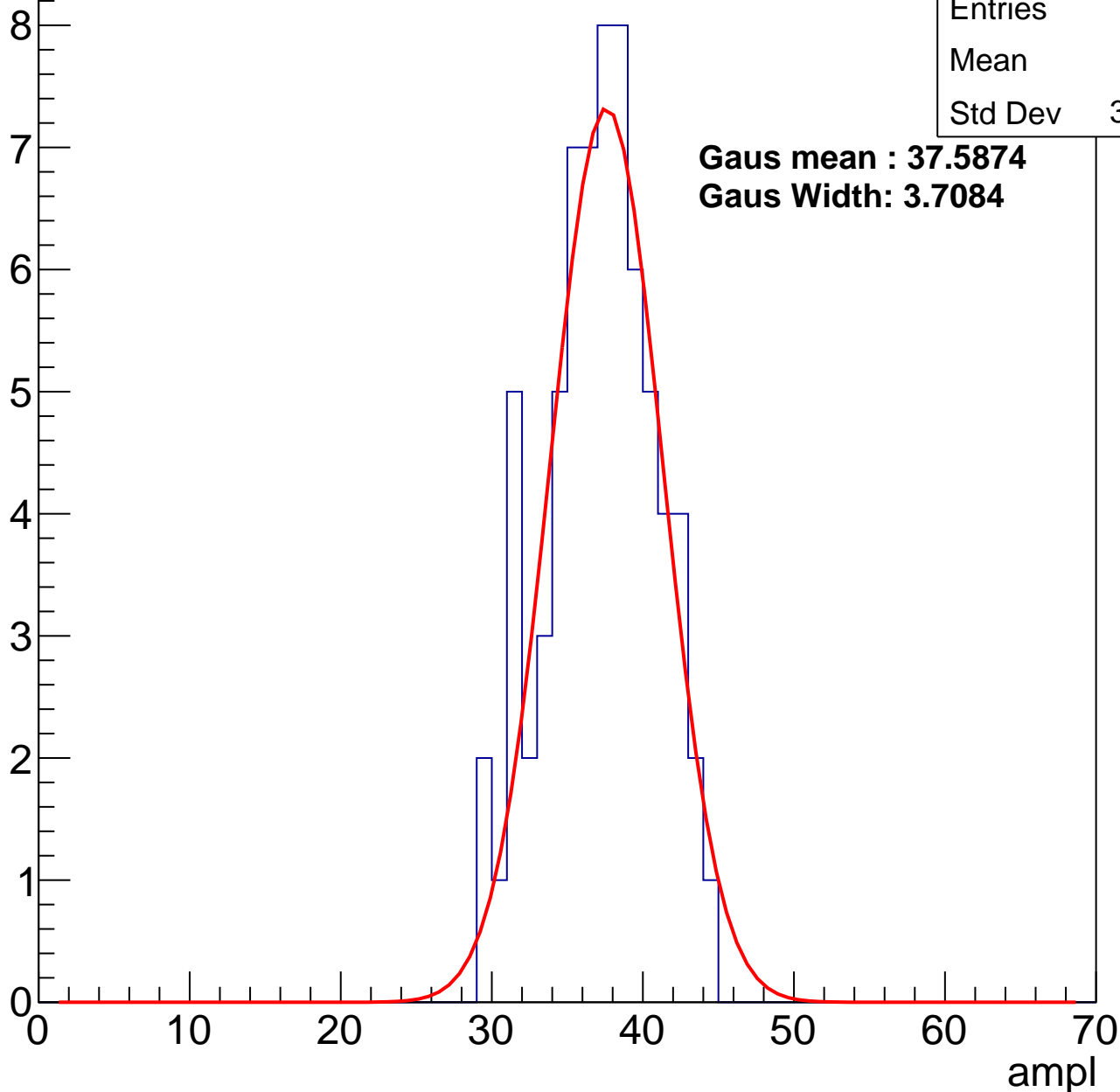
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	36.7
Std Dev	3.567

**Gaus mean : 37.5874**

**Gaus Width: 3.7084**



# B1L003S, U6-ch30, adc2

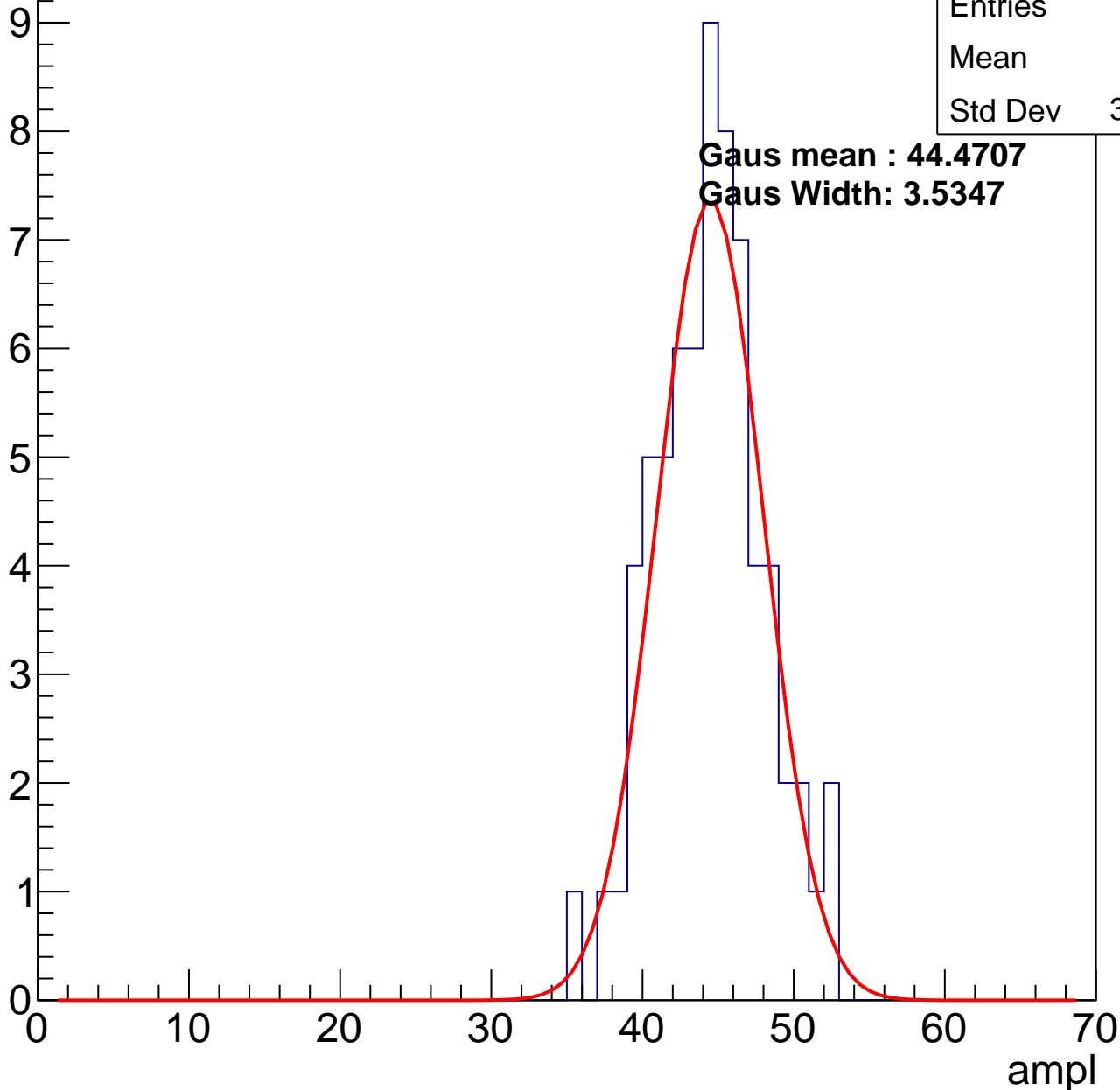
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	44
Std Dev	3.548

**Gaus mean : 44.4707**

**Gaus Width: 3.5347**

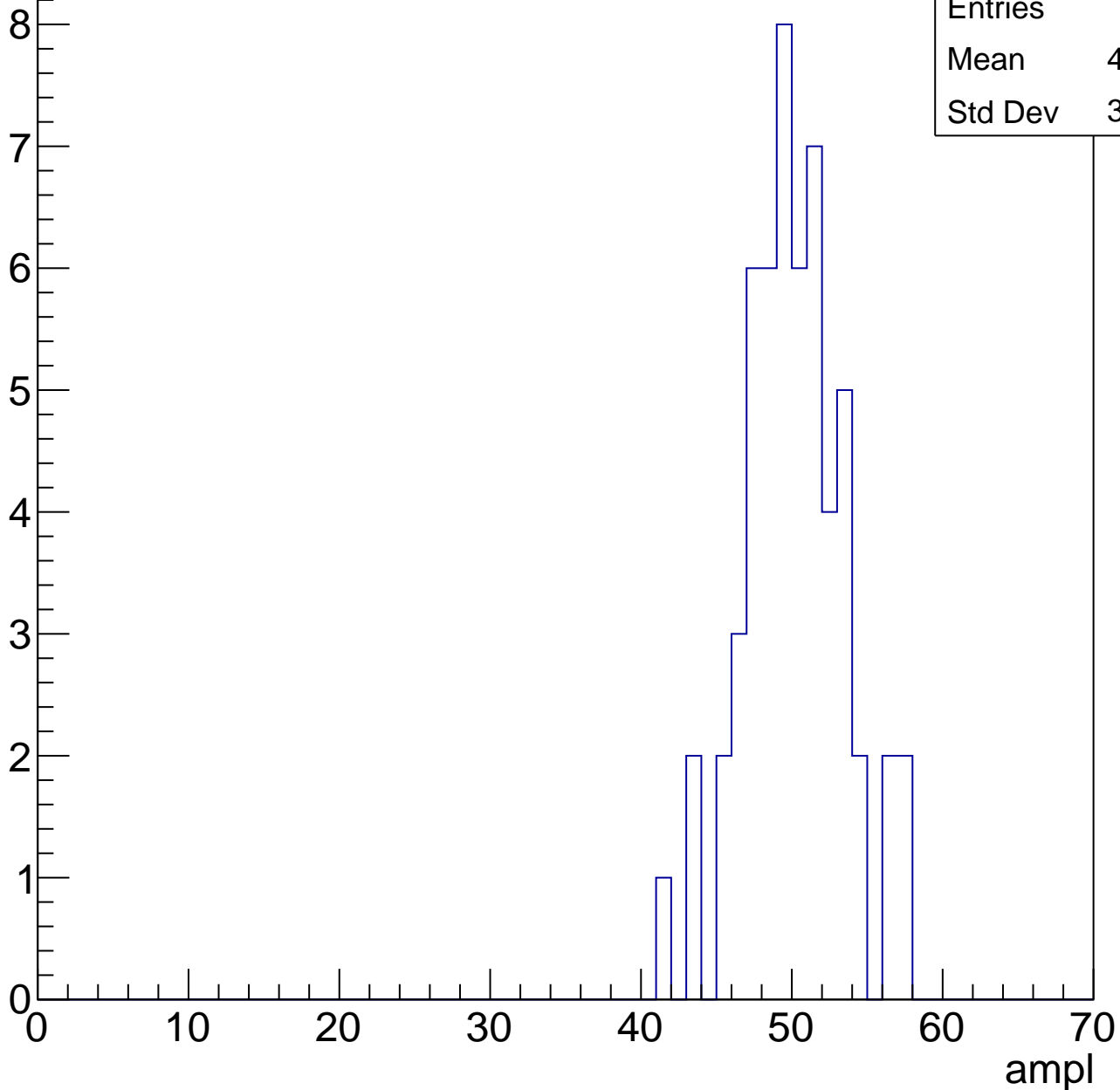


# B1L003S, U6-ch30, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

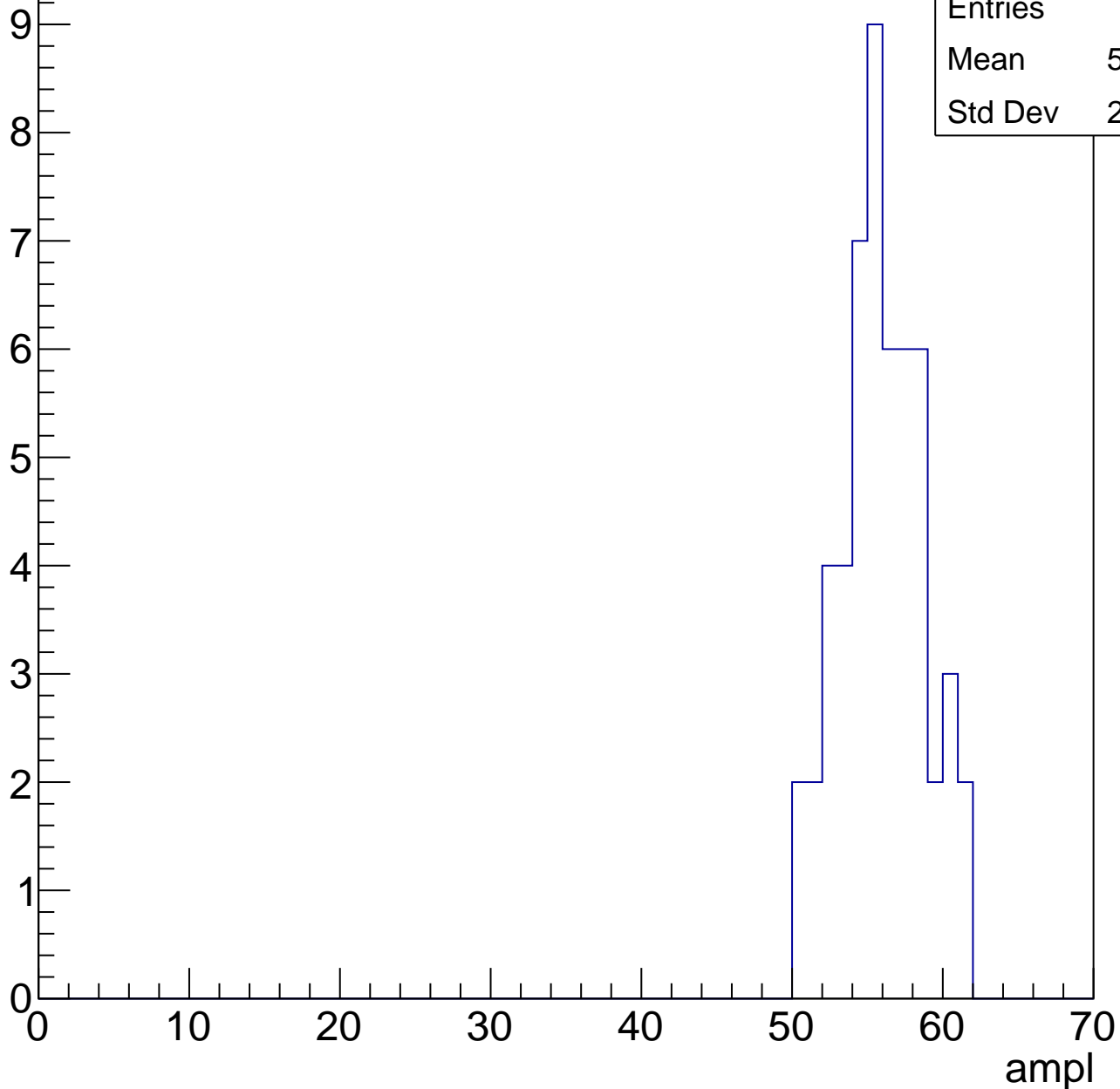
Entries	56
Mean	49.66
Std Dev	3.345



# B1L003S, U6-ch30, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



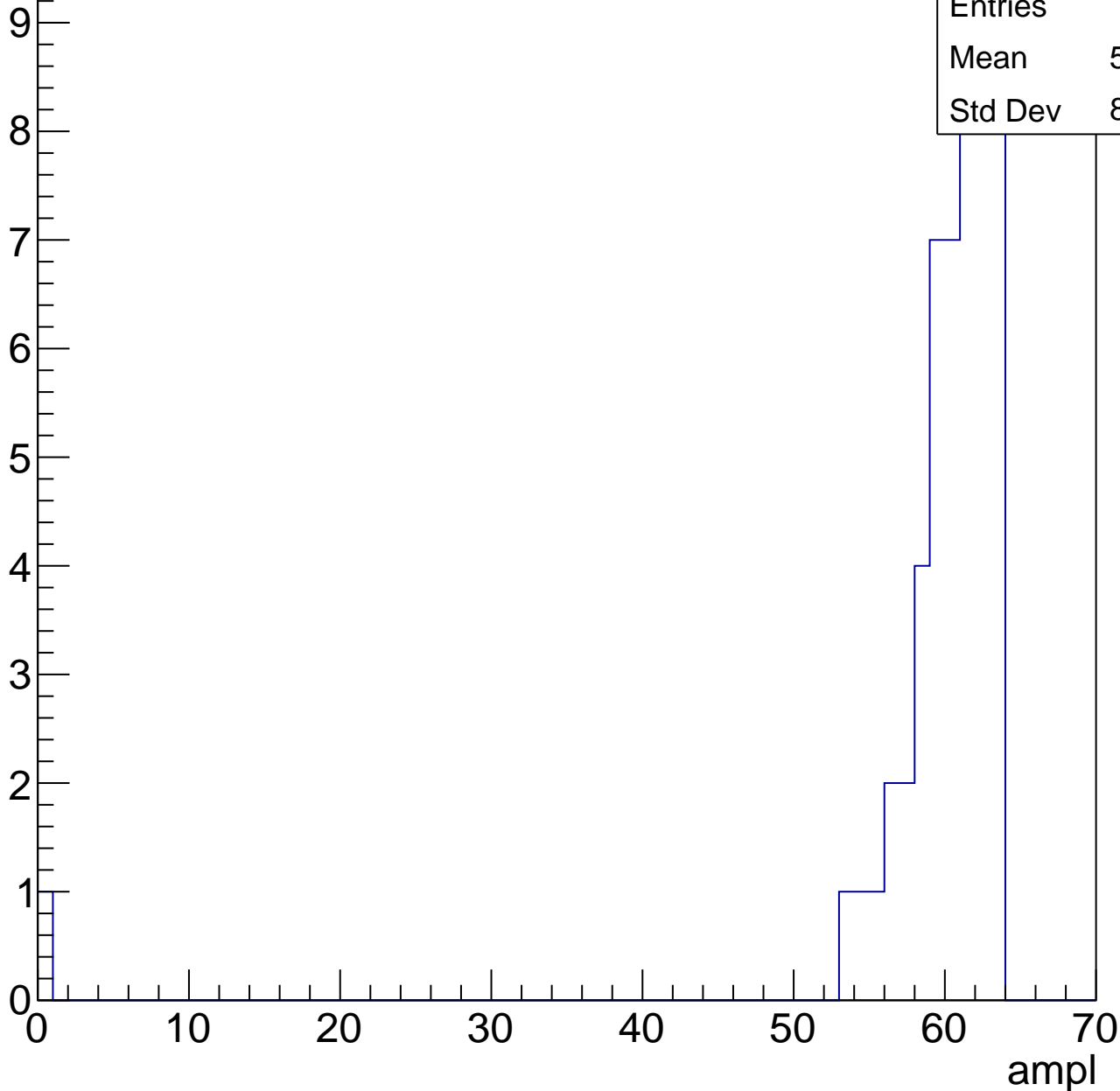
Entries	53
Mean	55.49
Std Dev	2.717

# B1L003S, U6-ch30, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	51
Mean	58.88
Std Dev	8.672



# B1L003S, U6-ch30, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch30, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch31, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	74
Mean	29.89
Std Dev	4.567

**Gaus mean : 30.9677**

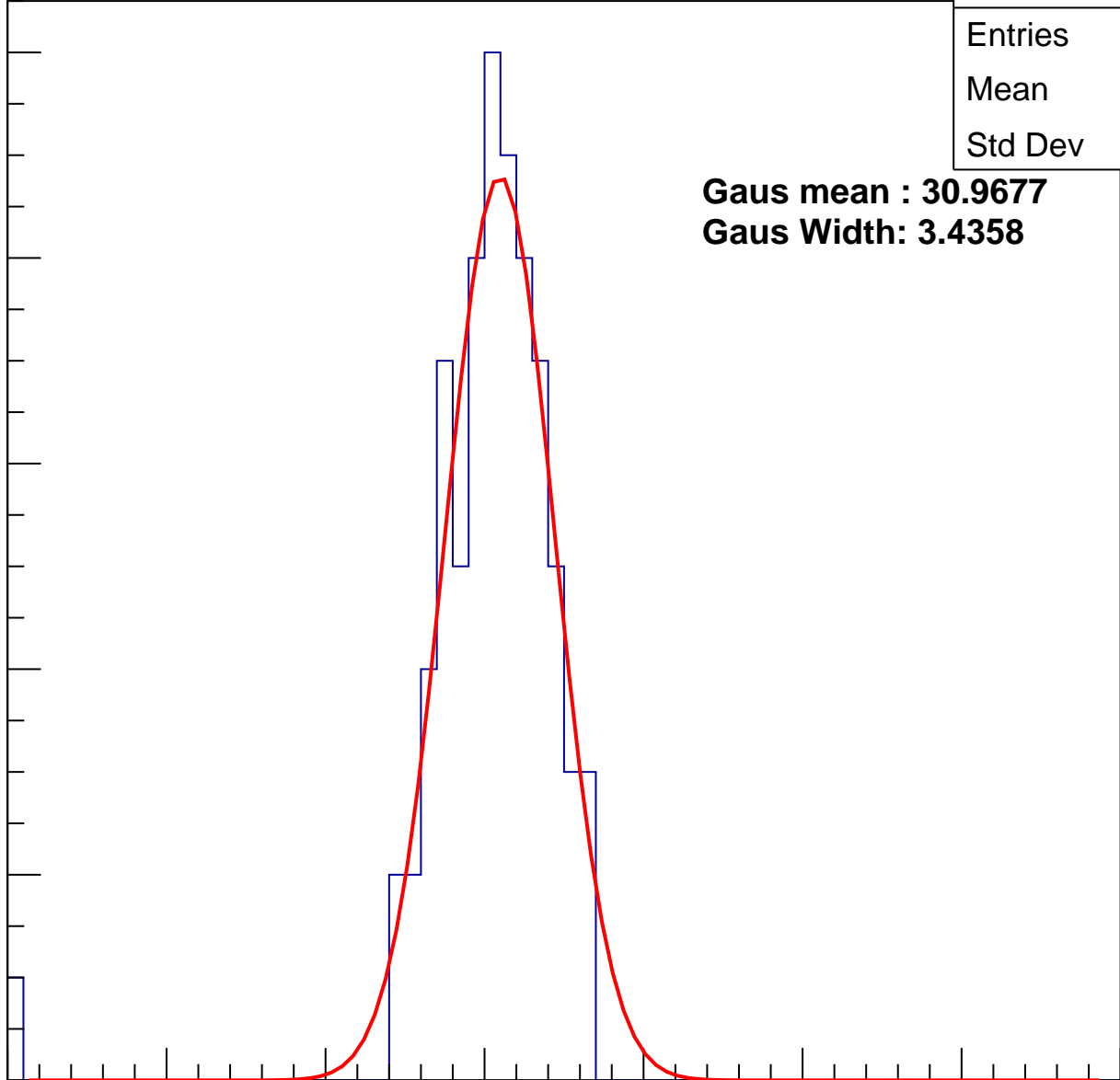
**Gaus Width: 3.4358**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U6-ch31, adc1

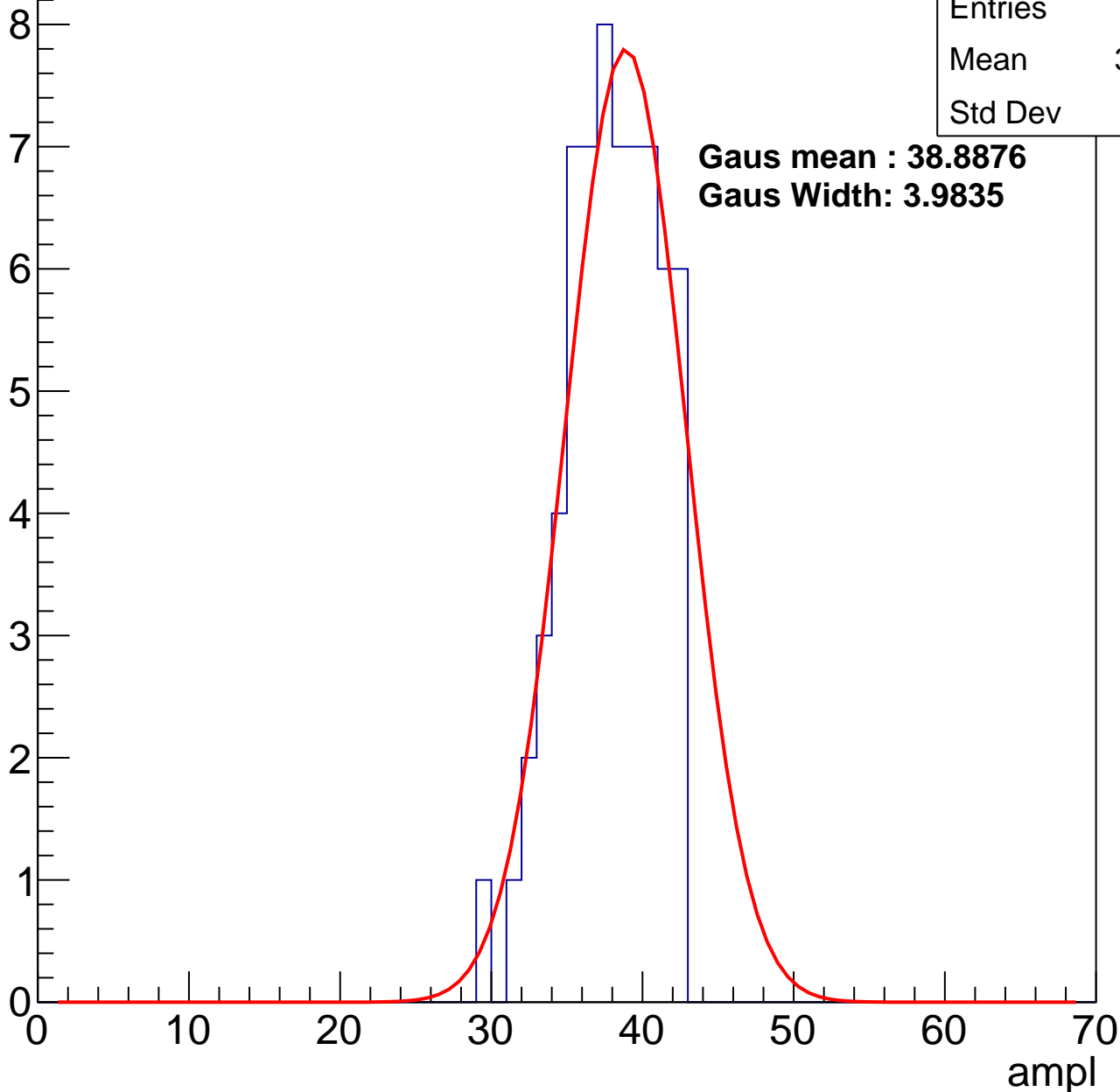
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	37.41
Std Dev	3.02

**Gaus mean : 38.8876**

**Gaus Width: 3.9835**



# B1L003S, U6-ch31, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	60
Mean	43.57
Std Dev	3.333

**Gaus mean : 45.2046**

**Gaus Width: 4.7424**

Entry

10

8

6

4

2

0

0

10

20

30

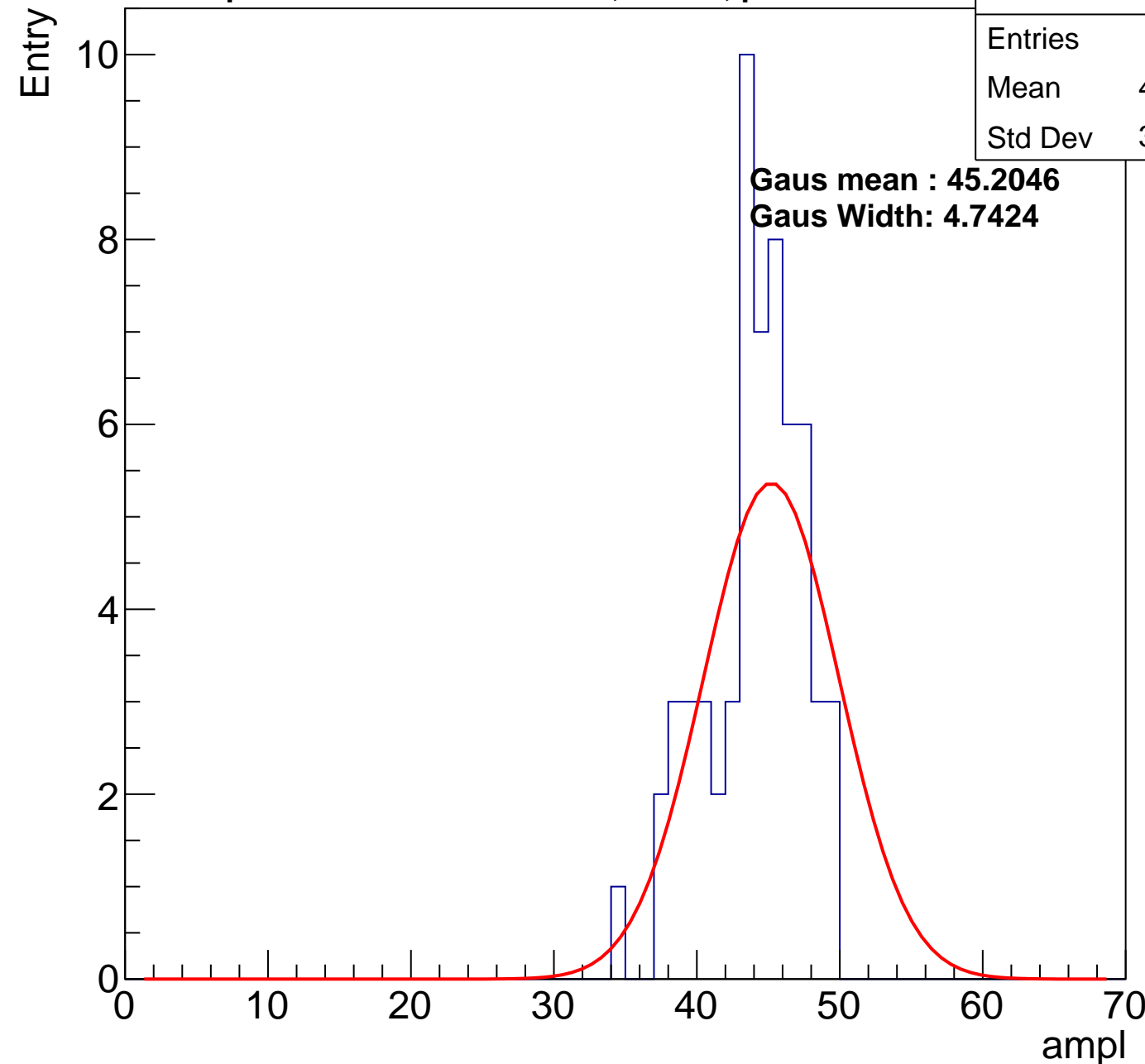
40

50

60

70

ampl

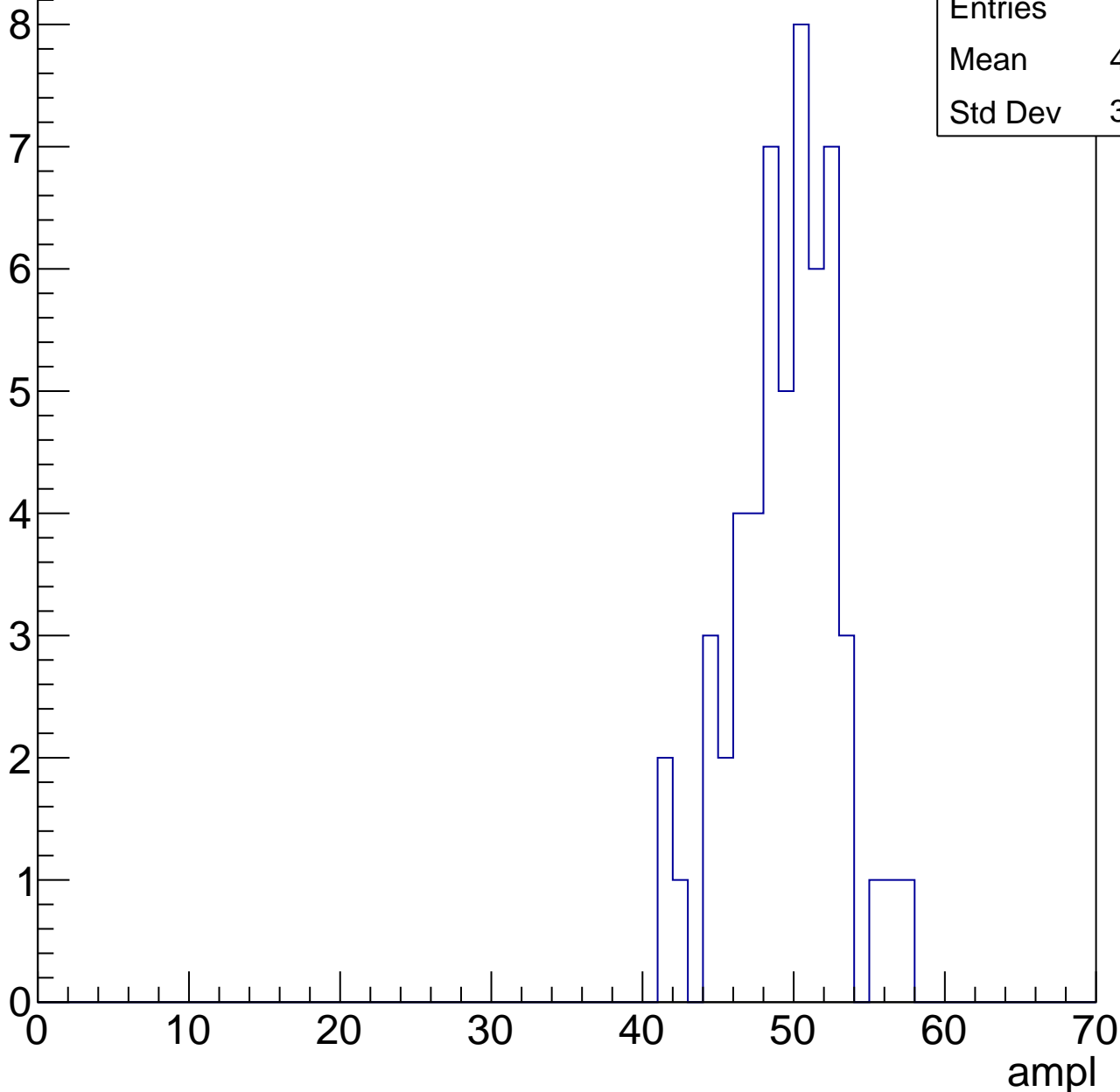


# B1L003S, U6-ch31, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	49.02
Std Dev	3.398



# B1L003S, U6-ch31, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

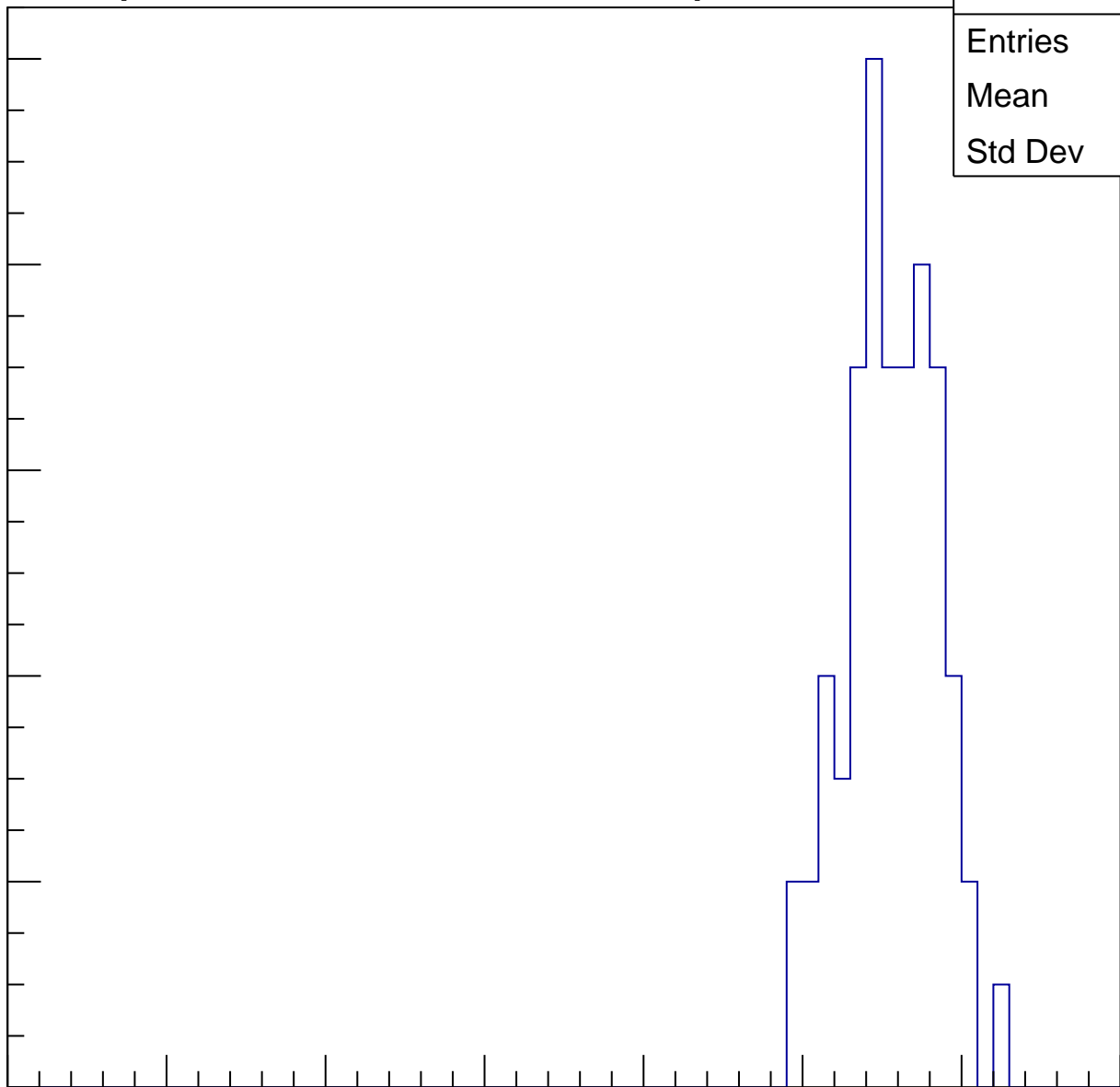
Entries	64
Mean	55.09
Std Dev	2.838

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

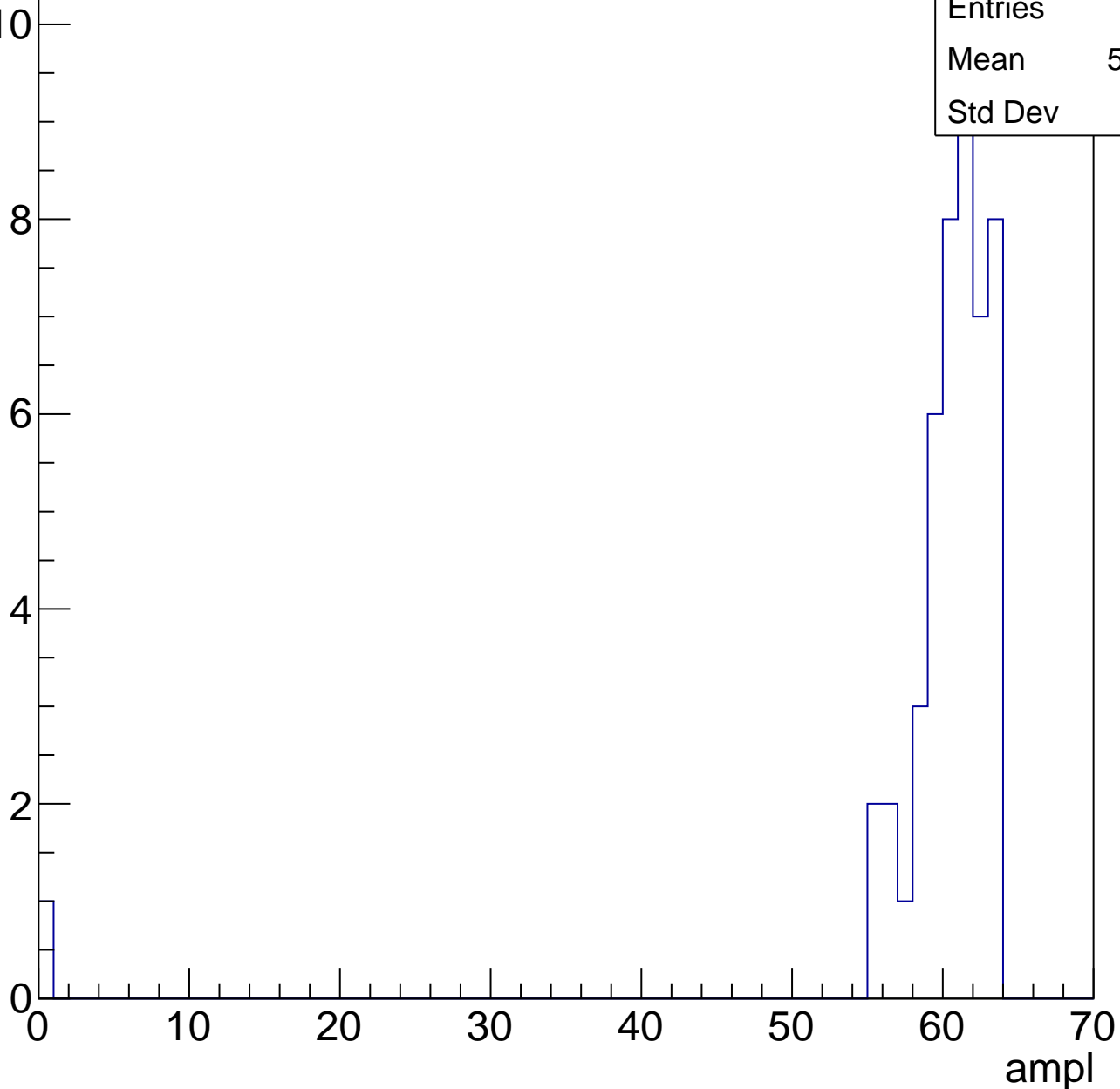


# B1L003S, U6-ch31, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	48
Mean	59.06
Std Dev	8.87



# B1L003S, U6-ch31, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

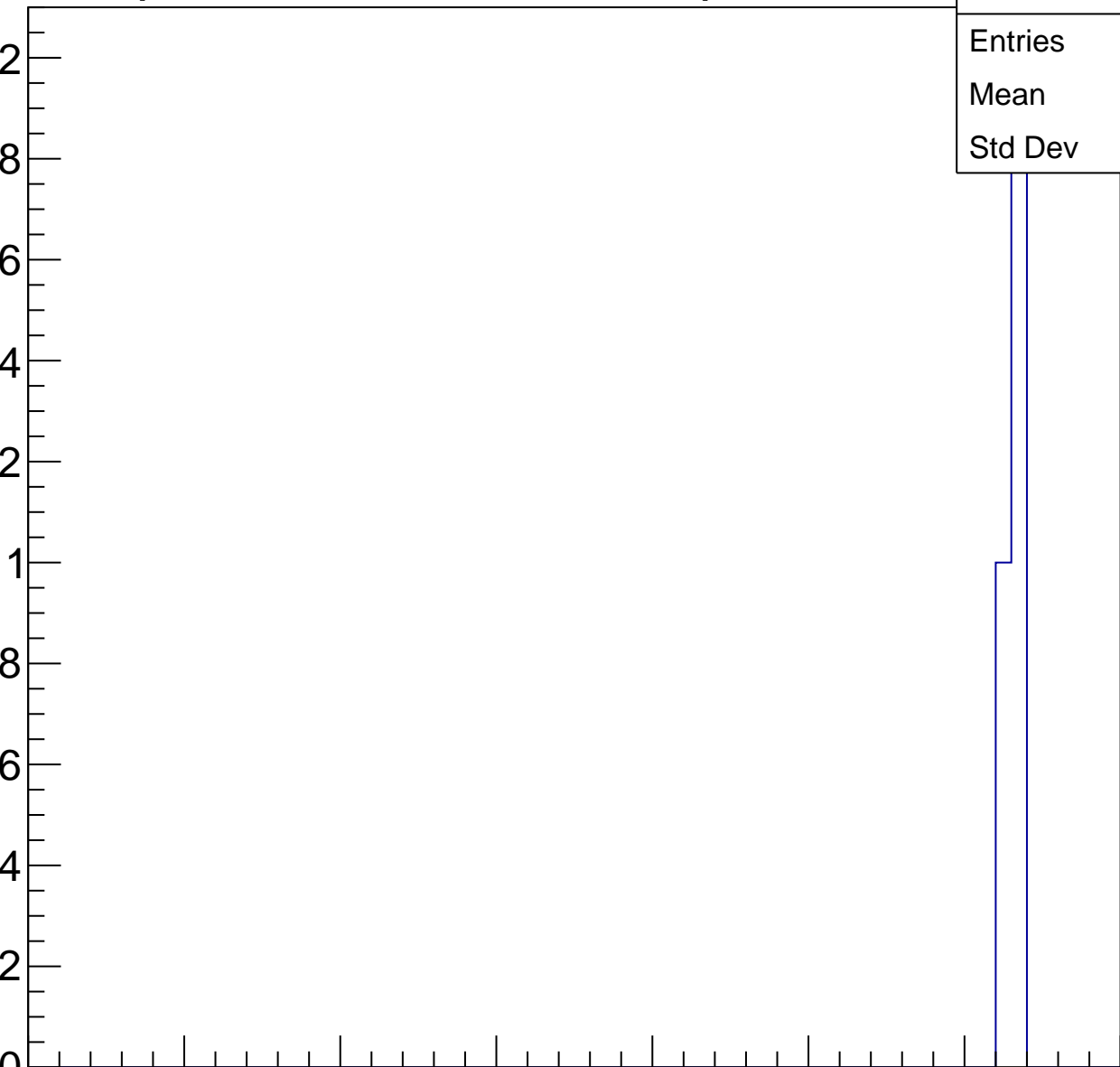
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.67
Std Dev	0.4714

0 10 20 30 40 50 60 70

ampl





# B1L003S, U6-ch31, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	3
Mean	20.67
Std Dev	29.23

# B1L003S, U6-ch32, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	62
Mean	30.06
Std Dev	2.85

**Gaus mean : 29.7922**

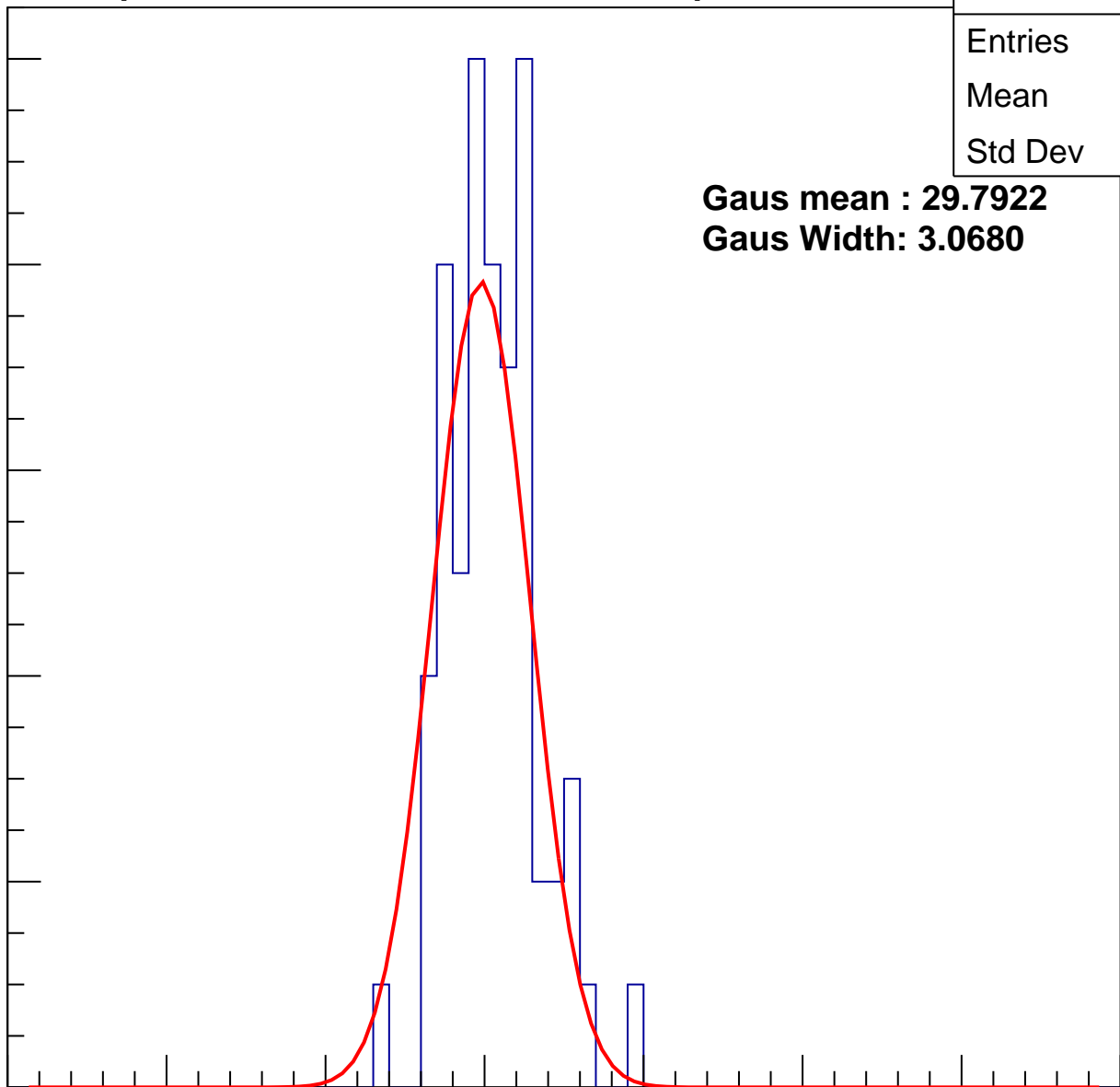
**Gaus Width: 3.0680**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U6-ch32, adc1

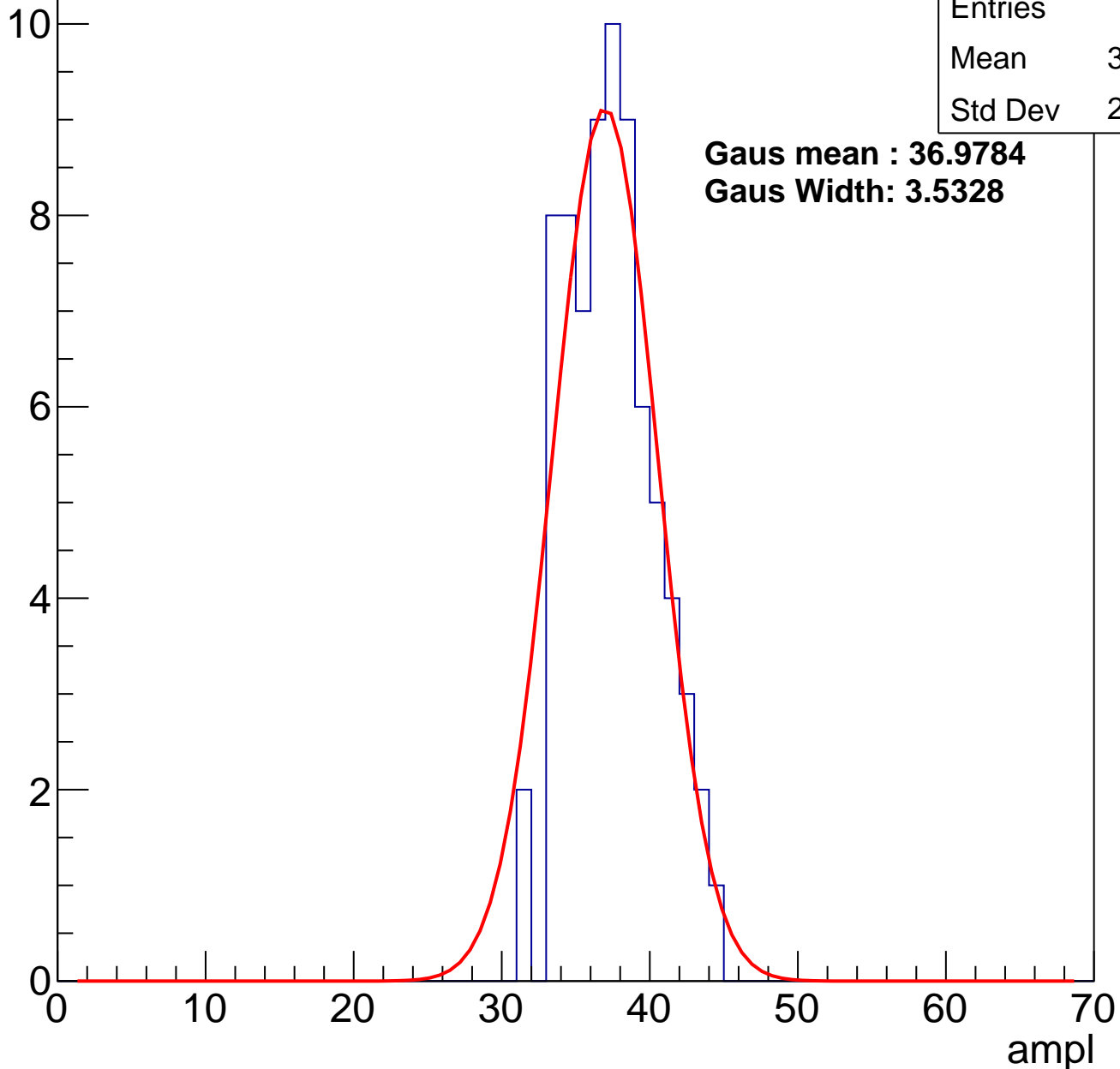
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	74
Mean	36.93
Std Dev	2.956

**Gaus mean : 36.9784**

**Gaus Width: 3.5328**

Entry



# B1L003S, U6-ch32, adc2

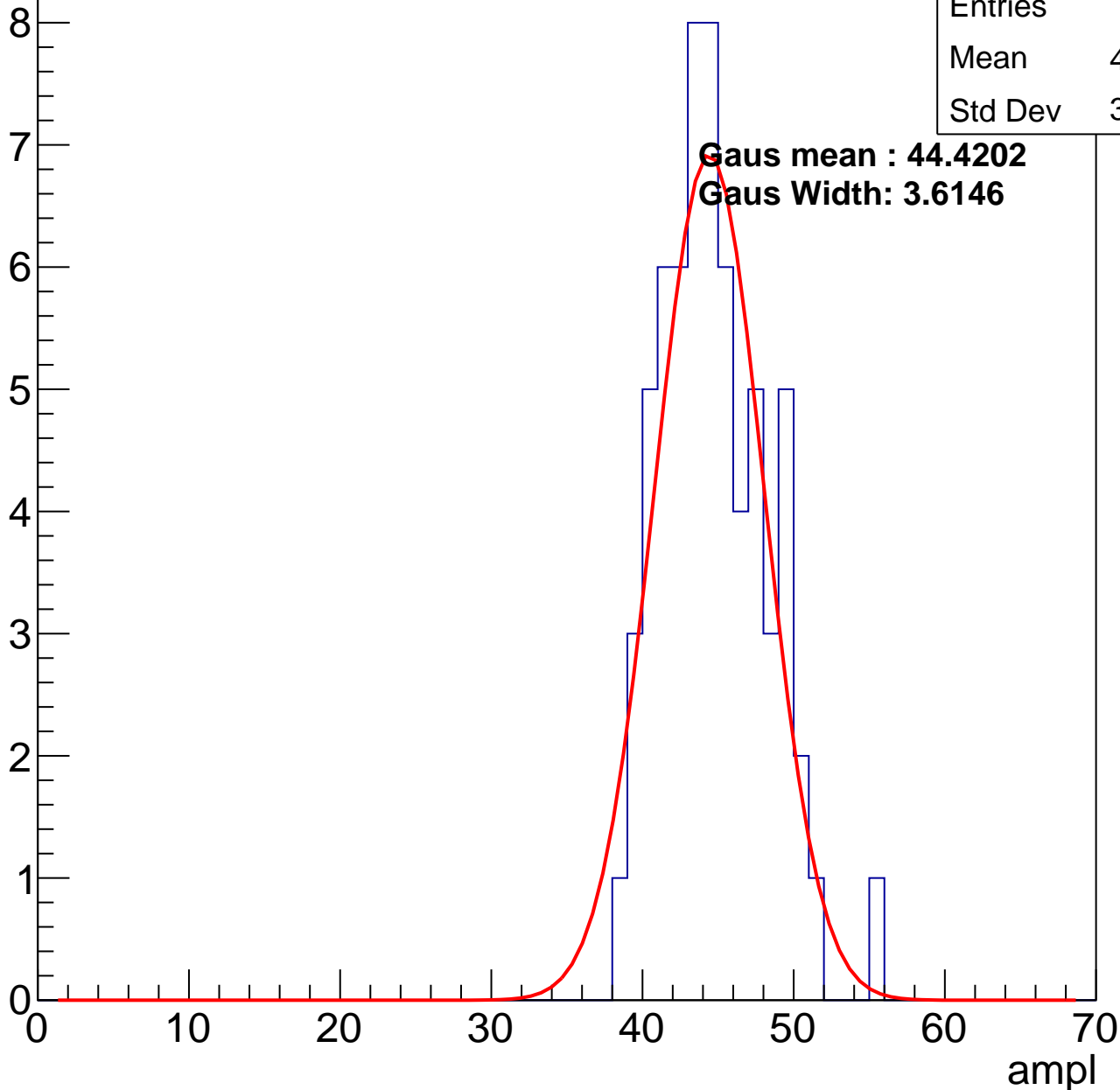
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	44.27
Std Dev	3.433

**Gaus mean : 44.4202**

**Gaus Width: 3.6146**

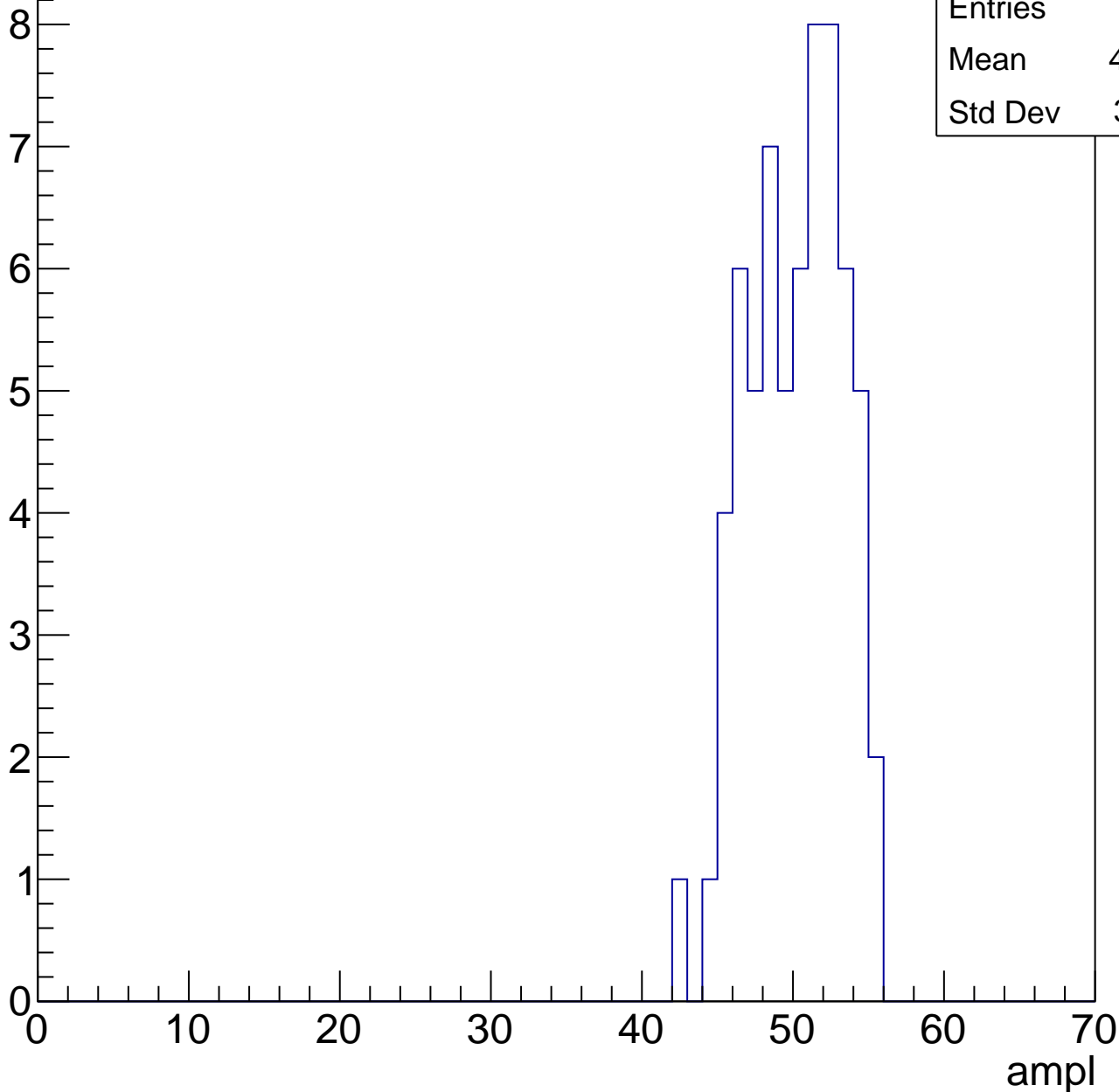


# B1L003S, U6-ch32, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

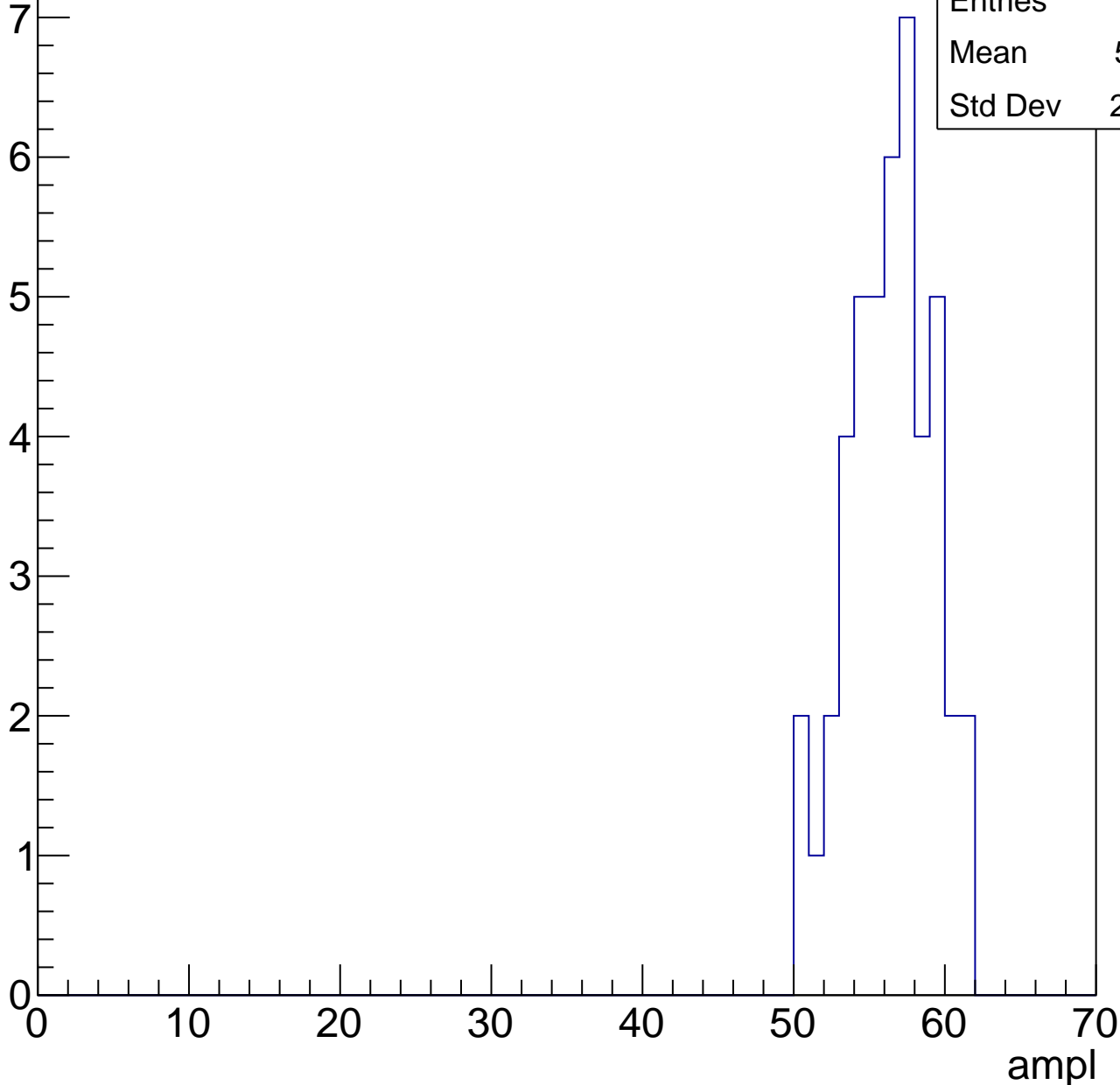
Entries	64
Mean	49.69
Std Dev	3.041



# B1L003S, U6-ch32, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



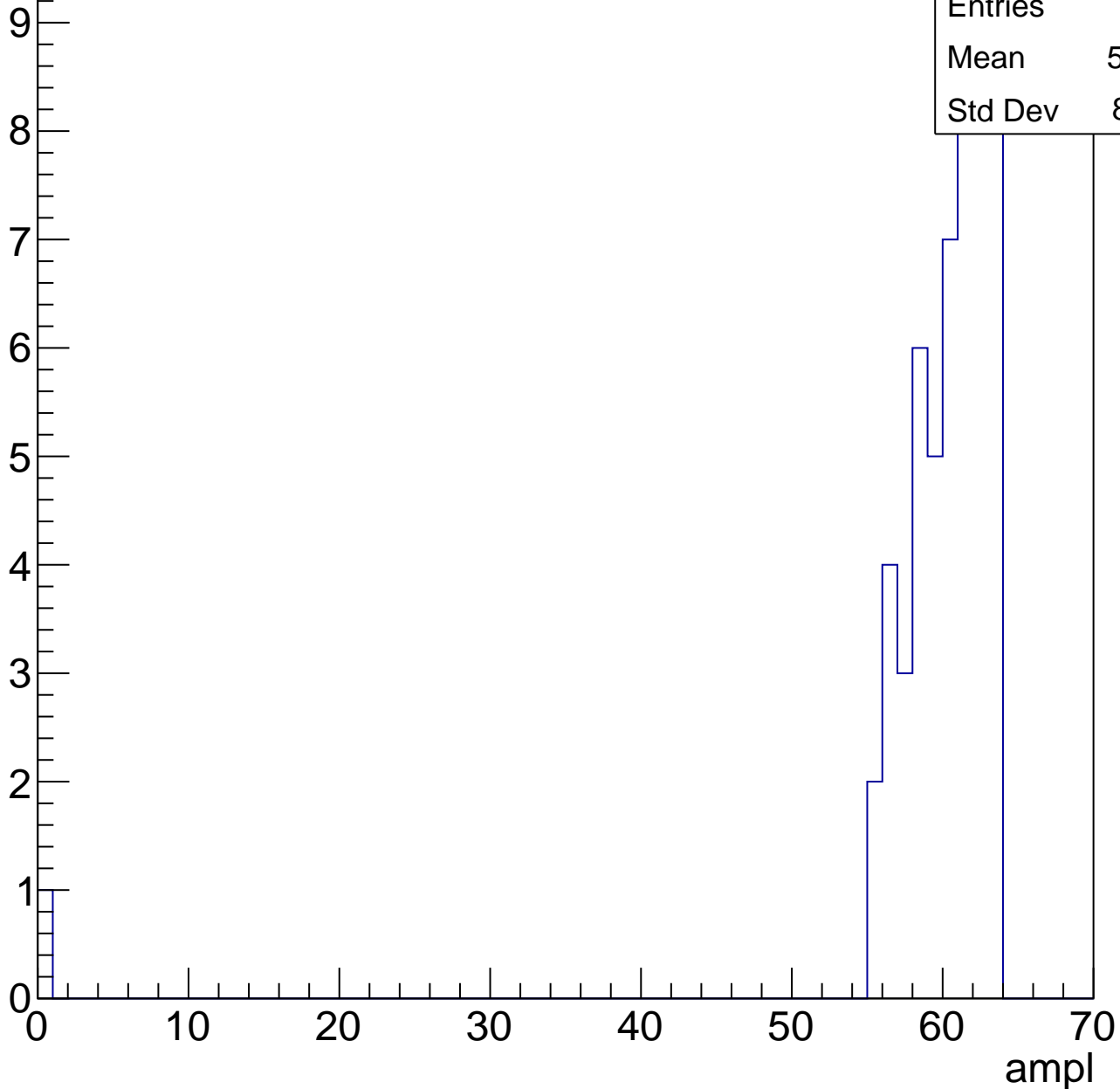
Entries	45
Mean	55.91
Std Dev	2.747

# B1L003S, U6-ch32, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	58.85
Std Dev	8.491



# B1L003S, U6-ch32, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

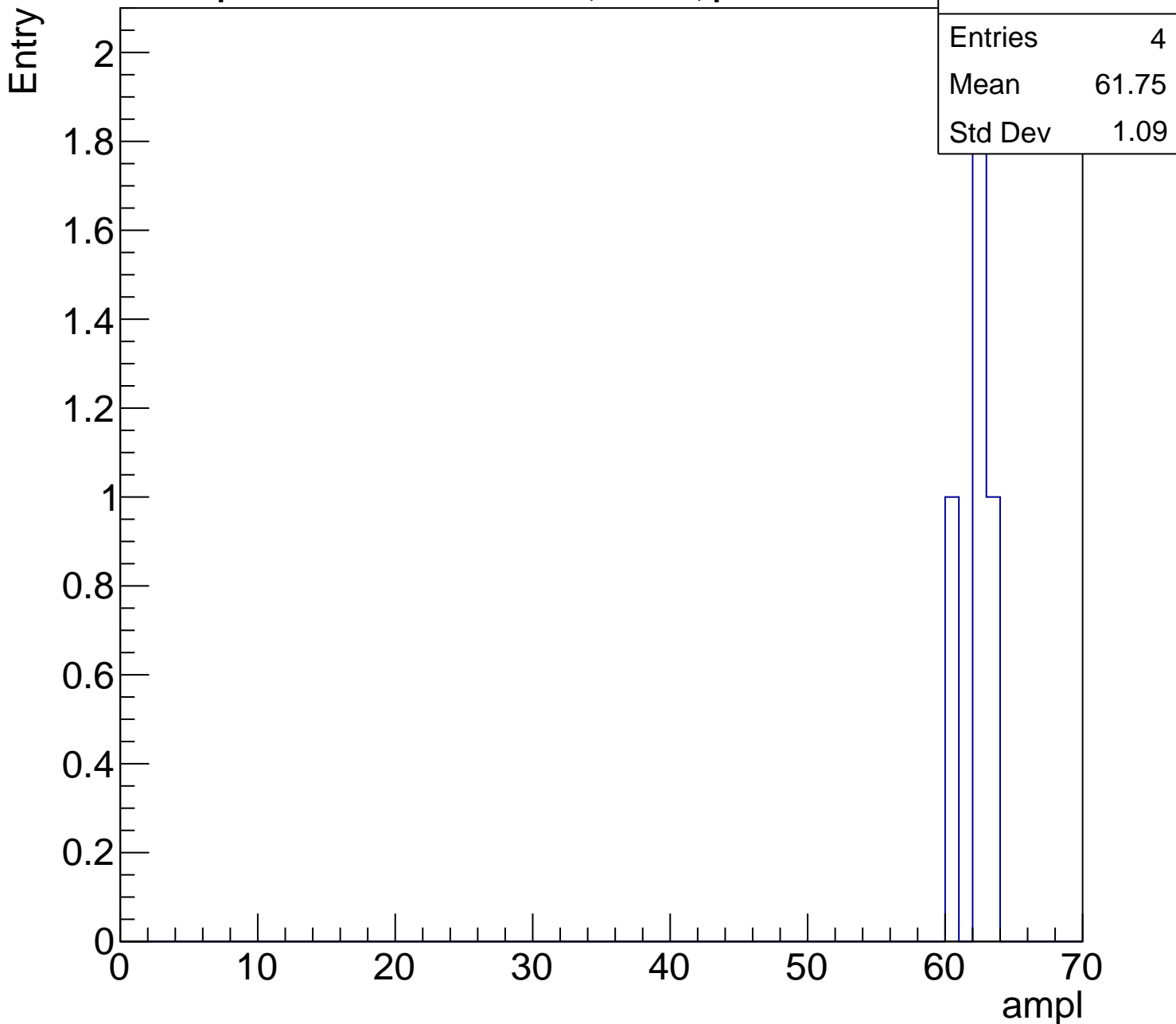
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	61.75
Std Dev	1.09

0 10 20 30 40 50 60 70

ampl





# B1L003S, U6-ch32, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch33, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	74
Mean	31.03
Std Dev	3.238

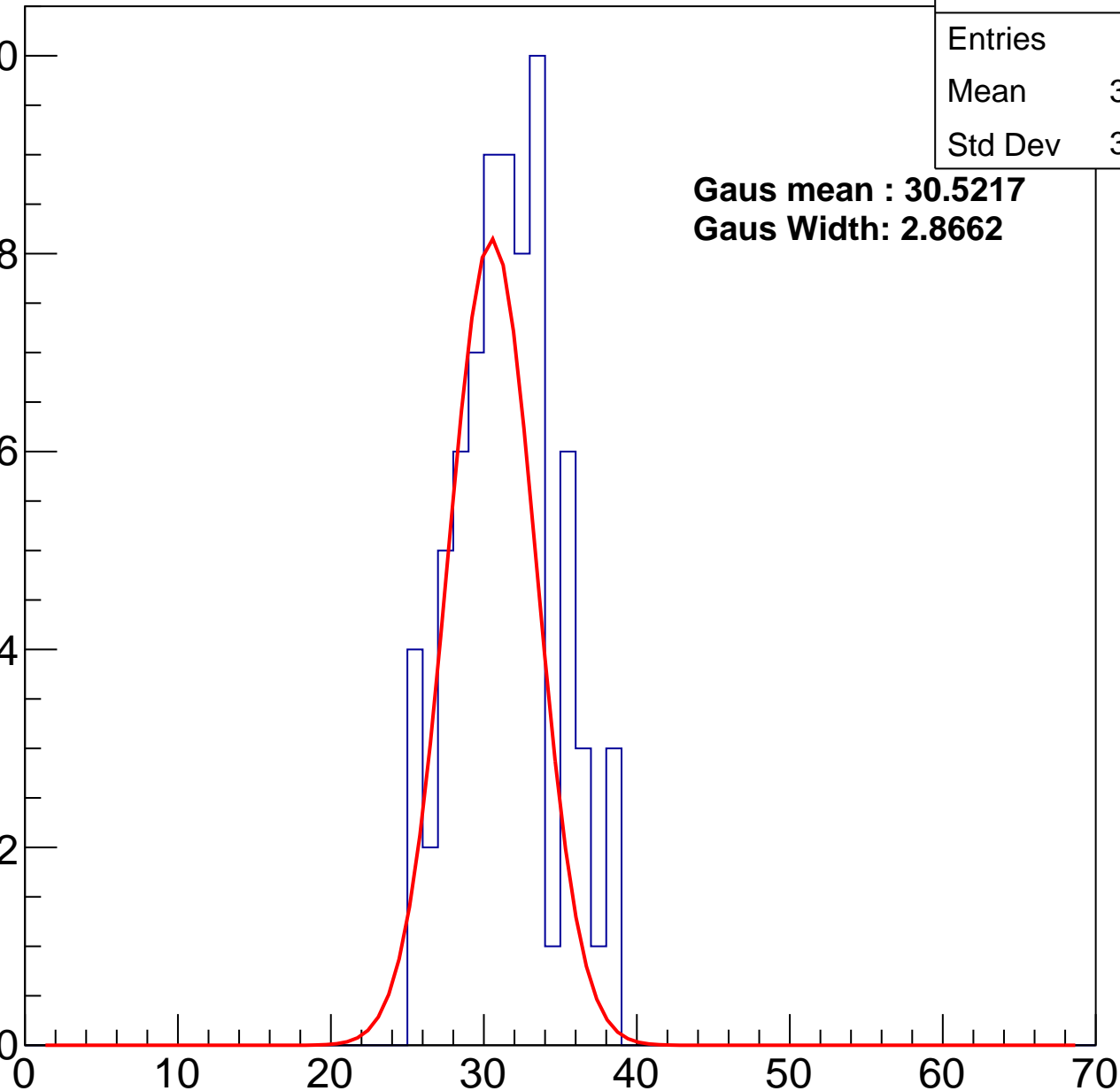
**Gaus mean : 30.5217**

**Gaus Width: 2.8662**

Entry

10  
8  
6  
4  
2  
0

ampl



# B1L003S, U6-ch33, adc1

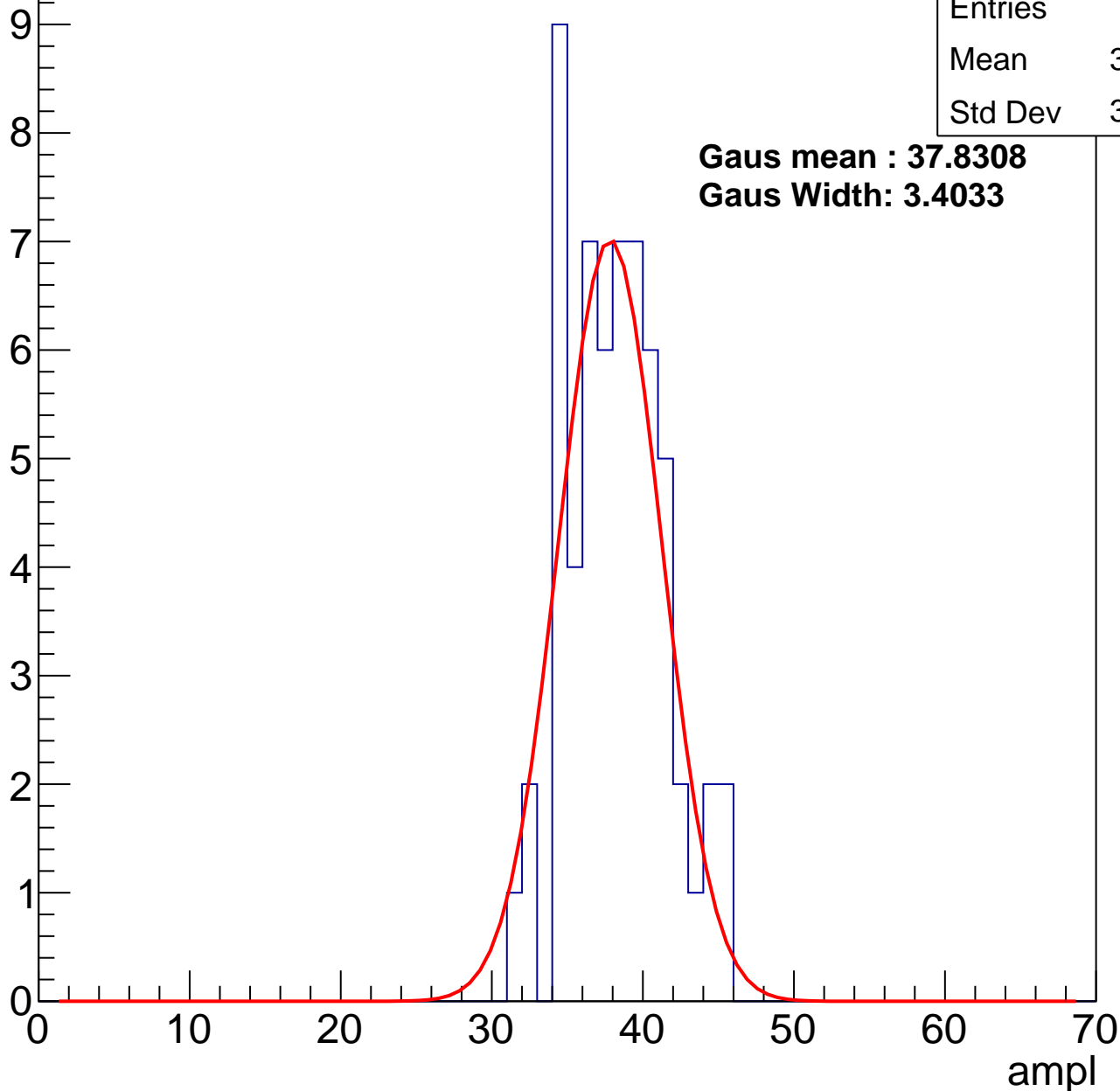
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	37.77
Std Dev	3.226

**Gaus mean : 37.8308**

**Gaus Width: 3.4033**



# B1L003S, U6-ch33, adc2

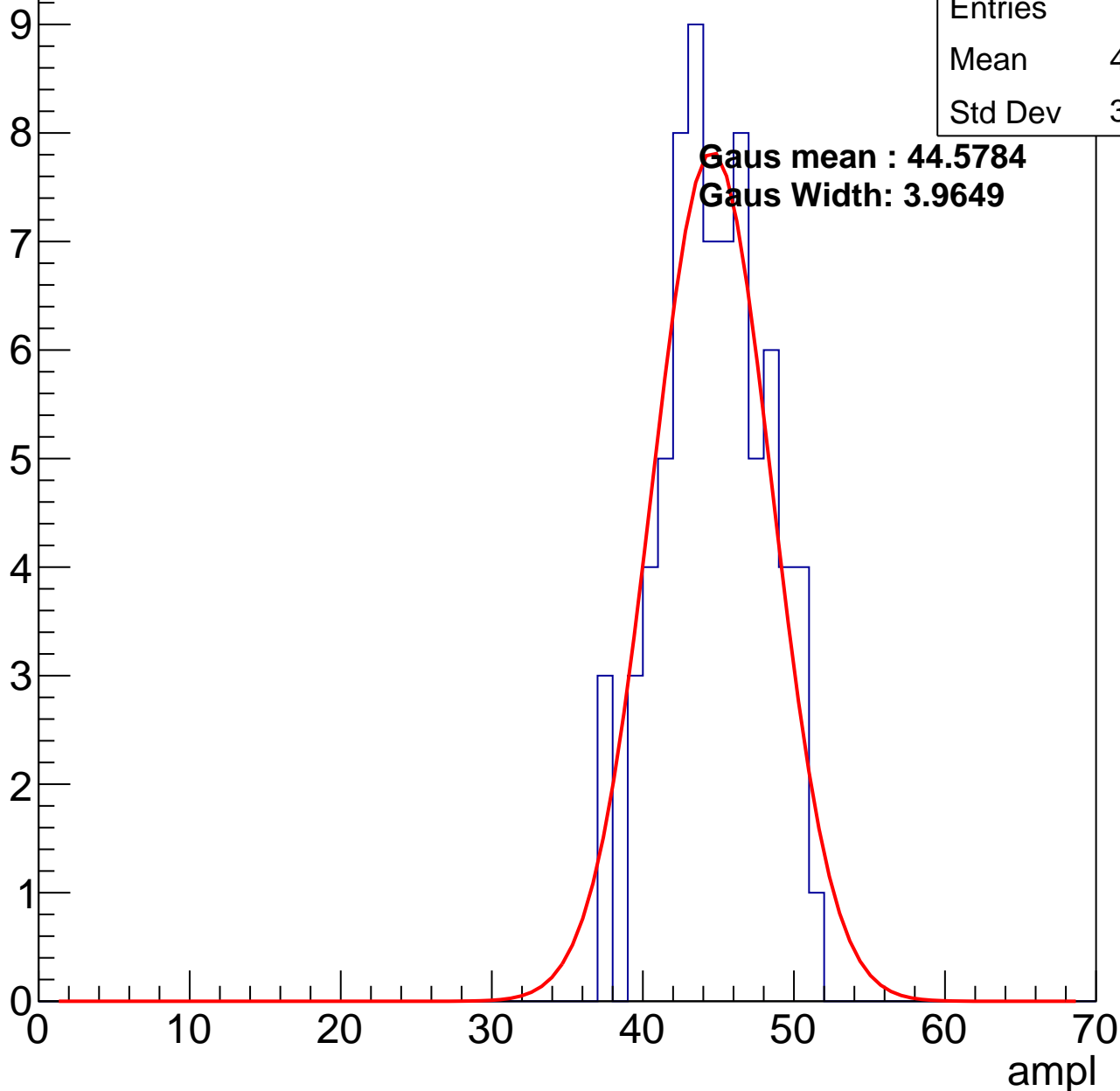
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	74
Mean	44.28
Std Dev	3.367

**Gaus mean : 44.5784**

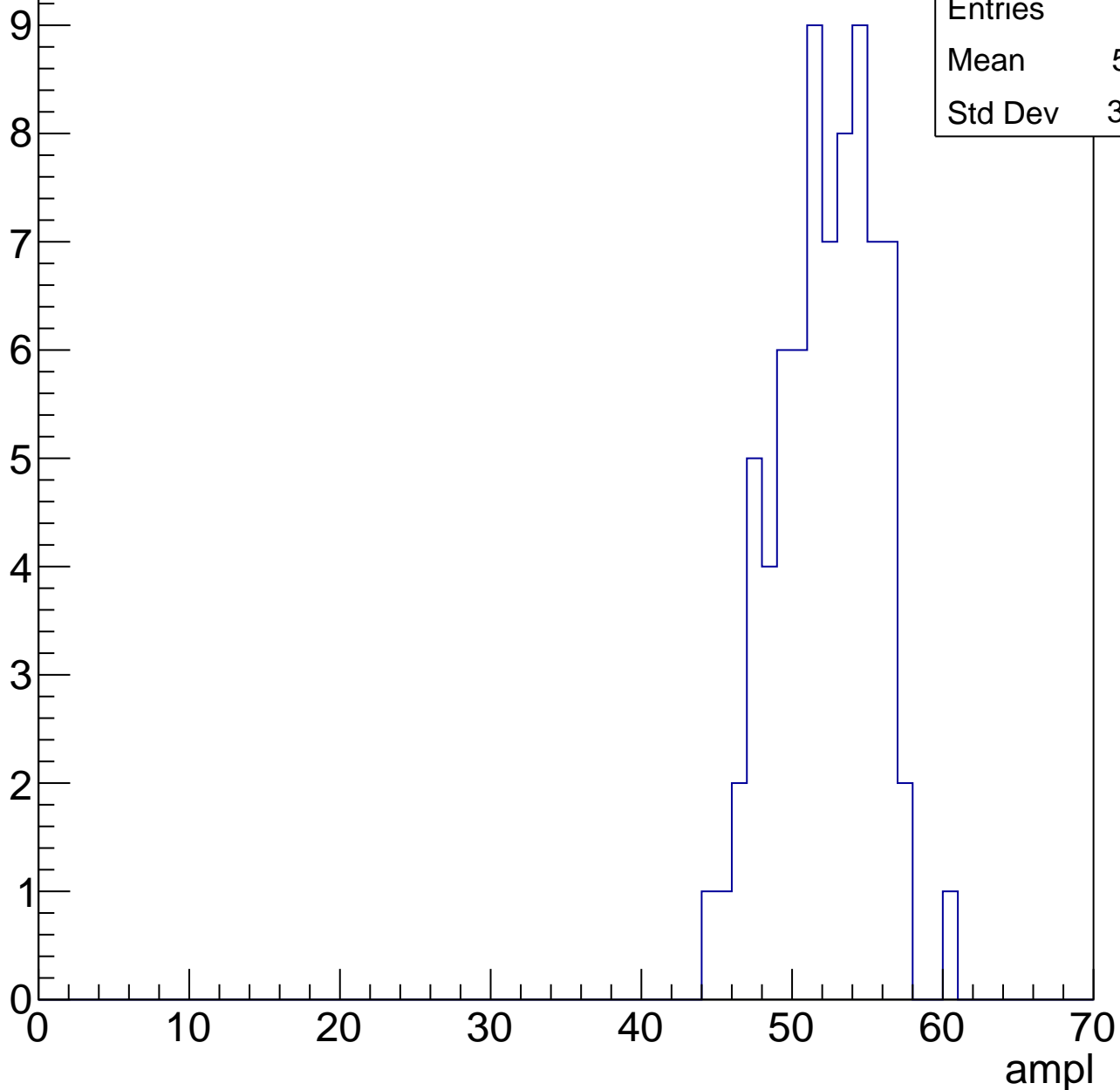
**Gaus Width: 3.9649**



# B1L003S, U6-ch33, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

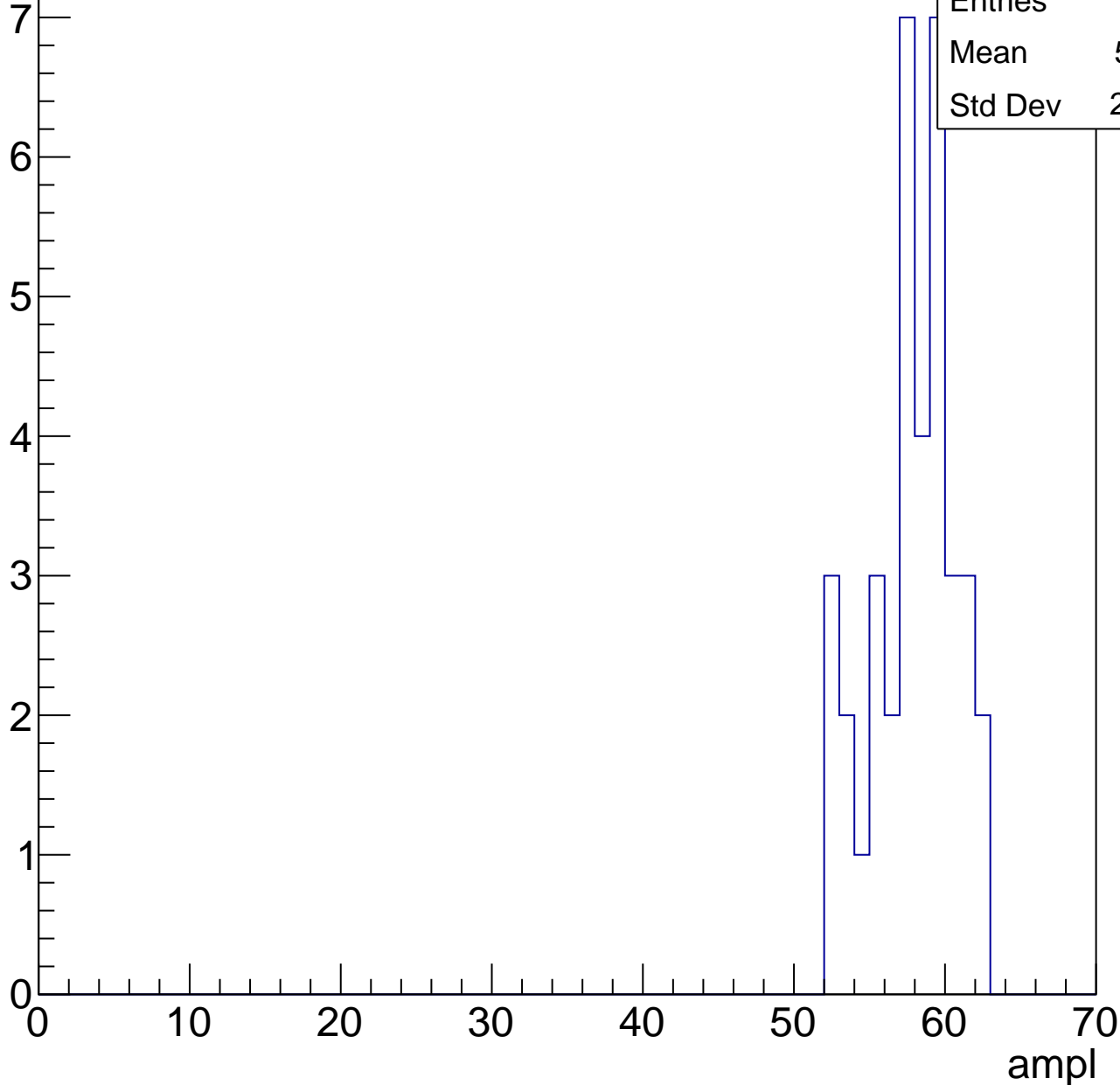


Entries	75
Mean	51.81
Std Dev	3.248

# B1L003S, U6-ch33, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

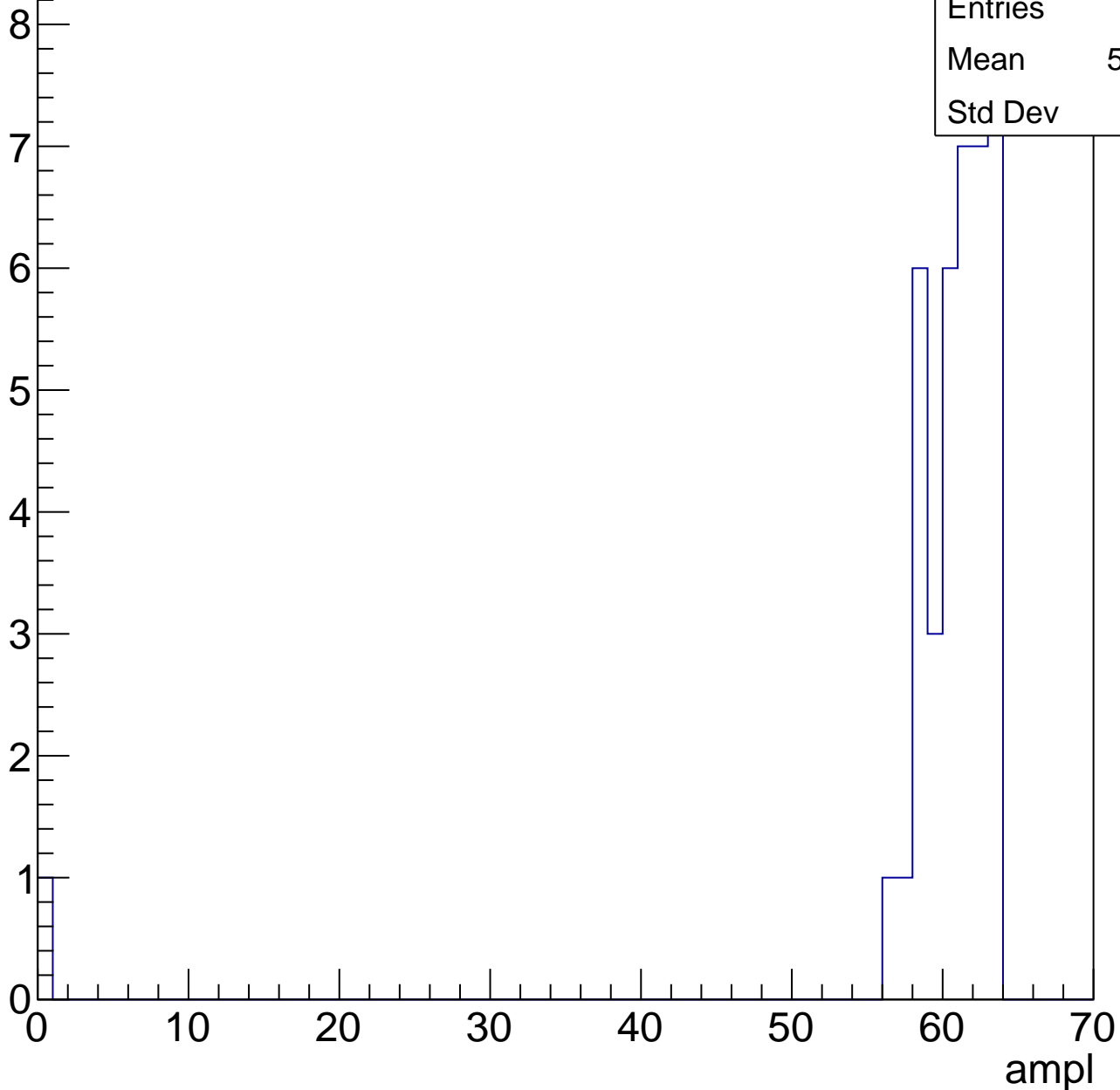


# B1L003S, U6-ch33, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	40
Mean	59.08
Std Dev	9.65



# B1L003S, U6-ch33, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

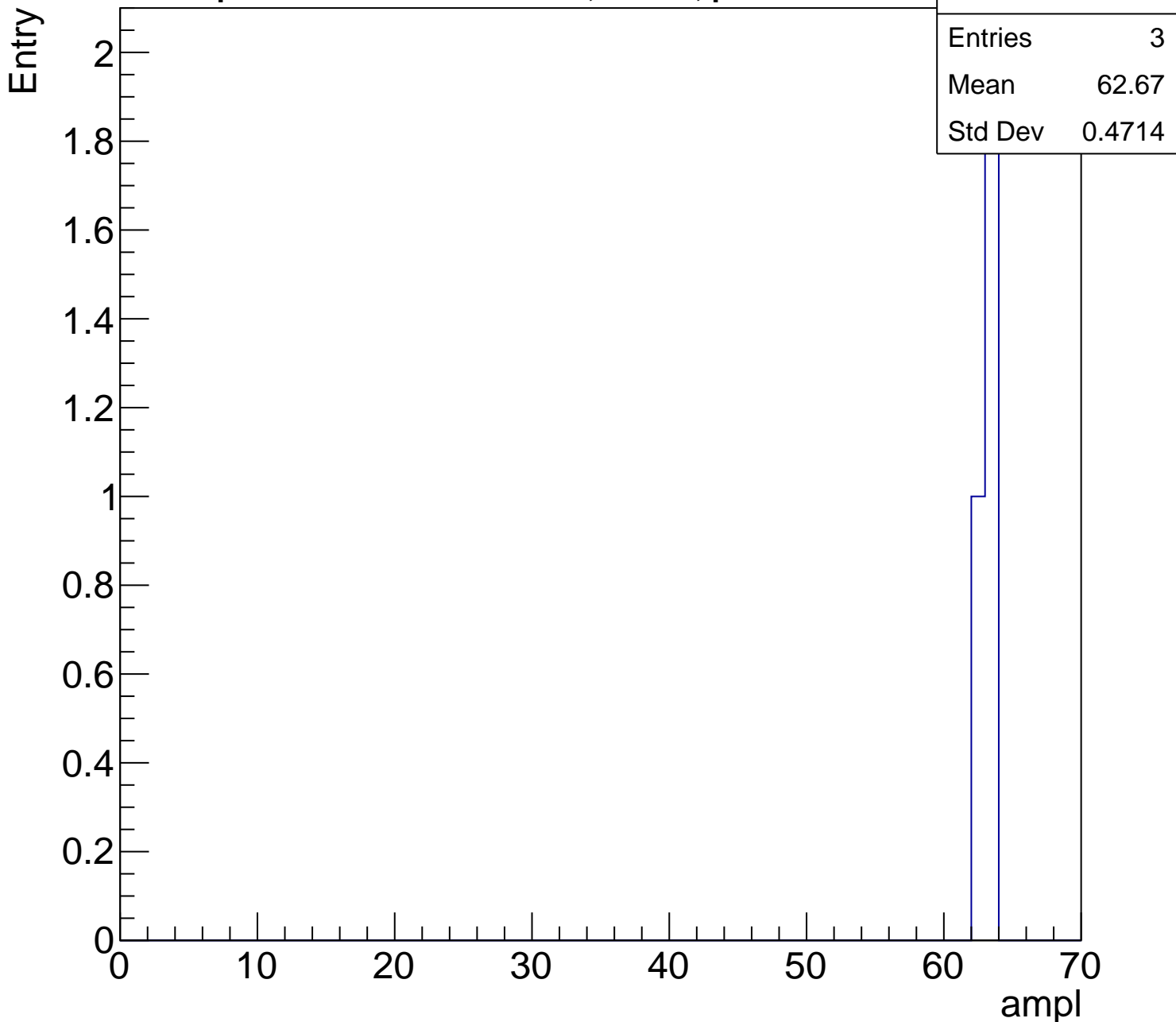
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.67
Std Dev	0.4714

0 10 20 30 40 50 60 70

ampl





# B1L003S, U6-ch33, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch34, adc0

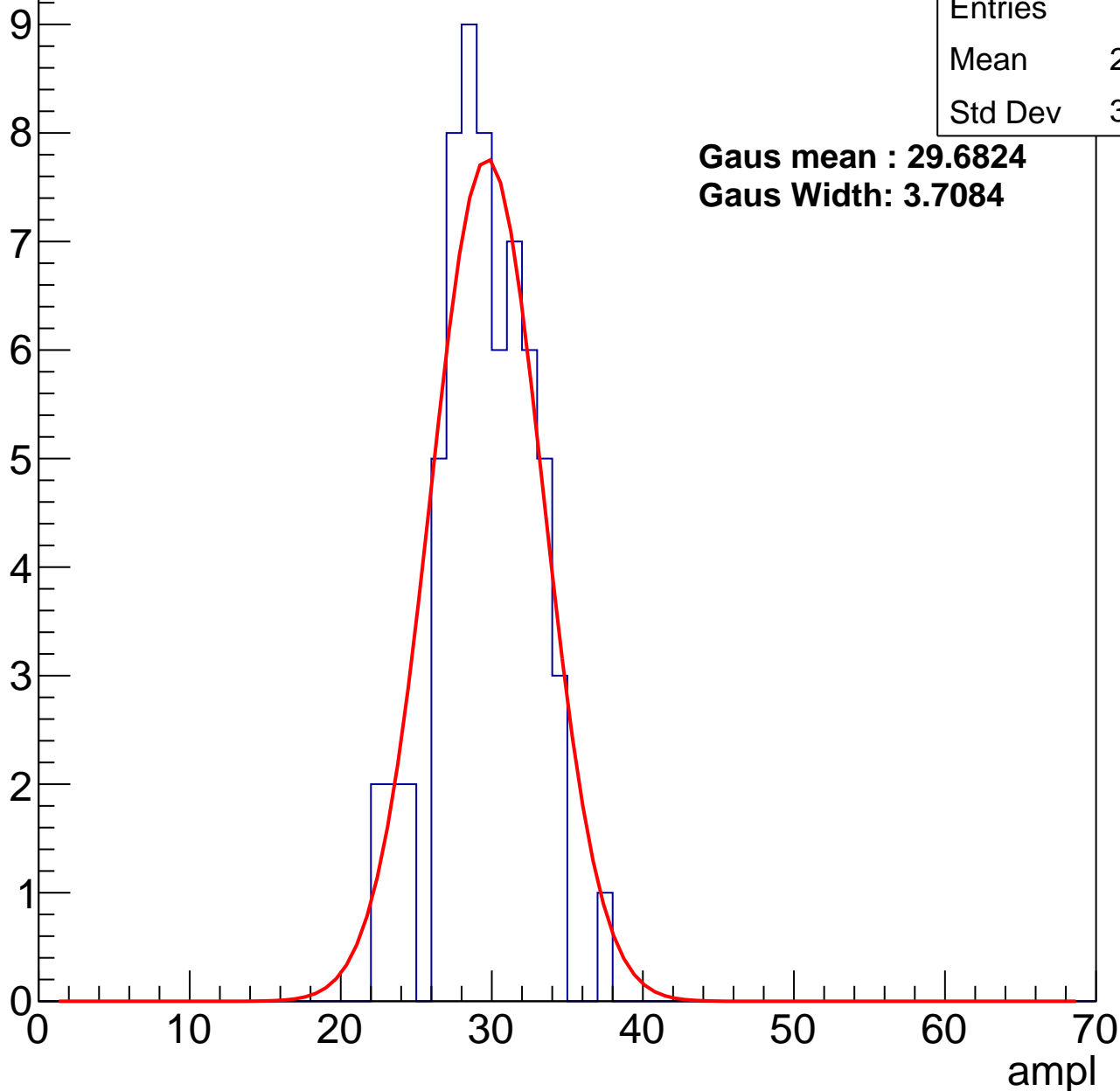
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	29.08
Std Dev	3.094

**Gaus mean : 29.6824**

**Gaus Width: 3.7084**



# B1L003S, U6-ch34, adc1

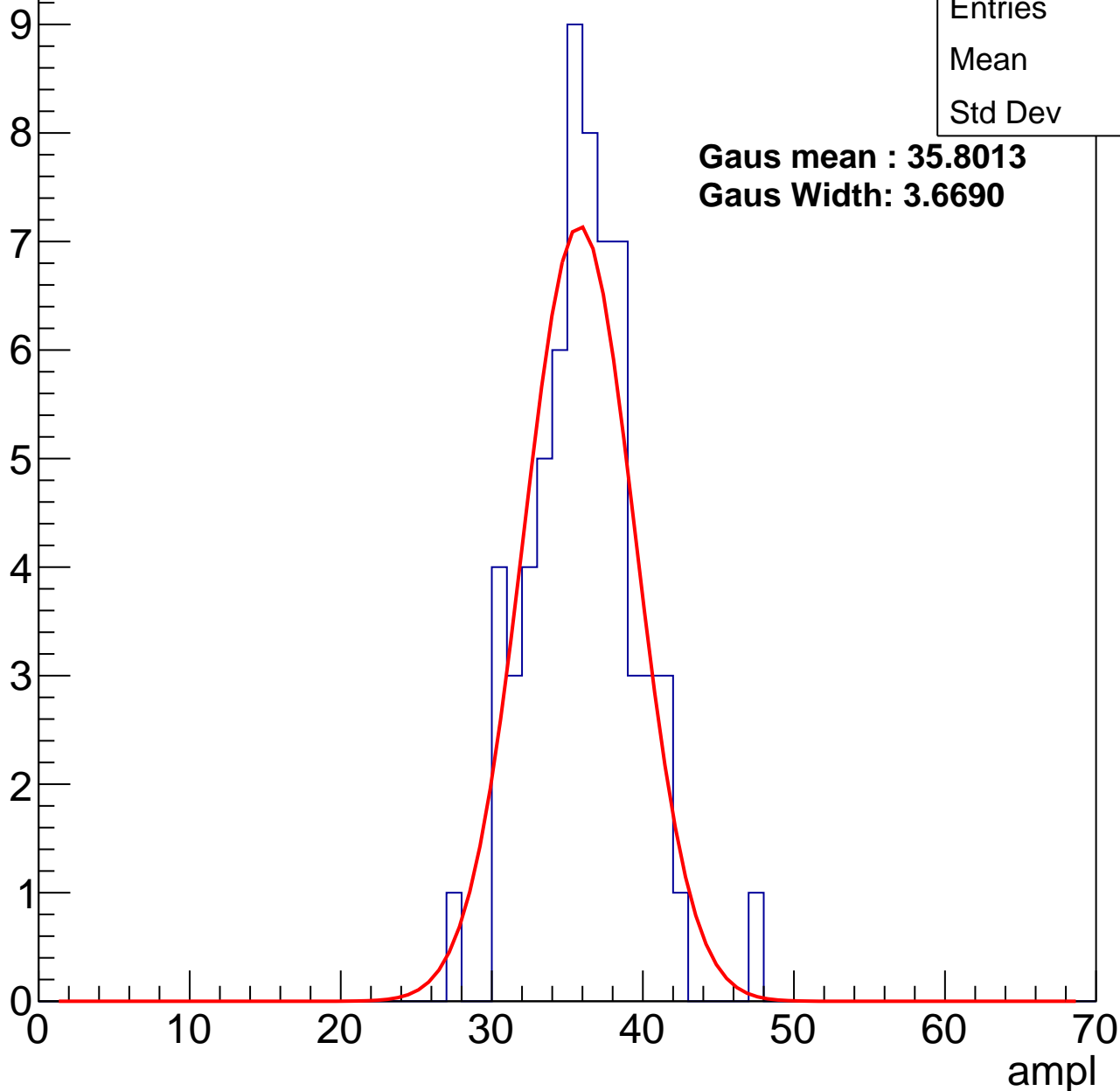
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	35.6
Std Dev	3.45

**Gaus mean : 35.8013**

**Gaus Width: 3.6690**



# B1L003S, U6-ch34, adc2

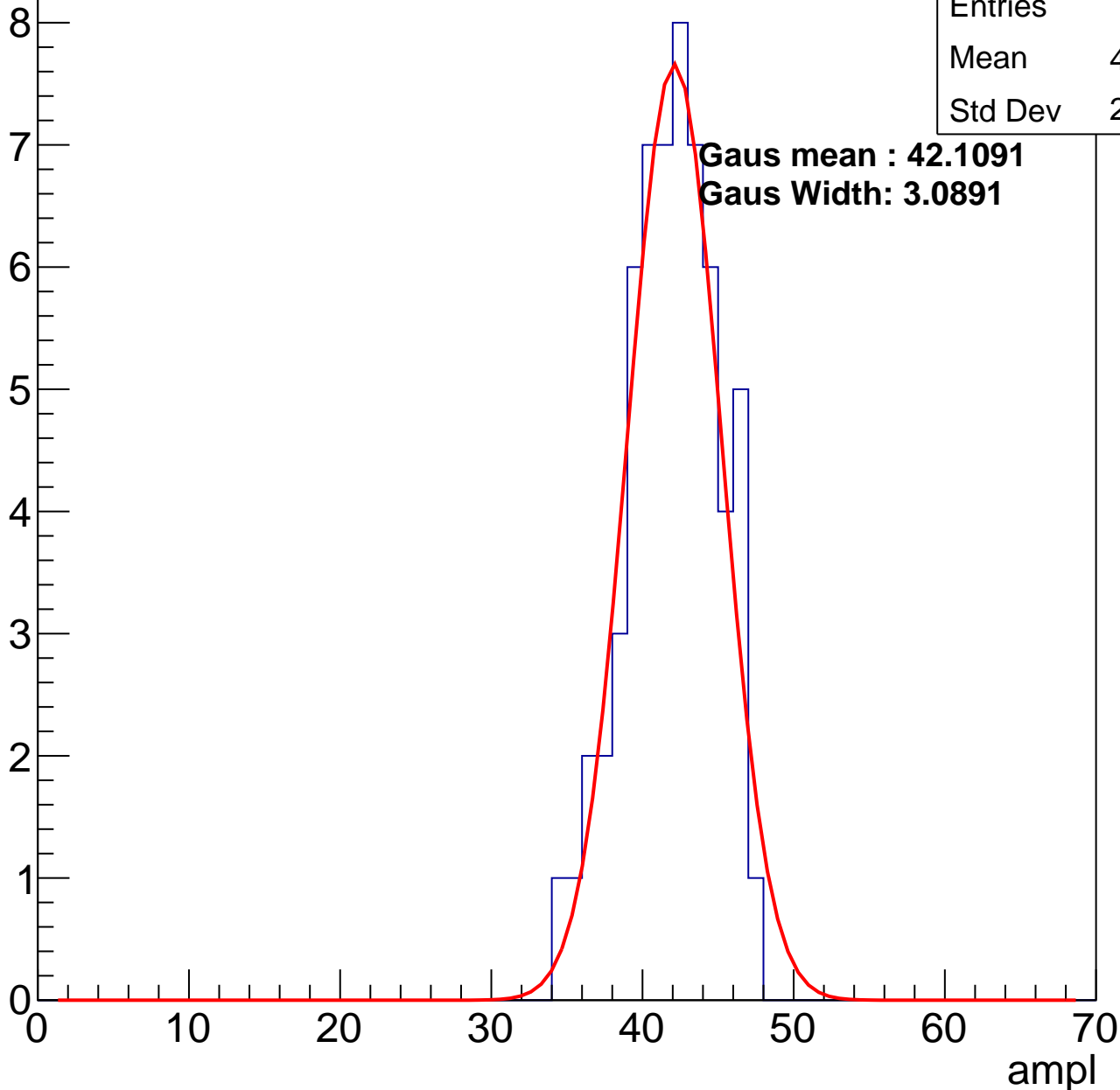
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	41.47
Std Dev	2.963

**Gaus mean : 42.1091**

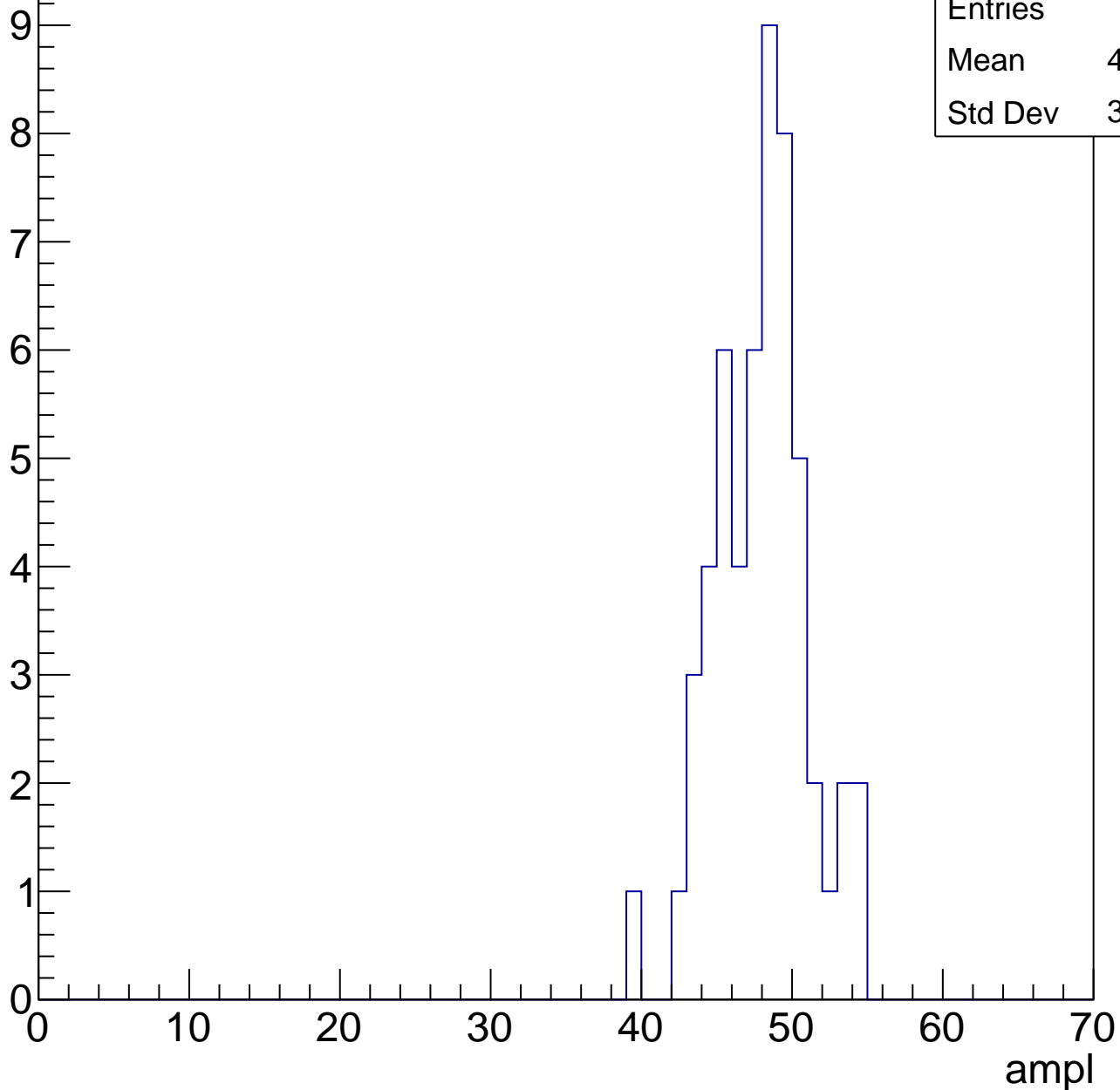
**Gaus Width: 3.0891**



# B1L003S, U6-ch34, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

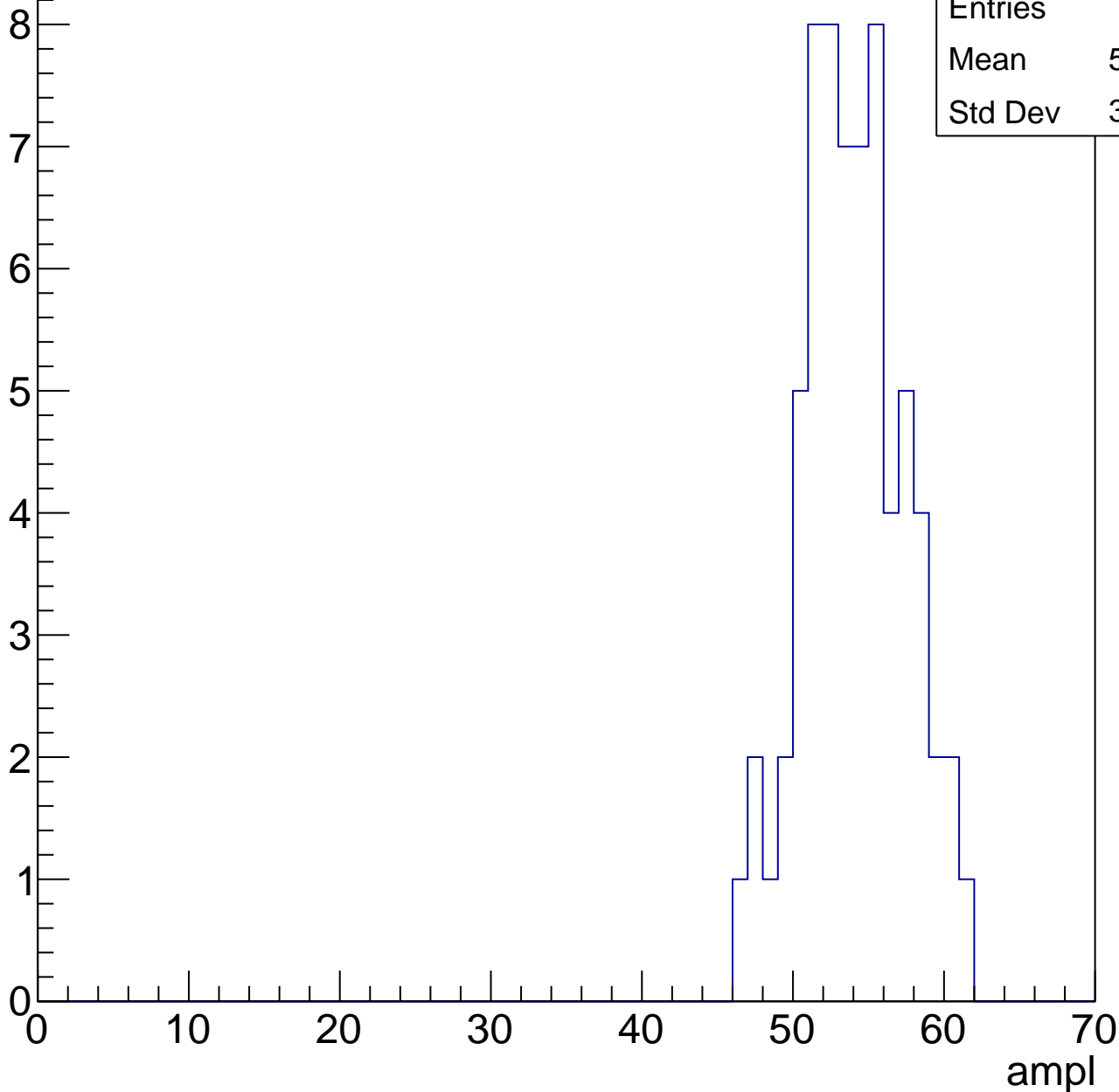


# B1L003S, U6-ch34, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	53.57
Std Dev	3.302



# B1L003S, U6-ch34, adc5

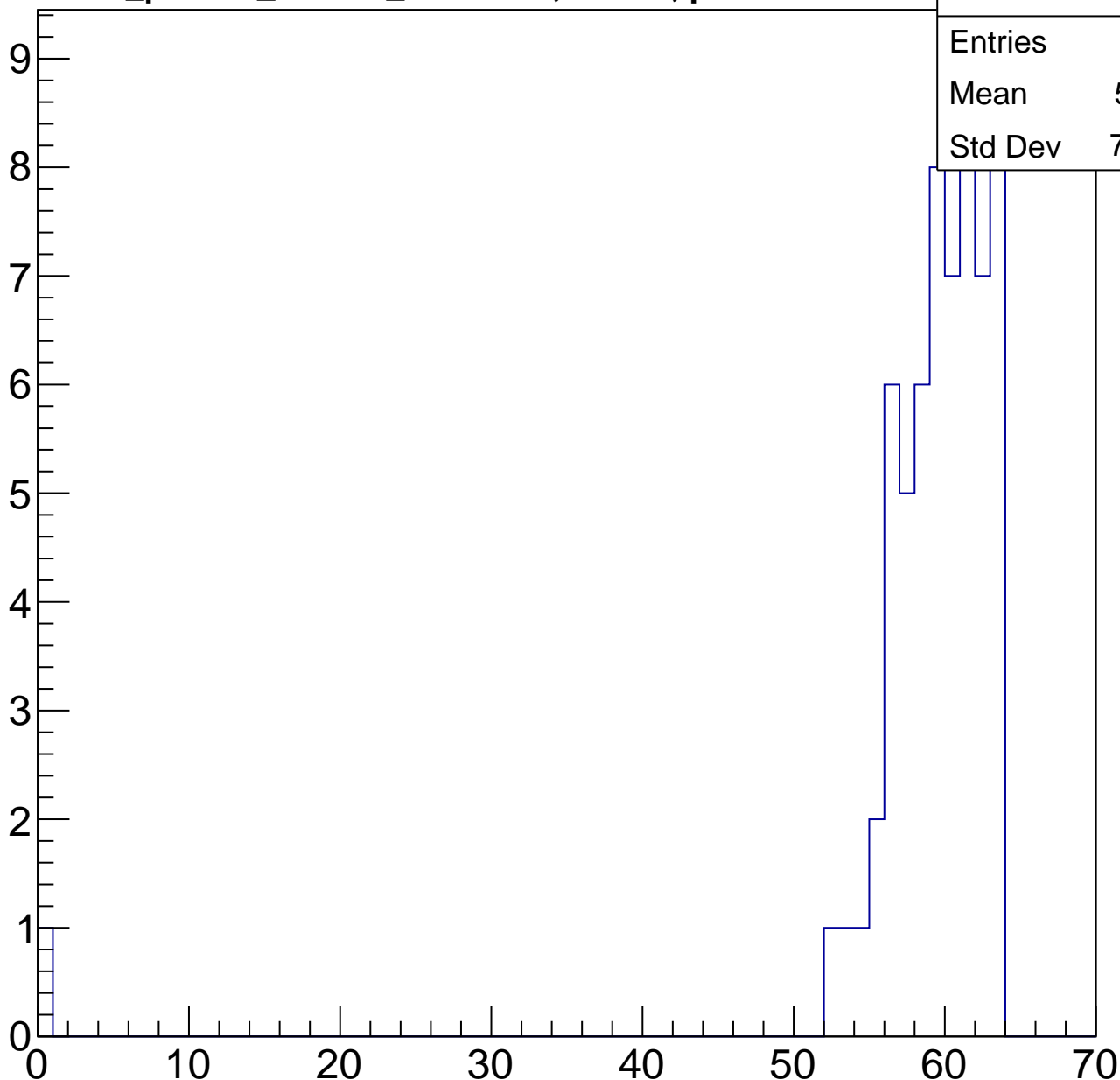
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	63
Mean	58.41
Std Dev	7.899

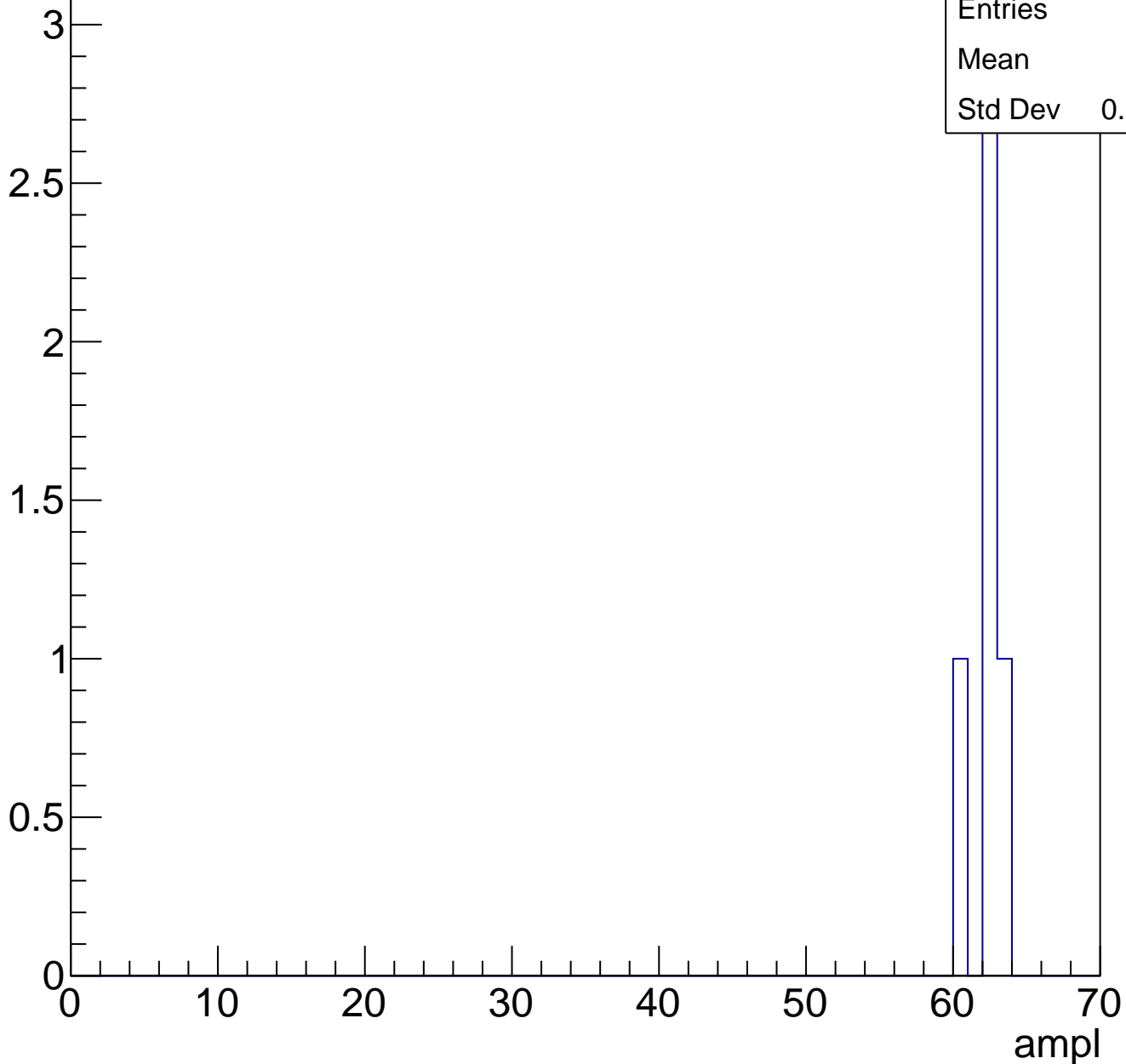
ampl



# B1L003S, U6-ch34, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch34, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U6-ch35, adc0

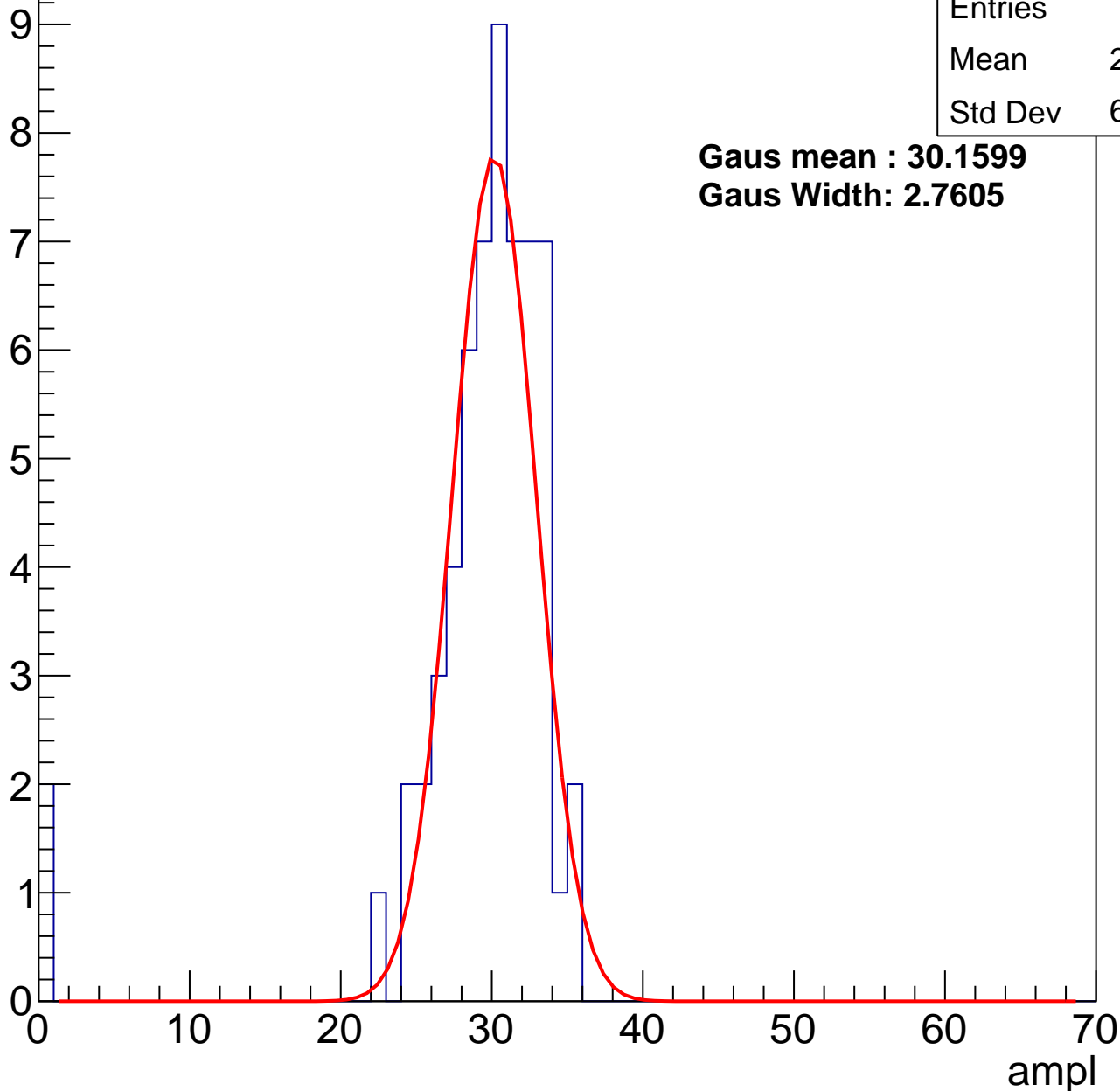
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	28.72
Std Dev	6.009

**Gaus mean : 30.1599**

**Gaus Width: 2.7605**



# B1L003S, U6-ch35, adc1

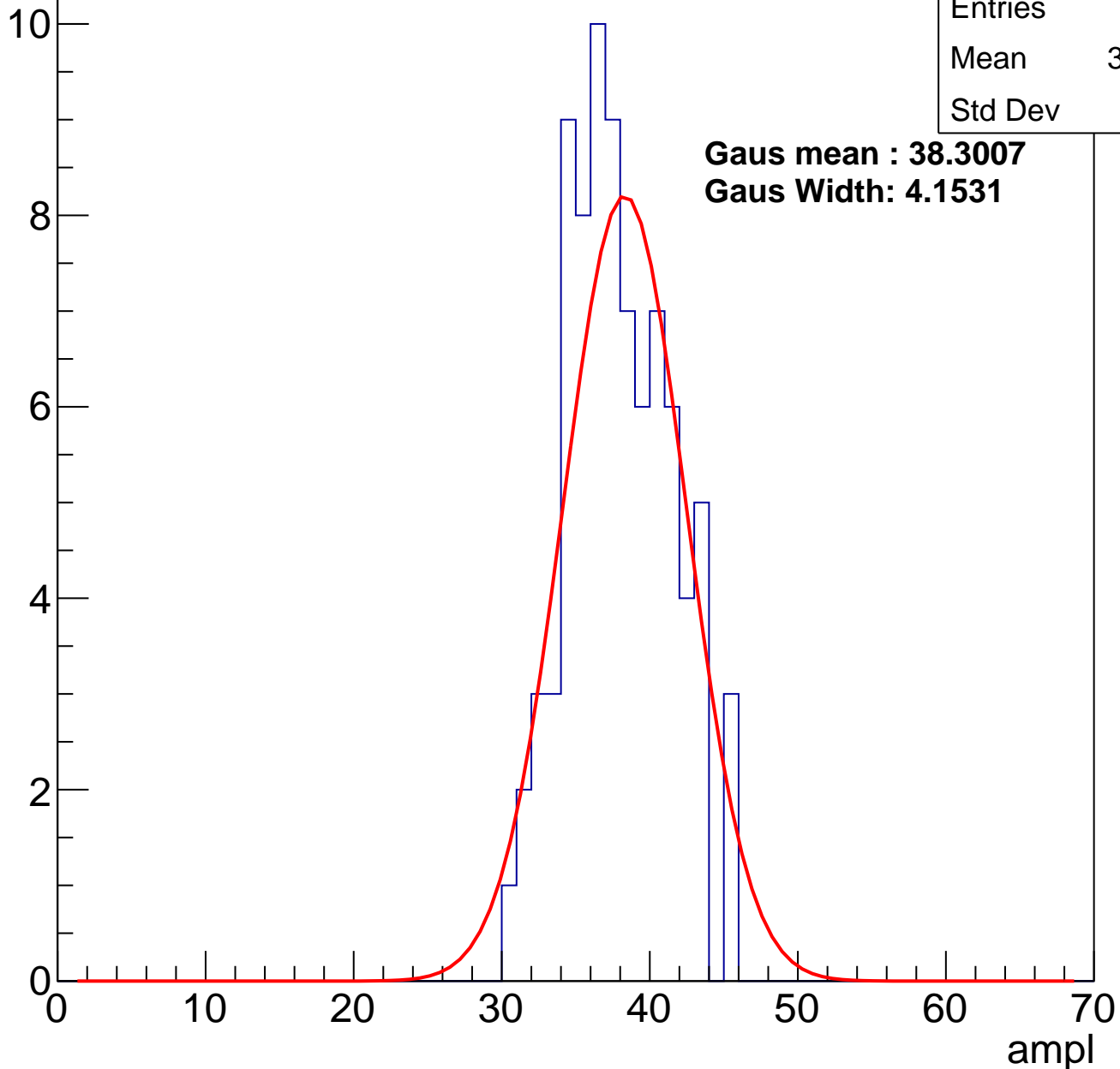
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	83
Mean	37.47
Std Dev	3.49

**Gaus mean : 38.3007**

**Gaus Width: 4.1531**

Entry



# B1L003S, U6-ch35, adc2

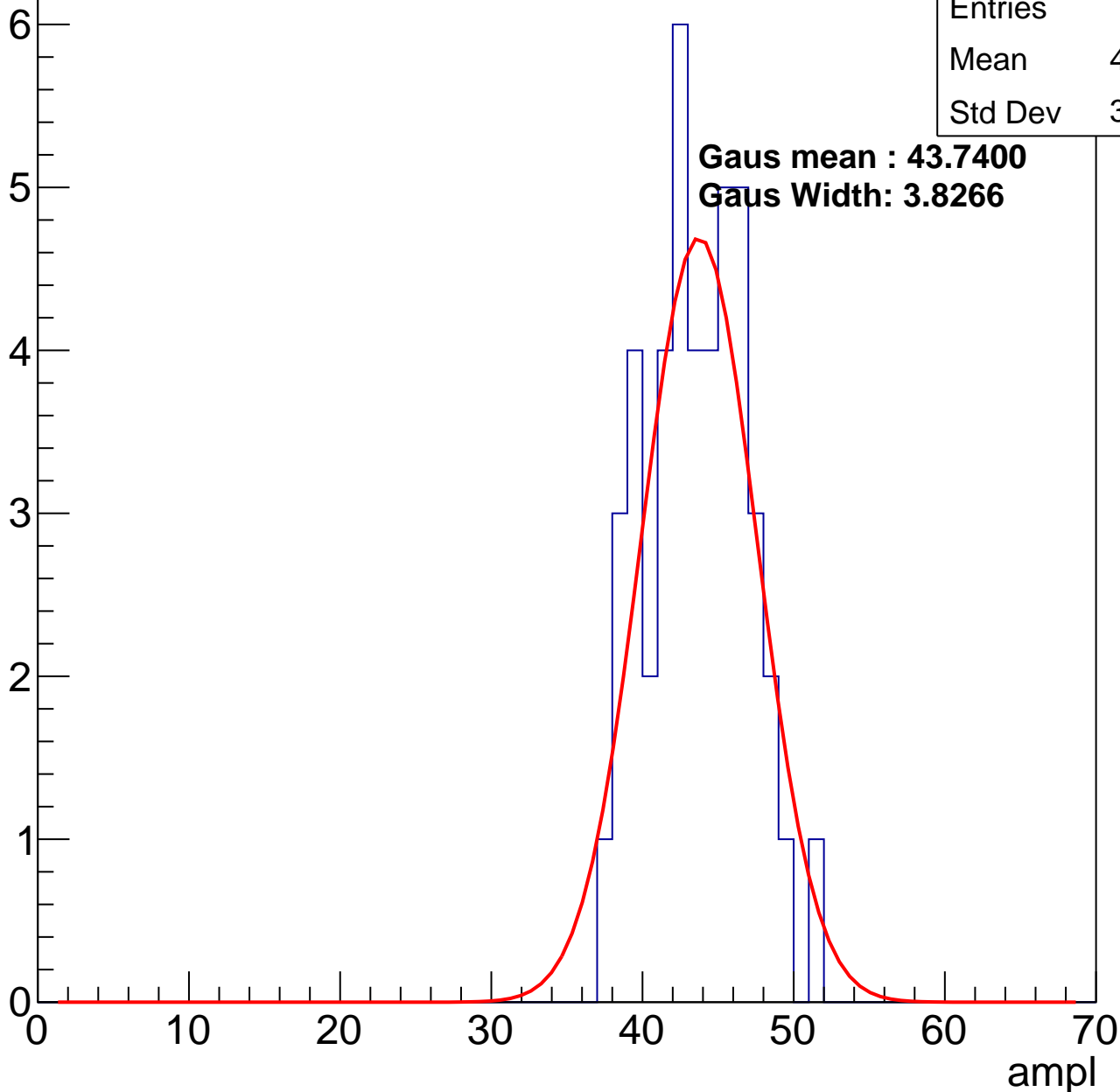
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	45
Mean	43.18
Std Dev	3.268

**Gaus mean : 43.7400**

**Gaus Width: 3.8266**

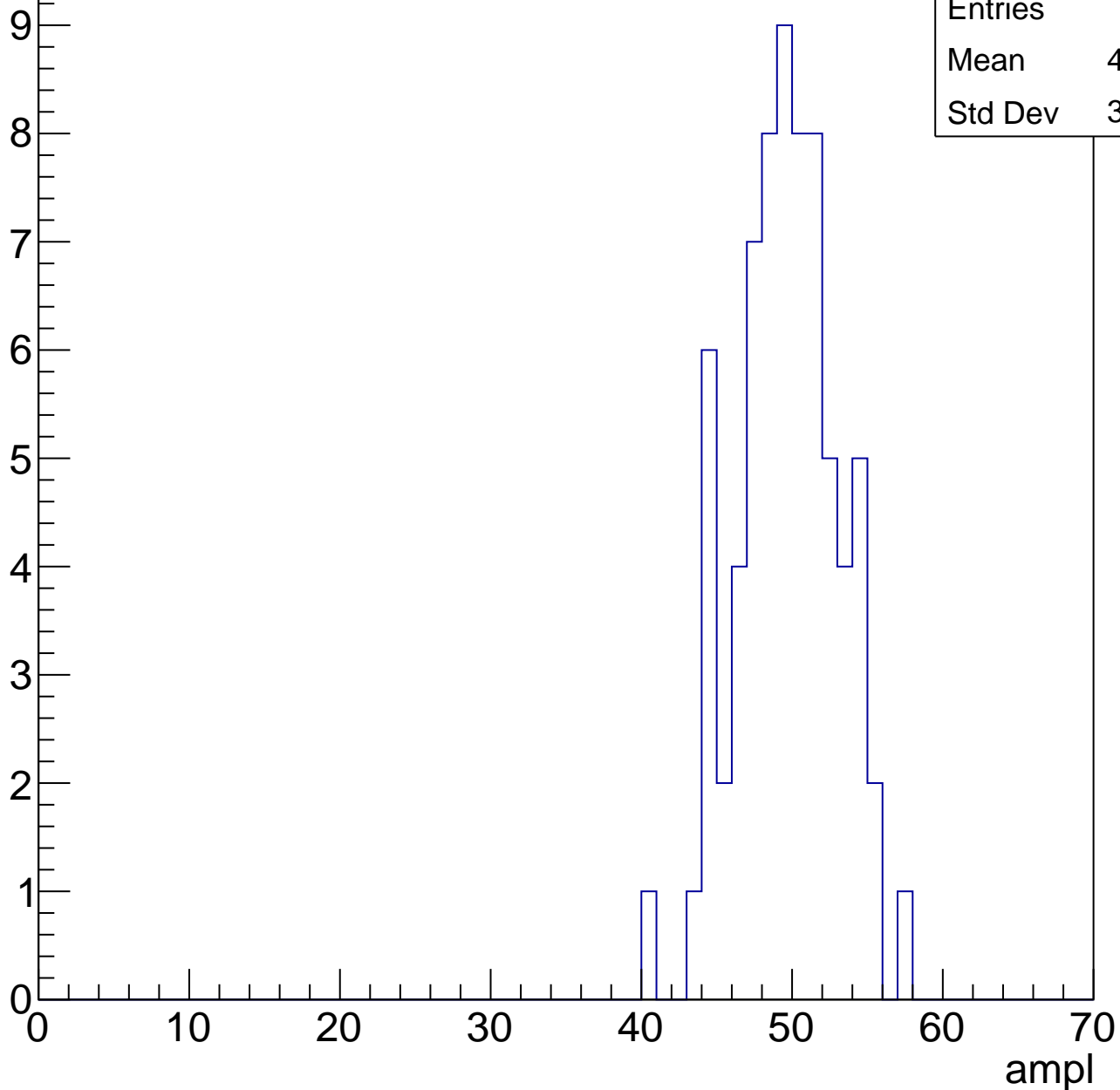


# B1L003S, U6-ch35, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	71
Mean	49.18
Std Dev	3.312

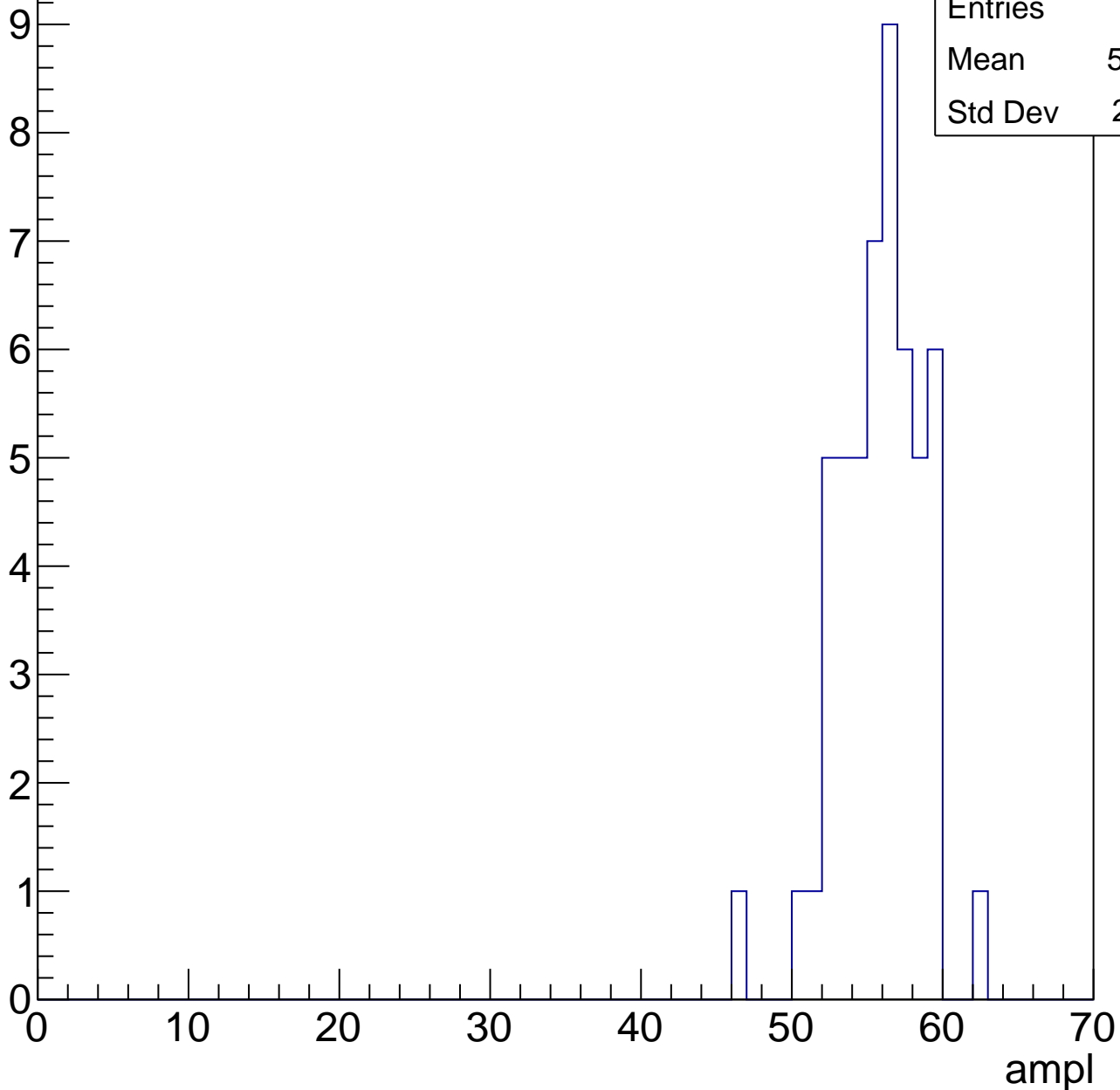


# B1L003S, U6-ch35, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	52
Mean	55.37
Std Dev	2.801

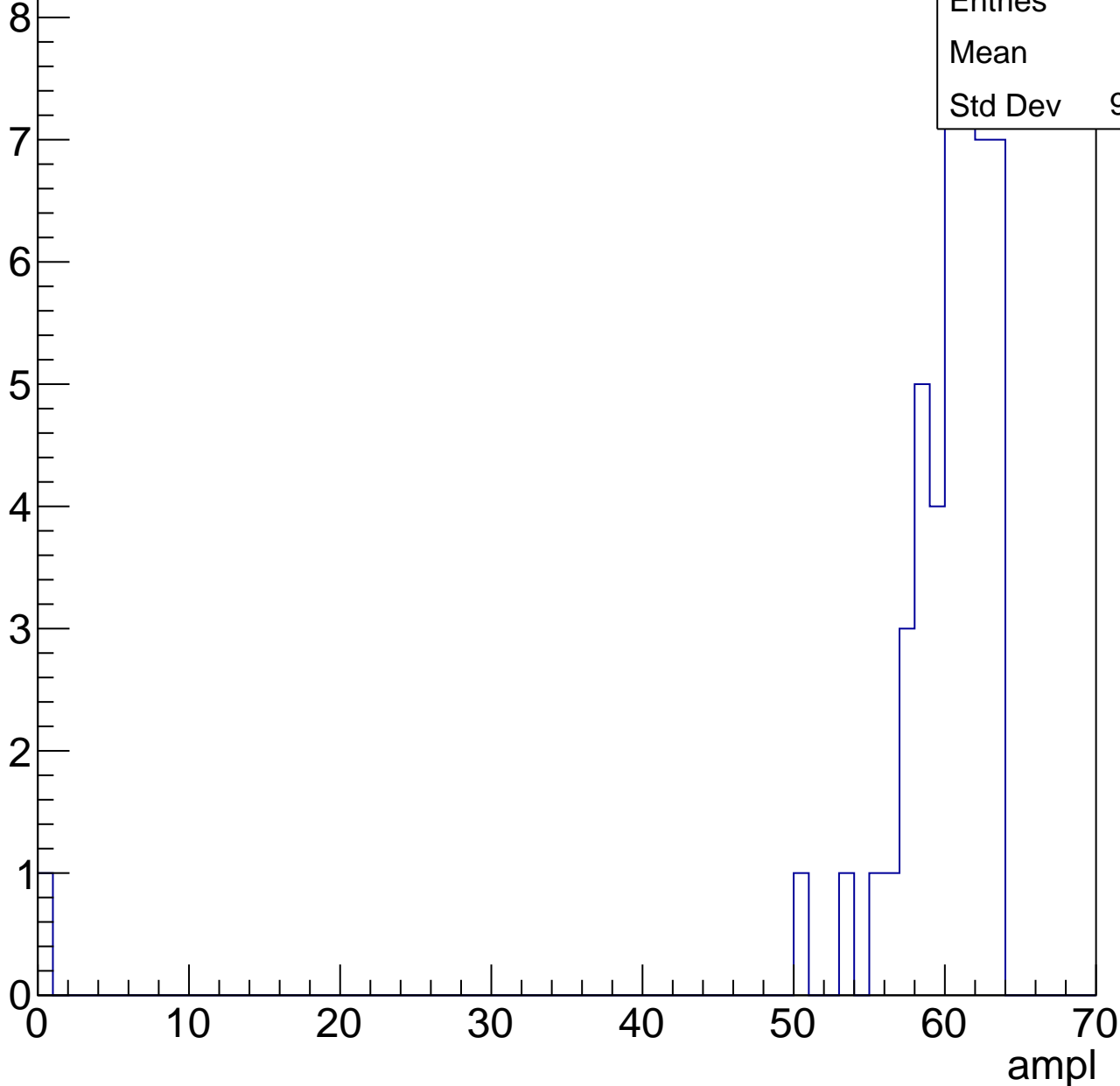


# B1L003S, U6-ch35, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	47
Mean	58.6
Std Dev	9.048



# B1L003S, U6-ch35, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries

9

Mean

61.67

Std Dev

1.155



# B1L003S, U6-ch35, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U6-ch36, adc0

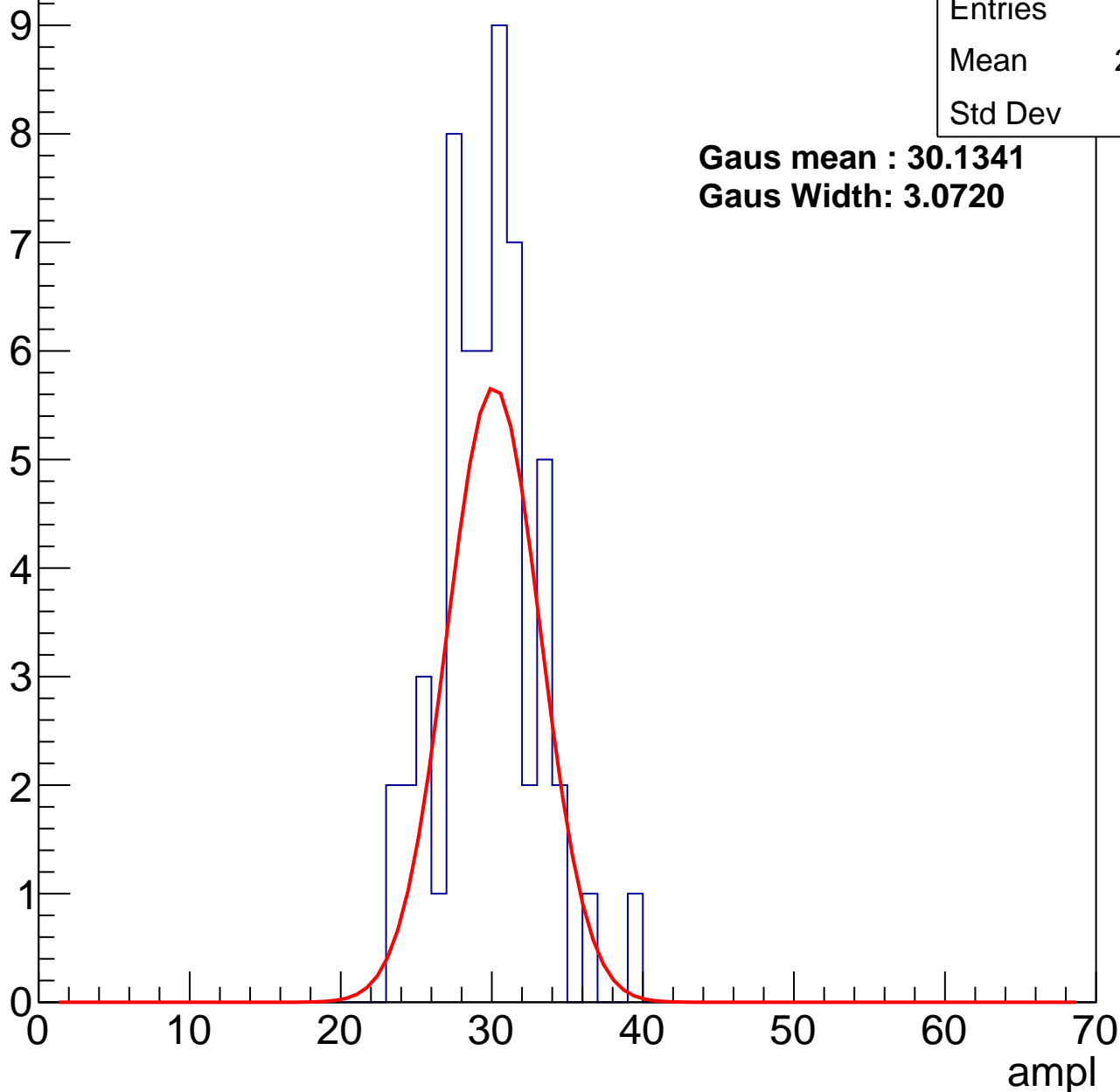
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	29.31
Std Dev	3.15

**Gaus mean : 30.1341**

**Gaus Width: 3.0720**



# B1L003S, U6-ch36, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

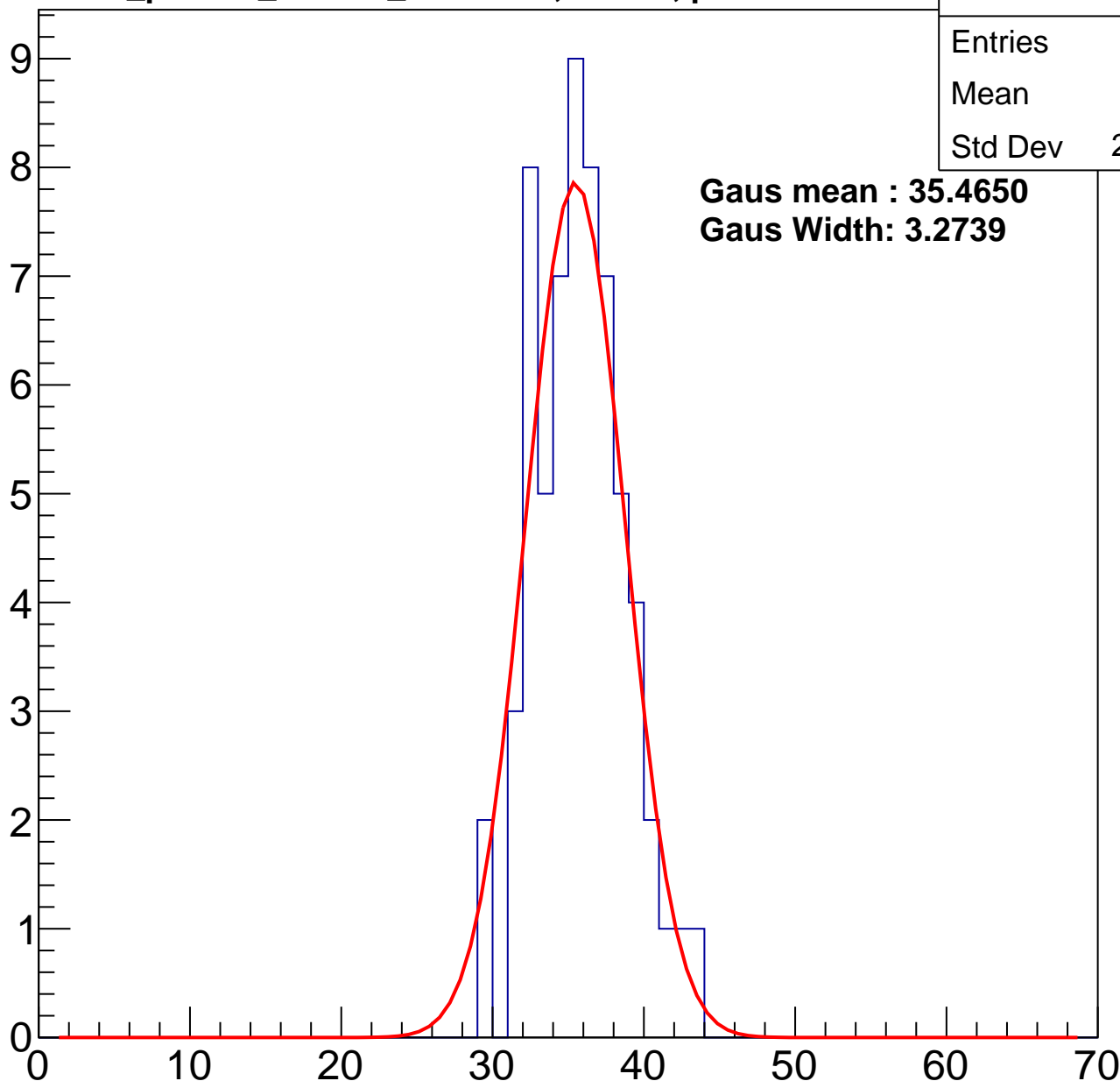
9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	63
Mean	35.3
Std Dev	2.974

**Gaus mean : 35.4650**

**Gaus Width: 3.2739**

ampl



# B1L003S, U6-ch36, adc2

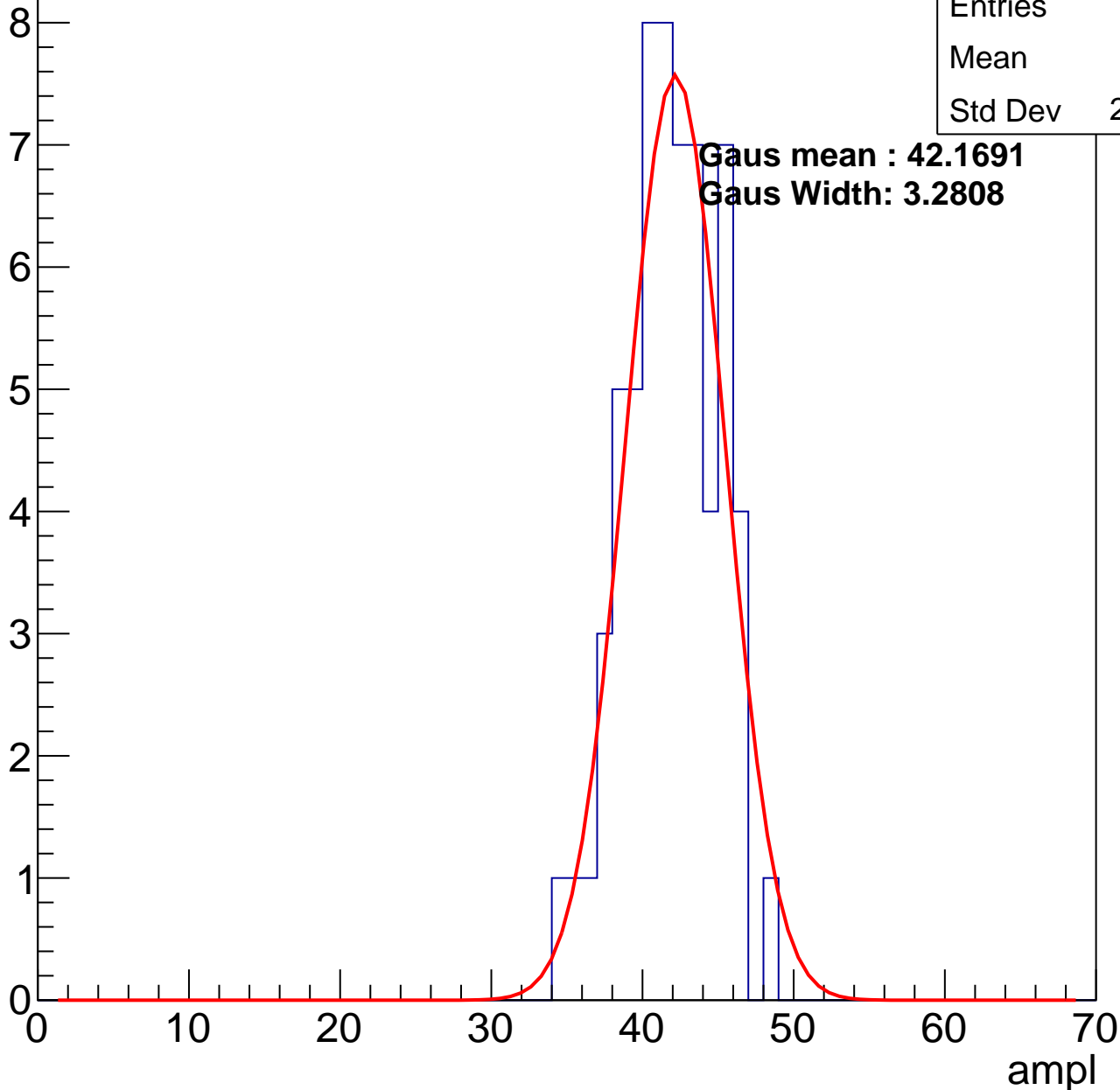
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	41.4
Std Dev	2.986

**Gaus mean : 42.1691**

**Gaus Width: 3.2808**



# B1L003S, U6-ch36, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

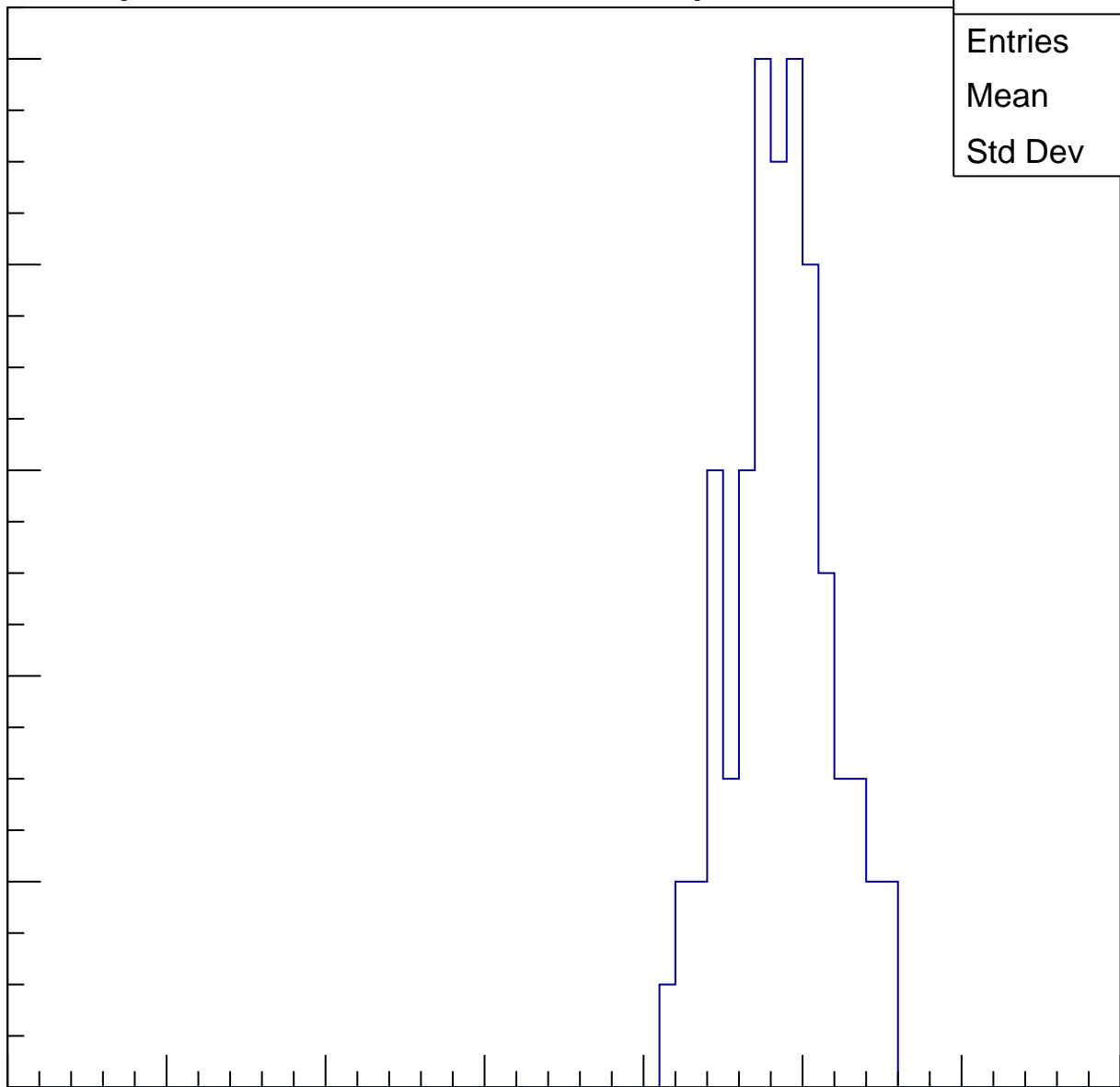
Entries	72
Mean	48.14
Std Dev	3.133

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

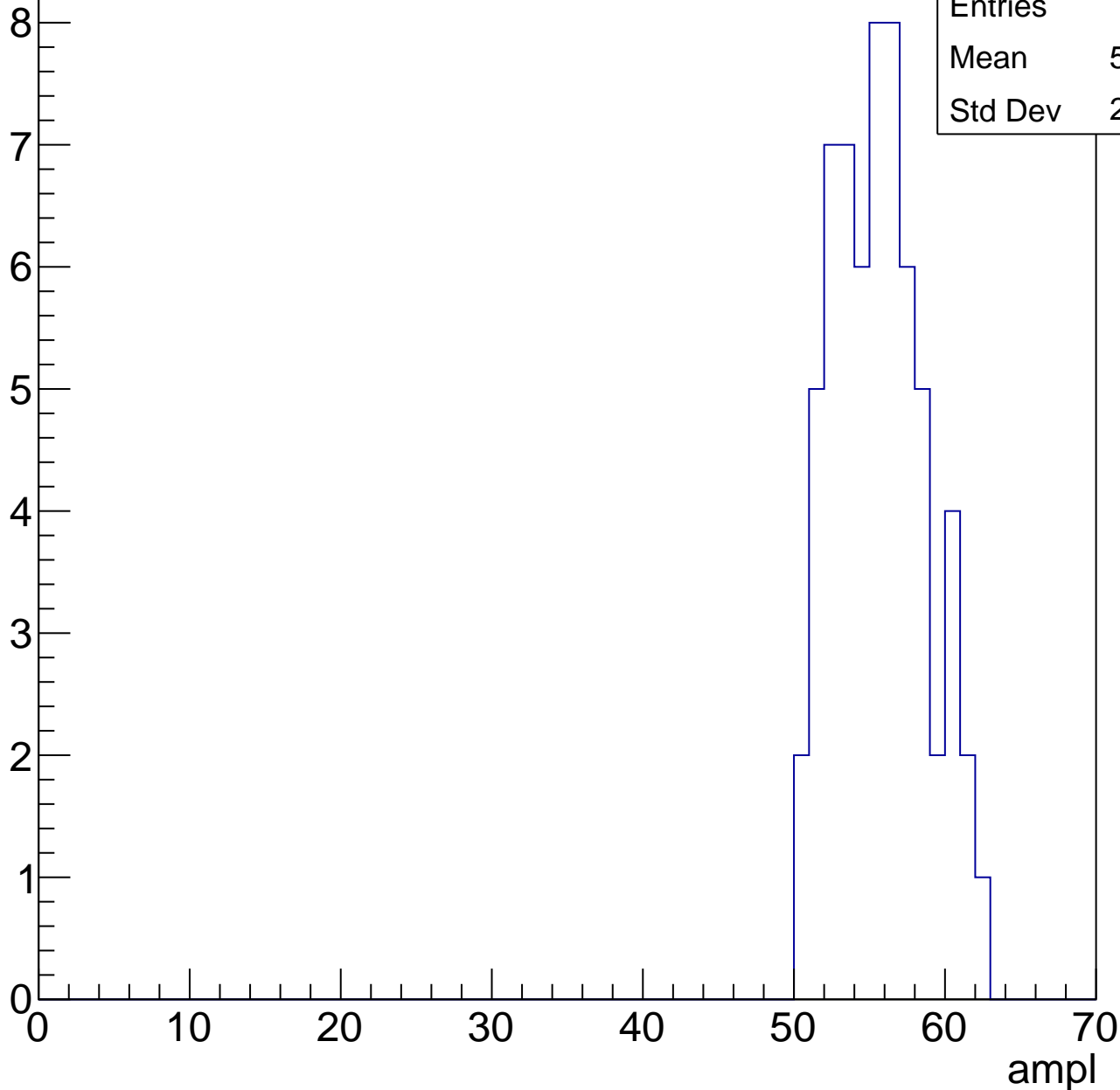


# B1L003S, U6-ch36, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

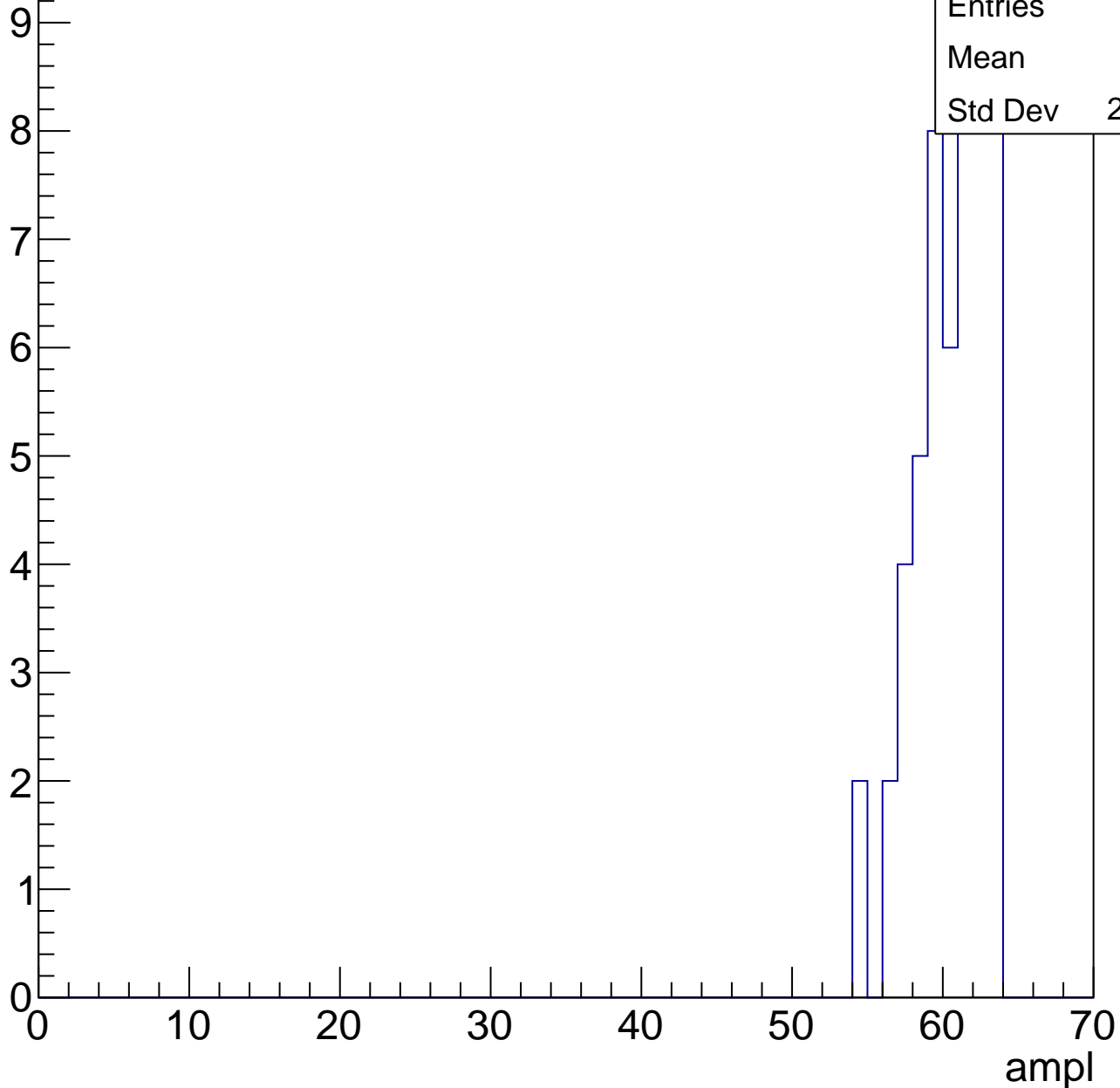
Entries	63
Mean	55.17
Std Dev	2.968



# B1L003S, U6-ch36, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	52
Mean	60
Std Dev	2.337

# B1L003S, U6-ch36, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch36, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U6-ch37, adc0

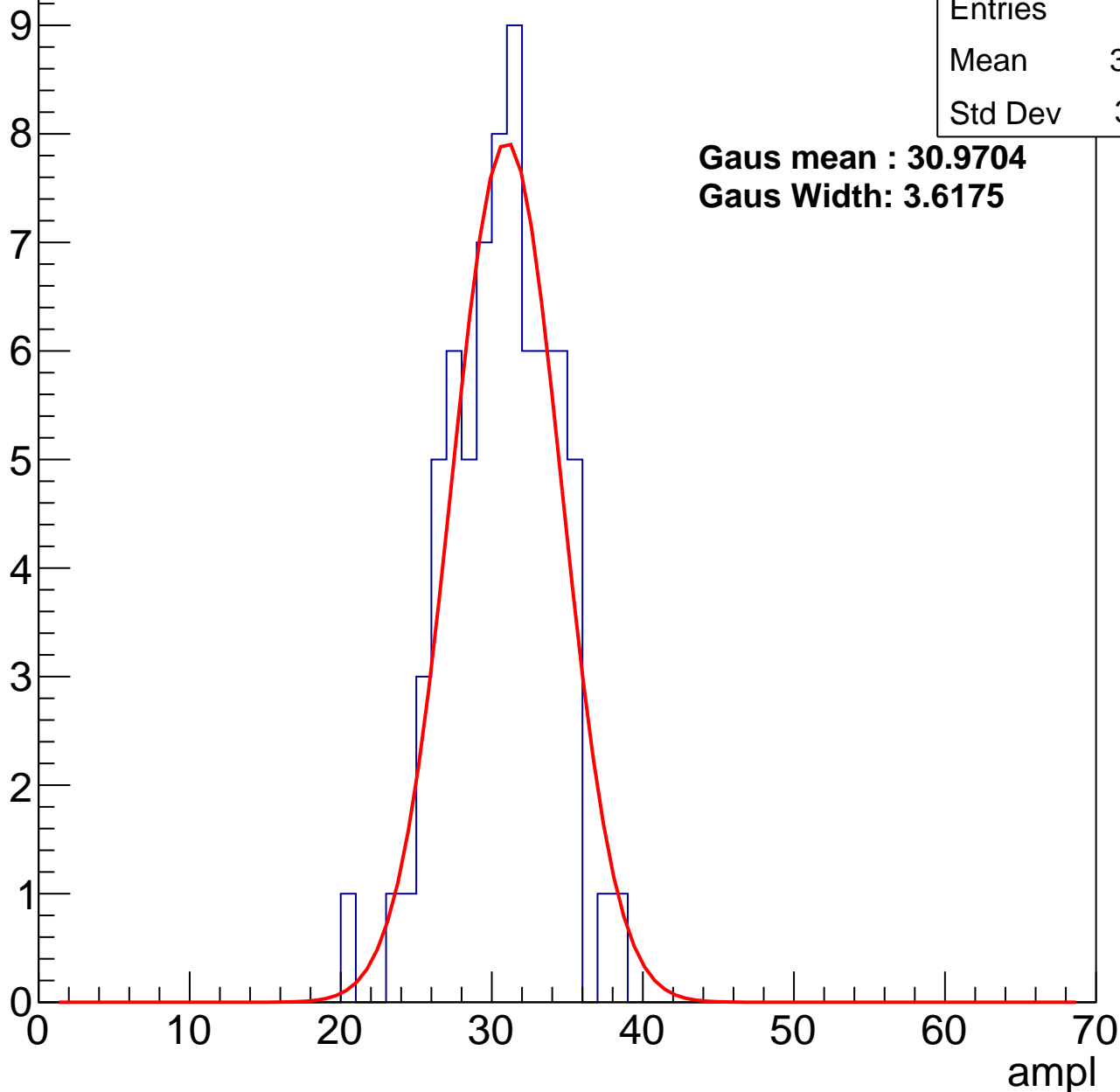
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	71
Mean	30.14
Std Dev	3.441

**Gaus mean : 30.9704**

**Gaus Width: 3.6175**



# B1L003S, U6-ch37, adc1

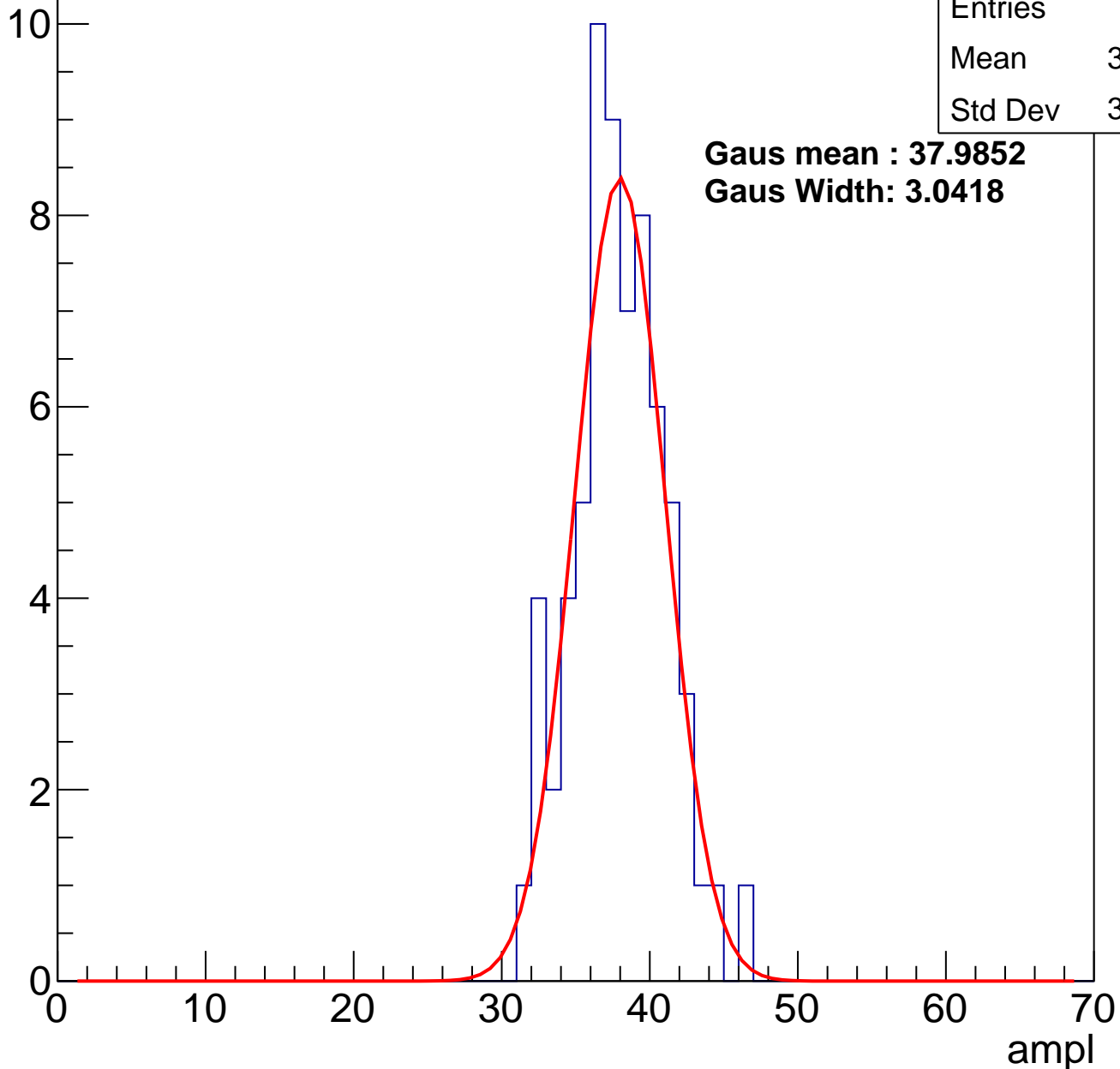
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	67
Mean	37.48
Std Dev	3.073

**Gaus mean : 37.9852**

**Gaus Width: 3.0418**

Entry



# B1L003S, U6-ch37, adc2

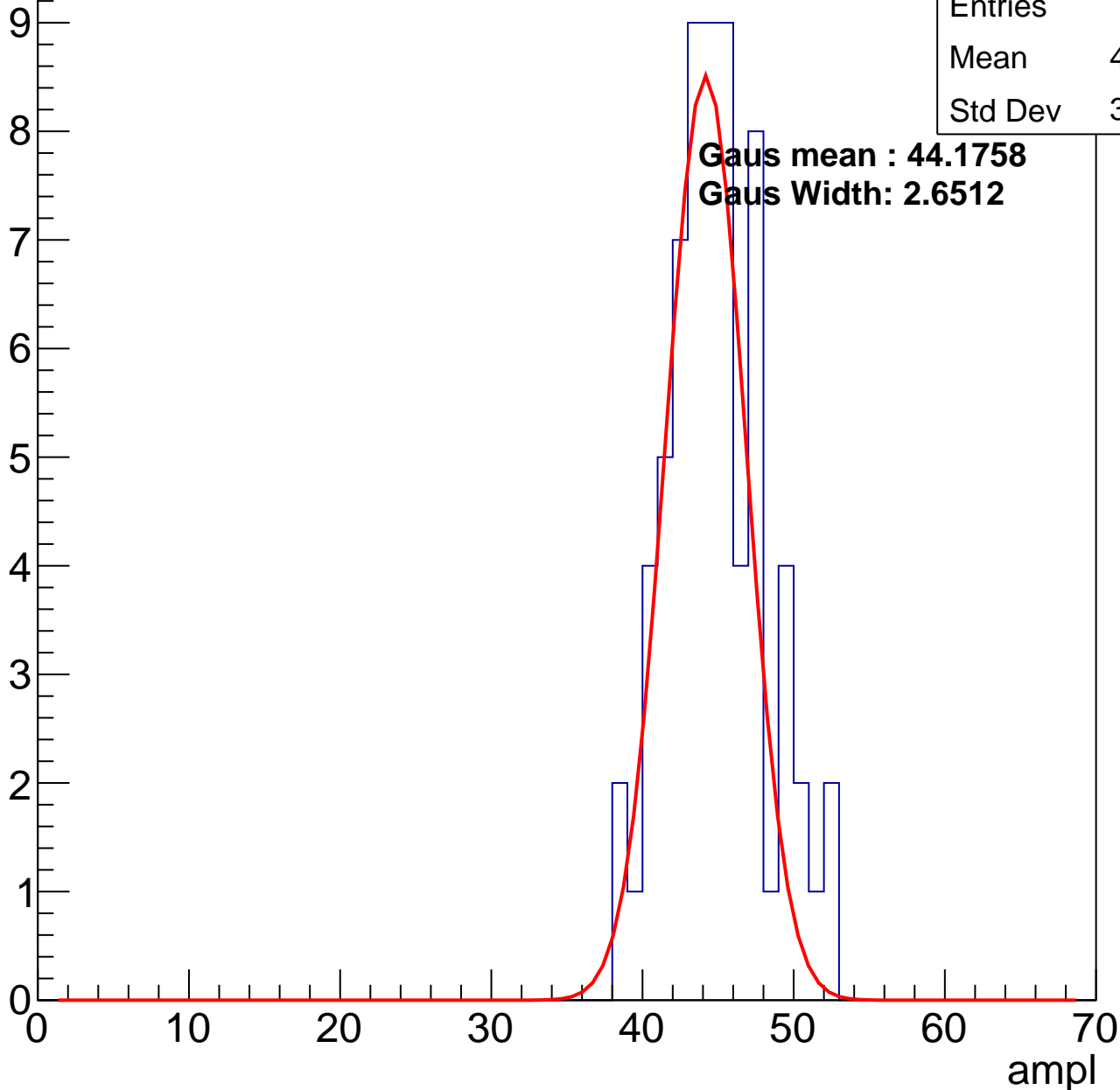
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	44.43
Std Dev	3.192

**Gaus mean : 44.1758**

**Gaus Width: 2.6512**

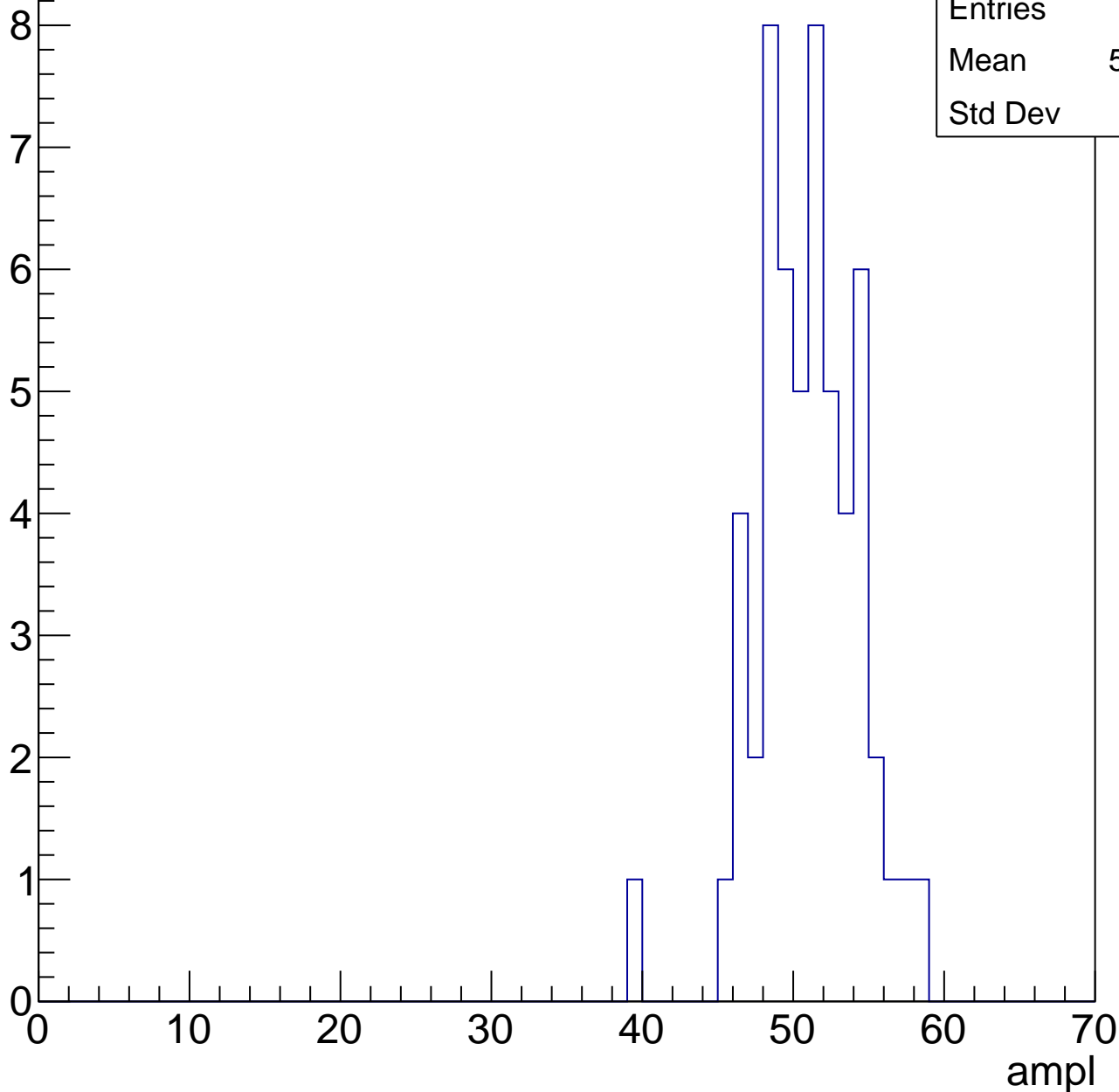


# B1L003S, U6-ch37, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	50.45
Std Dev	3.34

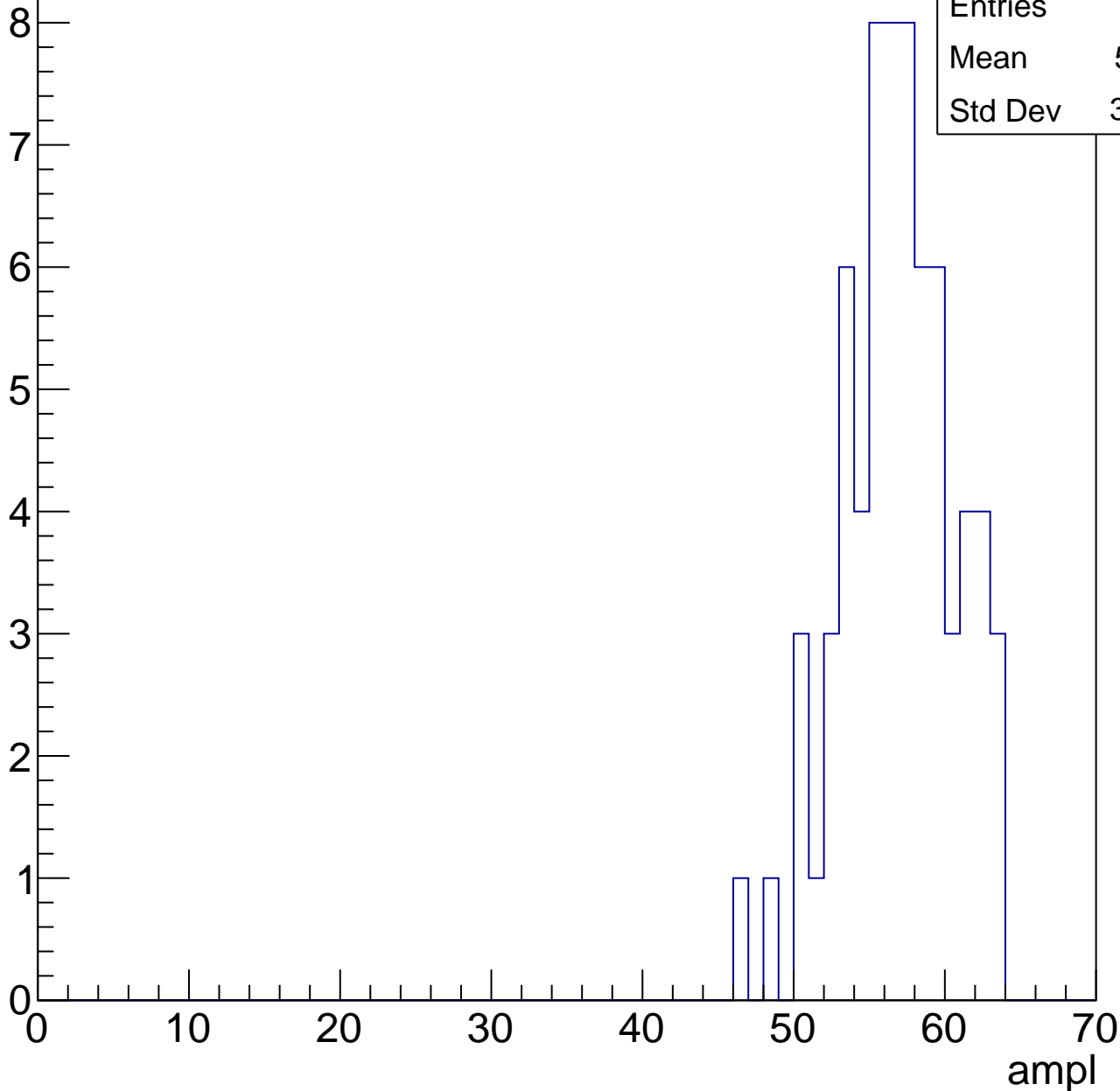


# B1L003S, U6-ch37, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

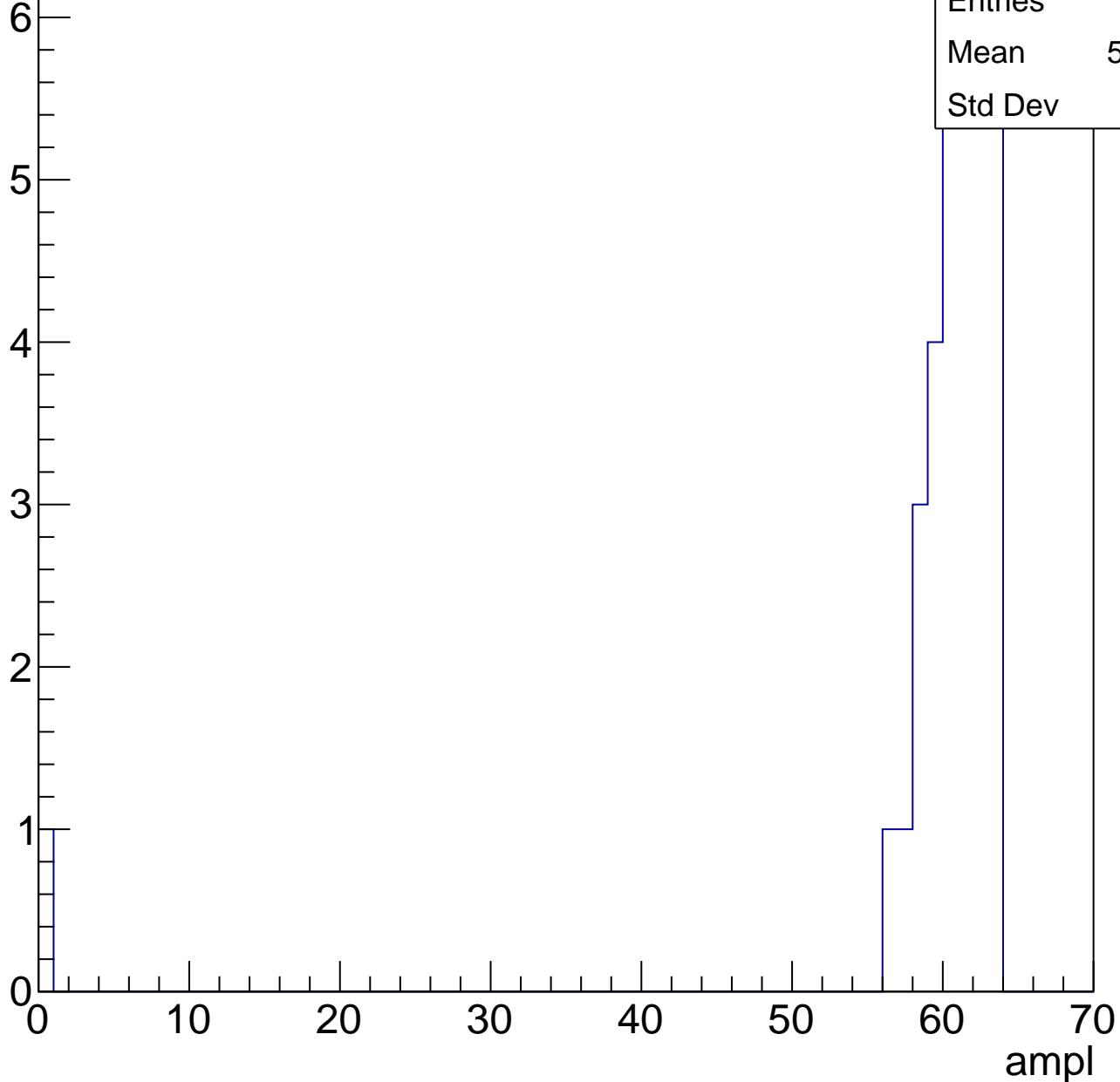
Entries	69
Mean	56.41
Std Dev	3.684



# B1L003S, U6-ch37, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch37, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch37, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch38, adc0

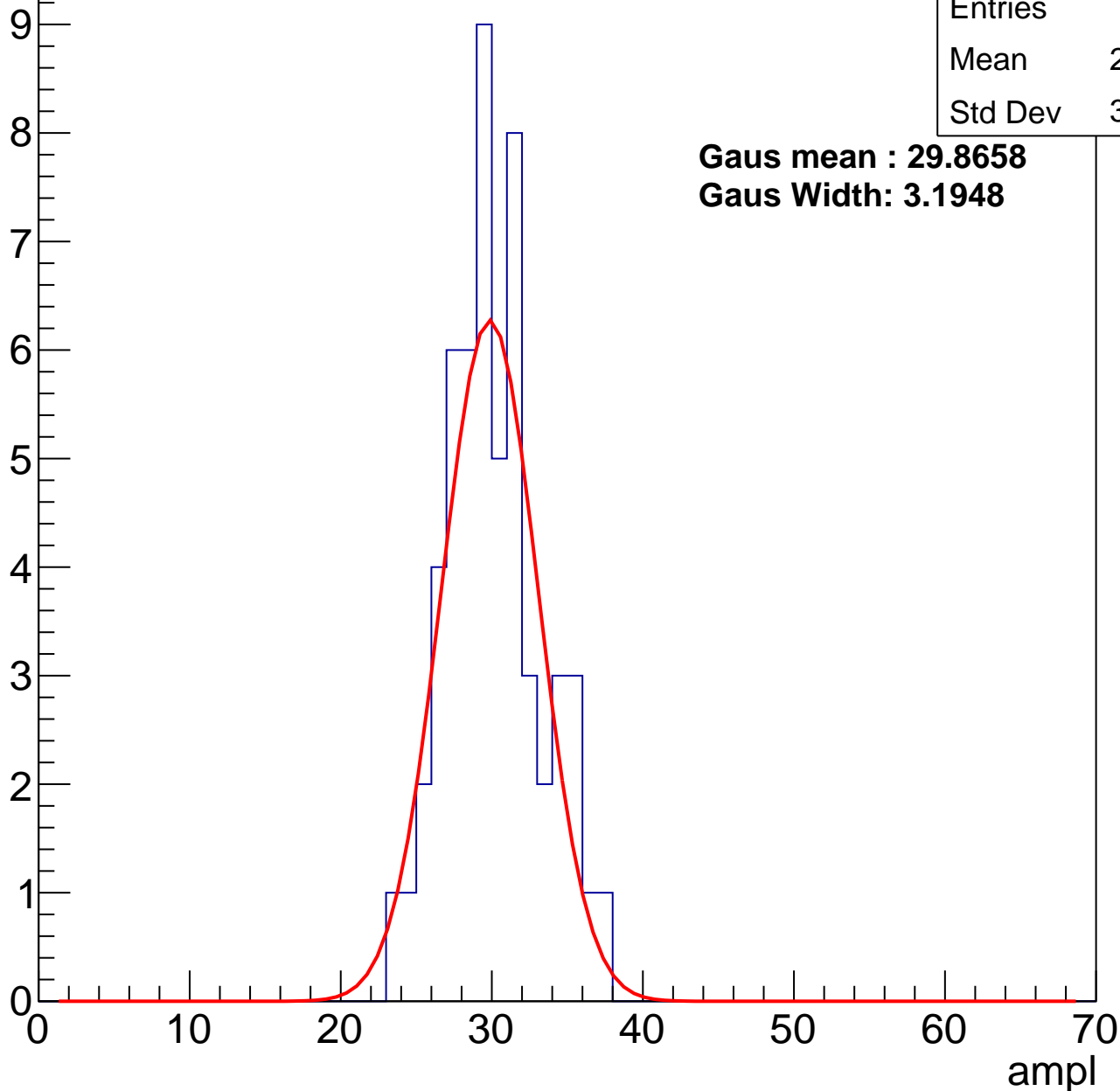
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	29.67
Std Dev	3.093

**Gaus mean : 29.8658**

**Gaus Width: 3.1948**



# B1L003S, U6-ch38, adc1

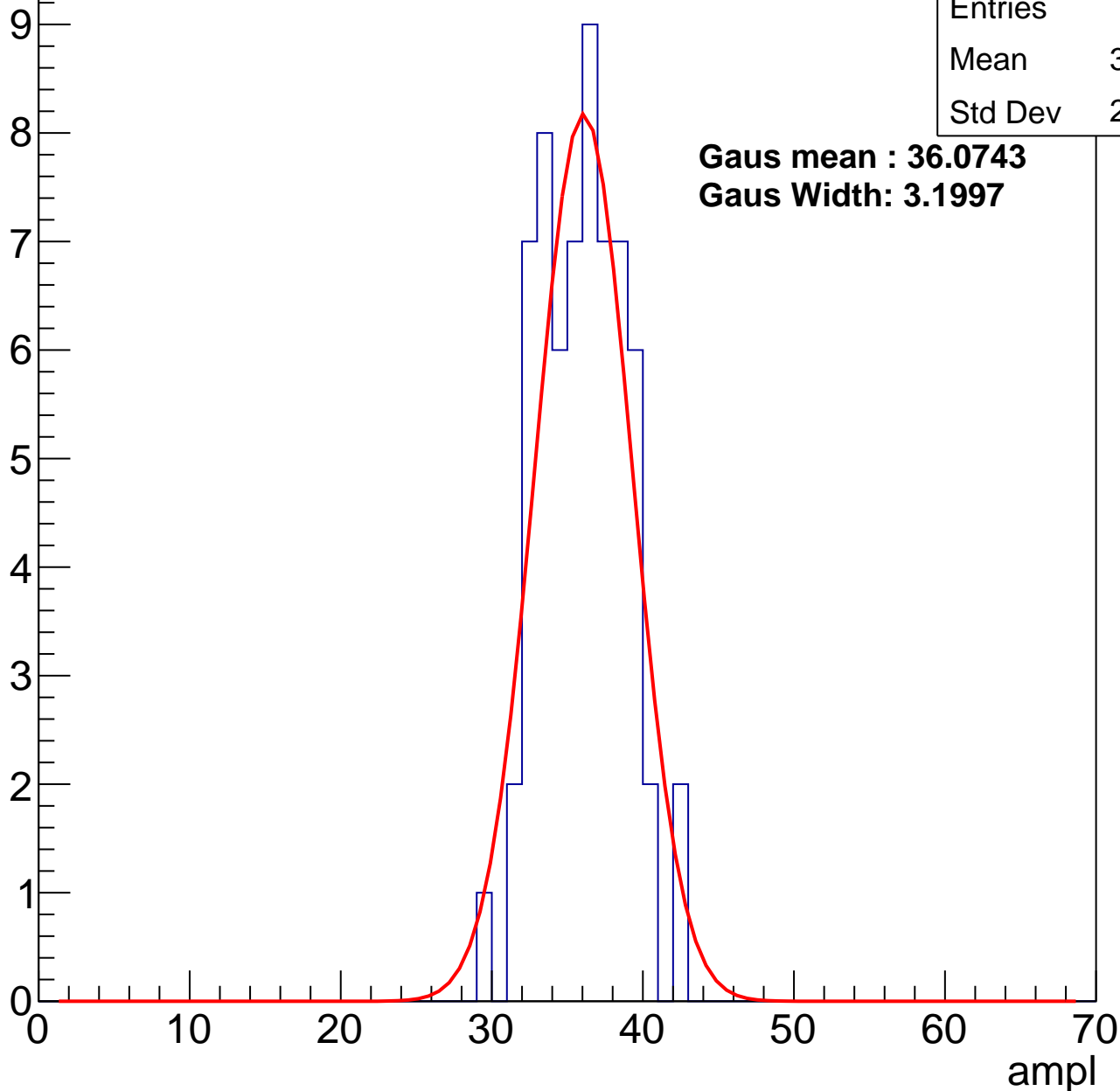
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	35.55
Std Dev	2.778

**Gaus mean : 36.0743**

**Gaus Width: 3.1997**



# B1L003S, U6-ch38, adc2

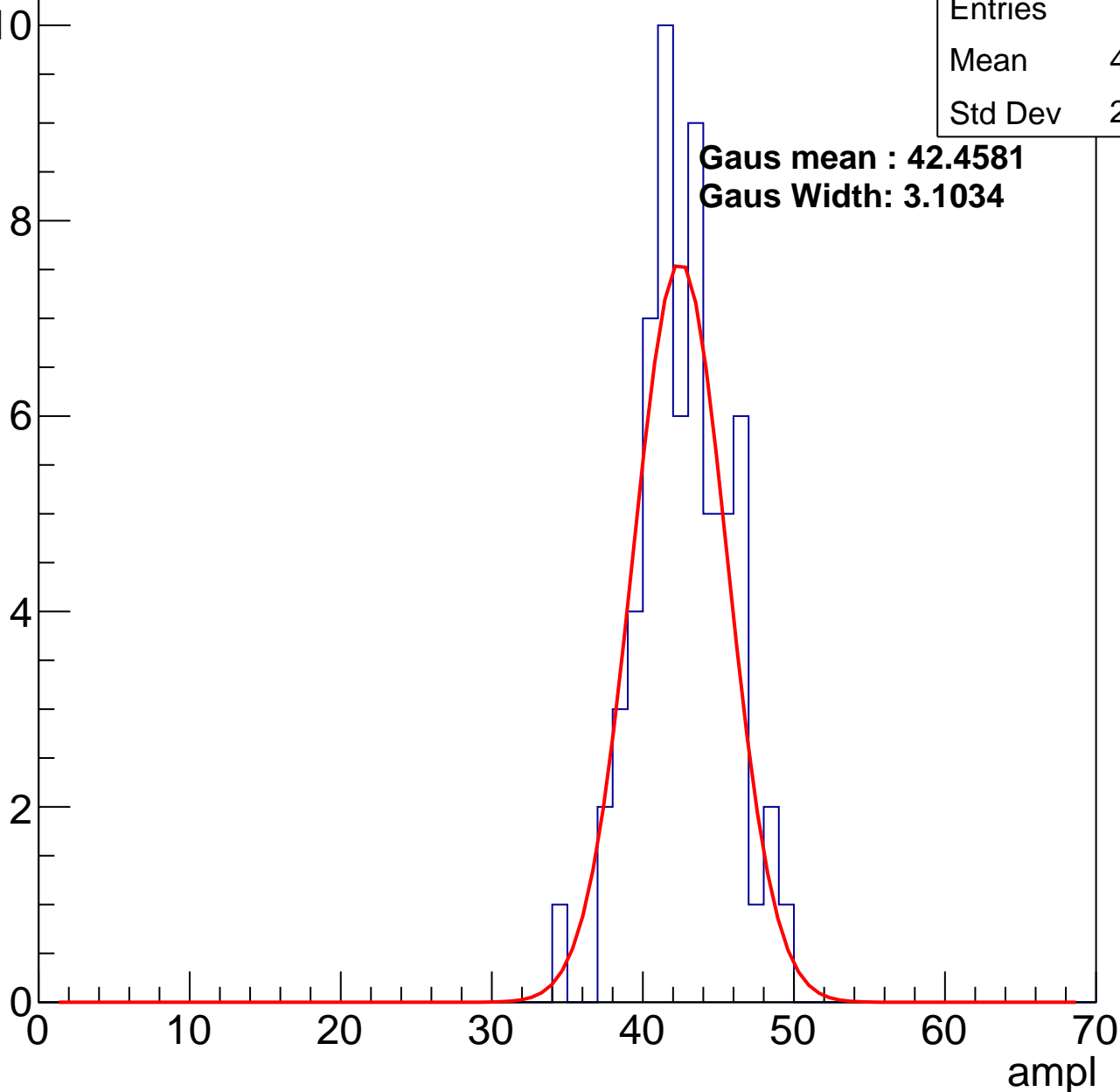
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	42.26
Std Dev	2.973

**Gaus mean : 42.4581**

**Gaus Width: 3.1034**

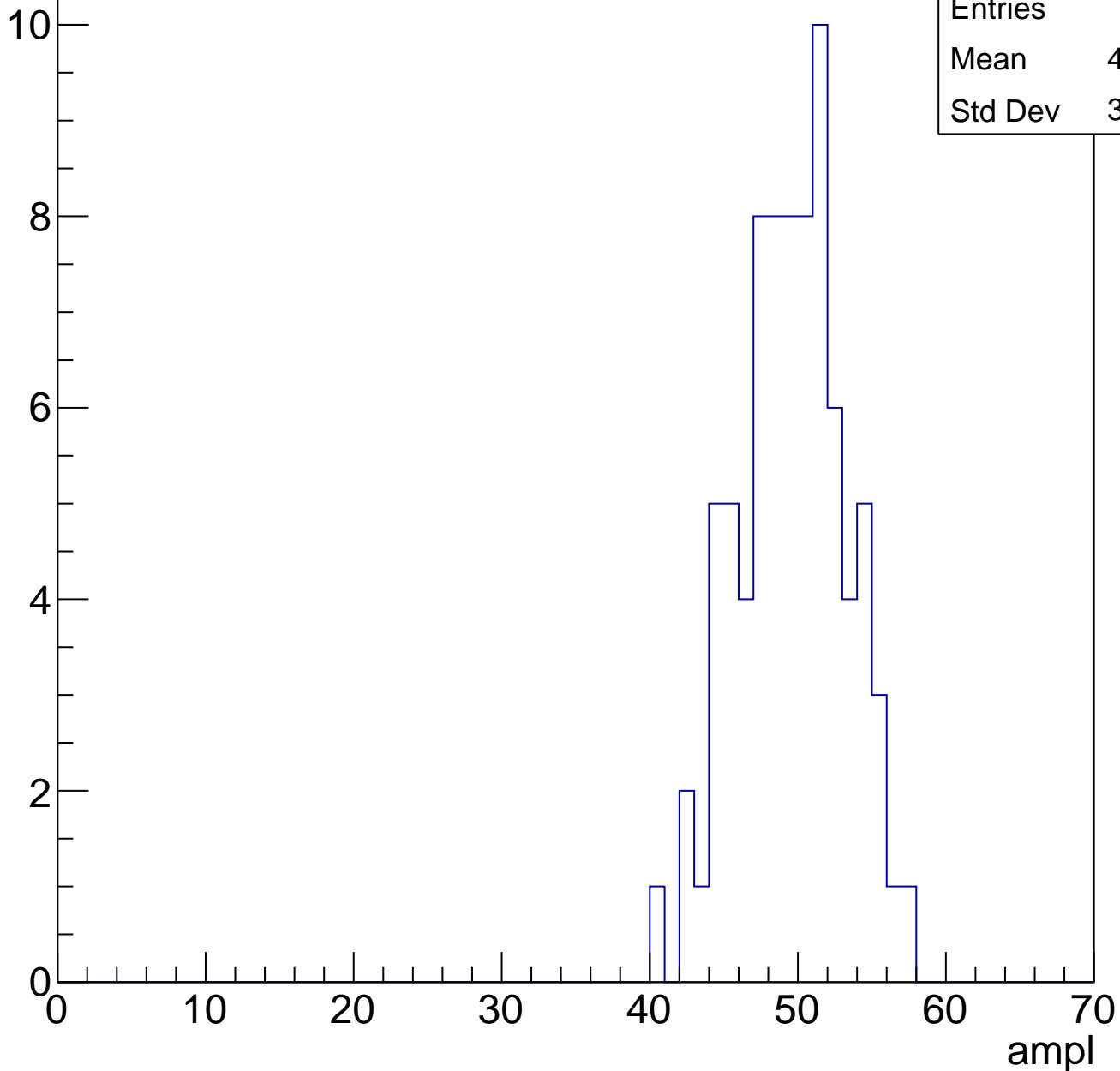


# B1L003S, U6-ch38, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	80
Mean	49.12
Std Dev	3.547

Entry

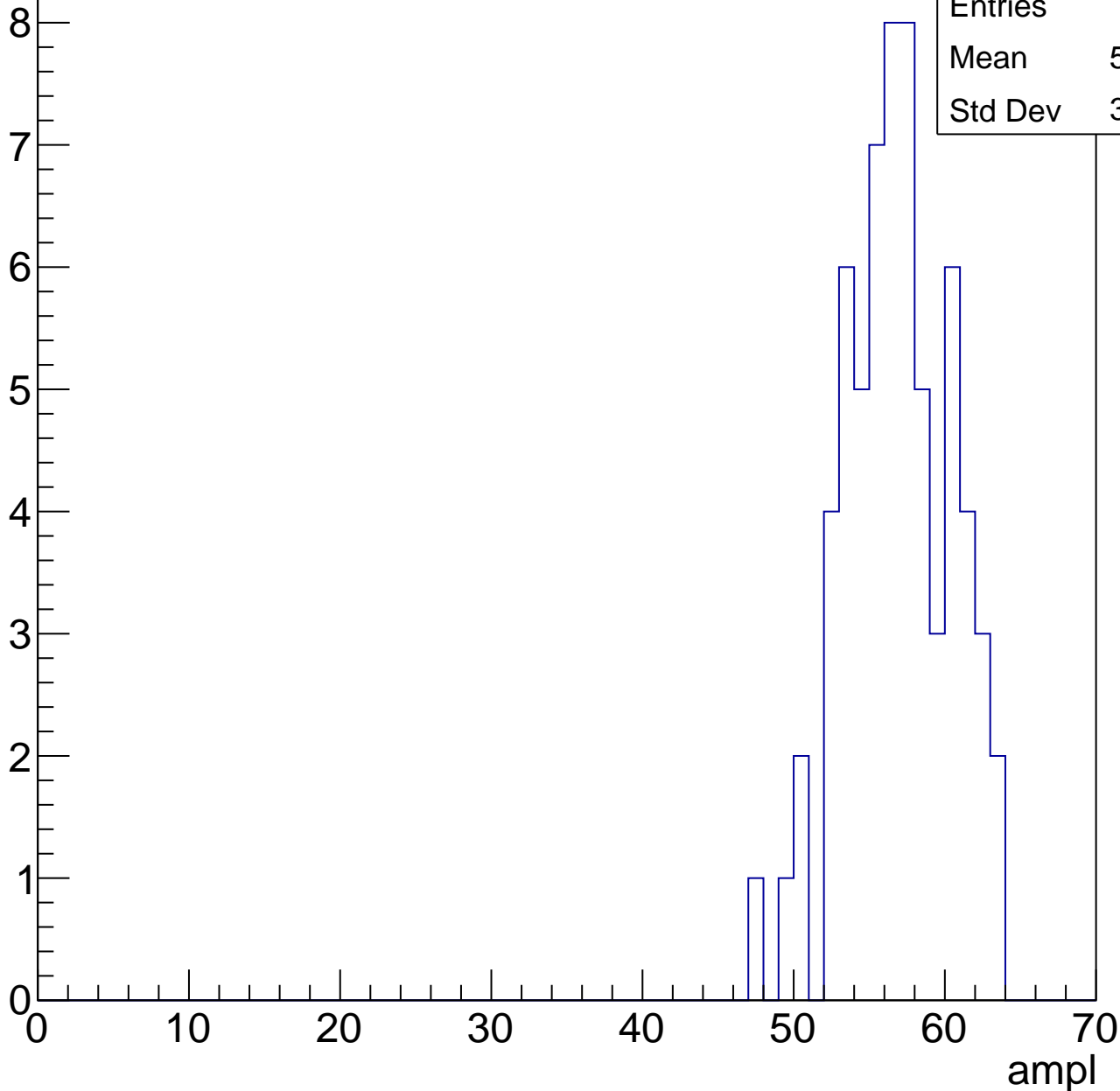


# B1L003S, U6-ch38, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

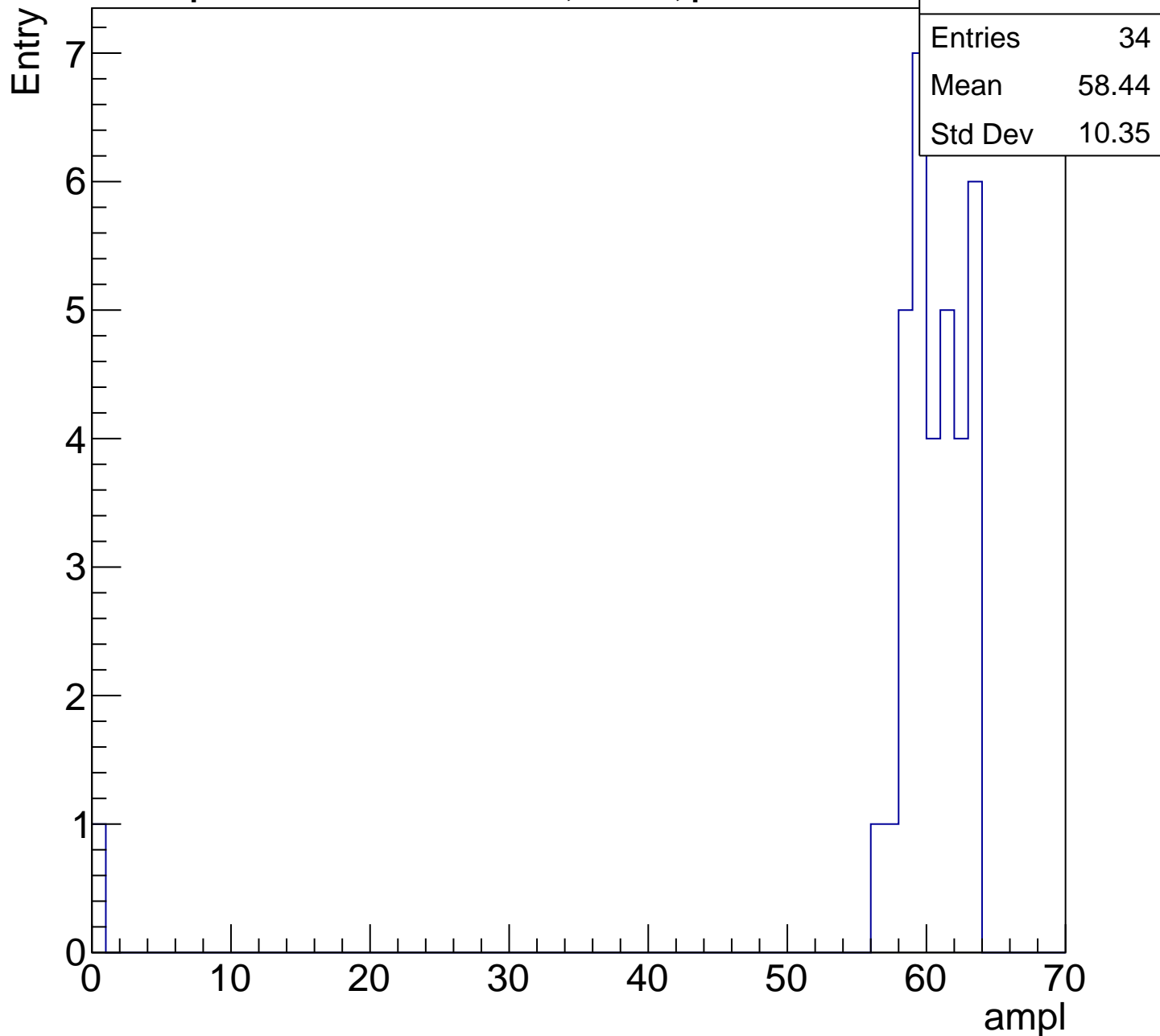
Entry

Entries	65
Mean	56.37
Std Dev	3.498



# B1L003S, U6-ch38, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2



# B1L003S, U6-ch38, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch38, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch39, adc0

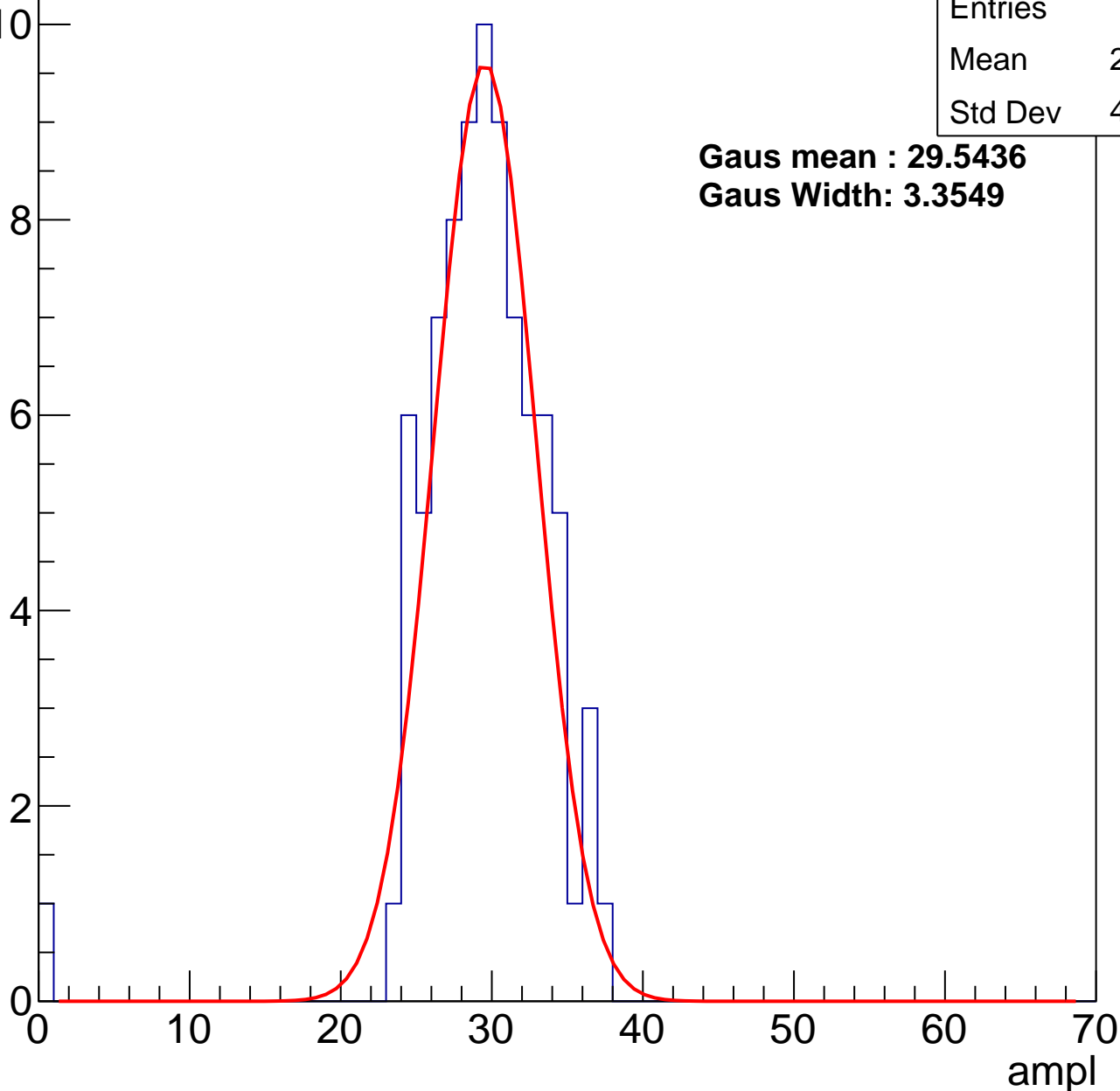
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	85
Mean	28.93
Std Dev	4.563

**Gaus mean : 29.5436**

**Gaus Width: 3.3549**



# B1L003S, U6-ch39, adc1

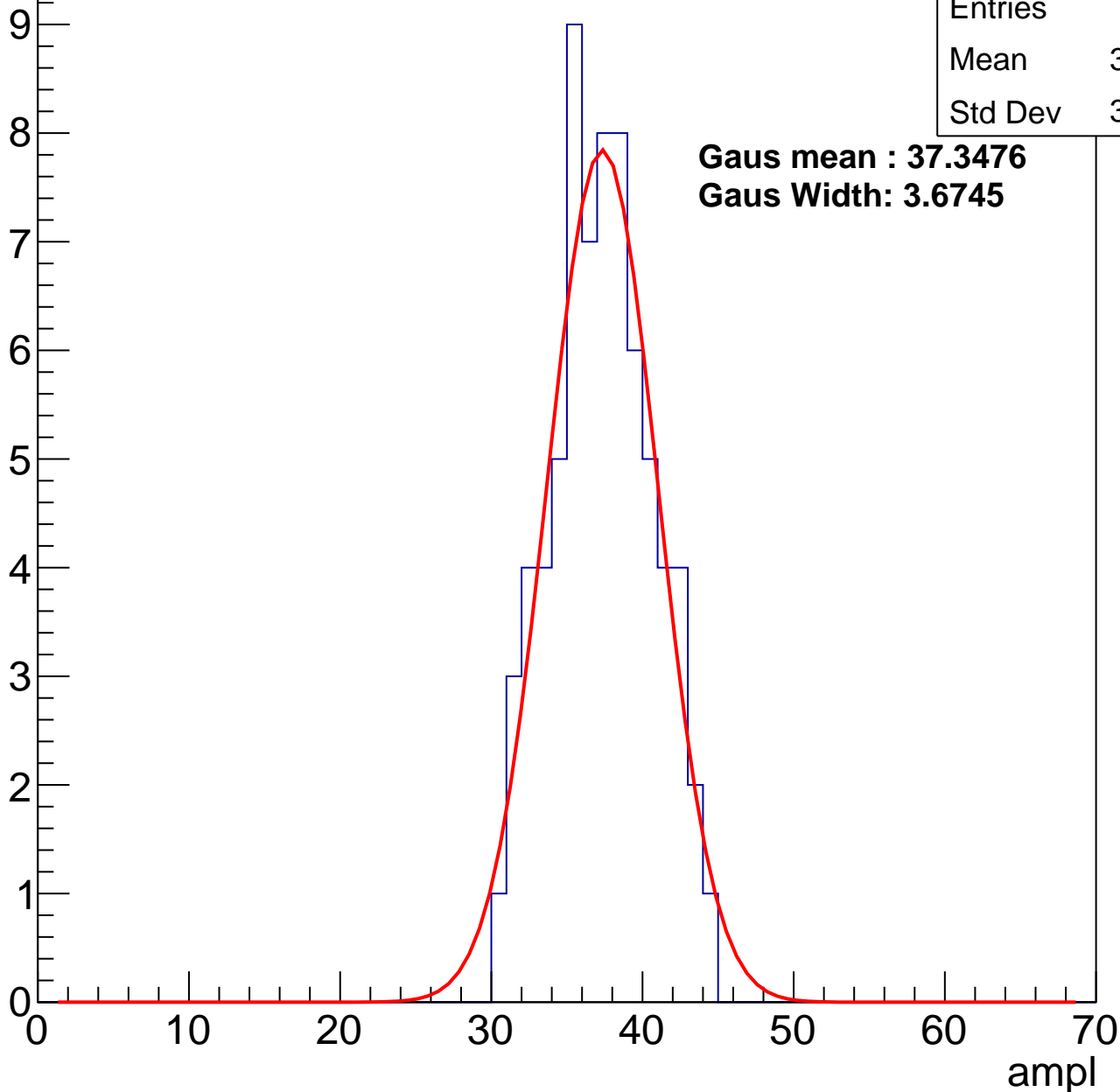
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	71
Mean	36.85
Std Dev	3.292

**Gaus mean : 37.3476**

**Gaus Width: 3.6745**

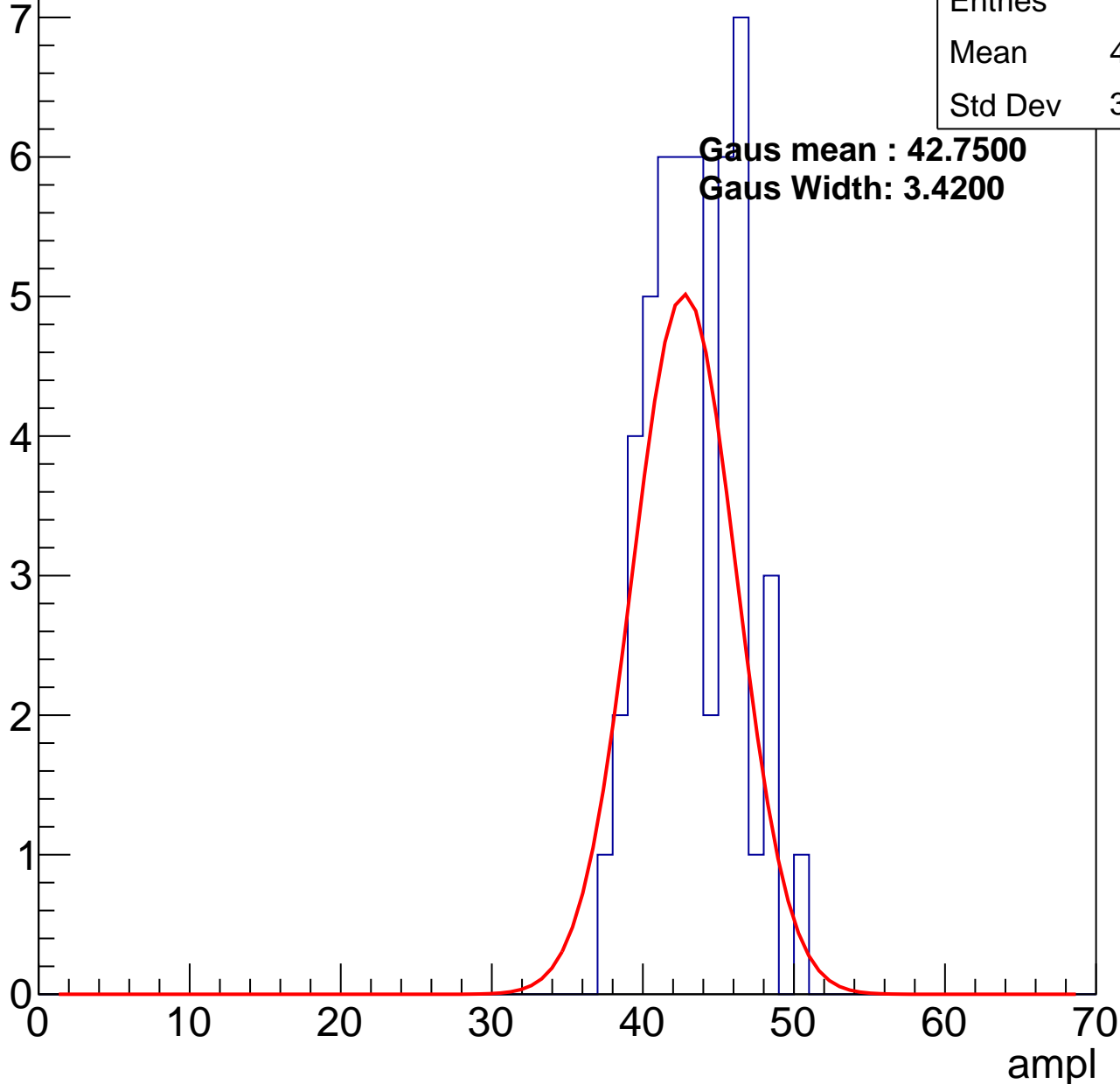


# B1L003S, U6-ch39, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

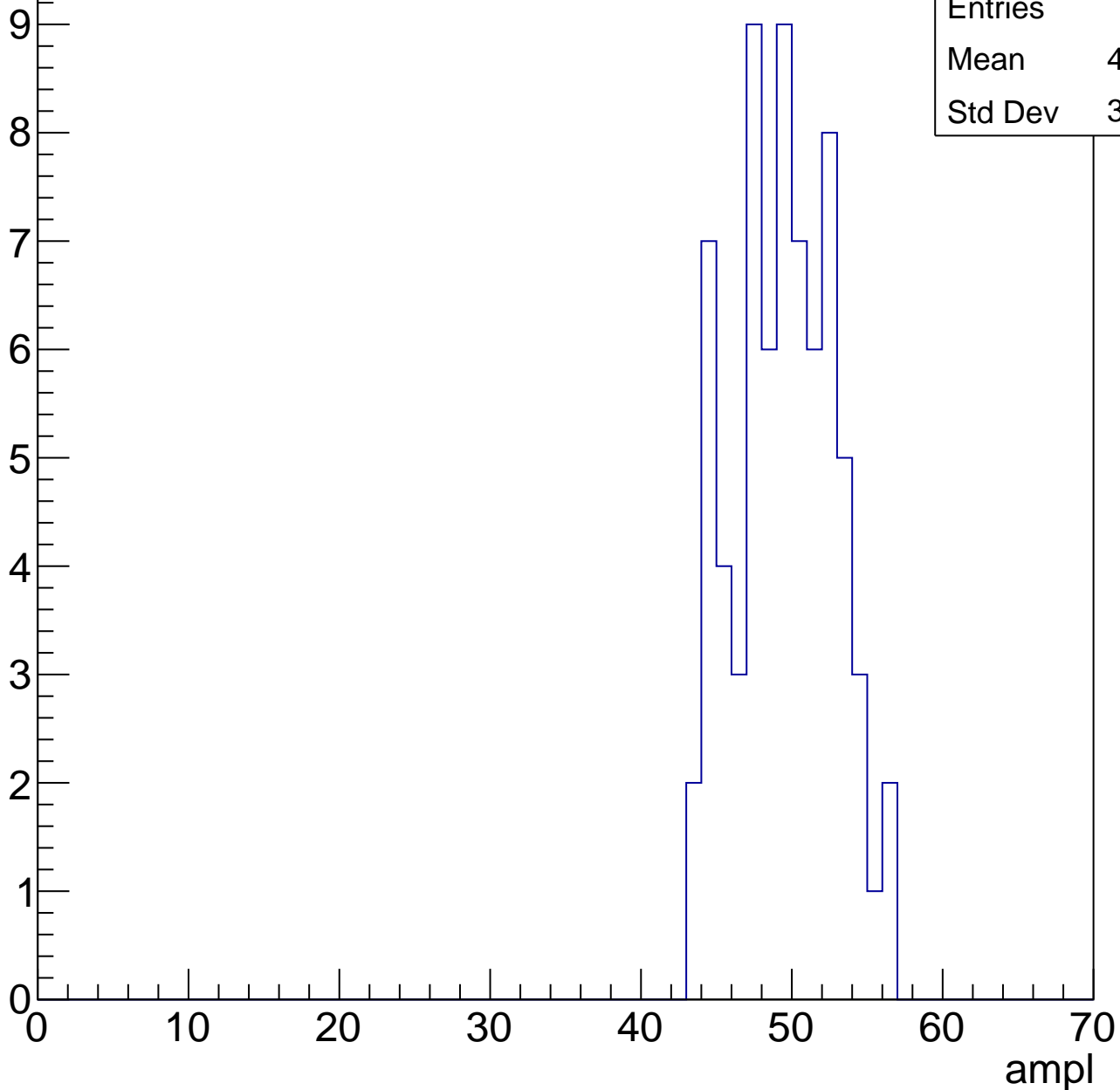
Entries	50
Mean	42.92
Std Dev	3.012



# B1L003S, U6-ch39, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



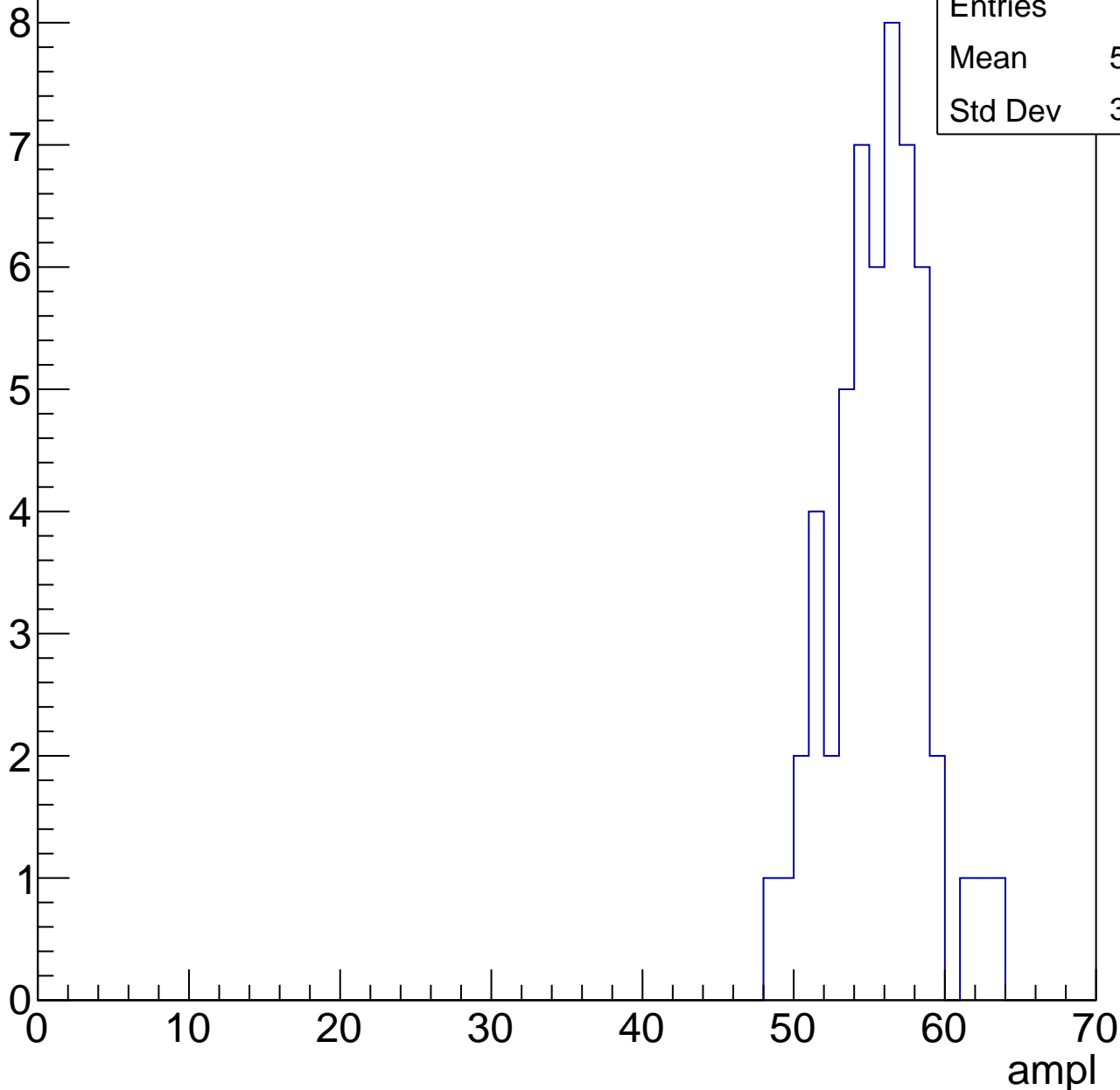
Entries	72
Mean	49.03
Std Dev	3.274

# B1L003S, U6-ch39, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	54
Mean	55.13
Std Dev	3.085



# B1L003S, U6-ch39, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

10

Entries 53

Mean 59

Std Dev 8.447

8

6

4

2

0

0

10

20

30

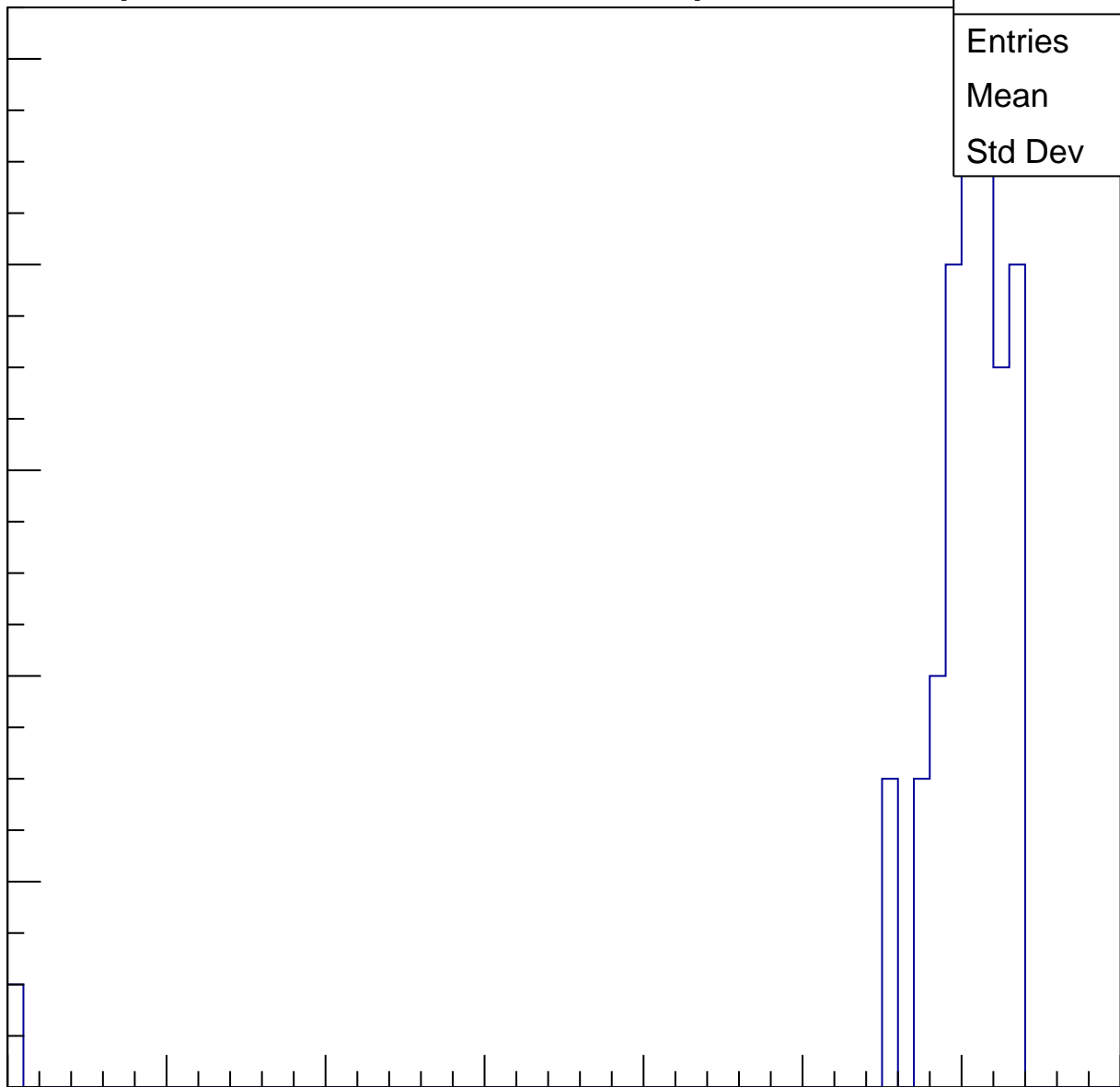
40

50

60

70

ampl



# B1L003S, U6-ch39, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch39, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch40, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	68
Mean	29.46
Std Dev	5.057

**Gaus mean : 30.4647**

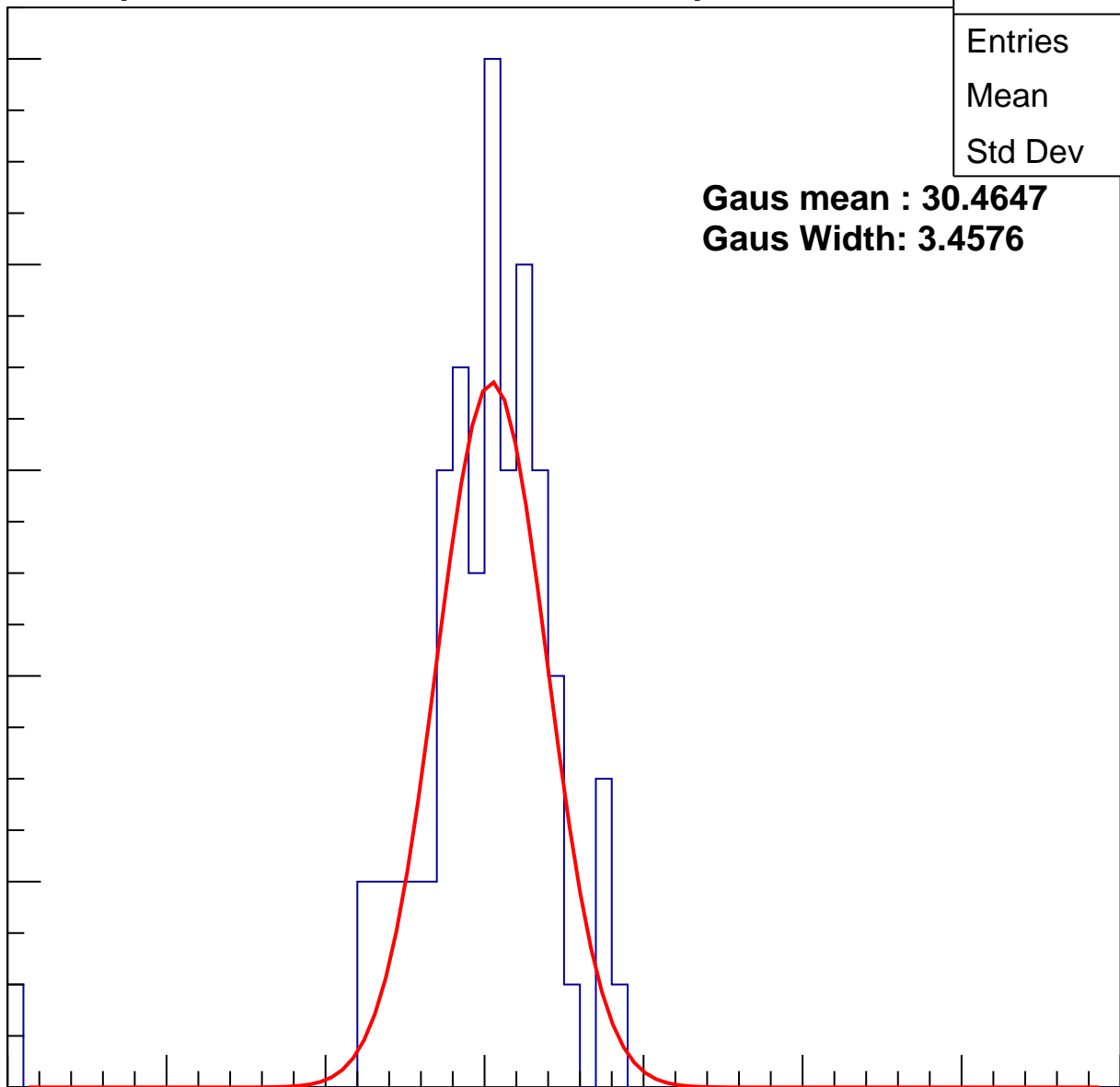
**Gaus Width: 3.4576**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U6-ch40, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	71
Mean	36.72
Std Dev	3.357

**Gaus mean : 37.0411**

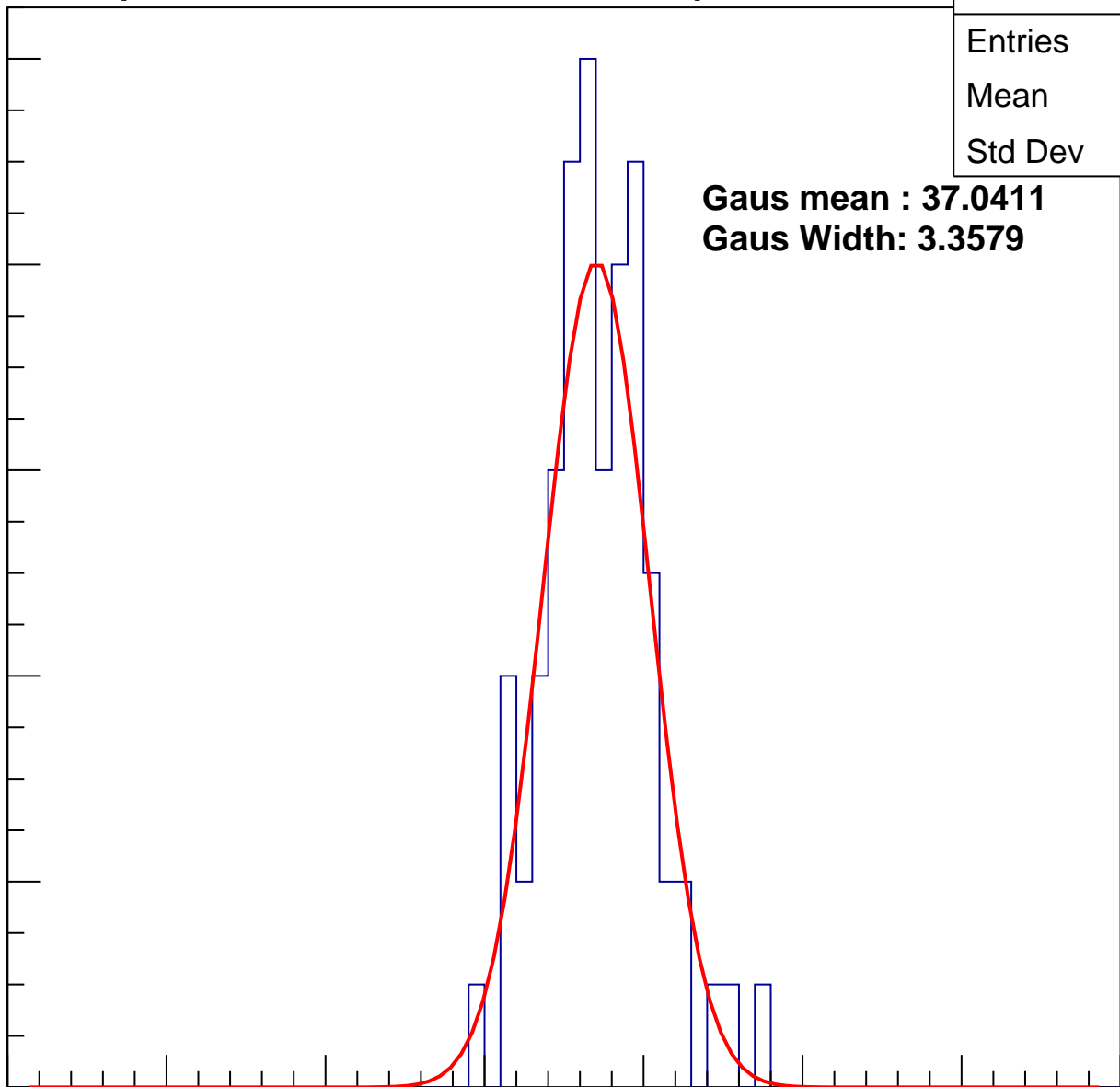
**Gaus Width: 3.3579**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L003S, U6-ch40, adc2

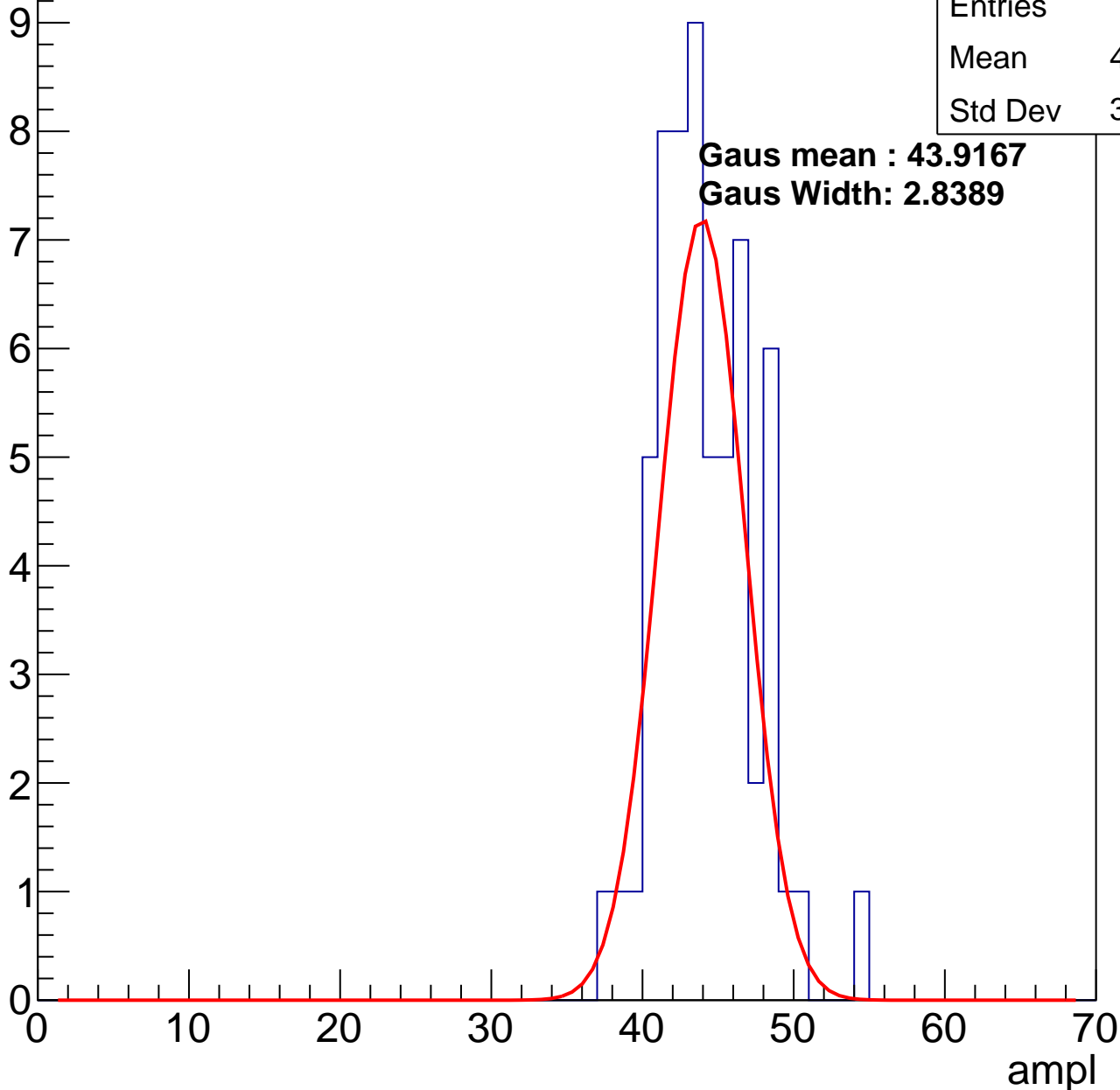
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	43.72
Std Dev	3.153

**Gaus mean : 43.9167**

**Gaus Width: 2.8389**

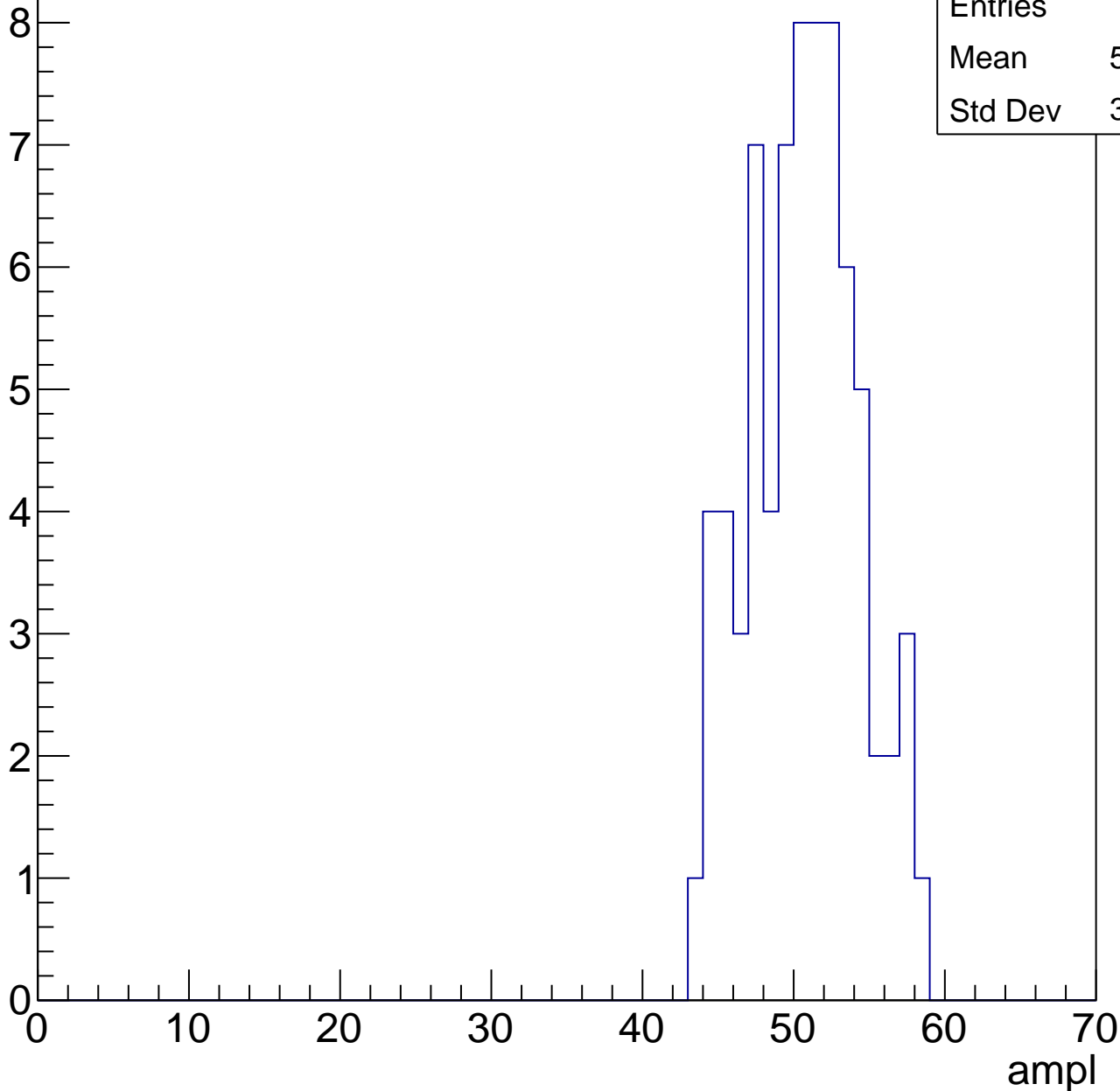


# B1L003S, U6-ch40, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	73
Mean	50.19
Std Dev	3.572

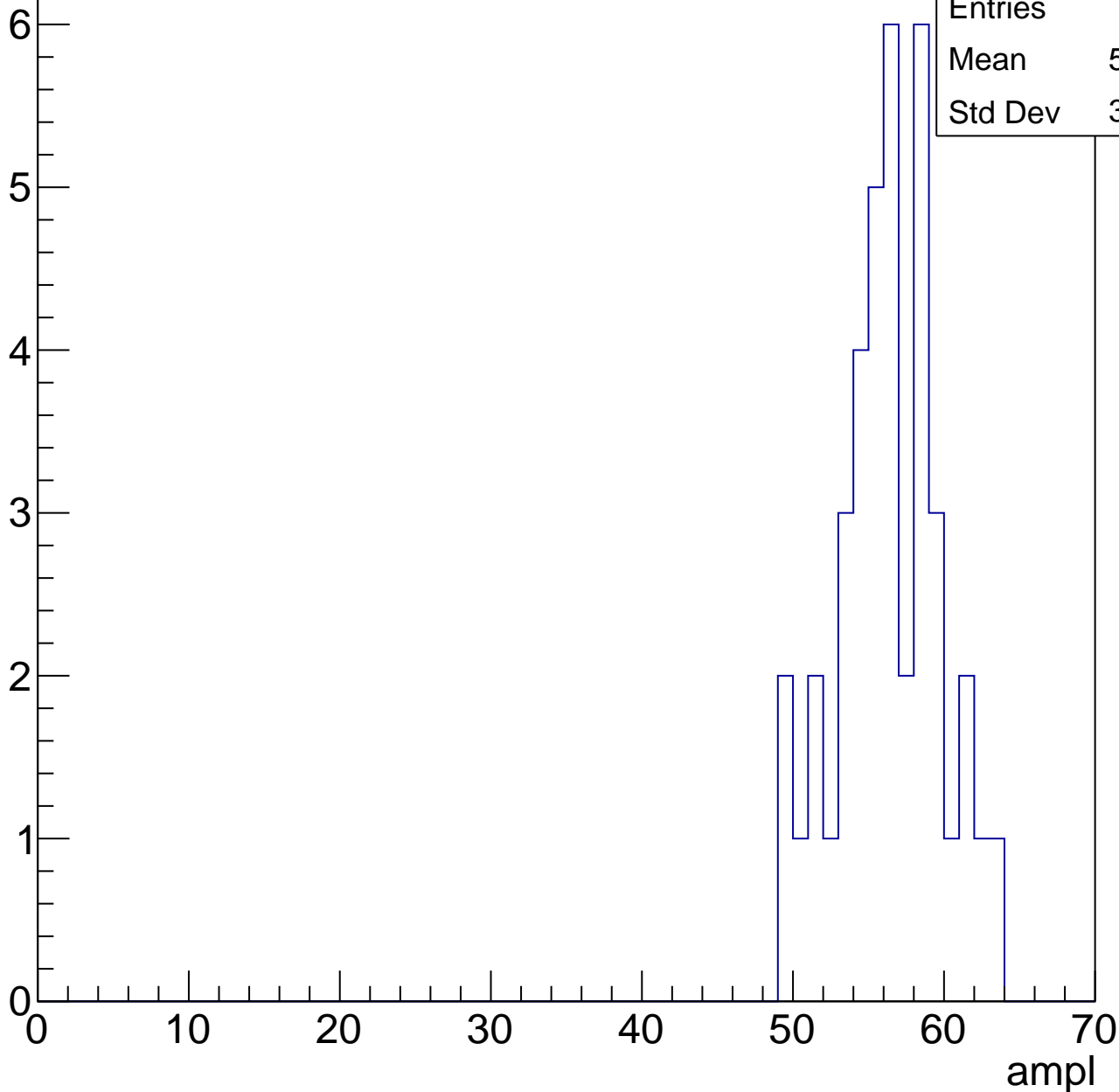


# B1L003S, U6-ch40, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	40
Mean	55.85
Std Dev	3.358

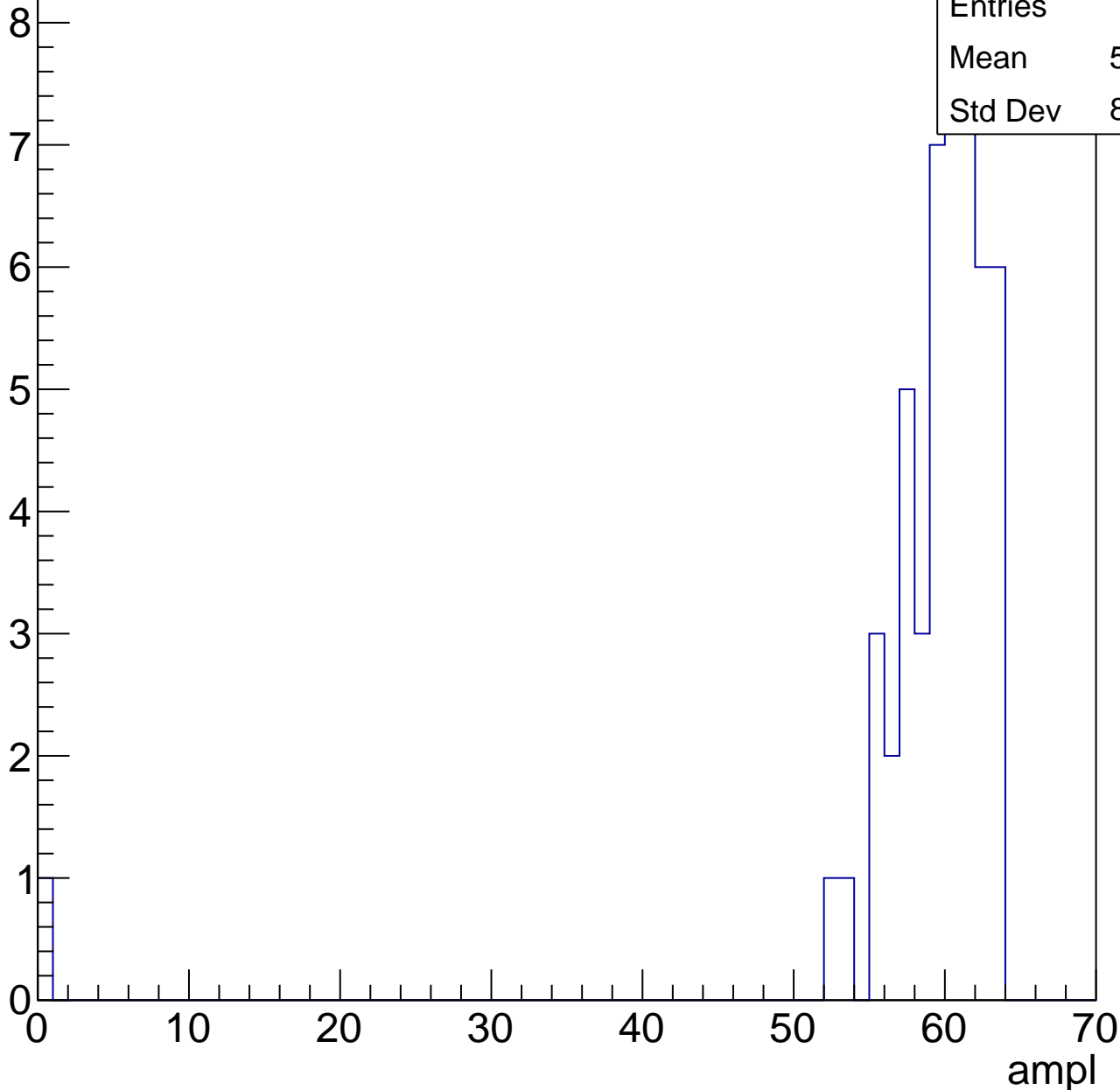


# B1L003S, U6-ch40, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

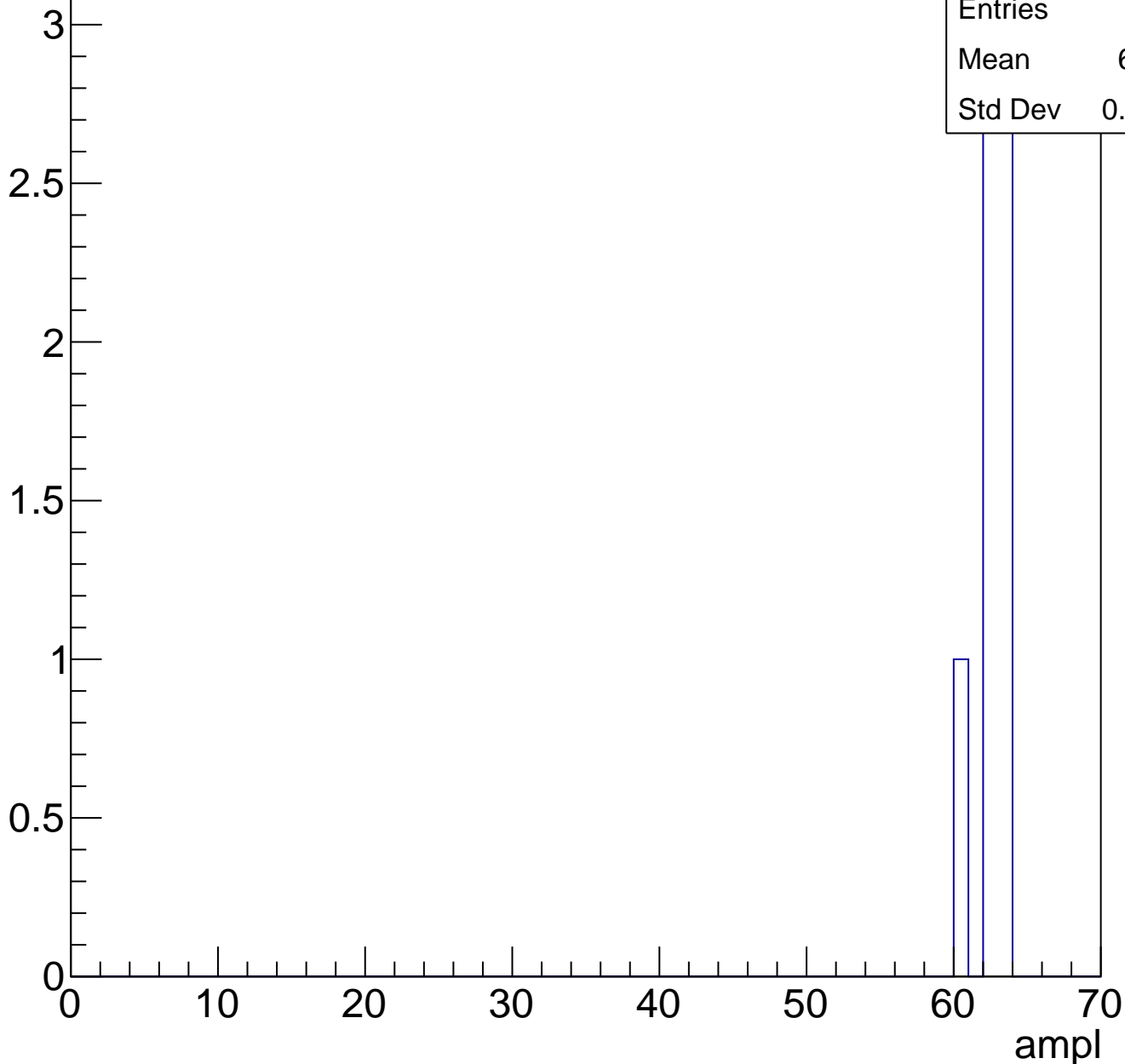
Entries	51
Mean	58.27
Std Dev	8.653



# B1L003S, U6-ch40, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch40, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch41, adc0

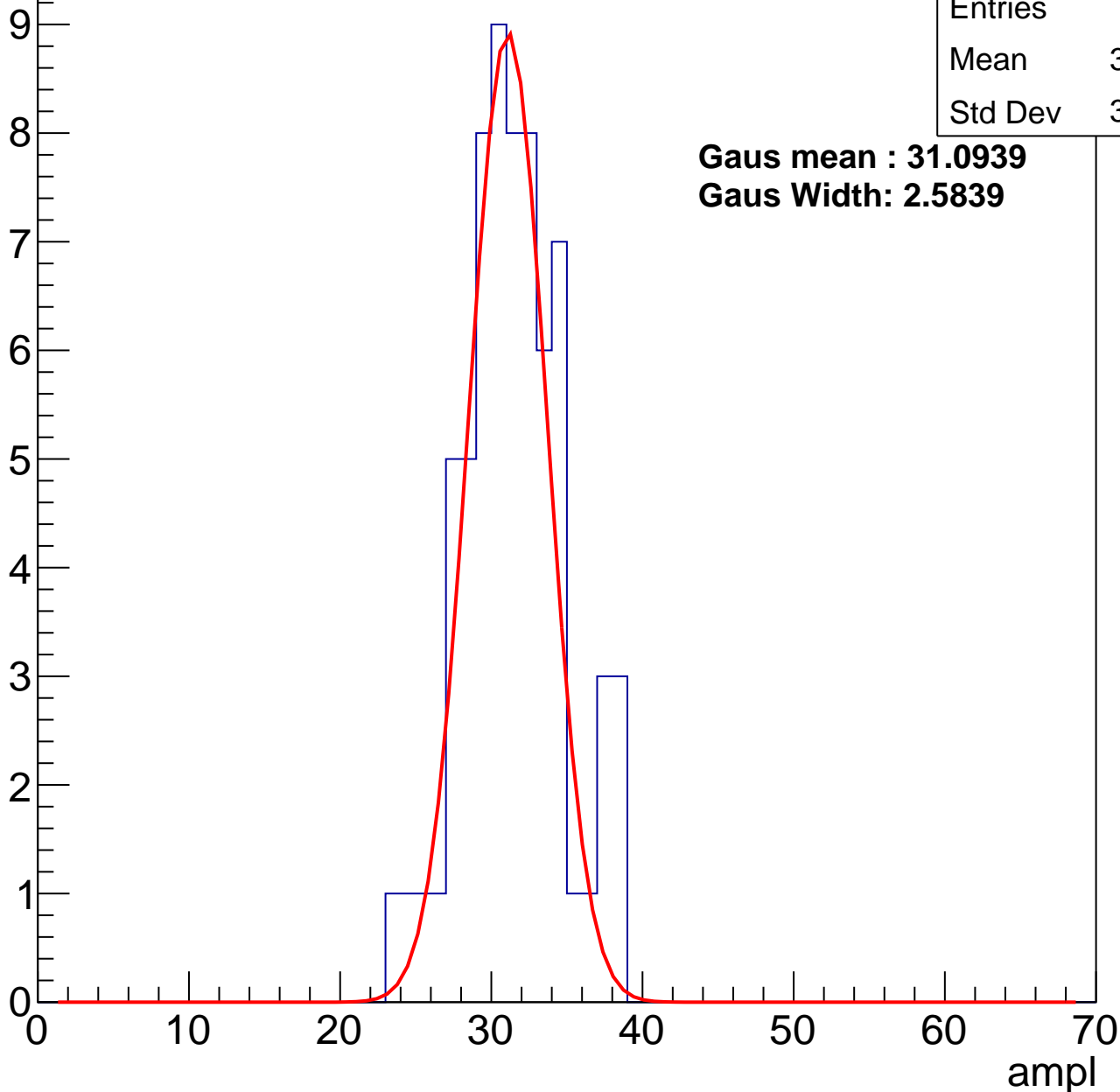
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	31.04
Std Dev	3.278

**Gaus mean : 31.0939**

**Gaus Width: 2.5839**



# B1L003S, U6-ch41, adc1

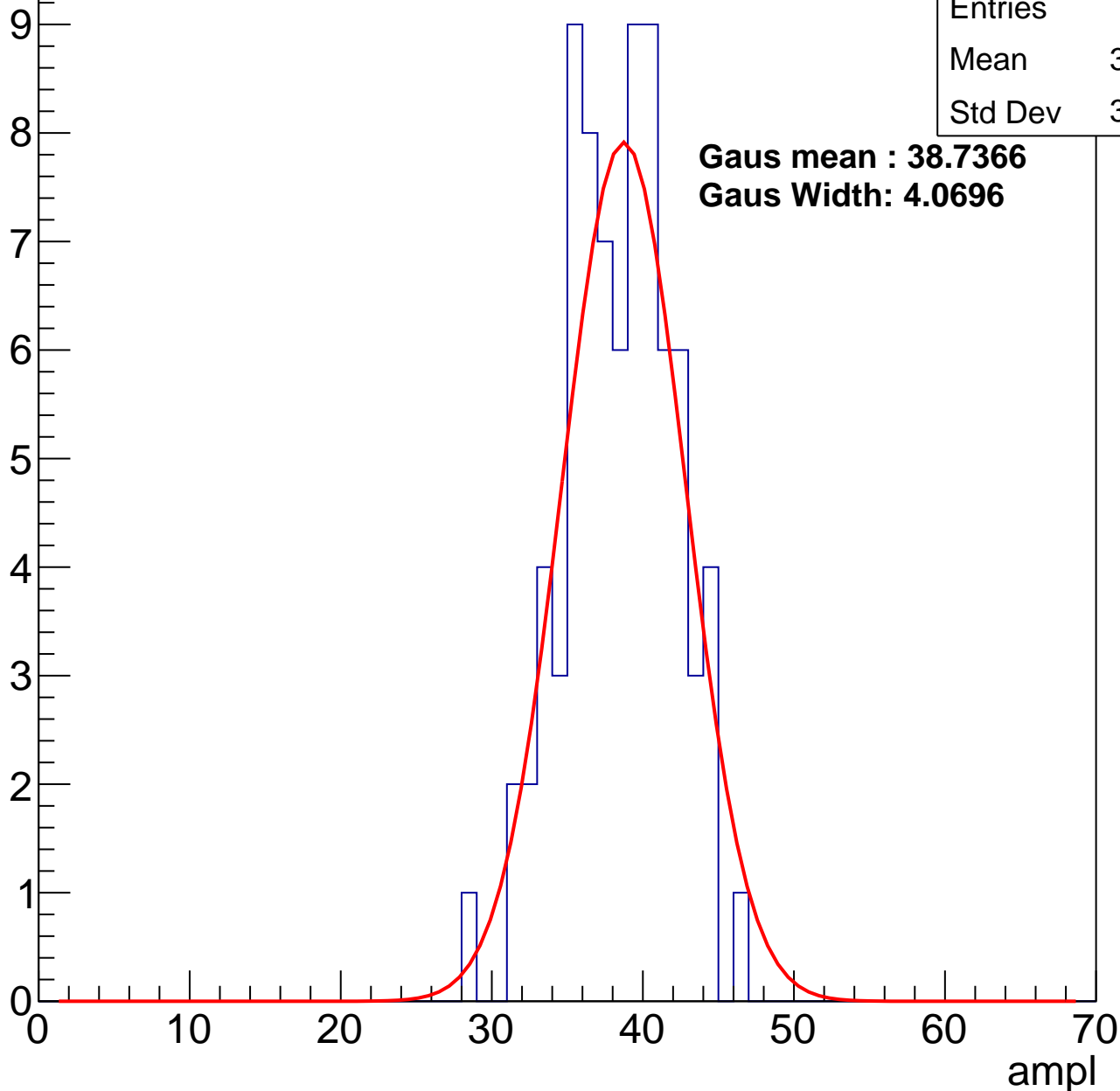
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	80
Mean	37.98
Std Dev	3.564

**Gaus mean : 38.7366**

**Gaus Width: 4.0696**



# B1L003S, U6-ch41, adc2

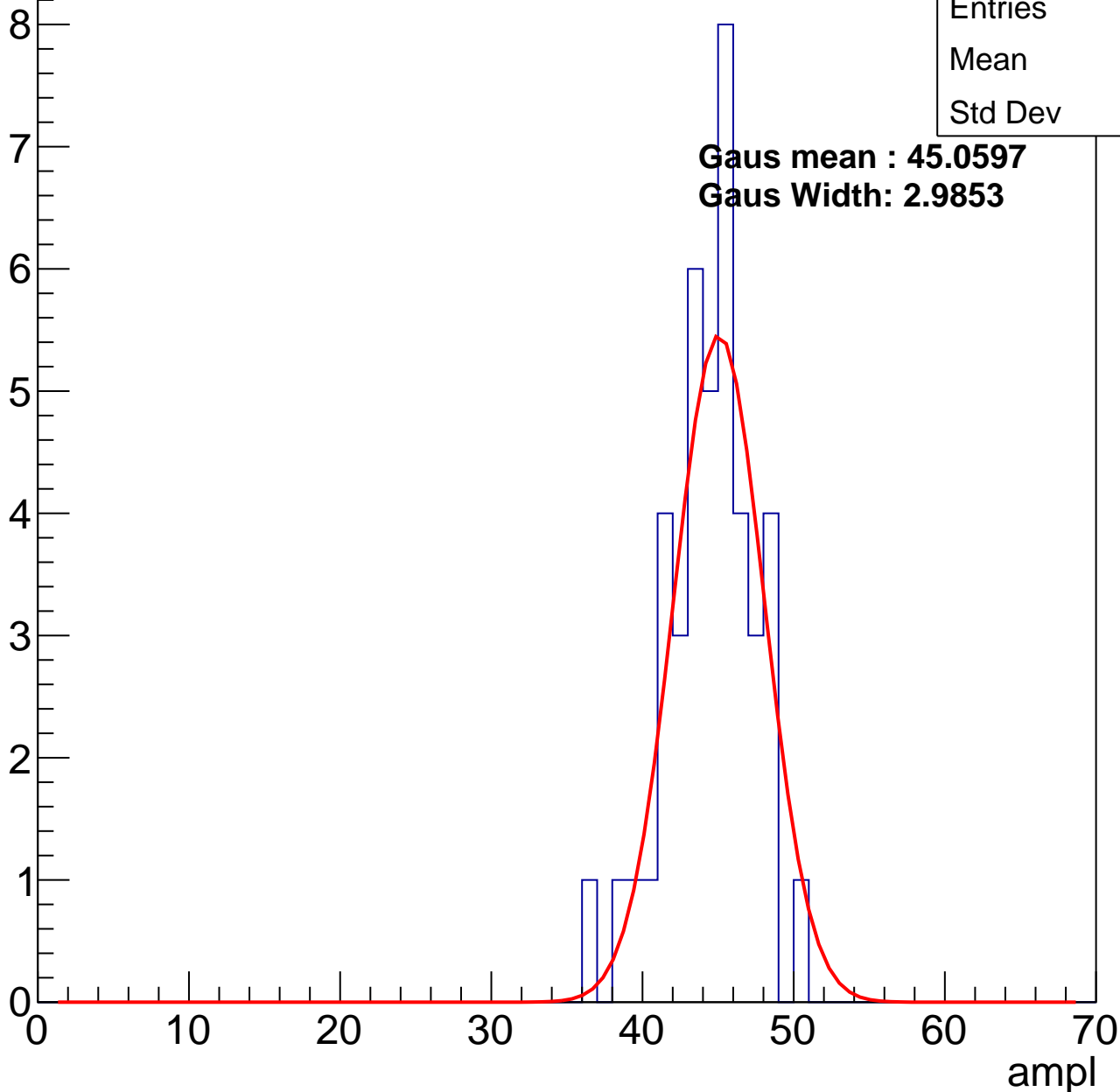
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	42
Mean	44
Std Dev	2.87

**Gaus mean : 45.0597**

**Gaus Width: 2.9853**



# B1L003S, U6-ch41, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

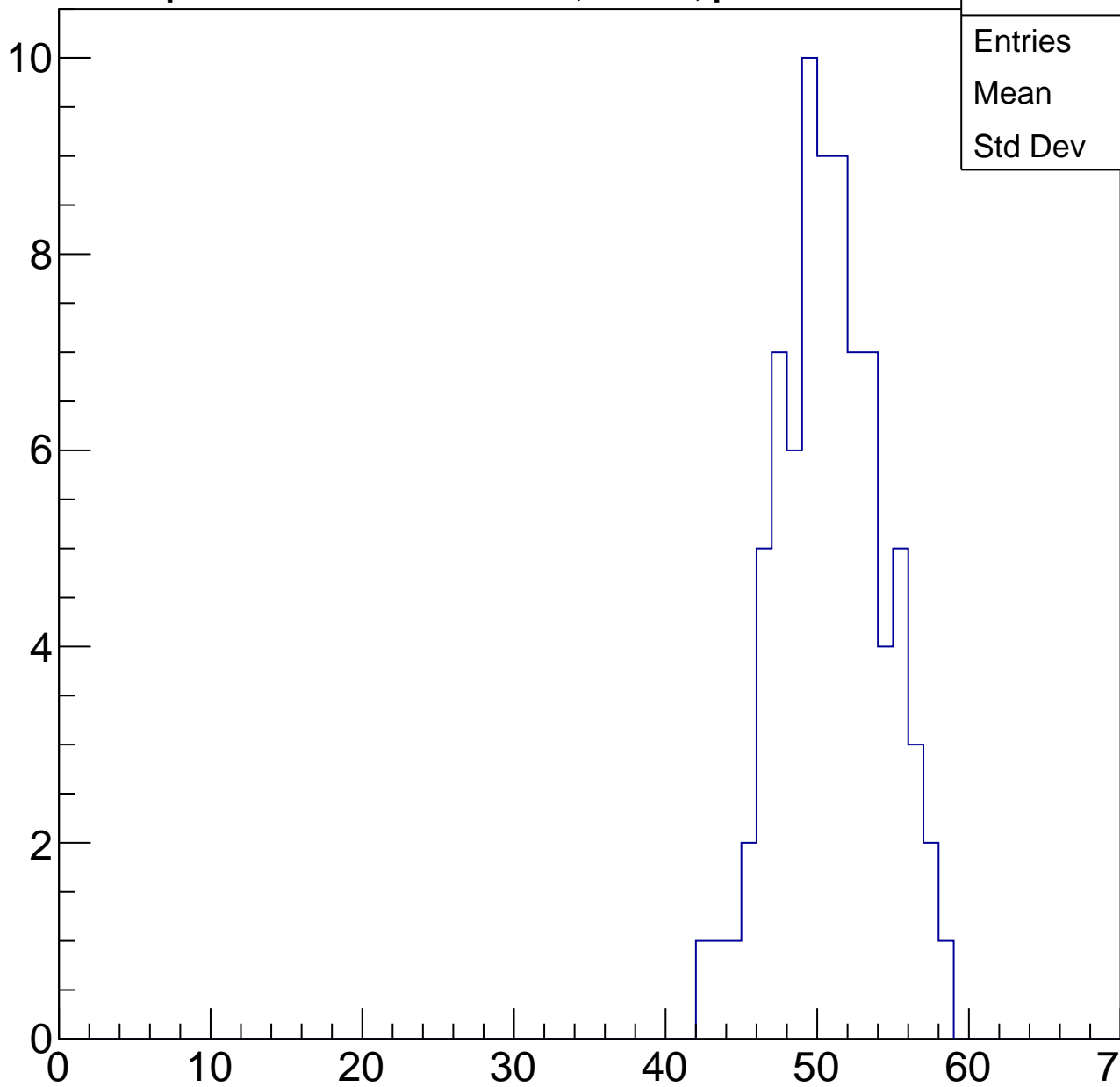
Entries	80
Mean	50.39
Std Dev	3.397

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

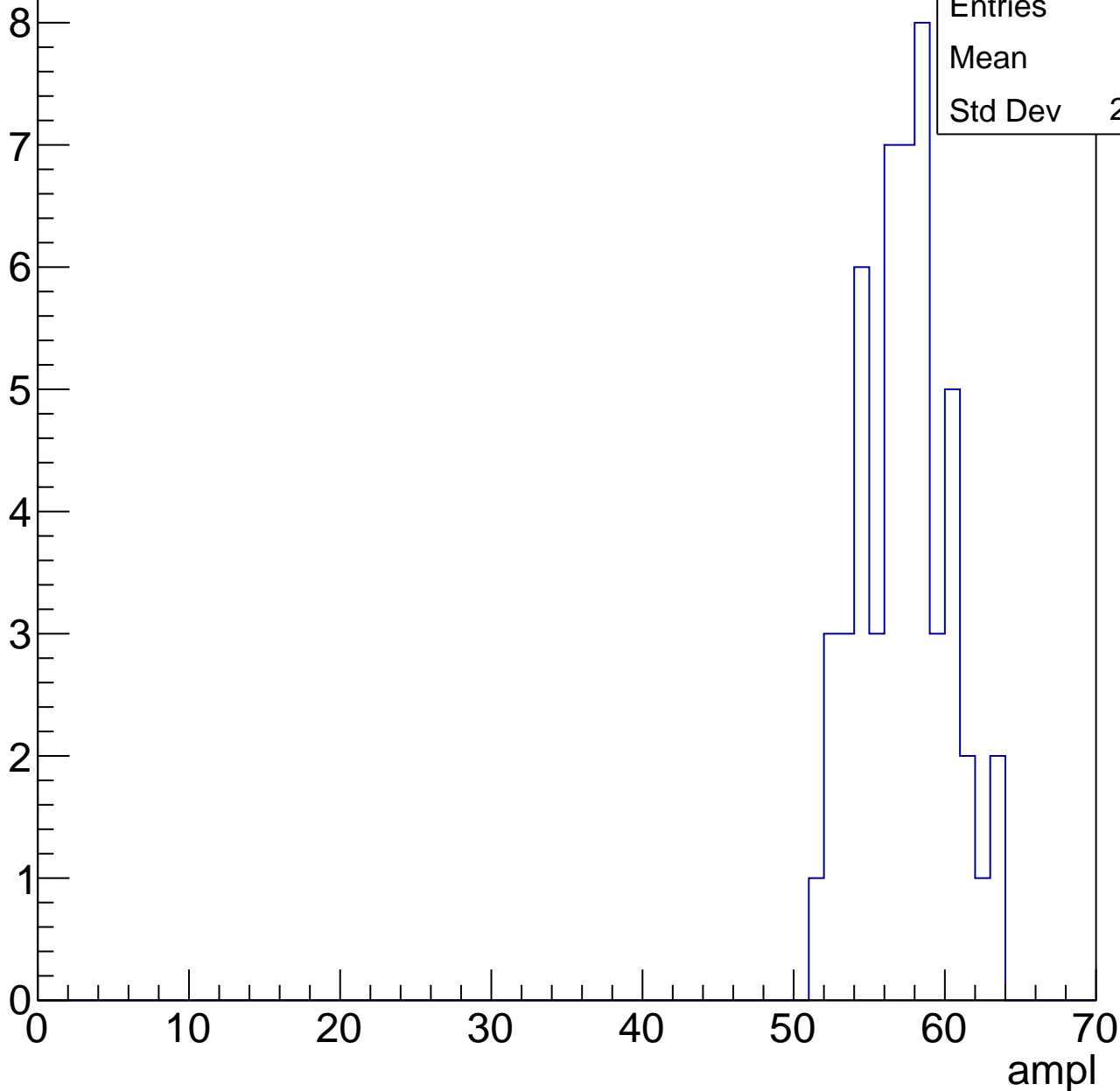


# B1L003S, U6-ch41, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	51
Mean	56.8
Std Dev	2.883

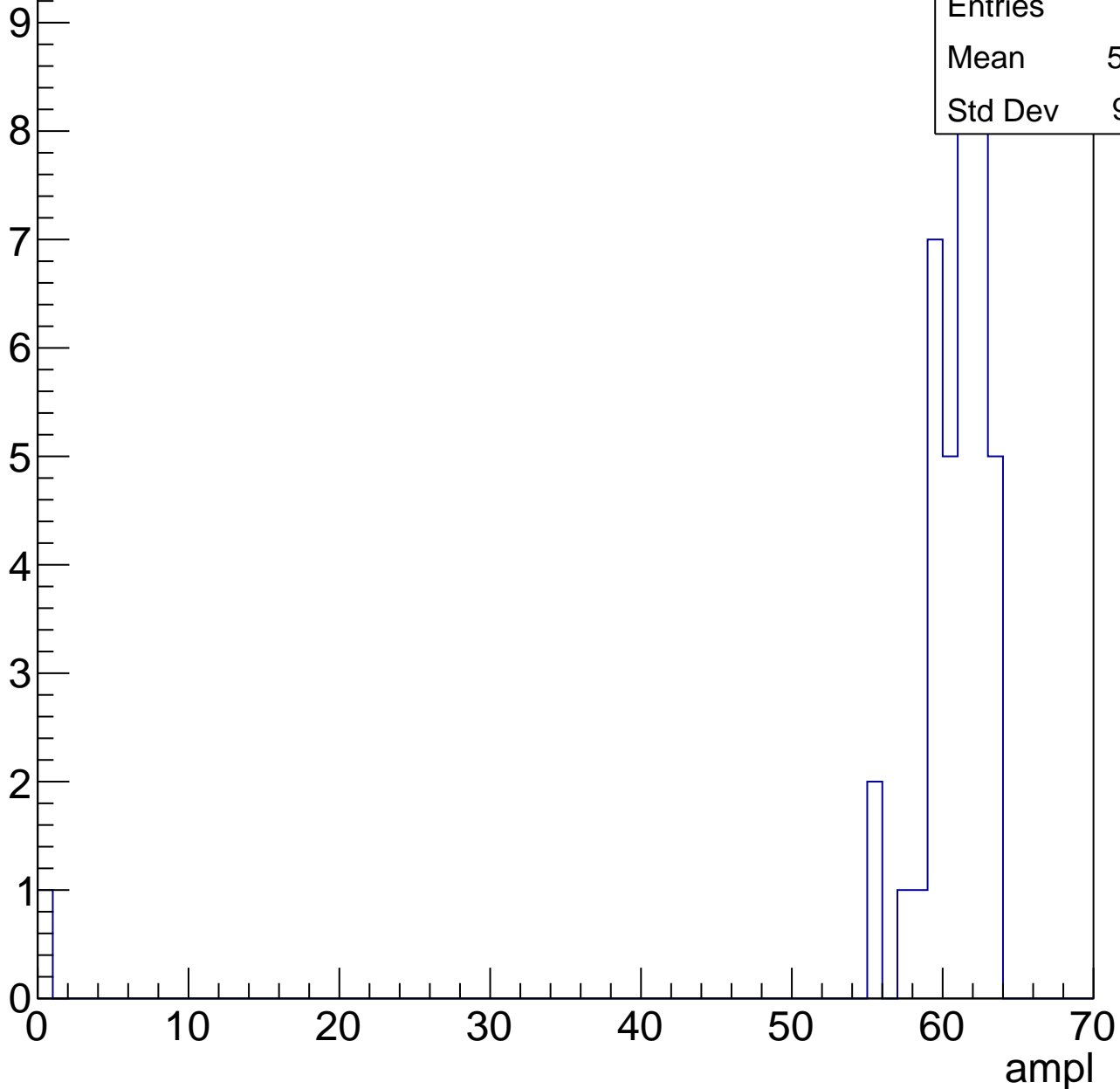


# B1L003S, U6-ch41, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	39
Mean	58.95
Std Dev	9.761



# B1L003S, U6-ch41, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch41, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch42, adc0

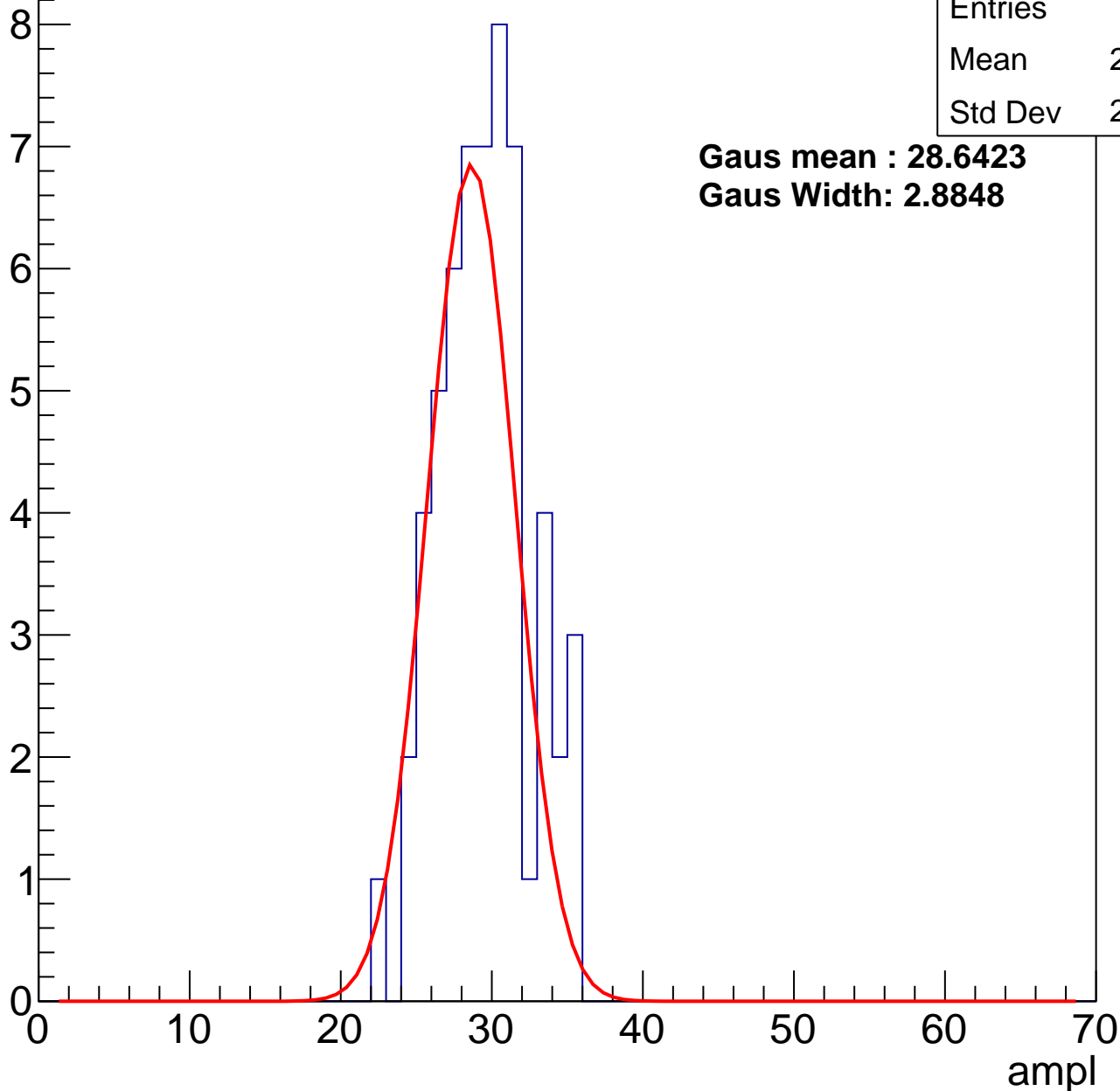
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	29.04
Std Dev	2.979

**Gaus mean : 28.6423**

**Gaus Width: 2.8848**



# B1L003S, U6-ch42, adc1

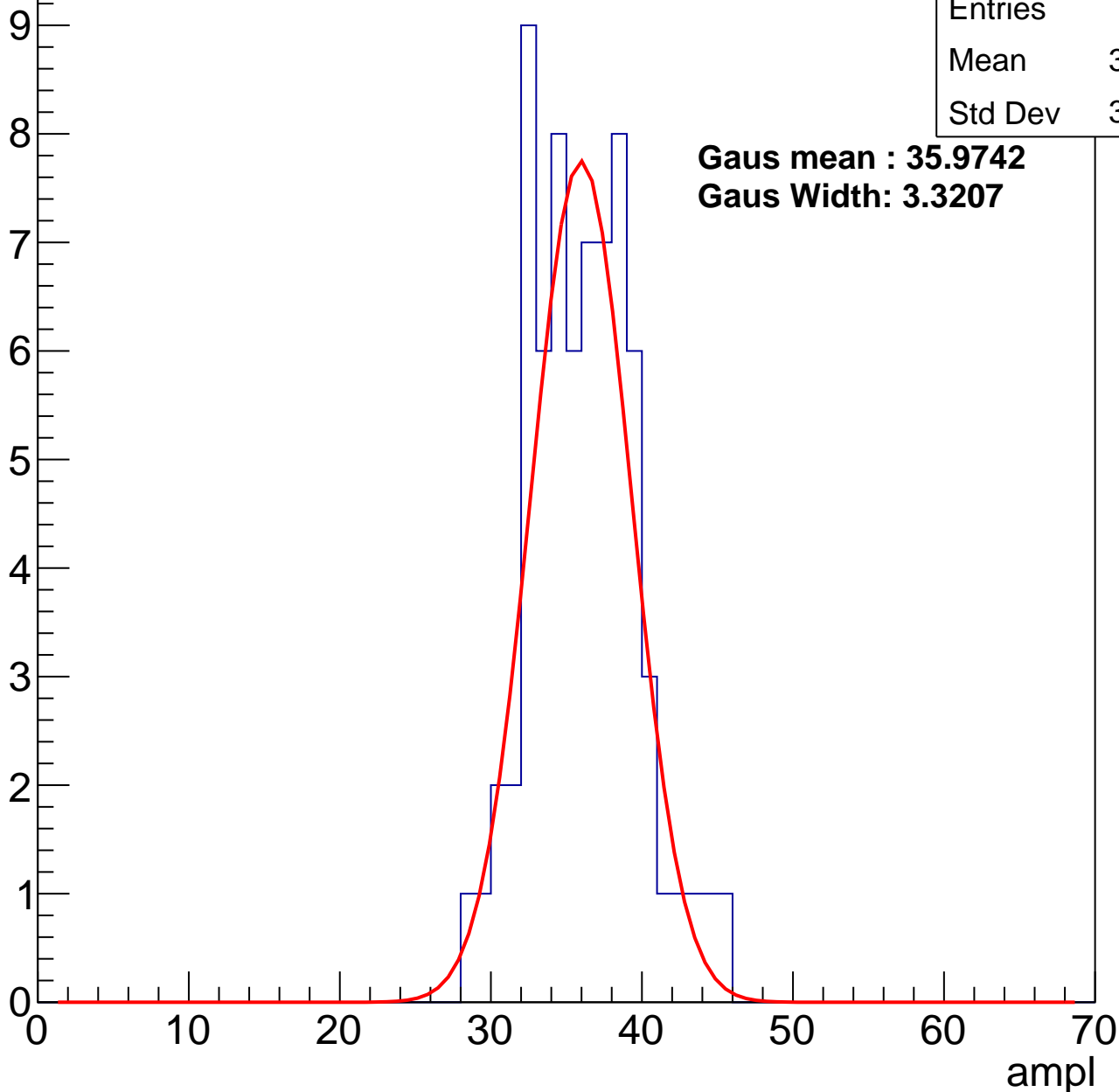
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	71
Mean	35.65
Std Dev	3.477

**Gaus mean : 35.9742**

**Gaus Width: 3.3207**



# B1L003S, U6-ch42, adc2

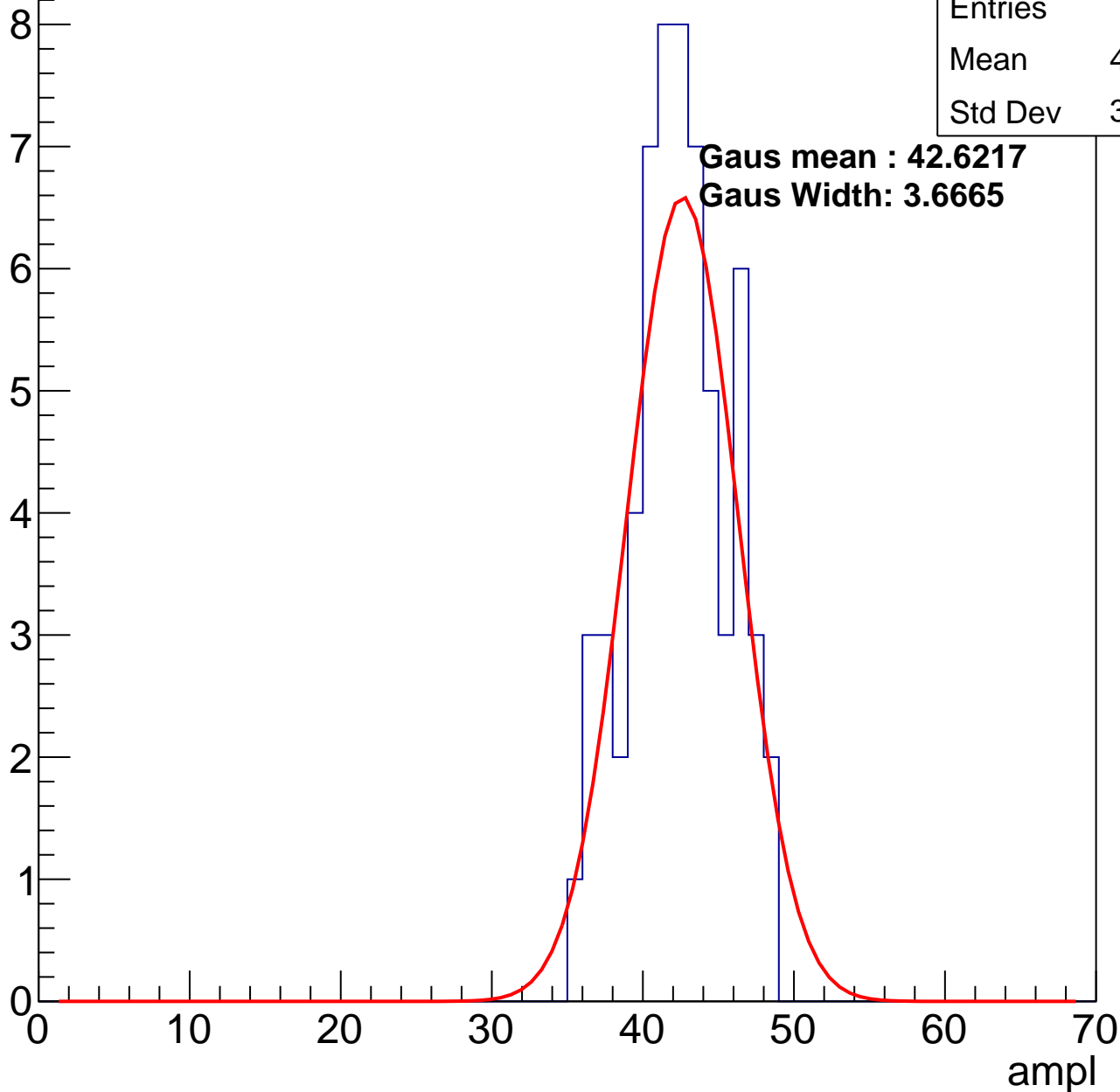
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	41.92
Std Dev	3.194

**Gaus mean : 42.6217**

**Gaus Width: 3.6665**

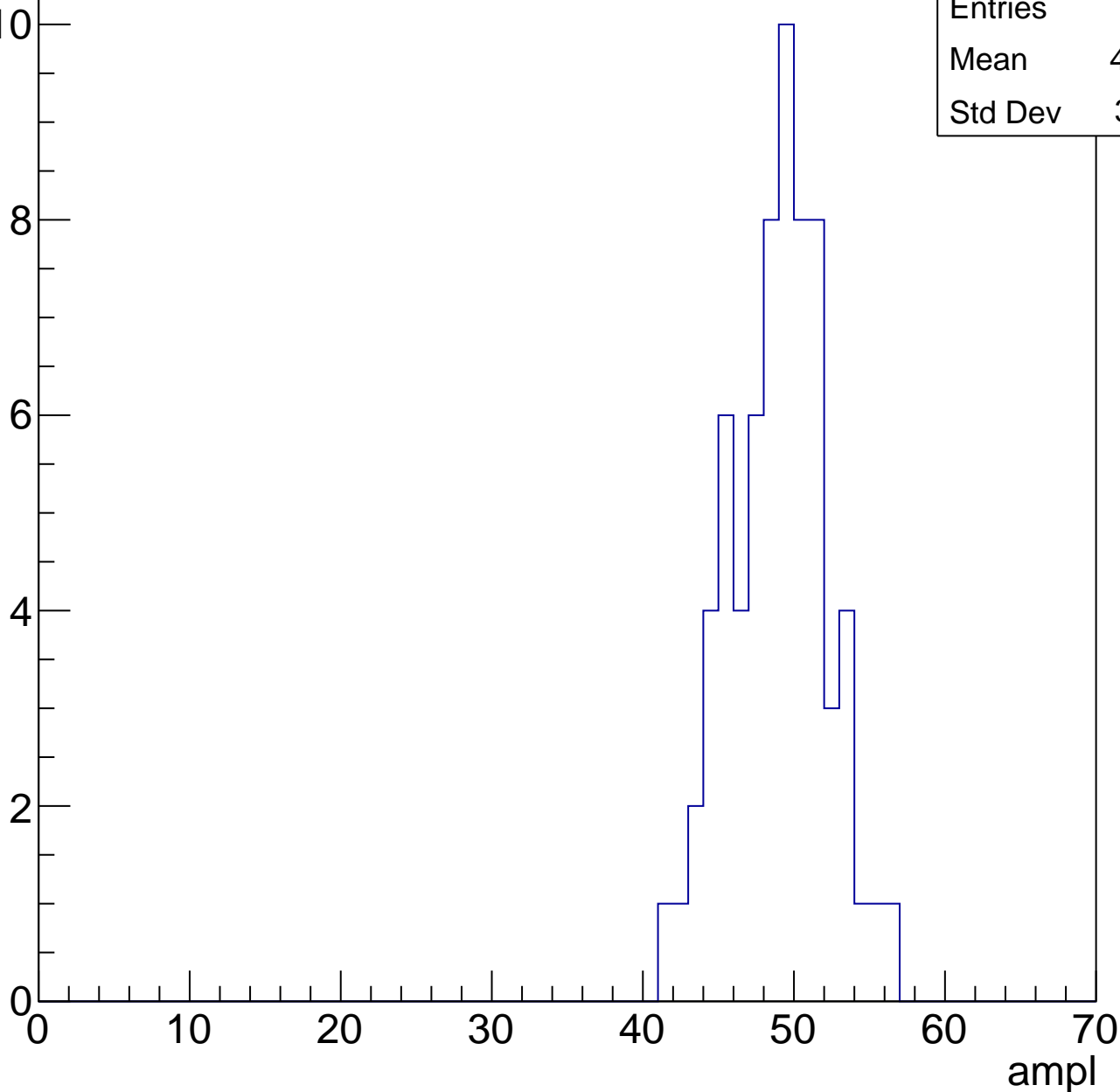


# B1L003S, U6-ch42, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

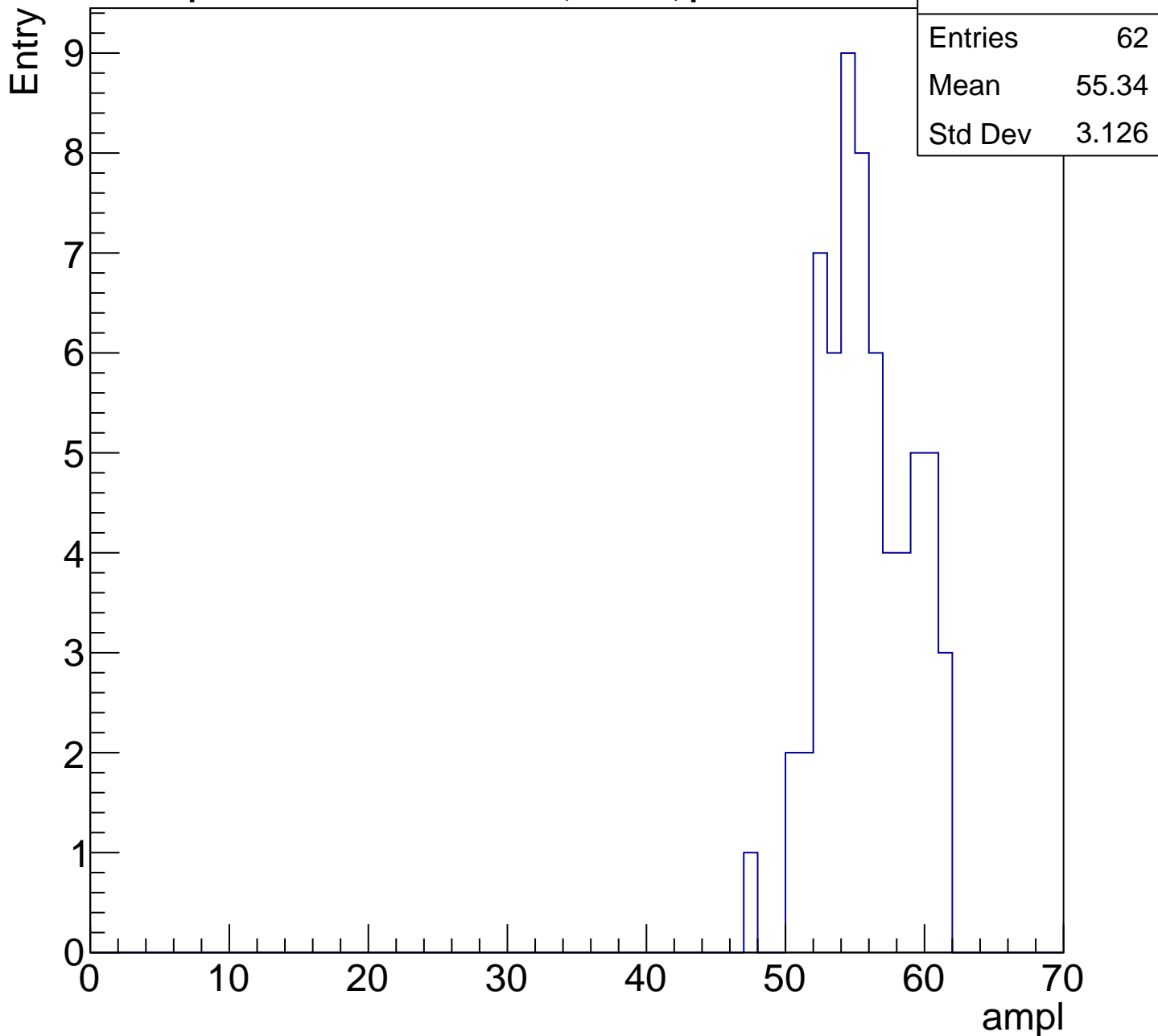
Entry

Entries	68
Mean	48.47
Std Dev	3.141



# B1L003S, U6-ch42, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

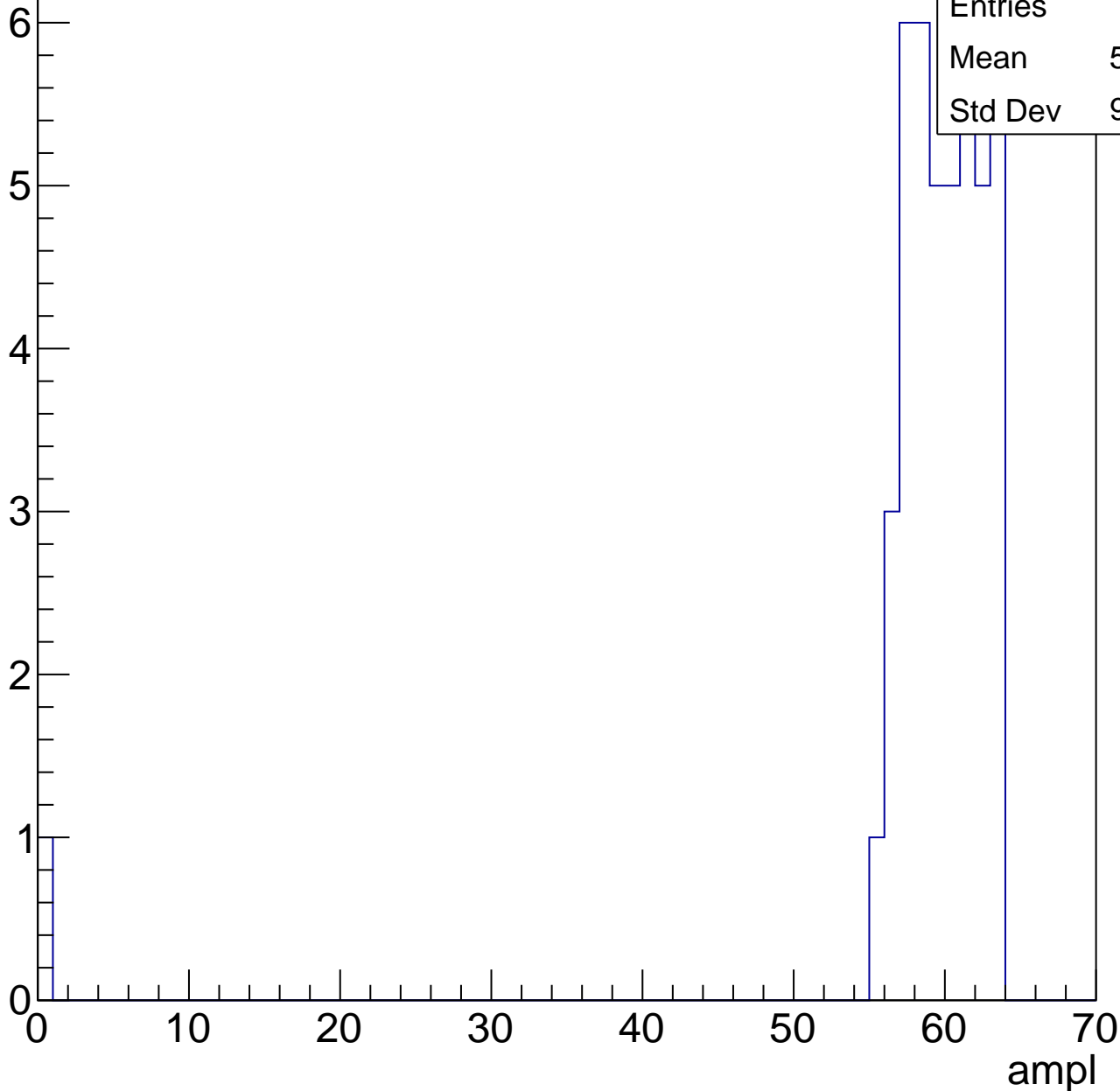


# B1L003S, U6-ch42, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

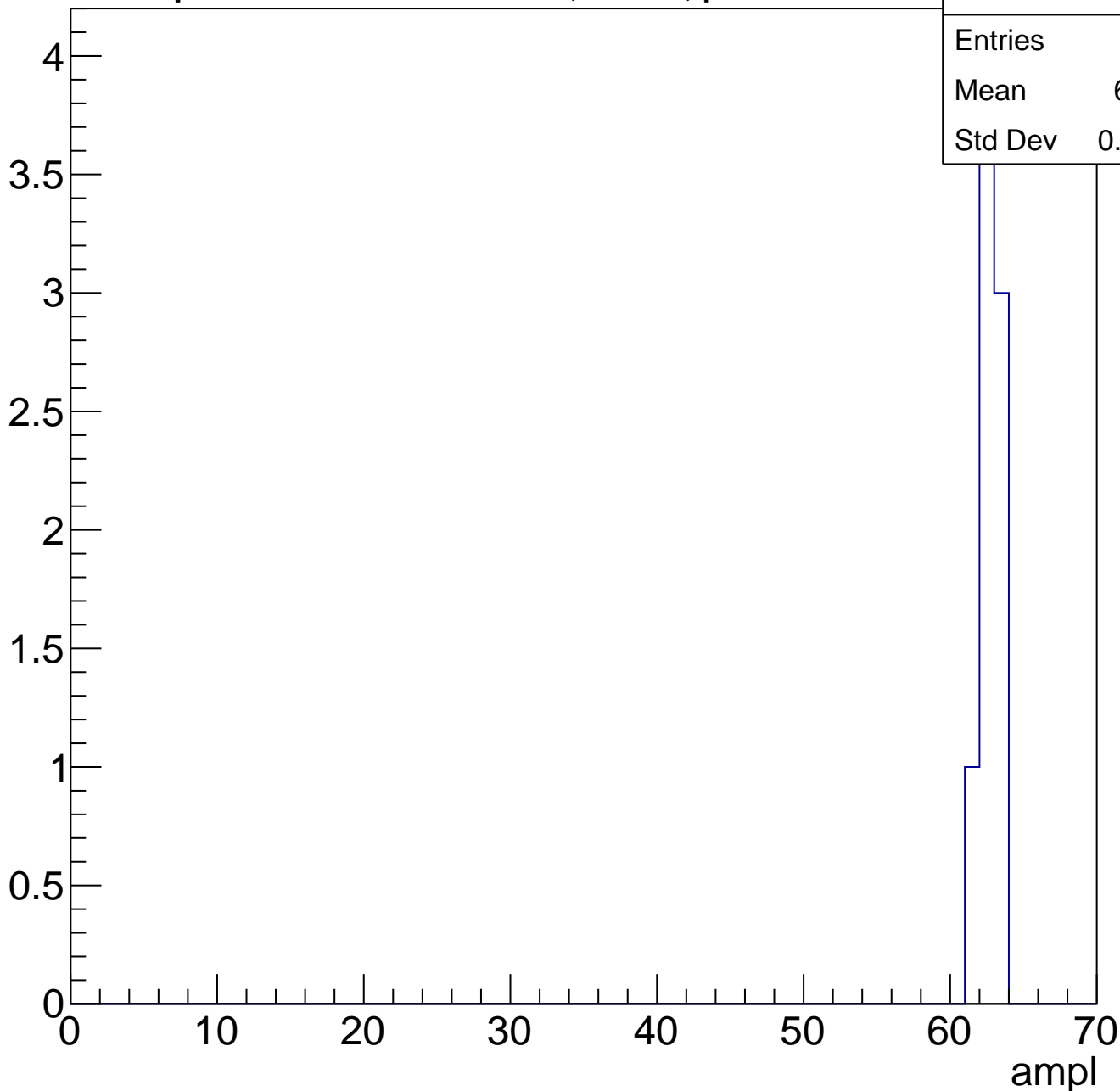
Entries	44
Mean	58.23
Std Dev	9.167



# B1L003S, U6-ch42, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

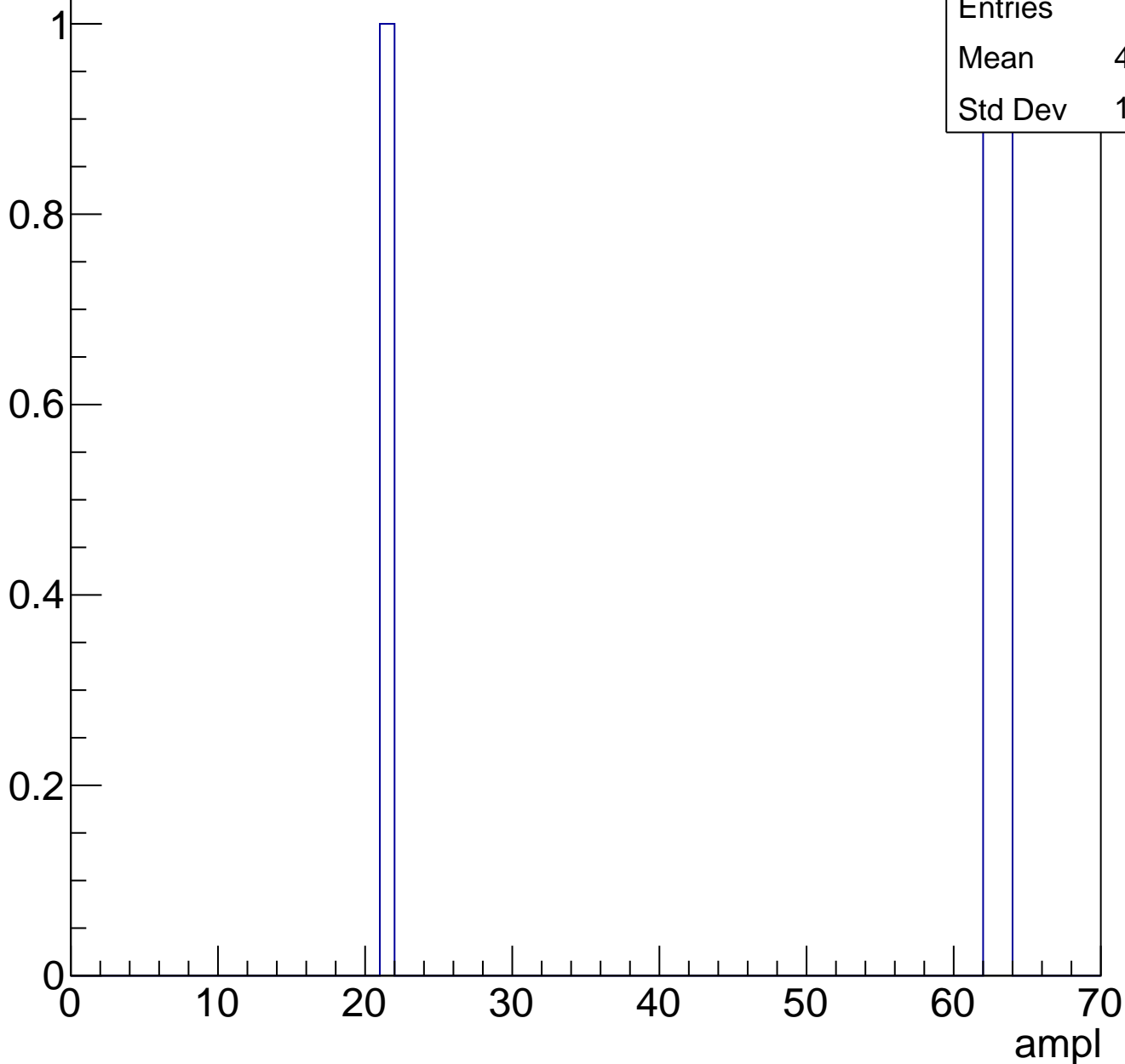




# B1L003S, U6-ch42, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch43, adc0

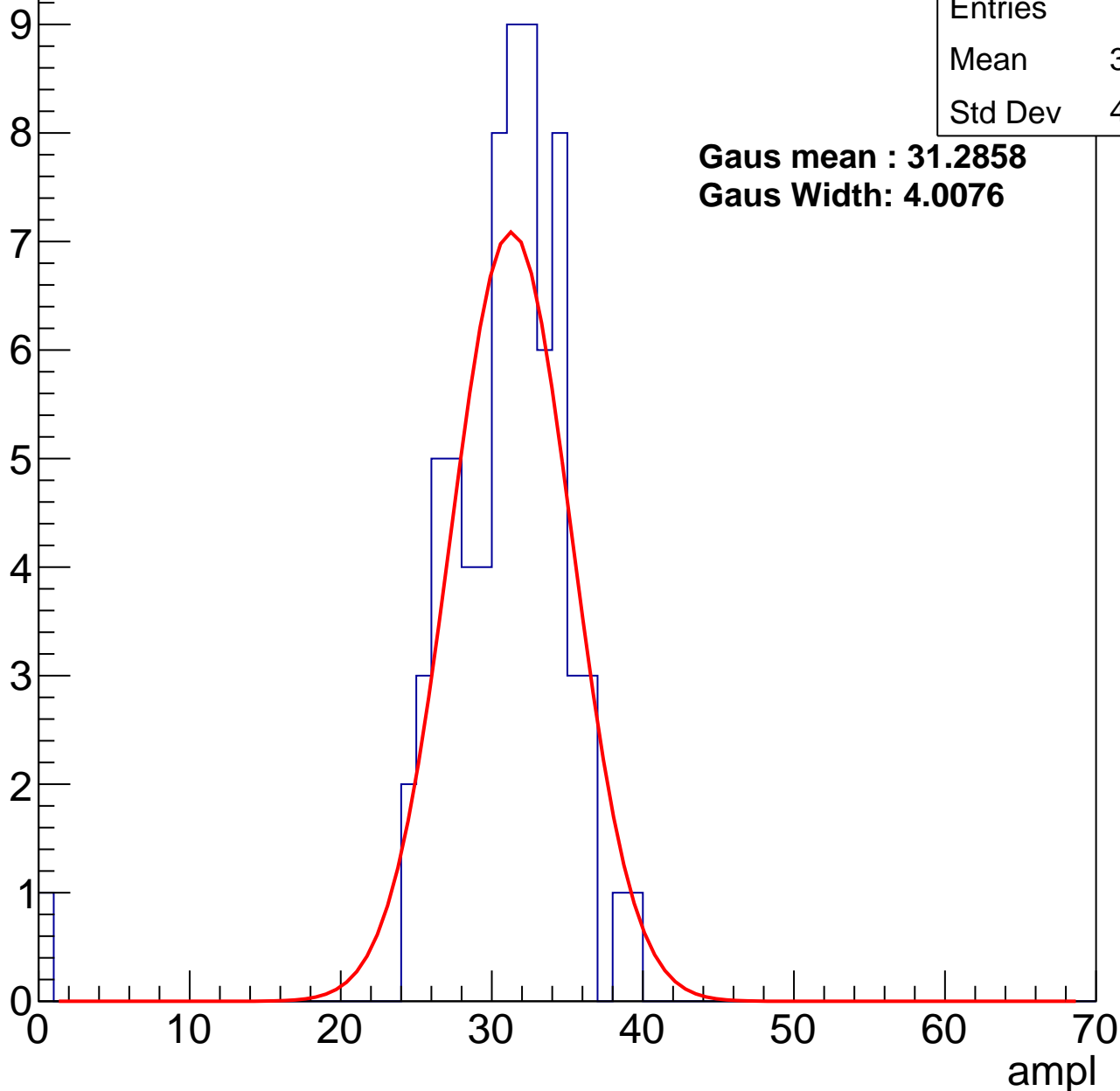
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	72
Mean	30.32
Std Dev	4.915

**Gaus mean : 31.2858**

**Gaus Width: 4.0076**



# B1L003S, U6-ch43, adc1

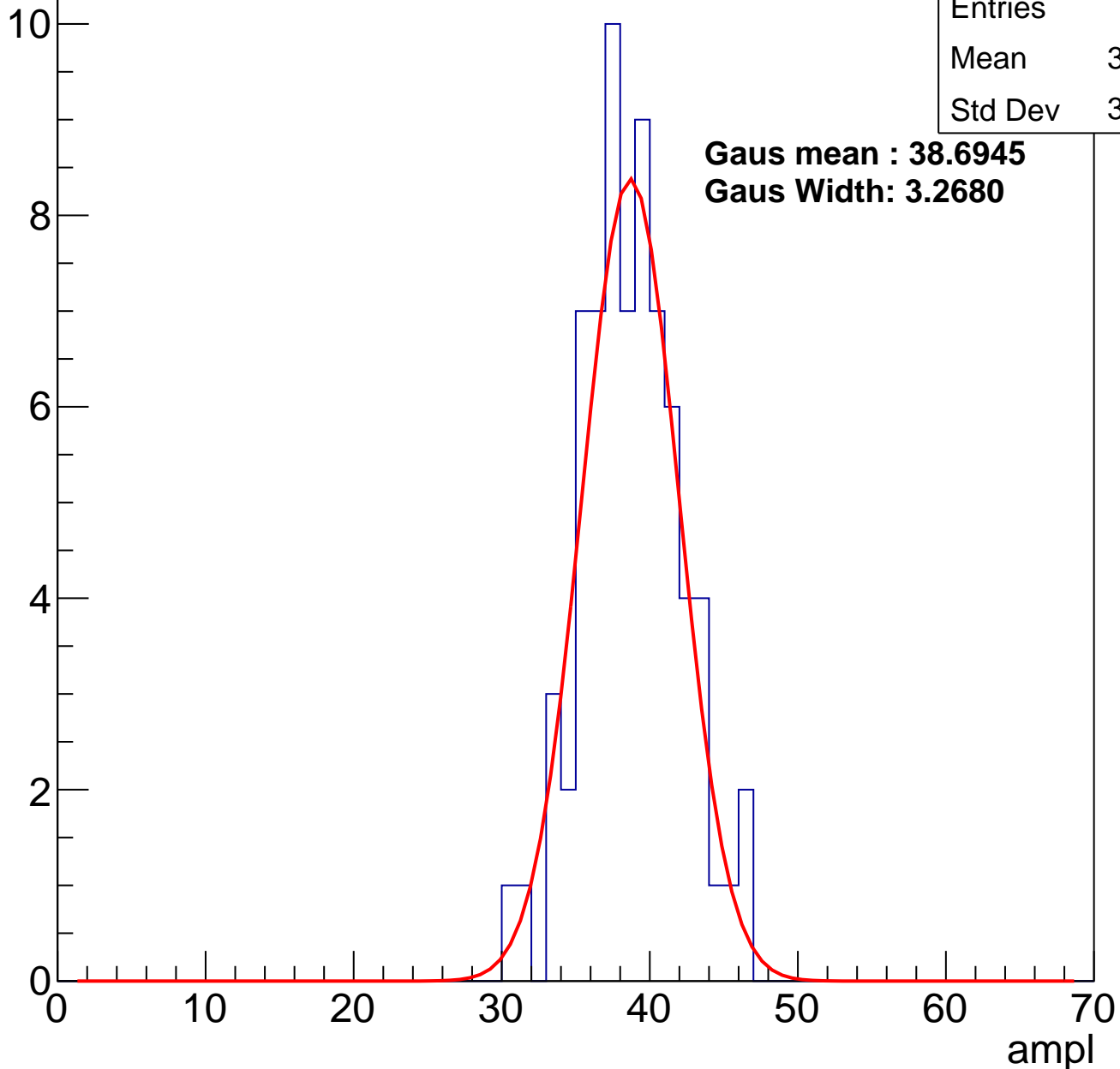
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	72
Mean	38.32
Std Dev	3.295

**Gaus mean : 38.6945**

**Gaus Width: 3.2680**

Entry



# B1L003S, U6-ch43, adc2

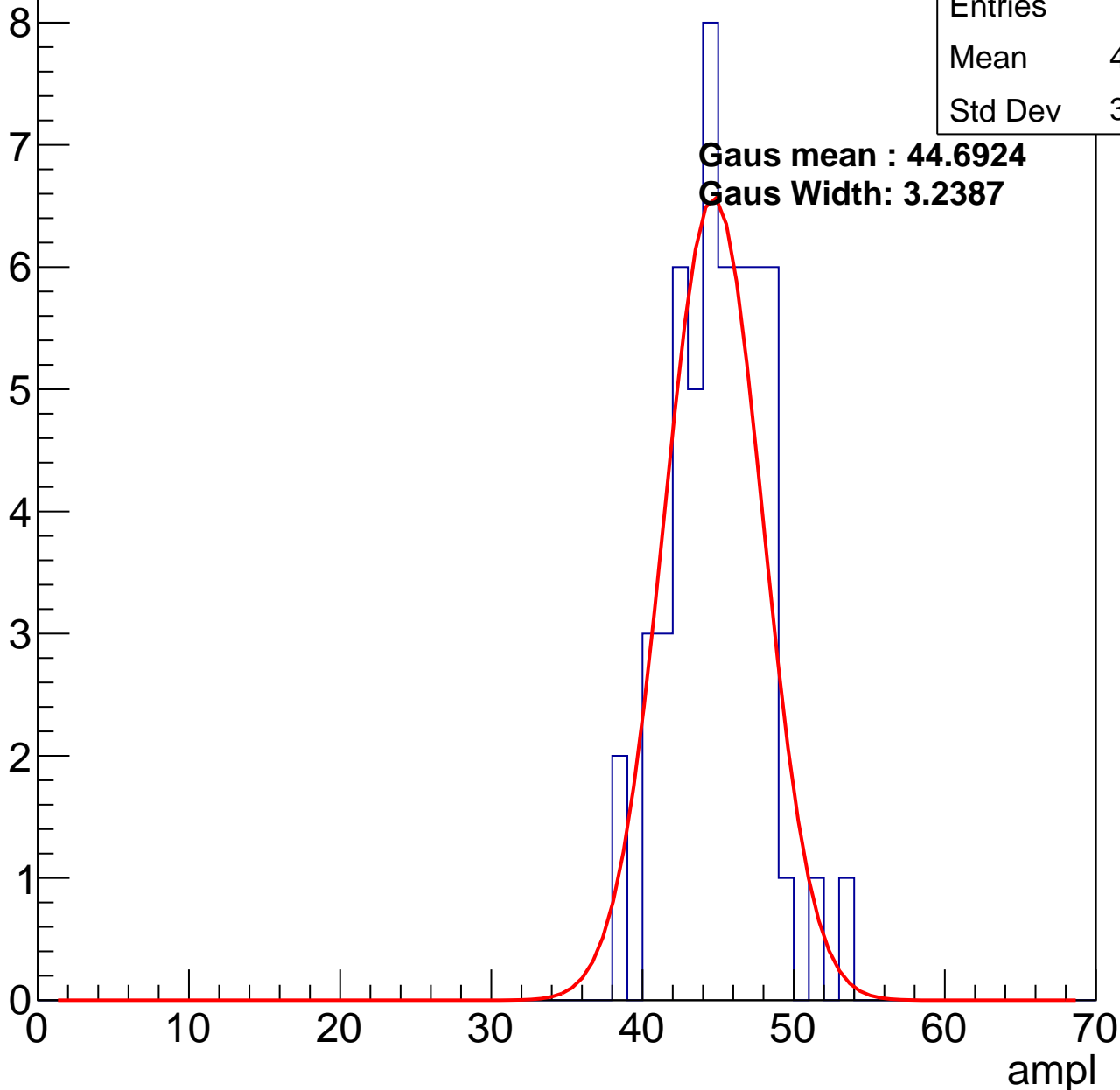
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	54
Mean	44.57
Std Dev	3.022

**Gaus mean : 44.6924**

**Gaus Width: 3.2387**

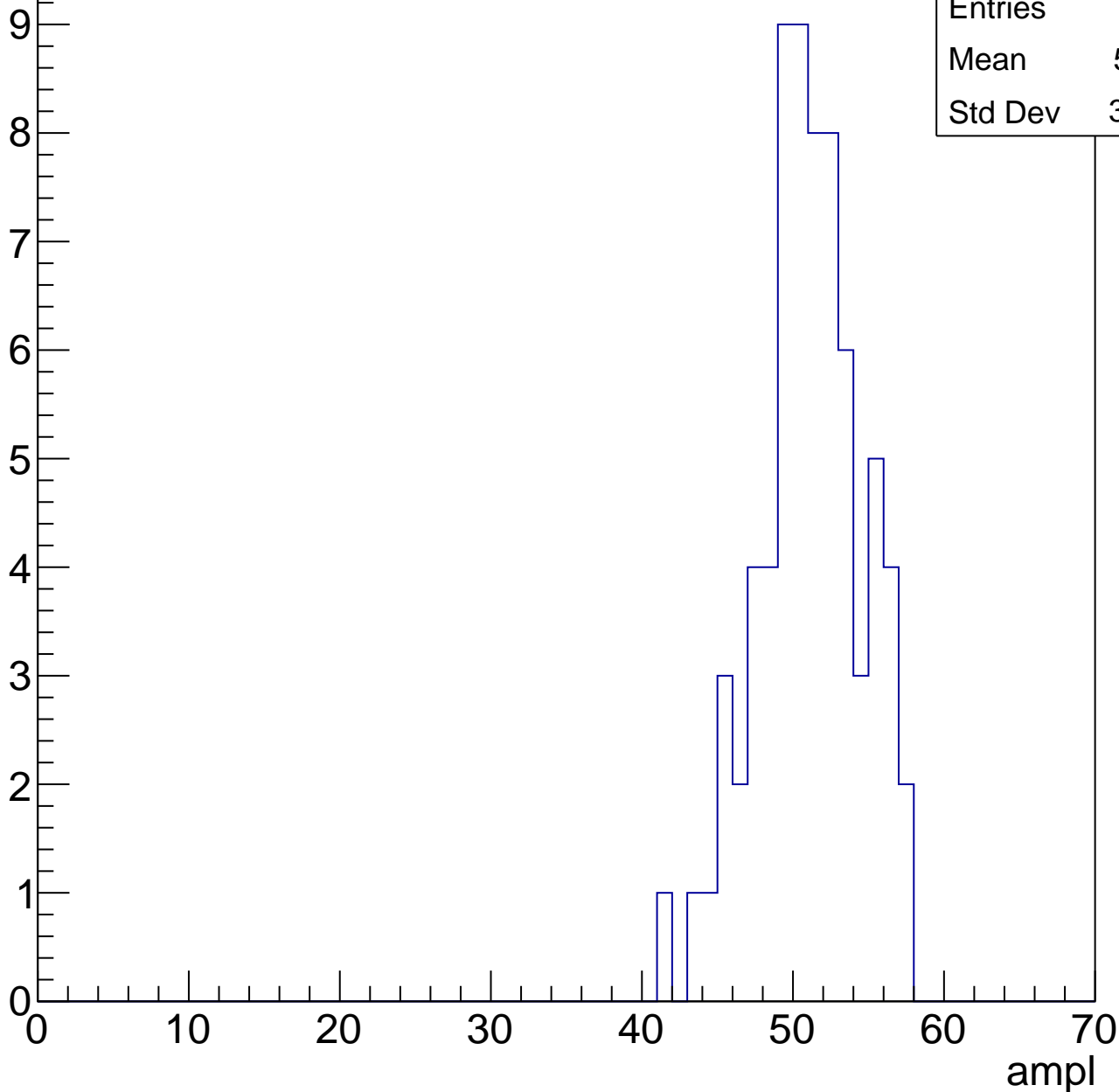


# B1L003S, U6-ch43, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	50.61
Std Dev	3.415

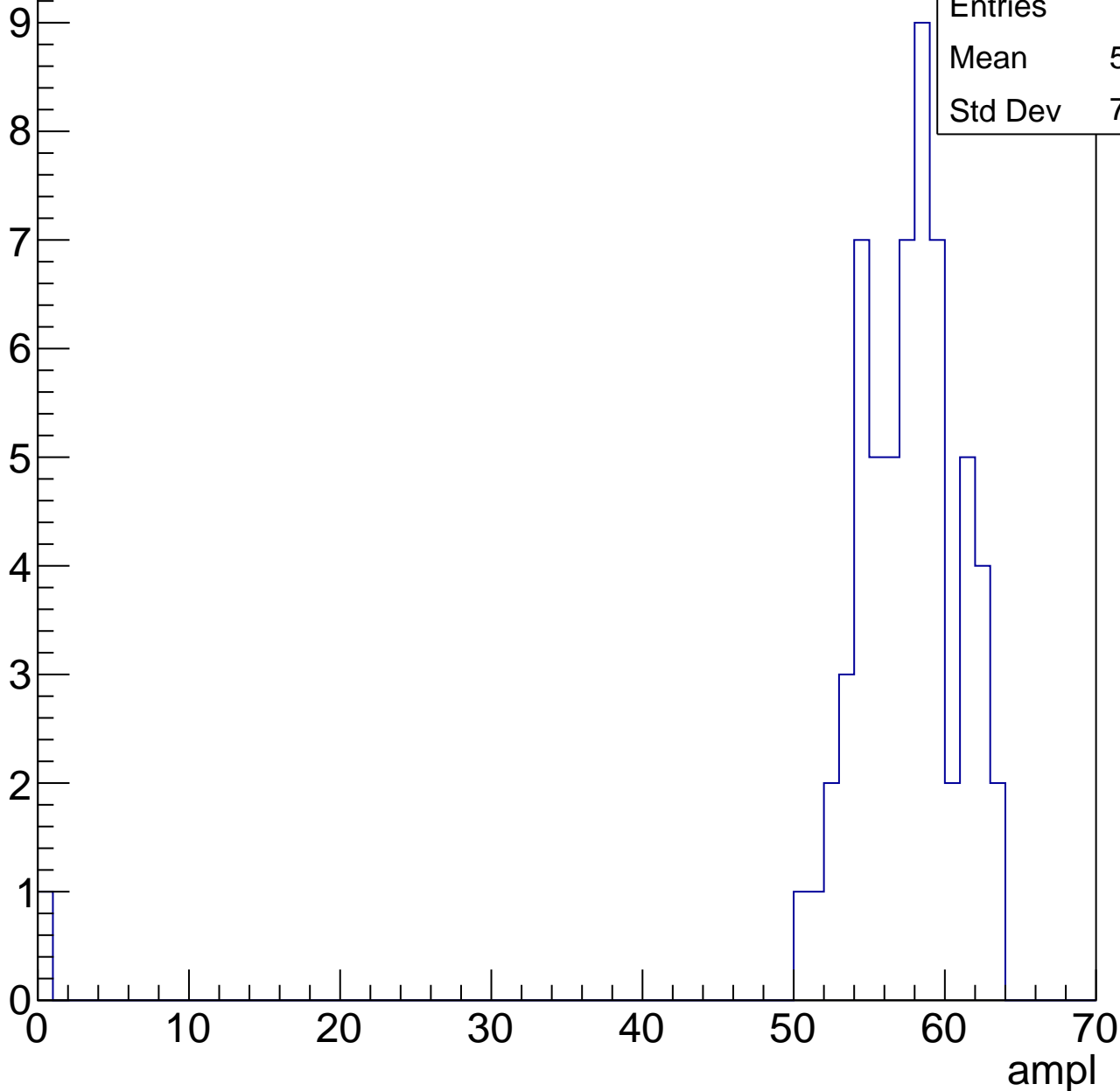


# B1L003S, U6-ch43, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	56.23
Std Dev	7.883



# B1L003S, U6-ch43, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	31
Mean	60.81
Std Dev	1.821

ampl

0 10 20 30 40 50 60 70

0

1

2

3

4

5

6

7

8

# B1L003S, U6-ch43, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch43, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L003S, U6-ch44, adc0

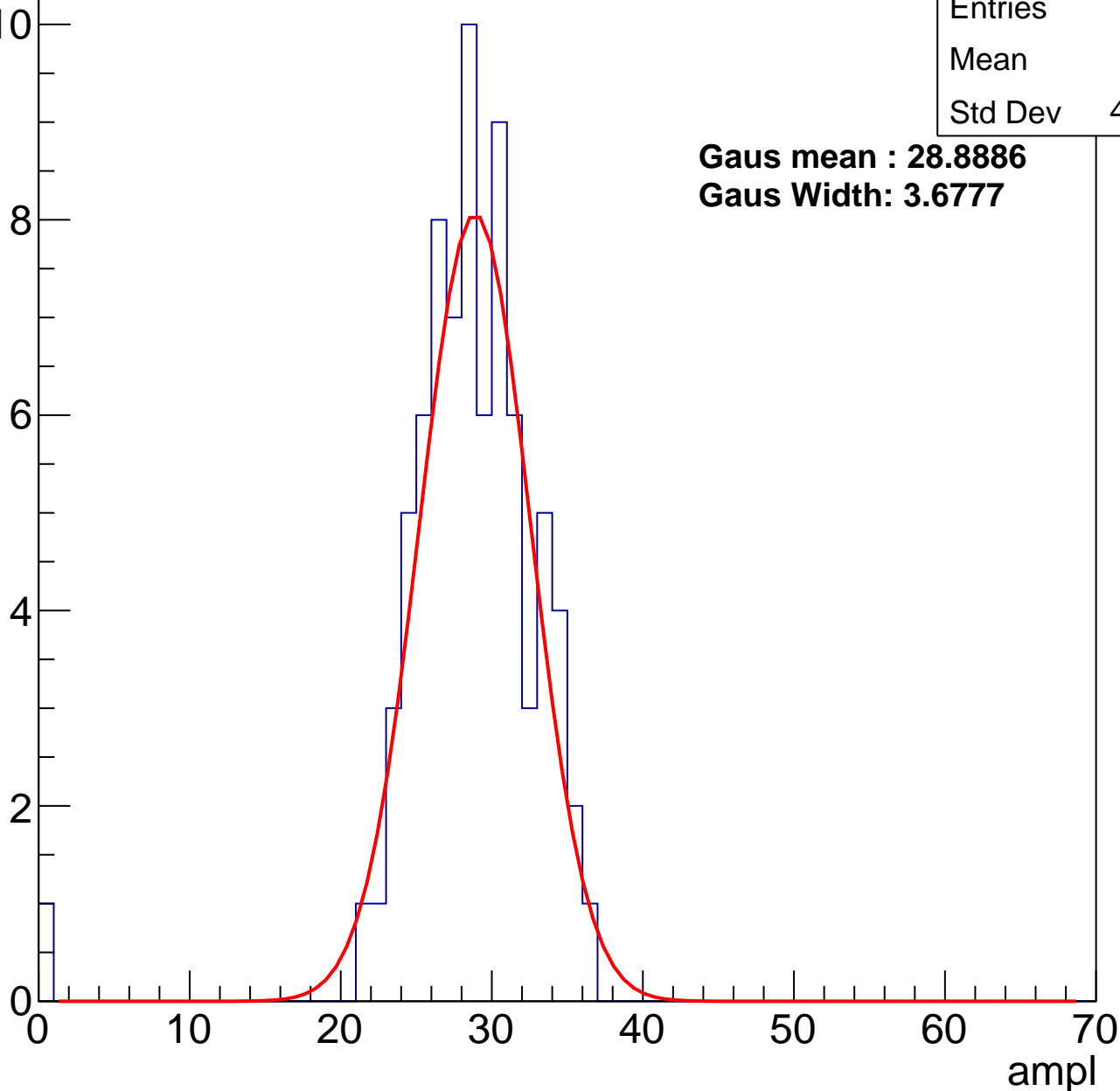
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	78
Mean	28.1
Std Dev	4.656

**Gaus mean : 28.8886**

**Gaus Width: 3.6777**



# B1L003S, U6-ch44, adc1

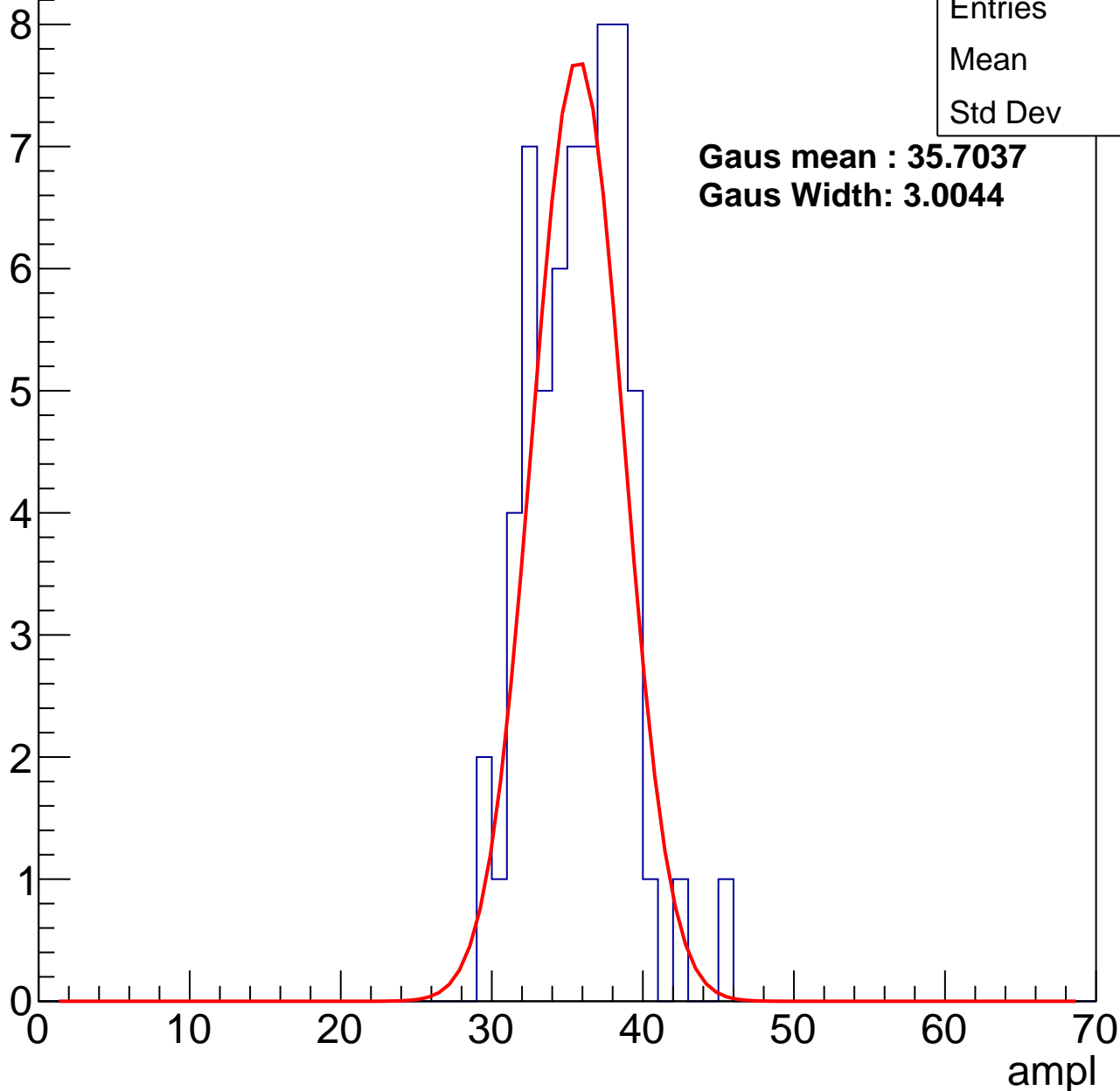
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	35.3
Std Dev	3.11

**Gaus mean : 35.7037**

**Gaus Width: 3.0044**



# B1L003S, U6-ch44, adc2

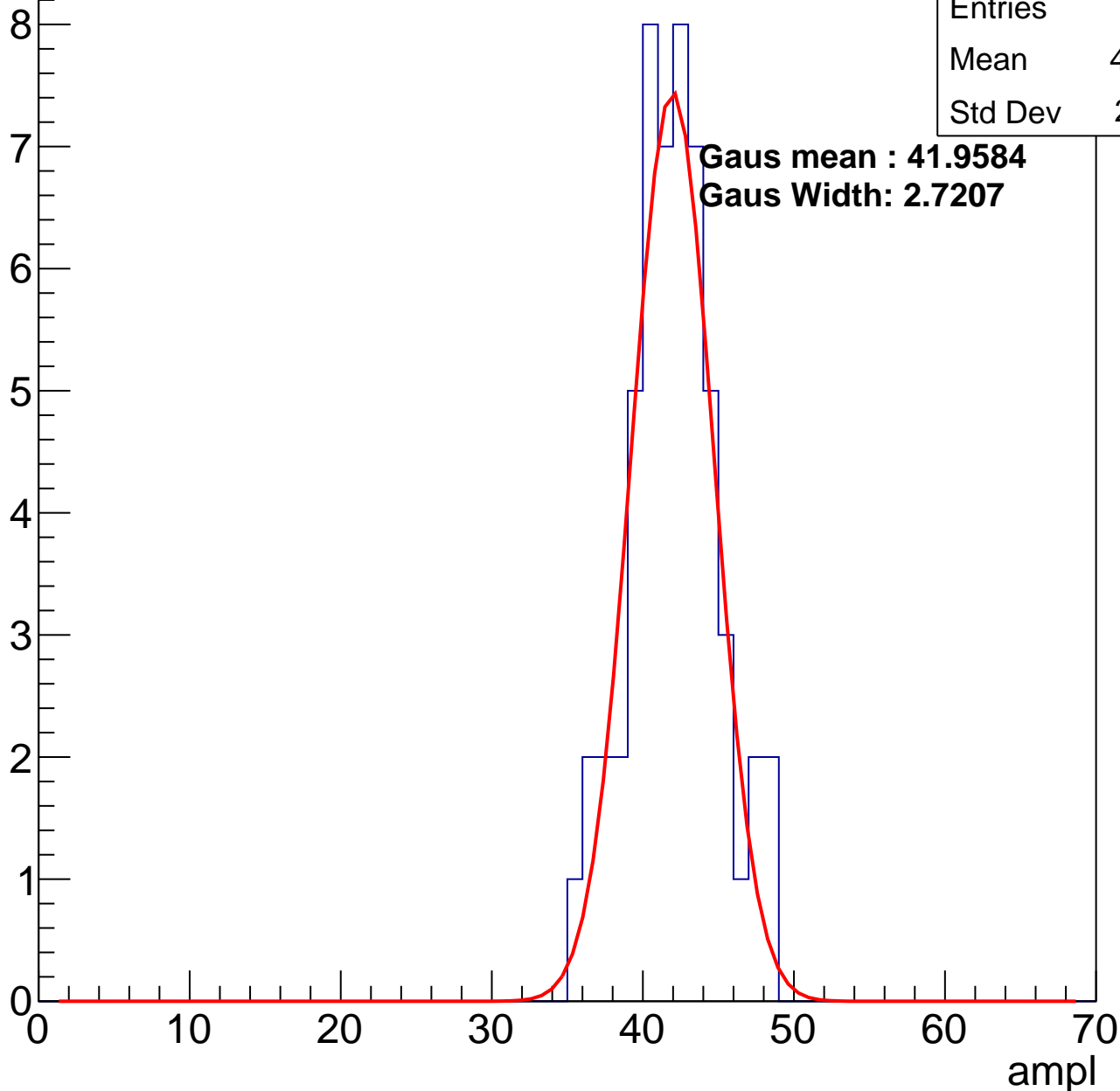
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	41.58
Std Dev	2.921

**Gaus mean : 41.9584**

**Gaus Width: 2.7207**

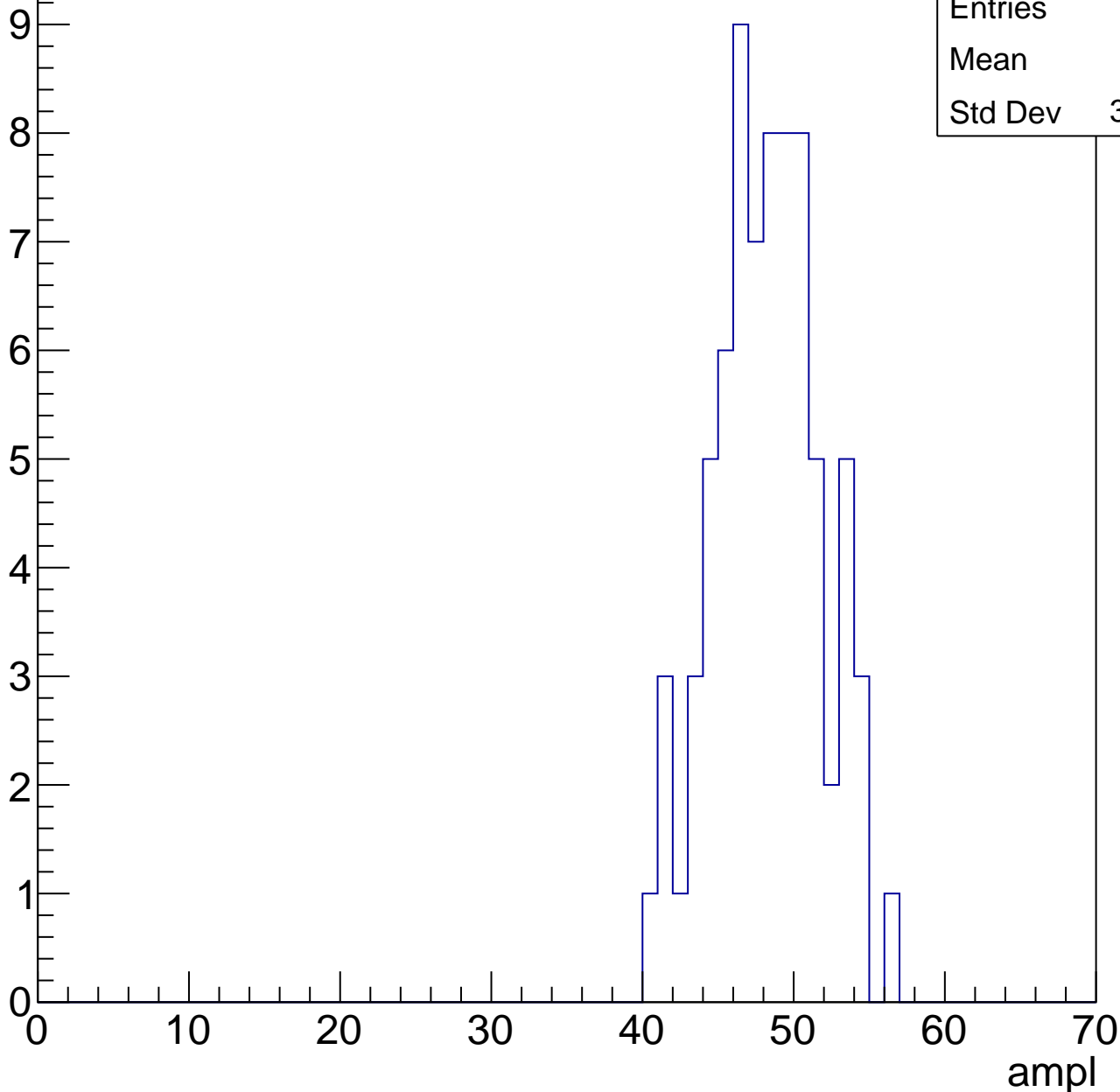


# B1L003S, U6-ch44, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	75
Mean	47.8
Std Dev	3.483

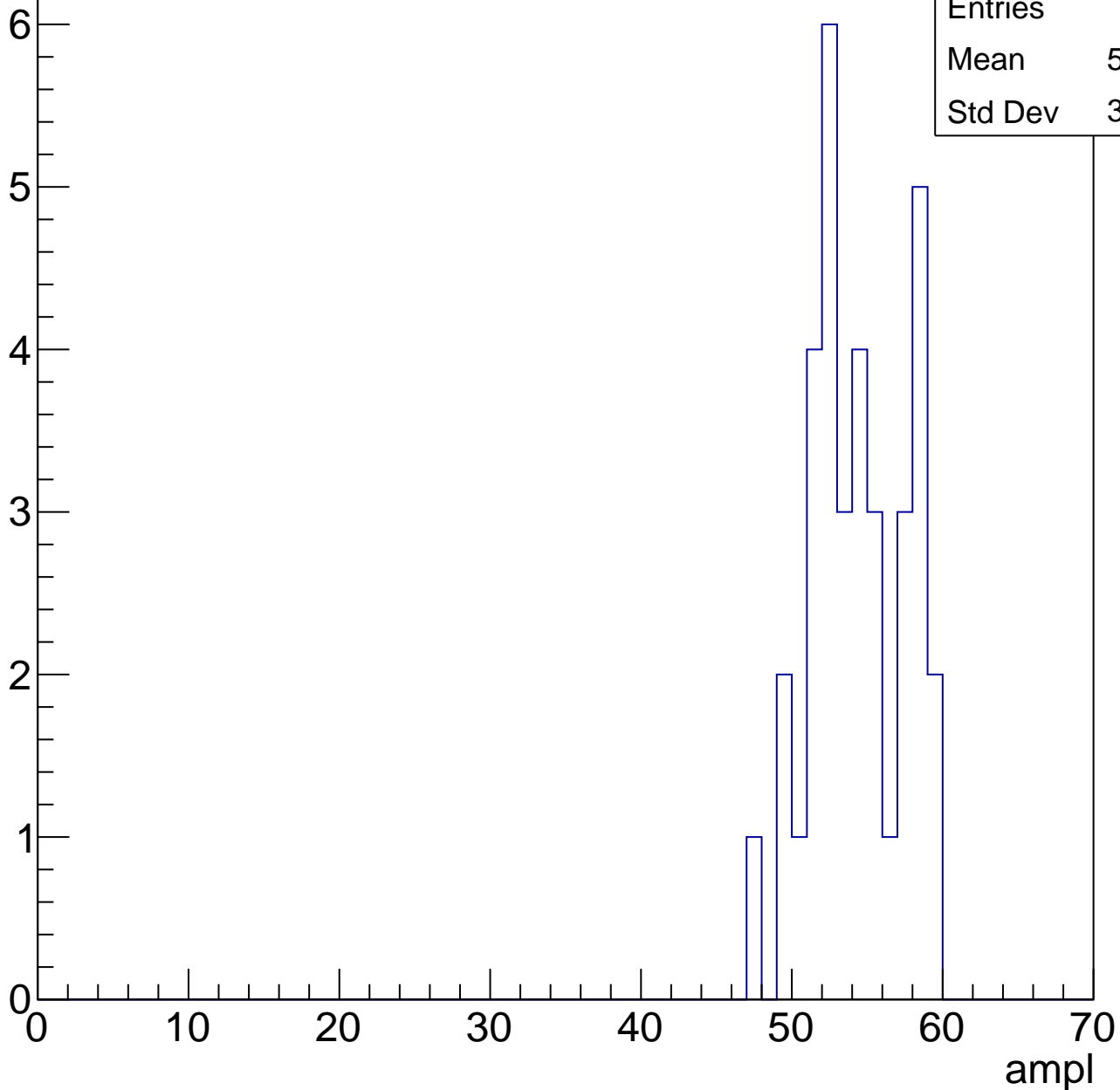


# B1L003S, U6-ch44, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

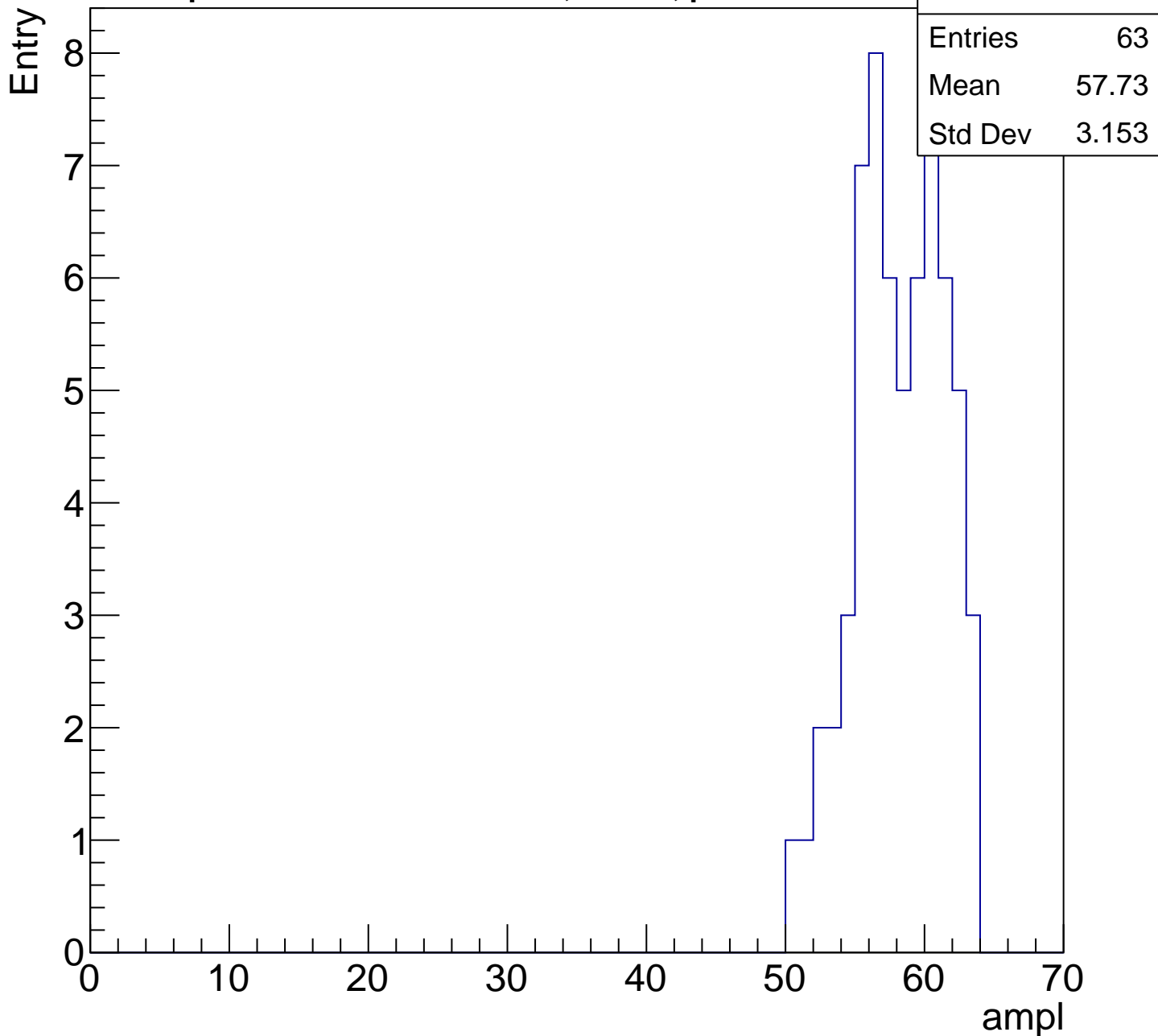
Entry

Entries	35
Mean	53.89
Std Dev	3.124



# B1L003S, U6-ch44, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

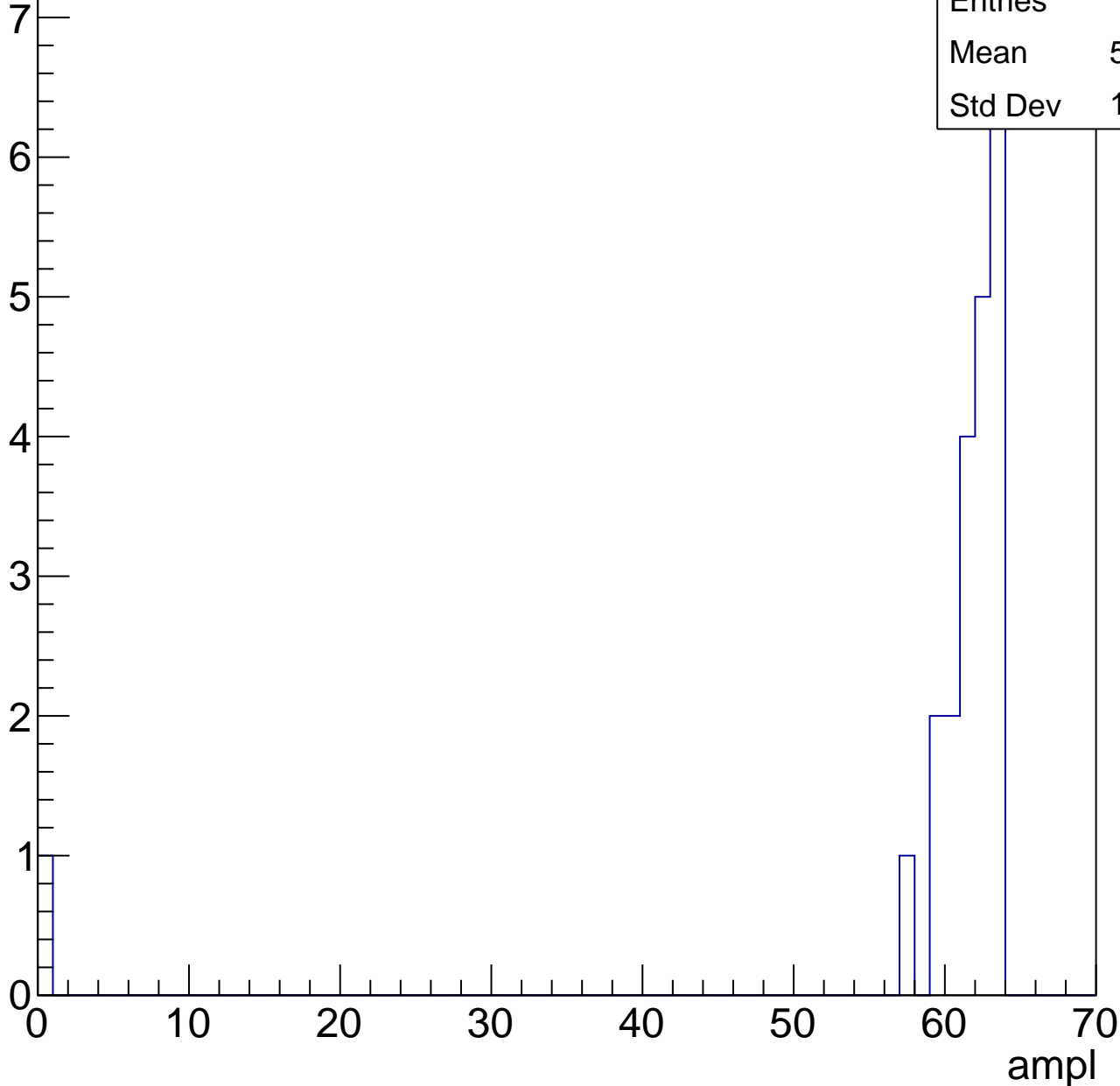


# B1L003S, U6-ch44, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	22
Mean	58.64
Std Dev	12.89





# B1L003S, U6-ch44, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch45, adc0

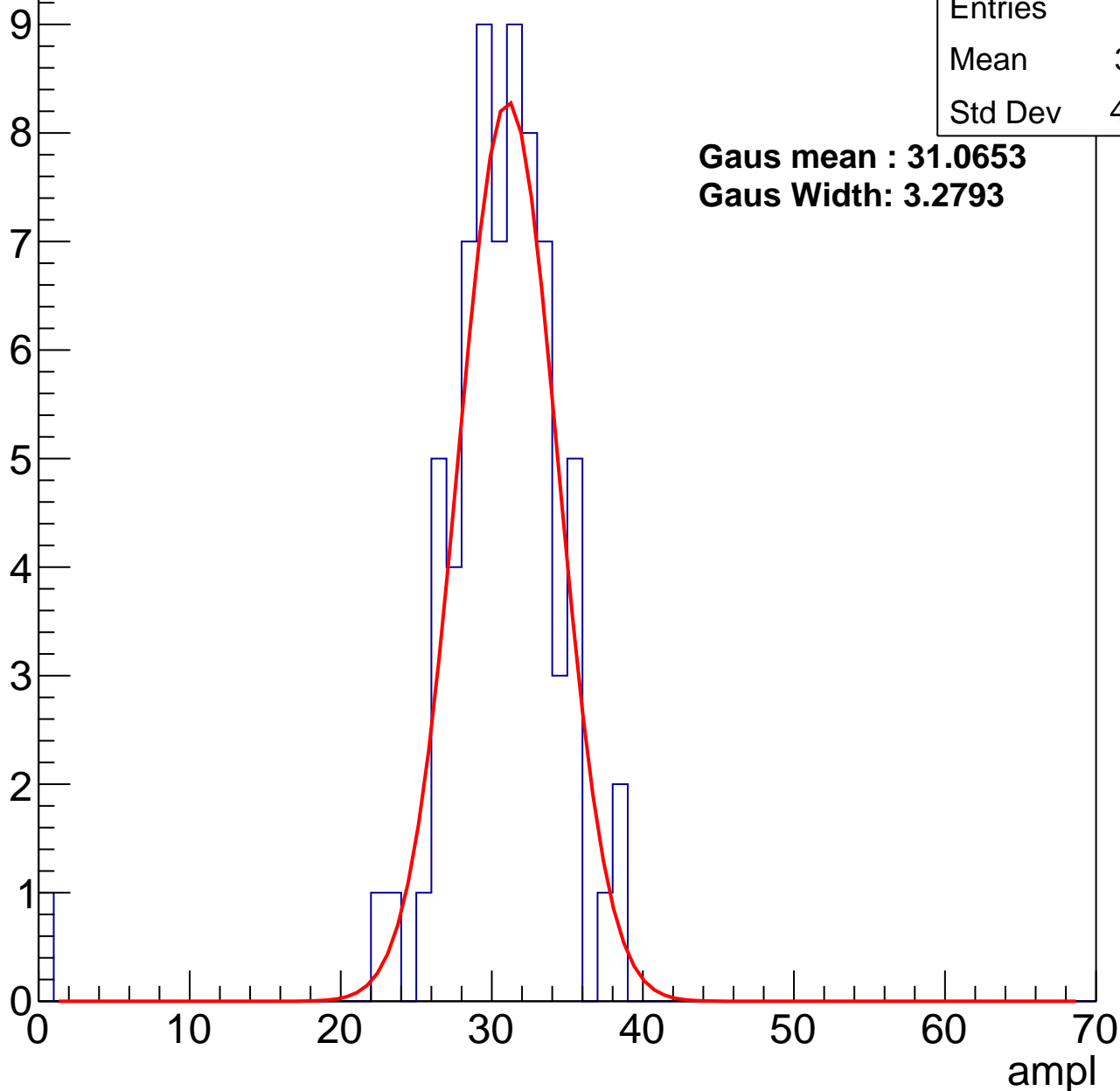
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	71
Mean	30.01
Std Dev	4.813

**Gaus mean : 31.0653**

**Gaus Width: 3.2793**



# B1L003S, U6-ch45, adc1

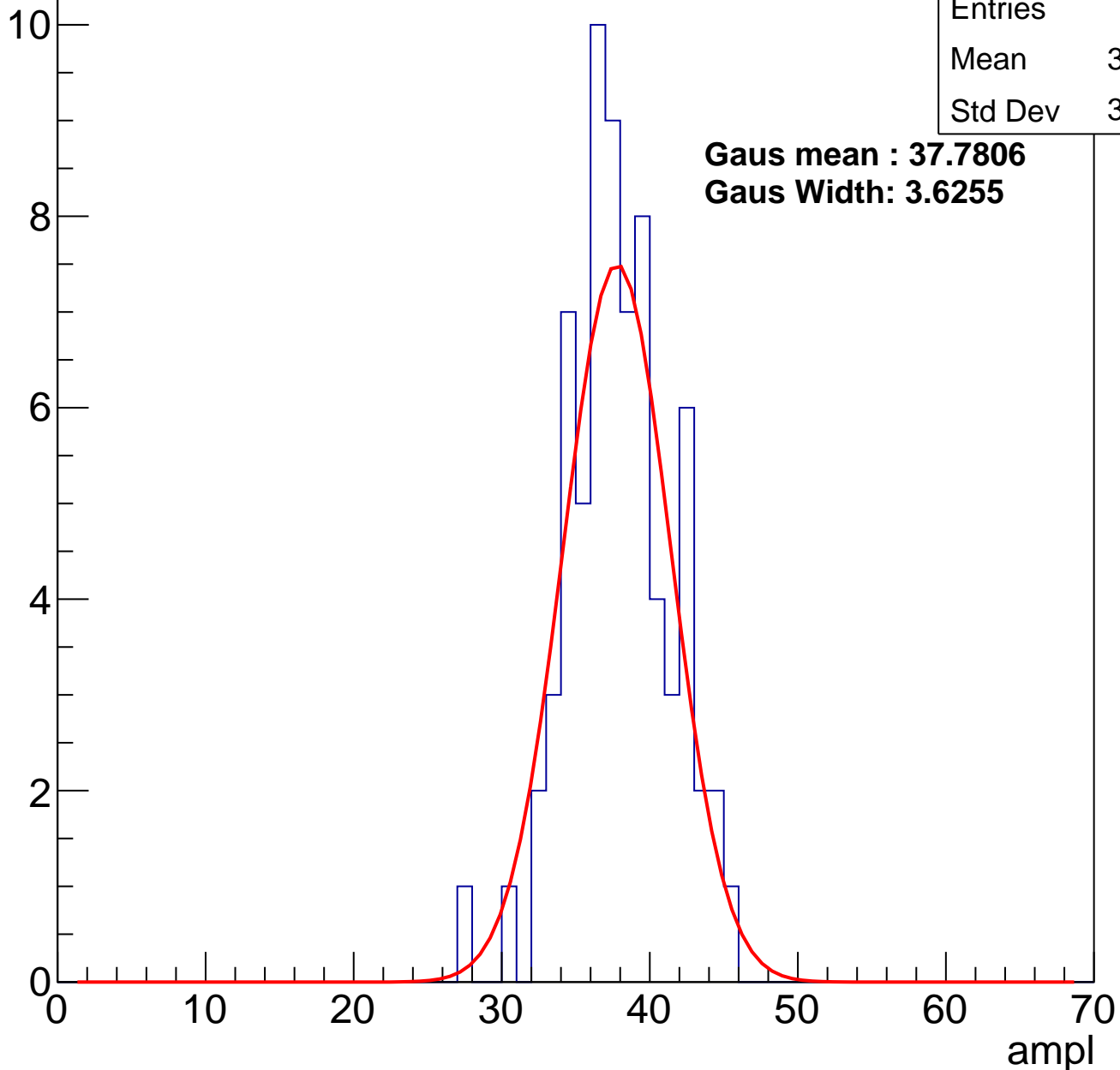
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	71
Mean	37.44
Std Dev	3.426

**Gaus mean : 37.7806**

**Gaus Width: 3.6255**

Entry

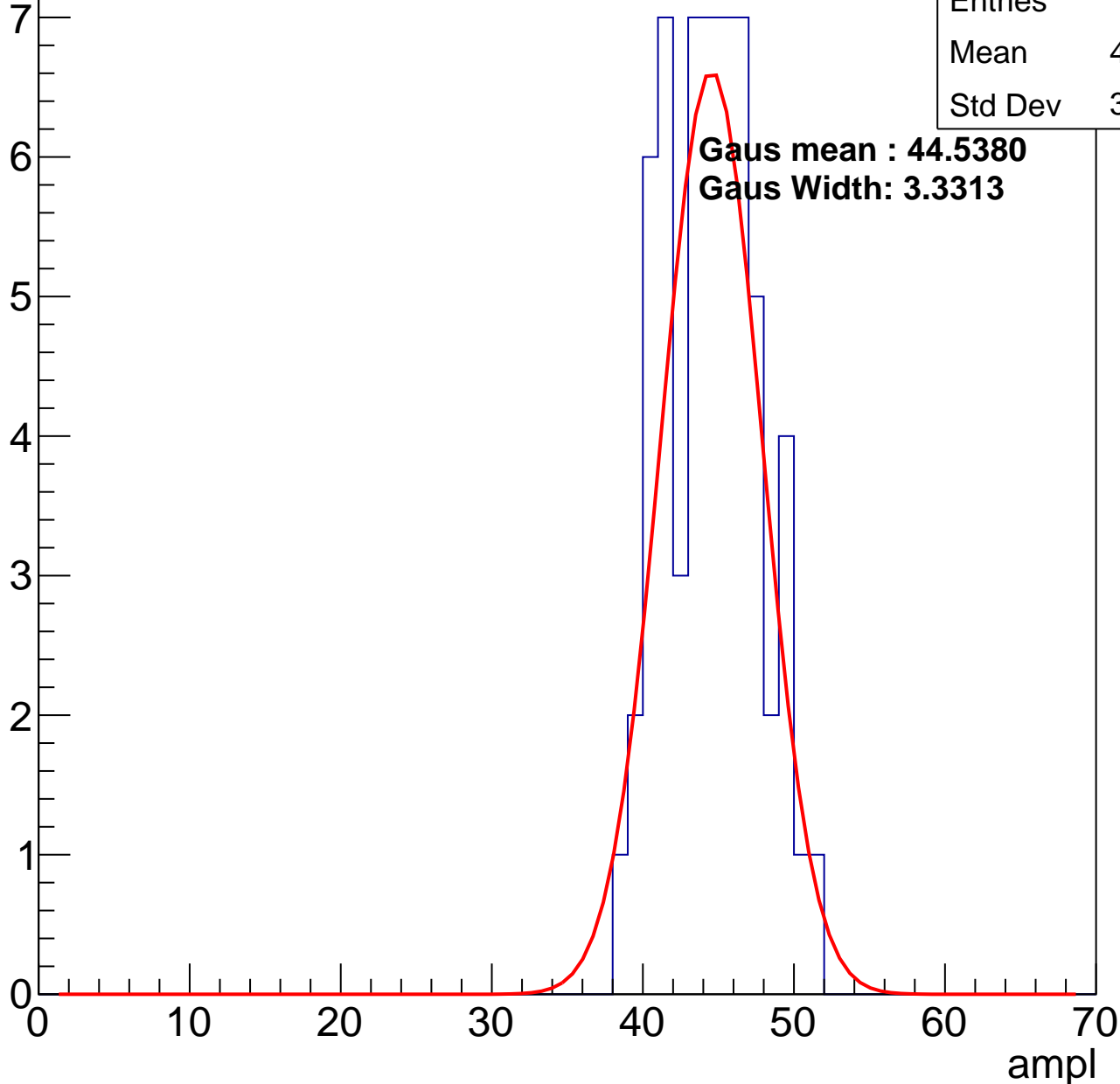


# B1L003S, U6-ch45, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	44.05
Std Dev	3.057

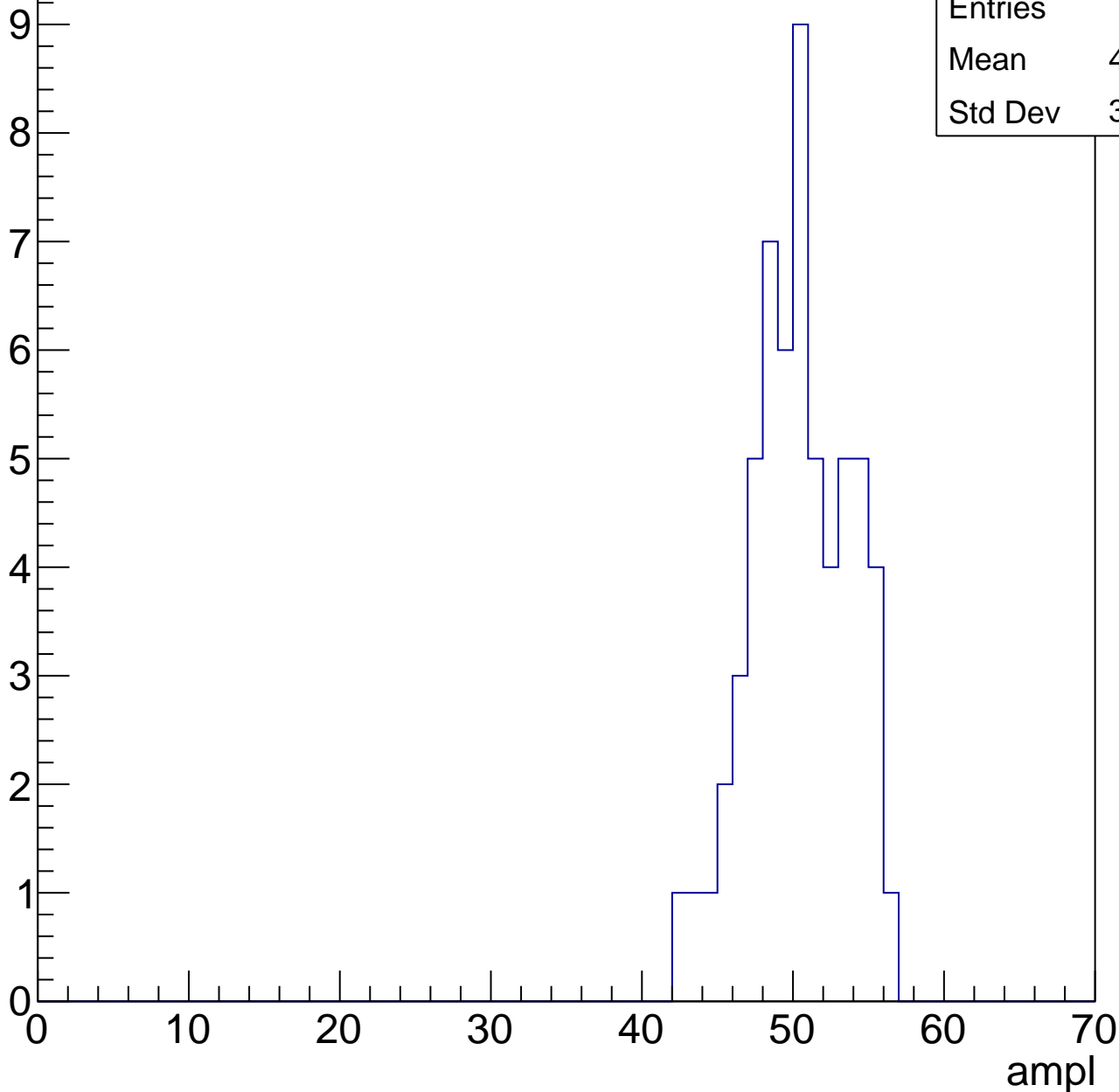


# B1L003S, U6-ch45, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	49.93
Std Dev	3.209

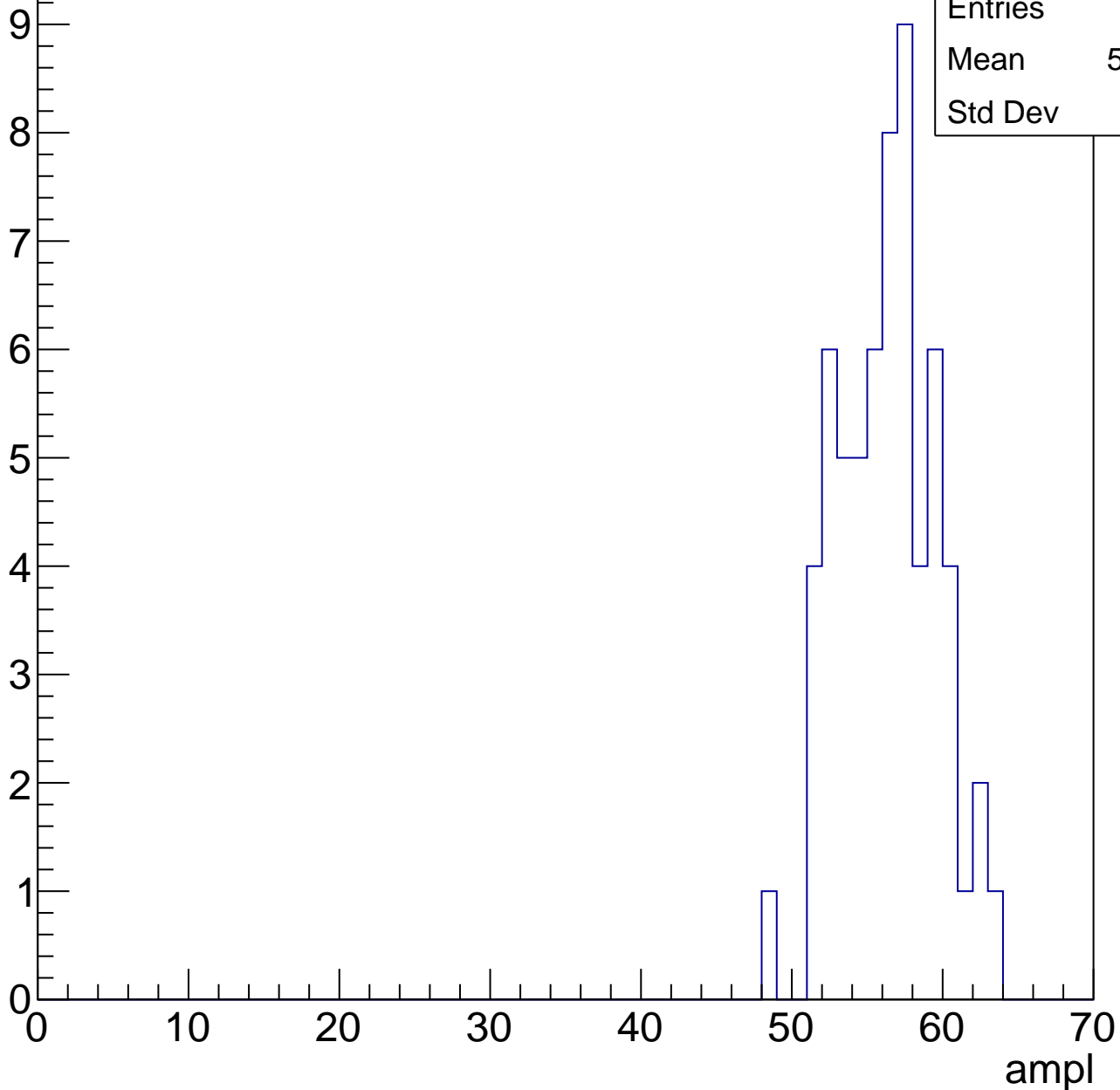


# B1L003S, U6-ch45, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	55.87
Std Dev	3.16

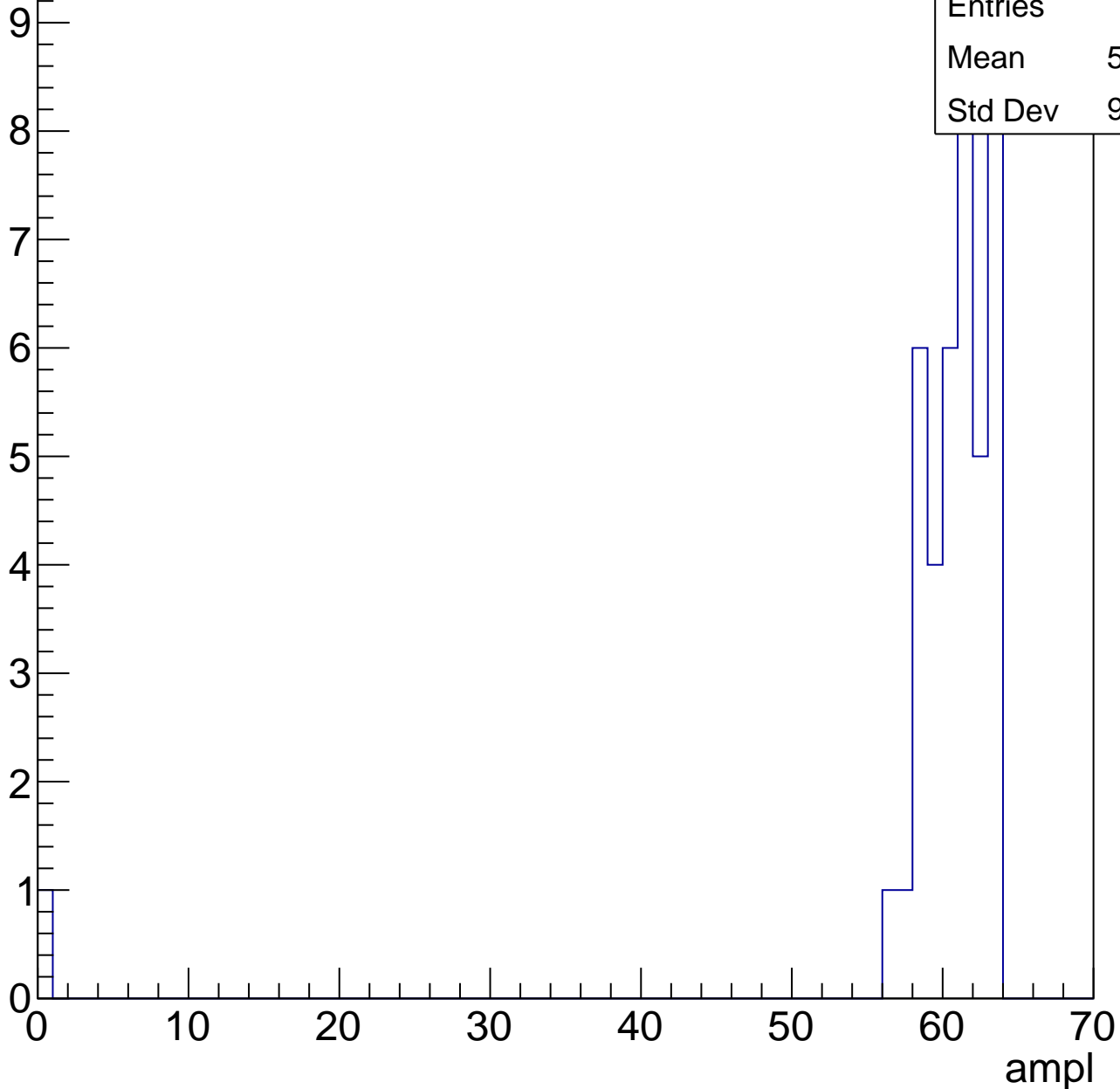


# B1L003S, U6-ch45, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

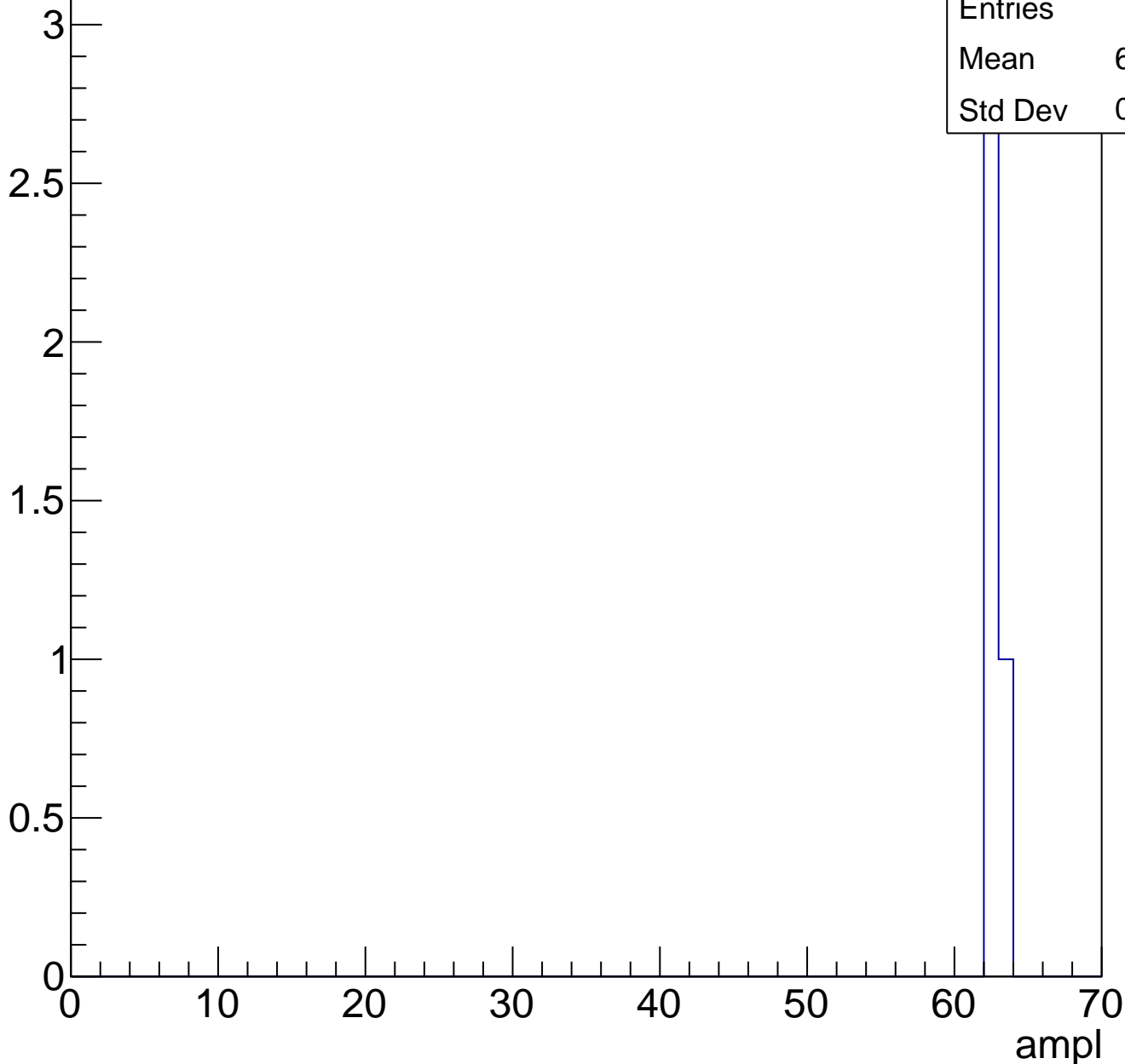
Entries	41
Mean	59.02
Std Dev	9.519



# B1L003S, U6-ch45, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch45, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch46, adc0

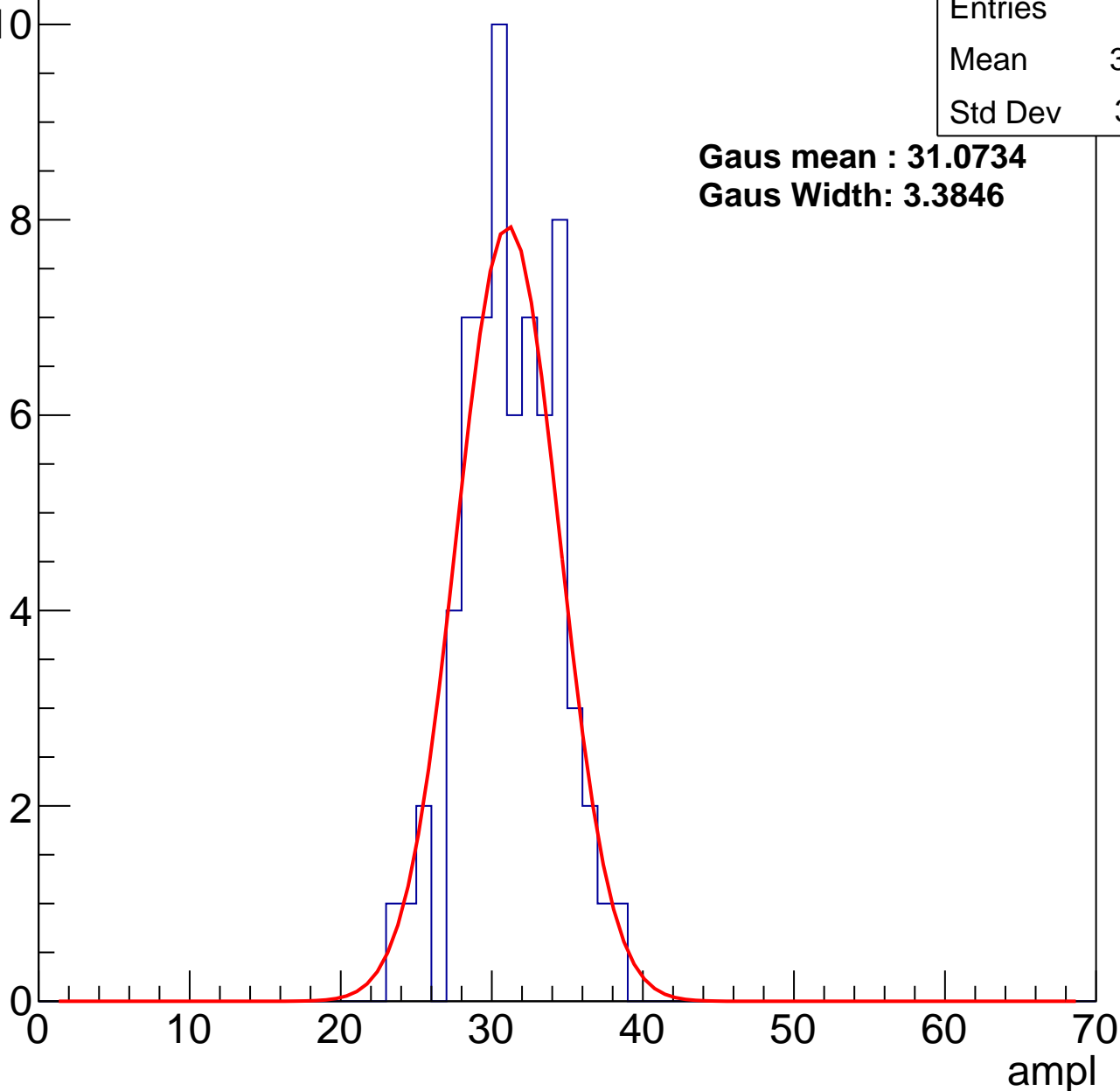
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	30.85
Std Dev	3.101

**Gaus mean : 31.0734**

**Gaus Width: 3.3846**



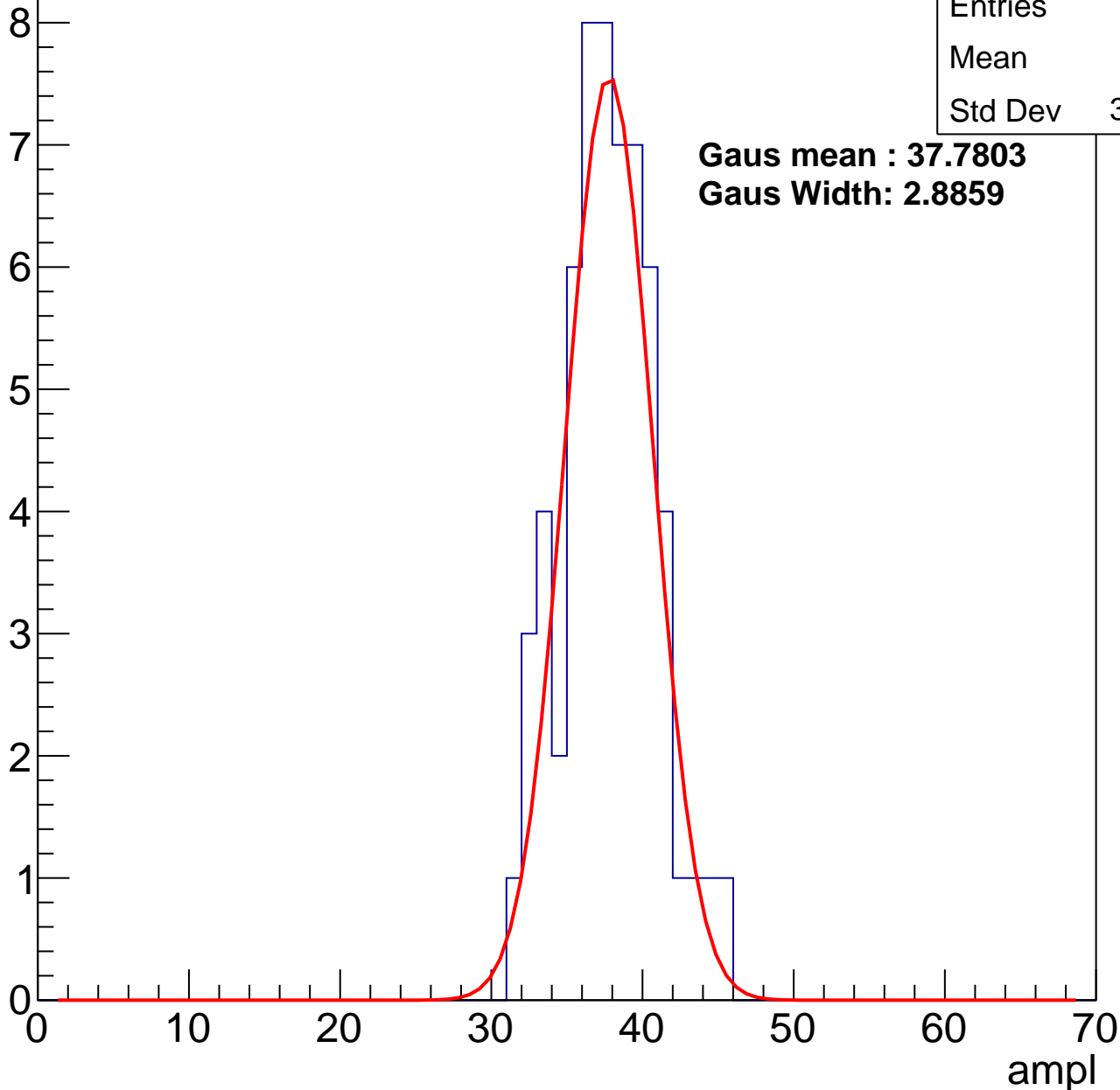
# B1L003S, U6-ch46, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	37.3
Std Dev	3.018

**Gaus mean : 37.7803**  
**Gaus Width: 2.8859**



# B1L003S, U6-ch46, adc2

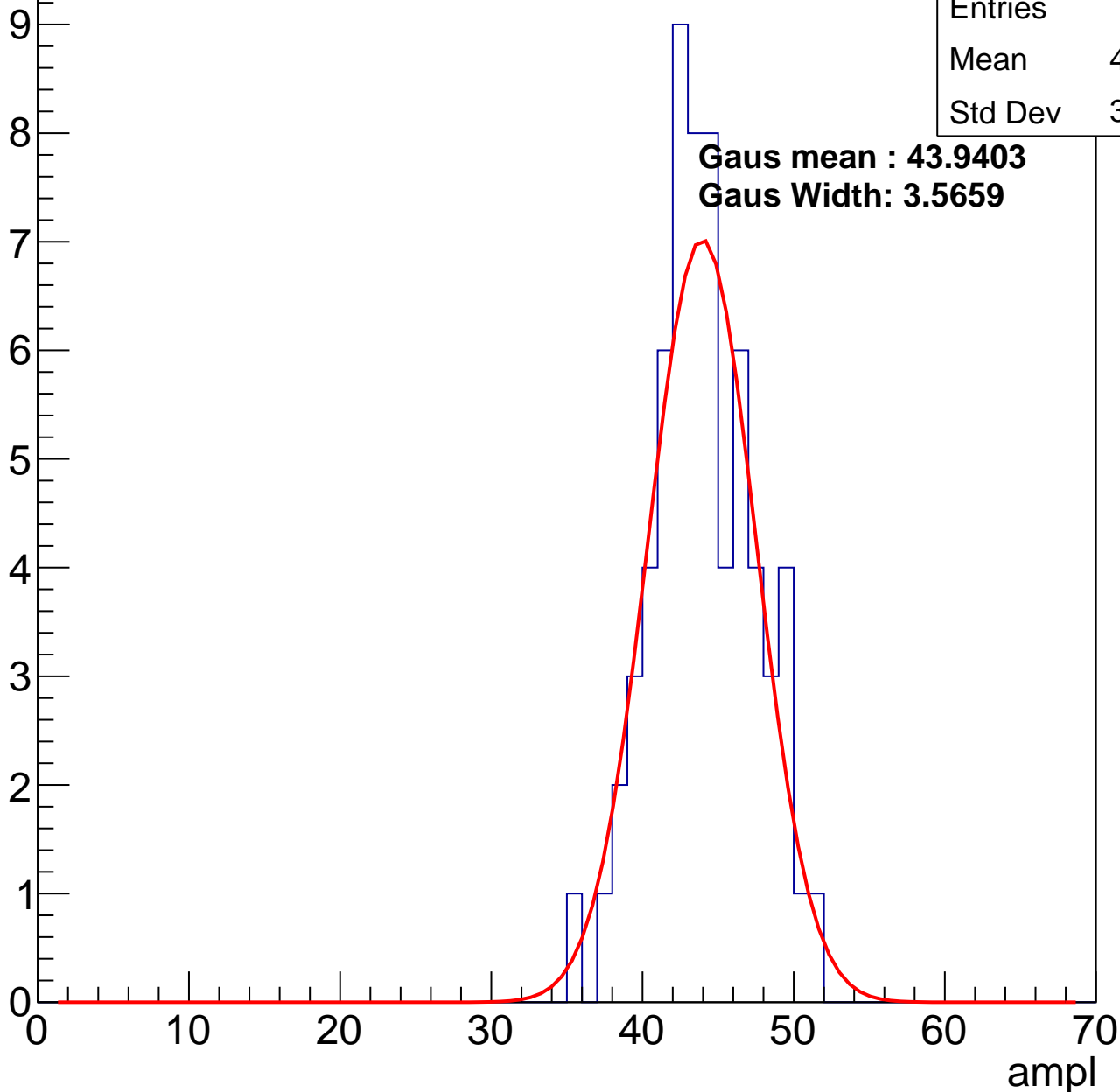
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	43.54
Std Dev	3.333

**Gaus mean : 43.9403**

**Gaus Width: 3.5659**

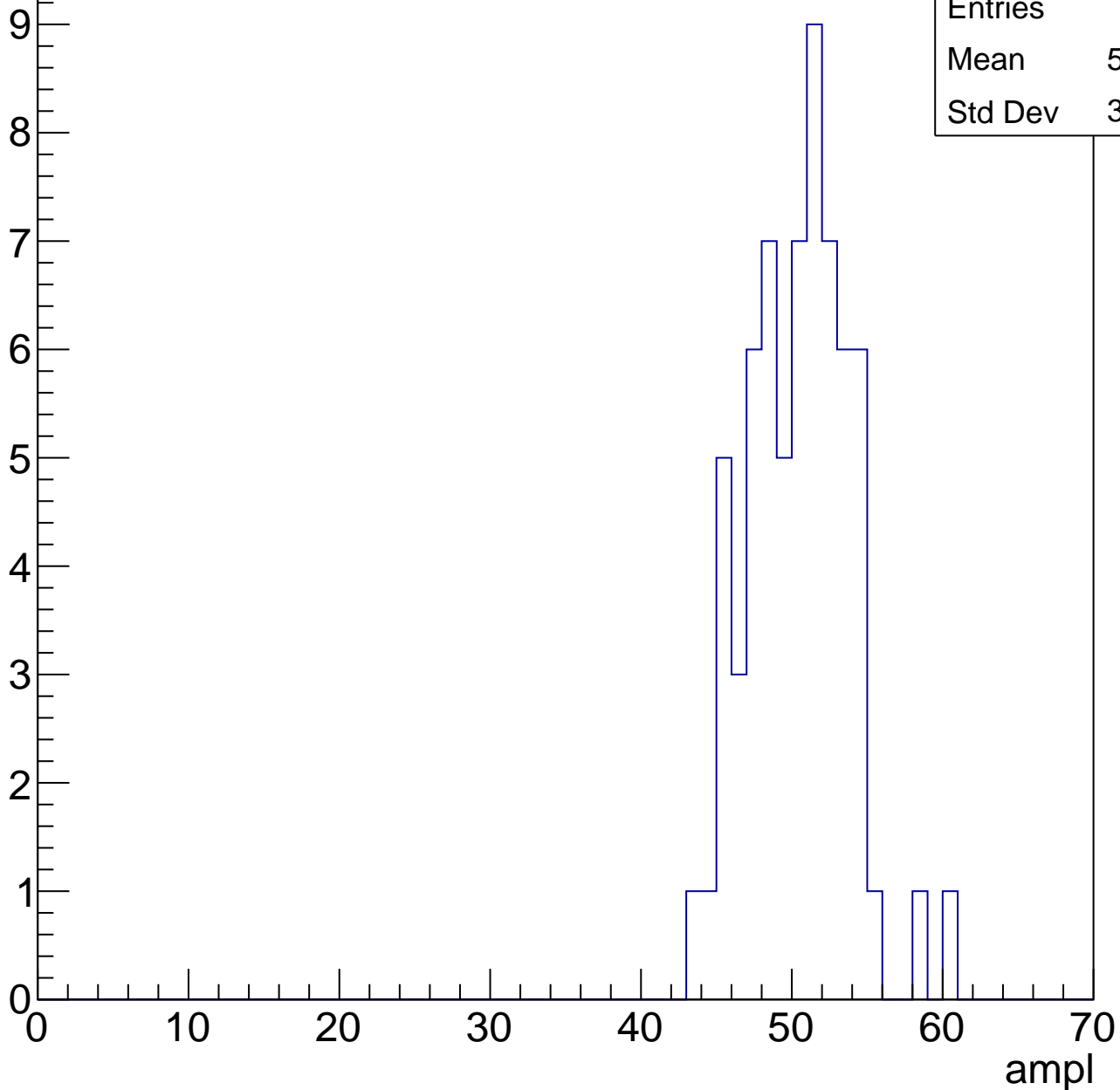


# B1L003S, U6-ch46, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	50.02
Std Dev	3.305



# B1L003S, U6-ch46, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

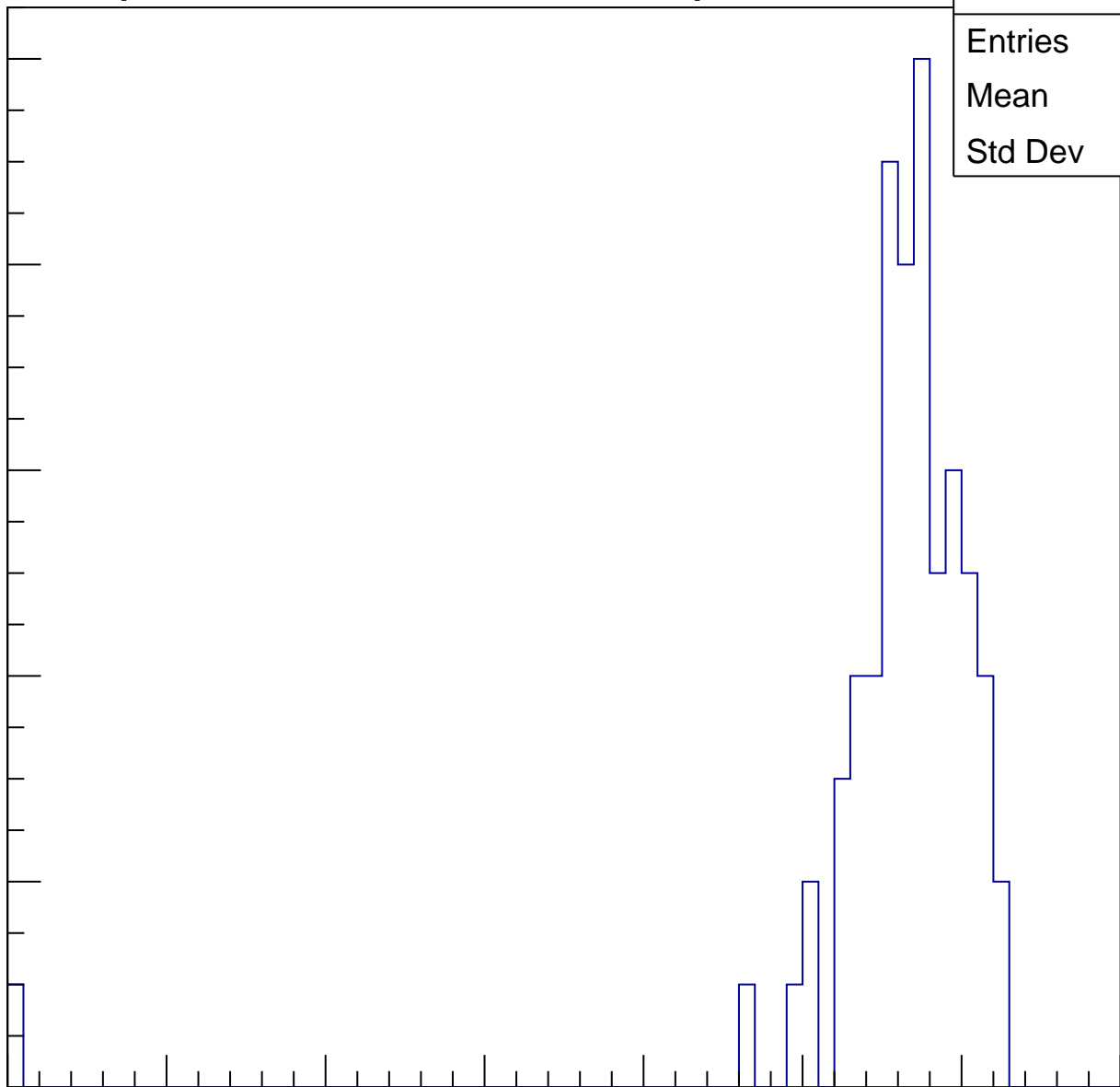
Entries	65
Mean	55.45
Std Dev	7.628

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

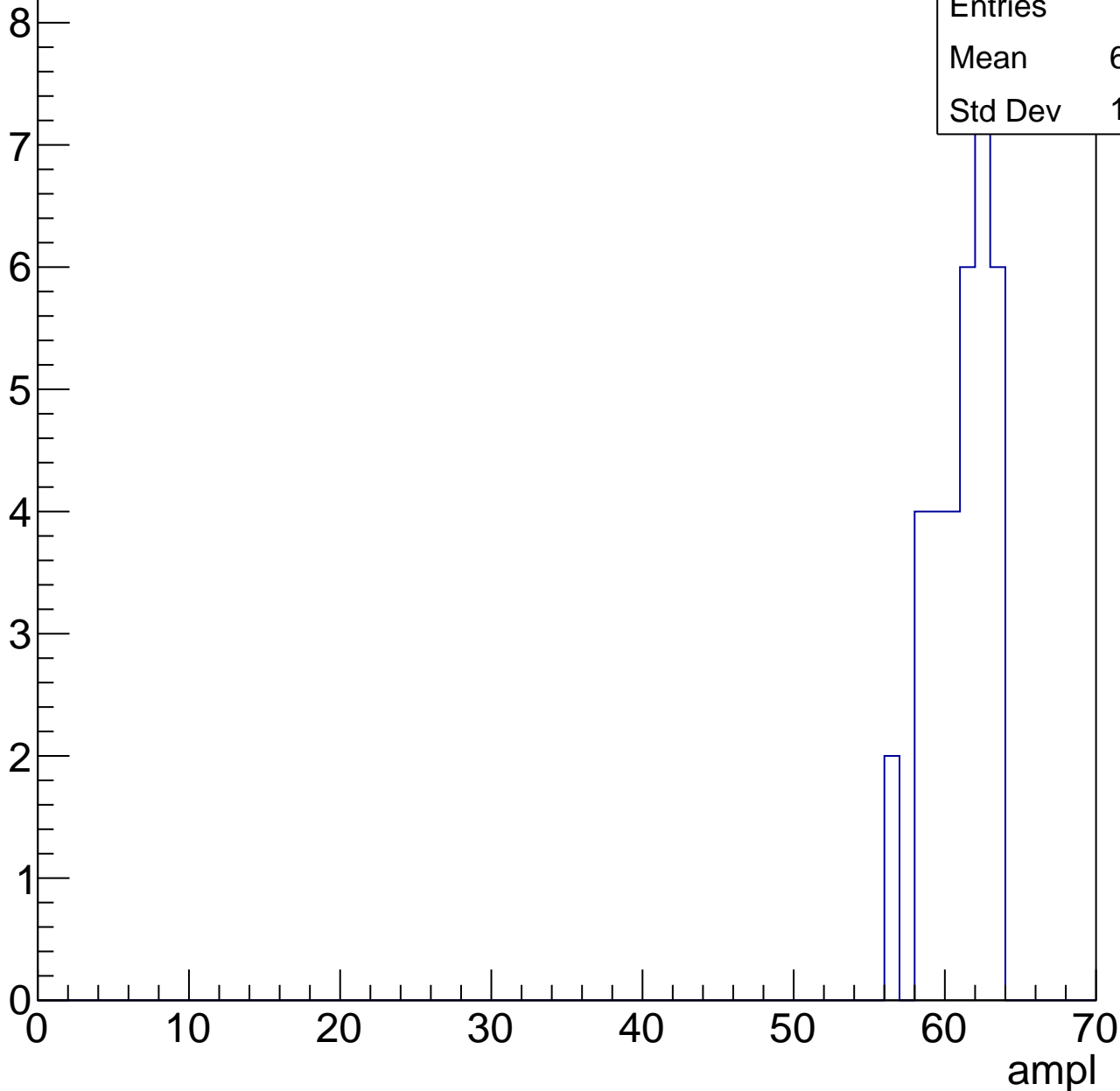


# B1L003S, U6-ch46, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	34
Mean	60.59
Std Dev	1.972



# B1L003S, U6-ch46, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

4  
3.5  
3  
2.5  
2  
1.5  
1  
0.5  
0

0

10

20

30

40

50

60

70

ampl

Entries

4

Mean

63

Std Dev

0



# B1L003S, U6-ch46, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch47, adc0

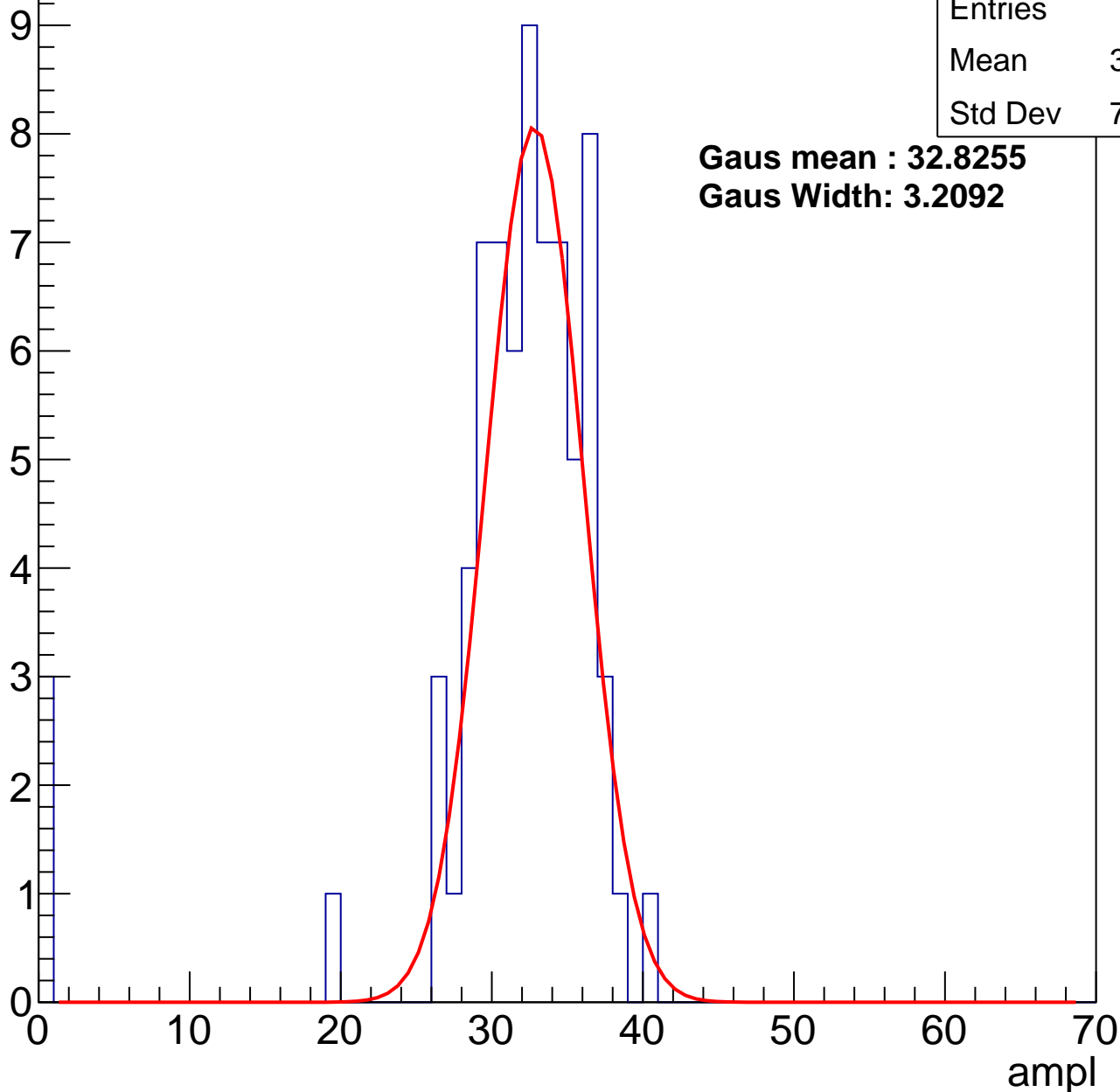
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	73
Mean	30.74
Std Dev	7.217

**Gaus mean : 32.8255**

**Gaus Width: 3.2092**



# B1L003S, U6-ch47, adc1

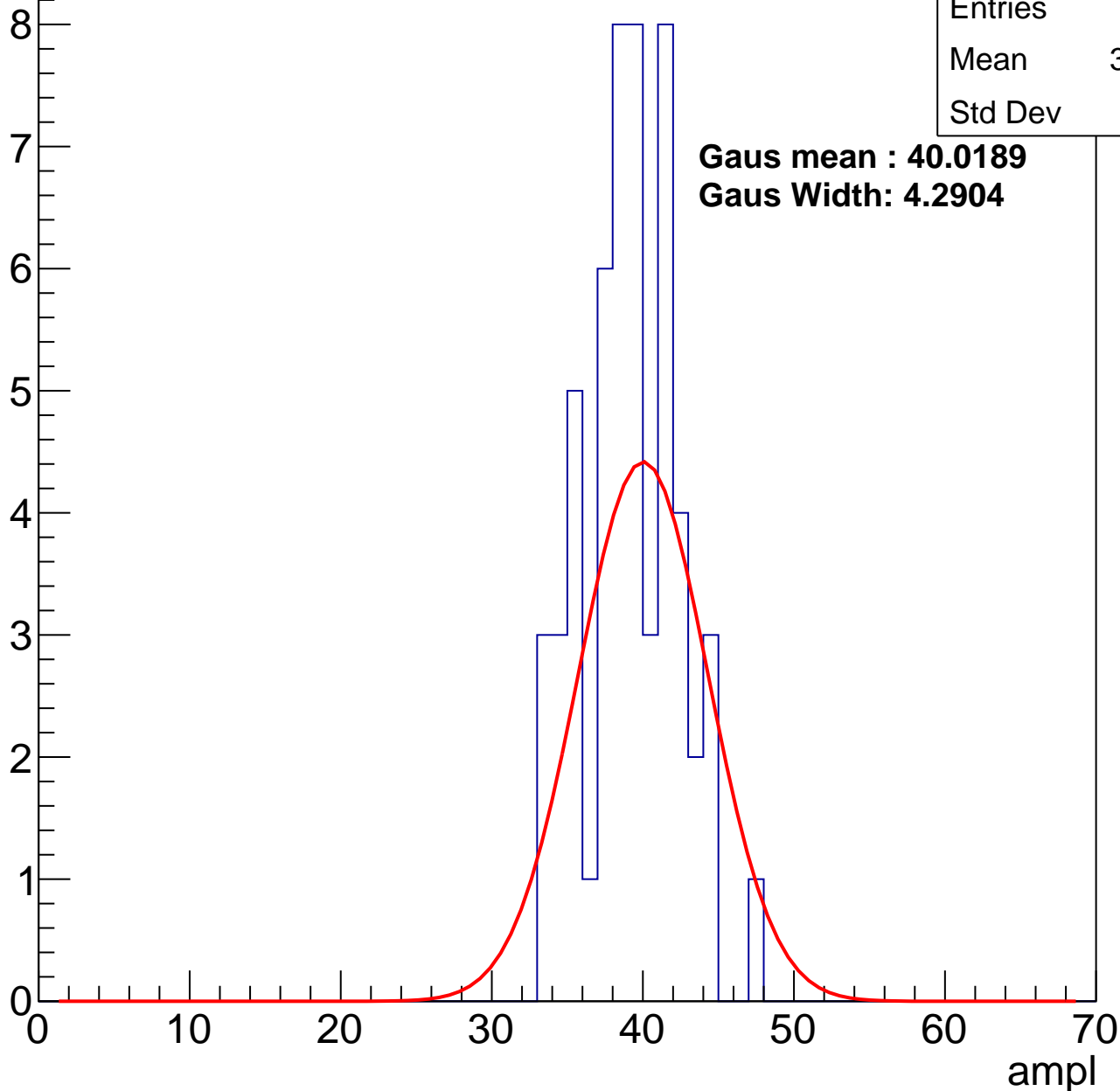
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	38.75
Std Dev	3.14

**Gaus mean : 40.0189**

**Gaus Width: 4.2904**



# B1L003S, U6-ch47, adc2

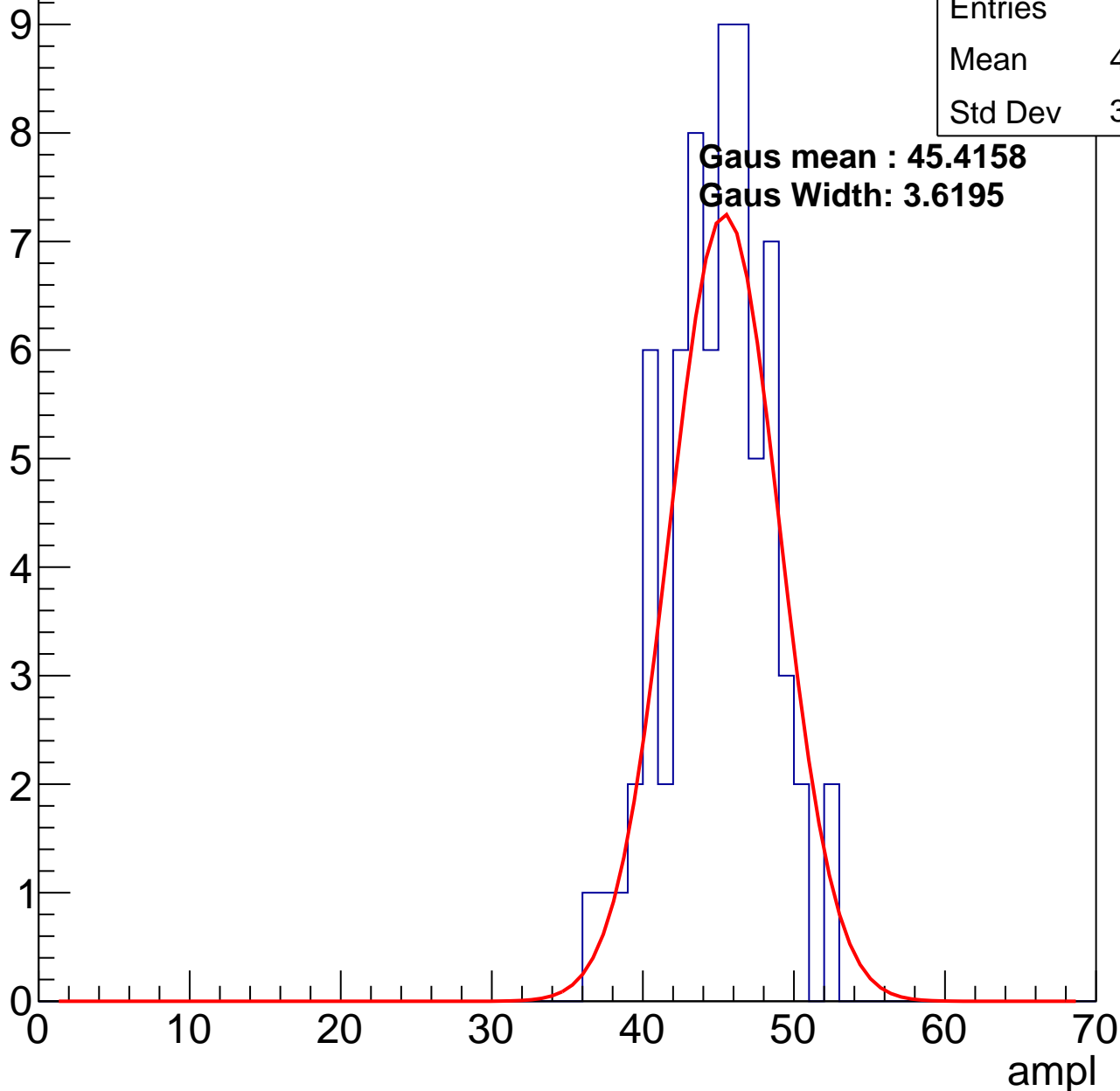
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	44.46
Std Dev	3.396

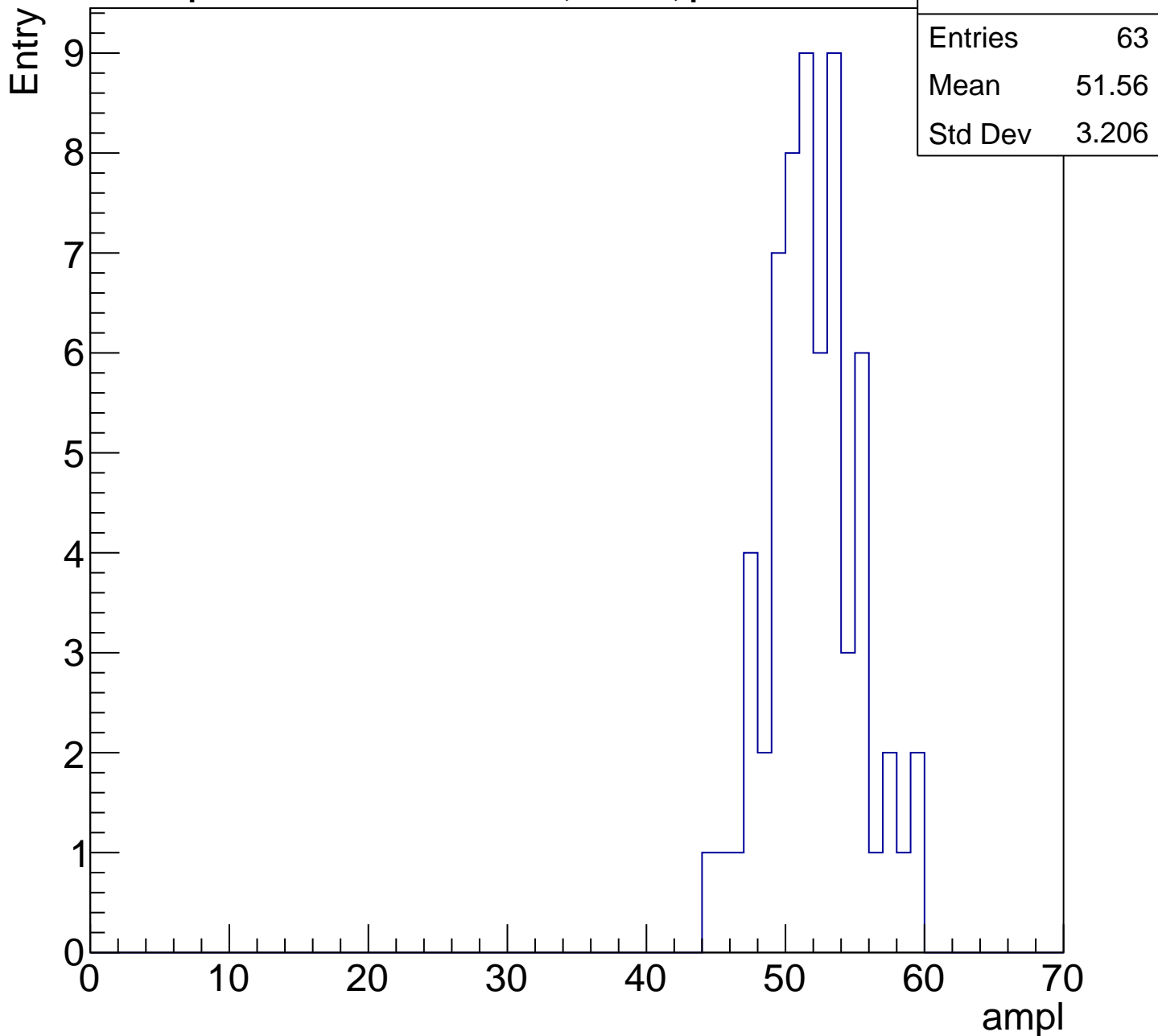
**Gaus mean : 45.4158**

**Gaus Width: 3.6195**



# B1L003S, U6-ch47, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

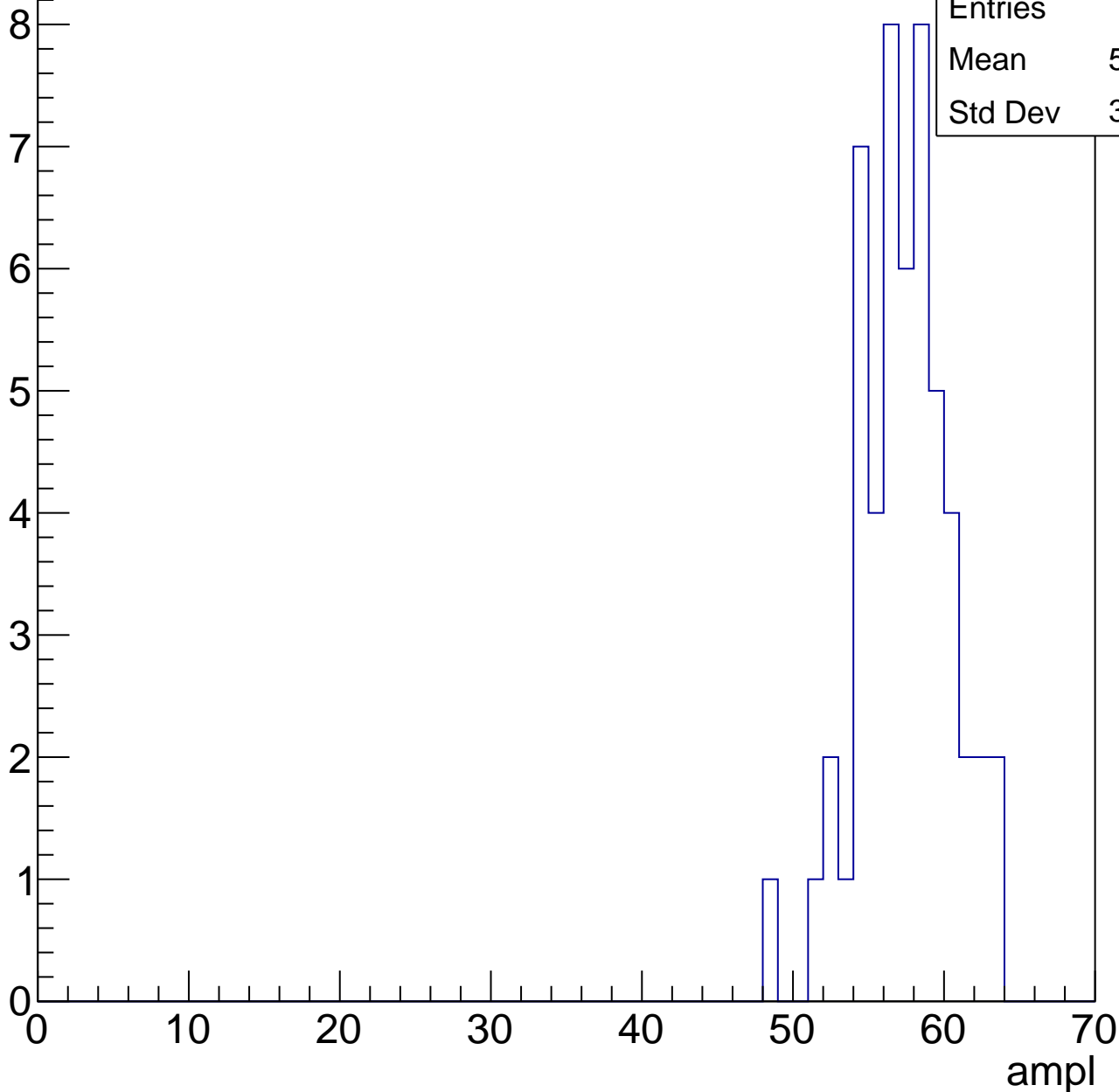


# B1L003S, U6-ch47, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	56.89
Std Dev	3.032

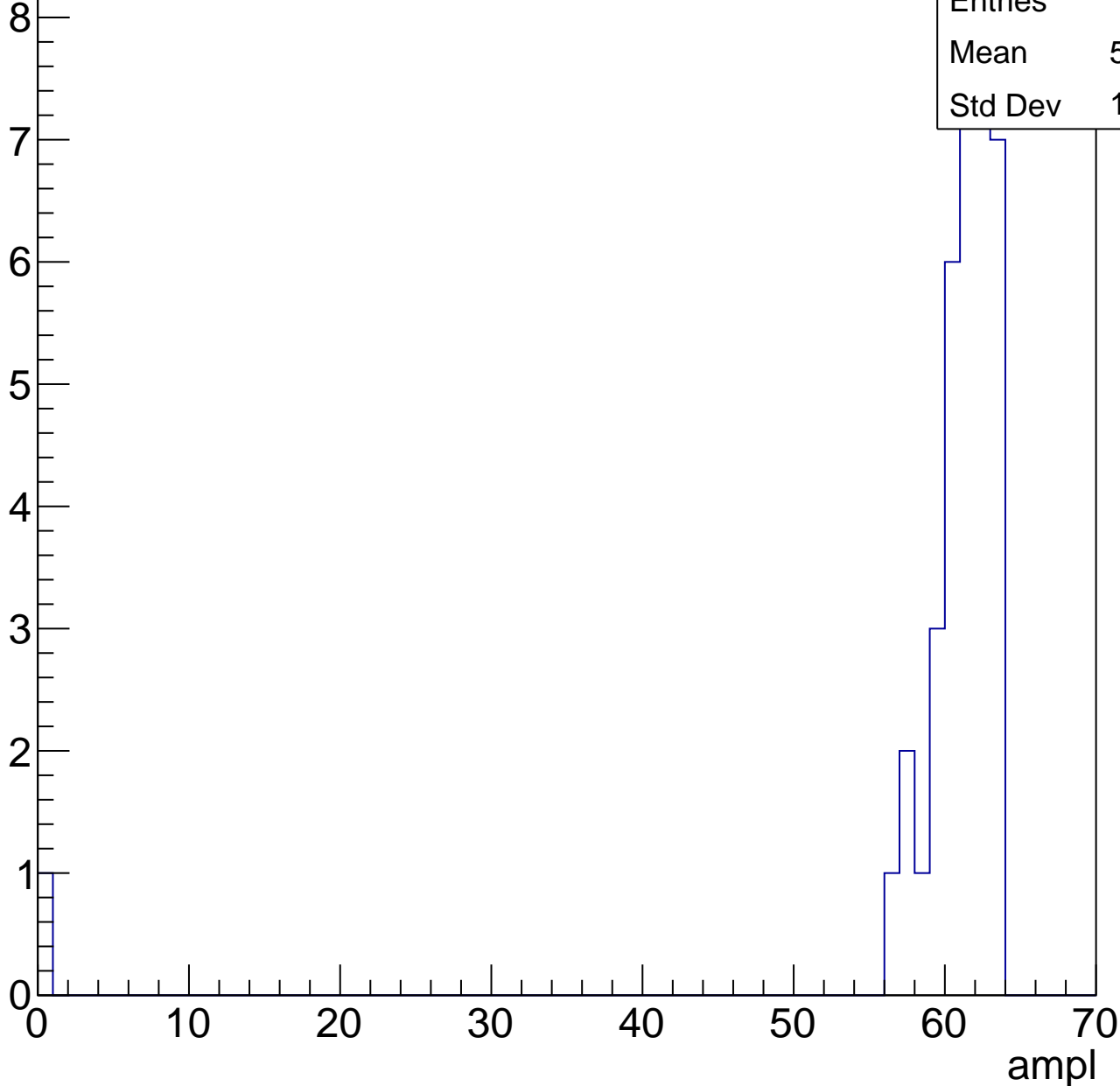


# B1L003S, U6-ch47, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

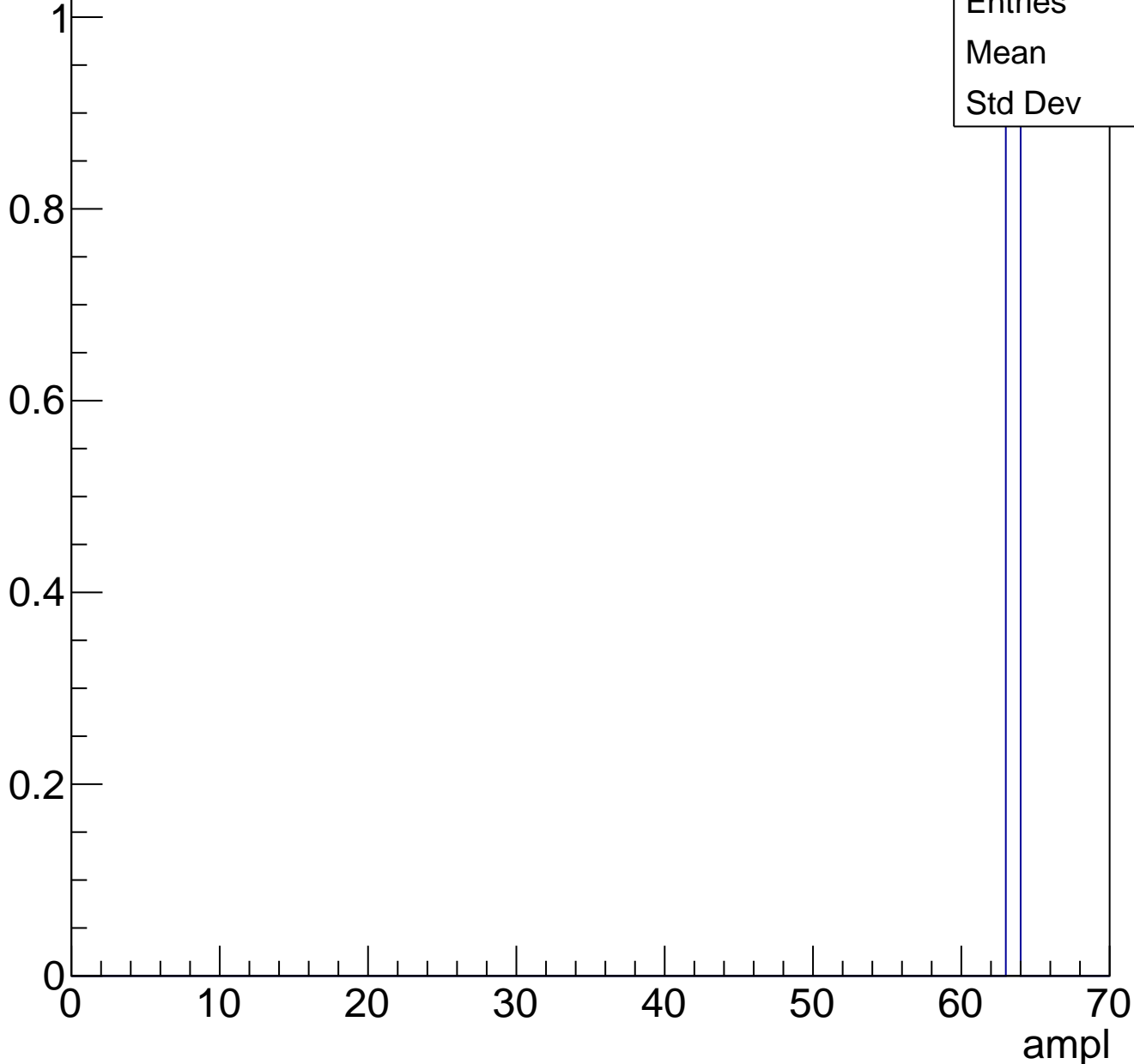
Entries	37
Mean	59.19
Std Dev	10.03



# B1L003S, U6-ch47, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch47, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U6-ch48, adc0

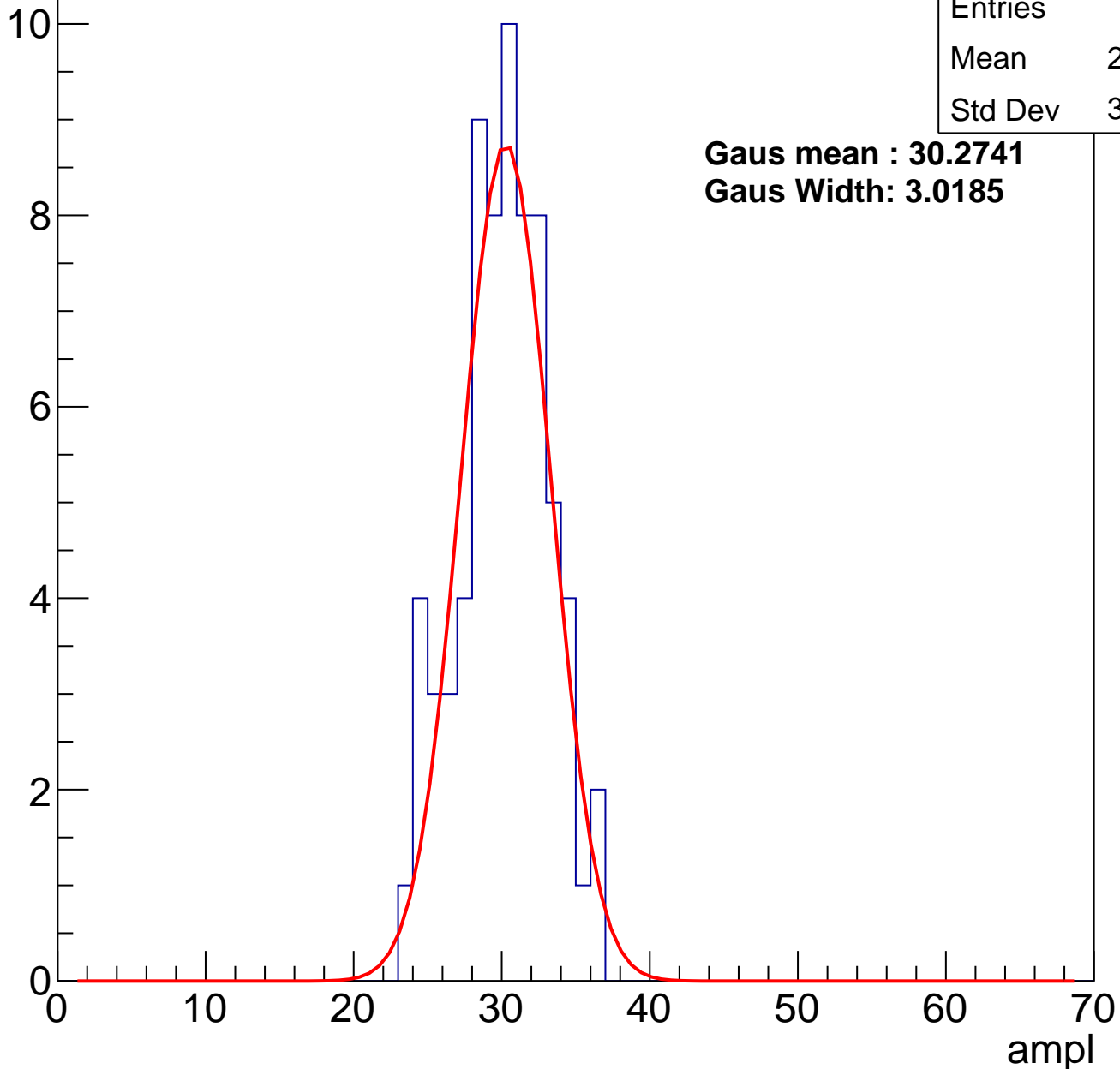
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	70
Mean	29.66
Std Dev	3.009

**Gaus mean : 30.2741**

**Gaus Width: 3.0185**

Entry



# B1L003S, U6-ch48, adc1

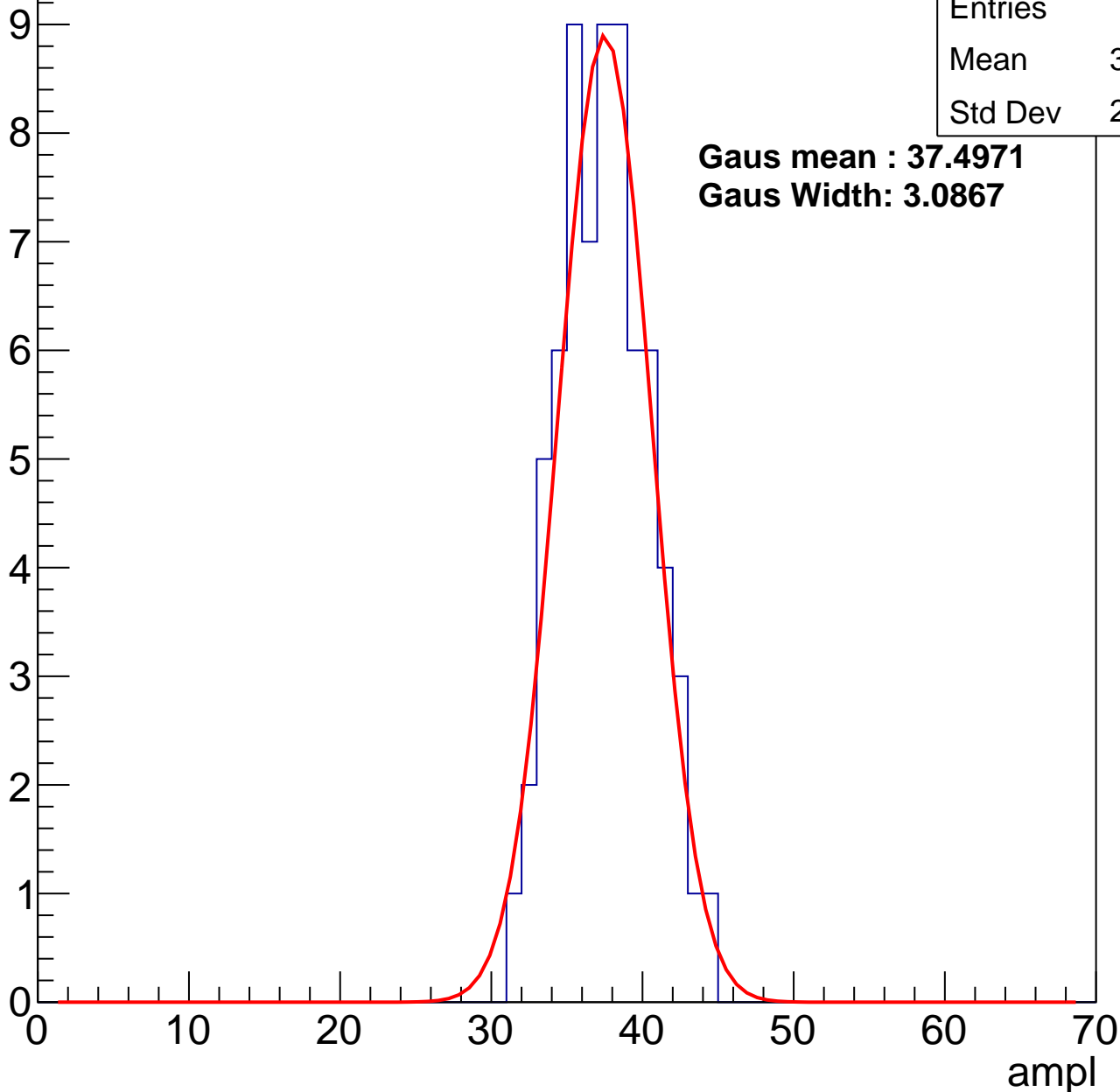
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	37.06
Std Dev	2.884

**Gaus mean : 37.4971**

**Gaus Width: 3.0867**



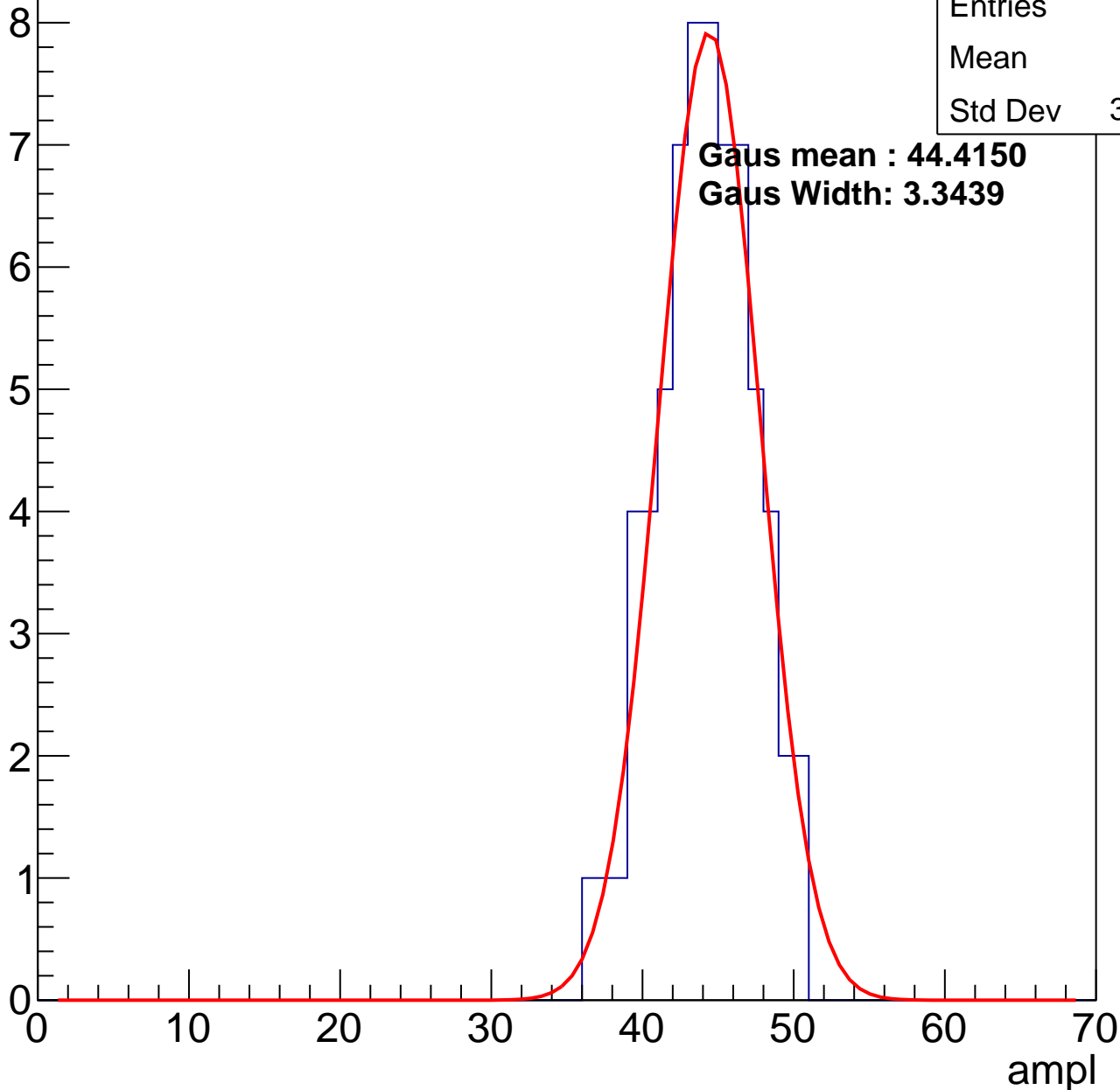
# B1L003S, U6-ch48, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	43.7
Std Dev	3.148

**Gaus mean : 44.4150**  
**Gaus Width: 3.3439**

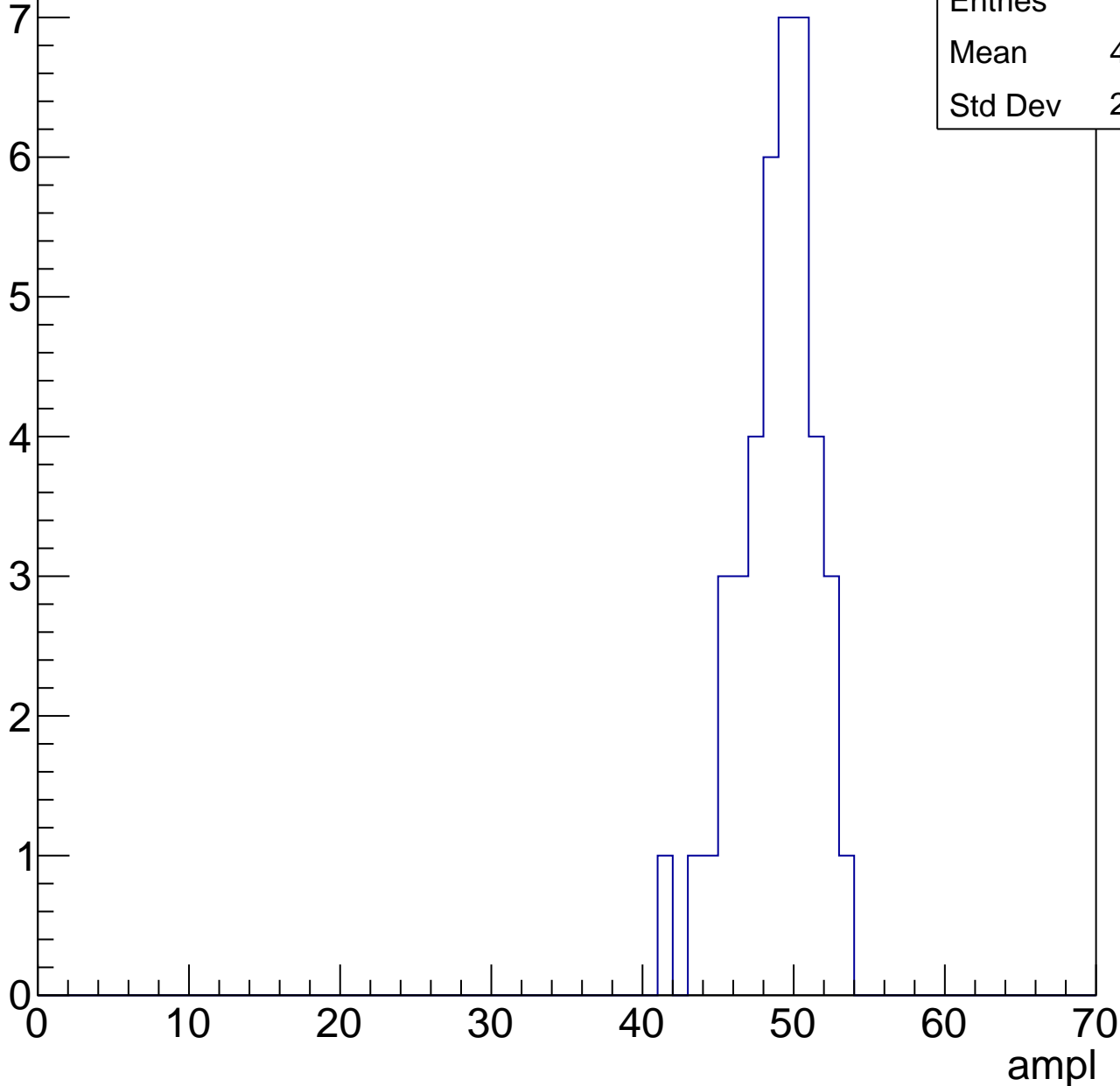


# B1L003S, U6-ch48, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

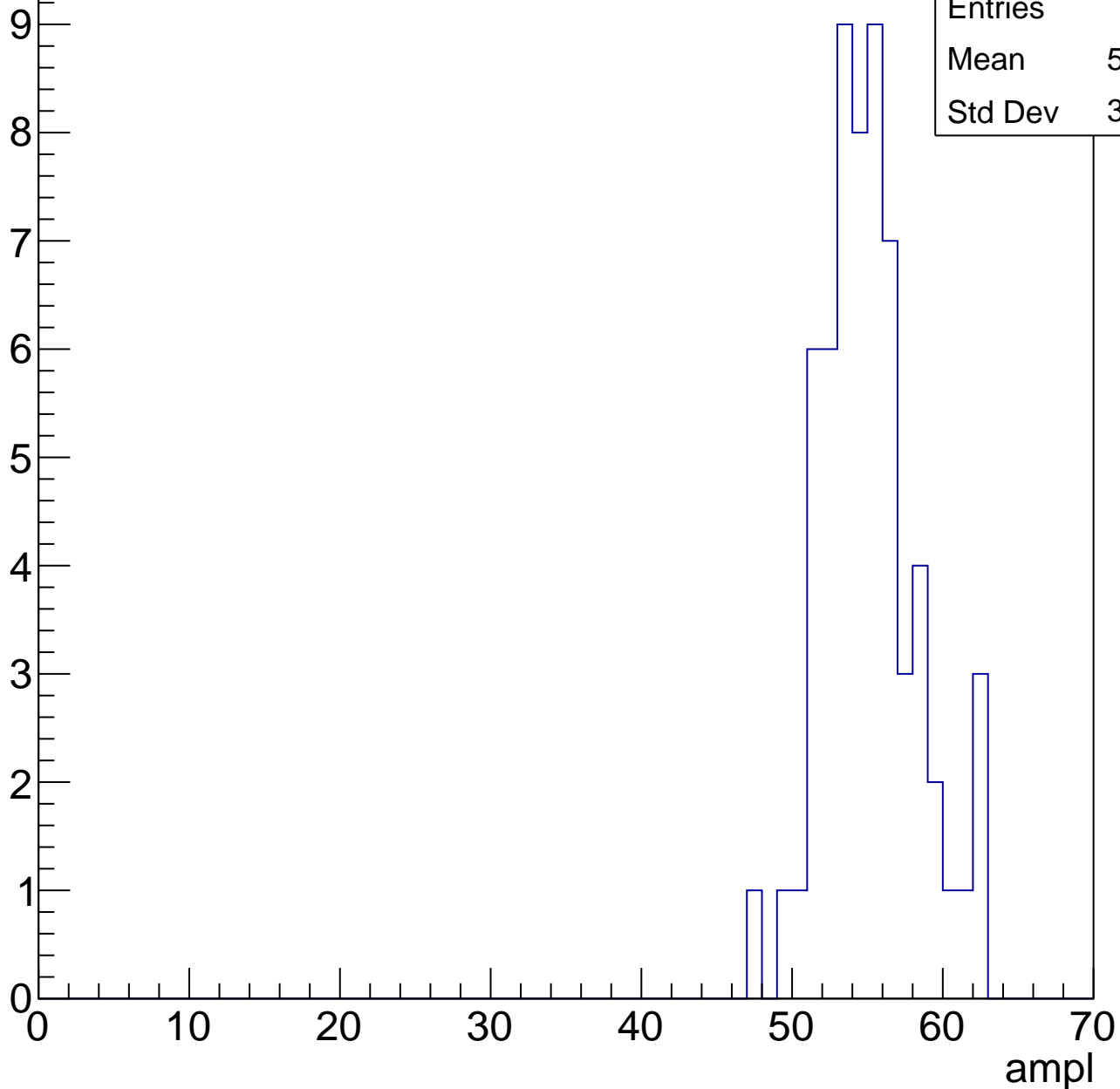
Entries	41
Mean	48.37
Std Dev	2.573



# B1L003S, U6-ch48, adc4

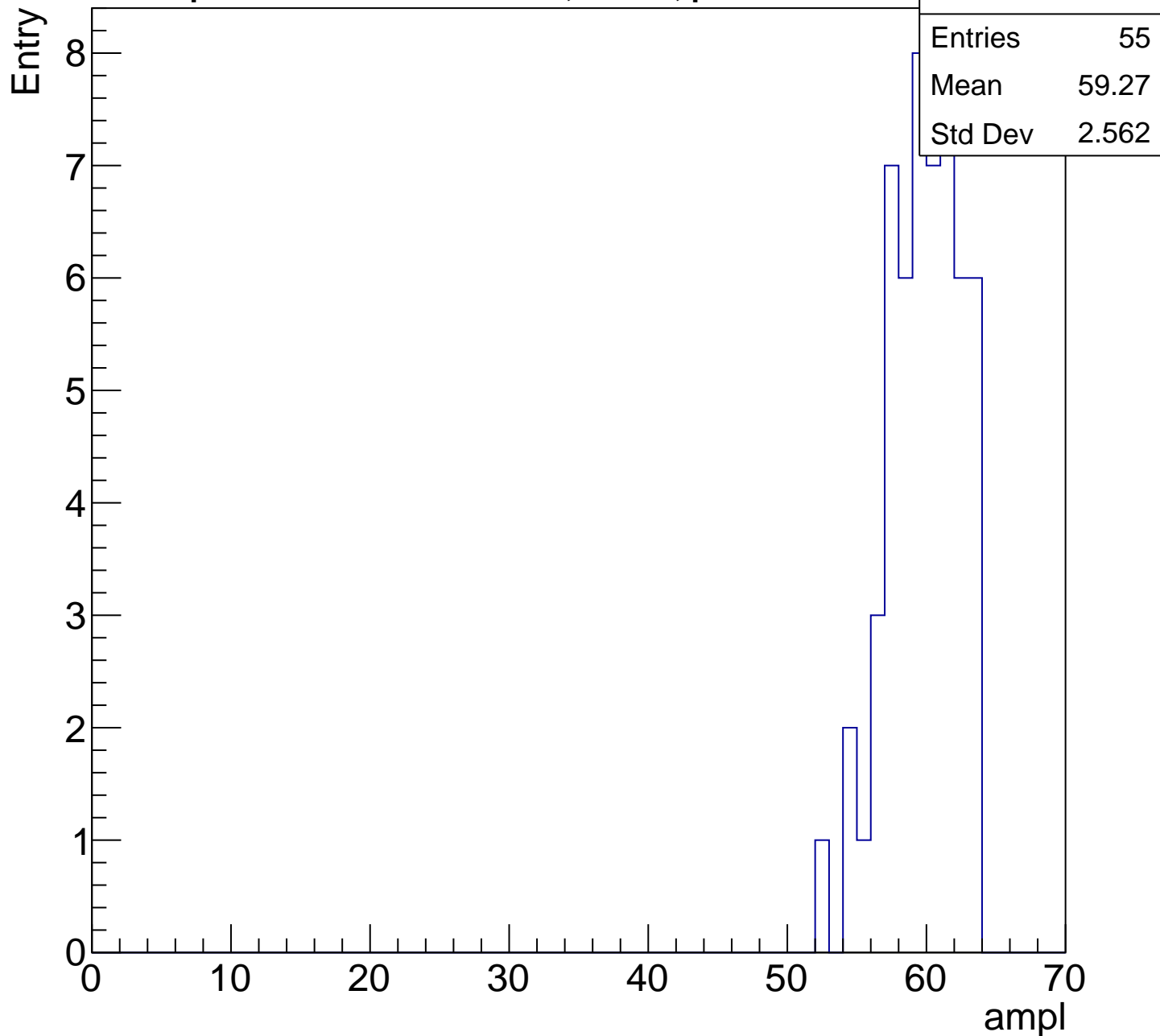
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch48, adc5

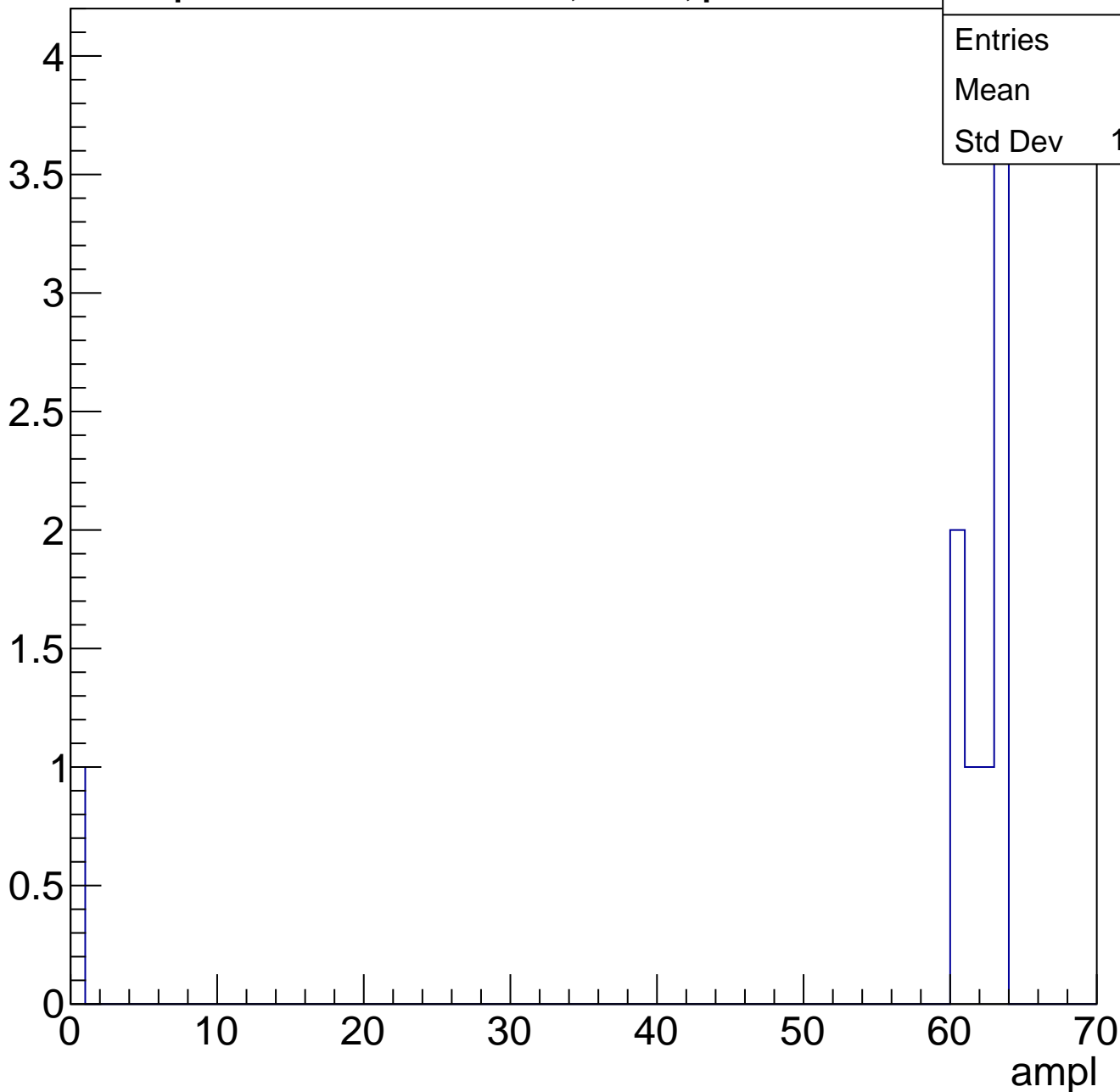
calib\_packv5\_042523\_0143.root, FC#13, port D2



# B1L003S, U6-ch48, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch48, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	23
Std Dev	0

ampl

# B1L003S, U6-ch49, adc0

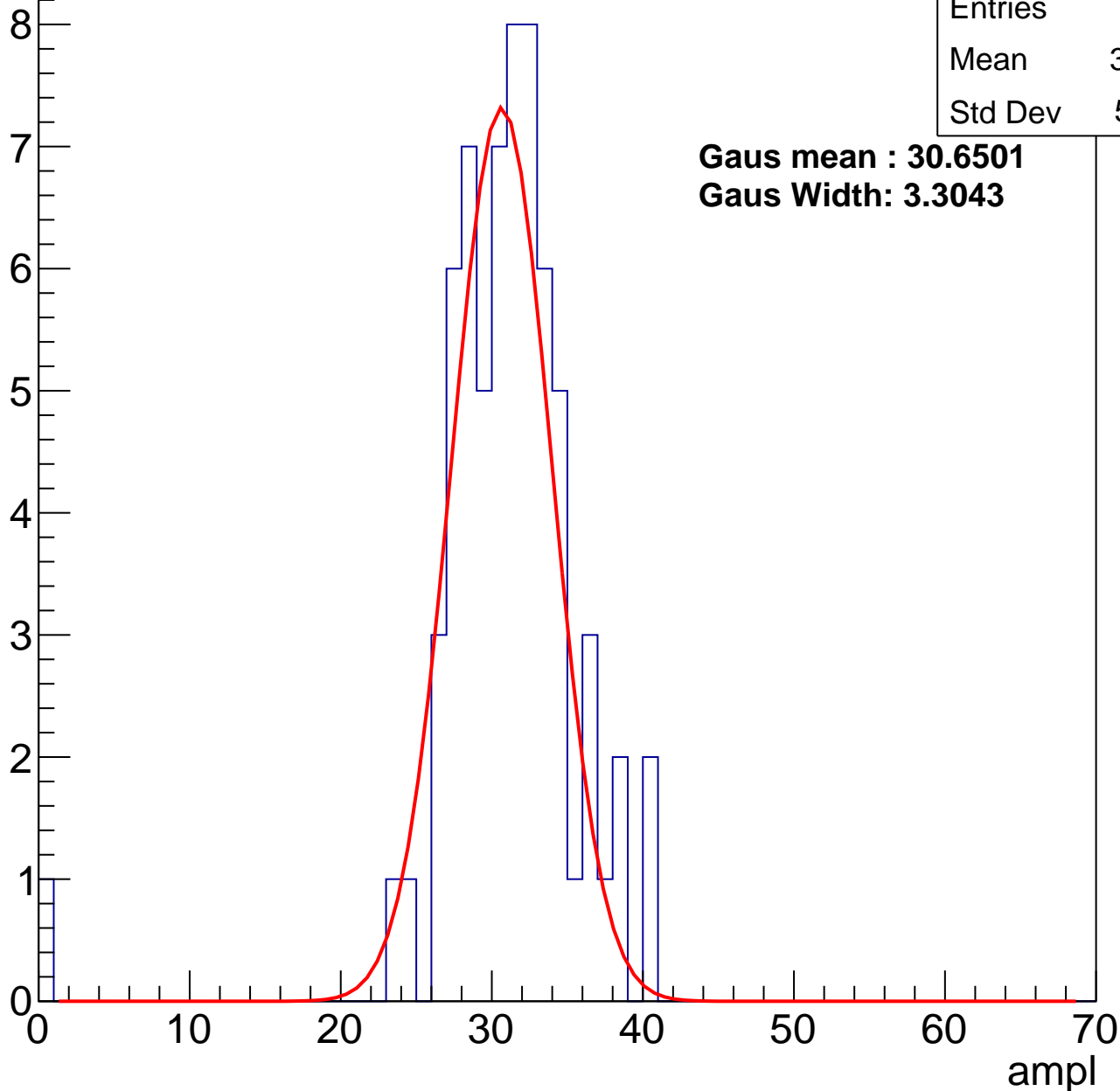
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	30.54
Std Dev	5.161

**Gaus mean : 30.6501**

**Gaus Width: 3.3043**



# B1L003S, U6-ch49, adc1

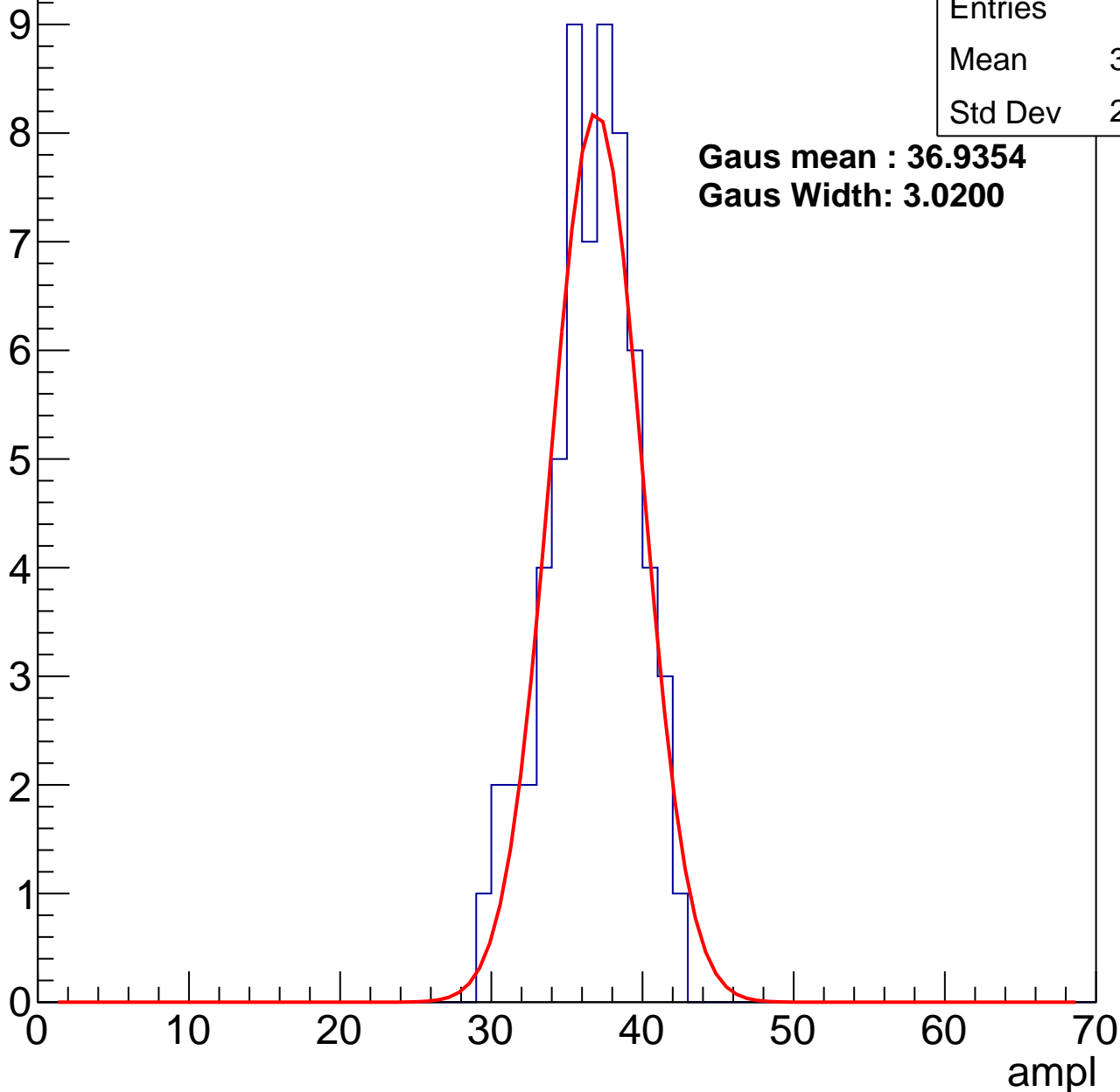
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	36.19
Std Dev	2.916

**Gaus mean : 36.9354**

**Gaus Width: 3.0200**



# B1L003S, U6-ch49, adc2

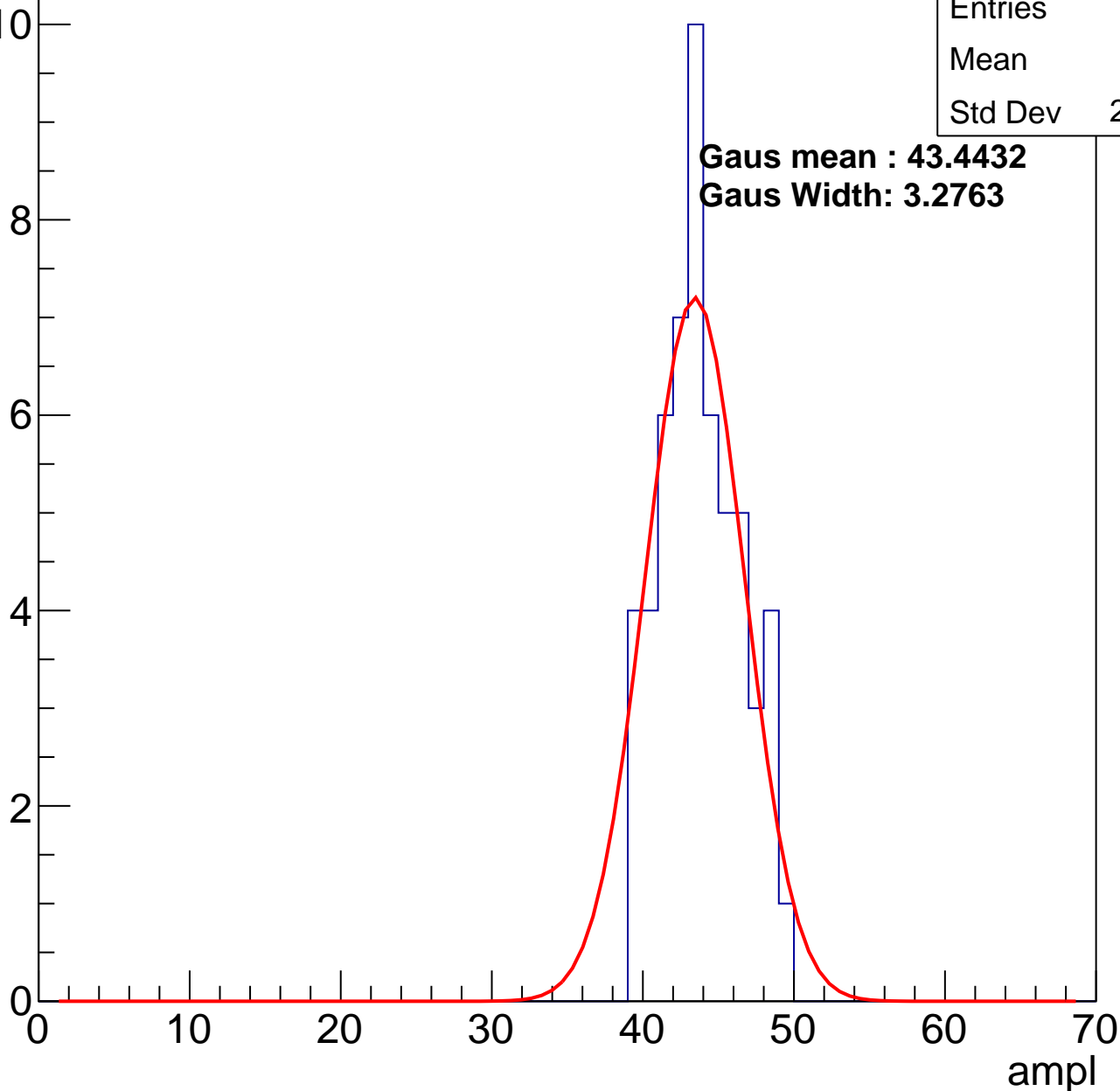
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	43.4
Std Dev	2.619

**Gaus mean : 43.4432**

**Gaus Width: 3.2763**

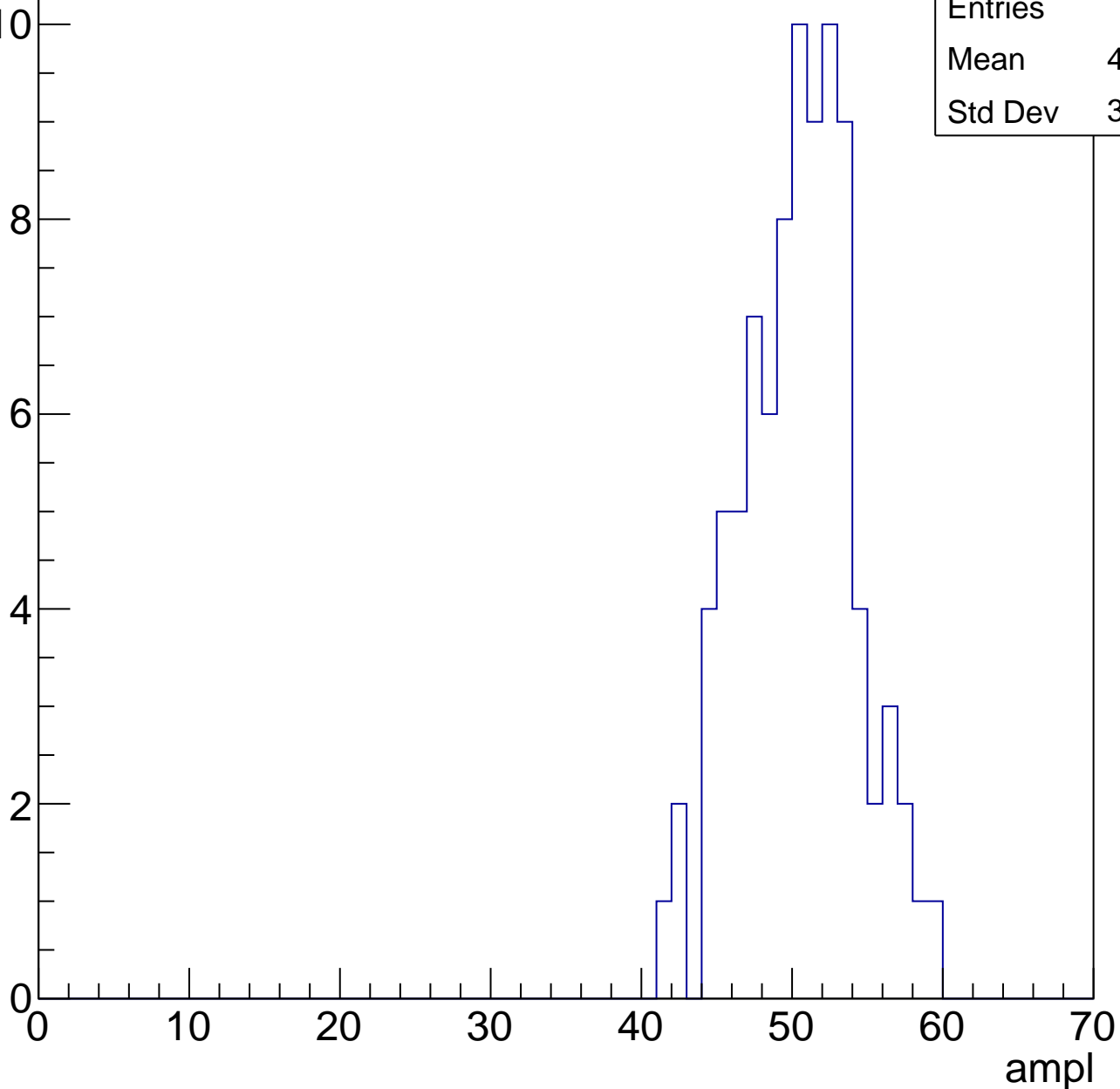


# B1L003S, U6-ch49, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	89
Mean	49.96
Std Dev	3.744

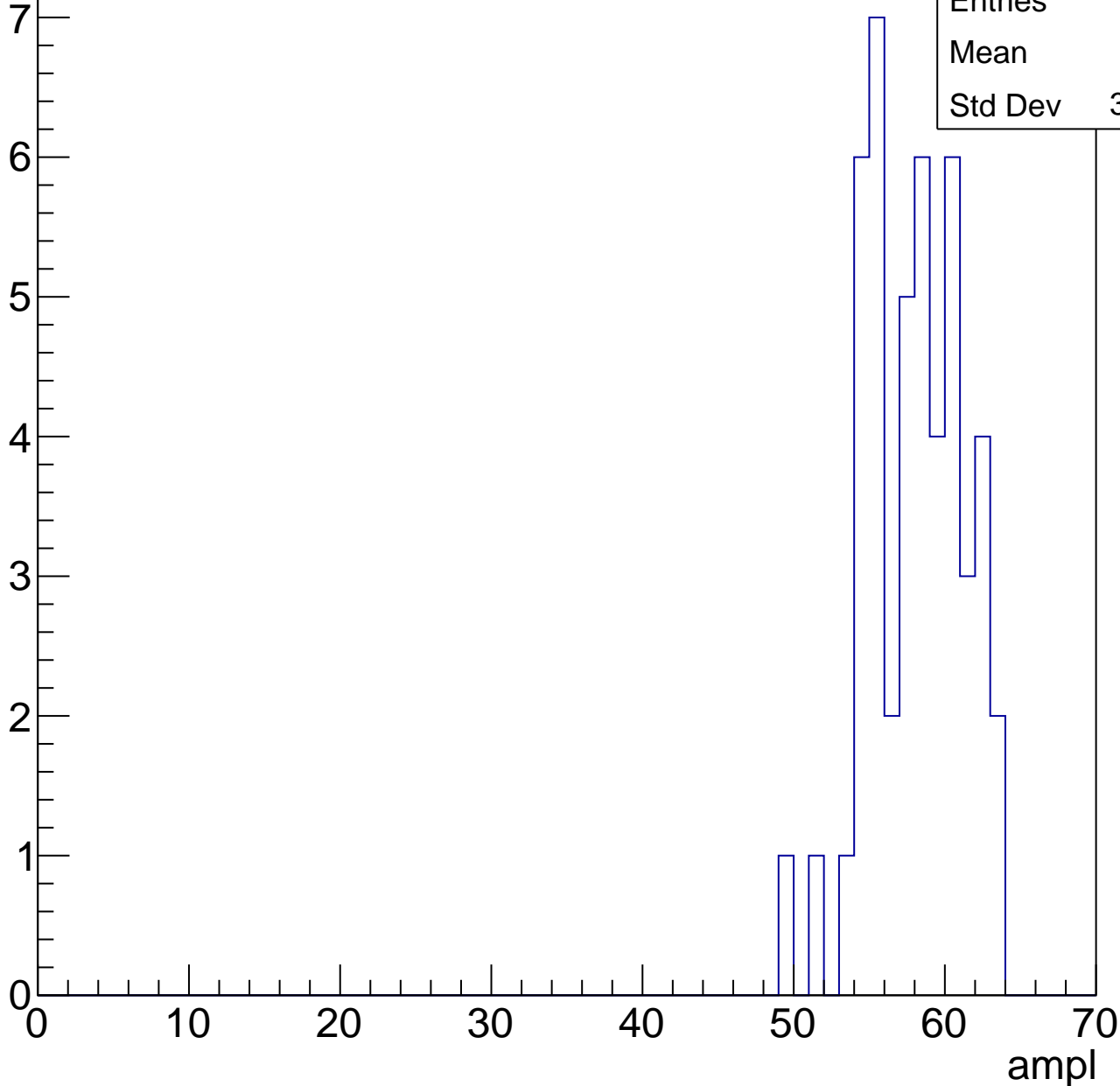


# B1L003S, U6-ch49, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	48
Mean	57.5
Std Dev	3.175

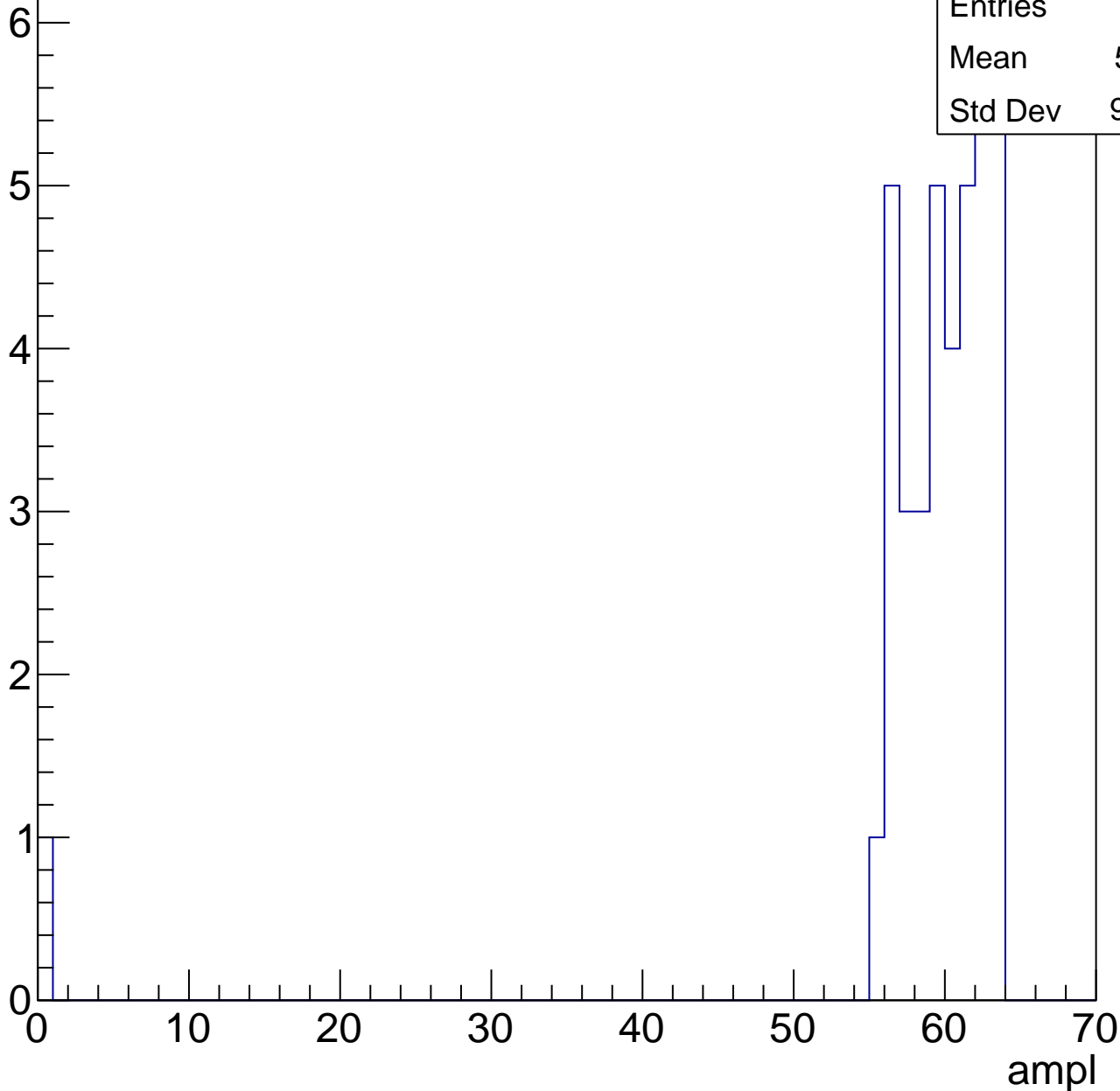


# B1L003S, U6-ch49, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	39
Mean	58.21
Std Dev	9.749



# B1L003S, U6-ch49, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

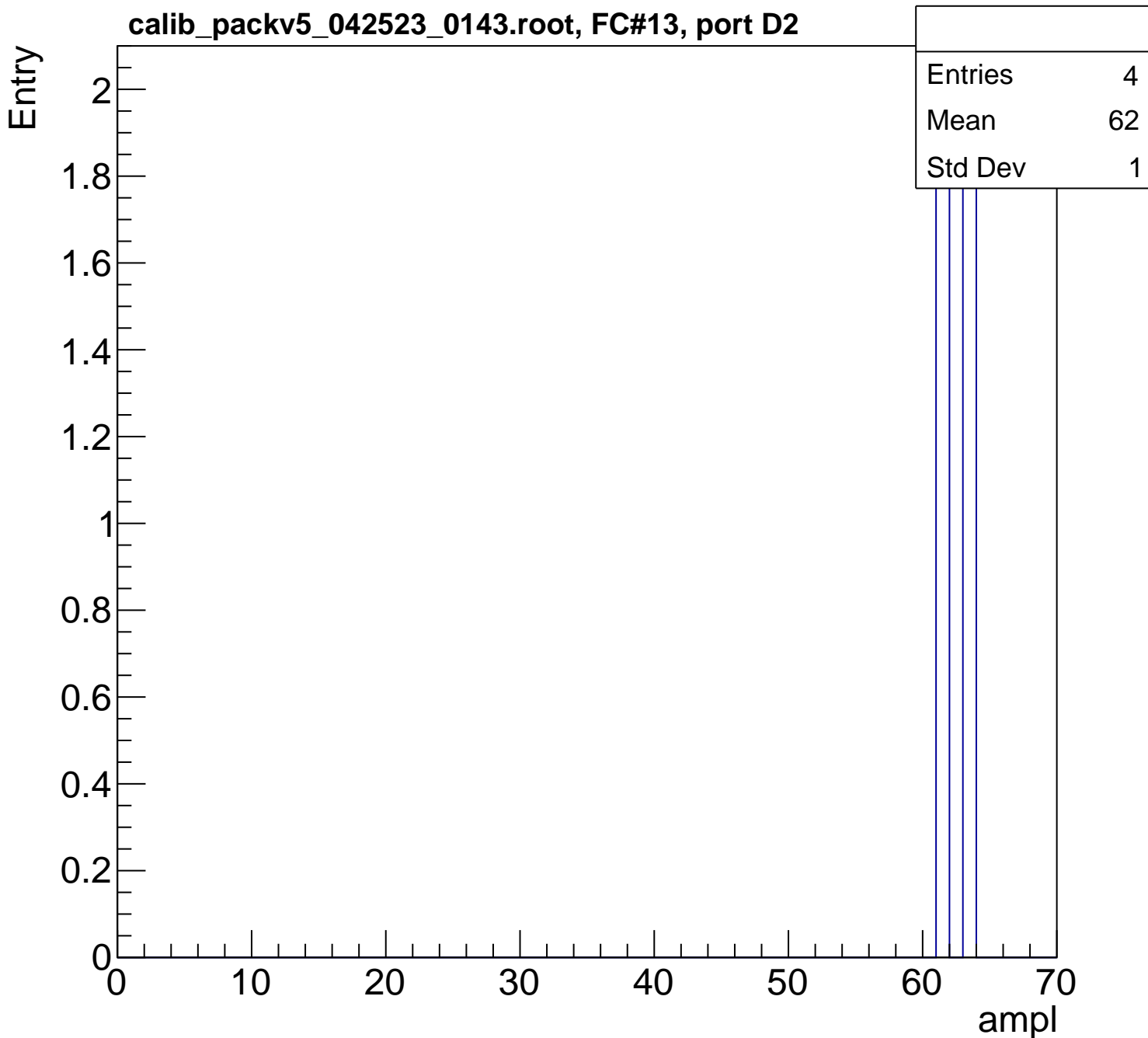
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	62
Std Dev	1

0 10 20 30 40 50 60 70

ampl





# B1L003S, U6-ch49, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L003S, U6-ch50, adc0

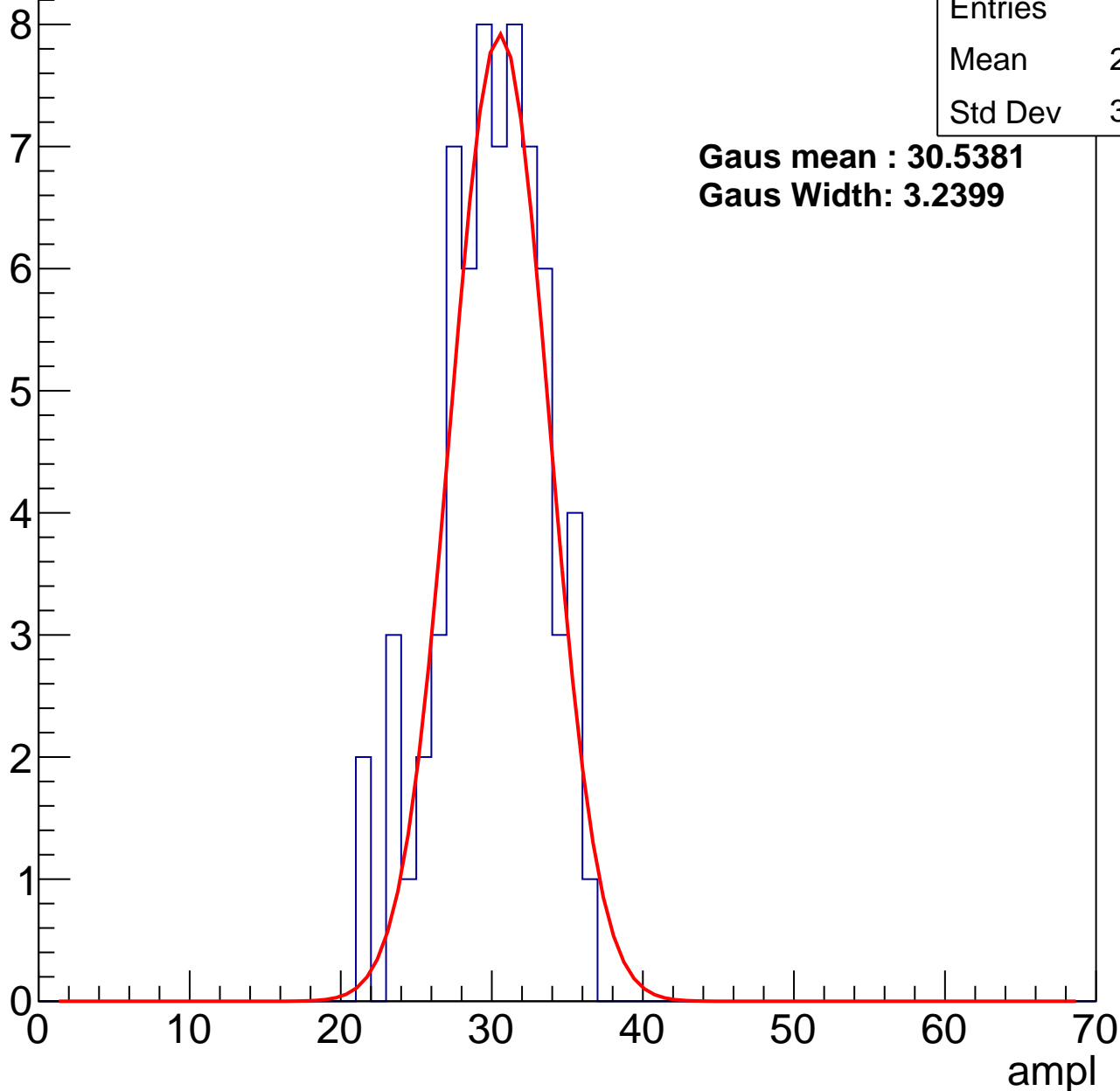
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	29.56
Std Dev	3.427

**Gaus mean : 30.5381**

**Gaus Width: 3.2399**



# B1L003S, U6-ch50, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	69
Mean	36.99
Std Dev	3.155

**Gaus mean : 37.5385**

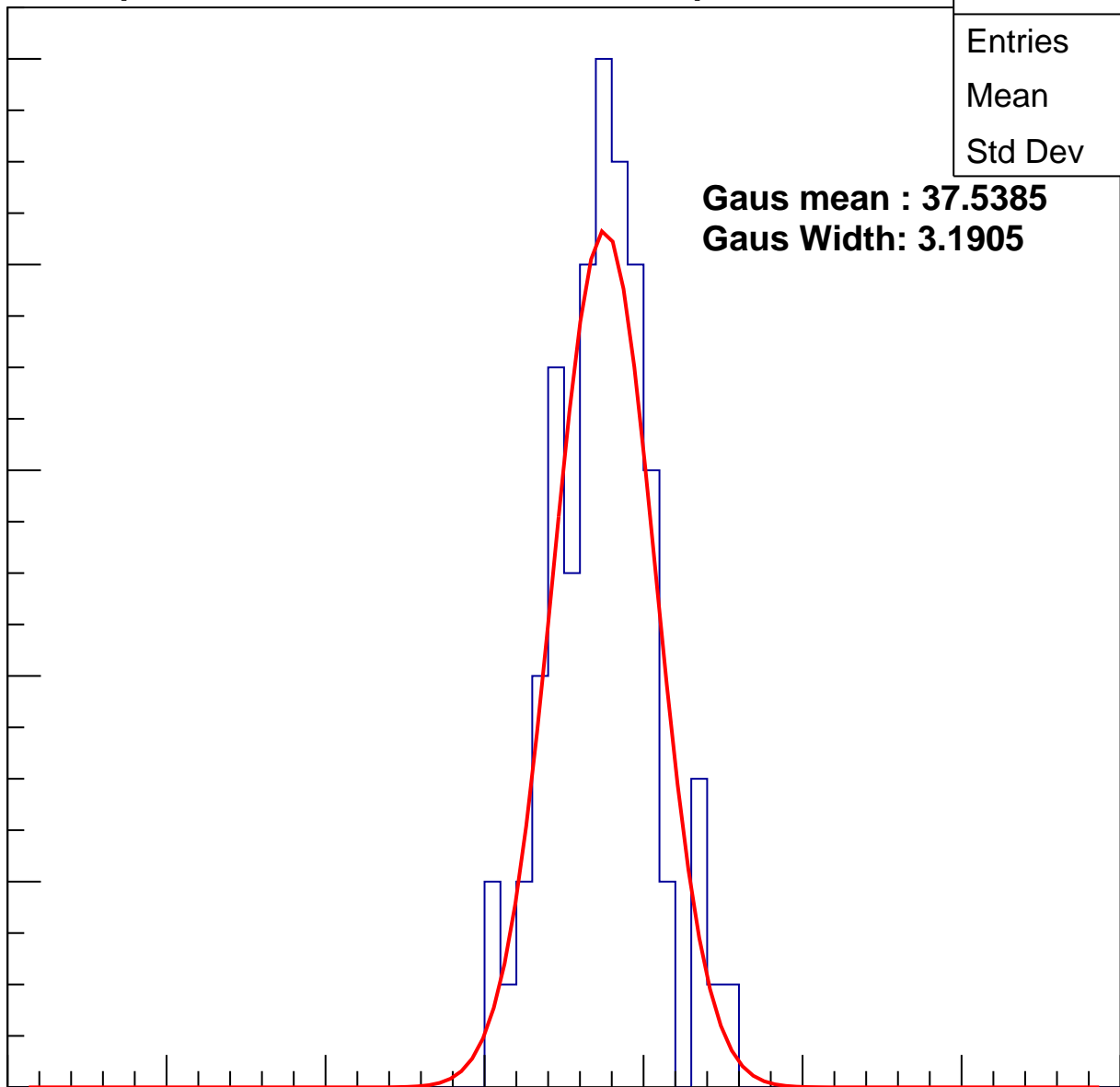
**Gaus Width: 3.1905**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U6-ch50, adc2

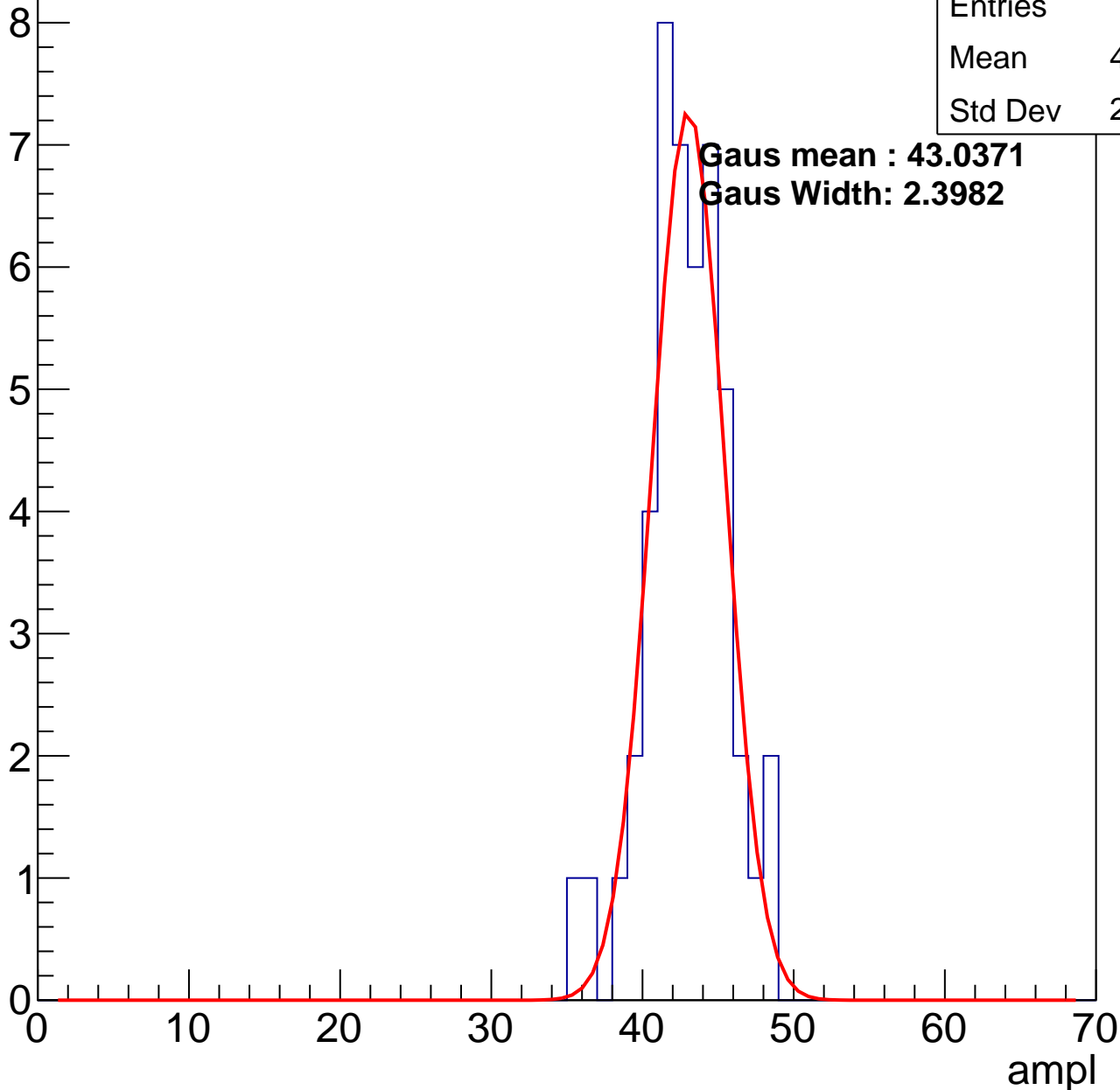
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	47
Mean	42.45
Std Dev	2.696

**Gaus mean : 43.0371**

**Gaus Width: 2.3982**



# B1L003S, U6-ch50, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

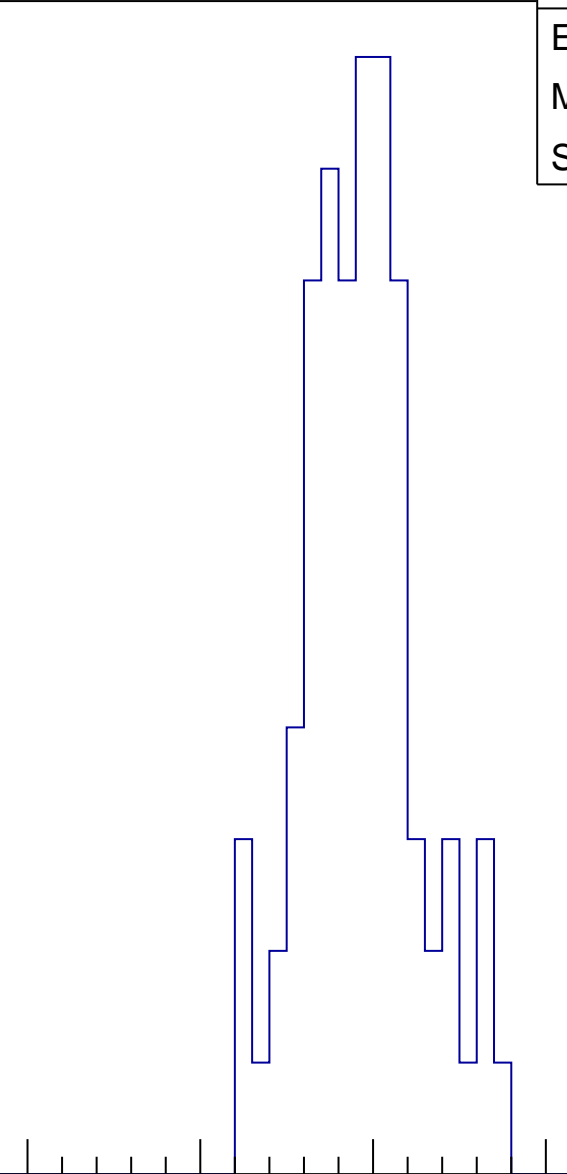
Entries	76
Mean	48.87
Std Dev	3.314

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

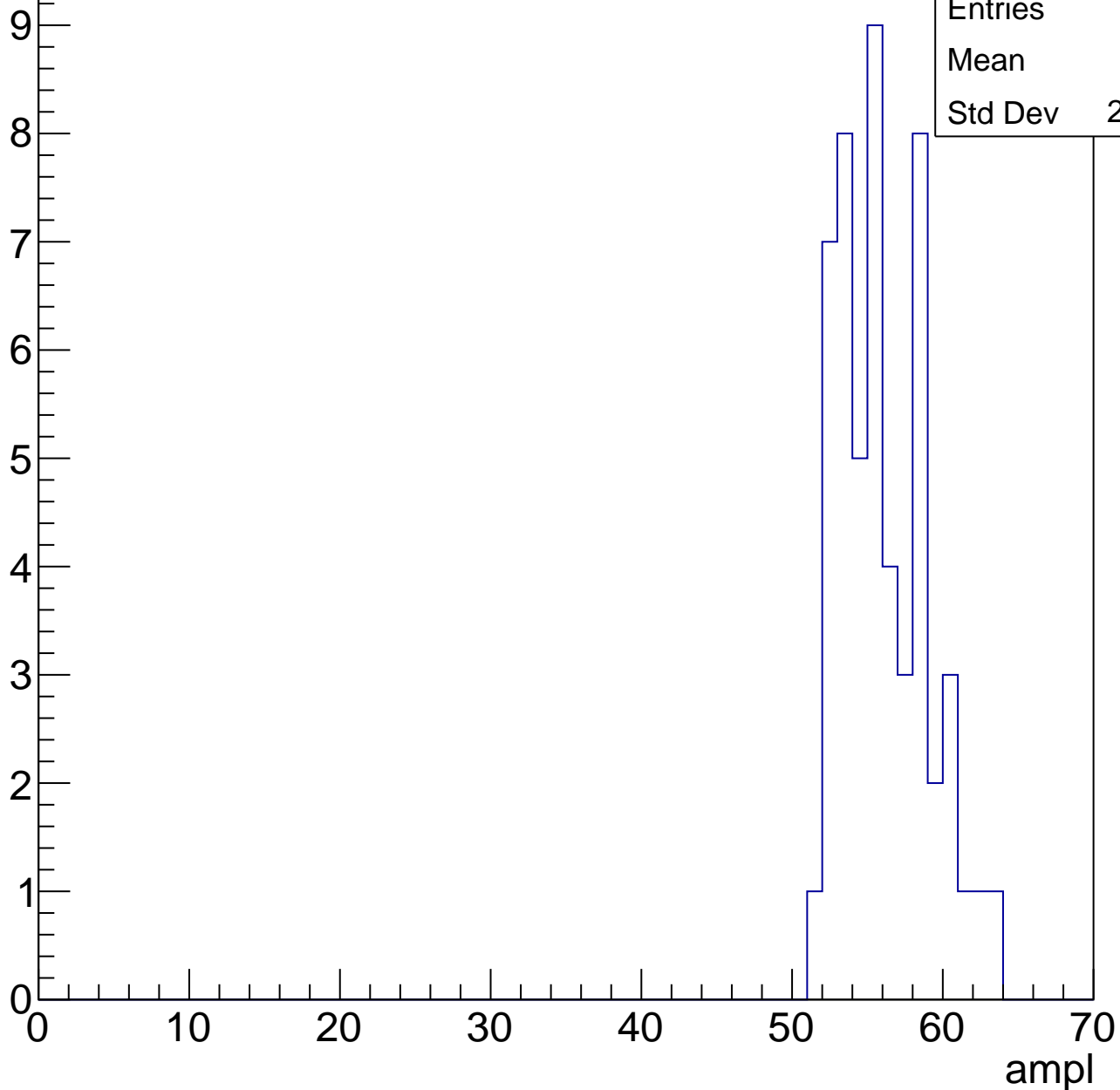
ampl



# B1L003S, U6-ch50, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

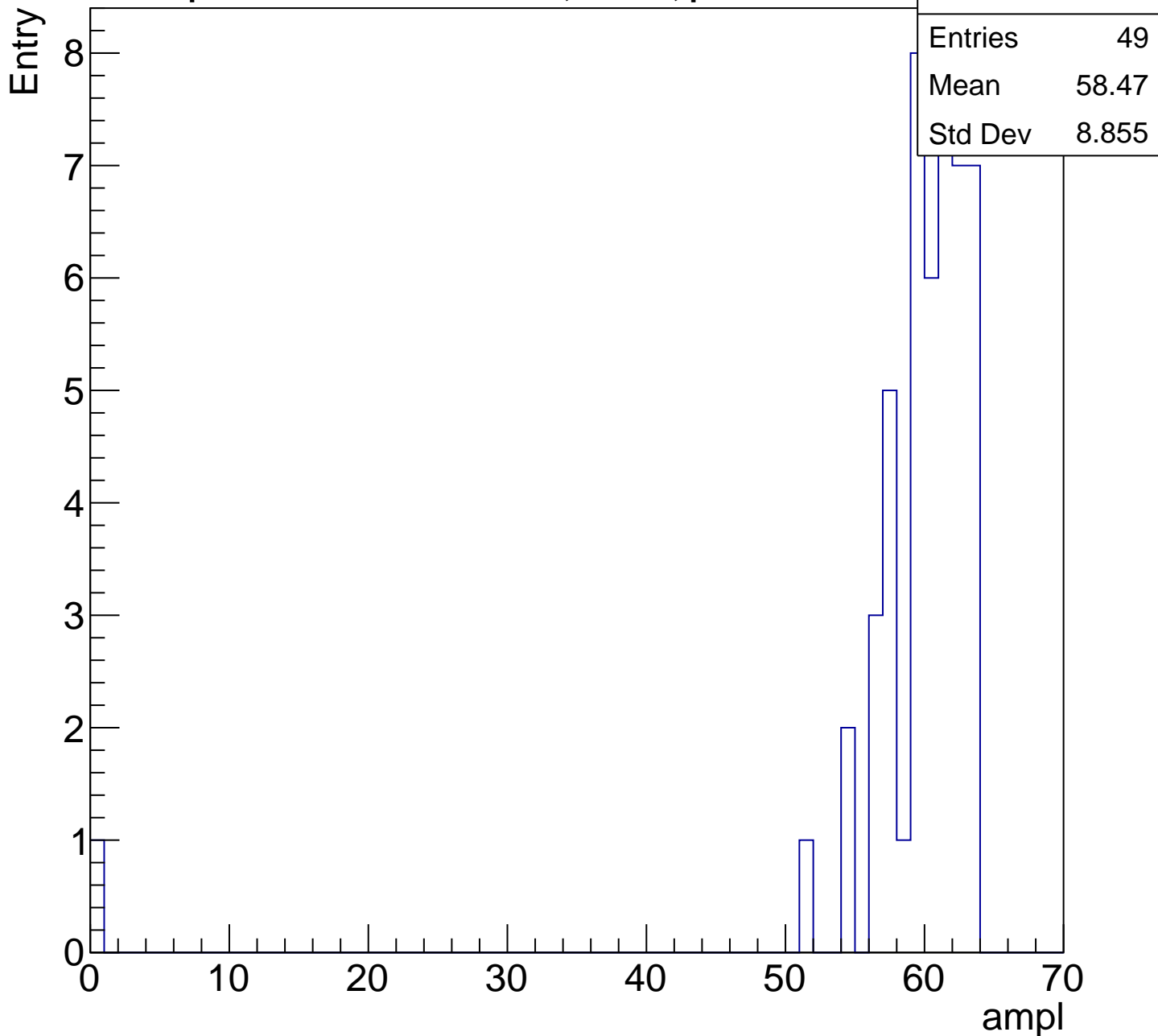
Entry



Entries	53
Mean	55.6
Std Dev	2.884

# B1L003S, U6-ch50, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2



# B1L003S, U6-ch50, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

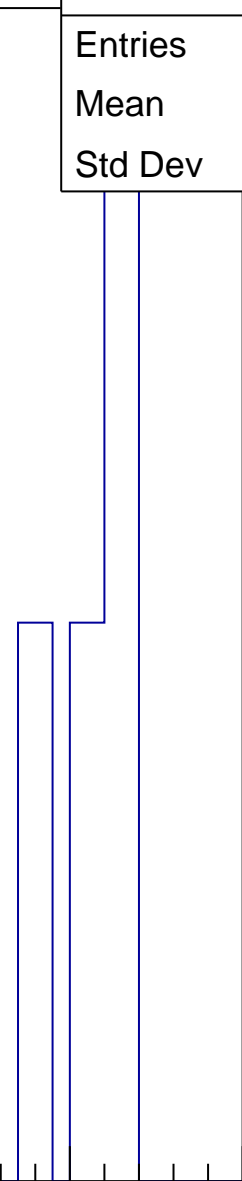
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	8
Mean	60.75
Std Dev	2.107

0 10 20 30 40 50 60 70

ampl





# B1L003S, U6-ch50, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U6-ch51, adc0

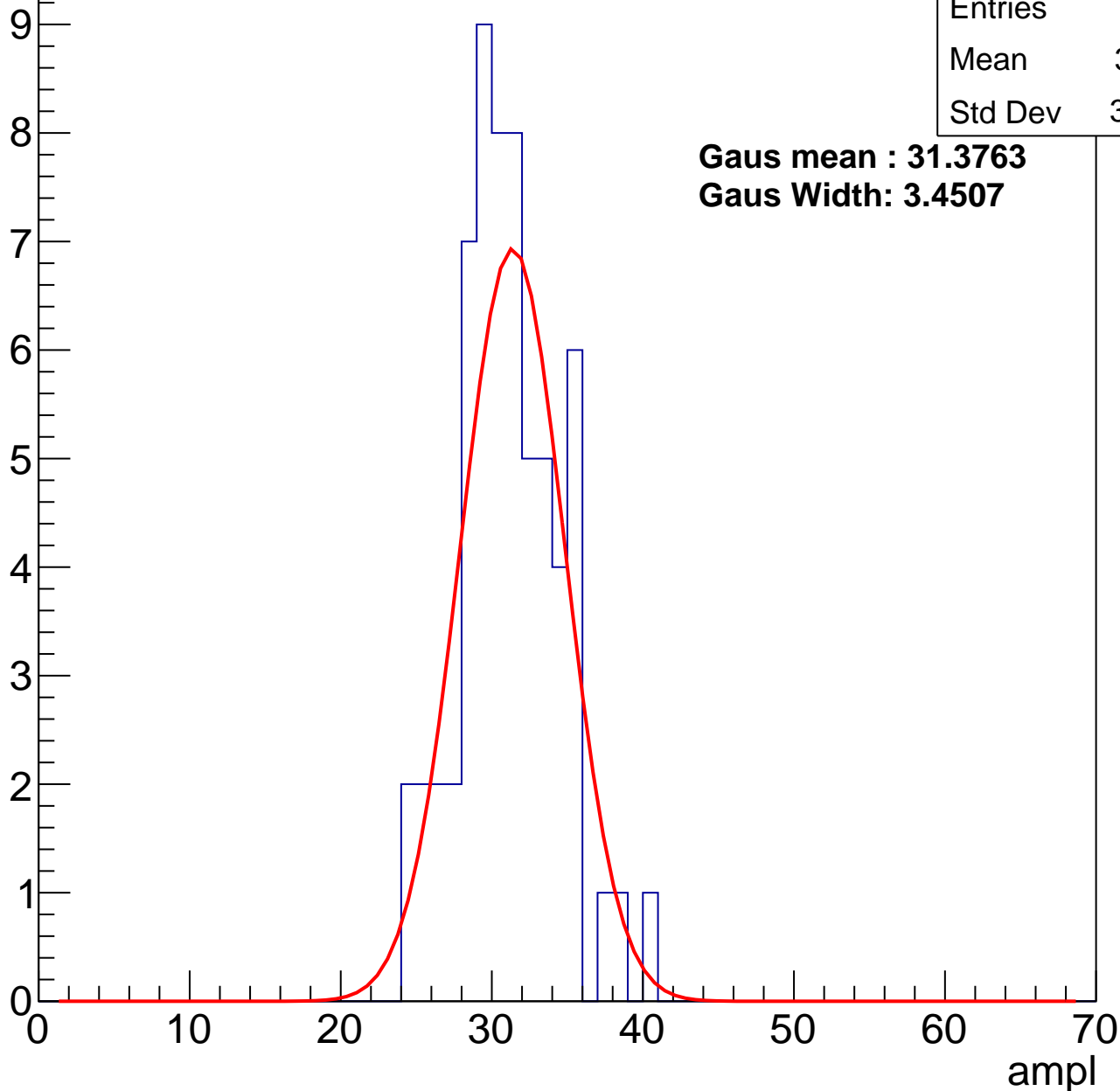
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	30.71
Std Dev	3.278

**Gaus mean : 31.3763**

**Gaus Width: 3.4507**



# B1L003S, U6-ch51, adc1

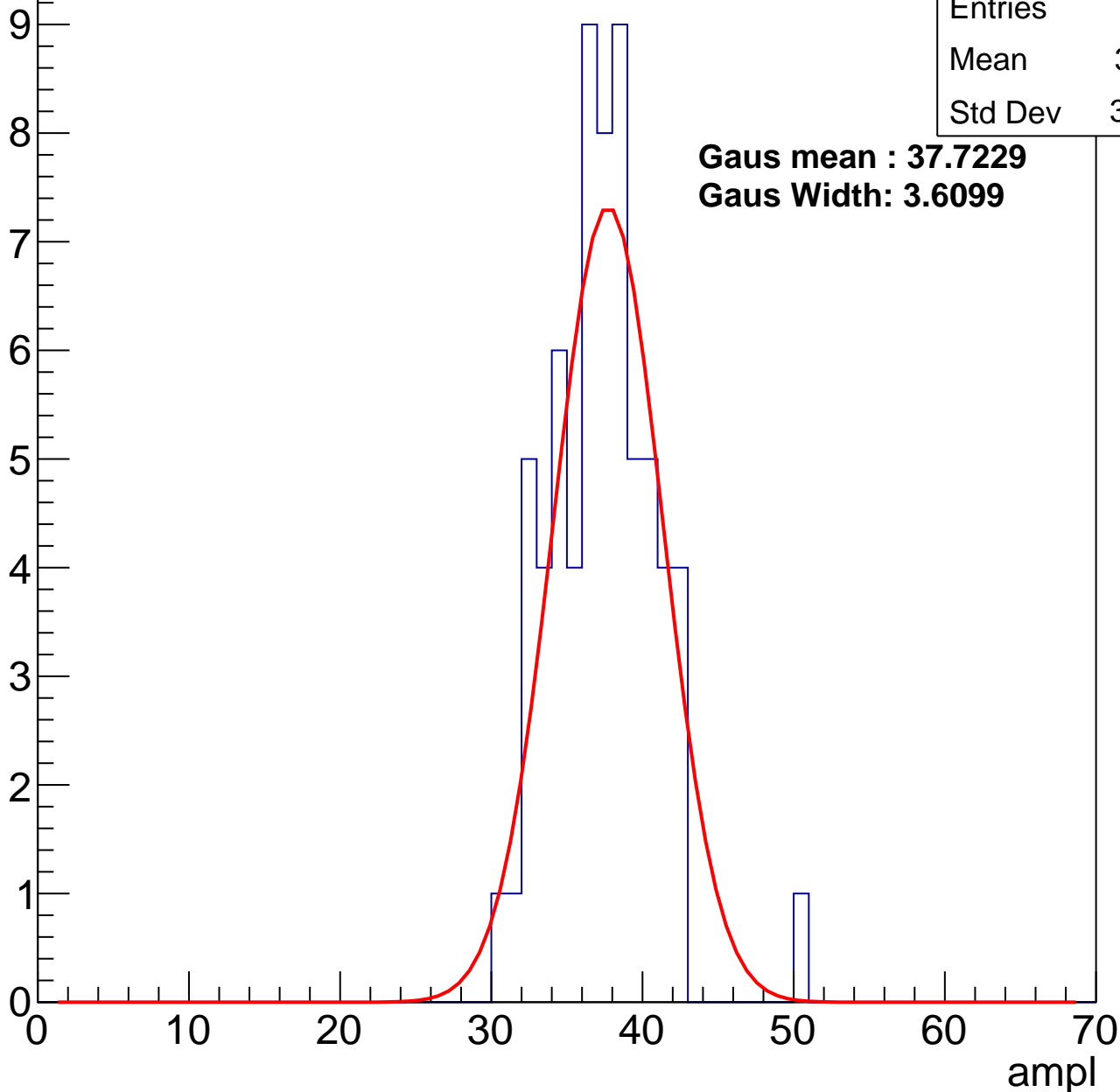
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	36.91
Std Dev	3.392

**Gaus mean : 37.7229**

**Gaus Width: 3.6099**



# B1L003S, U6-ch51, adc2

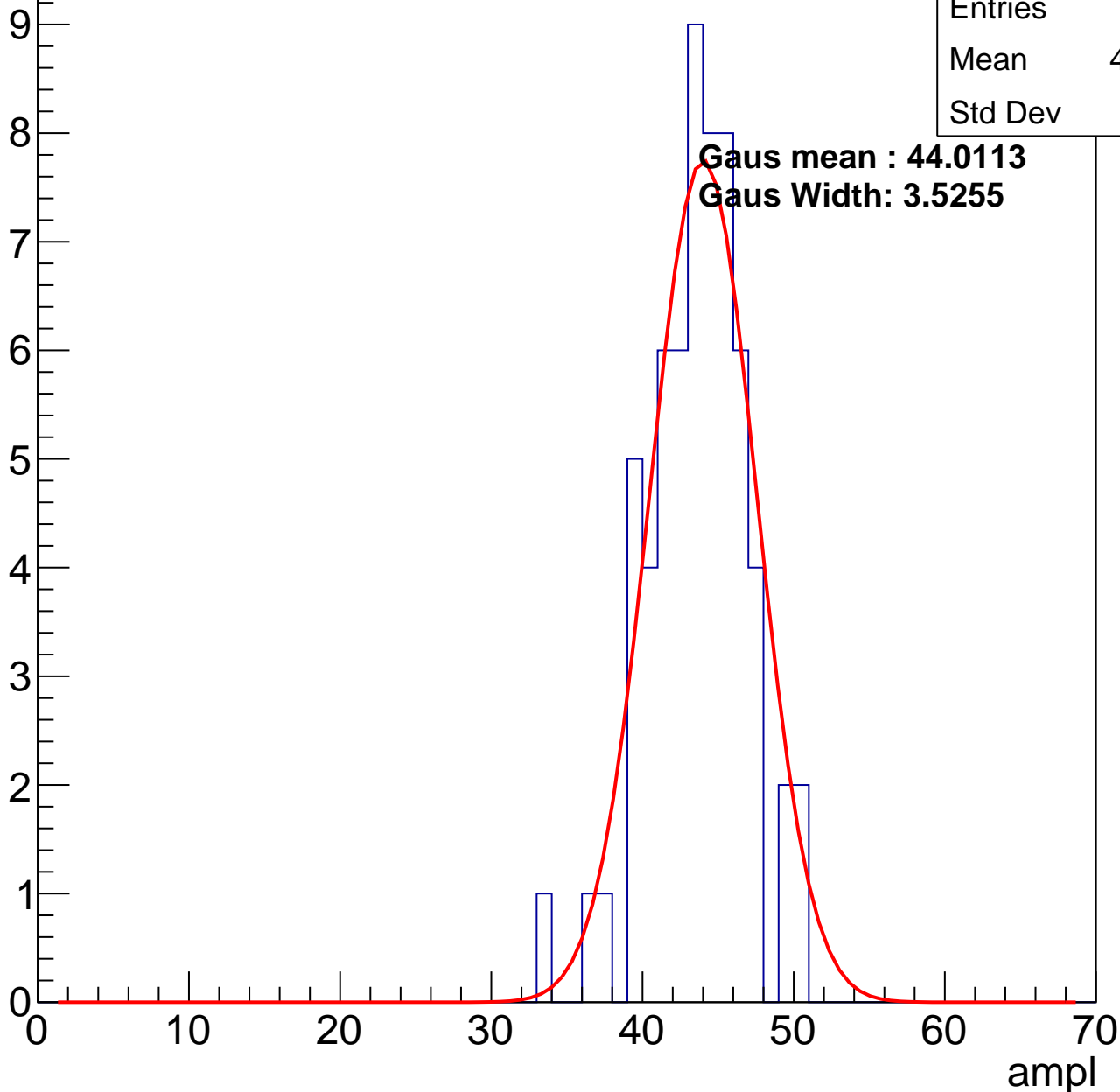
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	43.17
Std Dev	3.23

**Gaus mean : 44.0113**

**Gaus Width: 3.5255**

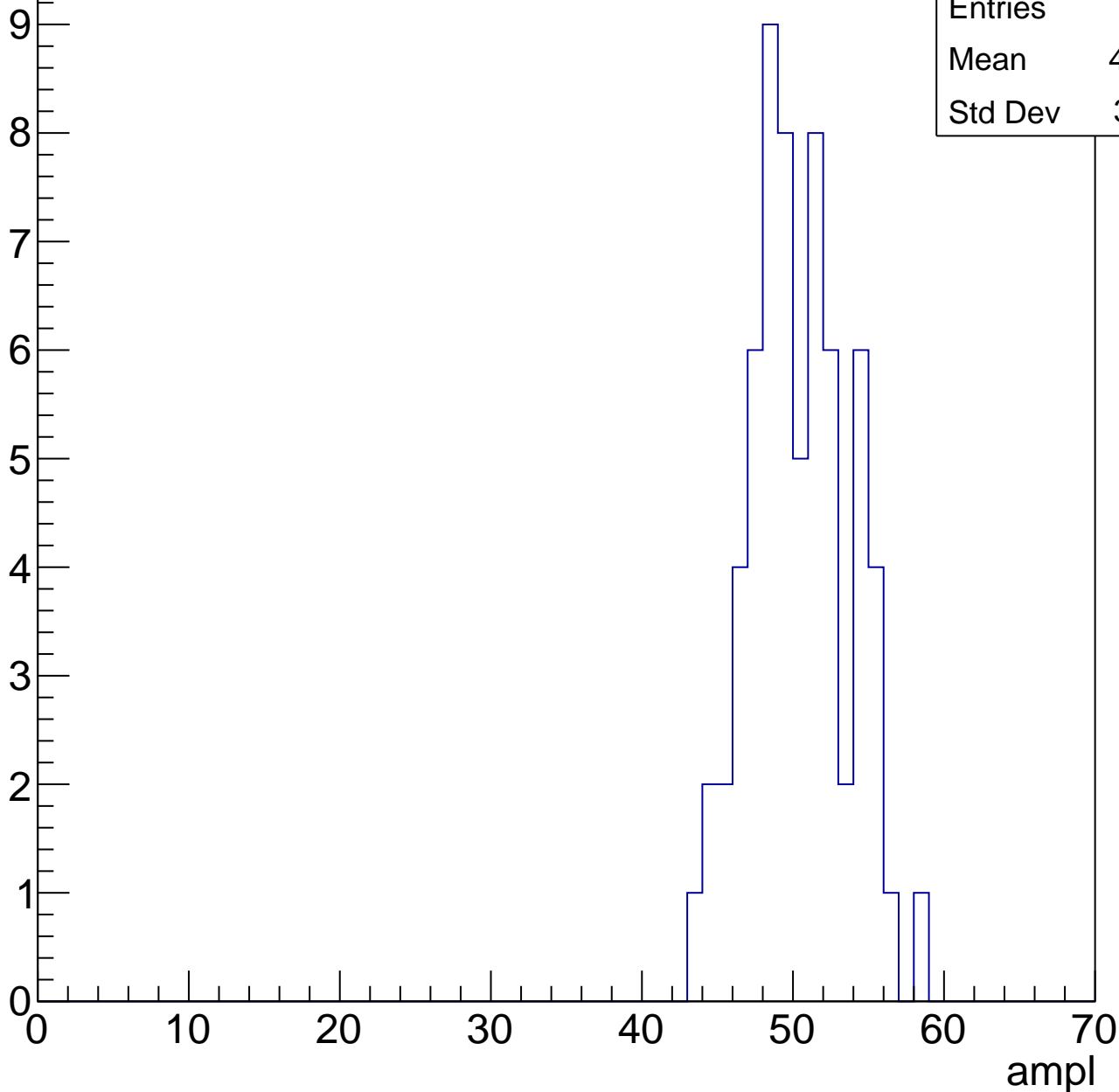


# B1L003S, U6-ch51, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	49.92
Std Dev	3.231

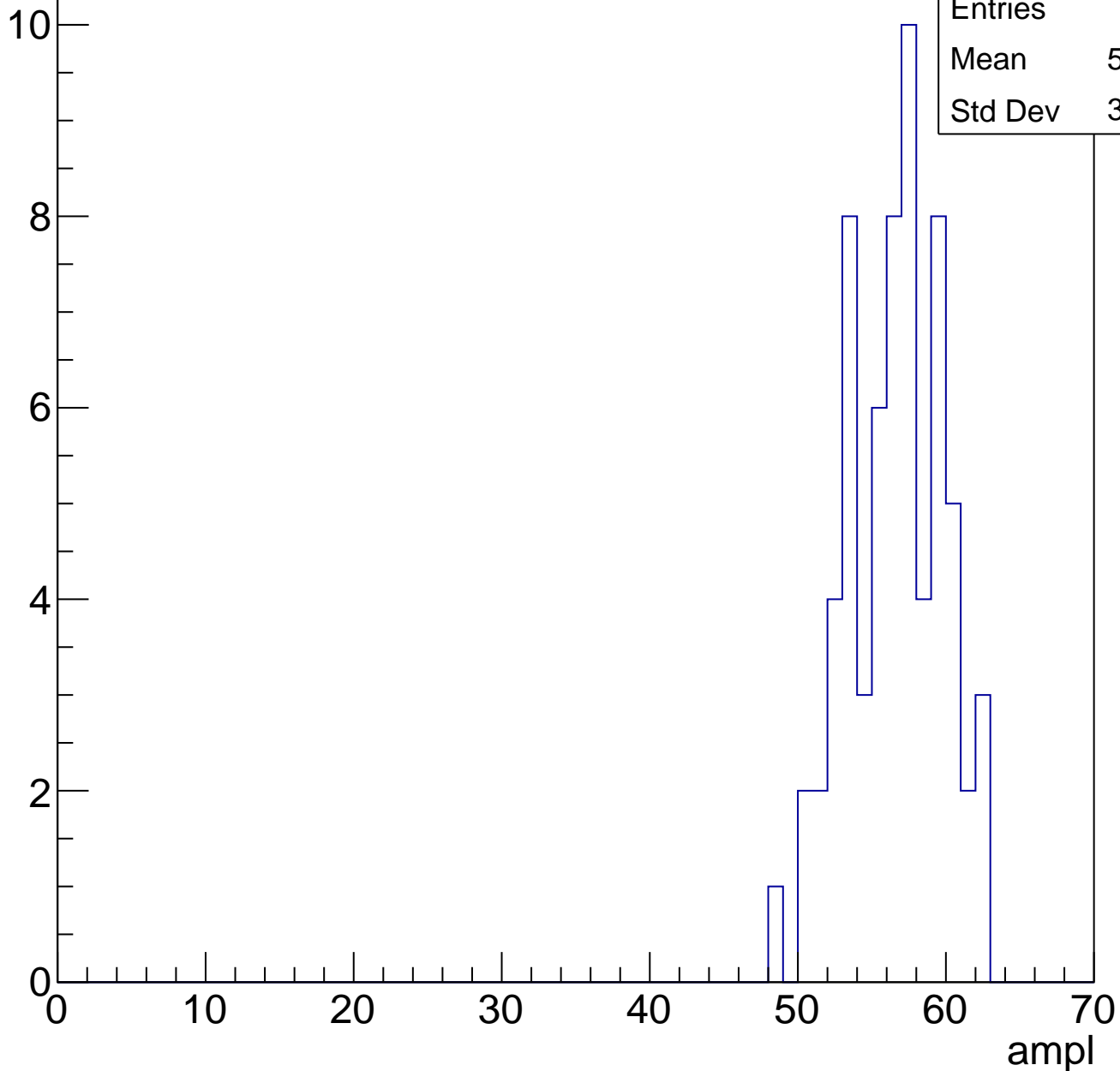


# B1L003S, U6-ch51, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	66
Mean	56.12
Std Dev	3.198

Entry

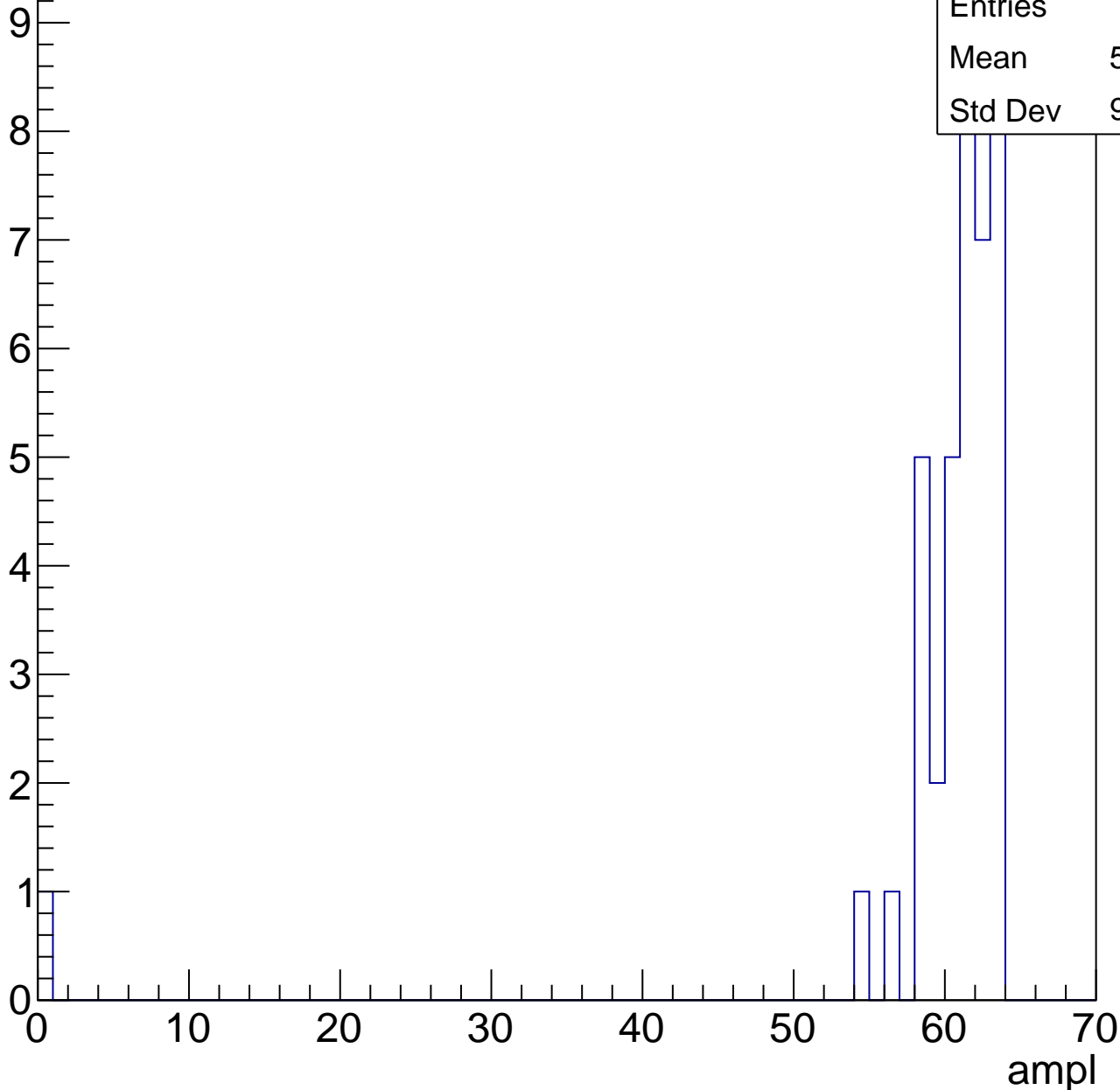


# B1L003S, U6-ch51, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	39
Mean	59.15
Std Dev	9.823



# B1L003S, U6-ch51, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L003S, U6-ch51, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch52, adc0

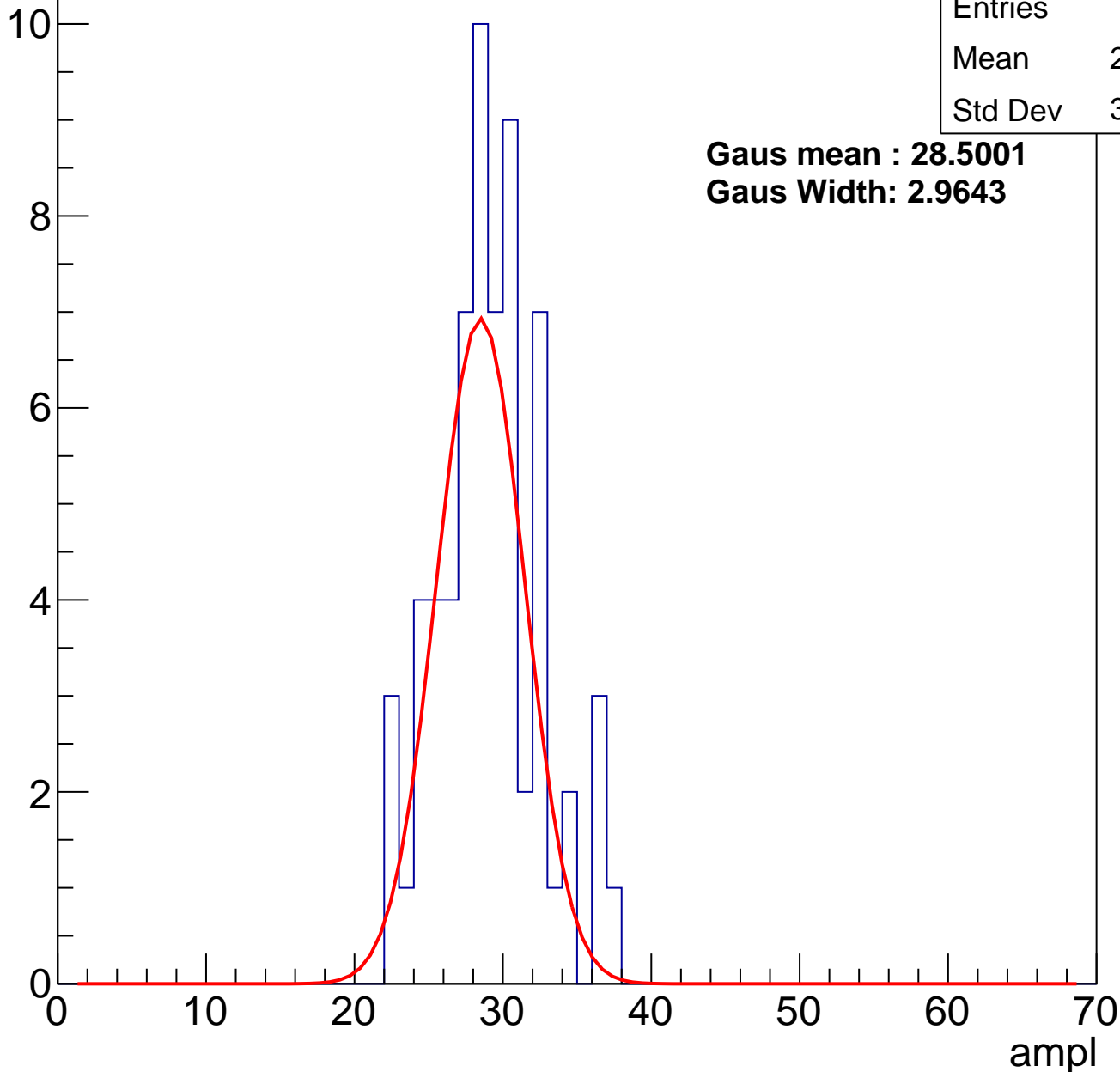
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	65
Mean	28.66
Std Dev	3.443

**Gaus mean : 28.5001**

**Gaus Width: 2.9643**

Entry



# B1L003S, U6-ch52, adc1

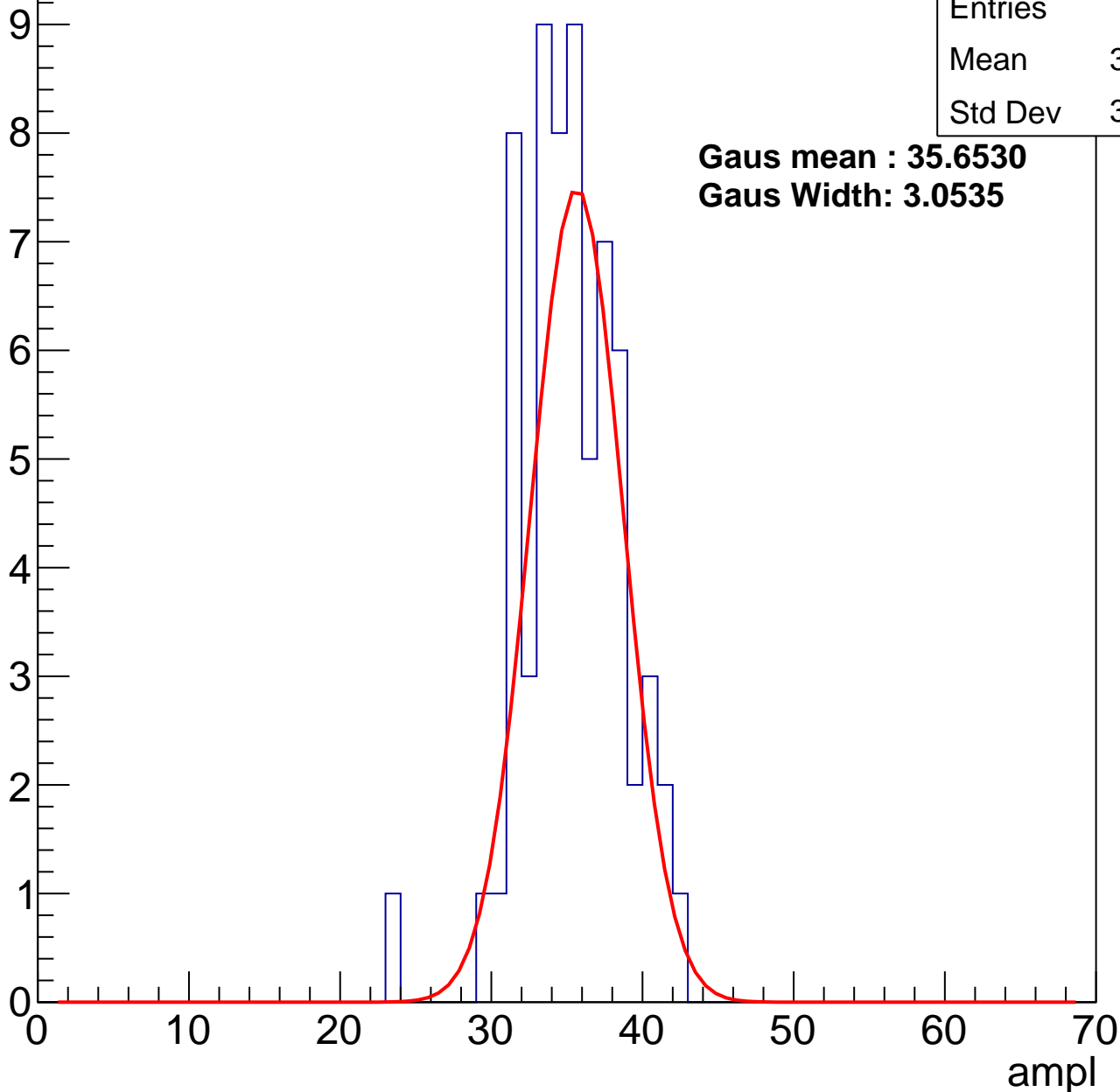
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	34.83
Std Dev	3.296

**Gaus mean : 35.6530**

**Gaus Width: 3.0535**



# B1L003S, U6-ch52, adc2

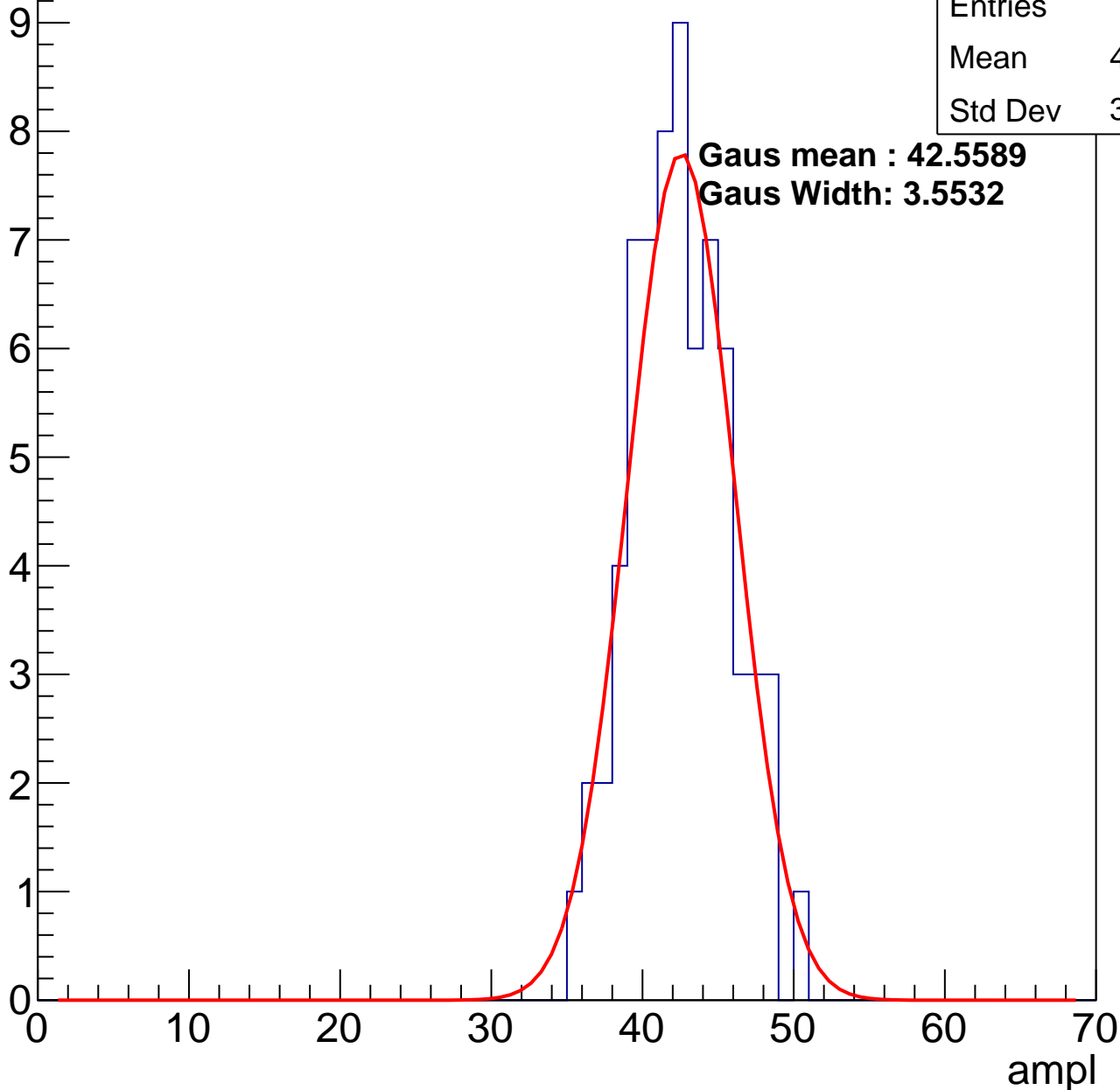
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	42.04
Std Dev	3.223

**Gaus mean : 42.5589**

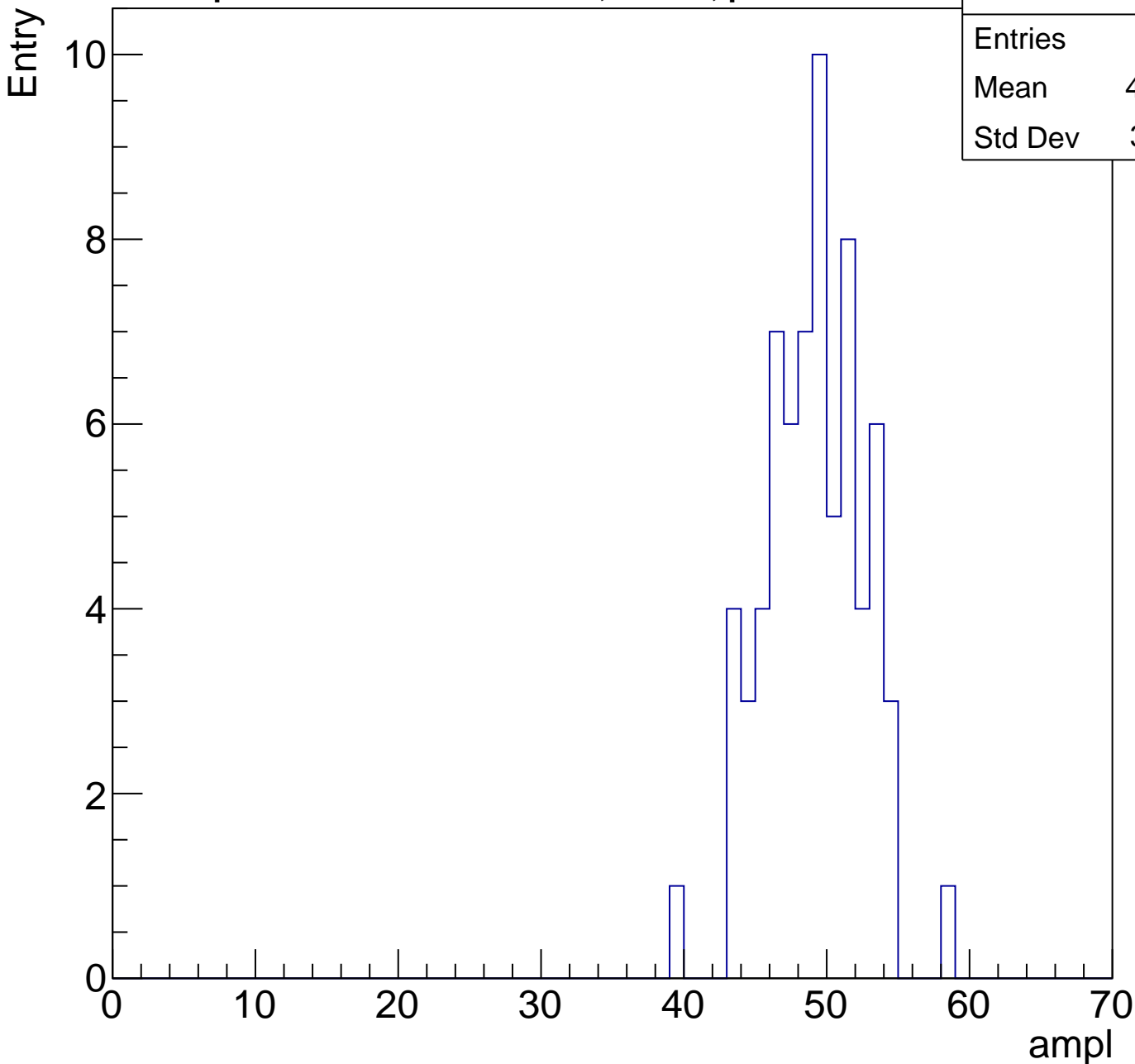
**Gaus Width: 3.5532**



# B1L003S, U6-ch52, adc3

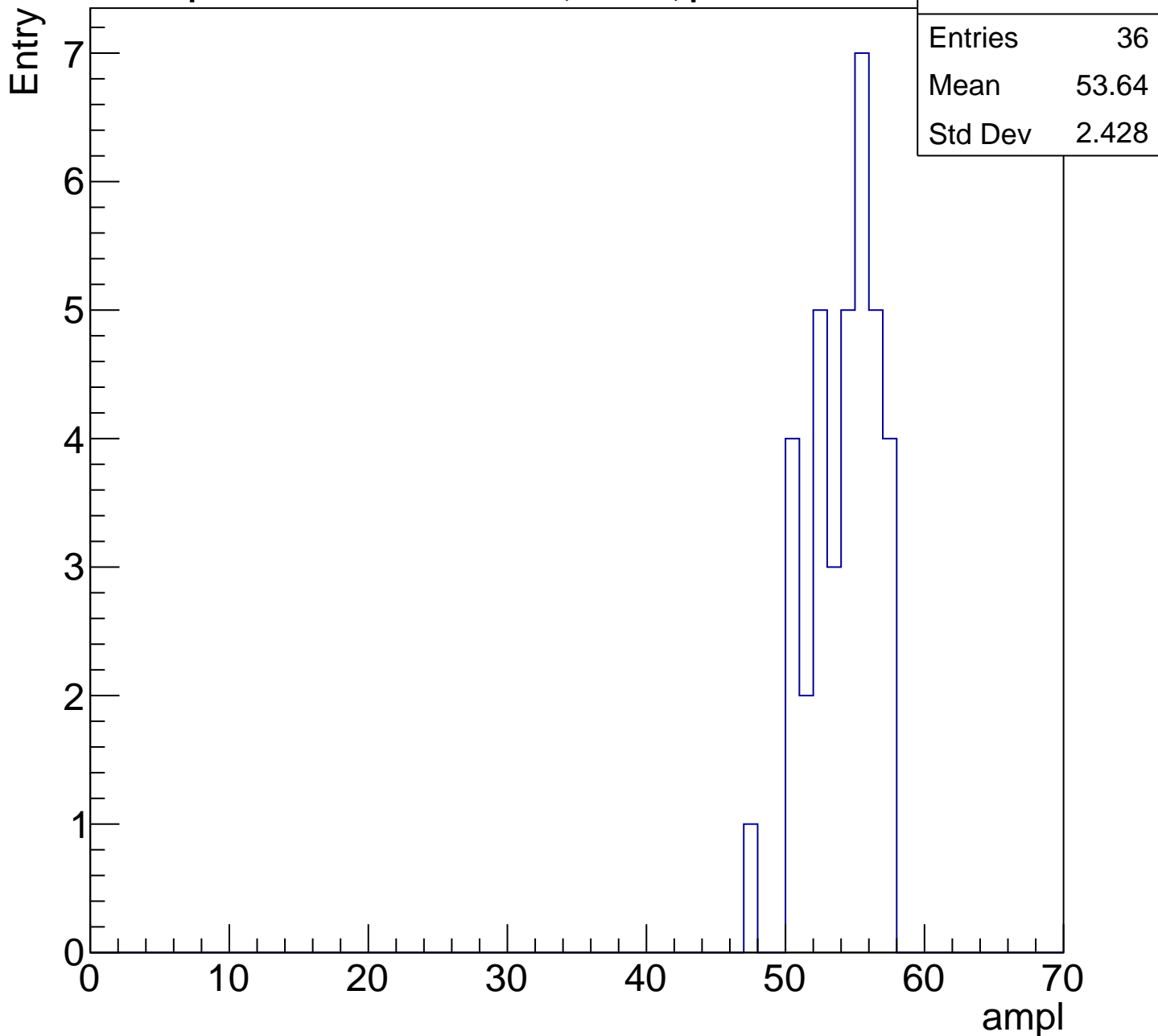
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	69
Mean	48.65
Std Dev	3.391



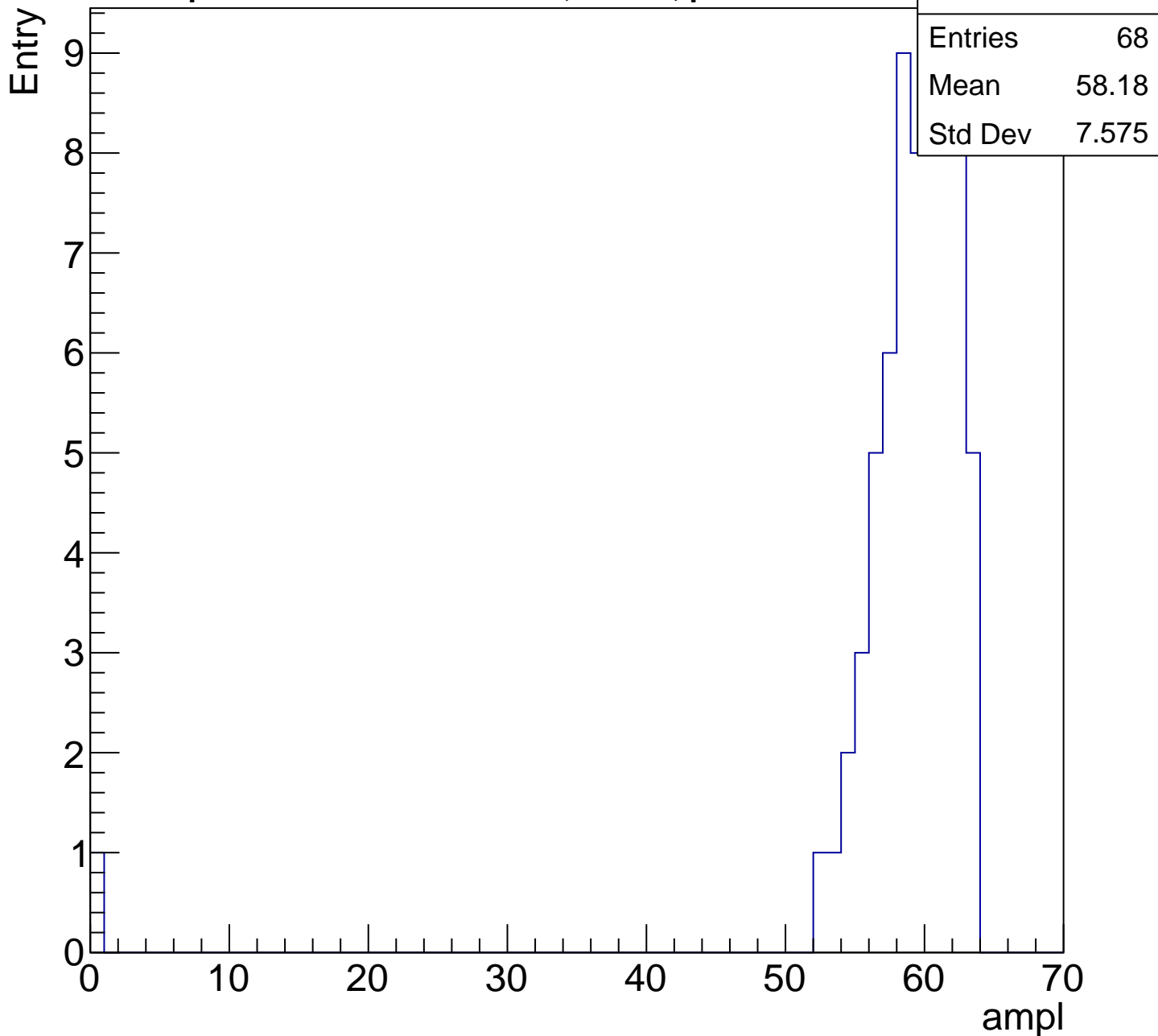
# B1L003S, U6-ch52, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2



# B1L003S, U6-ch52, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

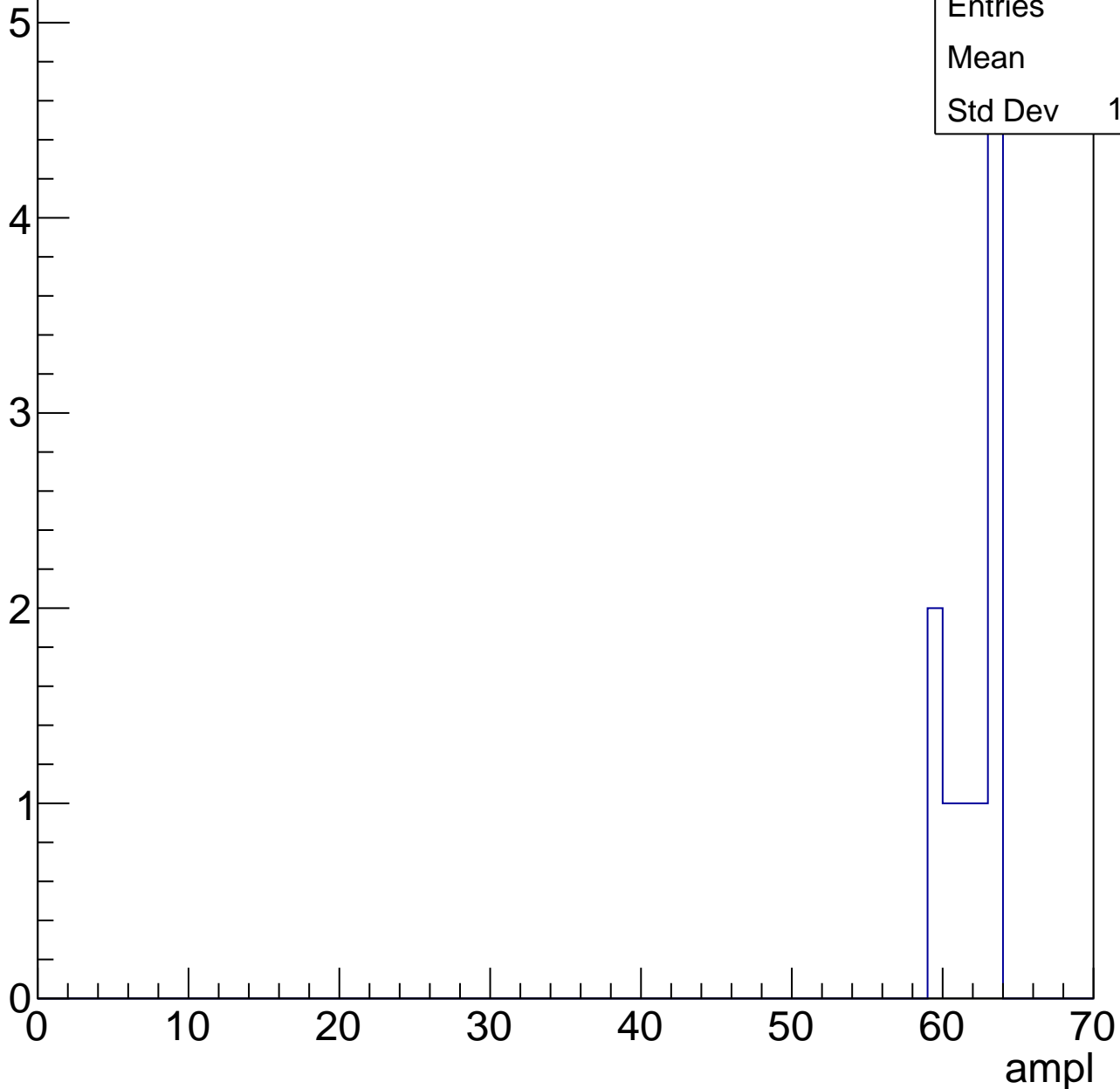


# B1L003S, U6-ch52, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	10
Mean	61.6
Std Dev	1.625





# B1L003S, U6-ch52, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch53, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	88
Mean	31.24
Std Dev	4.034

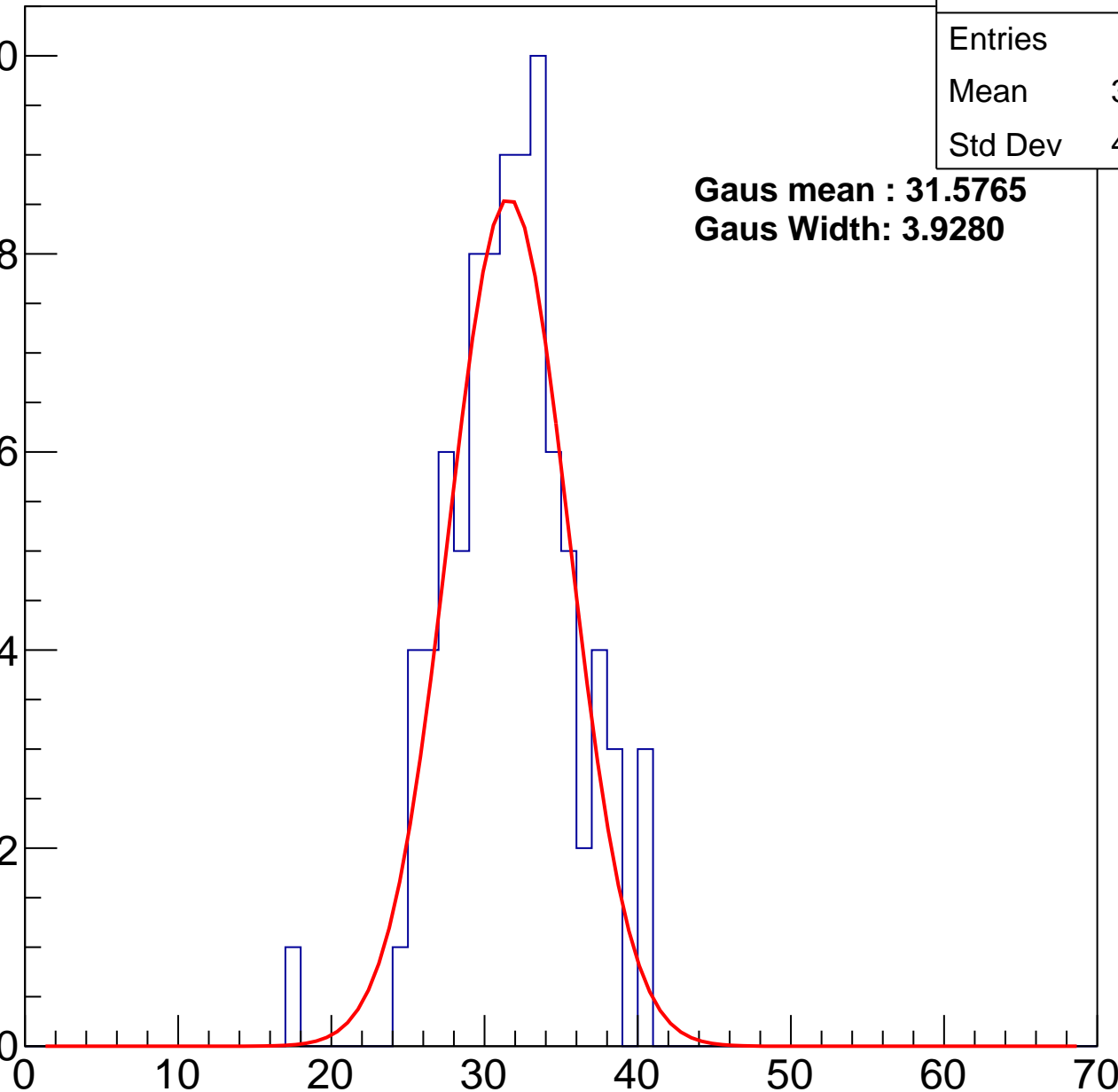
**Gaus mean : 31.5765**

**Gaus Width: 3.9280**

Entry

10  
8  
6  
4  
2  
0

ampl



# B1L003S, U6-ch53, adc1

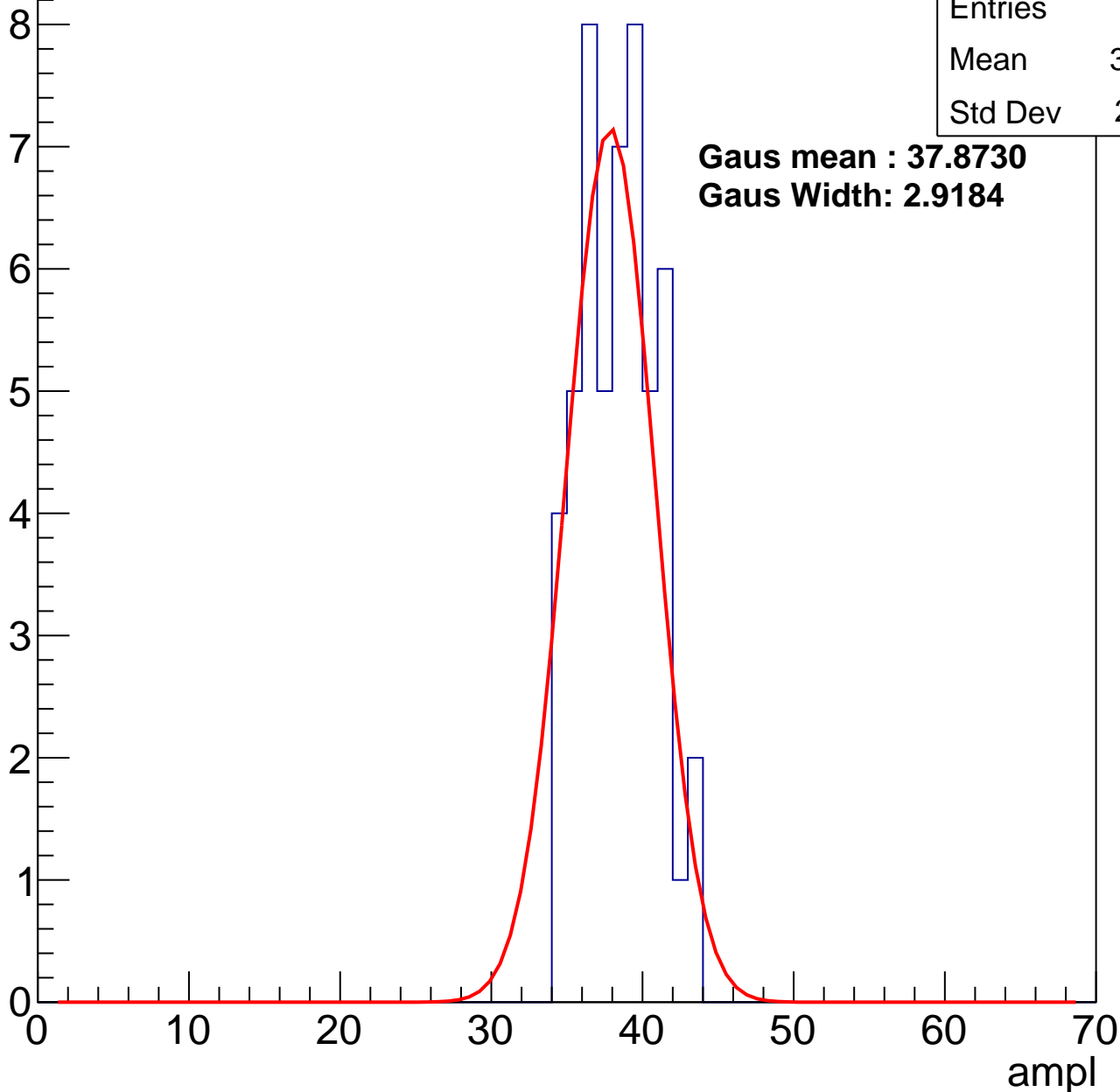
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	51
Mean	37.96
Std Dev	2.401

**Gaus mean : 37.8730**

**Gaus Width: 2.9184**



# B1L003S, U6-ch53, adc2

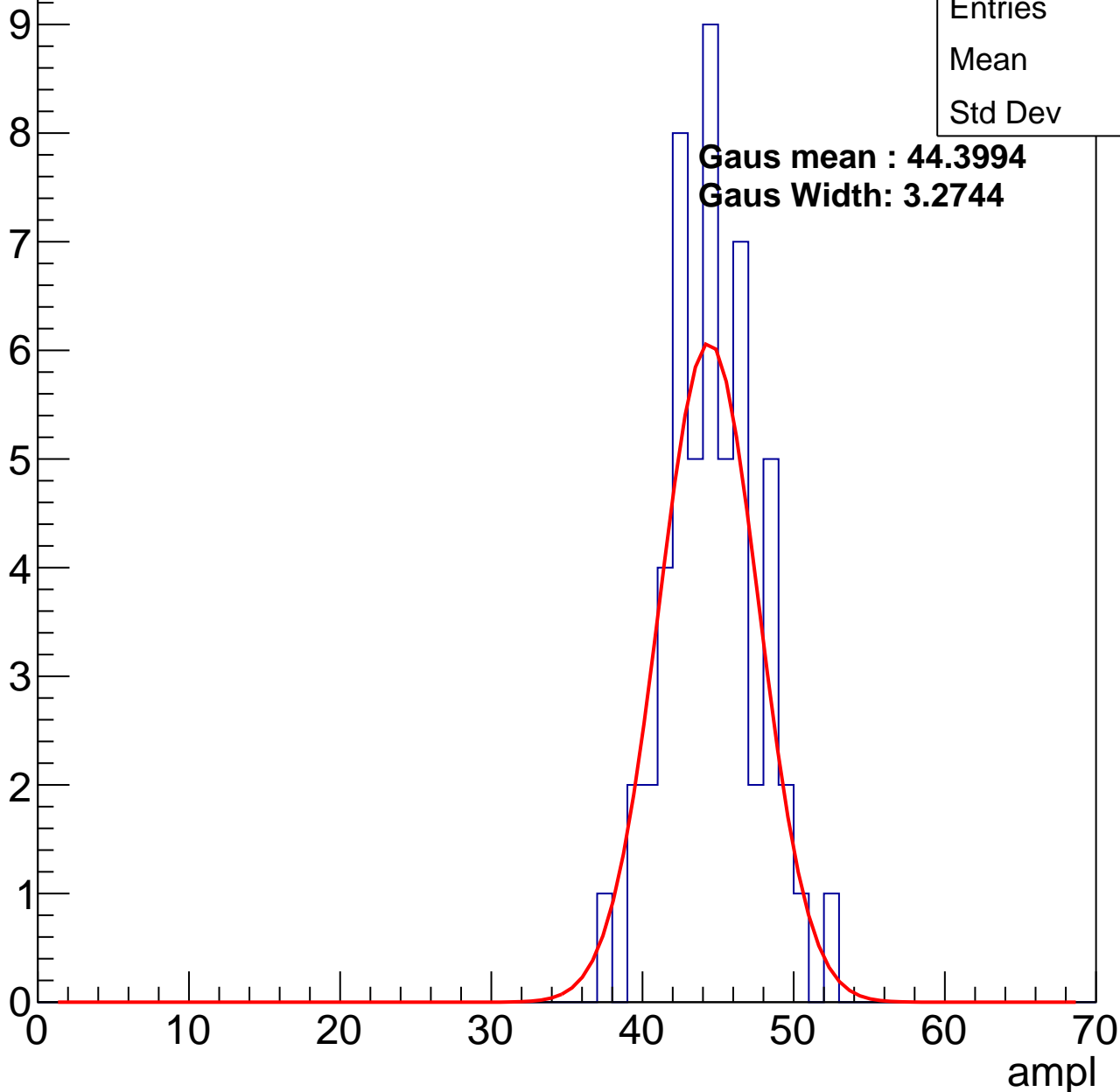
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	54
Mean	44.2
Std Dev	2.99

**Gaus mean : 44.3994**

**Gaus Width: 3.2744**

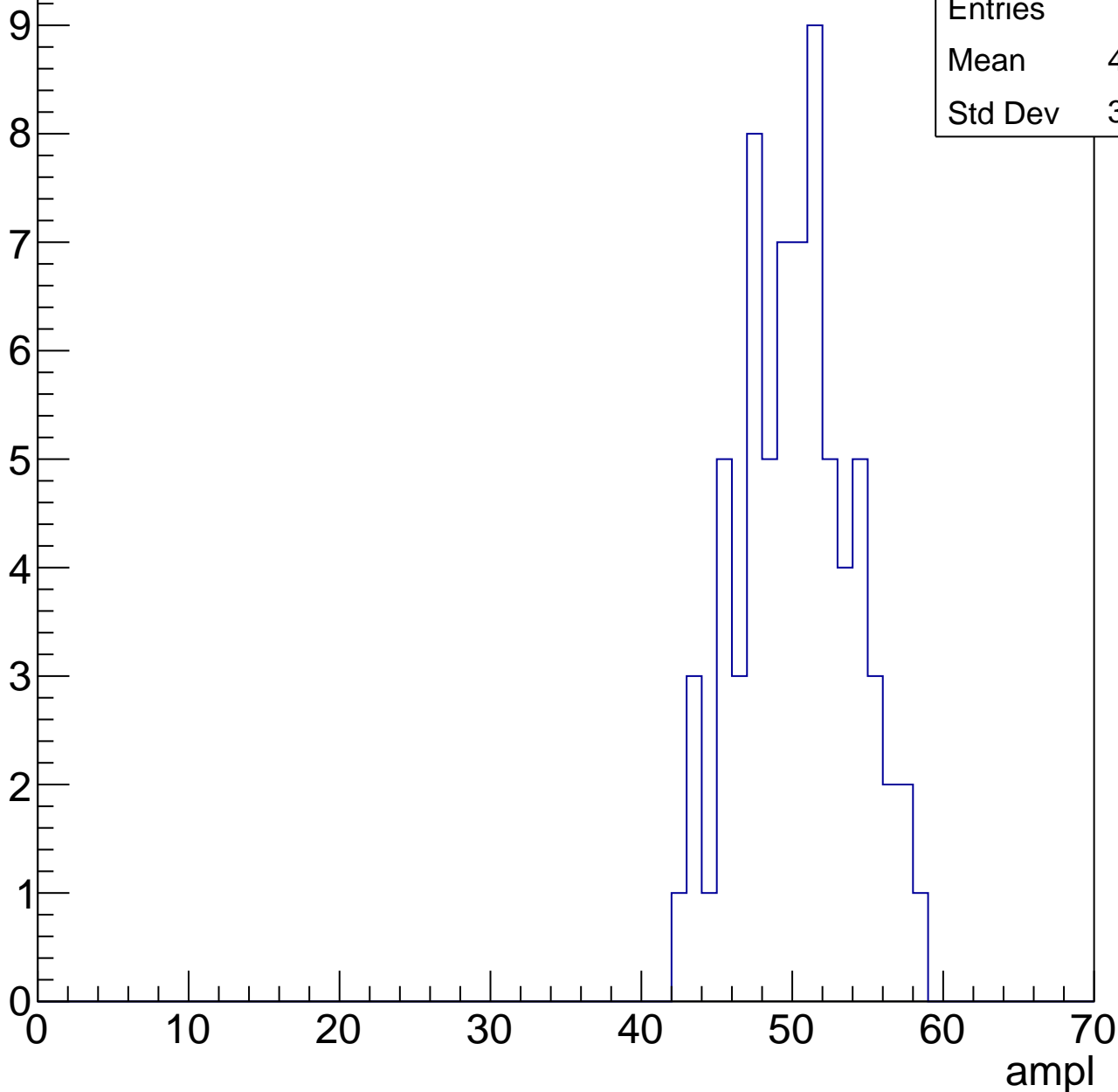


# B1L003S, U6-ch53, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	71
Mean	49.82
Std Dev	3.697

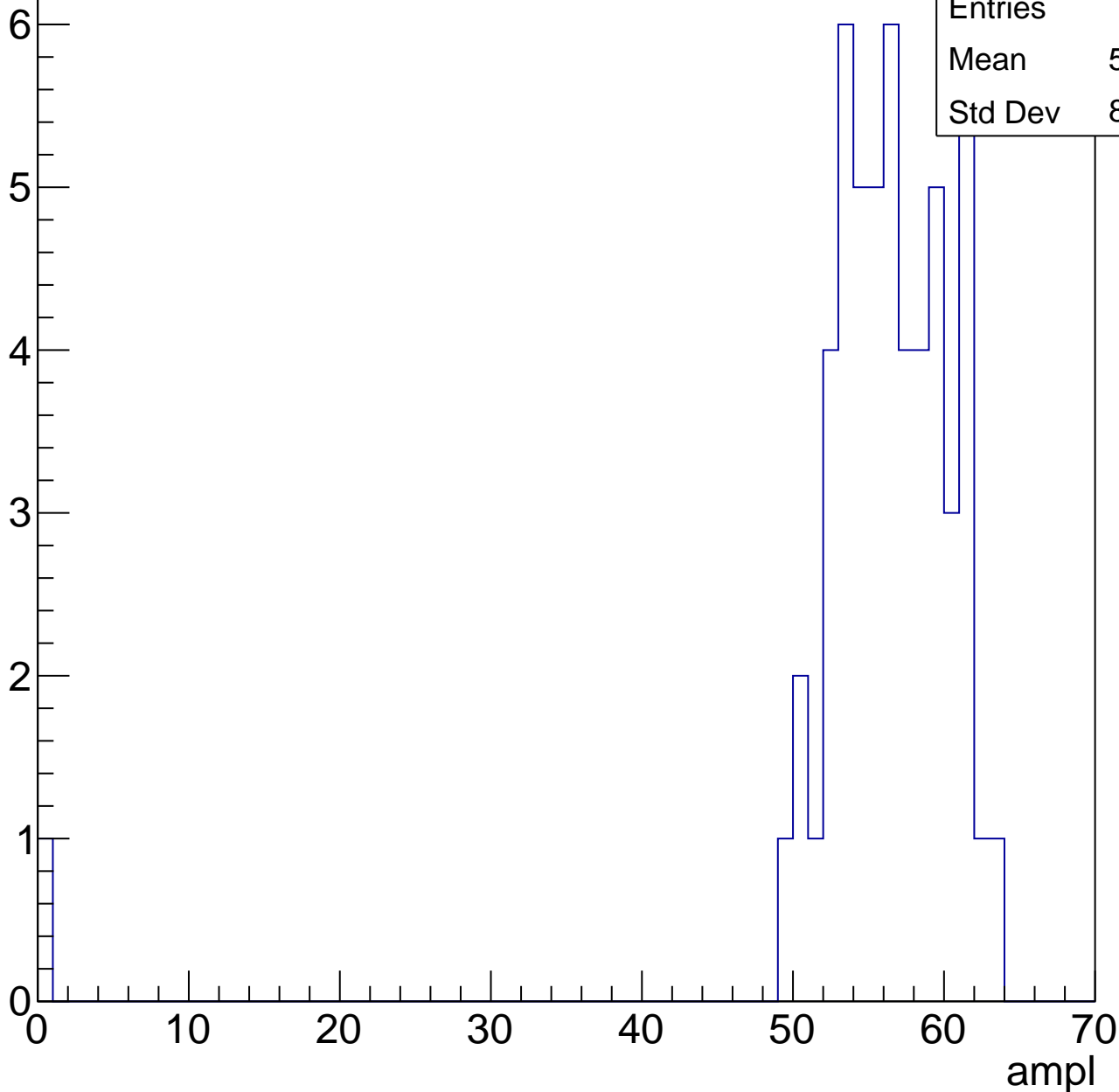


# B1L003S, U6-ch53, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	55.15
Std Dev	8.238



# B1L003S, U6-ch53, adc5

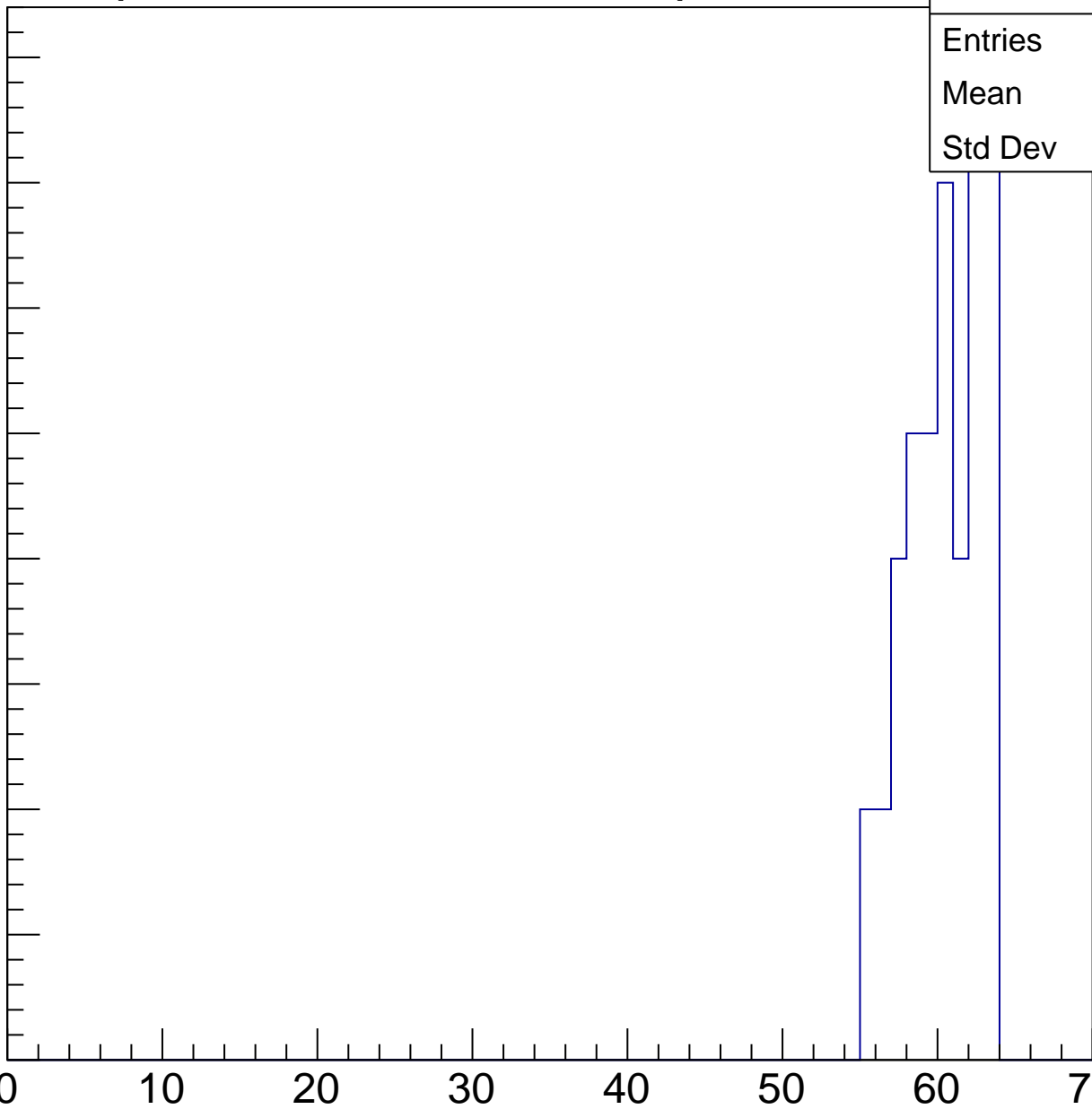
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	45
Mean	59.98
Std Dev	2.362

ampl



# B1L003S, U6-ch53, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch53, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U6-ch54, adc0

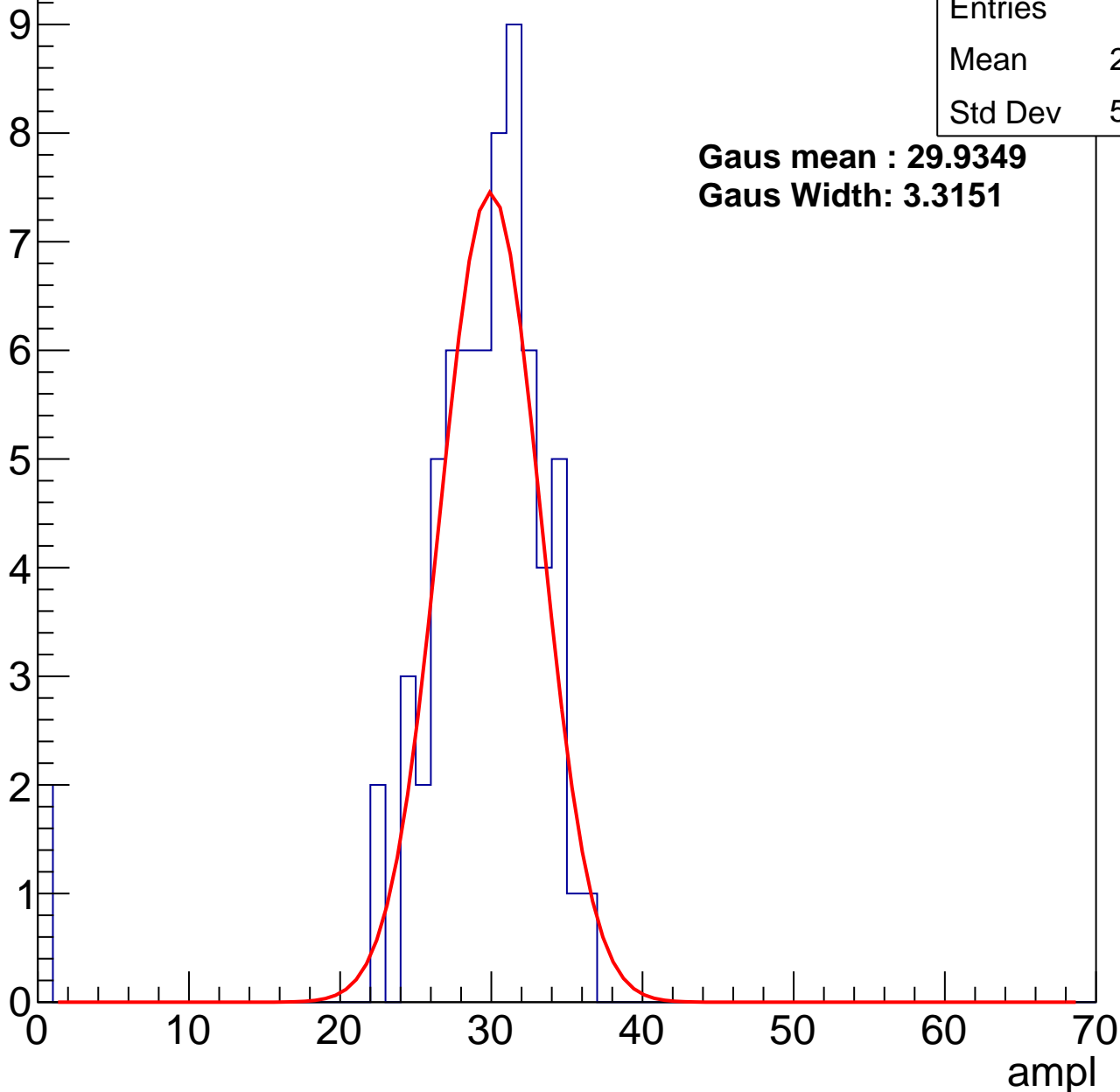
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	28.55
Std Dev	5.929

**Gaus mean : 29.9349**

**Gaus Width: 3.3151**



# B1L003S, U6-ch54, adc1

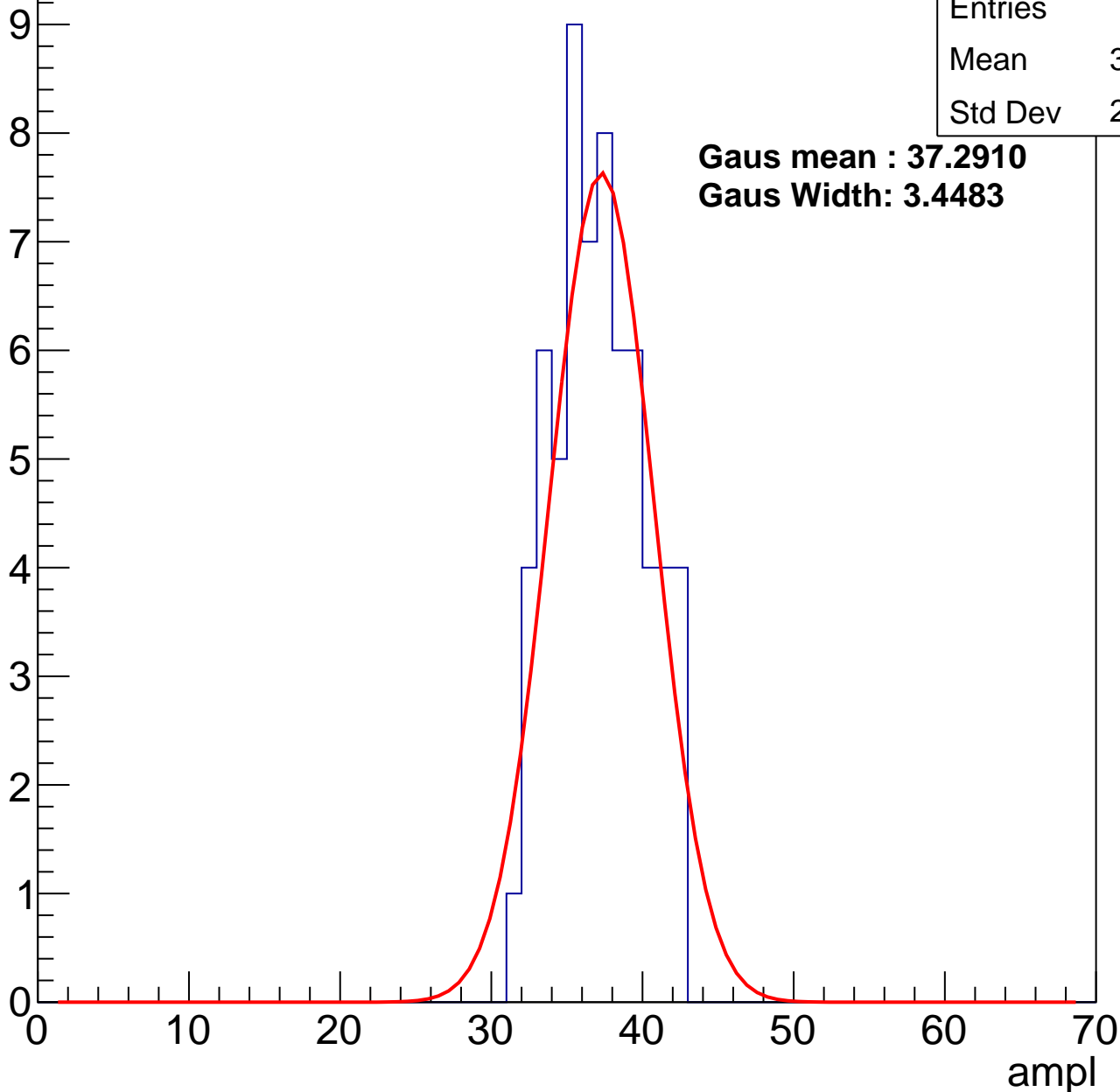
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	36.62
Std Dev	2.907

**Gaus mean : 37.2910**

**Gaus Width: 3.4483**



# B1L003S, U6-ch54, adc2

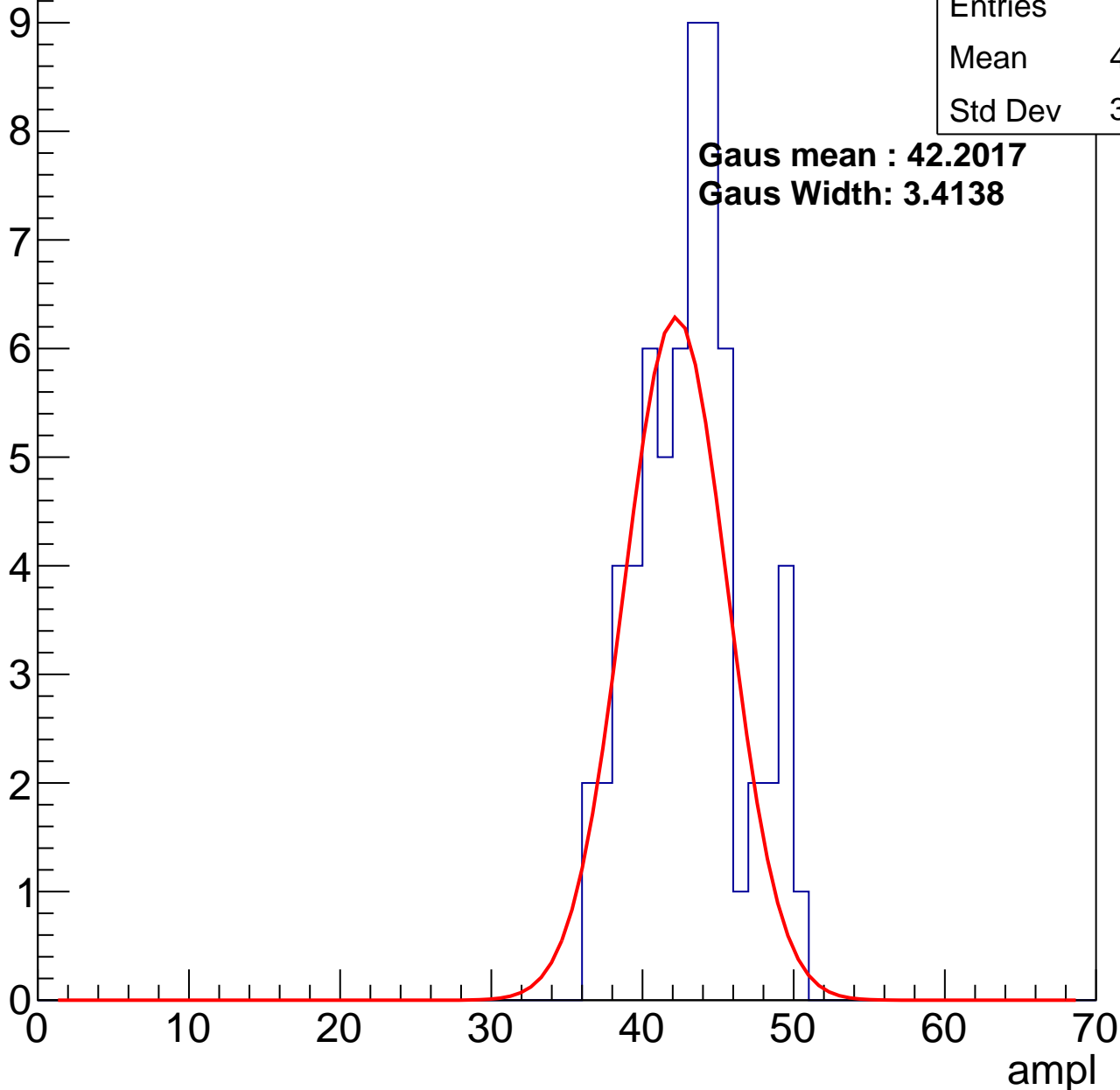
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	42.63
Std Dev	3.387

**Gaus mean : 42.2017**

**Gaus Width: 3.4138**

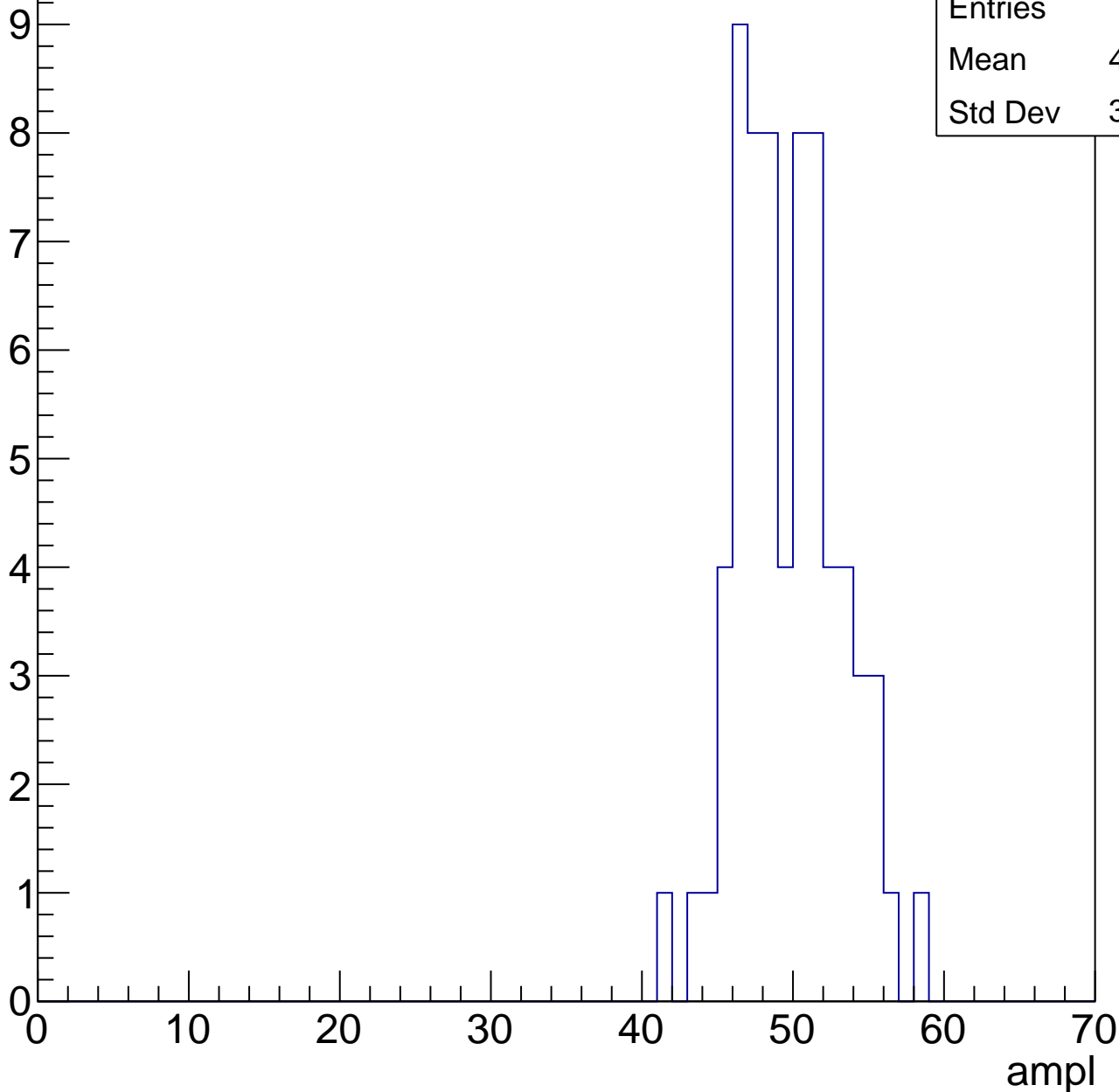


# B1L003S, U6-ch54, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	49.22
Std Dev	3.342

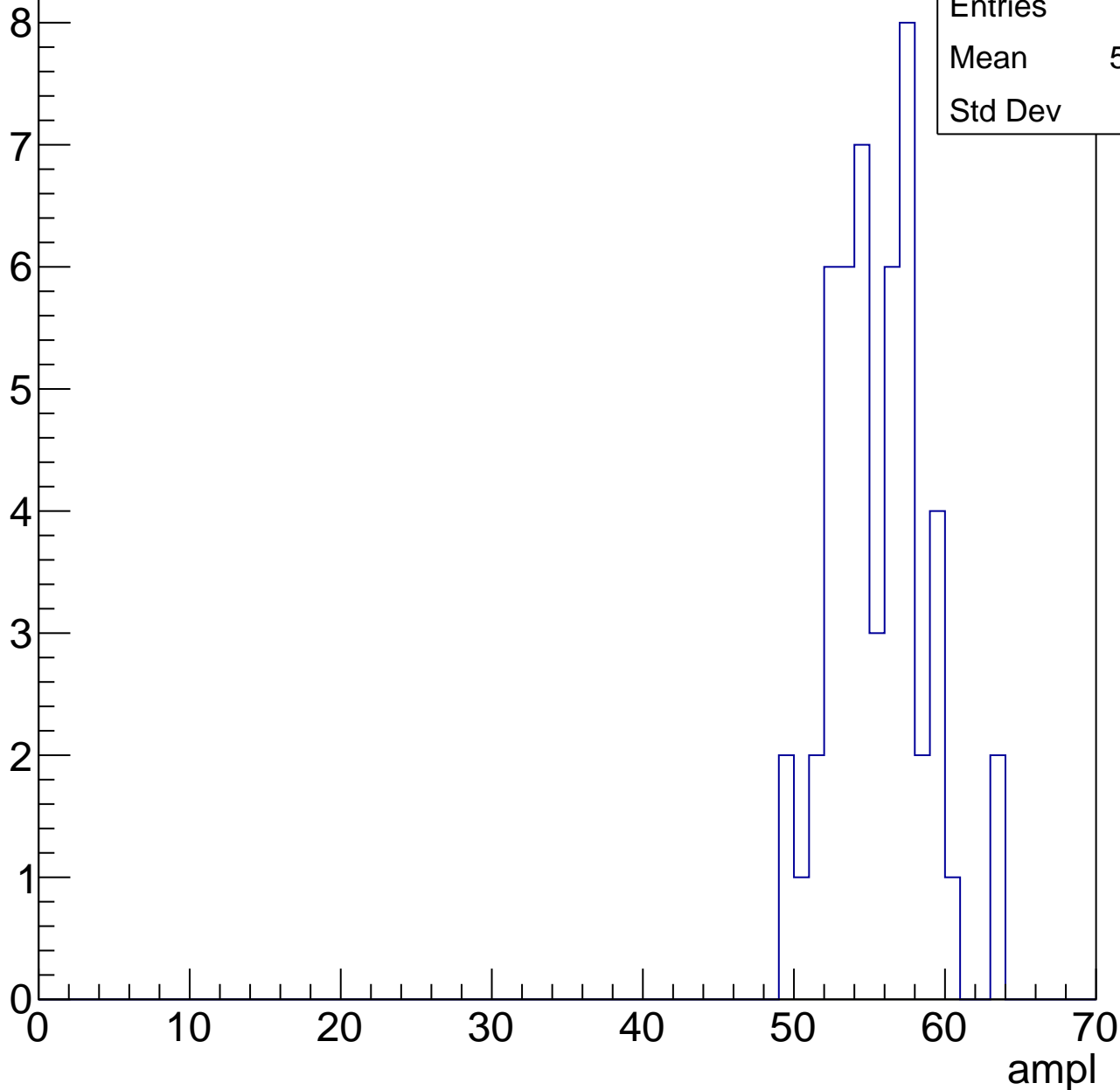


# B1L003S, U6-ch54, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	50
Mean	55.06
Std Dev	3.12

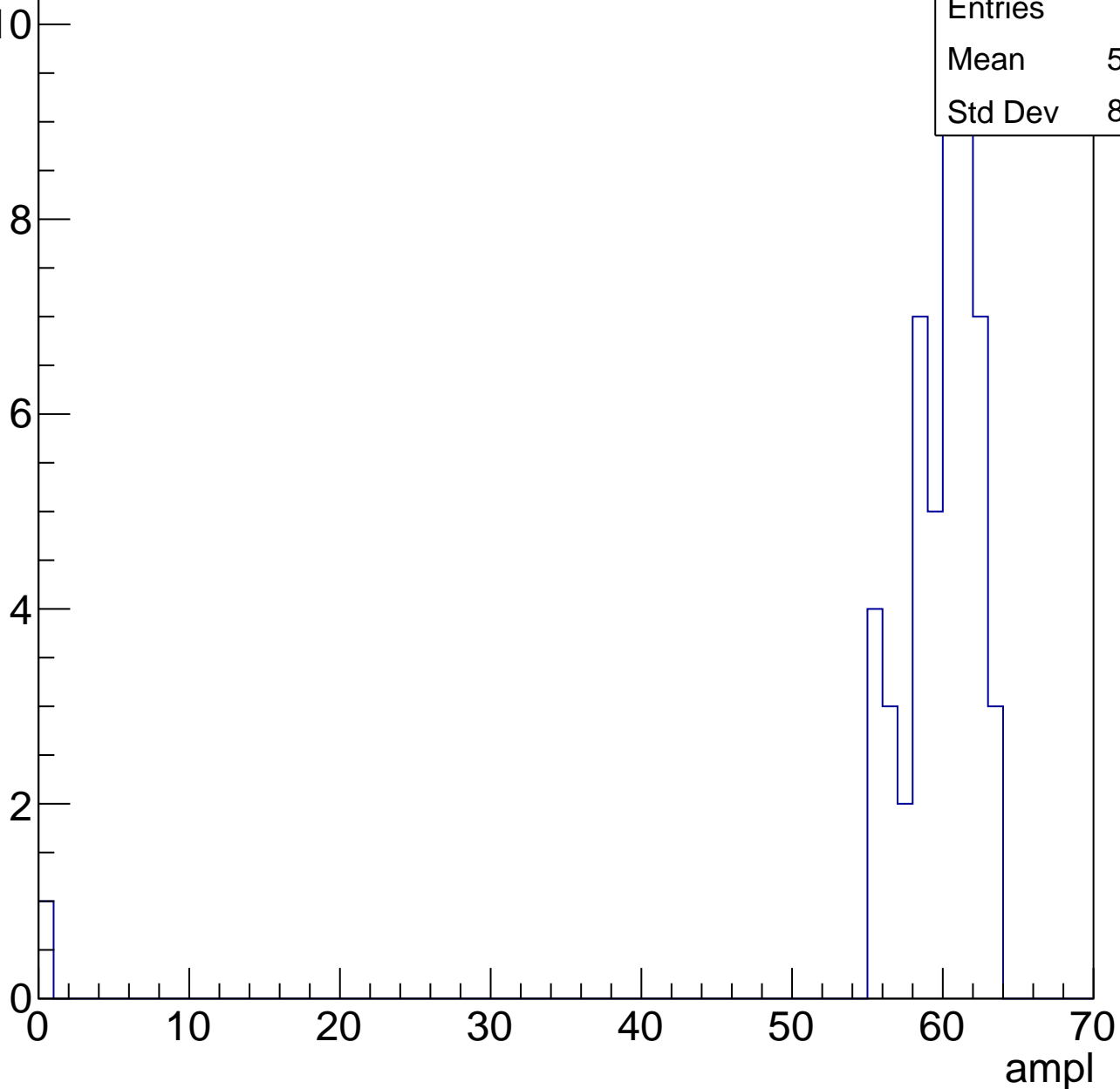


# B1L003S, U6-ch54, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

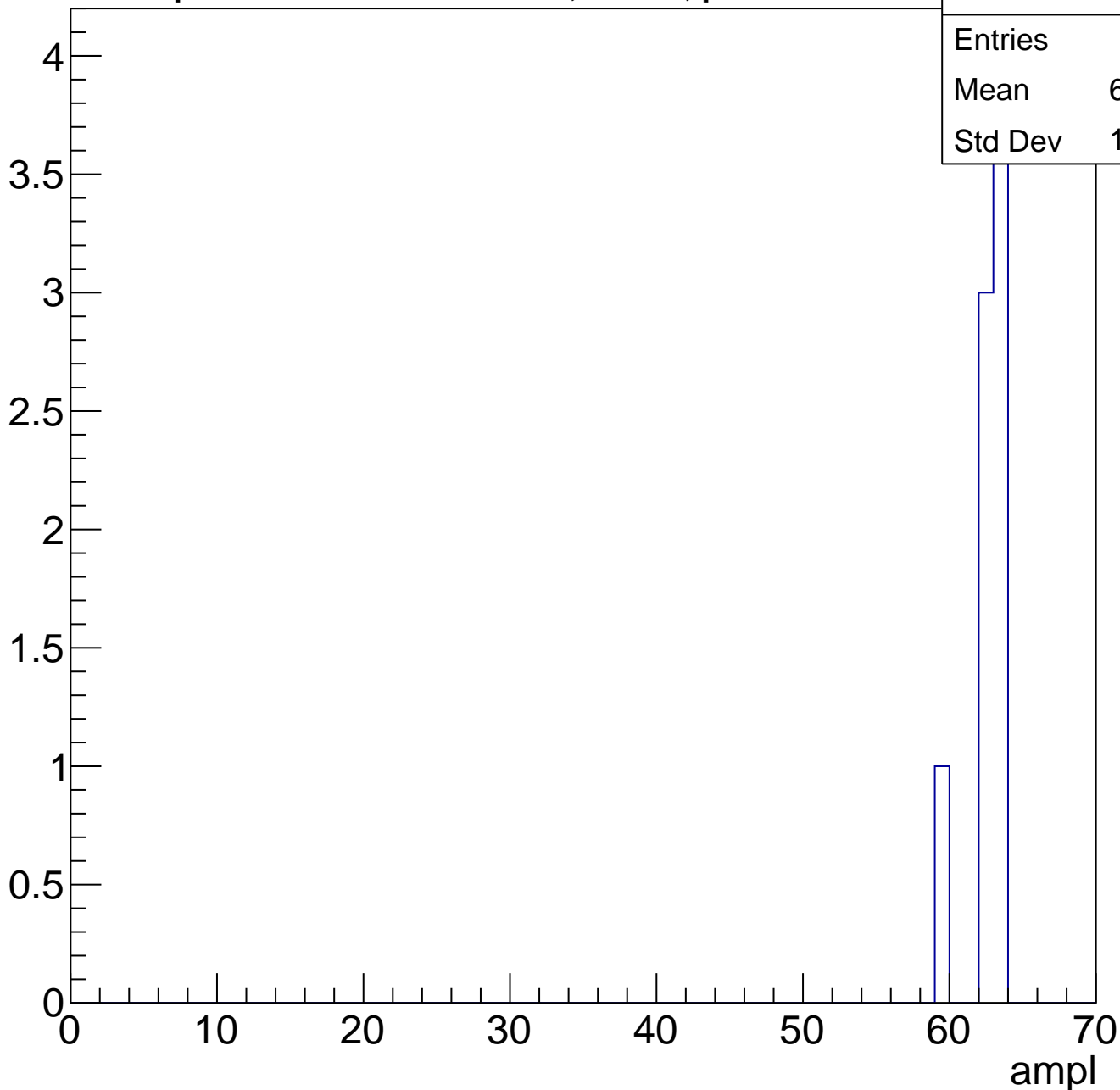
Entries	51
Mean	58.35
Std Dev	8.547



# B1L003S, U6-ch54, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

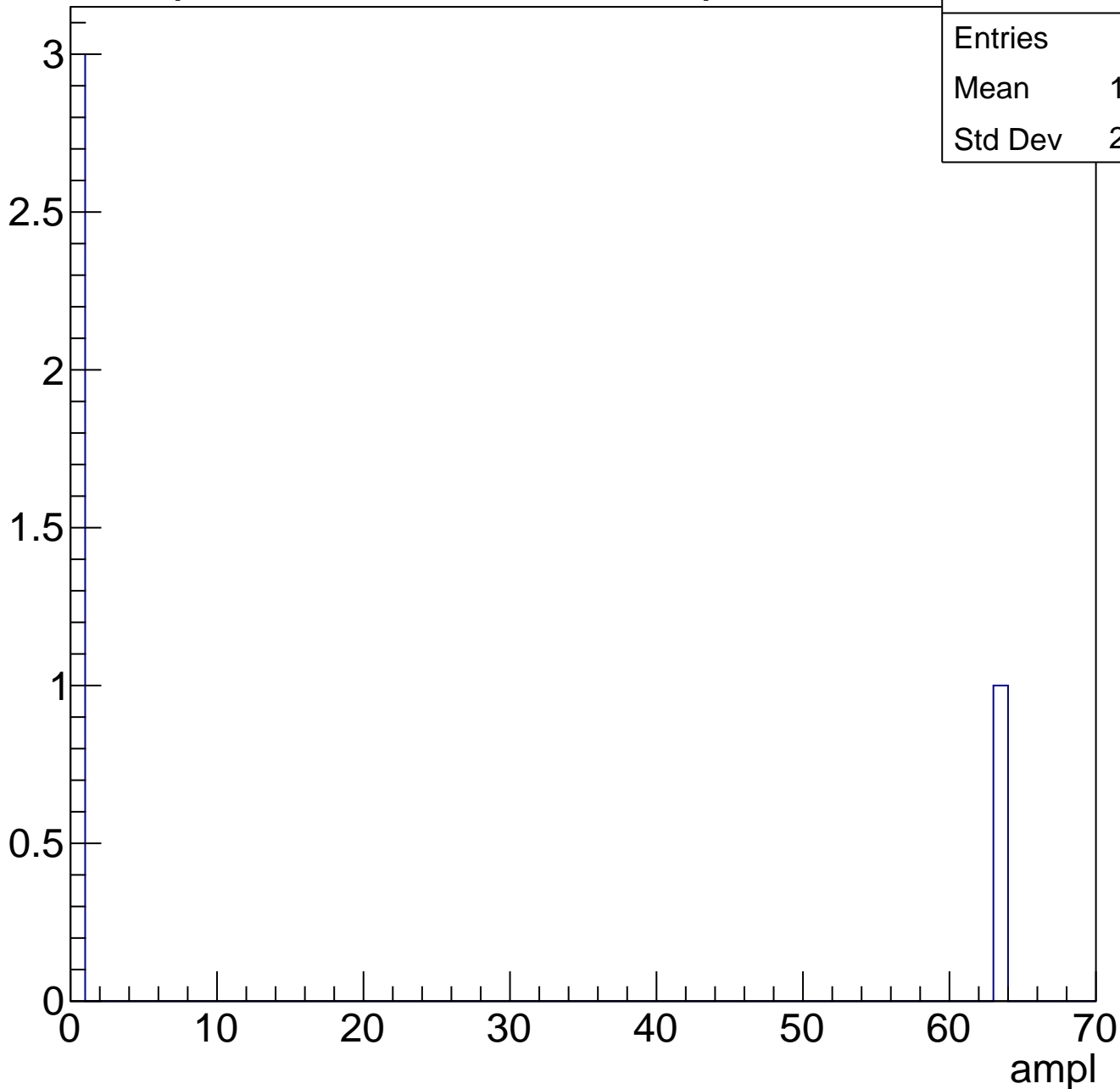




# B1L003S, U6-ch54, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch55, adc0

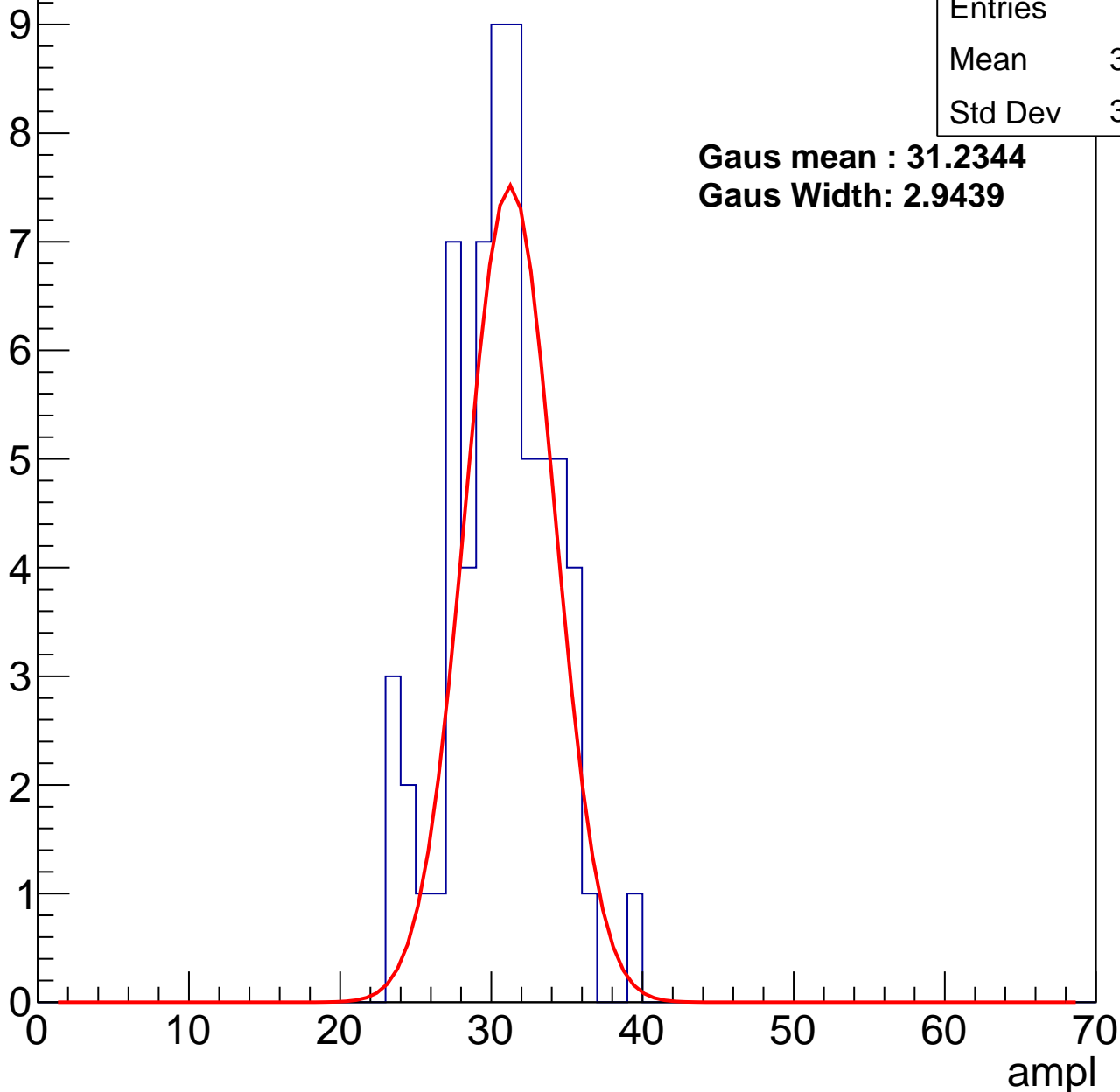
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	30.17
Std Dev	3.343

**Gaus mean : 31.2344**

**Gaus Width: 2.9439**



# B1L003S, U6-ch55, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	74
Mean	37.11
Std Dev	3.391

**Gaus mean : 37.4423**

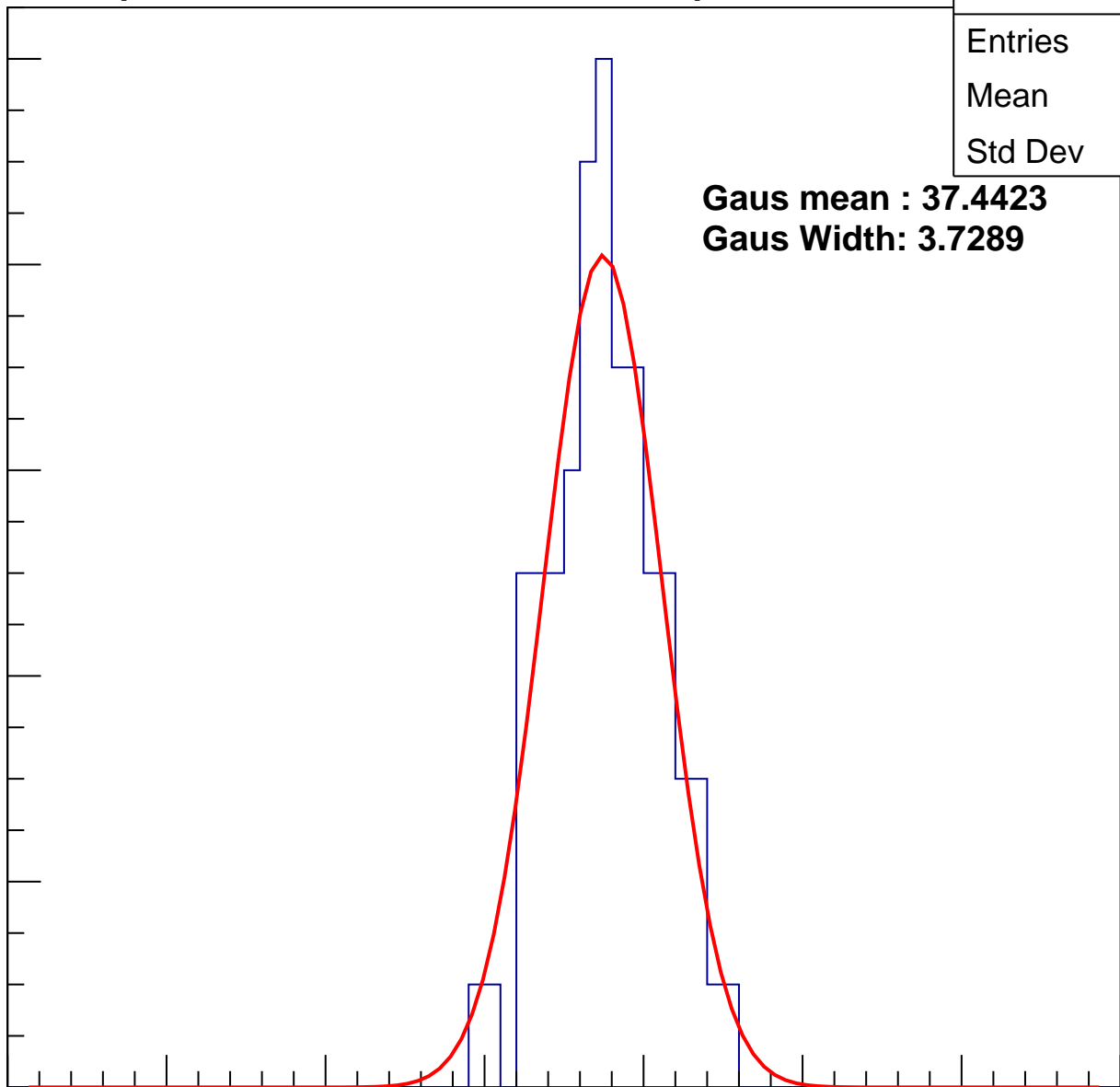
**Gaus Width: 3.7289**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

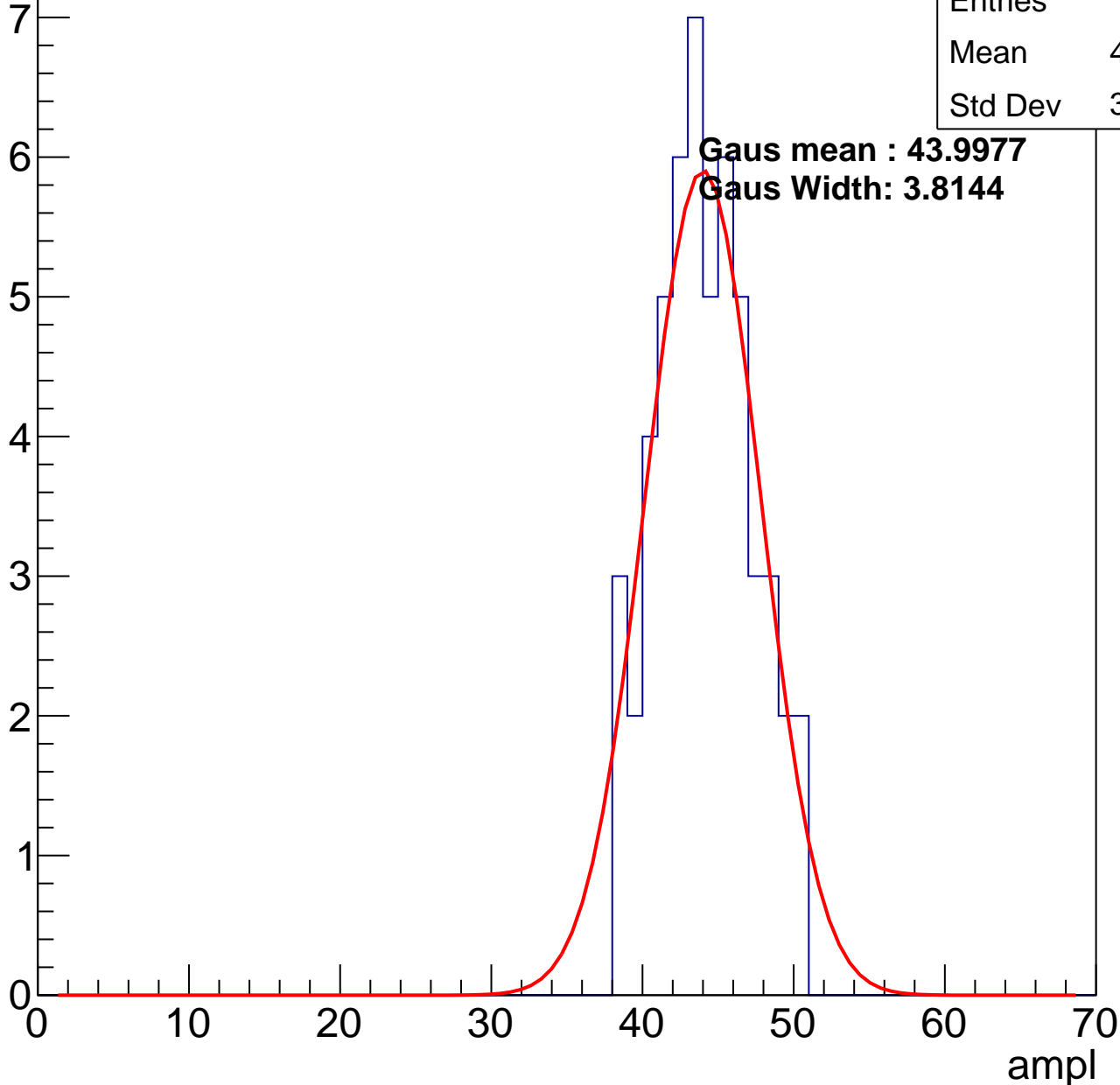


# B1L003S, U6-ch55, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

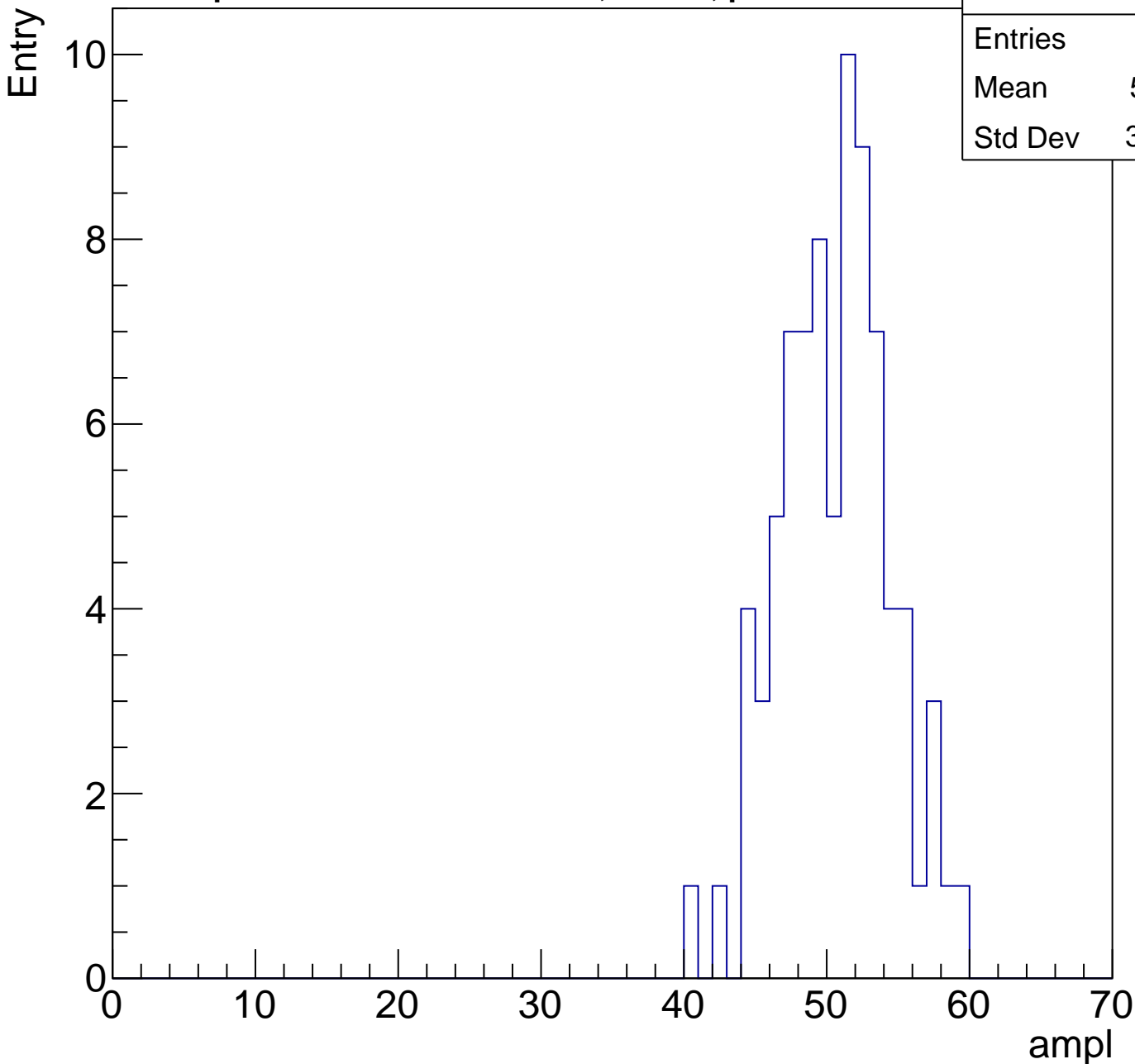
Entries	53
Mean	43.64
Std Dev	3.115



# B1L003S, U6-ch55, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

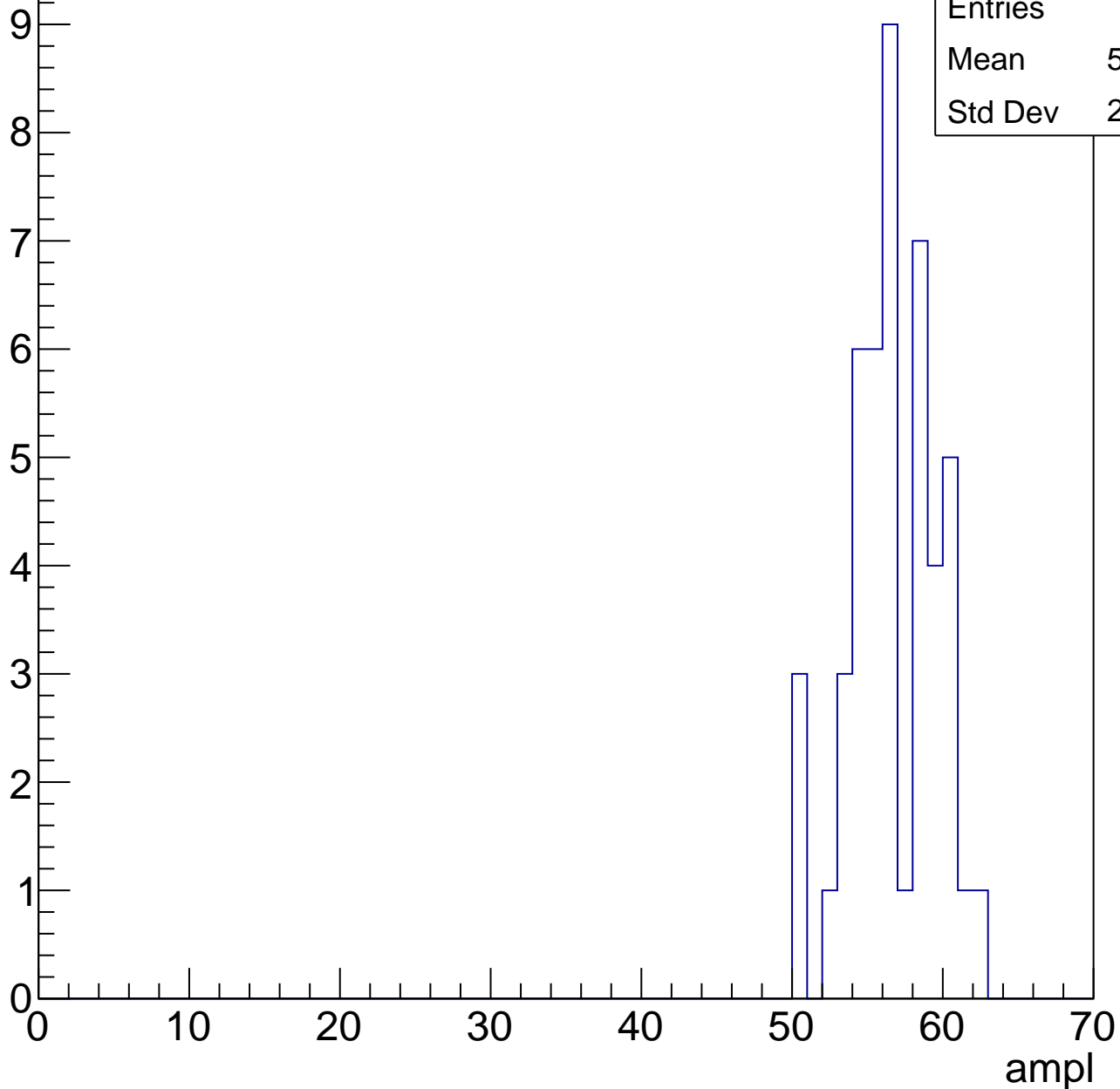
Entries	81
Mean	50.11
Std Dev	3.788



# B1L003S, U6-ch55, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

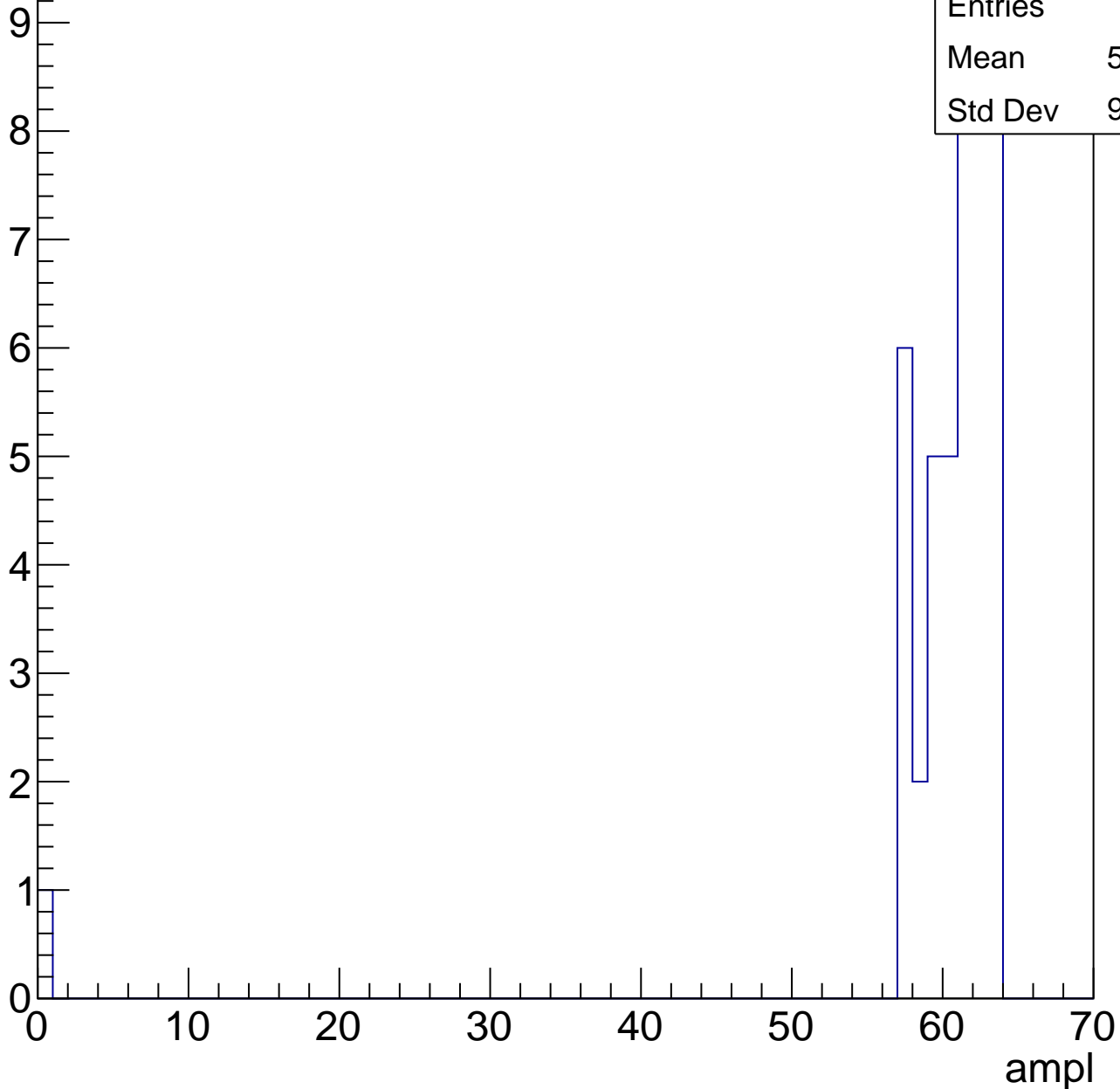
Entry



# B1L003S, U6-ch55, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch55, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch55, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L003S, U6-ch56, adc0

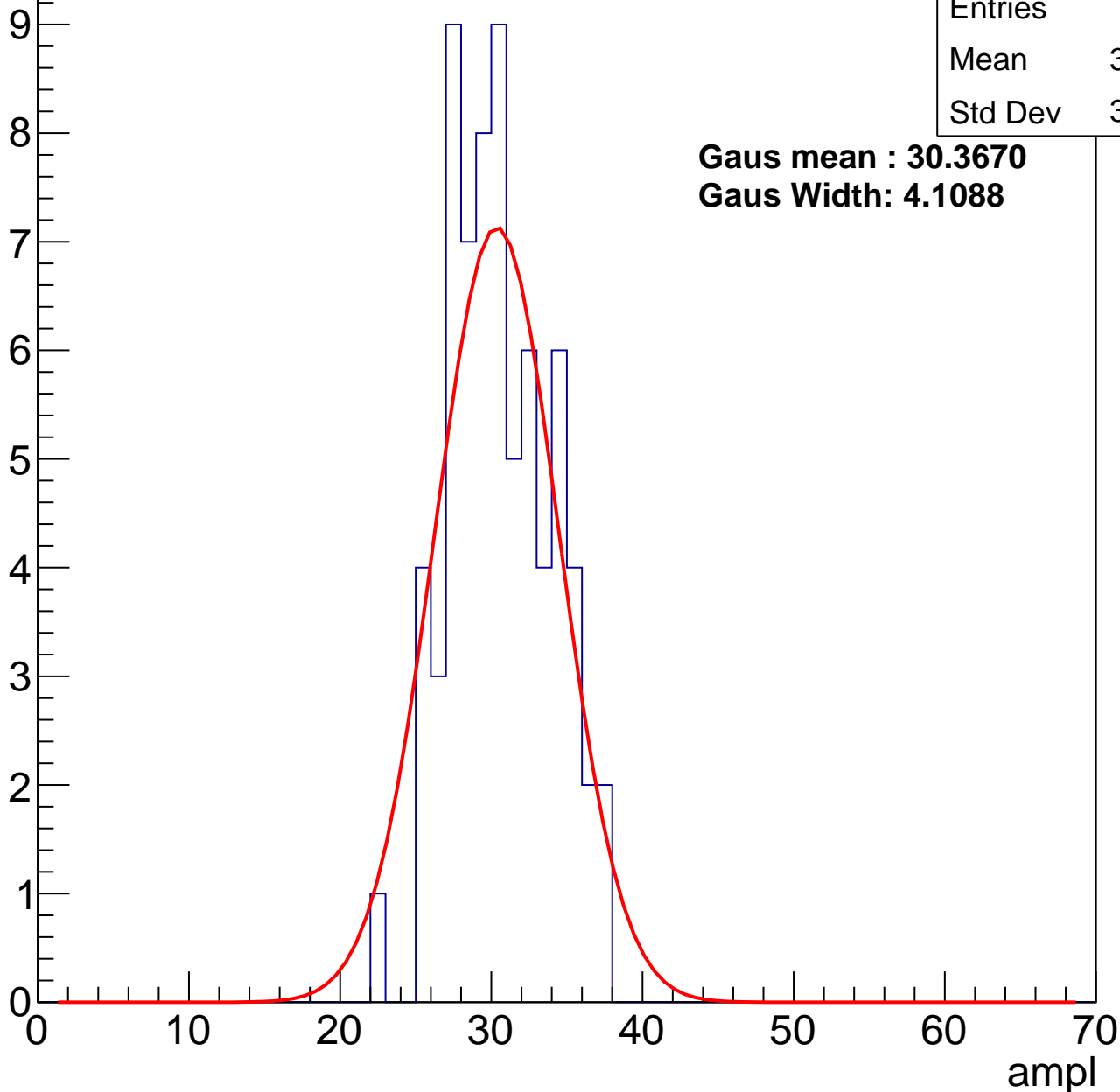
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	30.14
Std Dev	3.292

**Gaus mean : 30.3670**

**Gaus Width: 4.1088**



# B1L003S, U6-ch56, adc1

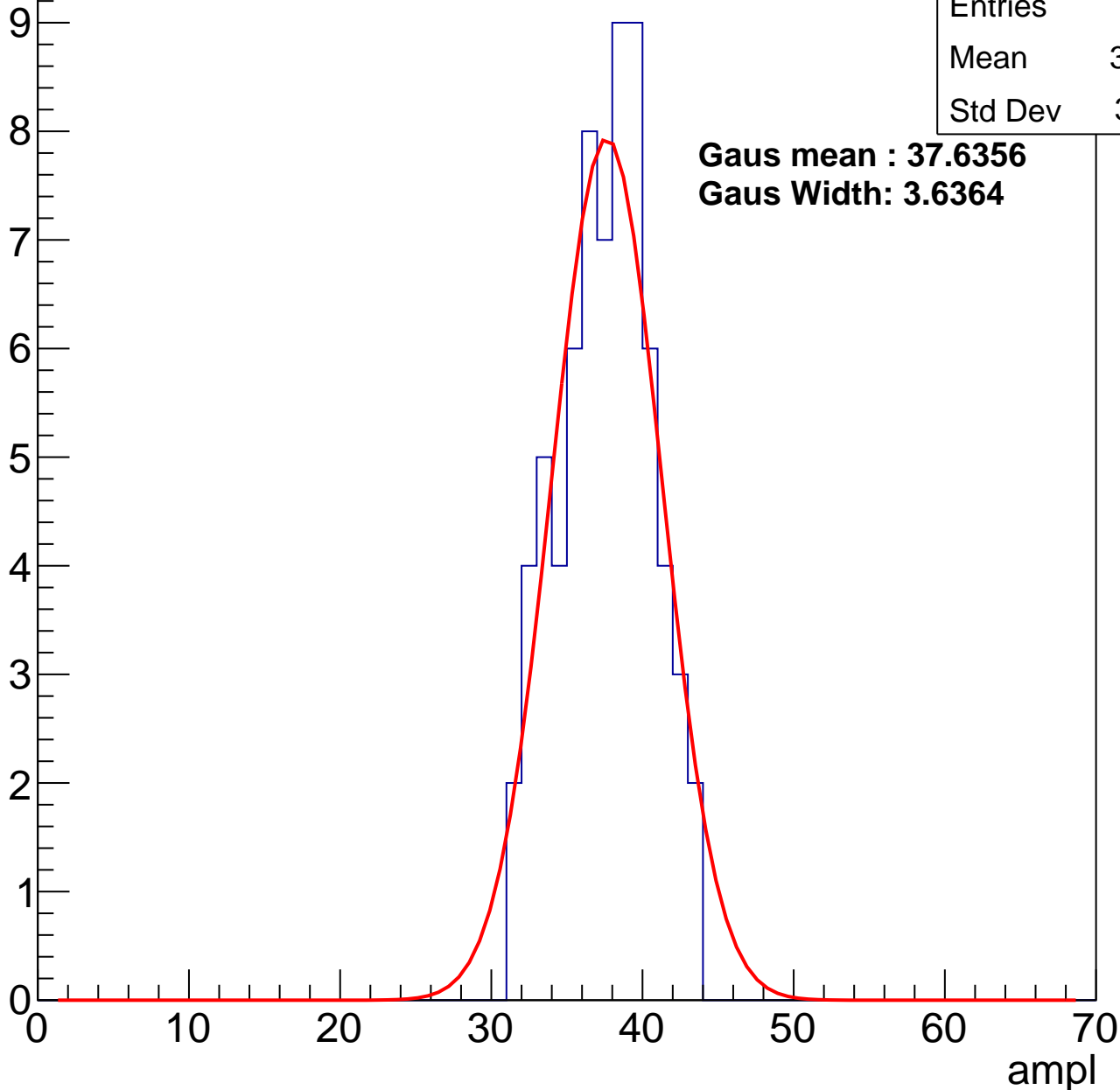
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	37.06
Std Dev	3.021

**Gaus mean : 37.6356**

**Gaus Width: 3.6364**



# B1L003S, U6-ch56, adc2

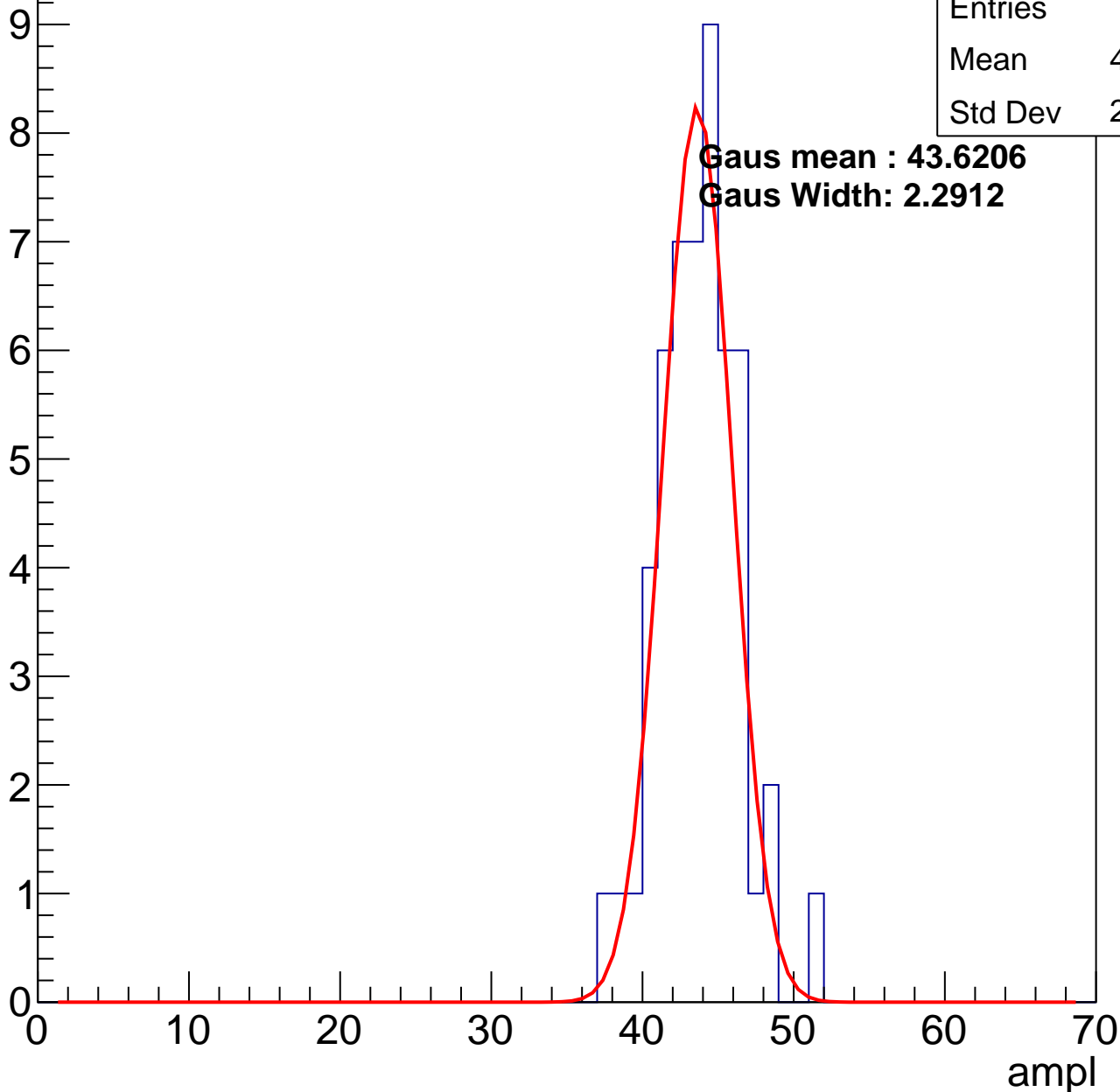
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	52
Mean	43.29
Std Dev	2.619

**Gaus mean : 43.6206**

**Gaus Width: 2.2912**



# B1L003S, U6-ch56, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

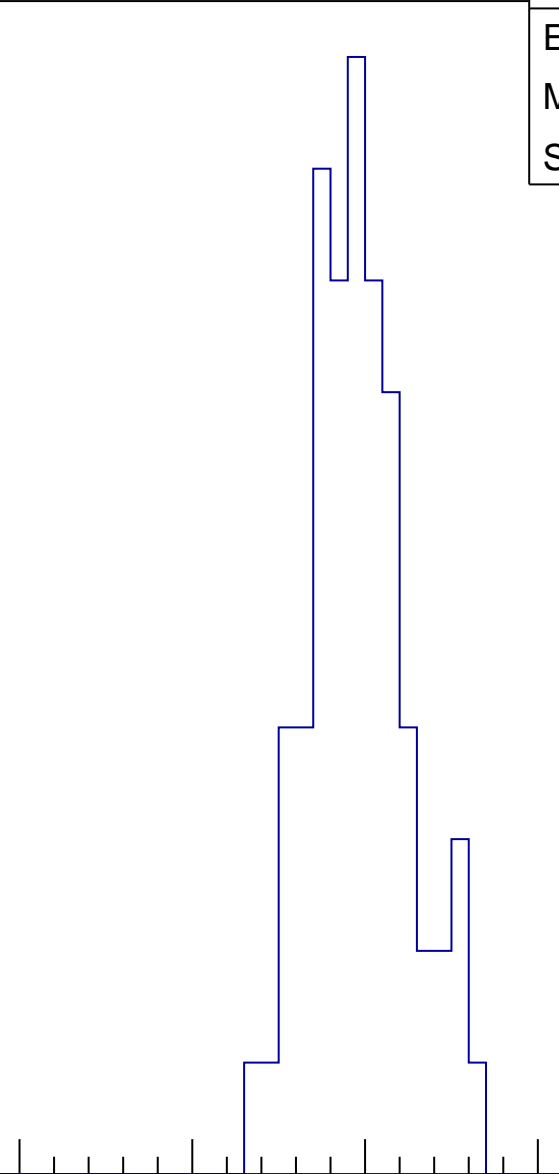
Entries	64
Mean	49.19
Std Dev	2.833

Entry

10  
8  
6  
4  
2  
0

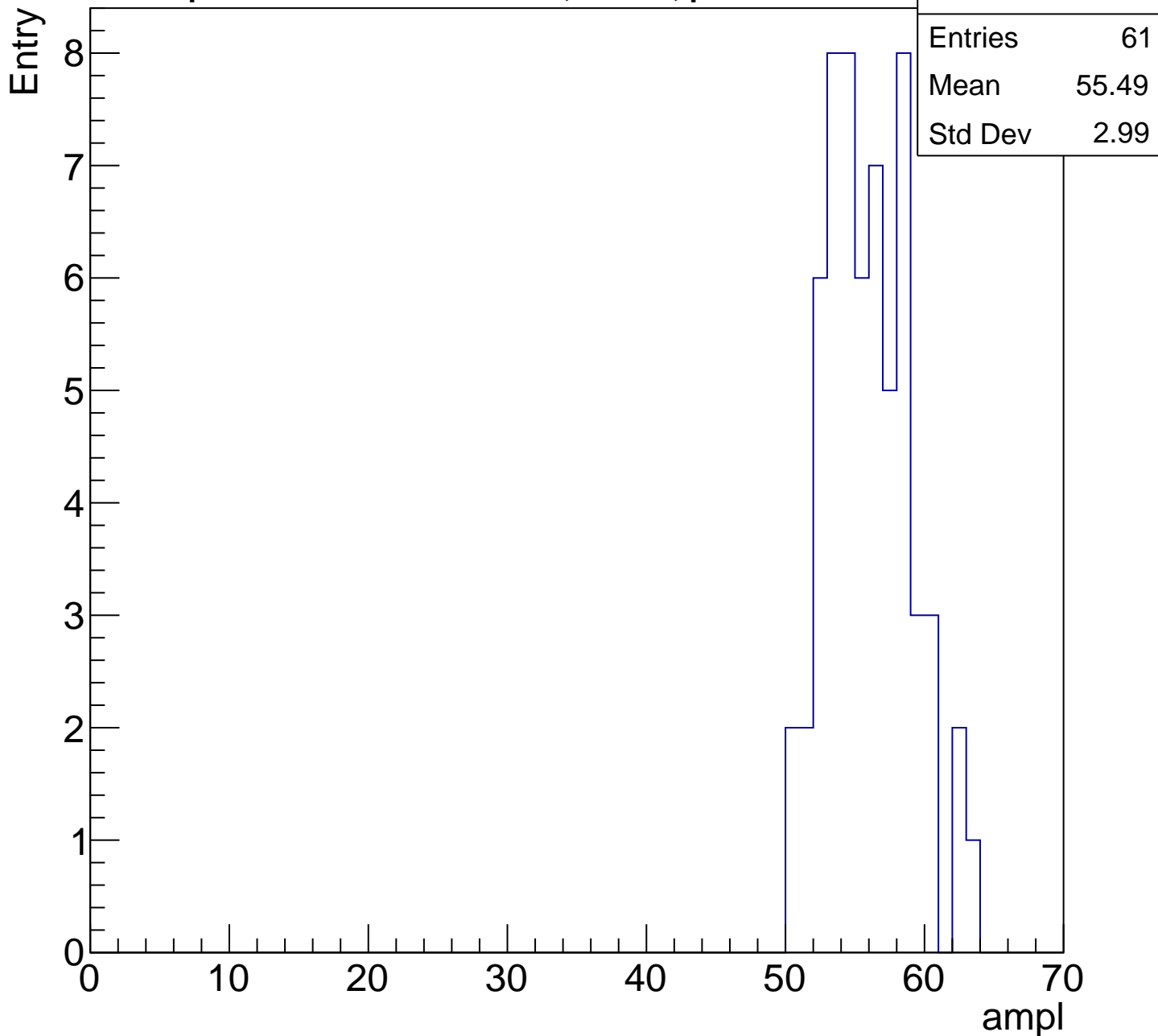
0 10 20 30 40 50 60 70

ampl



# B1L003S, U6-ch56, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

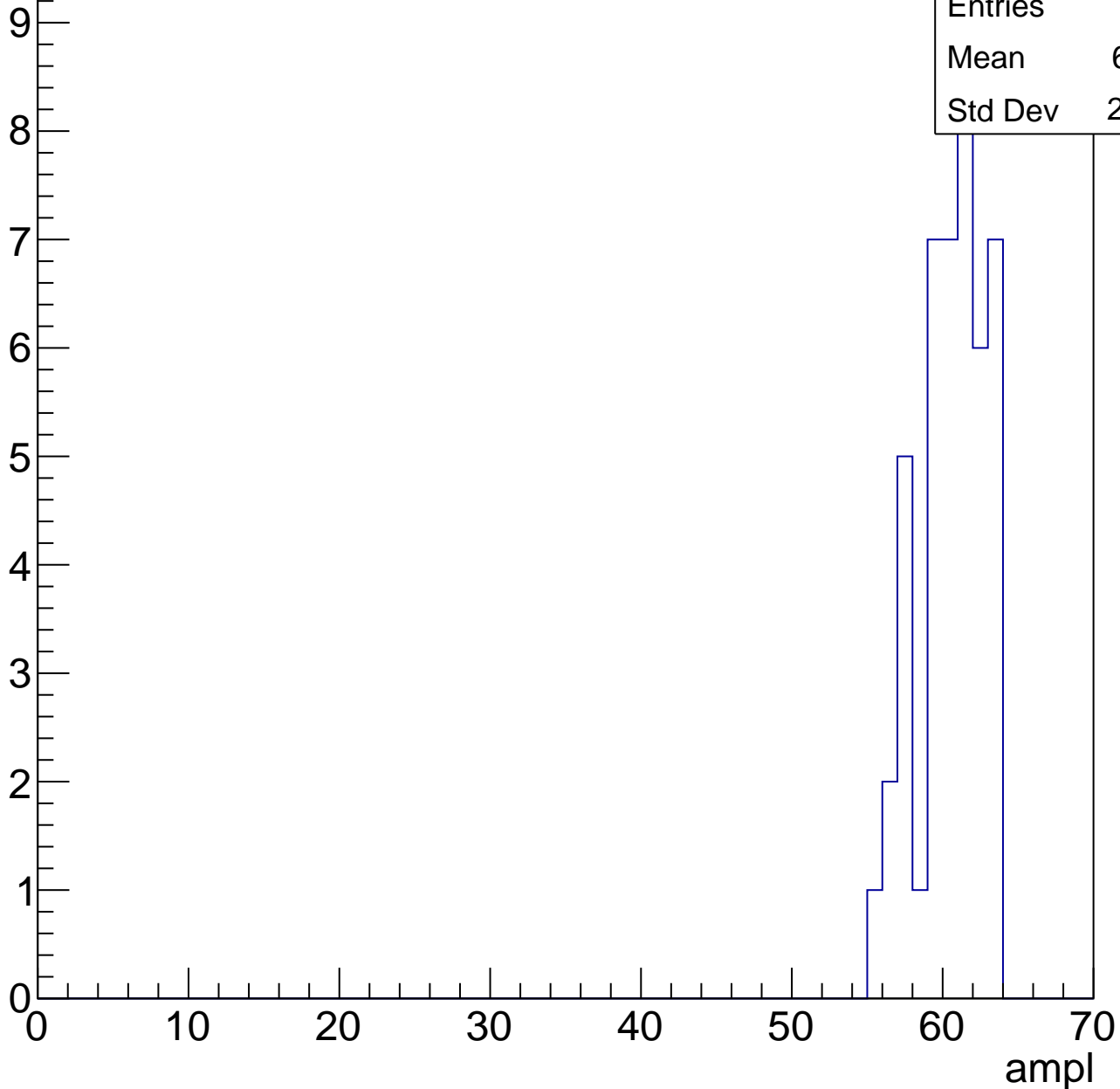


# B1L003S, U6-ch56, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

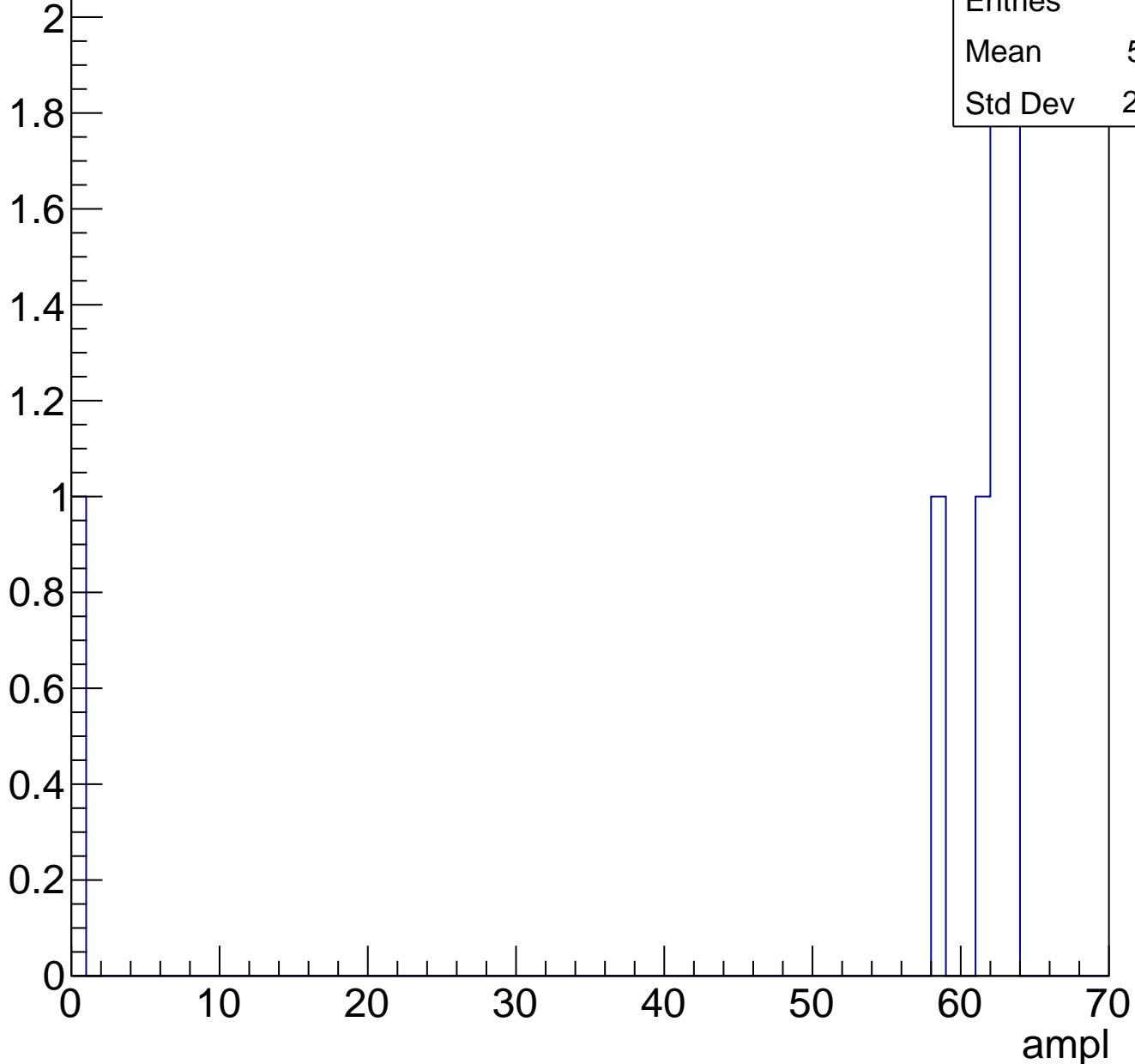
Entries	45
Mean	60.11
Std Dev	2.152



# B1L003S, U6-ch56, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch56, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch57, adc0

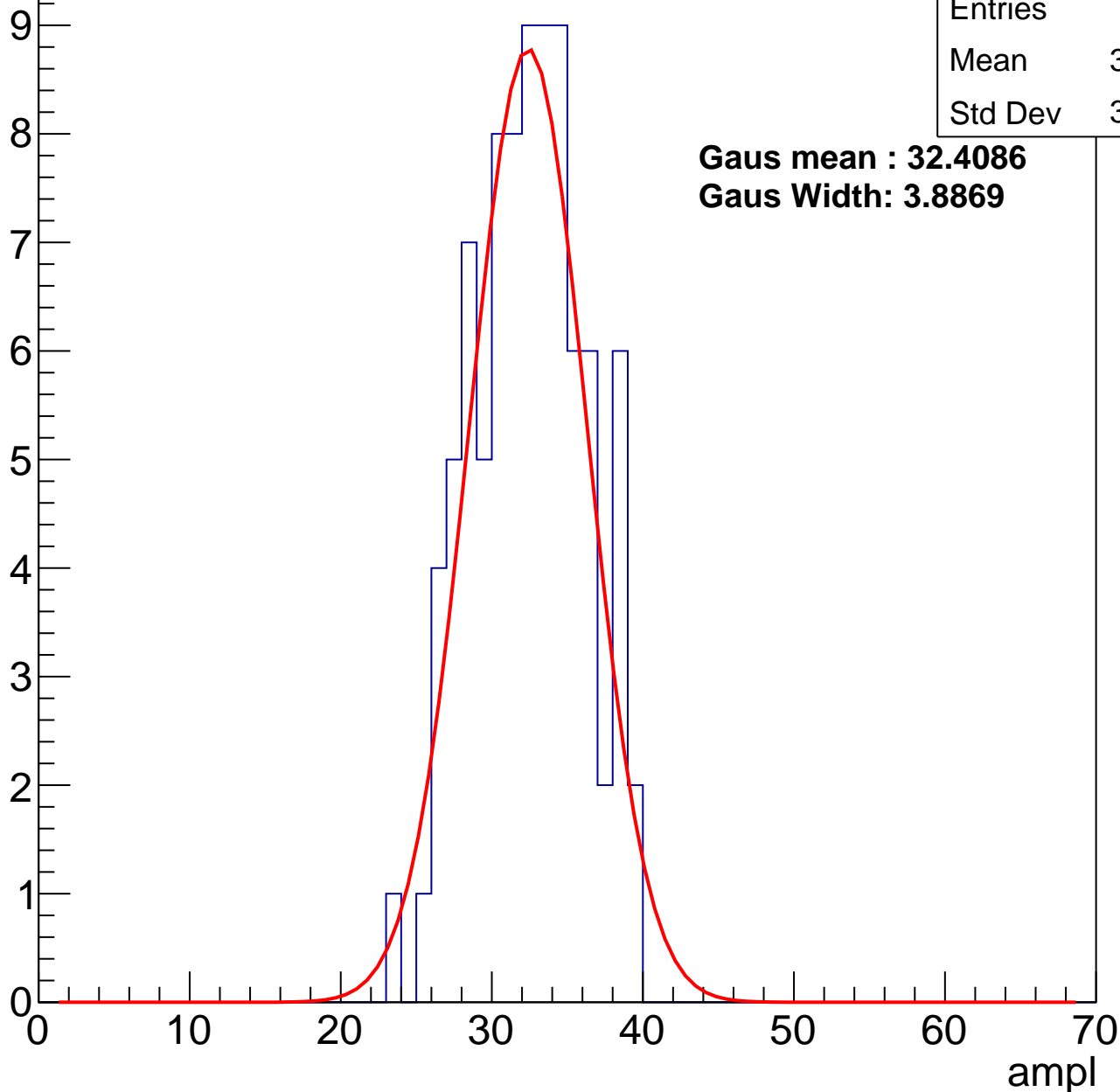
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	88
Mean	31.97
Std Dev	3.623

**Gaus mean : 32.4086**

**Gaus Width: 3.8869**



# B1L003S, U6-ch57, adc1

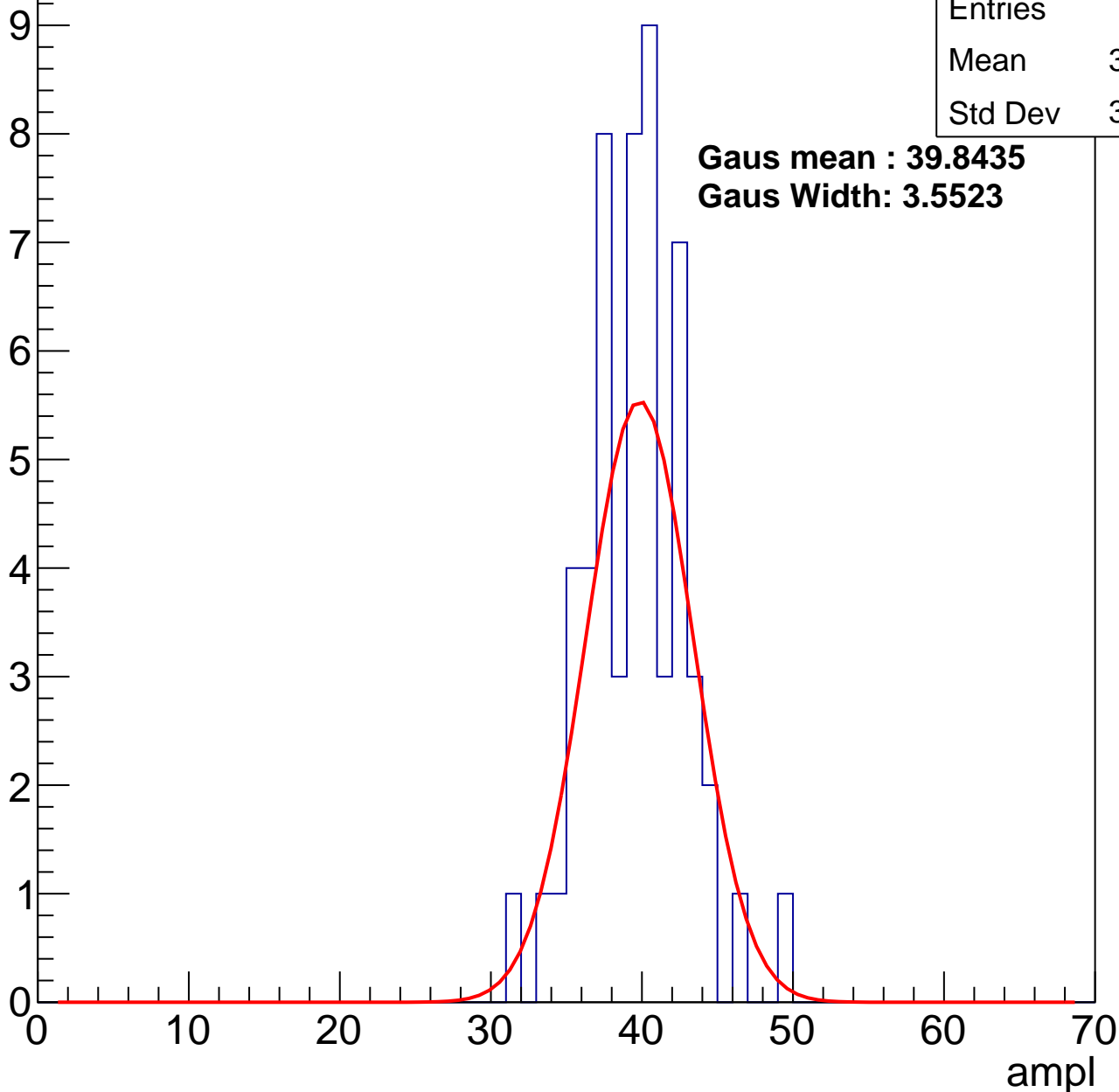
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	39.16
Std Dev	3.245

**Gaus mean : 39.8435**

**Gaus Width: 3.5523**



# B1L003S, U6-ch57, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	81
Mean	46.2
Std Dev	3.383

**Gaus mean : 46.7794**

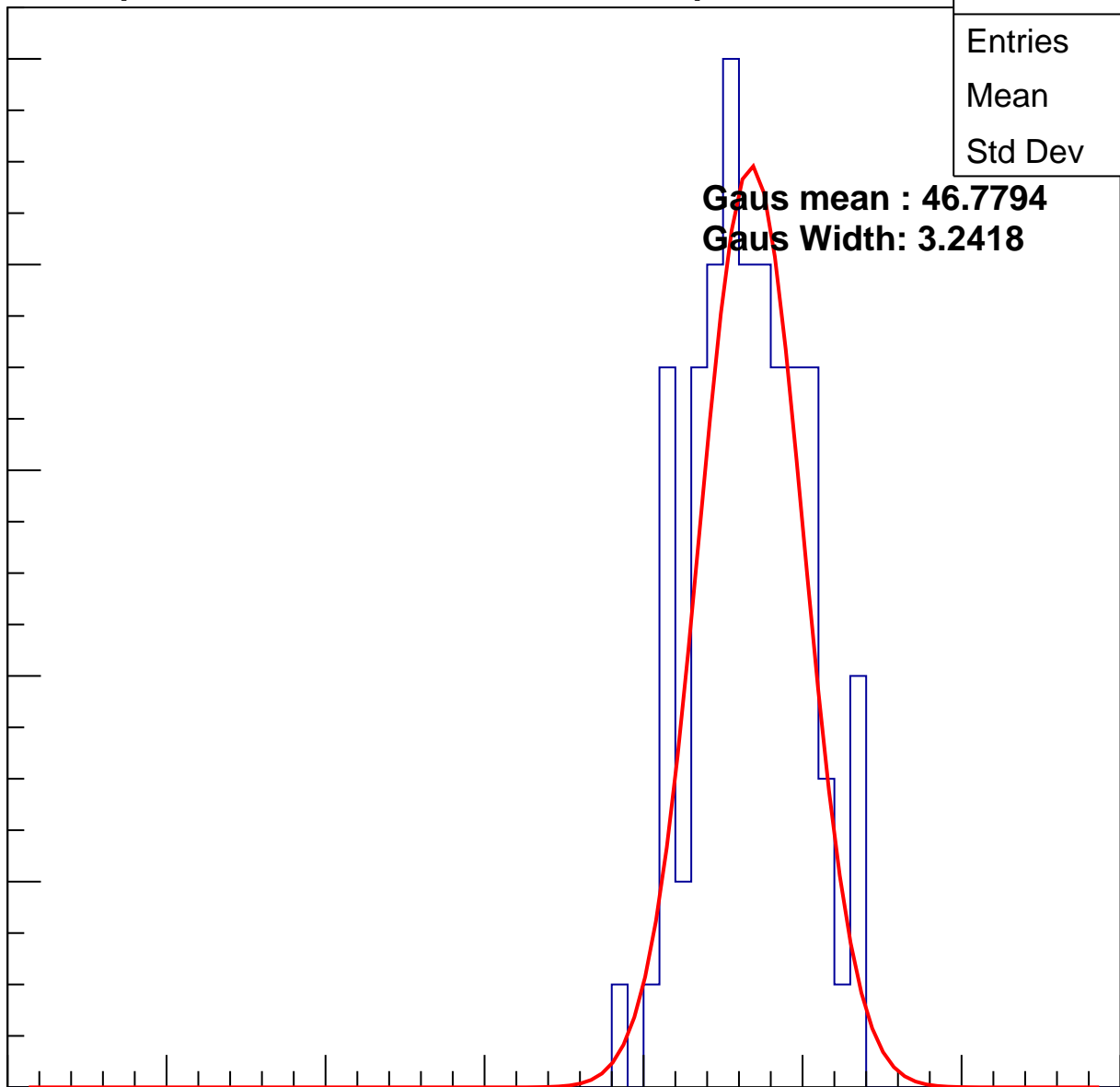
**Gaus Width: 3.2418**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

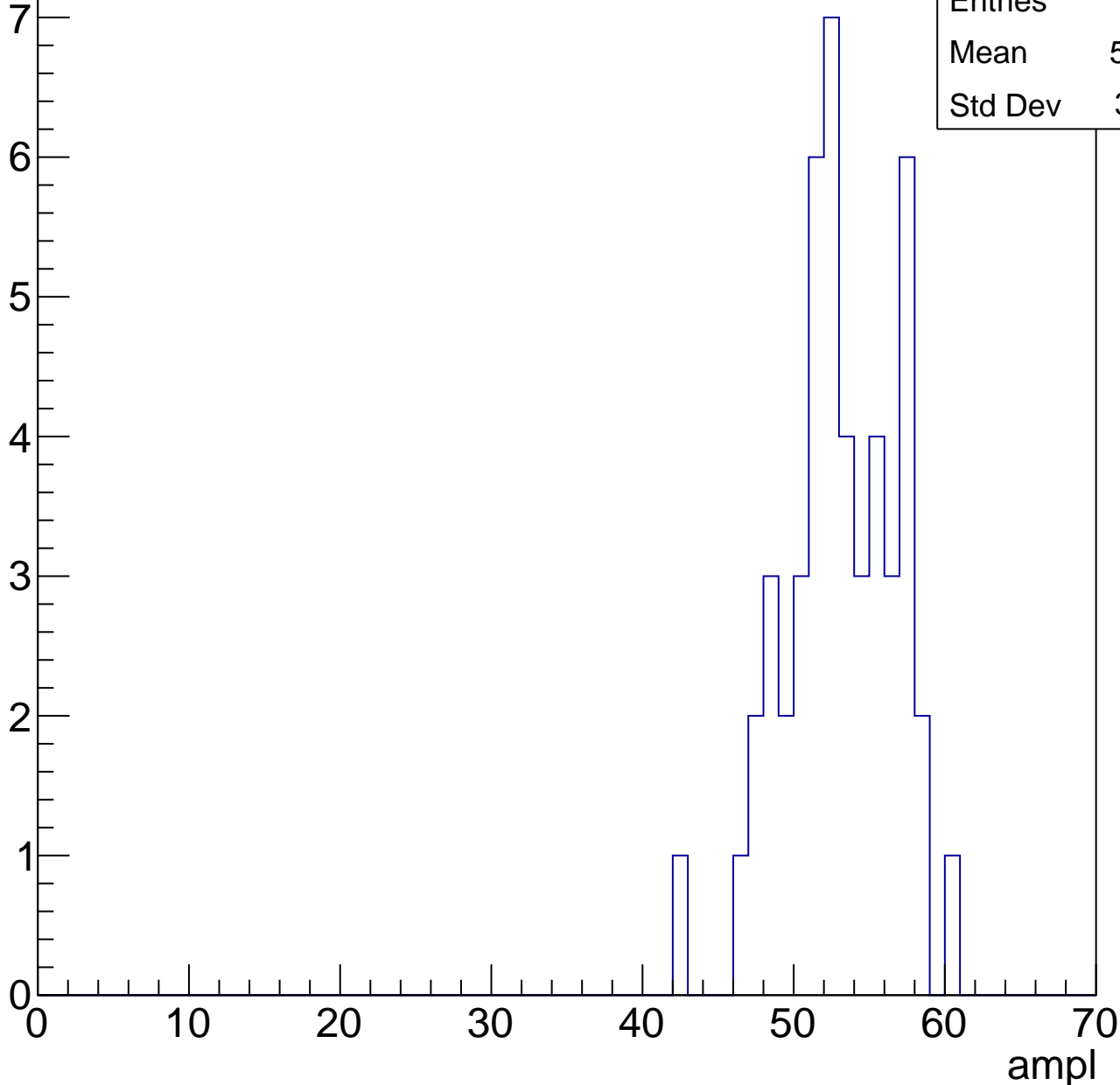


# B1L003S, U6-ch57, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	48
Mean	52.58
Std Dev	3.651

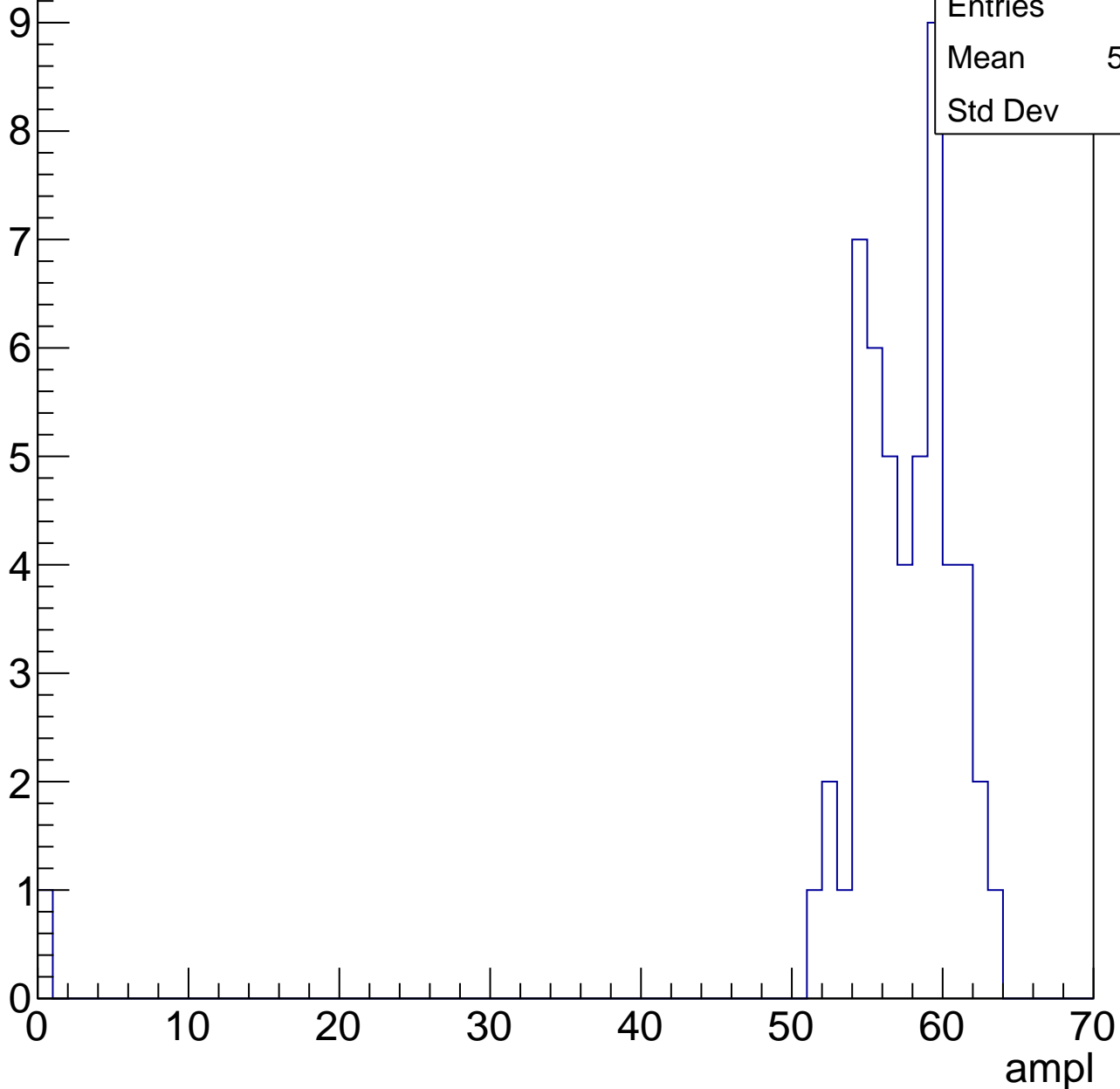


# B1L003S, U6-ch57, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	52
Mean	56.08
Std Dev	8.35

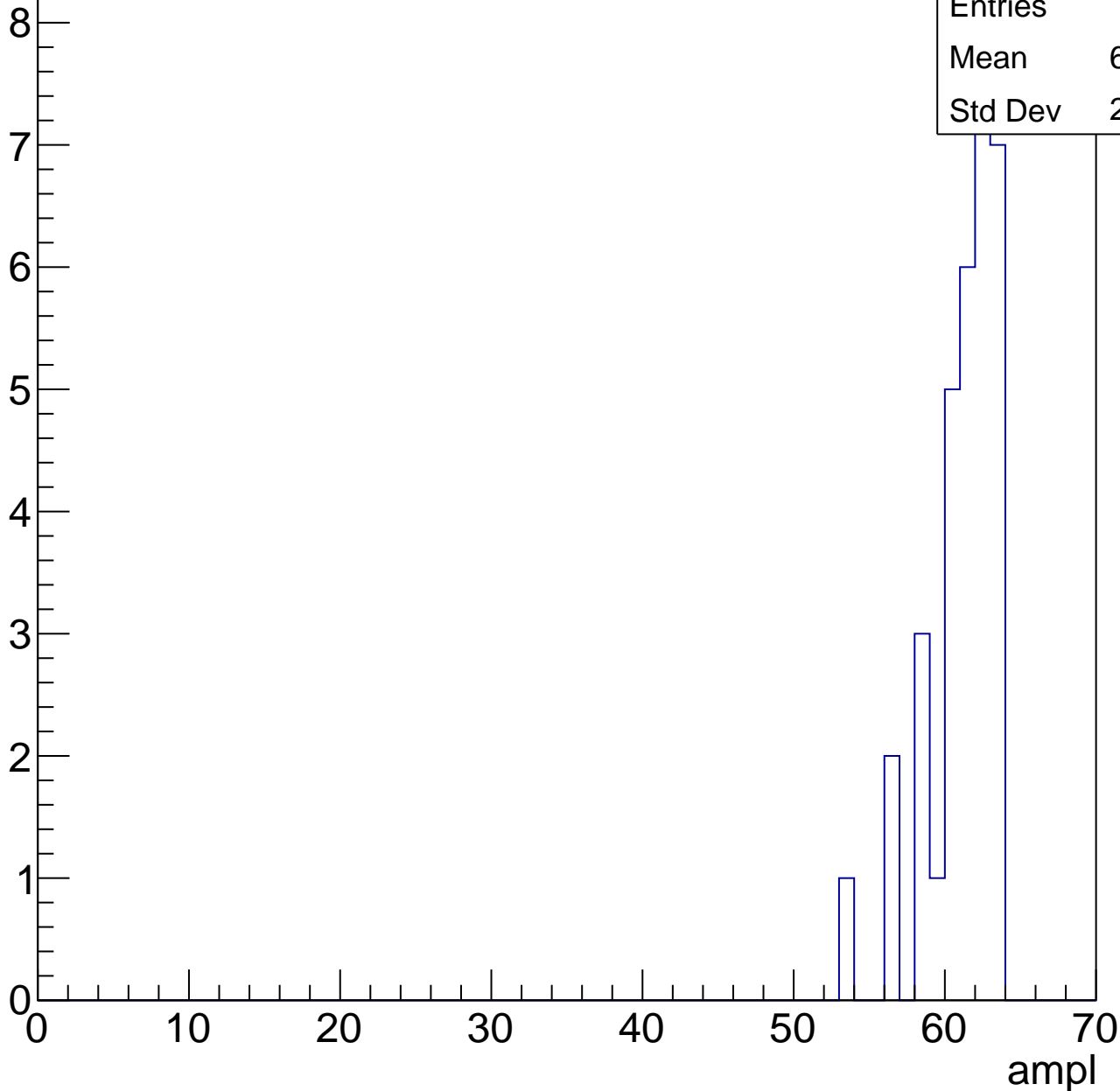


# B1L003S, U6-ch57, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	33
Mean	60.64
Std Dev	2.346



# B1L003S, U6-ch57, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	63
Std Dev	0

ampl



# B1L003S, U6-ch57, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U6-ch58, adc0

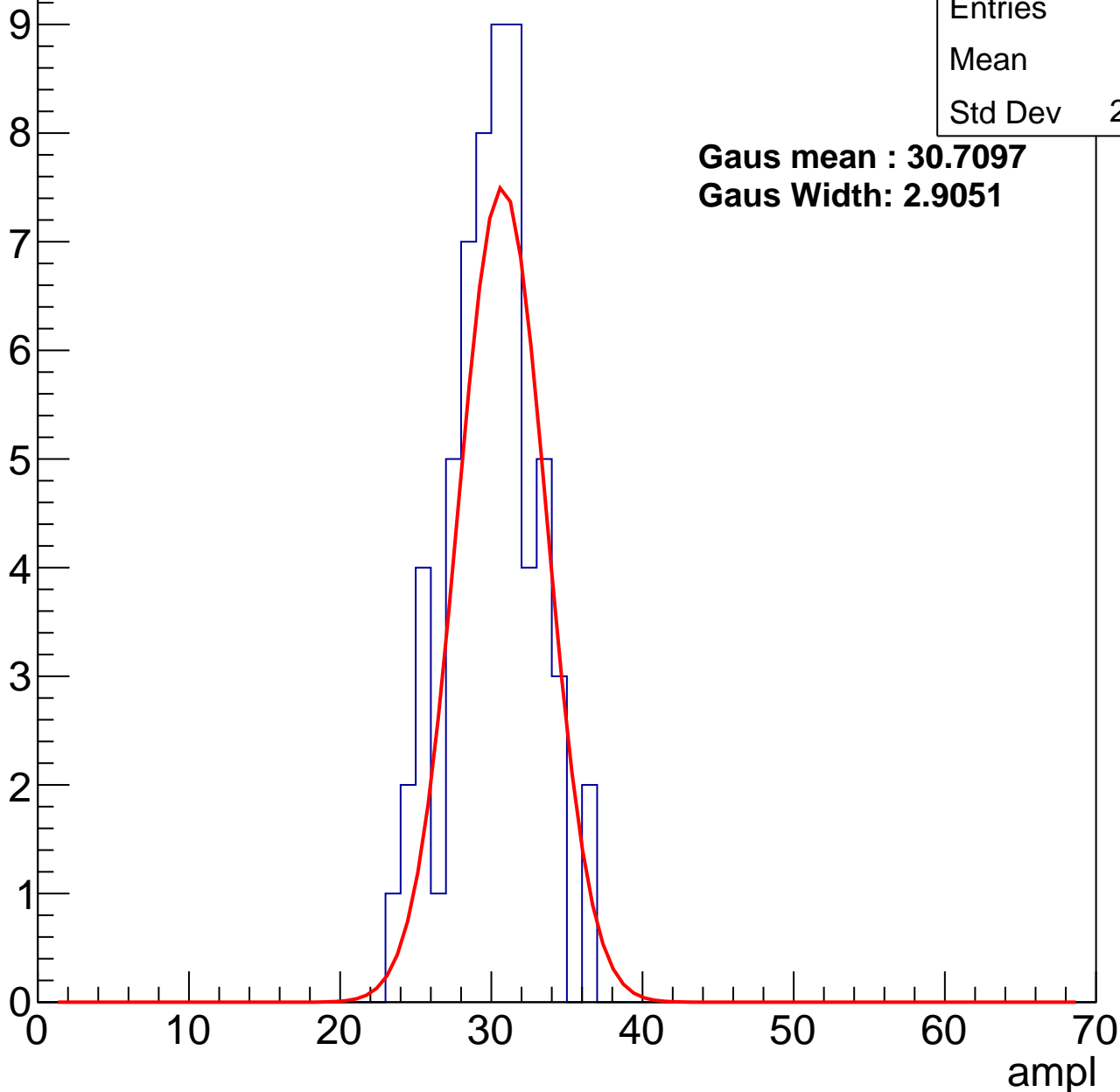
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	29.6
Std Dev	2.882

**Gaus mean : 30.7097**

**Gaus Width: 2.9051**



# B1L003S, U6-ch58, adc1

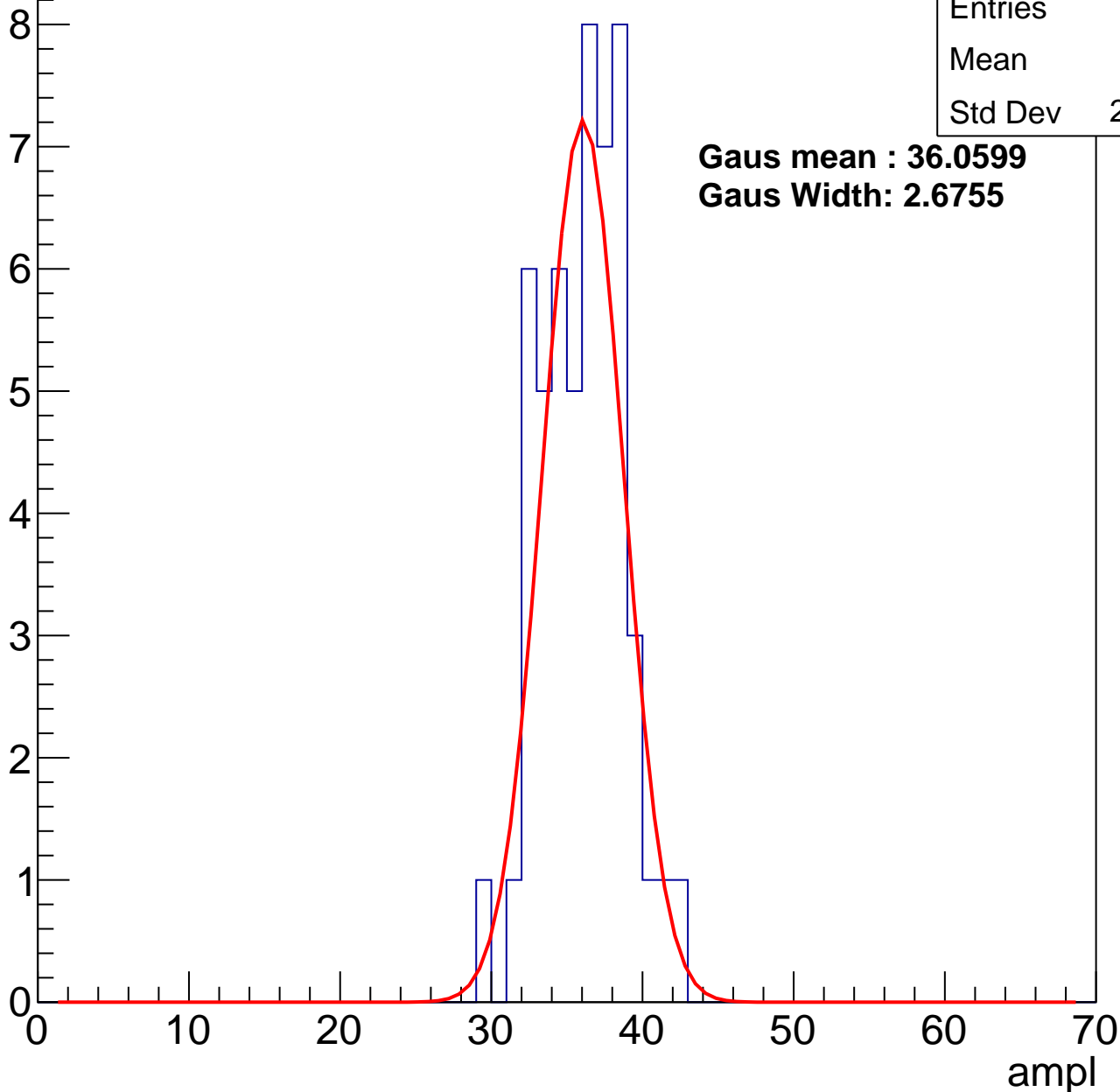
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	35.6
Std Dev	2.673

**Gaus mean : 36.0599**

**Gaus Width: 2.6755**



# B1L003S, U6-ch58, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	89
Mean	42.4
Std Dev	3.708

**Gaus mean : 43.1489**

**Gaus Width: 3.7499**

Entry

10

8

6

4

2

0

0

10

20

30

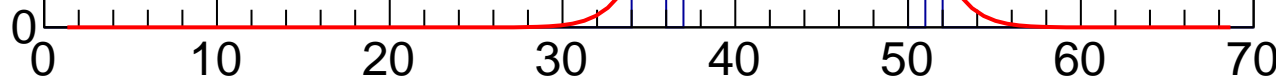
40

50

60

70

ampl

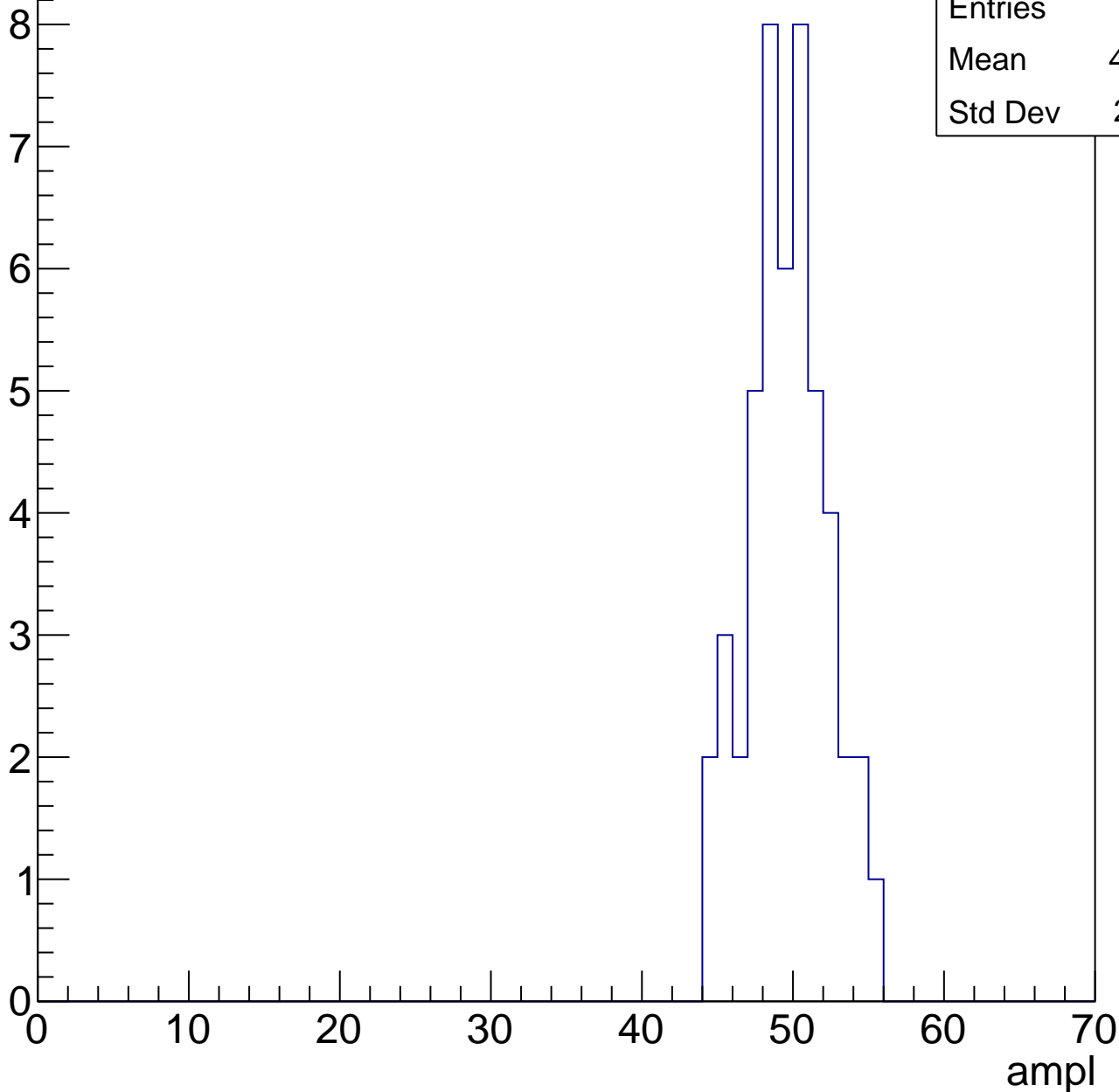


# B1L003S, U6-ch58, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	48
Mean	49.17
Std Dev	2.601

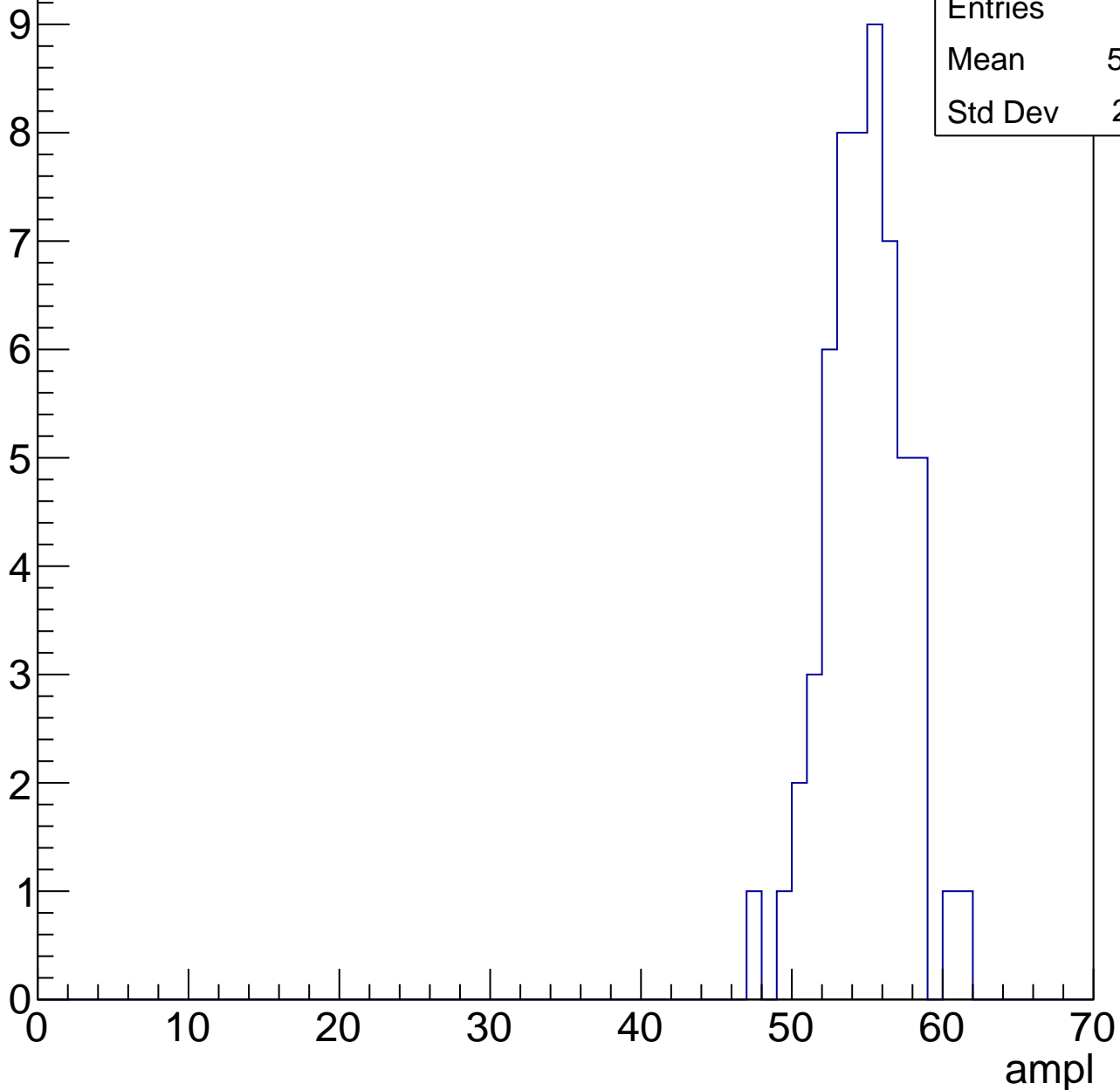


# B1L003S, U6-ch58, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	54.39
Std Dev	2.661

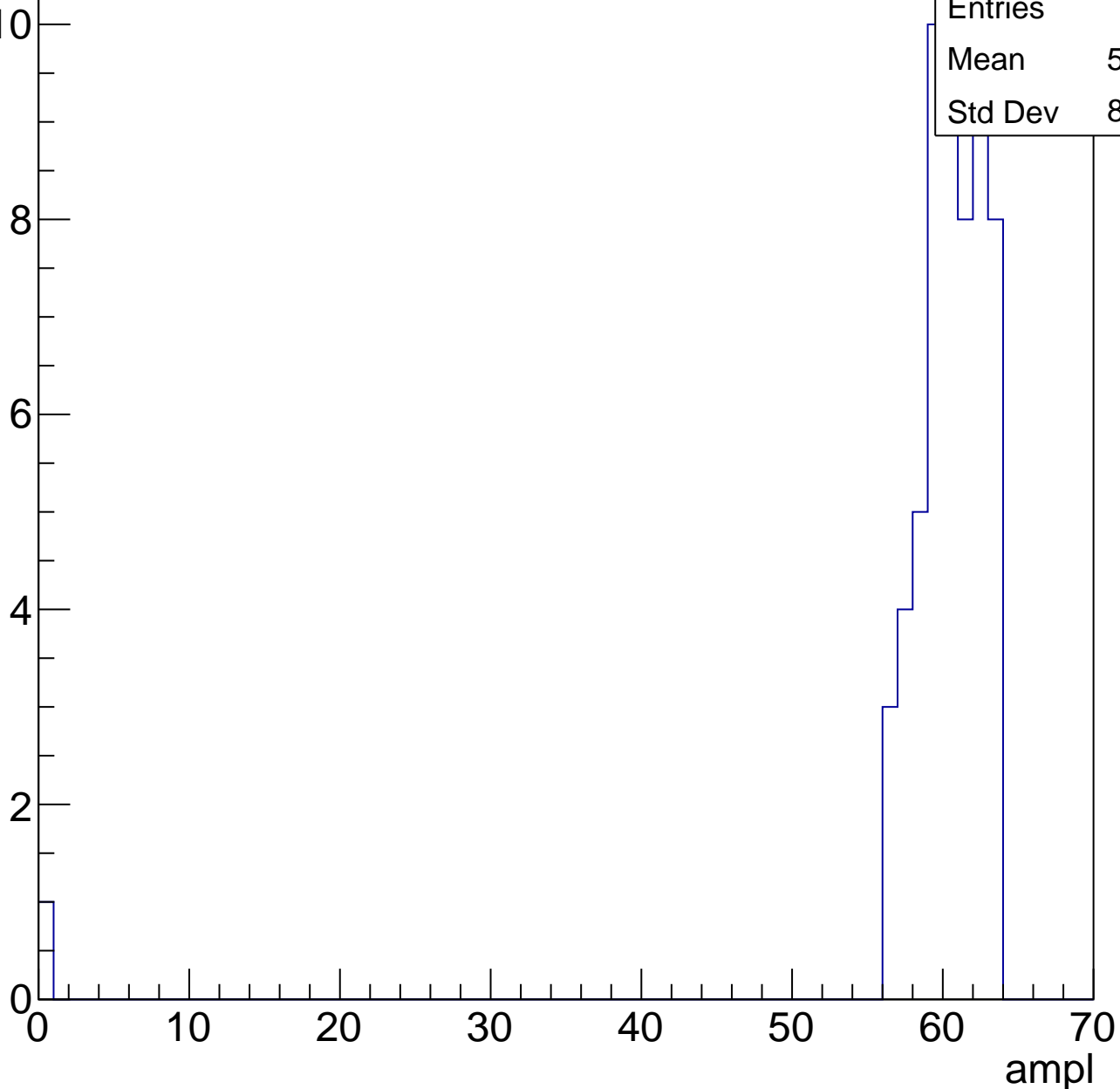


# B1L003S, U6-ch58, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

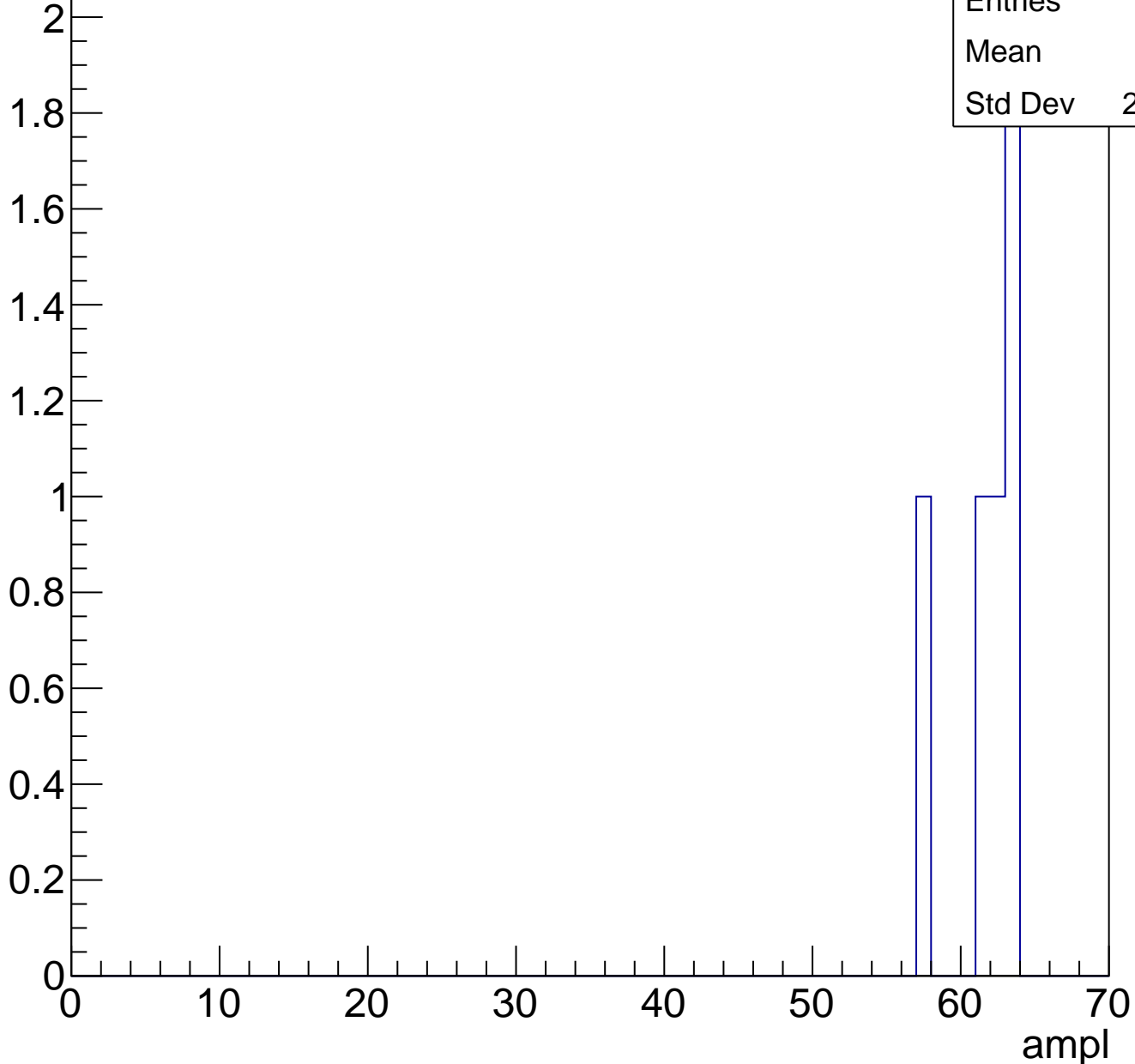
Entries	57
Mean	59.05
Std Dev	8.142



# B1L003S, U6-ch58, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch58, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch59, adc0

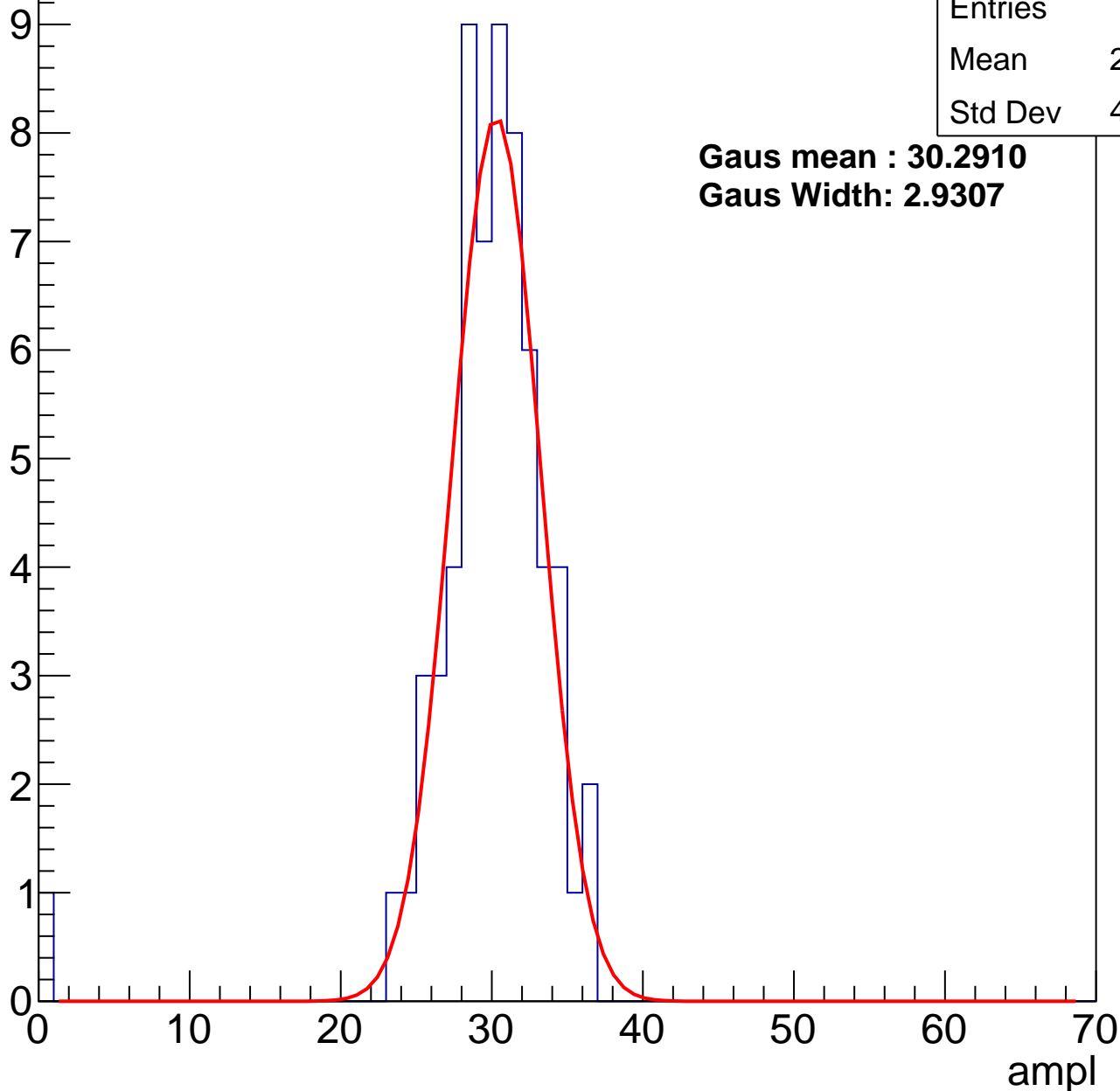
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	29.33
Std Dev	4.694

**Gaus mean : 30.2910**

**Gaus Width: 2.9307**



# B1L003S, U6-ch59, adc1

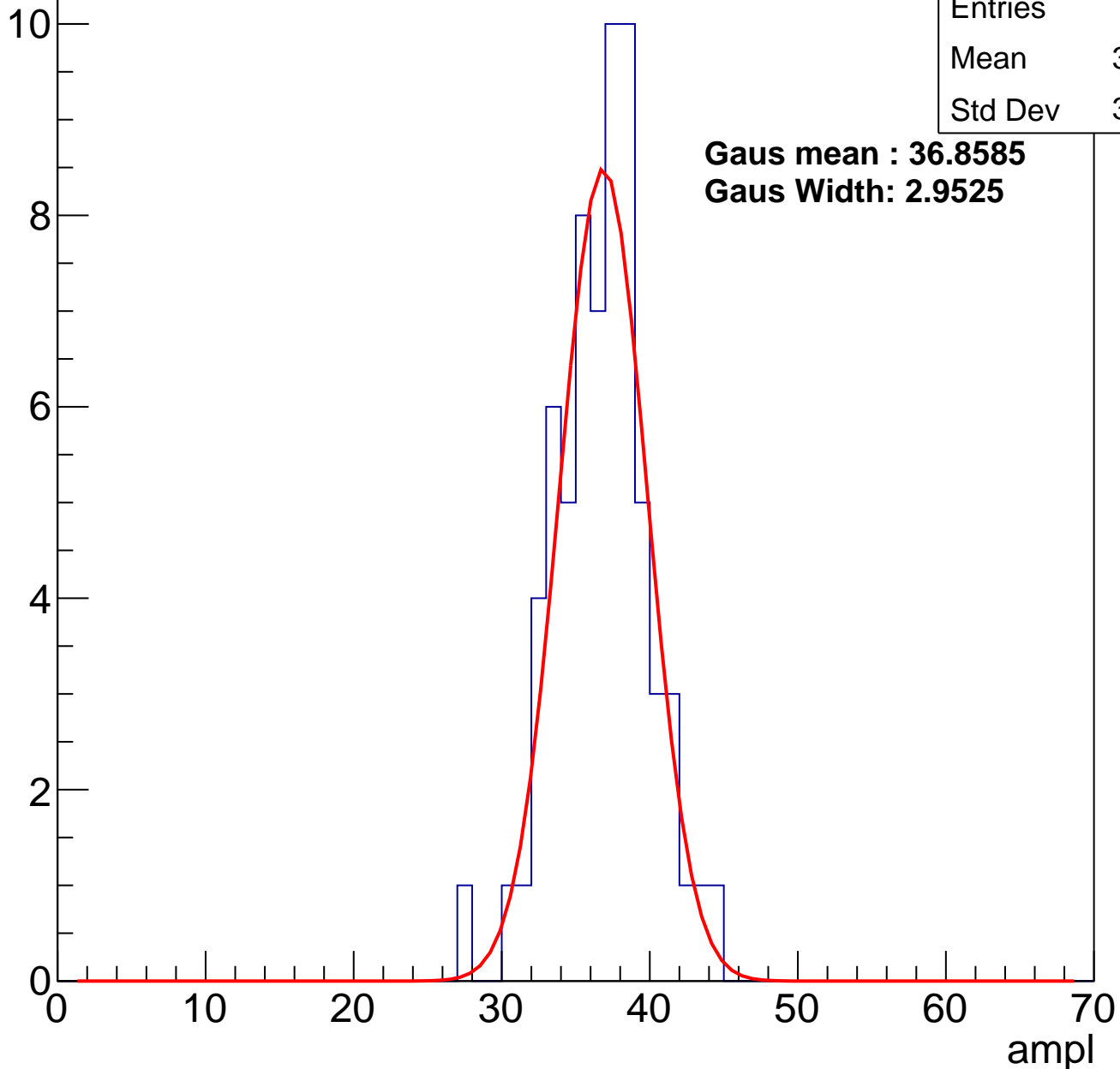
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	67
Mean	36.31
Std Dev	3.111

**Gaus mean : 36.8585**

**Gaus Width: 2.9525**

Entry



# B1L003S, U6-ch59, adc2

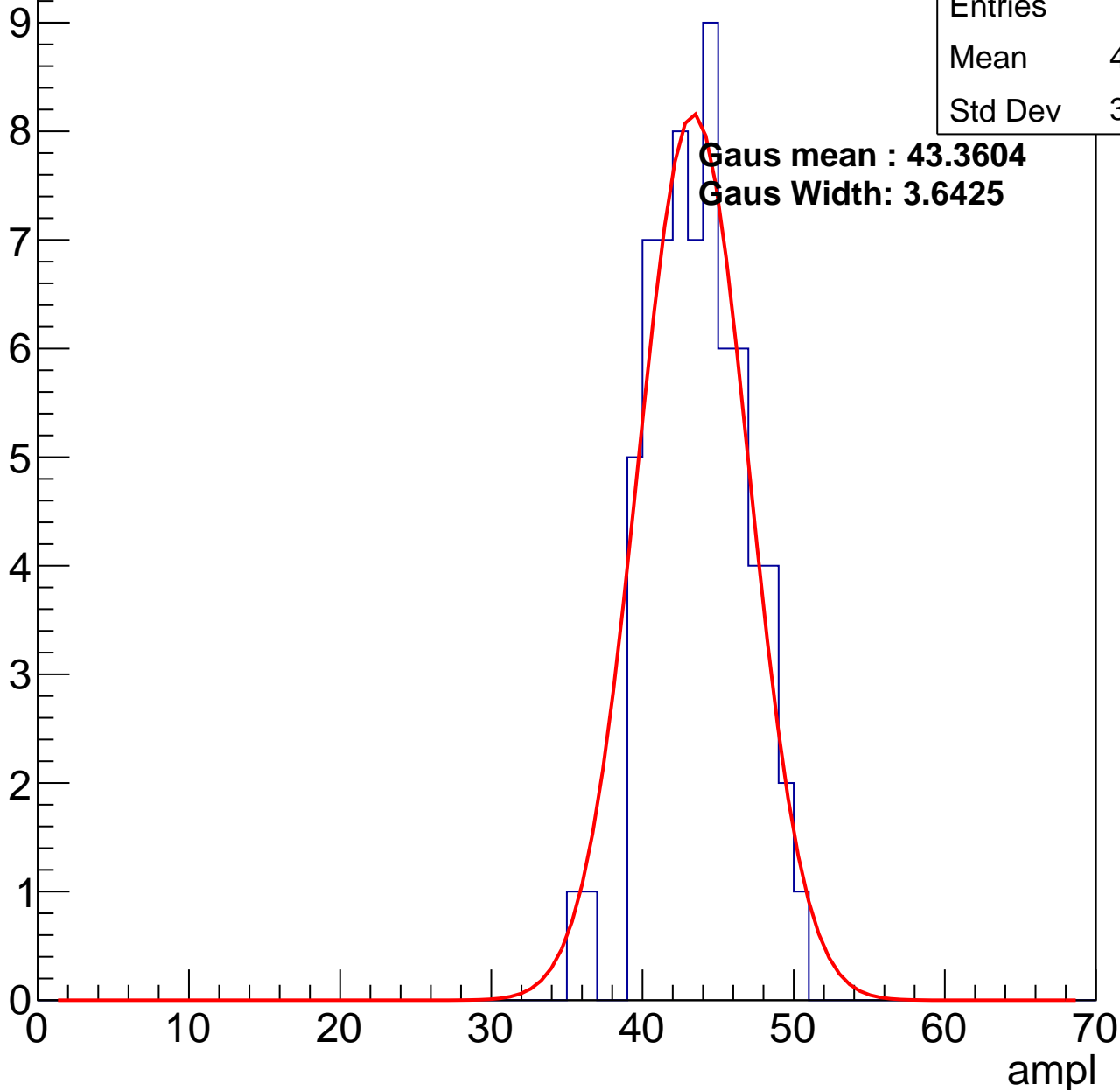
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	43.24
Std Dev	3.116

**Gaus mean : 43.3604**

**Gaus Width: 3.6425**

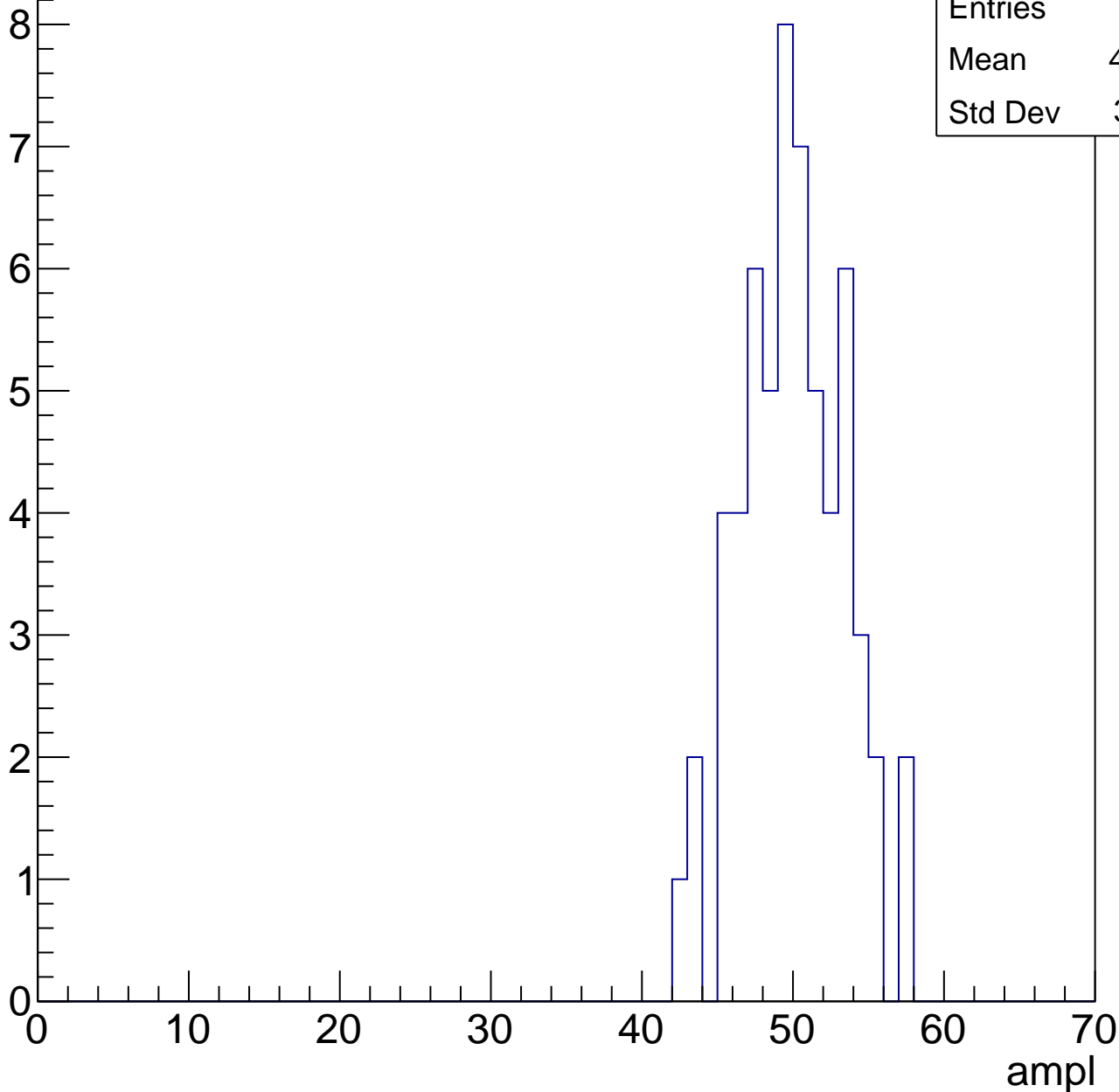


# B1L003S, U6-ch59, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	49.54
Std Dev	3.361

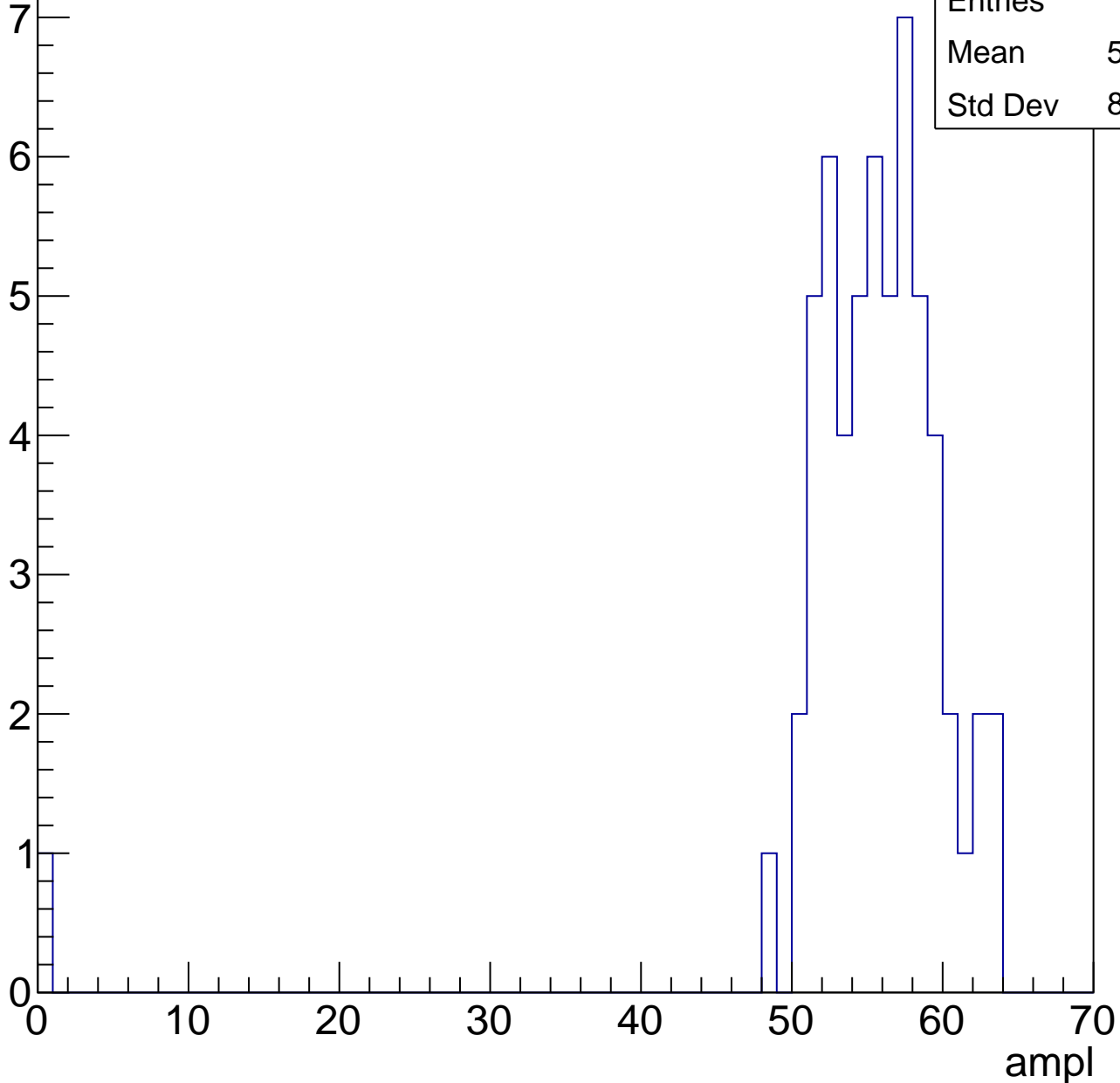


# B1L003S, U6-ch59, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

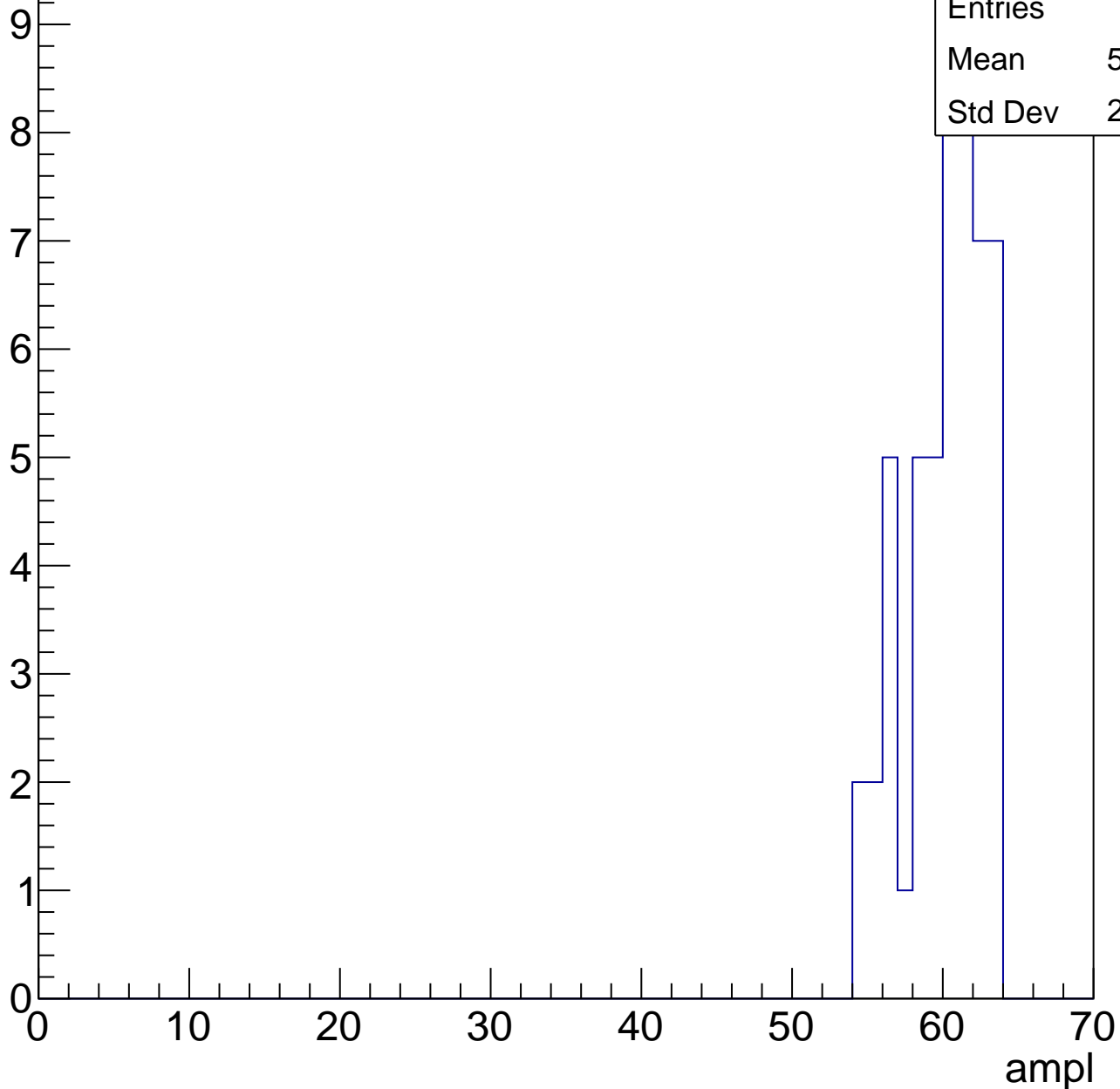
Entries	58
Mean	54.53
Std Dev	8.009



# B1L003S, U6-ch59, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

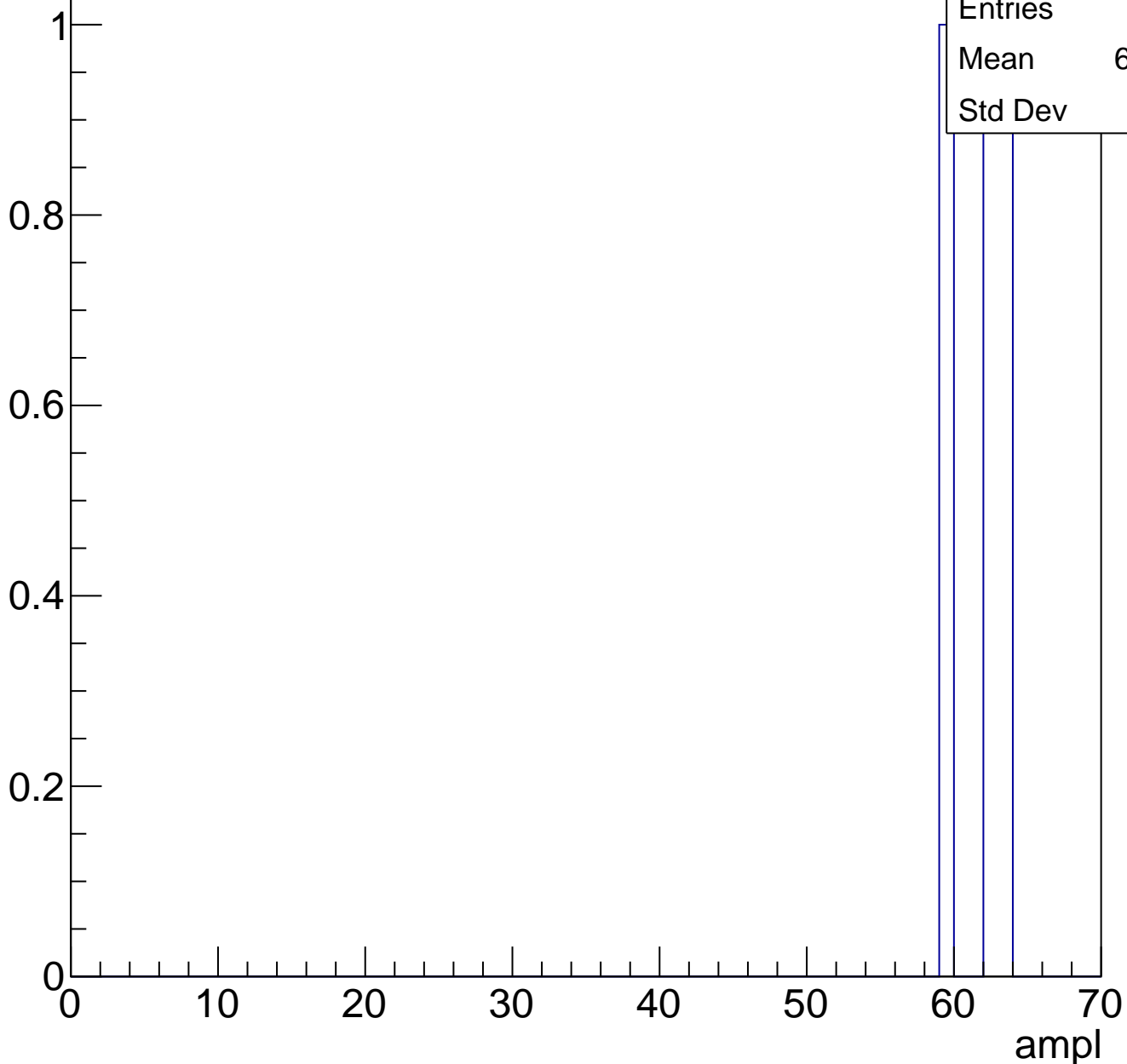


Entries	51
Mean	59.69
Std Dev	2.548

# B1L003S, U6-ch59, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch59, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch60, adc0

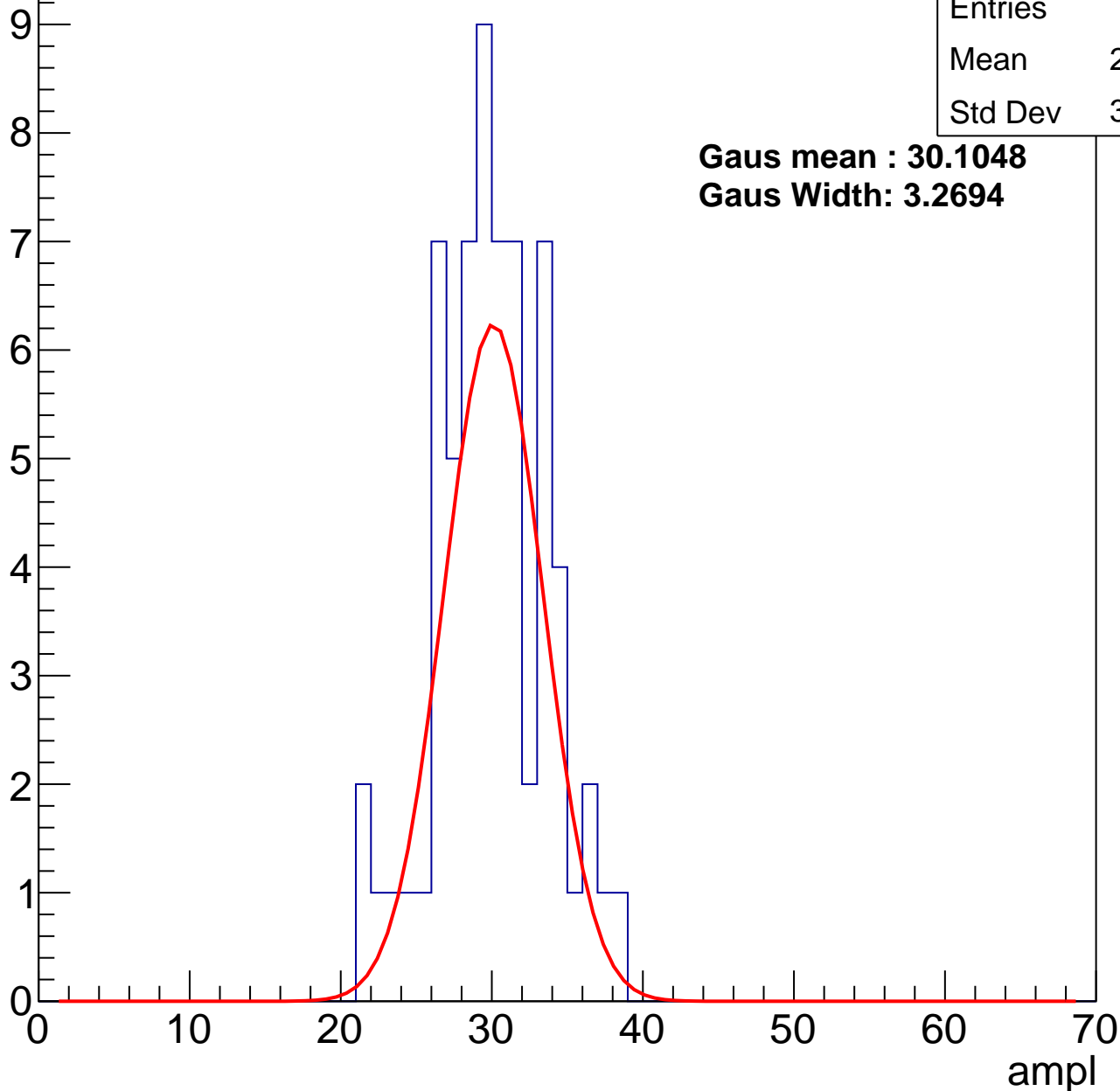
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	29.55
Std Dev	3.627

**Gaus mean : 30.1048**

**Gaus Width: 3.2694**



# B1L003S, U6-ch60, adc1

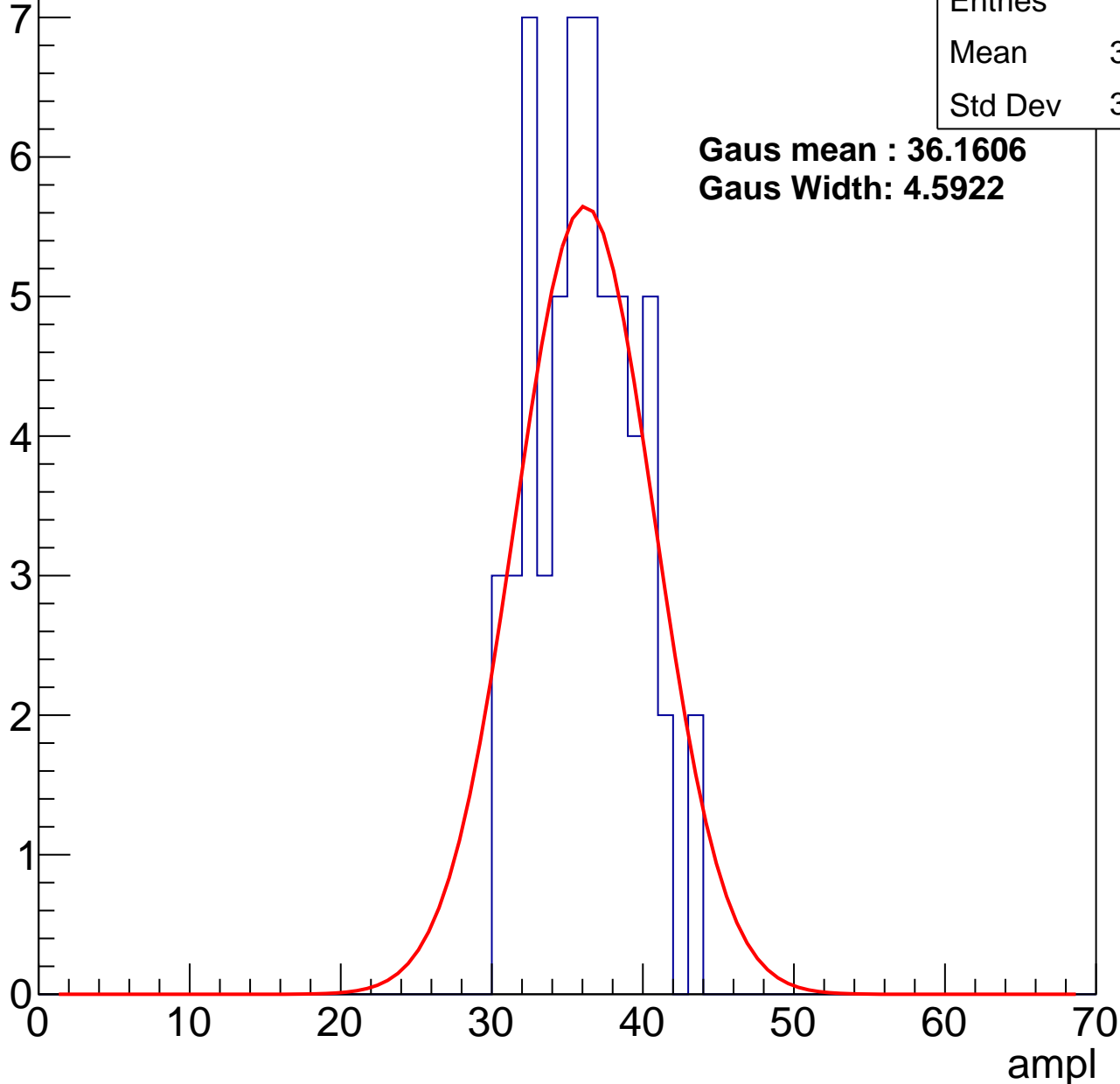
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	35.72
Std Dev	3.305

**Gaus mean : 36.1606**

**Gaus Width: 4.5922**



# B1L003S, U6-ch60, adc2

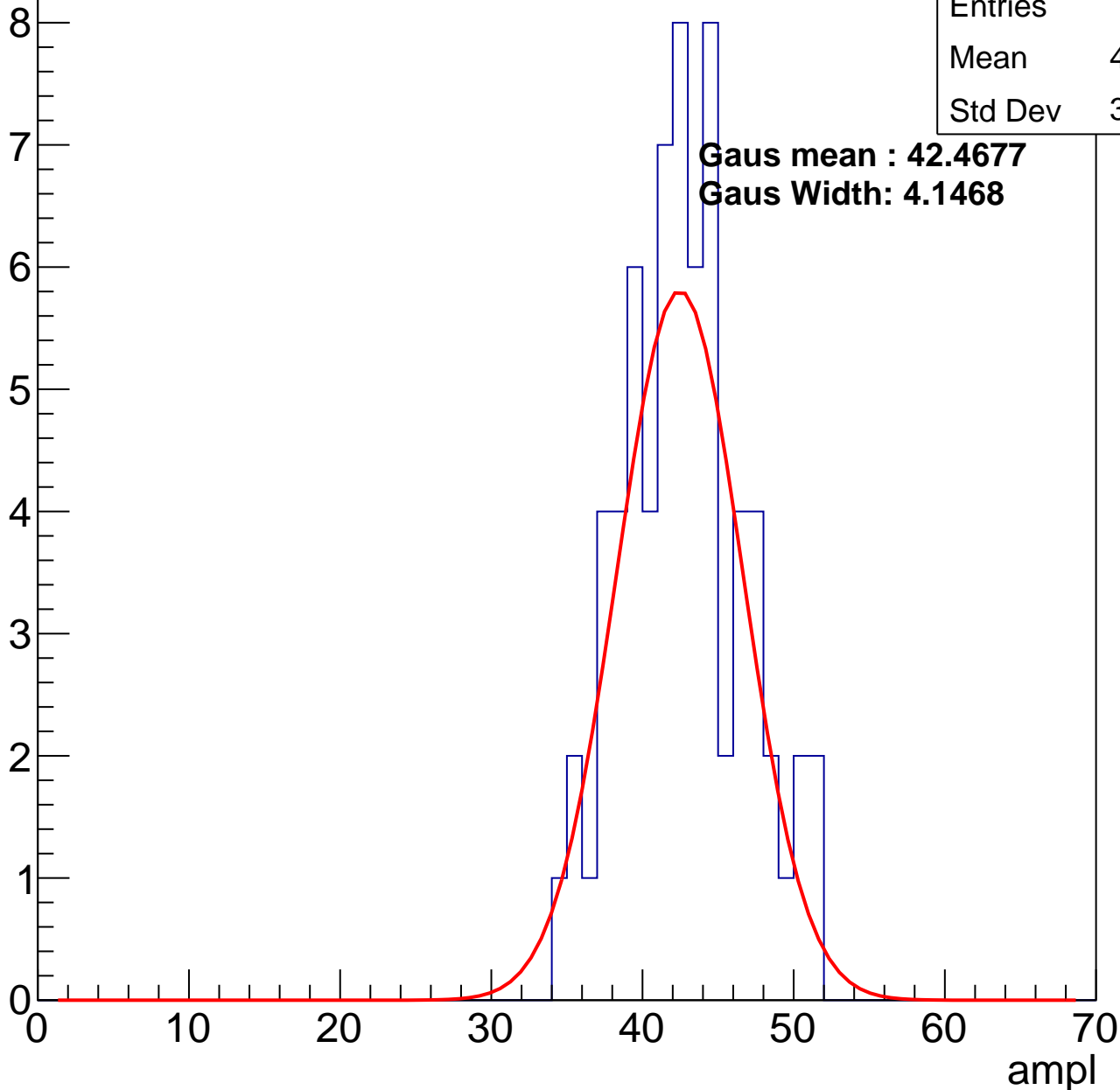
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	42.29
Std Dev	3.956

**Gaus mean : 42.4677**

**Gaus Width: 4.1468**

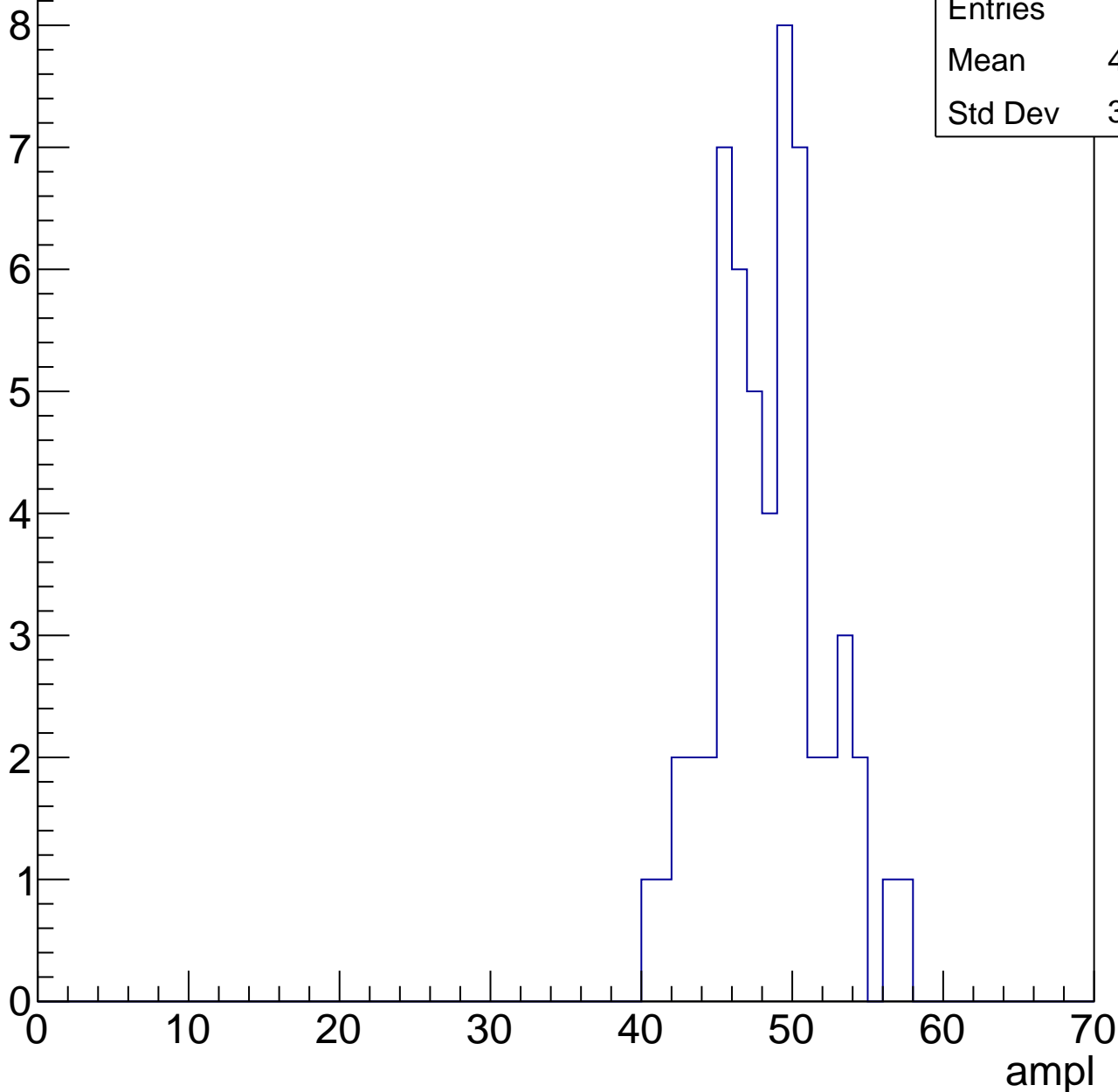


# B1L003S, U6-ch60, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	47.95
Std Dev	3.627

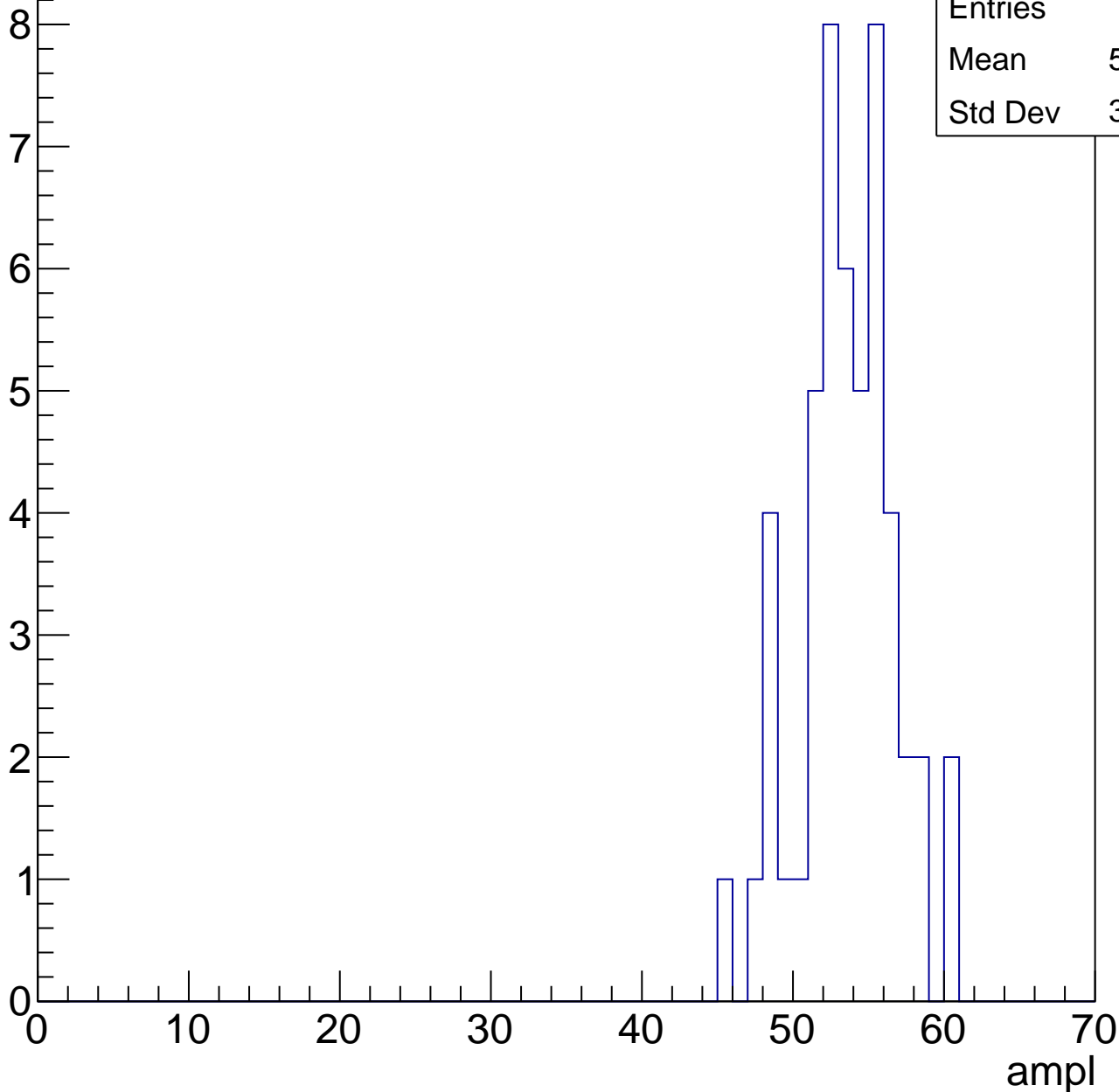


# B1L003S, U6-ch60, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

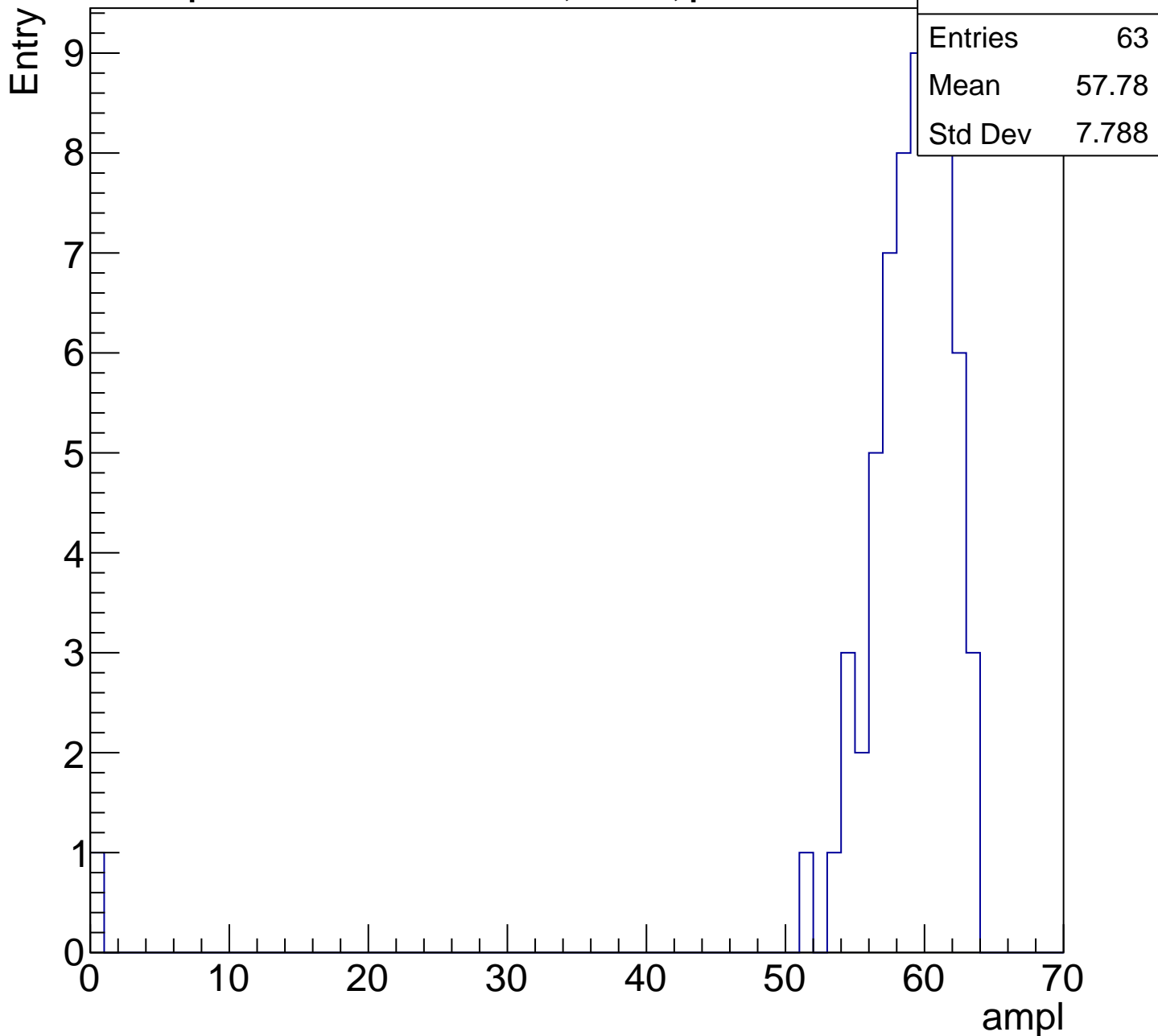
Entry

Entries	50
Mean	53.12
Std Dev	3.179



# B1L003S, U6-ch60, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

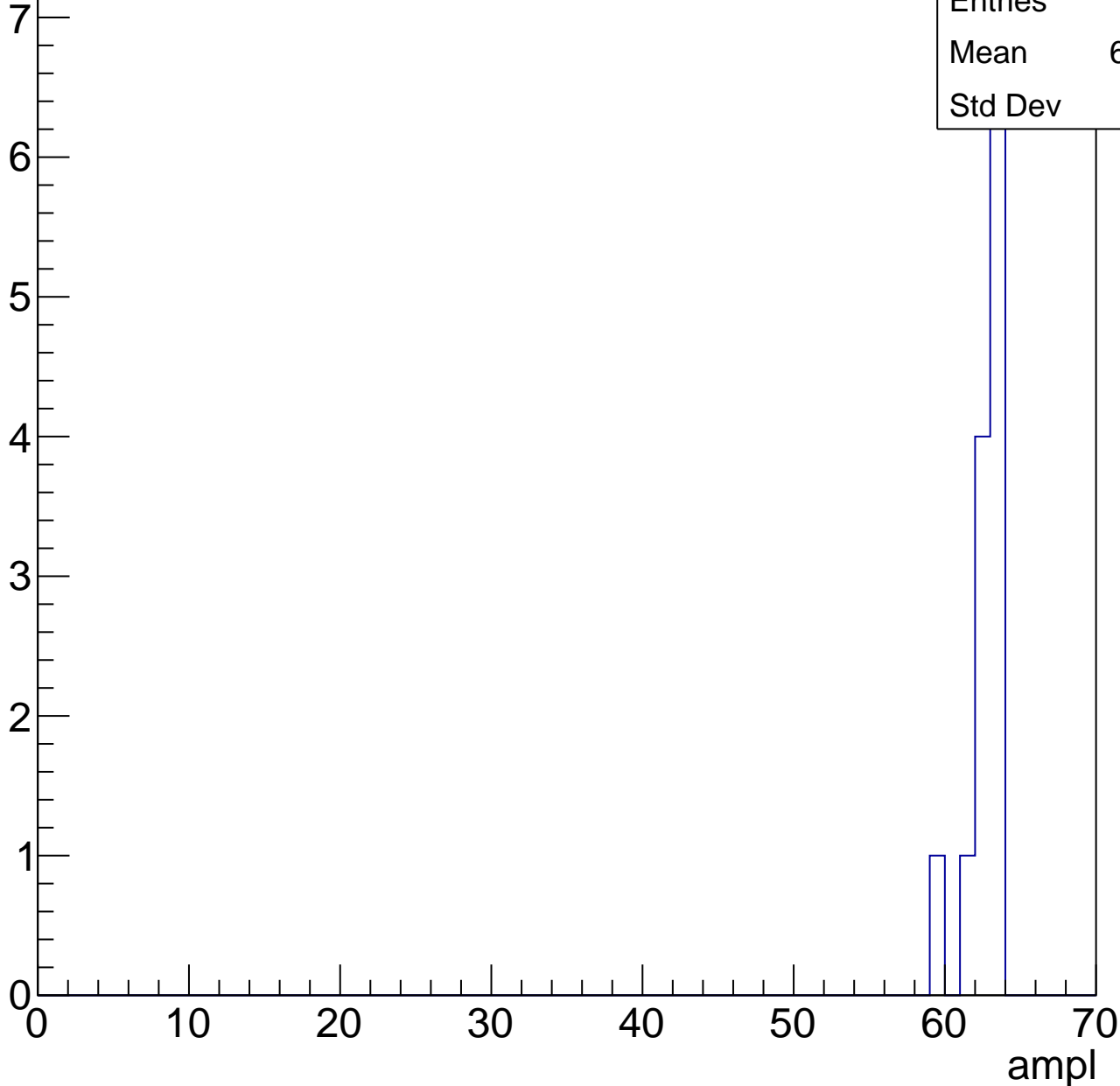


# B1L003S, U6-ch60, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	13
Mean	62.23
Std Dev	1.12





# B1L003S, U6-ch60, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	3
Mean	6.333
Std Dev	8.957

# B1L003S, U6-ch61, adc0

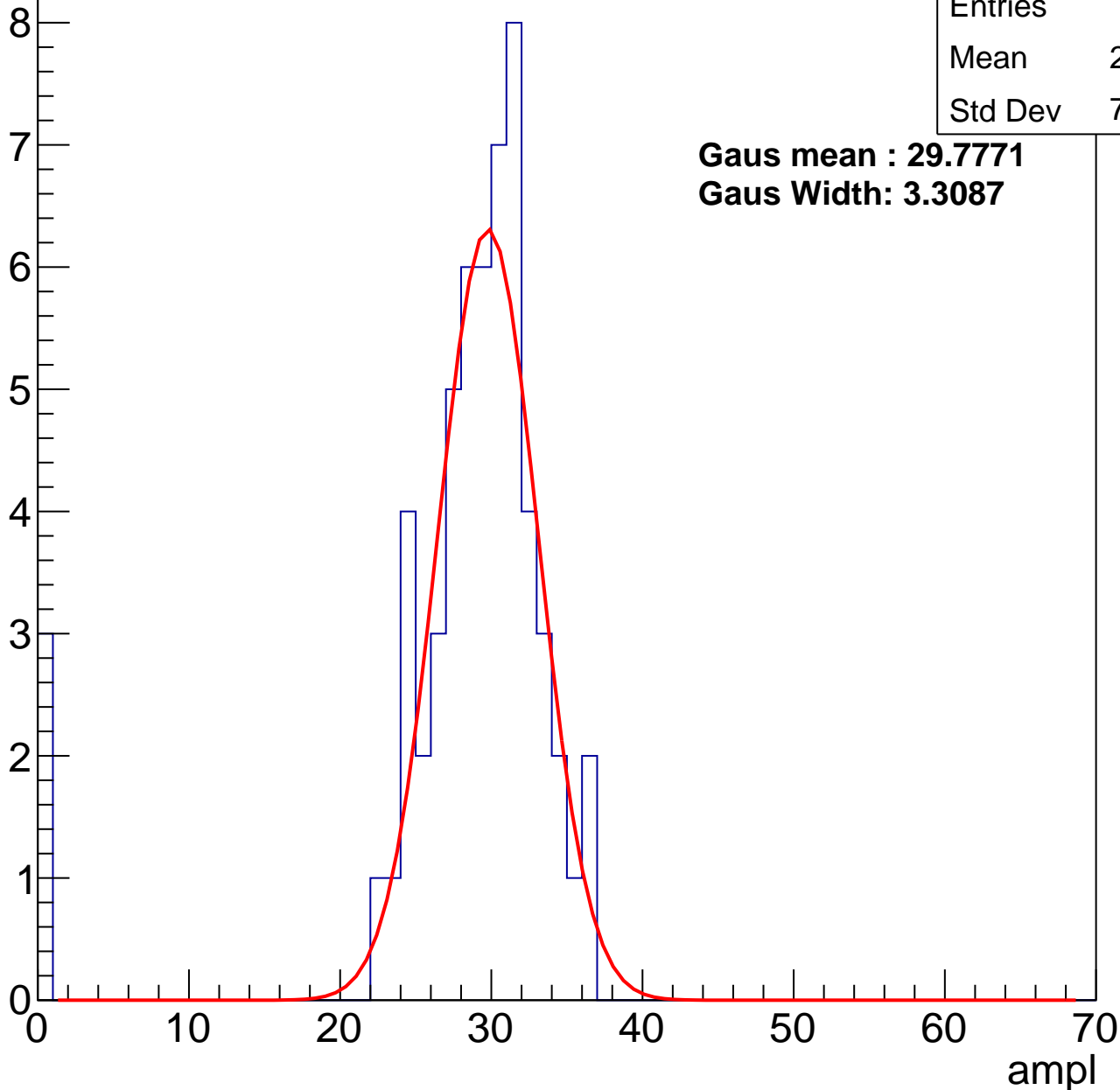
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	27.69
Std Dev	7.192

**Gaus mean : 29.7771**

**Gaus Width: 3.3087**



# B1L003S, U6-ch61, adc1

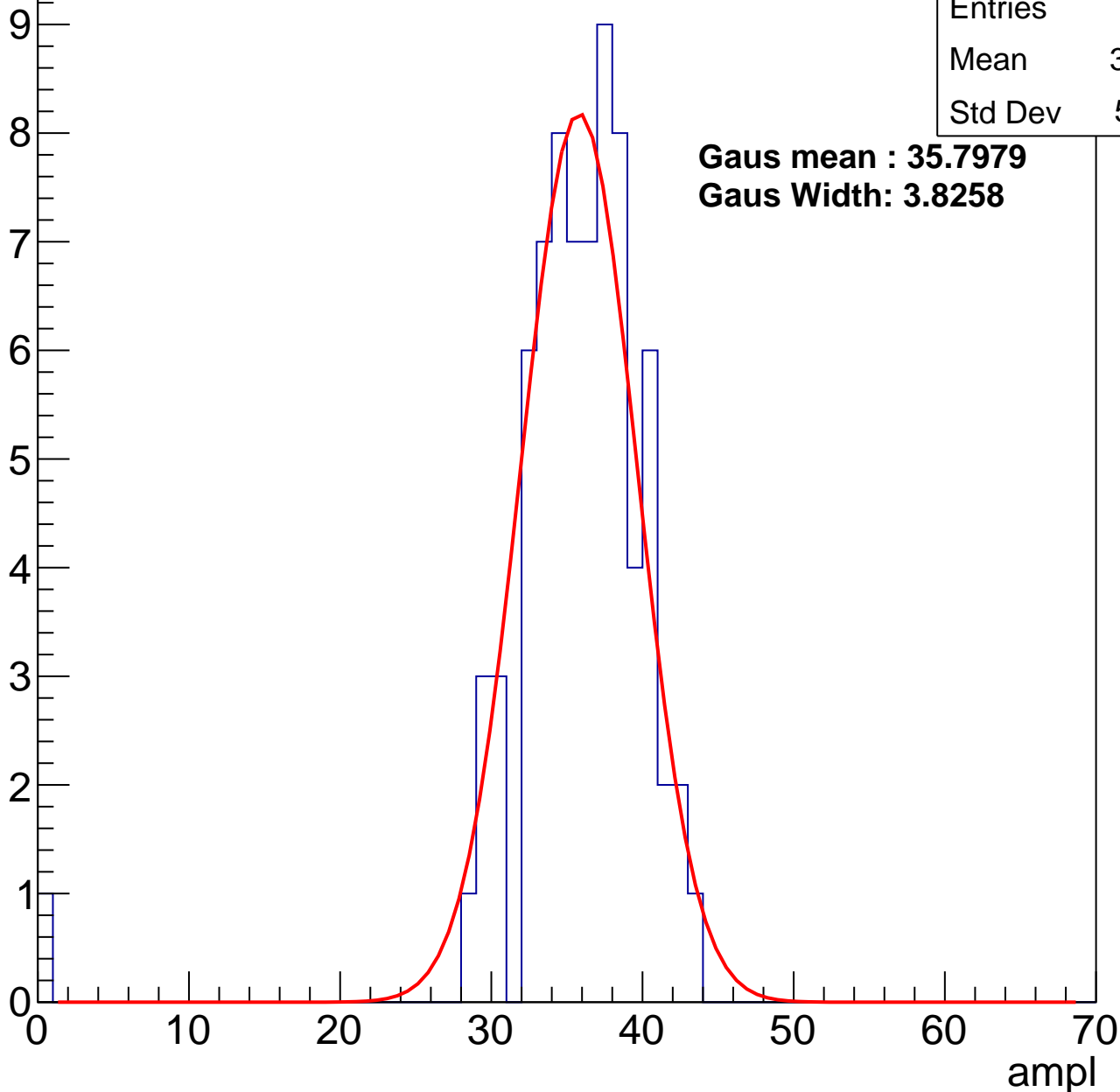
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	75
Mean	35.19
Std Dev	5.301

**Gaus mean : 35.7979**

**Gaus Width: 3.8258**



# B1L003S, U6-ch61, adc2

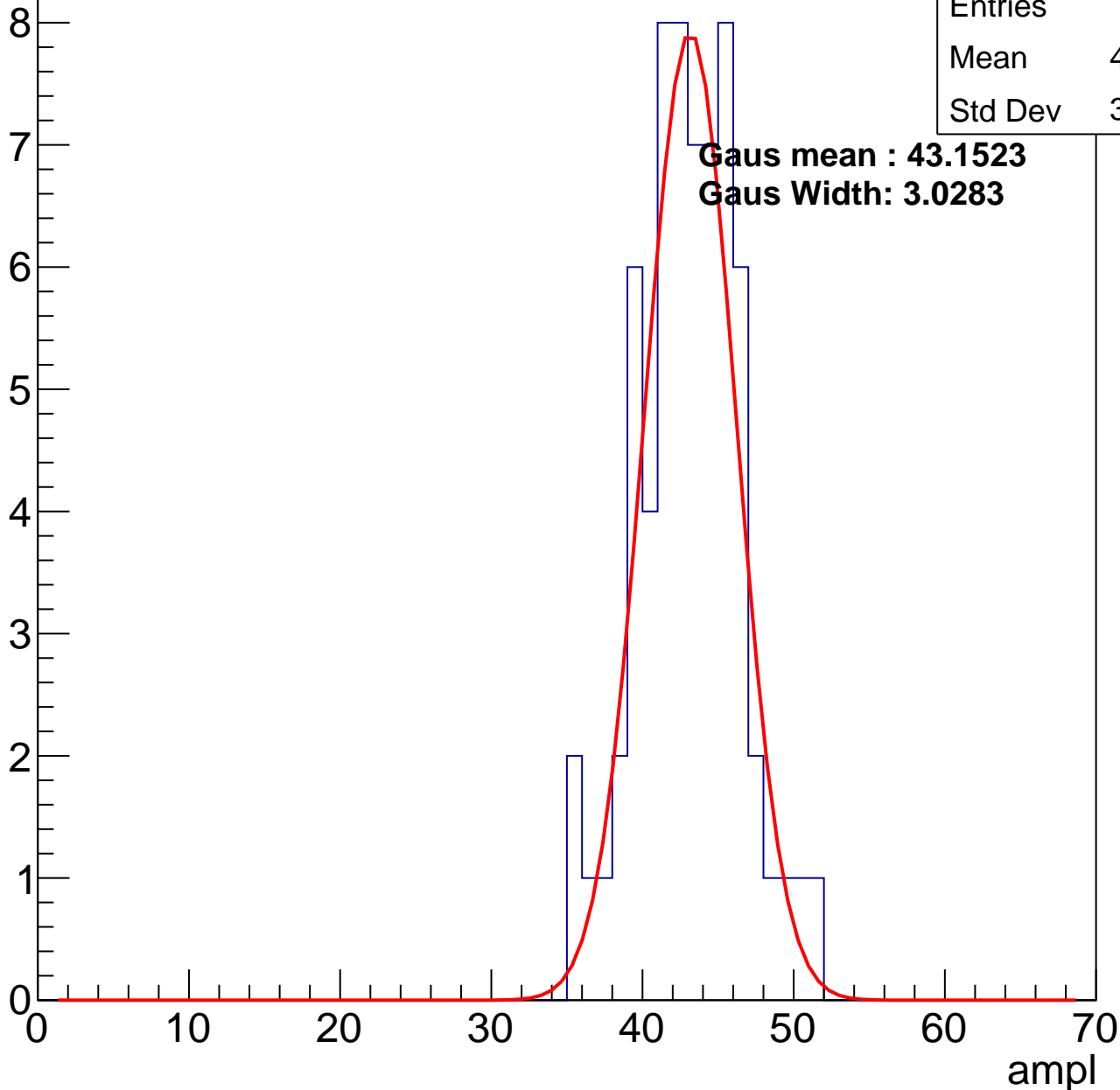
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	42.64
Std Dev	3.315

**Gaus mean : 43.1523**

**Gaus Width: 3.0283**

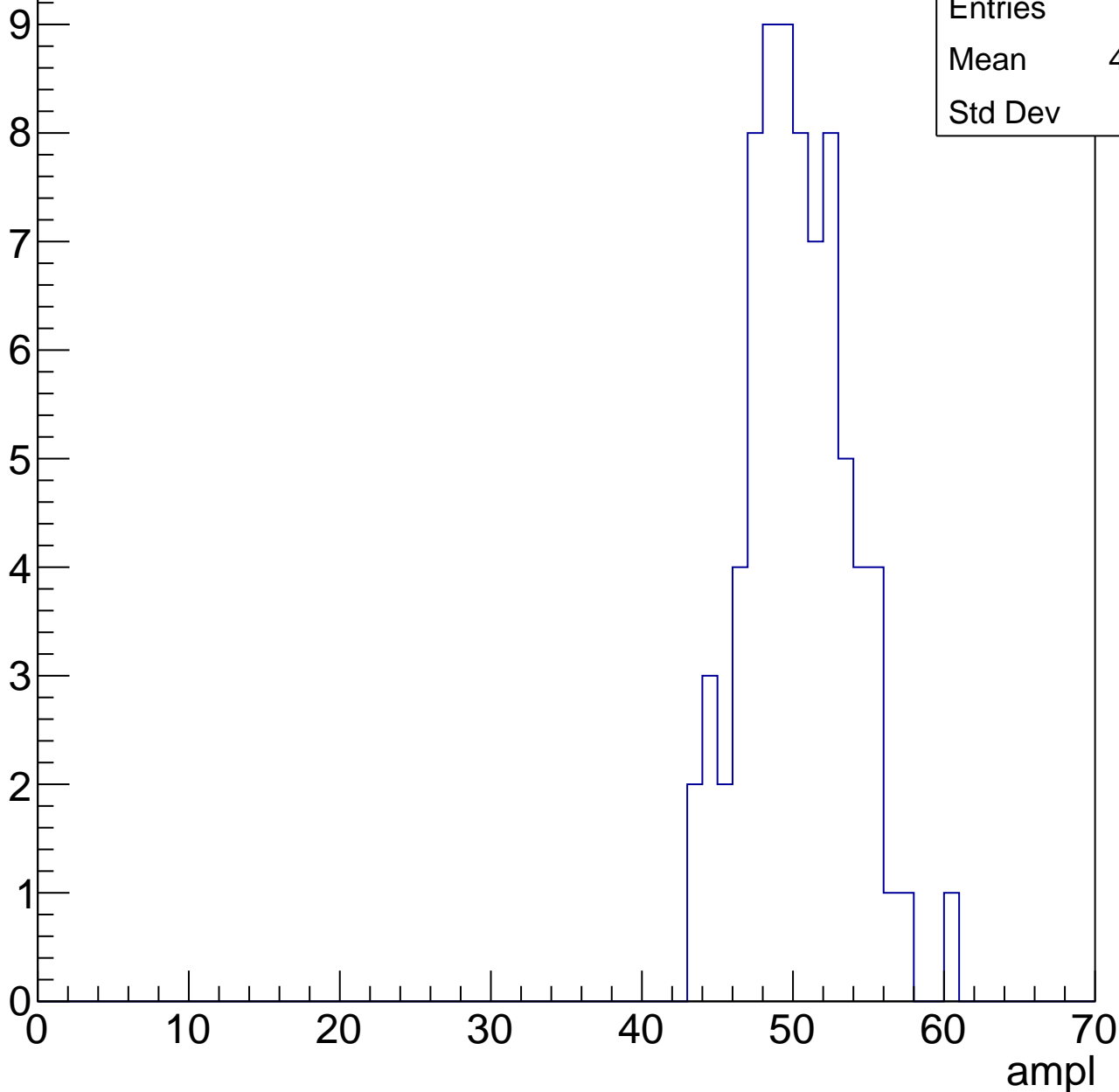


# B1L003S, U6-ch61, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	76
Mean	49.84
Std Dev	3.38

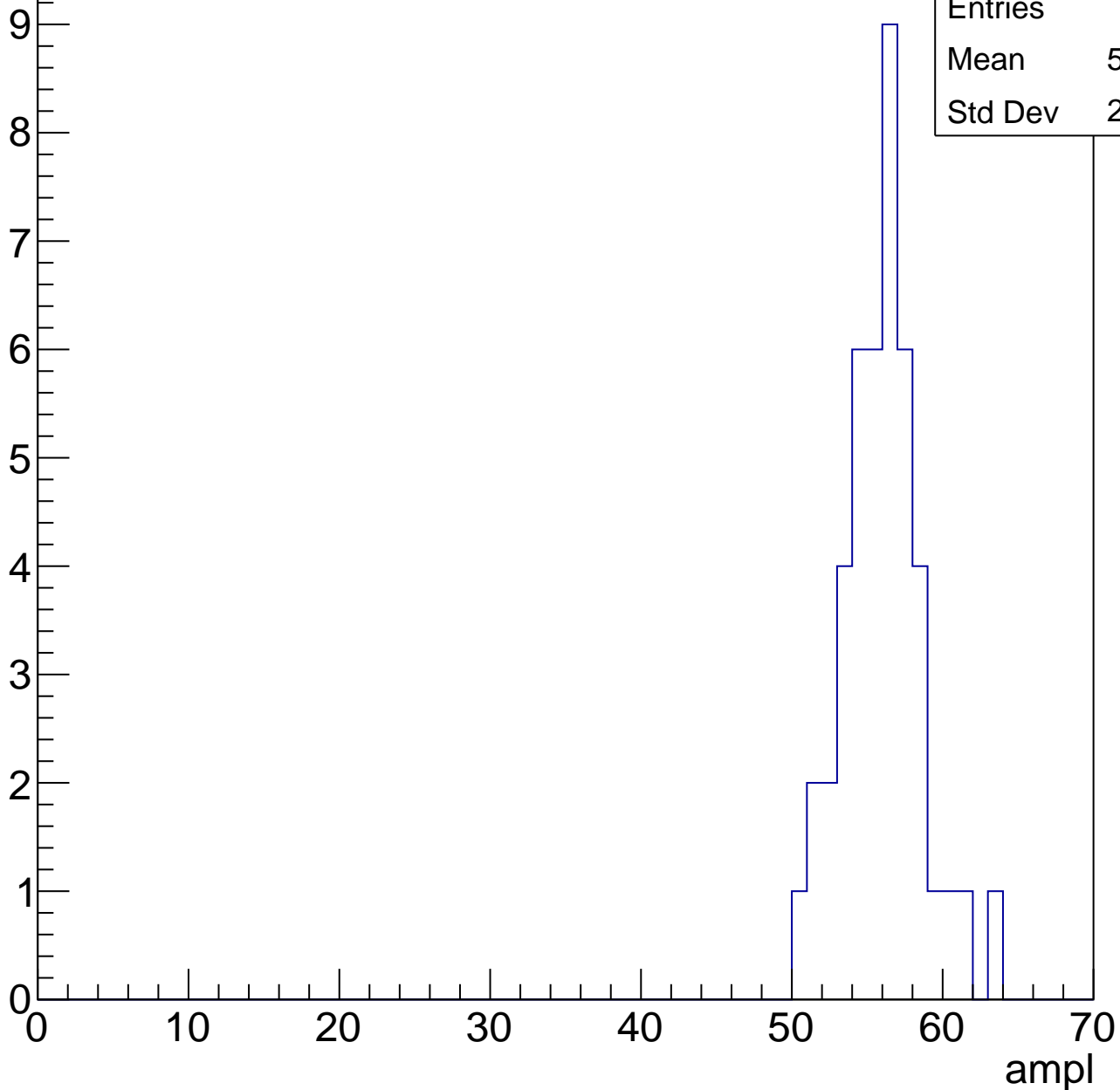


# B1L003S, U6-ch61, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	44
Mean	55.52
Std Dev	2.589

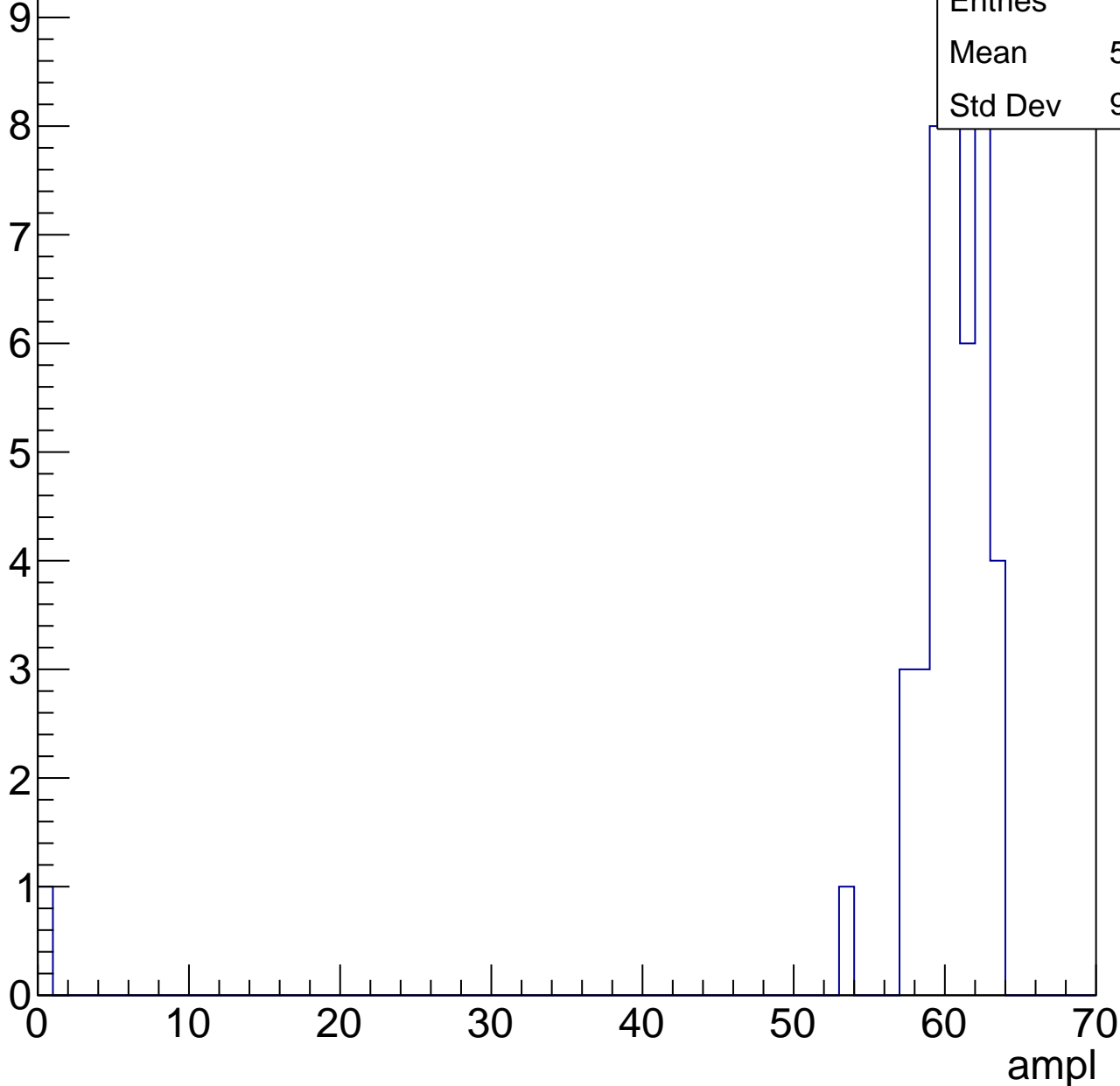


# B1L003S, U6-ch61, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	43
Mean	58.74
Std Dev	9.284

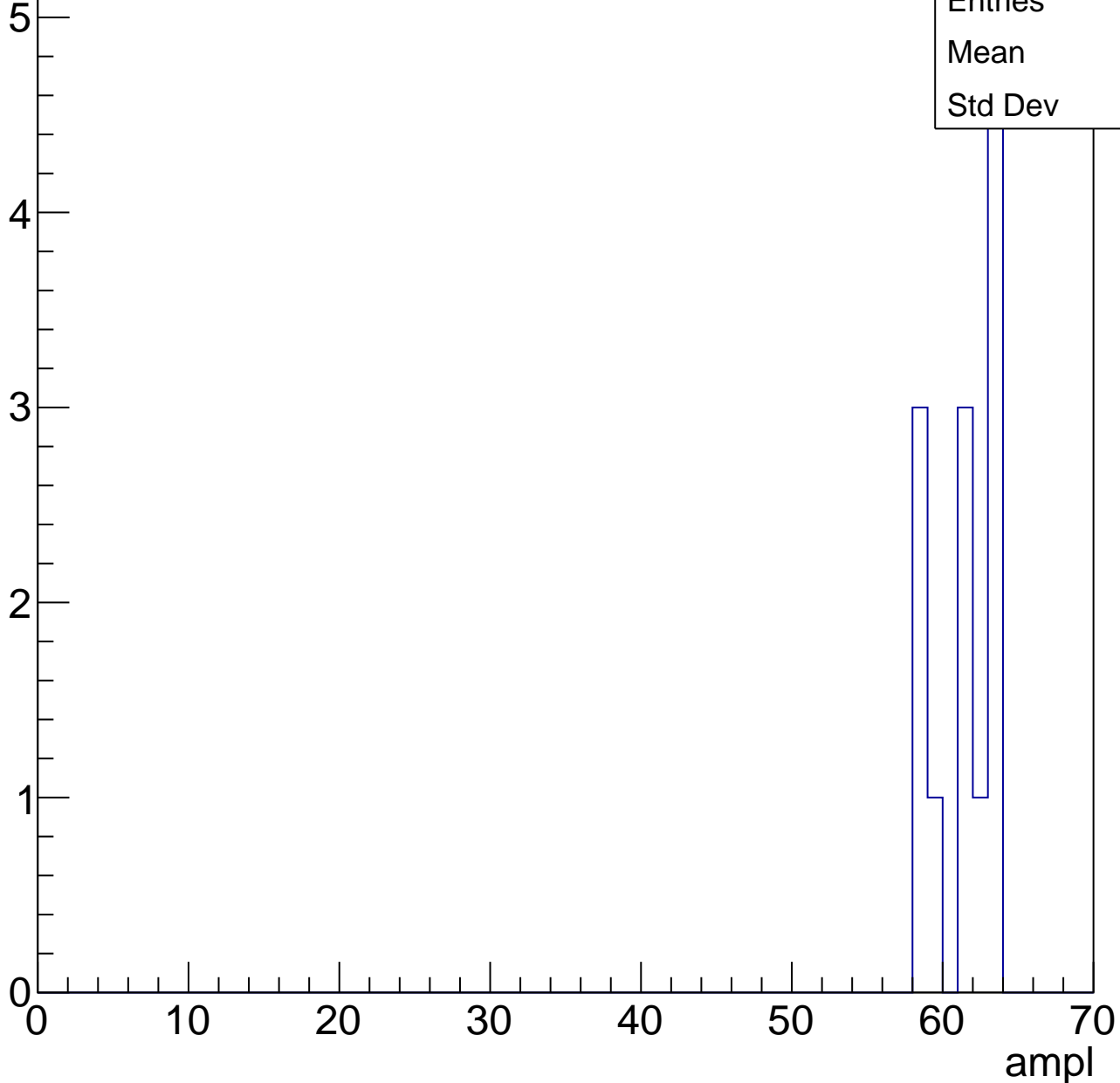


# B1L003S, U6-ch61, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	13
Mean	61
Std Dev	2





# B1L003S, U6-ch61, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch62, adc0

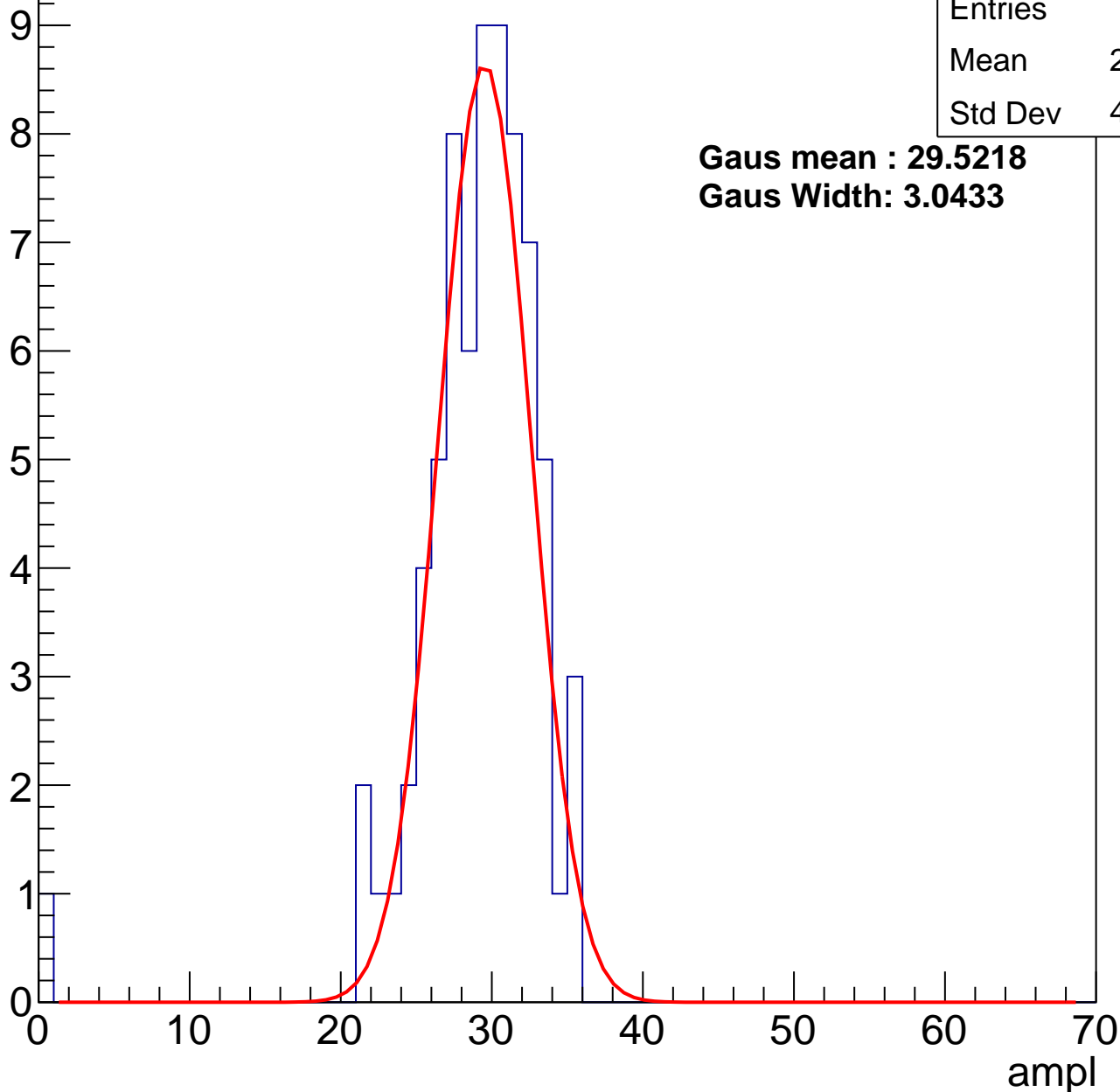
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	72
Mean	28.56
Std Dev	4.645

**Gaus mean : 29.5218**

**Gaus Width: 3.0433**



# B1L003S, U6-ch62, adc1

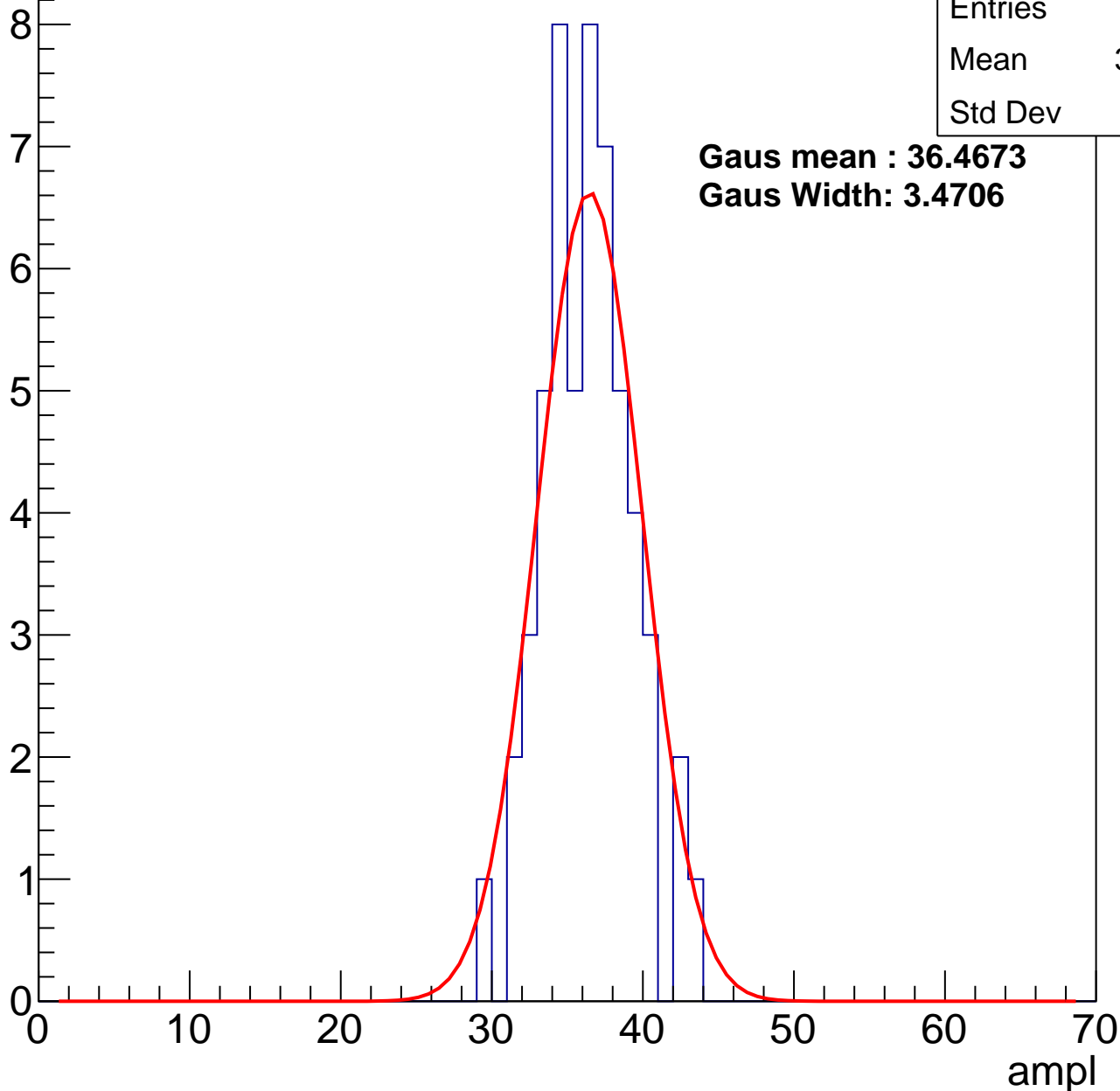
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	54
Mean	35.91
Std Dev	2.92

**Gaus mean : 36.4673**

**Gaus Width: 3.4706**



# B1L003S, U6-ch62, adc2

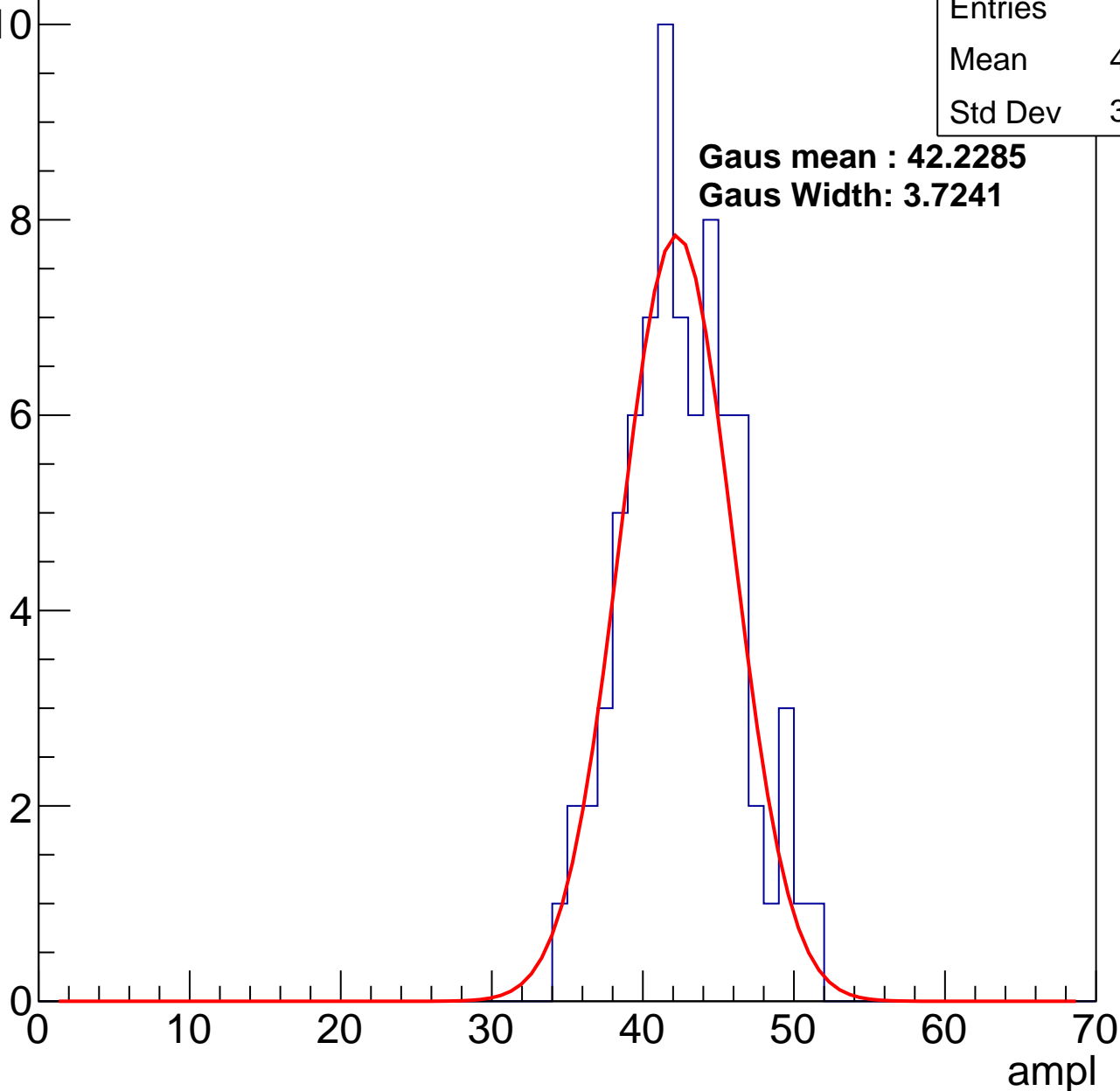
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	77
Mean	42.09
Std Dev	3.686

**Gaus mean : 42.2285**

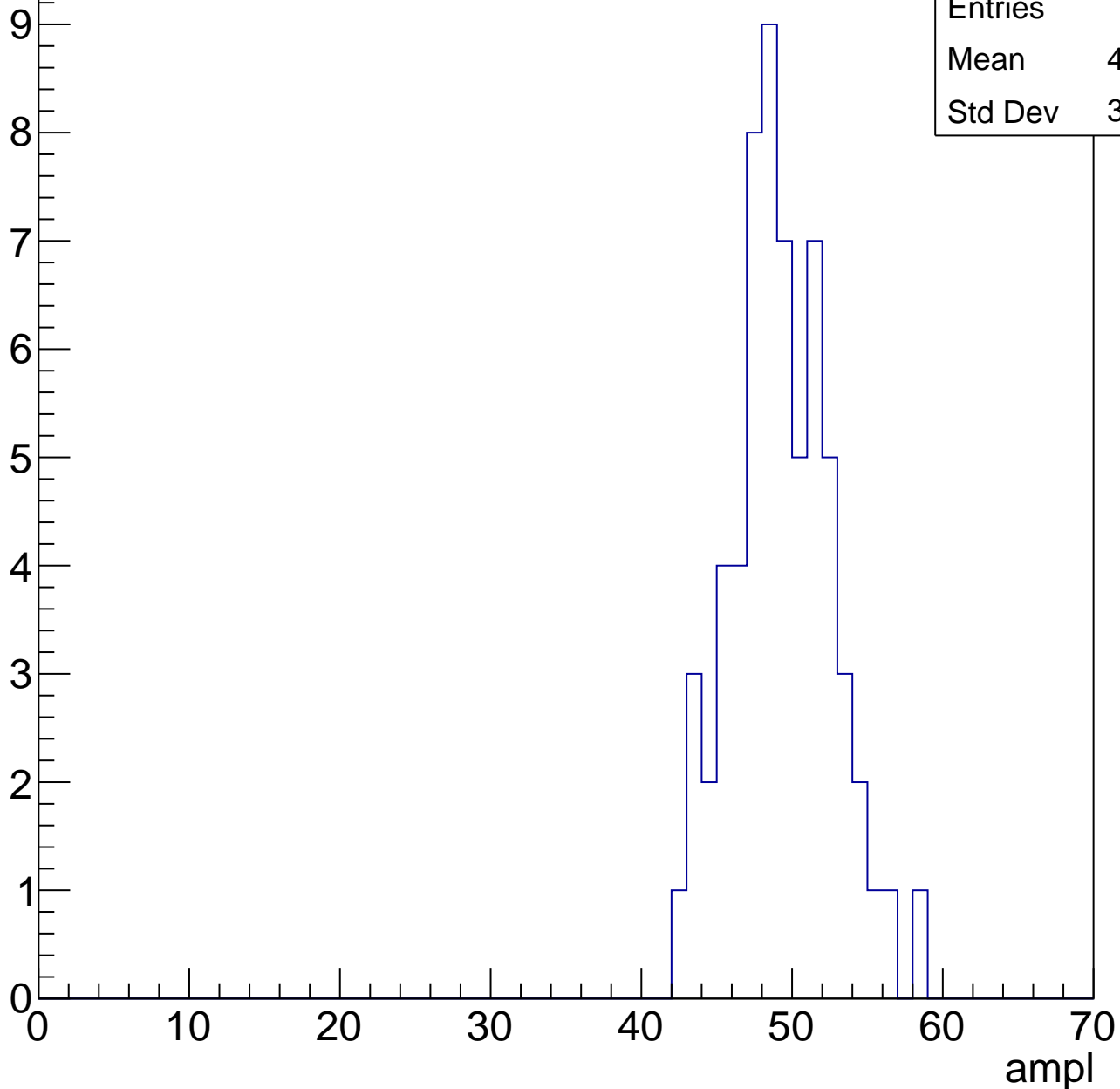
**Gaus Width: 3.7241**



# B1L003S, U6-ch62, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

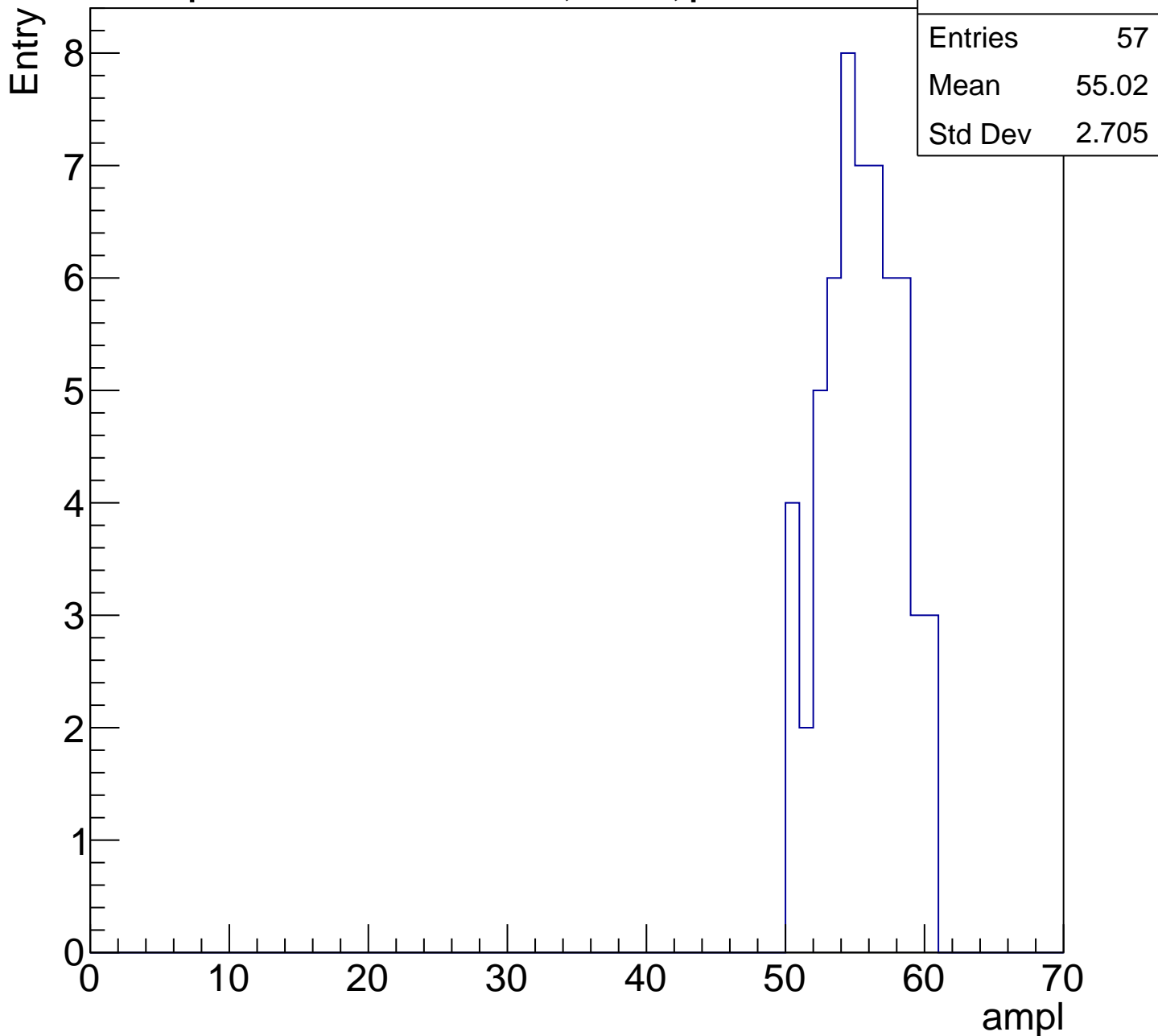
Entry



Entries	63
Mean	48.84
Std Dev	3.306

# B1L003S, U6-ch62, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

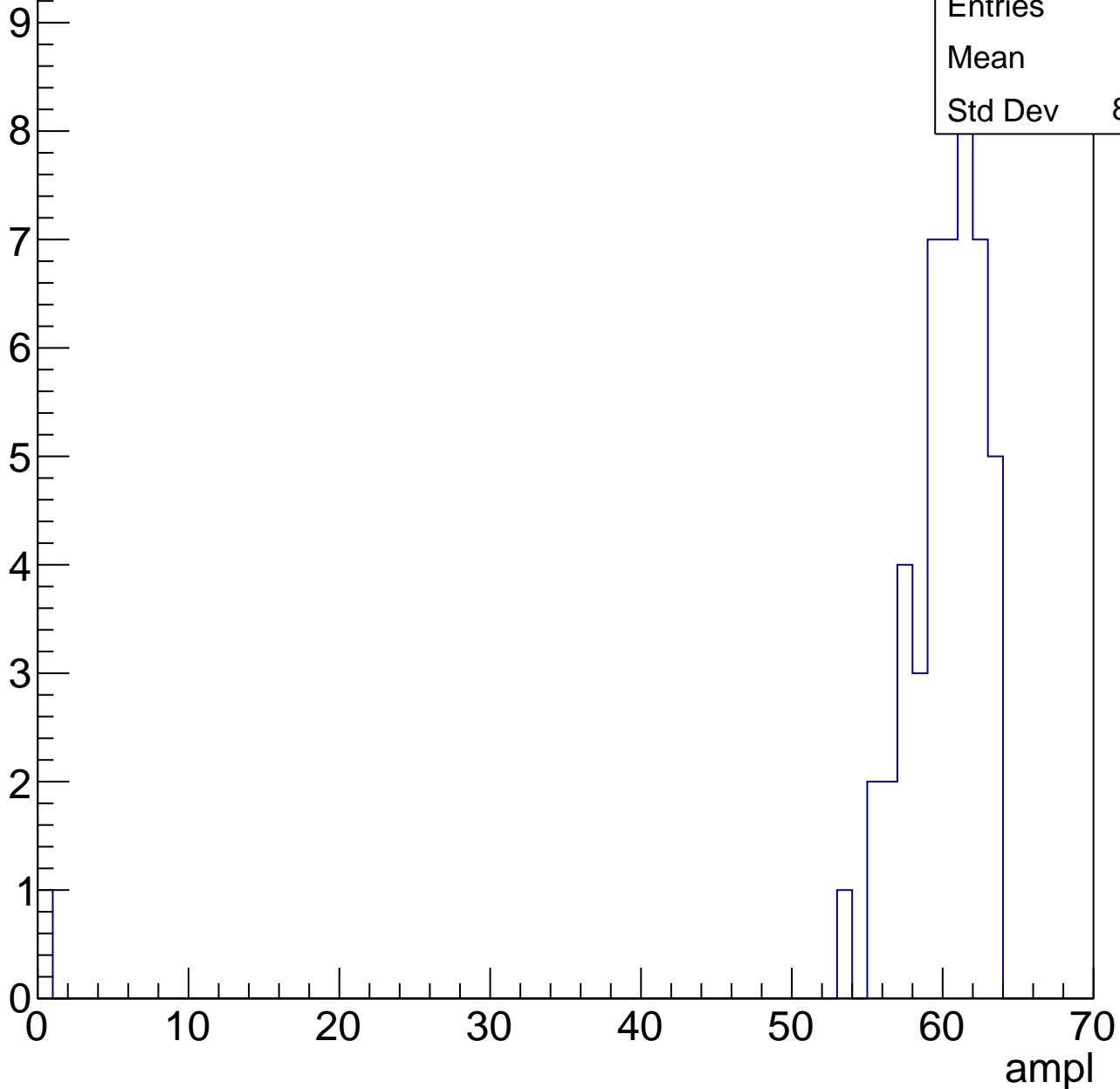


# B1L003S, U6-ch62, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

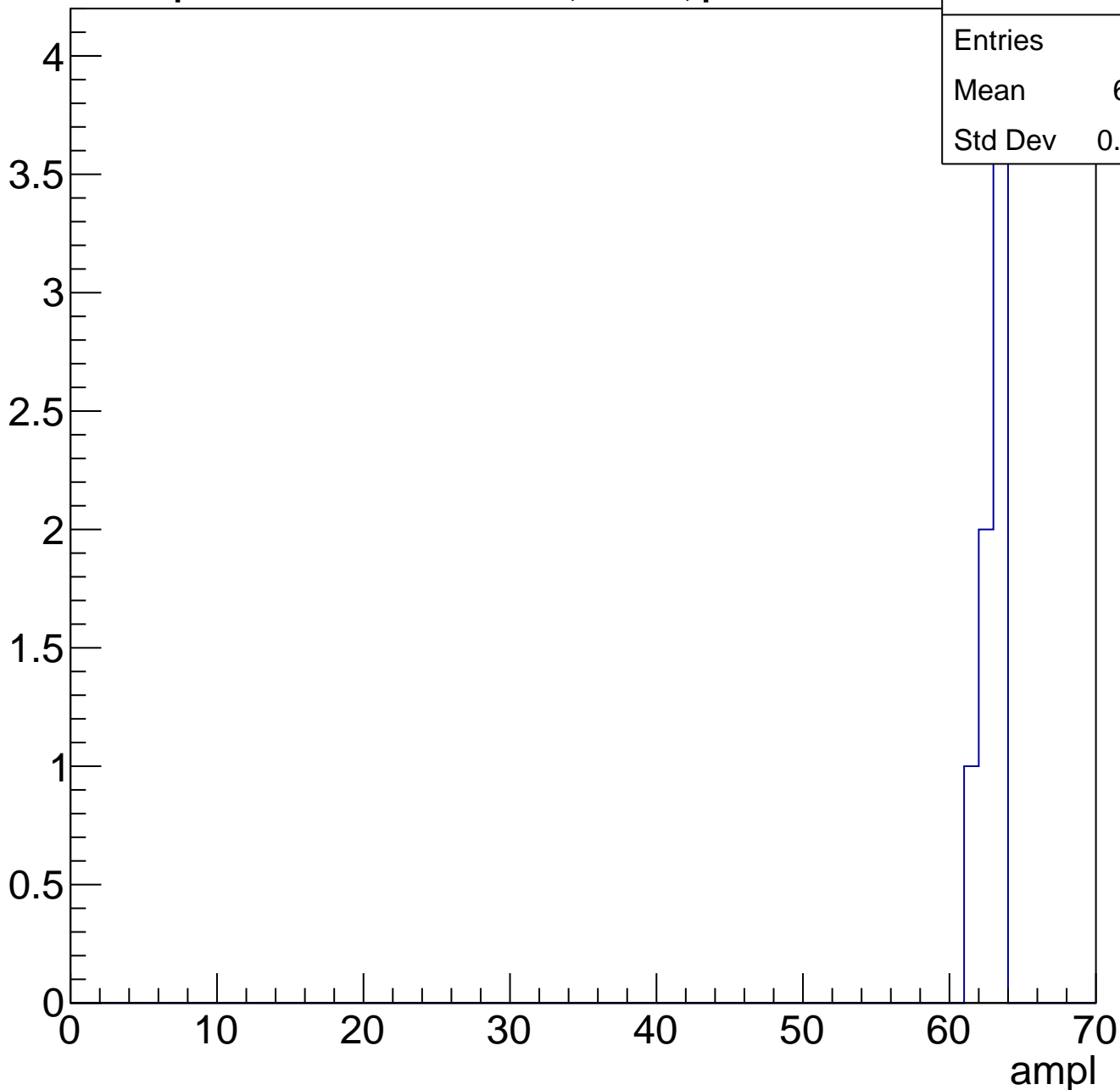
Entries	48
Mean	58.5
Std Dev	8.851



# B1L003S, U6-ch62, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

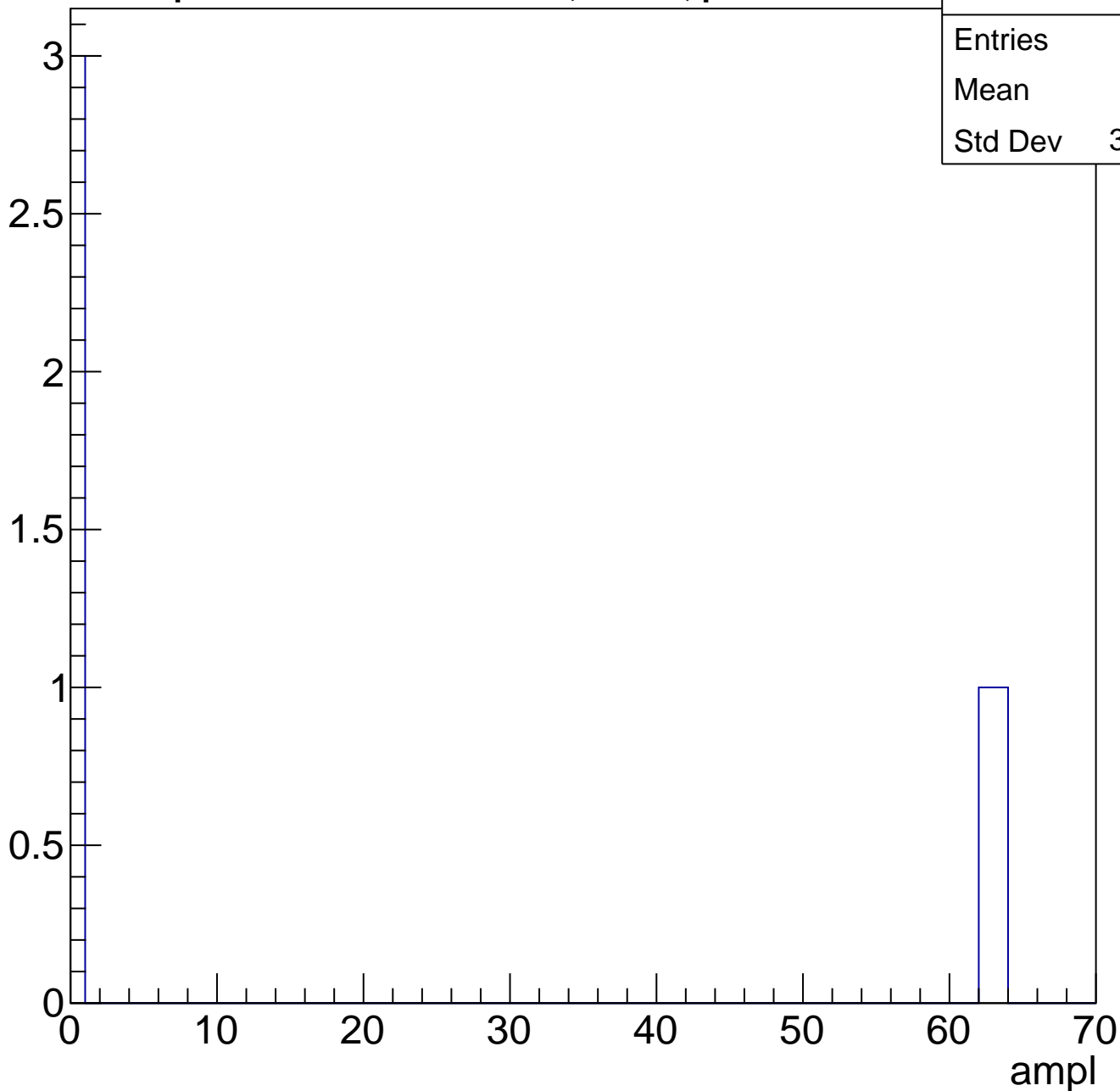




# B1L003S, U6-ch62, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch63, adc0

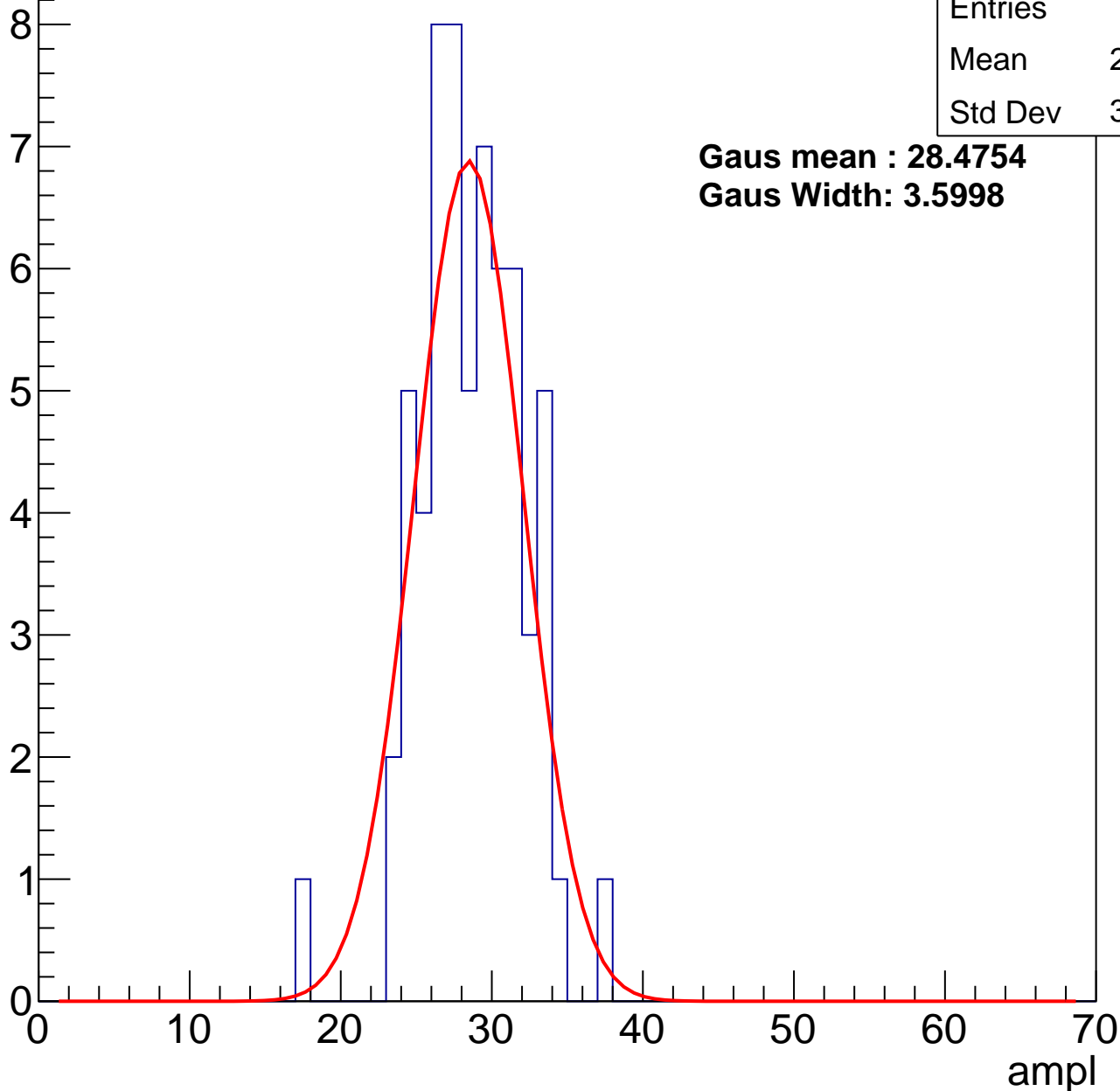
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	28.19
Std Dev	3.359

**Gaus mean : 28.4754**

**Gaus Width: 3.5998**



# B1L003S, U6-ch63, adc1

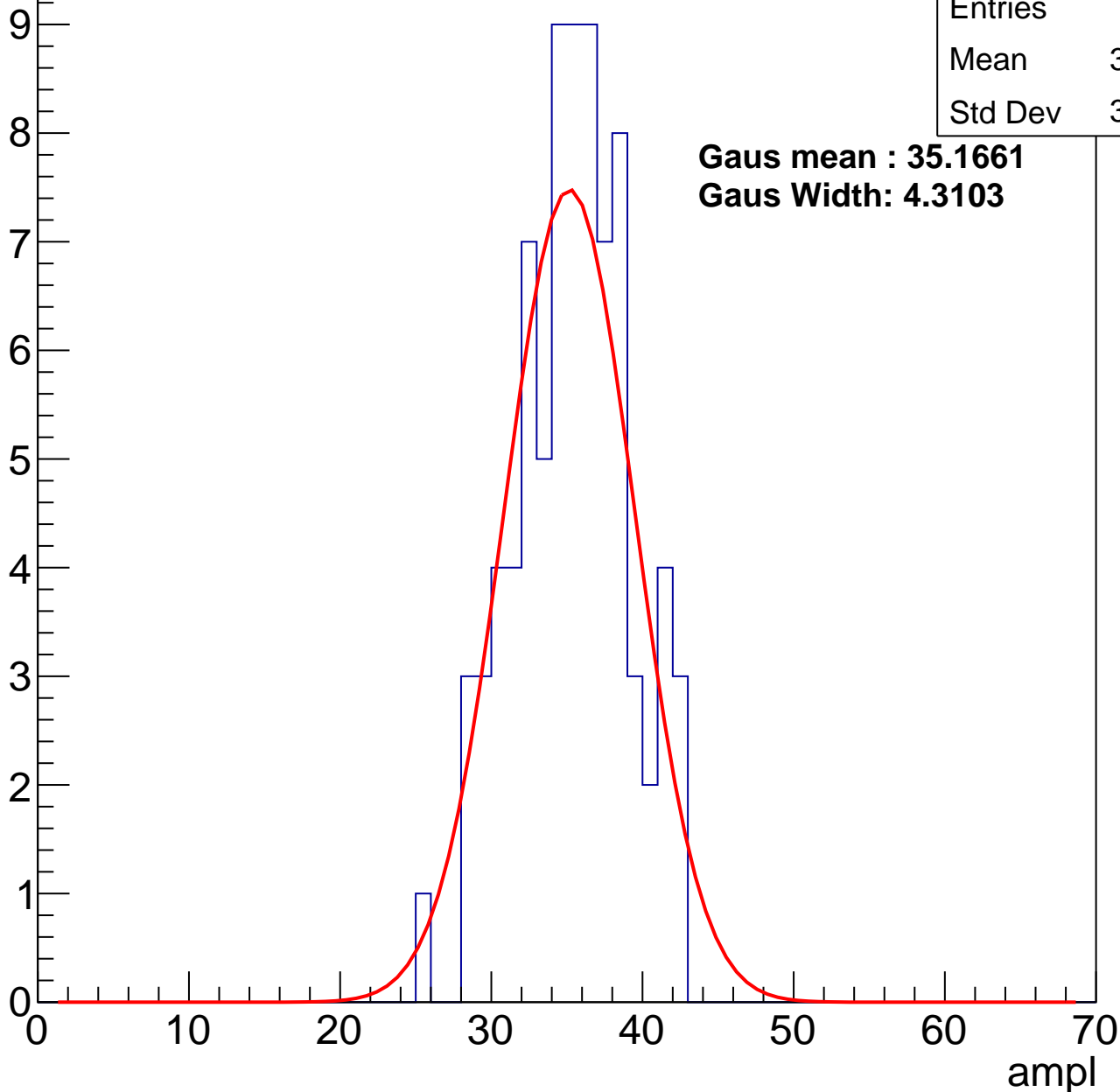
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	81
Mean	34.86
Std Dev	3.698

**Gaus mean : 35.1661**

**Gaus Width: 4.3103**



# B1L003S, U6-ch63, adc2

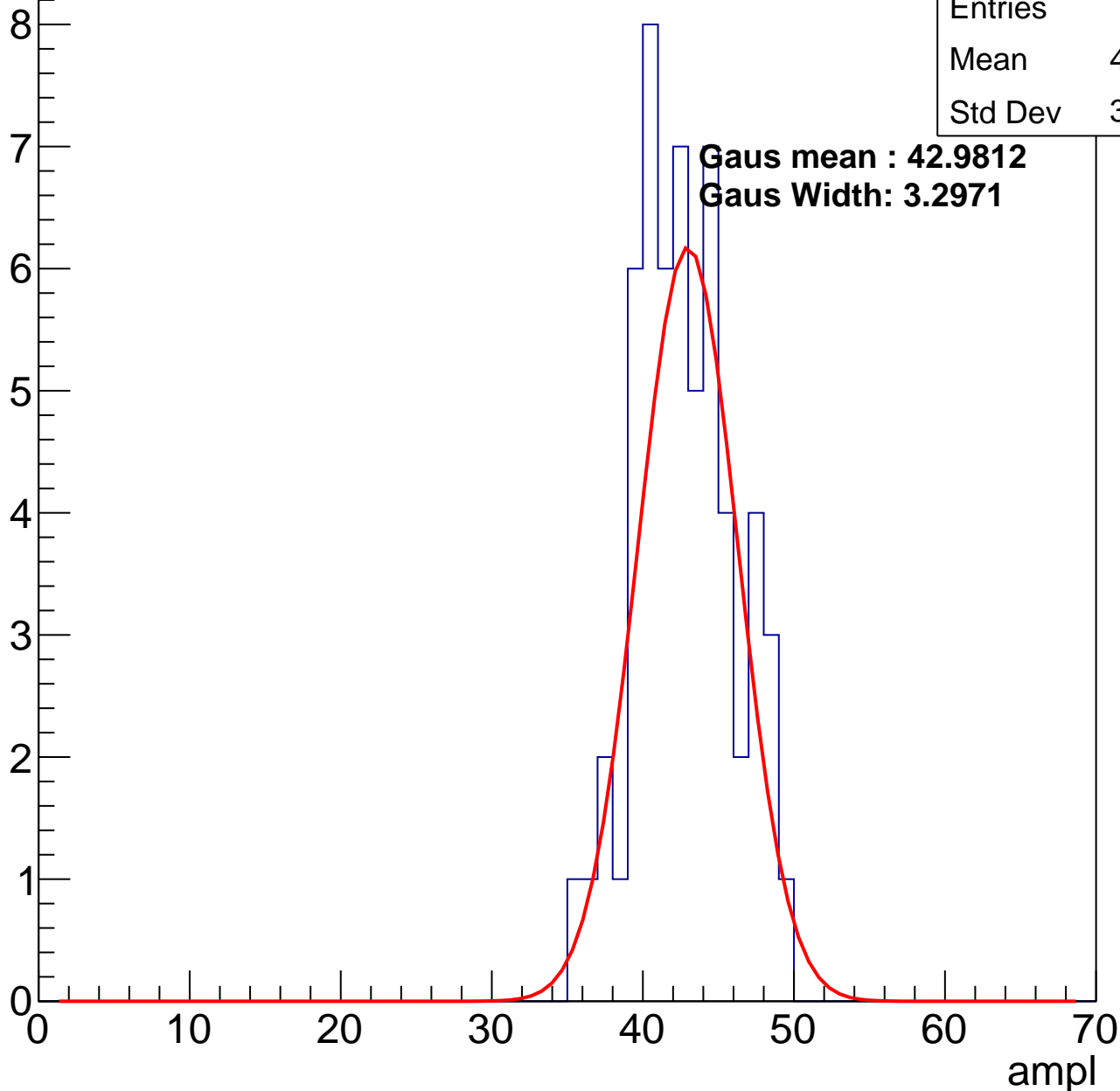
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	42.29
Std Dev	3.206

**Gaus mean : 42.9812**

**Gaus Width: 3.2971**

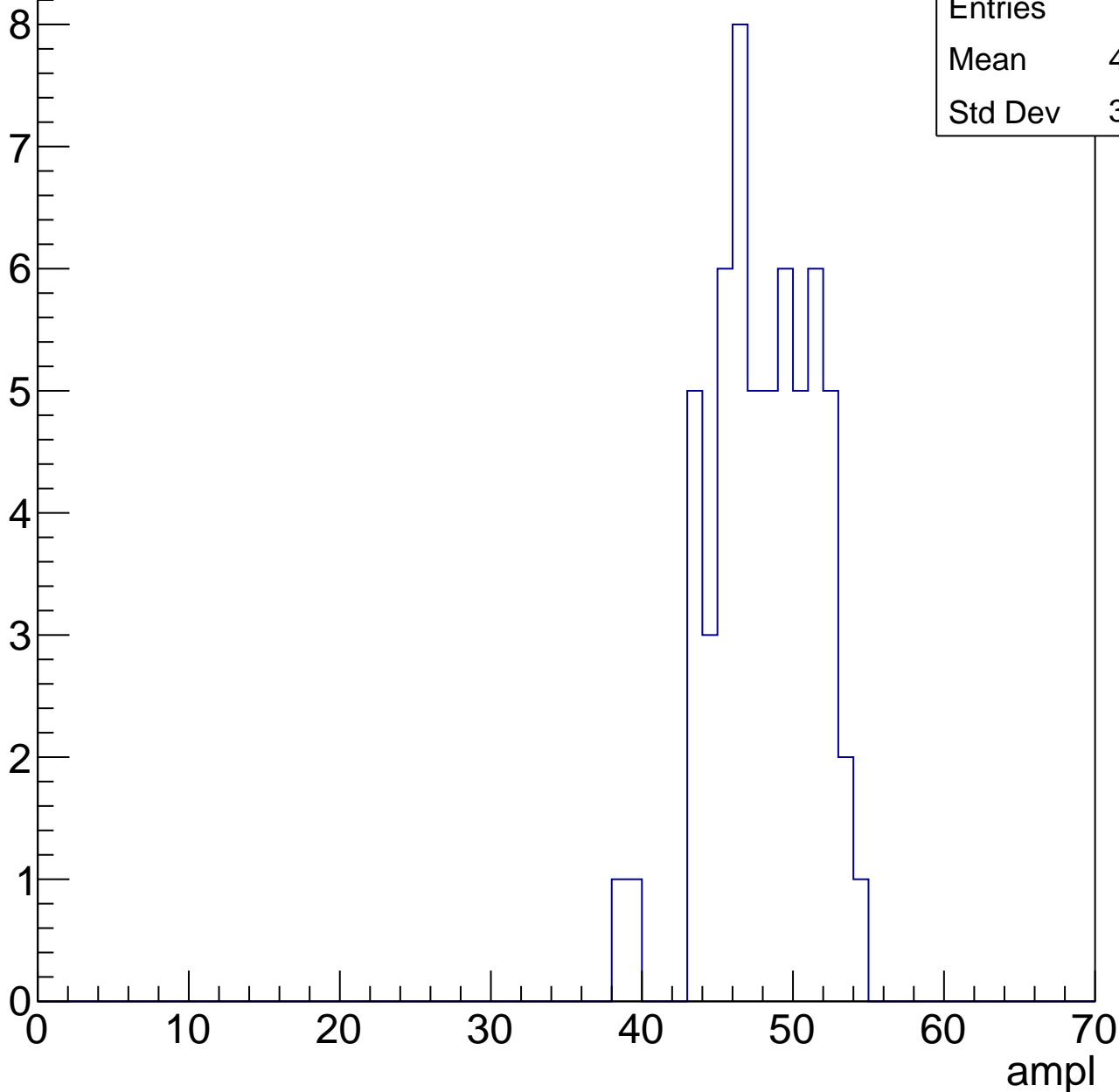


# B1L003S, U6-ch63, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	47.58
Std Dev	3.396



# B1L003S, U6-ch63, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

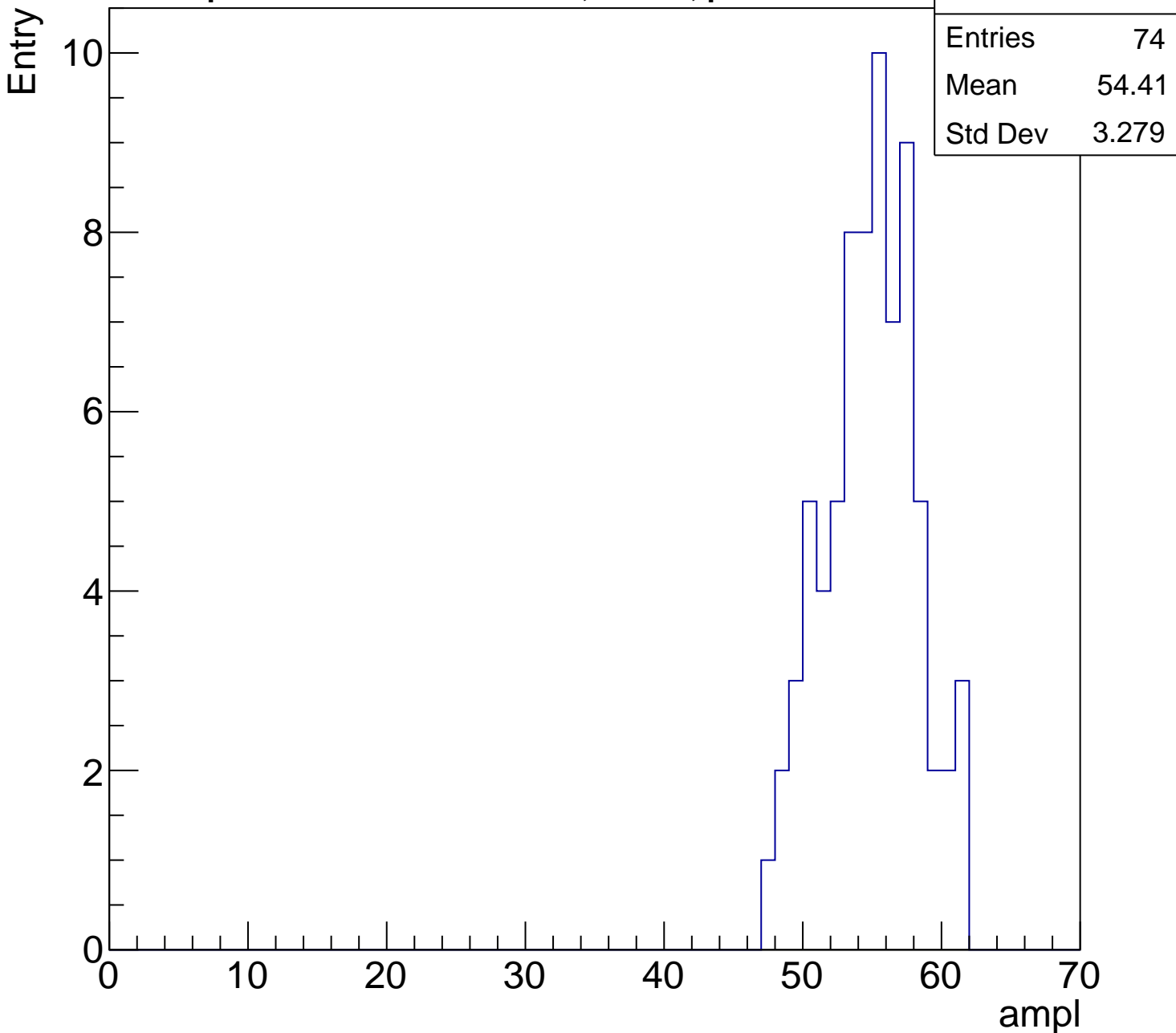
Entries	74
Mean	54.41
Std Dev	3.279

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

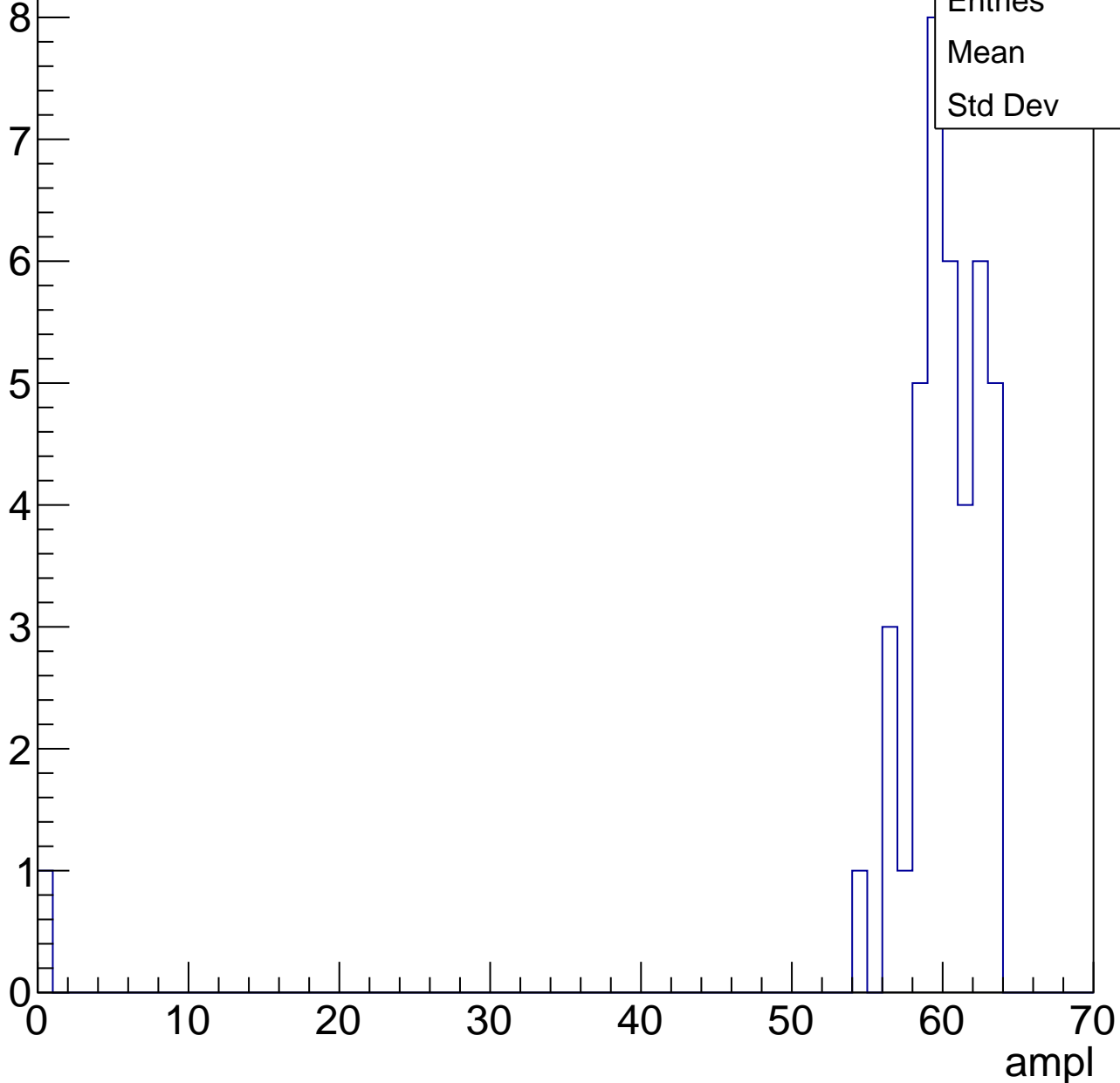


# B1L003S, U6-ch63, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	40
Mean	58.3
Std Dev	9.59

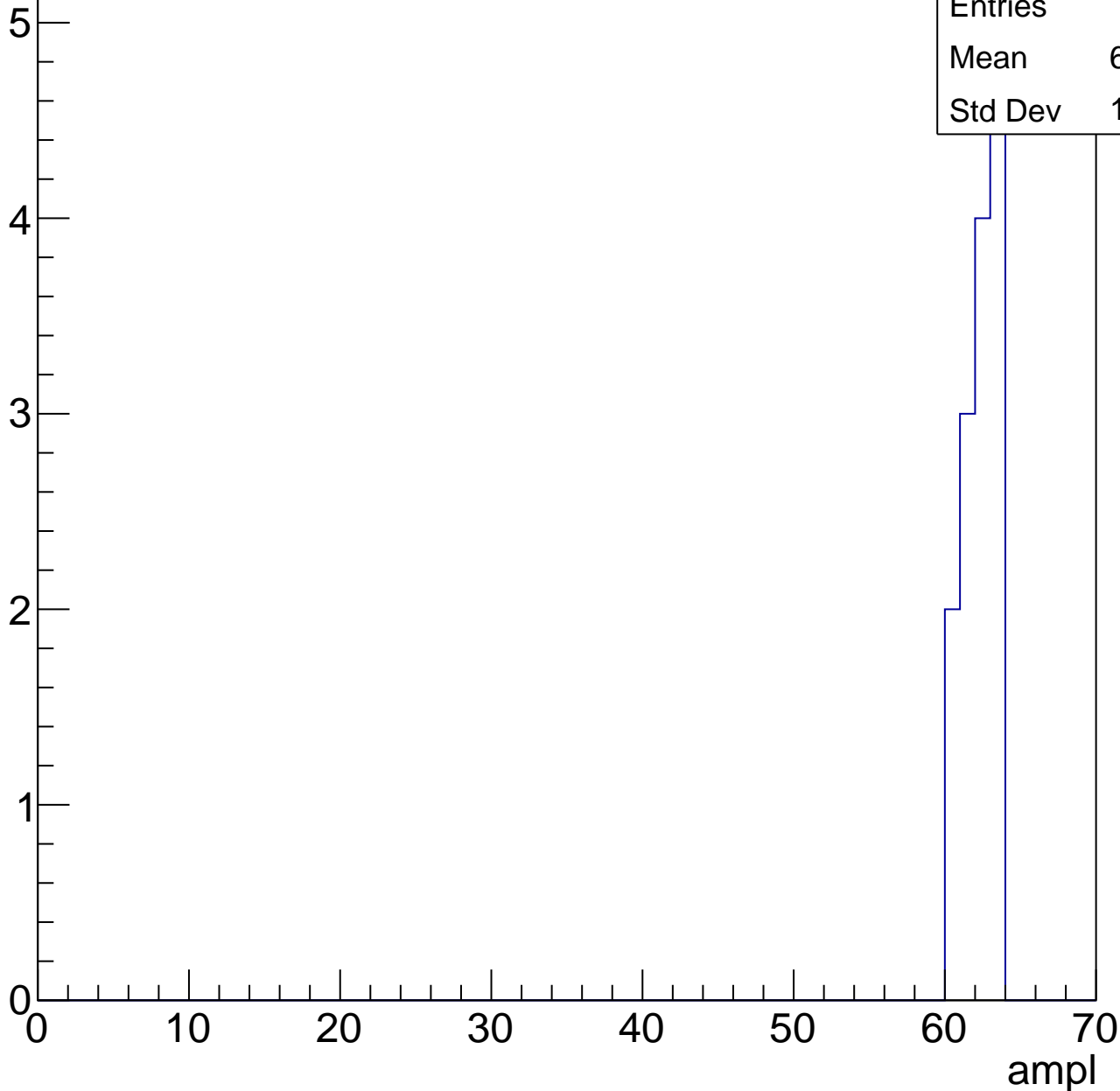


# B1L003S, U6-ch63, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	14
Mean	61.86
Std Dev	1.059





# B1L003S, U6-ch63, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U6-ch64, adc0

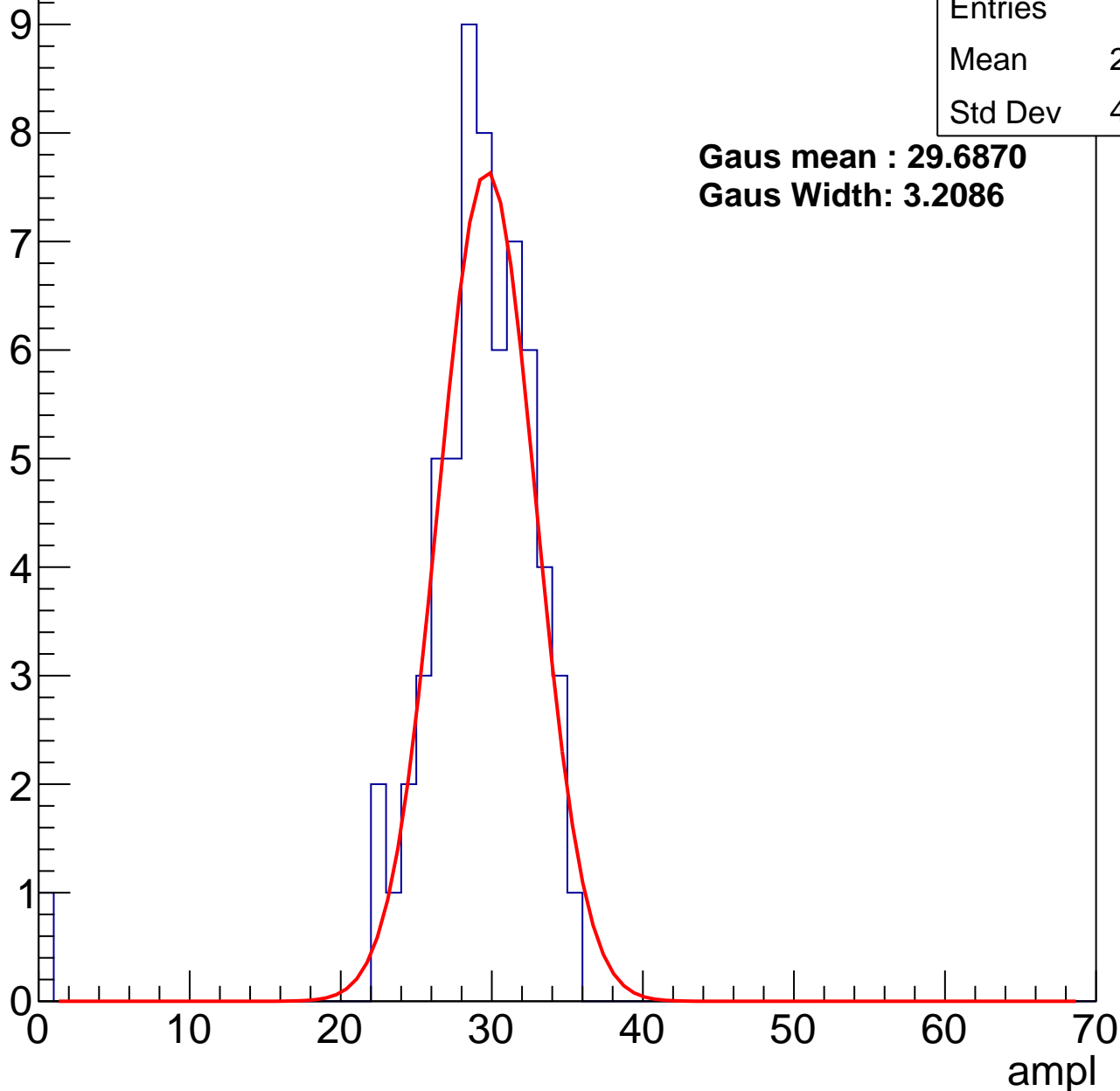
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	28.52
Std Dev	4.707

**Gaus mean : 29.6870**

**Gaus Width: 3.2086**



# B1L003S, U6-ch64, adc1

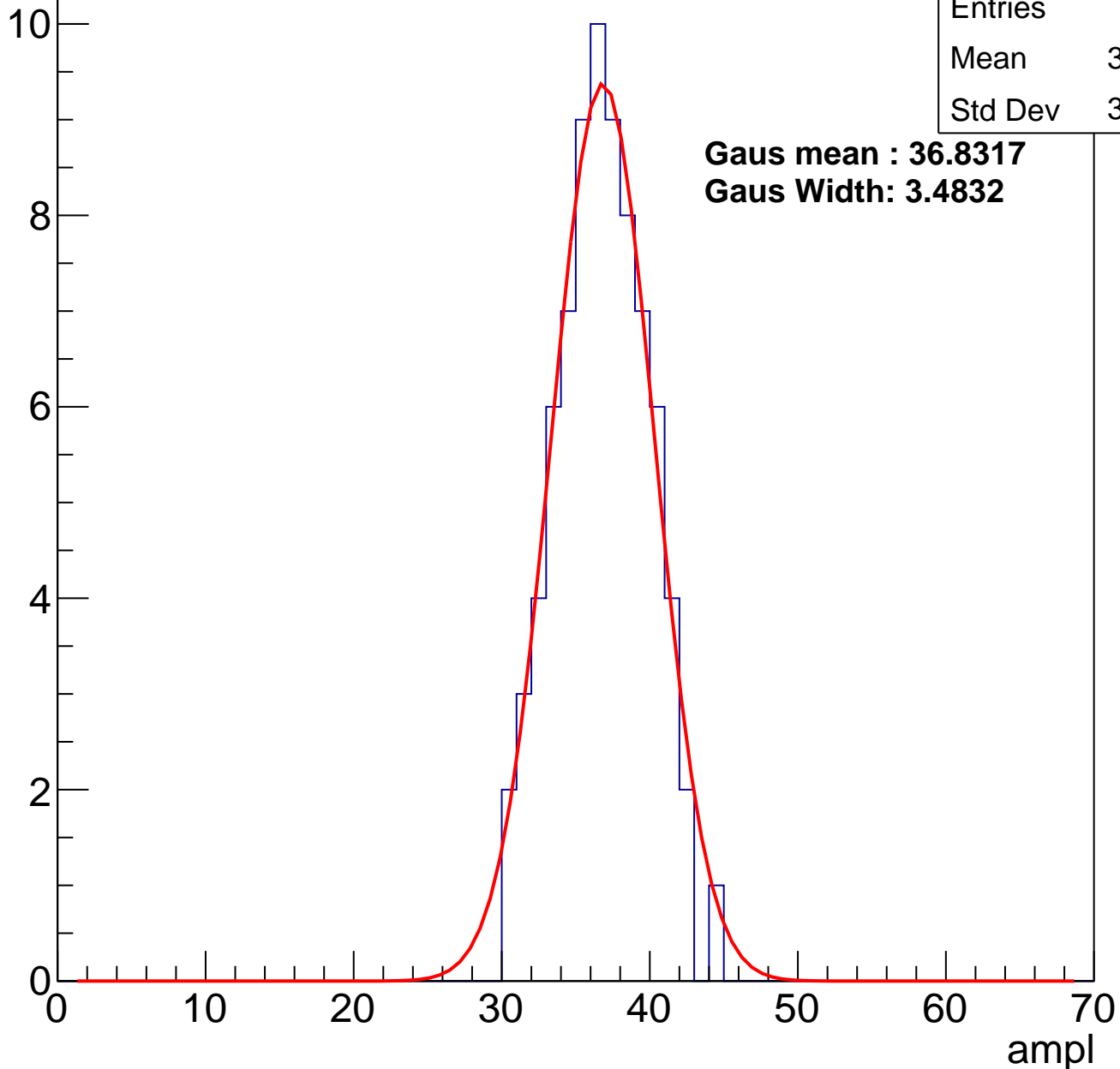
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	78
Mean	36.33
Std Dev	3.058

**Gaus mean : 36.8317**

**Gaus Width: 3.4832**

Entry



# B1L003S, U6-ch64, adc2

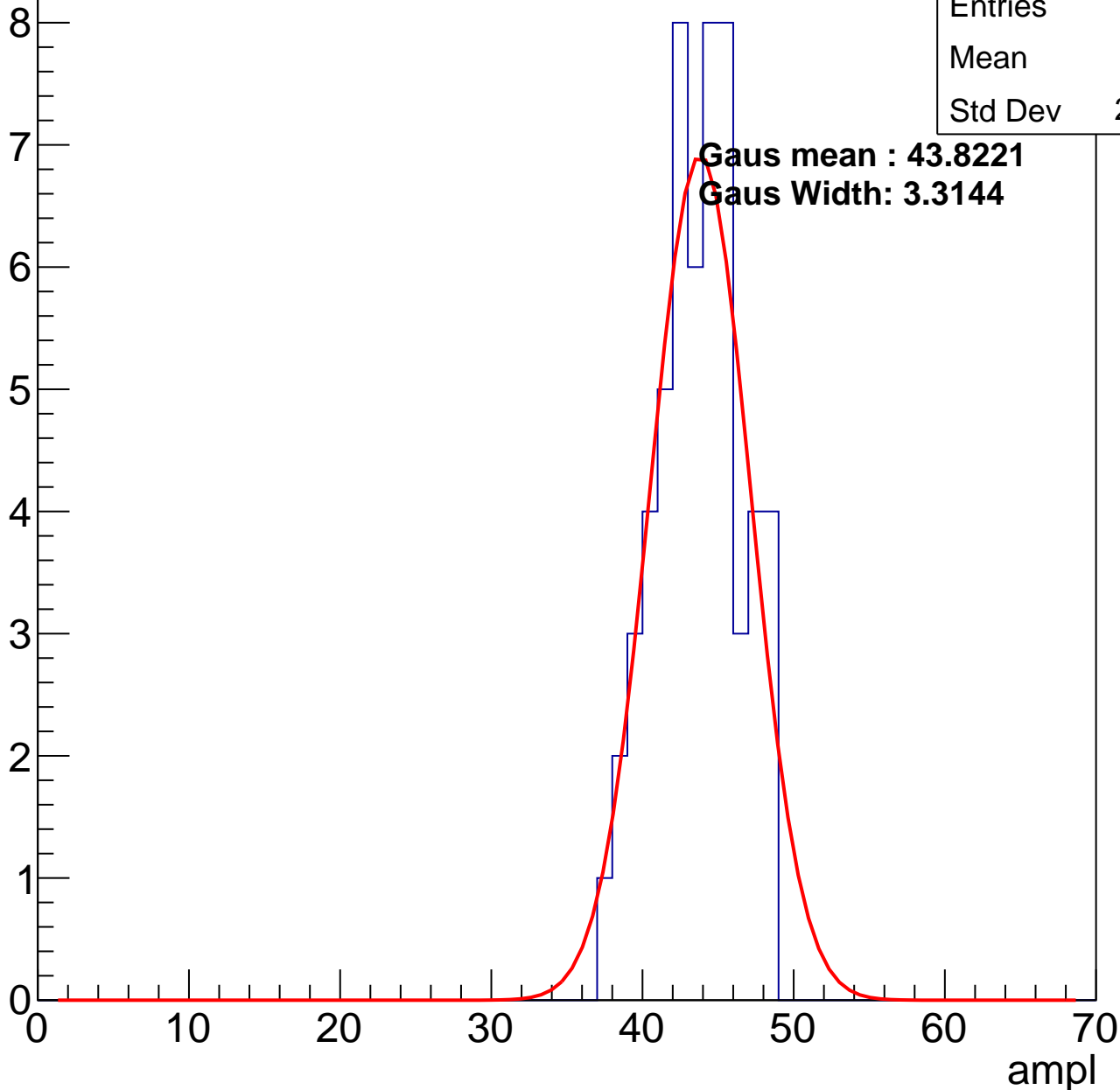
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	43.2
Std Dev	2.761

**Gaus mean : 43.8221**

**Gaus Width: 3.3144**

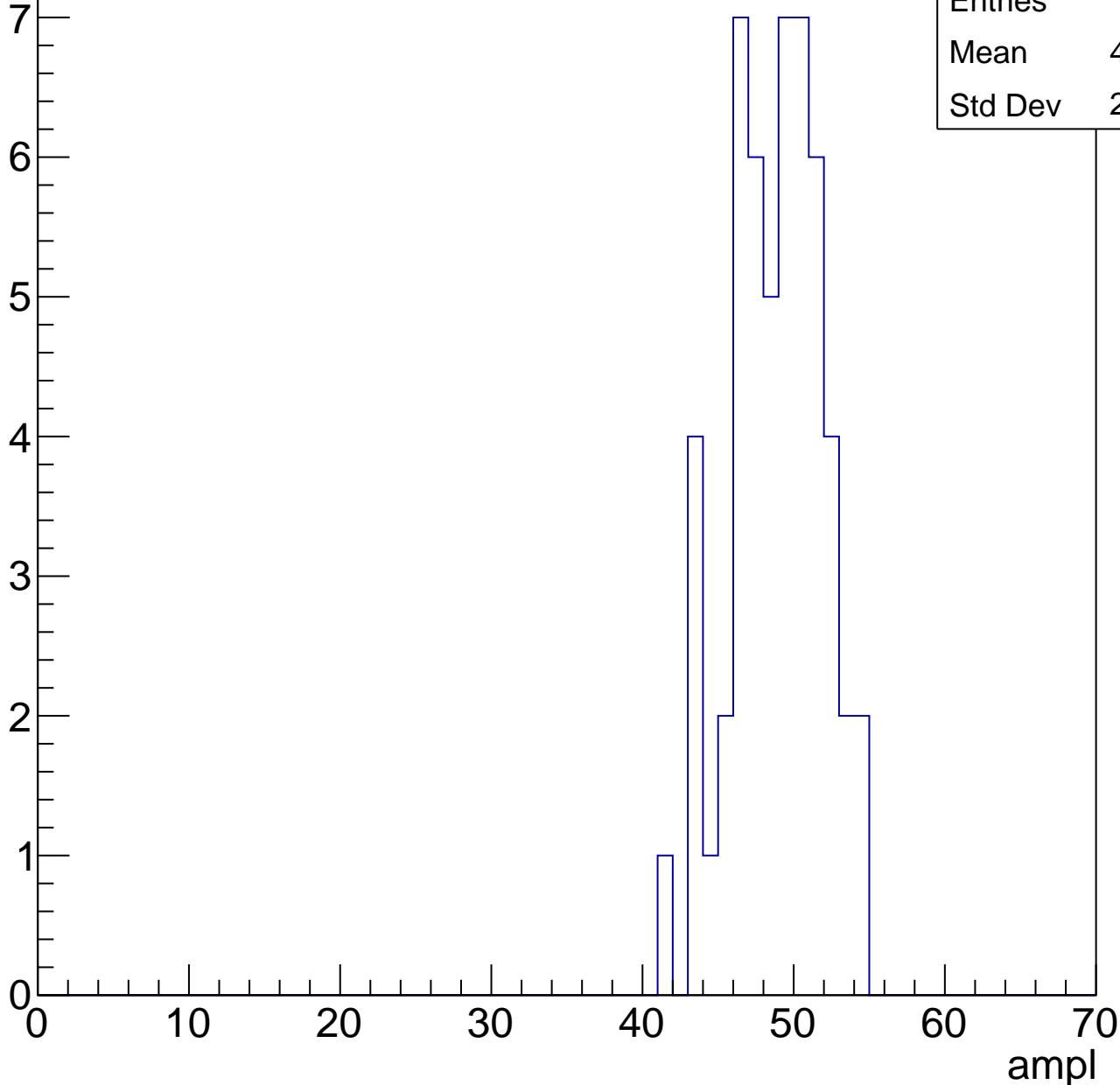


# B1L003S, U6-ch64, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

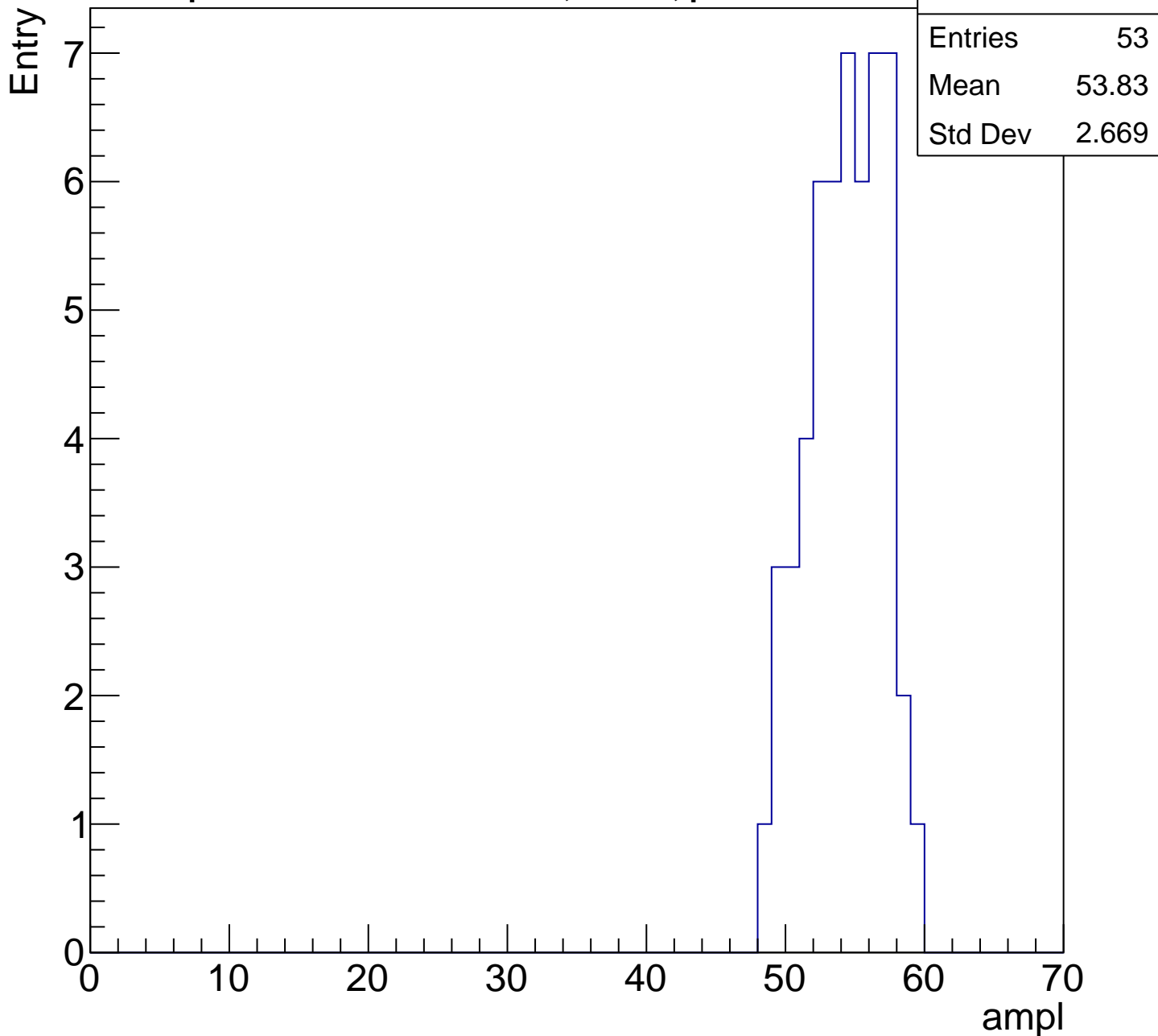
Entry

Entries	54
Mean	48.37
Std Dev	2.996



# B1L003S, U6-ch64, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2



# B1L003S, U6-ch64, adc5

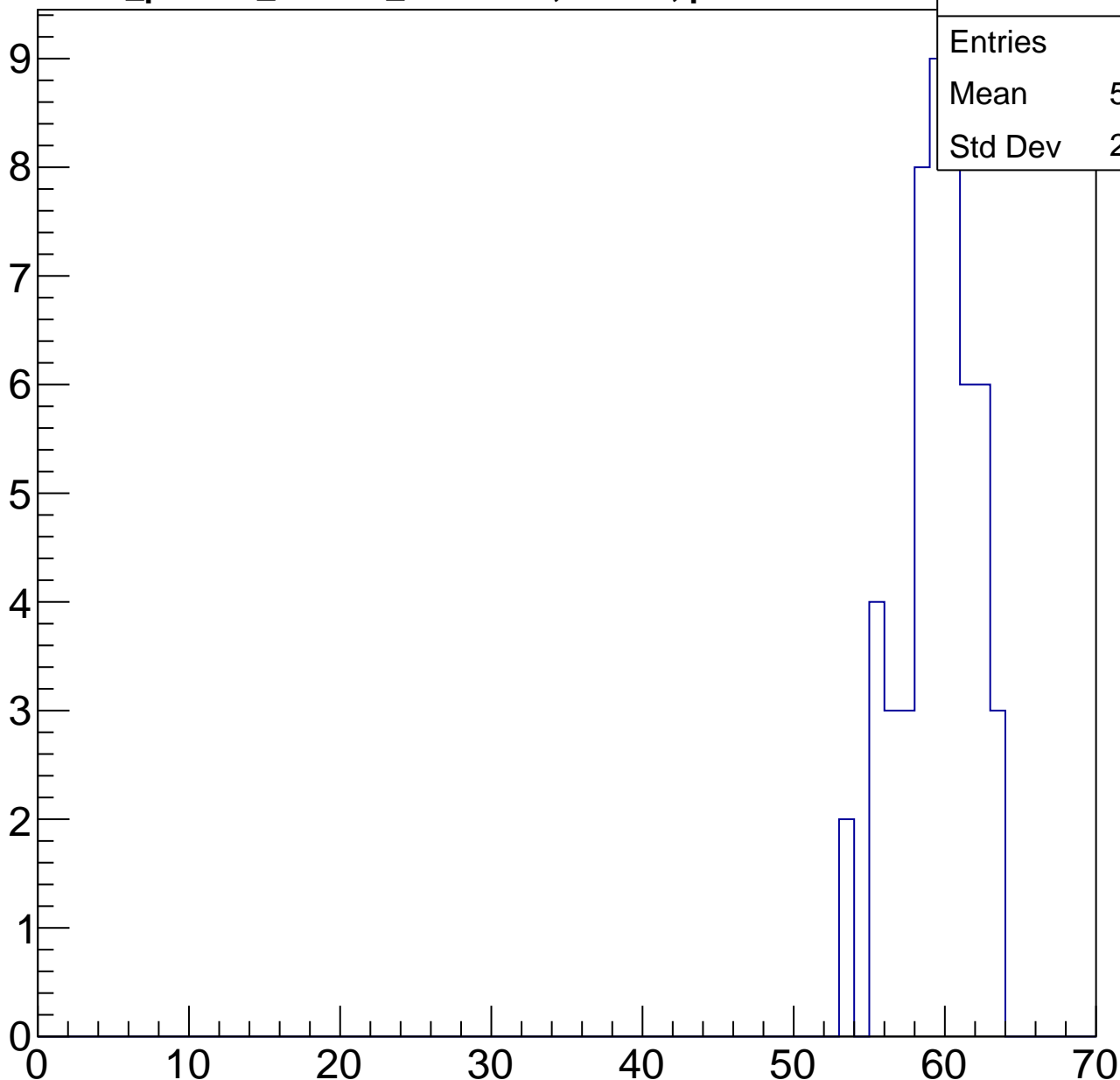
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	52
Mean	58.98
Std Dev	2.469

ampl

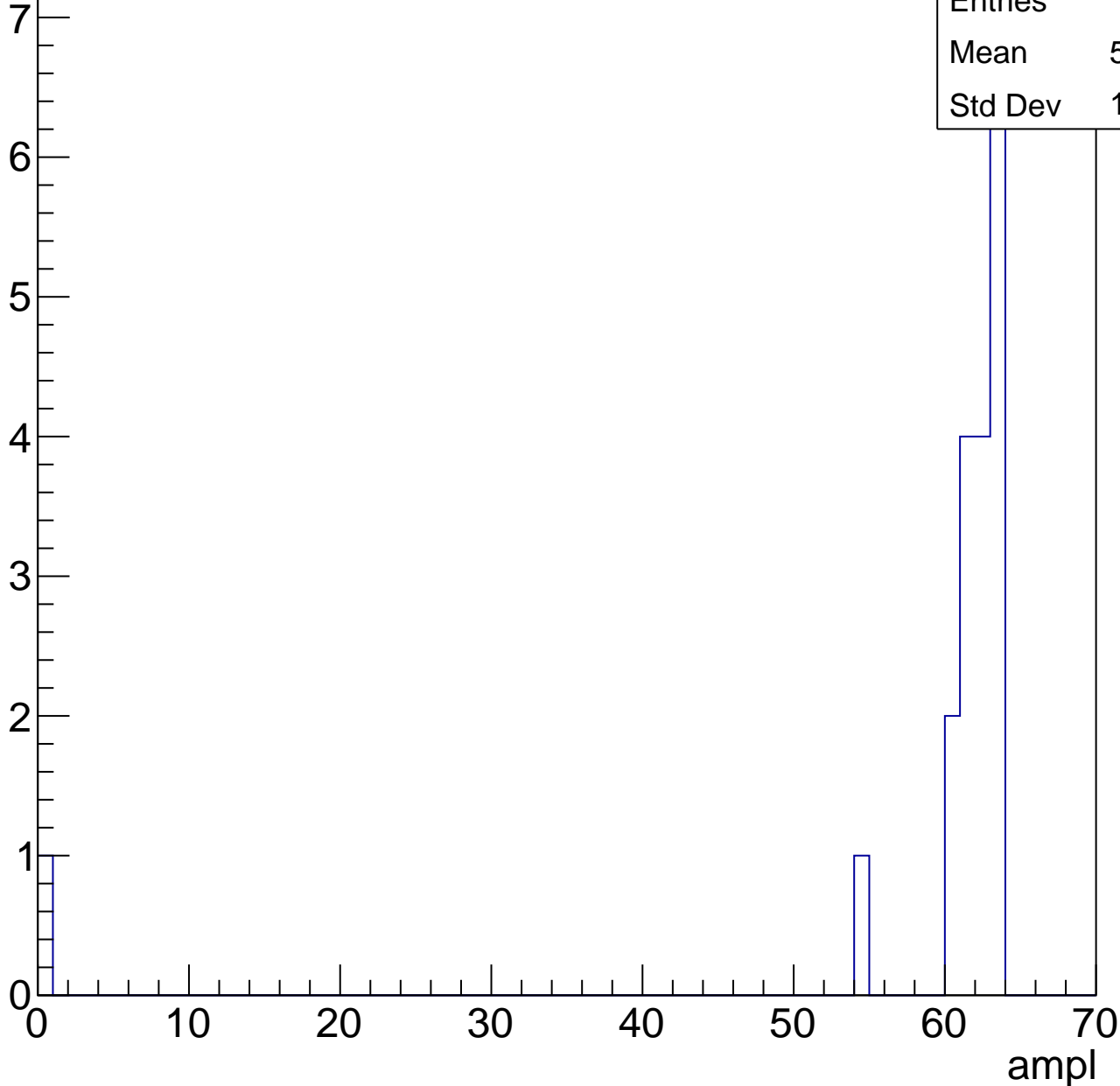


# B1L003S, U6-ch64, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	19
Mean	58.26
Std Dev	13.88





# B1L003S, U6-ch64, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U6-ch65, adc0

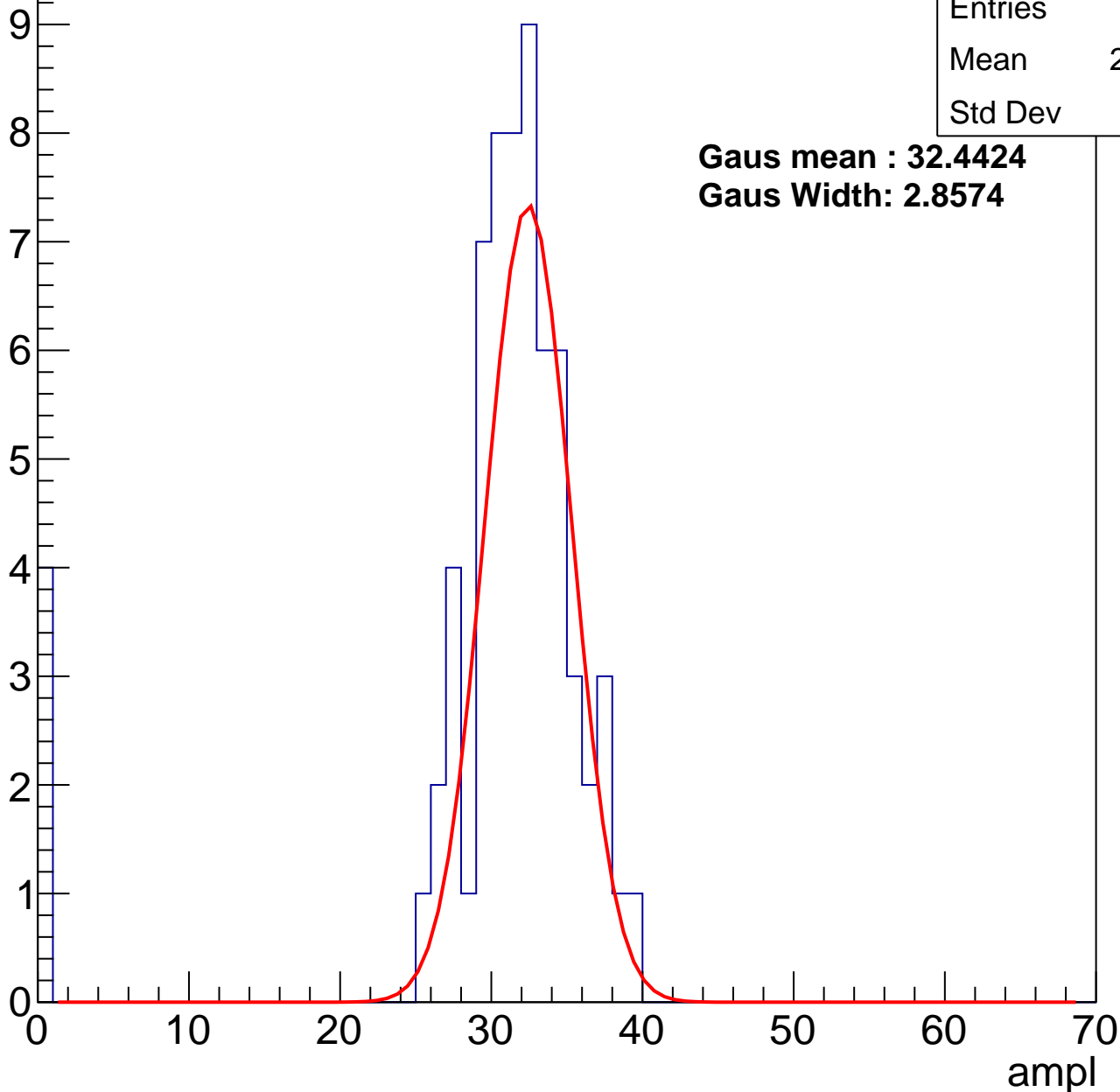
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	29.68
Std Dev	8.1

**Gaus mean : 32.4424**

**Gaus Width: 2.8574**



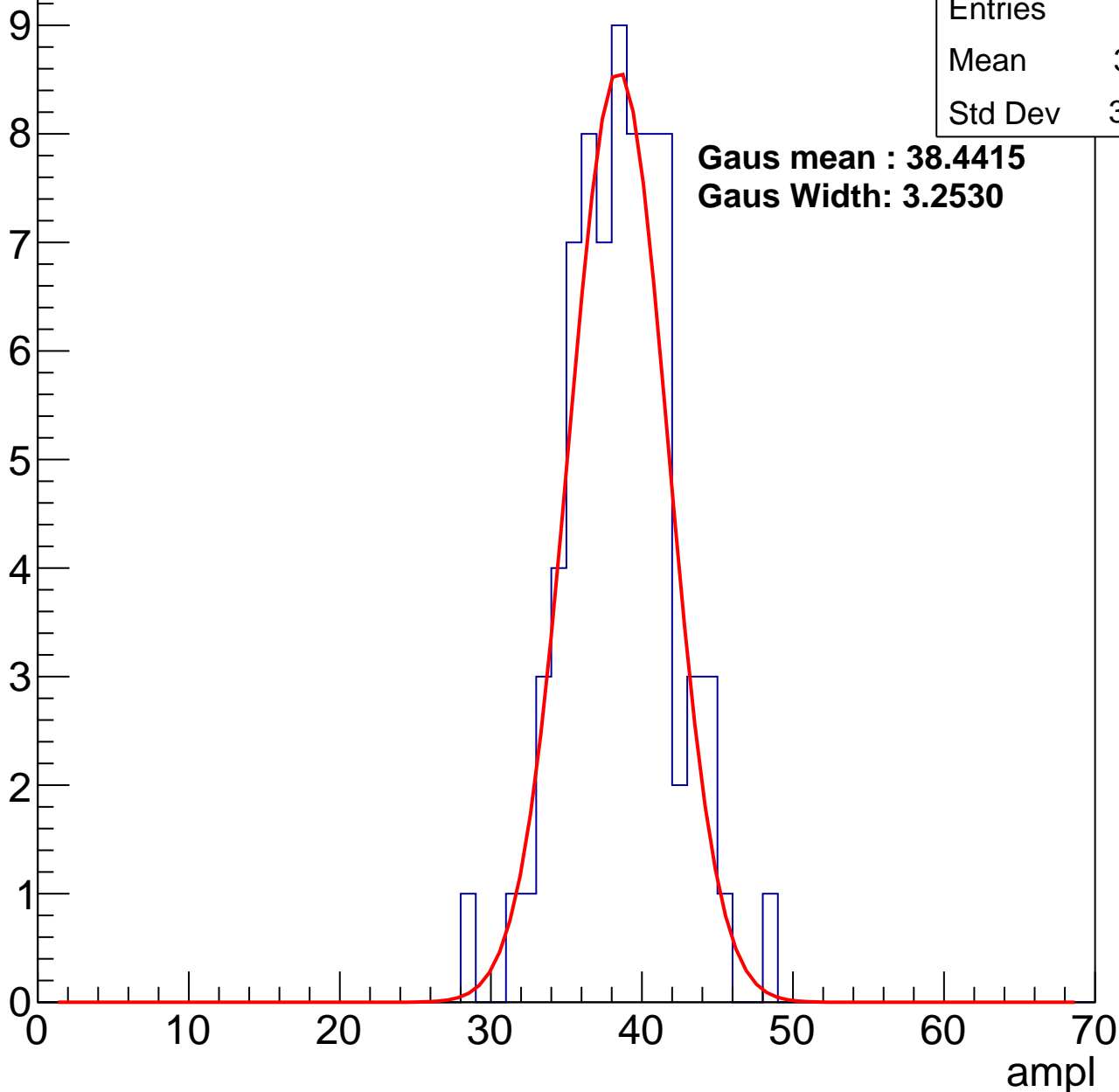
# B1L003S, U6-ch65, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	75
Mean	38.11
Std Dev	3.466

**Gaus mean : 38.4415**  
**Gaus Width: 3.2530**



# B1L003S, U6-ch65, adc2

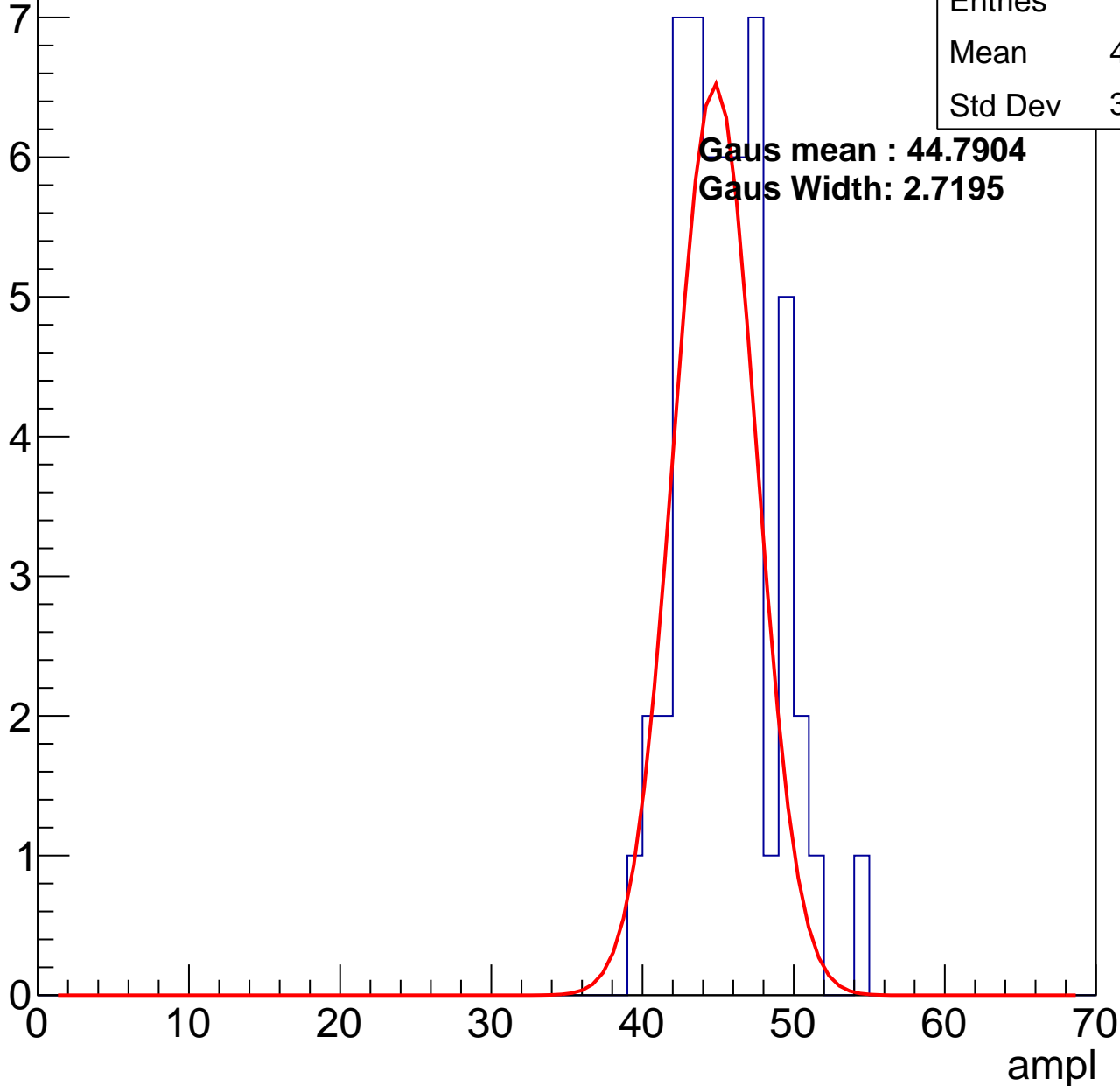
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	54
Mean	45.06
Std Dev	3.058

**Gaus mean : 44.7904**

**Gaus Width: 2.7195**

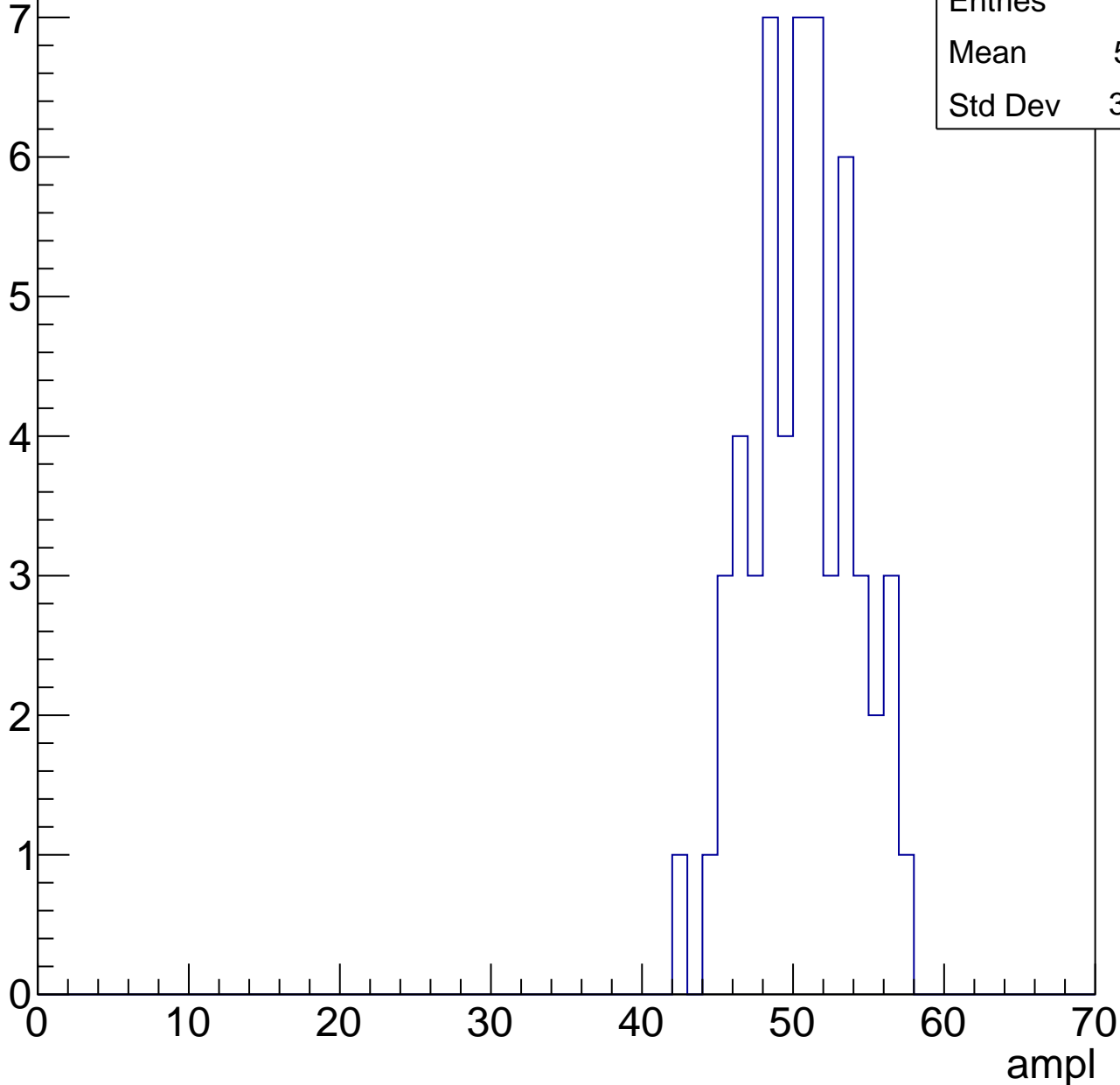


# B1L003S, U6-ch65, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	50.11
Std Dev	3.372

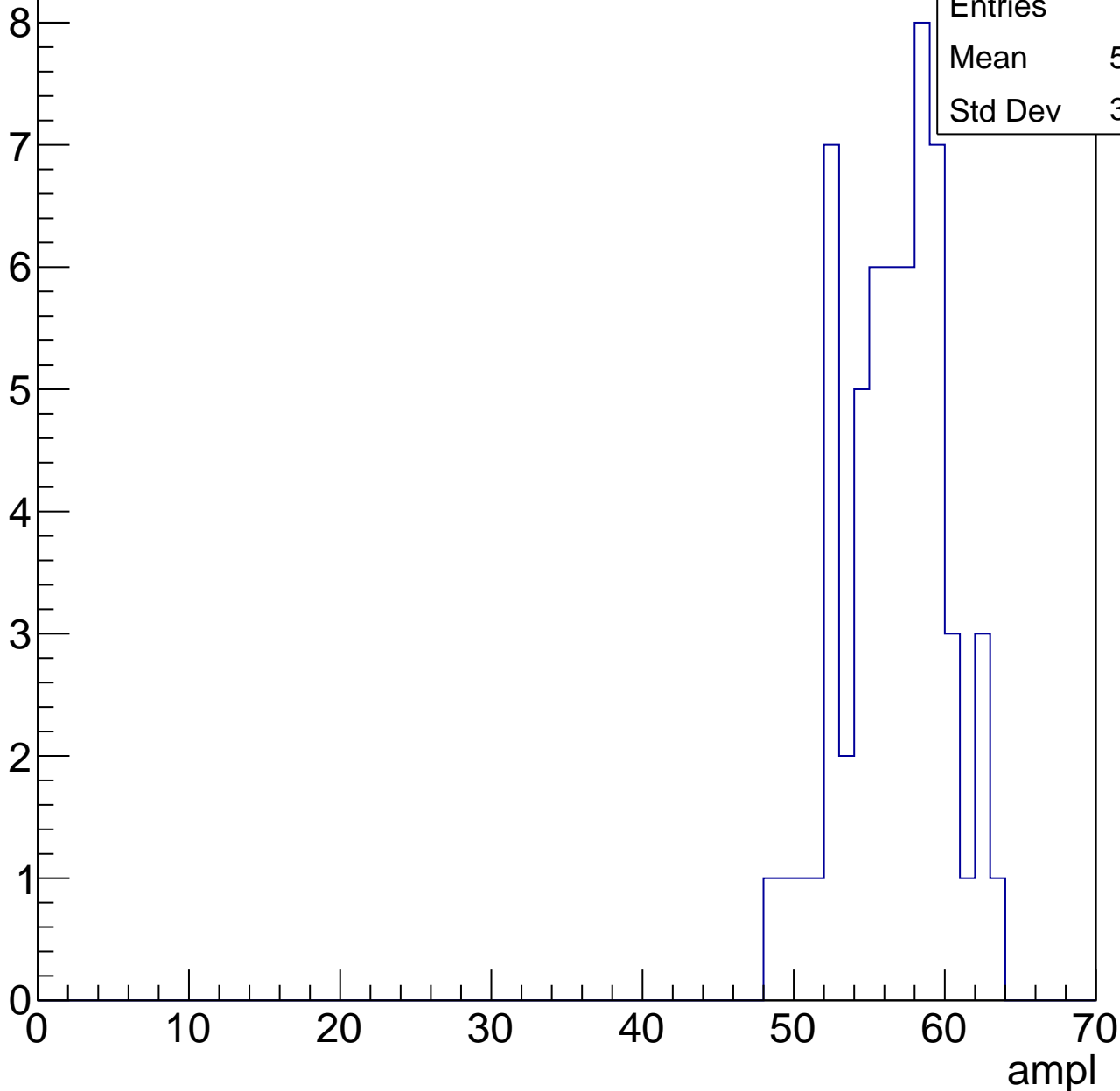


# B1L003S, U6-ch65, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	56.15
Std Dev	3.344

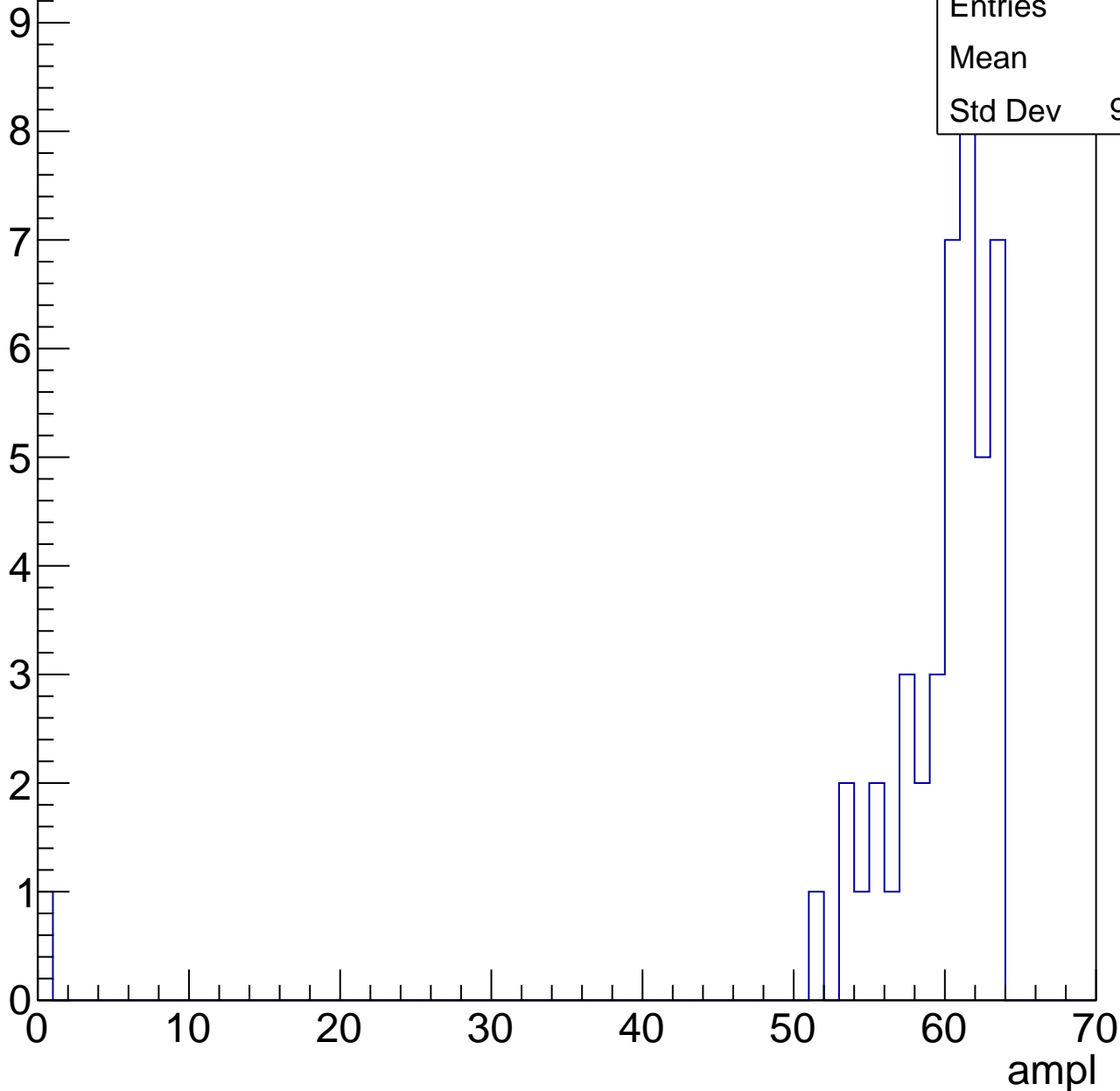


# B1L003S, U6-ch65, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	44
Mean	58.2
Std Dev	9.377



# B1L003S, U6-ch65, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch65, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch66, adc0

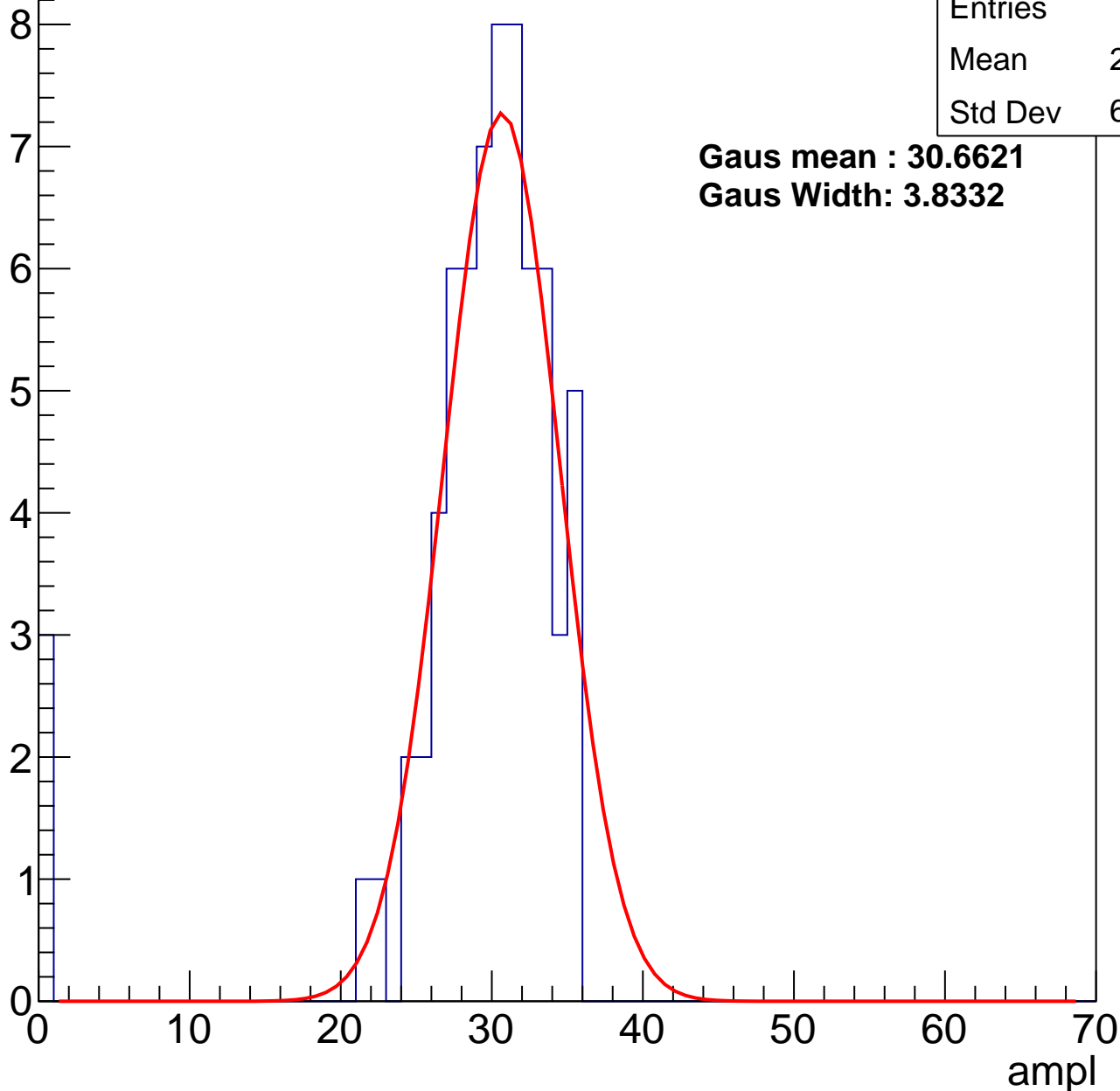
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	28.43
Std Dev	6.867

**Gaus mean : 30.6621**

**Gaus Width: 3.8332**



# B1L003S, U6-ch66, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	64
Mean	36.42
Std Dev	3.376

**Gaus mean : 36.5811**

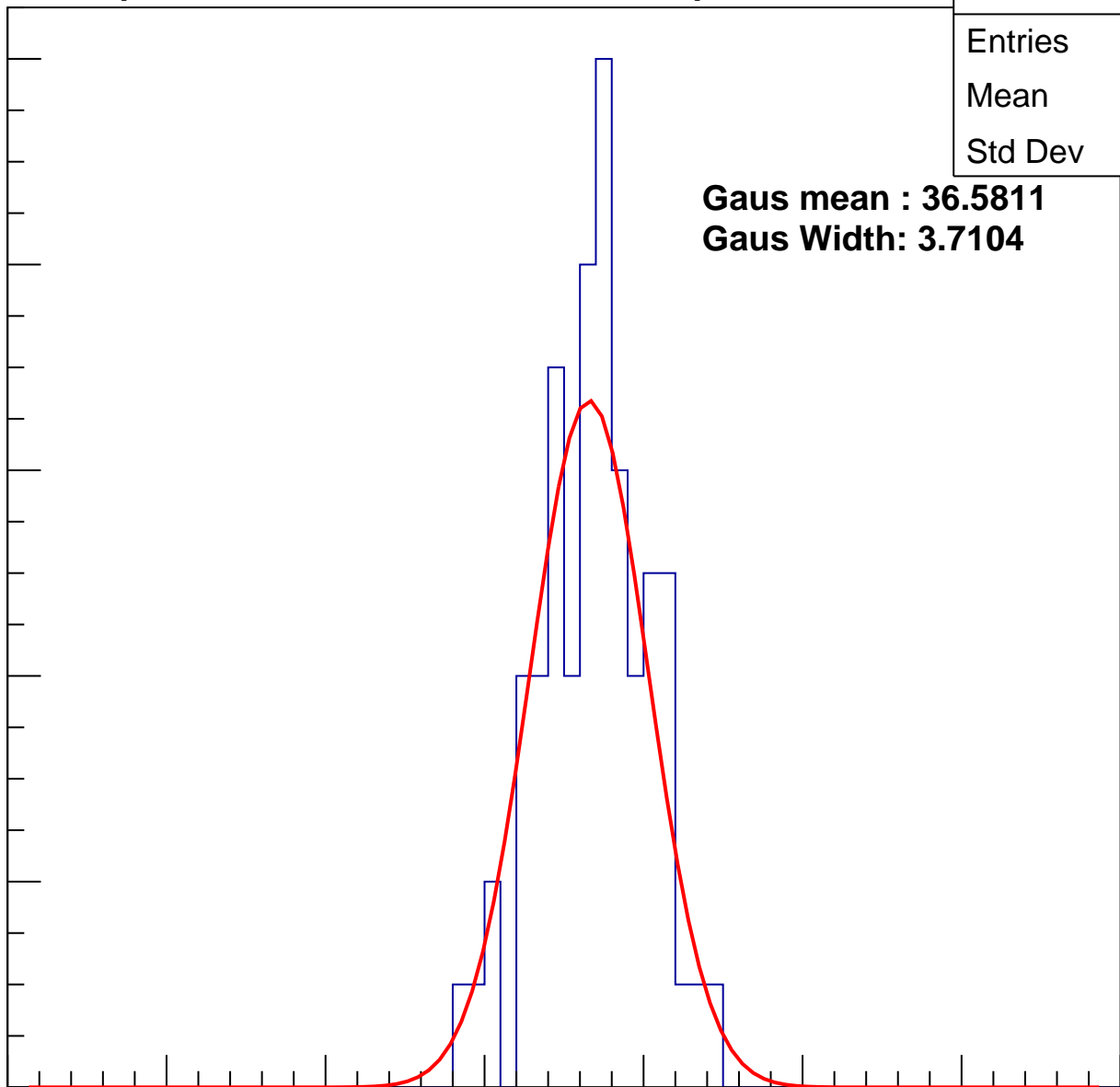
**Gaus Width: 3.7104**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U6-ch66, adc2

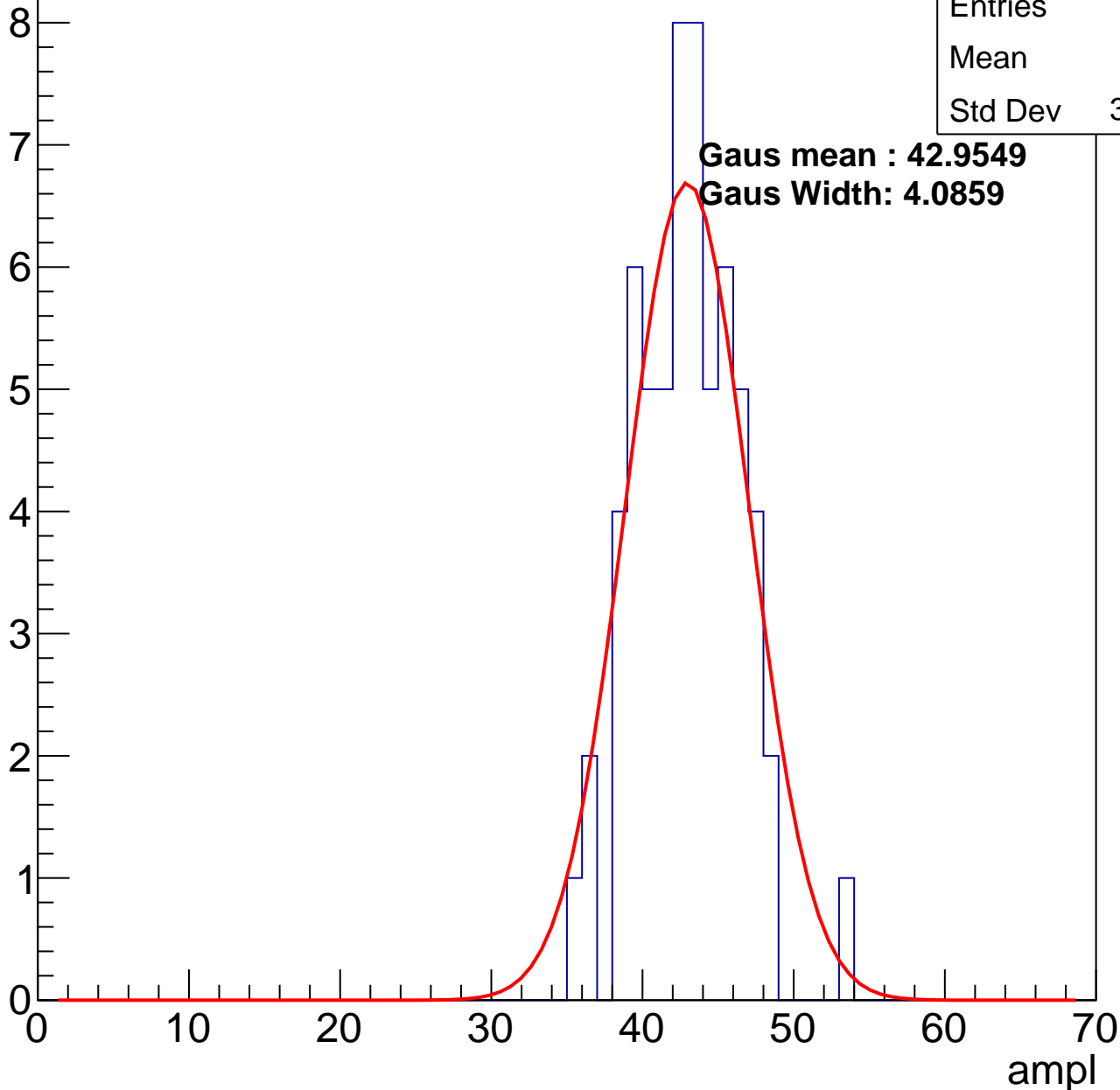
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	42.5
Std Dev	3.368

**Gaus mean : 42.9549**

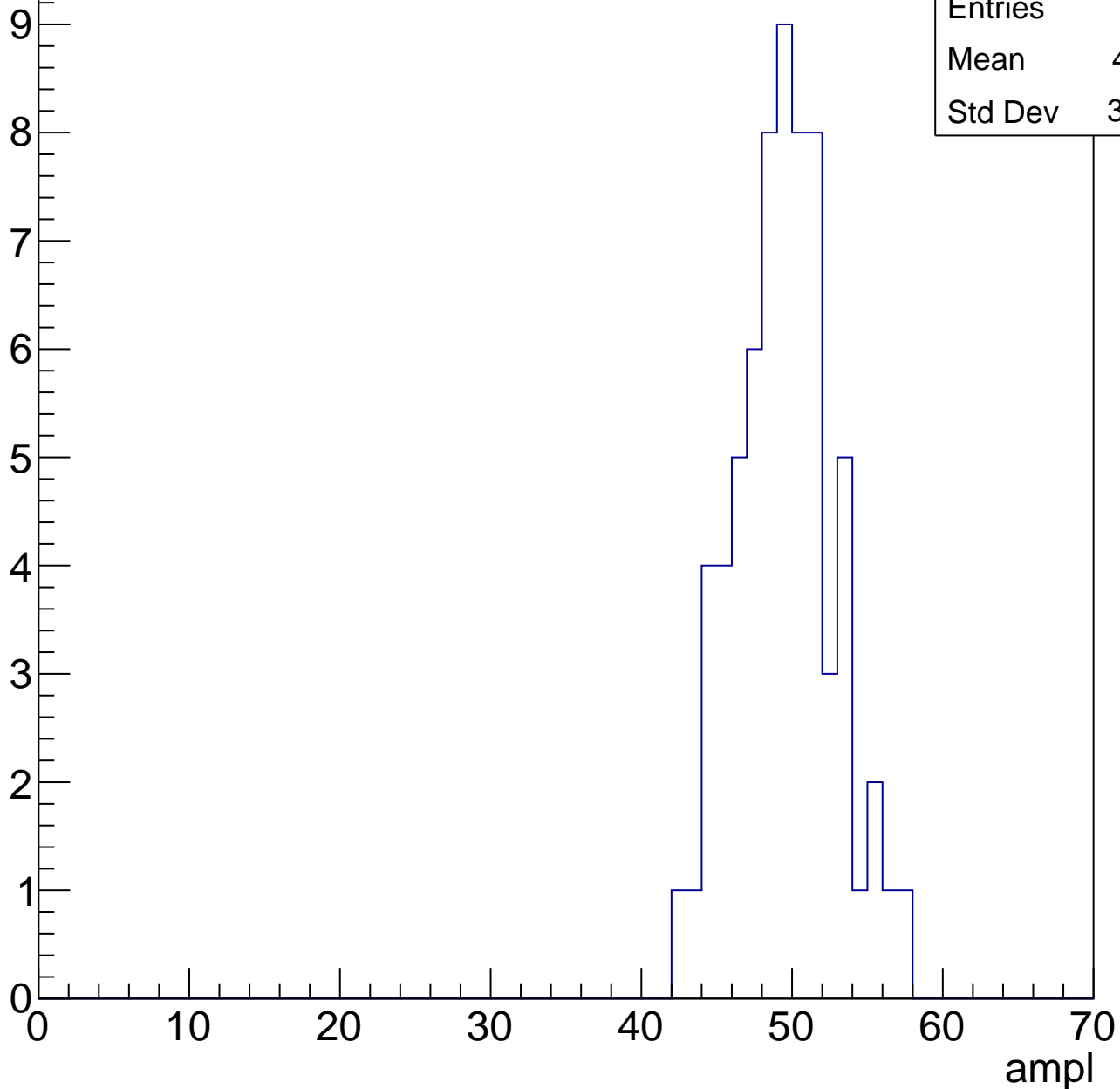
**Gaus Width: 4.0859**



# B1L003S, U6-ch66, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

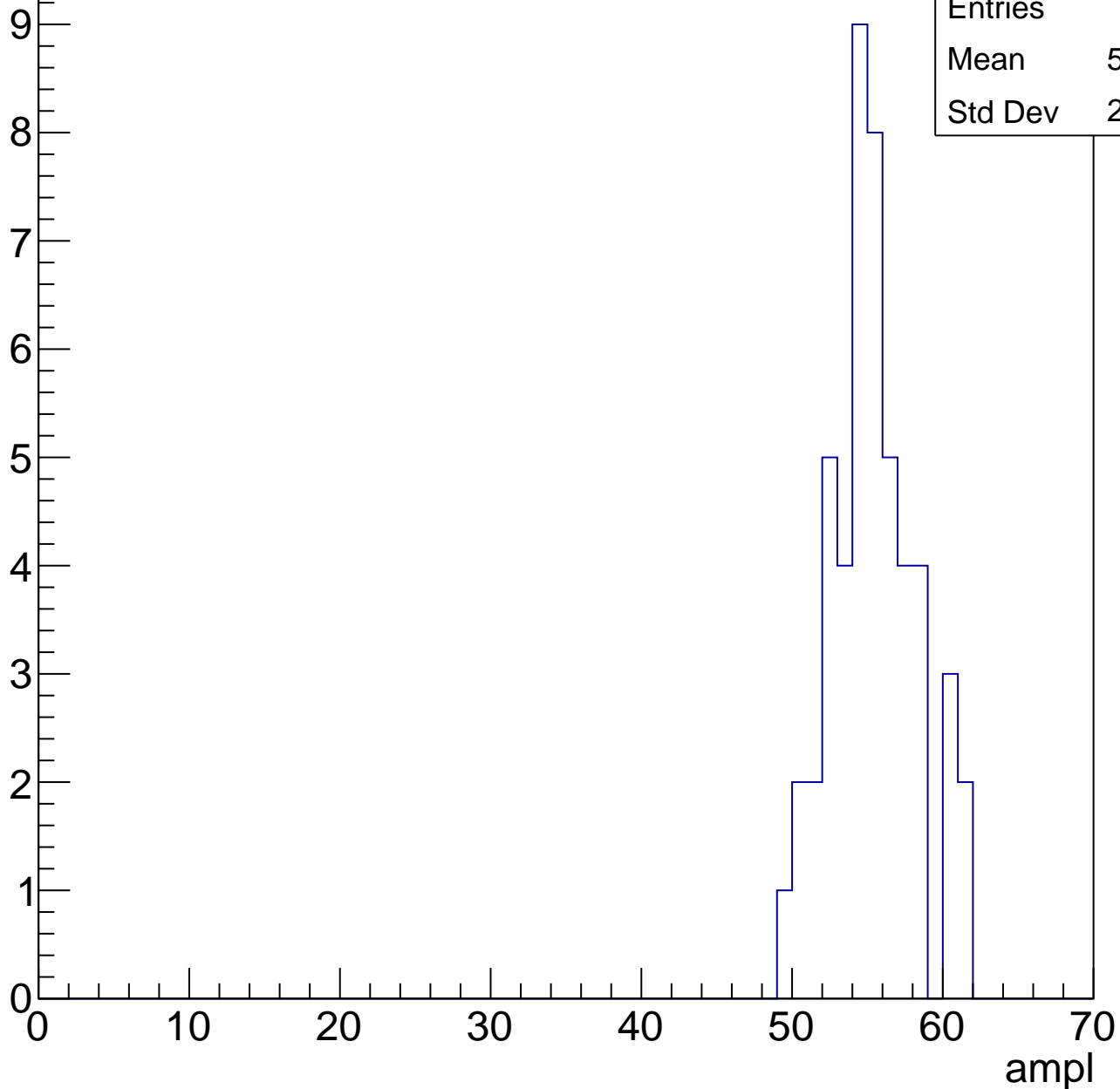


Entries	67
Mean	49.01
Std Dev	3.193

# B1L003S, U6-ch66, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

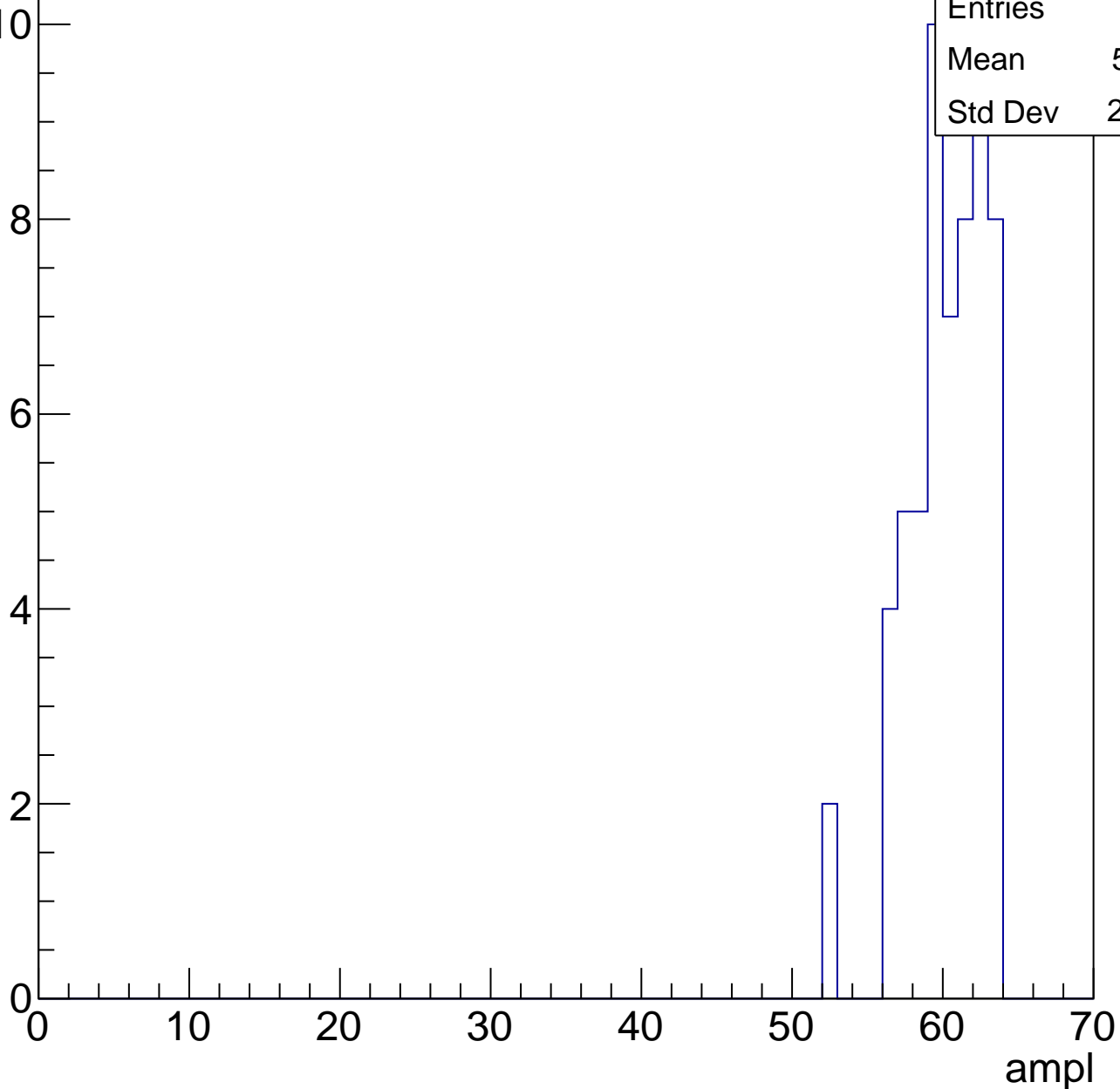


# B1L003S, U6-ch66, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

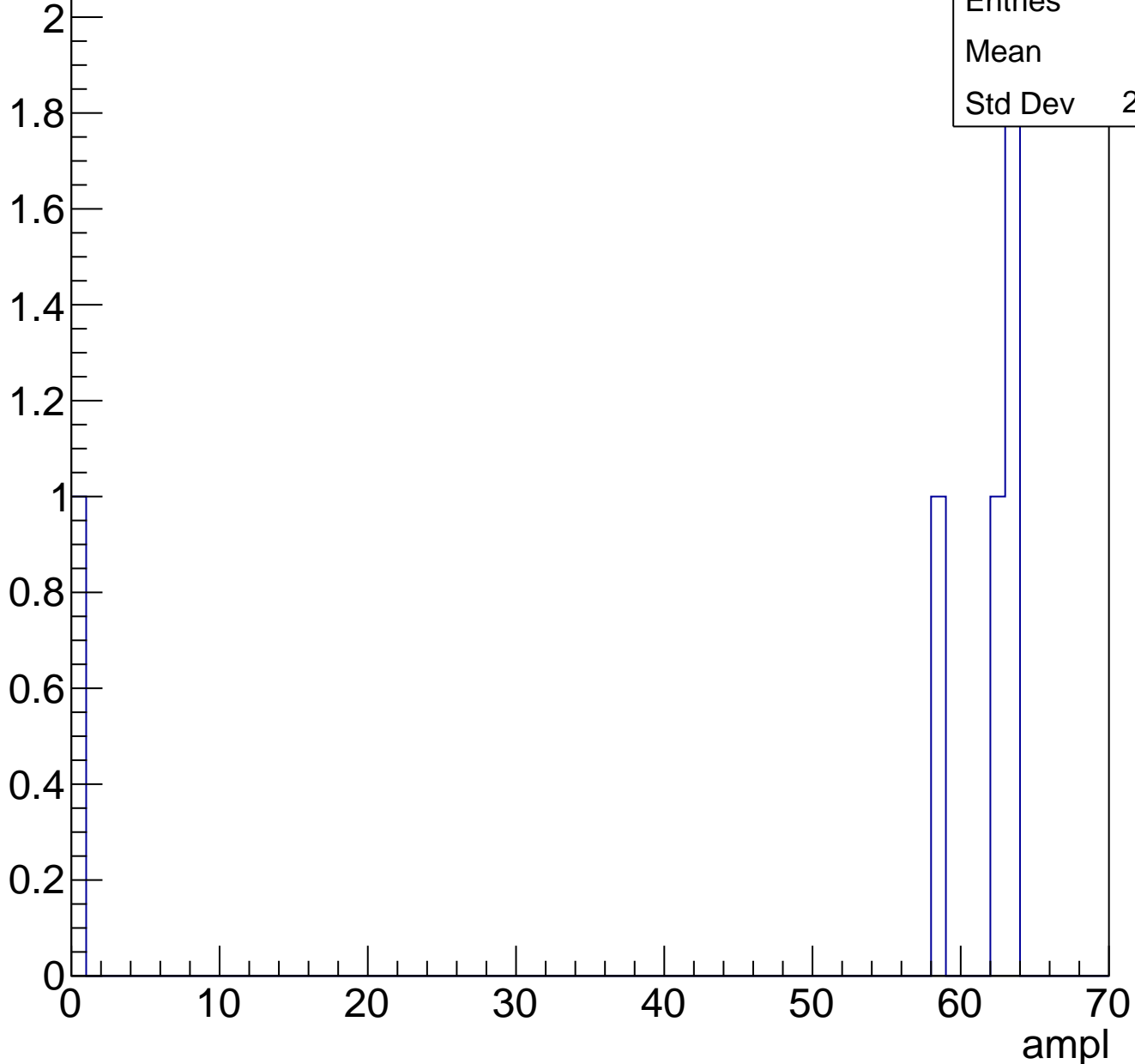
Entries	58
Mean	59.71
Std Dev	2.553



# B1L003S, U6-ch66, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch66, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U6-ch67, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	68
Mean	28.54
Std Dev	6.035

**Gaus mean : 30.0180**

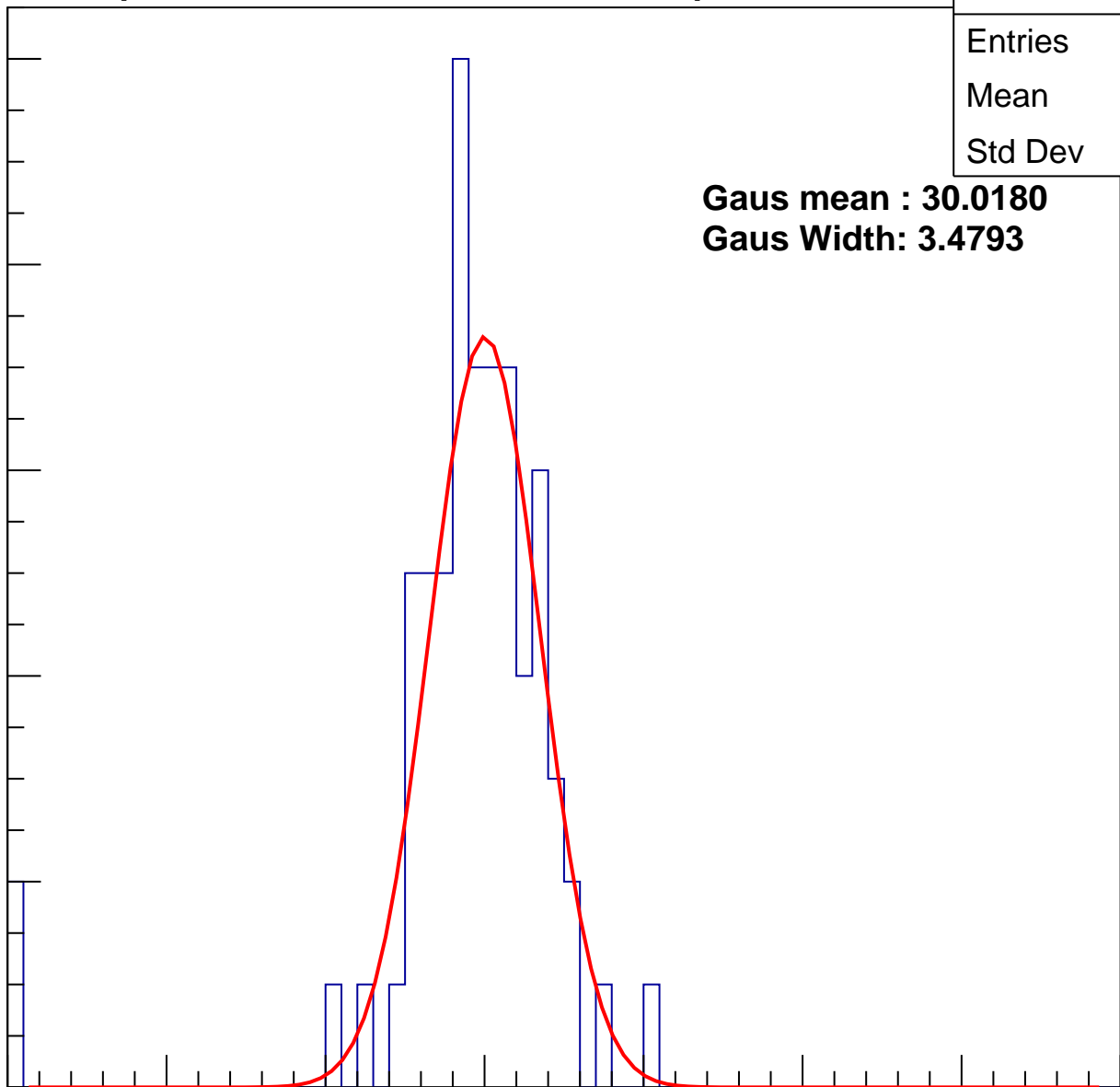
**Gaus Width: 3.4793**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U6-ch67, adc1

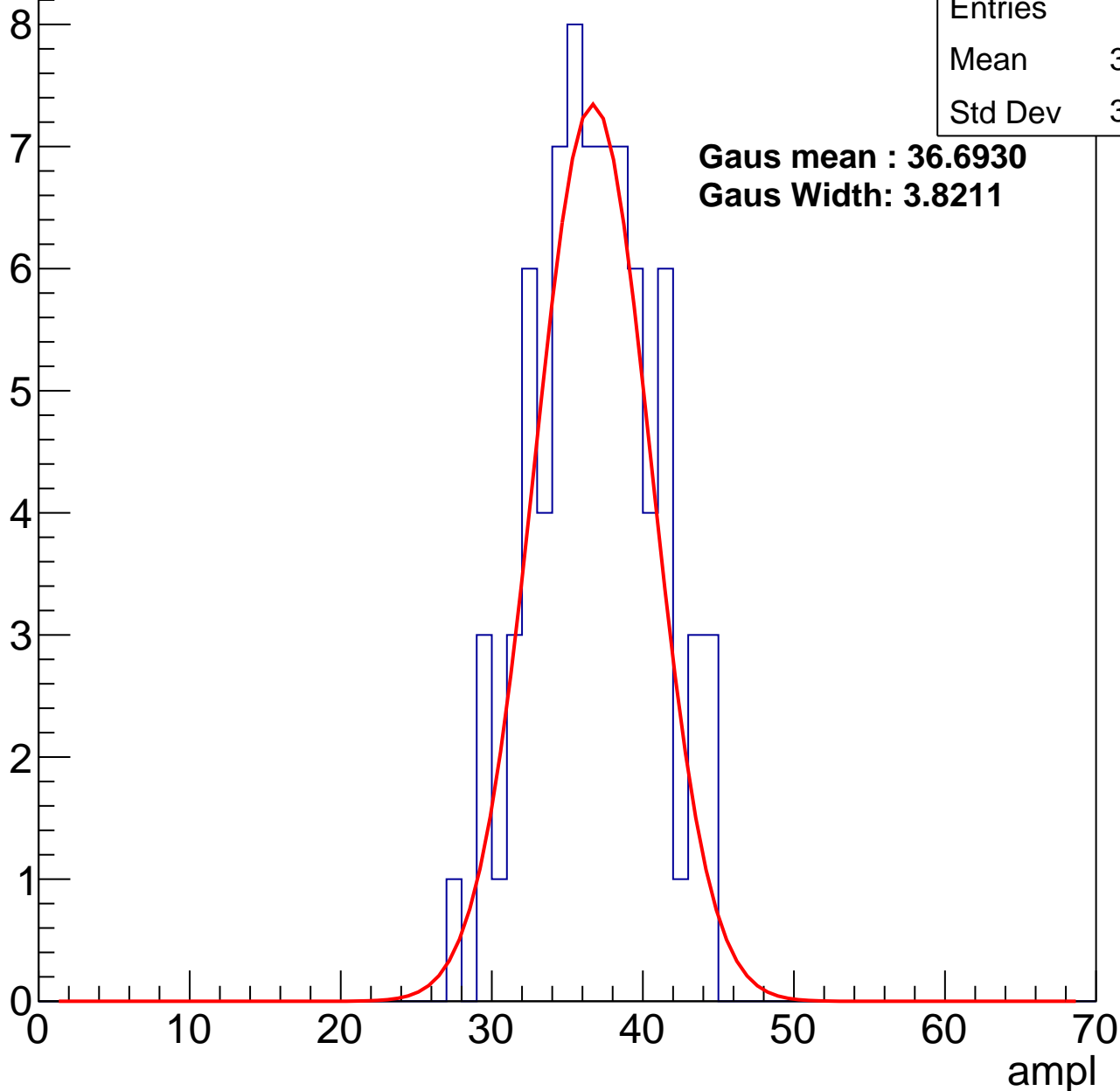
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	77
Mean	36.35
Std Dev	3.907

**Gaus mean : 36.6930**

**Gaus Width: 3.8211**



# B1L003S, U6-ch67, adc2

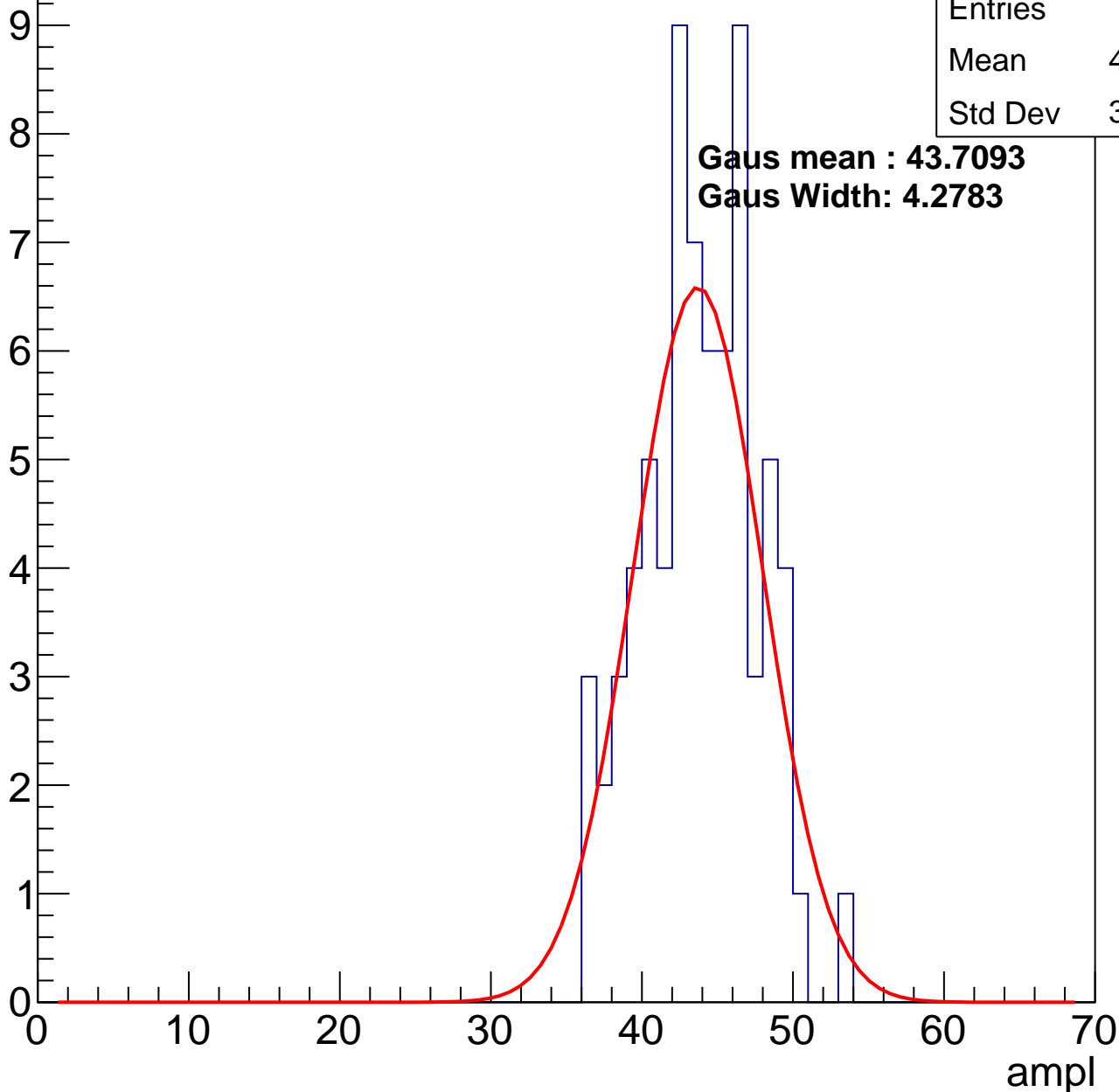
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	72
Mean	43.38
Std Dev	3.717

**Gaus mean : 43.7093**

**Gaus Width: 4.2783**

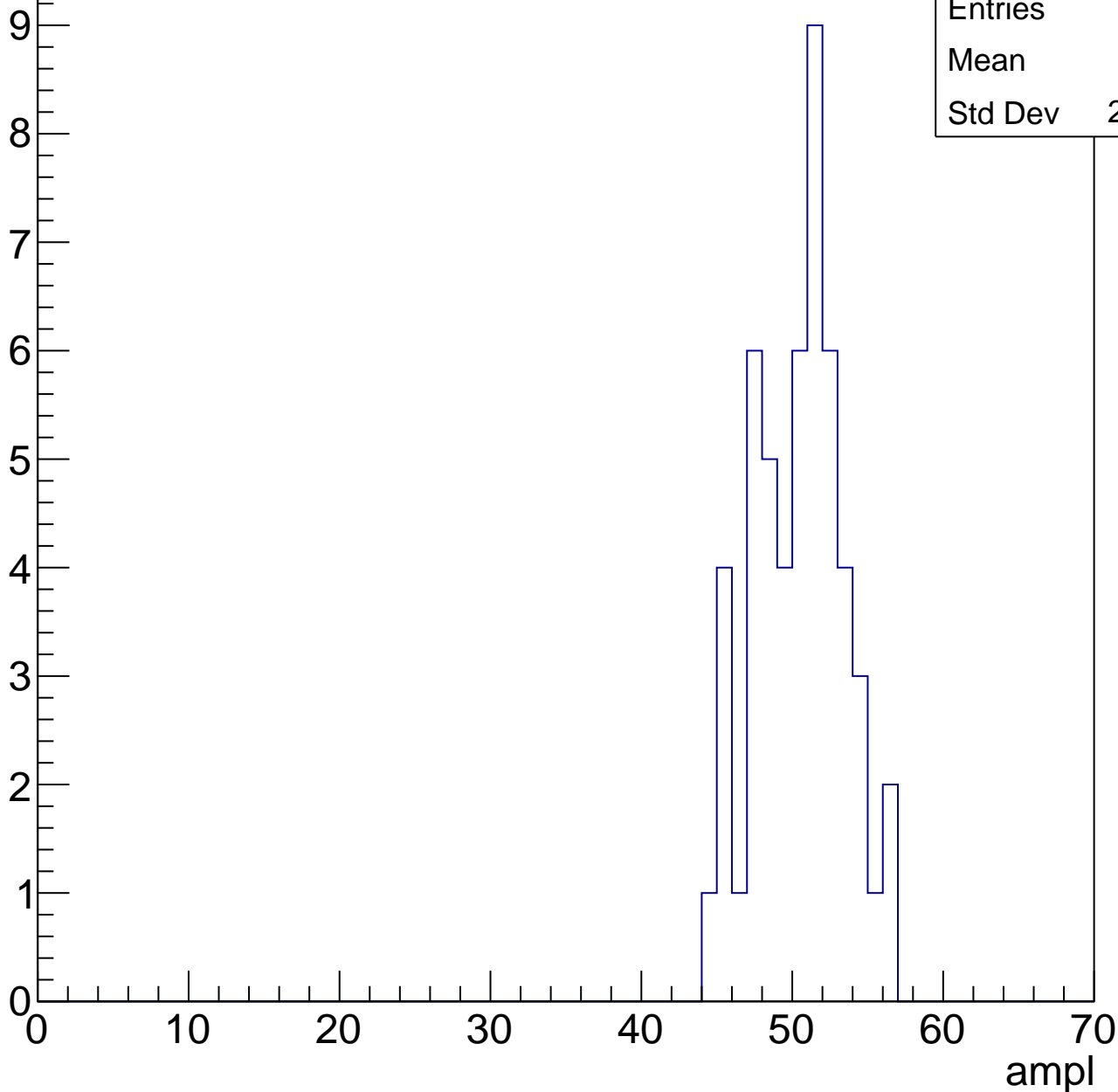


# B1L003S, U6-ch67, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	52
Mean	50
Std Dev	2.922

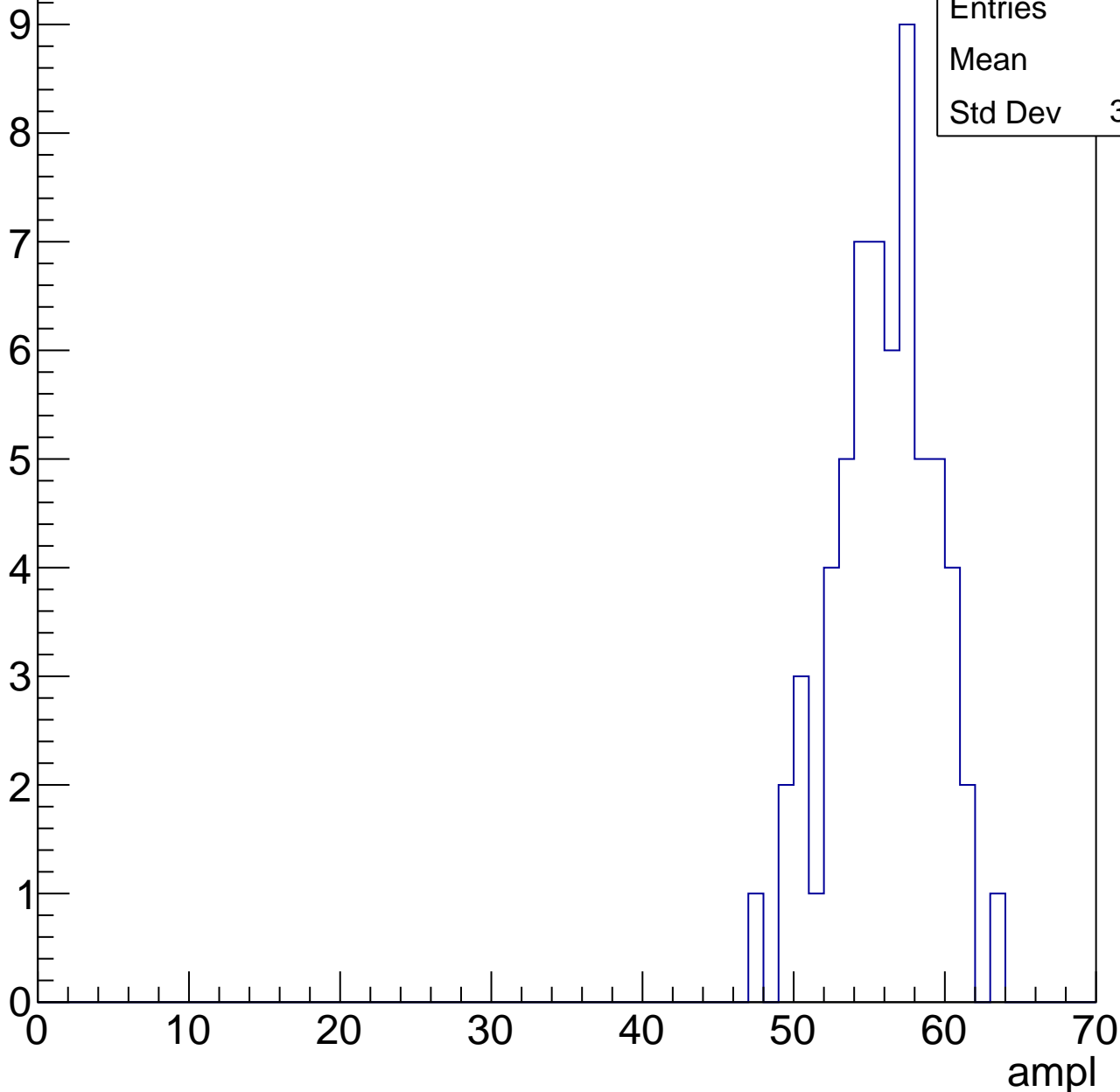


# B1L003S, U6-ch67, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	55.5
Std Dev	3.306

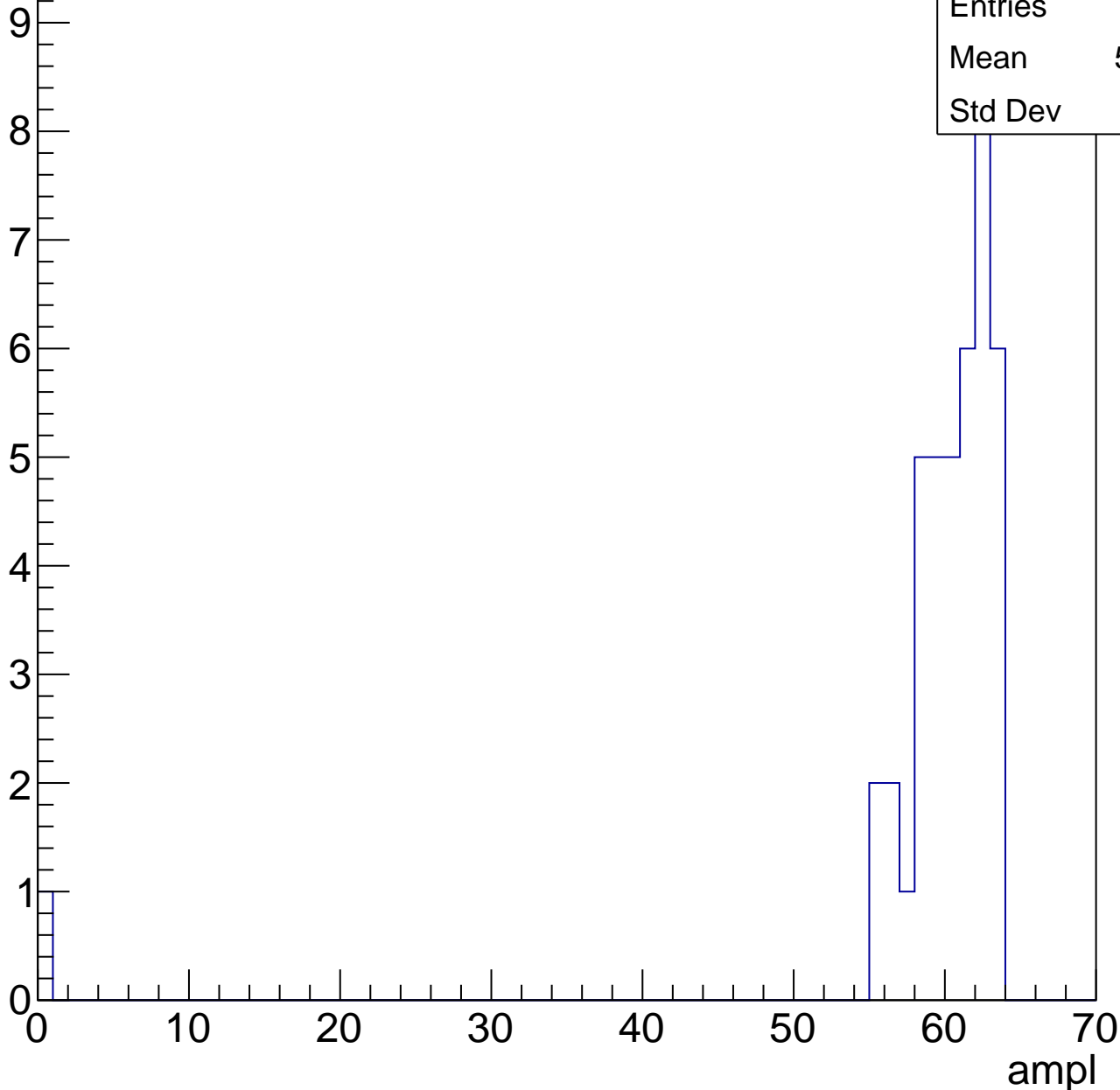


# B1L003S, U6-ch67, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

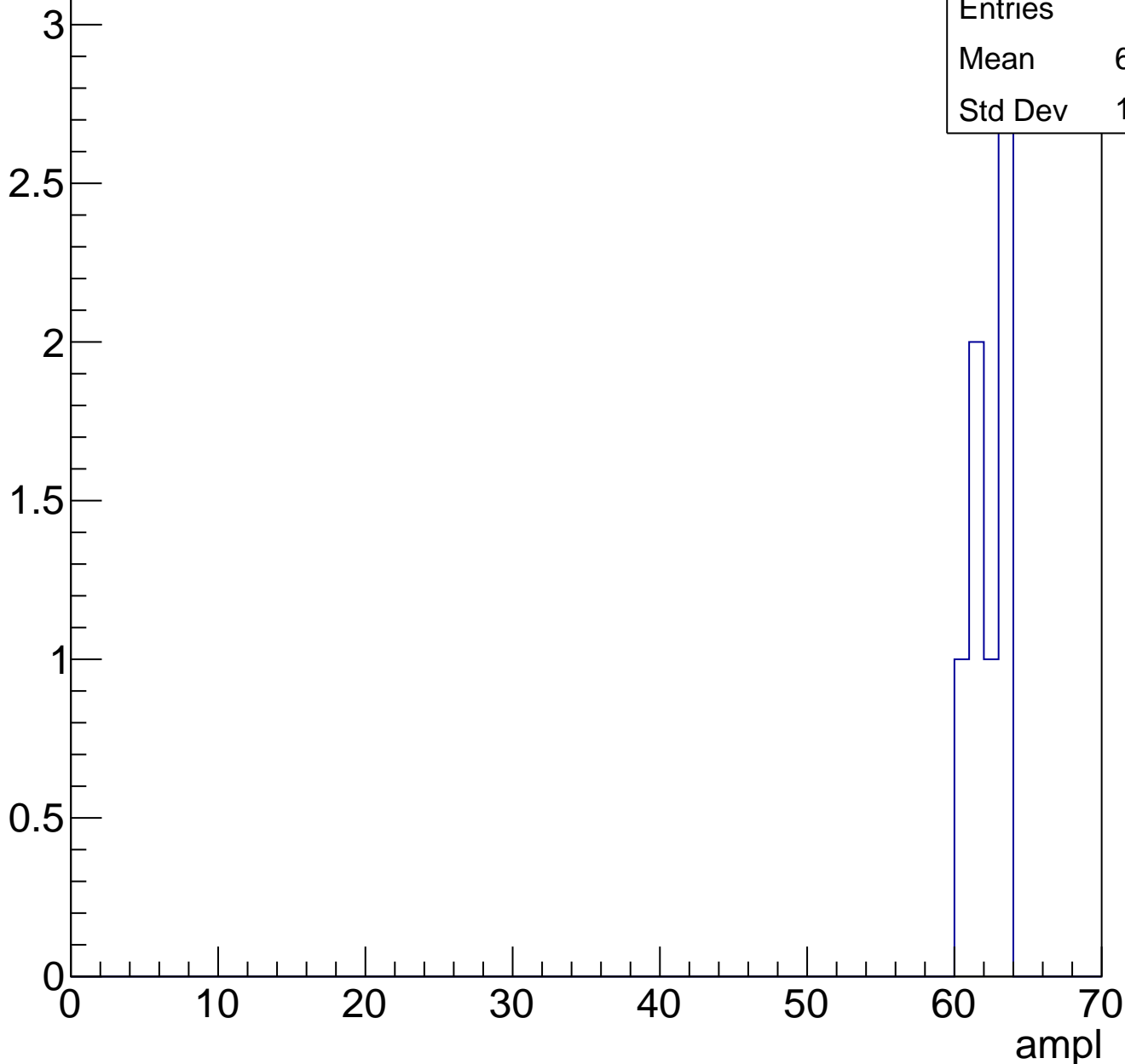
Entries	42
Mean	58.71
Std Dev	9.44



# B1L003S, U6-ch67, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch67, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U6-ch68, adc0

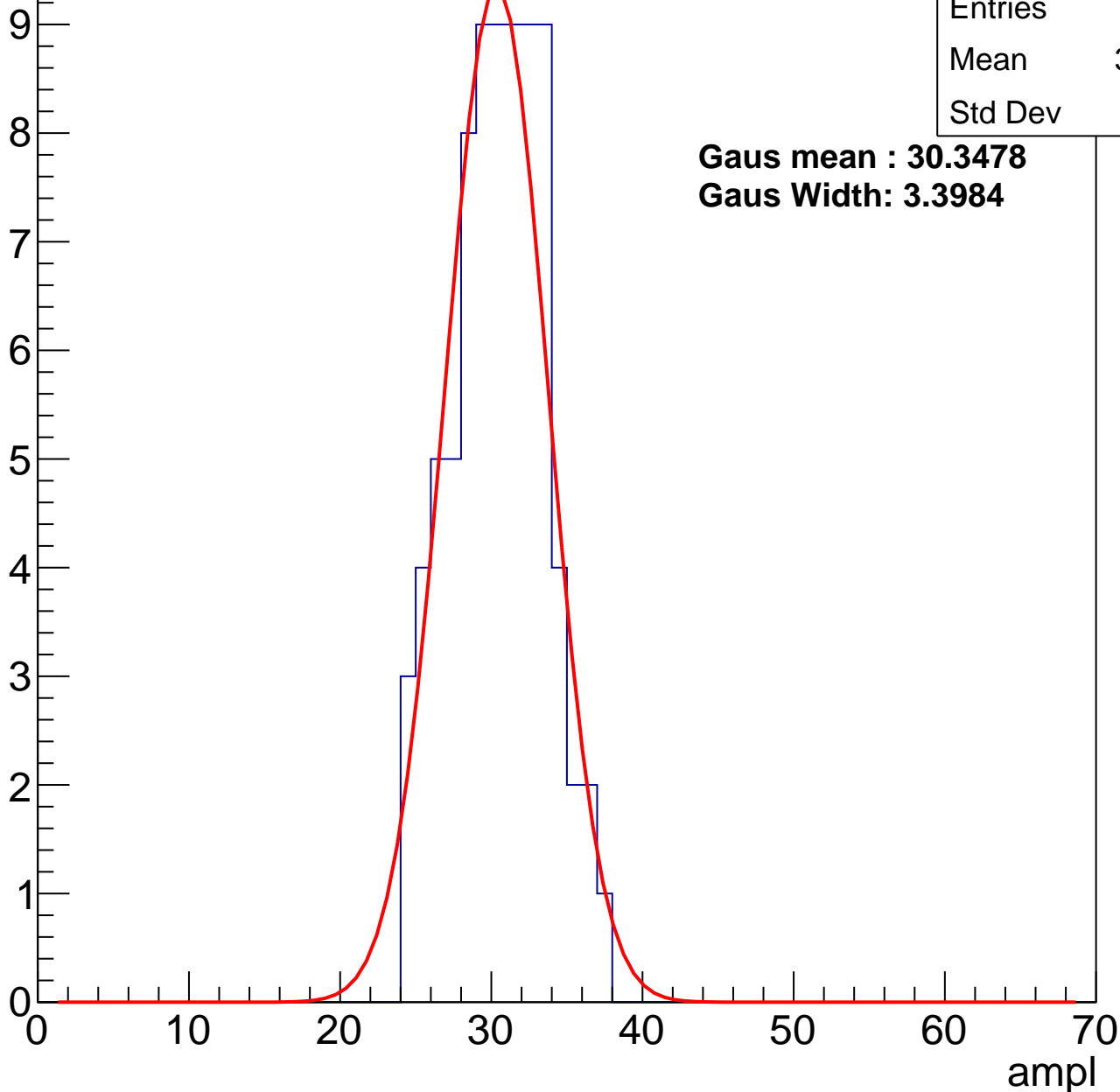
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	79
Mean	30.01
Std Dev	3.05

**Gaus mean : 30.3478**

**Gaus Width: 3.3984**



# B1L003S, U6-ch68, adc1

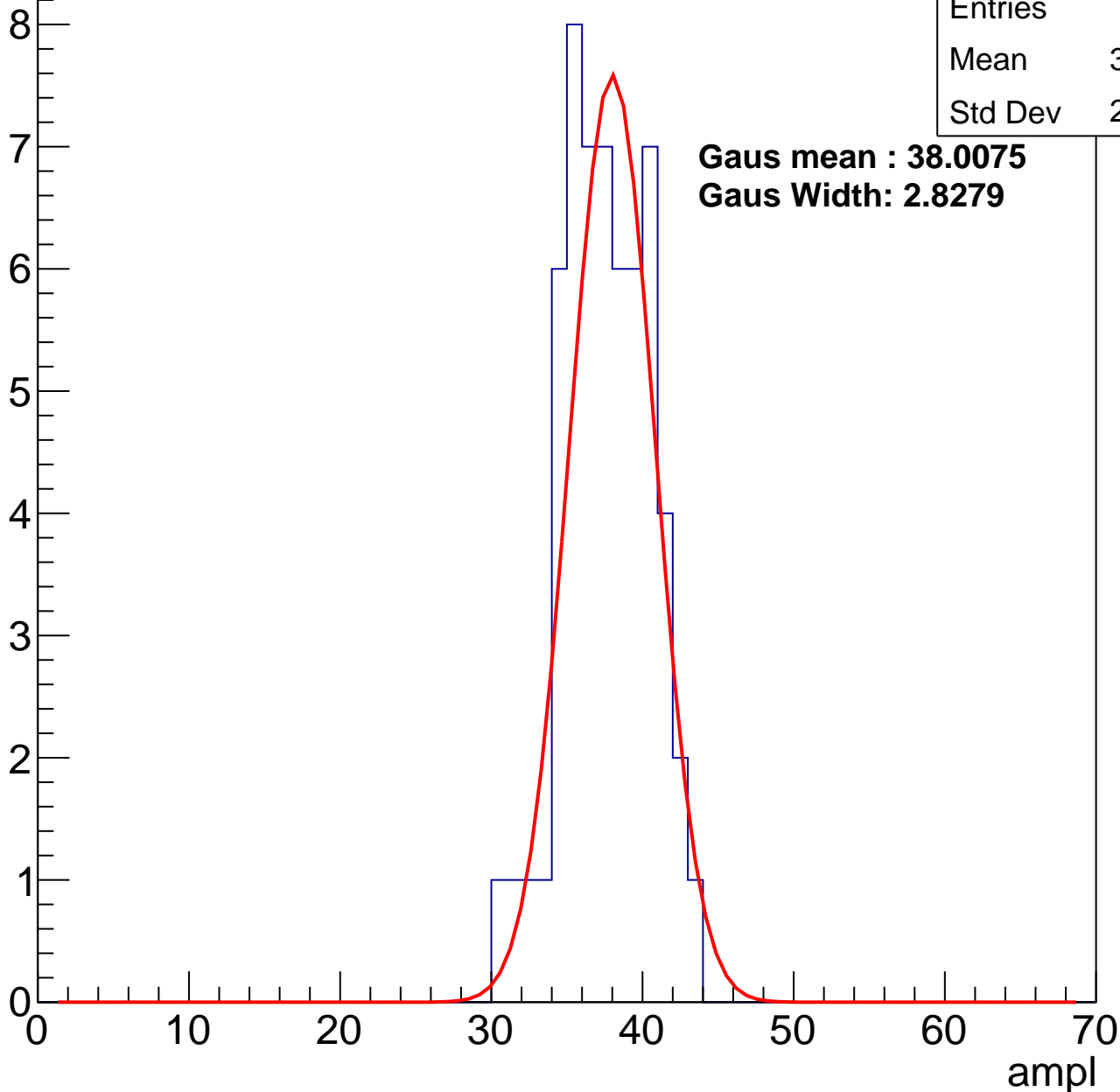
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	37.14
Std Dev	2.819

**Gaus mean : 38.0075**

**Gaus Width: 2.8279**



# B1L003S, U6-ch68, adc2

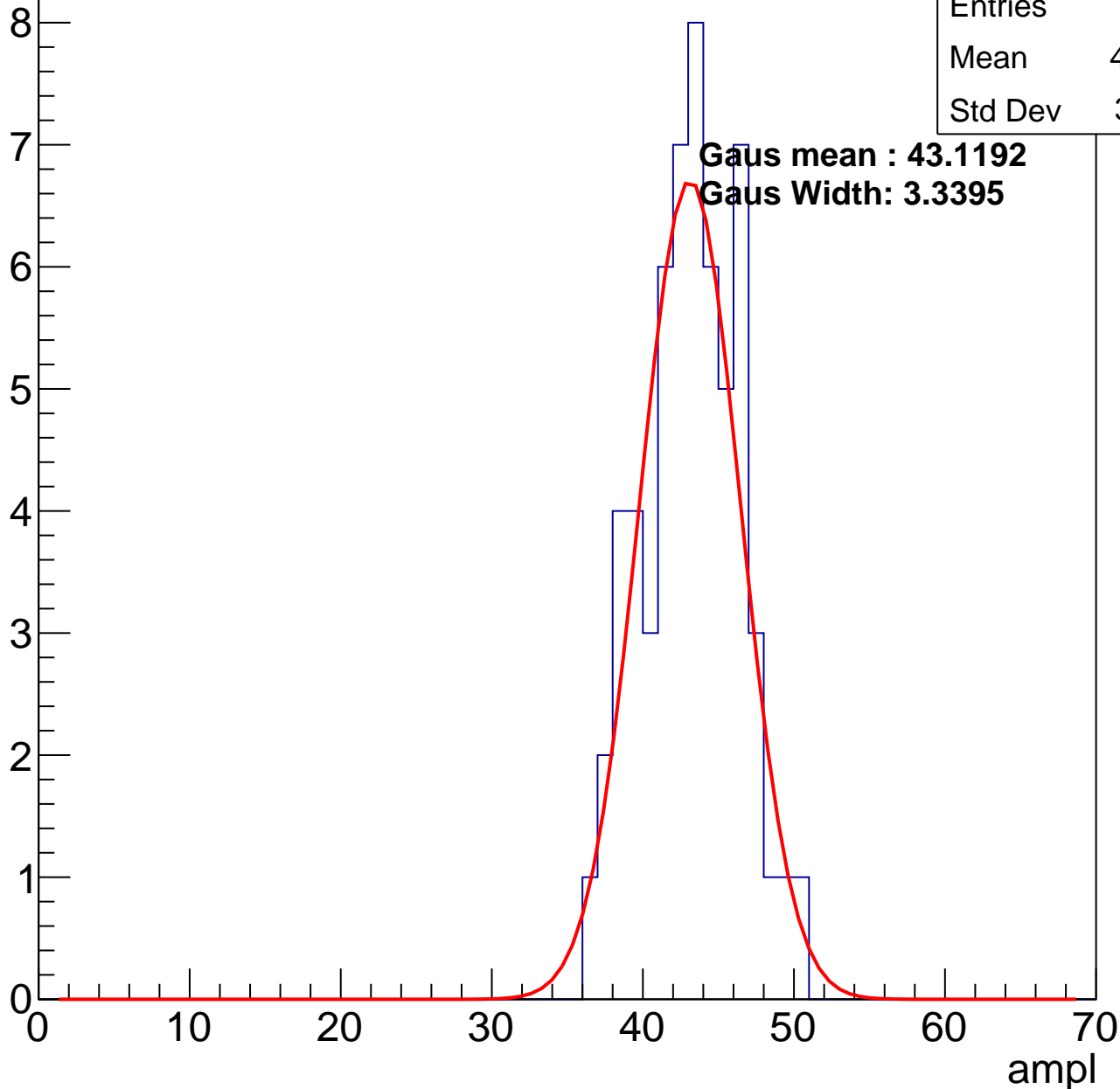
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	42.73
Std Dev	3.151

**Gaus mean : 43.1192**

**Gaus Width: 3.3395**

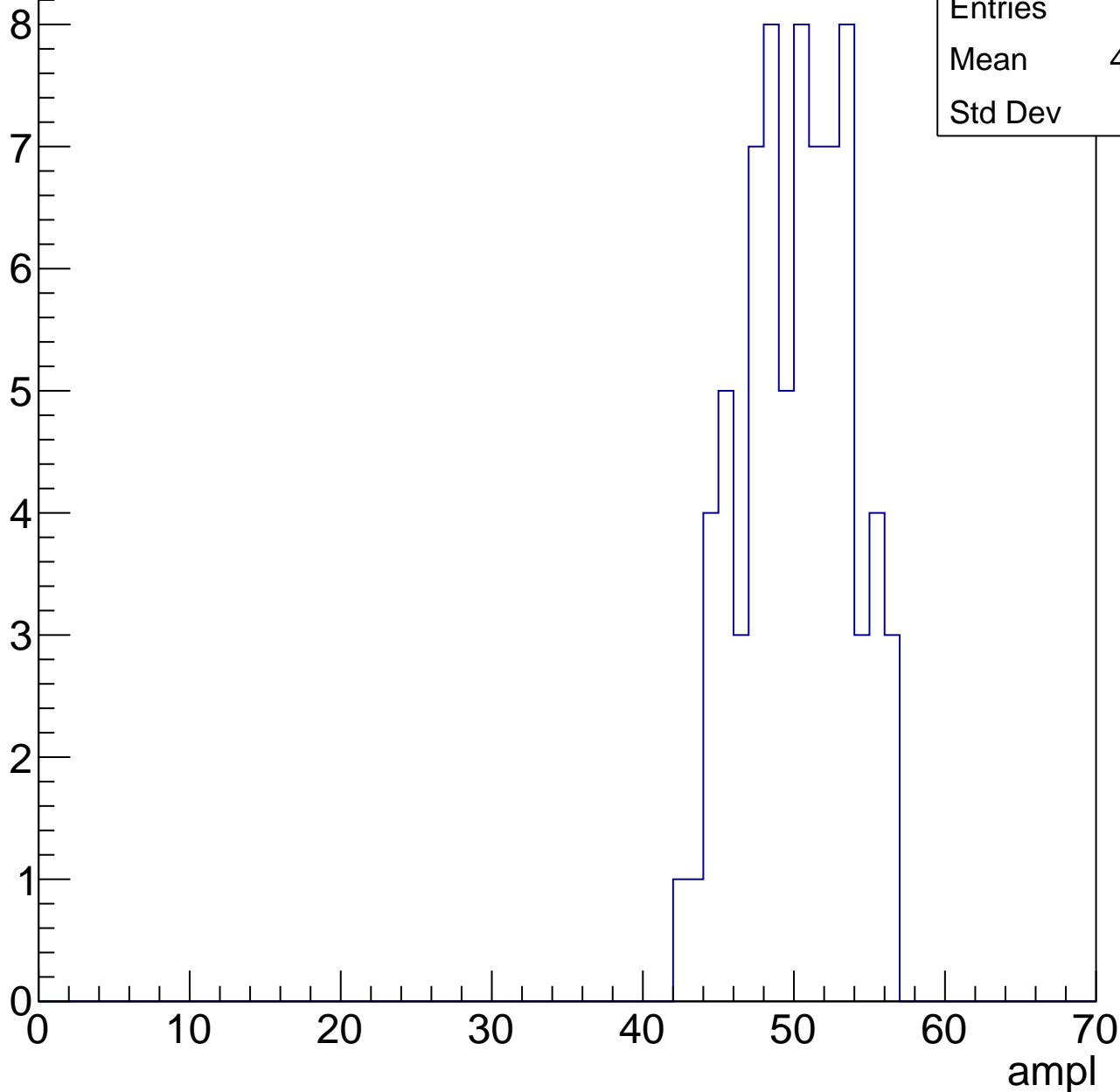


# B1L003S, U6-ch68, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

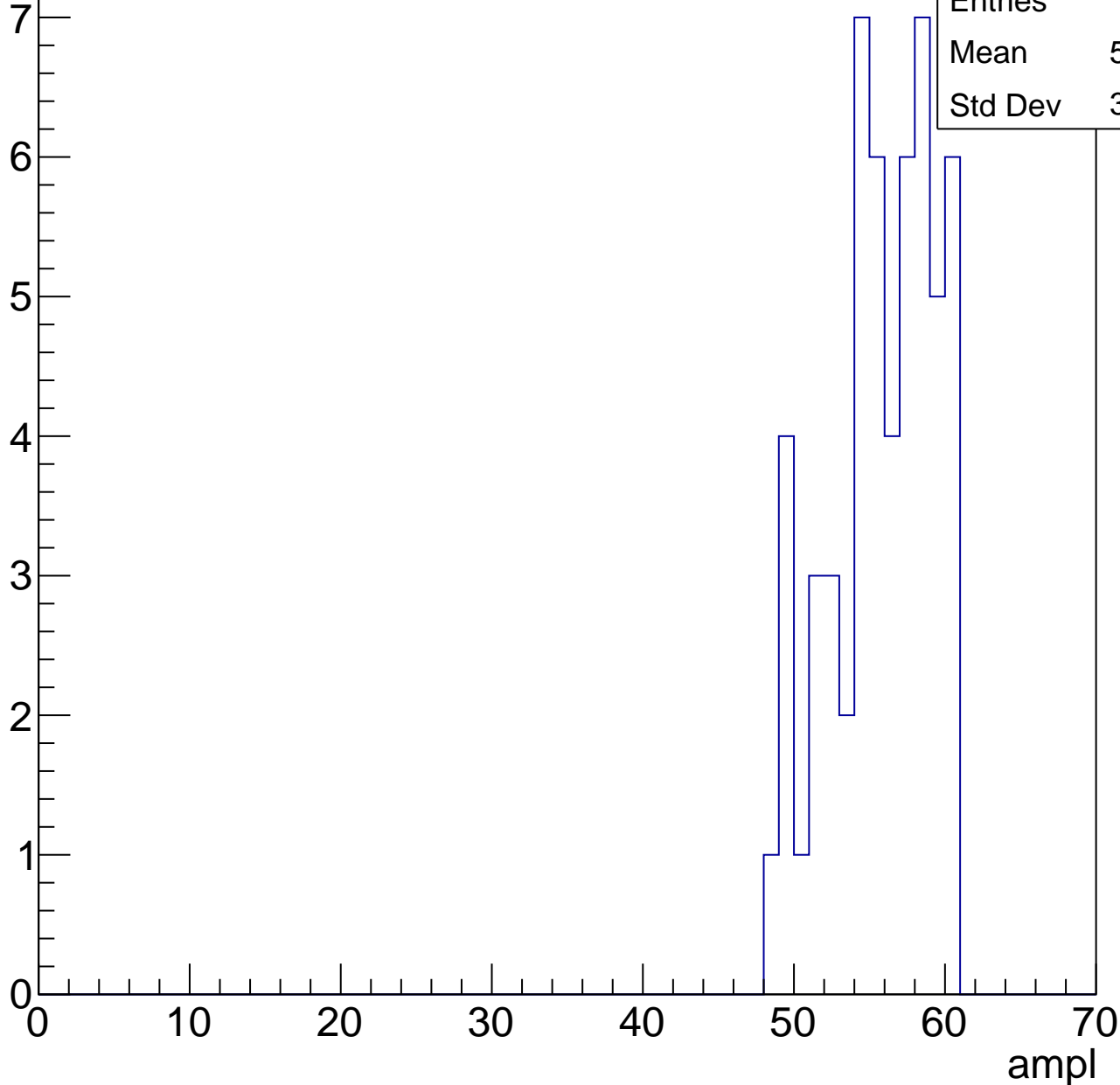
Entries	74
Mean	49.69
Std Dev	3.46



# B1L003S, U6-ch68, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



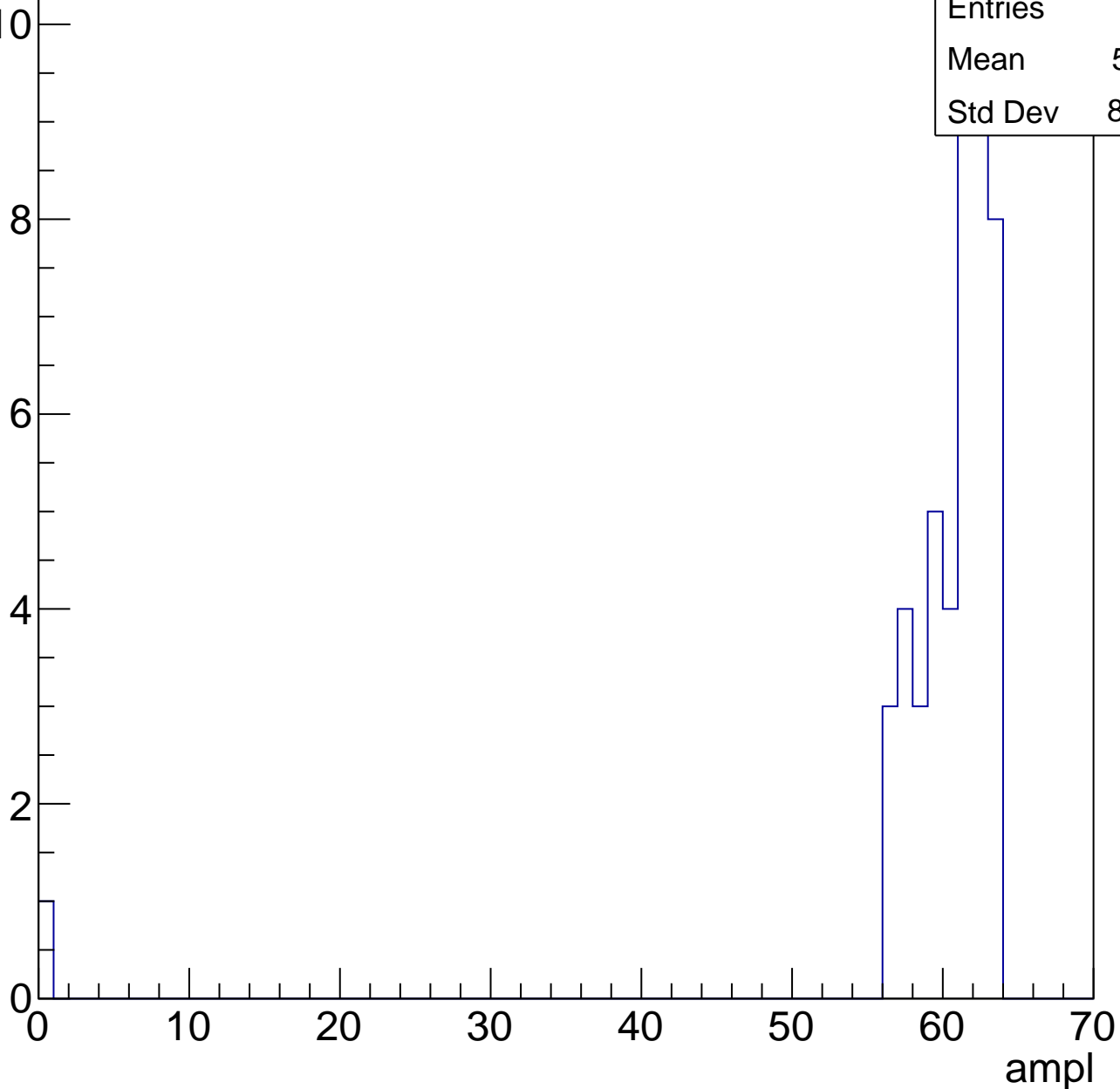
Entries	55
Mean	55.35
Std Dev	3.364

# B1L003S, U6-ch68, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	47
Mean	59.11
Std Dev	8.973



# B1L003S, U6-ch68, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch68, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch69, adc0

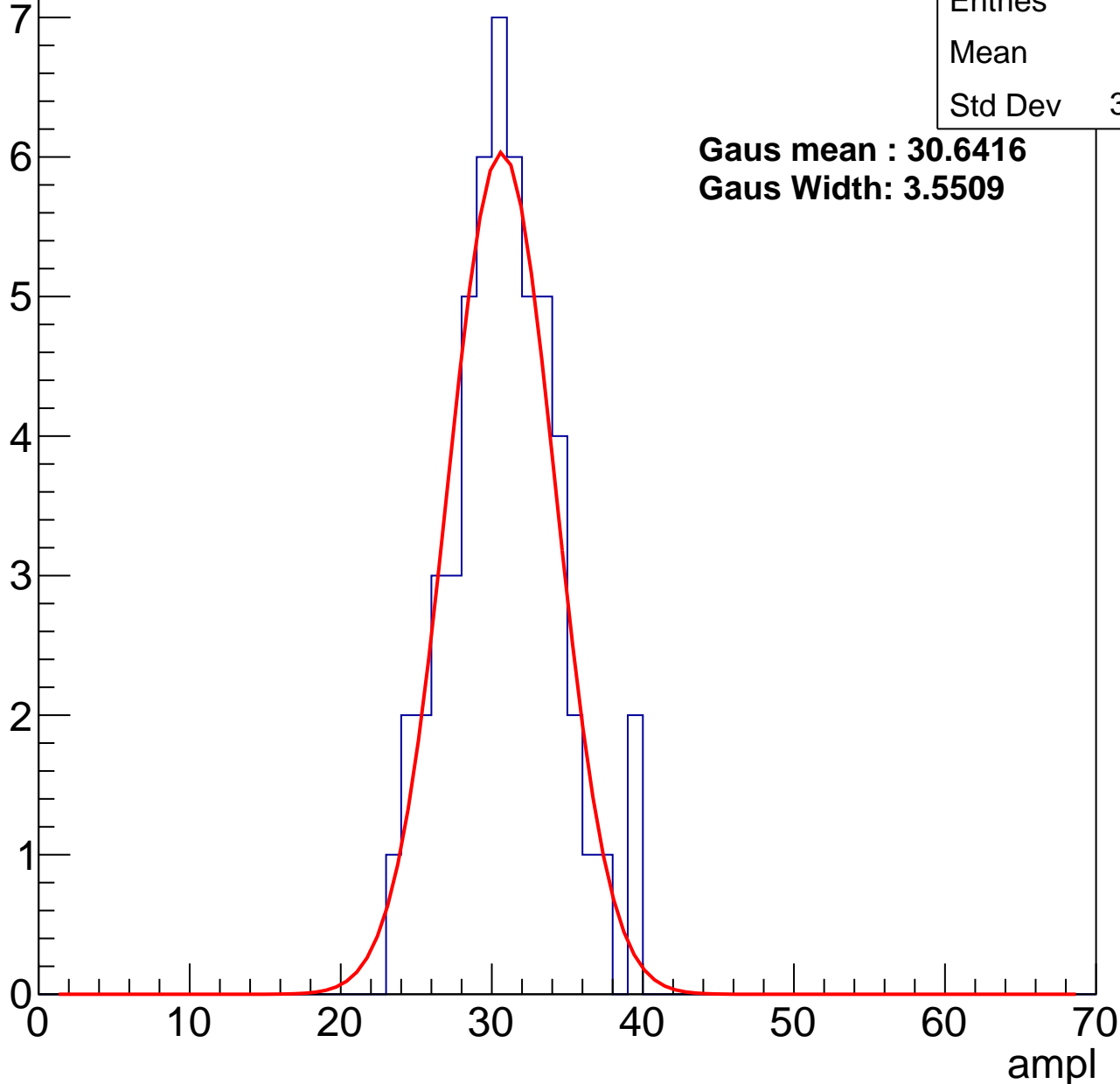
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	30.4
Std Dev	3.555

**Gaus mean : 30.6416**

**Gaus Width: 3.5509**



# B1L003S, U6-ch69, adc1

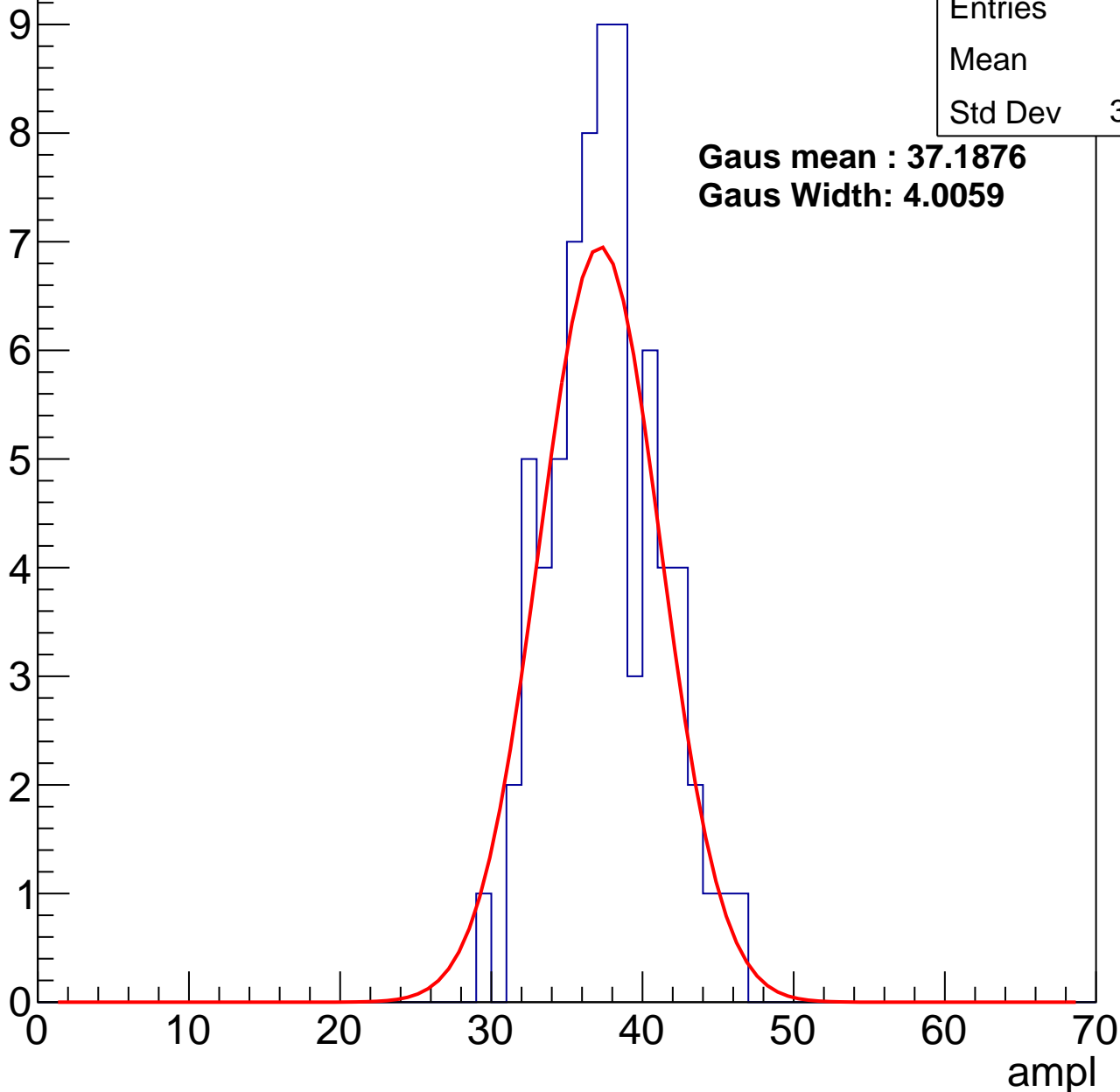
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	72
Mean	37.1
Std Dev	3.556

**Gaus mean : 37.1876**

**Gaus Width: 4.0059**



# B1L003S, U6-ch69, adc2

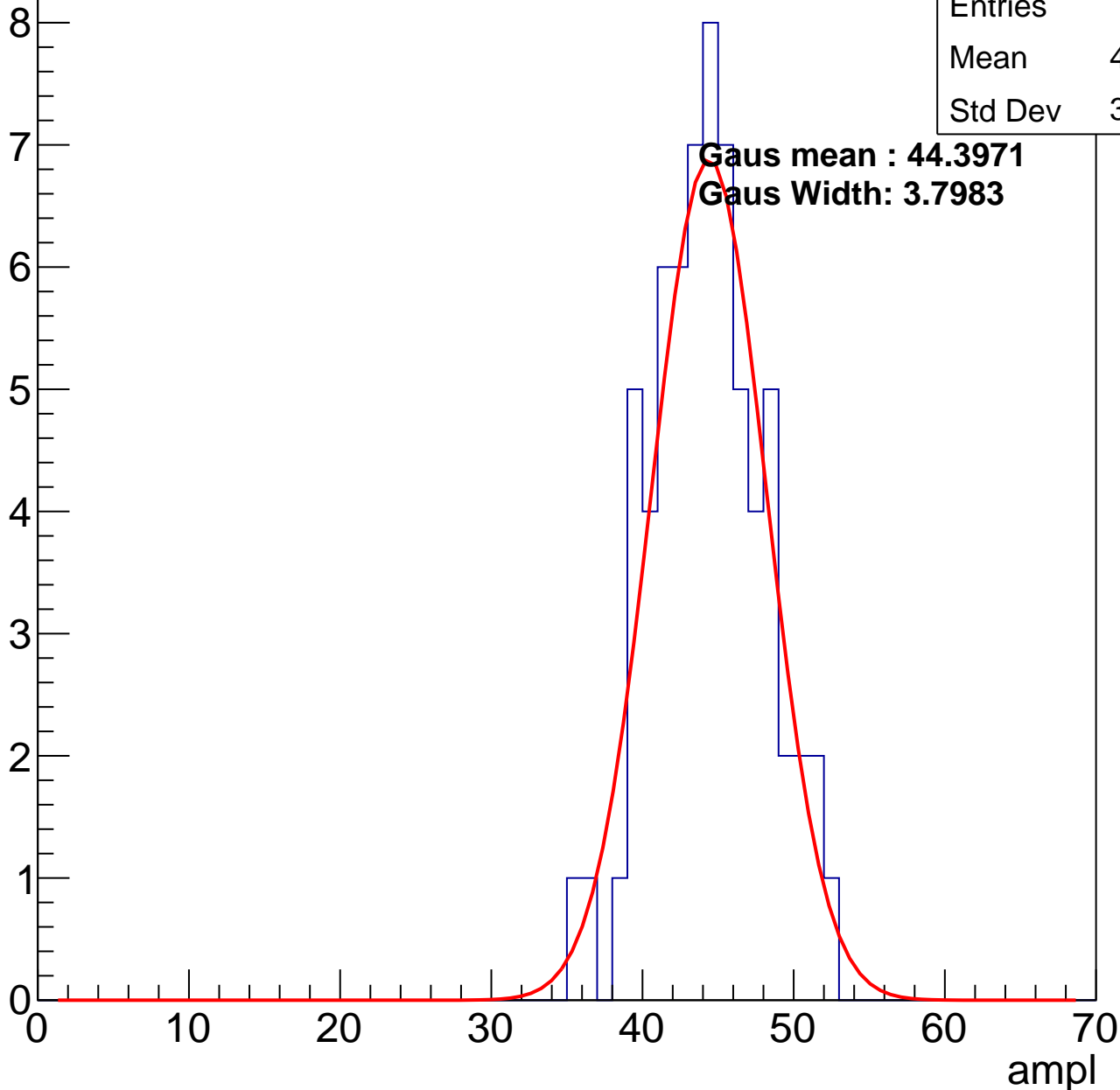
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	43.88
Std Dev	3.626

**Gaus mean : 44.3971**

**Gaus Width: 3.7983**

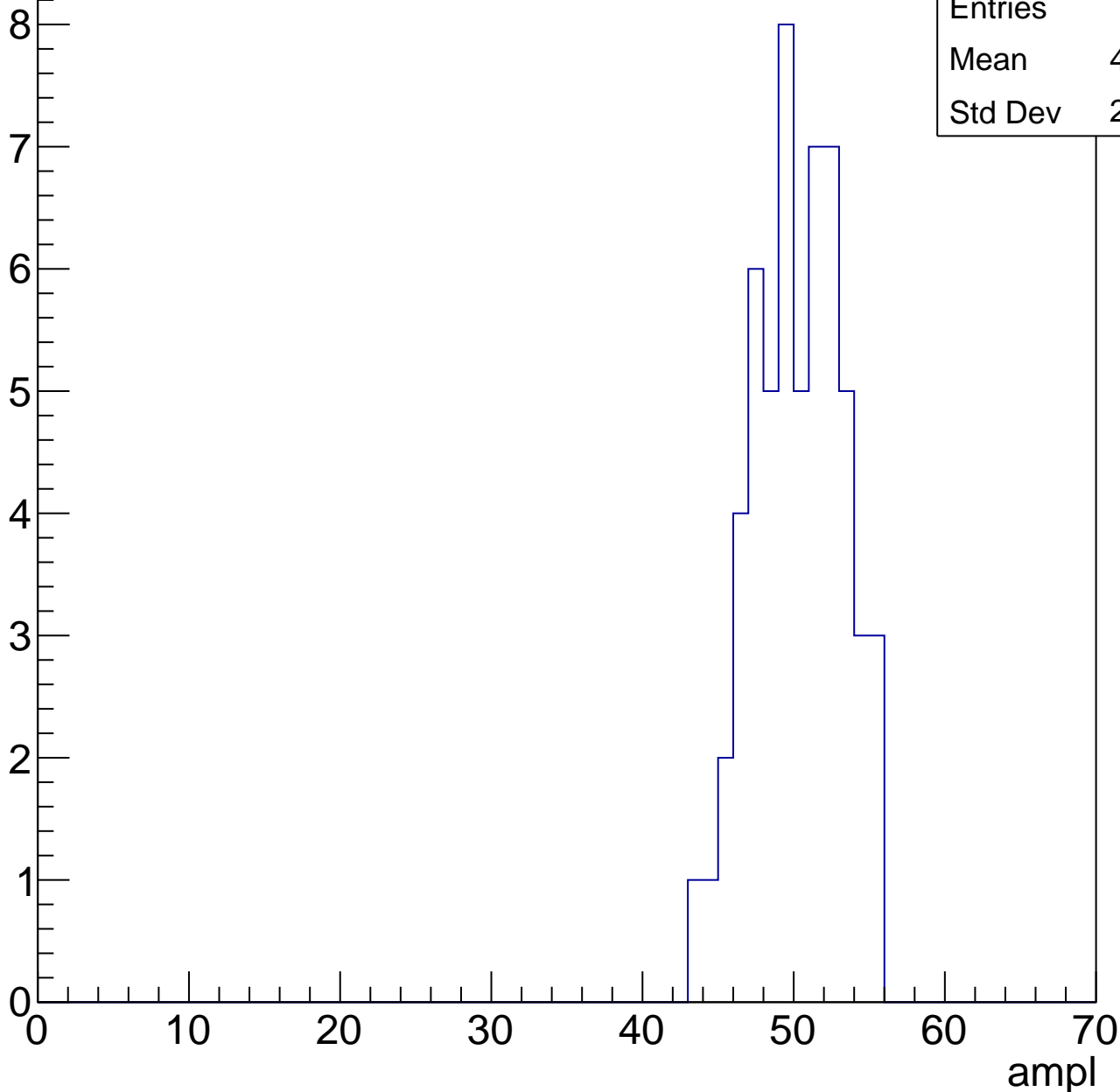


# B1L003S, U6-ch69, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	49.79
Std Dev	2.906



# B1L003S, U6-ch69, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

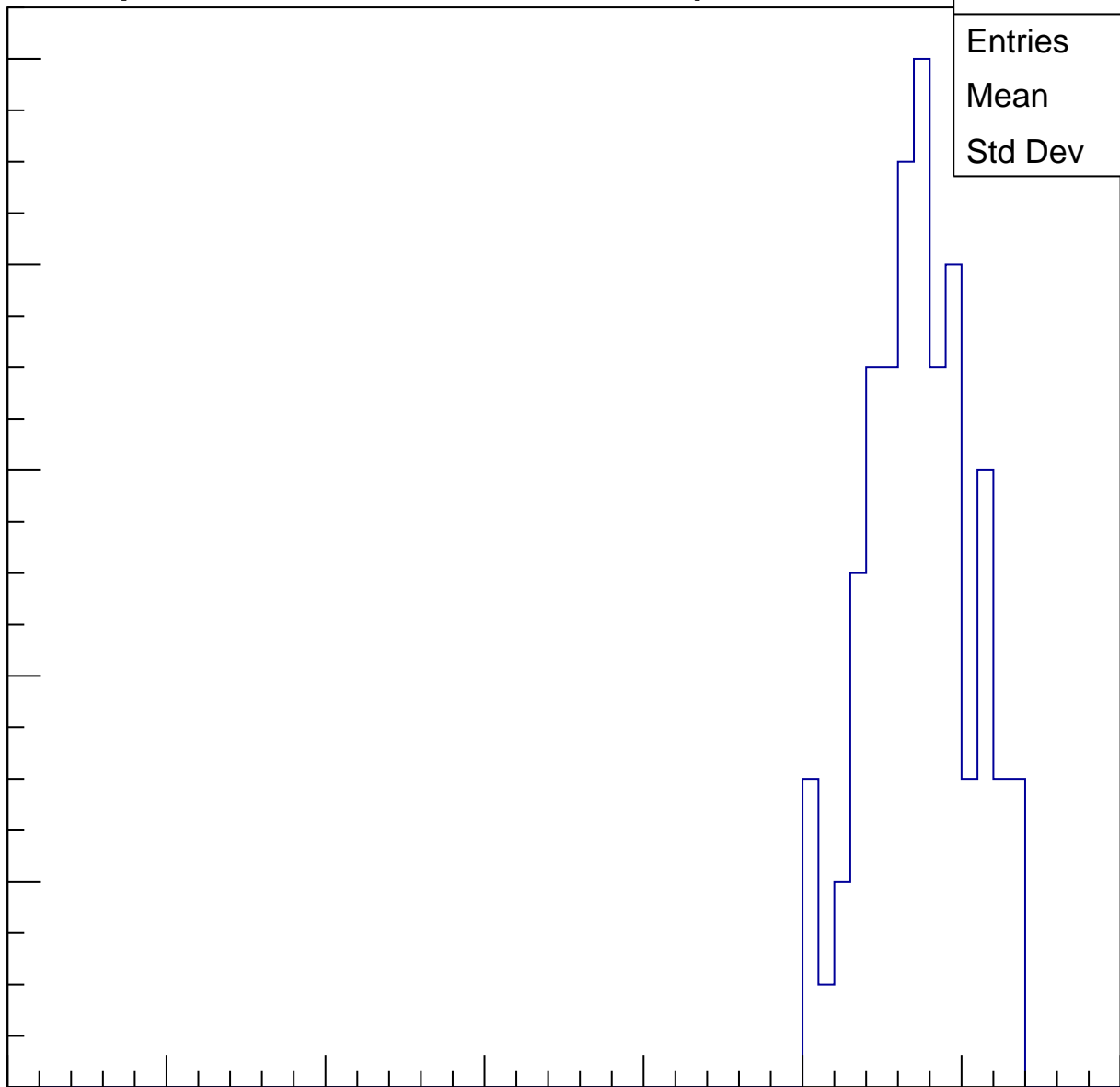
Entries	74
Mean	56.84
Std Dev	3.196

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

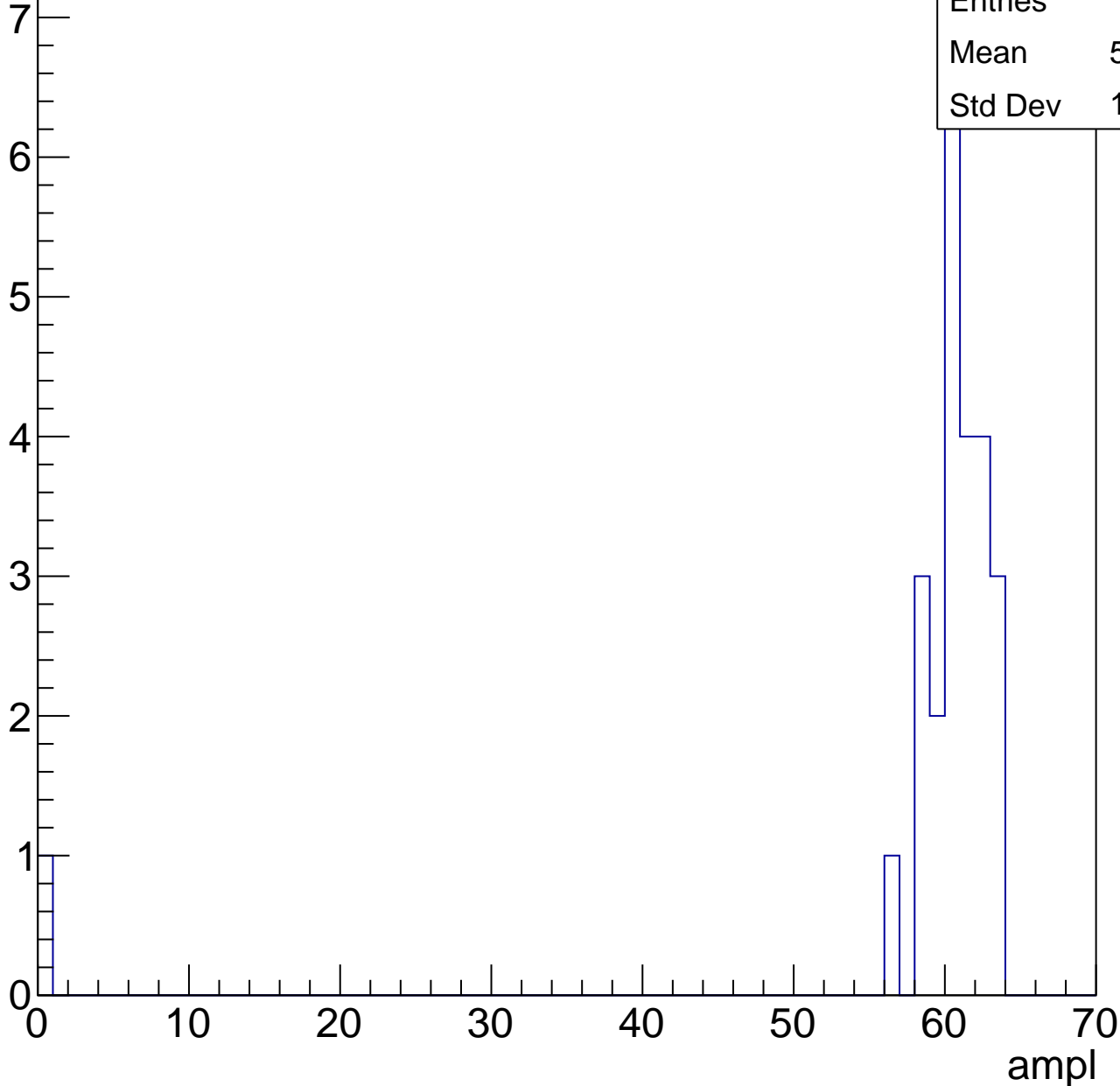


# B1L003S, U6-ch69, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

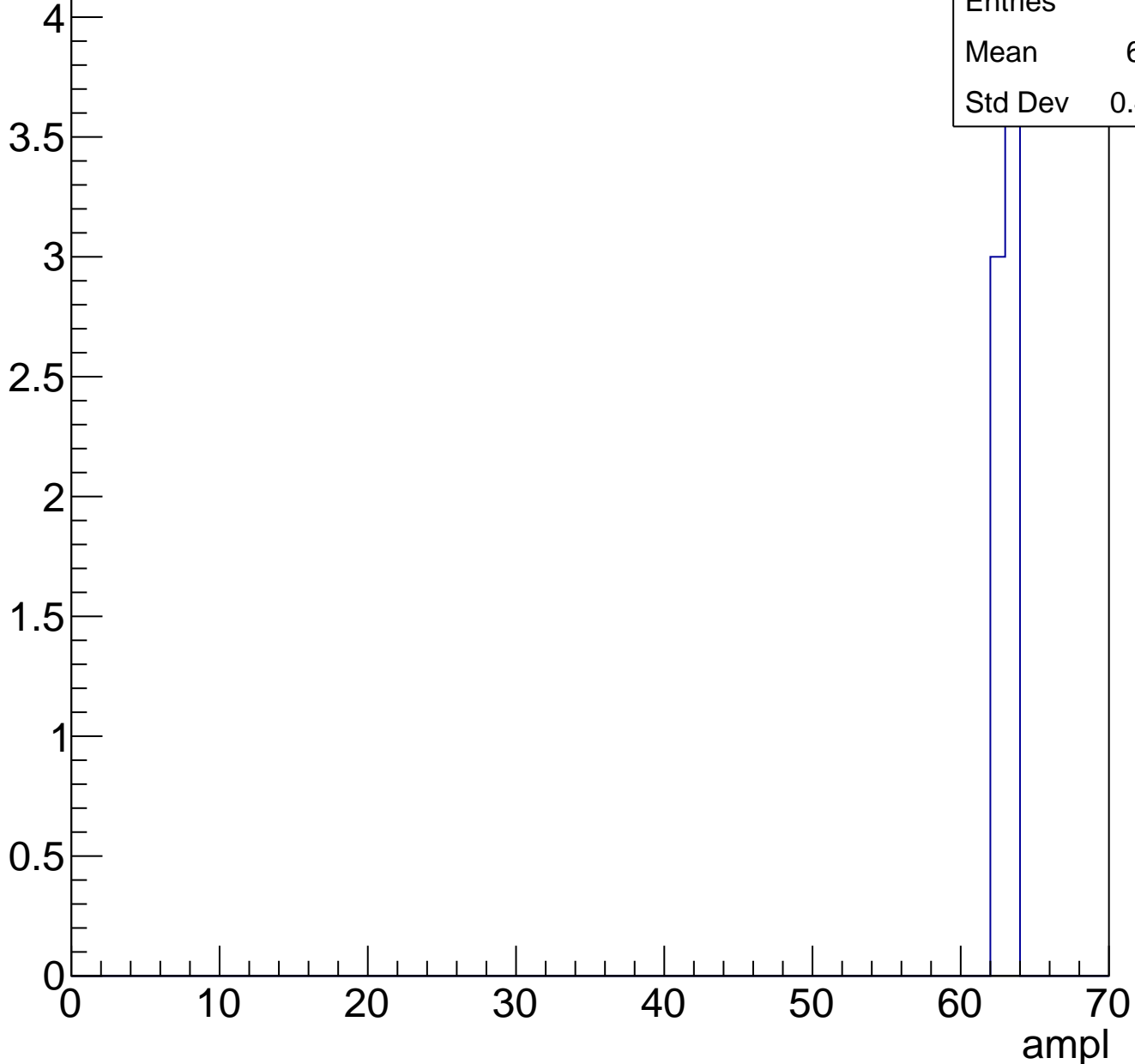
Entries	25
Mean	57.96
Std Dev	11.95



# B1L003S, U6-ch69, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch69, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U6-ch70, adc0

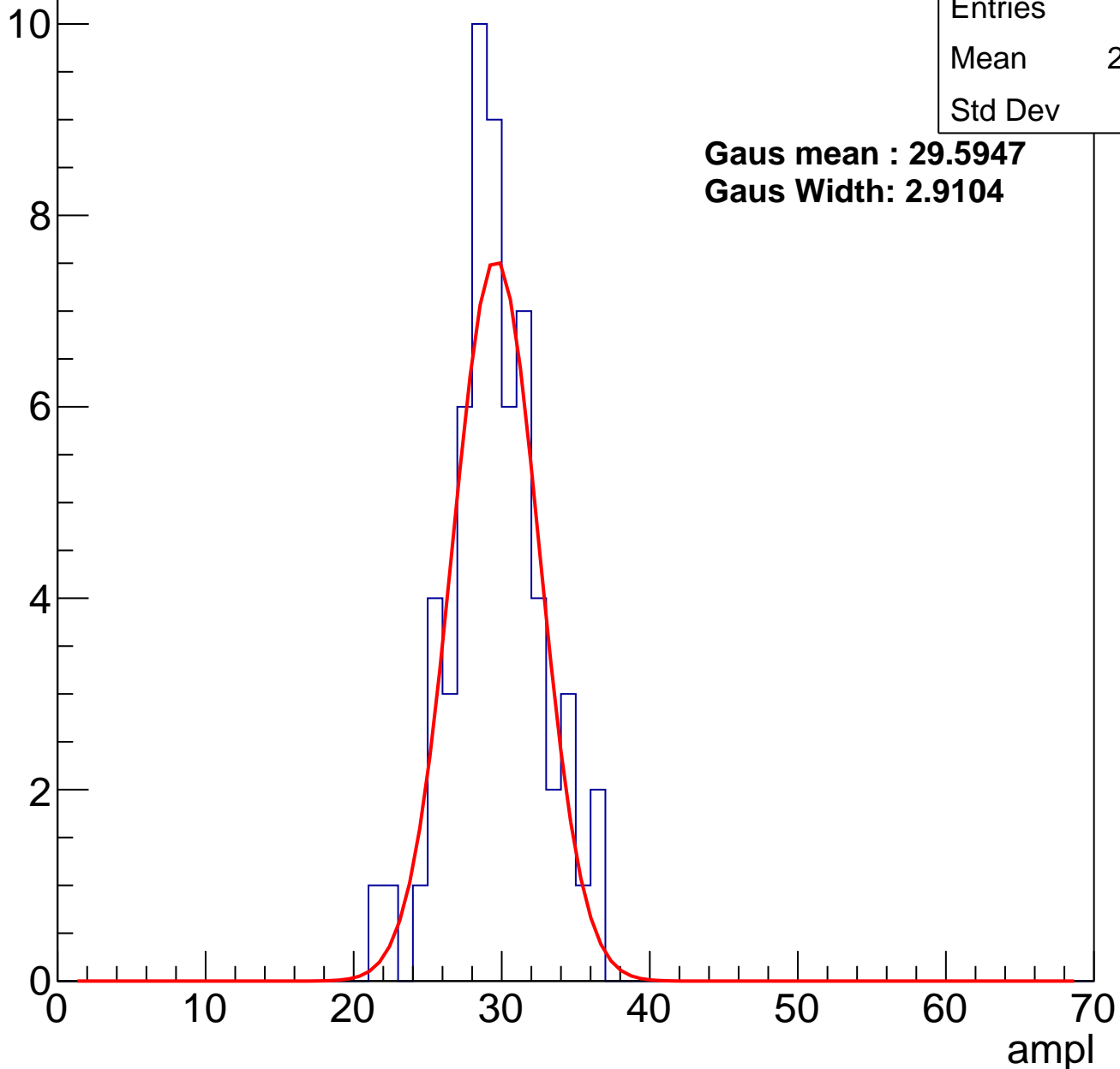
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	60
Mean	29.13
Std Dev	3.09

**Gaus mean : 29.5947**

**Gaus Width: 2.9104**

Entry



# B1L003S, U6-ch70, adc1

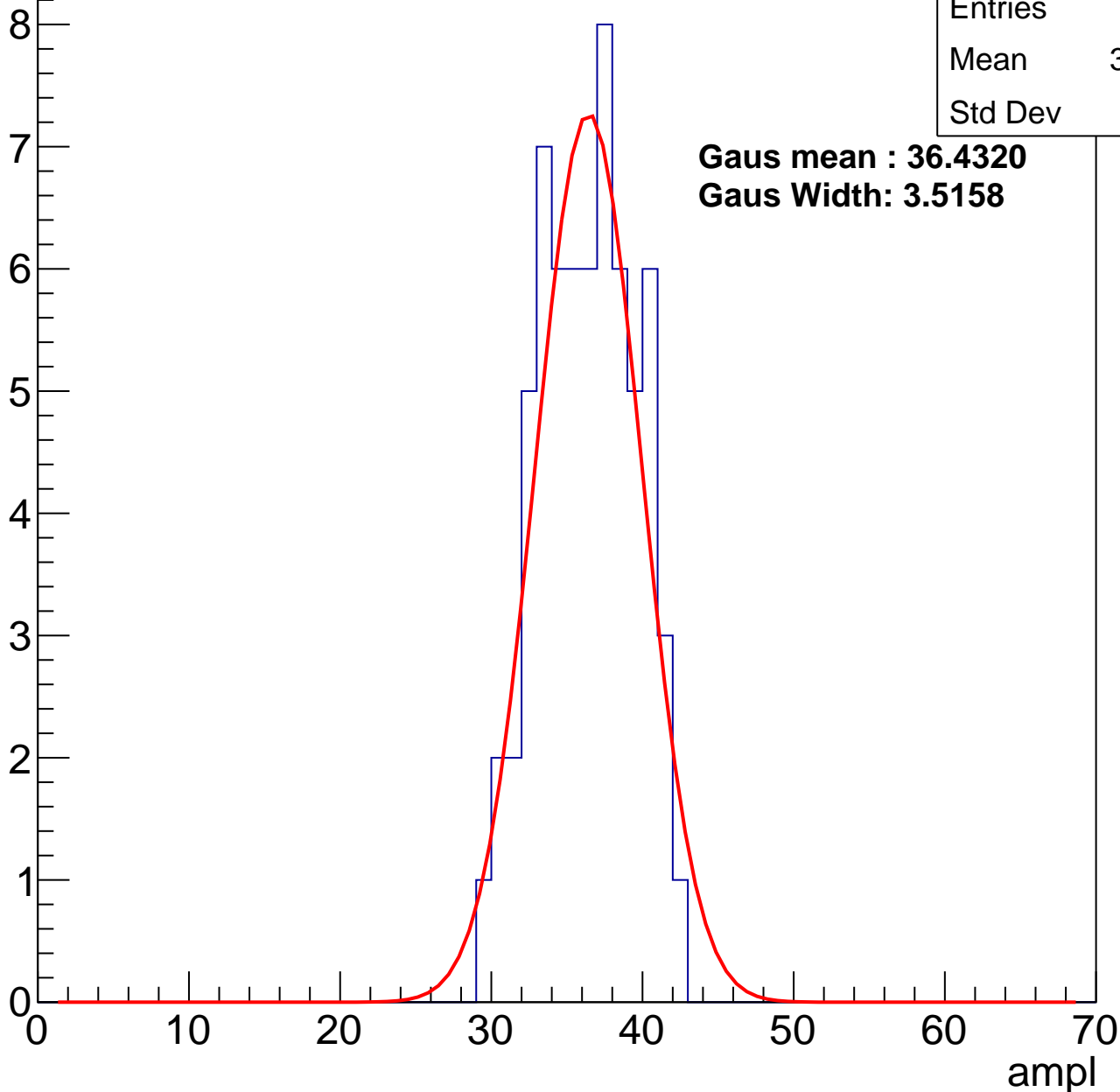
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	35.88
Std Dev	3.13

**Gaus mean : 36.4320**

**Gaus Width: 3.5158**



# B1L003S, U6-ch70, adc2

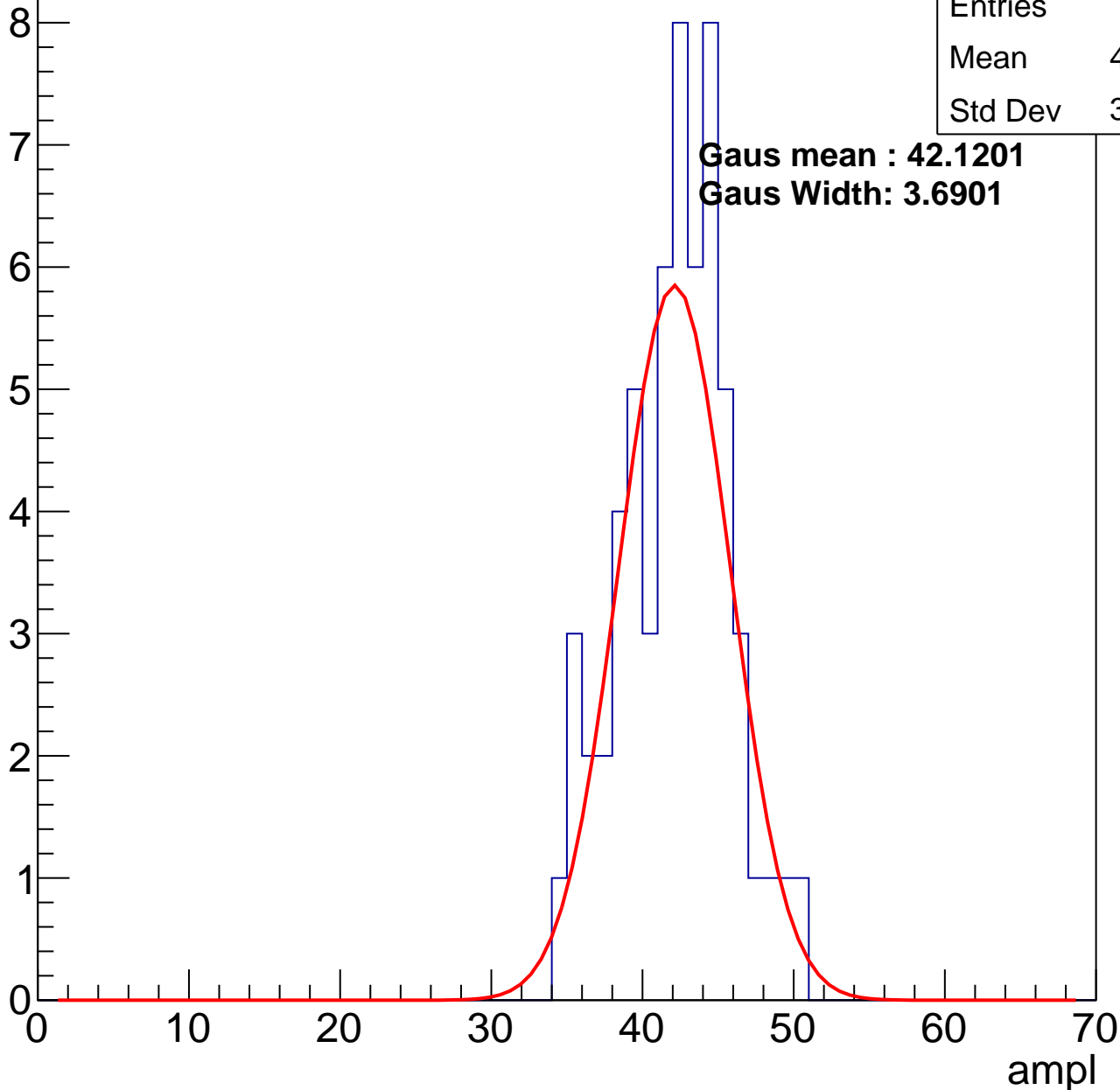
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	41.68
Std Dev	3.557

**Gaus mean : 42.1201**

**Gaus Width: 3.6901**

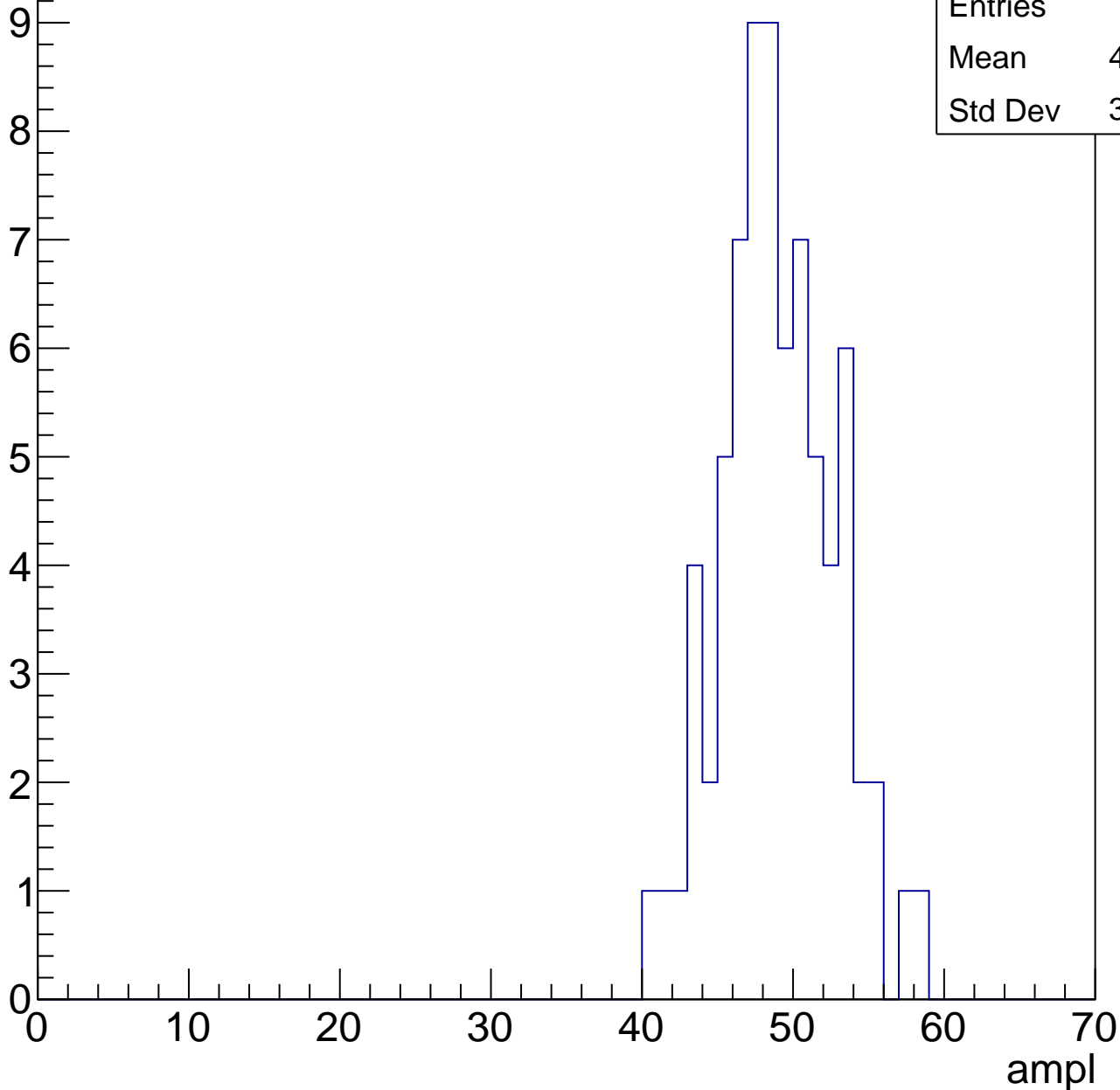


# B1L003S, U6-ch70, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

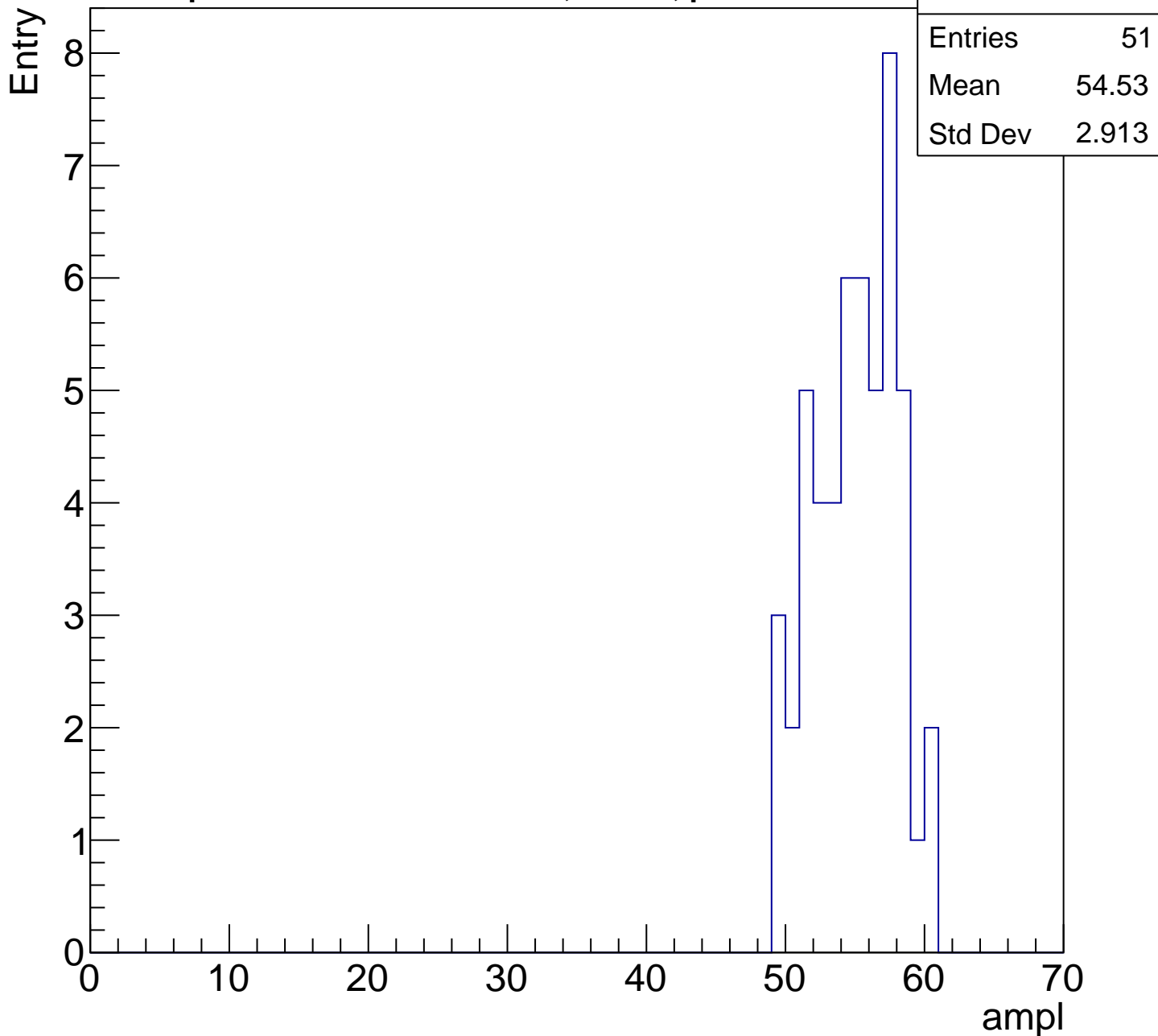
Entry

Entries	73
Mean	48.53
Std Dev	3.675



# B1L003S, U6-ch70, adc4

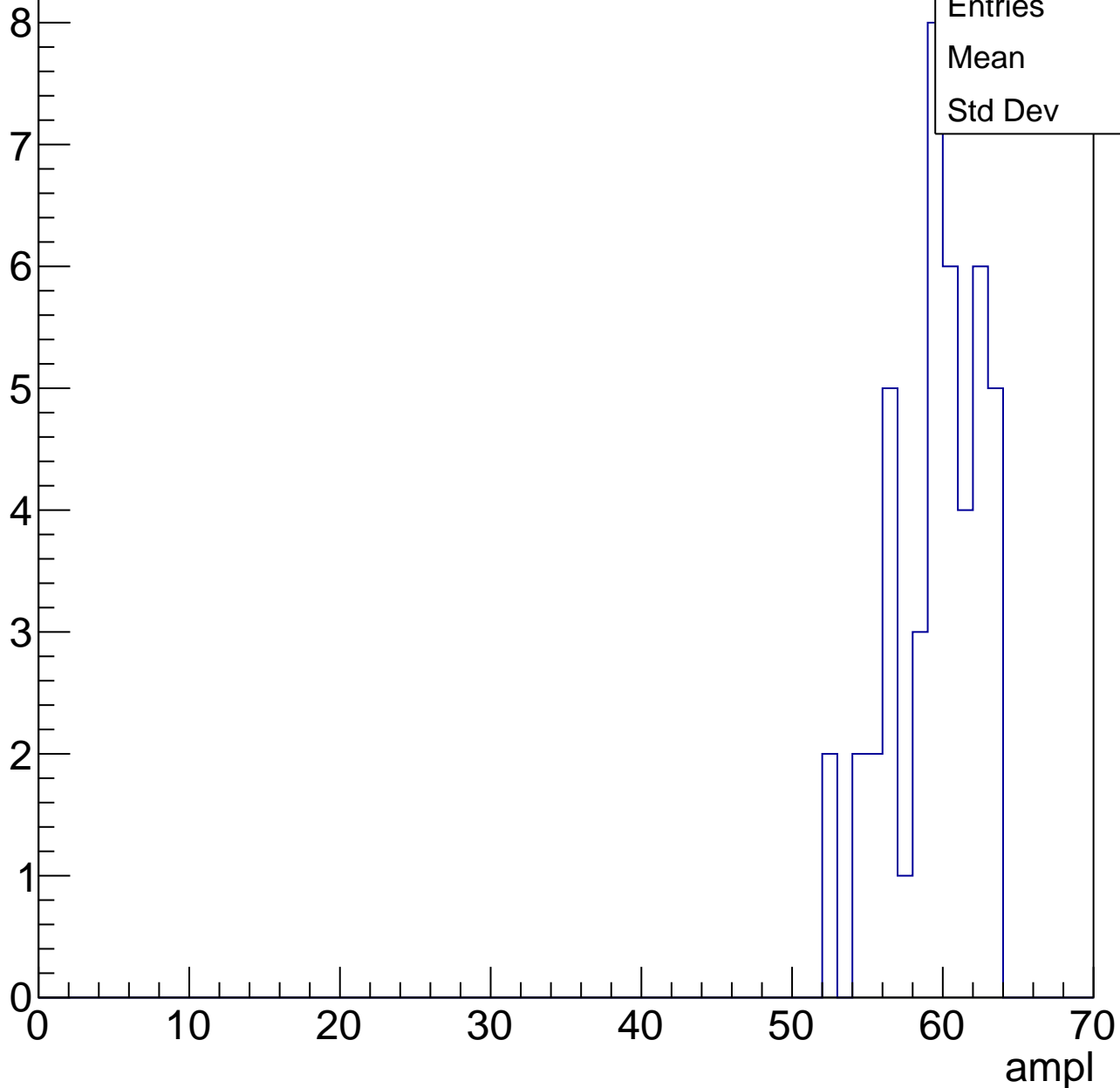
calib\_packv5\_042523\_0143.root, FC#13, port D2



# B1L003S, U6-ch70, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



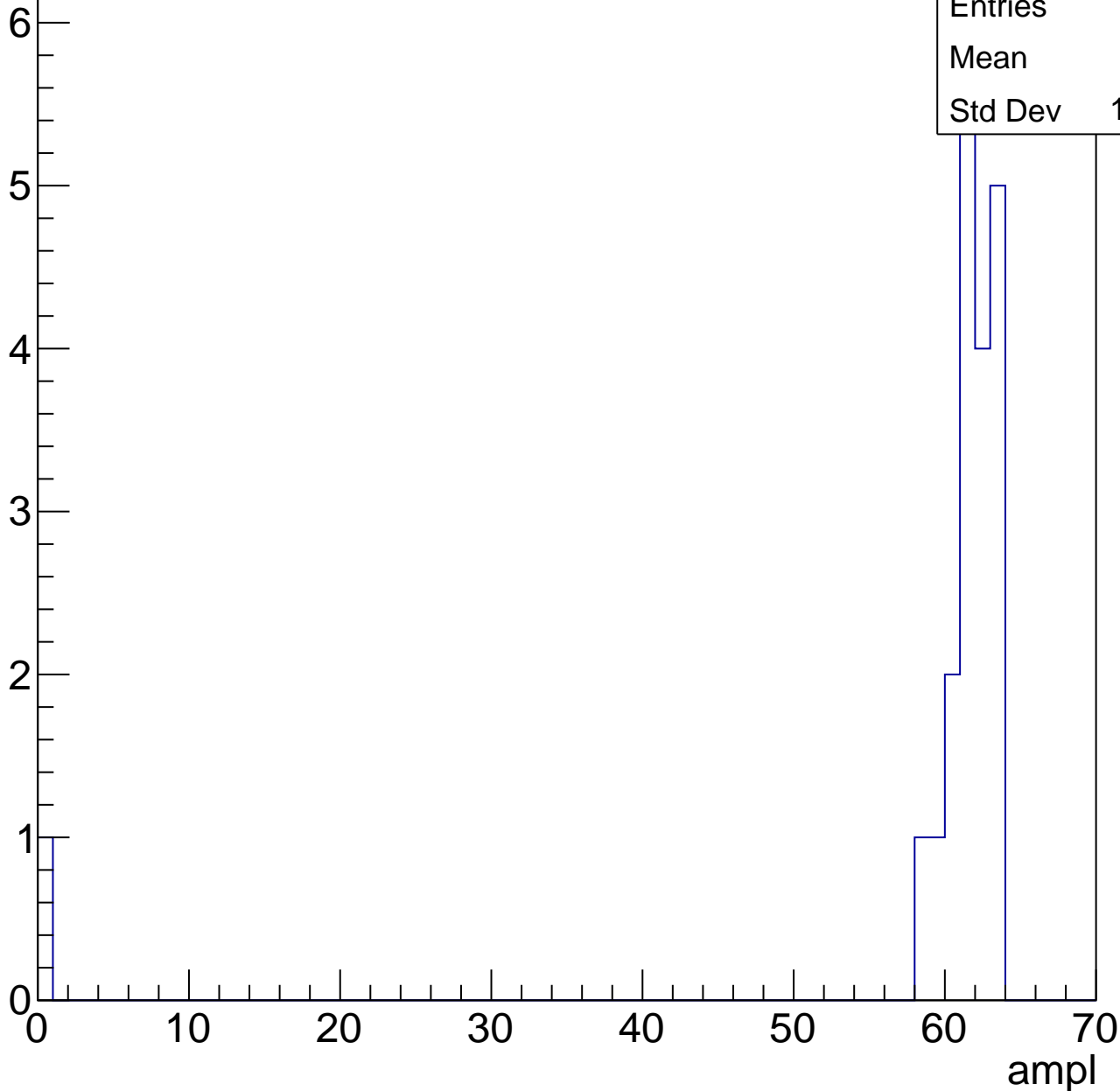
Entries	44
Mean	59
Std Dev	2.97

# B1L003S, U6-ch70, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	20
Mean	58.3
Std Dev	13.44





# B1L003S, U6-ch70, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L003S, U6-ch71, adc0

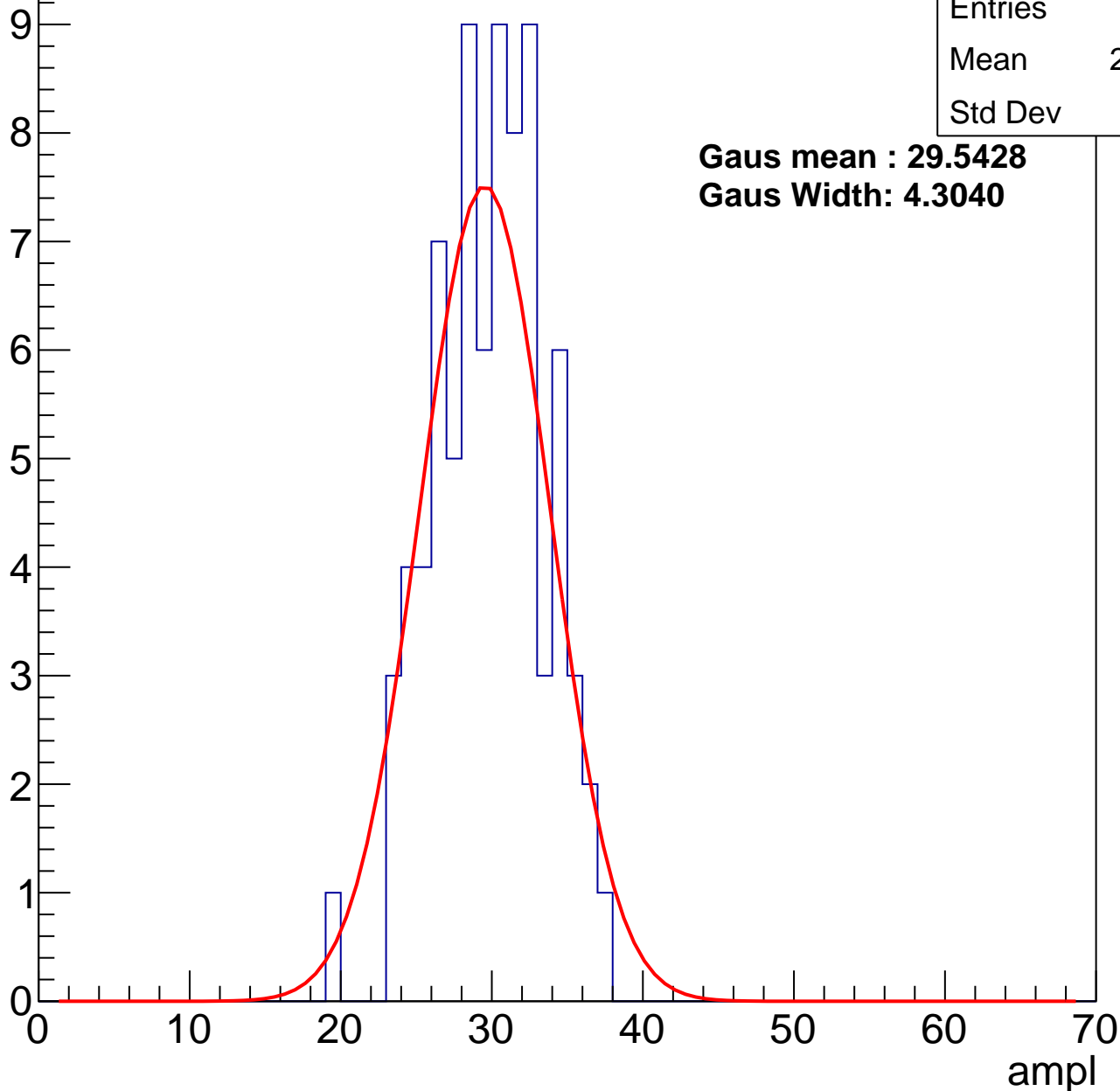
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	80
Mean	29.38
Std Dev	3.61

**Gaus mean : 29.5428**

**Gaus Width: 4.3040**



# B1L003S, U6-ch71, adc1

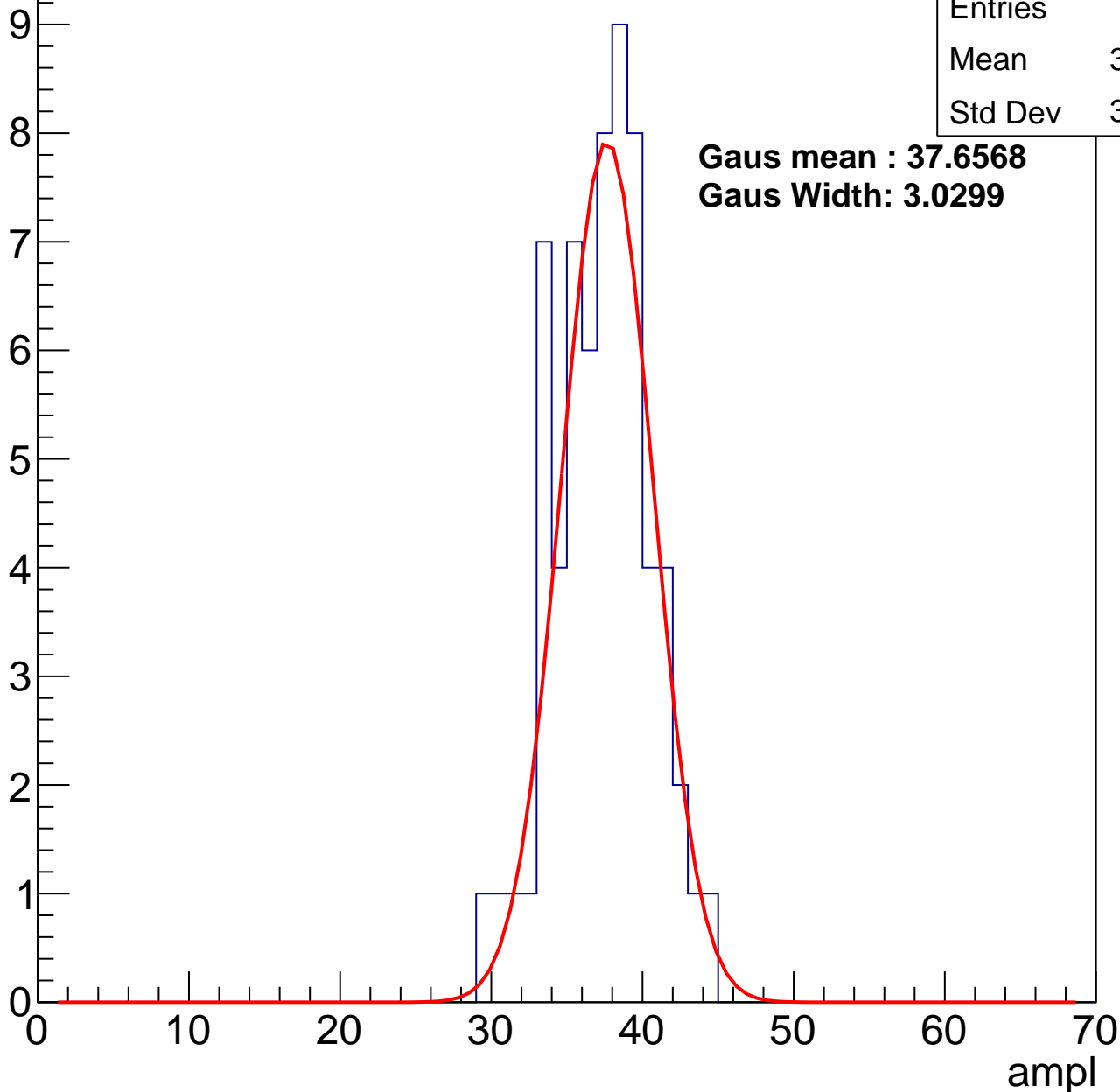
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	36.85
Std Dev	3.114

**Gaus mean : 37.6568**

**Gaus Width: 3.0299**



# B1L003S, U6-ch71, adc2

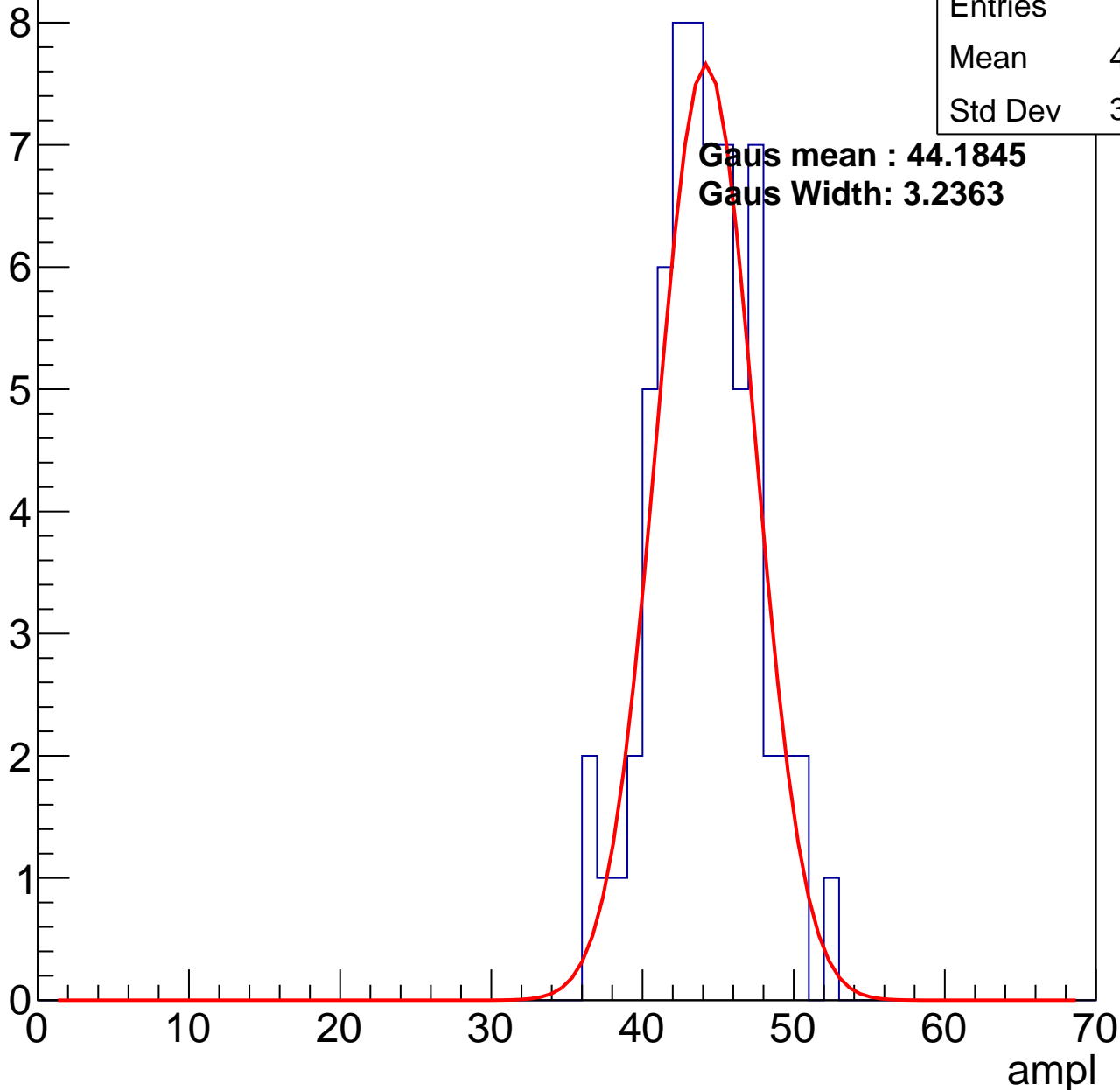
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	43.62
Std Dev	3.338

**Gaus mean : 44.1845**

**Gaus Width: 3.2363**

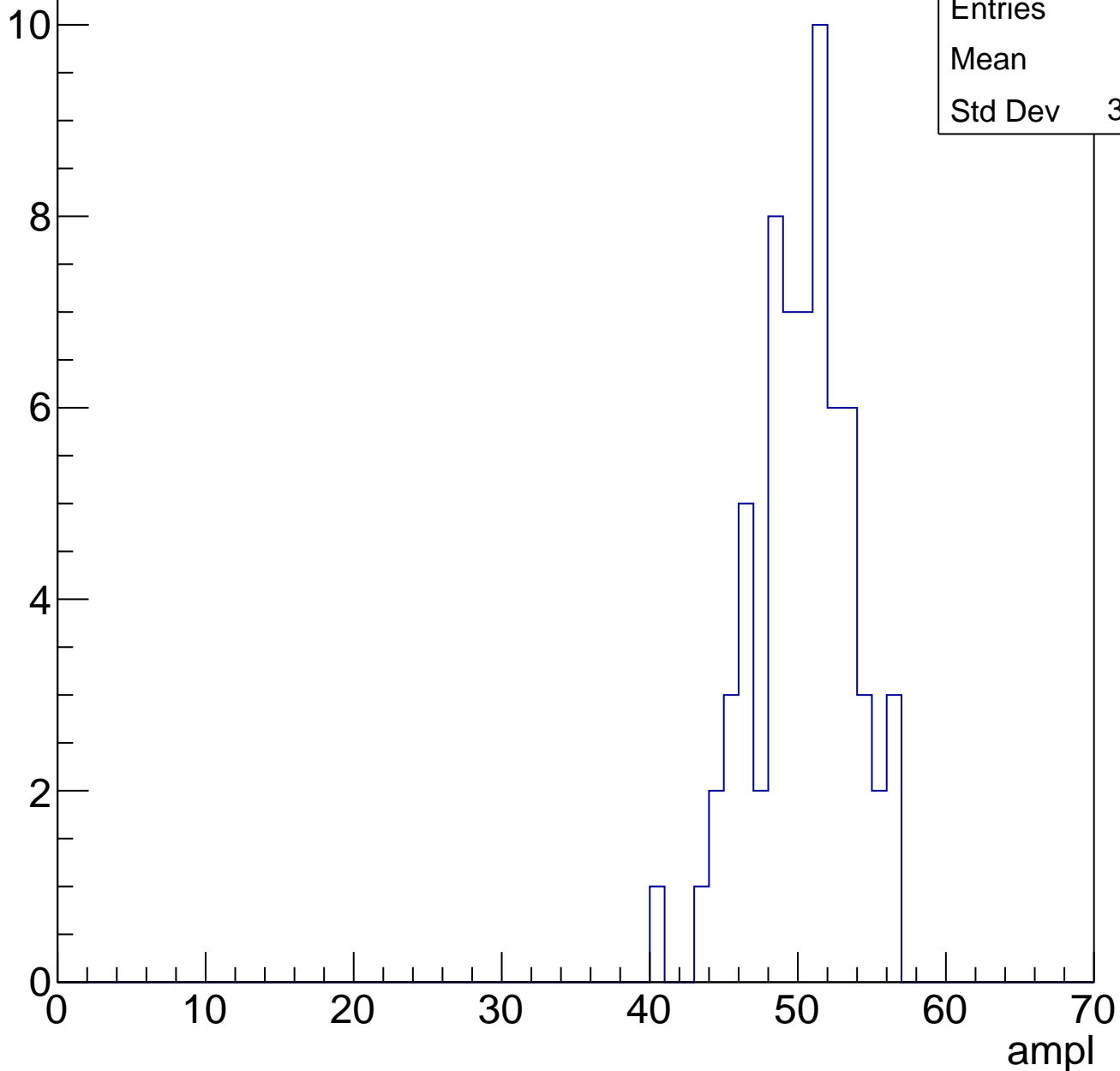


# B1L003S, U6-ch71, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

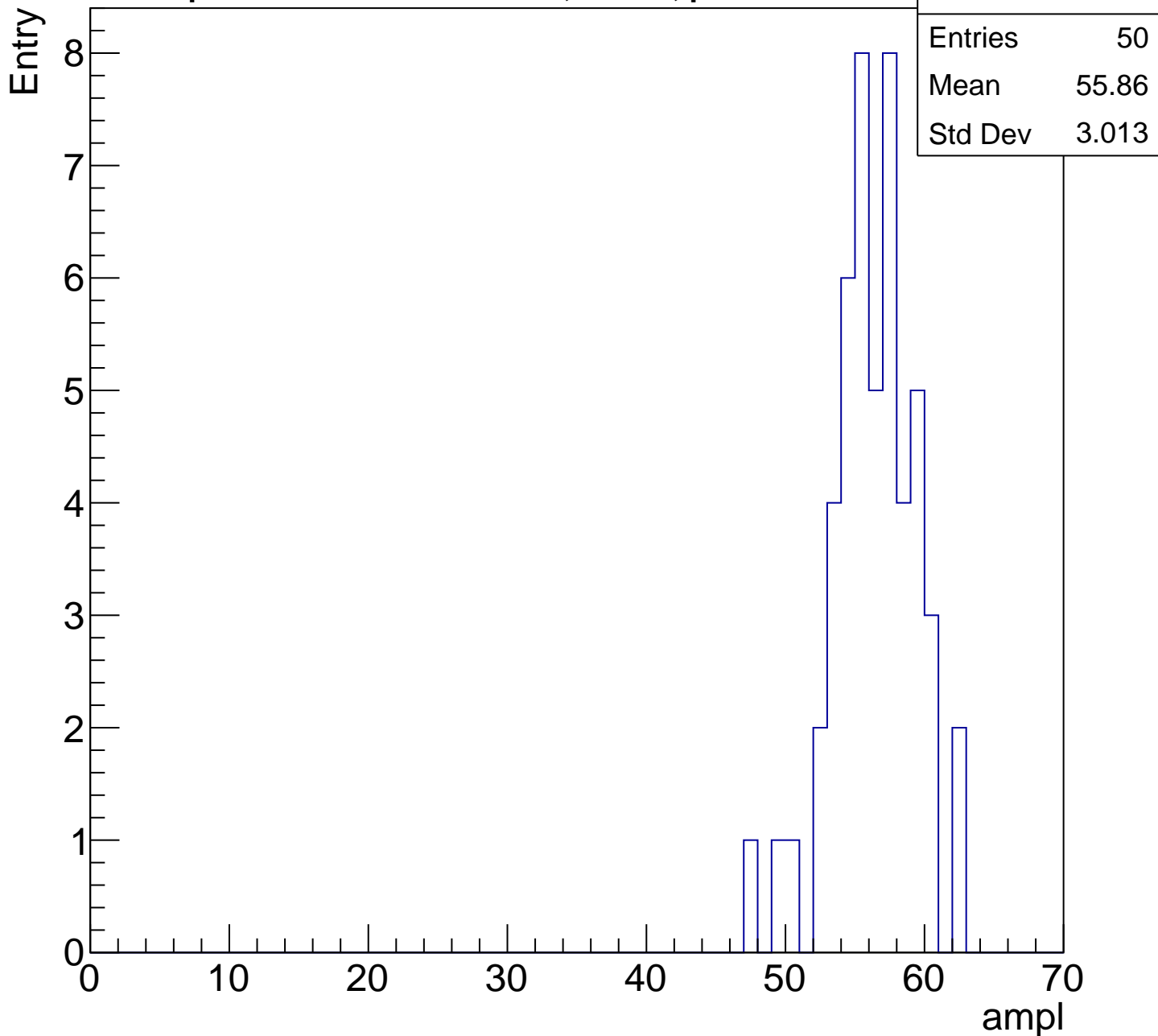
Entries	66
Mean	49.8
Std Dev	3.313

Entry



# B1L003S, U6-ch71, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

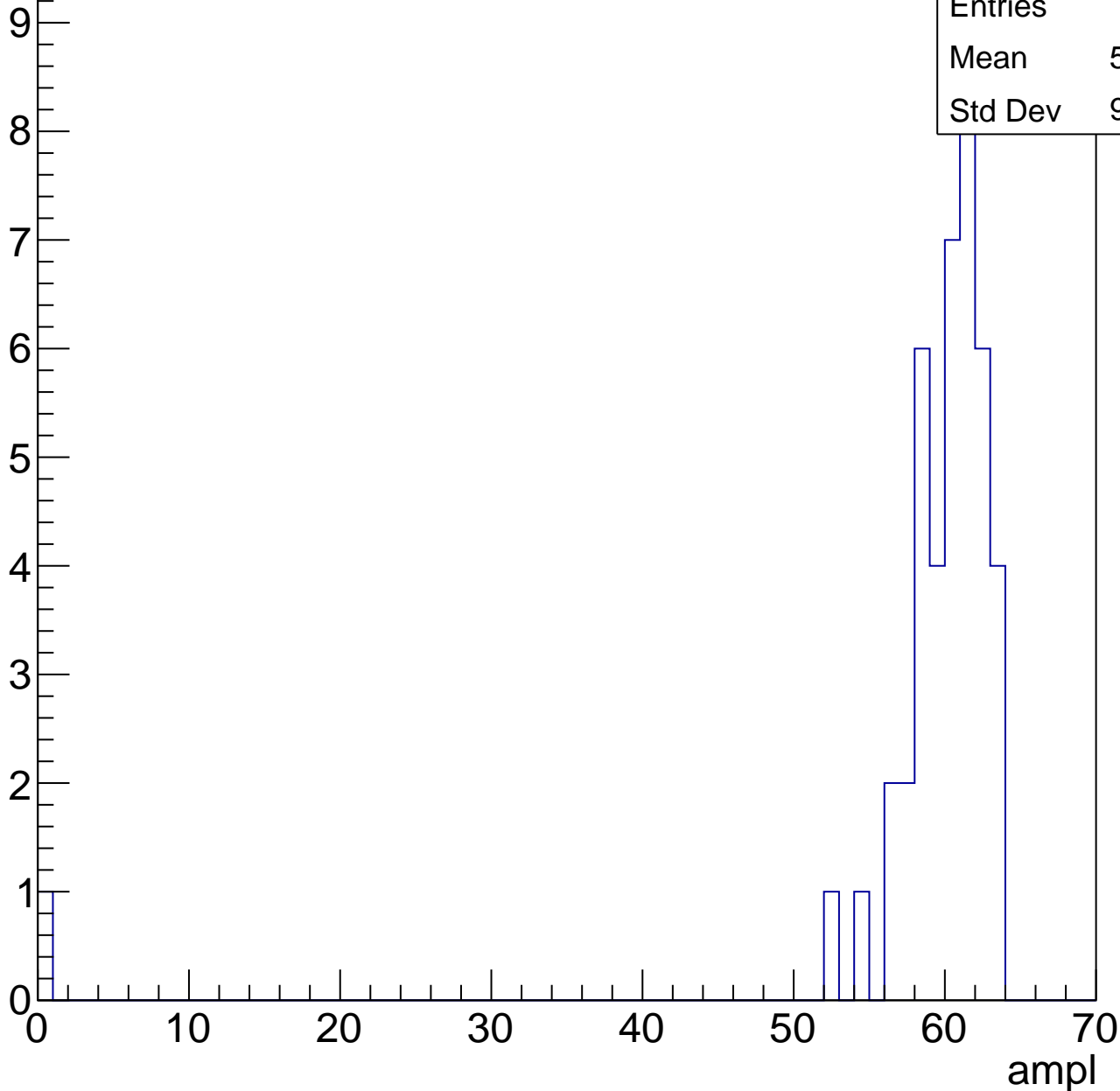


# B1L003S, U6-ch71, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	43
Mean	58.35
Std Dev	9.313

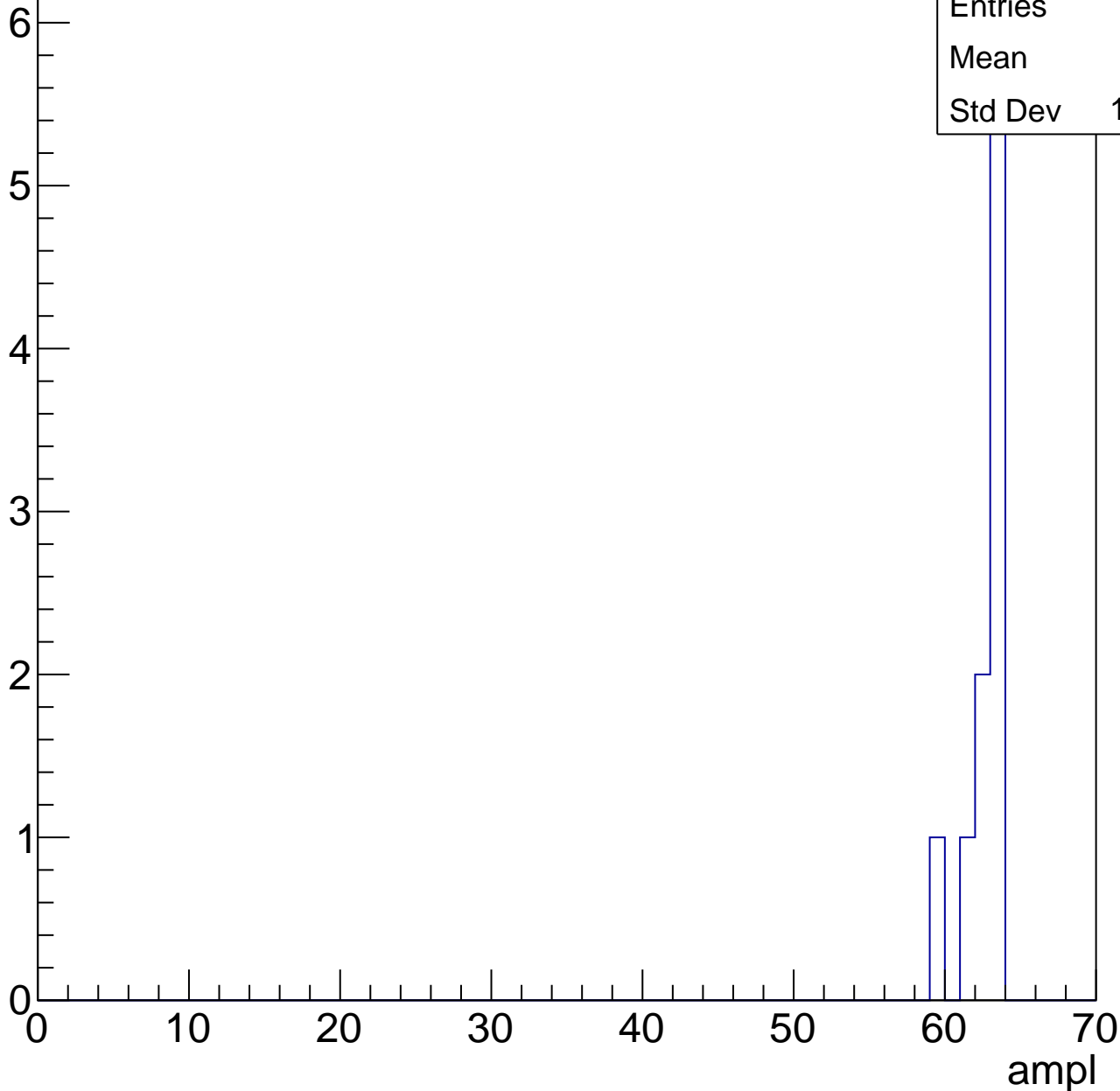


# B1L003S, U6-ch71, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	10
Mean	62.2
Std Dev	1.249





# B1L003S, U6-ch71, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U6-ch72, adc0

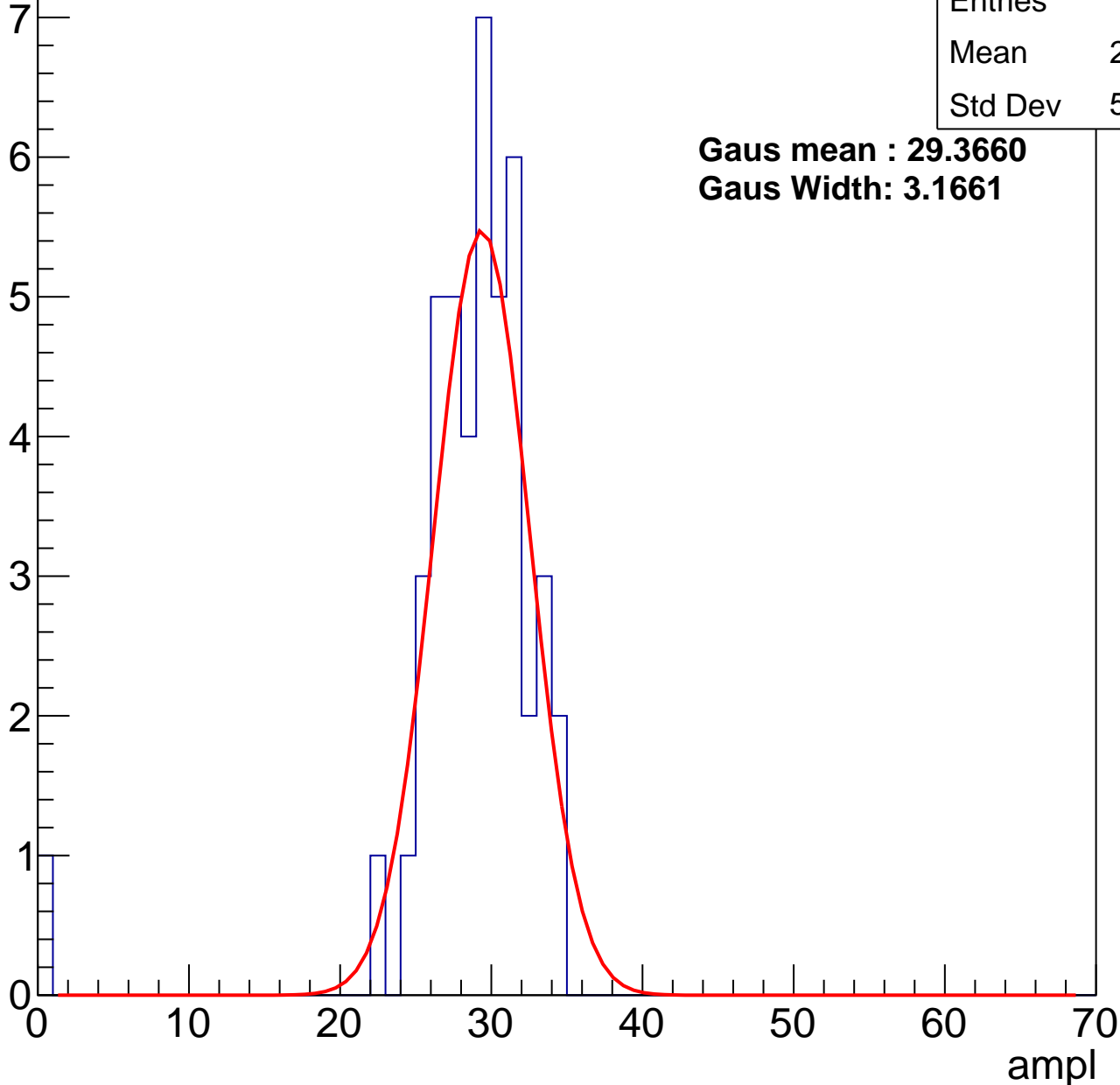
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	45
Mean	28.18
Std Dev	5.048

**Gaus mean : 29.3660**

**Gaus Width: 3.1661**



# B1L003S, U6-ch72, adc1

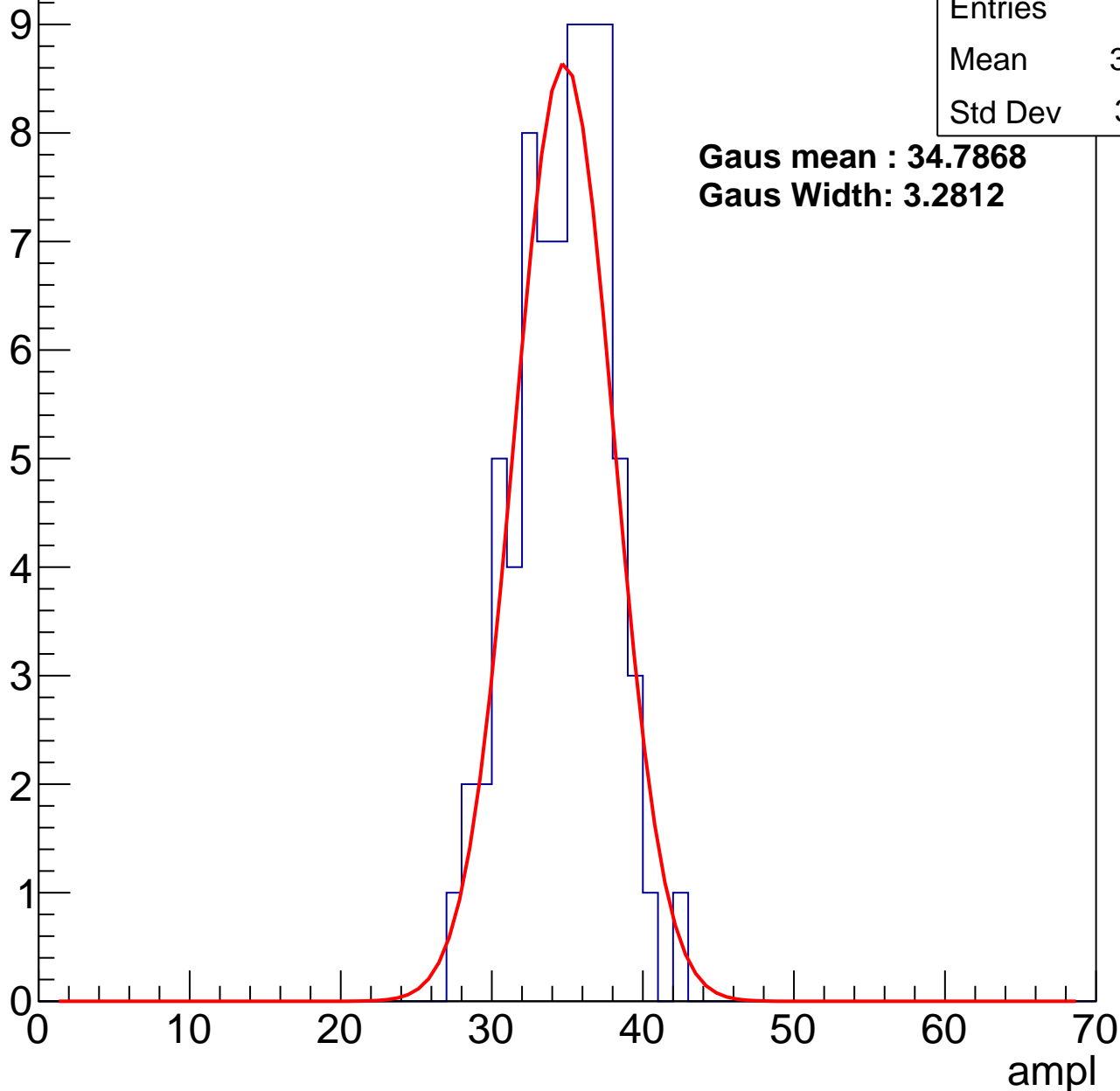
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	73
Mean	34.26
Std Dev	3.101

**Gaus mean : 34.7868**

**Gaus Width: 3.2812**



# B1L003S, U6-ch72, adc2

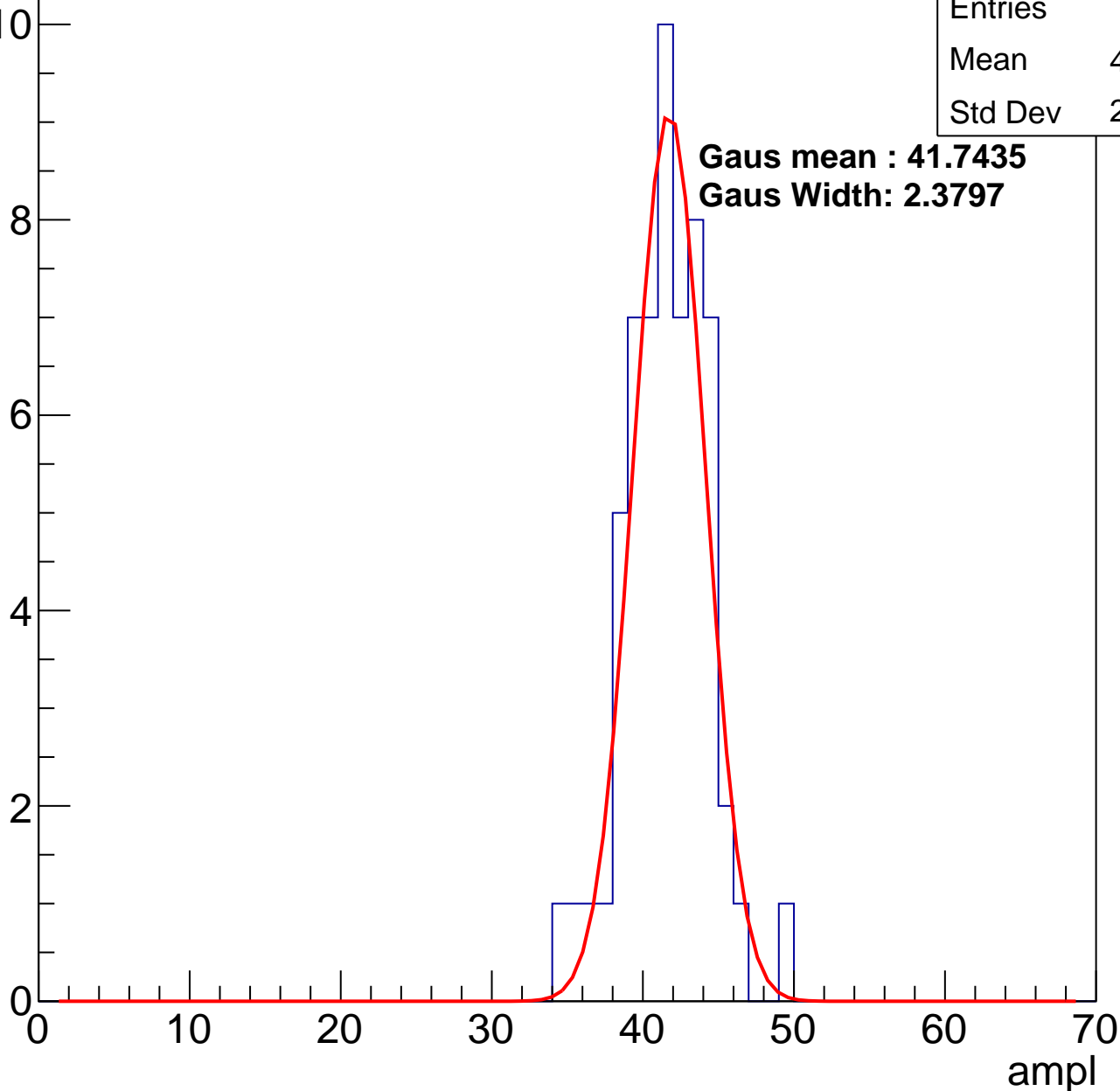
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	41.12
Std Dev	2.694

**Gaus mean : 41.7435**

**Gaus Width: 2.3797**

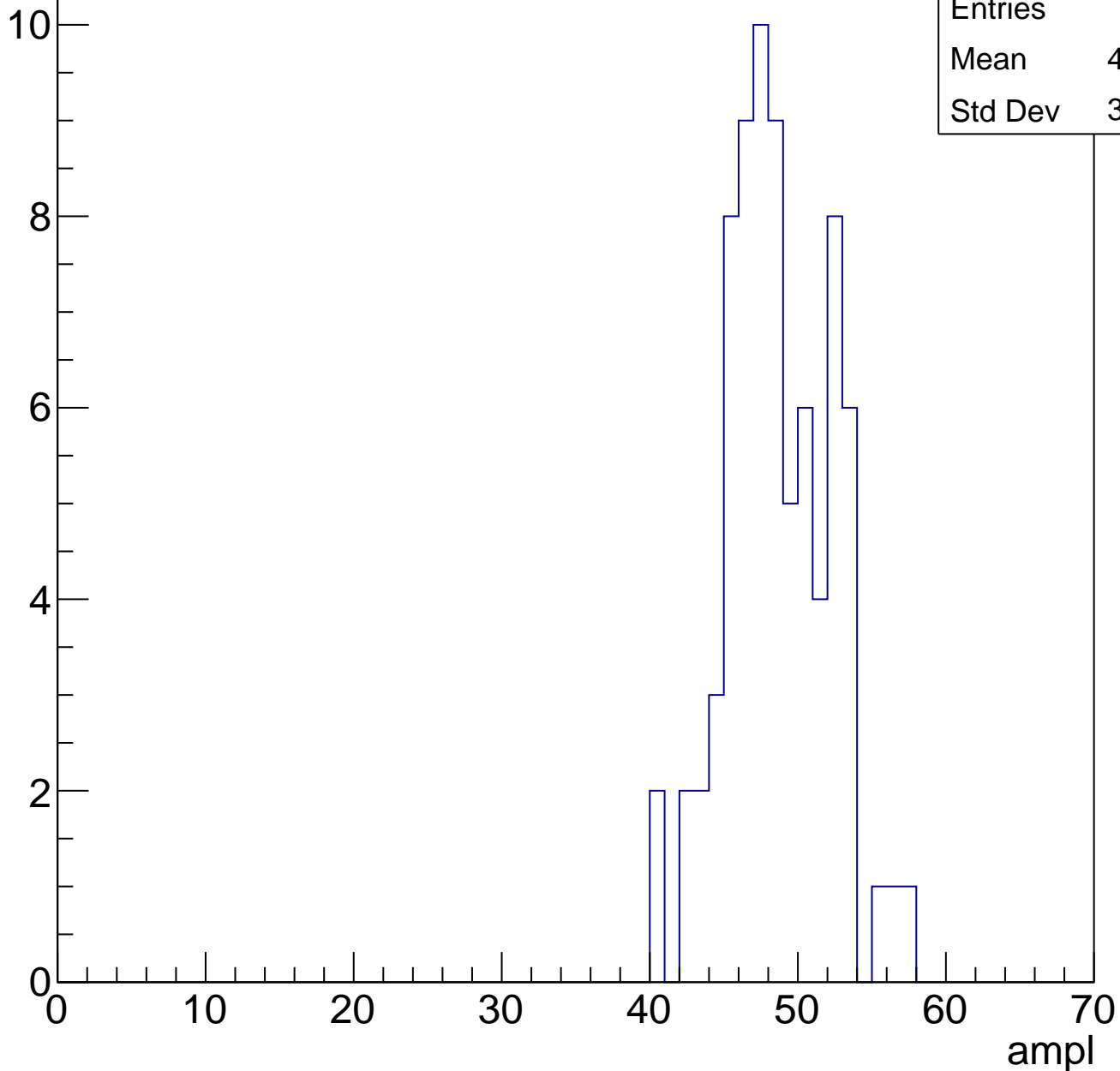


# B1L003S, U6-ch72, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	77
Mean	48.17
Std Dev	3.514

Entry

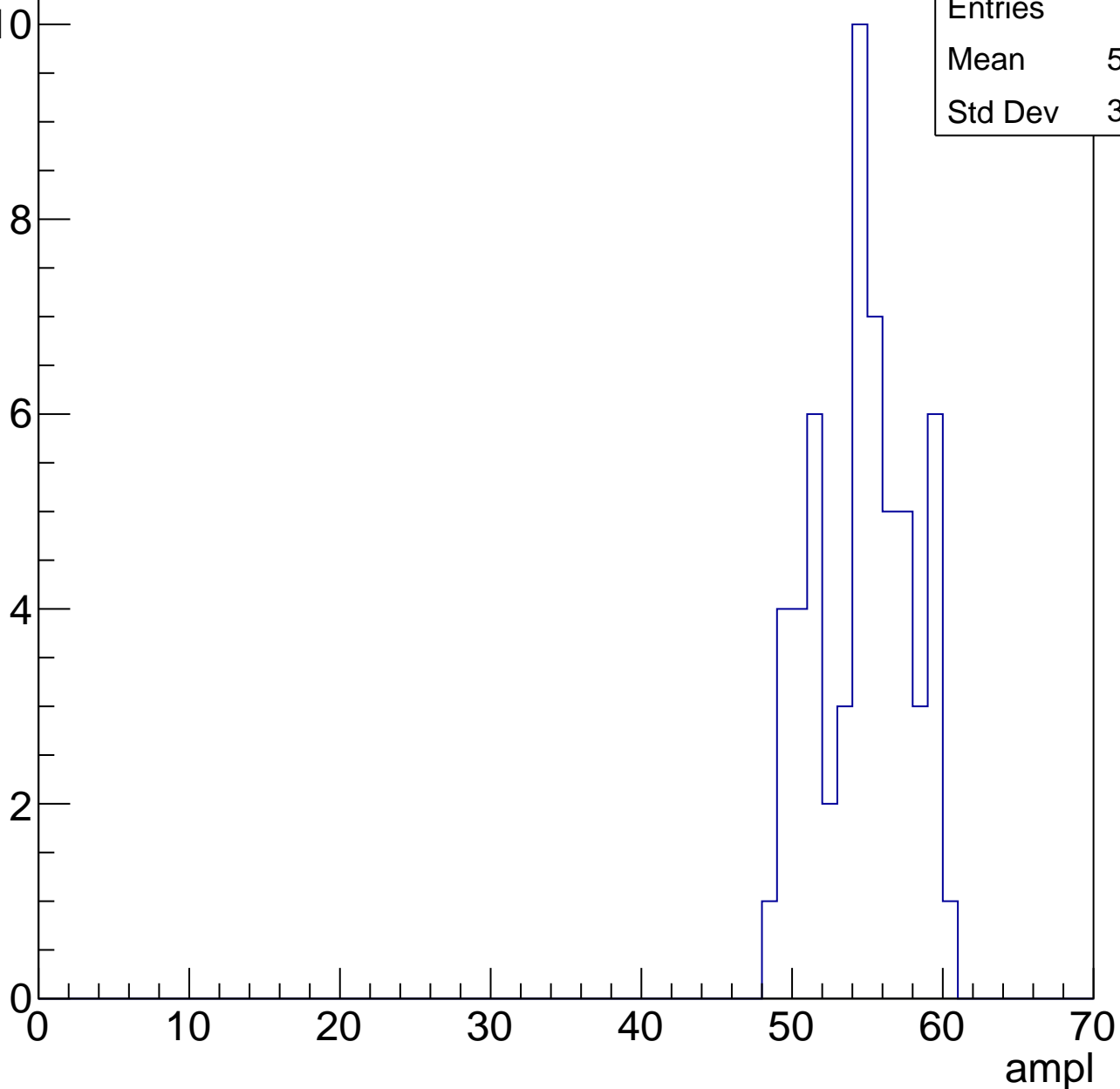


# B1L003S, U6-ch72, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	54.23
Std Dev	3.157

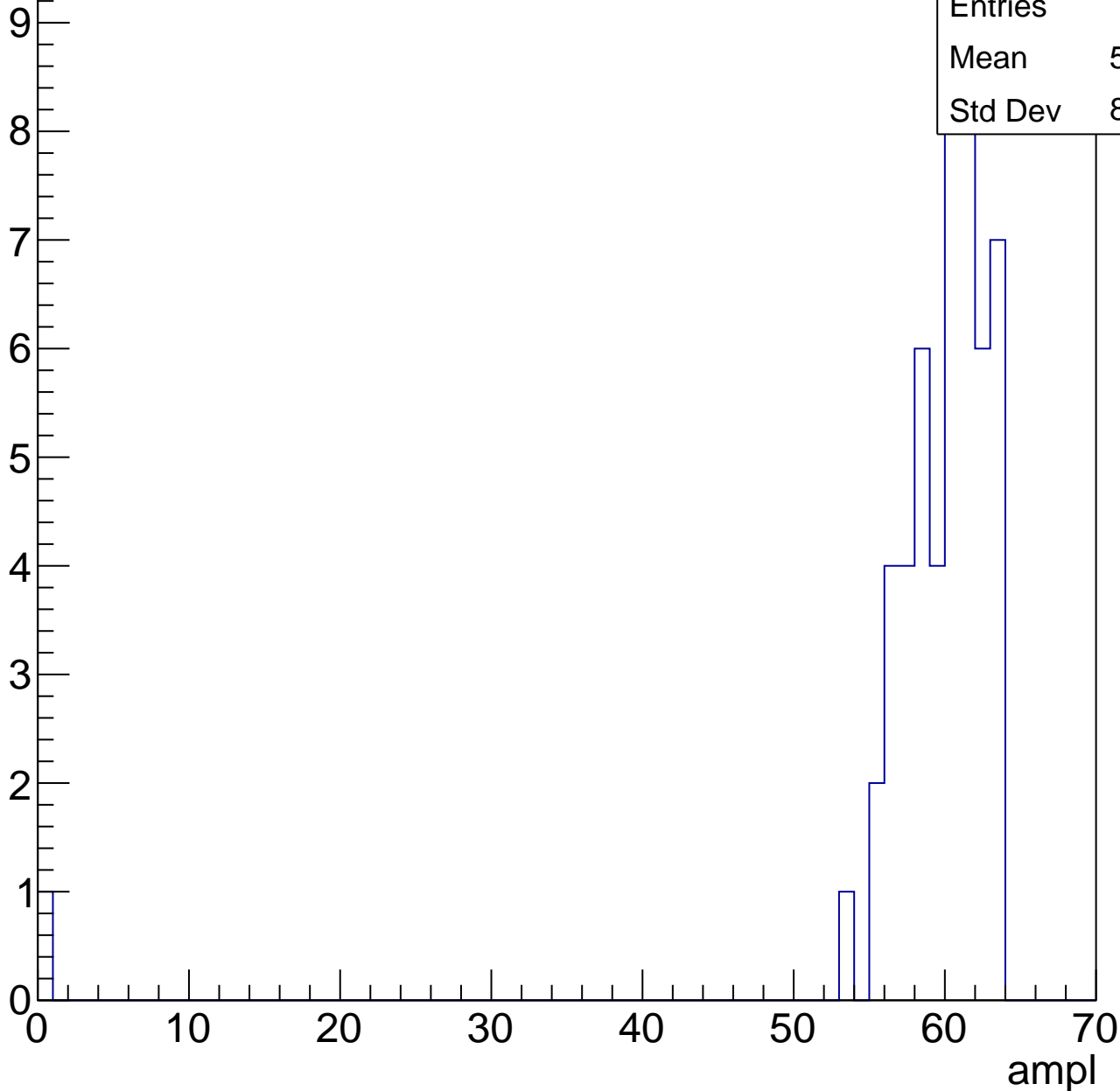


# B1L003S, U6-ch72, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

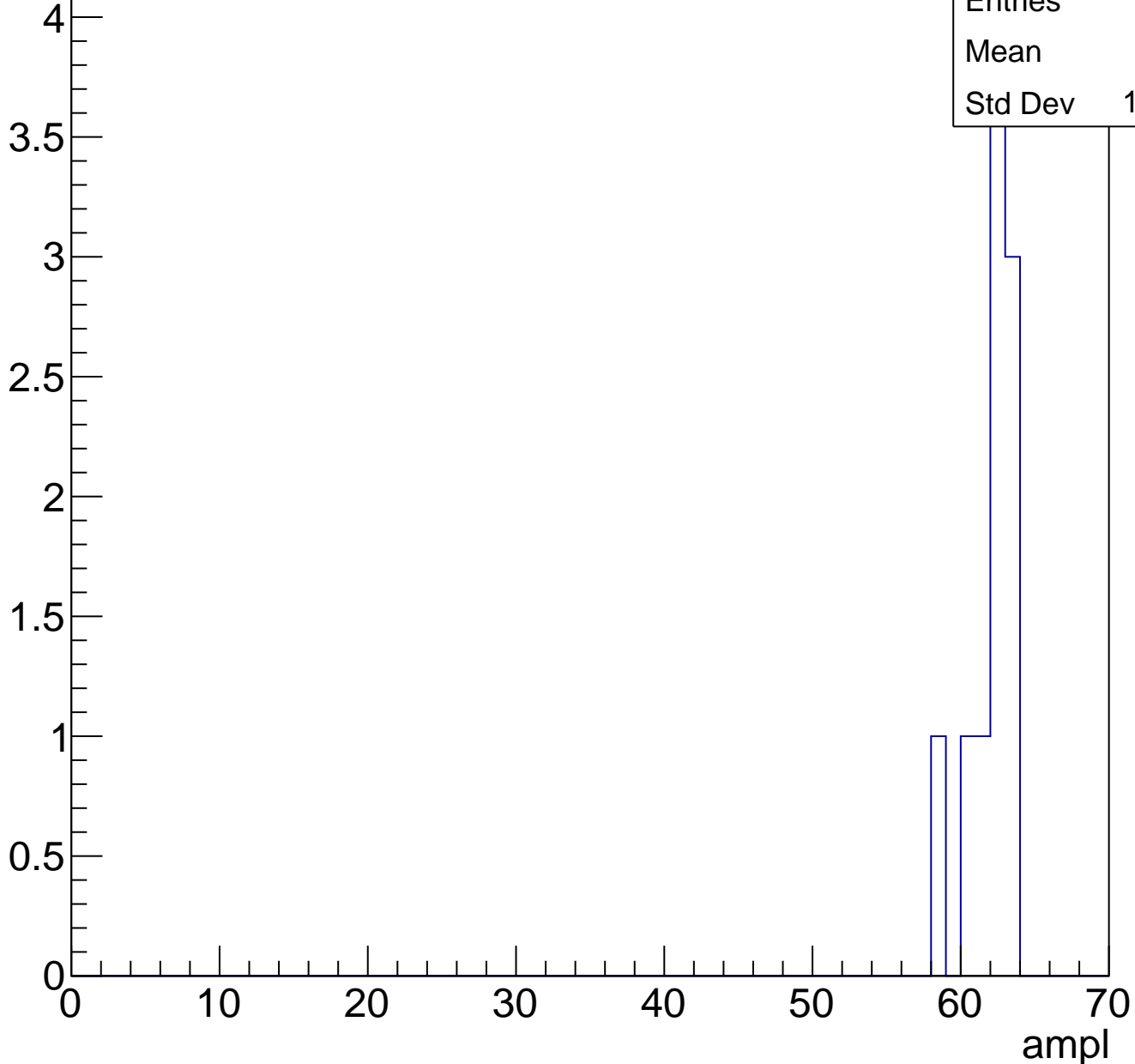
Entries	52
Mean	58.48
Std Dev	8.552



# B1L003S, U6-ch72, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



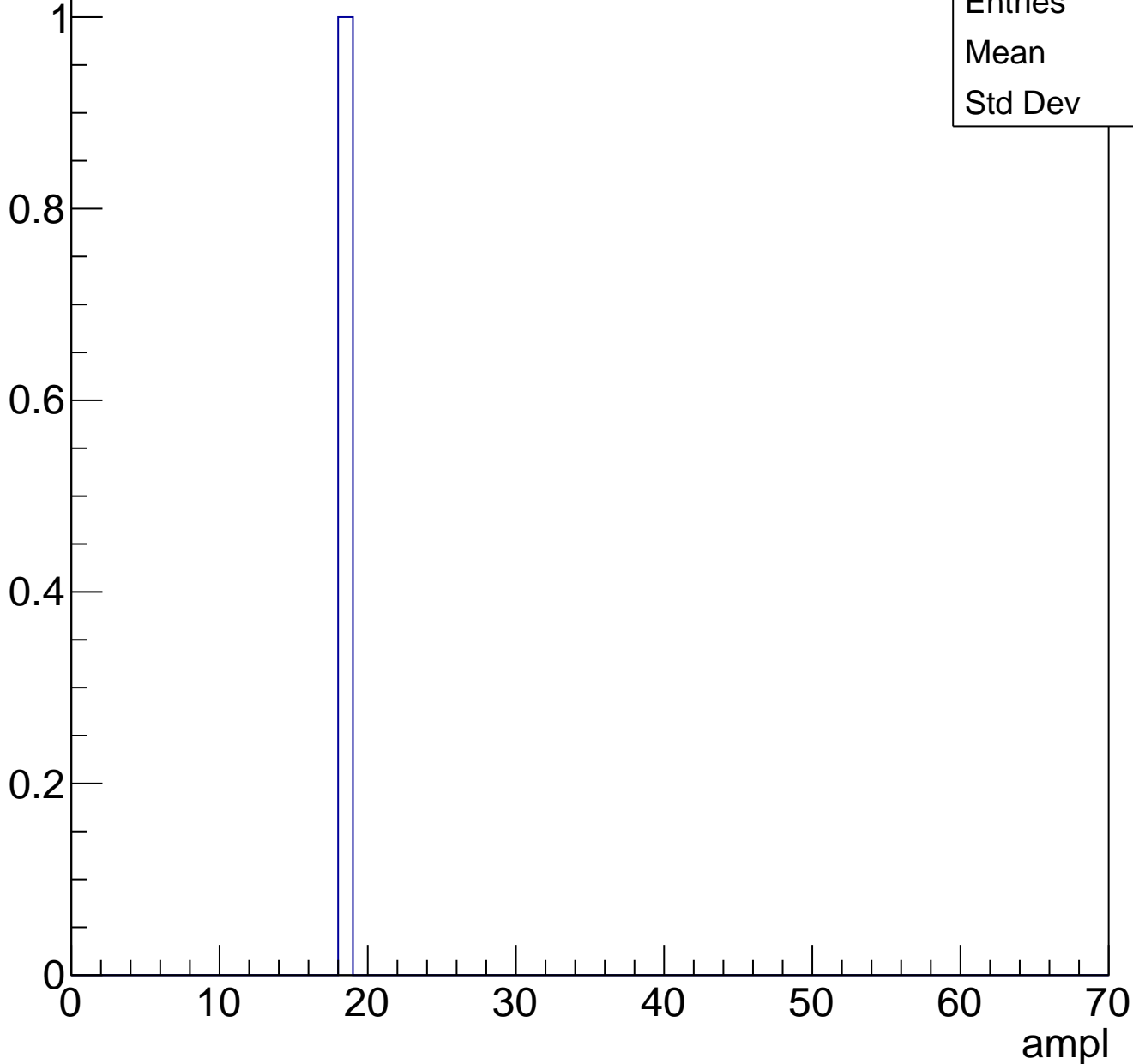
Entries	10
Mean	61.6
Std Dev	1.497



# B1L003S, U6-ch72, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch73, adc0

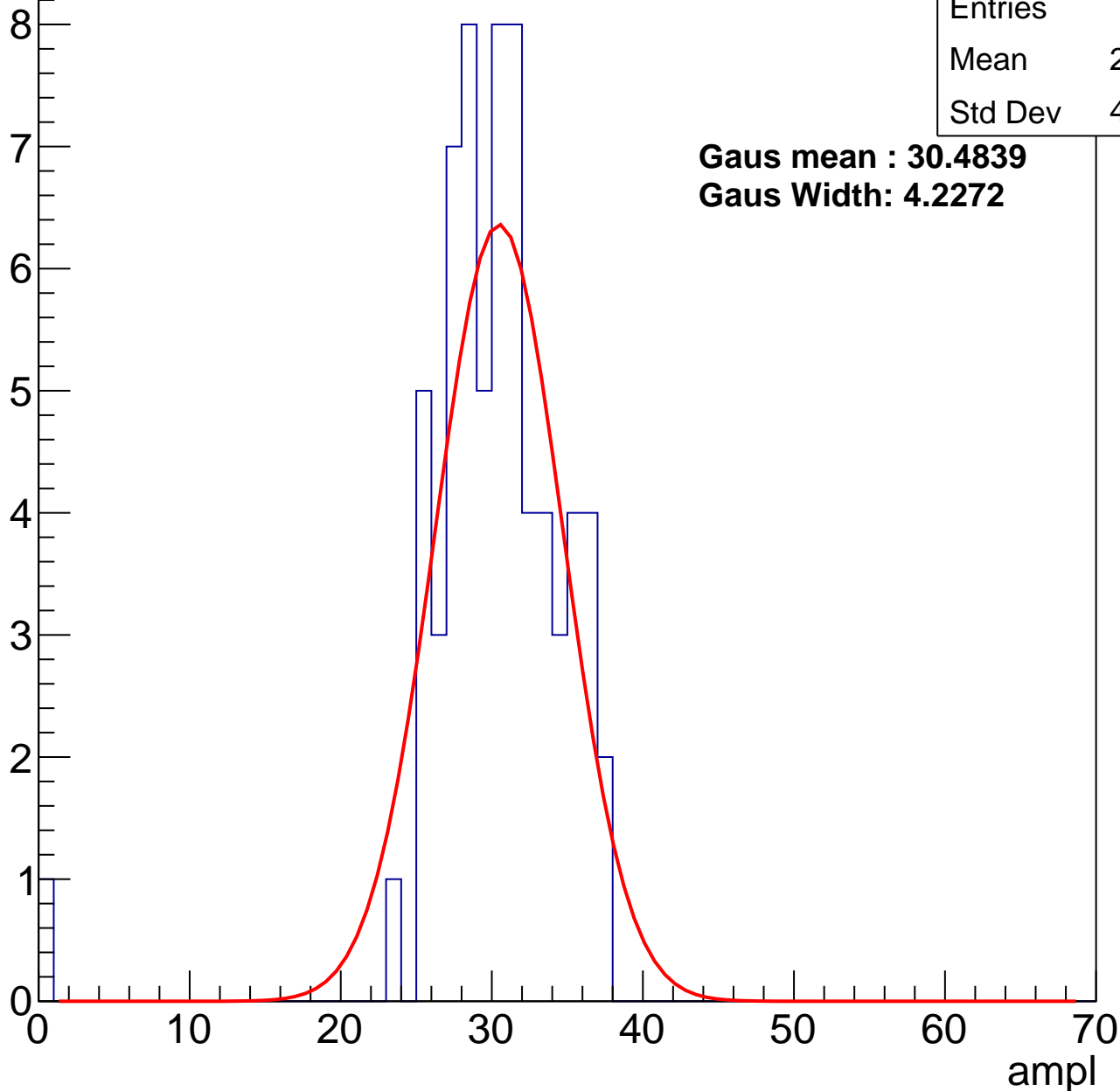
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	29.73
Std Dev	4.988

**Gaus mean : 30.4839**

**Gaus Width: 4.2272**



# B1L003S, U6-ch73, adc1

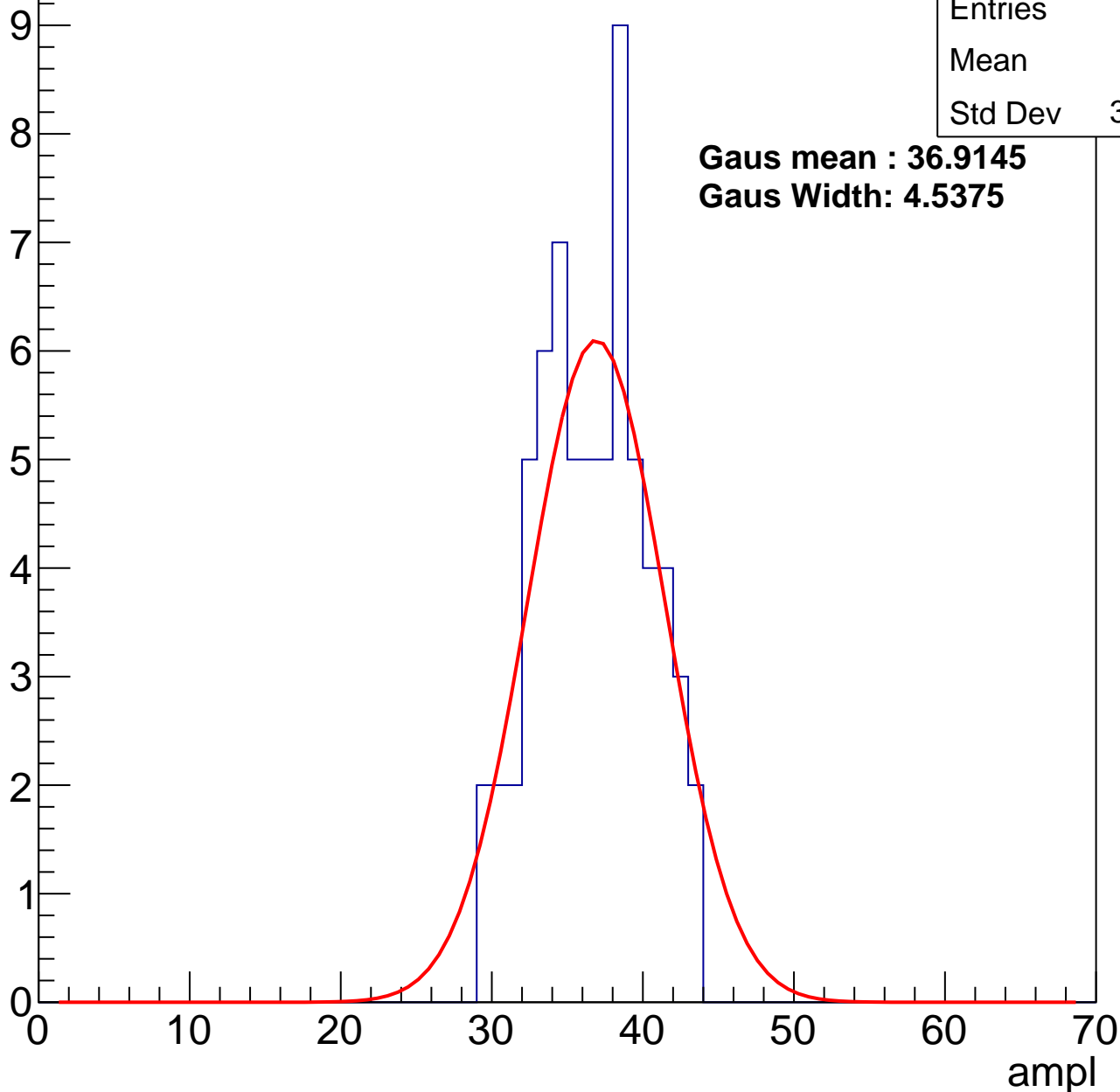
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	36.2
Std Dev	3.568

**Gaus mean : 36.9145**

**Gaus Width: 4.5375**



# B1L003S, U6-ch73, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	79
Mean	43.62
Std Dev	3.516

**Gaus mean : 44.5203**

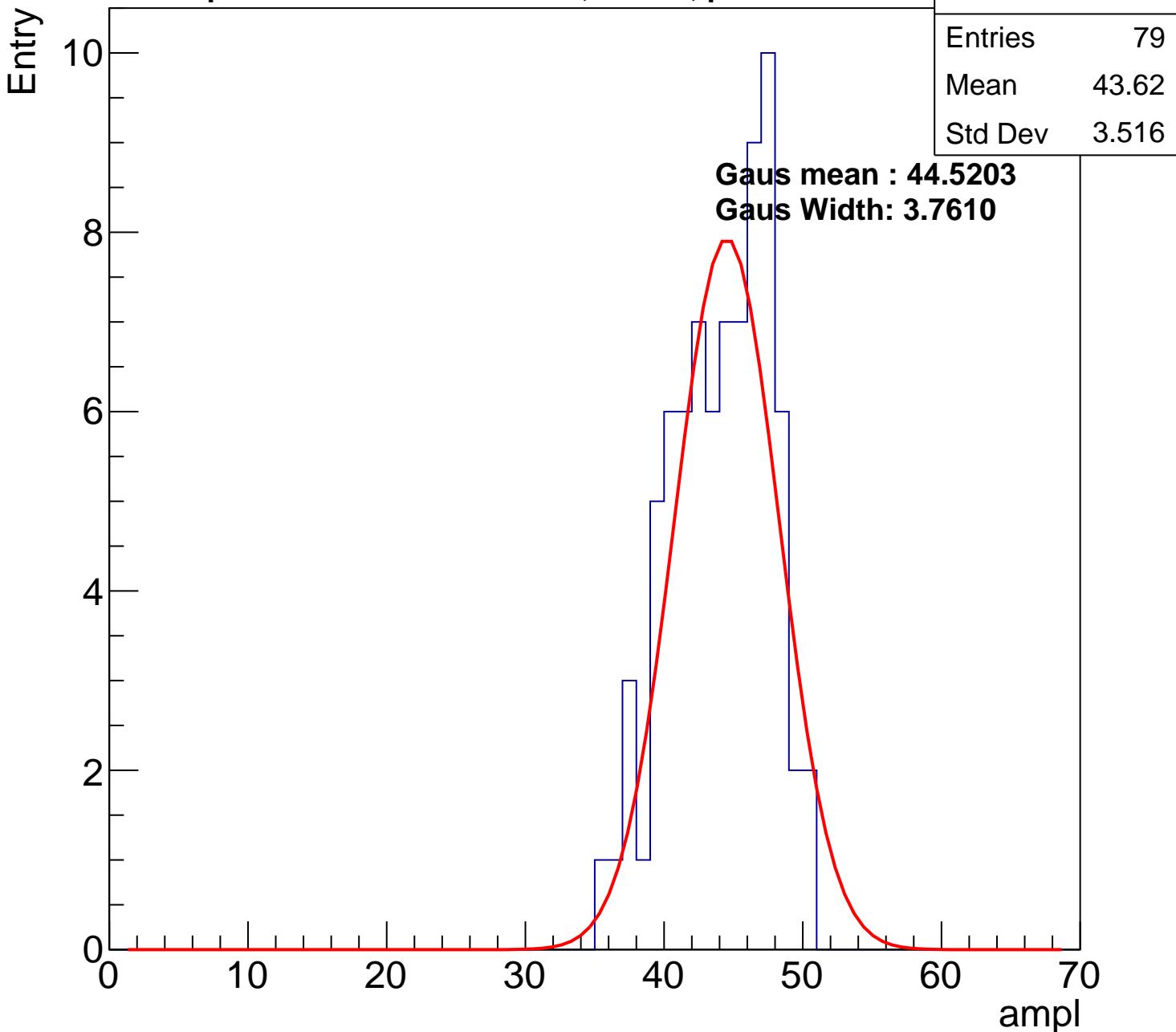
**Gaus Width: 3.7610**

Entry

10  
8  
6  
4  
2  
0

ampl

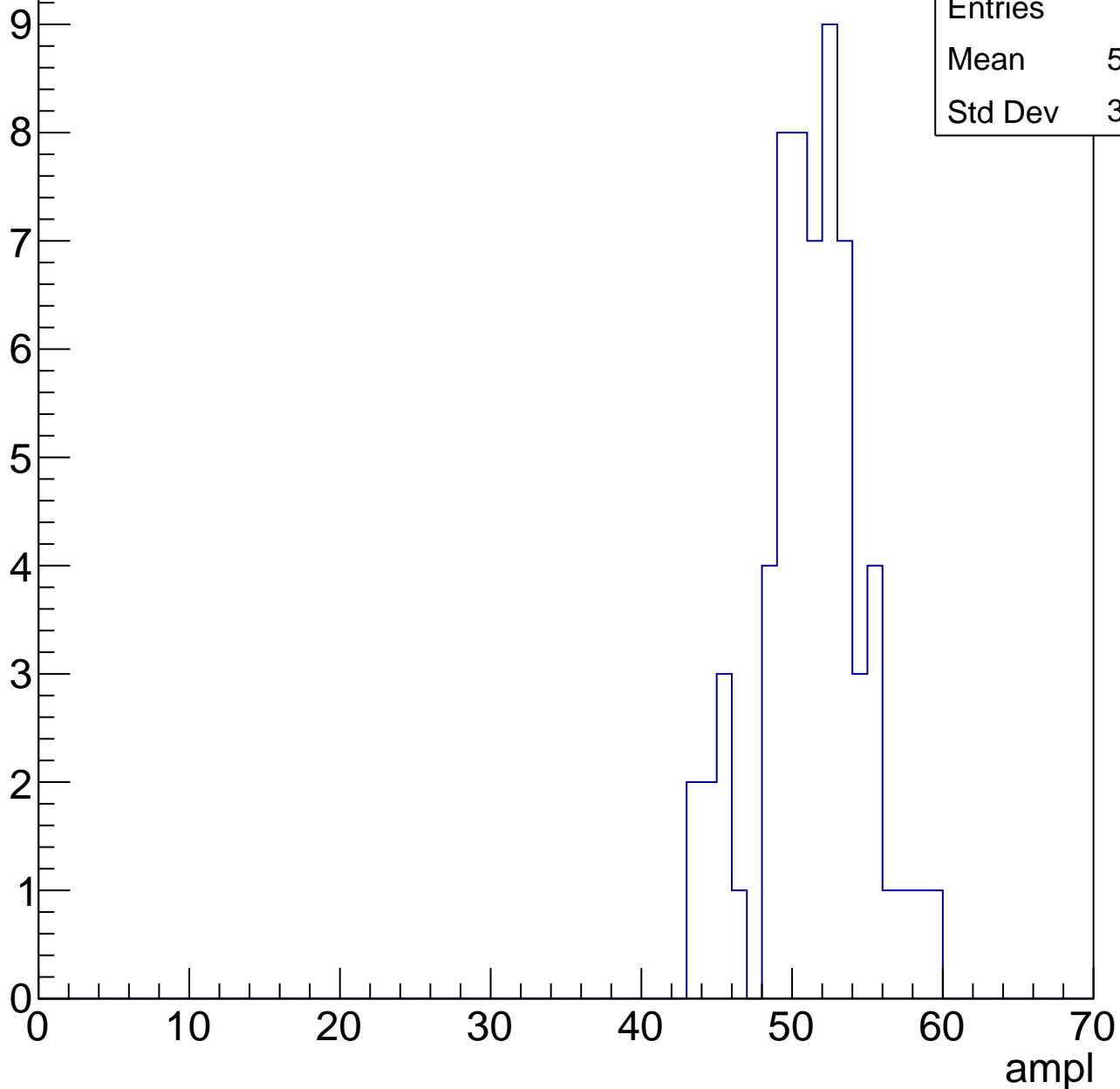
0 10 20 30 40 50 60 70



# B1L003S, U6-ch73, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



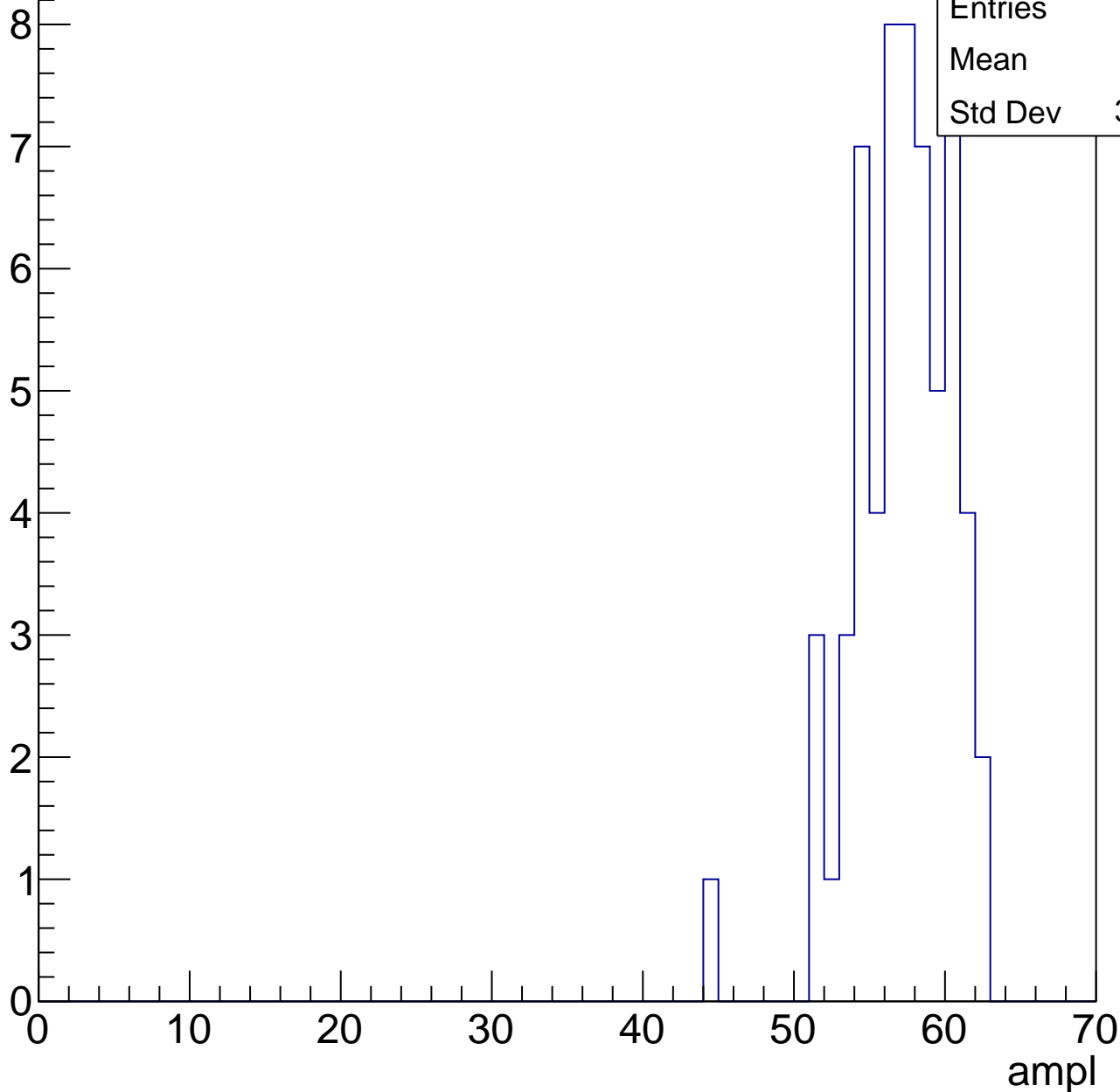
Entries	62
Mean	50.76
Std Dev	3.439

# B1L003S, U6-ch73, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	56.7
Std Dev	3.251

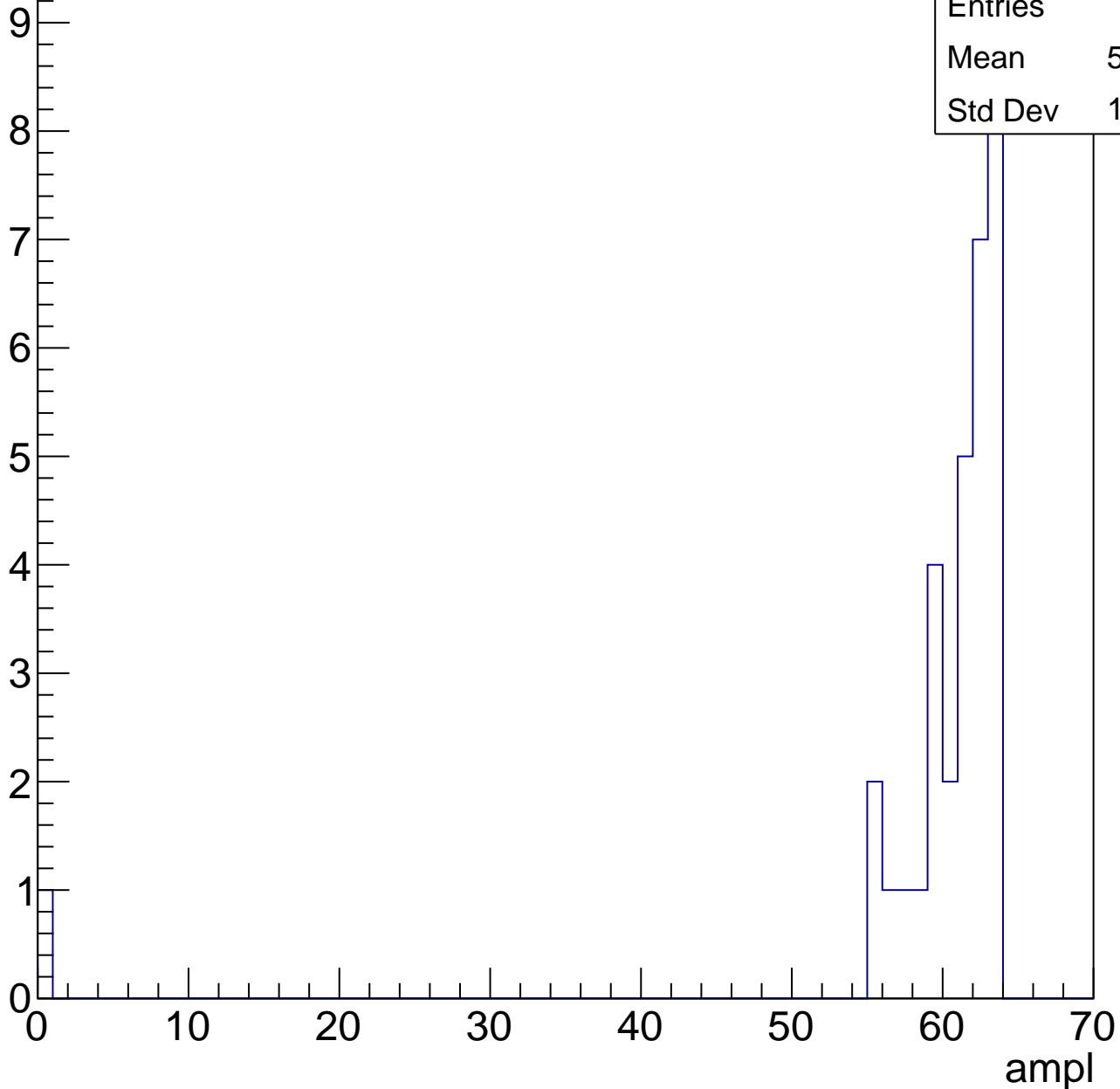


# B1L003S, U6-ch73, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

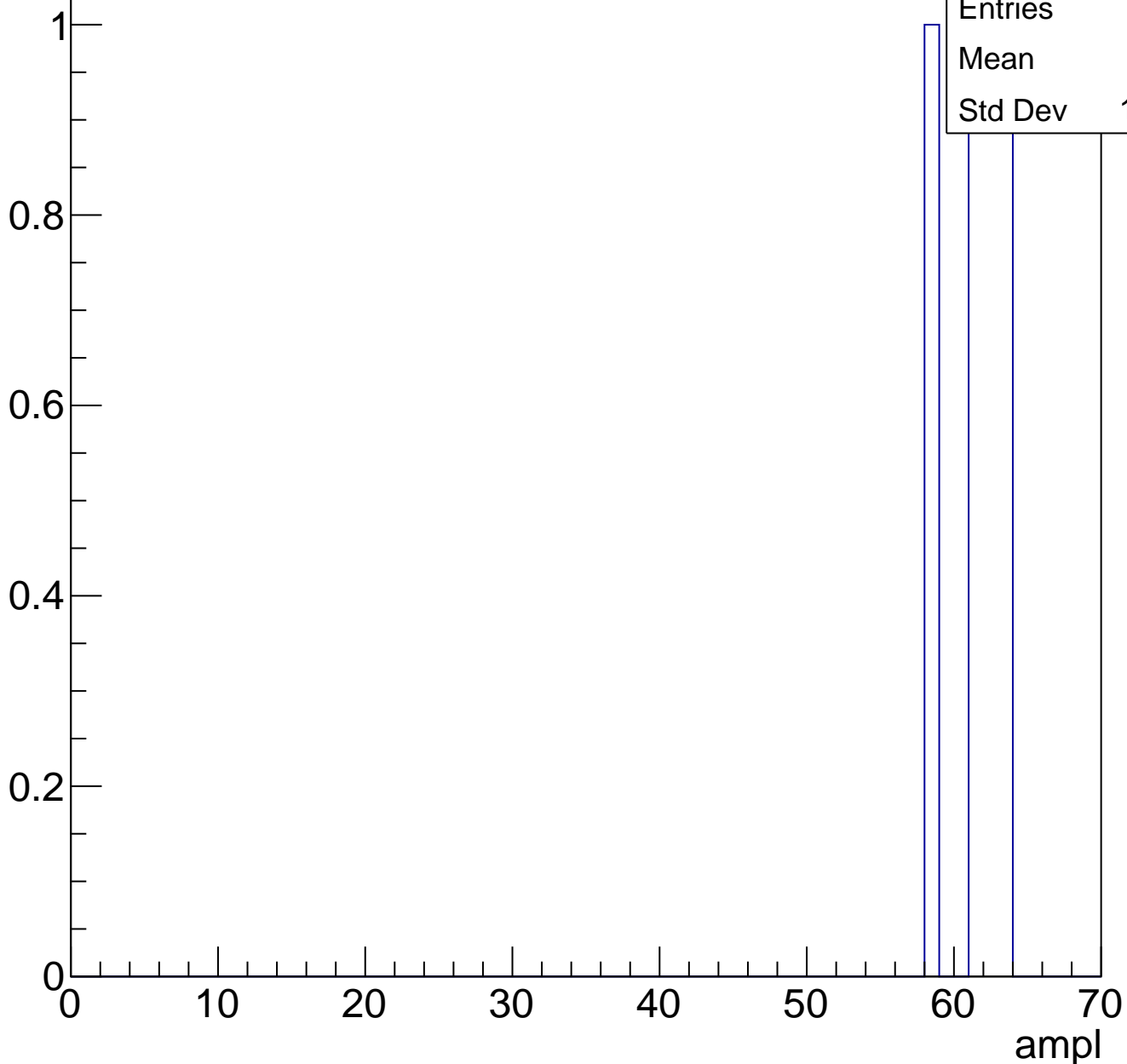
Entries	33
Mean	58.88
Std Dev	10.67



# B1L003S, U6-ch73, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch73, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch74, adc0

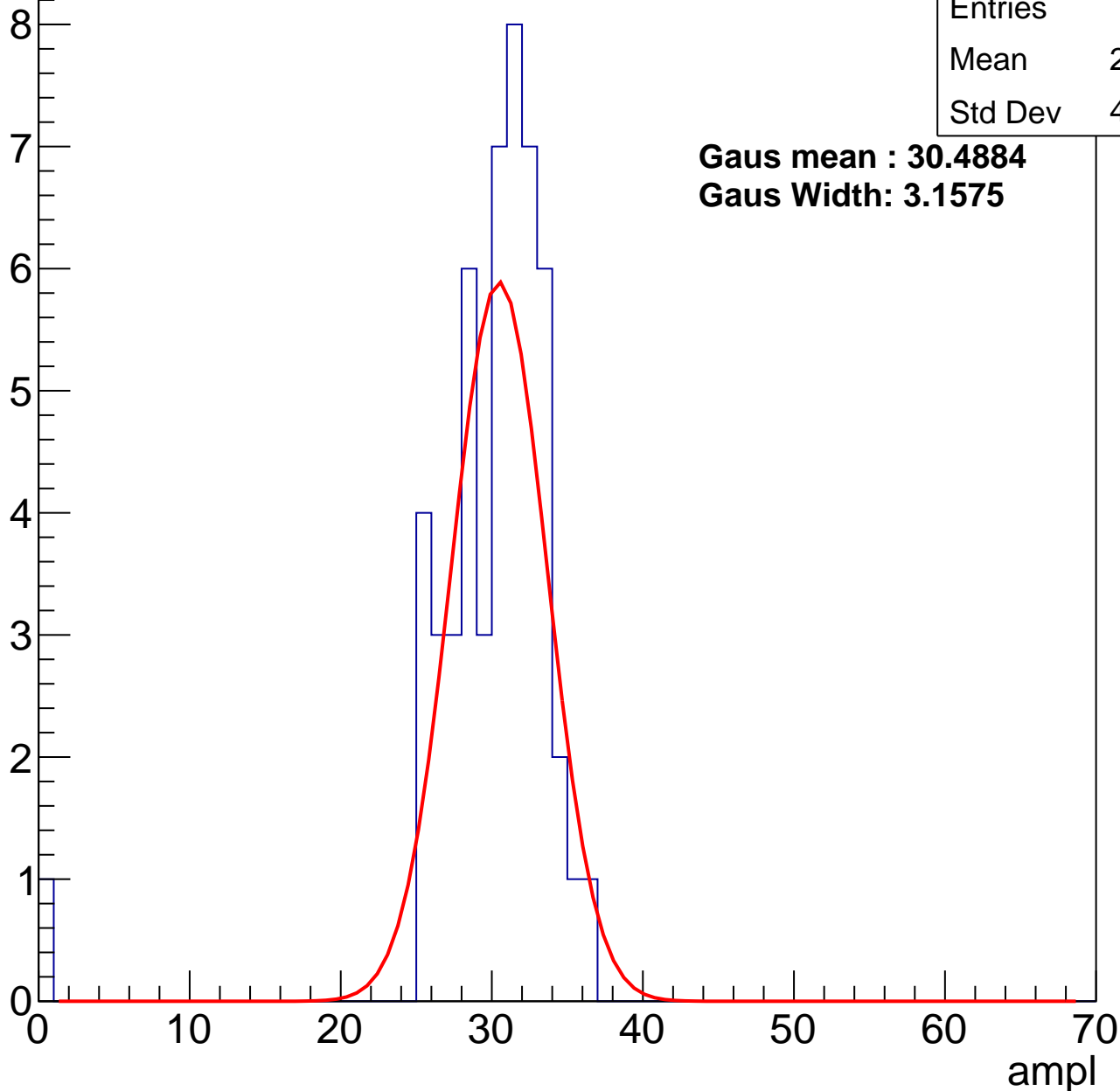
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	52
Mean	29.48
Std Dev	4.944

**Gaus mean : 30.4884**

**Gaus Width: 3.1575**



# B1L003S, U6-ch74, adc1

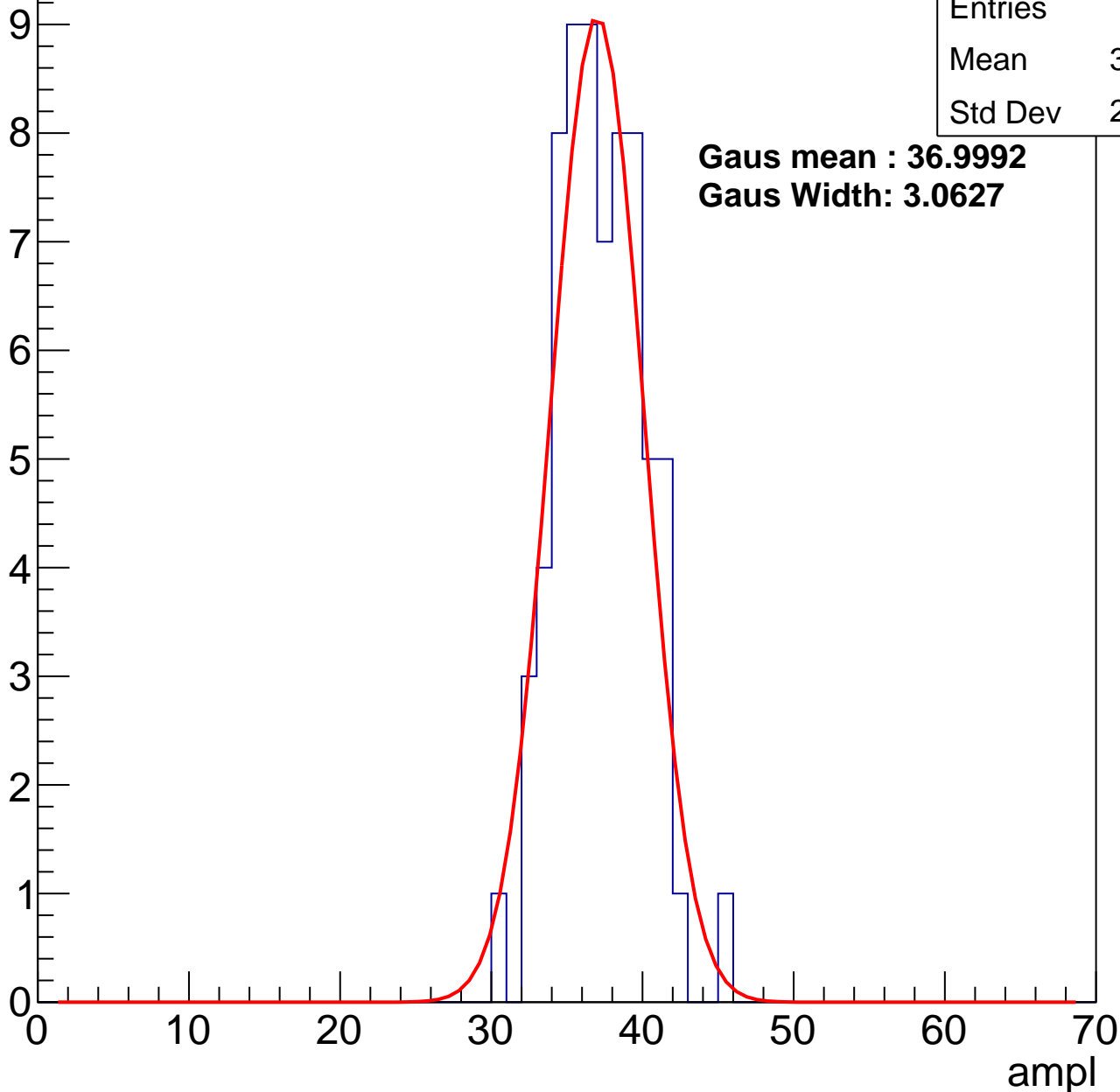
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	36.75
Std Dev	2.836

**Gaus mean : 36.9992**

**Gaus Width: 3.0627**



# B1L003S, U6-ch74, adc2

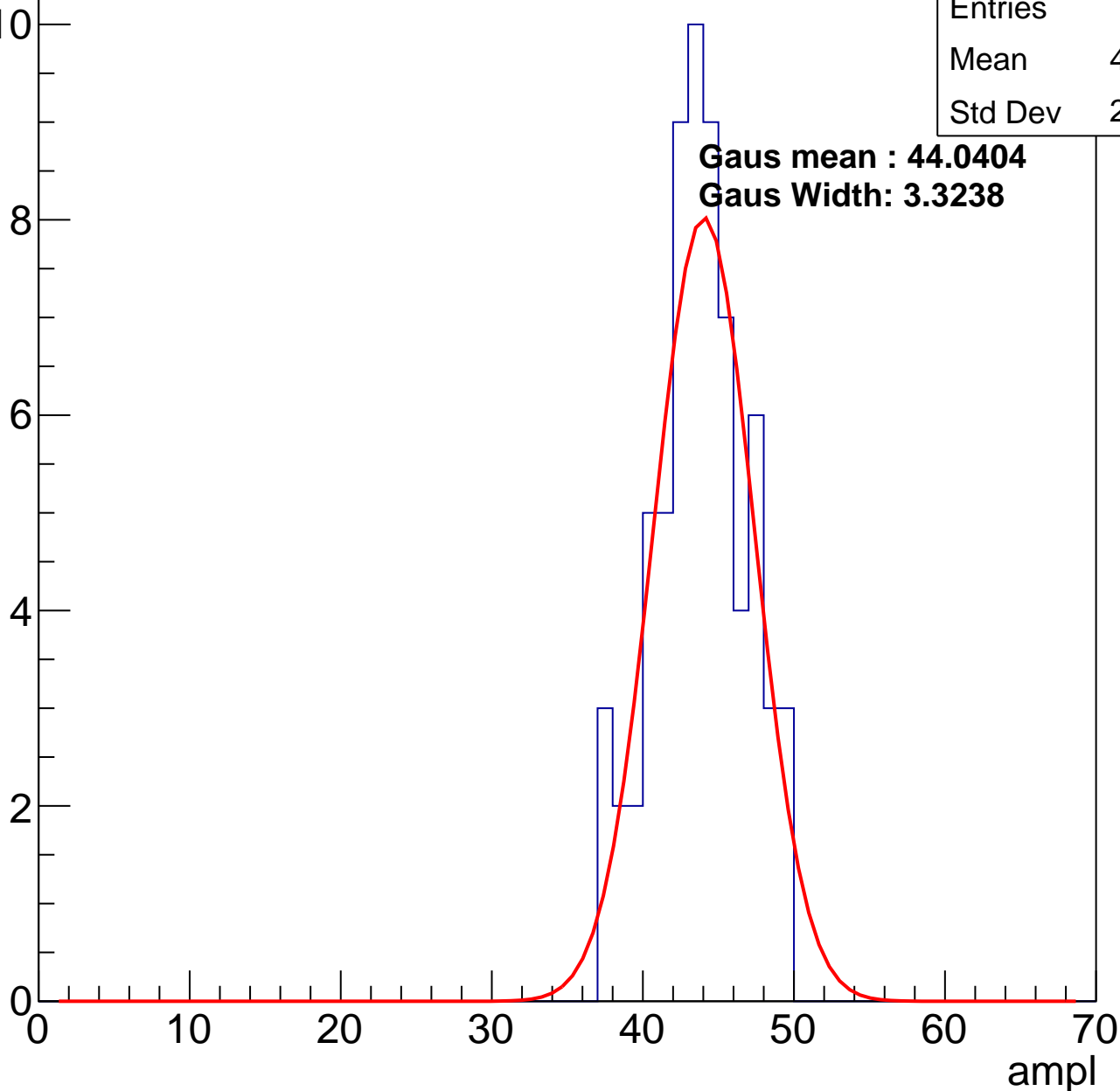
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	43.32
Std Dev	2.992

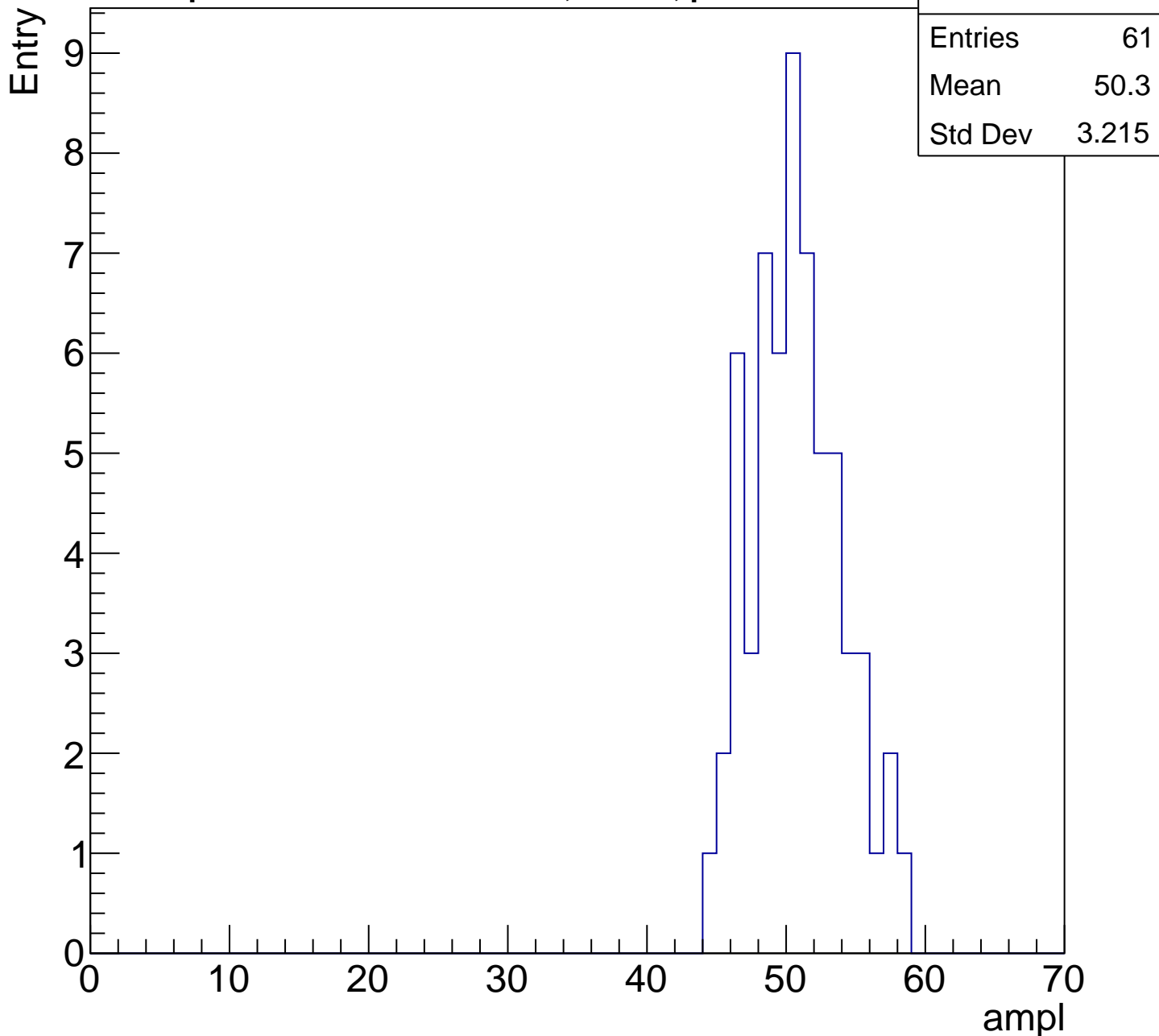
**Gaus mean : 44.0404**

**Gaus Width: 3.3238**



# B1L003S, U6-ch74, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

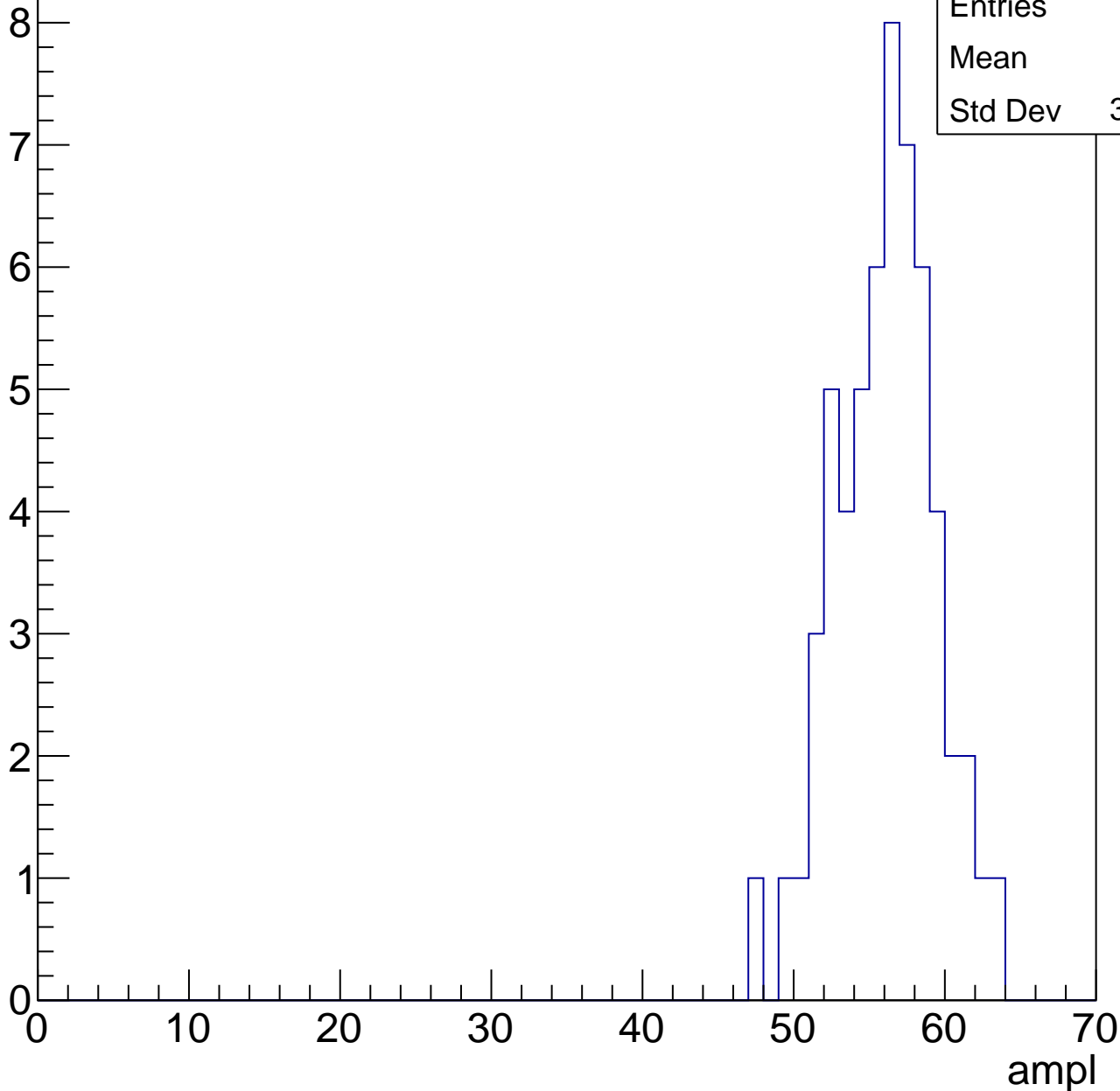


# B1L003S, U6-ch74, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	55.6
Std Dev	3.265

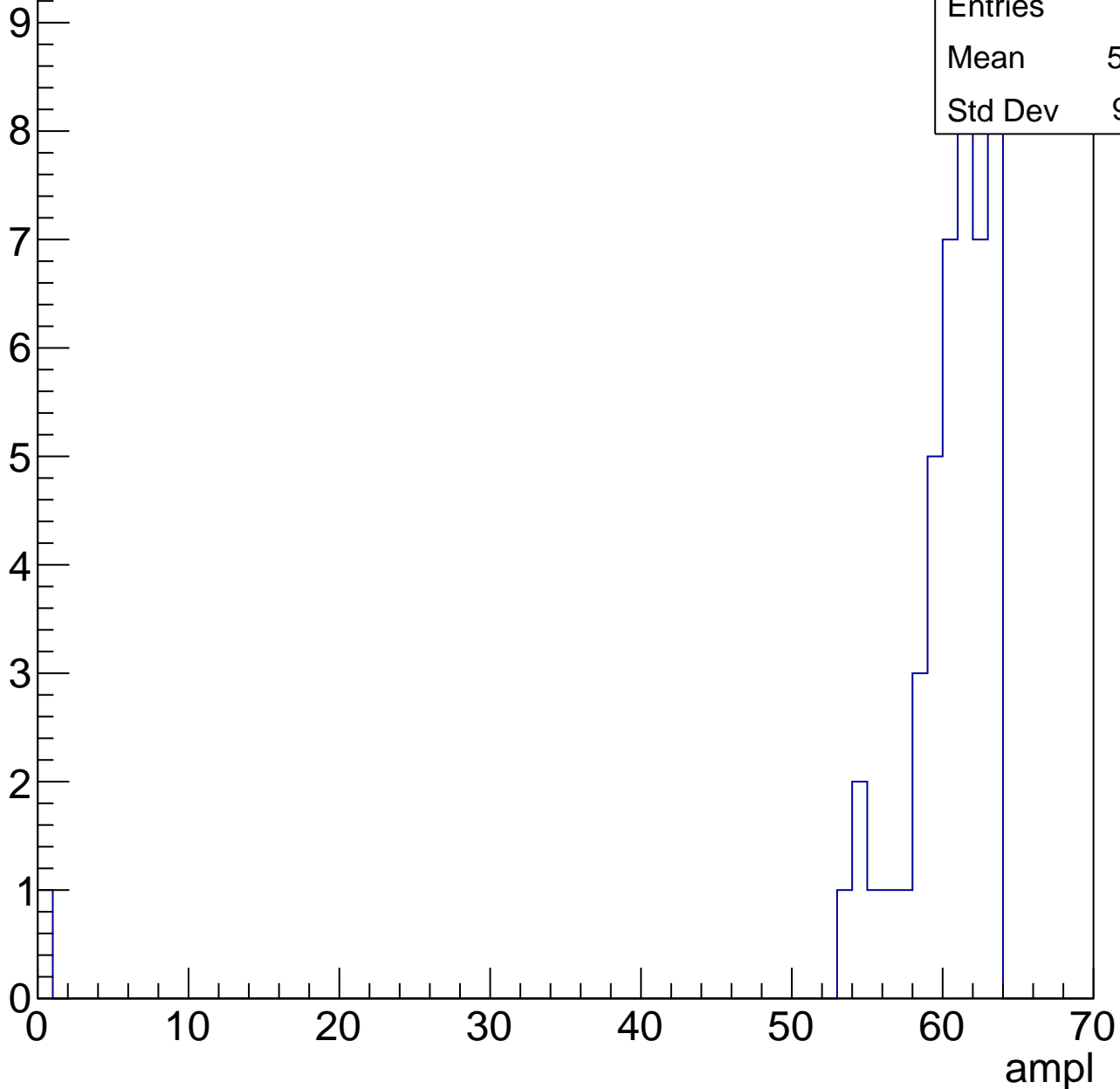


# B1L003S, U6-ch74, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

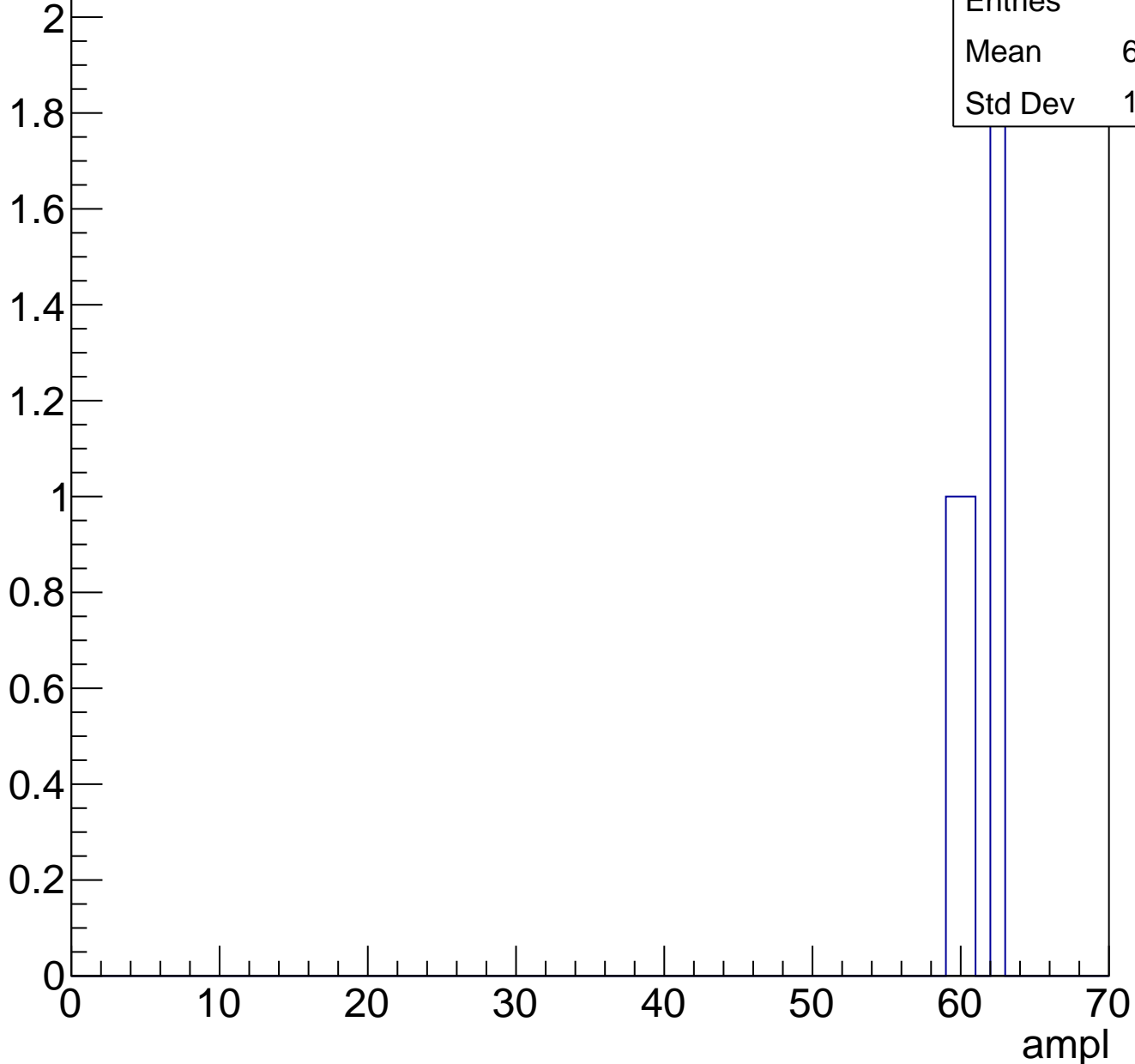
Entries	46
Mean	58.85
Std Dev	9.141



# B1L003S, U6-ch74, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

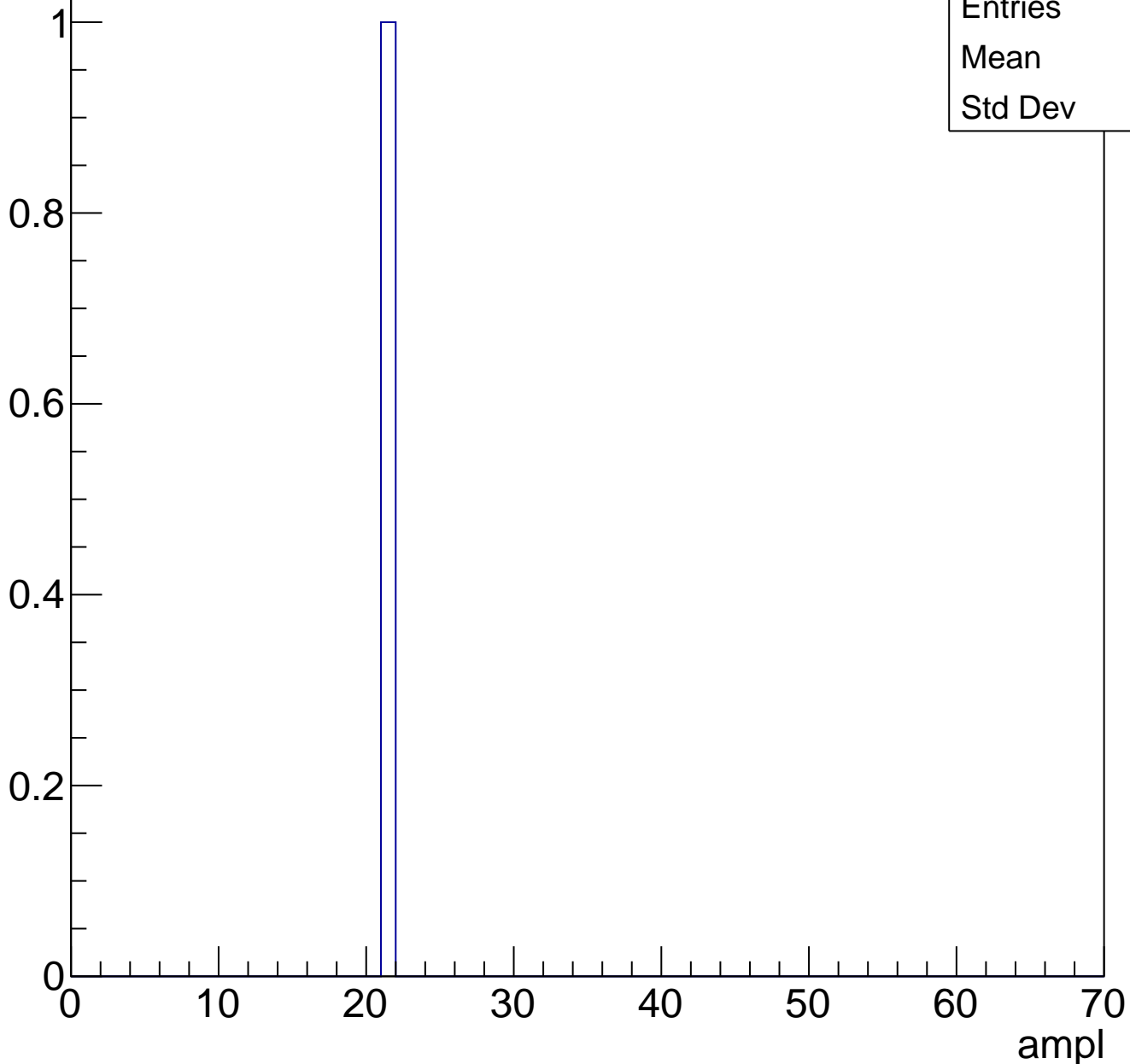




# B1L003S, U6-ch74, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch75, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	83
Mean	30.14
Std Dev	6.03

**Gaus mean : 31.3702**

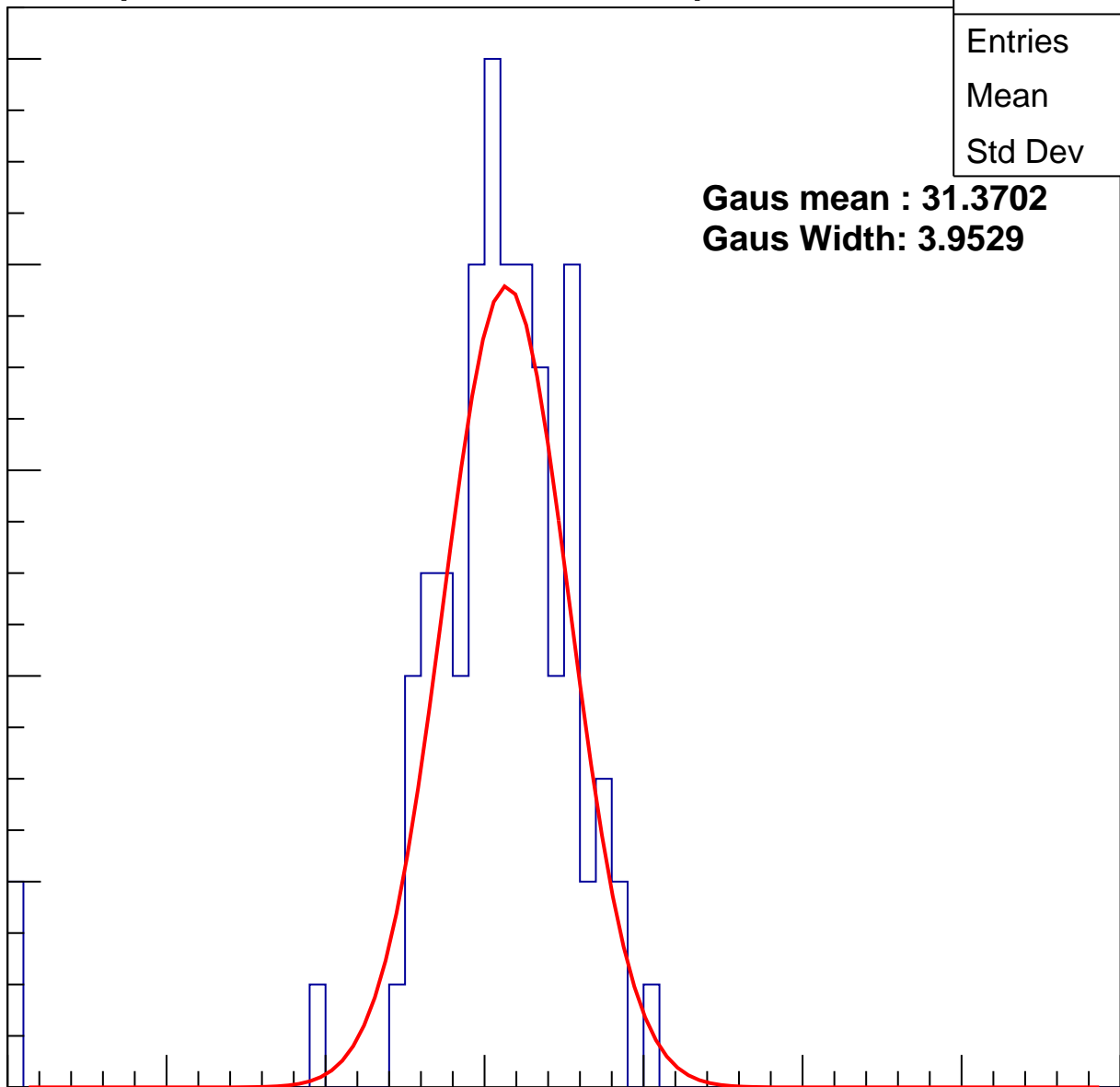
**Gaus Width: 3.9529**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U6-ch75, adc1

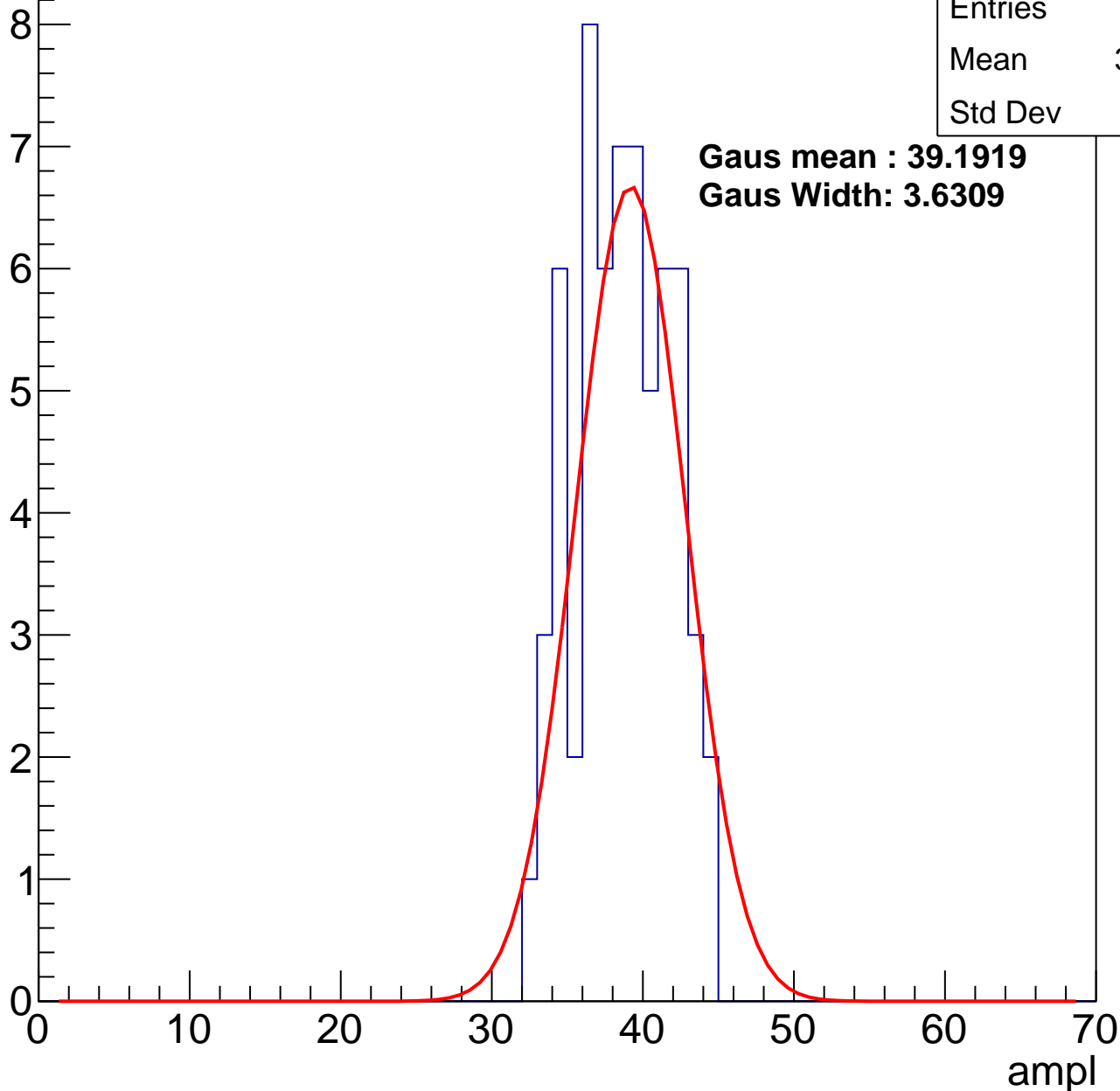
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	38.21
Std Dev	3.07

**Gaus mean : 39.1919**

**Gaus Width: 3.6309**



# B1L003S, U6-ch75, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	65
Mean	44.42
Std Dev	3.157

**Gaus mean : 45.0376**

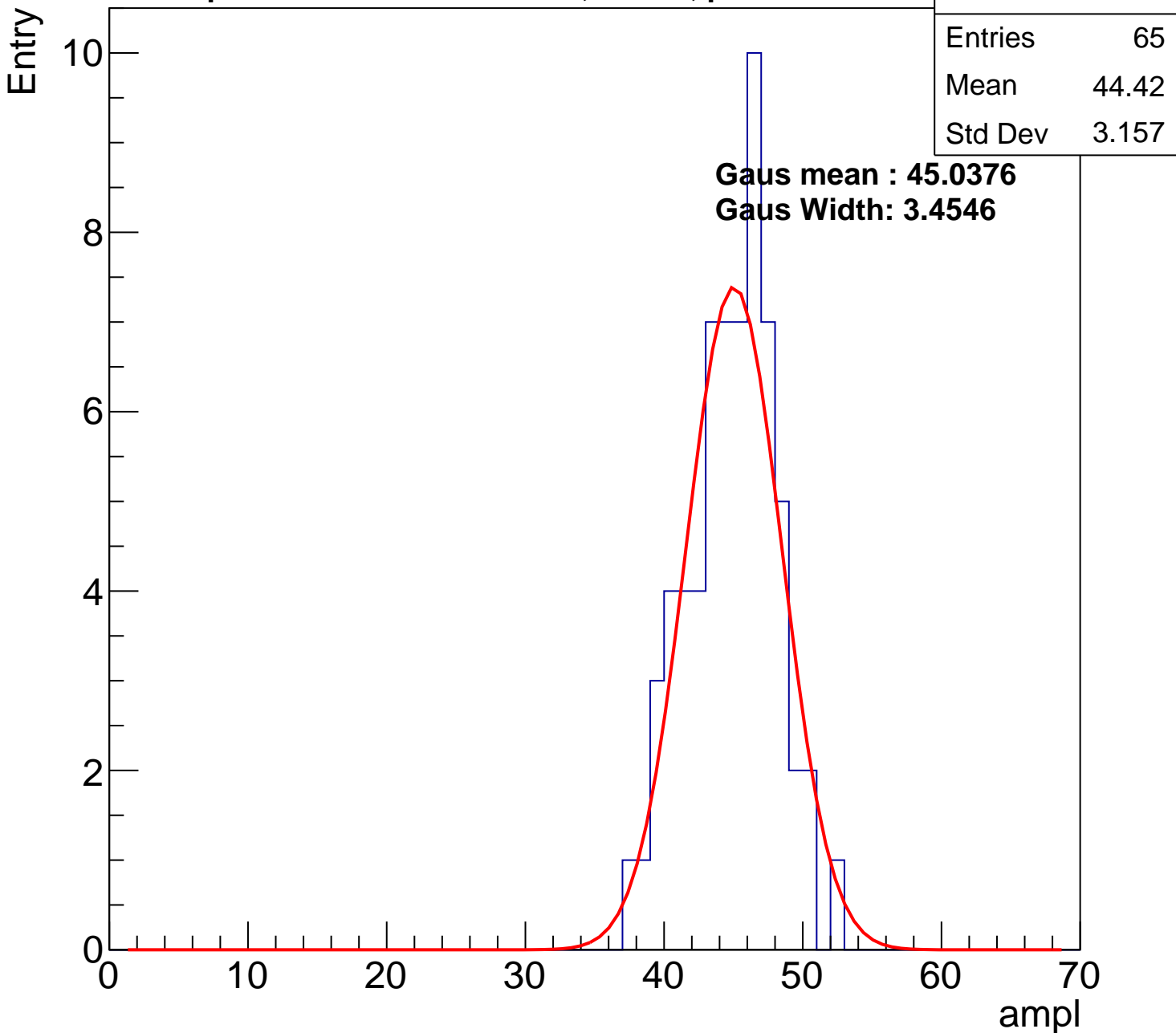
**Gaus Width: 3.4546**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

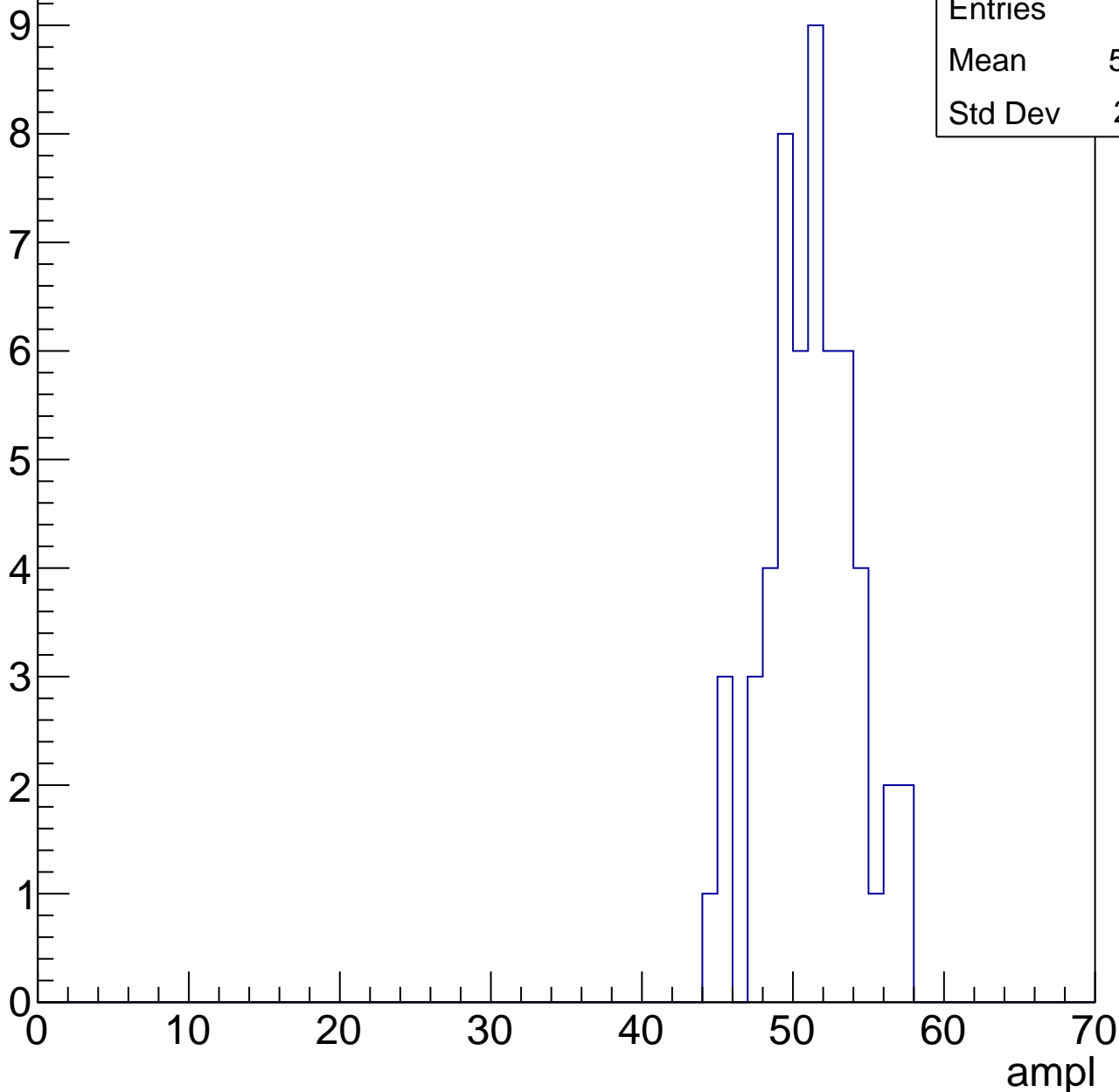


# B1L003S, U6-ch75, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	50.73
Std Dev	2.951



# B1L003S, U6-ch75, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	73
Mean	56.9
Std Dev	3.323

Entry

10

8

6

4

2

0

0

10

20

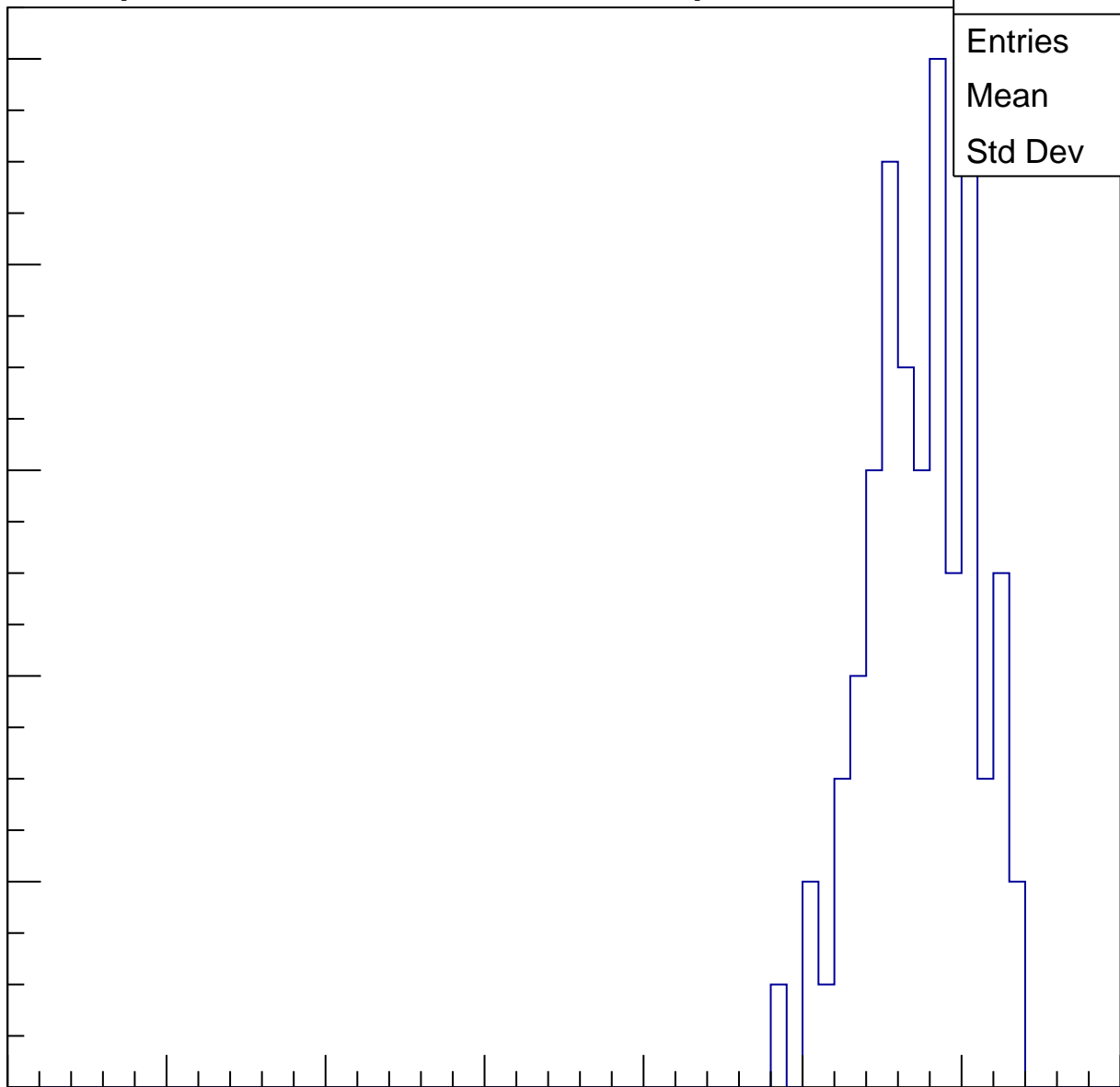
30

40

50

60

ampl

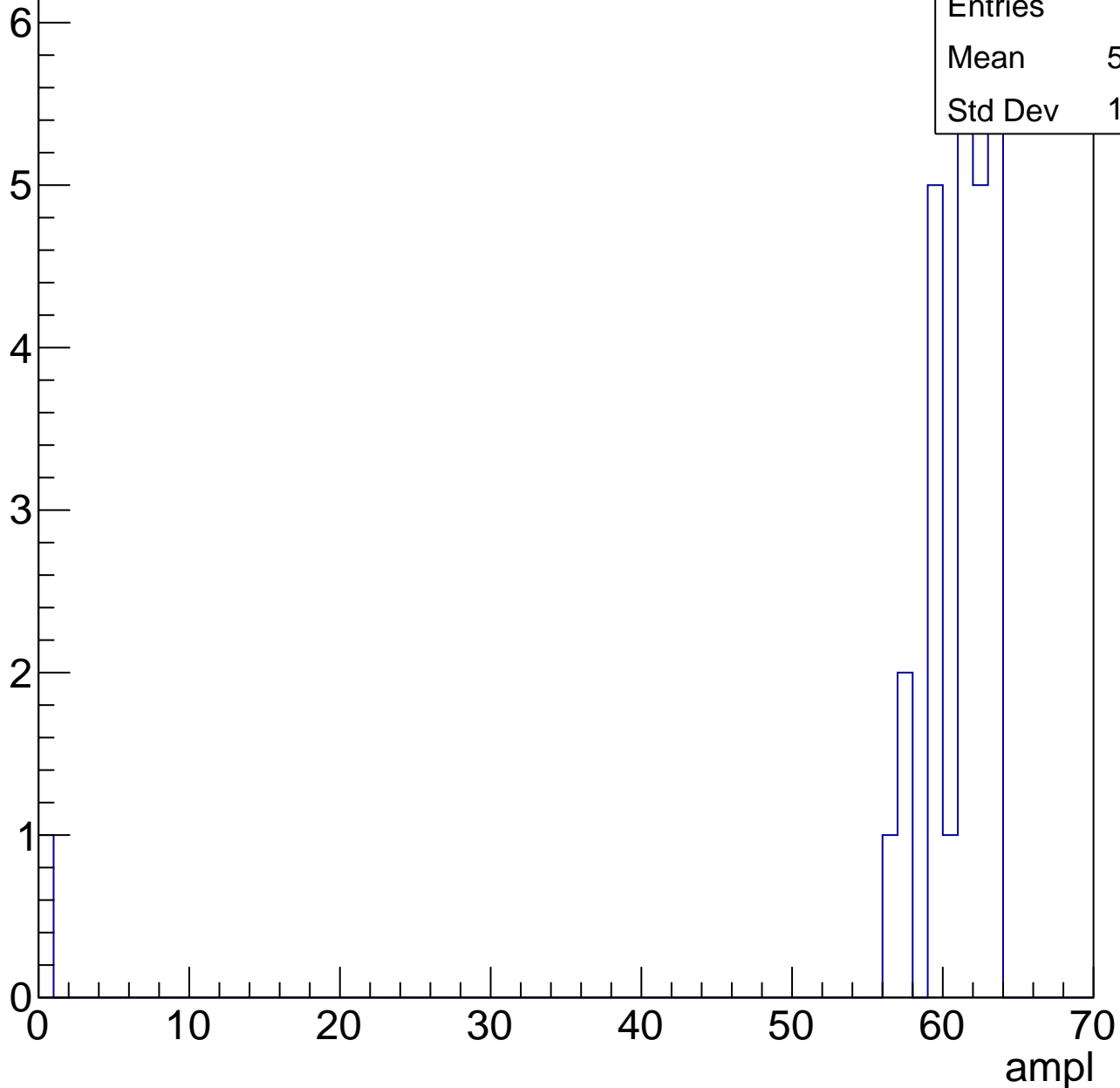


# B1L003S, U6-ch75, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	27
Mean	58.48
Std Dev	11.64



# B1L003S, U6-ch75, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch75, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L003S, U6-ch76, adc0

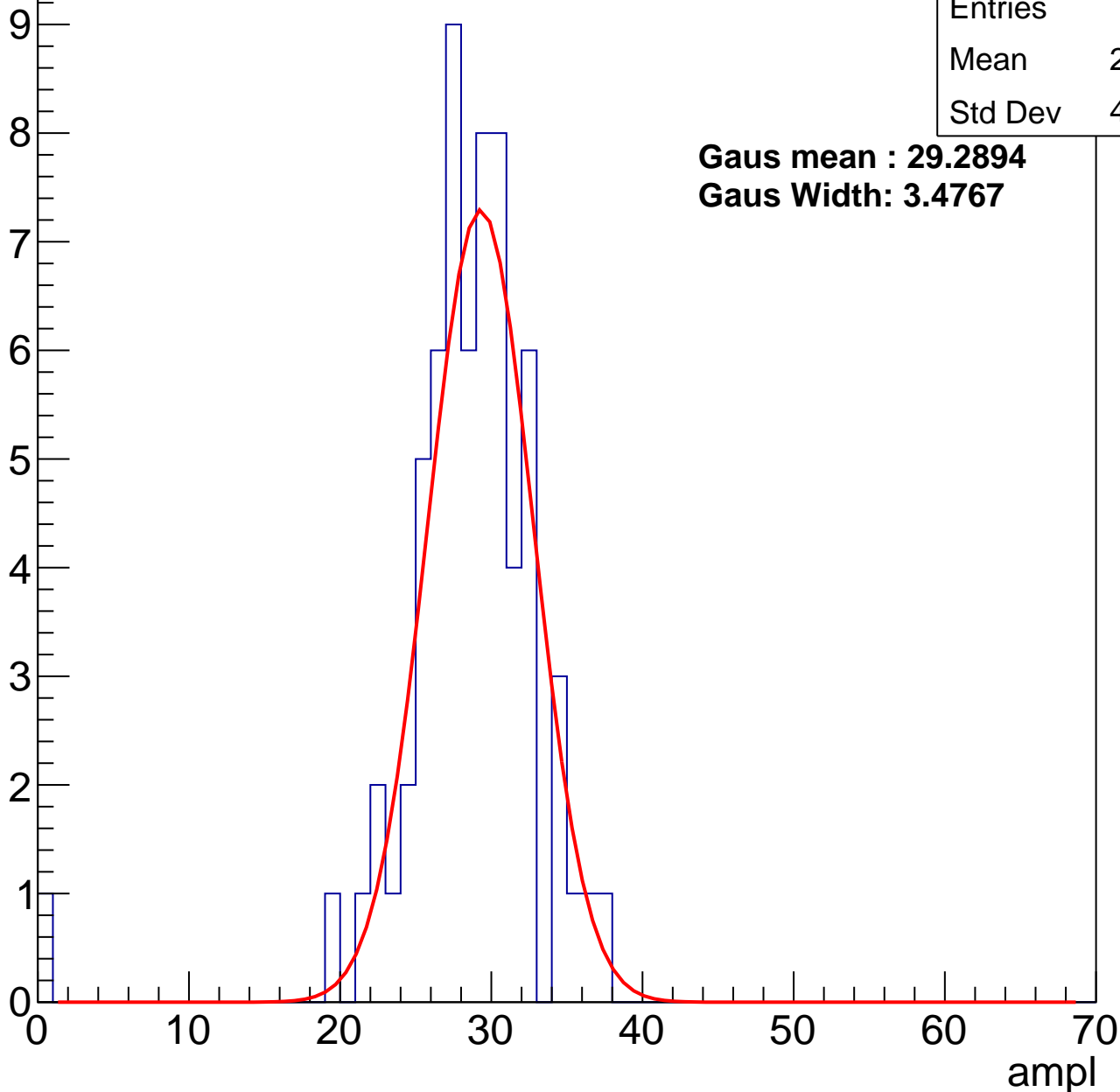
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	27.95
Std Dev	4.916

**Gaus mean : 29.2894**

**Gaus Width: 3.4767**



# B1L003S, U6-ch76, adc1

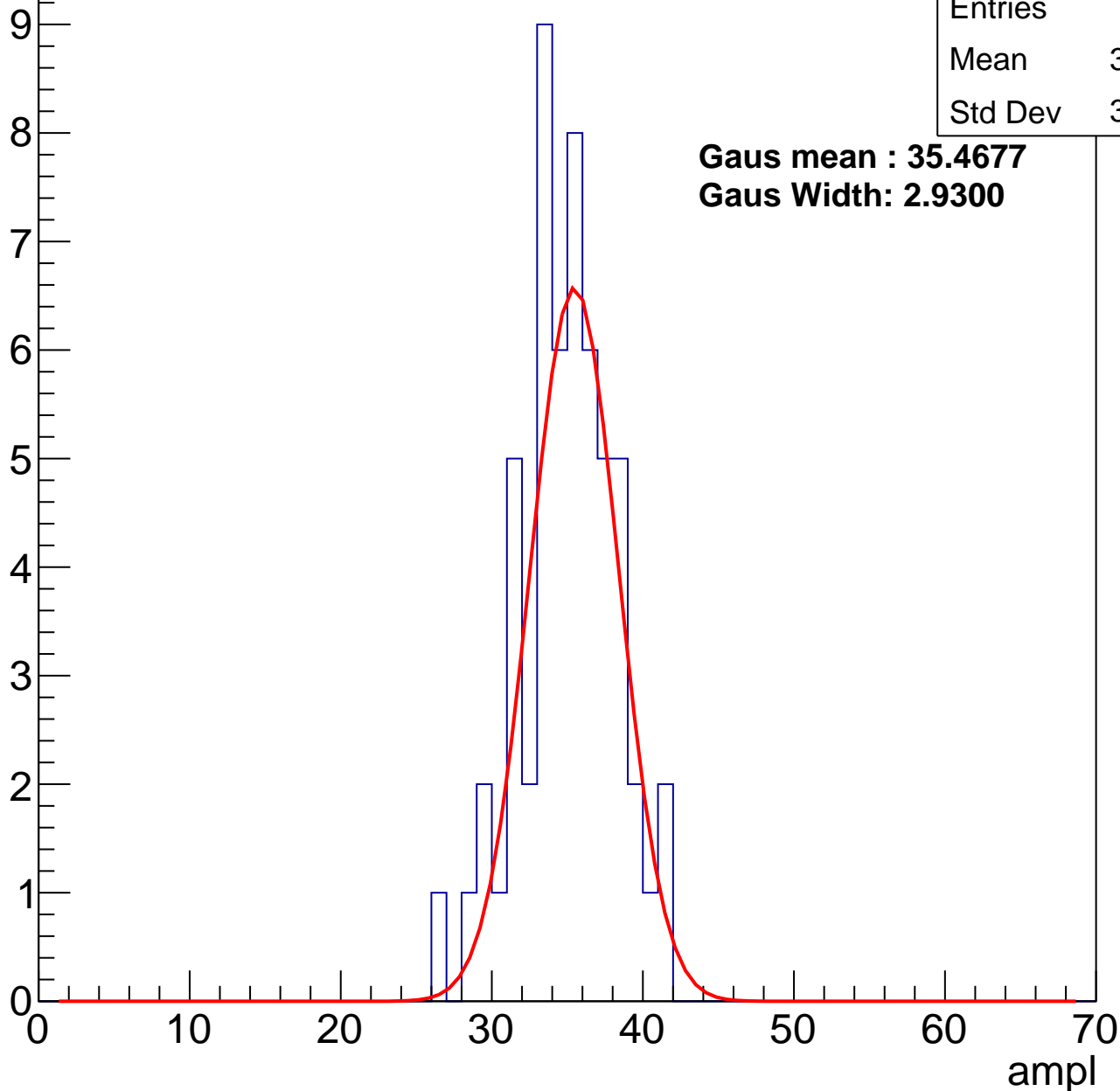
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	34.52
Std Dev	3.145

**Gaus mean : 35.4677**

**Gaus Width: 2.9300**



# B1L003S, U6-ch76, adc2

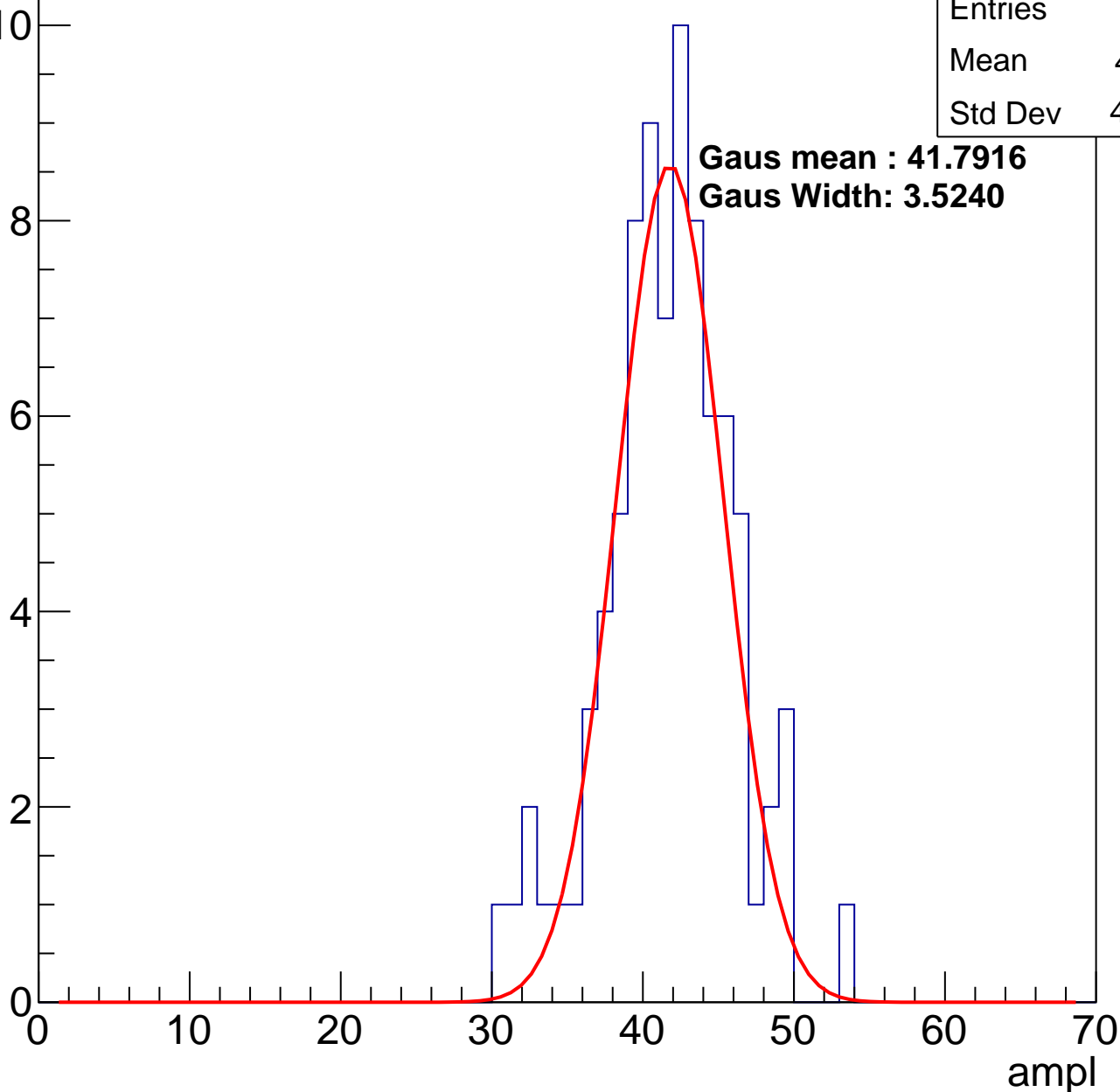
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	85
Mean	41.21
Std Dev	4.257

**Gaus mean : 41.7916**

**Gaus Width: 3.5240**

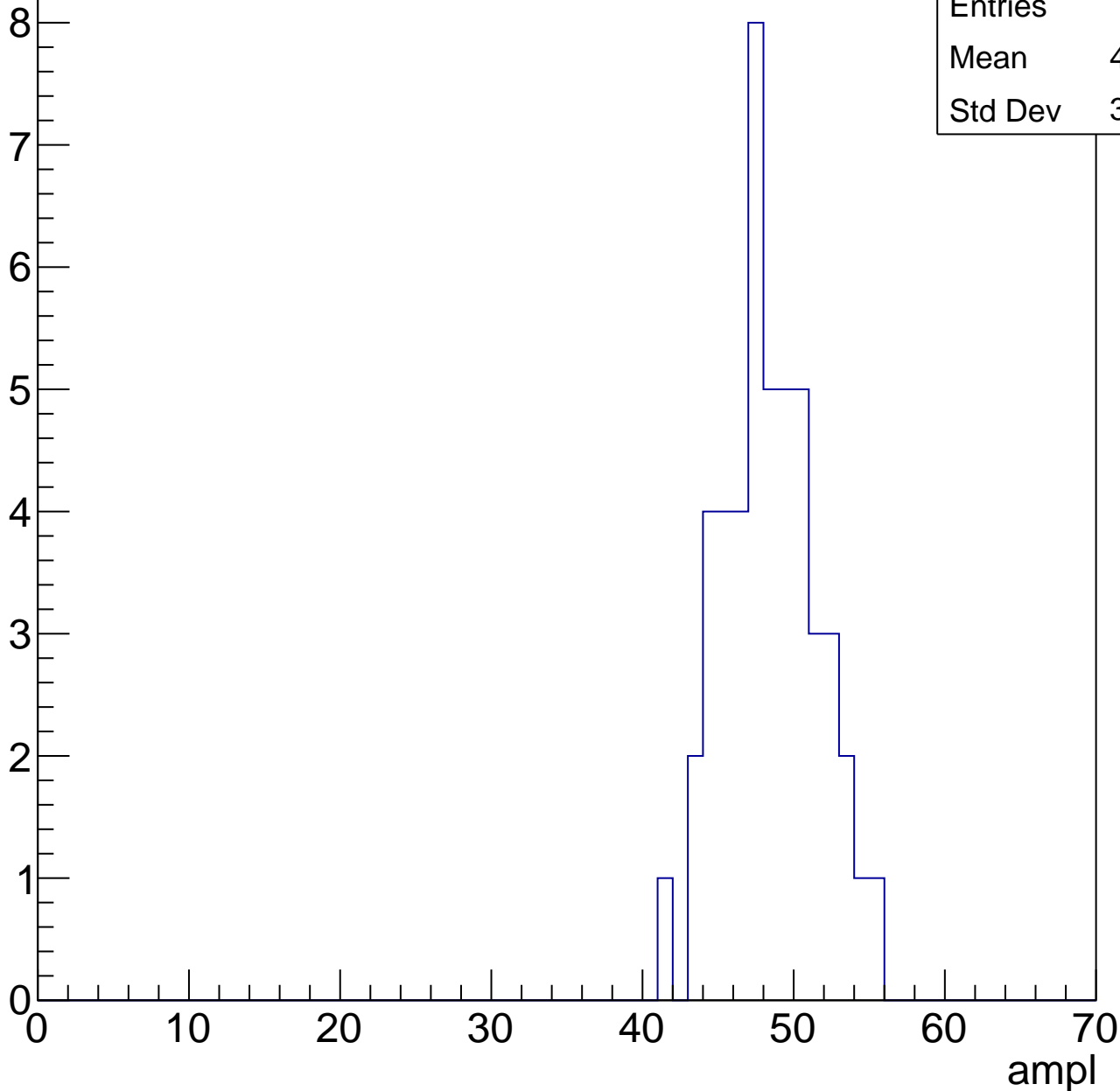


# B1L003S, U6-ch76, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	48
Mean	47.96
Std Dev	3.089

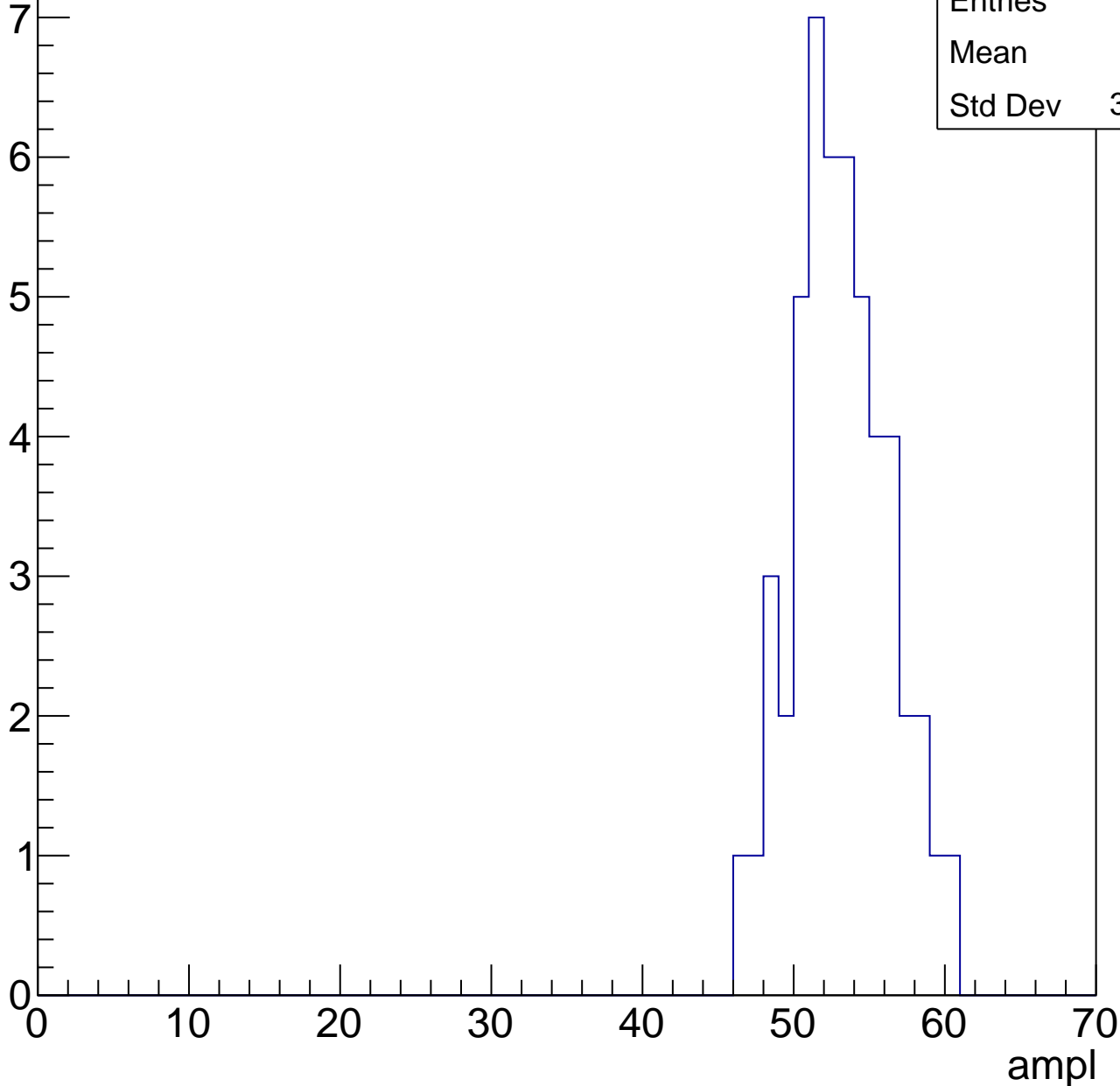


# B1L003S, U6-ch76, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

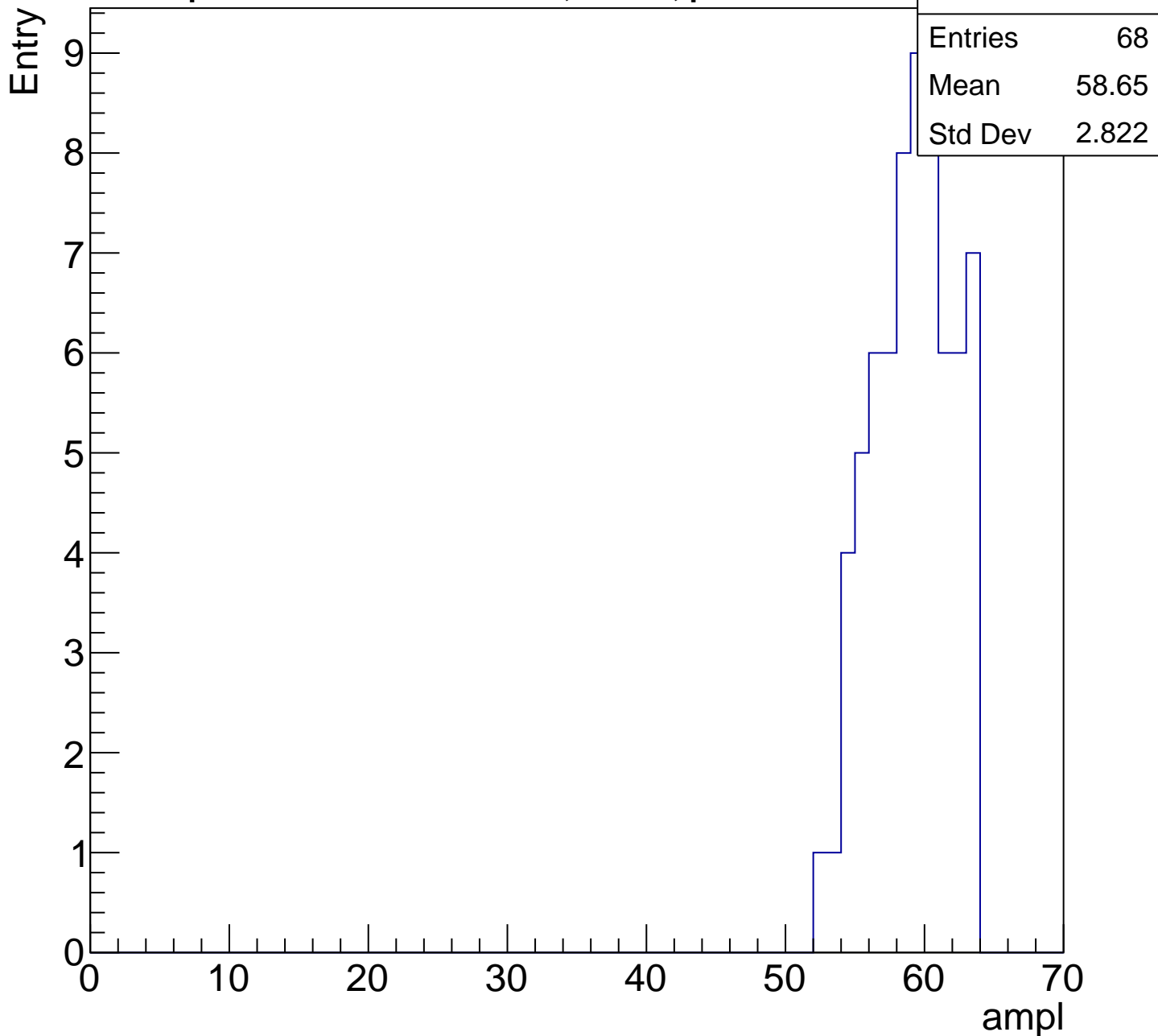
Entry

Entries	50
Mean	52.7
Std Dev	3.132



# B1L003S, U6-ch76, adc5

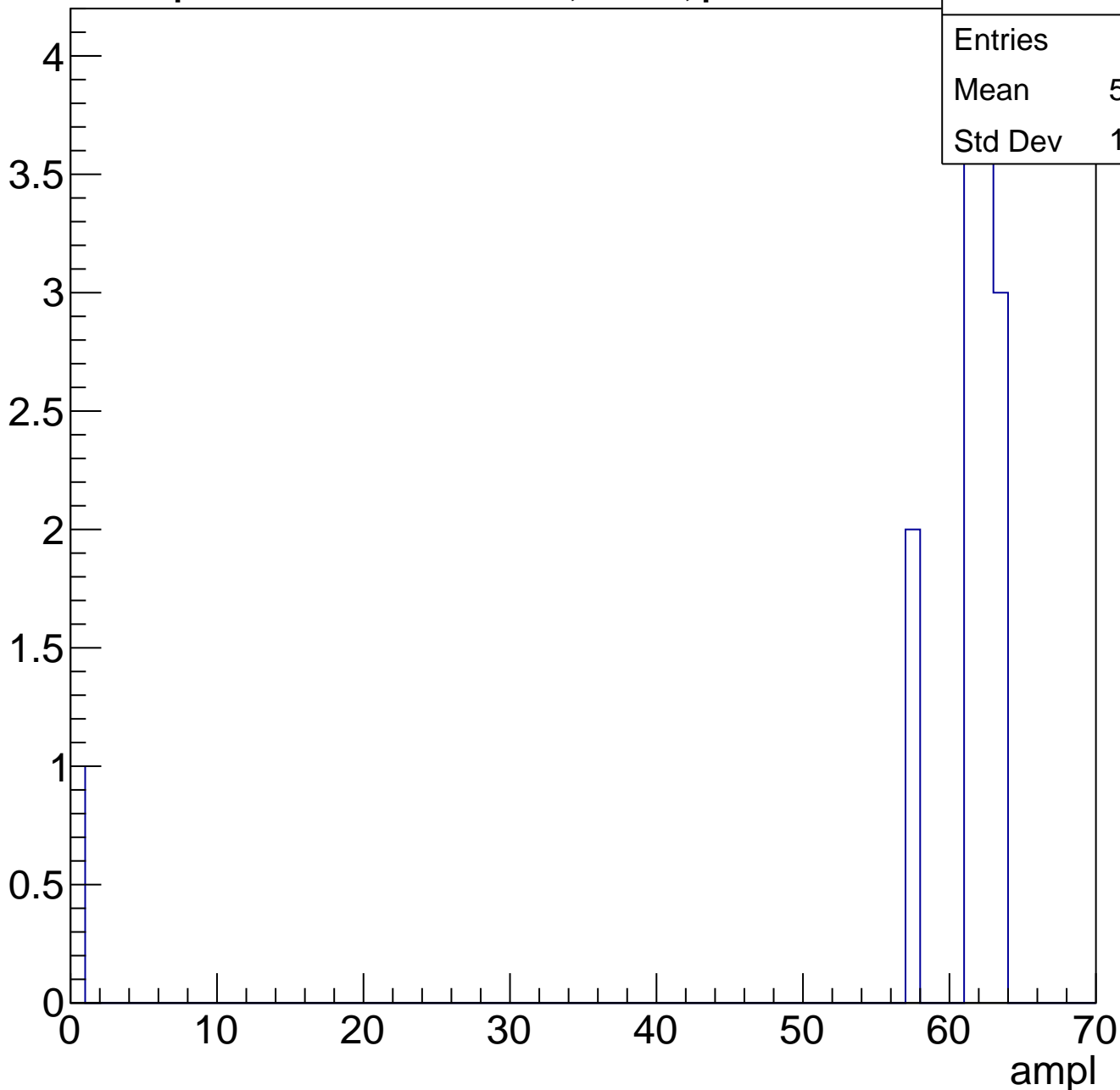
calib\_packv5\_042523\_0143.root, FC#13, port D2



# B1L003S, U6-ch76, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch76, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U6-ch77, adc0

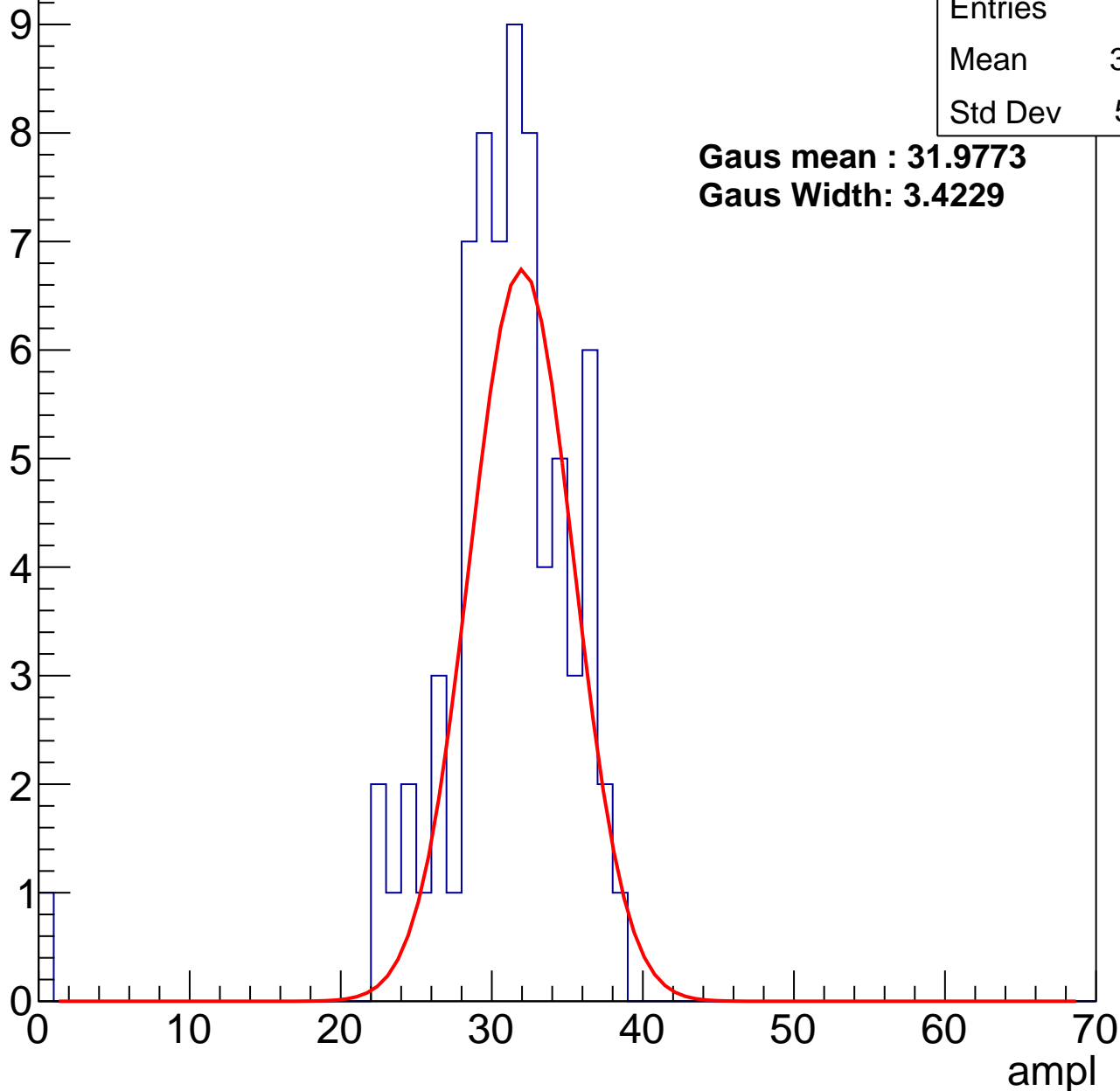
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	71
Mean	30.32
Std Dev	5.131

**Gaus mean : 31.9773**

**Gaus Width: 3.4229**



# B1L003S, U6-ch77, adc1

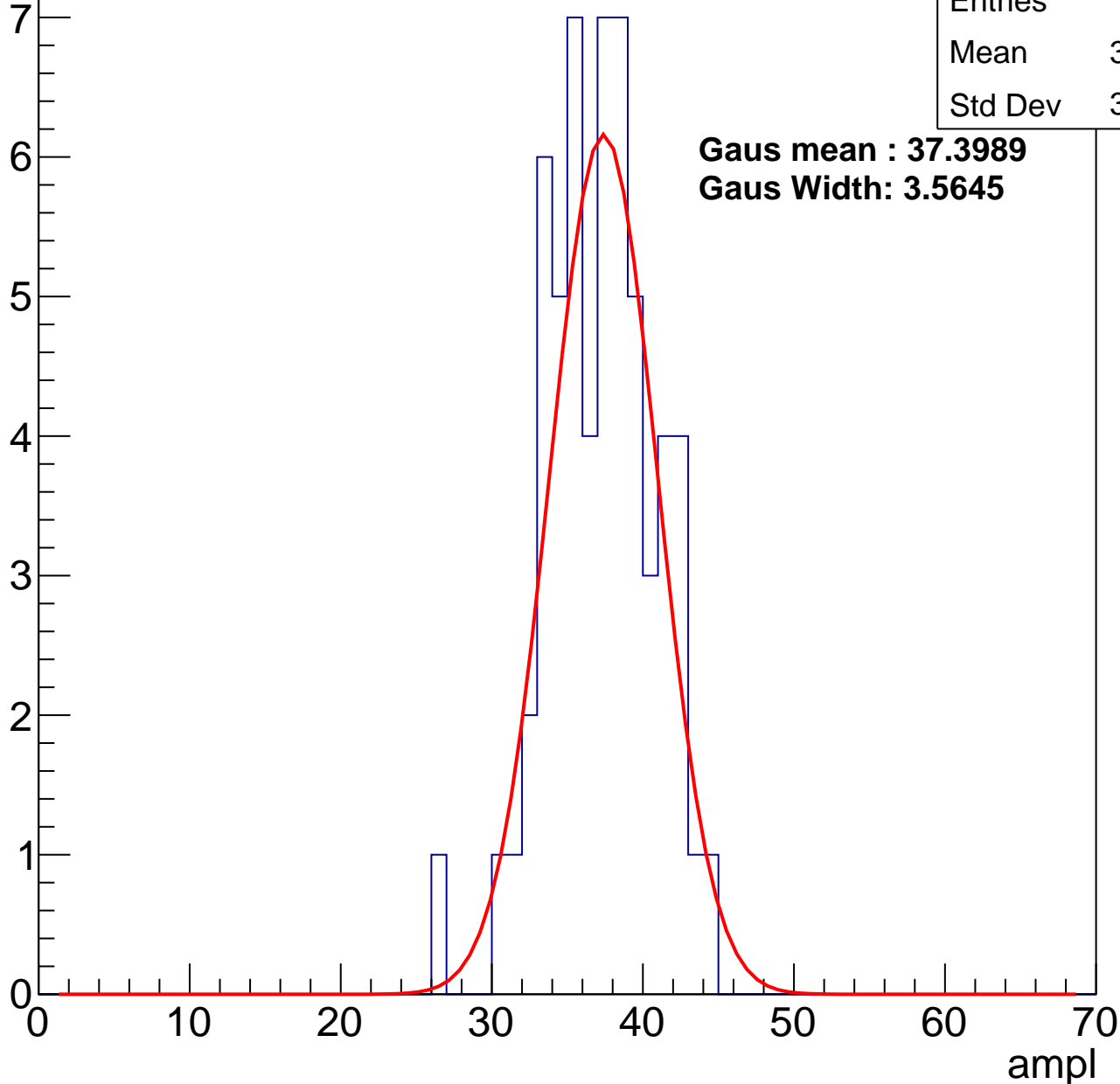
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	36.73
Std Dev	3.512

**Gaus mean : 37.3989**

**Gaus Width: 3.5645**



# B1L003S, U6-ch77, adc2

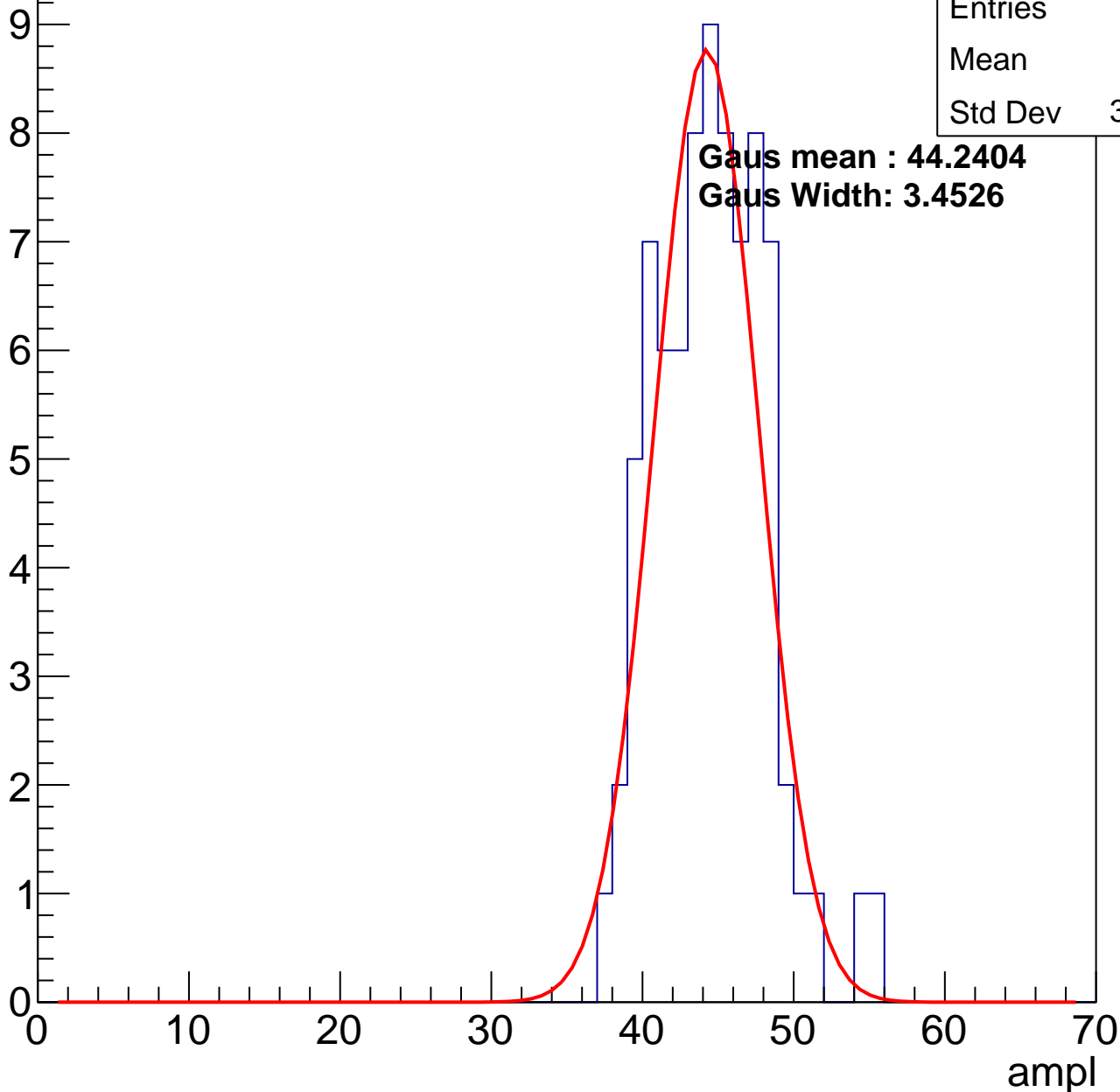
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	80
Mean	44.1
Std Dev	3.569

**Gaus mean : 44.2404**

**Gaus Width: 3.4526**

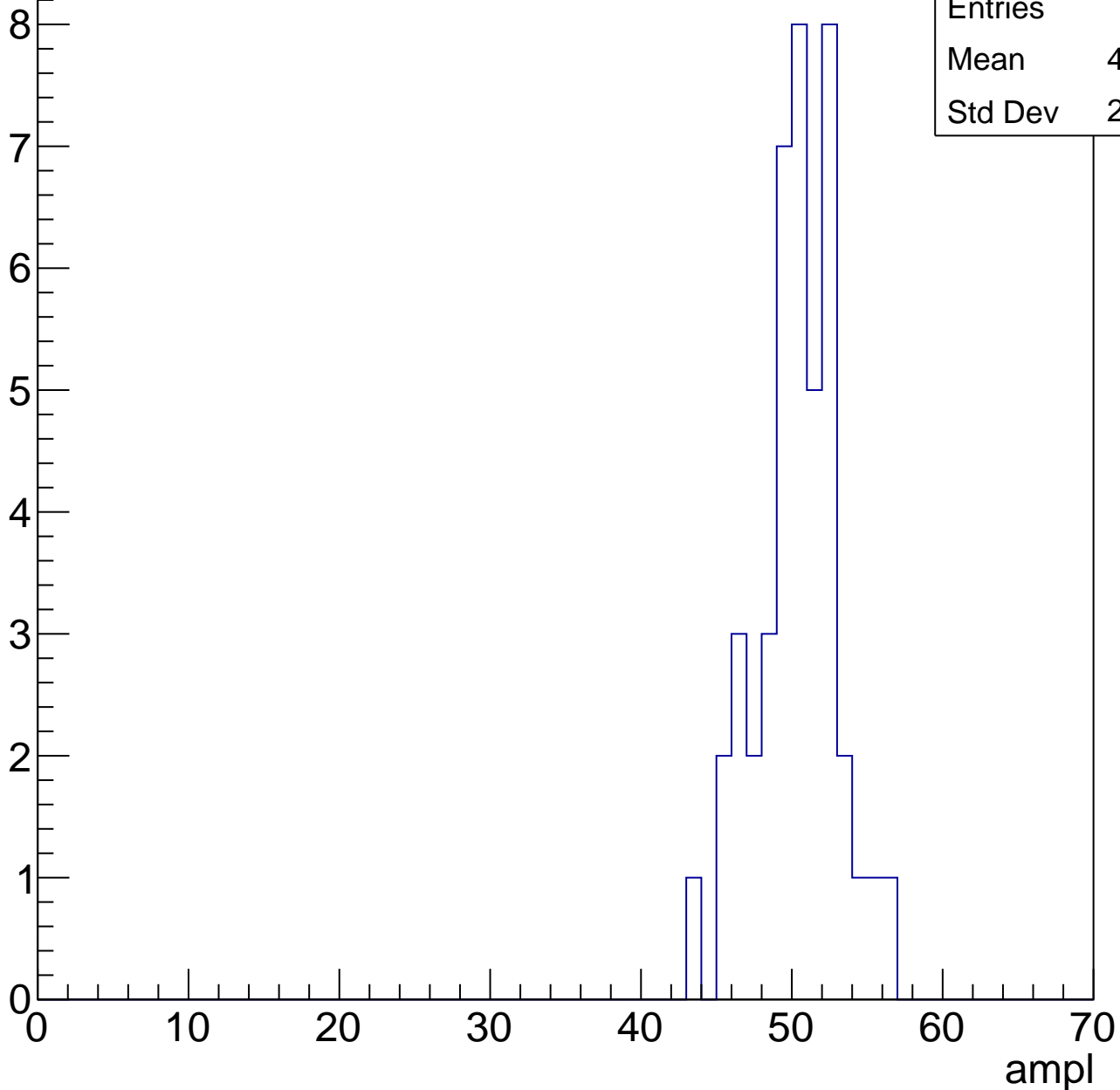


# B1L003S, U6-ch77, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	44
Mean	49.86
Std Dev	2.676

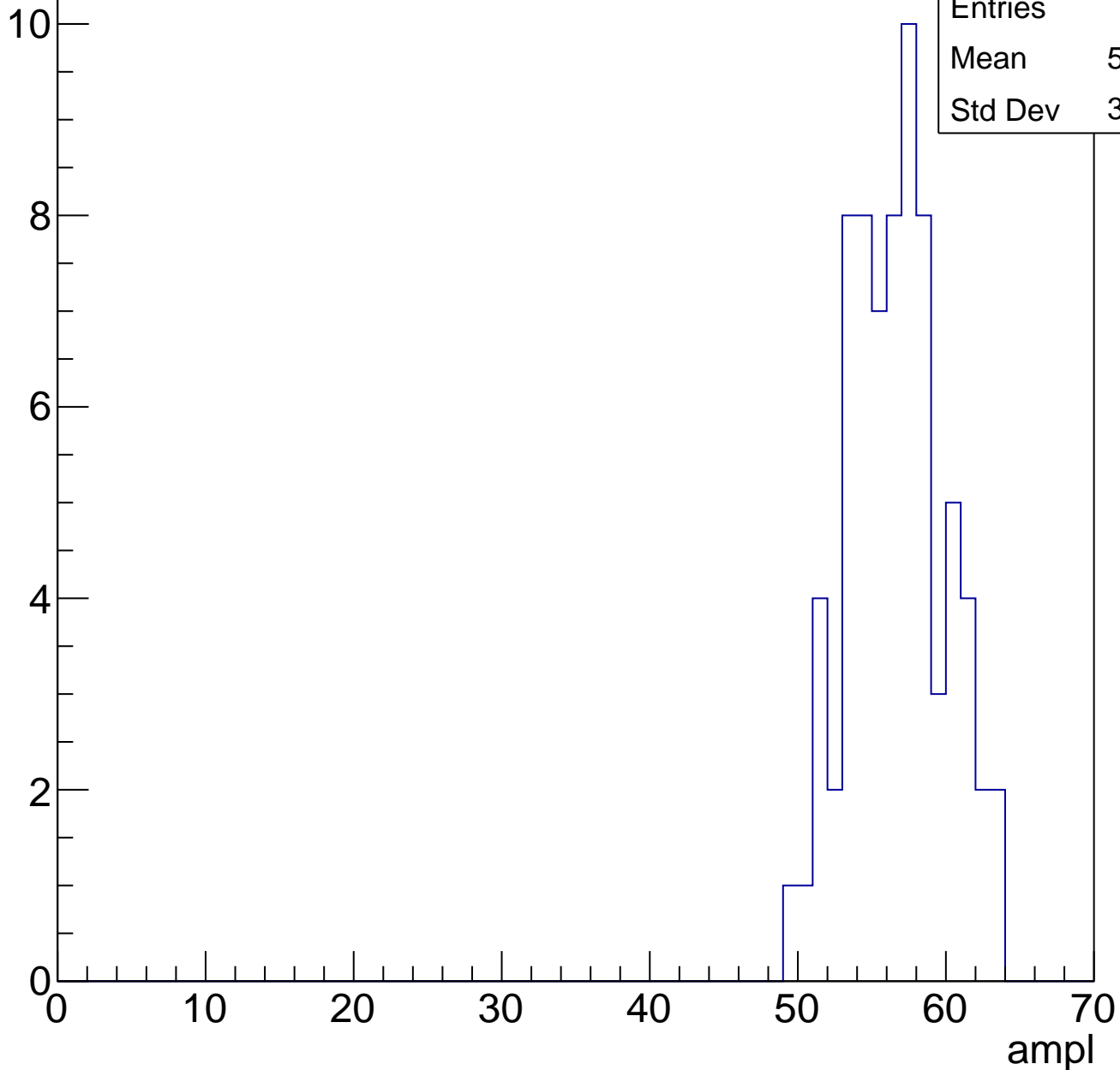


# B1L003S, U6-ch77, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

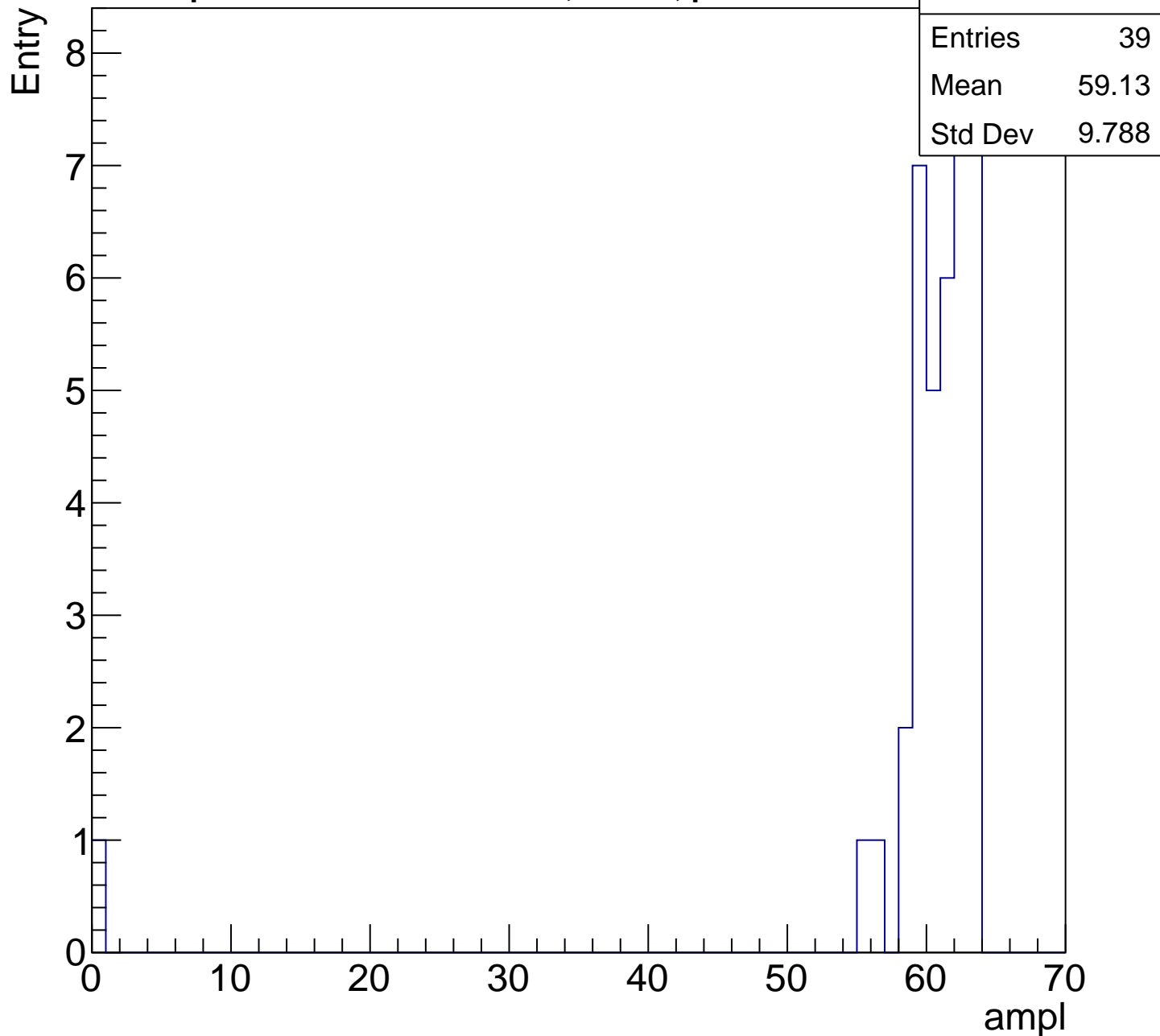
Entries	73
Mean	56.18
Std Dev	3.194

Entry



# B1L003S, U6-ch77, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2



# B1L003S, U6-ch77, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

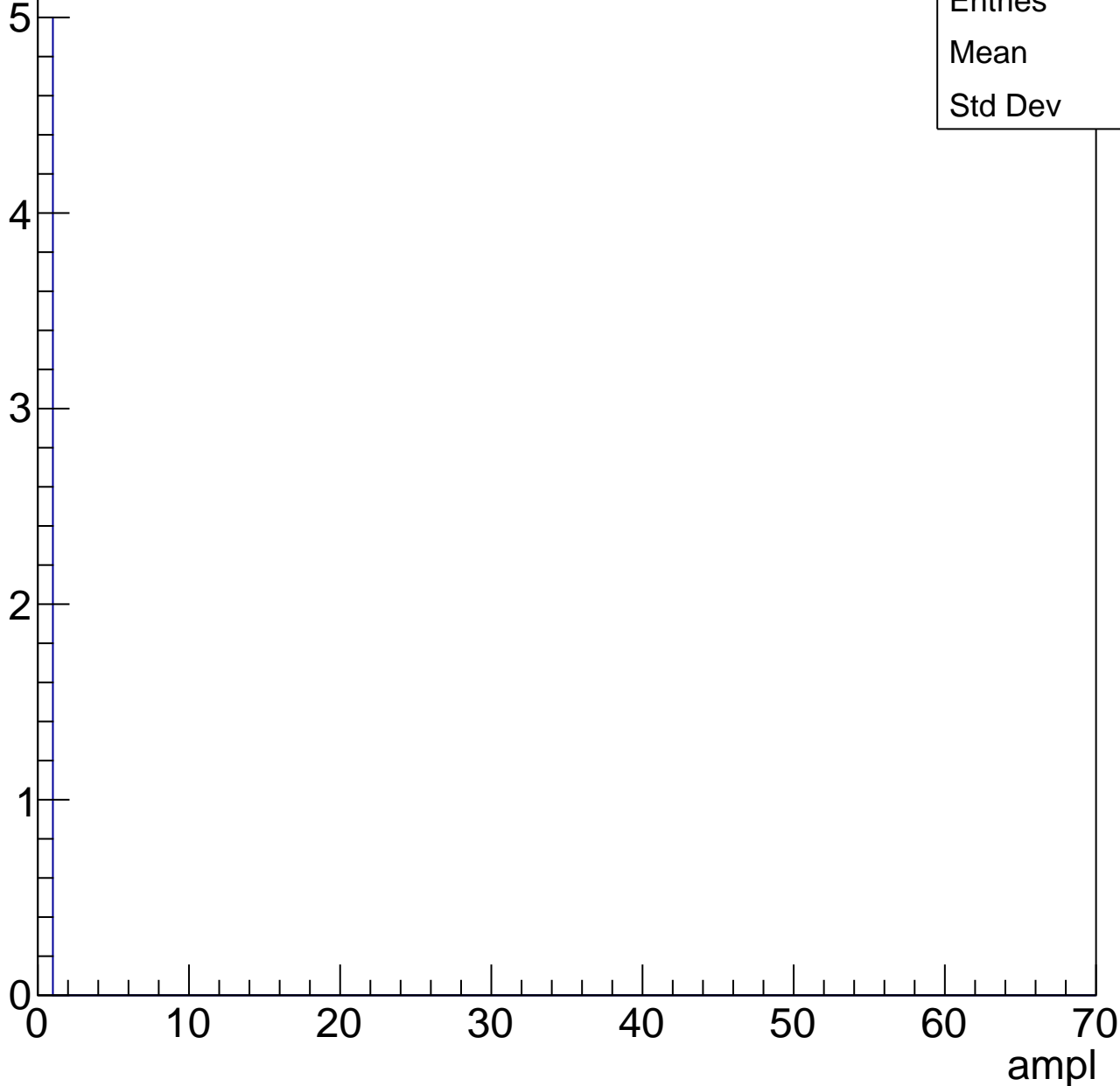


# B1L003S, U6-ch77, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	5
Mean	0
Std Dev	0



# B1L003S, U6-ch78, adc0

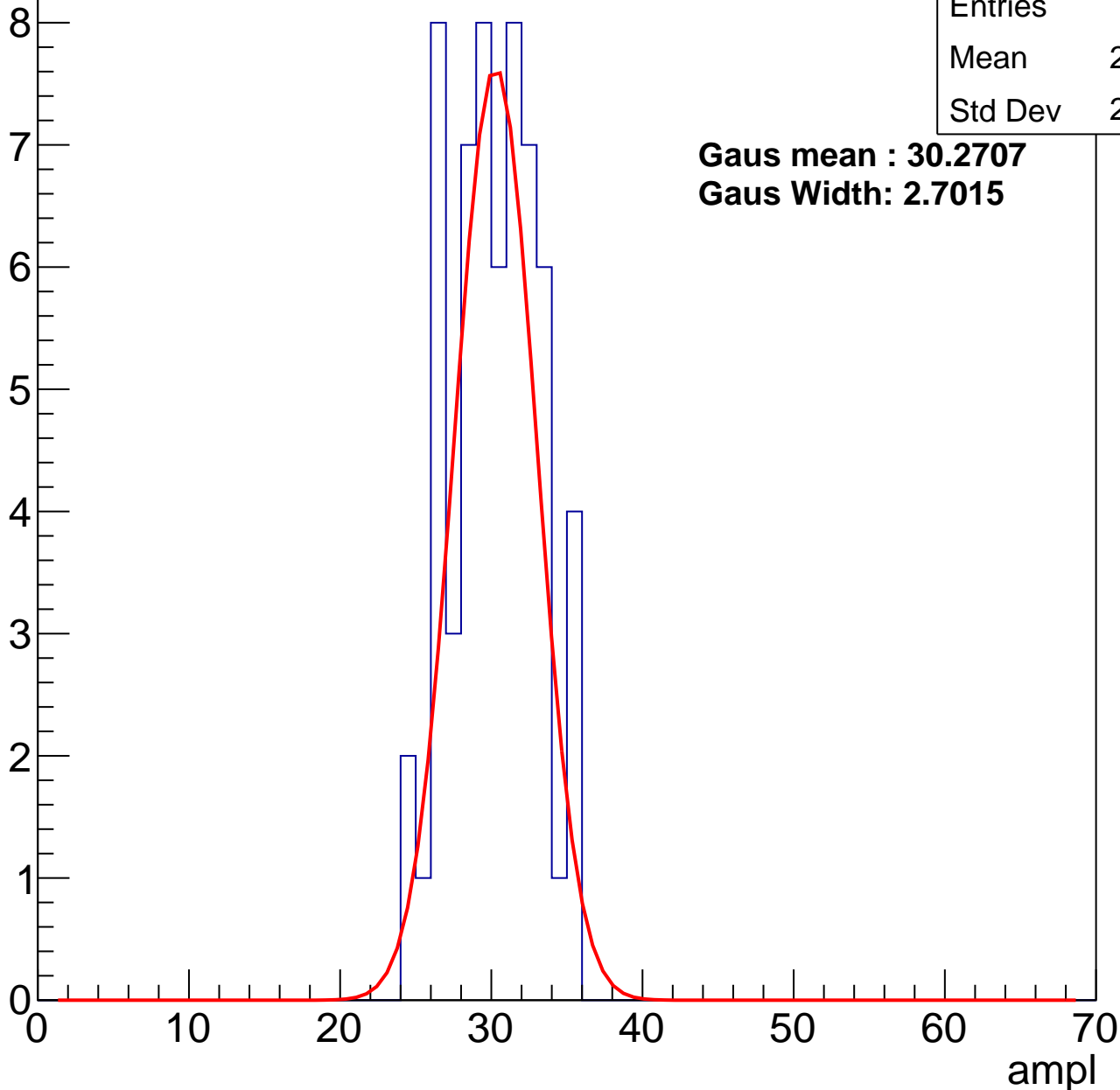
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	29.74
Std Dev	2.834

**Gaus mean : 30.2707**

**Gaus Width: 2.7015**



# B1L003S, U6-ch78, adc1

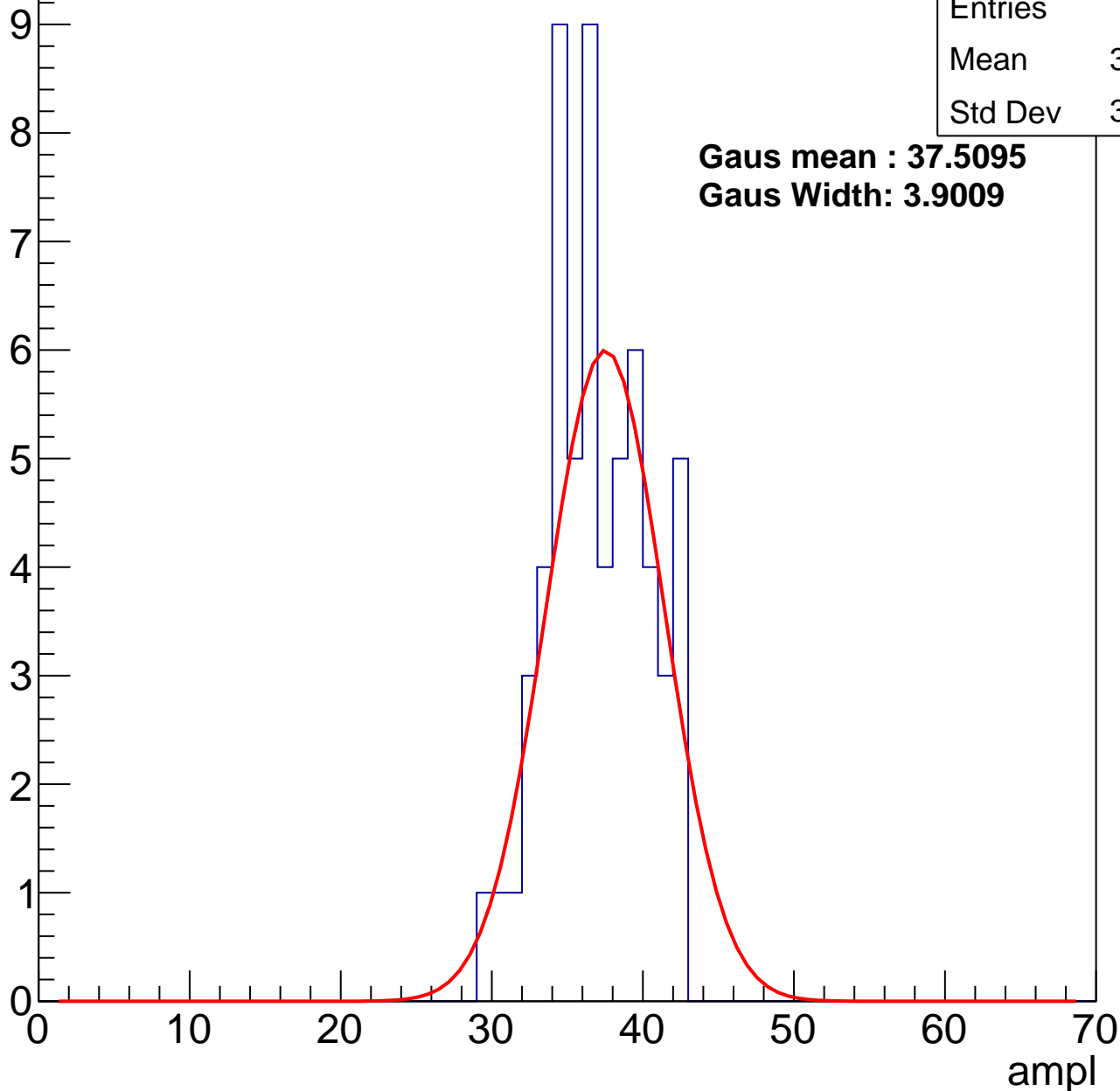
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	36.47
Std Dev	3.212

**Gaus mean : 37.5095**

**Gaus Width: 3.9009**



# B1L003S, U6-ch78, adc2

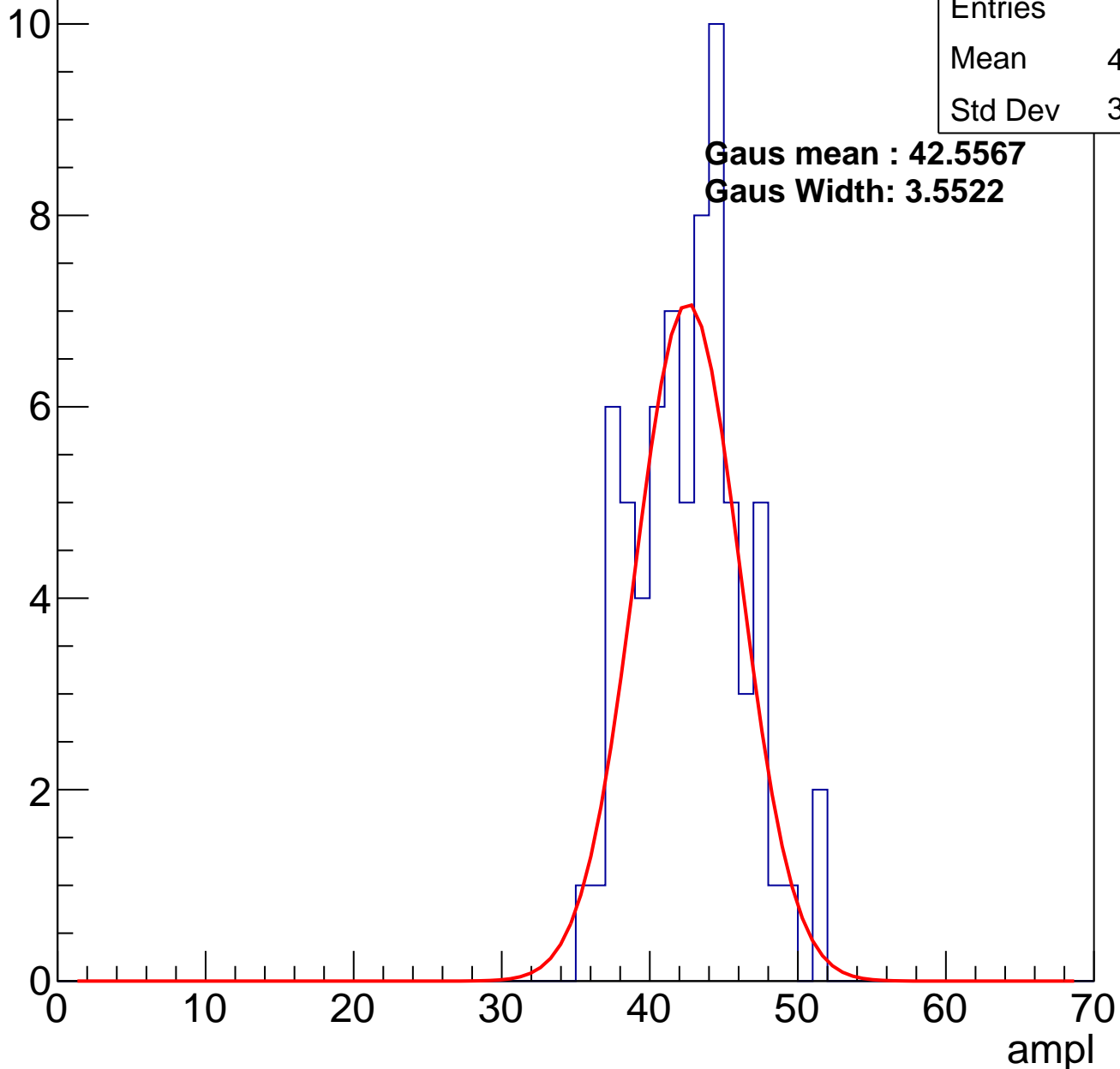
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	70
Mean	42.24
Std Dev	3.567

**Gaus mean : 42.5567**

**Gaus Width: 3.5522**

Entry

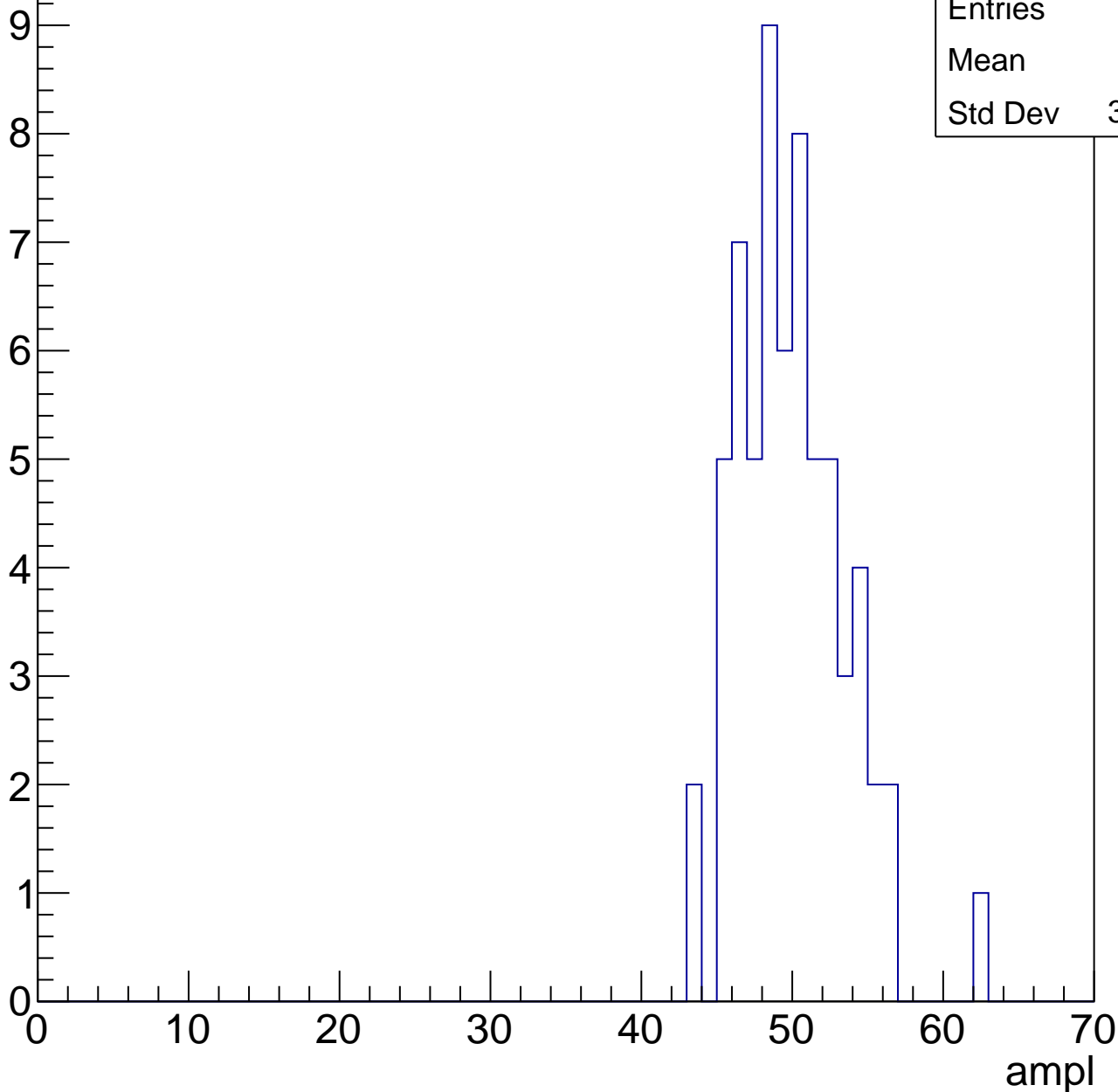


# B1L003S, U6-ch78, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

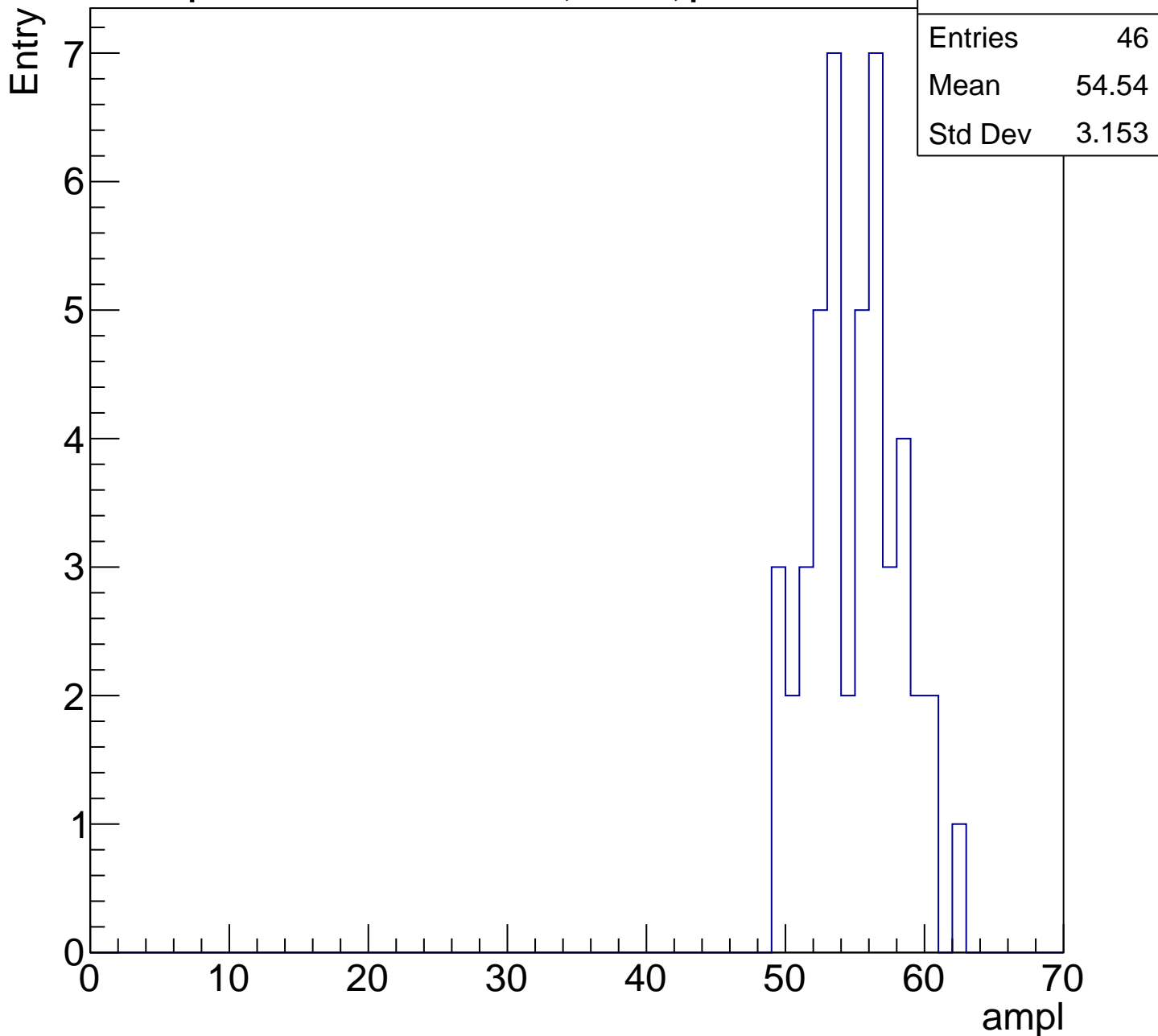
Entry

Entries	64
Mean	49.5
Std Dev	3.509



# B1L003S, U6-ch78, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

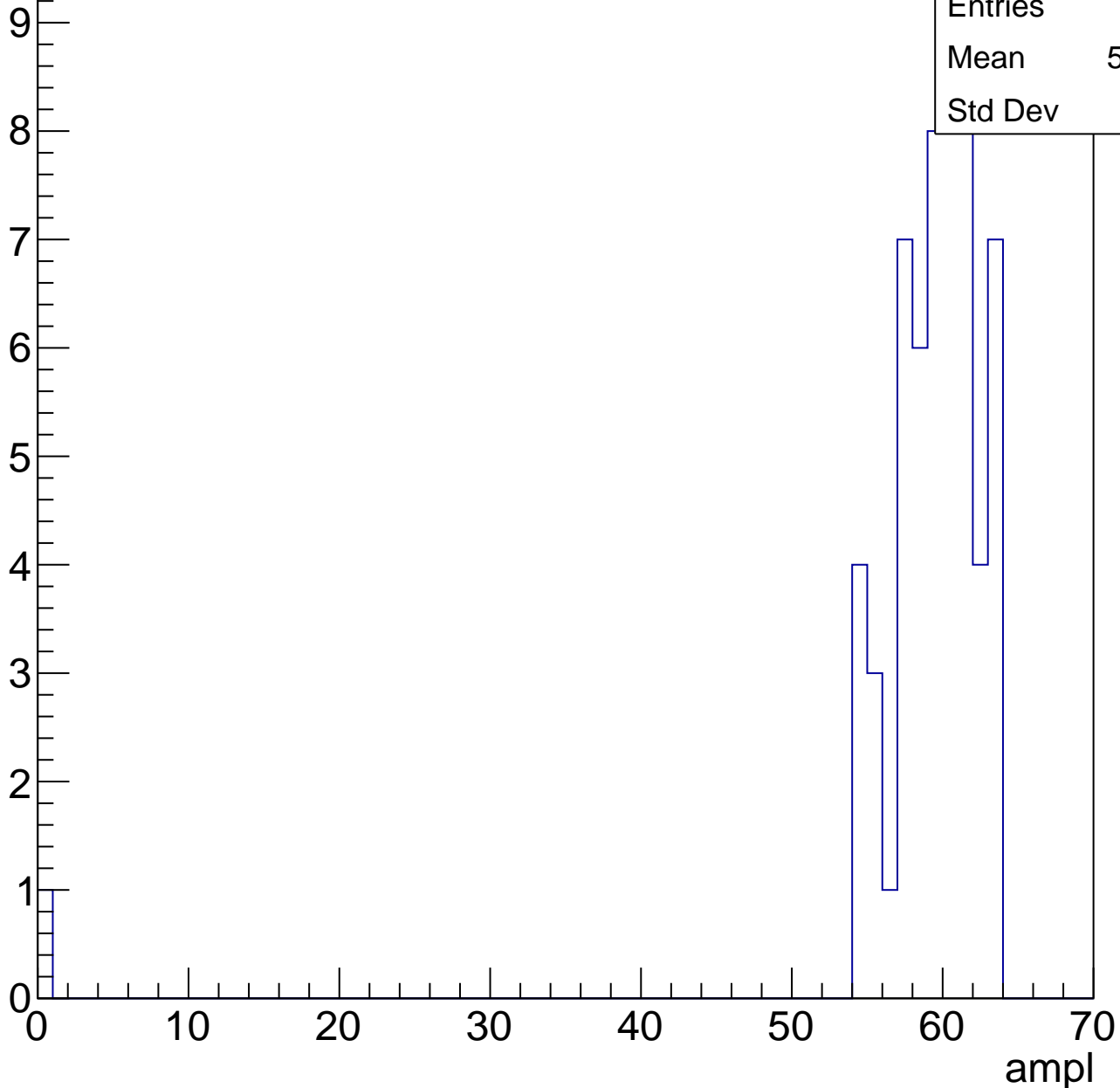


# B1L003S, U6-ch78, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

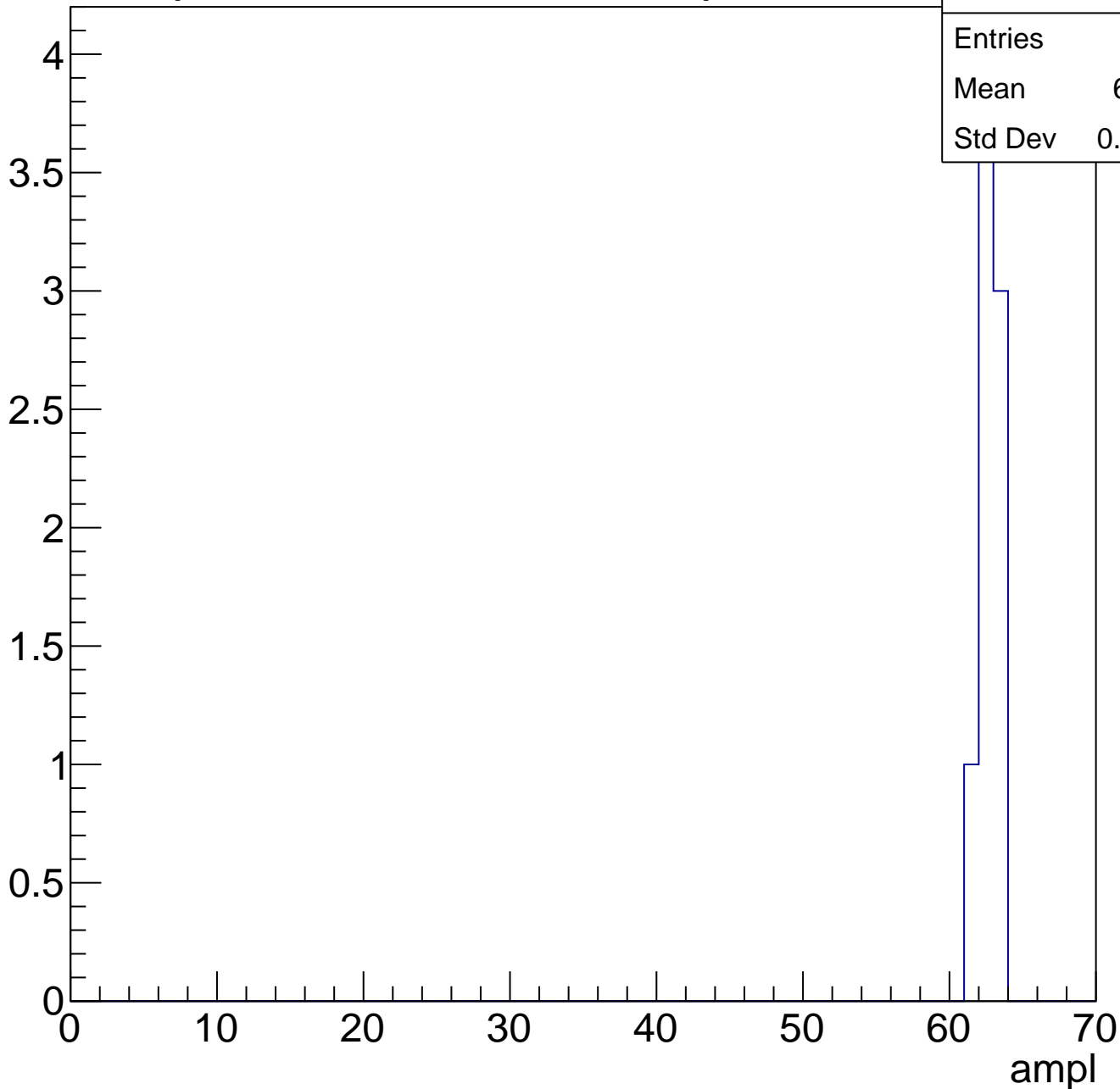
Entries	58
Mean	58.17
Std Dev	8.12



# B1L003S, U6-ch78, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

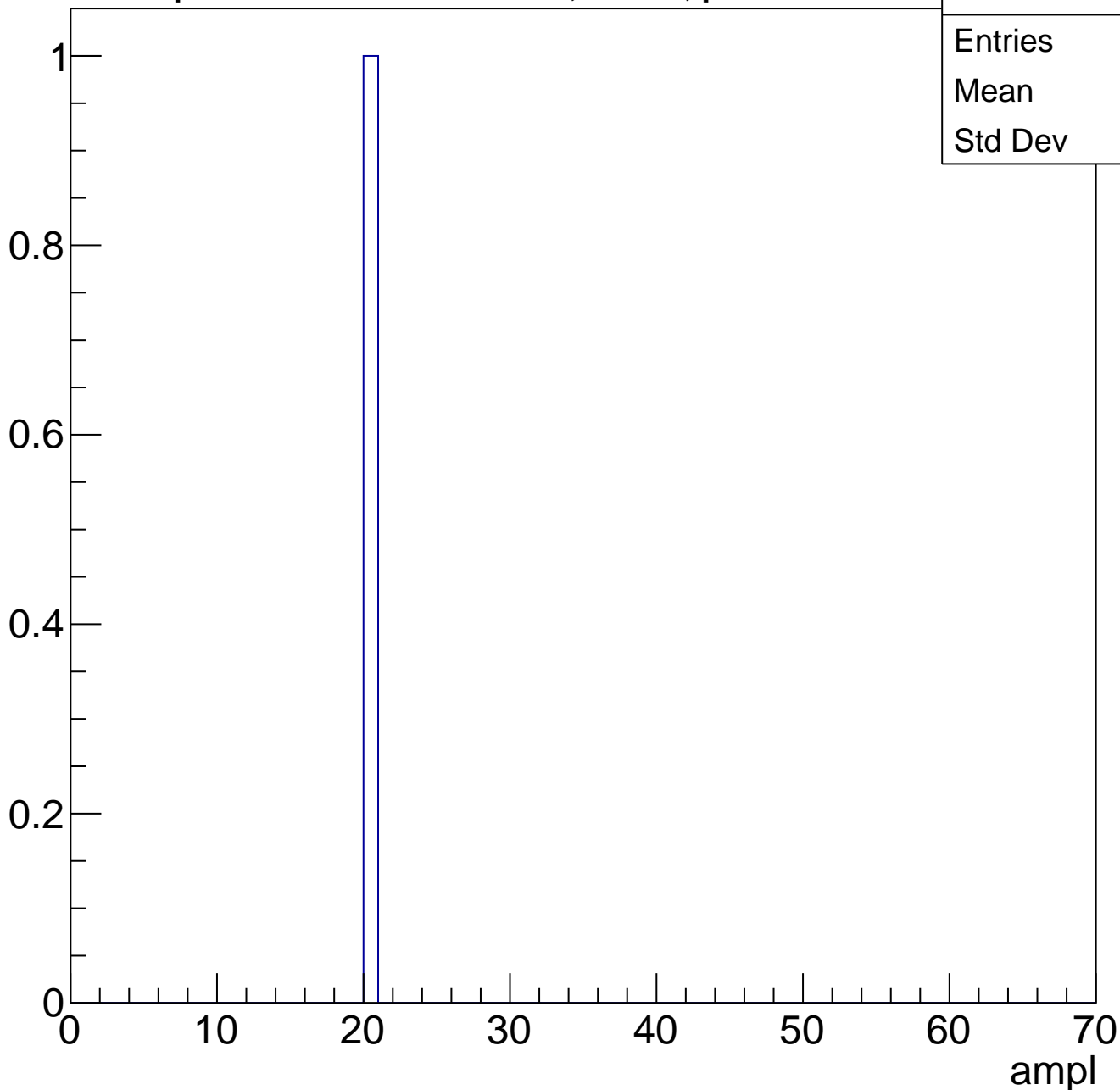




# B1L003S, U6-ch78, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	20
Std Dev	0

# B1L003S, U6-ch79, adc0

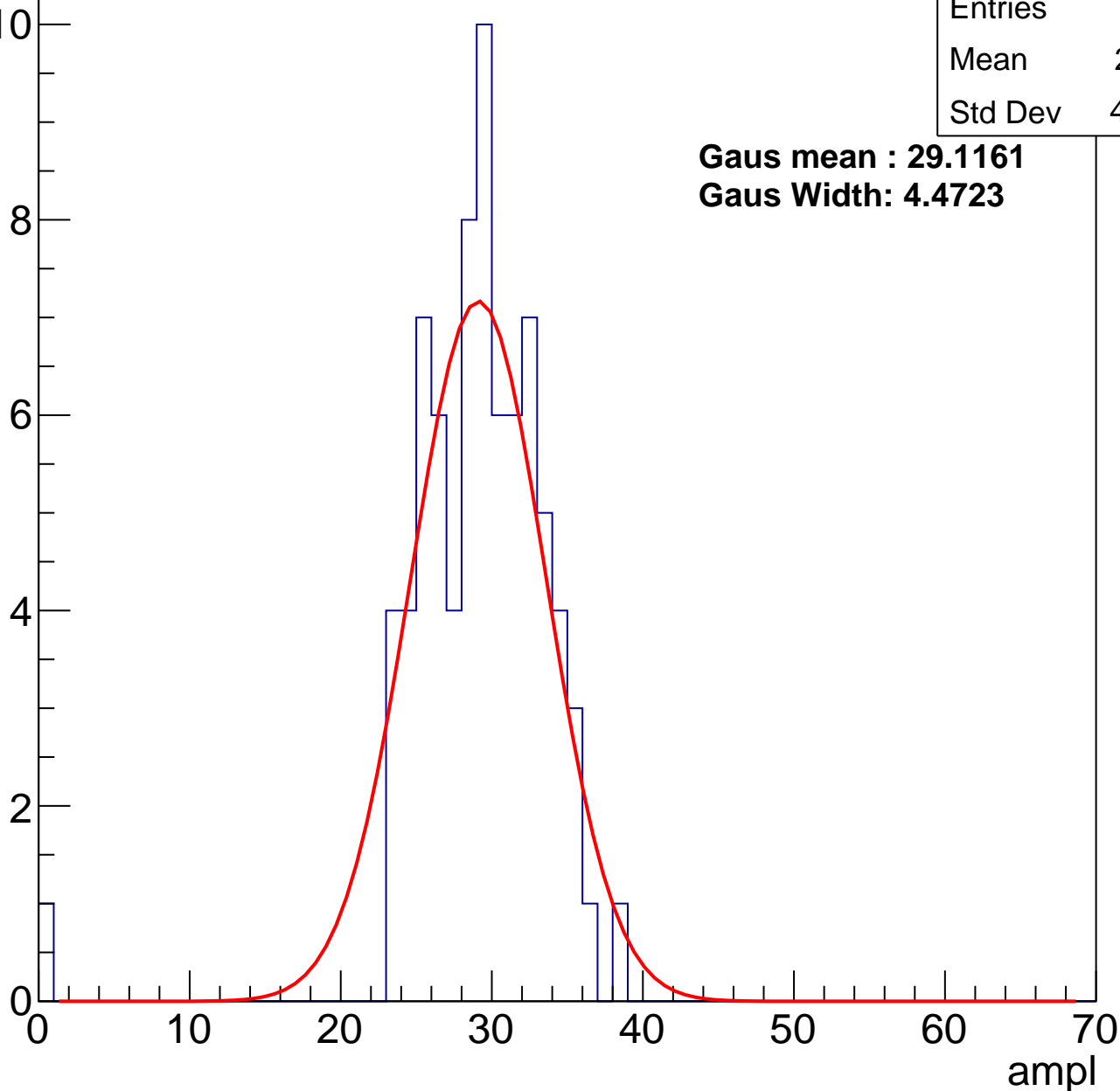
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	77
Mean	28.71
Std Dev	4.808

**Gaus mean : 29.1161**

**Gaus Width: 4.4723**



# B1L003S, U6-ch79, adc1

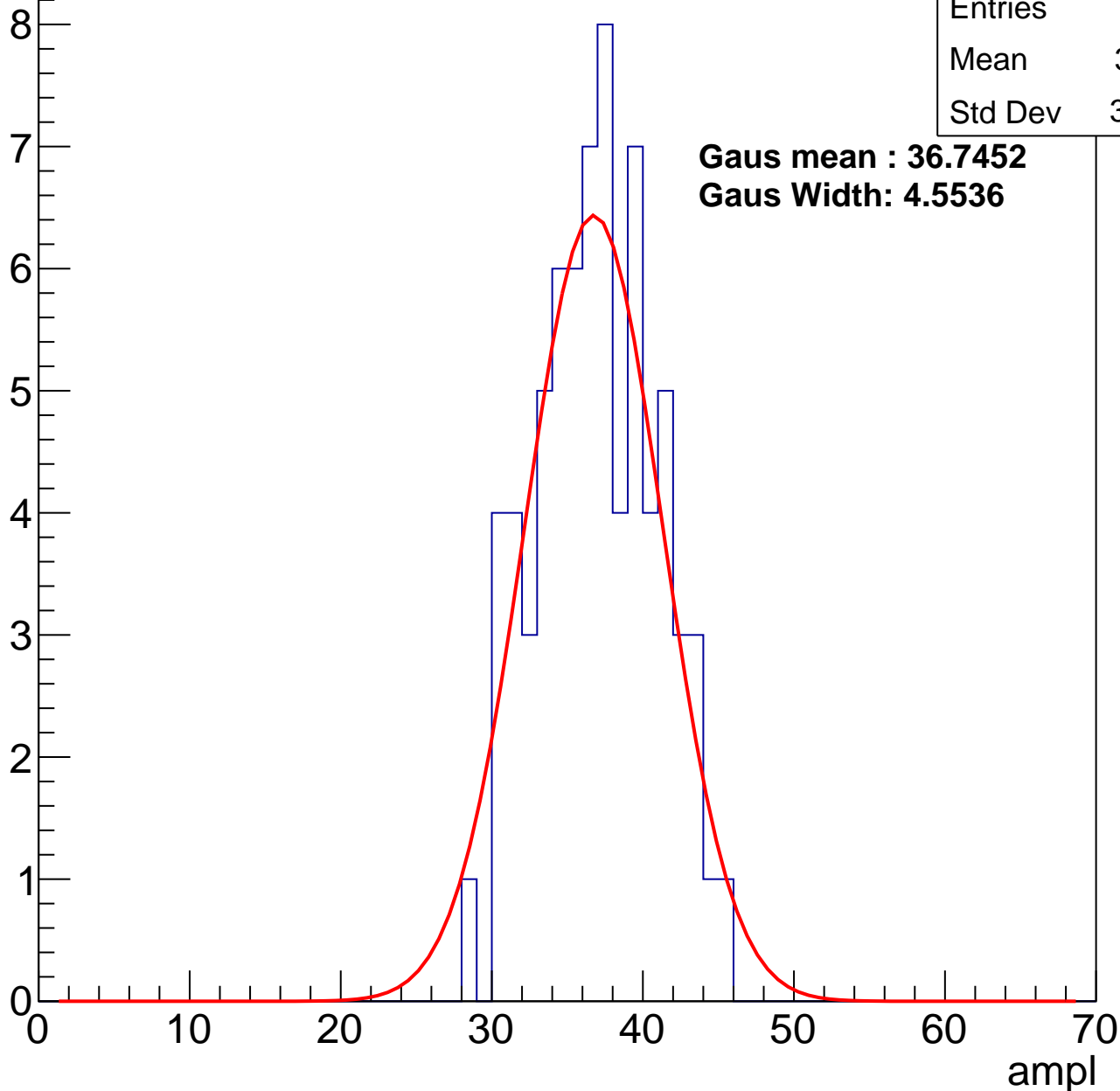
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	72
Mean	36.51
Std Dev	3.887

**Gaus mean : 36.7452**

**Gaus Width: 4.5536**



# B1L003S, U6-ch79, adc2

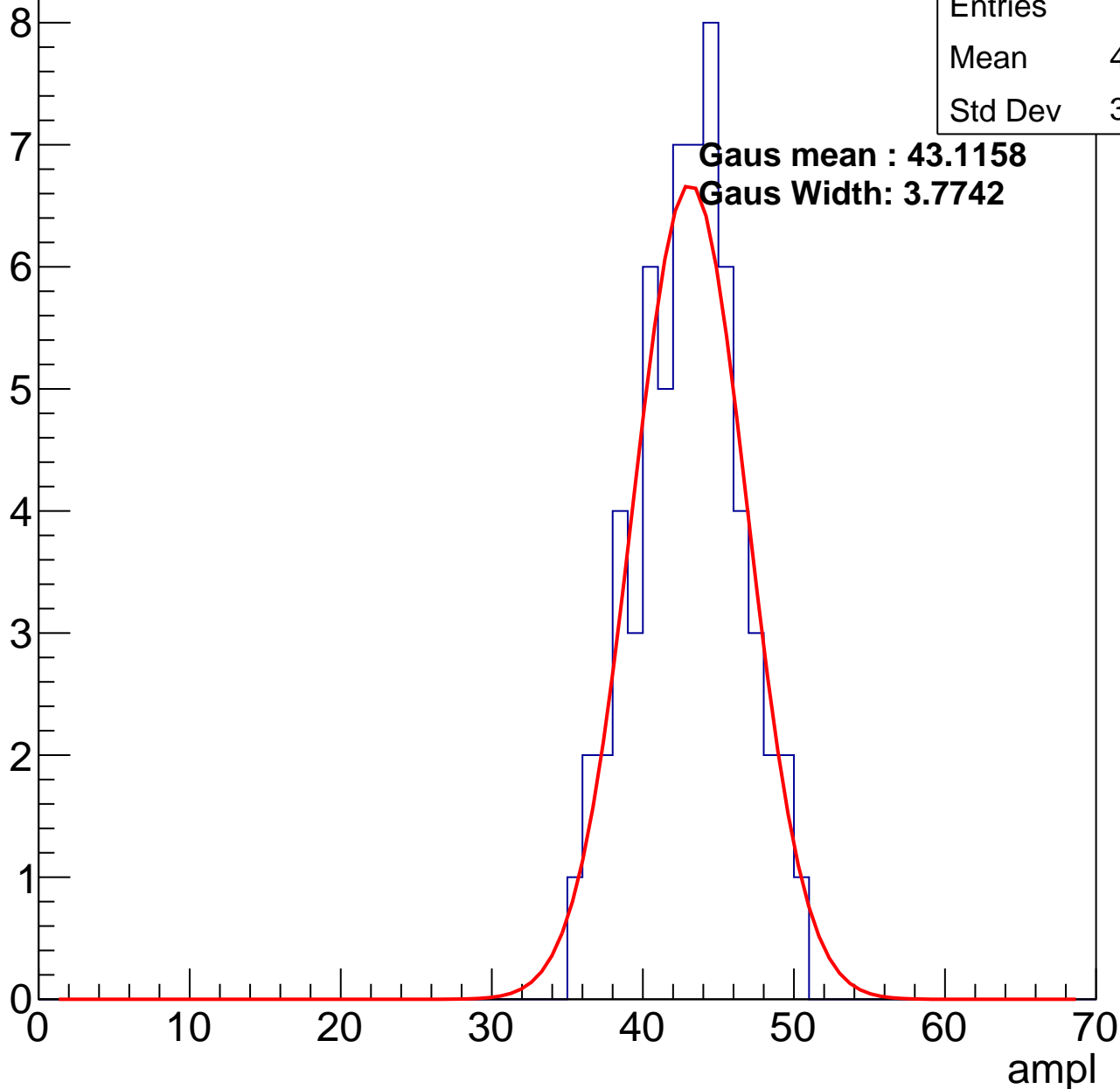
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	42.56
Std Dev	3.422

**Gaus mean : 43.1158**

**Gaus Width: 3.7742**

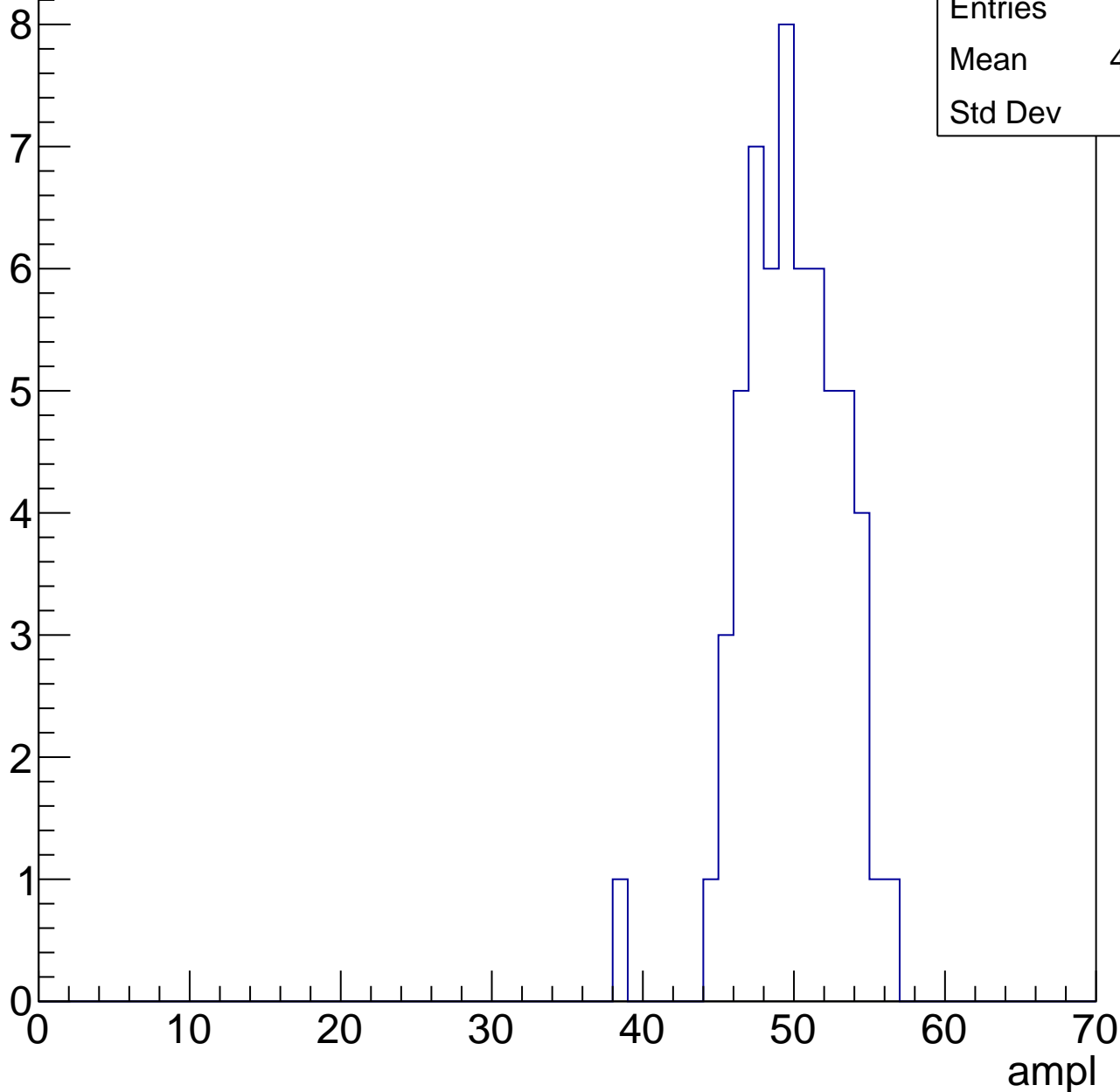


# B1L003S, U6-ch79, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	49.39
Std Dev	3.2

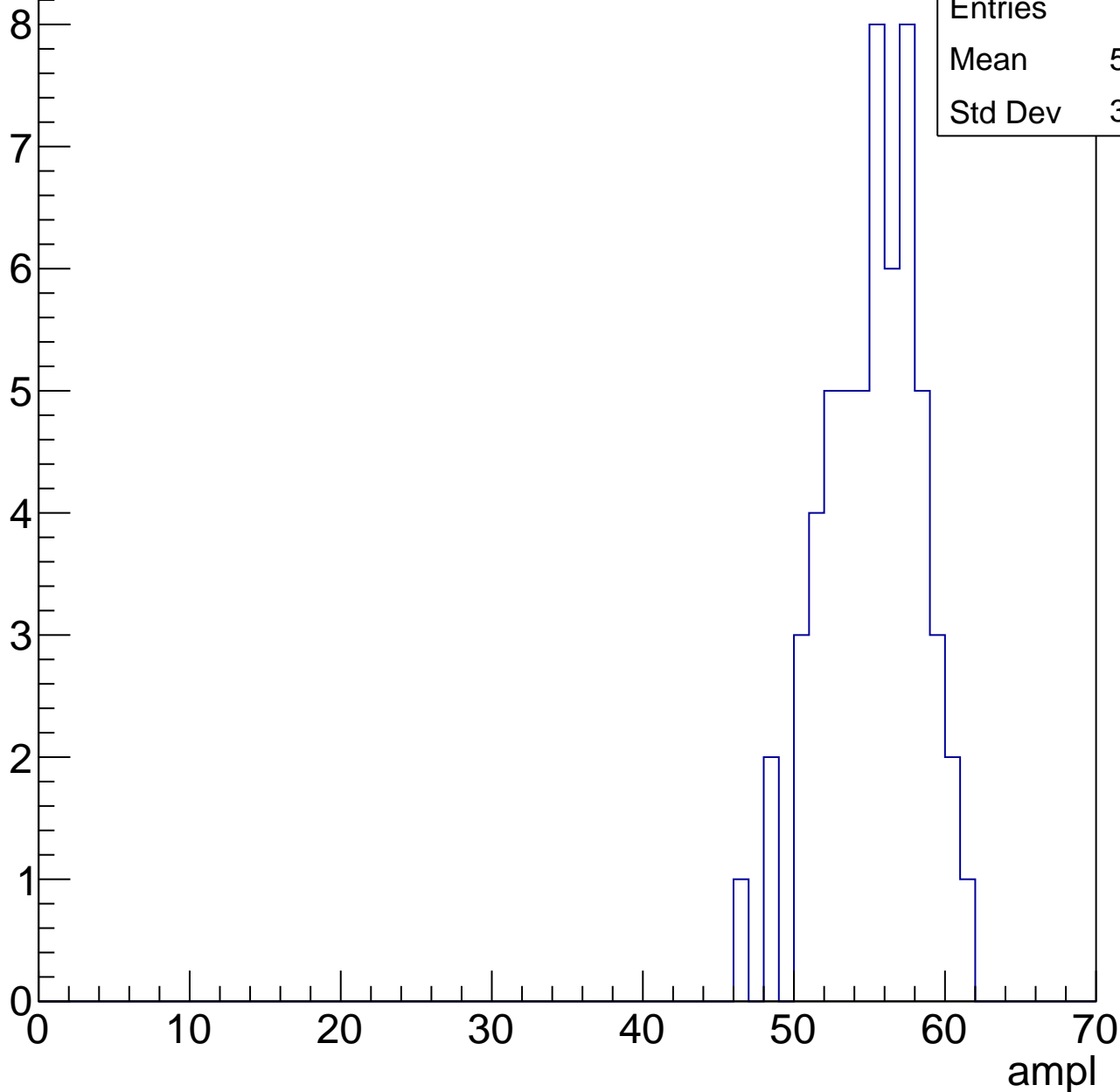


# B1L003S, U6-ch79, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	54.67
Std Dev	3.213



# B1L003S, U6-ch79, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	47
Mean	59.87
Std Dev	2.294

ampl

0 10 20 30 40 50 60 70

0

1

2

3

4

5

6

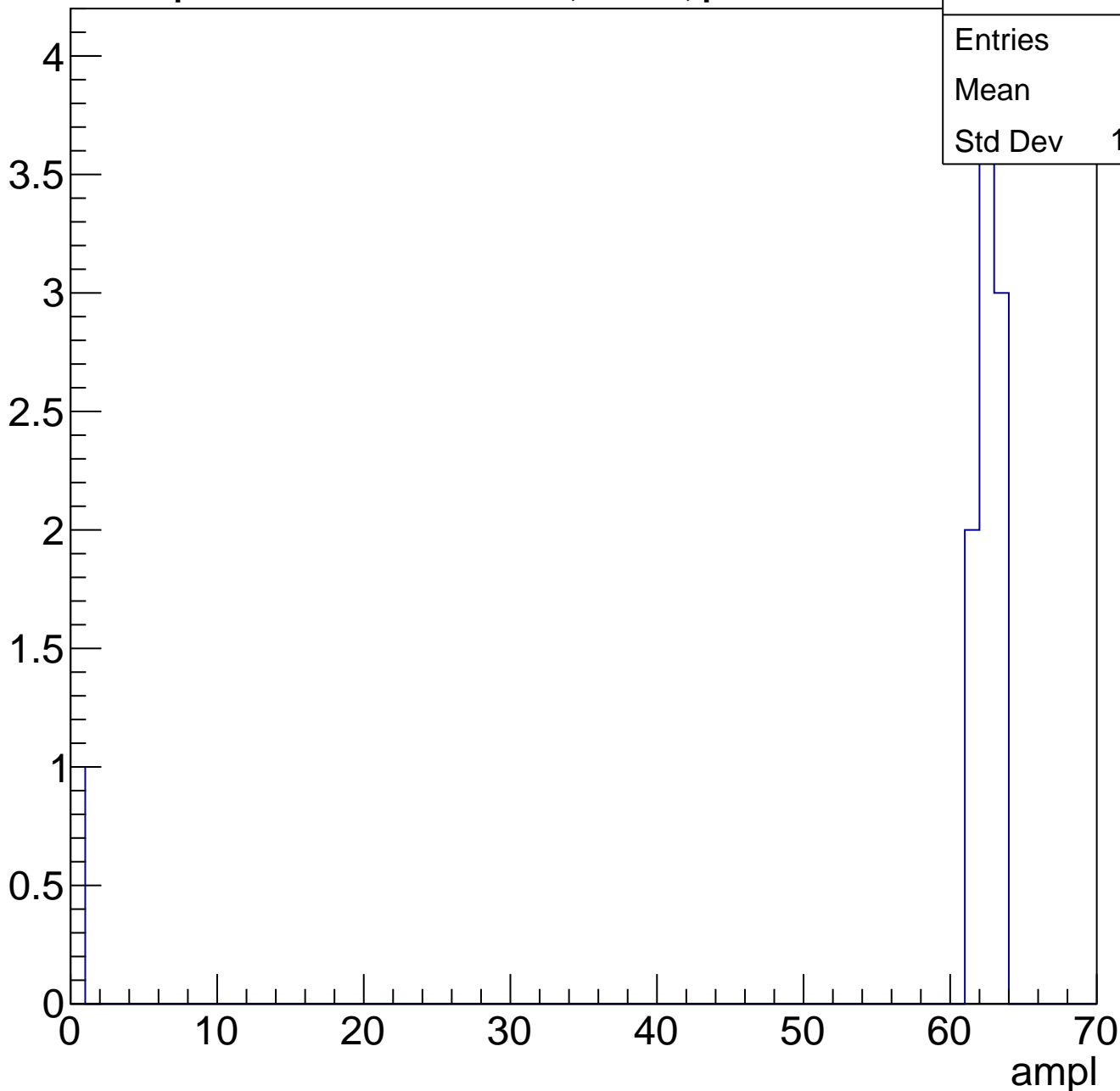
7

8

# B1L003S, U6-ch79, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch79, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U6-ch80, adc0

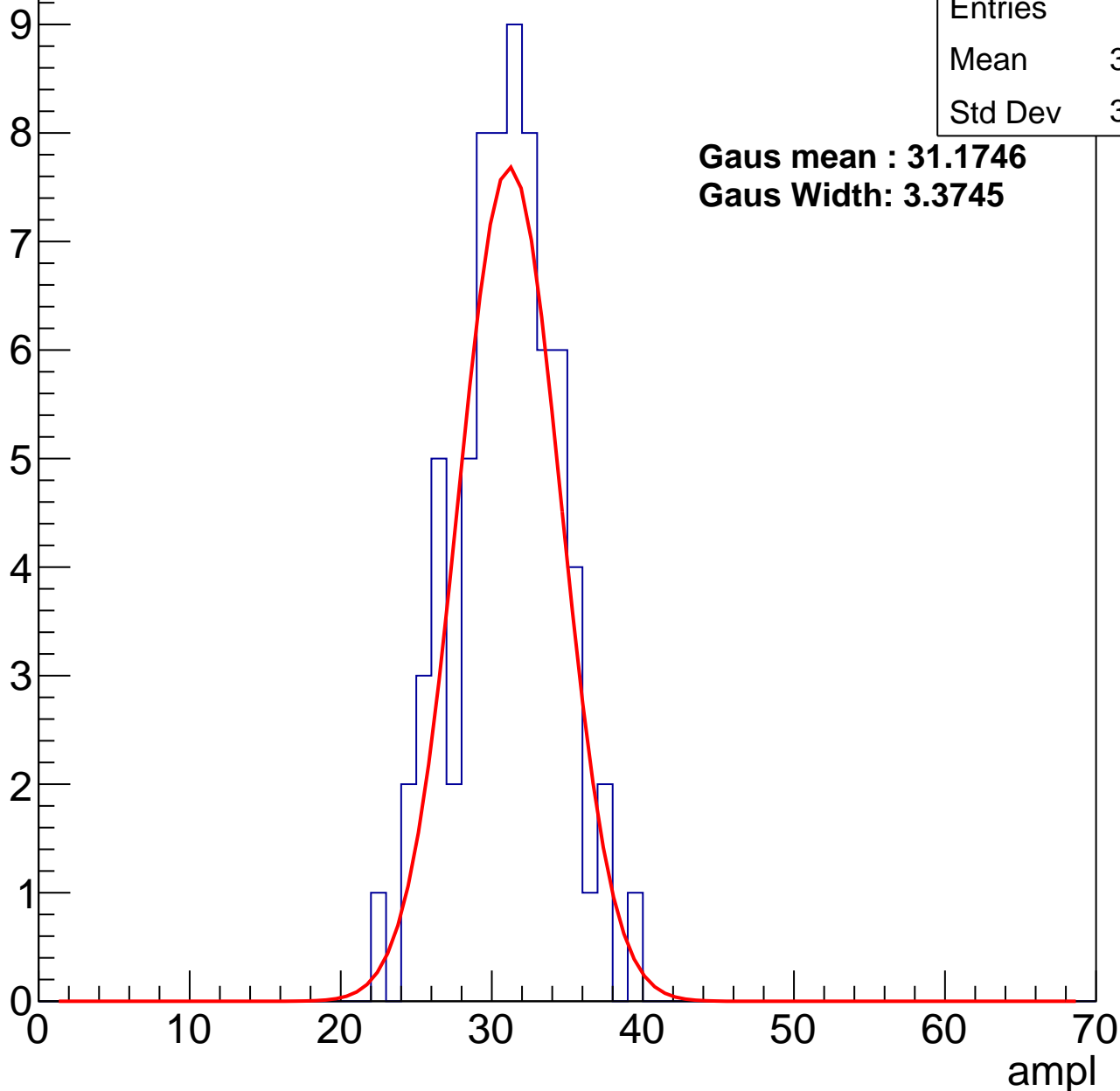
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	71
Mean	30.52
Std Dev	3.406

**Gaus mean : 31.1746**

**Gaus Width: 3.3745**



# B1L003S, U6-ch80, adc1

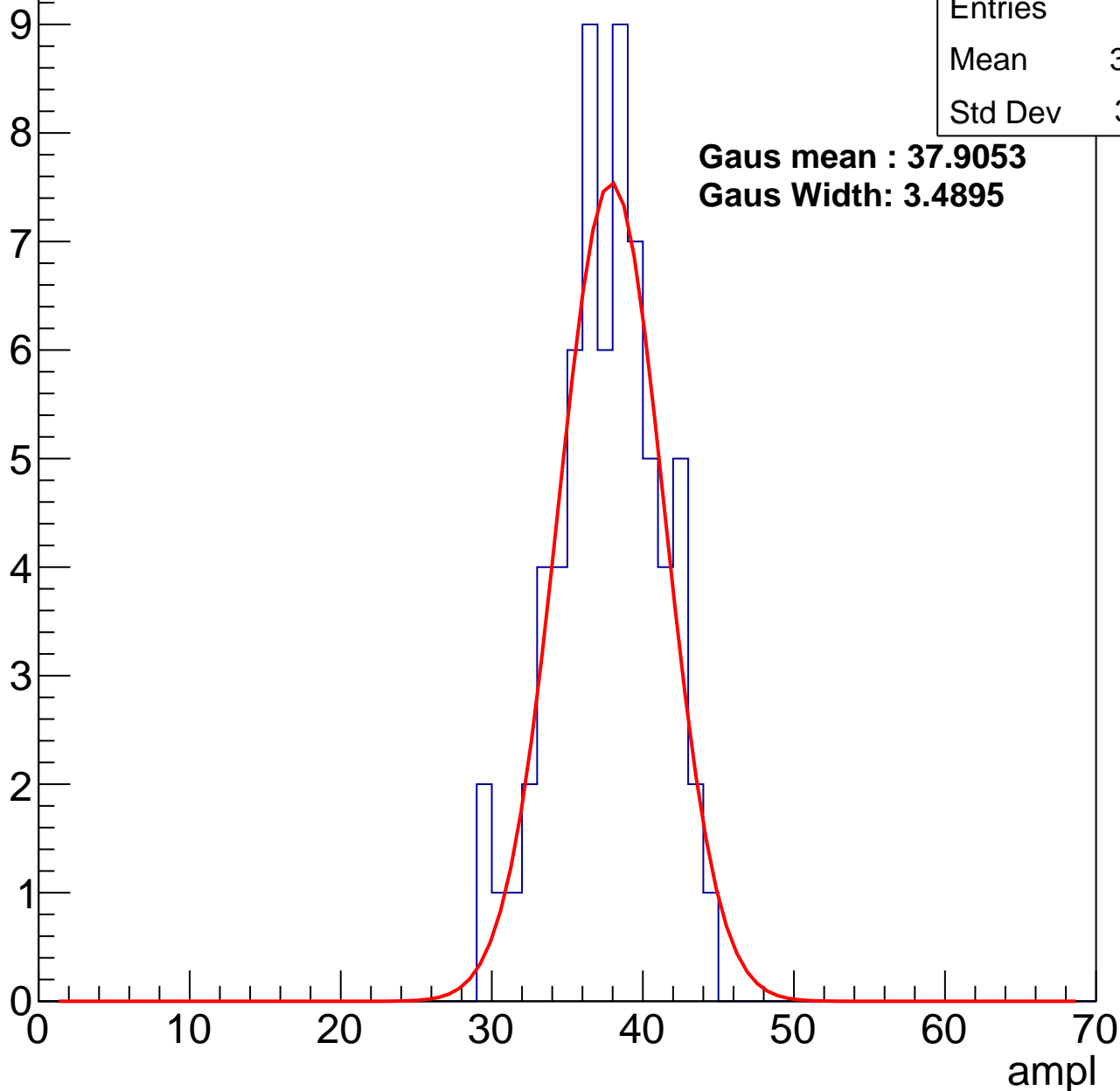
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	37.15
Std Dev	3.401

**Gaus mean : 37.9053**

**Gaus Width: 3.4895**



# B1L003S, U6-ch80, adc2

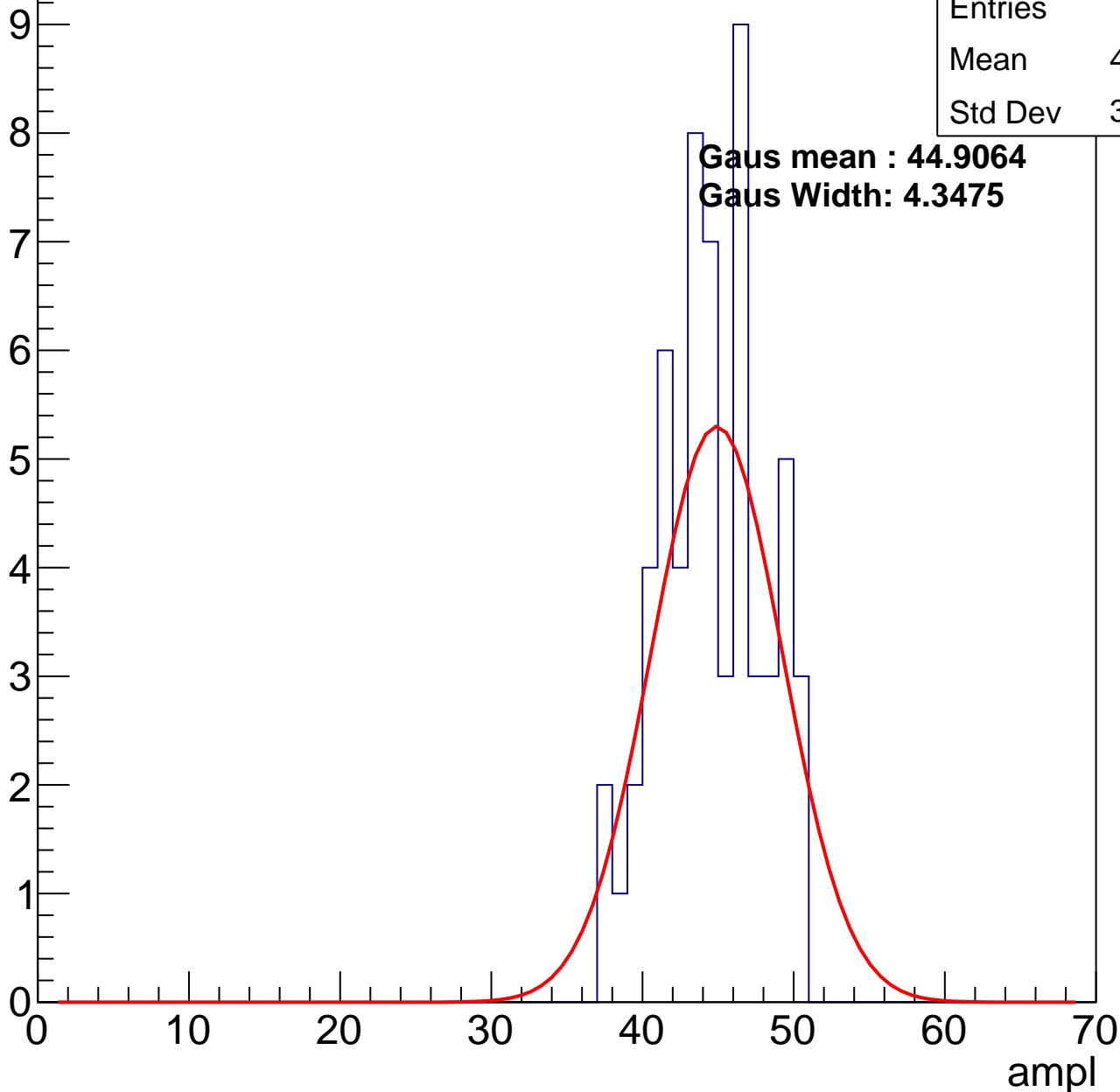
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	44.08
Std Dev	3.348

**Gaus mean : 44.9064**

**Gaus Width: 4.3475**

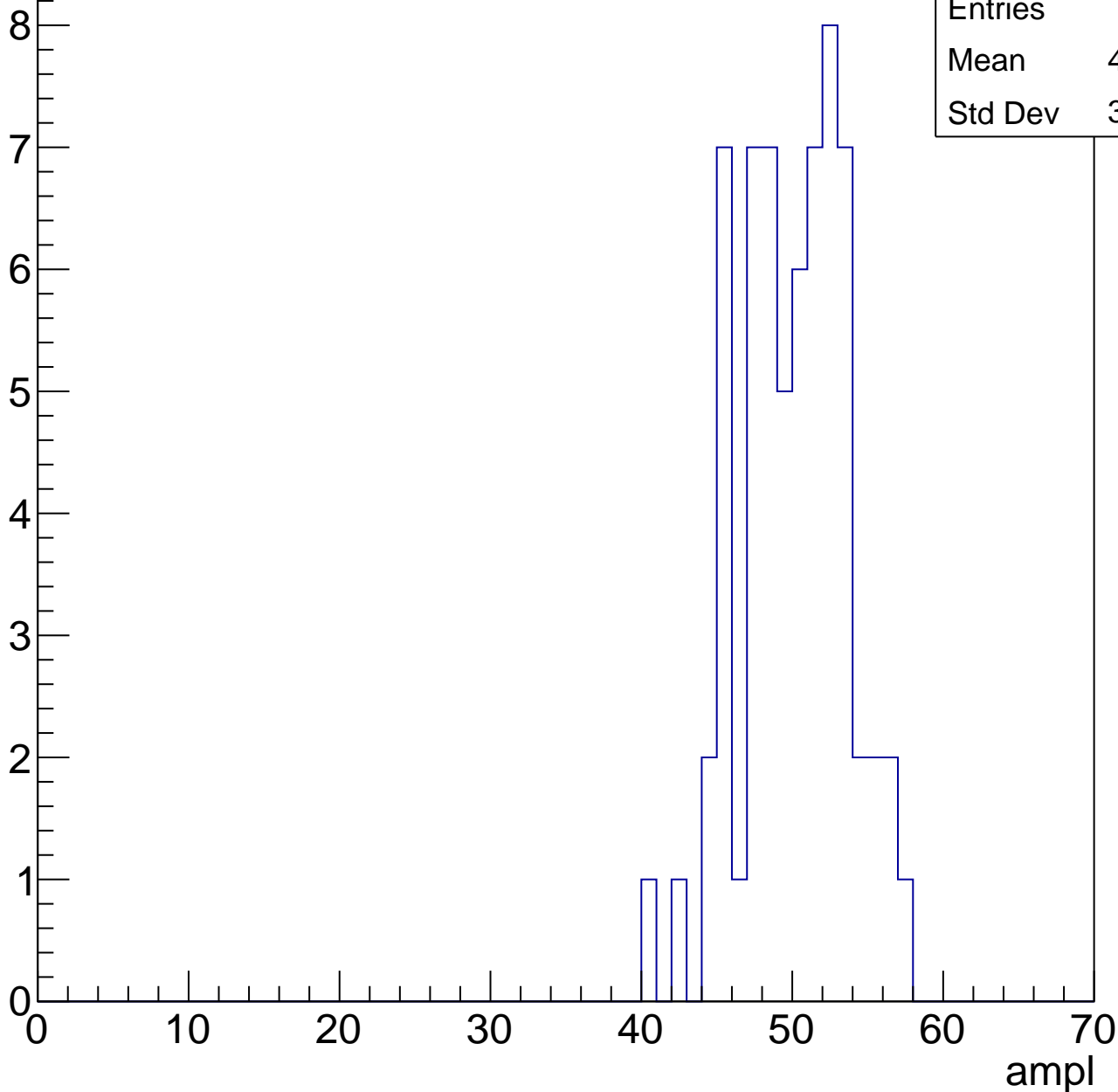


# B1L003S, U6-ch80, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	49.58
Std Dev	3.516

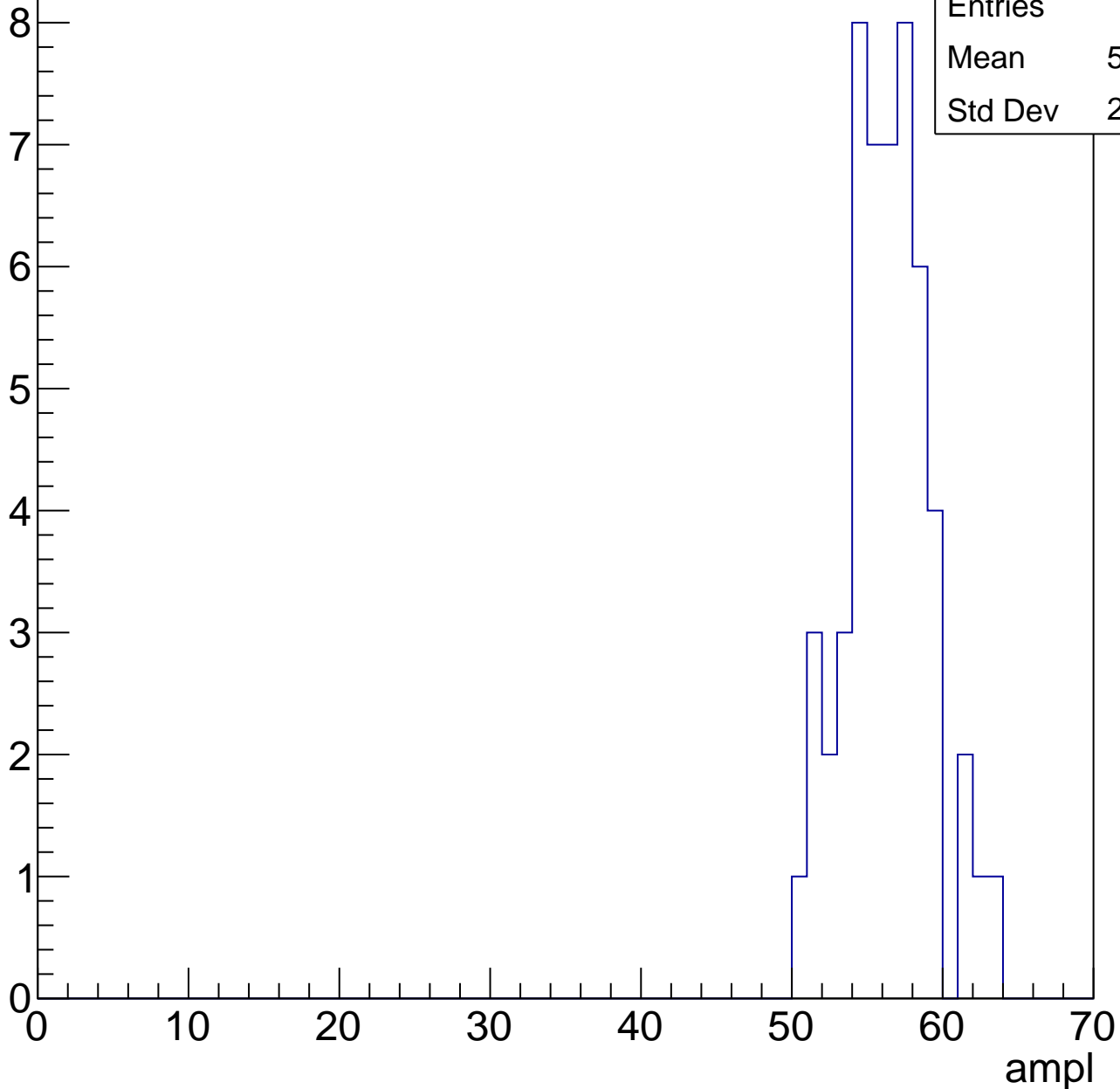


# B1L003S, U6-ch80, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	55.89
Std Dev	2.786

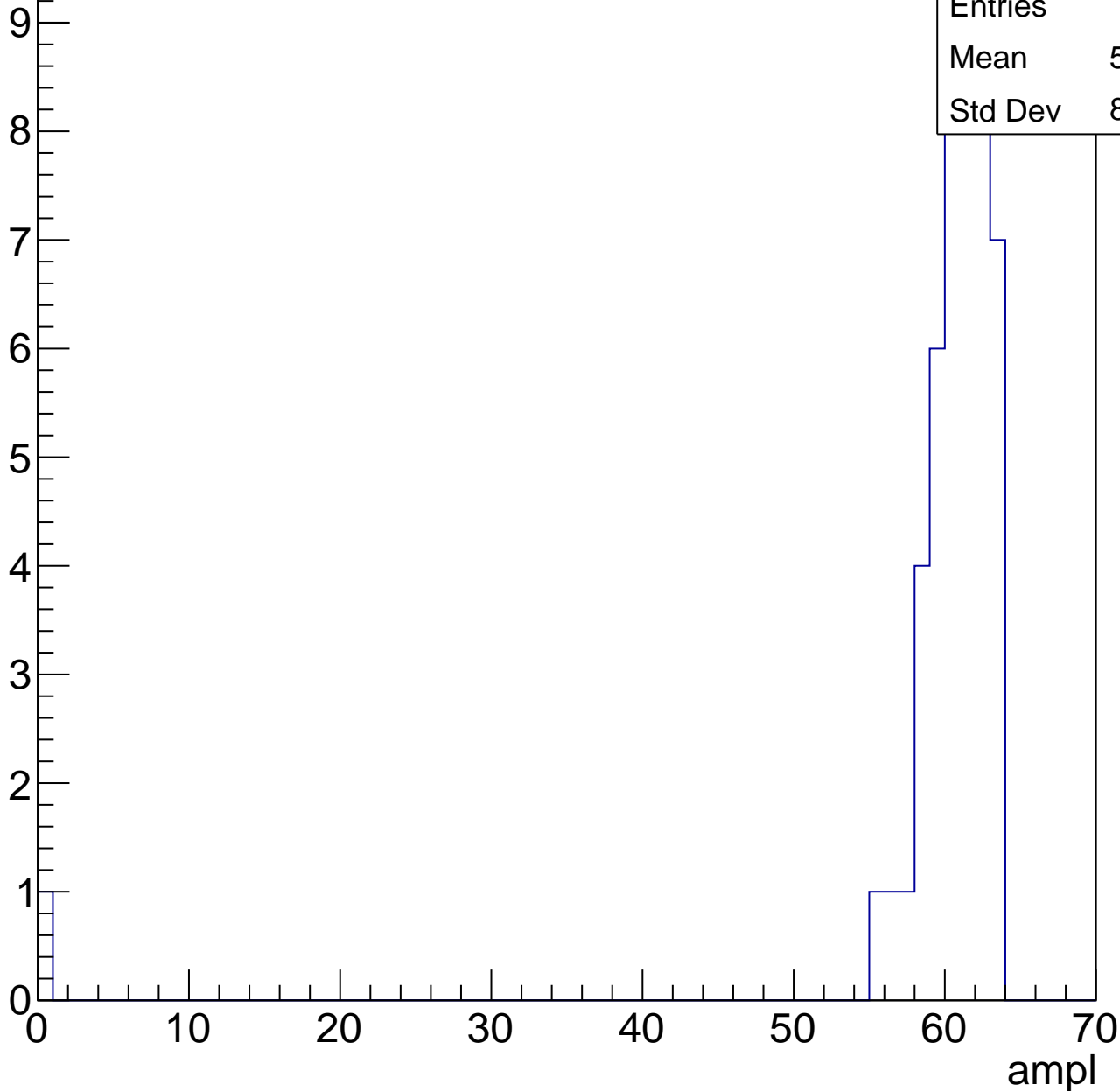


# B1L003S, U6-ch80, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	47
Mean	59.17
Std Dev	8.928



# B1L003S, U6-ch80, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch80, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	11
Std Dev	11

# B1L003S, U6-ch81, adc0

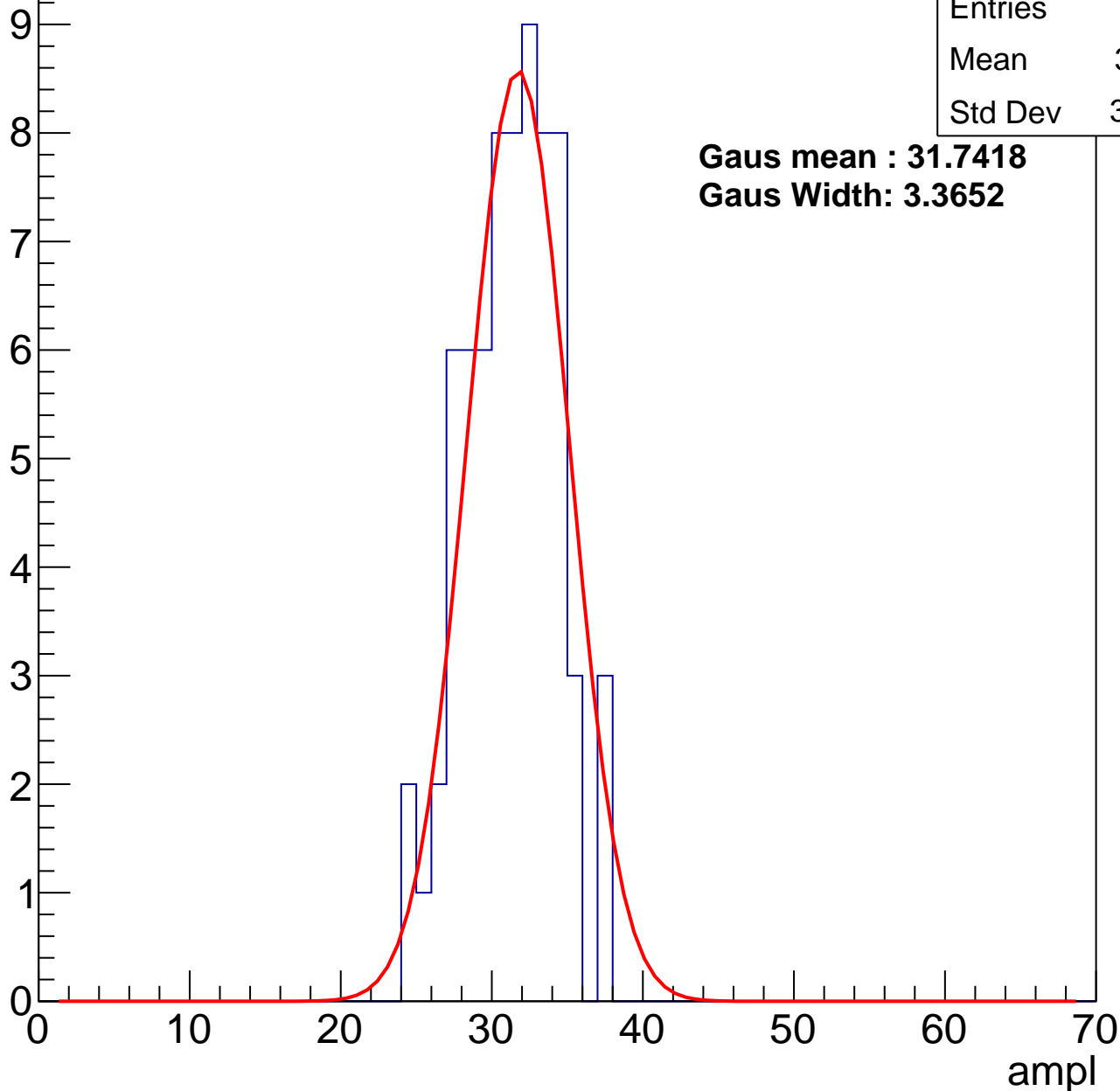
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	30.81
Std Dev	3.006

**Gaus mean : 31.7418**

**Gaus Width: 3.3652**



# B1L003S, U6-ch81, adc1

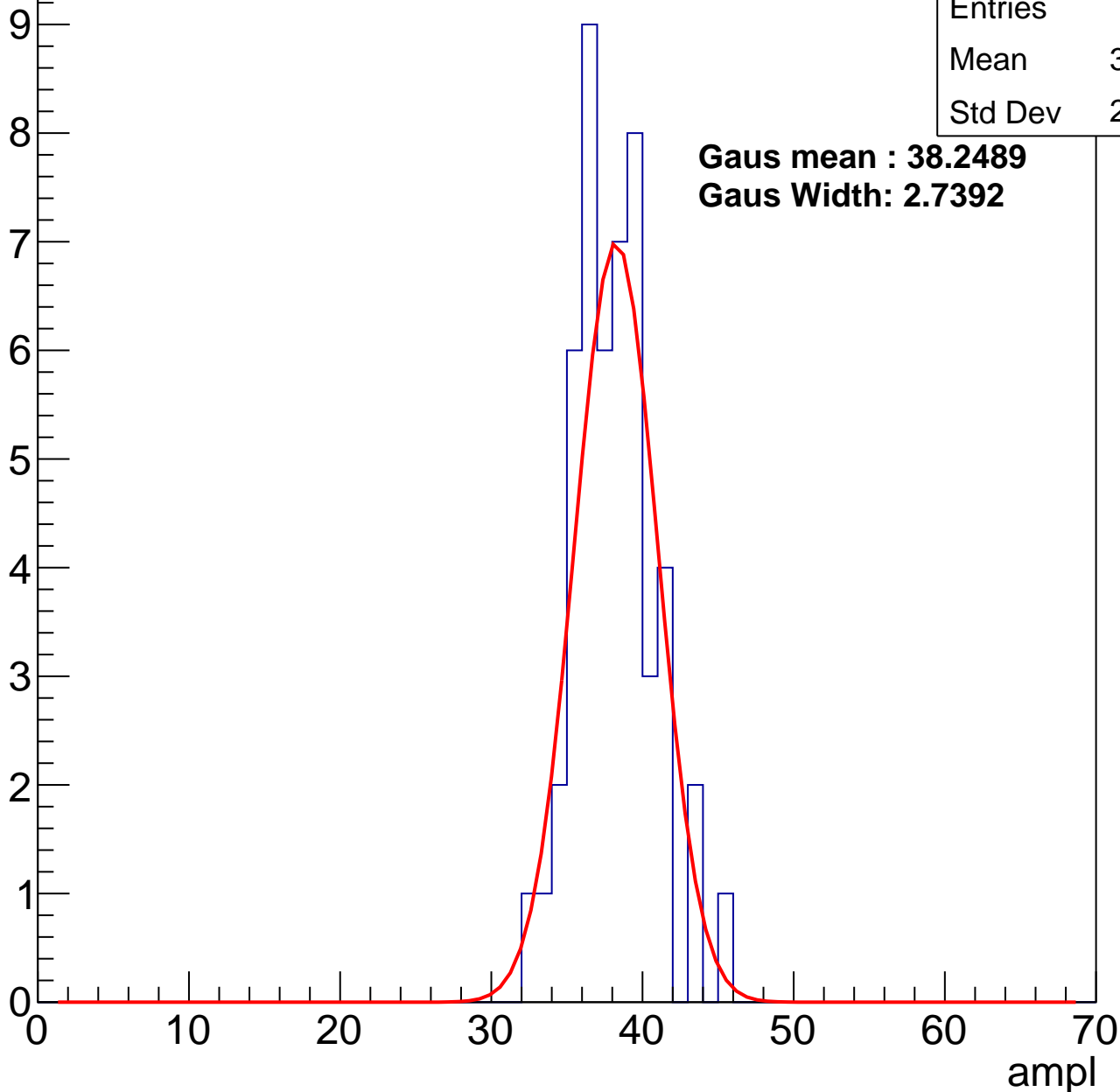
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	50
Mean	37.64
Std Dev	2.598

**Gaus mean : 38.2489**

**Gaus Width: 2.7392**



# B1L003S, U6-ch81, adc2

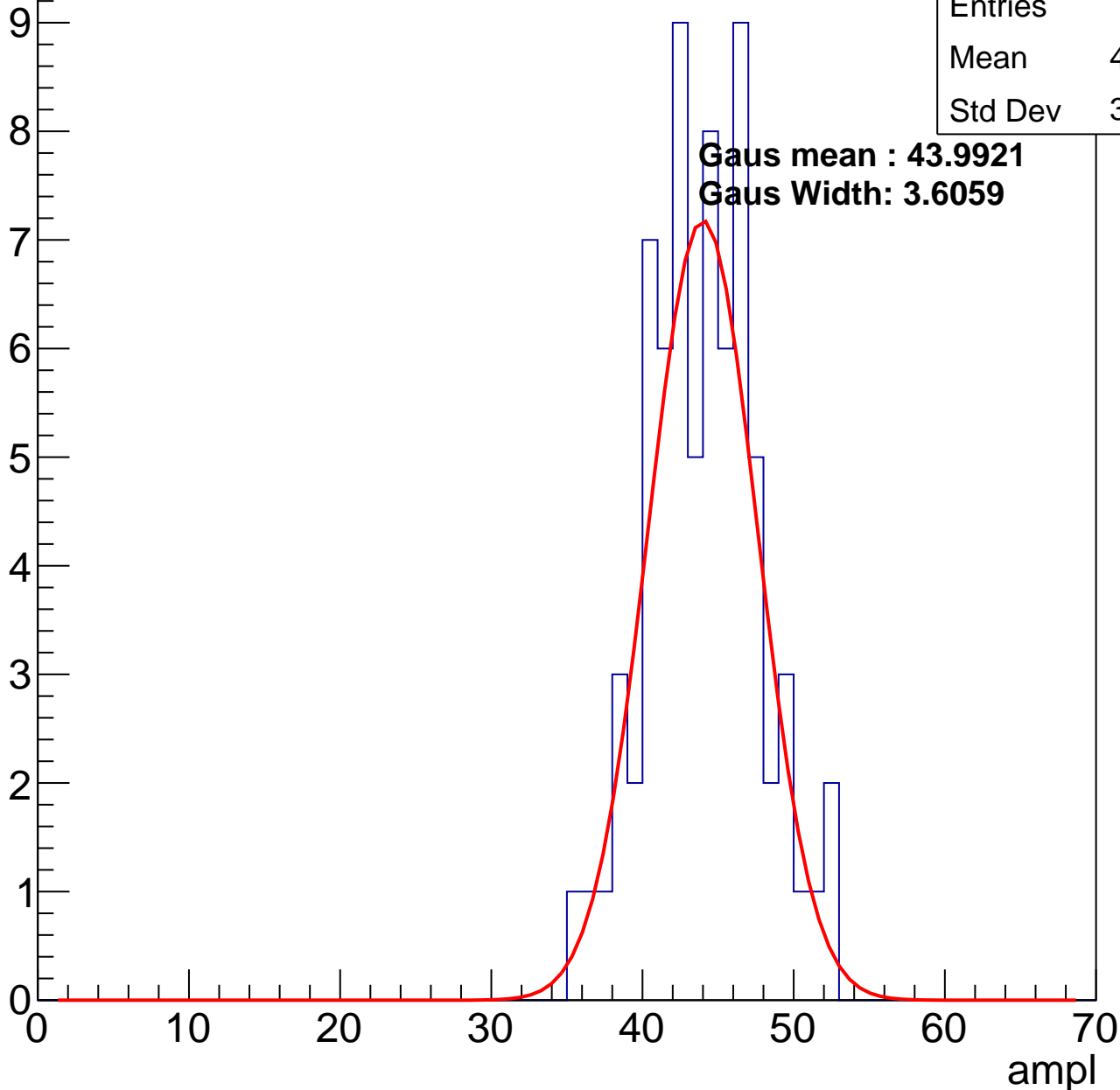
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	72
Mean	43.58
Std Dev	3.639

**Gaus mean : 43.9921**

**Gaus Width: 3.6059**

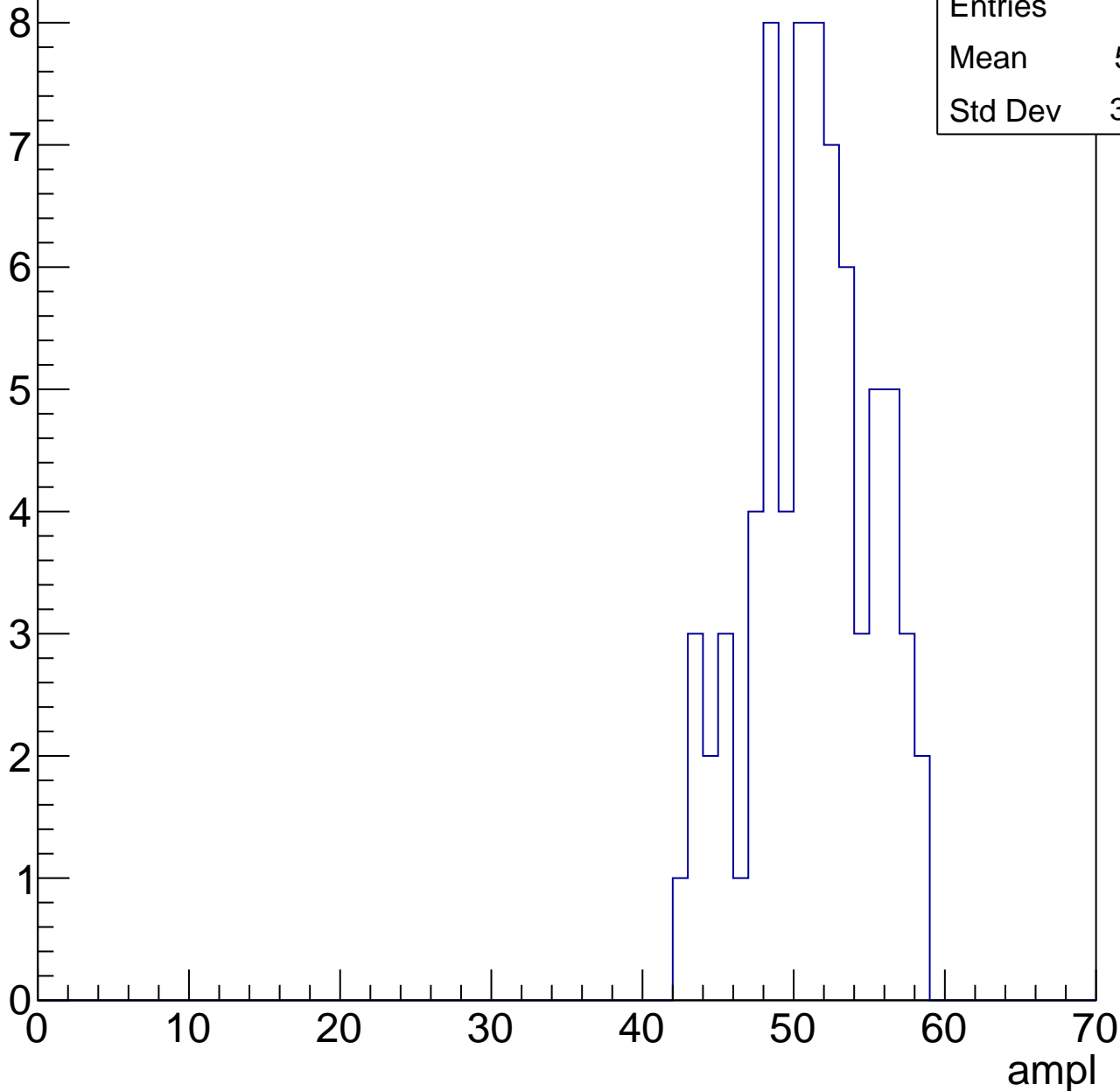


# B1L003S, U6-ch81, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	73
Mean	50.71
Std Dev	3.929

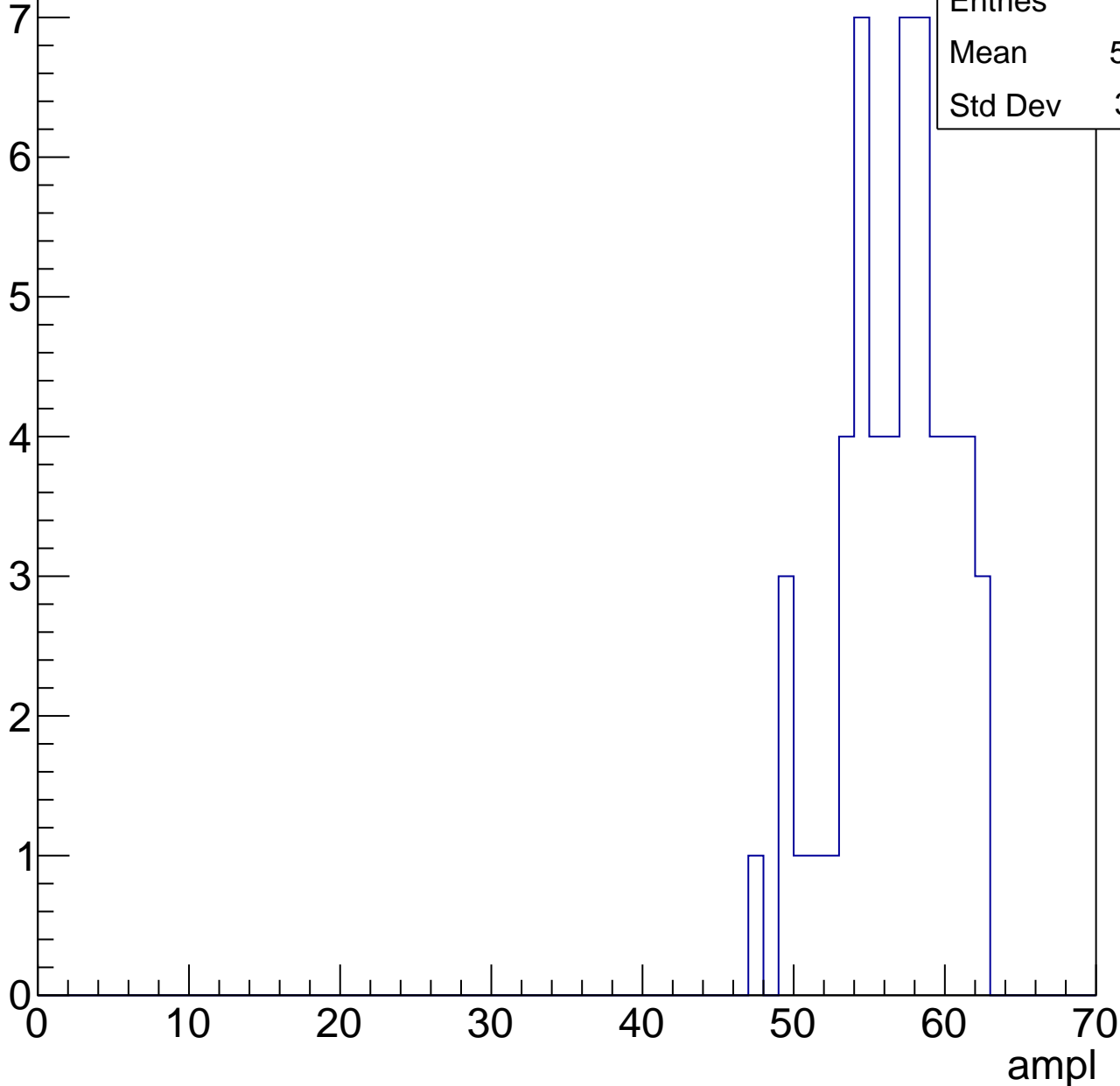


# B1L003S, U6-ch81, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	56.22
Std Dev	3.601

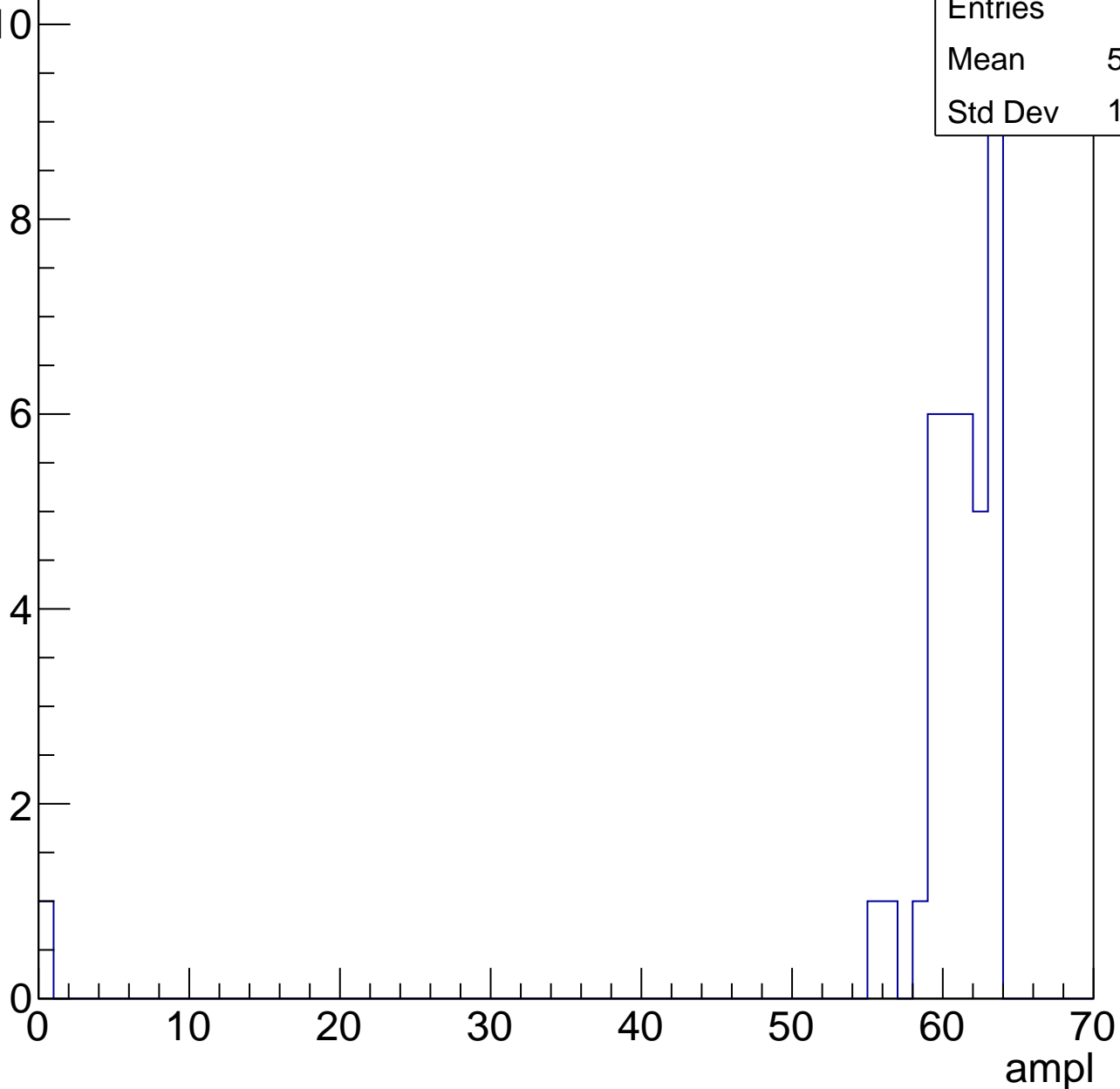


# B1L003S, U6-ch81, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	37
Mean	59.16
Std Dev	10.06



# B1L003S, U6-ch81, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch81, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L003S, U6-ch82, adc0

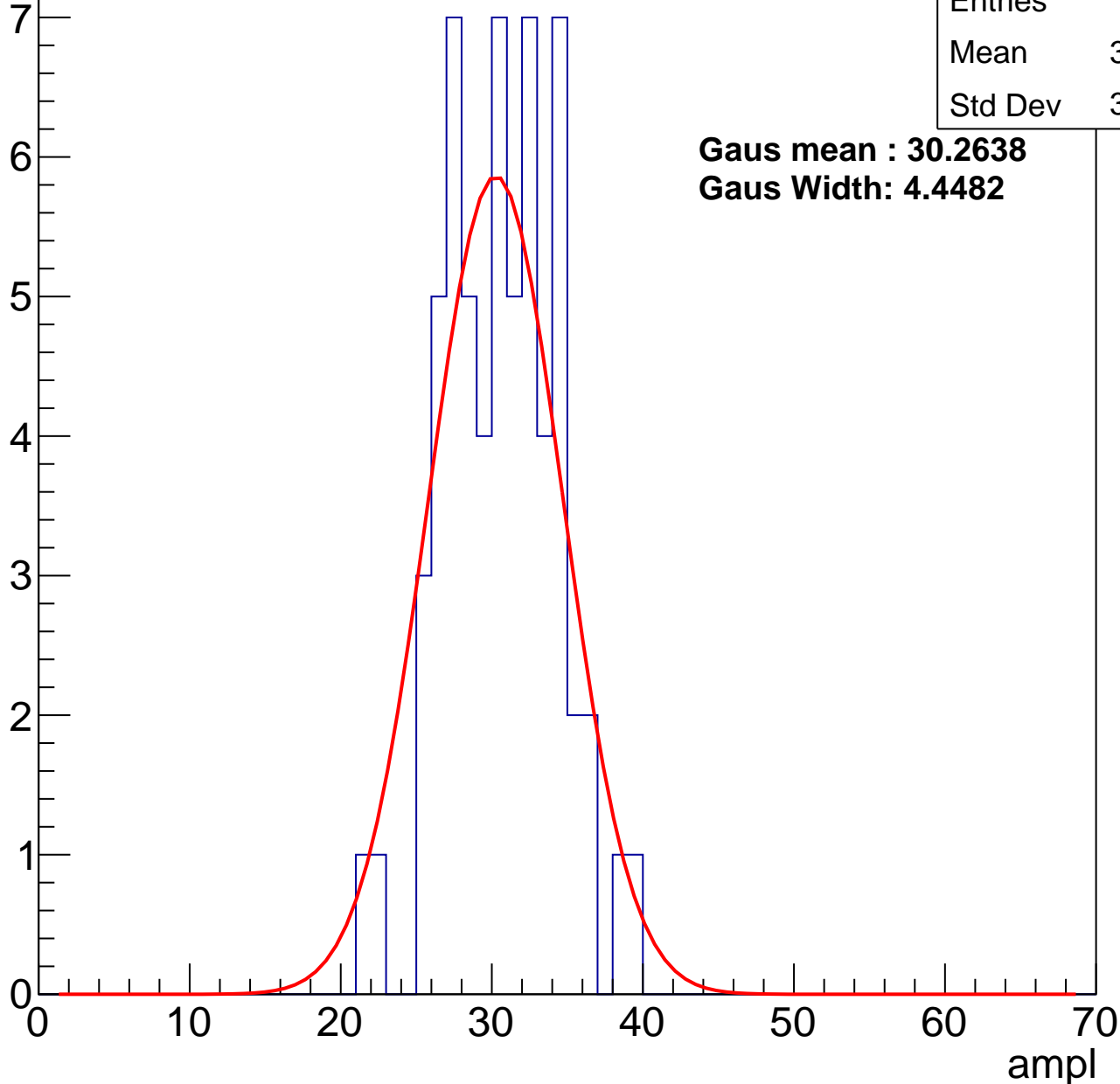
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	30.18
Std Dev	3.666

**Gaus mean : 30.2638**

**Gaus Width: 4.4482**



# B1L003S, U6-ch82, adc1

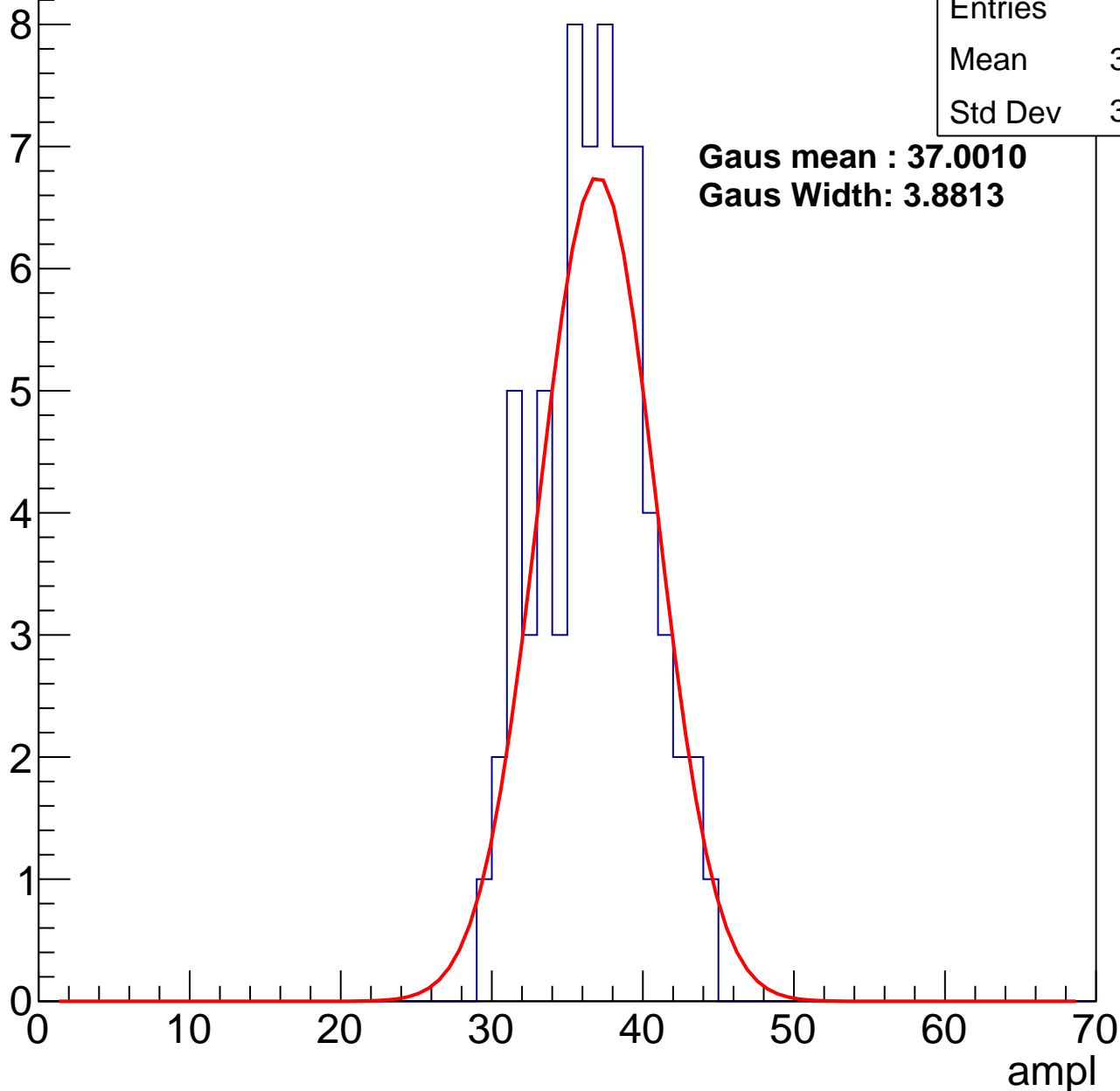
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	36.34
Std Dev	3.479

**Gaus mean : 37.0010**

**Gaus Width: 3.8813**



# B1L003S, U6-ch82, adc2

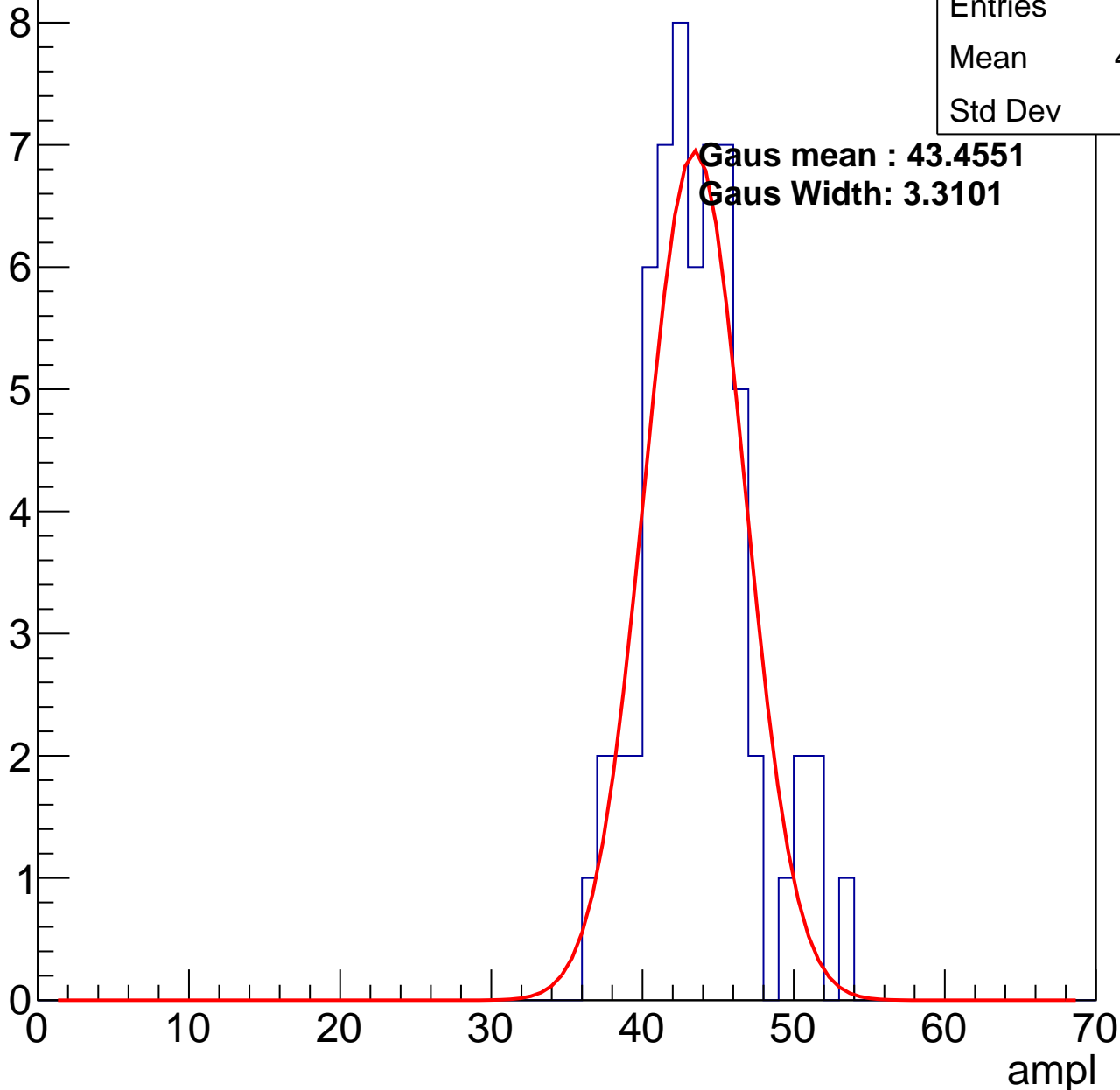
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	43.21
Std Dev	3.54

**Gaus mean : 43.4551**

**Gaus Width: 3.3101**

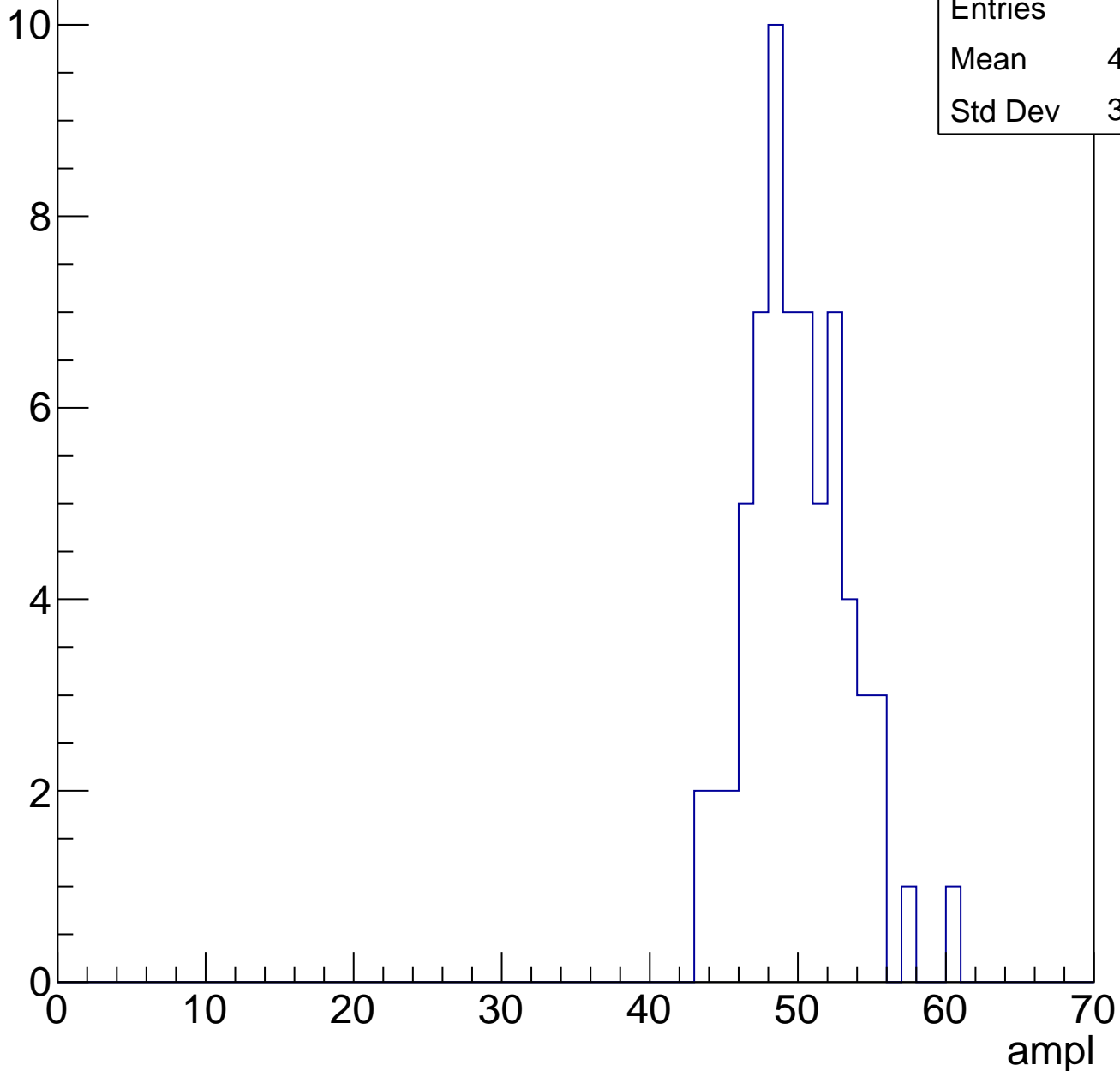


# B1L003S, U6-ch82, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	66
Mean	49.56
Std Dev	3.345

Entry

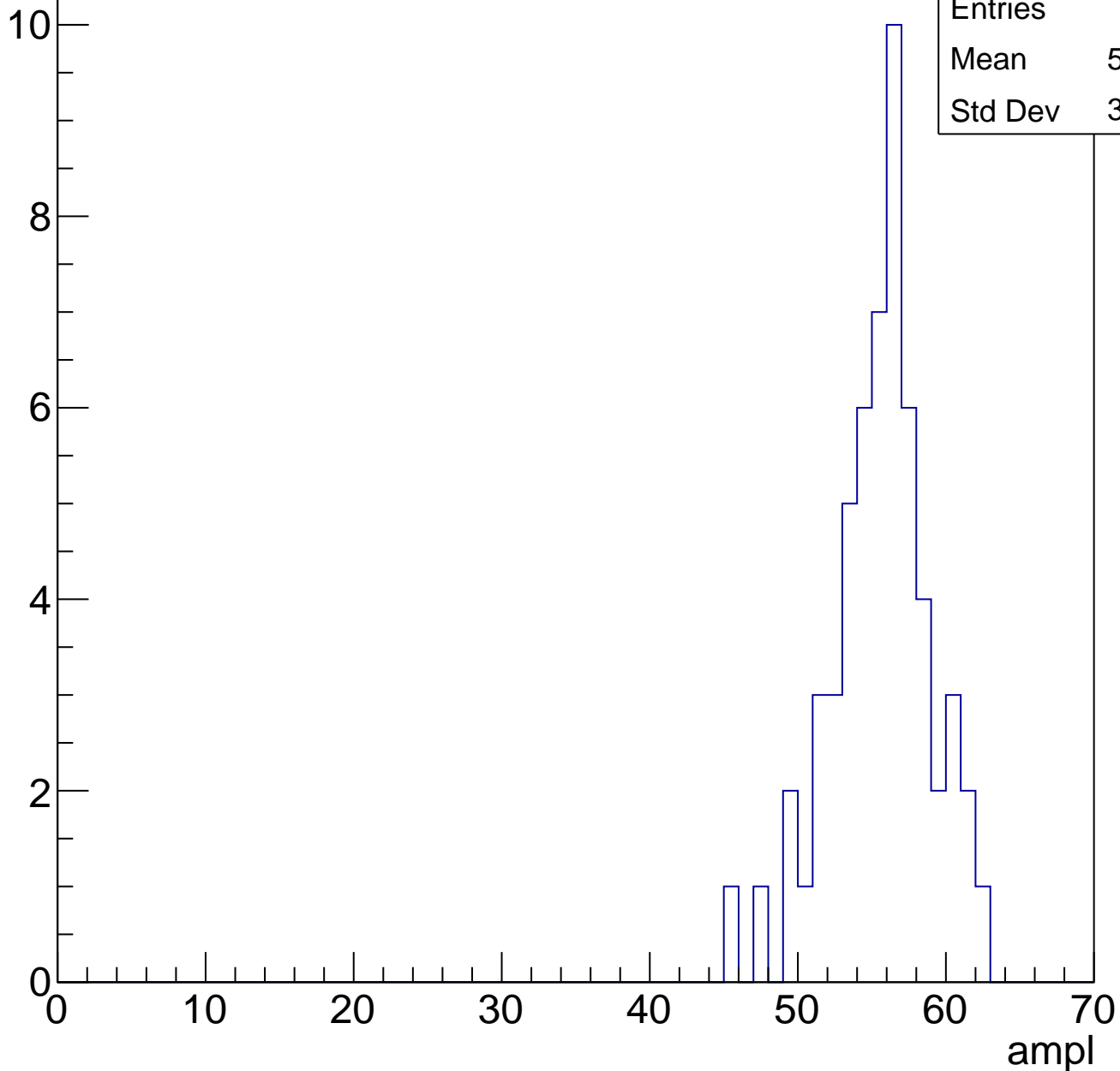


# B1L003S, U6-ch82, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	57
Mean	55.07
Std Dev	3.402

Entry

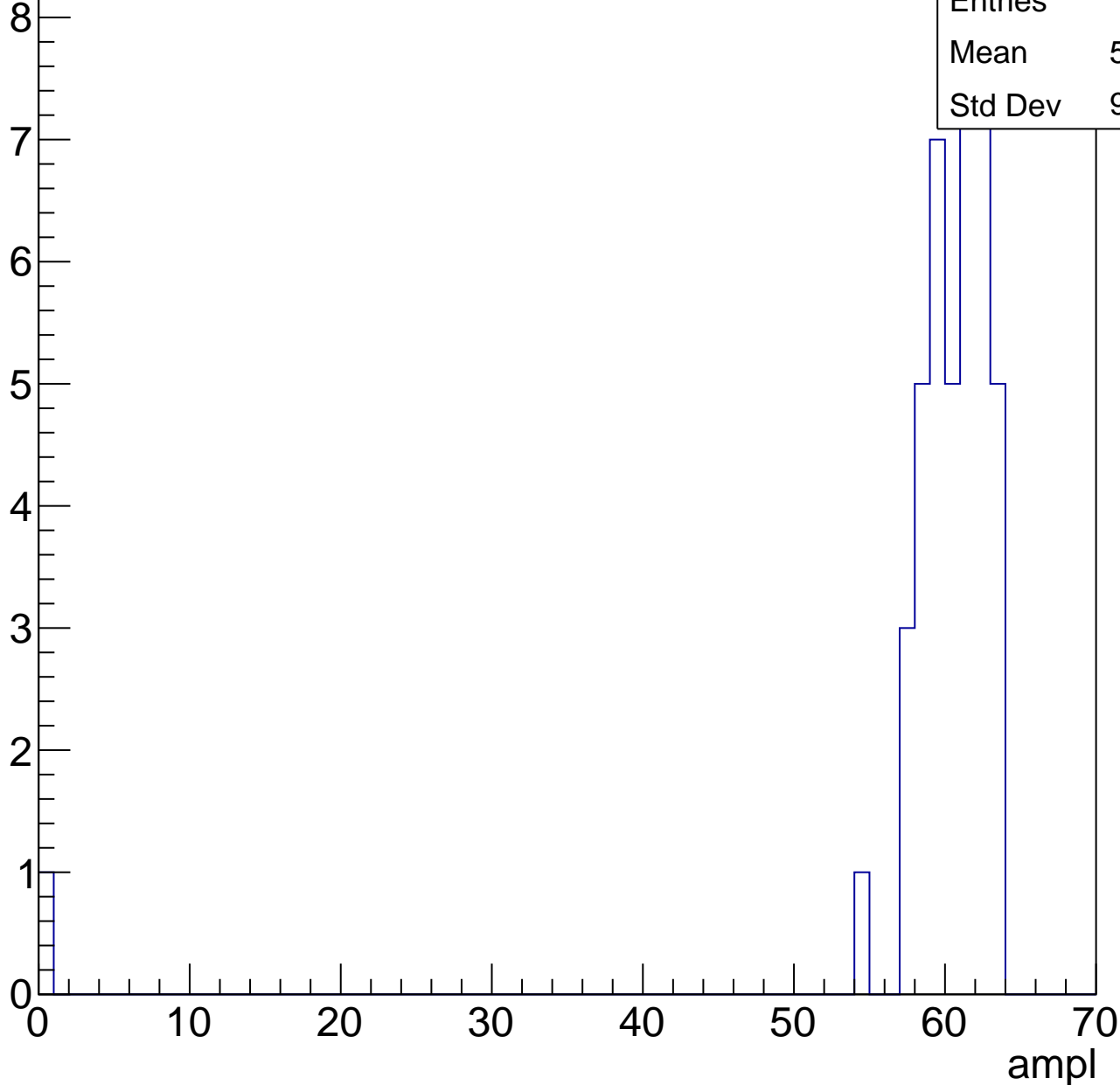


# B1L003S, U6-ch82, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	43
Mean	58.77
Std Dev	9.288

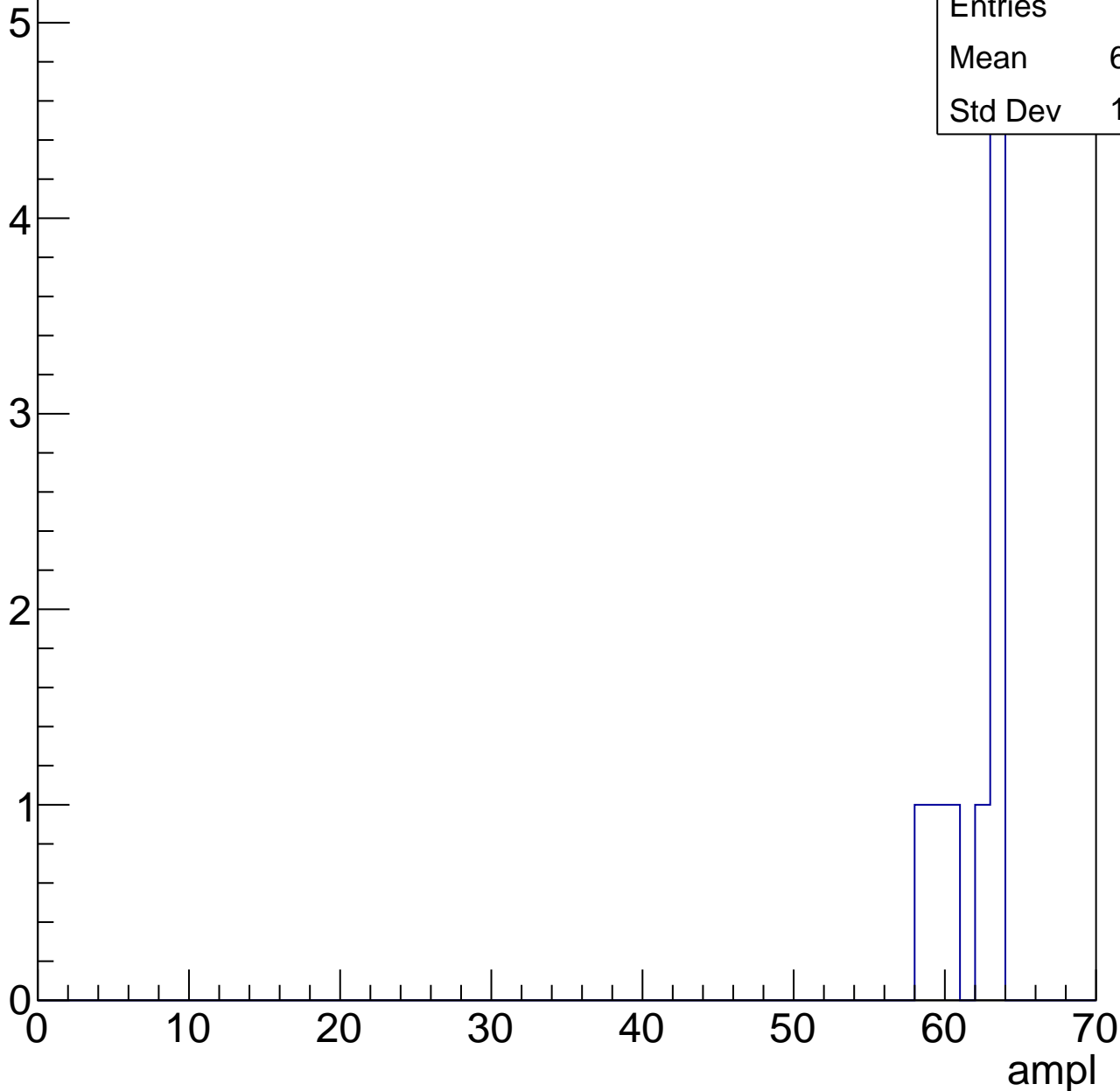


# B1L003S, U6-ch82, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	9
Mean	61.56
Std Dev	1.892





# B1L003S, U6-ch82, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U6-ch83, adc0

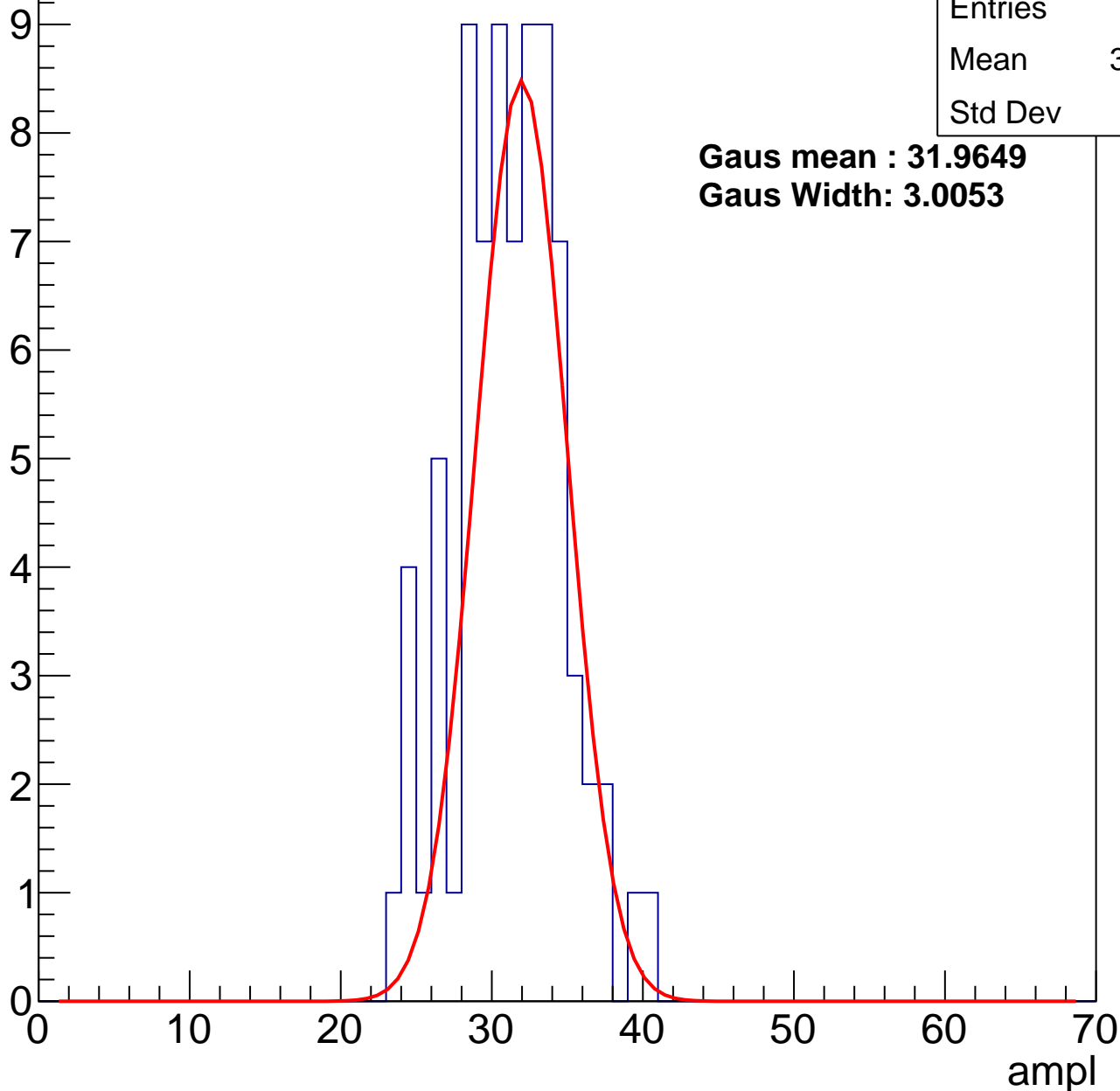
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	78
Mean	30.72
Std Dev	3.53

**Gaus mean : 31.9649**

**Gaus Width: 3.0053**



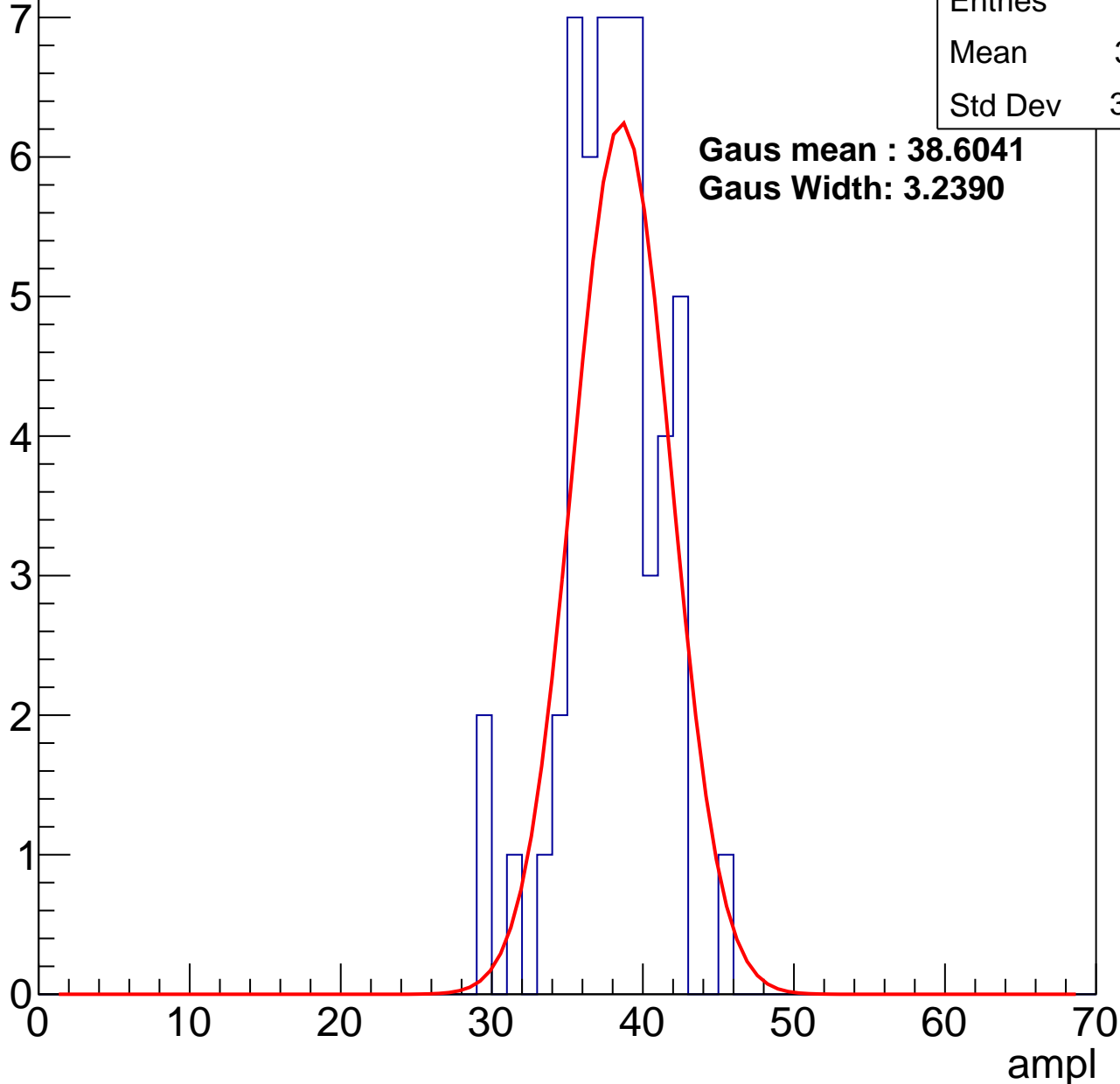
# B1L003S, U6-ch83, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	37.51
Std Dev	3.172

**Gaus mean : 38.6041**  
**Gaus Width: 3.2390**



# B1L003S, U6-ch83, adc2

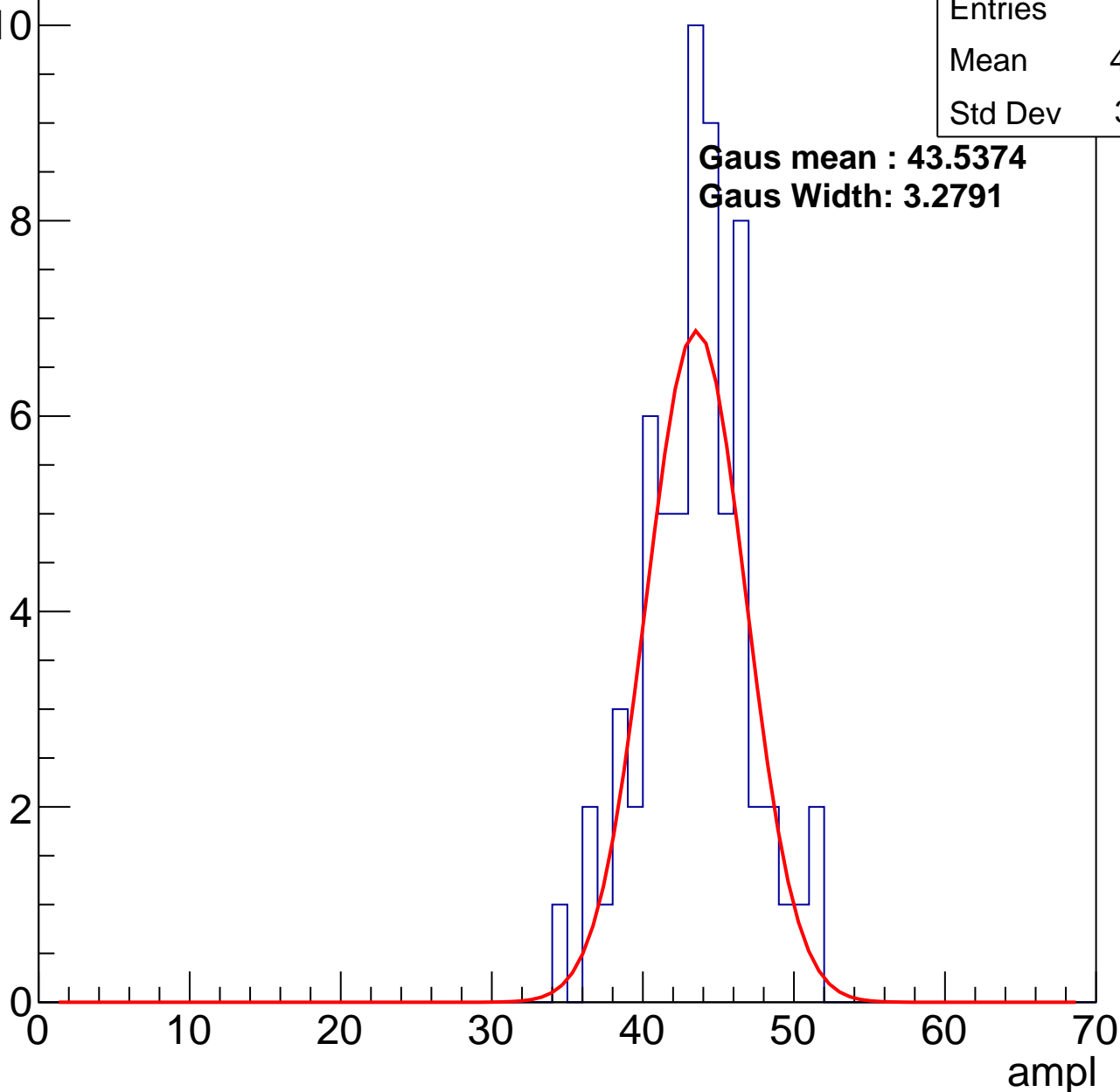
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	43.08
Std Dev	3.501

**Gaus mean : 43.5374**

**Gaus Width: 3.2791**

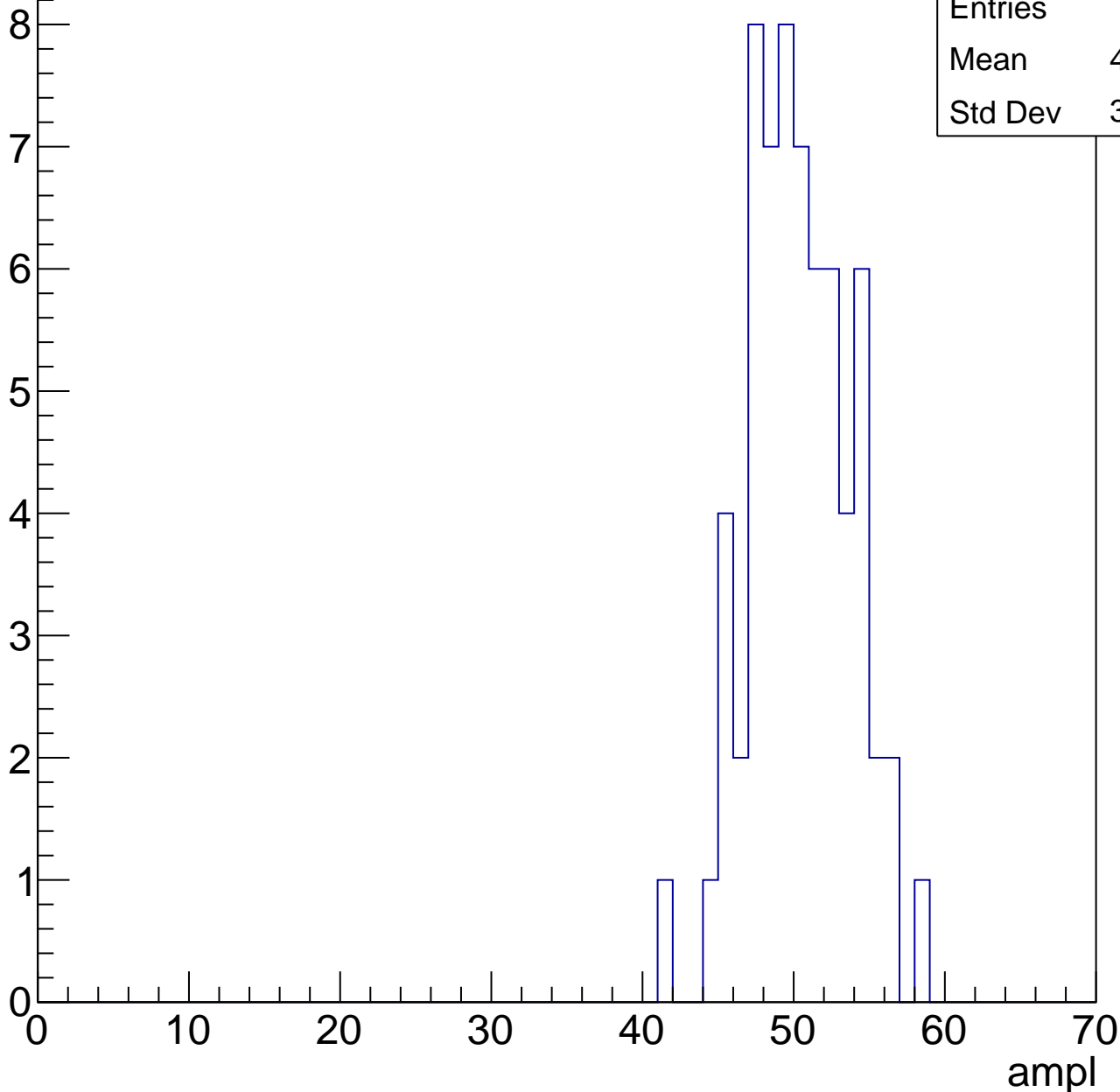


# B1L003S, U6-ch83, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	49.92
Std Dev	3.292

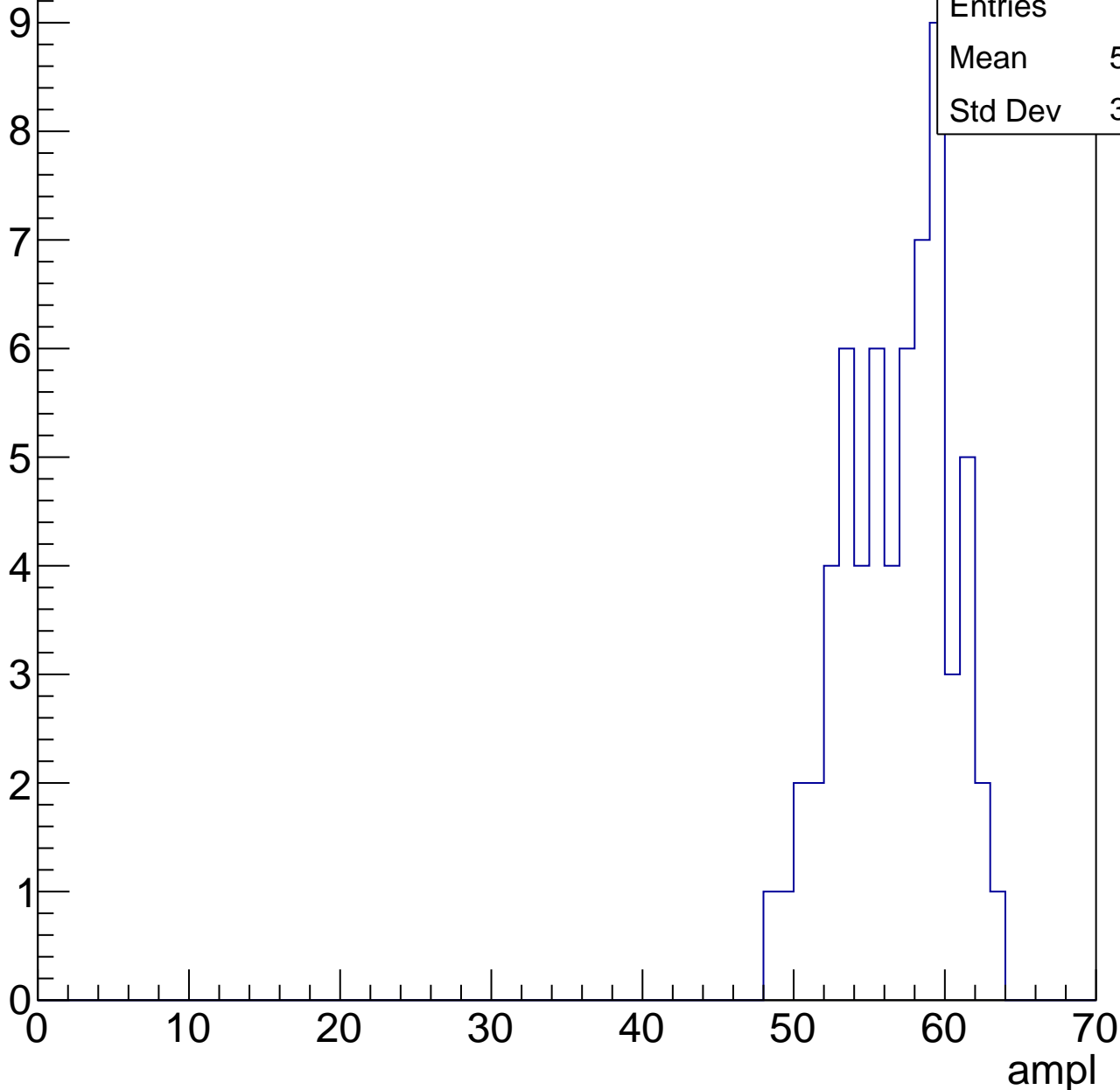


# B1L003S, U6-ch83, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

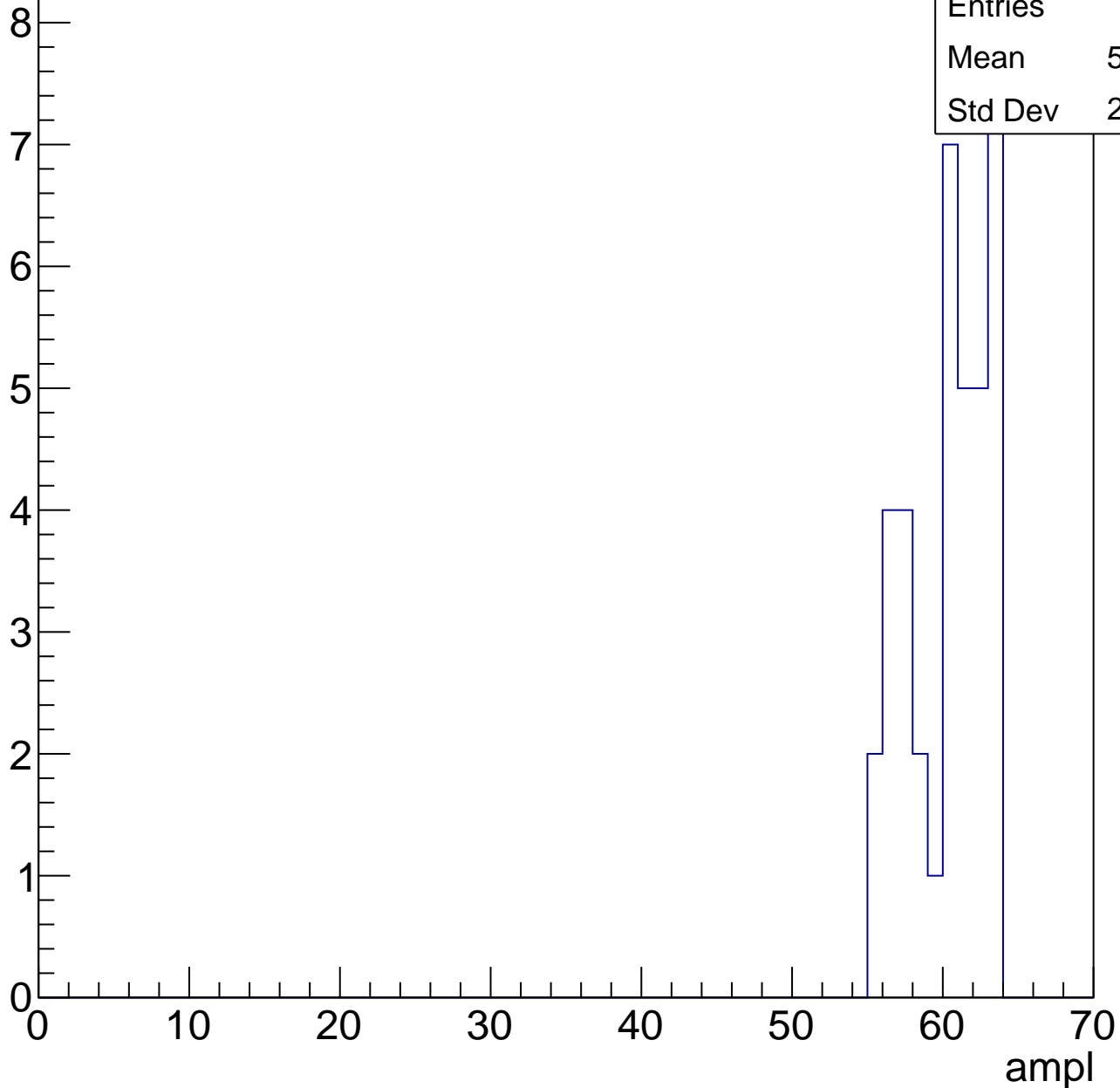
Entries	63
Mean	56.29
Std Dev	3.516



# B1L003S, U6-ch83, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

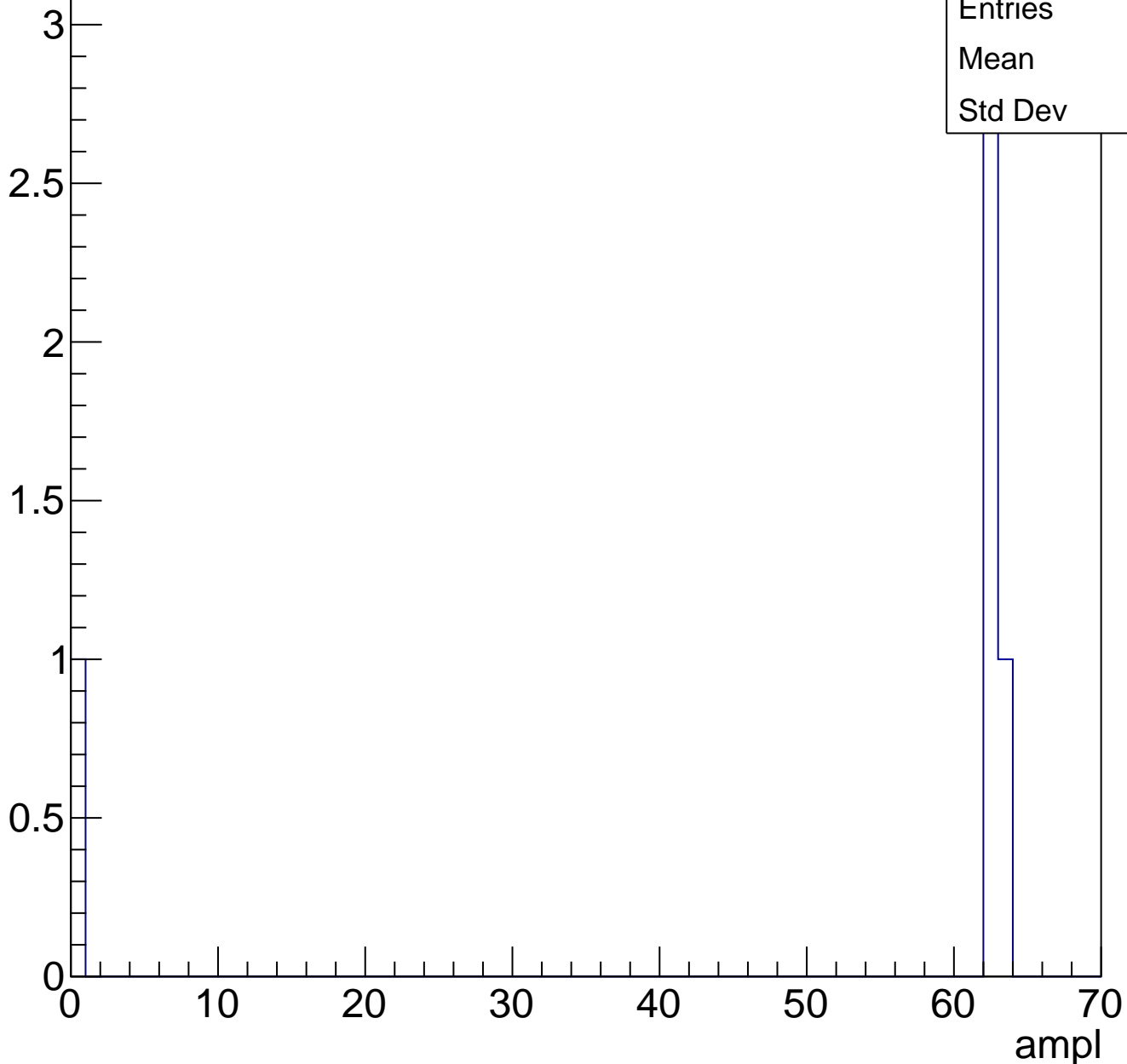
Entry



# B1L003S, U6-ch83, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

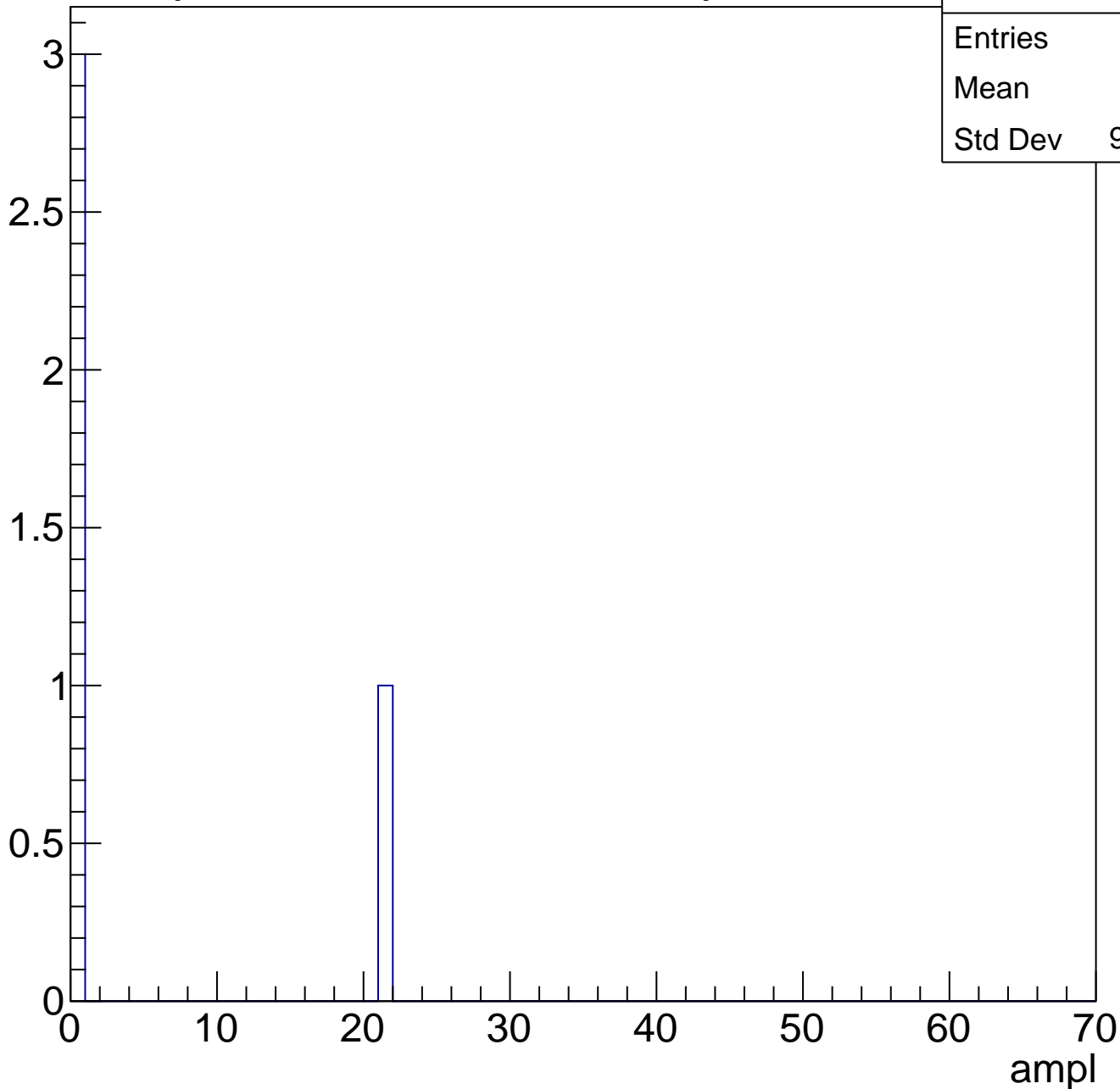




# B1L003S, U6-ch83, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch84, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	74
Mean	29.65
Std Dev	4.867

**Gaus mean : 30.7245**

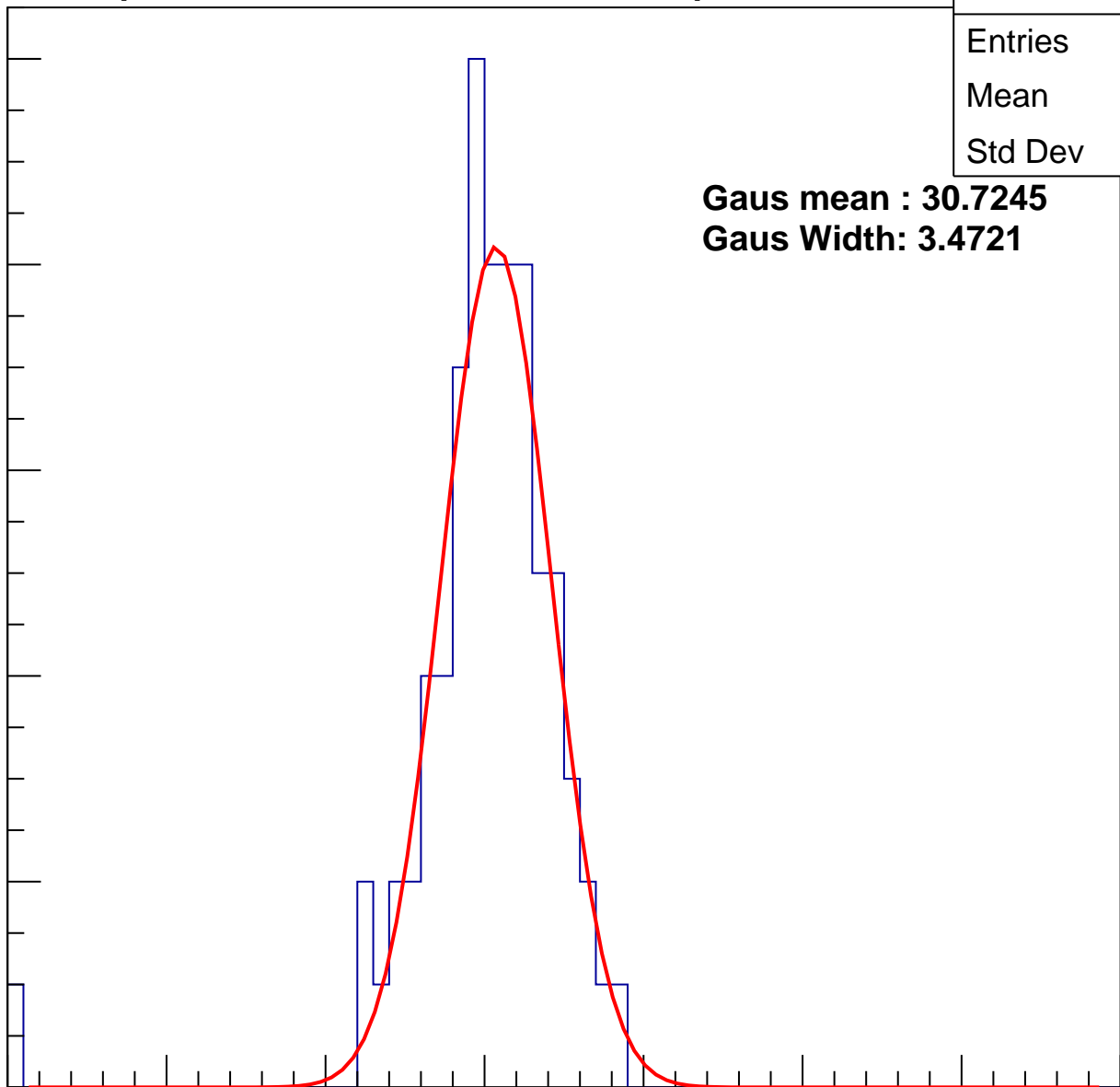
**Gaus Width: 3.4721**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U6-ch84, adc1

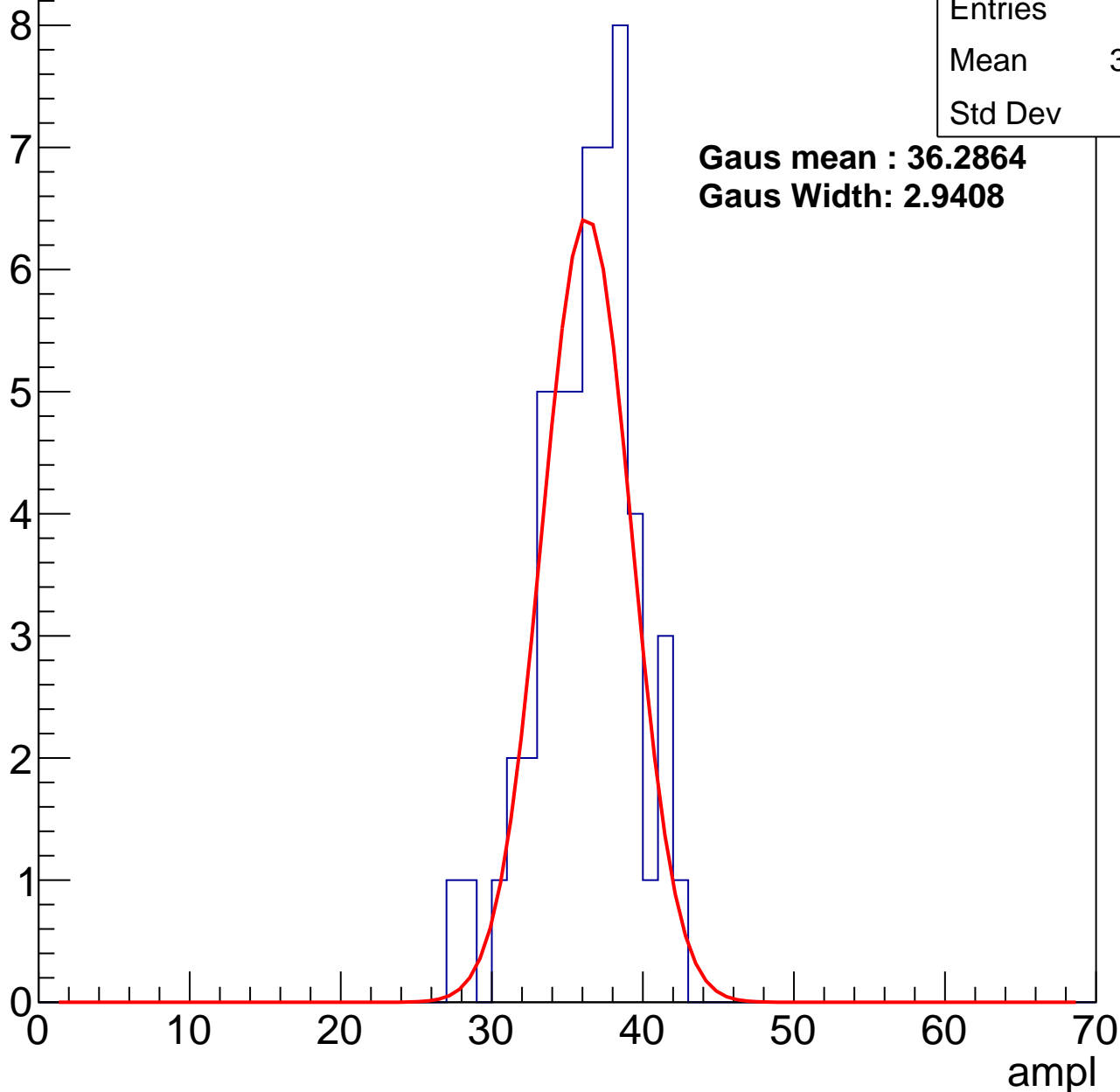
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	35.79
Std Dev	3.17

**Gaus mean : 36.2864**

**Gaus Width: 2.9408**



# B1L003S, U6-ch84, adc2

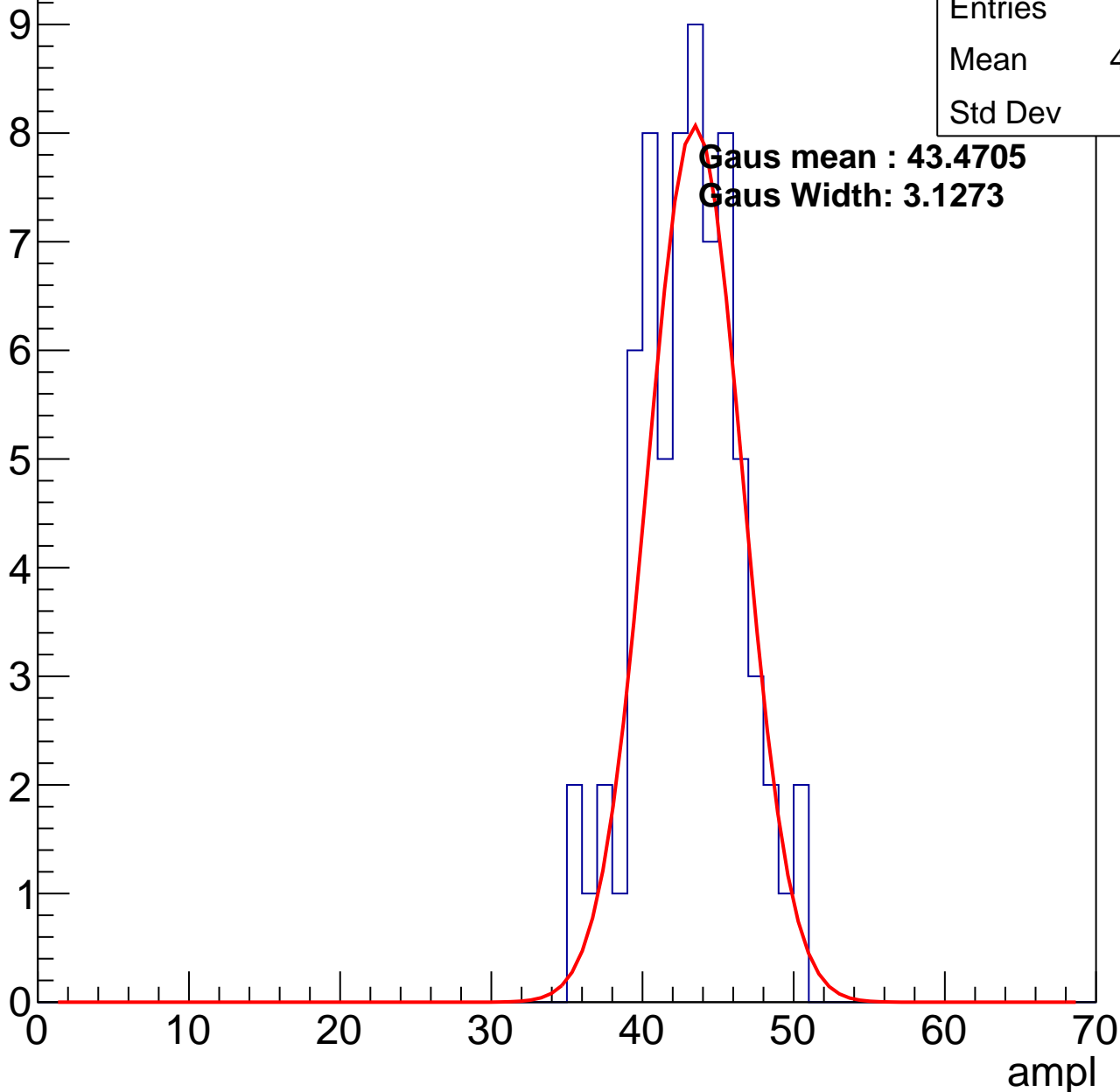
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	42.63
Std Dev	3.33

**Gaus mean : 43.4705**

**Gaus Width: 3.1273**

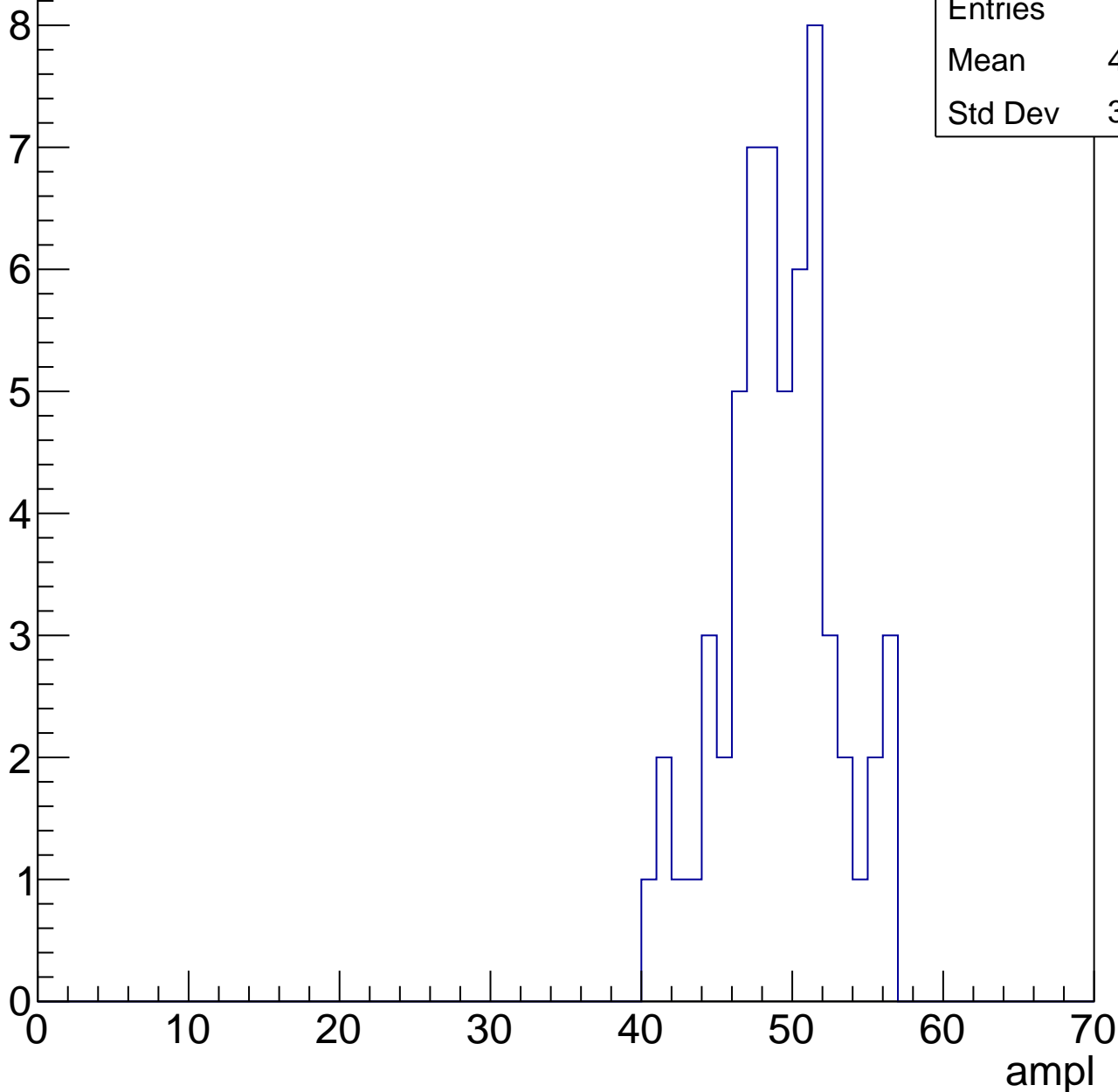


# B1L003S, U6-ch84, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	48.66
Std Dev	3.717

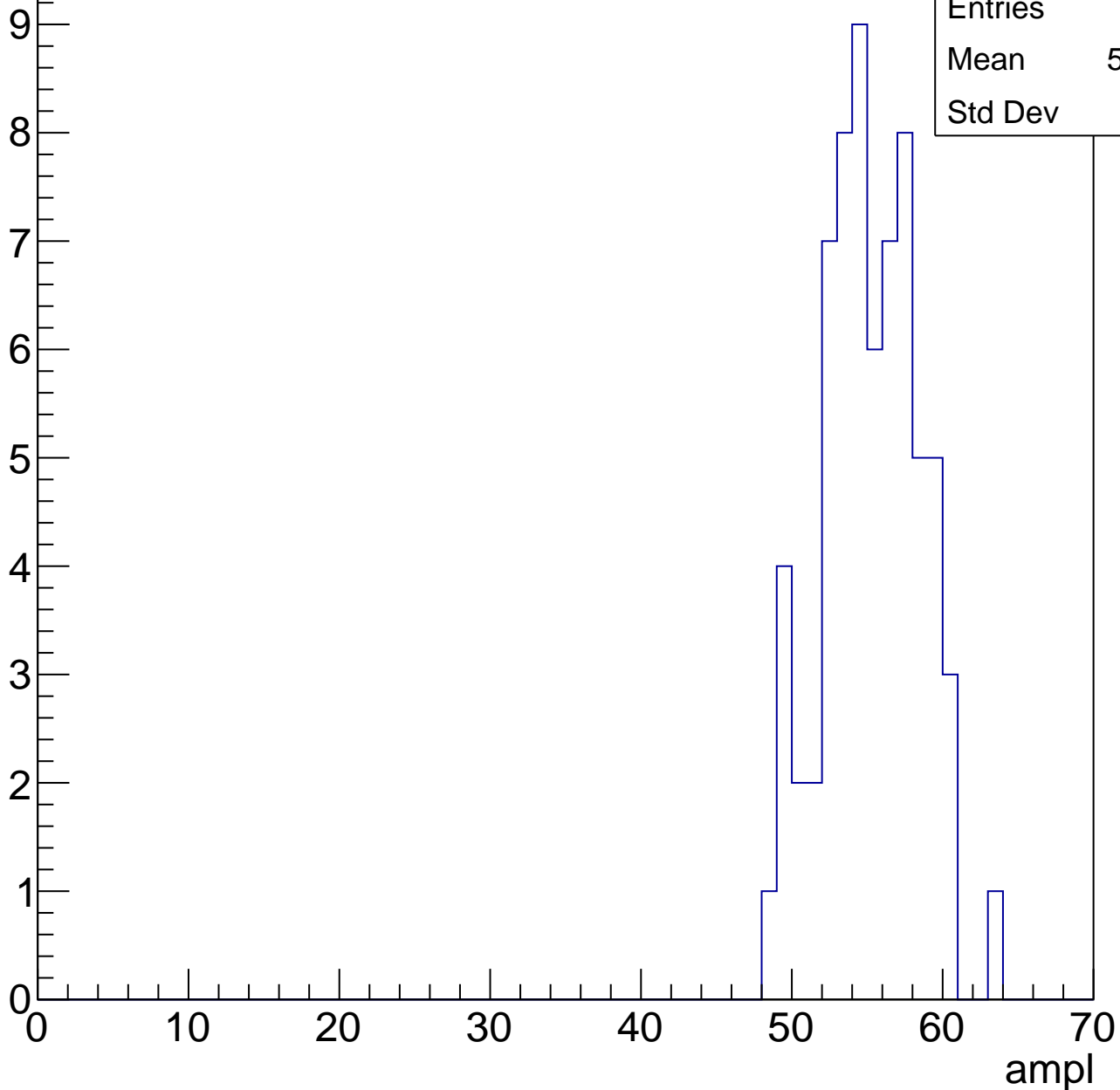


# B1L003S, U6-ch84, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	54.79
Std Dev	3.16

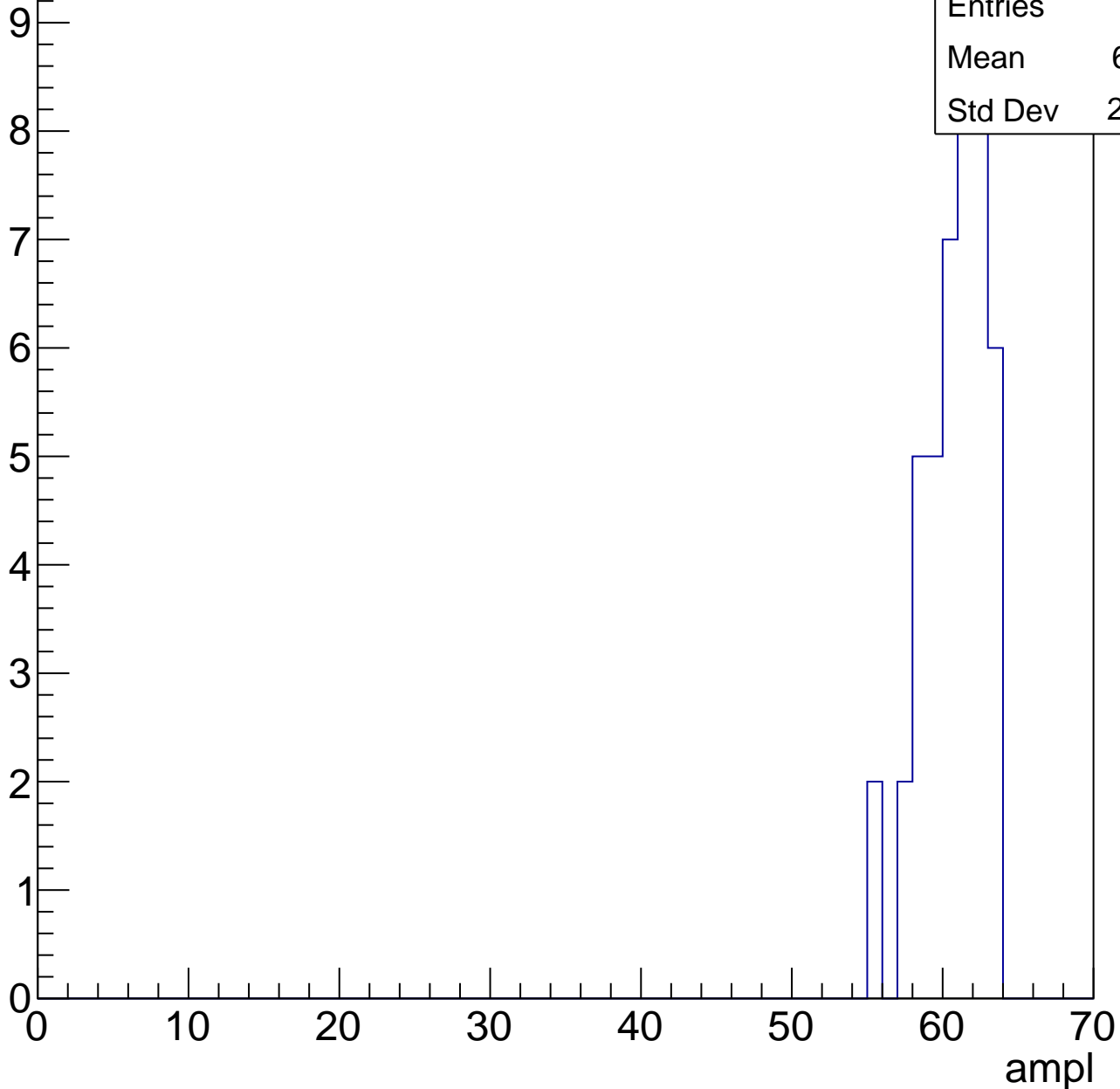


# B1L003S, U6-ch84, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	45
Mean	60.31
Std Dev	2.042



# B1L003S, U6-ch84, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

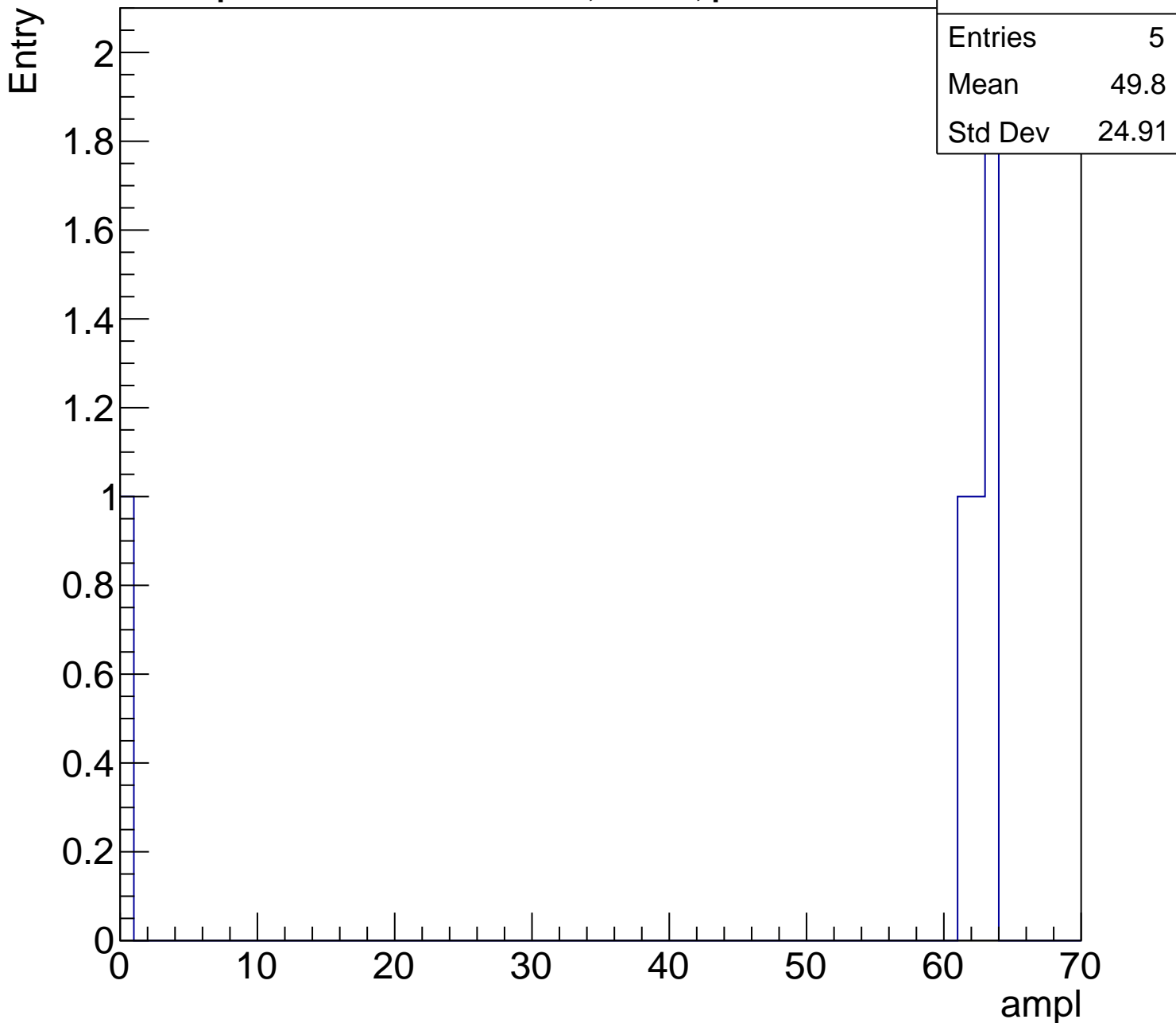
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	49.8
Std Dev	24.91

0 10 20 30 40 50 60 70

ampl





# B1L003S, U6-ch84, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch85, adc0

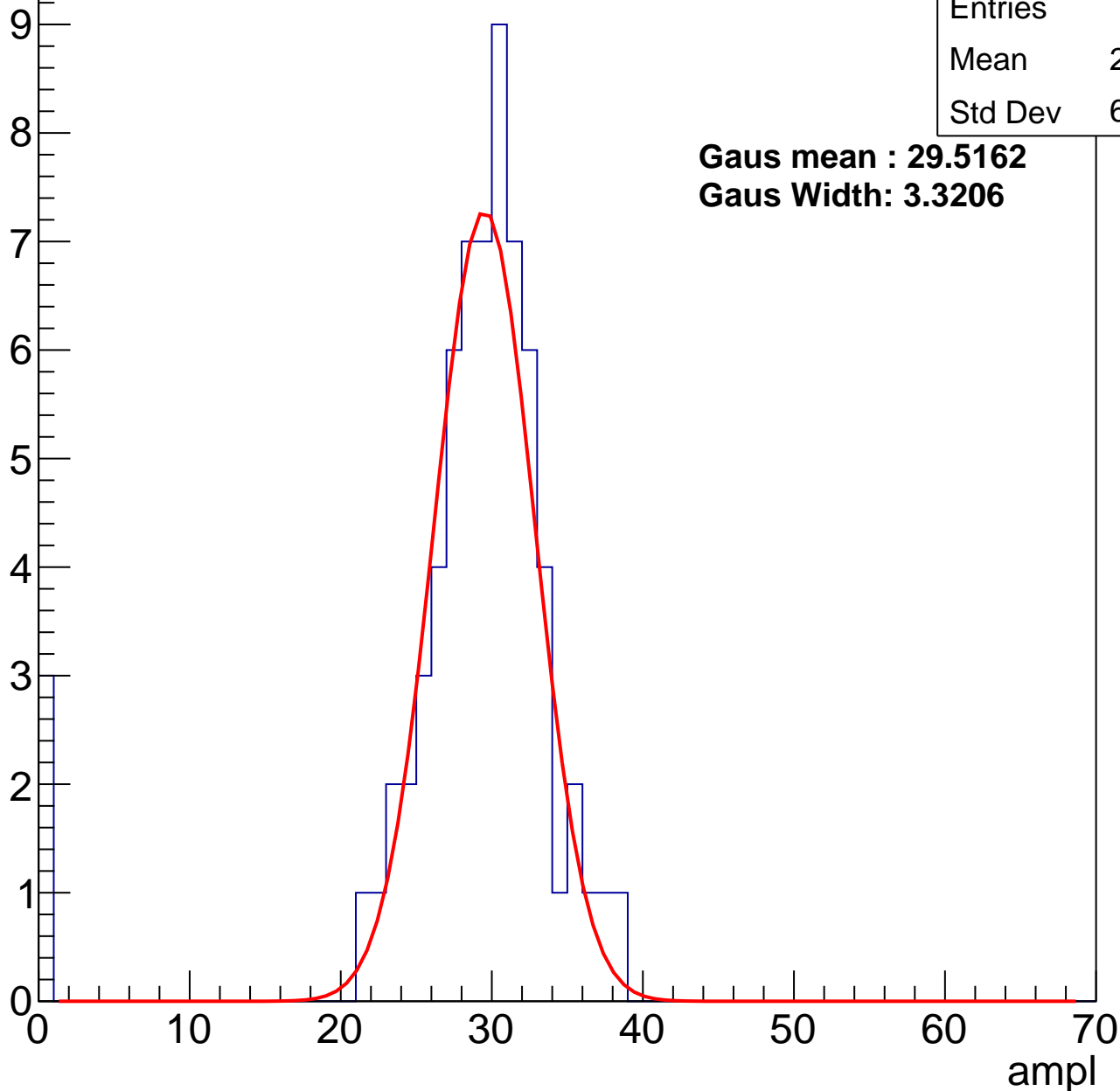
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	27.99
Std Dev	6.912

**Gaus mean : 29.5162**

**Gaus Width: 3.3206**



# B1L003S, U6-ch85, adc1

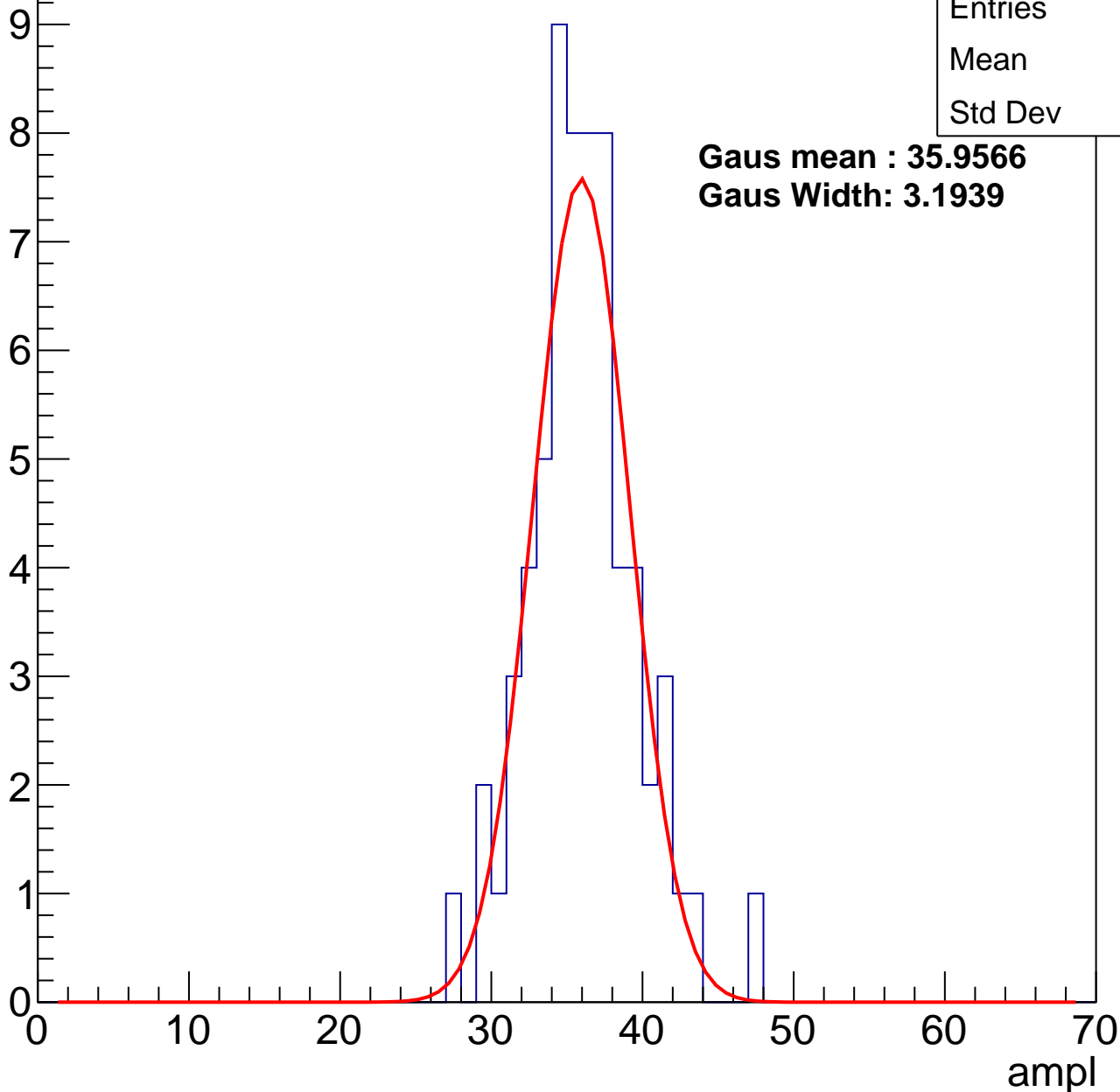
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	35.6
Std Dev	3.52

**Gaus mean : 35.9566**

**Gaus Width: 3.1939**



# B1L003S, U6-ch85, adc2

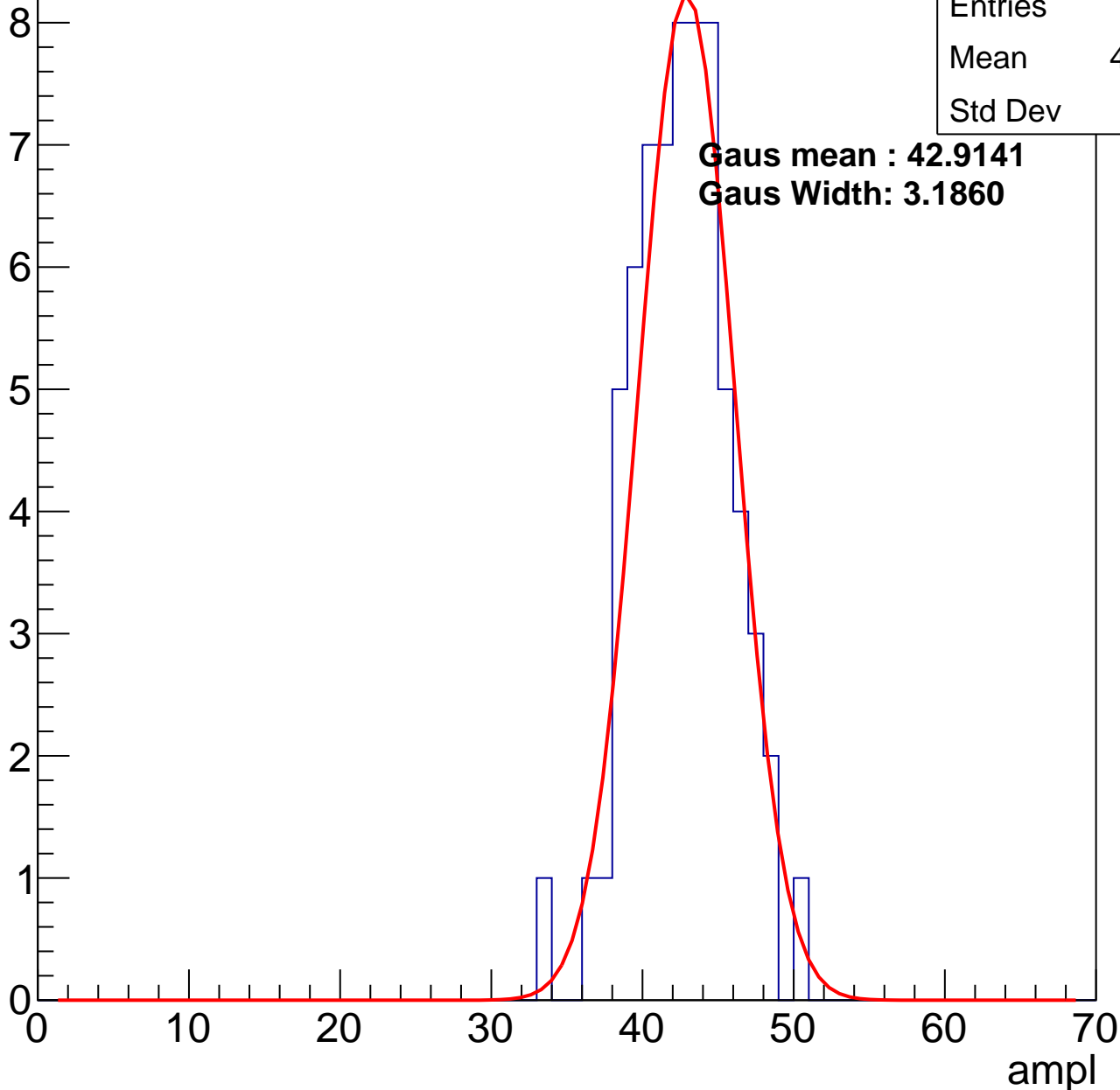
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	42.16
Std Dev	3.16

**Gaus mean : 42.9141**

**Gaus Width: 3.1860**



# B1L003S, U6-ch85, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	68
Mean	49
Std Dev	3.391

Entry

10

8

6

4

2

0

0

10

20

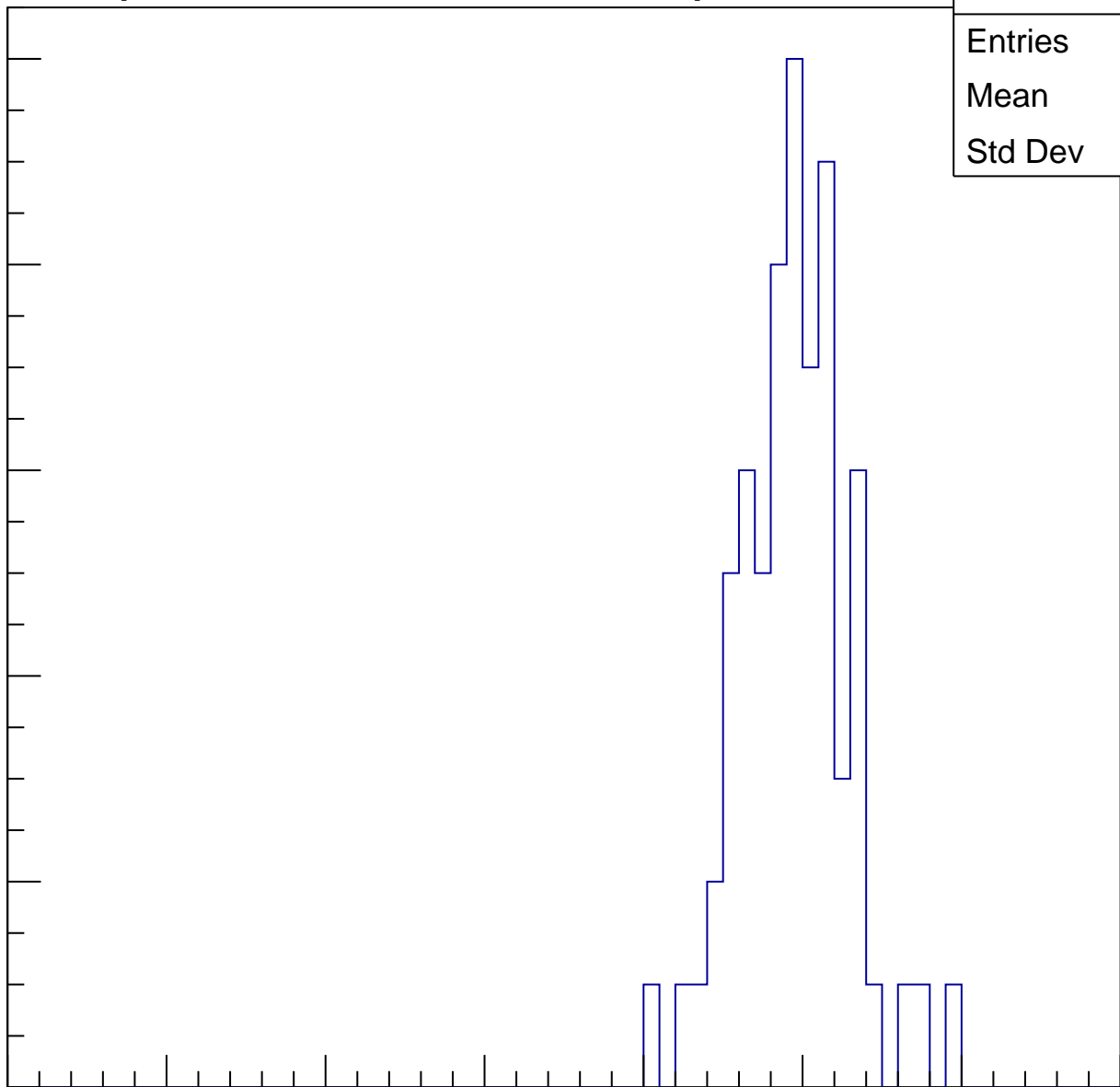
30

40

50

60

ampl

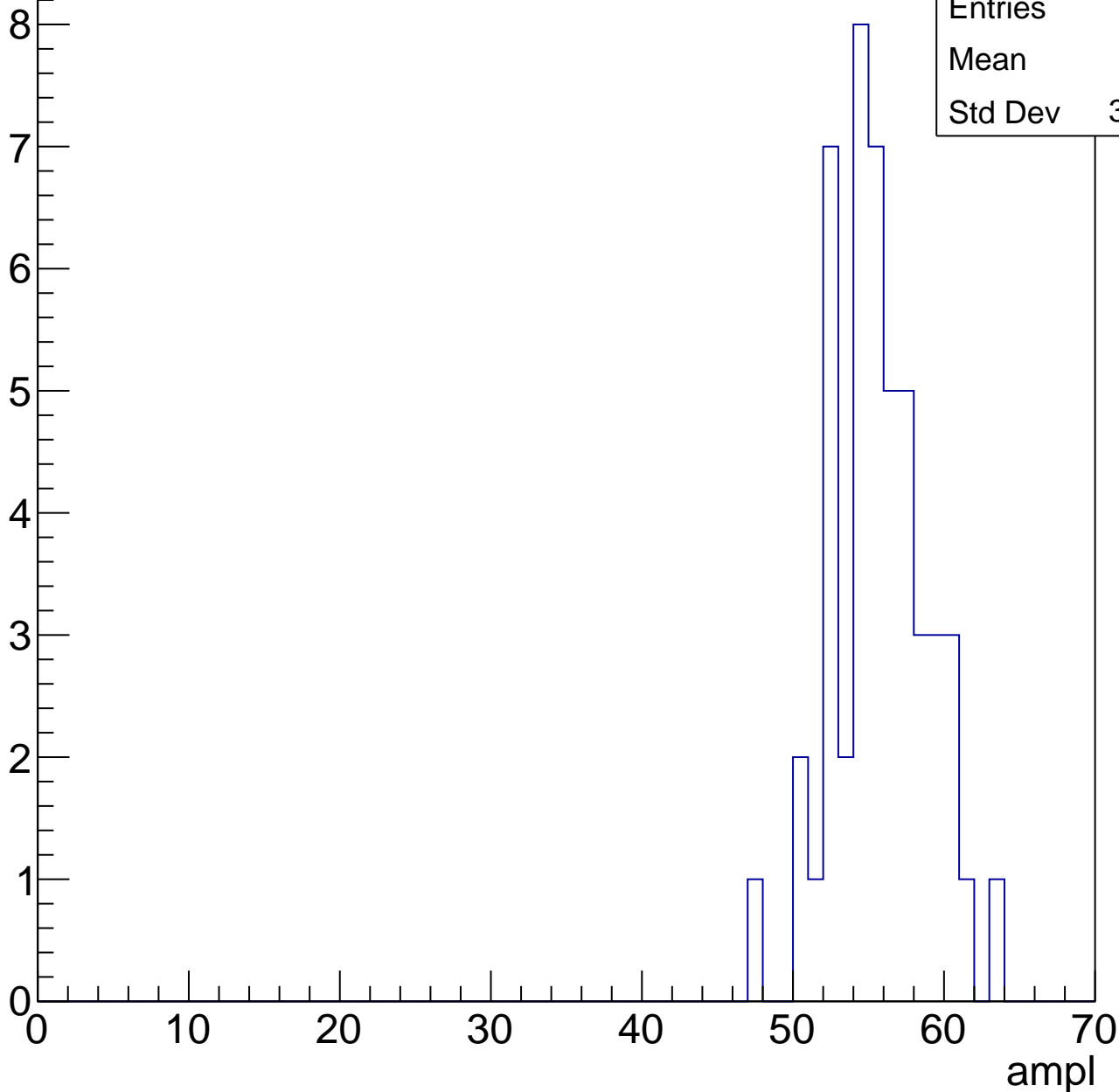


# B1L003S, U6-ch85, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

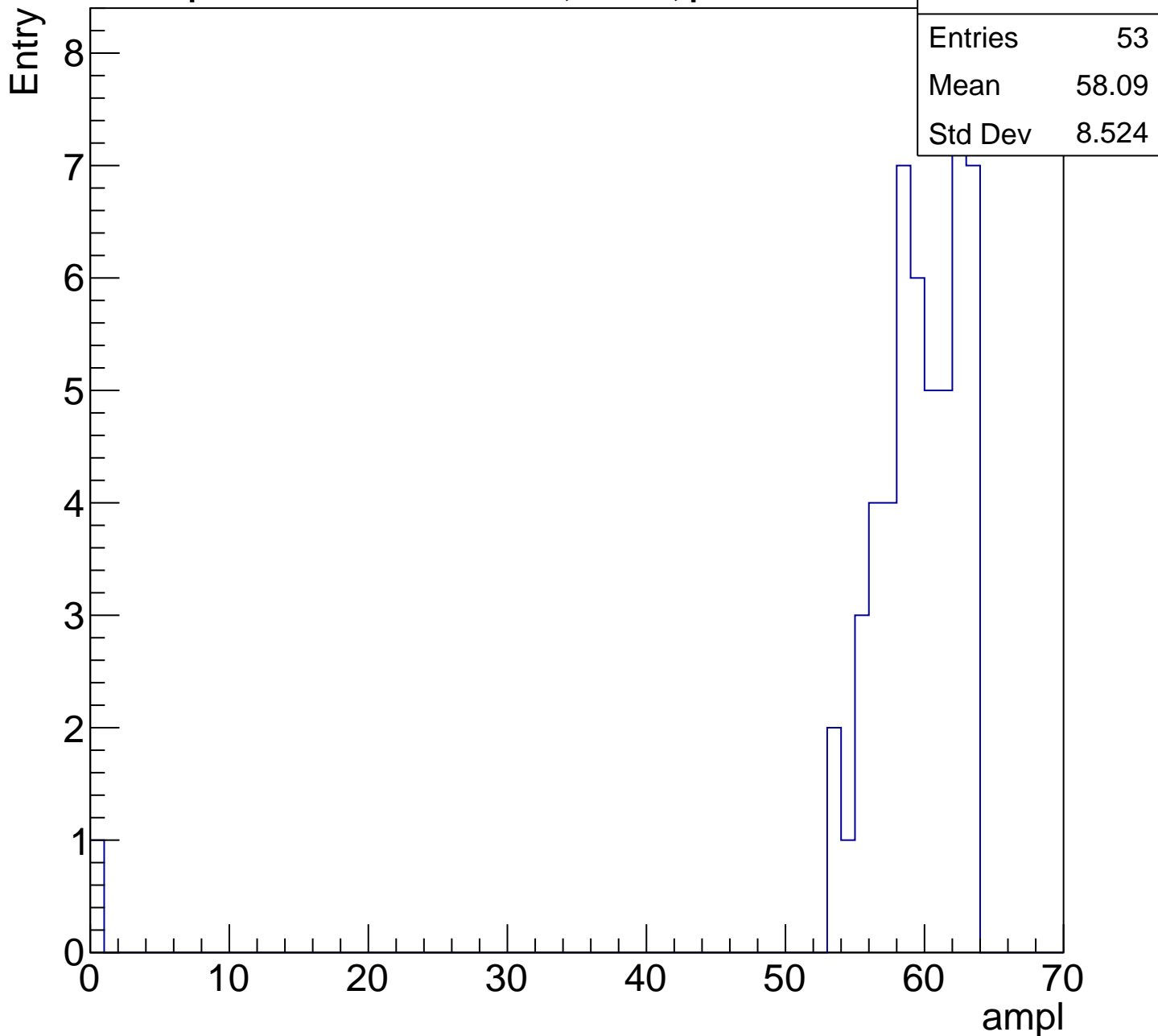
Entry

Entries	49
Mean	55.2
Std Dev	3.136



# B1L003S, U6-ch85, adc5

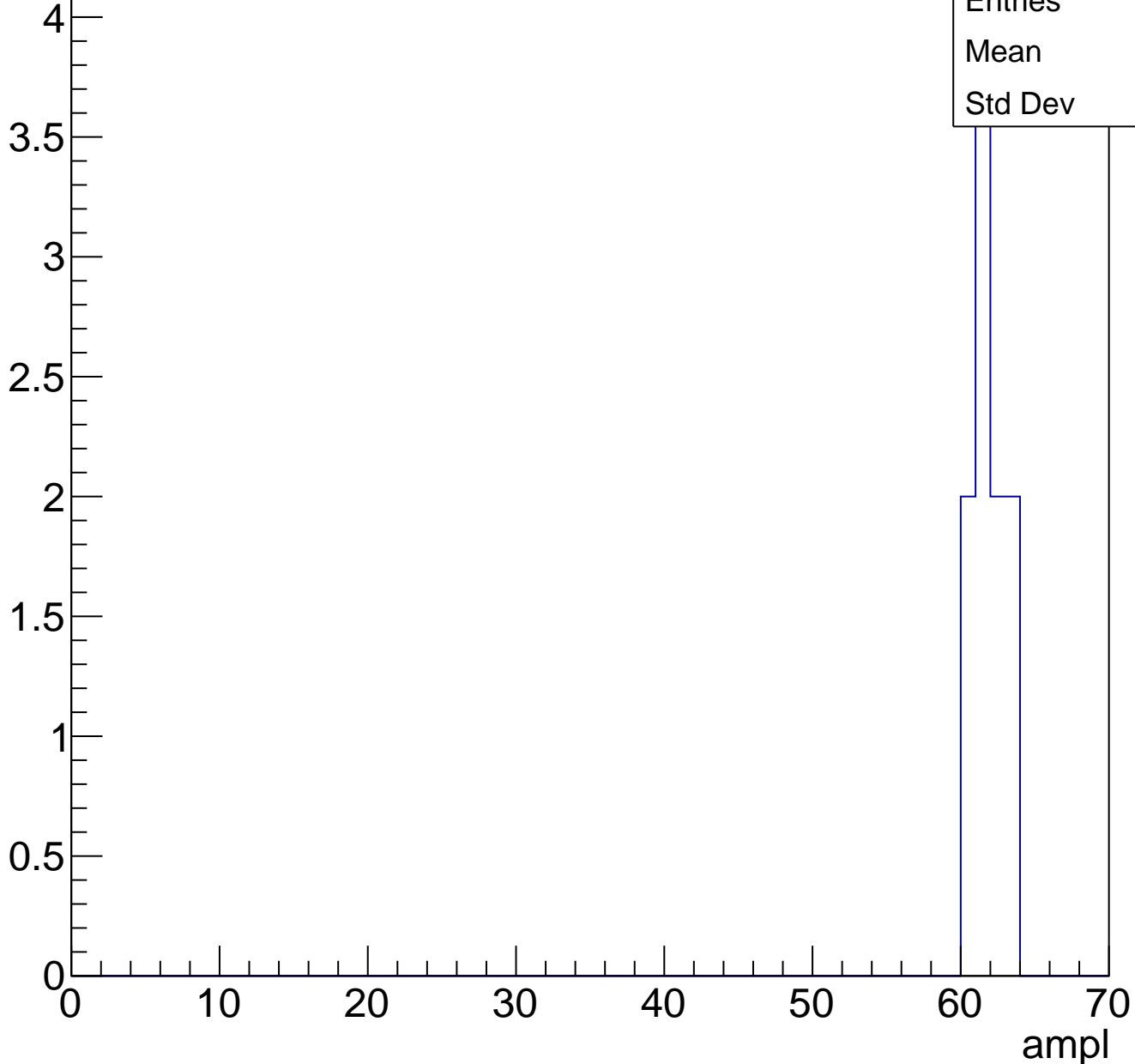
calib\_packv5\_042523\_0143.root, FC#13, port D2



# B1L003S, U6-ch85, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	10
Mean	61.4
Std Dev	1.02



# B1L003S, U6-ch85, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch86, adc0

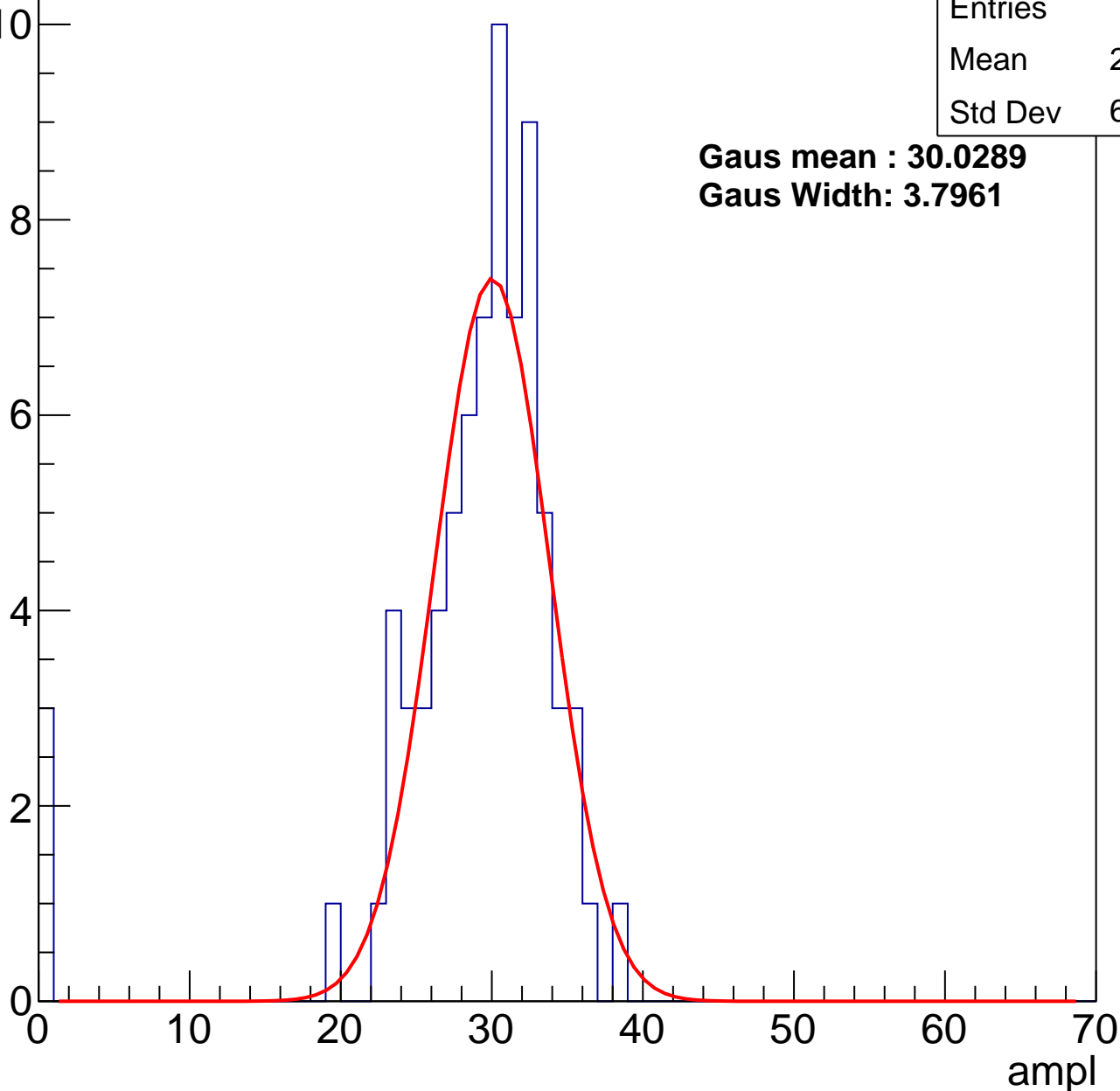
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	76
Mean	28.17
Std Dev	6.748

**Gaus mean : 30.0289**

**Gaus Width: 3.7961**



# B1L003S, U6-ch86, adc1

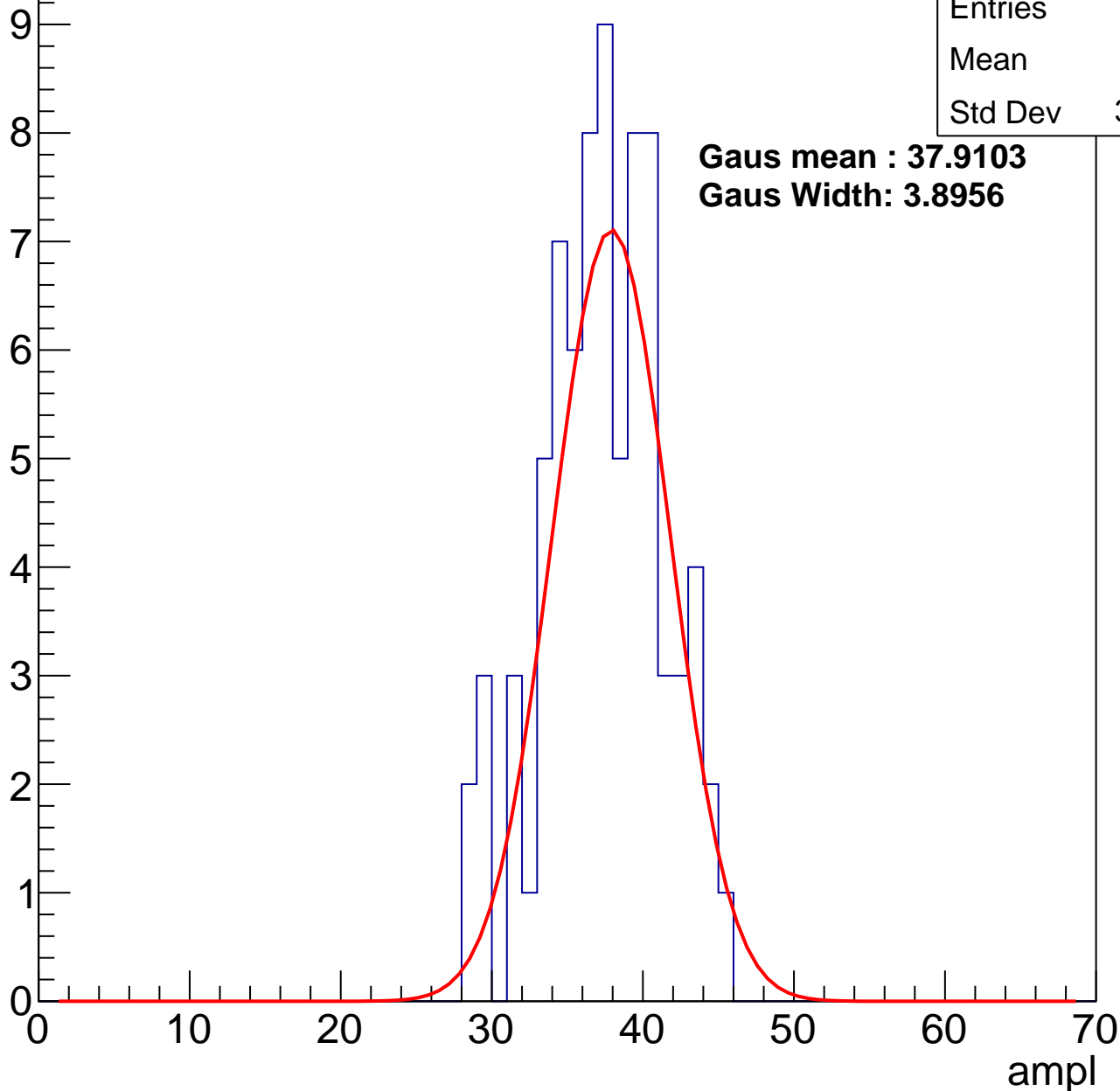
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	78
Mean	36.9
Std Dev	3.921

**Gaus mean : 37.9103**

**Gaus Width: 3.8956**



# B1L003S, U6-ch86, adc2

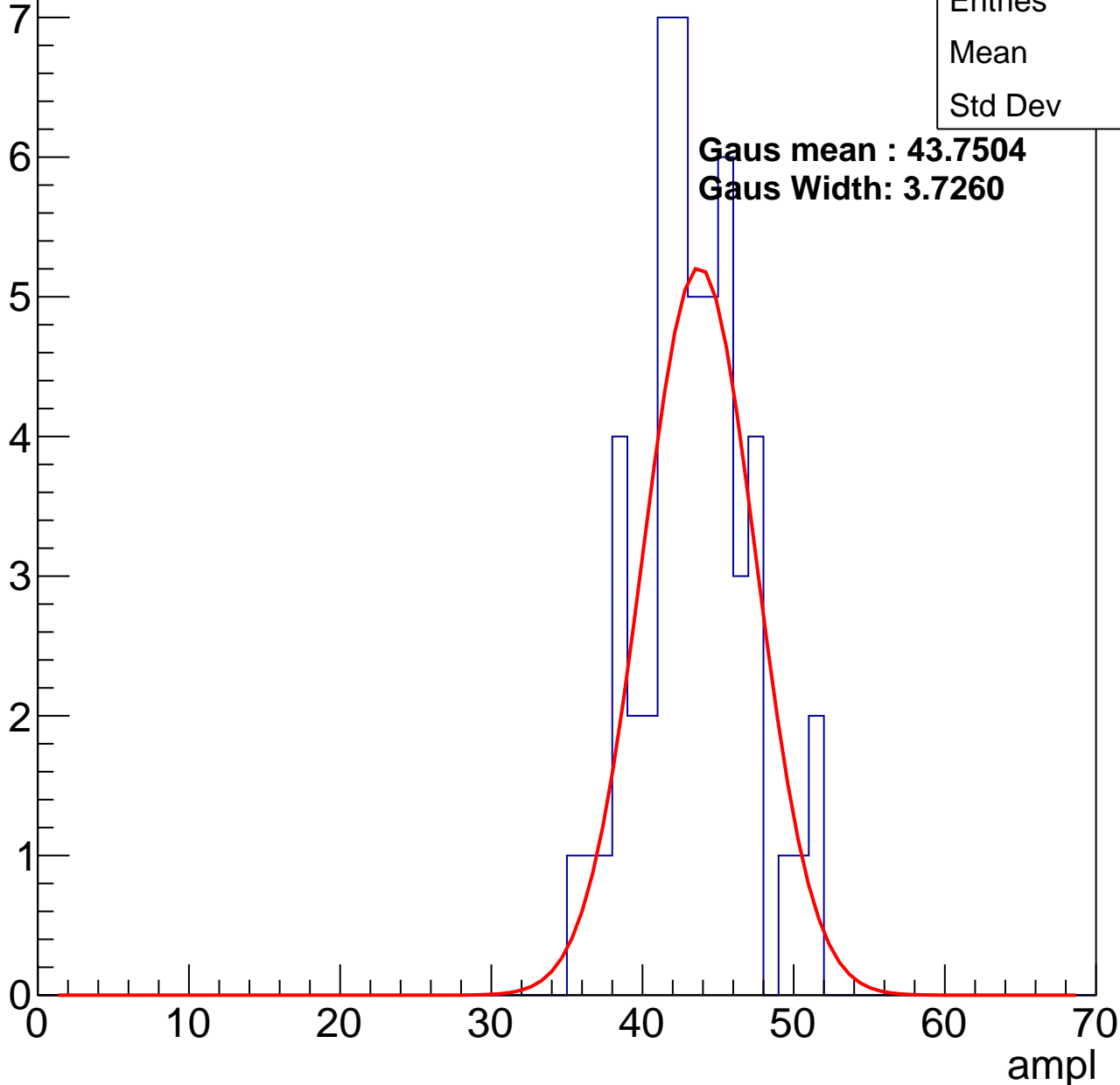
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	52
Mean	42.9
Std Dev	3.58

**Gaus mean : 43.7504**

**Gaus Width: 3.7260**

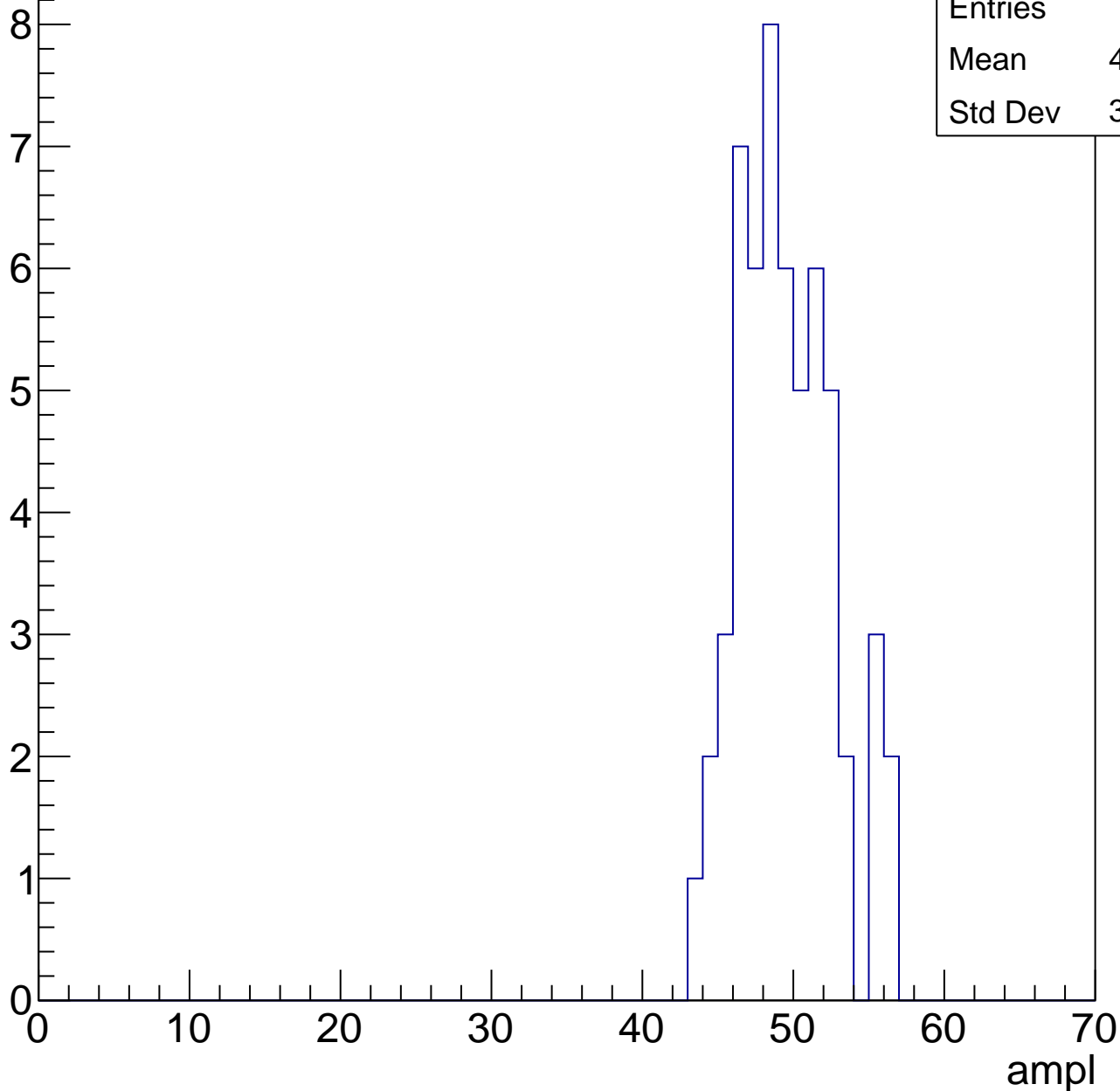


# B1L003S, U6-ch86, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	49.05
Std Dev	3.108



# B1L003S, U6-ch86, adc4

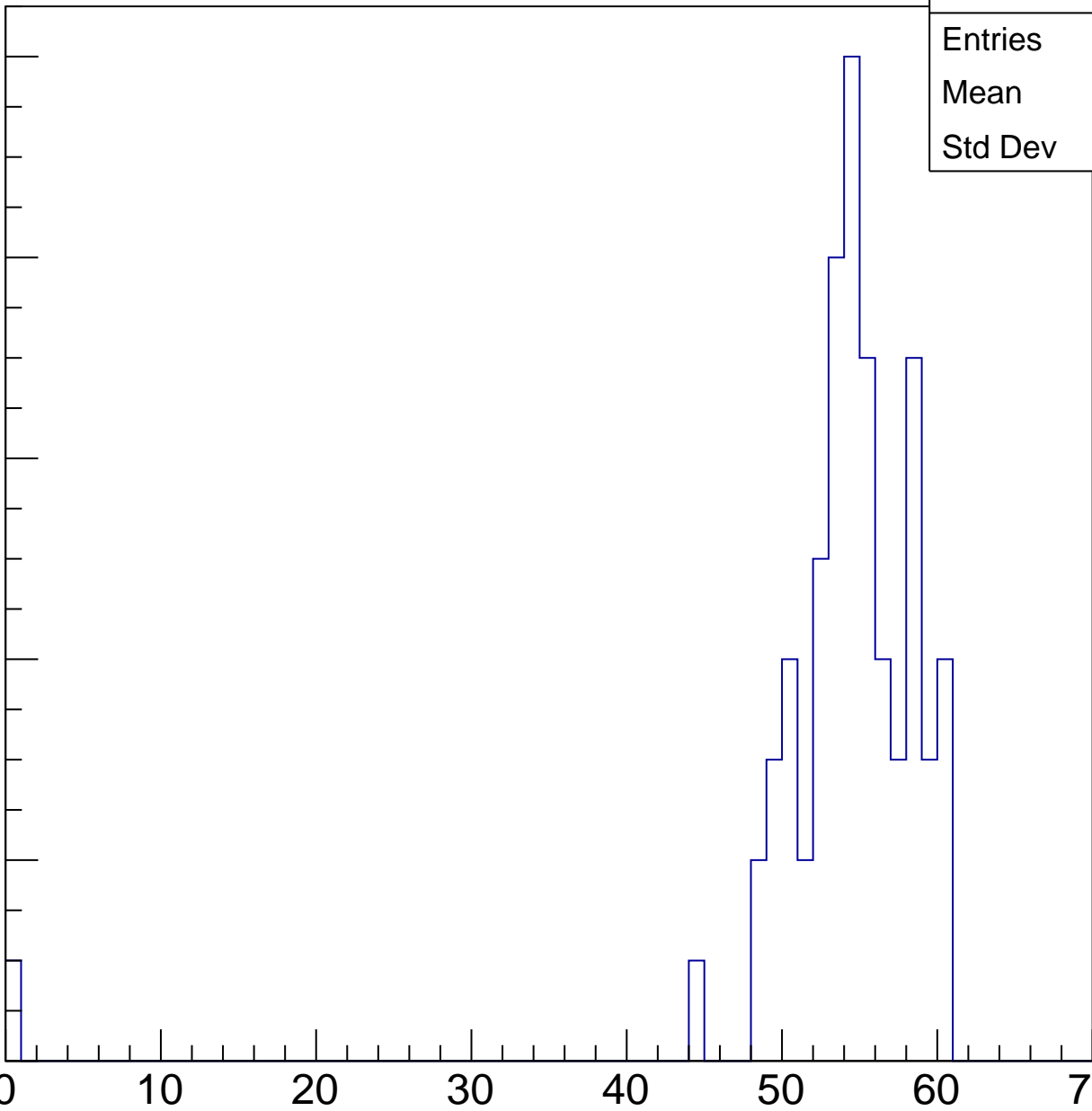
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	64
Mean	53.38
Std Dev	7.53

Entry

10  
8  
6  
4  
2  
0

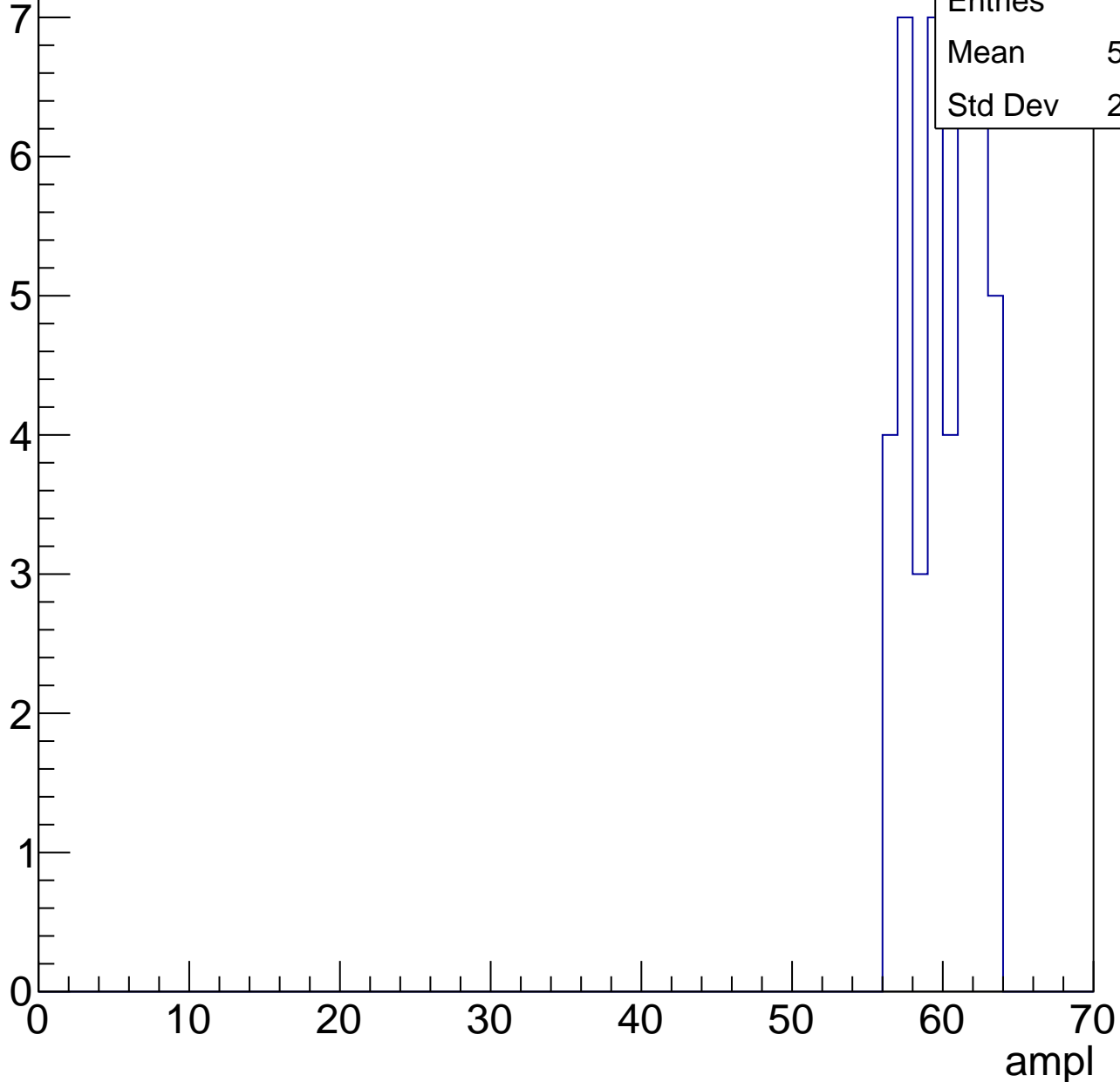
ampl



# B1L003S, U6-ch86, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

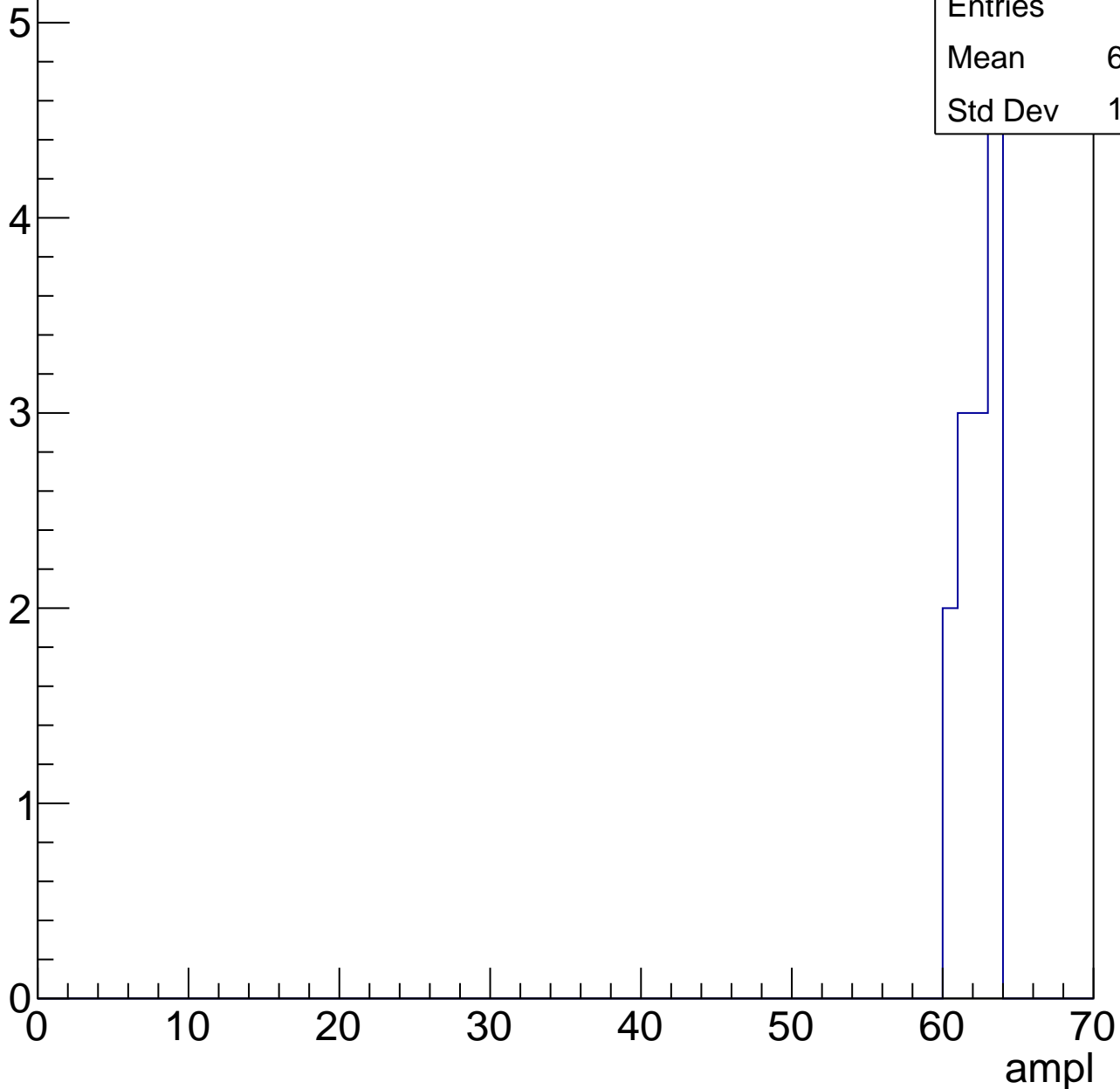


# B1L003S, U6-ch86, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	13
Mean	61.85
Std Dev	1.099





# B1L003S, U6-ch86, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U6-ch87, adc0

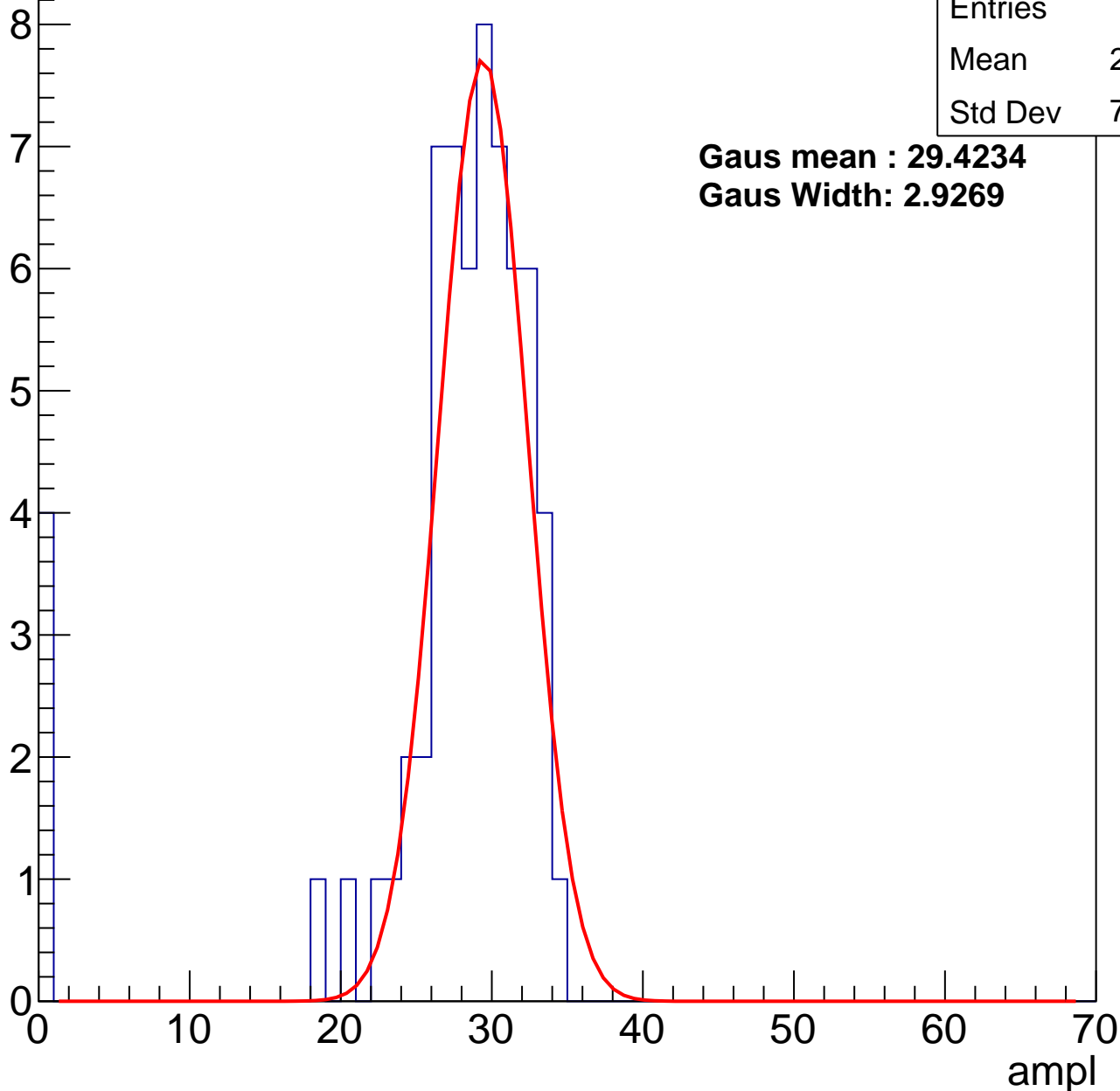
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	26.66
Std Dev	7.554

**Gaus mean : 29.4234**

**Gaus Width: 2.9269**



# B1L003S, U6-ch87, adc1

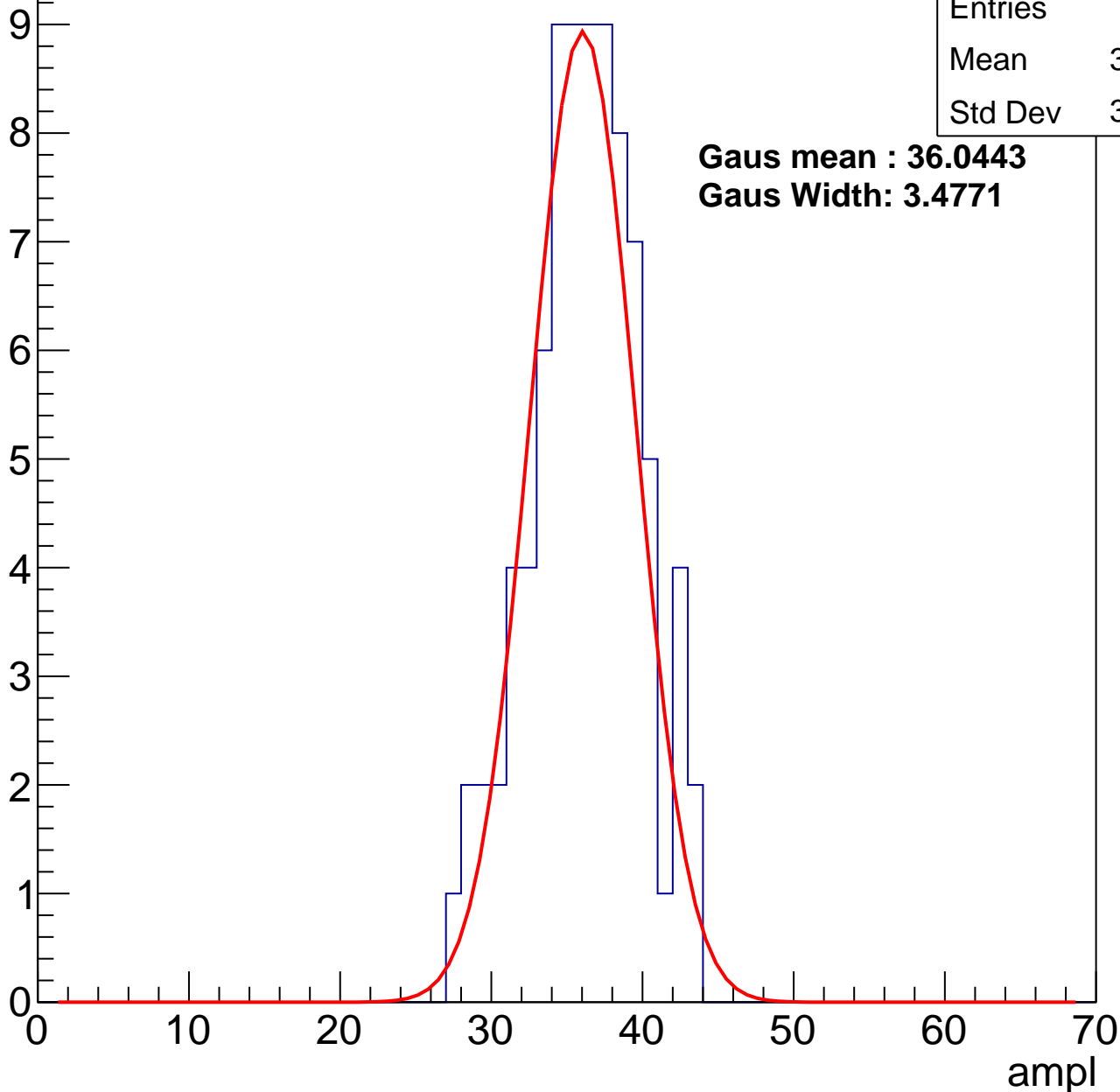
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	84
Mean	35.73
Std Dev	3.597

**Gaus mean : 36.0443**

**Gaus Width: 3.4771**

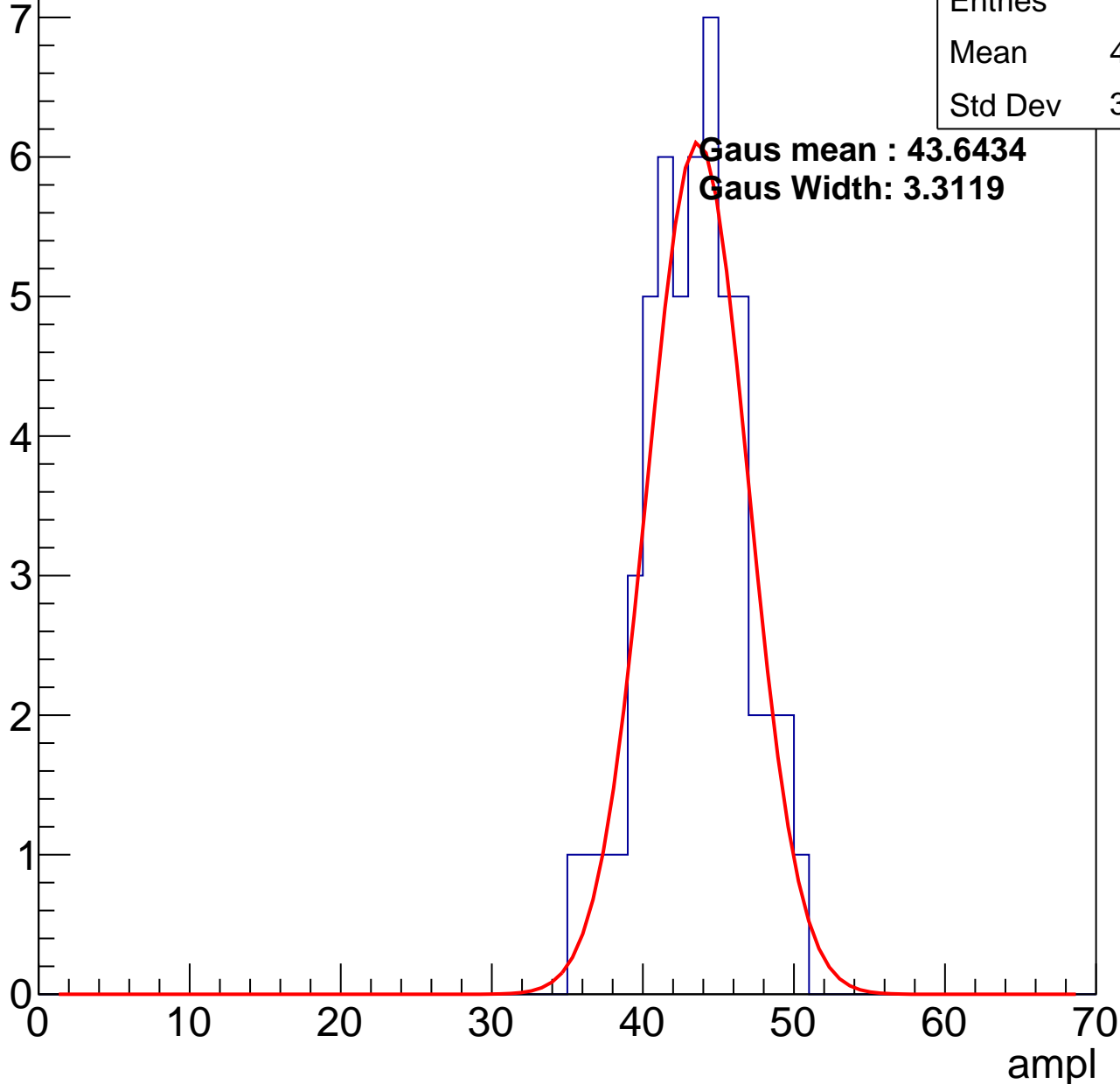


# B1L003S, U6-ch87, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

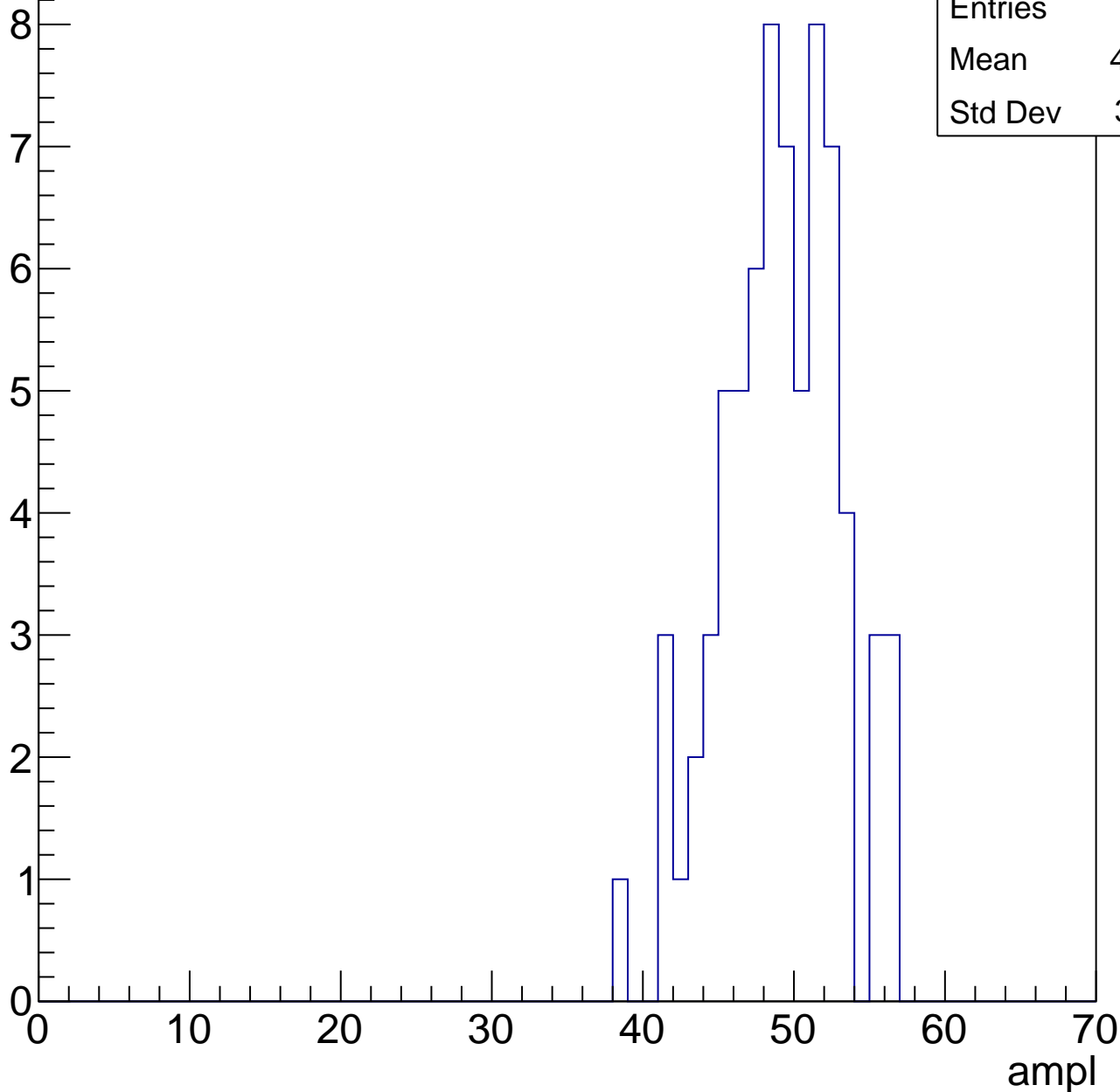
Entries	53
Mean	42.98
Std Dev	3.282



# B1L003S, U6-ch87, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



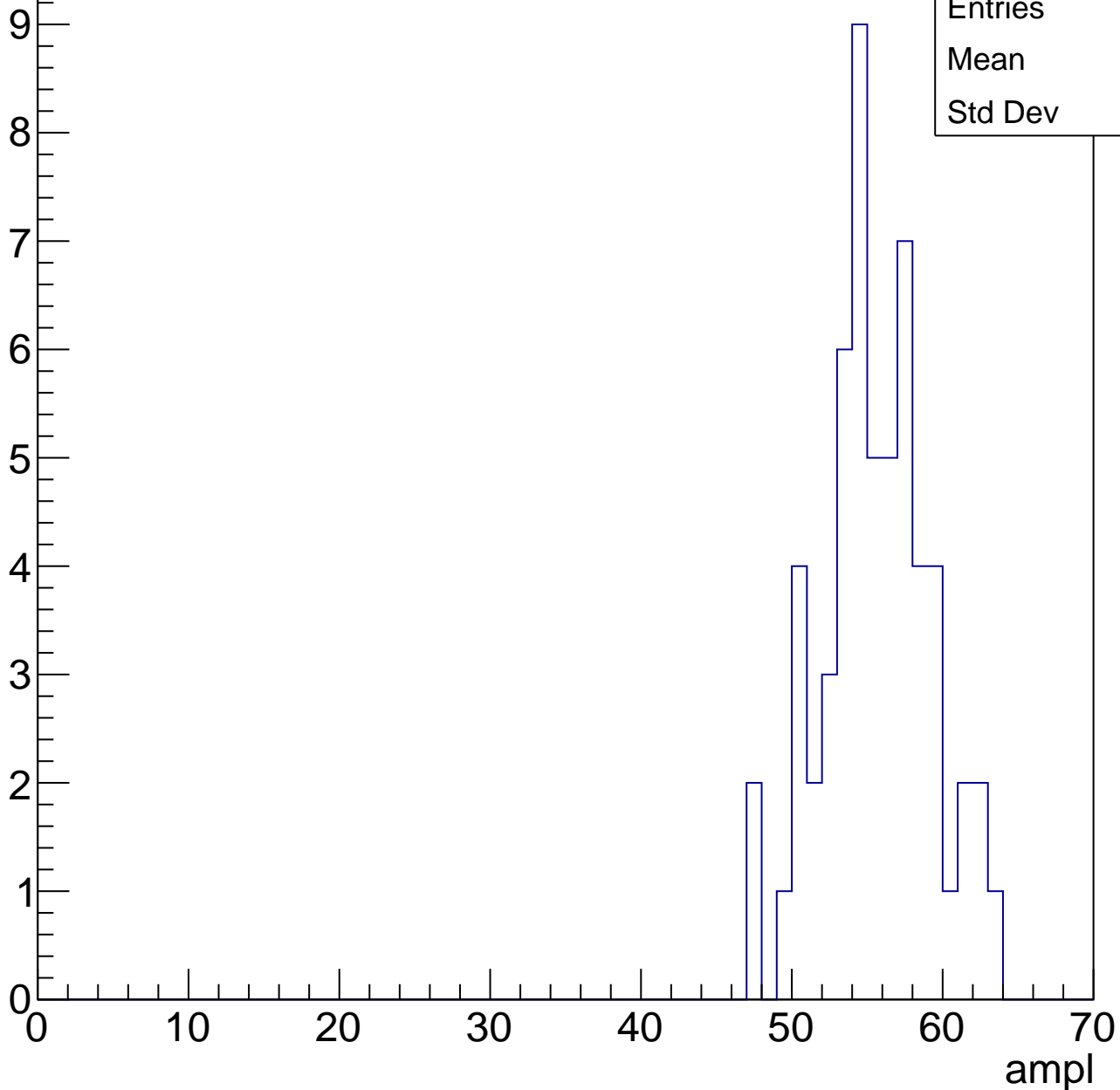
Entries	71
Mean	48.62
Std Dev	3.891

# B1L003S, U6-ch87, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	55.1
Std Dev	3.59

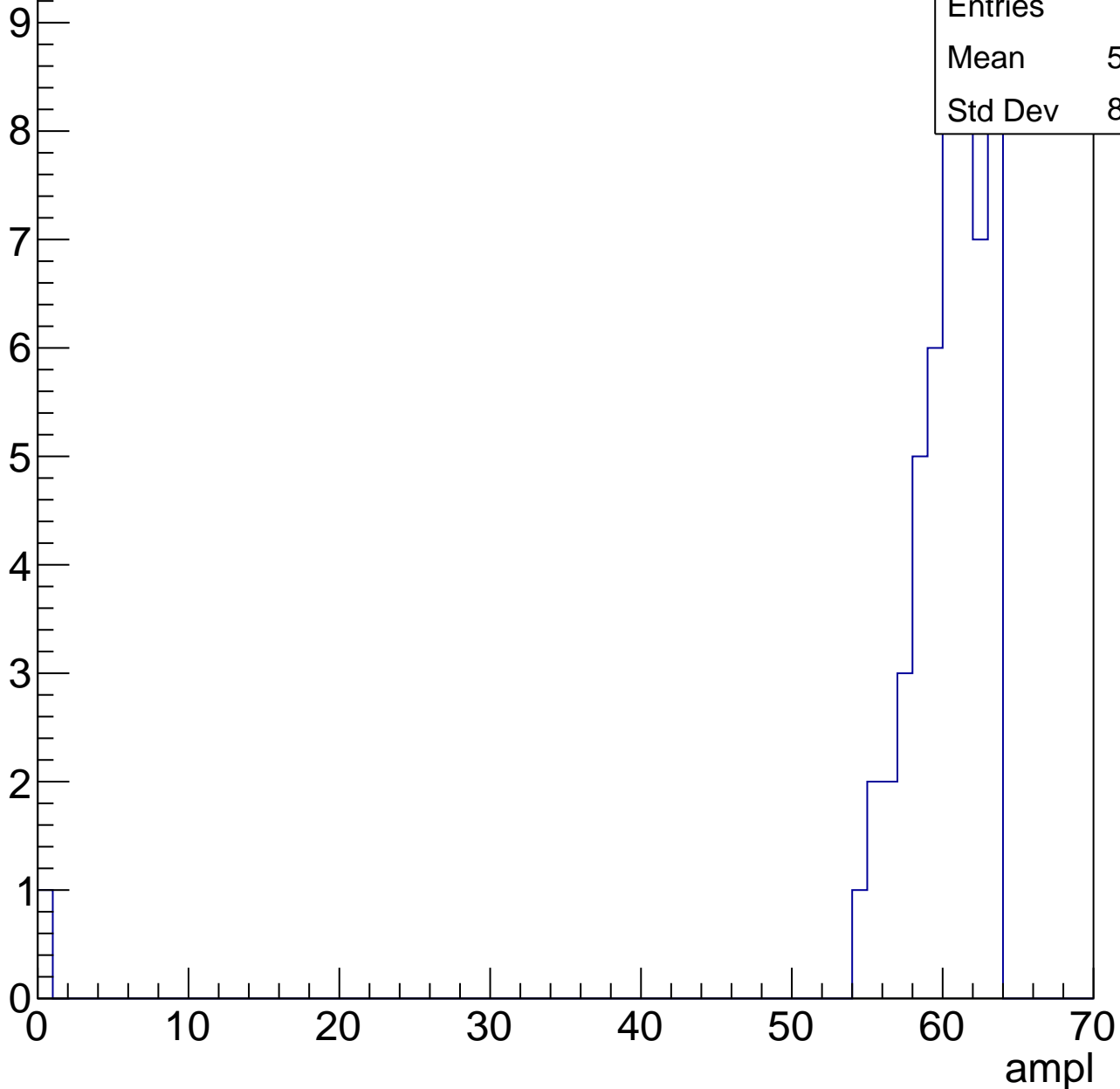


# B1L003S, U6-ch87, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

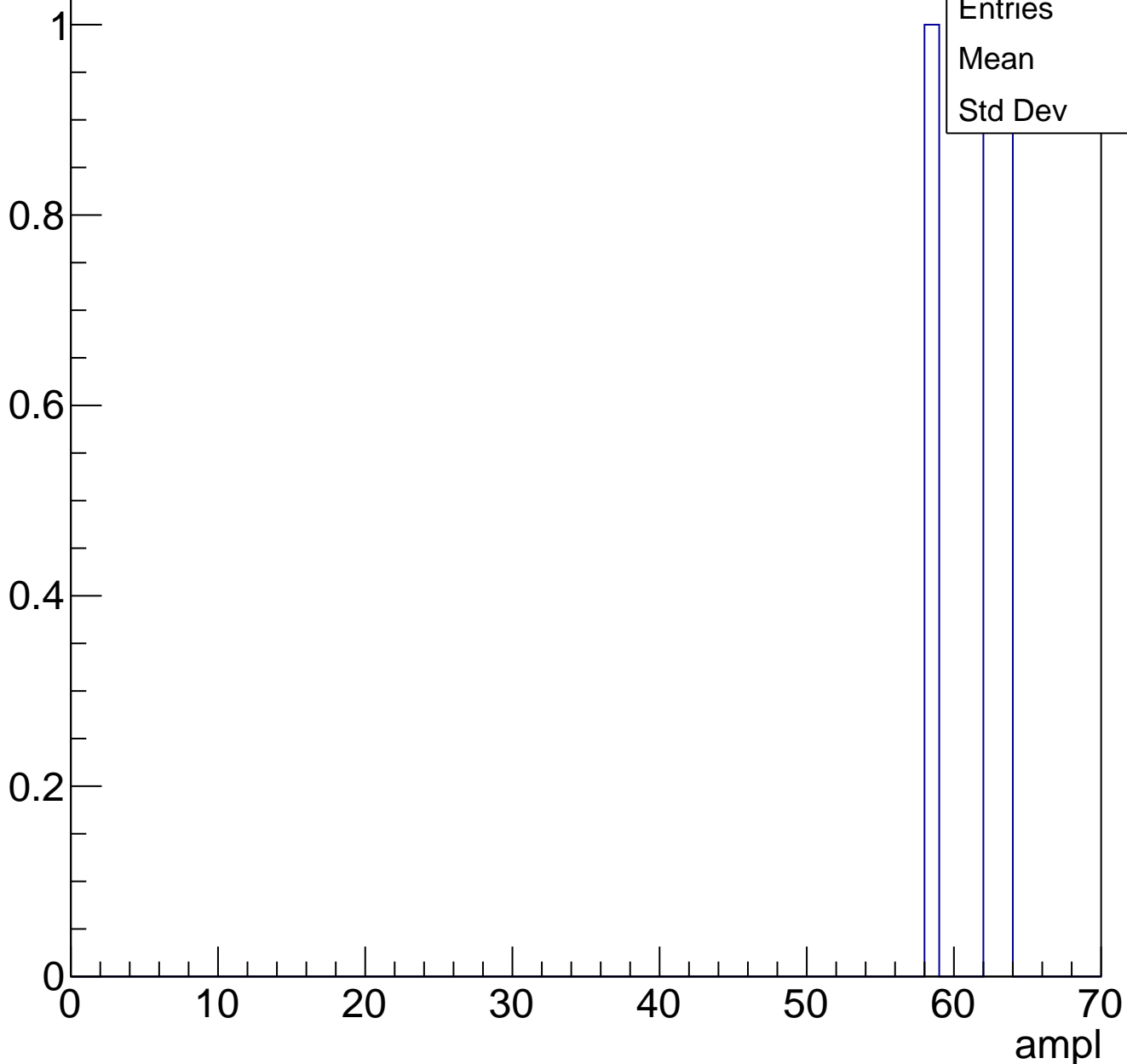
Entries	52
Mean	58.79
Std Dev	8.552



# B1L003S, U6-ch87, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch87, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch88, adc0

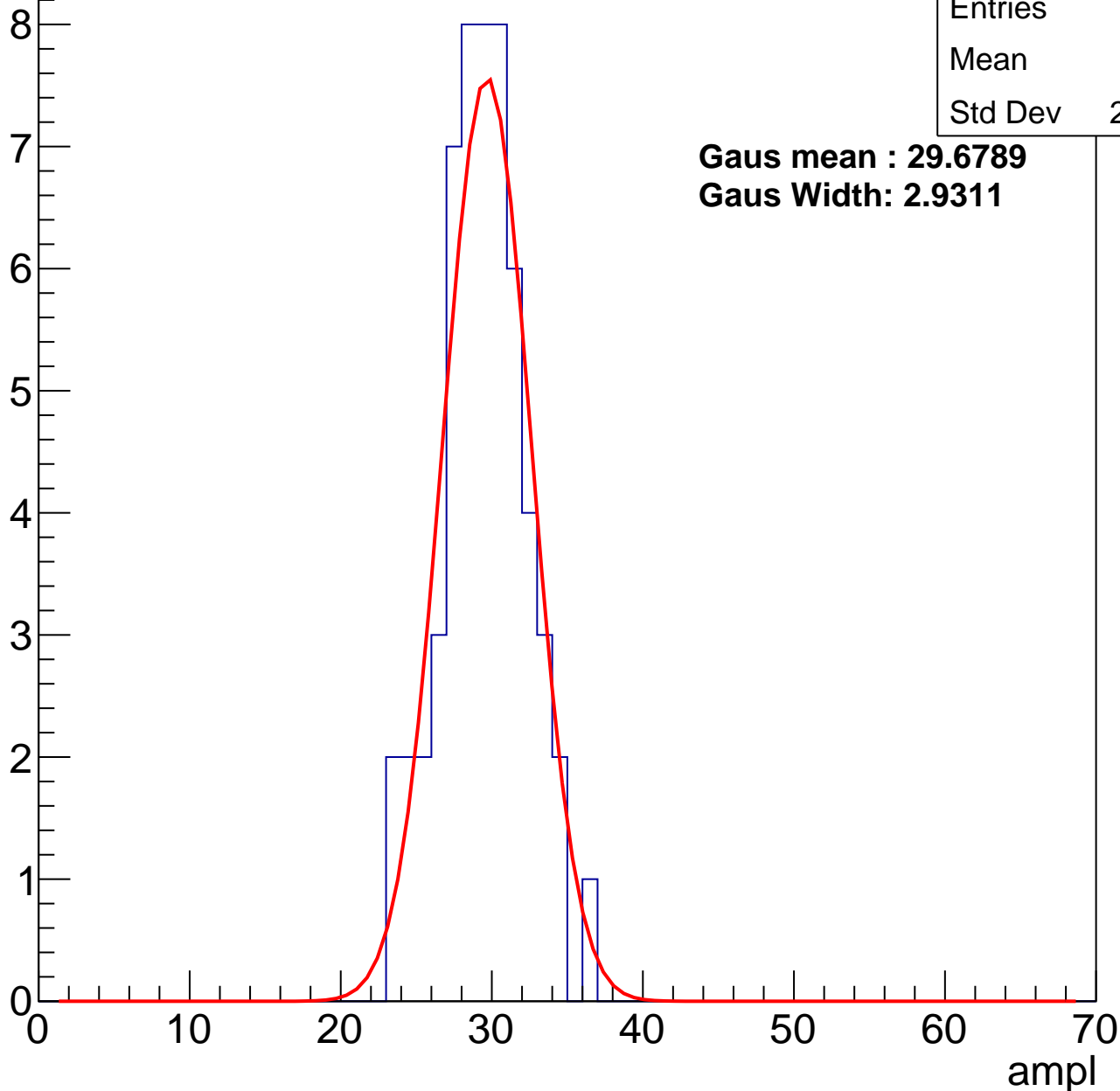
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	29
Std Dev	2.777

**Gaus mean : 29.6789**

**Gaus Width: 2.9311**



# B1L003S, U6-ch88, adc1

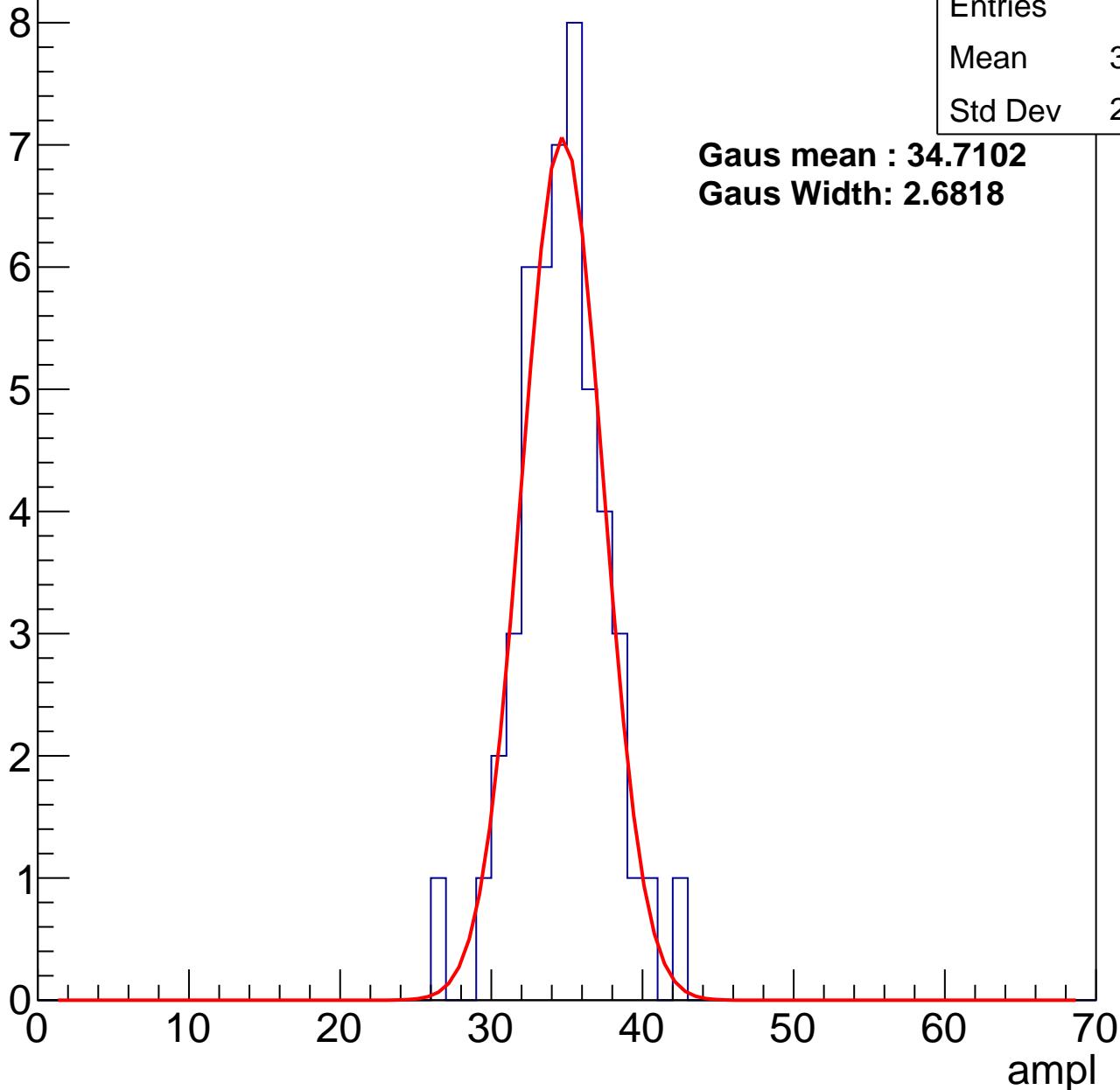
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	49
Mean	34.27
Std Dev	2.898

**Gaus mean : 34.7102**

**Gaus Width: 2.6818**



# B1L003S, U6-ch88, adc2

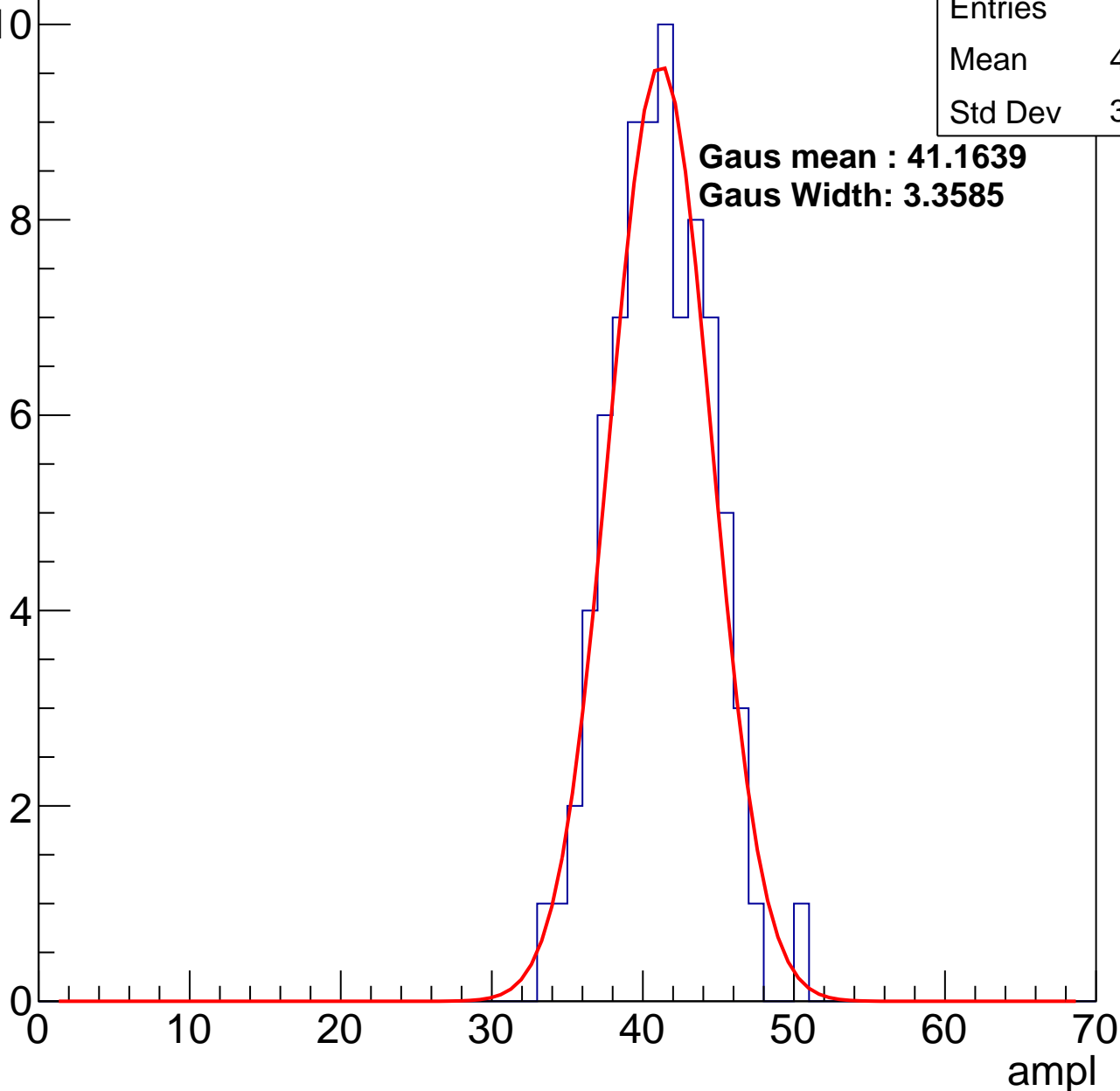
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	81
Mean	40.69
Std Dev	3.249

**Gaus mean : 41.1639**

**Gaus Width: 3.3585**

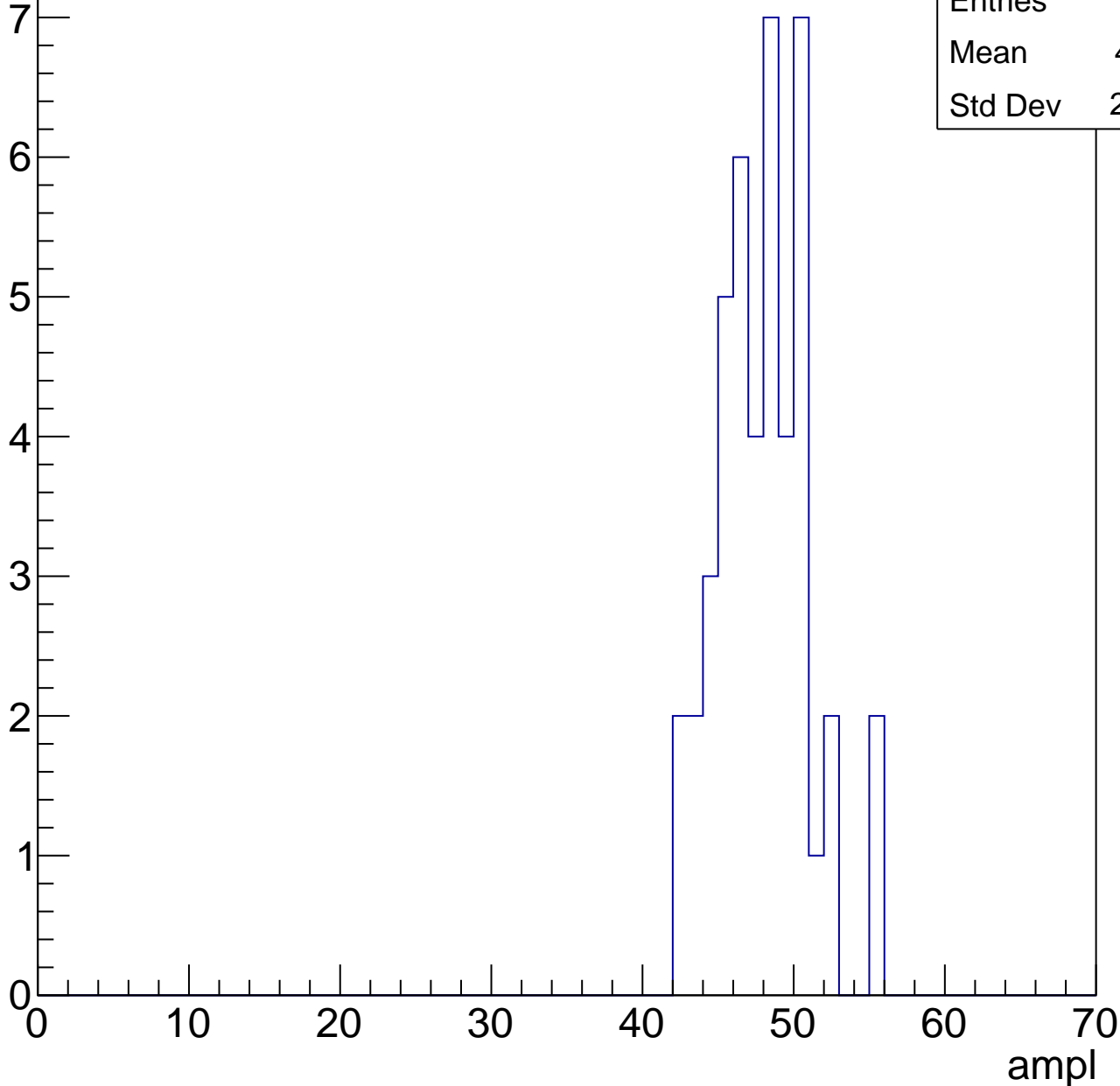


# B1L003S, U6-ch88, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

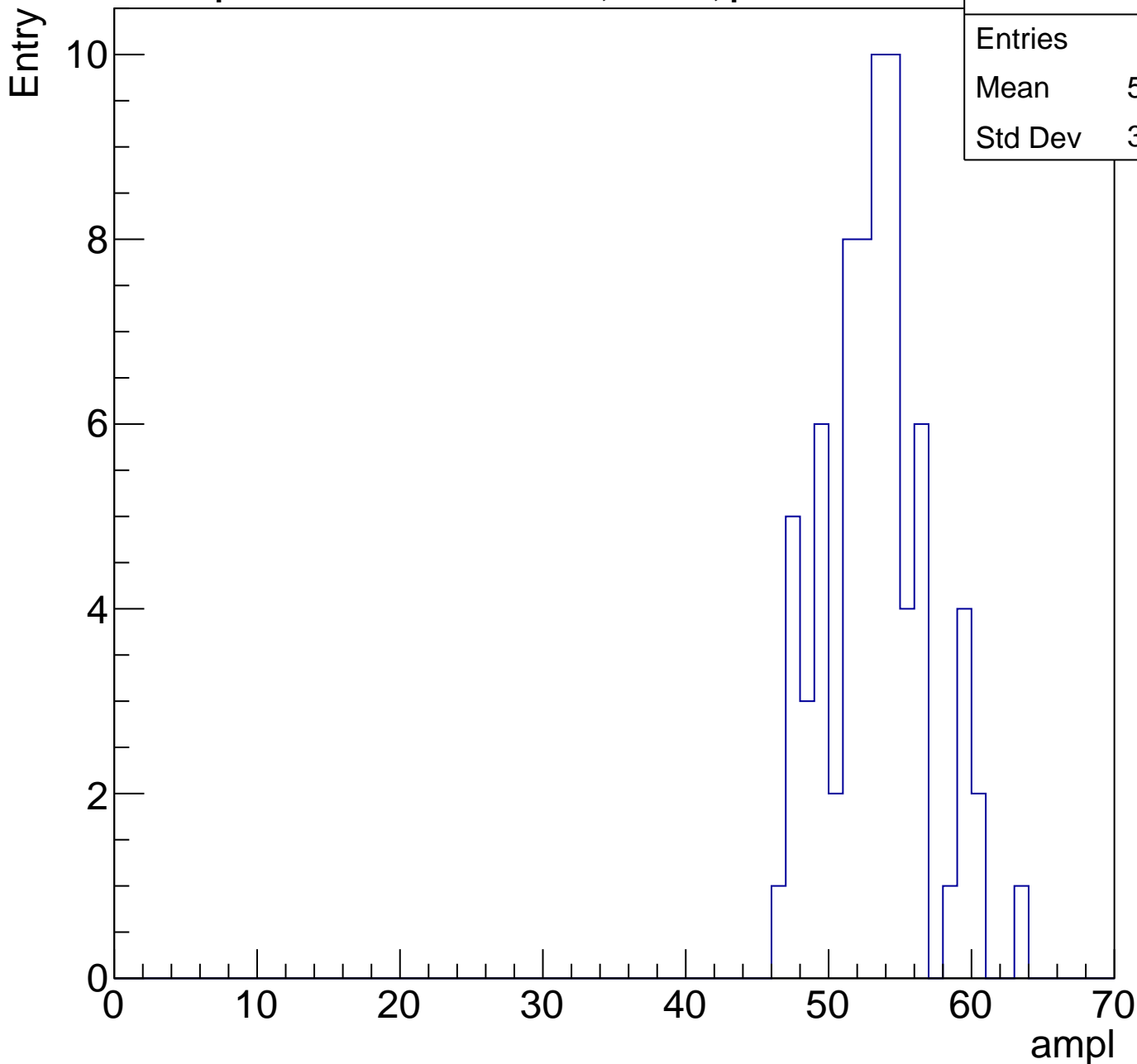
Entries	45
Mean	47.51
Std Dev	2.993



# B1L003S, U6-ch88, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	71
Mean	52.76
Std Dev	3.562



# B1L003S, U6-ch88, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	56
Mean	58.82
Std Dev	2.529

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

70

ampl

1

4

10

8

6

4

2

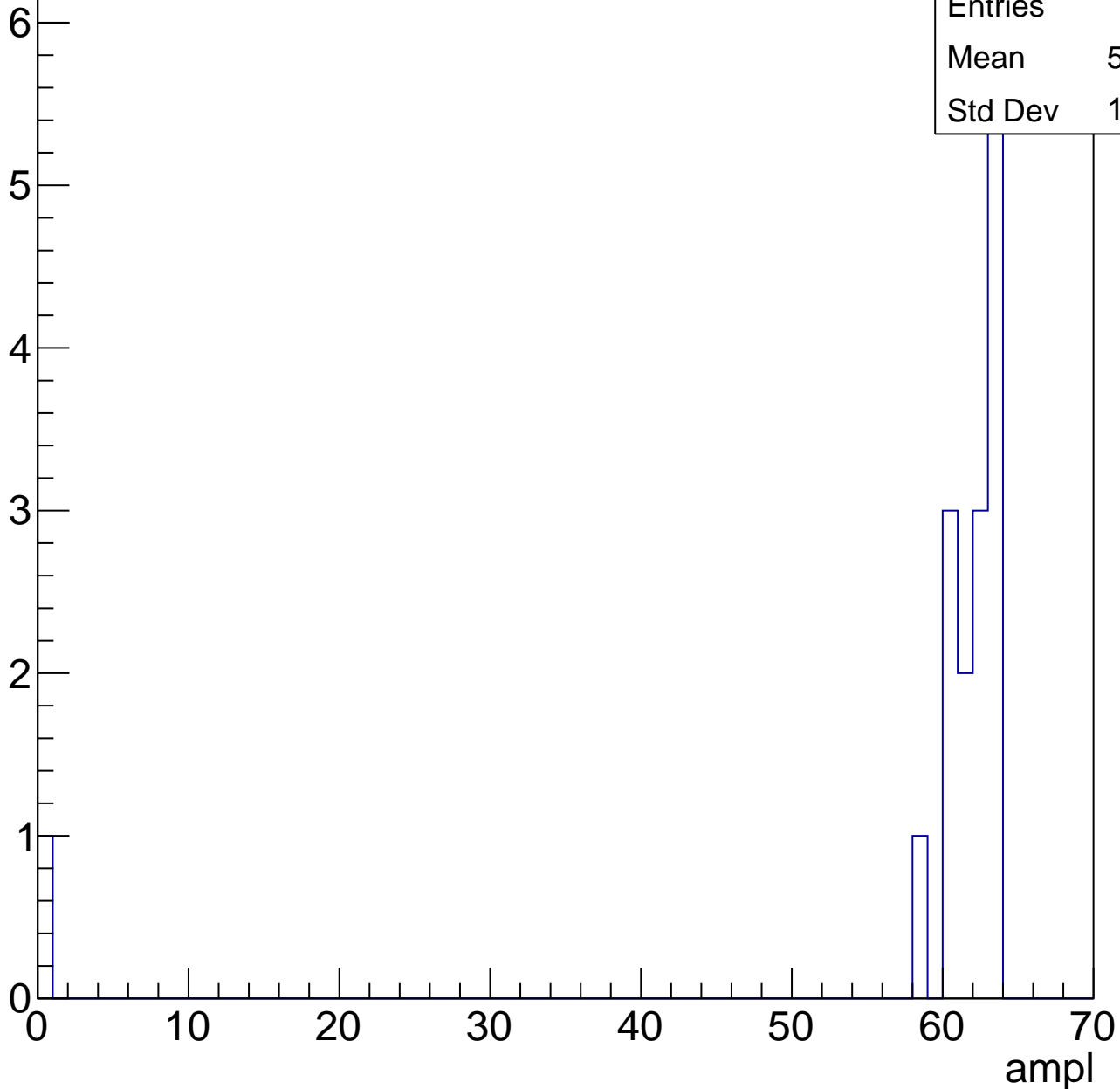
0

# B1L003S, U6-ch88, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	16
Mean	57.75
Std Dev	14.98





# B1L003S, U6-ch88, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch89, adc0

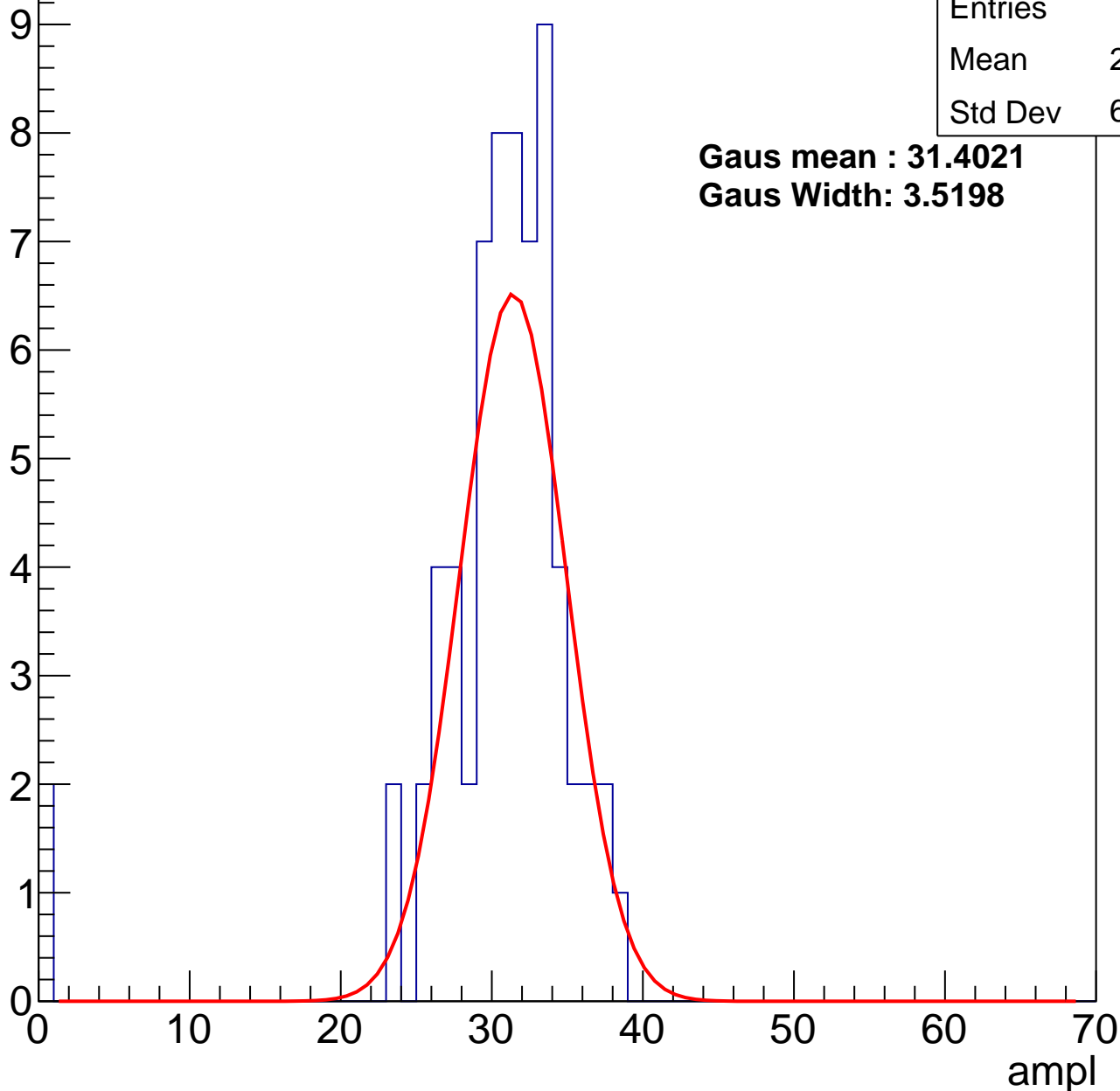
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	29.79
Std Dev	6.185

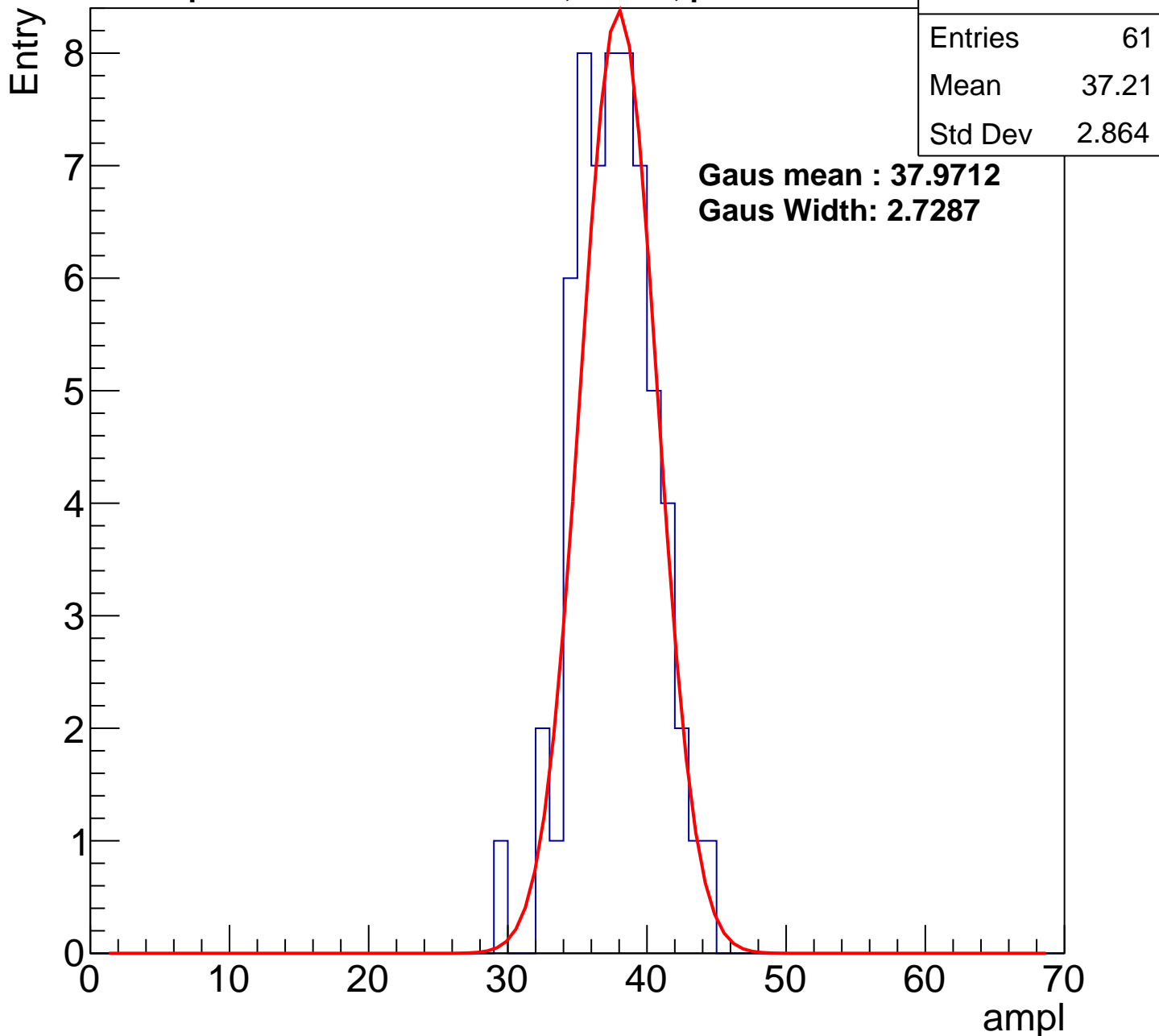
**Gaus mean : 31.4021**

**Gaus Width: 3.5198**



# B1L003S, U6-ch89, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2



# B1L003S, U6-ch89, adc2

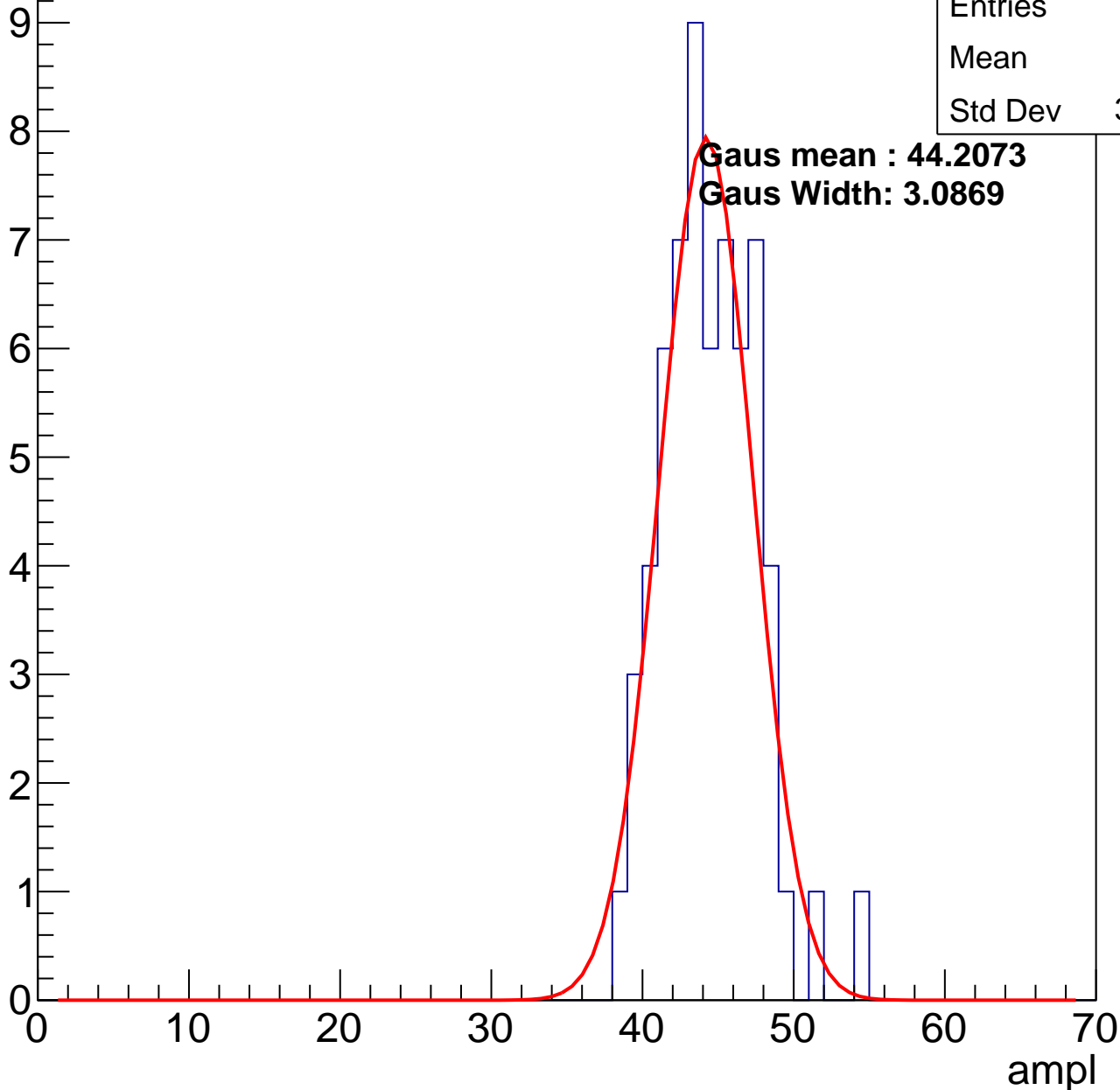
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	44
Std Dev	3.081

**Gaus mean : 44.2073**

**Gaus Width: 3.0869**

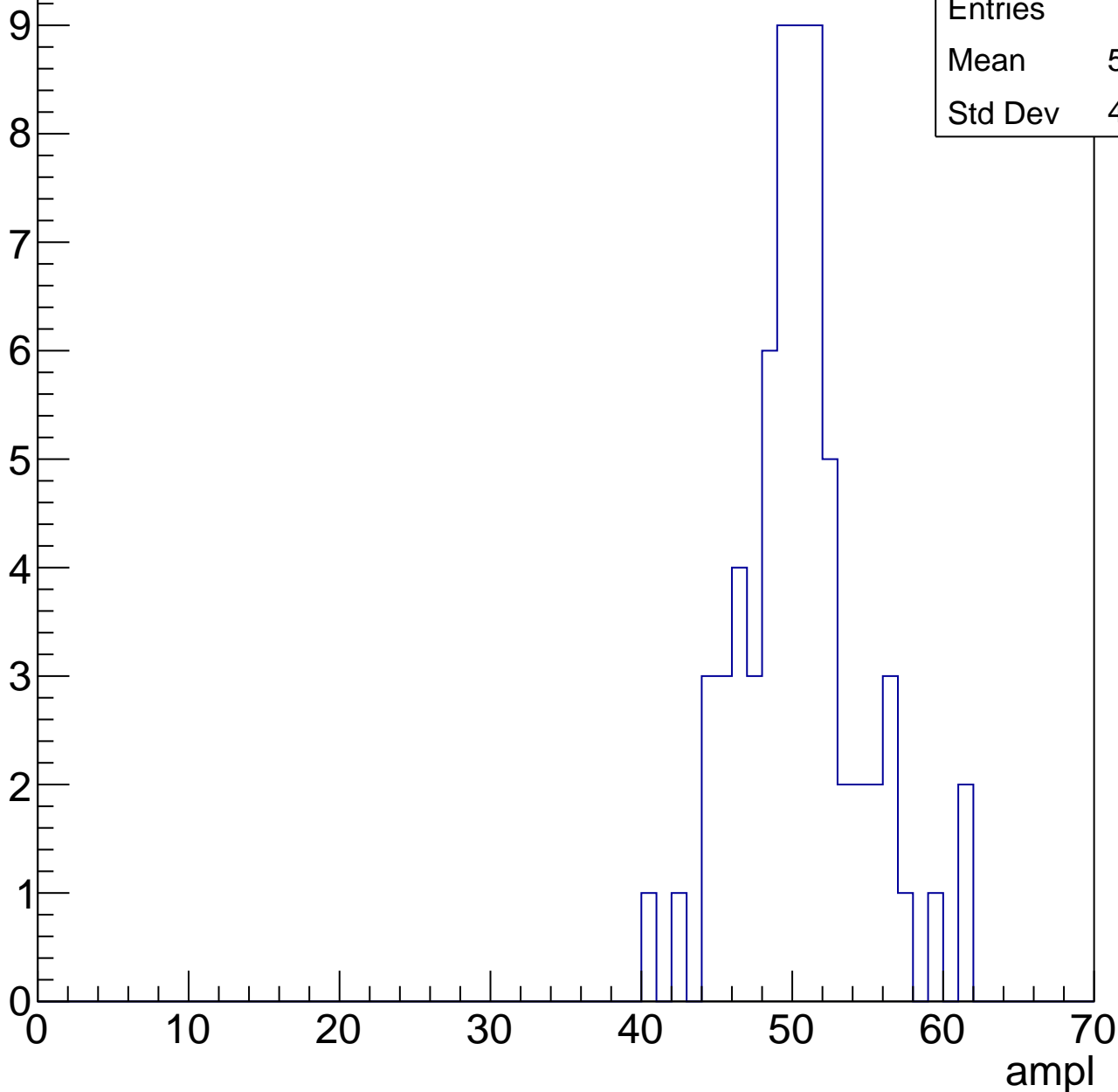


# B1L003S, U6-ch89, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	50.03
Std Dev	4.045

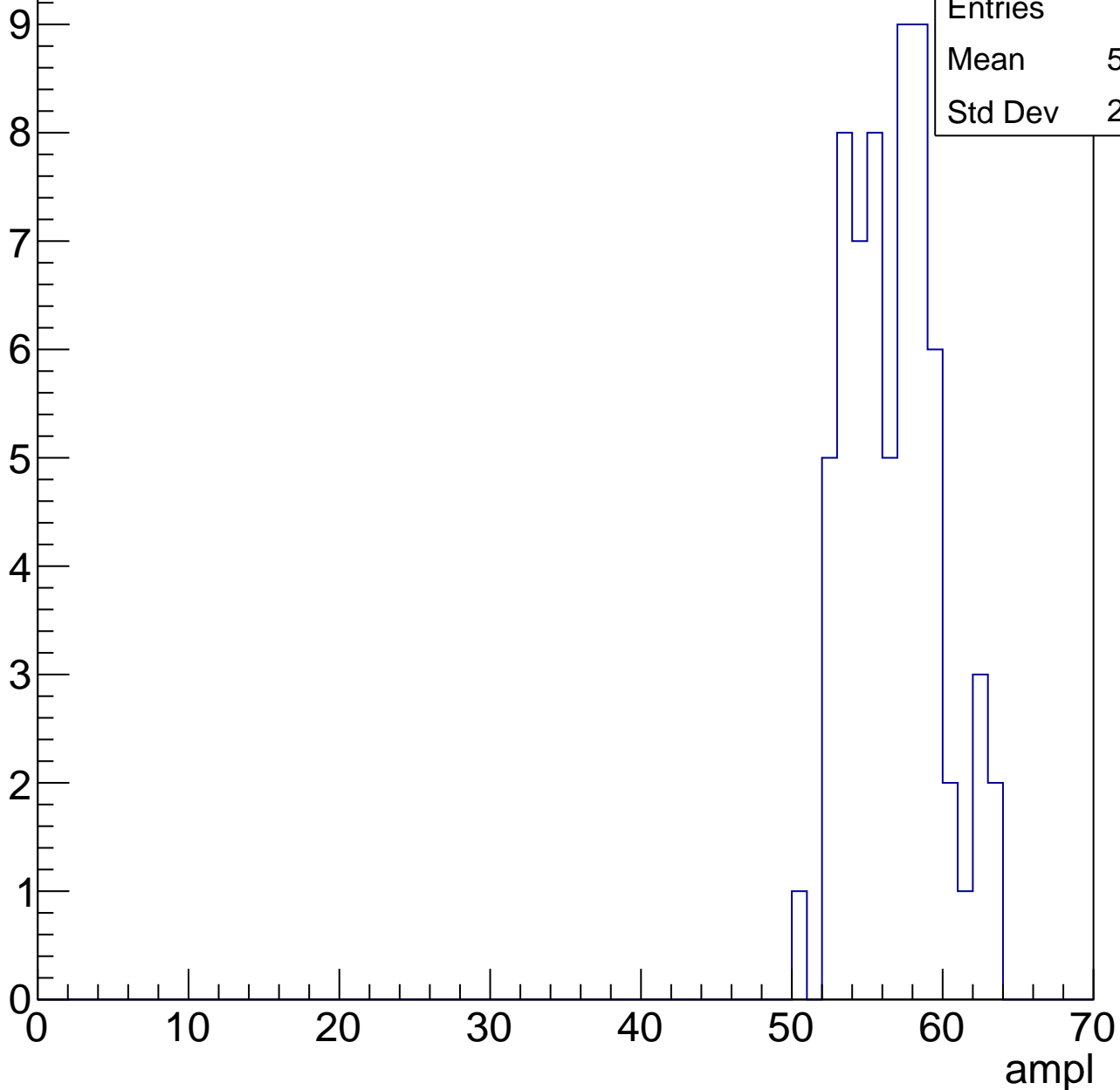


# B1L003S, U6-ch89, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	56.27
Std Dev	2.967

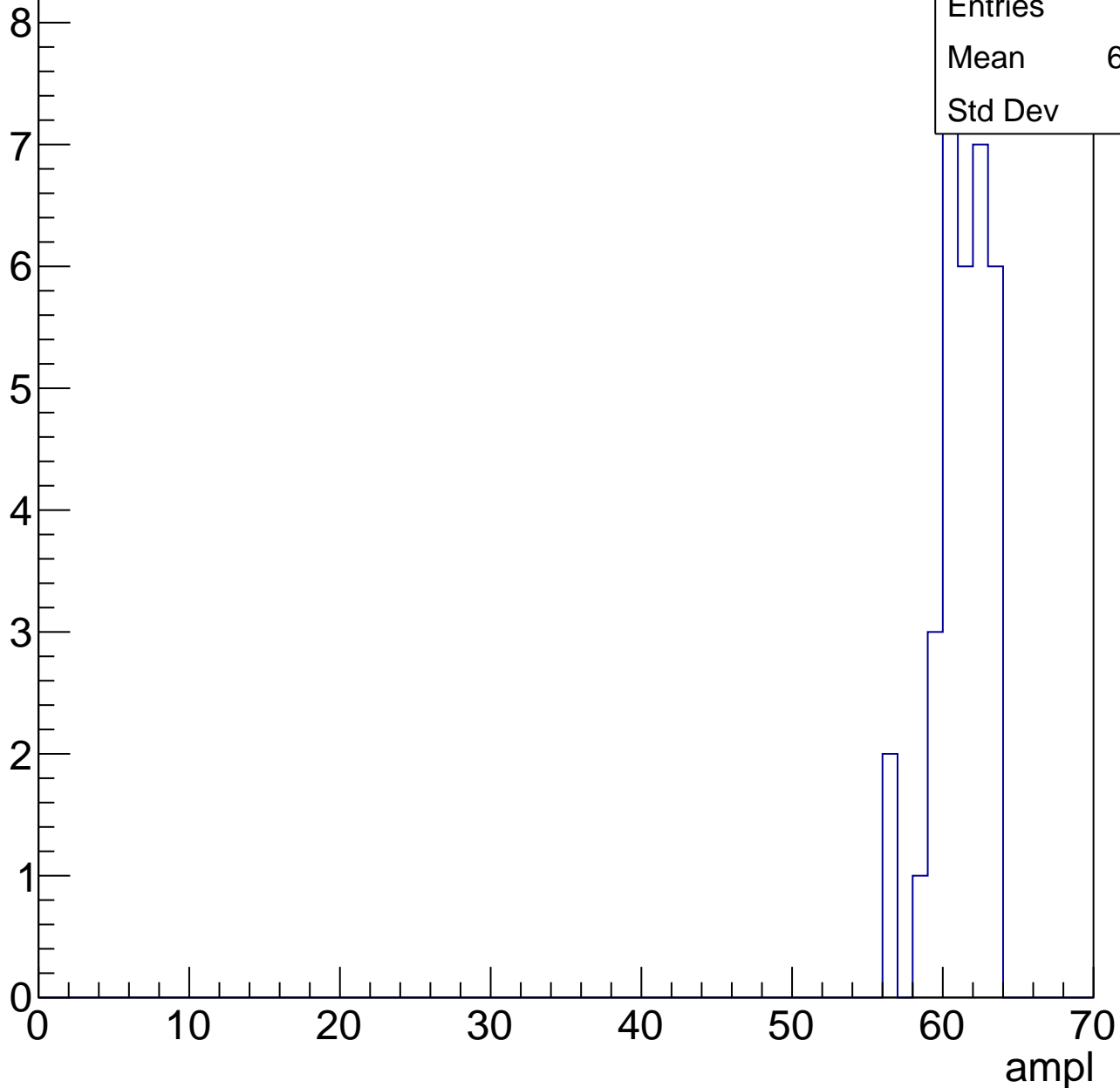


# B1L003S, U6-ch89, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

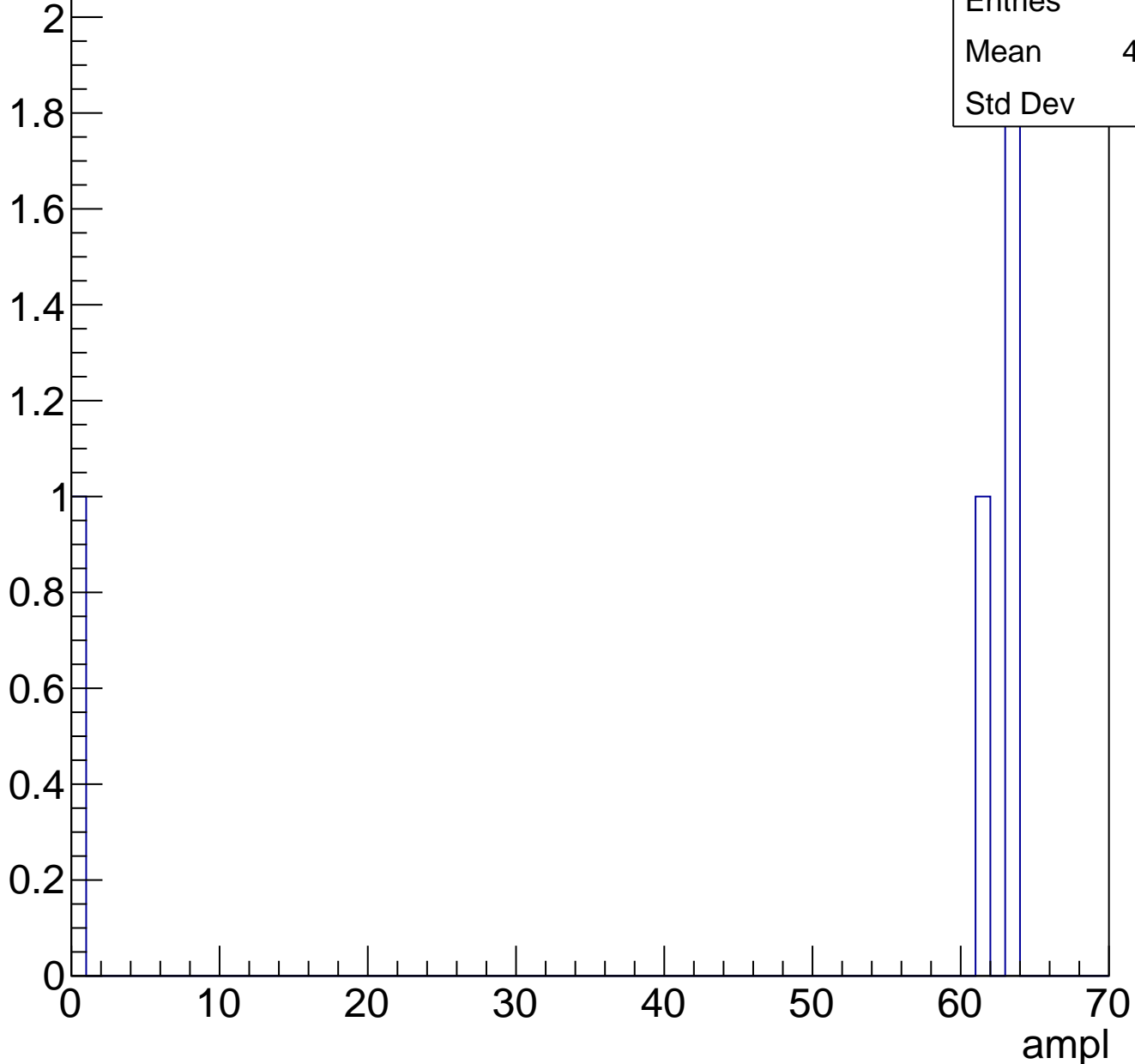
Entries	33
Mean	60.76
Std Dev	1.81



# B1L003S, U6-ch89, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	4
Mean	46.75
Std Dev	27



# B1L003S, U6-ch89, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch90, adc0

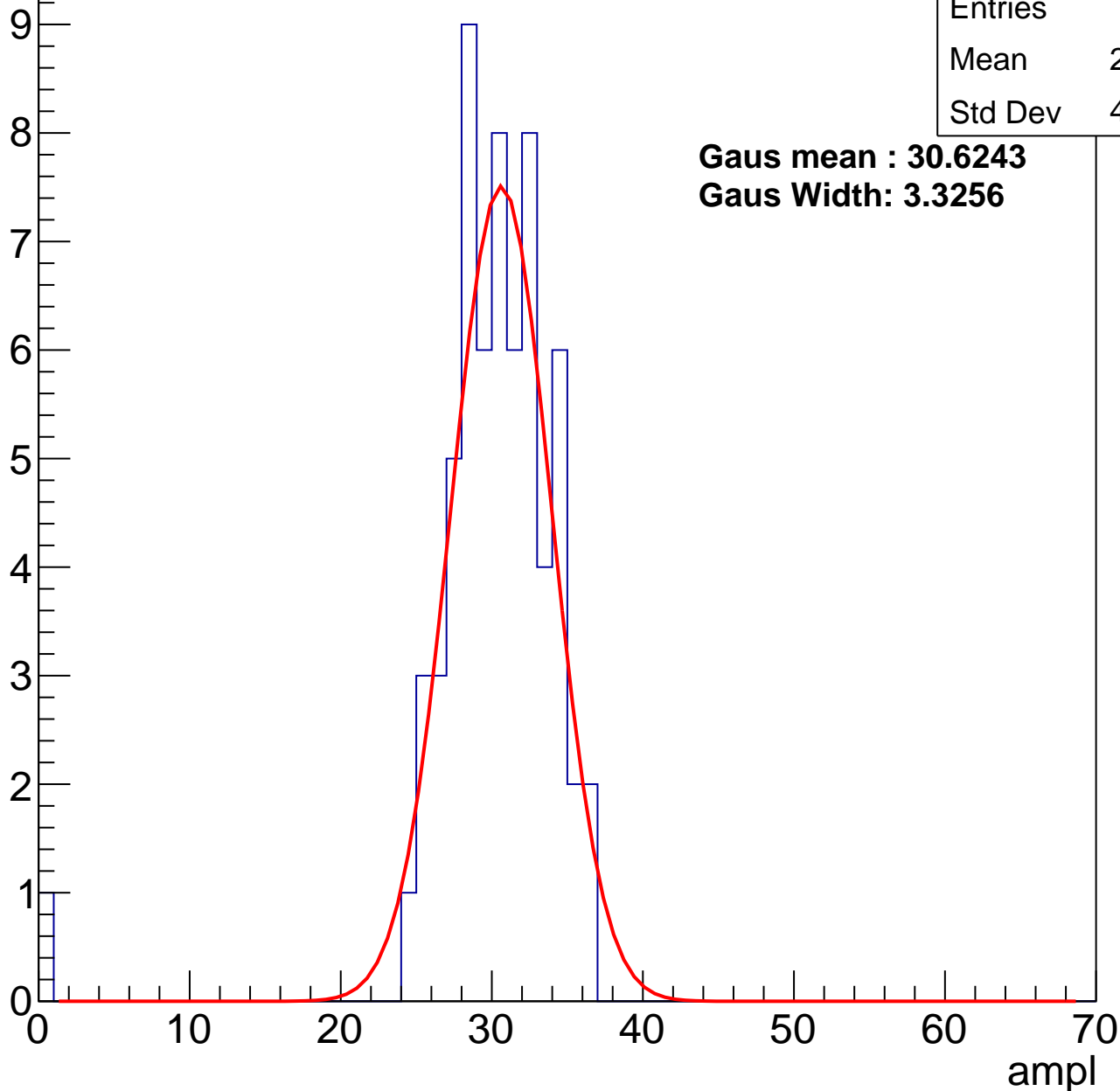
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	29.66
Std Dev	4.728

**Gaus mean : 30.6243**

**Gaus Width: 3.3256**



# B1L003S, U6-ch90, adc1

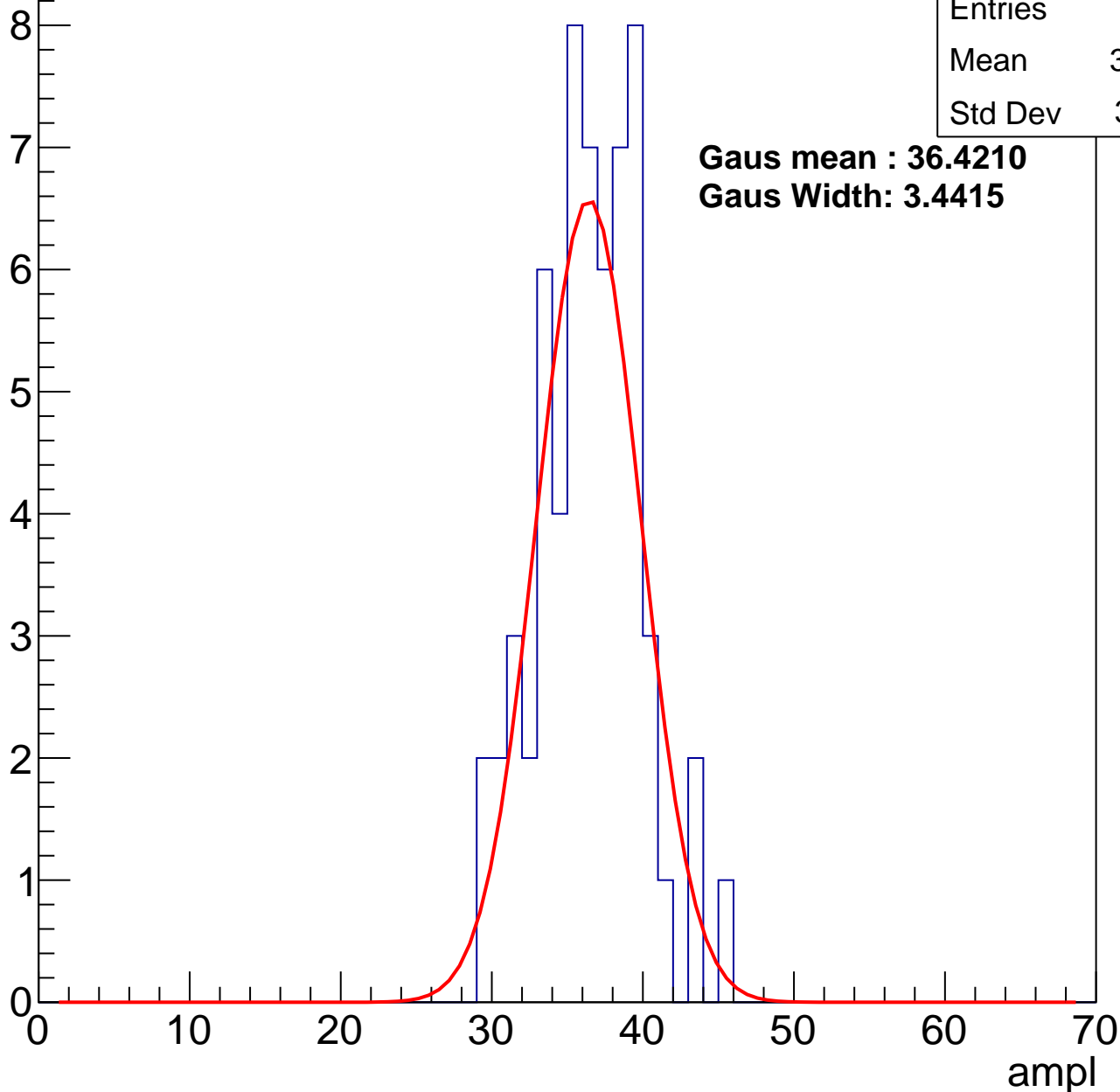
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	36.02
Std Dev	3.391

**Gaus mean : 36.4210**

**Gaus Width: 3.4415**



# B1L003S, U6-ch90, adc2

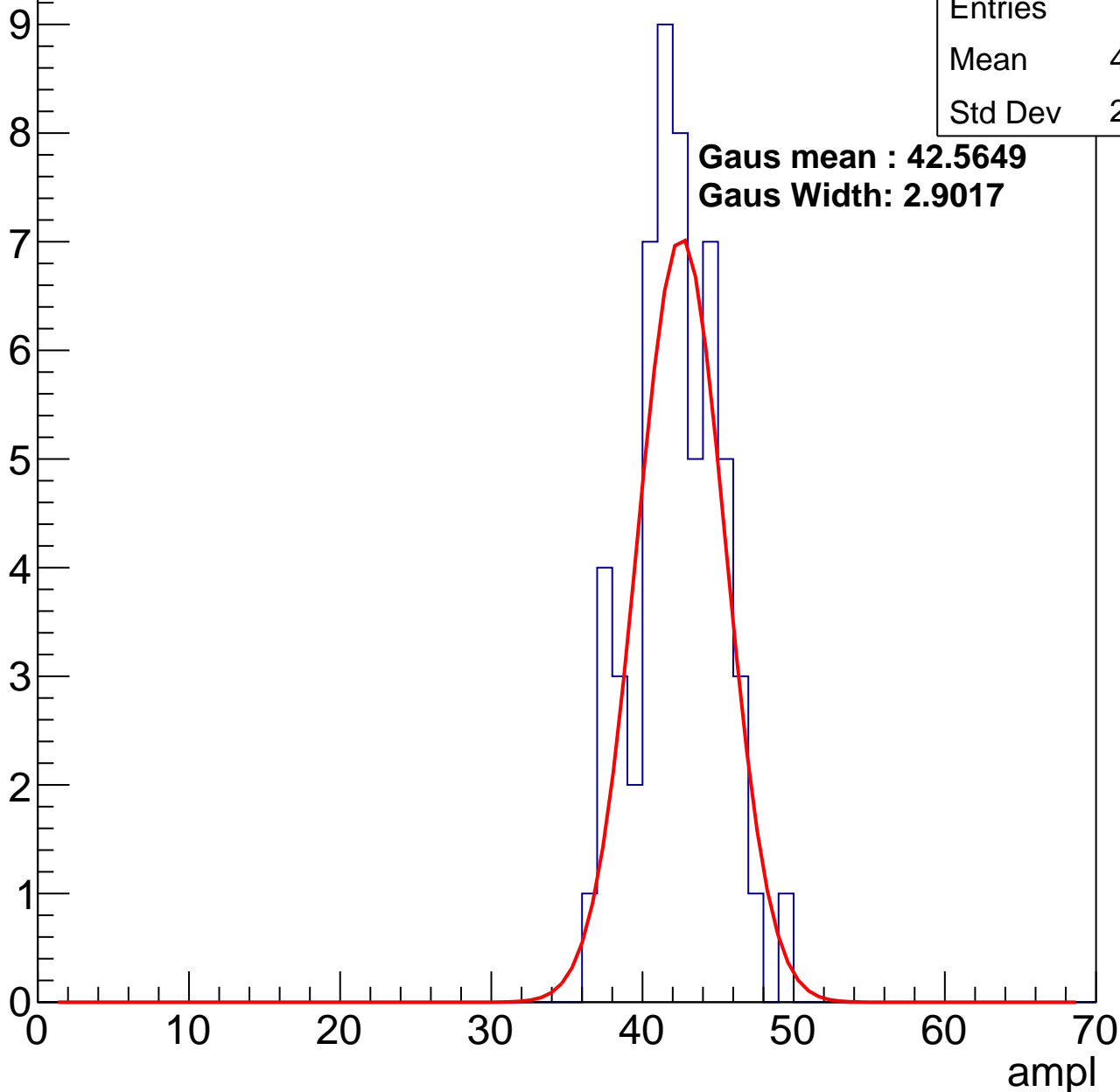
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	41.84
Std Dev	2.795

**Gaus mean : 42.5649**

**Gaus Width: 2.9017**

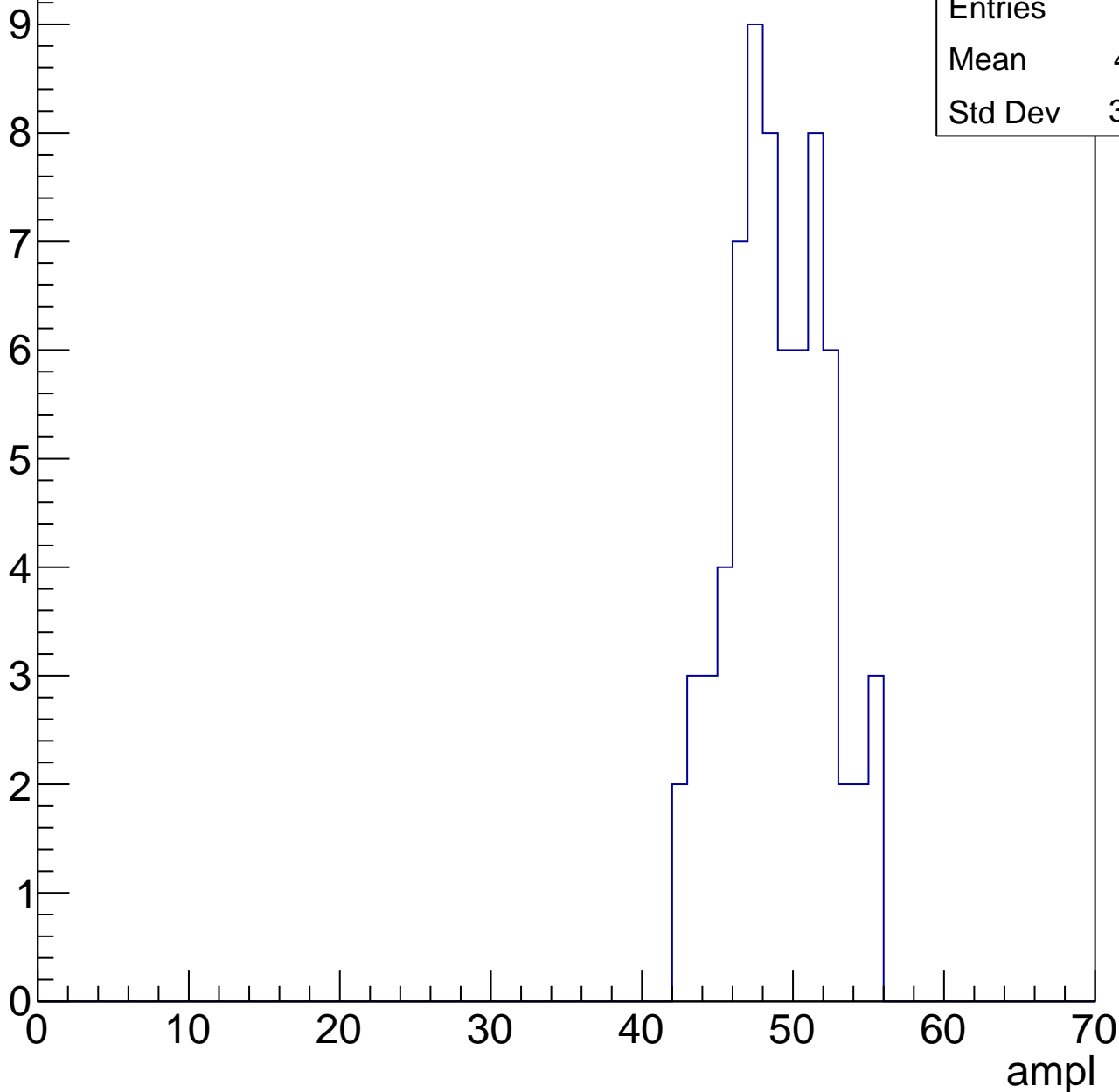


# B1L003S, U6-ch90, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	48.51
Std Dev	3.224

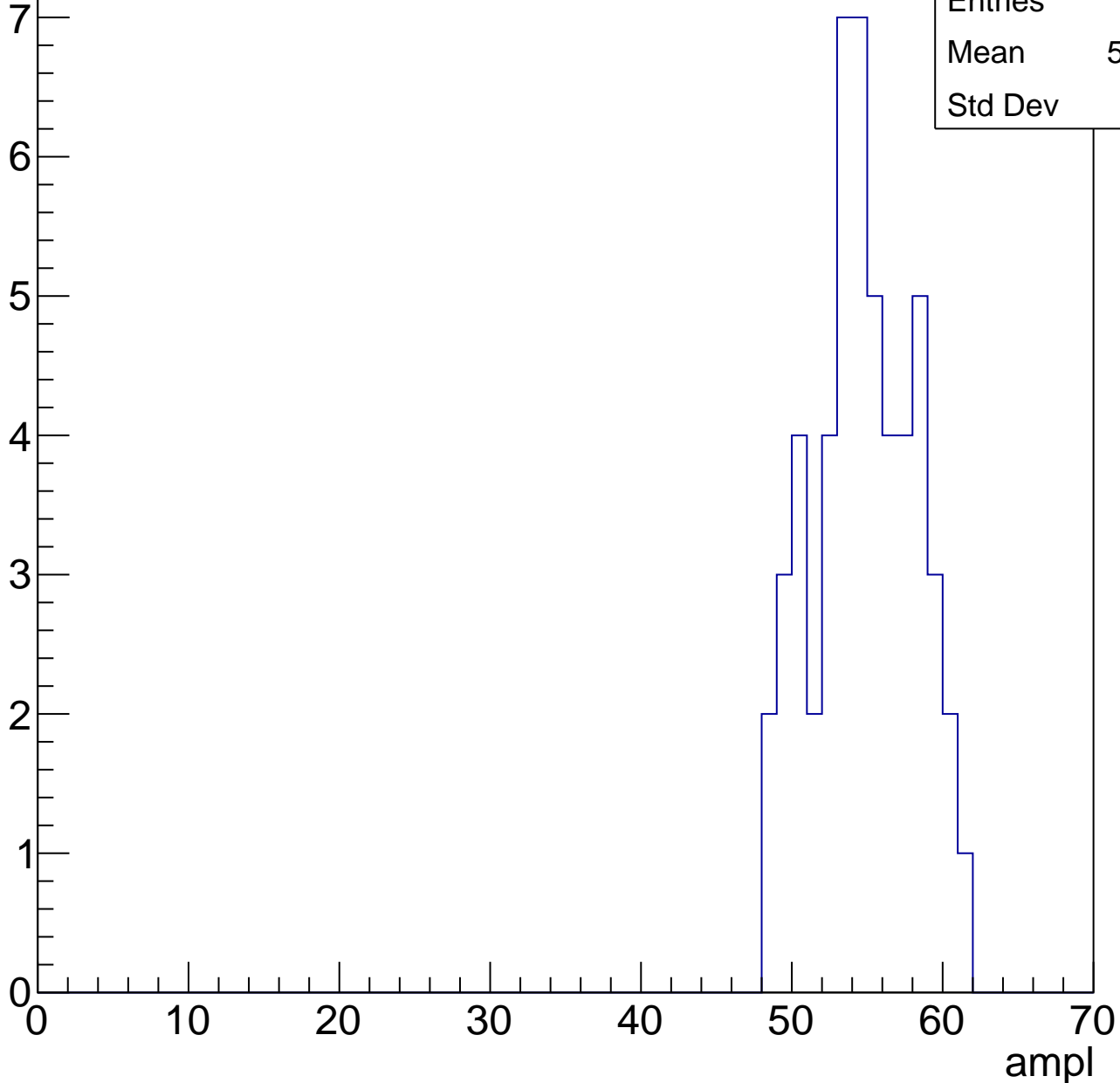


# B1L003S, U6-ch90, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	54.28
Std Dev	3.31



# B1L003S, U6-ch90, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

7

6

5

4

3

2

1

0

Entries

52

Mean

59.08

Std Dev

2.586

0

0

10

20

30

40

50

60

70

ampl

0

1

2

3

4

5

6

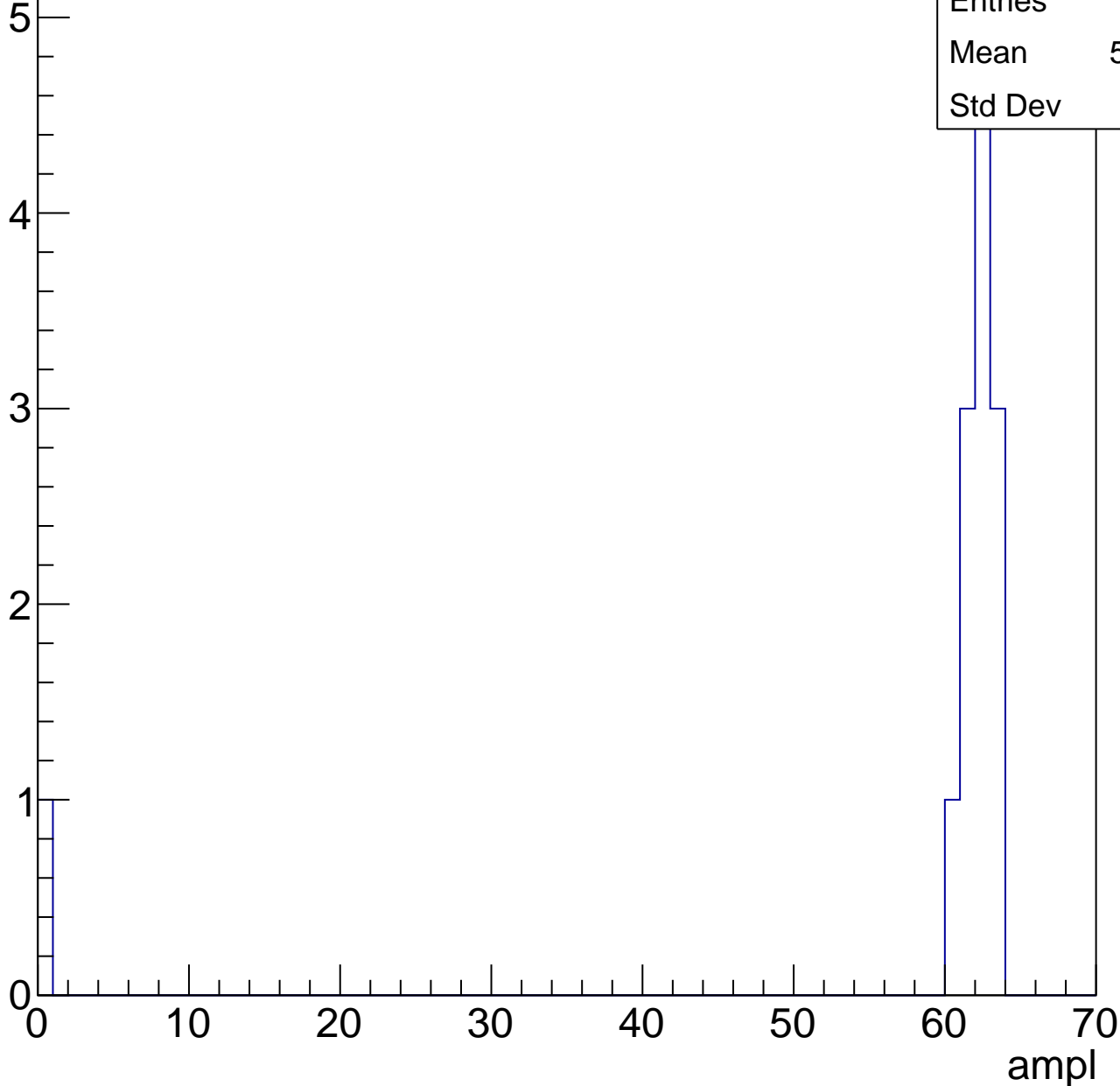
7

# B1L003S, U6-ch90, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	13
Mean	57.08
Std Dev	16.5





# B1L003S, U6-ch90, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch91, adc0

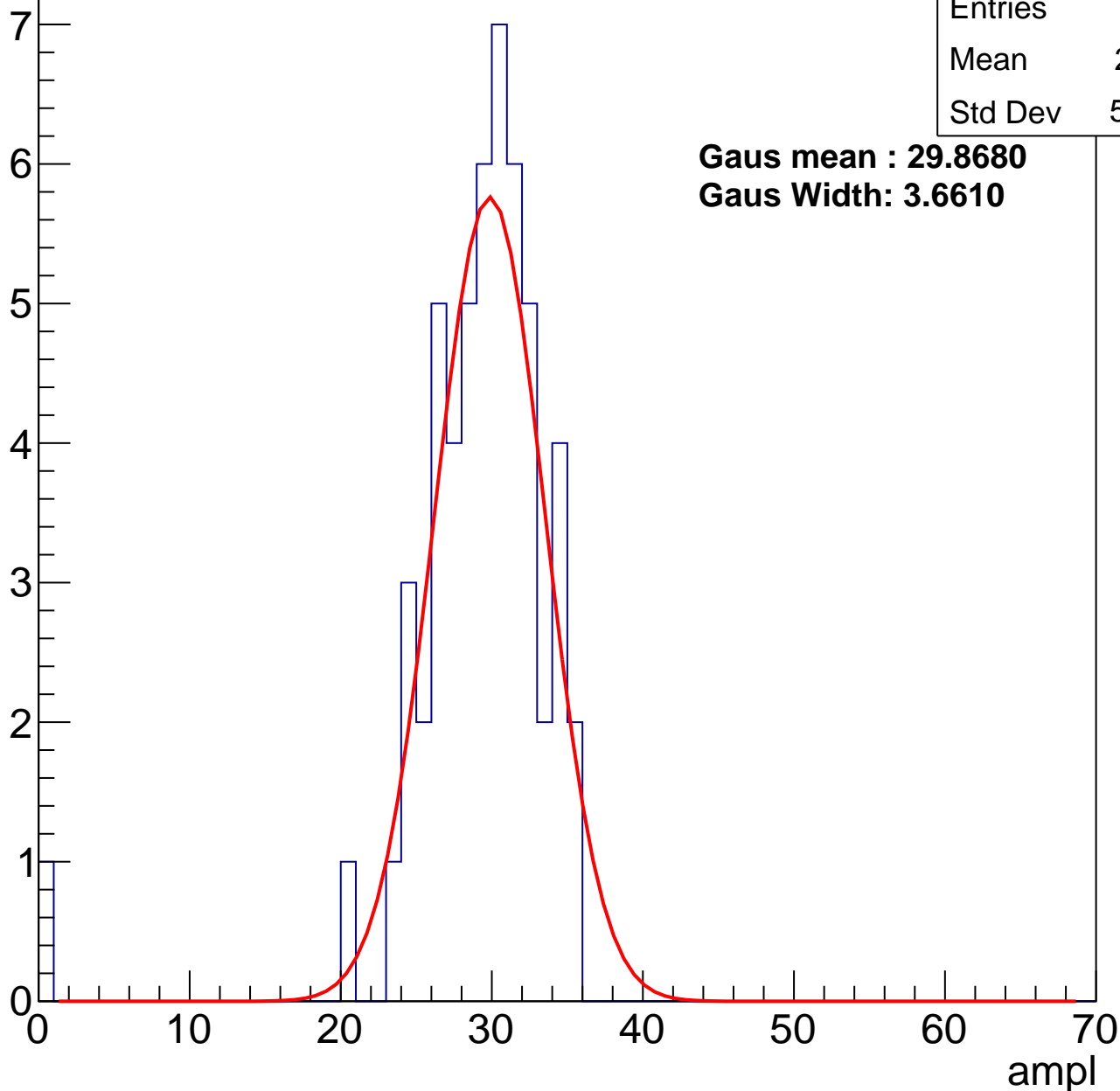
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	54
Mean	28.61
Std Dev	5.097

**Gaus mean : 29.8680**

**Gaus Width: 3.6610**



# B1L003S, U6-ch91, adc1

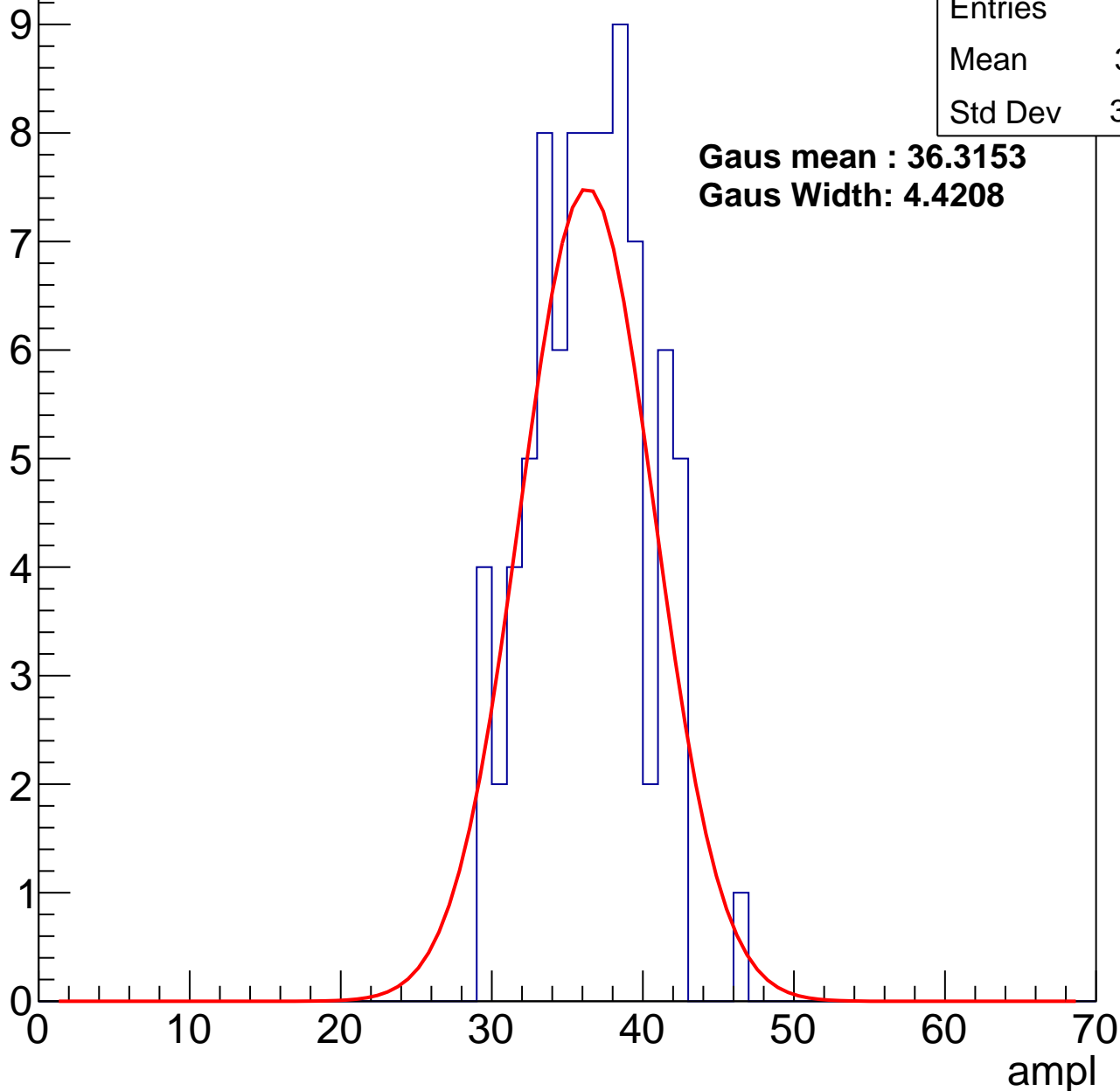
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	83
Mean	36.01
Std Dev	3.675

**Gaus mean : 36.3153**

**Gaus Width: 4.4208**



# B1L003S, U6-ch91, adc2

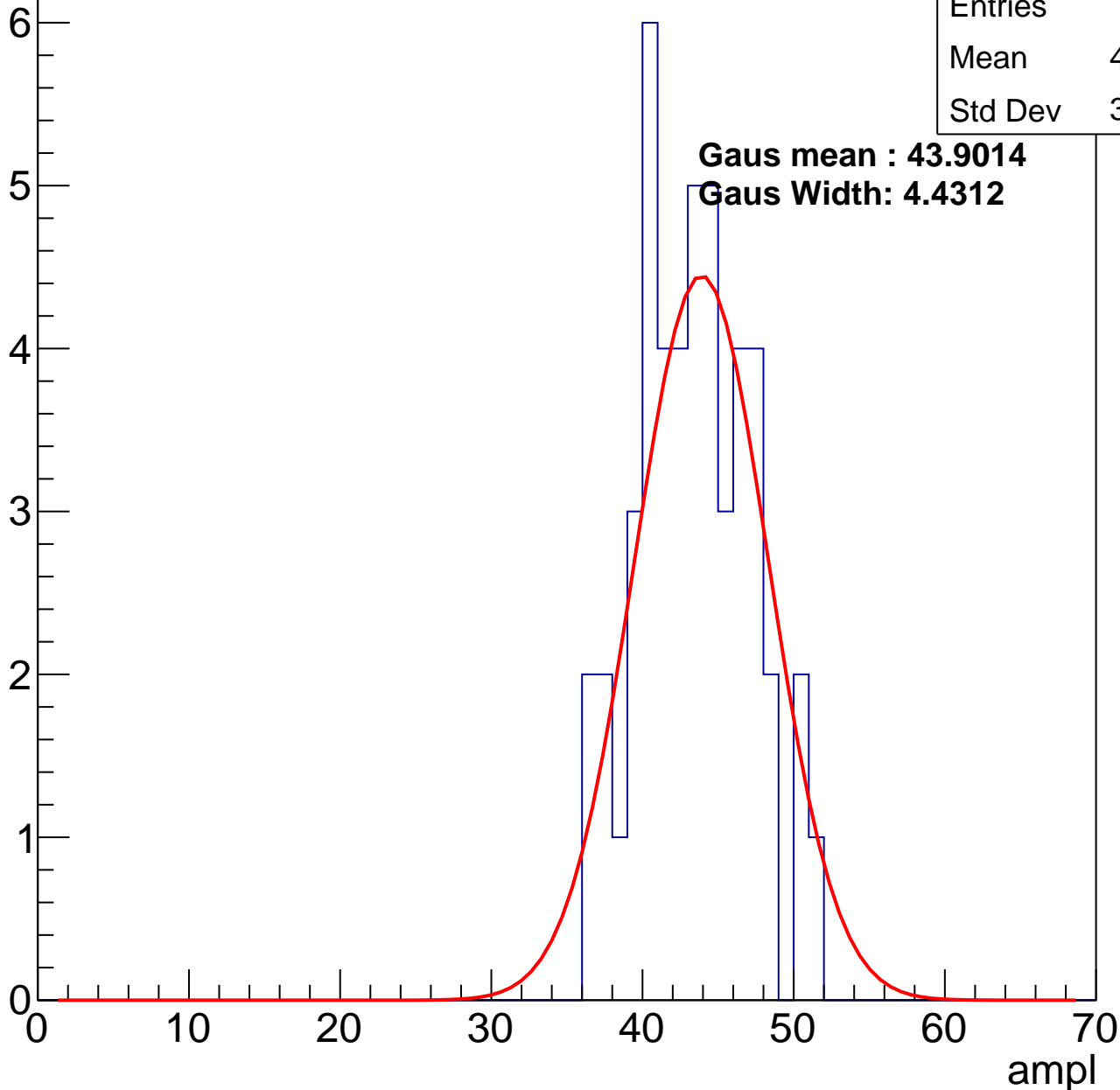
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	48
Mean	42.96
Std Dev	3.668

**Gaus mean : 43.9014**

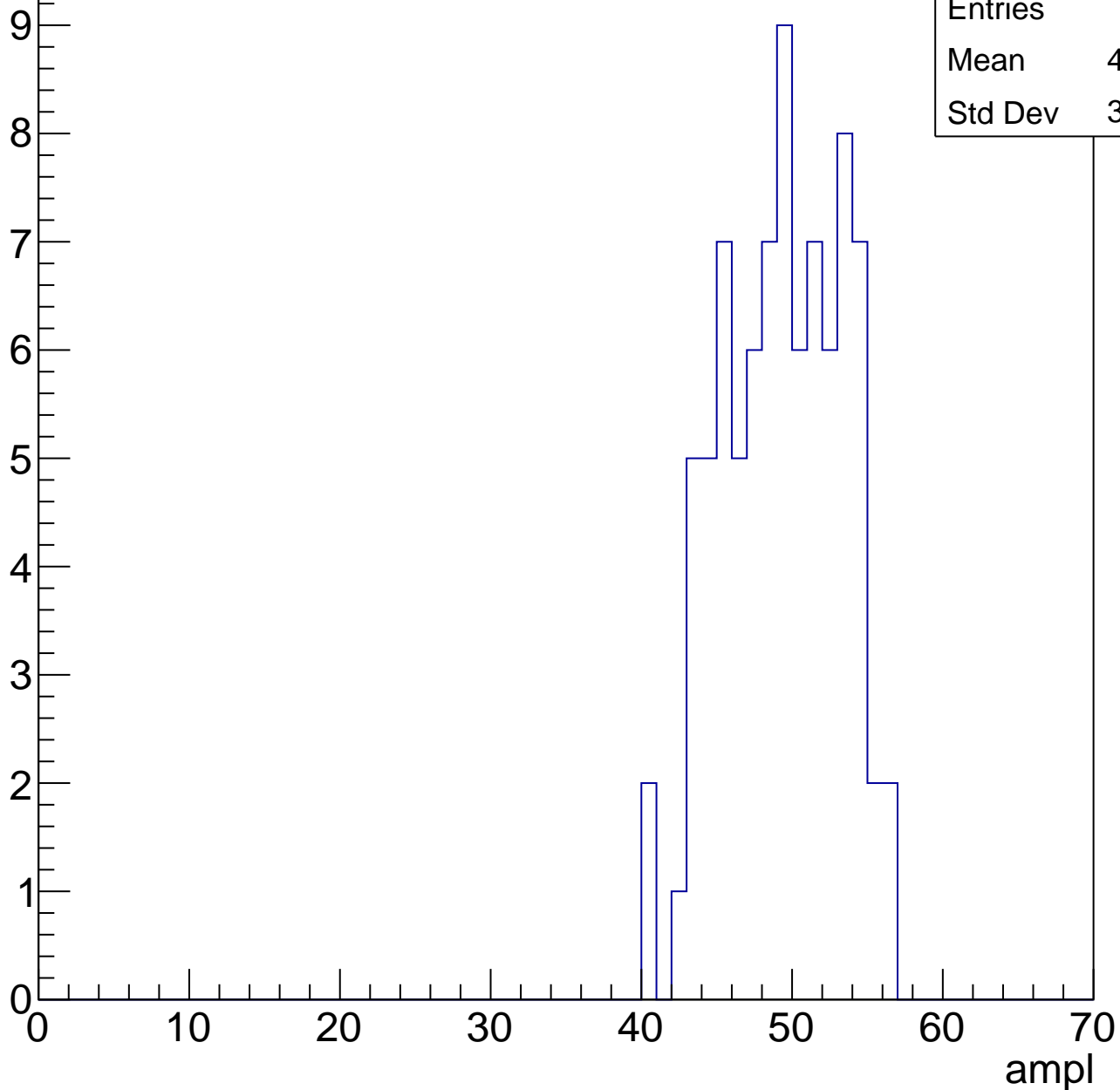
**Gaus Width: 4.4312**



# B1L003S, U6-ch91, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



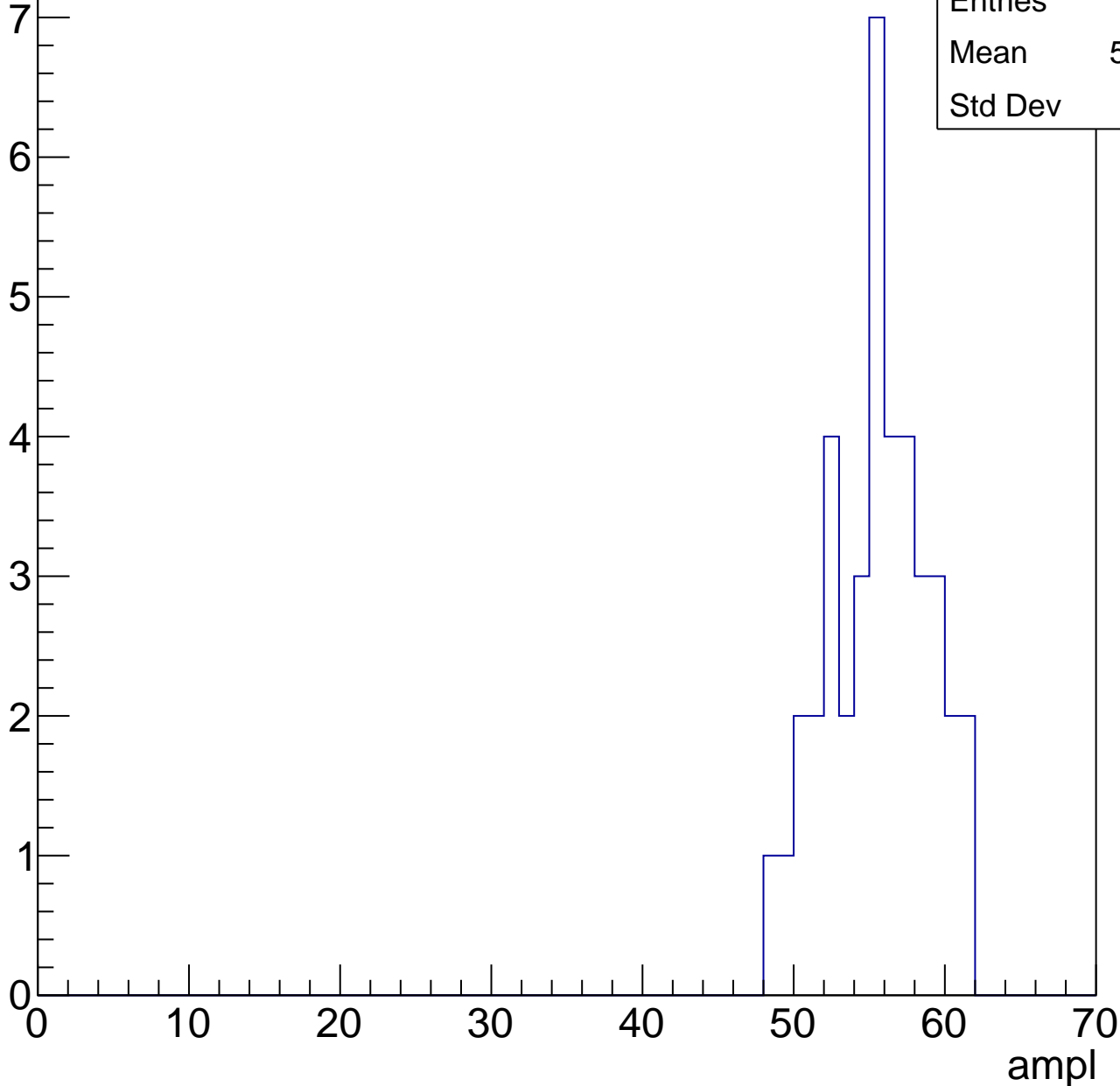
Entries	85
Mean	48.87
Std Dev	3.856

# B1L003S, U6-ch91, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	40
Mean	55.12
Std Dev	3.28

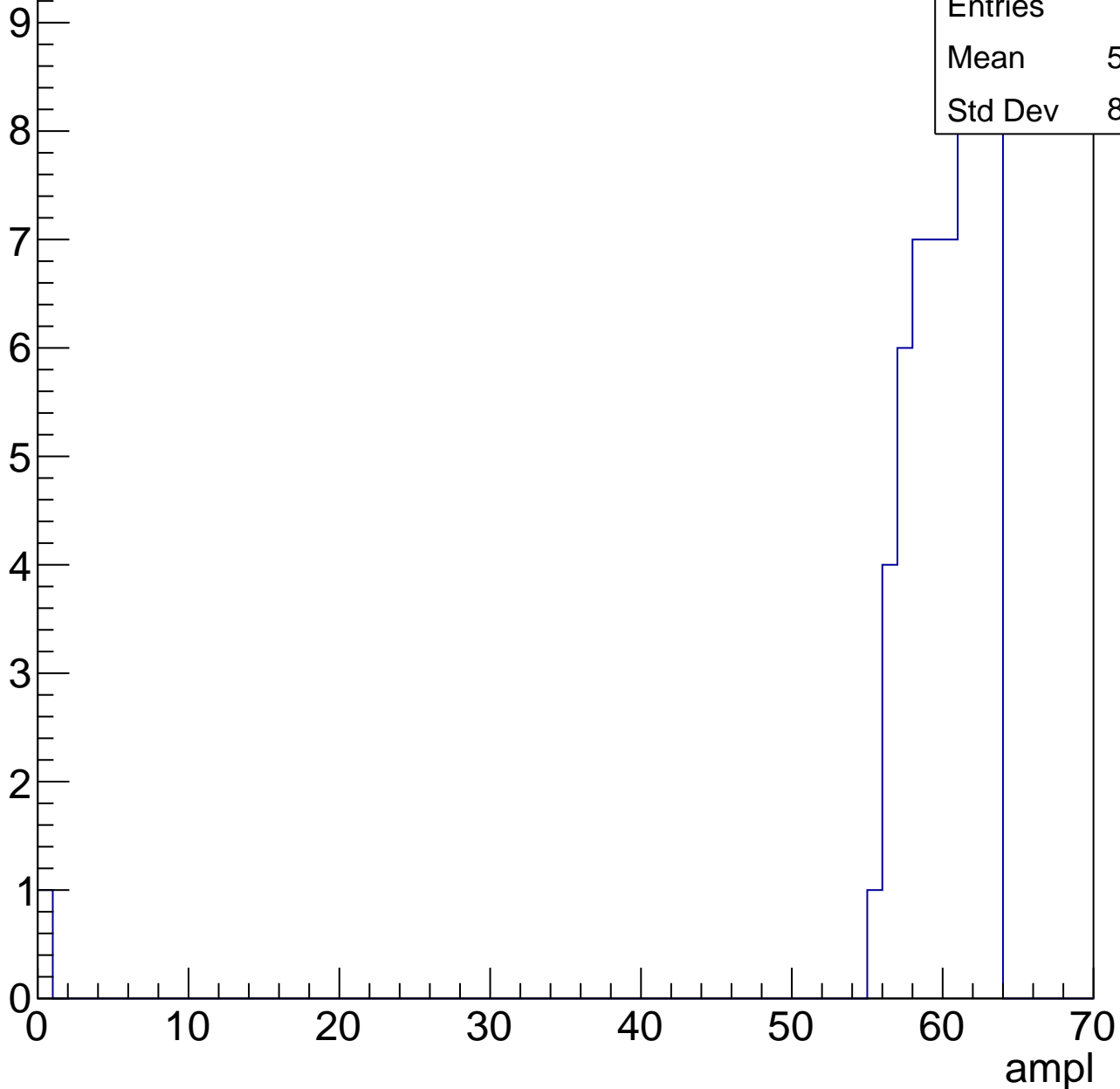


# B1L003S, U6-ch91, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	58.79
Std Dev	8.104



# B1L003S, U6-ch91, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch91, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U6-ch92, adc0

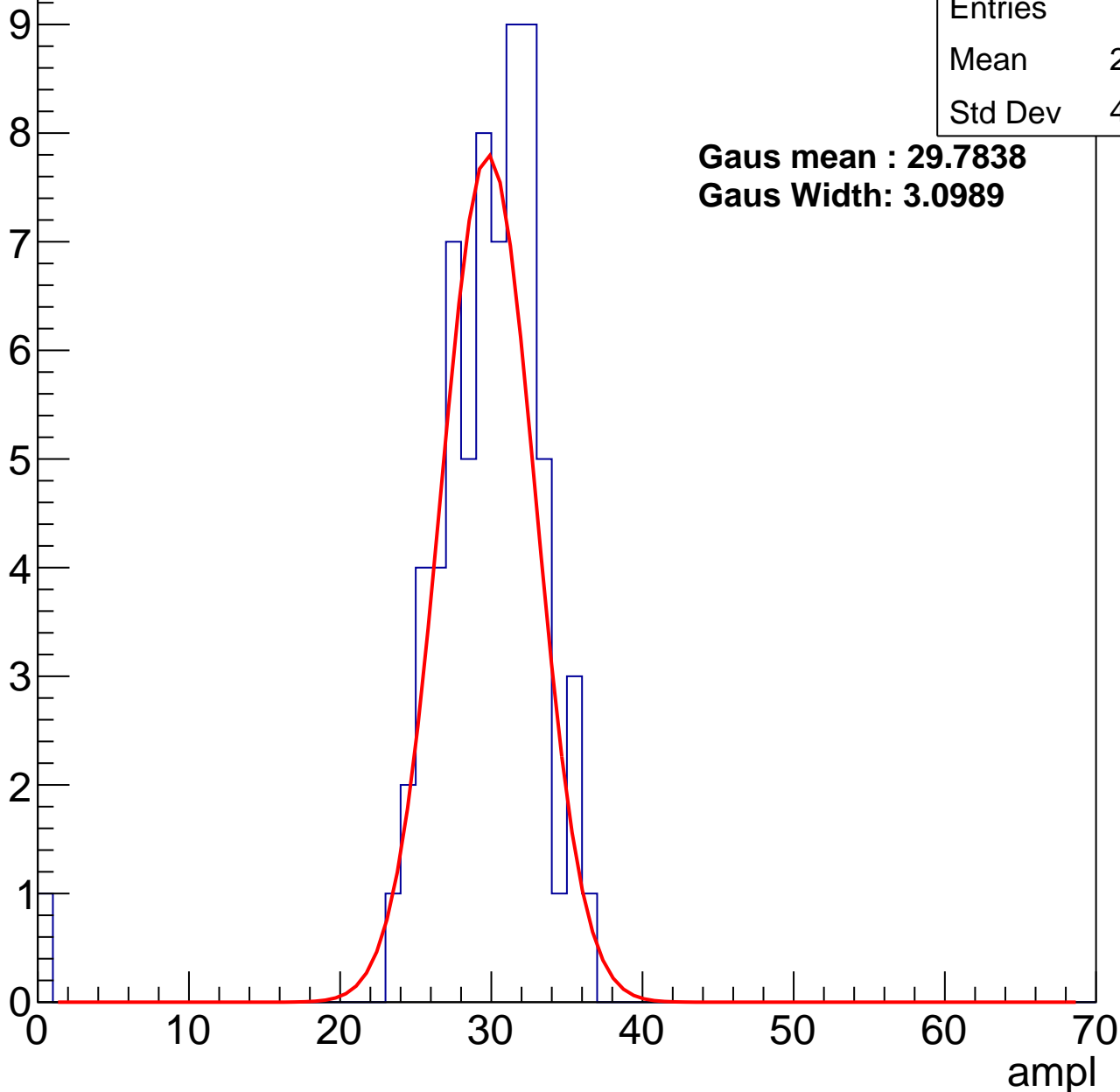
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	29.15
Std Dev	4.643

**Gaus mean : 29.7838**

**Gaus Width: 3.0989**



# B1L003S, U6-ch92, adc1

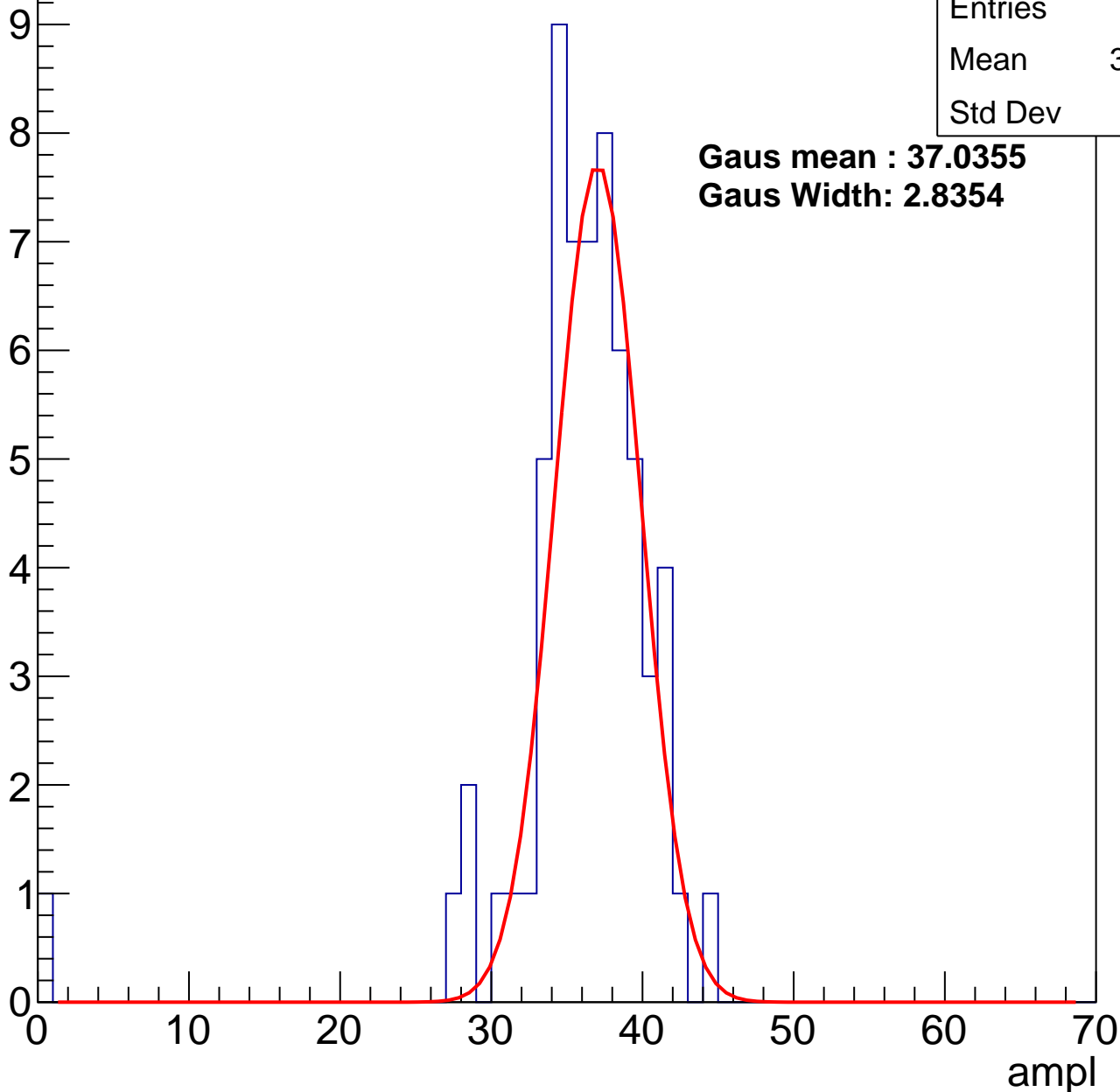
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	35.44
Std Dev	5.6

**Gaus mean : 37.0355**

**Gaus Width: 2.8354**



# B1L003S, U6-ch92, adc2

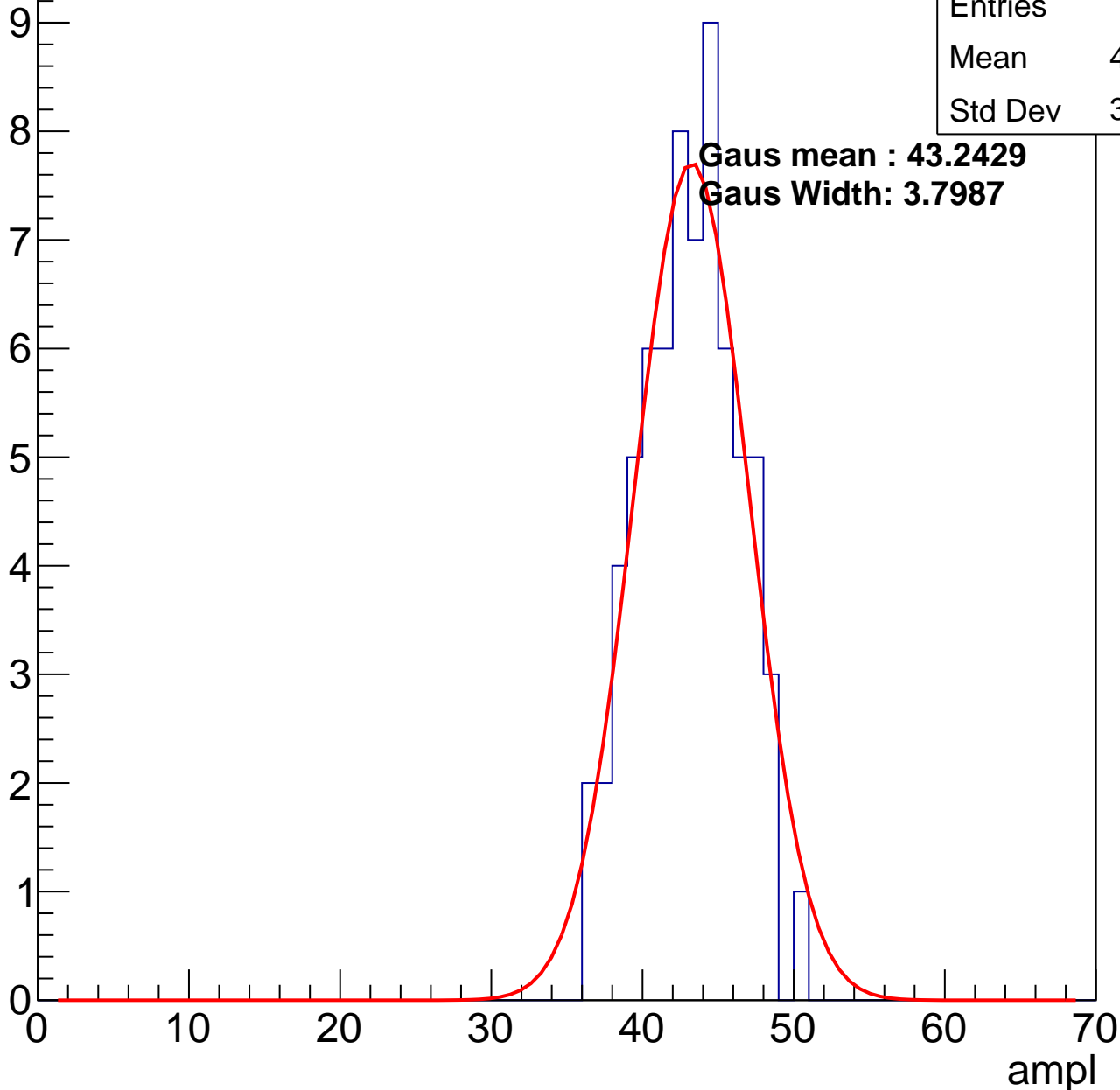
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	42.62
Std Dev	3.204

**Gaus mean : 43.2429**

**Gaus Width: 3.7987**

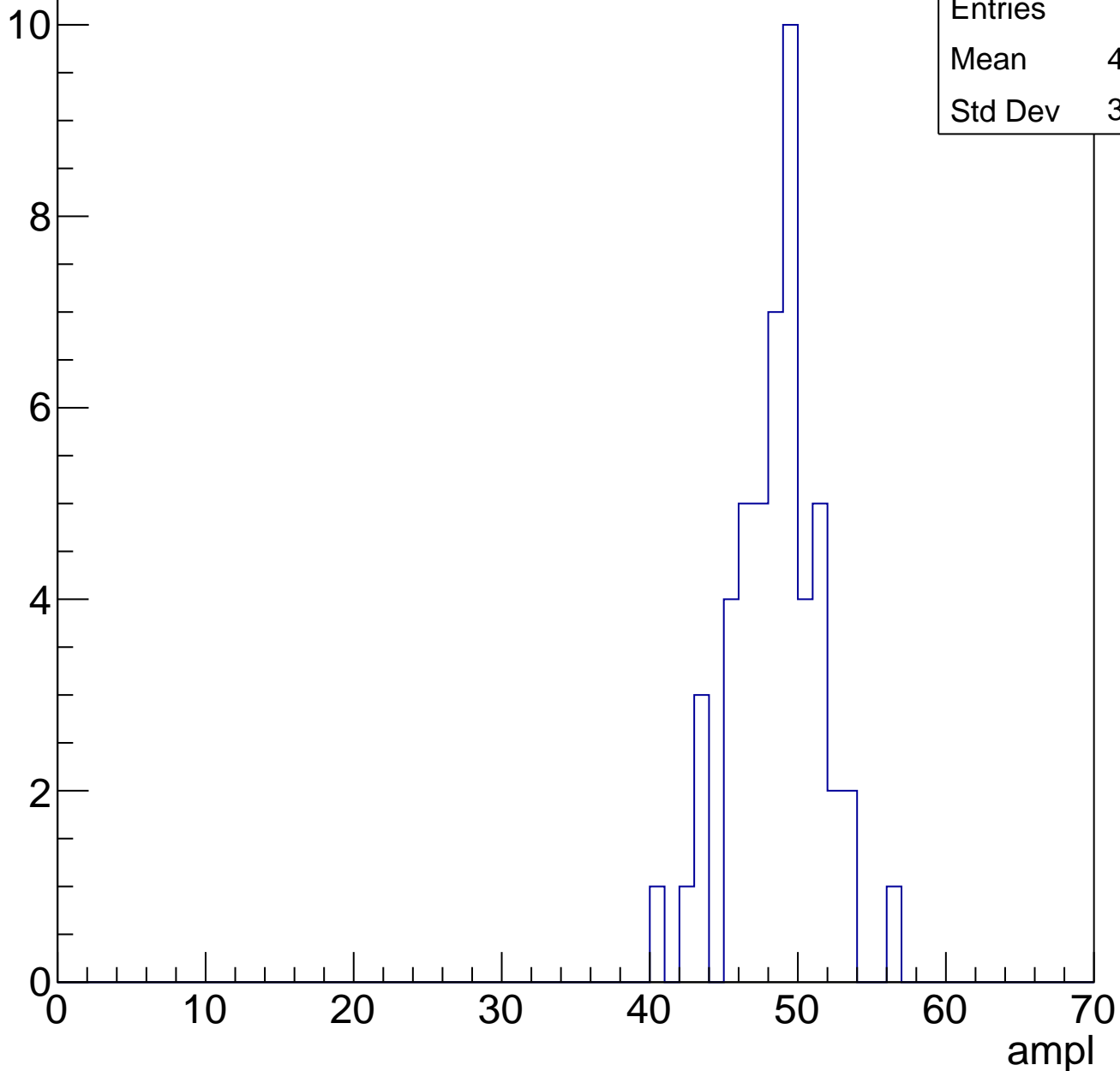


# B1L003S, U6-ch92, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	50
Mean	48.06
Std Dev	3.009

Entry

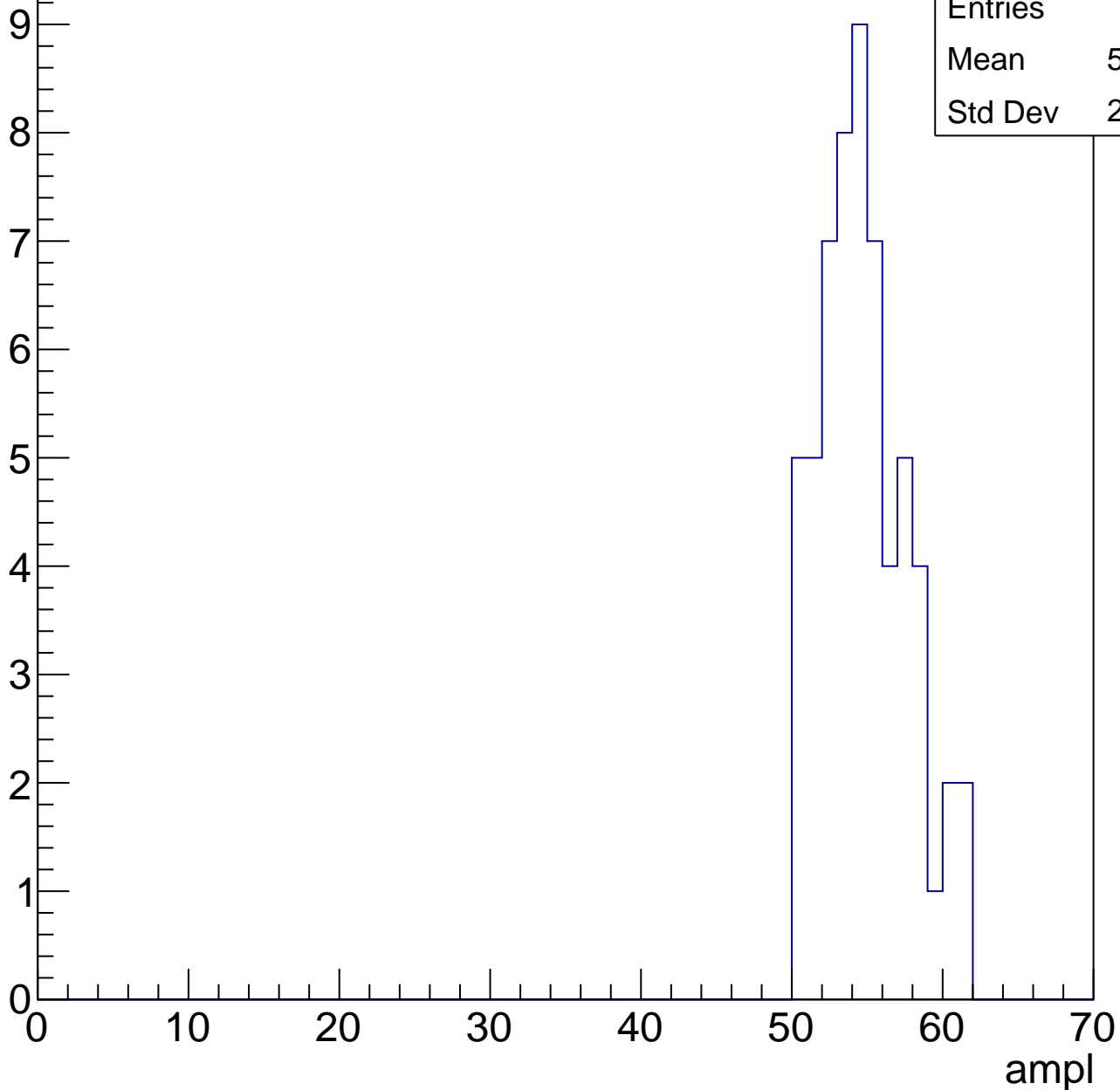


# B1L003S, U6-ch92, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	54.34
Std Dev	2.856

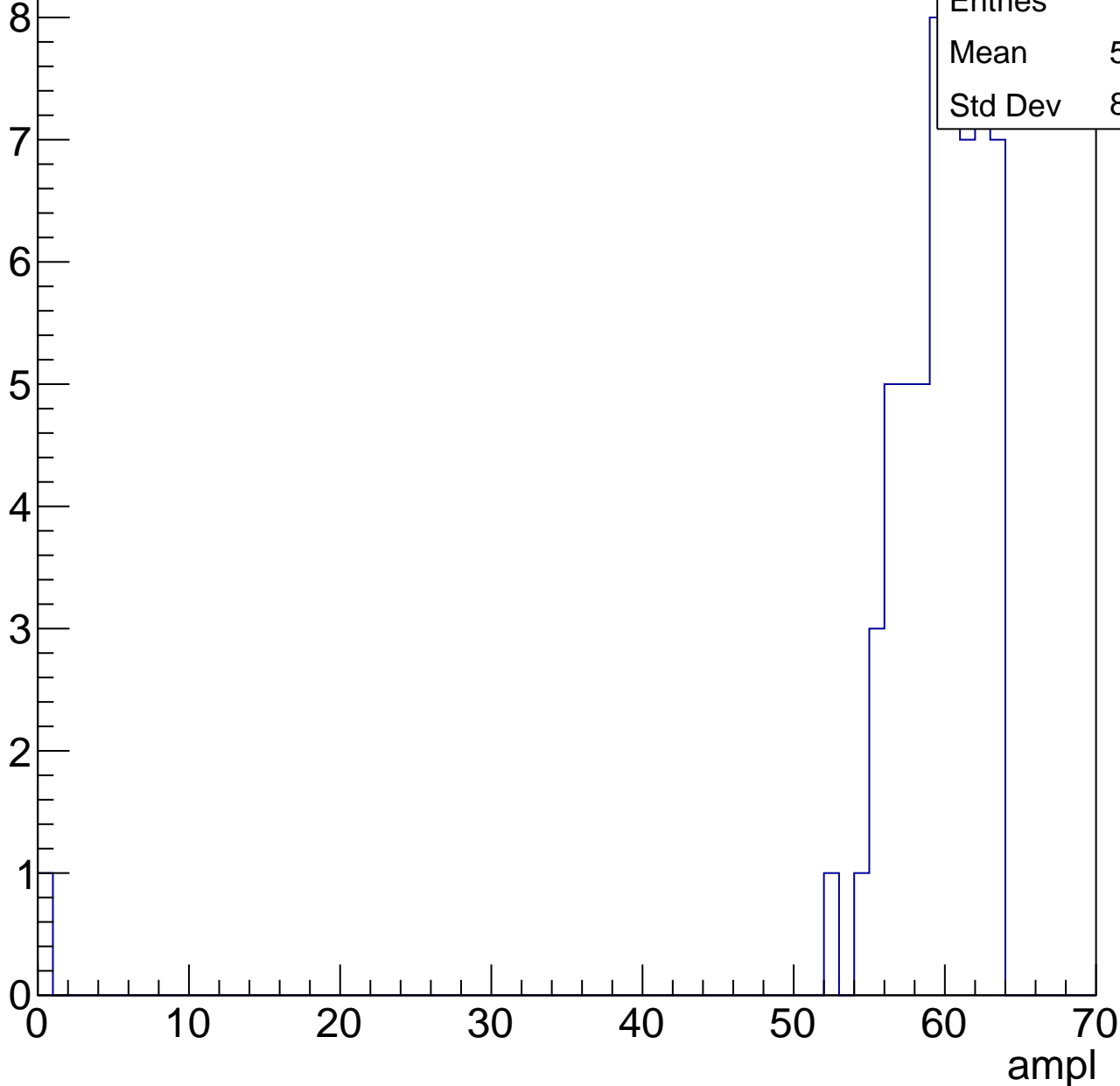


# B1L003S, U6-ch92, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	58.34
Std Dev	8.096



# B1L003S, U6-ch92, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries

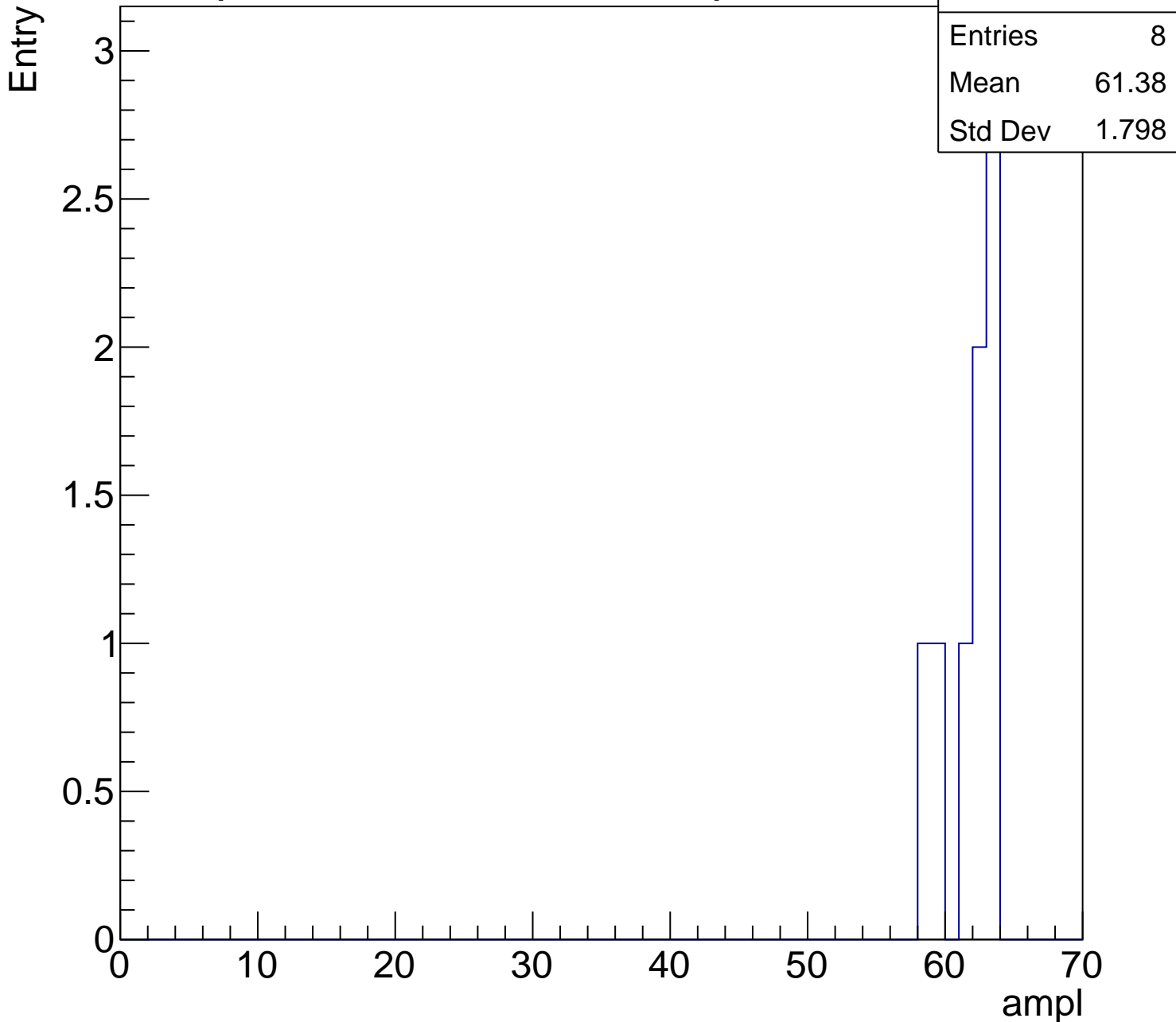
8

Mean

61.38

Std Dev

1.798





# B1L003S, U6-ch92, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U6-ch93, adc0

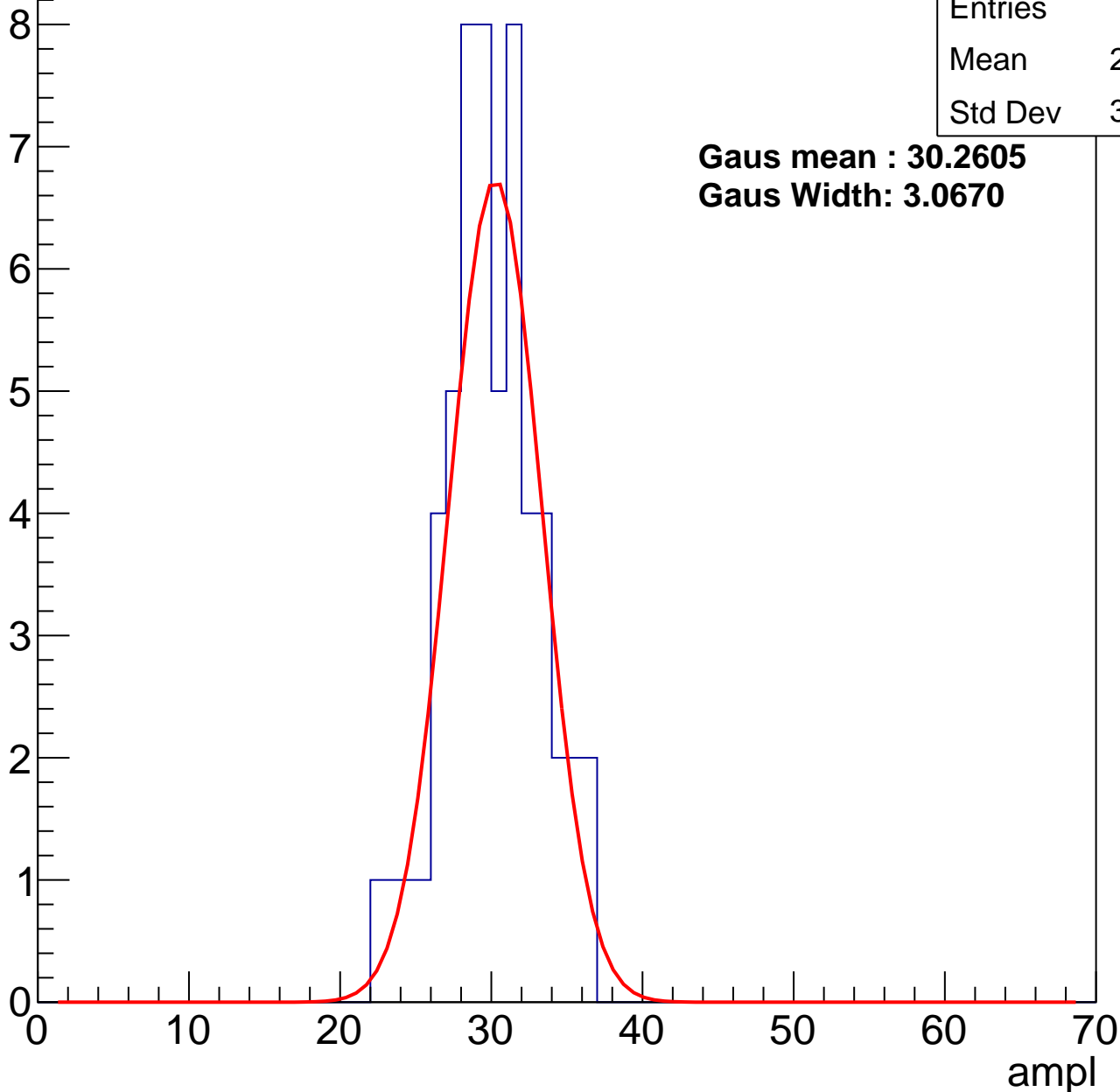
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	29.59
Std Dev	3.069

**Gaus mean : 30.2605**

**Gaus Width: 3.0670**



# B1L003S, U6-ch93, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	77
Mean	36.42
Std Dev	3.648

**Gaus mean : 36.9954**

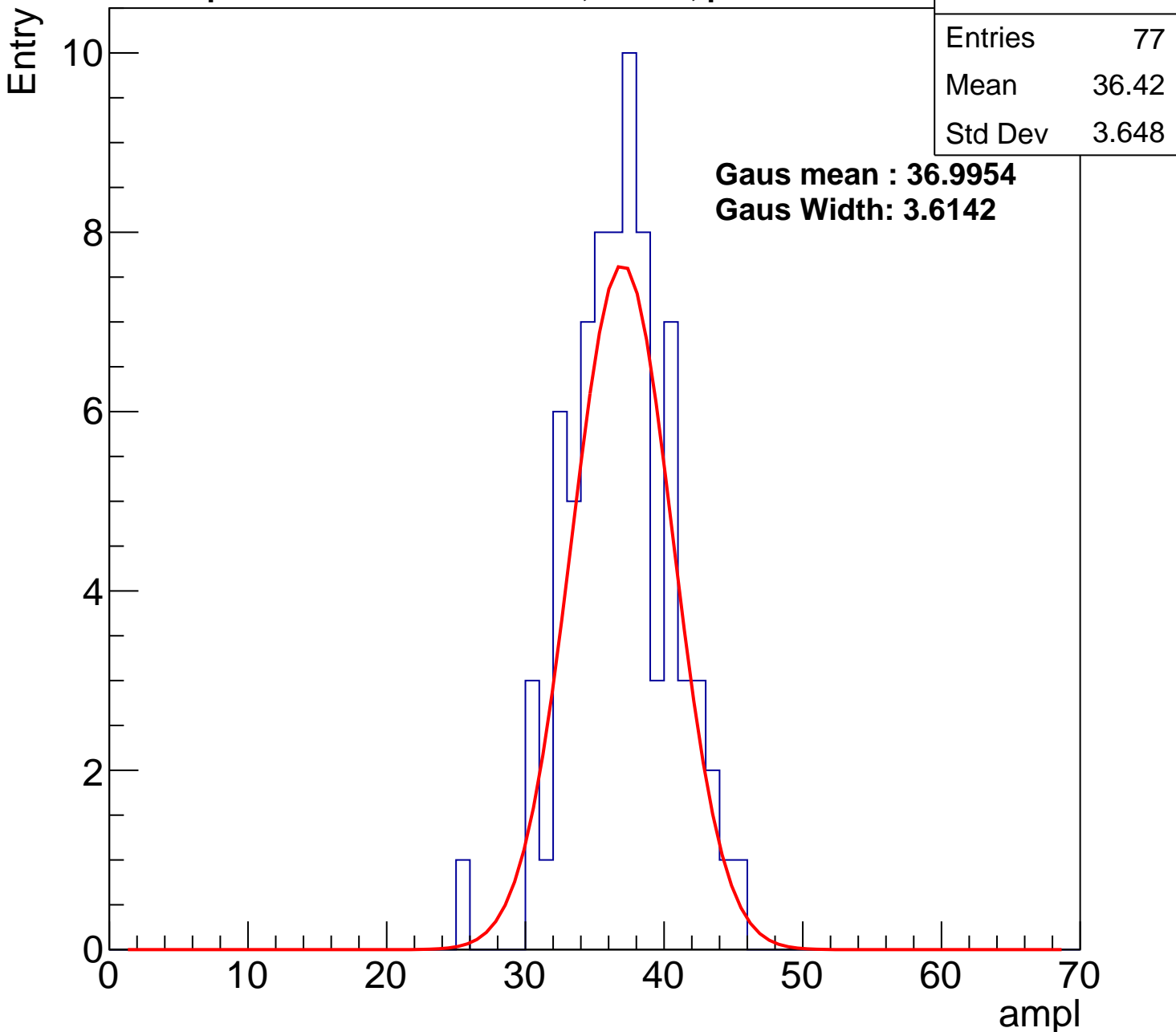
**Gaus Width: 3.6142**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L003S, U6-ch93, adc2

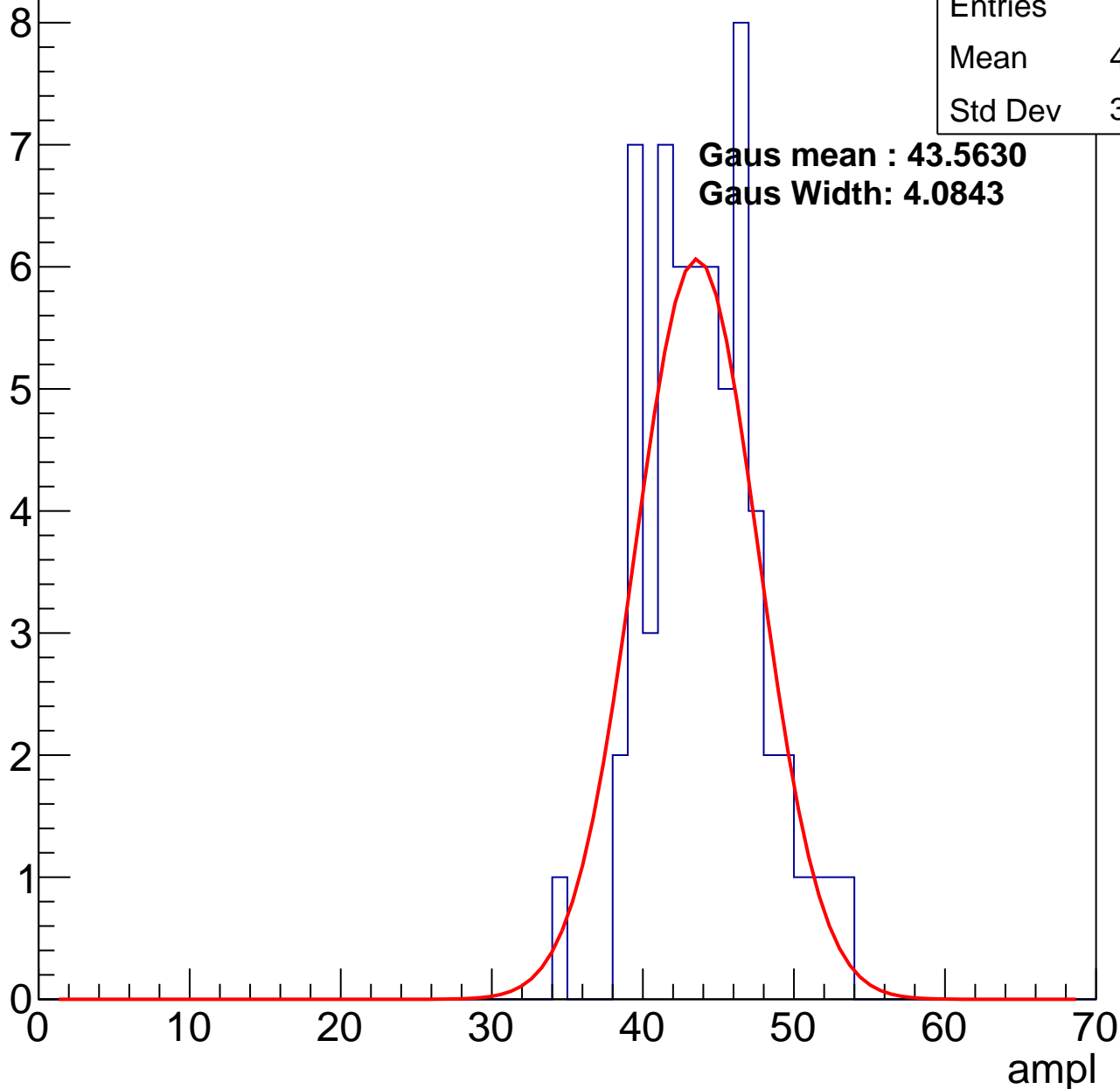
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	43.57
Std Dev	3.698

**Gaus mean : 43.5630**

**Gaus Width: 4.0843**

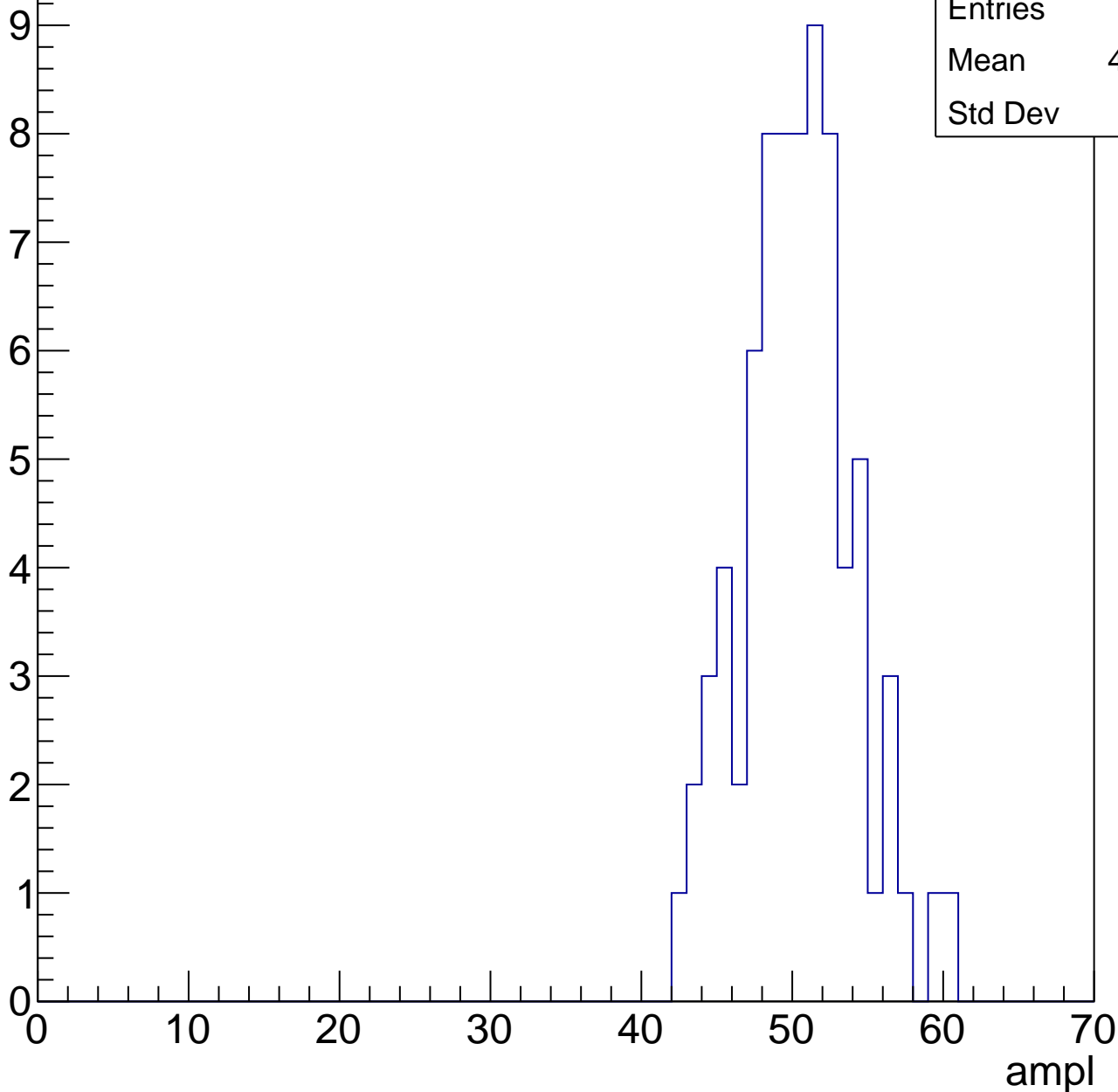


# B1L003S, U6-ch93, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	75
Mean	49.95
Std Dev	3.68

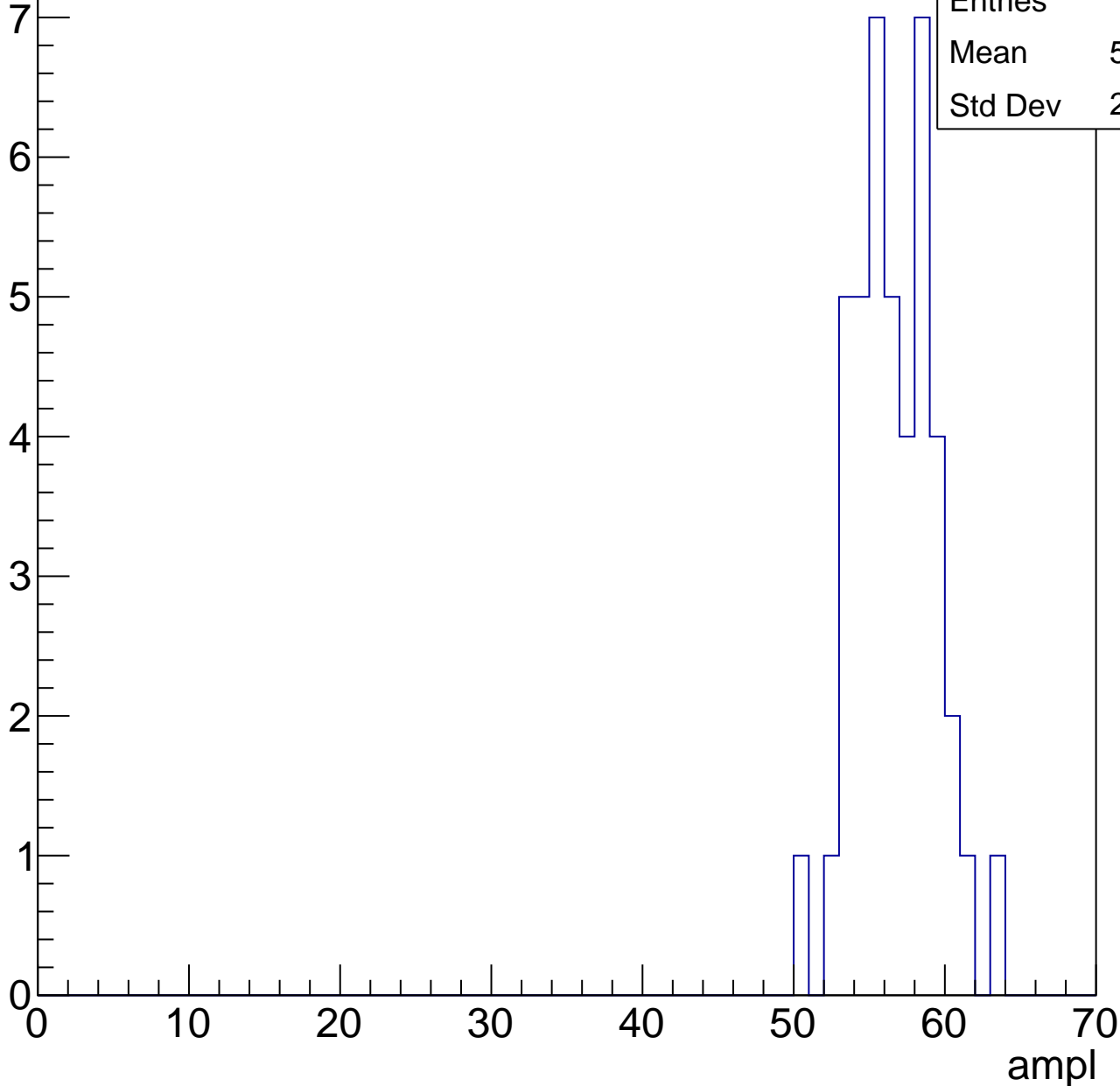


# B1L003S, U6-ch93, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	43
Mean	56.19
Std Dev	2.626

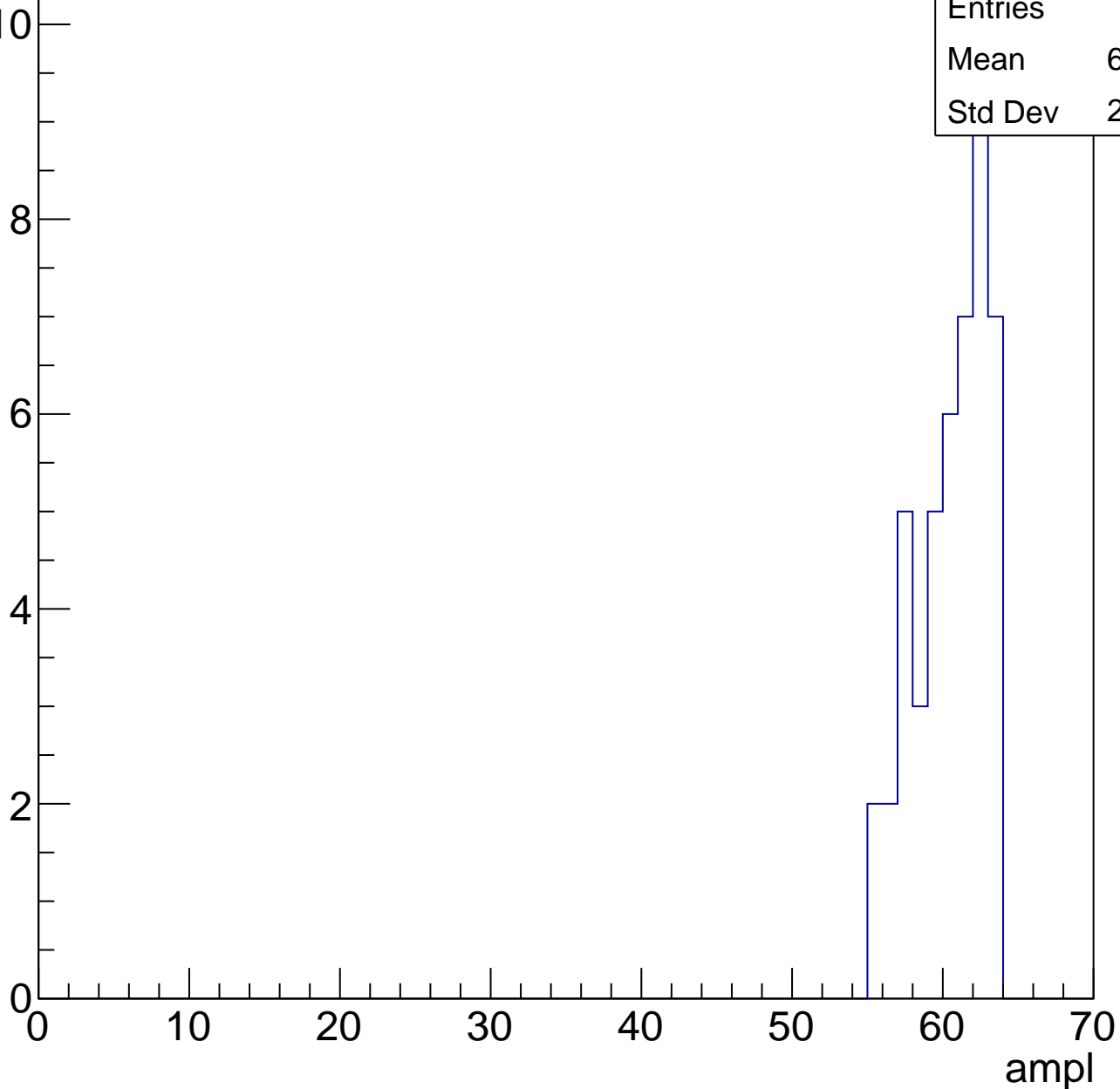


# B1L003S, U6-ch93, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	47
Mean	60.09
Std Dev	2.323



# B1L003S, U6-ch93, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

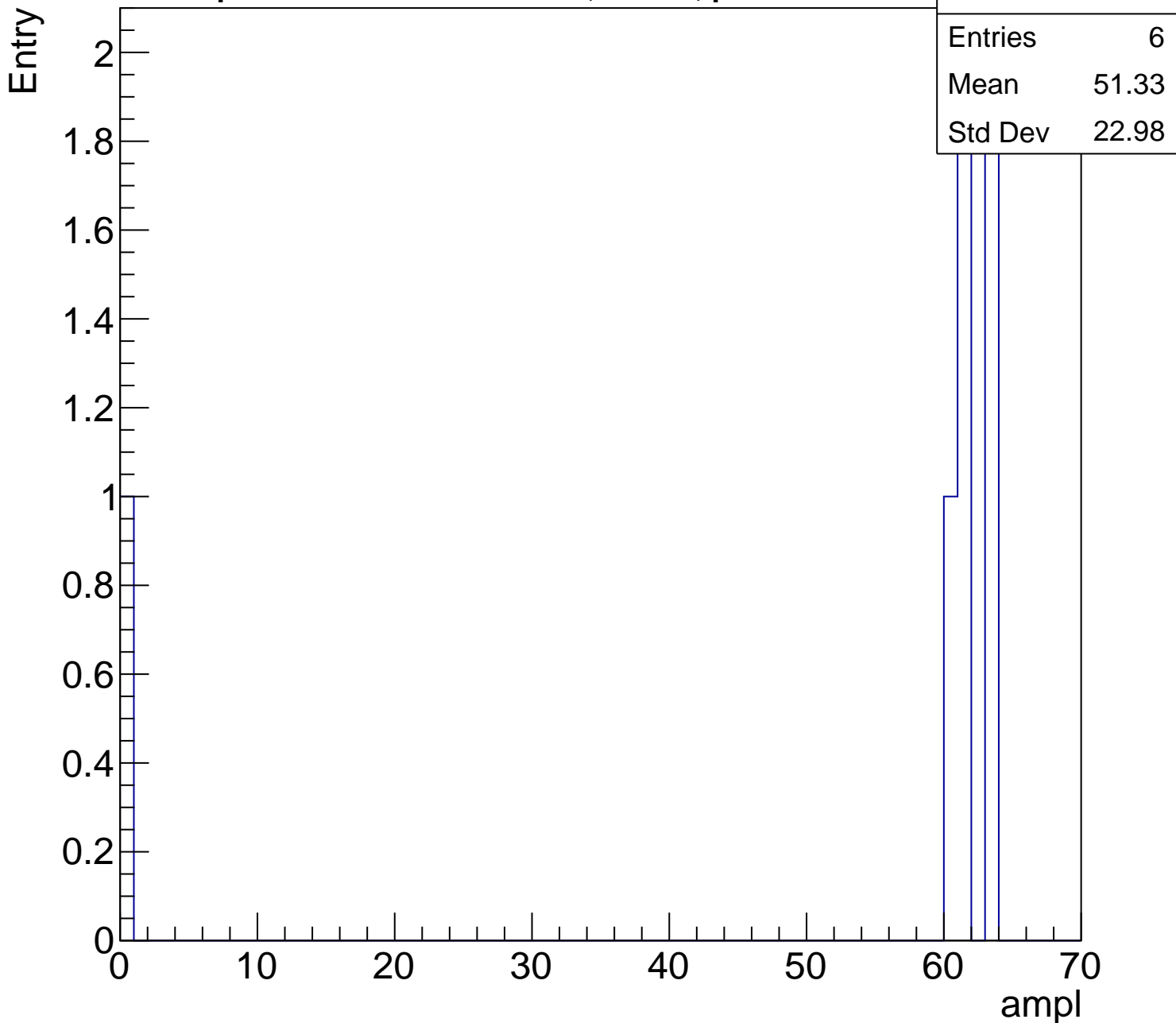
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	51.33
Std Dev	22.98

0 10 20 30 40 50 60 70

ampl





# B1L003S, U6-ch93, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U6-ch94, adc0

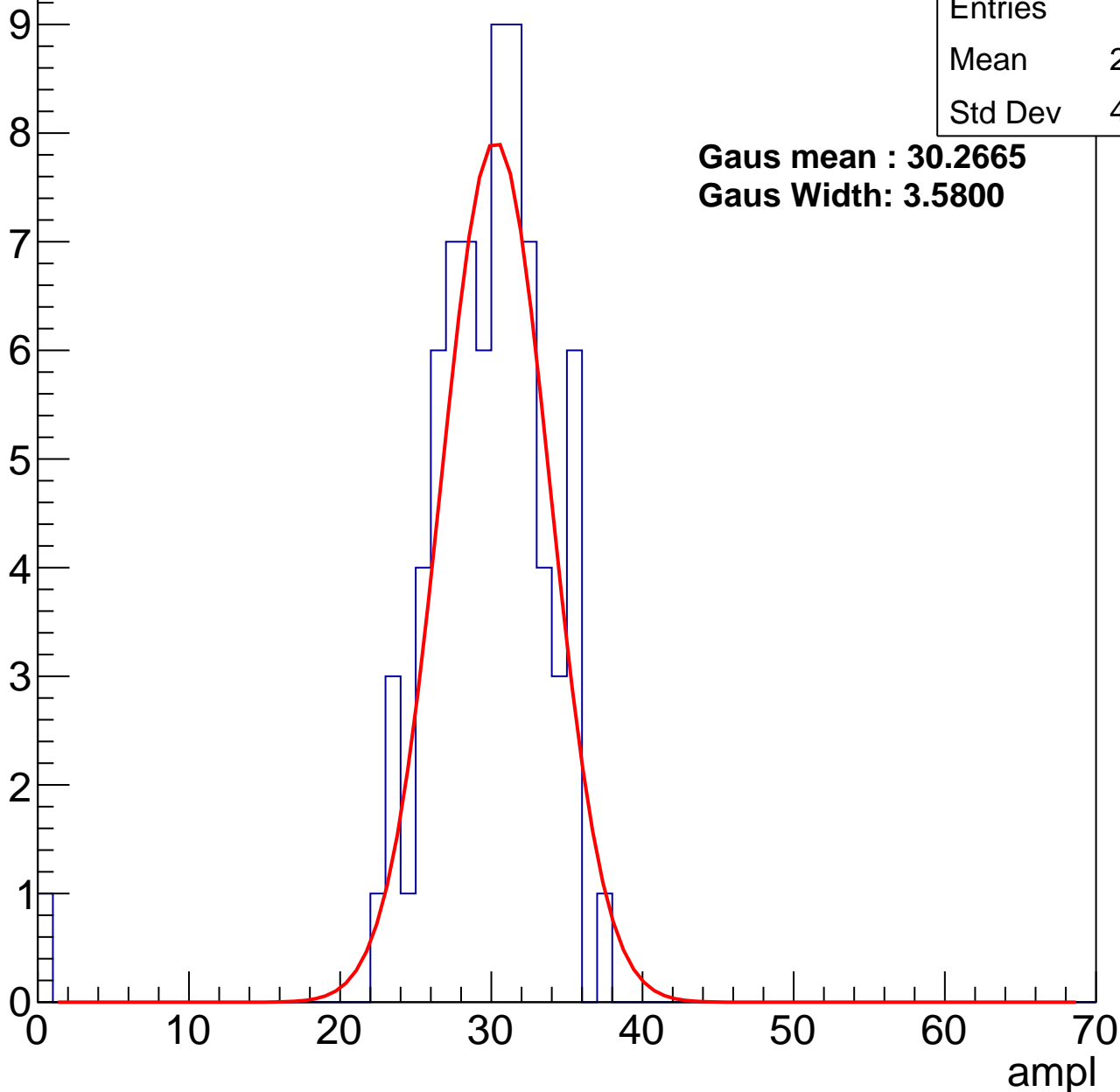
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	75
Mean	29.12
Std Dev	4.764

**Gaus mean : 30.2665**

**Gaus Width: 3.5800**



# B1L003S, U6-ch94, adc1

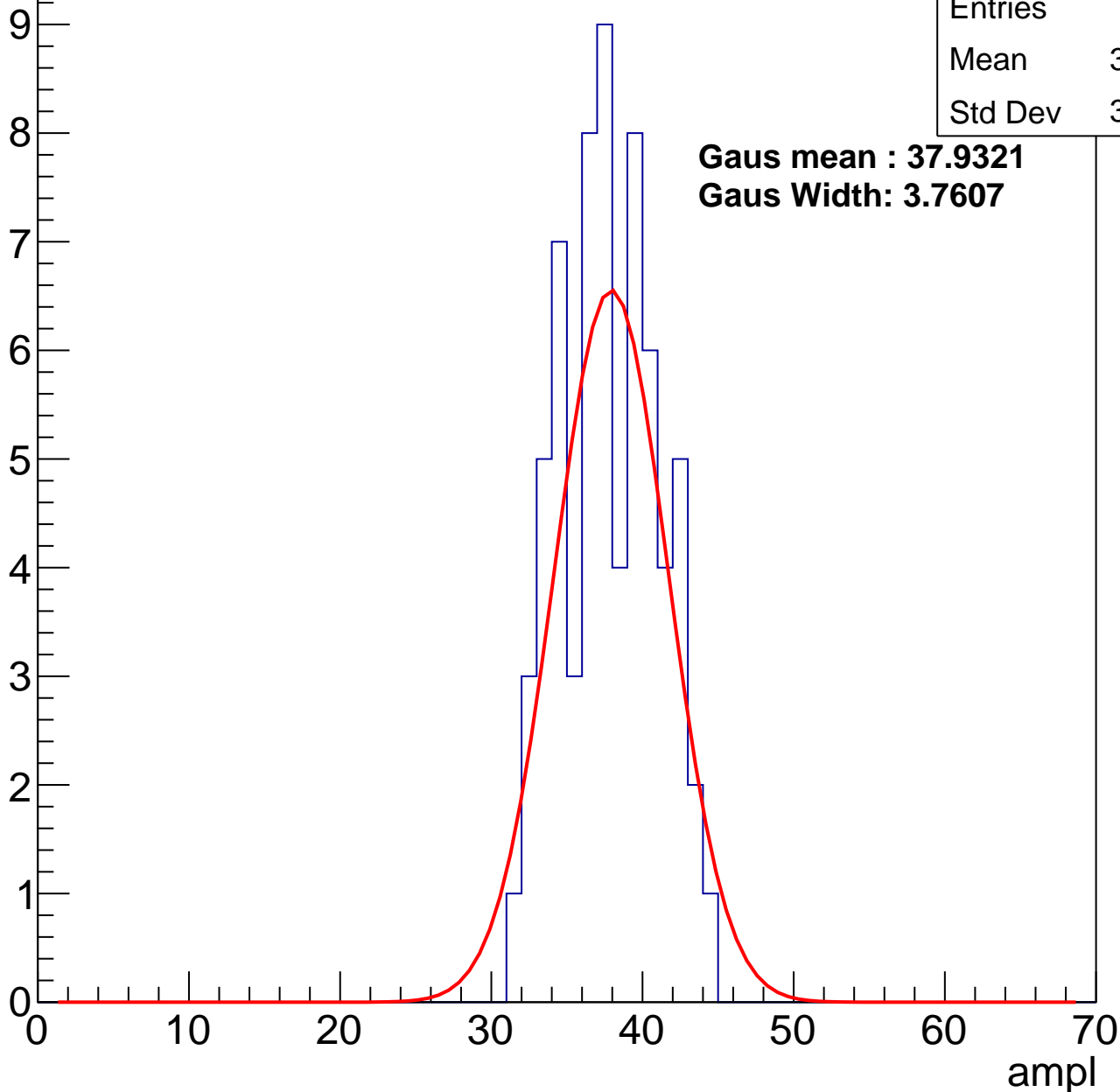
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	37.33
Std Dev	3.178

**Gaus mean : 37.9321**

**Gaus Width: 3.7607**



# B1L003S, U6-ch94, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	76
Mean	43.88
Std Dev	3.801

**Gaus mean : 44.6156**

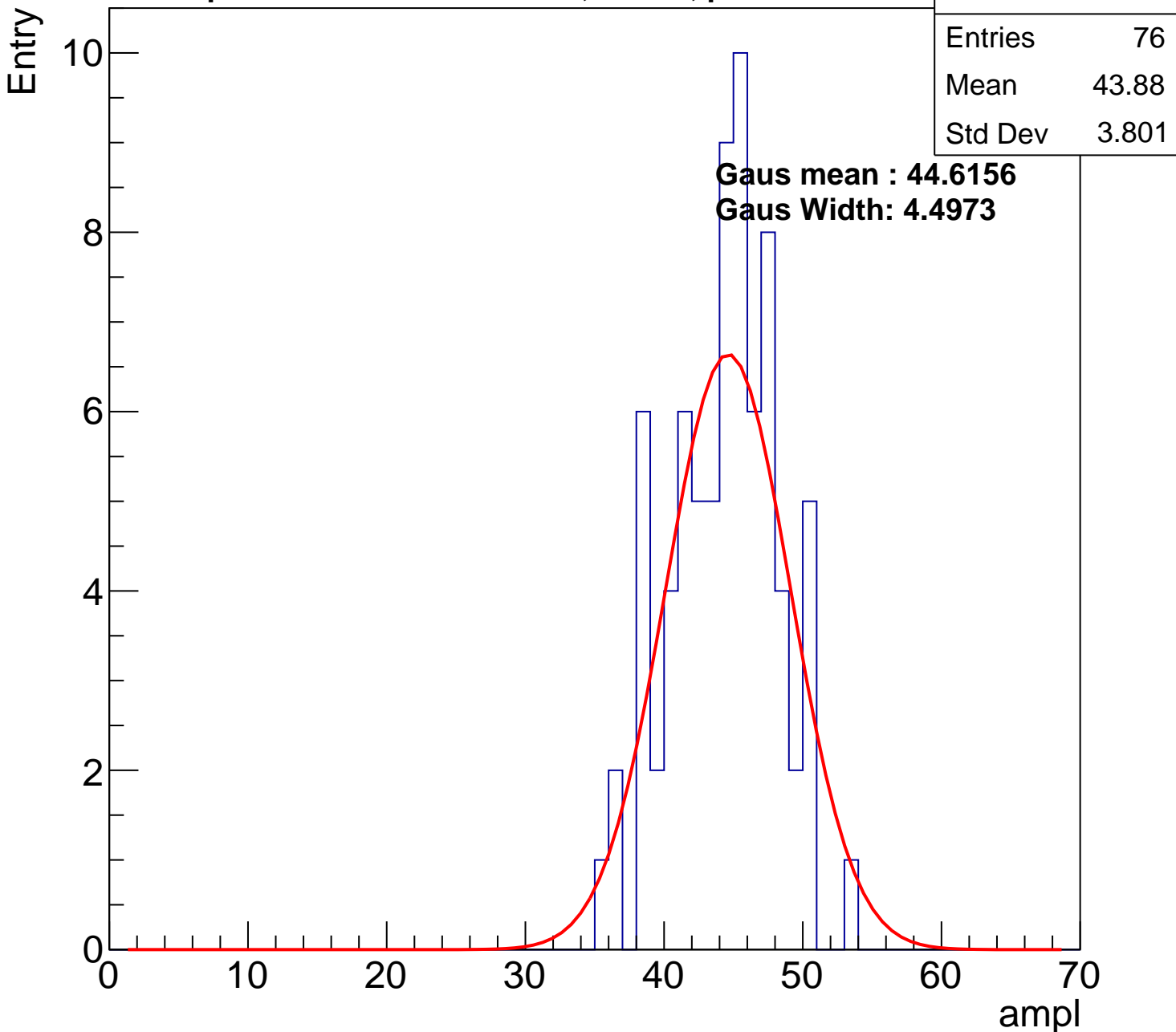
**Gaus Width: 4.4973**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

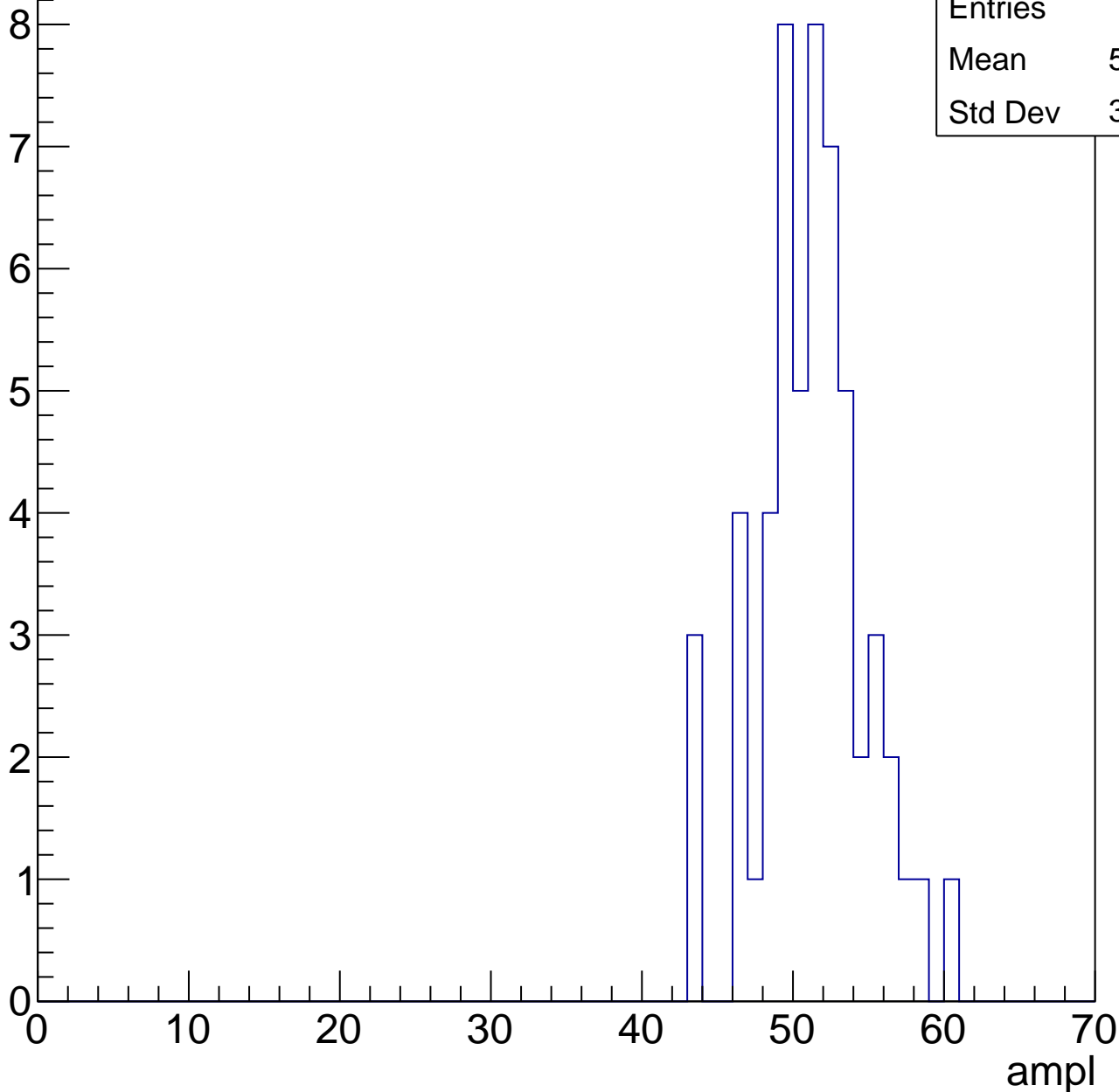


# B1L003S, U6-ch94, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	50.75
Std Dev	3.533

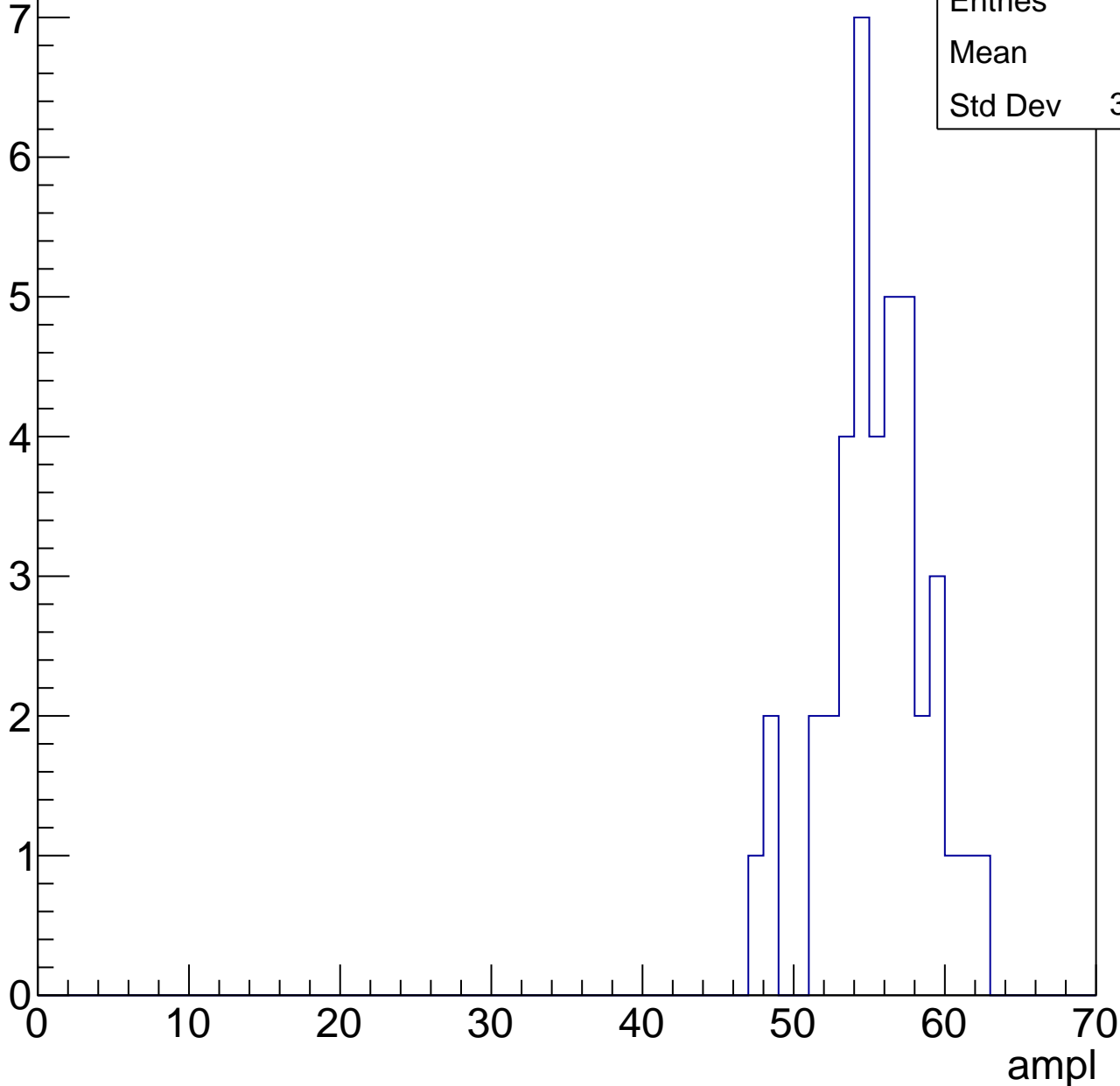


# B1L003S, U6-ch94, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	40
Mean	55
Std Dev	3.302

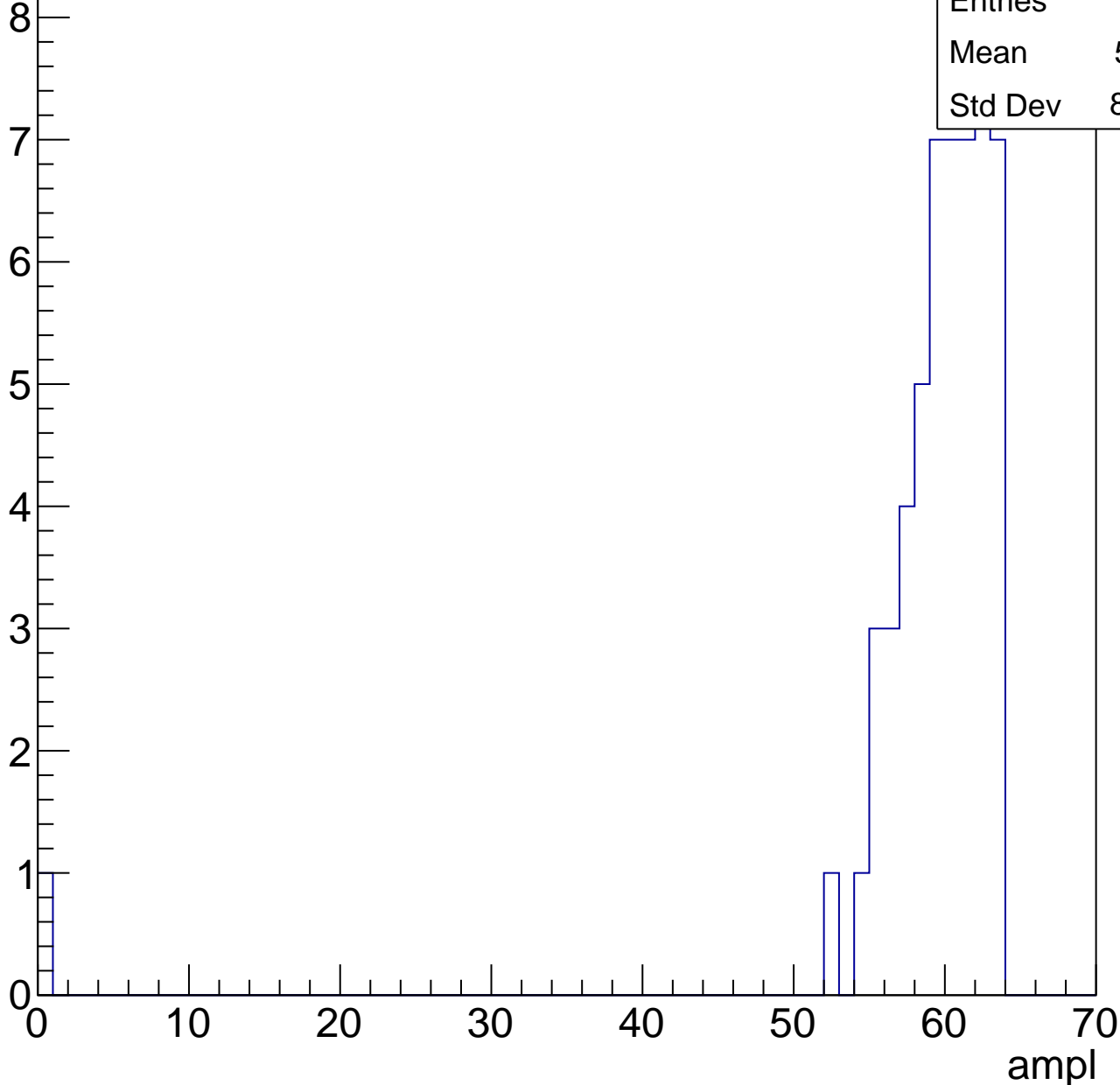


# B1L003S, U6-ch94, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	54
Mean	58.41
Std Dev	8.445



# B1L003S, U6-ch94, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries

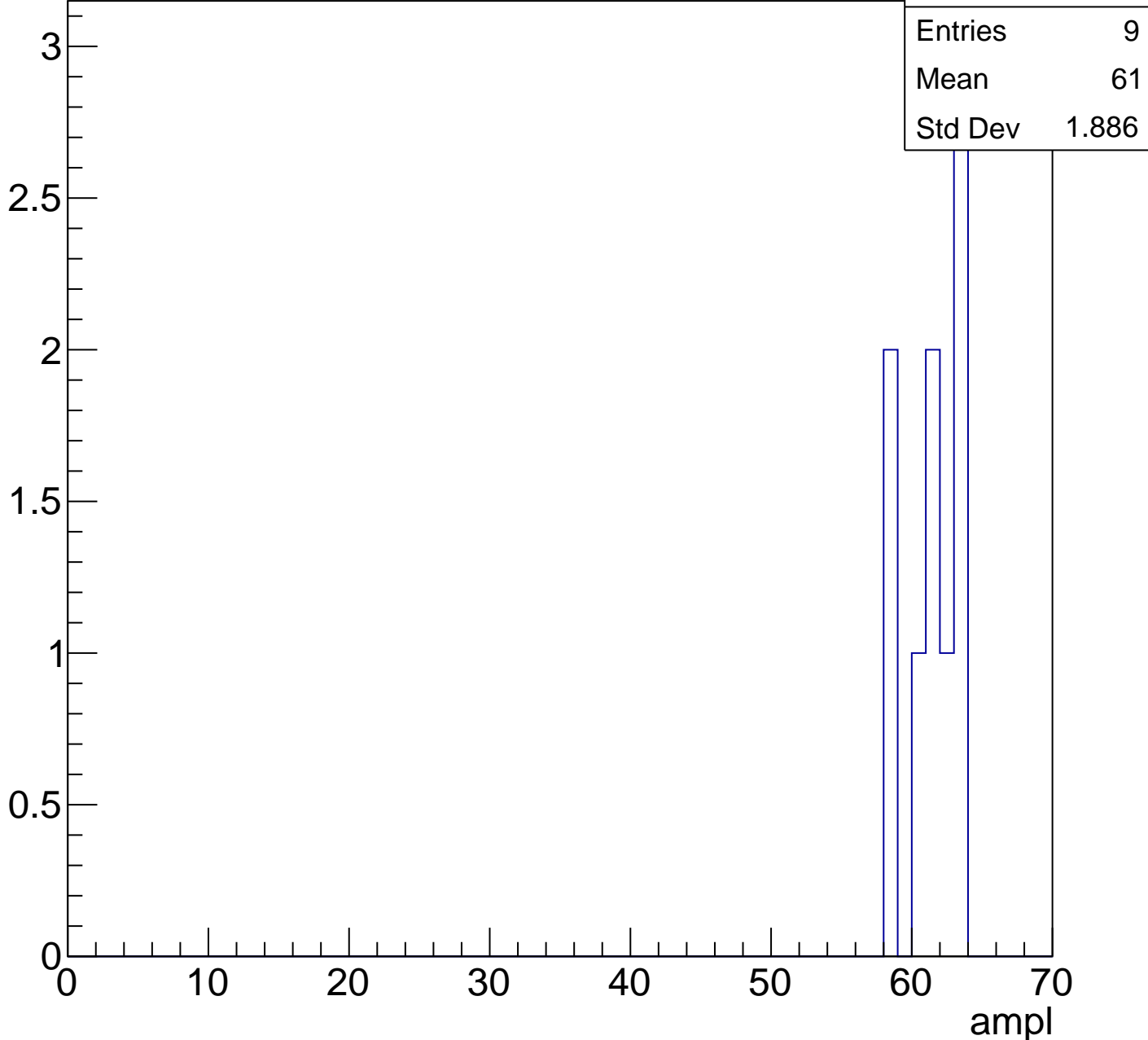
9

Mean

61

Std Dev

1.886





# B1L003S, U6-ch94, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U6-ch95, adc0

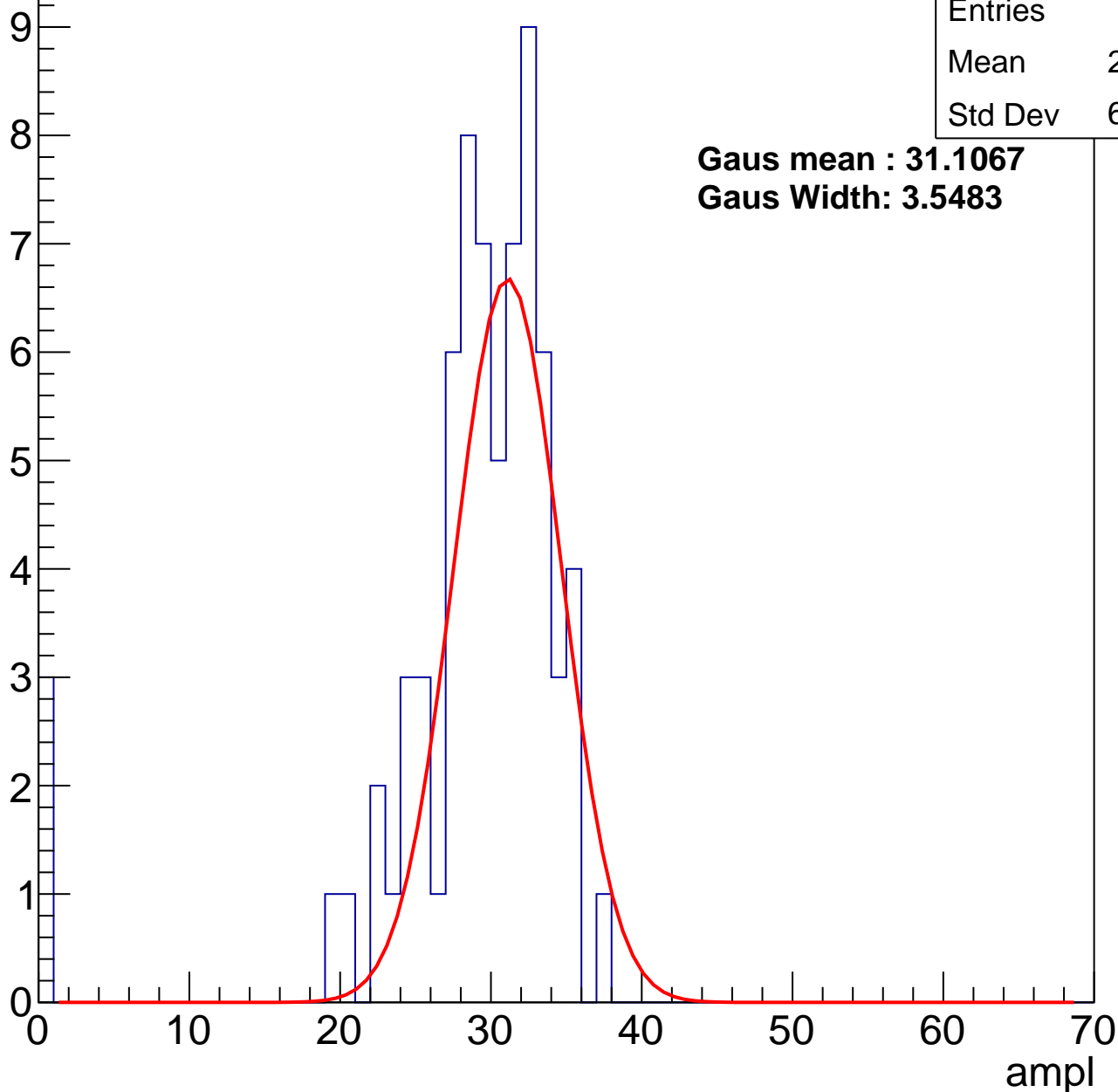
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	71
Mean	28.17
Std Dev	6.967

**Gaus mean : 31.1067**

**Gaus Width: 3.5483**



# B1L003S, U6-ch95, adc1

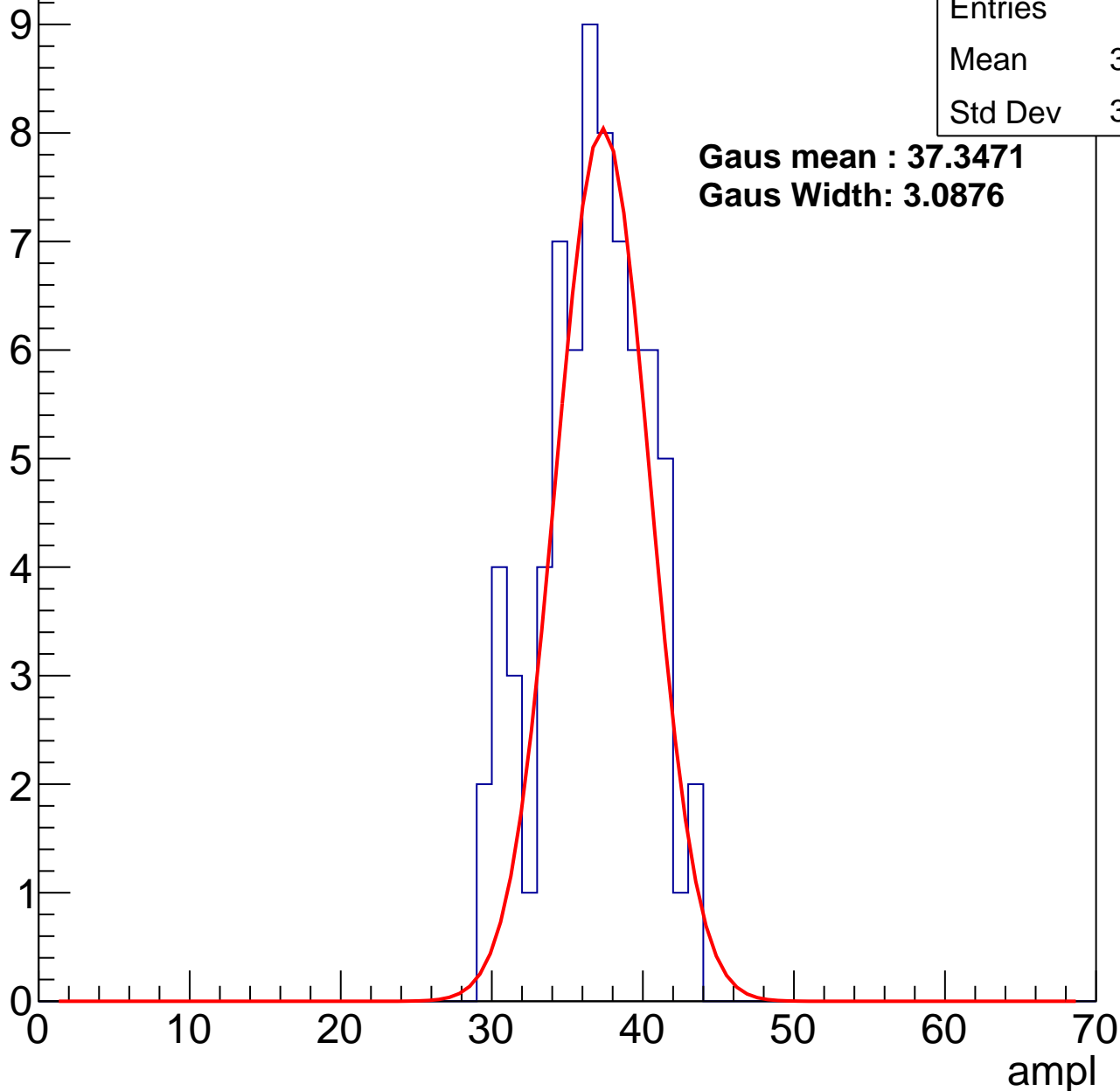
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	71
Mean	36.28
Std Dev	3.444

**Gaus mean : 37.3471**

**Gaus Width: 3.0876**



# B1L003S, U6-ch95, adc2

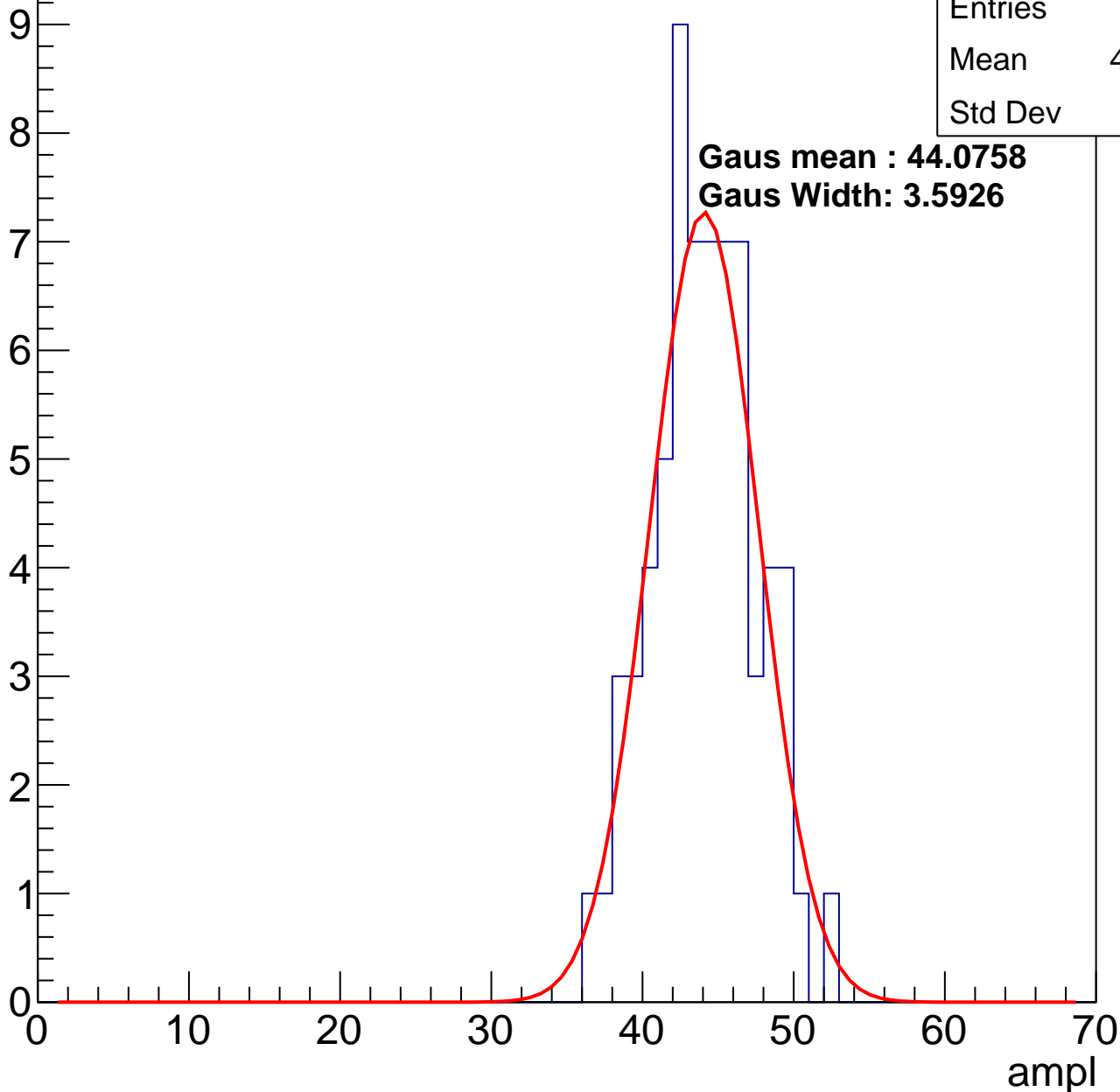
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	43.64
Std Dev	3.38

**Gaus mean : 44.0758**

**Gaus Width: 3.5926**

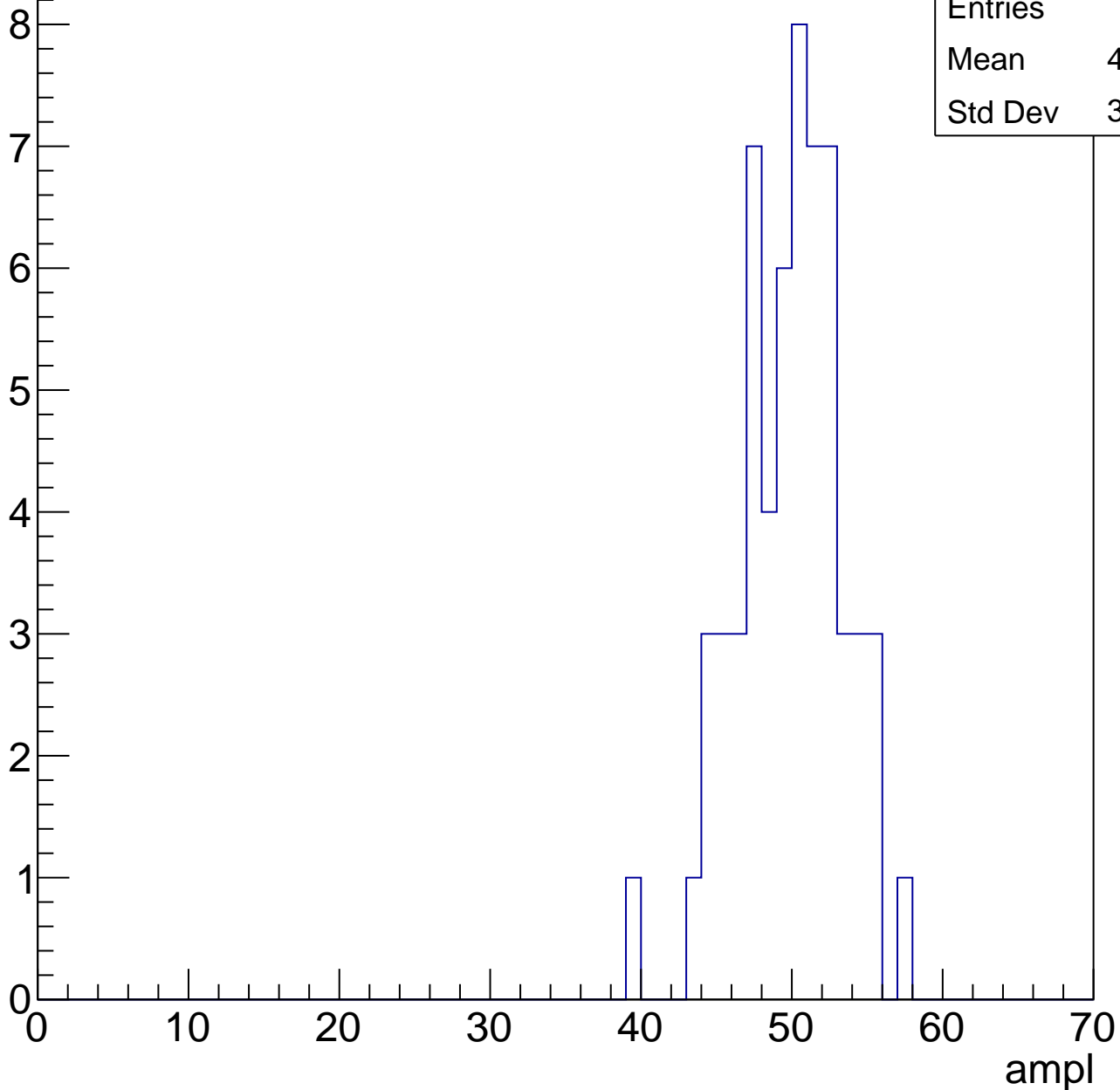


# B1L003S, U6-ch95, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	49.43
Std Dev	3.417

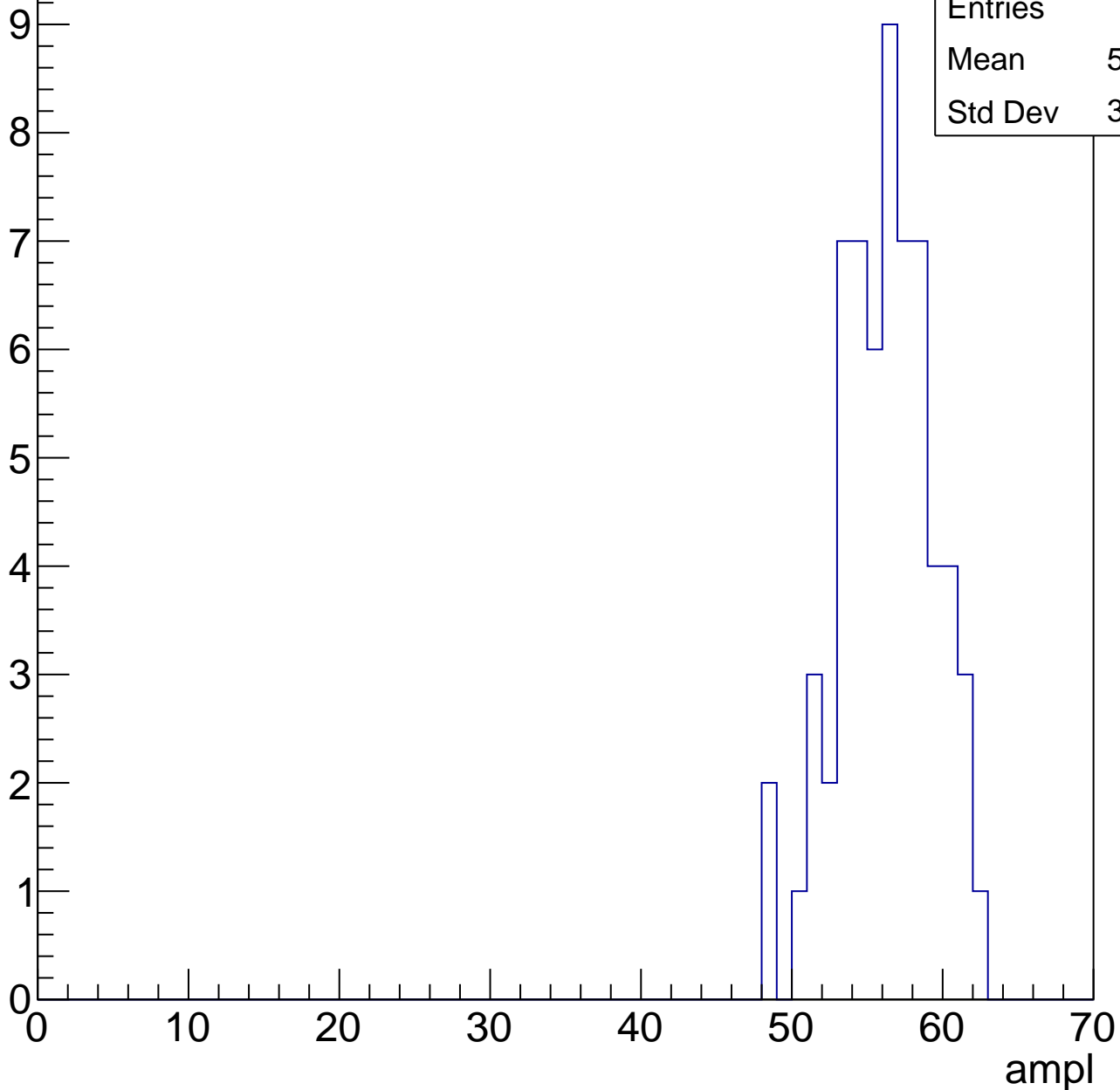


# B1L003S, U6-ch95, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	55.75
Std Dev	3.112

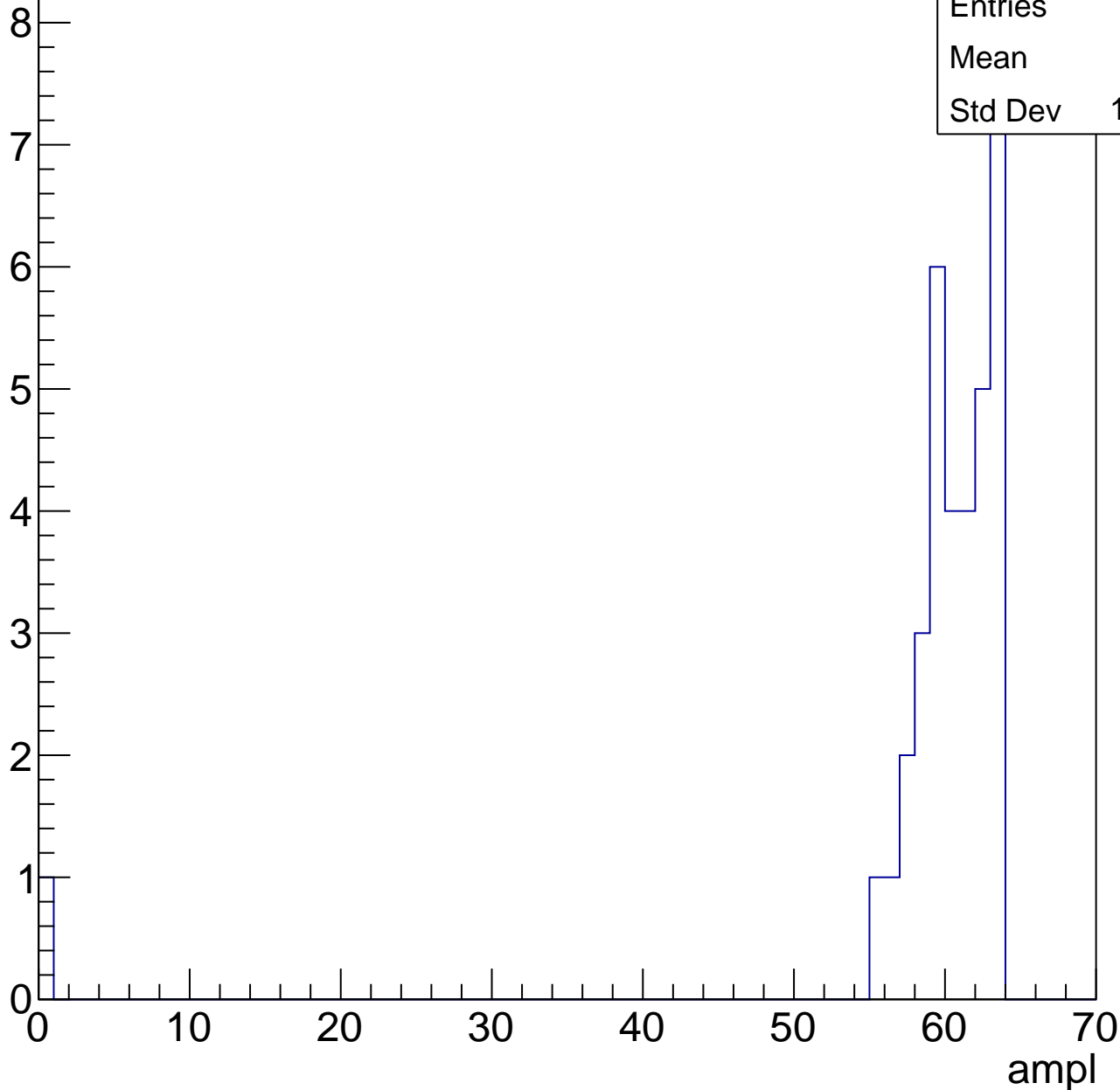


# B1L003S, U6-ch95, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

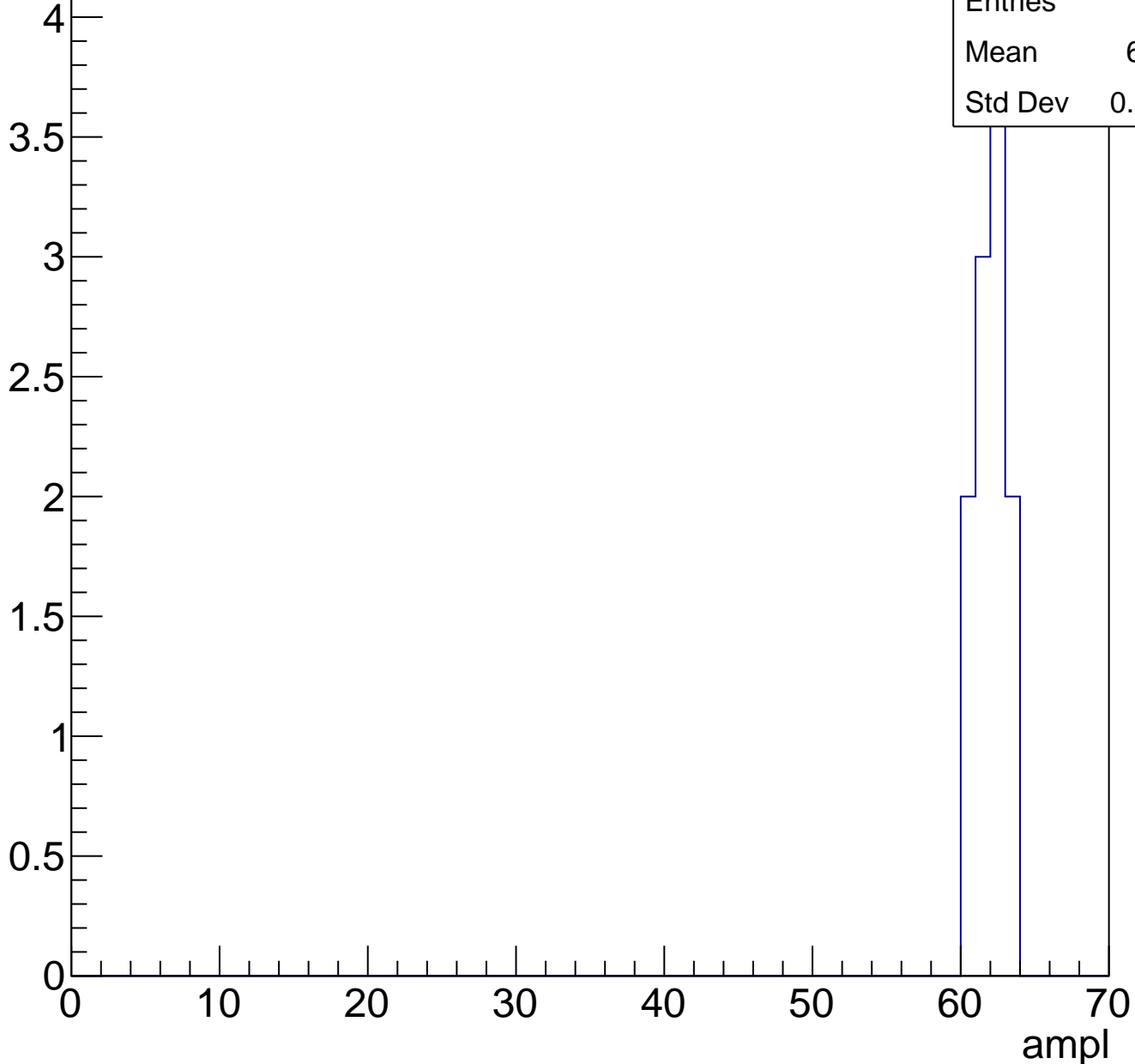
Entries	35
Mean	58.6
Std Dev	10.29



# B1L003S, U6-ch95, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	11
Mean	61.55
Std Dev	0.9875



# B1L003S, U6-ch95, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch96, adc0

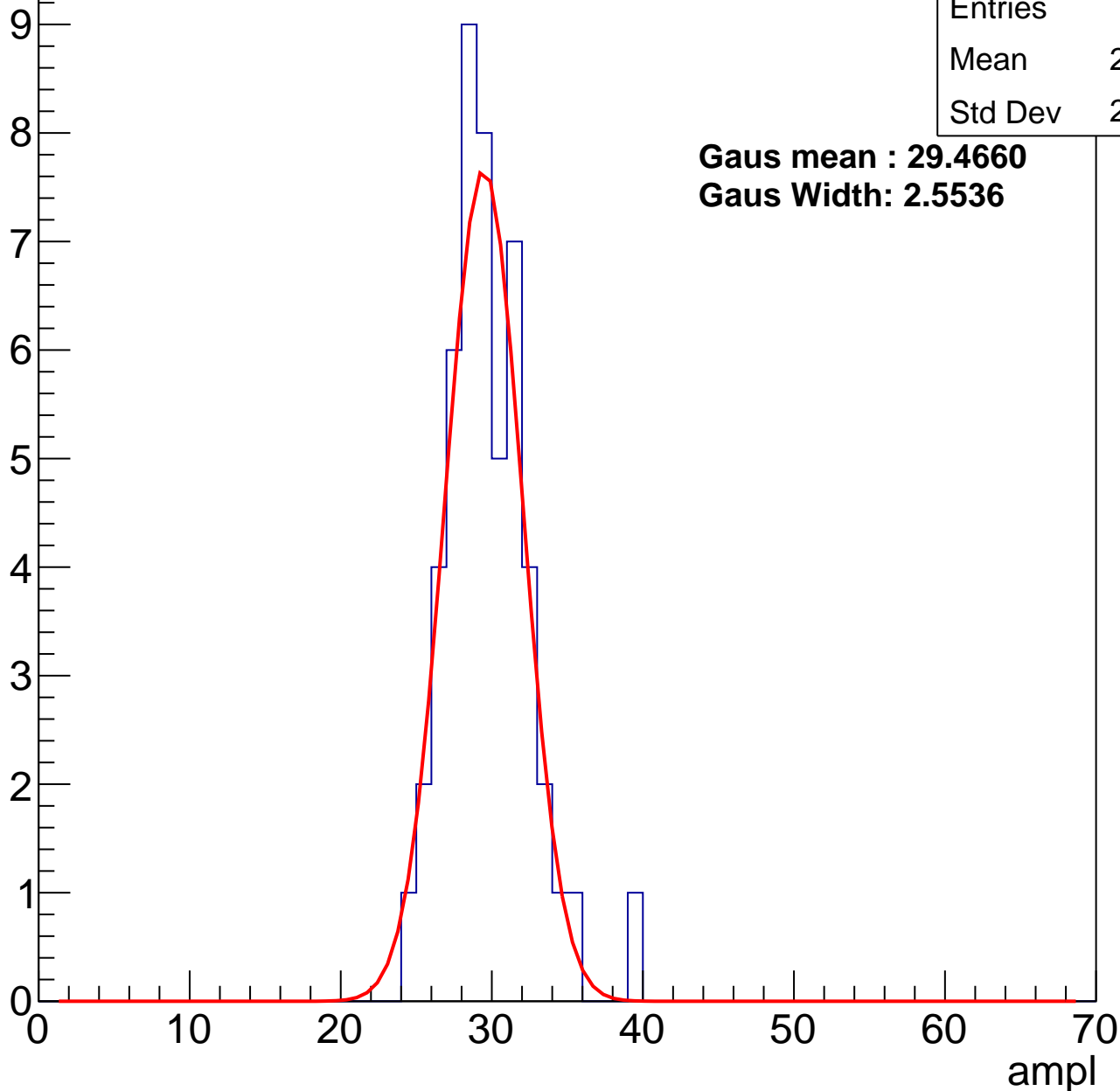
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	51
Mean	29.27
Std Dev	2.745

**Gaus mean : 29.4660**

**Gaus Width: 2.5536**



# B1L003S, U6-ch96, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	76
Mean	35.78
Std Dev	3.21

**Gaus mean : 35.9829**

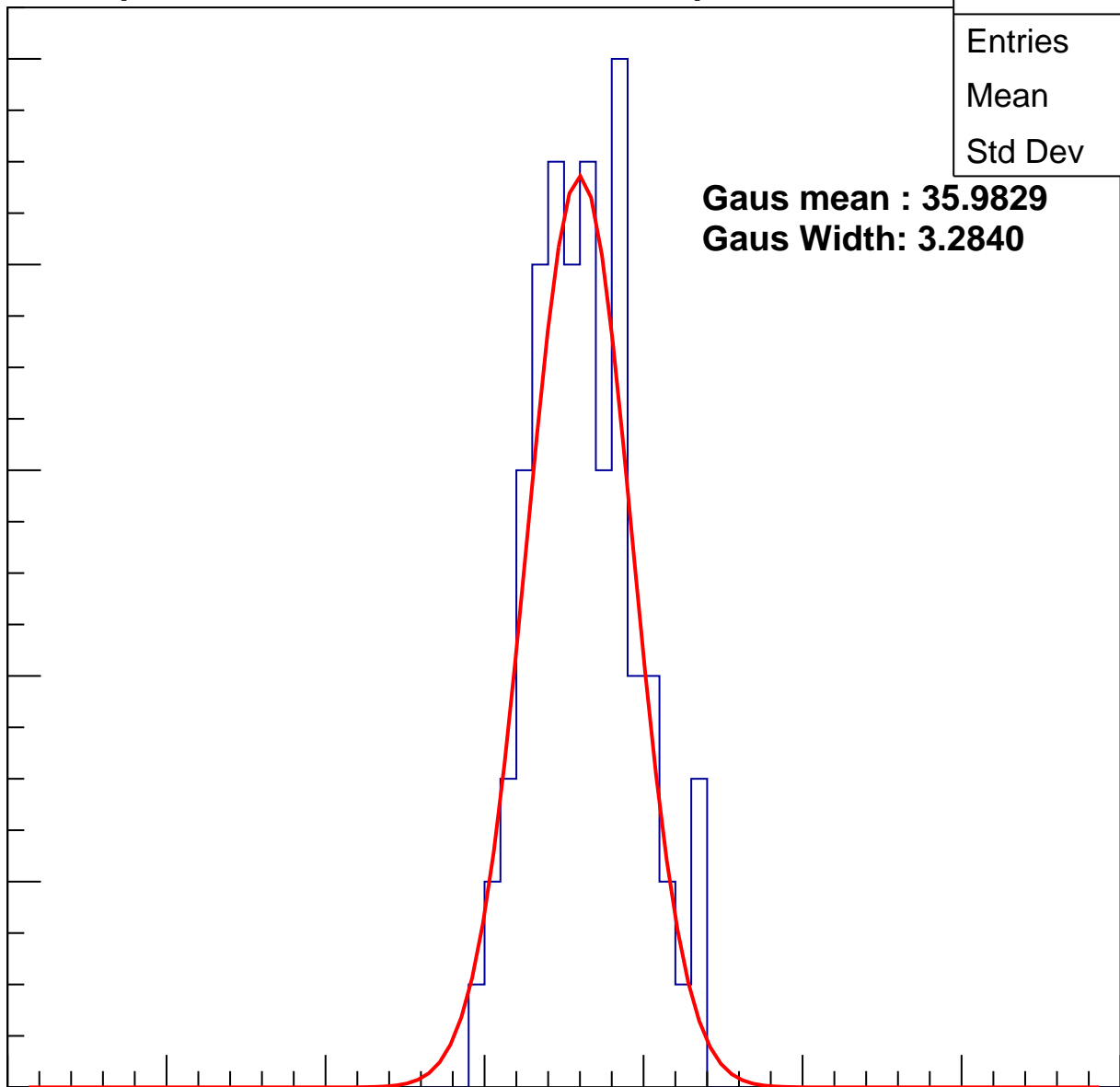
**Gaus Width: 3.2840**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L003S, U6-ch96, adc2

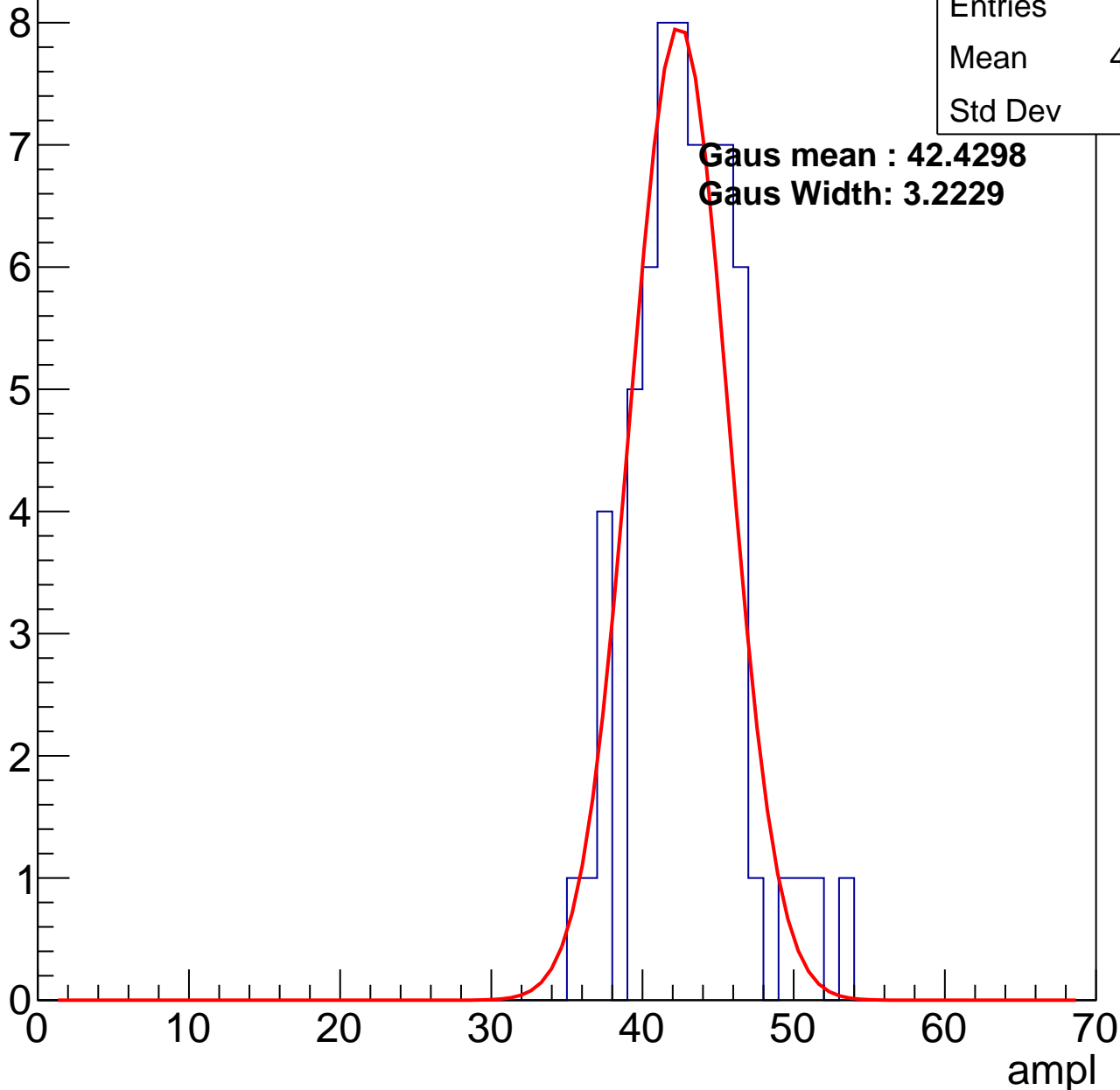
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	42.58
Std Dev	3.45

**Gaus mean : 42.4298**

**Gaus Width: 3.2229**

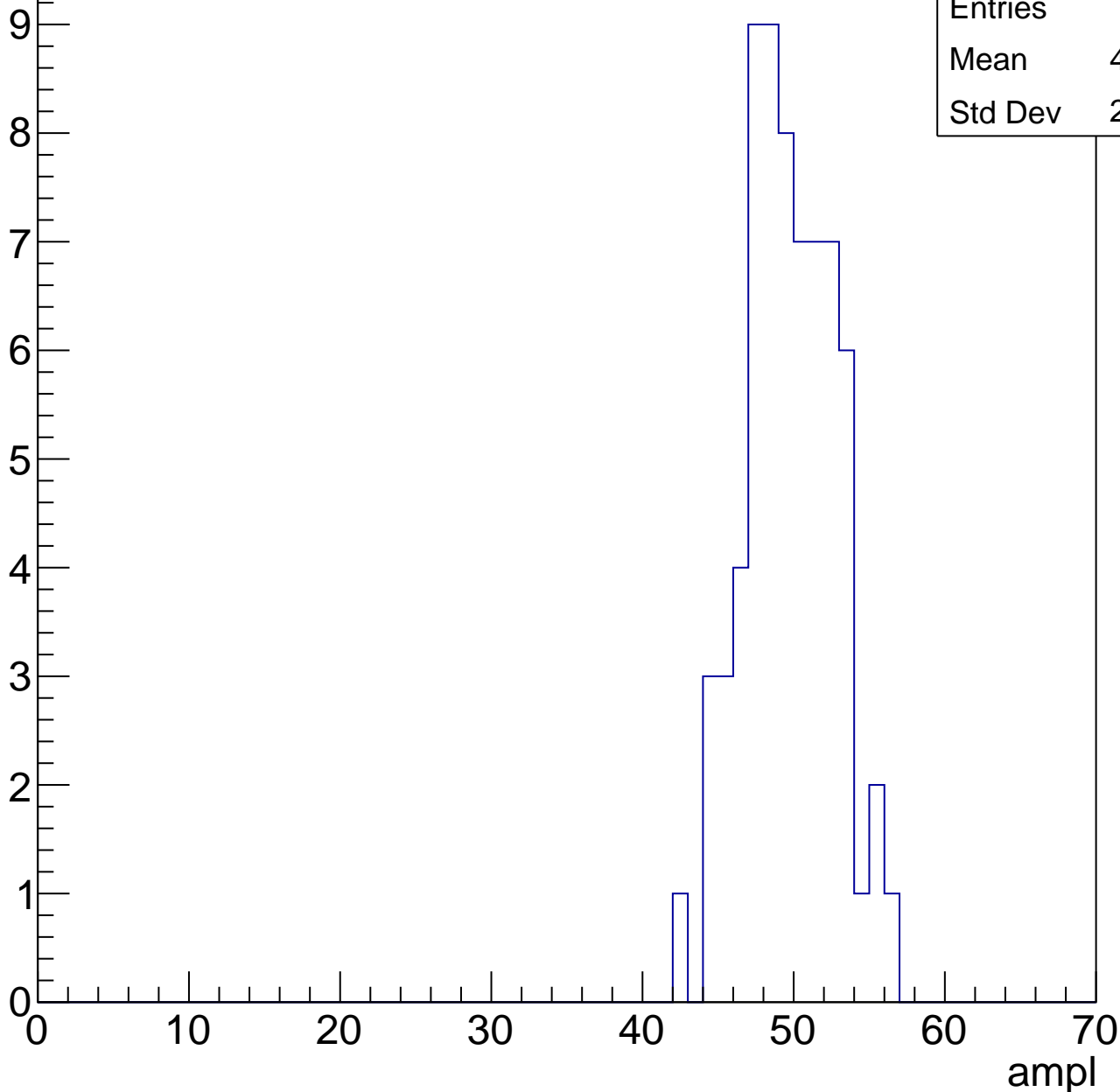


# B1L003S, U6-ch96, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	49.25
Std Dev	2.942

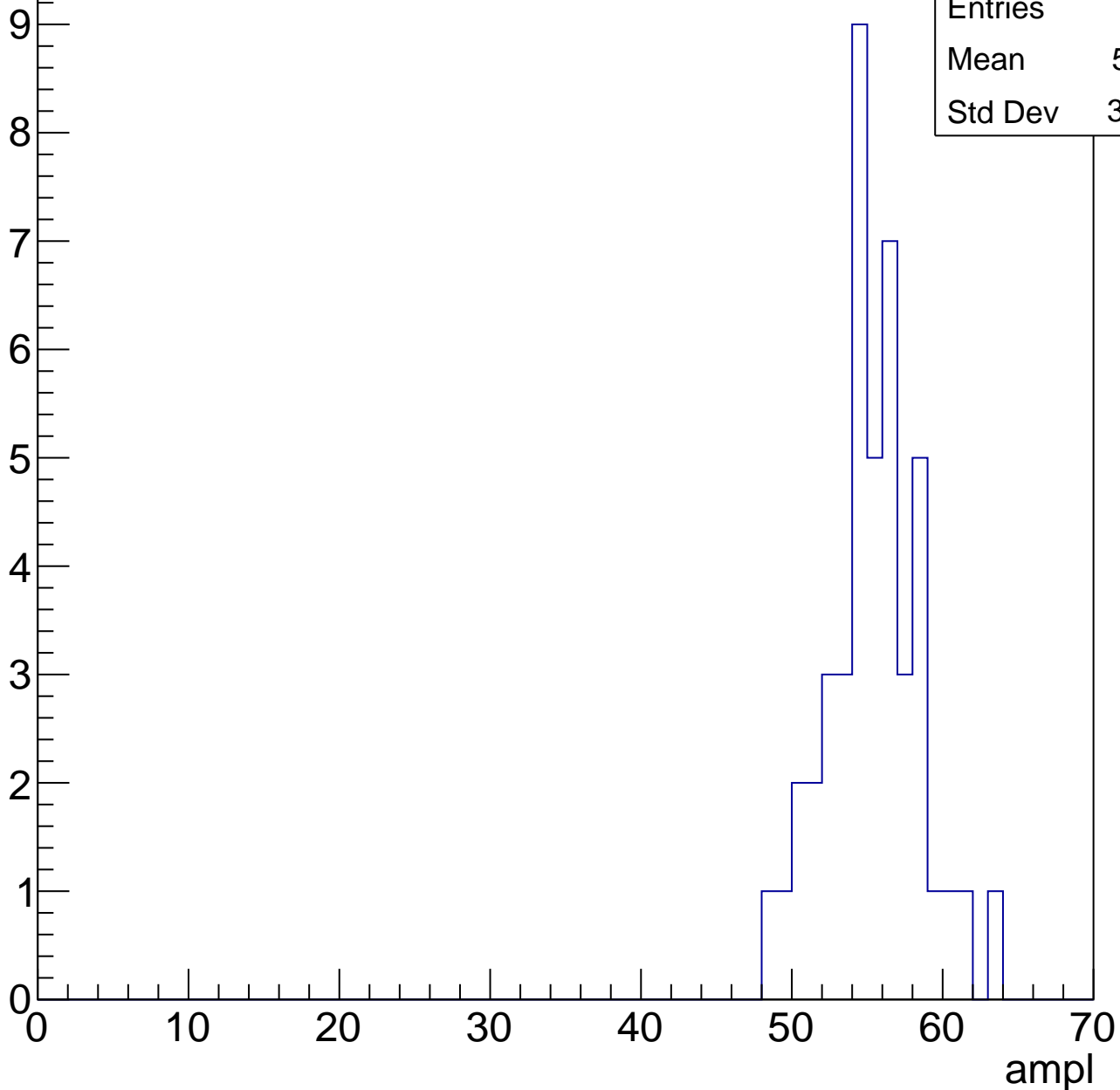


# B1L003S, U6-ch96, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	45
Mean	54.91
Std Dev	3.054

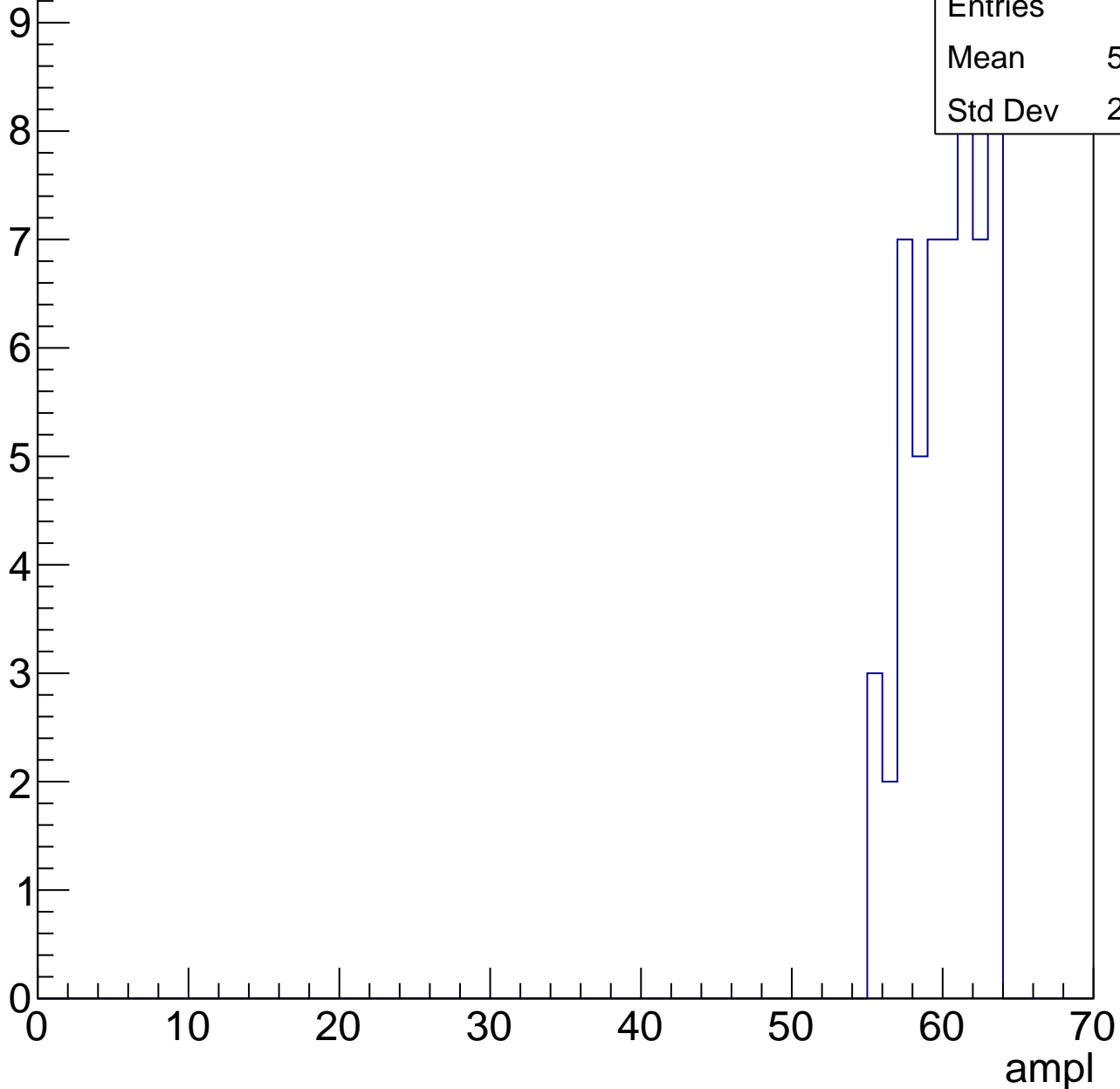


# B1L003S, U6-ch96, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	59.75
Std Dev	2.345



# B1L003S, U6-ch96, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries

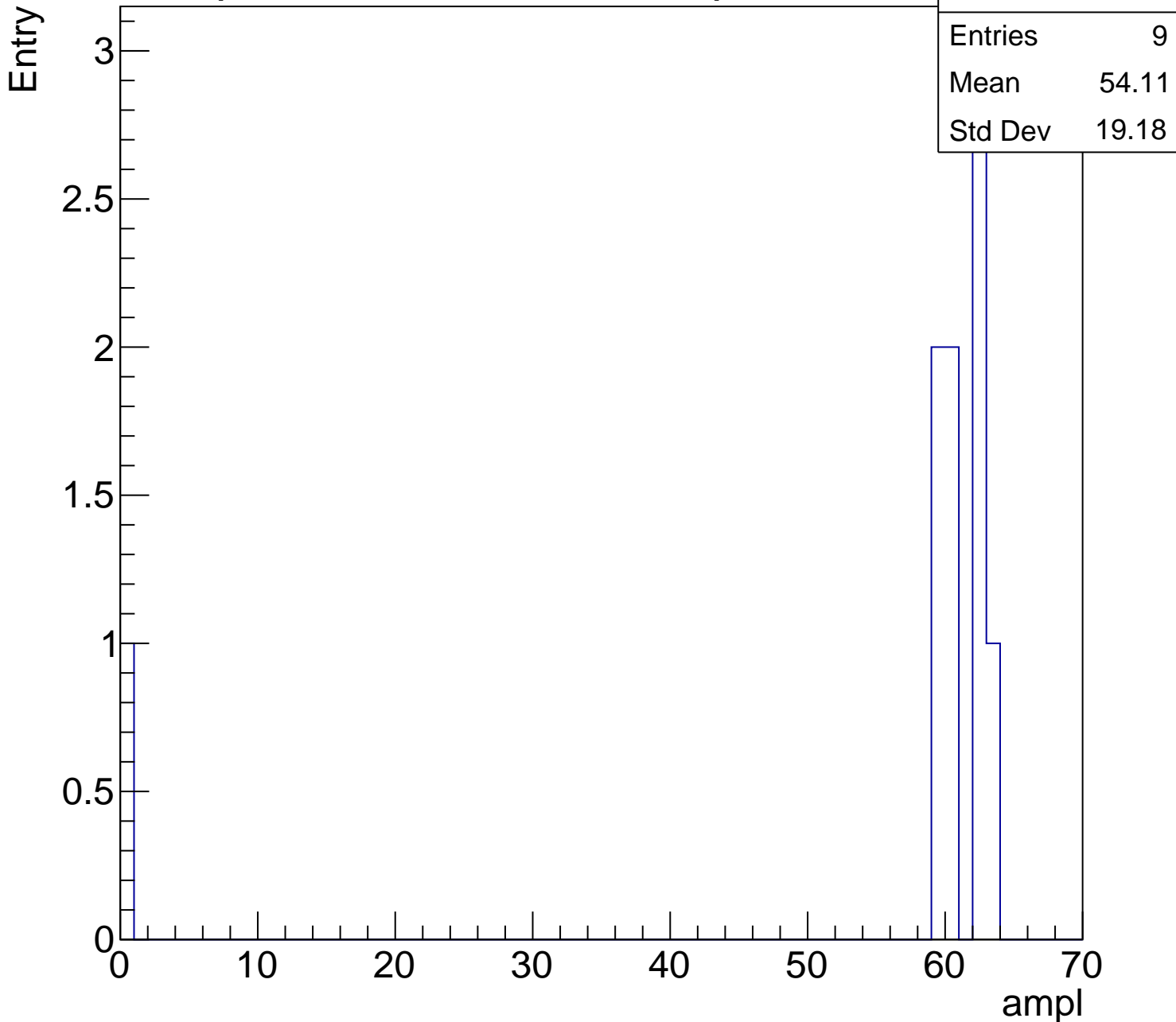
9

Mean

54.11

Std Dev

19.18





# B1L003S, U6-ch96, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch97, adc0

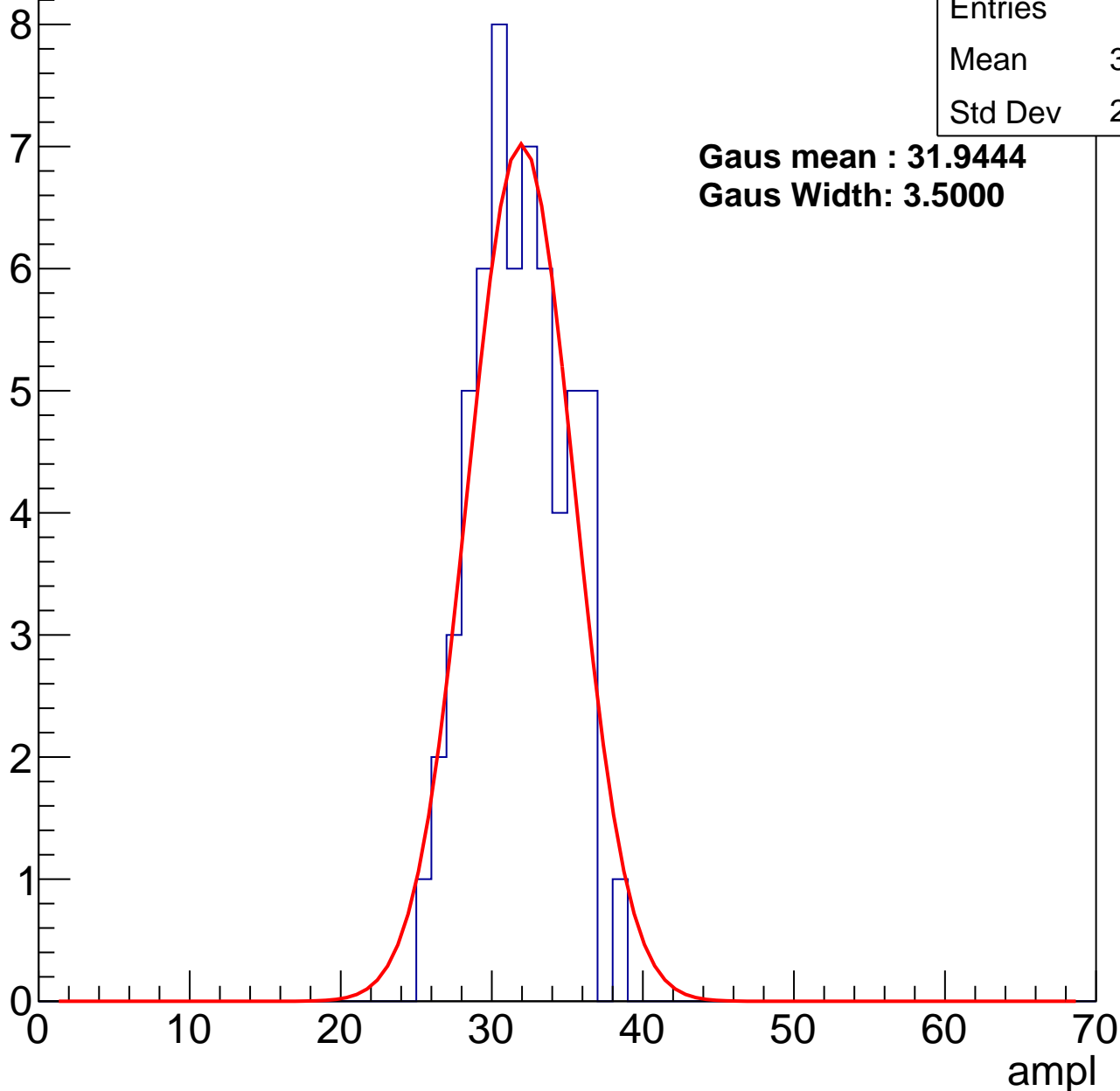
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	31.34
Std Dev	2.984

**Gaus mean : 31.9444**

**Gaus Width: 3.5000**



# B1L003S, U6-ch97, adc1

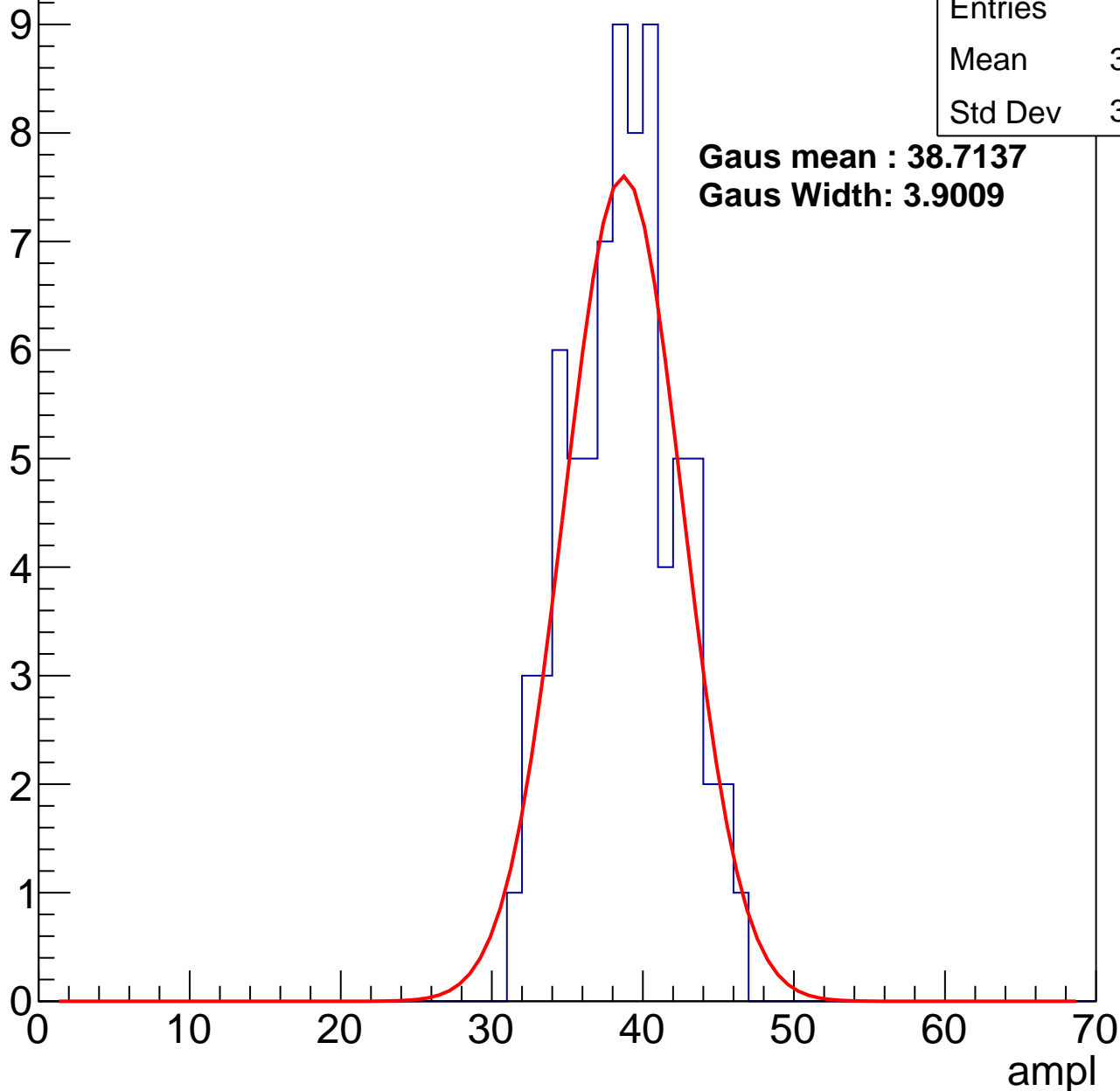
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	75
Mean	38.28
Std Dev	3.489

**Gaus mean : 38.7137**

**Gaus Width: 3.9009**



# B1L003S, U6-ch97, adc2

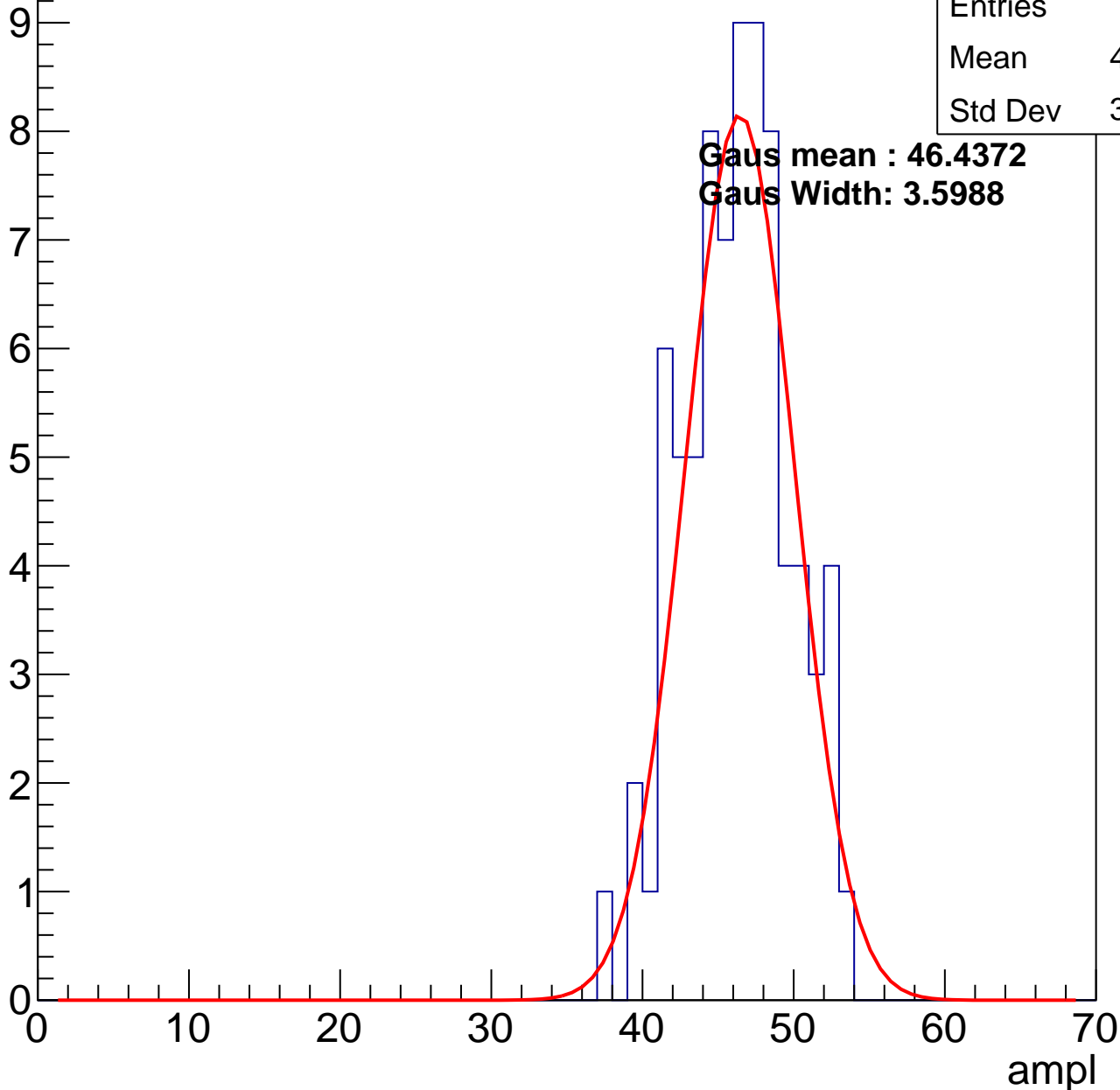
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	77
Mean	45.77
Std Dev	3.482

**Gaus mean : 46.4372**

**Gaus Width: 3.5988**

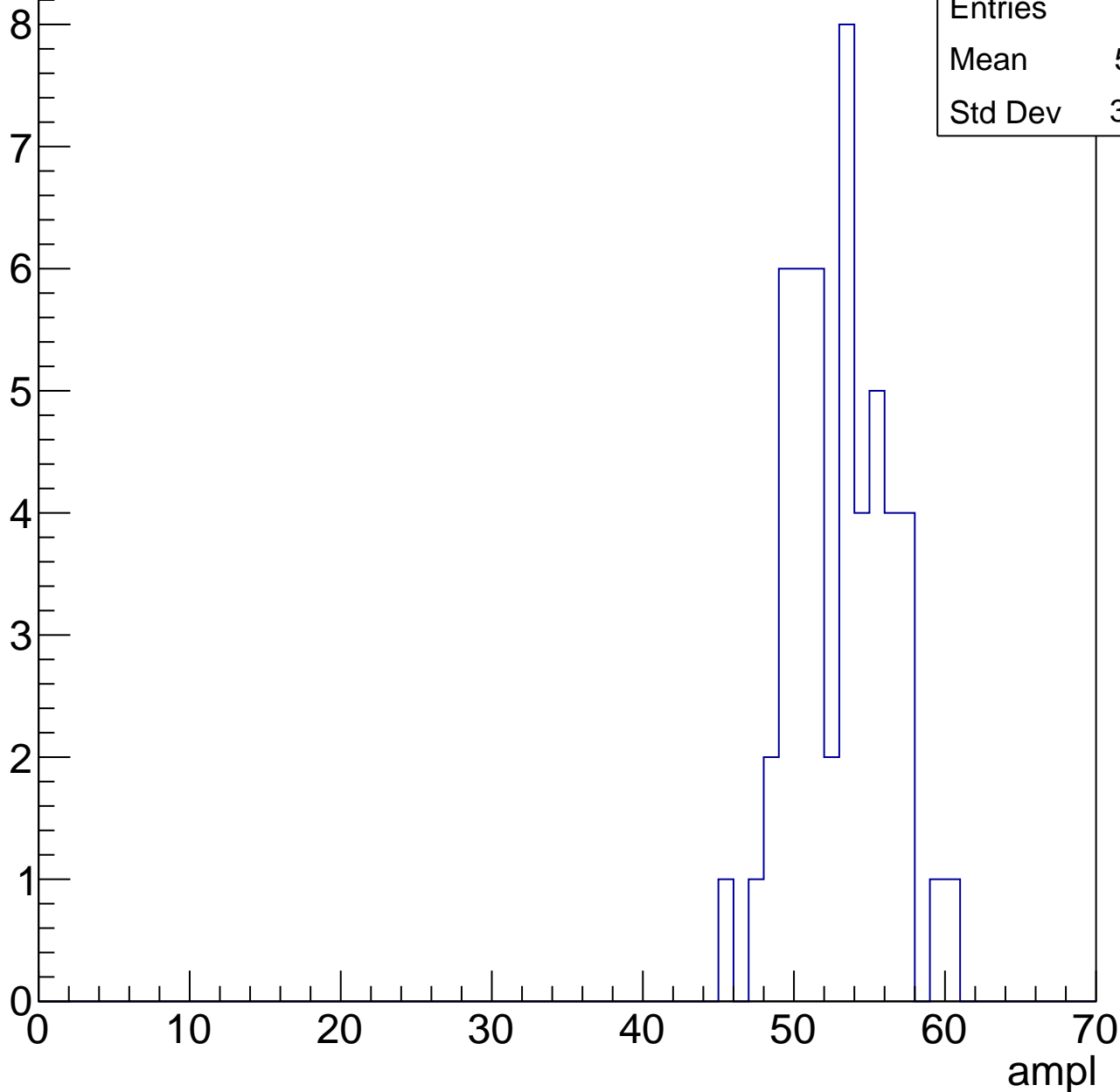


# B1L003S, U6-ch97, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

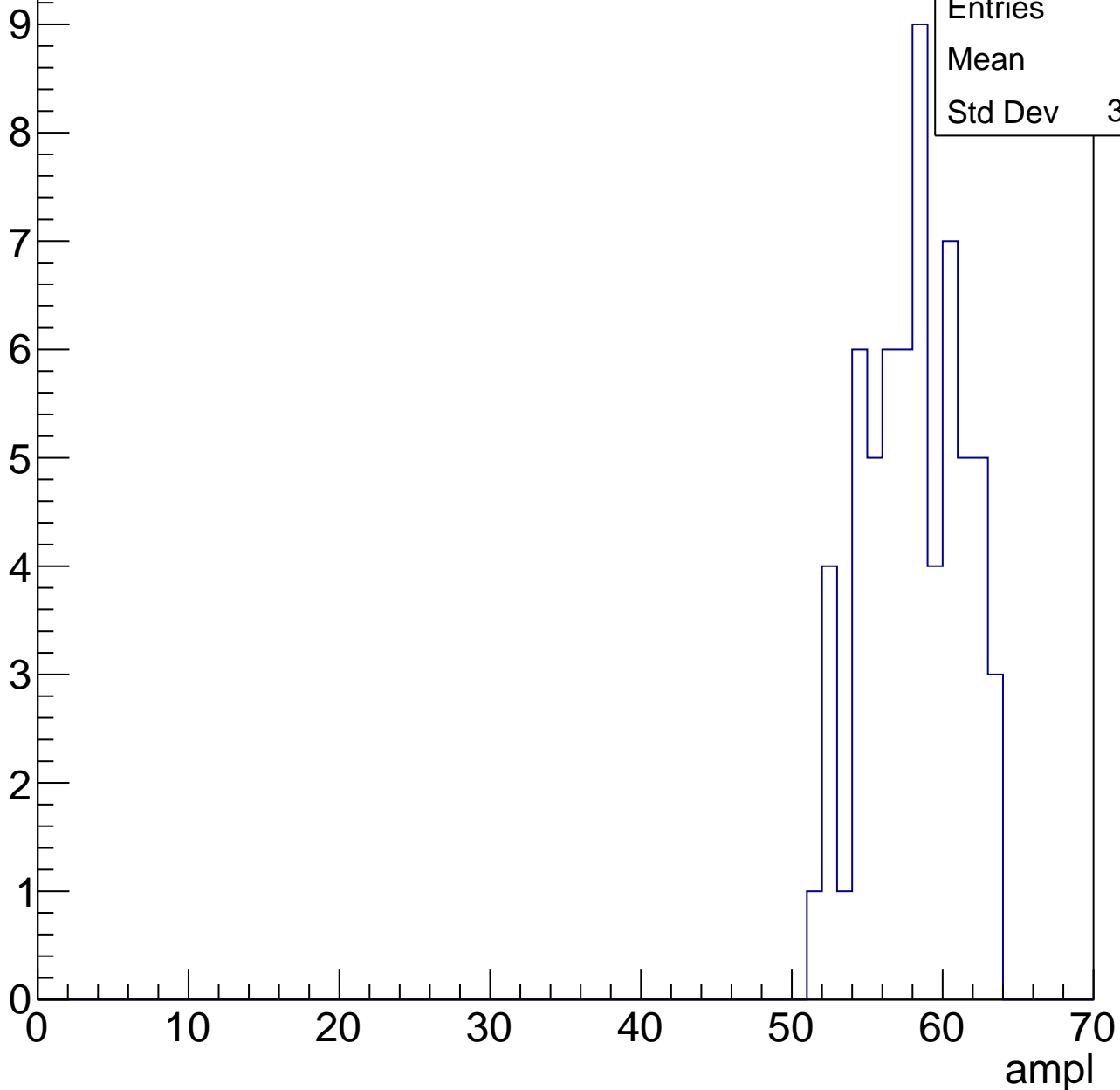
Entries	51
Mean	52.51
Std Dev	3.202



# B1L003S, U6-ch97, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



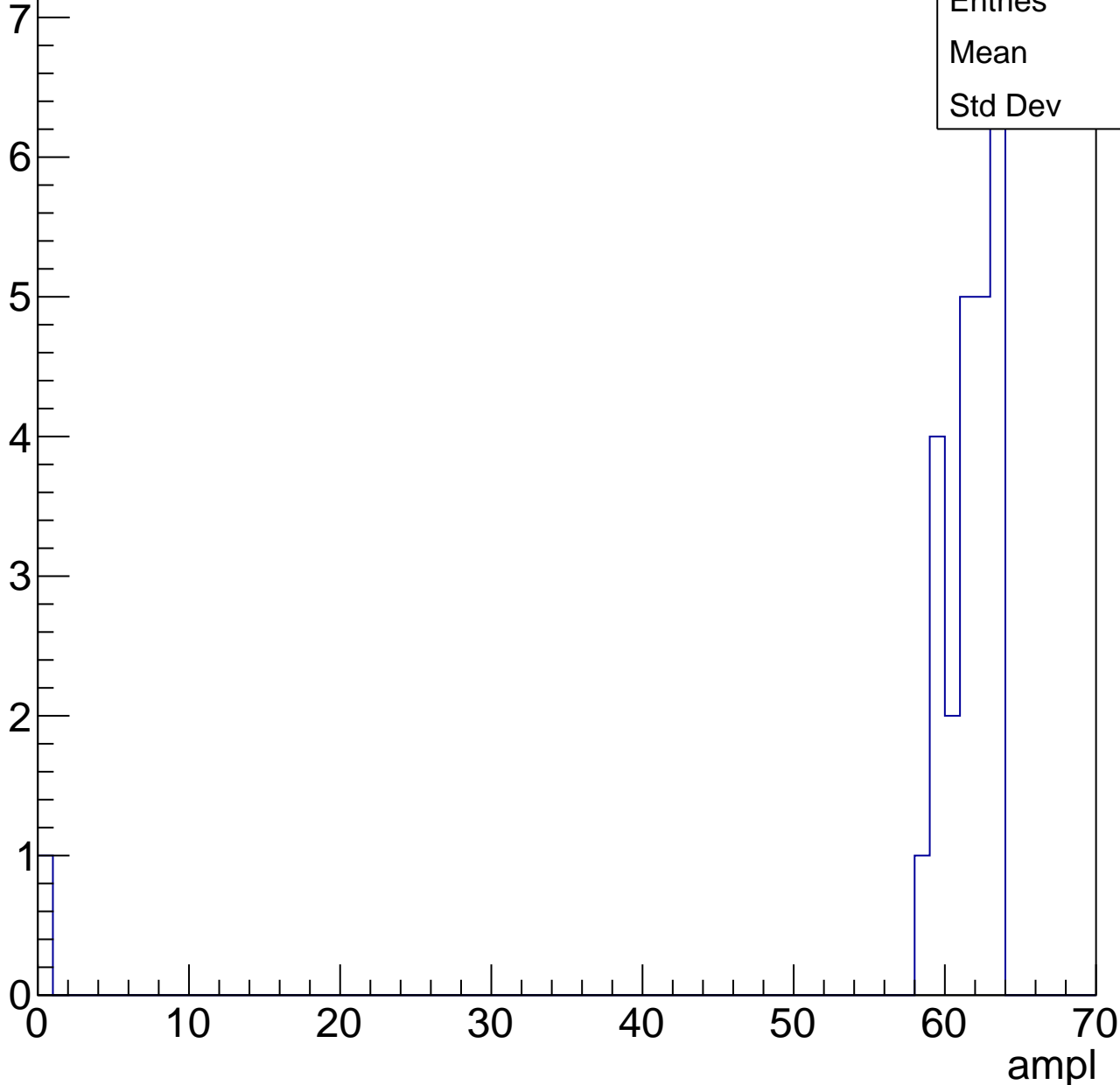
Entries	62
Mean	57.6
Std Dev	3.139

# B1L003S, U6-ch97, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	25
Mean	58.8
Std Dev	12.1



# B1L003S, U6-ch97, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

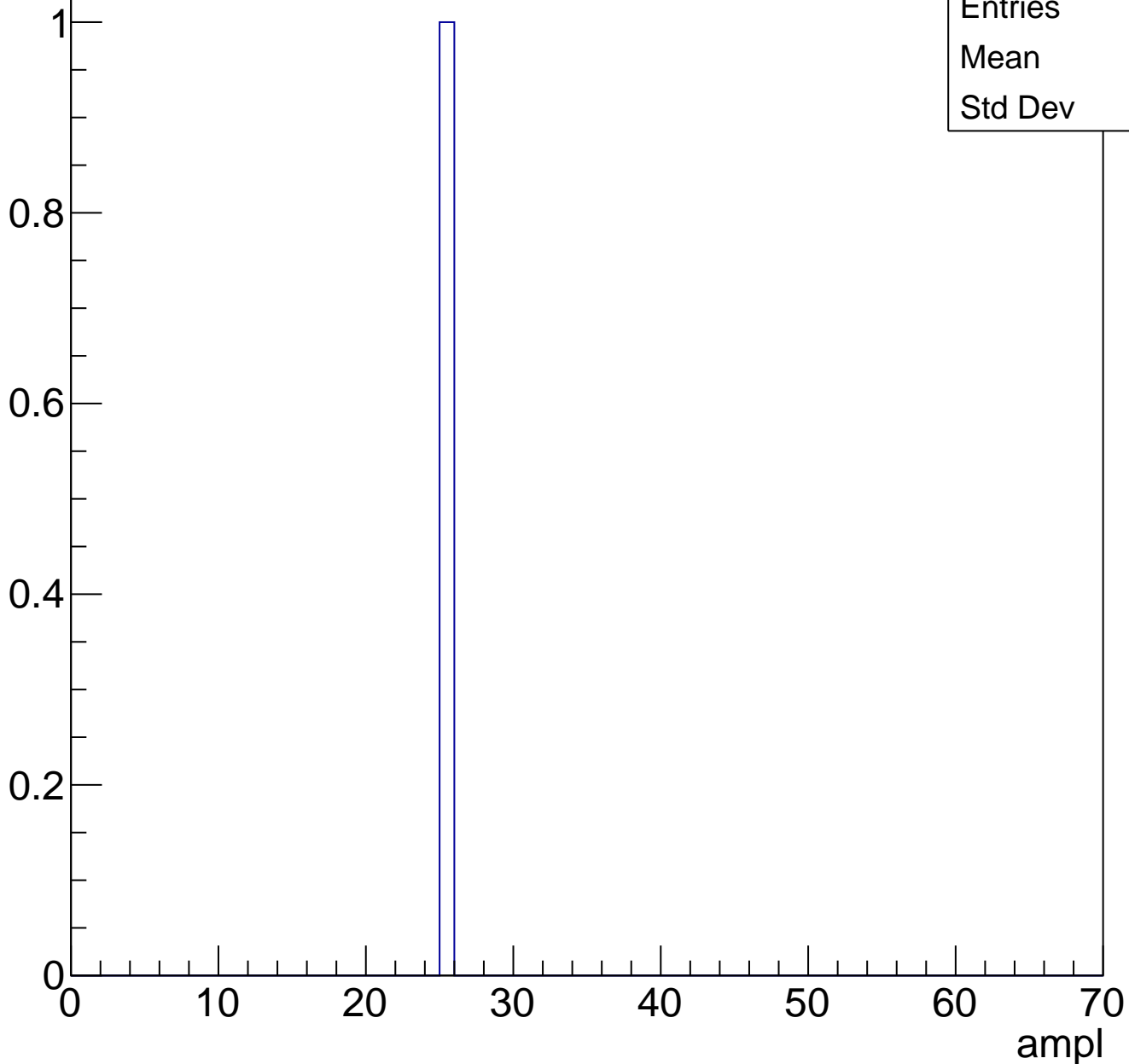




# B1L003S, U6-ch97, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	25
Std Dev	0

# B1L003S, U6-ch98, adc0

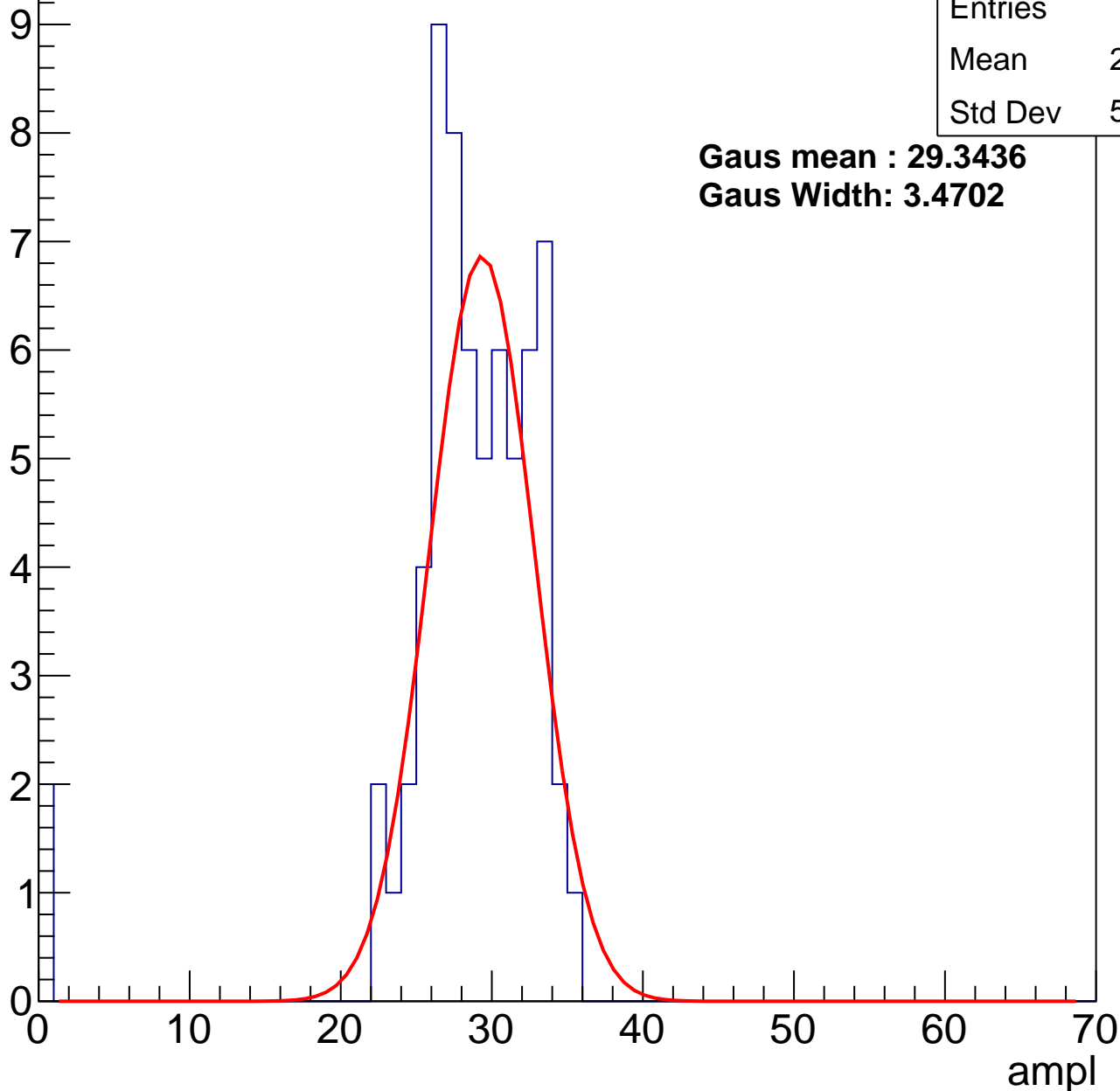
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	27.86
Std Dev	5.828

**Gaus mean : 29.3436**

**Gaus Width: 3.4702**



# B1L003S, U6-ch98, adc1

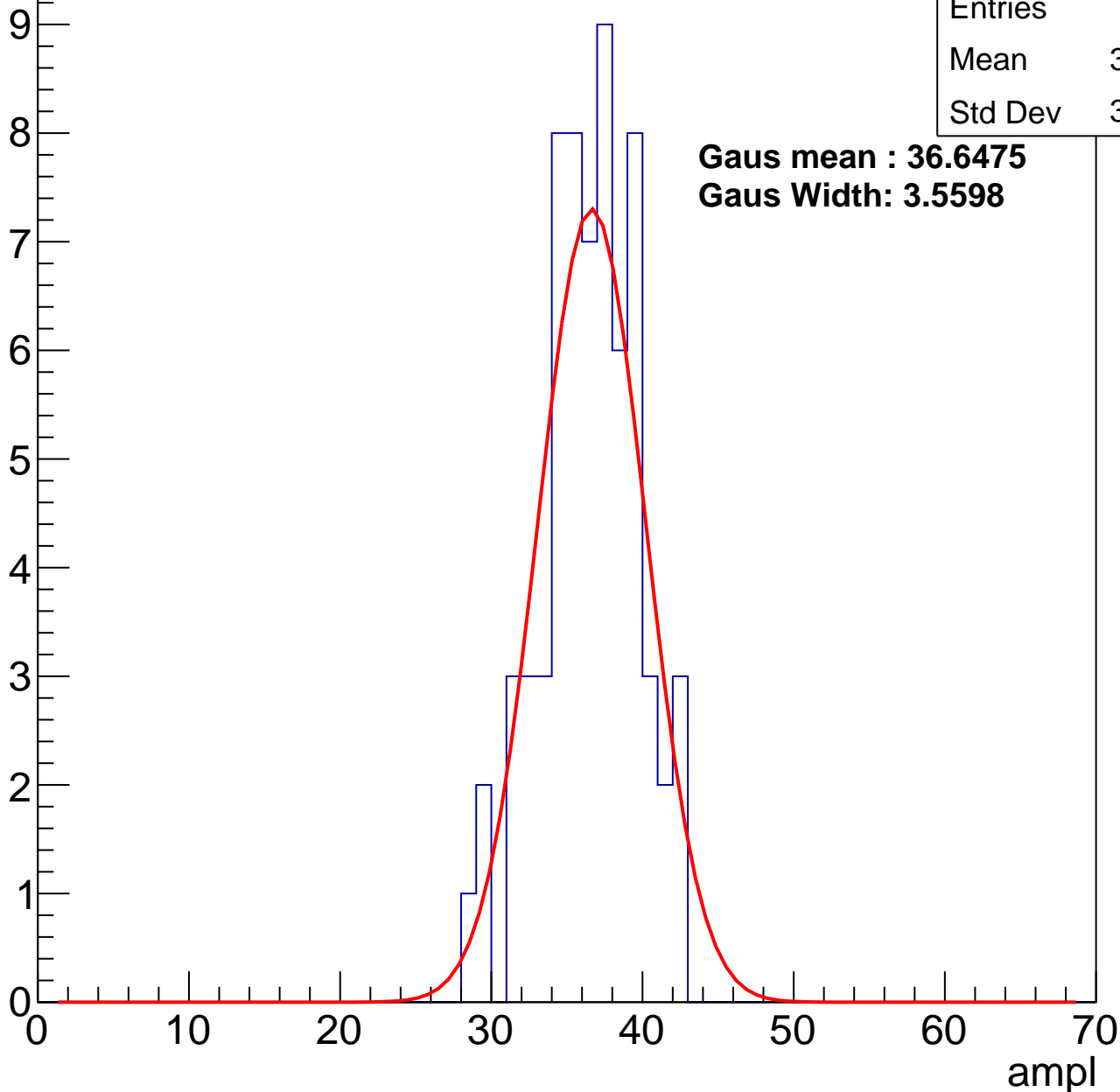
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	36.05
Std Dev	3.169

**Gaus mean : 36.6475**

**Gaus Width: 3.5598**



# B1L003S, U6-ch98, adc2

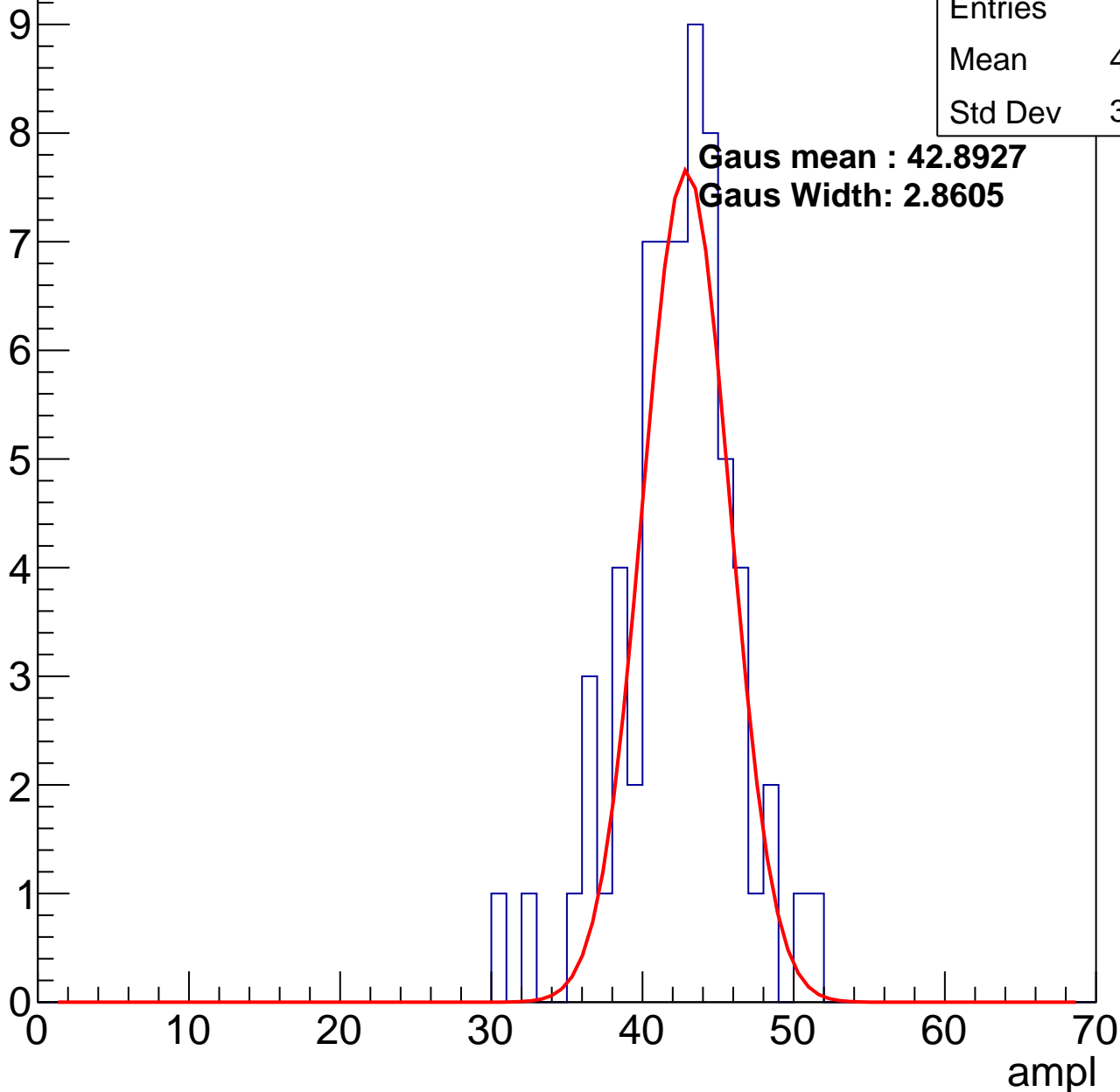
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	41.92
Std Dev	3.792

**Gaus mean : 42.8927**

**Gaus Width: 2.8605**

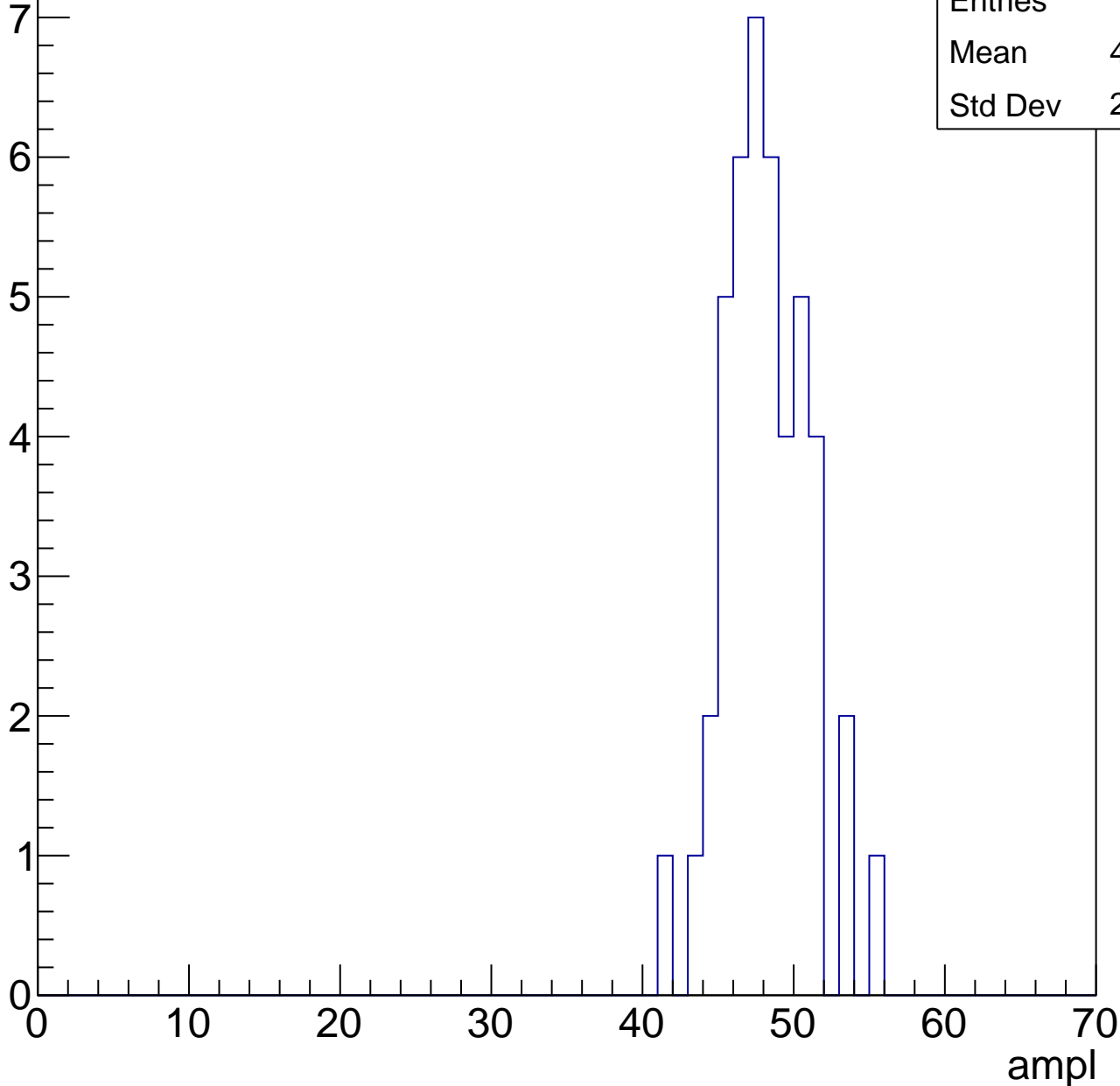


# B1L003S, U6-ch98, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	44
Mean	47.75
Std Dev	2.773

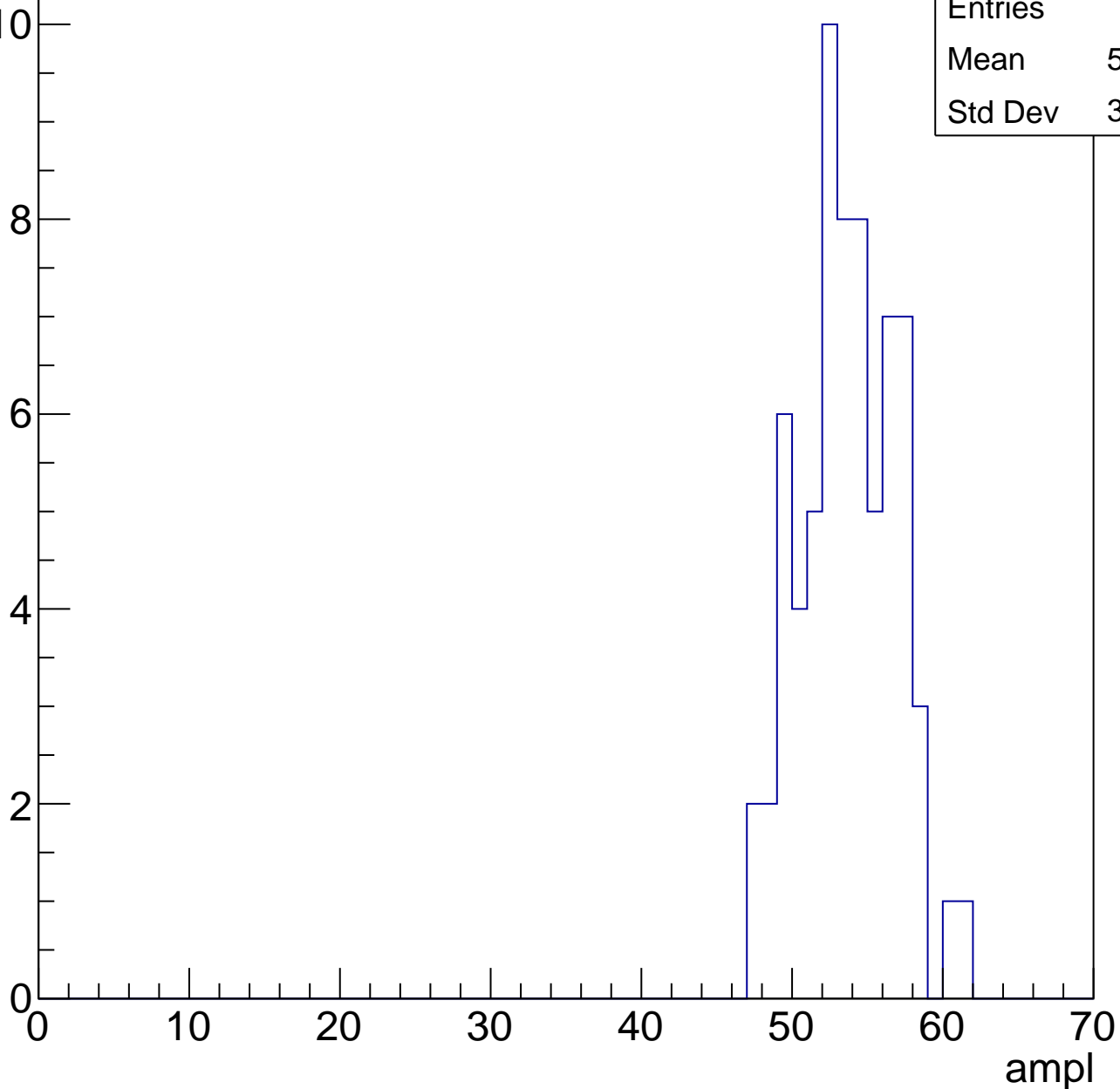


# B1L003S, U6-ch98, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	53.28
Std Dev	3.116



# B1L003S, U6-ch98, adc5

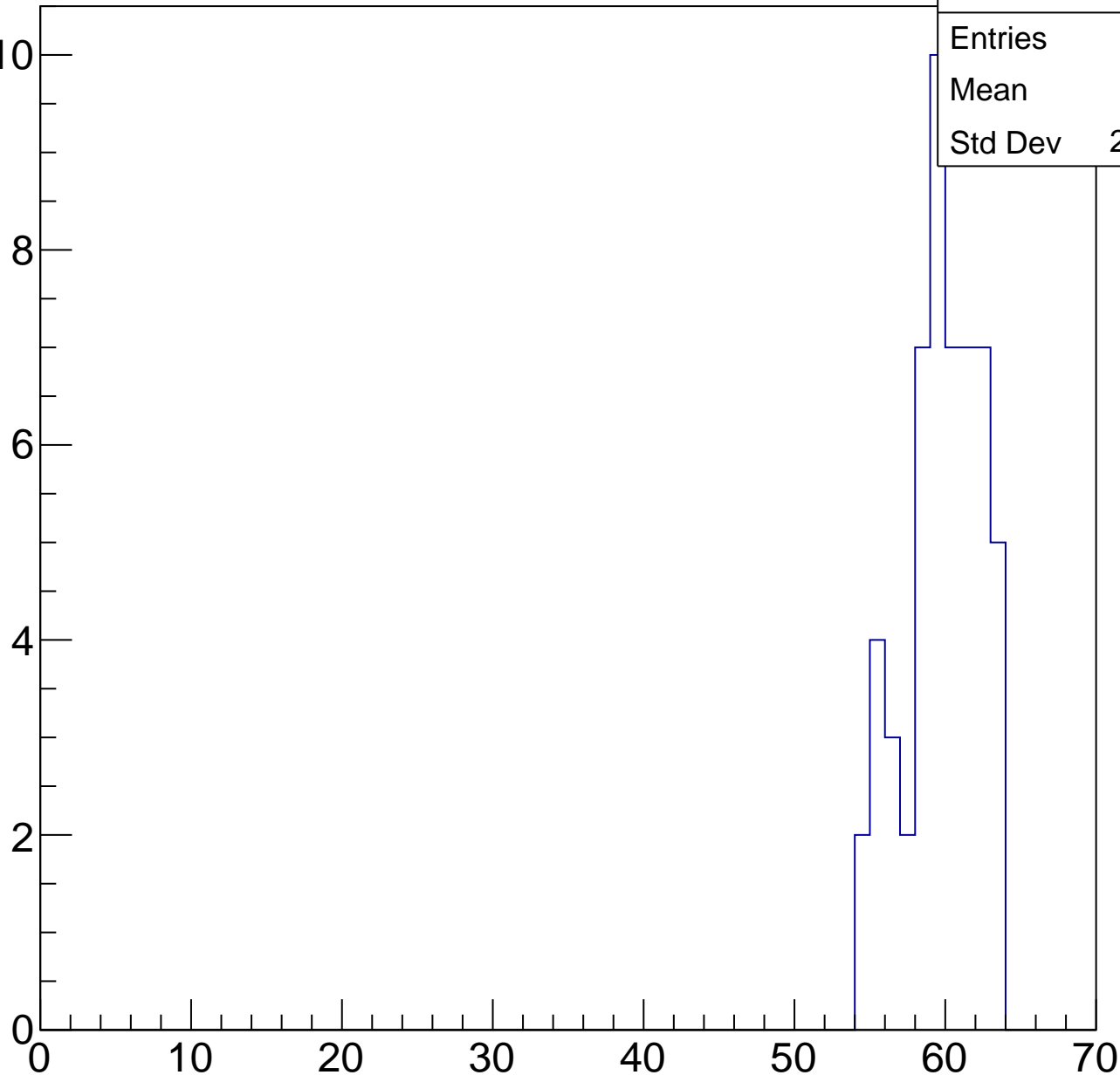
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

10  
8  
6  
4  
2  
0

Entries	54
Mean	59.3
Std Dev	2.469

ampl

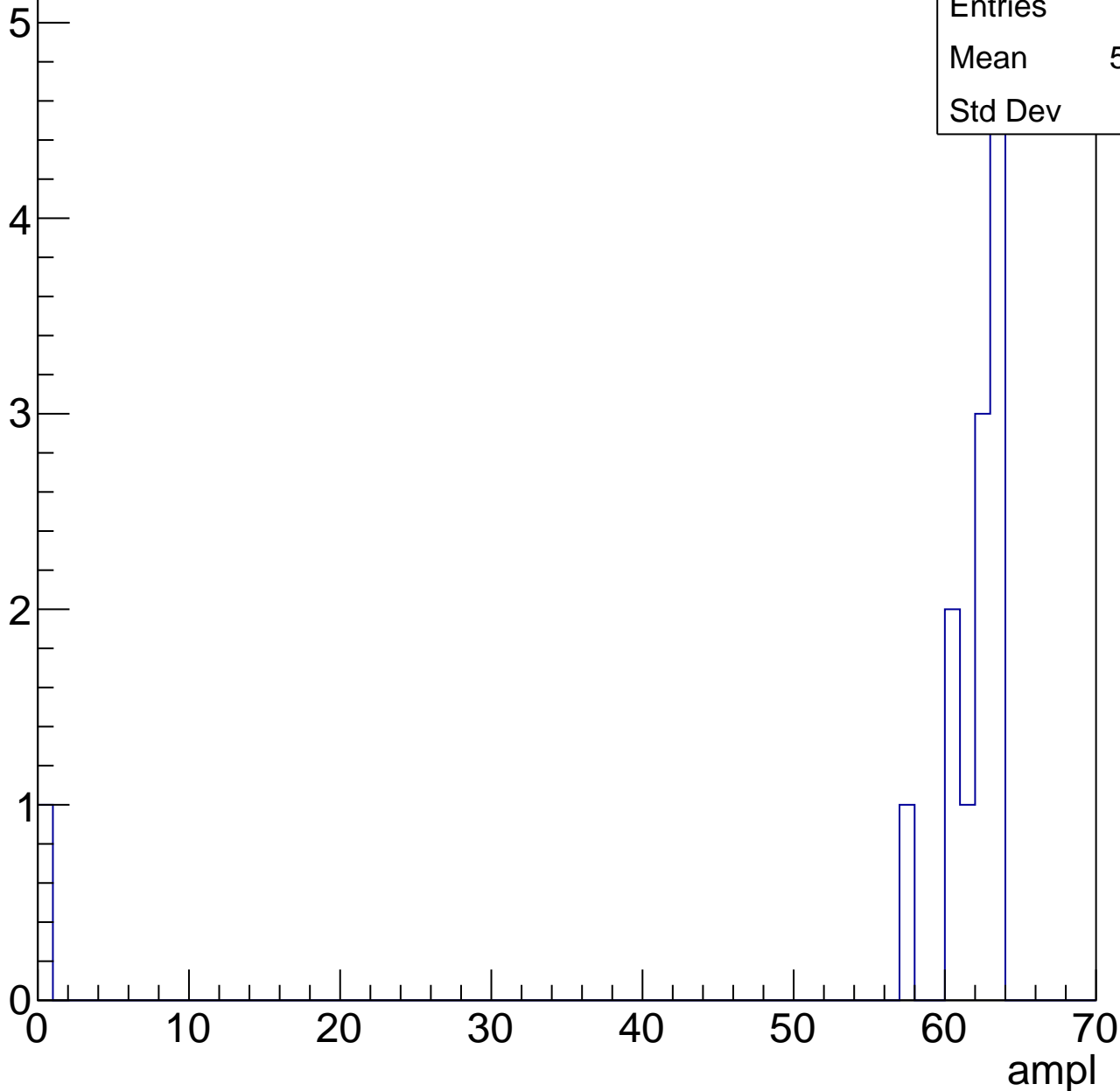


# B1L003S, U6-ch98, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	13
Mean	56.85
Std Dev	16.5

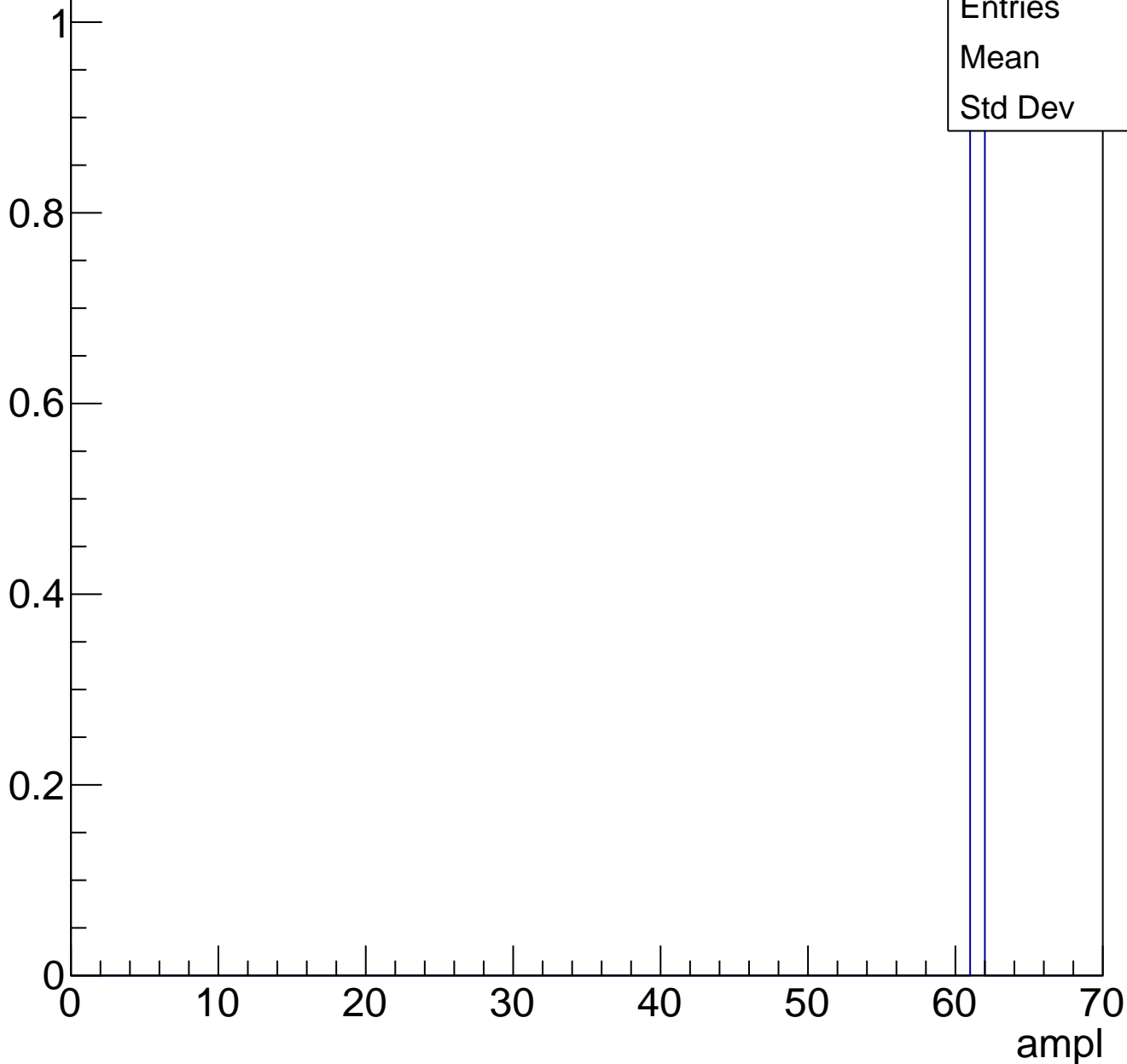




# B1L003S, U6-ch98, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch99, adc0

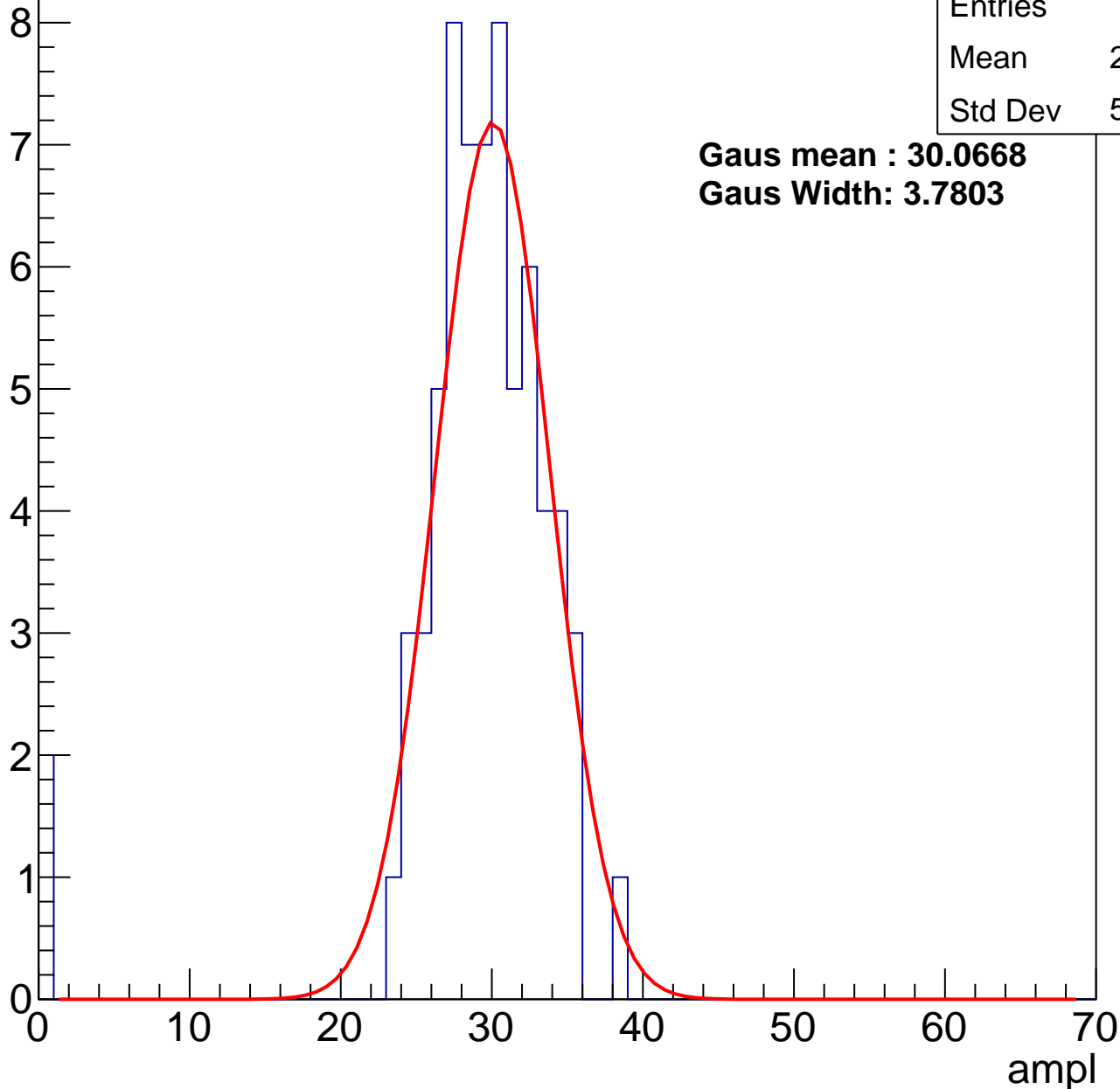
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	28.55
Std Dev	5.918

**Gaus mean : 30.0668**

**Gaus Width: 3.7803**



# B1L003S, U6-ch99, adc1

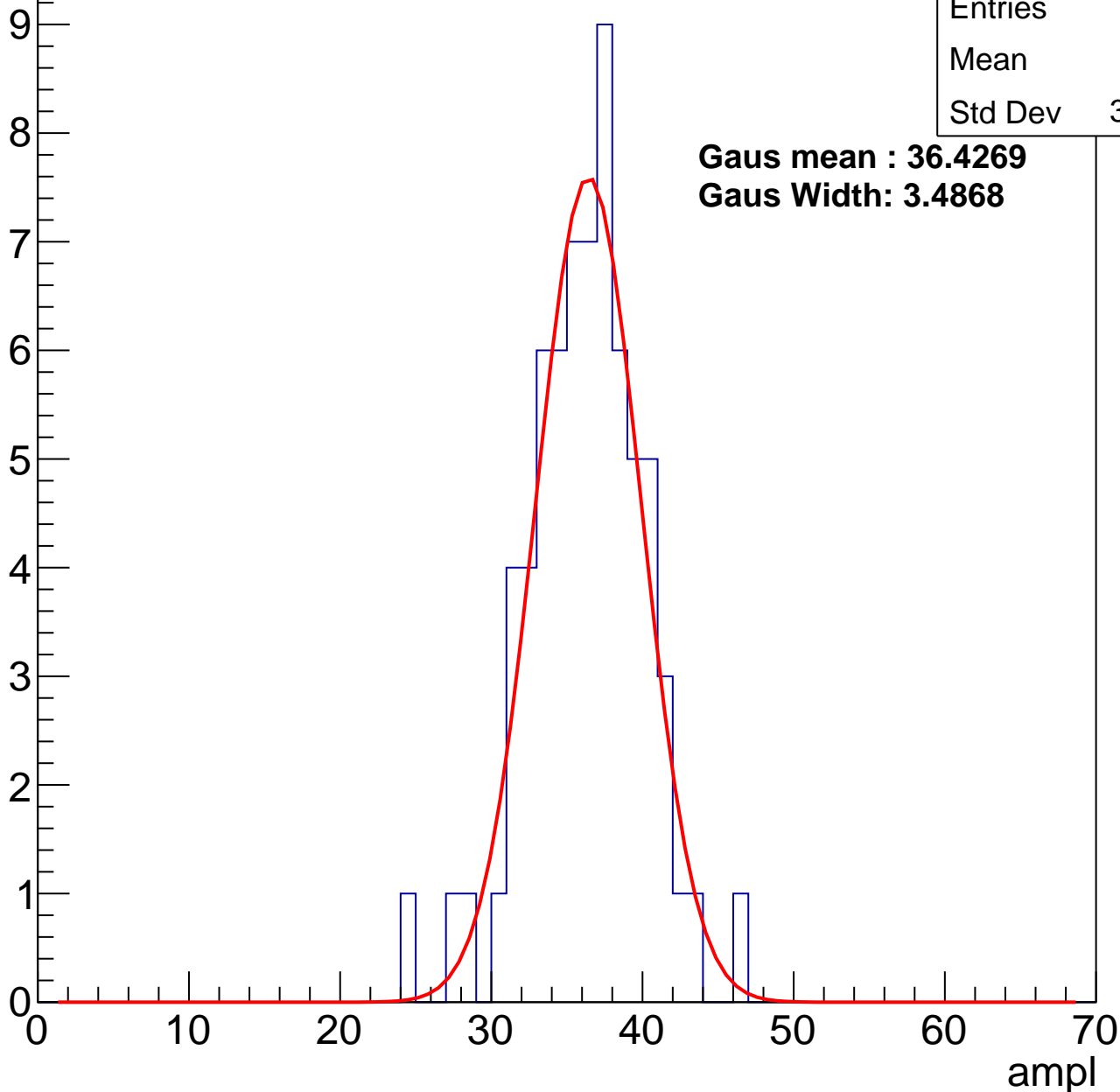
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	35.8
Std Dev	3.786

**Gaus mean : 36.4269**

**Gaus Width: 3.4868**



# B1L003S, U6-ch99, adc2

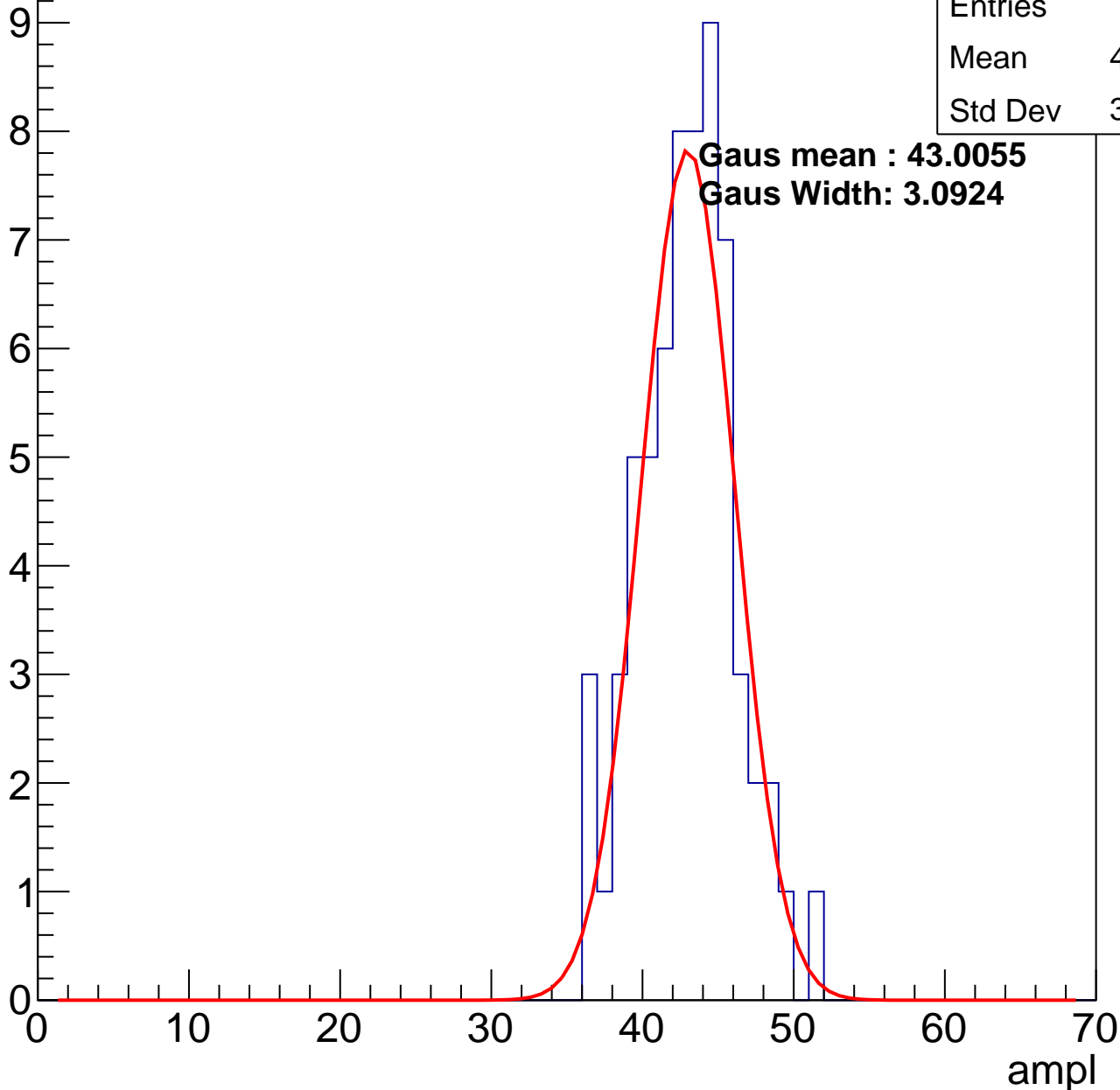
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	42.48
Std Dev	3.172

**Gaus mean : 43.0055**

**Gaus Width: 3.0924**

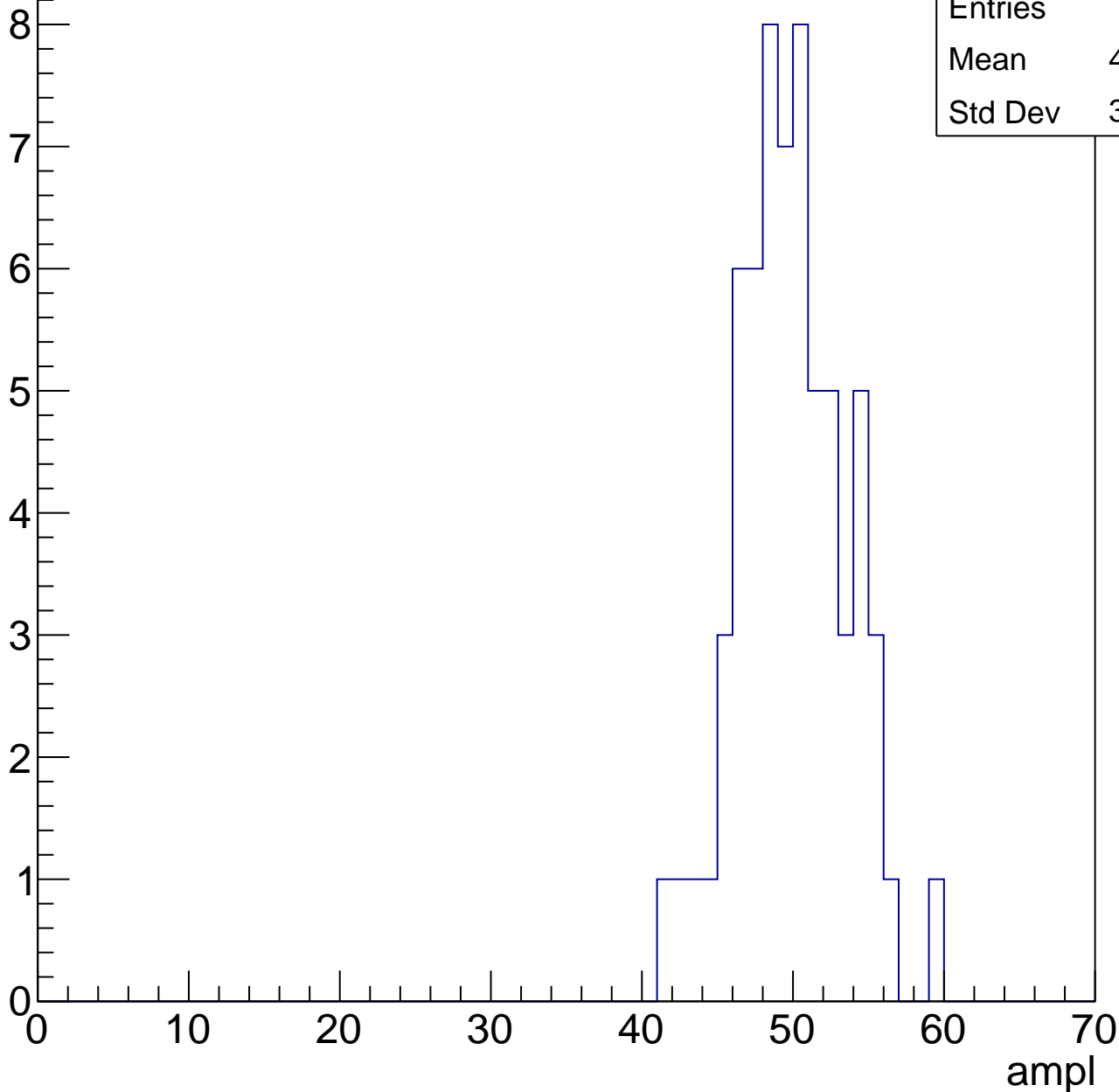


# B1L003S, U6-ch99, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	49.45
Std Dev	3.504

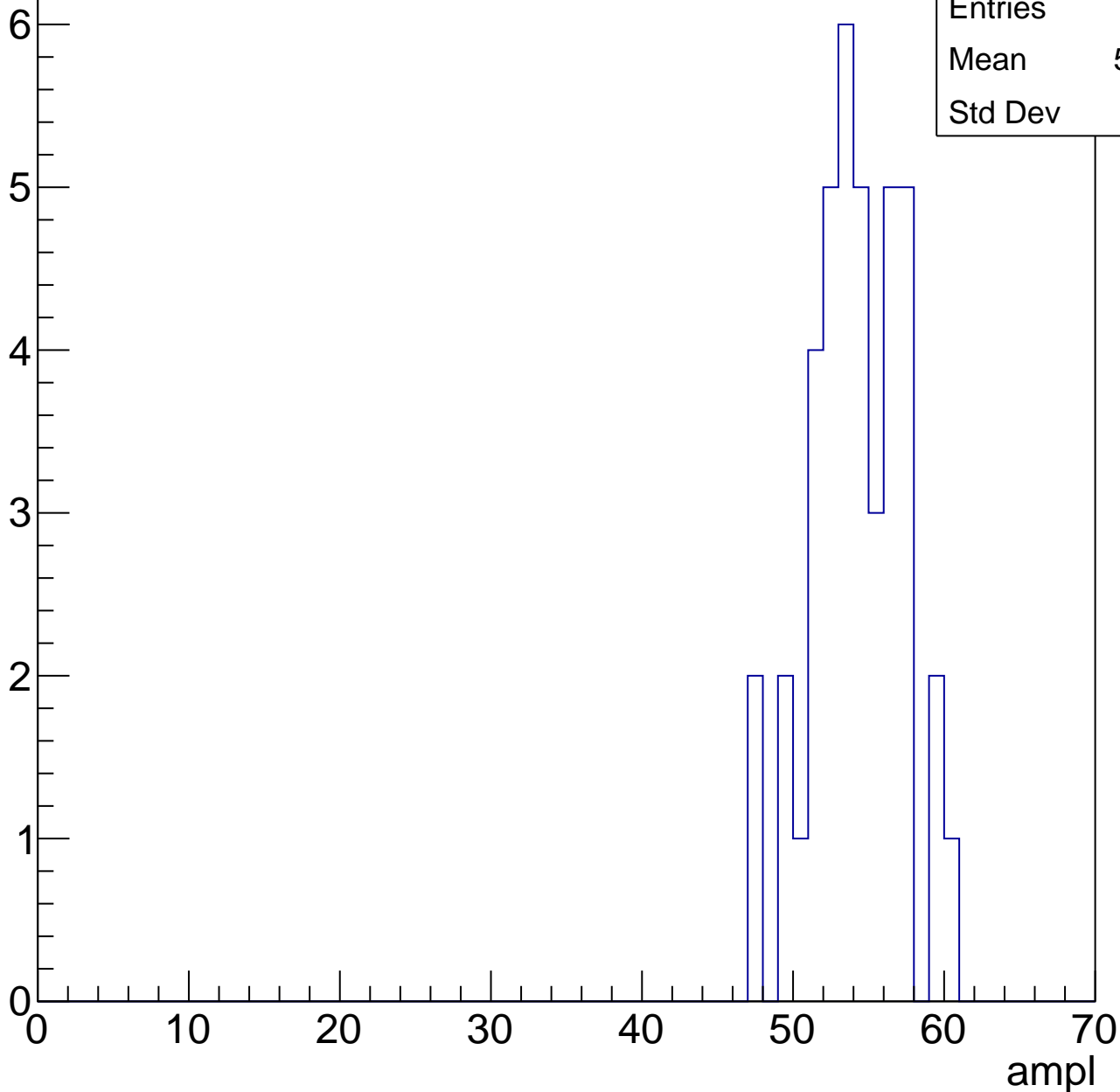


# B1L003S, U6-ch99, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	41
Mean	53.71
Std Dev	3.03

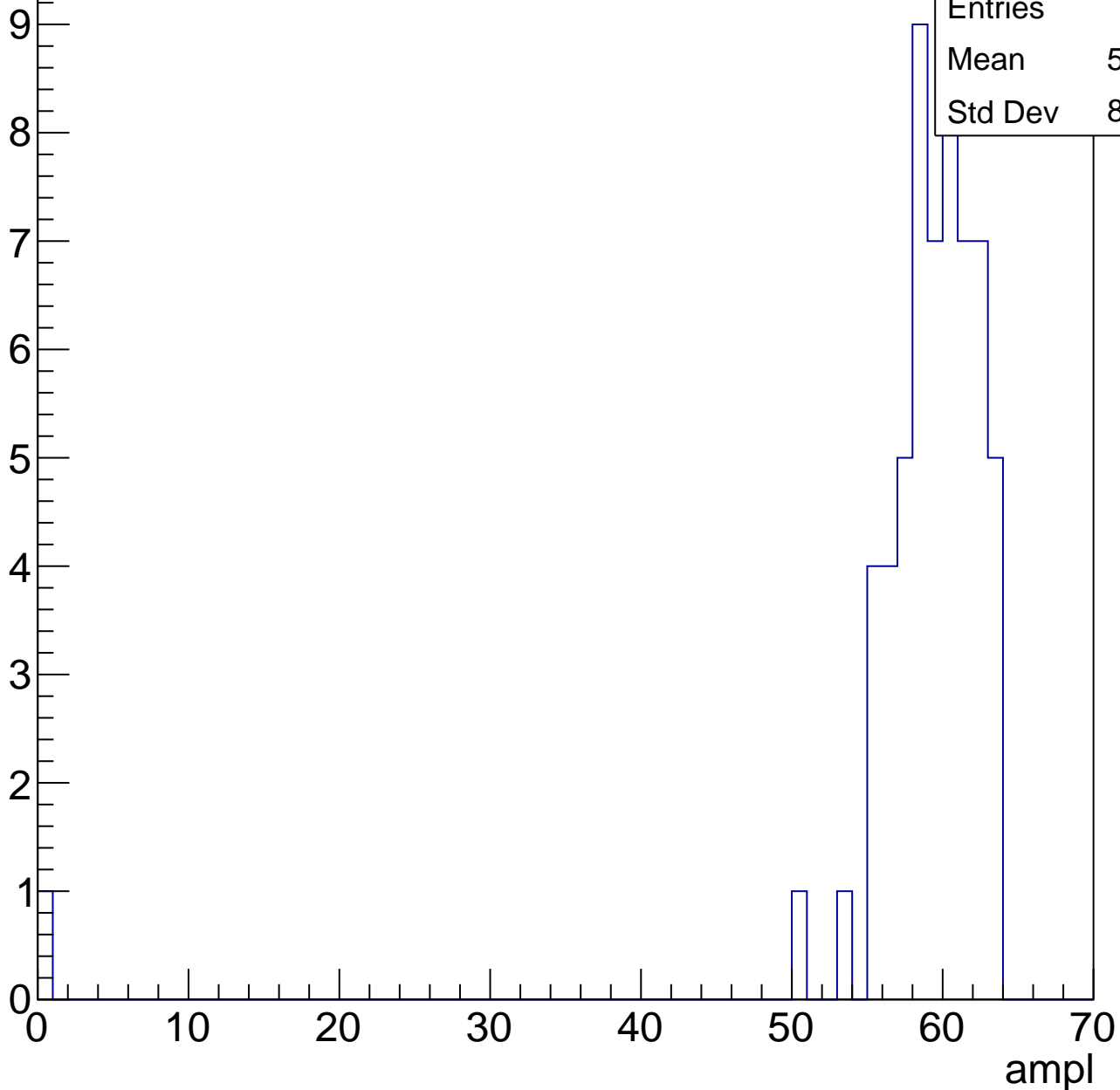


# B1L003S, U6-ch99, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

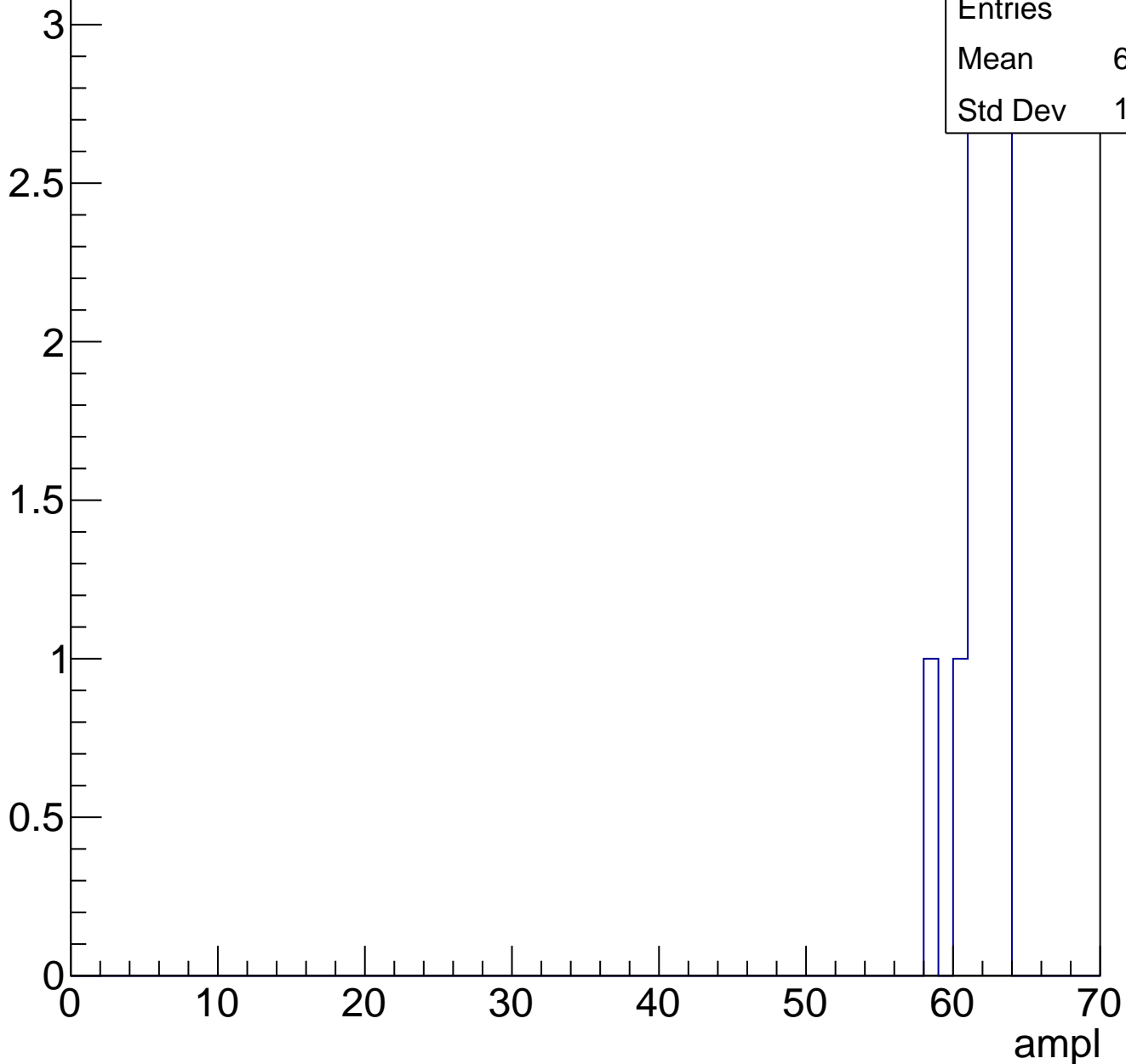
Entries	59
Mean	58.02
Std Dev	8.077



# B1L003S, U6-ch99, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch99, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch100, adc0

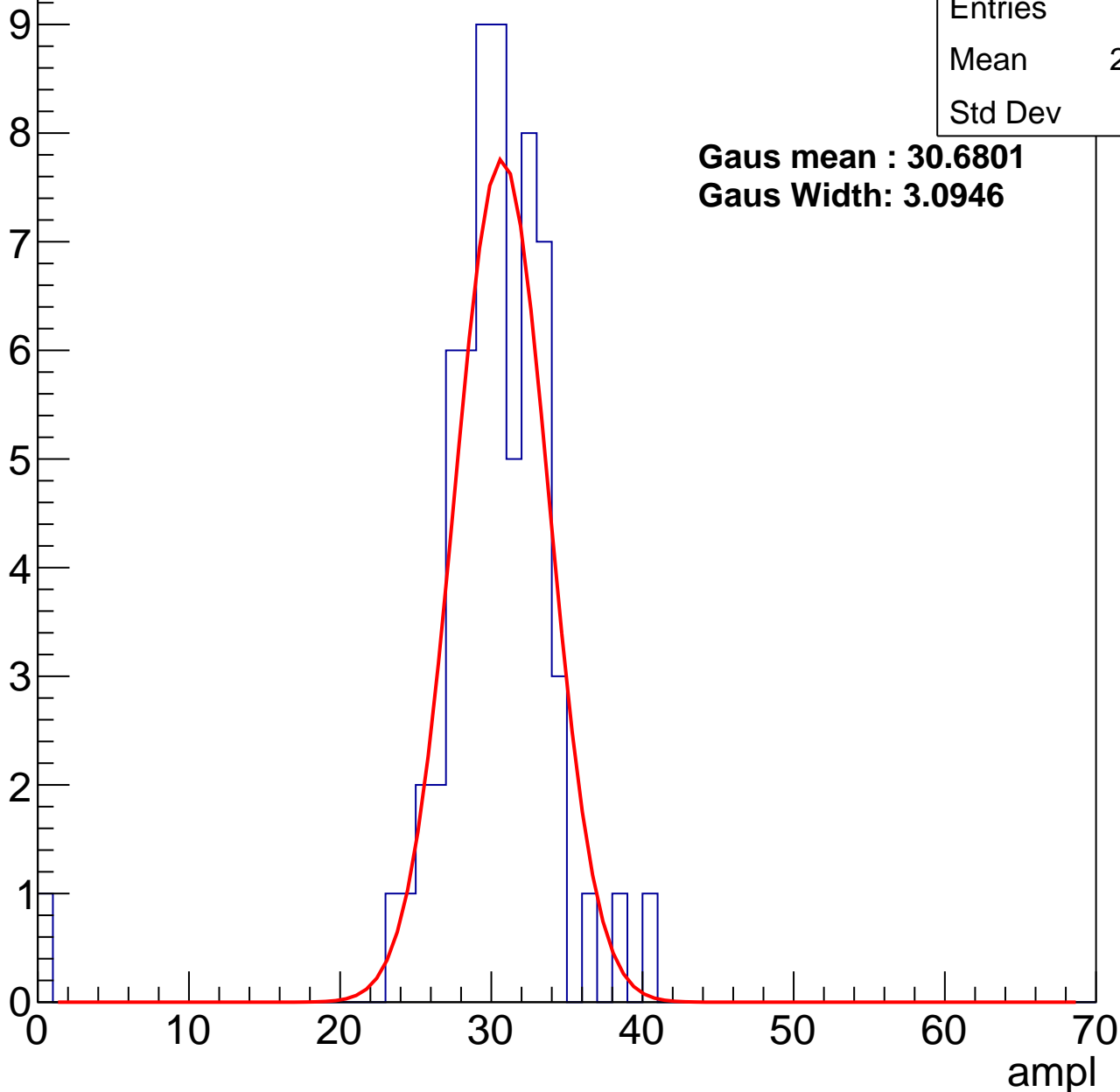
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	29.65
Std Dev	4.87

**Gaus mean : 30.6801**

**Gaus Width: 3.0946**



# B1L003S, U6-ch100, adc1

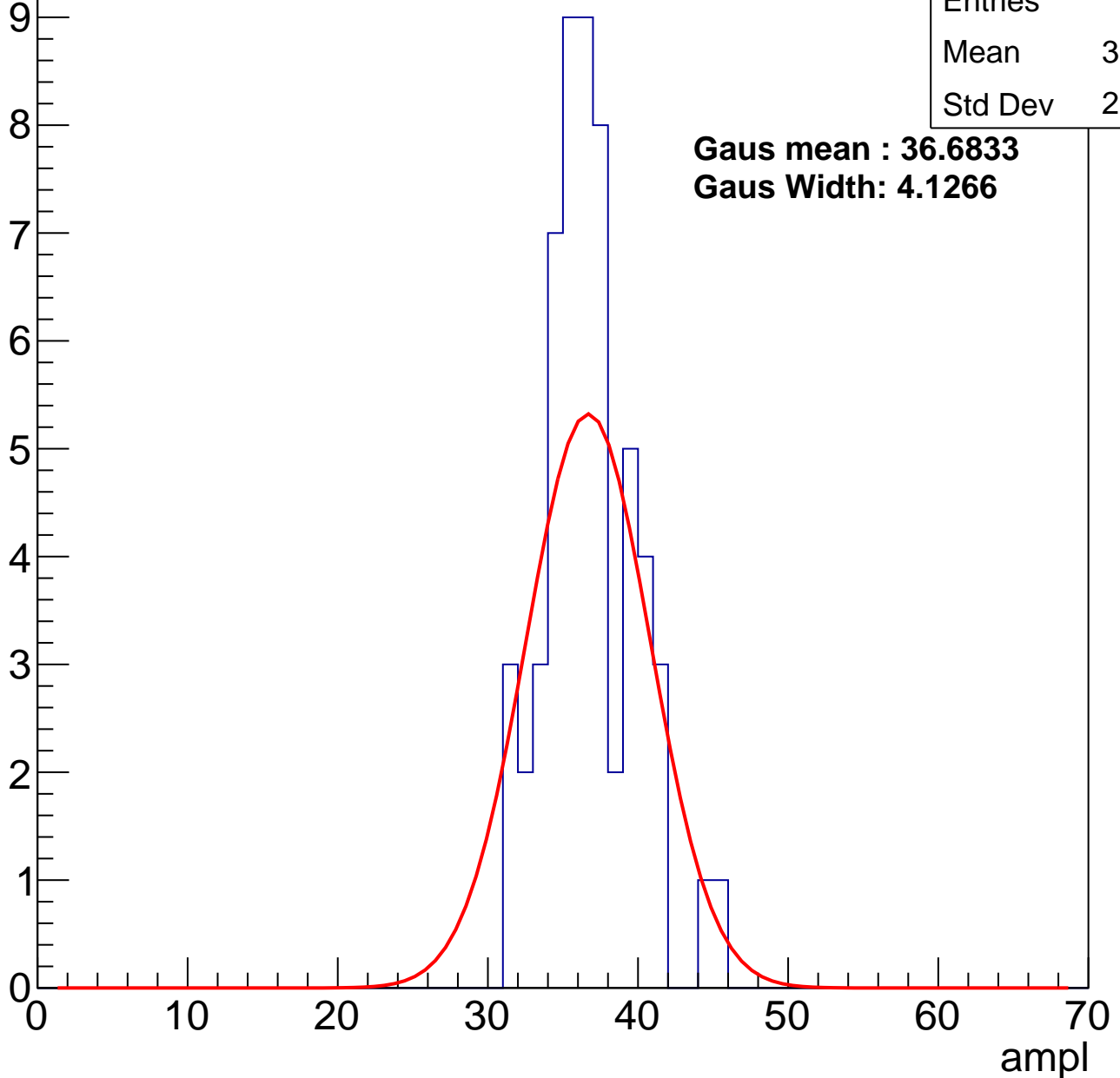
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	36.35
Std Dev	2.988

**Gaus mean : 36.6833**

**Gaus Width: 4.1266**



# B1L003S, U6-ch100, adc2

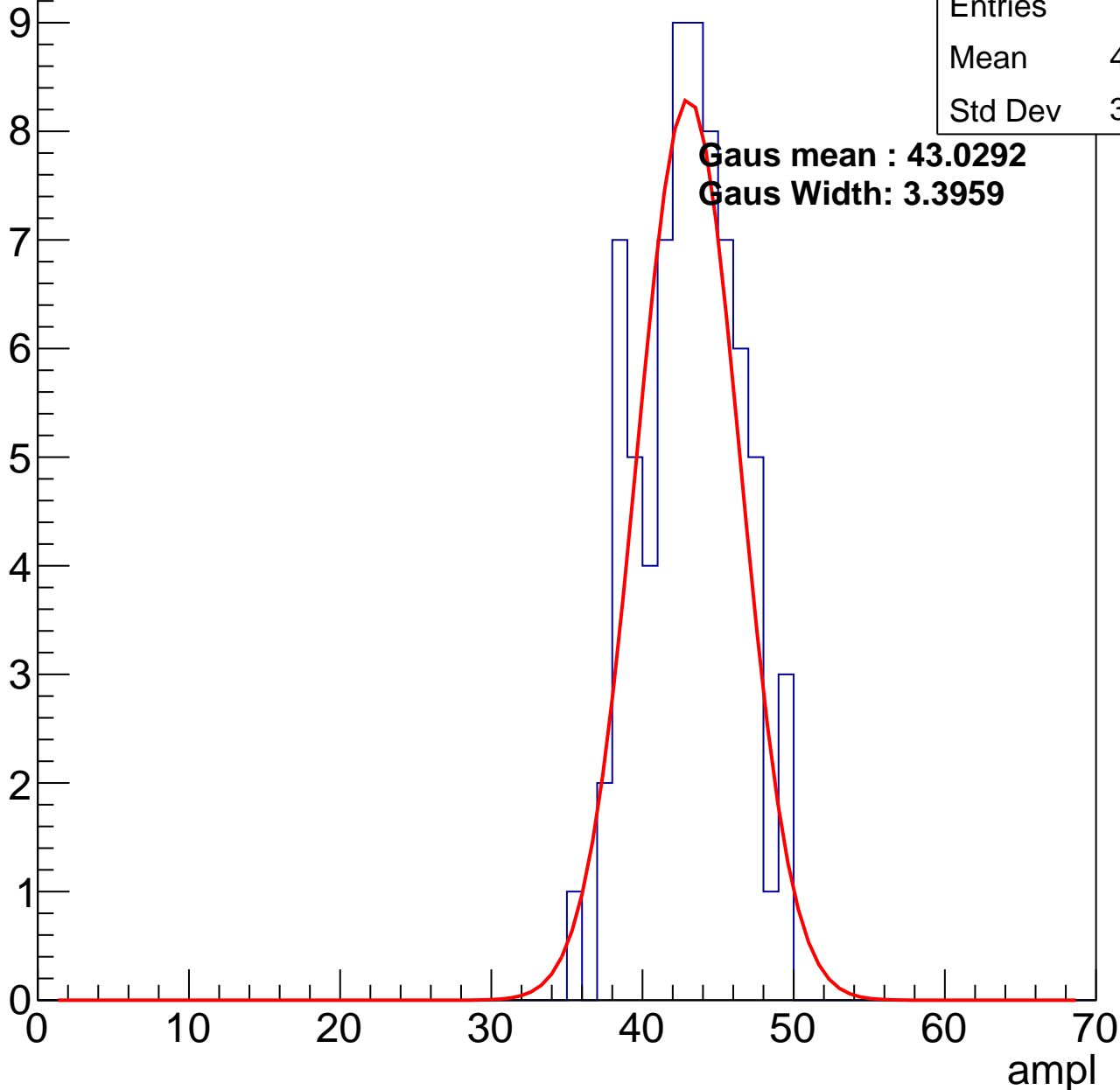
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	74
Mean	42.64
Std Dev	3.199

**Gaus mean : 43.0292**

**Gaus Width: 3.3959**

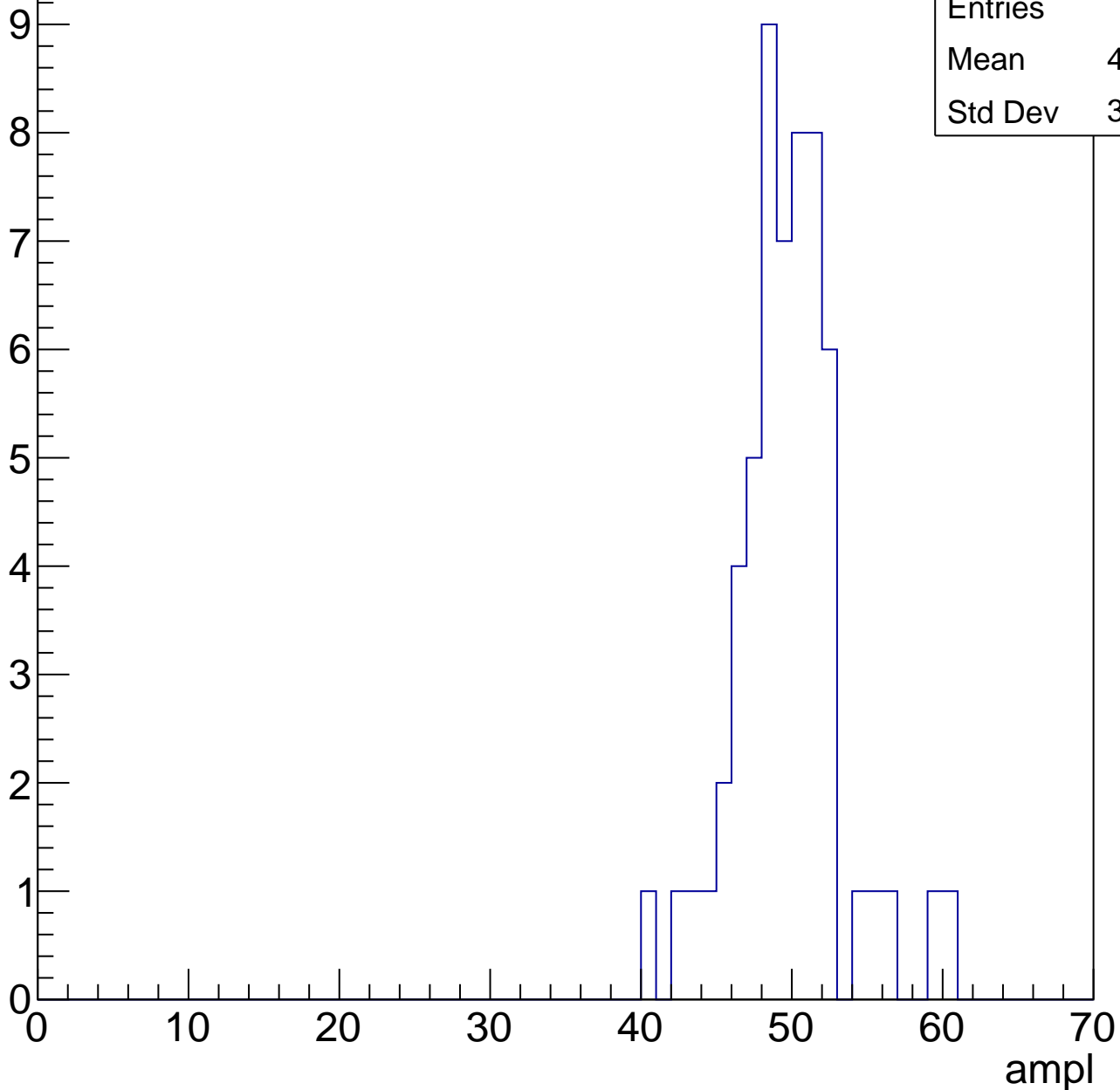


# B1L003S, U6-ch100, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	49.26
Std Dev	3.497



# B1L003S, U6-ch100, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	71
Mean	55.69
Std Dev	2.766

Entry

10

8

6

4

2

0

0

10

20

30

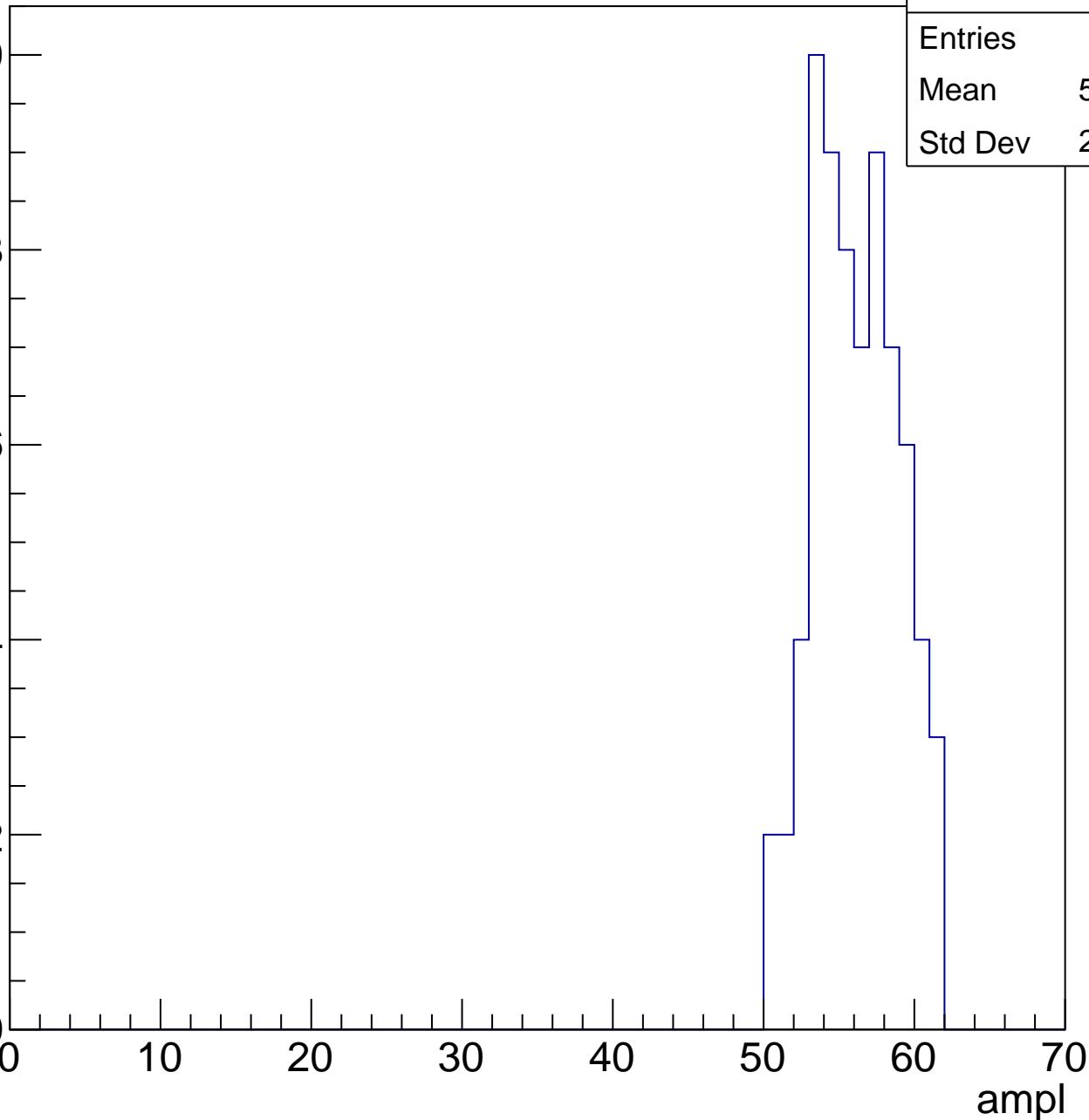
40

50

ampl

60

70

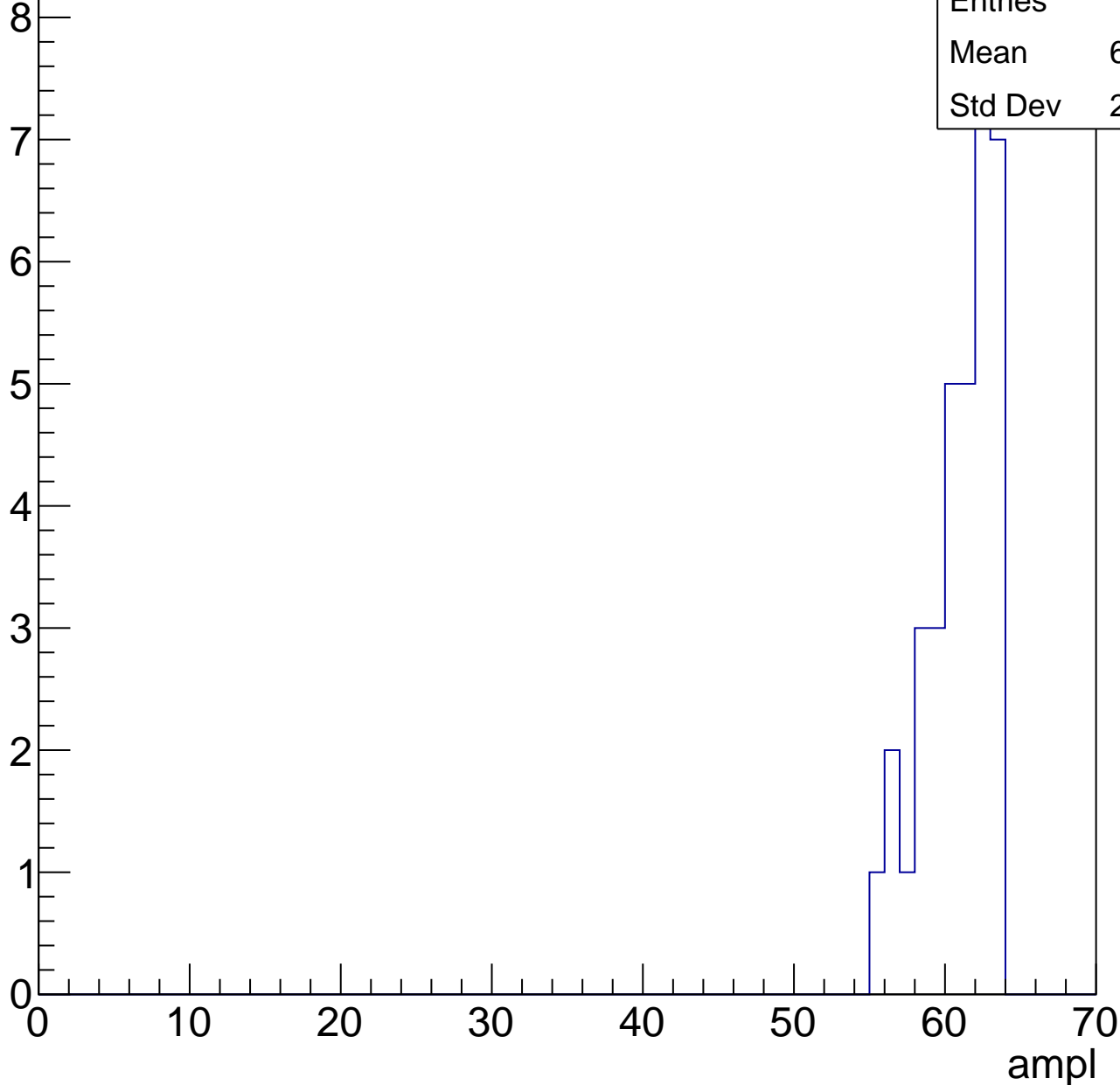


# B1L003S, U6-ch100, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

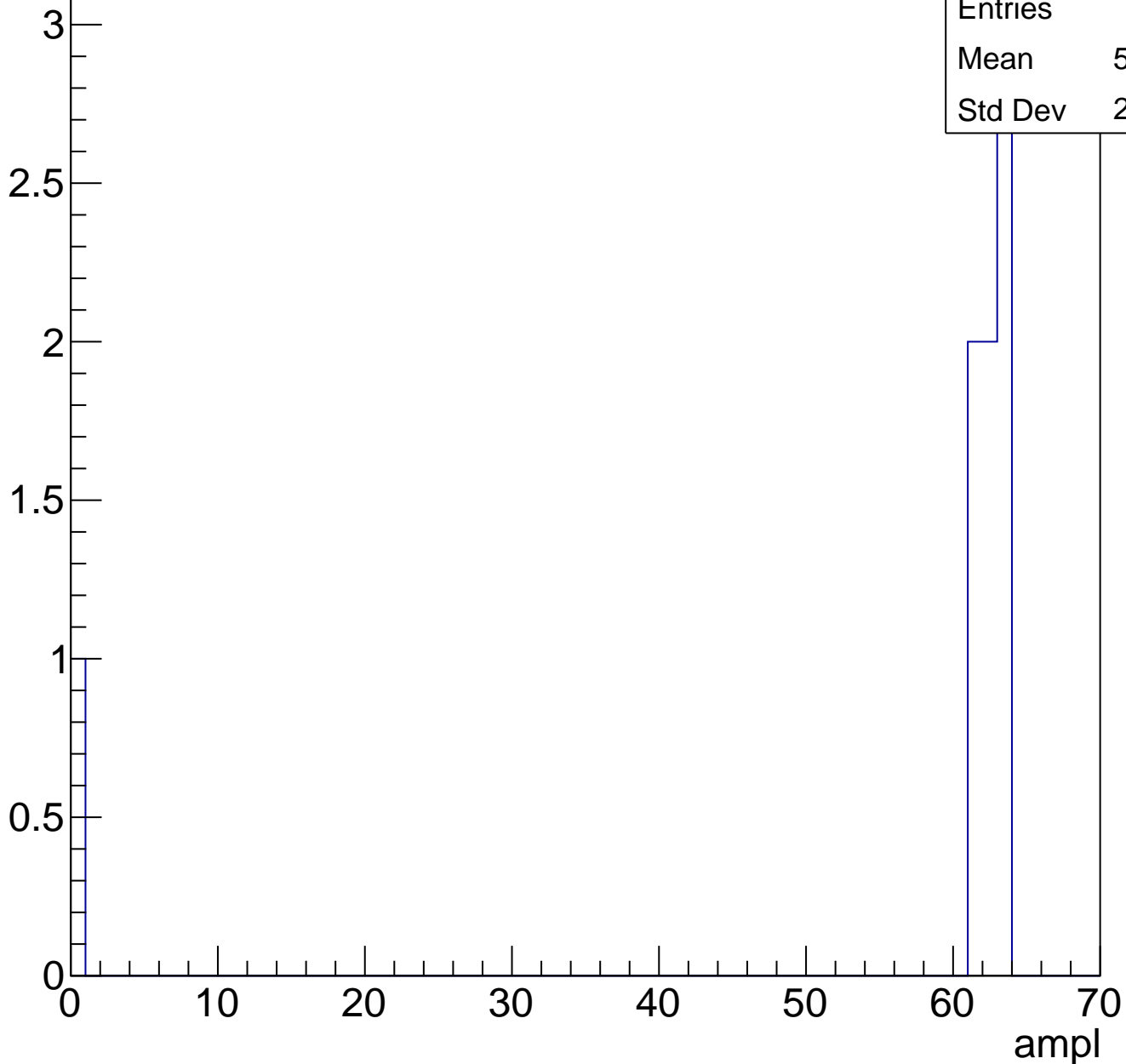
Entries	35
Mean	60.49
Std Dev	2.222



# B1L003S, U6-ch100, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch100, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch101, adc0

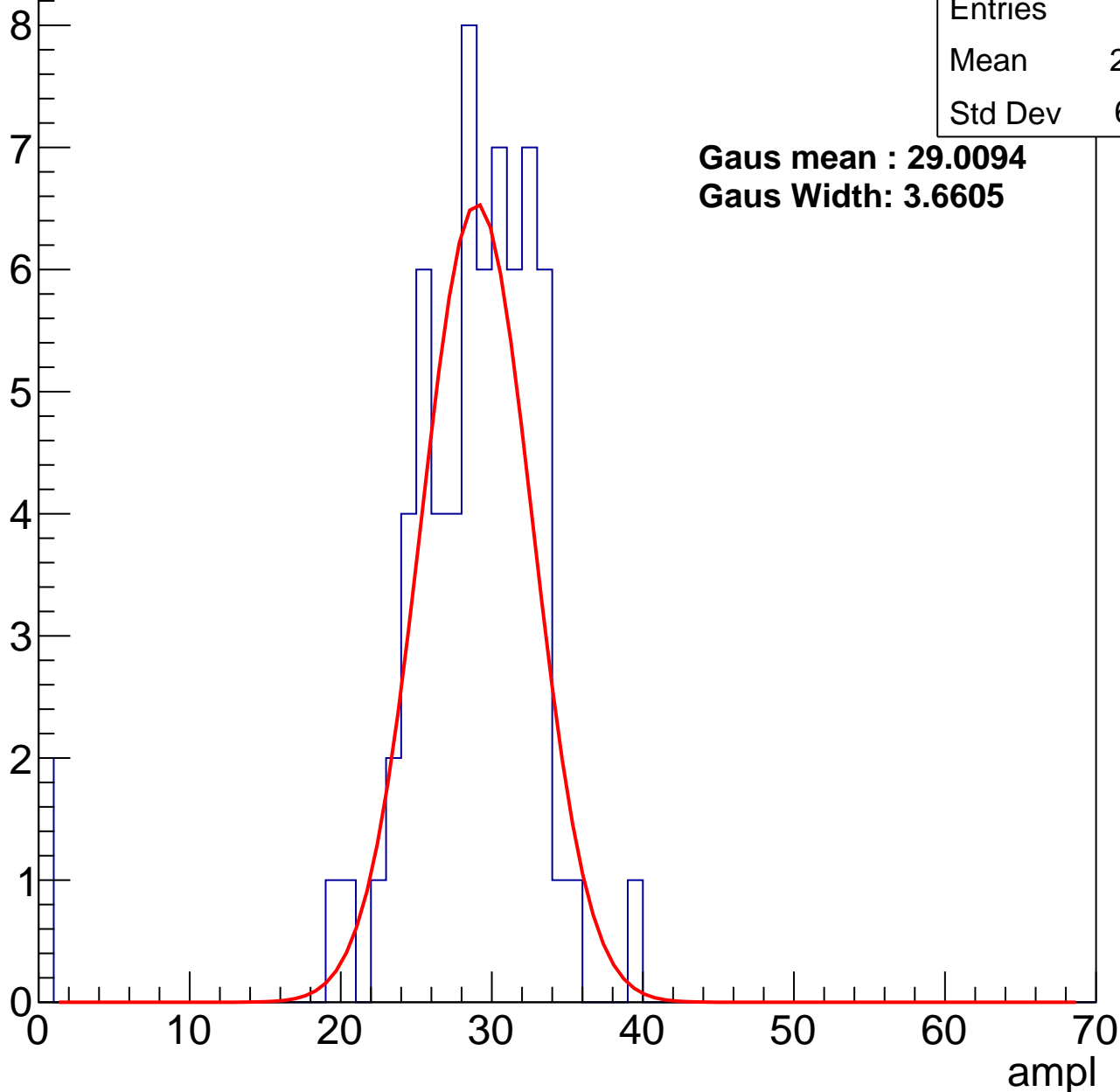
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	27.78
Std Dev	6.051

**Gaus mean : 29.0094**

**Gaus Width: 3.6605**



# B1L003S, U6-ch101, adc1

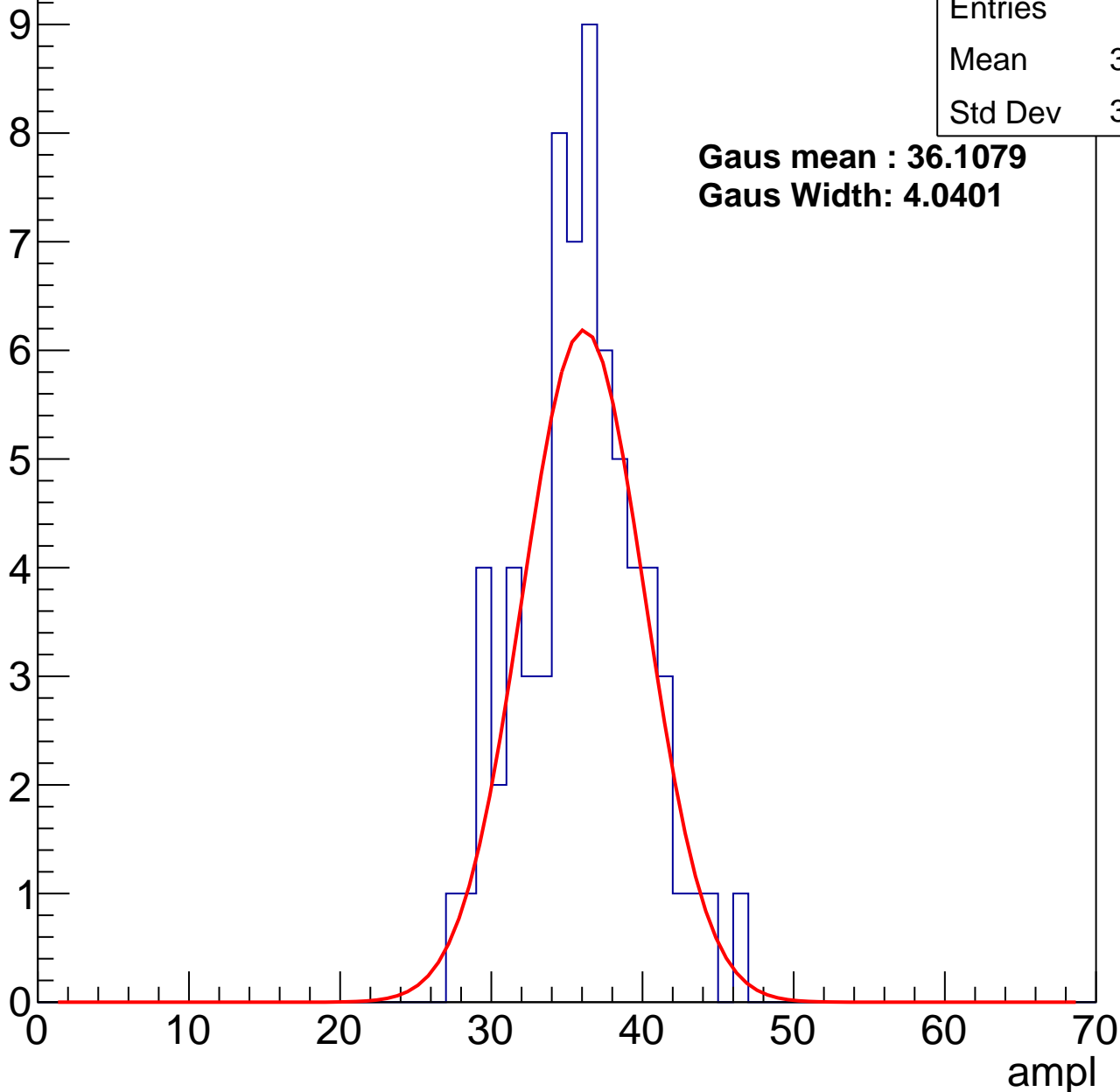
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	35.54
Std Dev	3.954

**Gaus mean : 36.1079**

**Gaus Width: 4.0401**



# B1L003S, U6-ch101, adc2

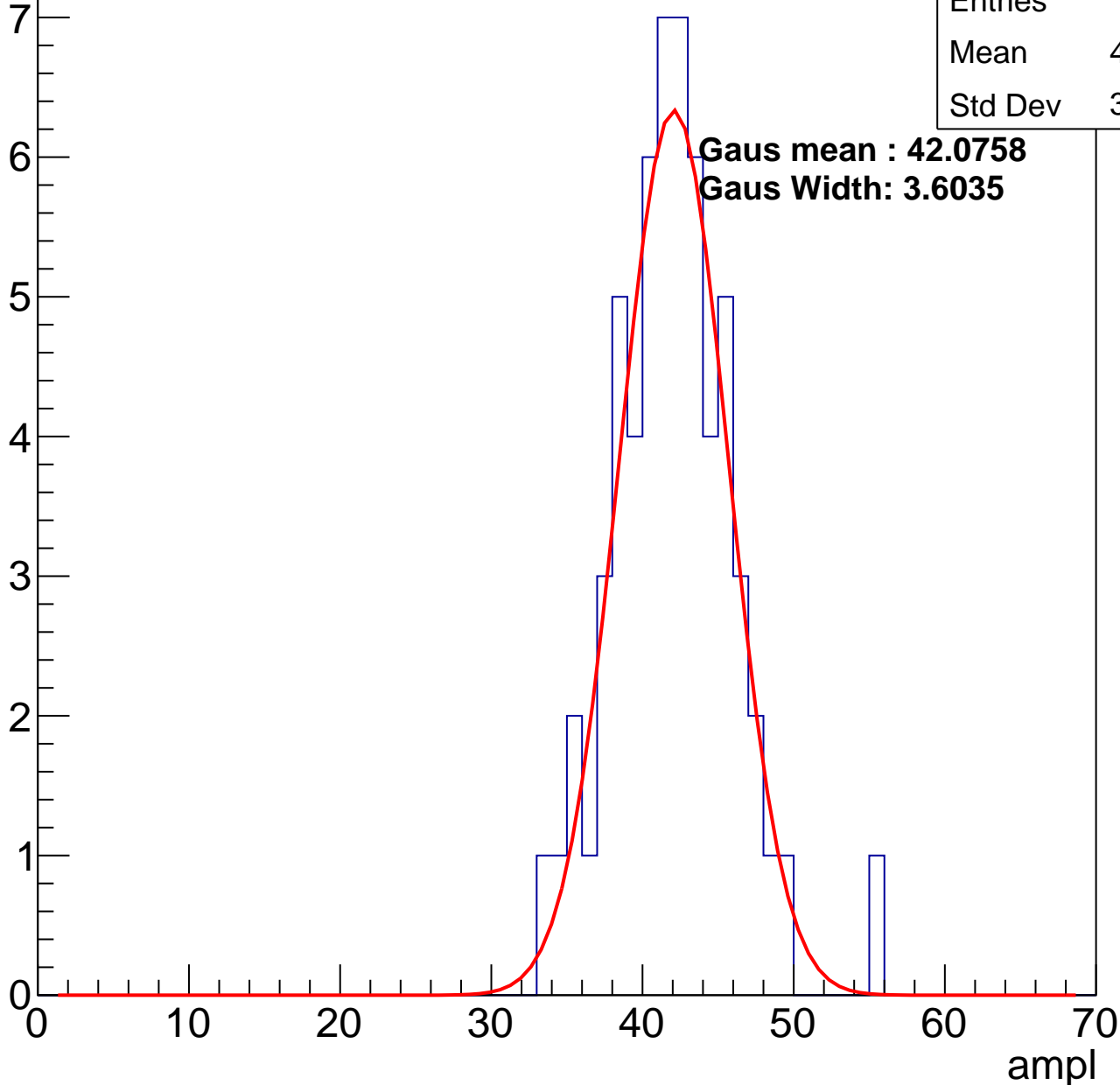
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	41.57
Std Dev	3.892

**Gaus mean : 42.0758**

**Gaus Width: 3.6035**

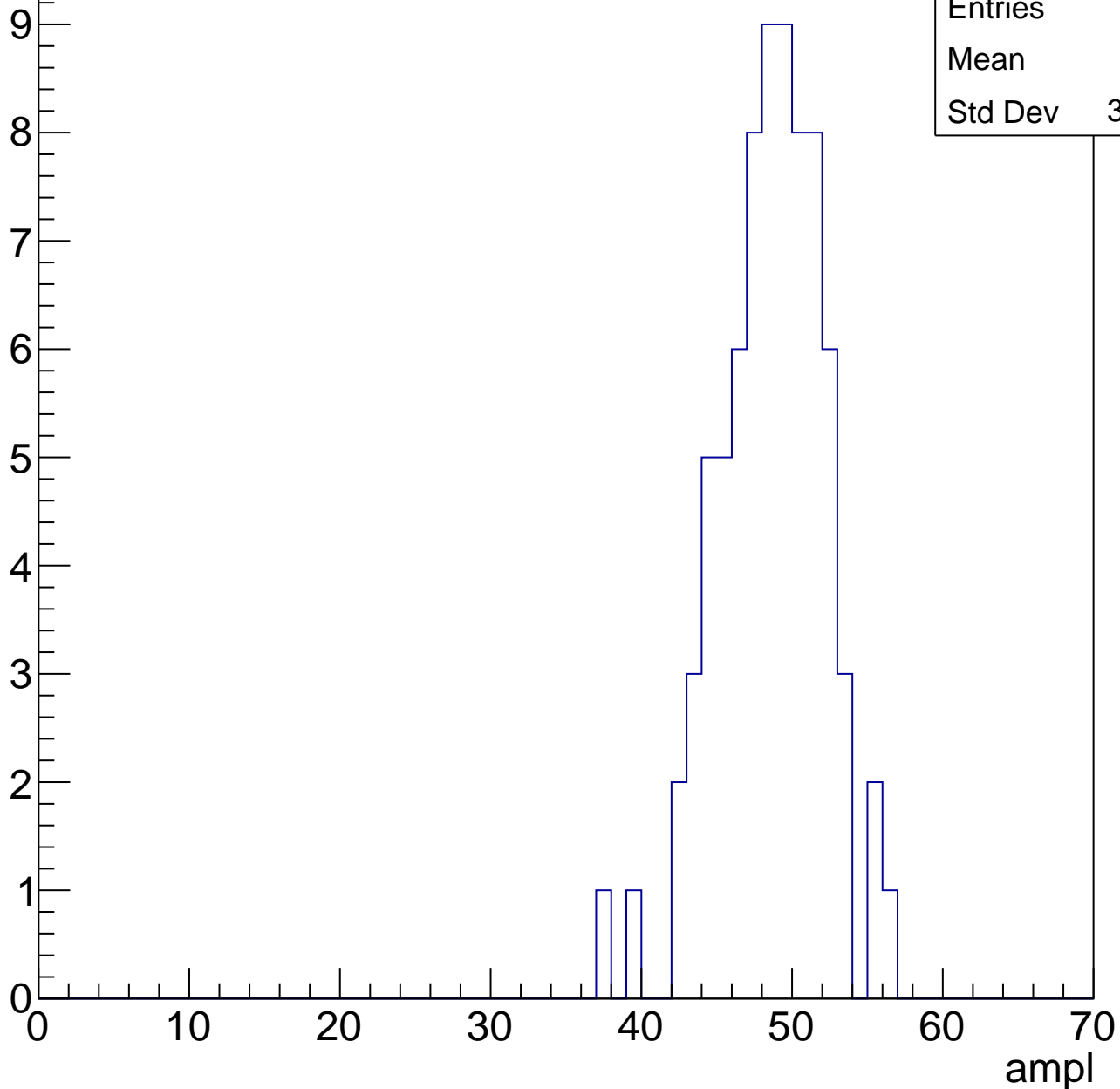


# B1L003S, U6-ch101, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	77
Mean	48.1
Std Dev	3.515



# B1L003S, U6-ch101, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	44
Mean	54.66
Std Dev	2.44

Entry

10

8

6

4

2

0

0

10

20

30

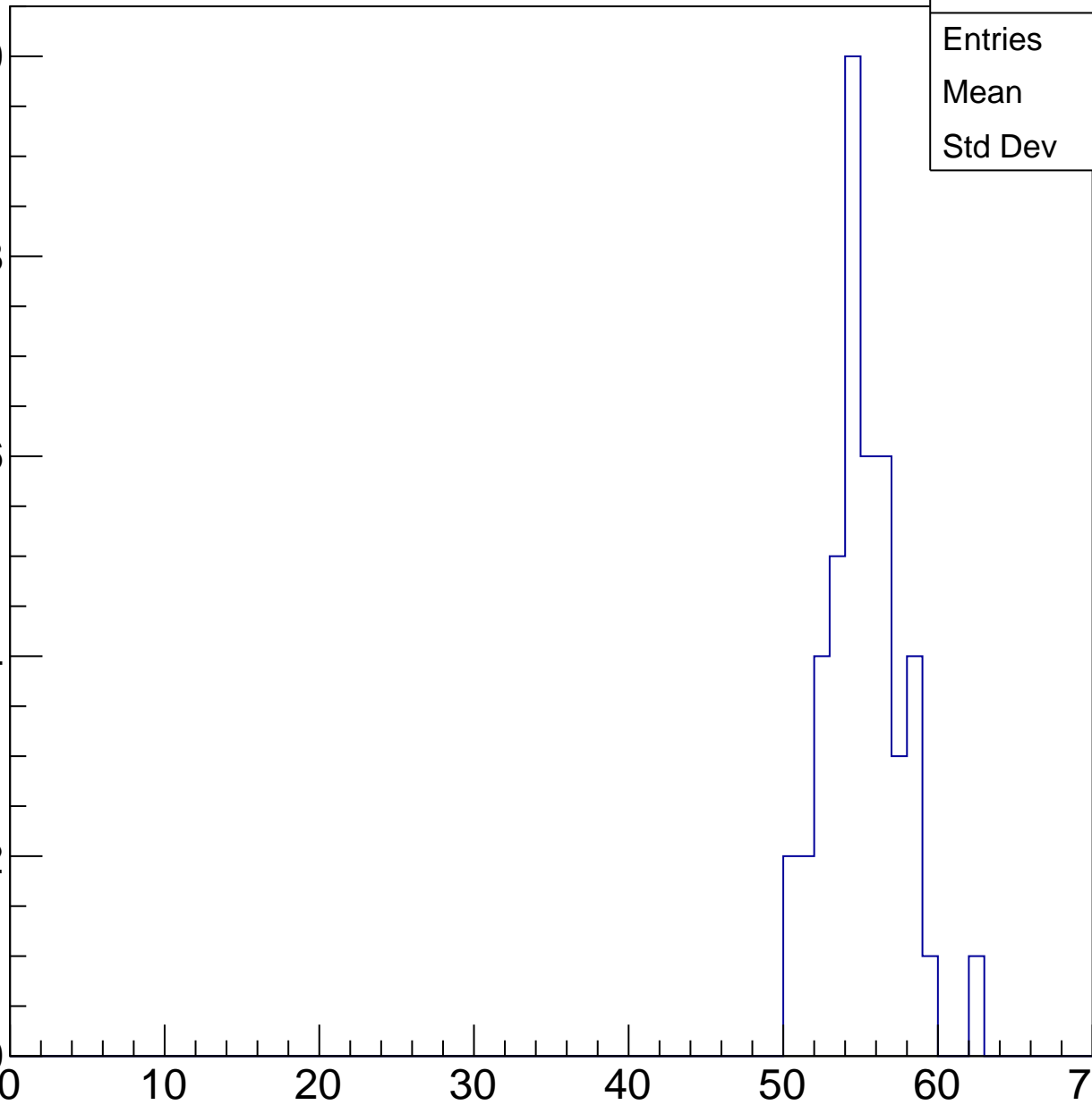
40

50

60

70

ampl

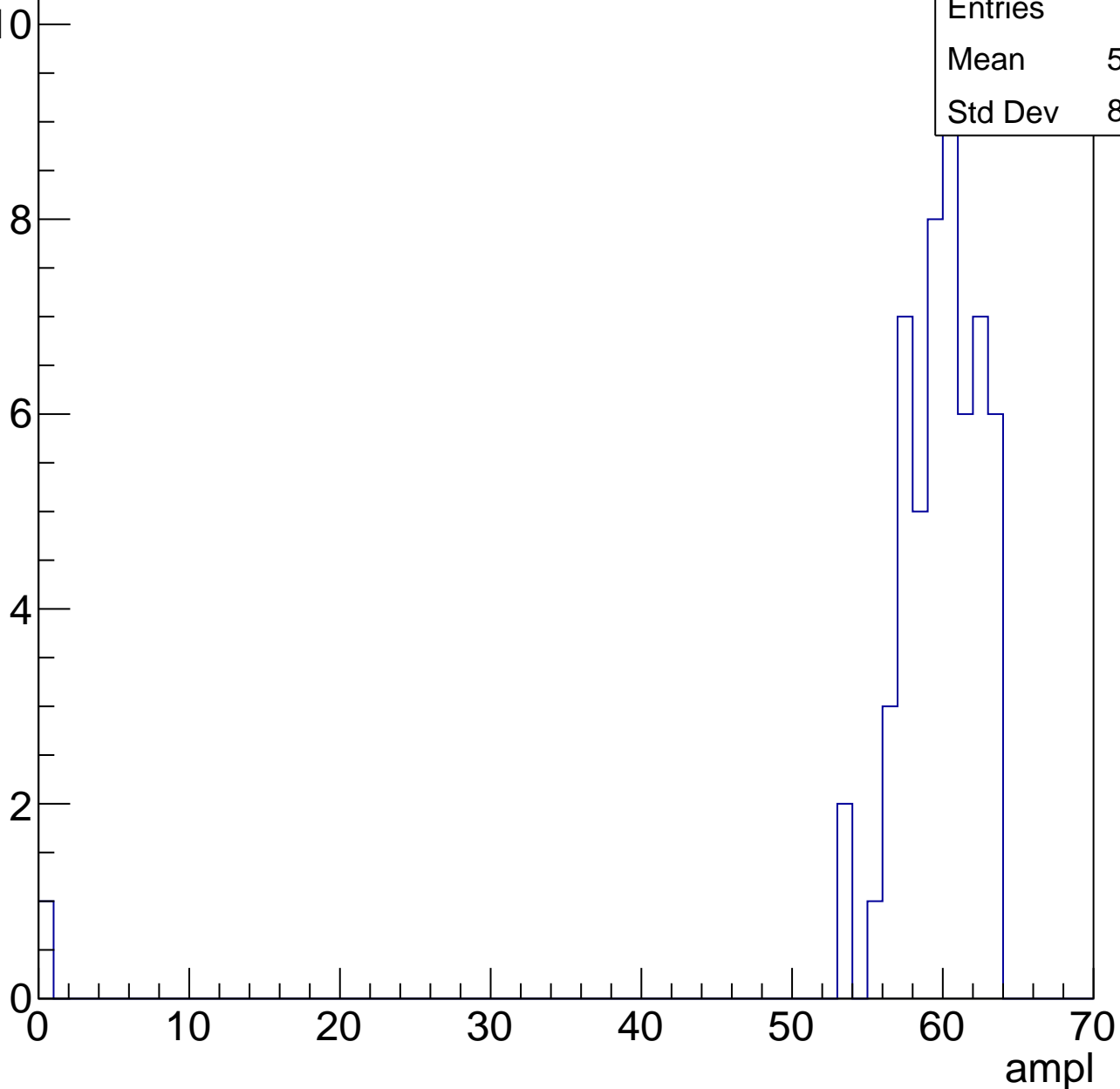


# B1L003S, U6-ch101, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

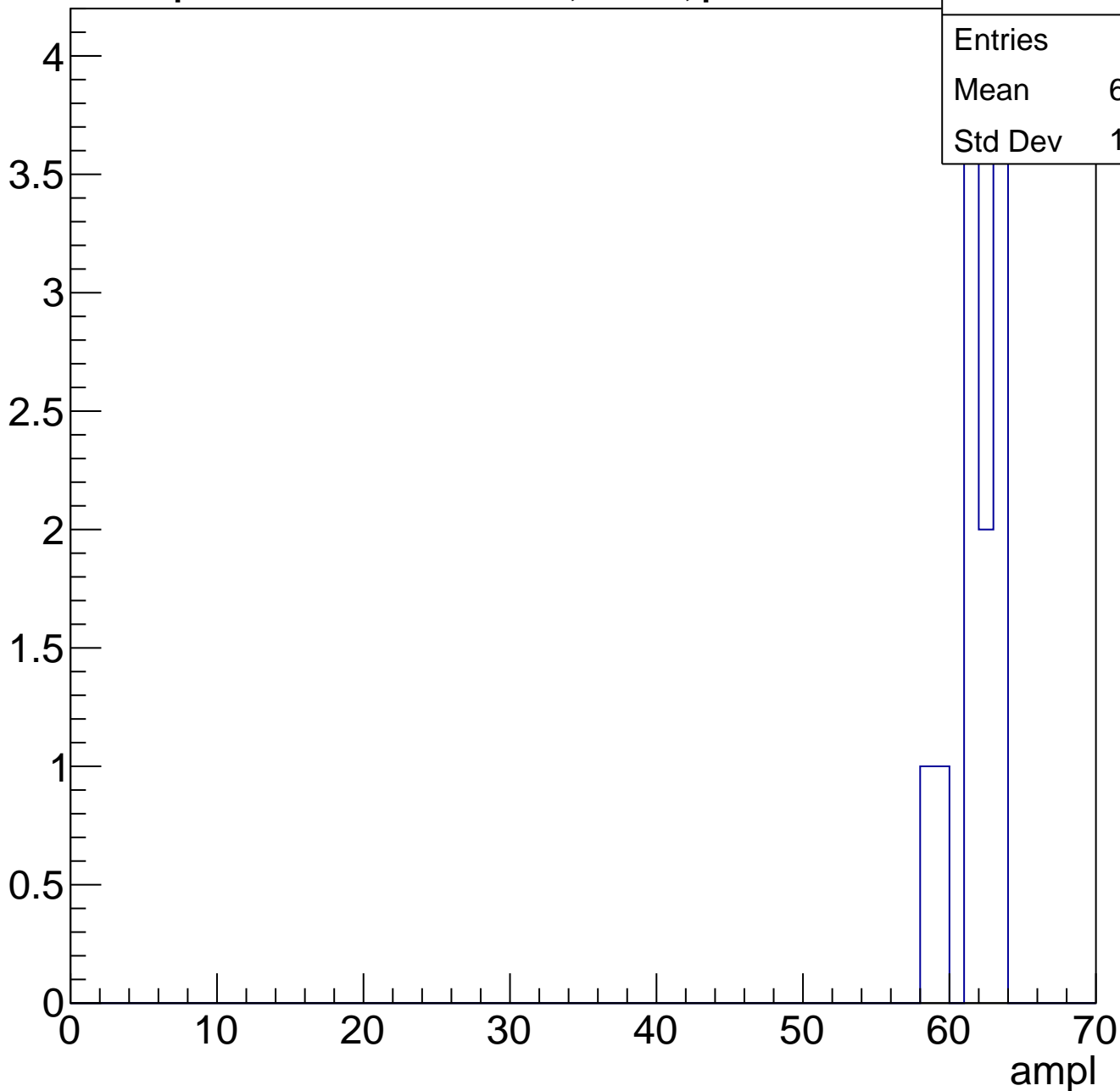
Entries	56
Mean	58.36
Std Dev	8.236



# B1L003S, U6-ch101, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch101, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch102, adc0

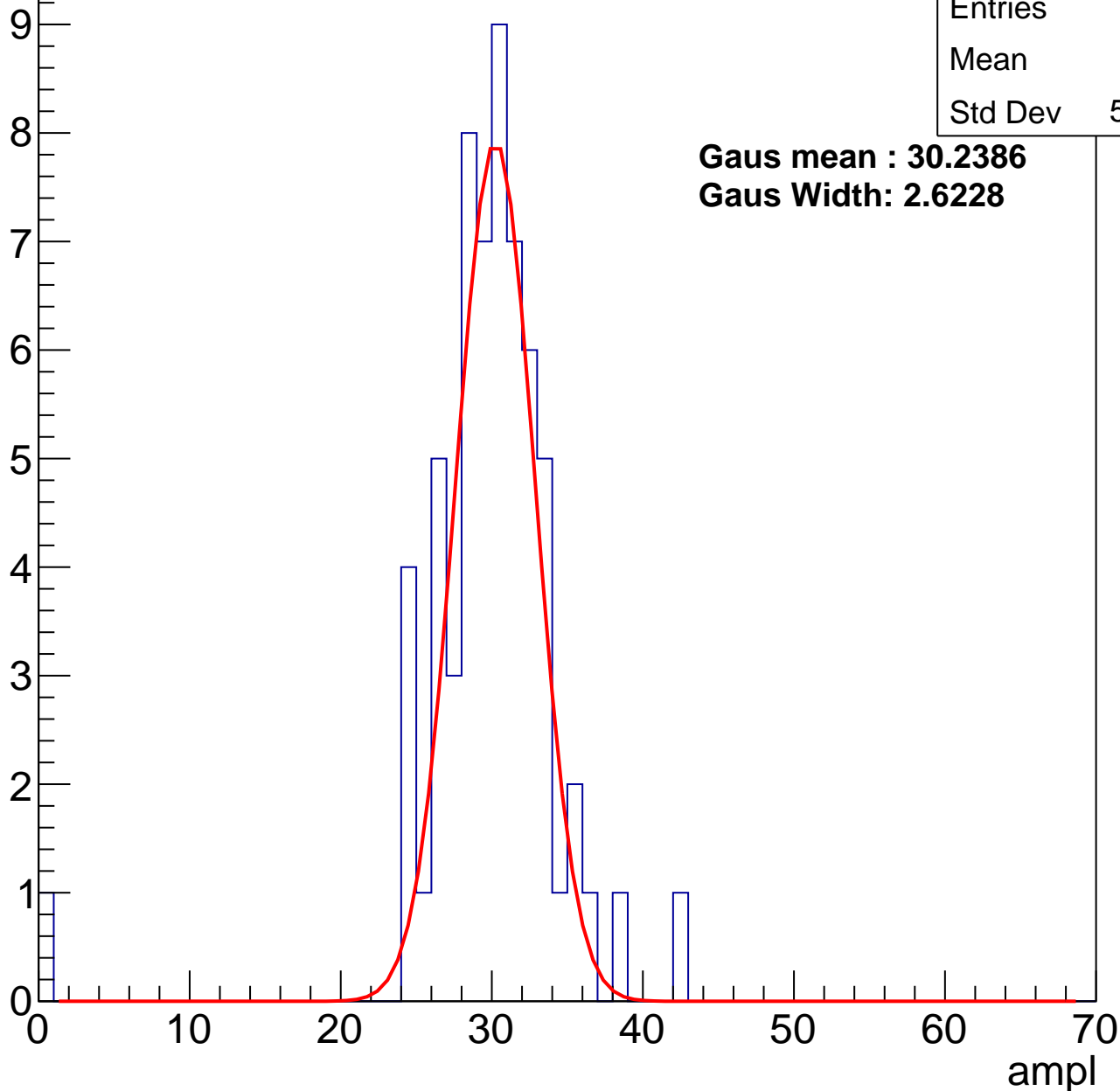
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	29.4
Std Dev	5.046

**Gaus mean : 30.2386**

**Gaus Width: 2.6228**



# B1L003S, U6-ch102, adc1

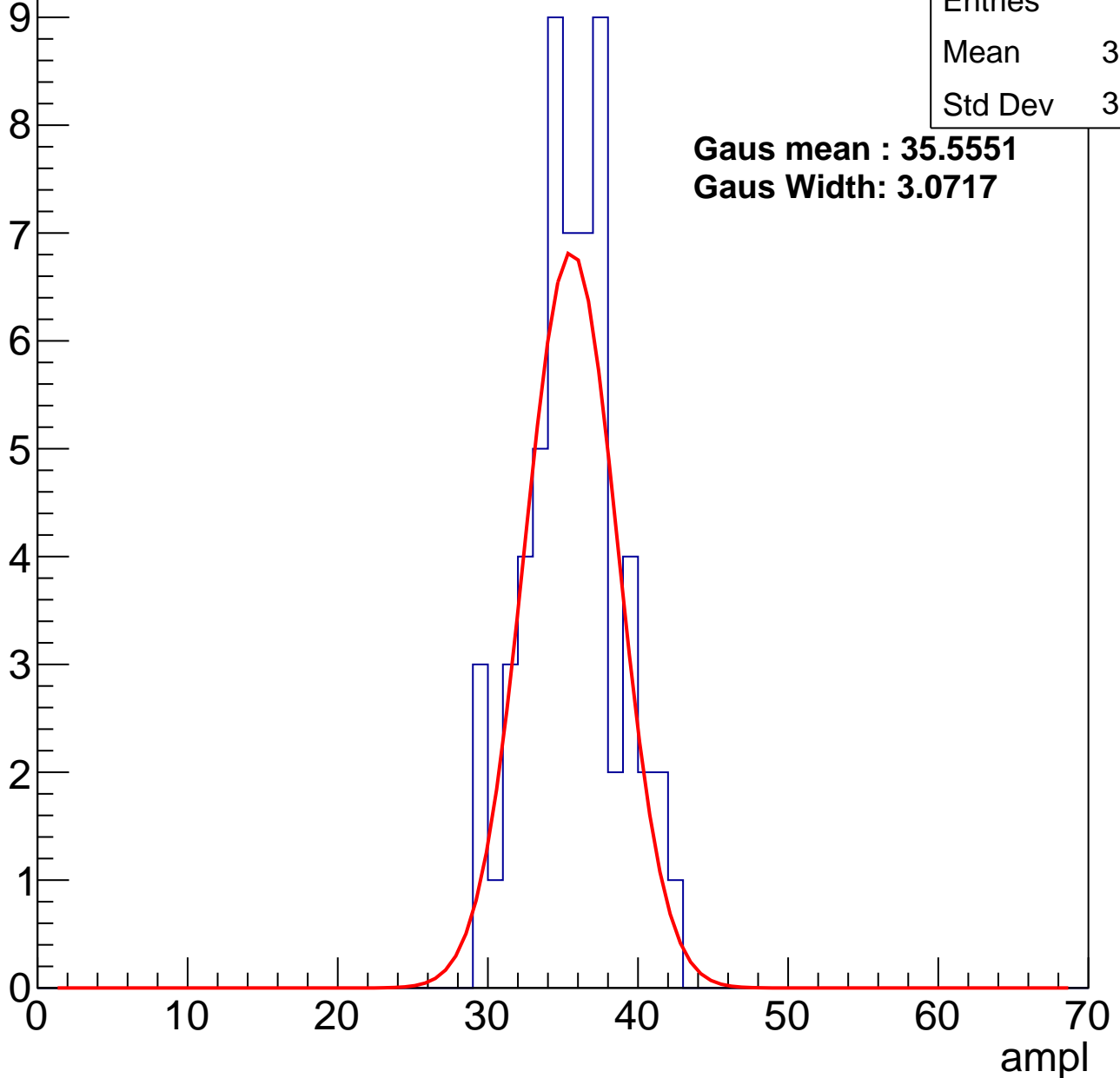
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	35.17
Std Dev	3.026

**Gaus mean : 35.5551**

**Gaus Width: 3.0717**



# B1L003S, U6-ch102, adc2

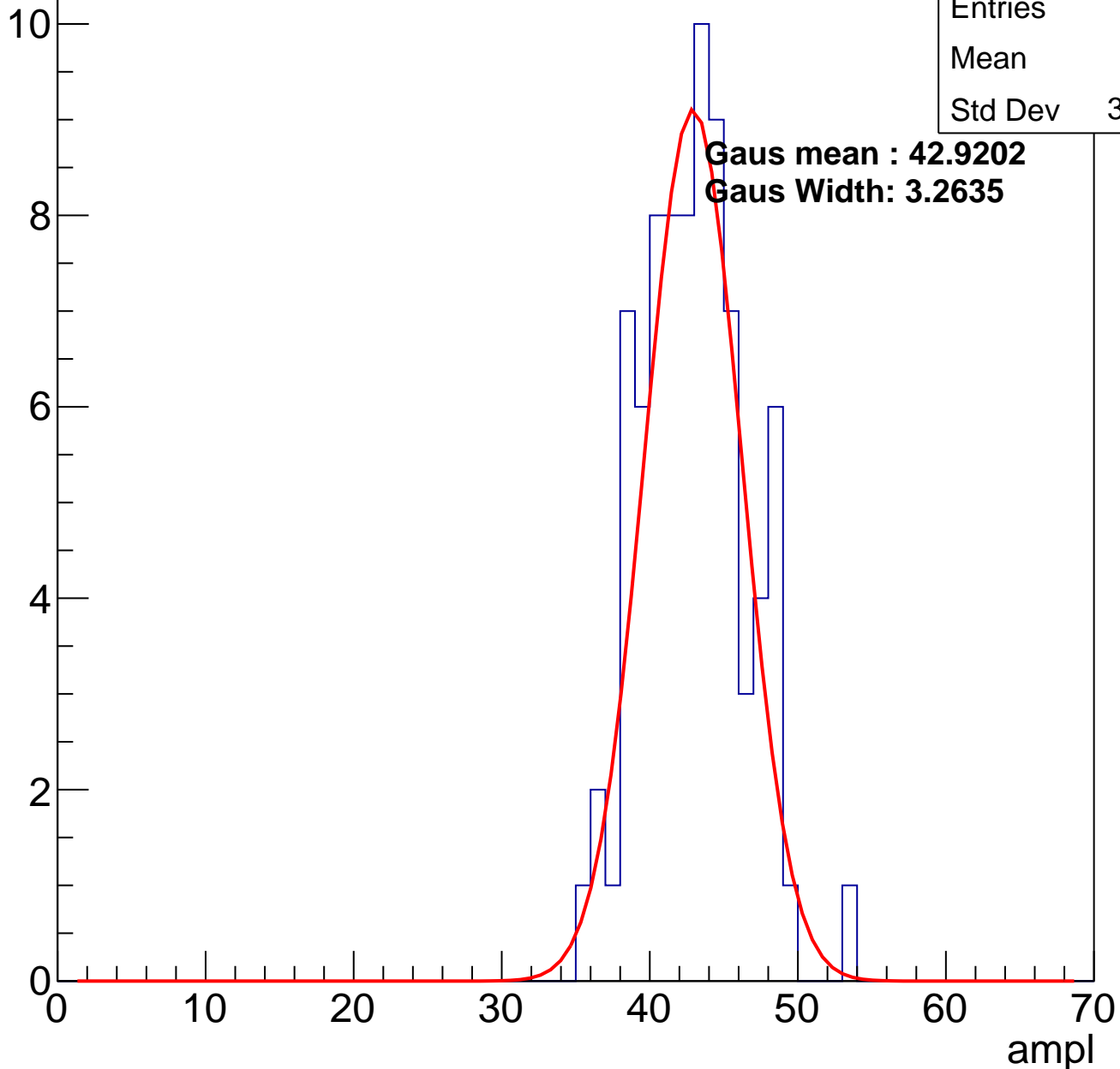
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	82
Mean	42.5
Std Dev	3.447

**Gaus mean : 42.9202**

**Gaus Width: 3.2635**

Entry

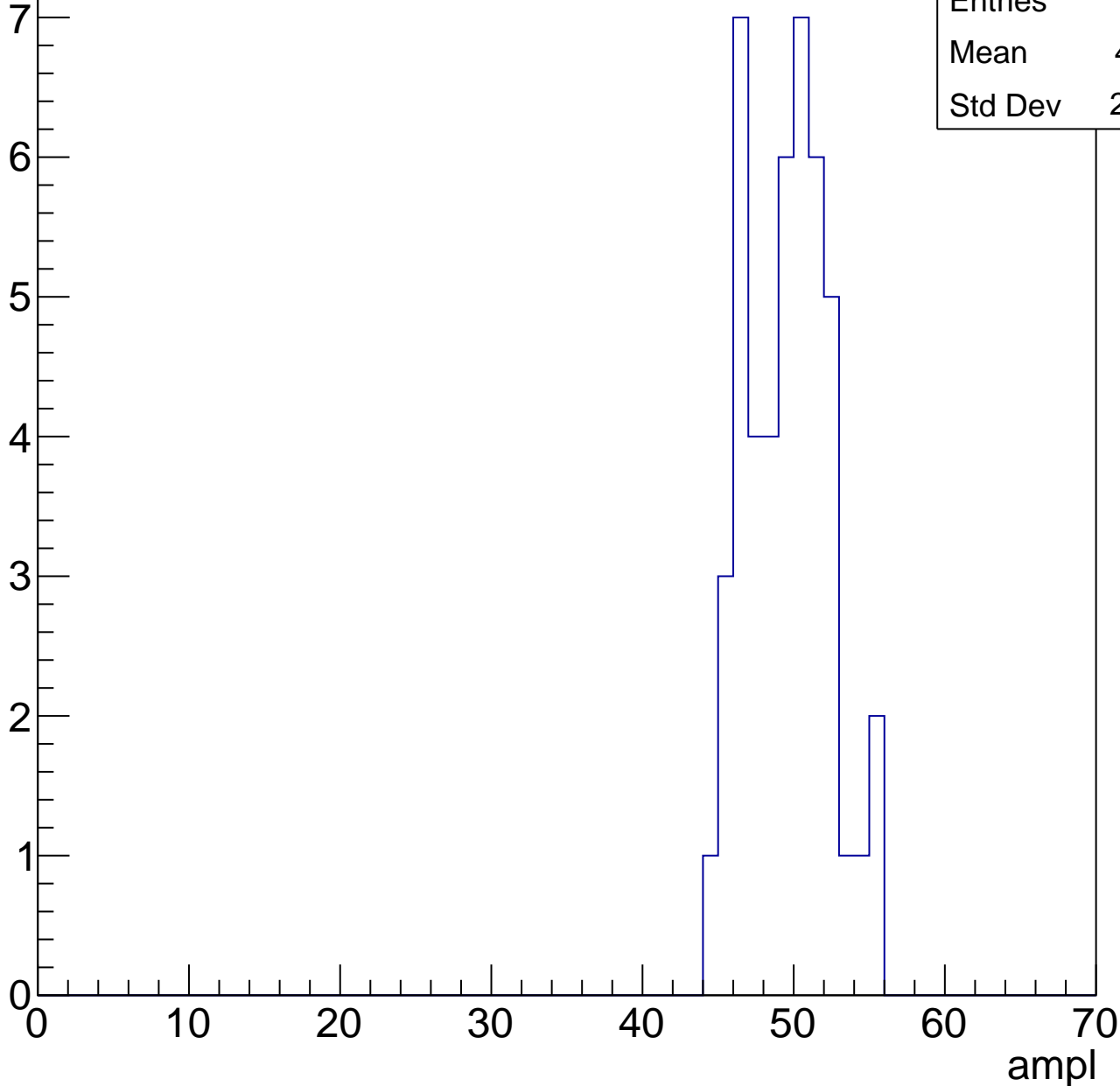


# B1L003S, U6-ch102, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	47
Mean	49.11
Std Dev	2.707

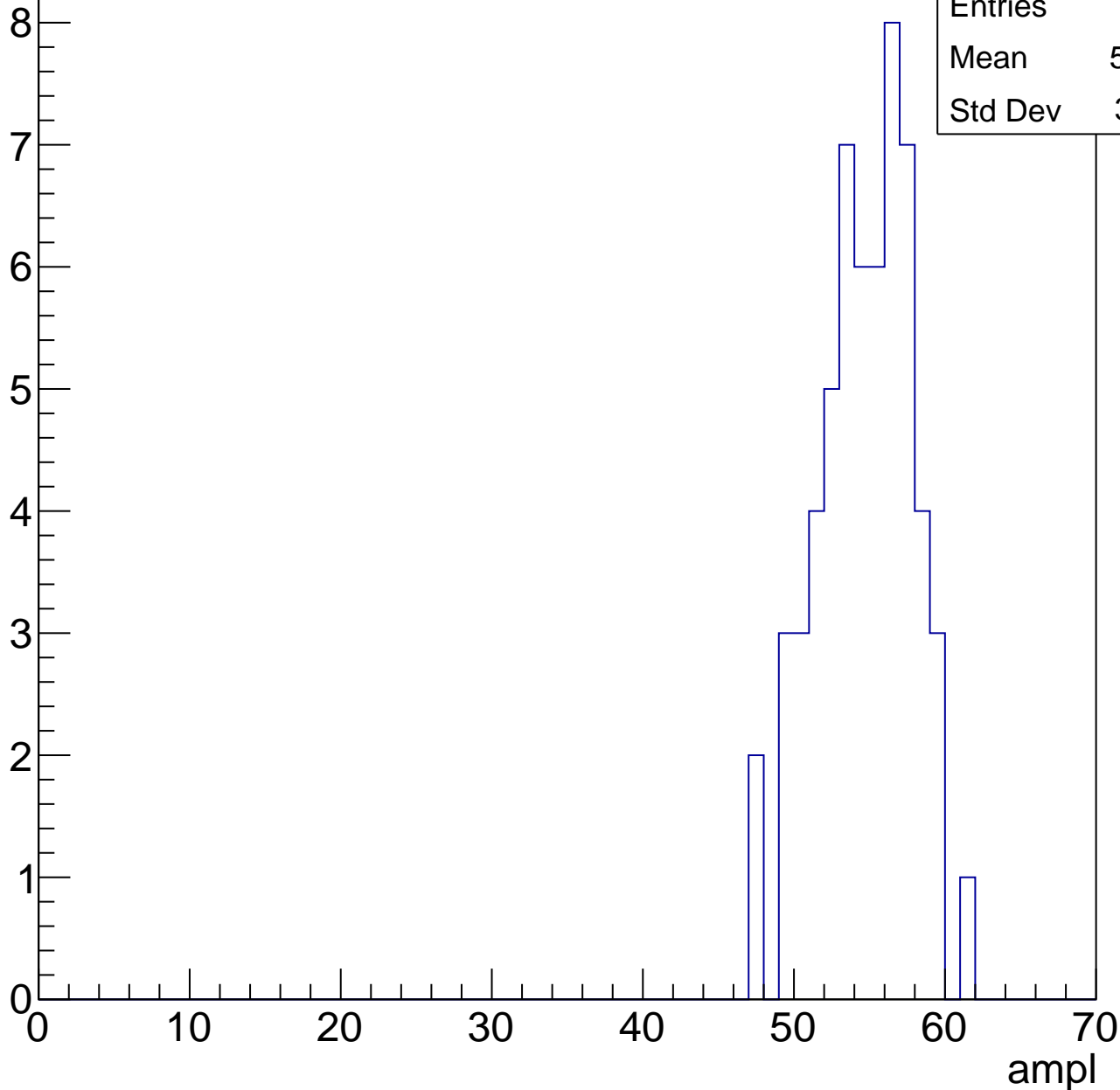


# B1L003S, U6-ch102, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	54.19
Std Dev	3.111

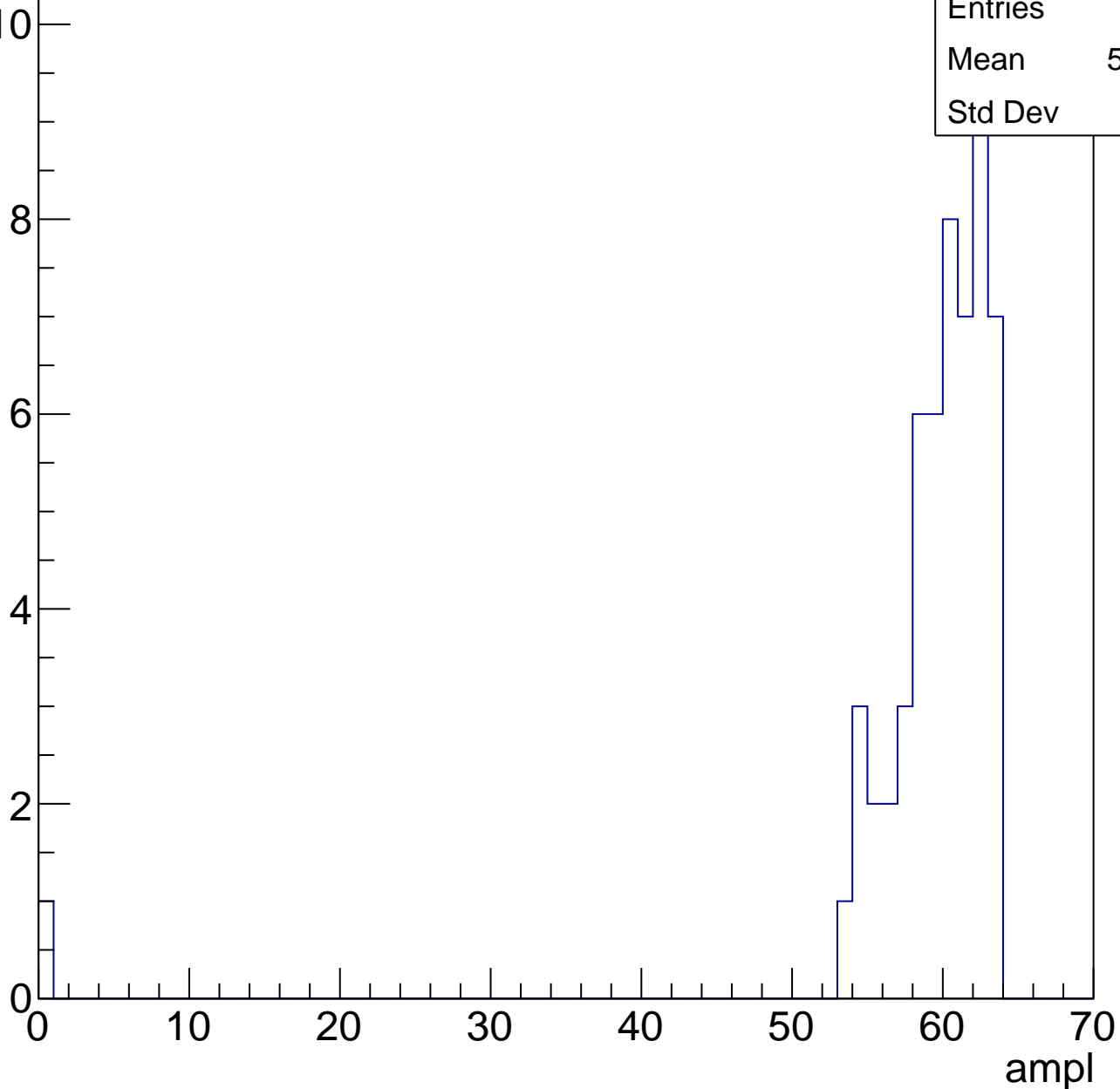


# B1L003S, U6-ch102, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	58.54
Std Dev	8.33



# B1L003S, U6-ch102, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries

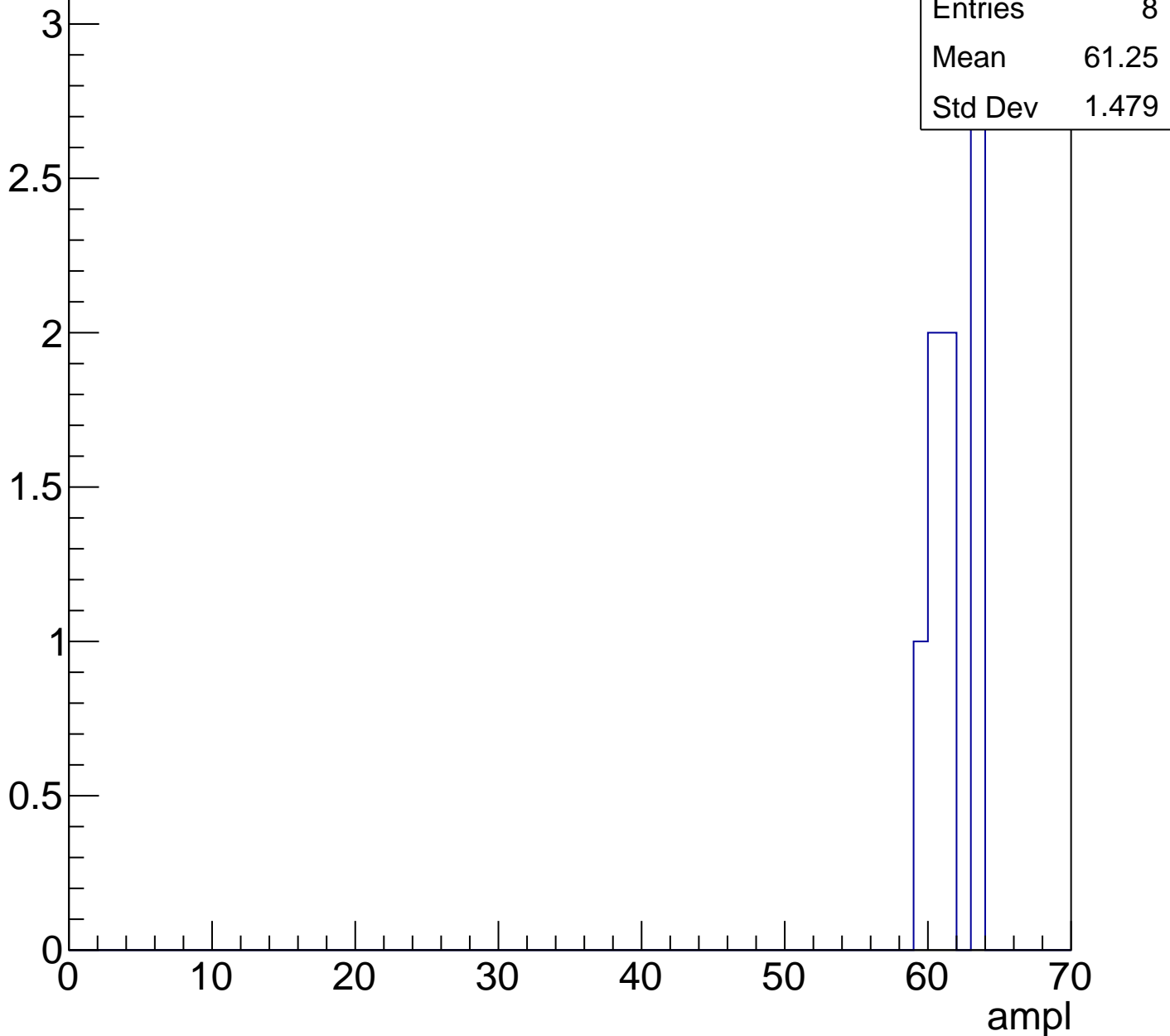
8

Mean

61.25

Std Dev

1.479





# B1L003S, U6-ch102, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	23
Std Dev	0

ampl

# B1L003S, U6-ch103, adc0

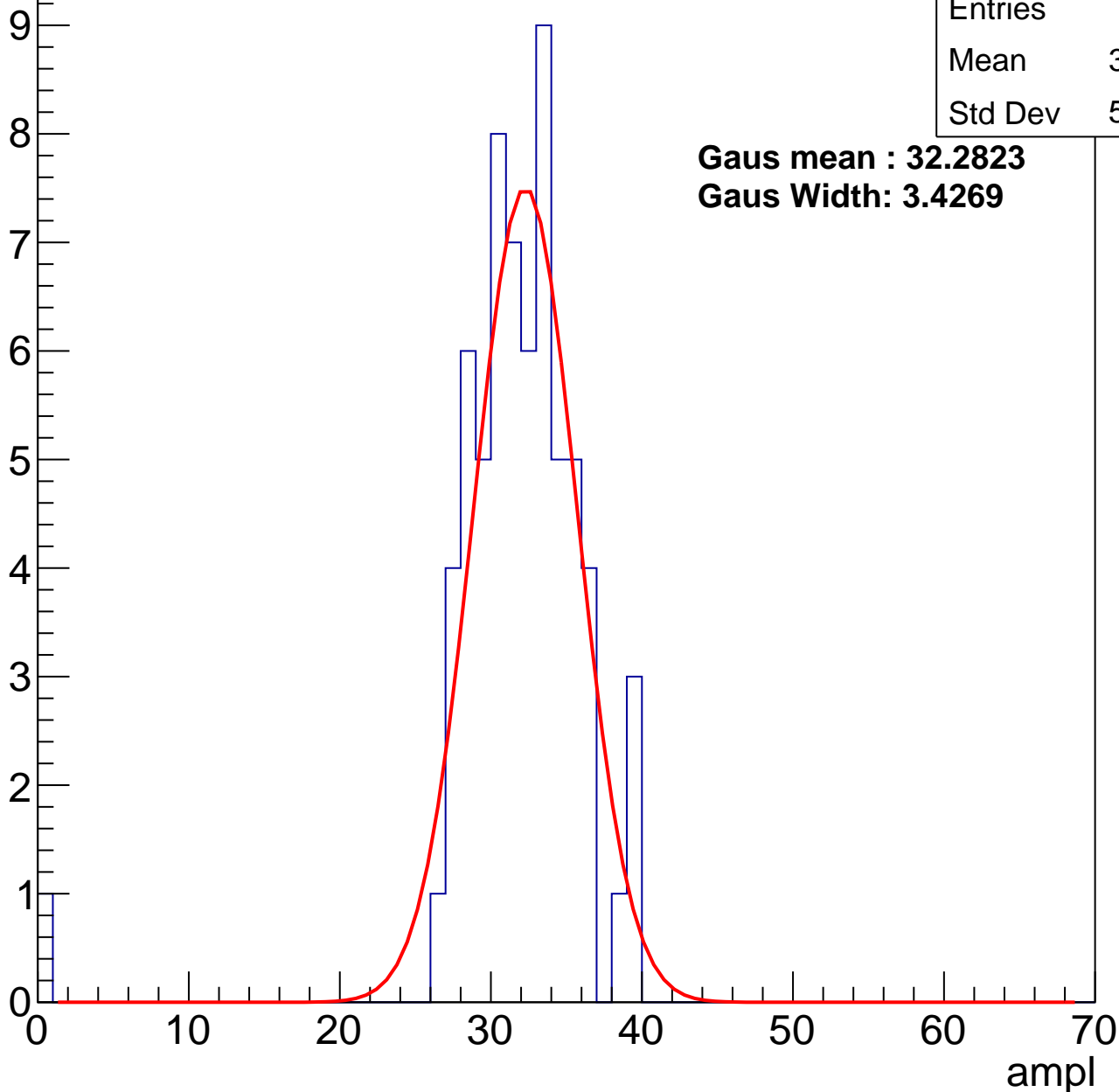
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	31.34
Std Dev	5.012

**Gaus mean : 32.2823**

**Gaus Width: 3.4269**



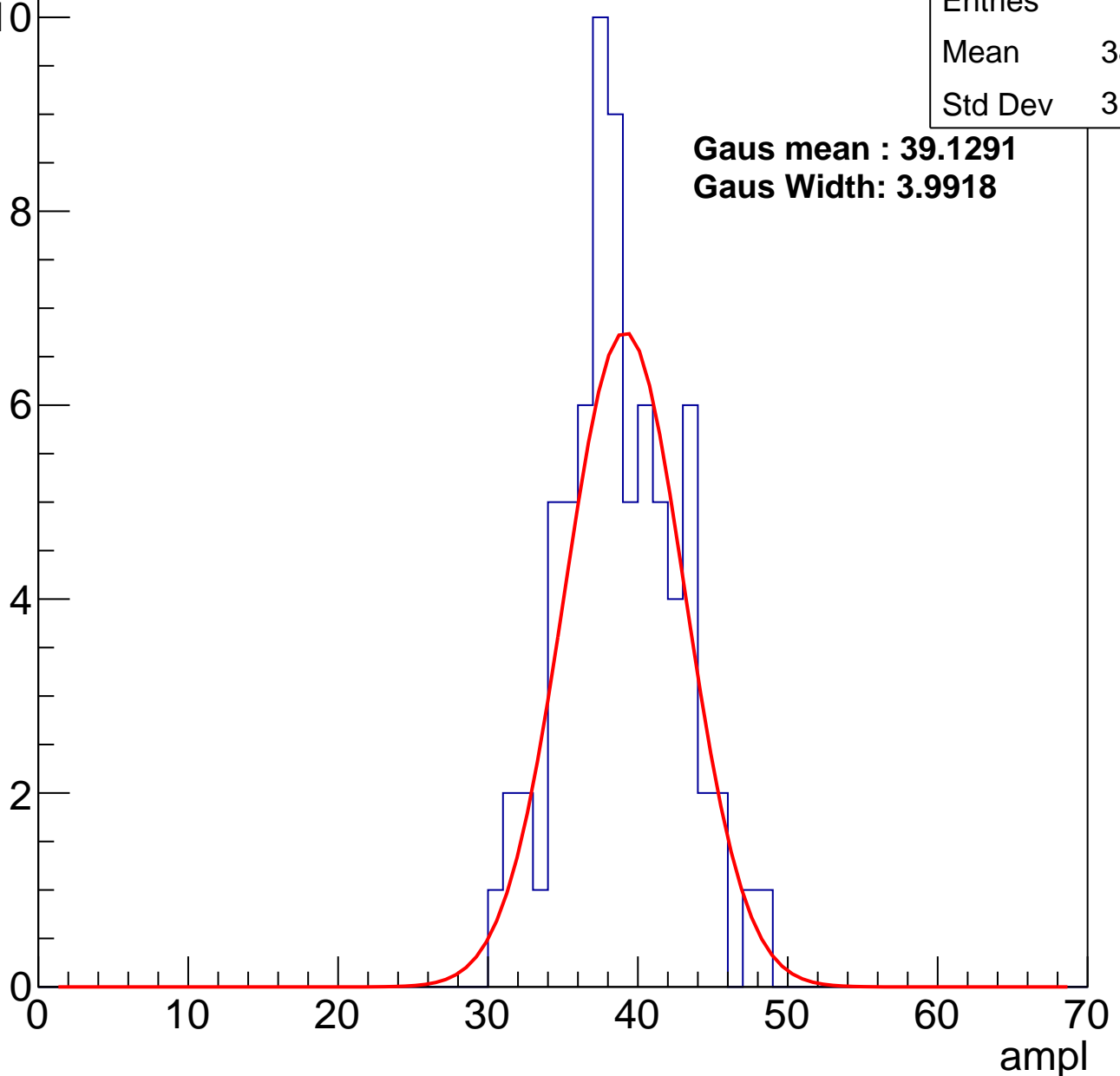
# B1L003S, U6-ch103, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	73
Mean	38.37
Std Dev	3.787

**Gaus mean : 39.1291**  
**Gaus Width: 3.9918**



# B1L003S, U6-ch103, adc2

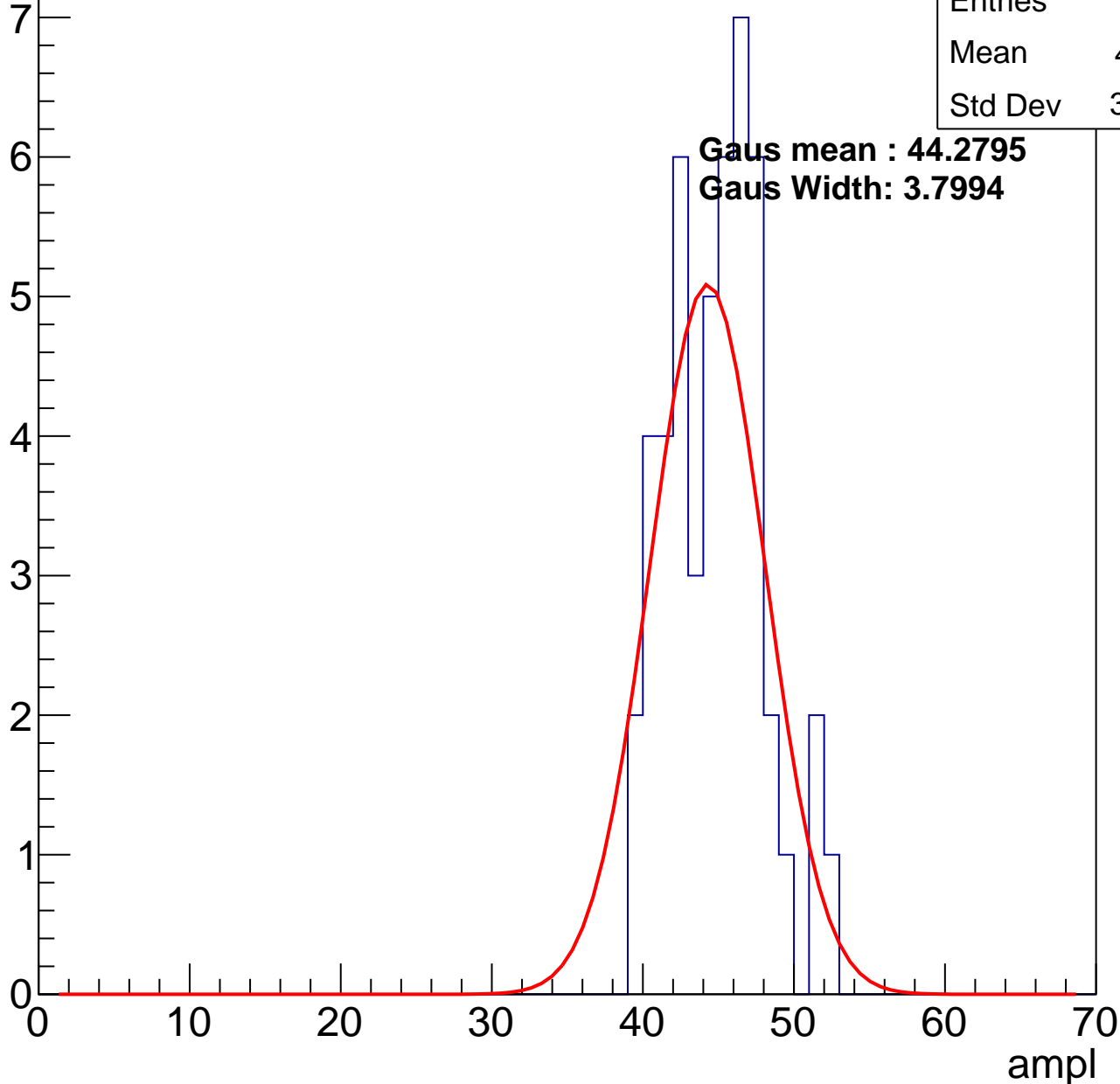
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	49
Mean	44.41
Std Dev	3.116

**Gaus mean : 44.2795**

**Gaus Width: 3.7994**

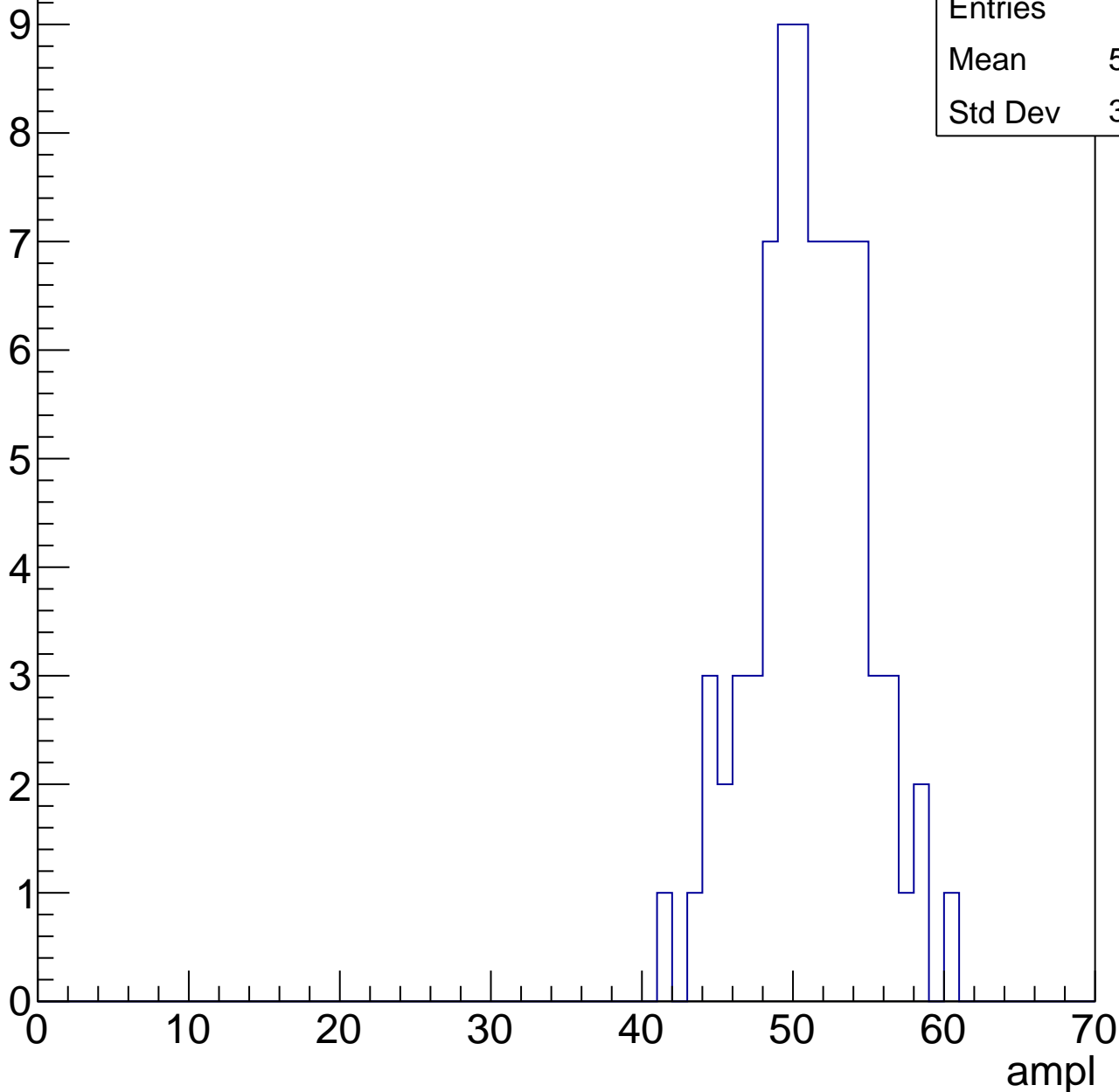


# B1L003S, U6-ch103, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

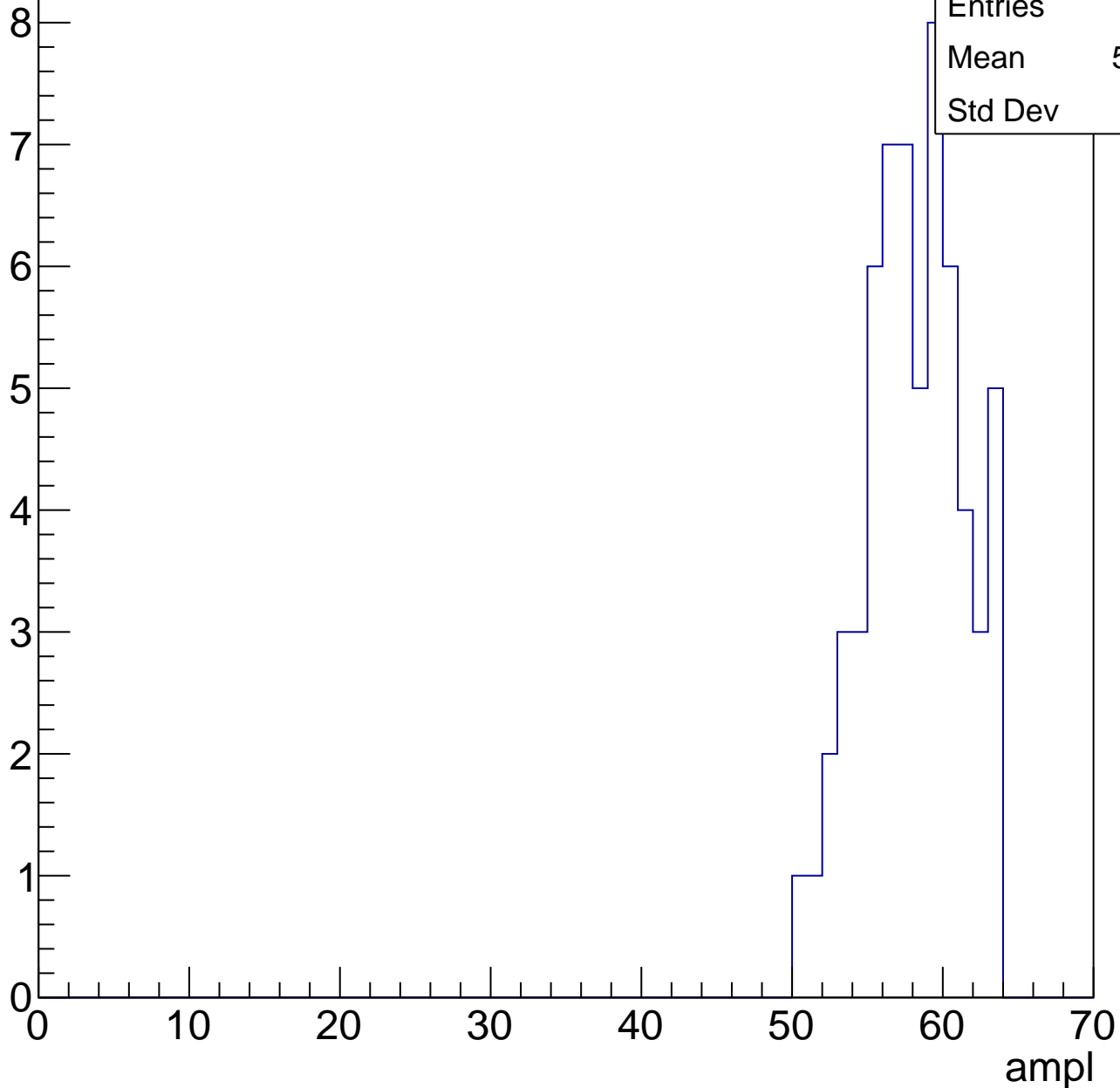
Entries	76
Mean	50.63
Std Dev	3.699



# B1L003S, U6-ch103, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



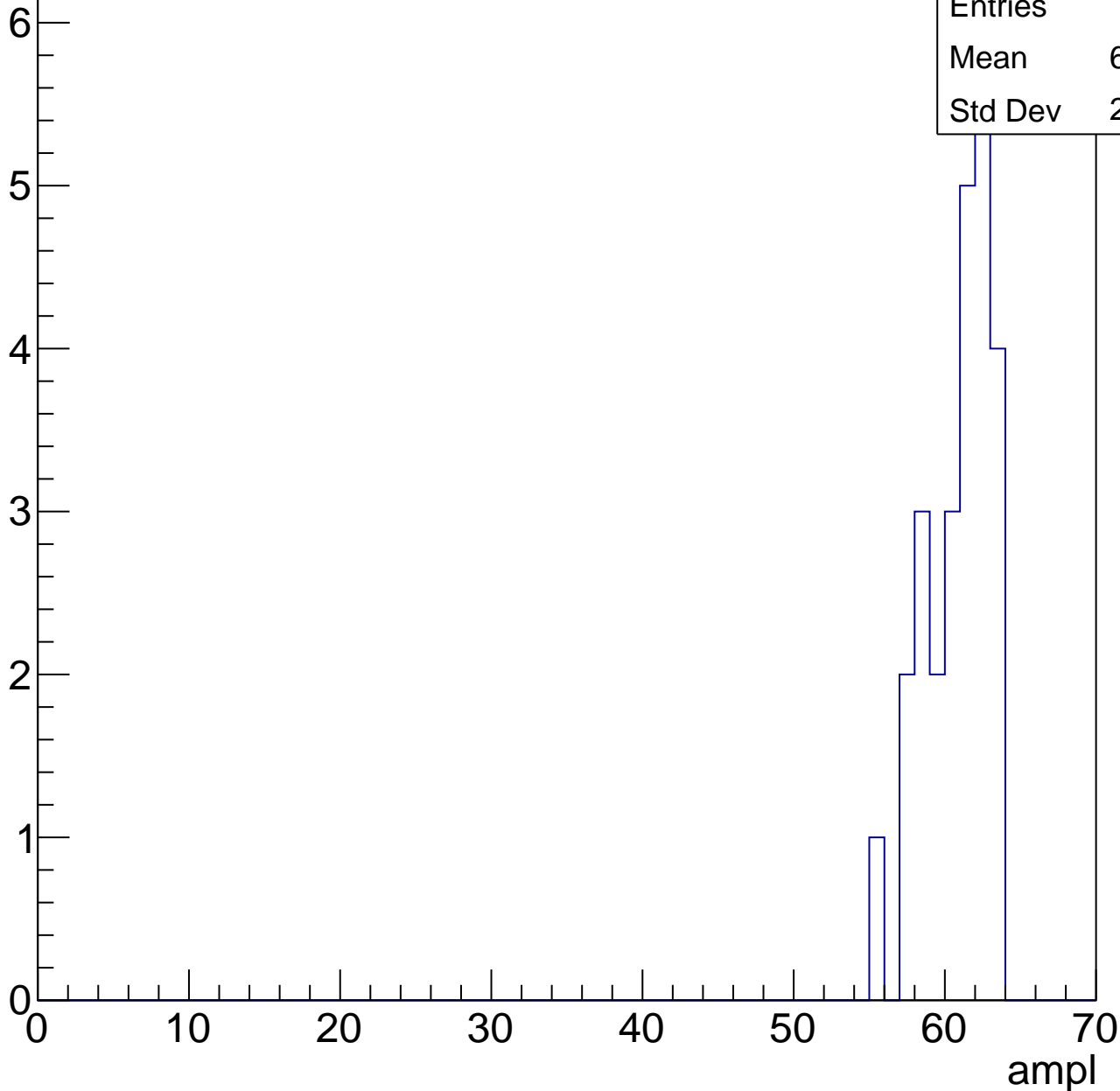
Entries	61
Mean	57.61
Std Dev	3.21

# B1L003S, U6-ch103, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	26
Mean	60.38
Std Dev	2.132



# B1L003S, U6-ch103, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch103, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	25
Std Dev	0

ampl

# B1L003S, U6-ch104, adc0

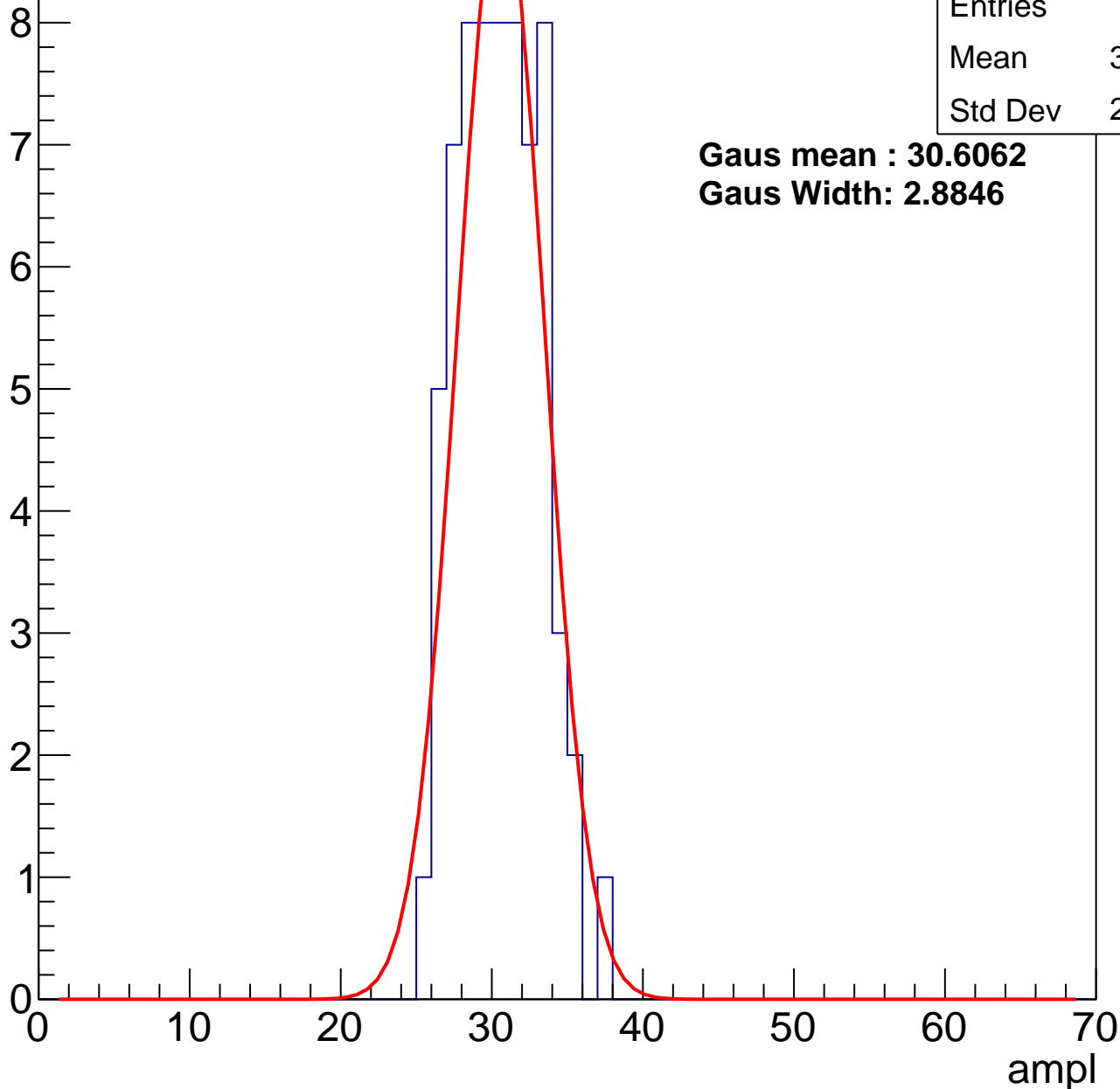
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	30.08
Std Dev	2.648

**Gaus mean : 30.6062**

**Gaus Width: 2.8846**



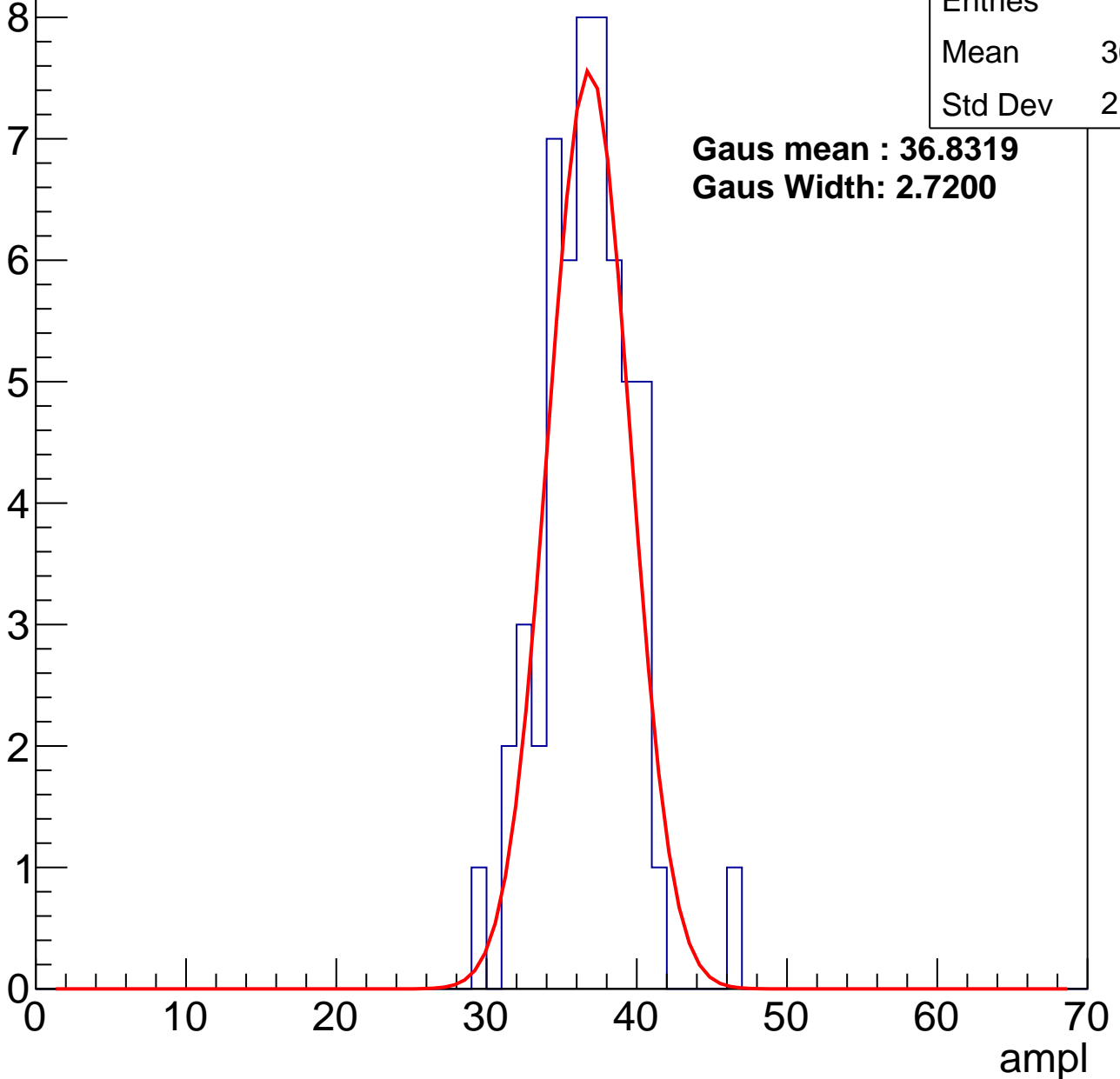
# B1L003S, U6-ch104, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	36.27
Std Dev	2.945

**Gaus mean : 36.8319**  
**Gaus Width: 2.7200**



# B1L003S, U6-ch104, adc2

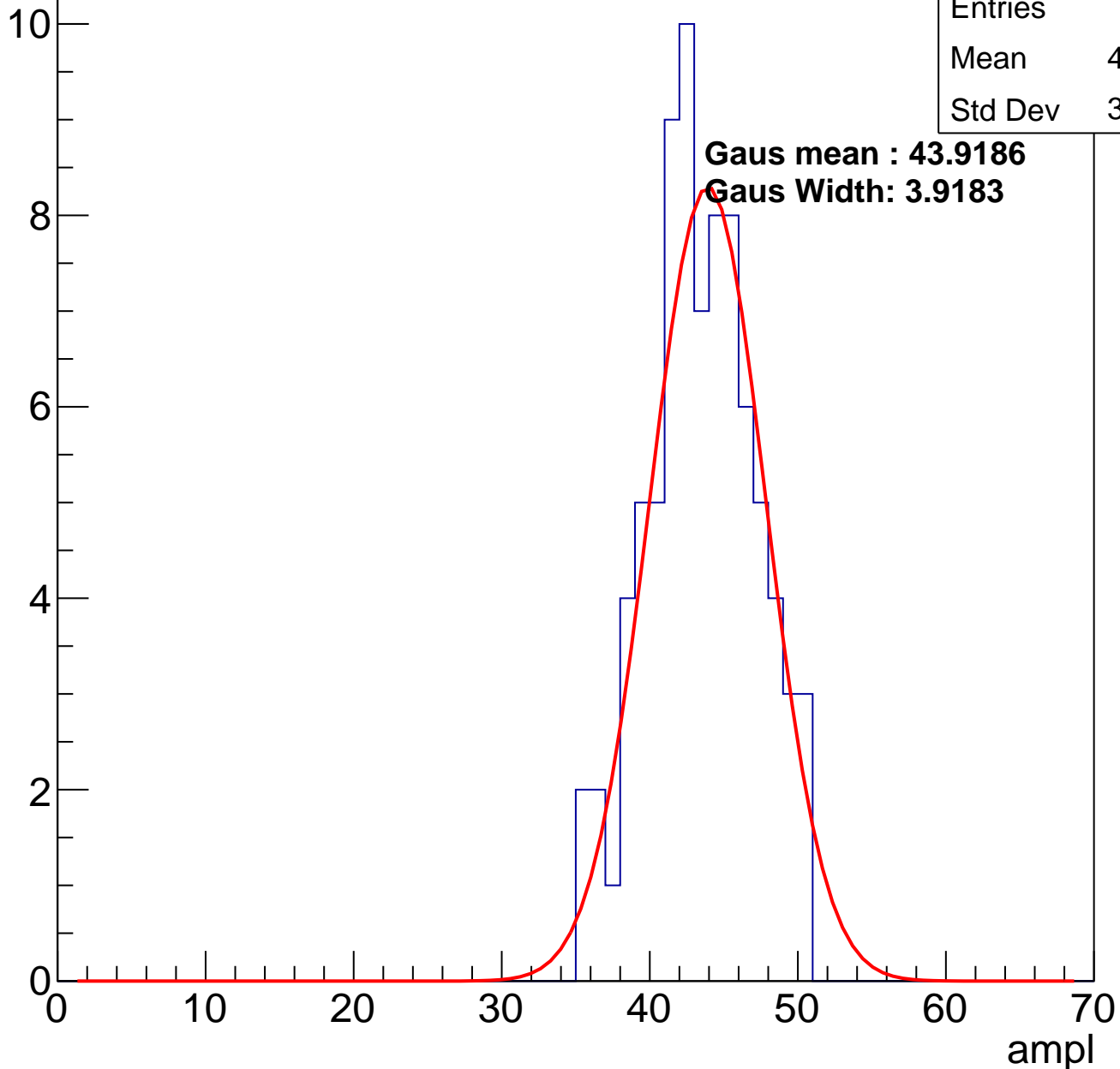
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	82
Mean	43.02
Std Dev	3.599

**Gaus mean : 43.9186**

**Gaus Width: 3.9183**

Entry

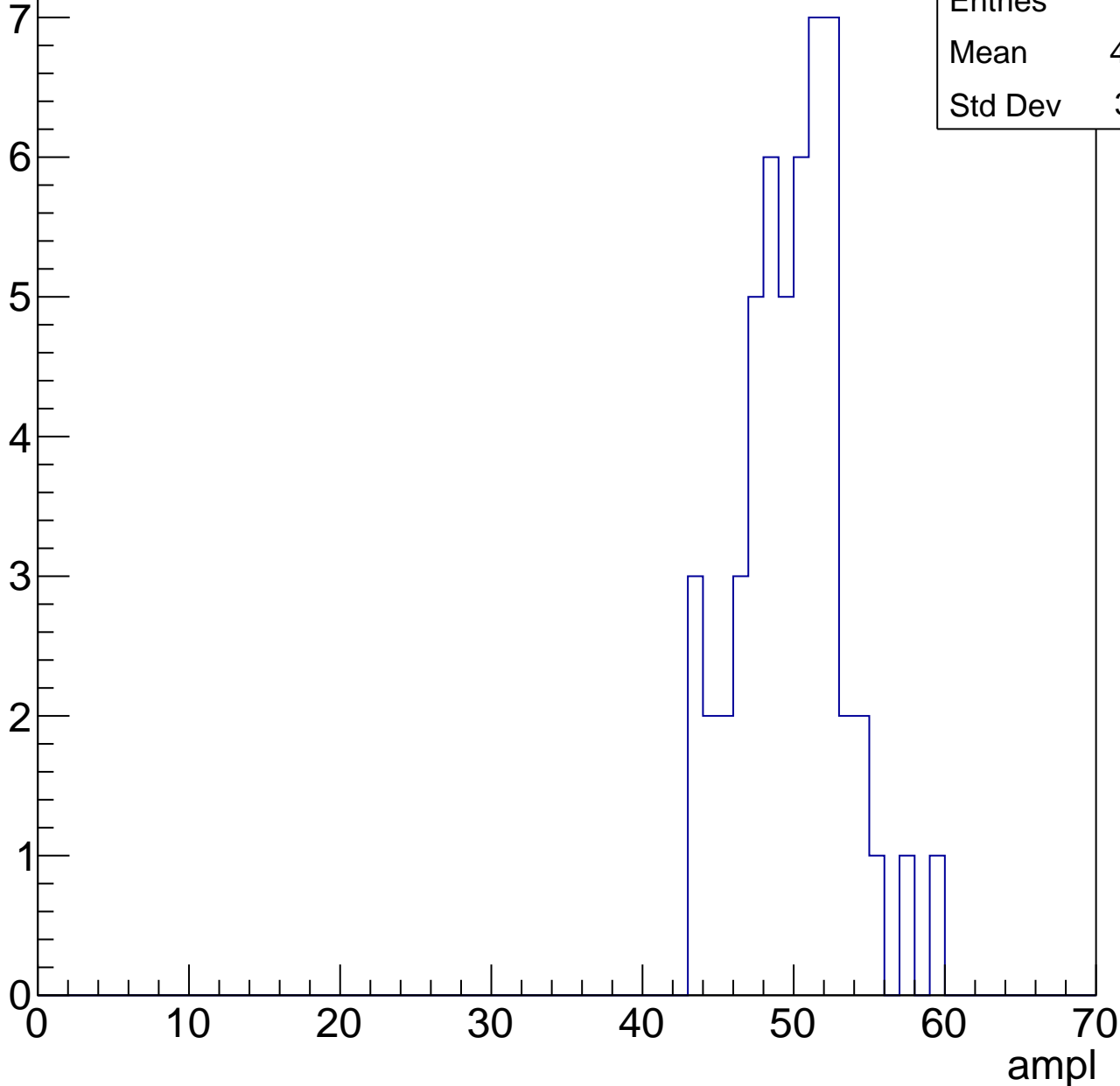


# B1L003S, U6-ch104, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	49.42
Std Dev	3.401

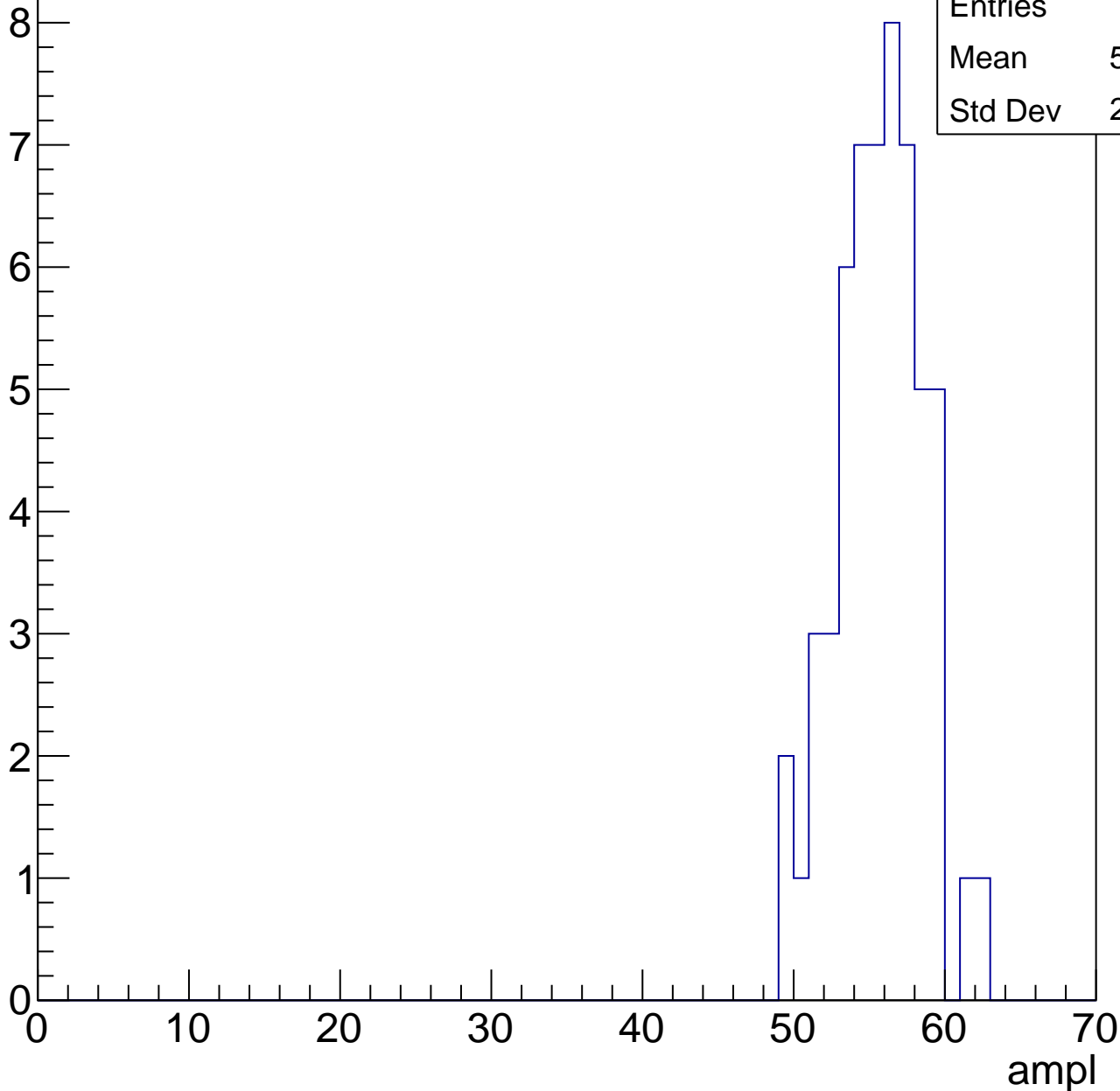


# B1L003S, U6-ch104, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	55.23
Std Dev	2.822



# B1L003S, U6-ch104, adc5

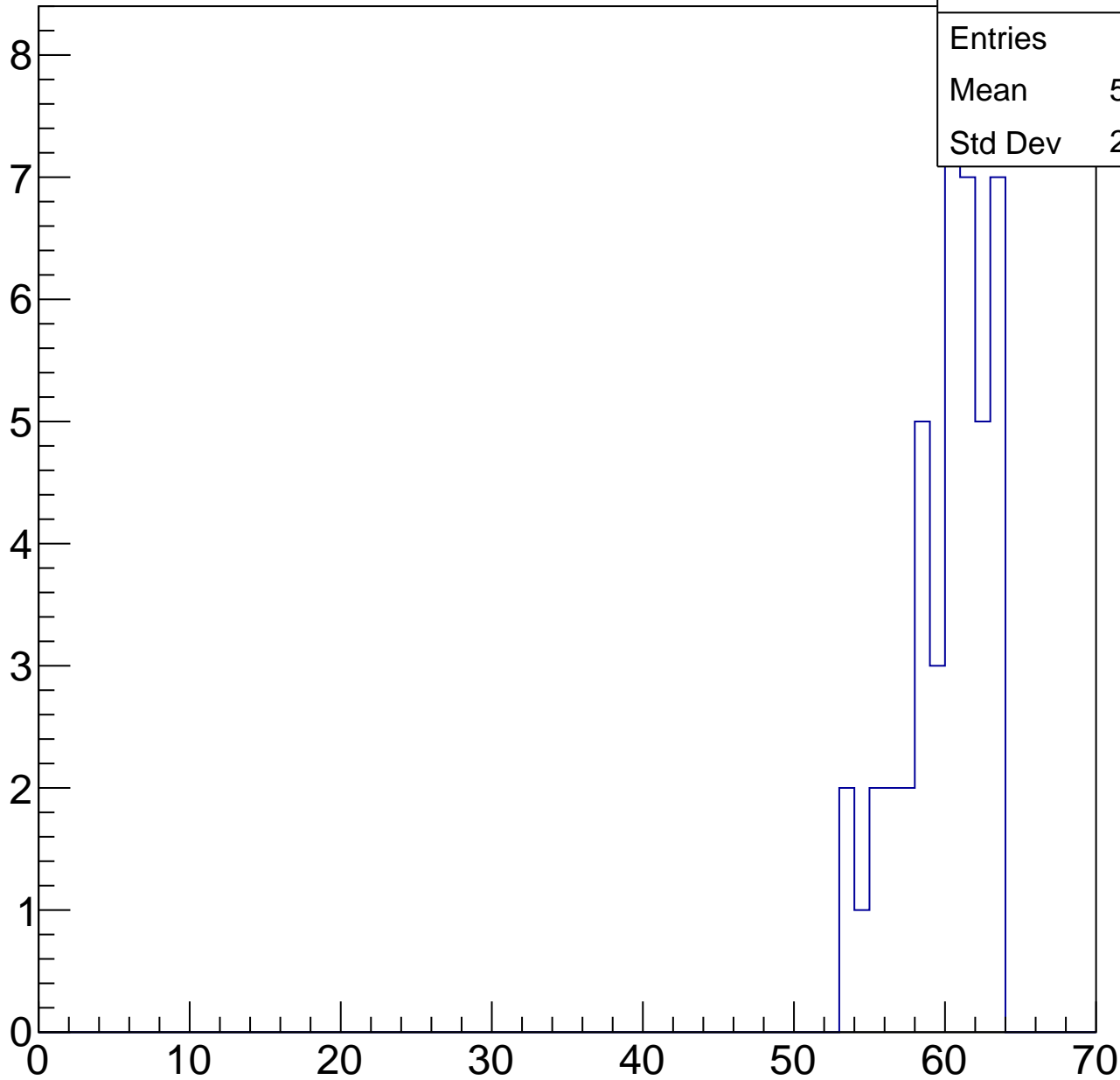
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	44
Mean	59.57
Std Dev	2.775

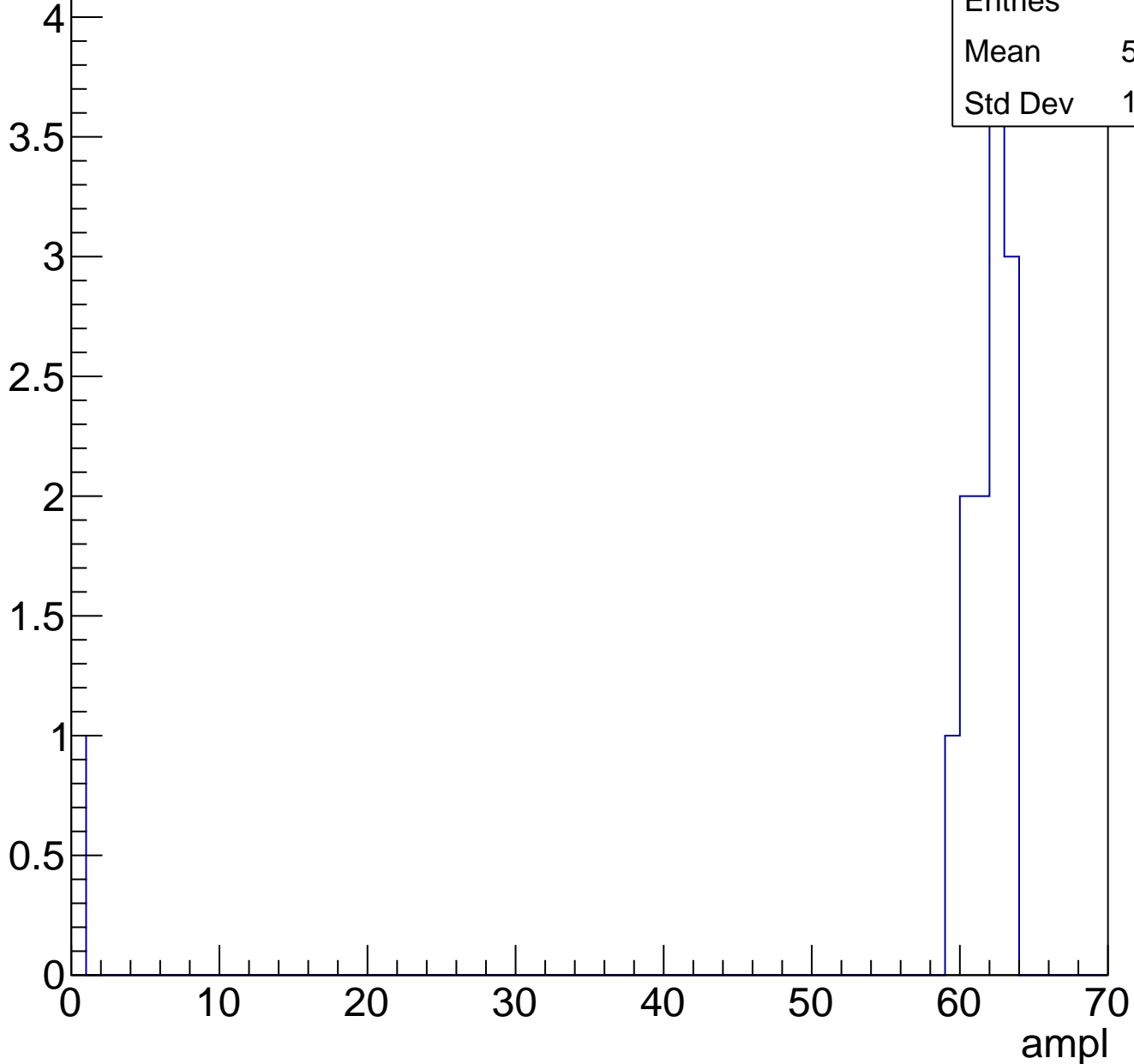
ampl



# B1L003S, U6-ch104, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch104, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U6-ch105, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	85
Mean	30.42
Std Dev	4.924

**Gaus mean : 31.4451**

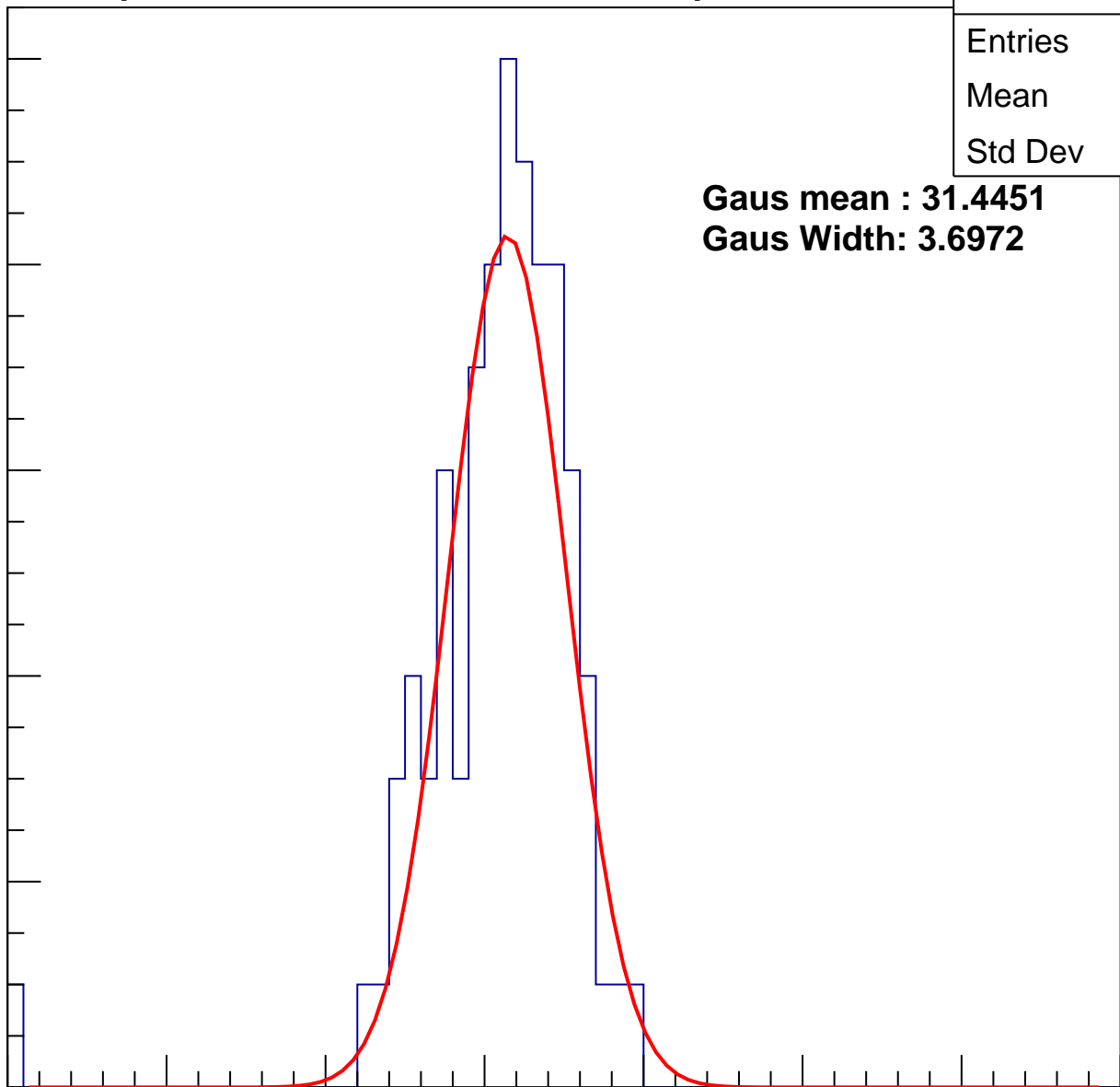
**Gaus Width: 3.6972**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U6-ch105, adc1

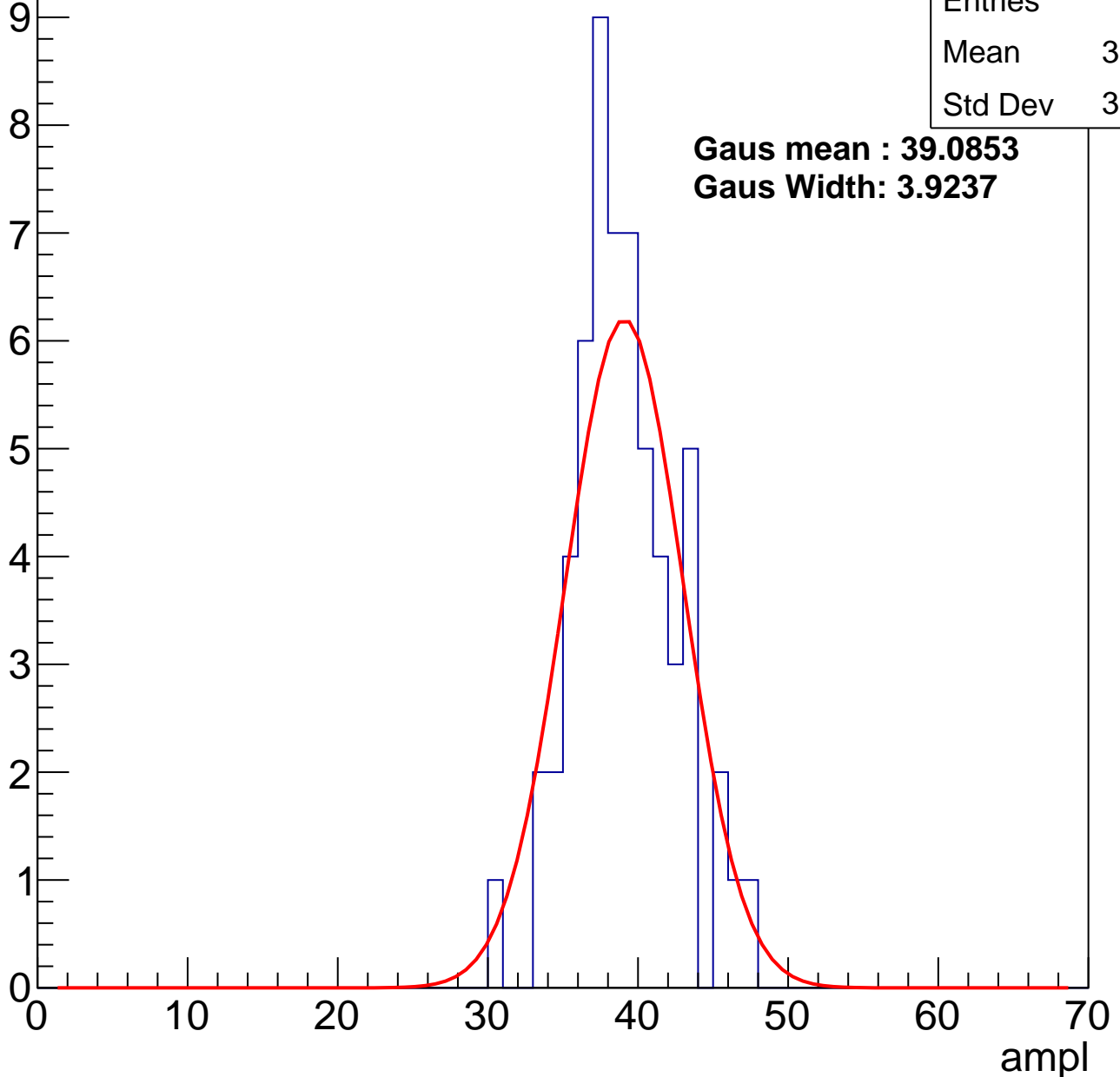
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	38.64
Std Dev	3.369

**Gaus mean : 39.0853**

**Gaus Width: 3.9237**



# B1L003S, U6-ch105, adc2

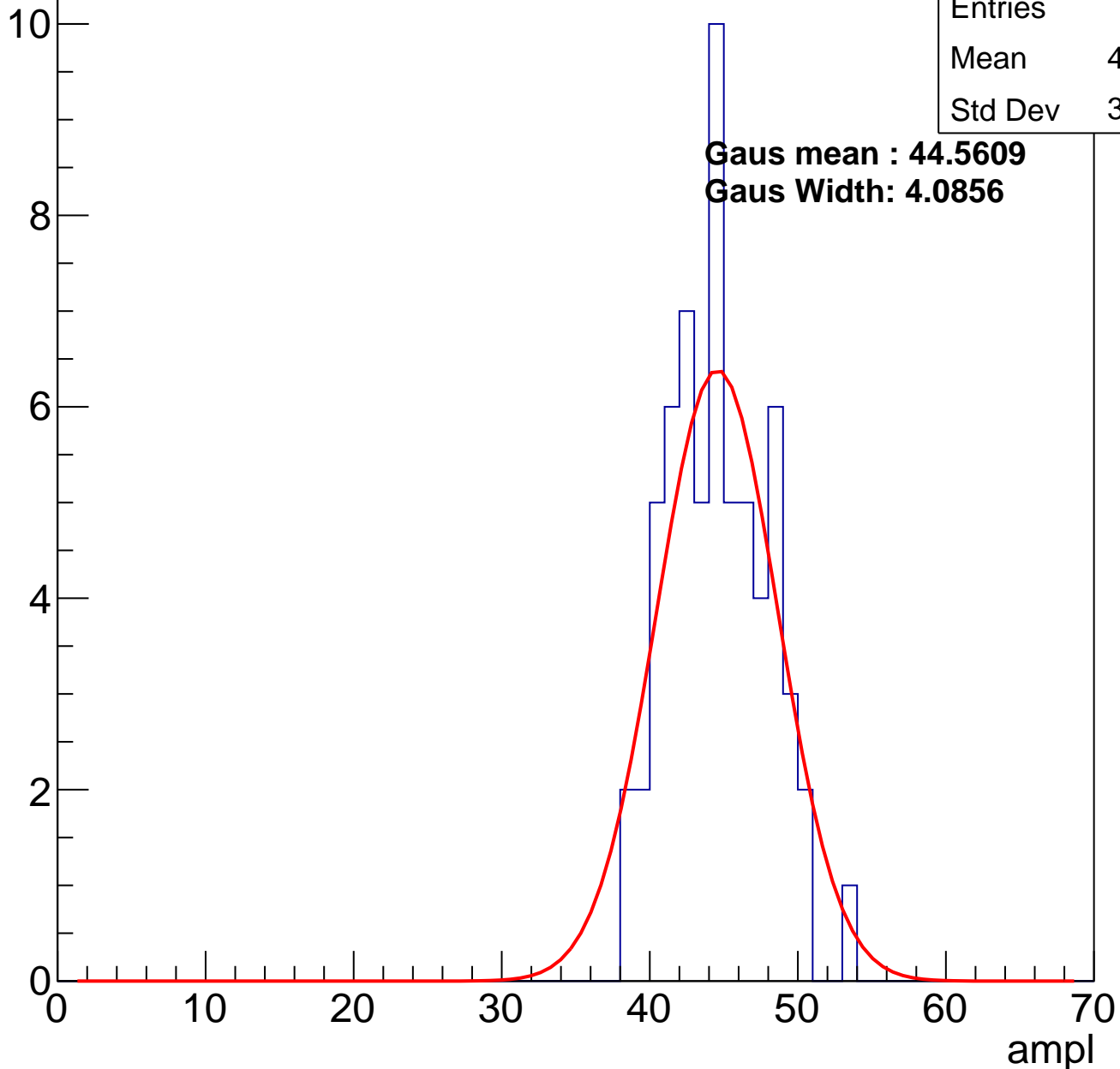
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	63
Mean	44.13
Std Dev	3.268

**Gaus mean : 44.5609**

**Gaus Width: 4.0856**

Entry



# B1L003S, U6-ch105, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

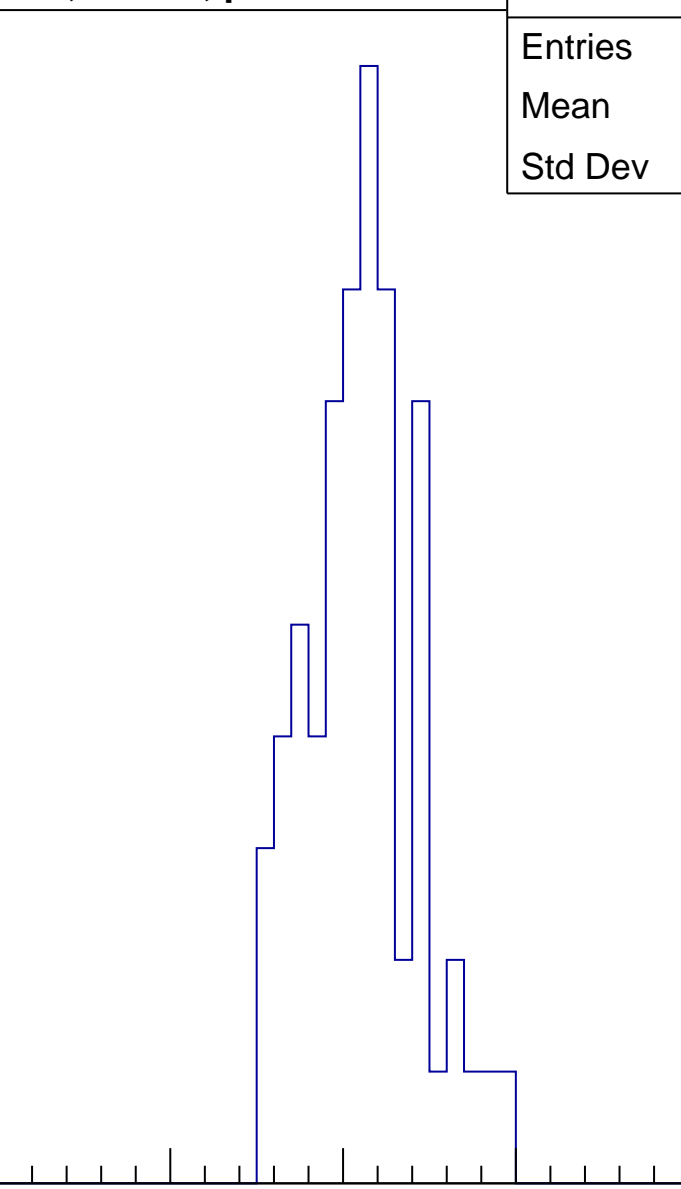
Entries	64
Mean	50.62
Std Dev	3.175

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

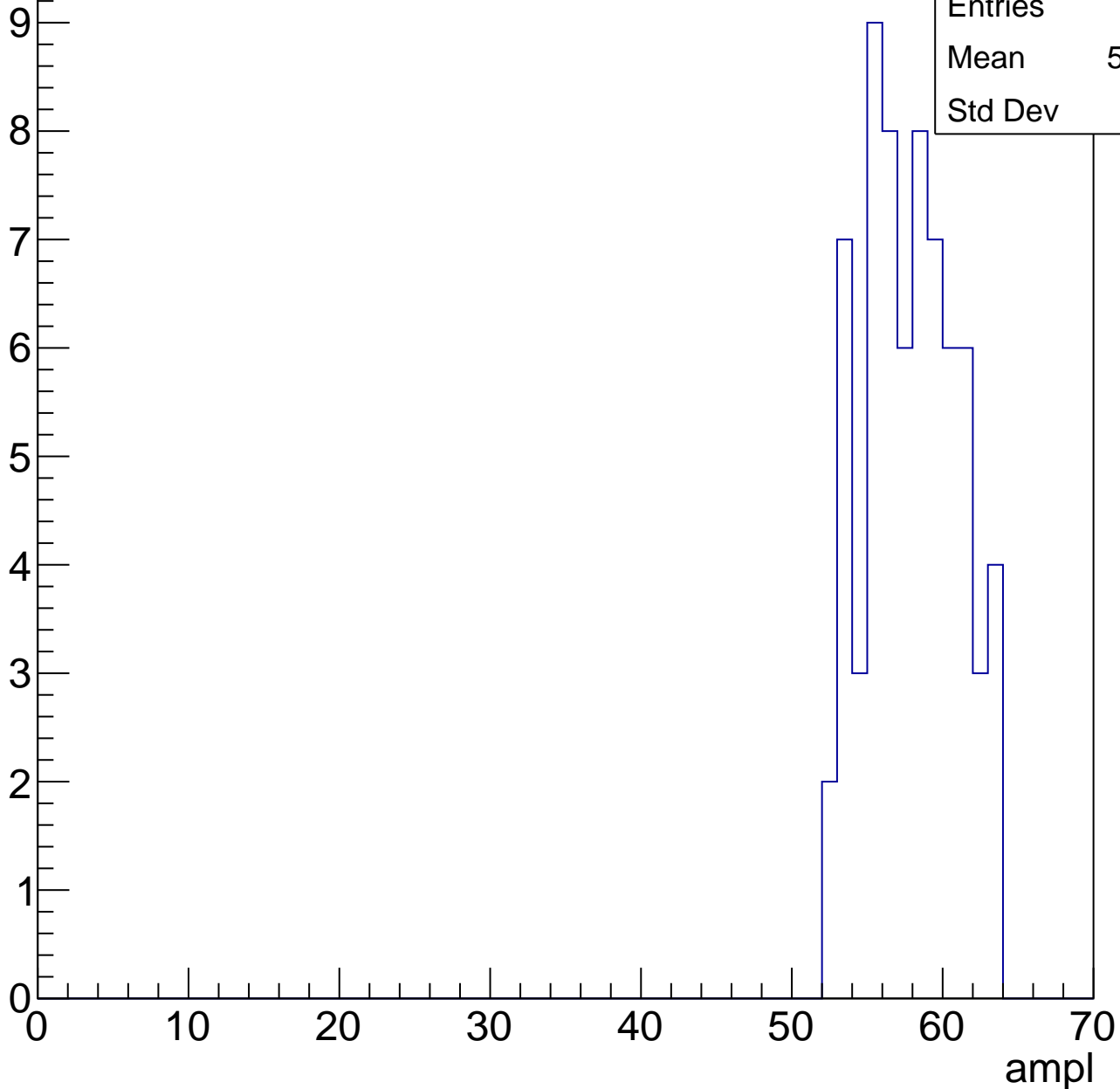


# B1L003S, U6-ch105, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	57.43
Std Dev	3.01

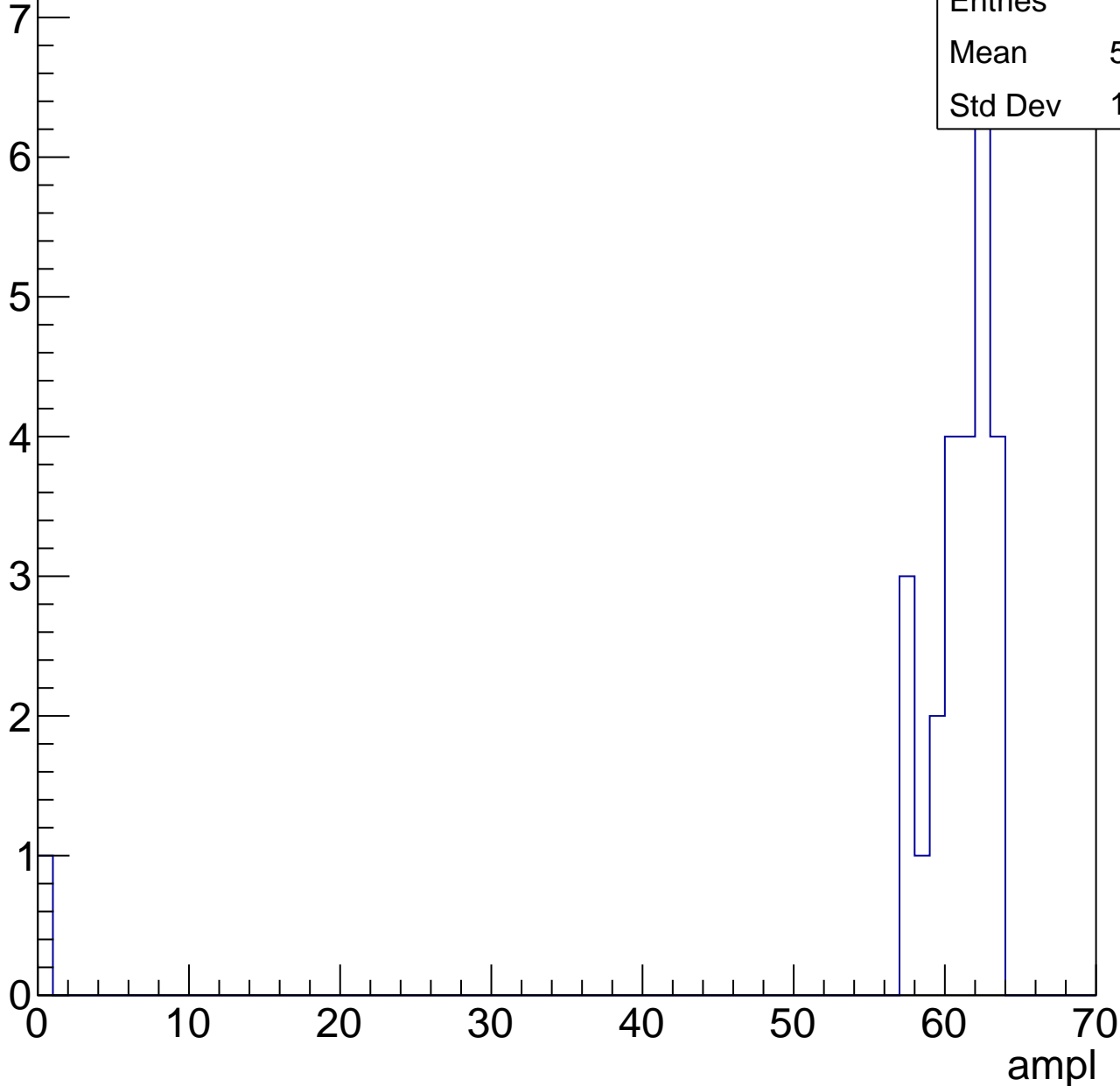


# B1L003S, U6-ch105, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	26
Mean	58.35
Std Dev	11.82



# B1L003S, U6-ch105, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch105, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch106, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	72
Mean	28.54
Std Dev	5.821

**Gaus mean : 29.6905**

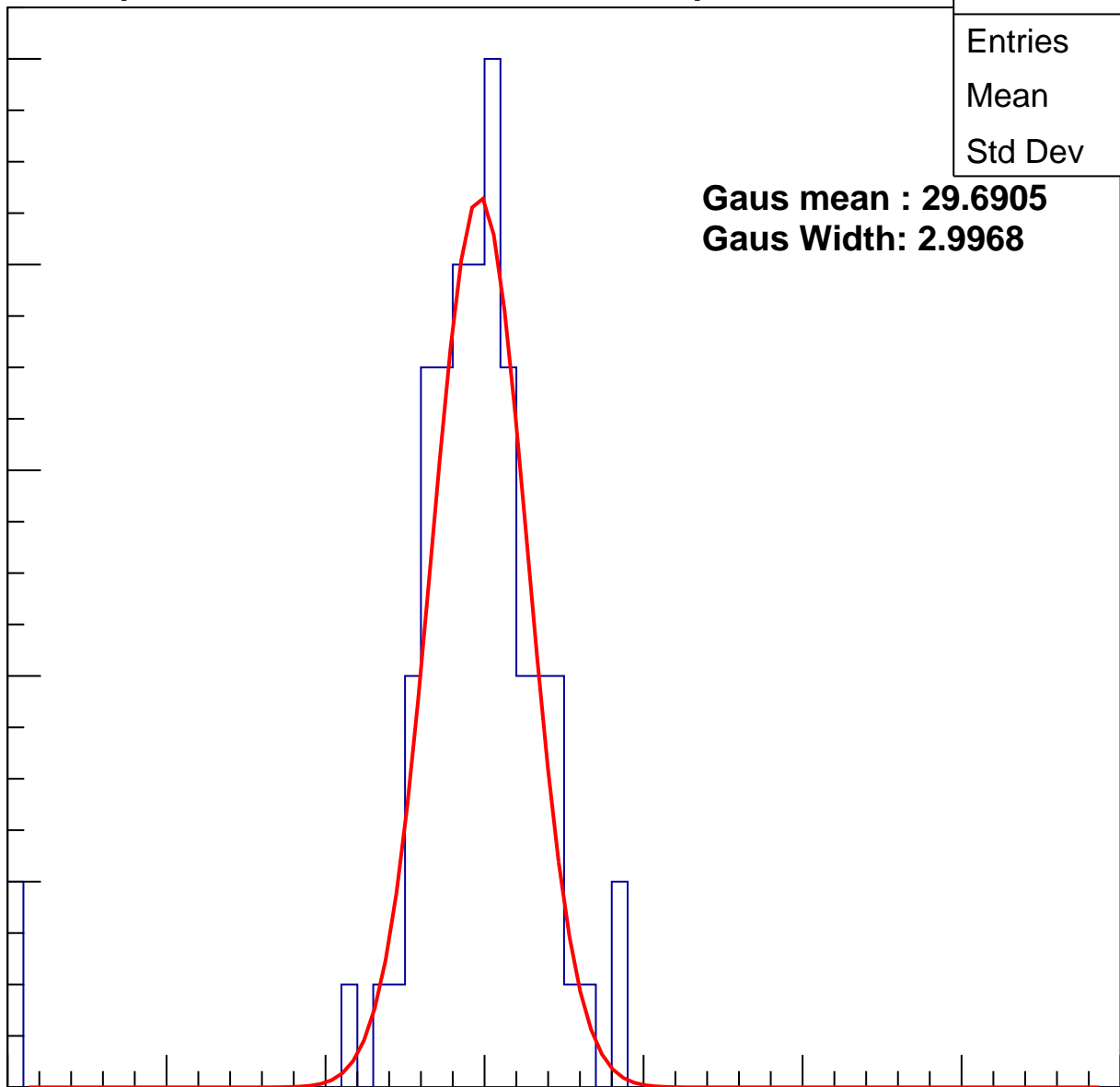
**Gaus Width: 2.9968**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U6-ch106, adc1

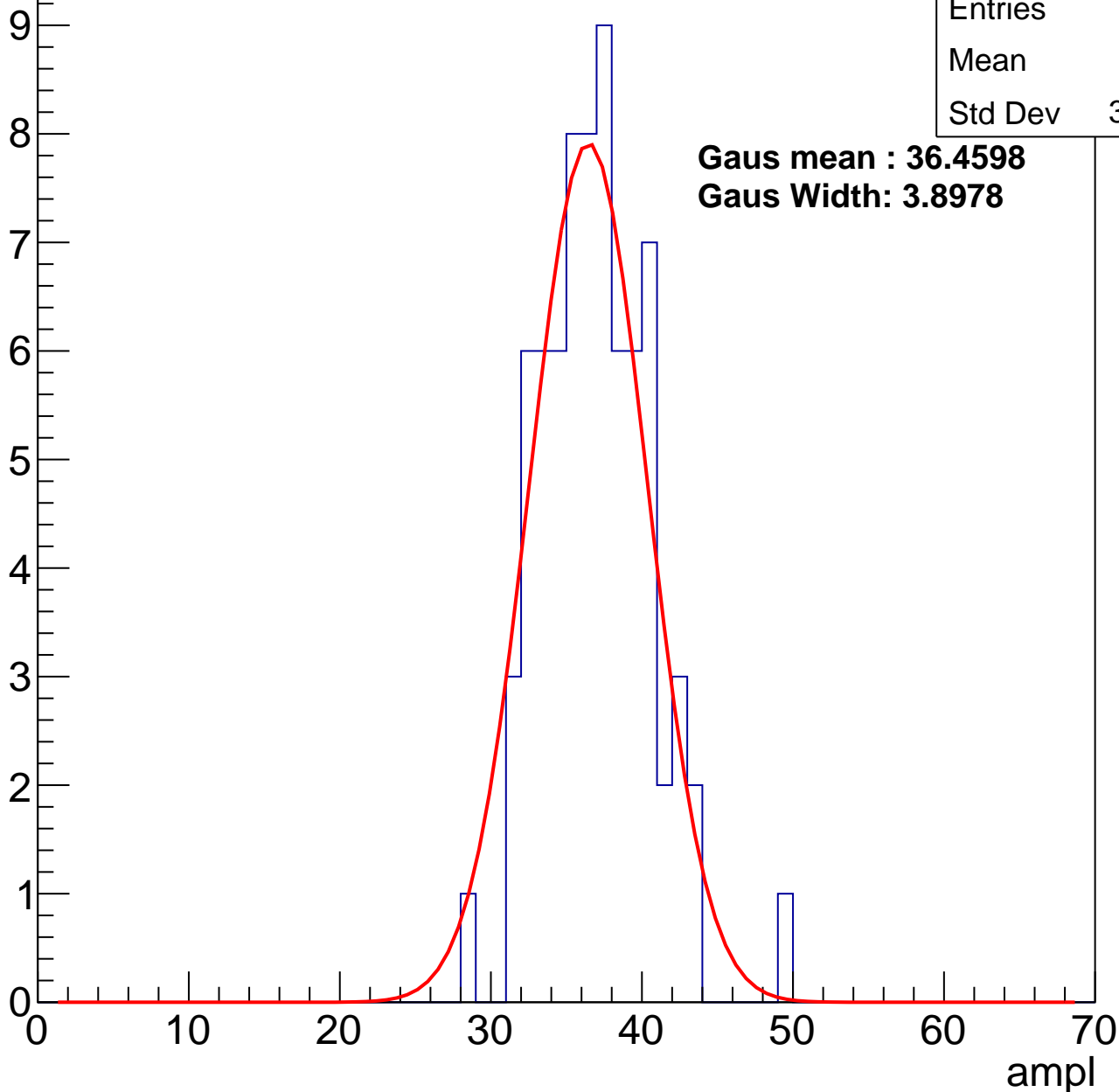
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	74
Mean	36.5
Std Dev	3.538

**Gaus mean : 36.4598**

**Gaus Width: 3.8978**



# B1L003S, U6-ch106, adc2

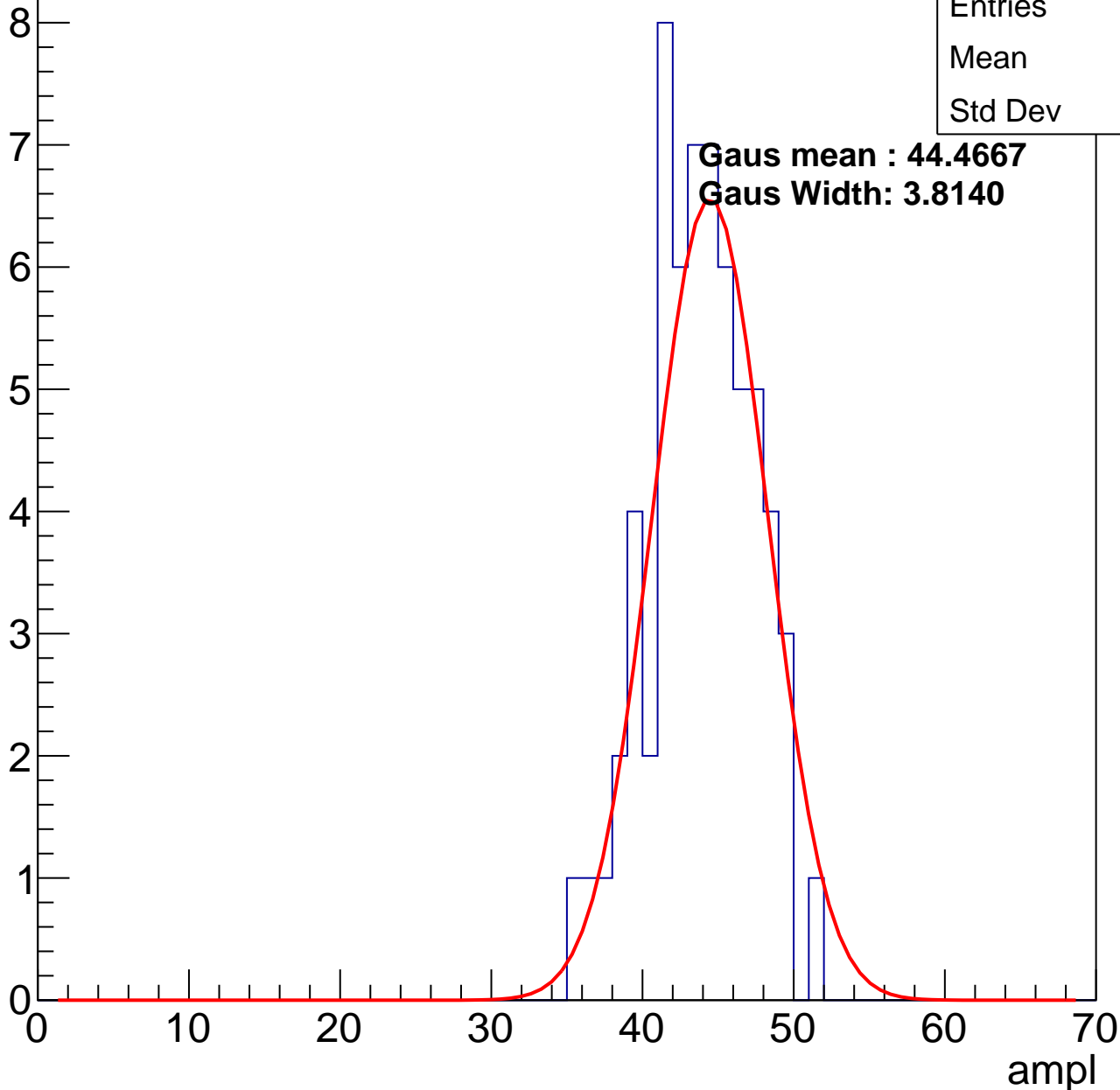
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	43.4
Std Dev	3.42

**Gaus mean : 44.4667**

**Gaus Width: 3.8140**



# B1L003S, U6-ch106, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

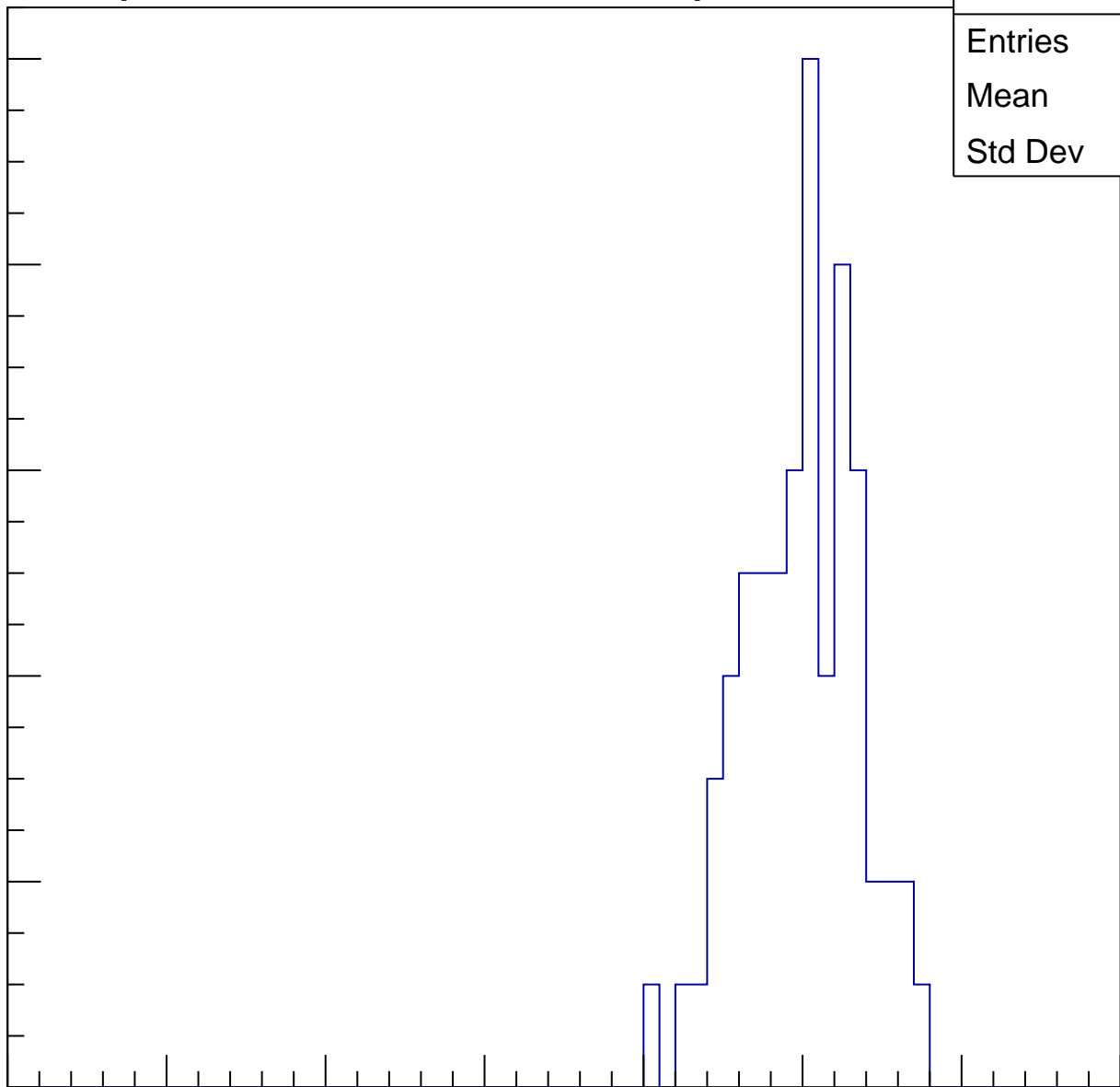
Entries	66
Mean	49.41
Std Dev	3.572

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

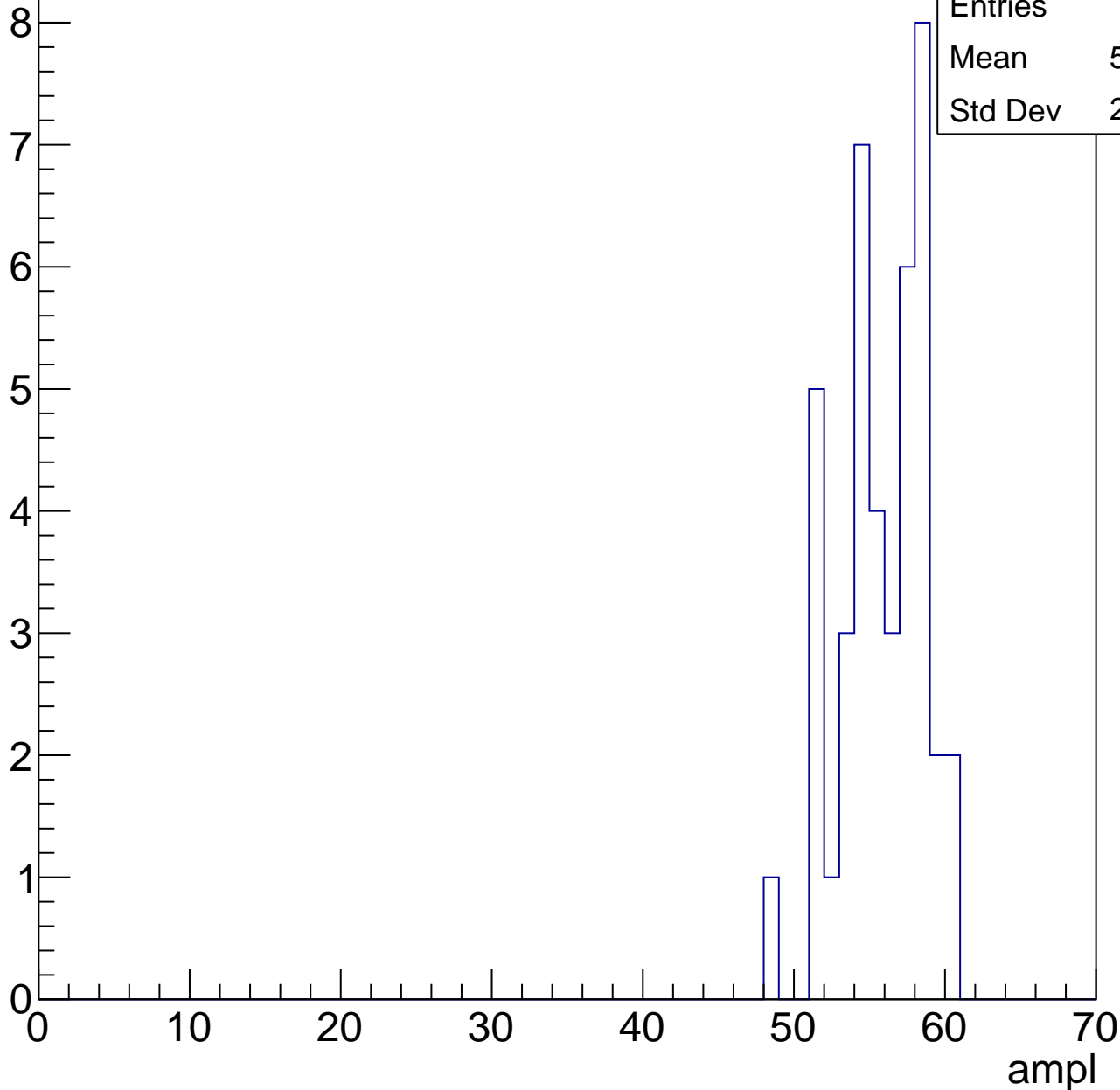


# B1L003S, U6-ch106, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

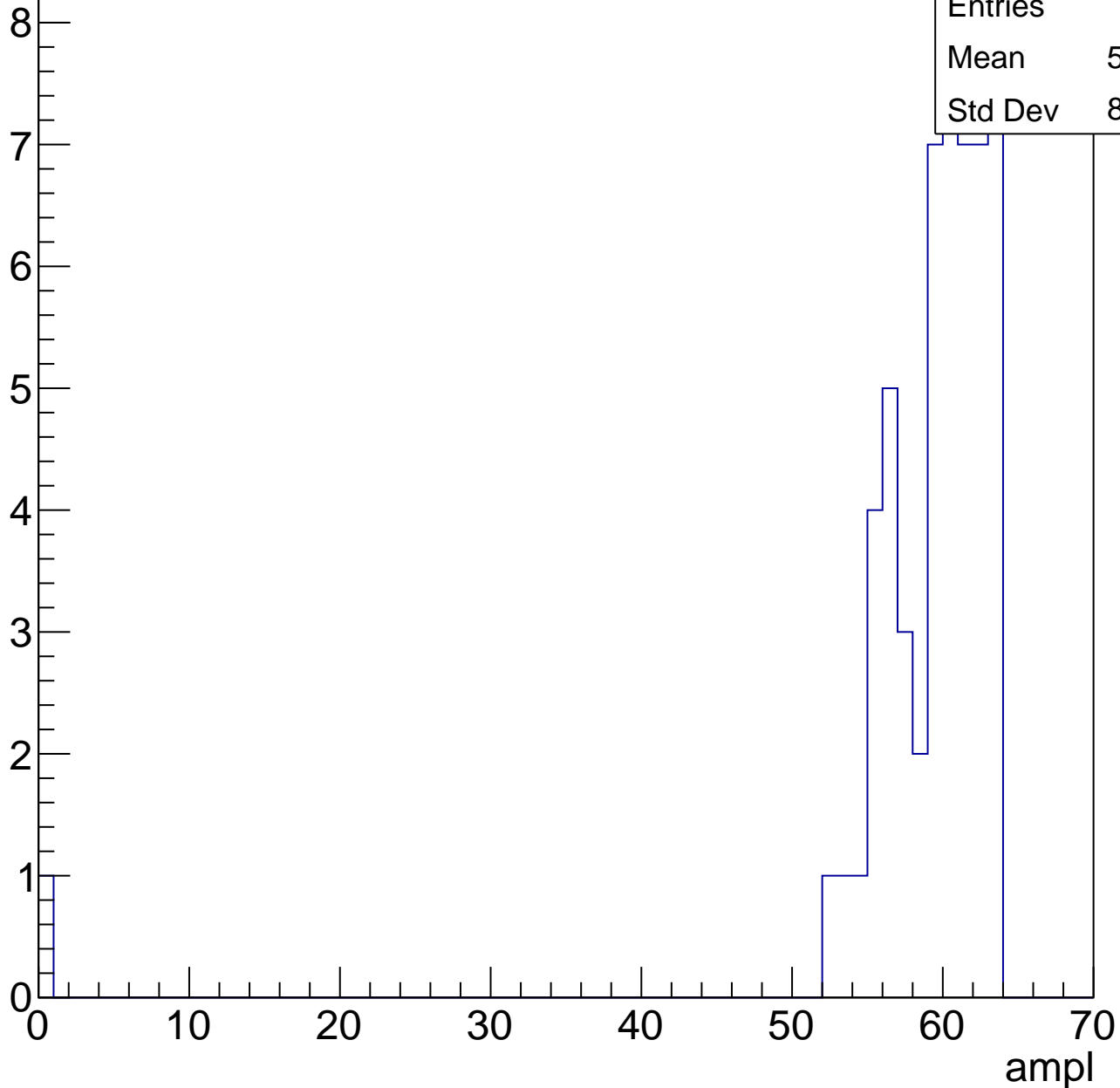
Entries	42
Mean	55.33
Std Dev	2.817



# B1L003S, U6-ch106, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

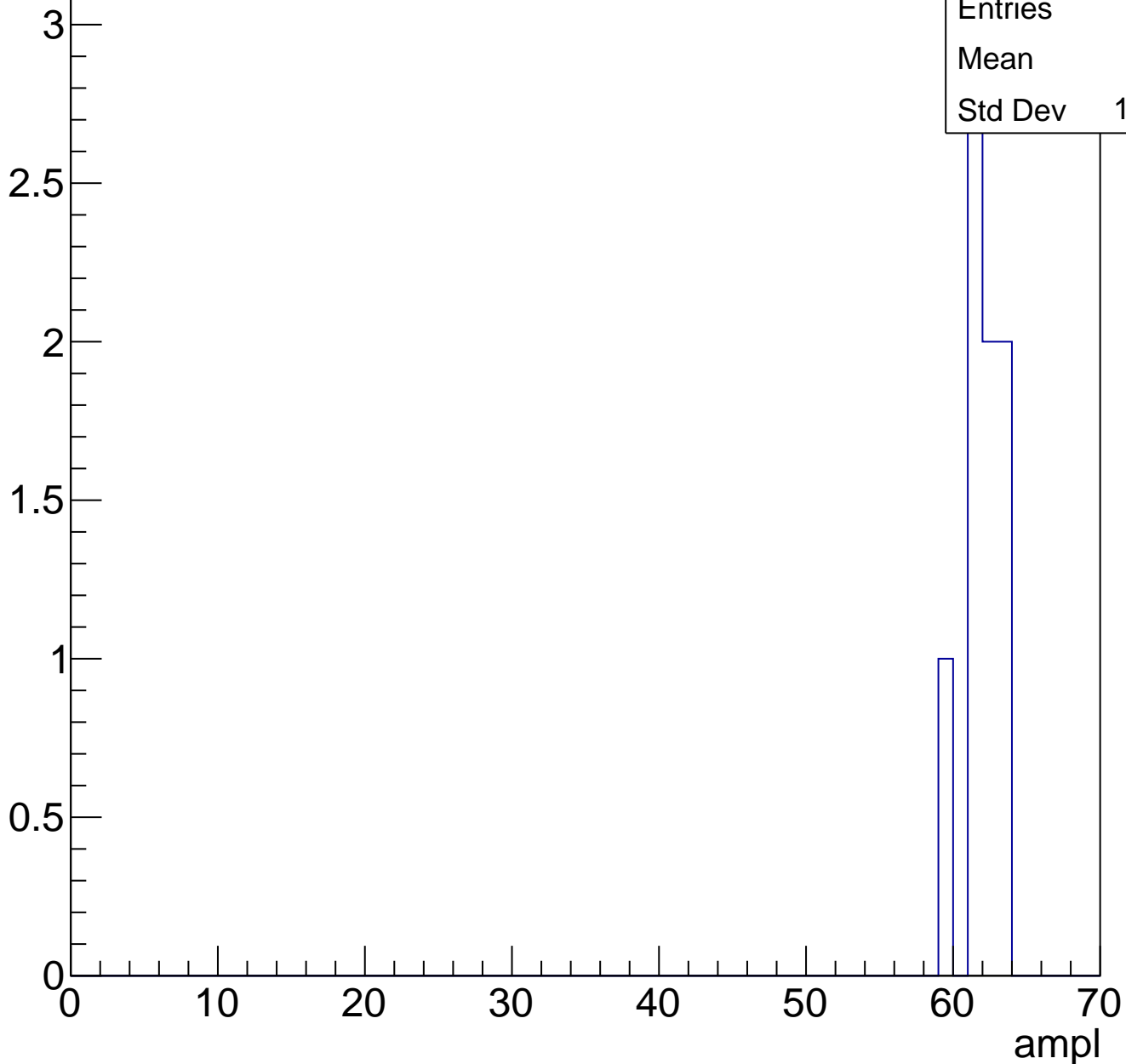


Entries	55
Mean	58.25
Std Dev	8.432

# B1L003S, U6-ch106, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch106, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch107, adc0

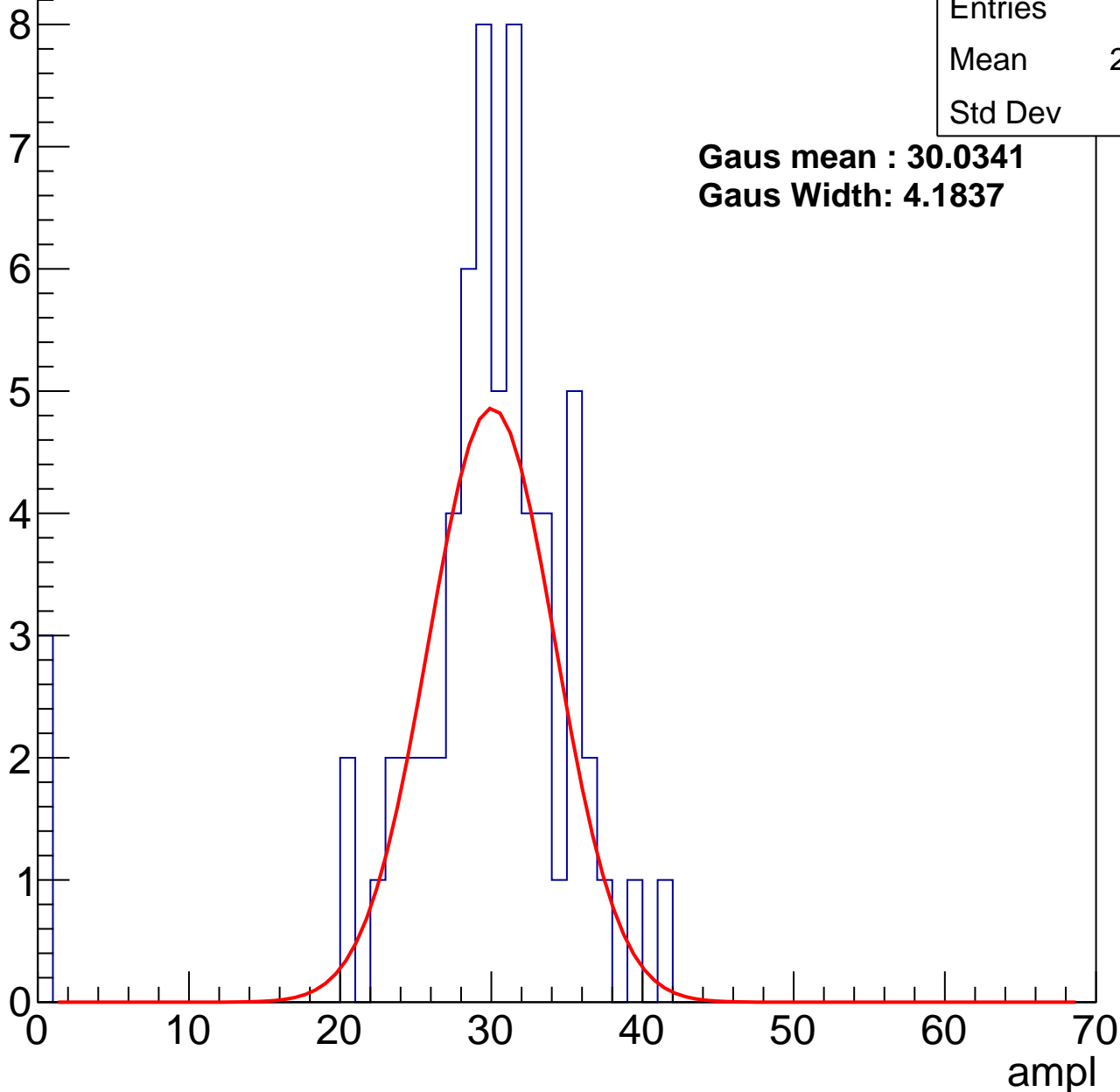
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	28.47
Std Dev	7.56

**Gaus mean : 30.0341**

**Gaus Width: 4.1837**



# B1L003S, U6-ch107, adc1

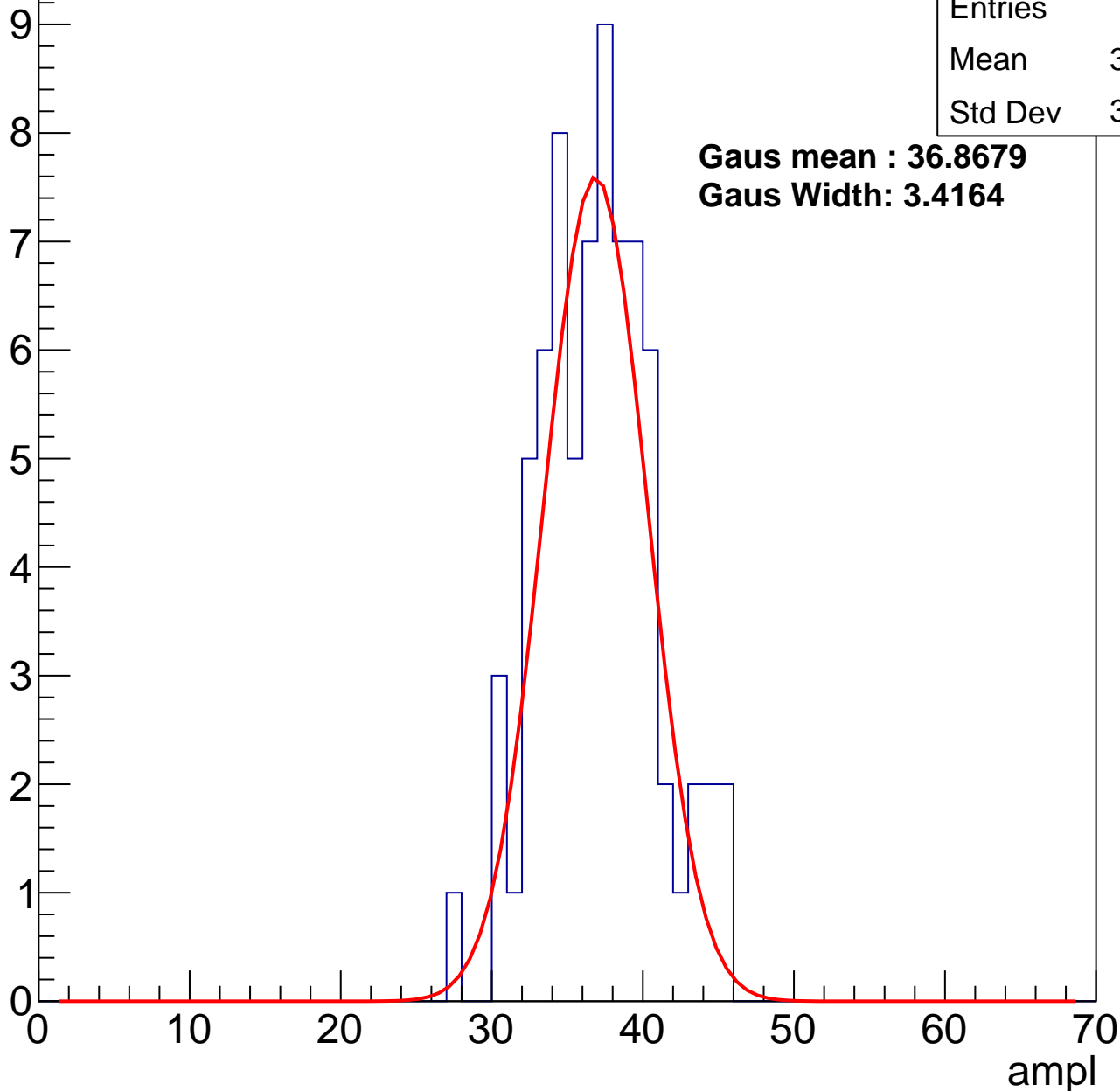
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	74
Mean	36.55
Std Dev	3.735

**Gaus mean : 36.8679**

**Gaus Width: 3.4164**



# B1L003S, U6-ch107, adc2

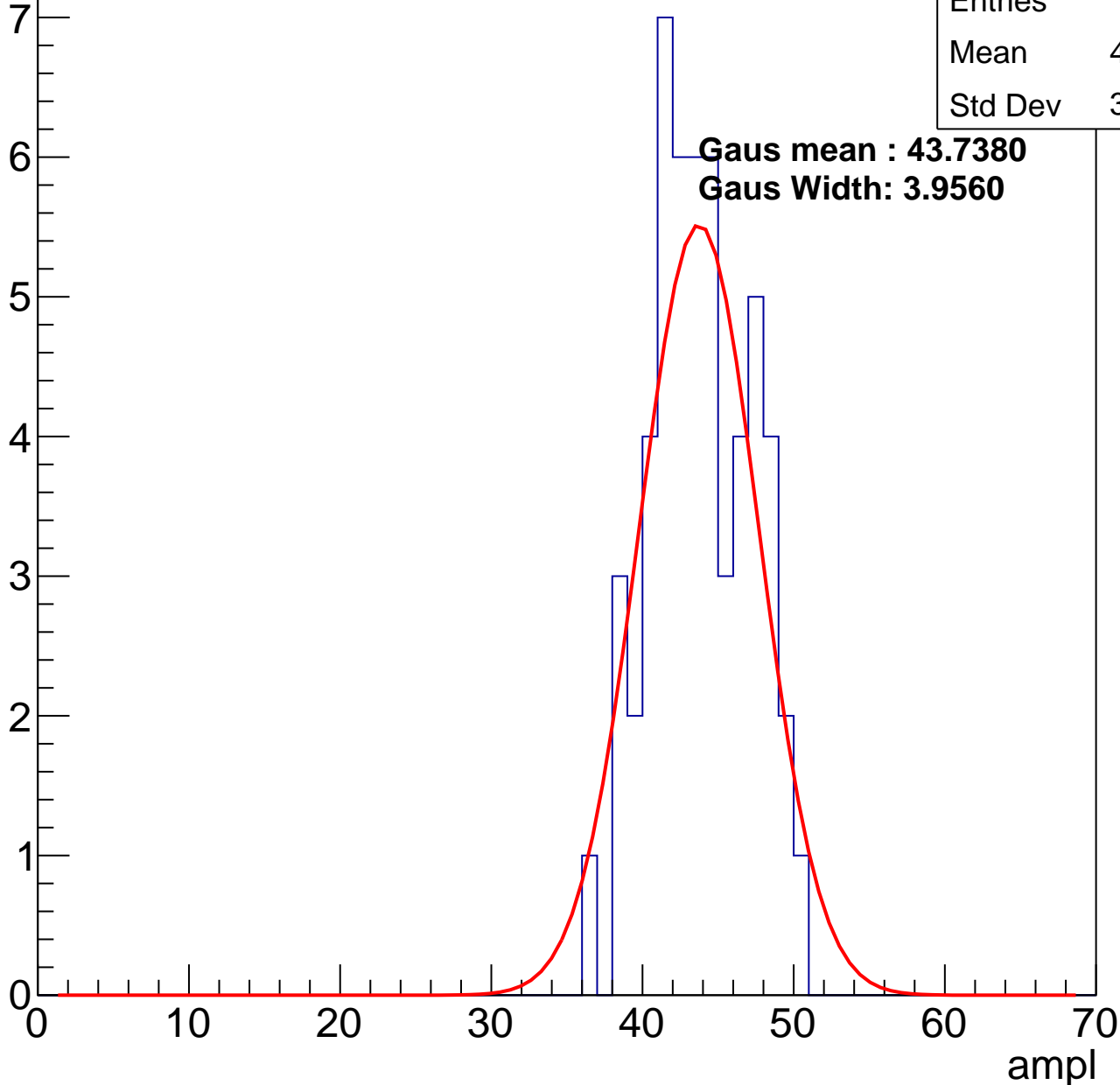
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	54
Mean	43.39
Std Dev	3.257

**Gaus mean : 43.7380**

**Gaus Width: 3.9560**

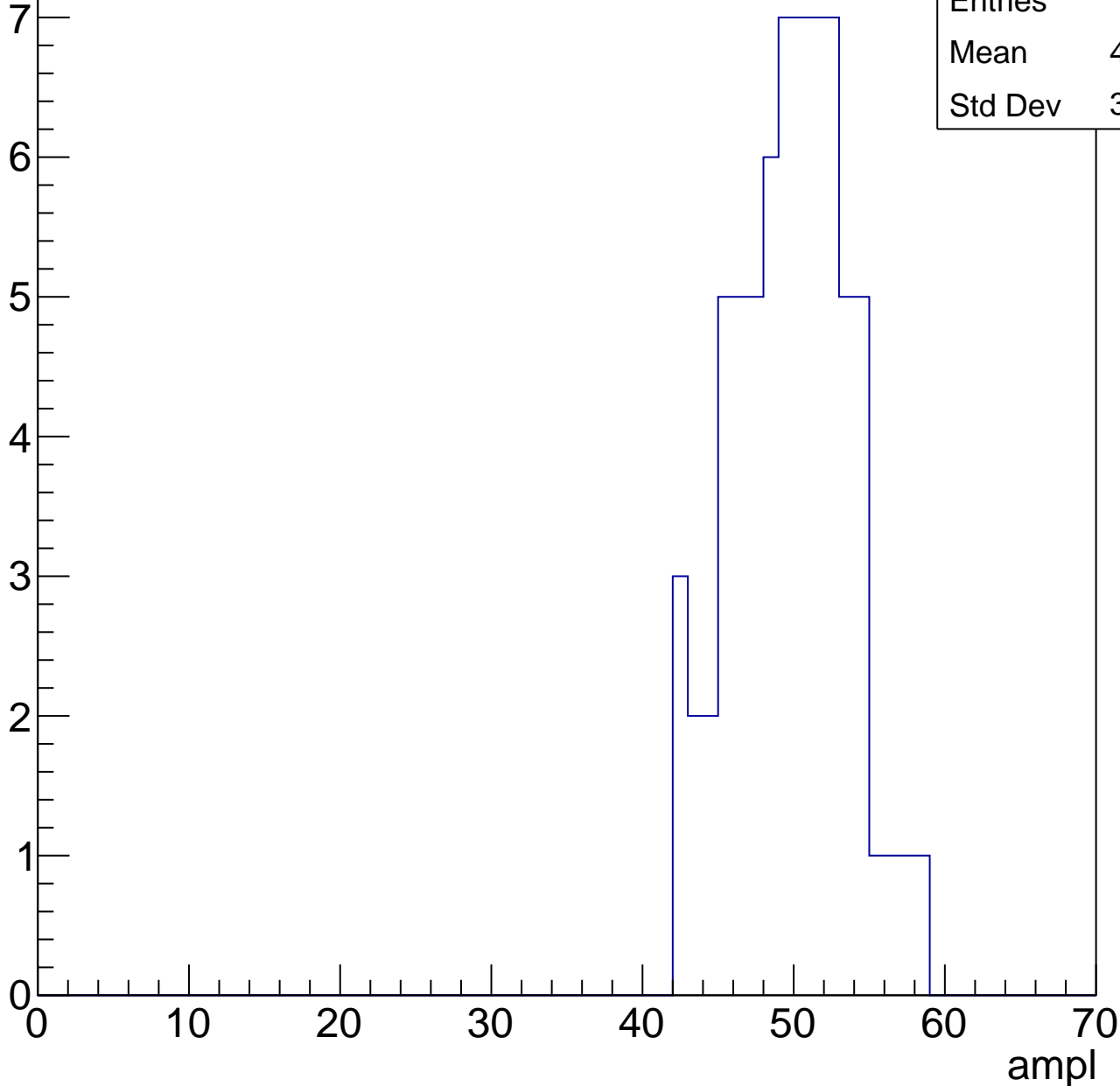


# B1L003S, U6-ch107, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	49.33
Std Dev	3.675

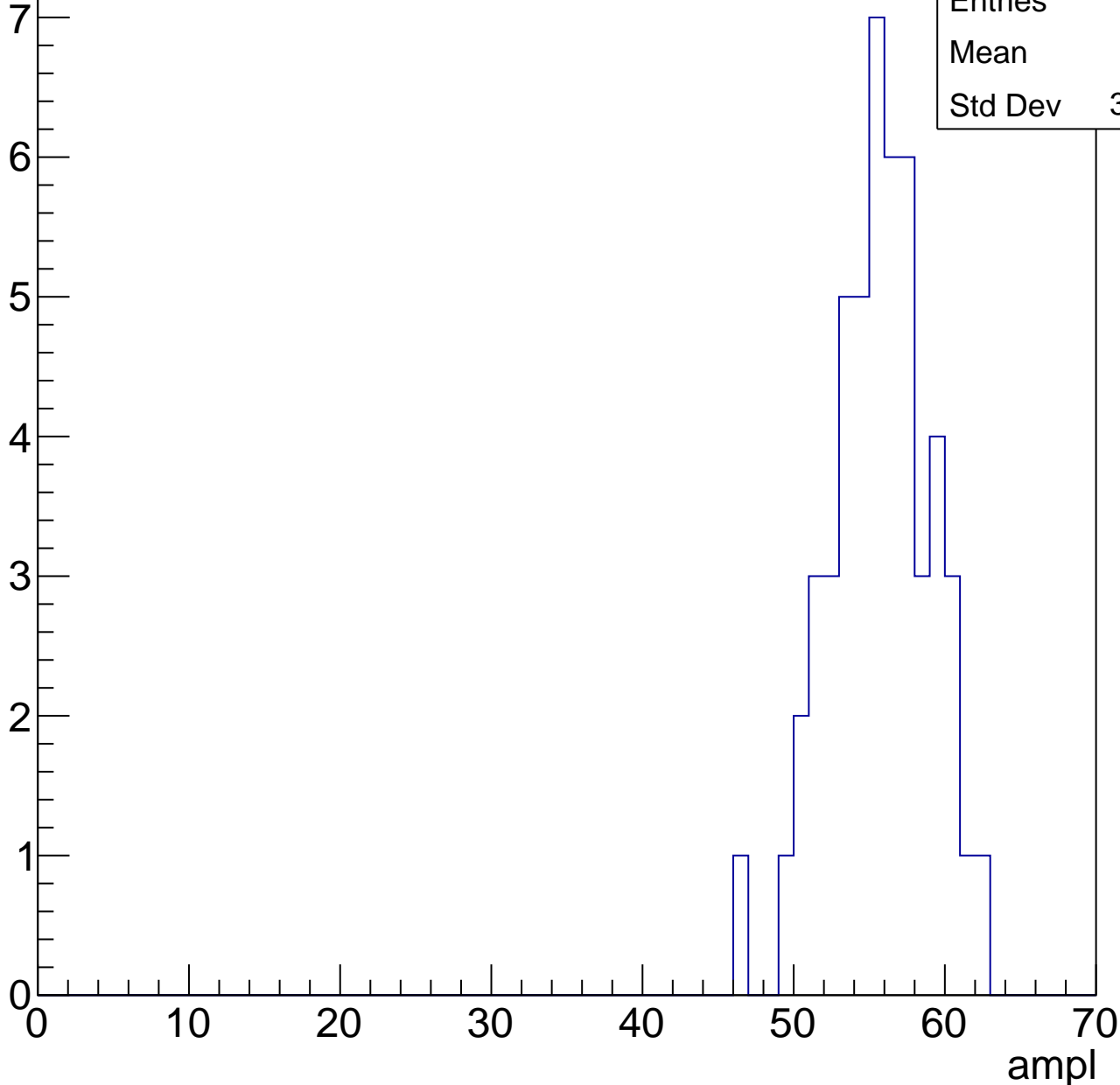


# B1L003S, U6-ch107, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	51
Mean	55.2
Std Dev	3.272

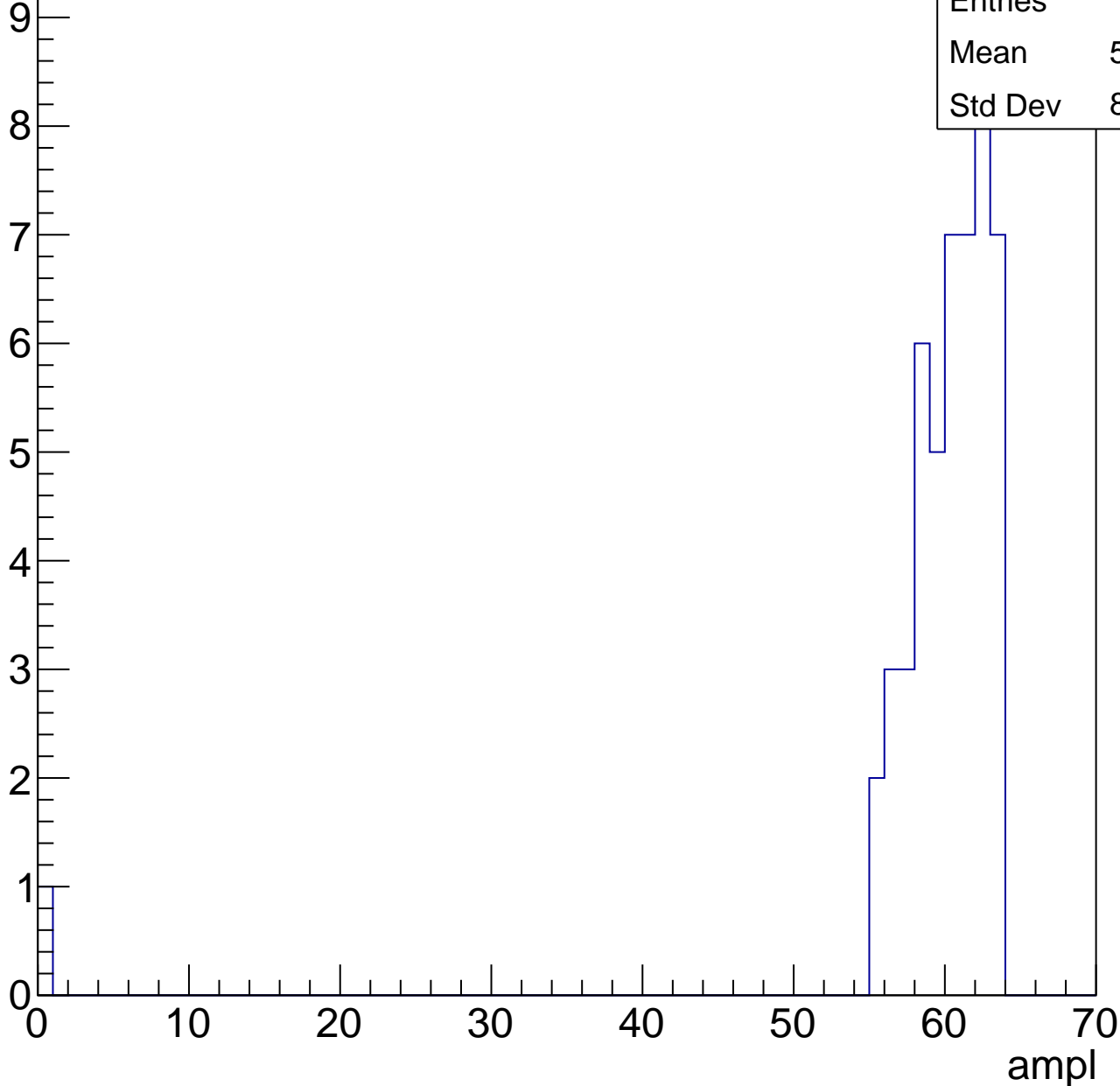


# B1L003S, U6-ch107, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

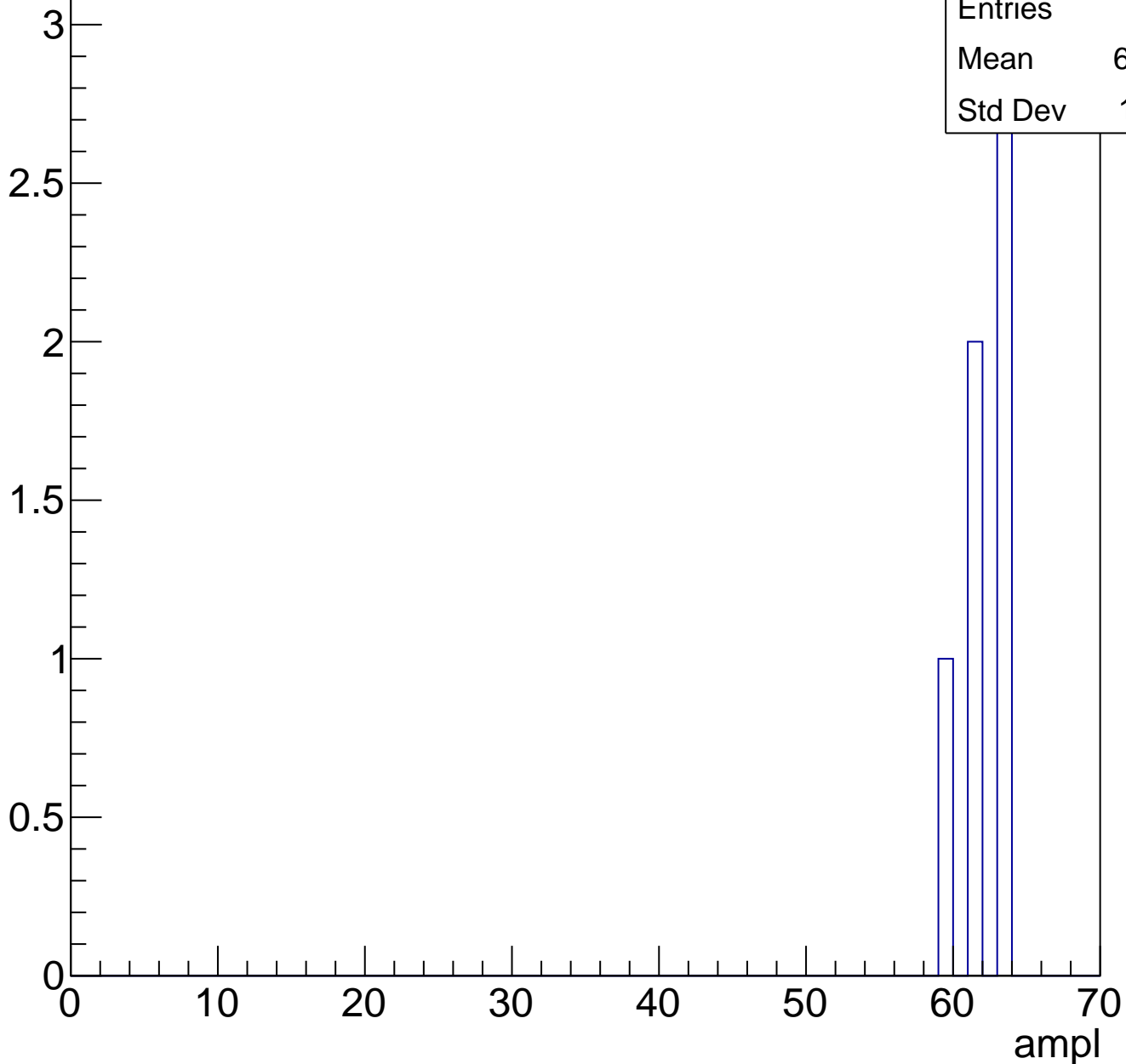
Entries	50
Mean	58.76
Std Dev	8.698



# B1L003S, U6-ch107, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch107, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U6-ch108, adc0

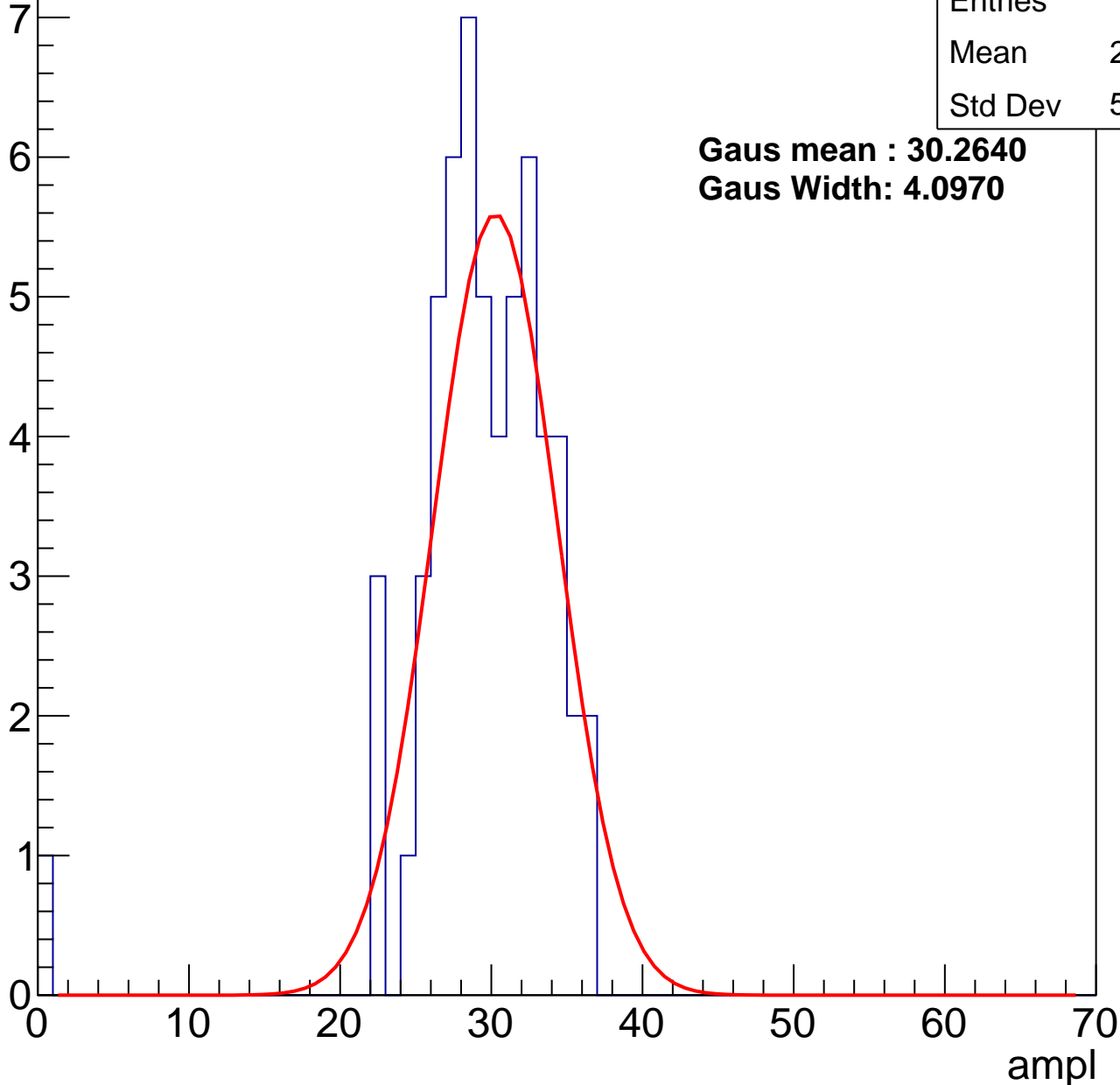
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	28.88
Std Dev	5.166

**Gaus mean : 30.2640**

**Gaus Width: 4.0970**



# B1L003S, U6-ch108, adc1

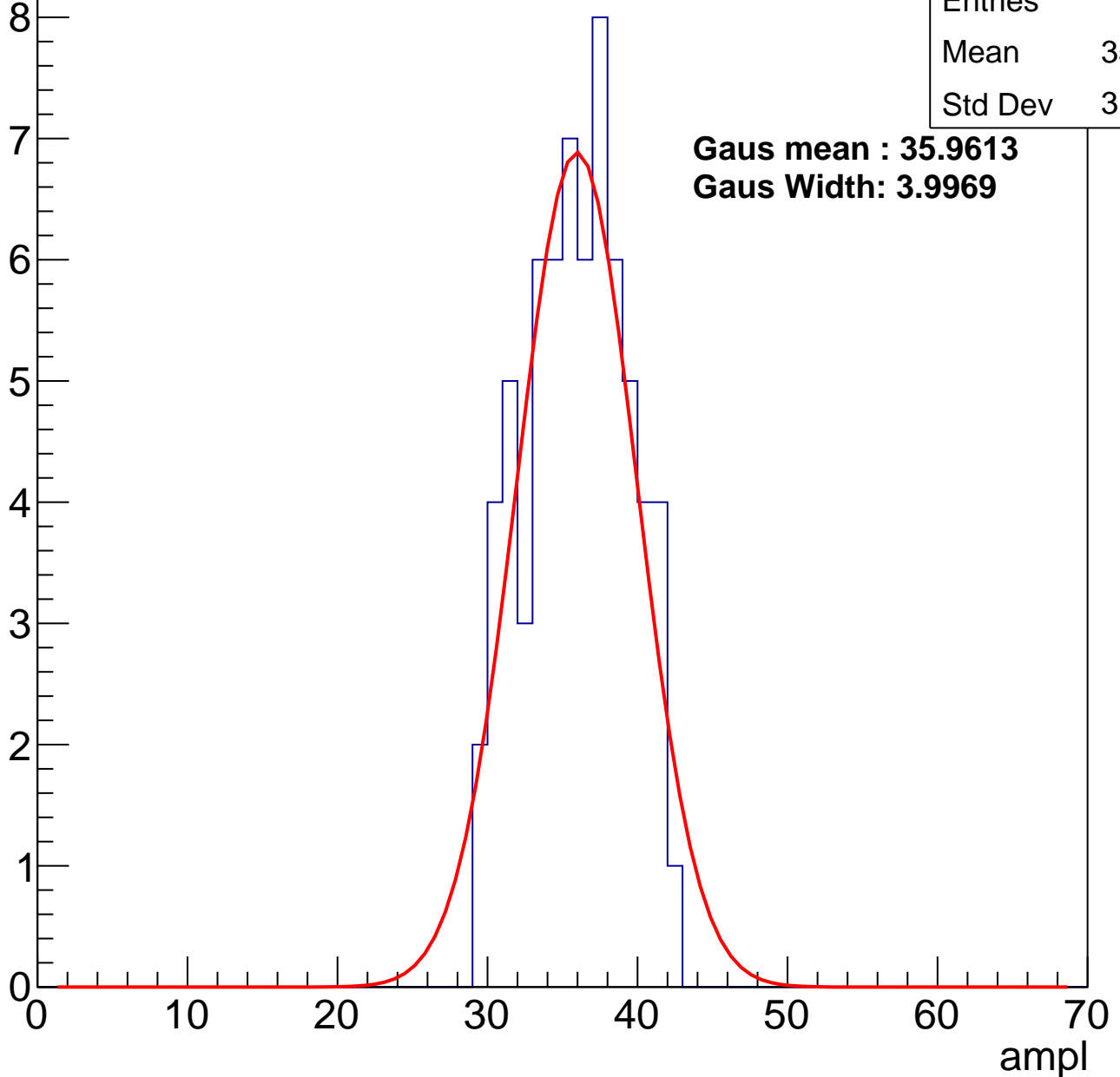
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	35.48
Std Dev	3.365

**Gaus mean : 35.9613**

**Gaus Width: 3.9969**



# B1L003S, U6-ch108, adc2

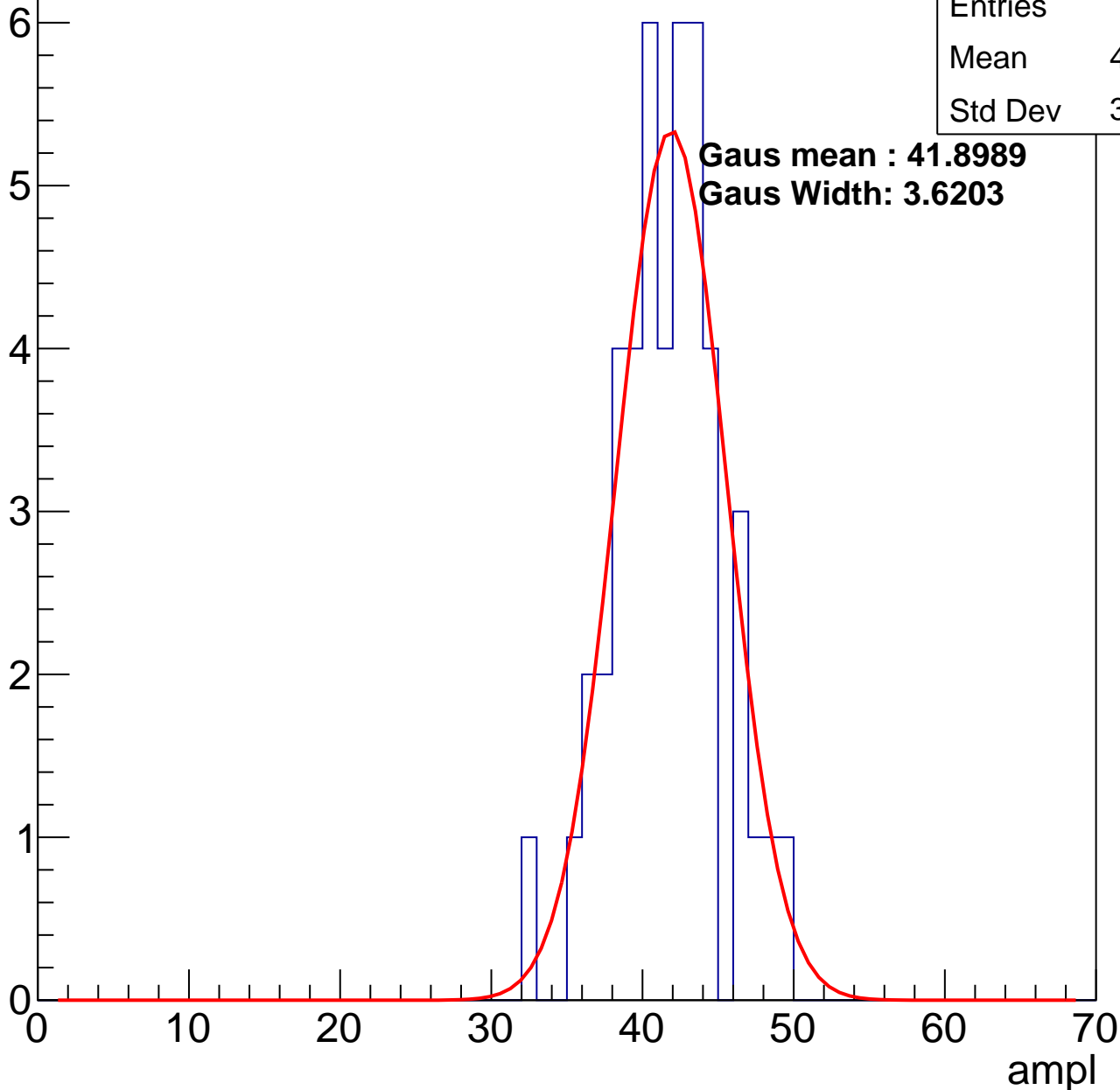
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	46
Mean	41.15
Std Dev	3.445

**Gaus mean : 41.8989**

**Gaus Width: 3.6203**

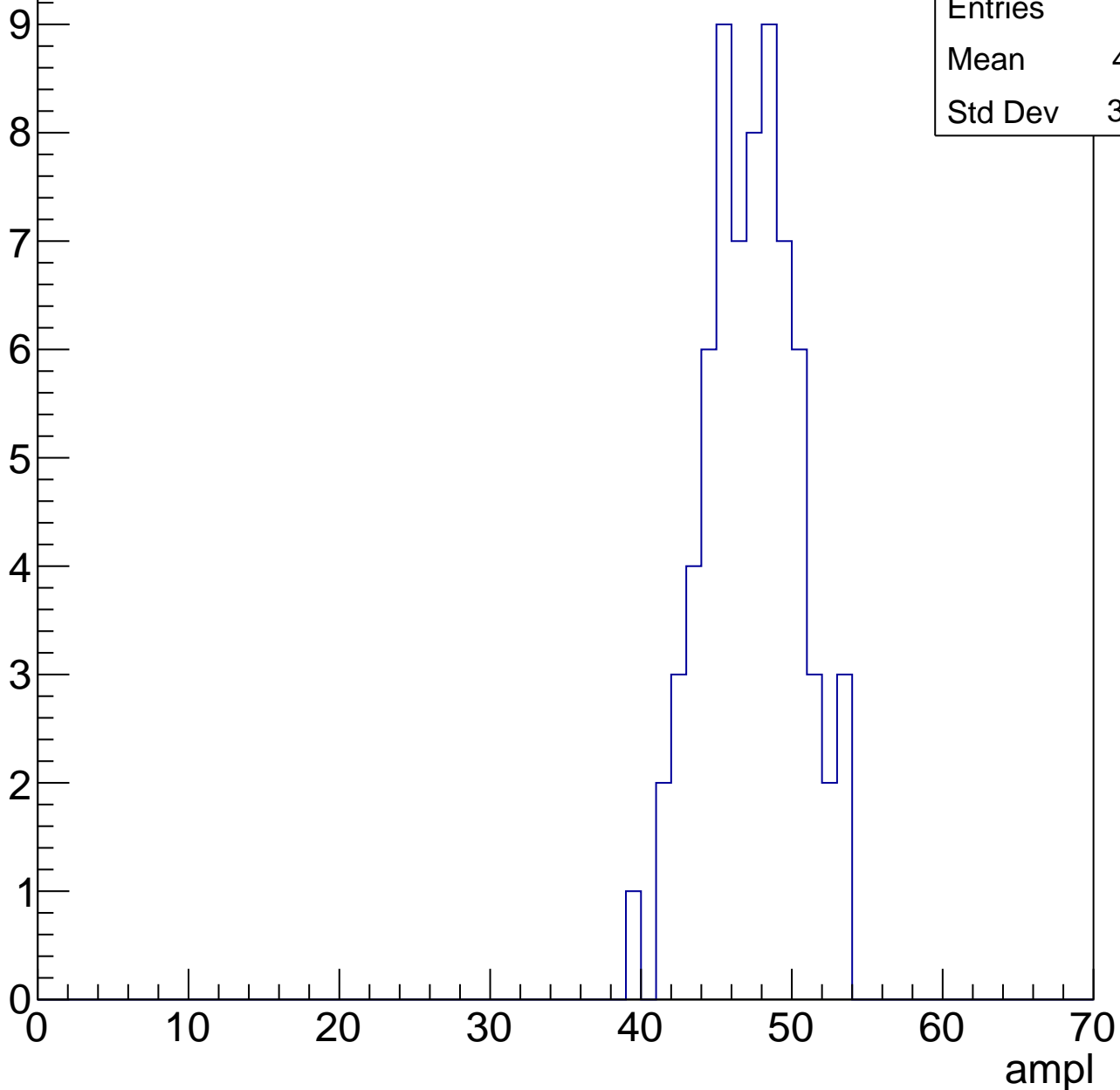


# B1L003S, U6-ch108, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	46.81
Std Dev	3.086

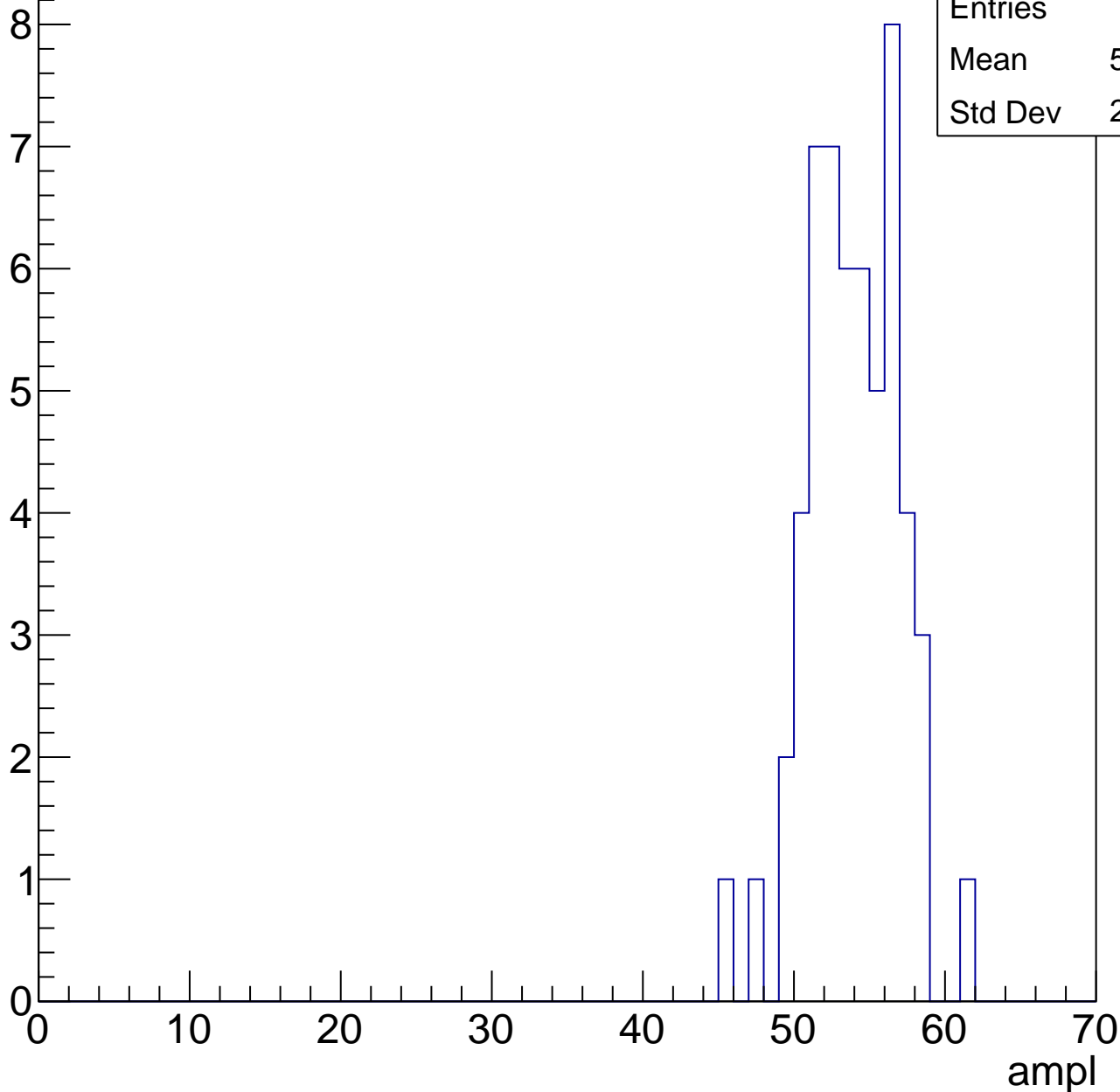


# B1L003S, U6-ch108, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	53.44
Std Dev	2.996

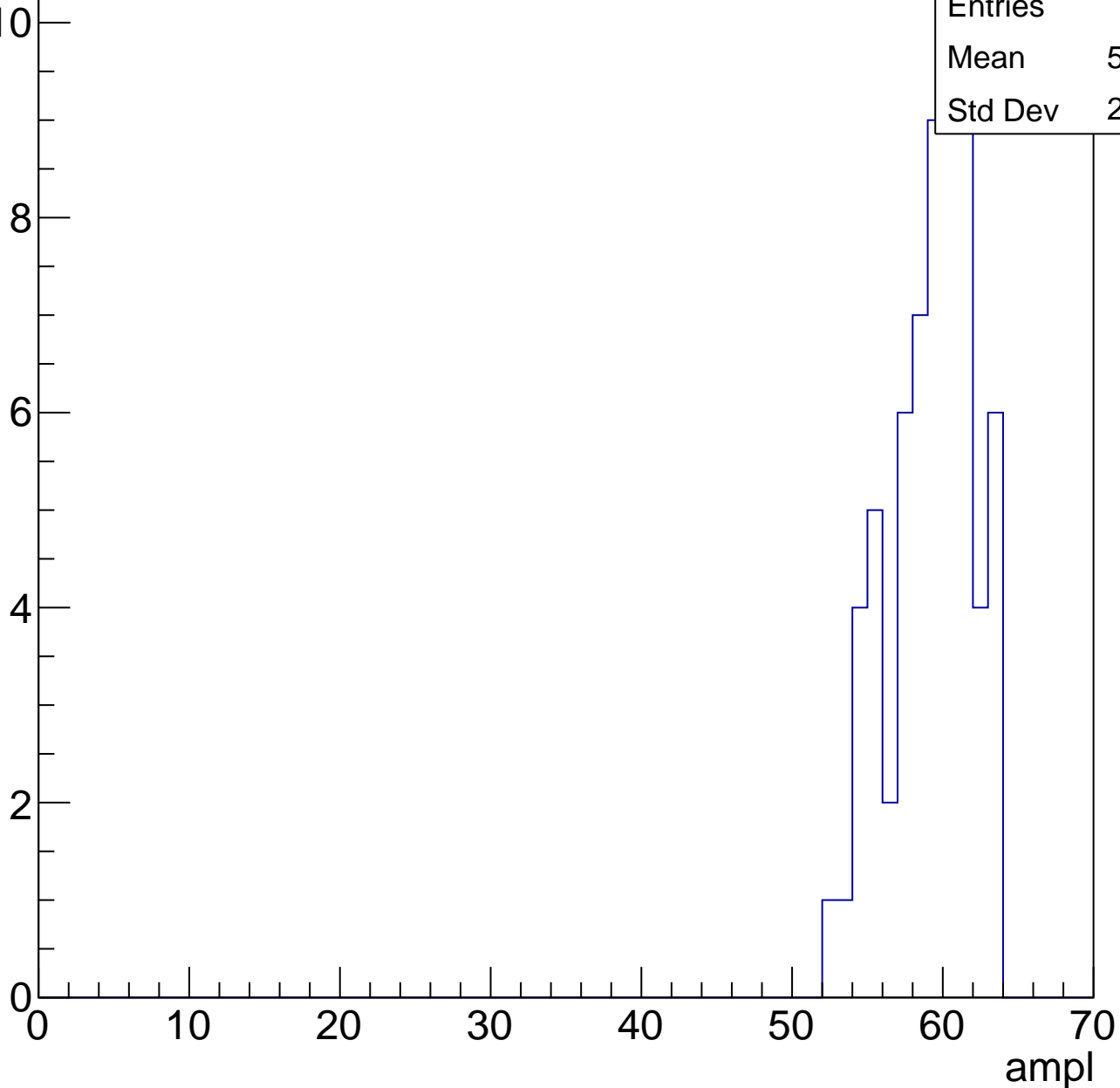


# B1L003S, U6-ch108, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	58.78
Std Dev	2.764

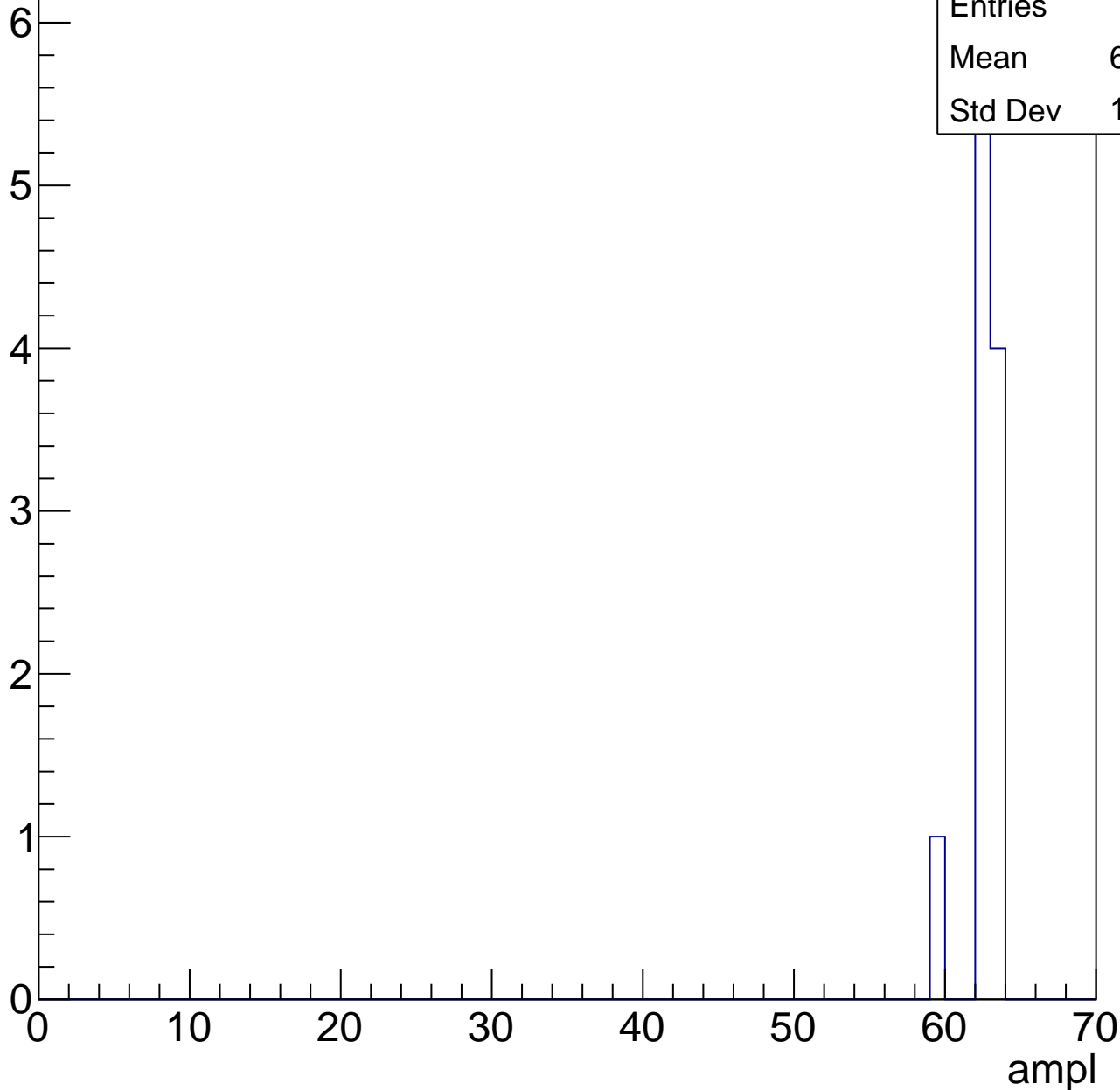


# B1L003S, U6-ch108, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	11
Mean	62.09
Std Dev	1.083





# B1L003S, U6-ch108, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch109, adc0

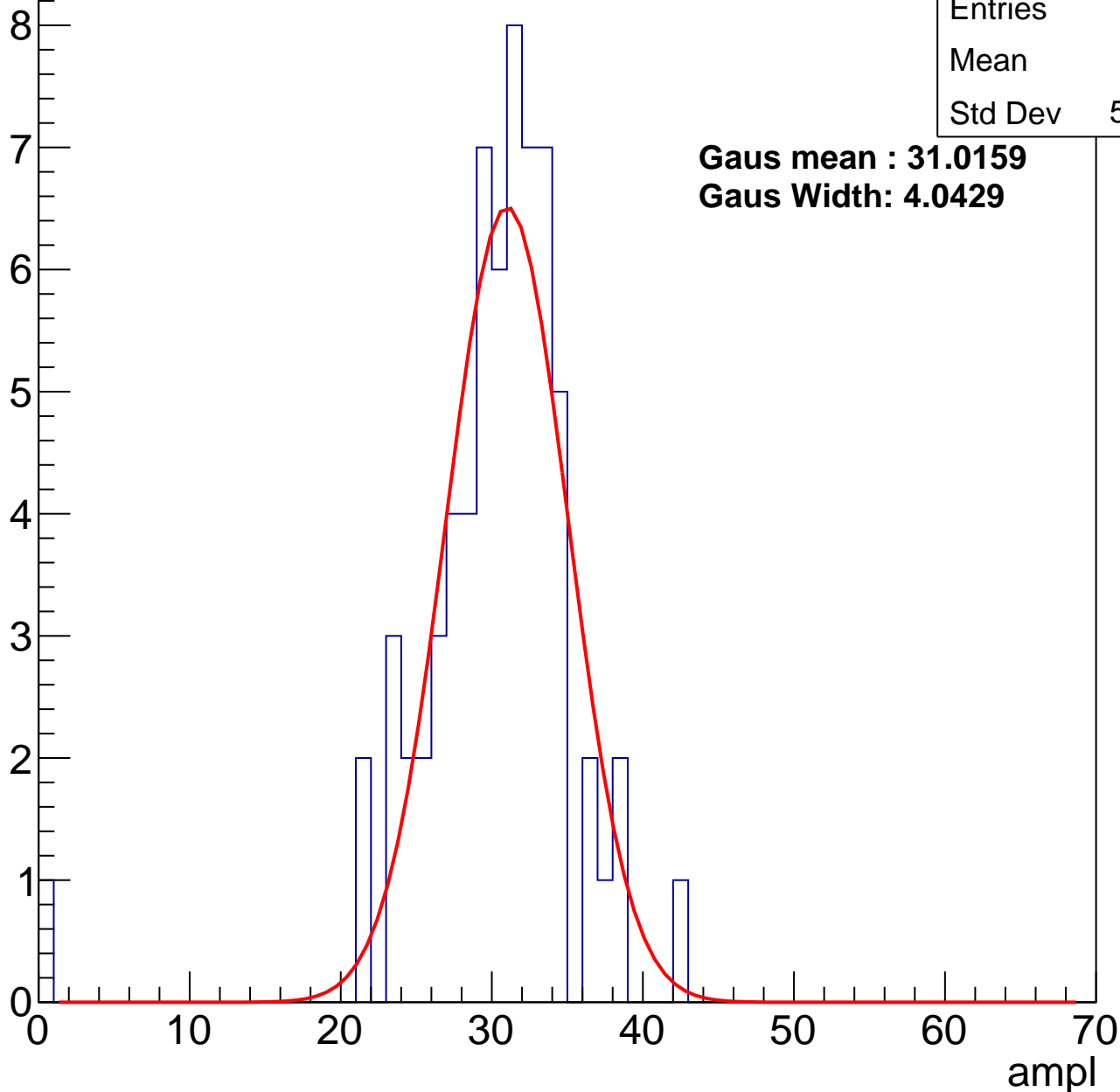
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	29.7
Std Dev	5.469

**Gaus mean : 31.0159**

**Gaus Width: 4.0429**



# B1L003S, U6-ch109, adc1

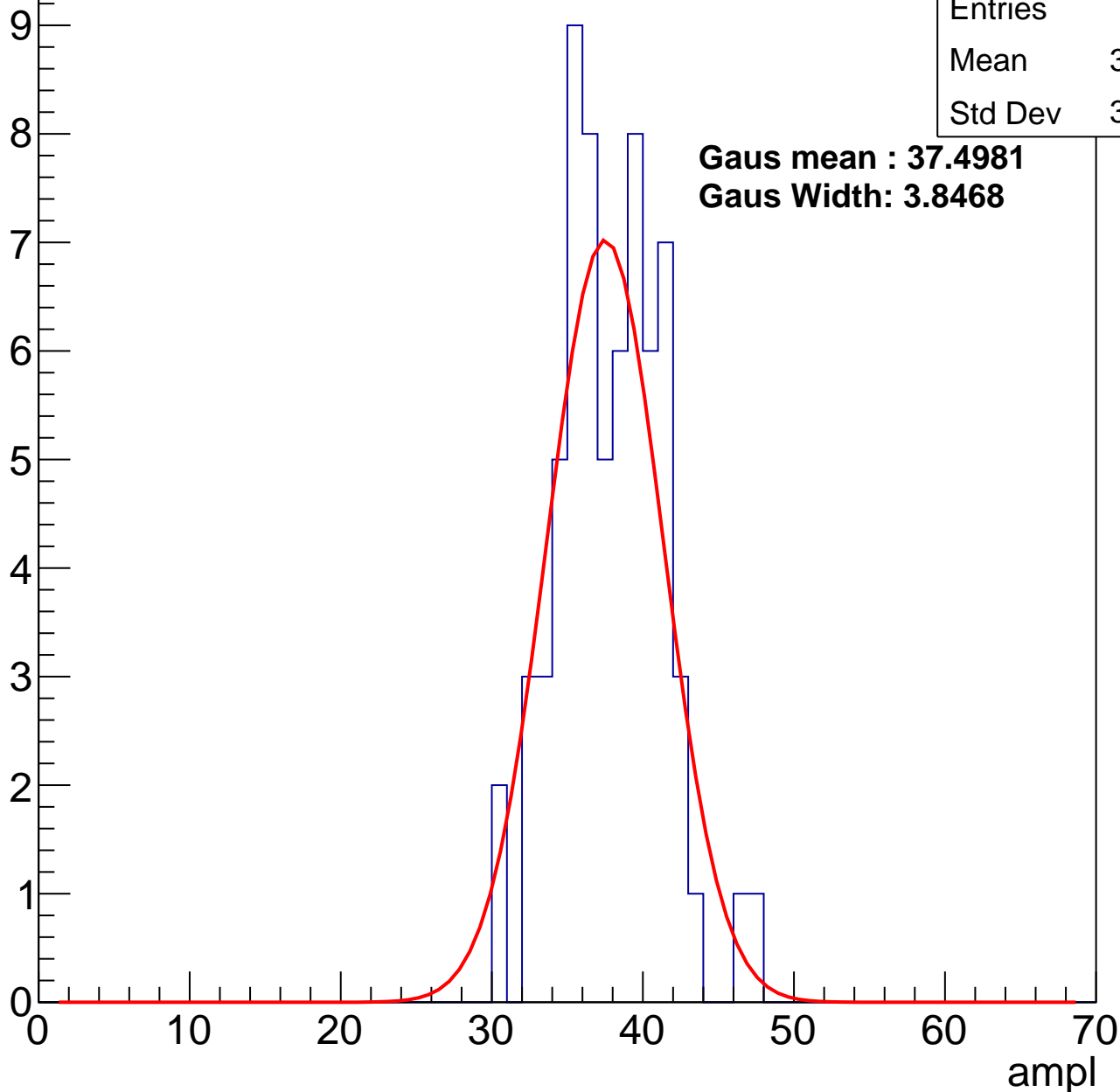
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	37.38
Std Dev	3.422

**Gaus mean : 37.4981**

**Gaus Width: 3.8468**

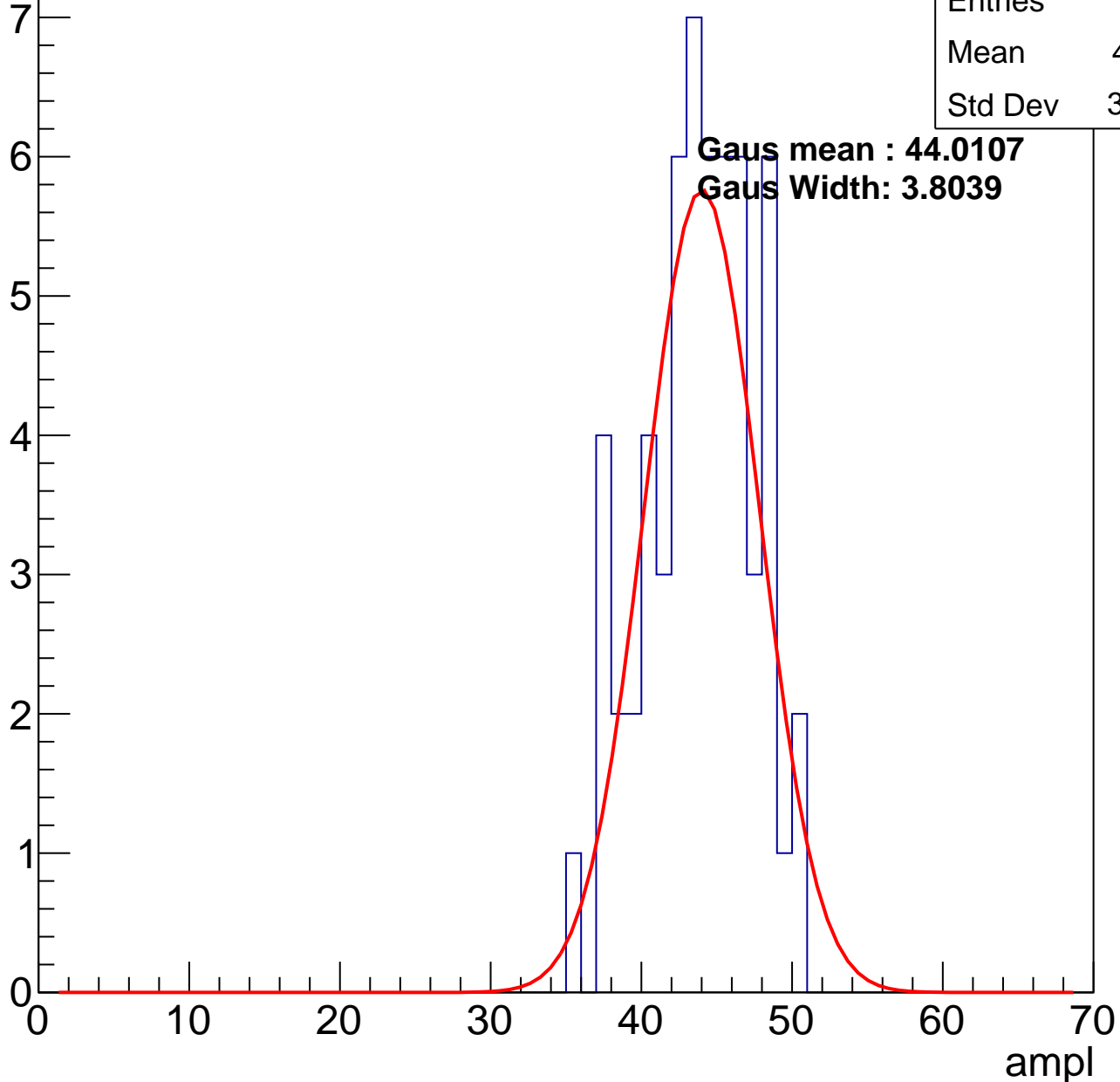


# B1L003S, U6-ch109, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

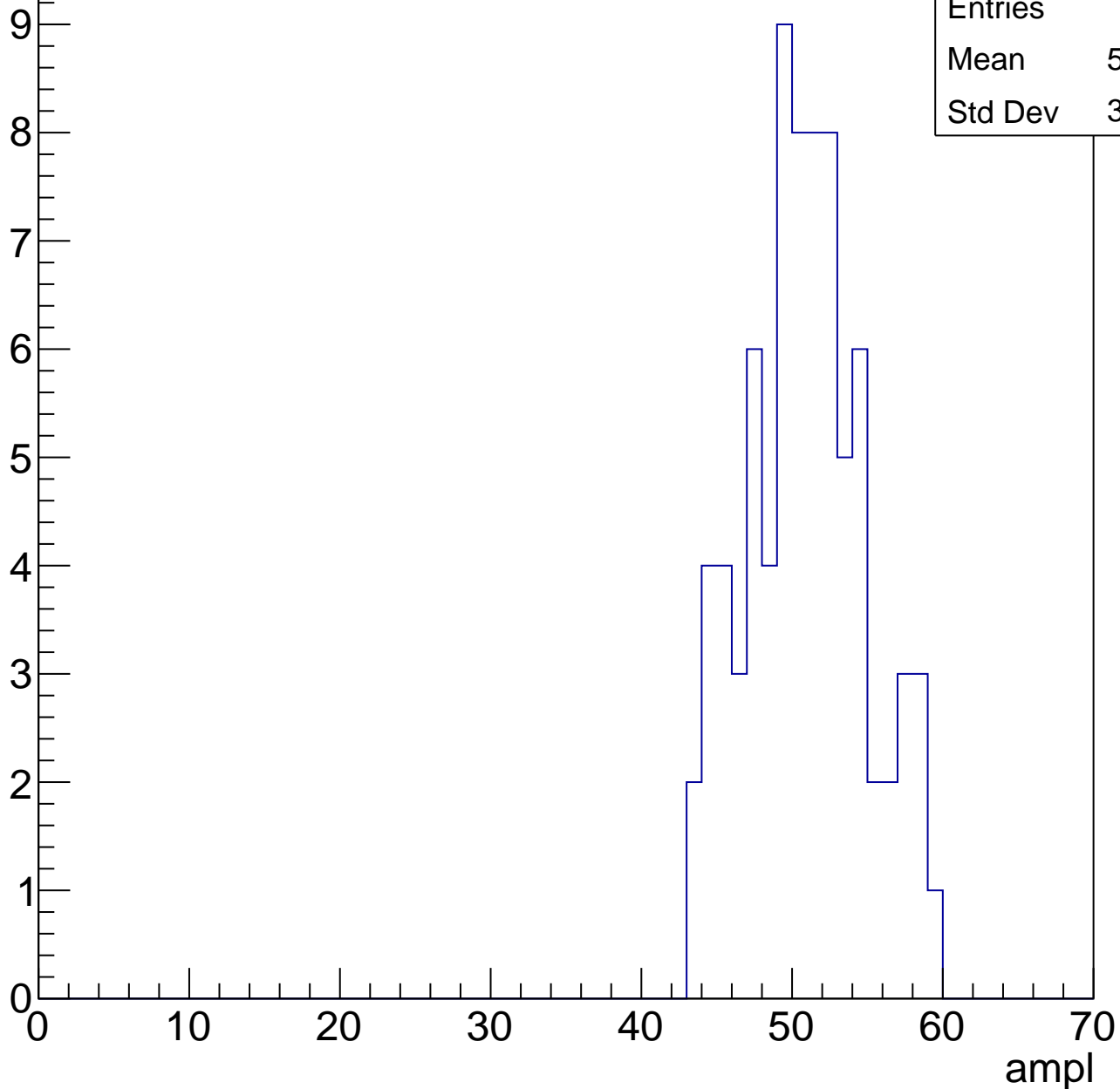
Entries	59
Mean	43.41
Std Dev	3.566



# B1L003S, U6-ch109, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



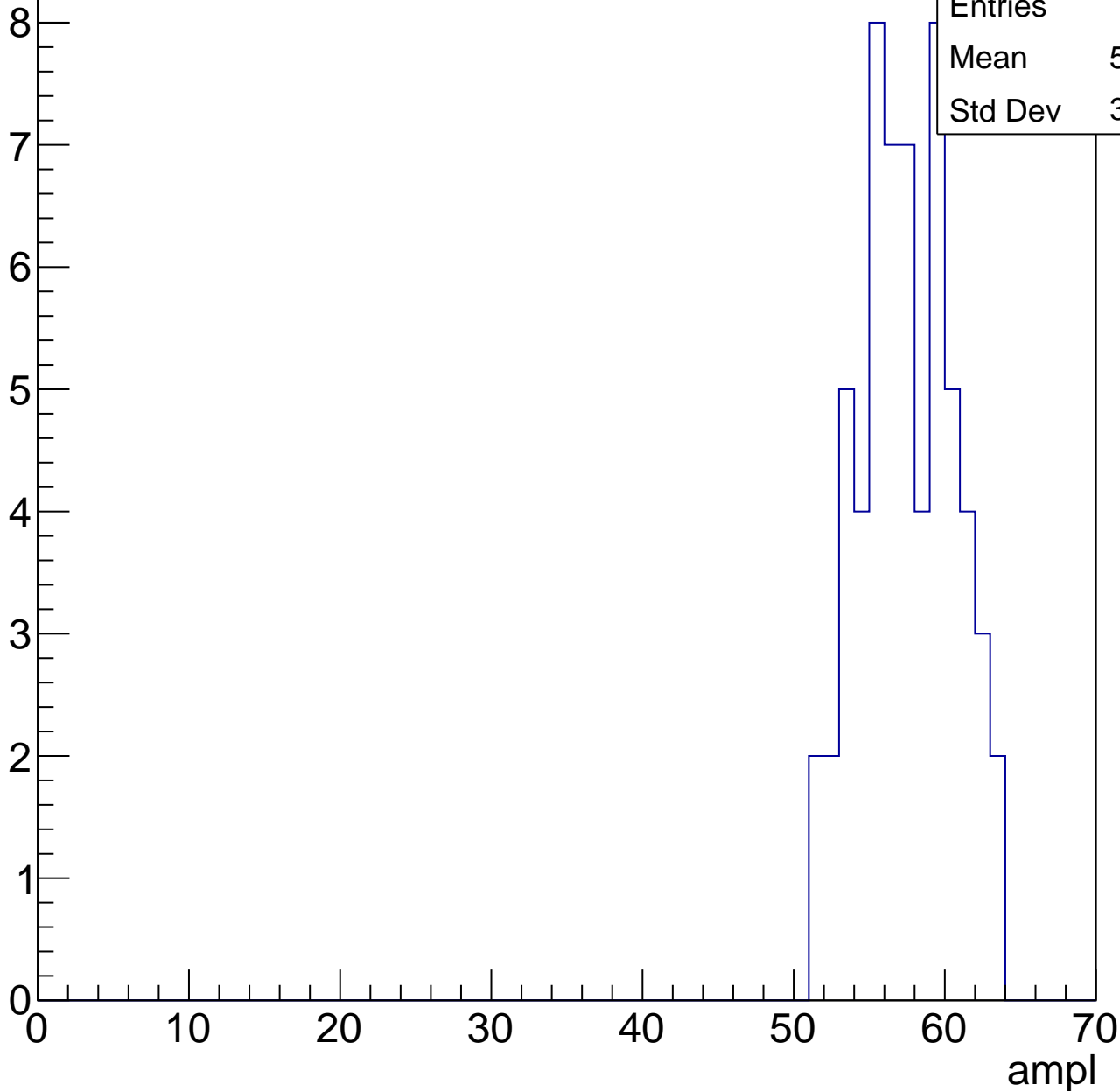
Entries	78
Mean	50.44
Std Dev	3.885

# B1L003S, U6-ch109, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	57.02
Std Dev	3.054

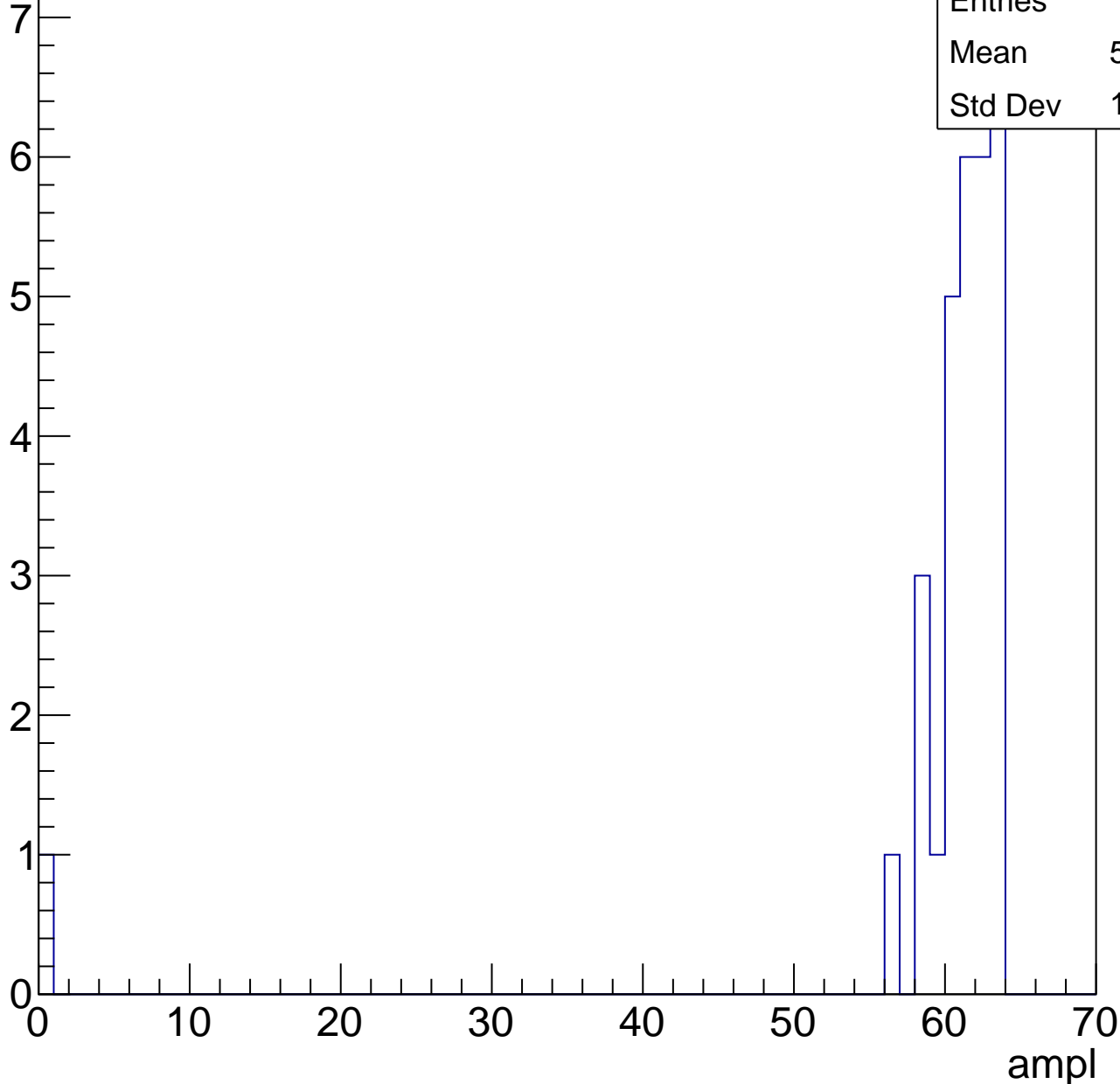


# B1L003S, U6-ch109, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	30
Mean	58.93
Std Dev	11.09



# B1L003S, U6-ch109, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch109, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch110, adc0

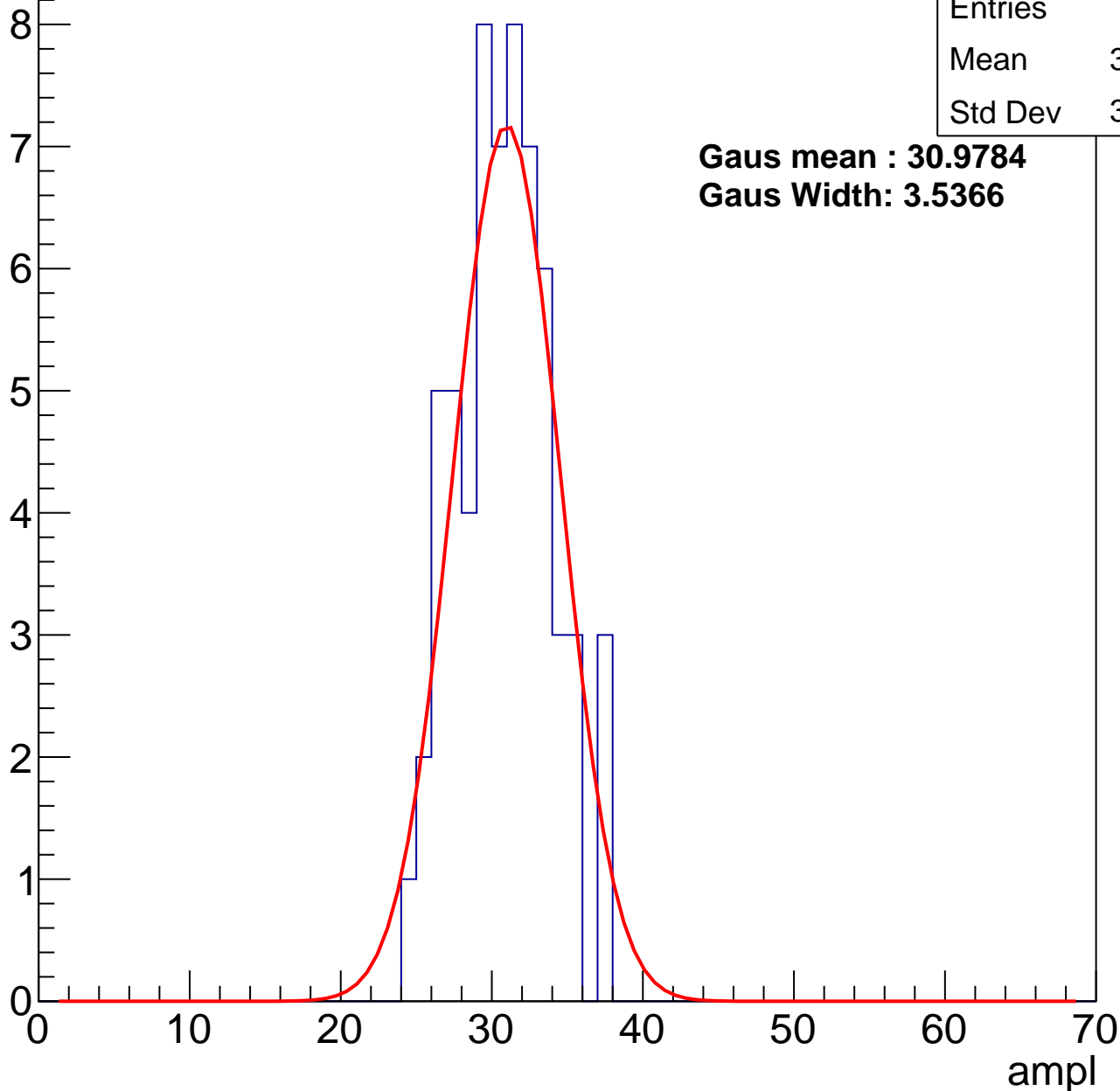
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	30.34
Std Dev	3.079

**Gaus mean : 30.9784**

**Gaus Width: 3.5366**



# B1L003S, U6-ch110, adc1

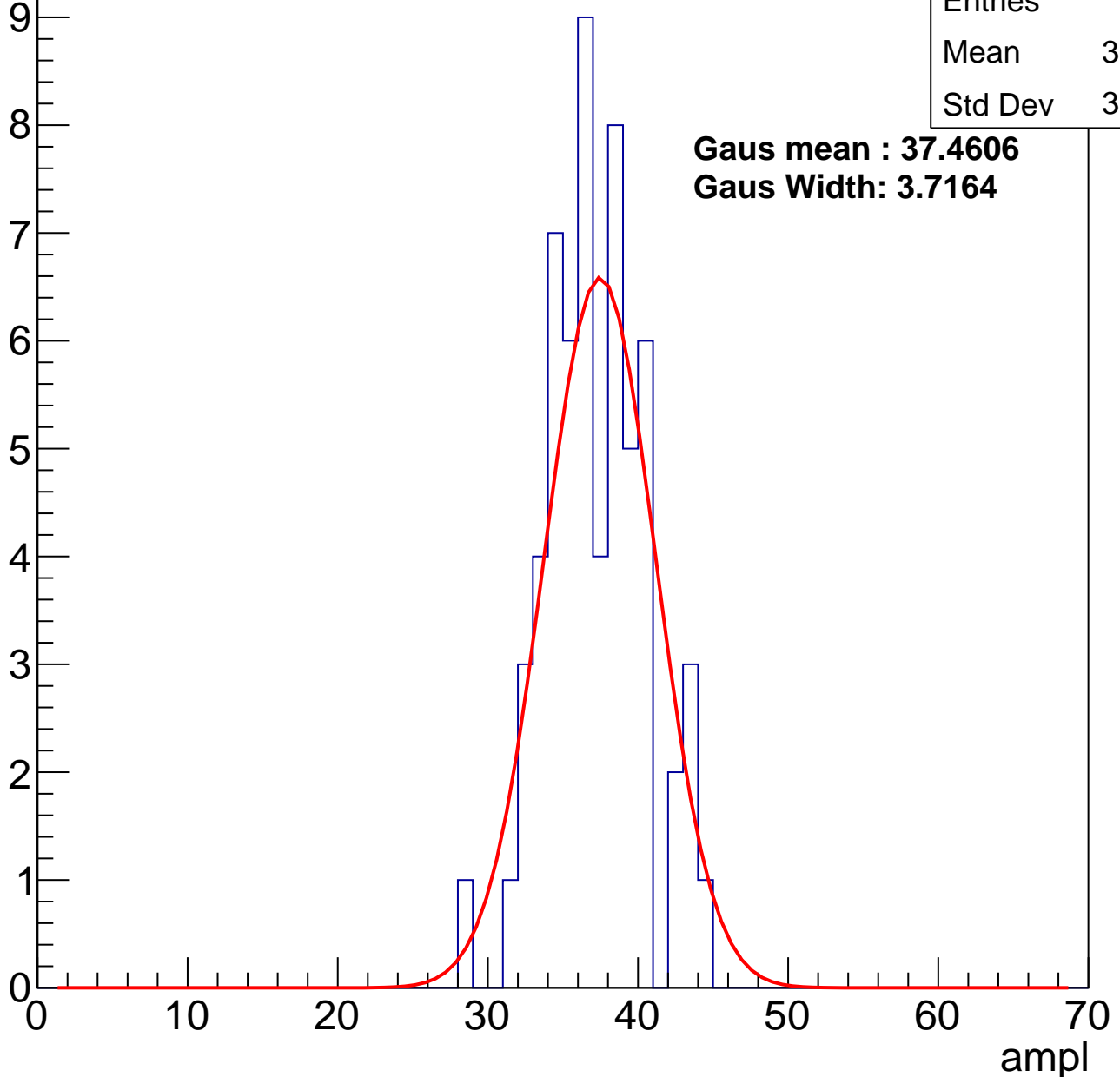
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	36.72
Std Dev	3.256

**Gaus mean : 37.4606**

**Gaus Width: 3.7164**



# B1L003S, U6-ch110, adc2

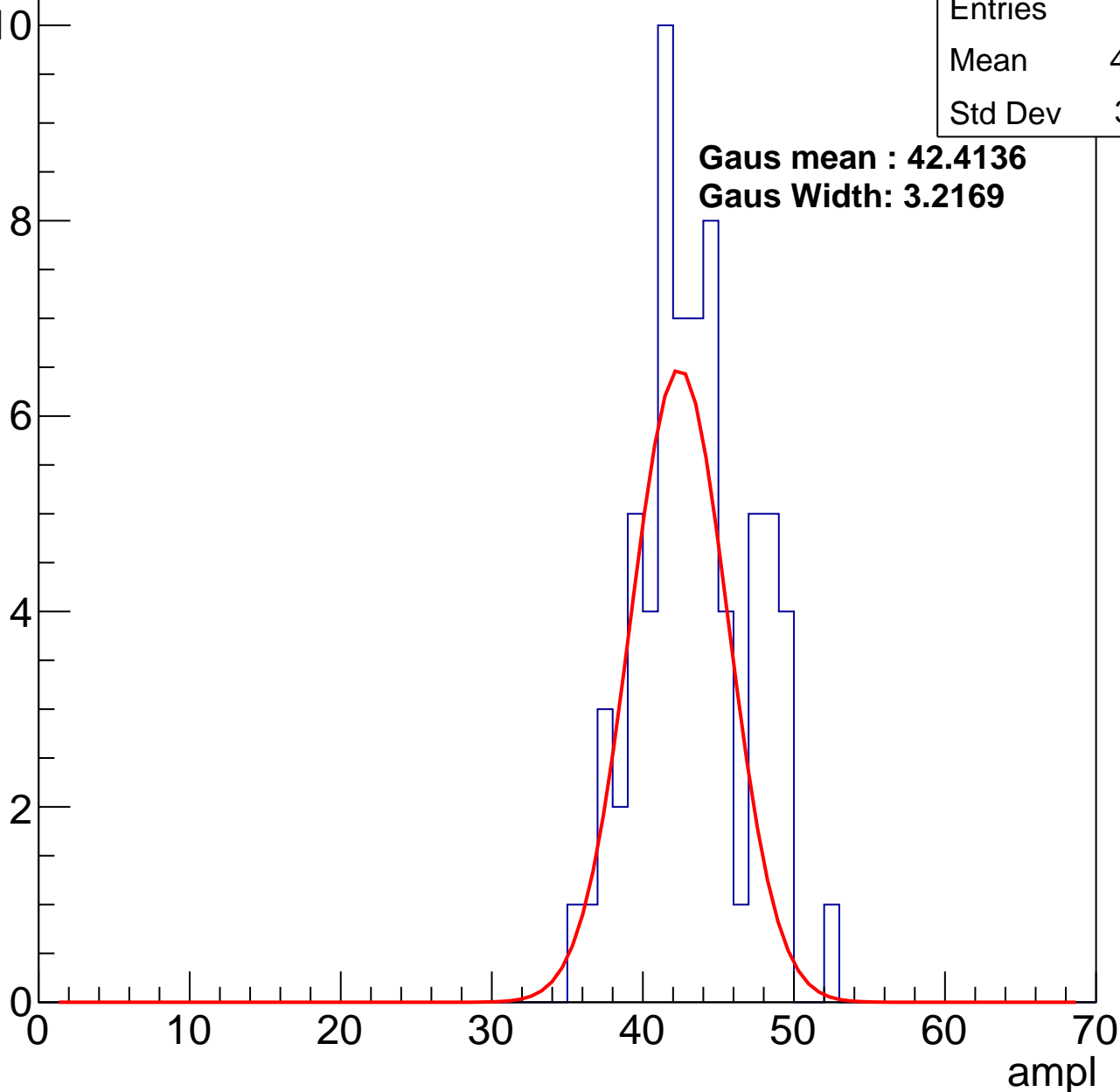
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	42.93
Std Dev	3.631

**Gaus mean : 42.4136**

**Gaus Width: 3.2169**

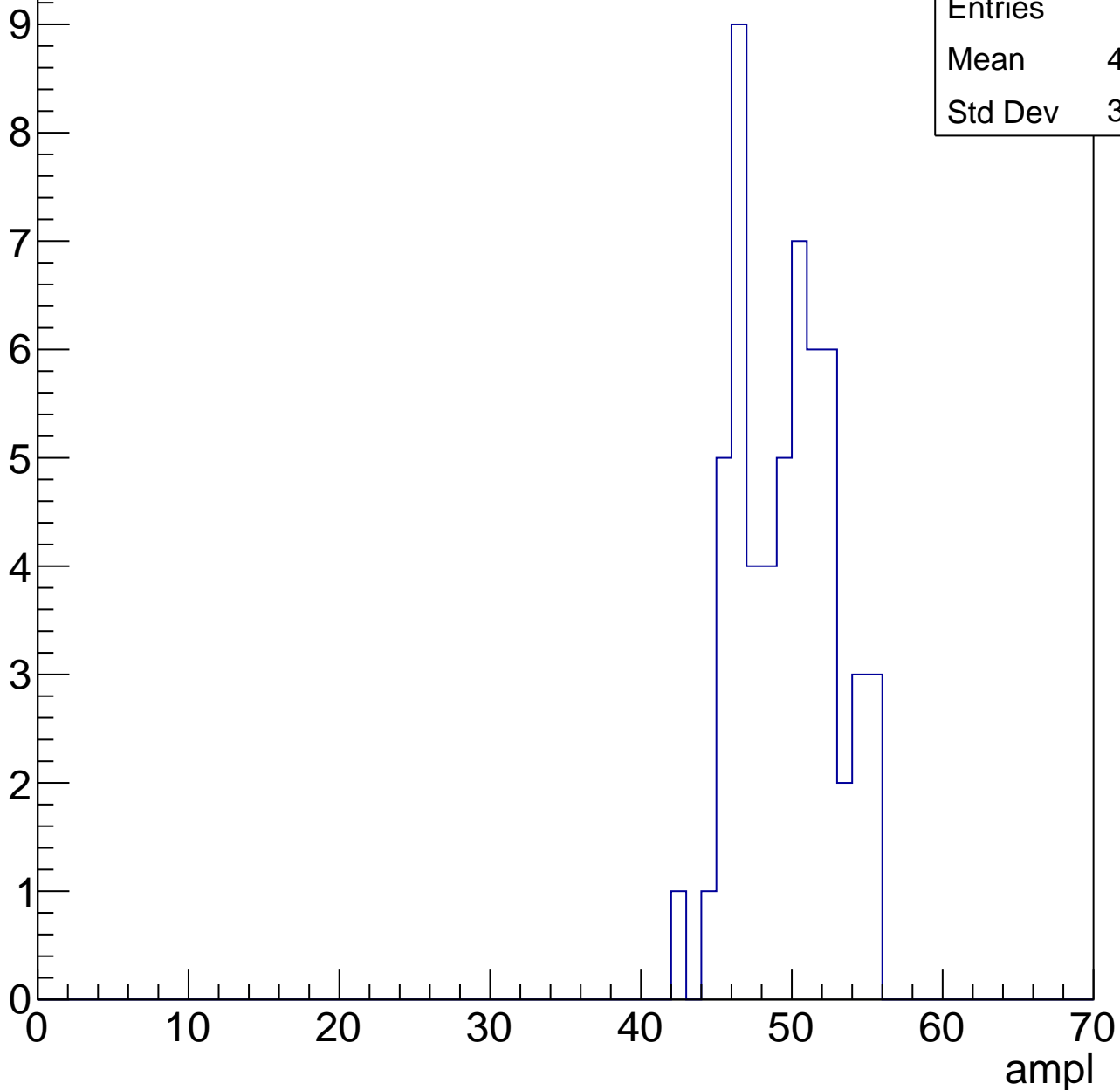


# B1L003S, U6-ch110, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	49.12
Std Dev	3.146

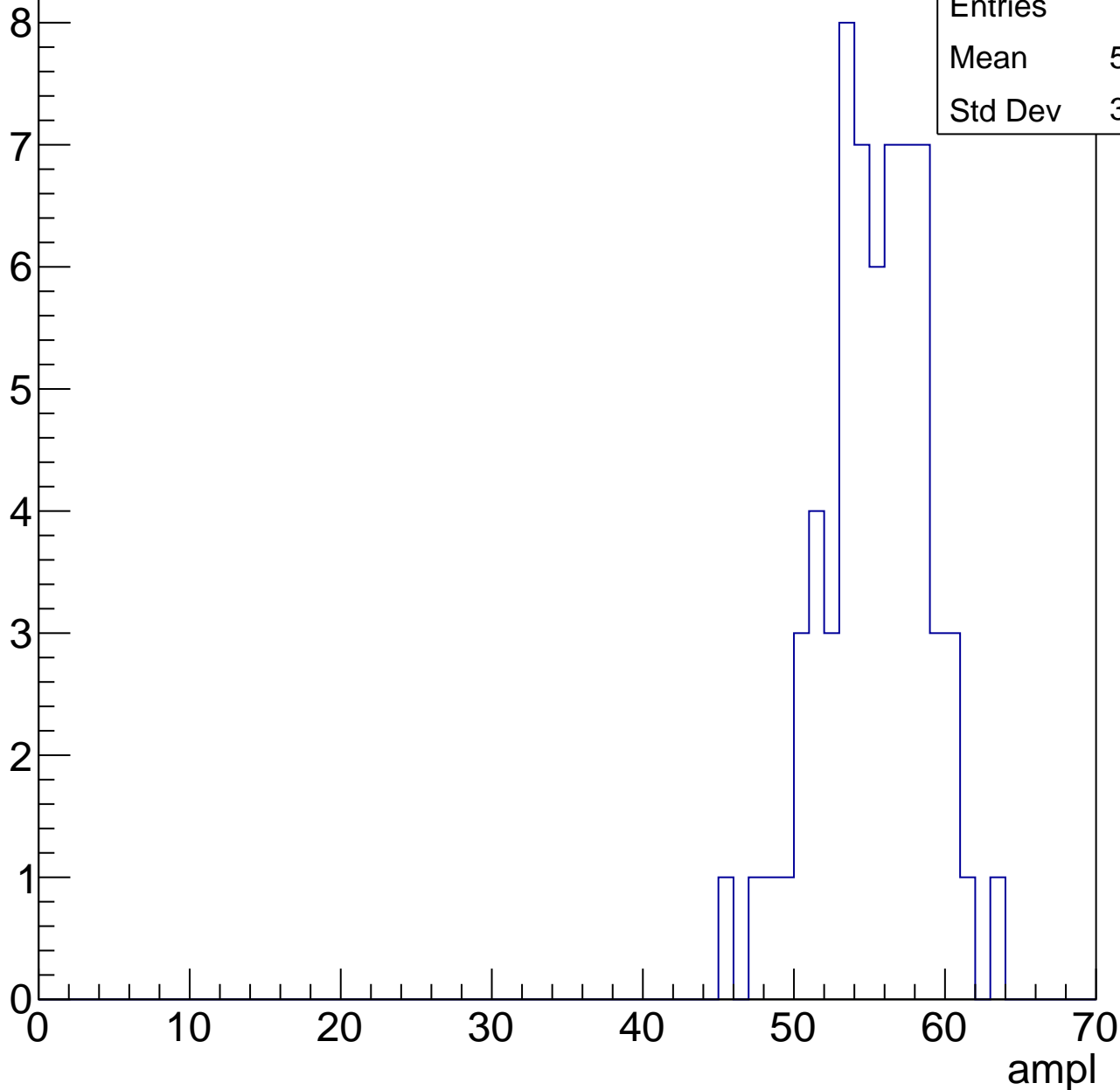


# B1L003S, U6-ch110, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	54.83
Std Dev	3.476

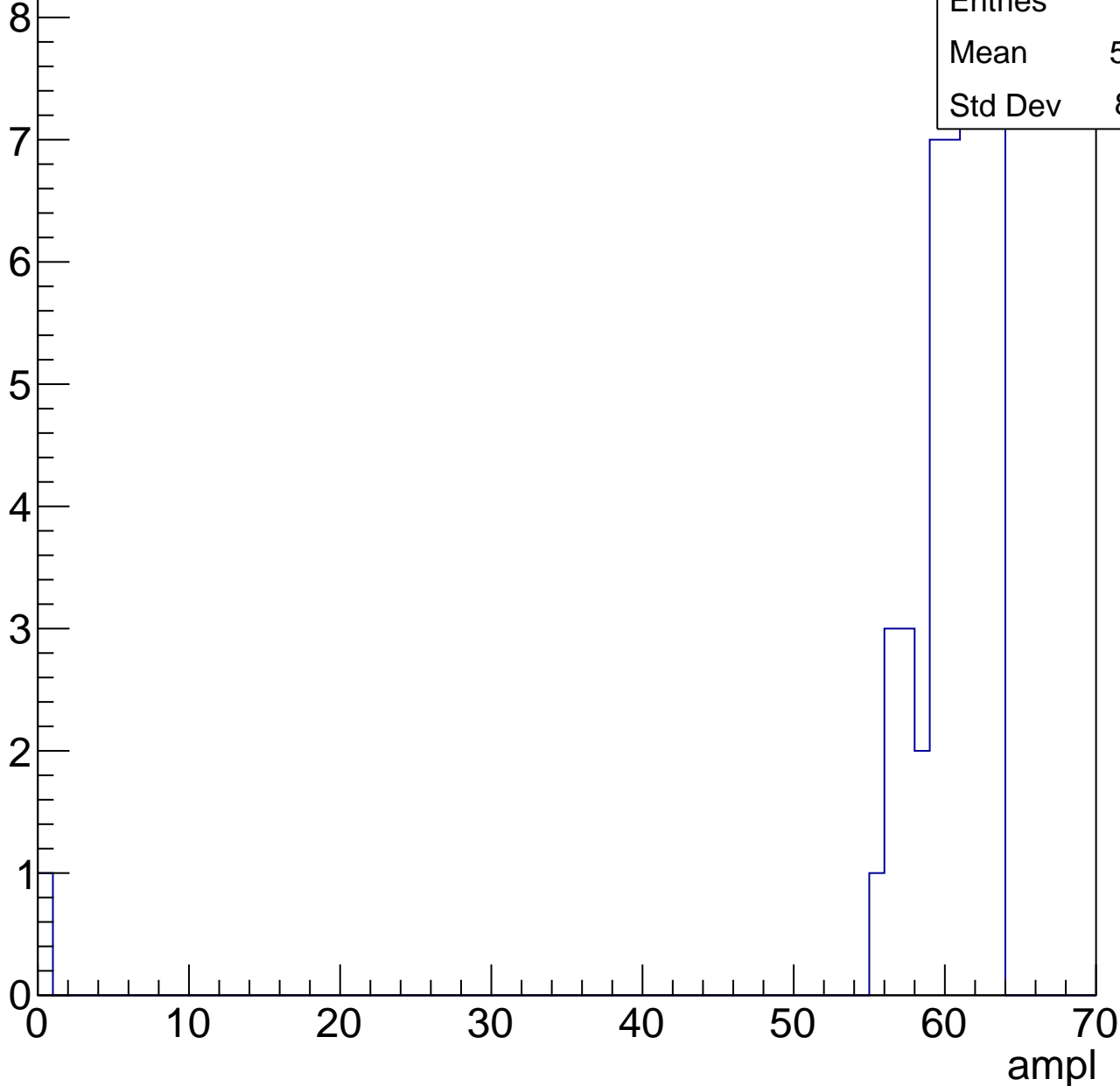


# B1L003S, U6-ch110, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	48
Mean	58.98
Std Dev	8.871



# B1L003S, U6-ch110, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

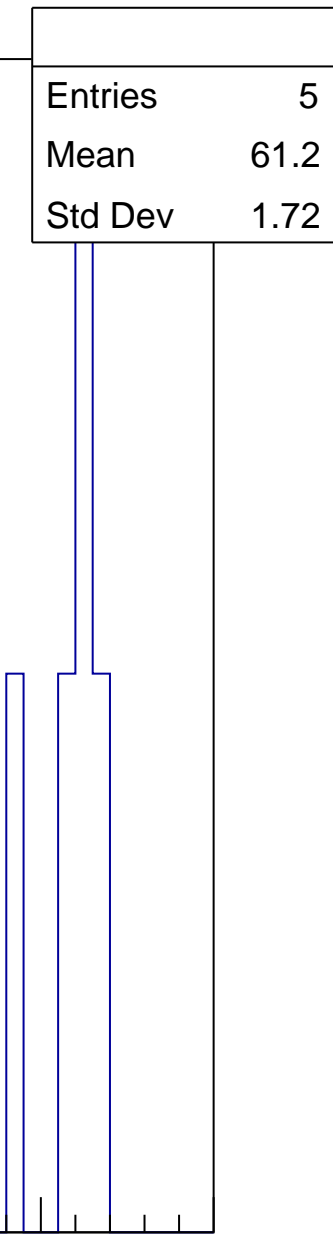
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	61.2
Std Dev	1.72

0 10 20 30 40 50 60 70

ampl





# B1L003S, U6-ch110, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

0

Mean

0

Std Dev

0

# B1L003S, U6-ch111, adc0

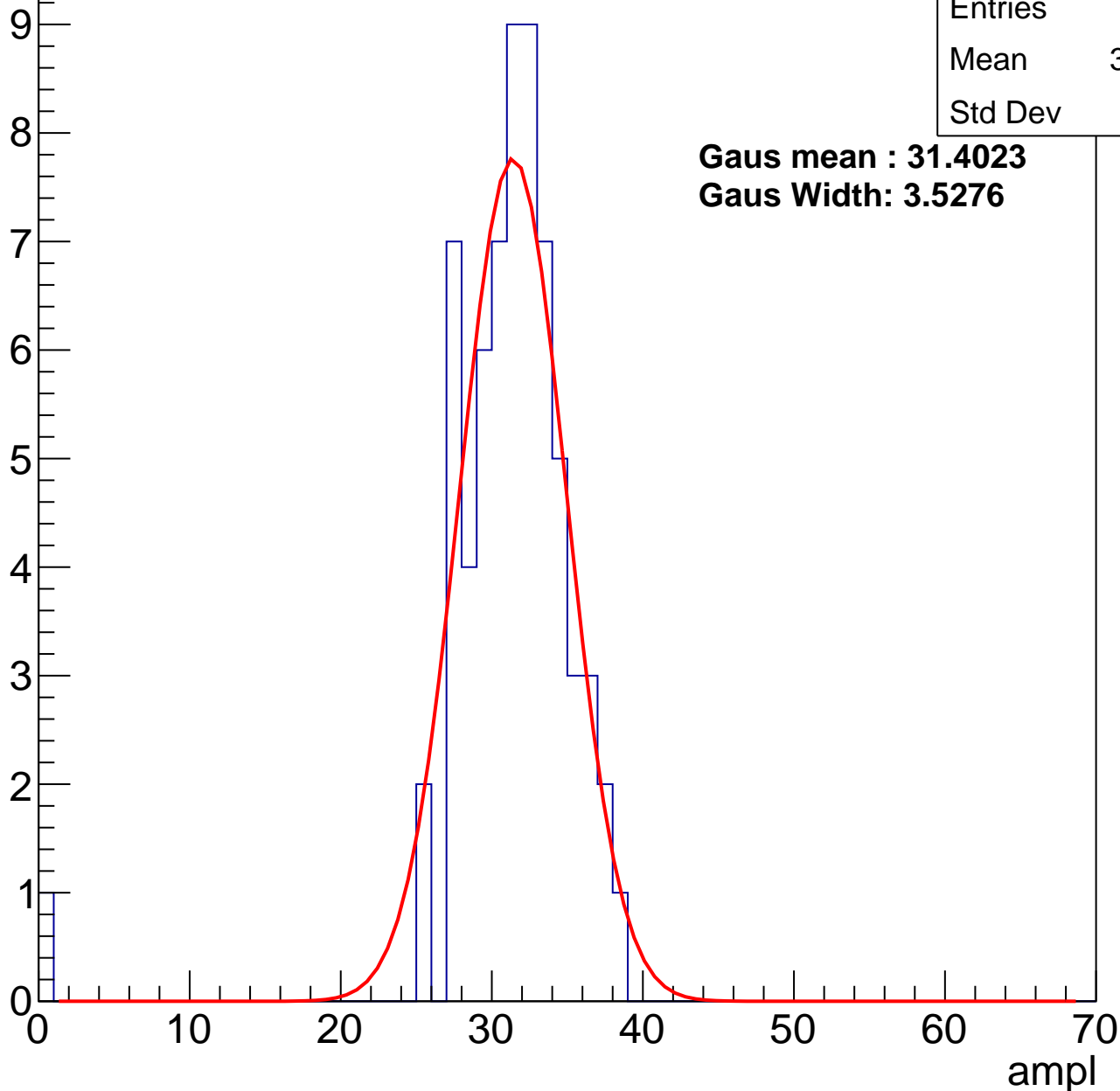
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	30.73
Std Dev	4.82

**Gaus mean : 31.4023**

**Gaus Width: 3.5276**



# B1L003S, U6-ch111, adc1

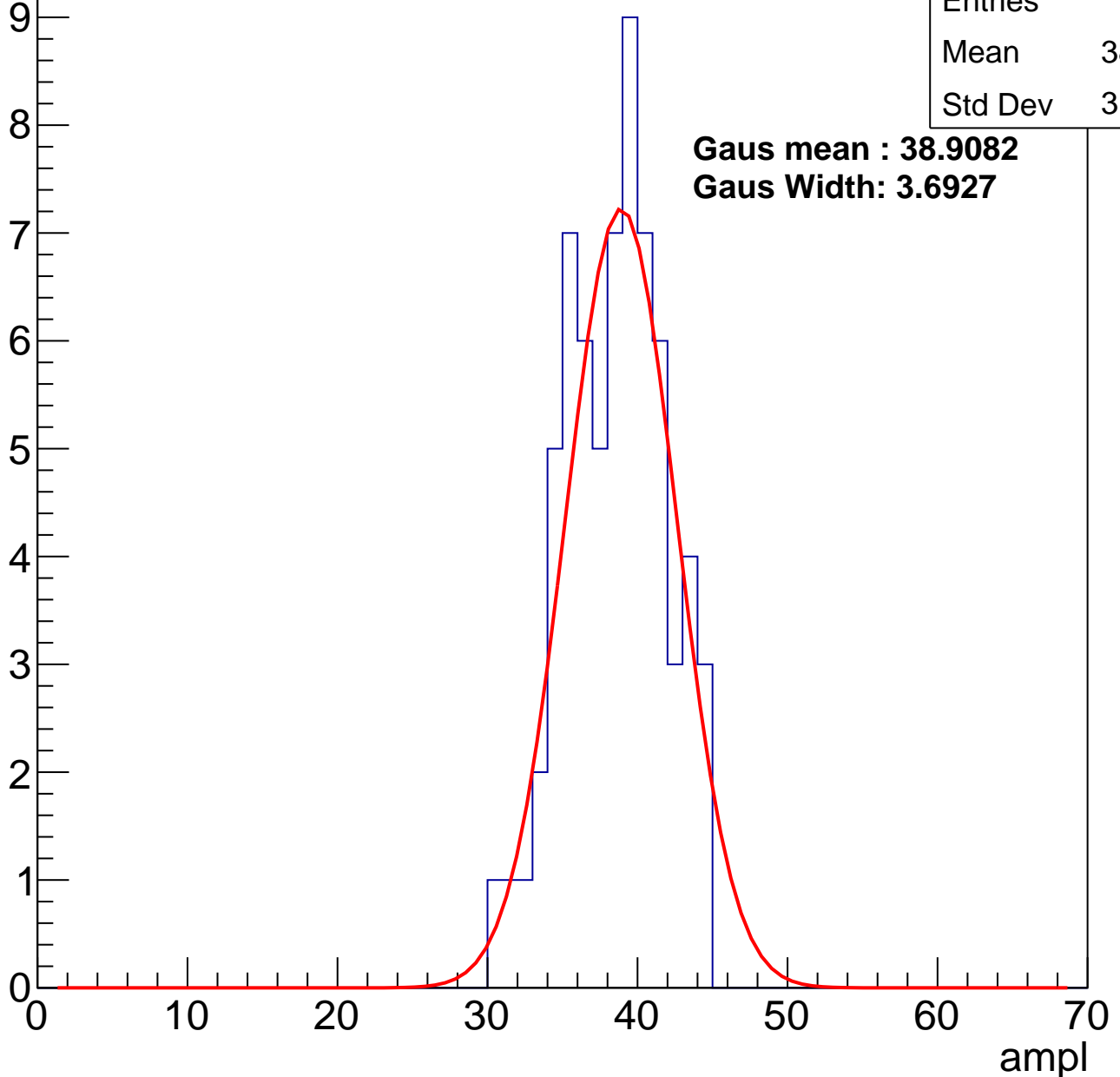
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	38.03
Std Dev	3.273

**Gaus mean : 38.9082**

**Gaus Width: 3.6927**



# B1L003S, U6-ch111, adc2

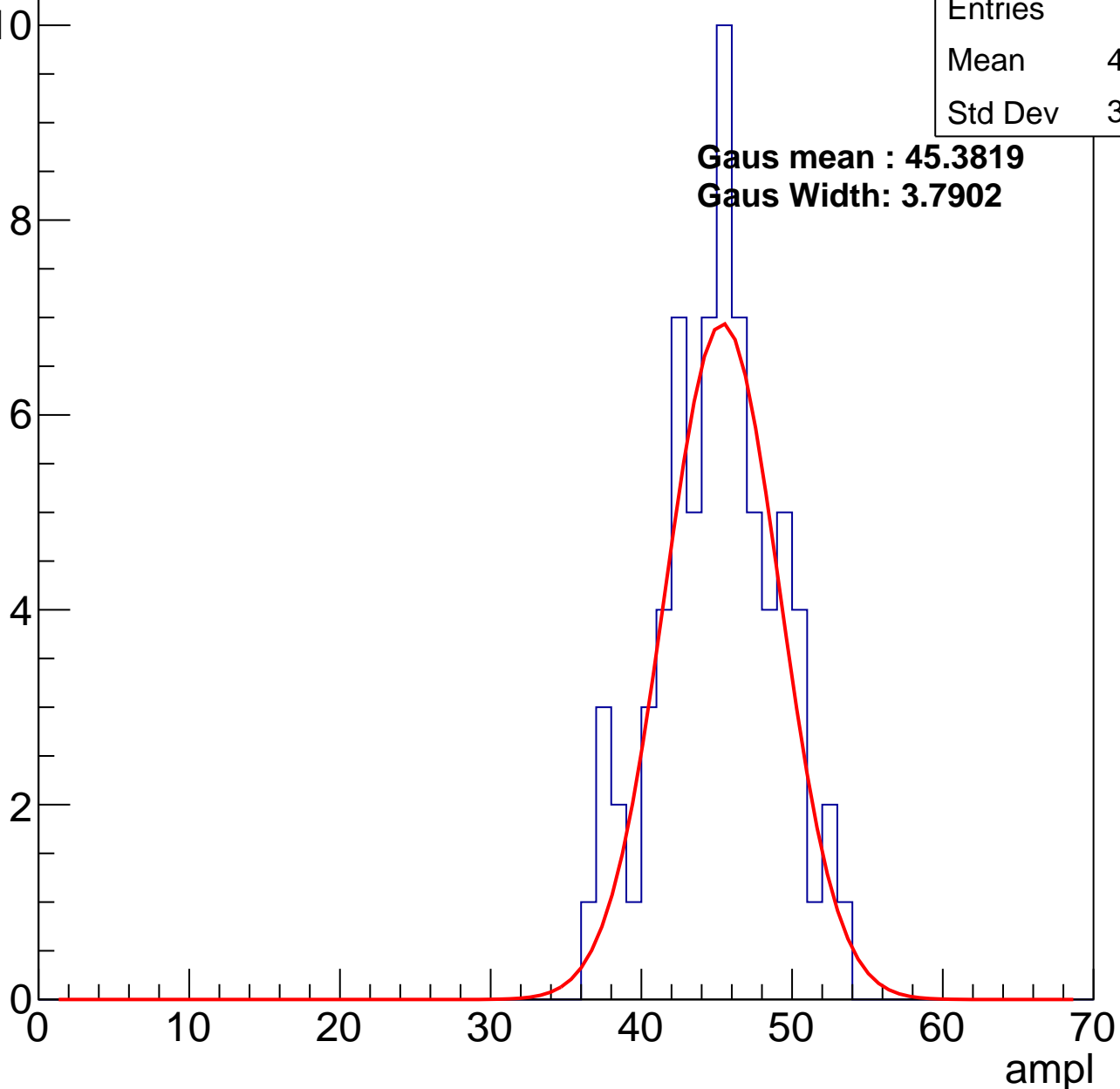
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	72
Mean	44.65
Std Dev	3.852

**Gaus mean : 45.3819**

**Gaus Width: 3.7902**

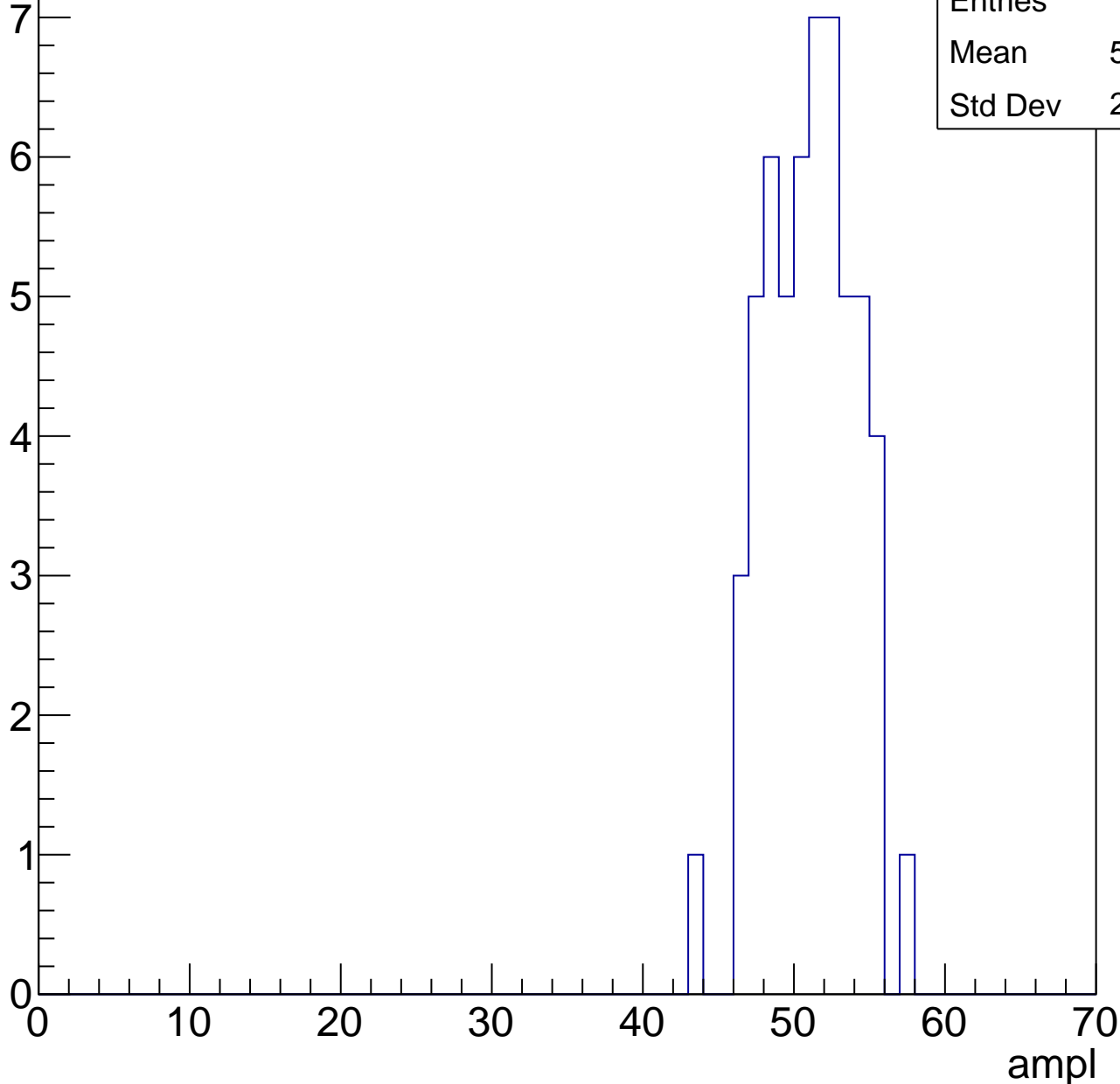


# B1L003S, U6-ch111, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

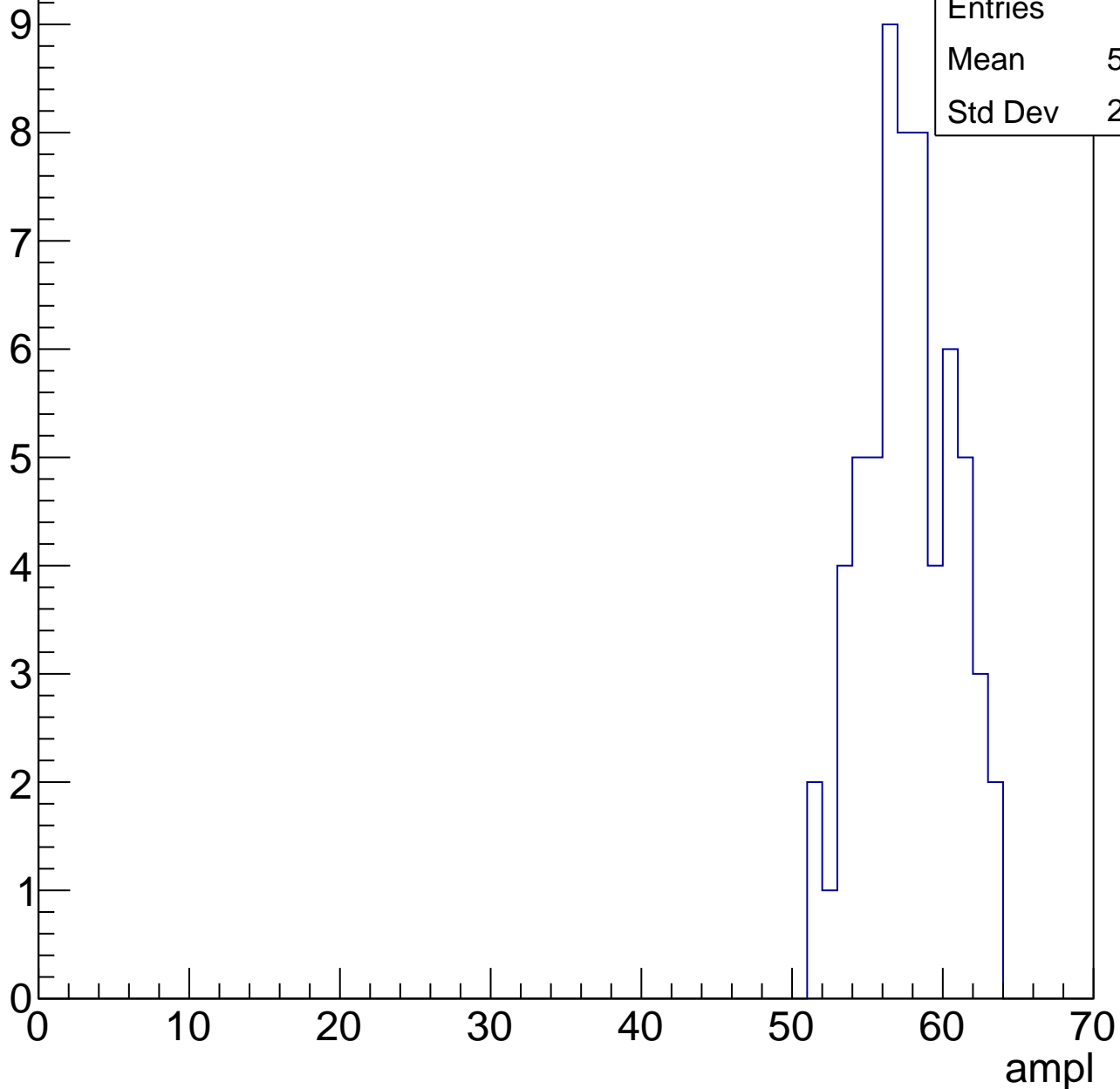
Entries	55
Mean	50.58
Std Dev	2.896



# B1L003S, U6-ch111, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



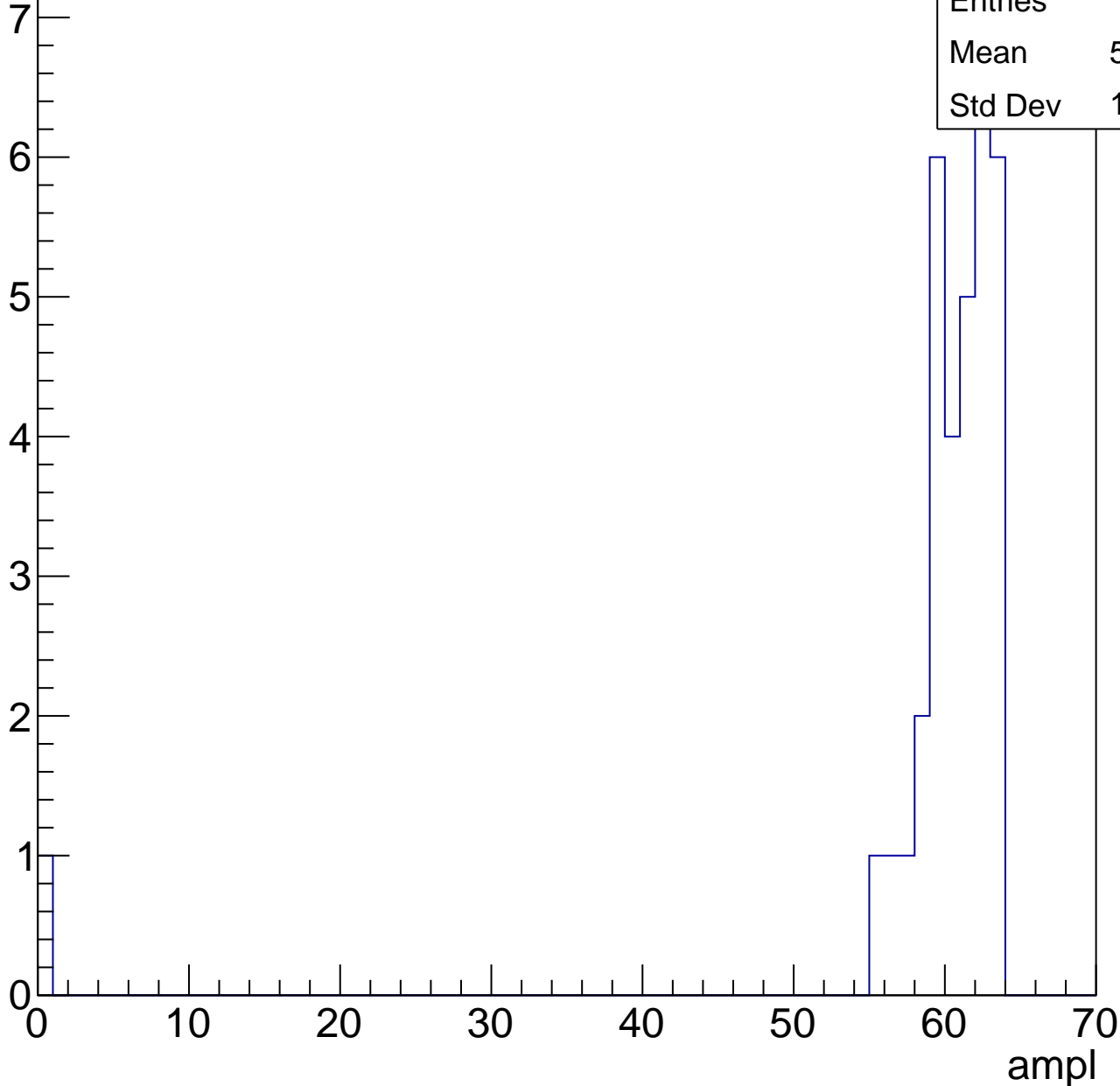
Entries	62
Mean	57.23
Std Dev	2.943

# B1L003S, U6-ch111, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	34
Mean	58.68
Std Dev	10.42



# B1L003S, U6-ch111, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	63
Std Dev	0

0 10 20 30 40 50 60 70

ampl



# B1L003S, U6-ch111, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch112, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	64
Mean	29.05
Std Dev	4.961

**Gaus mean : 30.0701**

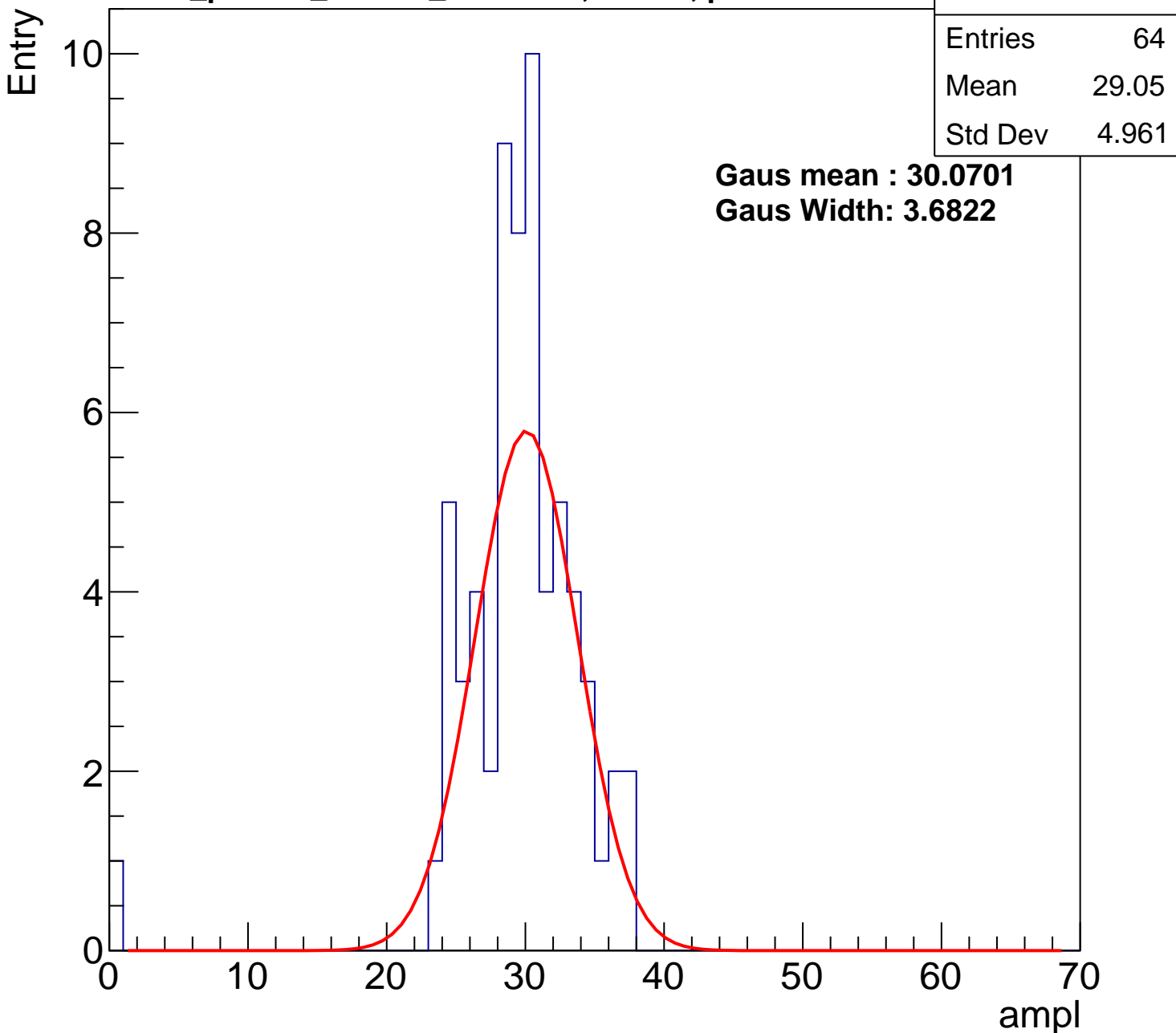
**Gaus Width: 3.6822**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U6-ch112, adc1

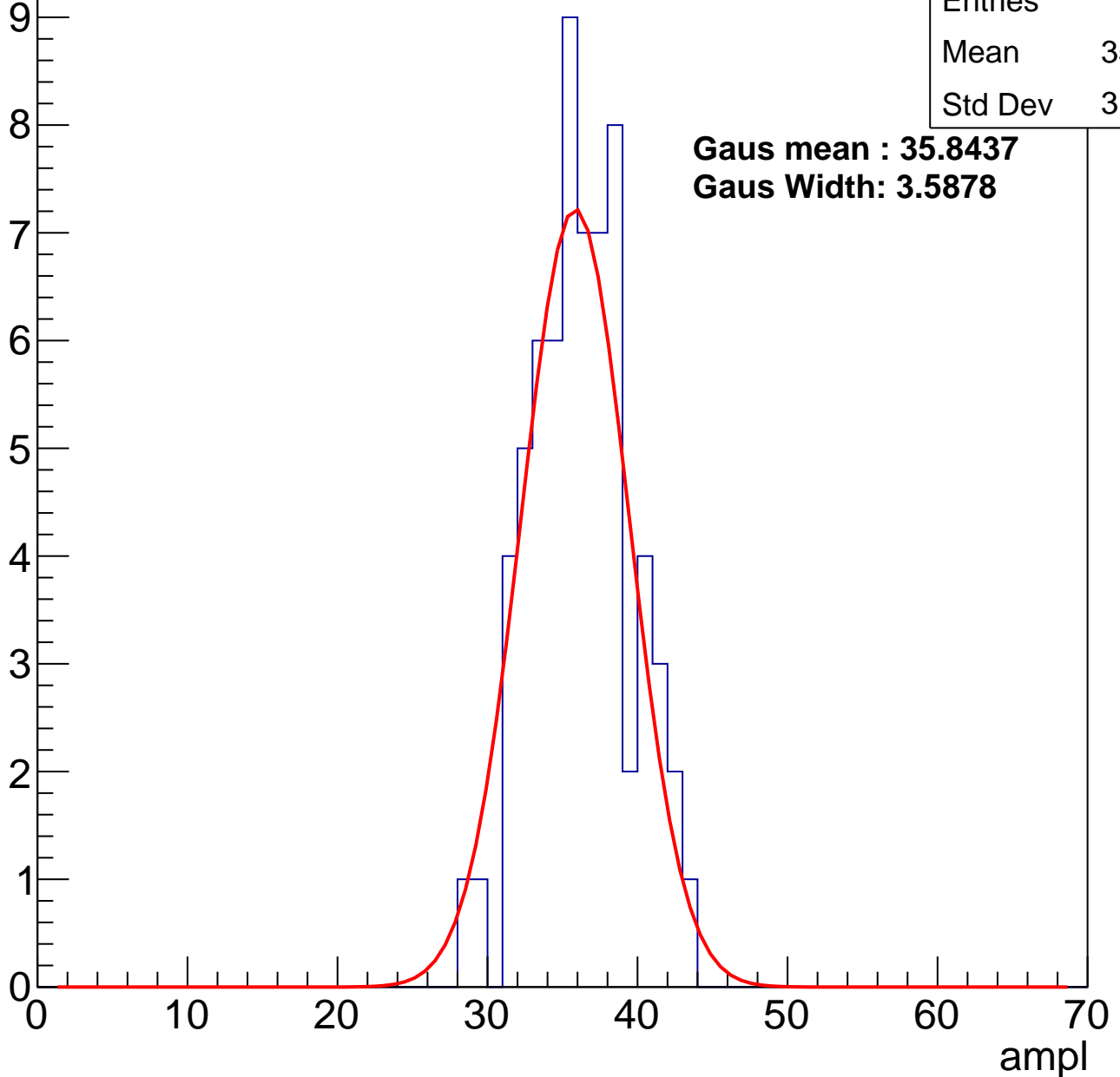
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	35.77
Std Dev	3.242

**Gaus mean : 35.8437**

**Gaus Width: 3.5878**



# B1L003S, U6-ch112, adc2

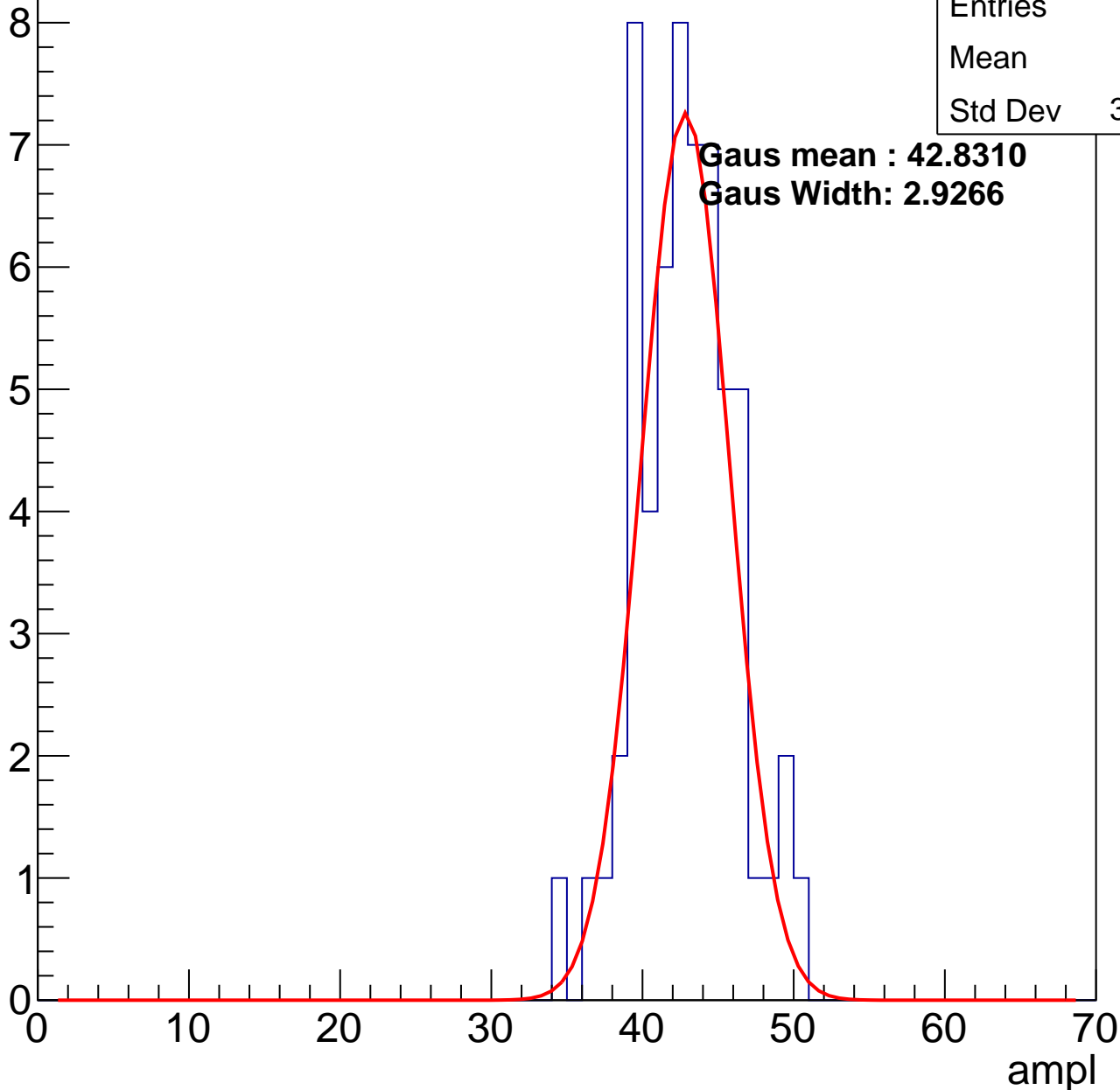
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	42.4
Std Dev	3.226

**Gaus mean : 42.8310**

**Gaus Width: 2.9266**

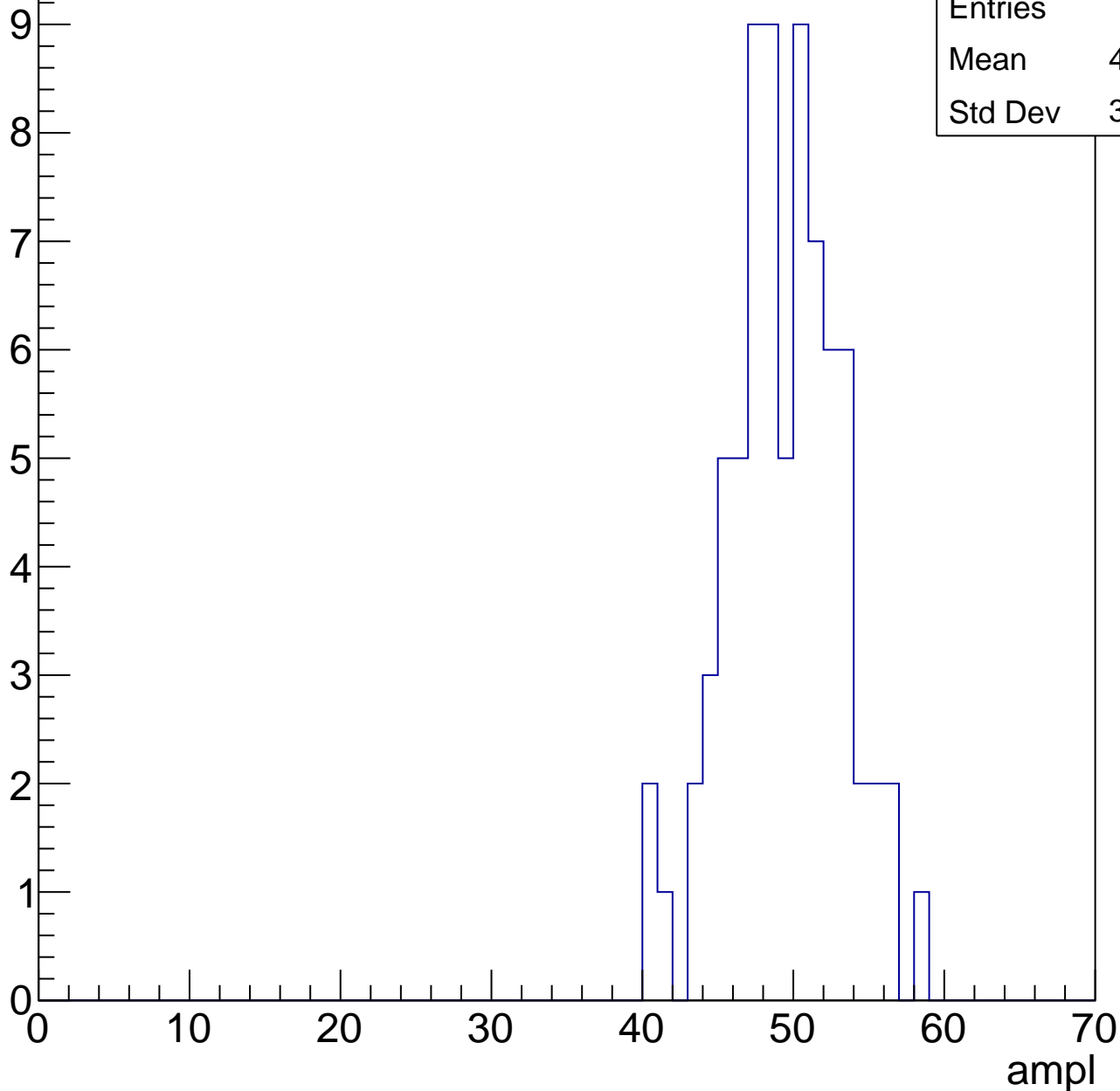


# B1L003S, U6-ch112, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

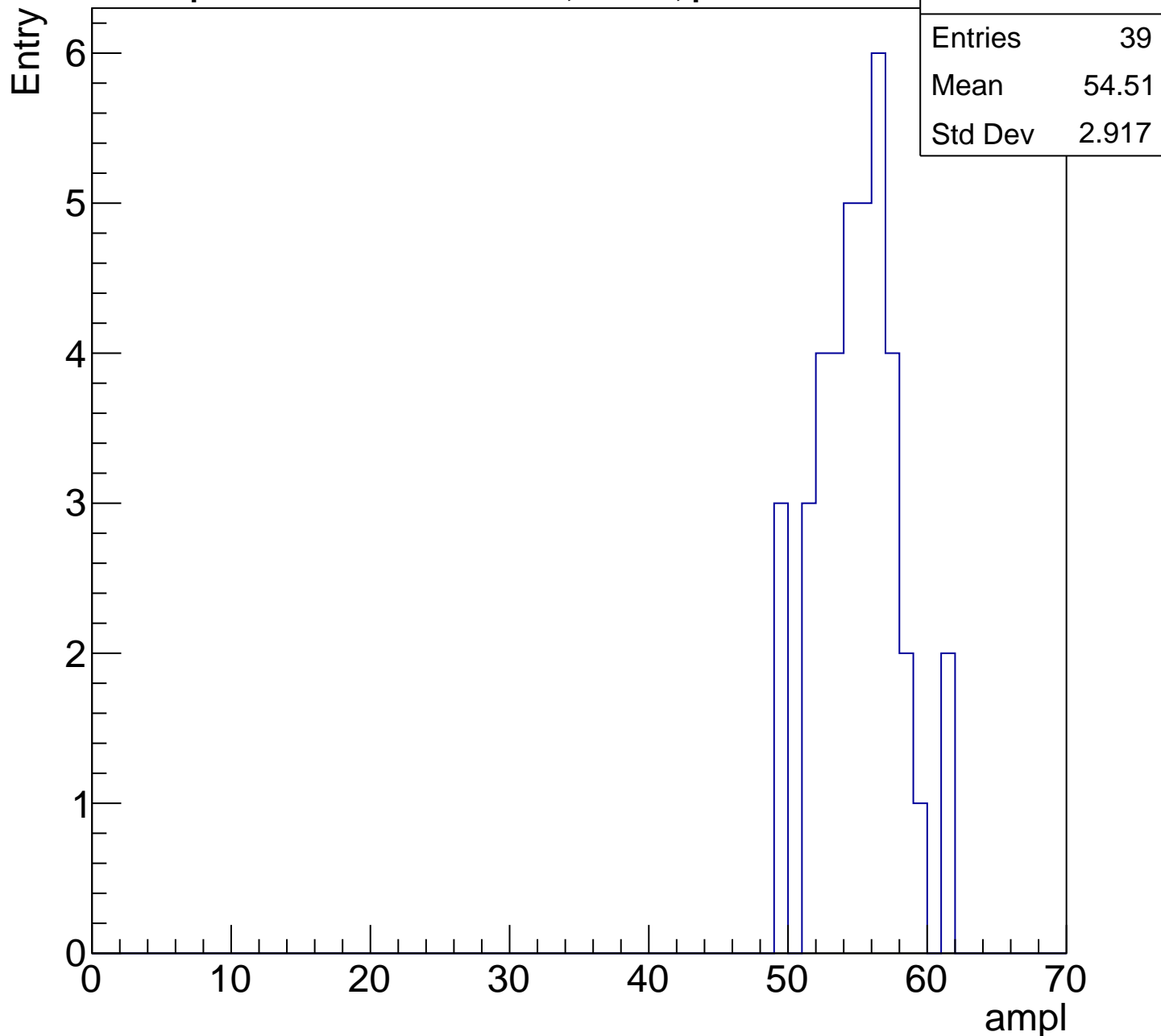
Entry

Entries	76
Mean	48.93
Std Dev	3.683



# B1L003S, U6-ch112, adc4

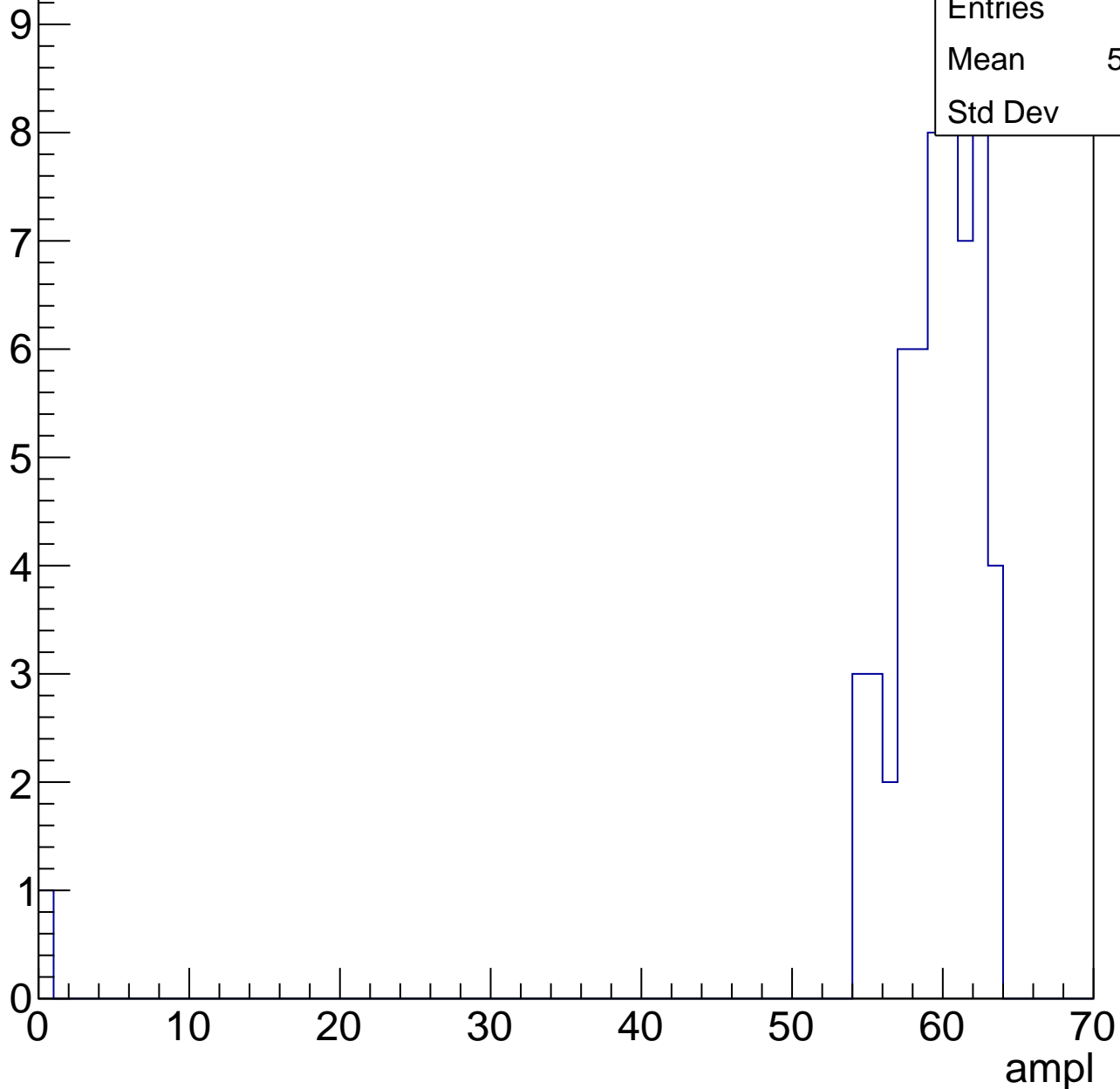
calib\_packv5\_042523\_0143.root, FC#13, port D2



# B1L003S, U6-ch112, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

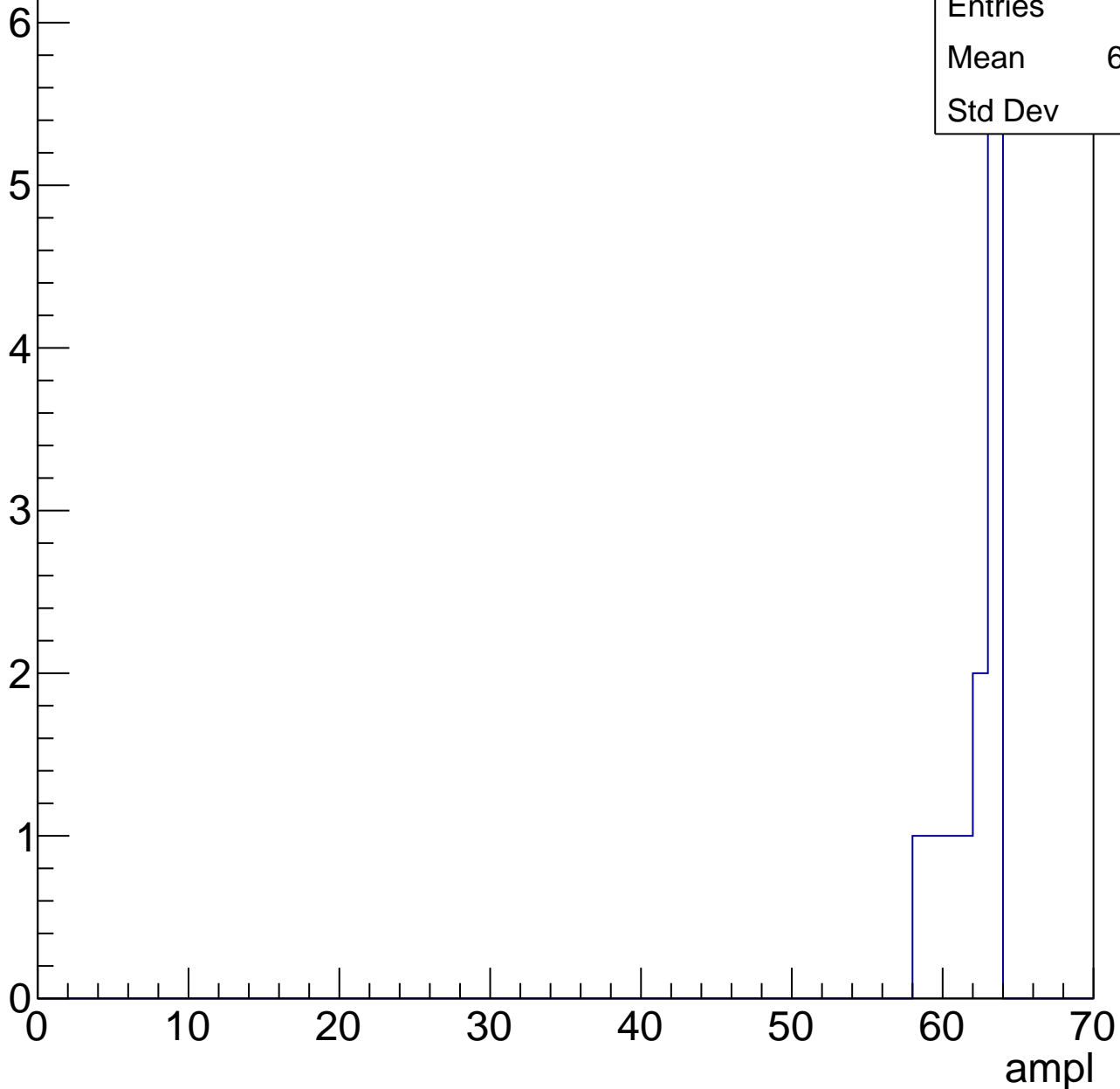


# B1L003S, U6-ch112, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	12
Mean	61.67
Std Dev	1.7





# B1L003S, U6-ch112, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U6-ch113, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	53
Mean	30.98
Std Dev	2.737

**Gaus mean : 31.5111**

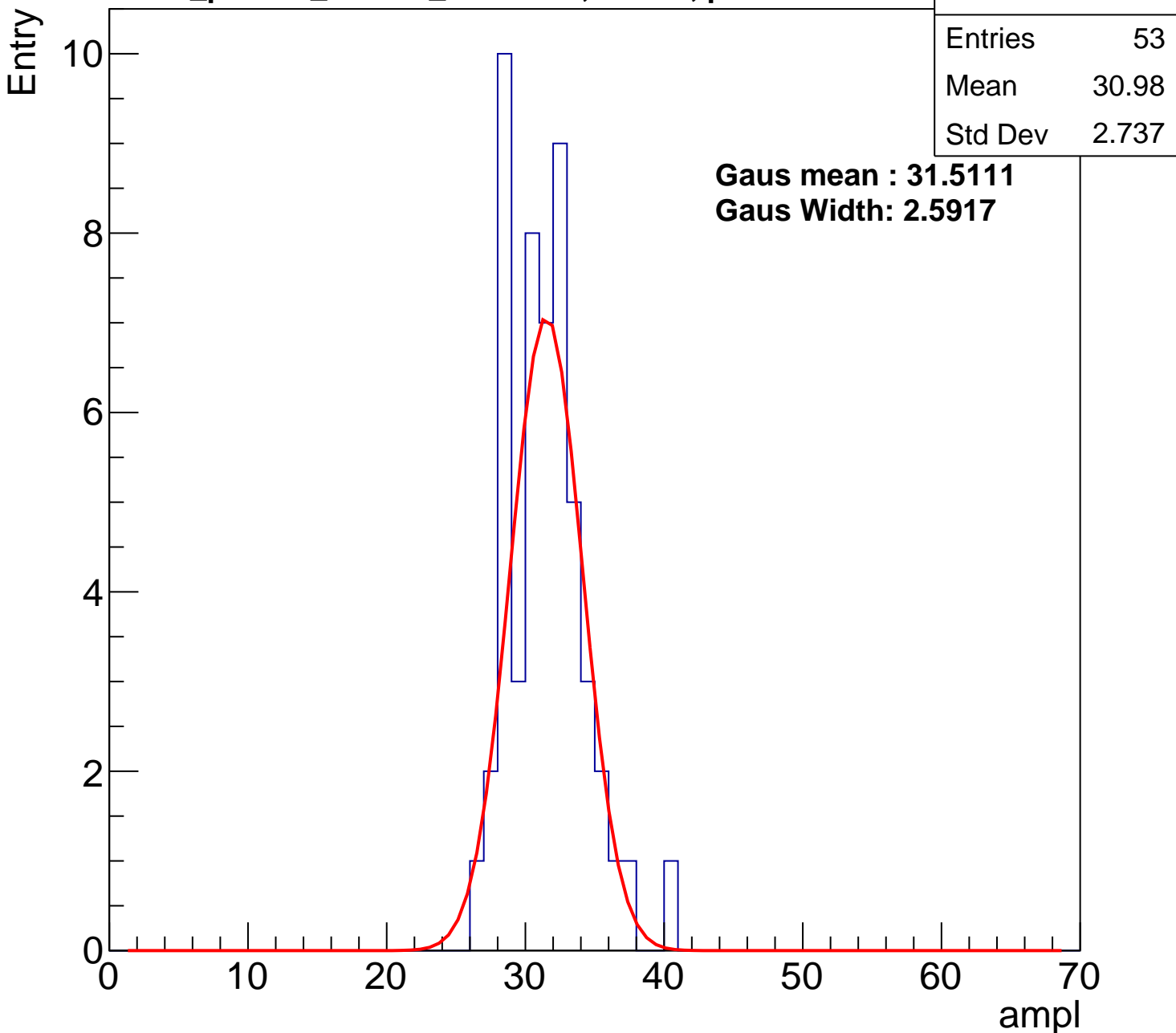
**Gaus Width: 2.5917**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U6-ch113, adc1

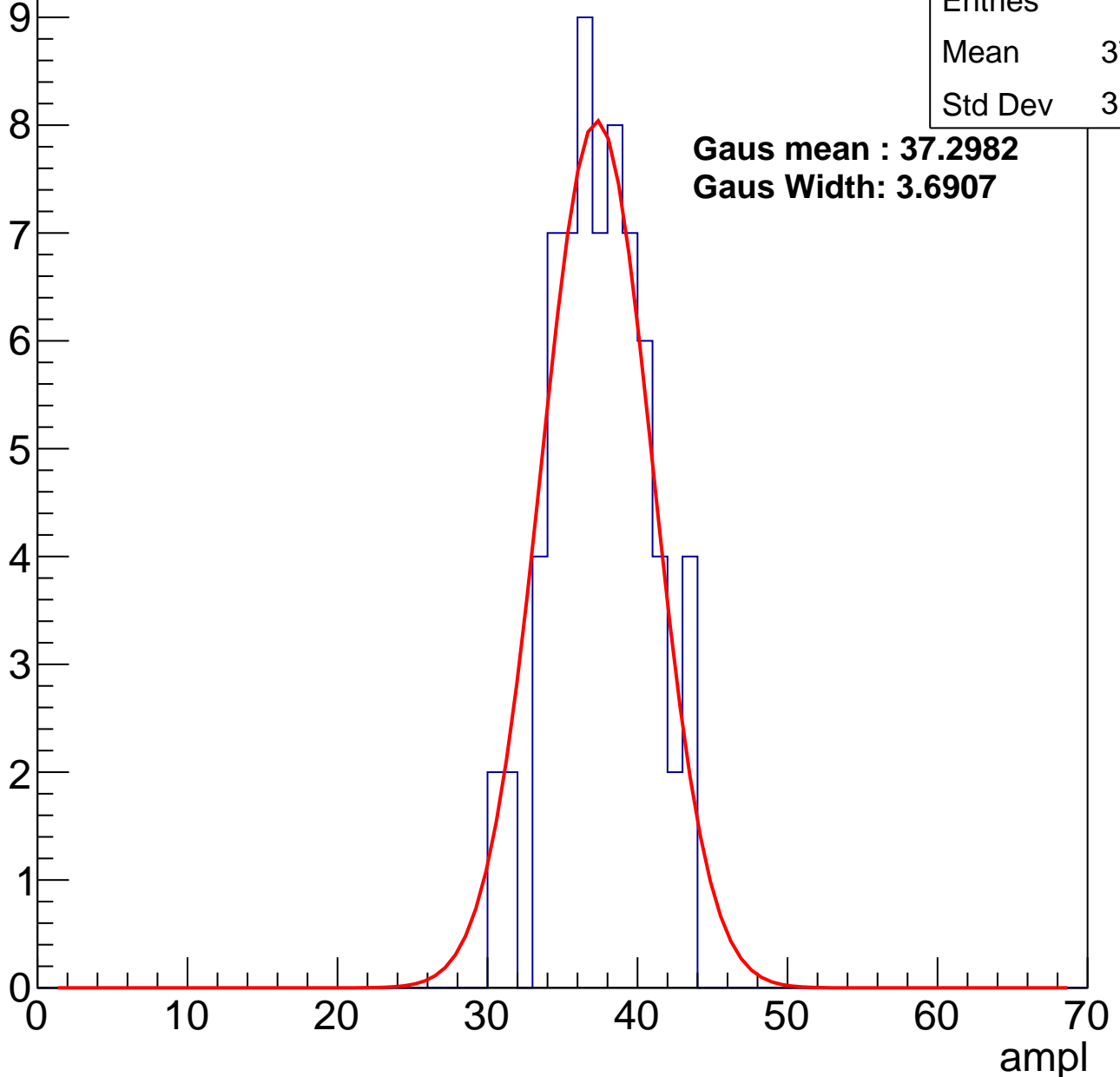
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	37.06
Std Dev	3.143

**Gaus mean : 37.2982**

**Gaus Width: 3.6907**



# B1L003S, U6-ch113, adc2

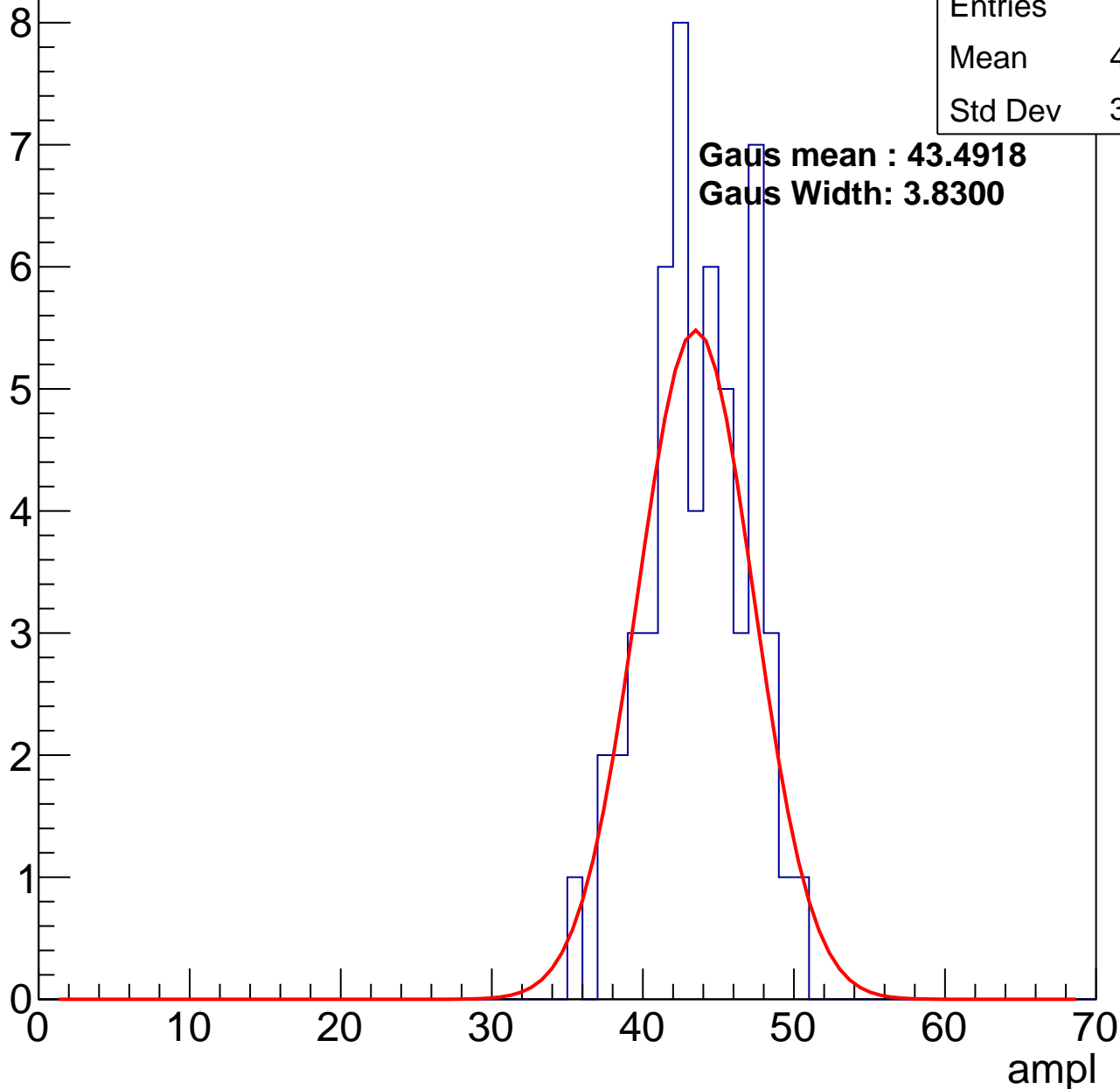
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	43.18
Std Dev	3.347

**Gaus mean : 43.4918**

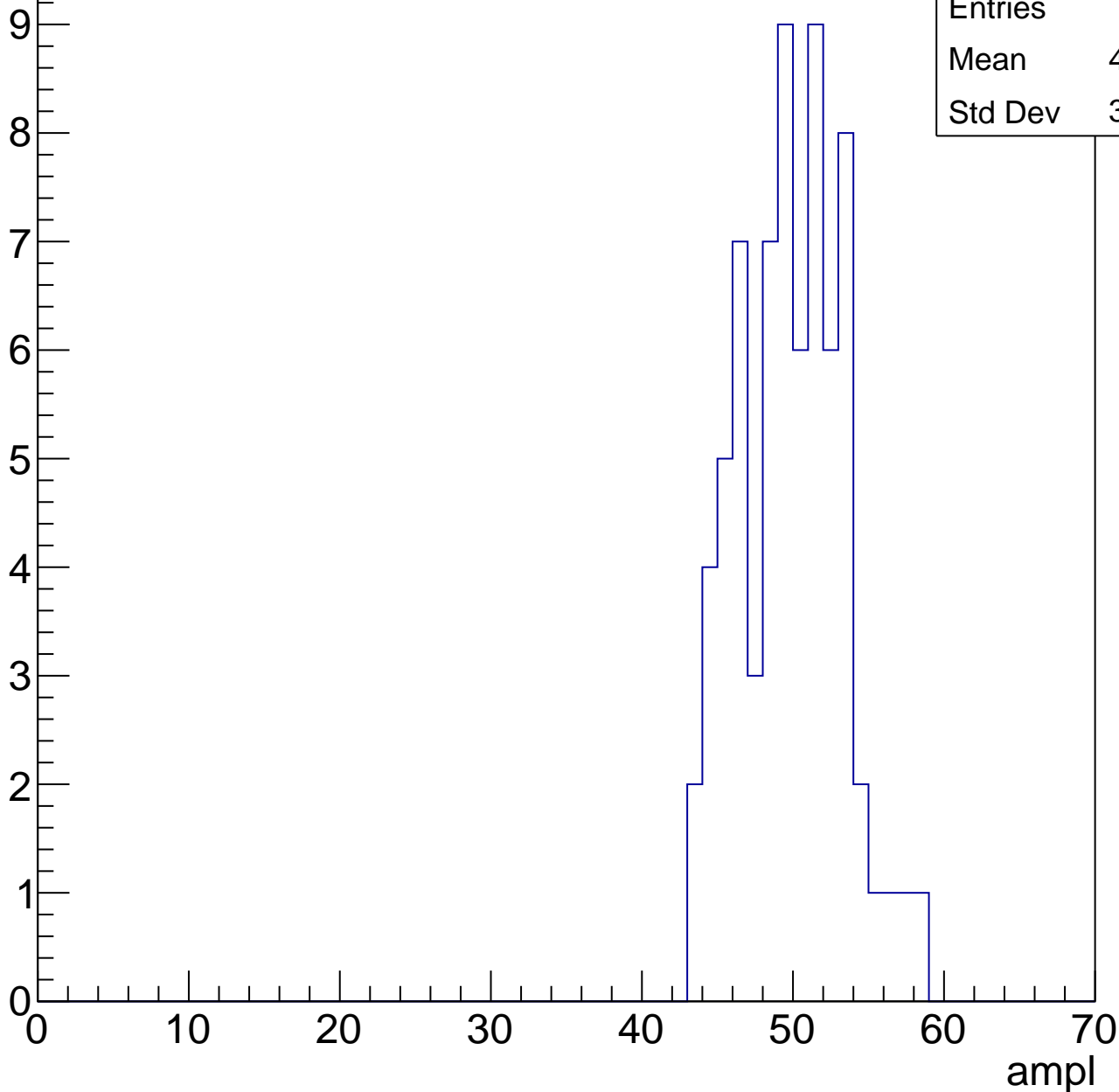
**Gaus Width: 3.8300**



# B1L003S, U6-ch113, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



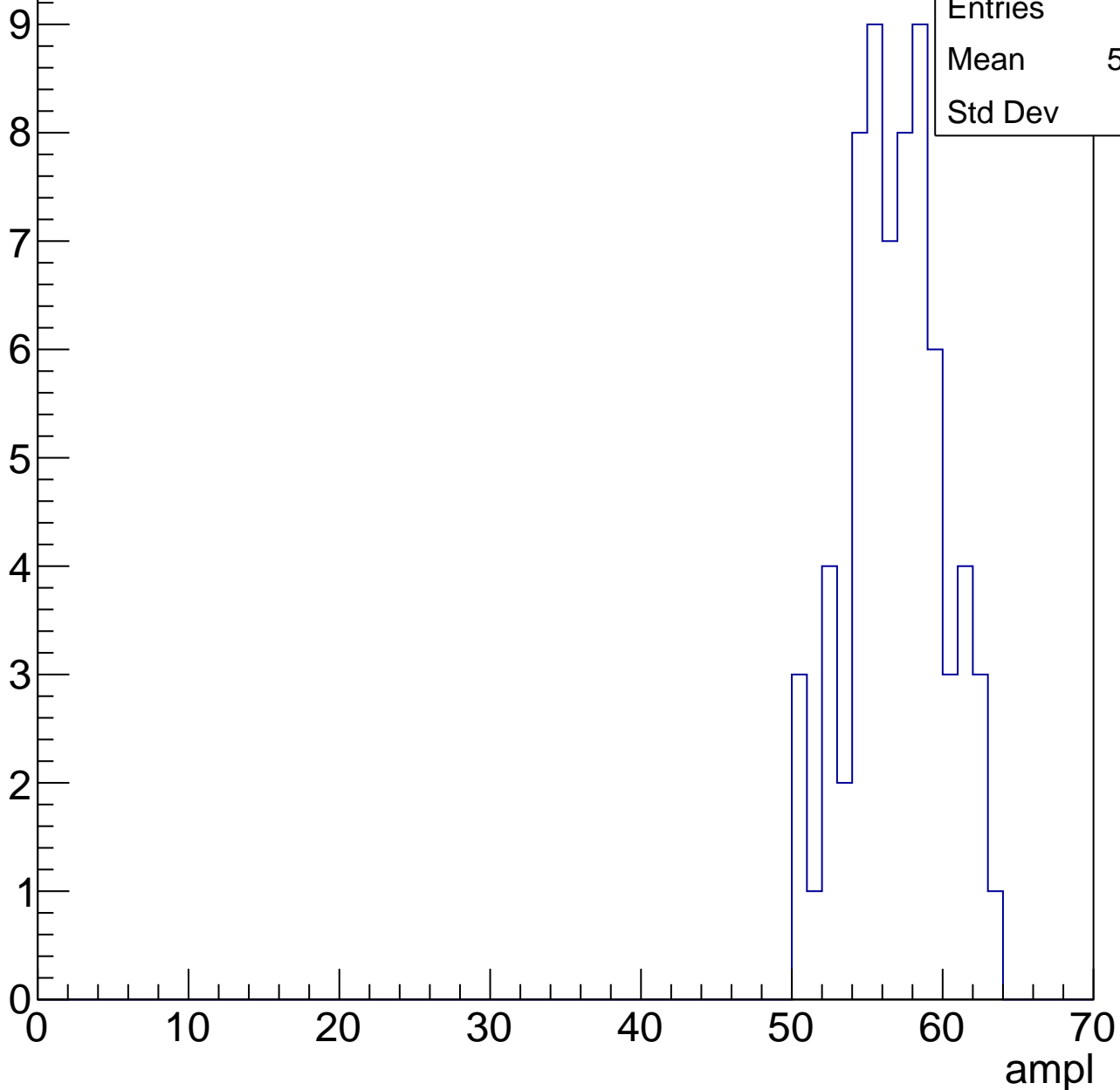
Entries	72
Mean	49.39
Std Dev	3.389

# B1L003S, U6-ch113, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	56.46
Std Dev	3.08

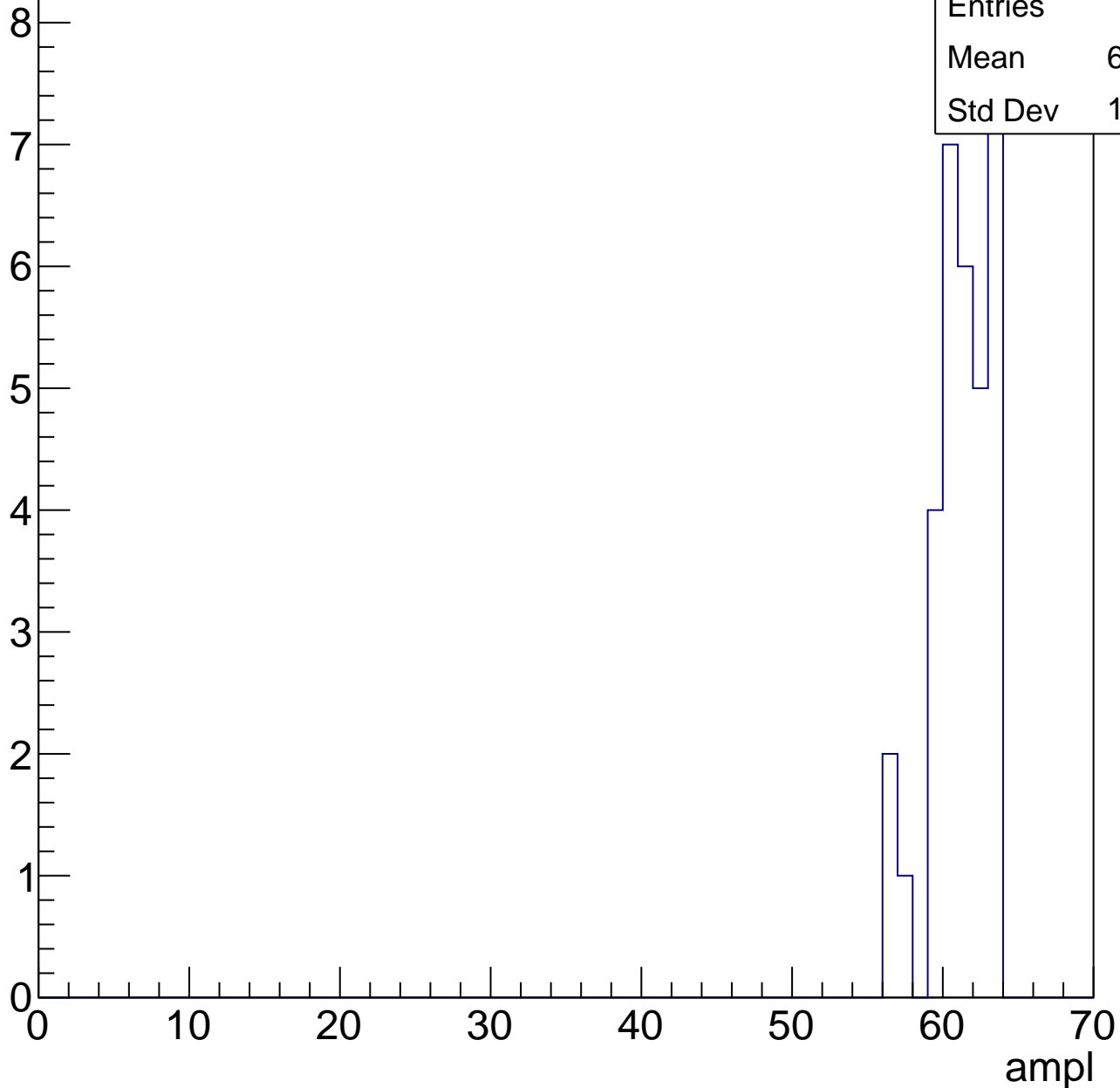


# B1L003S, U6-ch113, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

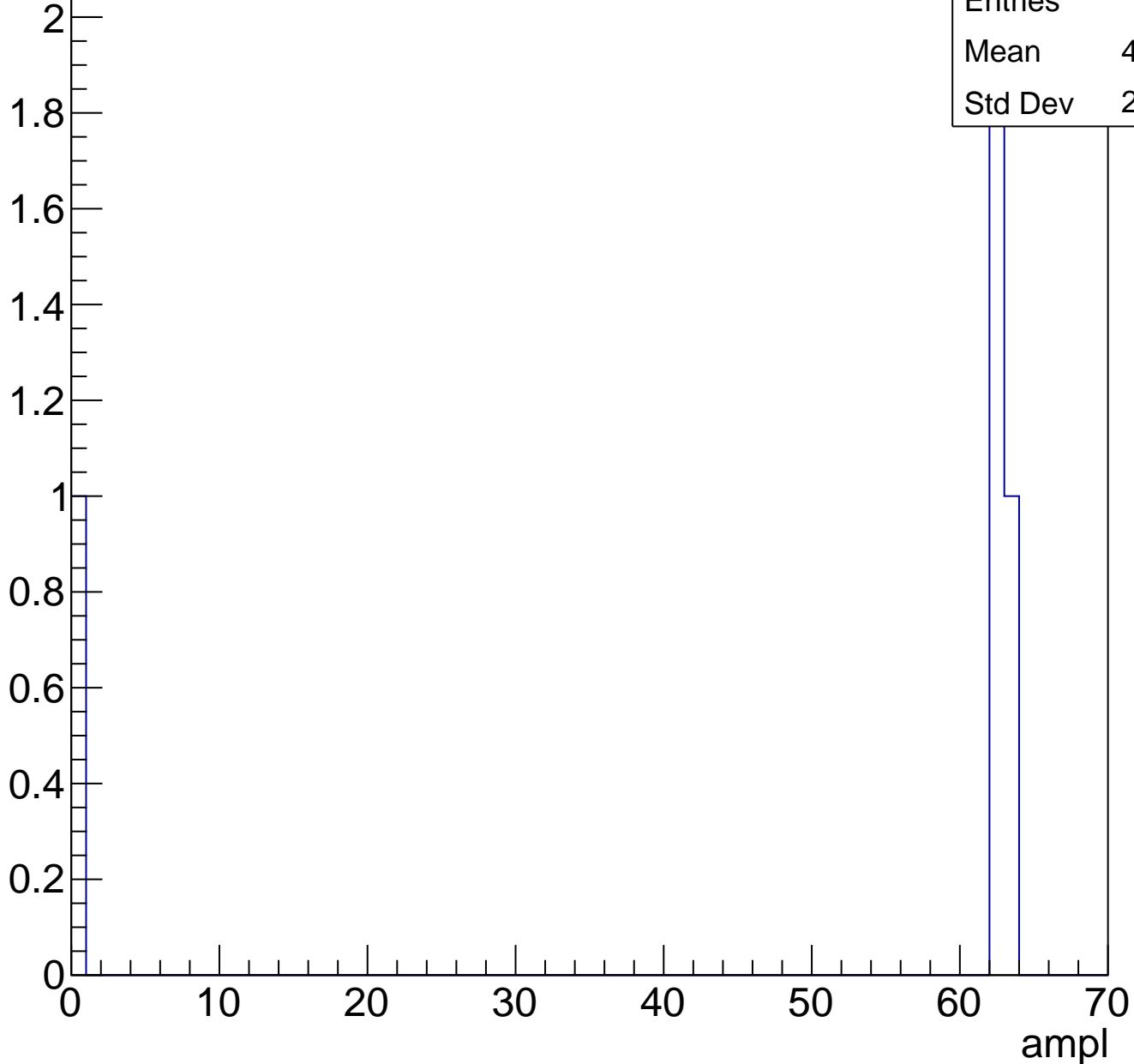
Entries	33
Mean	60.76
Std Dev	1.939



# B1L003S, U6-ch113, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

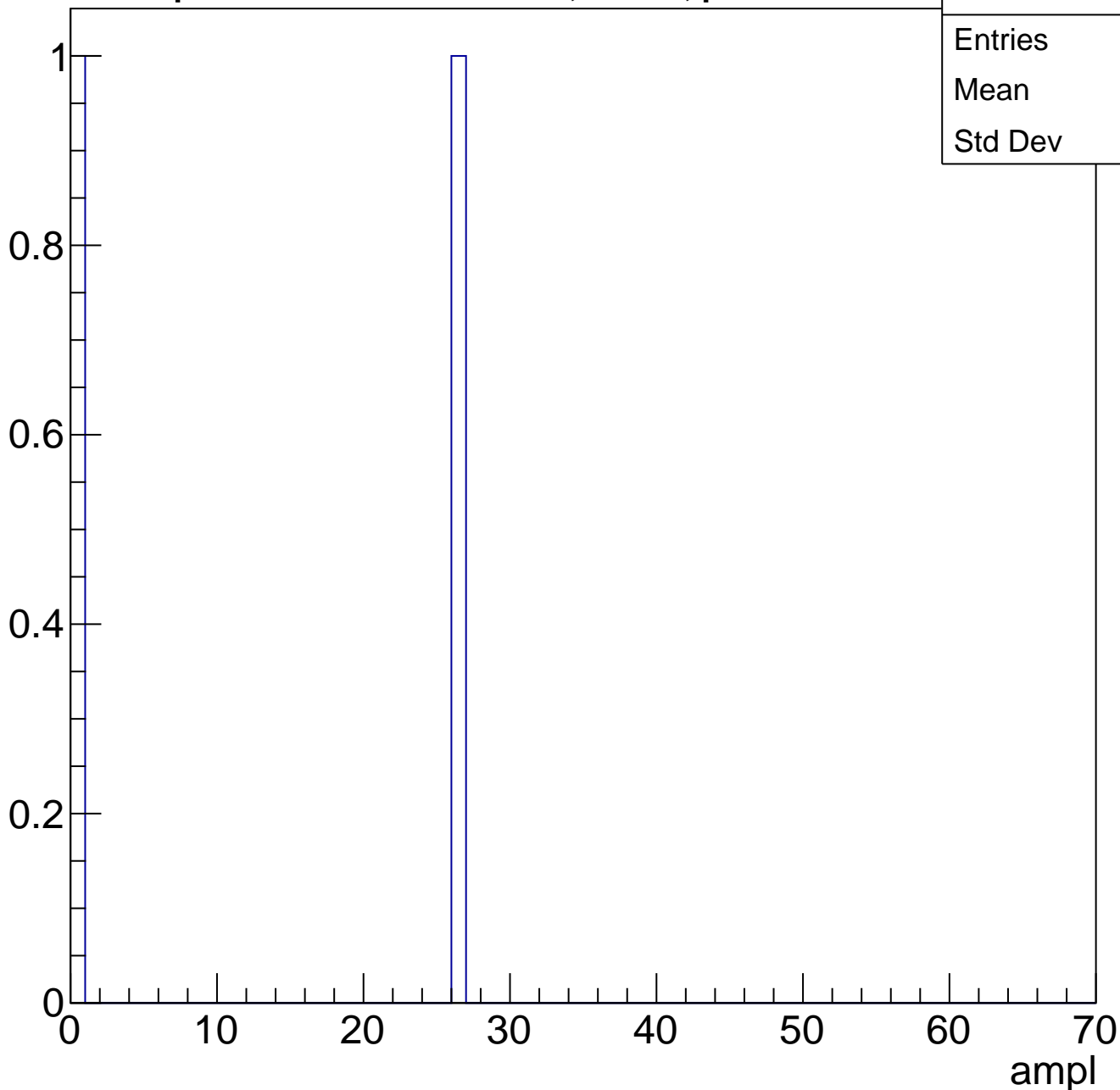




# B1L003S, U6-ch113, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch114, adc0

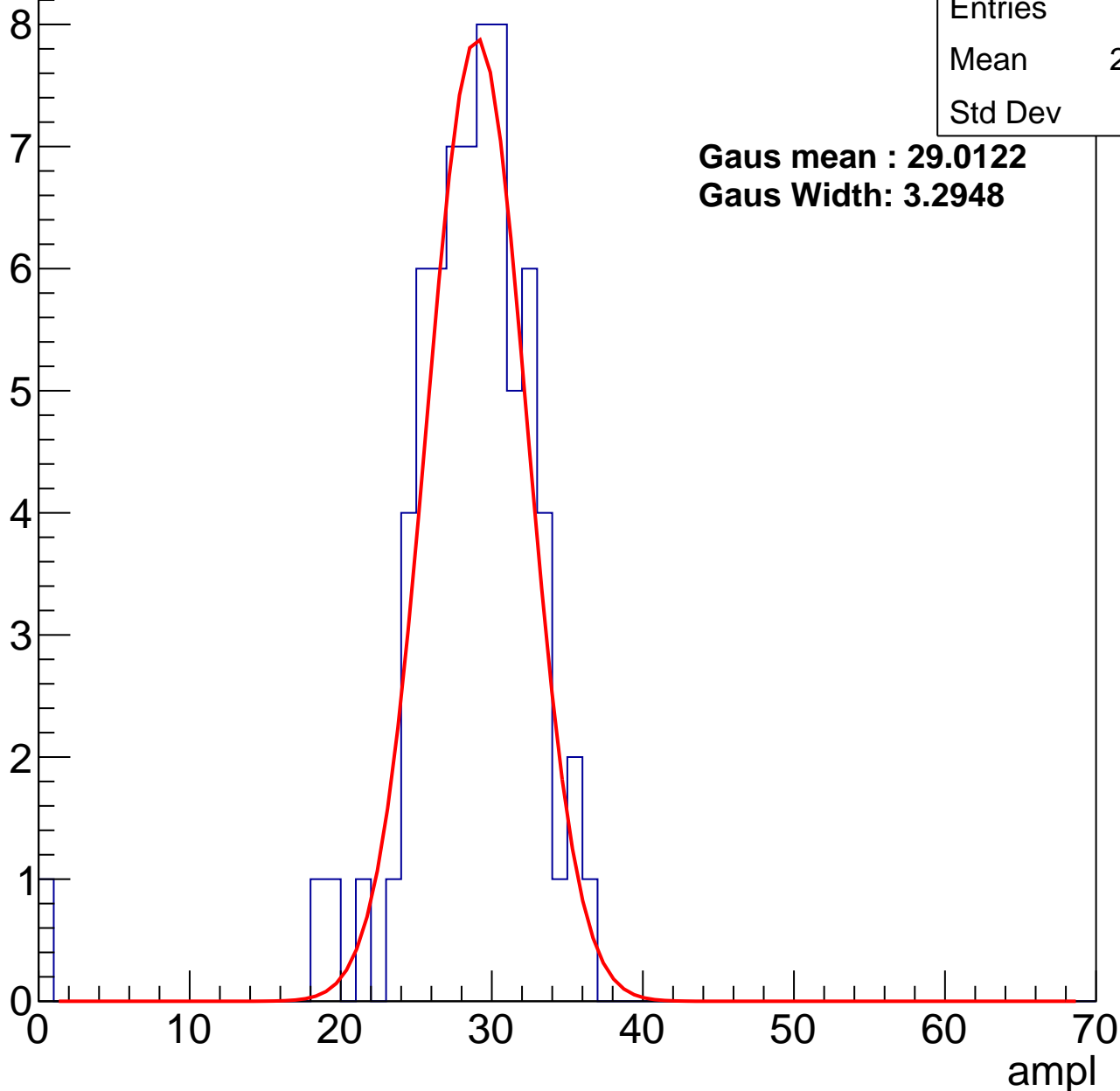
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	27.99
Std Dev	4.88

**Gaus mean : 29.0122**

**Gaus Width: 3.2948**



# B1L003S, U6-ch114, adc1

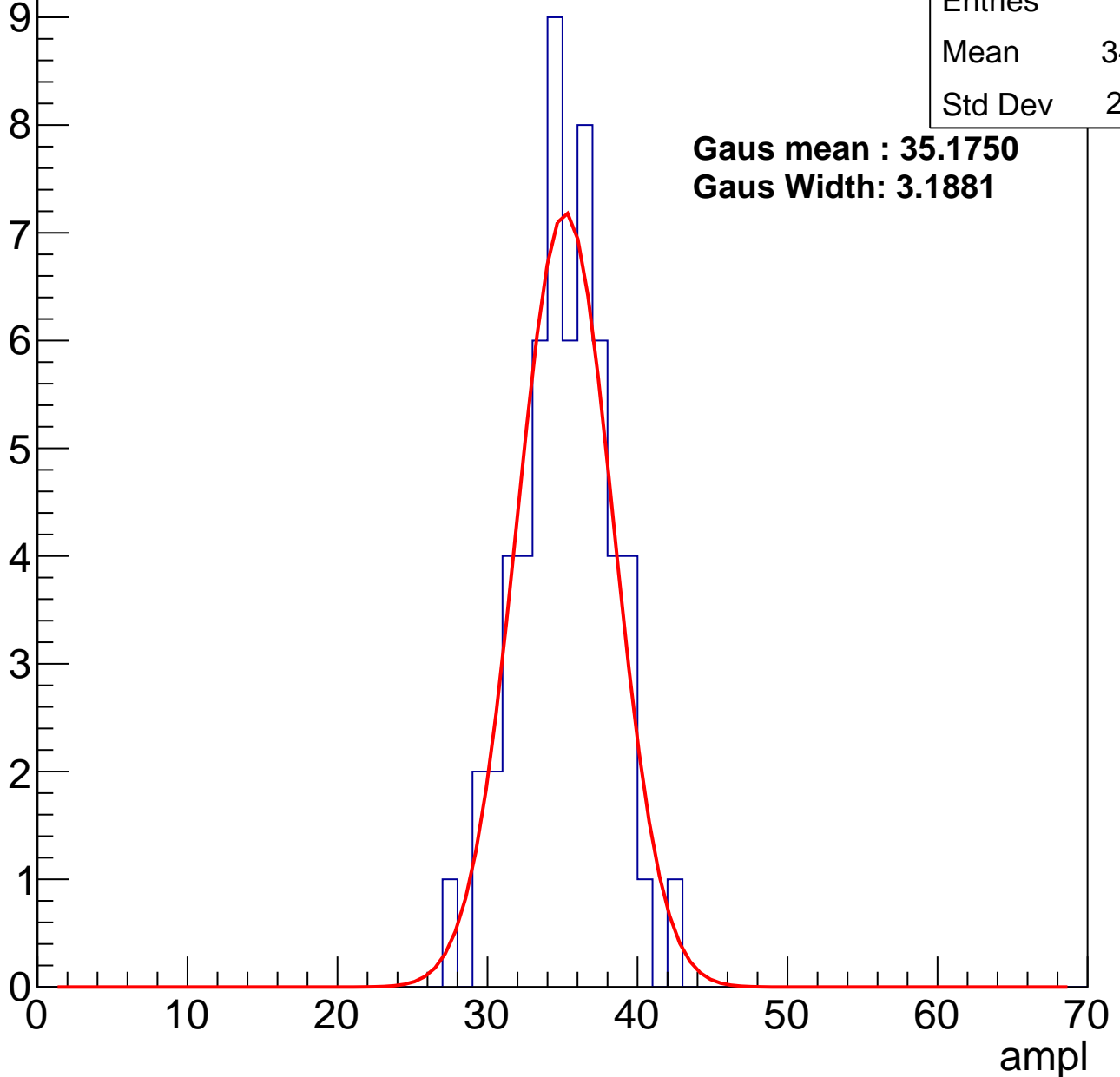
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	34.67
Std Dev	2.991

**Gaus mean : 35.1750**

**Gaus Width: 3.1881**



# B1L003S, U6-ch114, adc2

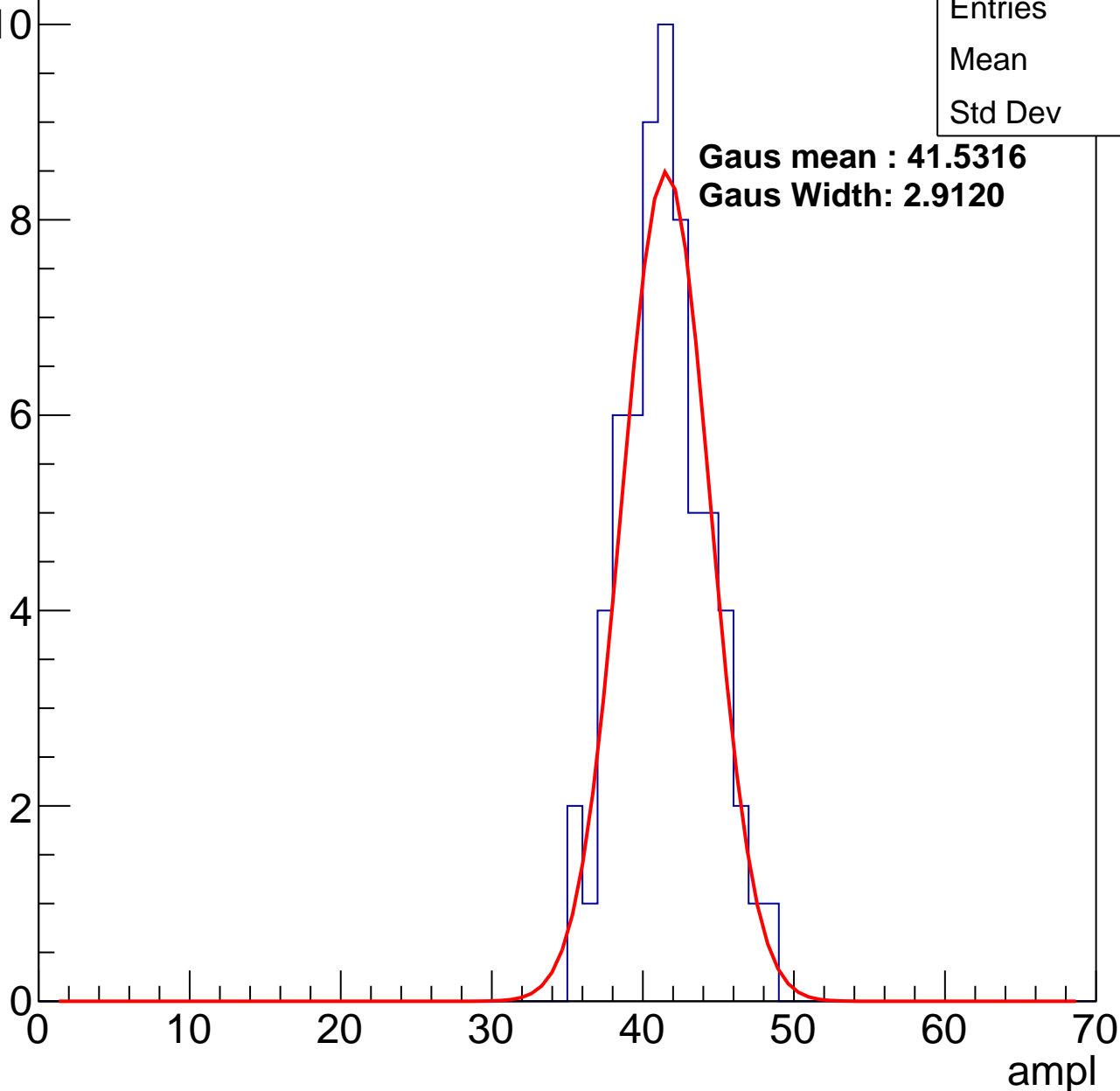
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	41
Std Dev	2.85

**Gaus mean : 41.5316**

**Gaus Width: 2.9120**

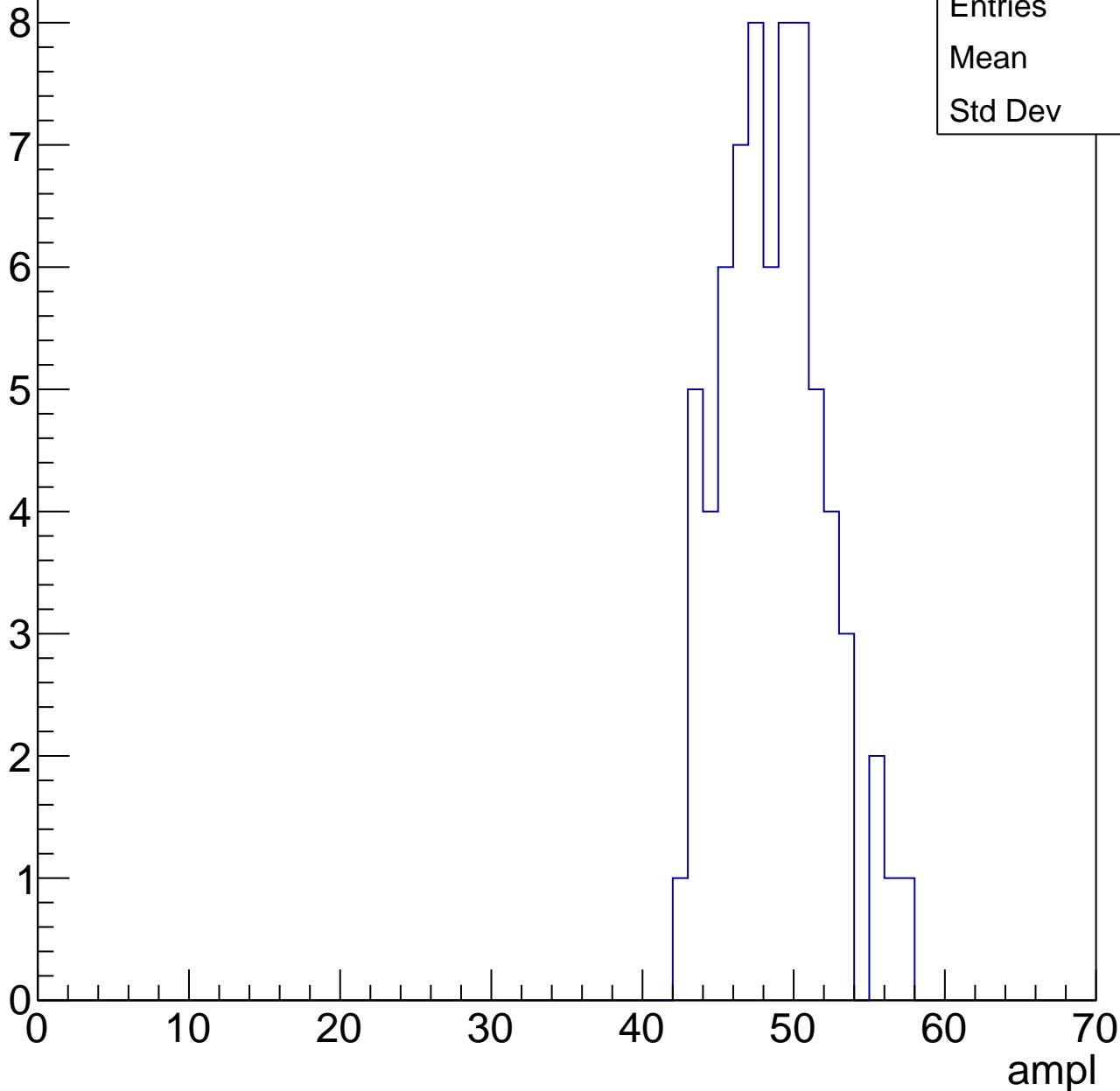


# B1L003S, U6-ch114, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	48.2
Std Dev	3.36

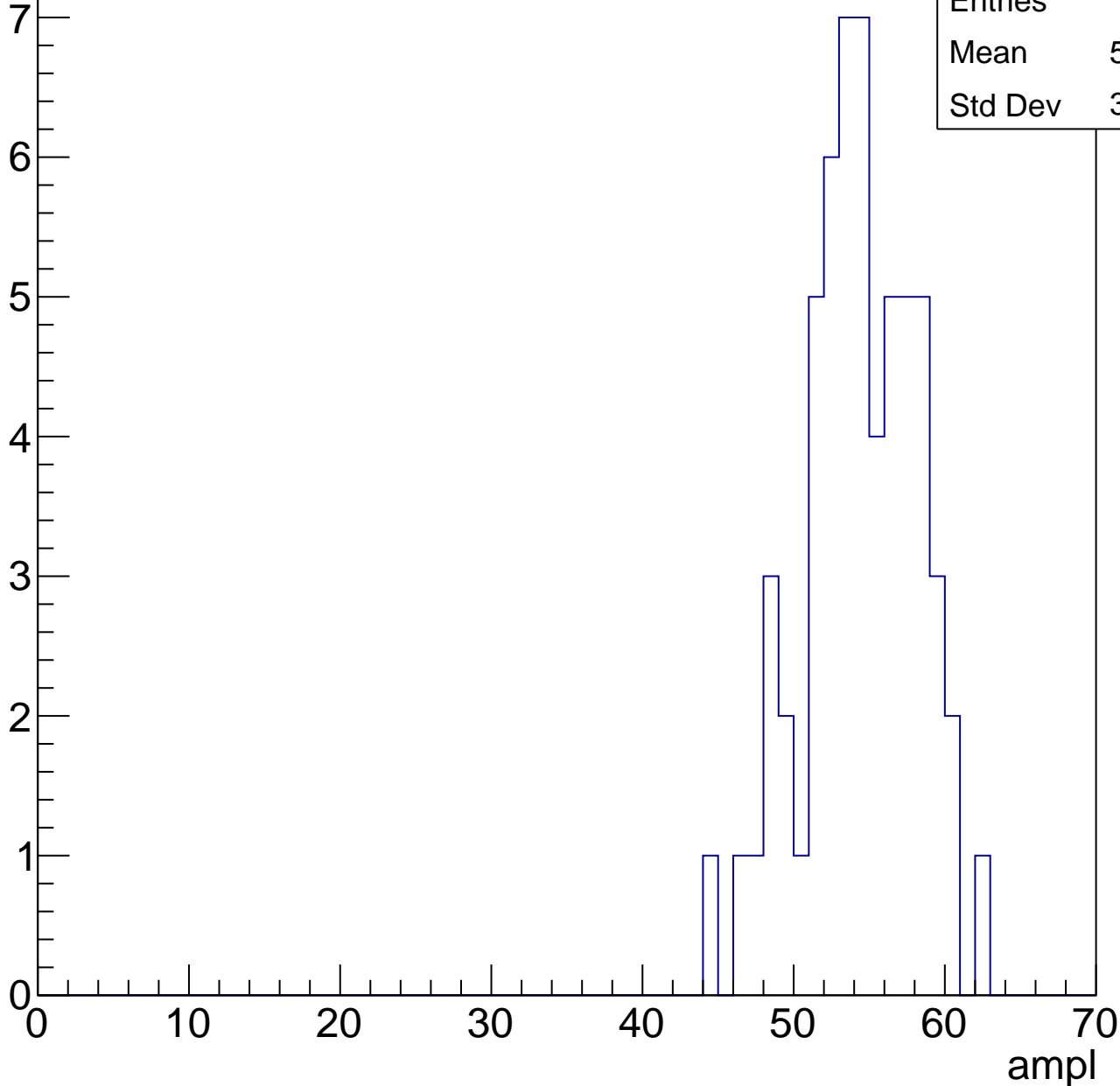


# B1L003S, U6-ch114, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	53.88
Std Dev	3.733

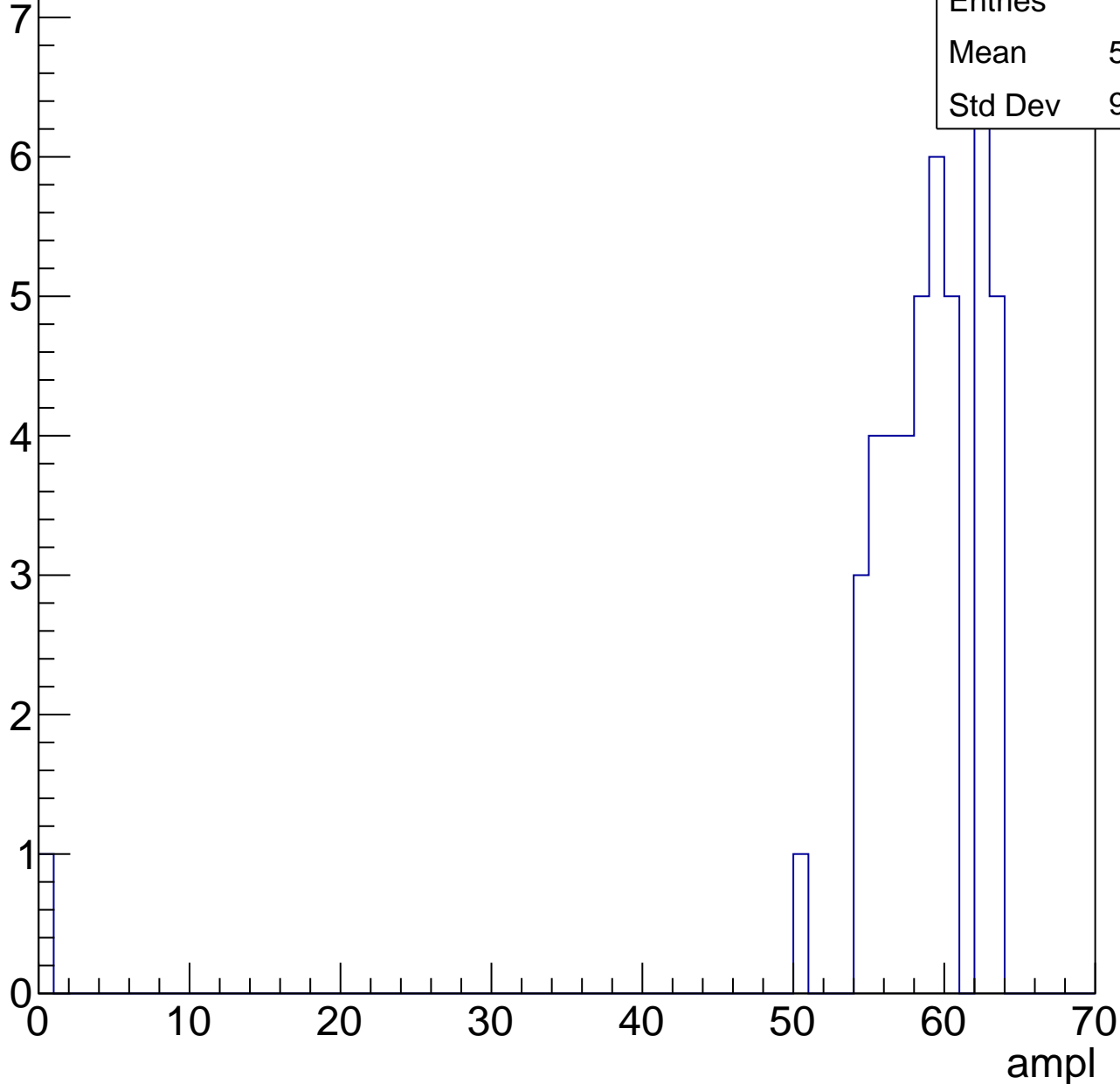


# B1L003S, U6-ch114, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	45
Mean	57.27
Std Dev	9.154

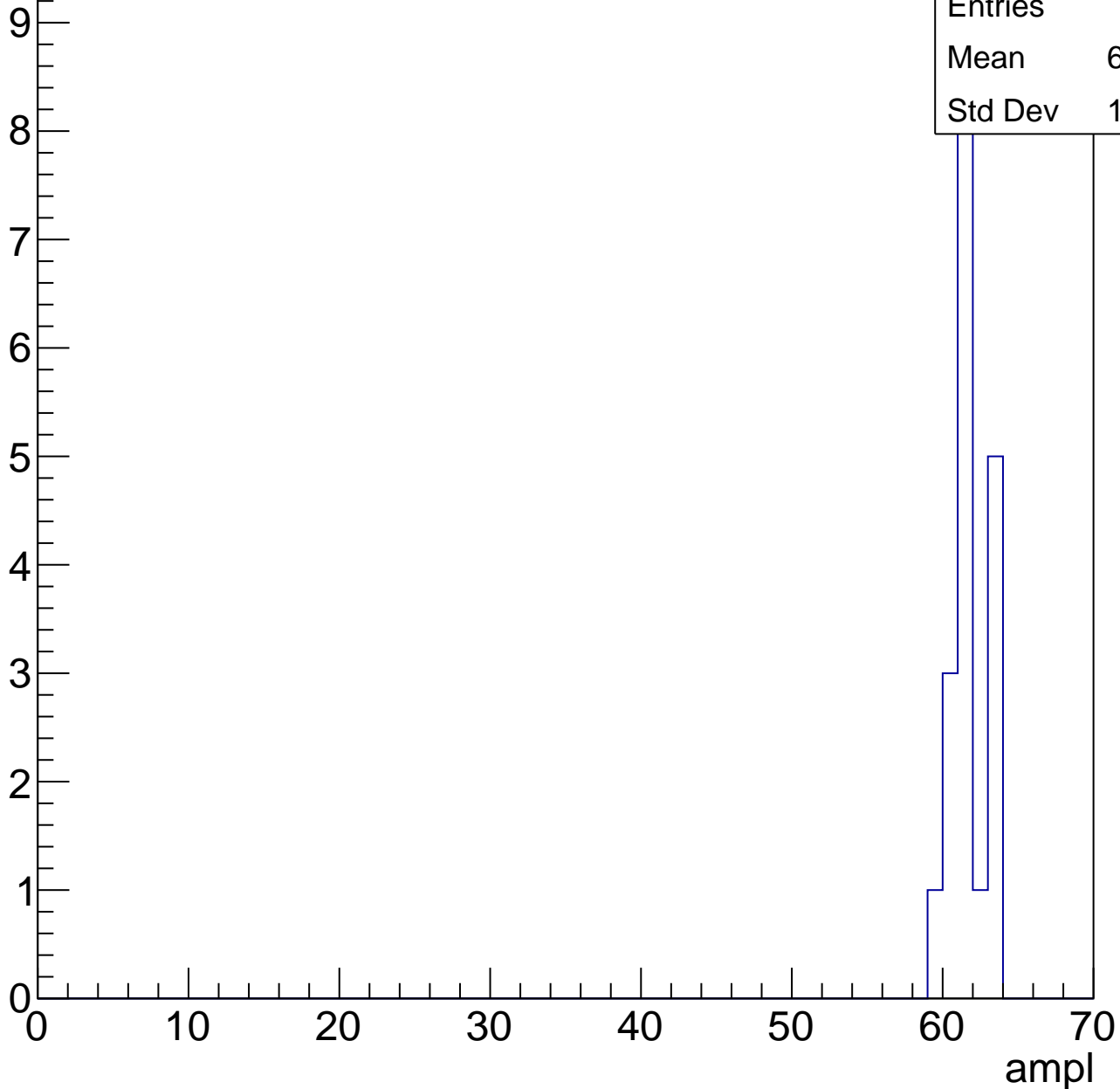


# B1L003S, U6-ch114, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	19
Mean	61.32
Std Dev	1.172

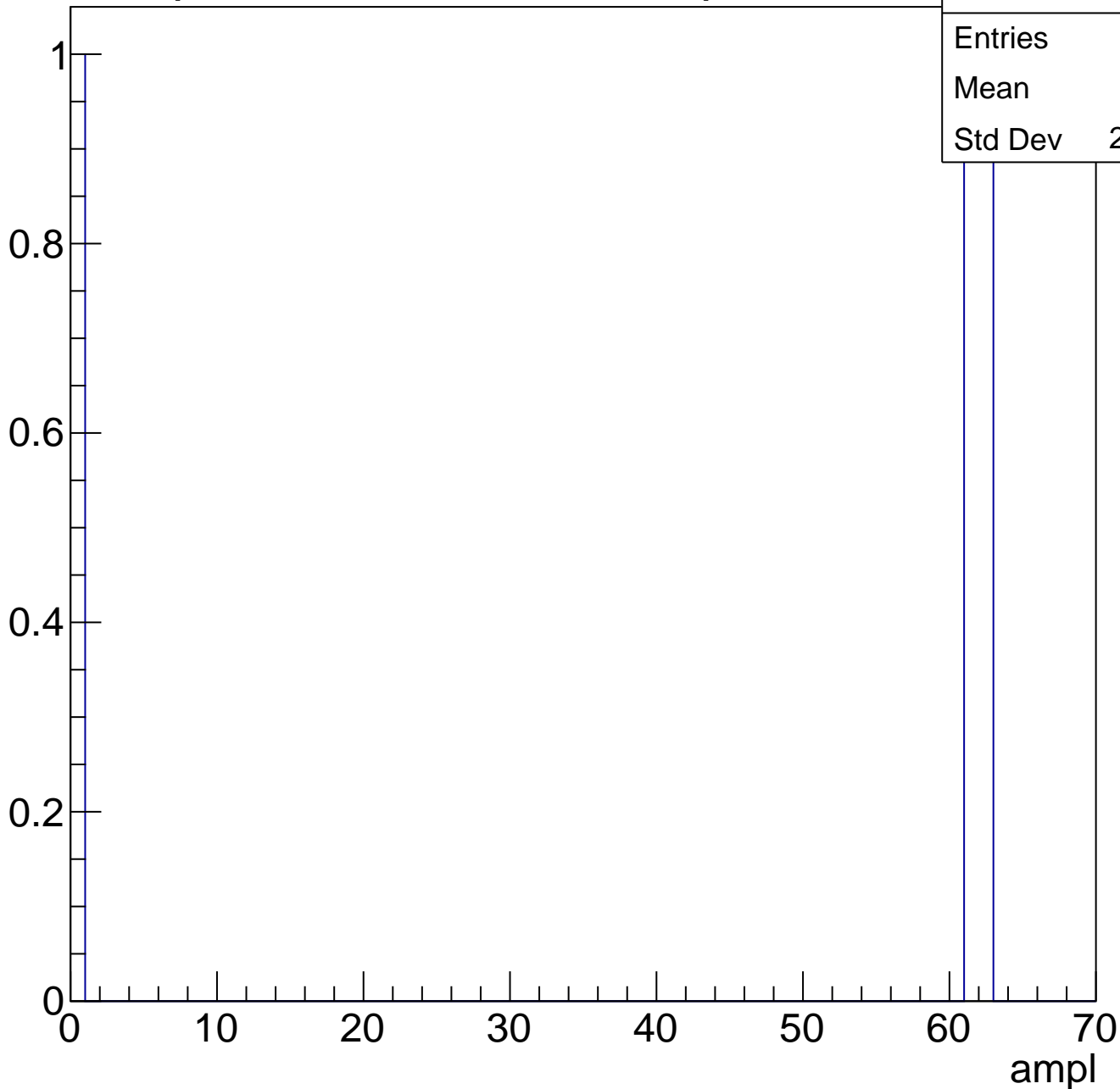




# B1L003S, U6-ch114, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch115, adc0

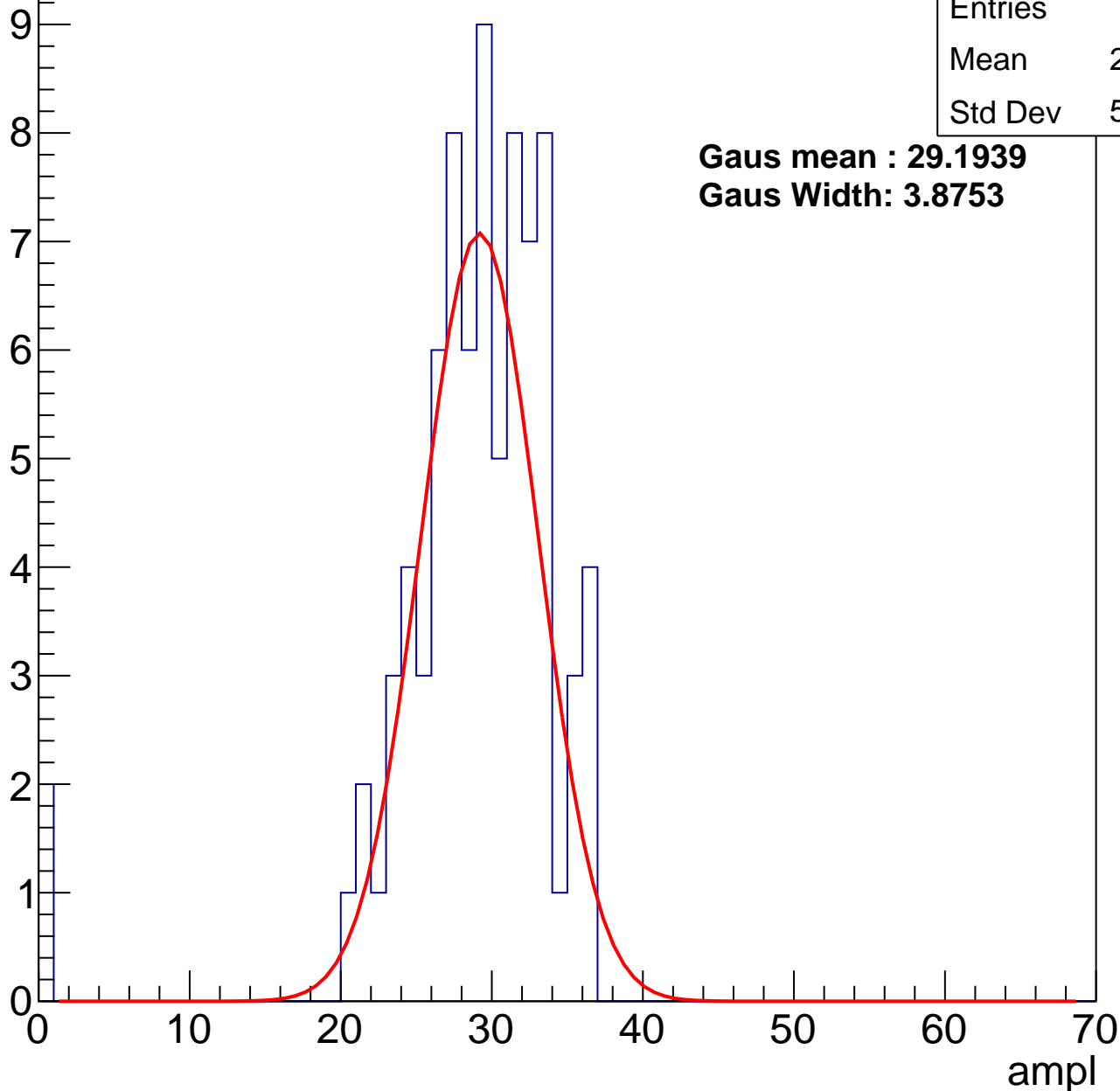
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	81
Mean	28.32
Std Dev	5.887

**Gaus mean : 29.1939**

**Gaus Width: 3.8753**



# B1L003S, U6-ch115, adc1

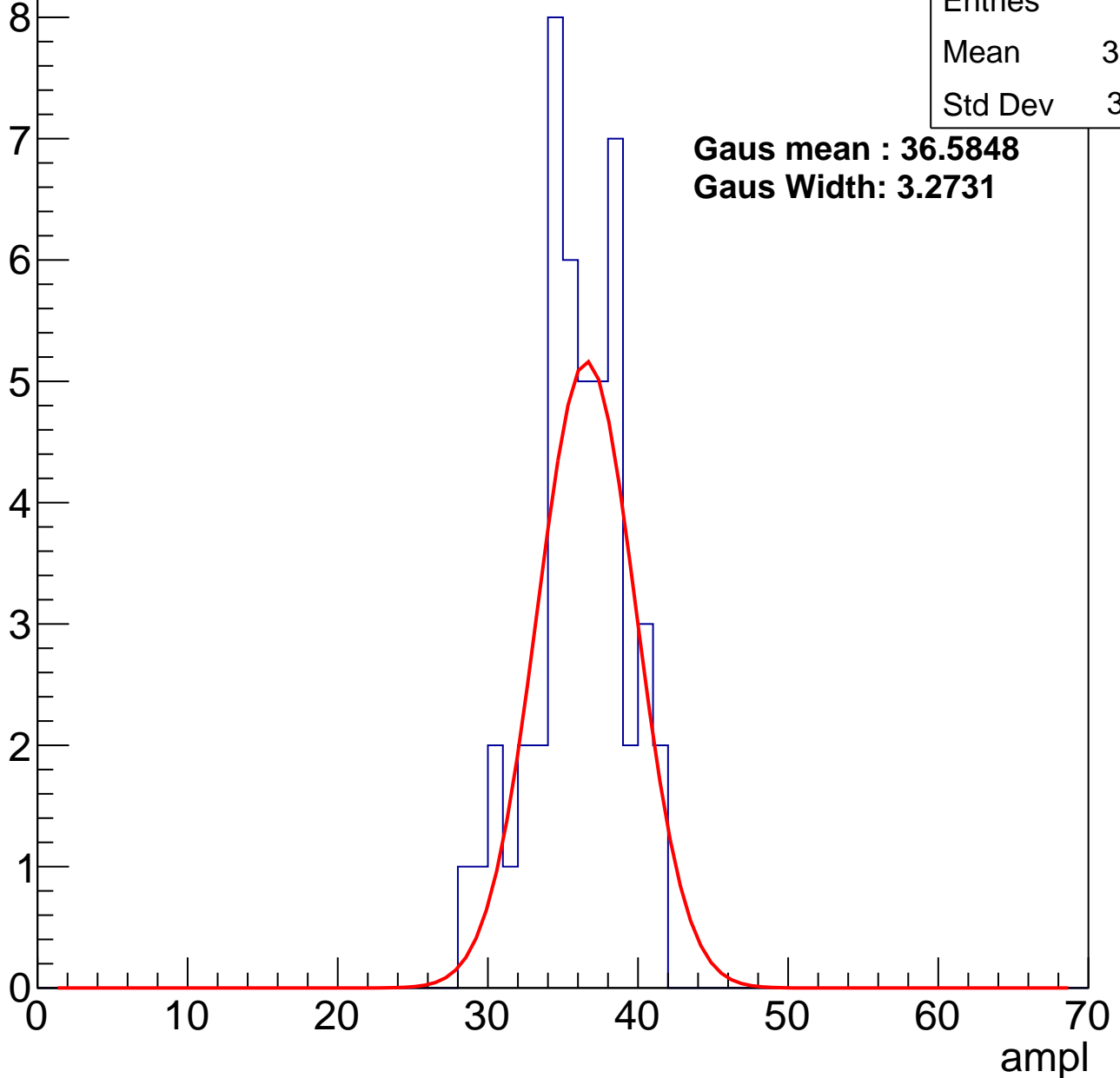
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	47
Mean	35.55
Std Dev	3.051

**Gaus mean : 36.5848**

**Gaus Width: 3.2731**



# B1L003S, U6-ch115, adc2

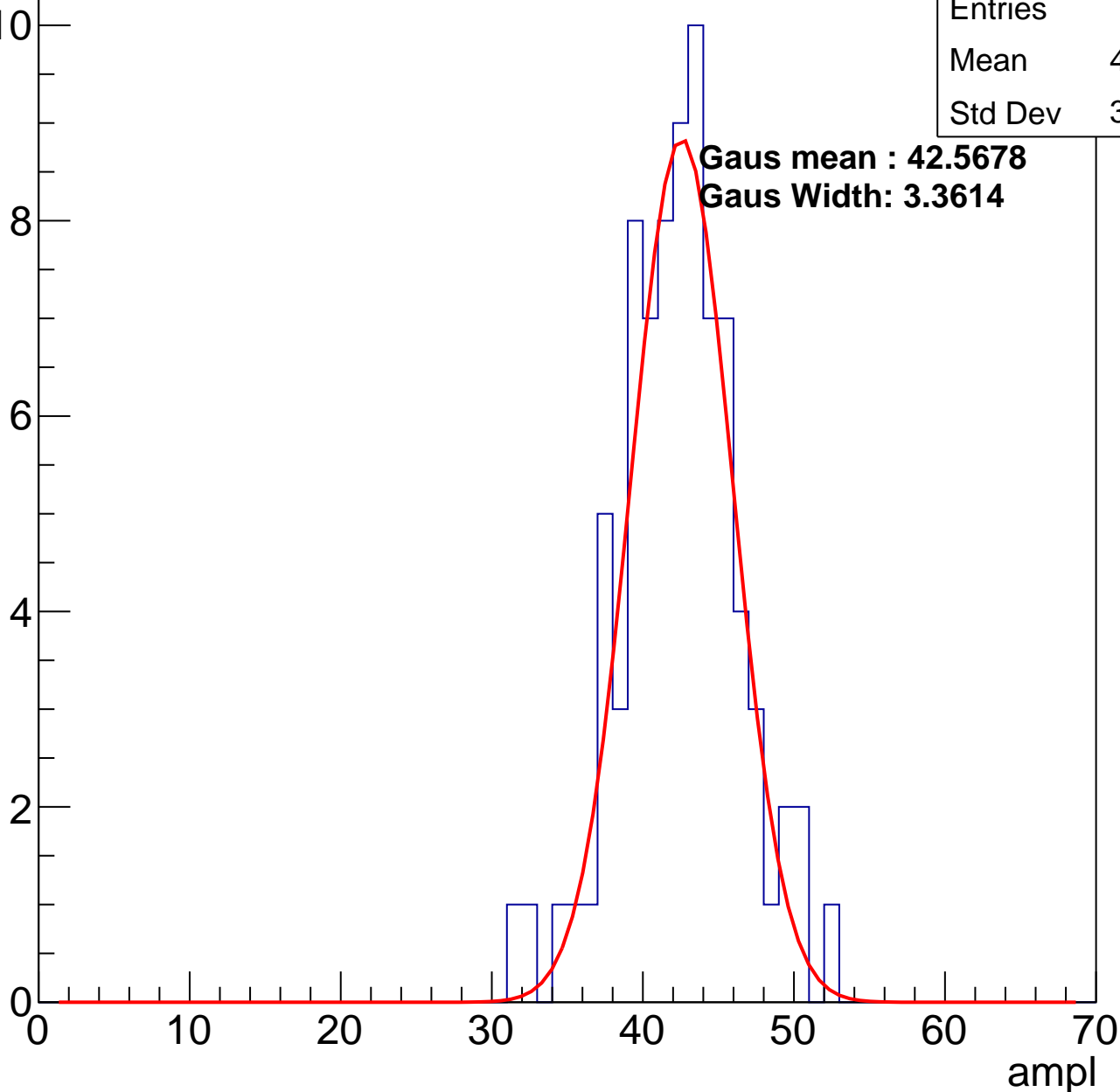
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	82
Mean	41.96
Std Dev	3.909

**Gaus mean : 42.5678**

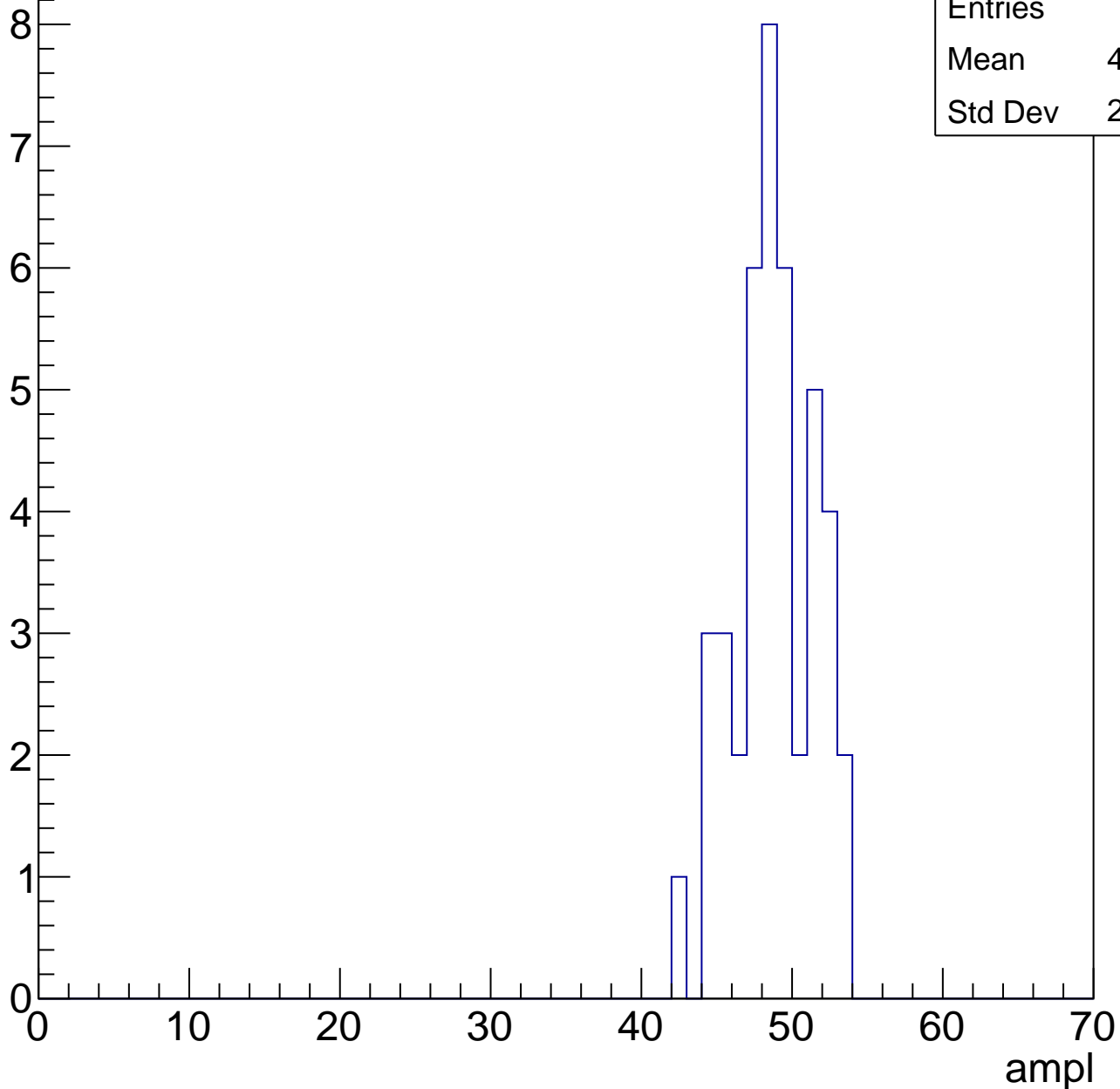
**Gaus Width: 3.3614**



# B1L003S, U6-ch115, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



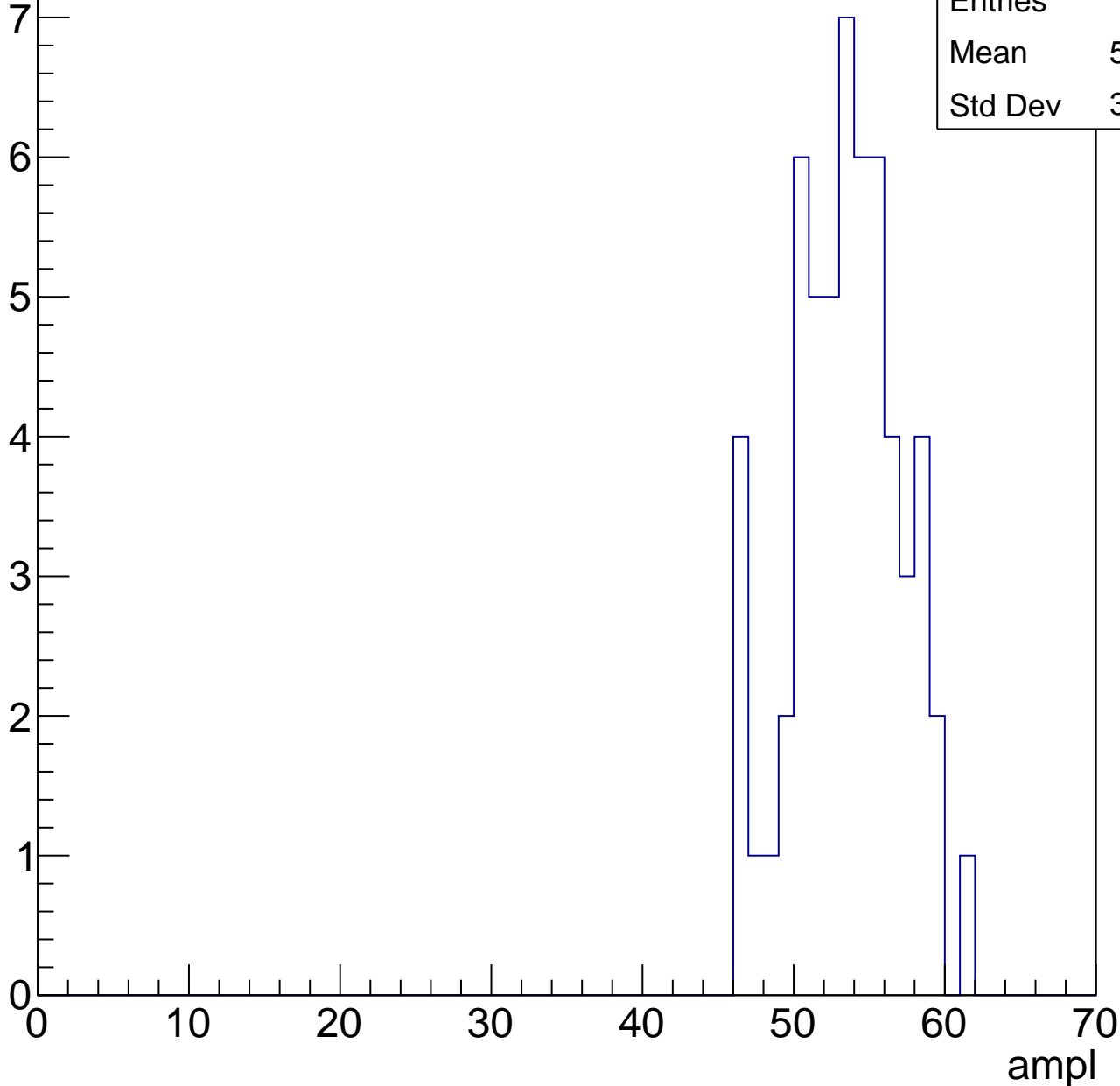
Entries	42
Mean	48.33
Std Dev	2.643

# B1L003S, U6-ch115, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	53.04
Std Dev	3.549



# B1L003S, U6-ch115, adc5

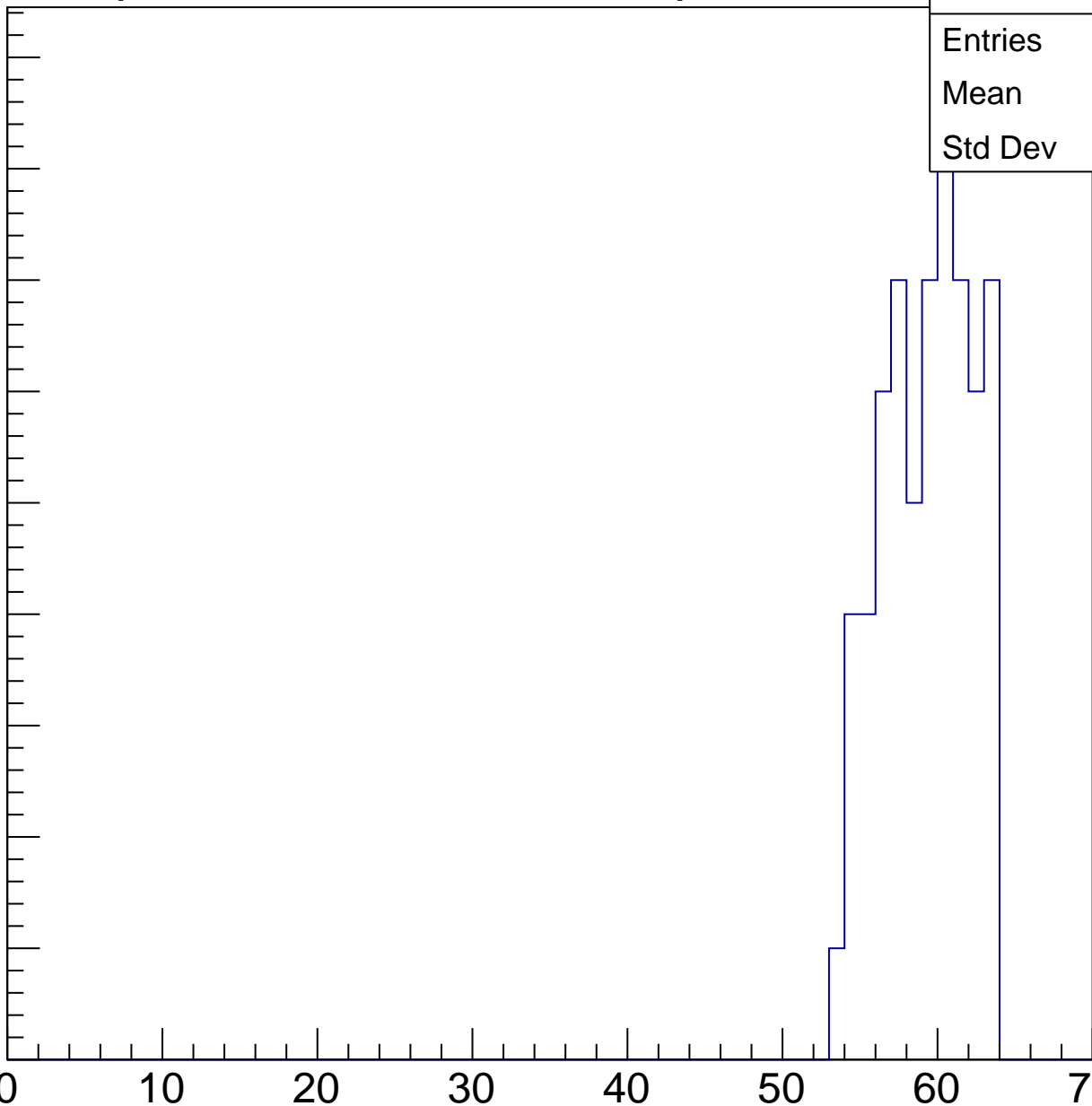
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	63
Mean	58.84
Std Dev	2.784

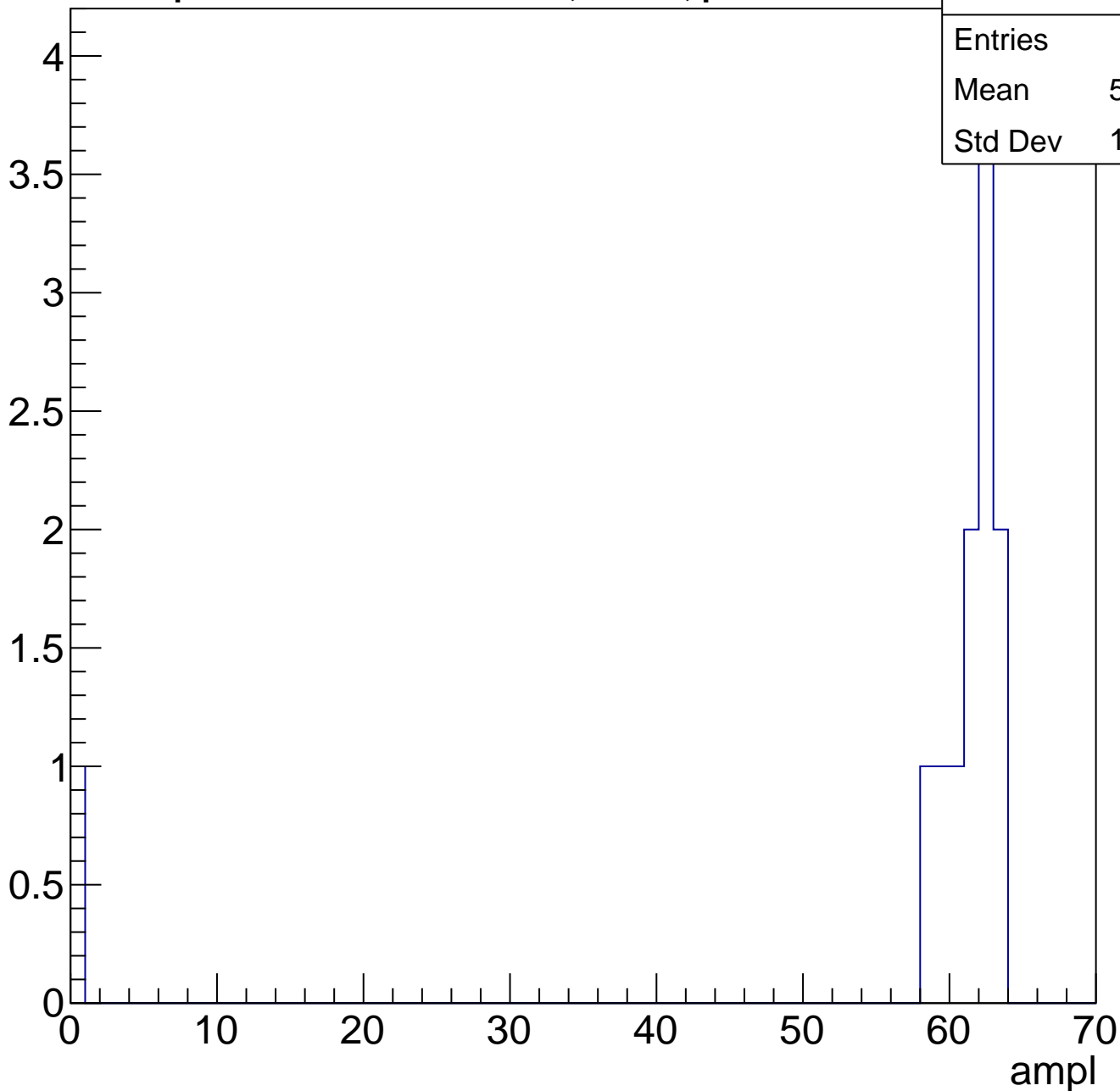
ampl



# B1L003S, U6-ch115, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch115, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	63
Std Dev	0

# B1L003S, U6-ch116, adc0

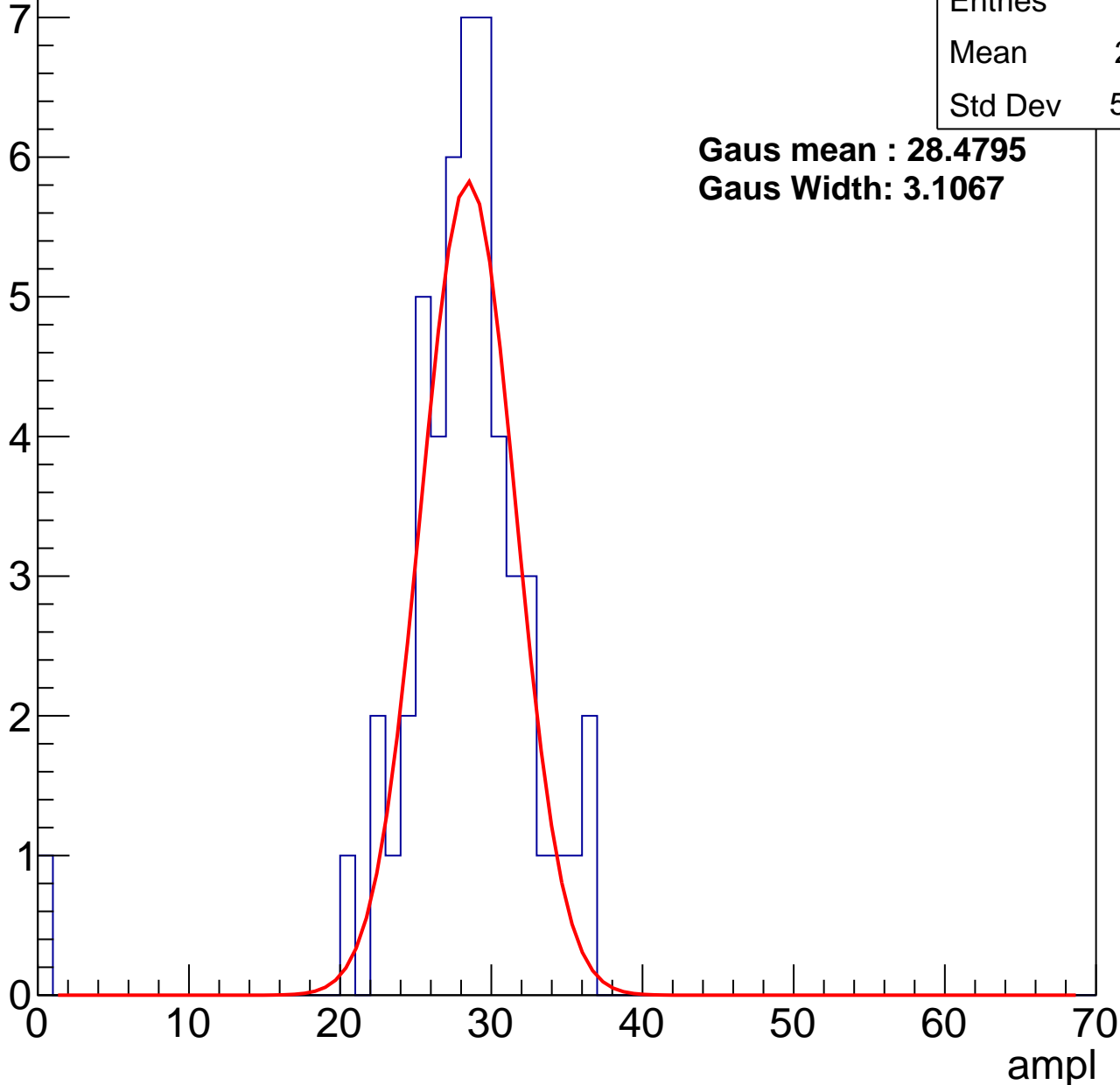
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	51
Mean	27.61
Std Dev	5.187

**Gaus mean : 28.4795**

**Gaus Width: 3.1067**



# B1L003S, U6-ch116, adc1

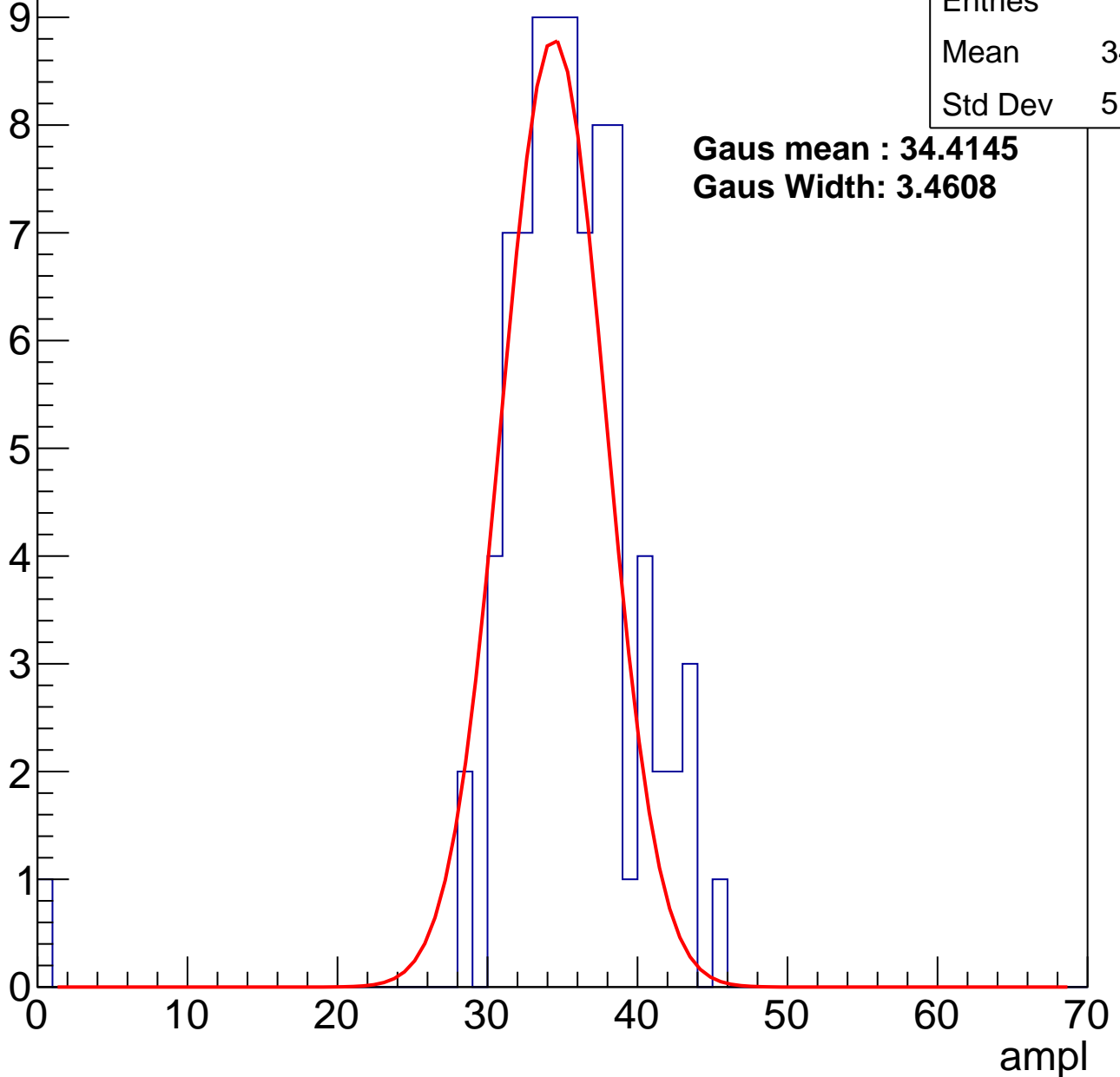
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	84
Mean	34.83
Std Dev	5.266

**Gaus mean : 34.4145**

**Gaus Width: 3.4608**



# B1L003S, U6-ch116, adc2

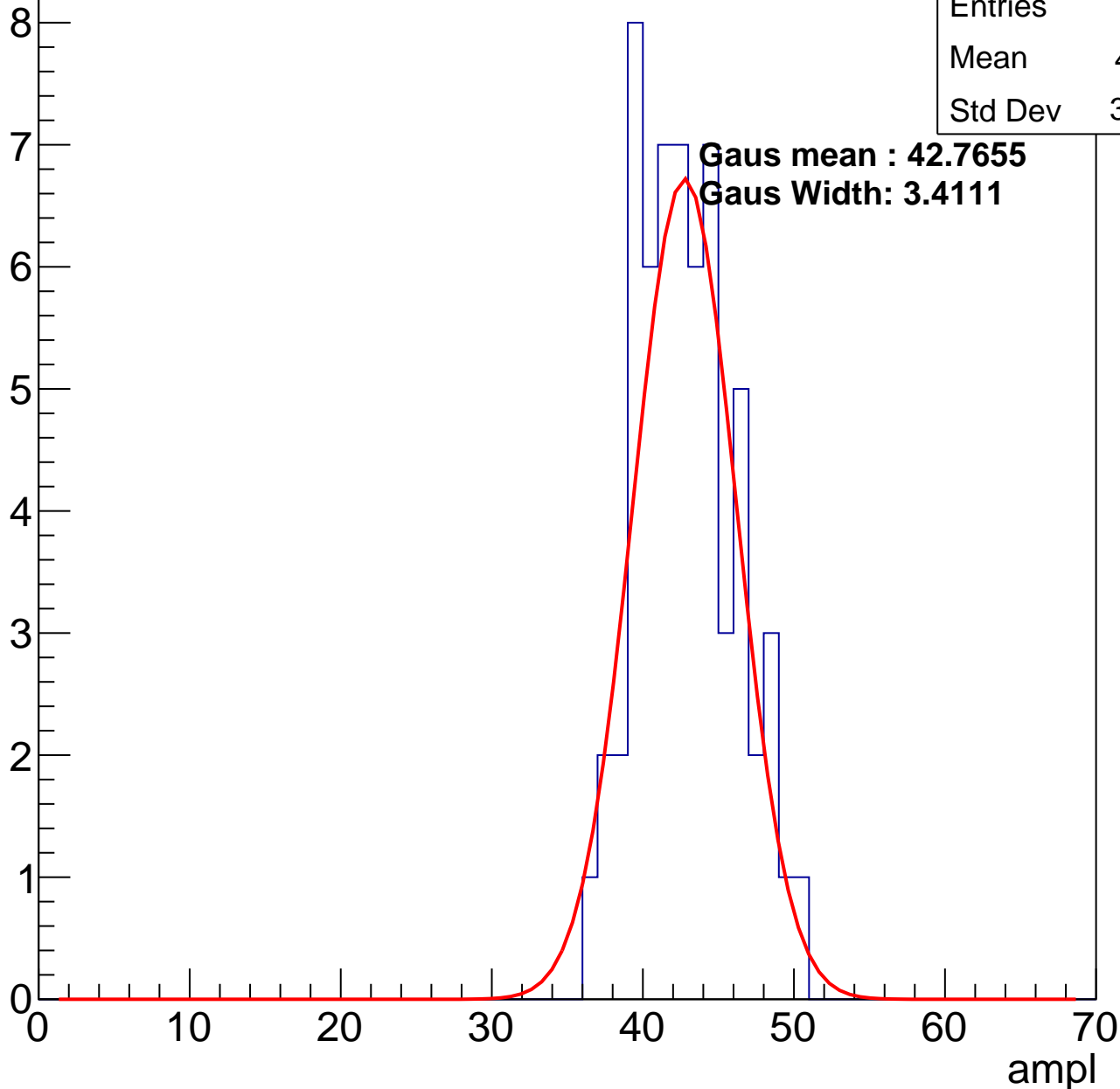
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	42.41
Std Dev	3.195

**Gaus mean : 42.7655**

**Gaus Width: 3.4111**

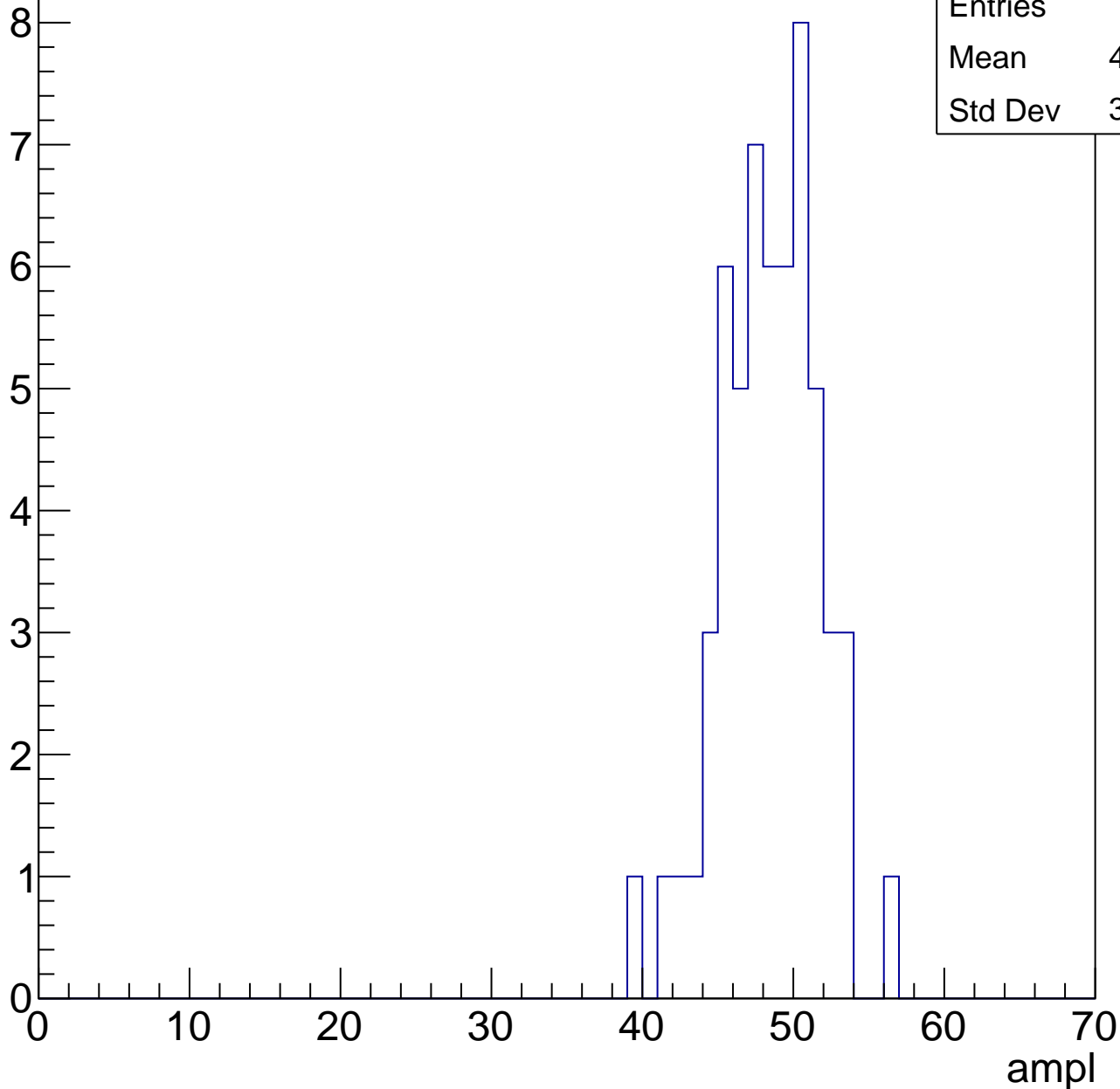


# B1L003S, U6-ch116, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	47.96
Std Dev	3.217



# B1L003S, U6-ch116, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	63
Mean	54.33
Std Dev	3.029

Entry

10

8

6

4

2

0

0

10

20

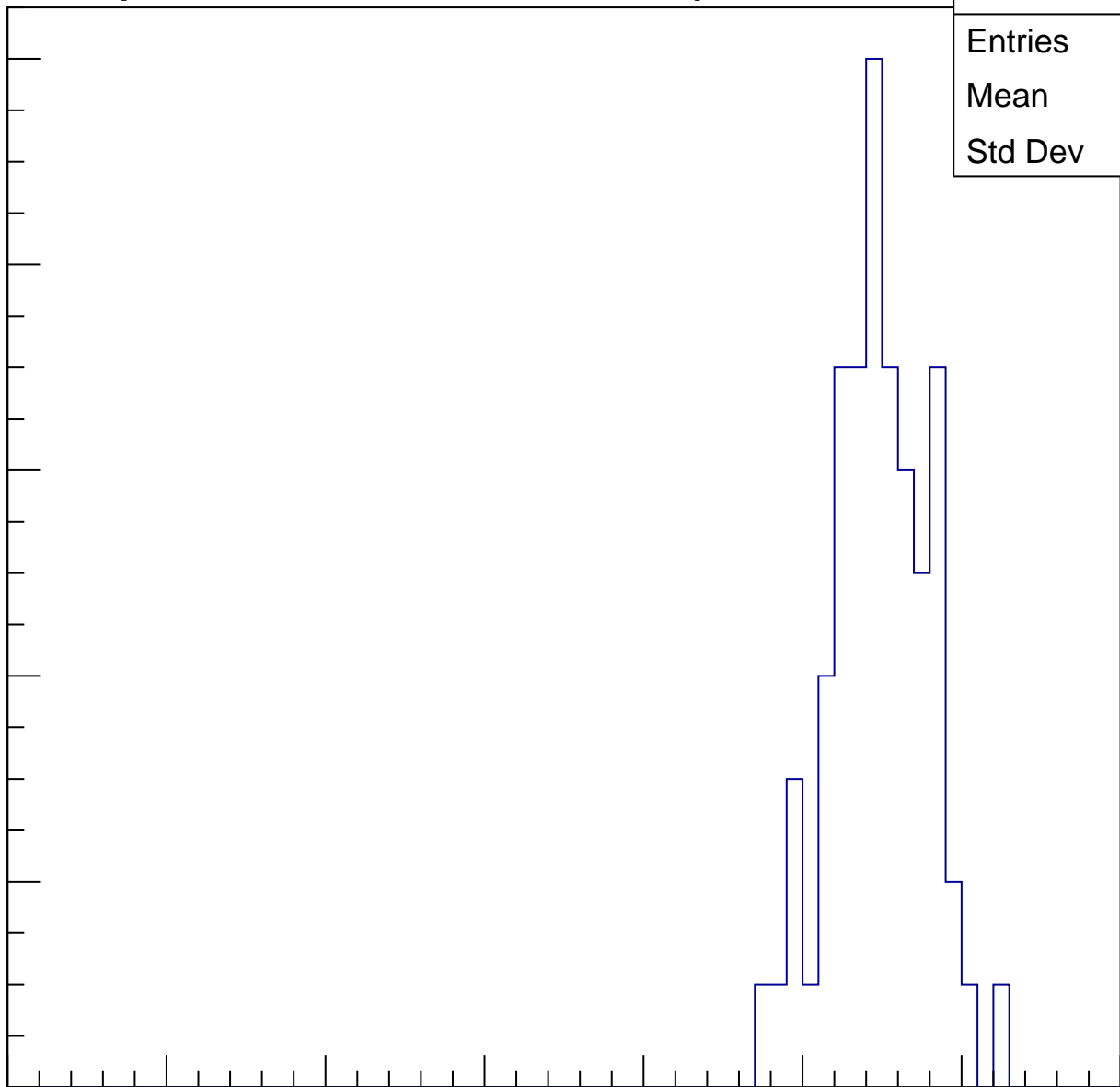
30

40

50

60

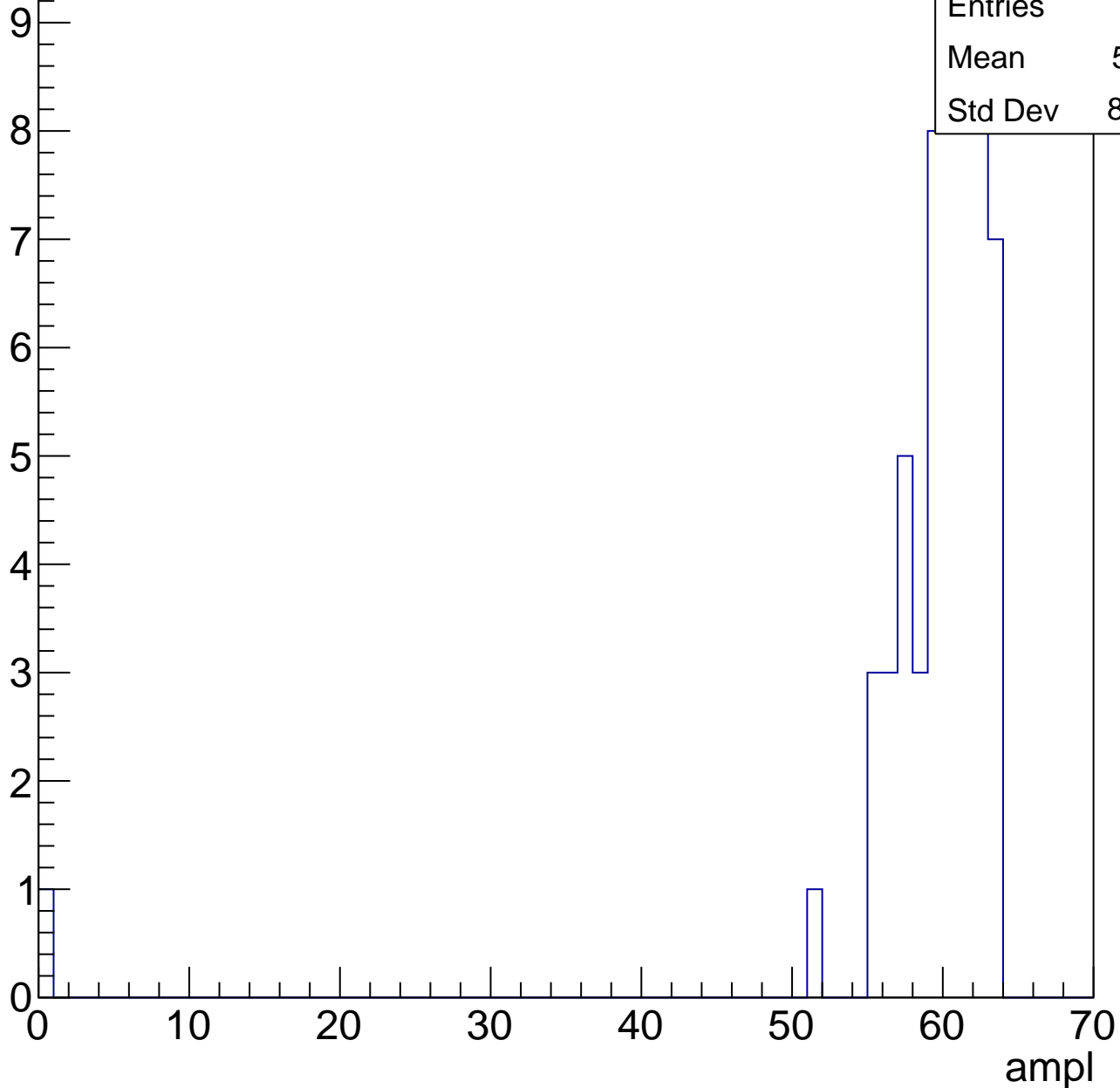
ampl



# B1L003S, U6-ch116, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch116, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	5
Mean	62.4
Std Dev	0.8



# B1L003S, U6-ch116, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch117, adc0

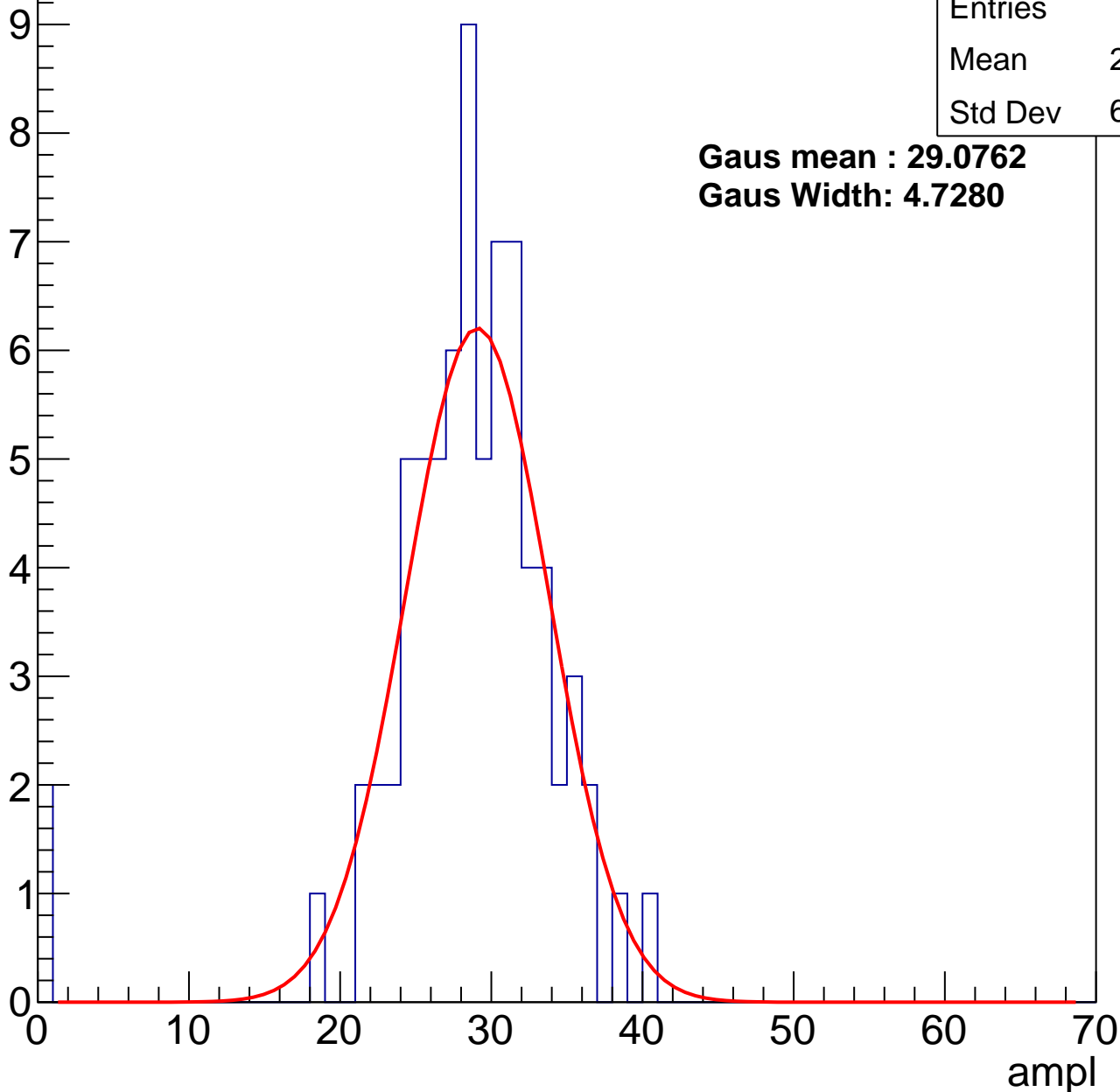
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	75
Mean	27.92
Std Dev	6.207

**Gaus mean : 29.0762**

**Gaus Width: 4.7280**



# B1L003S, U6-ch117, adc1

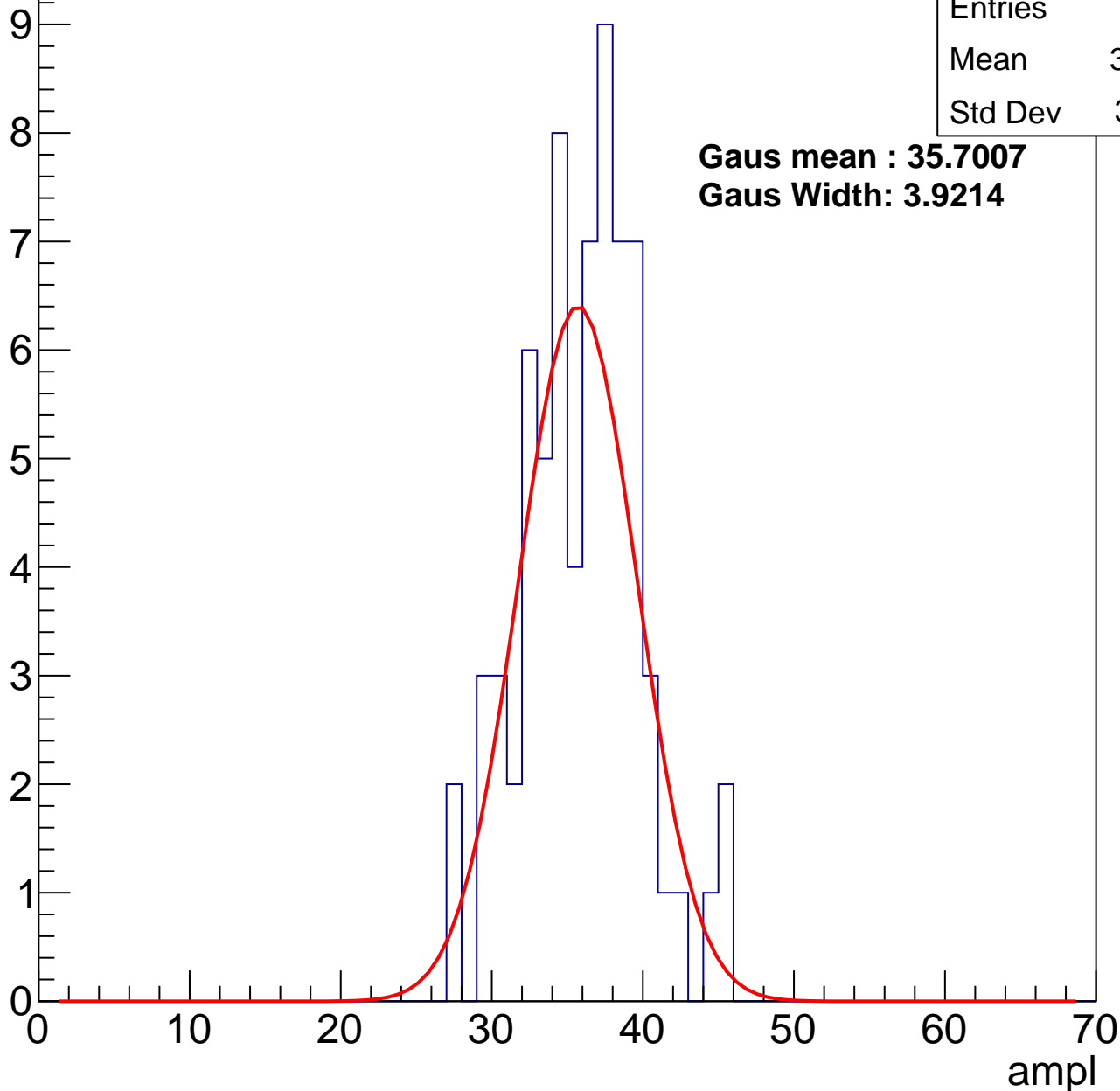
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	71
Mean	35.54
Std Dev	3.871

**Gaus mean : 35.7007**

**Gaus Width: 3.9214**



# B1L003S, U6-ch117, adc2

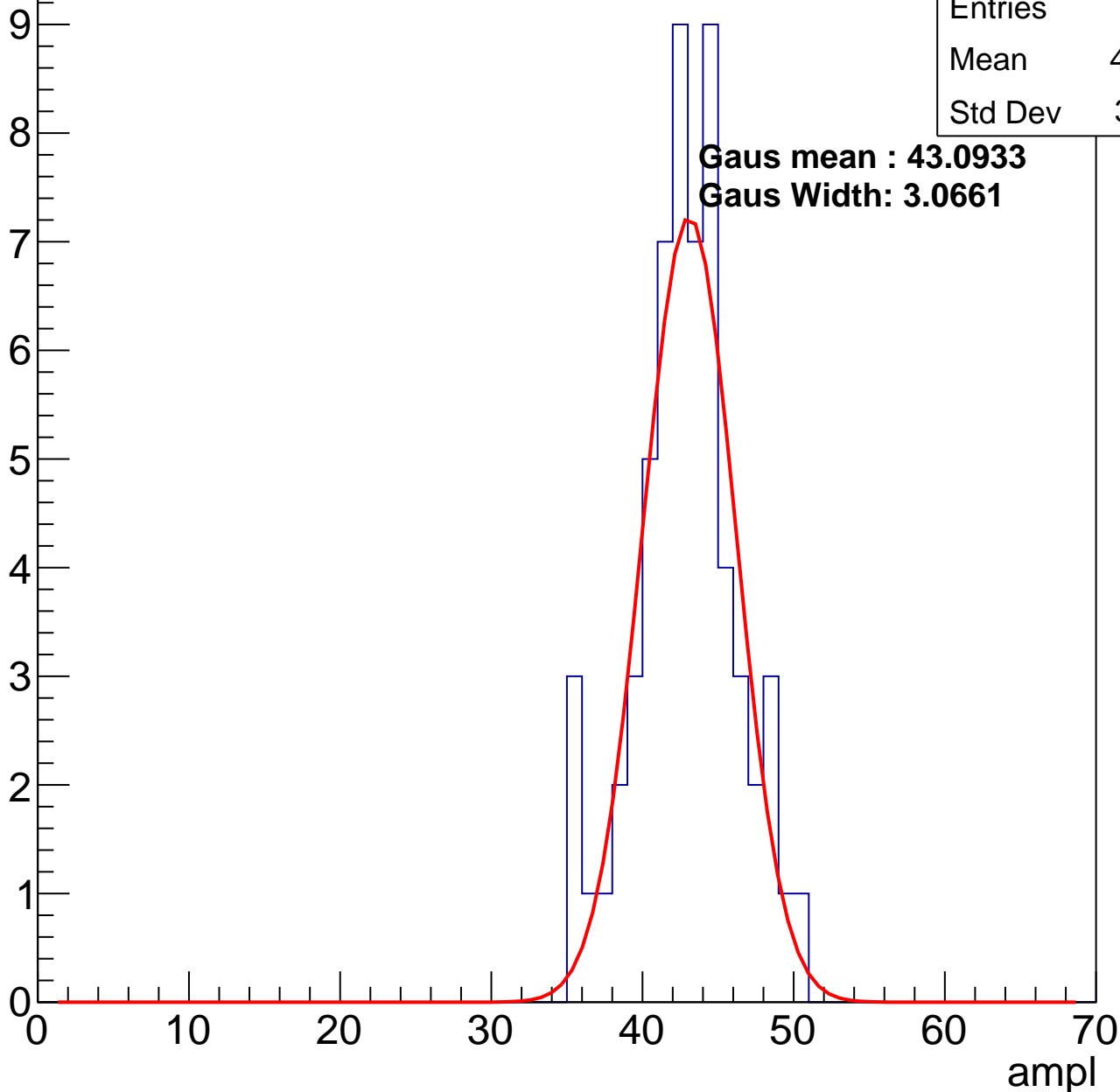
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	42.43
Std Dev	3.341

**Gaus mean : 43.0933**

**Gaus Width: 3.0661**

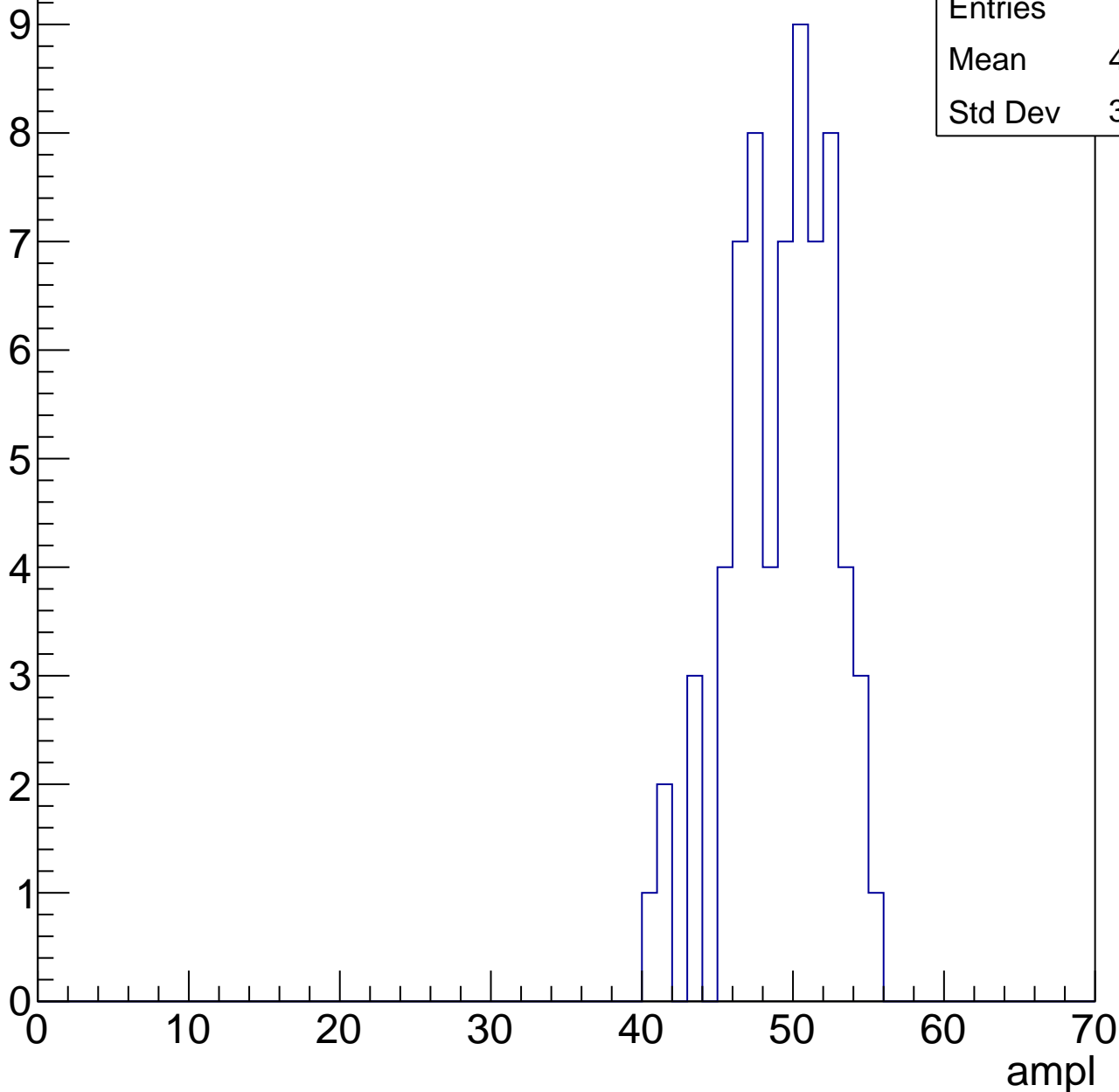


# B1L003S, U6-ch117, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	48.76
Std Dev	3.344

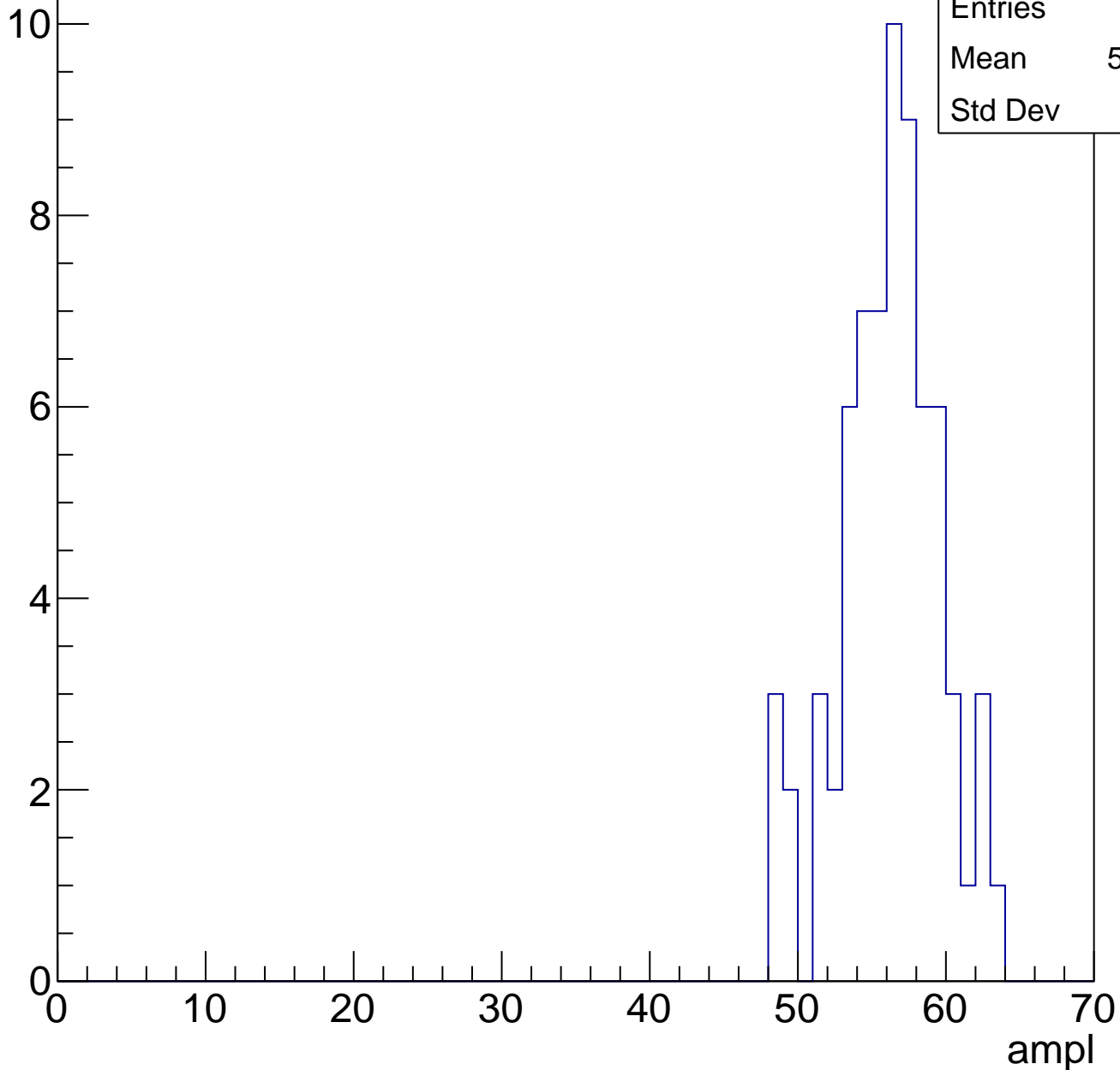


# B1L003S, U6-ch117, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	69
Mean	55.72
Std Dev	3.4

Entry

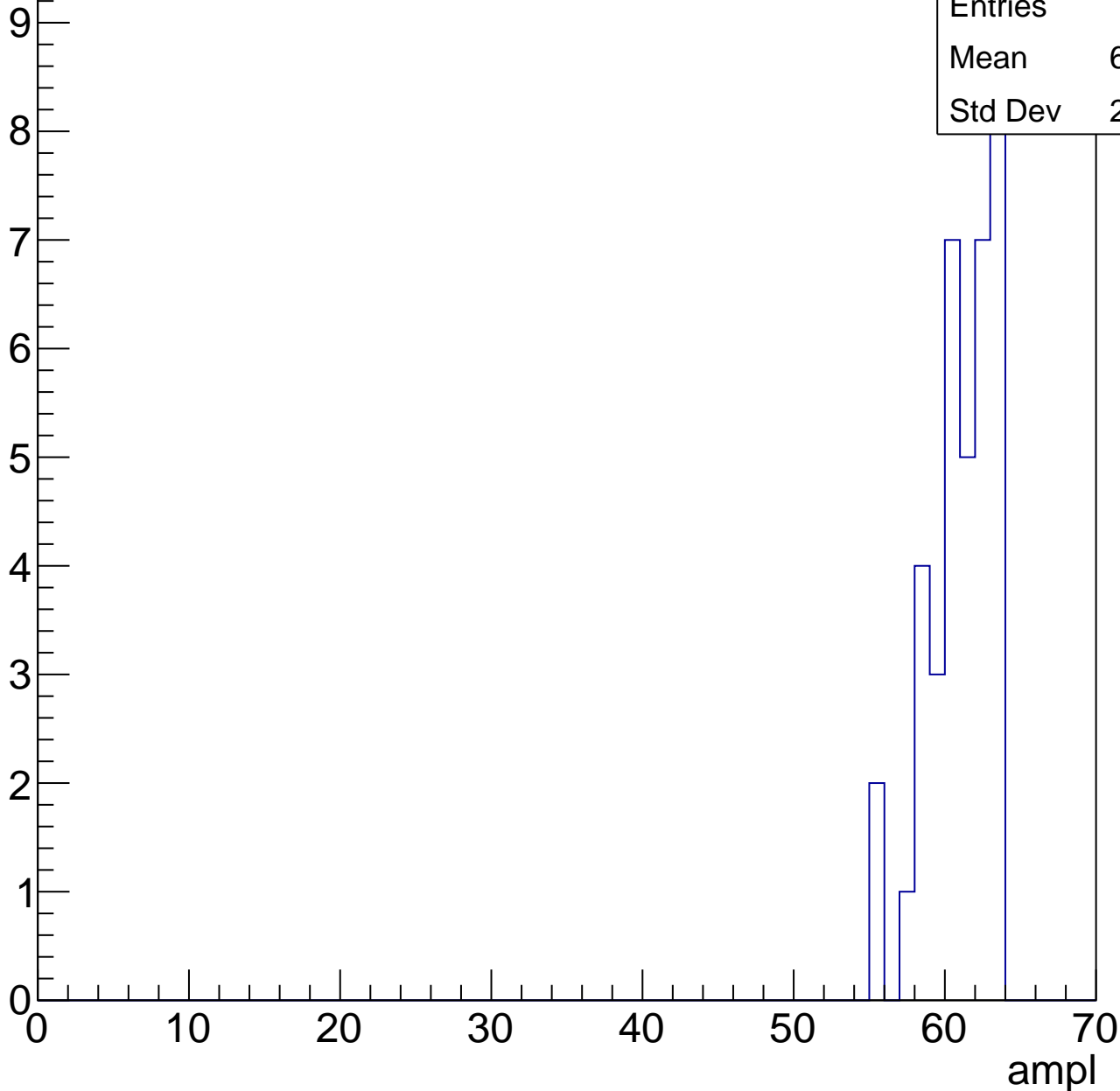


# B1L003S, U6-ch117, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

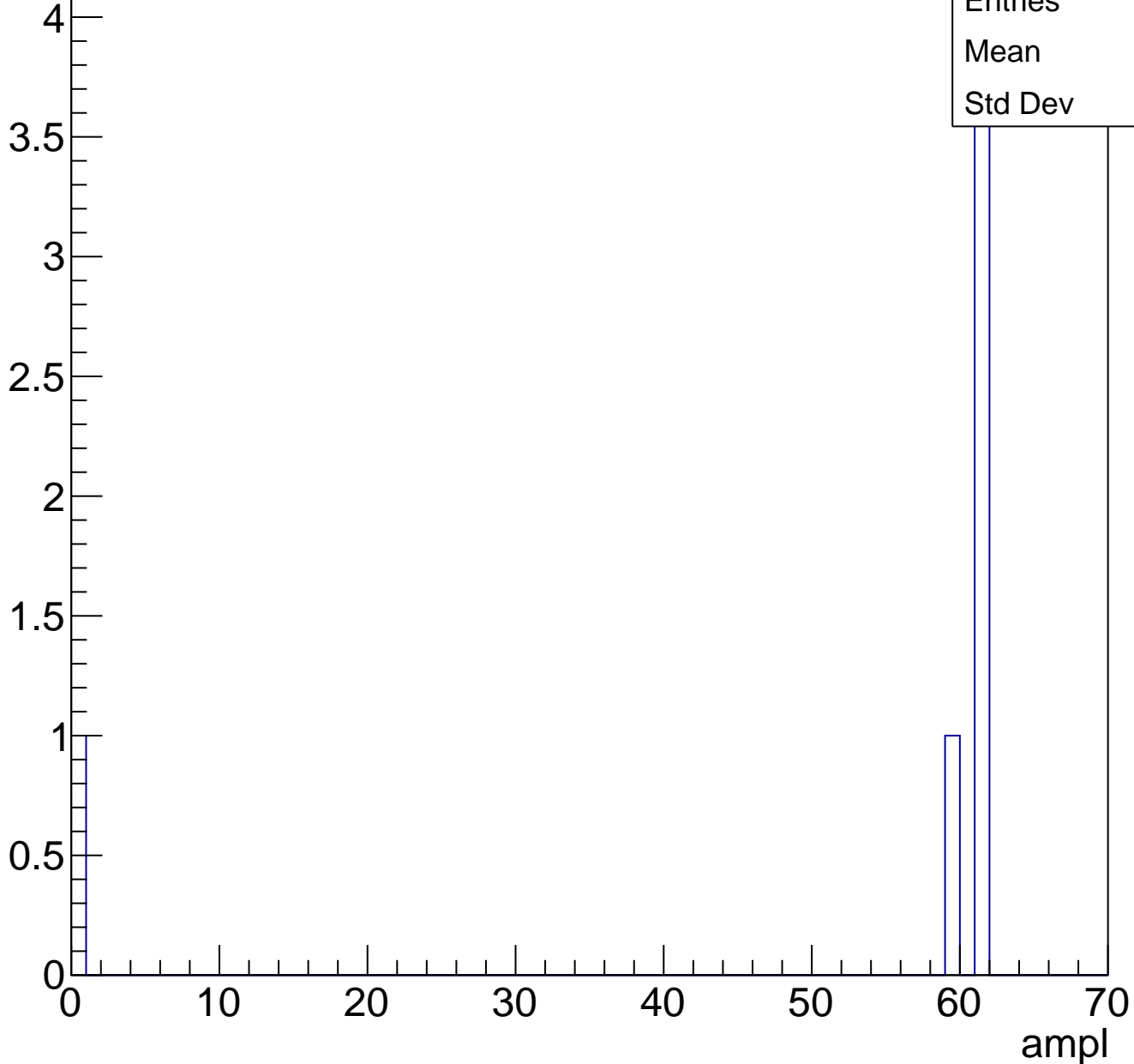
Entries	38
Mean	60.58
Std Dev	2.172



# B1L003S, U6-ch117, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	6
Mean	50.5
Std Dev	22.6



# B1L003S, U6-ch117, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch118, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	73
Mean	30.51
Std Dev	4.614

**Gaus mean : 31.4893**

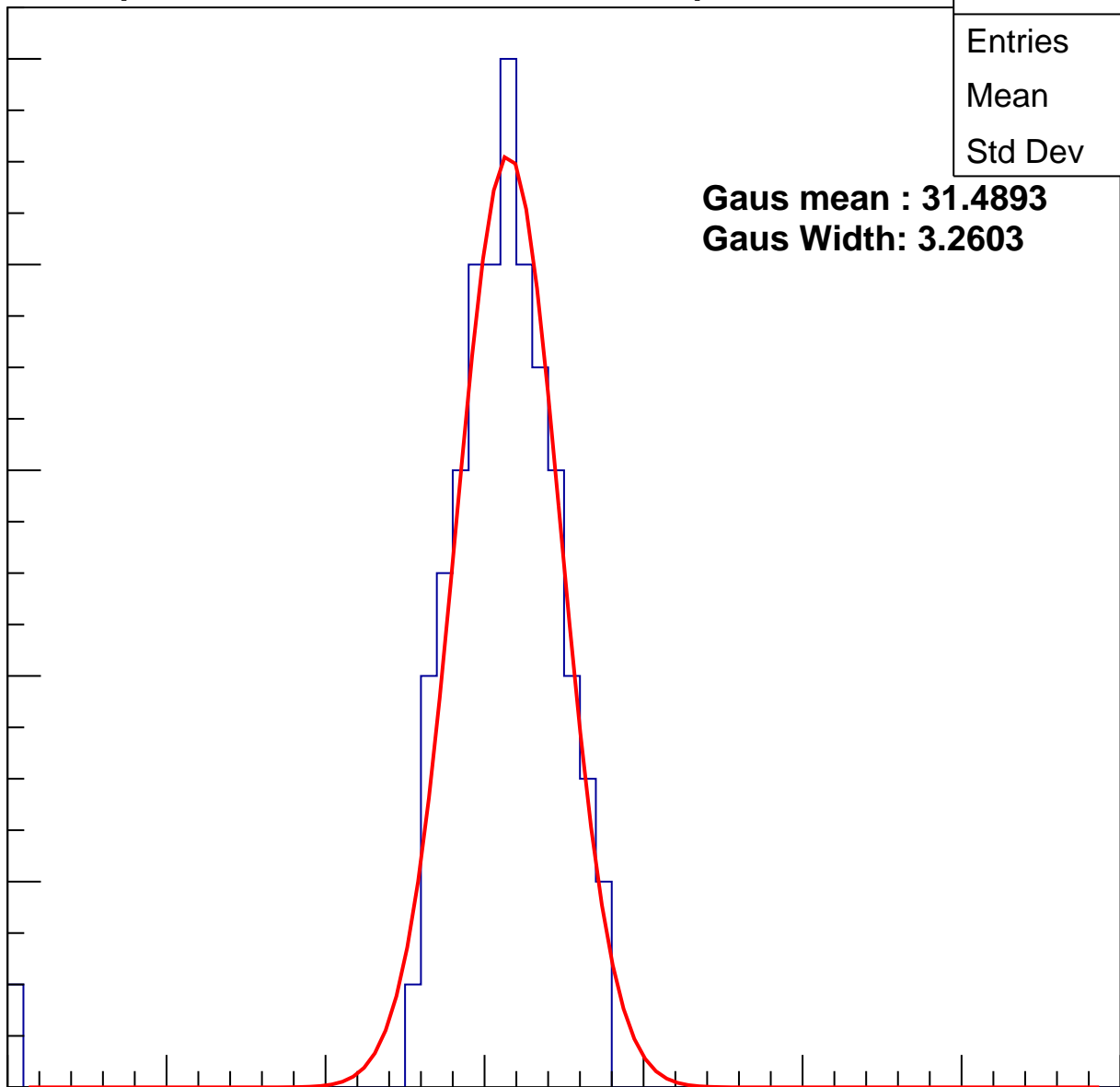
**Gaus Width: 3.2603**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U6-ch118, adc1

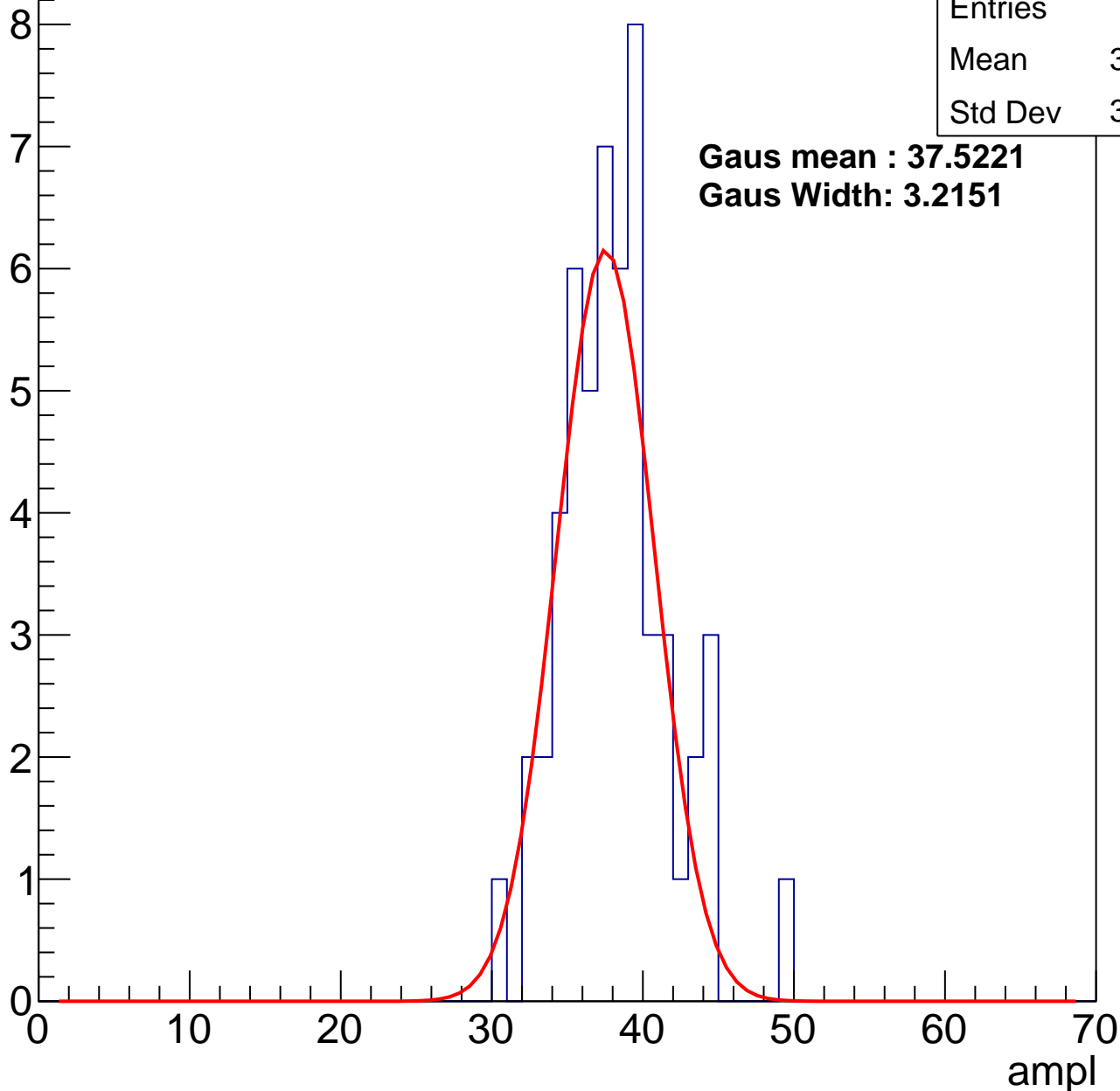
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	54
Mean	37.72
Std Dev	3.519

**Gaus mean : 37.5221**

**Gaus Width: 3.2151**



# B1L003S, U6-ch118, adc2

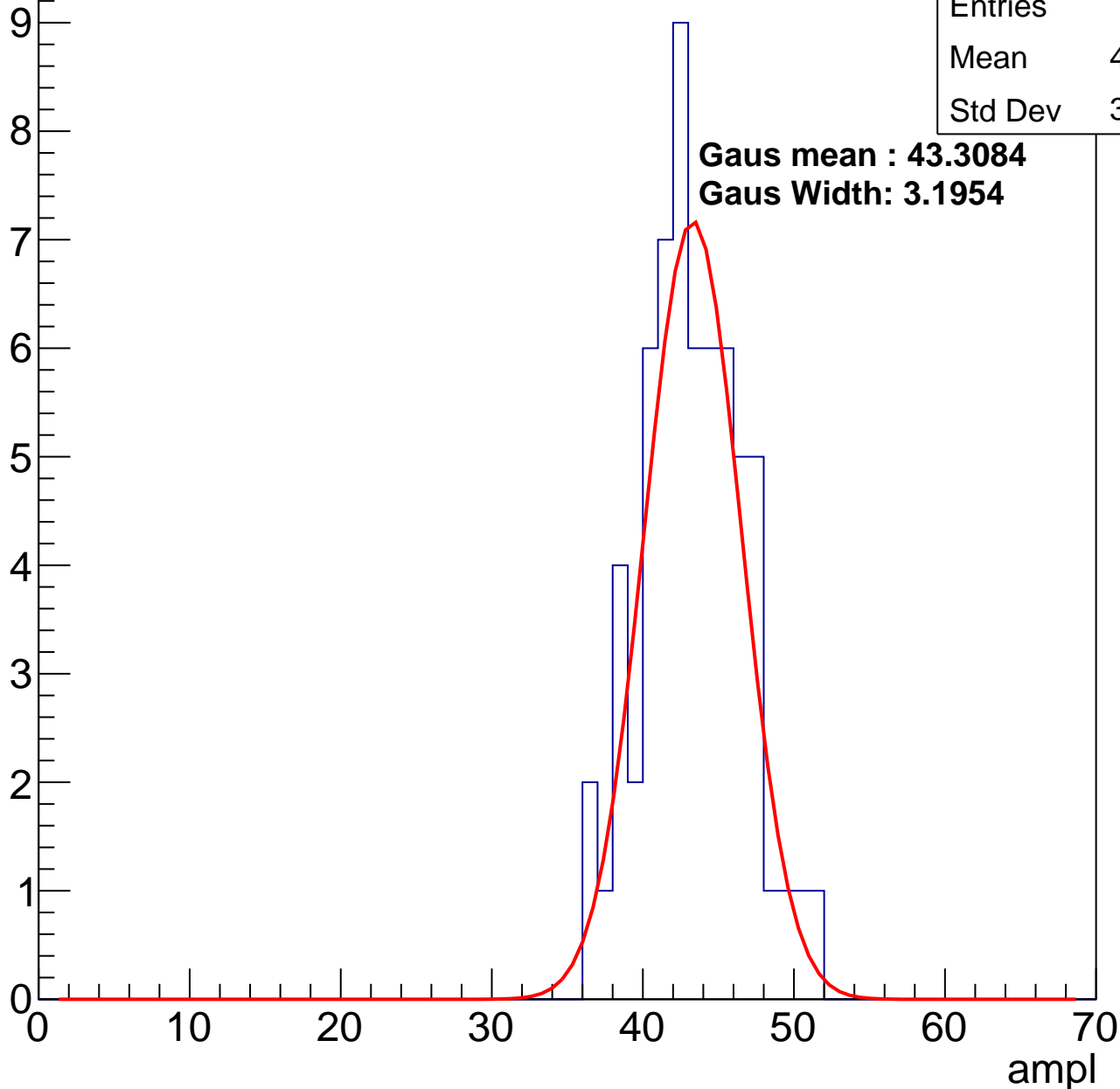
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	42.84
Std Dev	3.296

**Gaus mean : 43.3084**

**Gaus Width: 3.1954**

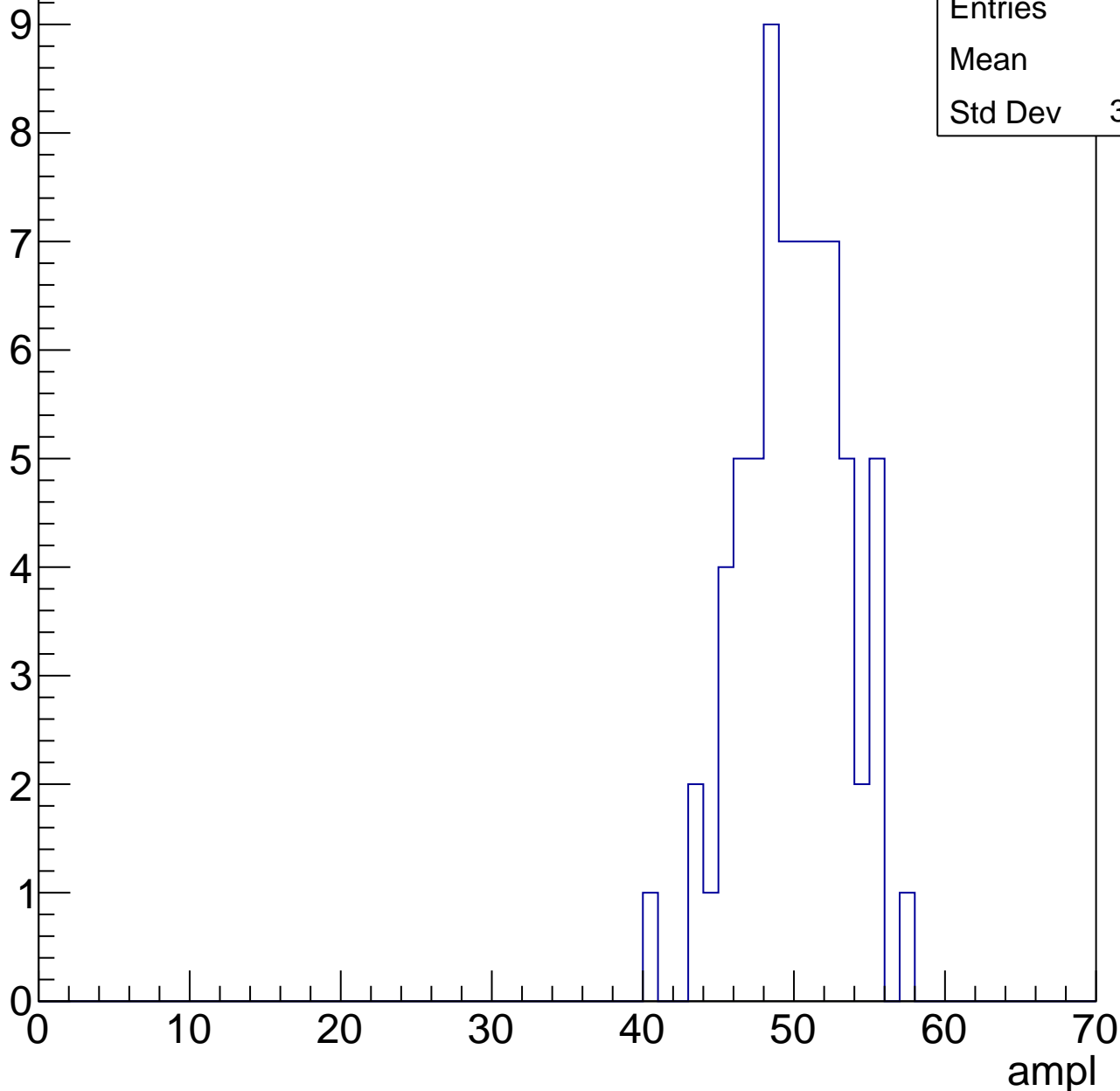


# B1L003S, U6-ch118, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	49.5
Std Dev	3.367

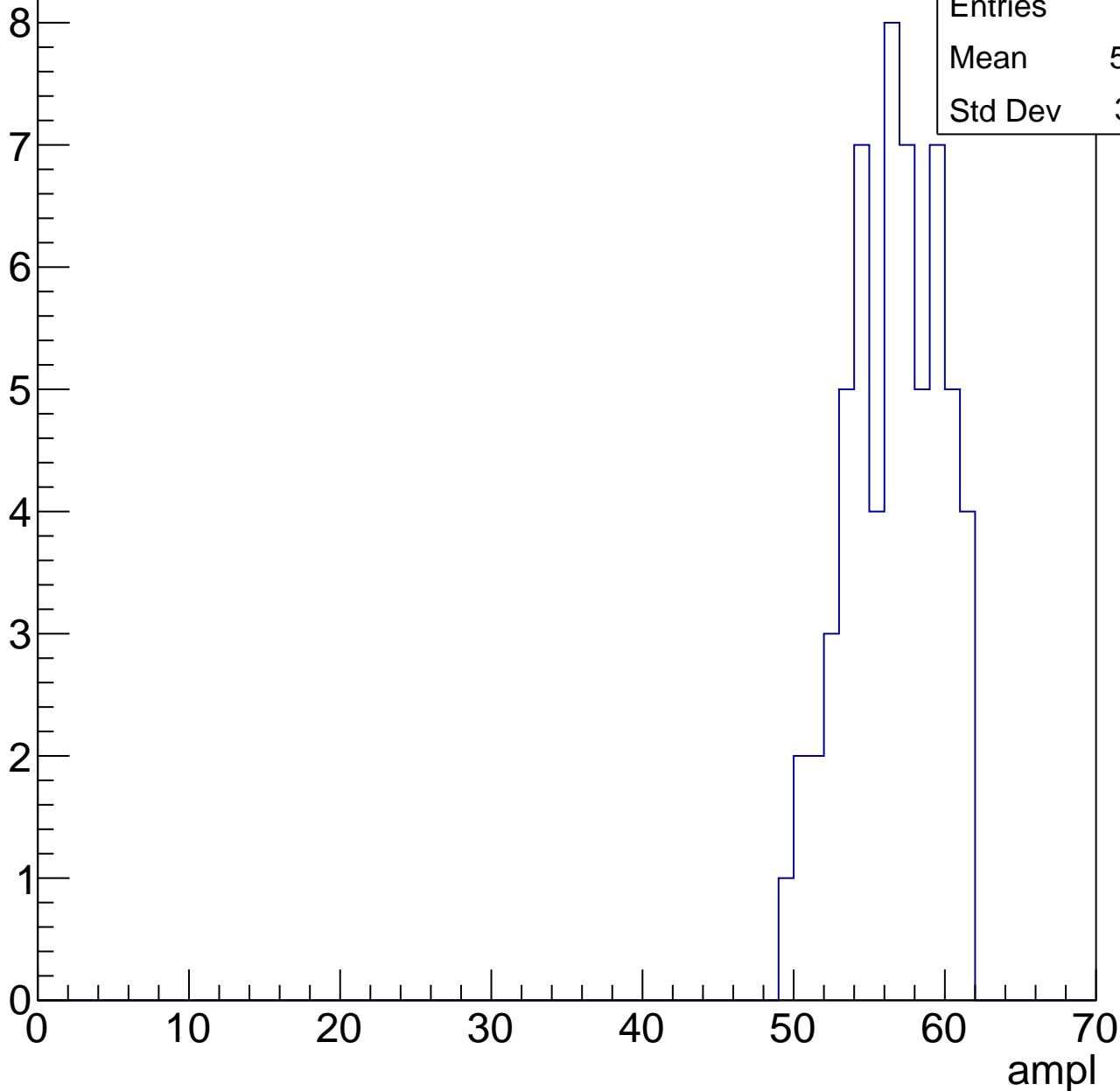


# B1L003S, U6-ch118, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	56.07
Std Dev	3.071

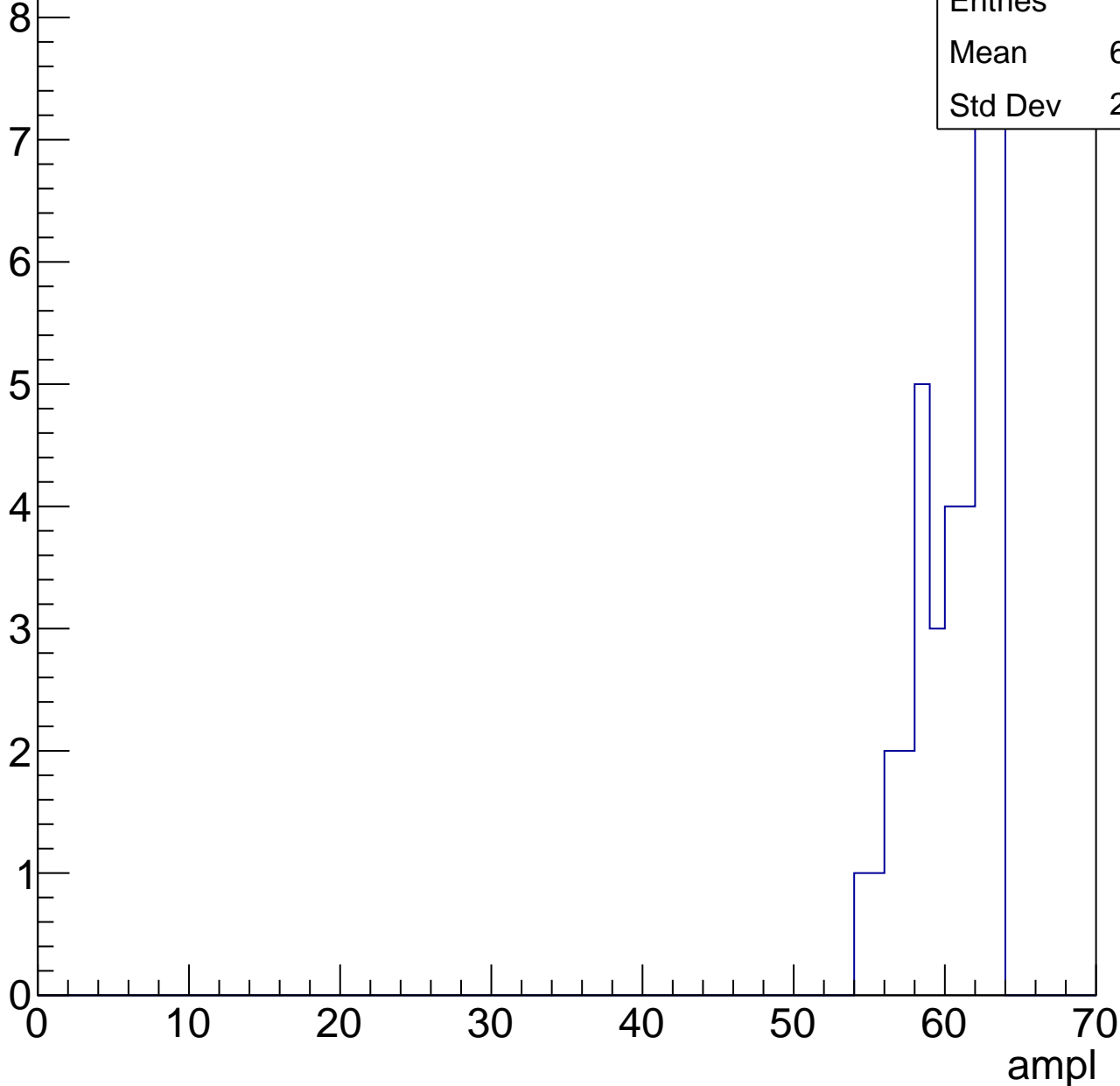


# B1L003S, U6-ch118, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	38
Mean	60.16
Std Dev	2.519



# B1L003S, U6-ch118, adc6

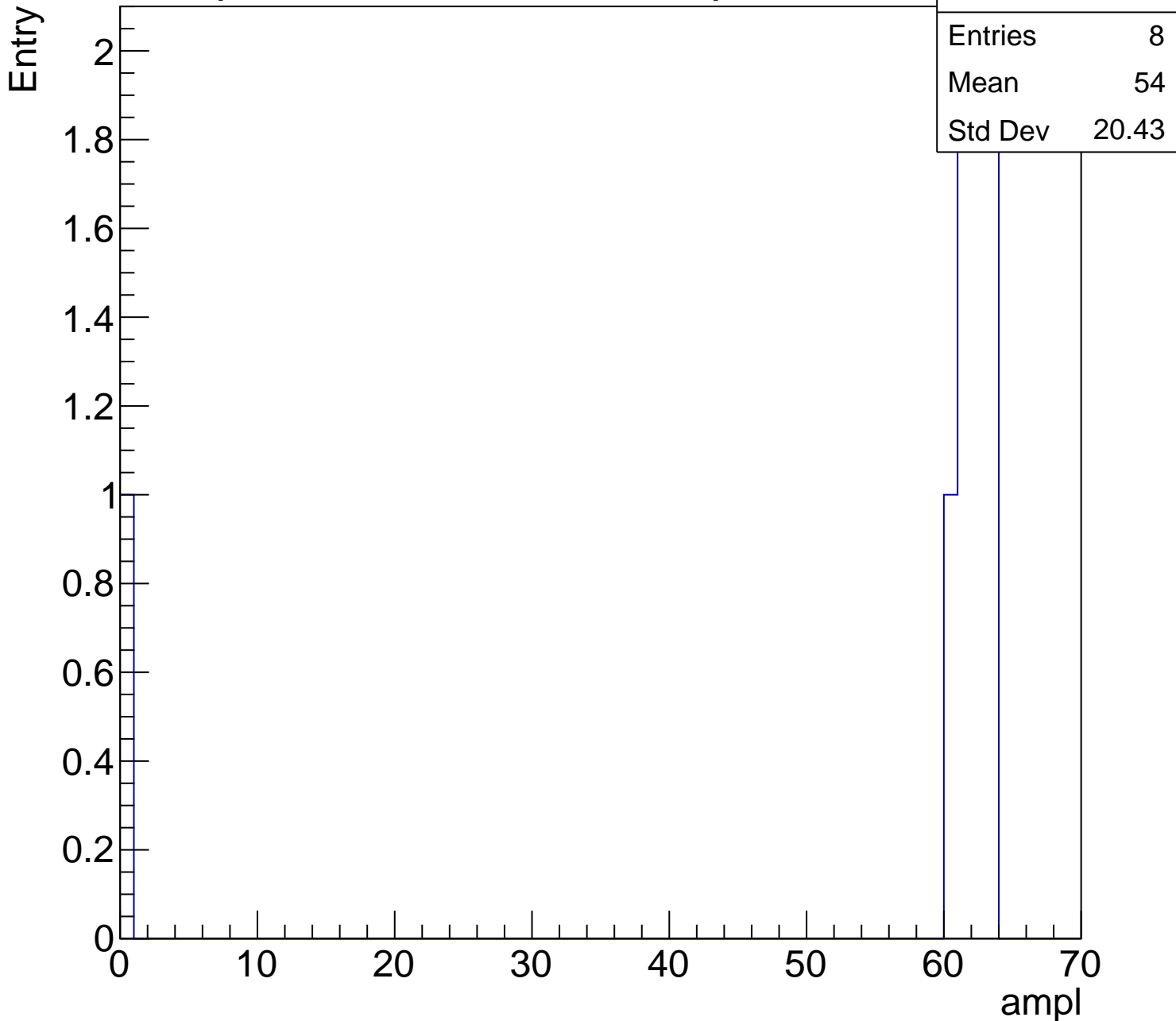
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	8
Mean	54
Std Dev	20.43

ampl

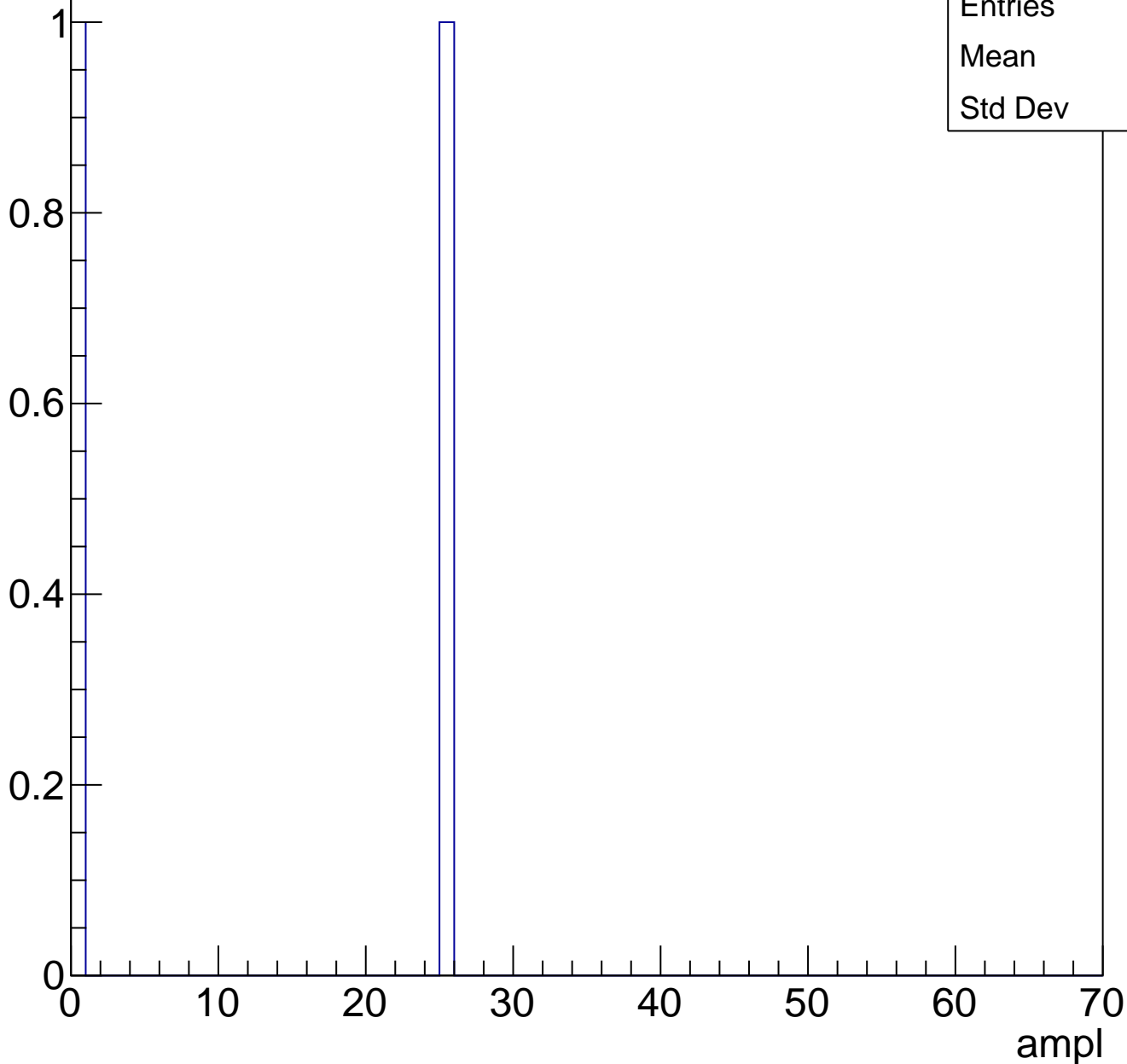




# B1L003S, U6-ch118, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch119, adc0

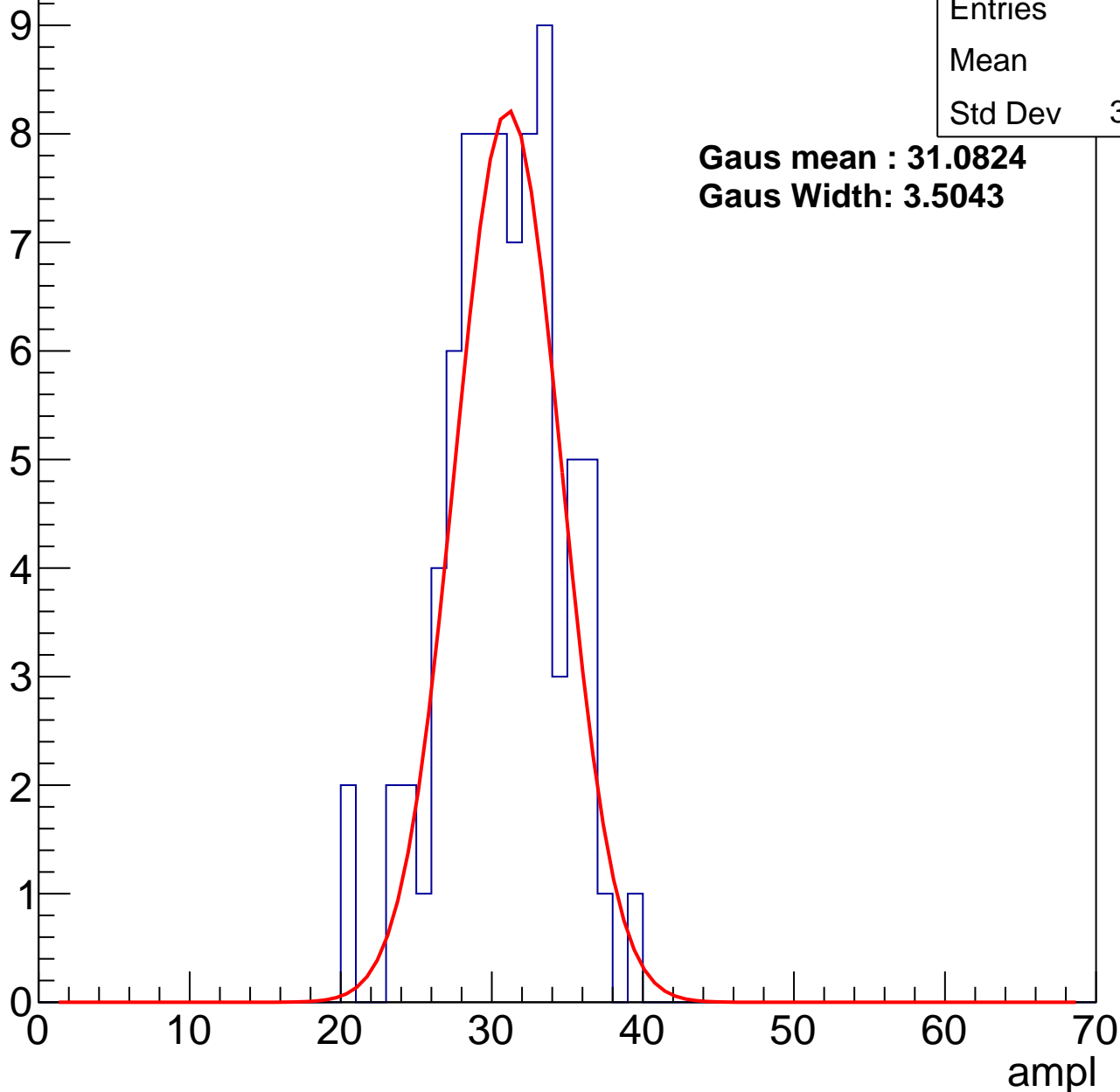
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	80
Mean	30.3
Std Dev	3.789

**Gaus mean : 31.0824**

**Gaus Width: 3.5043**



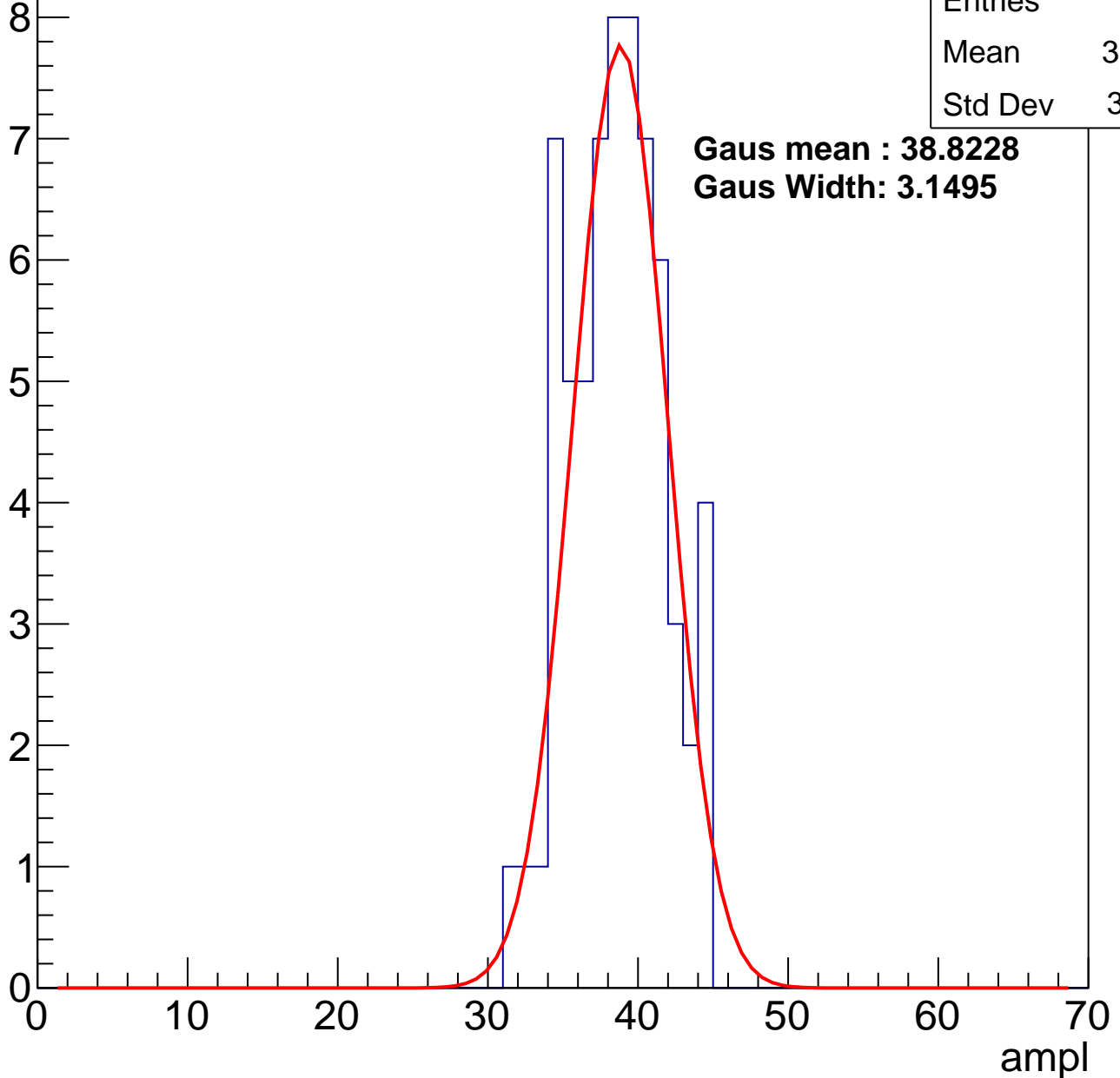
# B1L003S, U6-ch119, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	38.12
Std Dev	3.101

**Gaus mean : 38.8228**  
**Gaus Width: 3.1495**



# B1L003S, U6-ch119, adc2

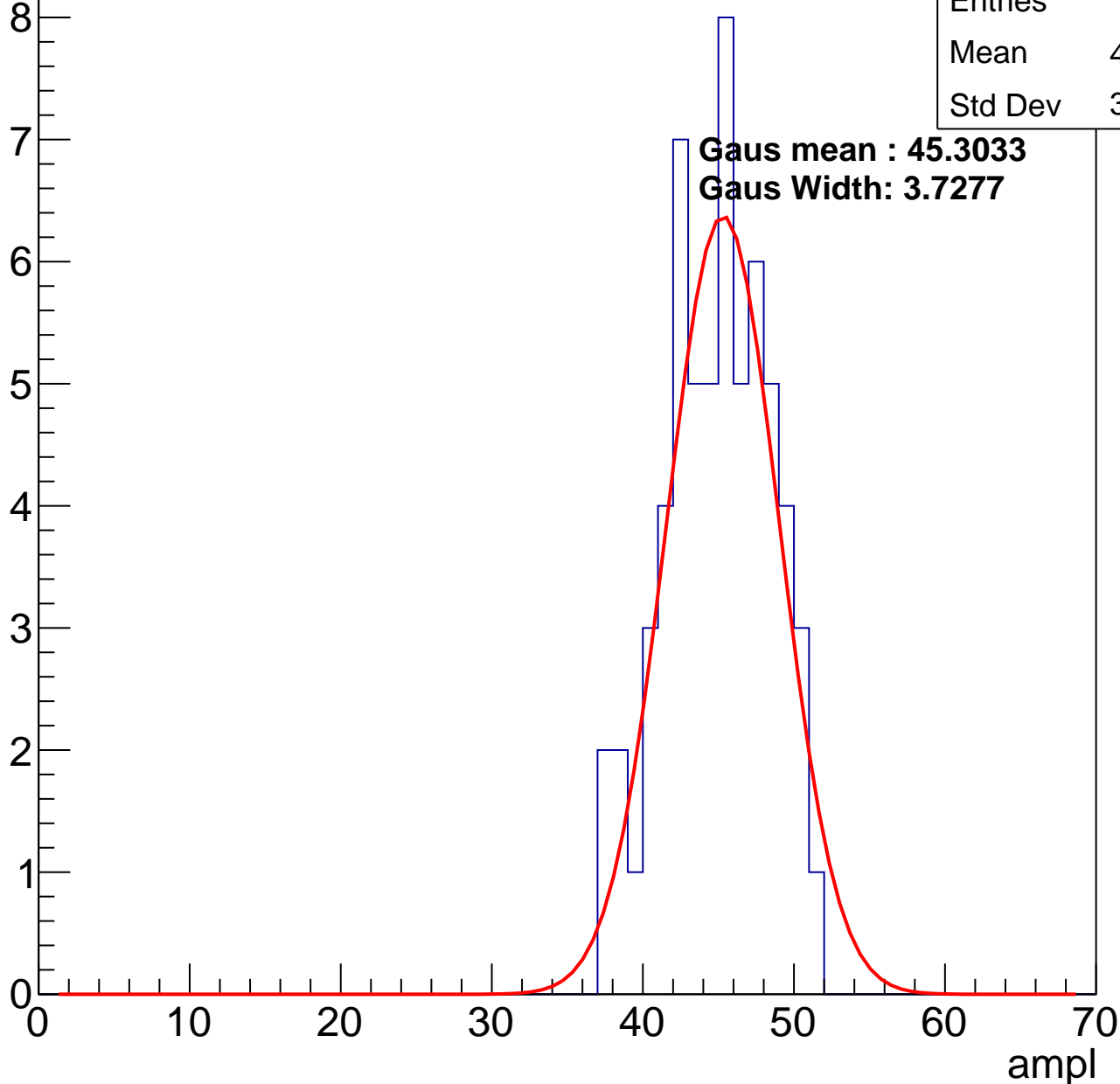
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	44.44
Std Dev	3.433

**Gaus mean : 45.3033**

**Gaus Width: 3.7277**

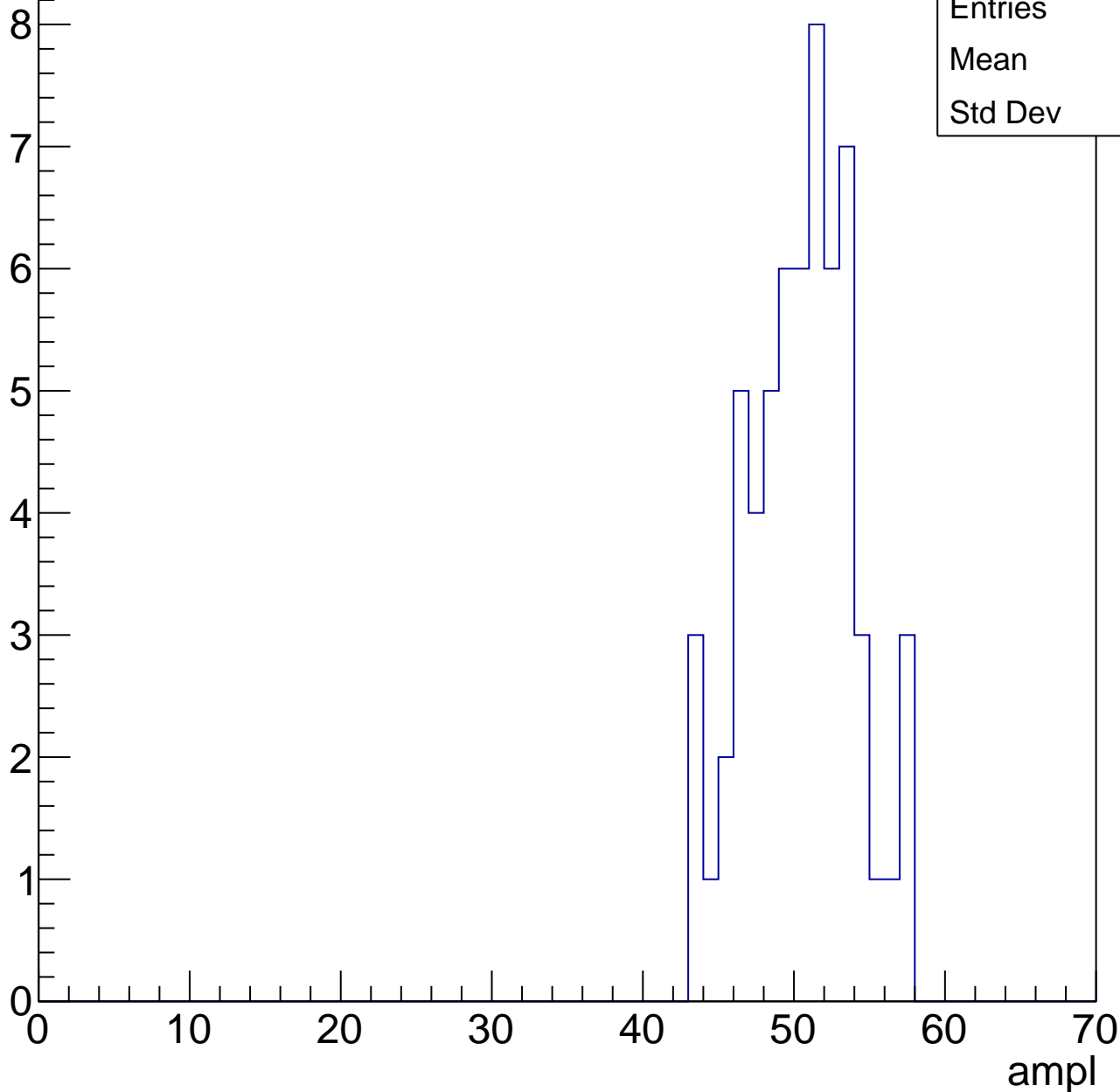


# B1L003S, U6-ch119, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	50
Std Dev	3.45

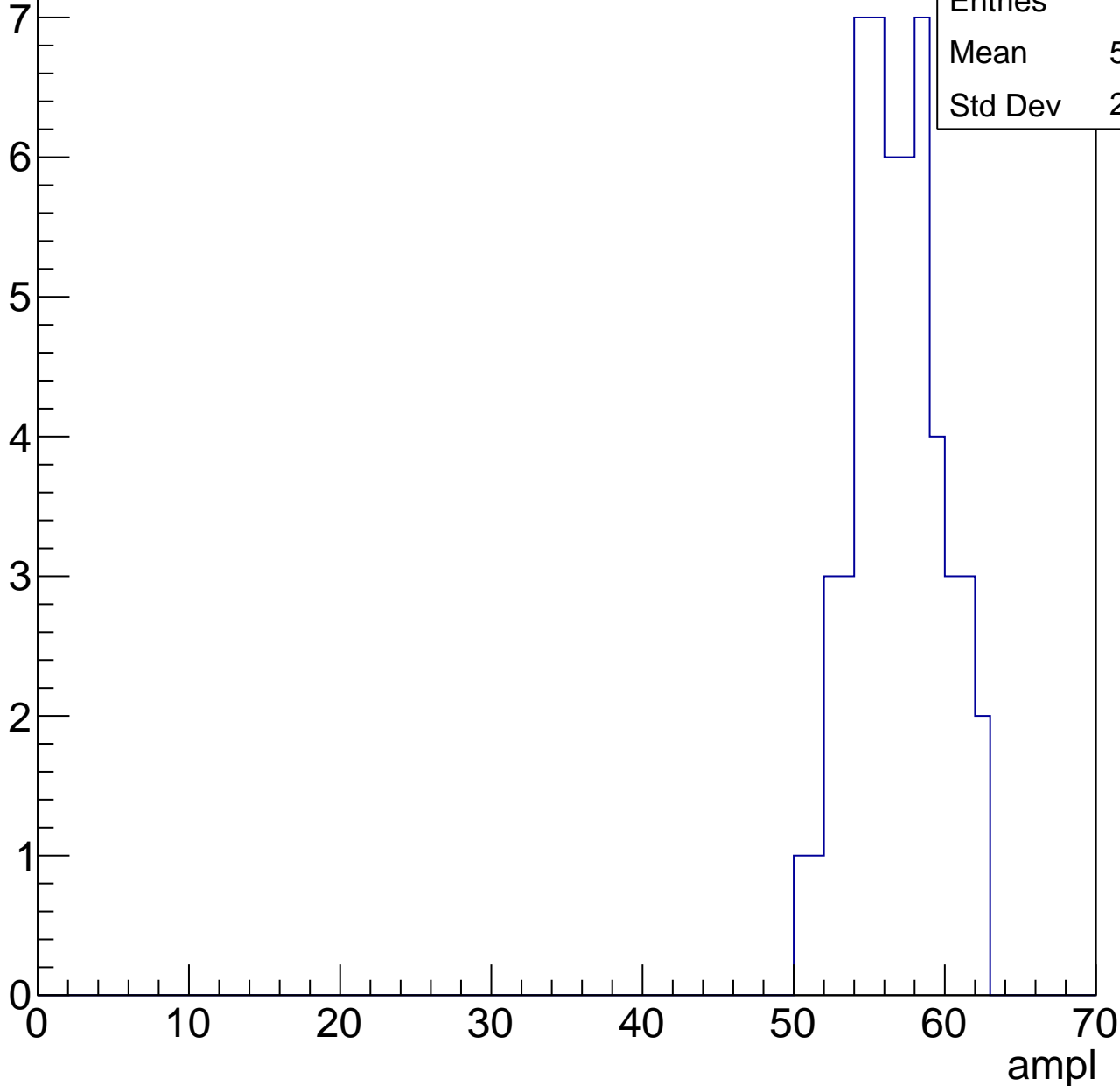


# B1L003S, U6-ch119, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	56.34
Std Dev	2.848

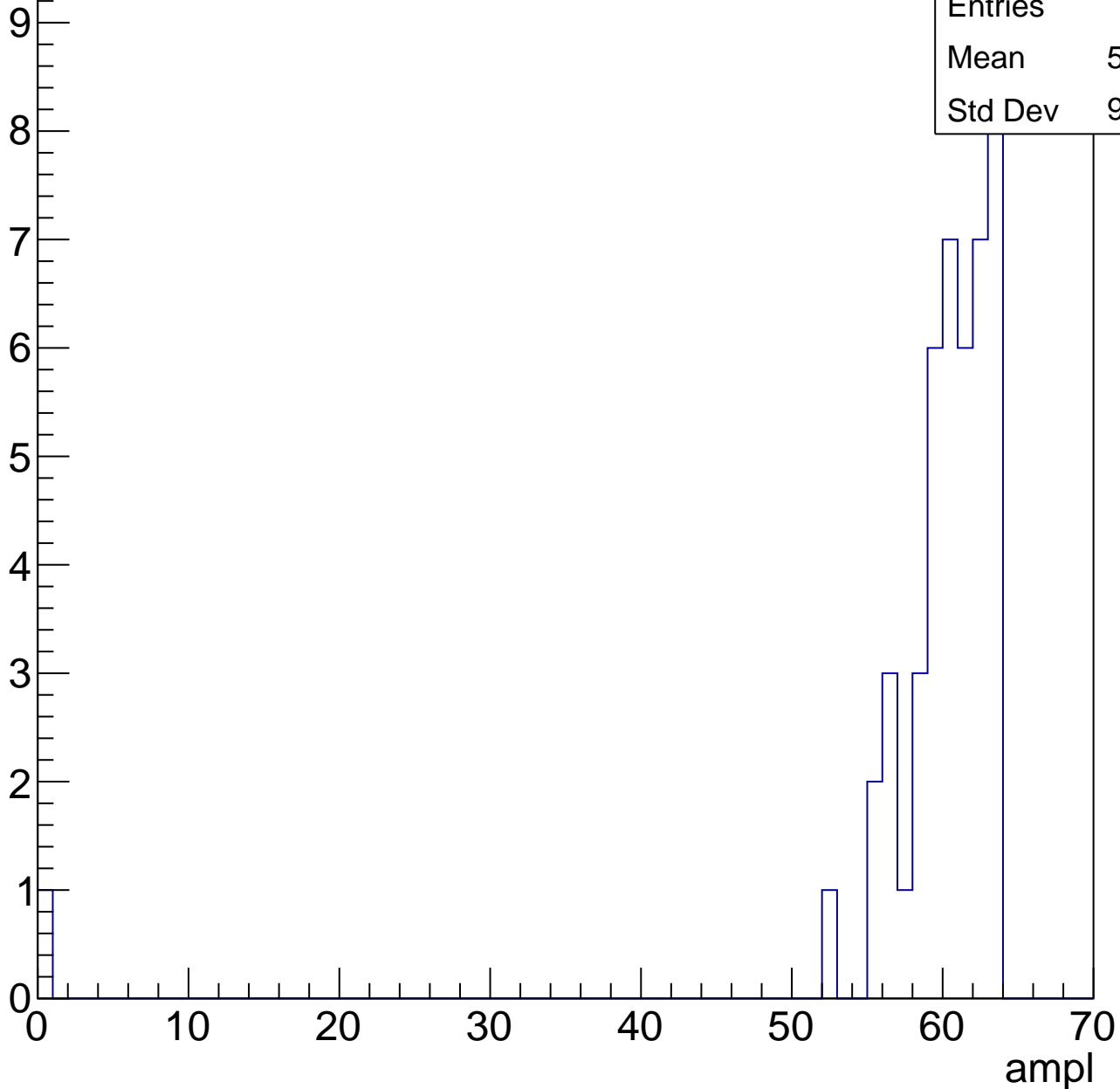


# B1L003S, U6-ch119, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	46
Mean	58.74
Std Dev	9.126



# B1L003S, U6-ch119, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch119, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U6-ch120, adc0

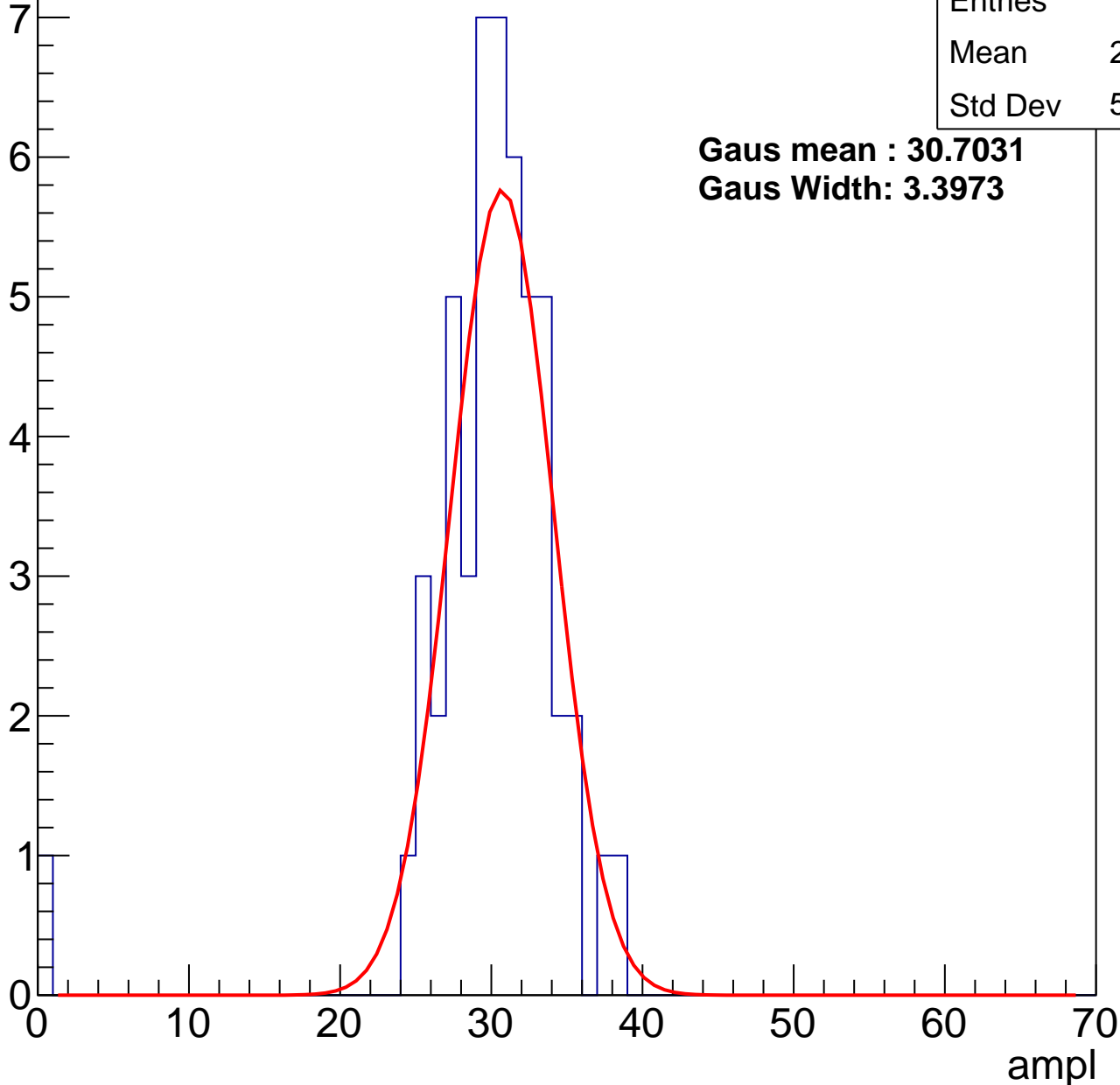
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	51
Mean	29.55
Std Dev	5.169

**Gaus mean : 30.7031**

**Gaus Width: 3.3973**



# B1L003S, U6-ch120, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	79
Mean	37.13
Std Dev	3.425

**Gaus mean : 37.1976**

**Gaus Width: 3.8530**

Entry

10

8

6

4

2

0

0

10

20

30

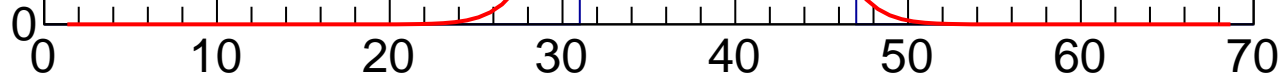
40

50

60

70

ampl



# B1L003S, U6-ch120, adc2

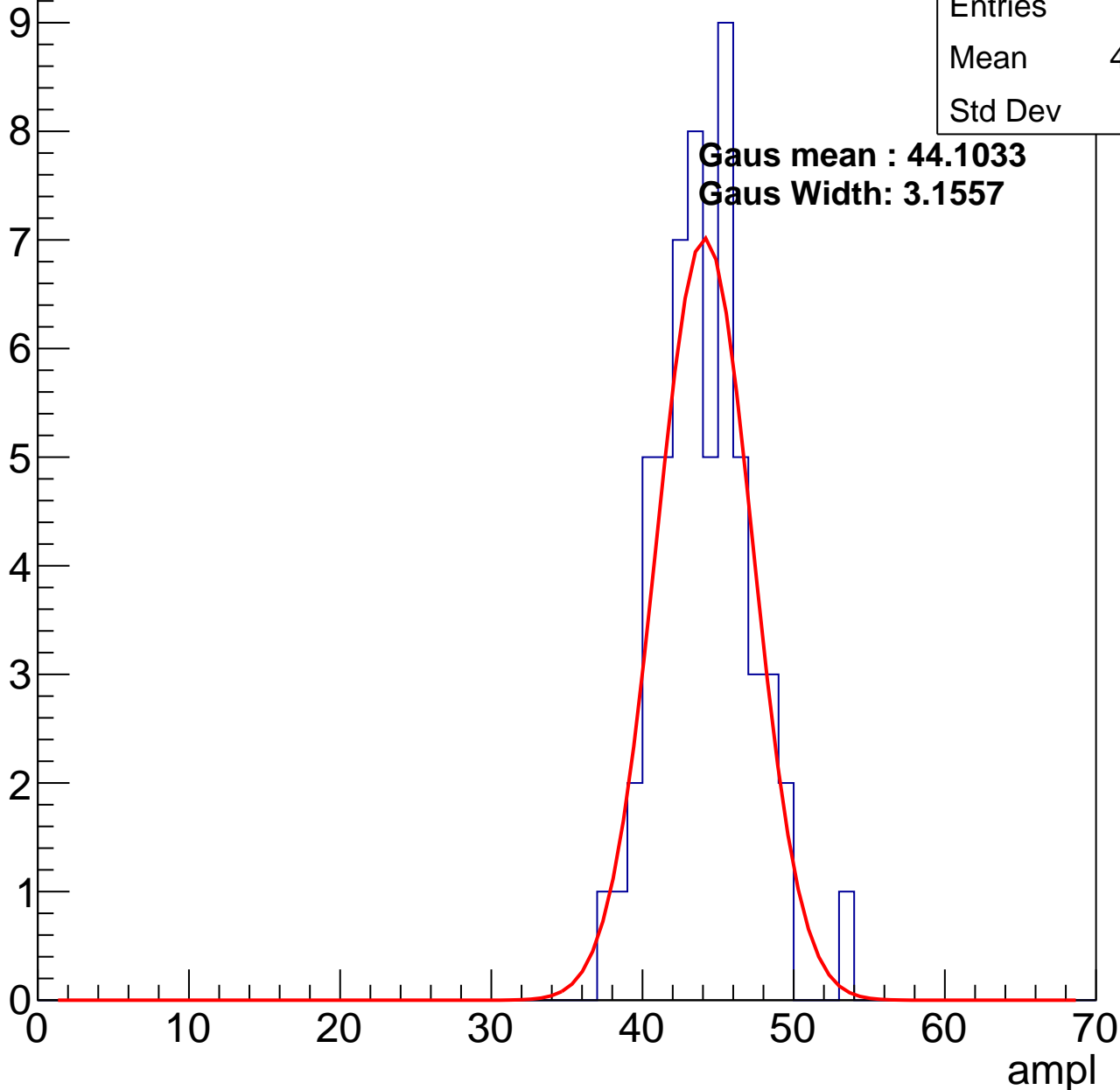
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	43.63
Std Dev	3.03

**Gaus mean : 44.1033**

**Gaus Width: 3.1557**

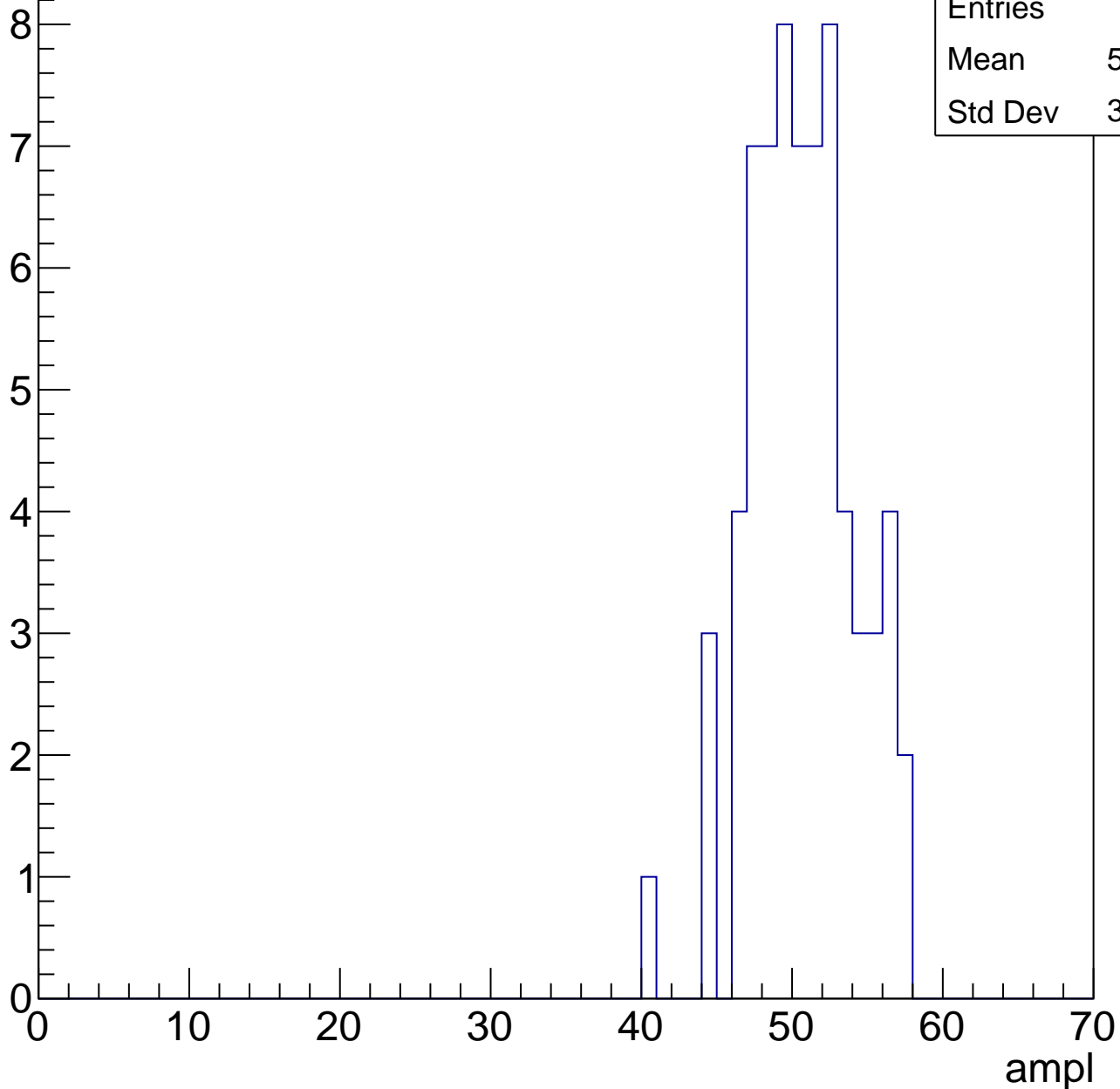


# B1L003S, U6-ch120, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	50.19
Std Dev	3.448

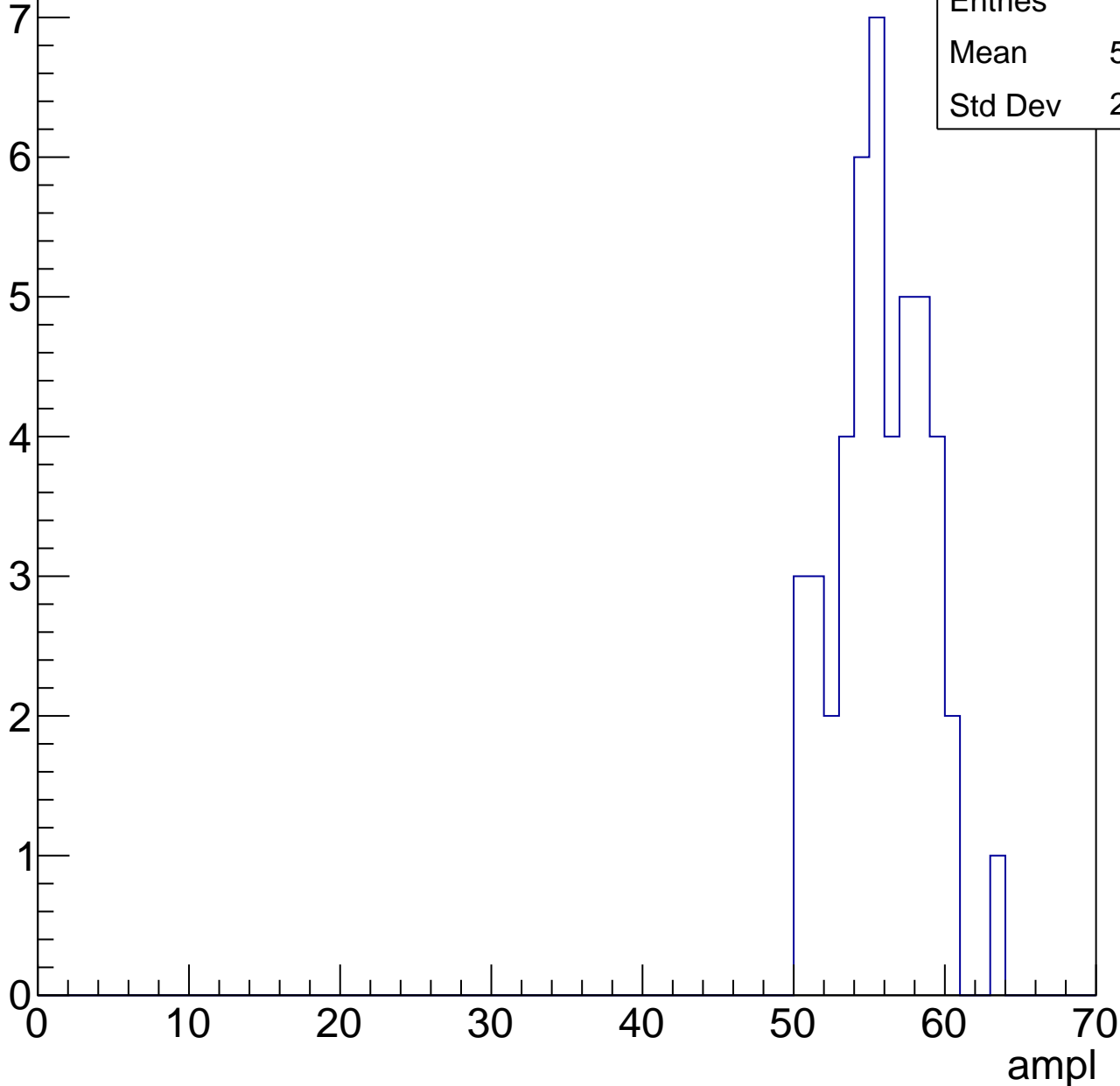


# B1L003S, U6-ch120, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	46
Mean	55.35
Std Dev	2.965

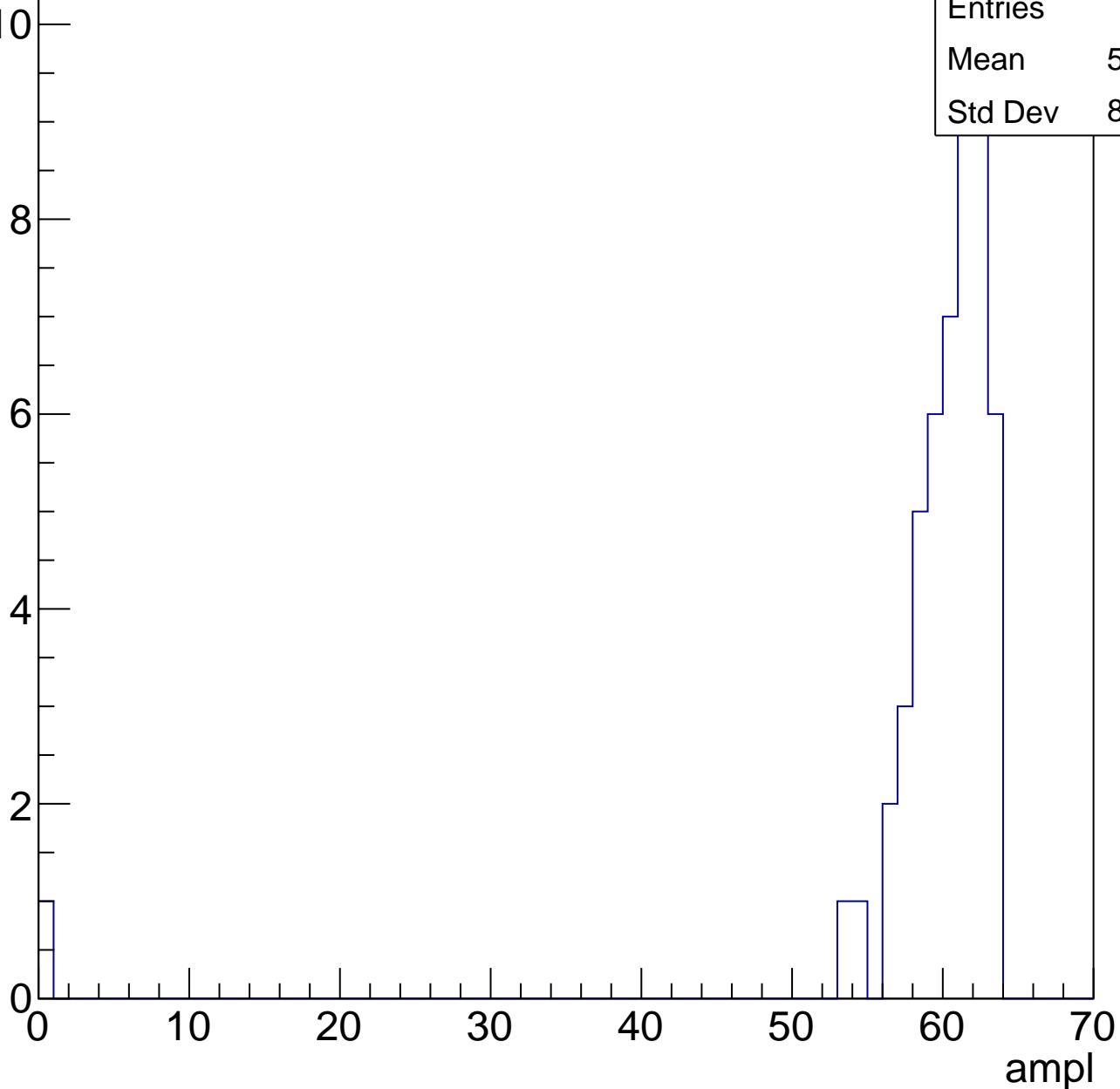


# B1L003S, U6-ch120, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	52
Mean	58.88
Std Dev	8.559



# B1L003S, U6-ch120, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch120, adc7

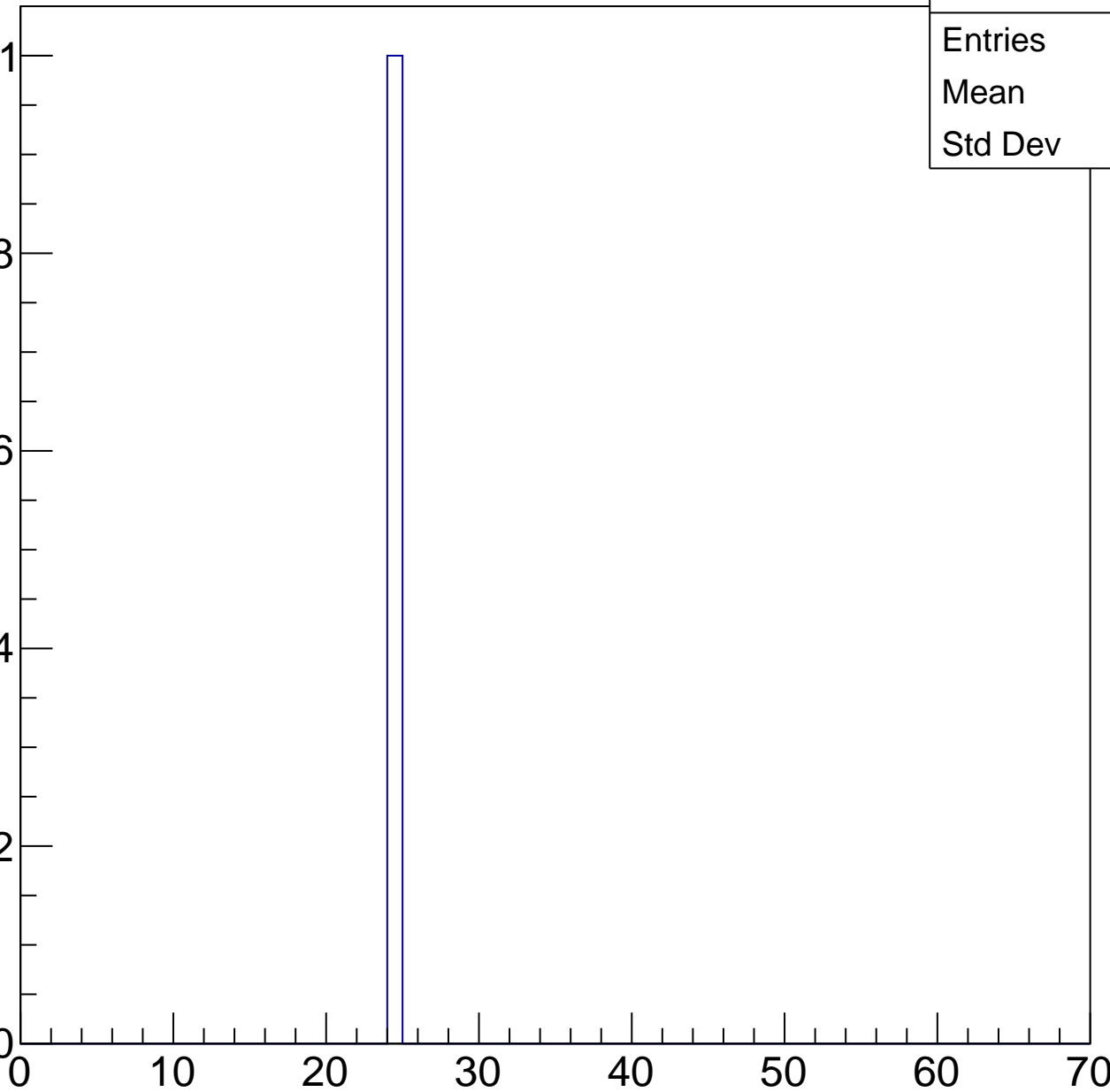
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	24
Std Dev	0

ampl



# B1L003S, U6-ch121, adc0

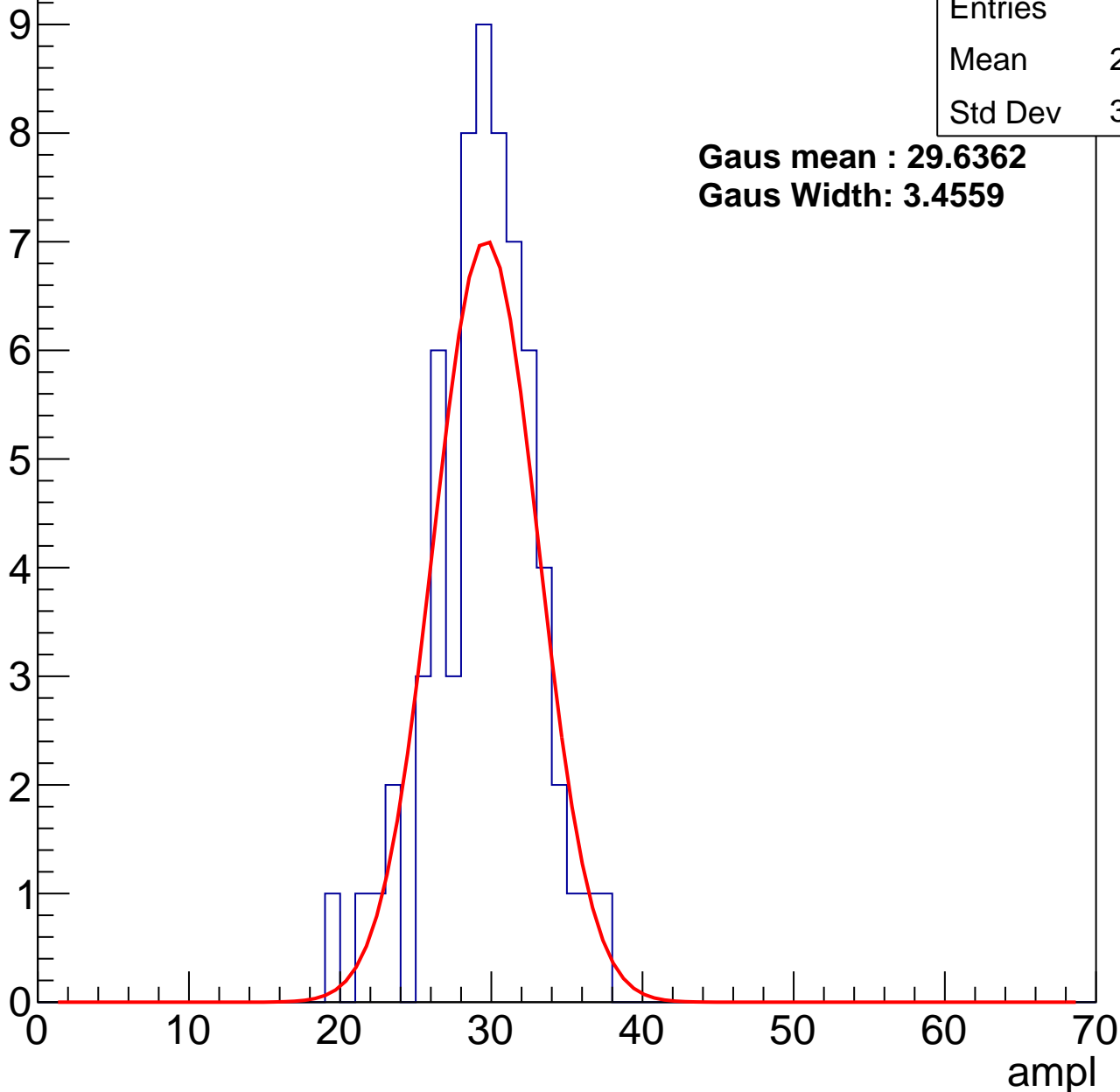
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	29.09
Std Dev	3.445

**Gaus mean : 29.6362**

**Gaus Width: 3.4559**



# B1L003S, U6-ch121, adc1

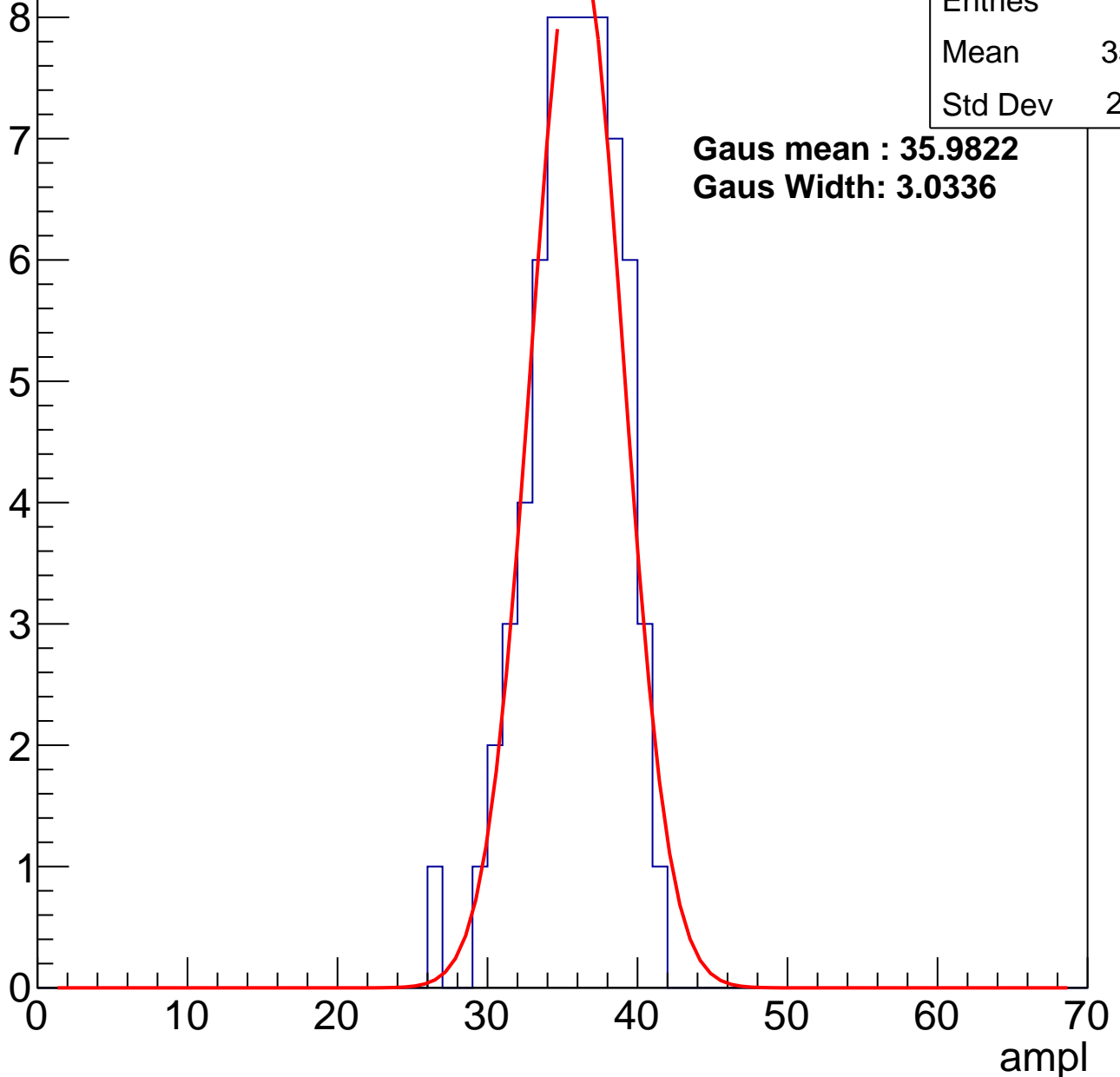
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	35.32
Std Dev	2.981

**Gaus mean : 35.9822**

**Gaus Width: 3.0336**



# B1L003S, U6-ch121, adc2

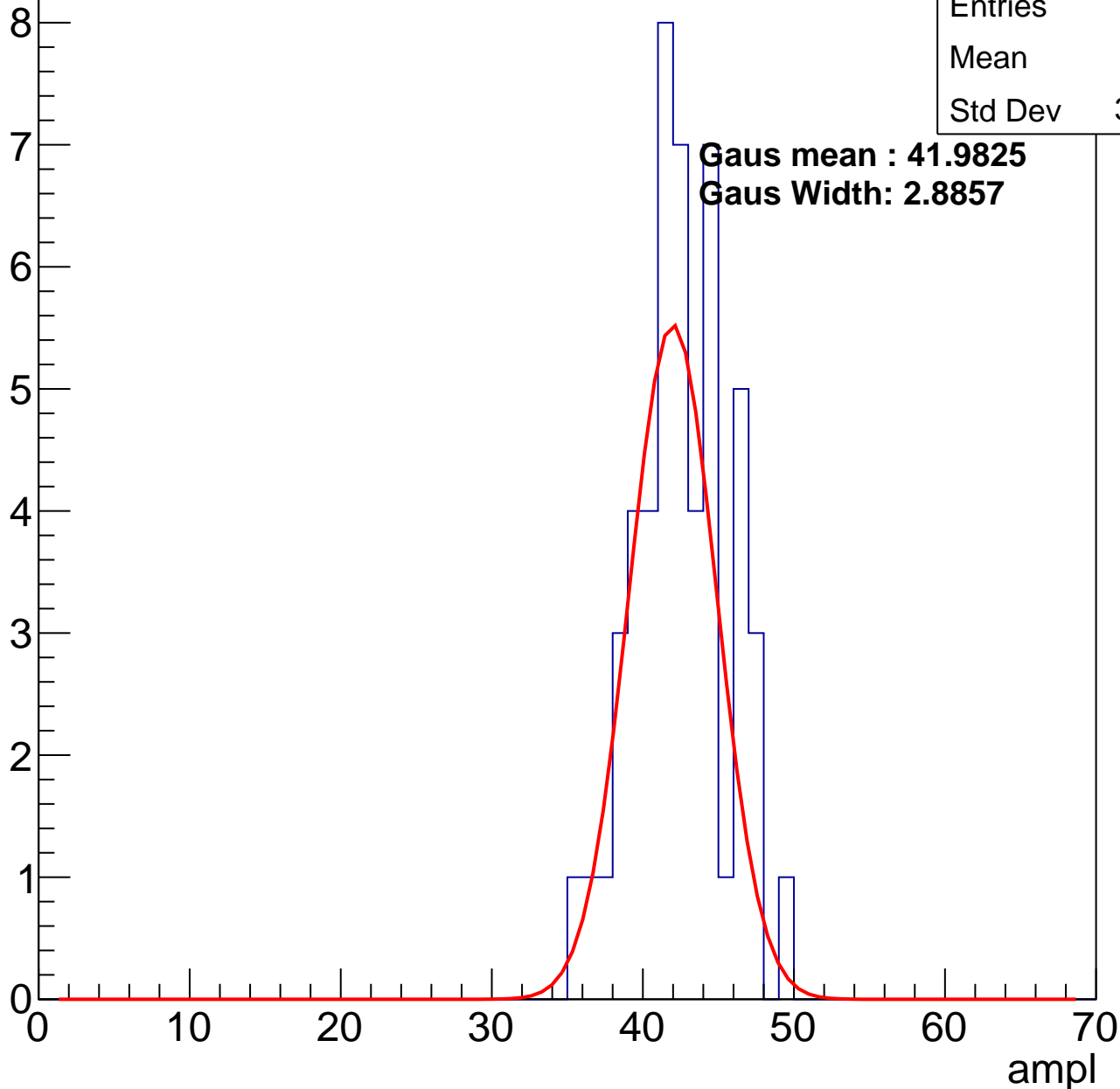
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	50
Mean	42.1
Std Dev	3.041

**Gaus mean : 41.9825**

**Gaus Width: 2.8857**

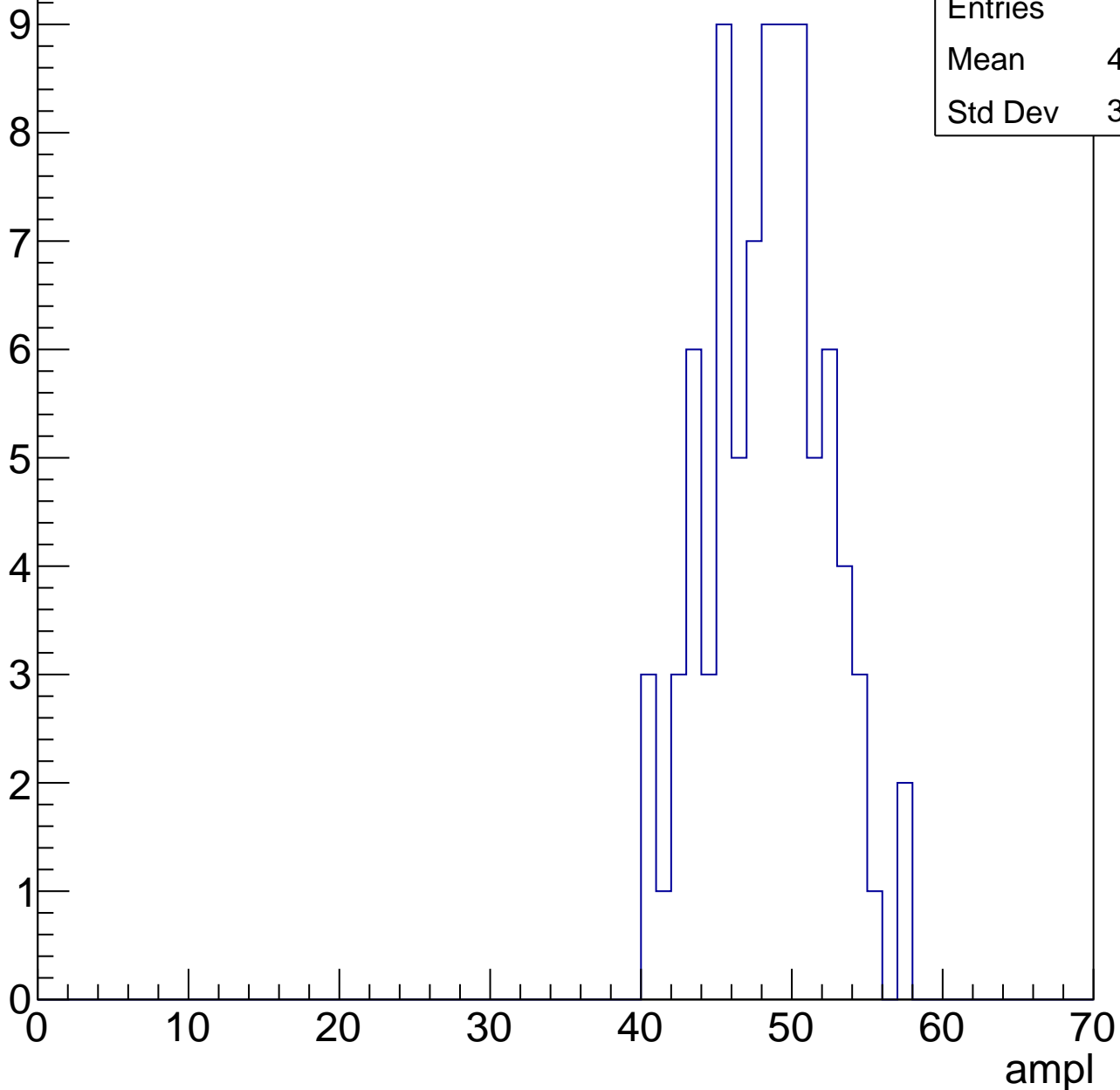


# B1L003S, U6-ch121, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

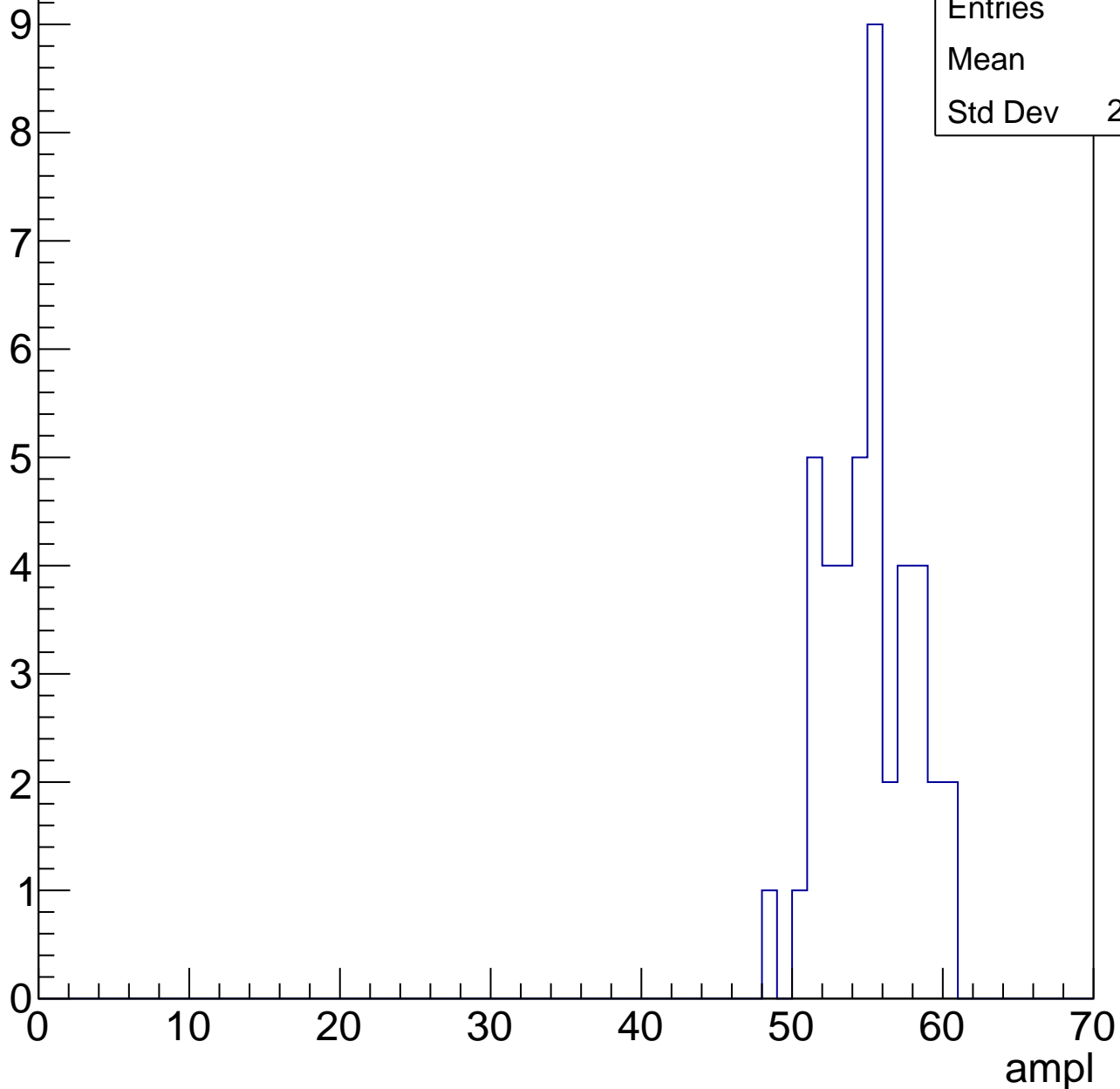
Entries	85
Mean	47.93
Std Dev	3.849



# B1L003S, U6-ch121, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



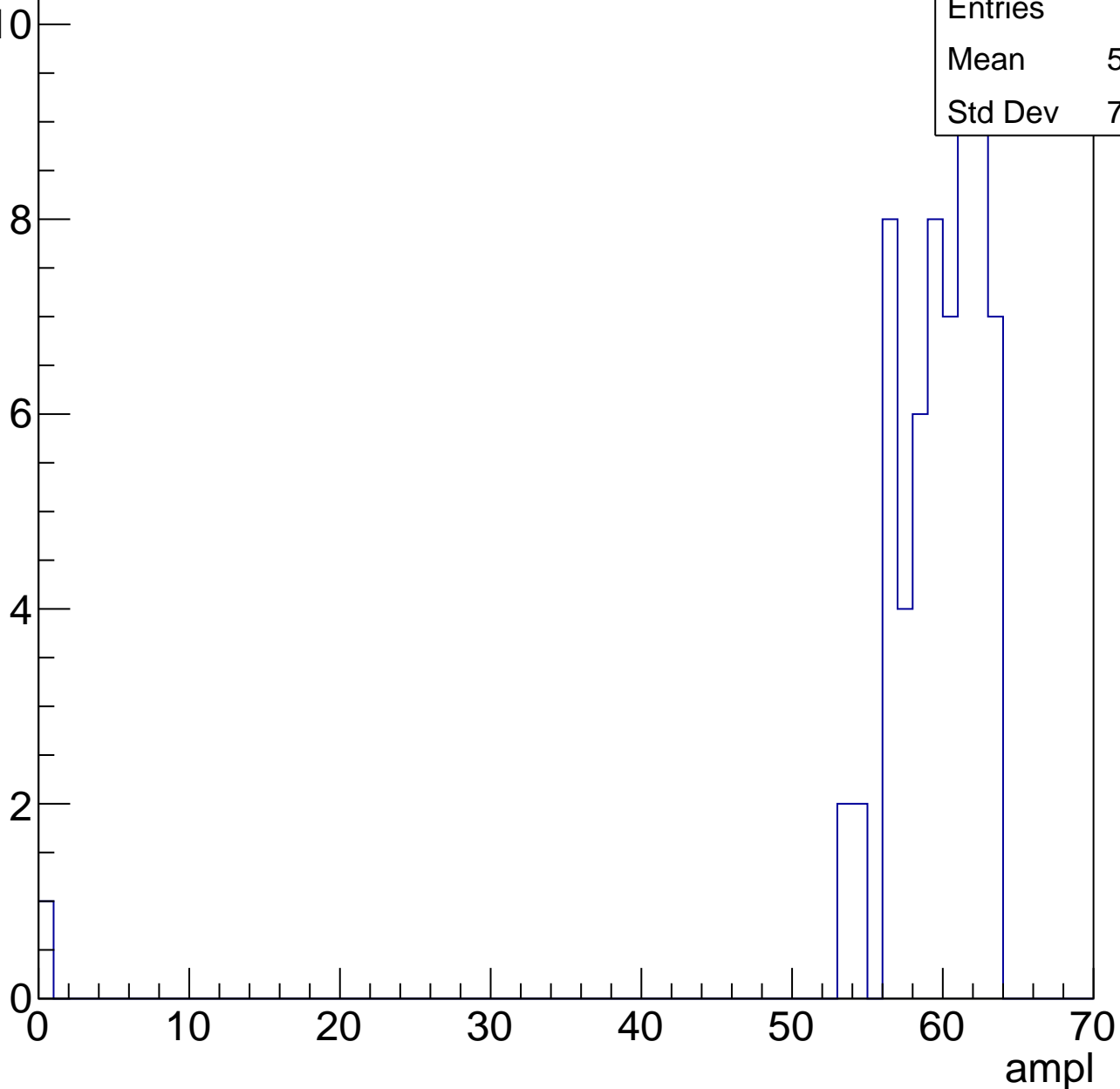
Entries	43
Mean	54.6
Std Dev	2.813

# B1L003S, U6-ch121, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	58.48
Std Dev	7.774



# B1L003S, U6-ch121, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch121, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch122, adc0

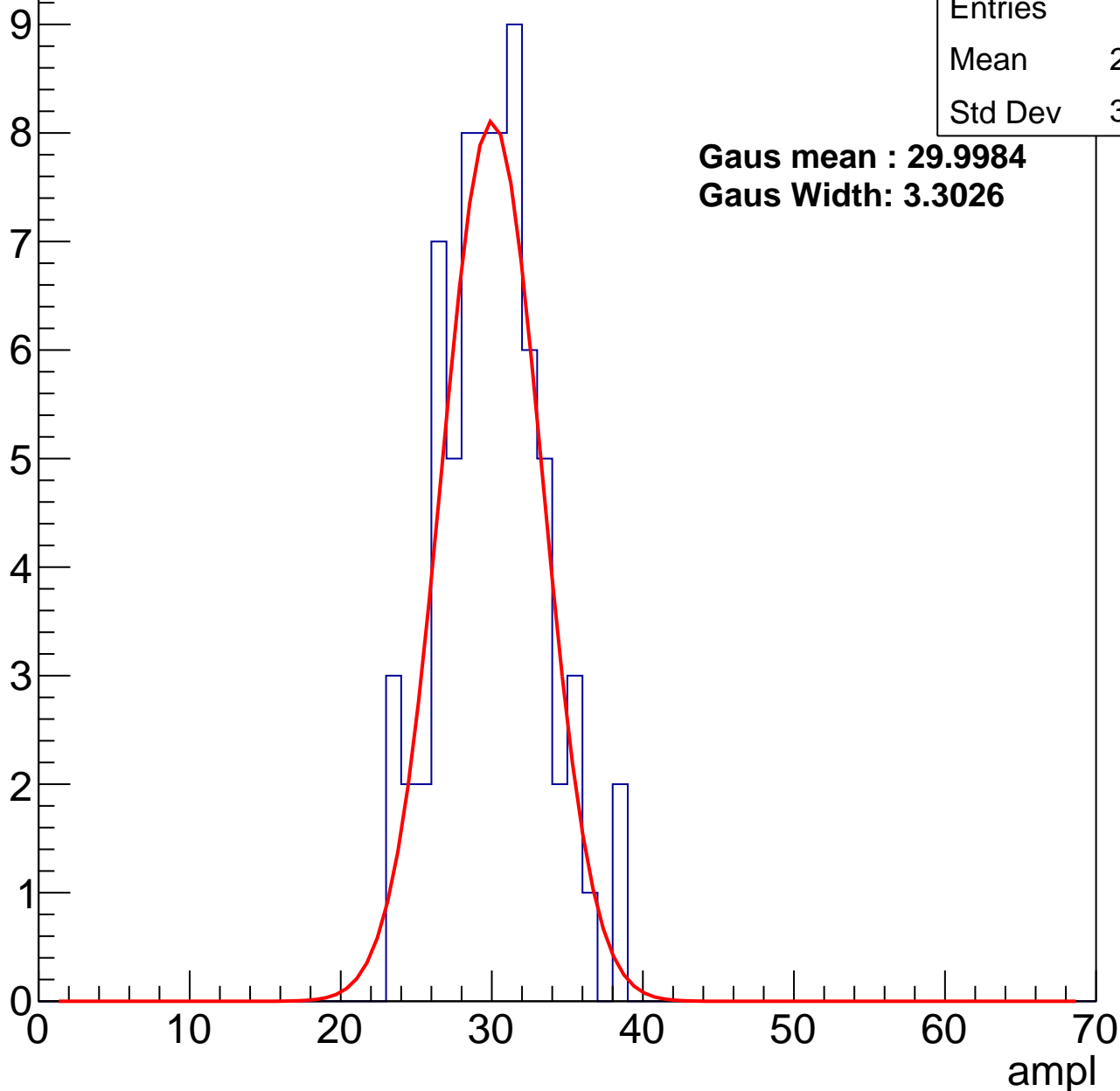
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	71
Mean	29.59
Std Dev	3.363

**Gaus mean : 29.9984**

**Gaus Width: 3.3026**



# B1L003S, U6-ch122, adc1

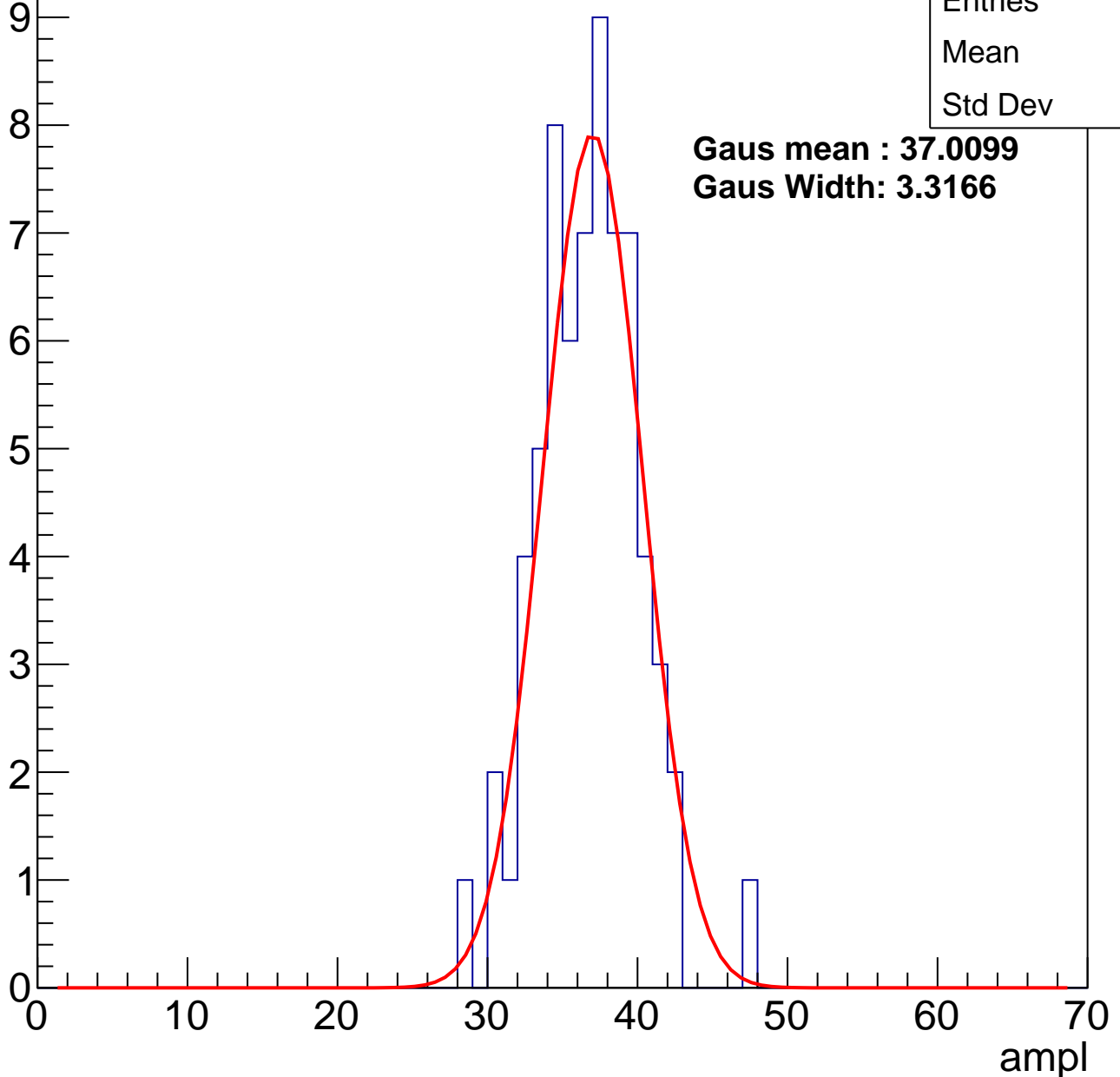
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	36.3
Std Dev	3.31

**Gaus mean : 37.0099**

**Gaus Width: 3.3166**



# B1L003S, U6-ch122, adc2

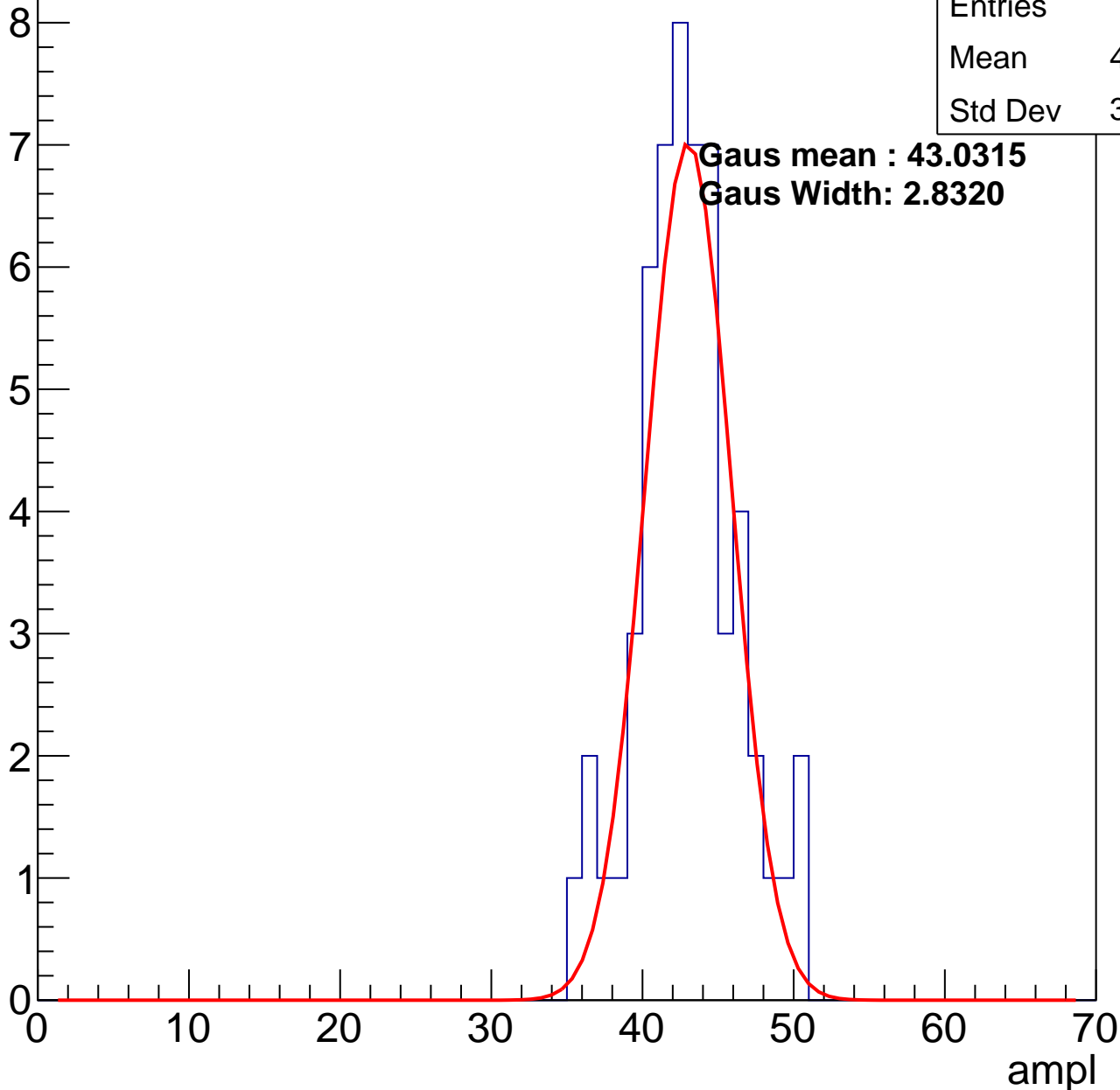
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	42.52
Std Dev	3.257

**Gaus mean : 43.0315**

**Gaus Width: 2.8320**

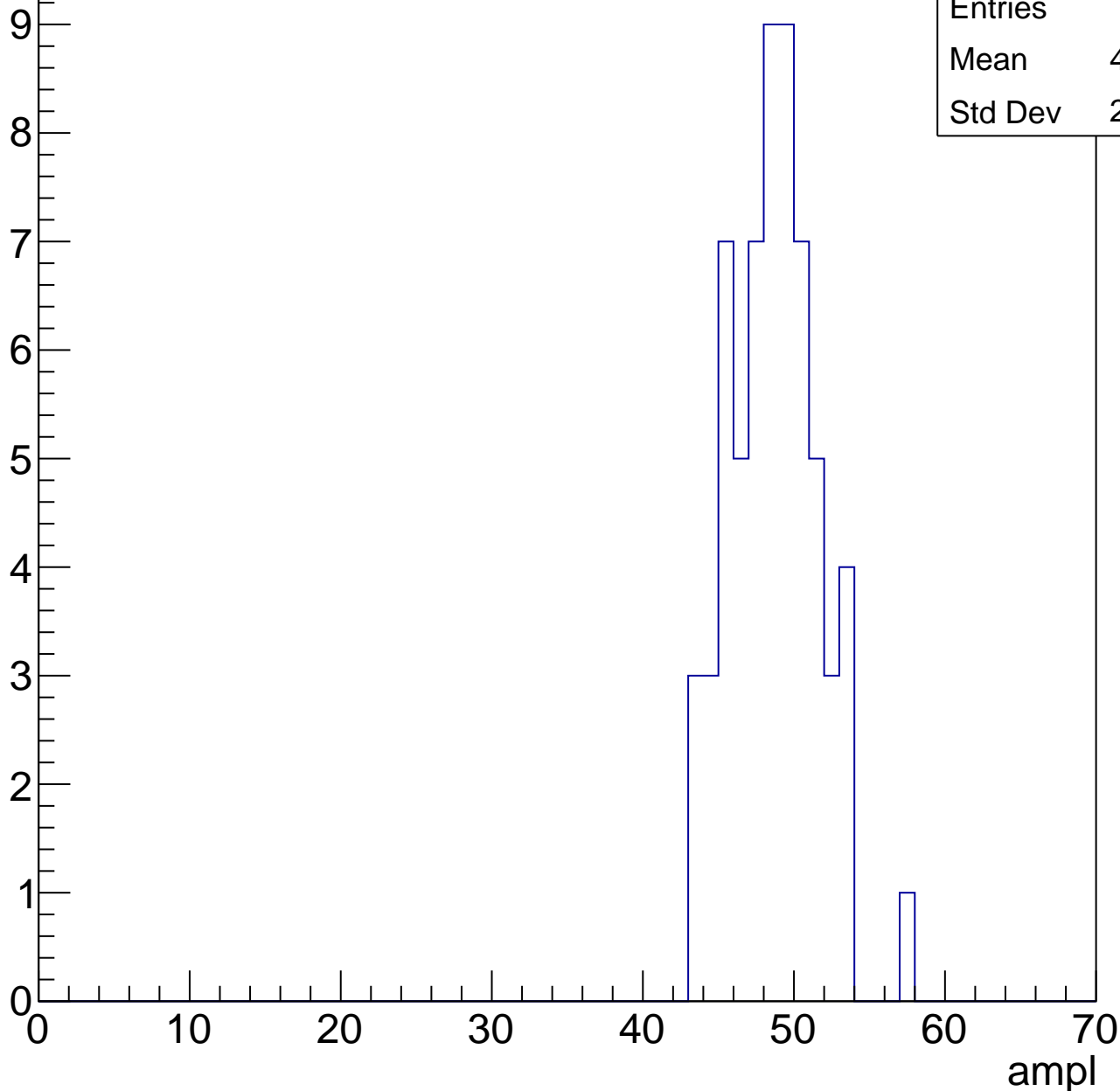


# B1L003S, U6-ch122, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	48.22
Std Dev	2.875

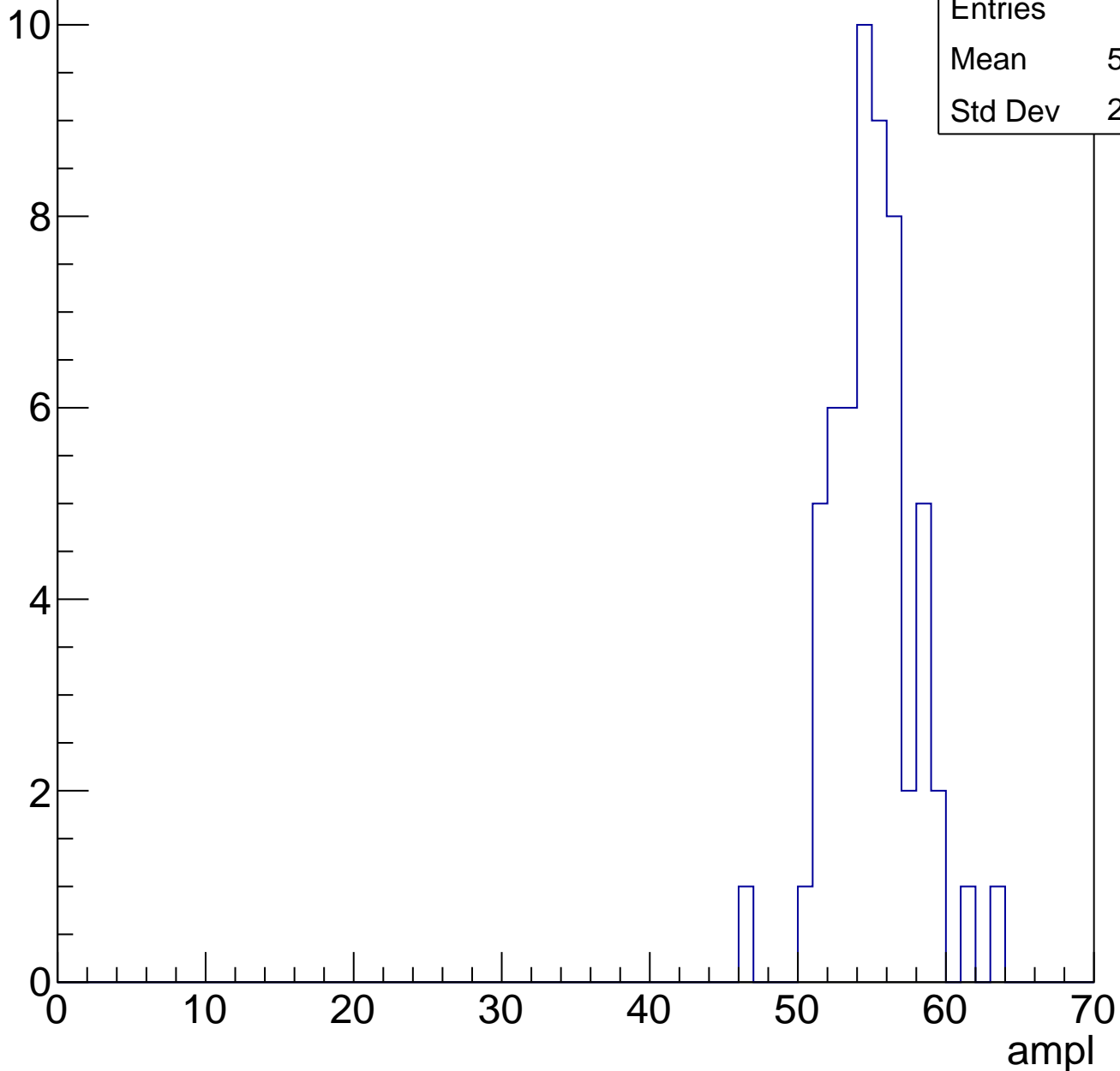


# B1L003S, U6-ch122, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	57
Mean	54.56
Std Dev	2.829

Entry

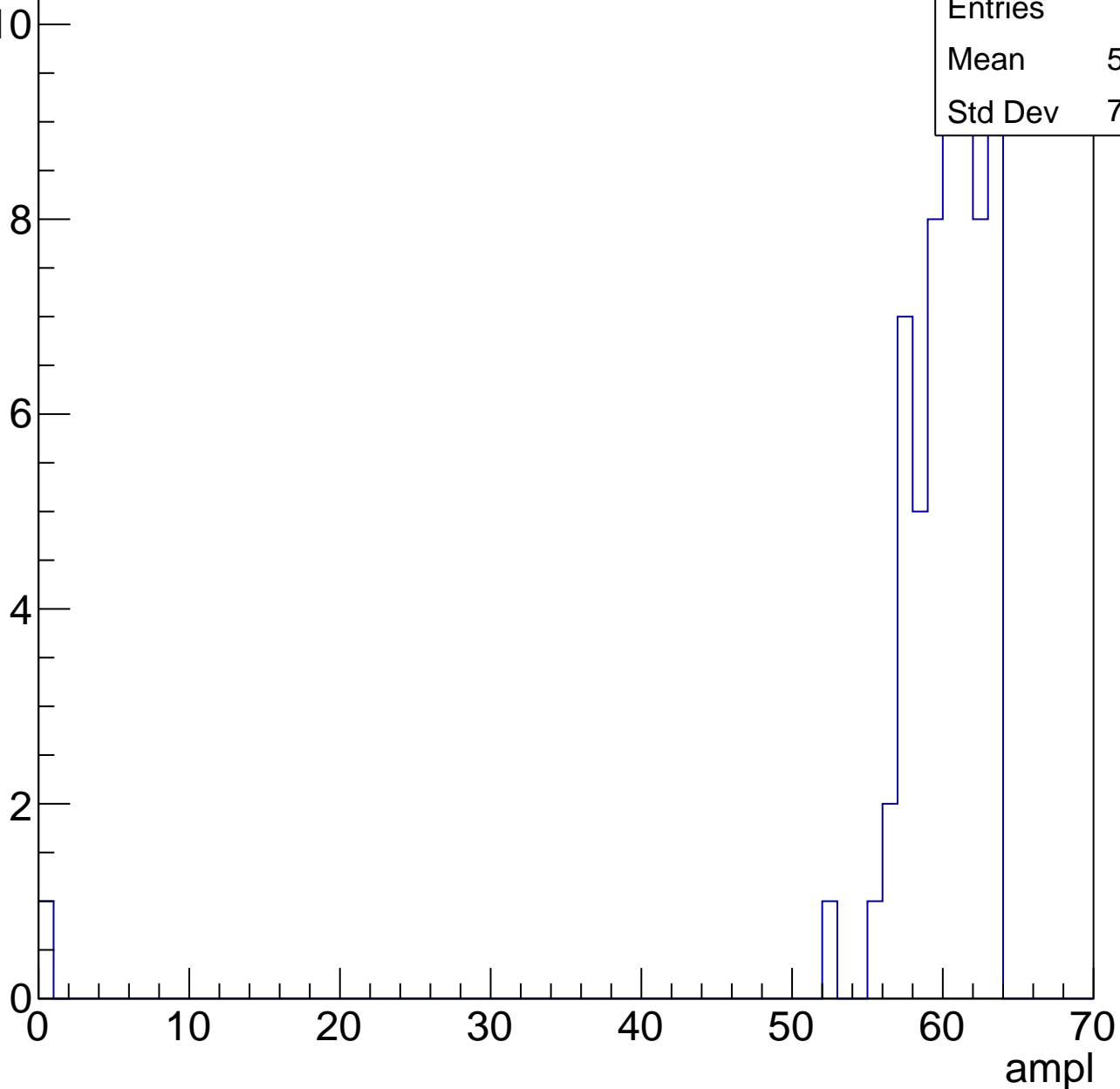


# B1L003S, U6-ch122, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	58.89
Std Dev	7.953



# B1L003S, U6-ch122, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch122, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U6-ch123, adc0

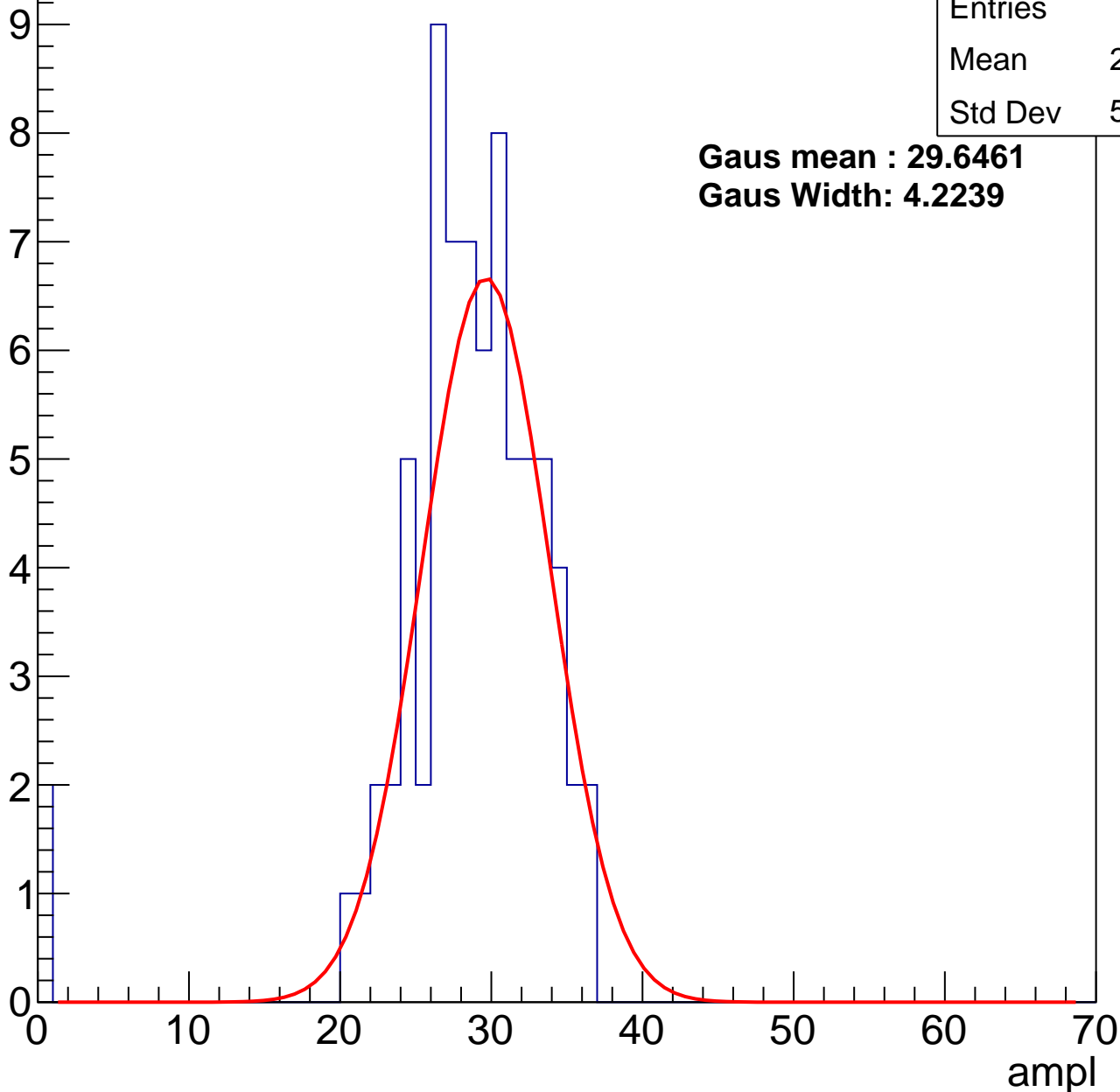
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	75
Mean	27.89
Std Dev	5.889

**Gaus mean : 29.6461**

**Gaus Width: 4.2239**



# B1L003S, U6-ch123, adc1

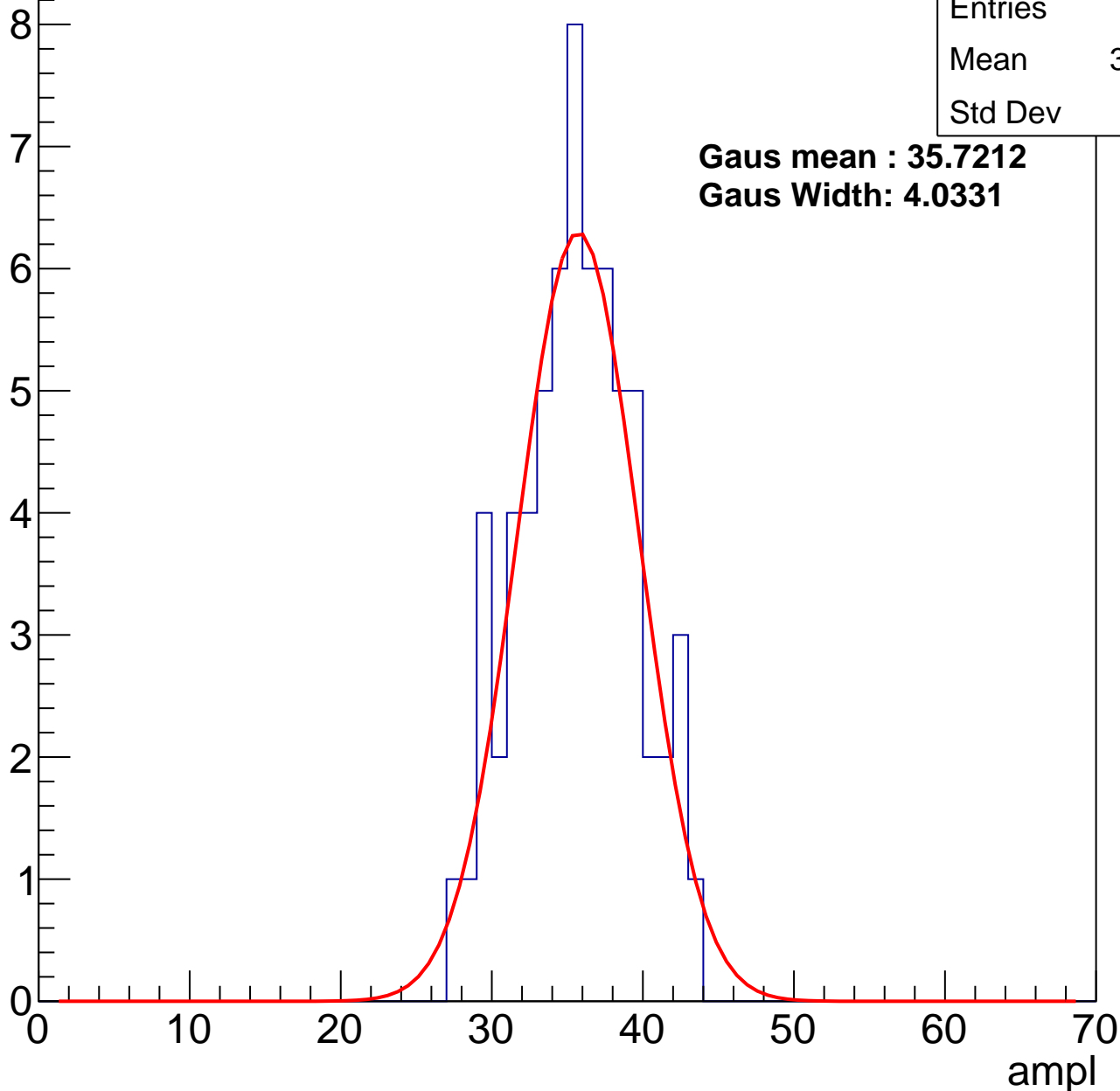
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	35.17
Std Dev	3.76

**Gaus mean : 35.7212**

**Gaus Width: 4.0331**



# B1L003S, U6-ch123, adc2

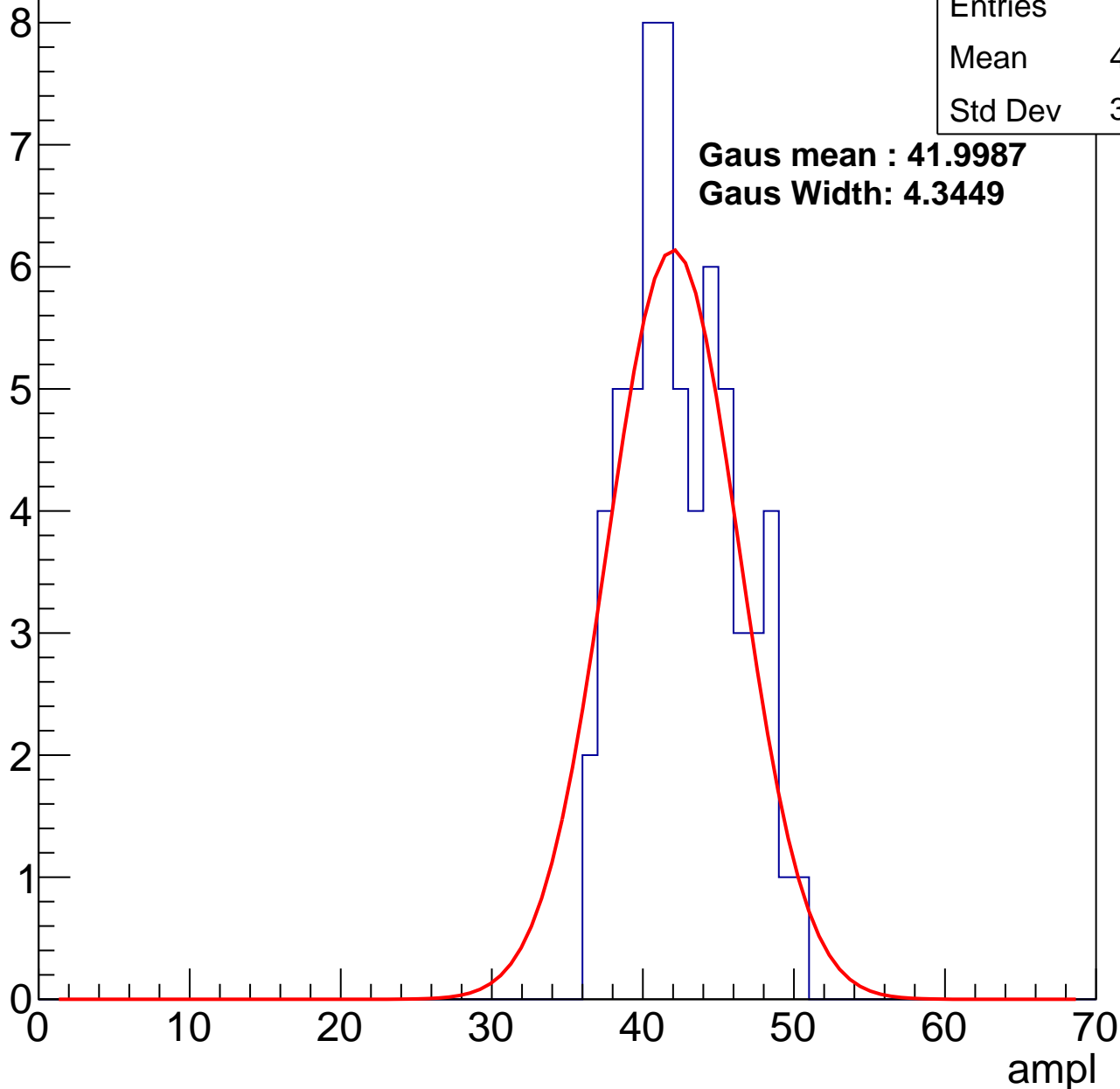
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	42.09
Std Dev	3.512

**Gaus mean : 41.9987**

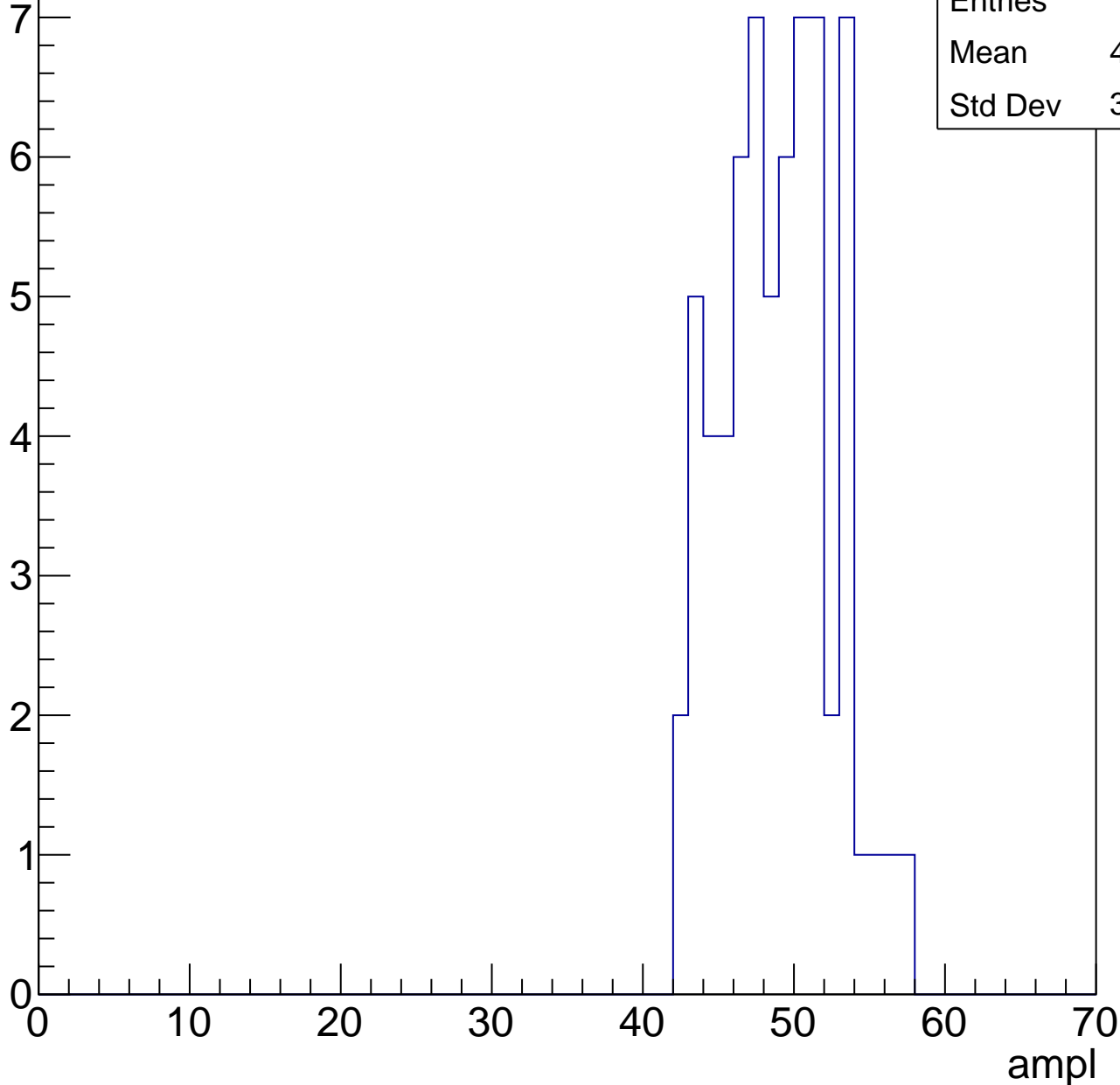
**Gaus Width: 4.3449**



# B1L003S, U6-ch123, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



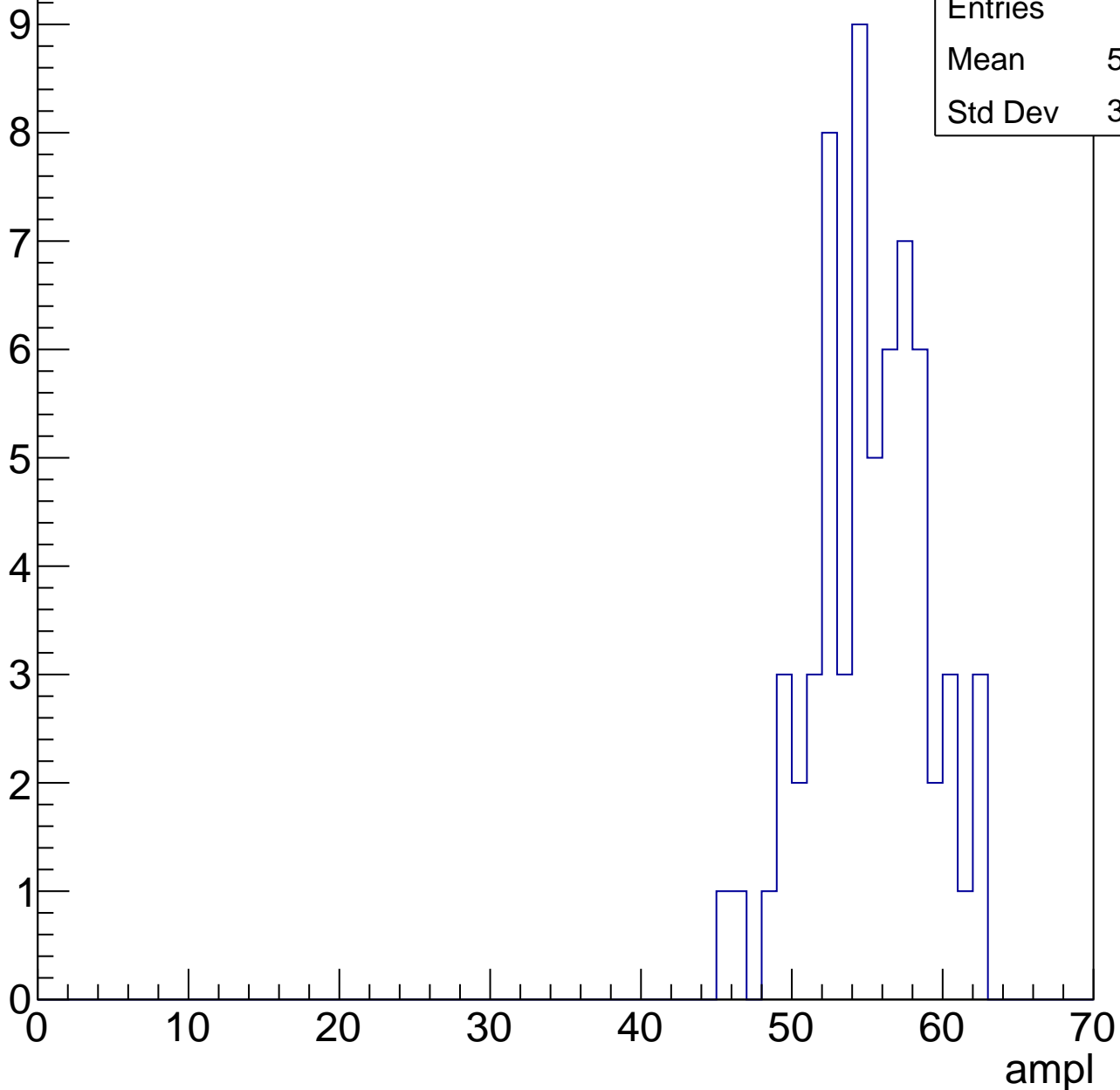
Entries	66
Mean	48.45
Std Dev	3.585

# B1L003S, U6-ch123, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	54.73
Std Dev	3.755

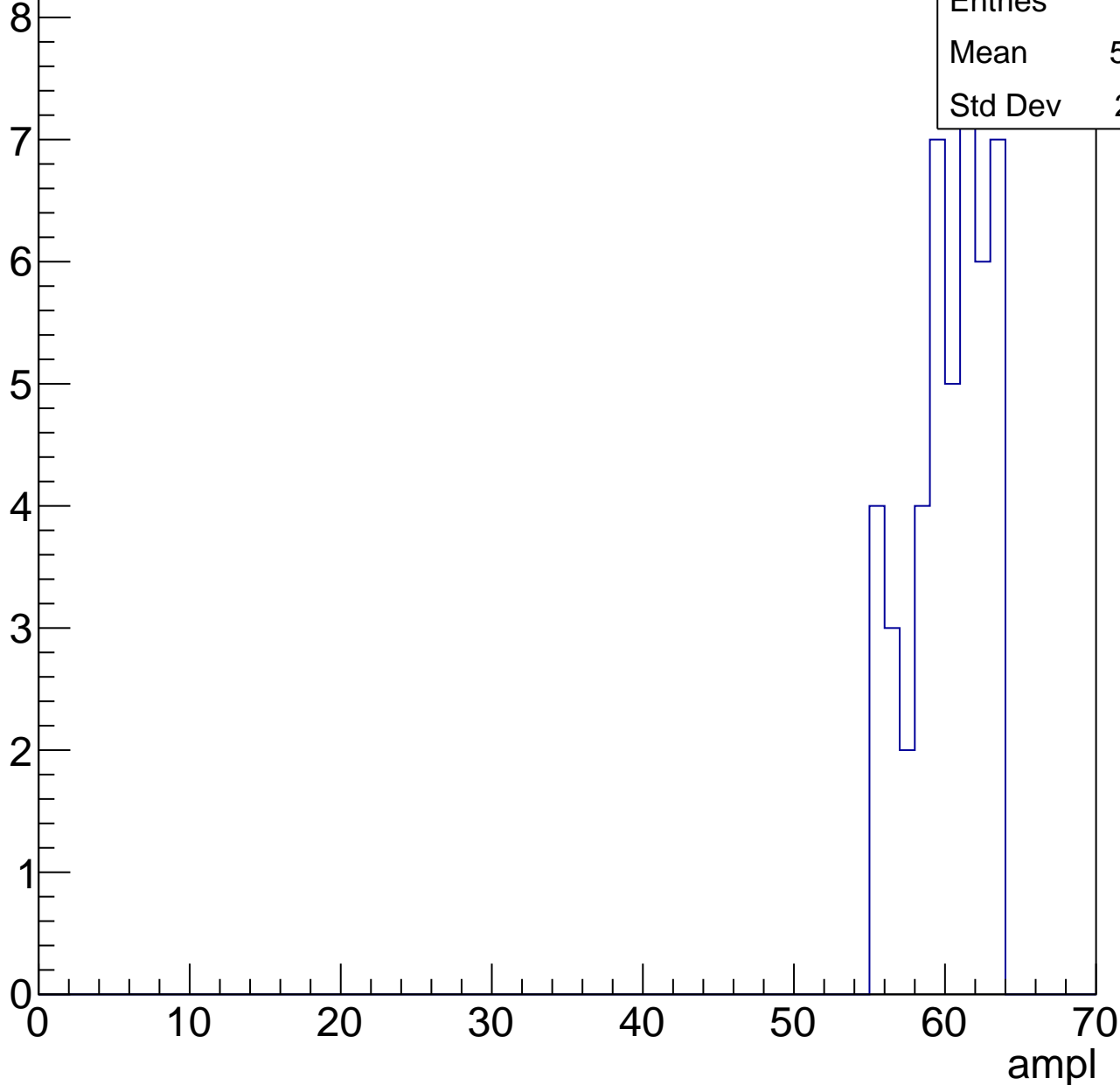


# B1L003S, U6-ch123, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

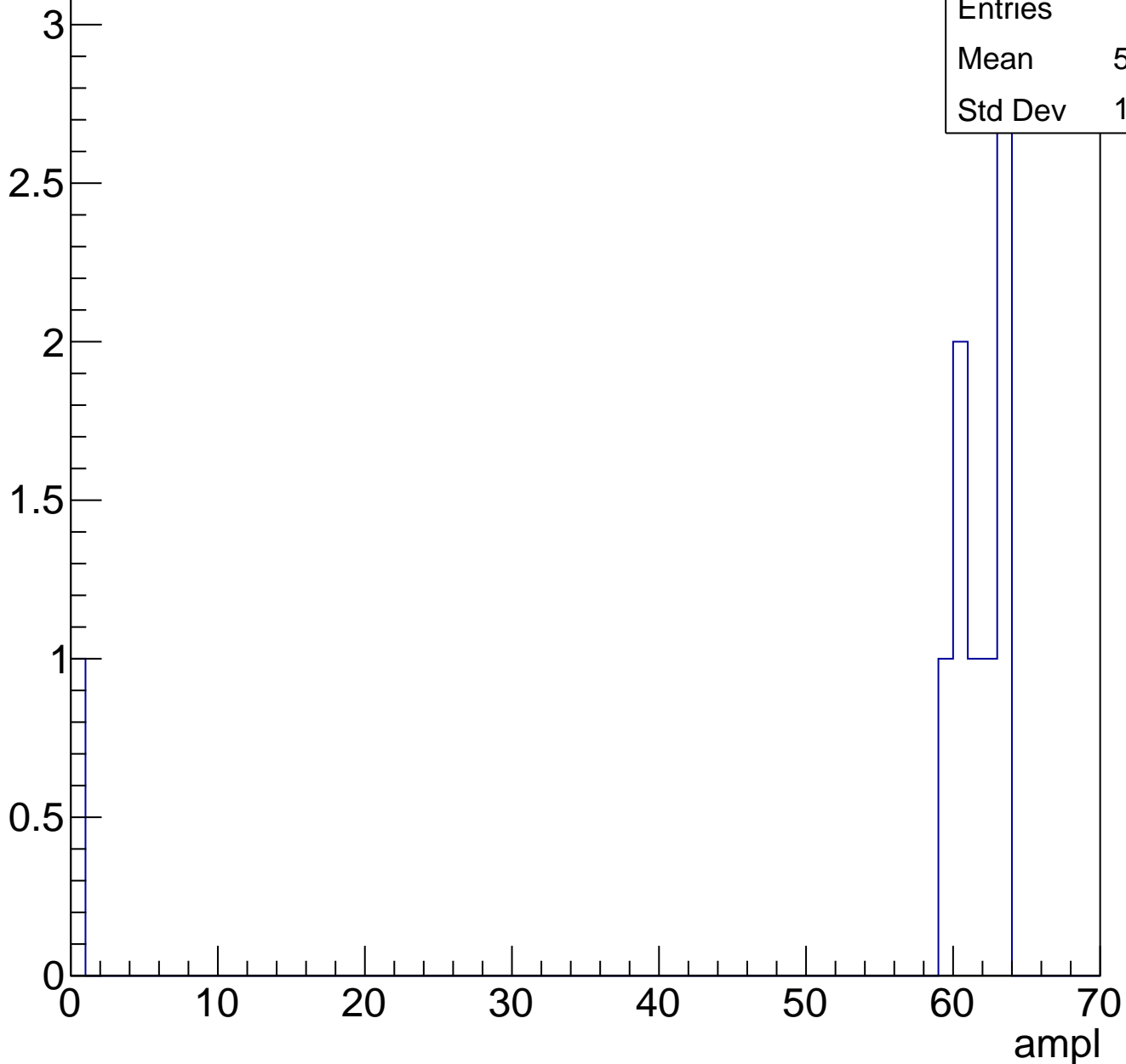
Entries	46
Mean	59.74
Std Dev	2.471



# B1L003S, U6-ch123, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	9
Mean	54.56
Std Dev	19.34



# B1L003S, U6-ch123, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch124, adc0

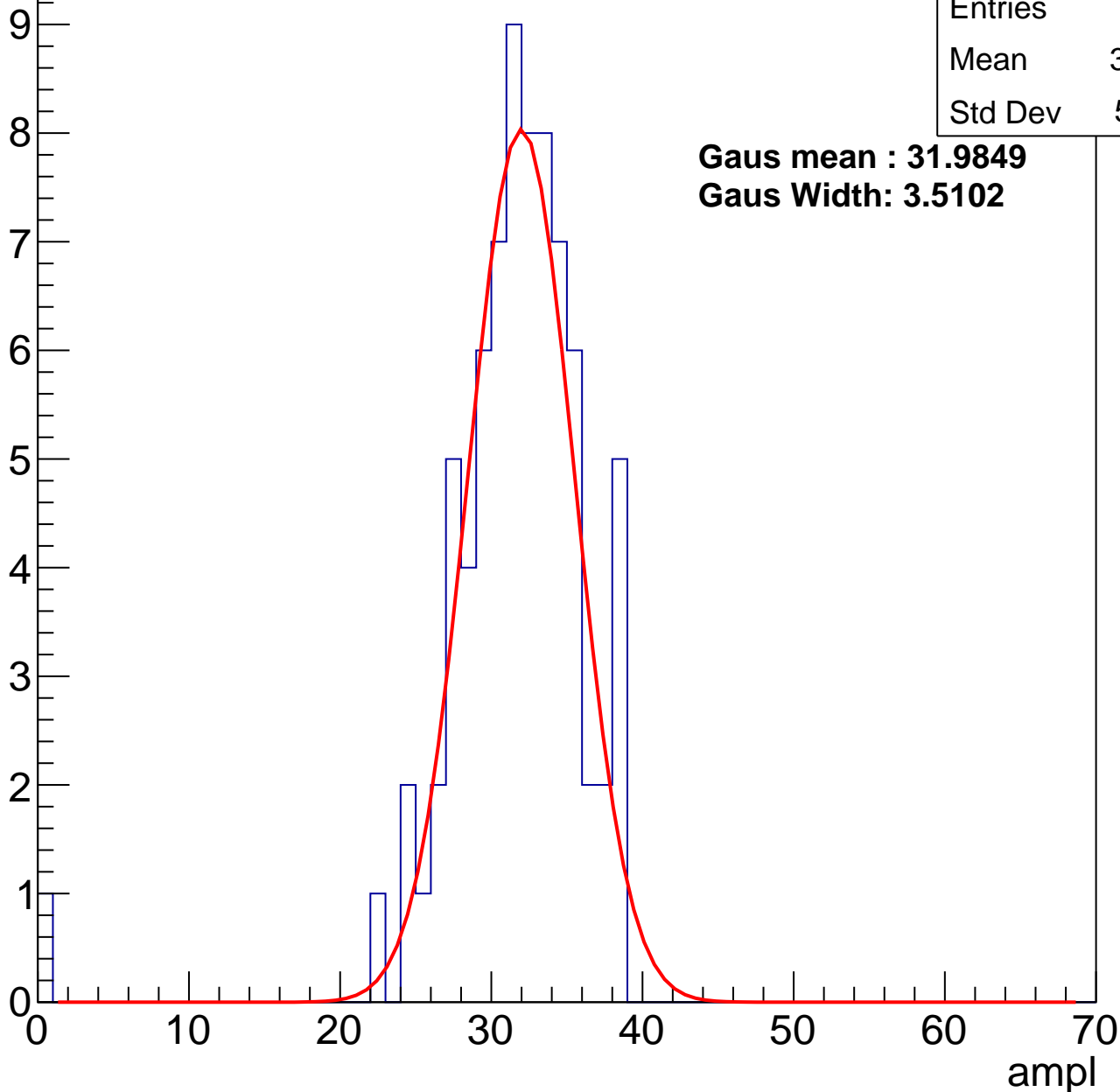
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	76
Mean	31.07
Std Dev	5.051

**Gaus mean : 31.9849**

**Gaus Width: 3.5102**



# B1L003S, U6-ch124, adc1

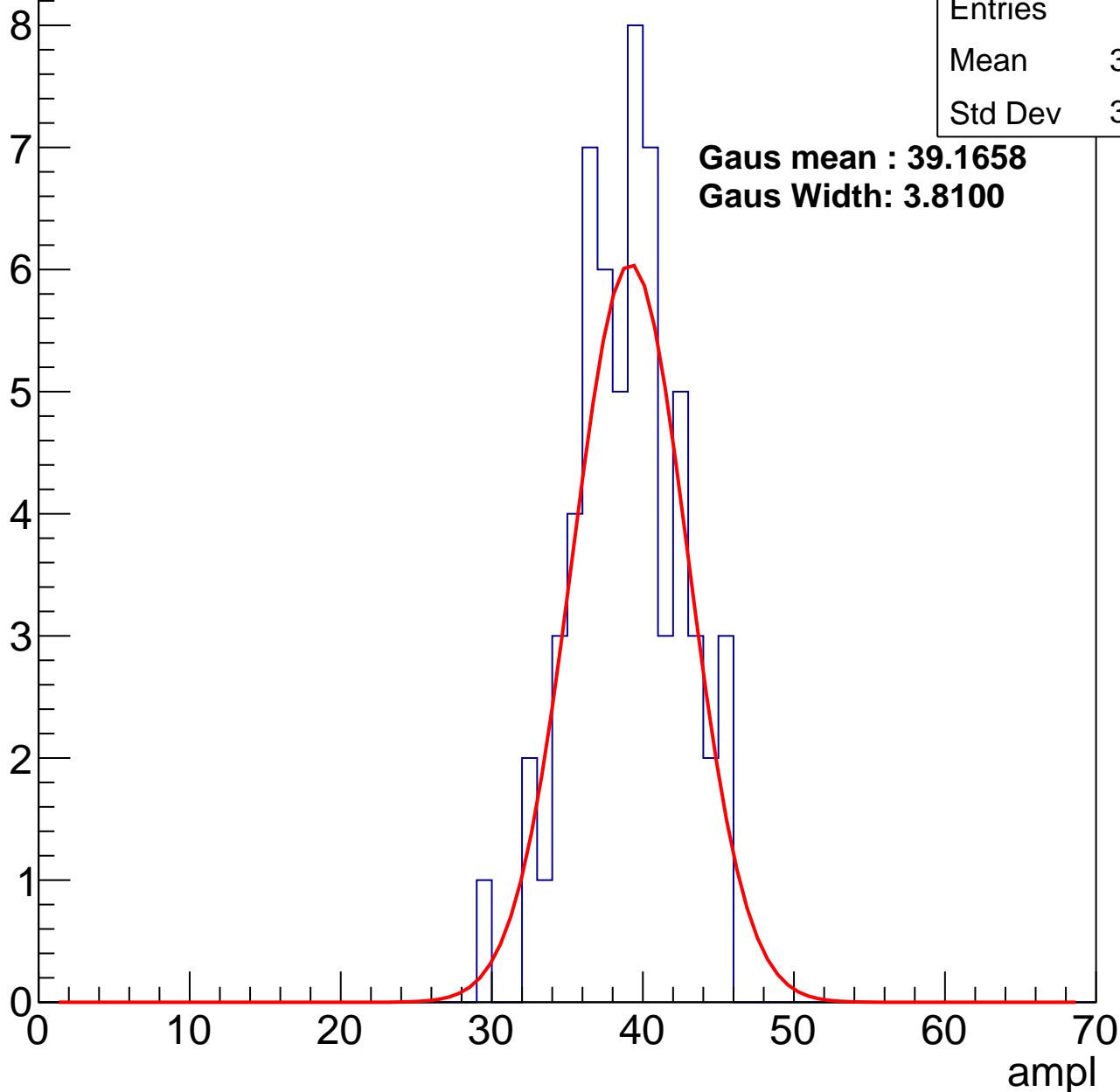
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	38.48
Std Dev	3.462

**Gaus mean : 39.1658**

**Gaus Width: 3.8100**



# B1L003S, U6-ch124, adc2

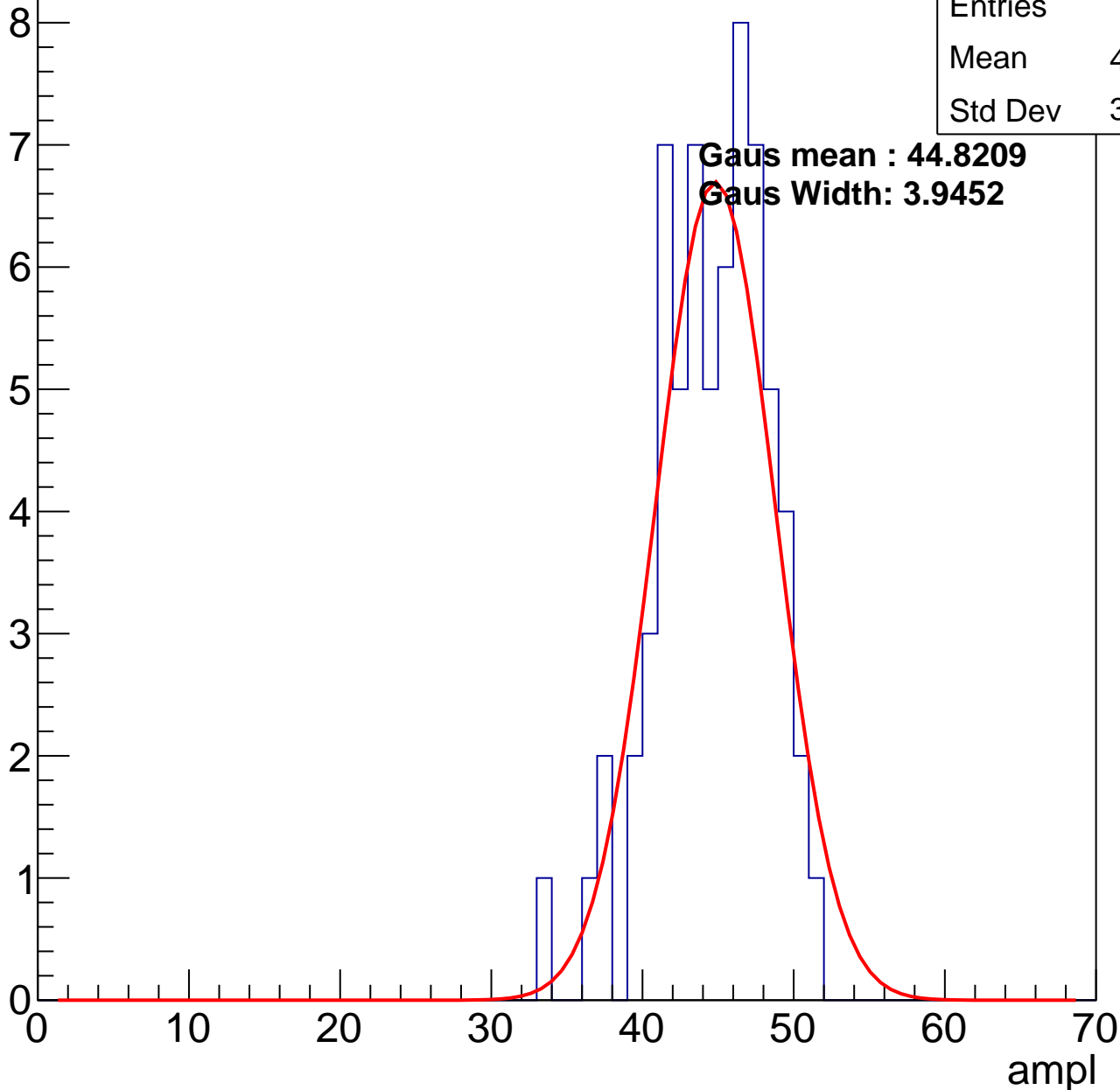
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	44.14
Std Dev	3.634

Gaus mean : 44.8209

Gaus Width: 3.9452

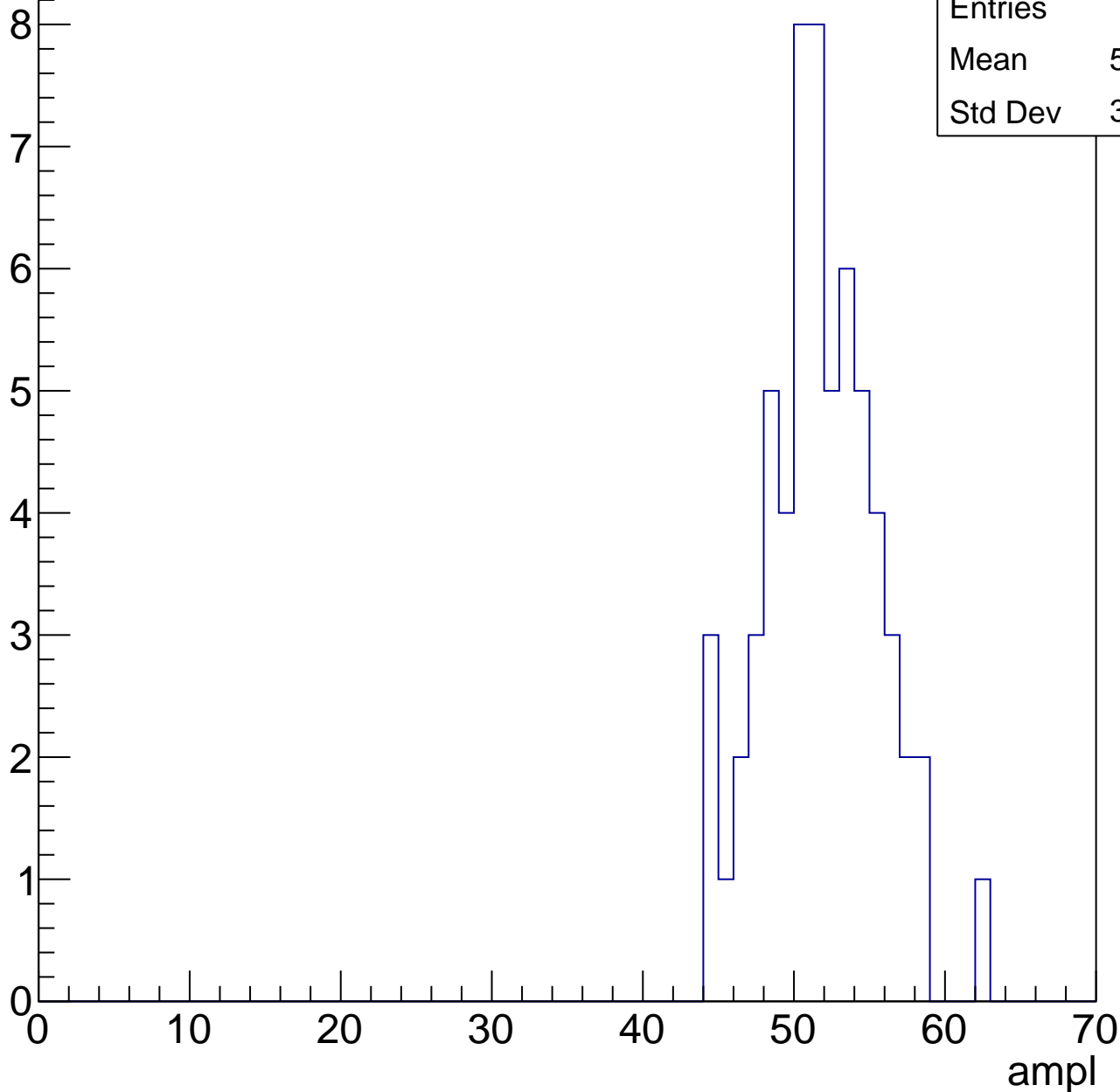


# B1L003S, U6-ch124, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

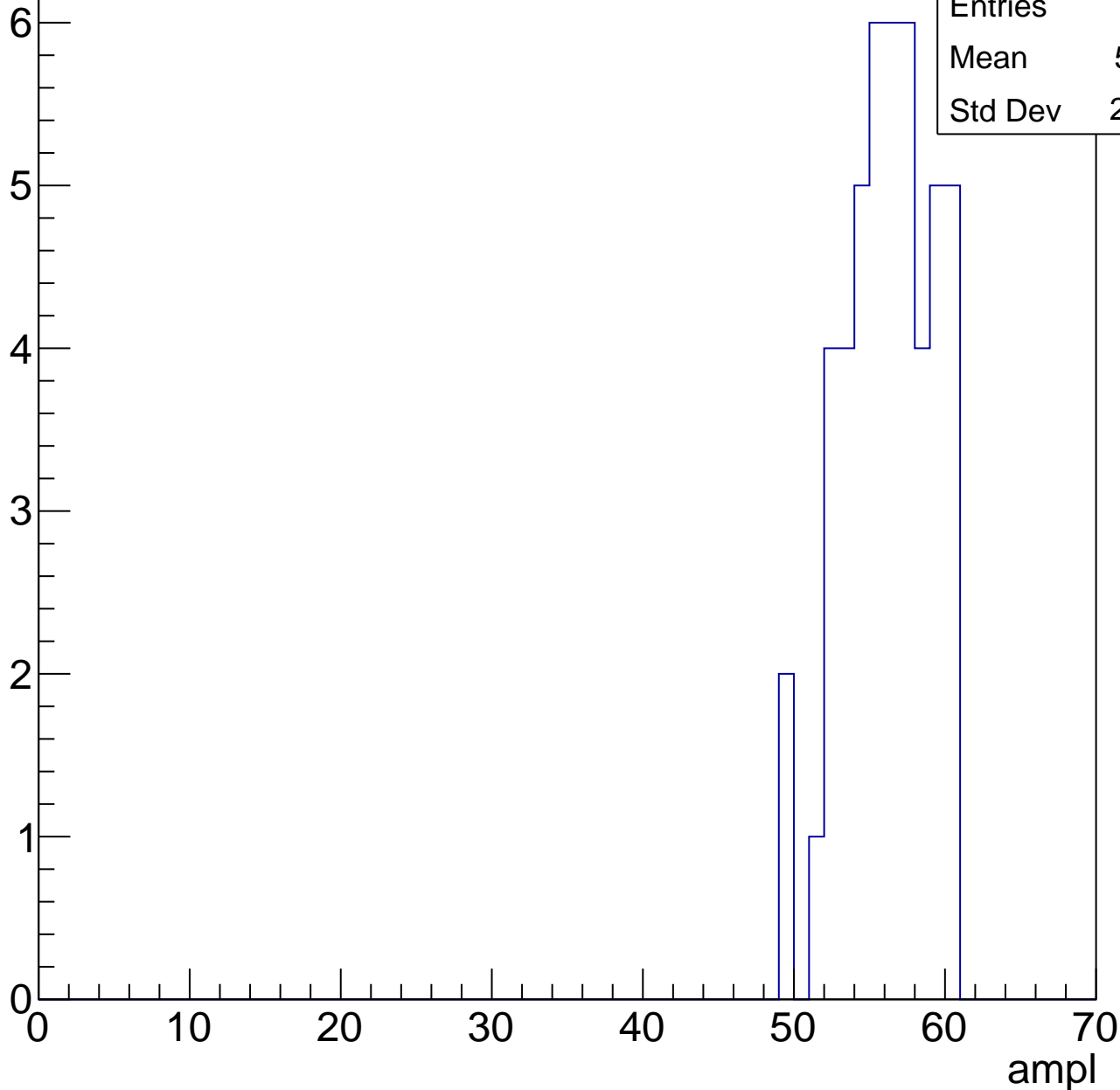
Entries	62
Mean	51.32
Std Dev	3.697



# B1L003S, U6-ch124, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



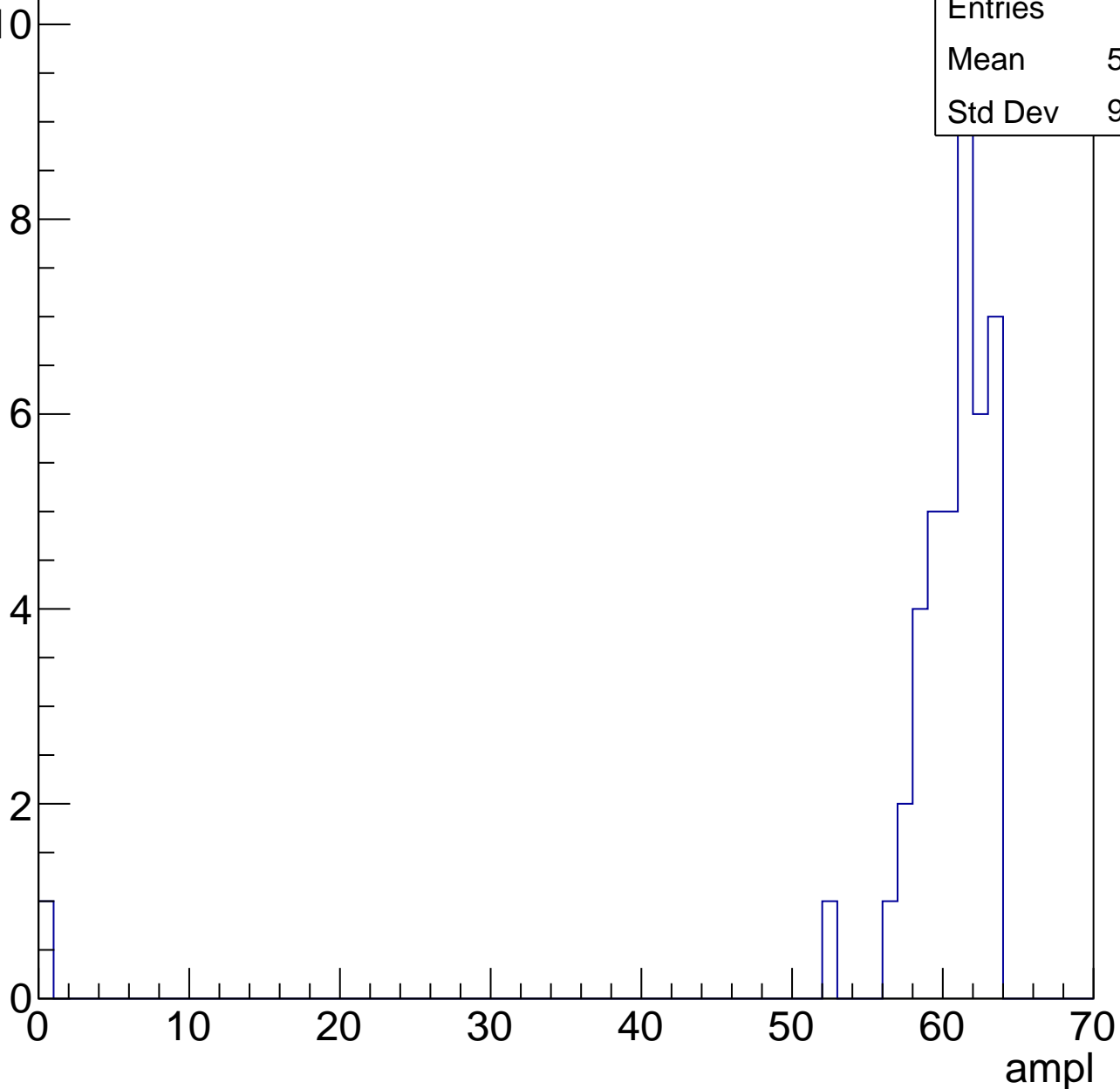
Entries	48
Mean	55.71
Std Dev	2.857

# B1L003S, U6-ch124, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	42
Mean	58.86
Std Dev	9.463



# B1L003S, U6-ch124, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch124, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U6-ch125, adc0

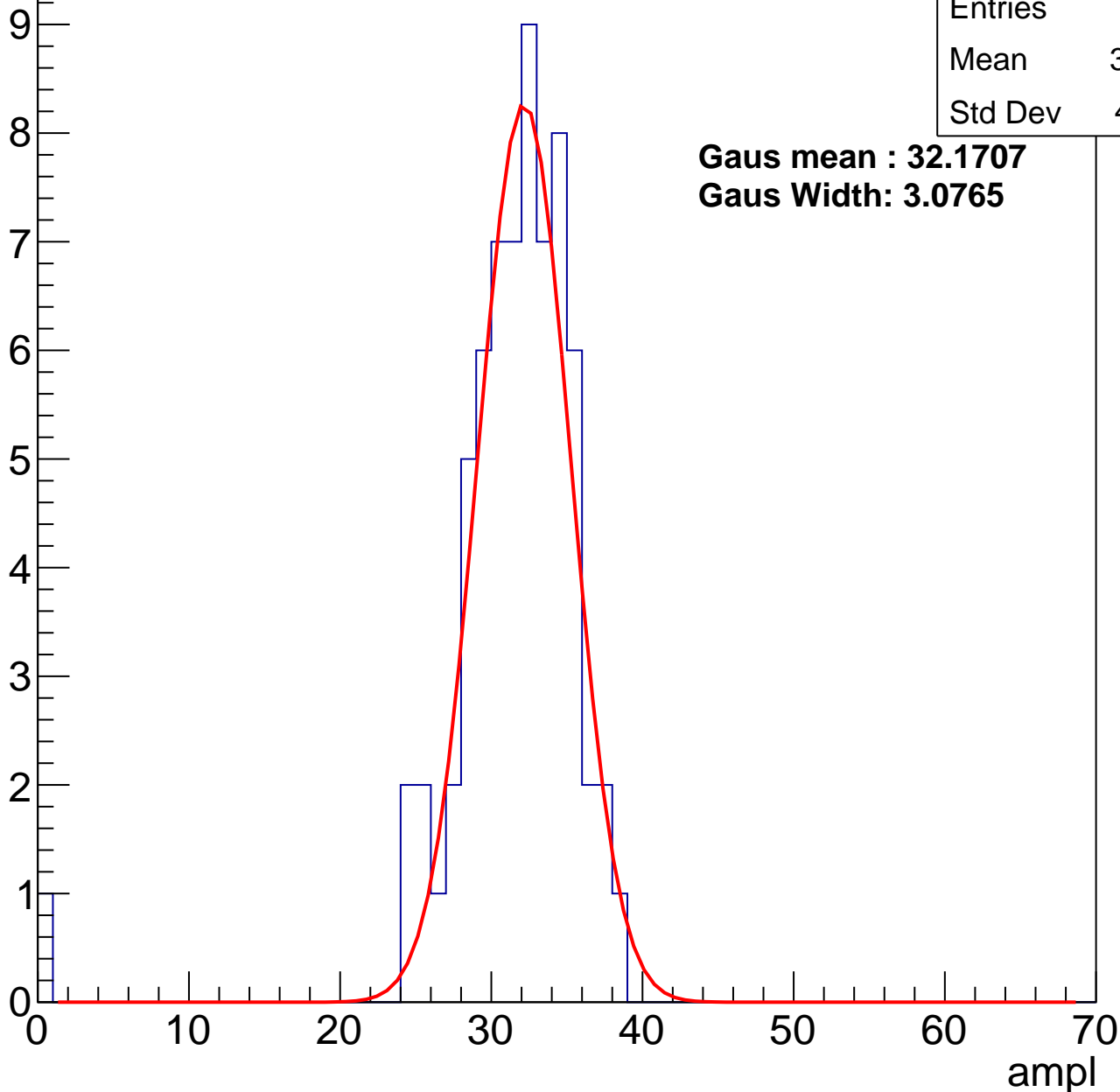
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	30.94
Std Dev	4.911

**Gaus mean : 32.1707**

**Gaus Width: 3.0765**



# B1L003S, U6-ch125, adc1

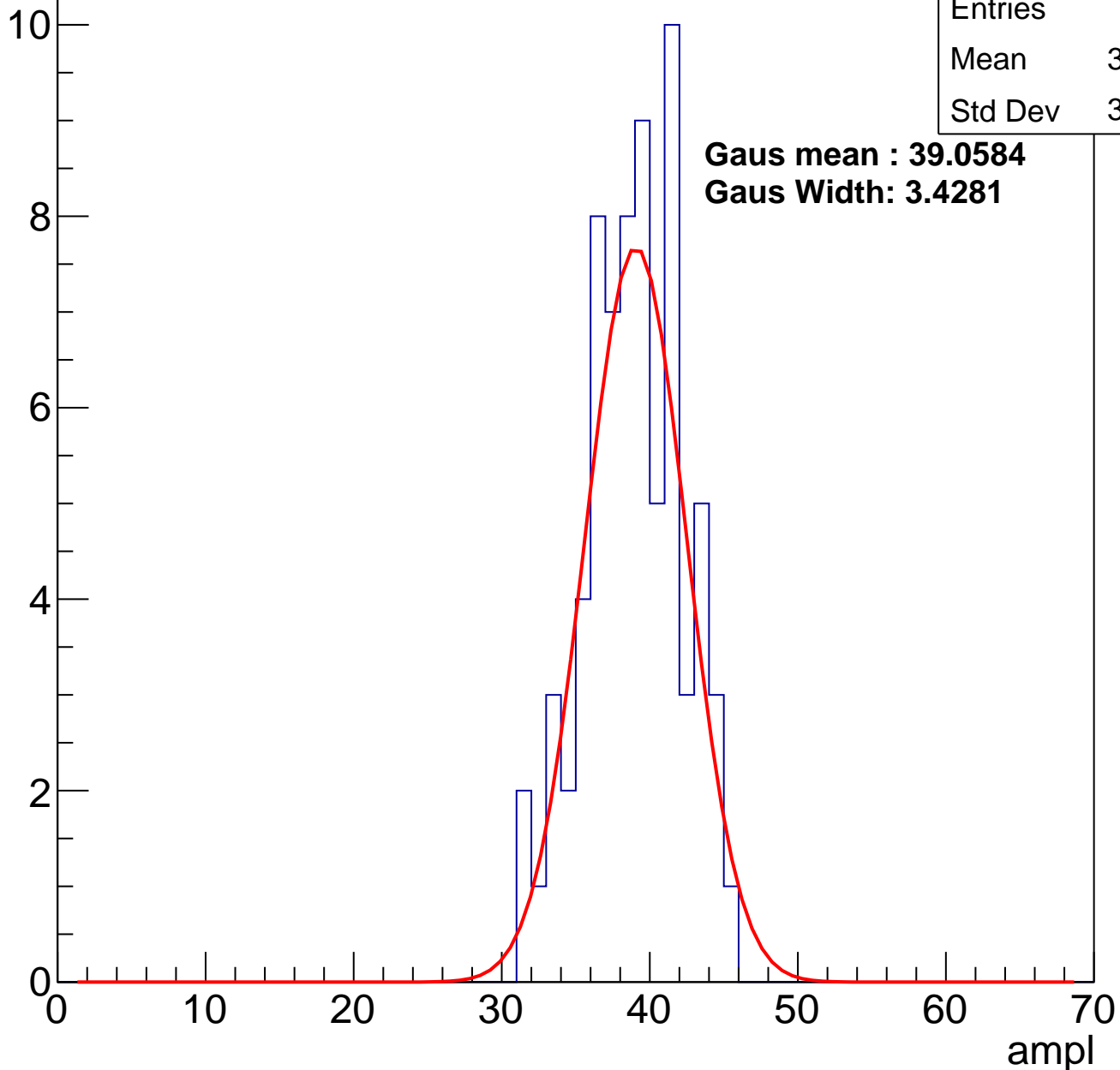
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	71
Mean	38.46
Std Dev	3.249

**Gaus mean : 39.0584**

**Gaus Width: 3.4281**

Entry



# B1L003S, U6-ch125, adc2

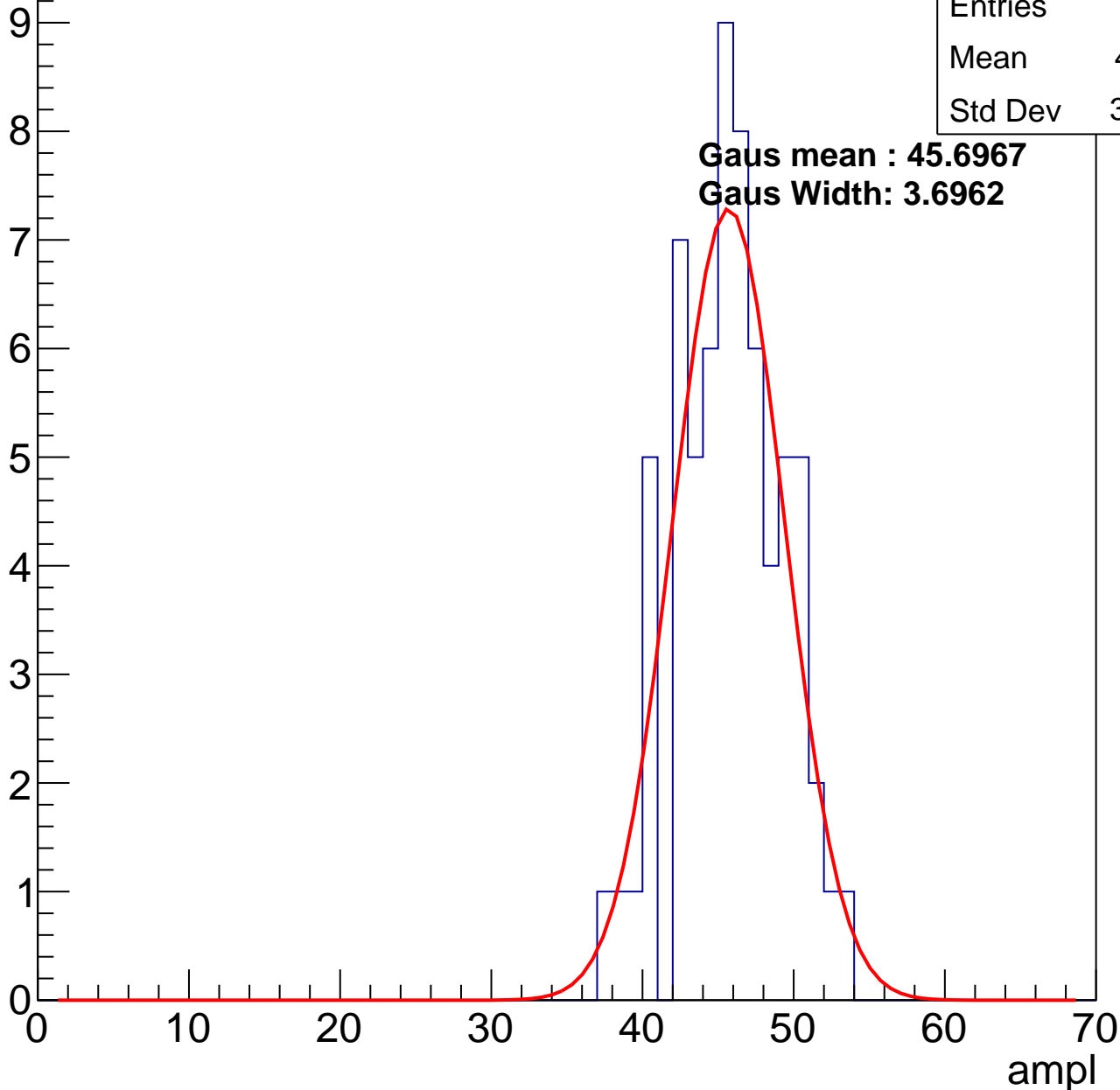
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	45.31
Std Dev	3.486

**Gaus mean : 45.6967**

**Gaus Width: 3.6962**

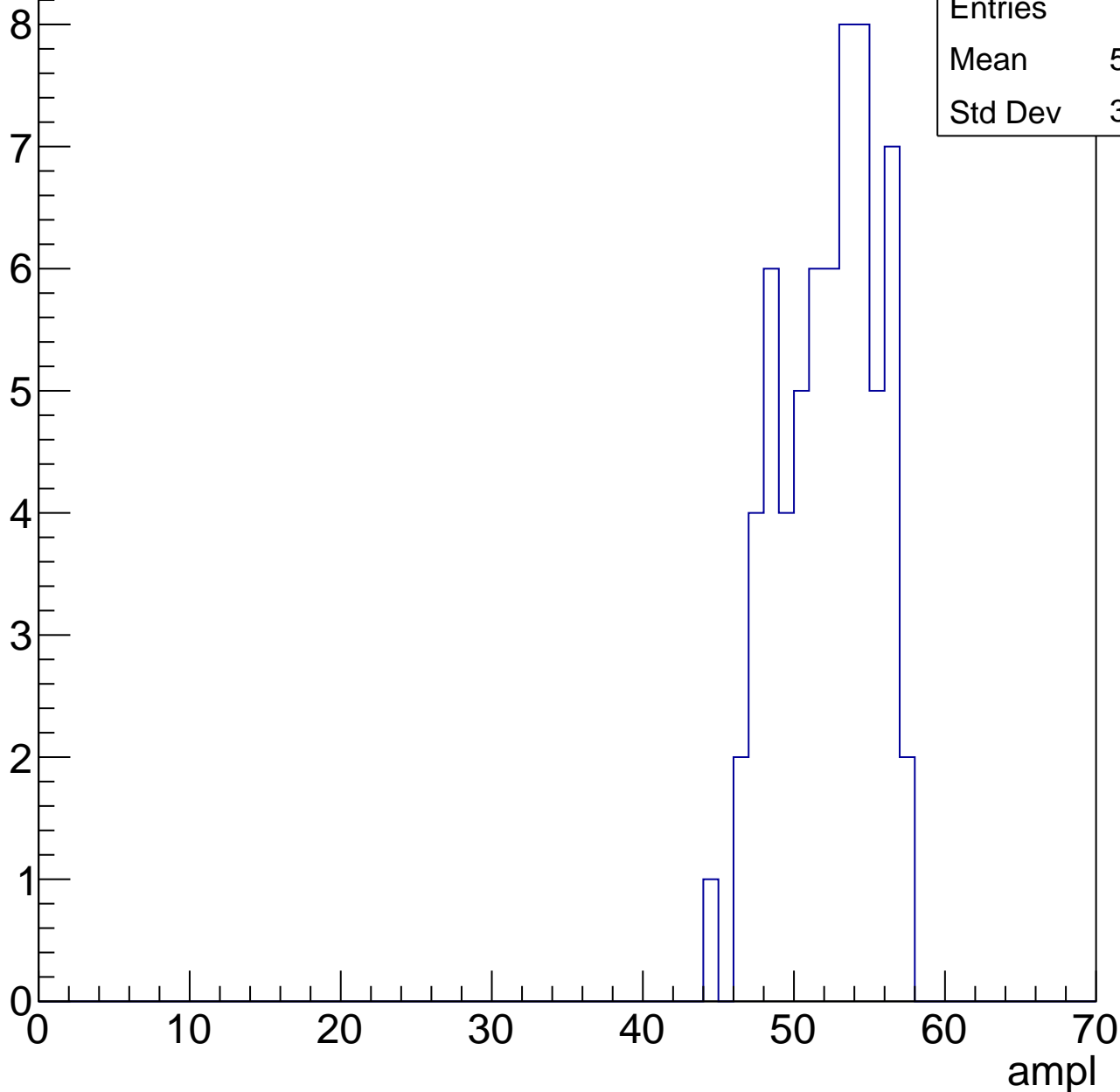


# B1L003S, U6-ch125, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	51.77
Std Dev	3.156

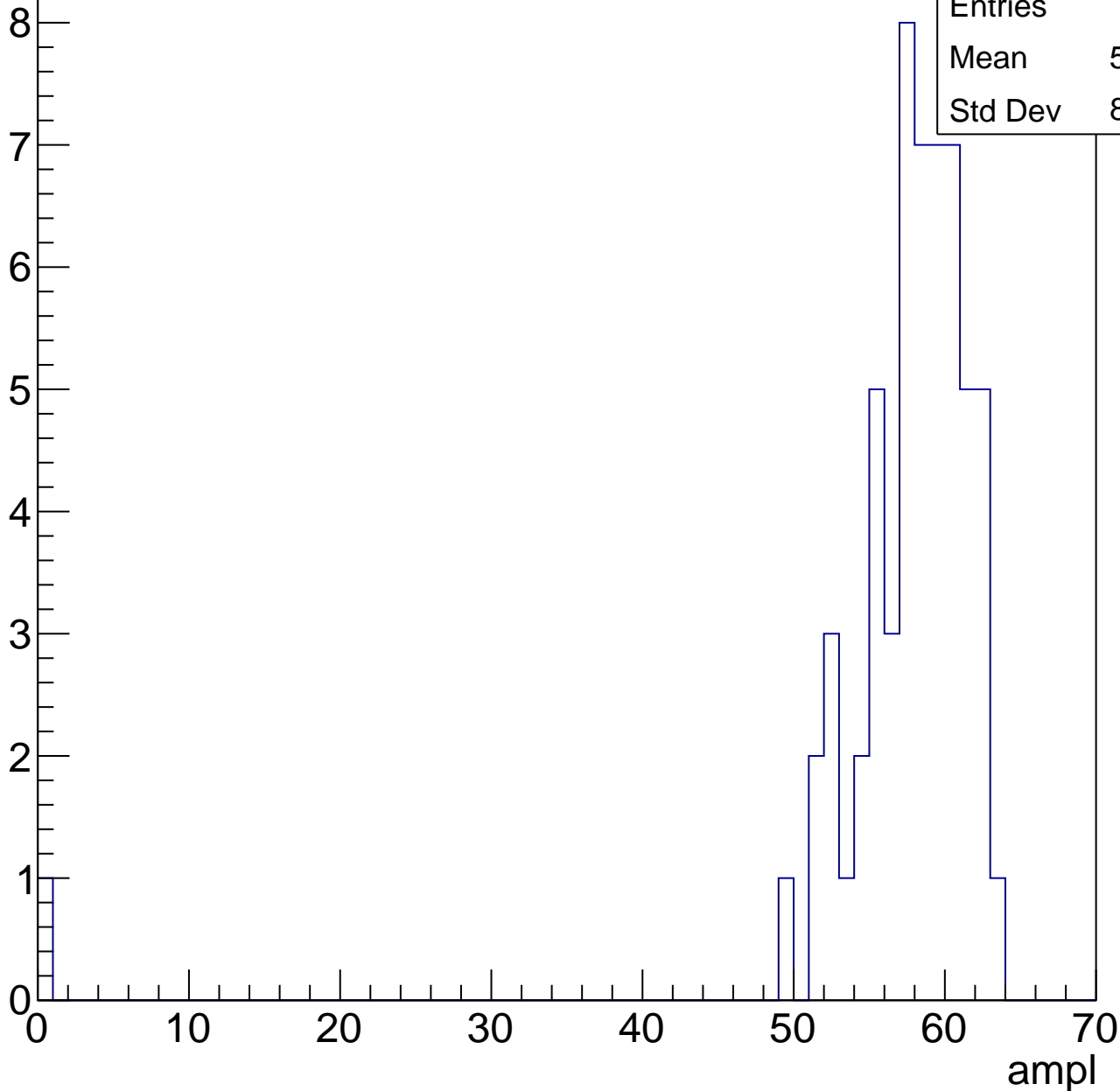


# B1L003S, U6-ch125, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	56.62
Std Dev	8.145

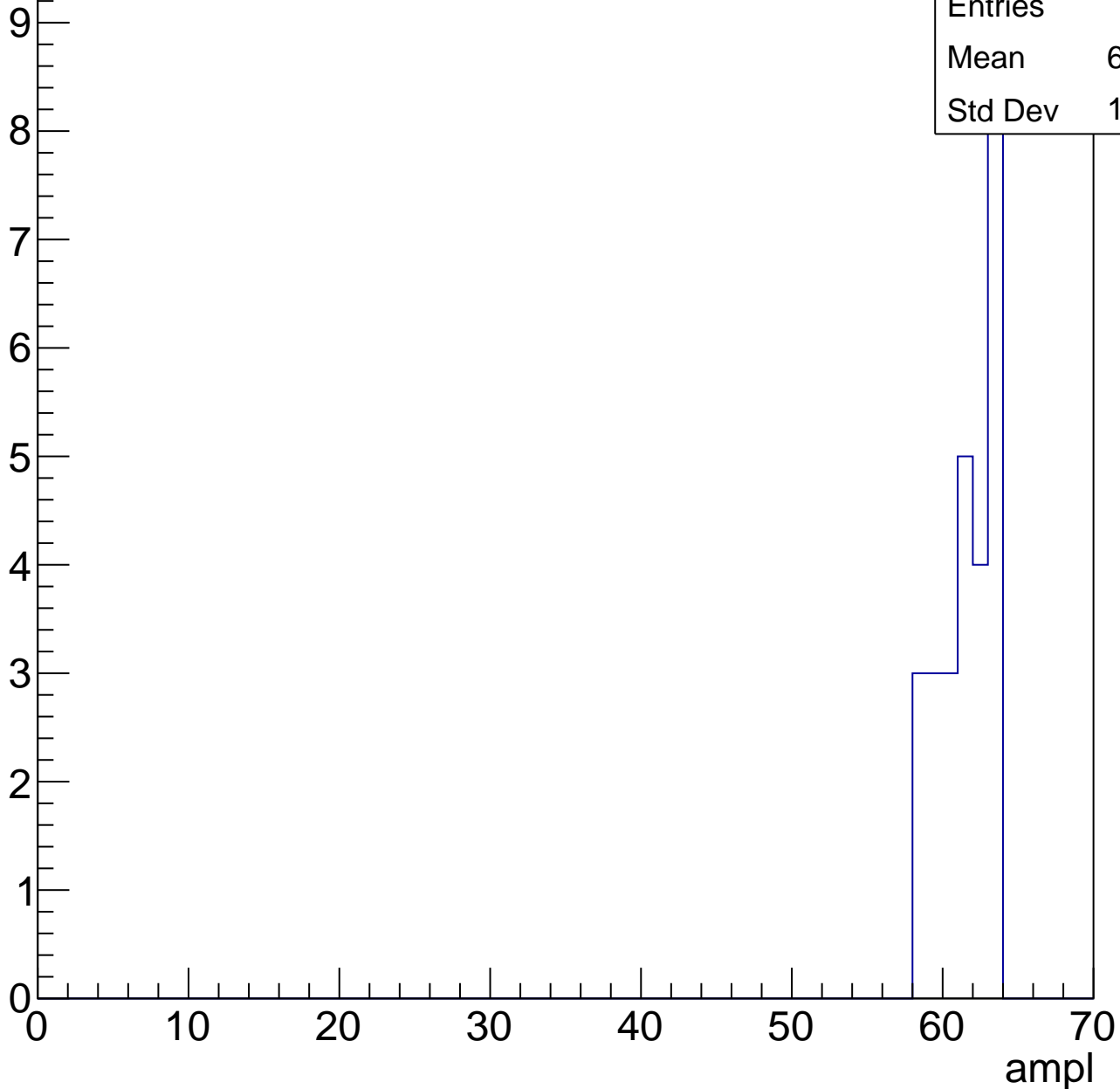


# B1L003S, U6-ch125, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	27
Mean	61.15
Std Dev	1.736



# B1L003S, U6-ch125, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch125, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U6-ch126, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	66
Mean	28.41
Std Dev	4.859

**Gaus mean : 29.3439**

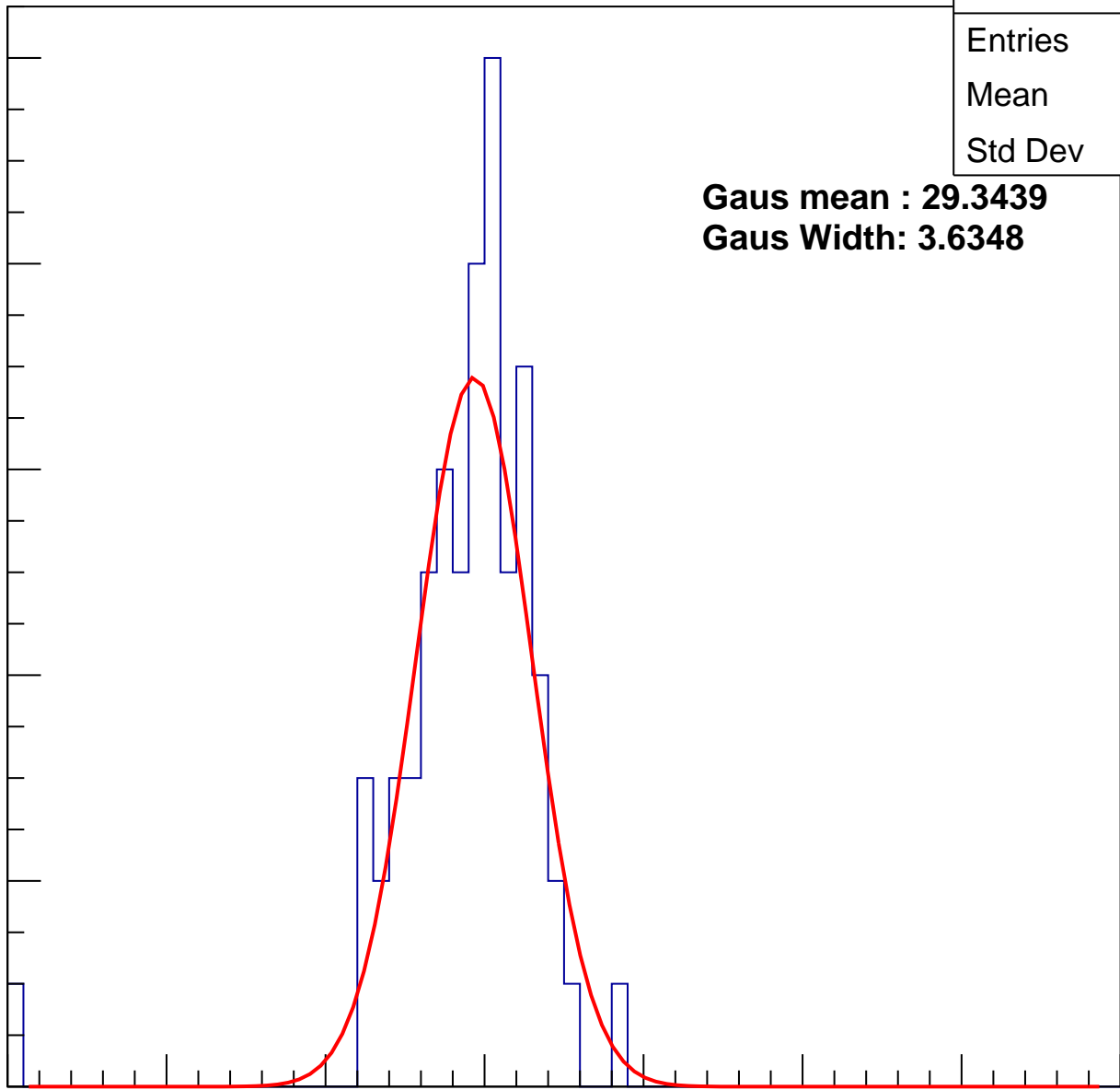
**Gaus Width: 3.6348**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U6-ch126, adc1

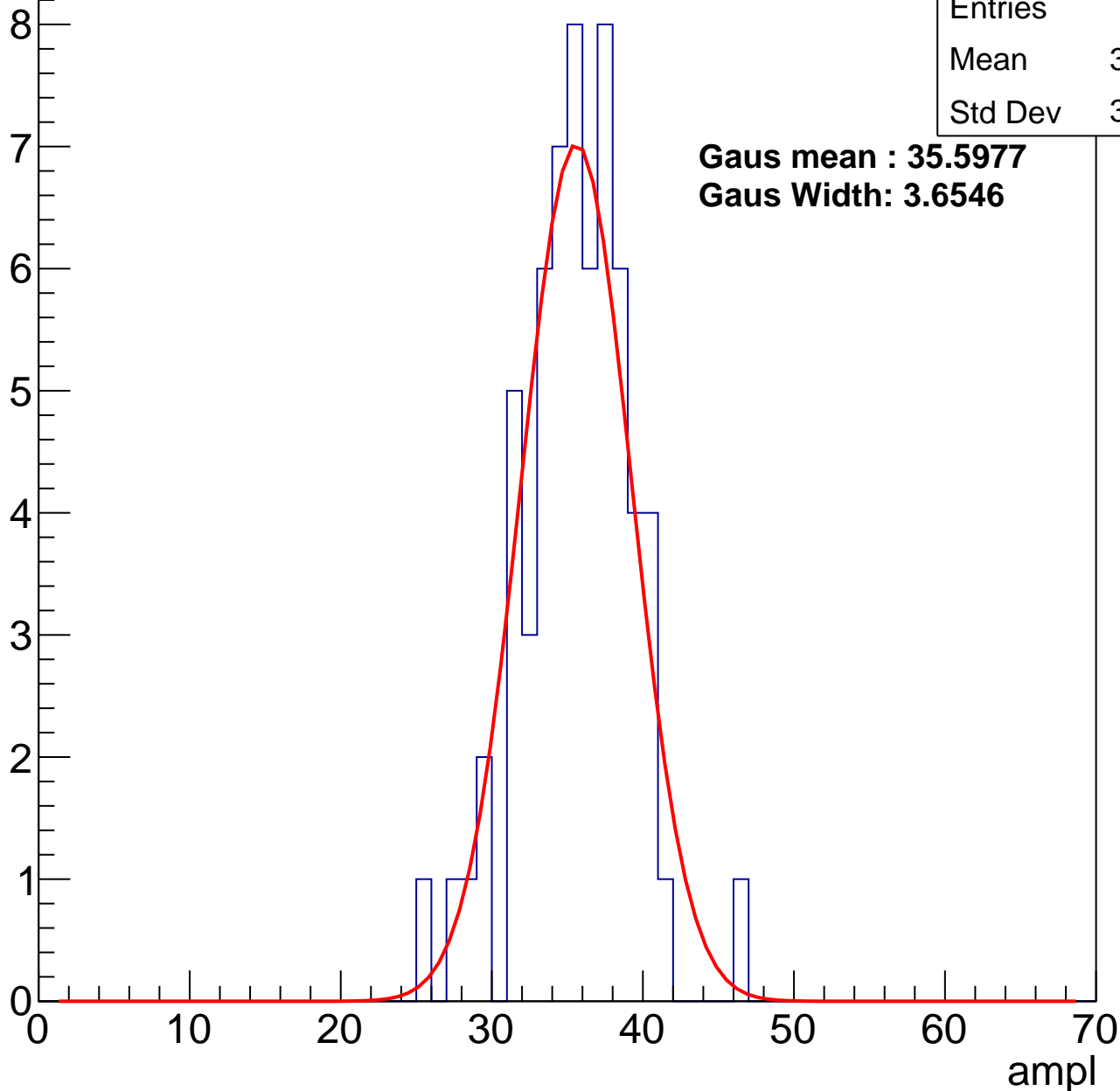
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	35.12
Std Dev	3.612

**Gaus mean : 35.5977**

**Gaus Width: 3.6546**



# B1L003S, U6-ch126, adc2

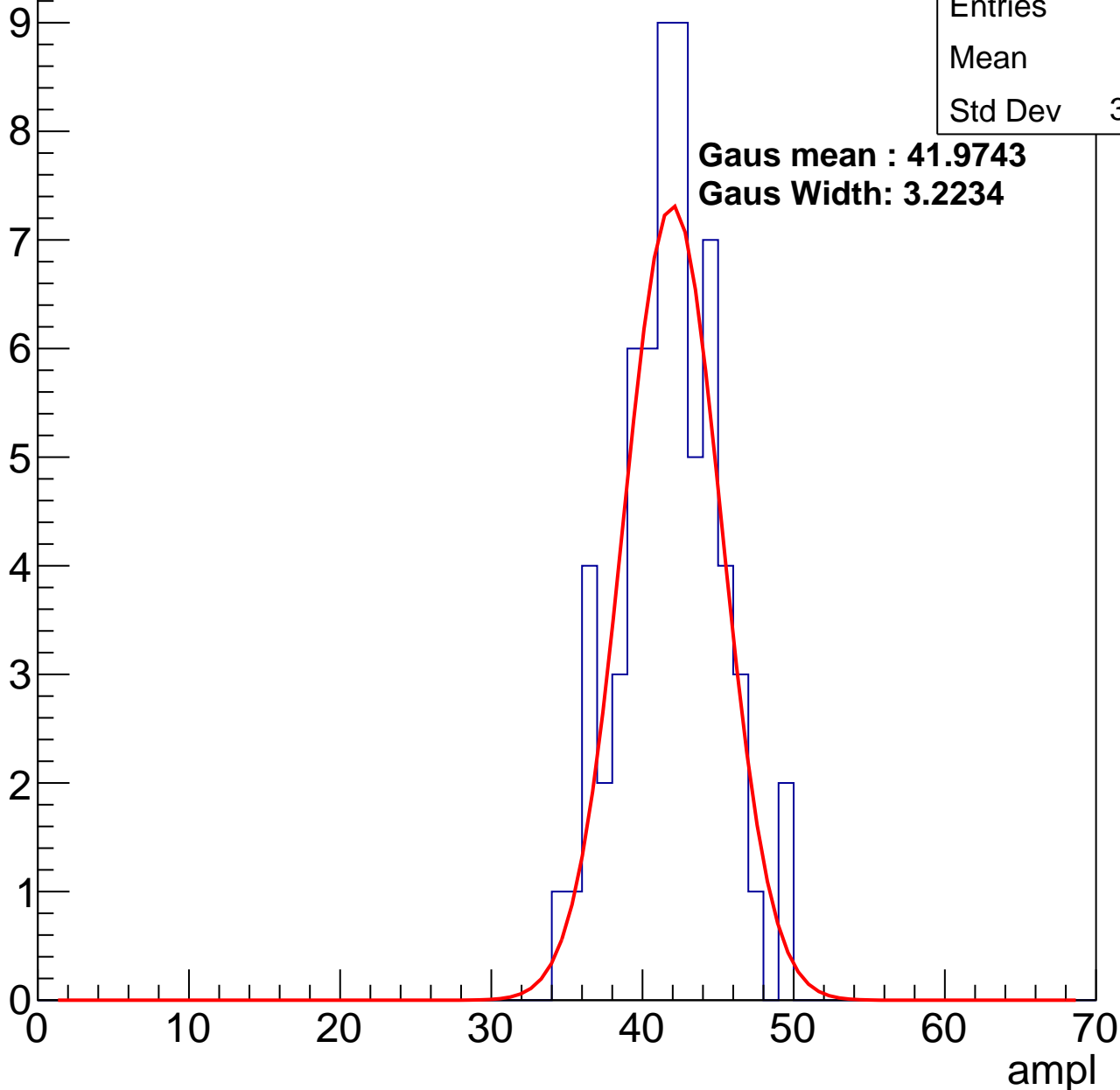
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	41.4
Std Dev	3.234

**Gaus mean : 41.9743**

**Gaus Width: 3.2234**

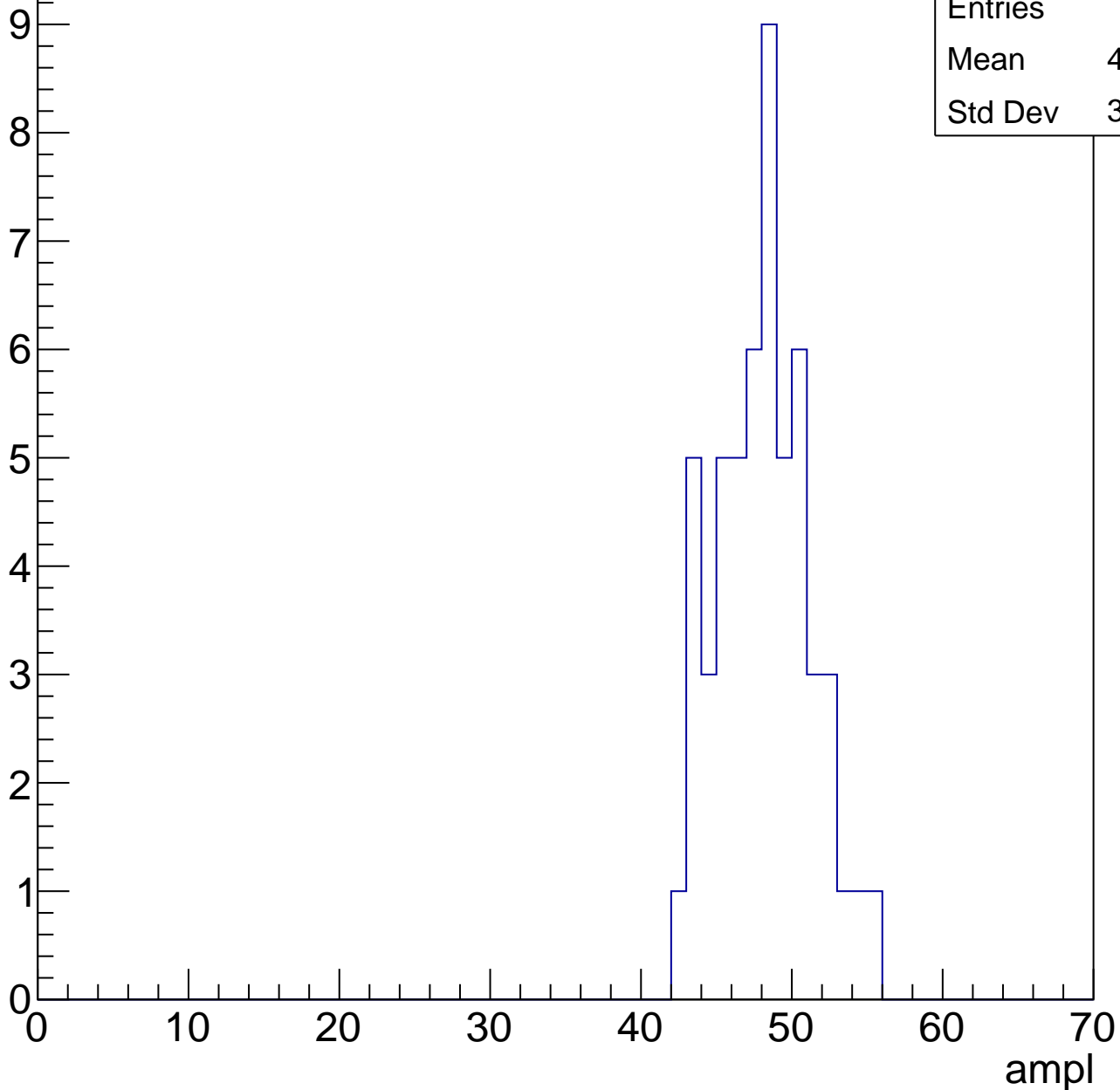


# B1L003S, U6-ch126, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	54
Mean	47.67
Std Dev	3.006

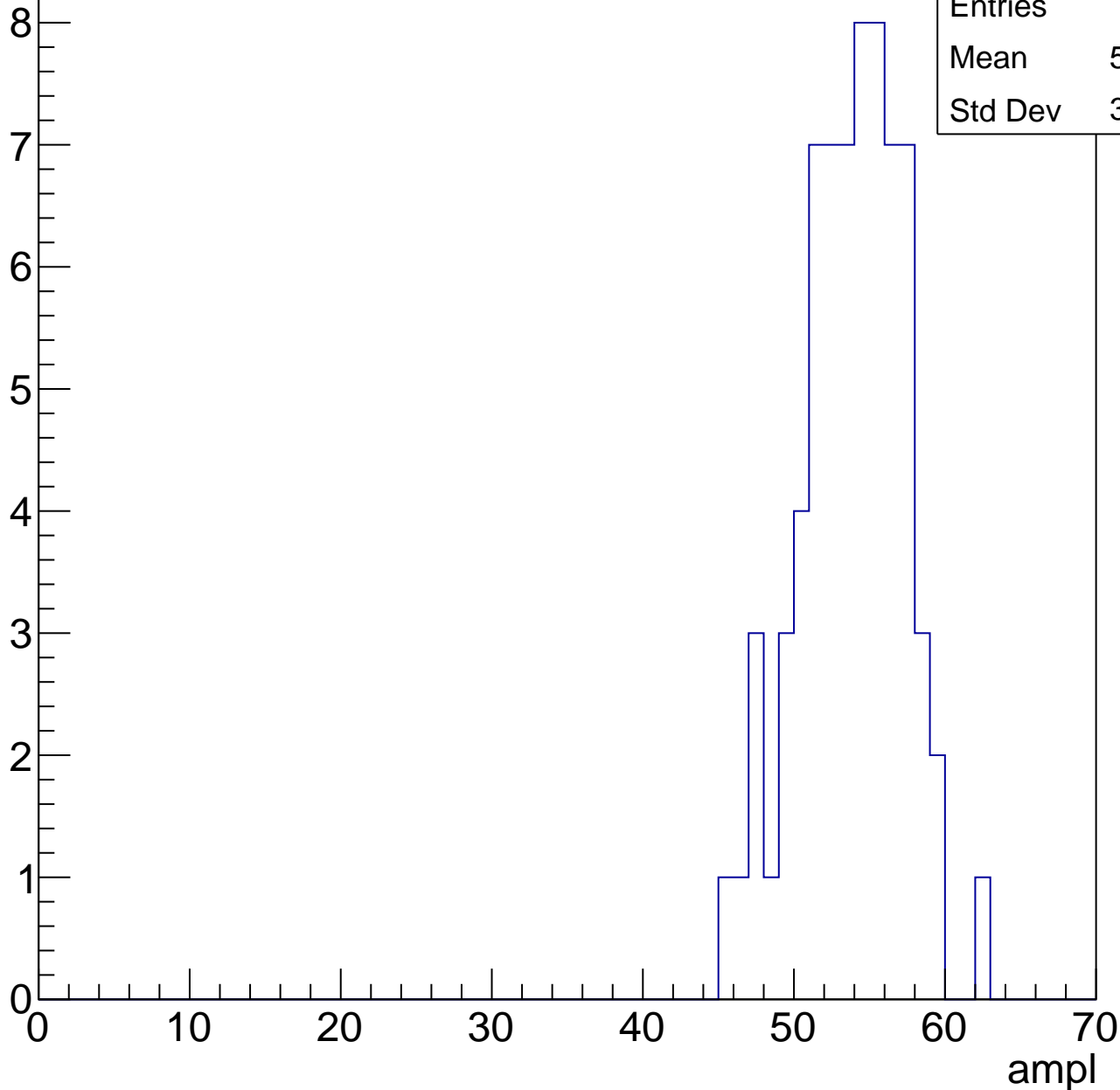


# B1L003S, U6-ch126, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

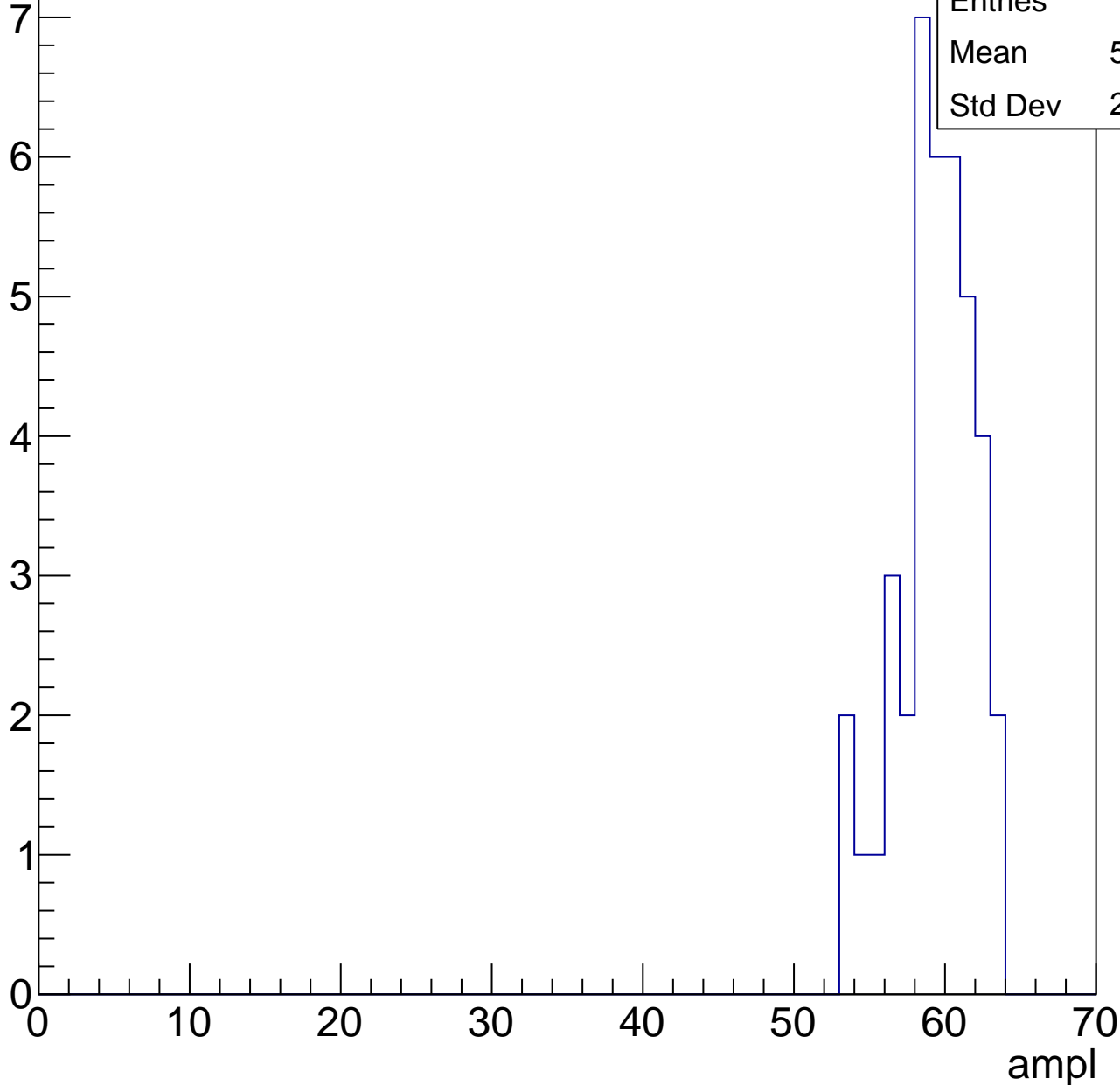
Entries	70
Mean	53.37
Std Dev	3.377



# B1L003S, U6-ch126, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

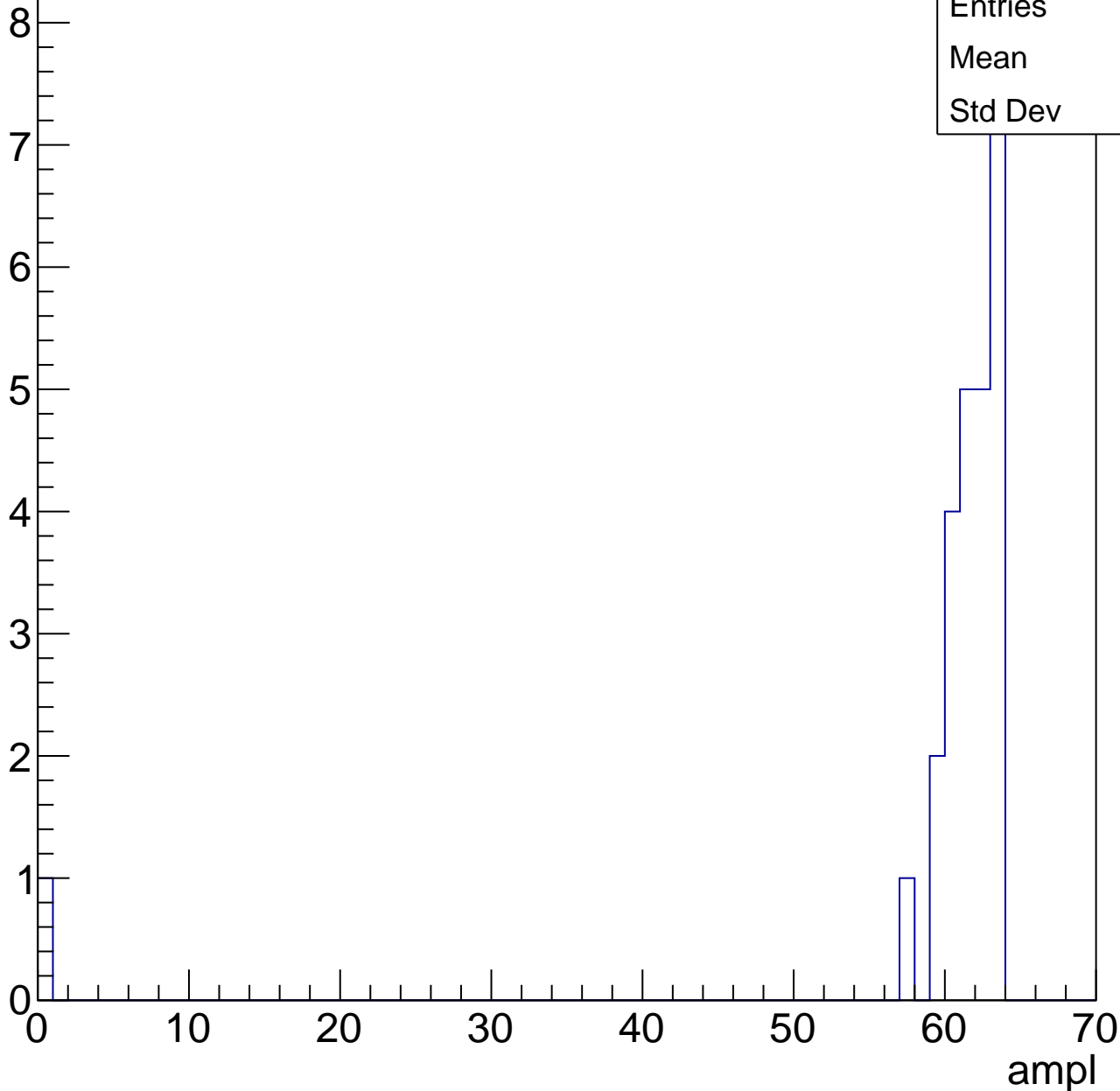


# B1L003S, U6-ch126, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	26
Mean	59
Std Dev	11.9





# B1L003S, U6-ch126, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U6-ch127, adc0

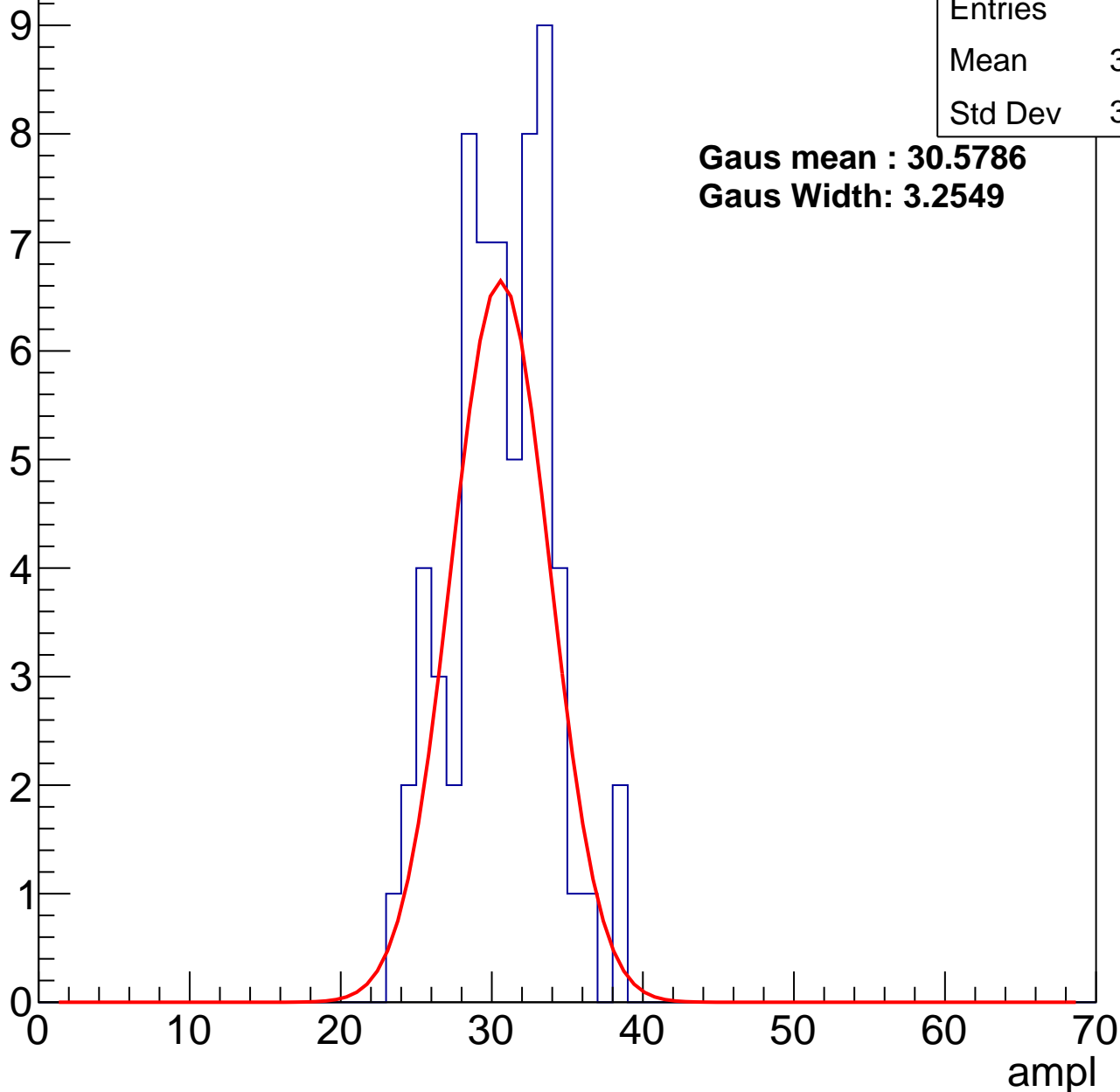
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	30.17
Std Dev	3.296

**Gaus mean : 30.5786**

**Gaus Width: 3.2549**



# B1L003S, U6-ch127, adc1

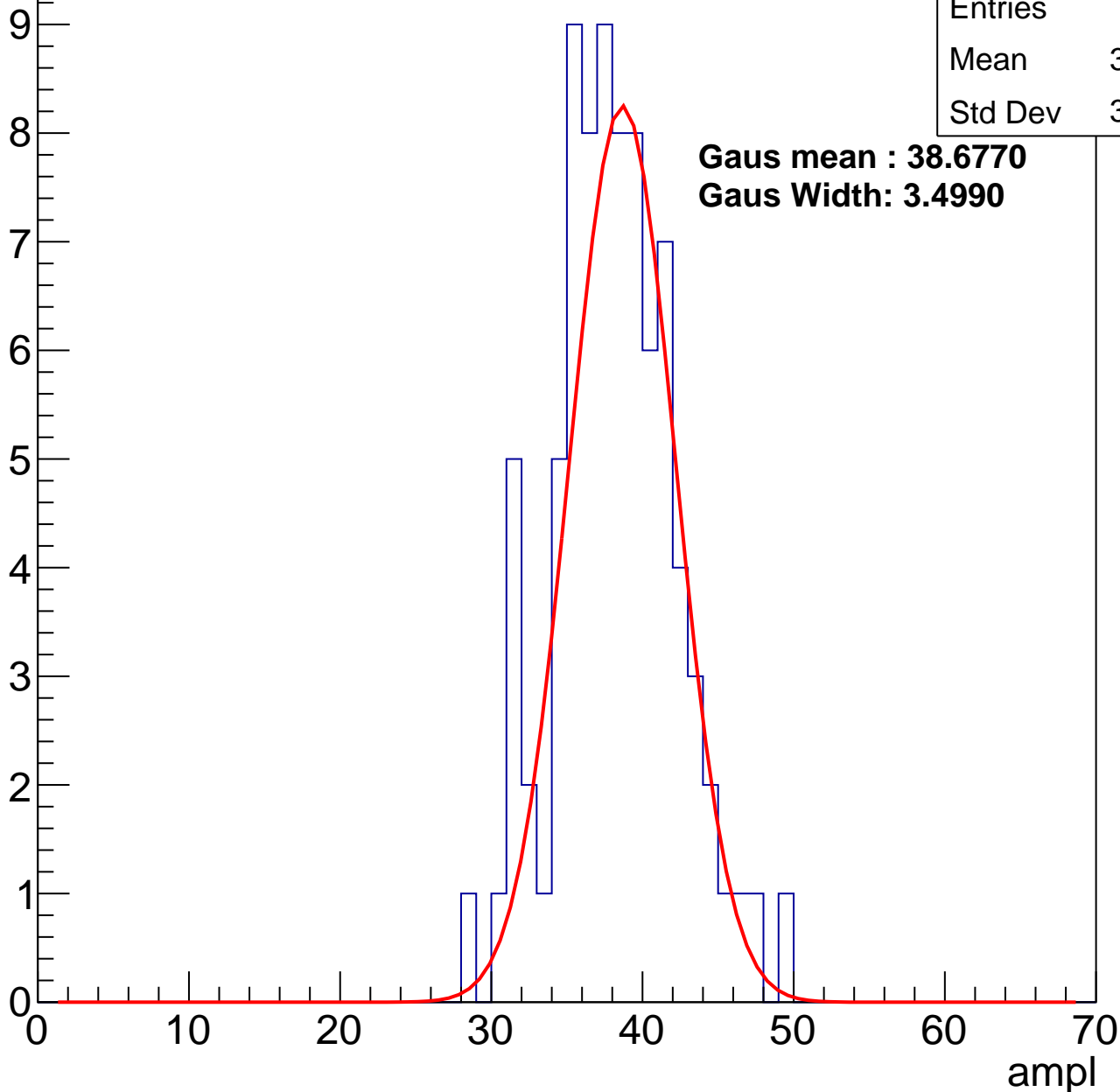
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	83
Mean	37.72
Std Dev	3.992

**Gaus mean : 38.6770**

**Gaus Width: 3.4990**



# B1L003S, U6-ch127, adc2

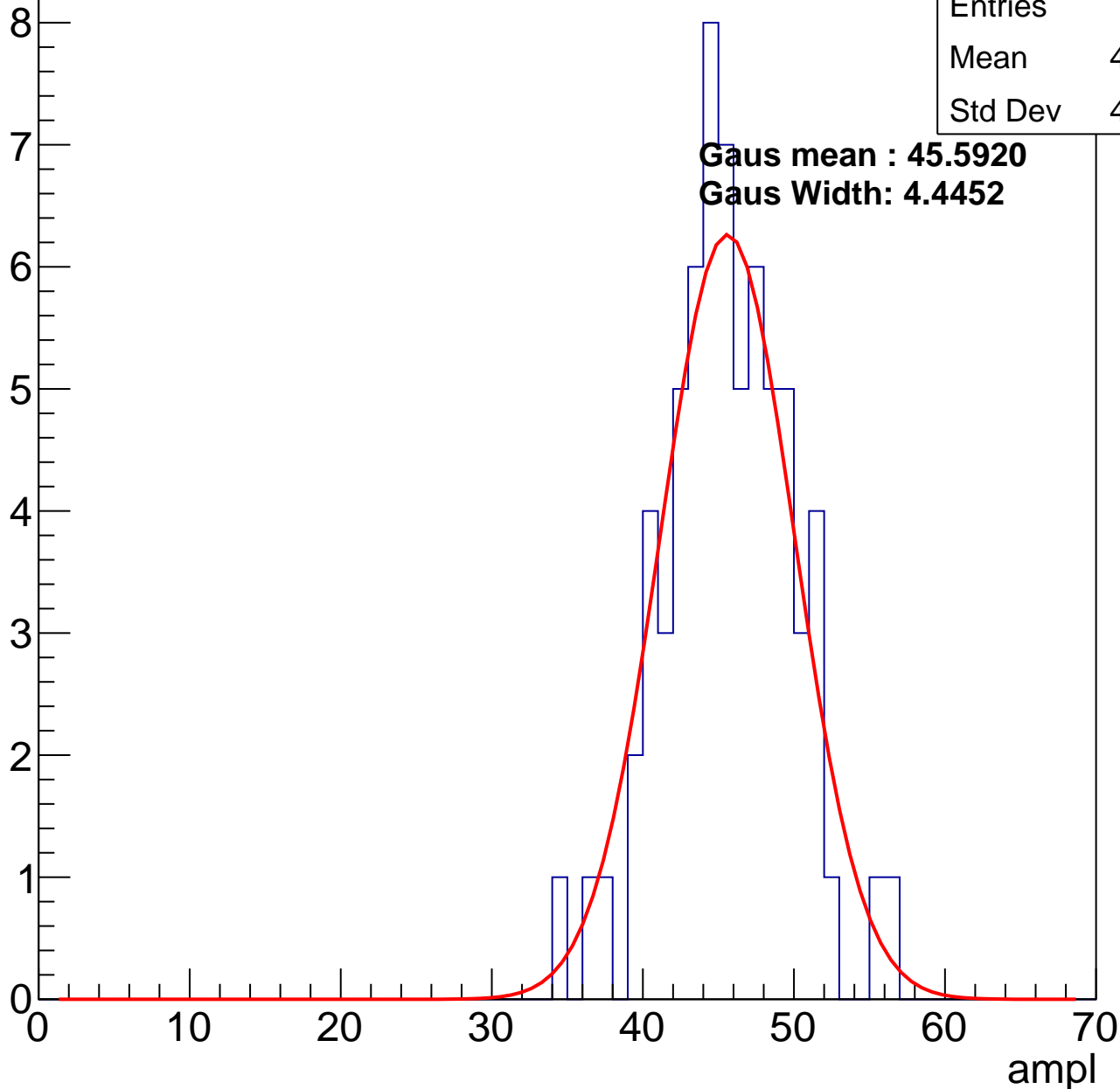
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	45.17
Std Dev	4.177

**Gaus mean : 45.5920**

**Gaus Width: 4.4452**

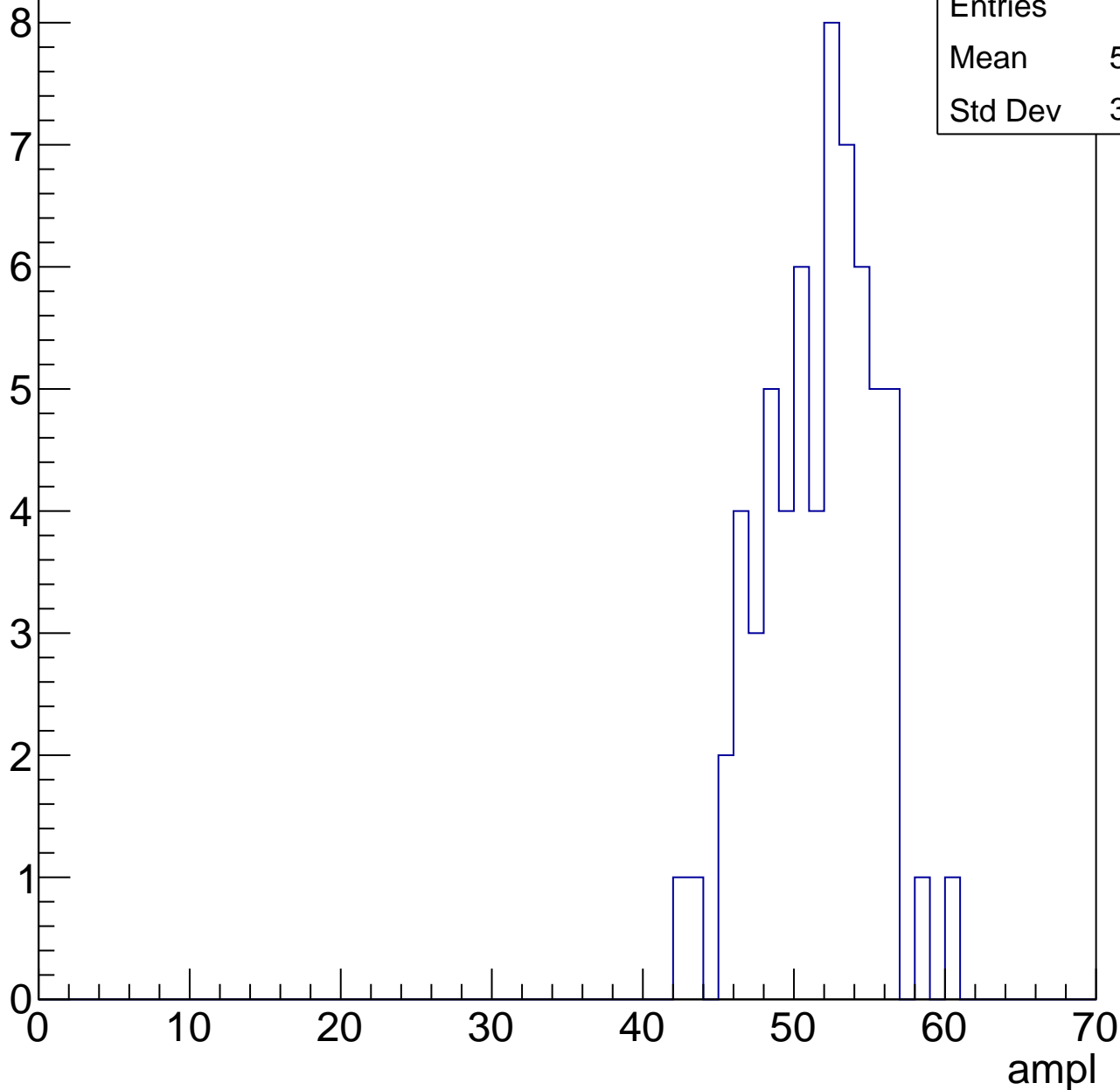


# B1L003S, U6-ch127, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	51.17
Std Dev	3.684

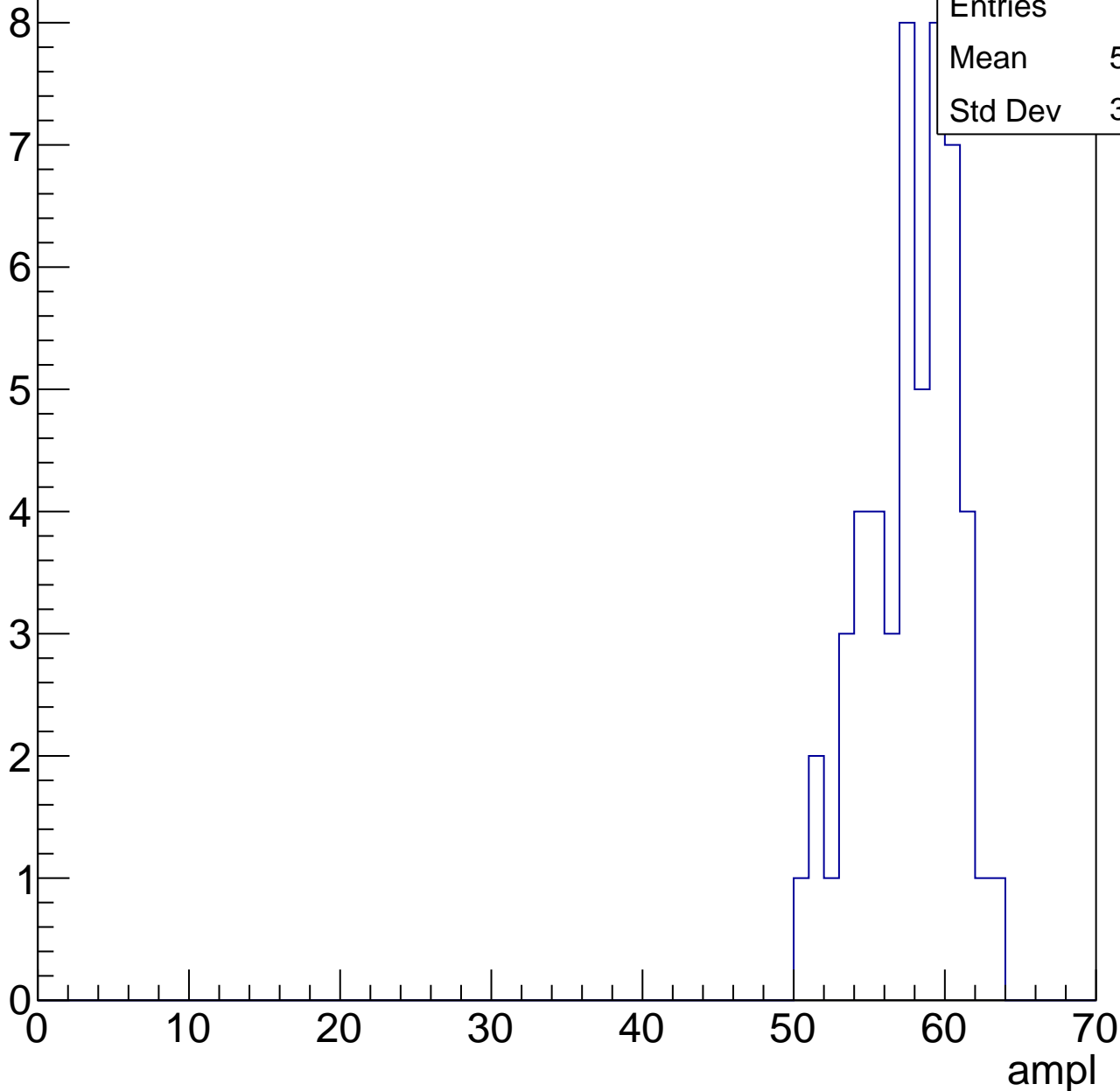


# B1L003S, U6-ch127, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	52
Mean	57.19
Std Dev	3.013

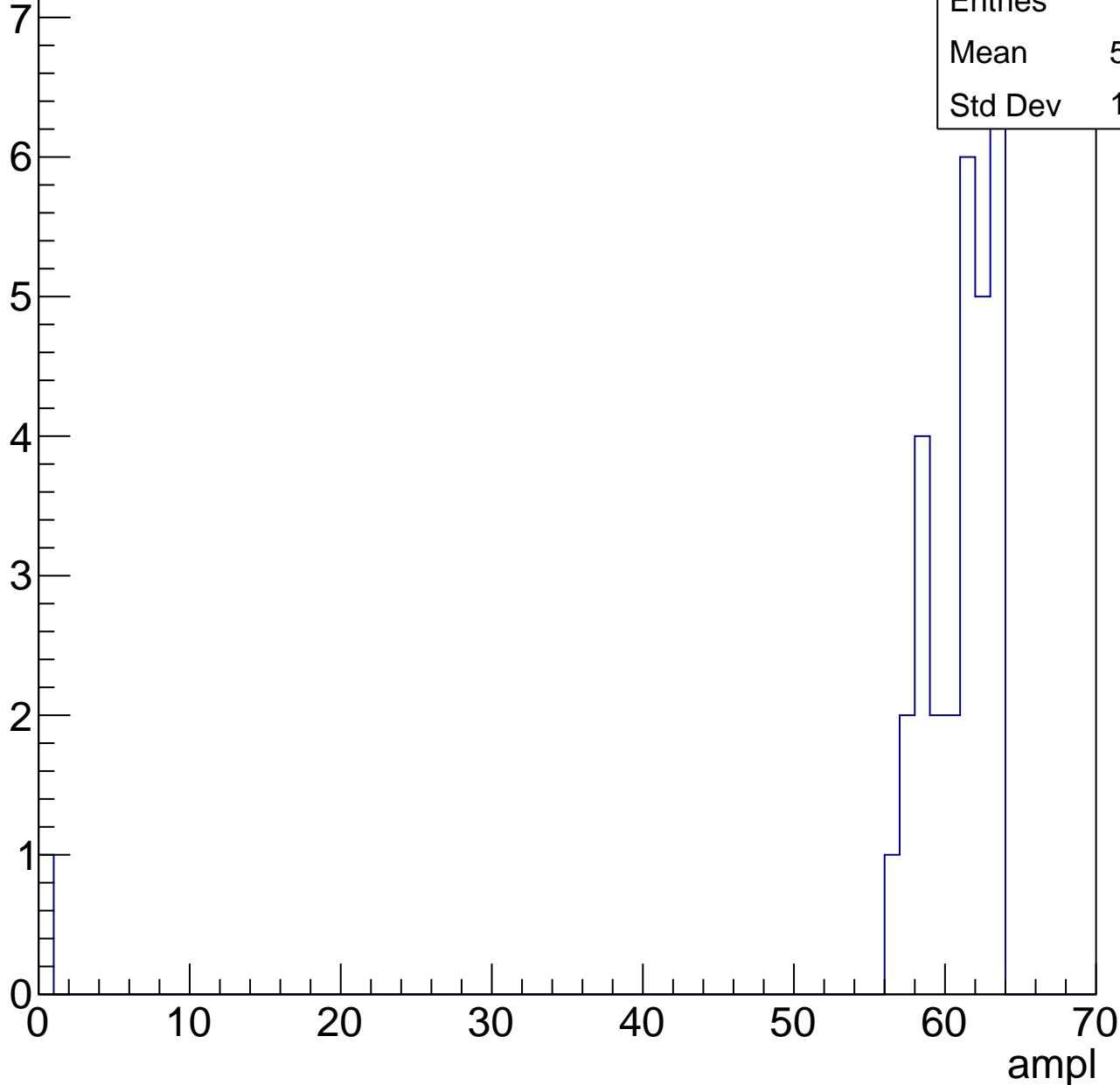


# B1L003S, U6-ch127, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

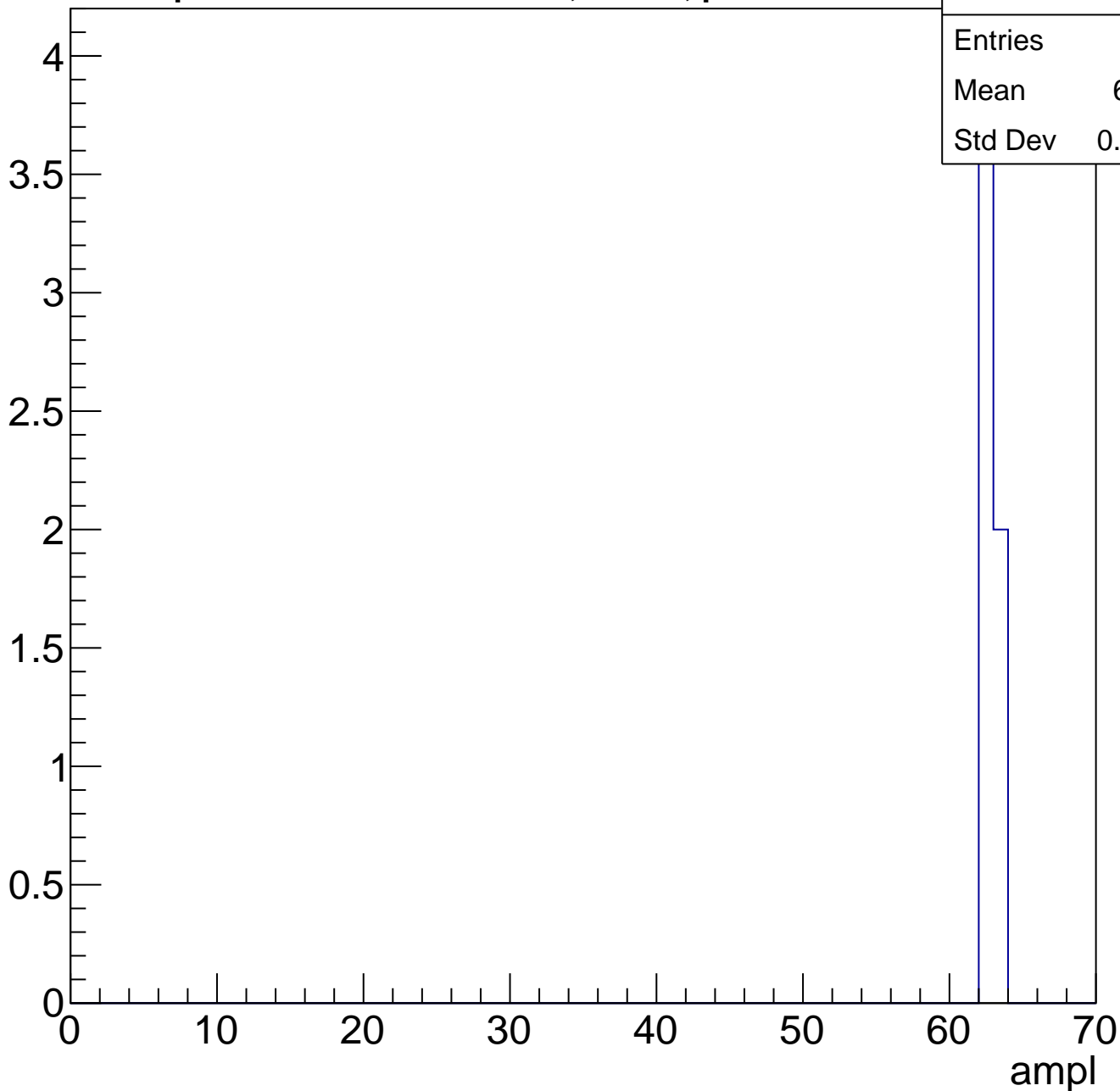
Entries	30
Mean	58.57
Std Dev	11.07



# B1L003S, U6-ch127, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U6-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

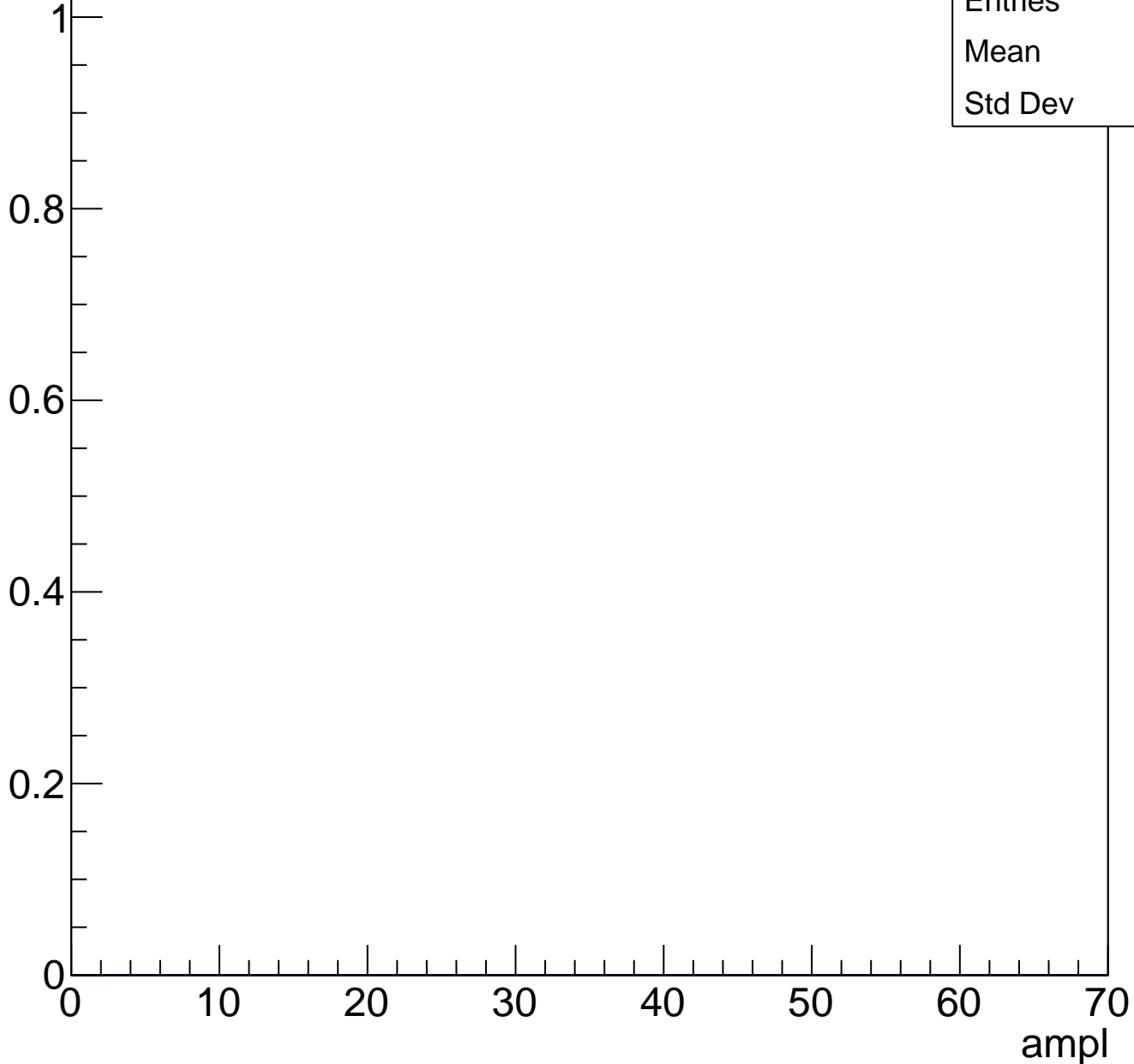


Entries	0
Mean	0
Std Dev	0

# B1L003S, U6-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0