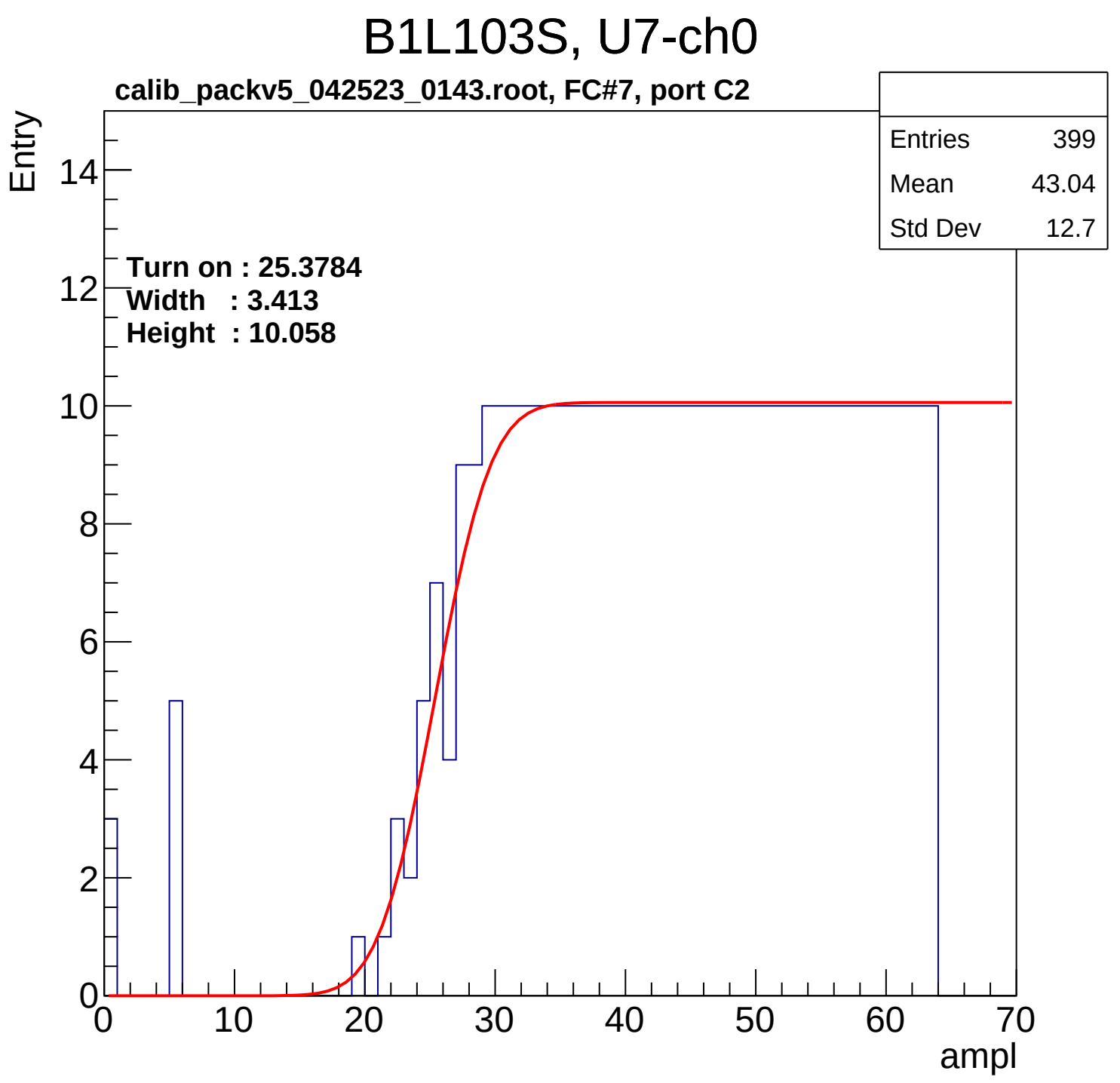
B1L103S, U7-ch0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 399
Mean 43.04
Std Dev 12.7
Turn on : 25.3784
Width : 3.413
Height : 10.058
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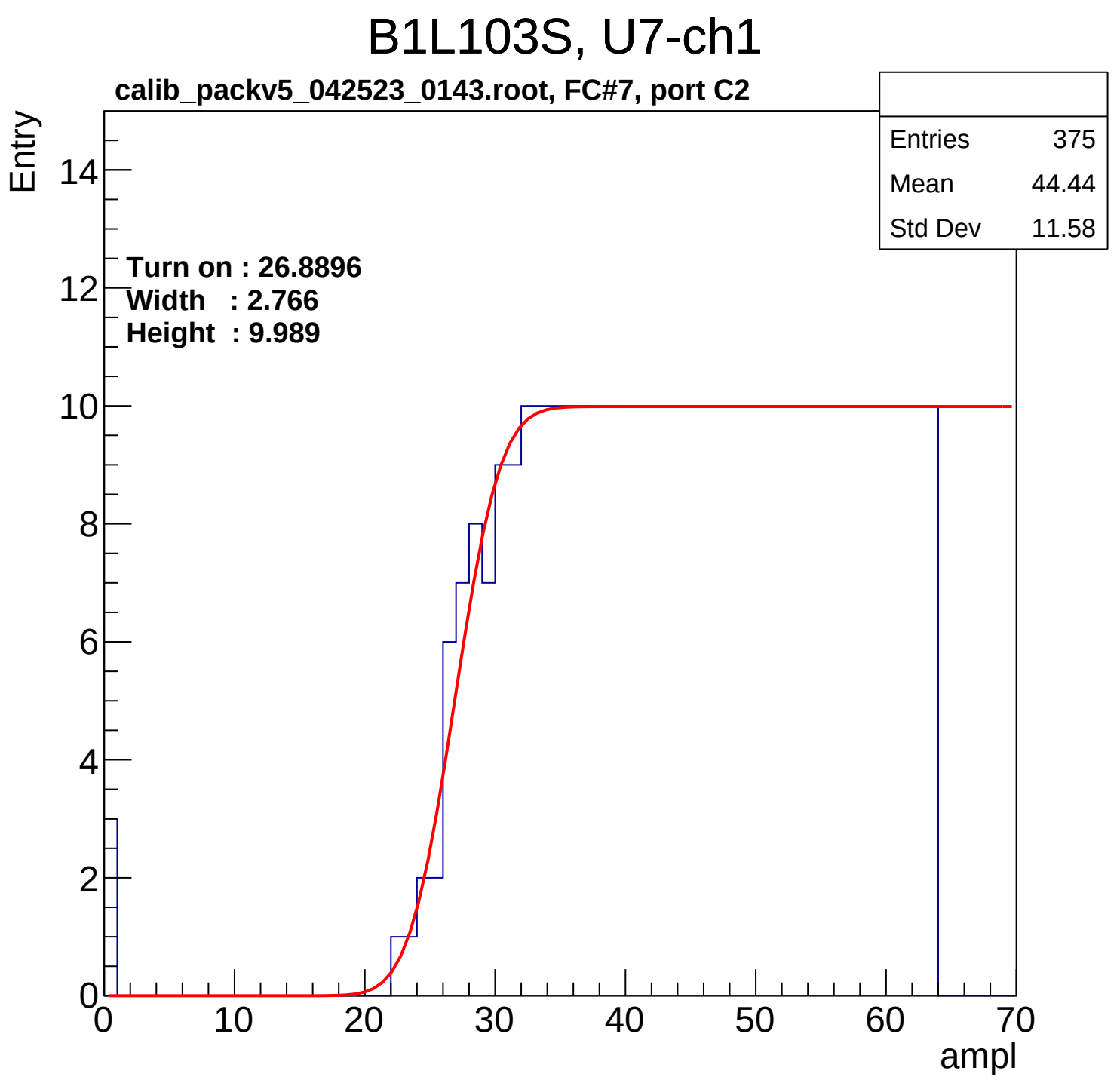
B1L103S, U7-ch1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 375
Mean 44.44
Std Dev 11.58
Turn on : 26.8896
Width : 2.766
Height : 9.989
Entry
ampl
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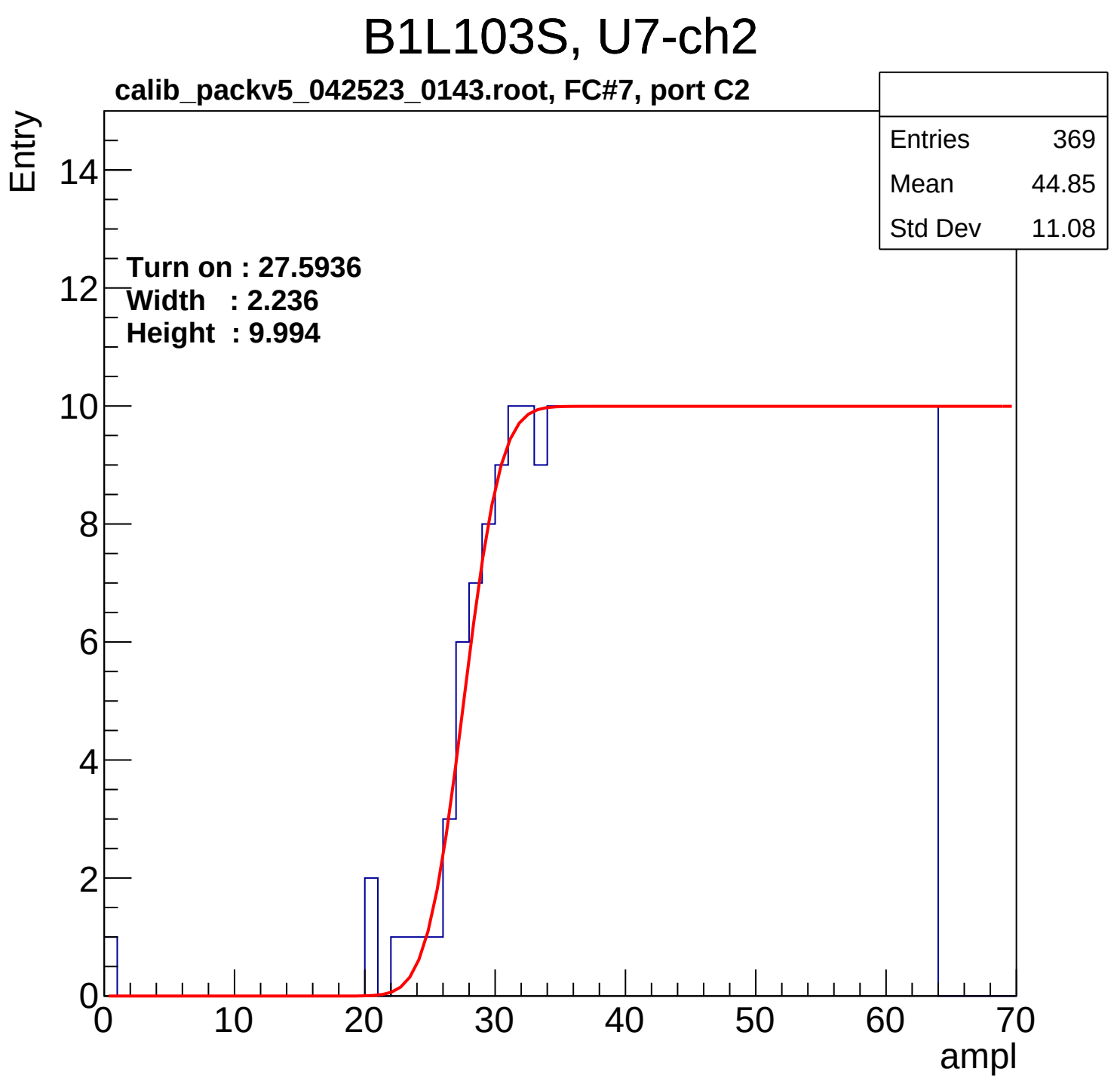
B1L103S, U7-ch2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 369
Mean 44.85
Std Dev 11.08
Turn on : 27.5936
Width : 2.236
Height : 9.994
Entry
ampl
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2
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6
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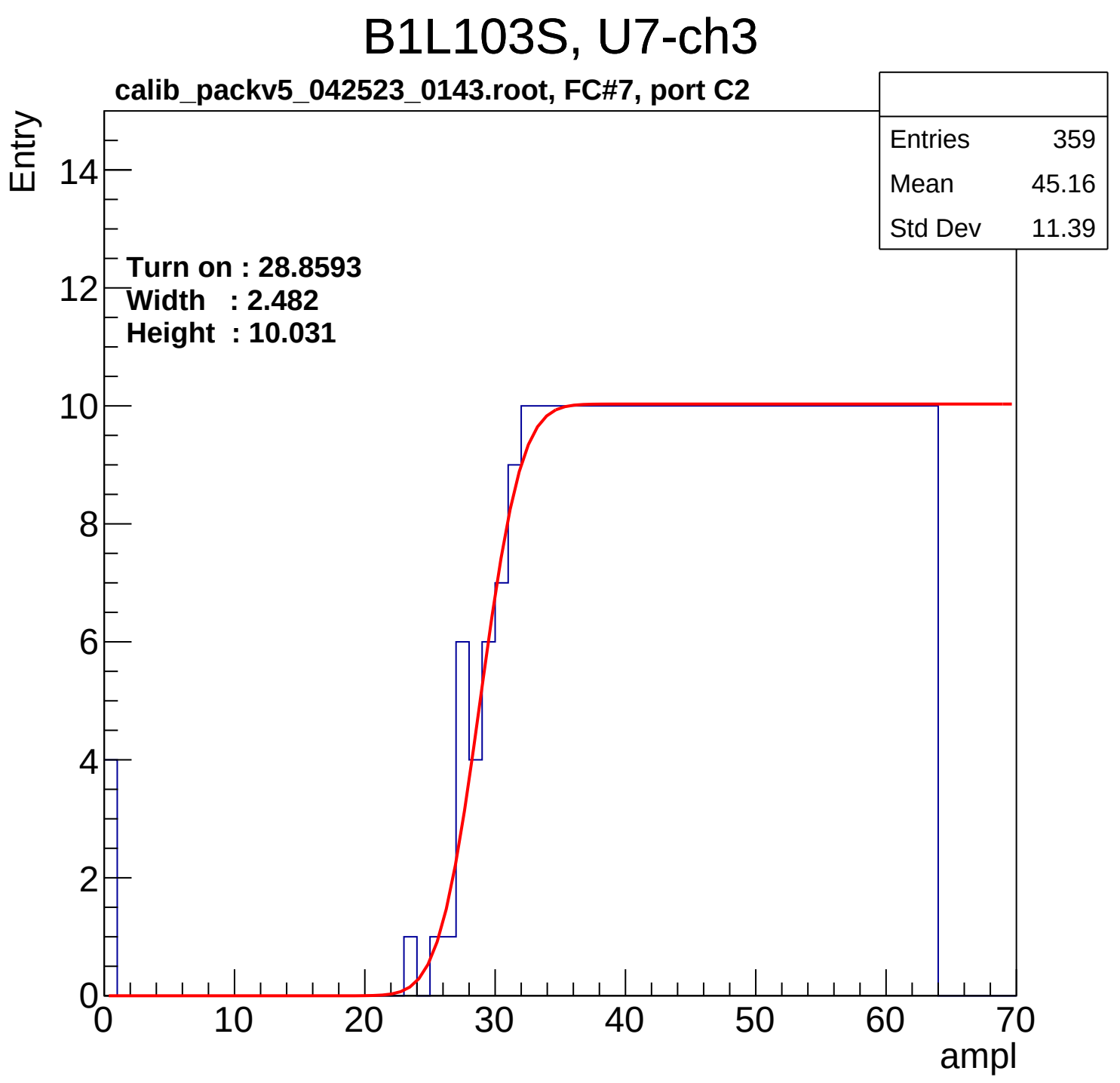
B1L103S, U7-ch3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 359
Mean 45.16
Std Dev 11.39
Turn on : 28.8593
Width : 2.482
Height : 10.031
Entry
ampl
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2
4
6
8
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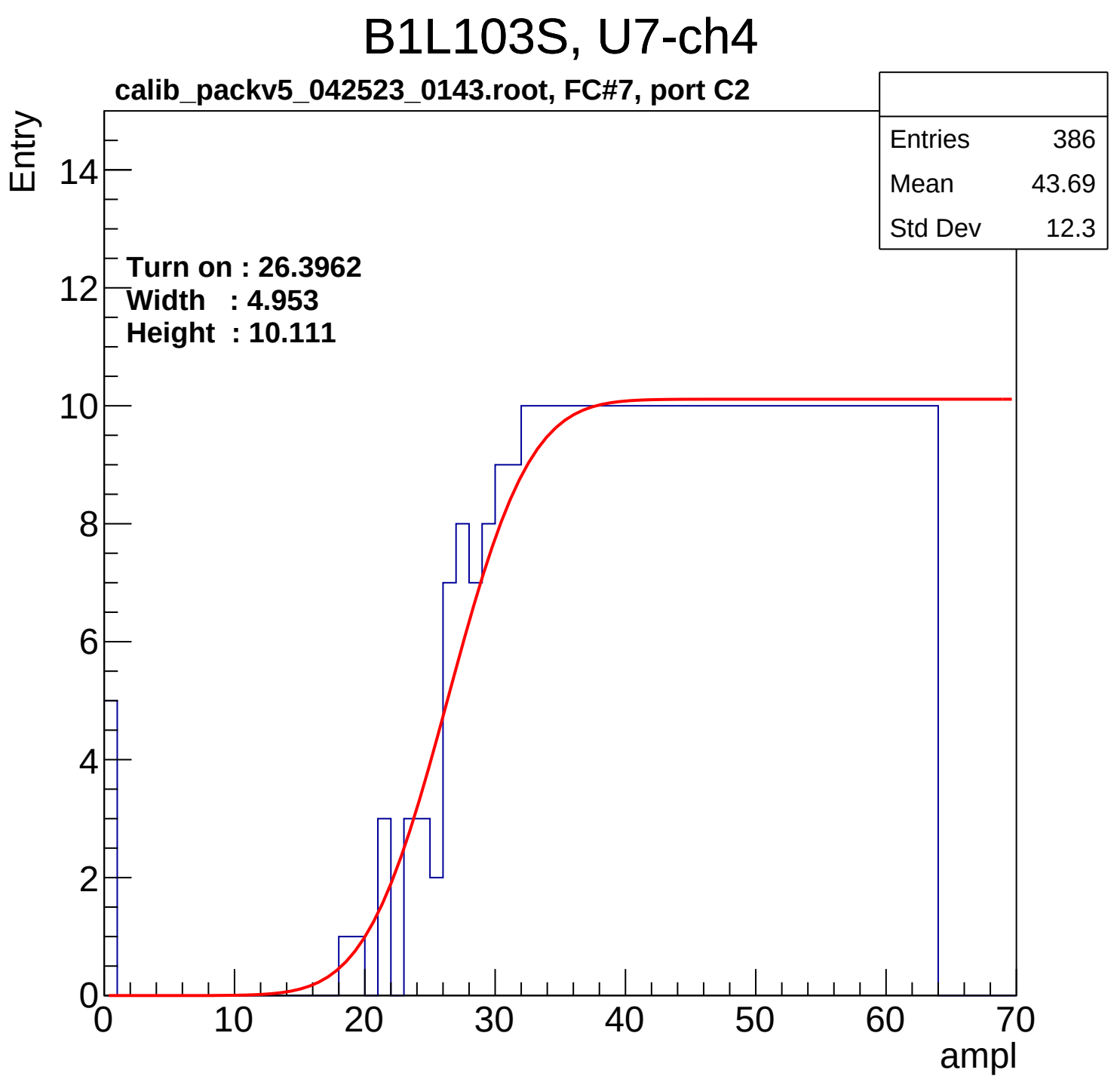
B1L103S, U7-ch4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 386
Mean 43.69
Std Dev 12.3
Turn on : 26.3962
Width : 4.953
Height : 10.111
Entry
ampl
0
2
4
6
8
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0
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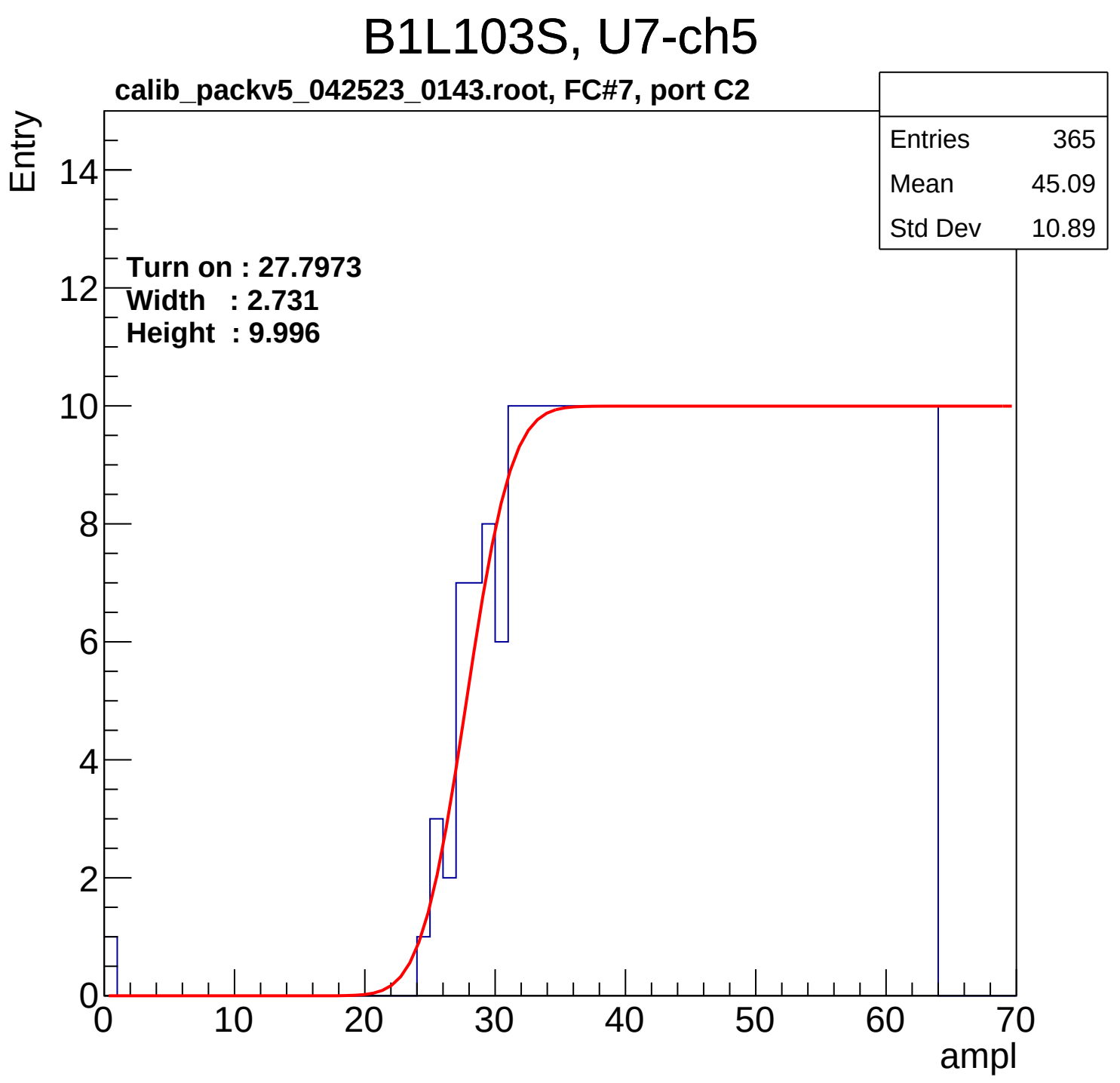
B1L103S, U7-ch5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 365
Mean 45.09
Std Dev 10.89
Turn on : 27.7973
Width : 2.731
Height : 9.996
Entry
ampl
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2
4
6
8
10
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0
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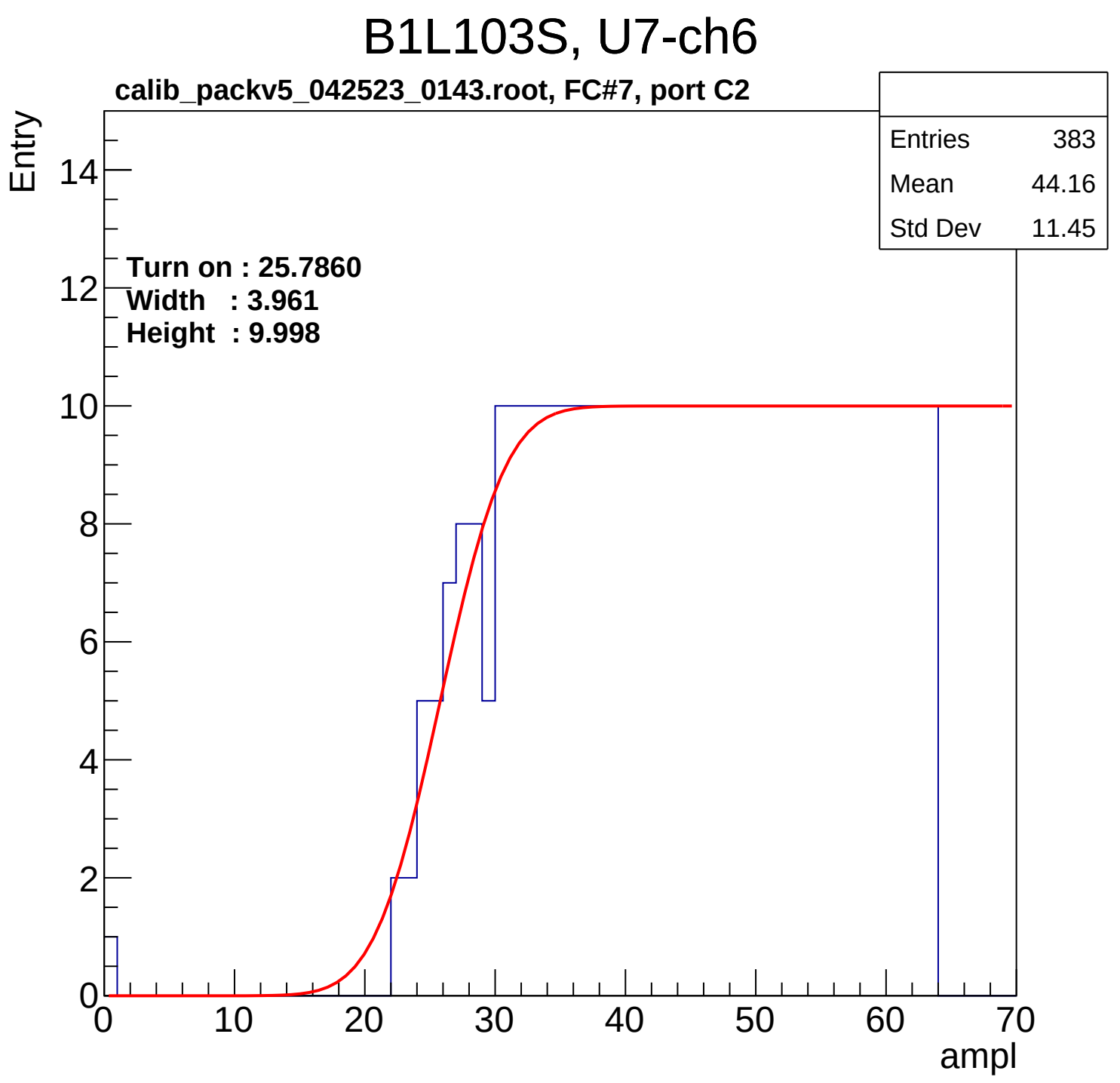
B1L103S, U7-ch6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 383
Mean 44.16
Std Dev 11.45
Turn on : 25.7860
Width : 3.961
Height : 9.998
Entry
ampl
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2
4
6
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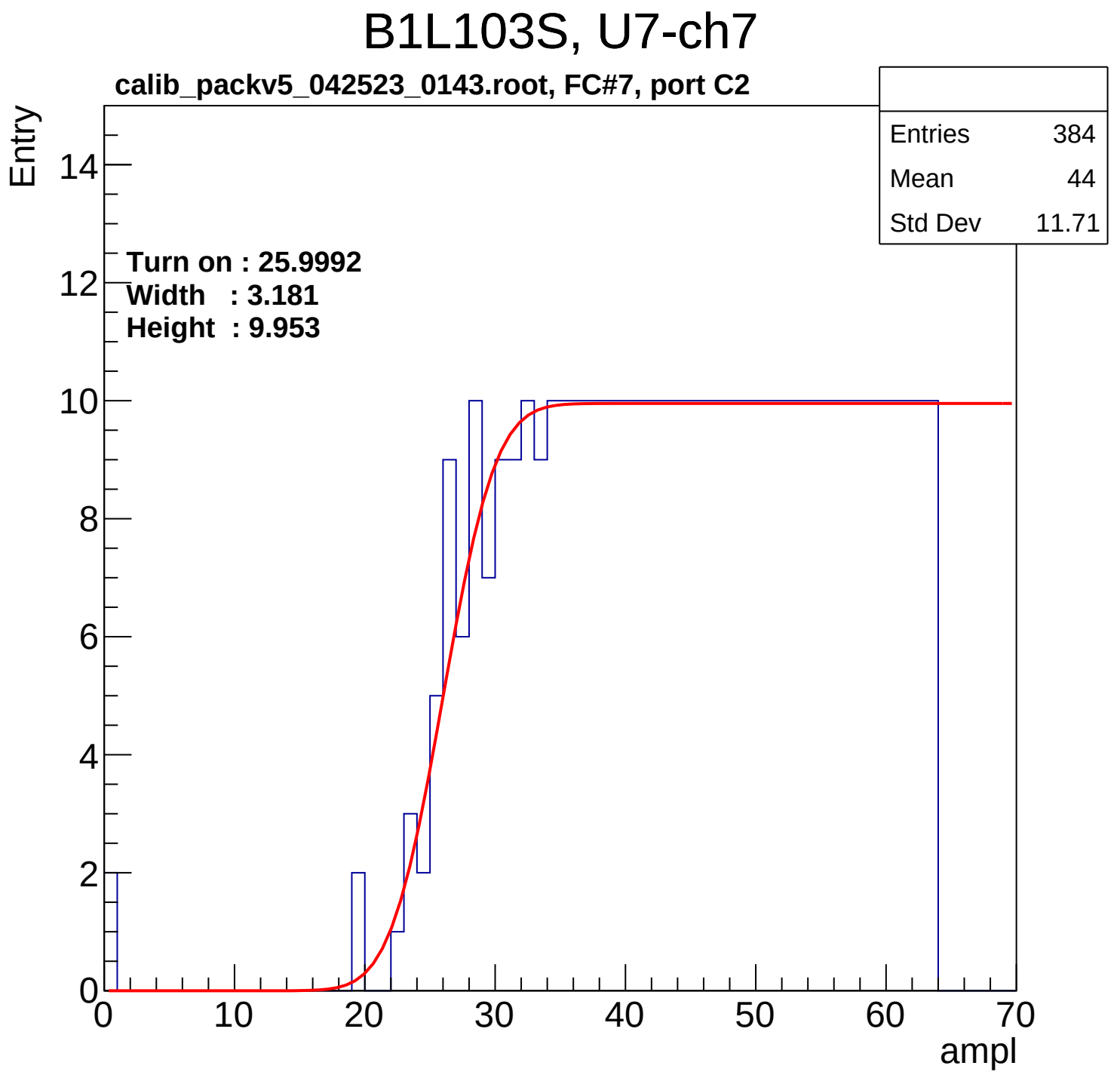
B1L103S, U7-ch7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 384
Mean 44
Std Dev 11.71
Turn on : 25.9992
Width : 3.181
Height : 9.953
Entry
ampl
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2
4
6
8
10
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0
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60
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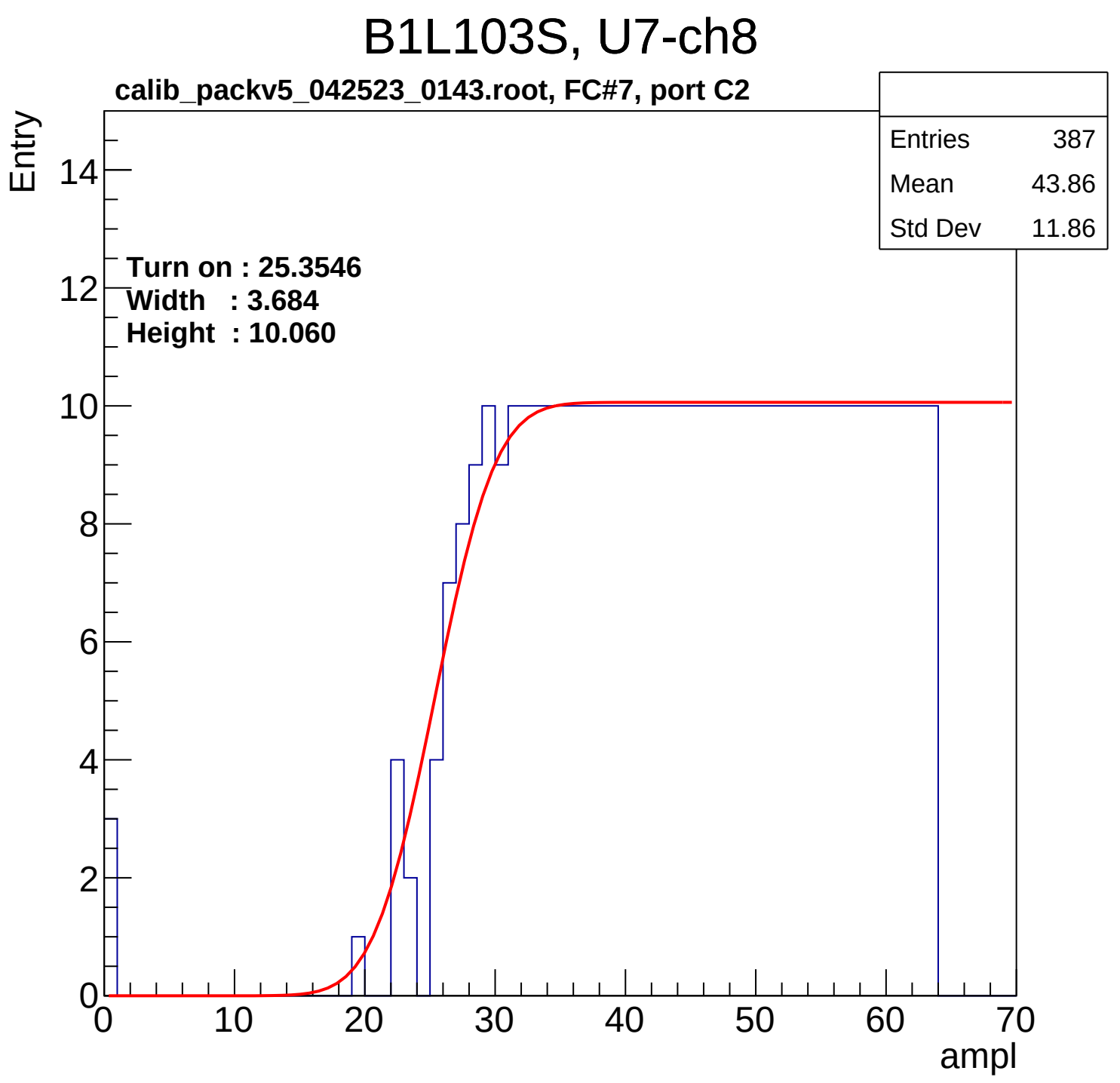
B1L103S, U7-ch8
calib_packv5_042523_0143.root, FC#7, port C2
Entries 387
Mean 43.86
Std Dev 11.86
Turn on : 25.3546
Width : 3.684
Height : 10.060
Entry
ampl
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6
8
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12
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0
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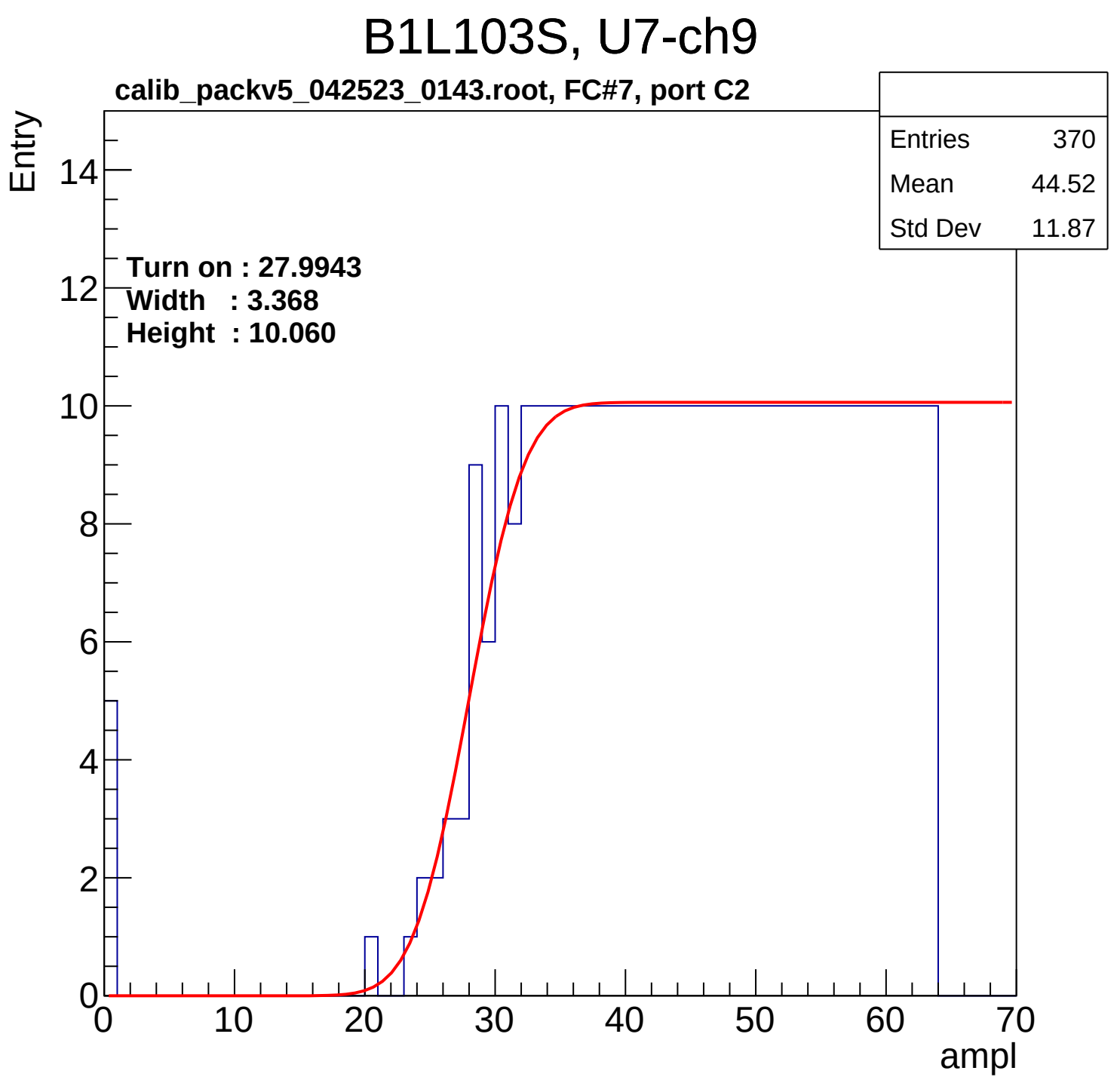
B1L103S, U7-ch9
calib_packv5_042523_0143.root, FC#7, port C2
Entries 370
Mean 44.52
Std Dev 11.87
Turn on : 27.9943
Width : 3.368
Height : 10.060
Entry
ampl
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4
6
8
10
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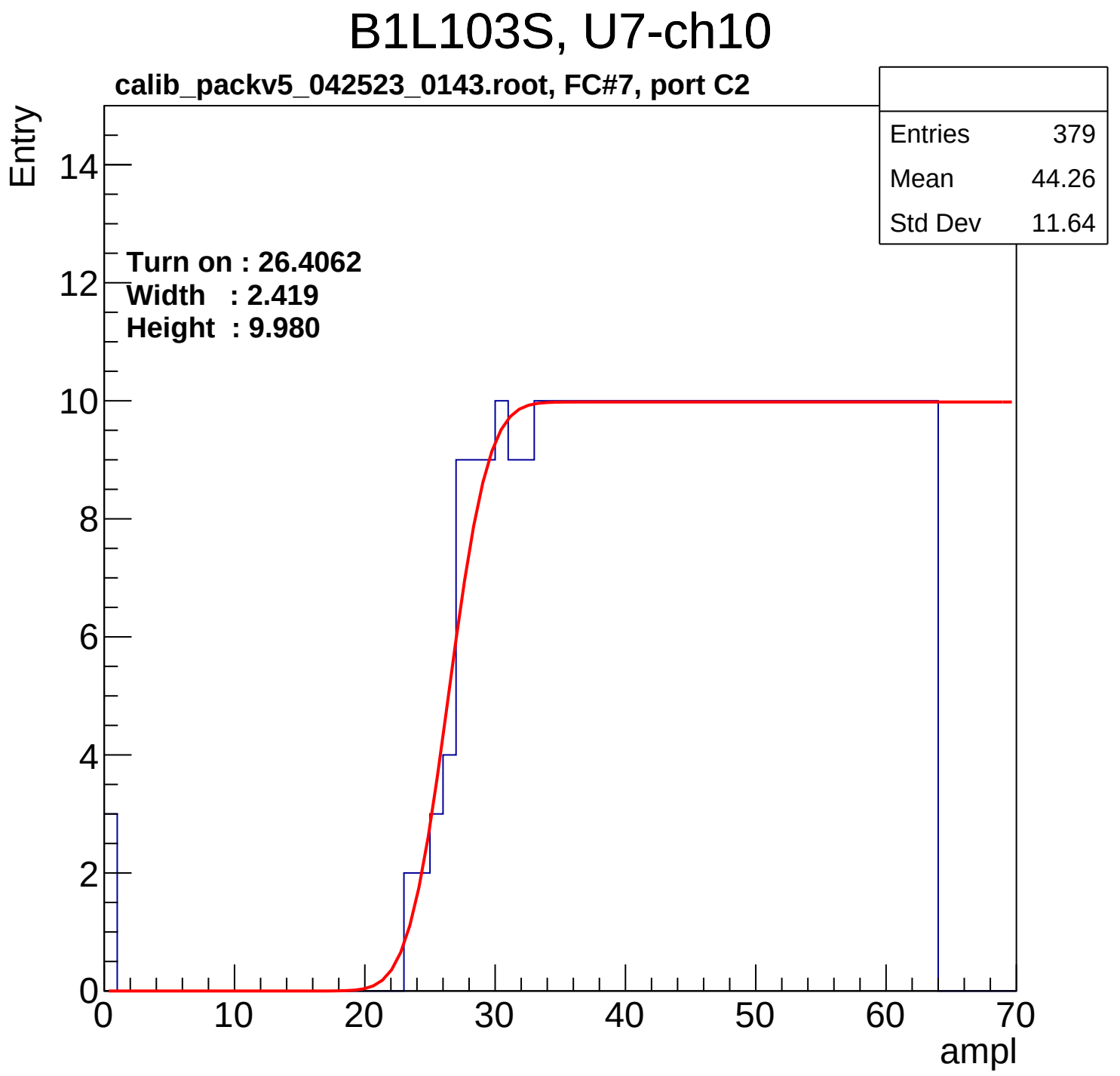
B1L103S, U7-ch10
calib_packv5_042523_0143.root, FC#7, port C2
Entries 379
Mean 44.26
Std Dev 11.64
Turn on : 26.4062
Width : 2.419
Height : 9.980
Entry
ampl
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2
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6
8
10
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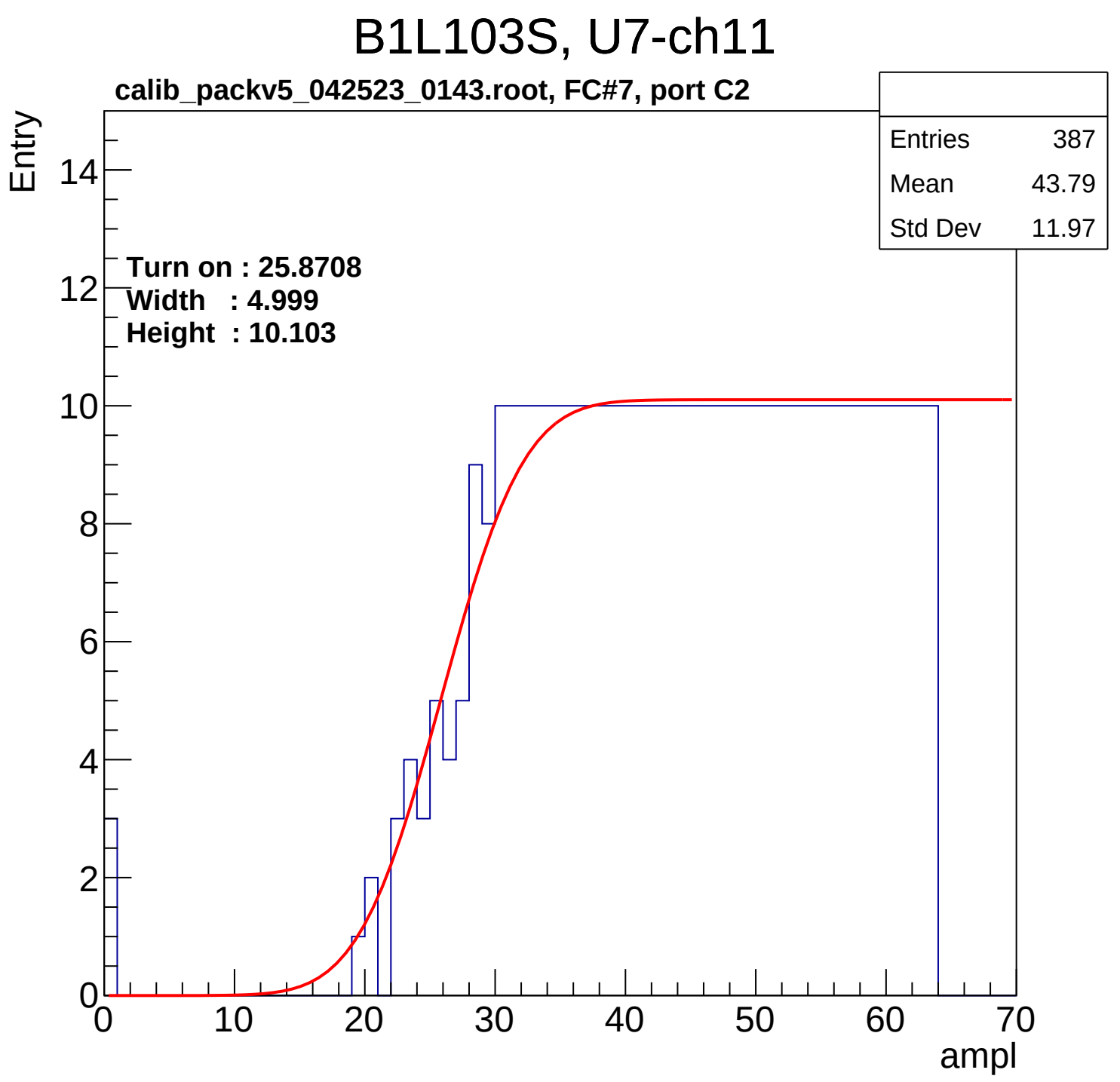
B1L103S, U7-ch11
calib_packv5_042523_0143.root, FC#7, port C2
Entries 387
Mean 43.79
Std Dev 11.97
Turn on : 25.8708
Width : 4.999
Height : 10.103
Entry
ampl
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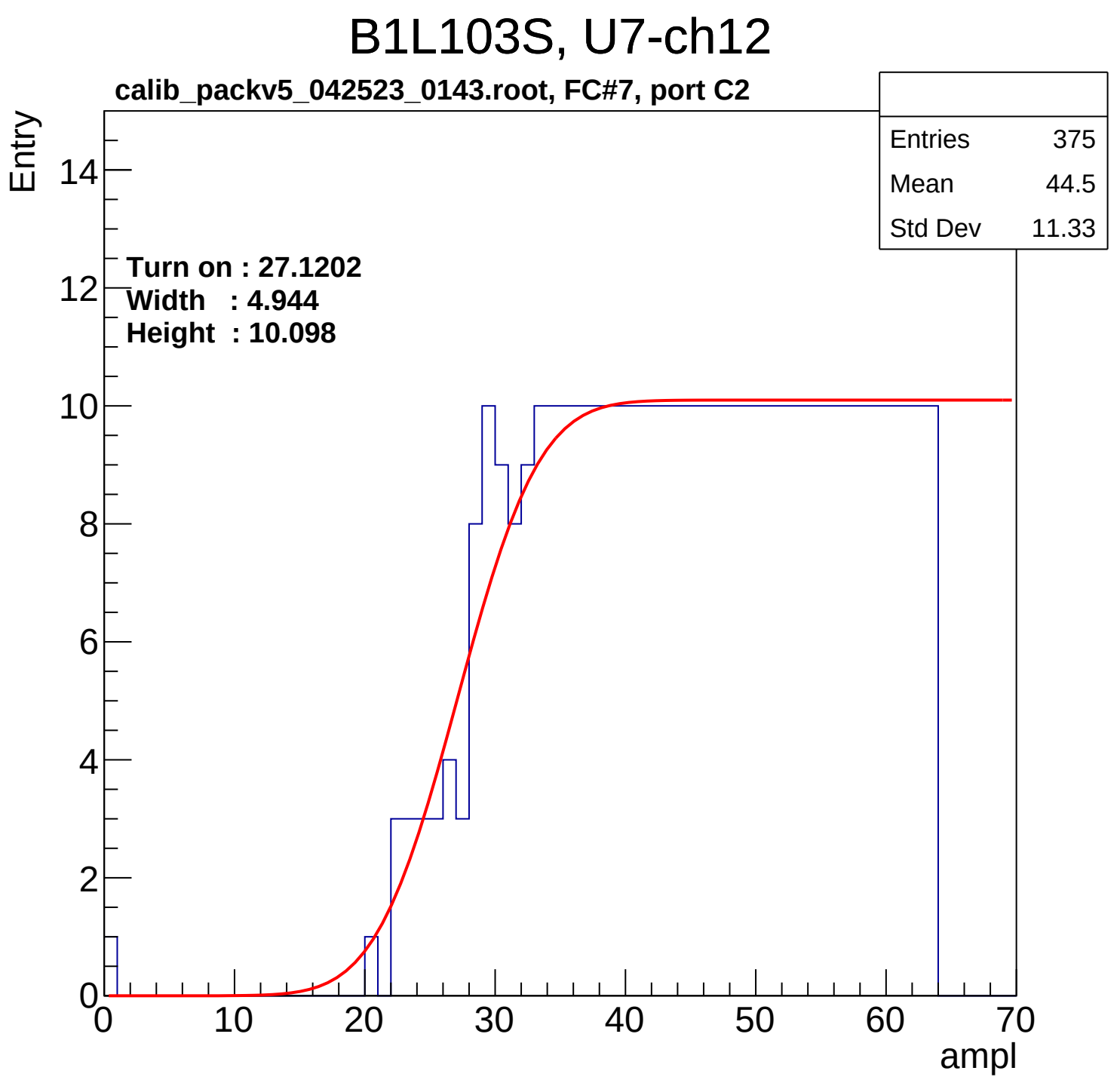
B1L103S, U7-ch12
calib_packv5_042523_0143.root, FC#7, port C2
Entries 375
Mean 44.5
Std Dev 11.33
Turn on : 27.1202
Width : 4.944
Height : 10.098
Entry
ampl
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6
8
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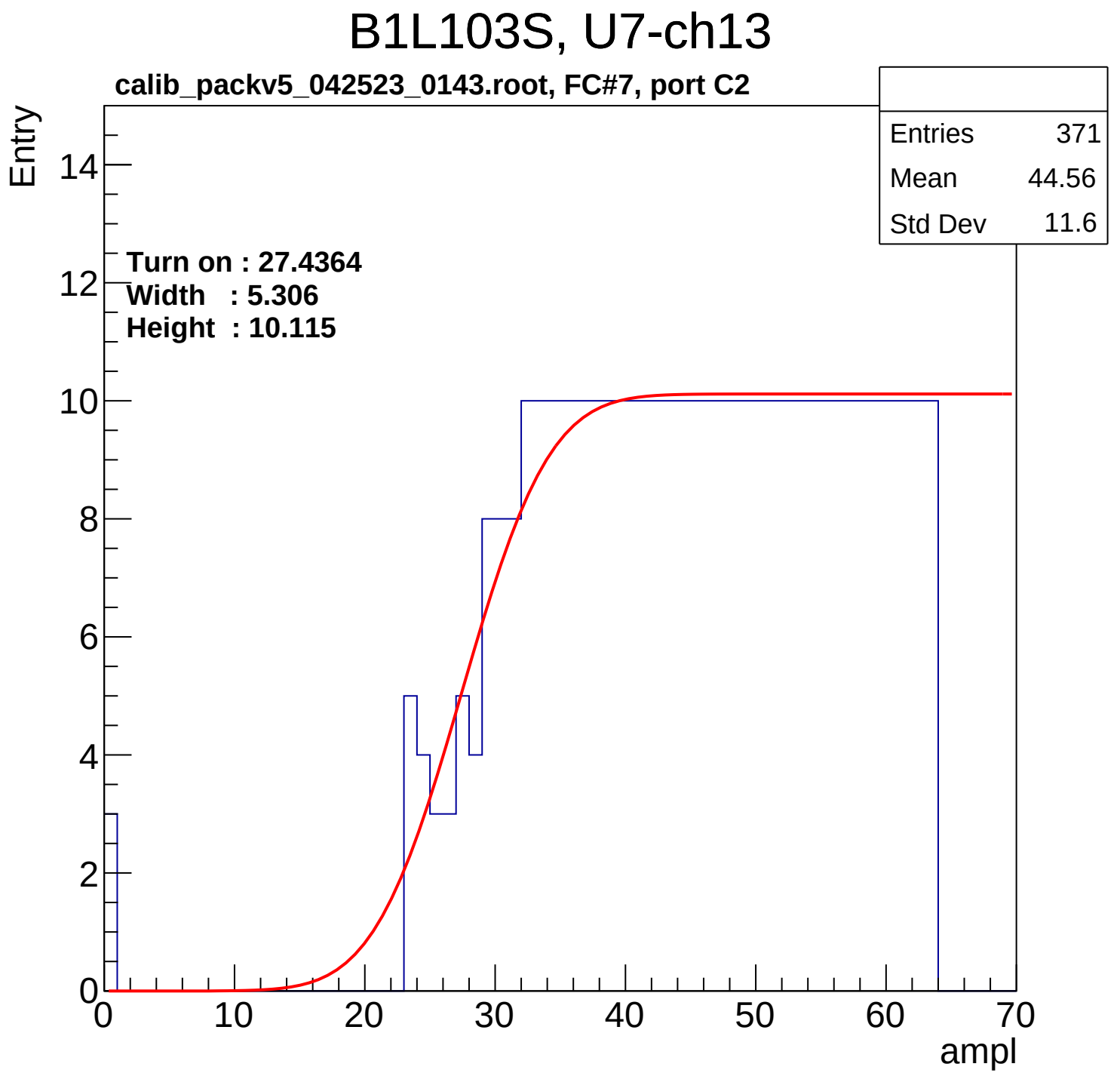
B1L103S, U7-ch13
calib_packv5_042523_0143.root, FC#7, port C2
Entries 371
Mean 44.56
Std Dev 11.6
Turn on : 27.4364
Width : 5.306
Height : 10.115
Entry
ampl
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8
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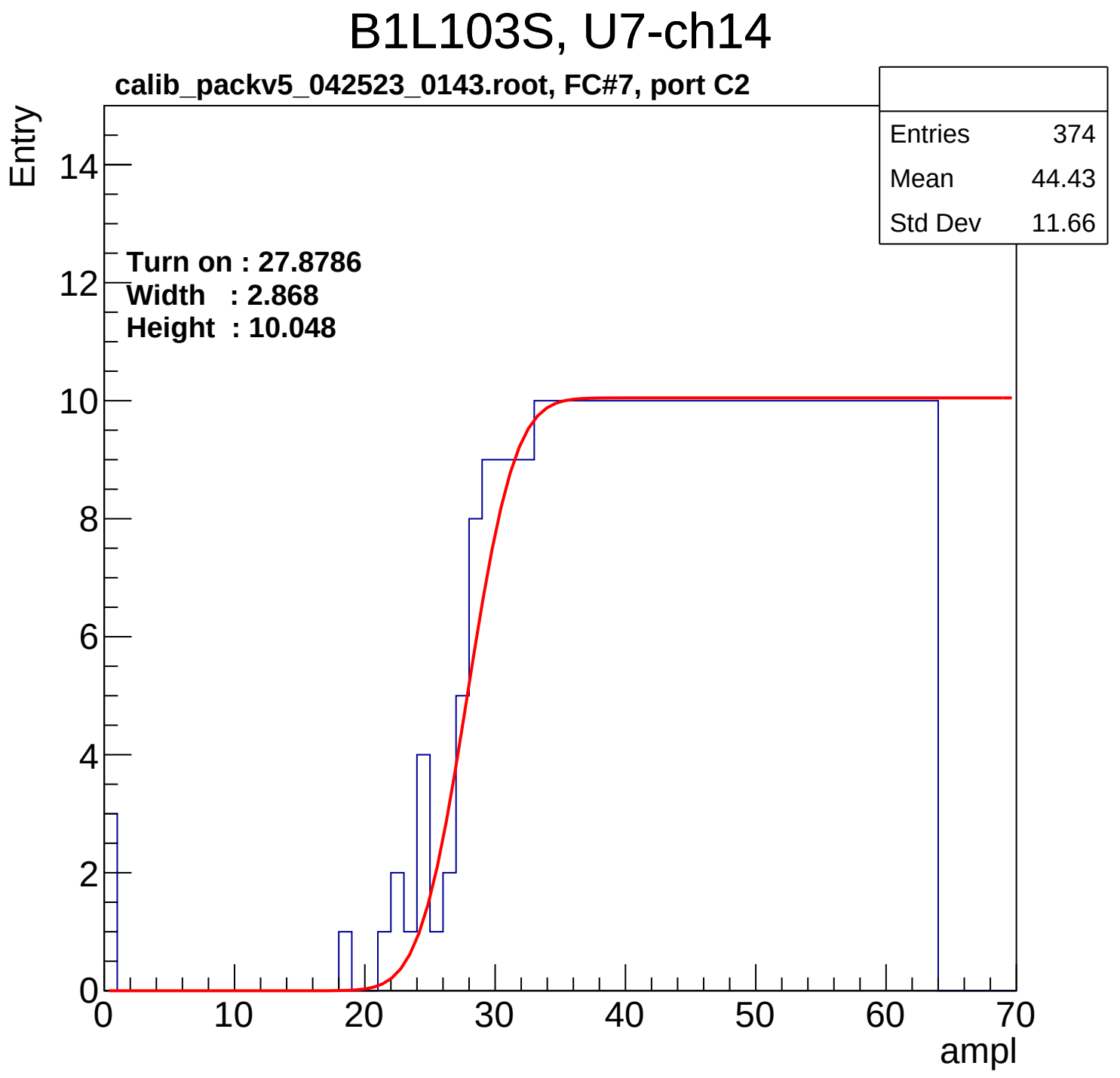
B1L103S, U7-ch14
calib_packv5_042523_0143.root, FC#7, port C2
Entries 374
Mean 44.43
Std Dev 11.66
Turn on : 27.8786
Width : 2.868
Height : 10.048
Entry
ampl
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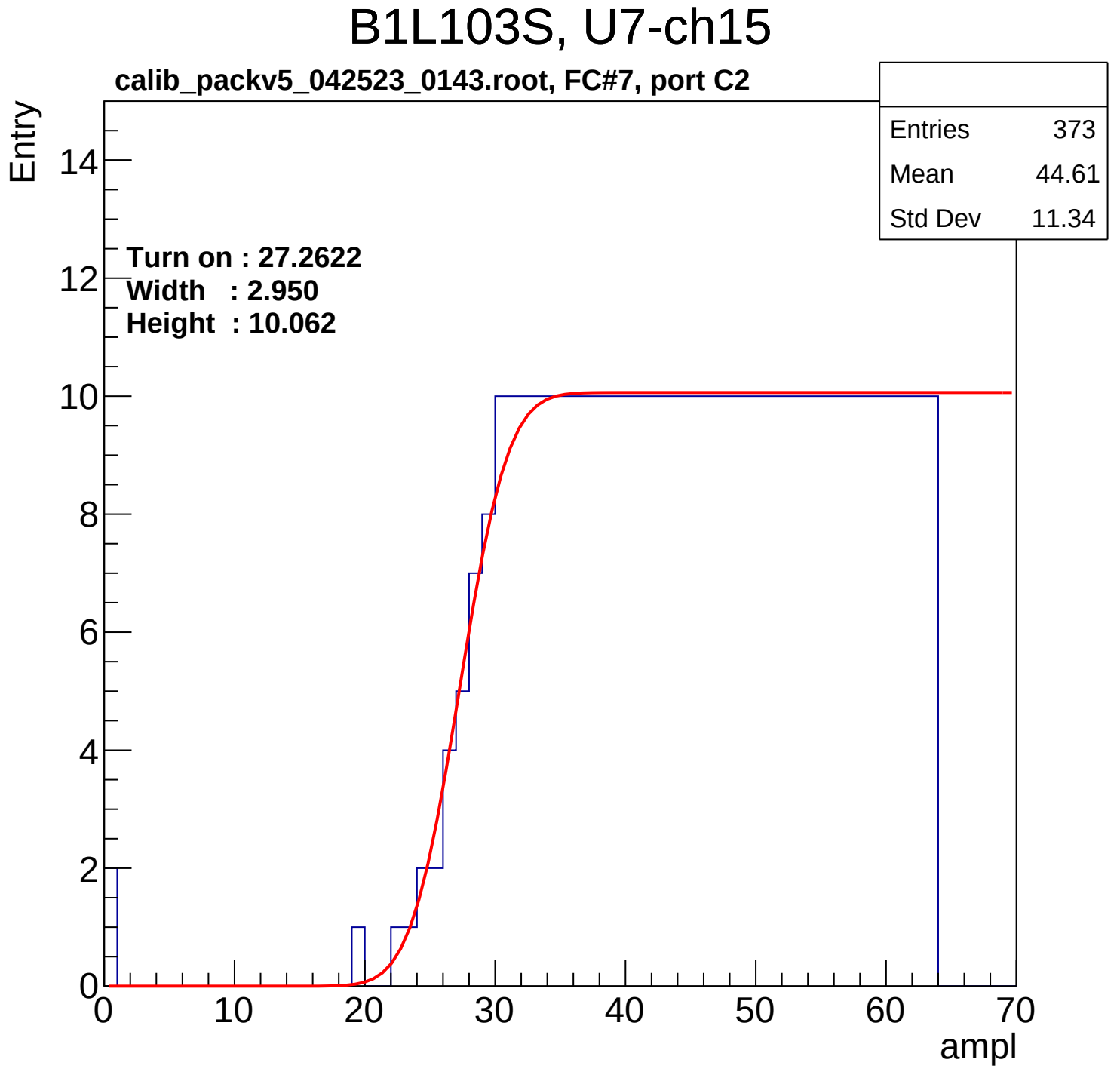
B1L103S, U7-ch15
calib_packv5_042523_0143.root, FC#7, port C2
Entries 373
Mean 44.61
Std Dev 11.34
Turn on : 27.2622
Width : 2.950
Height : 10.062
Entry
ampl
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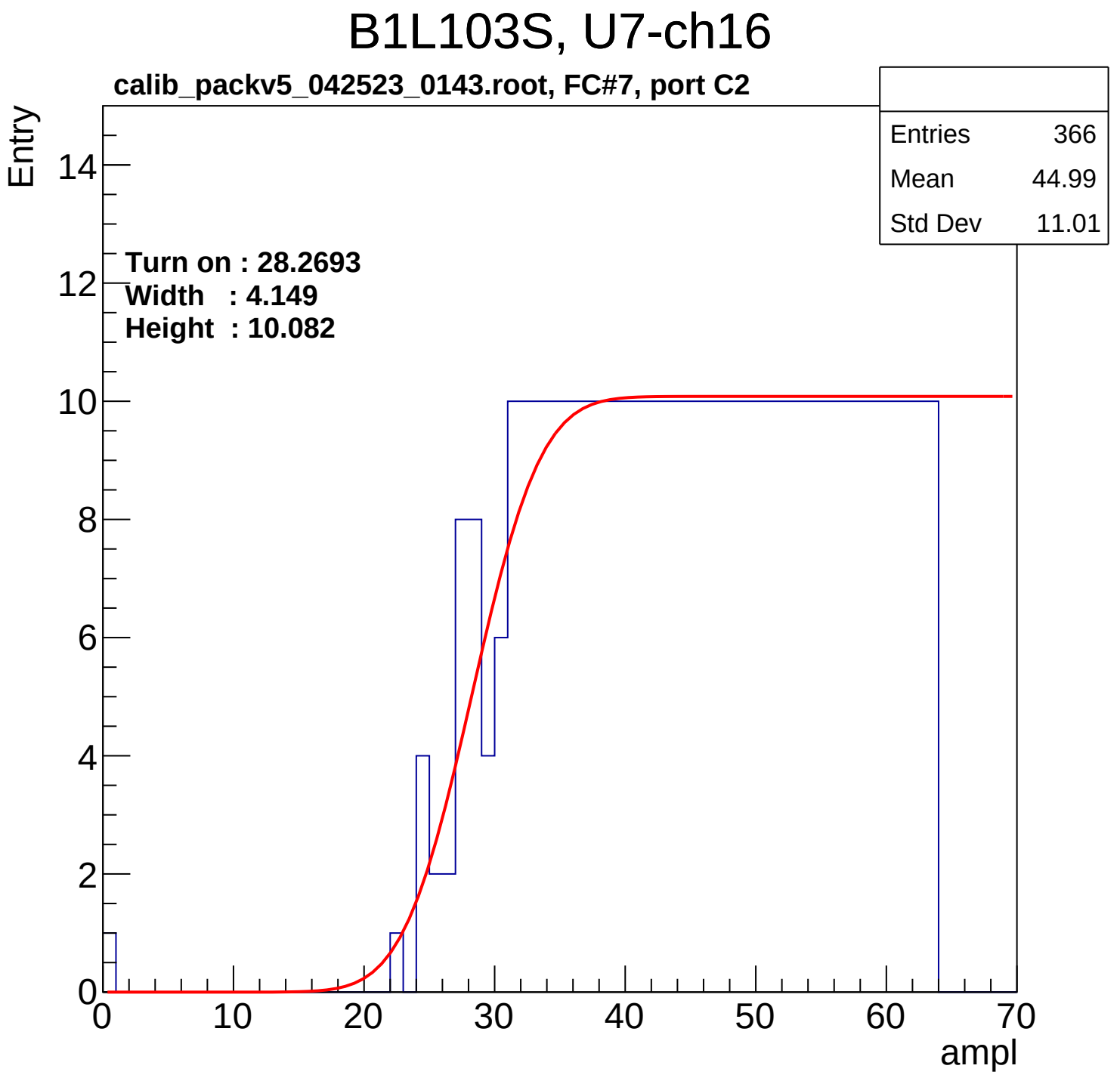
B1L103S, U7-ch16
calib_packv5_042523_0143.root, FC#7, port C2
Entries 366
Mean 44.99
Std Dev 11.01
Turn on : 28.2693
Width : 4.149
Height : 10.082
Entry
ampl
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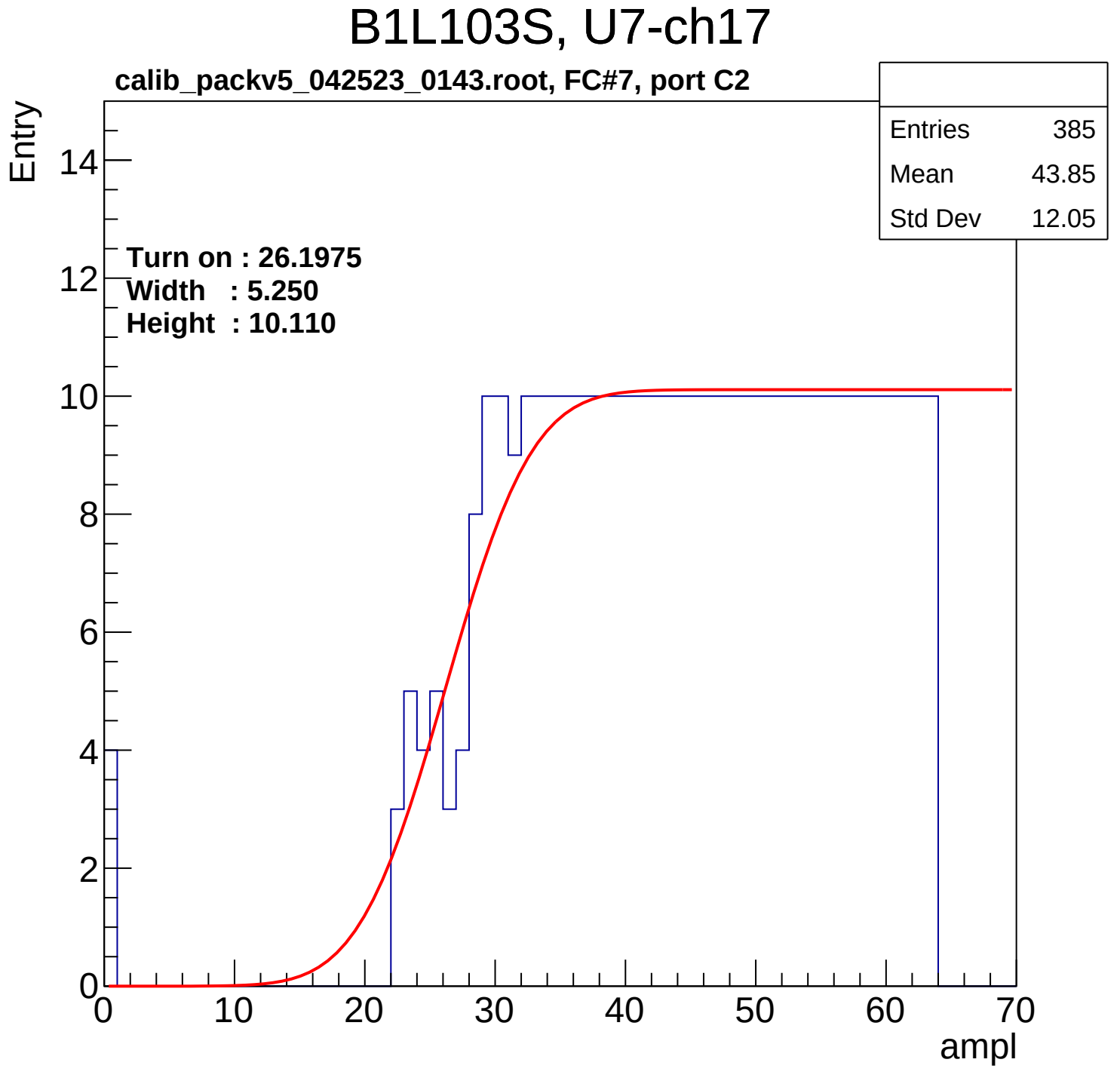
B1L103S, U7-ch17
calib_packv5_042523_0143.root, FC#7, port C2
Entries 385
Mean 43.85
Std Dev 12.05
Turn on : 26.1975
Width : 5.250
Height : 10.110
Entry
ampl
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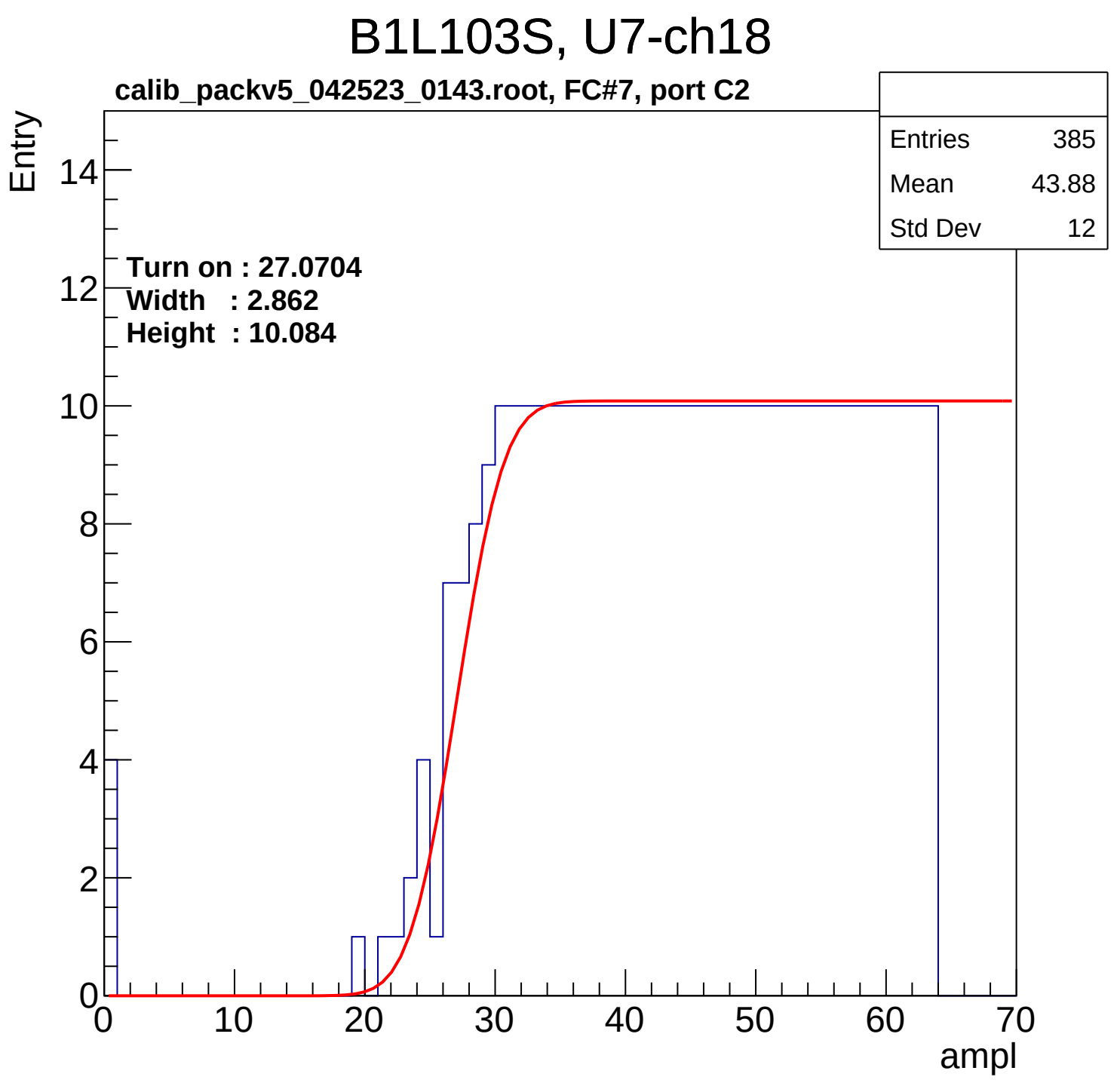
B1L103S, U7-ch18
calib_packv5_042523_0143.root, FC#7, port C2
Entries 385
Mean 43.88
Std Dev 12
Turn on : 27.0704
Width : 2.862
Height : 10.084
Entry
ampl
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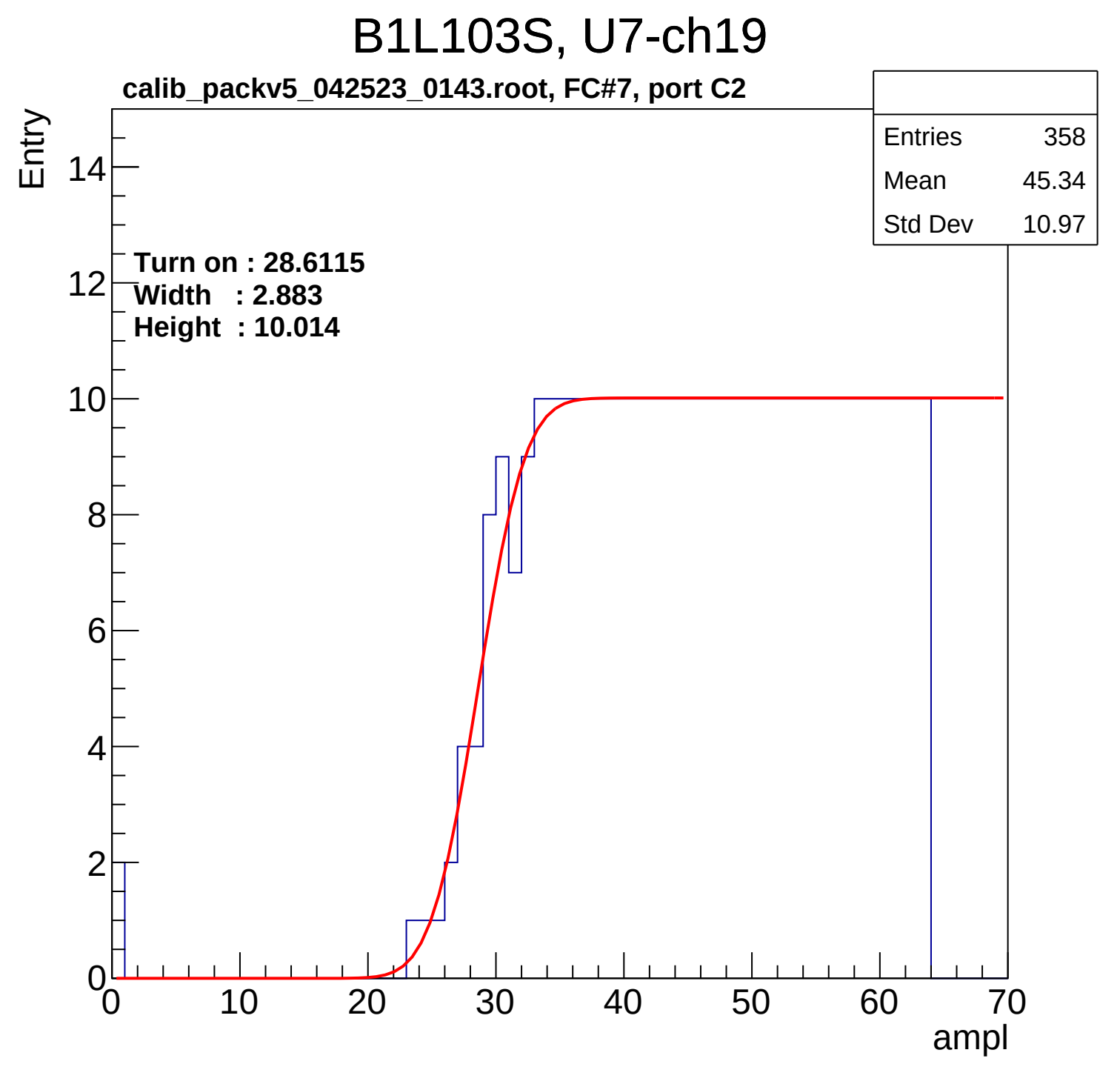
B1L103S, U7-ch19
calib_packv5_042523_0143.root, FC#7, port C2
Entries 358
Mean 45.34
Std Dev 10.97
Turn on : 28.6115
Width : 2.883
Height : 10.014
Entry
ampl
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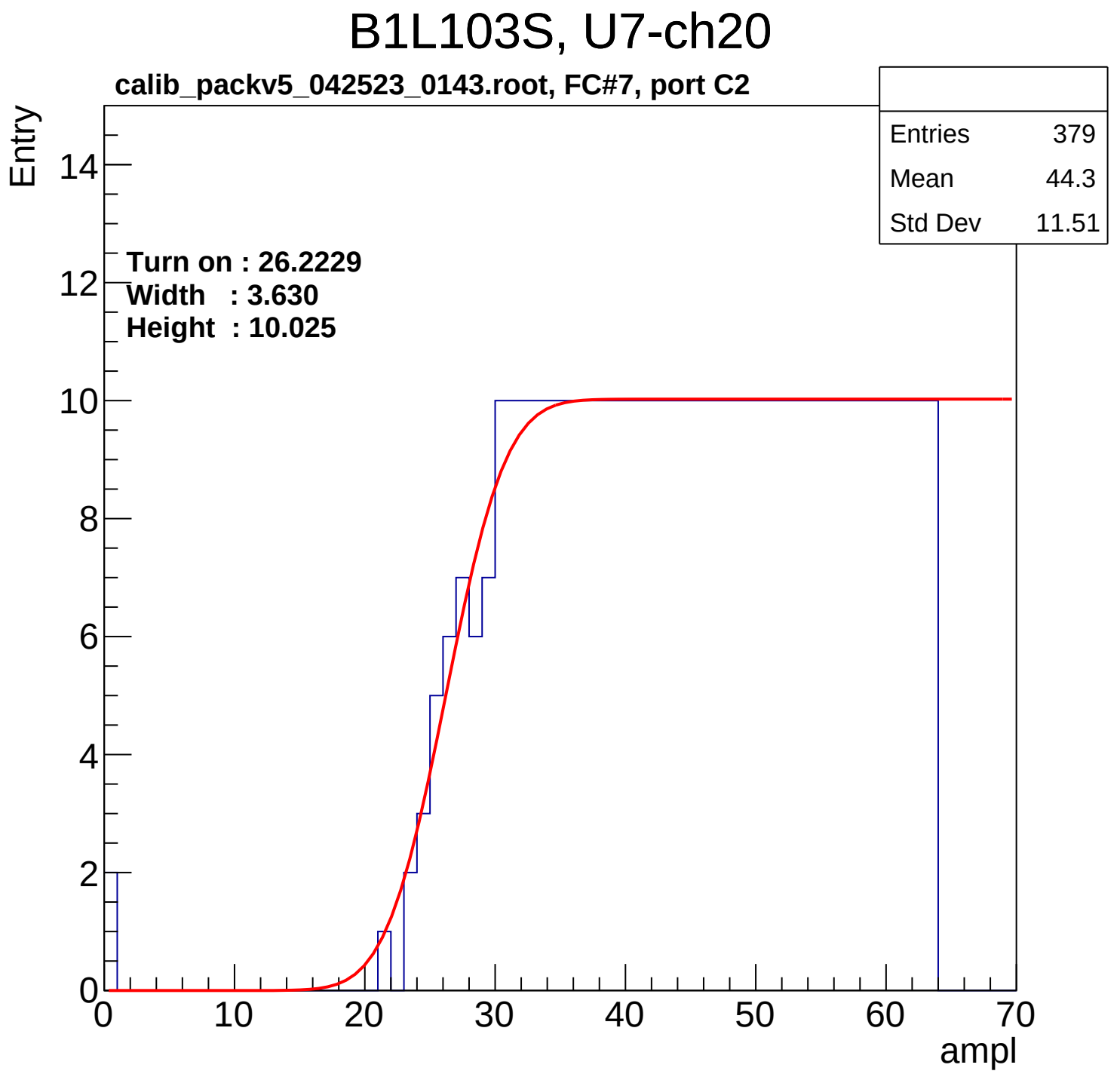
B1L103S, U7-ch20
calib_packv5_042523_0143.root, FC#7, port C2
Entries 379
Mean 44.3
Std Dev 11.51
Turn on : 26.2229
Width : 3.630
Height : 10.025
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ampl
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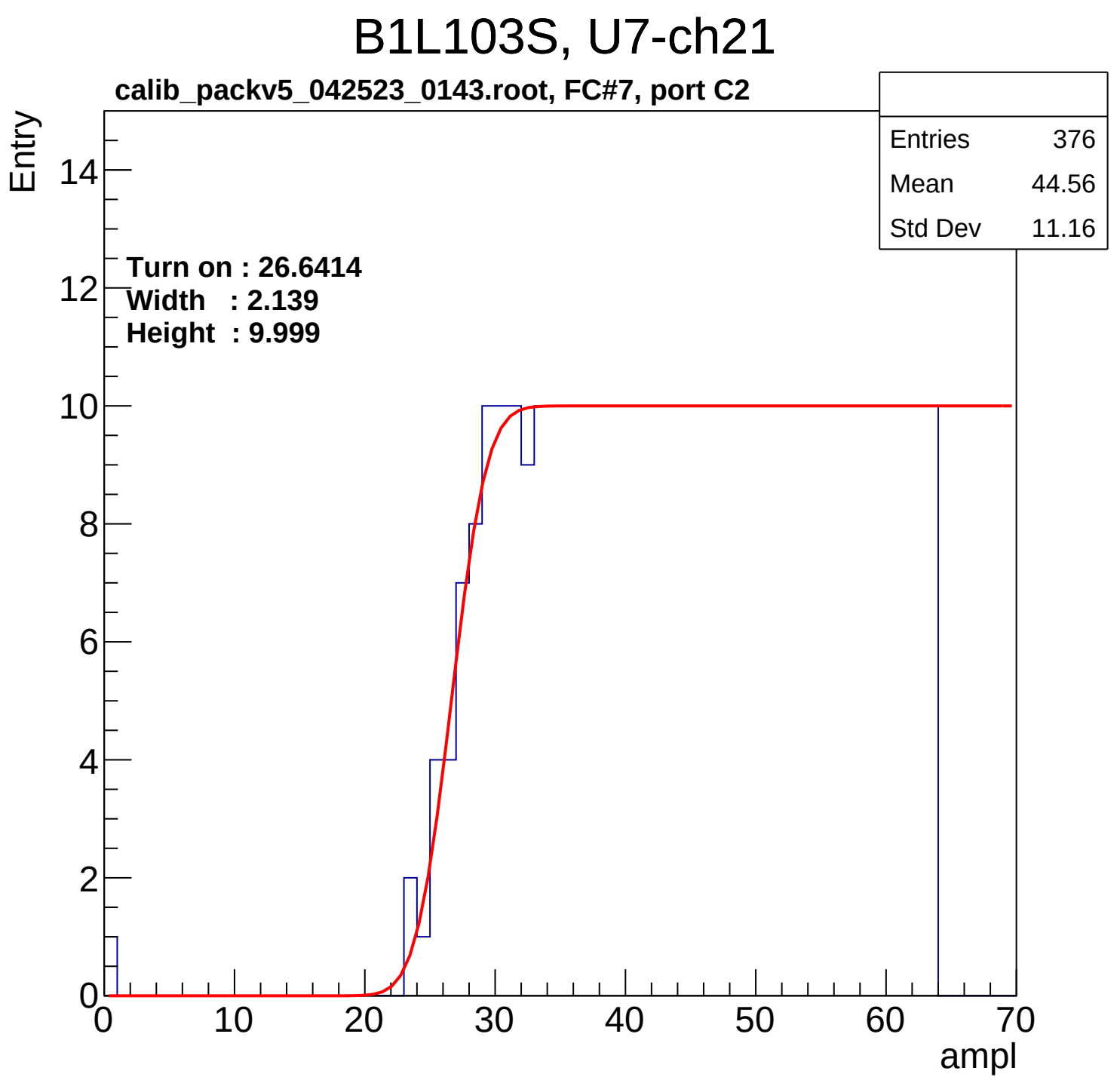
B1L103S, U7-ch21
calib_packv5_042523_0143.root, FC#7, port C2
Entries 376
Mean 44.56
Std Dev 11.16
Turn on : 26.6414
Width : 2.139
Height : 9.999
Entry
ampl
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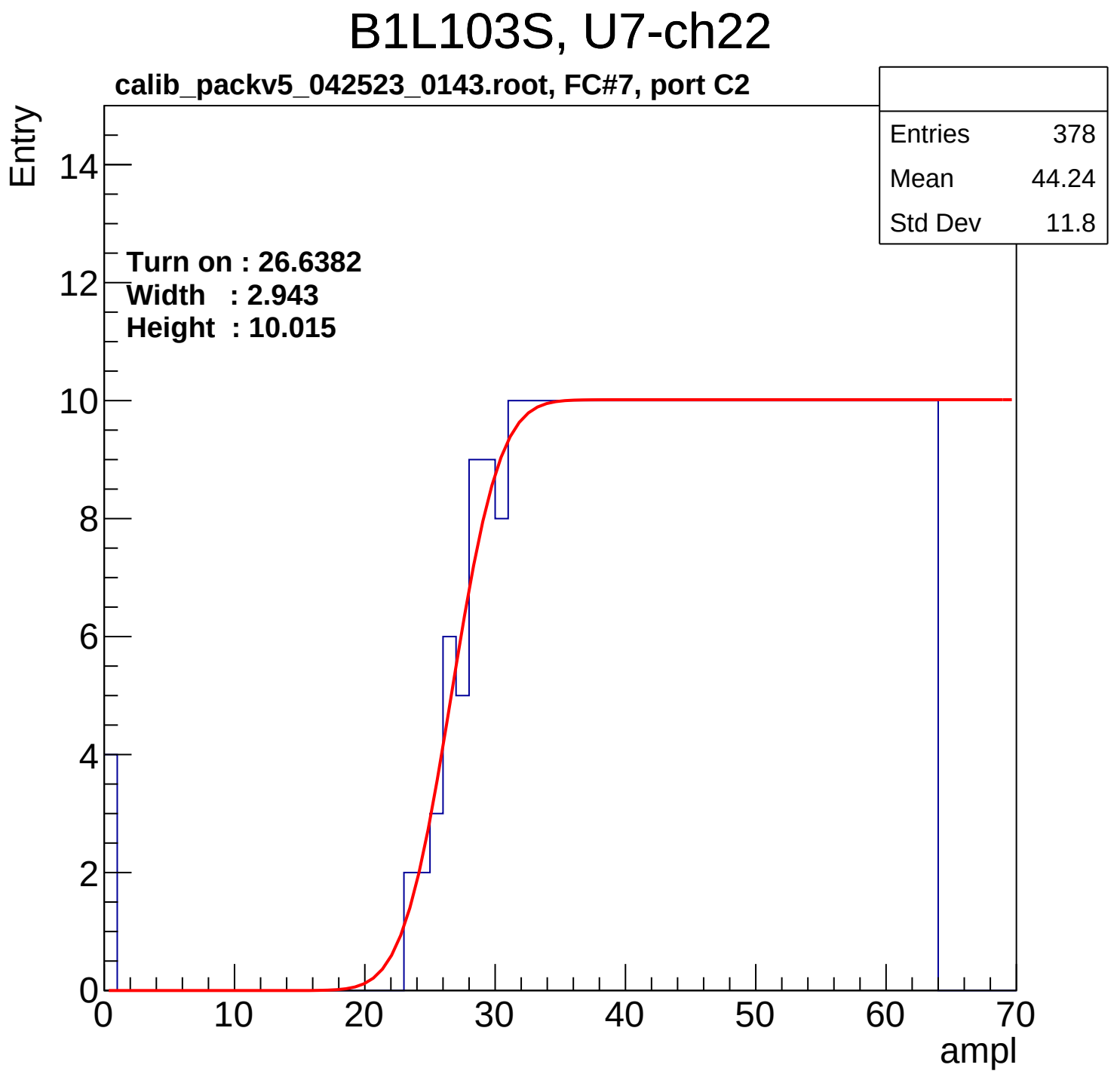
B1L103S, U7-ch22
calib_packv5_042523_0143.root, FC#7, port C2
Entries 378
Mean 44.24
Std Dev 11.8
Turn on : 26.6382
Width : 2.943
Height : 10.015
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ampl
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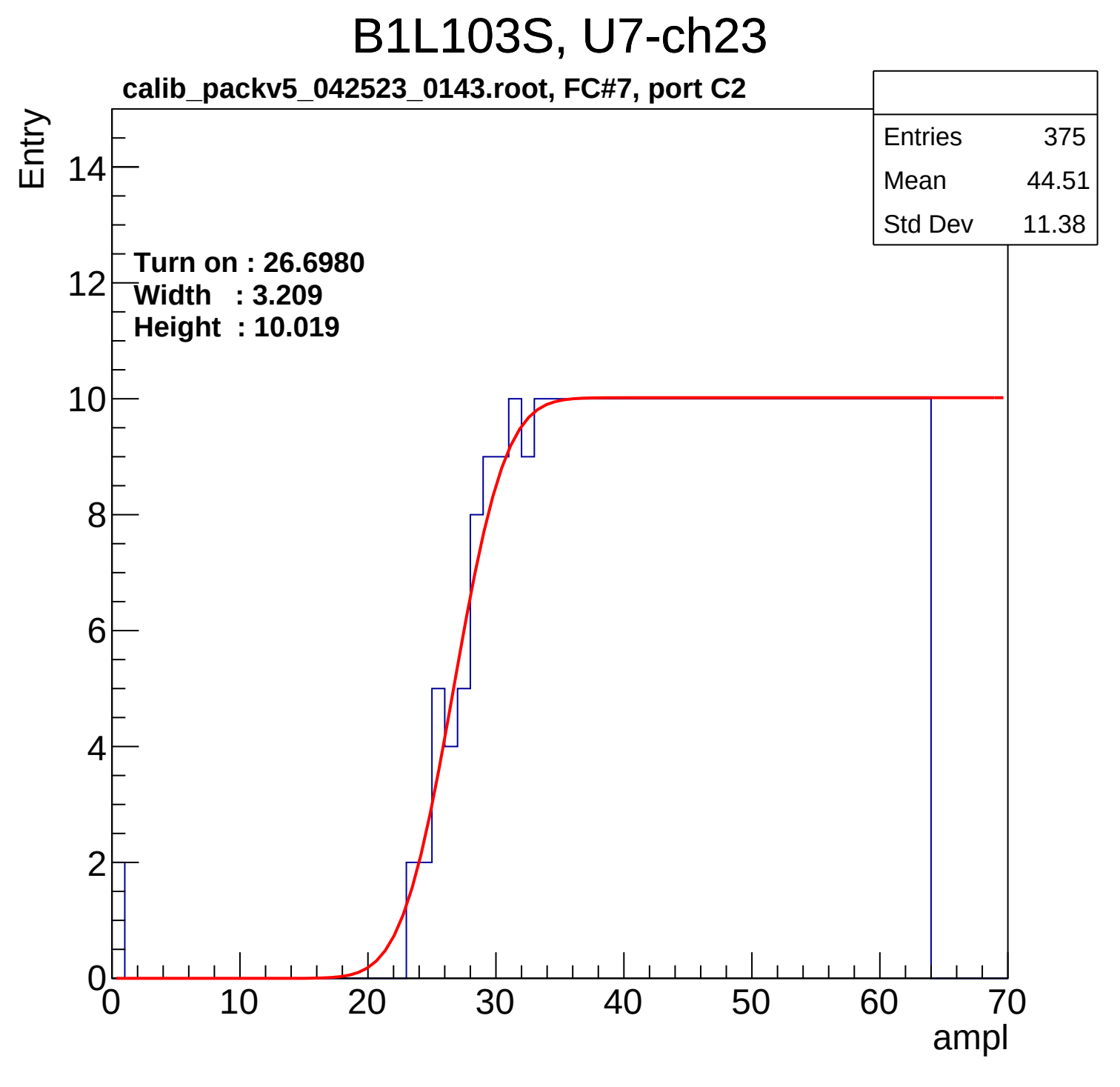
B1L103S, U7-ch23
calib_packv5_042523_0143.root, FC#7, port C2
Entries 375
Mean 44.51
Std Dev 11.38
Turn on : 26.6980
Width : 3.209
Height : 10.019
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ampl
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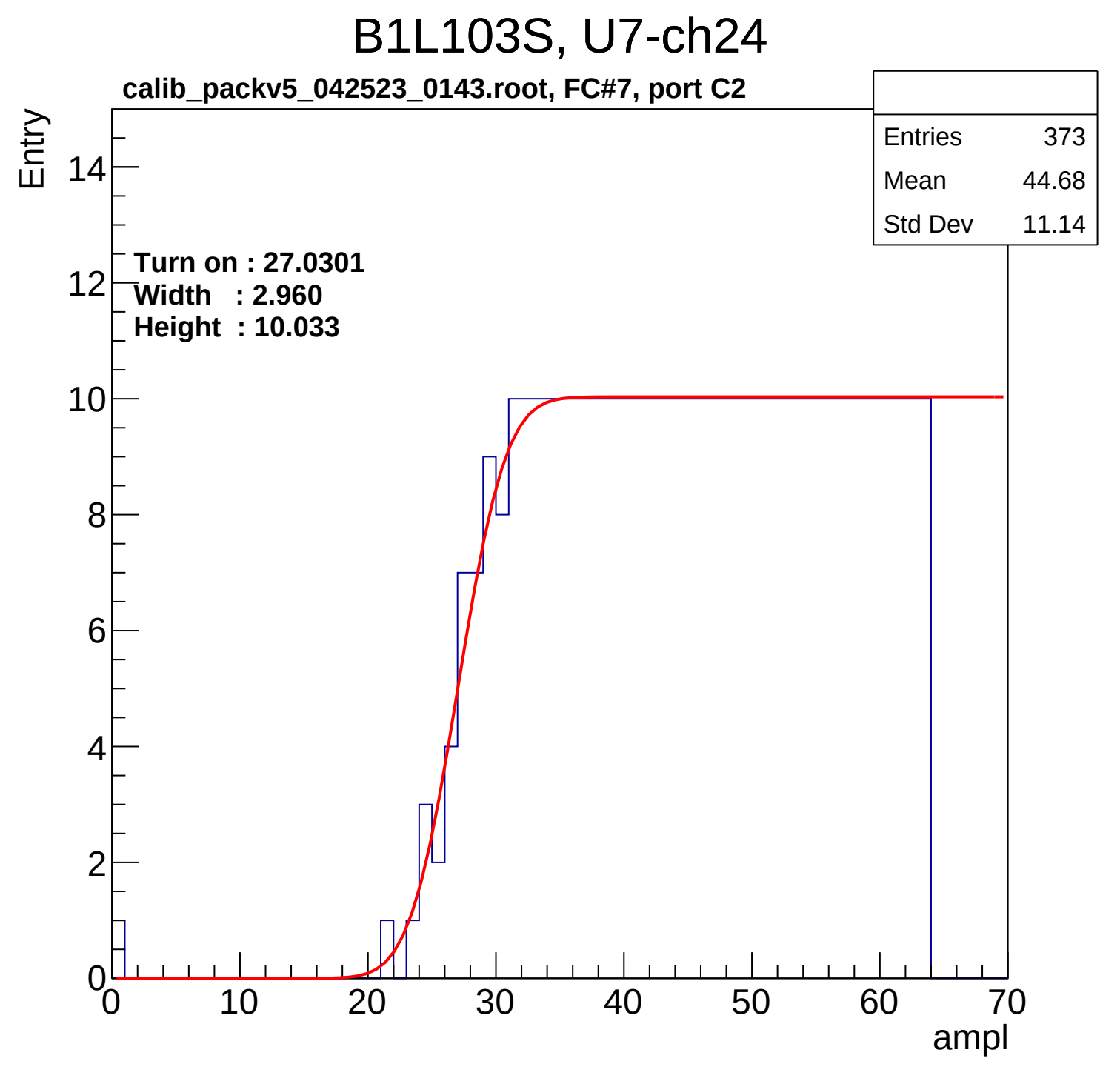
B1L103S, U7-ch24
calib_packv5_042523_0143.root, FC#7, port C2
Entries 373
Mean 44.68
Std Dev 11.14
Turn on : 27.0301
Width : 2.960
Height : 10.033
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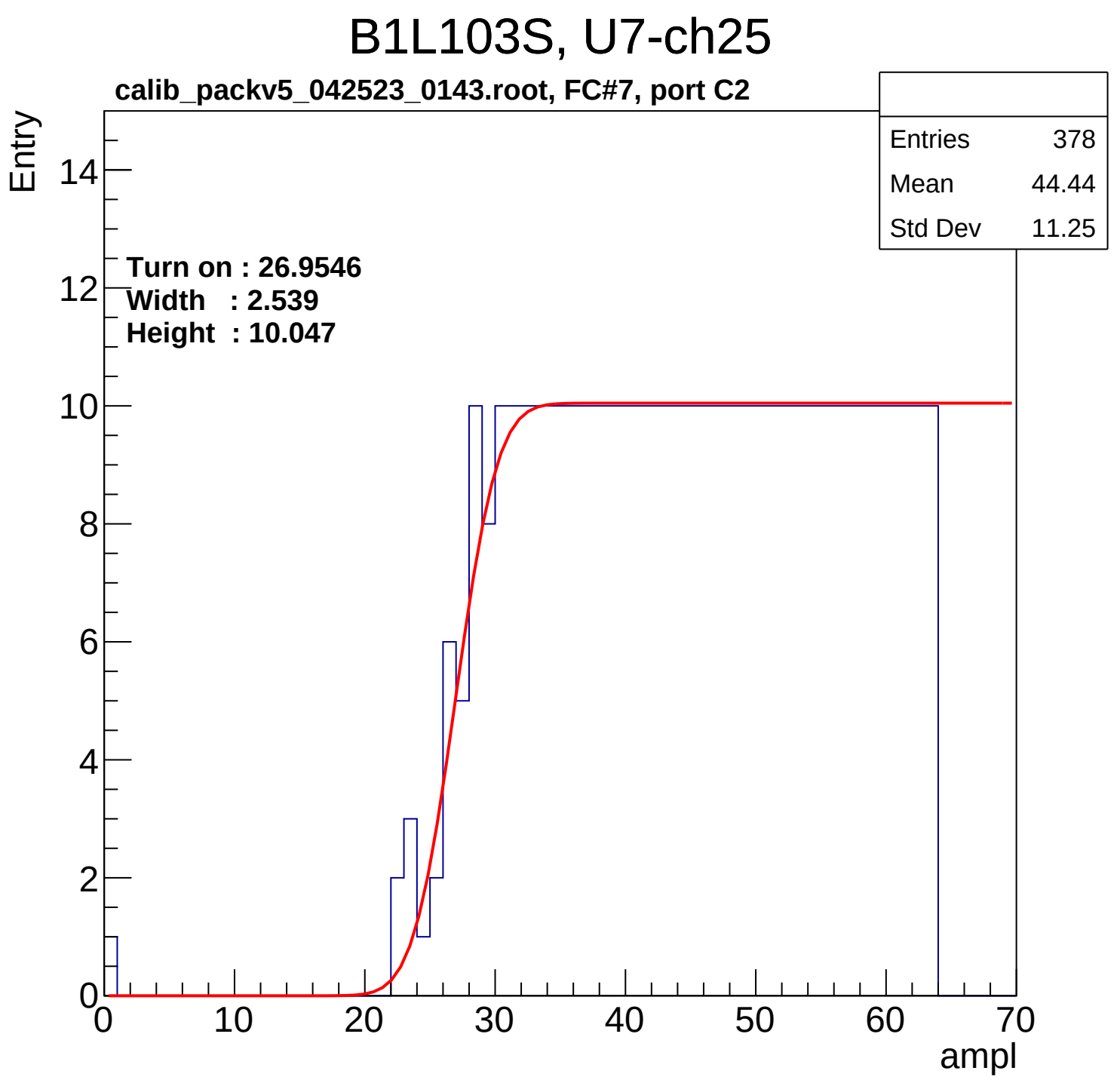
B1L103S, U7-ch25
calib_packv5_042523_0143.root, FC#7, port C2
Entries 378
Mean 44.44
Std Dev 11.25
Turn on : 26.9546
Width : 2.539
Height : 10.047
Entry
ampl
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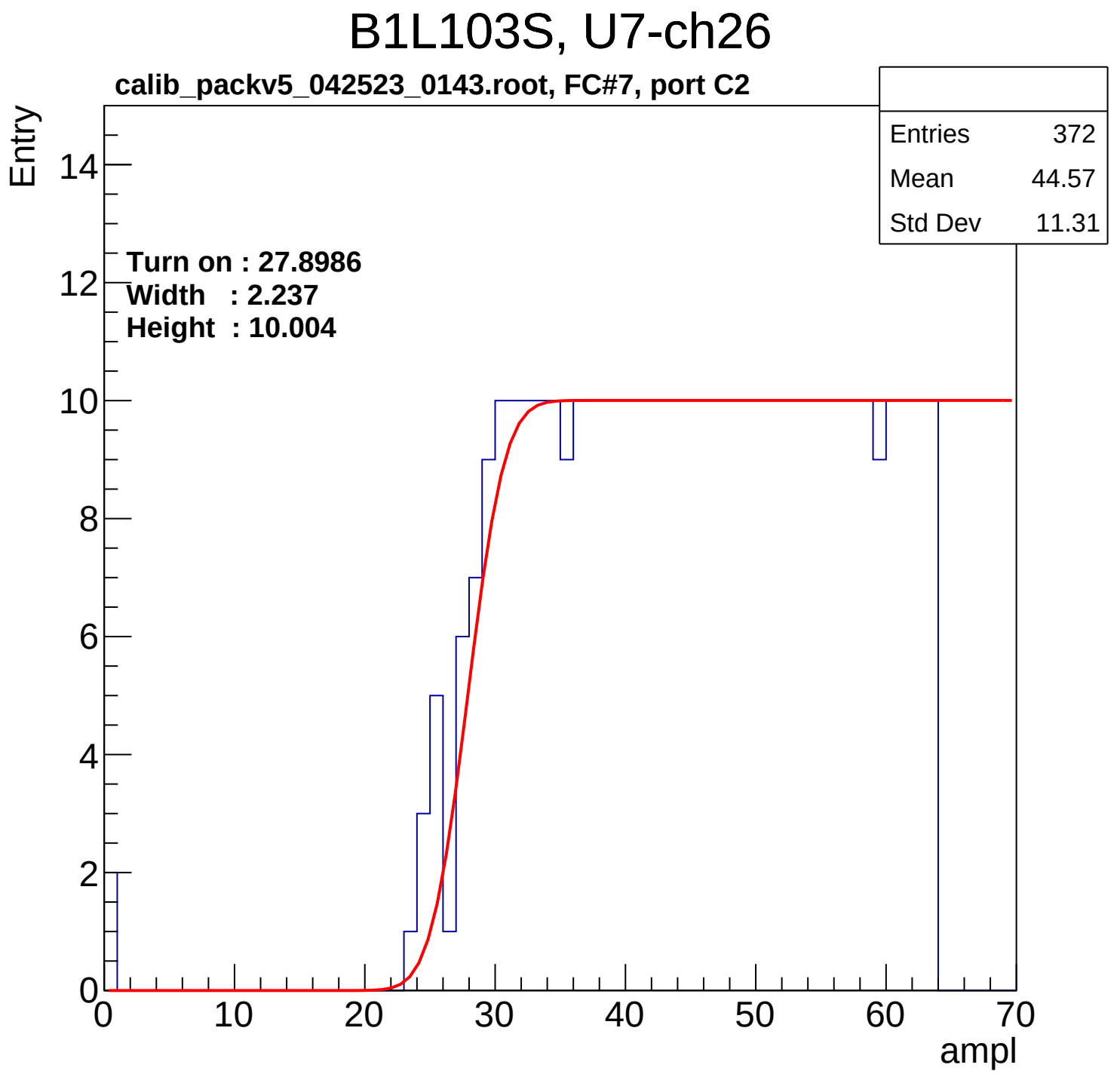
B1L103S, U7-ch26
calib_packv5_042523_0143.root, FC#7, port C2
Entries 372
Mean 44.57
Std Dev 11.31
Turn on : 27.8986
Width : 2.237
Height : 10.004
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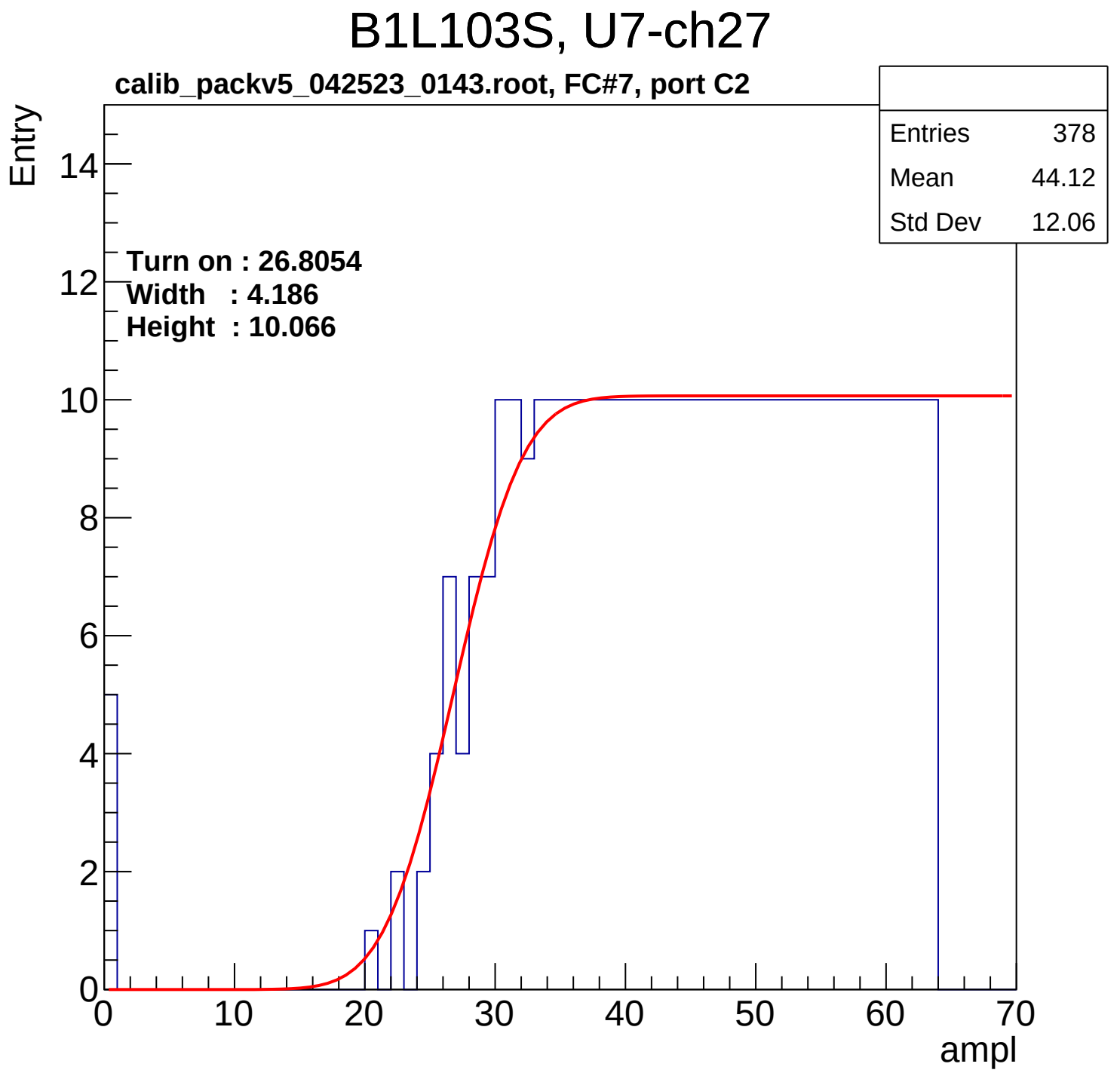
B1L103S, U7-ch27
calib_packv5_042523_0143.root, FC#7, port C2
Entries 378
Mean 44.12
Std Dev 12.06
Turn on : 26.8054
Width : 4.186
Height : 10.066
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ampl
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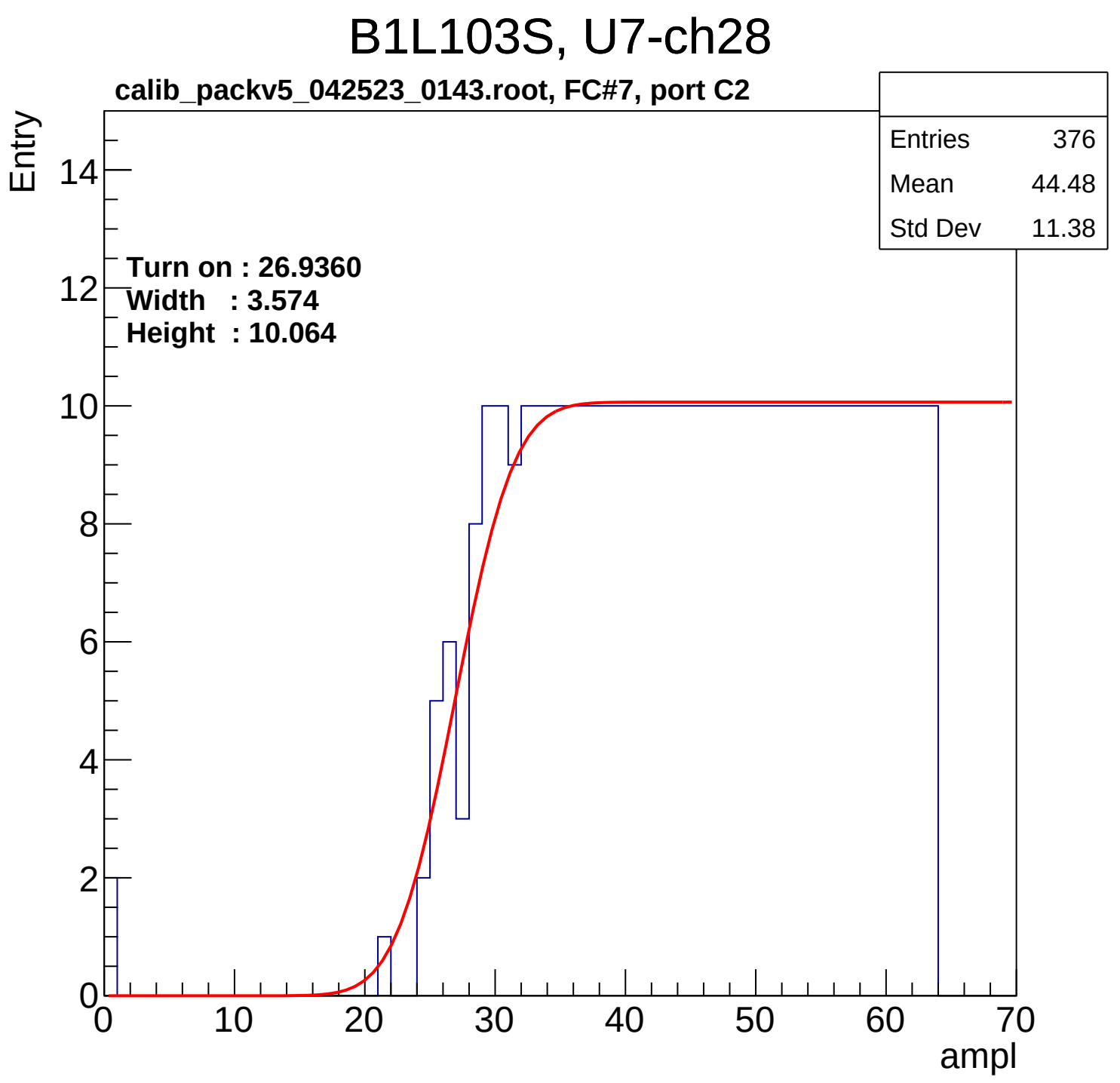
B1L103S, U7-ch28
calib_packv5_042523_0143.root, FC#7, port C2
Entries 376
Mean 44.48
Std Dev 11.38
Turn on : 26.9360
Width : 3.574
Height : 10.064
Entry
ampl
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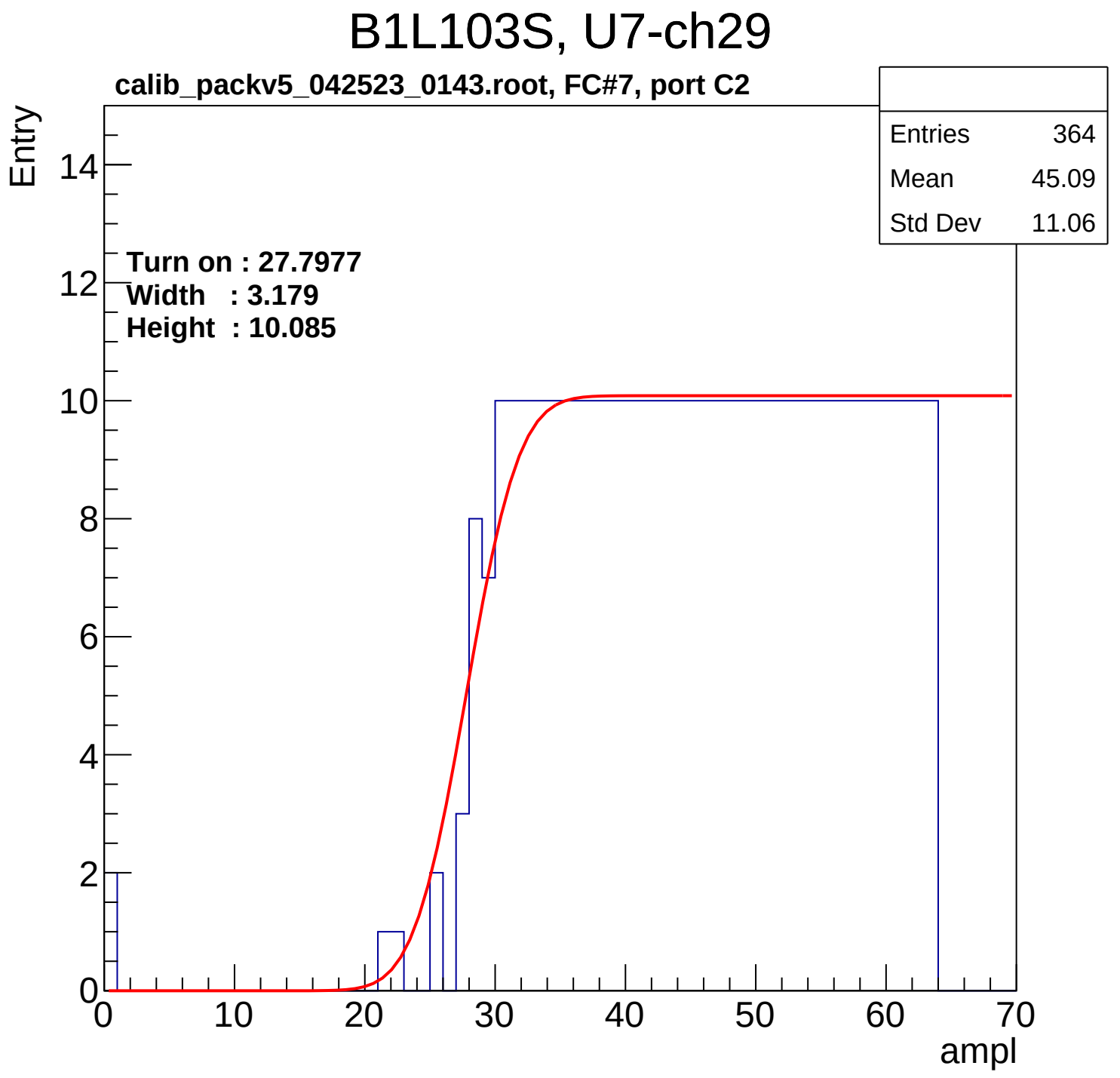
B1L103S, U7-ch29
calib_packv5_042523_0143.root, FC#7, port C2
Entries 364
Mean 45.09
Std Dev 11.06
Turn on : 27.7977
Width : 3.179
Height : 10.085
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ampl
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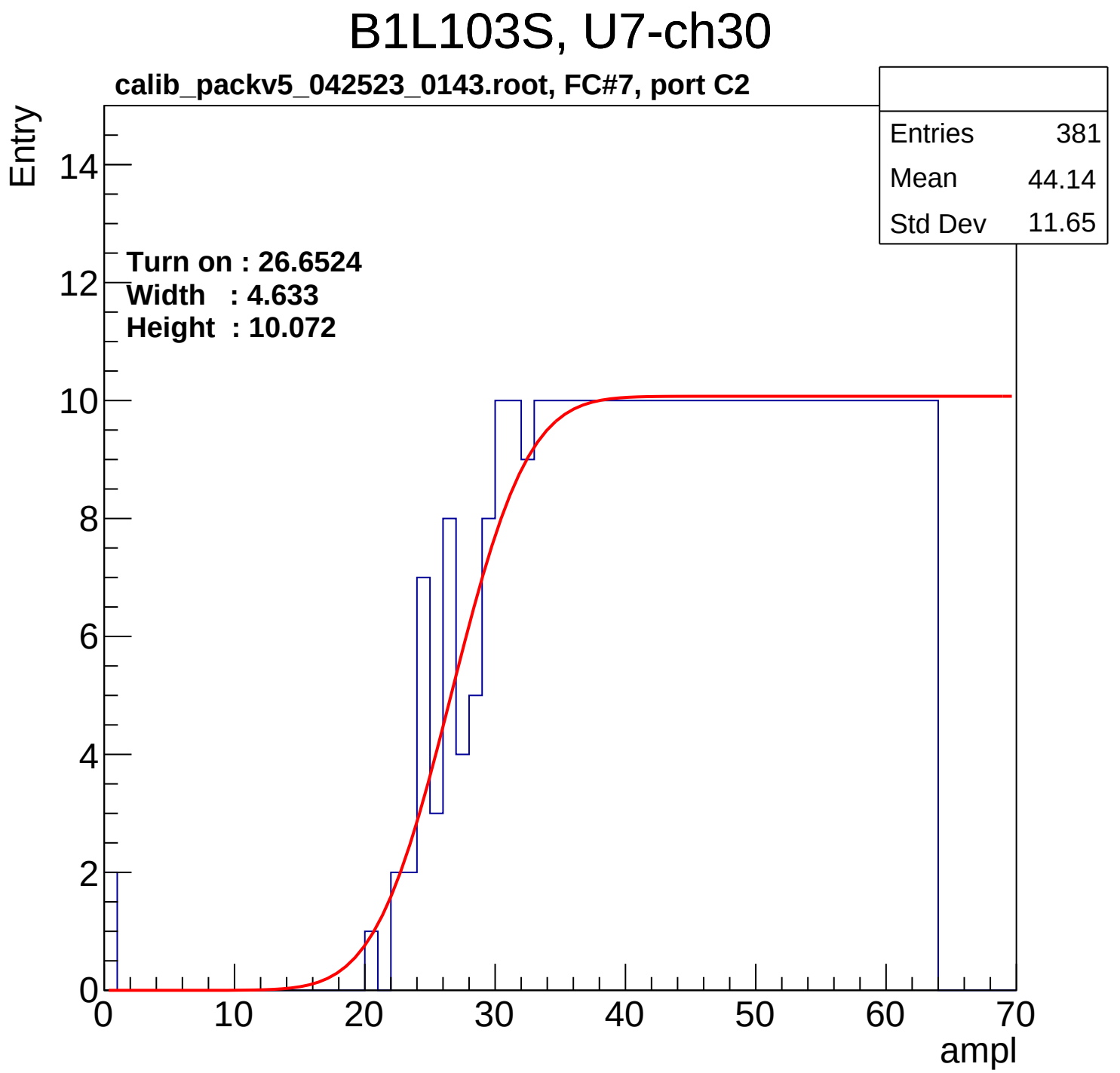
B1L103S, U7-ch30
calib_packv5_042523_0143.root, FC#7, port C2
Entries 381
Mean 44.14
Std Dev 11.65
Turn on : 26.6524
Width : 4.633
Height : 10.072
Entry
ampl
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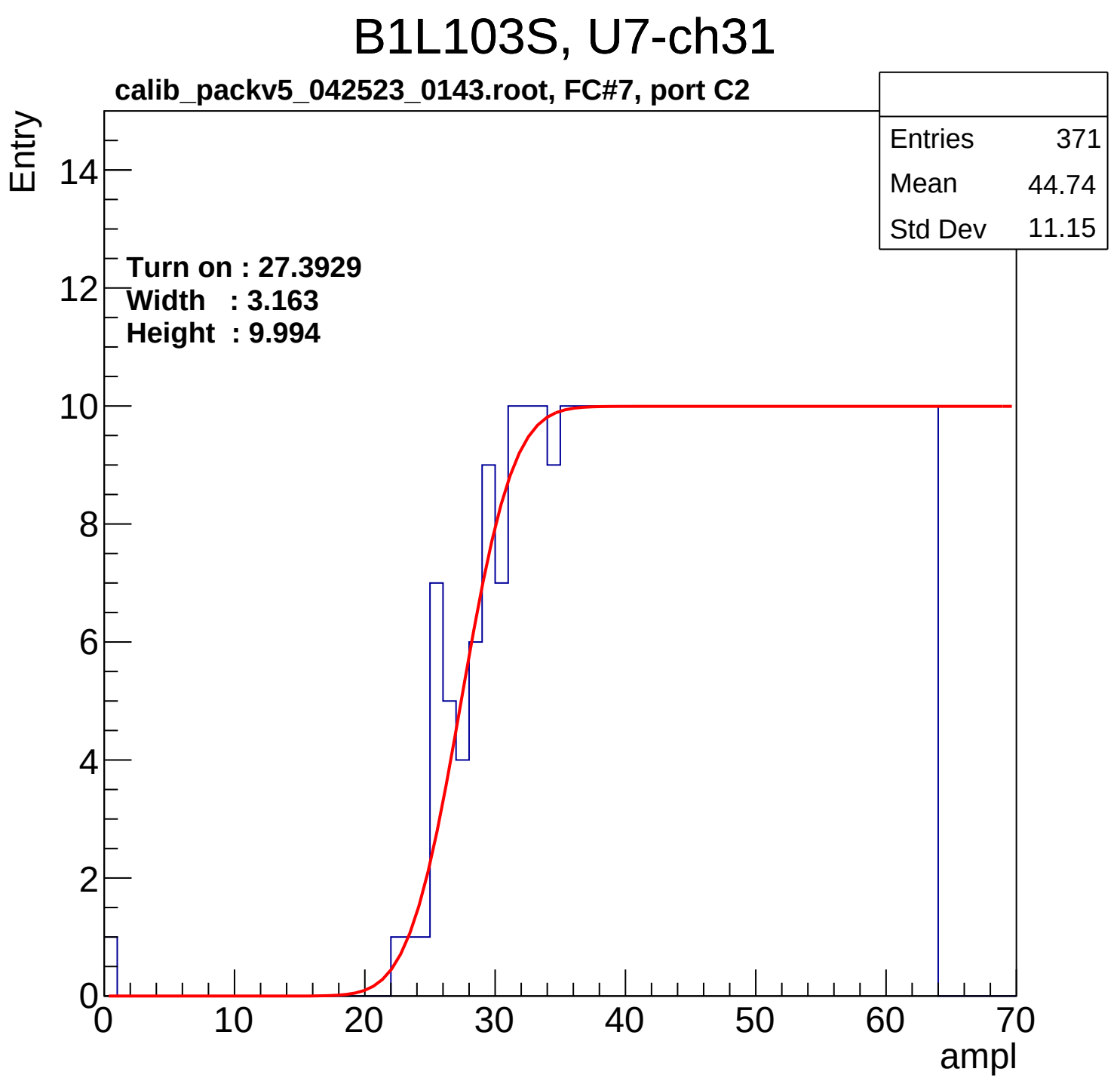
B1L103S, U7-ch31
calib_packv5_042523_0143.root, FC#7, port C2
Entries 371
Mean 44.74
Std Dev 11.15
Turn on : 27.3929
Width : 3.163
Height : 9.994
Entry
ampl
0
2
4
6
8
10
12
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0
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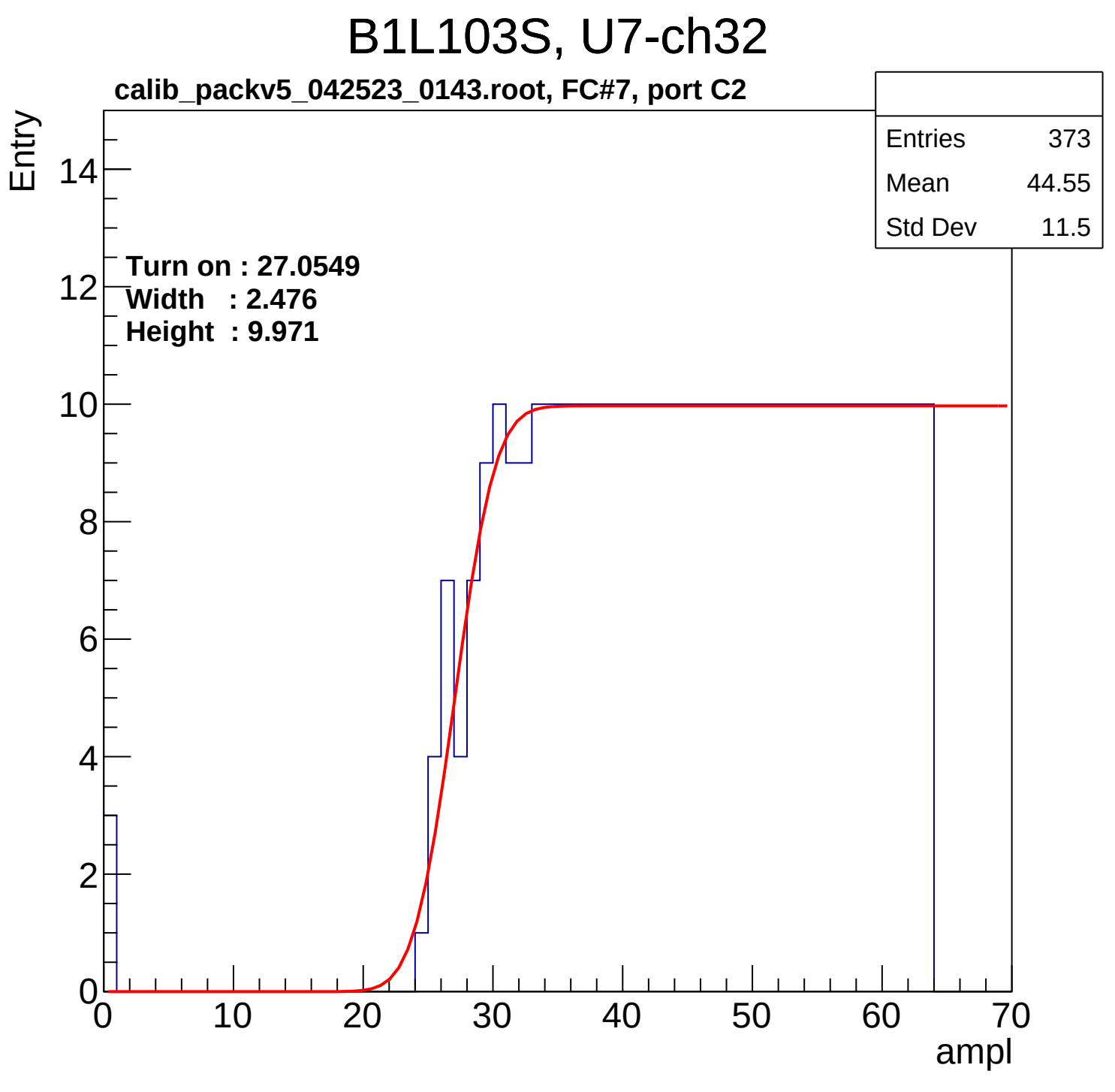
B1L103S, U7-ch32
calib_packv5_042523_0143.root, FC#7, port C2
Entries 373
Mean 44.55
Std Dev 11.5
Turn on : 27.0549
Width : 2.476
Height : 9.971
Entry
ampl
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2
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6
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12
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0
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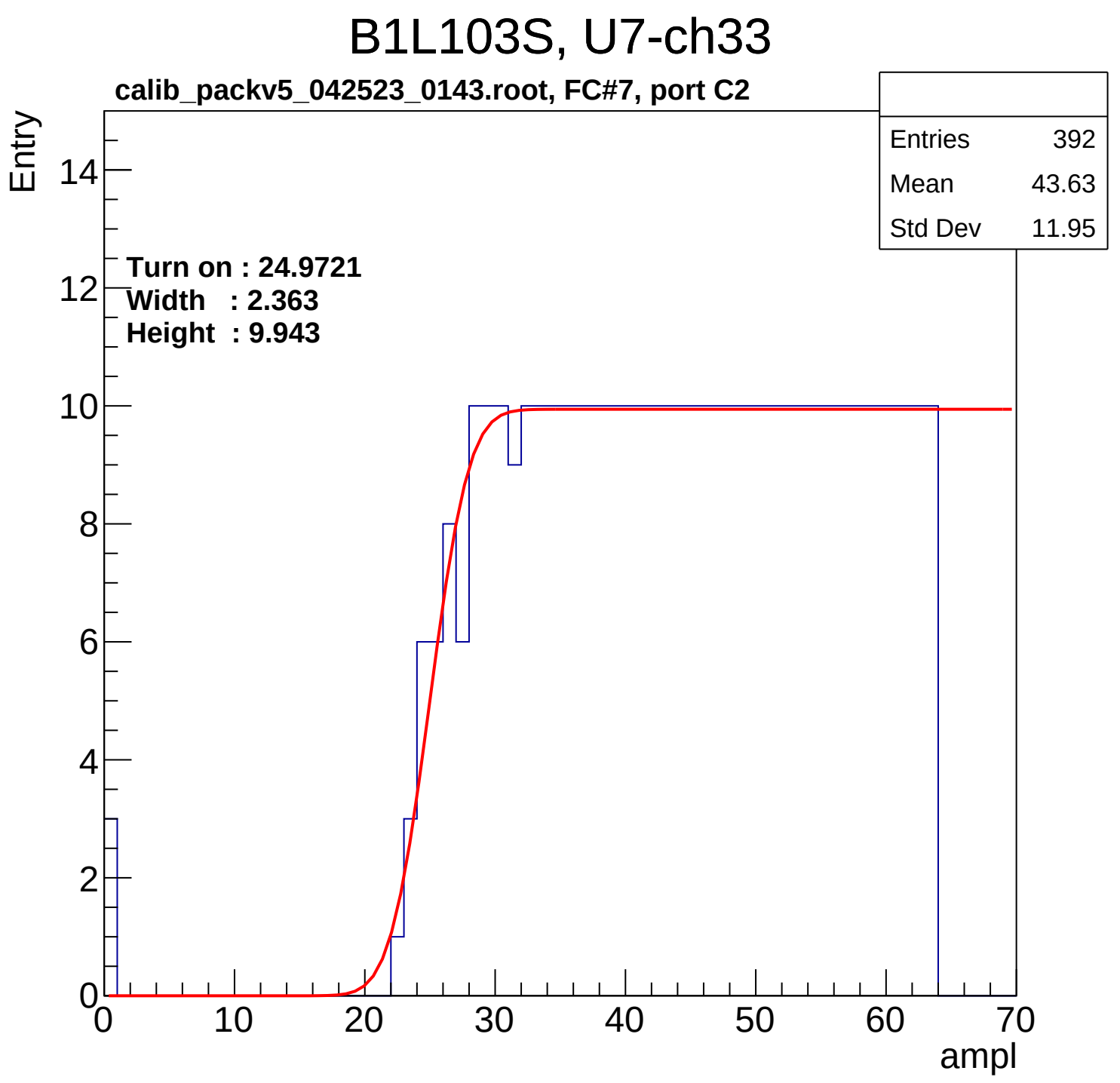
B1L103S, U7-ch33
calib_packv5_042523_0143.root, FC#7, port C2
Entries 392
Mean 43.63
Std Dev 11.95
Turn on : 24.9721
Width : 2.363
Height : 9.943
Entry
ampl
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2
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6
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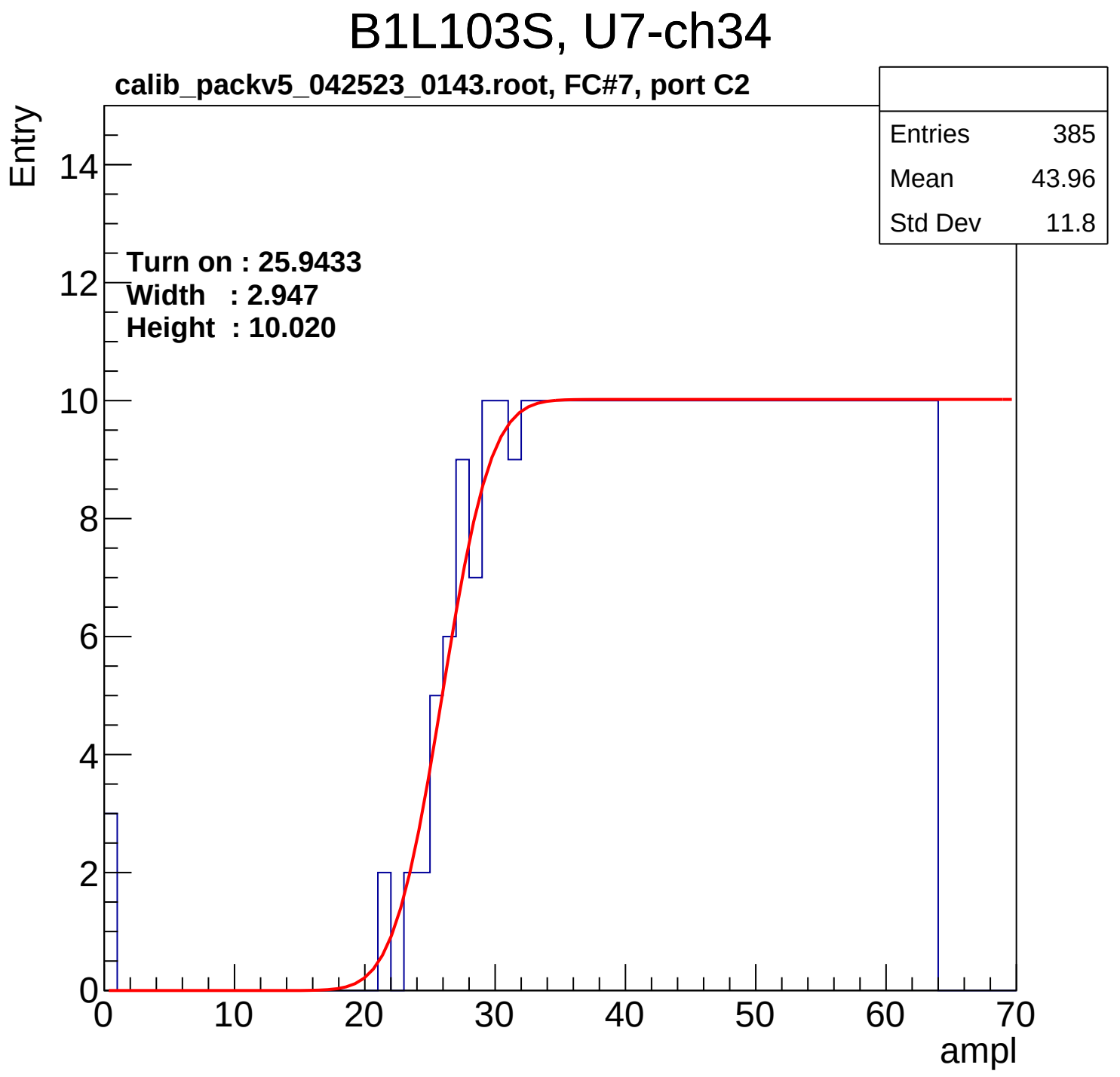
B1L103S, U7-ch34
calib_packv5_042523_0143.root, FC#7, port C2
Entries 385
Mean 43.96
Std Dev 11.8
Turn on : 25.9433
Width : 2.947
Height : 10.020
Entry
ampl
0
2
4
6
8
10
12
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0
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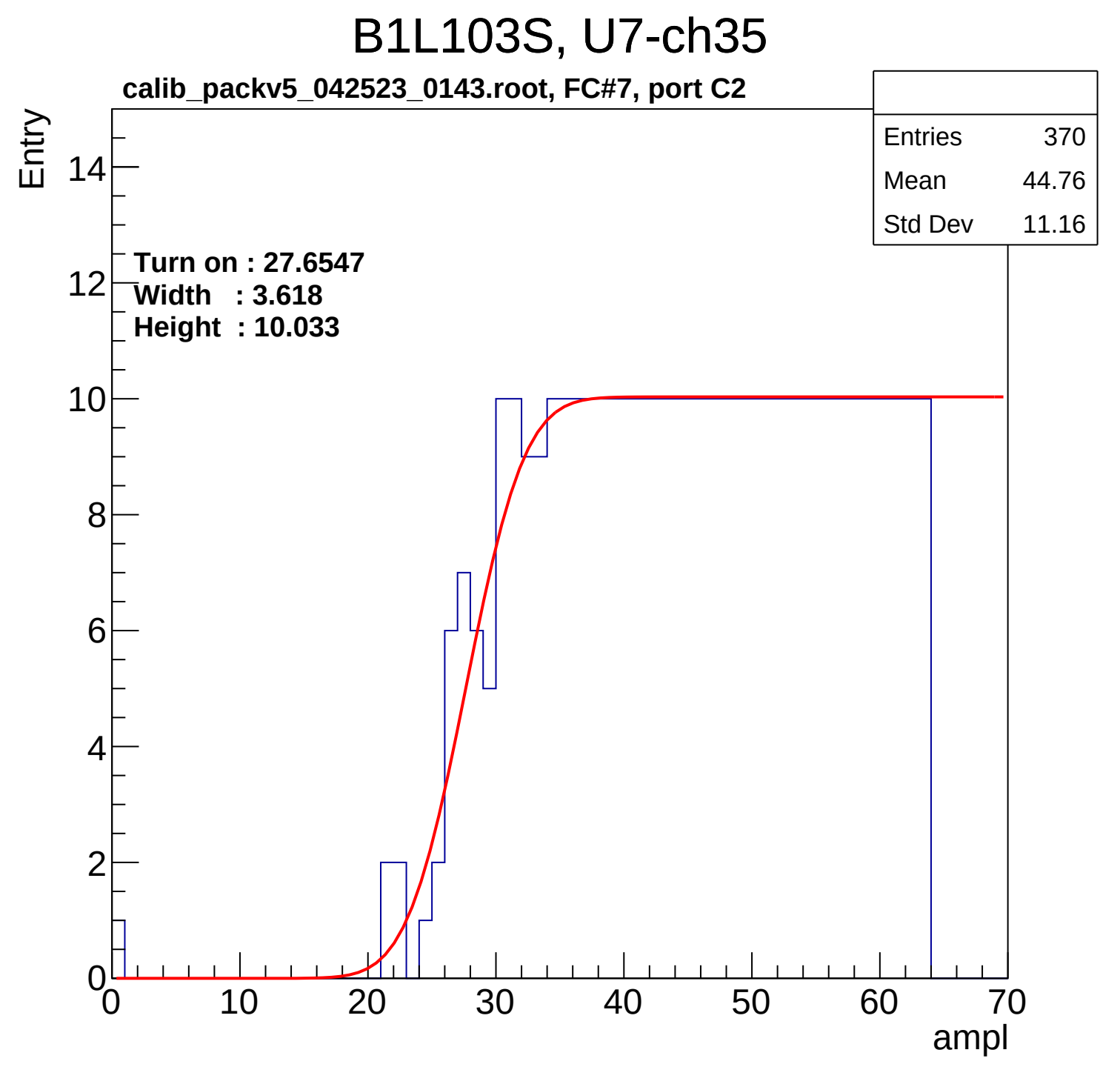
B1L103S, U7-ch35
calib_packv5_042523_0143.root, FC#7, port C2
Entries 370
Mean 44.76
Std Dev 11.16
Turn on : 27.6547
Width : 3.618
Height : 10.033
Entry
ampl
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2
4
6
8
10
12
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0
10
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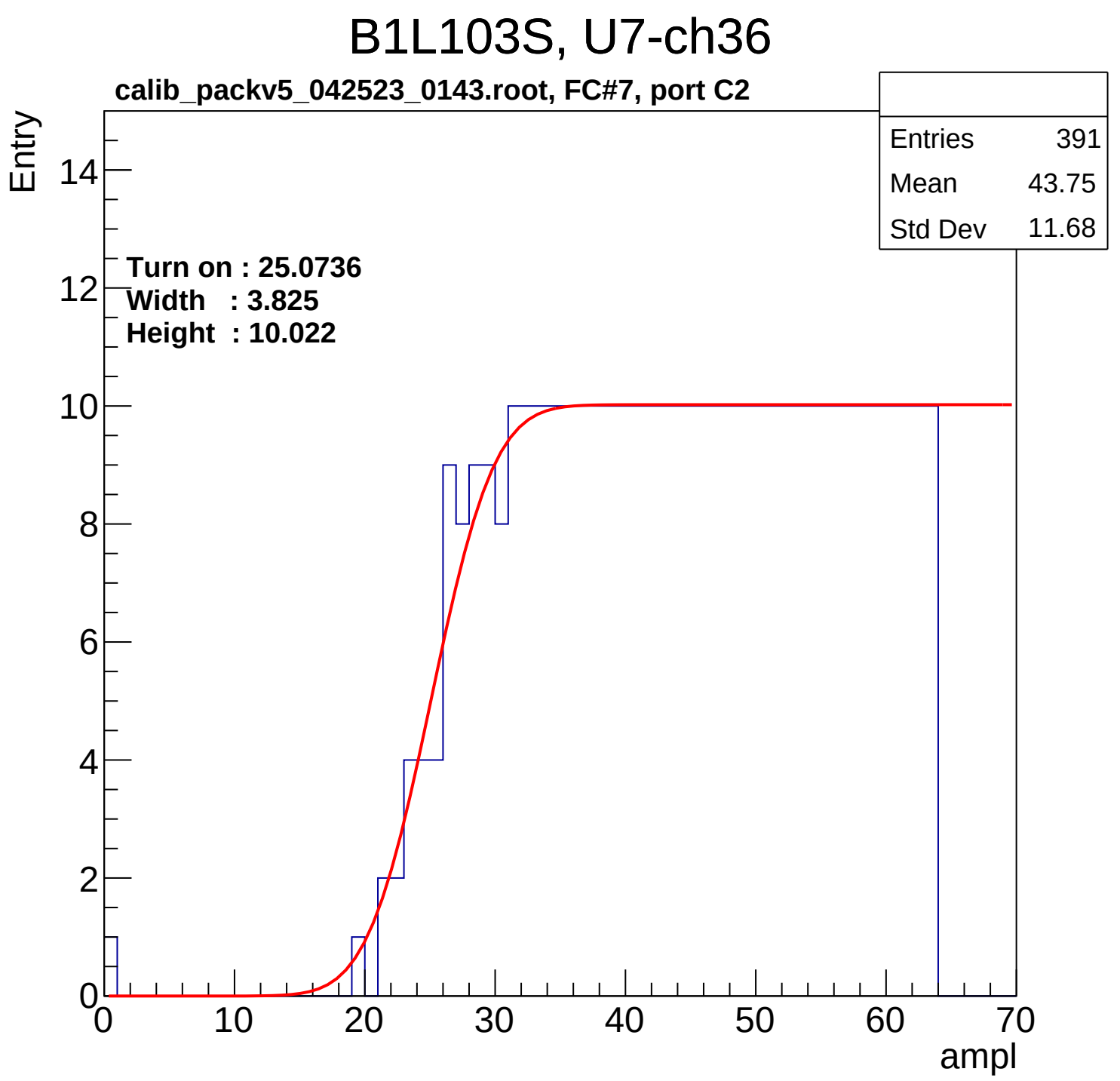
B1L103S, U7-ch36
calib_packv5_042523_0143.root, FC#7, port C2
Entries 391
Mean 43.75
Std Dev 11.68
Turn on : 25.0736
Width : 3.825
Height : 10.022
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
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60
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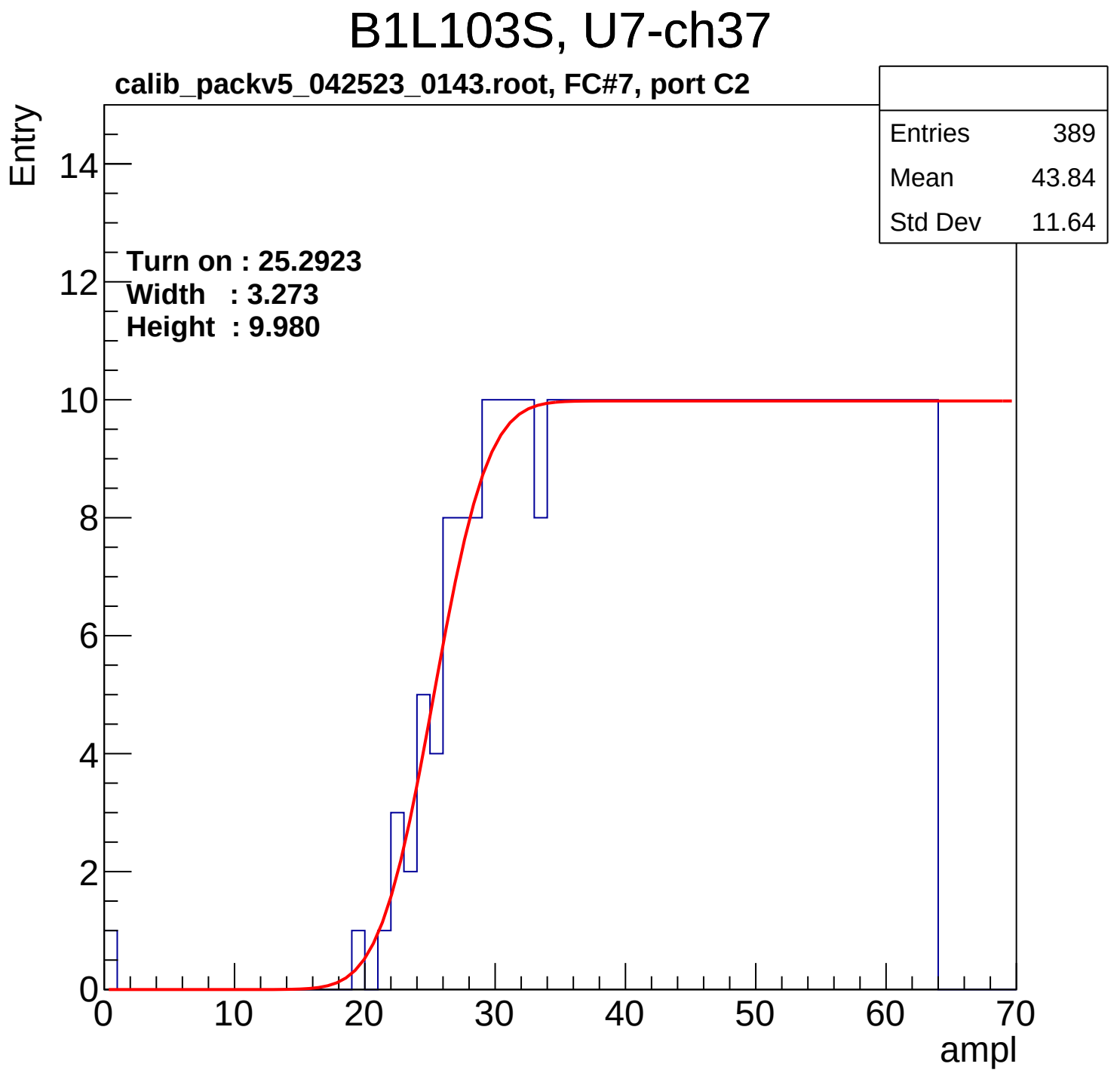
B1L103S, U7-ch37
calib_packv5_042523_0143.root, FC#7, port C2
Entries 389
Mean 43.84
Std Dev 11.64
Turn on : 25.2923
Width : 3.273
Height : 9.980
Entry
ampl
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2
4
6
8
10
12
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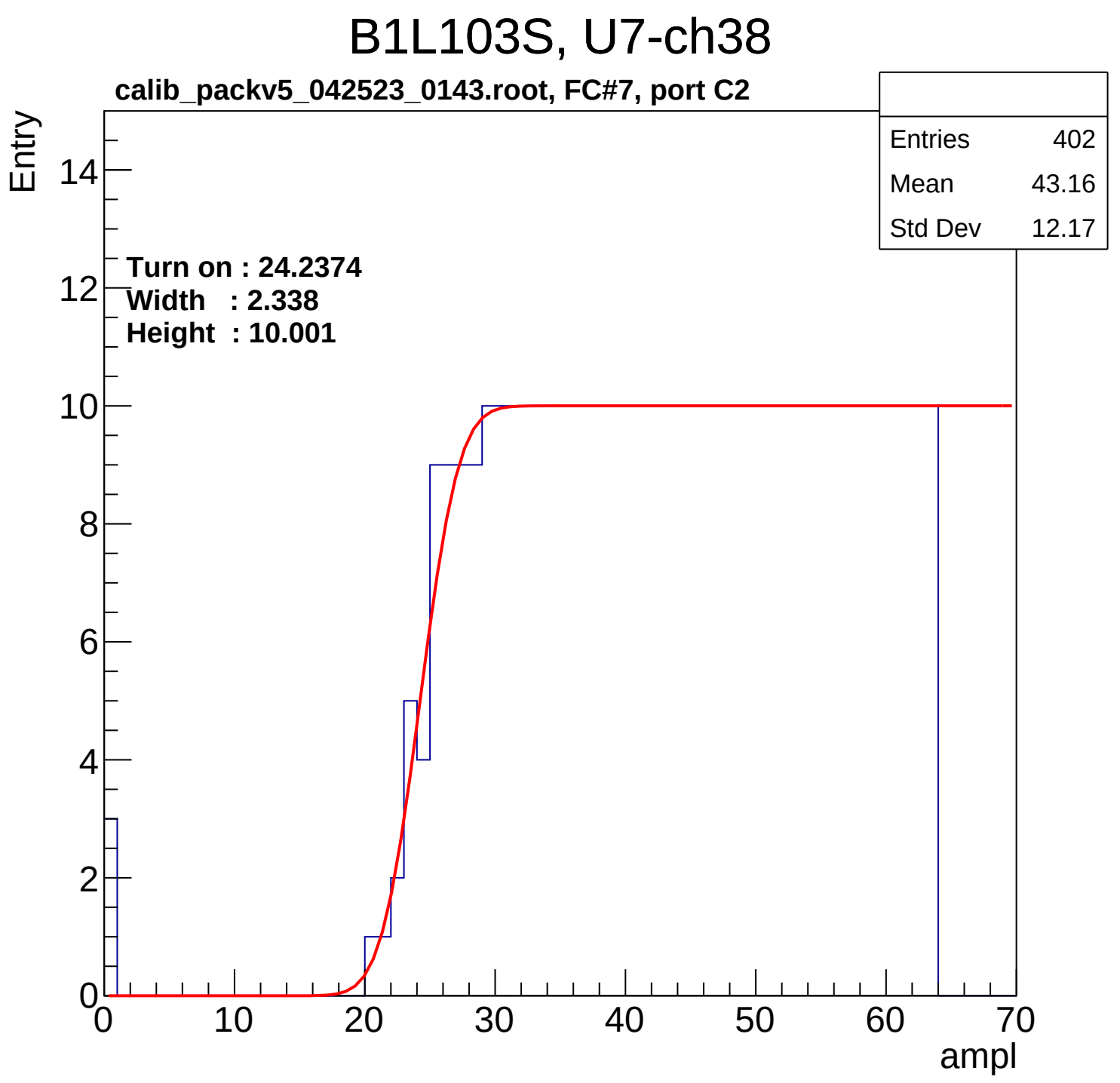
B1L103S, U7-ch38
calib_packv5_042523_0143.root, FC#7, port C2
Entries 402
Mean 43.16
Std Dev 12.17
Turn on : 24.2374
Width : 2.338
Height : 10.001
Entry
ampl
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6
8
10
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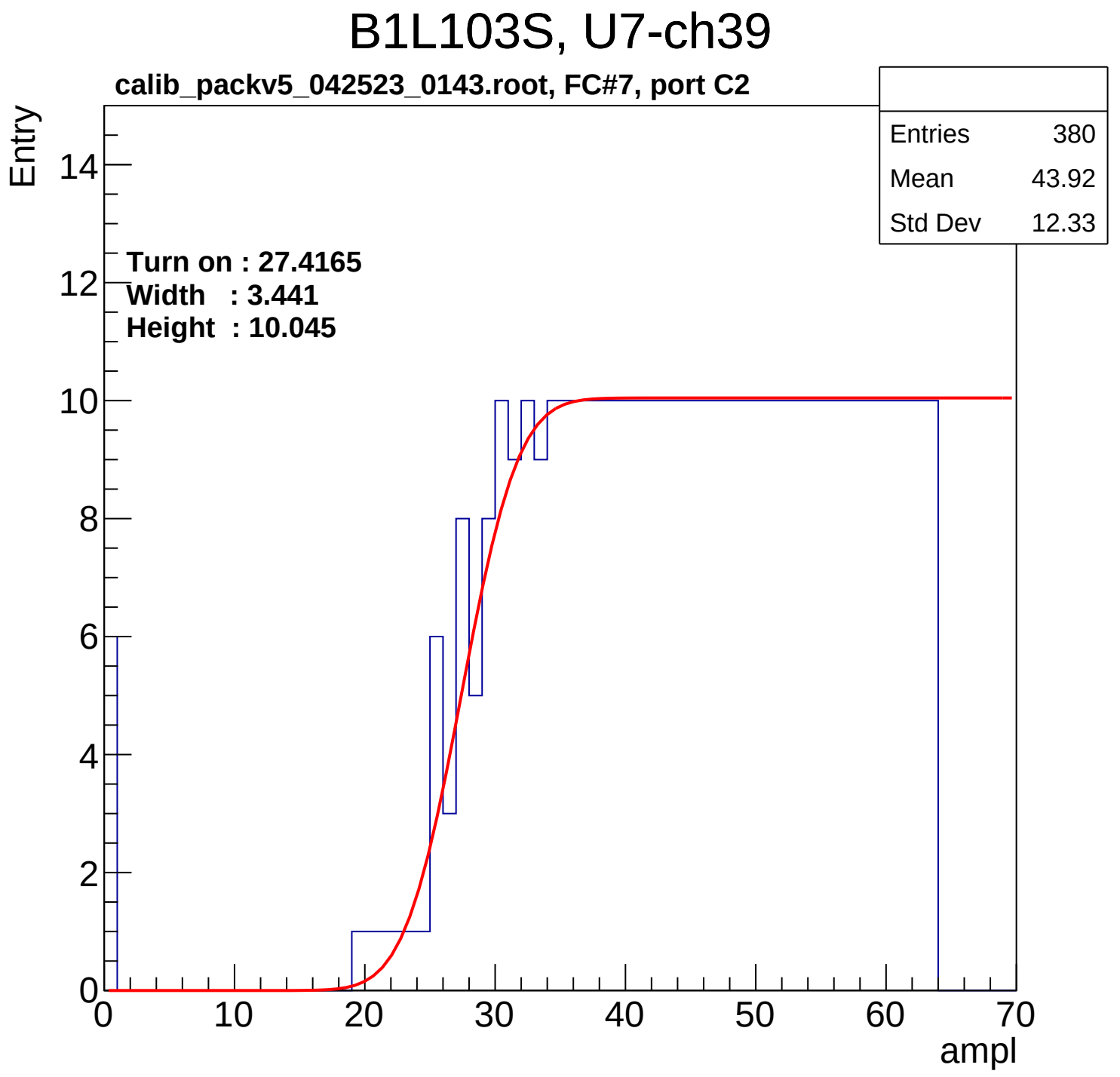
B1L103S, U7-ch39
calib_packv5_042523_0143.root, FC#7, port C2
Entries 380
Mean 43.92
Std Dev 12.33
Turn on : 27.4165
Width : 3.441
Height : 10.045
Entry
ampl
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6
8
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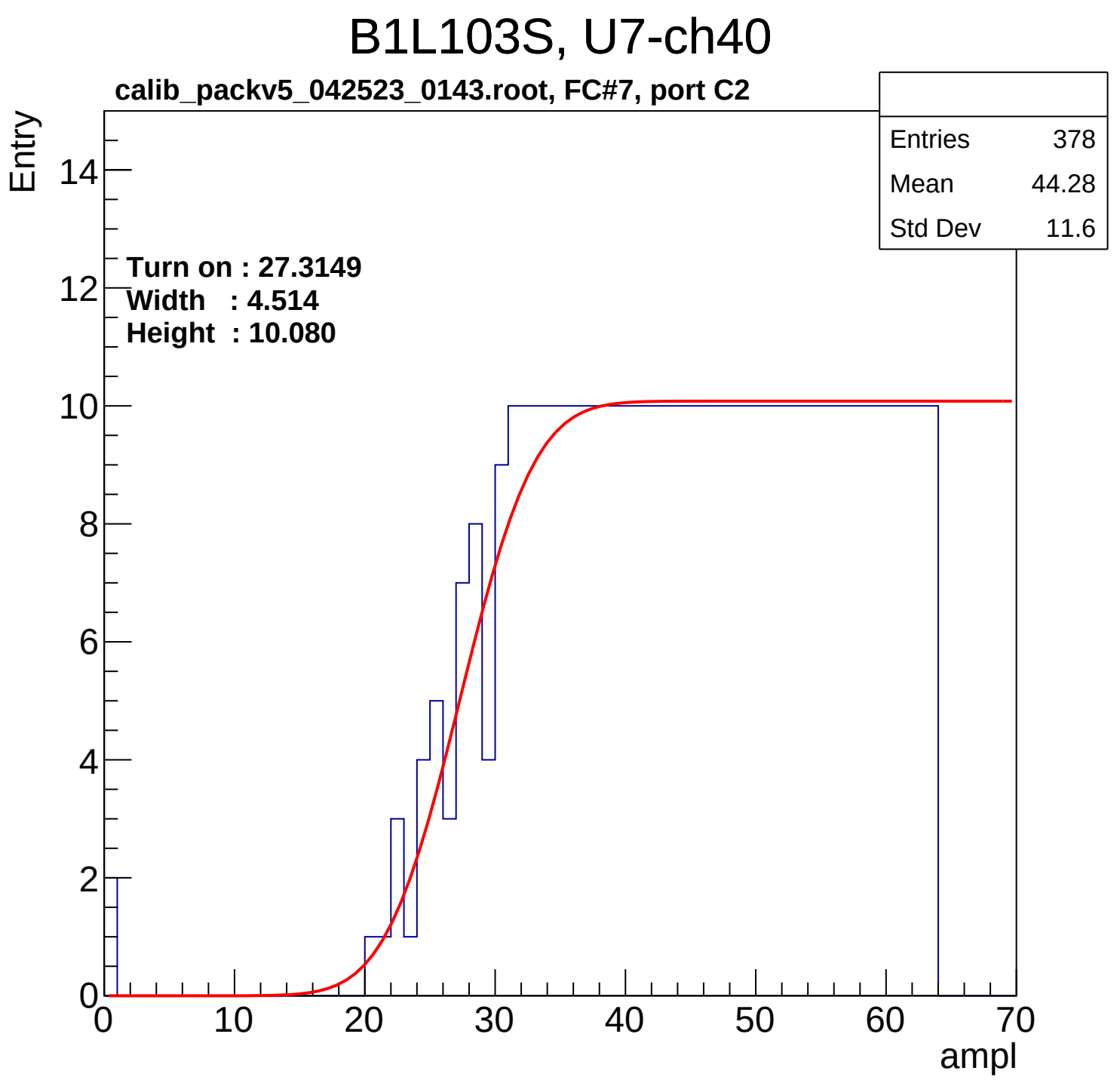
B1L103S, U7-ch40
calib_packv5_042523_0143.root, FC#7, port C2
Entries 378
Mean 44.28
Std Dev 11.6
Turn on : 27.3149
Width : 4.514
Height : 10.080
Entry
ampl
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6
8
10
12
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0
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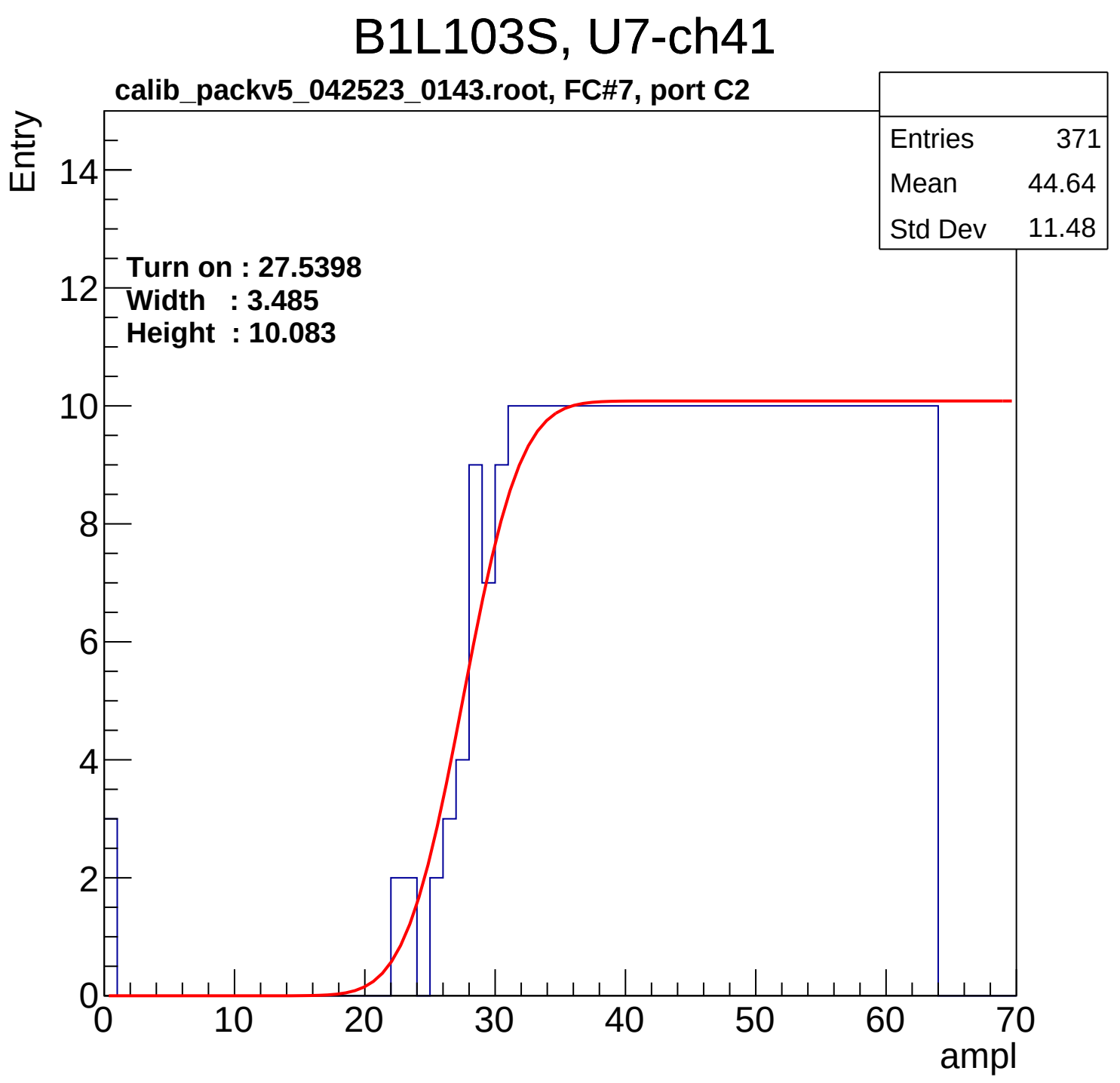
B1L103S, U7-ch41
calib_packv5_042523_0143.root, FC#7, port C2
Entries 371
Mean 44.64
Std Dev 11.48
Turn on : 27.5398
Width : 3.485
Height : 10.083
Entry
ampl
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6
8
10
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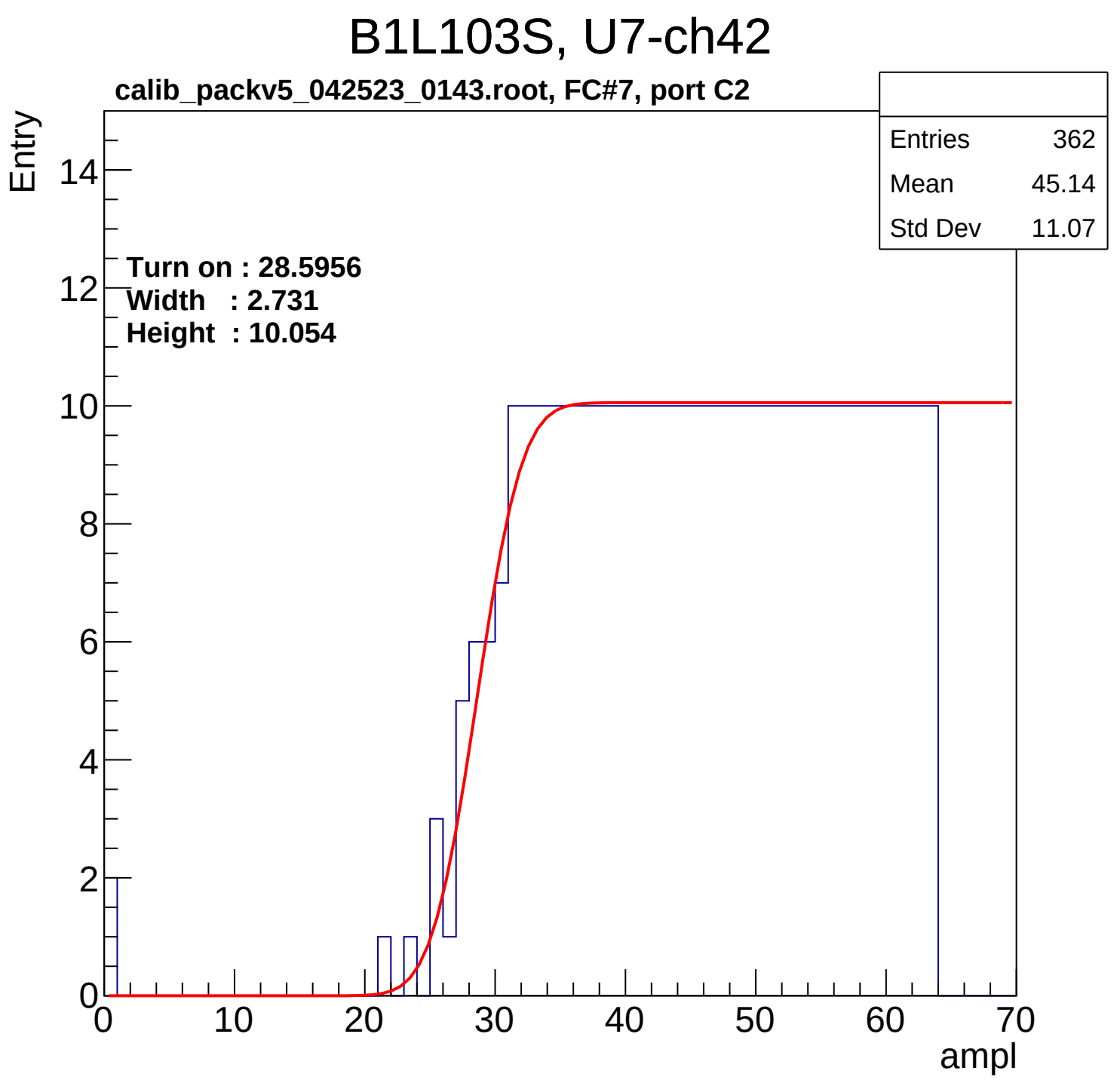
B1L103S, U7-ch42
calib_packv5_042523_0143.root, FC#7, port C2
Entries 362
Mean 45.14
Std Dev 11.07
Turn on : 28.5956
Width : 2.731
Height : 10.054
Entry
ampl
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4
6
8
10
12
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0
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60
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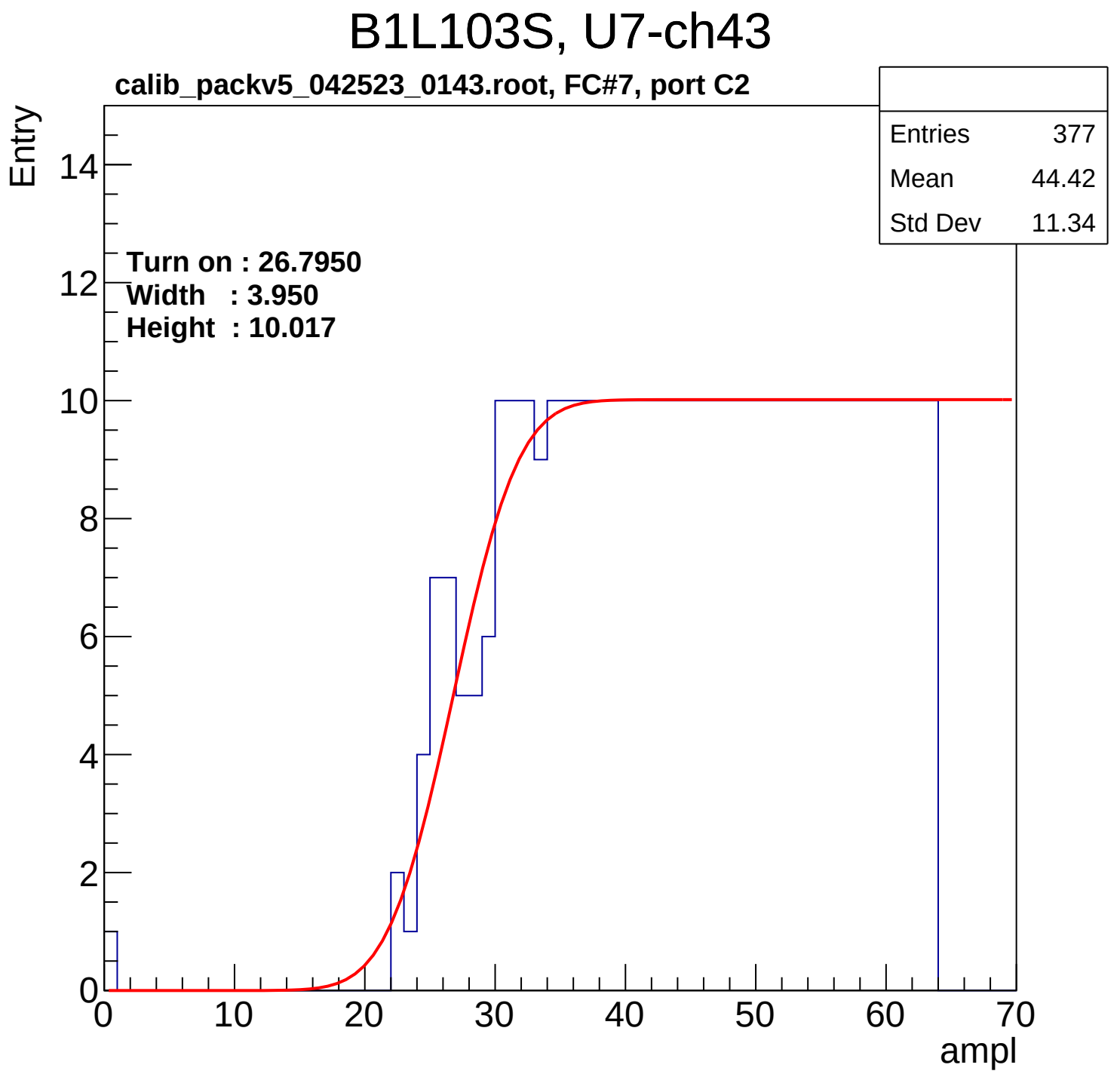
B1L103S, U7-ch43
calib_packv5_042523_0143.root, FC#7, port C2
Entries 377
Mean 44.42
Std Dev 11.34
Turn on : 26.7950
Width : 3.950
Height : 10.017
Entry
ampl
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6
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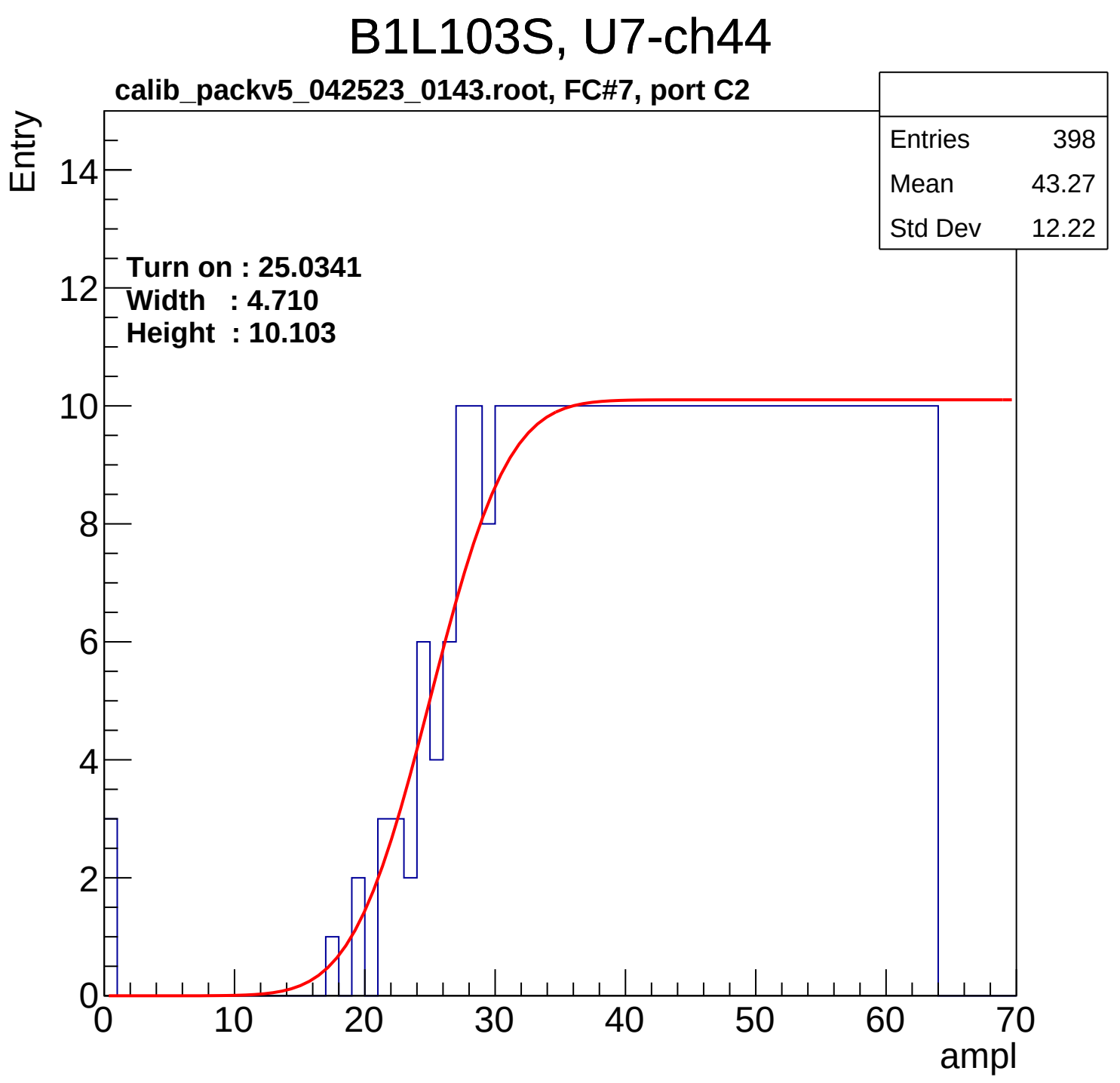
B1L103S, U7-ch44
calib_packv5_042523_0143.root, FC#7, port C2
Entries 398
Mean 43.27
Std Dev 12.22
Turn on : 25.0341
Width : 4.710
Height : 10.103
Entry
ampl
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2
4
6
8
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0
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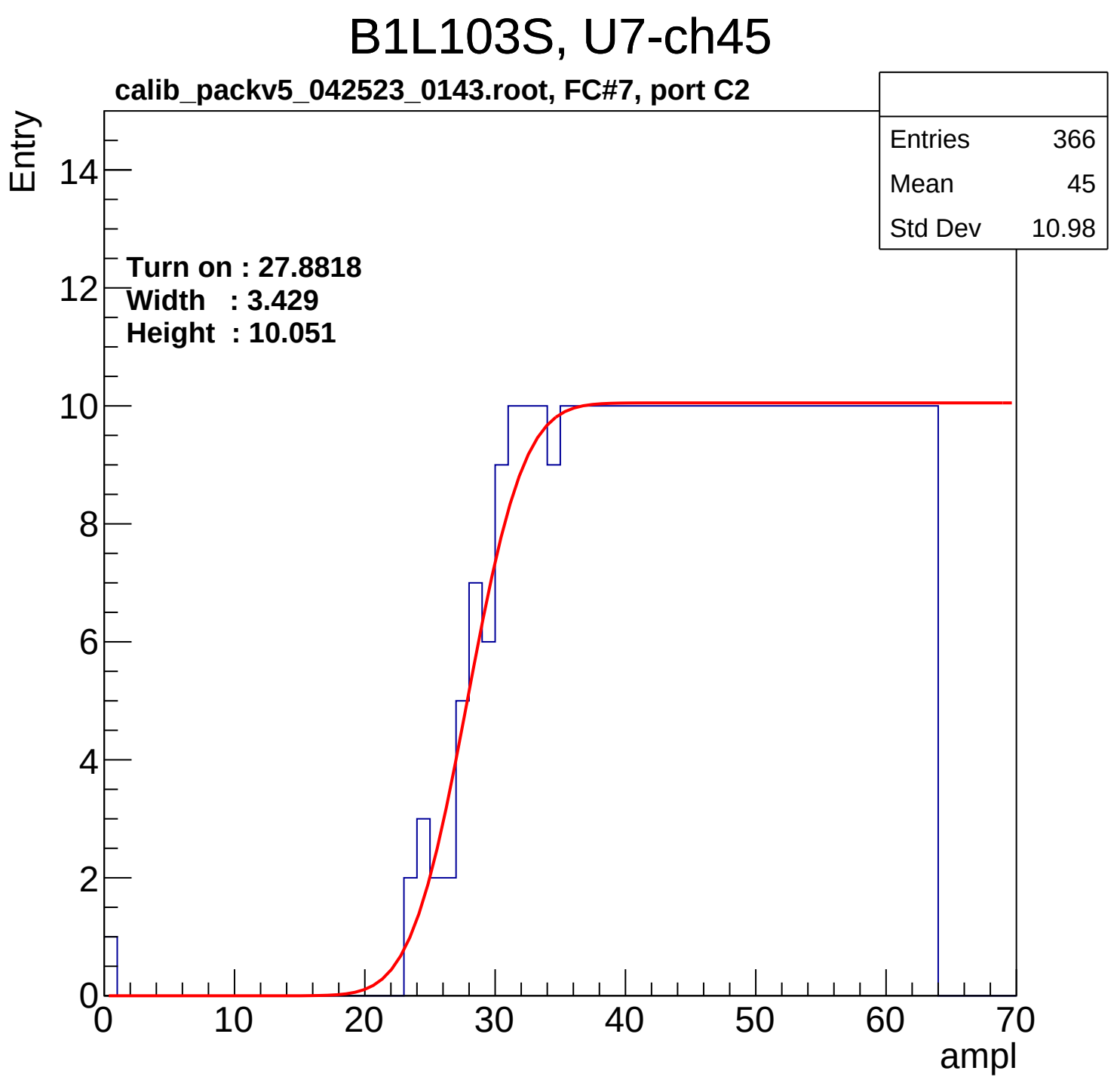
B1L103S, U7-ch45
calib_packv5_042523_0143.root, FC#7, port C2
Entries 366
Mean 45
Std Dev 10.98
Turn on : 27.8818
Width : 3.429
Height : 10.051
Entry
ampl
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10
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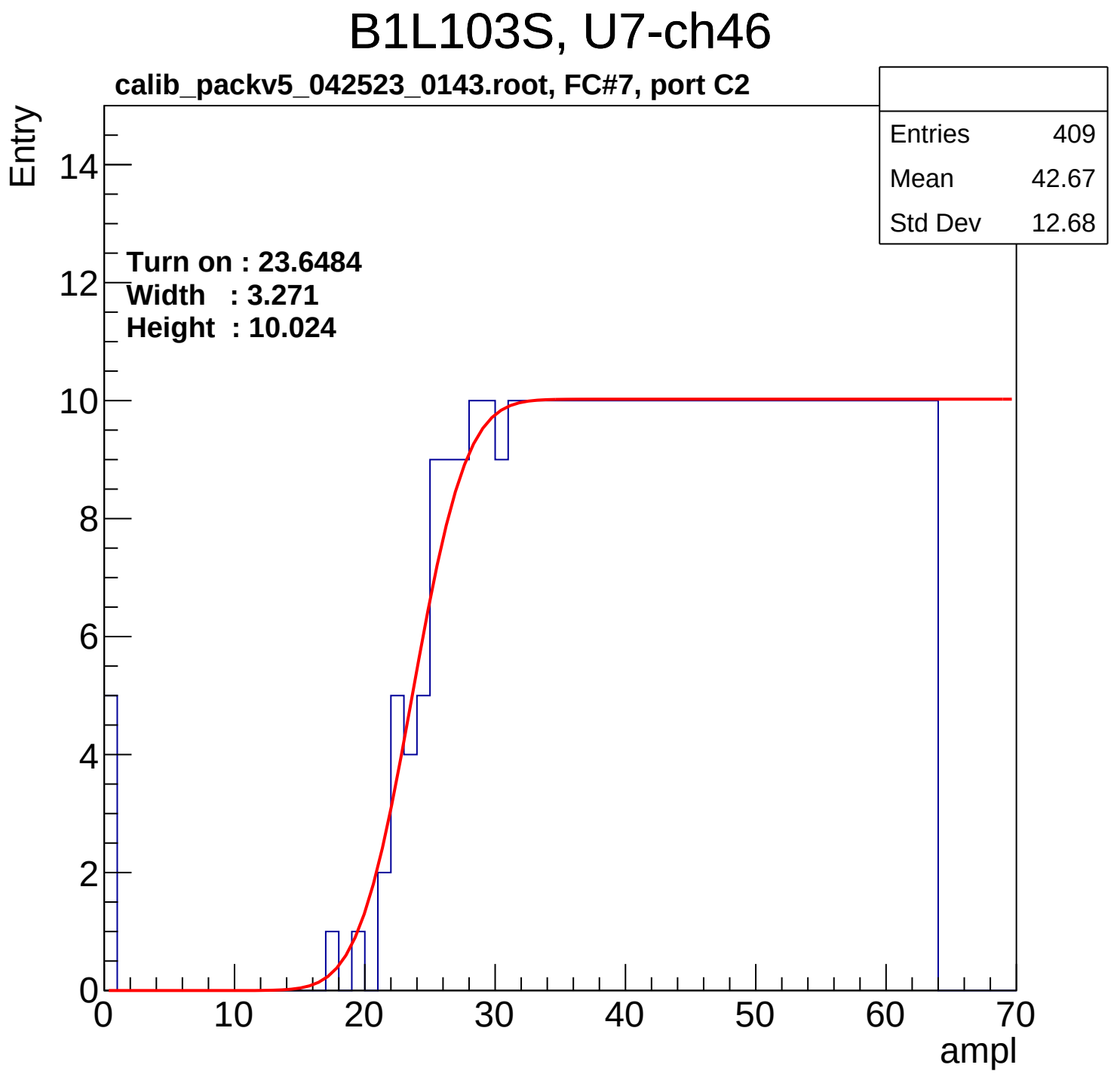
B1L103S, U7-ch46
calib_packv5_042523_0143.root, FC#7, port C2
Entries 409
Mean 42.67
Std Dev 12.68
Turn on : 23.6484
Width : 3.271
Height : 10.024
Entry
ampl
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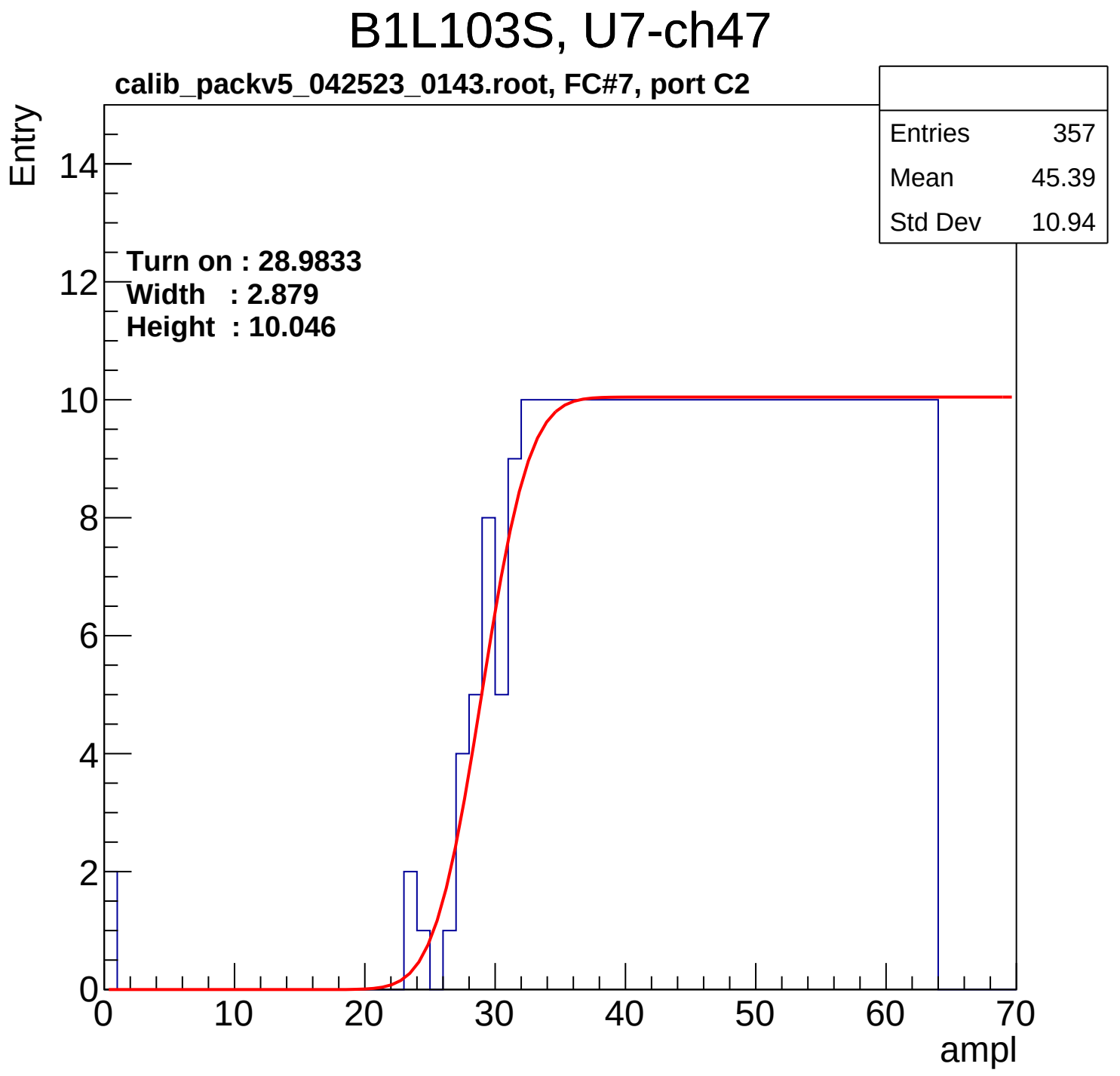
B1L103S, U7-ch47
calib_packv5_042523_0143.root, FC#7, port C2
Entries 357
Mean 45.39
Std Dev 10.94
Turn on : 28.9833
Width : 2.879
Height : 10.046
Entry
ampl
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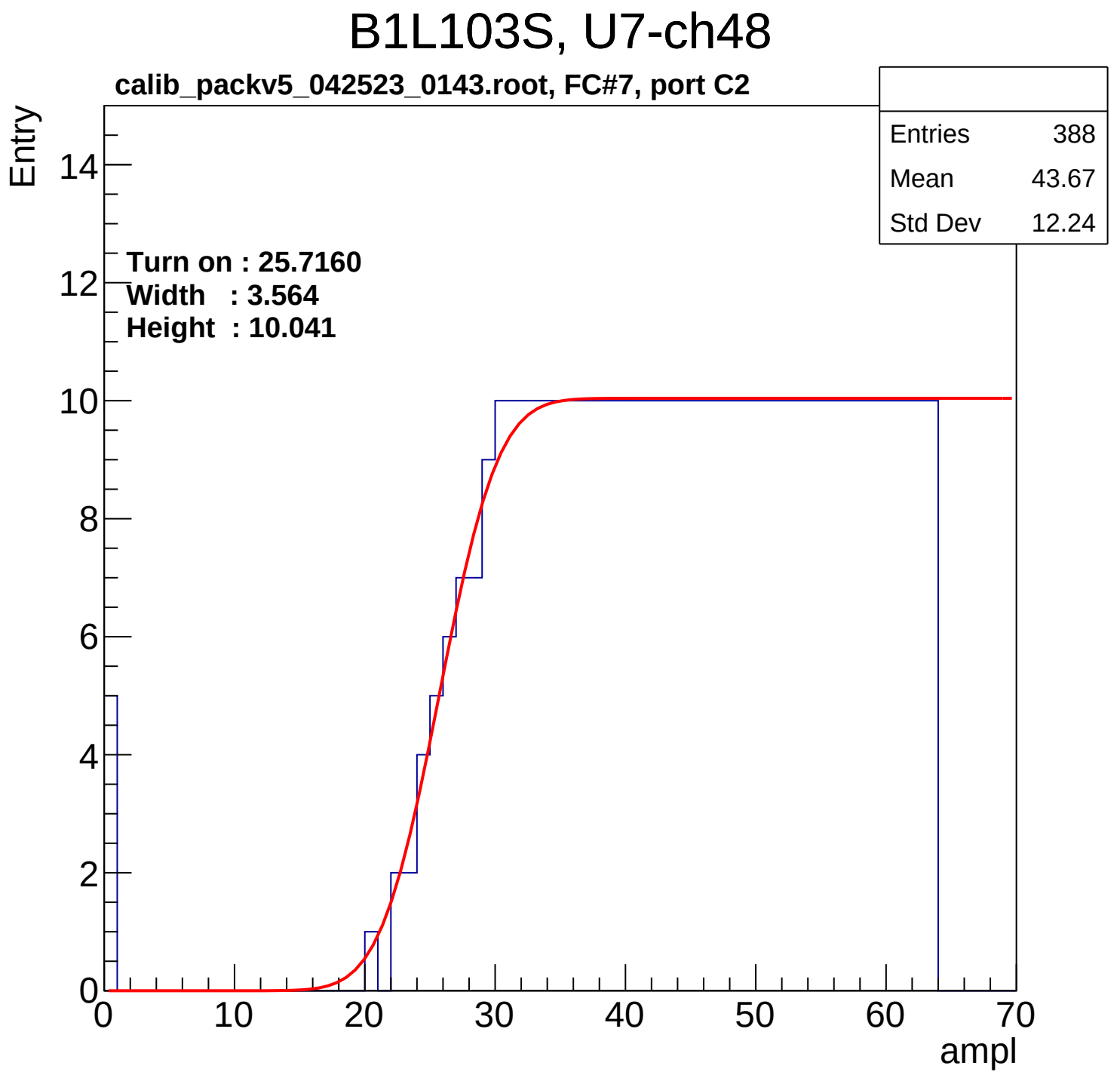
B1L103S, U7-ch48
calib_packv5_042523_0143.root, FC#7, port C2
Entries 388
Mean 43.67
Std Dev 12.24
Turn on : 25.7160
Width : 3.564
Height : 10.041
Entry
ampl
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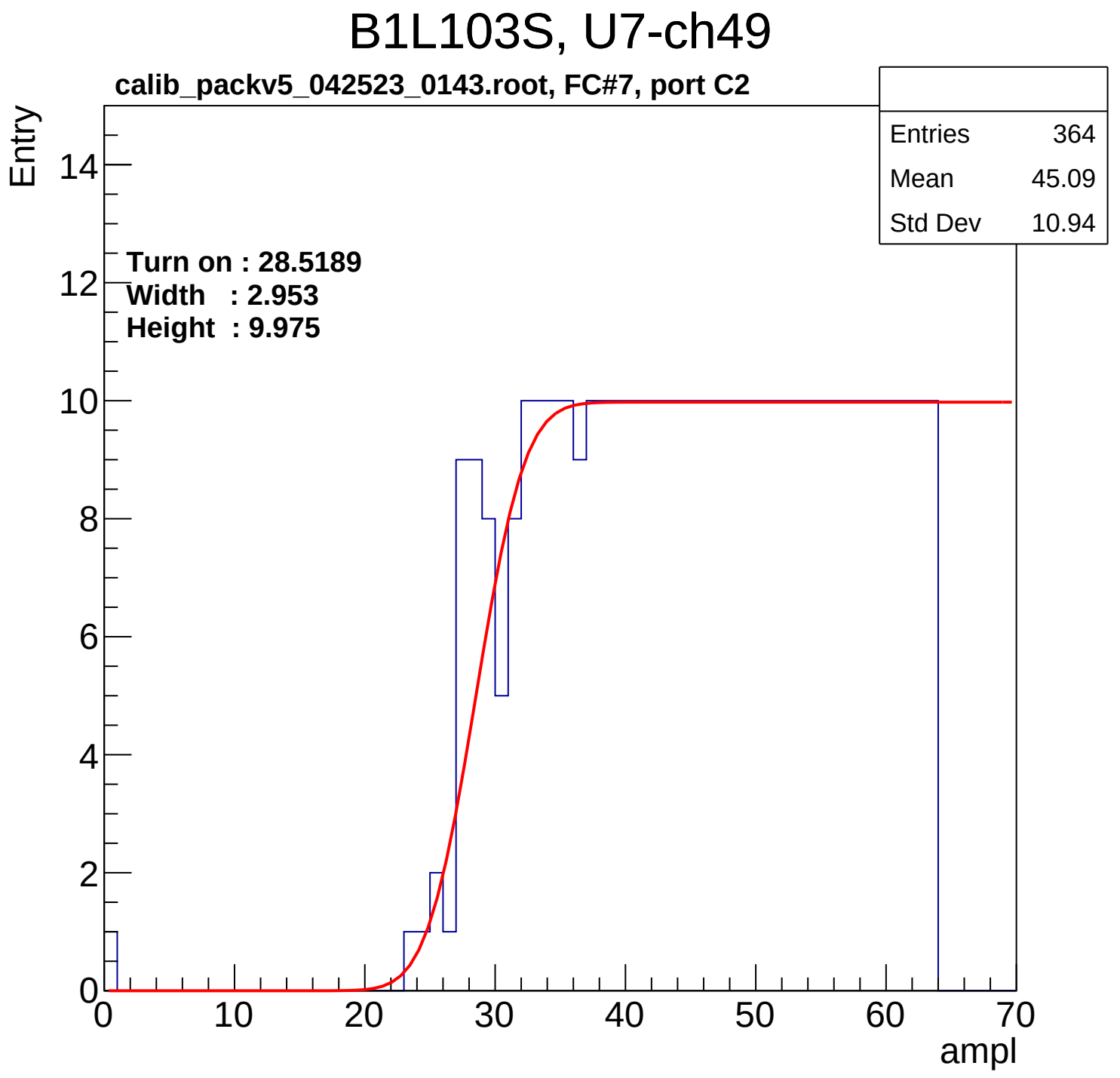
B1L103S, U7-ch49
calib_packv5_042523_0143.root, FC#7, port C2
Entries 364
Mean 45.09
Std Dev 10.94
Turn on : 28.5189
Width : 2.953
Height : 9.975
Entry
ampl
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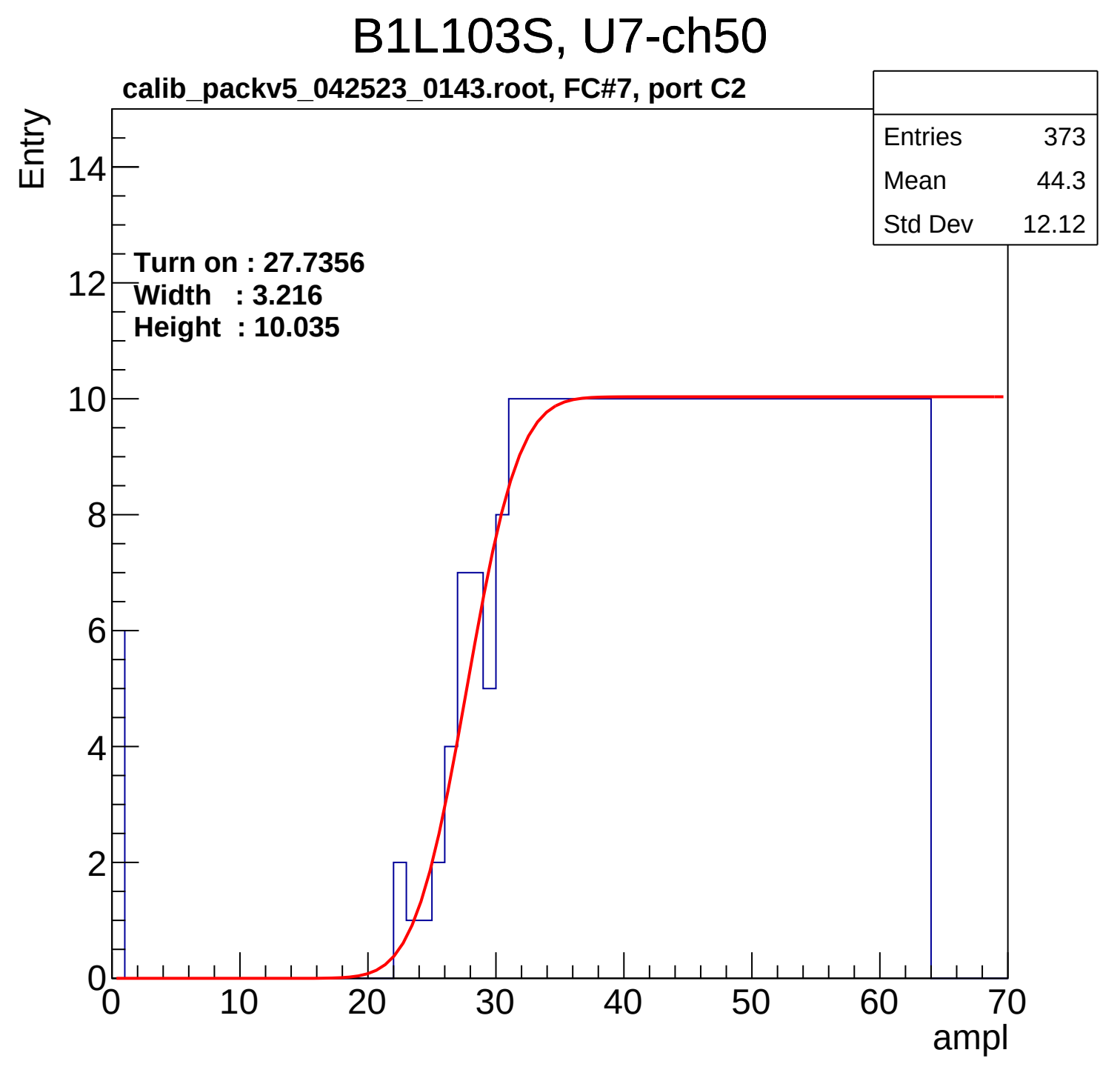
B1L103S, U7-ch50
calib_packv5_042523_0143.root, FC#7, port C2
Entries 373
Mean 44.3
Std Dev 12.12
Turn on : 27.7356
Width : 3.216
Height : 10.035
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ampl
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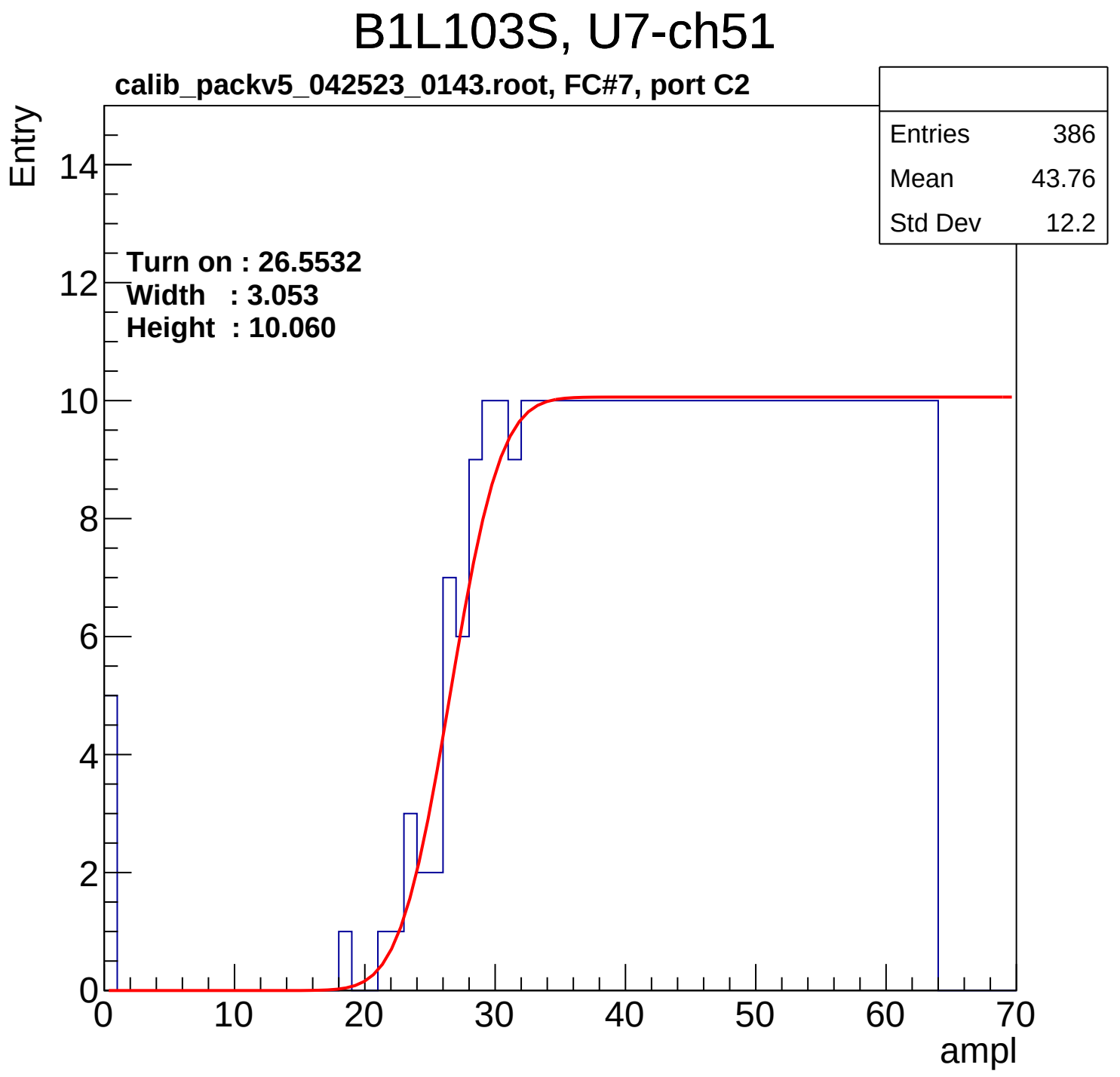
B1L103S, U7-ch51
calib_packv5_042523_0143.root, FC#7, port C2
Entries 386
Mean 43.76
Std Dev 12.2
Turn on : 26.5532
Width : 3.053
Height : 10.060
Entry
ampl
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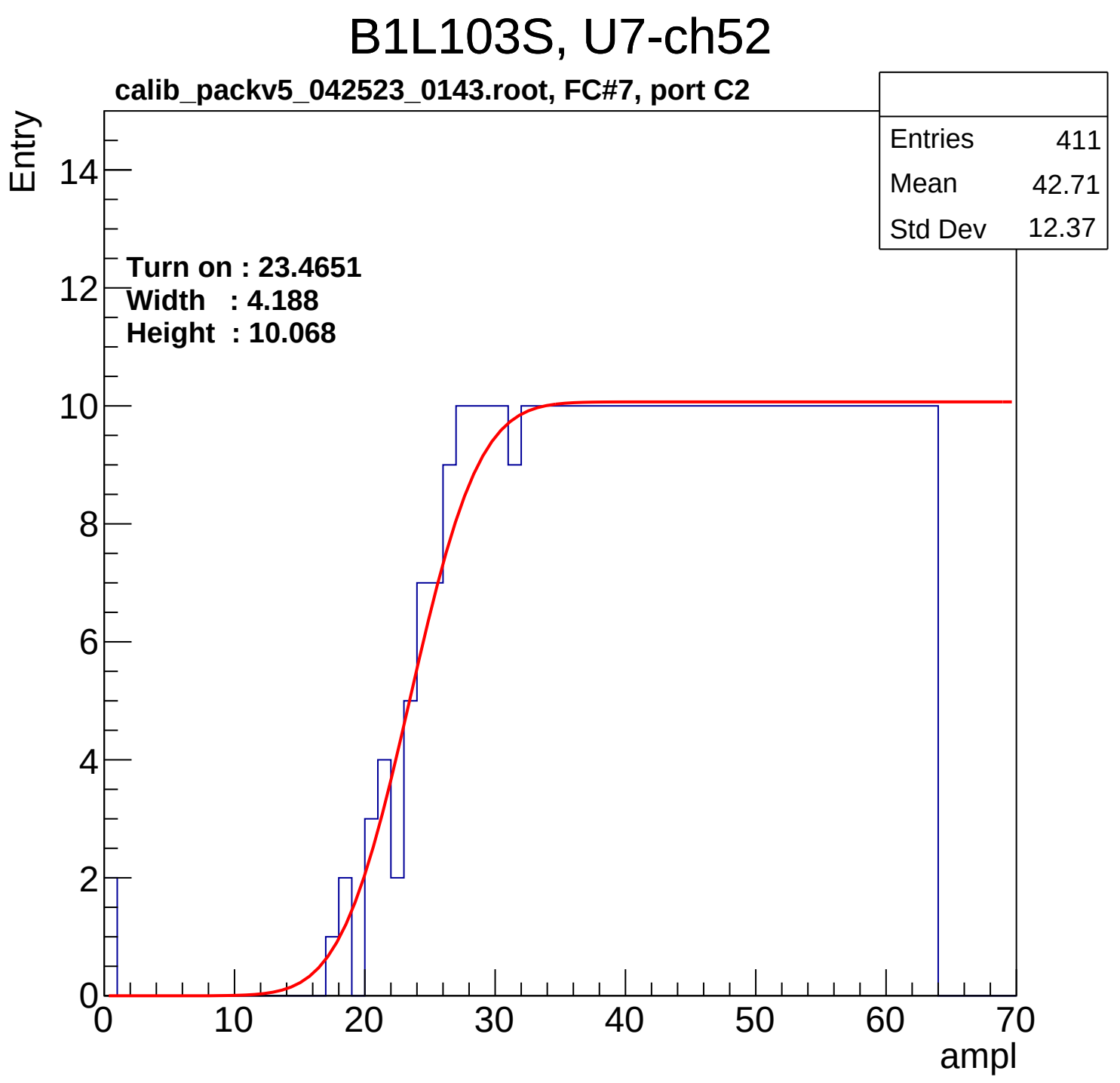
B1L103S, U7-ch52
calib_packv5_042523_0143.root, FC#7, port C2
Entries 411
Mean 42.71
Std Dev 12.37
Turn on : 23.4651
Width : 4.188
Height : 10.068
Entry
ampl
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4
6
8
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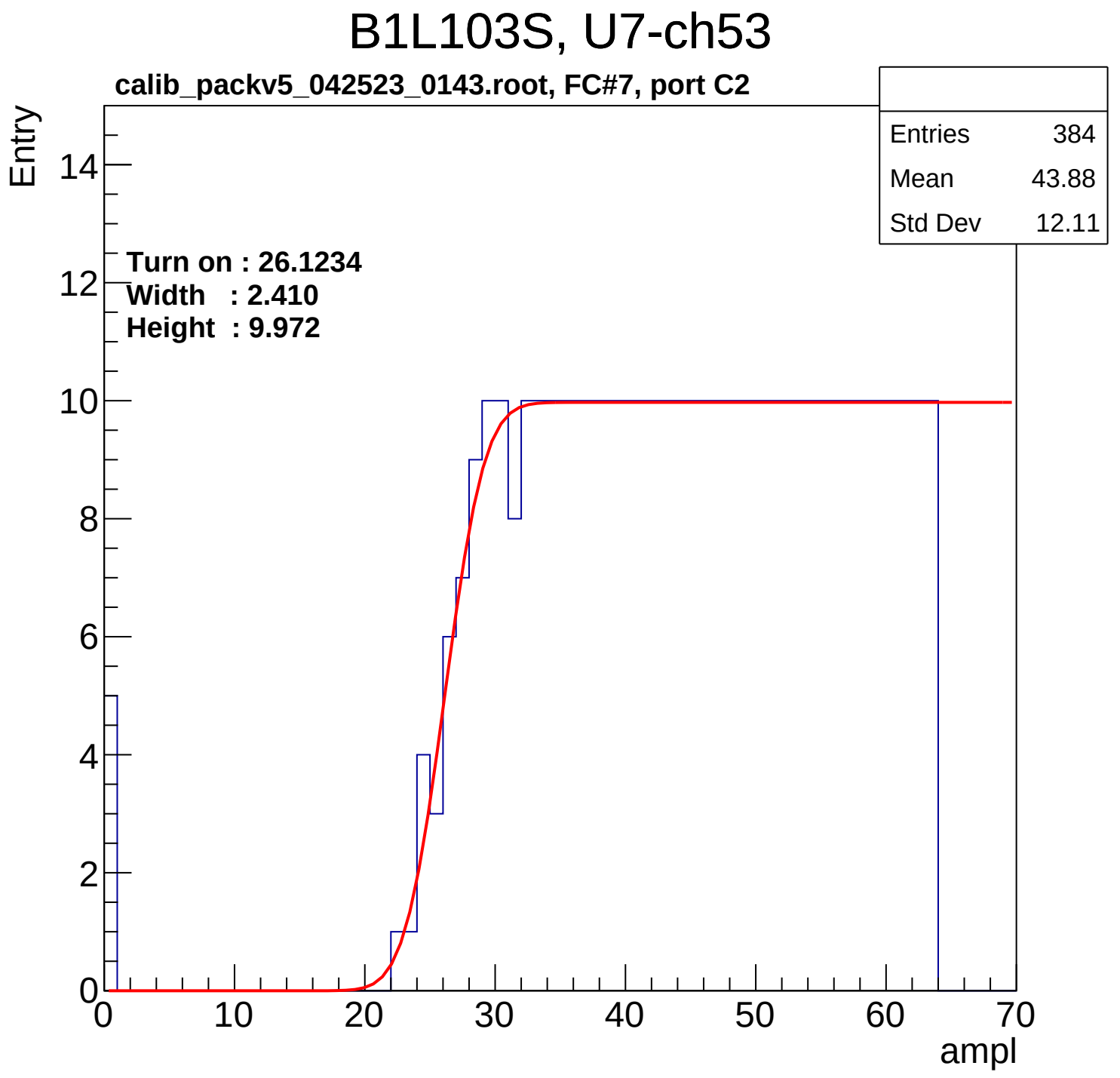
B1L103S, U7-ch53
calib_packv5_042523_0143.root, FC#7, port C2
Entries 384
Mean 43.88
Std Dev 12.11
Turn on : 26.1234
Width : 2.410
Height : 9.972
Entry
ampl
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6
8
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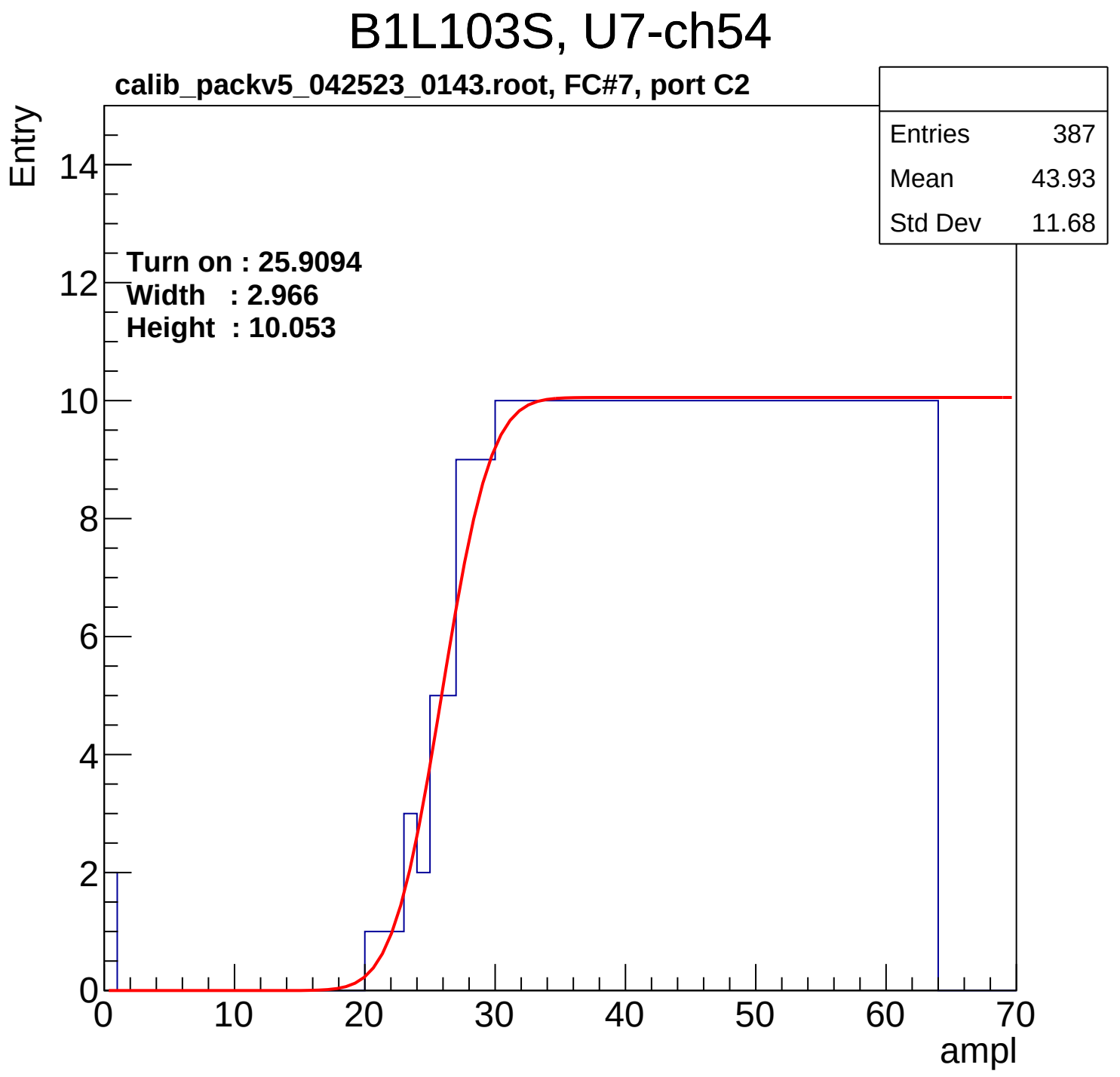
B1L103S, U7-ch54
calib_packv5_042523_0143.root, FC#7, port C2
Entries 387
Mean 43.93
Std Dev 11.68
Turn on : 25.9094
Width : 2.966
Height : 10.053
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ampl
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6
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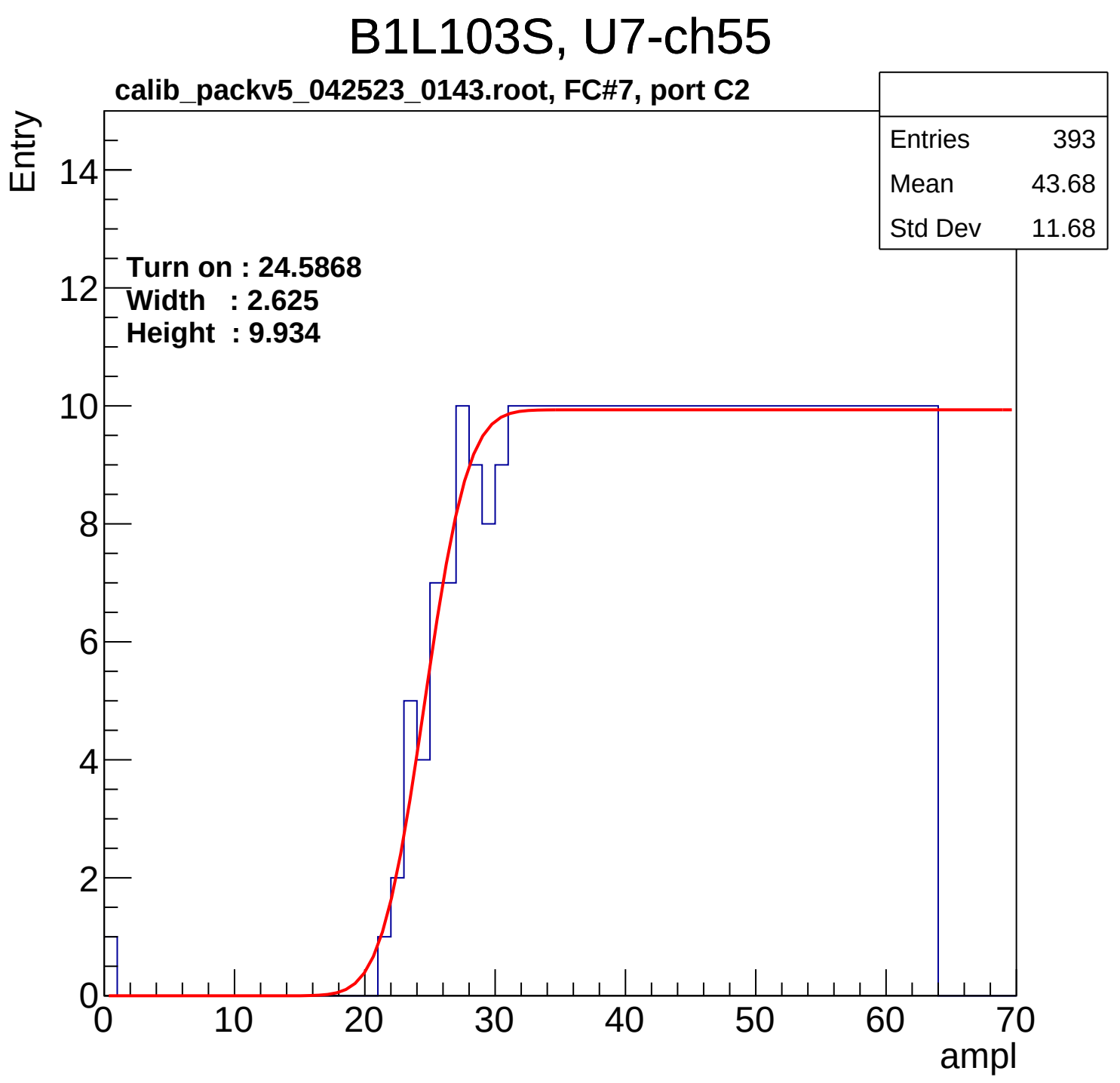
B1L103S, U7-ch55
calib_packv5_042523_0143.root, FC#7, port C2
Entries 393
Mean 43.68
Std Dev 11.68
Turn on : 24.5868
Width : 2.625
Height : 9.934
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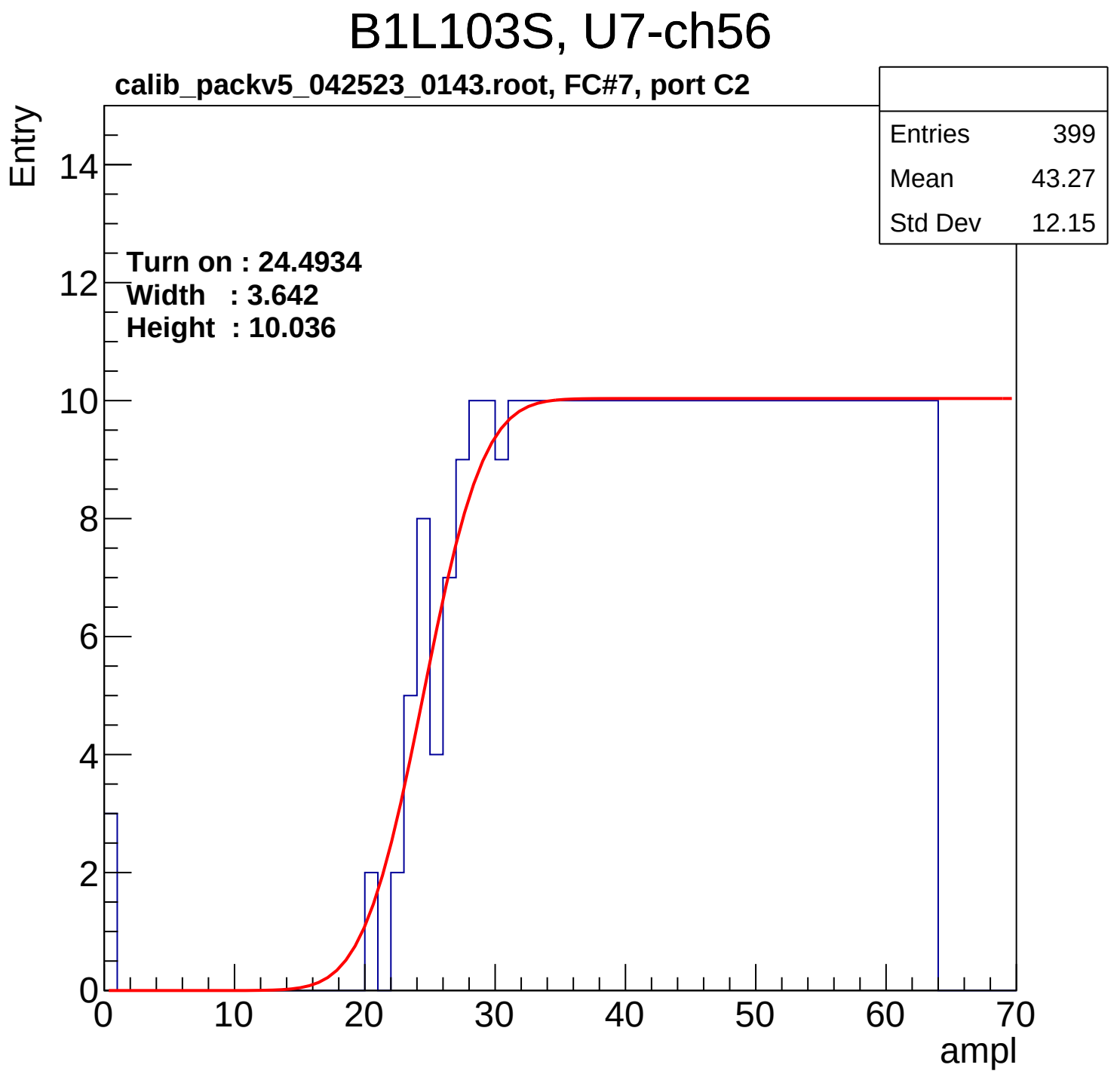
B1L103S, U7-ch56
calib_packv5_042523_0143.root, FC#7, port C2
Entries 399
Mean 43.27
Std Dev 12.15
Turn on : 24.4934
Width : 3.642
Height : 10.036
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ampl
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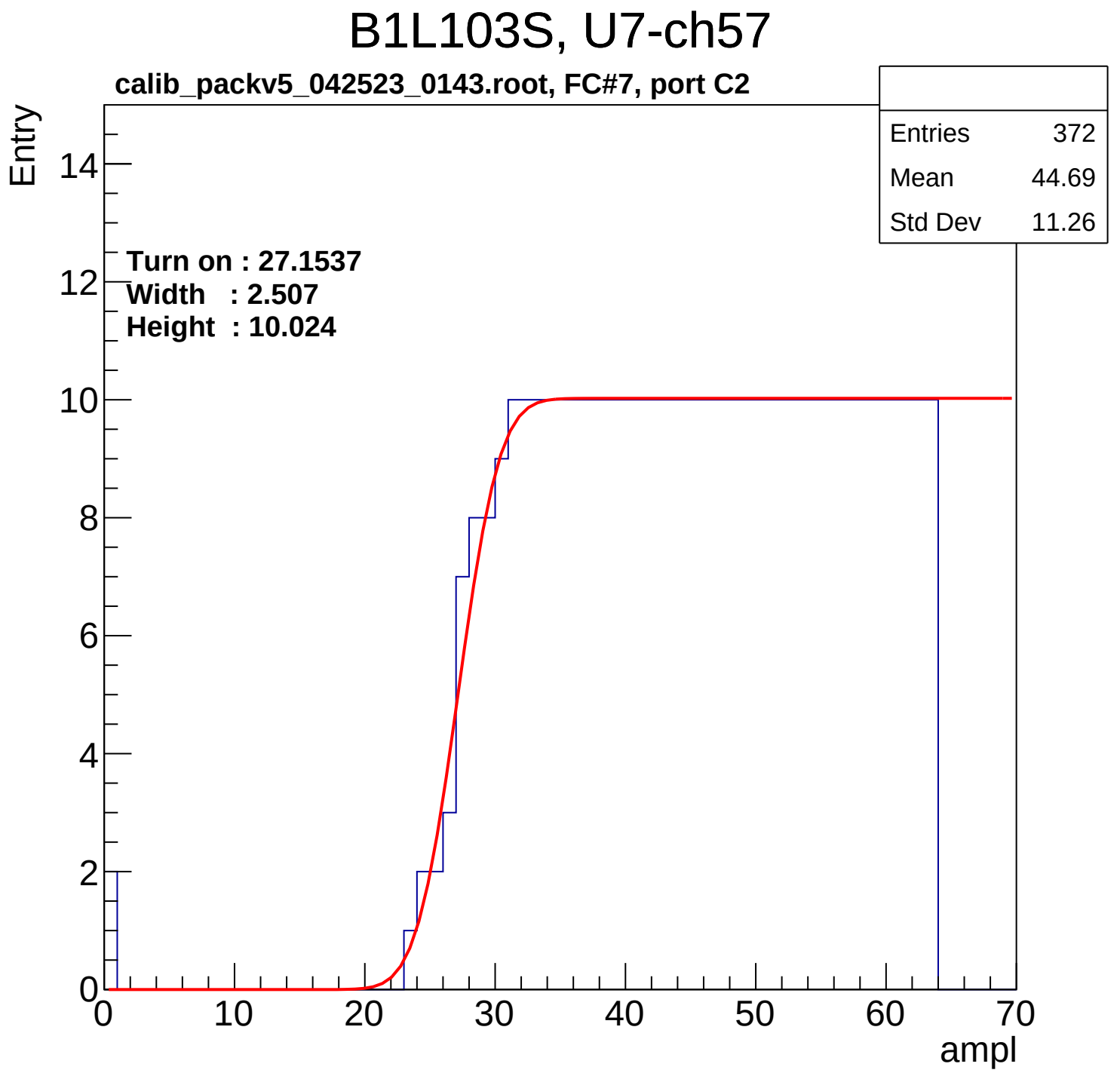
B1L103S, U7-ch57
calib_packv5_042523_0143.root, FC#7, port C2
Entries 372
Mean 44.69
Std Dev 11.26
Turn on : 27.1537
Width : 2.507
Height : 10.024
Entry
ampl
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4
6
8
10
12
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20
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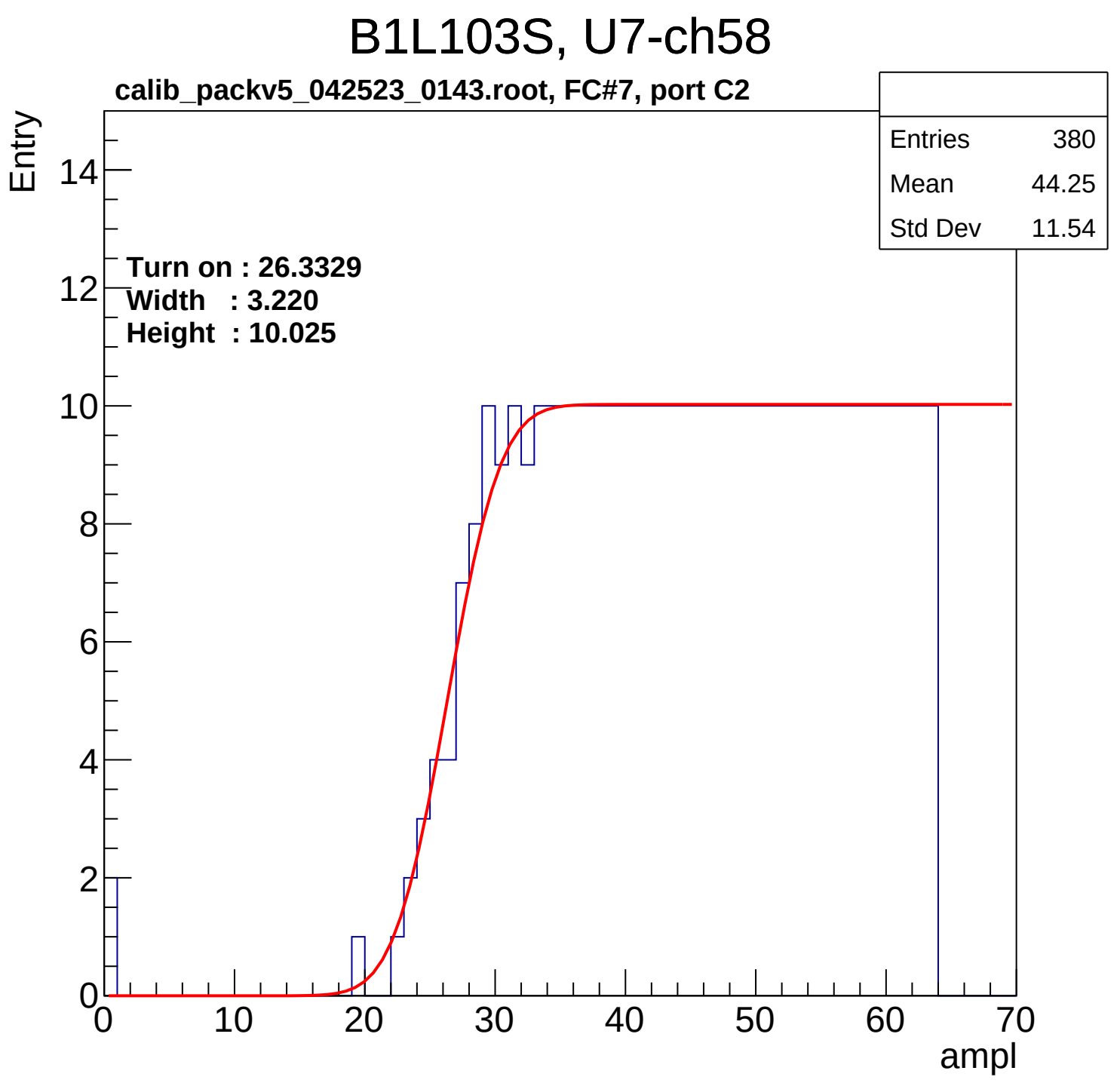
B1L103S, U7-ch58
calib_packv5_042523_0143.root, FC#7, port C2
Entries 380
Mean 44.25
Std Dev 11.54
Turn on : 26.3329
Width : 3.220
Height : 10.025
Entry
ampl
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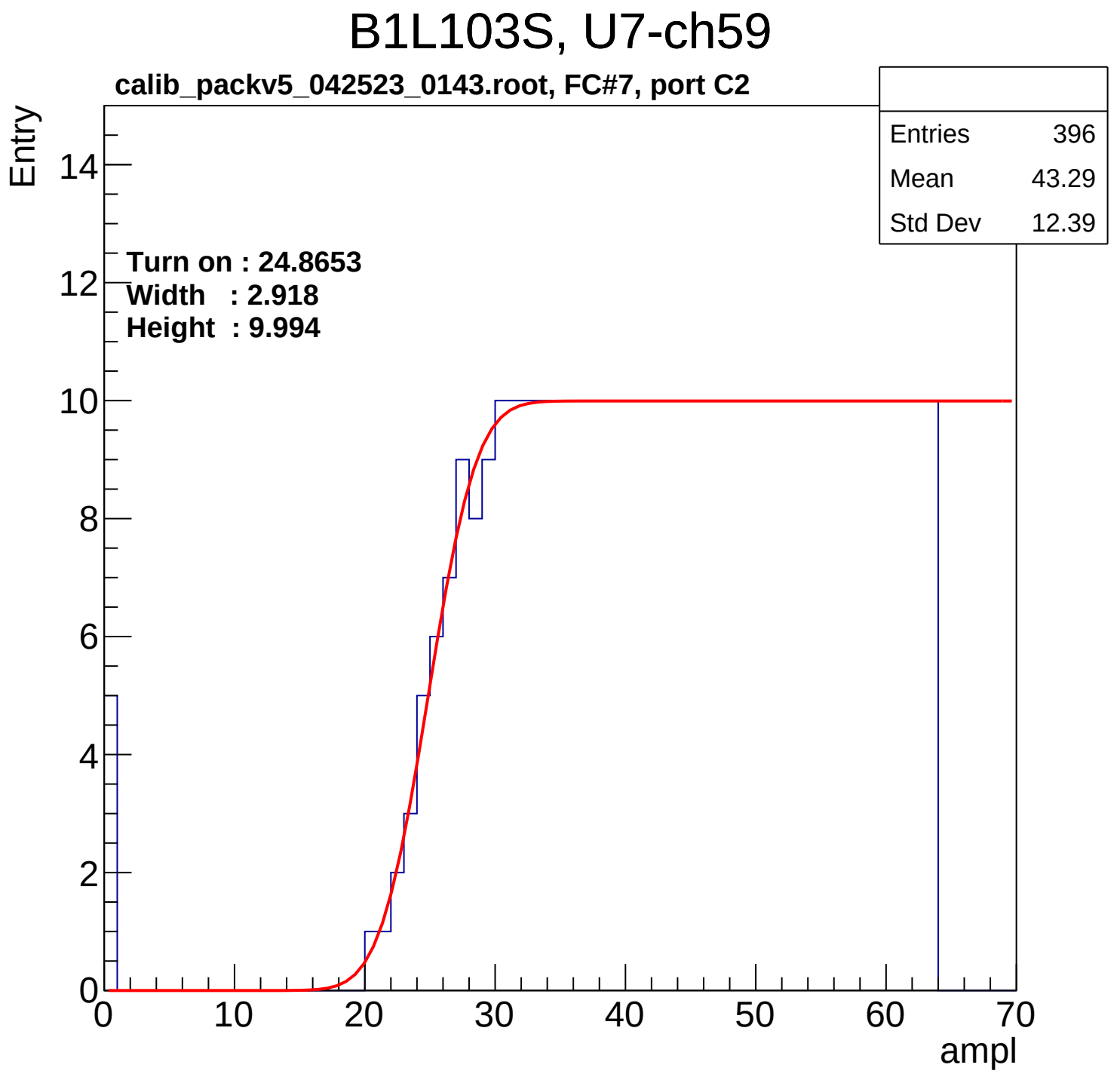
B1L103S, U7-ch59
calib_packv5_042523_0143.root, FC#7, port C2
Entries 396
Mean 43.29
Std Dev 12.39
Turn on : 24.8653
Width : 2.918
Height : 9.994
Entry
ampl
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2
4
6
8
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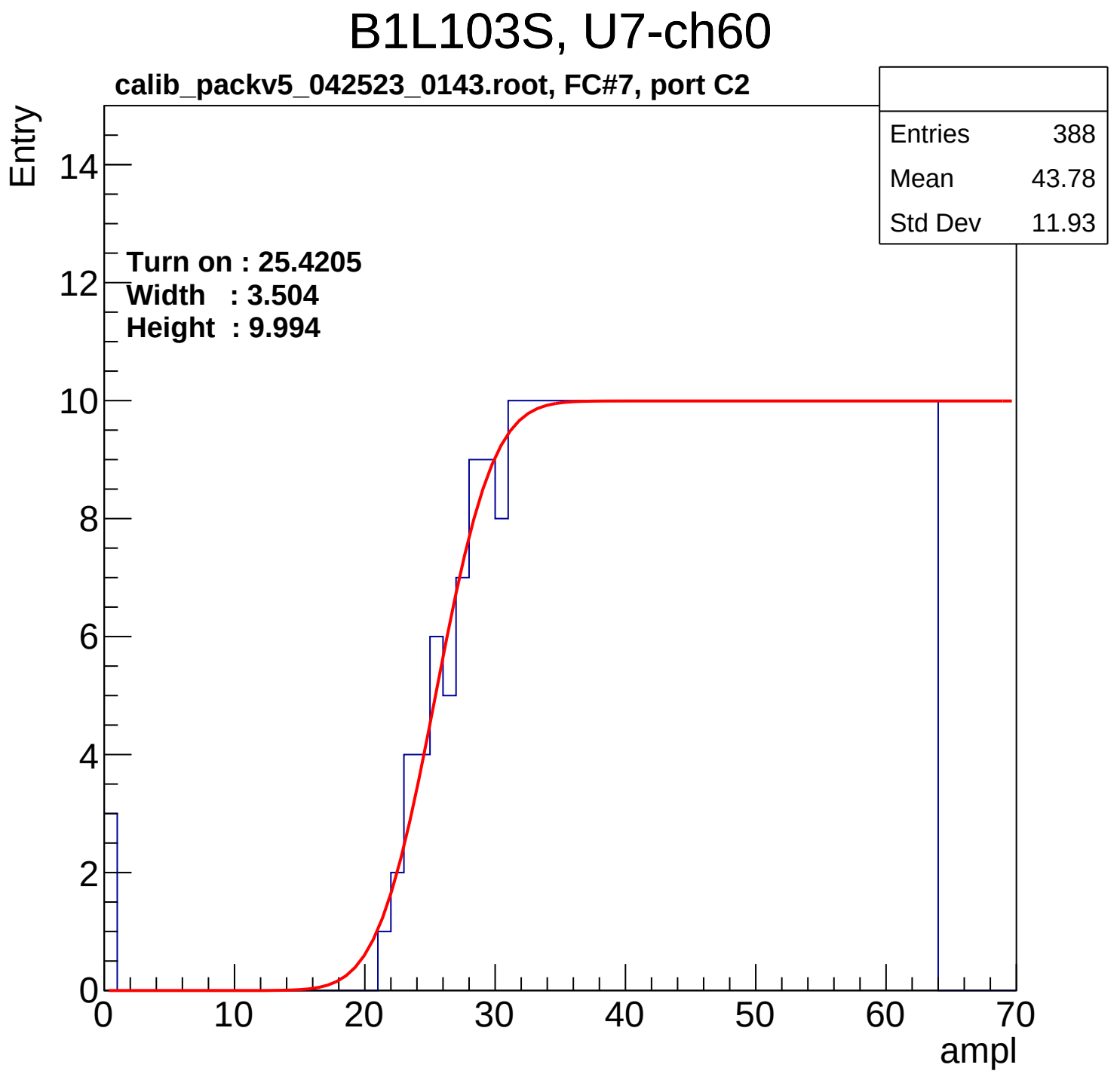
B1L103S, U7-ch60
calib_packv5_042523_0143.root, FC#7, port C2
Entries 388
Mean 43.78
Std Dev 11.93
Turn on : 25.4205
Width : 3.504
Height : 9.994
Entry
ampl
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2
4
6
8
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0
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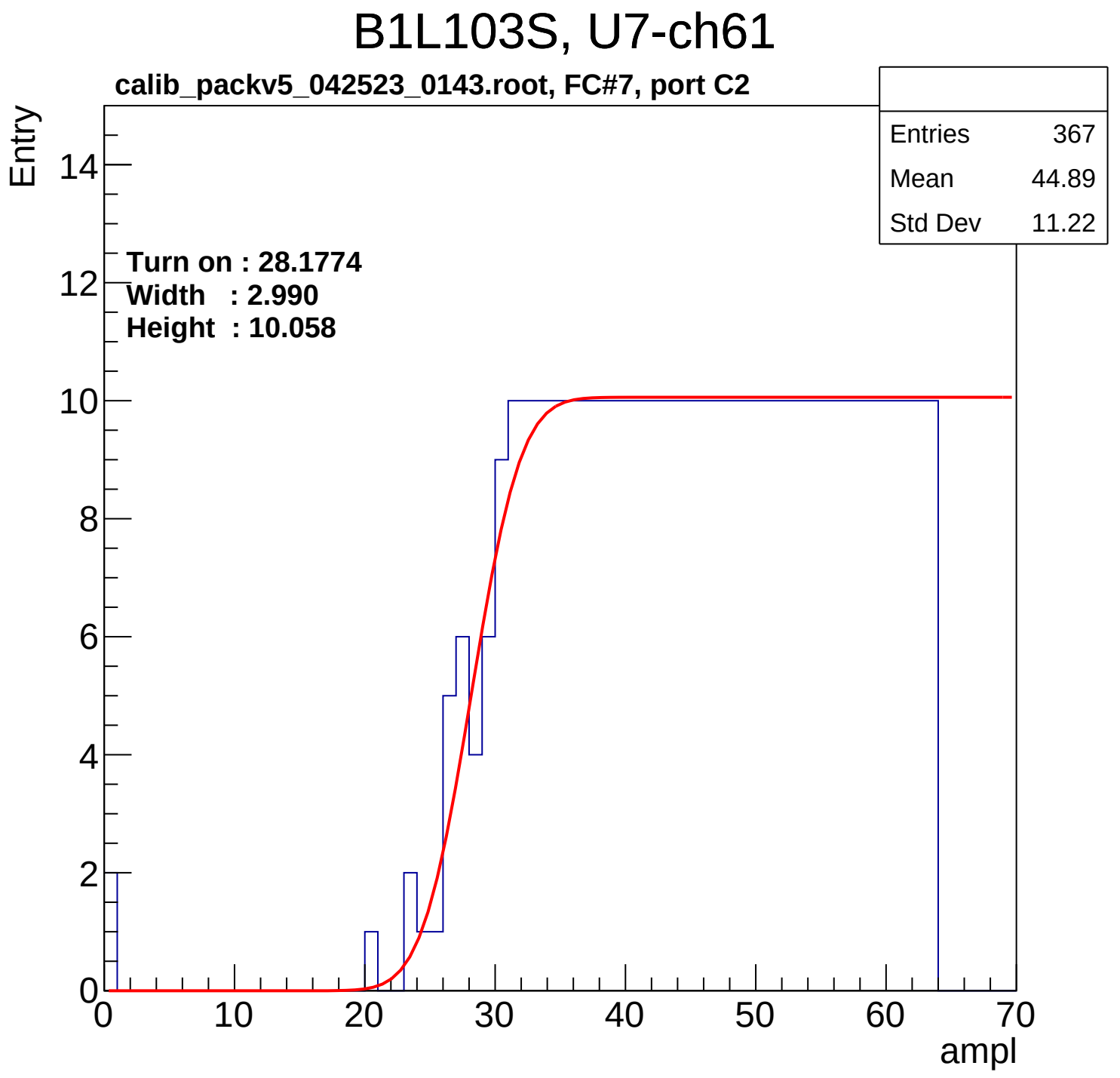
B1L103S, U7-ch61
calib_packv5_042523_0143.root, FC#7, port C2
Entries 367
Mean 44.89
Std Dev 11.22
Turn on : 28.1774
Width : 2.990
Height : 10.058
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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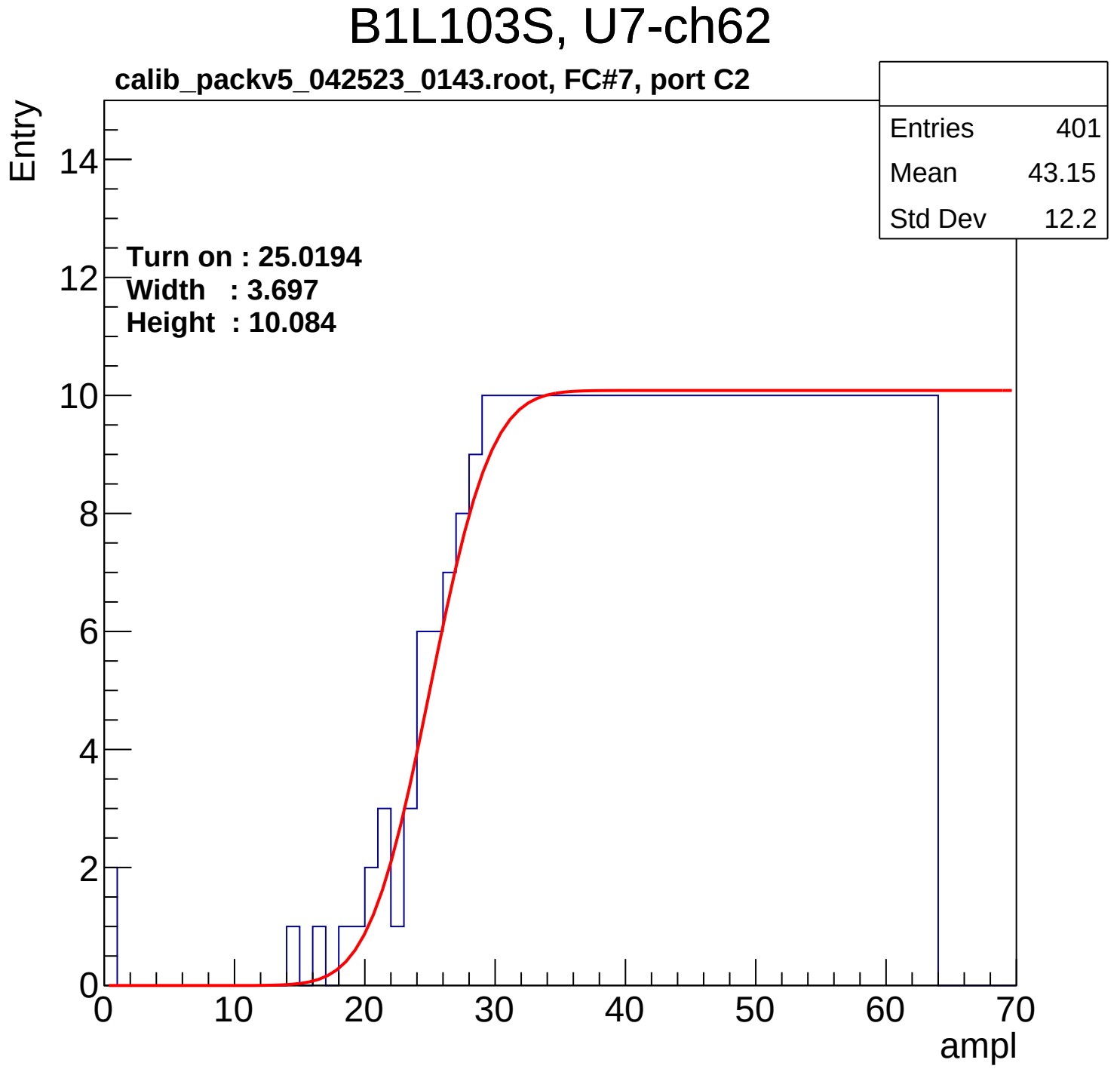
B1L103S, U7-ch62
calib_packv5_042523_0143.root, FC#7, port C2
Entries 401
Mean 43.15
Std Dev 12.2
Turn on : 25.0194
Width : 3.697
Height : 10.084
Entry
ampl
0
2
4
6
8
10
12
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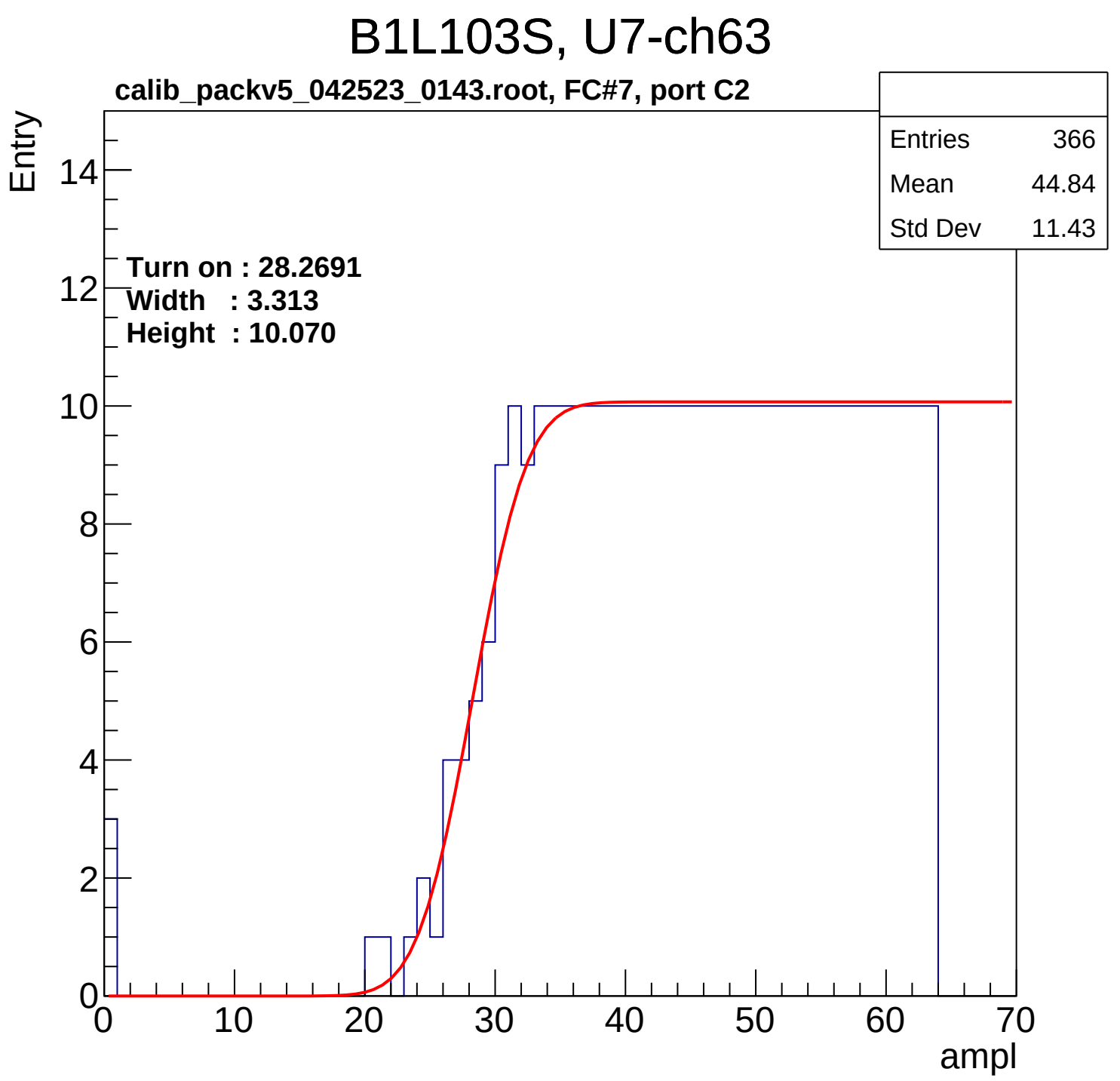
B1L103S, U7-ch63
calib_packv5_042523_0143.root, FC#7, port C2
Entries 366
Mean 44.84
Std Dev 11.43
Turn on : 28.2691
Width : 3.313
Height : 10.070
Entry
ampl
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2
4
6
8
10
12
14
0
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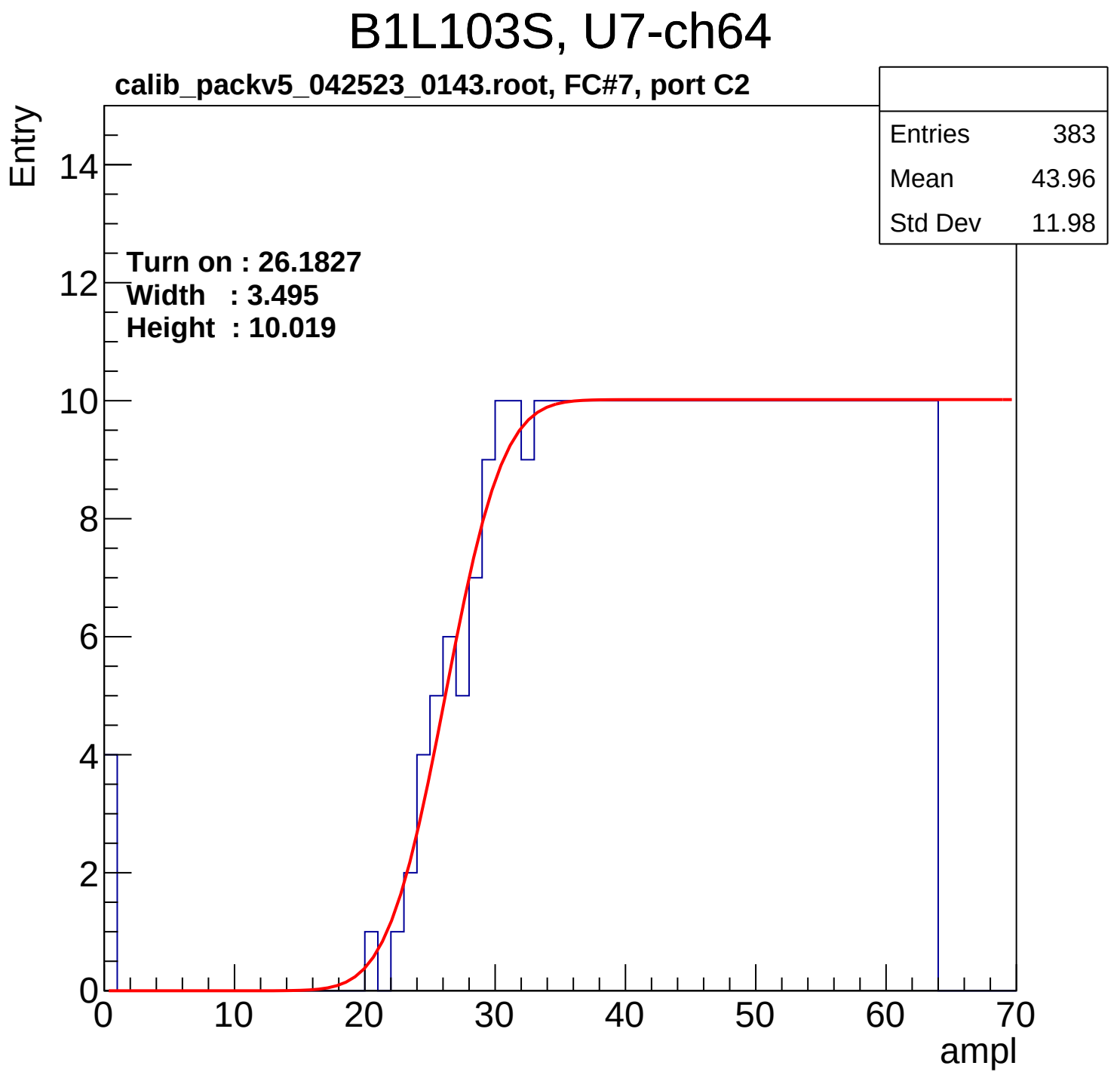
B1L103S, U7-ch64
calib_packv5_042523_0143.root, FC#7, port C2
Entries 383
Mean 43.96
Std Dev 11.98
Turn on : 26.1827
Width : 3.495
Height : 10.019
Entry
ampl
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2
4
6
8
10
12
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0
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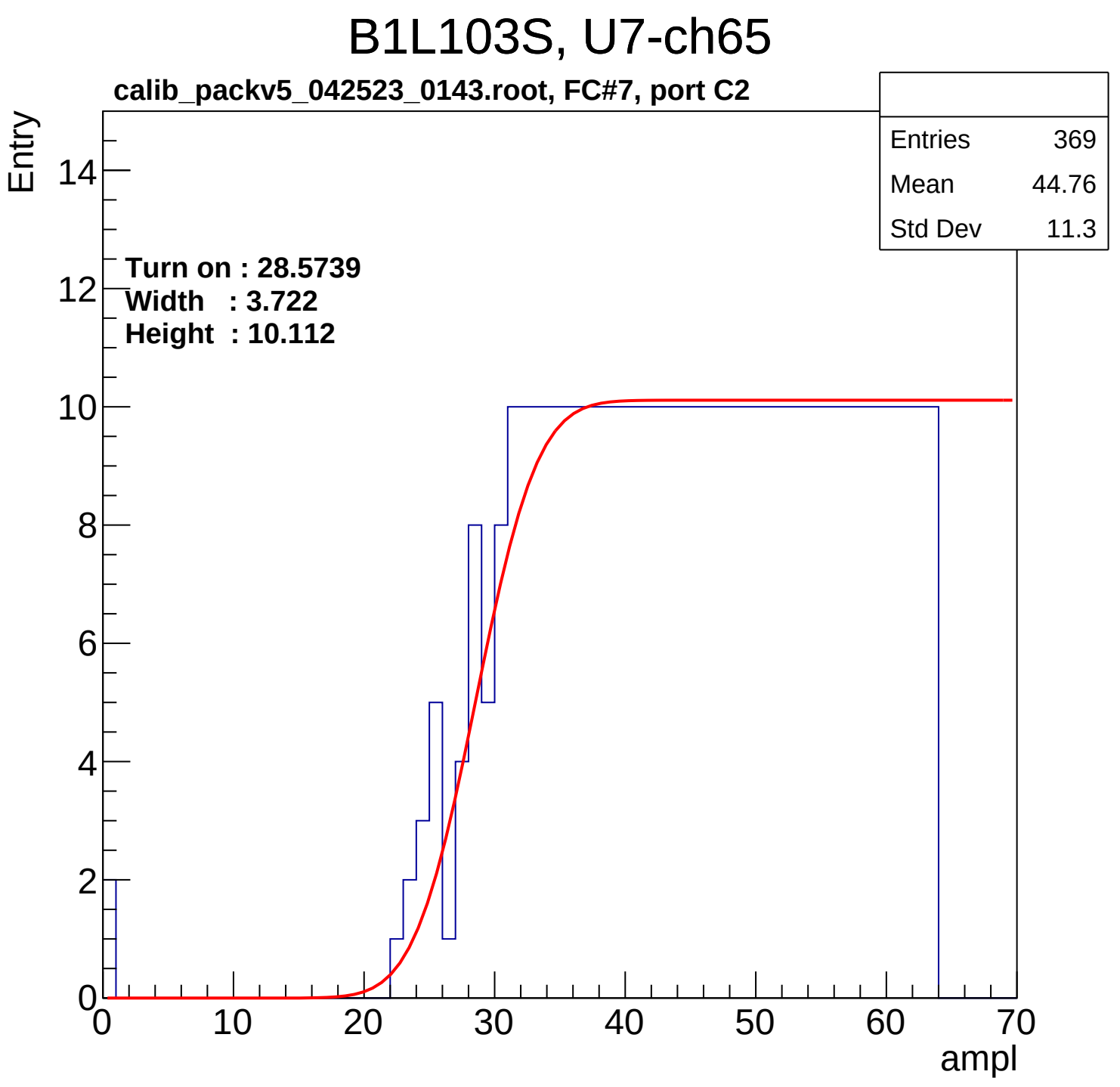
B1L103S, U7-ch65
calib_packv5_042523_0143.root, FC#7, port C2
Entries 369
Mean 44.76
Std Dev 11.3
Turn on : 28.5739
Width : 3.722
Height : 10.112
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
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60
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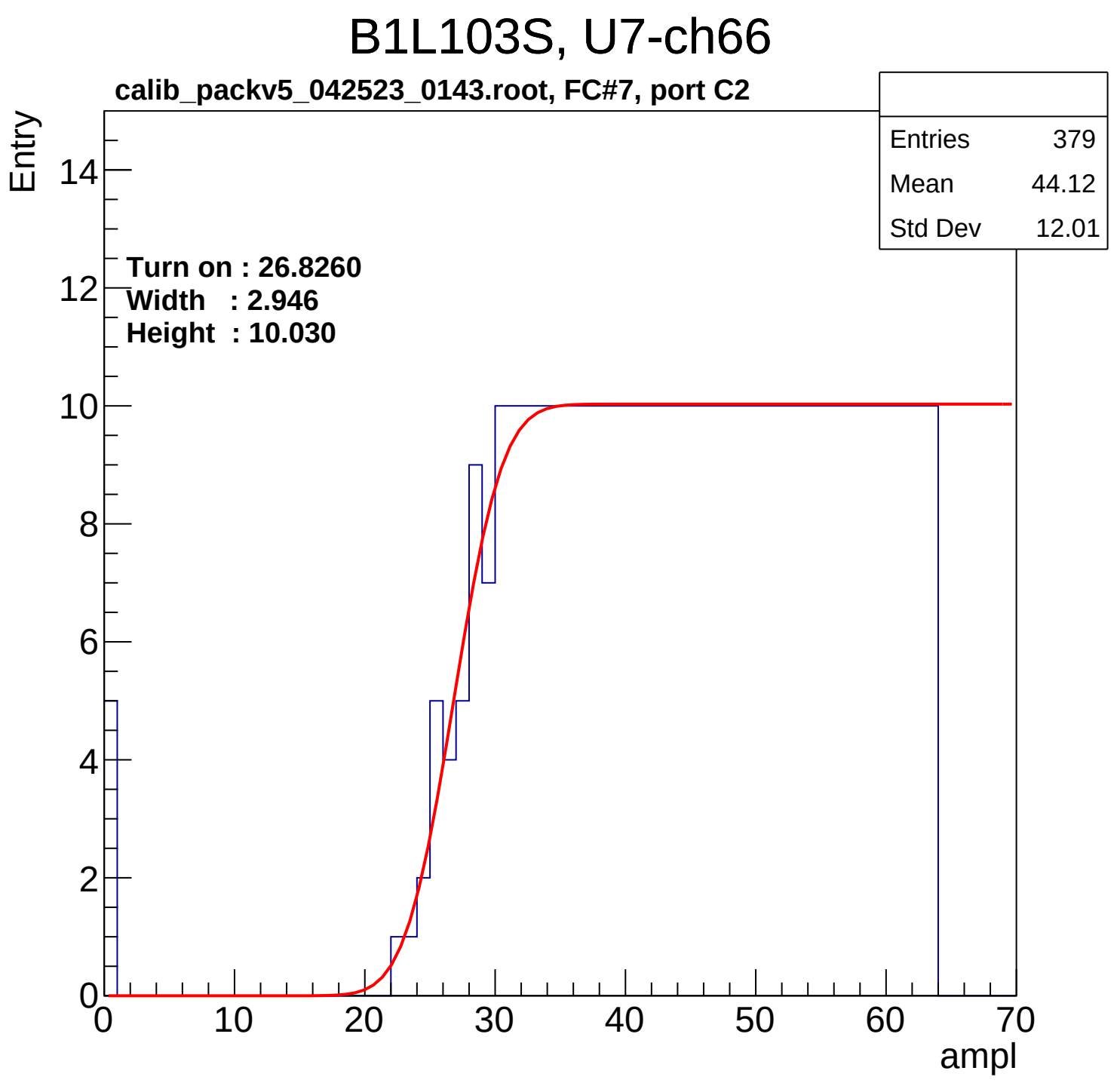
B1L103S, U7-ch66
calib_packv5_042523_0143.root, FC#7, port C2
Entries 379
Mean 44.12
Std Dev 12.01
Turn on : 26.8260
Width : 2.946
Height : 10.030
Entry
ampl
0
2
4
6
8
10
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0
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60
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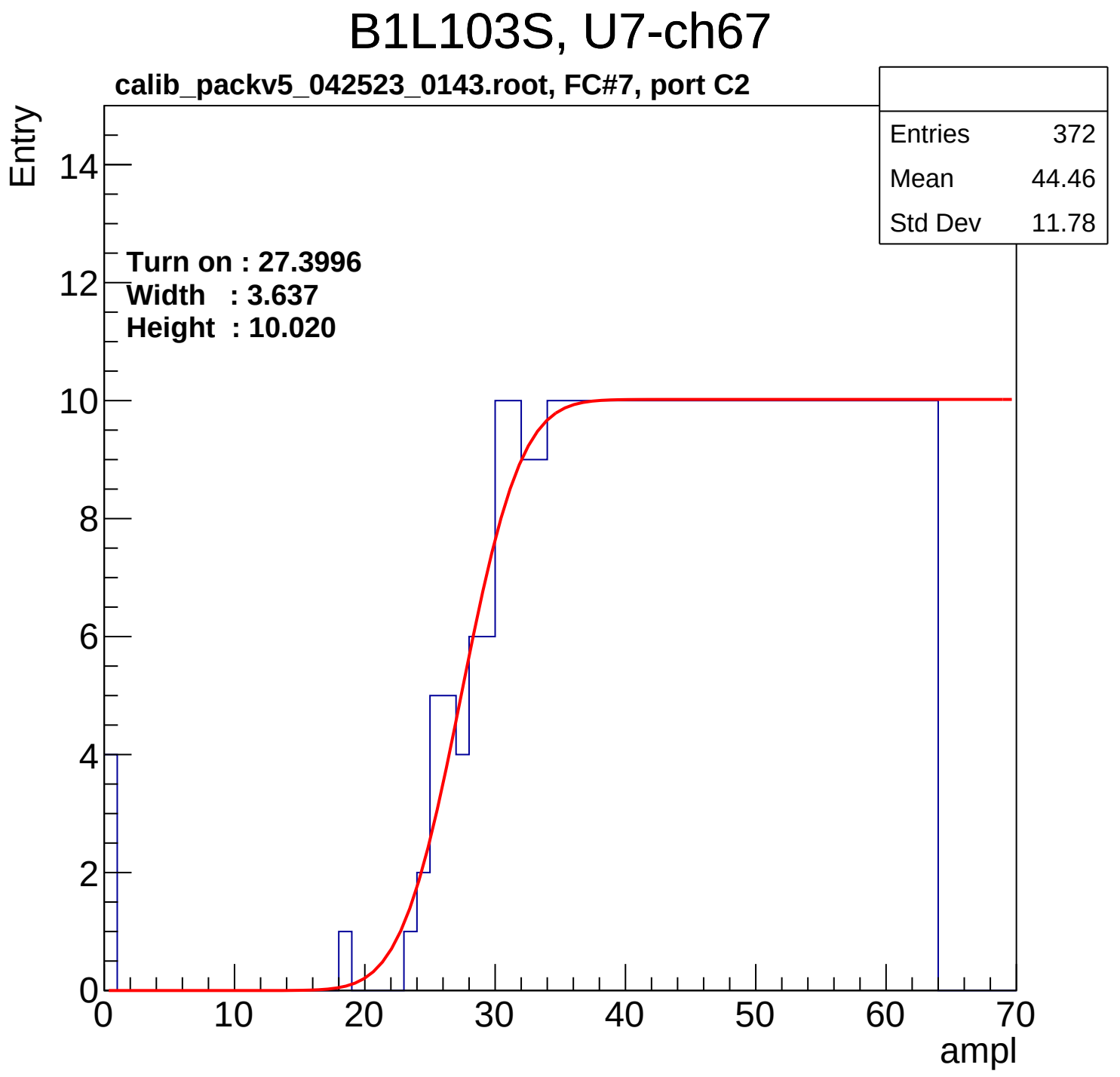
B1L103S, U7-ch67
calib_packv5_042523_0143.root, FC#7, port C2
Entries 372
Mean 44.46
Std Dev 11.78
Turn on : 27.3996
Width : 3.637
Height : 10.020
Entry
ampl
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2
4
6
8
10
12
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0
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20
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60
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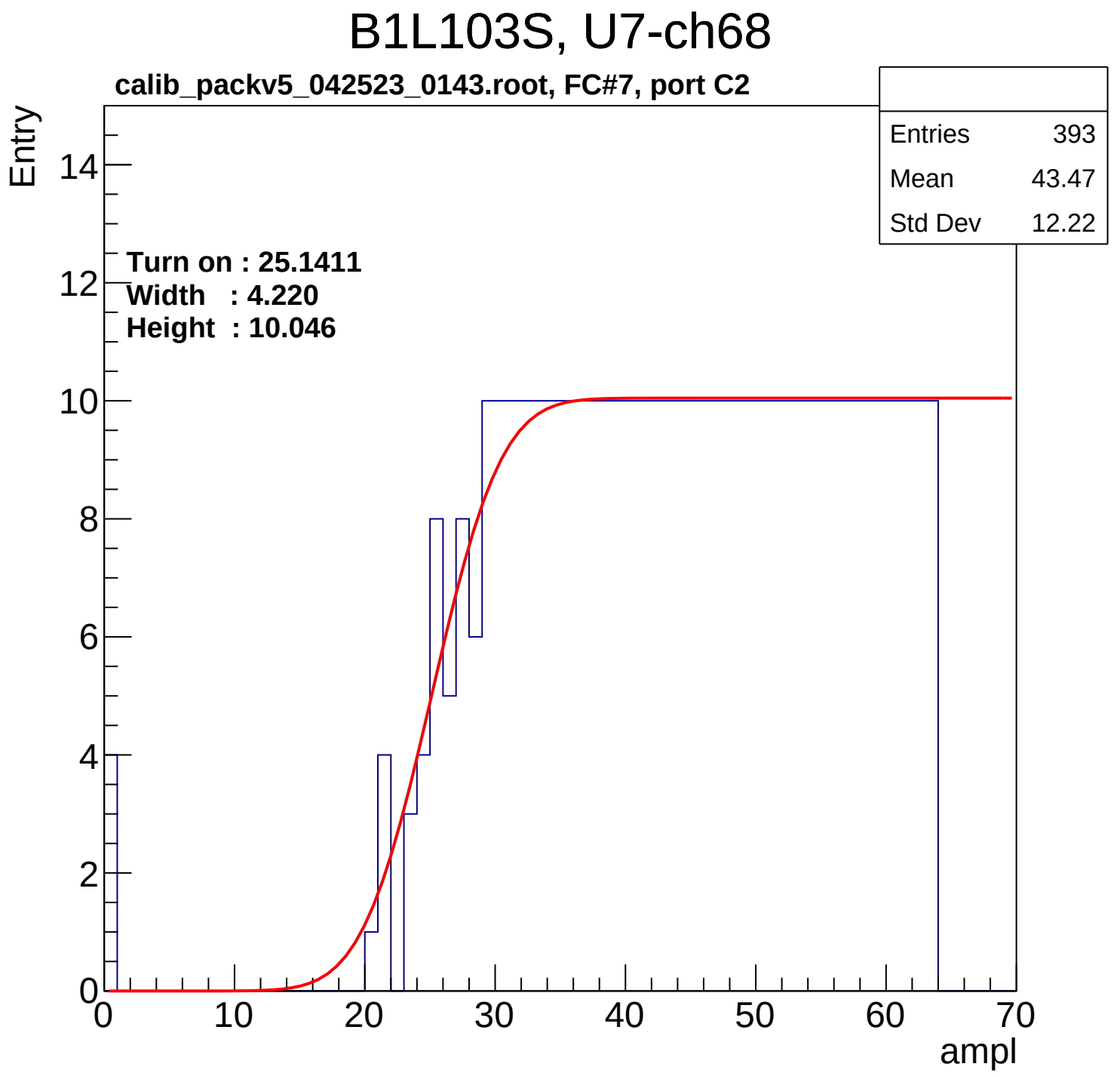
B1L103S, U7-ch68
calib_packv5_042523_0143.root, FC#7, port C2
Entries 393
Mean 43.47
Std Dev 12.22
Turn on : 25.1411
Width : 4.220
Height : 10.046
Entry
ampl
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2
4
6
8
10
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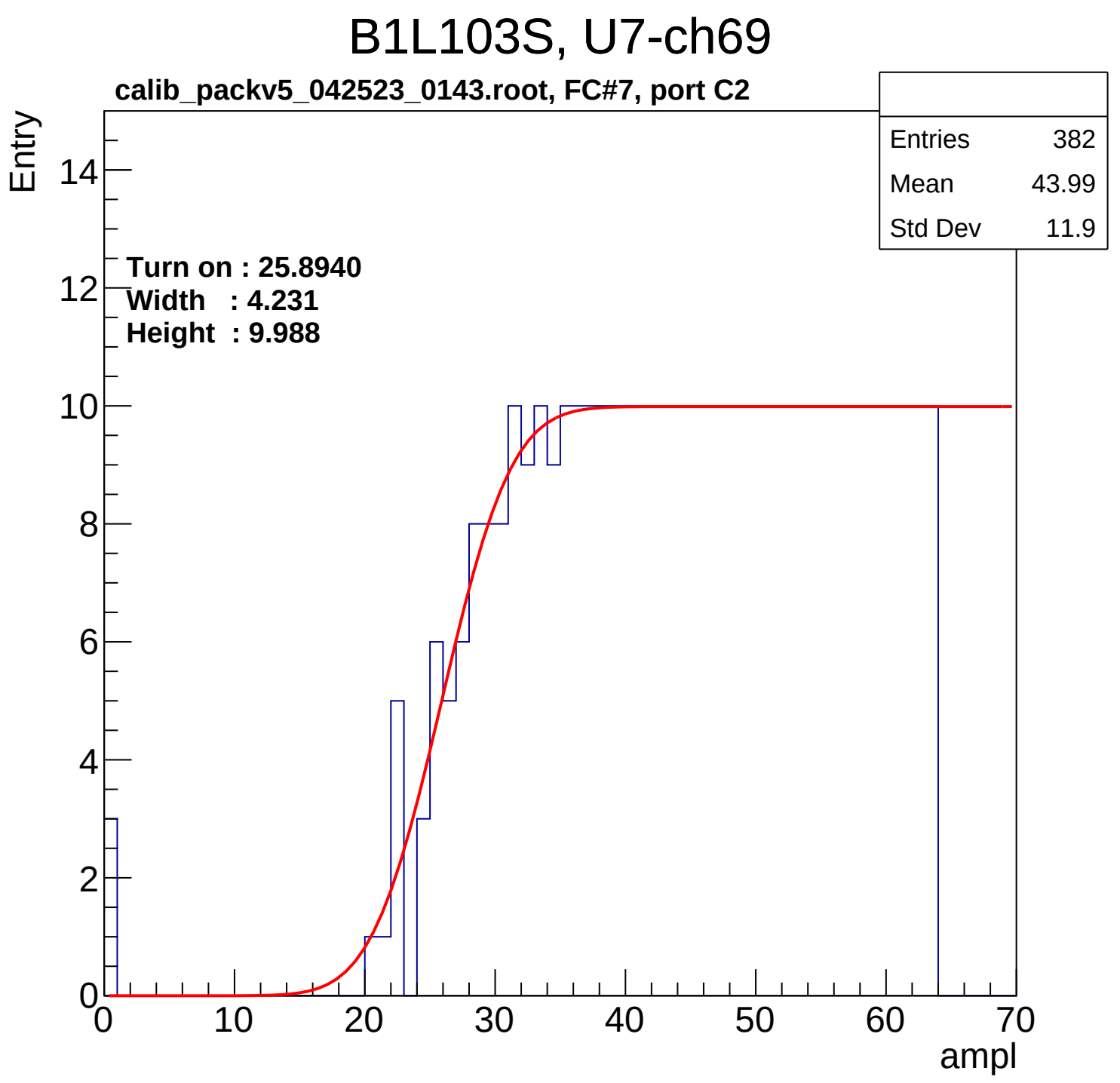
B1L103S, U7-ch69
calib_packv5_042523_0143.root, FC#7, port C2
Entries 382
Mean 43.99
Std Dev 11.9
Turn on : 25.8940
Width : 4.231
Height : 9.988
Entry
ampl
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6
8
10
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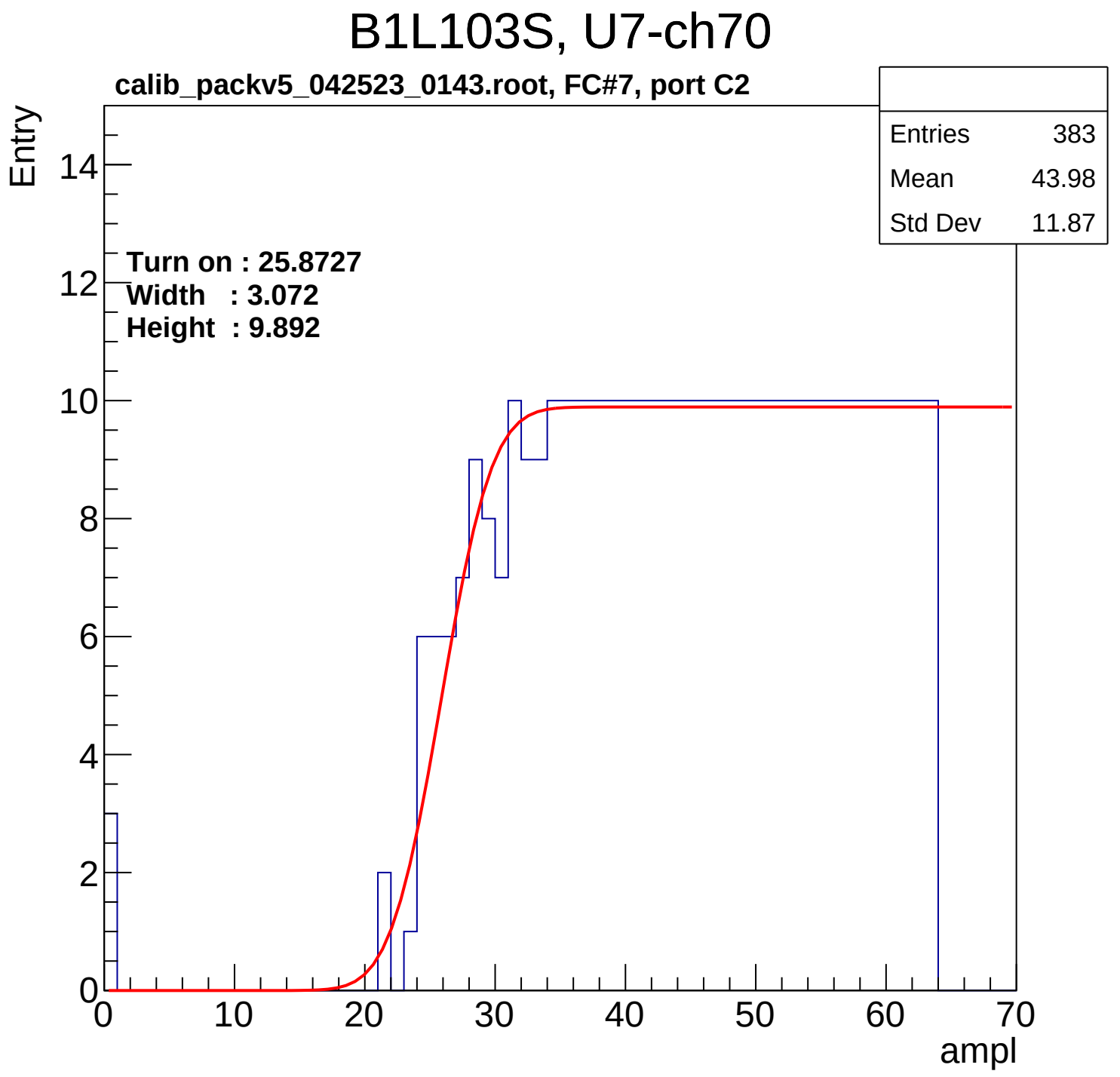
B1L103S, U7-ch70
calib_packv5_042523_0143.root, FC#7, port C2
Entries 383
Mean 43.98
Std Dev 11.87
Turn on : 25.8727
Width : 3.072
Height : 9.892
Entry
ampl
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6
8
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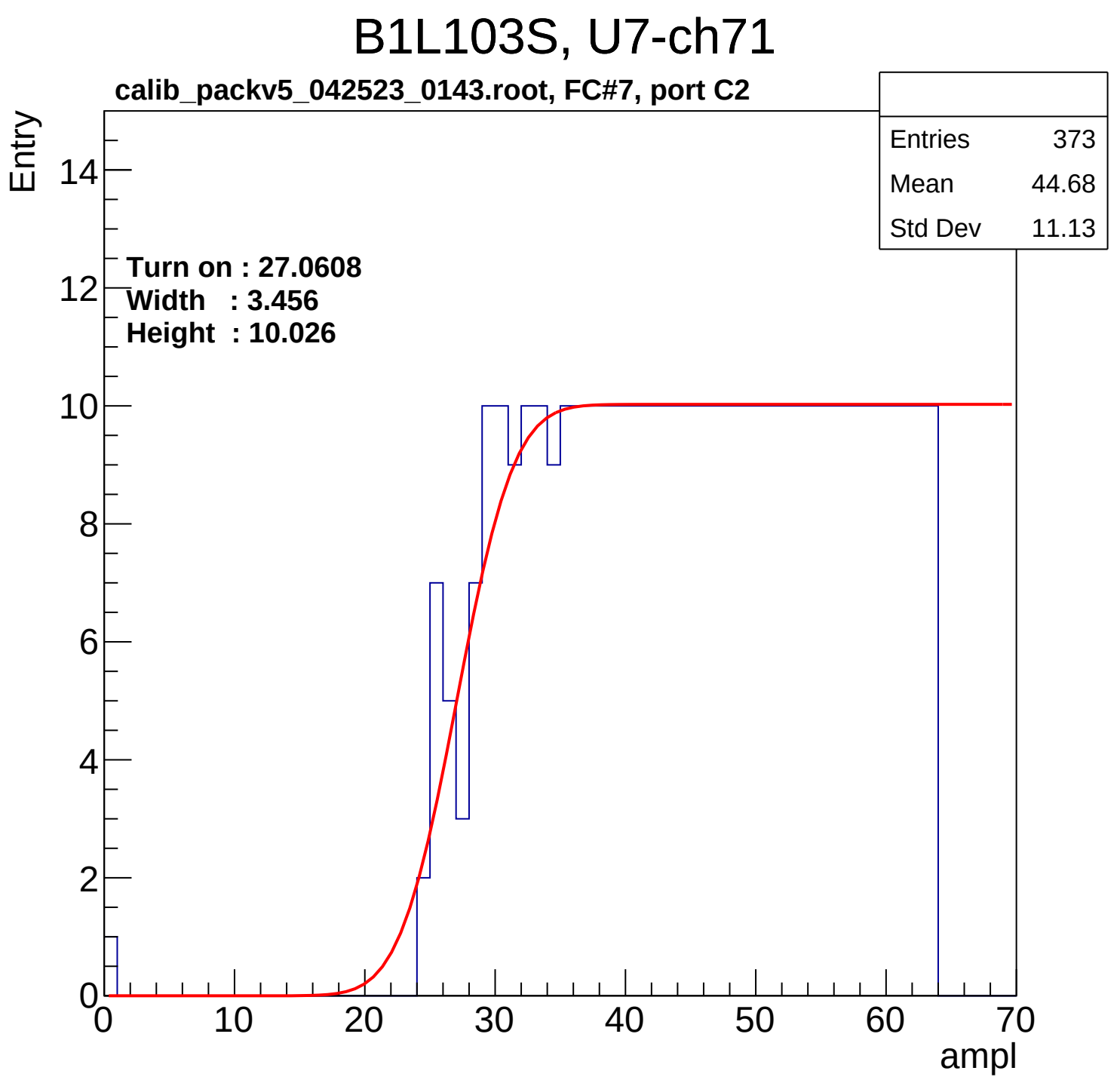
B1L103S, U7-ch71
calib_packv5_042523_0143.root, FC#7, port C2
Entries 373
Mean 44.68
Std Dev 11.13
Turn on : 27.0608
Width : 3.456
Height : 10.026
Entry
ampl
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8
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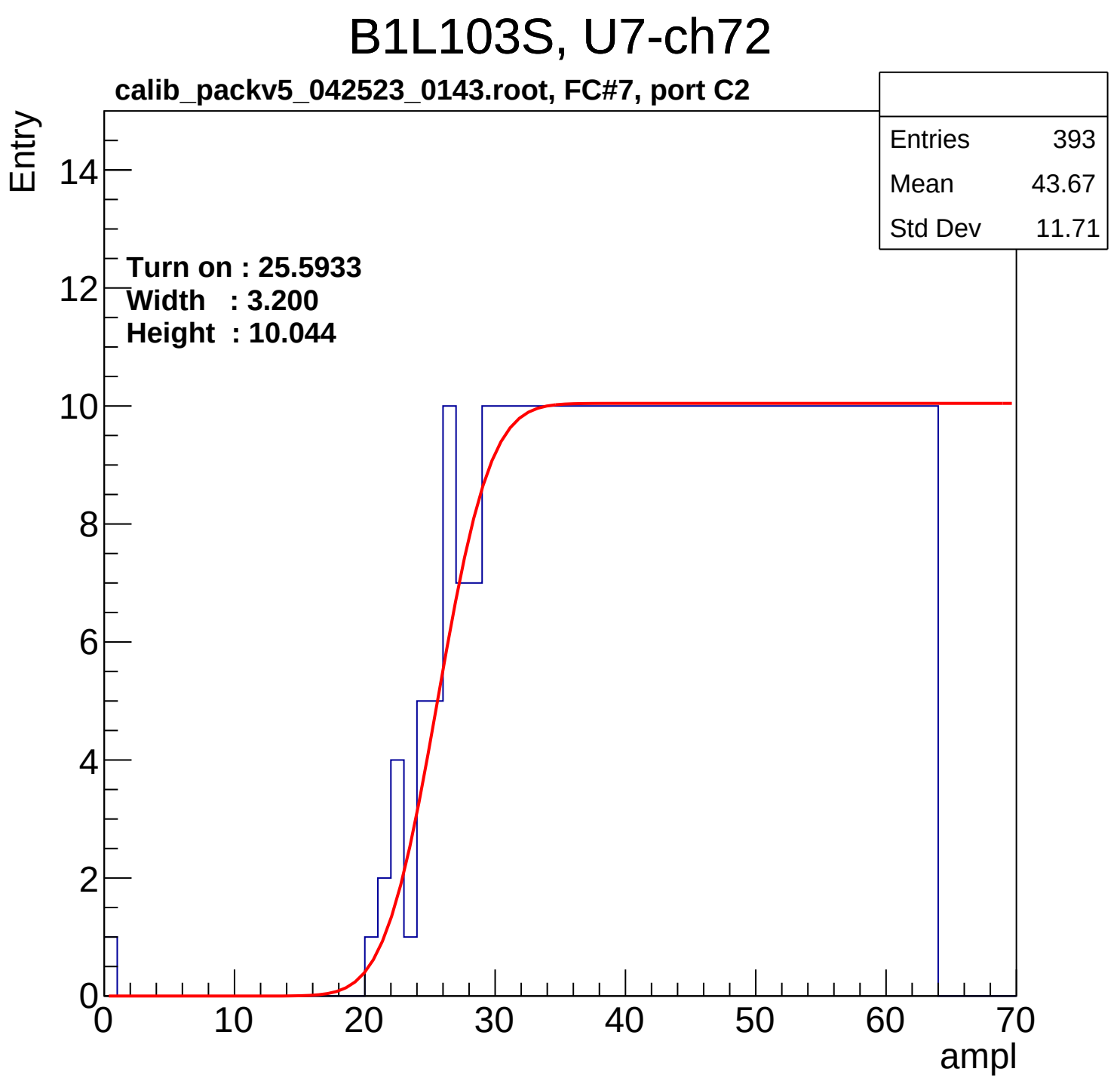
B1L103S, U7-ch72
calib_packv5_042523_0143.root, FC#7, port C2
Entries 393
Mean 43.67
Std Dev 11.71
Turn on : 25.5933
Width : 3.200
Height : 10.044
Entry
ampl
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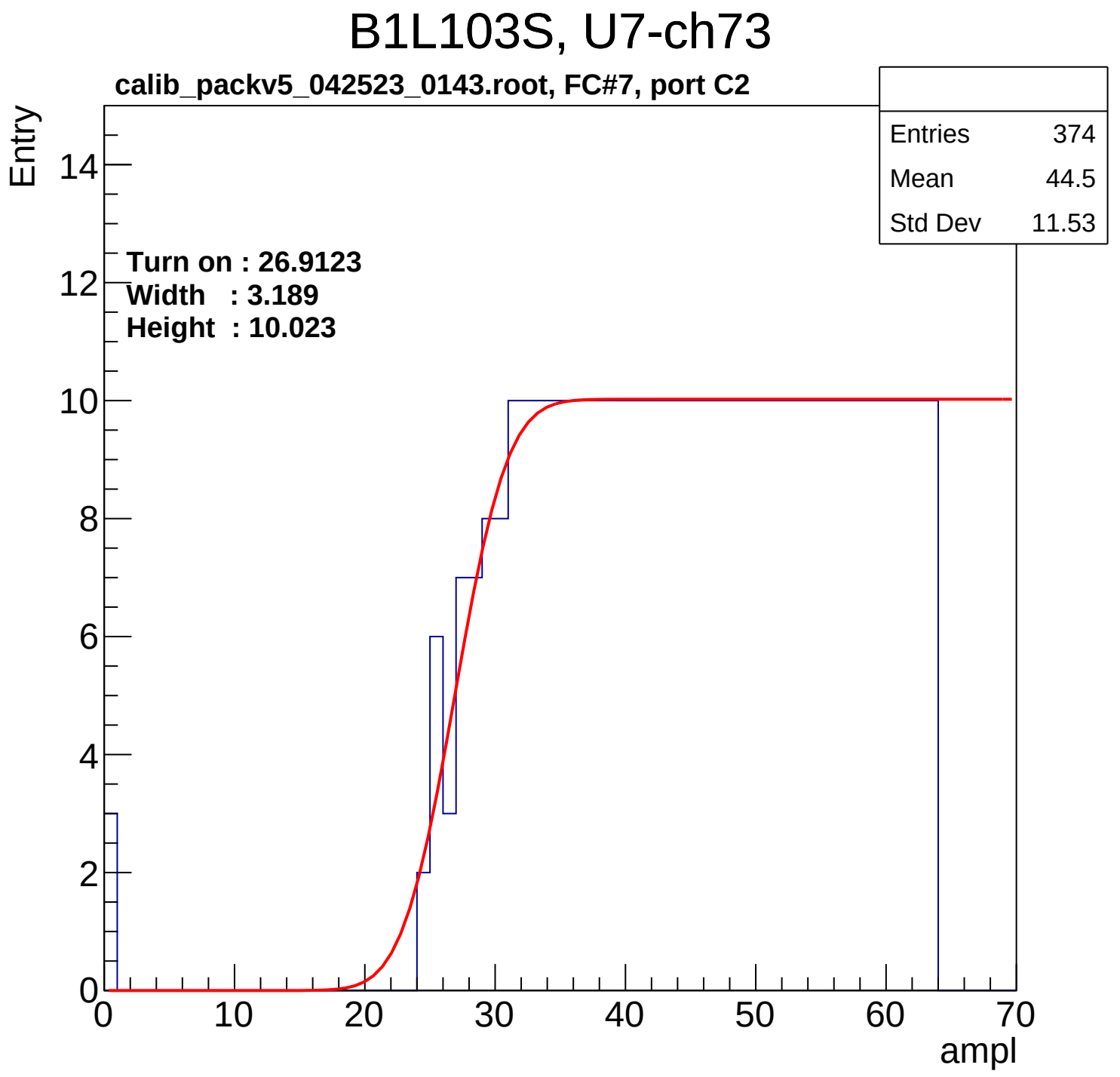
B1L103S, U7-ch73
calib_packv5_042523_0143.root, FC#7, port C2
Entries 374
Mean 44.5
Std Dev 11.53
Turn on : 26.9123
Width : 3.189
Height : 10.023
Entry
ampl
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8
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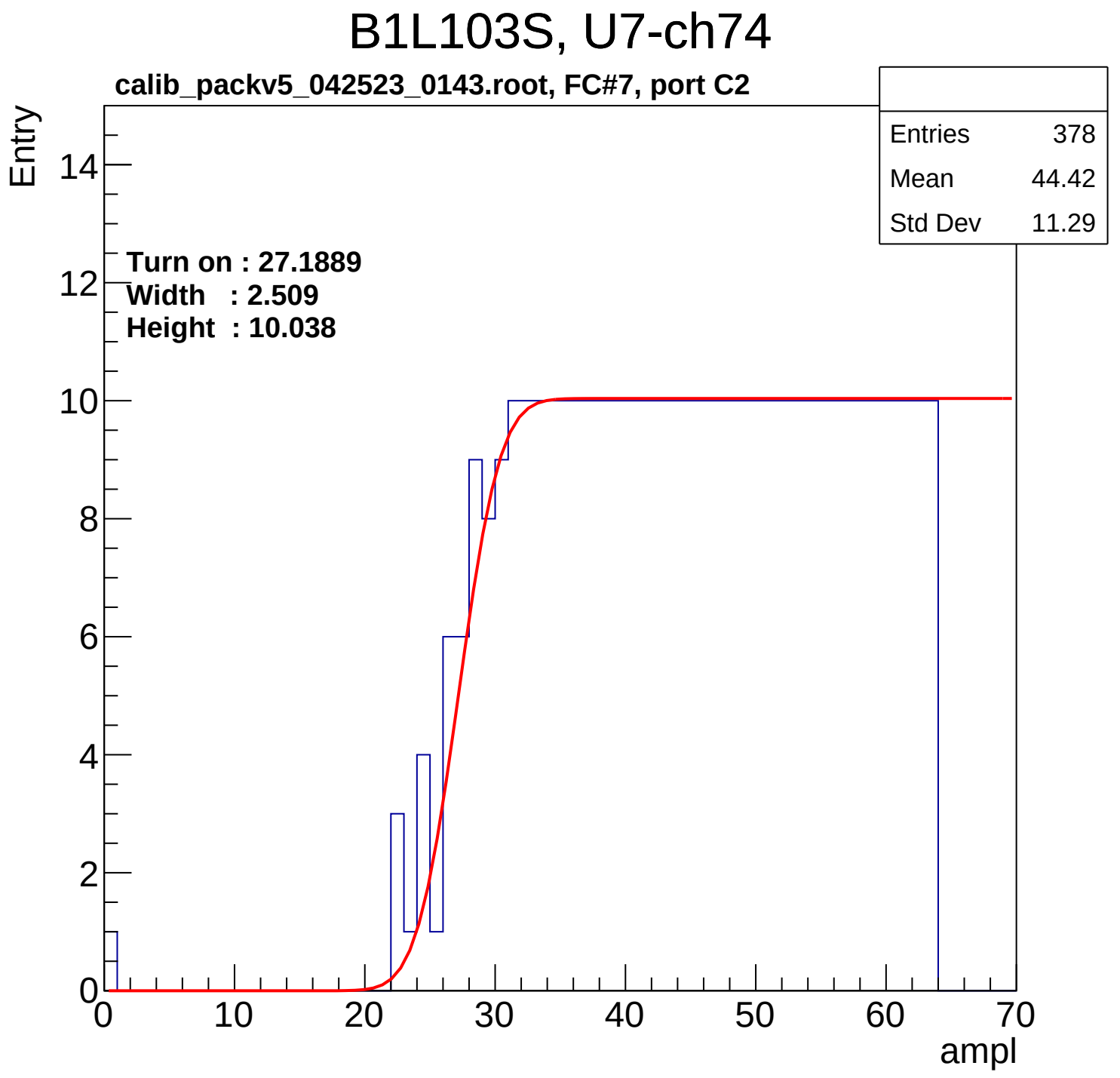
B1L103S, U7-ch74
calib_packv5_042523_0143.root, FC#7, port C2
Entries 378
Mean 44.42
Std Dev 11.29
Turn on : 27.1889
Width : 2.509
Height : 10.038
Entry
ampl
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4
6
8
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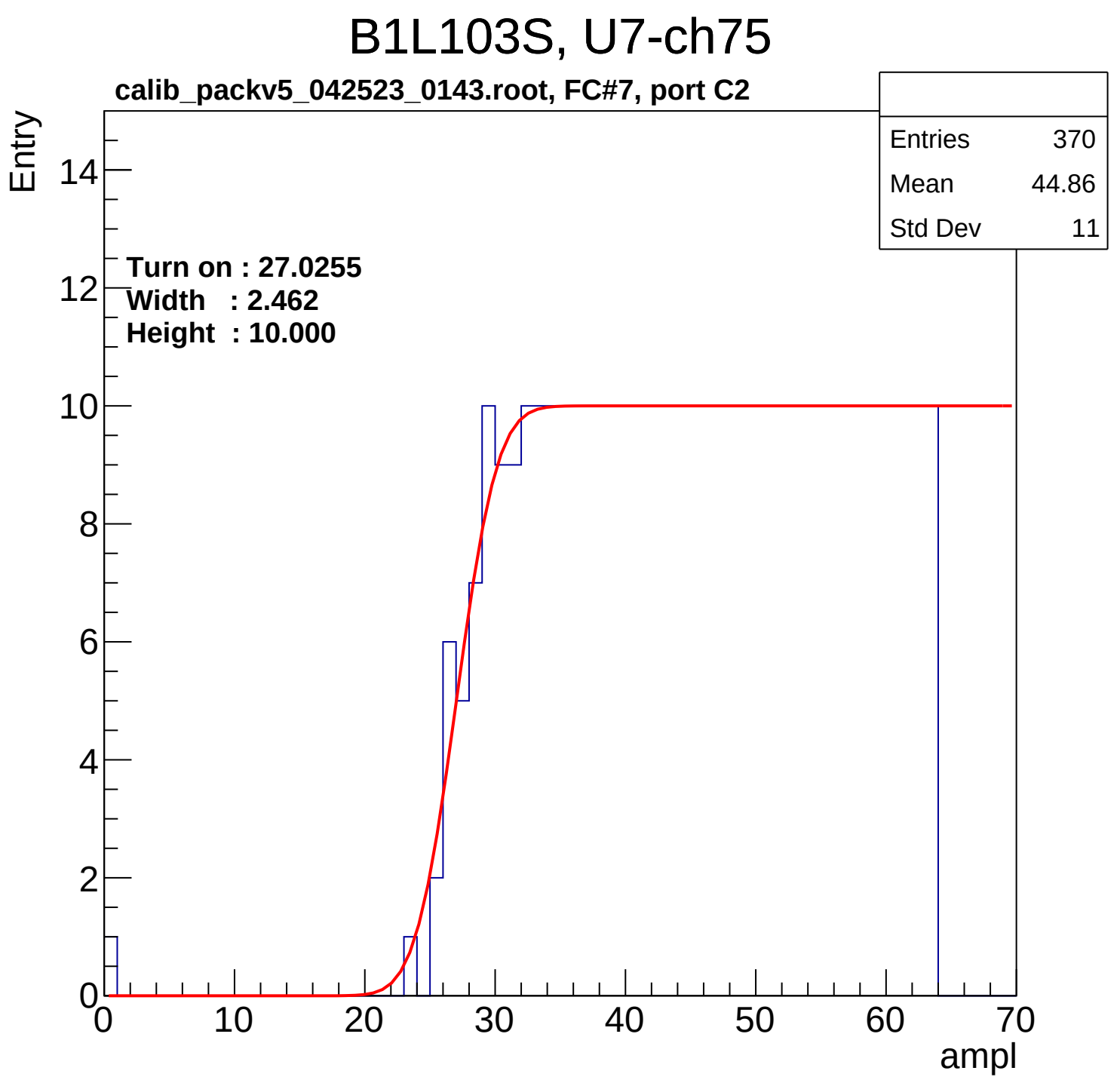
B1L103S, U7-ch75
calib_packv5_042523_0143.root, FC#7, port C2
Entries 370
Mean 44.86
Std Dev 11
Turn on : 27.0255
Width : 2.462
Height : 10.000
Entry
ampl
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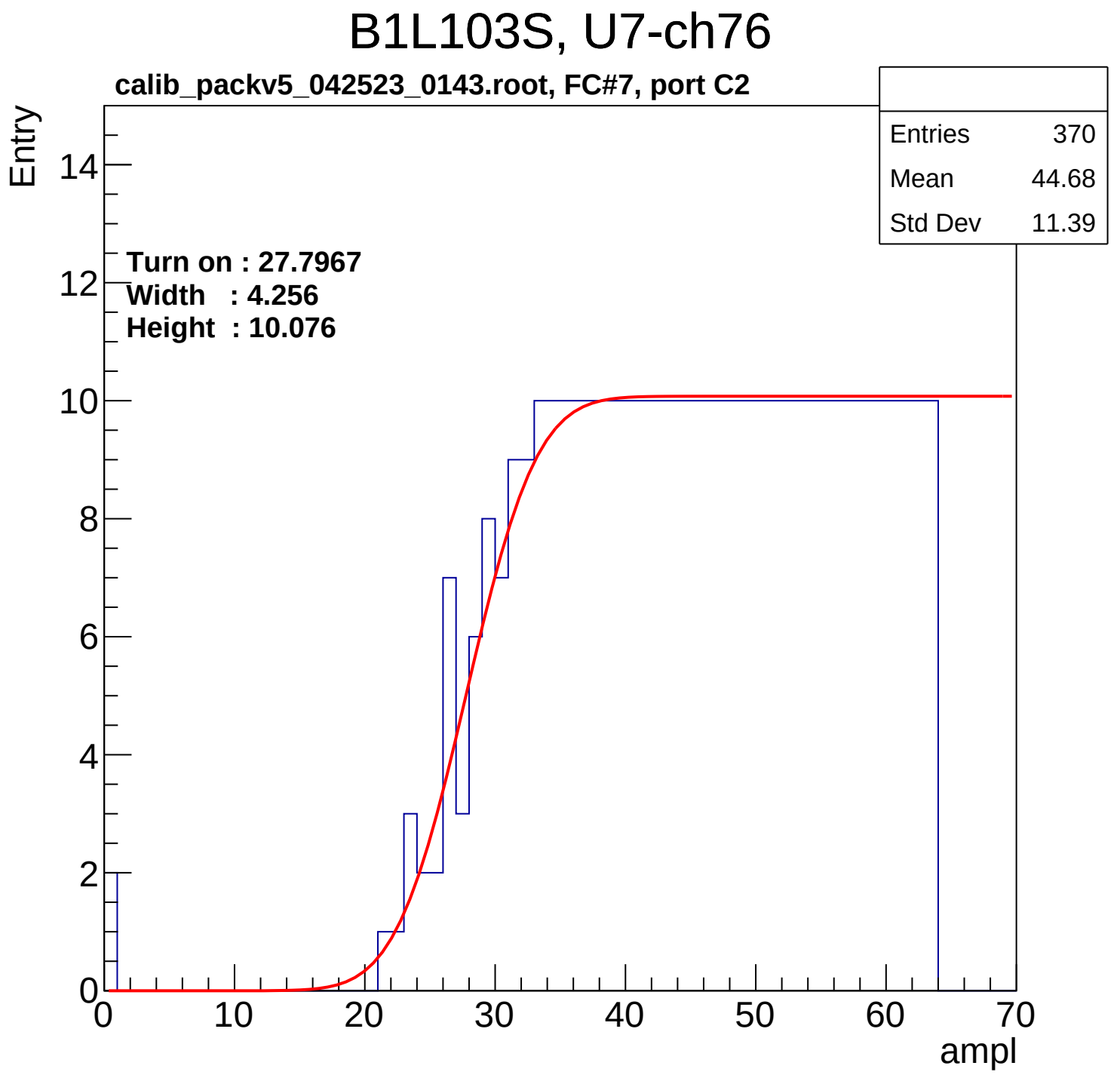
B1L103S, U7-ch76
calib_packv5_042523_0143.root, FC#7, port C2
Entries 370
Mean 44.68
Std Dev 11.39
Turn on : 27.7967
Width : 4.256
Height : 10.076
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ampl
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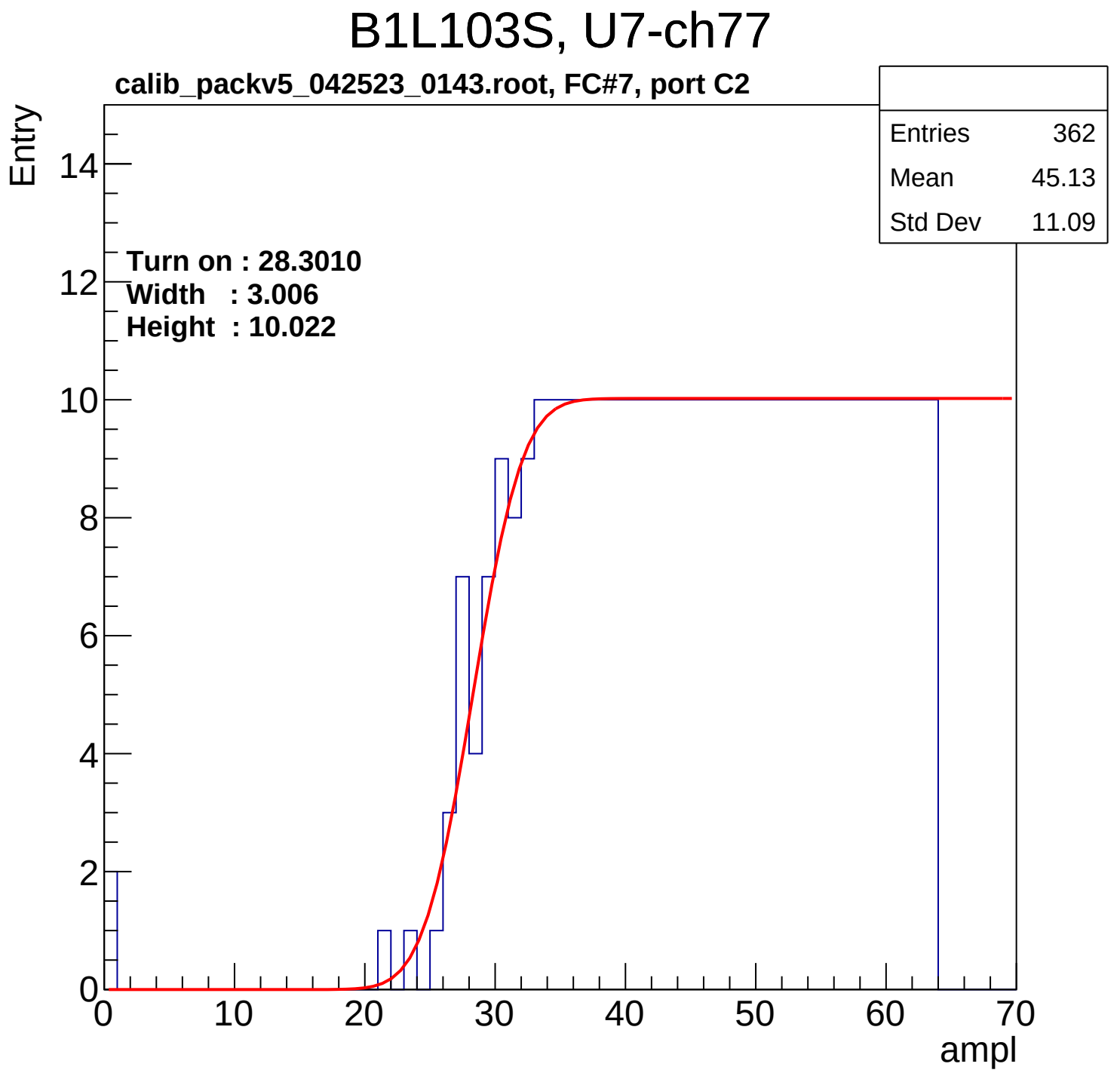
B1L103S, U7-ch77
calib_packv5_042523_0143.root, FC#7, port C2
Entries 362
Mean 45.13
Std Dev 11.09
Turn on : 28.3010
Width : 3.006
Height : 10.022
Entry
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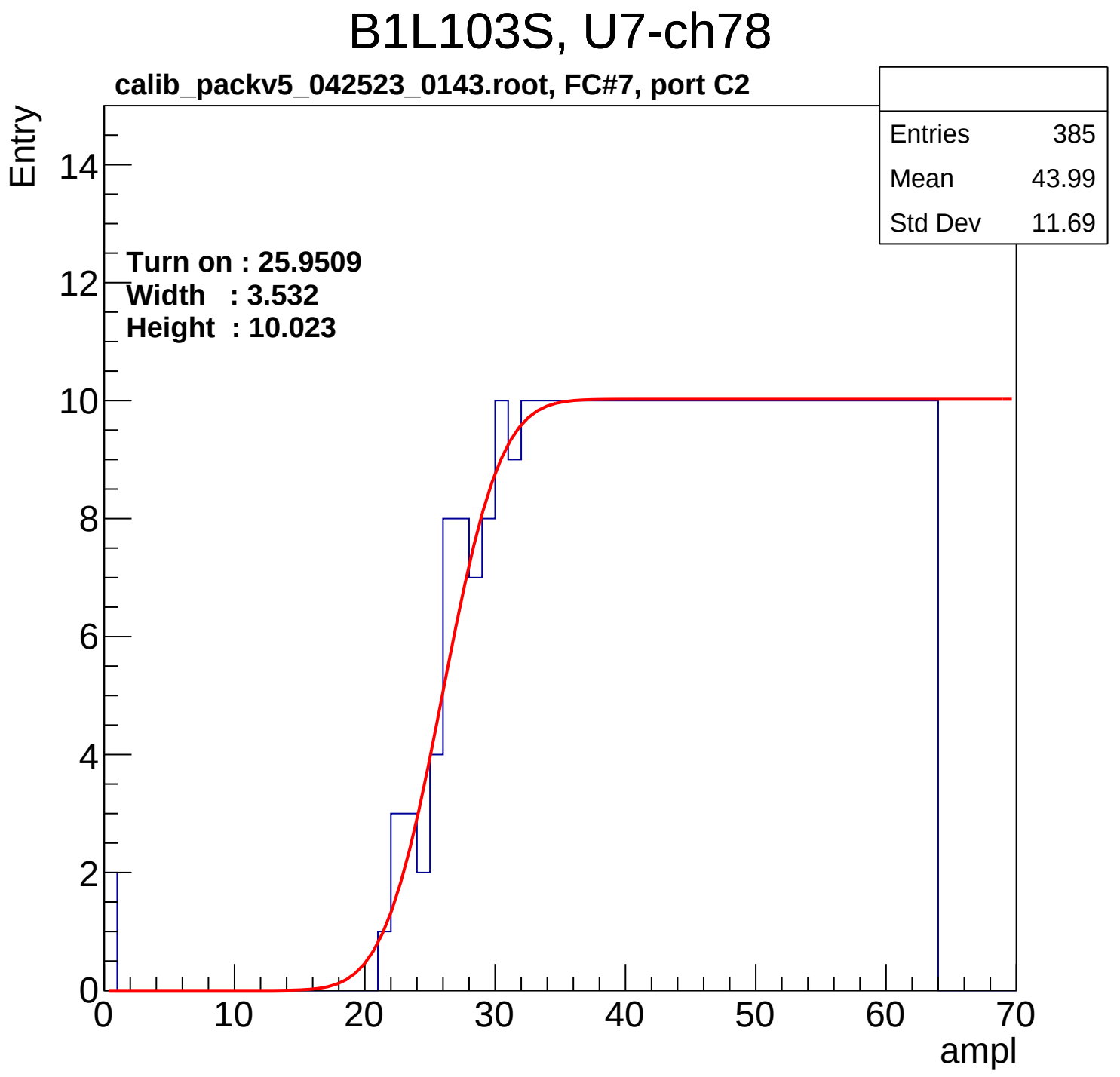
B1L103S, U7-ch78
calib_packv5_042523_0143.root, FC#7, port C2
Entries 385
Mean 43.99
Std Dev 11.69
Turn on : 25.9509
Width : 3.532
Height : 10.023
Entry
ampl
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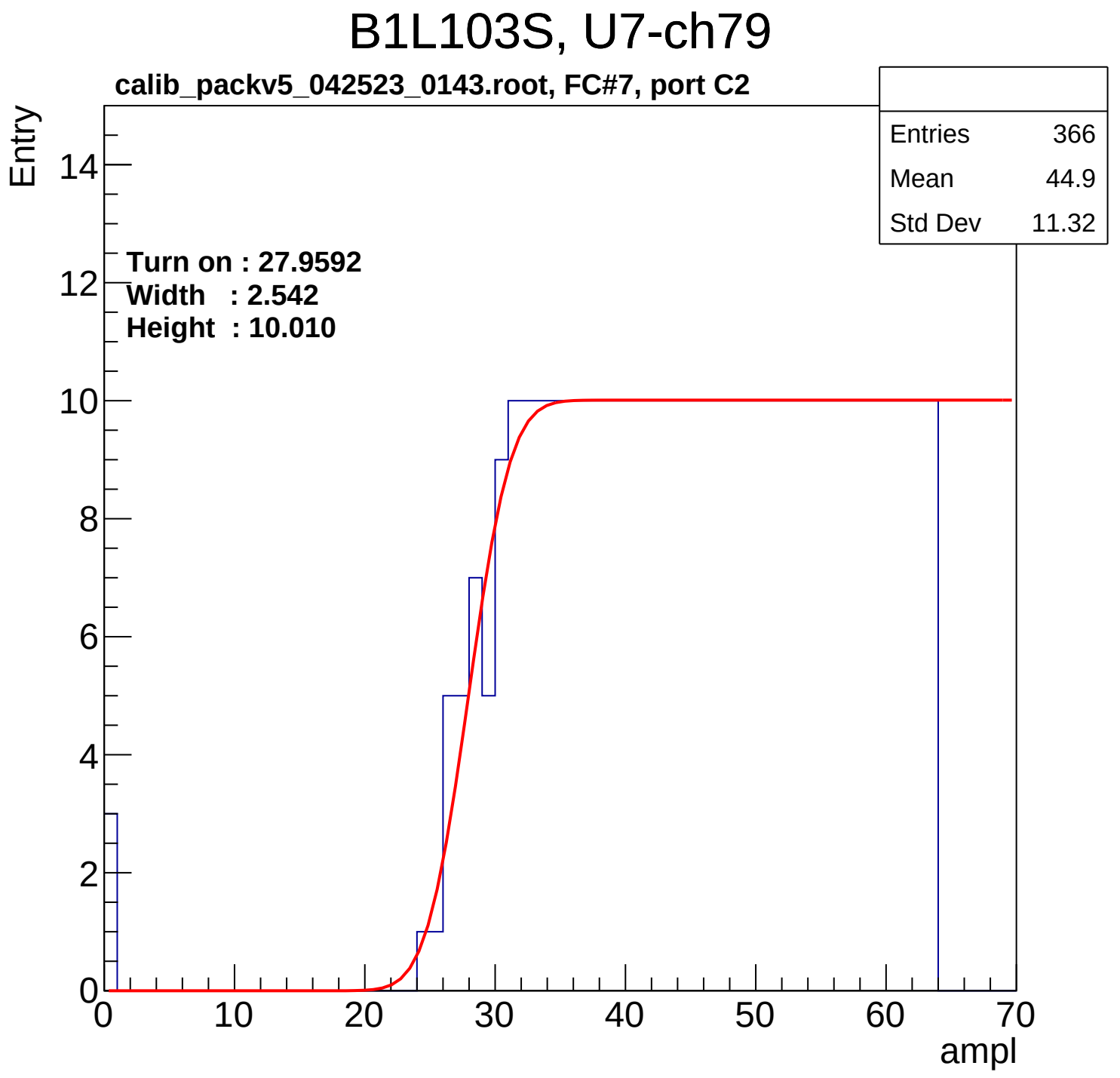
B1L103S, U7-ch79
calib_packv5_042523_0143.root, FC#7, port C2
Entries 366
Mean 44.9
Std Dev 11.32
Turn on : 27.9592
Width : 2.542
Height : 10.010
Entry
ampl
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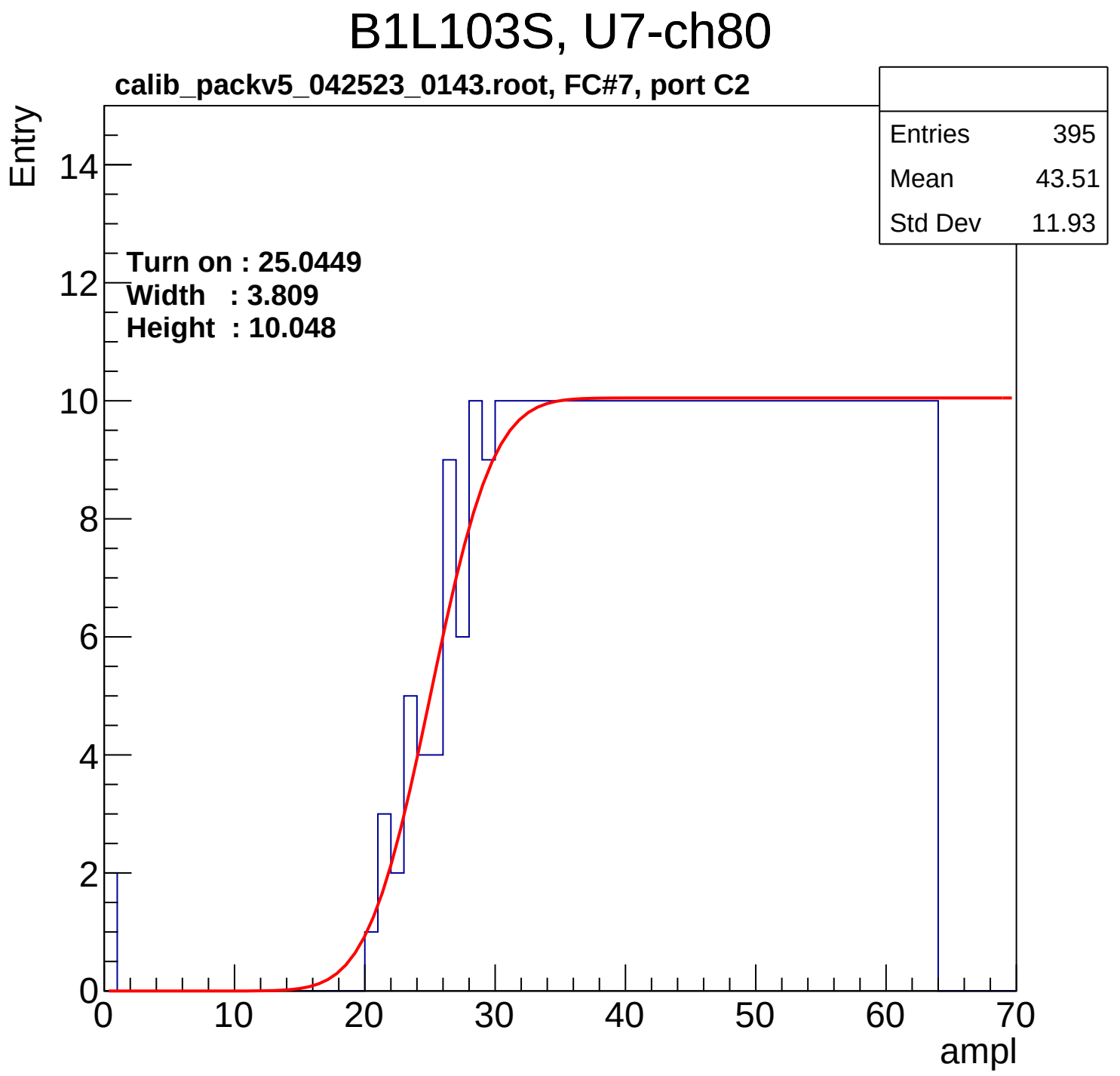
B1L103S, U7-ch80
calib_packv5_042523_0143.root, FC#7, port C2
Entries 395
Mean 43.51
Std Dev 11.93
Turn on : 25.0449
Width : 3.809
Height : 10.048
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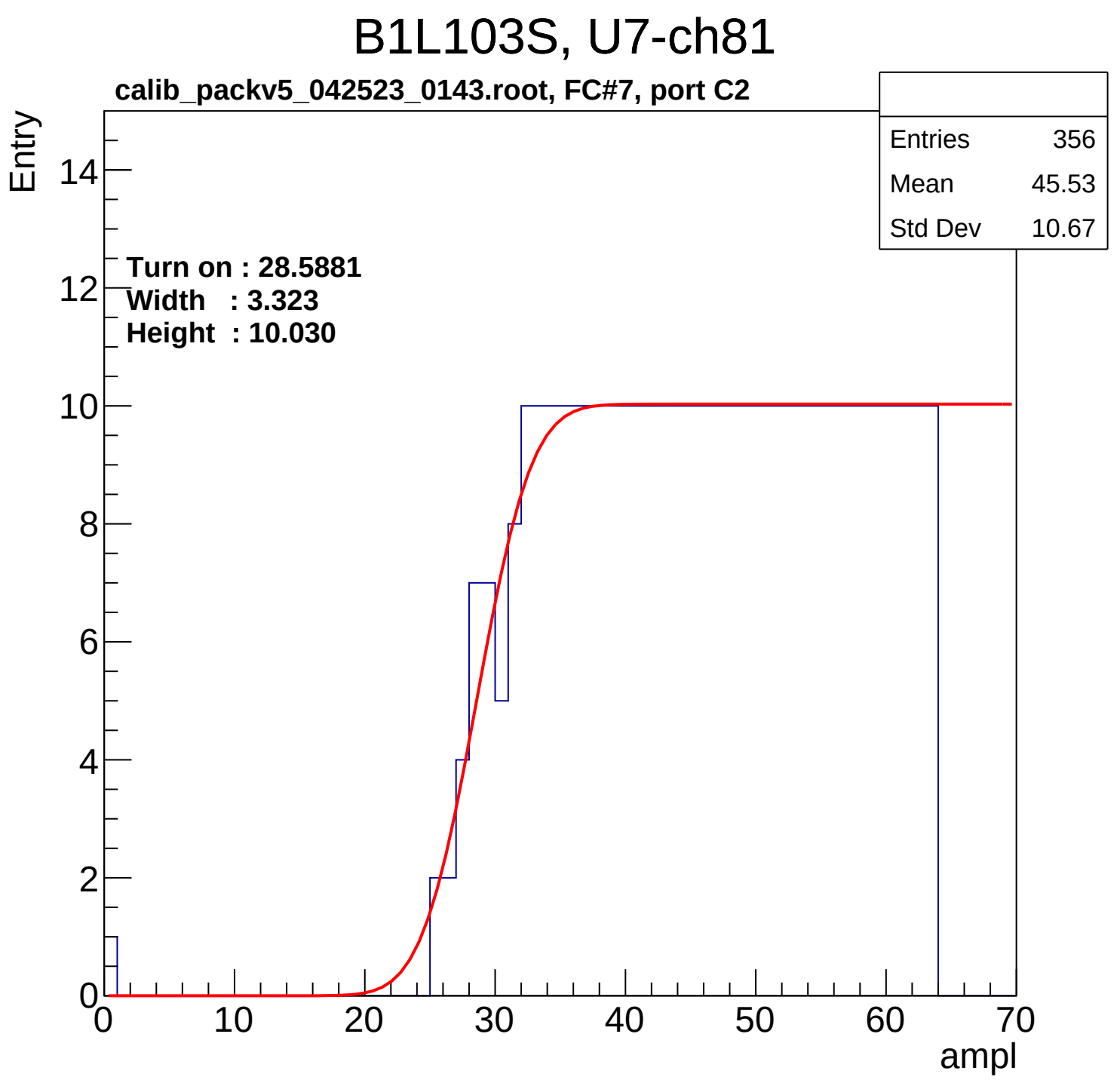
B1L103S, U7-ch81
calib_packv5_042523_0143.root, FC#7, port C2
Entries 356
Mean 45.53
Std Dev 10.67
Turn on : 28.5881
Width : 3.323
Height : 10.030
Entry
ampl
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0
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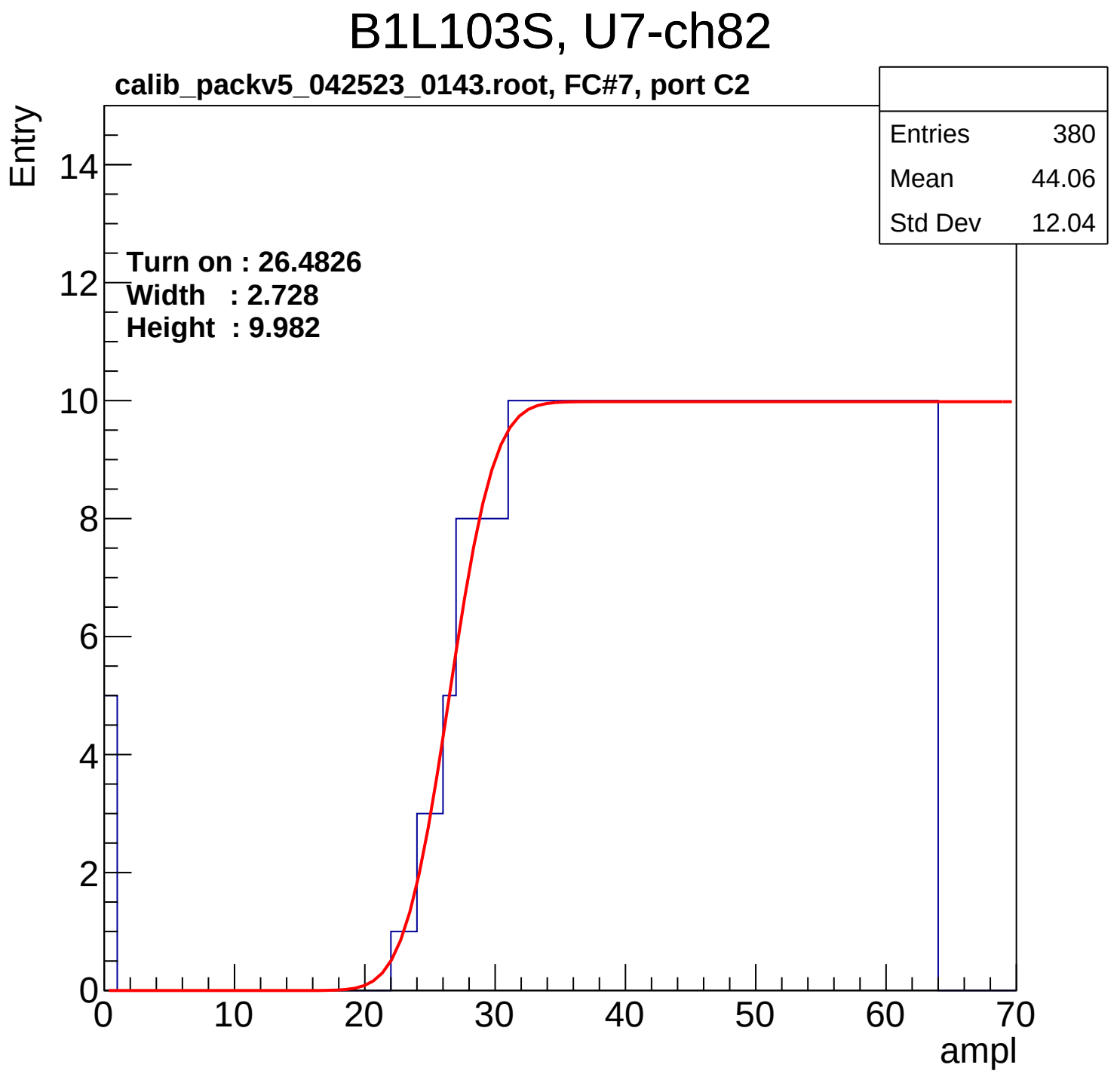
B1L103S, U7-ch82
calib_packv5_042523_0143.root, FC#7, port C2
Entries 380
Mean 44.06
Std Dev 12.04
Turn on : 26.4826
Width : 2.728
Height : 9.982
Entry
ampl
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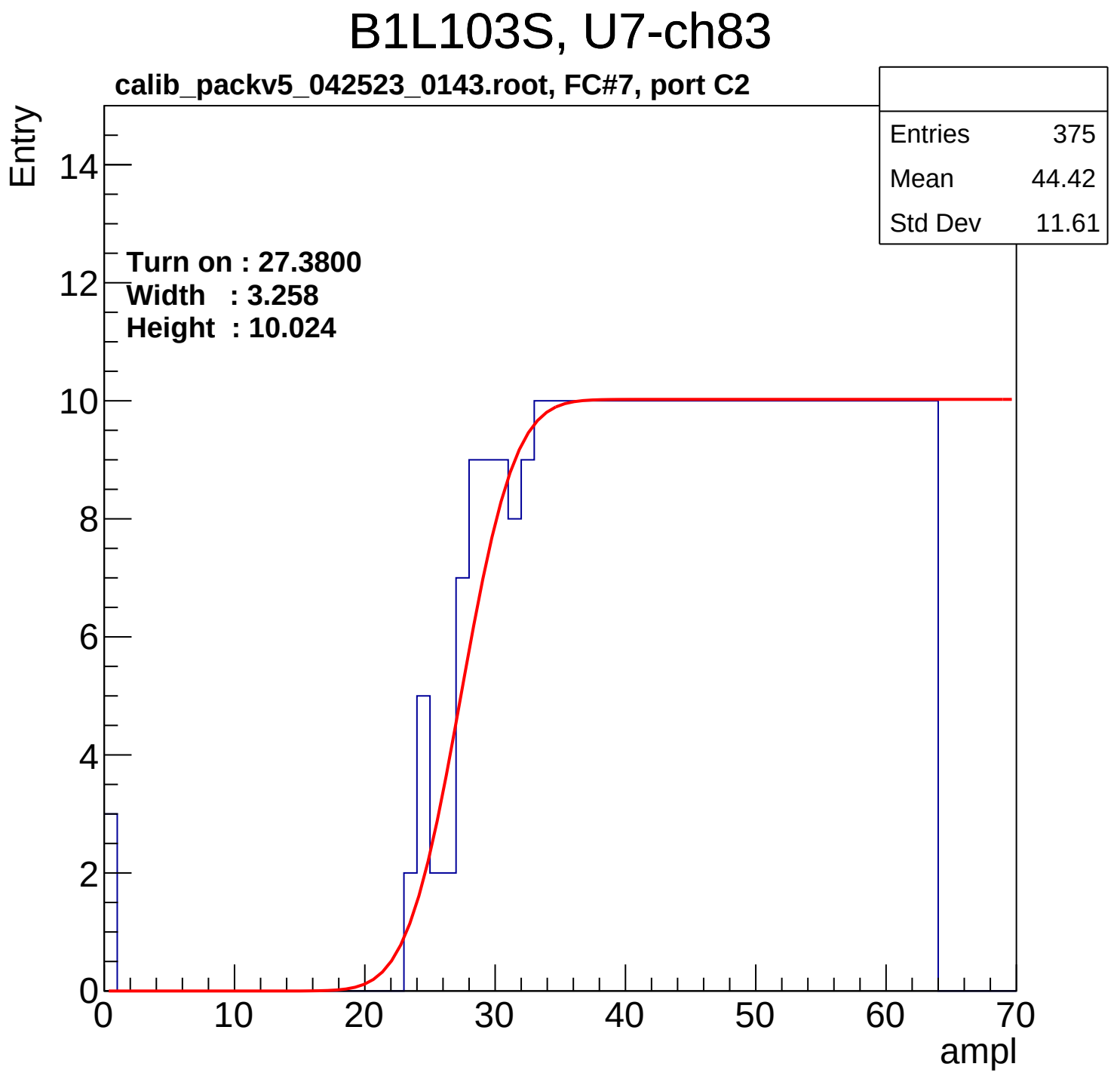
B1L103S, U7-ch83
calib_packv5_042523_0143.root, FC#7, port C2
Entries 375
Mean 44.42
Std Dev 11.61
Turn on : 27.3800
Width : 3.258
Height : 10.024
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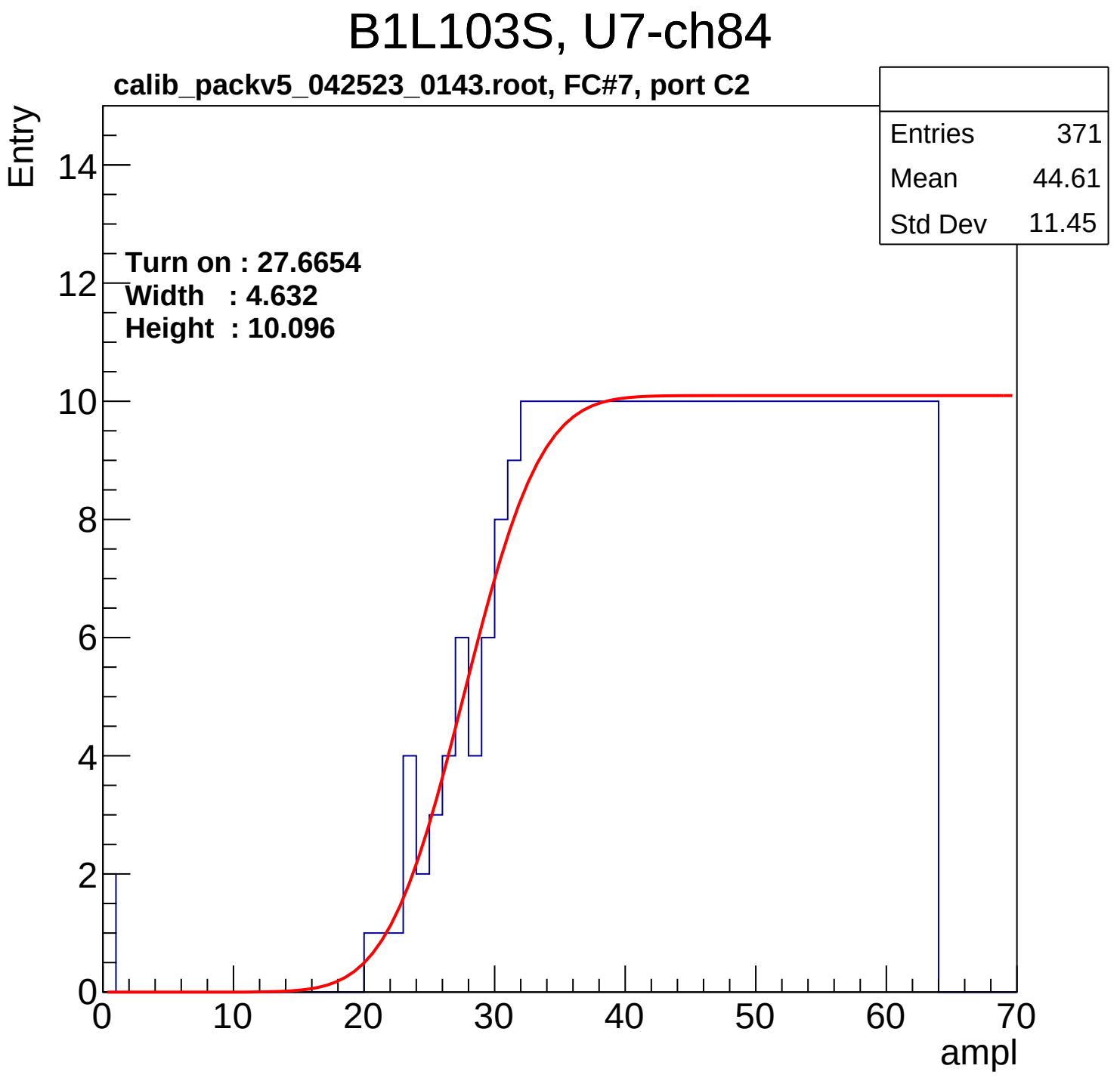
B1L103S, U7-ch84
calib_packv5_042523_0143.root, FC#7, port C2
Entries 371
Mean 44.61
Std Dev 11.45
Turn on : 27.6654
Width : 4.632
Height : 10.096
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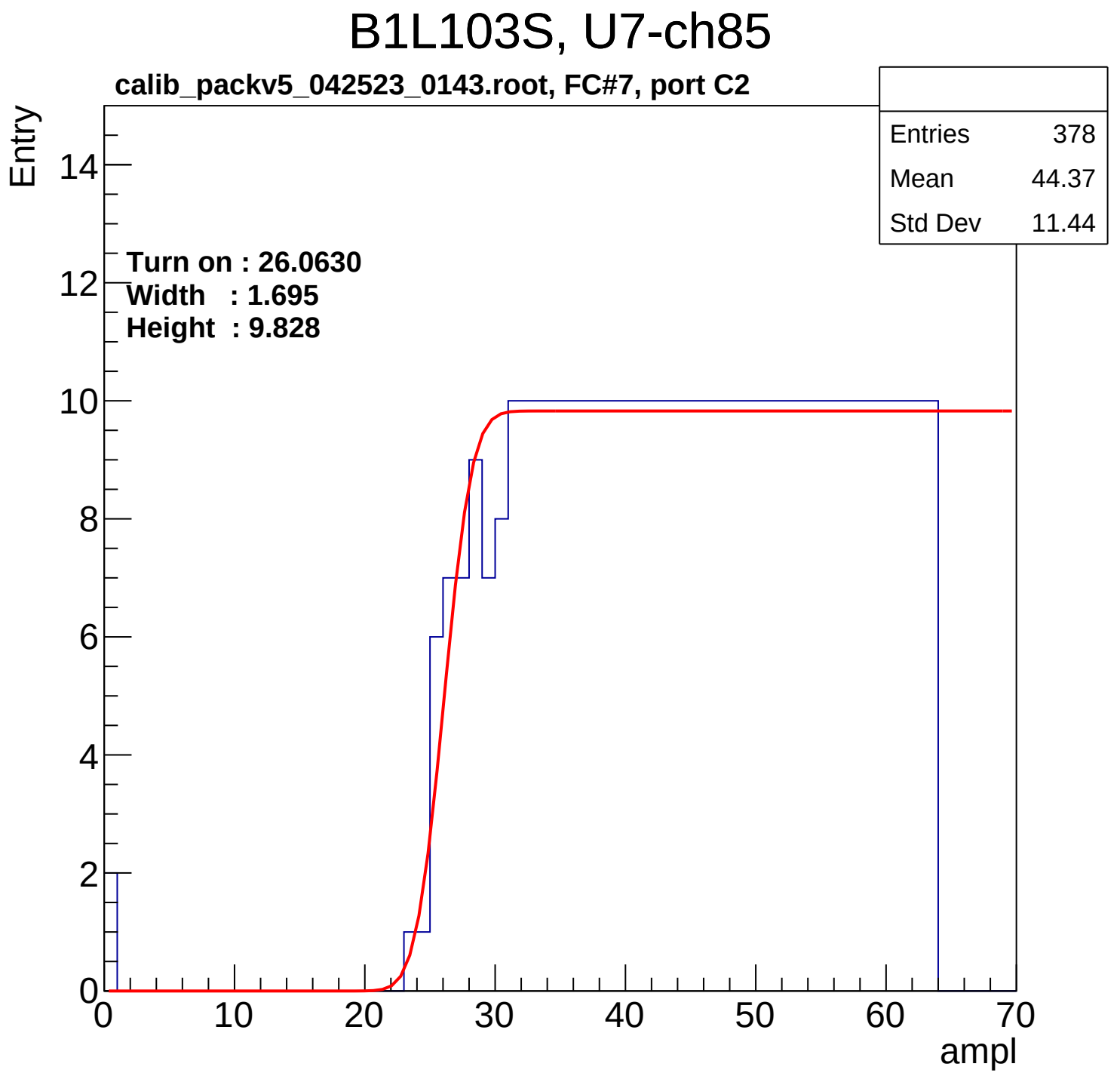
B1L103S, U7-ch85
calib_packv5_042523_0143.root, FC#7, port C2
Entries 378
Mean 44.37
Std Dev 11.44
Turn on : 26.0630
Width : 1.695
Height : 9.828
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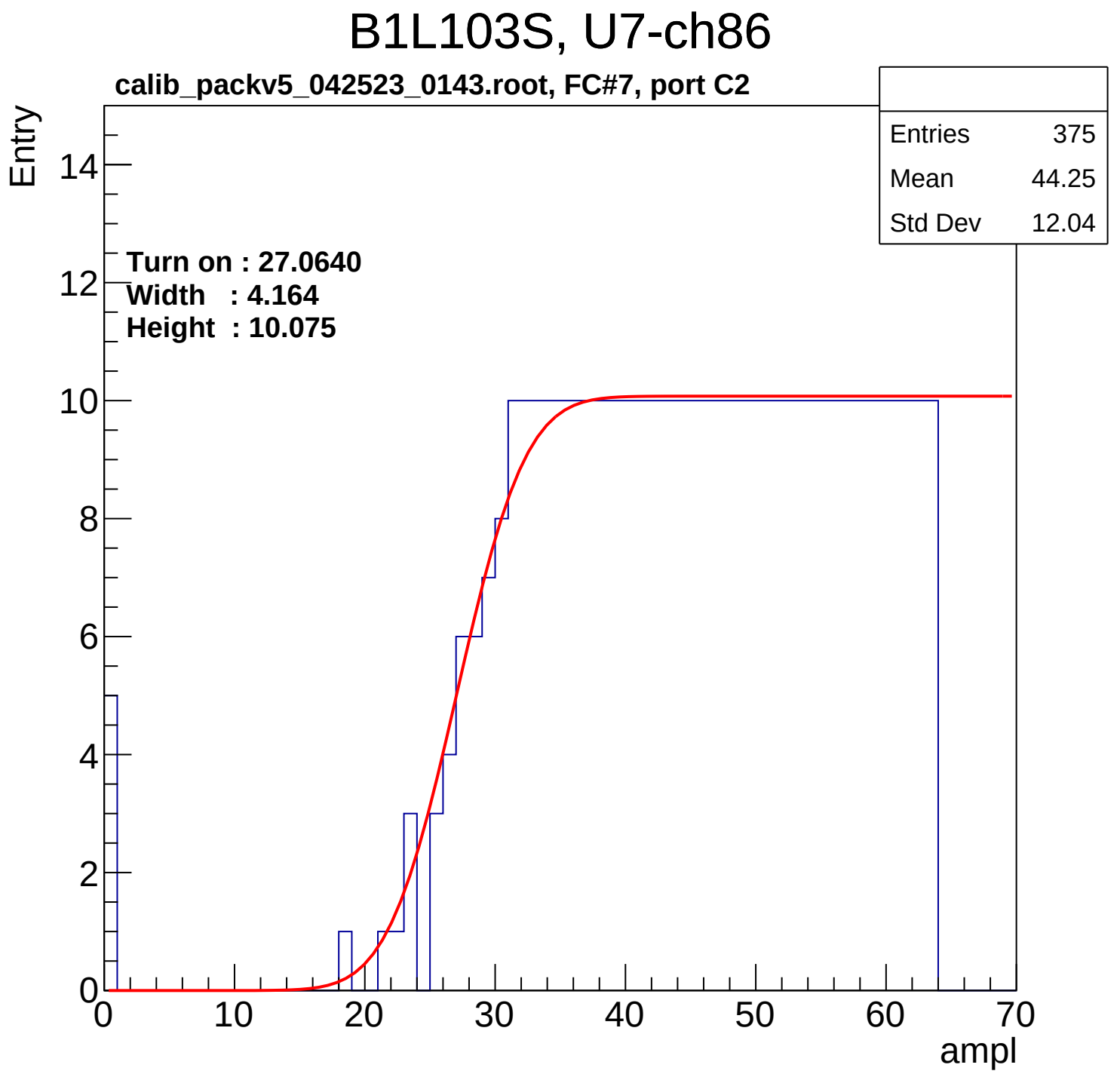
B1L103S, U7-ch86
calib_packv5_042523_0143.root, FC#7, port C2
Entries 375
Mean 44.25
Std Dev 12.04
Turn on : 27.0640
Width : 4.164
Height : 10.075
Entry
ampl
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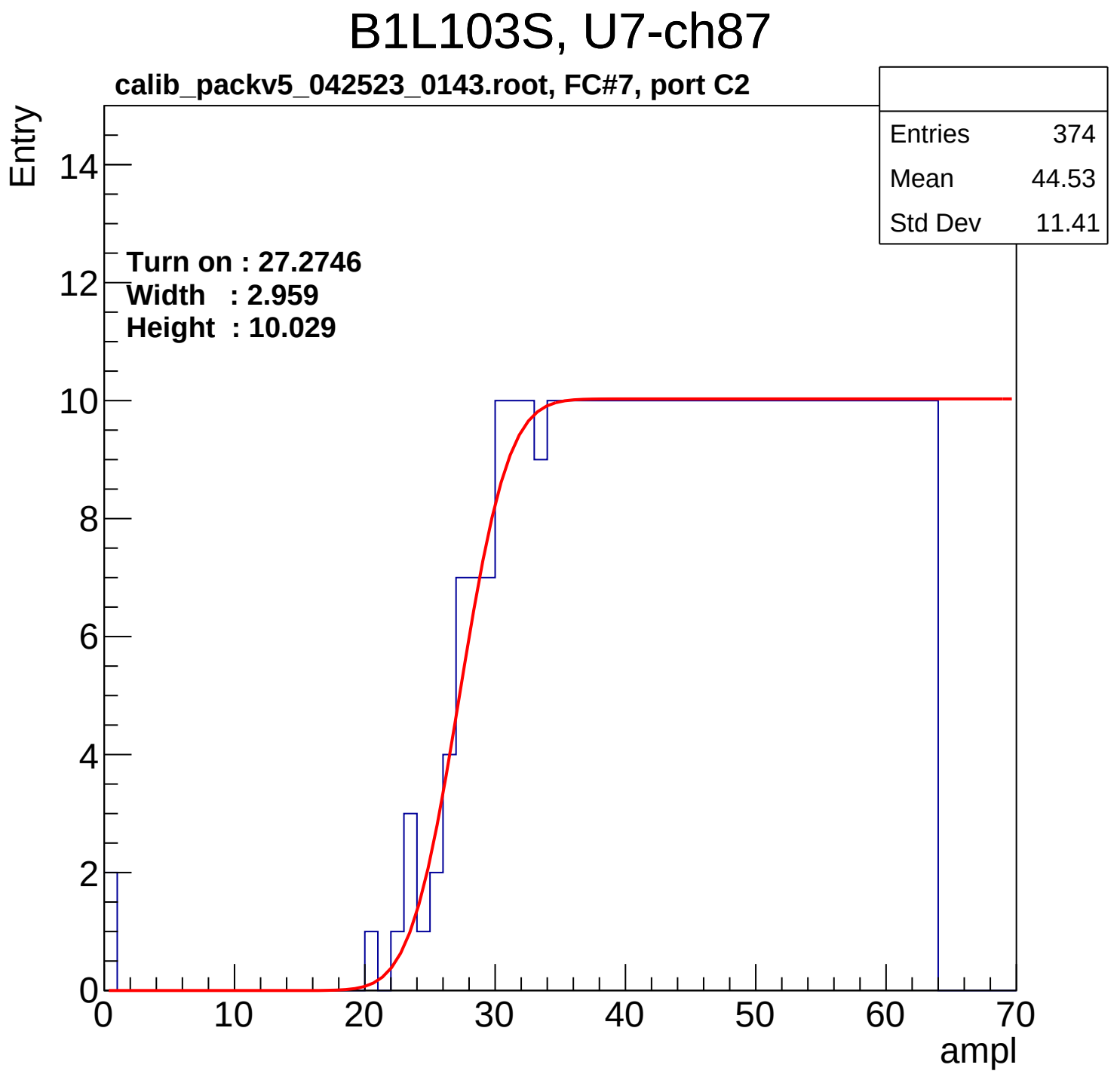
B1L103S, U7-ch87
calib_packv5_042523_0143.root, FC#7, port C2
Entries 374
Mean 44.53
Std Dev 11.41
Turn on : 27.2746
Width : 2.959
Height : 10.029
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ampl
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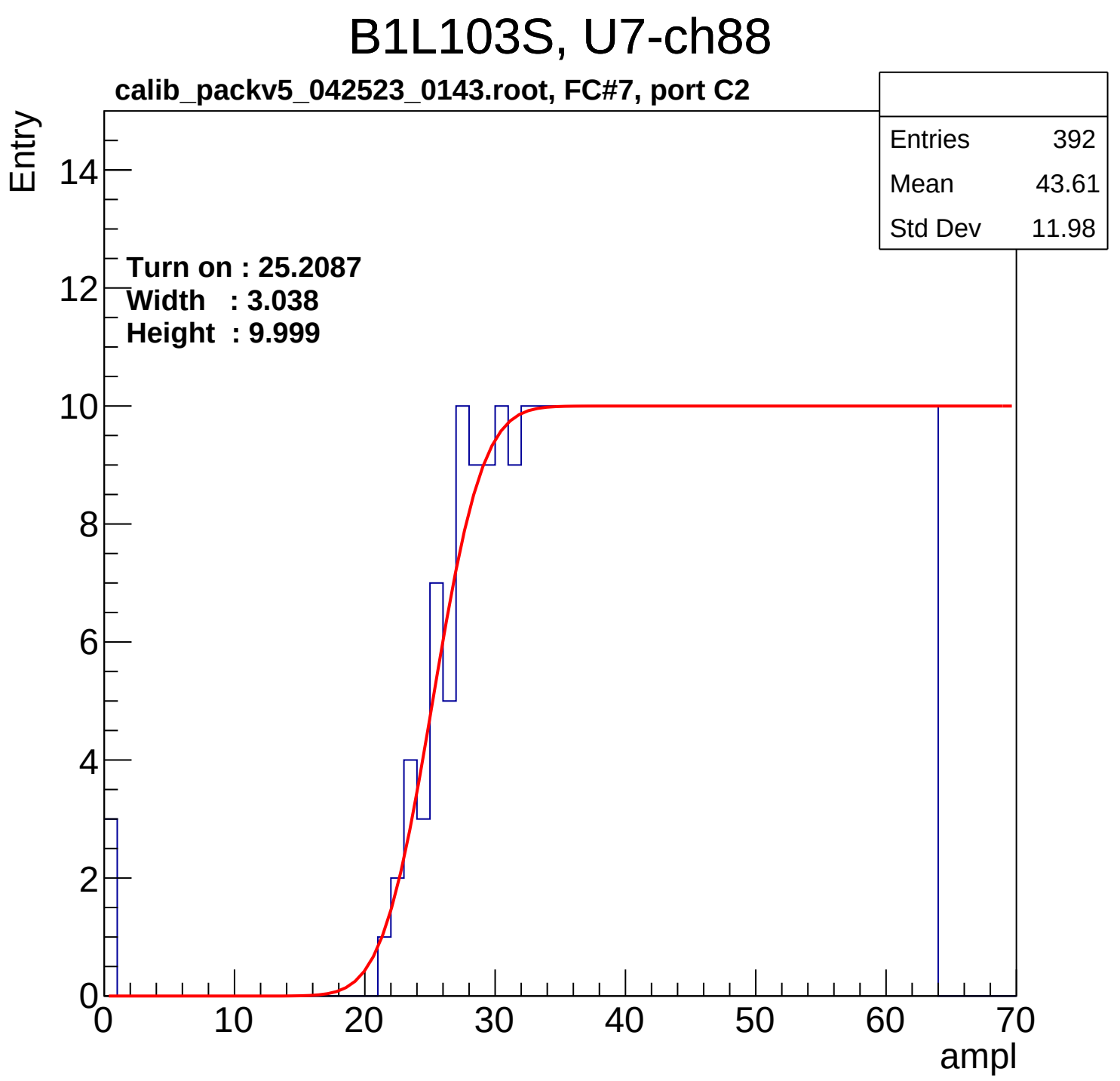
B1L103S, U7-ch88
calib_packv5_042523_0143.root, FC#7, port C2
Entries 392
Mean 43.61
Std Dev 11.98
Turn on : 25.2087
Width : 3.038
Height : 9.999
Entry
ampl
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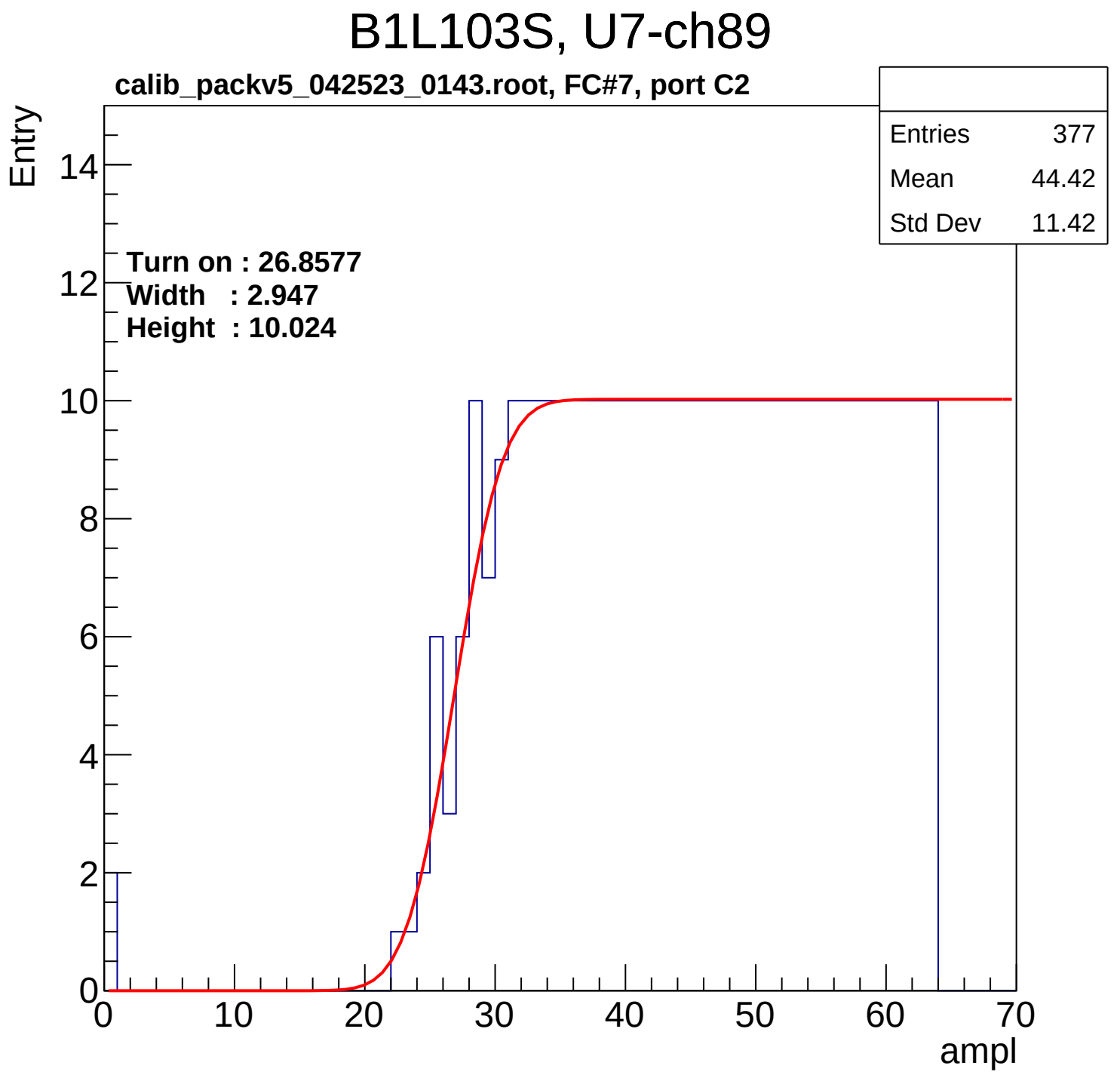
B1L103S, U7-ch89
calib_packv5_042523_0143.root, FC#7, port C2
Entries 377
Mean 44.42
Std Dev 11.42
Turn on : 26.8577
Width : 2.947
Height : 10.024
Entry
ampl
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2
4
6
8
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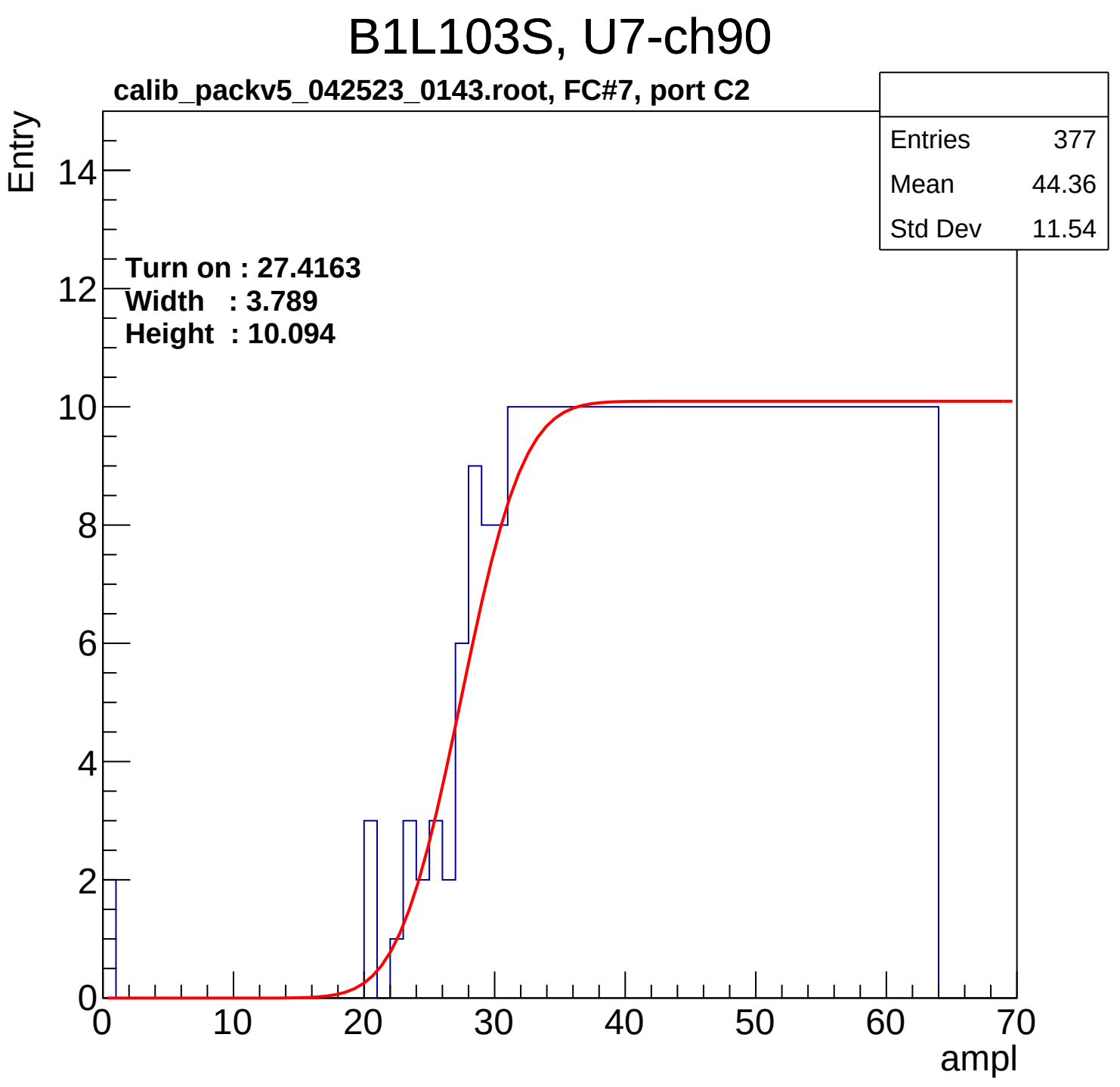
B1L103S, U7-ch90
calib_packv5_042523_0143.root, FC#7, port C2
Entries 377
Mean 44.36
Std Dev 11.54
Turn on : 27.4163
Width : 3.789
Height : 10.094
Entry
ampl
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2
4
6
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12
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0
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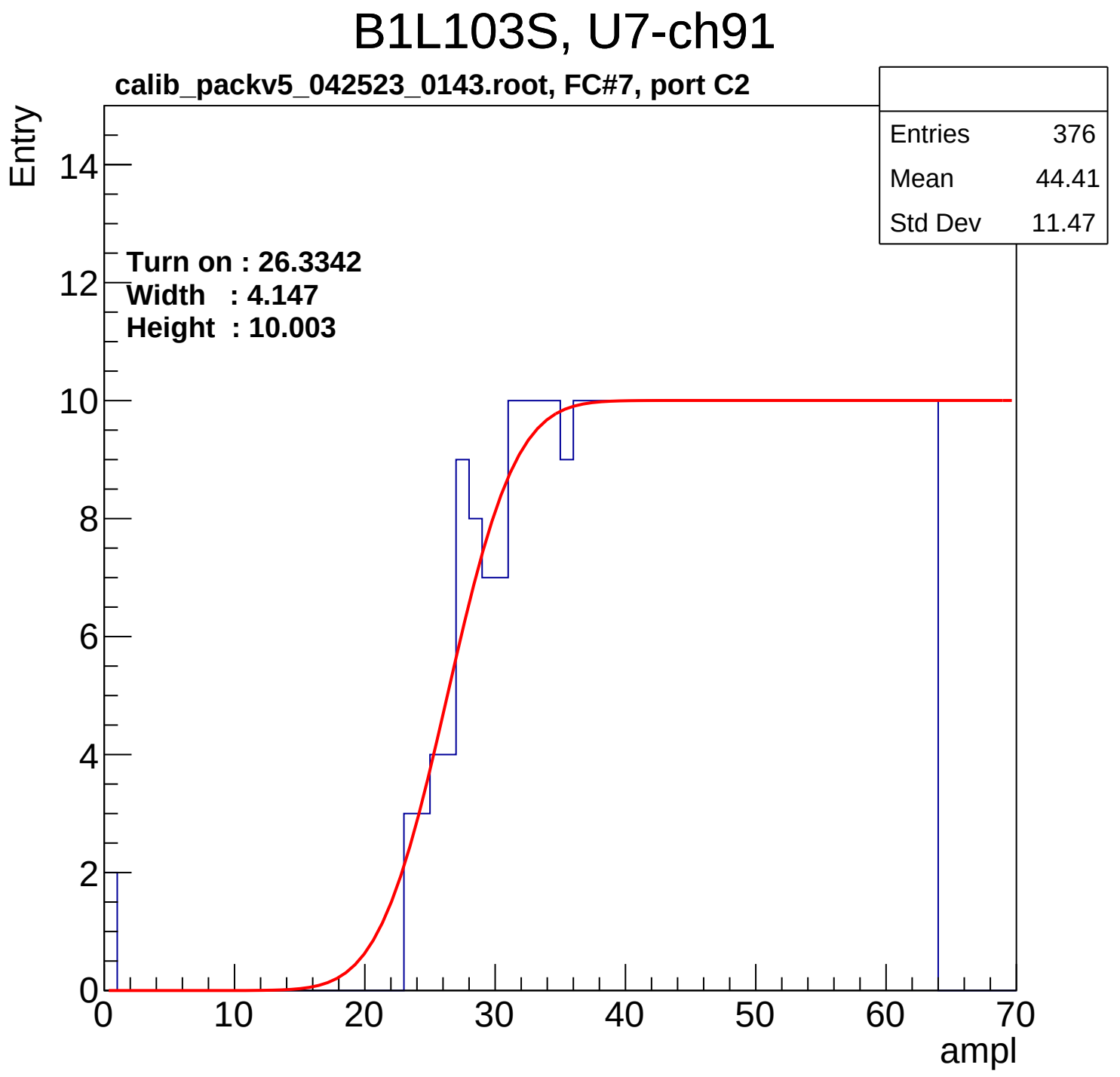
B1L103S, U7-ch91
calib_packv5_042523_0143.root, FC#7, port C2
Entries 376
Mean 44.41
Std Dev 11.47
Turn on : 26.3342
Width : 4.147
Height : 10.003
Entry
ampl
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2
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0
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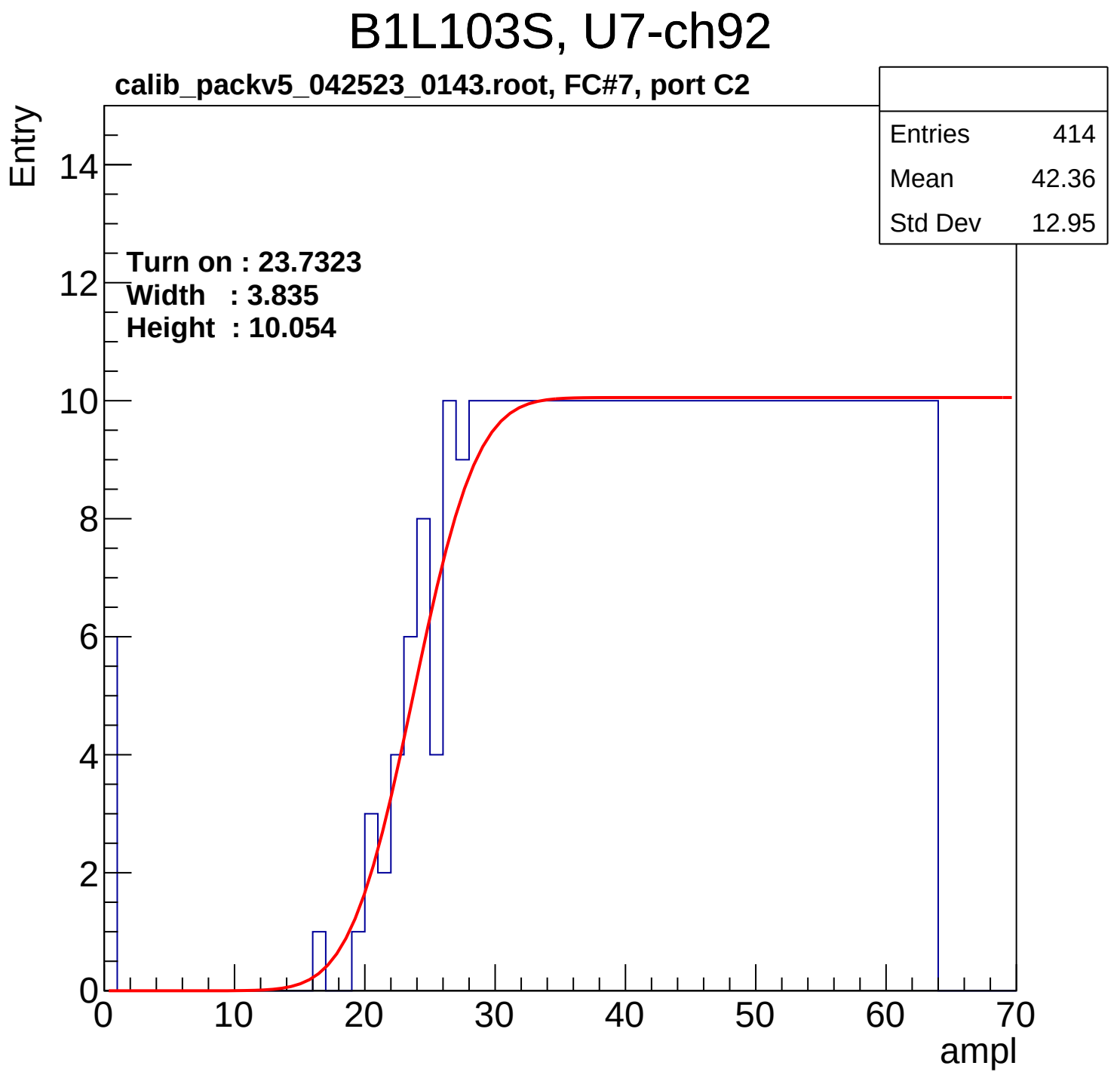
B1L103S, U7-ch92
calib_packv5_042523_0143.root, FC#7, port C2
Entries 414
Mean 42.36
Std Dev 12.95
Turn on : 23.7323
Width : 3.835
Height : 10.054
Entry
ampl
0
2
4
6
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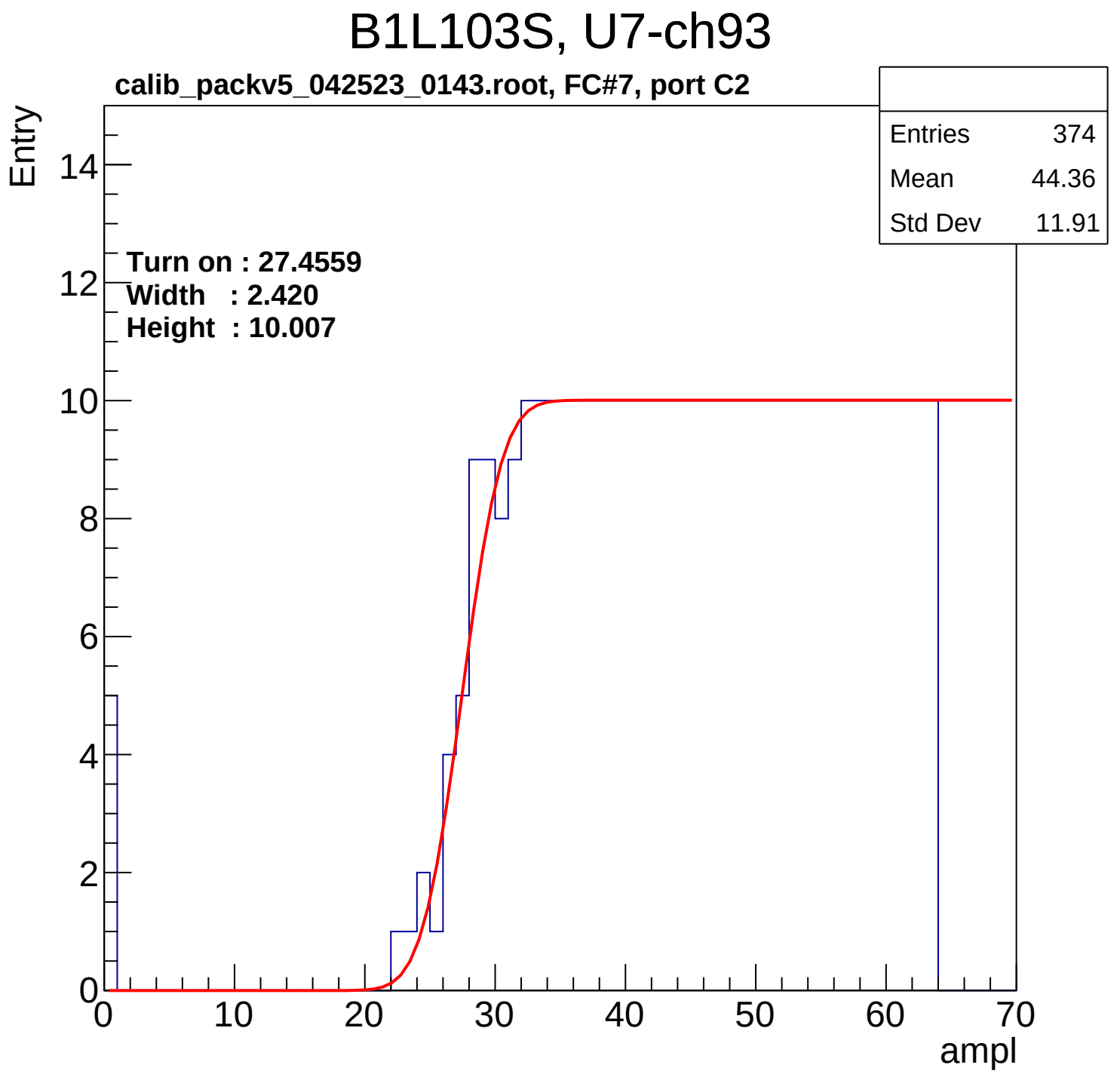
B1L103S, U7-ch93
calib_packv5_042523_0143.root, FC#7, port C2
Entries 374
Mean 44.36
Std Dev 11.91
Turn on : 27.4559
Width : 2.420
Height : 10.007
Entry
ampl
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6
8
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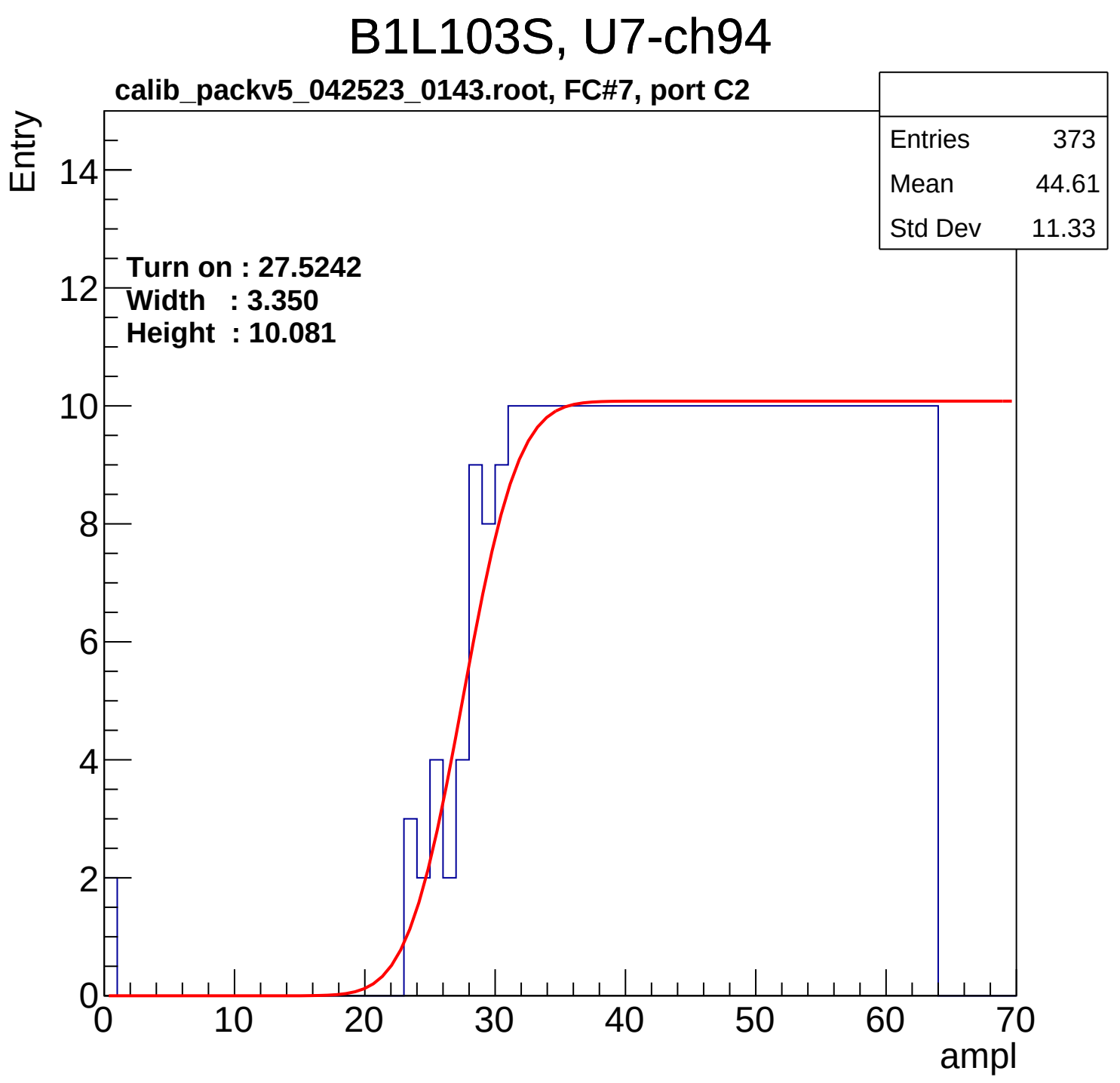
B1L103S, U7-ch94
calib_packv5_042523_0143.root, FC#7, port C2
Entries 373
Mean 44.61
Std Dev 11.33
Turn on : 27.5242
Width : 3.350
Height : 10.081
Entry
ampl
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4
6
8
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60
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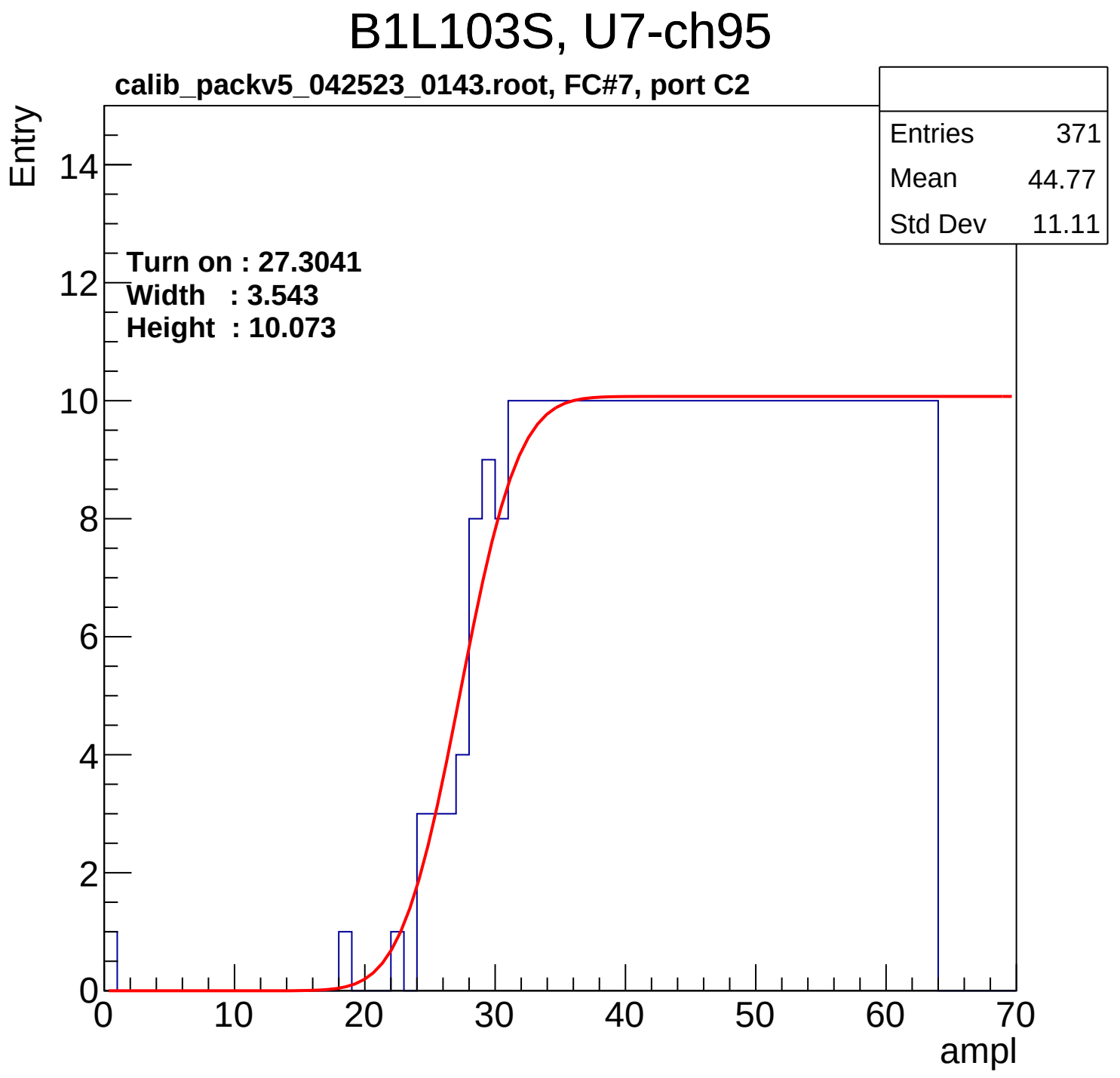
B1L103S, U7-ch95
calib_packv5_042523_0143.root, FC#7, port C2
Entries 371
Mean 44.77
Std Dev 11.11
Turn on : 27.3041
Width : 3.543
Height : 10.073
Entry
ampl
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6
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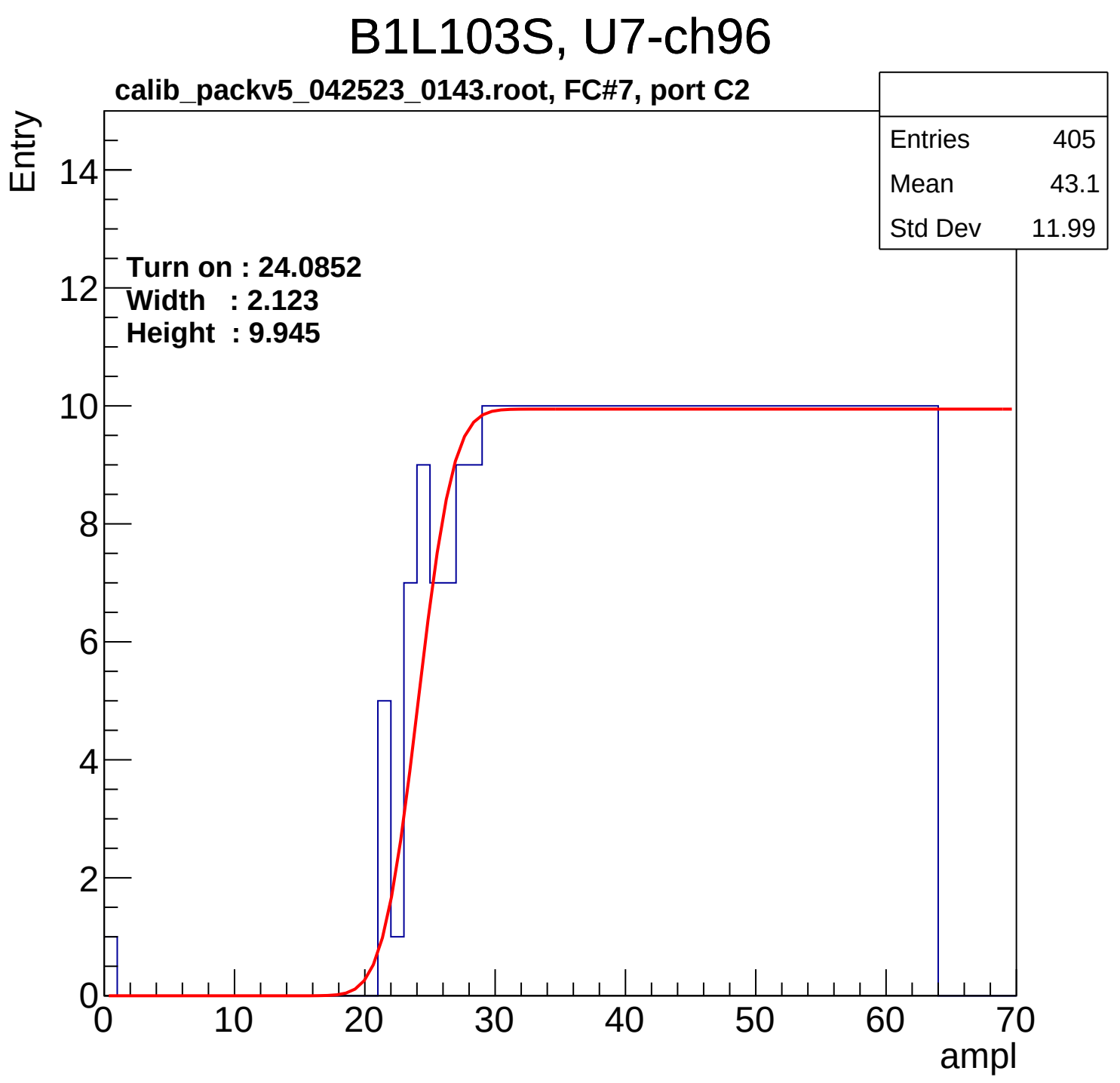
B1L103S, U7-ch96
calib_packv5_042523_0143.root, FC#7, port C2
Entries 405
Mean 43.1
Std Dev 11.99
Turn on : 24.0852
Width : 2.123
Height : 9.945
Entry
ampl
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6
8
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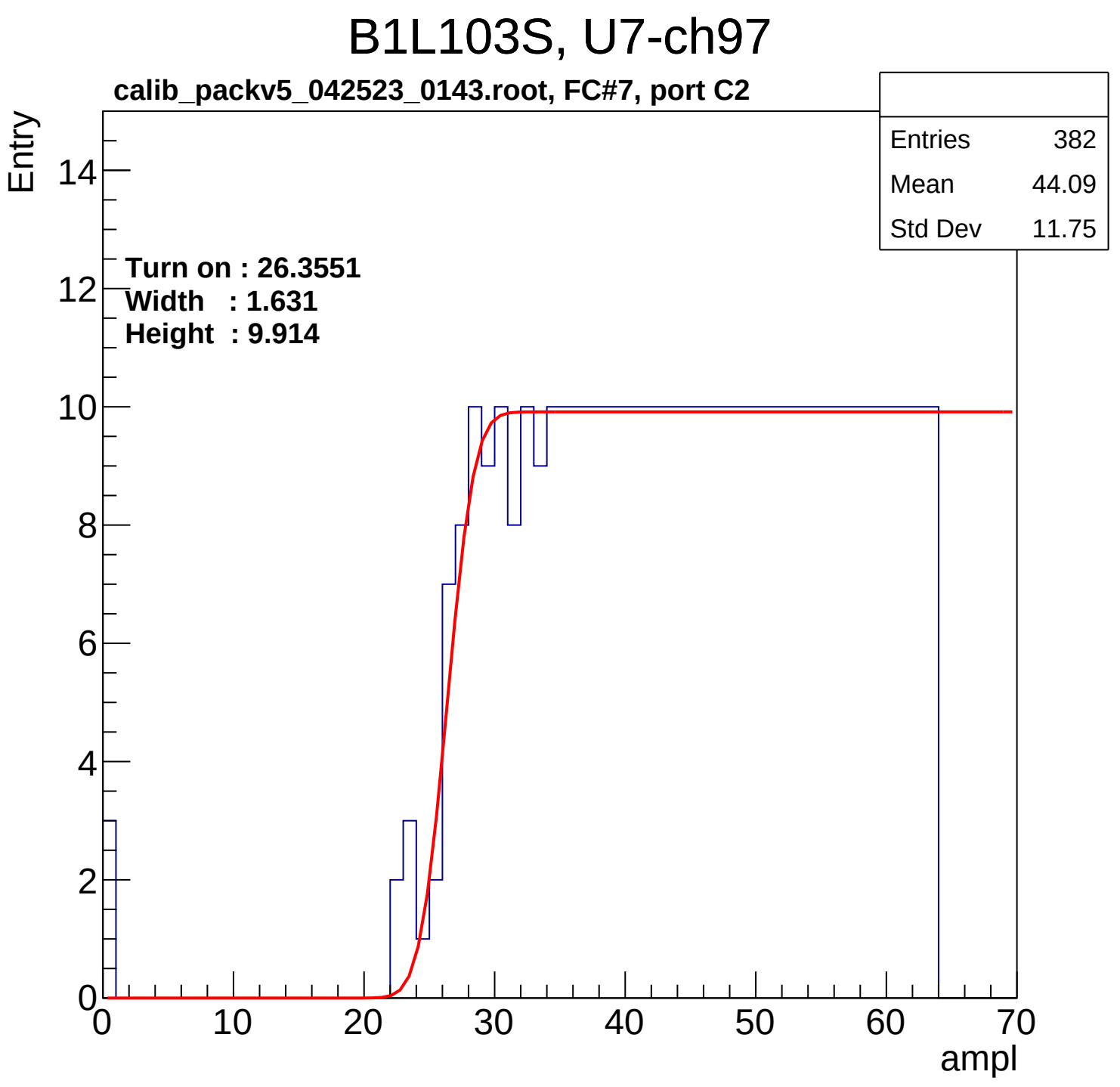
B1L103S, U7-ch97
calib_packv5_042523_0143.root, FC#7, port C2
Entries 382
Mean 44.09
Std Dev 11.75
Turn on : 26.3551
Width : 1.631
Height : 9.914
Entry
ampl
0
2
4
6
8
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0
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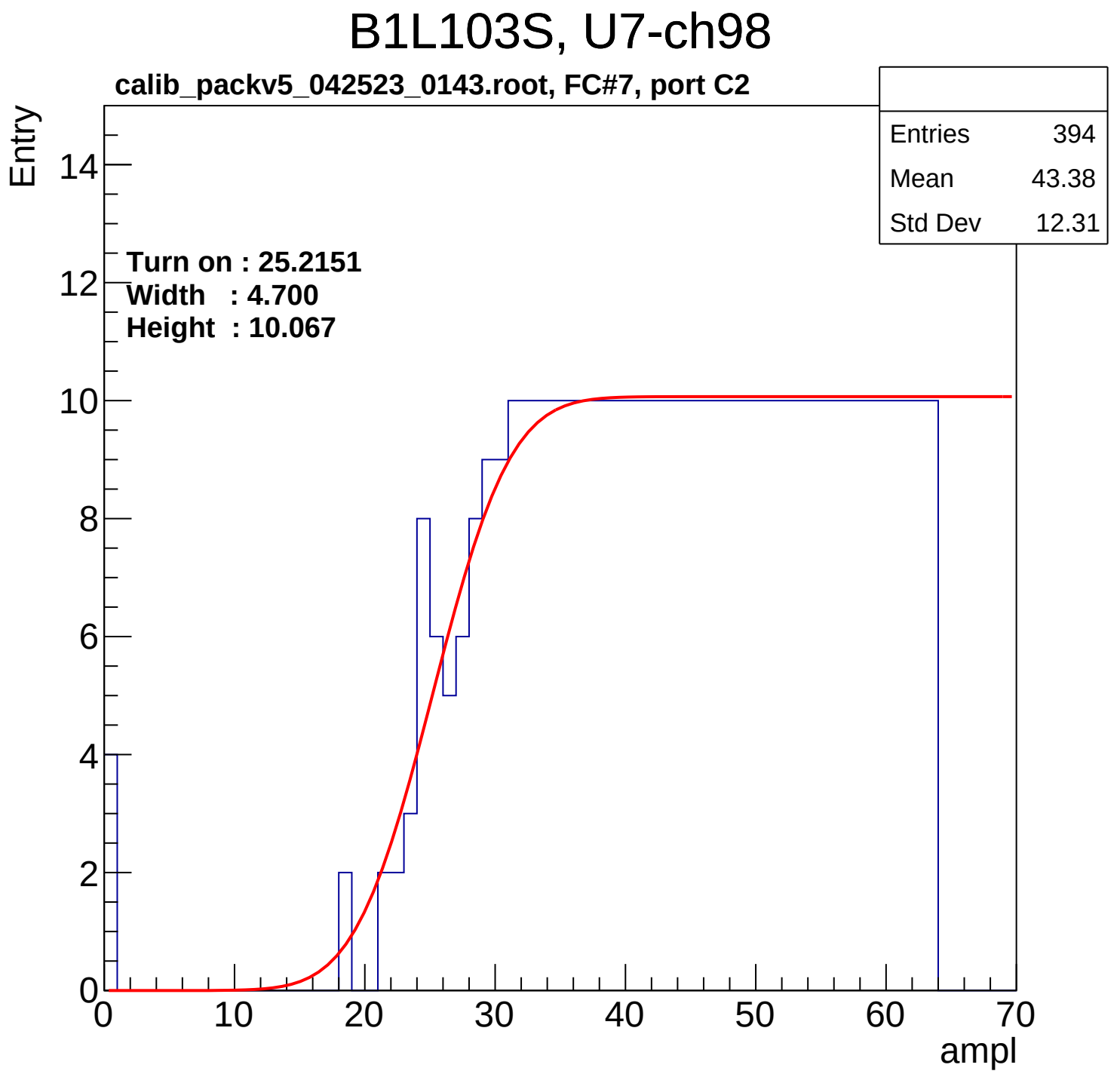
B1L103S, U7-ch98
calib_packv5_042523_0143.root, FC#7, port C2
Entries 394
Mean 43.38
Std Dev 12.31
Turn on : 25.2151
Width : 4.700
Height : 10.067
Entry
ampl
0
2
4
6
8
10
12
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0
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20
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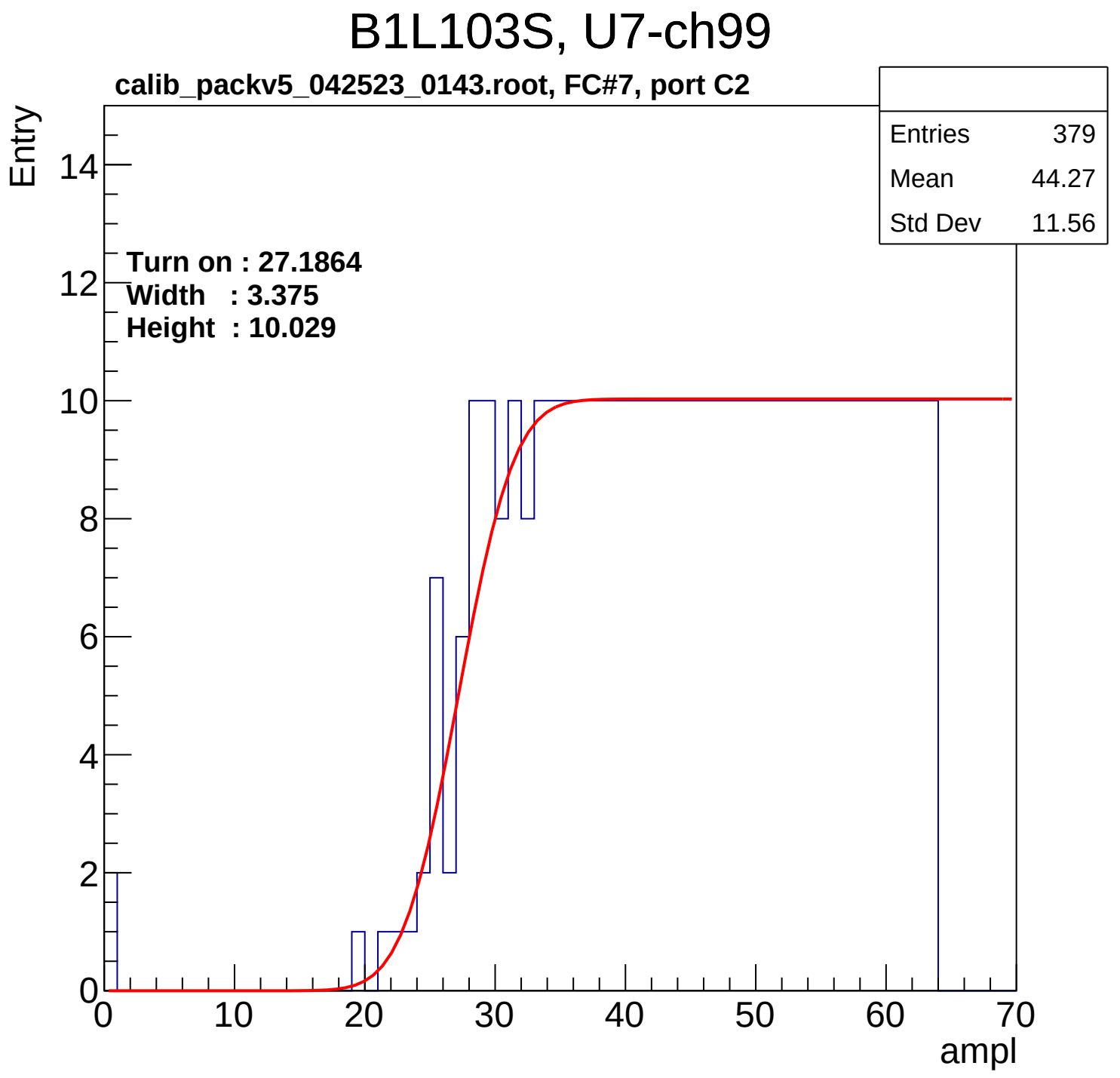
B1L103S, U7-ch99
calib_packv5_042523_0143.root, FC#7, port C2
Entries 379
Mean 44.27
Std Dev 11.56
Turn on : 27.1864
Width : 3.375
Height : 10.029
Entry
ampl
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6
8
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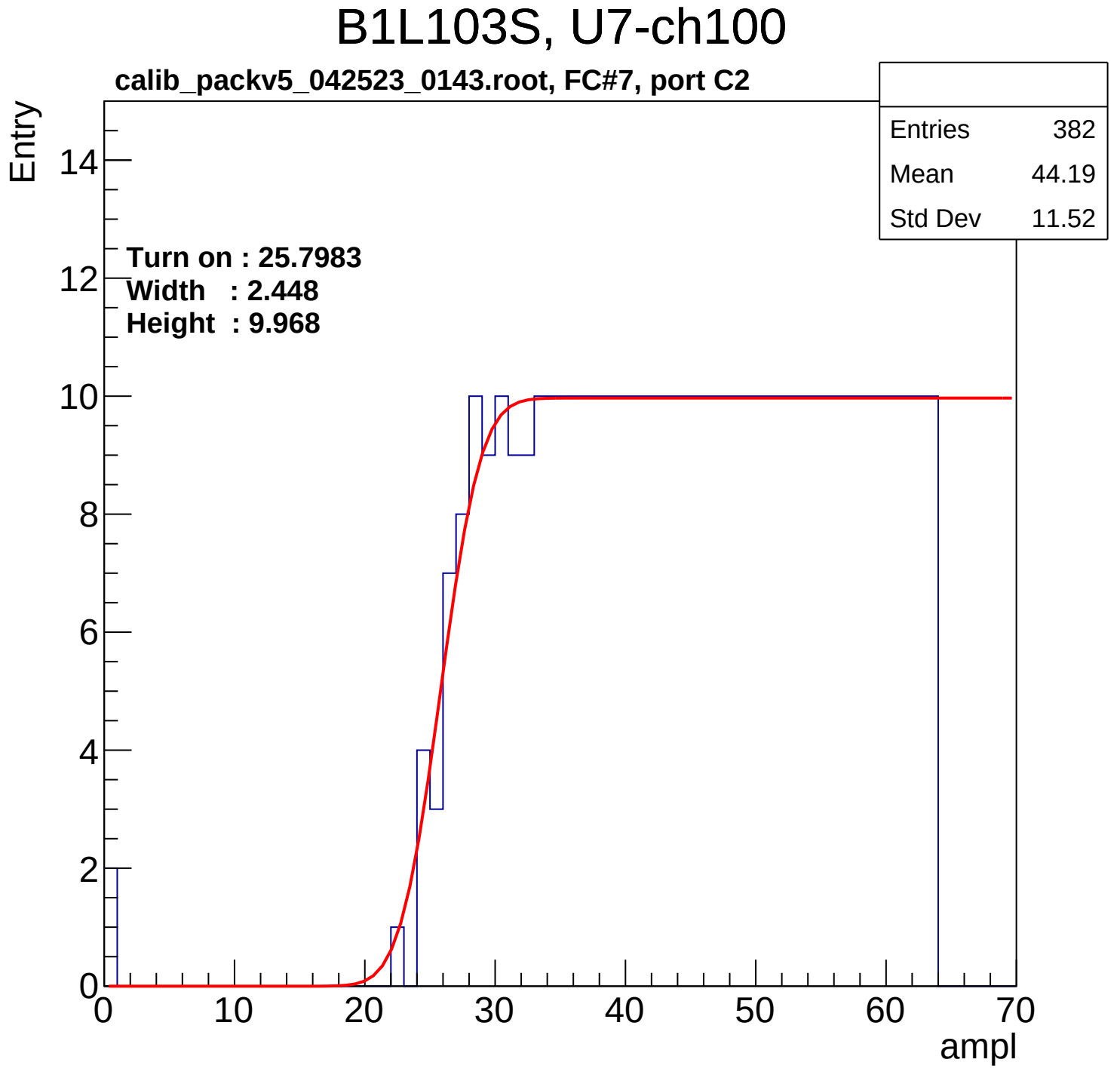
B1L103S, U7-ch100
calib_packv5_042523_0143.root, FC#7, port C2
Entries 382
Mean 44.19
Std Dev 11.52
Turn on : 25.7983
Width : 2.448
Height : 9.968
Entry
ampl
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6
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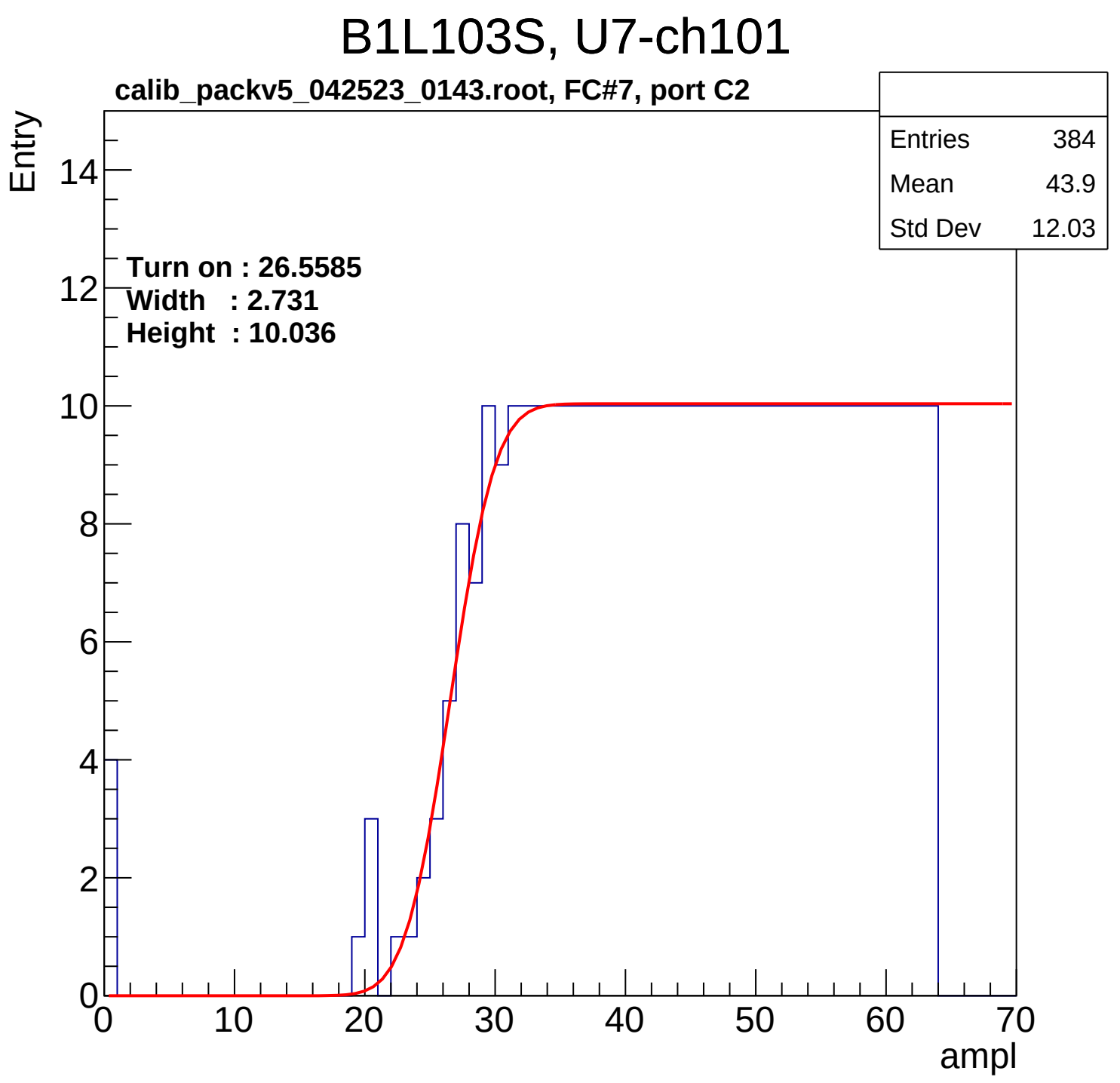
B1L103S, U7-ch101
calib_packv5_042523_0143.root, FC#7, port C2
Entries 384
Mean 43.9
Std Dev 12.03
Turn on : 26.5585
Width : 2.731
Height : 10.036
Entry
ampl
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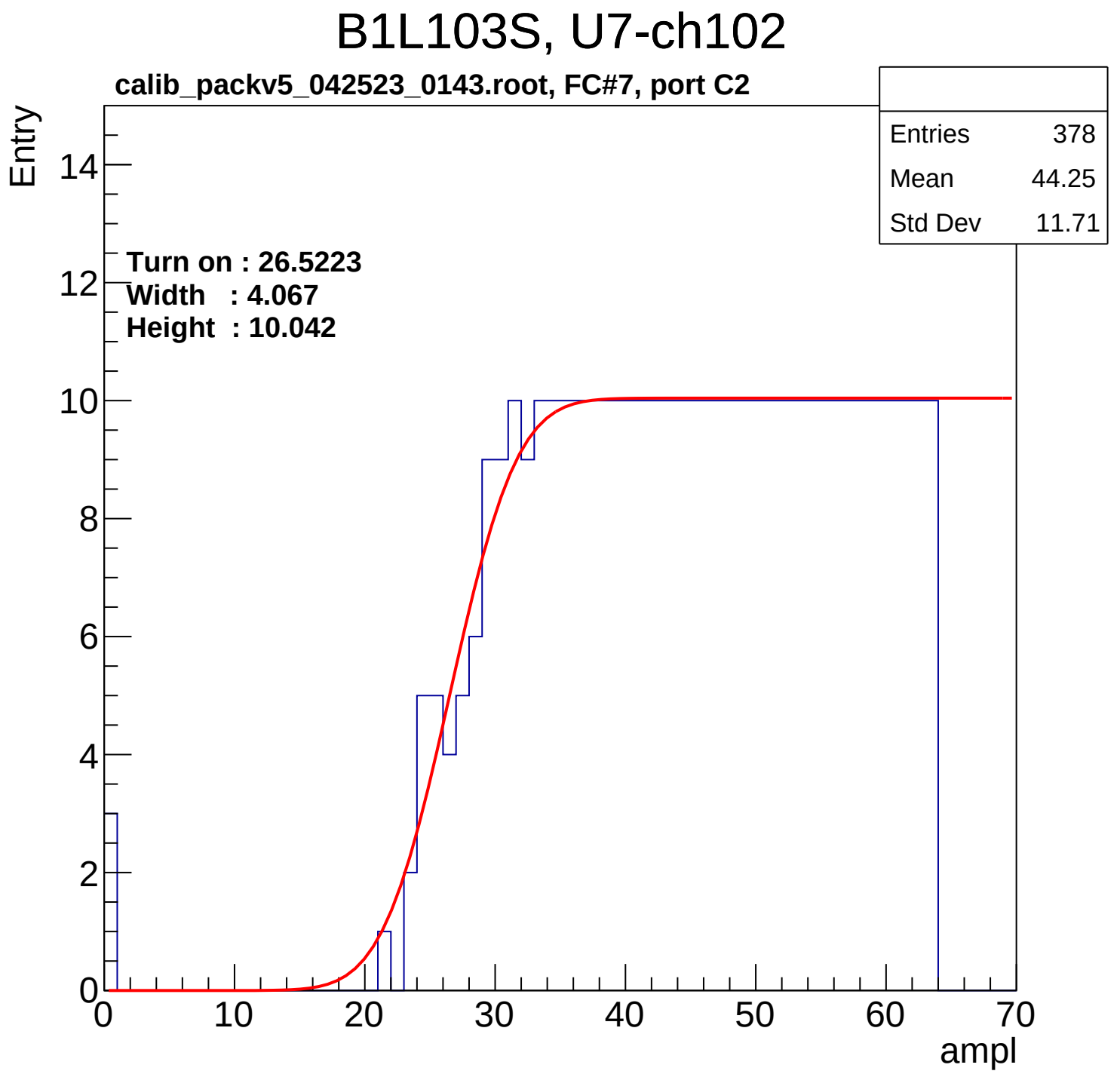
B1L103S, U7-ch102
calib_packv5_042523_0143.root, FC#7, port C2
Entries 378
Mean 44.25
Std Dev 11.71
Turn on : 26.5223
Width : 4.067
Height : 10.042
Entry
ampl
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6
8
10
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0
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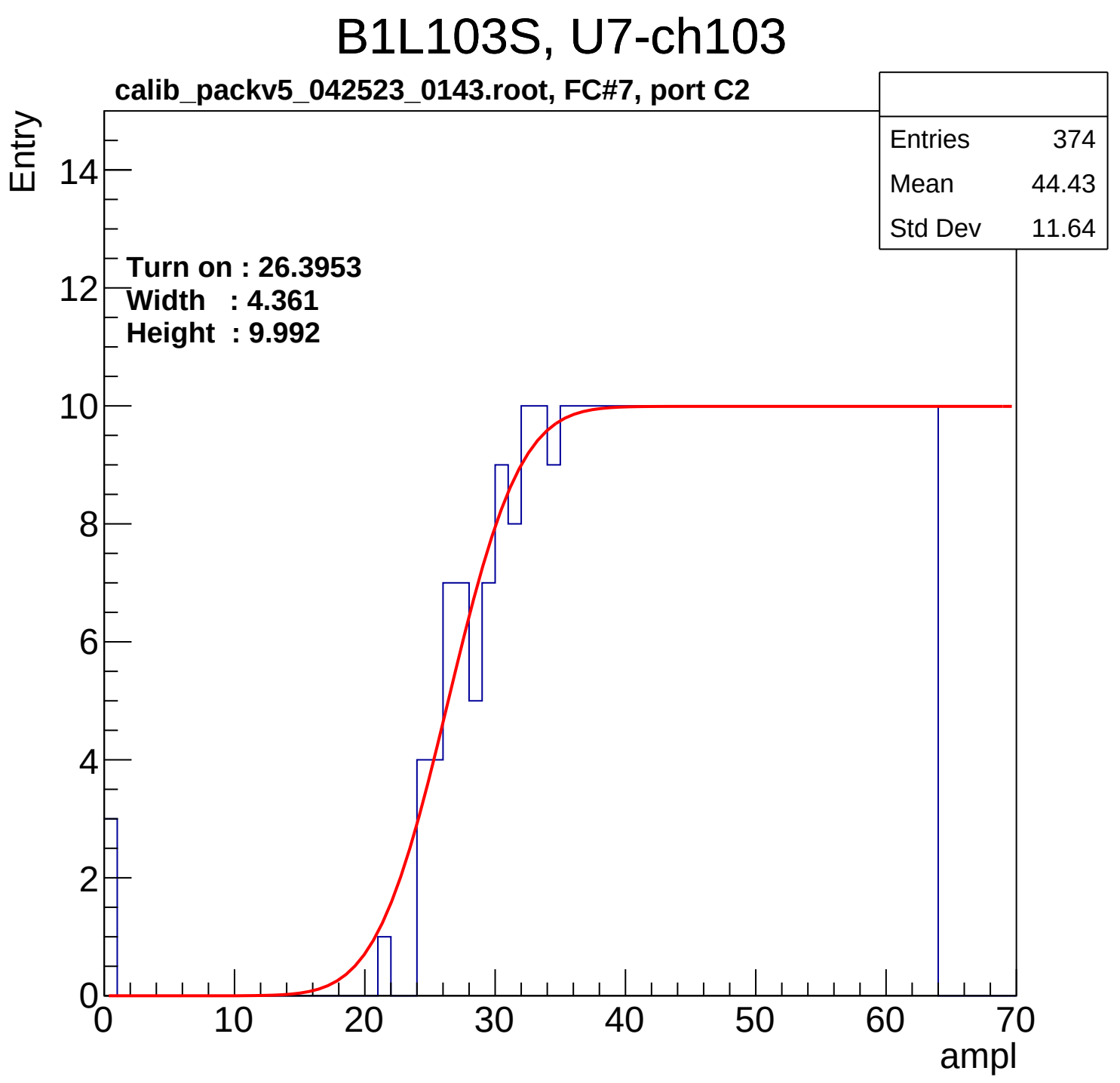
B1L103S, U7-ch103
calib_packv5_042523_0143.root, FC#7, port C2
Entries 374
Mean 44.43
Std Dev 11.64
Turn on : 26.3953
Width : 4.361
Height : 9.992
Entry
ampl
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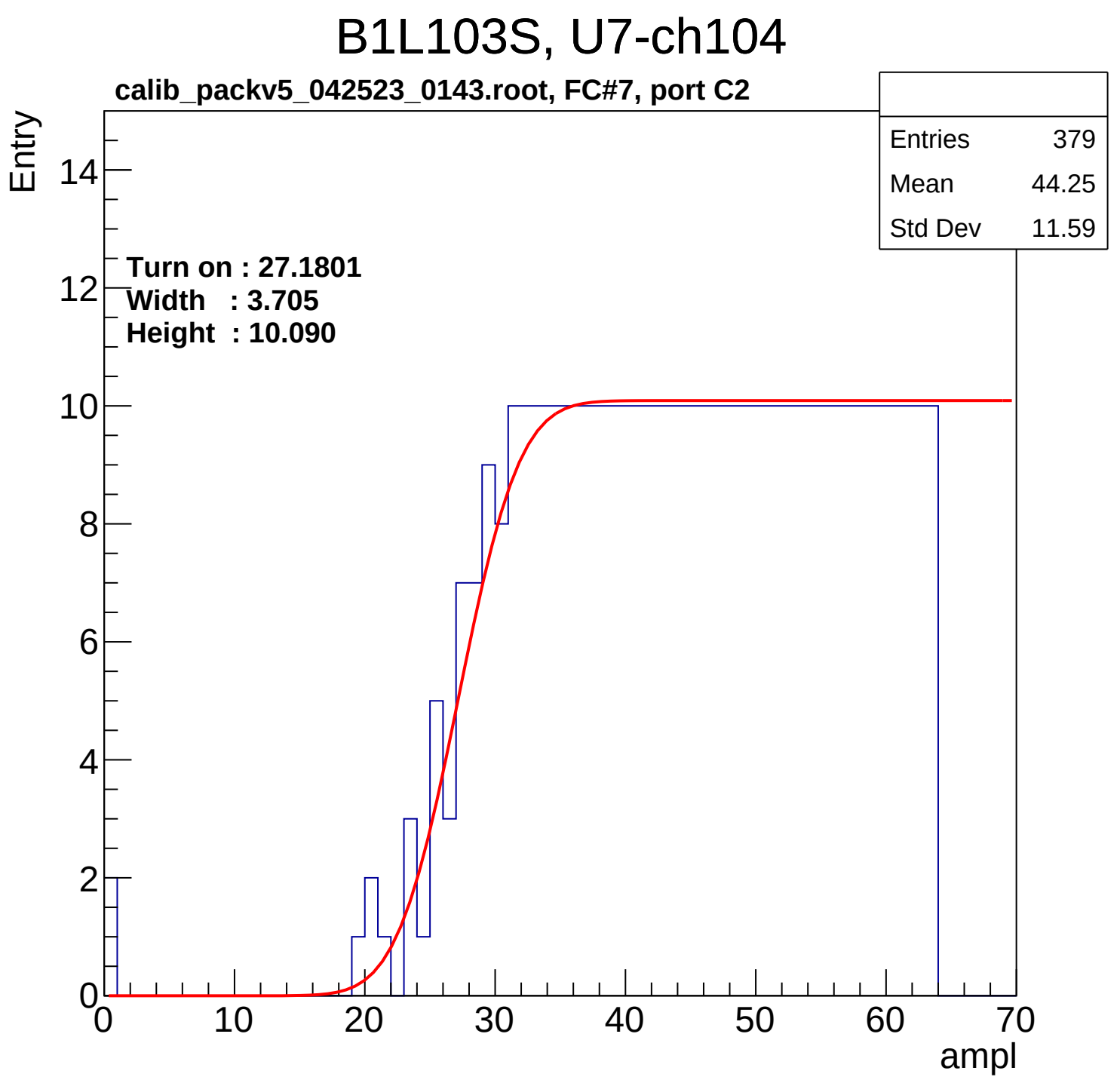
B1L103S, U7-ch104
calib_packv5_042523_0143.root, FC#7, port C2
Entries 379
Mean 44.25
Std Dev 11.59
Turn on : 27.1801
Width : 3.705
Height : 10.090
Entry
ampl
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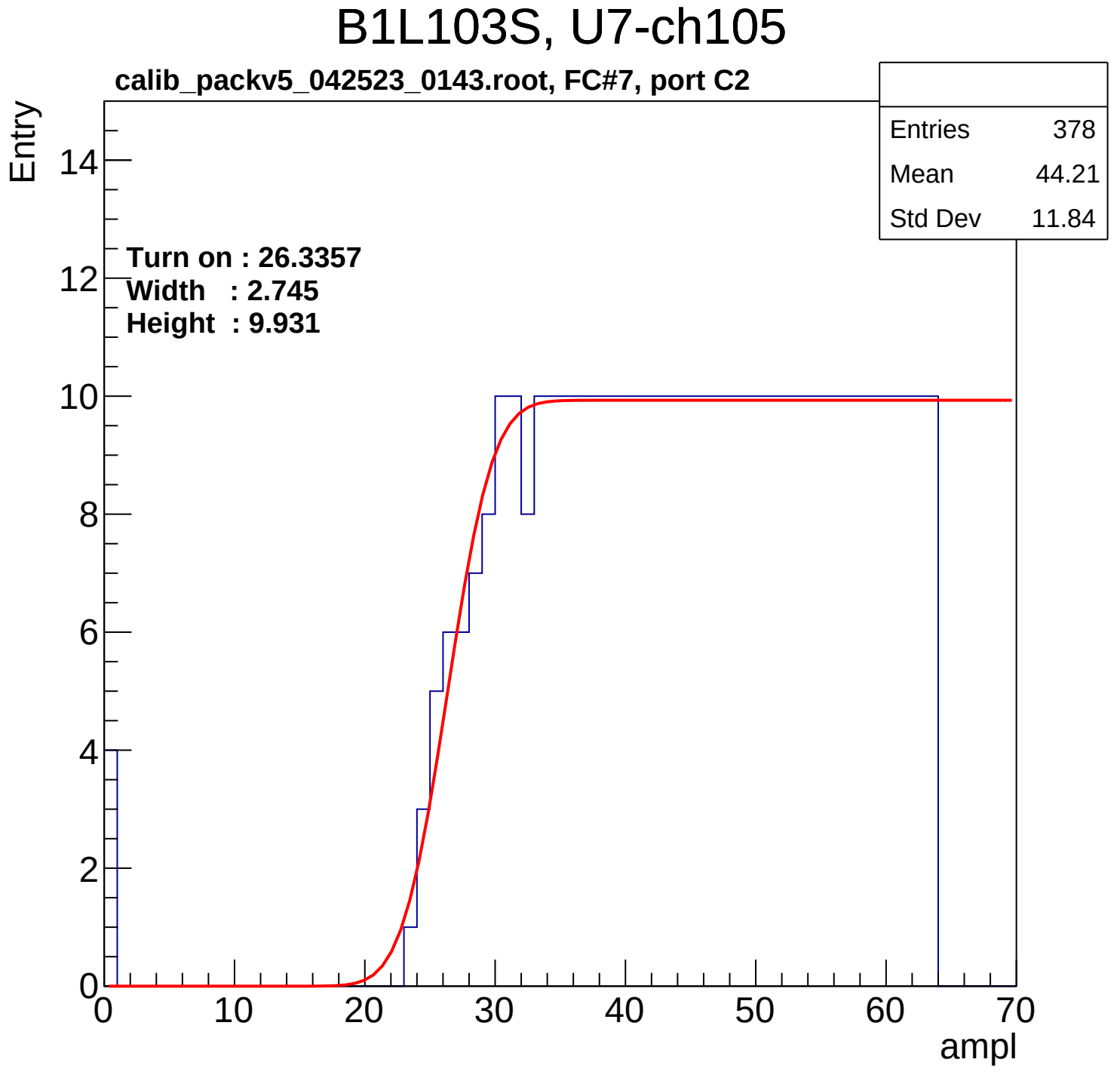
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calib_packv5_042523_0143.root, FC#7, port C2
Entries 378
Mean 44.21
Std Dev 11.84
Turn on : 26.3357
Width : 2.745
Height : 9.931
Entry
ampl
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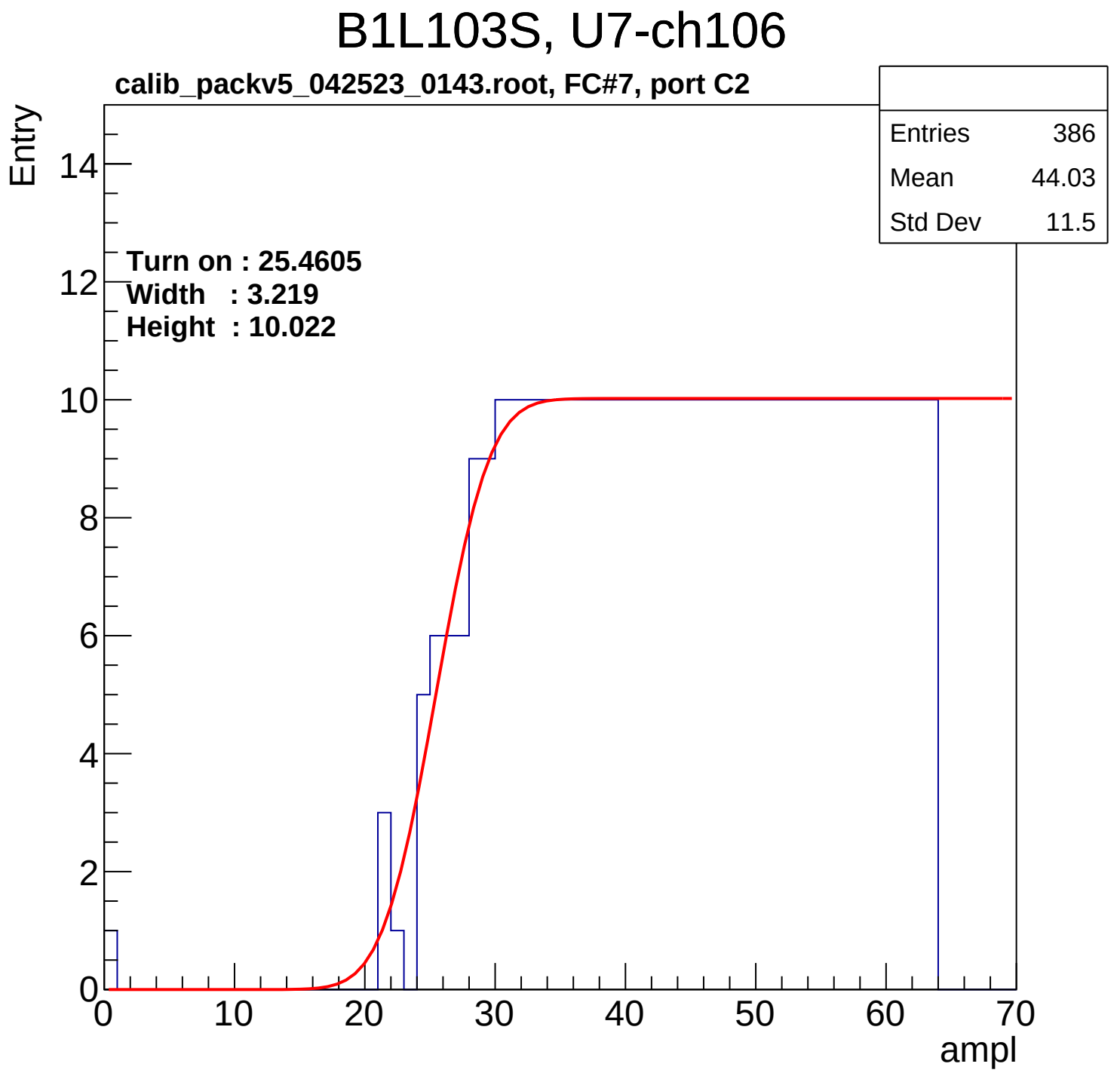
B1L103S, U7-ch106
calib_packv5_042523_0143.root, FC#7, port C2
Entries 386
Mean 44.03
Std Dev 11.5
Turn on : 25.4605
Width : 3.219
Height : 10.022
Entry
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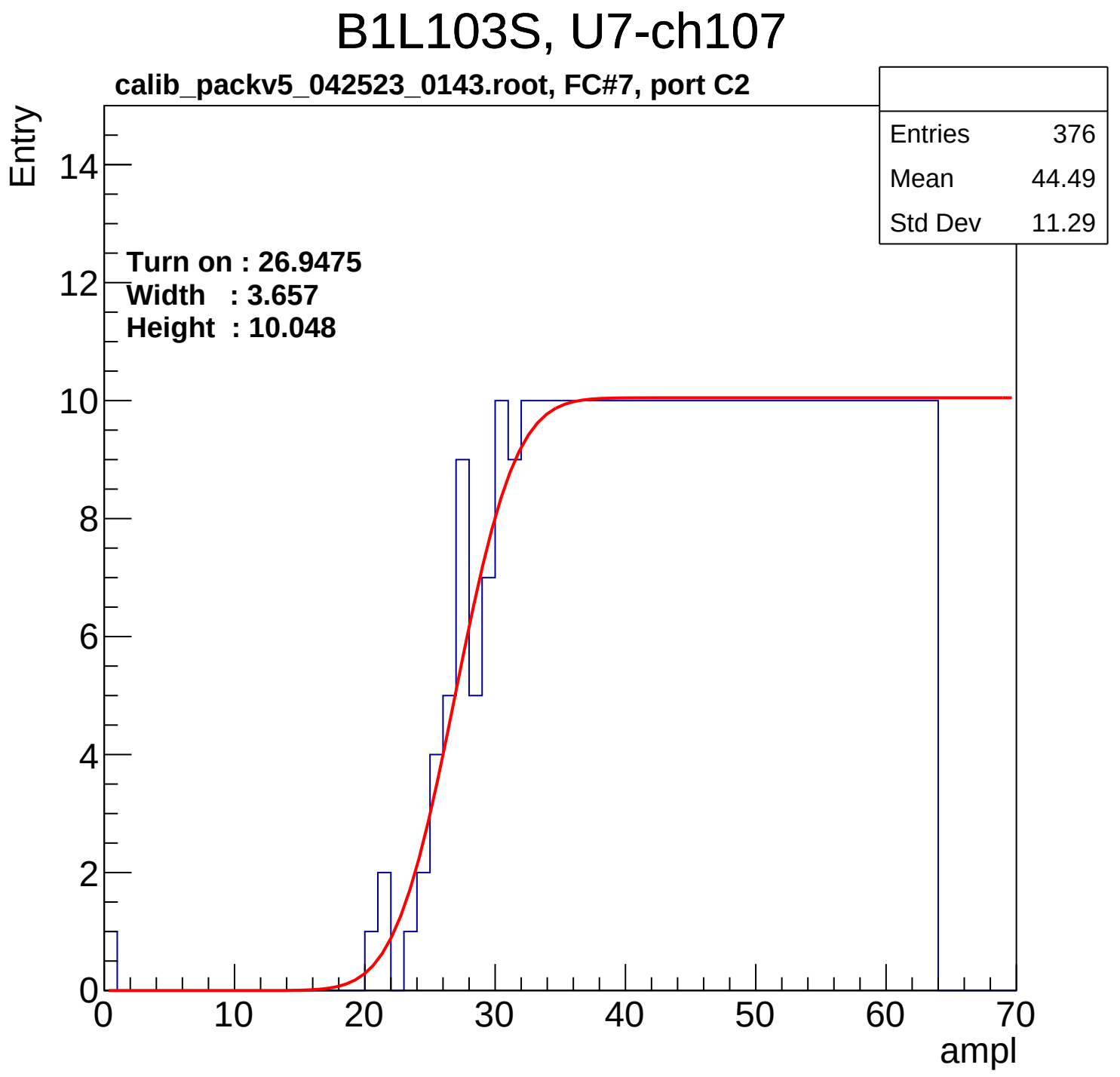
B1L103S, U7-ch107
calib_packv5_042523_0143.root, FC#7, port C2
Entries 376
Mean 44.49
Std Dev 11.29
Turn on : 26.9475
Width : 3.657
Height : 10.048
Entry
ampl
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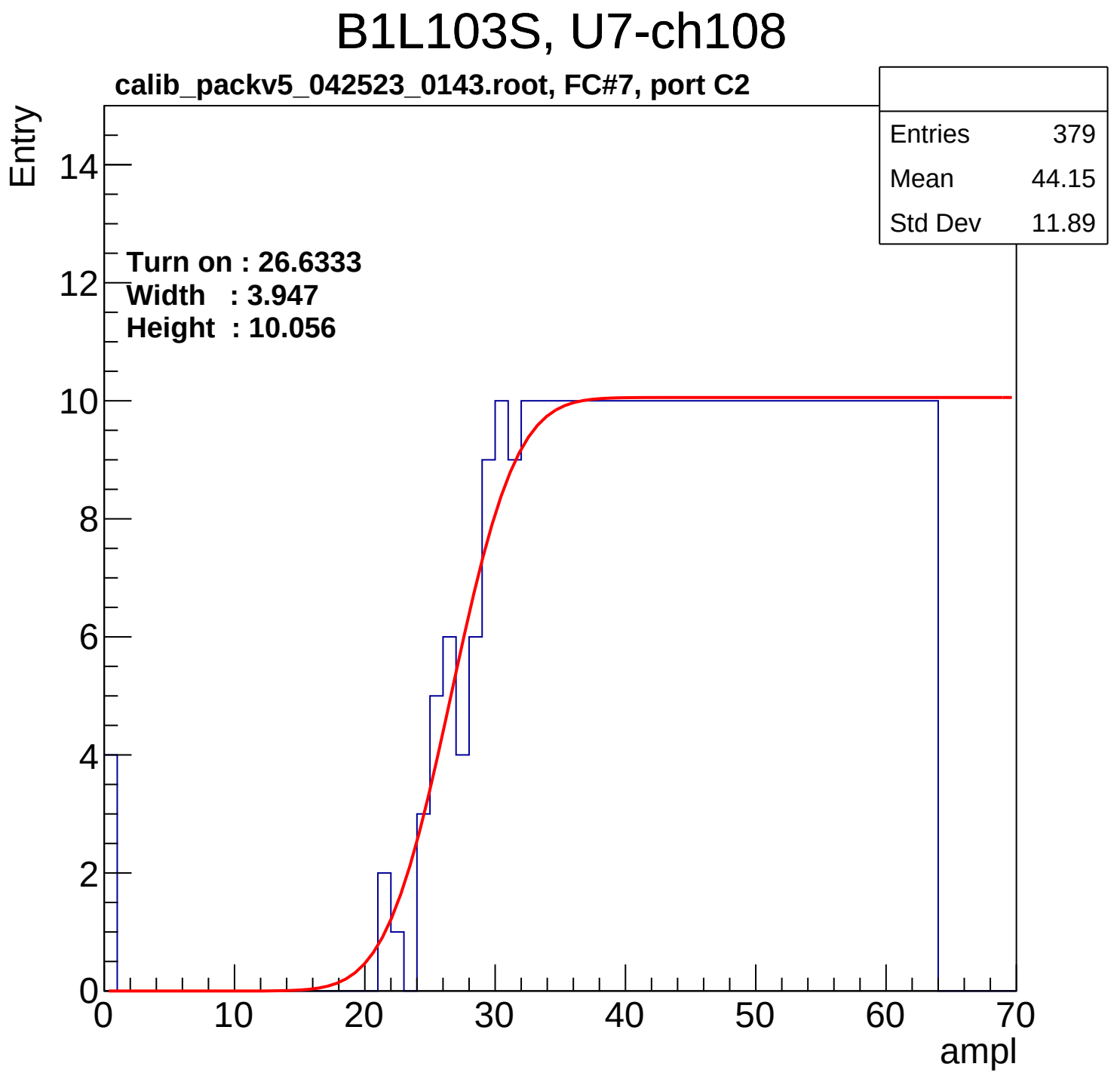
B1L103S, U7-ch108
calib_packv5_042523_0143.root, FC#7, port C2
Entries 379
Mean 44.15
Std Dev 11.89
Turn on : 26.6333
Width : 3.947
Height : 10.056
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ampl
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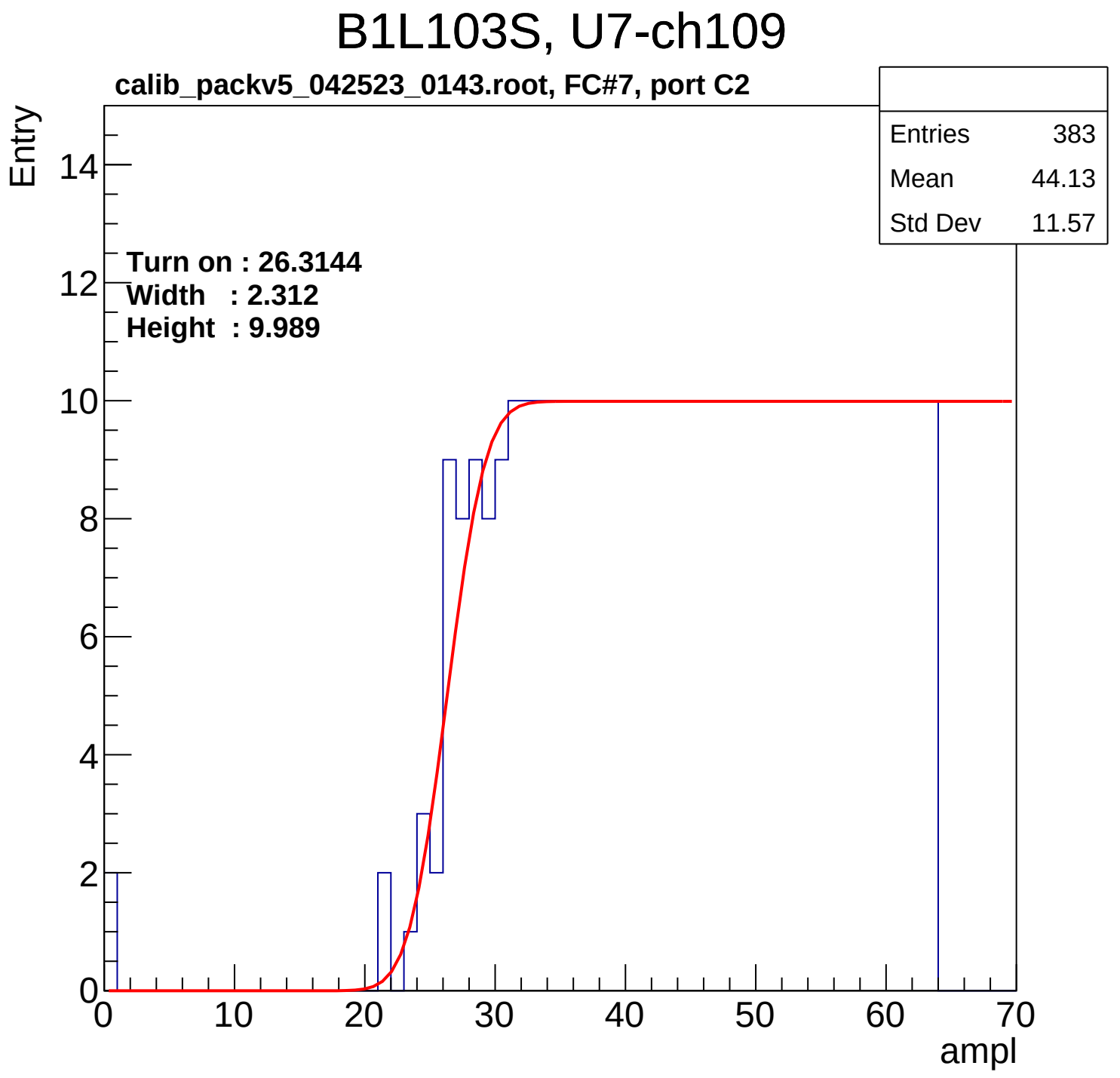
B1L103S, U7-ch109
calib_packv5_042523_0143.root, FC#7, port C2
Entries 383
Mean 44.13
Std Dev 11.57
Turn on : 26.3144
Width : 2.312
Height : 9.989
Entry
ampl
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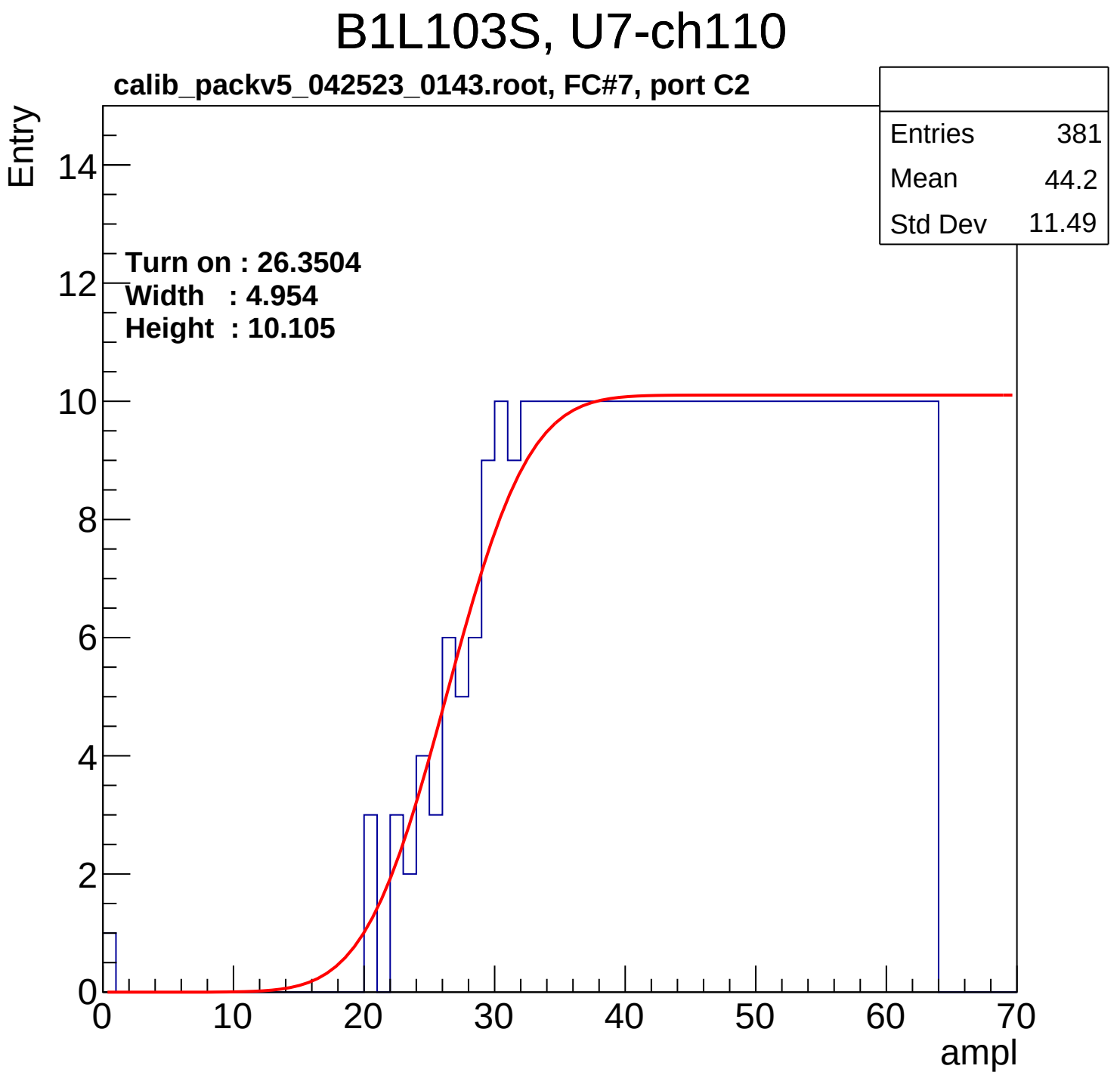
B1L103S, U7-ch110
calib_packv5_042523_0143.root, FC#7, port C2
Entries 381
Mean 44.2
Std Dev 11.49
Turn on : 26.3504
Width : 4.954
Height : 10.105
Entry
ampl
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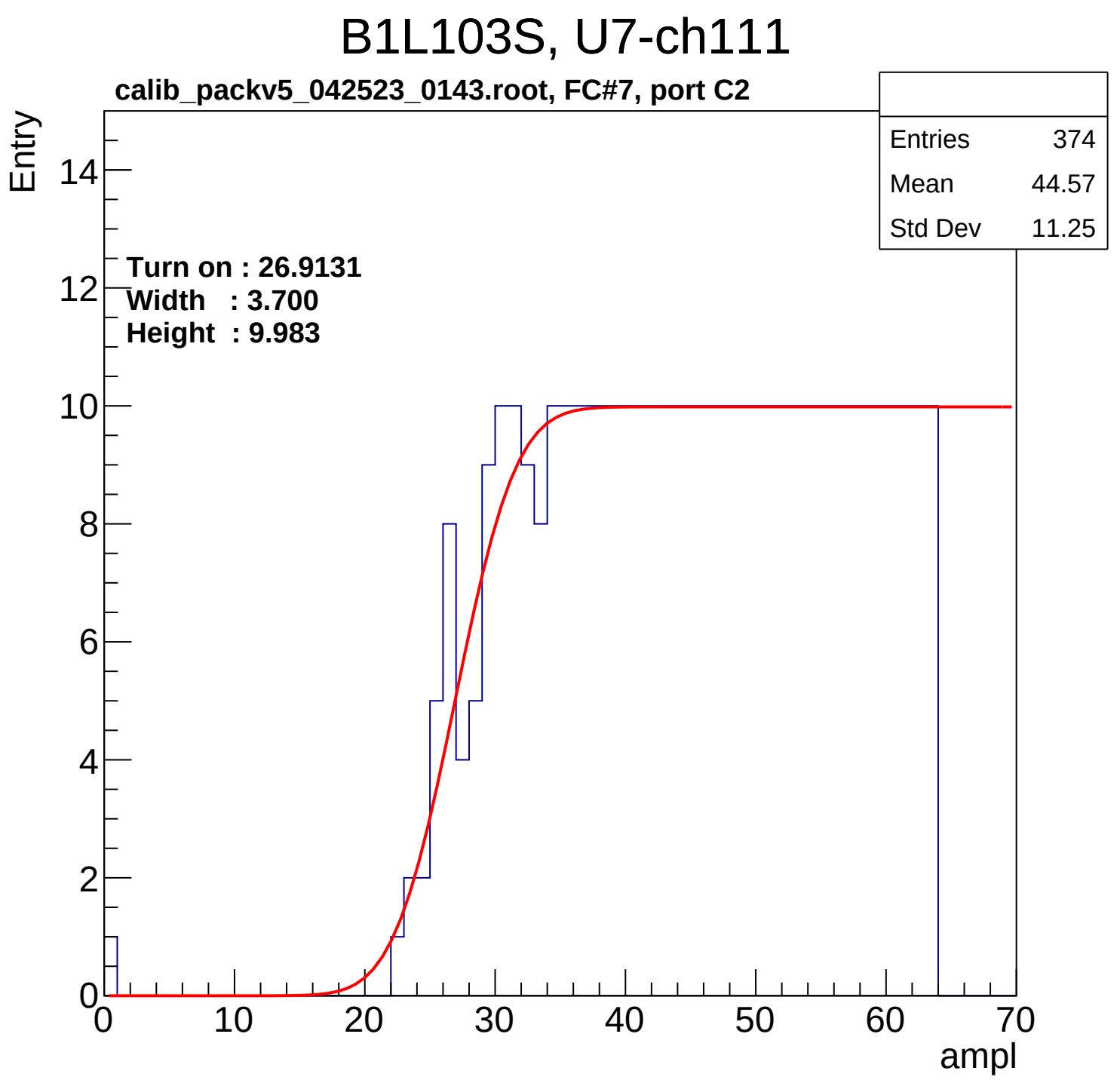
B1L103S, U7-ch111
calib_packv5_042523_0143.root, FC#7, port C2
Entries 374
Mean 44.57
Std Dev 11.25
Turn on : 26.9131
Width : 3.700
Height : 9.983
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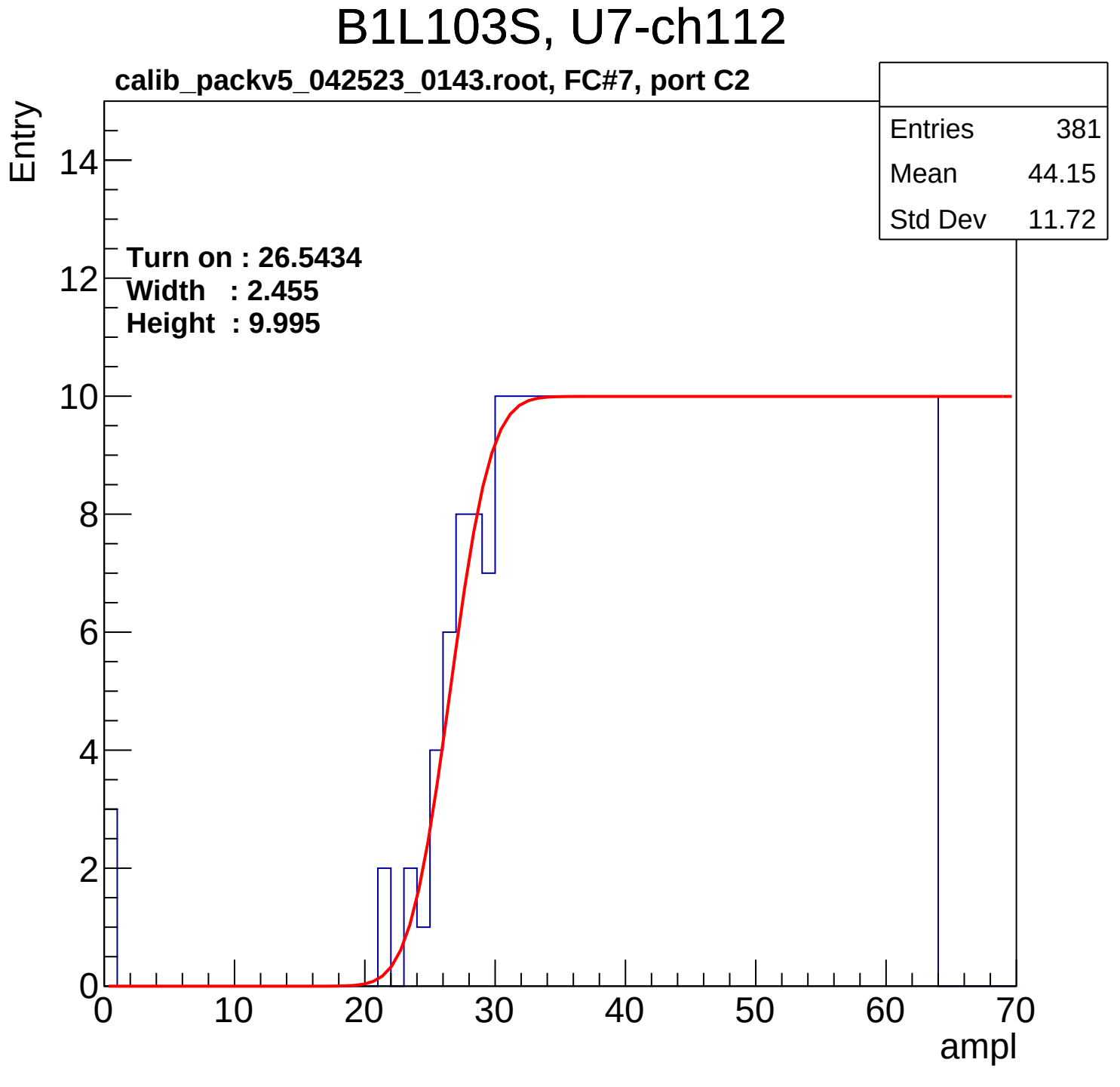
B1L103S, U7-ch112
calib_packv5_042523_0143.root, FC#7, port C2
Entries 381
Mean 44.15
Std Dev 11.72
Turn on : 26.5434
Width : 2.455
Height : 9.995
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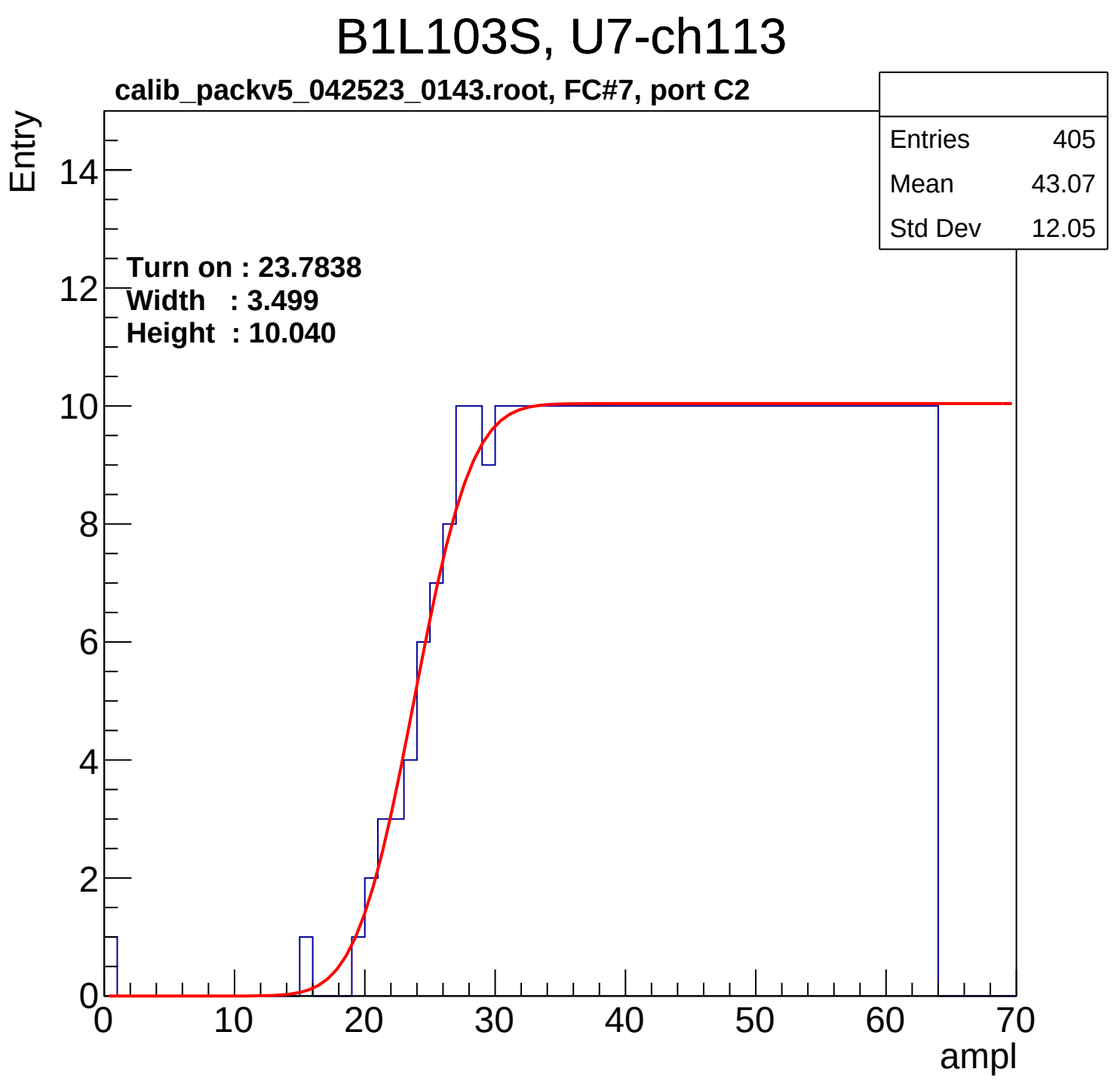
B1L103S, U7-ch113
calib_packv5_042523_0143.root, FC#7, port C2
Entries 405
Mean 43.07
Std Dev 12.05
Turn on : 23.7838
Width : 3.499
Height : 10.040
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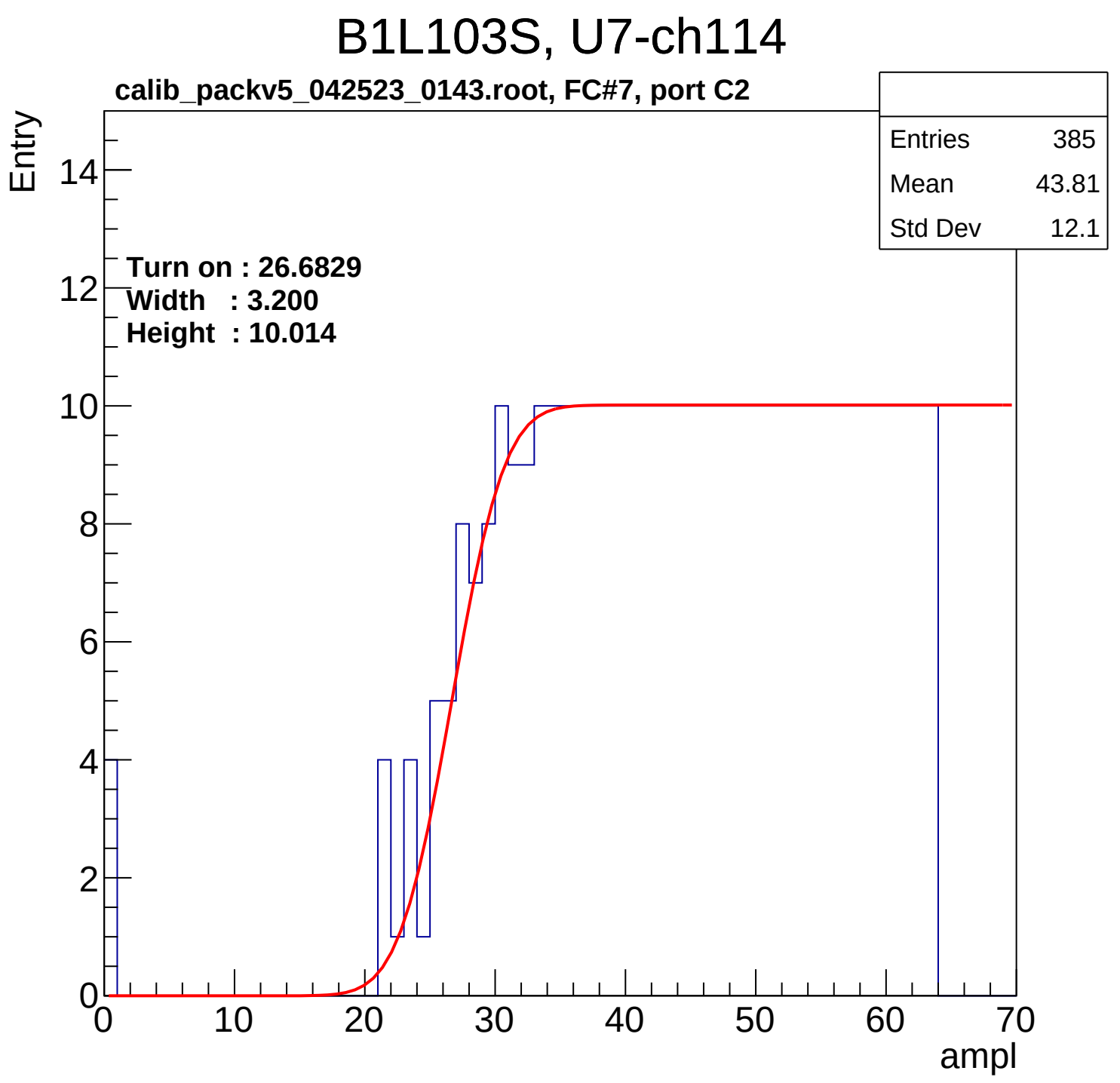
B1L103S, U7-ch114
calib_packv5_042523_0143.root, FC#7, port C2
Entries 385
Mean 43.81
Std Dev 12.1
Turn on : 26.6829
Width : 3.200
Height : 10.014
Entry
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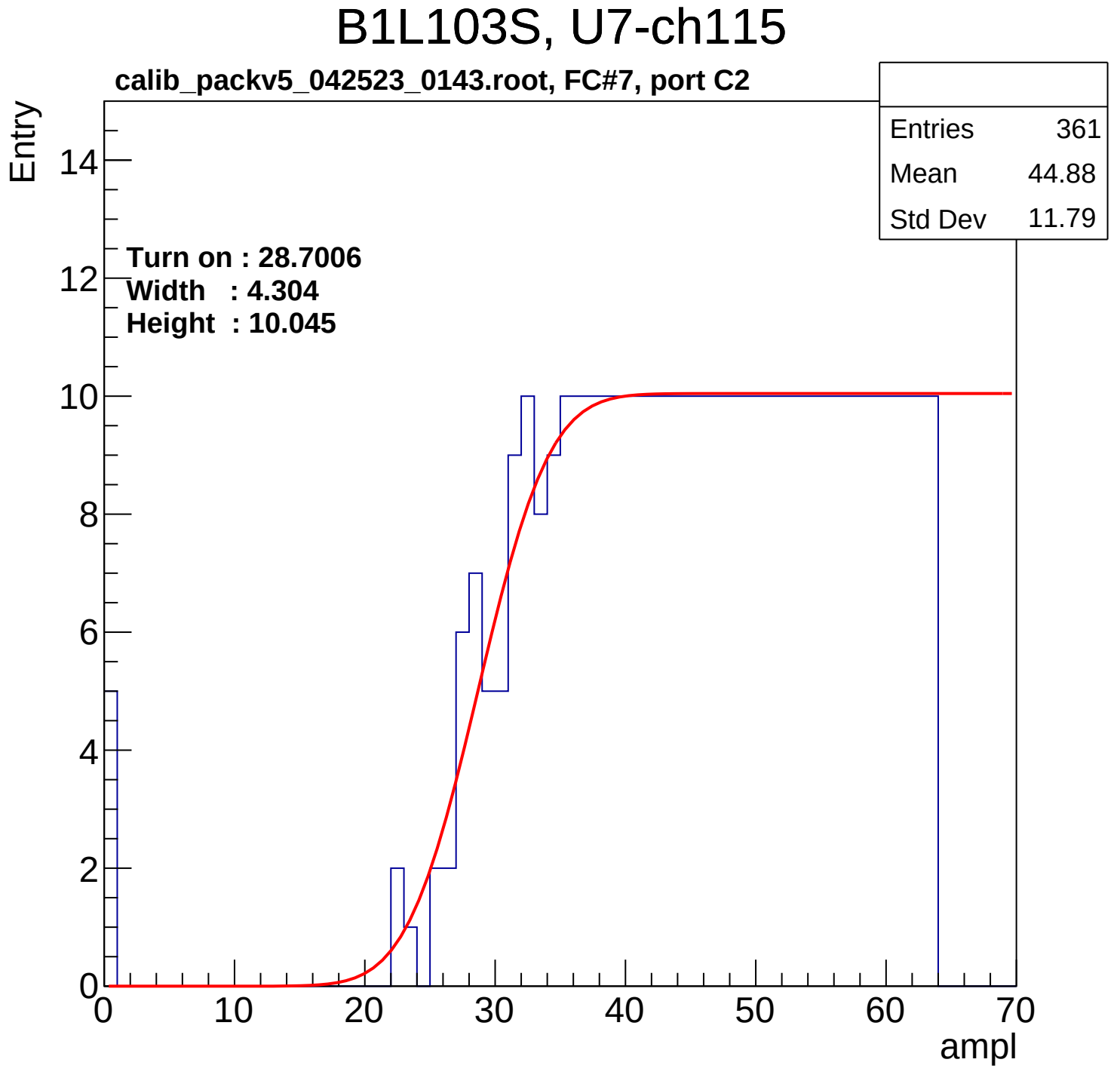
B1L103S, U7-ch115
calib_packv5_042523_0143.root, FC#7, port C2
Entries 361
Mean 44.88
Std Dev 11.79
Turn on : 28.7006
Width : 4.304
Height : 10.045
Entry
ampl
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4
6
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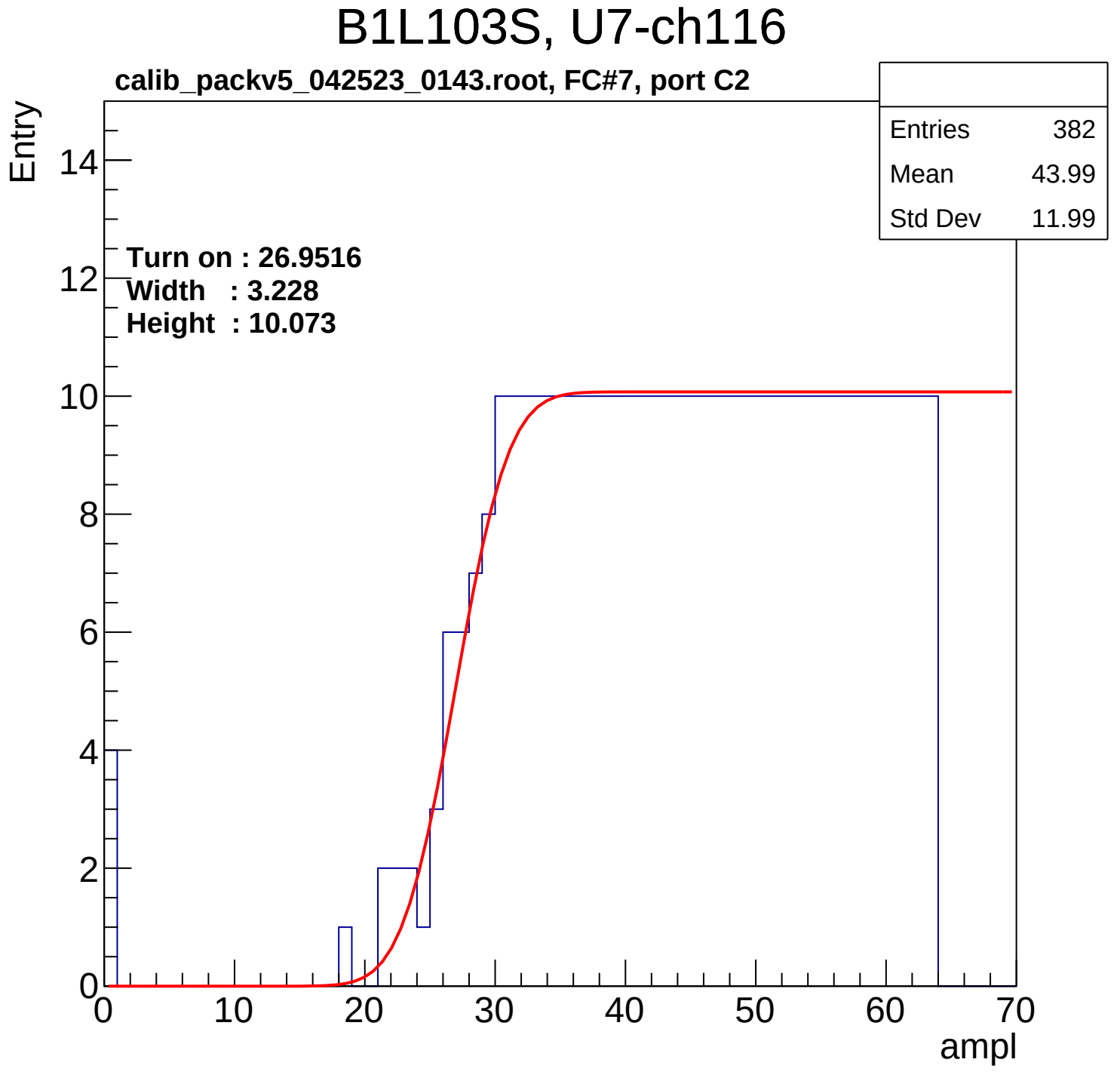
B1L103S, U7-ch116
calib_packv5_042523_0143.root, FC#7, port C2
Entries 382
Mean 43.99
Std Dev 11.99
Turn on : 26.9516
Width : 3.228
Height : 10.073
Entry
ampl
0
2
4
6
8
10
12
14
0
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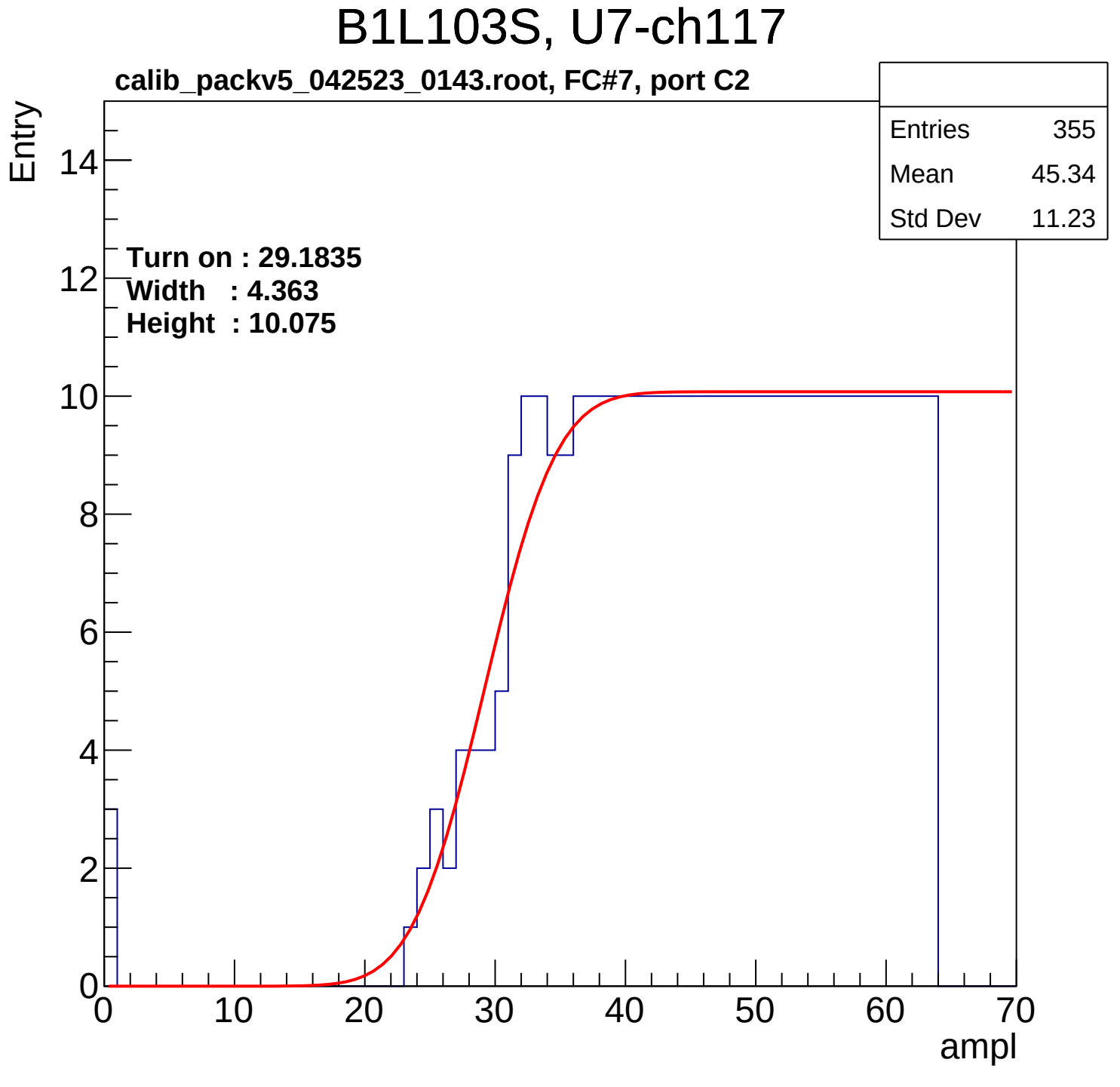
B1L103S, U7-ch117
calib_packv5_042523_0143.root, FC#7, port C2
Entries 355
Mean 45.34
Std Dev 11.23
Turn on : 29.1835
Width : 4.363
Height : 10.075
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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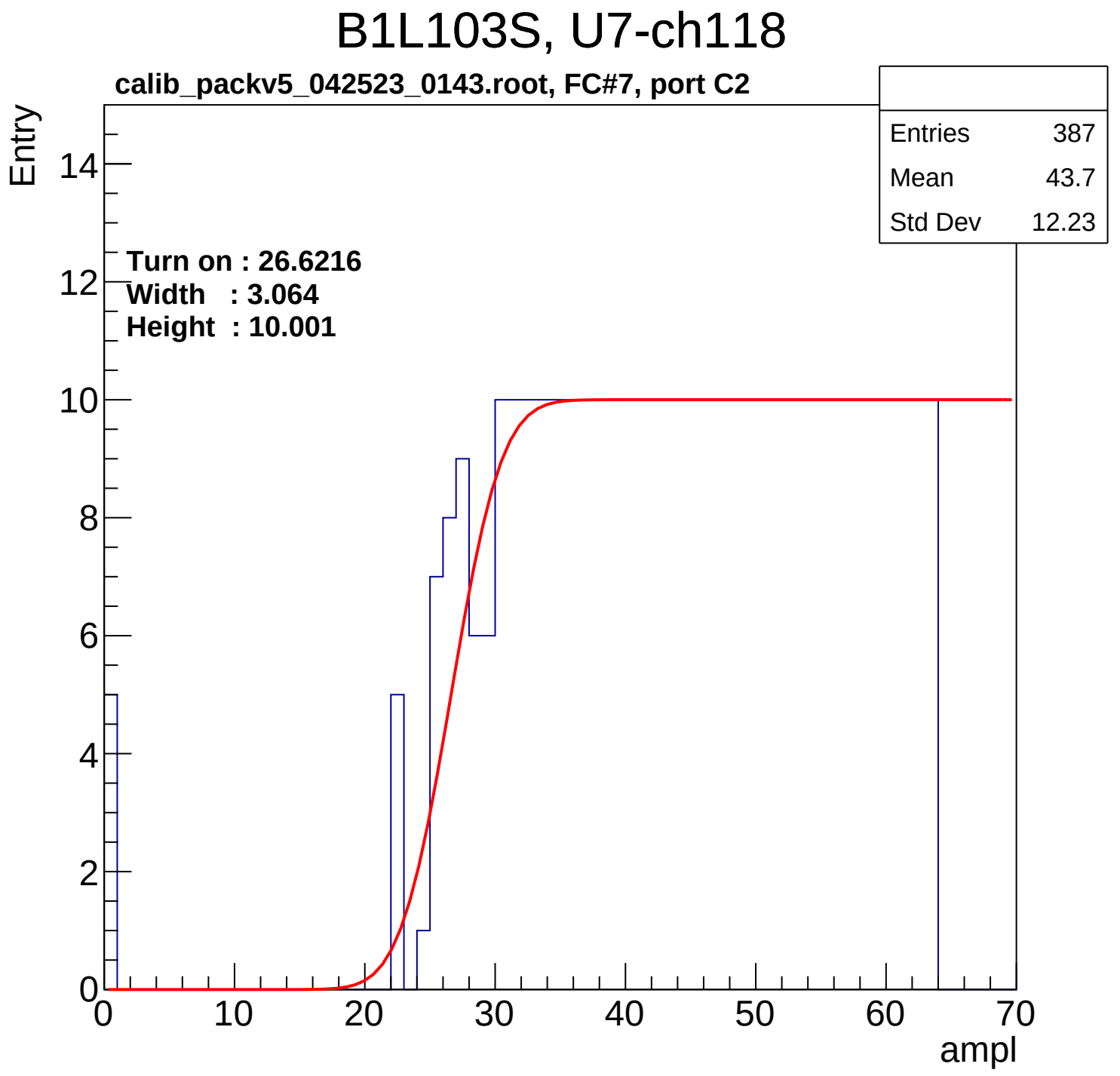
B1L103S, U7-ch118
calib_packv5_042523_0143.root, FC#7, port C2
Entries 387
Mean 43.7
Std Dev 12.23
Turn on : 26.6216
Width : 3.064
Height : 10.001
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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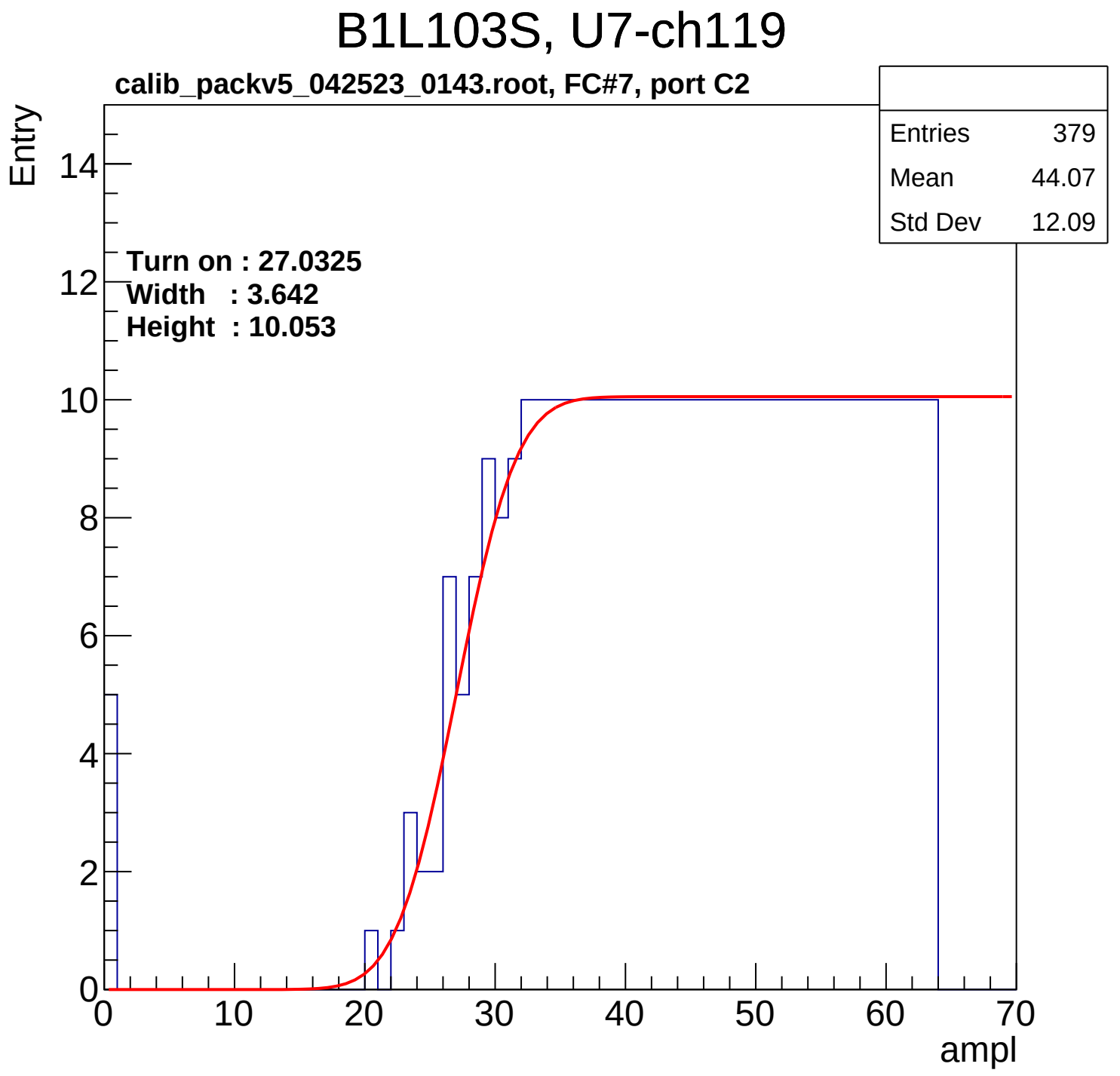
B1L103S, U7-ch119
calib_packv5_042523_0143.root, FC#7, port C2
Entries 379
Mean 44.07
Std Dev 12.09
Turn on : 27.0325
Width : 3.642
Height : 10.053
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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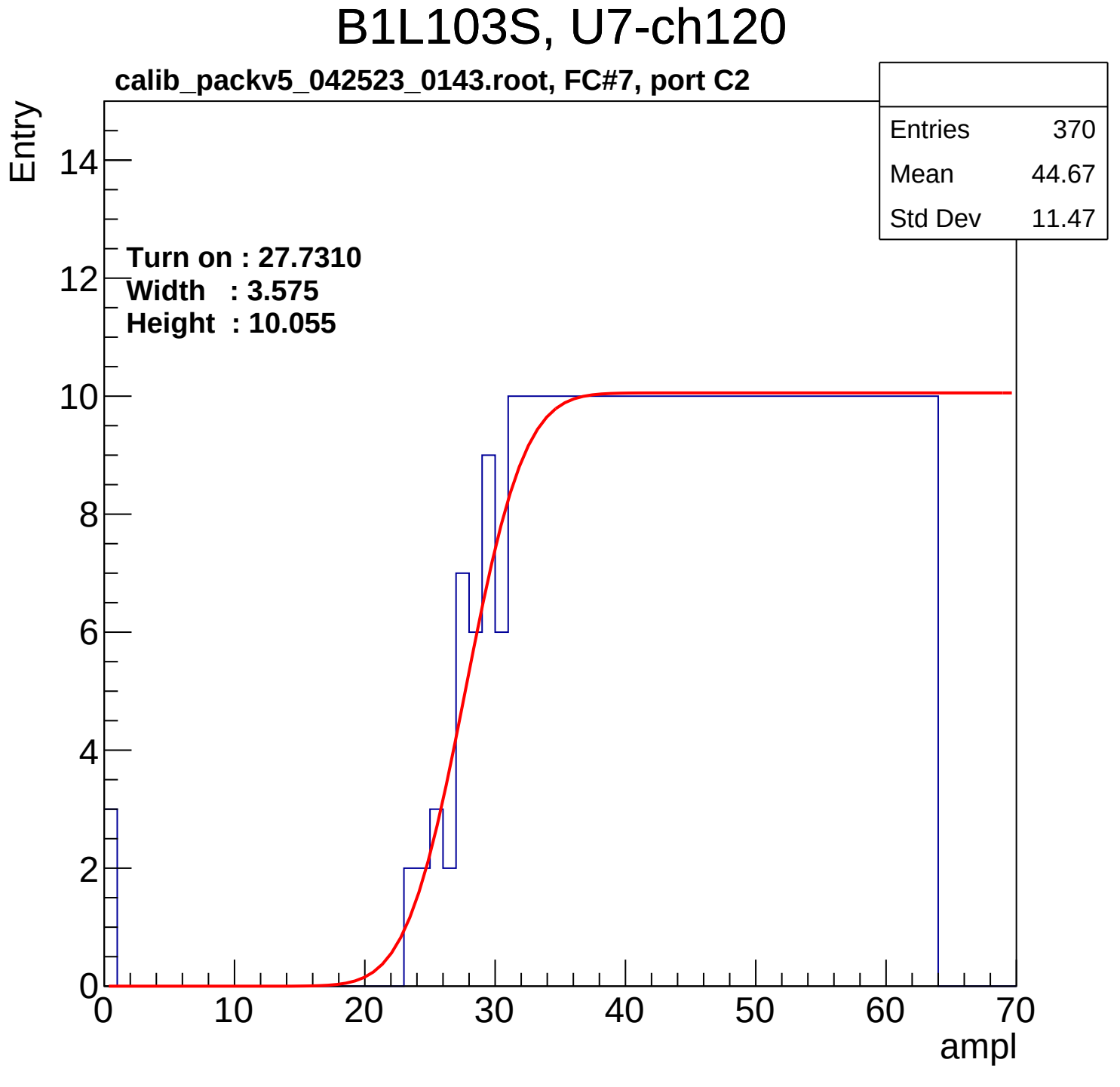
B1L103S, U7-ch120
calib_packv5_042523_0143.root, FC#7, port C2
Entries 370
Mean 44.67
Std Dev 11.47
Turn on : 27.7310
Width : 3.575
Height : 10.055
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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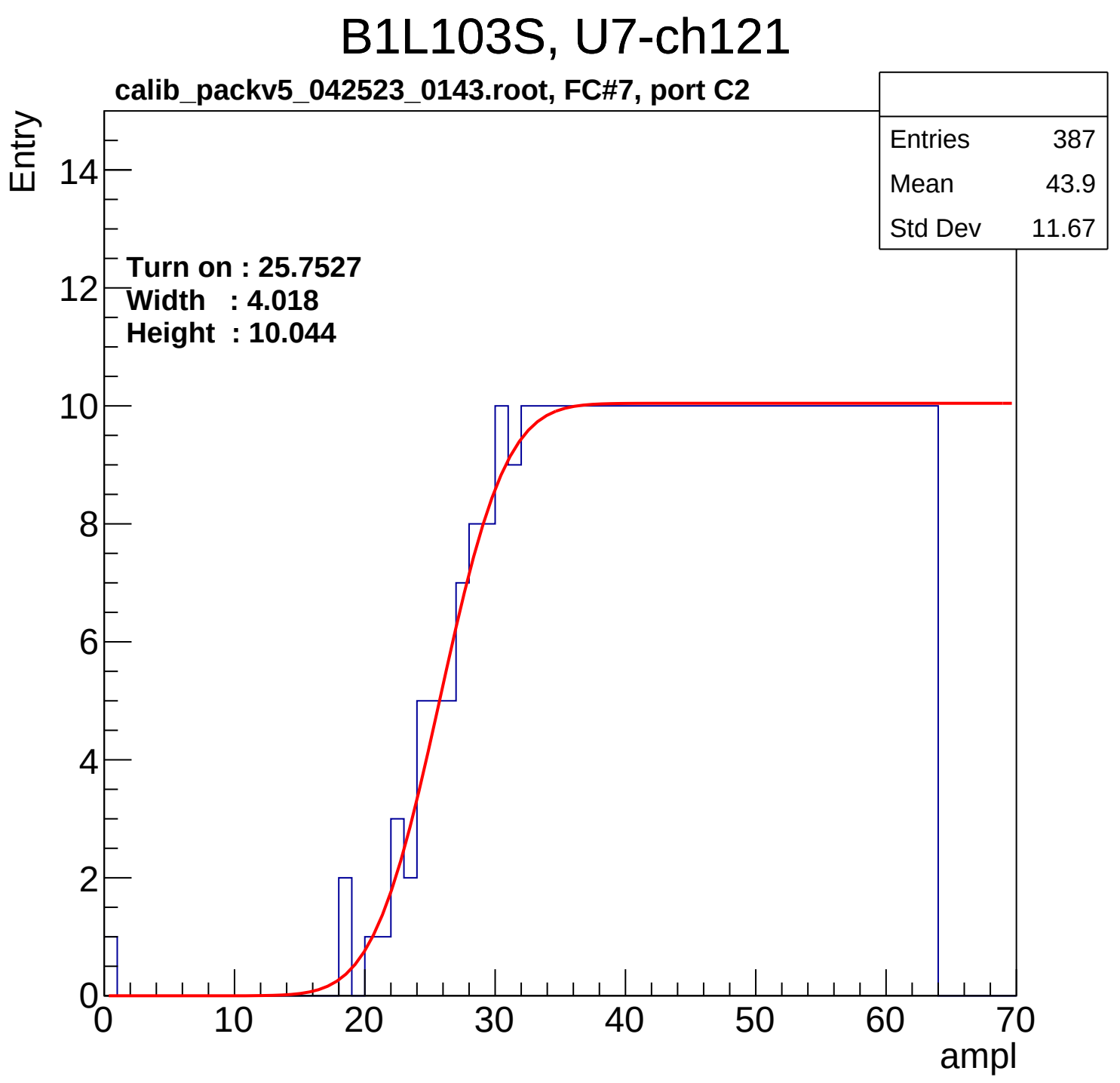
B1L103S, U7-ch121
calib_packv5_042523_0143.root, FC#7, port C2
Entries 387
Mean 43.9
Std Dev 11.67
Turn on : 25.7527
Width : 4.018
Height : 10.044
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
50
60
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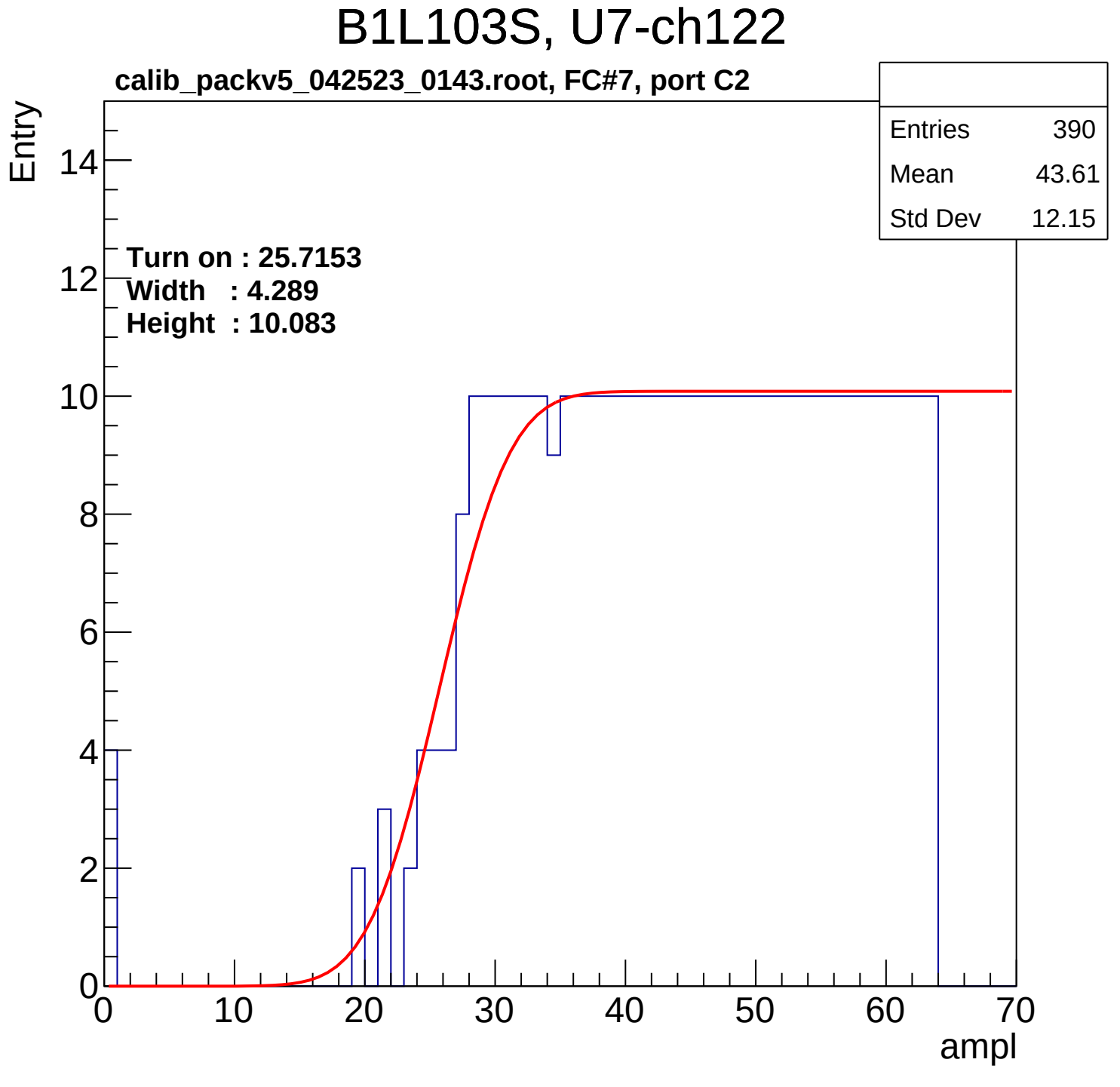
B1L103S, U7-ch122
calib_packv5_042523_0143.root, FC#7, port C2
Entries 390
Mean 43.61
Std Dev 12.15
Turn on : 25.7153
Width : 4.289
Height : 10.083
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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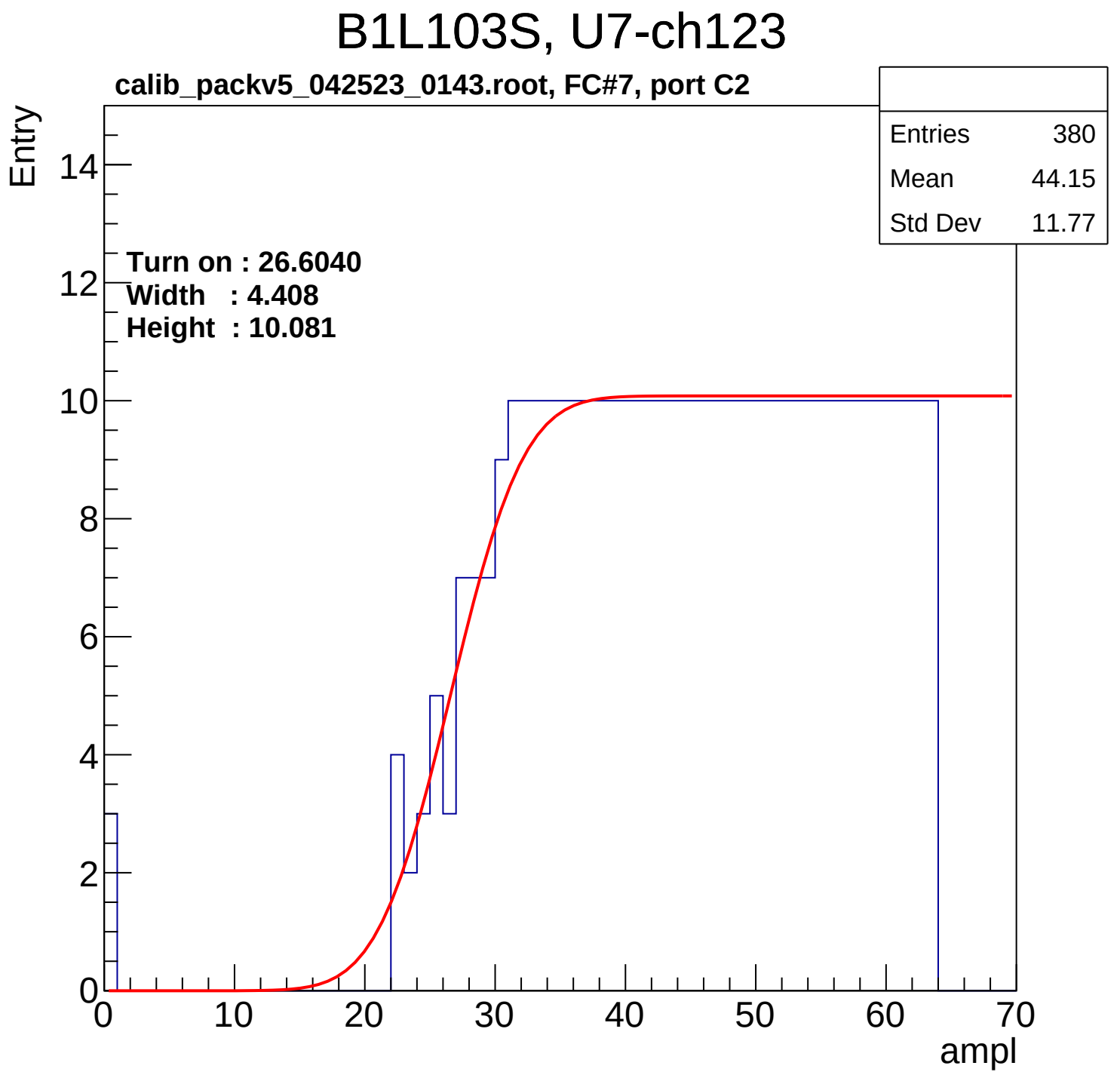
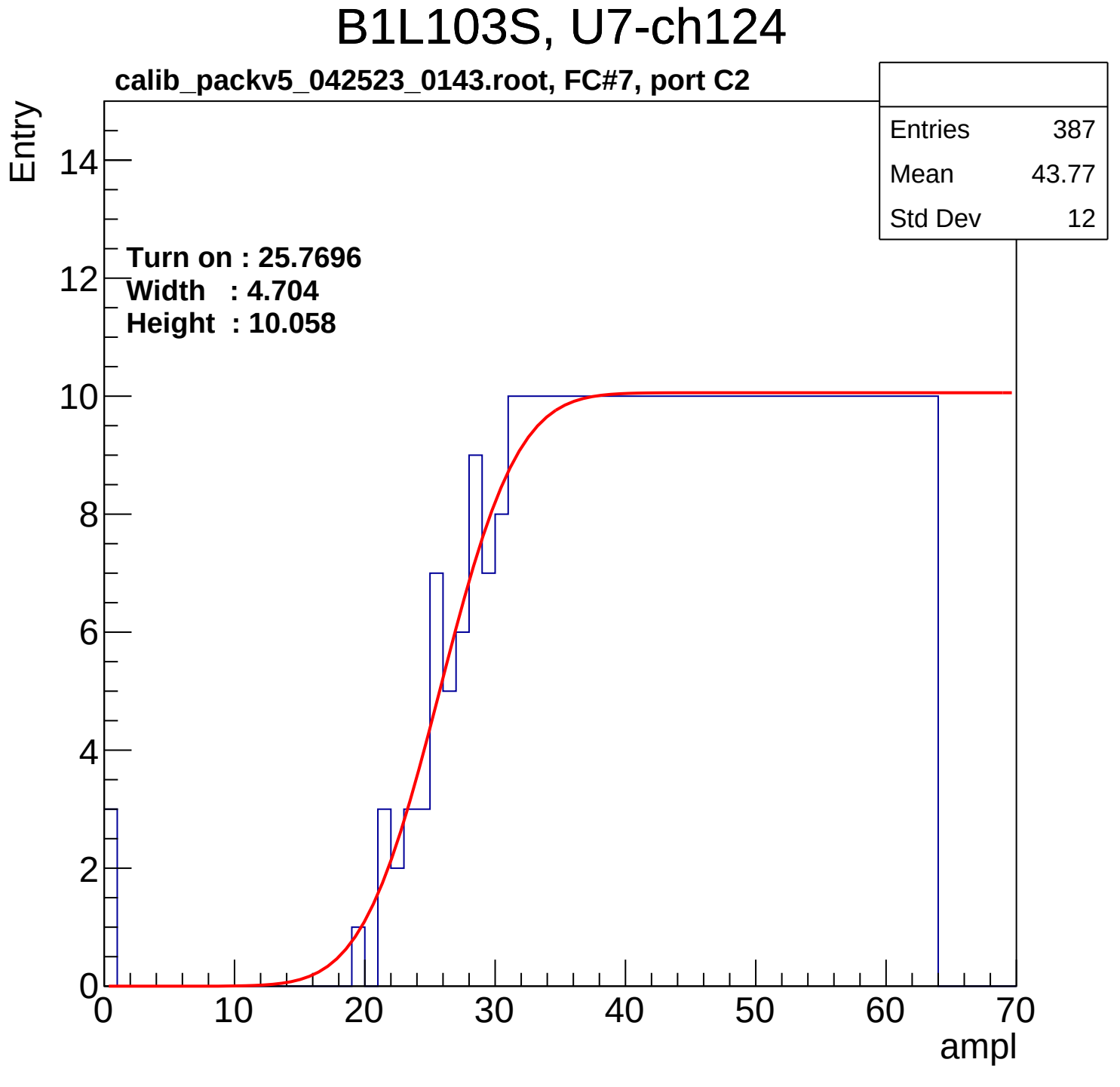

B1L103S, U7-ch123
calib_packv5_042523_0143.root, FC#7, port C2
Entries 380
Mean 44.15
Std Dev 11.77
Turn on : 26.6040
Width : 4.408
Height : 10.081
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U7-ch124
calib_packv5_042523_0143.root, FC#7, port C2
Entries 387
Mean 43.77
Std Dev 12
Turn on : 25.7696
Width : 4.704
Height : 10.058
Entry
ampl
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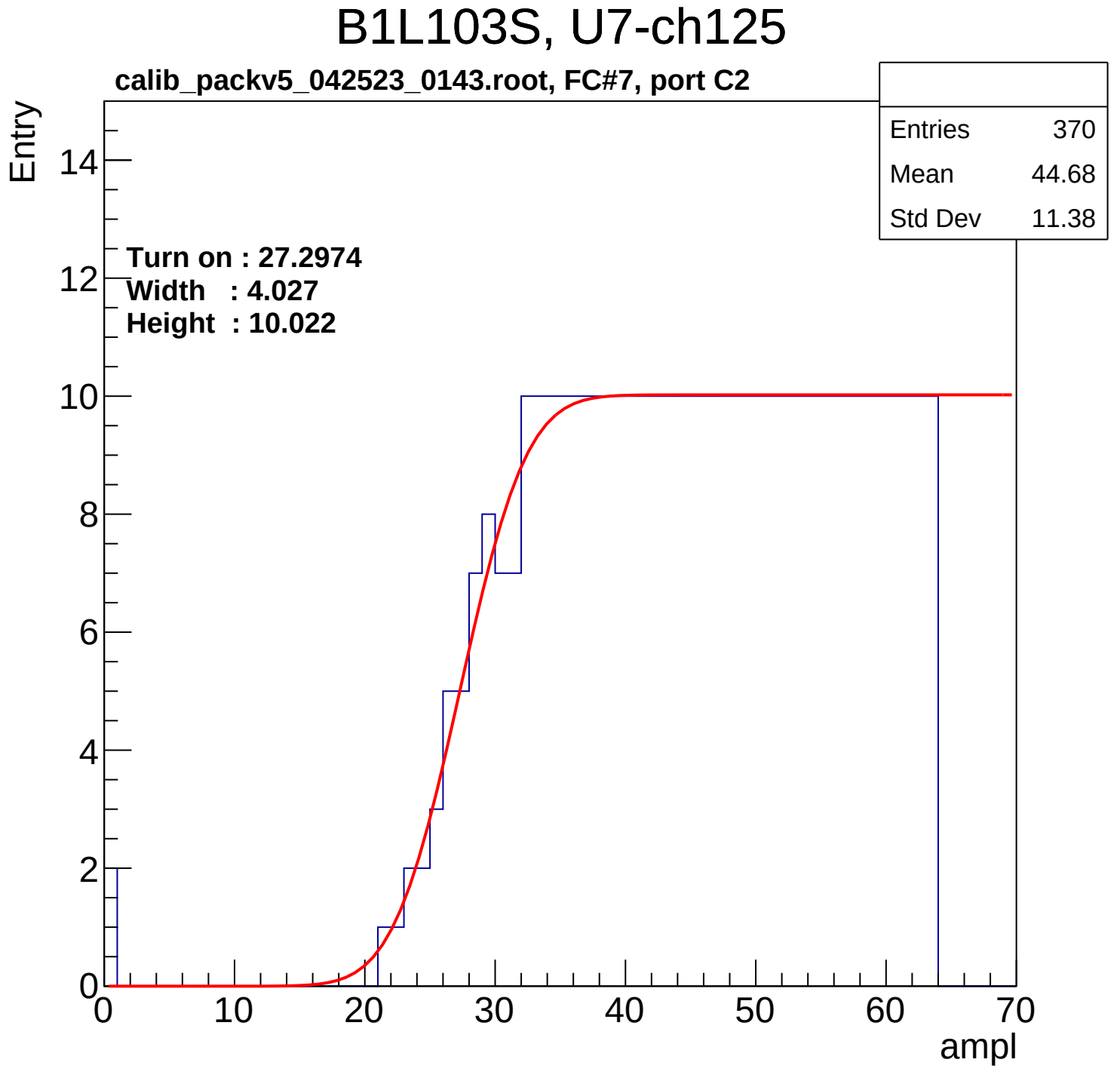
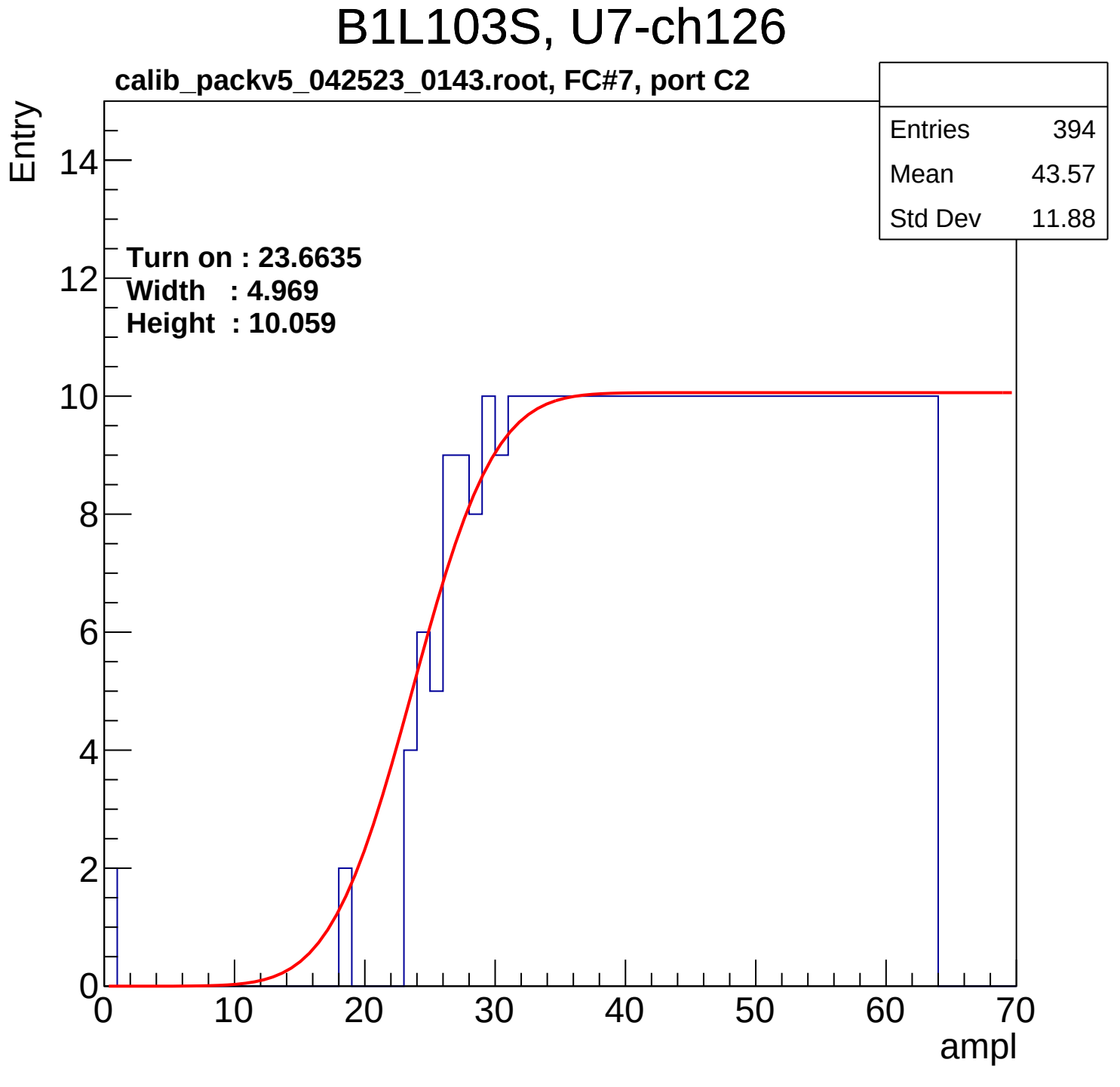
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U7-ch125
calib_packv5_042523_0143.root, FC#7, port C2
Entries 370
Mean 44.68
Std Dev 11.38
Turn on : 27.2974
Width : 4.027
Height : 10.022
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U7-ch126
calib_packv5_042523_0143.root, FC#7, port C2
Entries 394
Mean 43.57
Std Dev 11.88
Turn on : 23.6635
Width : 4.969
Height : 10.059
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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40
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60
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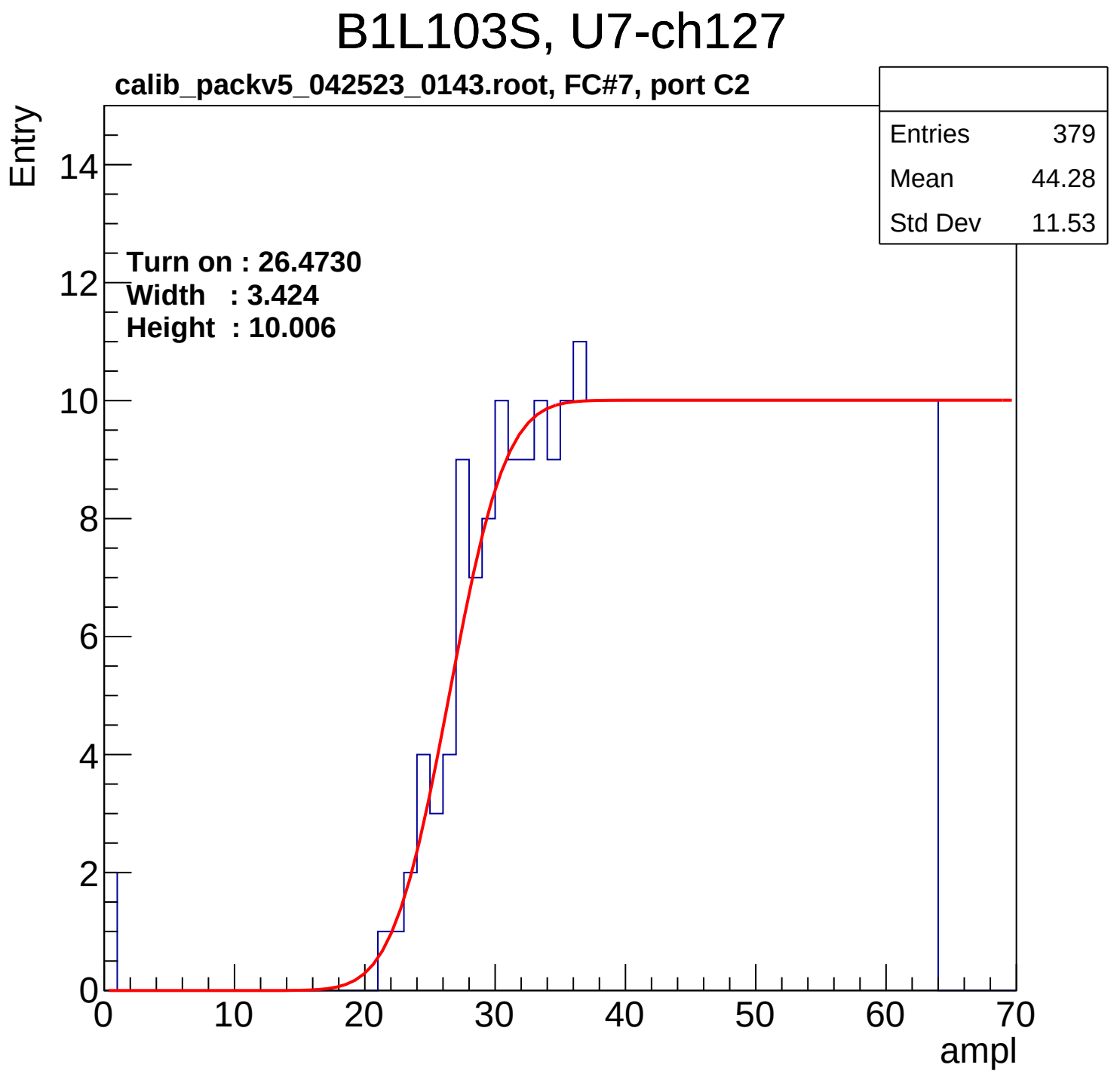
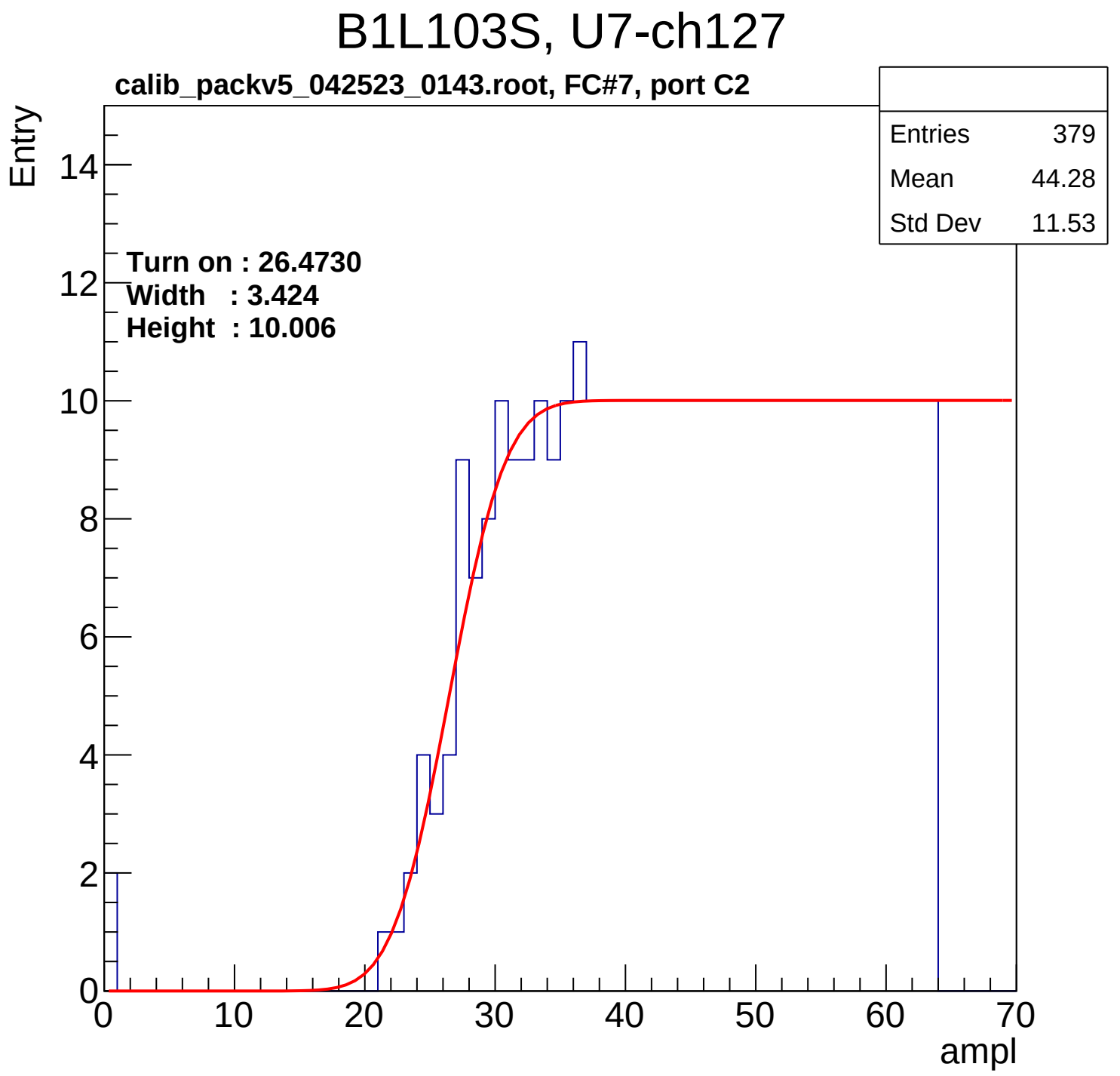

B1L103S, U7-ch127
calib_packv5_042523_0143.root, FC#7, port C2
Entries 379
Mean 44.28
Std Dev 11.53
Turn on : 26.4730
Width : 3.424
Height : 10.006
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U7-ch127
calib_packv5_042523_0143.root, FC#7, port C2
Entries 379
Mean 44.28
Std Dev 11.53
Turn on : 26.4730
Width : 3.424
Height : 10.006
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70