

B0L103S, U12-ch0

calib_packv5_040323_1717.root, FC#2, port C3

Entries	137
Mean	55.66
Std Dev	8.031

Turn on : 50.8132

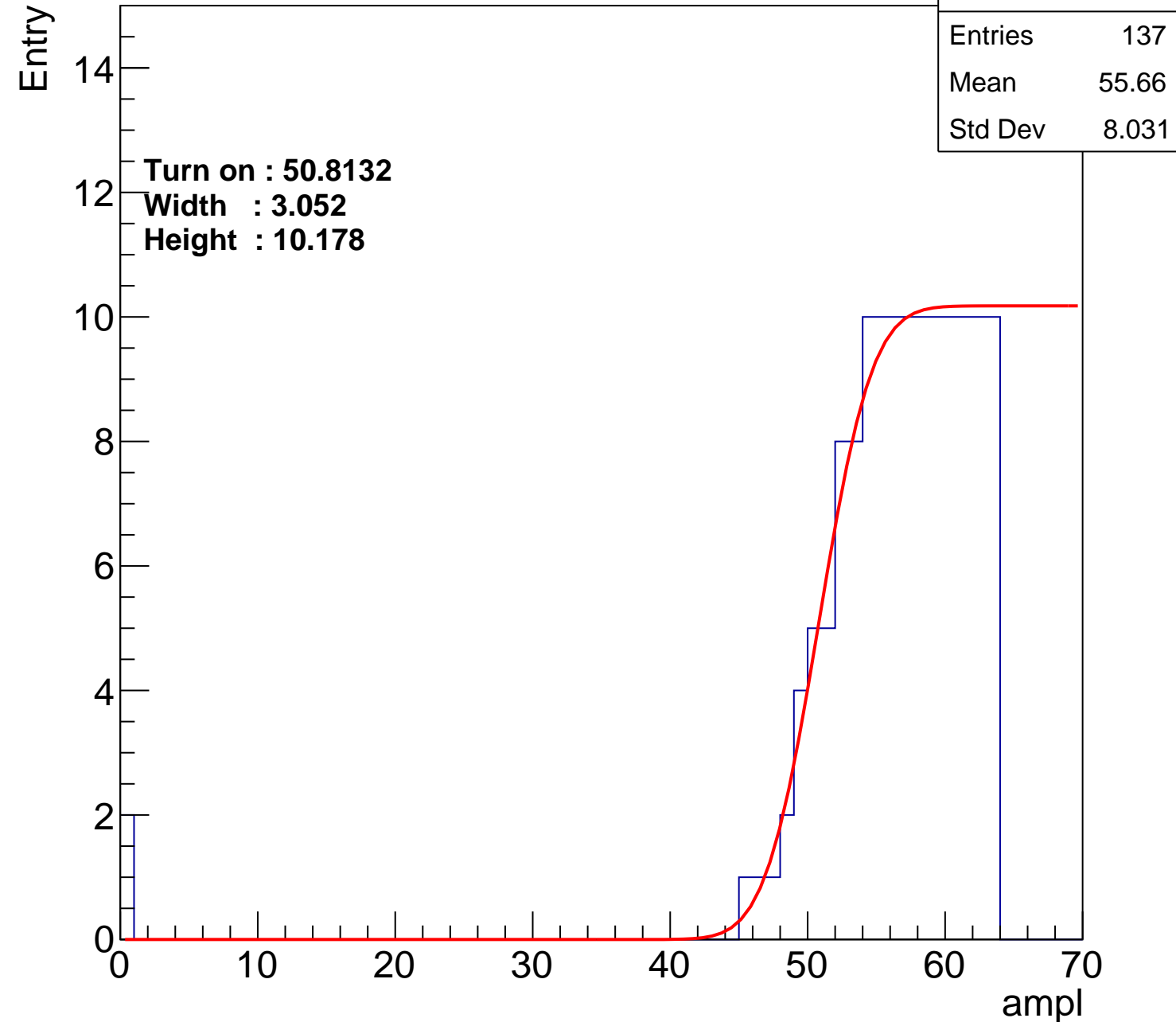
Width : 3.052

Height : 10.178

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch1

calib_packv5_040323_1717.root, FC#2, port C3

Entries	123
Mean	54.92
Std Dev	11.94

Turn on : 52.3866

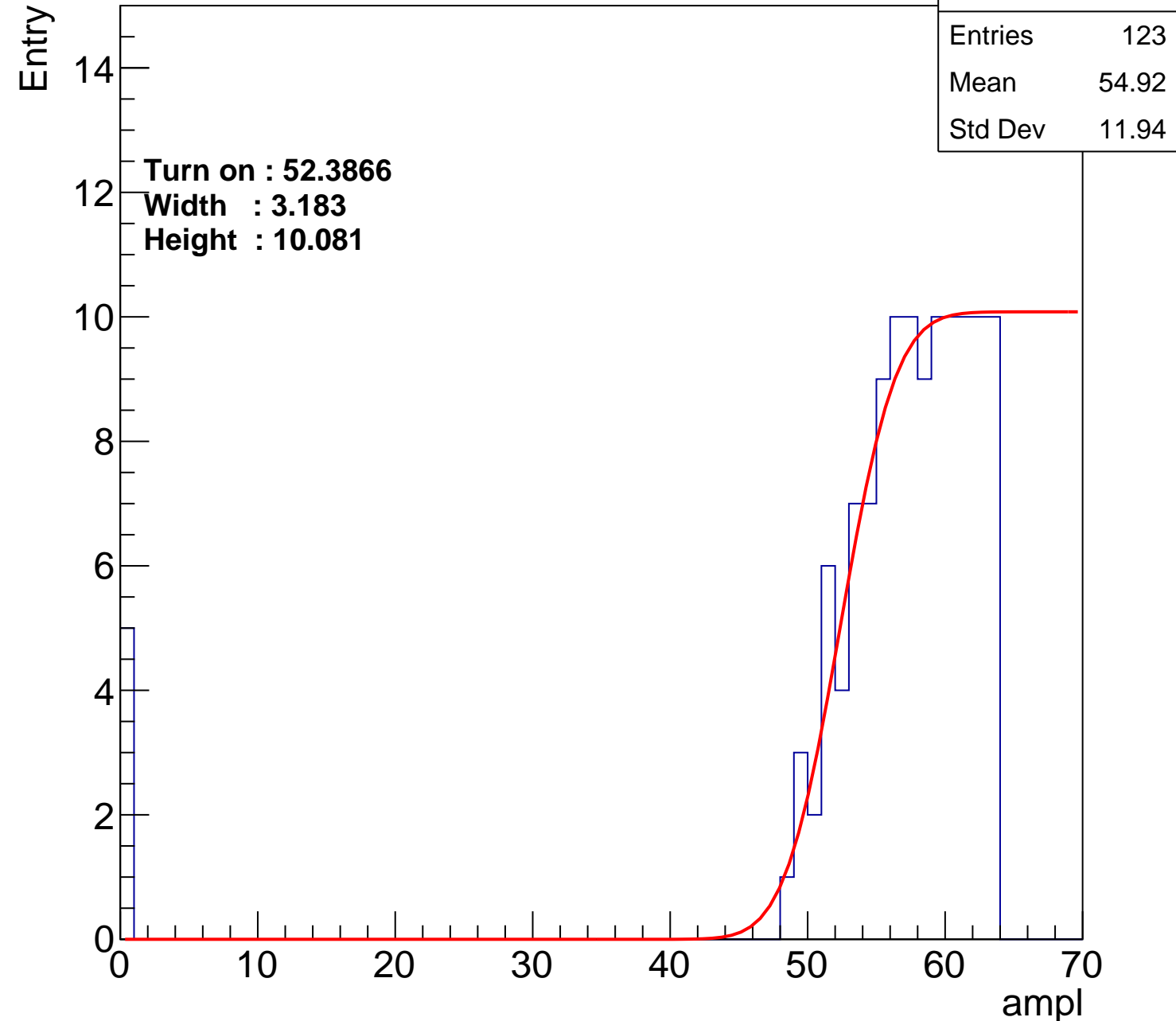
Width : 3.183

Height : 10.081

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch2

calib_packv5_040323_1717.root, FC#2, port C3

Entries	135
Mean	55.56
Std Dev	8.06

Turn on : 49.9013

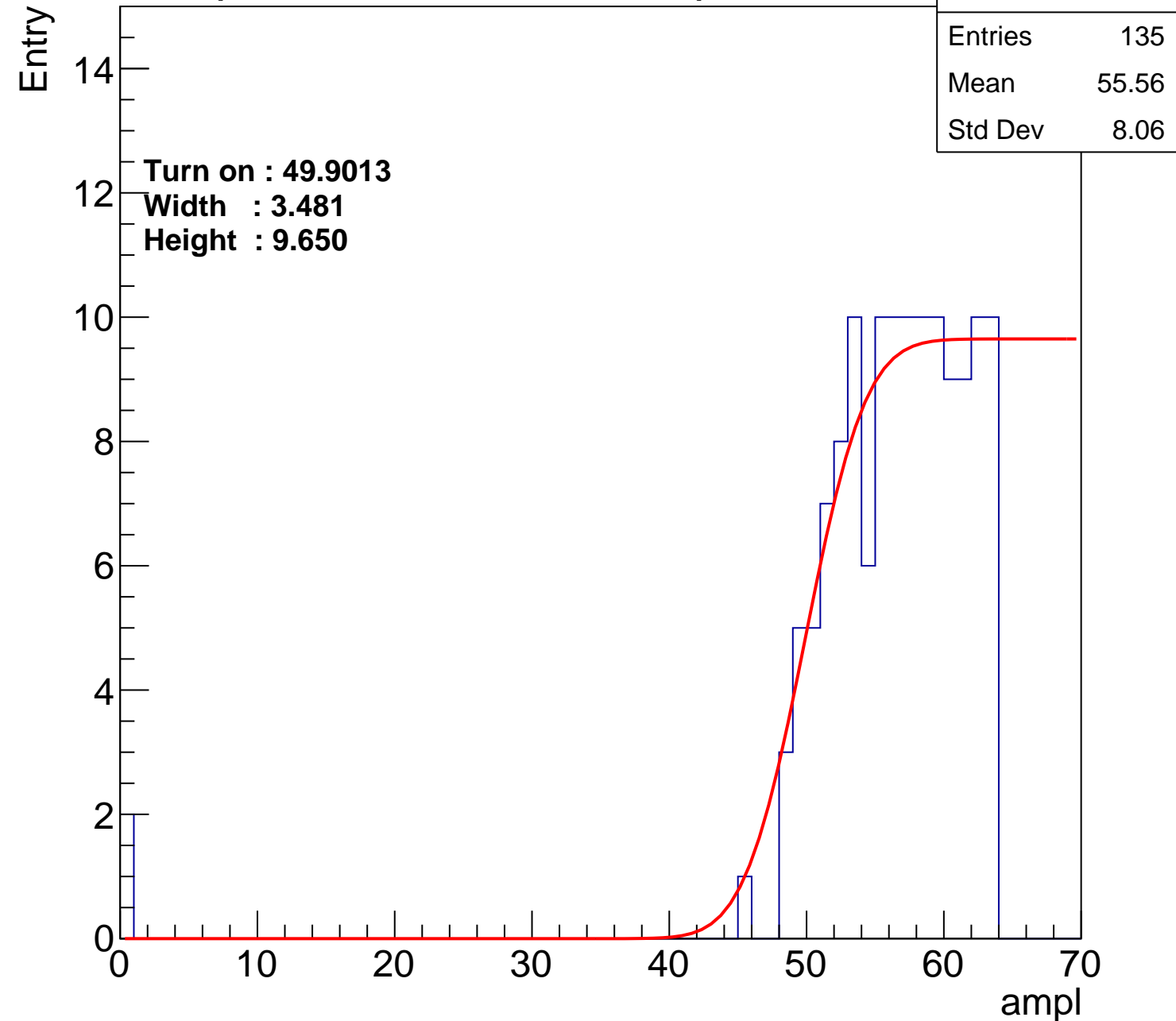
Width : 3.481

Height : 9.650

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch3

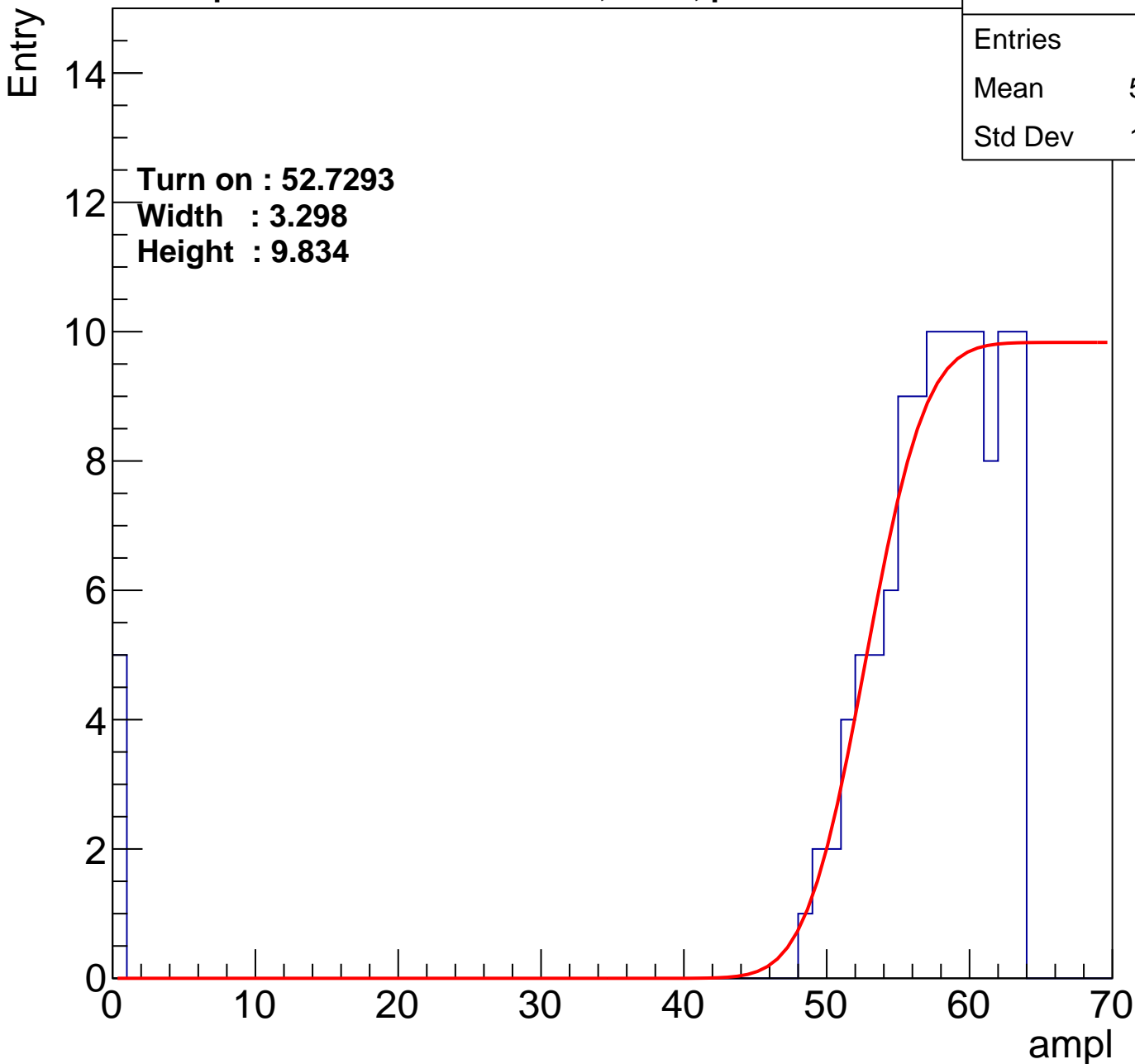
calib_packv5_040323_1717.root, FC#2, port C3

Entries	116
Mean	54.97
Std Dev	12.25

Turn on : 52.7293

Width : 3.298

Height : 9.834



B0L103S, U12-ch4

calib_packv5_040323_1717.root, FC#2, port C3

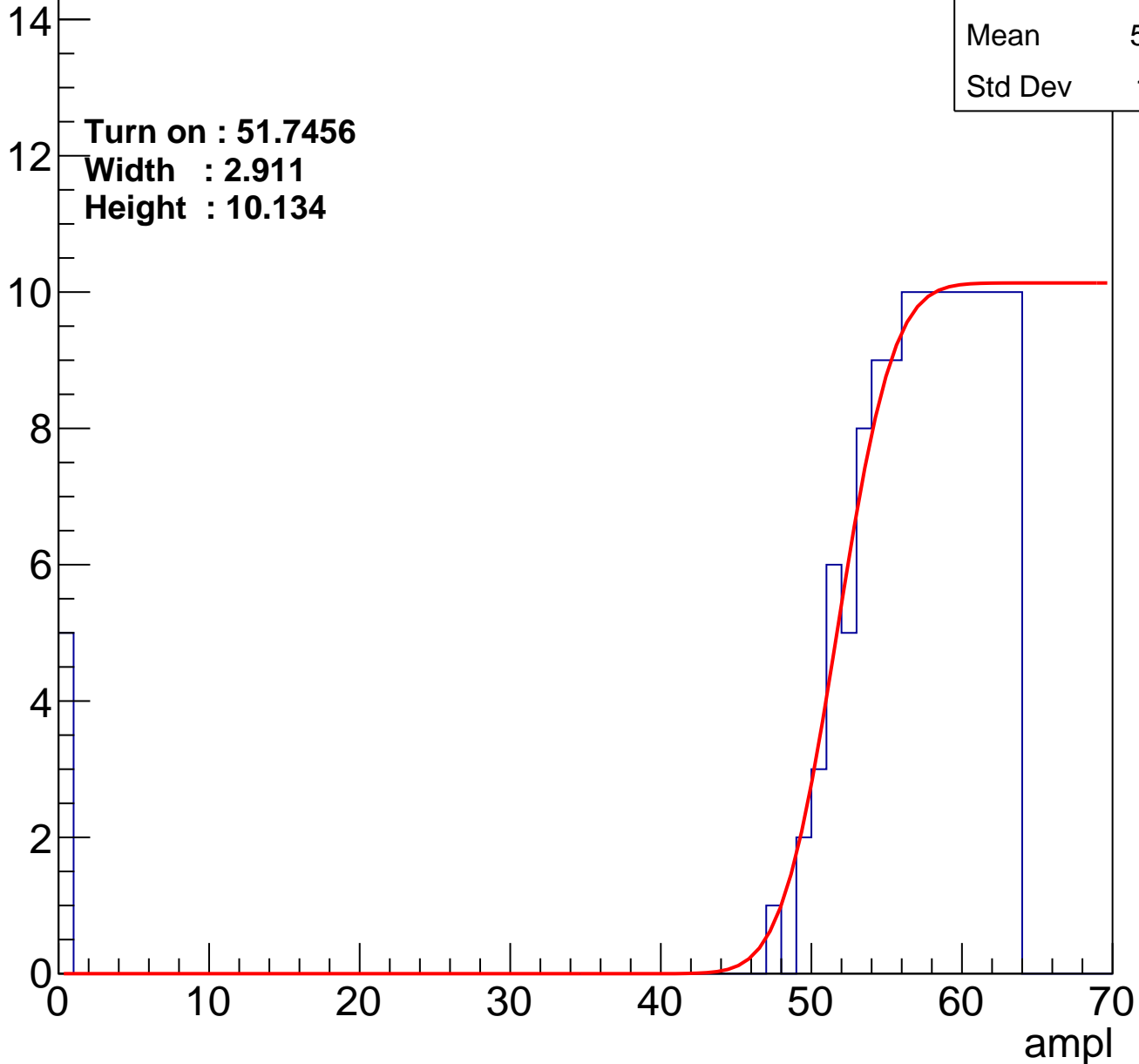
Entries	128
Mean	54.89
Std Dev	11.71

Turn on : 51.7456

Width : 2.911

Height : 10.134

Entry



B0L103S, U12-ch5

calib_packv5_040323_1717.root, FC#2, port C3

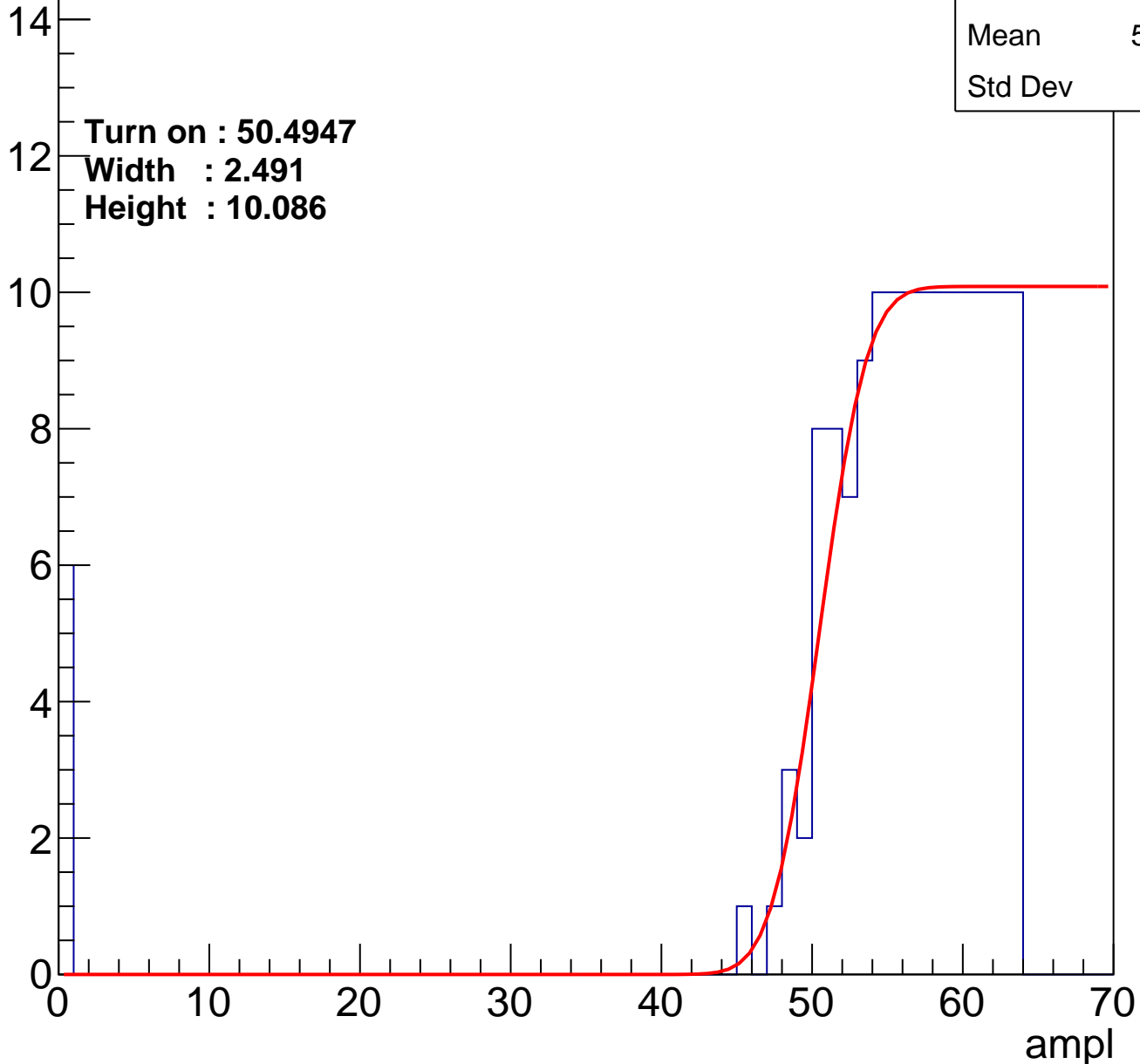
Entries	145
Mean	54.02
Std Dev	12

Turn on : 50.4947

Width : 2.491

Height : 10.086

Entry



B0L103S, U12-ch6

calib_packv5_040323_1717.root, FC#2, port C3

Entries	125
Mean	55.34
Std Dev	10.8

Turn on : 53.2237

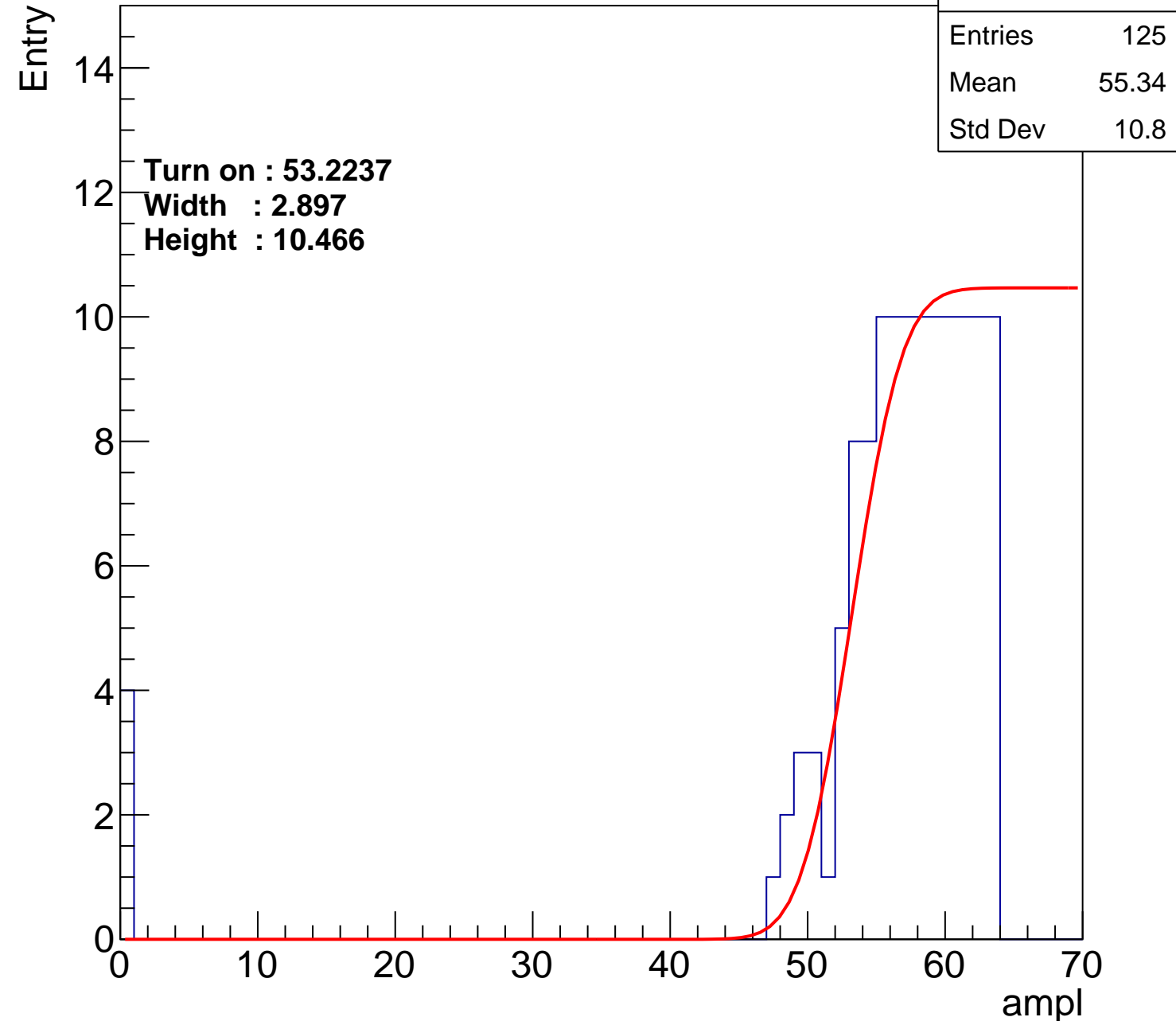
Width : 2.897

Height : 10.466

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch7

calib_packv5_040323_1717.root, FC#2, port C3

Entries	109
Mean	56.82
Std Dev	8.492

Turn on : 53.0474

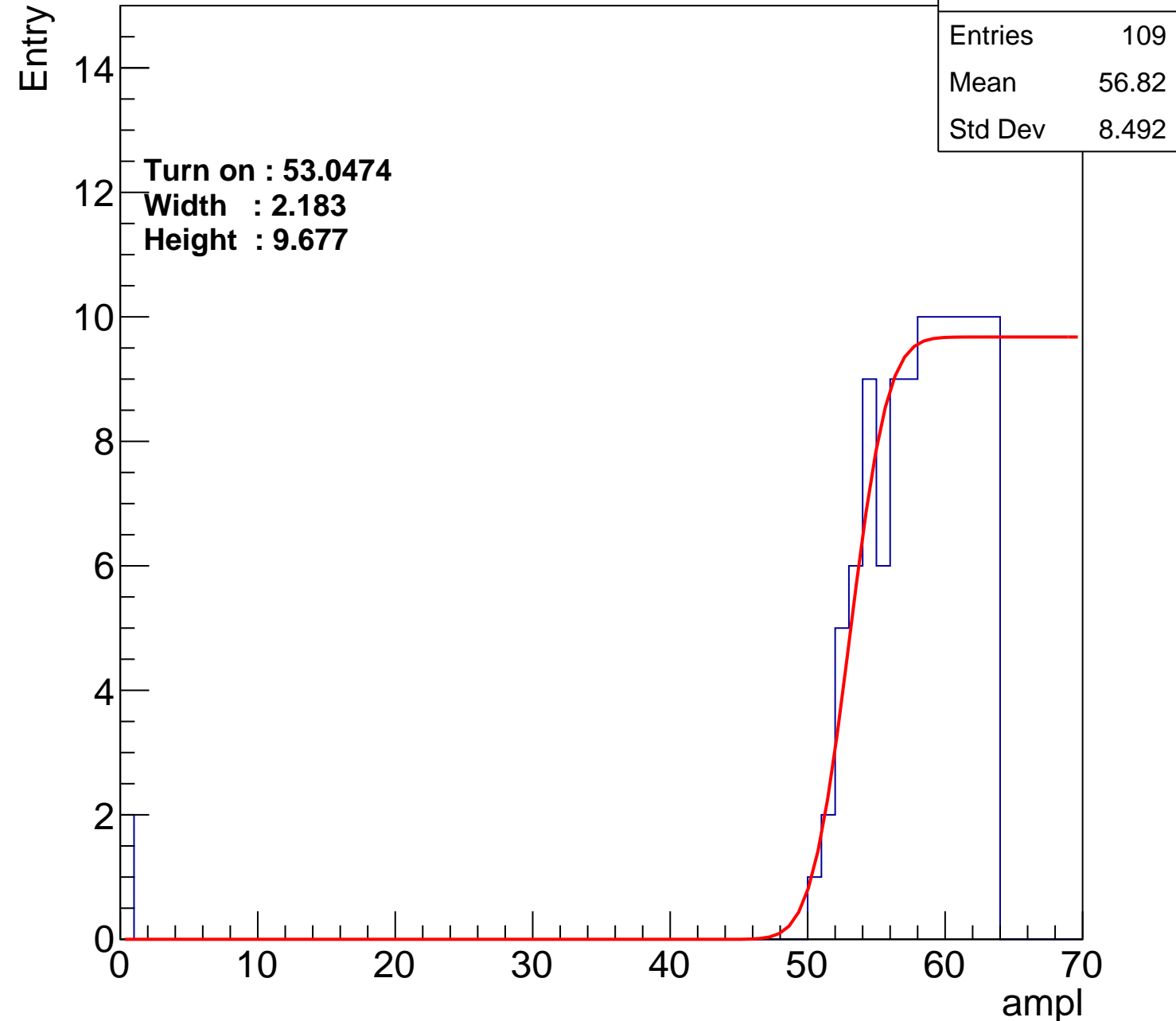
Width : 2.183

Height : 9.677

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch8

calib_packv5_040323_1717.root, FC#2, port C3

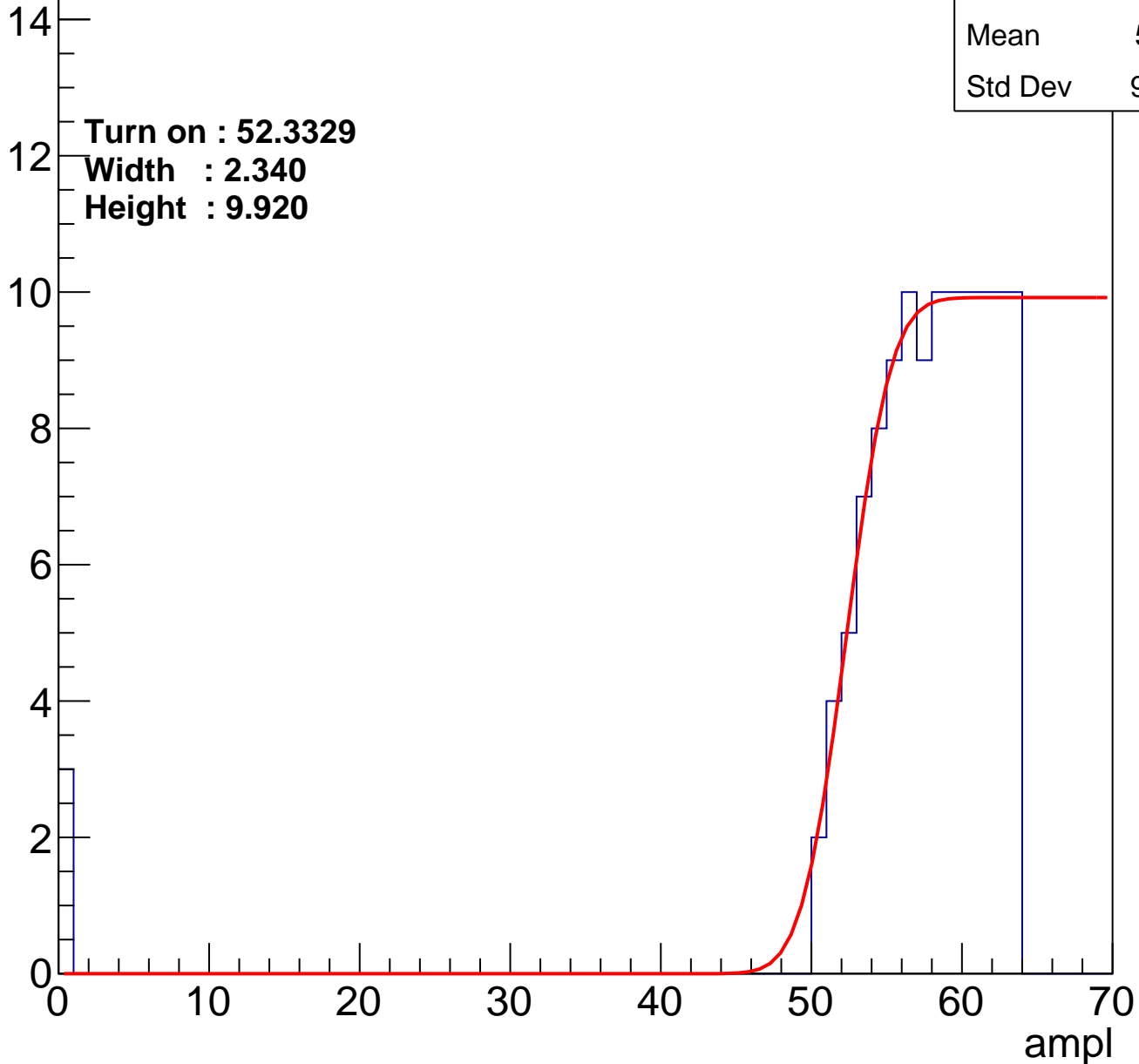
Entries	117
Mean	56.11
Std Dev	9.767

Turn on : 52.3329

Width : 2.340

Height : 9.920

Entry



B0L103S, U12-ch9

calib_packv5_040323_1717.root, FC#2, port C3

Entries	120
Mean	55.36
Std Dev	11.01

Turn on : 52.7964

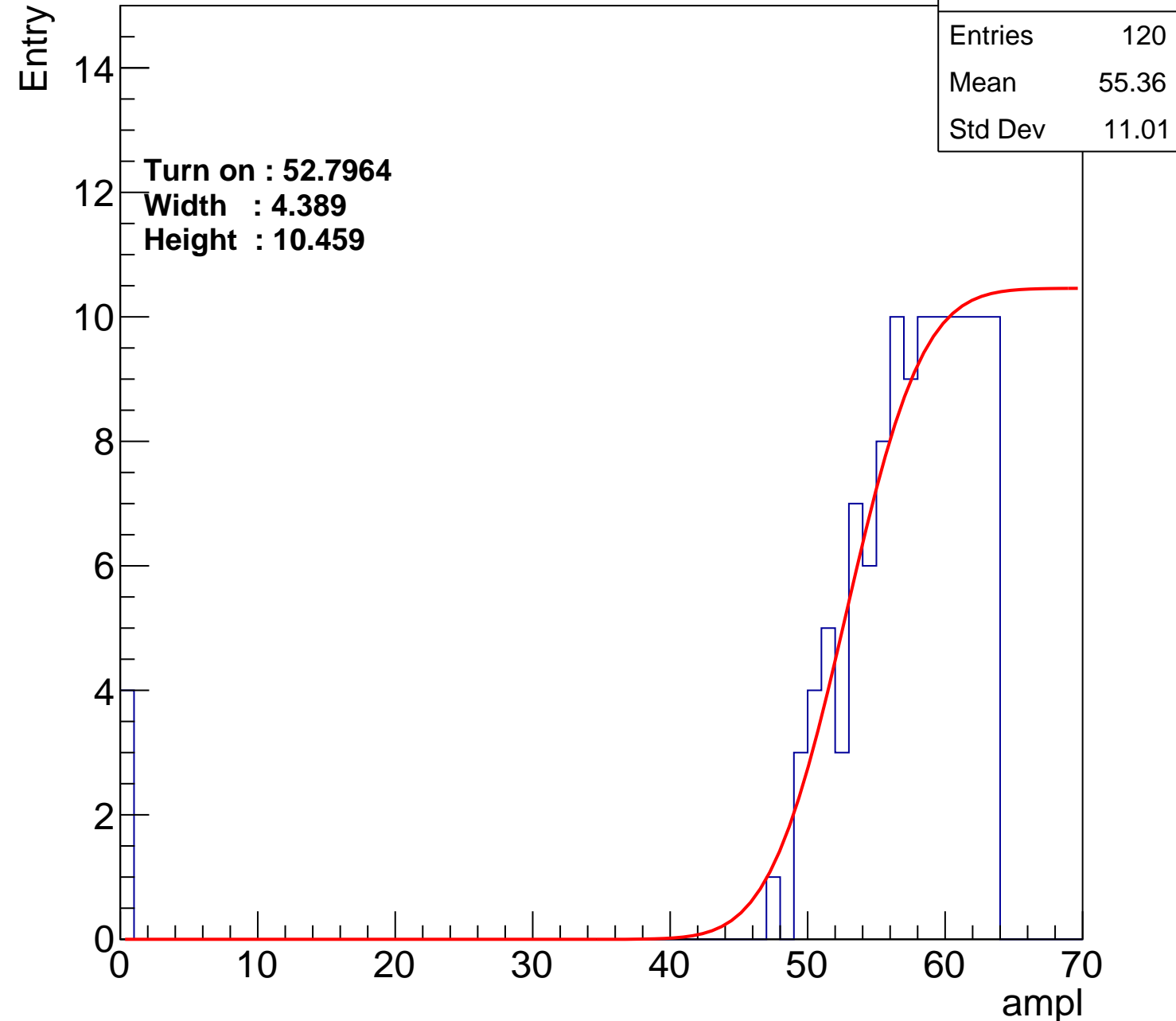
Width : 4.389

Height : 10.459

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch10

calib_packv5_040323_1717.root, FC#2, port C3

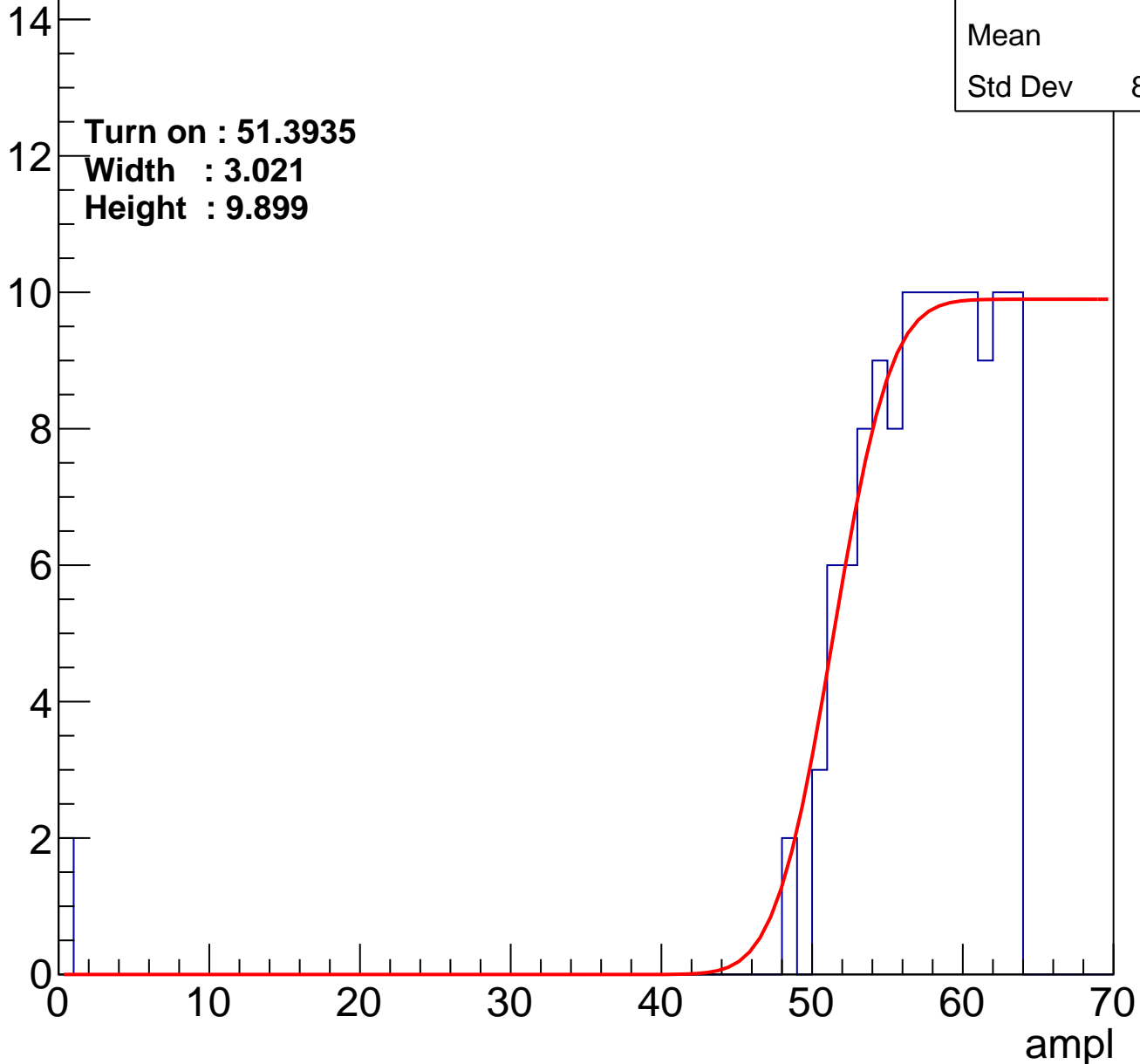
Entries	123
Mean	56.2
Std Dev	8.185

Turn on : 51.3935

Width : 3.021

Height : 9.899

Entry



B0L103S, U12-ch11

calib_packv5_040323_1717.root, FC#2, port C3

Entries	100
Mean	57.52
Std Dev	6.697

Turn on : 54.1939

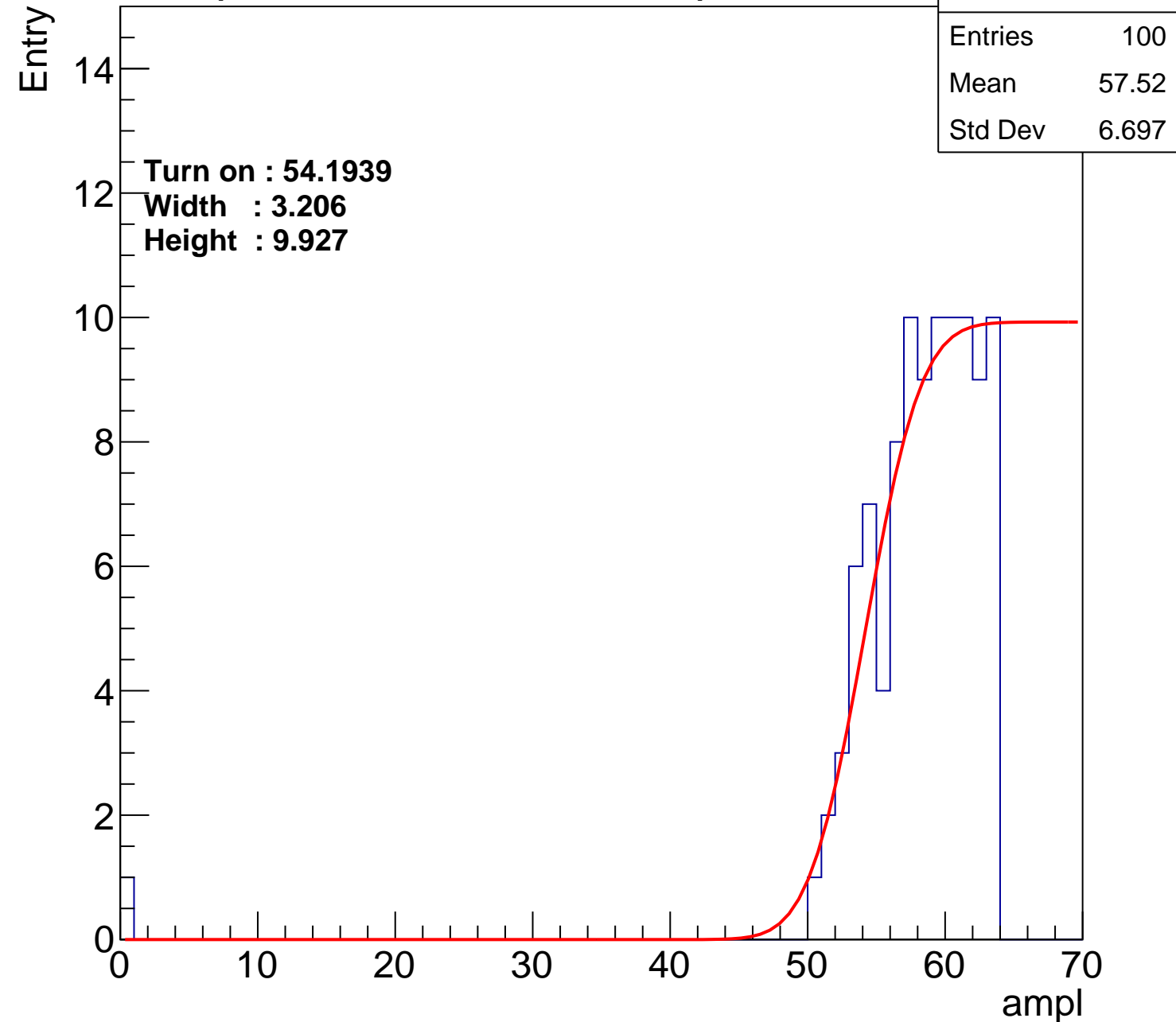
Width : 3.206

Height : 9.927

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch12

calib_packv5_040323_1717.root, FC#2, port C3

Entries	119
Mean	55.43
Std Dev	10.99

Turn on : 52.4338

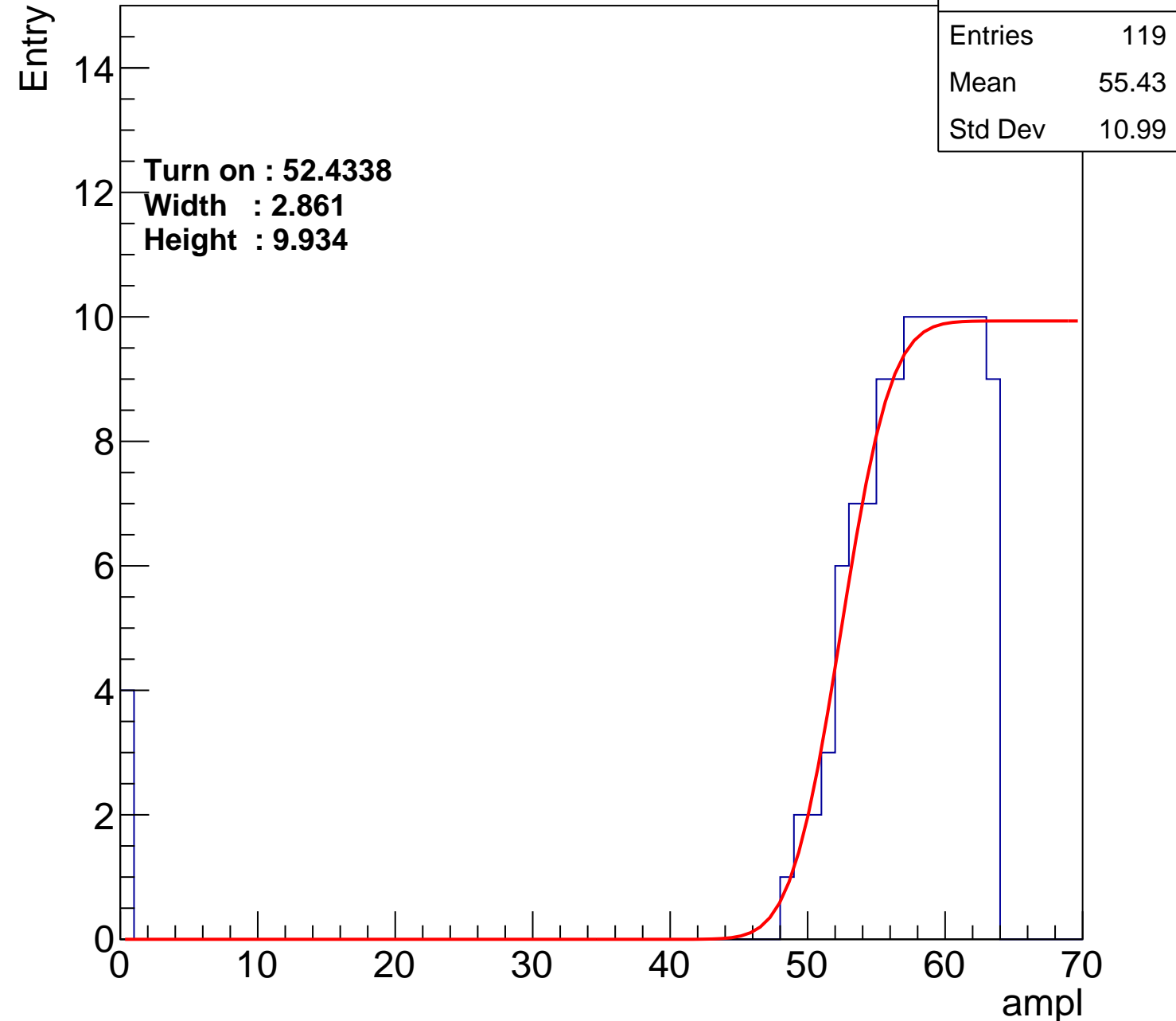
Width : 2.861

Height : 9.934

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch13

calib_packv5_040323_1717.root, FC#2, port C3

Entries	119
Mean	56.27
Std Dev	8.32

Turn on : 51.9881

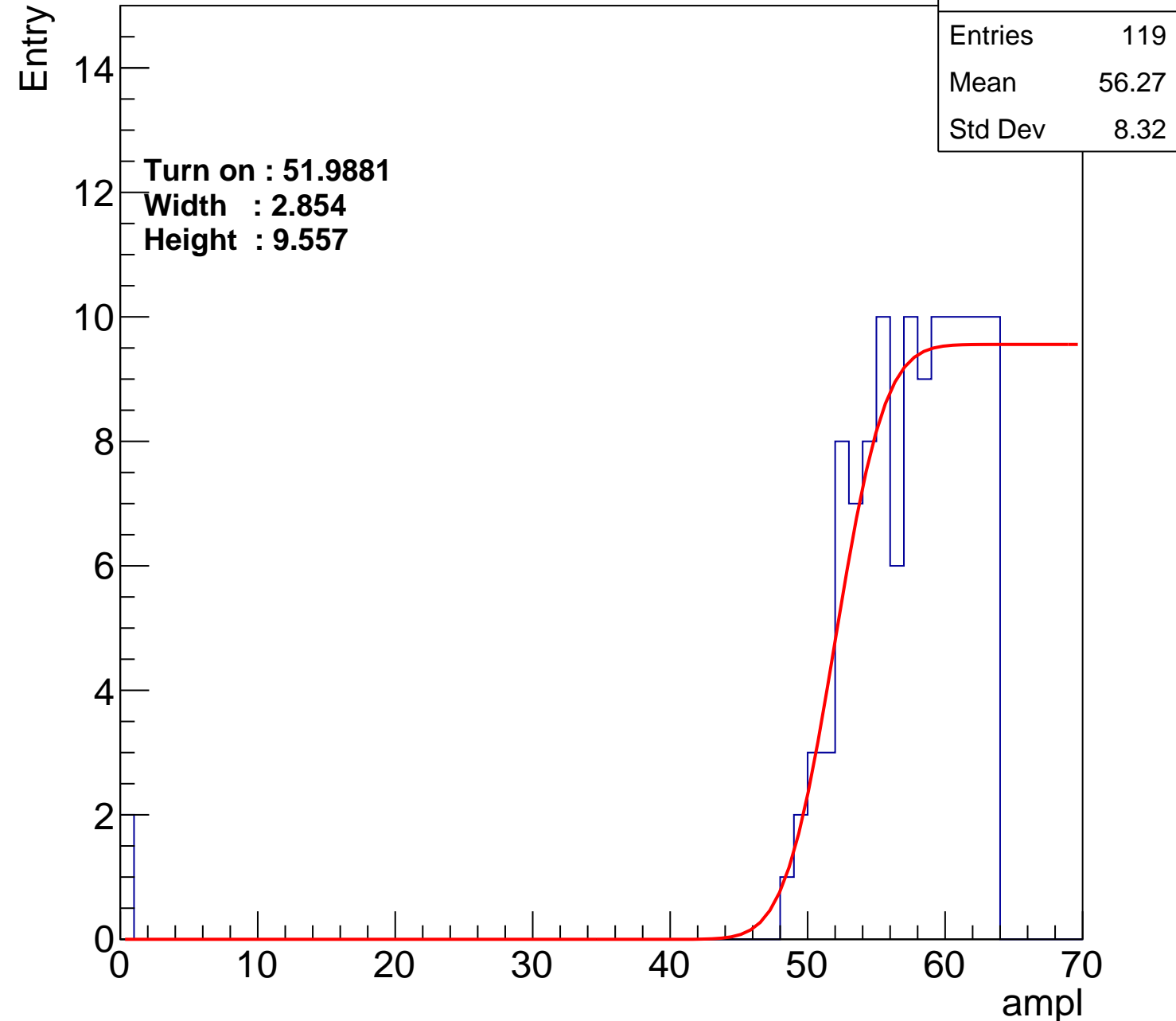
Width : 2.854

Height : 9.557

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch14

calib_packv5_040323_1717.root, FC#2, port C3

Entries	103
Mean	56.81
Std Dev	8.77

Turn on : 54.4366

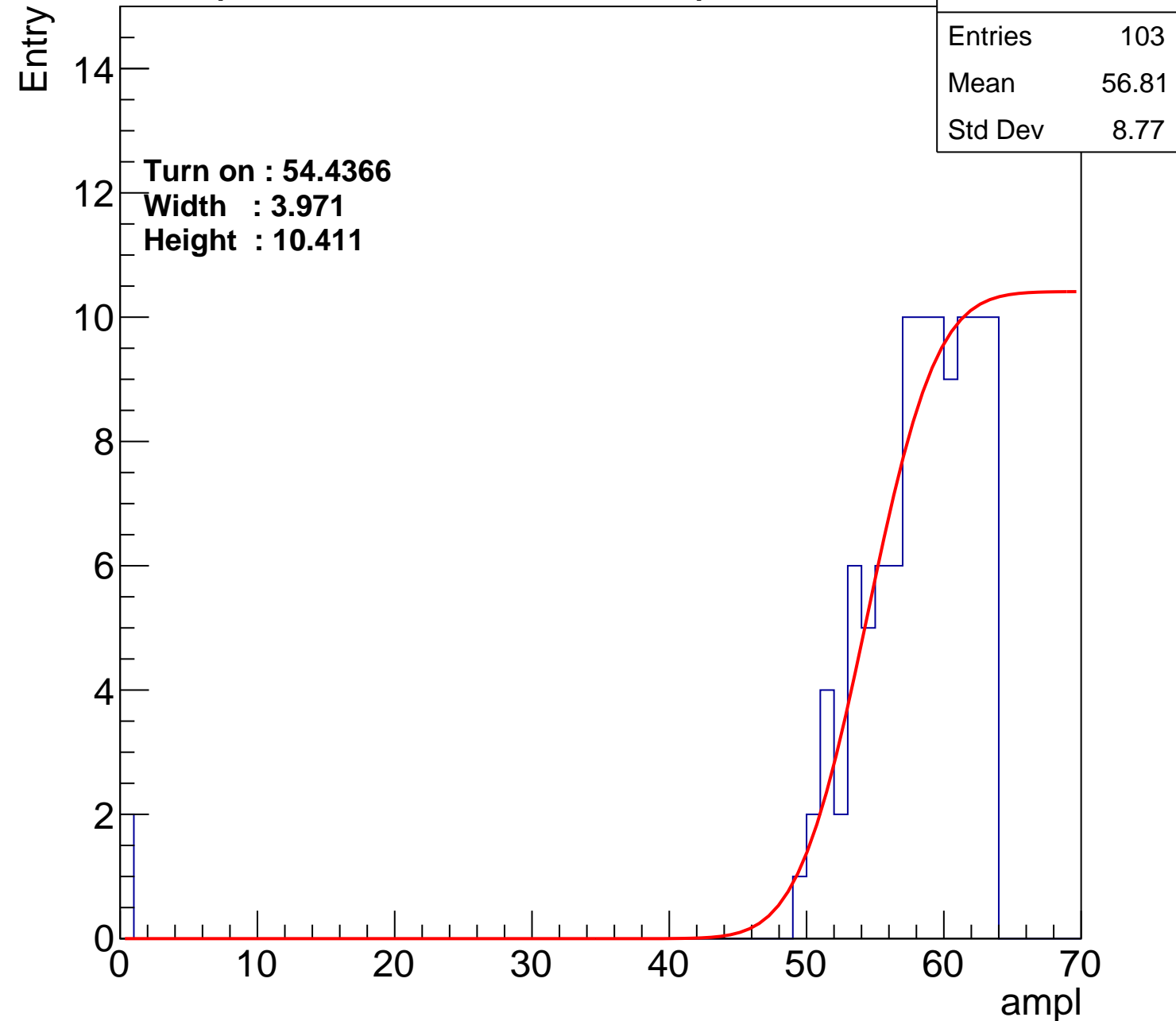
Width : 3.971

Height : 10.411

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch15

calib_packv5_040323_1717.root, FC#2, port C3

Entries	107
Mean	54.81
Std Dev	13.76

Turn on : 54.0008

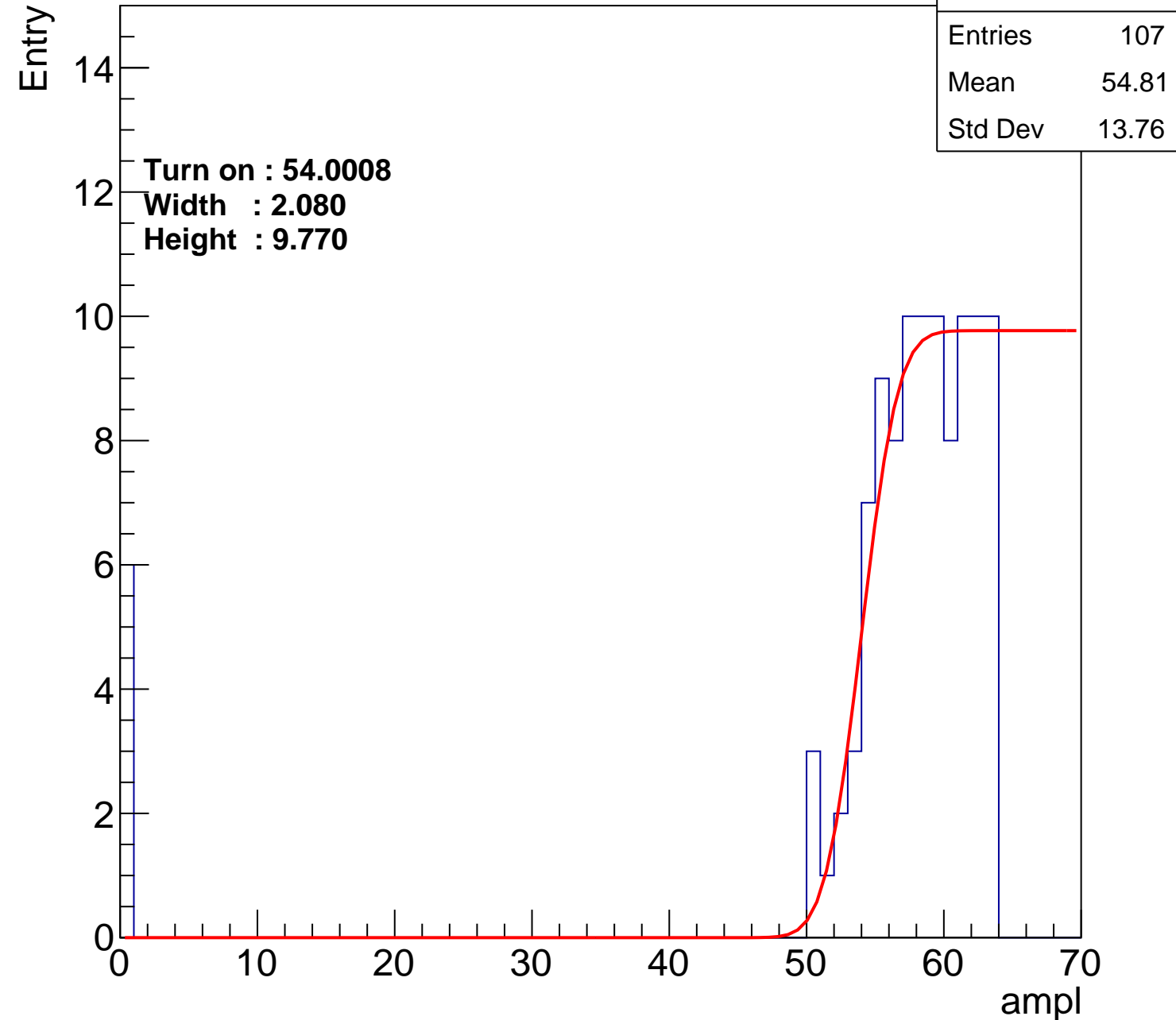
Width : 2.080

Height : 9.770

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch16

calib_packv5_040323_1717.root, FC#2, port C3

Entries	113
Mean	55.75
Std Dev	11.24

Turn on : 53.6496

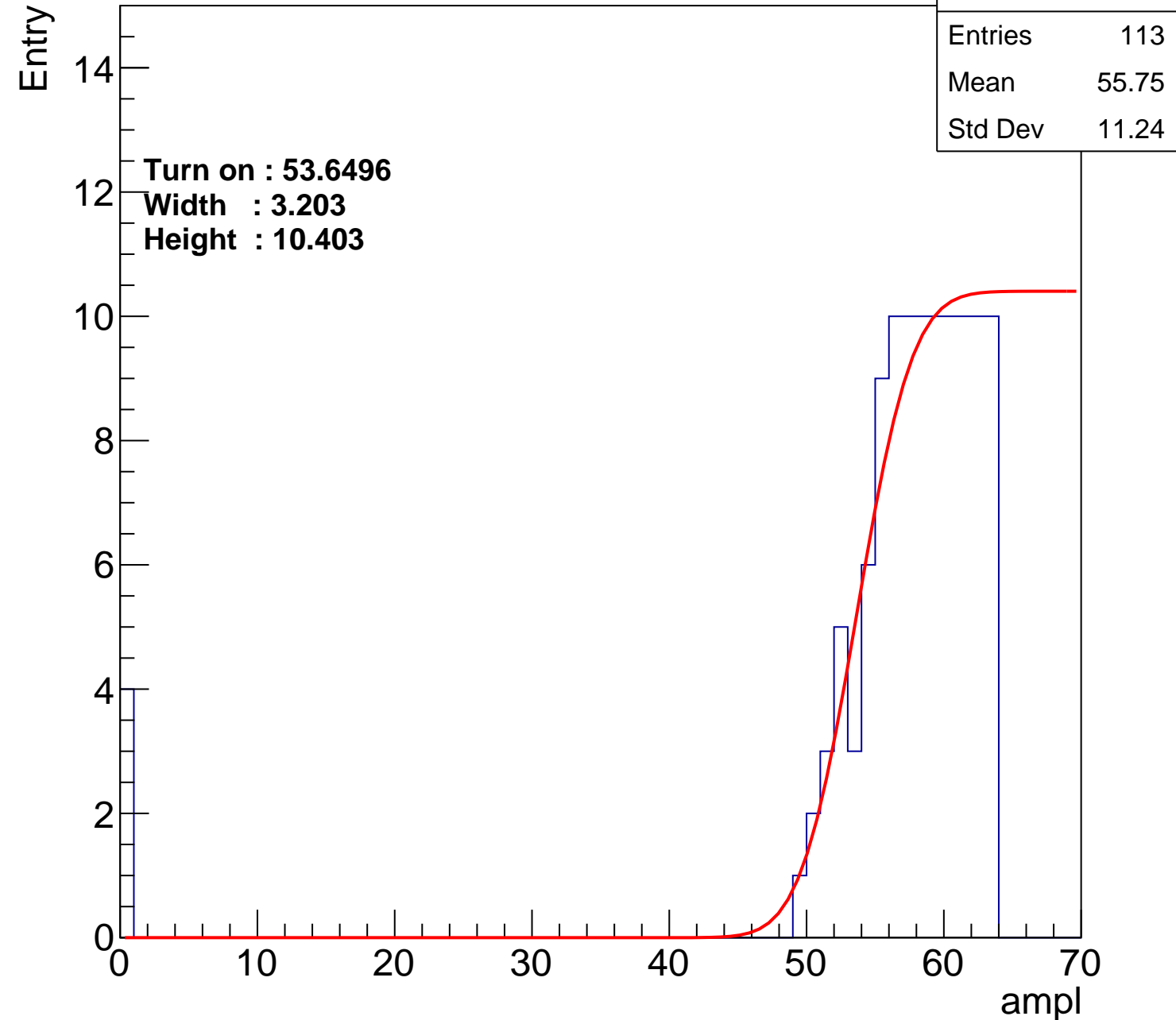
Width : 3.203

Height : 10.403

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch17

calib_packv5_040323_1717.root, FC#2, port C3

Entries	121
Mean	56.46
Std Dev	8.16

Turn on : 51.6095

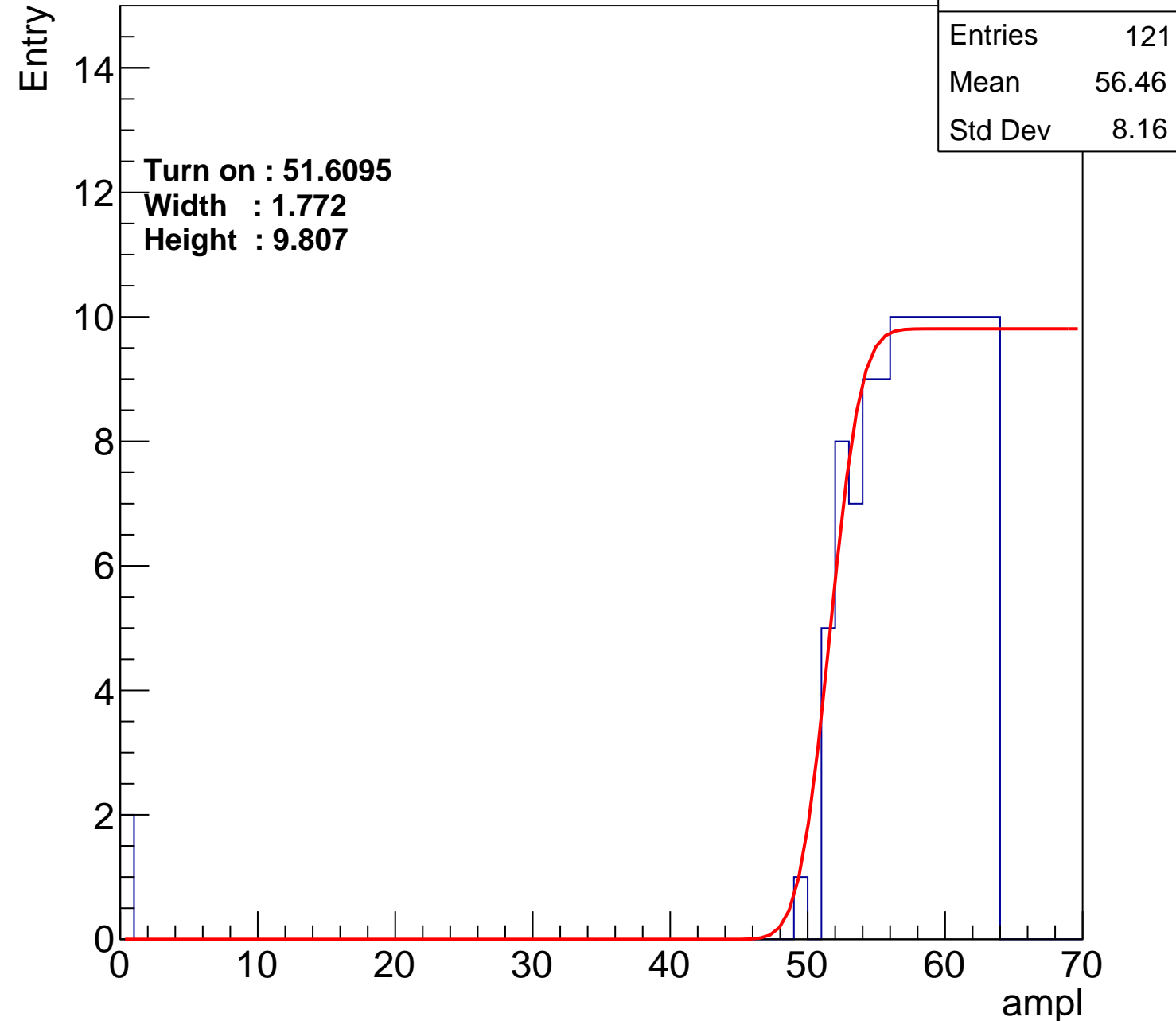
Width : 1.772

Height : 9.807

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch18

calib_packv5_040323_1717.root, FC#2, port C3

Entries	110
Mean	56.57
Std Dev	8.561

Turn on : 53.5707

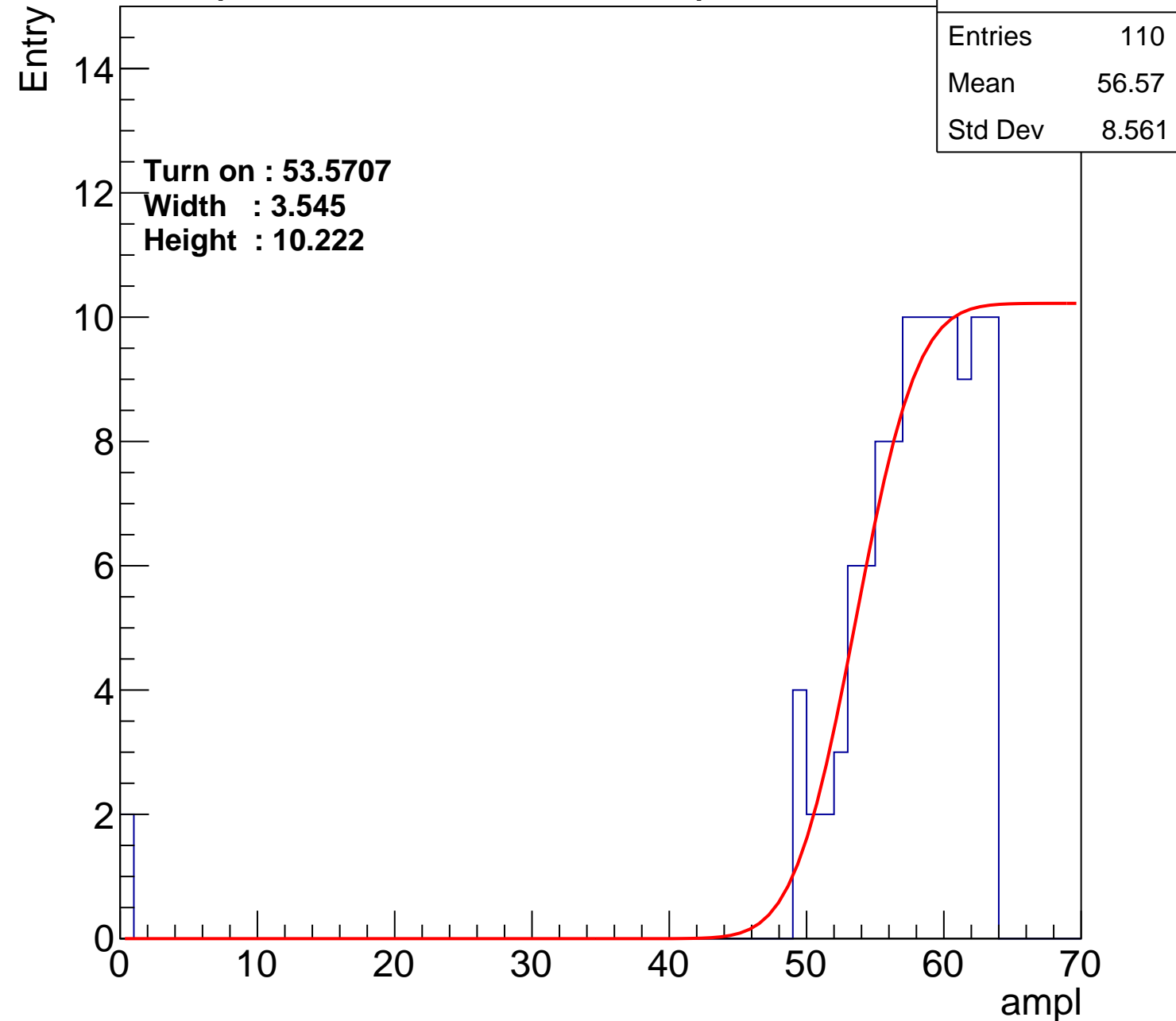
Width : 3.545

Height : 10.222

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch19

calib_packv5_040323_1717.root, FC#2, port C3

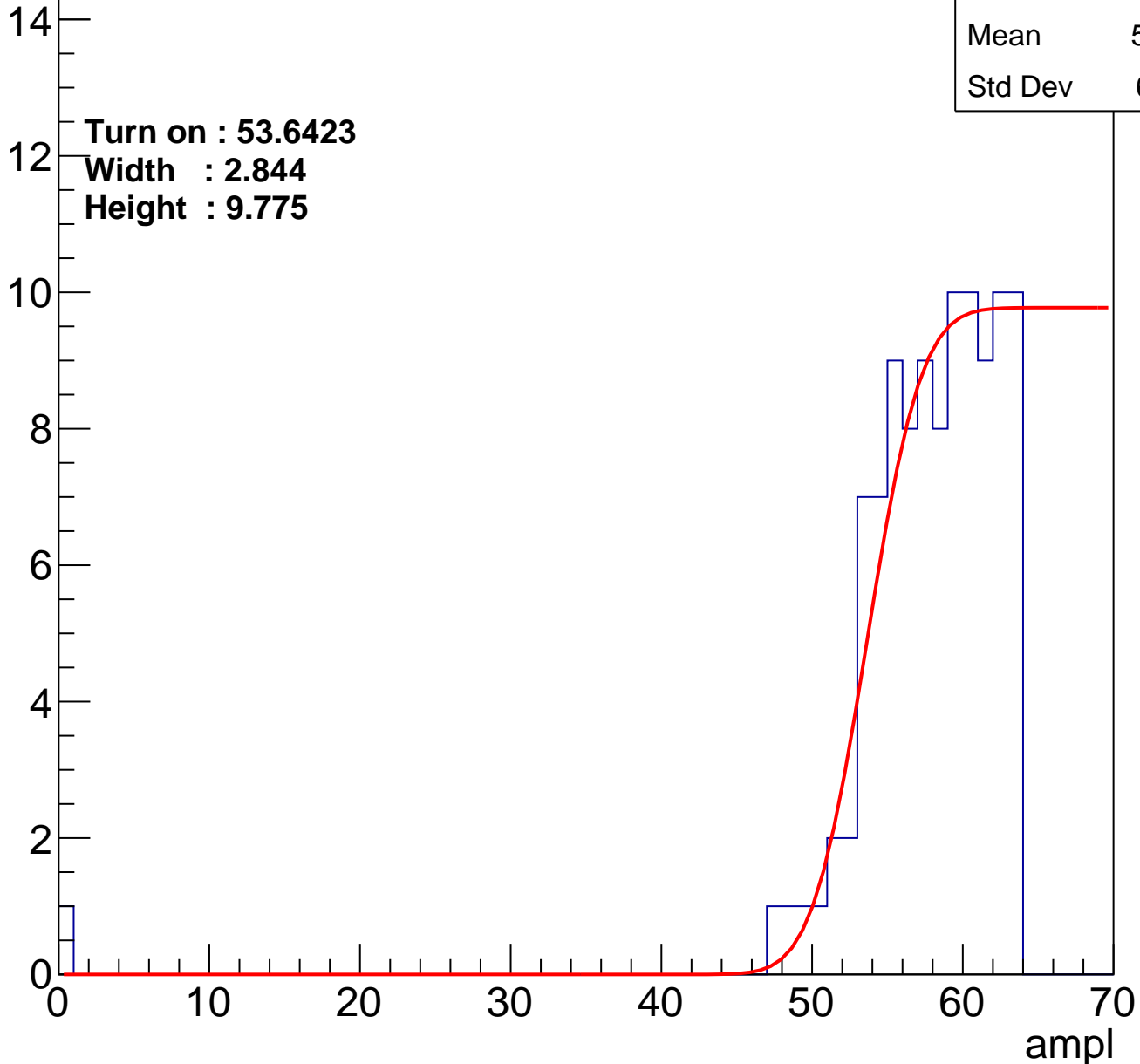
Entries	106
Mean	57.15
Std Dev	6.711

Turn on : 53.6423

Width : 2.844

Height : 9.775

Entry



B0L103S, U12-ch20

calib_packv5_040323_1717.root, FC#2, port C3

Entries	114
Mean	55.7
Std Dev	11.19

Turn on : 53.2287

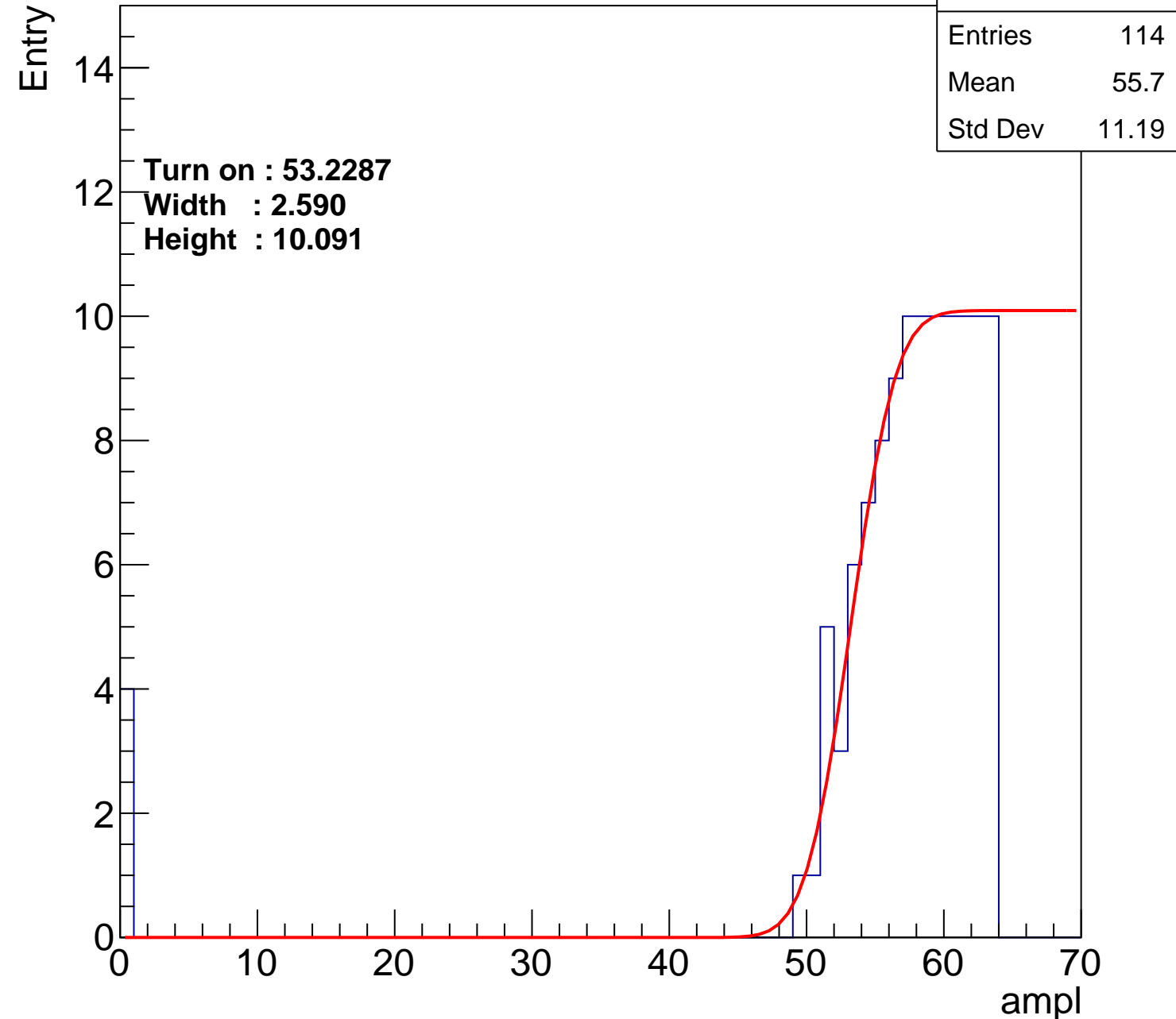
Width : 2.590

Height : 10.091

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch21

calib_packv5_040323_1717.root, FC#2, port C3

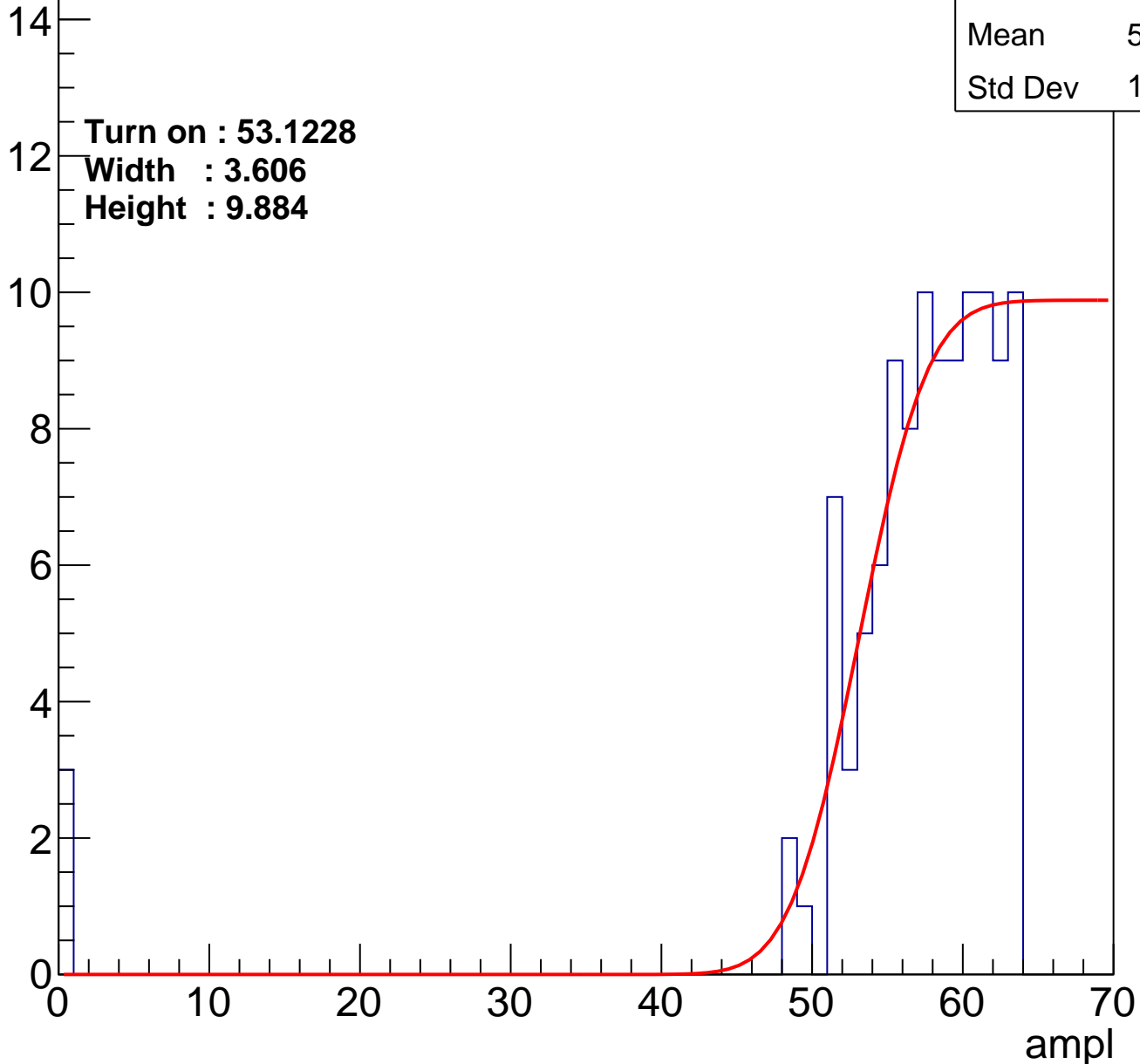
Entries	111
Mean	55.95
Std Dev	10.06

Turn on : 53.1228

Width : 3.606

Height : 9.884

Entry



B0L103S, U12-ch22

calib_packv5_040323_1717.root, FC#2, port C3

Entries	124
Mean	55.79
Std Dev	9.59

Turn on : 51.5239

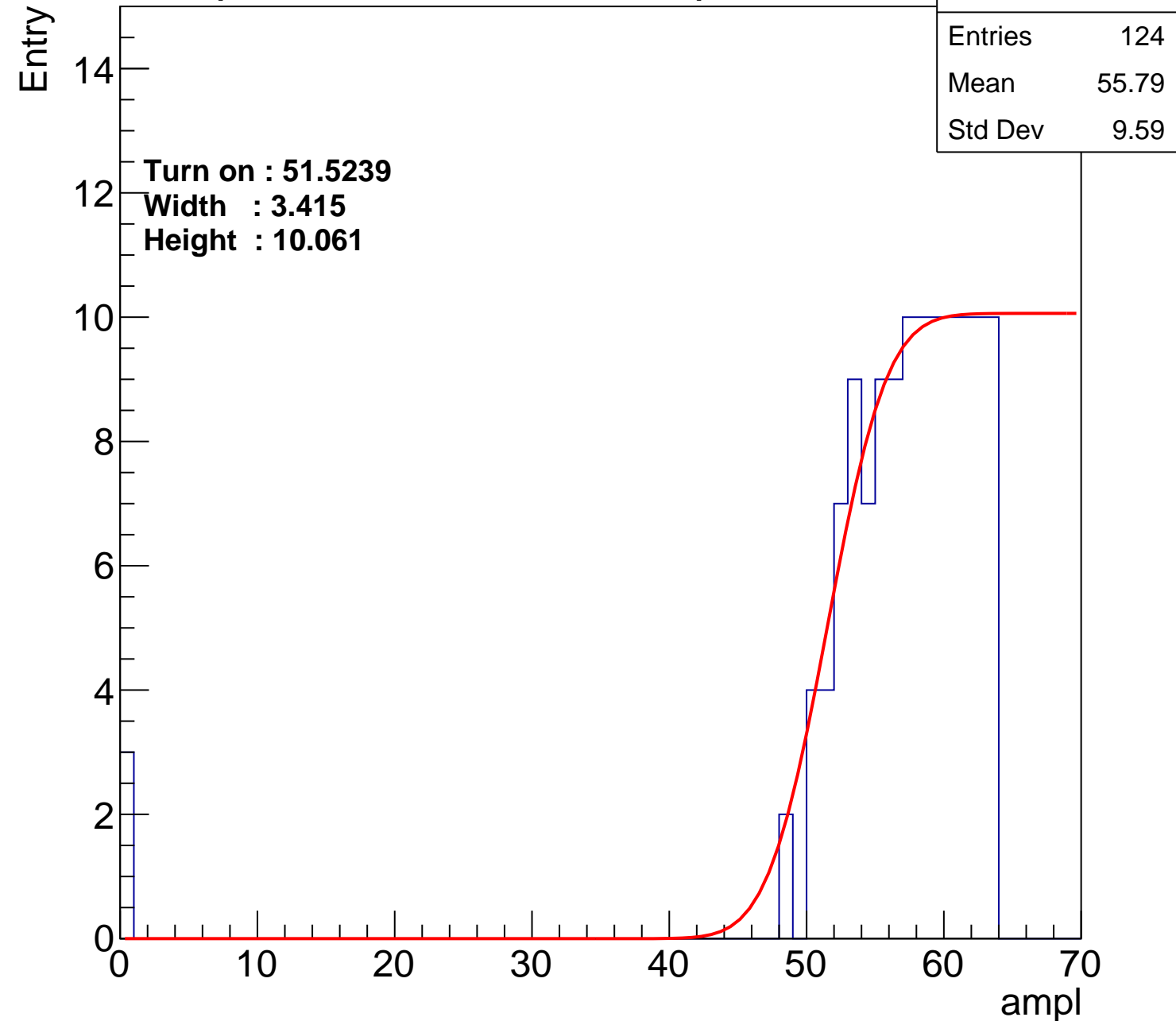
Width : 3.415

Height : 10.061

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch23

calib_packv5_040323_1717.root, FC#2, port C3

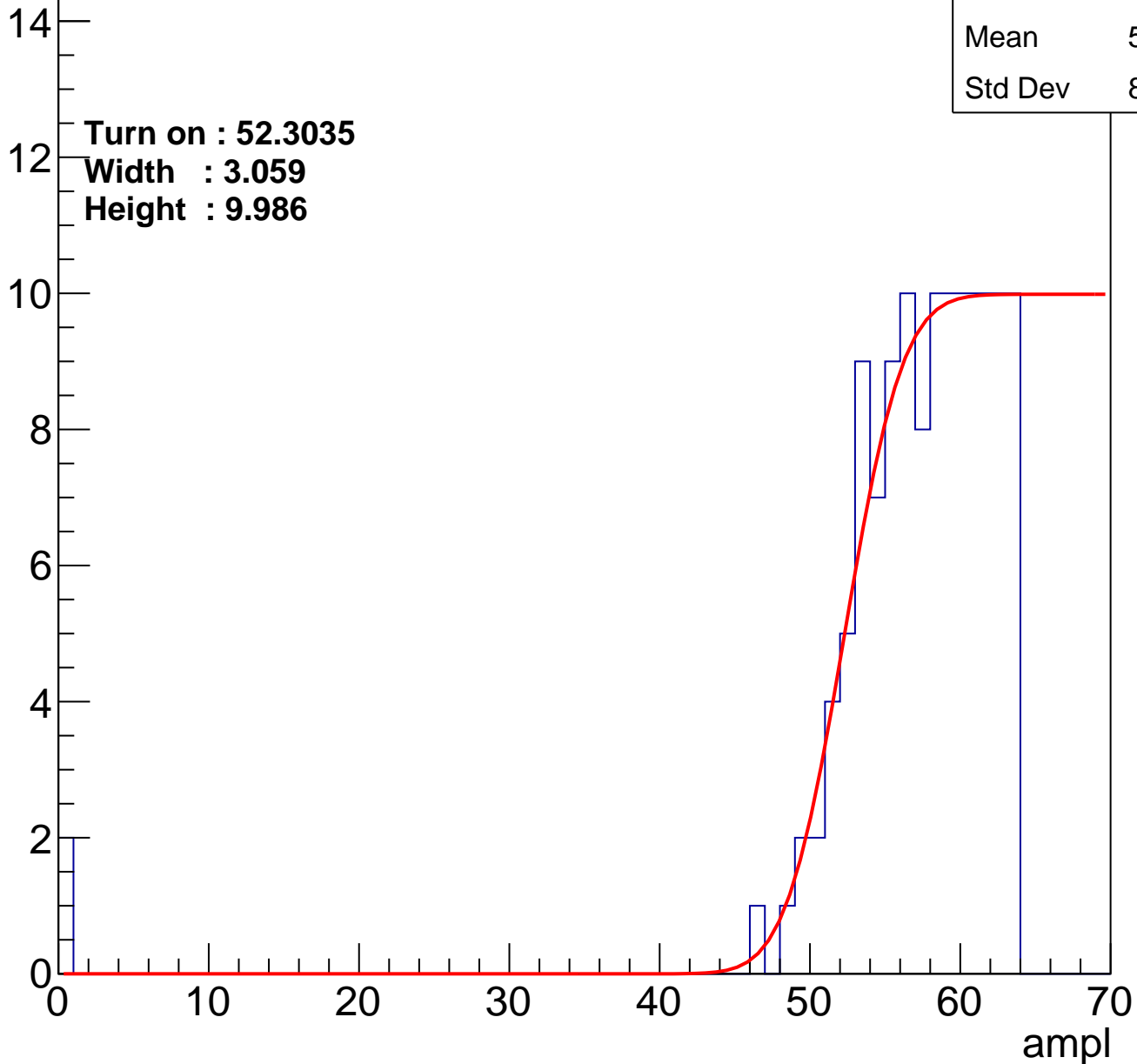
Entries	120
Mean	56.27
Std Dev	8.313

Turn on : 52.3035

Width : 3.059

Height : 9.986

Entry



B0L103S, U12-ch24

calib_packv5_040323_1717.root, FC#2, port C3

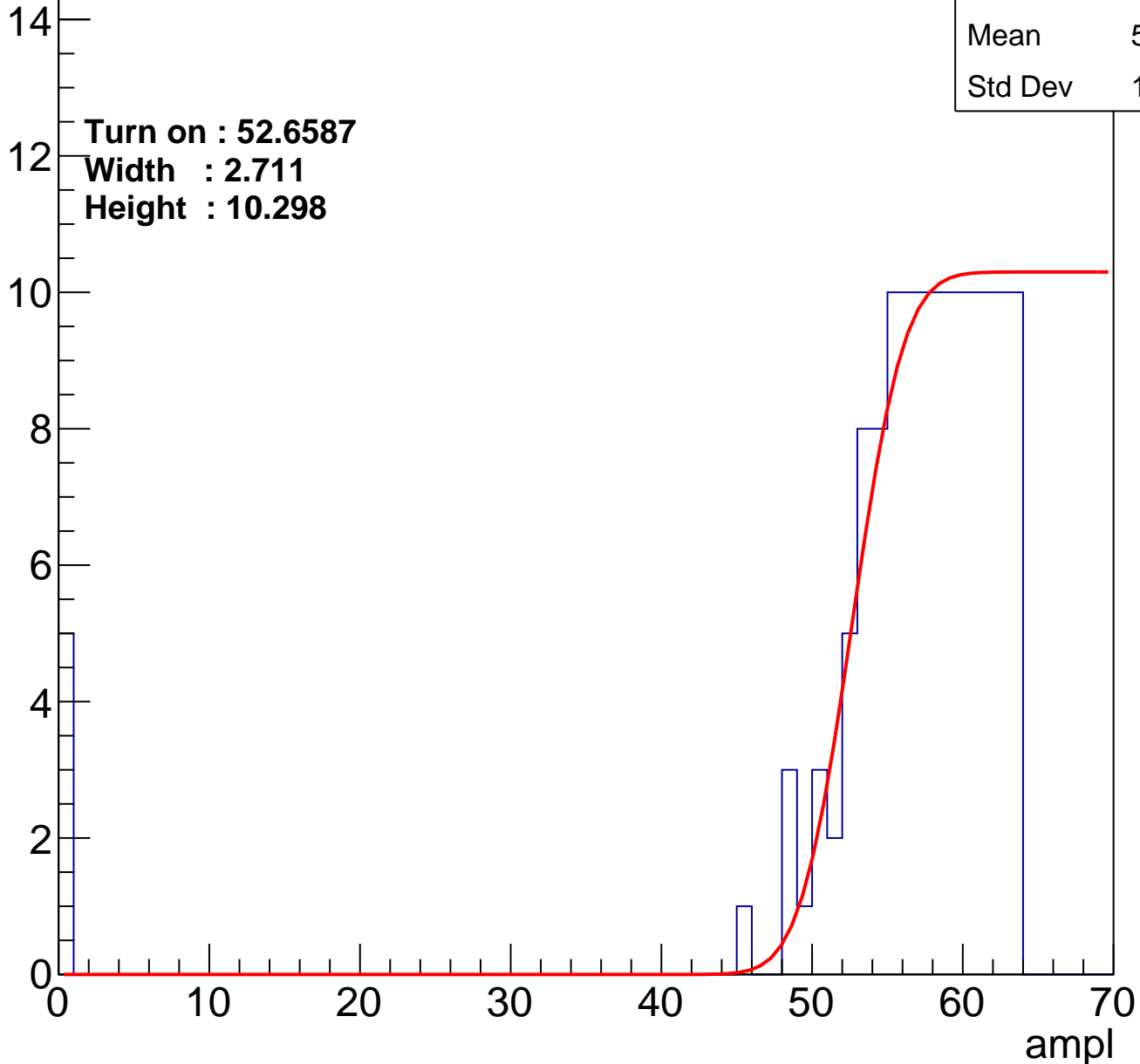
Entries	126
Mean	54.89
Std Dev	11.83

Turn on : 52.6587

Width : 2.711

Height : 10.298

Entry



B0L103S, U12-ch25

calib_packv5_040323_1717.root, FC#2, port C3

Entries	115
Mean	57.08
Std Dev	6.477

Turn on : 53.0461

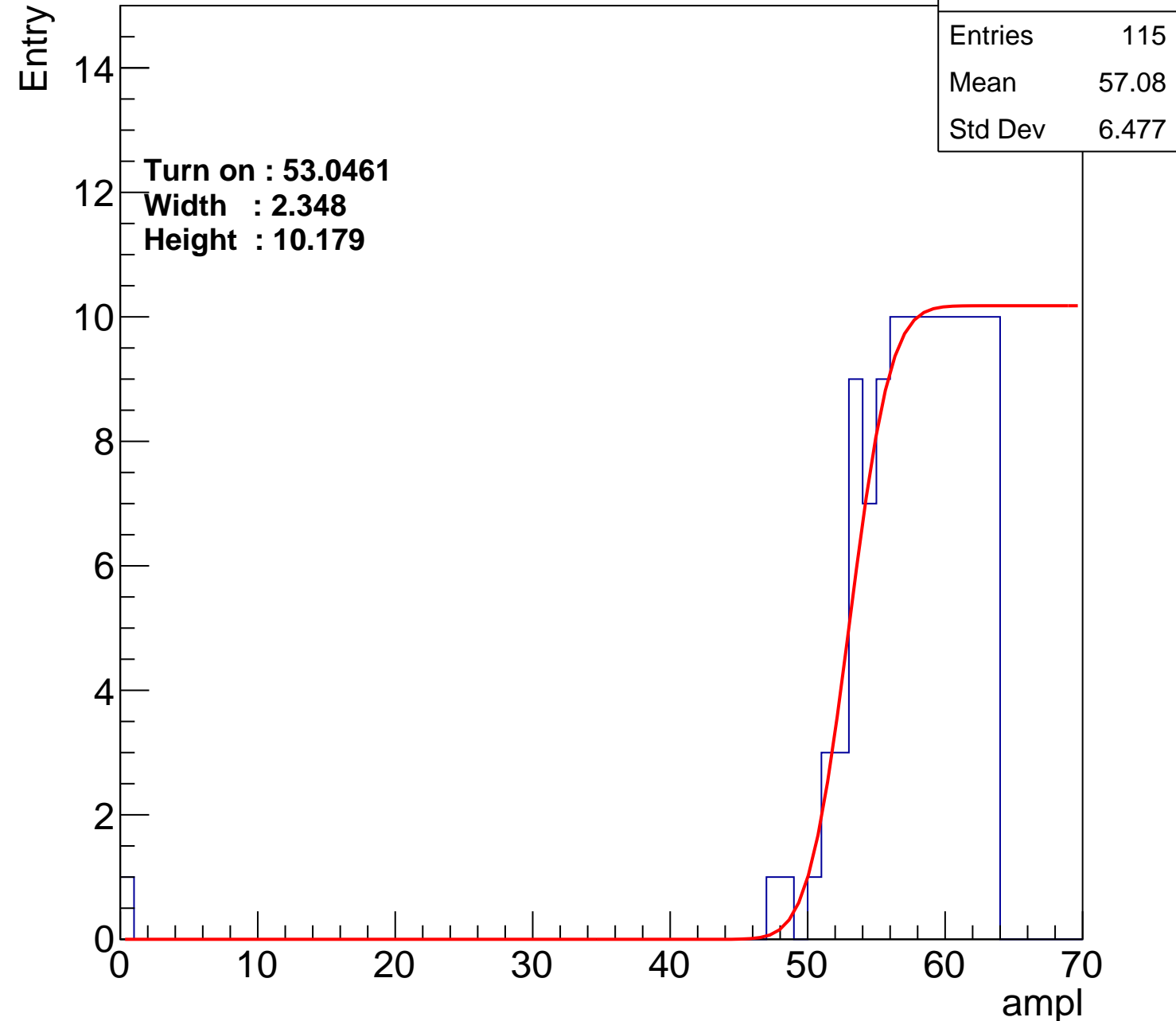
Width : 2.348

Height : 10.179

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch26

calib_packv5_040323_1717.root, FC#2, port C3

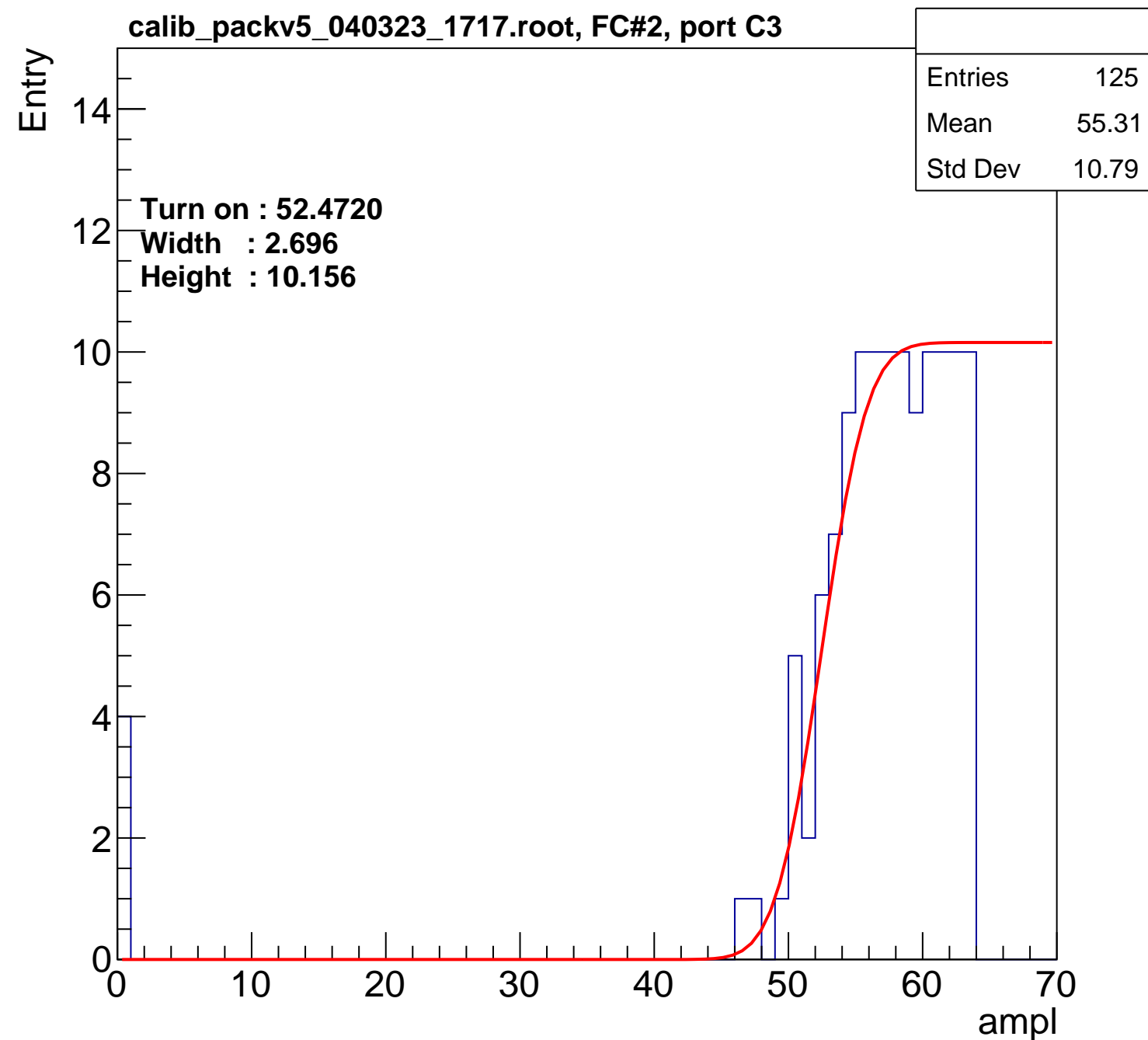
Entry

14
12
10
8
6
4
2
0

Turn on : 52.4720
Width : 2.696
Height : 10.156

Entries	125
Mean	55.31
Std Dev	10.79

ampl



B0L103S, U12-ch27

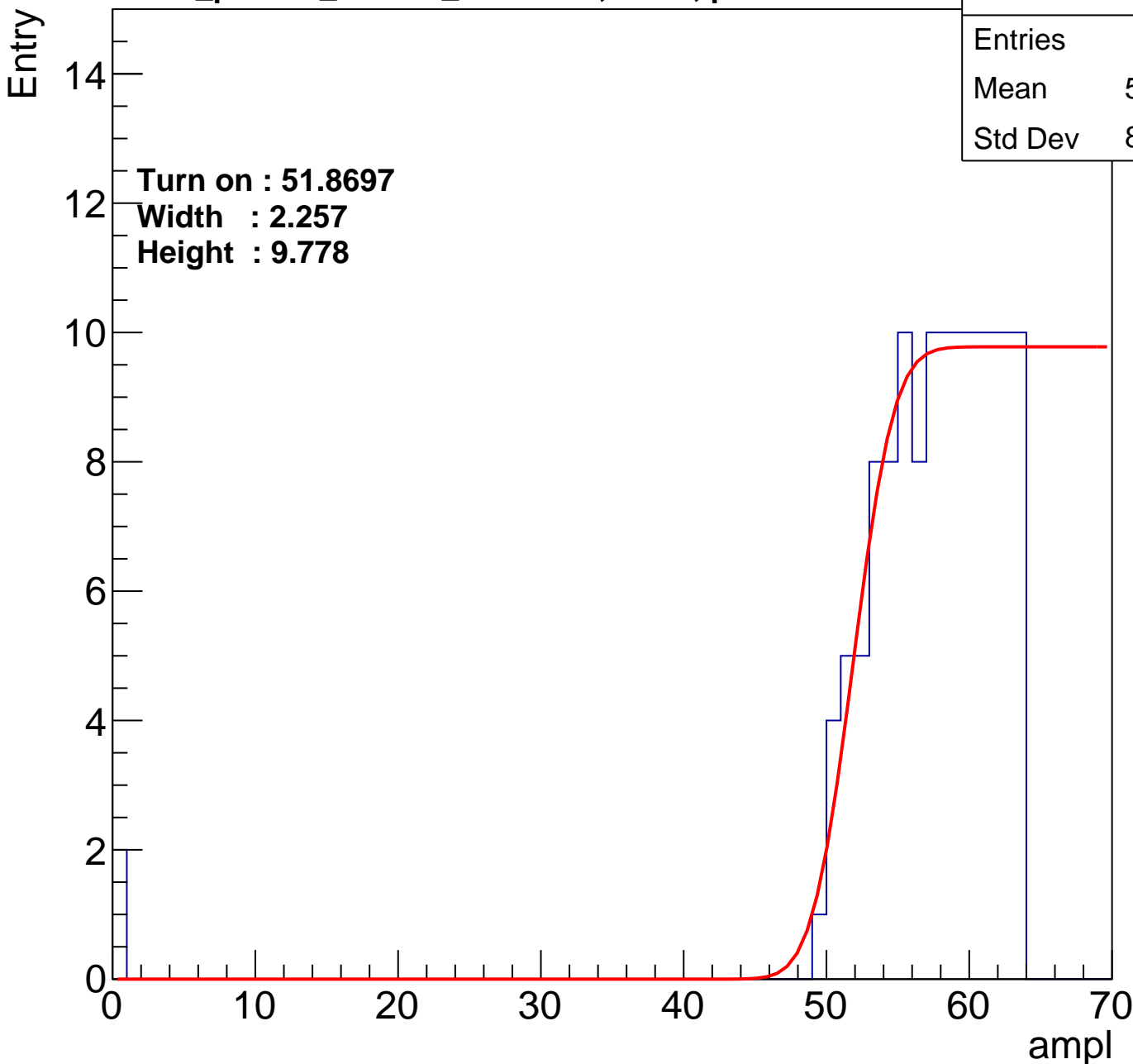
calib_packv5_040323_1717.root, FC#2, port C3

Entries	121
Mean	56.35
Std Dev	8.217

Turn on : 51.8697

Width : 2.257

Height : 9.778



B0L103S, U12-ch28

calib_packv5_040323_1717.root, FC#2, port C3

Entries	107
Mean	56.29
Std Dev	10.17

Turn on : 53.8834

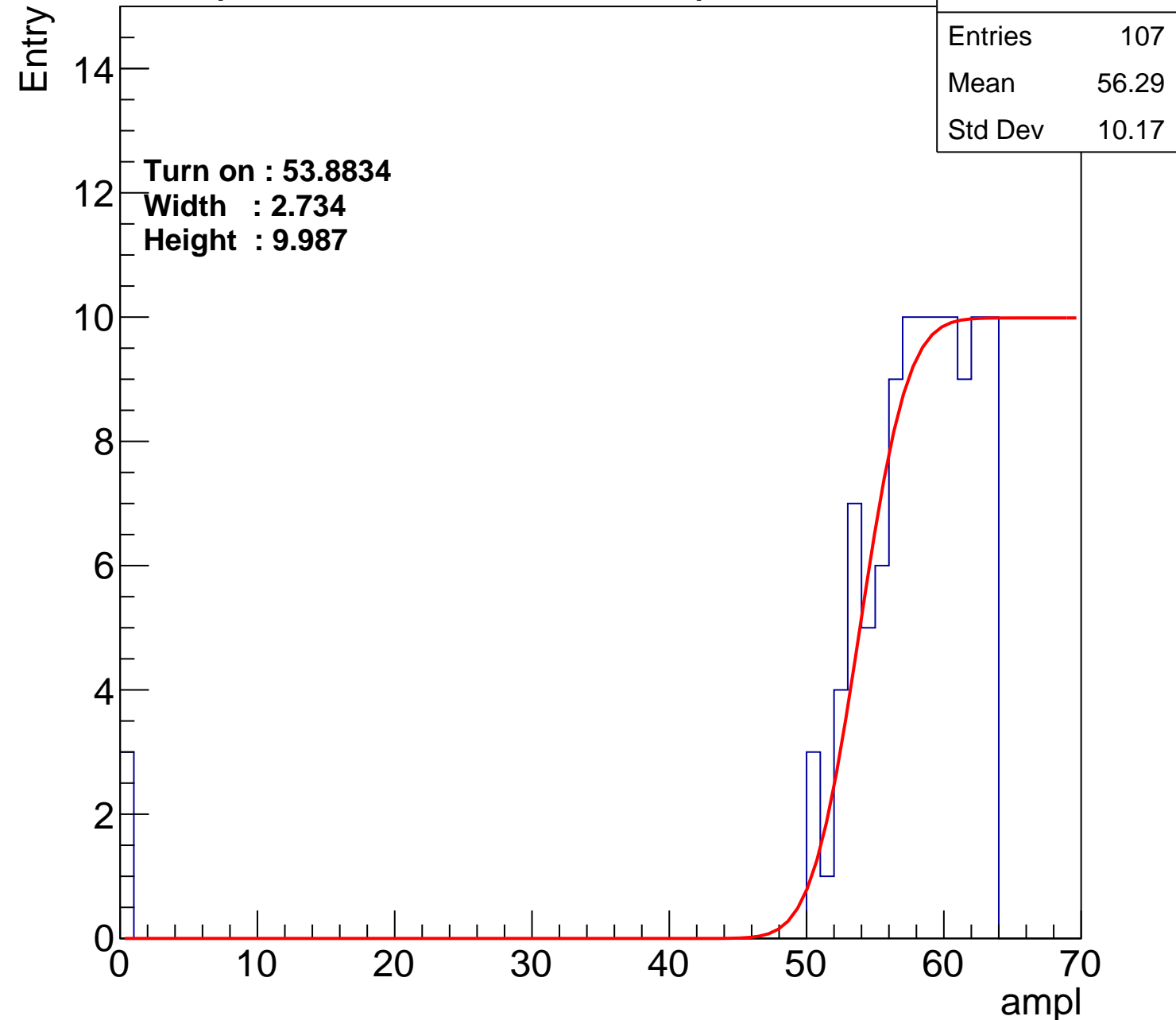
Width : 2.734

Height : 9.987

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch29

calib_packv5_040323_1717.root, FC#2, port C3

Entries	140
Mean	55.11
Std Dev	9.298

Turn on : 50.9811

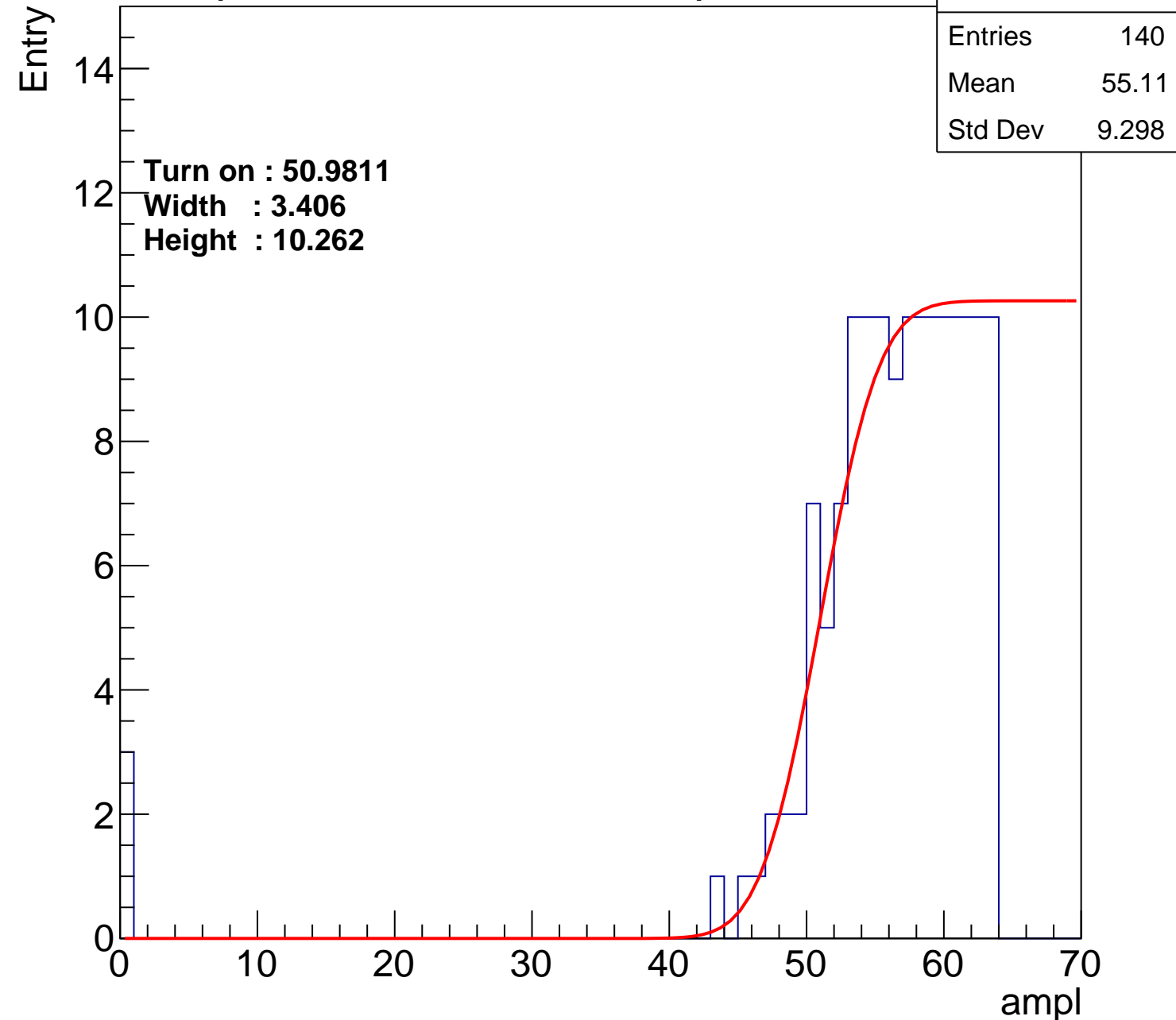
Width : 3.406

Height : 10.262

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch30

calib_packv5_040323_1717.root, FC#2, port C3

Entries	105
Mean	55.79
Std Dev	11.63

Turn on : 53.4135

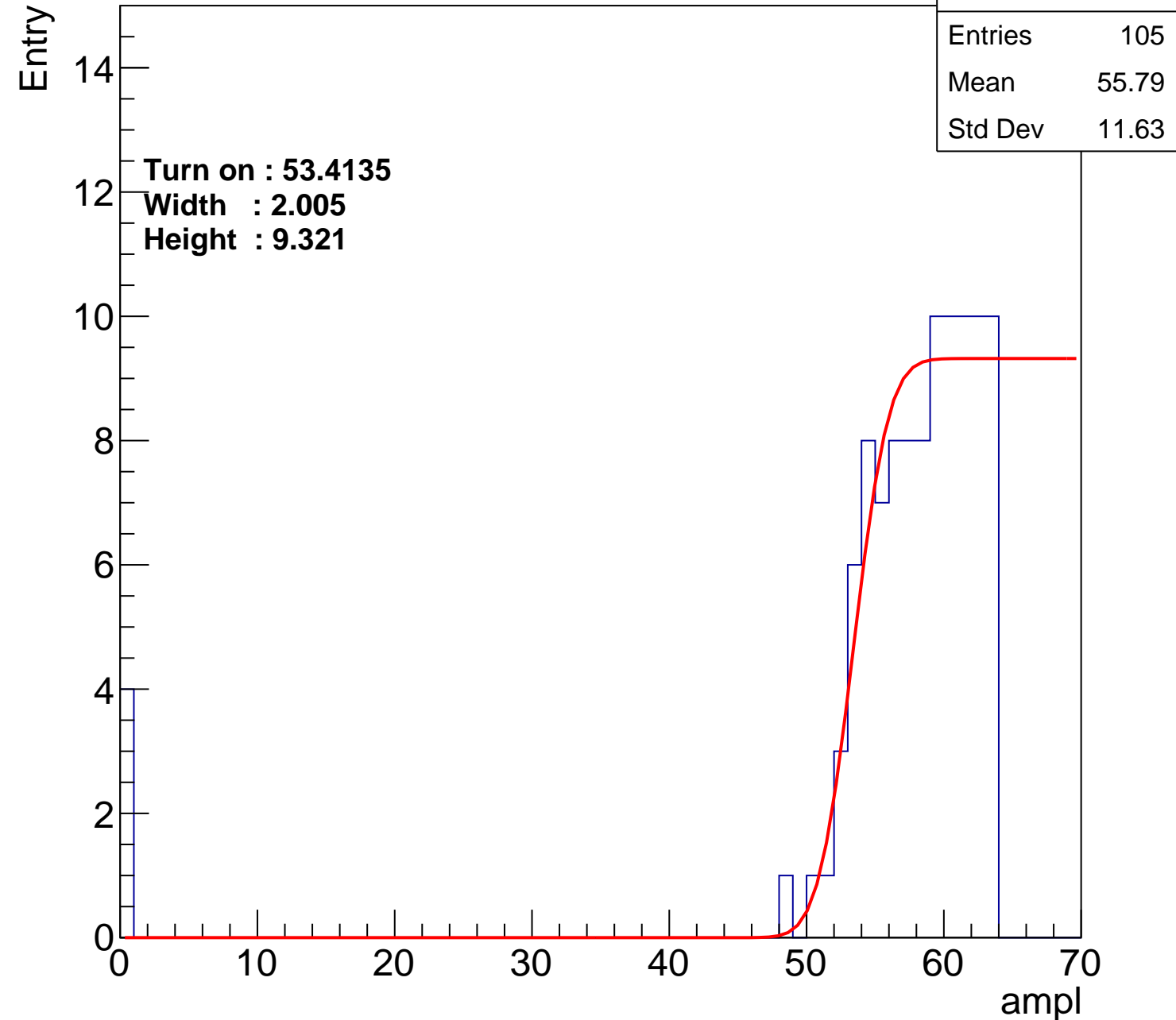
Width : 2.005

Height : 9.321

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch31

calib_packv5_040323_1717.root, FC#2, port C3

Entries	119
Mean	55.92
Std Dev	9.767

Turn on : 52.3446

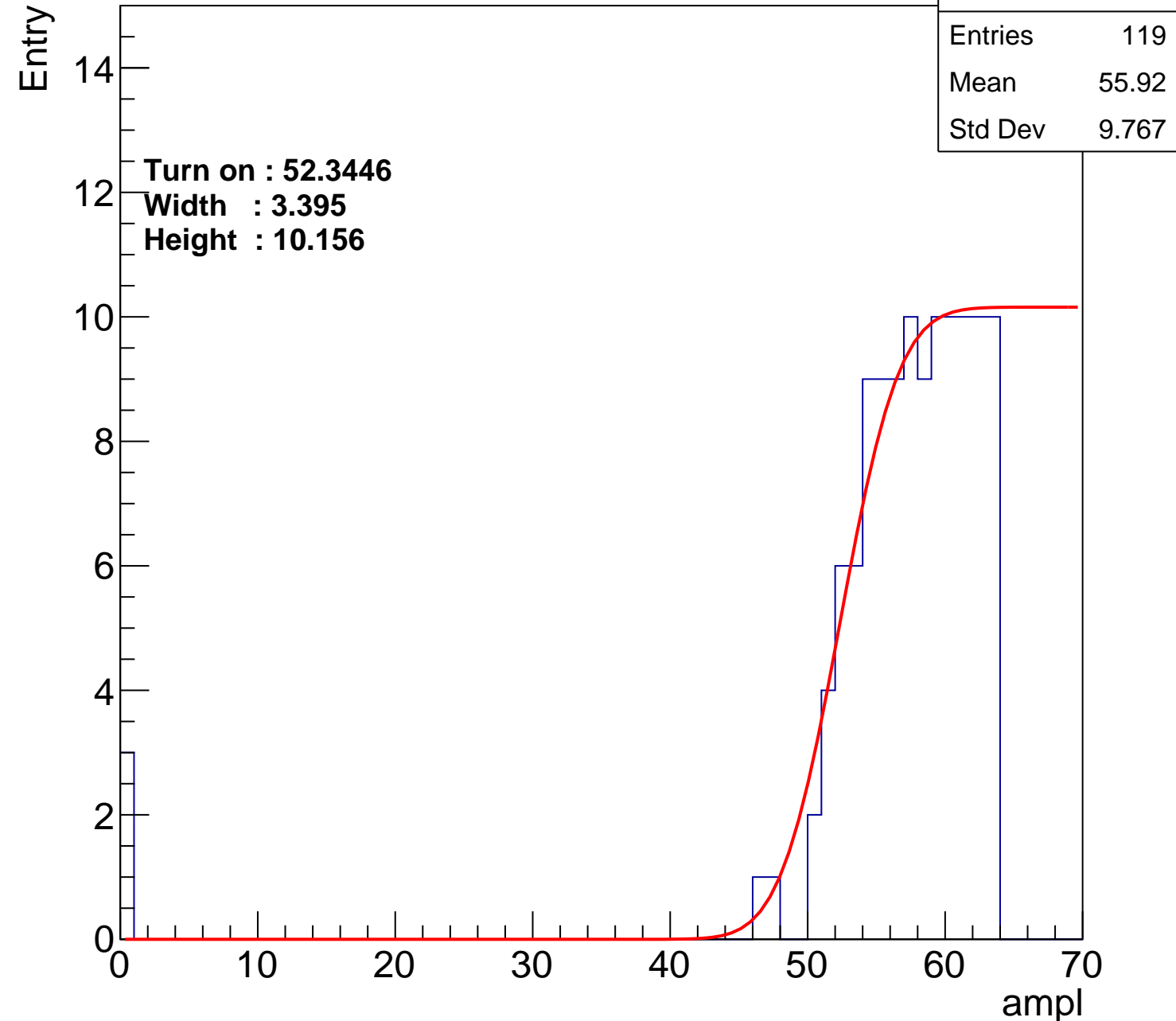
Width : 3.395

Height : 10.156

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch32

calib_packv5_040323_1717.root, FC#2, port C3

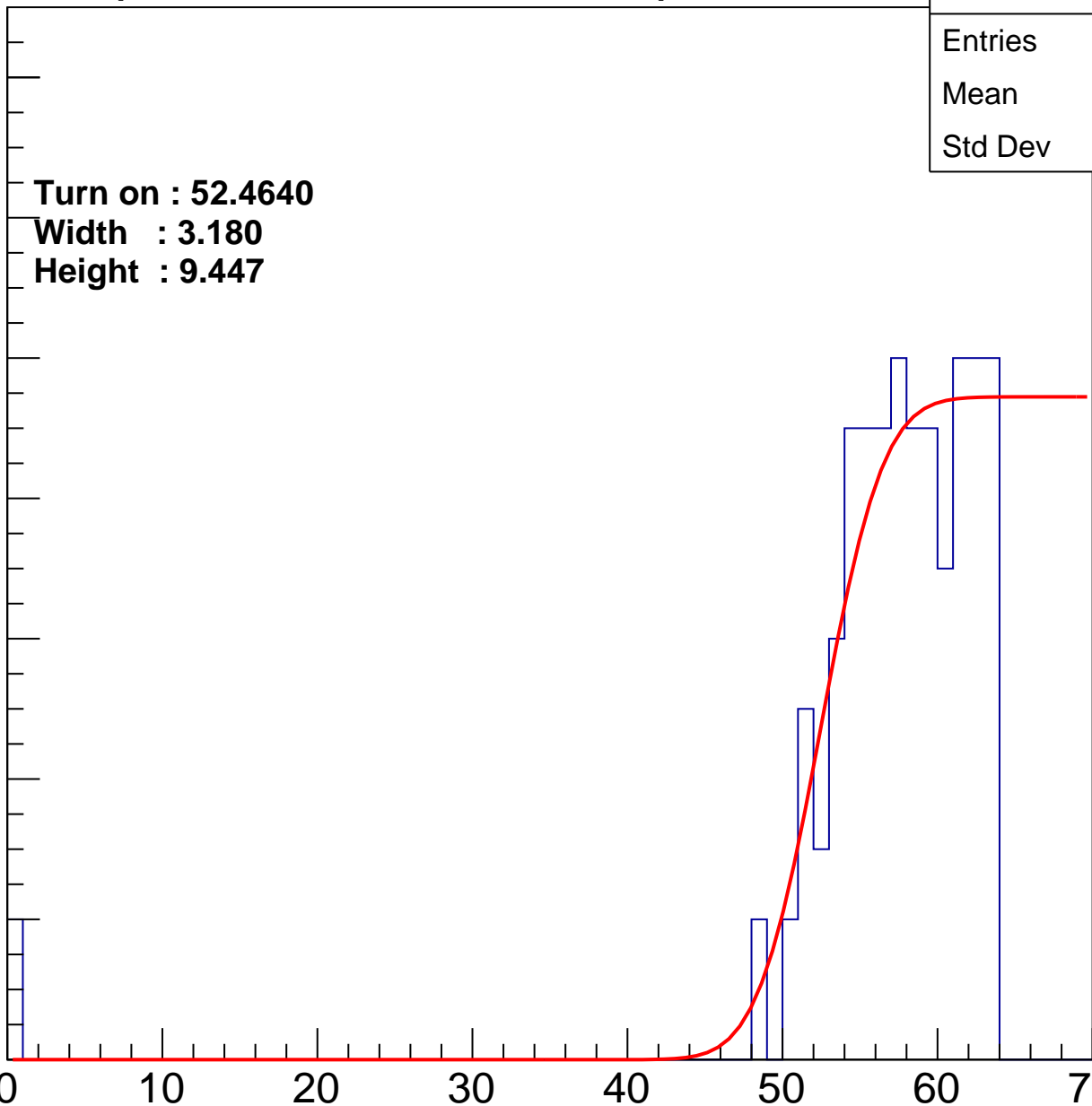
Entry

14
12
10
8
6
4
2
0

Turn on : 52.4640
Width : 3.180
Height : 9.447

Entries	112
Mean	56.37
Std Dev	8.487

ampl



B0L103S, U12-ch33

calib_packv5_040323_1717.root, FC#2, port C3

Entries	116
Mean	56.04
Std Dev	9.849

Turn on : 52.9174

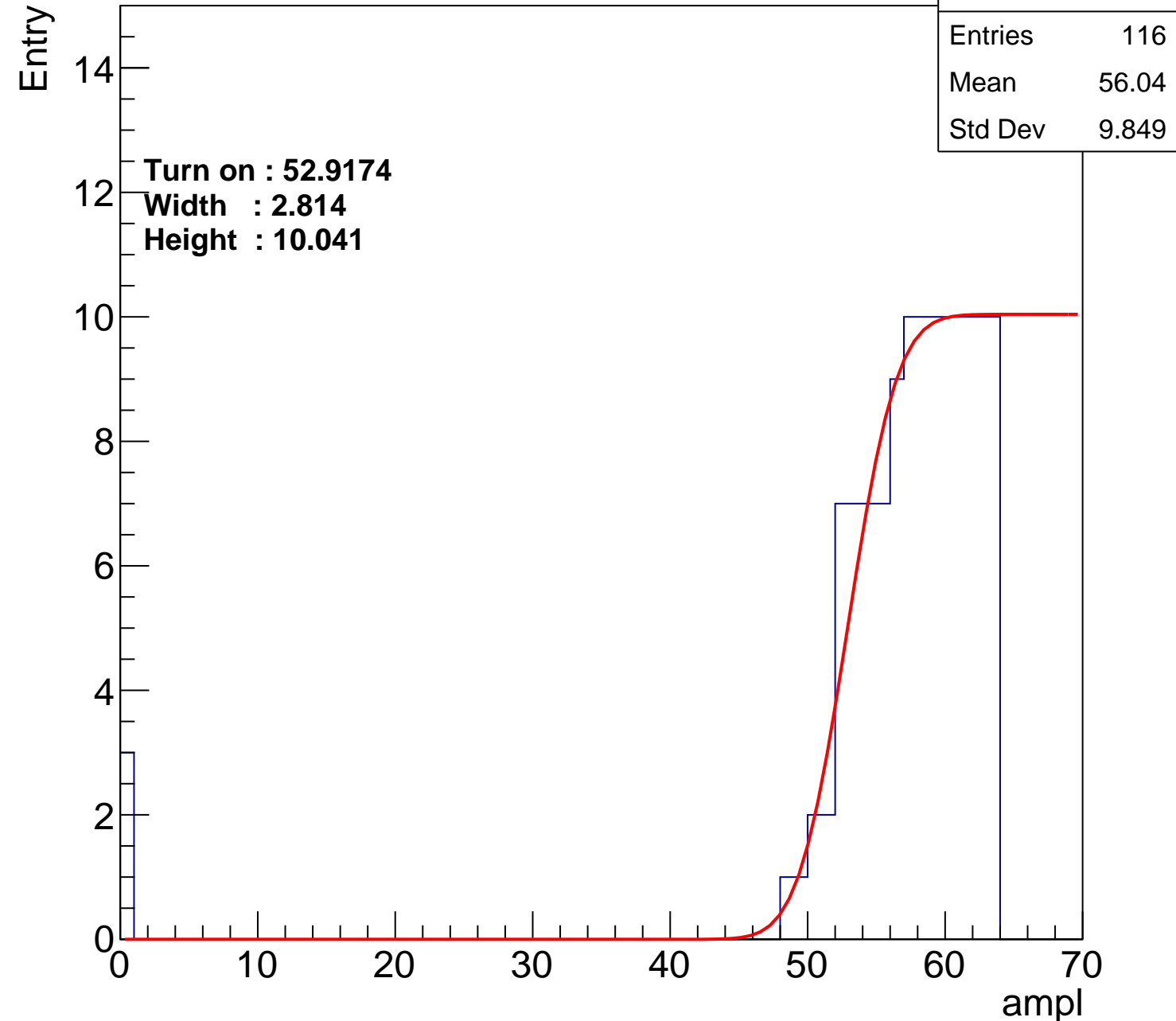
Width : 2.814

Height : 10.041

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch34

calib_packv5_040323_1717.root, FC#2, port C3

Entries	116
Mean	55.34
Std Dev	11.15

Turn on : 53.0713

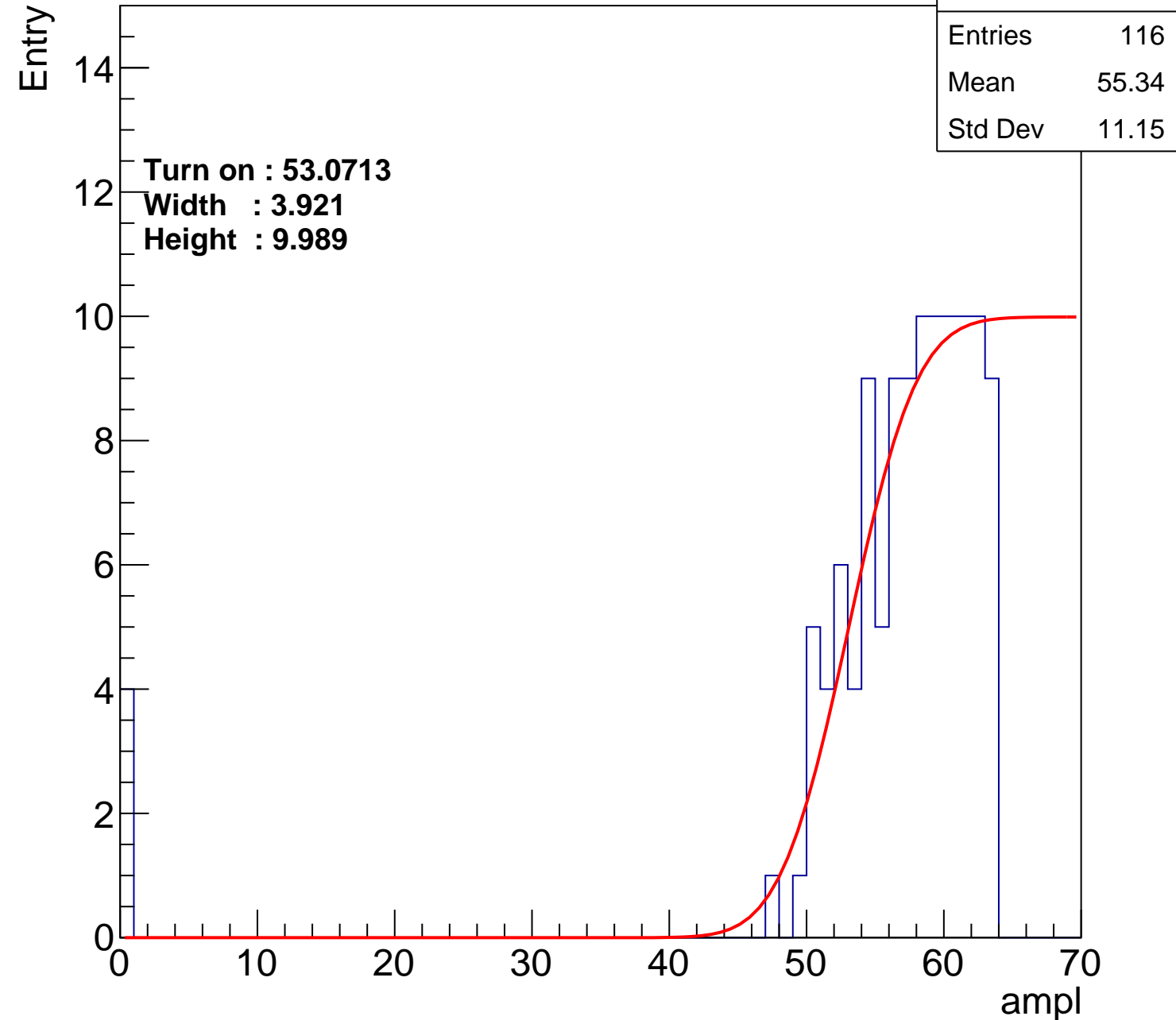
Width : 3.921

Height : 9.989

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch35

calib_packv5_040323_1717.root, FC#2, port C3

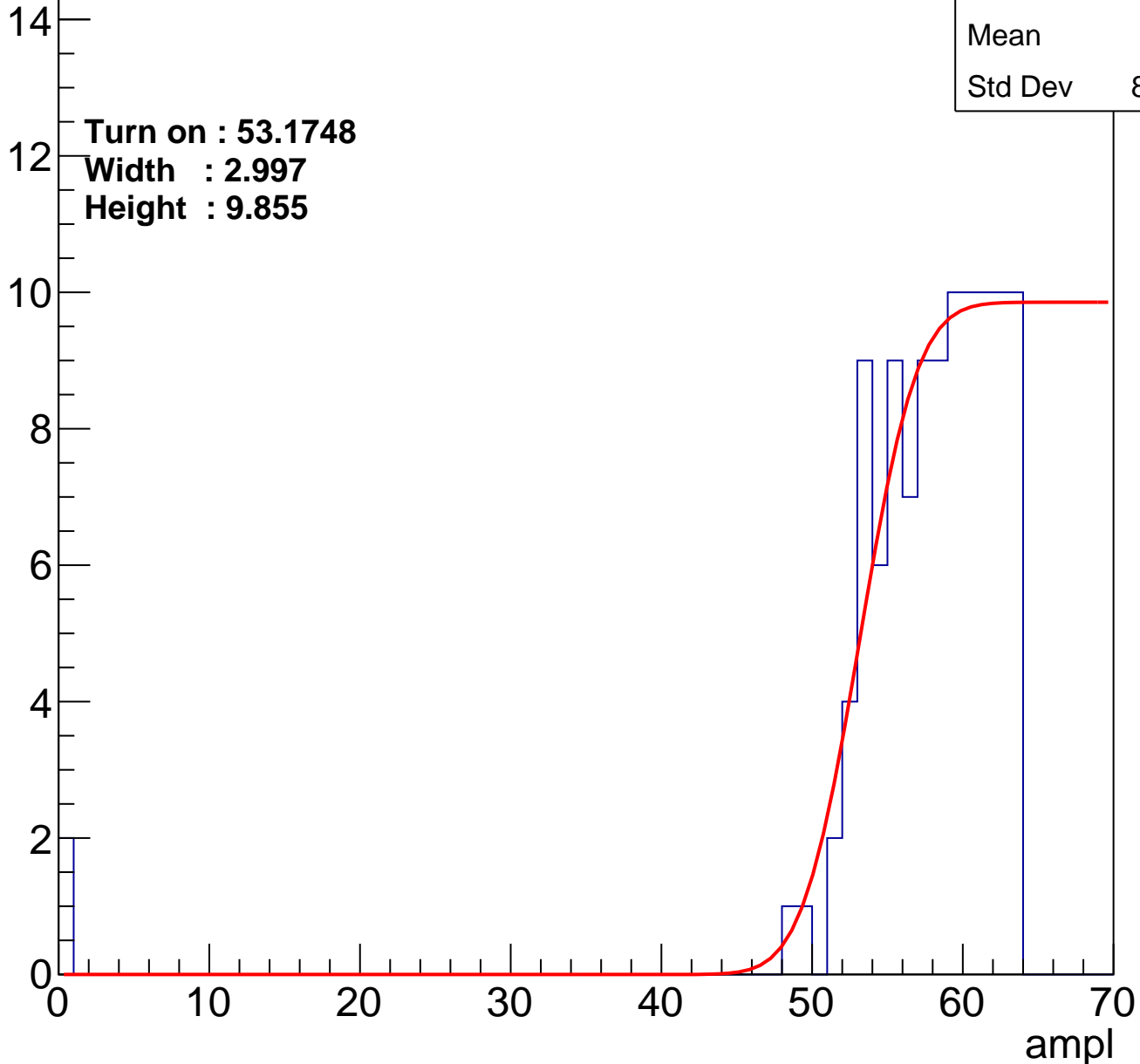
Entries	109
Mean	56.7
Std Dev	8.543

Turn on : 53.1748

Width : 2.997

Height : 9.855

Entry



B0L103S, U12-ch36

calib_packv5_040323_1717.root, FC#2, port C3

Entries	123
Mean	55.84
Std Dev	9.617

Turn on : 52.2563

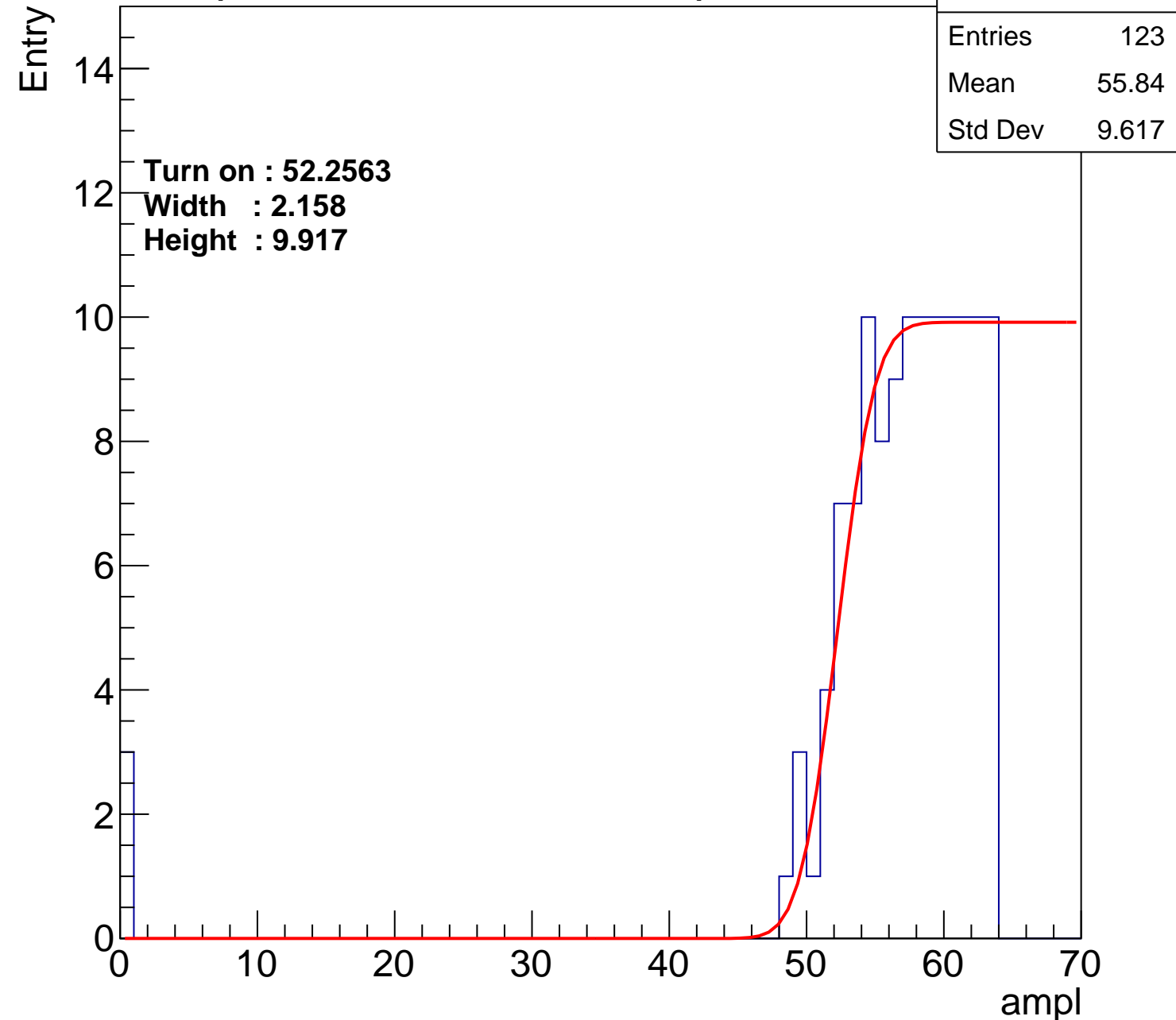
Width : 2.158

Height : 9.917

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch37

calib_packv5_040323_1717.root, FC#2, port C3

Entries	134
Mean	54.72
Std Dev	10.52

Turn on : 51.2968

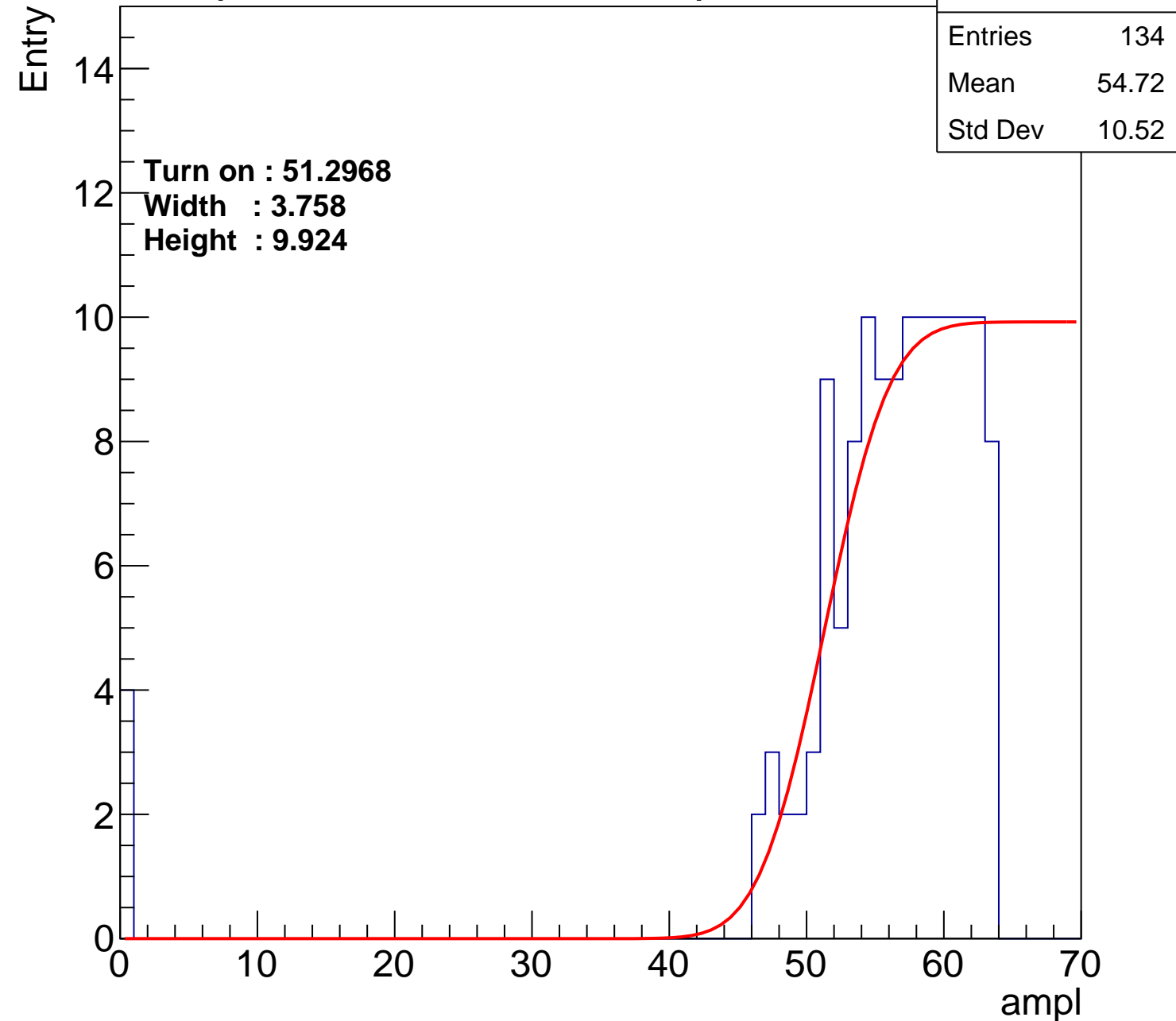
Width : 3.758

Height : 9.924

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch38

calib_packv5_040323_1717.root, FC#2, port C3

Entries	115
Mean	56.42
Std Dev	8.402

Turn on : 53.4383

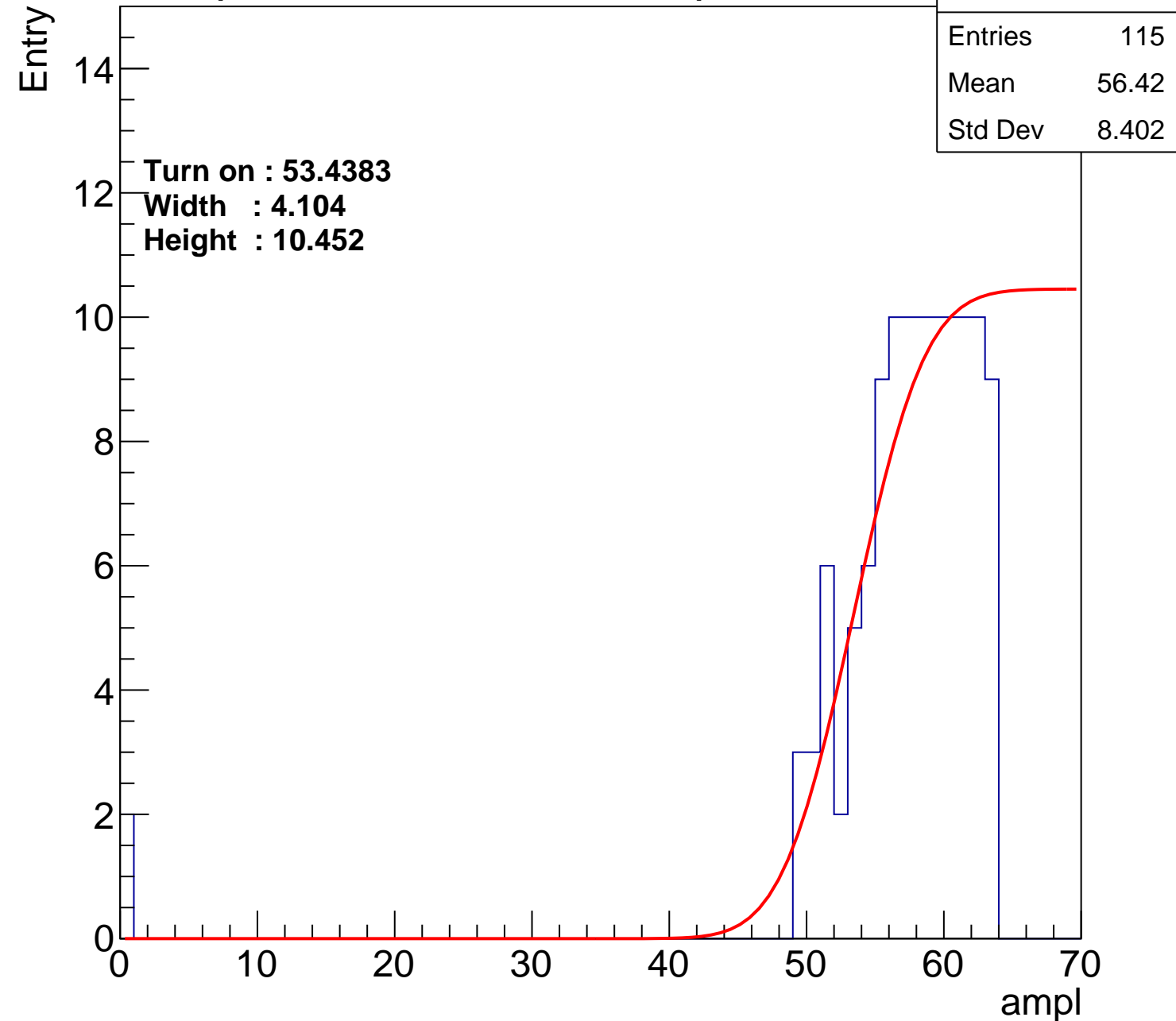
Width : 4.104

Height : 10.452

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch39

calib_packv5_040323_1717.root, FC#2, port C3

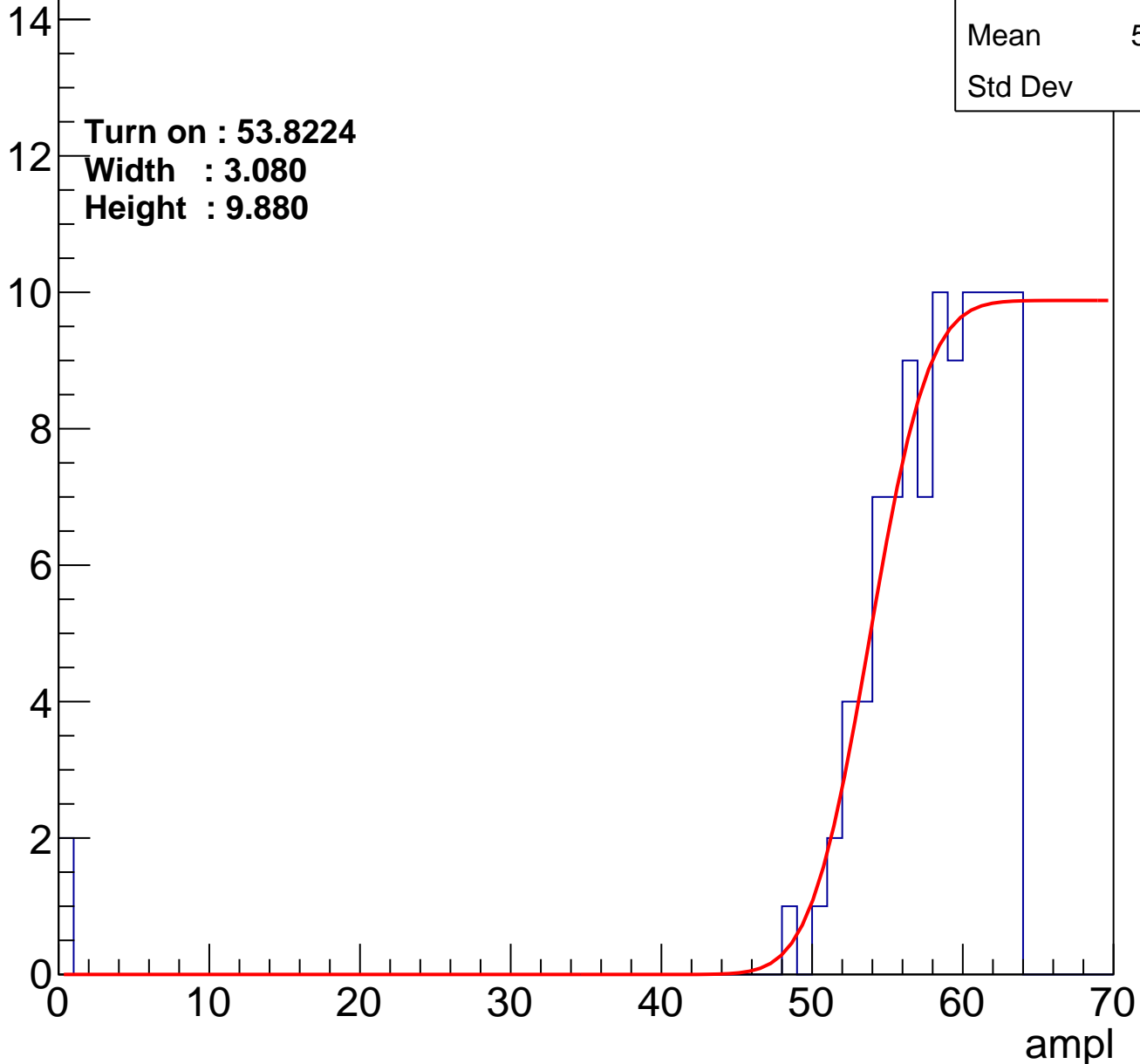
Entries	103
Mean	56.86
Std Dev	8.74

Turn on : 53.8224

Width : 3.080

Height : 9.880

Entry



B0L103S, U12-ch40

calib_packv5_040323_1717.root, FC#2, port C3

Entries	118
Mean	55.66
Std Dev	10.99

Turn on : 52.2251

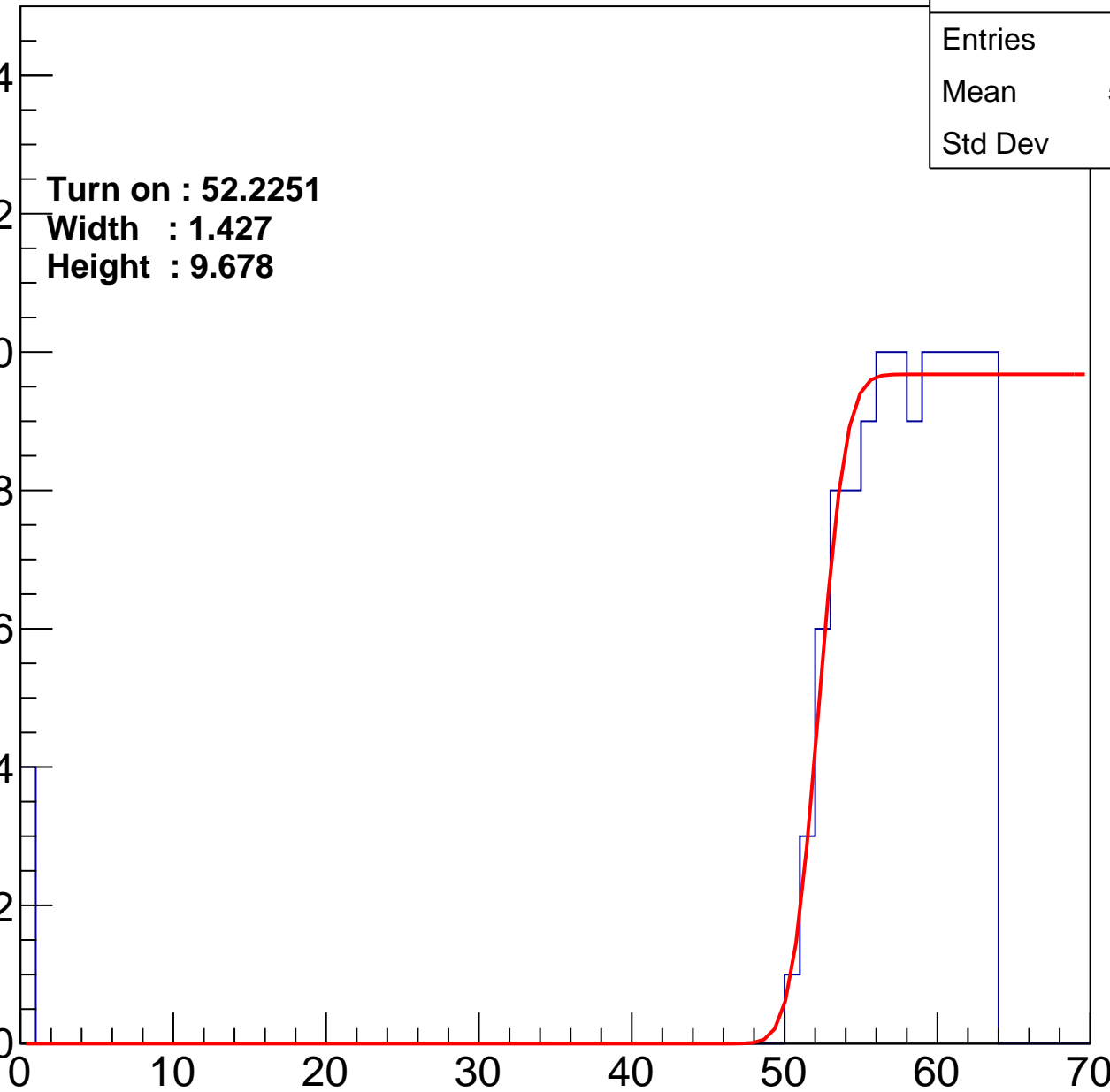
Width : 1.427

Height : 9.678

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch41

calib_packv5_040323_1717.root, FC#2, port C3

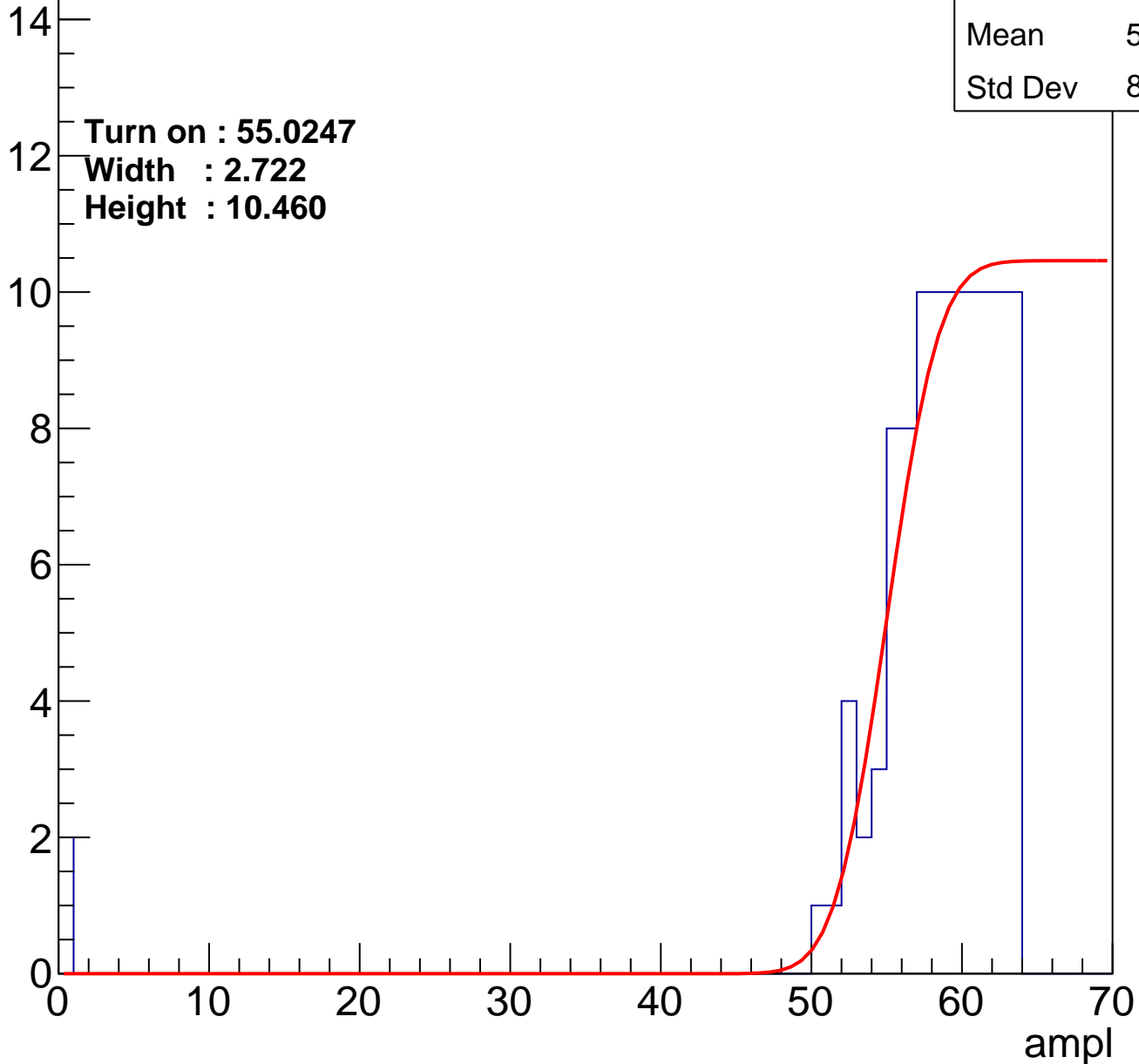
Entries	99
Mean	57.22
Std Dev	8.812

Turn on : 55.0247

Width : 2.722

Height : 10.460

Entry



B0L103S, U12-ch42

calib_packv5_040323_1717.root, FC#2, port C3

Entries	121
Mean	56.55
Std Dev	6.588

Turn on : 52.0101

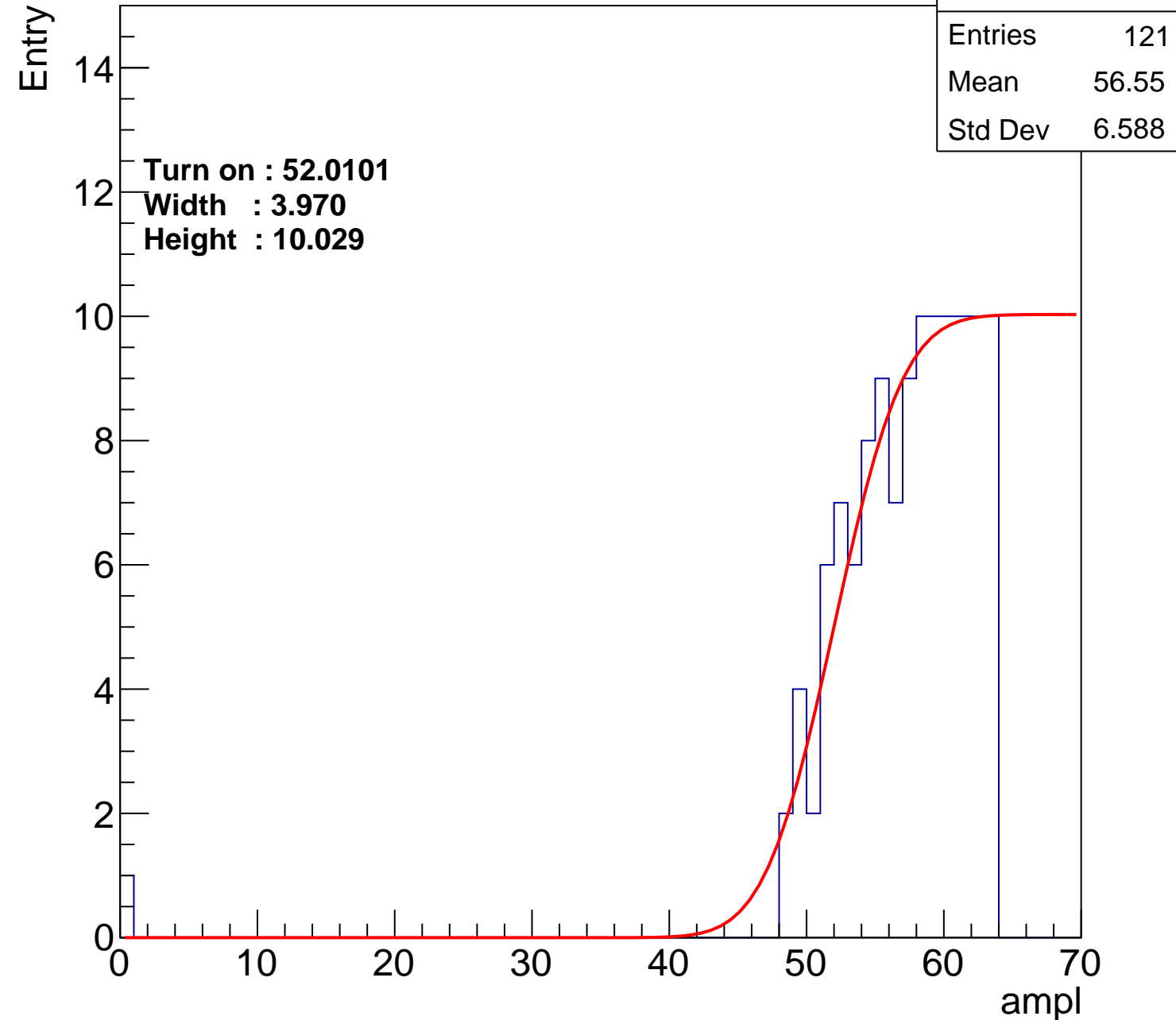
Width : 3.970

Height : 10.029

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch43

calib_packv5_040323_1717.root, FC#2, port C3

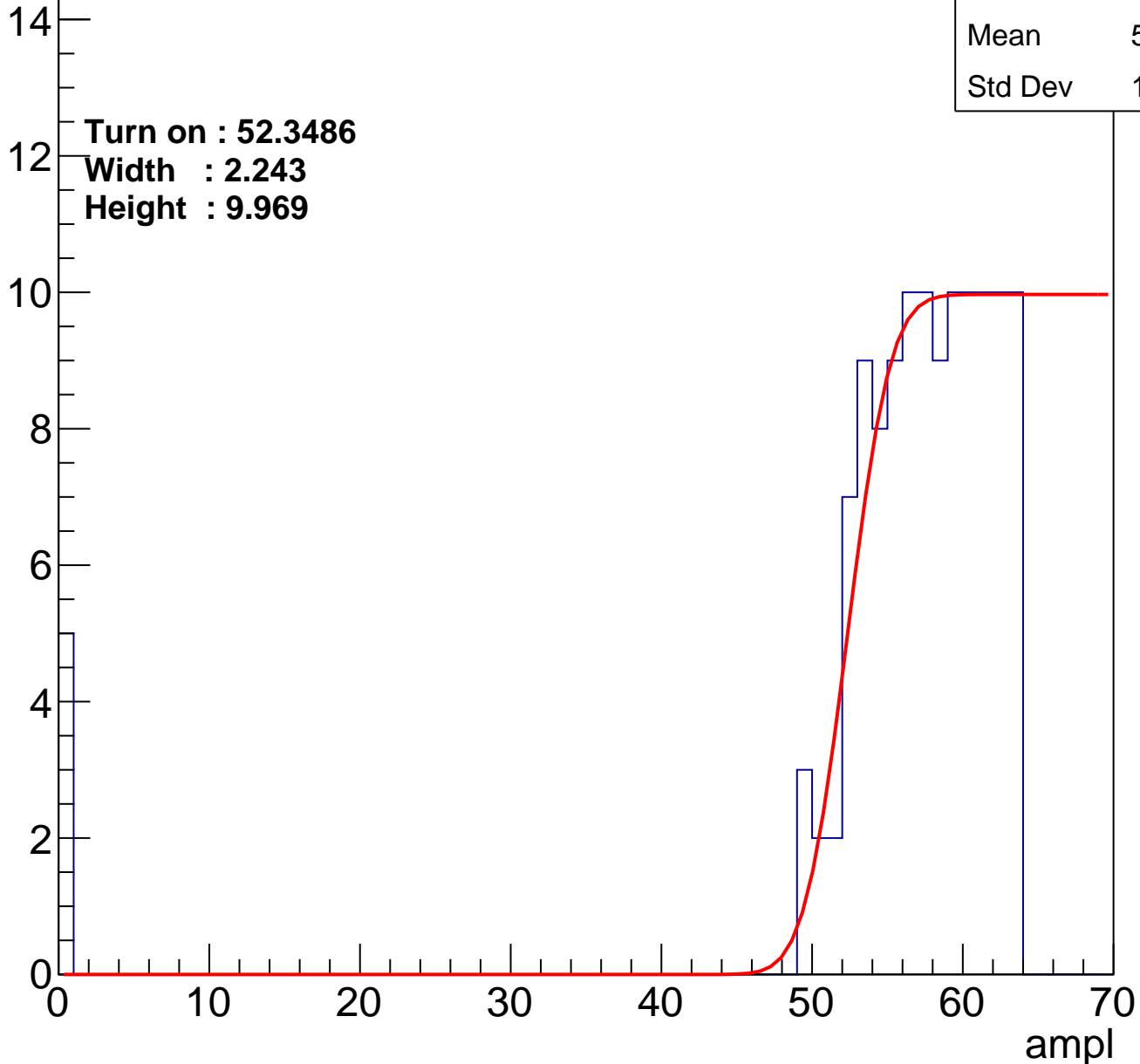
Entries	124
Mean	54.99
Std Dev	11.86

Turn on : 52.3486

Width : 2.243

Height : 9.969

Entry



B0L103S, U12-ch44

calib_packv5_040323_1717.root, FC#2, port C3

Entries	111
Mean	56.11
Std Dev	10.05

Turn on : 54.3041

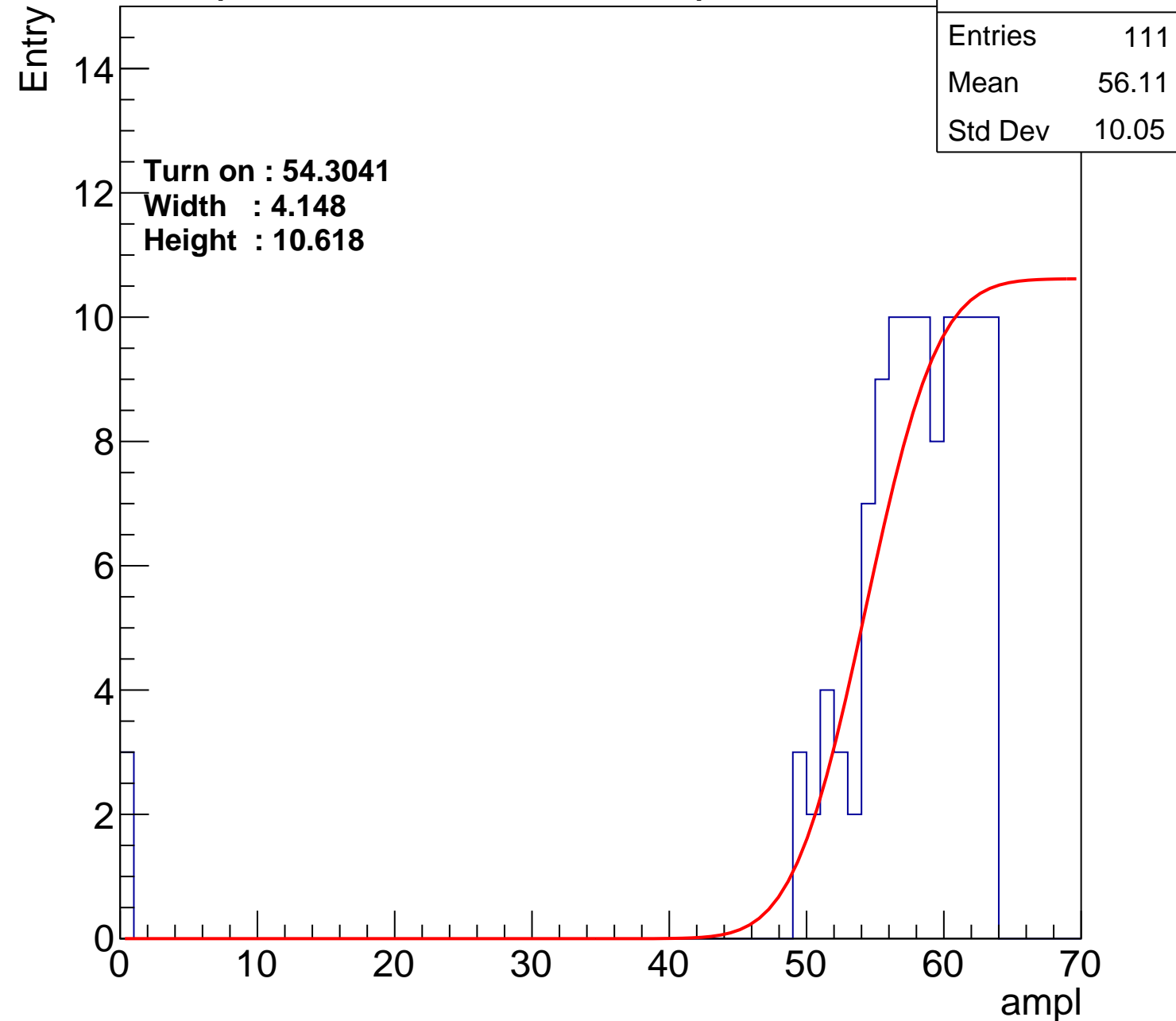
Width : 4.148

Height : 10.618

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch45

calib_packv5_040323_1717.root, FC#2, port C3

Entries	126
Mean	55.23
Std Dev	10.73

Turn on : 50.7149

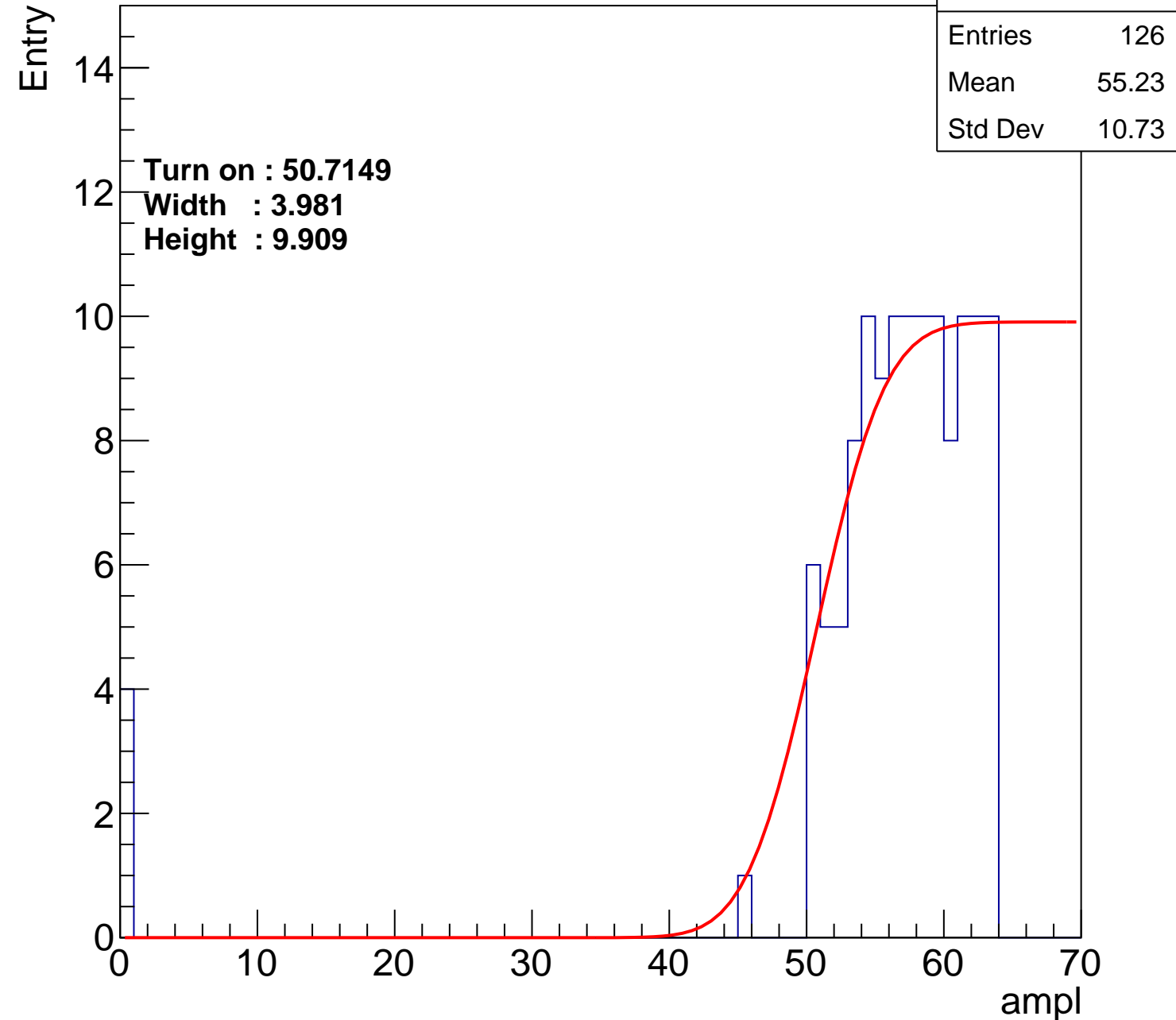
Width : 3.981

Height : 9.909

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch46

calib_packv5_040323_1717.root, FC#2, port C3

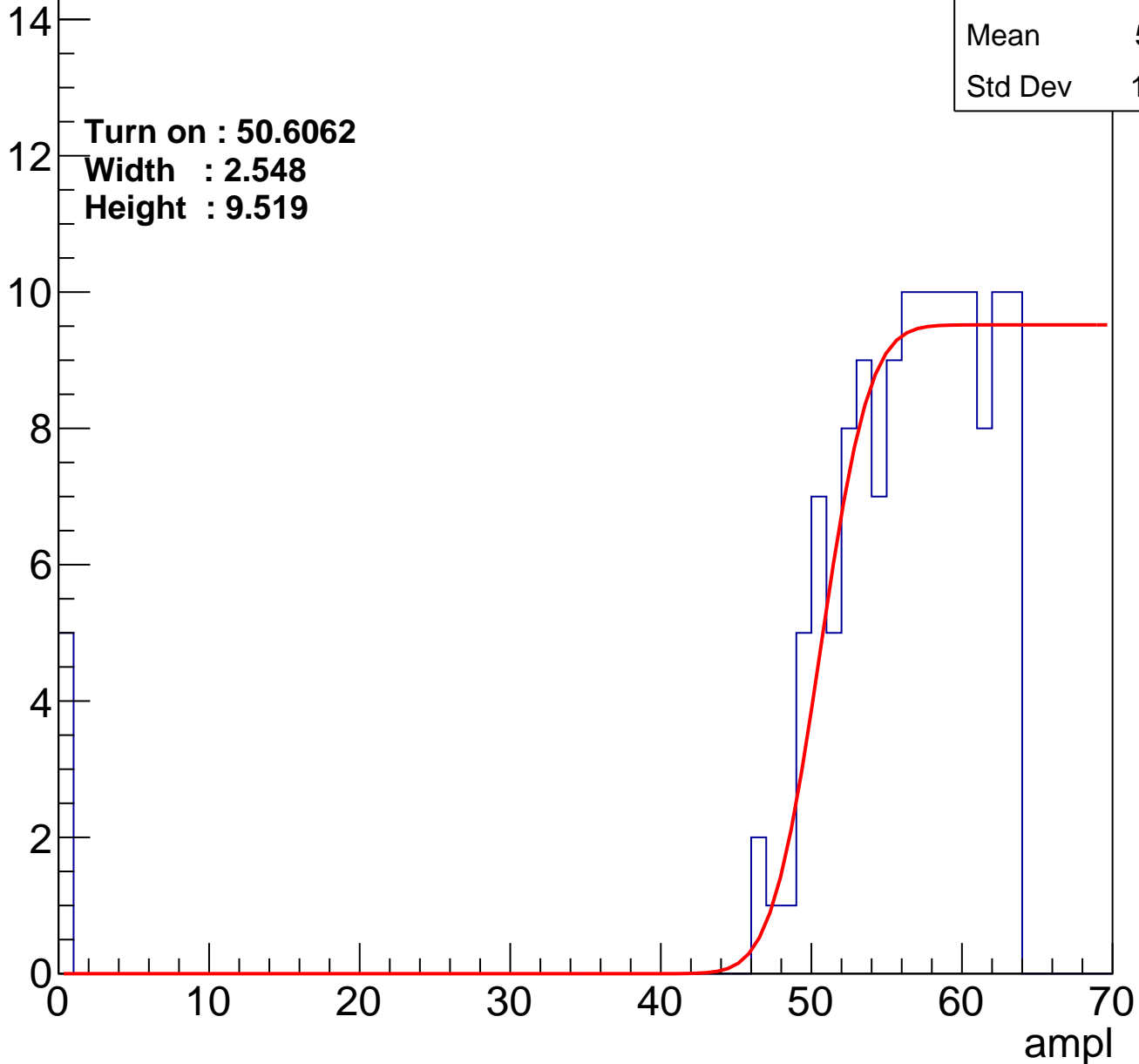
Entries	137
Mean	54.31
Std Dev	11.42

Turn on : 50.6062

Width : 2.548

Height : 9.519

Entry



B0L103S, U12-ch47

calib_packv5_040323_1717.root, FC#2, port C3

Entries	138
Mean	55.63
Std Dev	8.001

Turn on : 50.9785

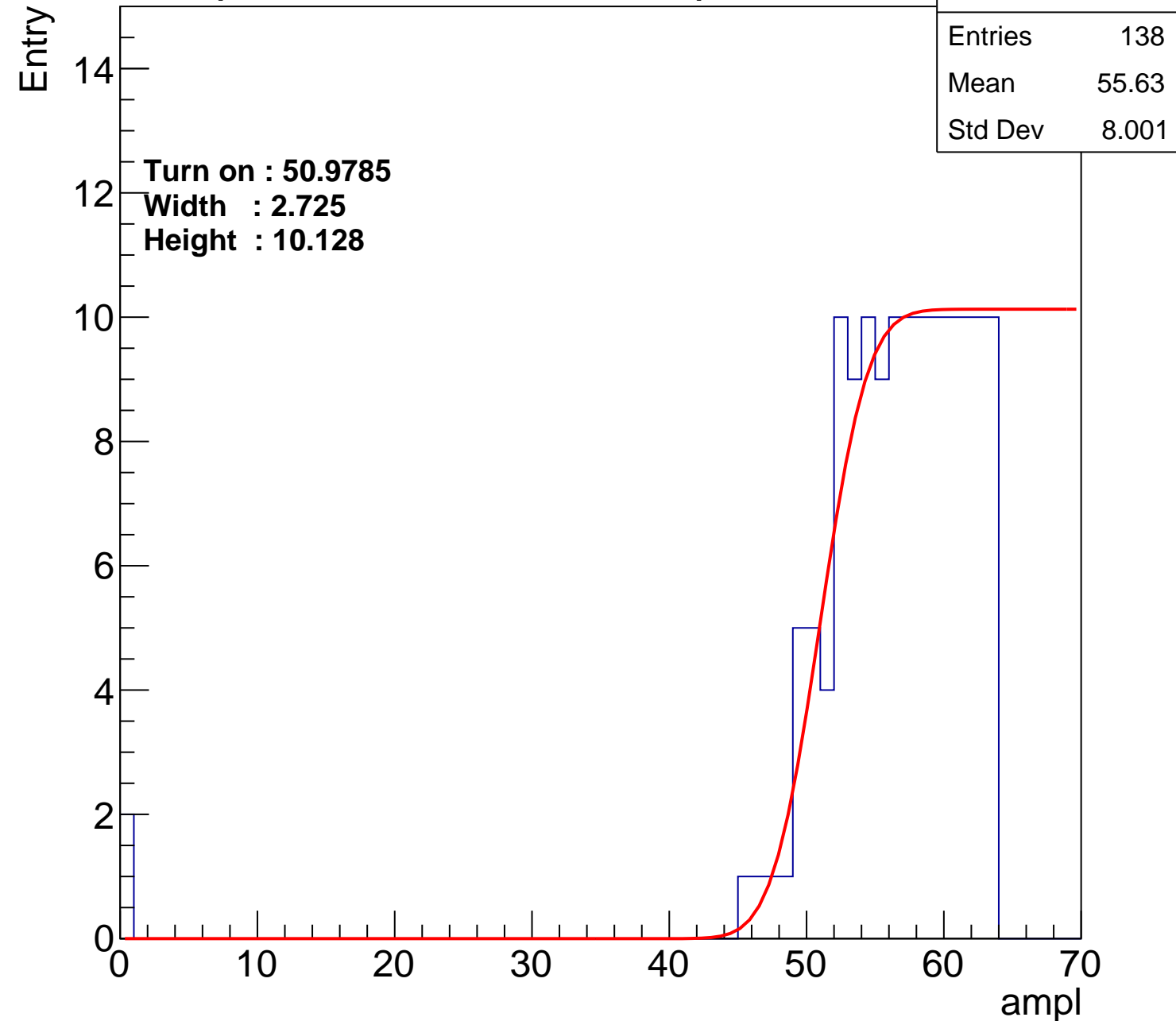
Width : 2.725

Height : 10.128

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch48

calib_packv5_040323_1717.root, FC#2, port C3

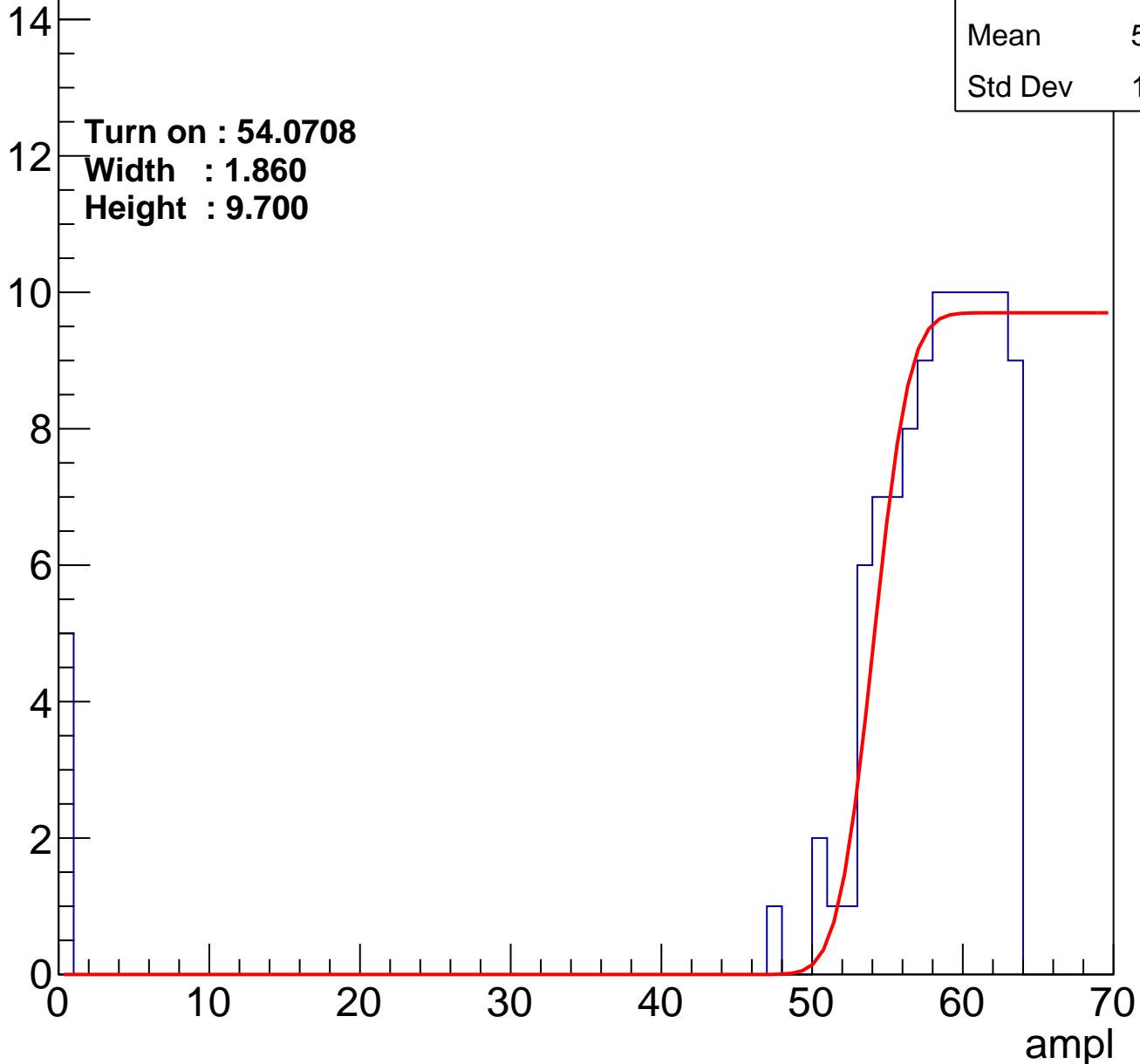
Entries	106
Mean	55.27
Std Dev	12.76

Turn on : 54.0708

Width : 1.860

Height : 9.700

Entry



calib_packv5_040323_1717.root, FC#2, port C3

Entries	116
Mean	56.09
Std Dev	9.834

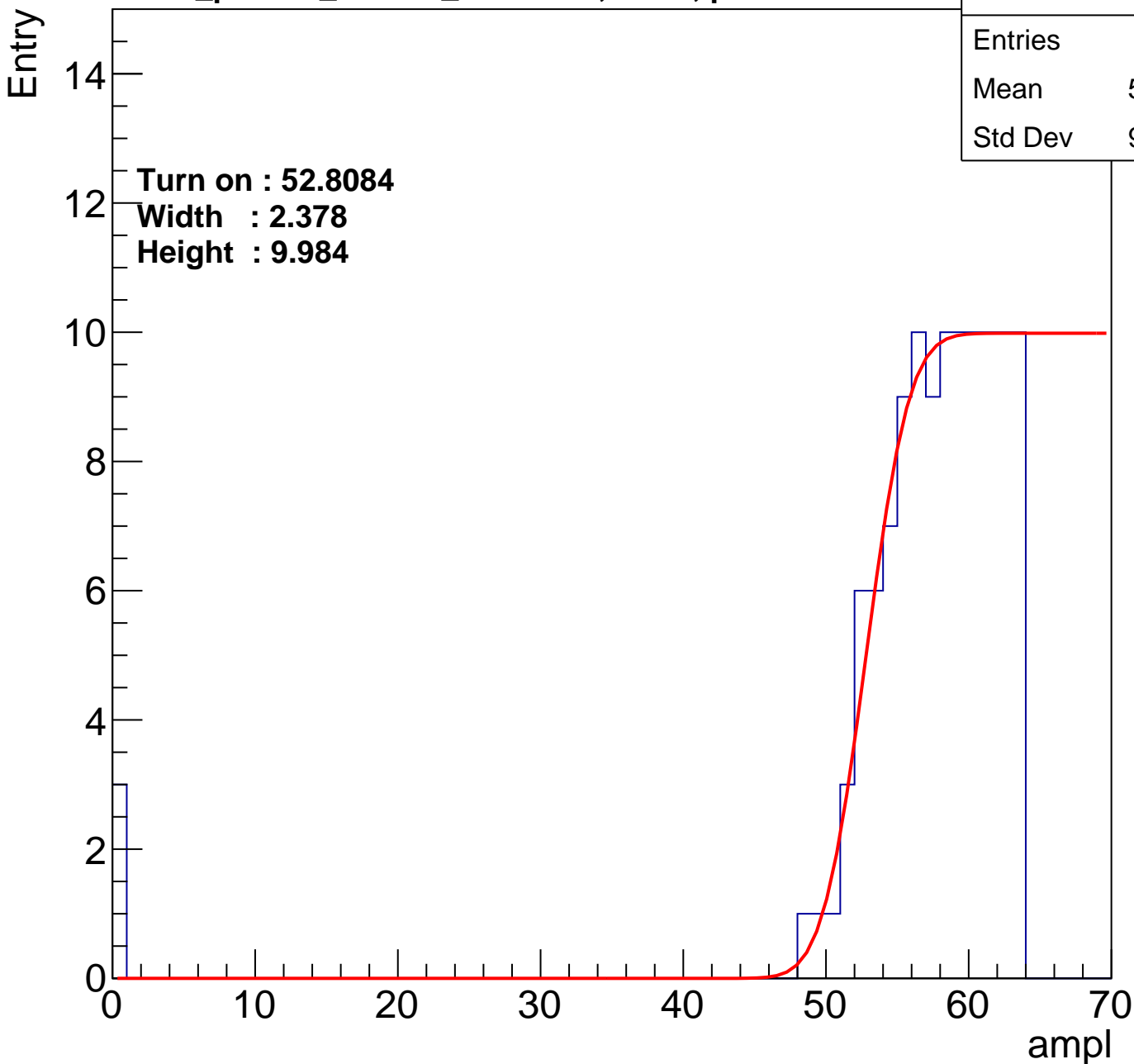
Entries	116
Mean	56.09
Std Dev	9.834

Mean	56.09
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Std Dev	9.834
---------	-------

Width : 2.378

Height : 9.984



B0L103S, U12-ch50

calib_packv5_040323_1717.root, FC#2, port C3

Entries	106
Mean	56.55
Std Dev	10.16

Turn on : 54.1243

Width : 2.193

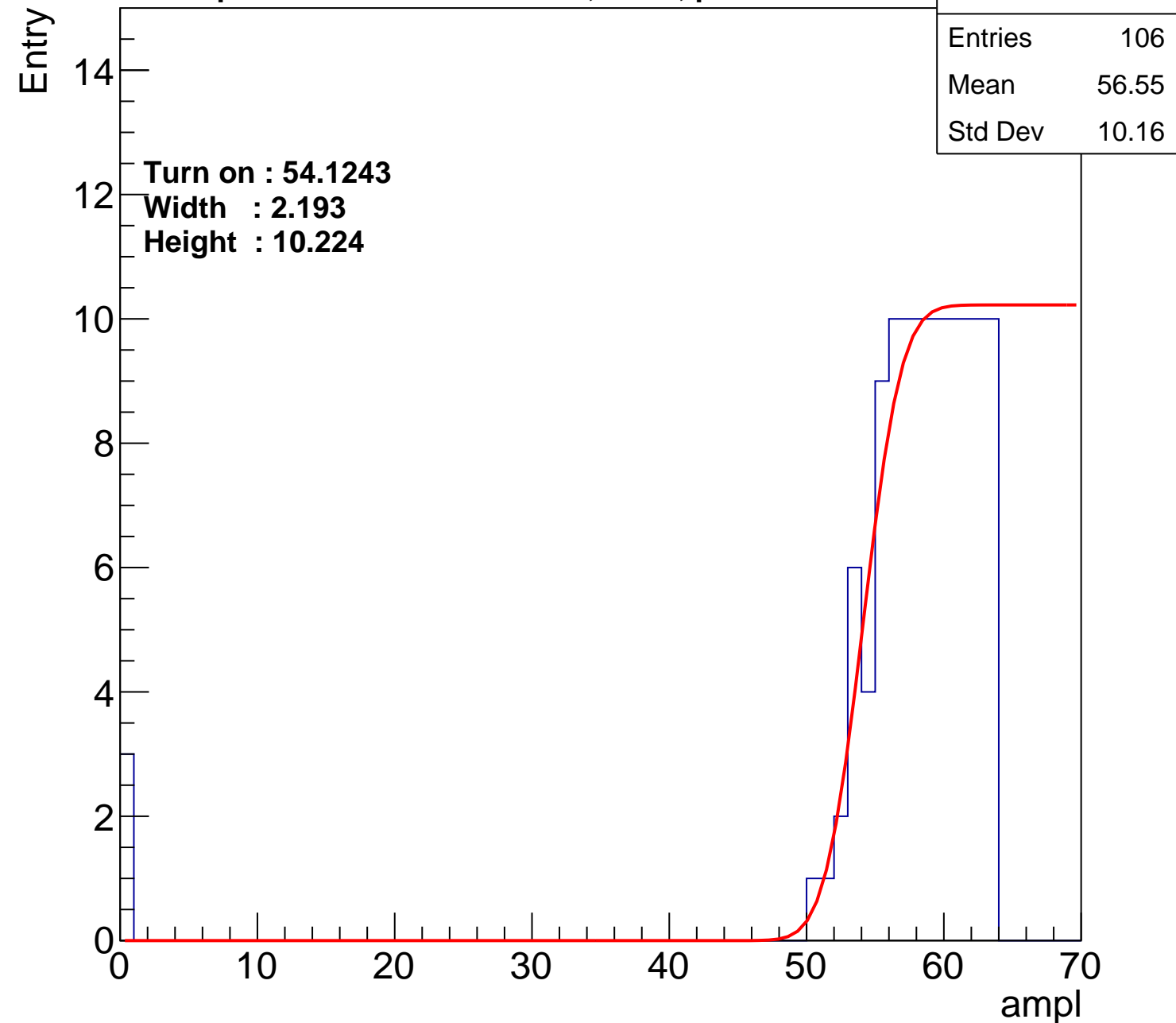
Height : 10.224

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B0L103S, U12-ch51

calib_packv5_040323_1717.root, FC#2, port C3

Entries	106
Mean	56.9
Std Dev	8.596

Turn on : 53.5241

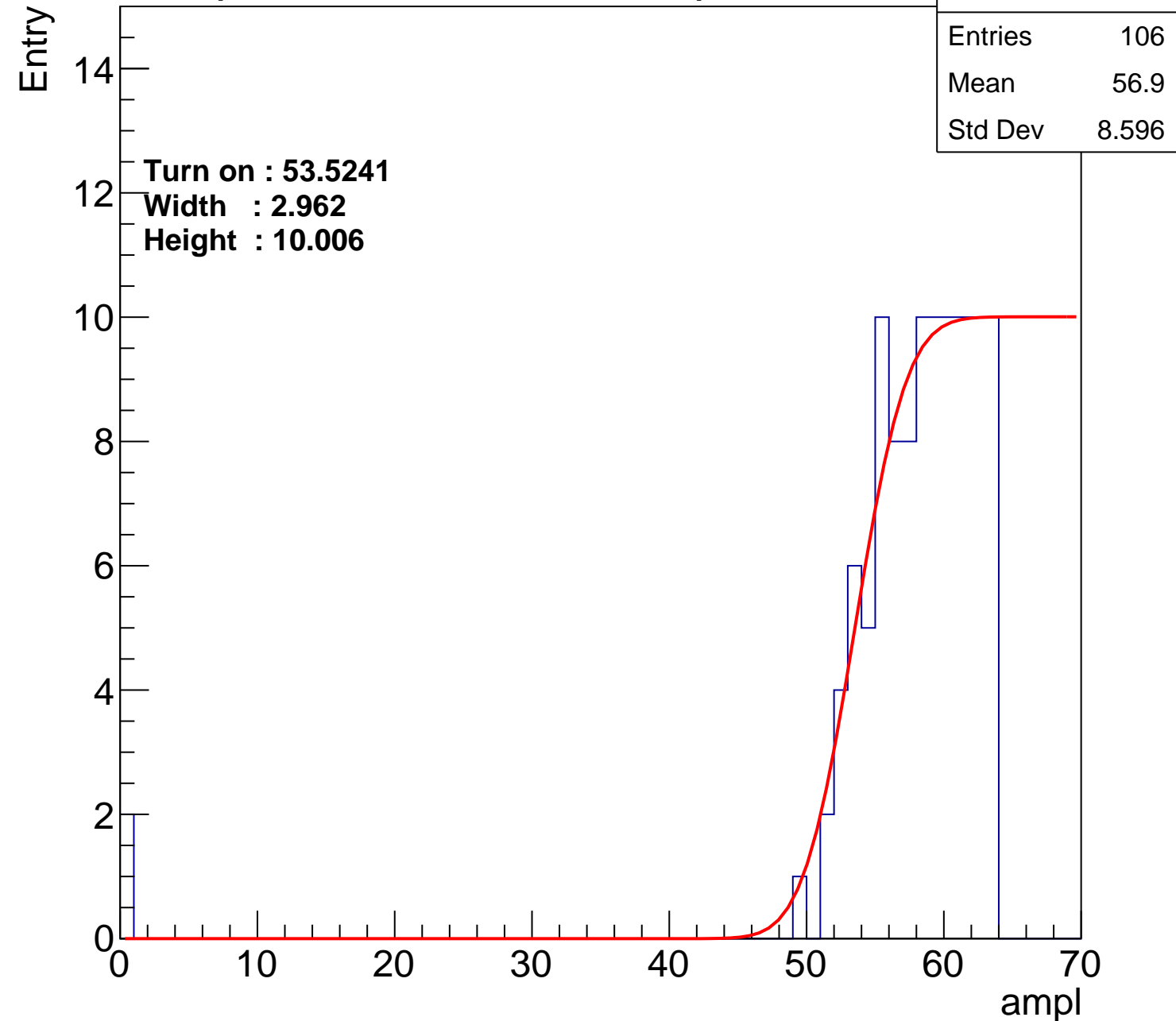
Width : 2.962

Height : 10.006

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch52

calib_packv5_040323_1717.root, FC#2, port C3

Entries	127
Mean	56
Std Dev	8.208

Turn on : 52.0110

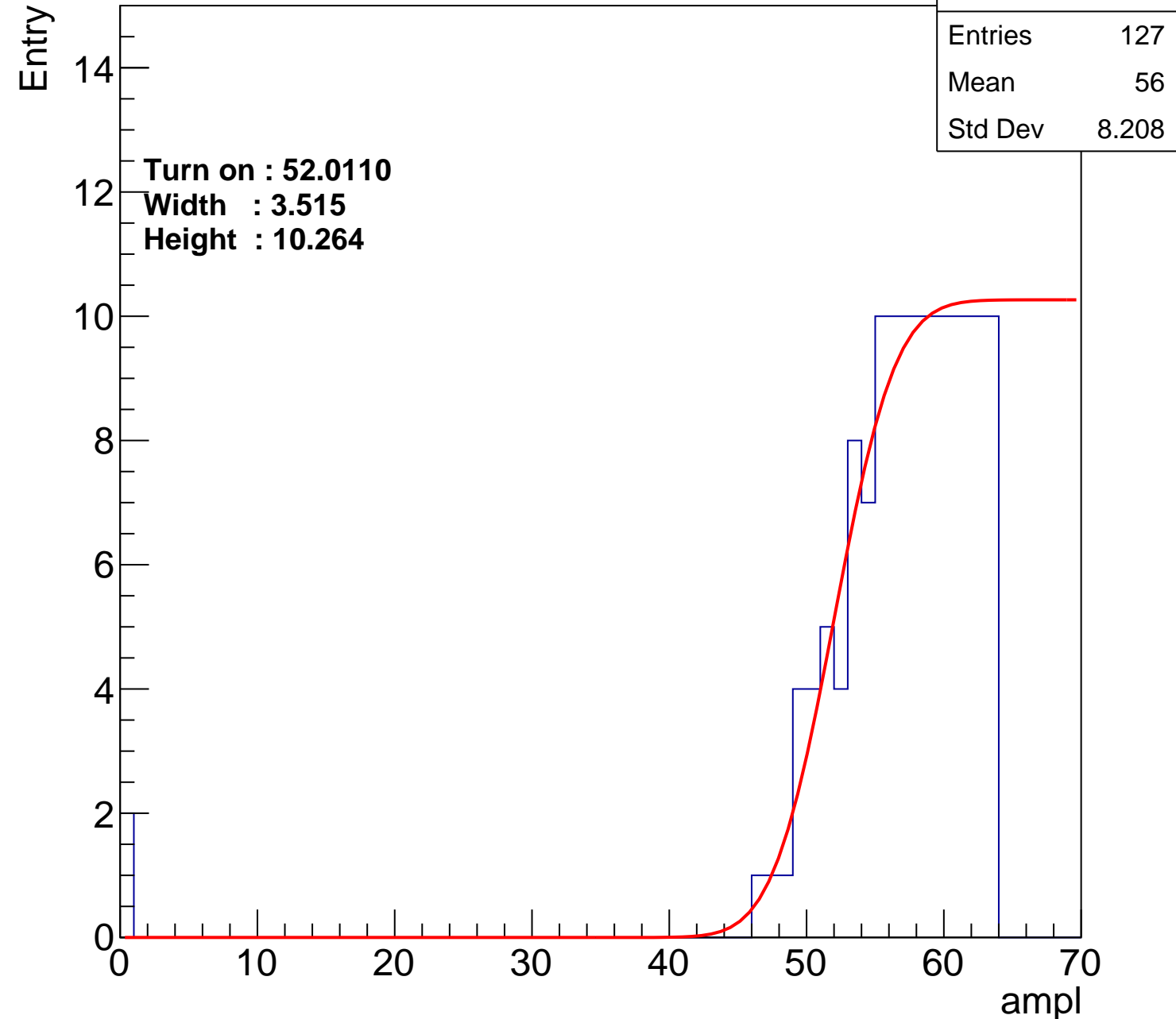
Width : 3.515

Height : 10.264

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch53

calib_packv5_040323_1717.root, FC#2, port C3

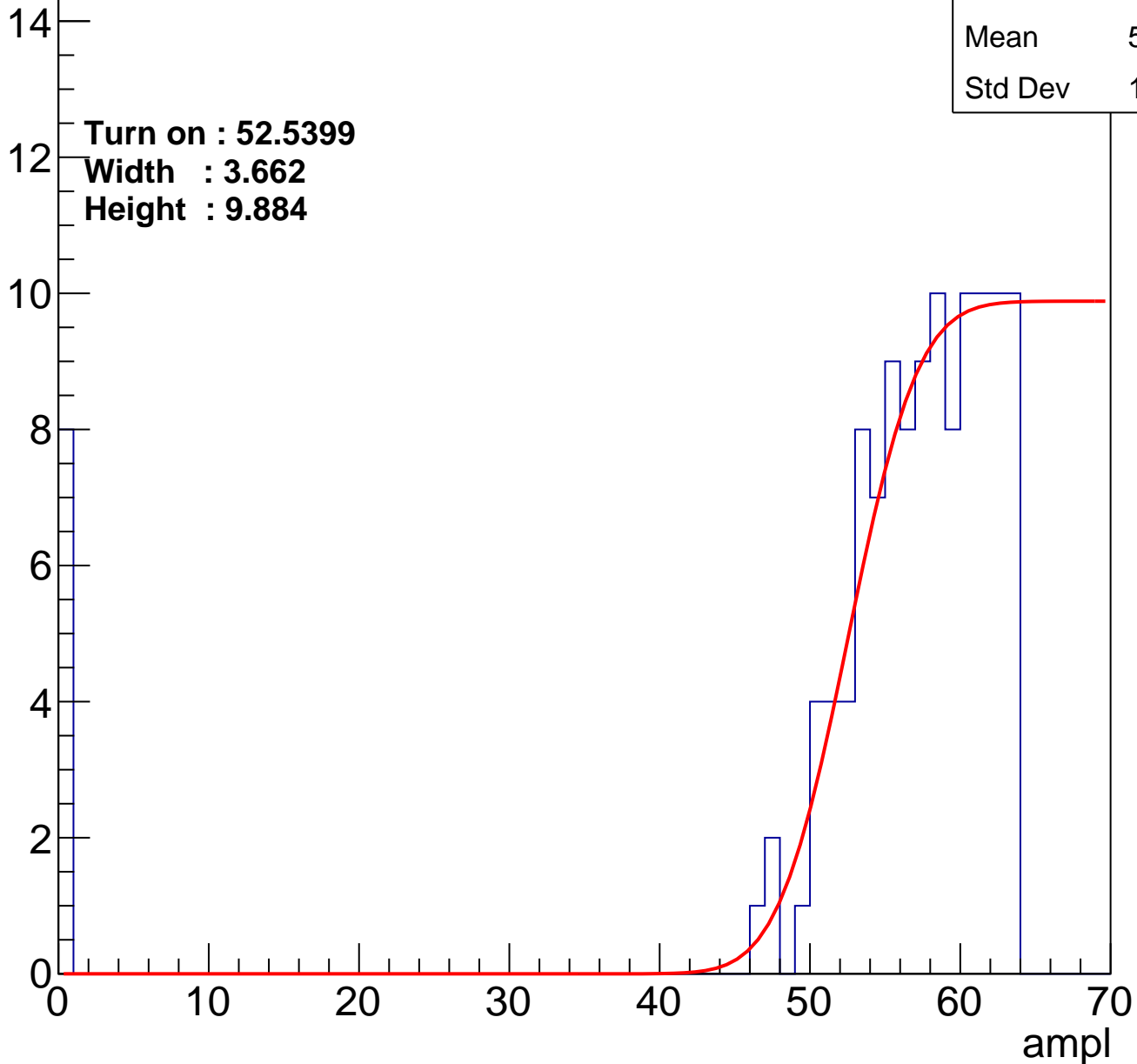
Entries	123
Mean	53.42
Std Dev	14.64

Turn on : 52.5399

Width : 3.662

Height : 9.884

Entry



B0L103S, U12-ch54

calib_packv5_040323_1717.root, FC#2, port C3

Entries	111
Mean	56.54
Std Dev	8.565

Turn on : 53.2325

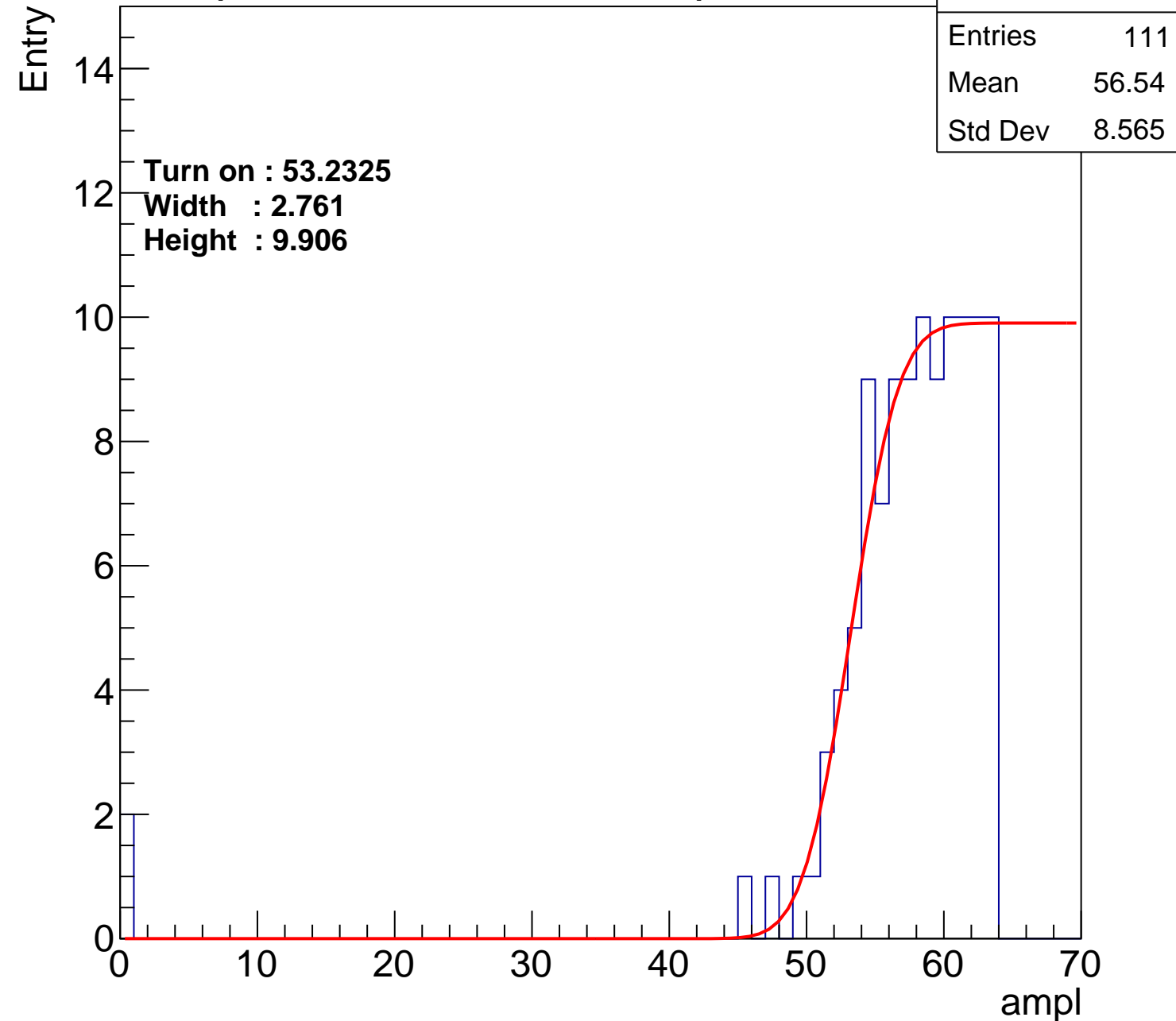
Width : 2.761

Height : 9.906

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch55

calib_packv5_040323_1717.root, FC#2, port C3

Entries	91
Mean	57.26
Std Dev	9.151

Turn on : 55.7675

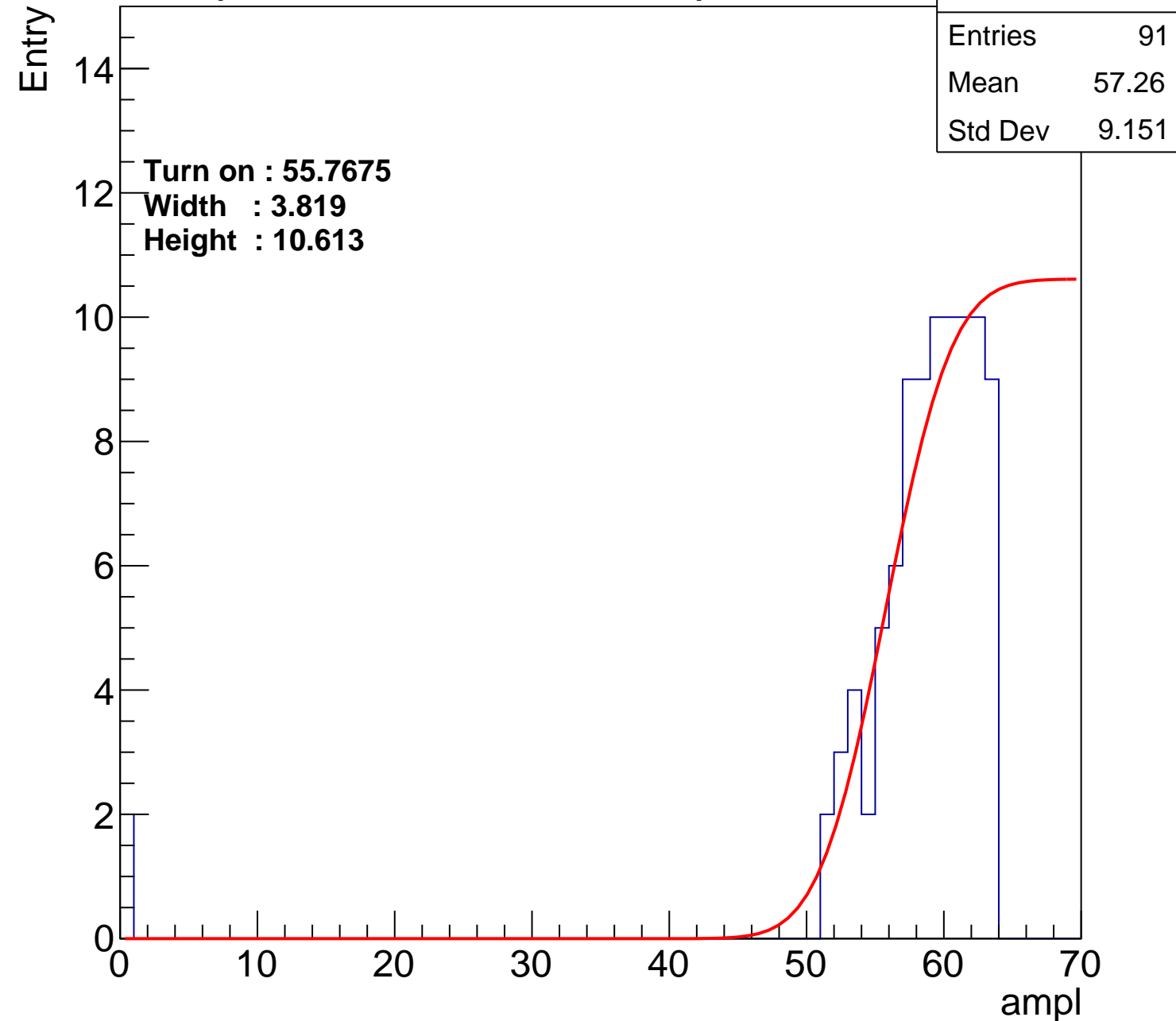
Width : 3.819

Height : 10.613

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch56

calib_packv5_040323_1717.root, FC#2, port C3

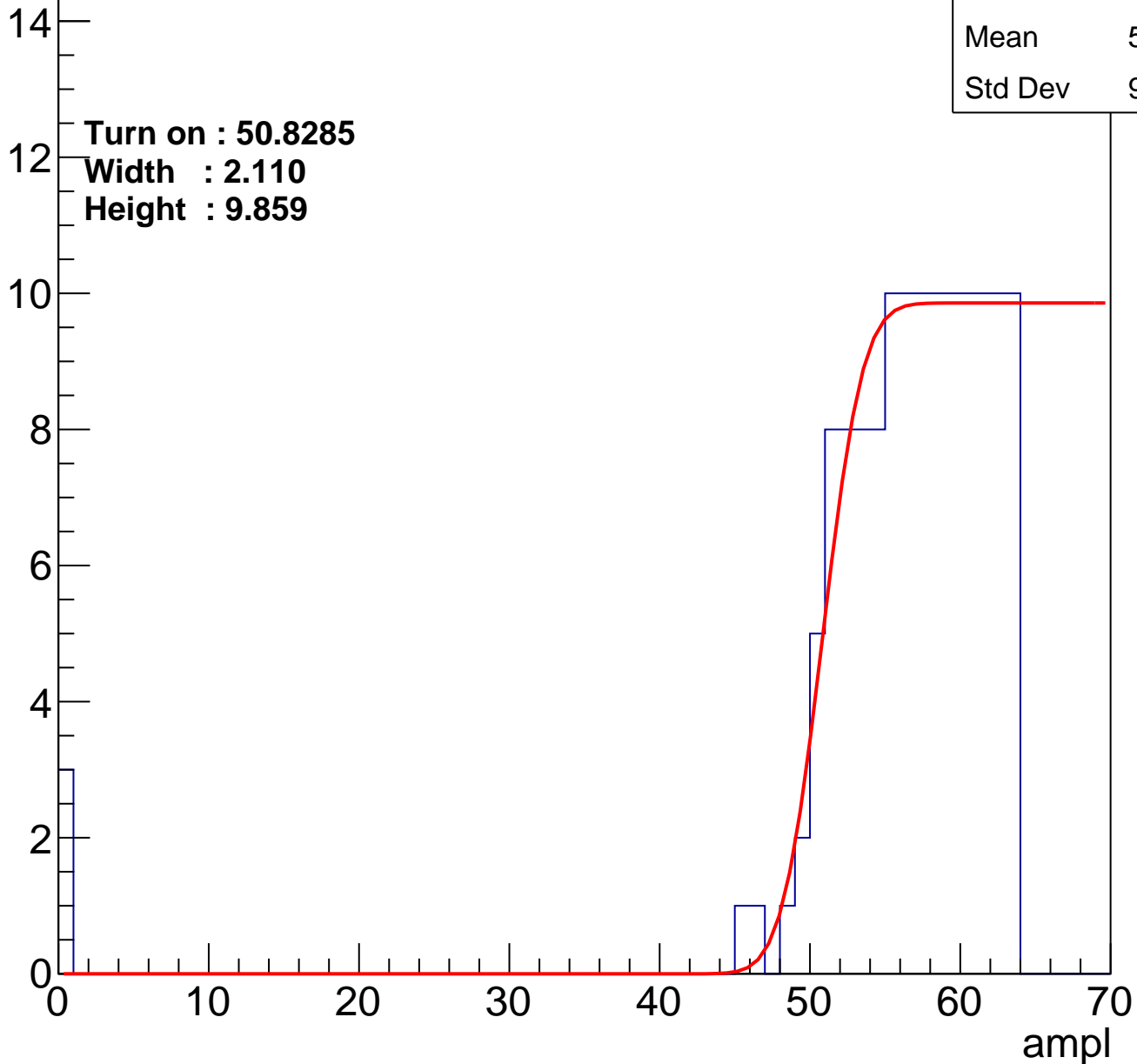
Entries	135
Mean	55.39
Std Dev	9.334

Turn on : 50.8285

Width : 2.110

Height : 9.859

Entry



B0L103S, U12-ch57

calib_packv5_040323_1717.root, FC#2, port C3

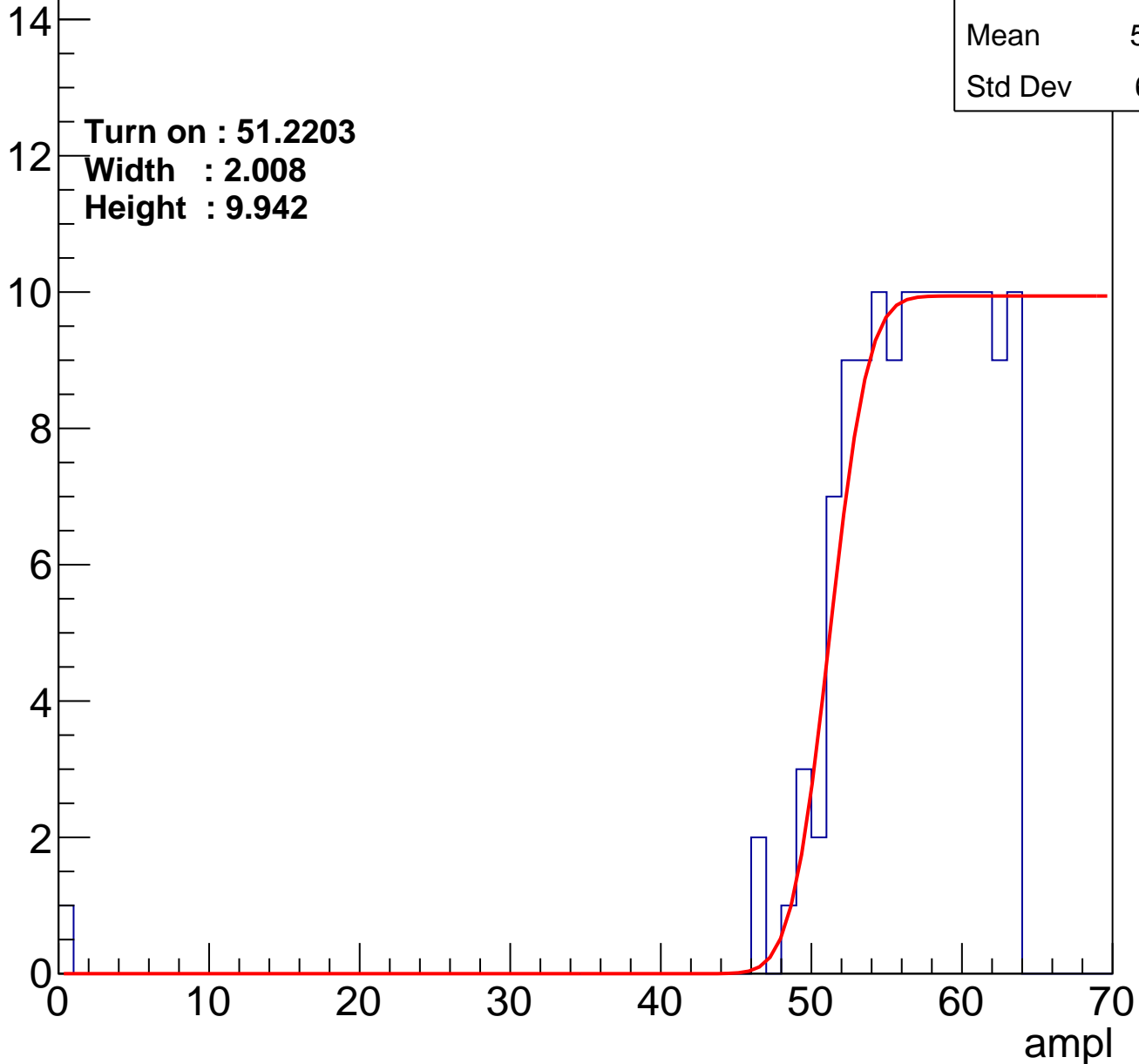
Entries	132
Mean	56.23
Std Dev	6.411

Turn on : 51.2203

Width : 2.008

Height : 9.942

Entry



B0L103S, U12-ch58

calib_packv5_040323_1717.root, FC#2, port C3

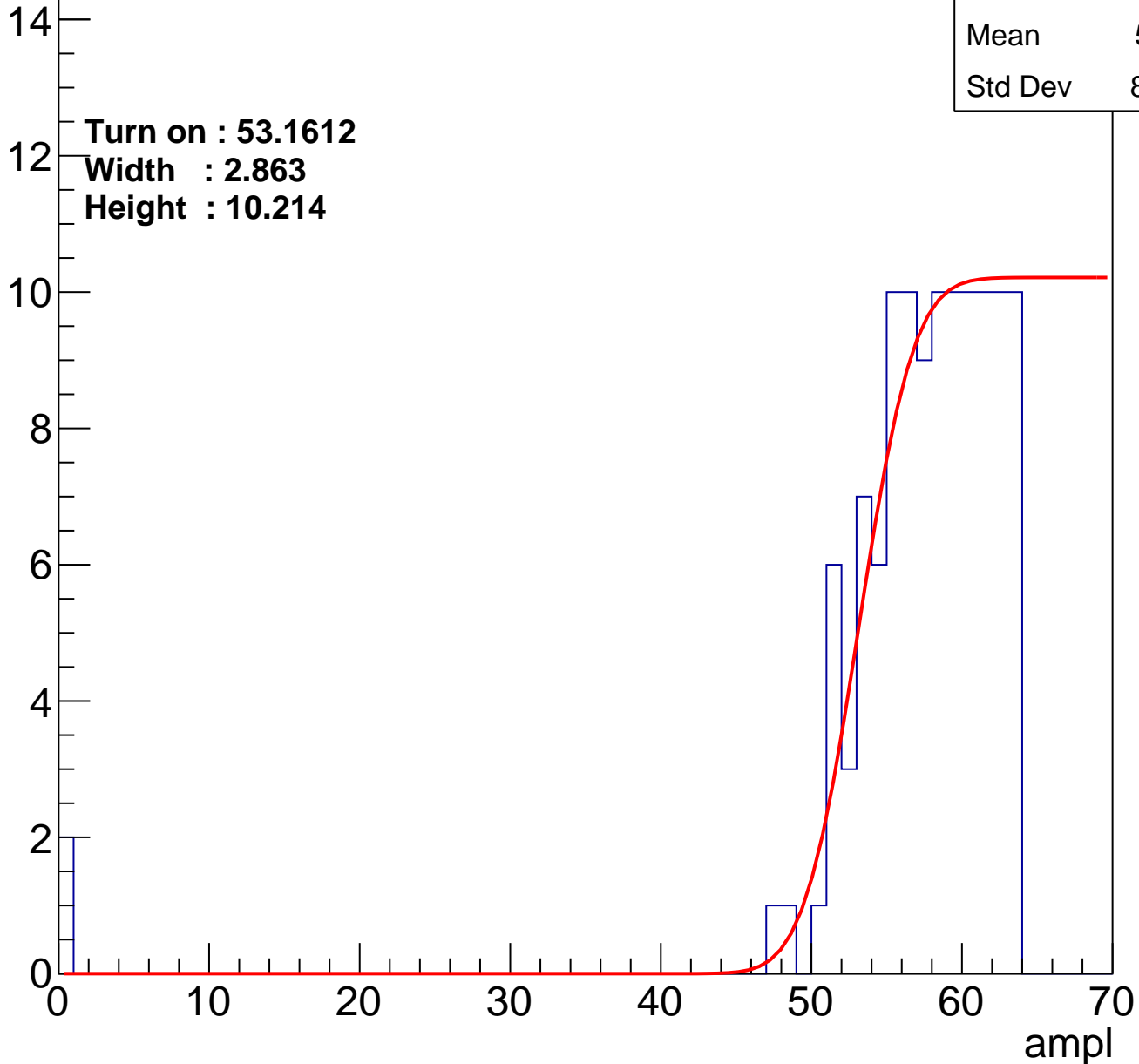
Entries	116
Mean	56.51
Std Dev	8.365

Turn on : 53.1612

Width : 2.863

Height : 10.214

Entry



B0L103S, U12-ch59

calib_packv5_040323_1717.root, FC#2, port C3

Entries	128
Mean	56.45
Std Dev	6.461

Turn on : 51.3065

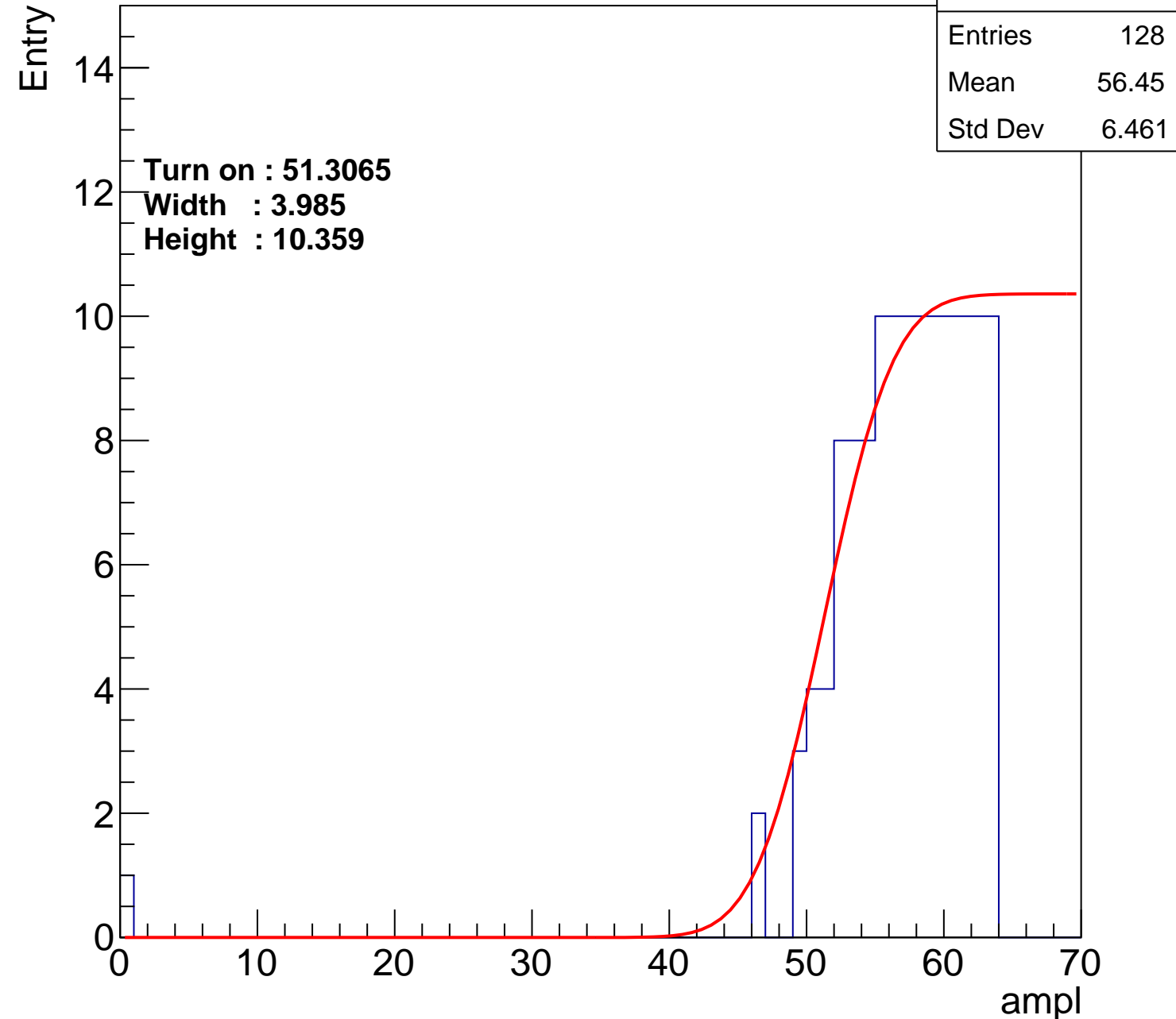
Width : 3.985

Height : 10.359

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch60

calib_packv5_040323_1717.root, FC#2, port C3

Entries	142
Mean	53.62
Std Dev	12.96

Turn on : 51.1000

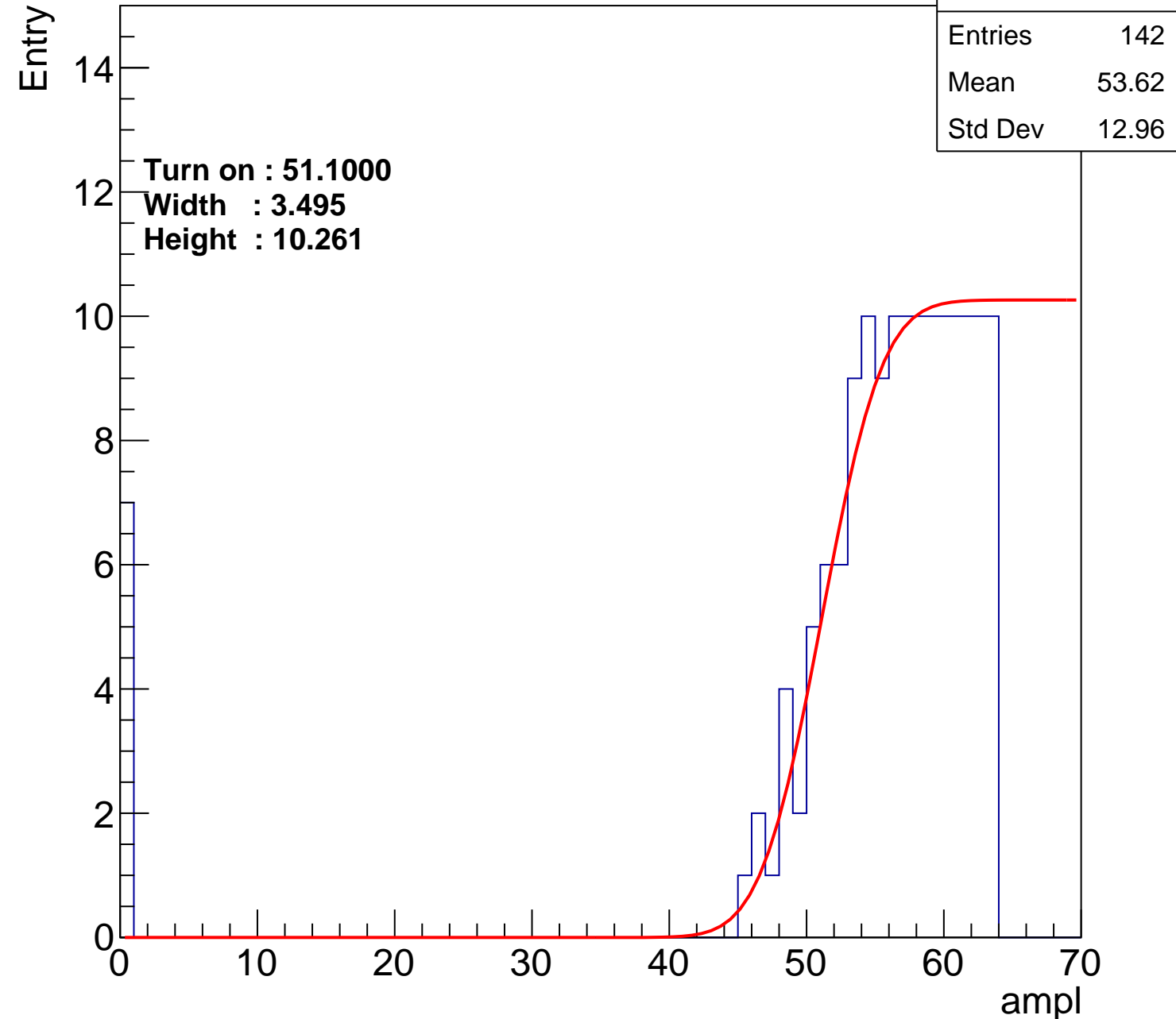
Width : 3.495

Height : 10.261

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch61

calib_packv5_040323_1717.root, FC#2, port C3

Entries	131
Mean	56.09
Std Dev	6.597

Turn on : 50.9528

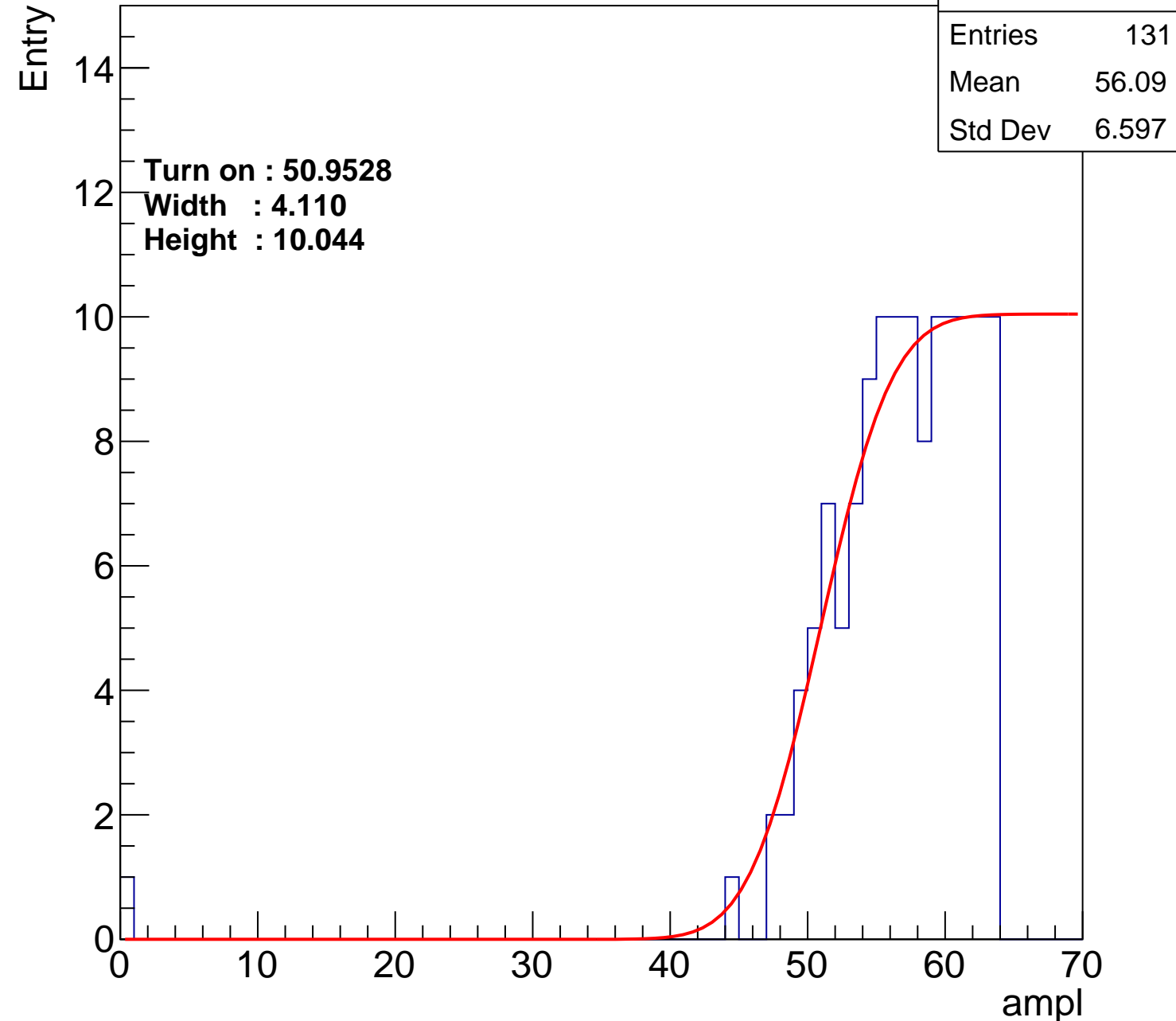
Width : 4.110

Height : 10.044

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch62

calib_packv5_040323_1717.root, FC#2, port C3

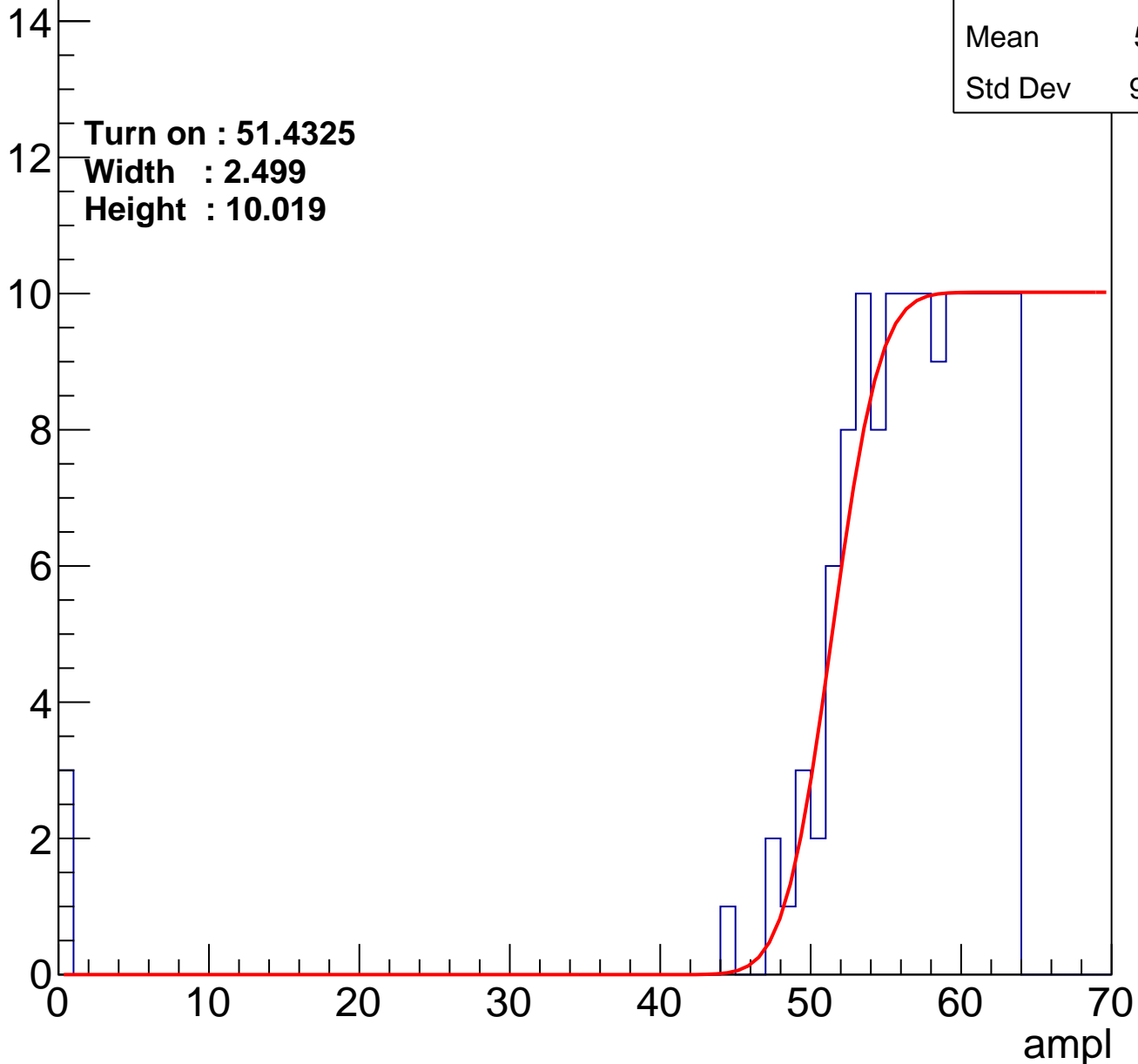
Entries	133
Mean	55.41
Std Dev	9.402

Turn on : 51.4325

Width : 2.499

Height : 10.019

Entry



B0L103S, U12-ch63

calib_packv5_040323_1717.root, FC#2, port C3

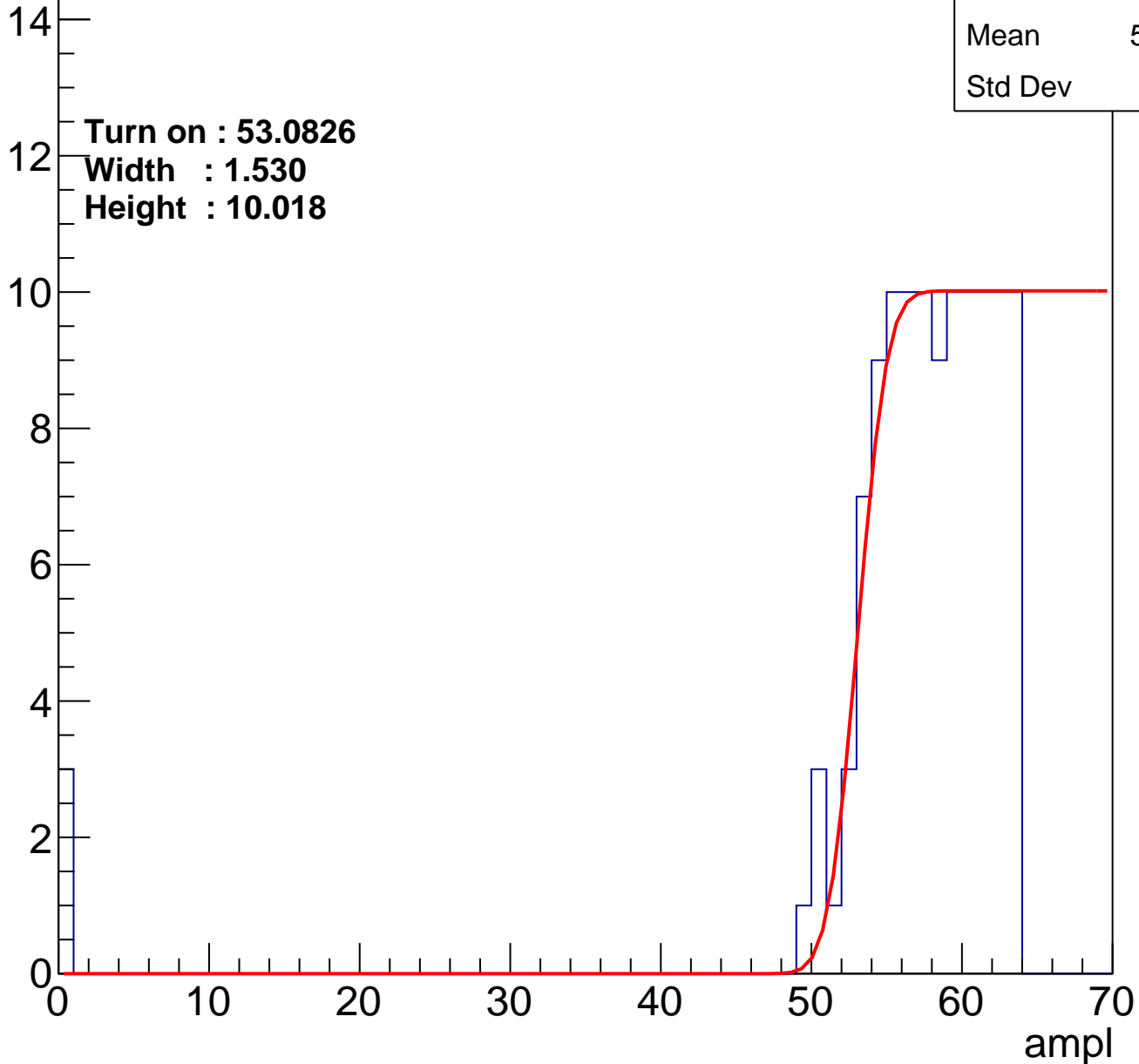
Entries	116
Mean	56.16
Std Dev	9.8

Turn on : 53.0826

Width : 1.530

Height : 10.018

Entry



B0L103S, U12-ch64

calib_packv5_040323_1717.root, FC#2, port C3

Entries	139
Mean	55.92
Std Dev	6.496

Turn on : 49.8859

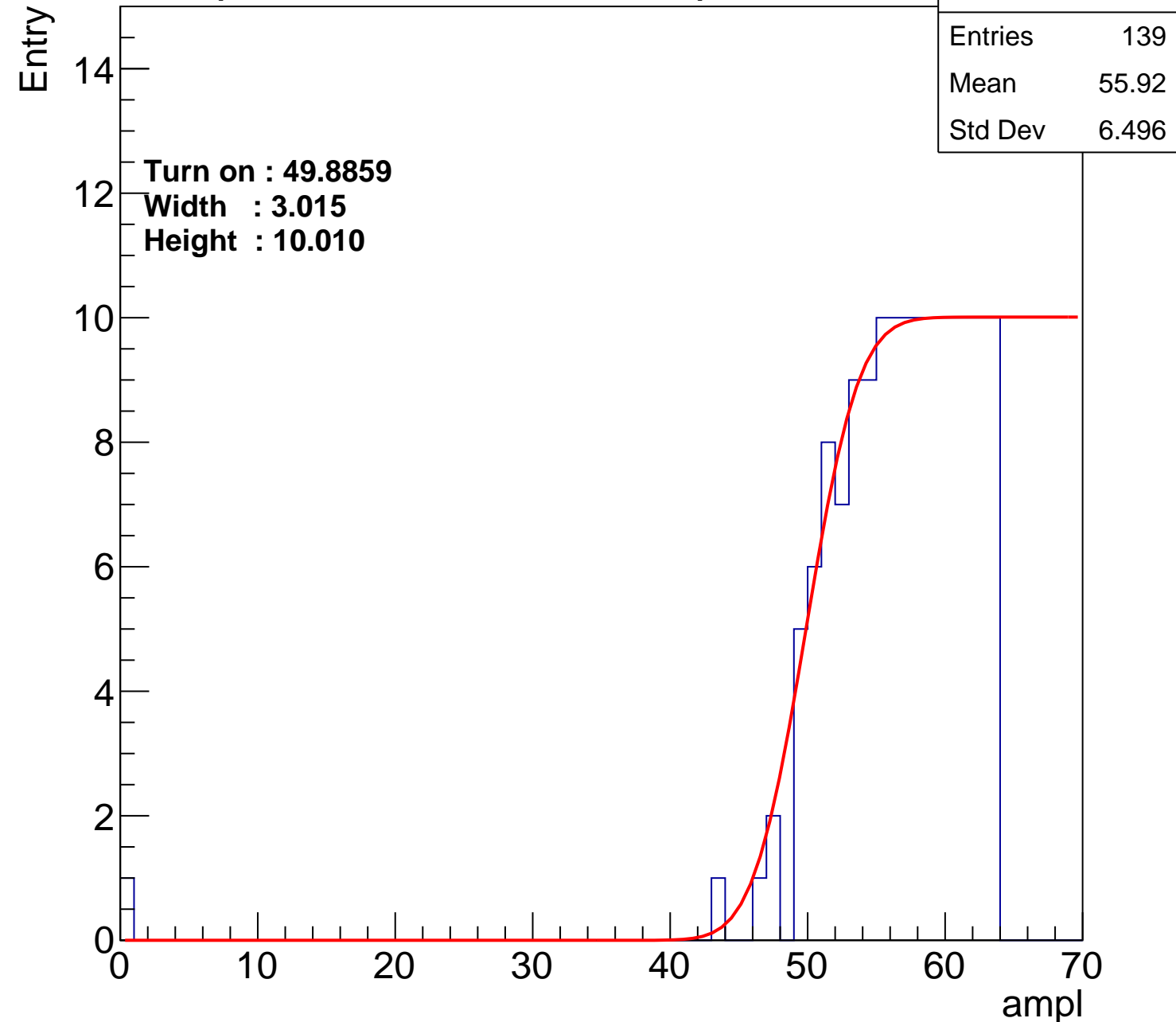
Width : 3.015

Height : 10.010

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch65

calib_packv5_040323_1717.root, FC#2, port C3

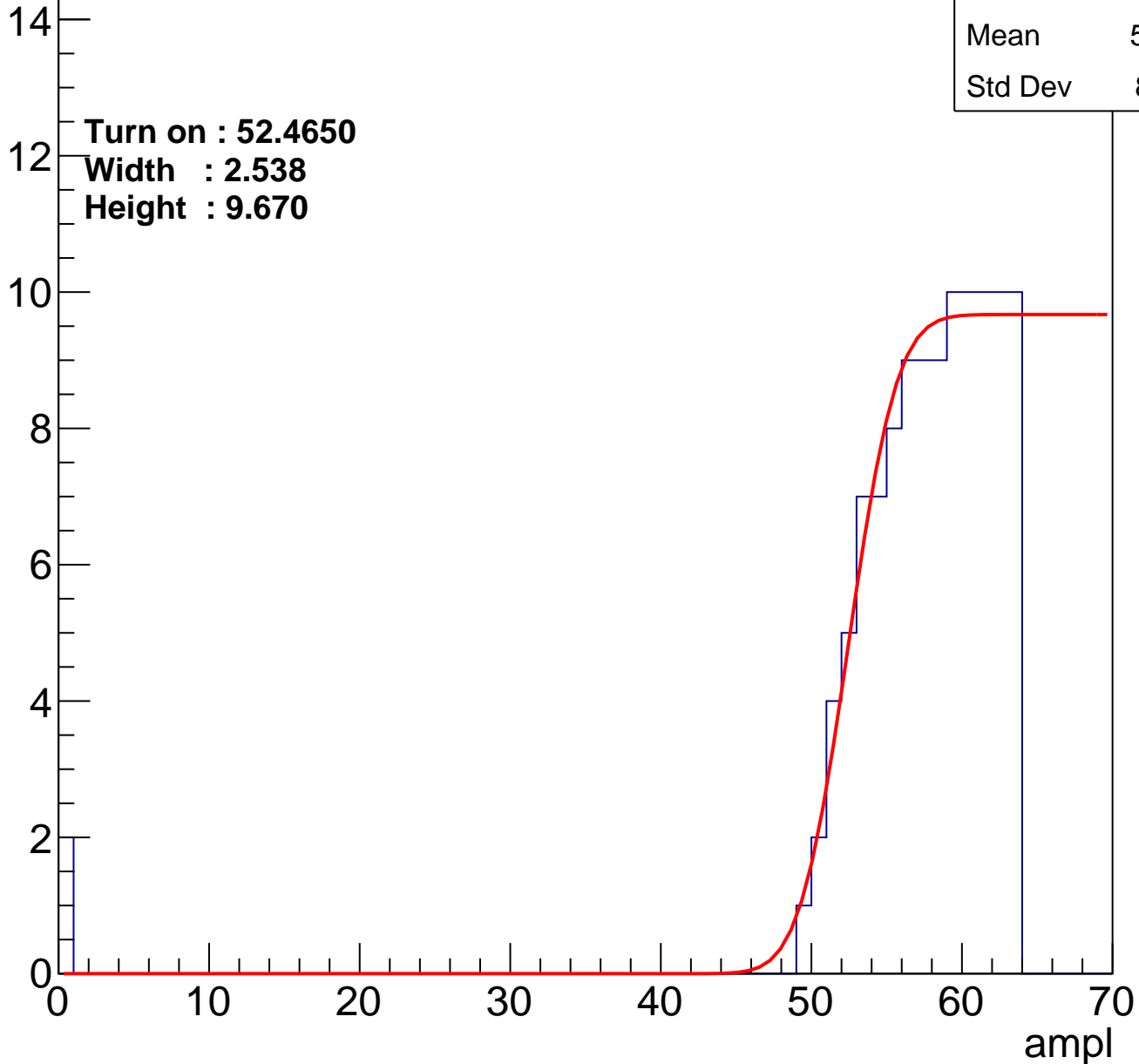
Entries	113
Mean	56.56
Std Dev	8.431

Turn on : 52.4650

Width : 2.538

Height : 9.670

Entry



B0L103S, U12-ch66

calib_packv5_040323_1717.root, FC#2, port C3

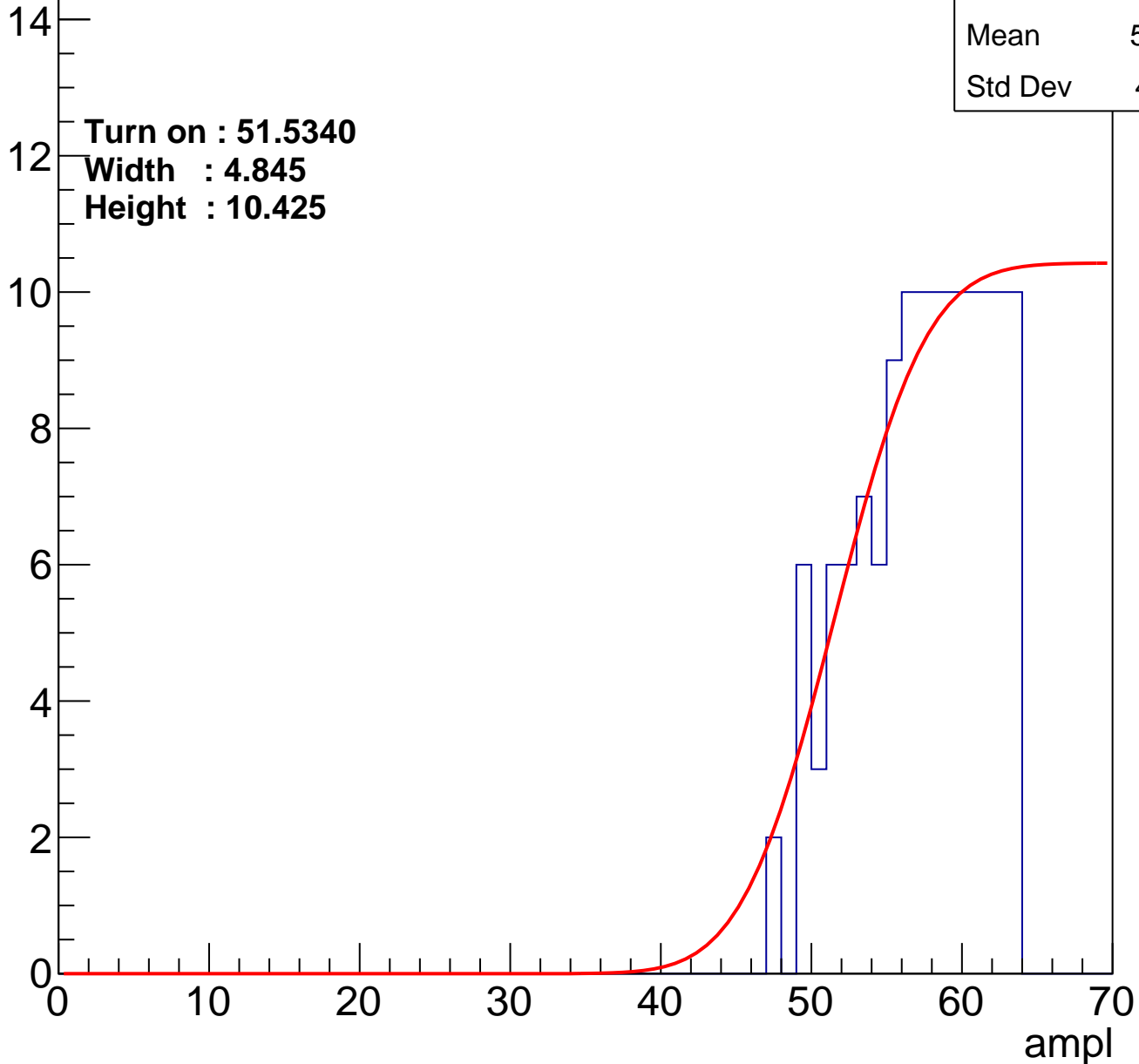
Entries	125
Mean	56.85
Std Dev	4.211

Turn on : 51.5340

Width : 4.845

Height : 10.425

Entry



B0L103S, U12-ch67

calib_packv5_040323_1717.root, FC#2, port C3

Entries	139
Mean	55.12
Std Dev	9.277

Turn on : 50.1276

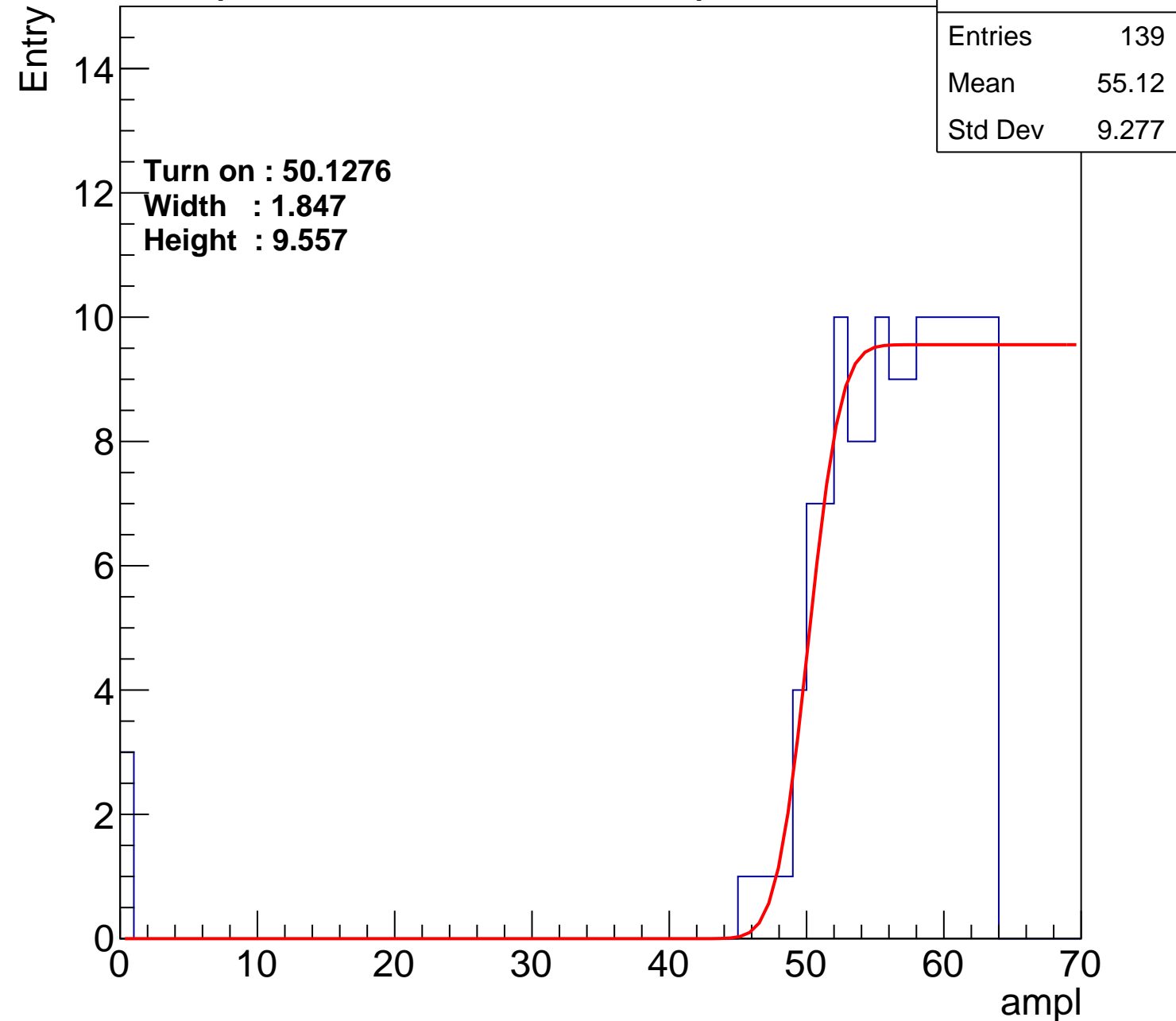
Width : 1.847

Height : 9.557

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch68

calib_packv5_040323_1717.root, FC#2, port C3

Entries	134
Mean	54.57
Std Dev	11.52

Turn on : 51.1017

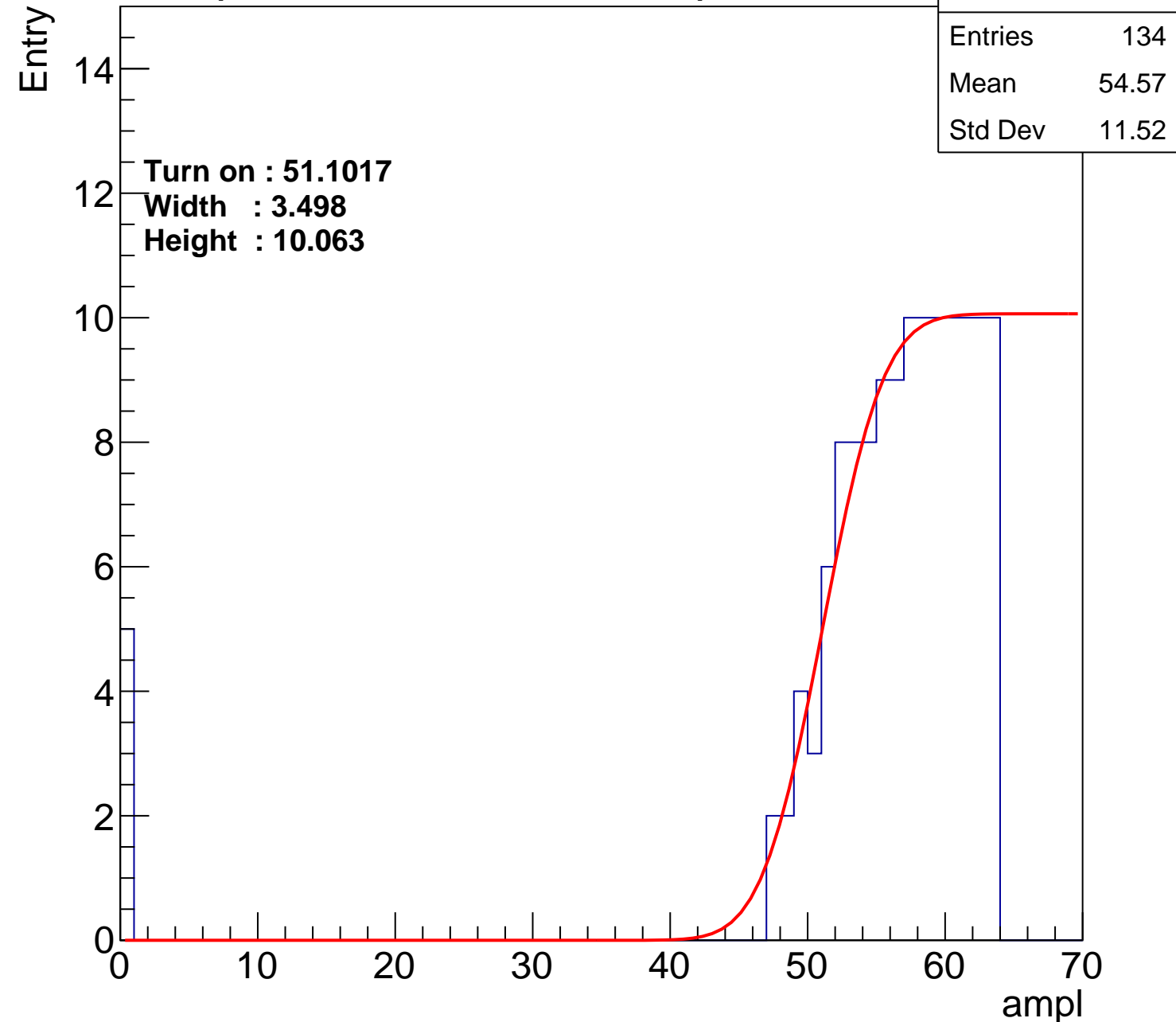
Width : 3.498

Height : 10.063

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch69

calib_packv5_040323_1717.root, FC#2, port C3

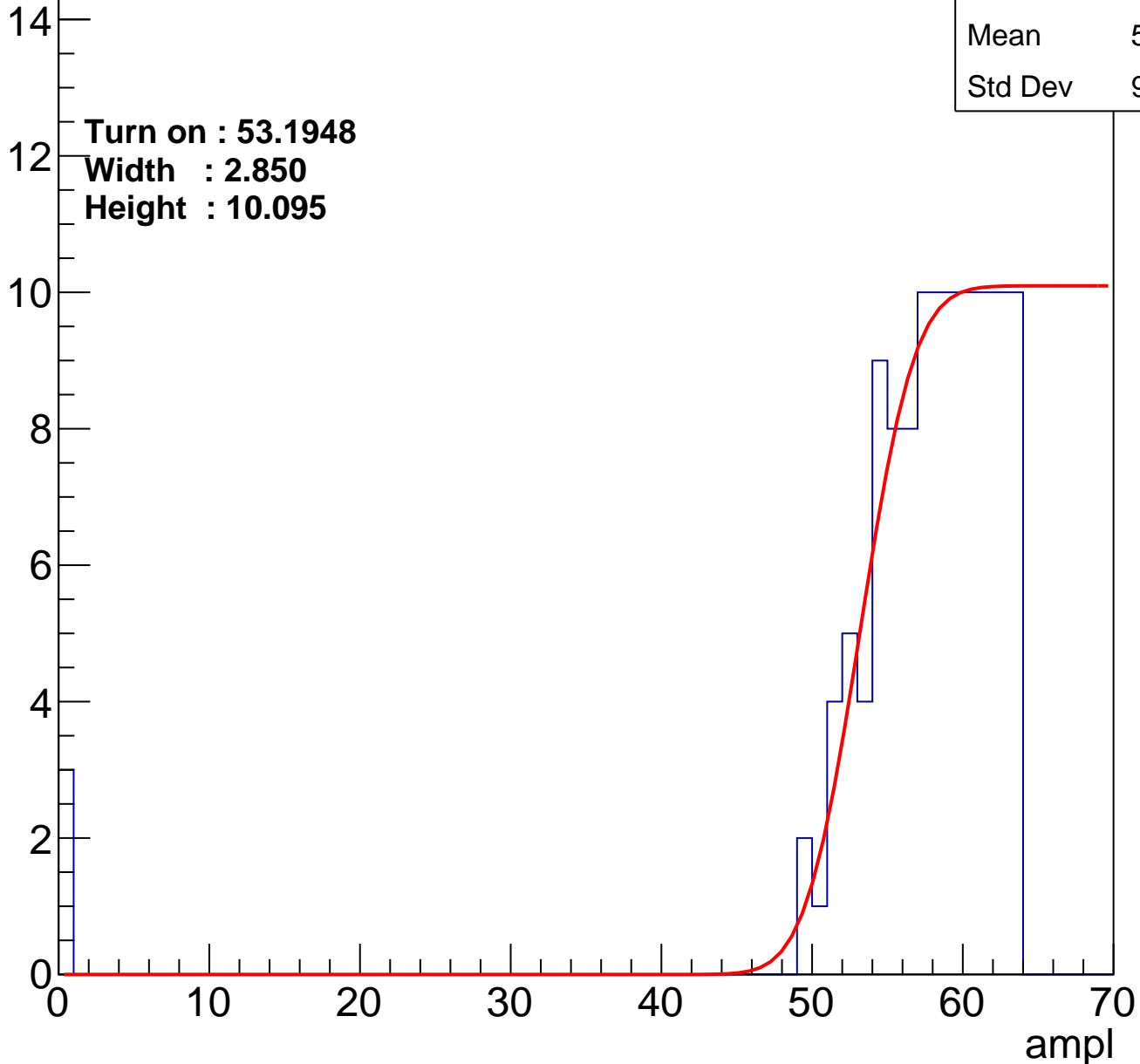
Entries	114
Mean	56.12
Std Dev	9.912

Turn on : 53.1948

Width : 2.850

Height : 10.095

Entry



B0L103S, U12-ch70

calib_packv5_040323_1717.root, FC#2, port C3

Entries	119
Mean	55.27
Std Dev	11.03

Turn on : 52.7882

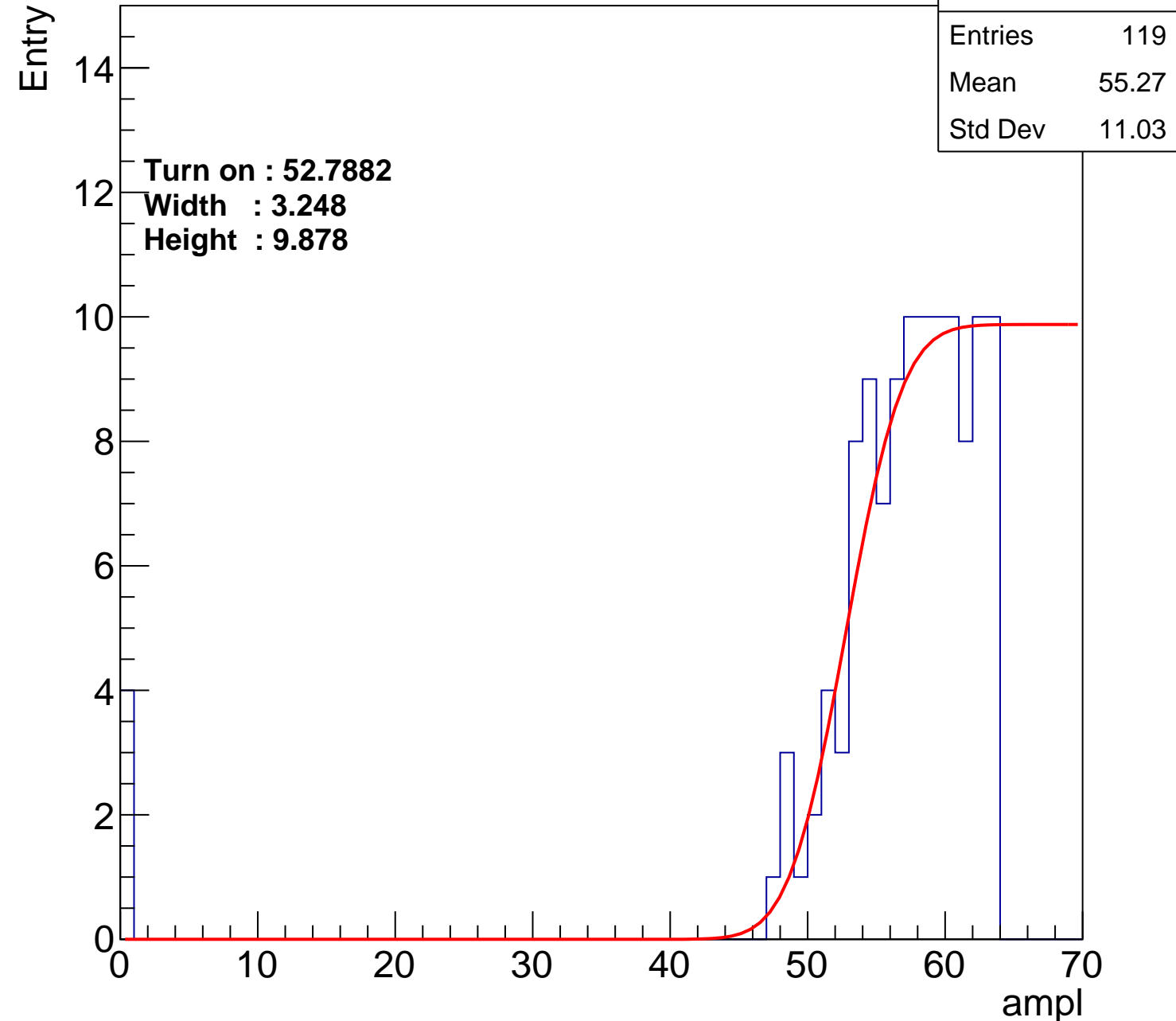
Width : 3.248

Height : 9.878

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch71

calib_packv5_040323_1717.root, FC#2, port C3

Entries	115
Mean	55.04
Std Dev	12.33

Turn on : 53.3844

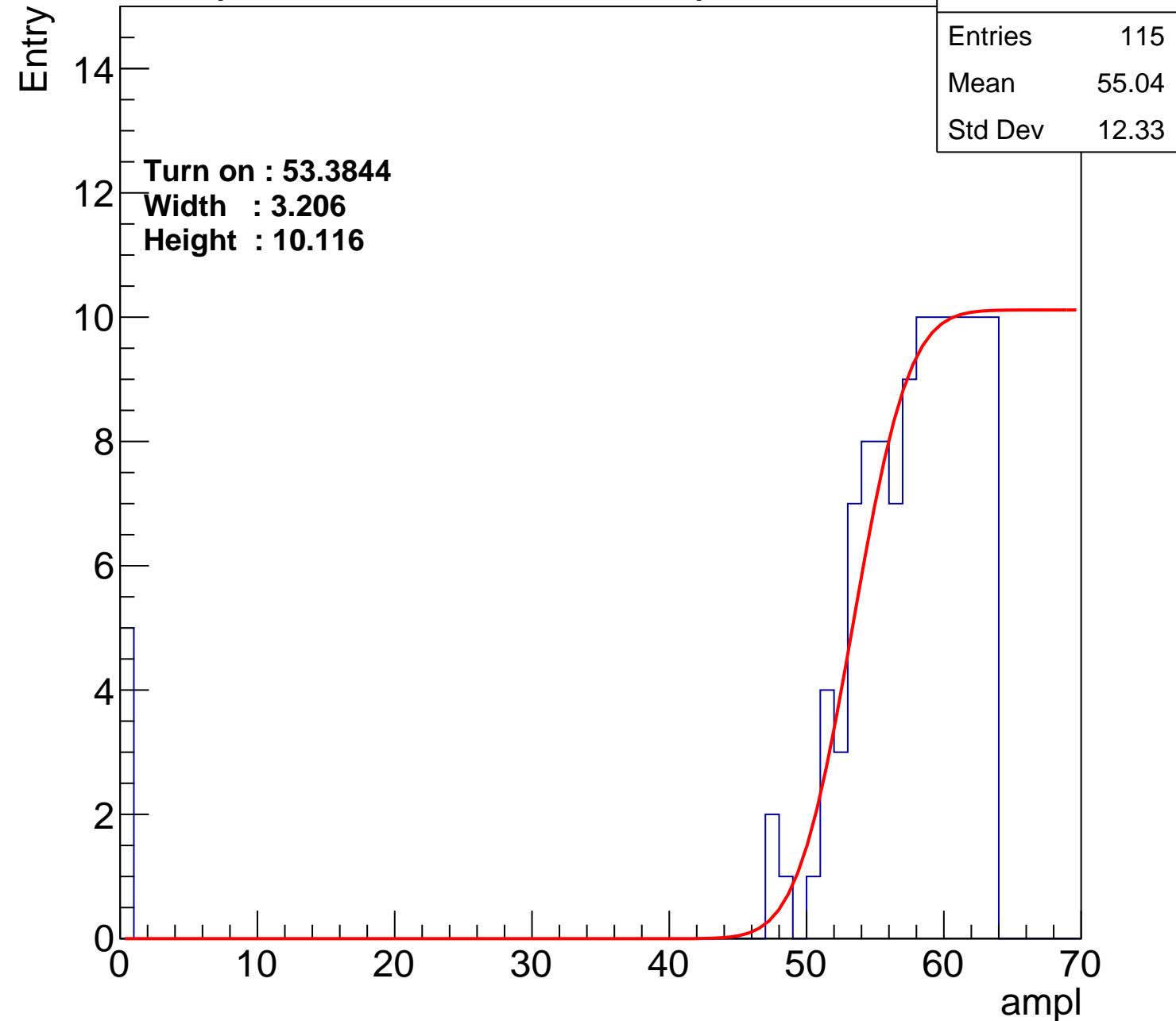
Width : 3.206

Height : 10.116

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch72

calib_packv5_040323_1717.root, FC#2, port C3

Entries	117
Mean	54.98
Std Dev	12.23

Turn on : 53.2817

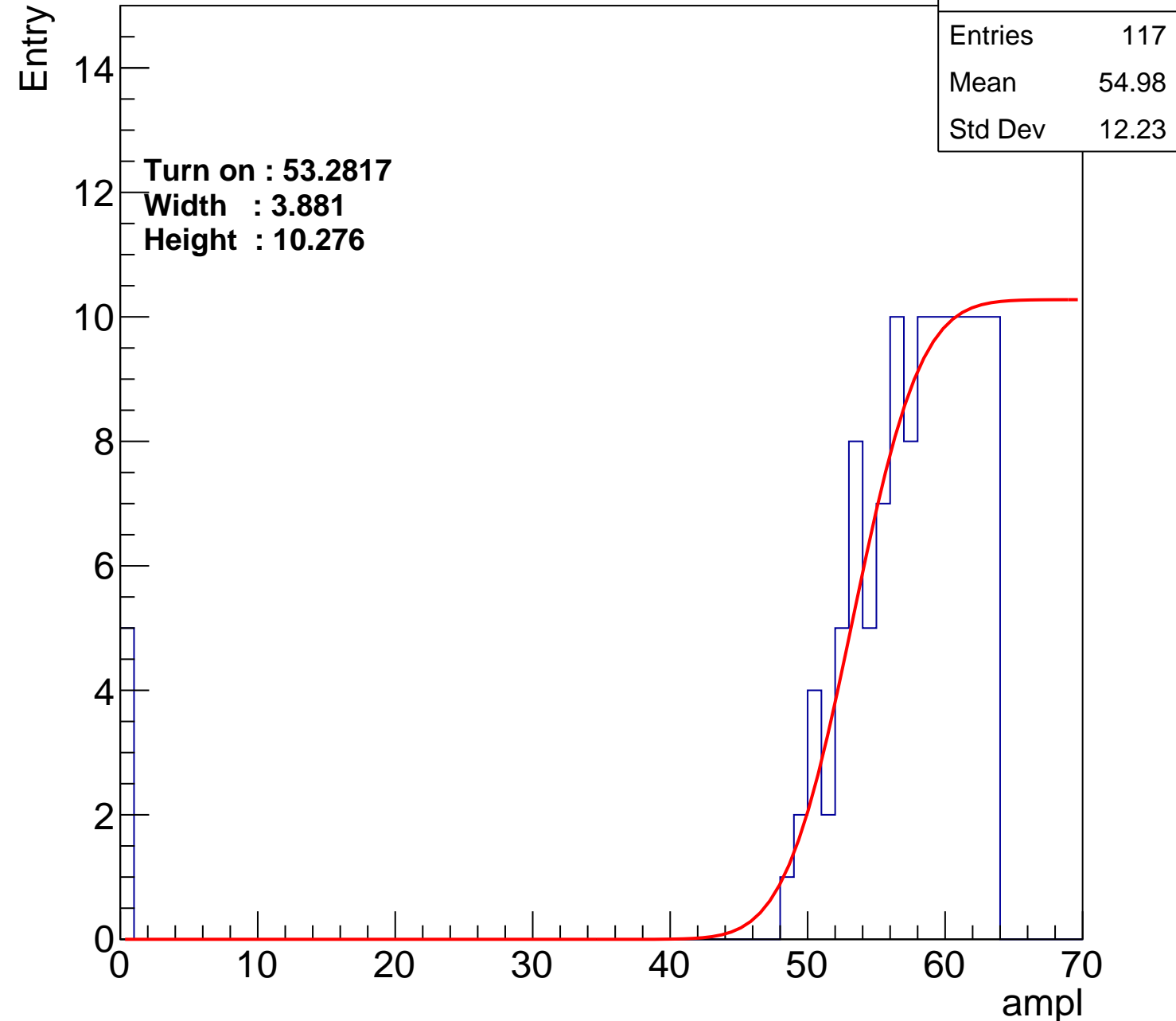
Width : 3.881

Height : 10.276

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch73

calib_packv5_040323_1717.root, FC#2, port C3

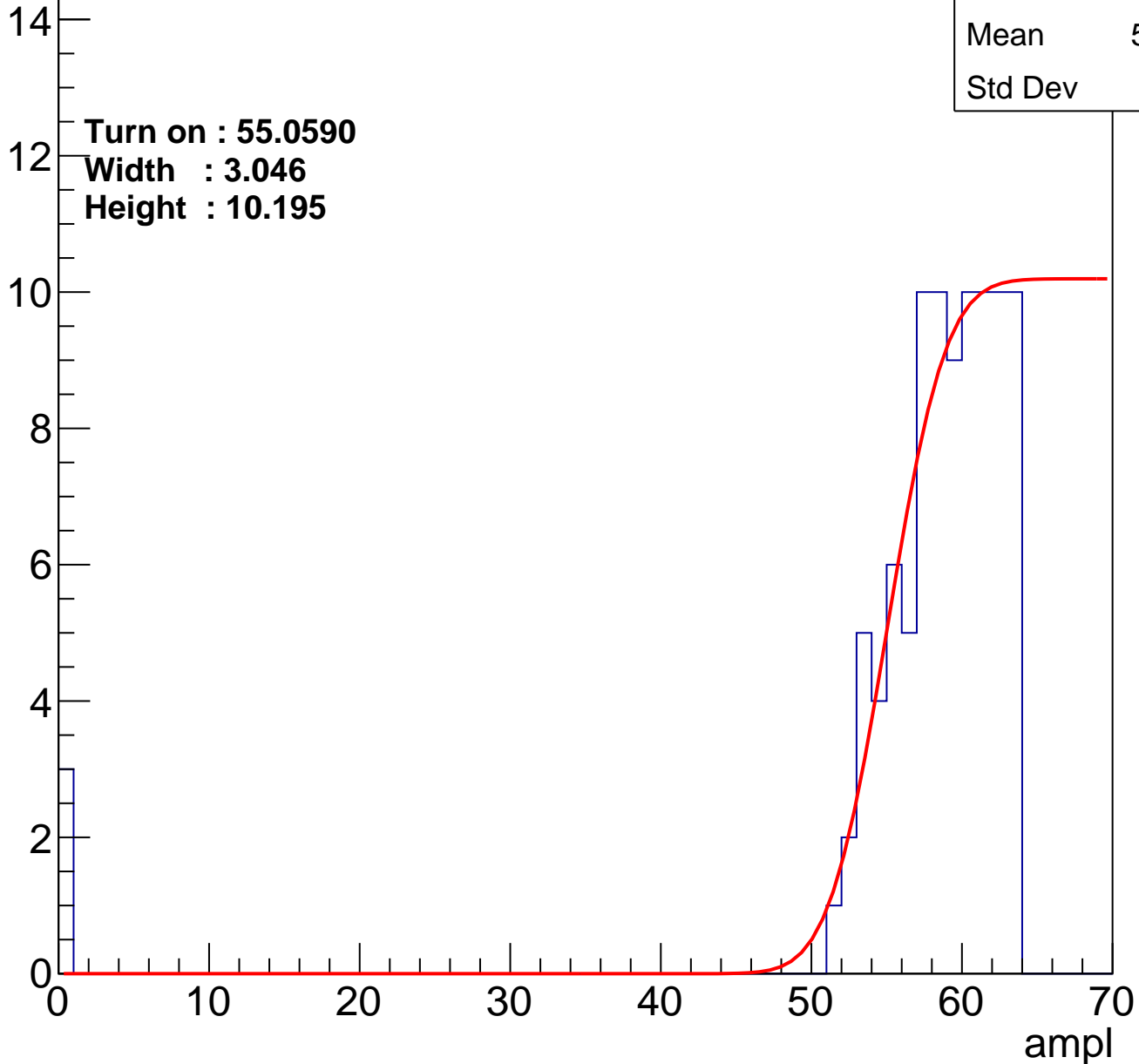
Entries	95
Mean	56.71
Std Dev	10.7

Turn on : 55.0590

Width : 3.046

Height : 10.195

Entry



B0L103S, U12-ch74

calib_packv5_040323_1717.root, FC#2, port C3

Entries	124
Mean	54.93
Std Dev	11.86

Turn on : 52.2058

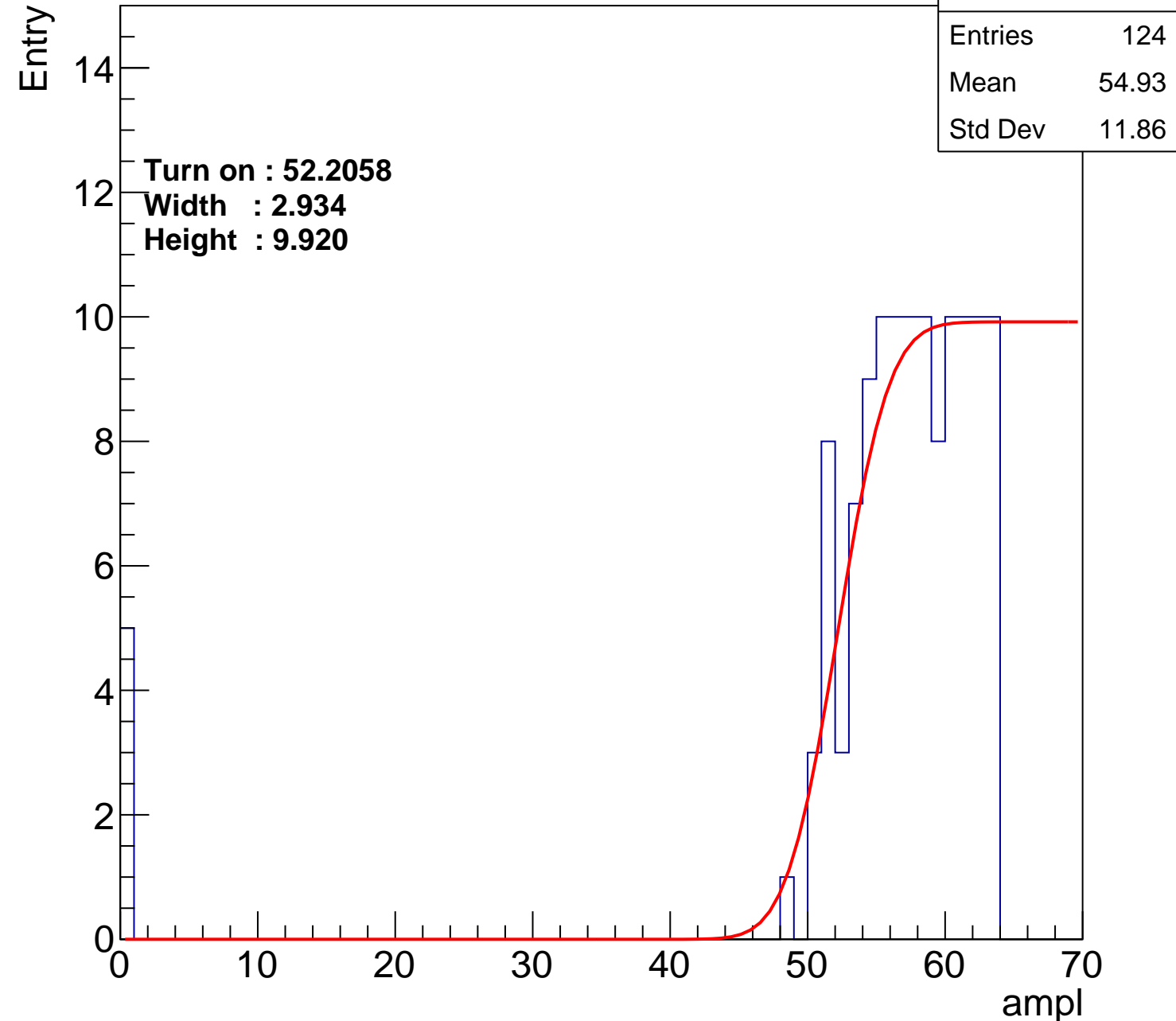
Width : 2.934

Height : 9.920

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch75

calib_packv5_040323_1717.root, FC#2, port C3

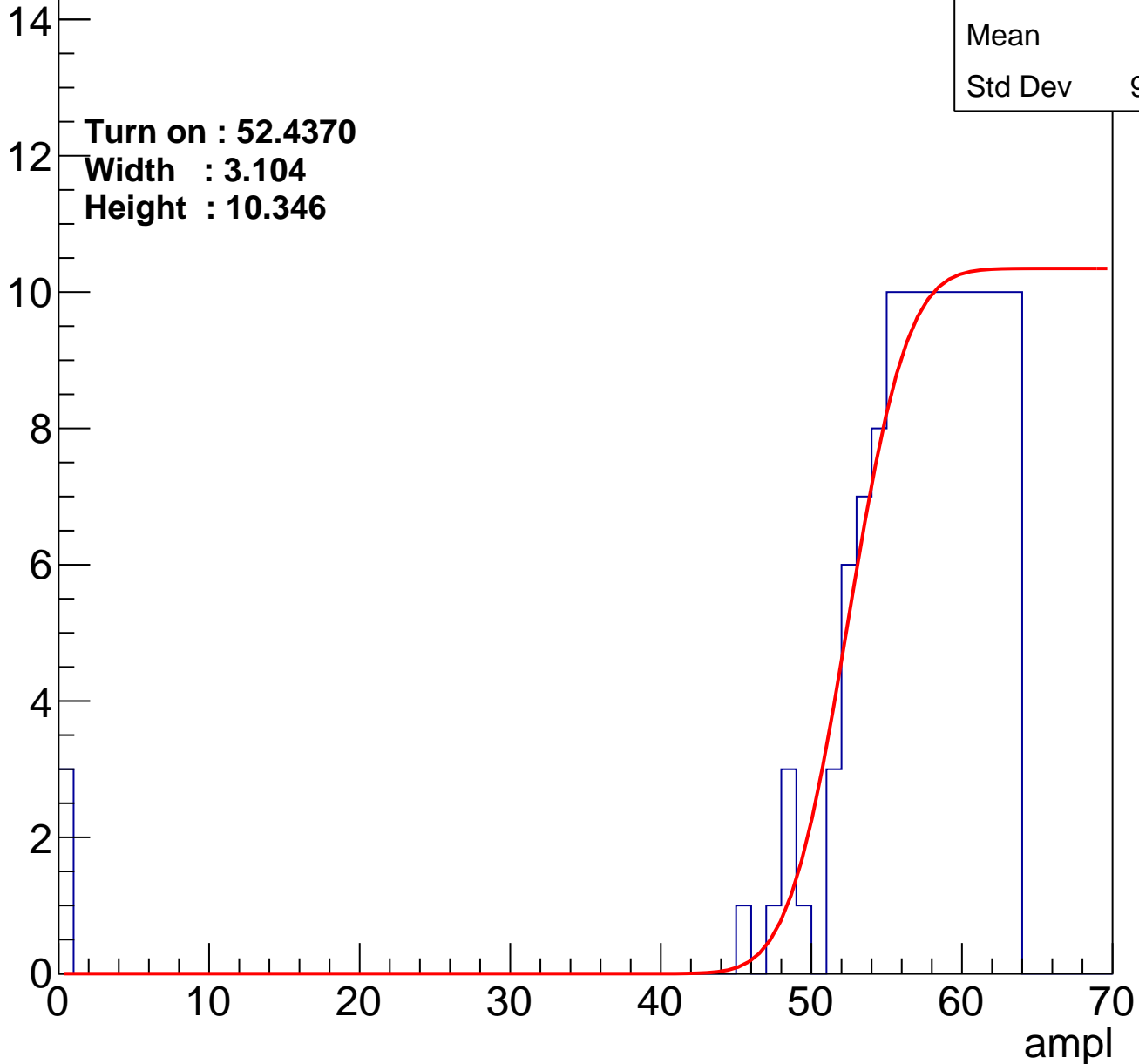
Entries	123
Mean	55.8
Std Dev	9.679

Turn on : 52.4370

Width : 3.104

Height : 10.346

Entry



B0L103S, U12-ch76

calib_packv5_040323_1717.root, FC#2, port C3

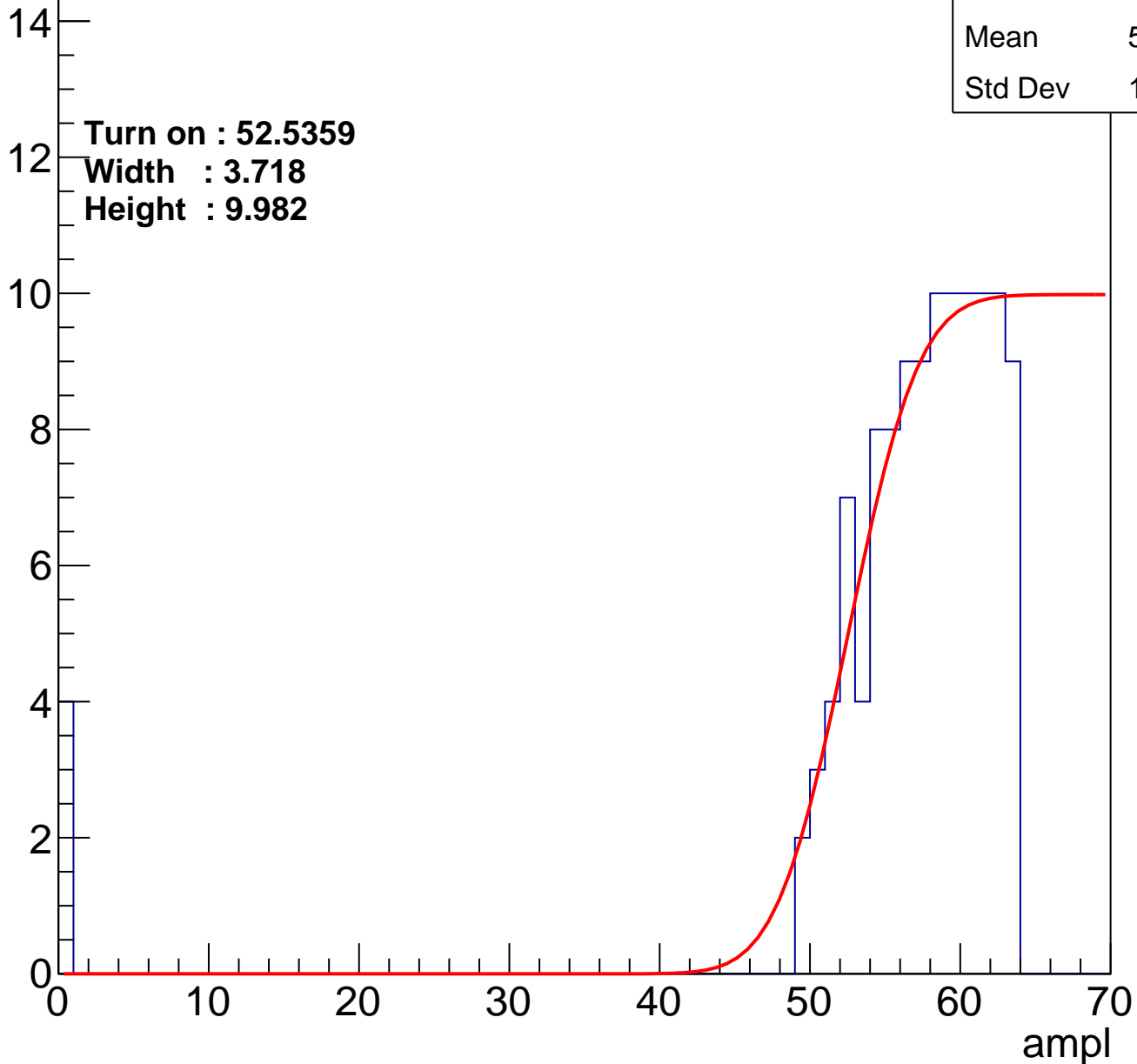
Entries	117
Mean	55.42
Std Dev	11.07

Turn on : 52.5359

Width : 3.718

Height : 9.982

Entry



B0L103S, U12-ch77

calib_packv5_040323_1717.root, FC#2, port C3

Entries	108
Mean	54.89
Std Dev	13.7

Turn on : 53.9613

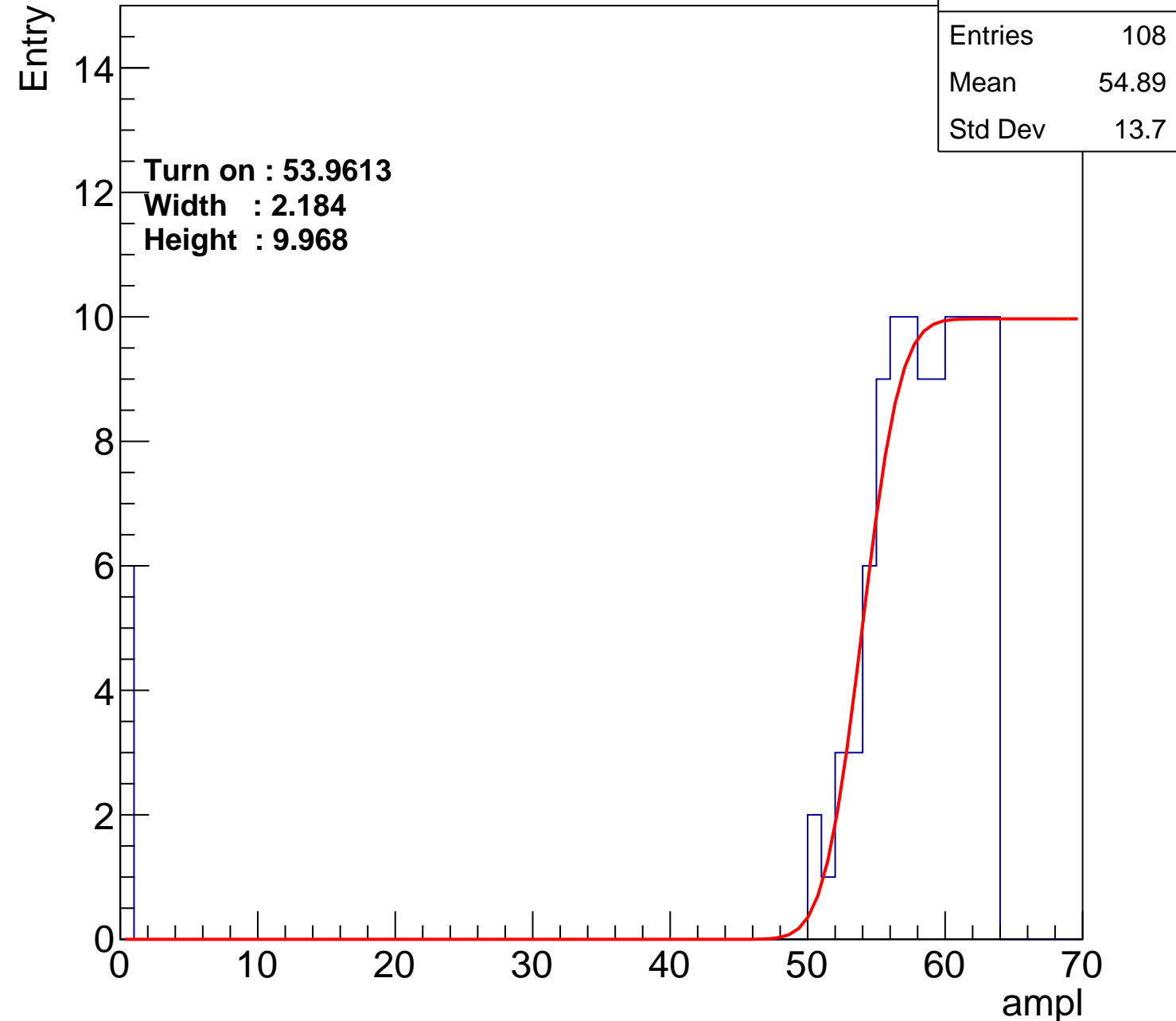
Width : 2.184

Height : 9.968

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch78

calib_packv5_040323_1717.root, FC#2, port C3

Entries	125
Mean	54.39
Std Dev	12.83

Turn on : 51.9492

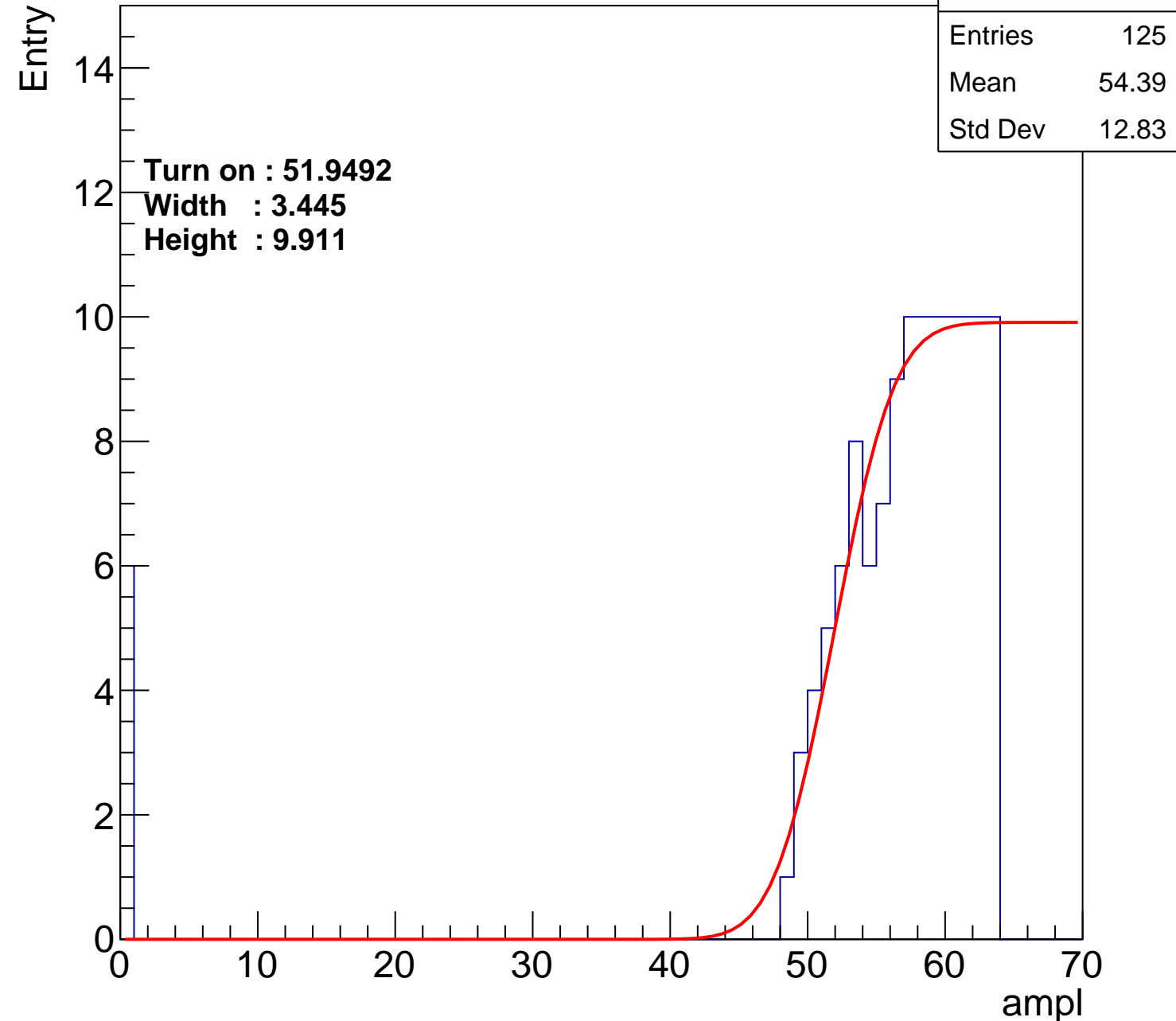
Width : 3.445

Height : 9.911

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch79

calib_packv5_040323_1717.root, FC#2, port C3

Entries	106
Mean	56.4
Std Dev	10.23

Turn on : 54.5712

Width : 3.306

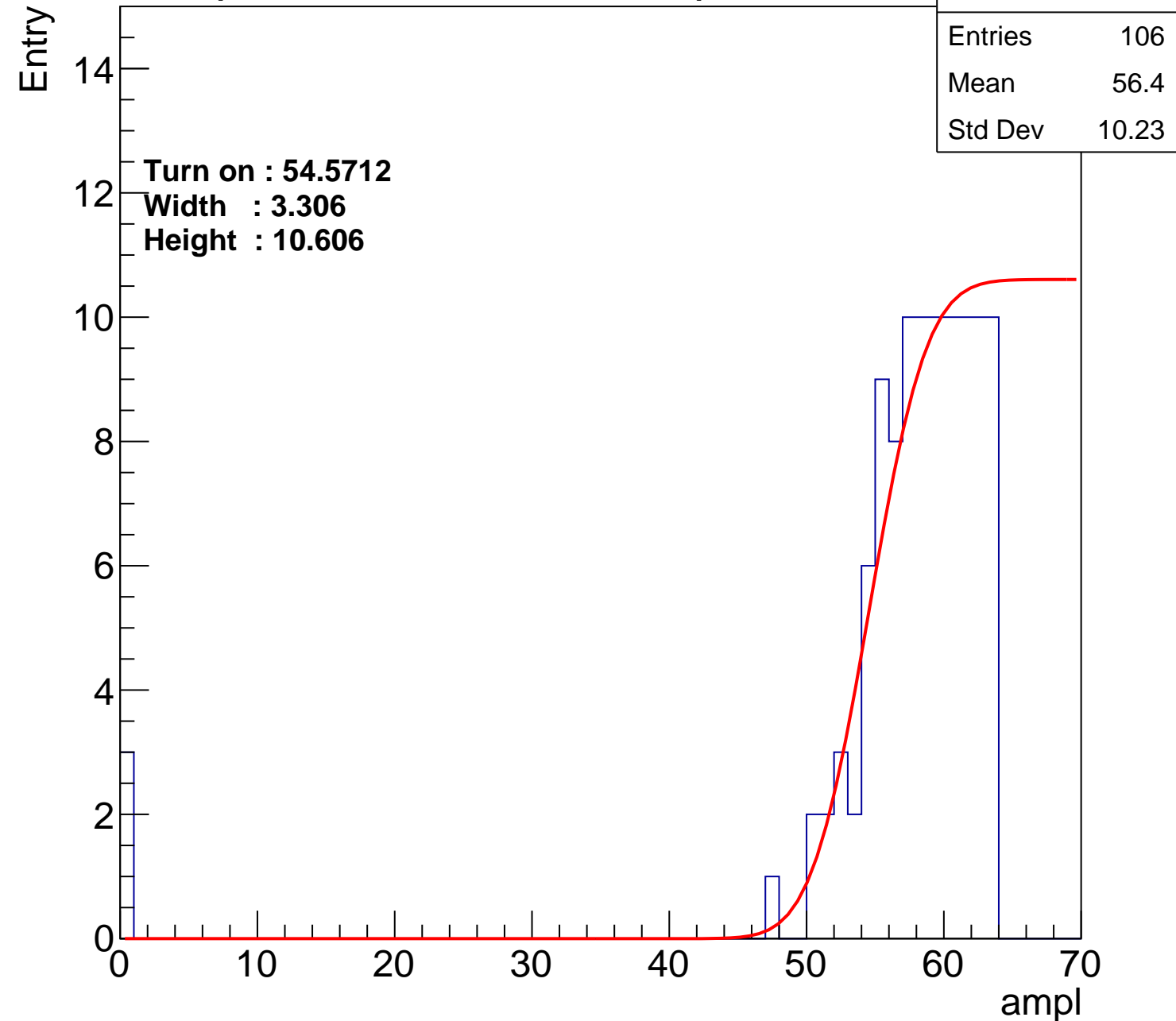
Height : 10.606

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B0L103S, U12-ch80

calib_packv5_040323_1717.root, FC#2, port C3

Entries	102
Mean	55.96
Std Dev	11.8

Turn on : 54.6140

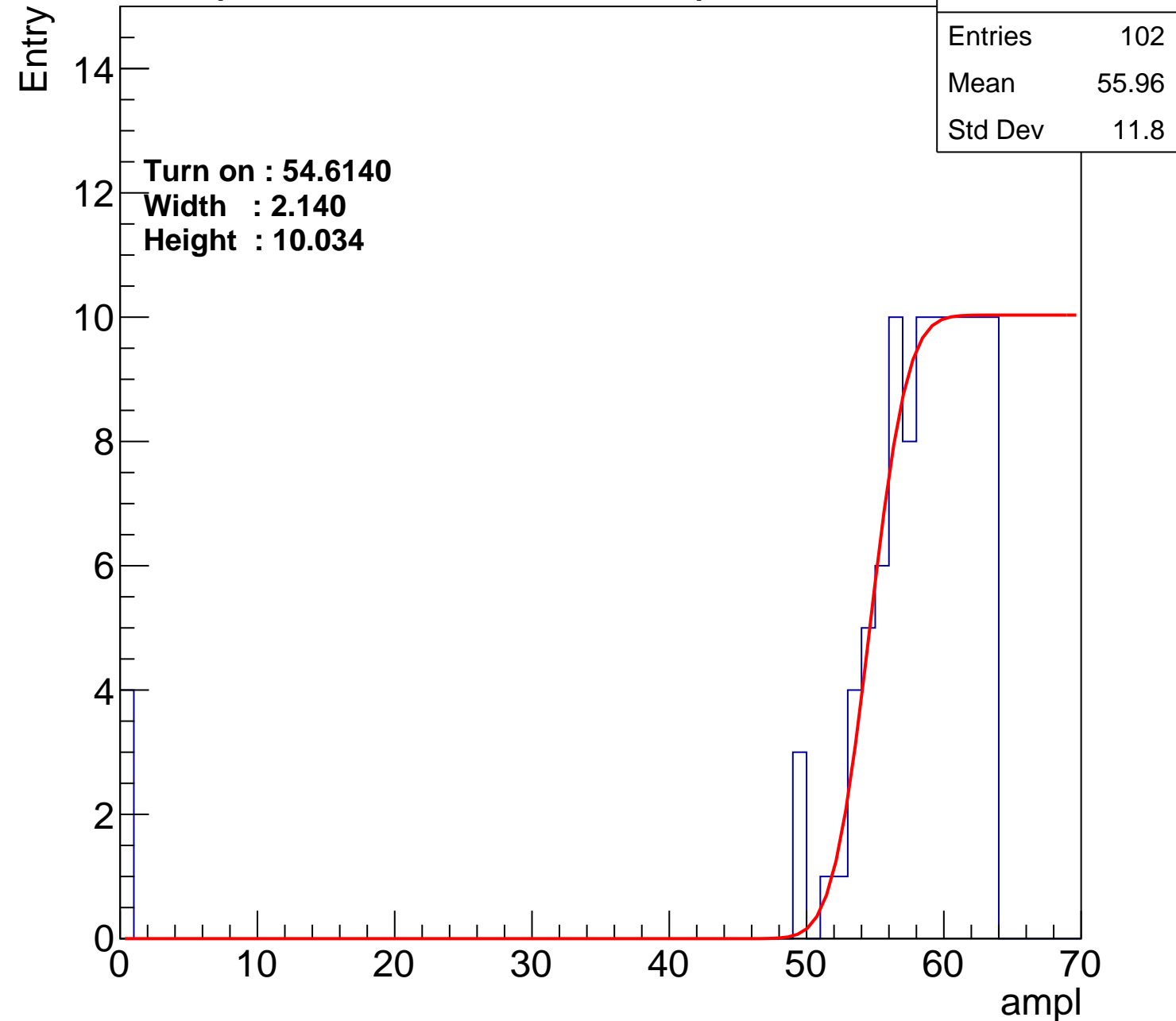
Width : 2.140

Height : 10.034

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch81

calib_packv5_040323_1717.root, FC#2, port C3

Entries	105
Mean	57.39
Std Dev	6.602

Turn on : 53.3818

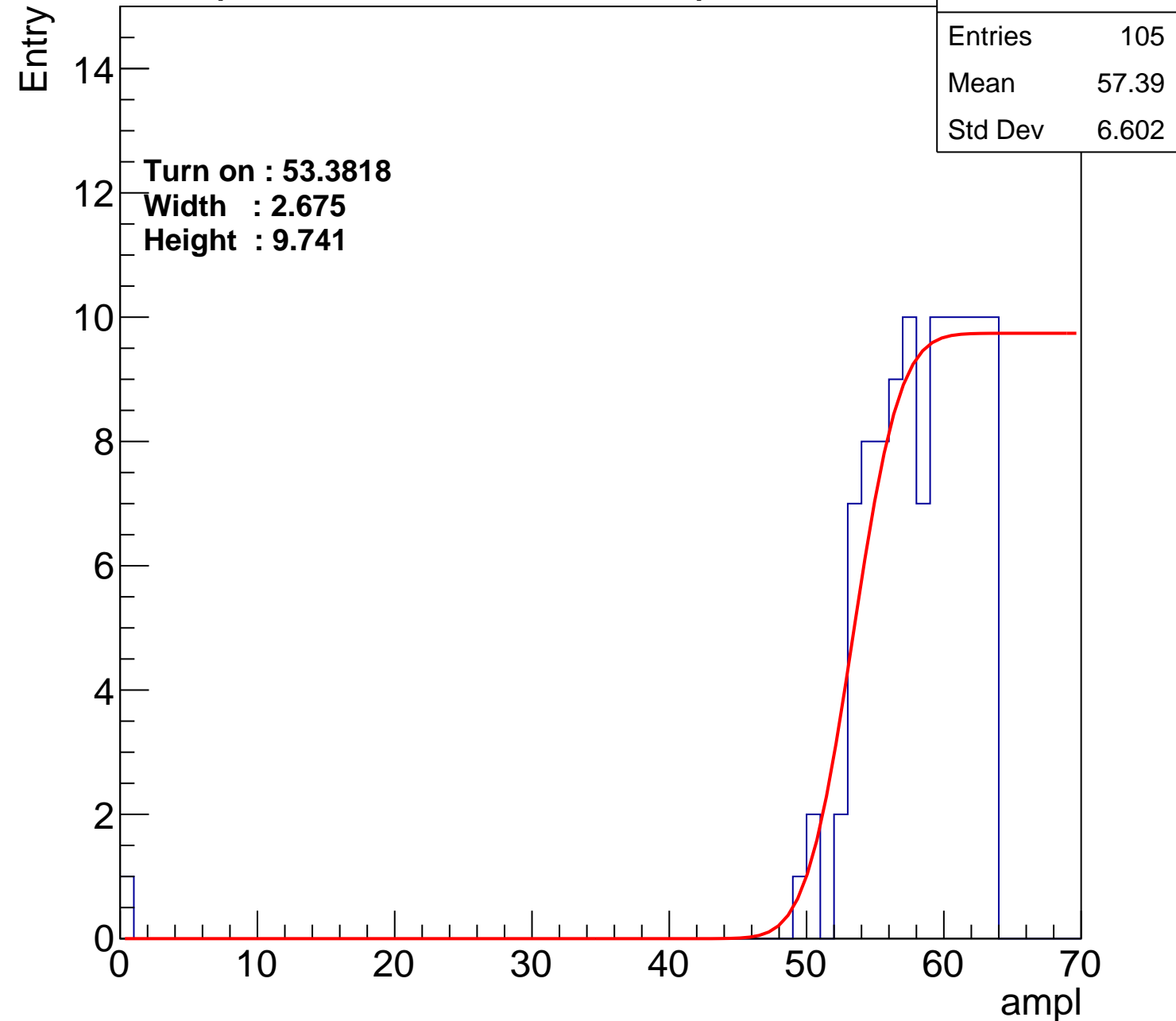
Width : 2.675

Height : 9.741

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch82

calib_packv5_040323_1717.root, FC#2, port C3

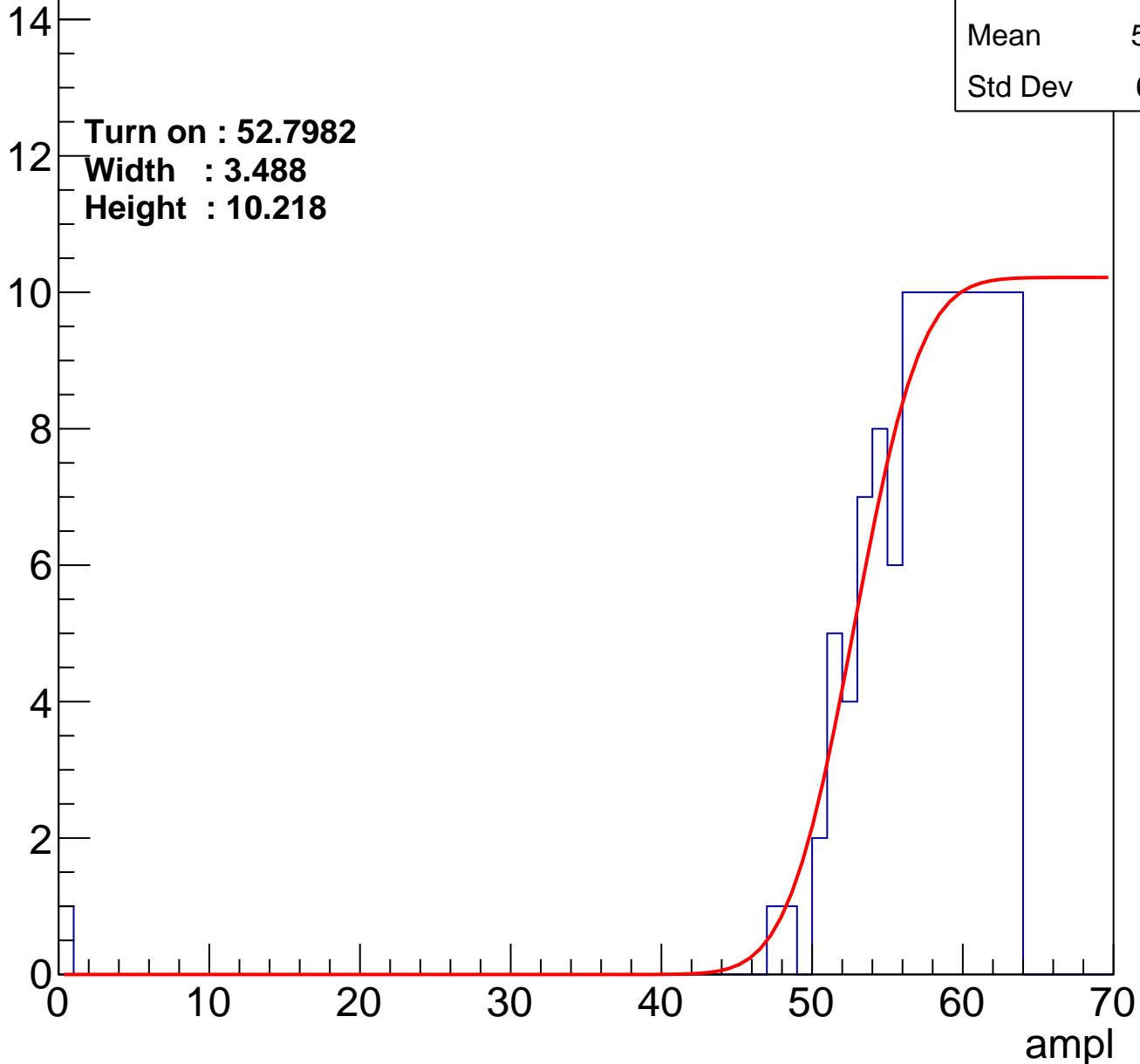
Entries	115
Mean	56.97
Std Dev	6.551

Turn on : 52.7982

Width : 3.488

Height : 10.218

Entry



B0L103S, U12-ch83

calib_packv5_040323_1717.root, FC#2, port C3

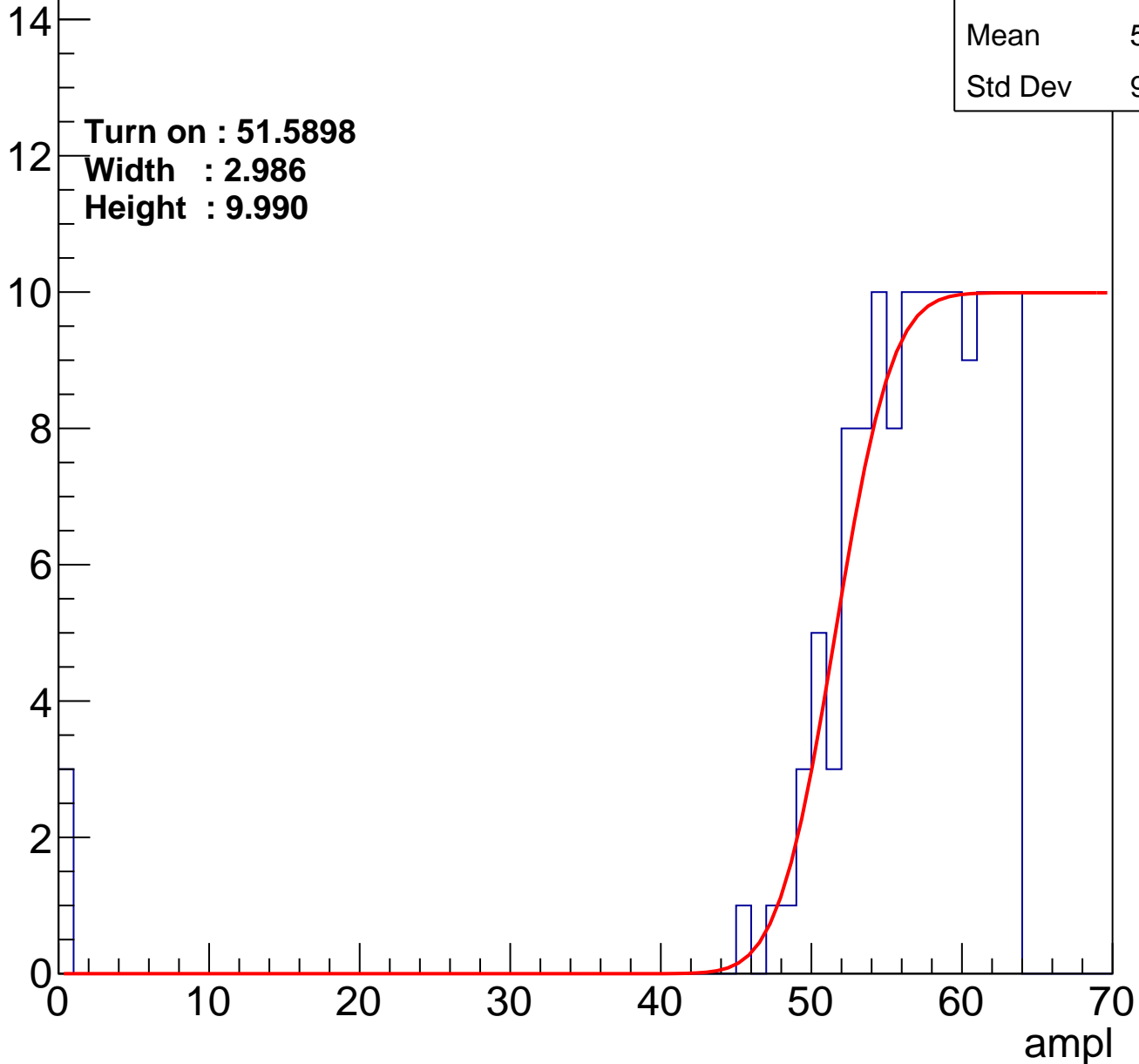
Entries	130
Mean	55.46
Std Dev	9.475

Turn on : 51.5898

Width : 2.986

Height : 9.990

Entry



B0L103S, U12-ch84

calib_packv5_040323_1717.root, FC#2, port C3

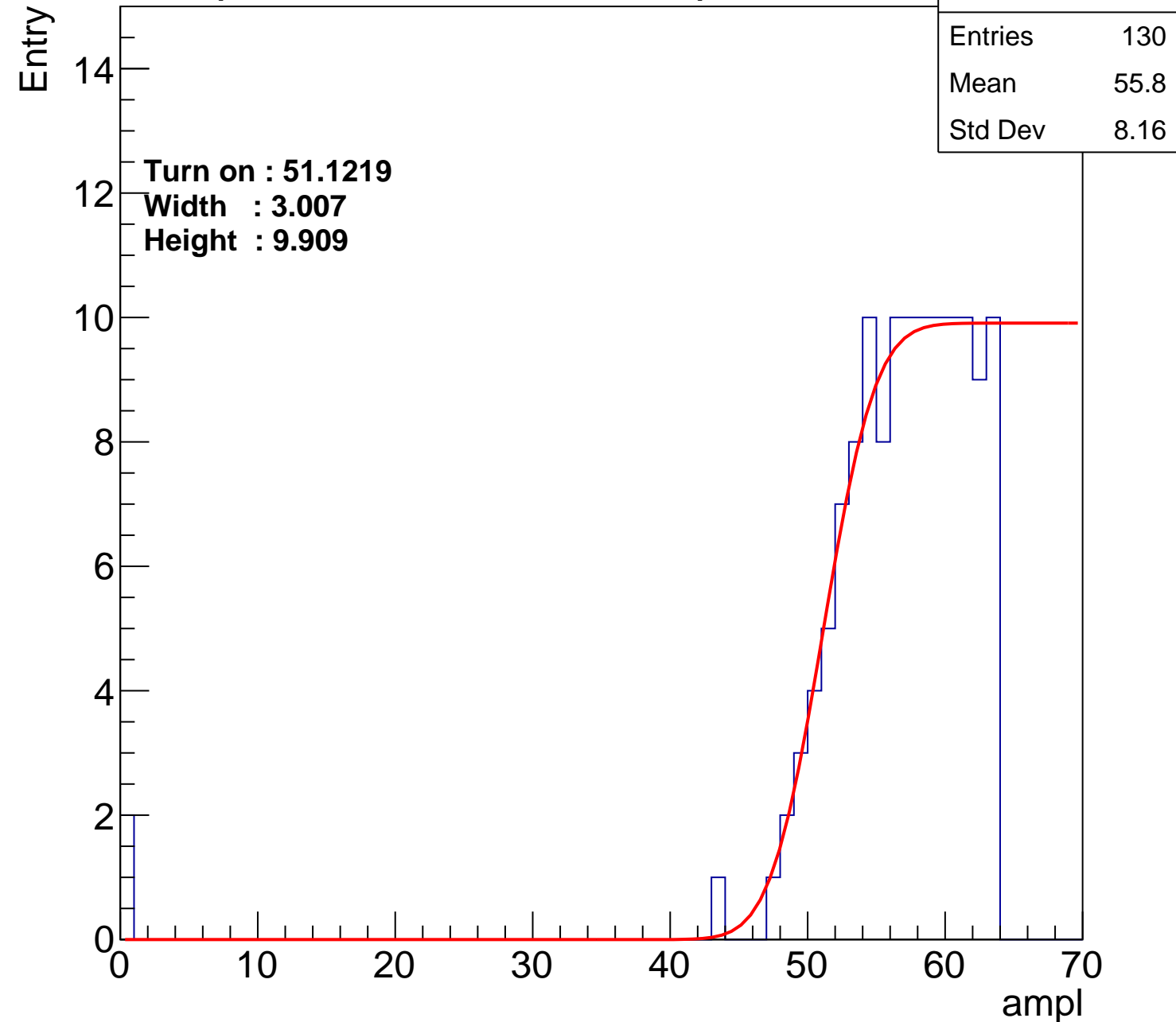
Entry

14
12
10
8
6
4
2
0

Turn on : 51.1219
Width : 3.007
Height : 9.909

Entries	130
Mean	55.8
Std Dev	8.16

ampl



B0L103S, U12-ch85

calib_packv5_040323_1717.root, FC#2, port C3

Entries	122
Mean	55.12
Std Dev	10.89

Turn on : 51.8538

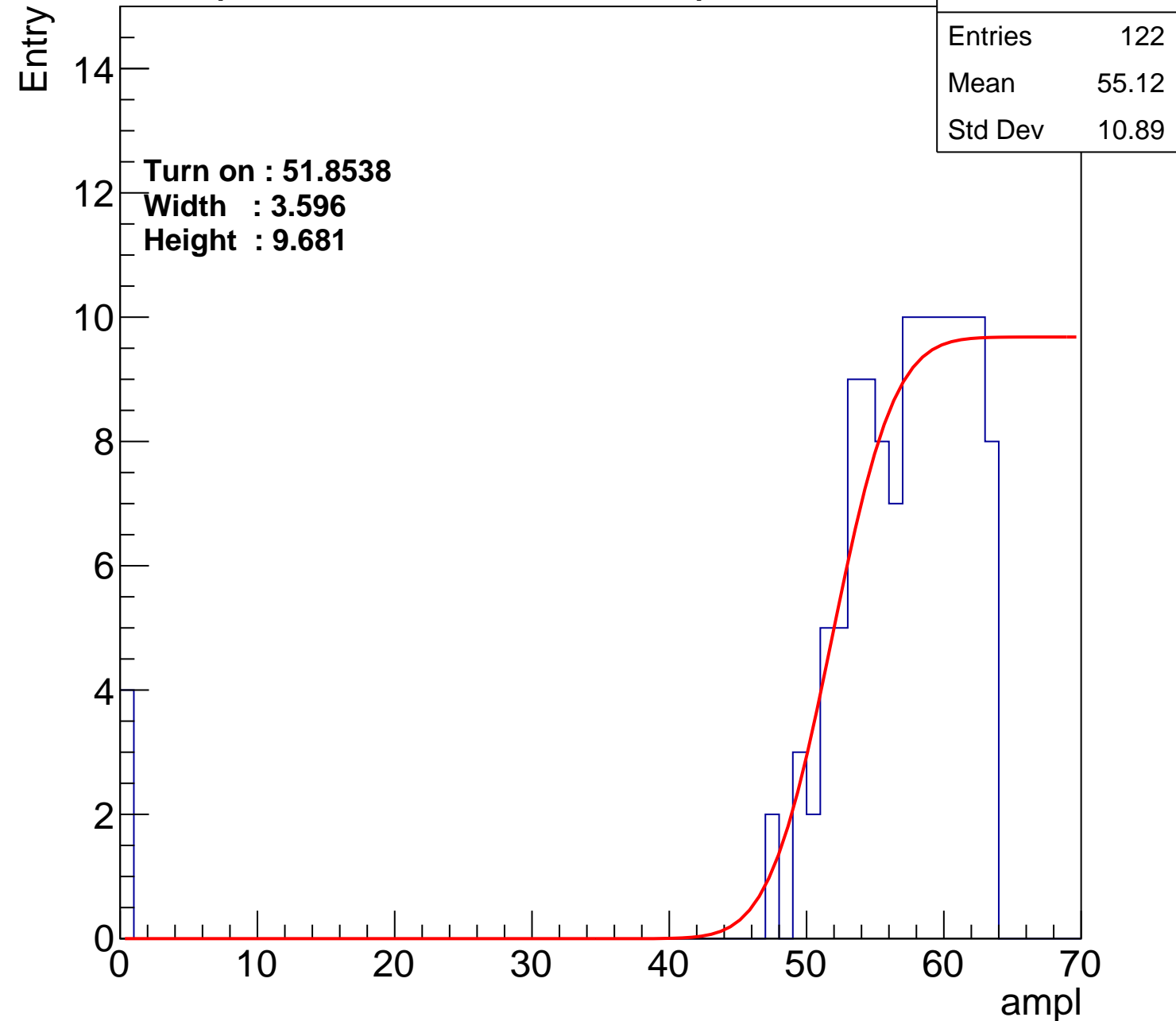
Width : 3.596

Height : 9.681

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch86

calib_packv5_040323_1717.root, FC#2, port C3

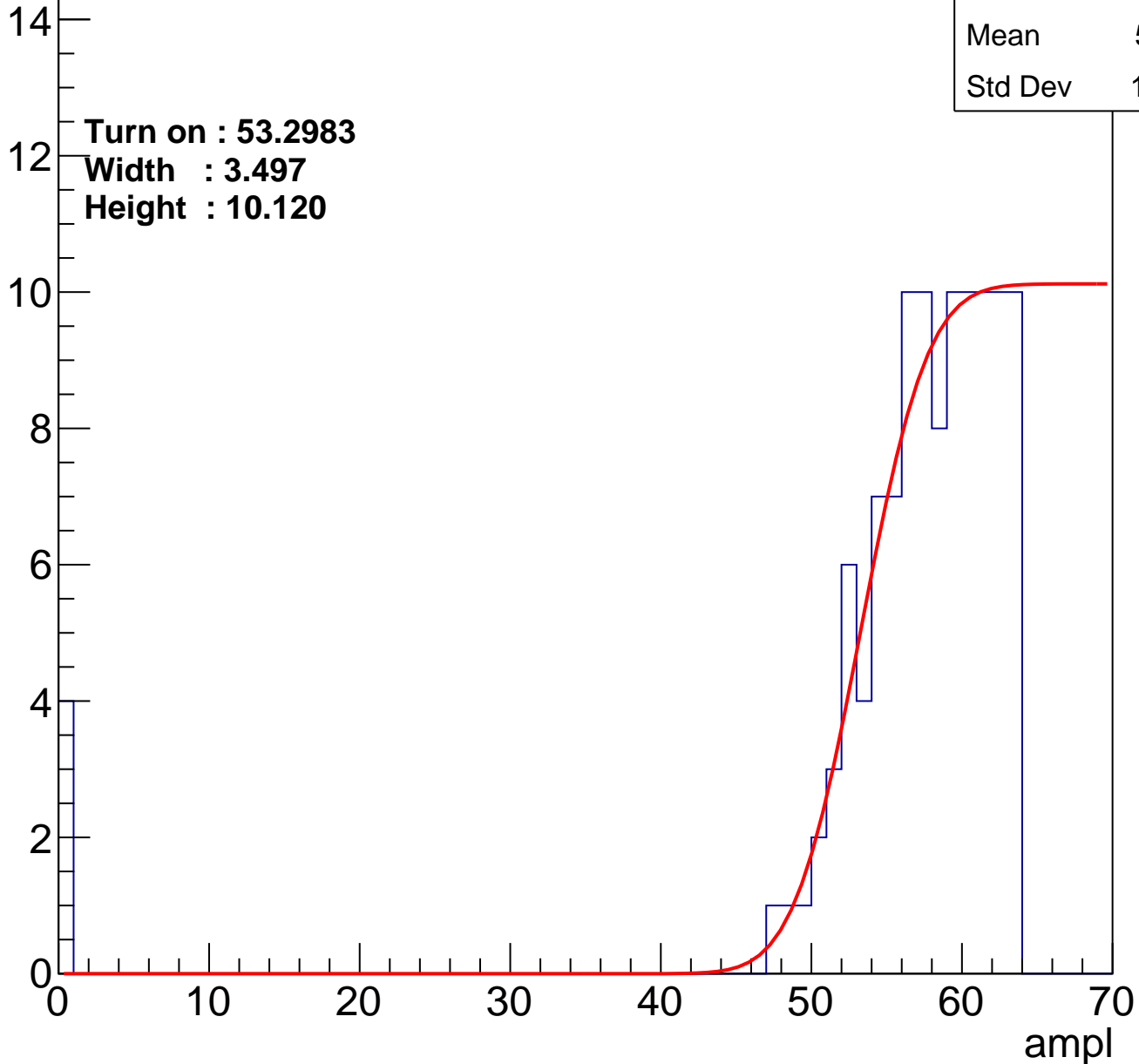
Entries	114
Mean	55.51
Std Dev	11.25

Turn on : 53.2983

Width : 3.497

Height : 10.120

Entry



B0L103S, U12-ch87

calib_packv5_040323_1717.root, FC#2, port C3

Entries	123
Mean	55.77
Std Dev	9.661

Turn on : 52.0800

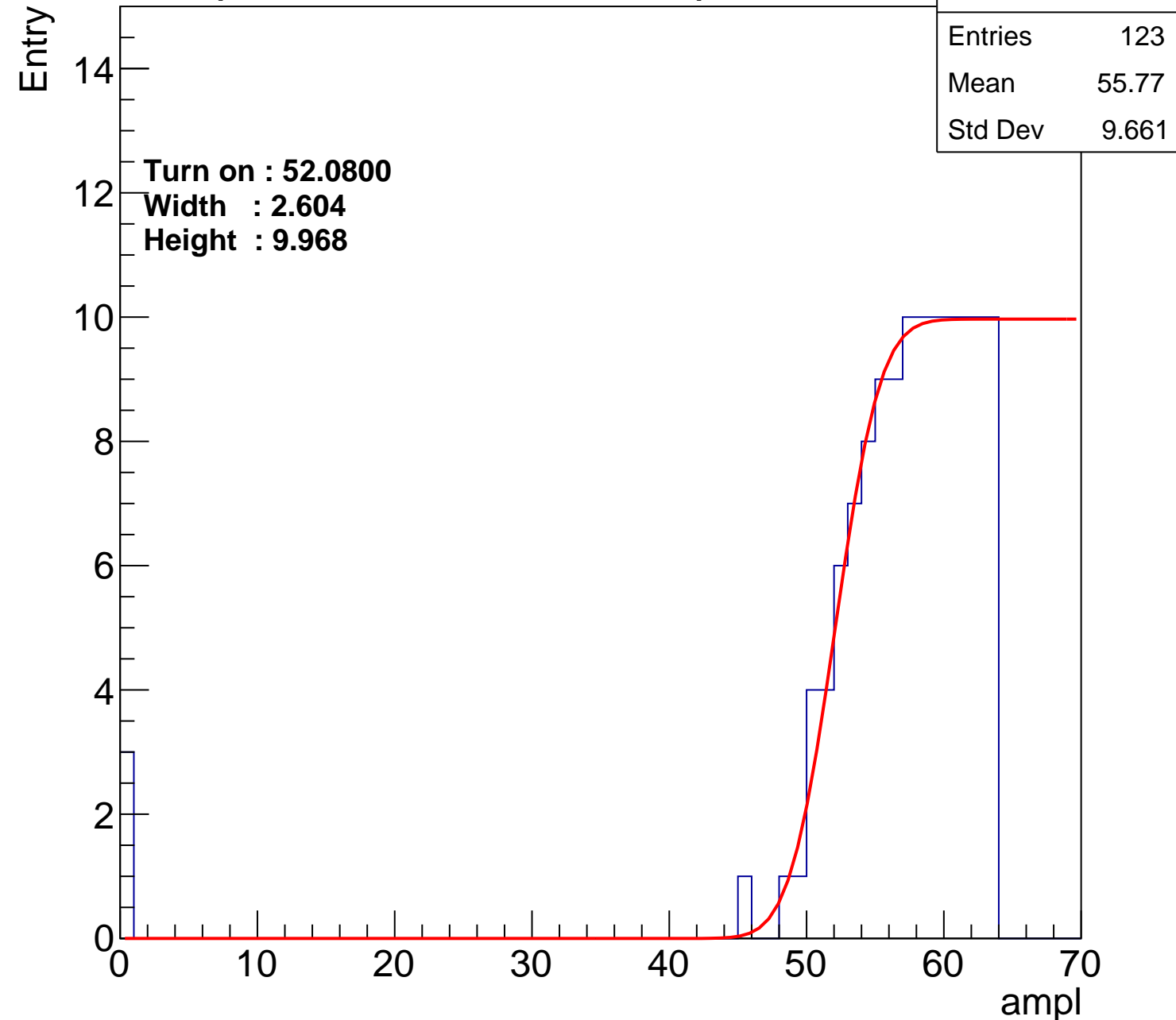
Width : 2.604

Height : 9.968

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch88

calib_packv5_040323_1717.root, FC#2, port C3

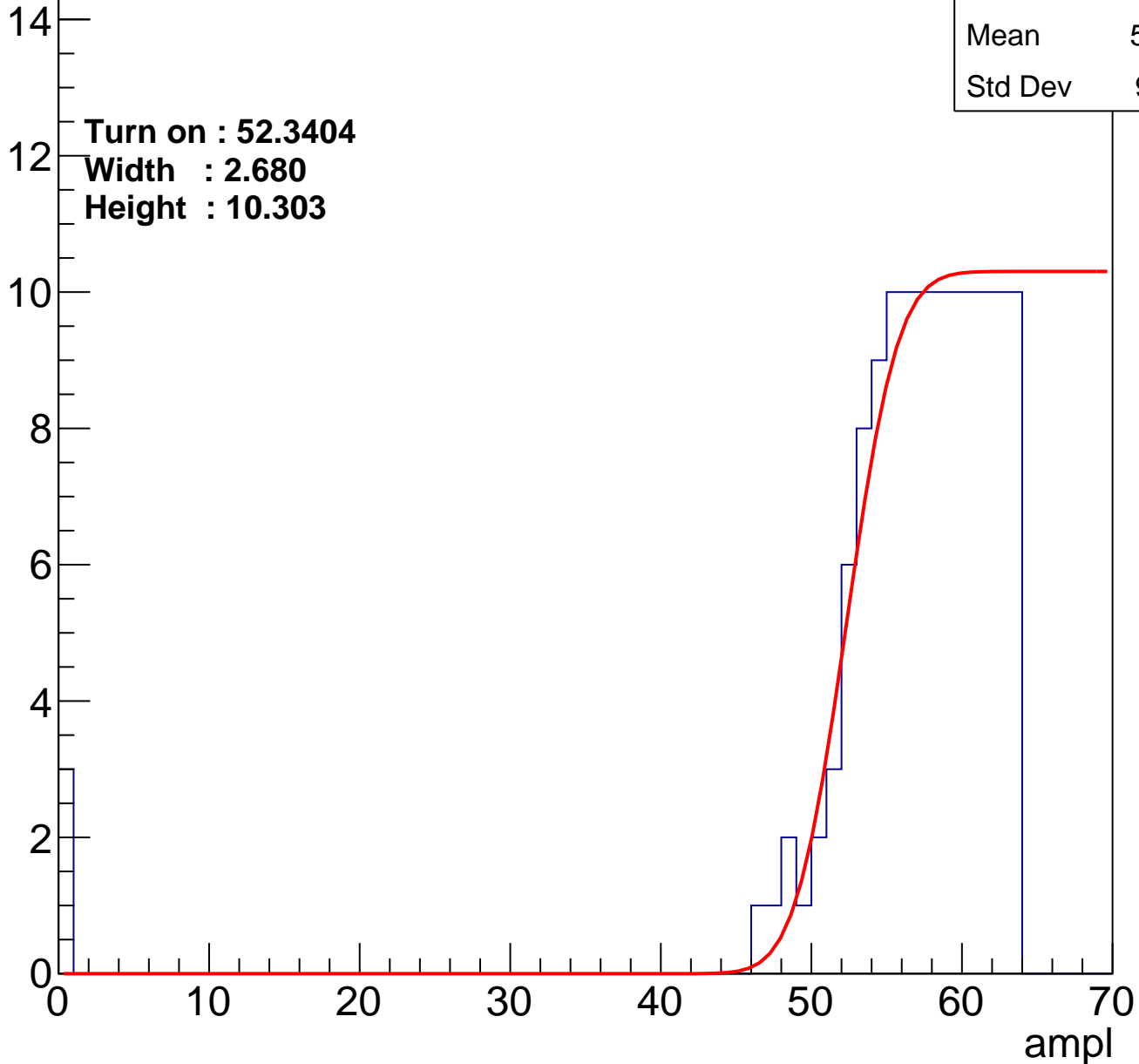
Entries	126
Mean	55.74
Std Dev	9.561

Turn on : 52.3404

Width : 2.680

Height : 10.303

Entry



B0L103S, U12-ch89

calib_packv5_040323_1717.root, FC#2, port C3

Entries	122
Mean	55
Std Dev	11.97

Turn on : 52.6310

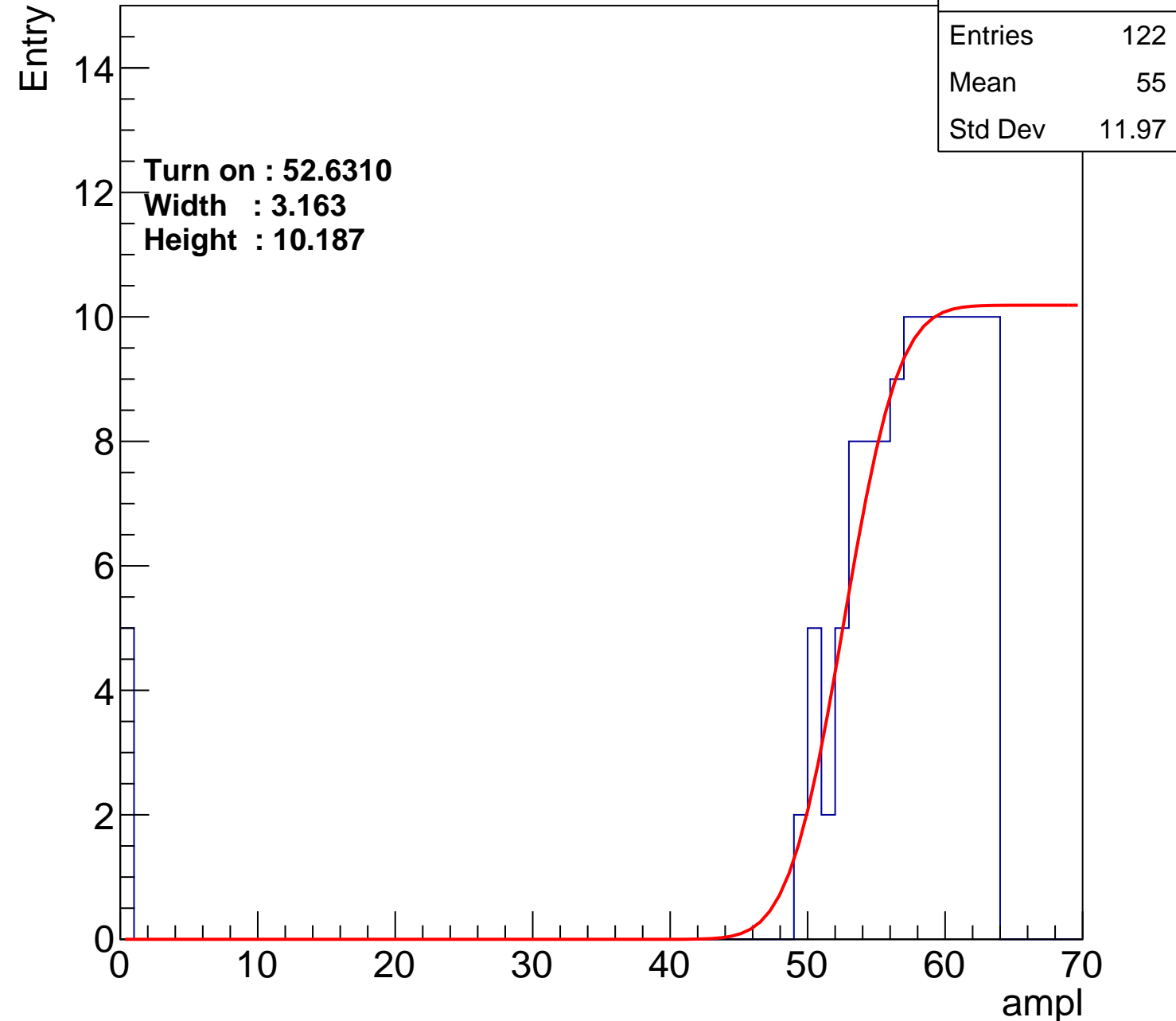
Width : 3.163

Height : 10.187

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch90

calib_packv5_040323_1717.root, FC#2, port C3

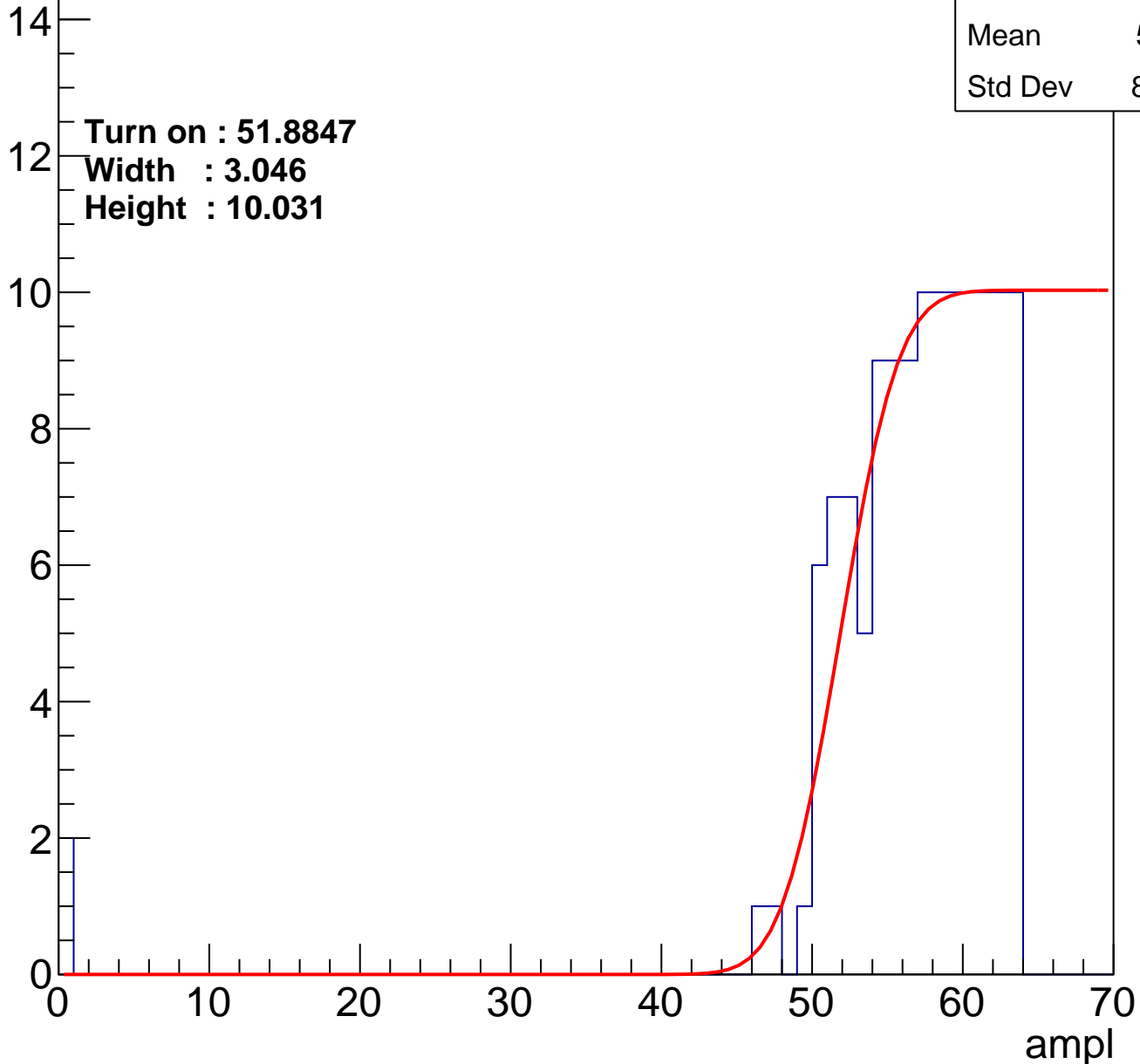
Entries	127
Mean	56.01
Std Dev	8.179

Turn on : 51.8847

Width : 3.046

Height : 10.031

Entry



B0L103S, U12-ch91

calib_packv5_040323_1717.root, FC#2, port C3

Entries	113
Mean	55.73
Std Dev	11.21

Turn on : 52.7563

Width : 2.095

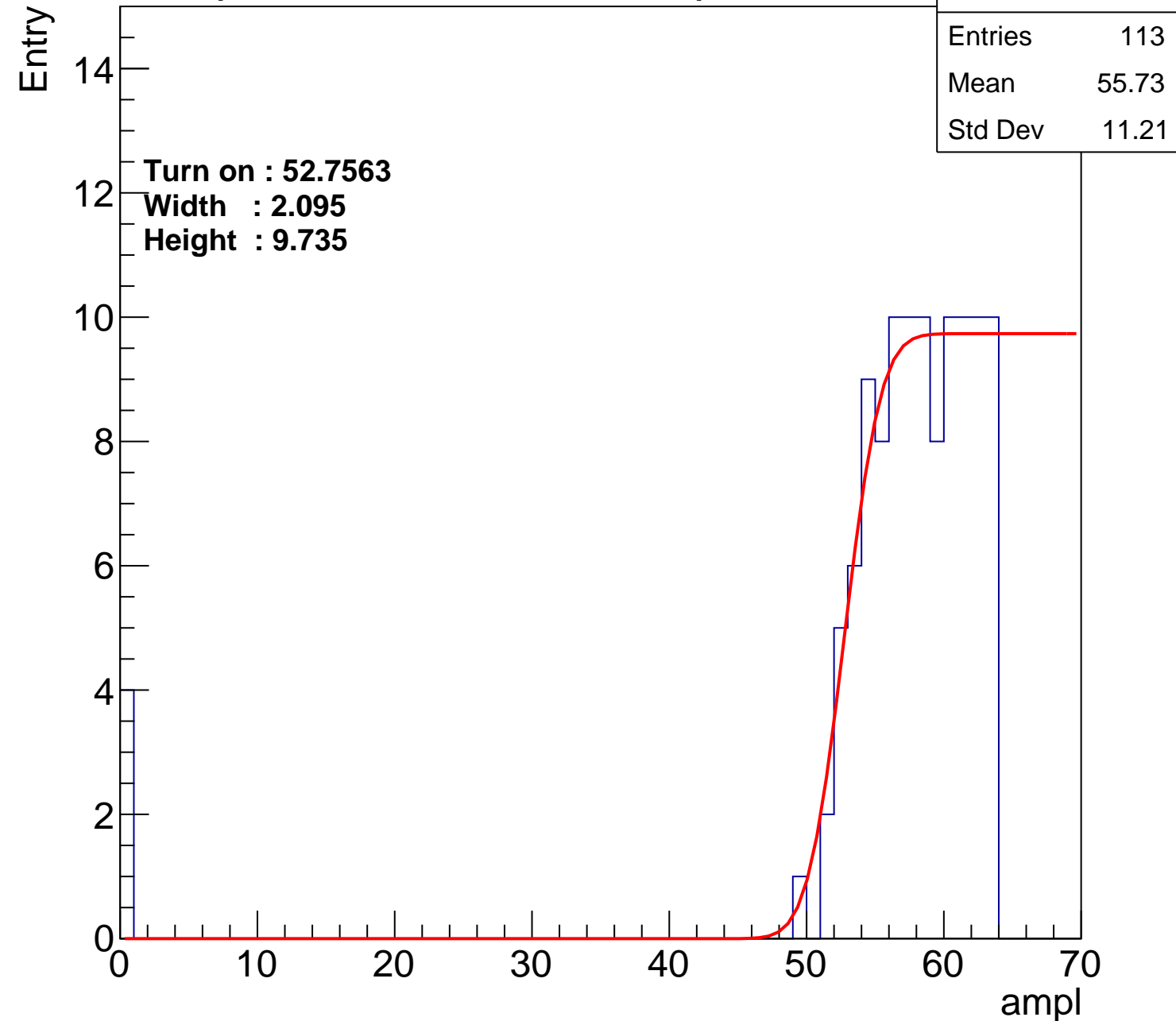
Height : 9.735

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B0L103S, U12-ch92

calib_packv5_040323_1717.root, FC#2, port C3

Entries	114
Mean	57.03
Std Dev	6.525

Turn on : 52.6797

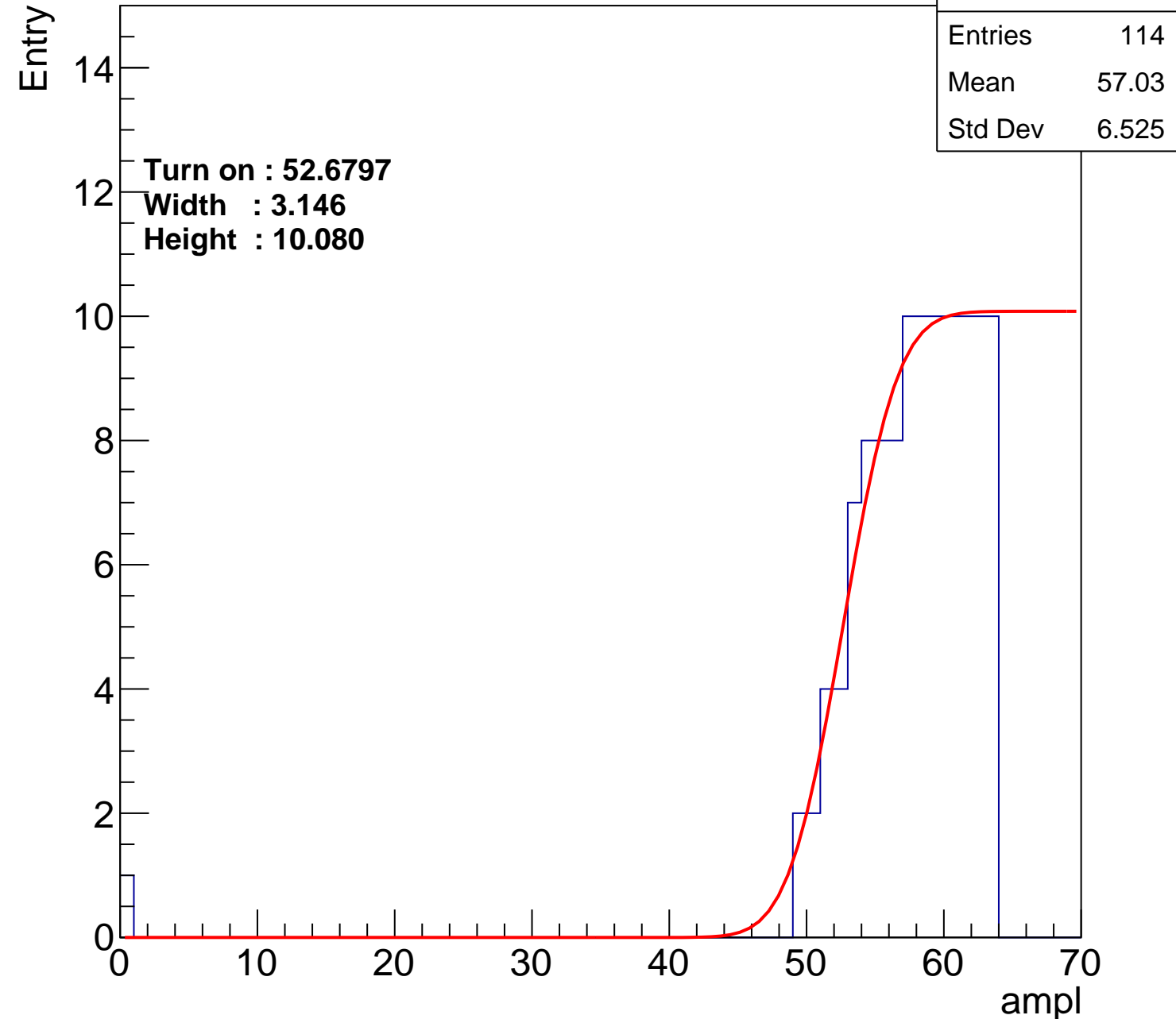
Width : 3.146

Height : 10.080

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch93

calib_packv5_040323_1717.root, FC#2, port C3

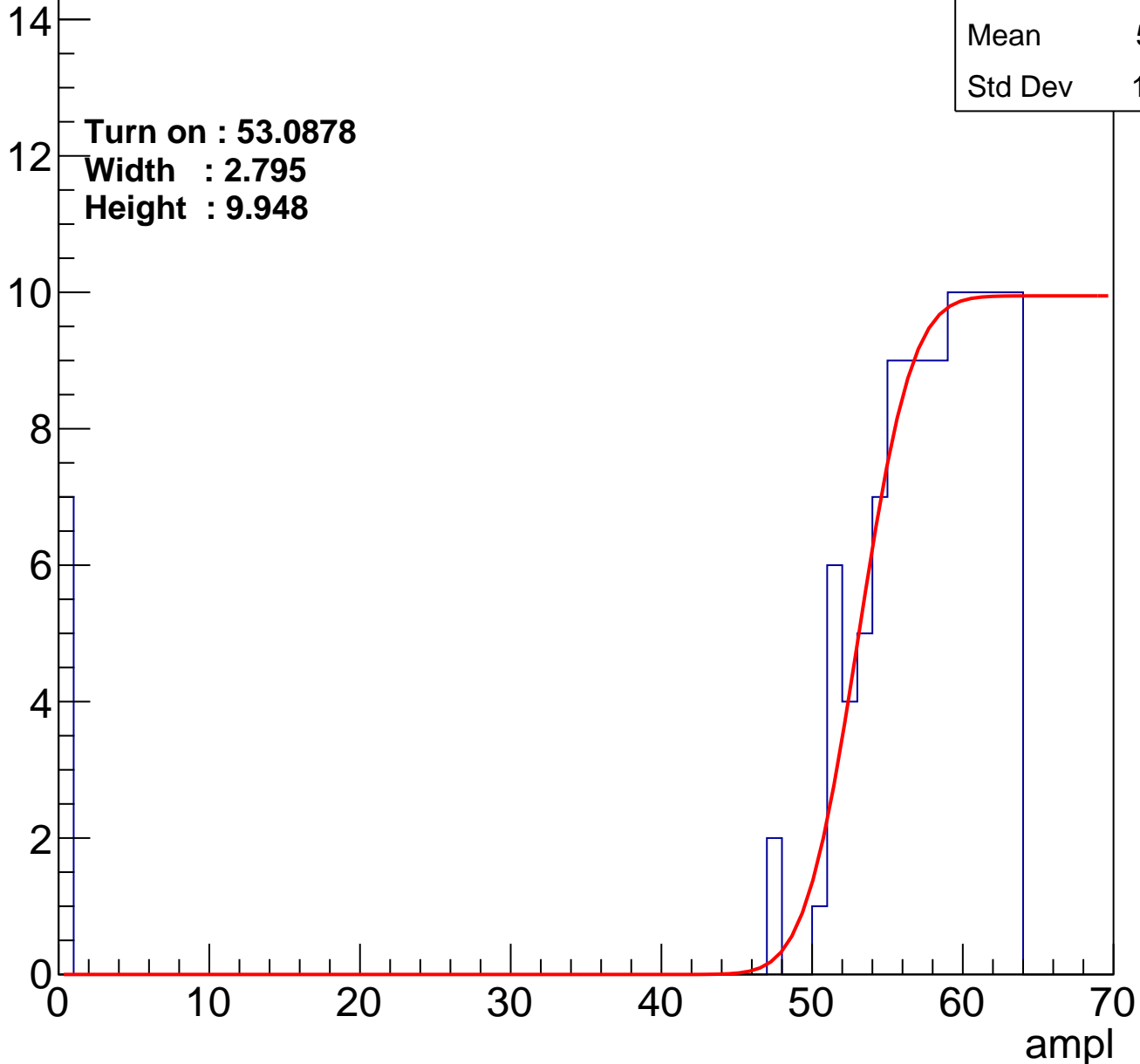
Entries	118
Mean	54.11
Std Dev	14.09

Turn on : 53.0878

Width : 2.795

Height : 9.948

Entry



B0L103S, U12-ch94

calib_packv5_040323_1717.root, FC#2, port C3

Entries	135
Mean	53.85
Std Dev	13.22

Turn on : 51.2084

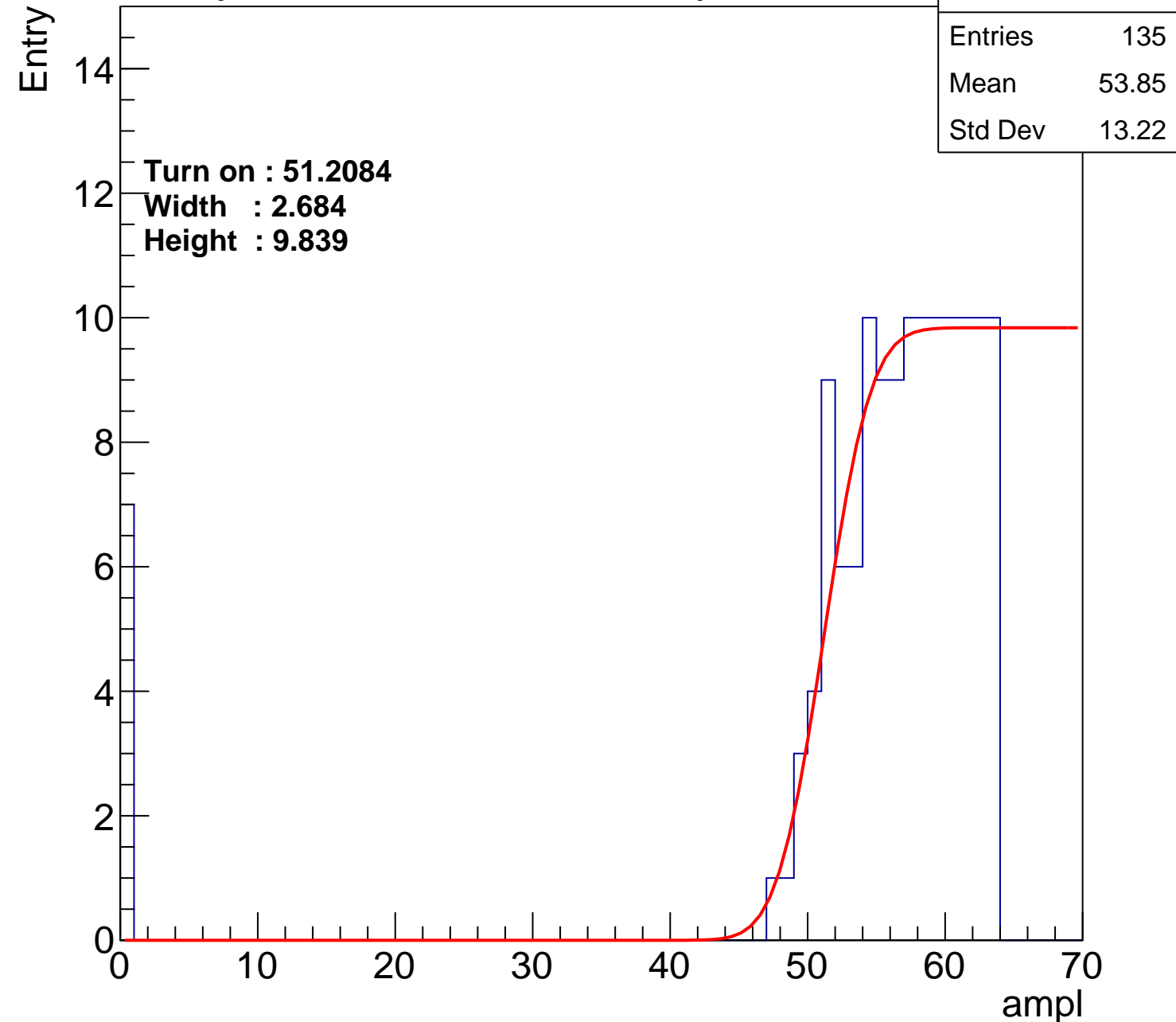
Width : 2.684

Height : 9.839

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch95

calib_packv5_040323_1717.root, FC#2, port C3

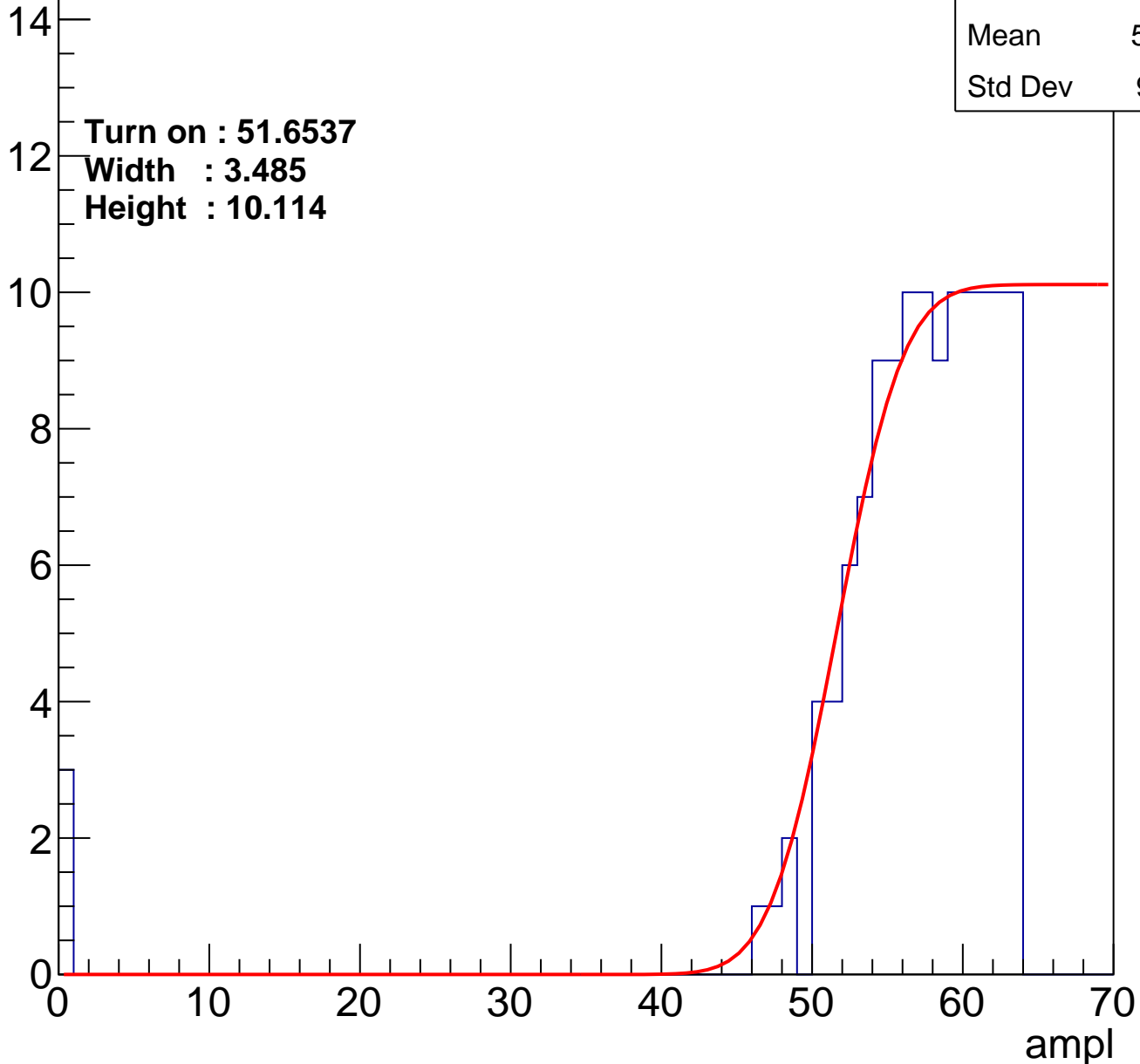
Entries	125
Mean	55.67
Std Dev	9.611

Turn on : 51.6537

Width : 3.485

Height : 10.114

Entry



B0L103S, U12-ch96

calib_packv5_040323_1717.root, FC#2, port C3

Entries	118
Mean	56.69
Std Dev	6.675

Turn on : 53.2734

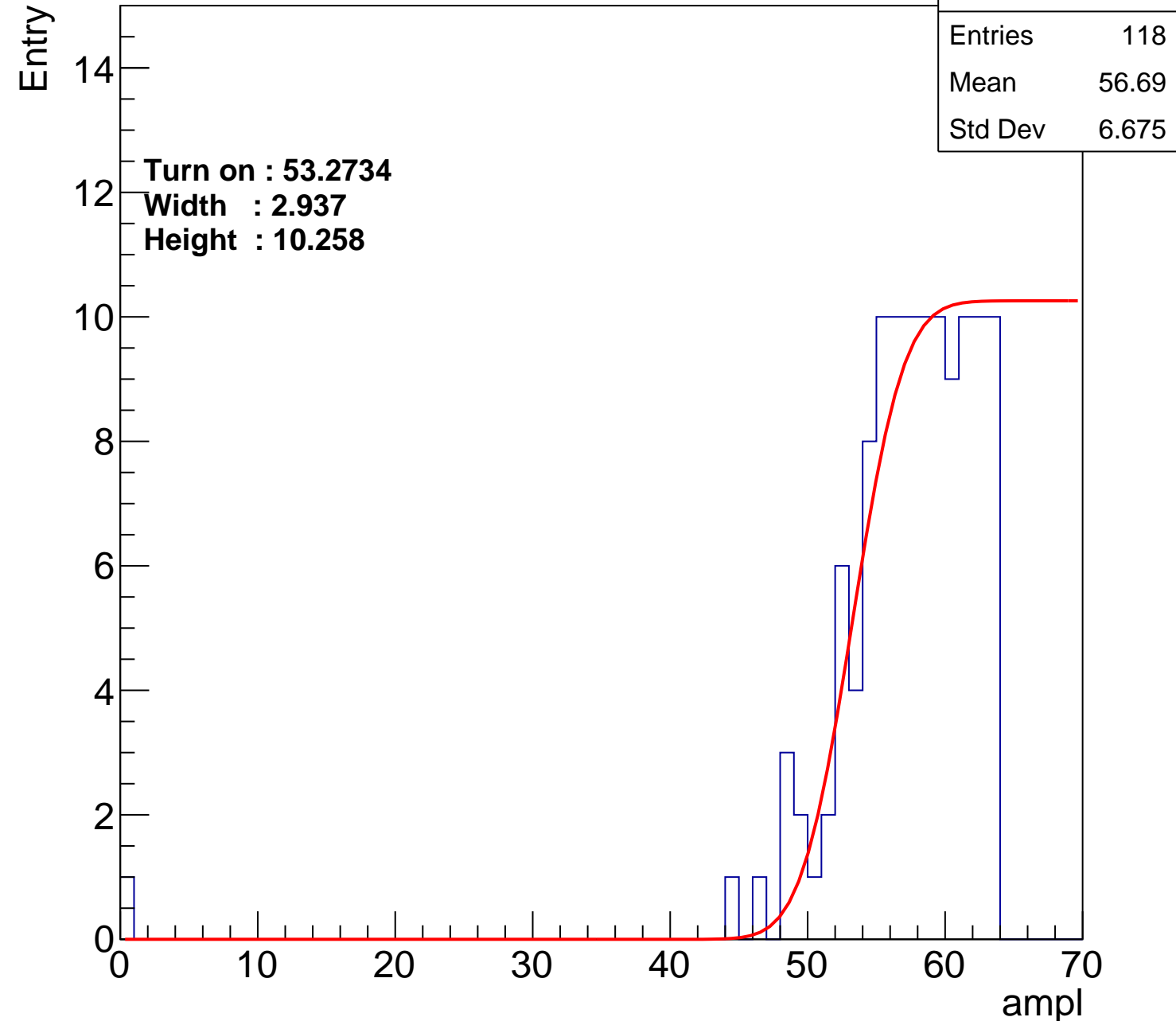
Width : 2.937

Height : 10.258

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch97

calib_packv5_040323_1717.root, FC#2, port C3

Entries	116
Mean	55.28
Std Dev	11.18

Turn on : 53.0350

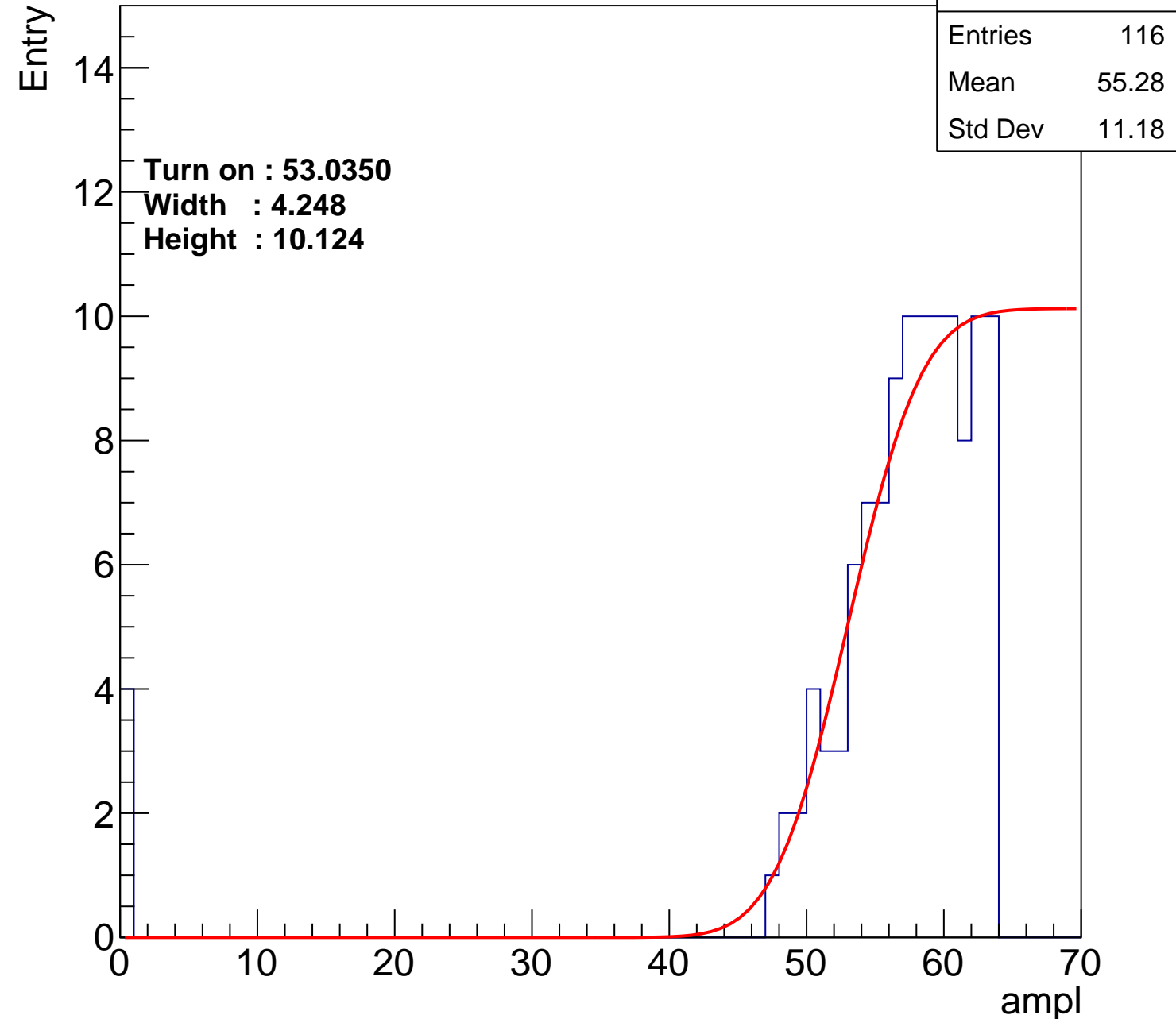
Width : 4.248

Height : 10.124

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch98

calib_packv5_040323_1717.root, FC#2, port C3

Entries	132
Mean	55.8
Std Dev	8.135

Turn on : 51.2458

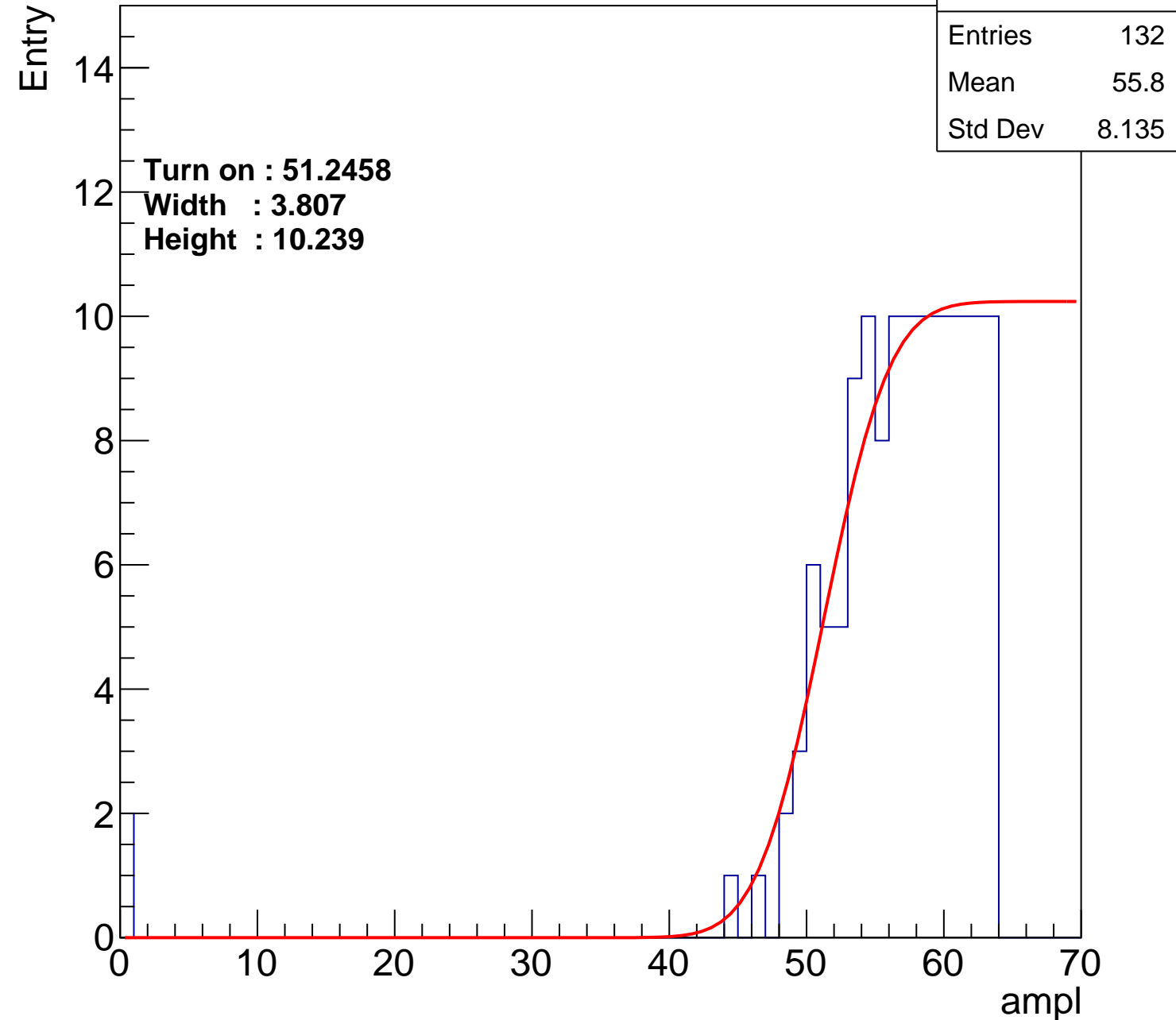
Width : 3.807

Height : 10.239

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch99

calib_packv5_040323_1717.root, FC#2, port C3

Entries	103
Mean	55.95
Std Dev	11.76

Turn on : 54.8440

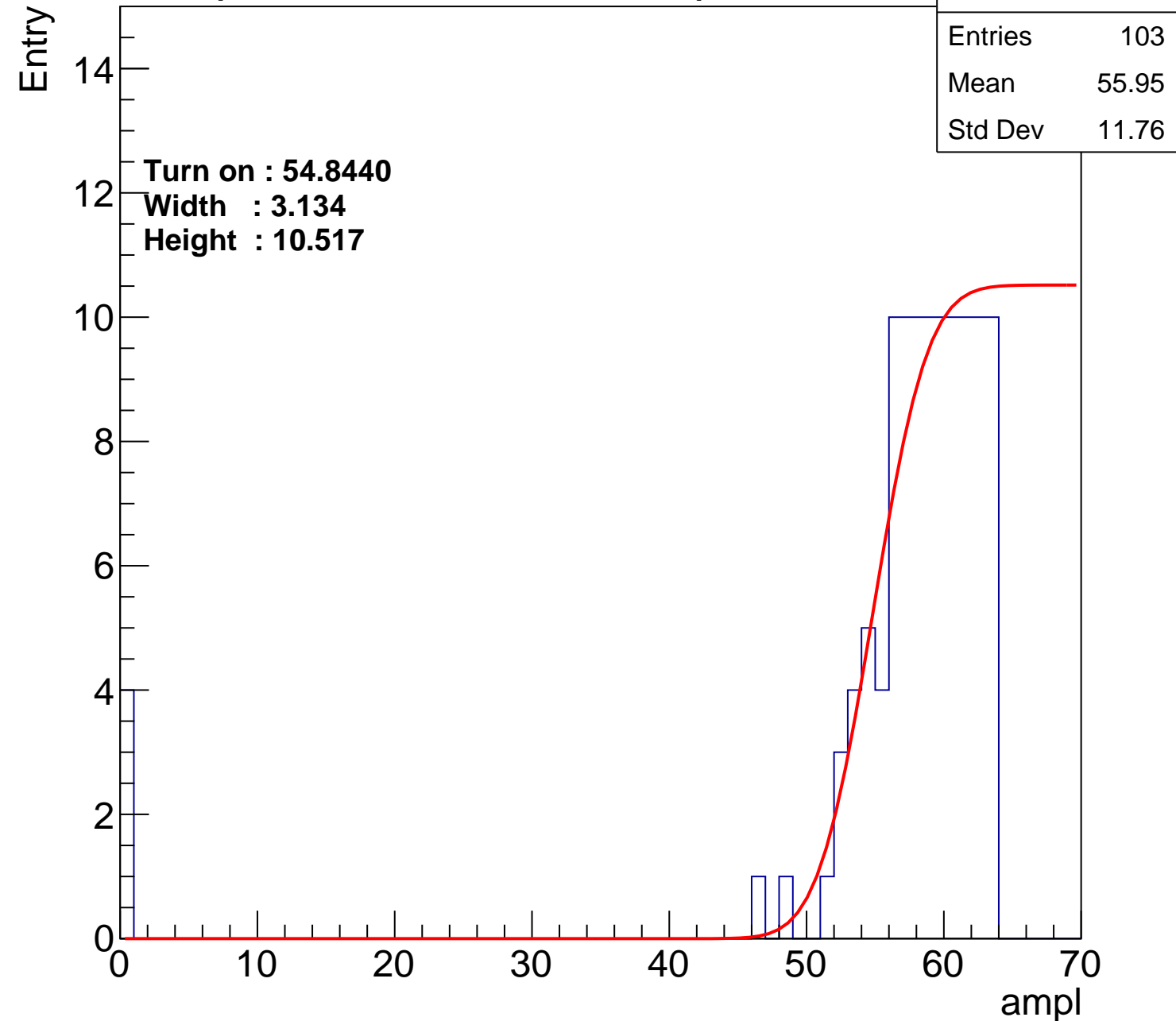
Width : 3.134

Height : 10.517

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch100

calib_packv5_040323_1717.root, FC#2, port C3

Entries	119
Mean	55.83
Std Dev	9.765

Turn on : 52.4019

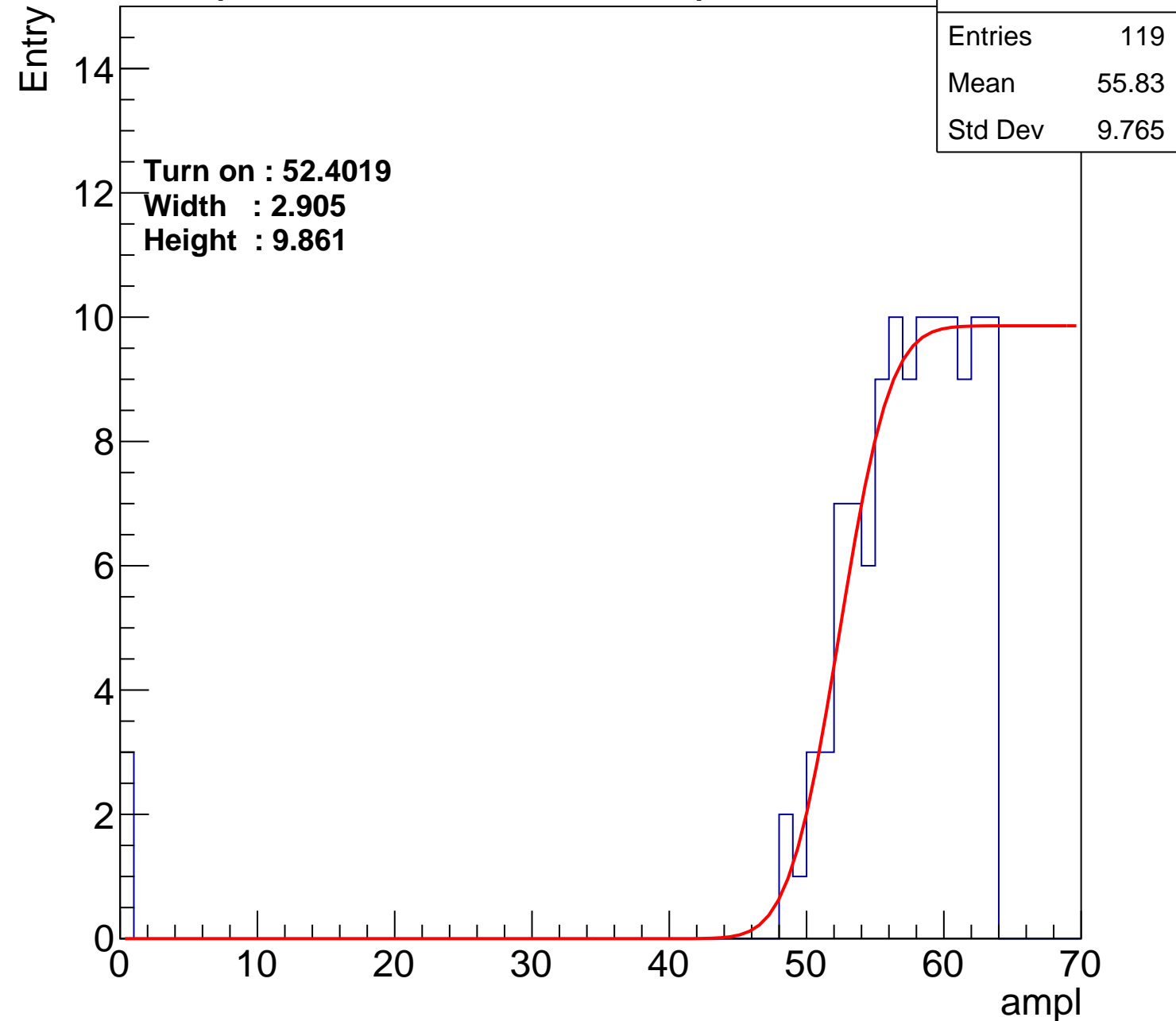
Width : 2.905

Height : 9.861

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch101

calib_packv5_040323_1717.root, FC#2, port C3

Entries	112
Mean	53.74
Std Dev	15.29

Turn on : 53.6184

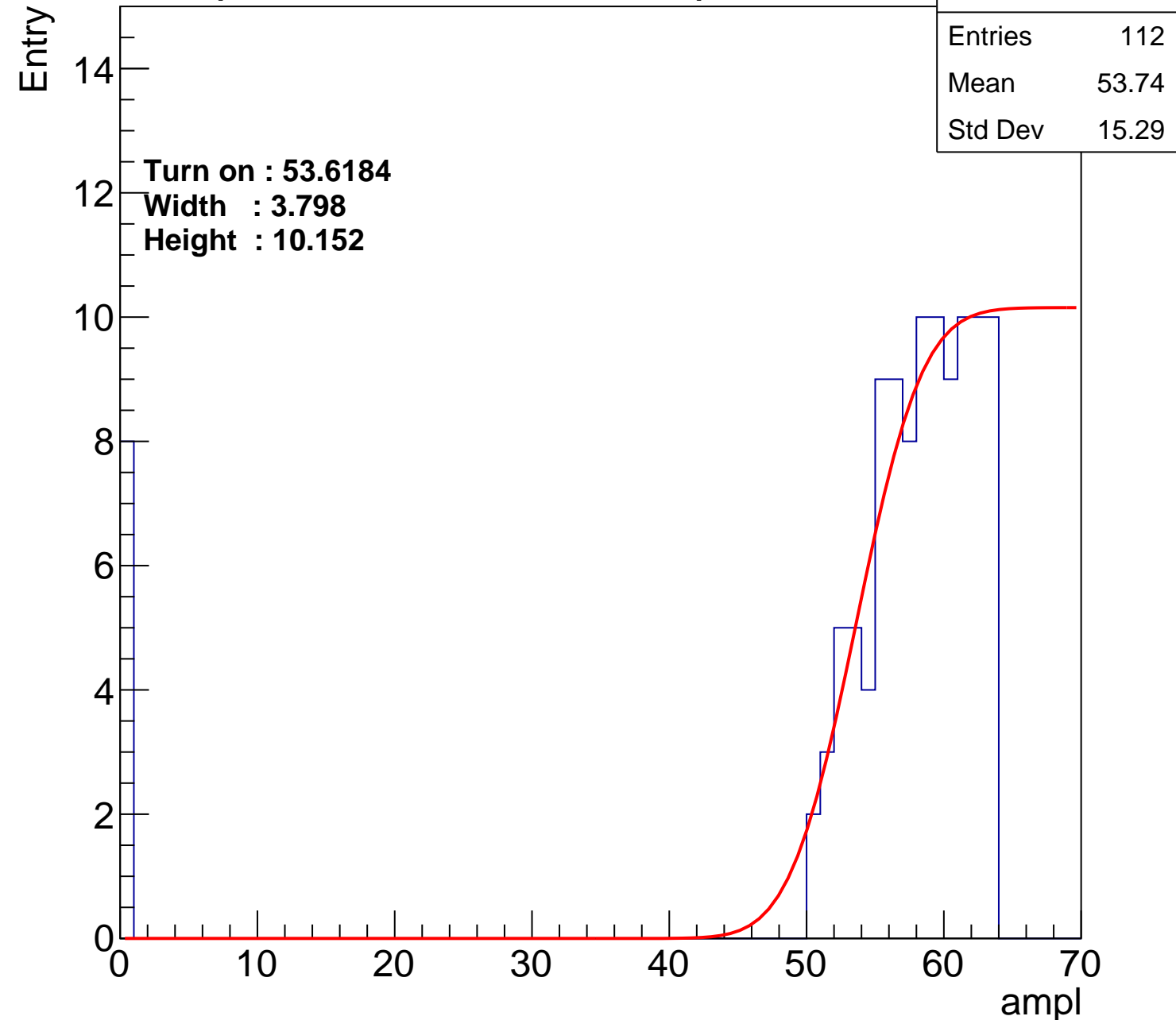
Width : 3.798

Height : 10.152

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch102

calib_packv5_040323_1717.root, FC#2, port C3

Entries	130
Mean	54.07
Std Dev	12.63

Turn on : 51.5400

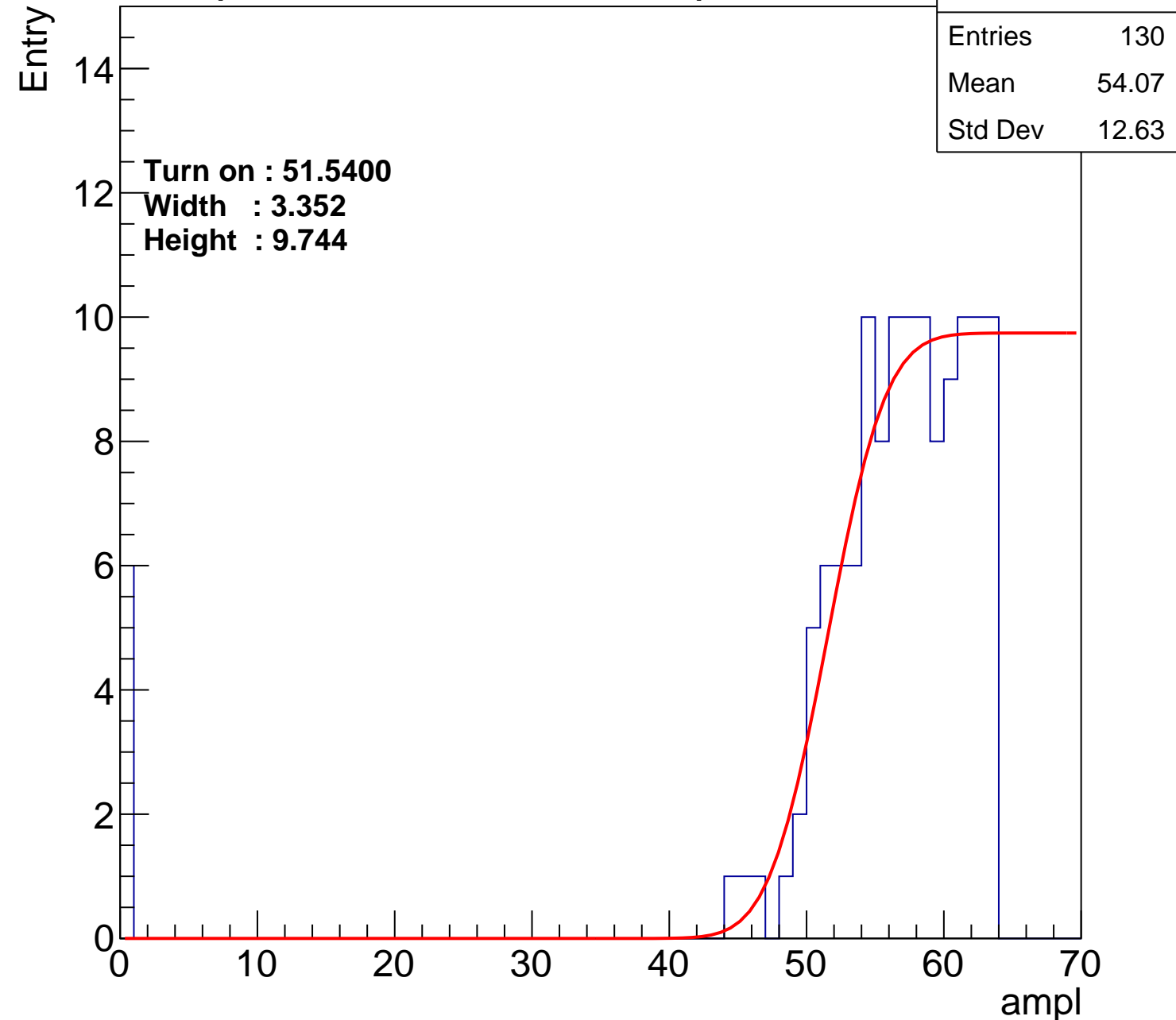
Width : 3.352

Height : 9.744

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch103

calib_packv5_040323_1717.root, FC#2, port C3

Entries	154
Mean	54.9
Std Dev	7.938

Turn on : 49.2779

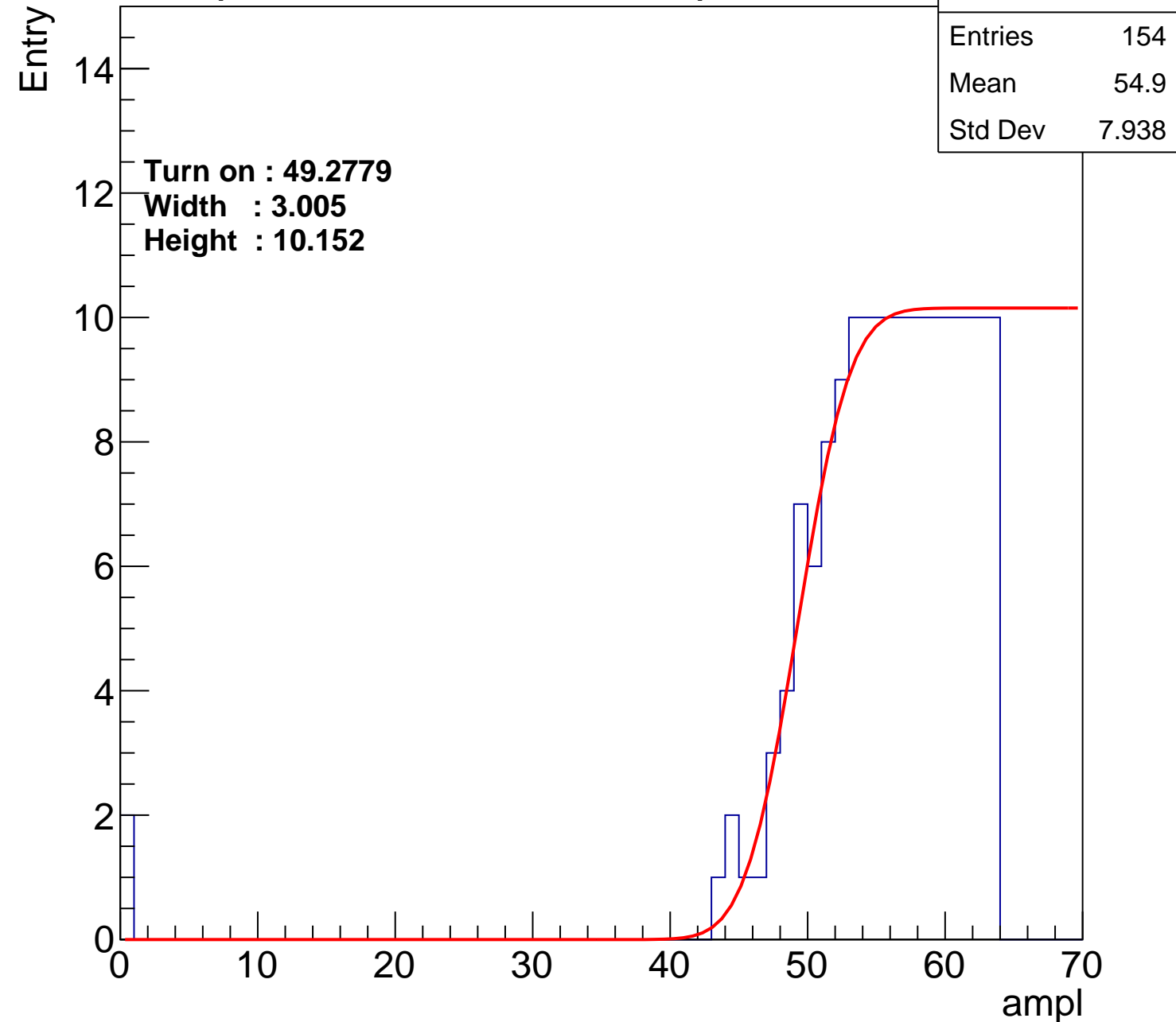
Width : 3.005

Height : 10.152

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch104

calib_packv5_040323_1717.root, FC#2, port C3

Entries	121
Mean	54.49
Std Dev	13.01

Turn on : 52.3492

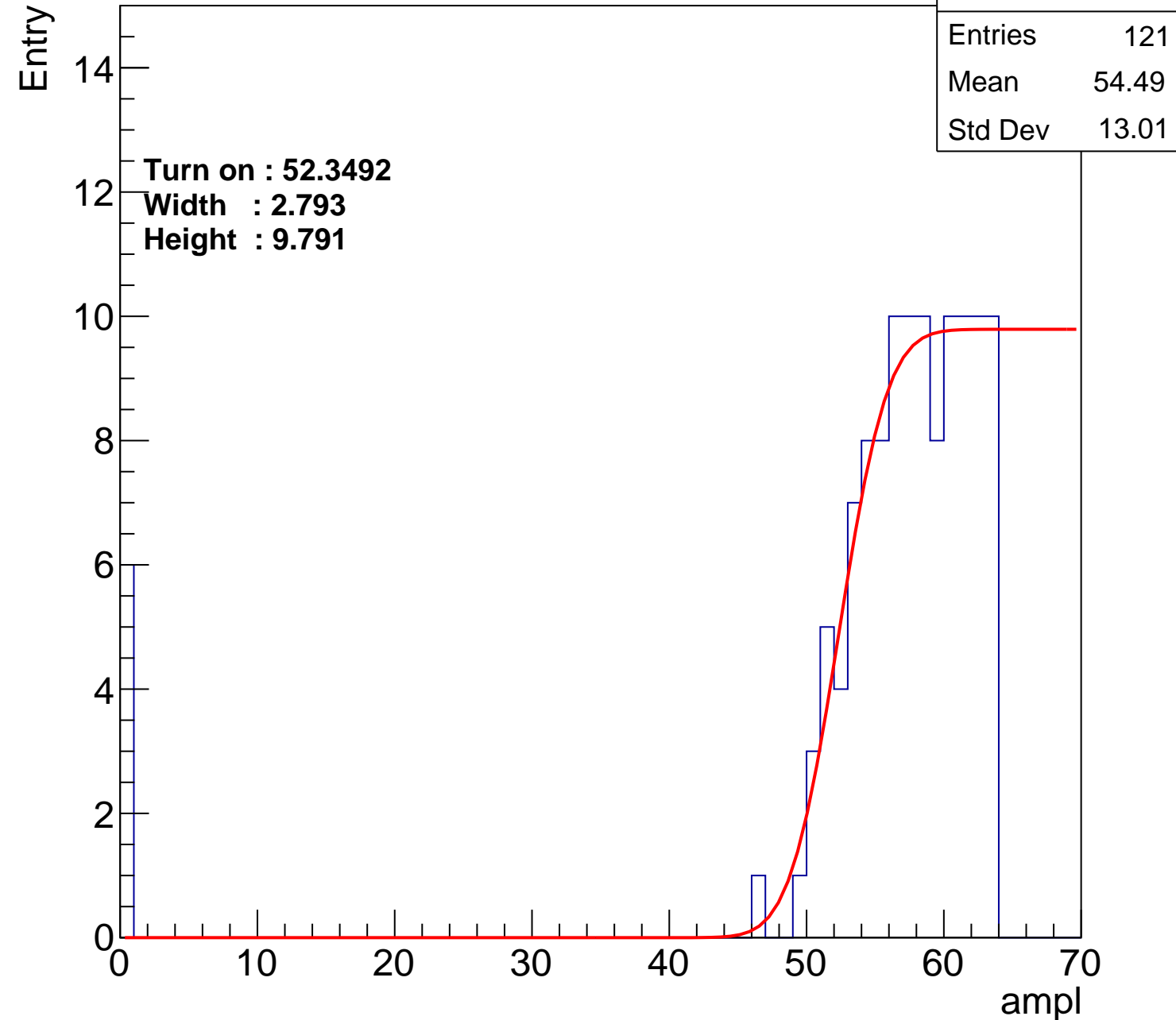
Width : 2.793

Height : 9.791

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch105

calib_packv5_040323_1717.root, FC#2, port C3

Entries	132
Mean	54.64
Std Dev	11.58

Turn on : 51.4737

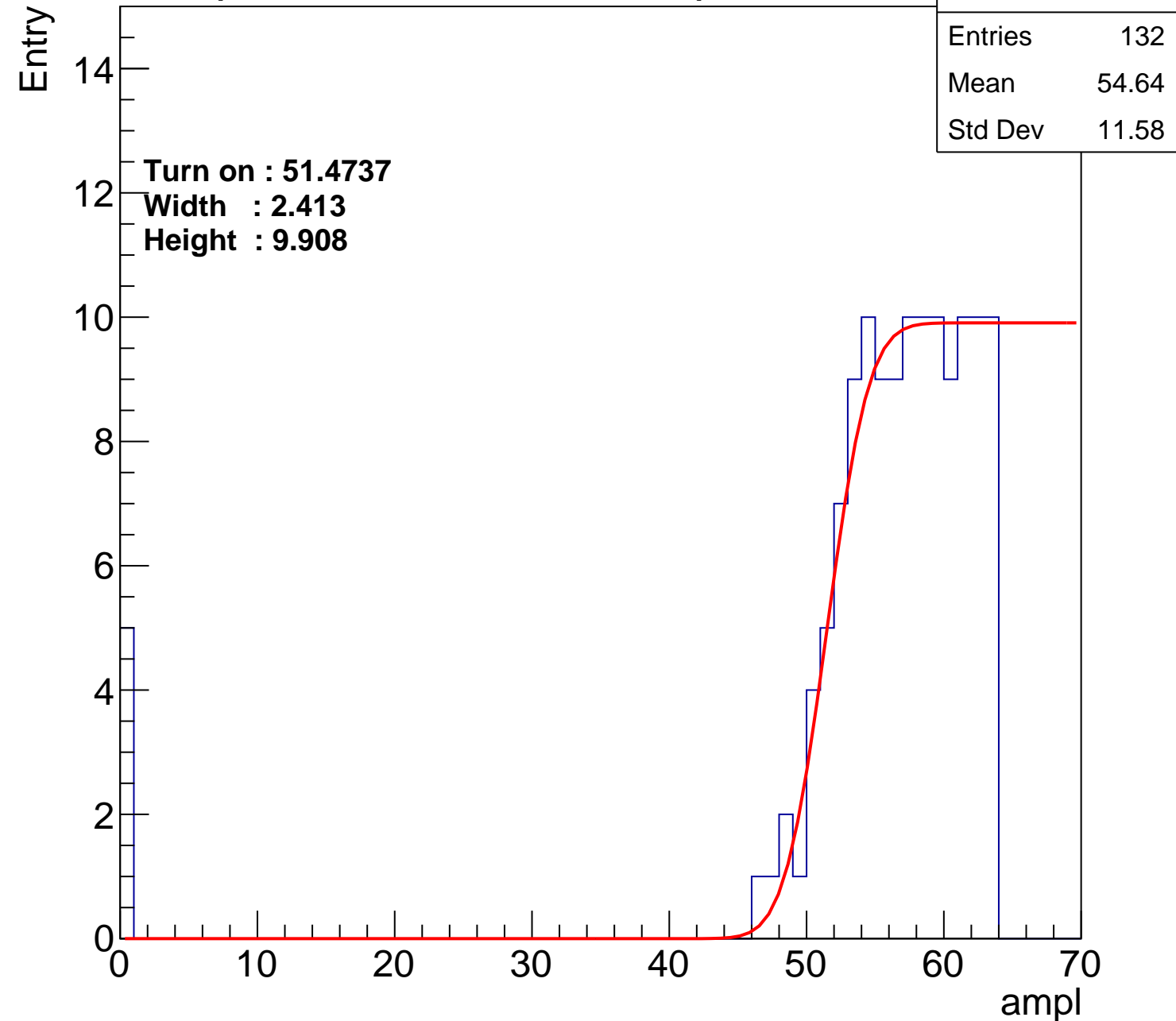
Width : 2.413

Height : 9.908

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch106

calib_packv5_040323_1717.root, FC#2, port C3

Entries	137
Mean	55.24
Std Dev	9.312

Turn on : 50.5355

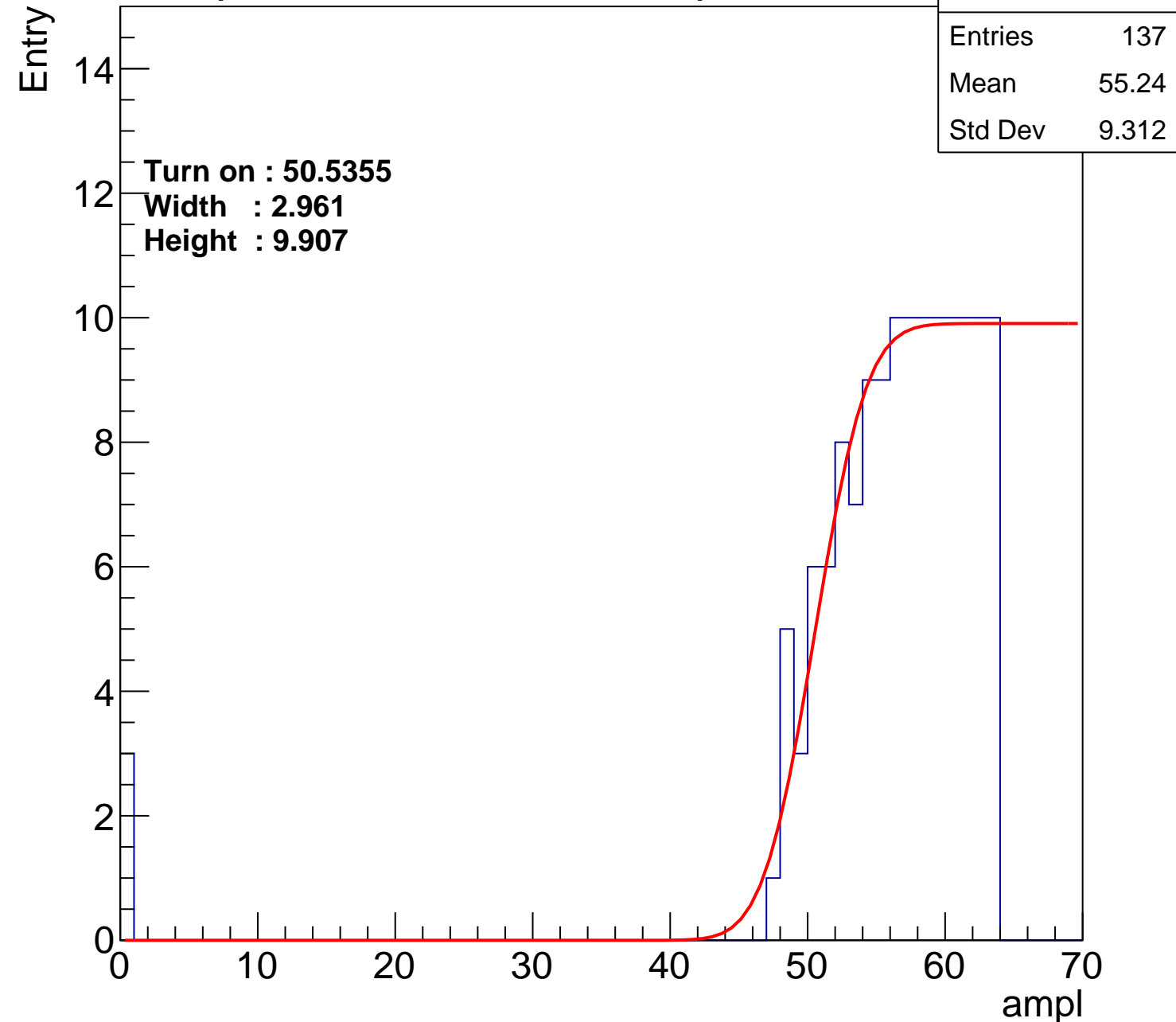
Width : 2.961

Height : 9.907

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch107

calib_packv5_040323_1717.root, FC#2, port C3

Entries	143
Mean	55.27
Std Dev	7.998

Turn on : 50.5522

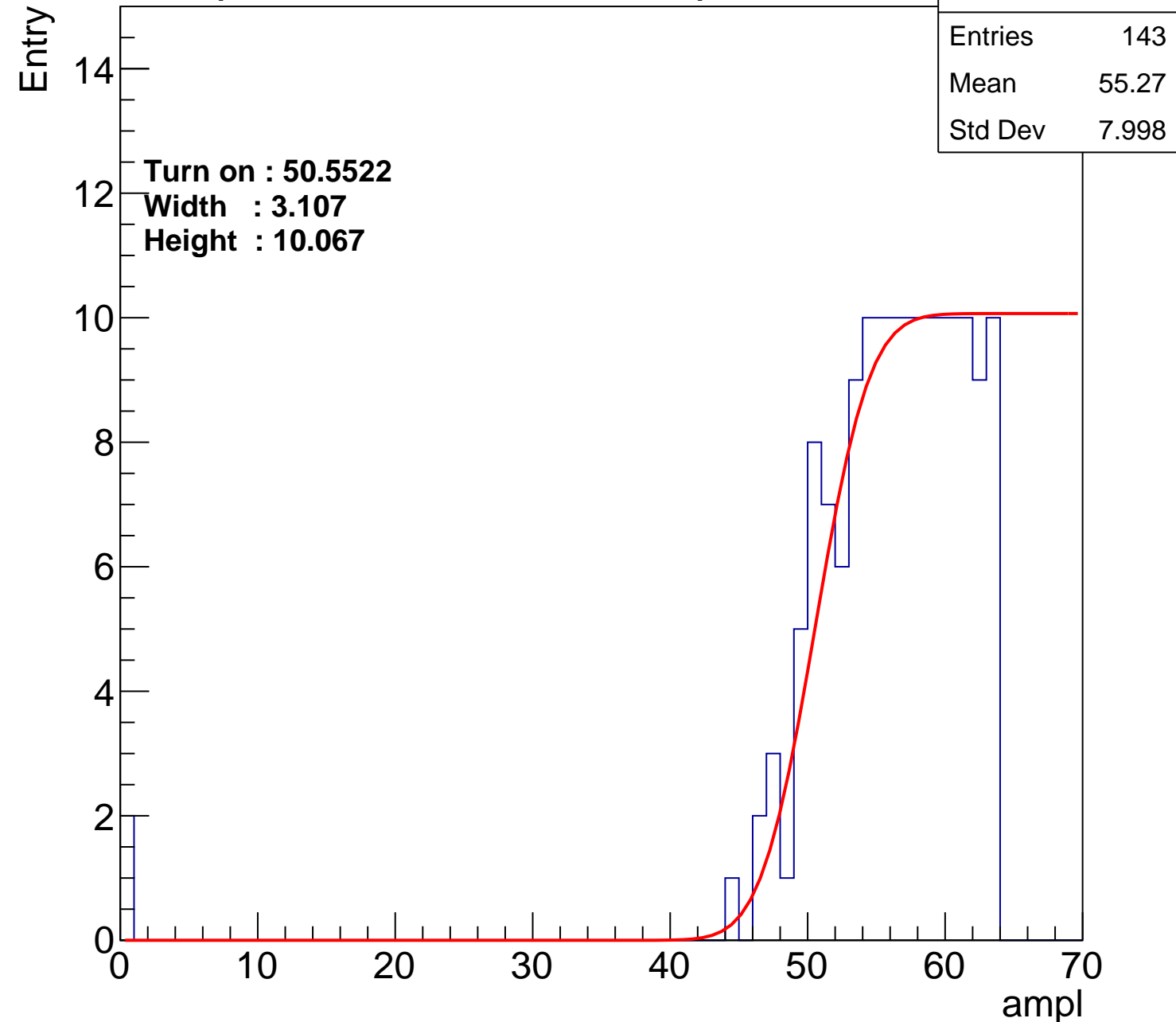
Width : 3.107

Height : 10.067

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch108

calib_packv5_040323_1717.root, FC#2, port C3

Entries	139
Mean	54.72
Std Dev	10.43

Turn on : 51.0810

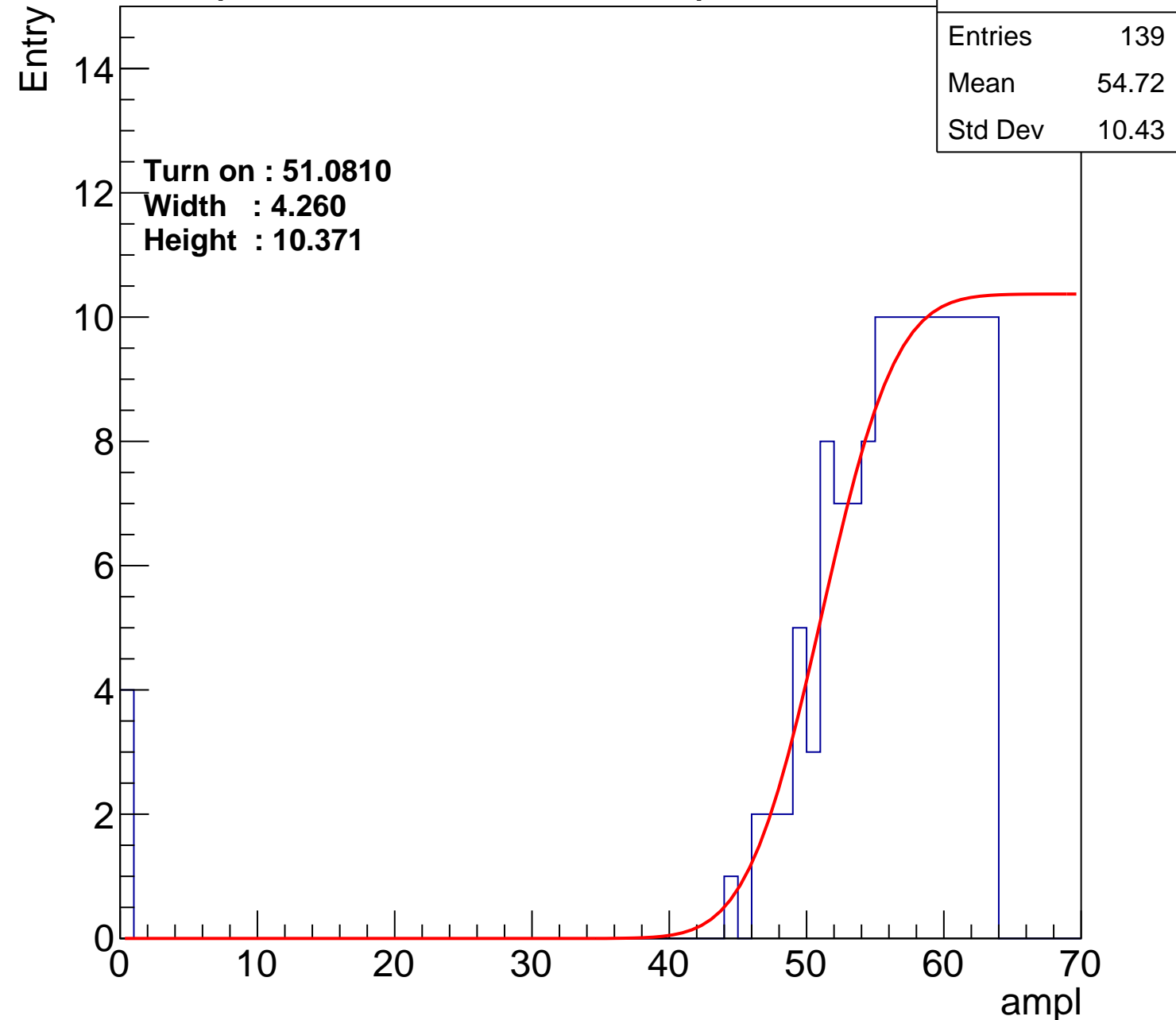
Width : 4.260

Height : 10.371

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch109

calib_packv5_040323_1717.root, FC#2, port C3

Entries	113
Mean	56.59
Std Dev	8.418

Turn on : 52.9564

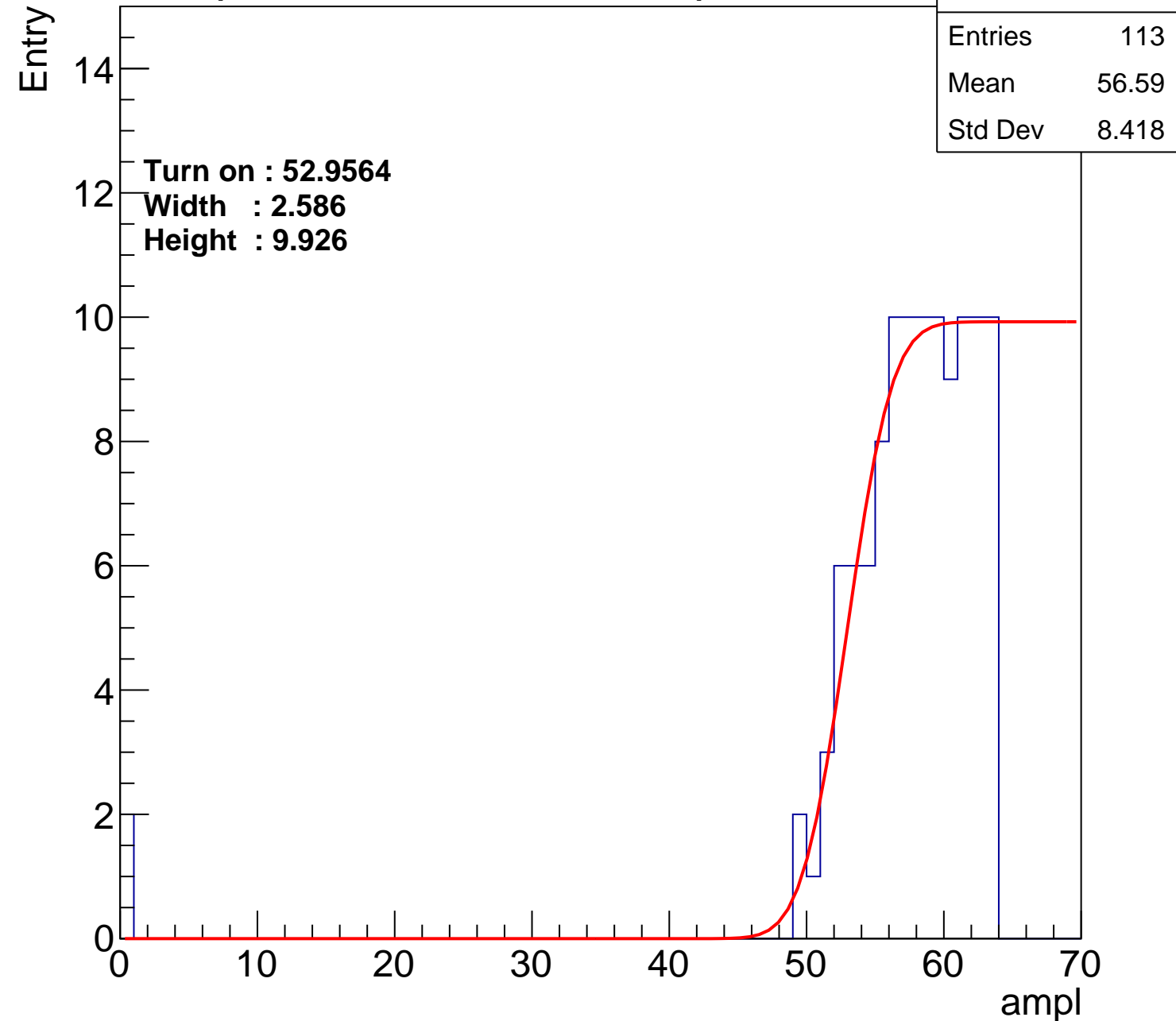
Width : 2.586

Height : 9.926

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch110

calib_packv5_040323_1717.root, FC#2, port C3

Entries	152
Mean	54.5
Std Dev	9.105

Turn on : 48.6109

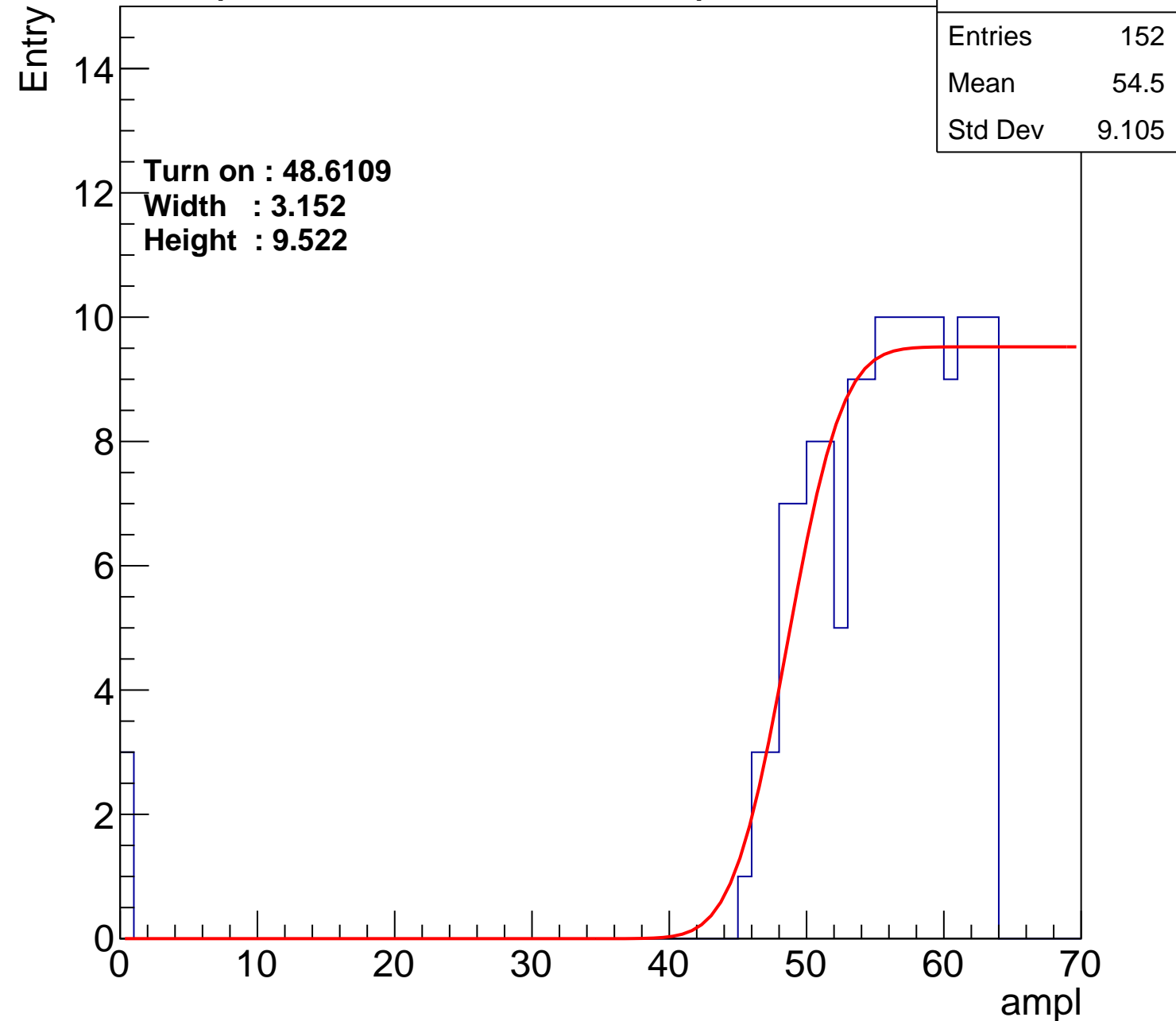
Width : 3.152

Height : 9.522

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch111

calib_packv5_040323_1717.root, FC#2, port C3

Entries	127
Mean	54.87
Std Dev	11.79

Turn on : 52.3411

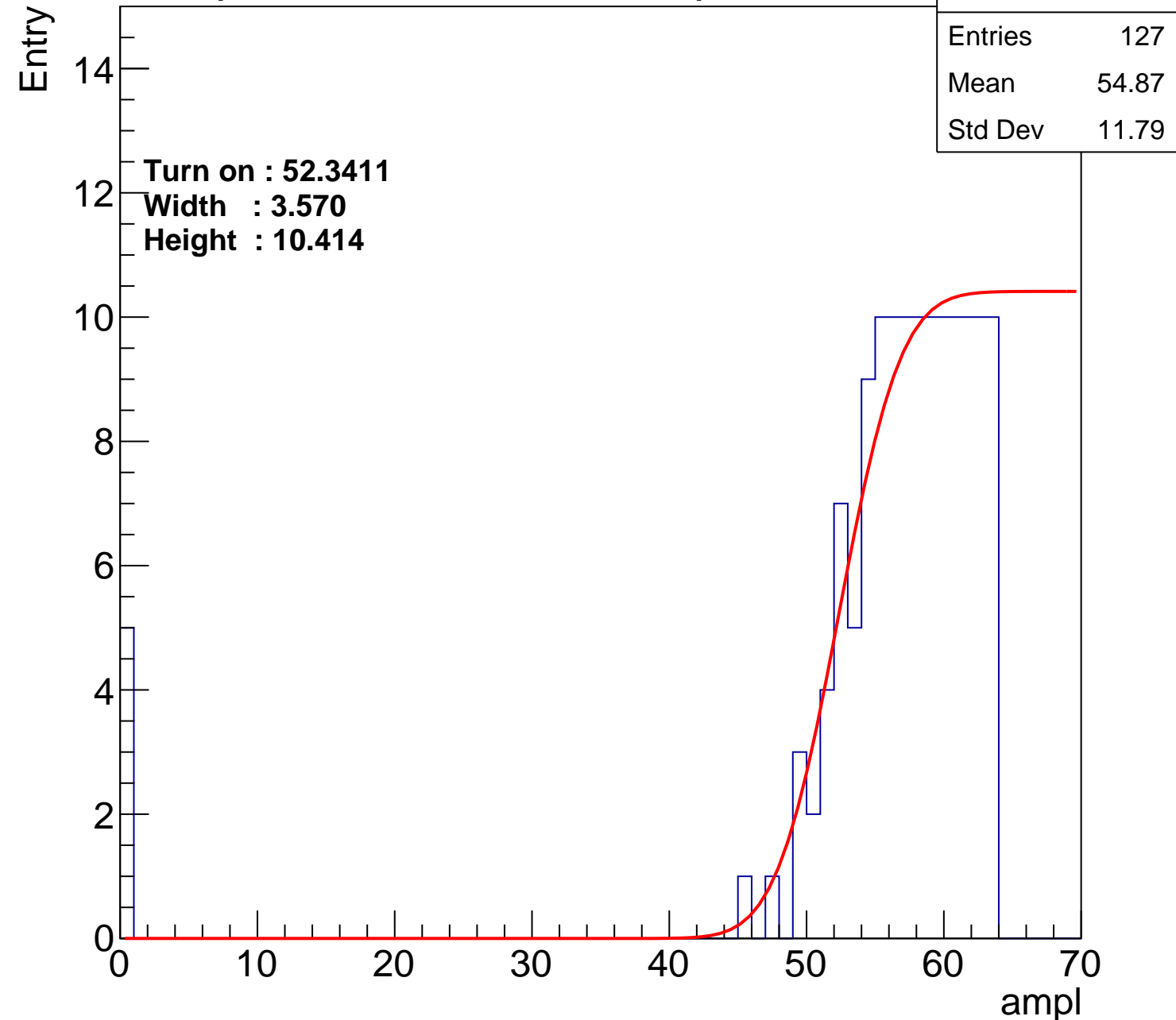
Width : 3.570

Height : 10.414

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch112

calib_packv5_040323_1717.root, FC#2, port C3

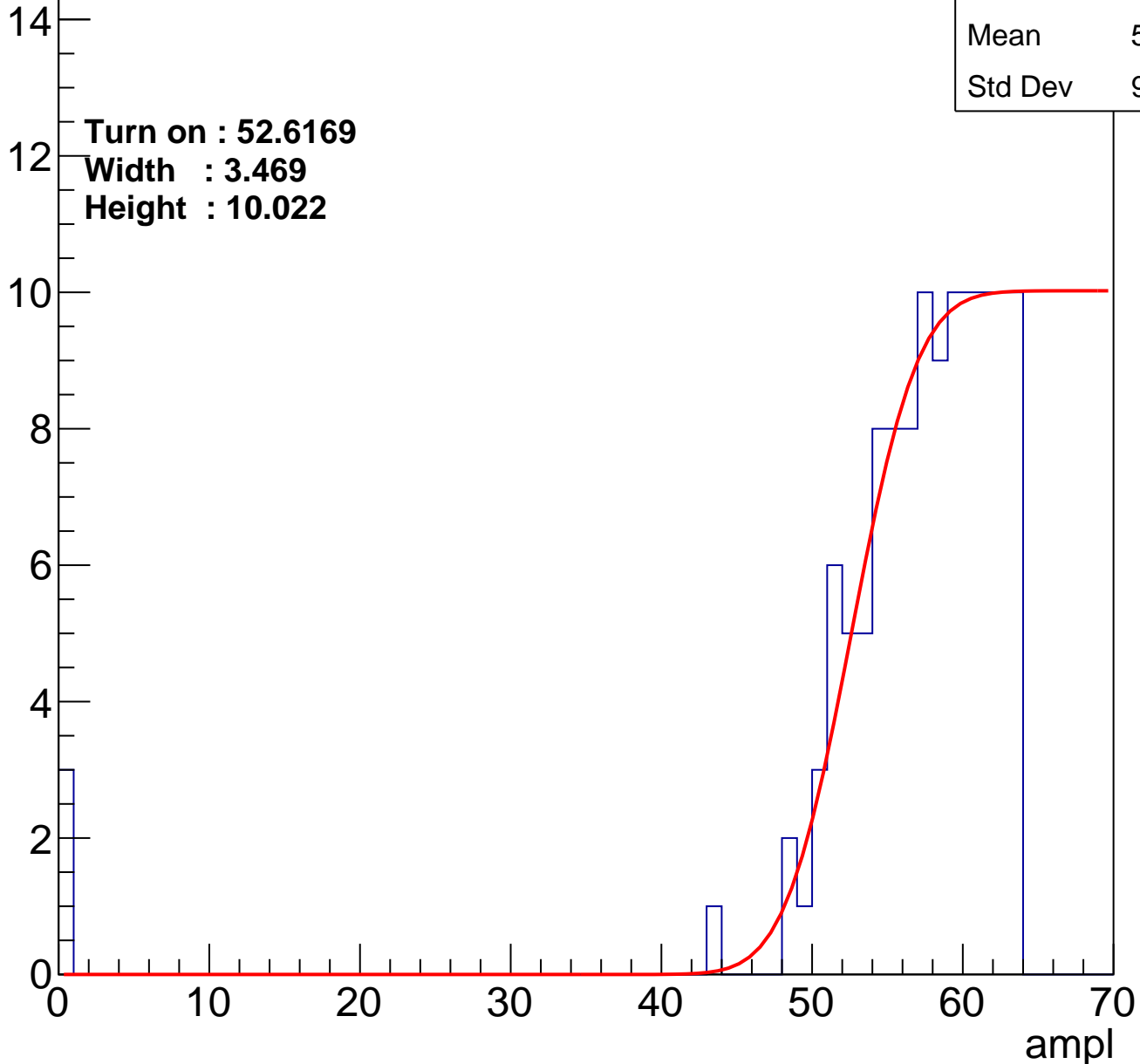
Entries	119
Mean	55.72
Std Dev	9.858

Turn on : 52.6169

Width : 3.469

Height : 10.022

Entry



B0L103S, U12-ch113

calib_packv5_040323_1717.root, FC#2, port C3

Entries	112
Mean	56.19
Std Dev	9.992

Turn on : 53.6773

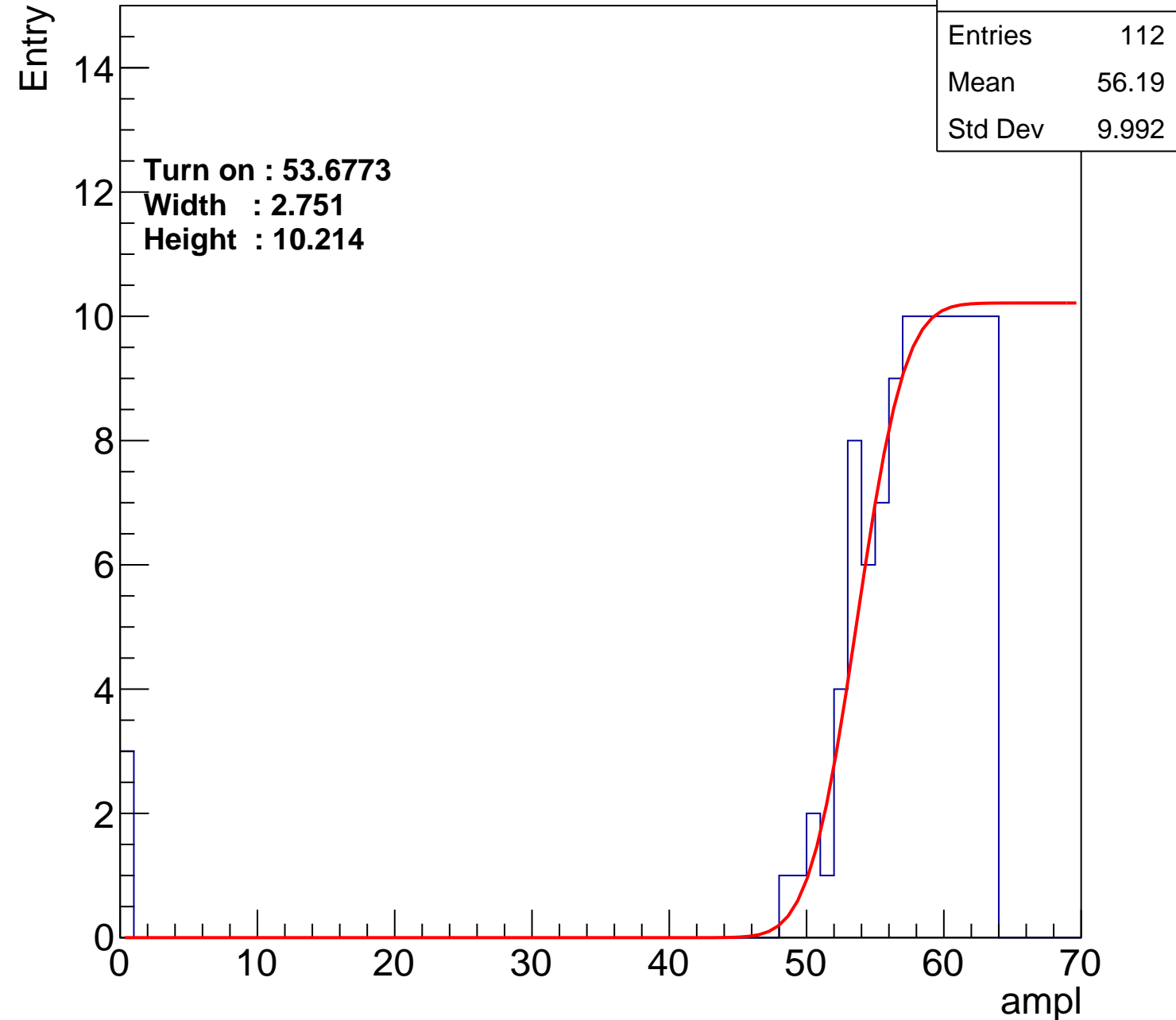
Width : 2.751

Height : 10.214

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch114

calib_packv5_040323_1717.root, FC#2, port C3

Entries	128
Mean	53.57
Std Dev	14.34

Turn on : 52.0585

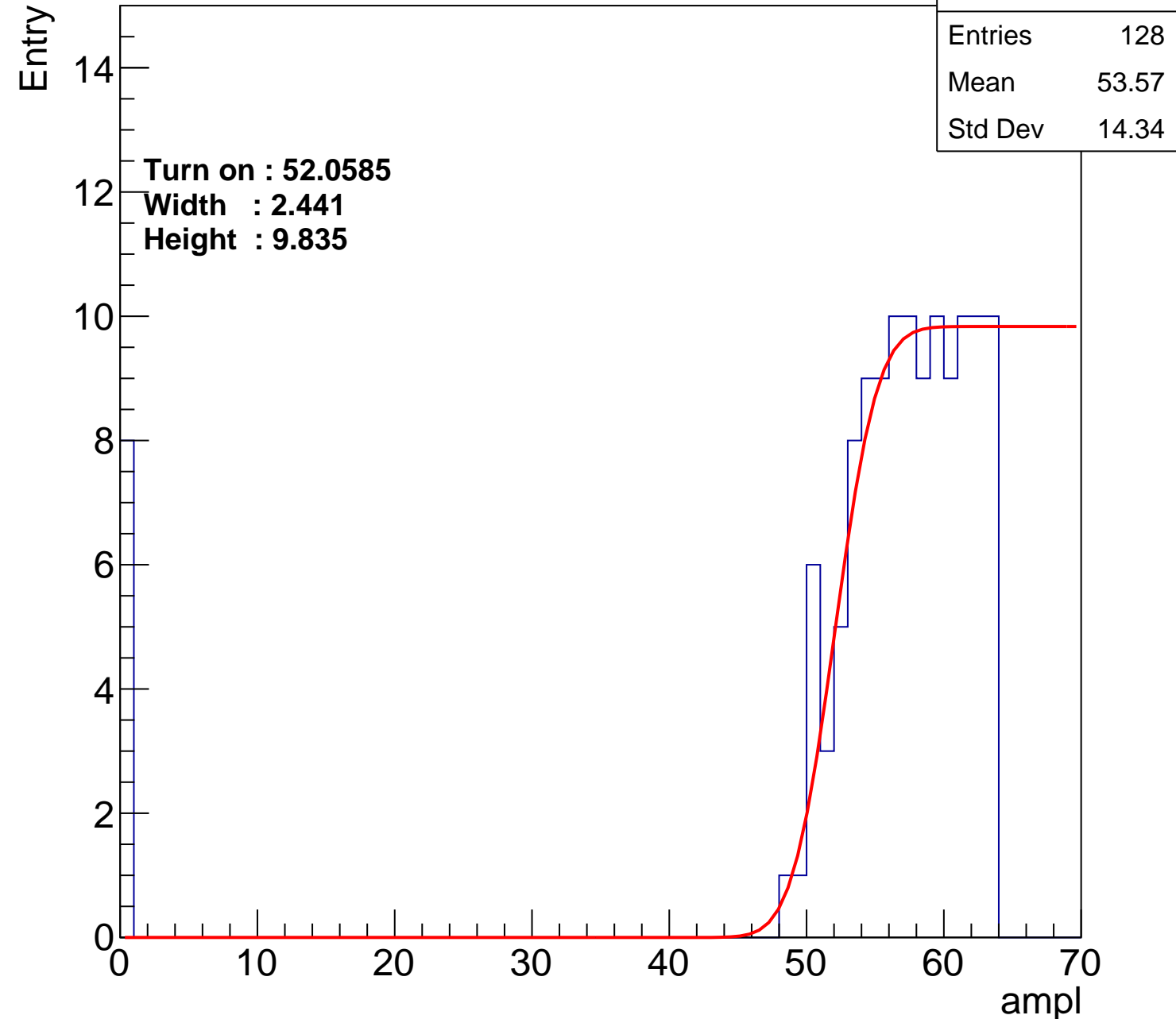
Width : 2.441

Height : 9.835

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch115

calib_packv5_040323_1717.root, FC#2, port C3

Entries	114
Mean	55.65
Std Dev	11.22

Turn on : 55.1021

Width : 3.213

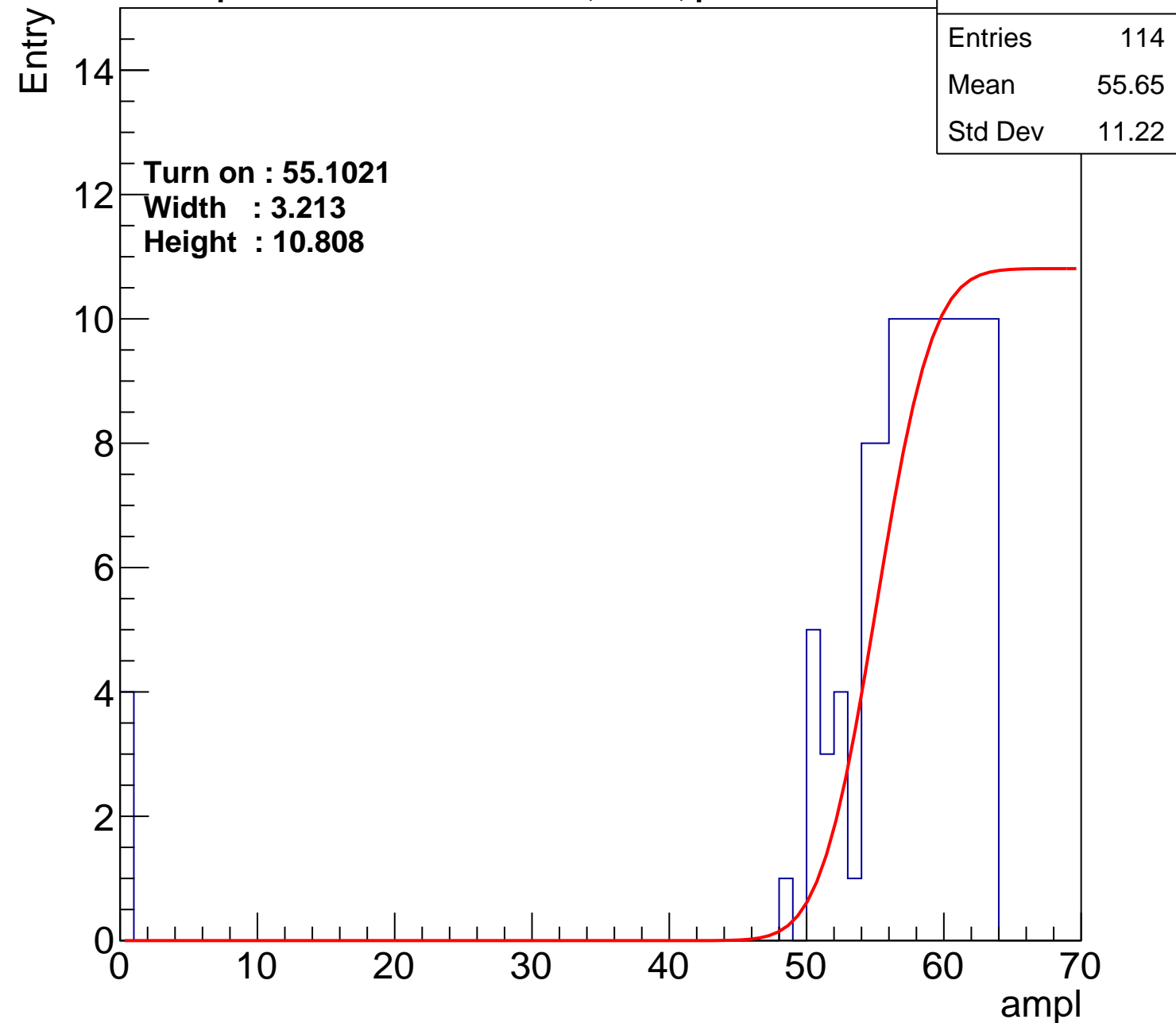
Height : 10.808

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B0L103S, U12-ch116

calib_packv5_040323_1717.root, FC#2, port C3

Entries	134
Mean	56.04
Std Dev	6.496

Turn on : 50.7139

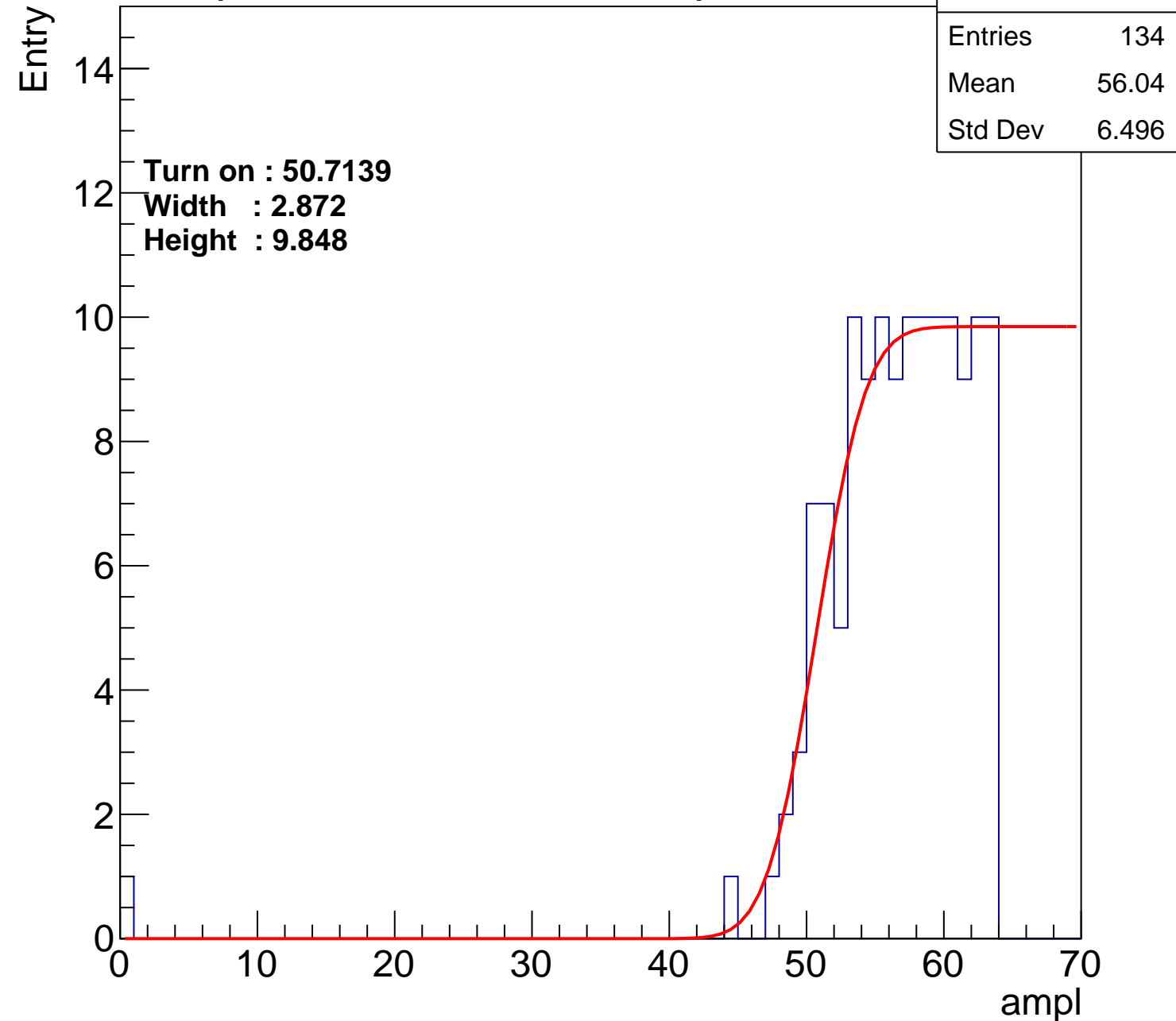
Width : 2.872

Height : 9.848

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch117

calib_packv5_040323_1717.root, FC#2, port C3

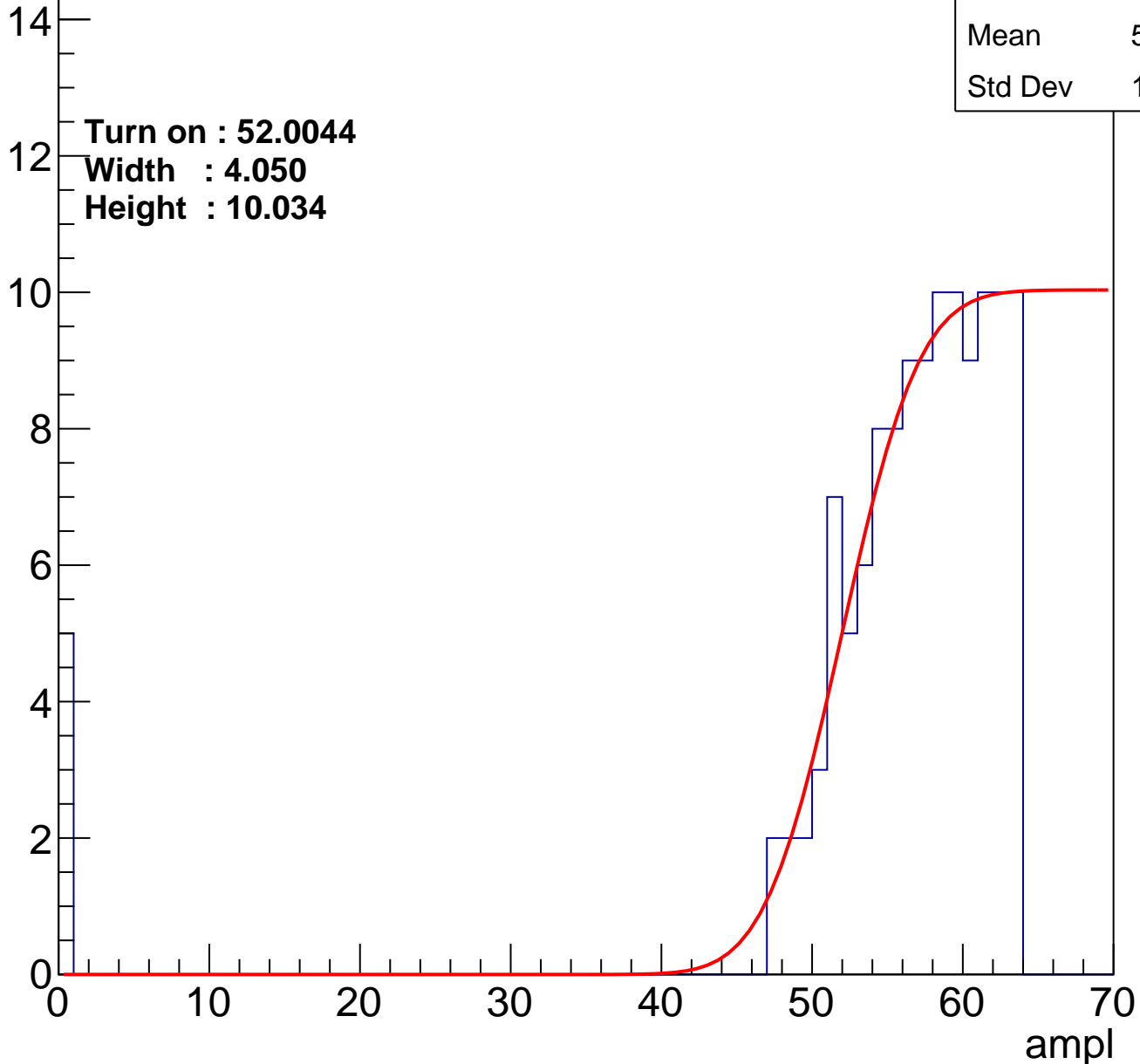
Entries	125
Mean	54.66
Std Dev	11.89

Turn on : 52.0044

Width : 4.050

Height : 10.034

Entry



B0L103S, U12-ch118

calib_packv5_040323_1717.root, FC#2, port C3

Entries	130
Mean	55.5
Std Dev	9.489

Turn on : 51.4225

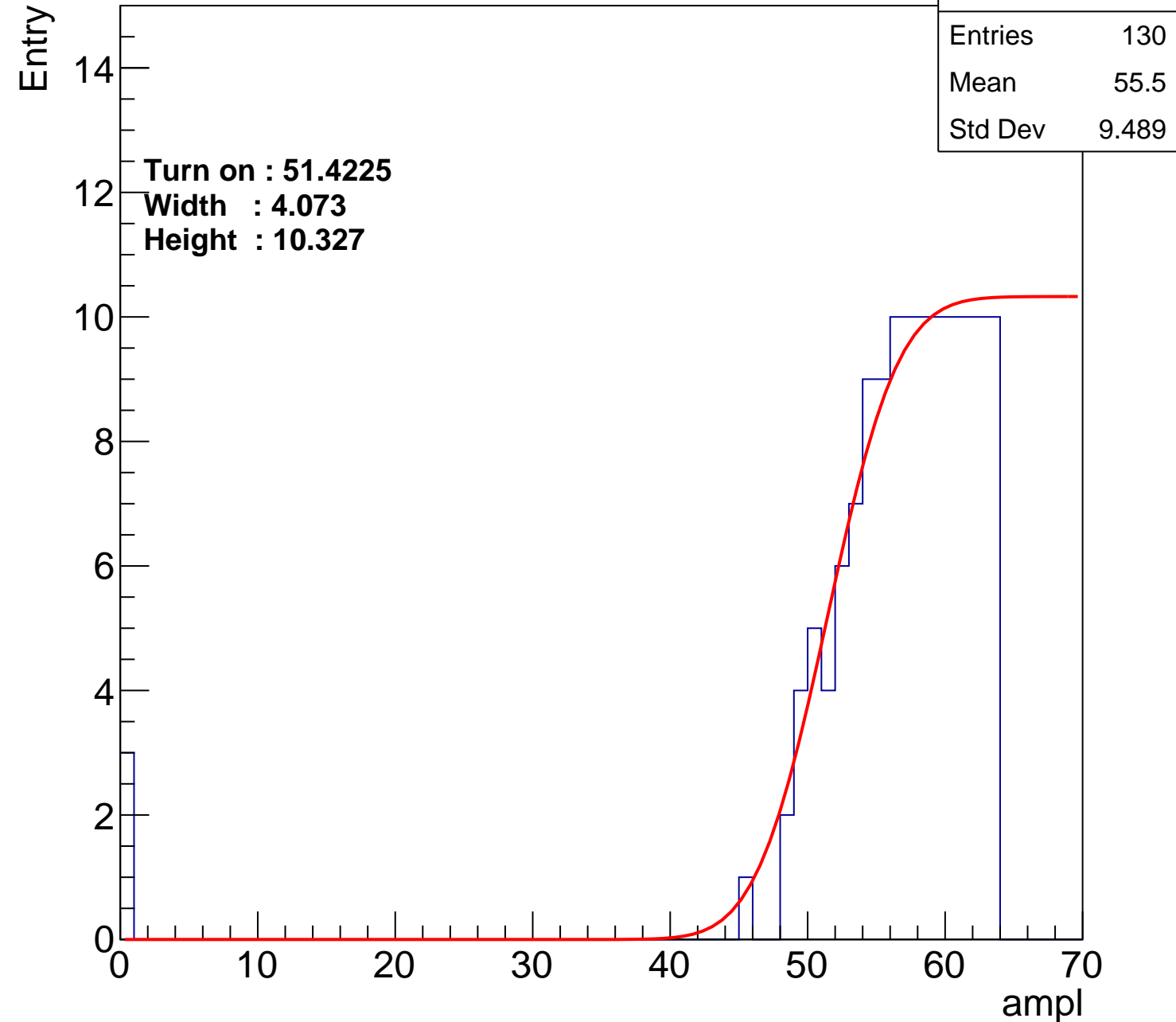
Width : 4.073

Height : 10.327

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch119

calib_packv5_040323_1717.root, FC#2, port C3

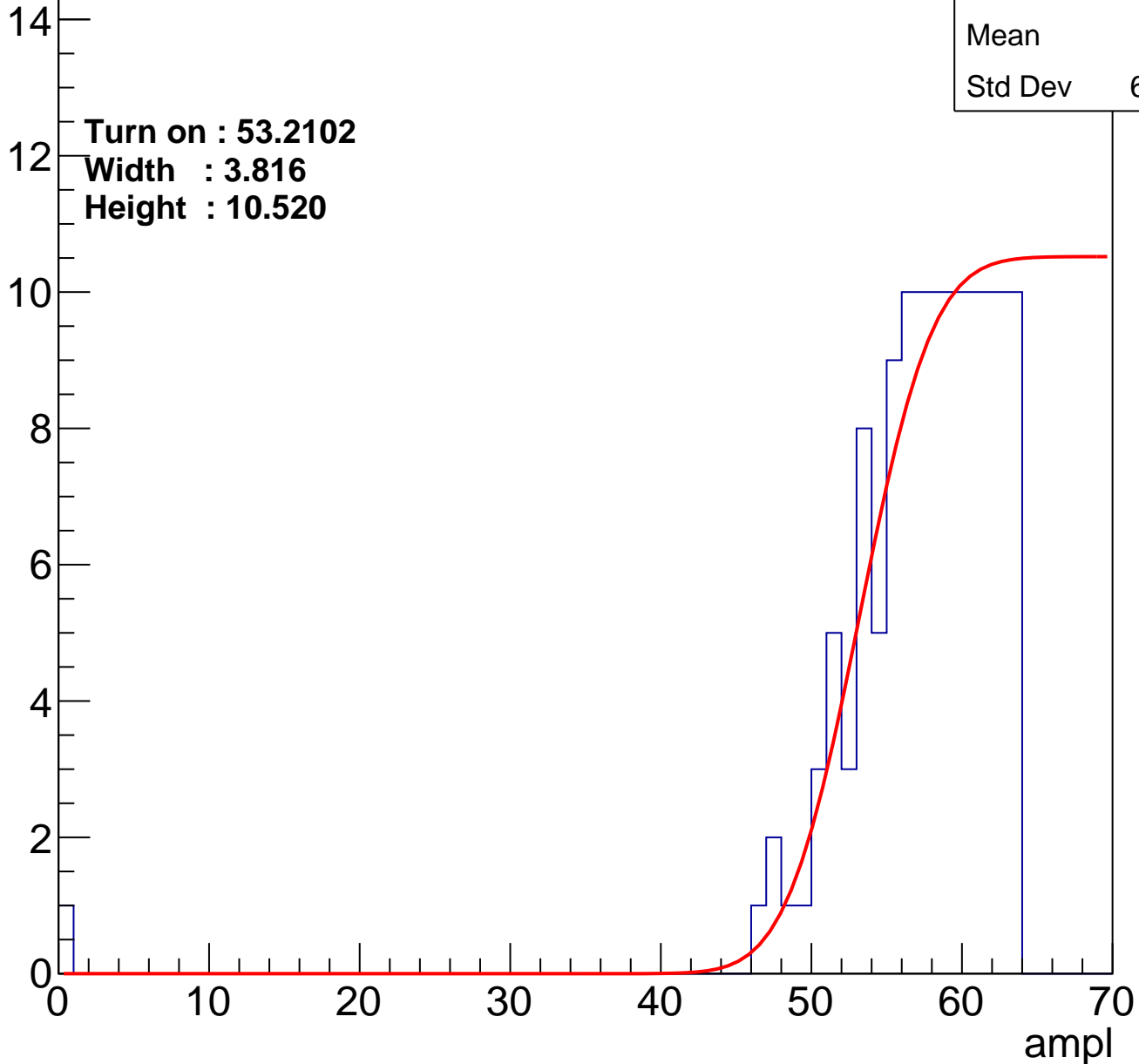
Entries	119
Mean	56.7
Std Dev	6.633

Turn on : 53.2102

Width : 3.816

Height : 10.520

Entry



B0L103S, U12-ch120

calib_packv5_040323_1717.root, FC#2, port C3

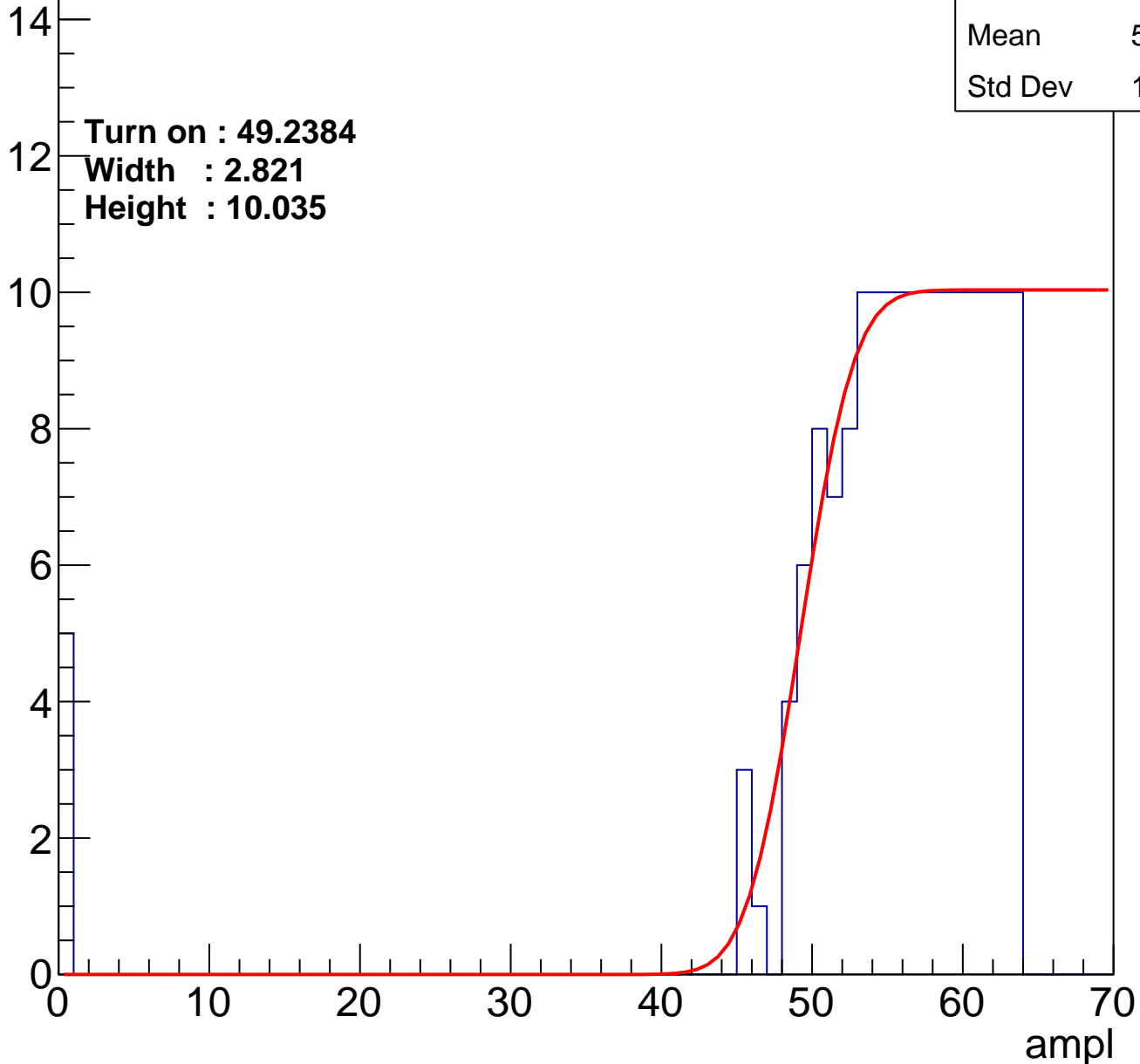
Entries	152
Mean	54.08
Std Dev	10.96

Turn on : 49.2384

Width : 2.821

Height : 10.035

Entry



B0L103S, U12-ch121

calib_packv5_040323_1717.root, FC#2, port C3

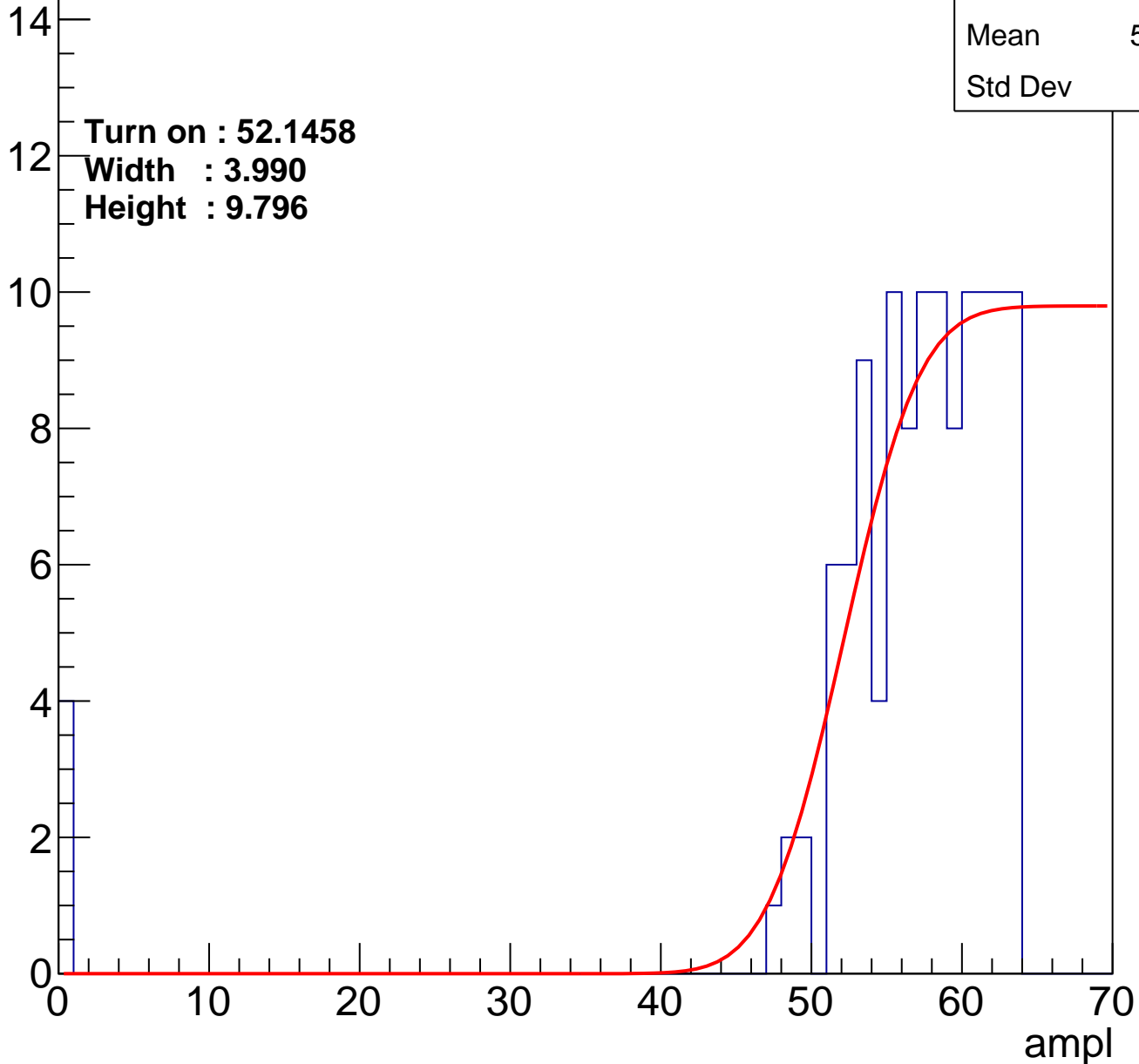
Entries	120
Mean	55.27
Std Dev	11

Turn on : 52.1458

Width : 3.990

Height : 9.796

Entry



B0L103S, U12-ch122

calib_packv5_040323_1717.root, FC#2, port C3

Entries	126
Mean	55.49
Std Dev	9.615

Turn on : 51.6867

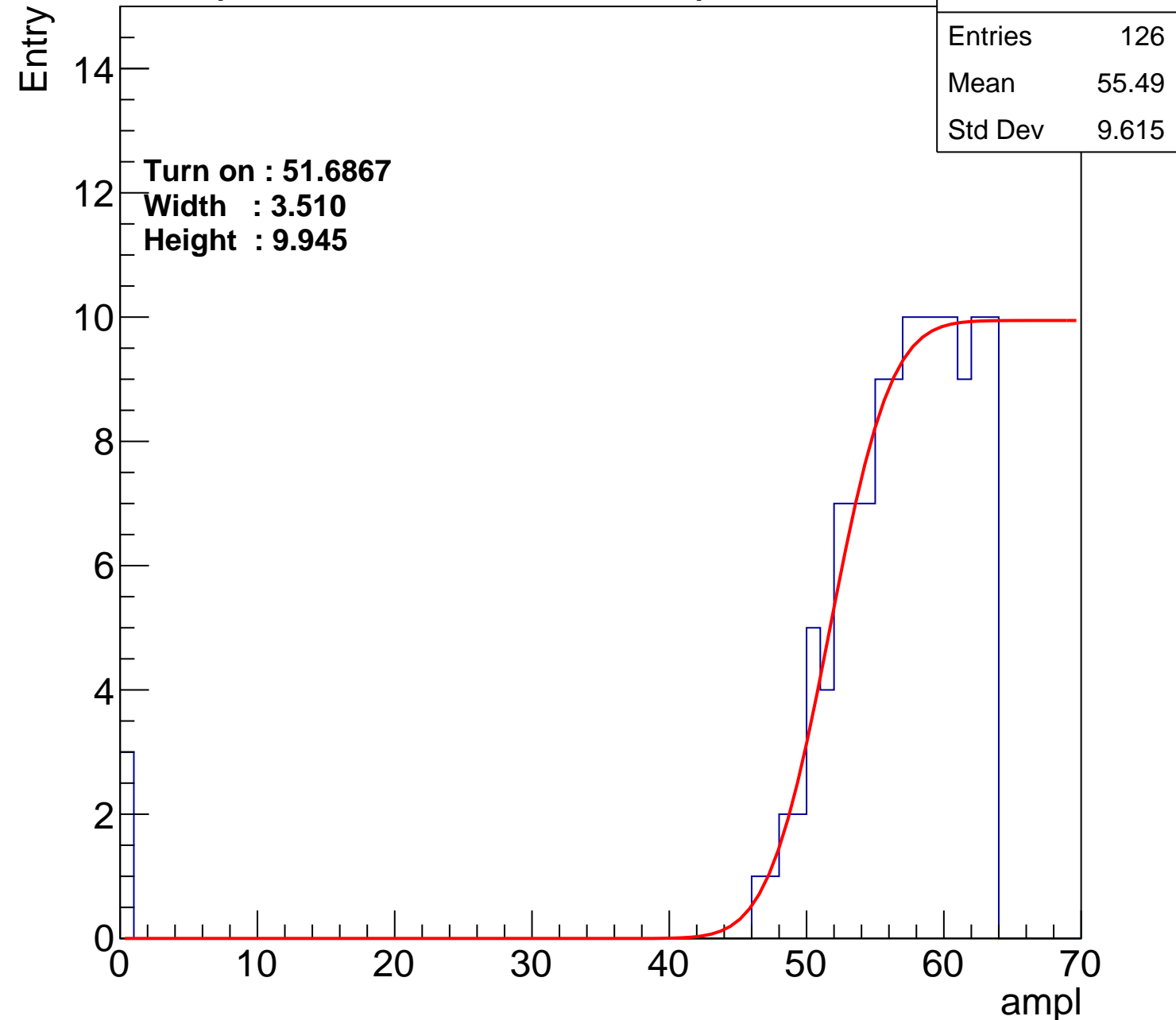
Width : 3.510

Height : 9.945

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch123

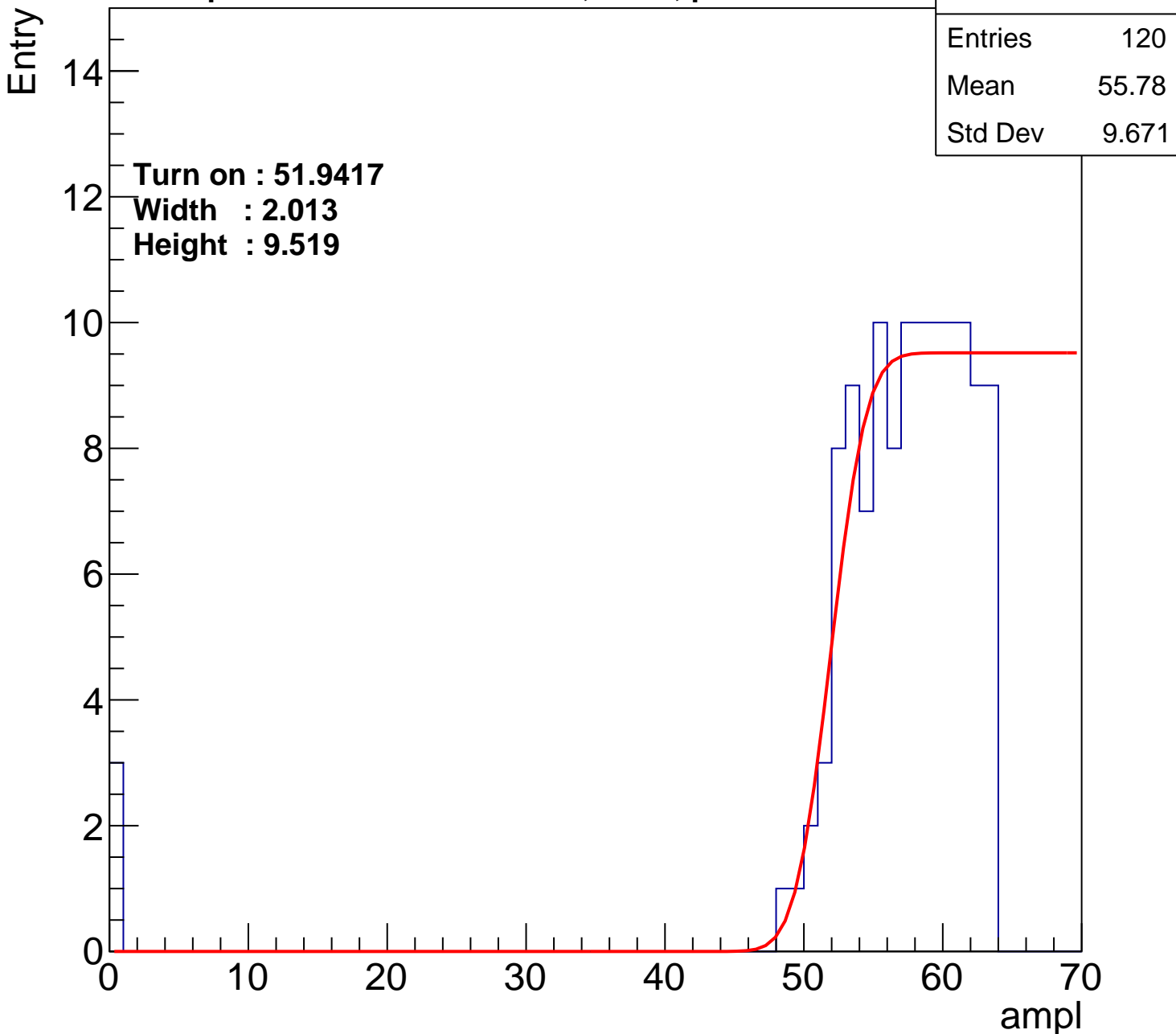
calib_packv5_040323_1717.root, FC#2, port C3

Turn on : 51.9417

Width : 2.013

Height : 9.519

Entries	120
Mean	55.78
Std Dev	9.671



B0L103S, U12-ch124

calib_packv5_040323_1717.root, FC#2, port C3

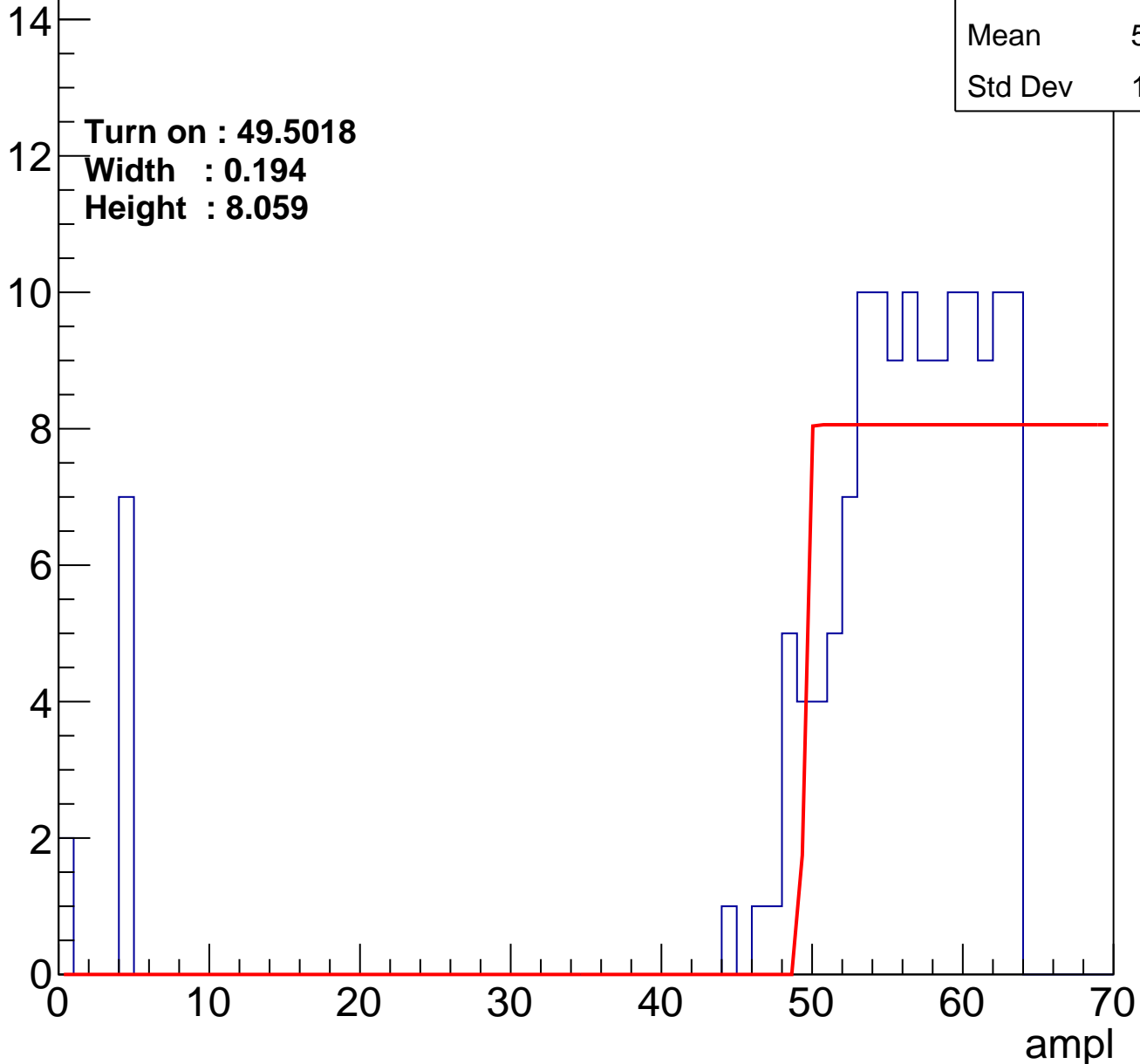
Entries	143
Mean	52.93
Std Dev	13.63

Turn on : 49.5018

Width : 0.194

Height : 8.059

Entry



B0L103S, U12-ch125

calib_packv5_040323_1717.root, FC#2, port C3

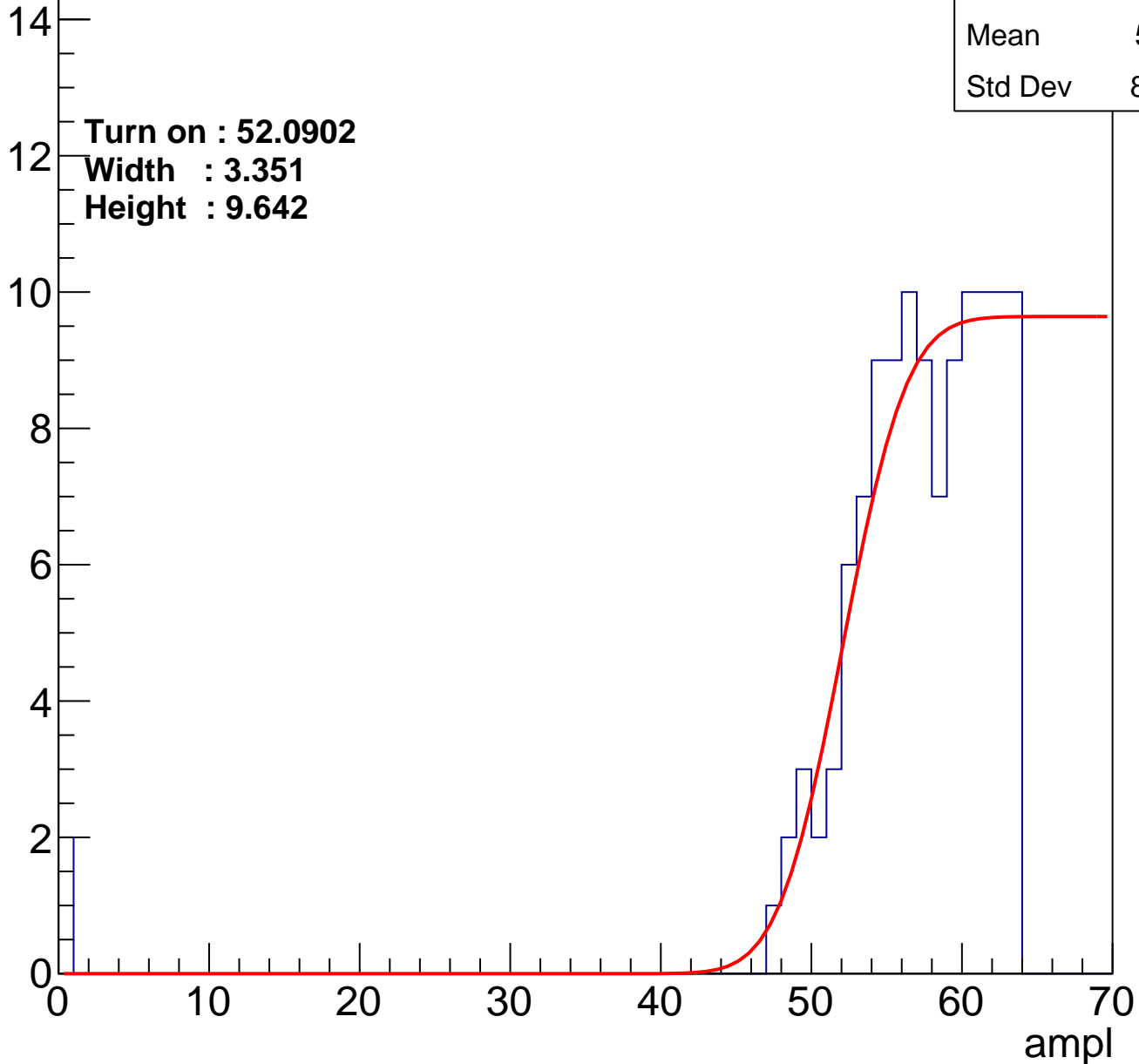
Entries	119
Mean	56.11
Std Dev	8.379

Turn on : 52.0902

Width : 3.351

Height : 9.642

Entry



B0L103S, U12-ch126

calib_packv5_040323_1717.root, FC#2, port C3

Entries	131
Mean	56.18
Std Dev	6.538

Turn on : 51.3474

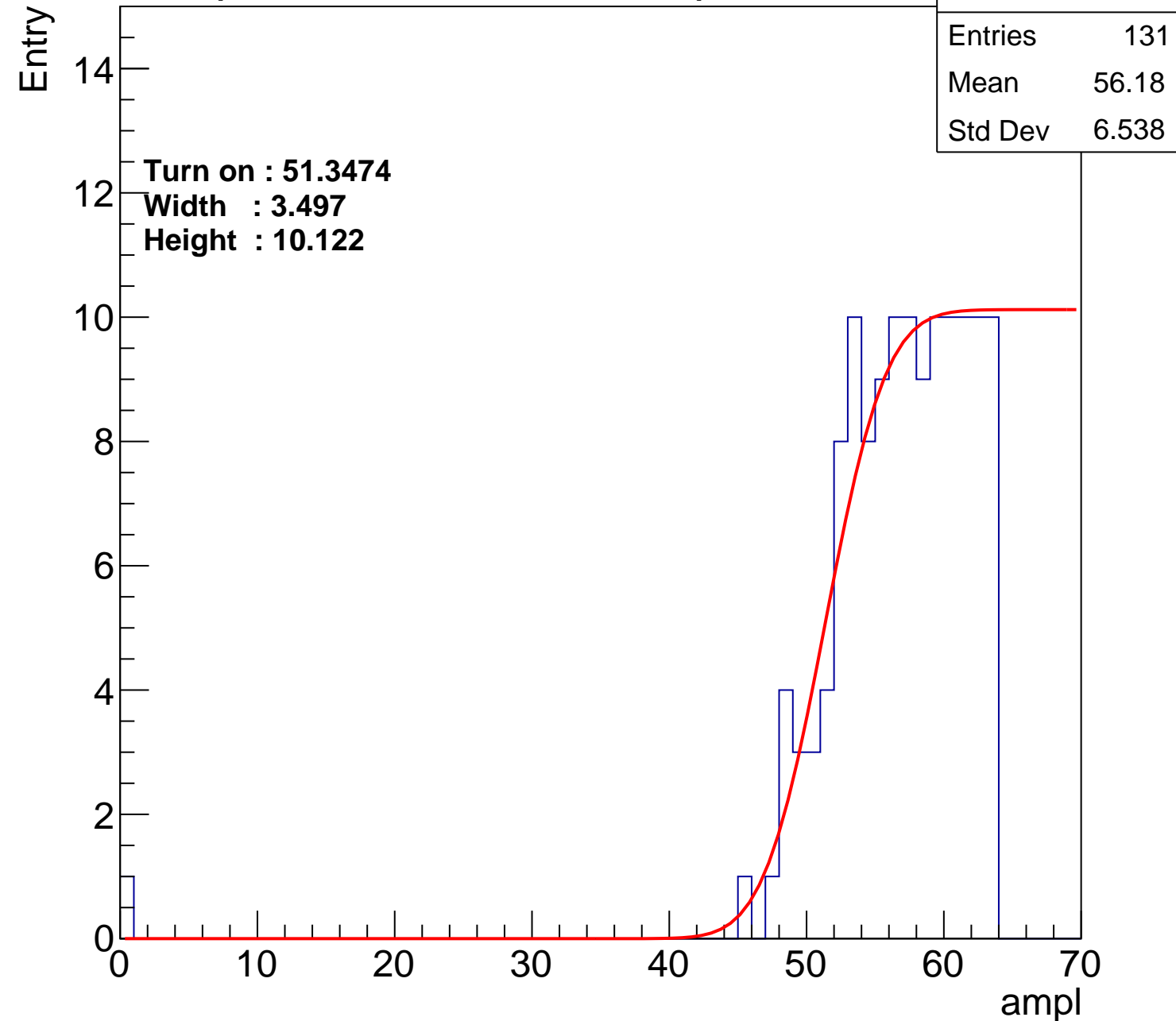
Width : 3.497

Height : 10.122

Entry

14
12
10
8
6
4
2
0

ampl



B0L103S, U12-ch127

calib_packv5_040323_1717.root, FC#2, port C3

Entries	106
Mean	56.25
Std Dev	10.29

Turn on : 54.5088

Width : 3.254

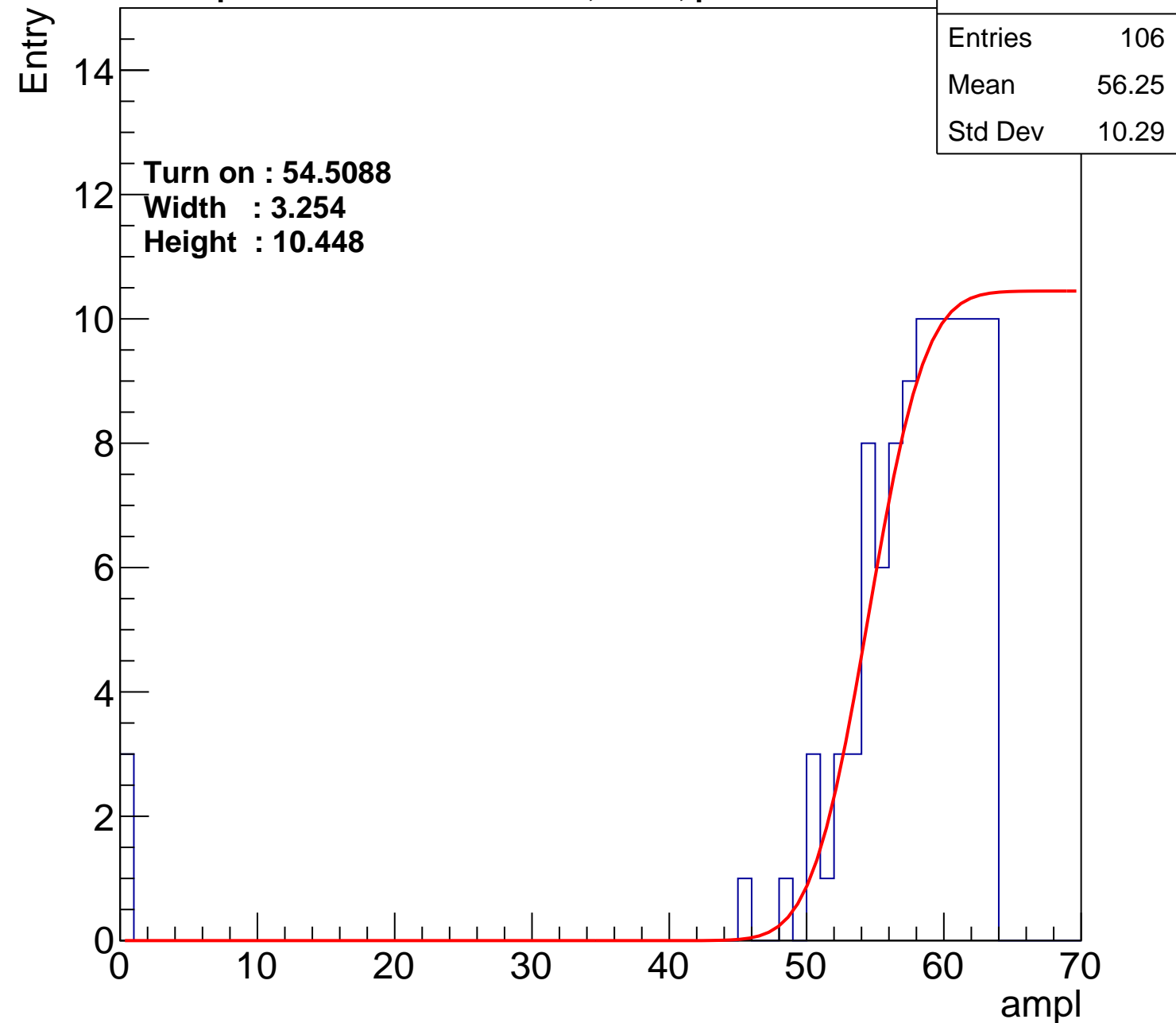
Height : 10.448

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B0L103S, U12-ch127

calib_packv5_040323_1717.root, FC#2, port C3

Entries	106
Mean	56.25
Std Dev	10.29

Turn on : 54.5088

Width : 3.254

Height : 10.448

Entry

