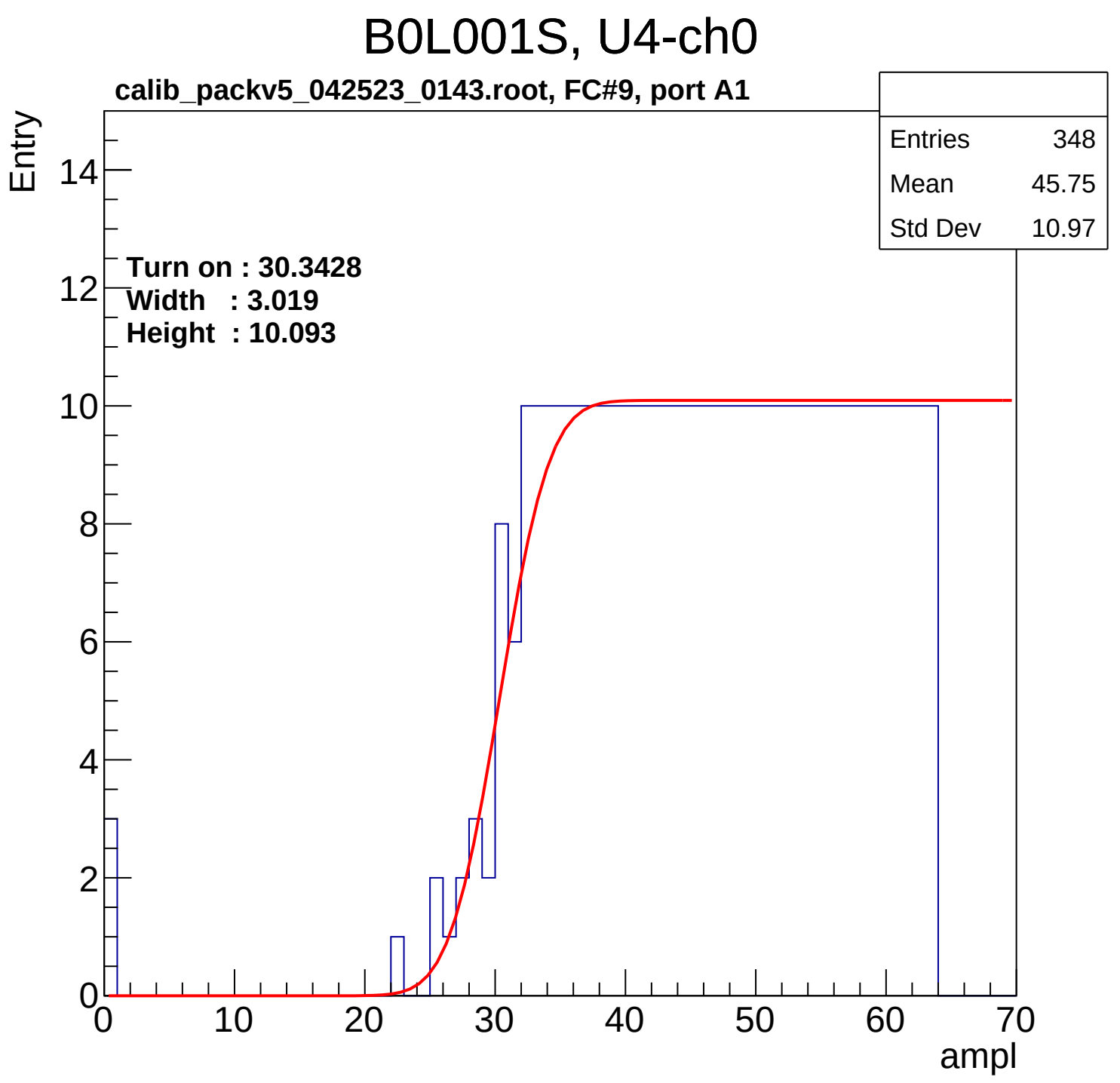
B0L001S, U4-ch0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 348
Mean 45.75
Std Dev 10.97
Turn on : 30.3428
Width : 3.019
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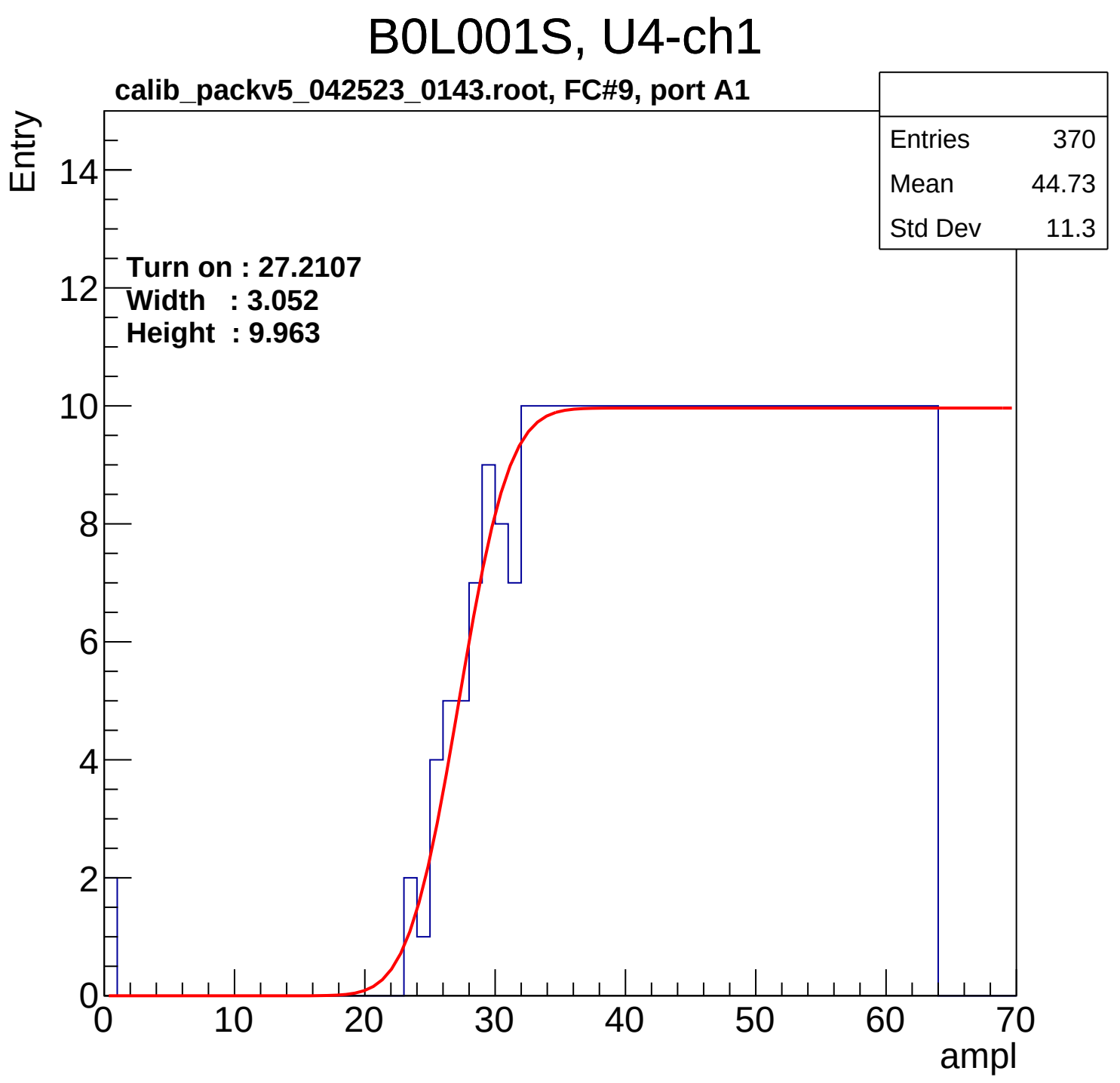
B0L001S, U4-ch1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 370
Mean 44.73
Std Dev 11.3
Turn on : 27.2107
Width : 3.052
Height : 9.963
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ampl
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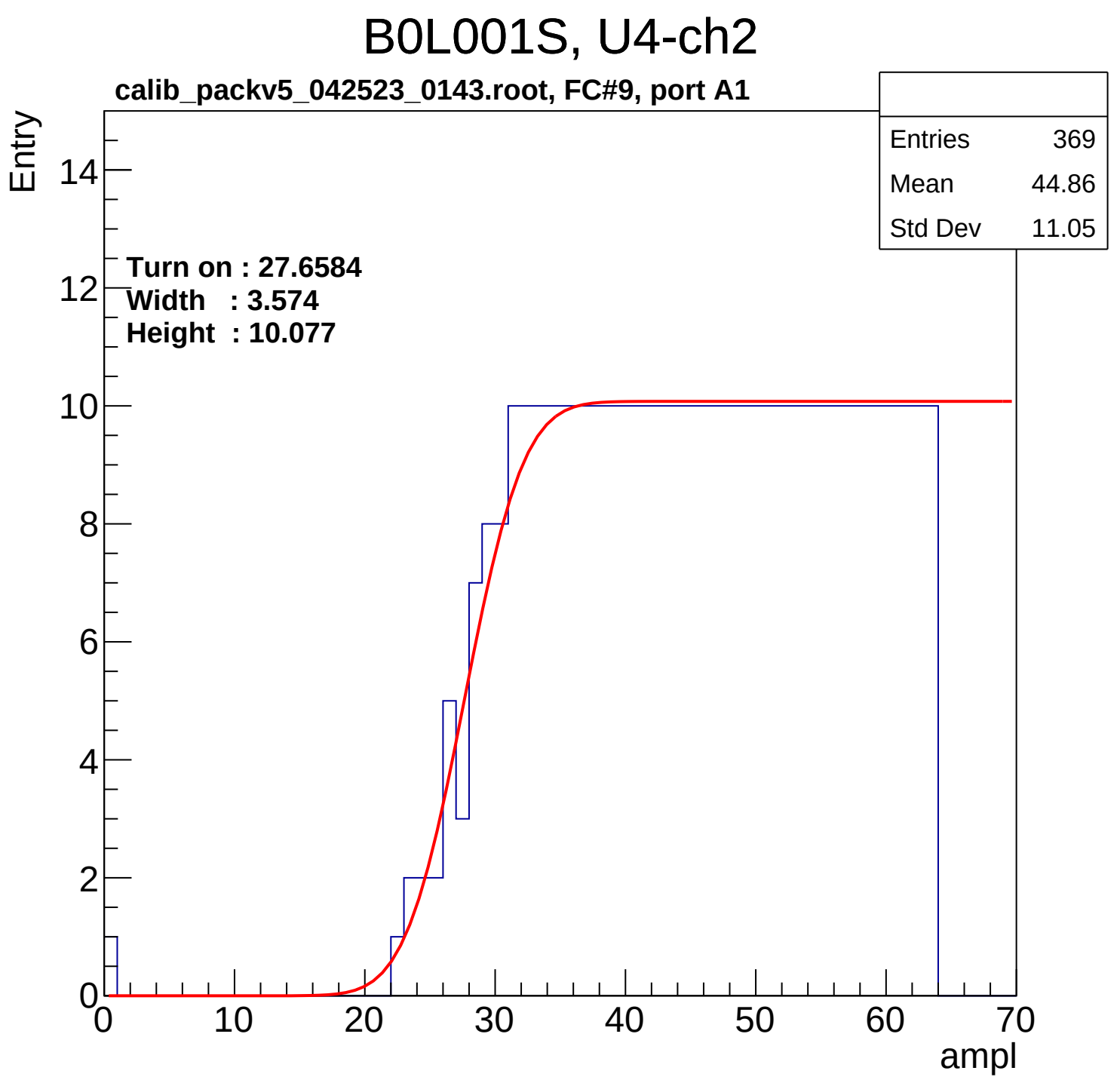
B0L001S, U4-ch2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.86
Std Dev 11.05
Turn on : 27.6584
Width : 3.574
Height : 10.077
Entry
ampl
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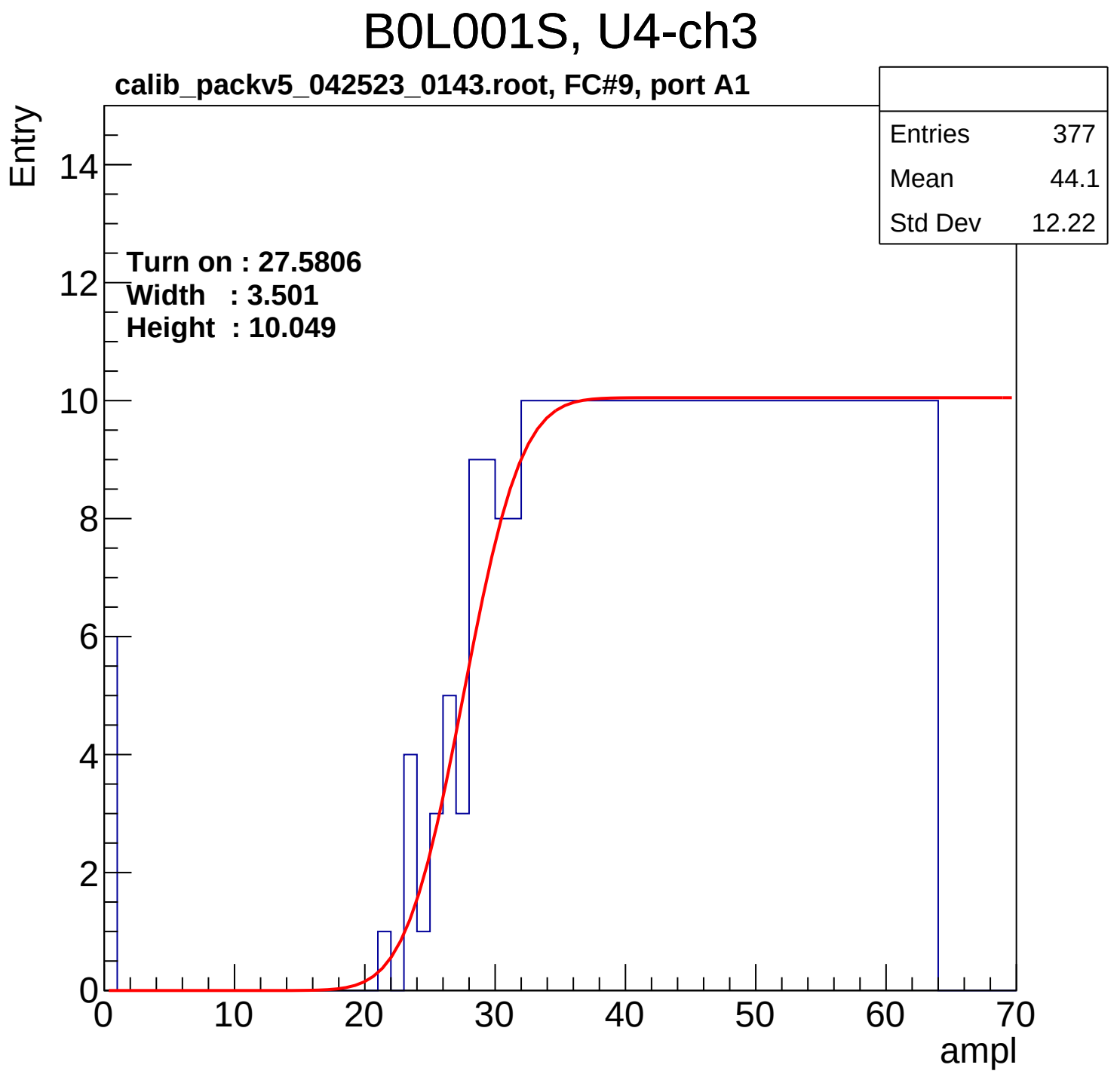
B0L001S, U4-ch3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 377
Mean 44.1
Std Dev 12.22
Turn on : 27.5806
Width : 3.501
Height : 10.049
Entry
ampl
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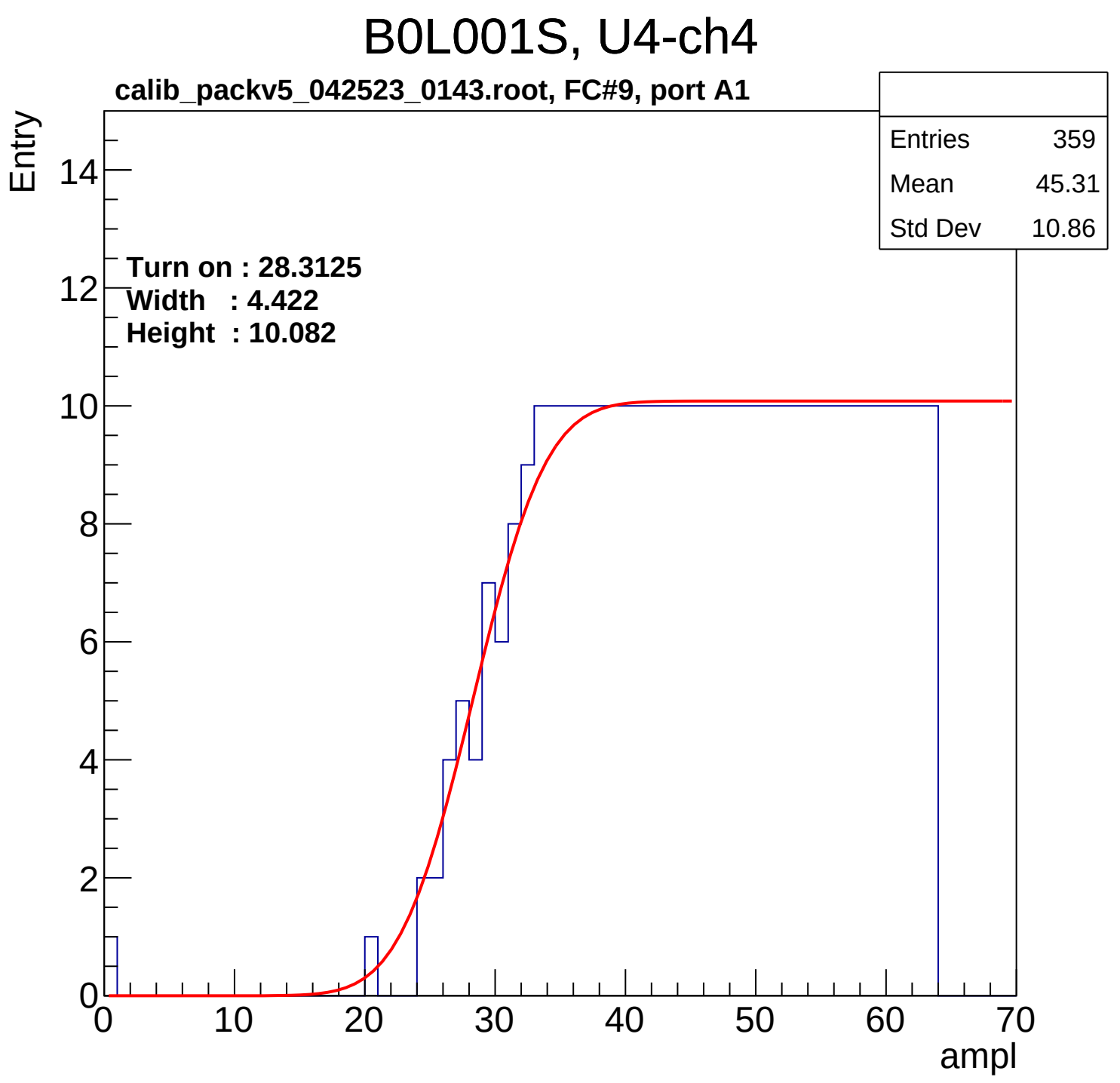
B0L001S, U4-ch4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 45.31
Std Dev 10.86
Turn on : 28.3125
Width : 4.422
Height : 10.082
Entry
ampl
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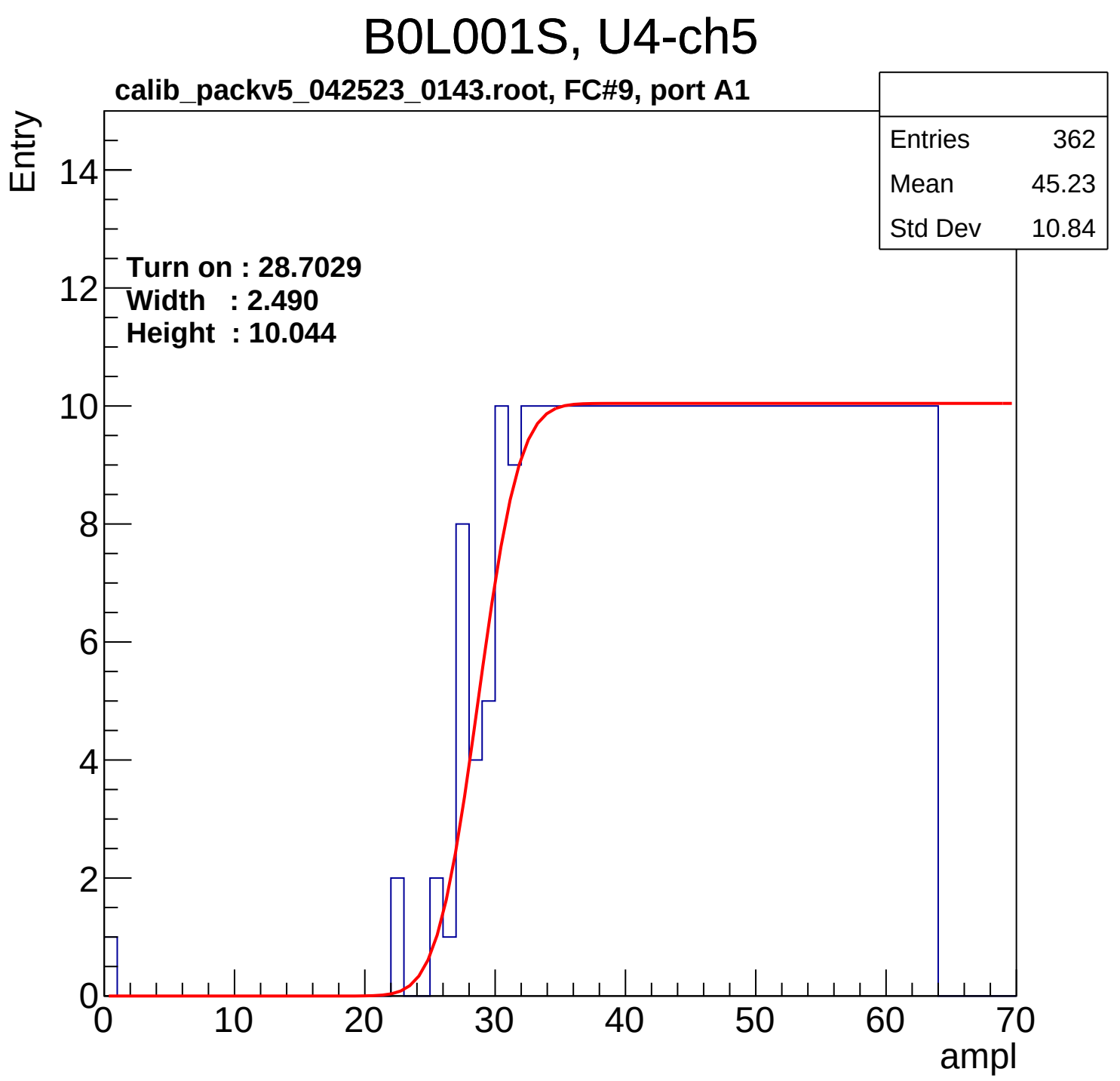
B0L001S, U4-ch5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 45.23
Std Dev 10.84
Turn on : 28.7029
Width : 2.490
Height : 10.044
Entry
ampl
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6
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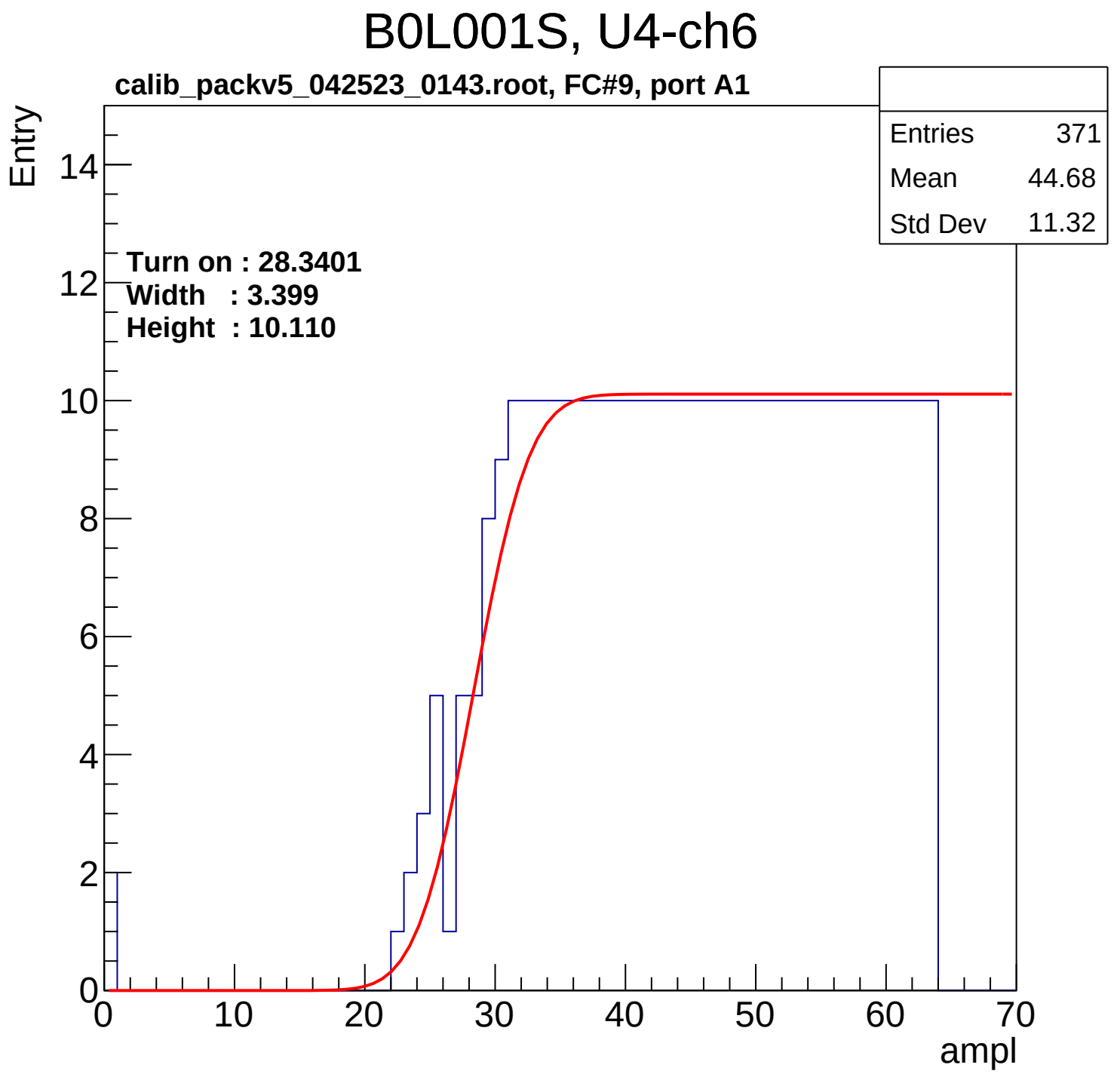
B0L001S, U4-ch6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 371
Mean 44.68
Std Dev 11.32
Turn on : 28.3401
Width : 3.399
Height : 10.110
Entry
ampl
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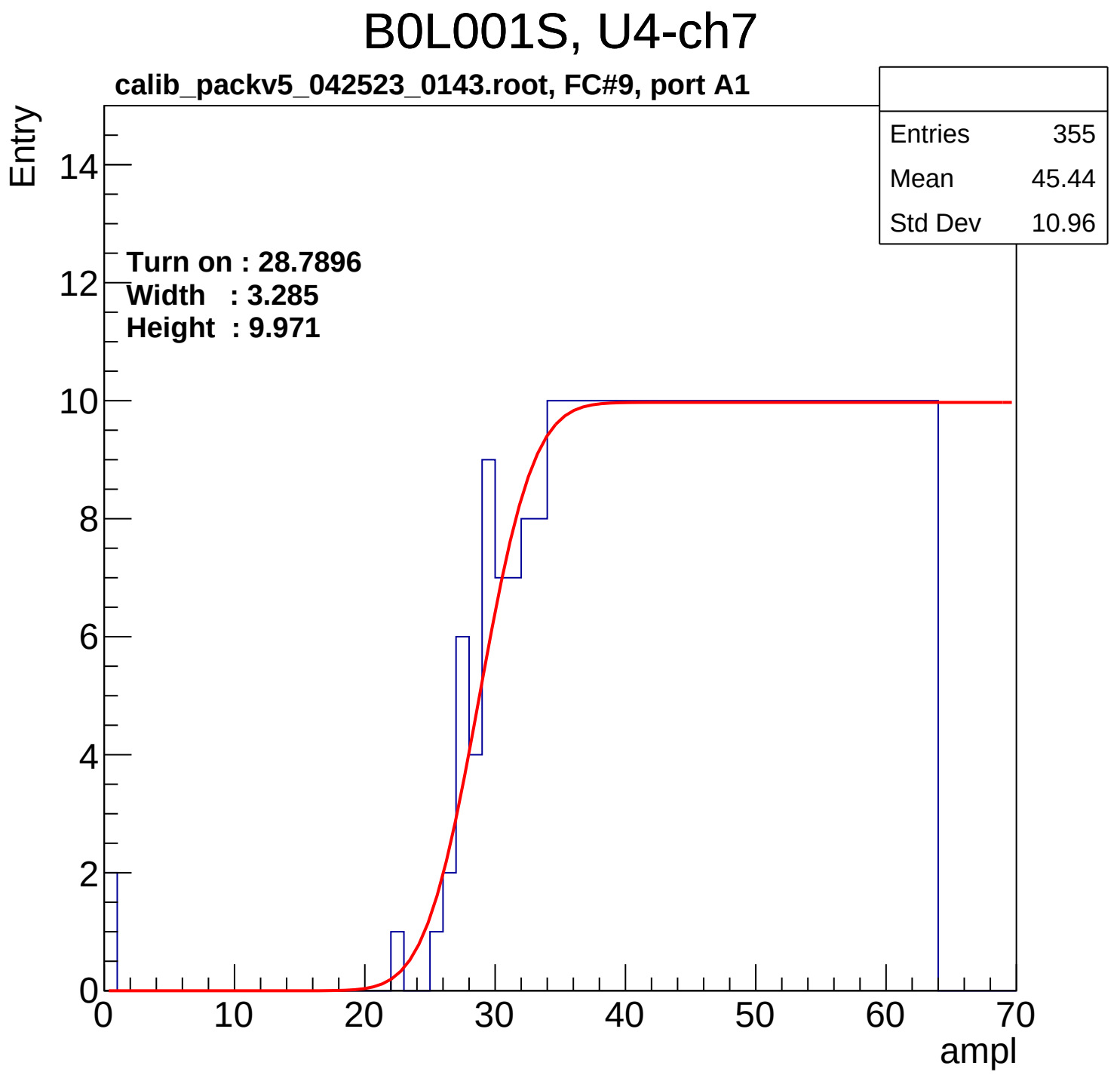
B0L001S, U4-ch7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 355
Mean 45.44
Std Dev 10.96
Turn on : 28.7896
Width : 3.285
Height : 9.971
Entry
ampl
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6
8
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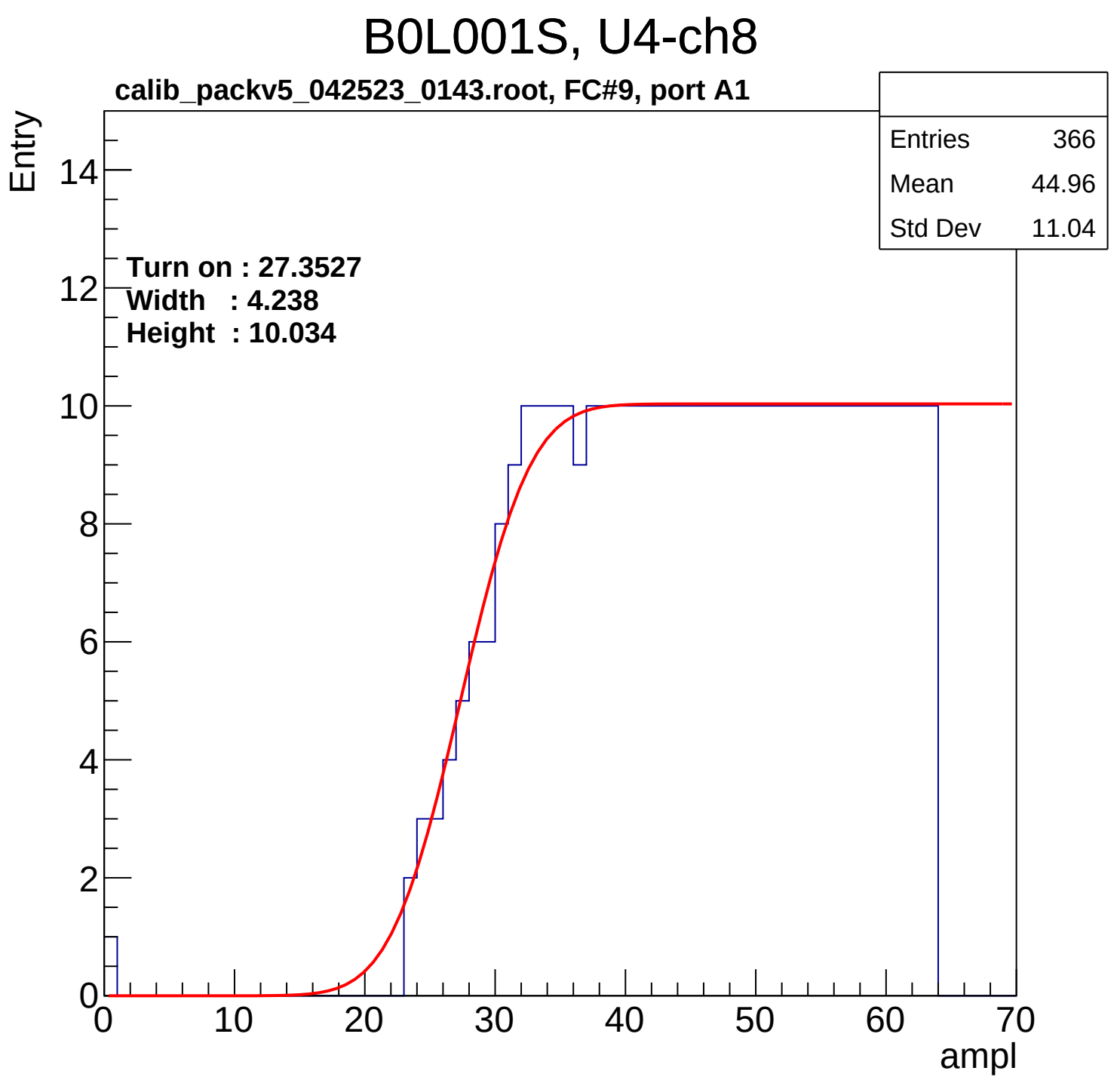
B0L001S, U4-ch8
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.96
Std Dev 11.04
Turn on : 27.3527
Width : 4.238
Height : 10.034
Entry
ampl
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8
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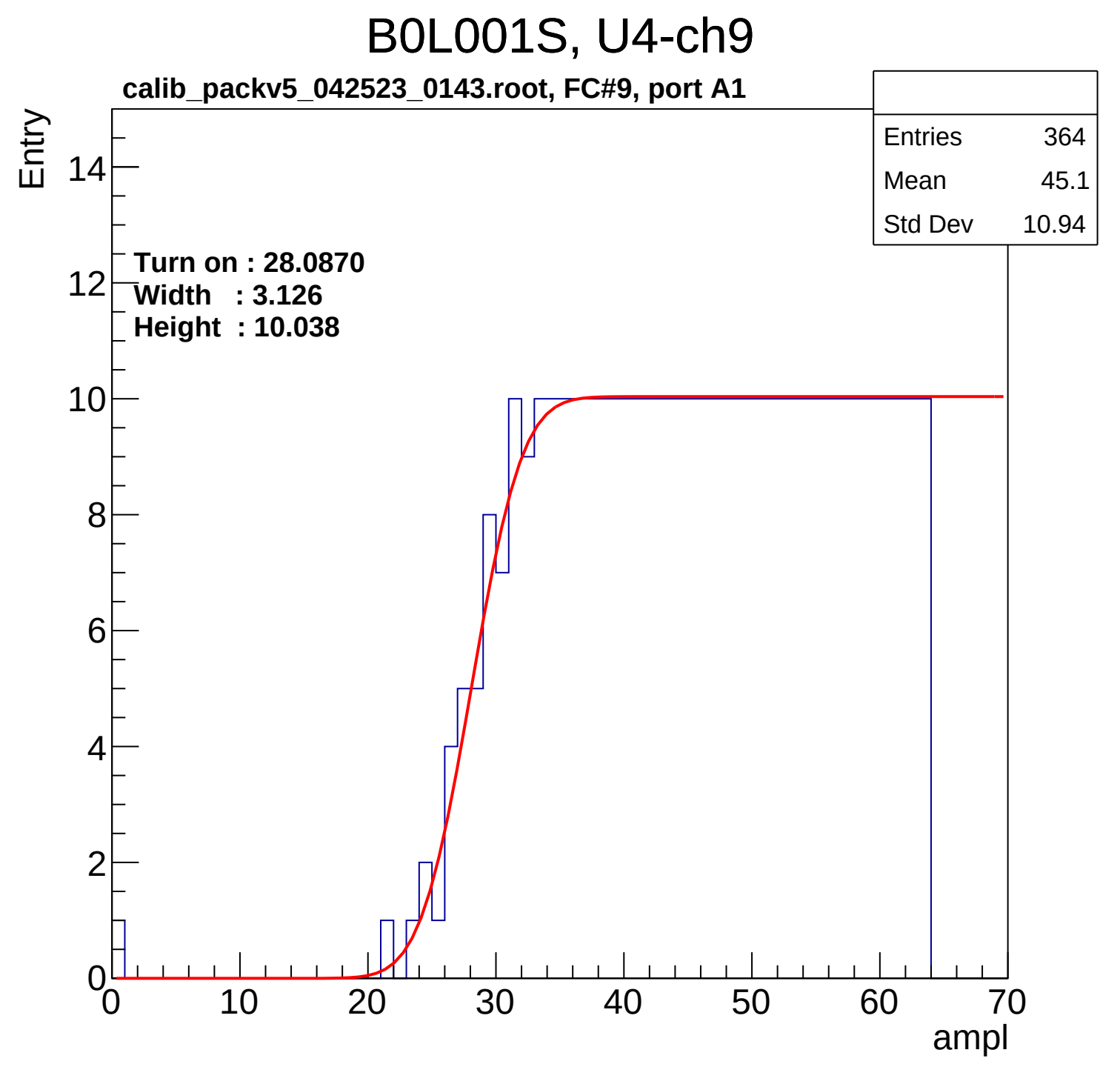
B0L001S, U4-ch9
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 45.1
Std Dev 10.94
Turn on : 28.0870
Width : 3.126
Height : 10.038
Entry
ampl
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6
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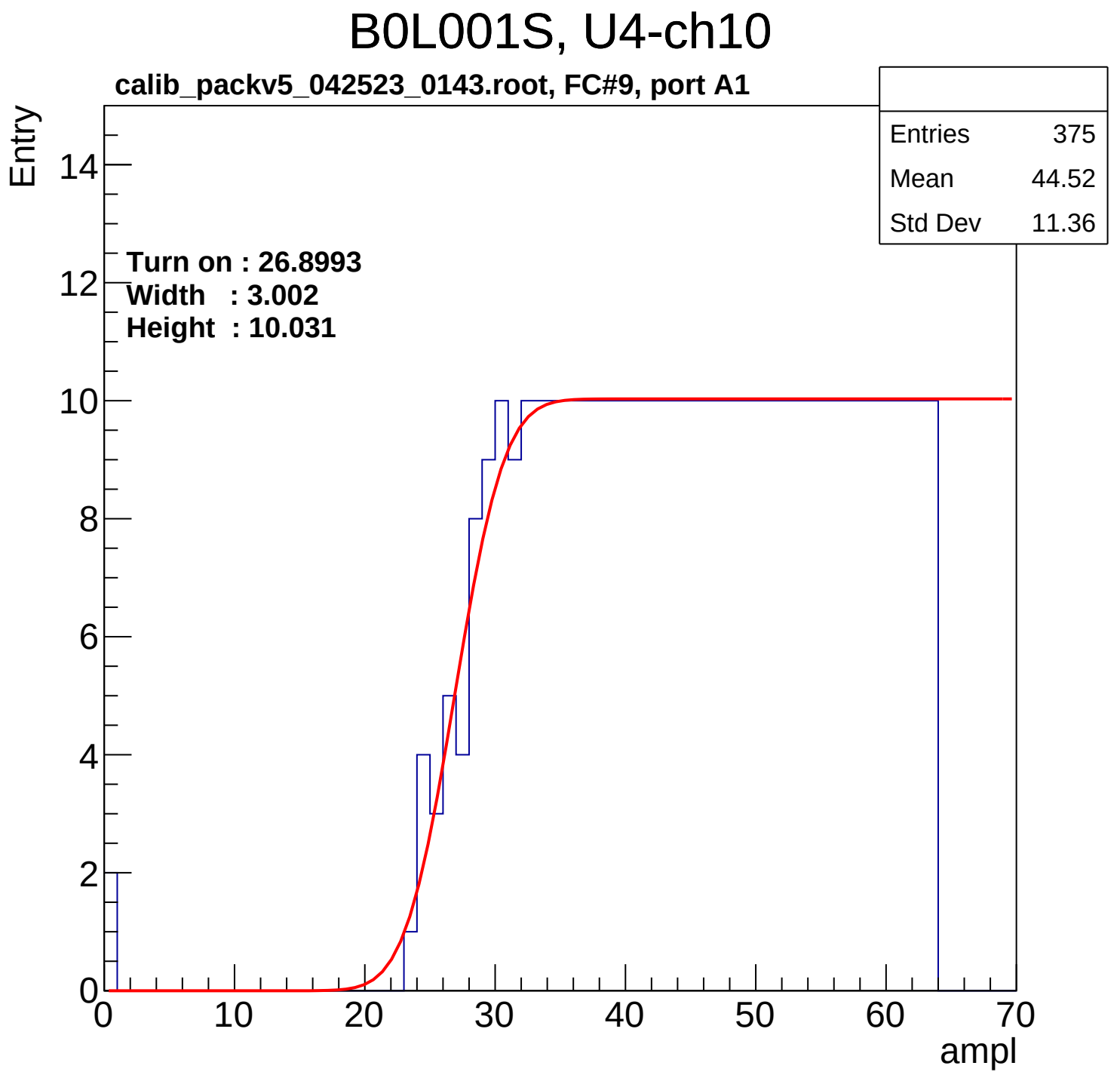
B0L001S, U4-ch10
calib_packv5_042523_0143.root, FC#9, port A1
Entries 375
Mean 44.52
Std Dev 11.36
Turn on : 26.8993
Width : 3.002
Height : 10.031
Entry
ampl
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6
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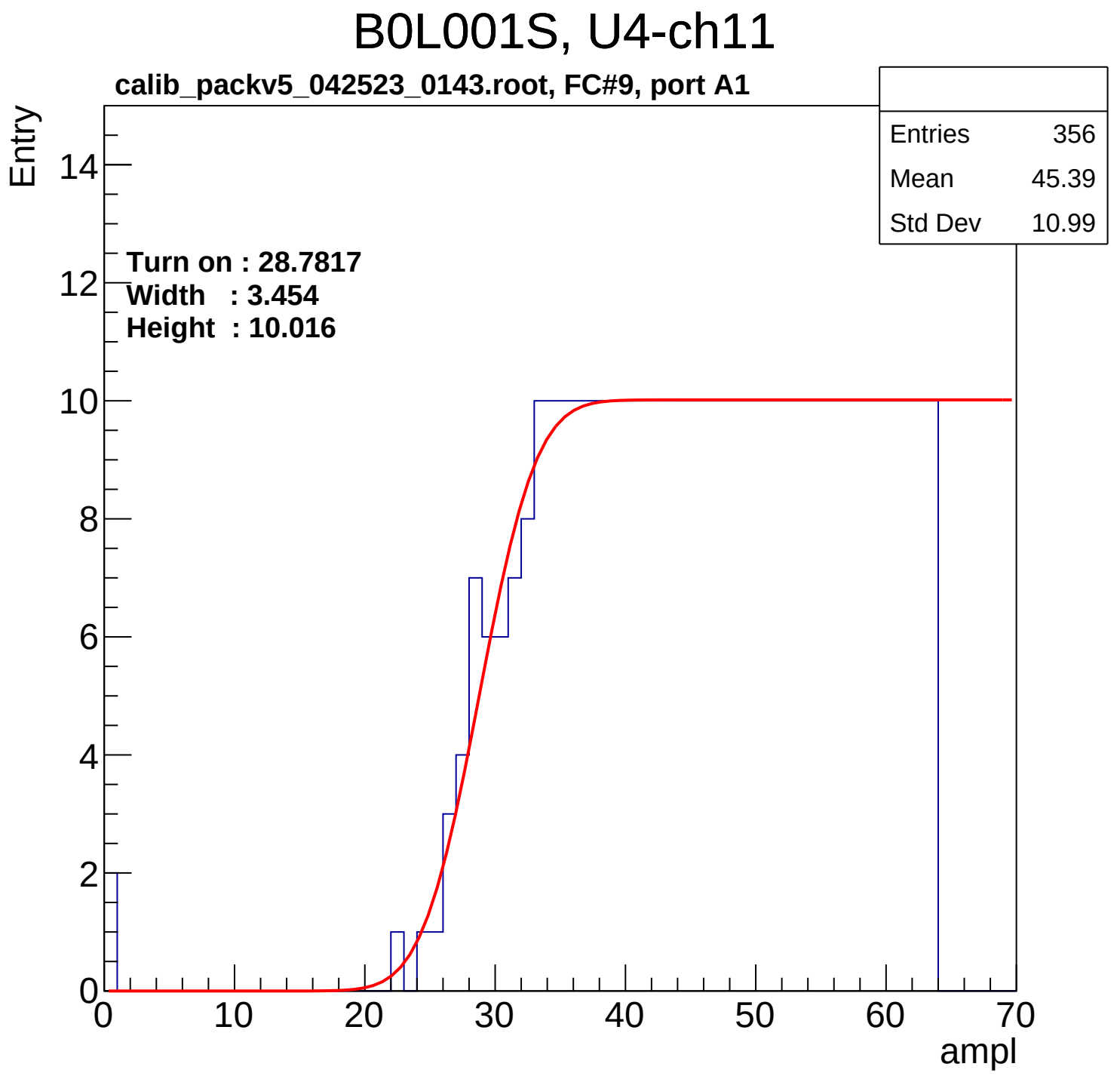
B0L001S, U4-ch11
calib_packv5_042523_0143.root, FC#9, port A1
Entries 356
Mean 45.39
Std Dev 10.99
Turn on : 28.7817
Width : 3.454
Height : 10.016
Entry
ampl
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6
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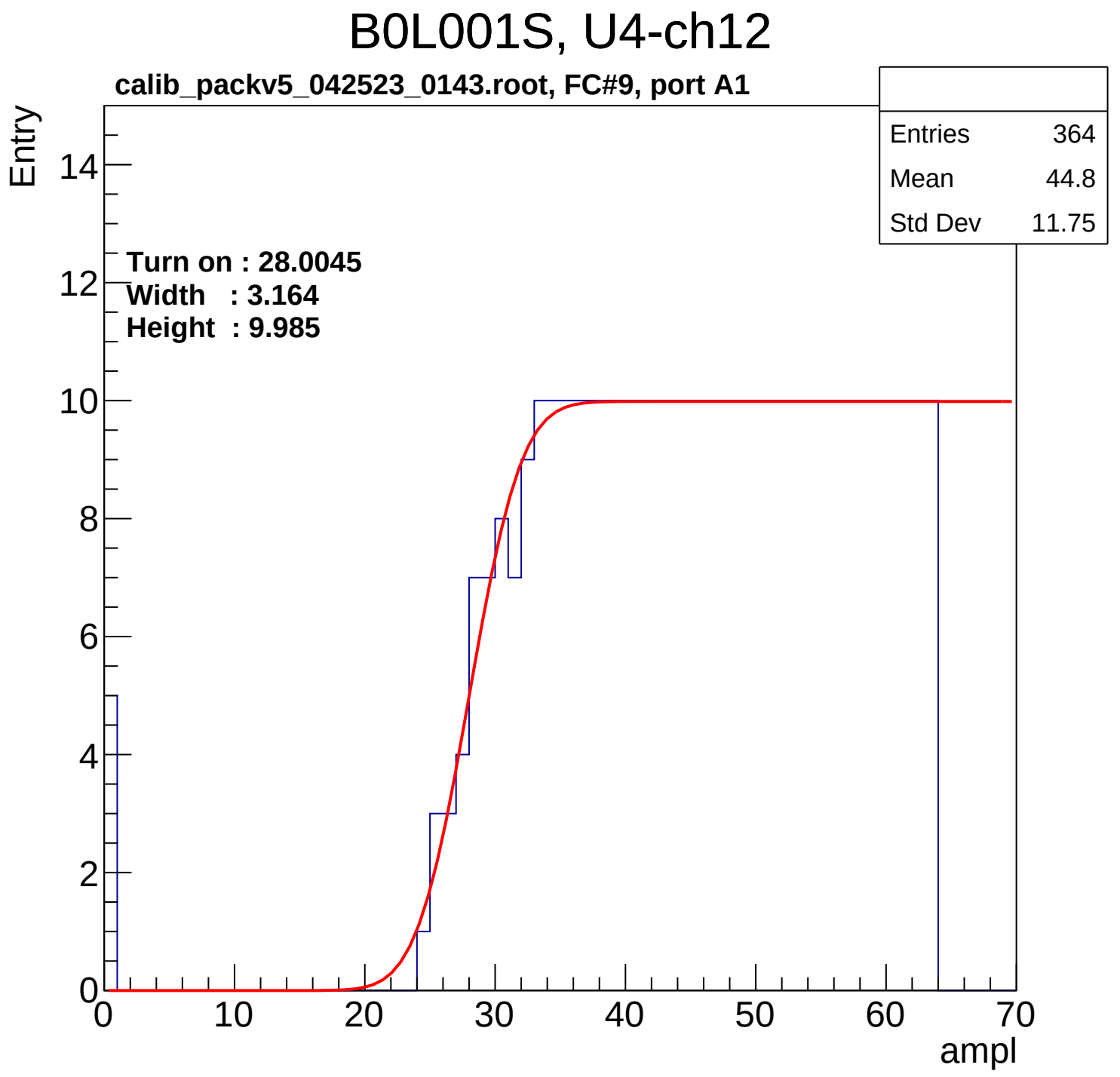
B0L001S, U4-ch12
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 44.8
Std Dev 11.75
Turn on : 28.0045
Width : 3.164
Height : 9.985
Entry
ampl
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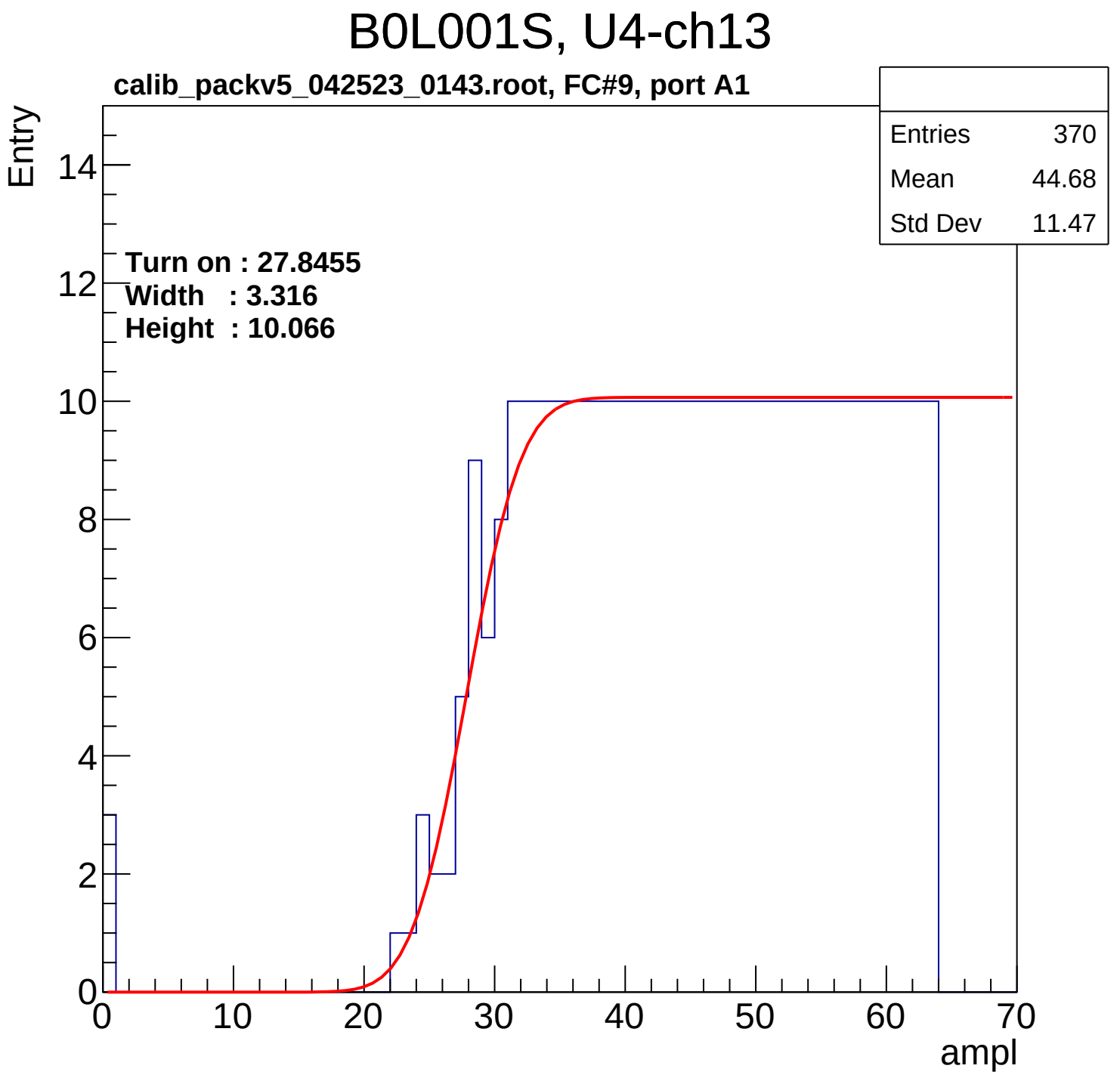
B0L001S, U4-ch13
calib_packv5_042523_0143.root, FC#9, port A1
Entries 370
Mean 44.68
Std Dev 11.47
Turn on : 27.8455
Width : 3.316
Height : 10.066
Entry
ampl
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6
8
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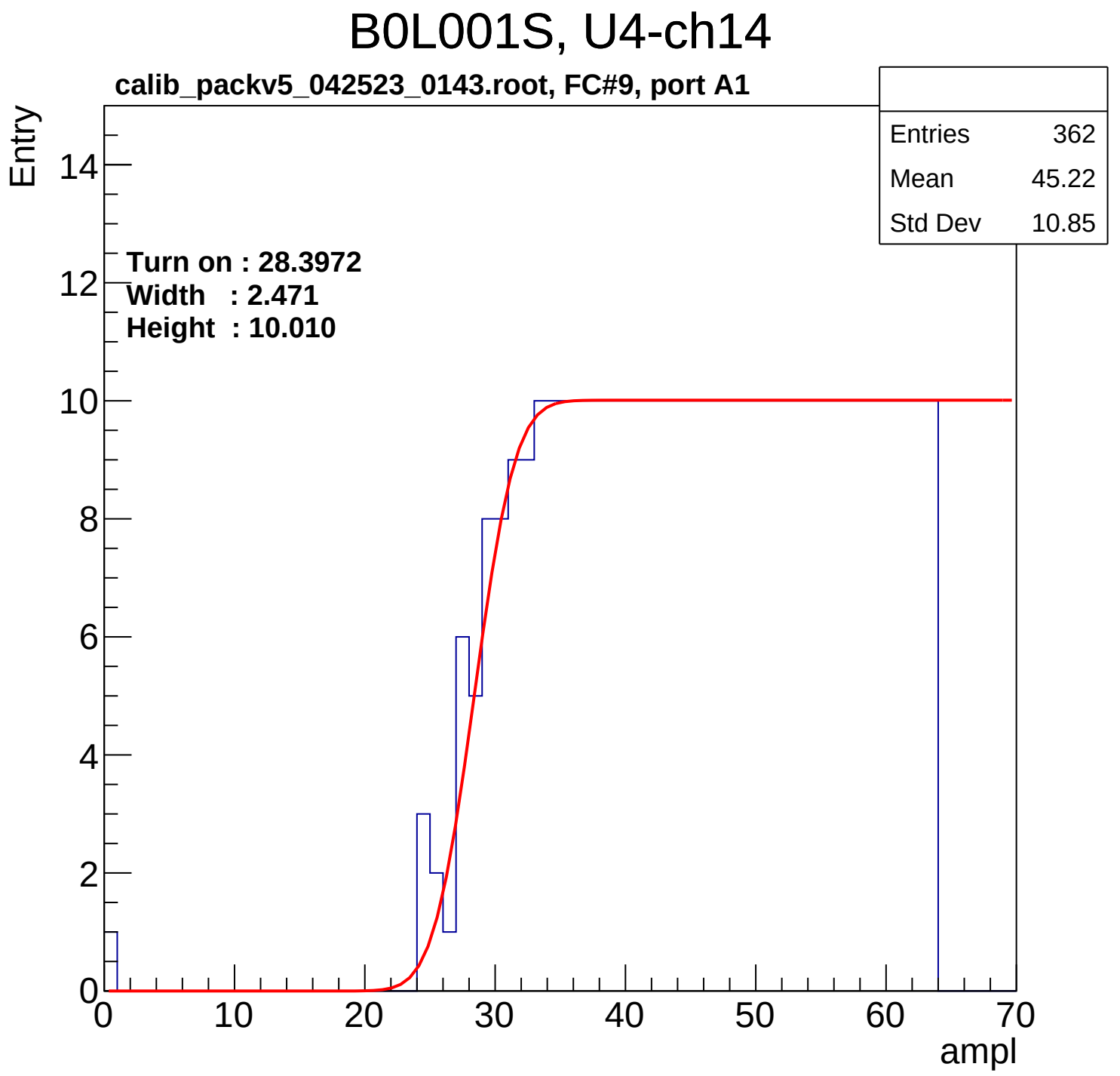
B0L001S, U4-ch14
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 45.22
Std Dev 10.85
Turn on : 28.3972
Width : 2.471
Height : 10.010
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ampl
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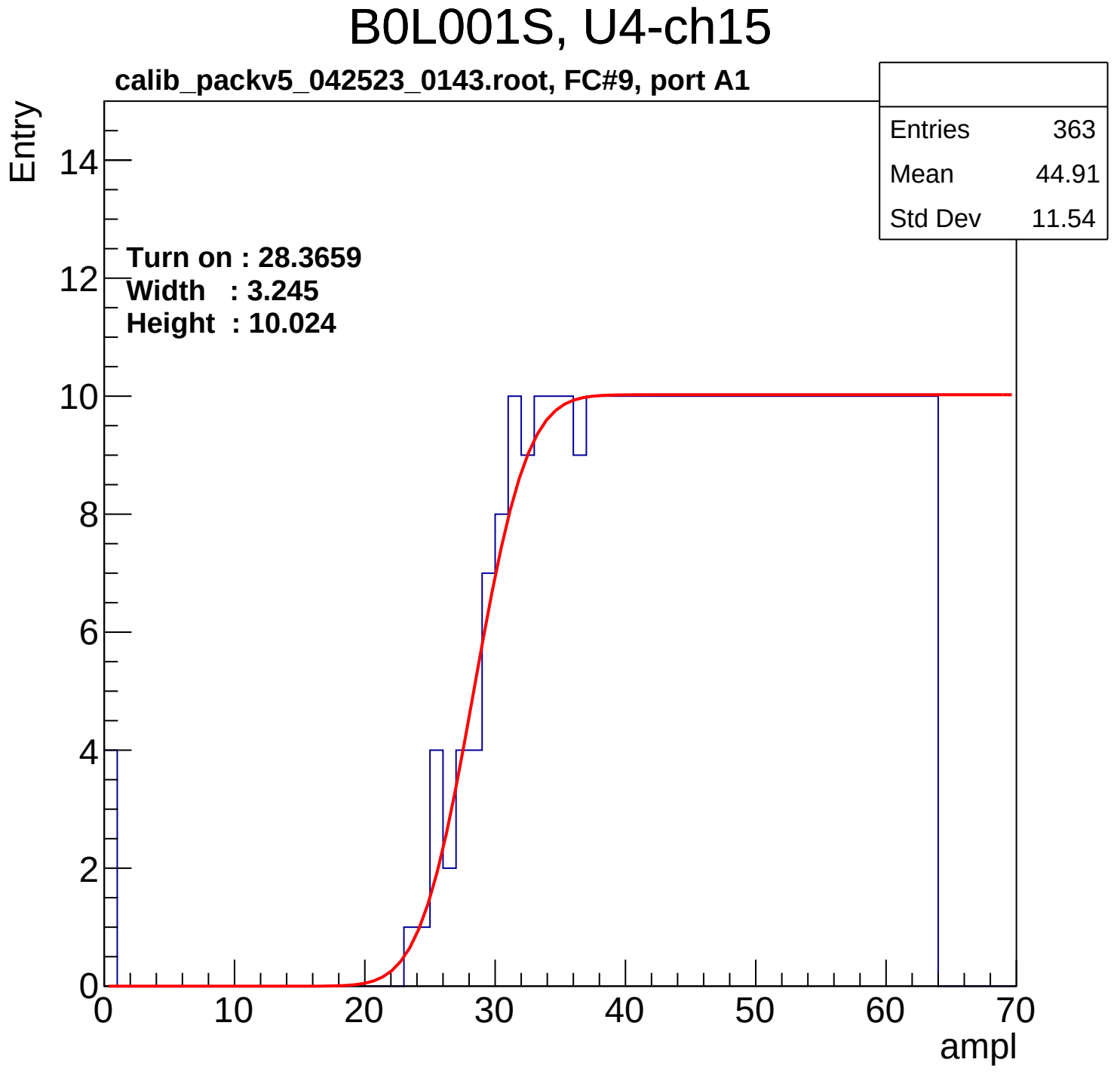
B0L001S, U4-ch15
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 44.91
Std Dev 11.54
Turn on : 28.3659
Width : 3.245
Height : 10.024
Entry
ampl
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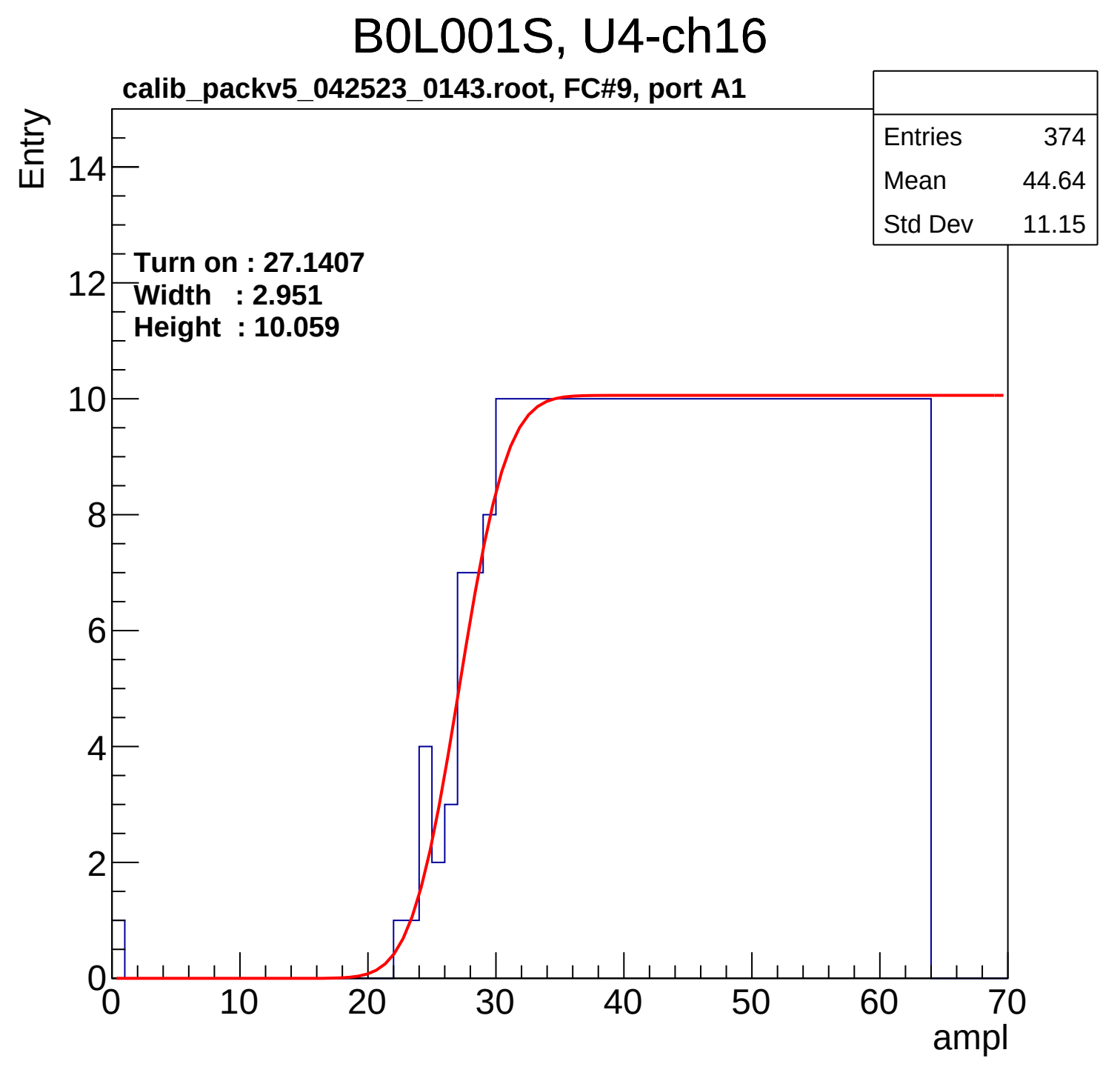
B0L001S, U4-ch16
calib_packv5_042523_0143.root, FC#9, port A1
Entries 374
Mean 44.64
Std Dev 11.15
Turn on : 27.1407
Width : 2.951
Height : 10.059
Entry
ampl
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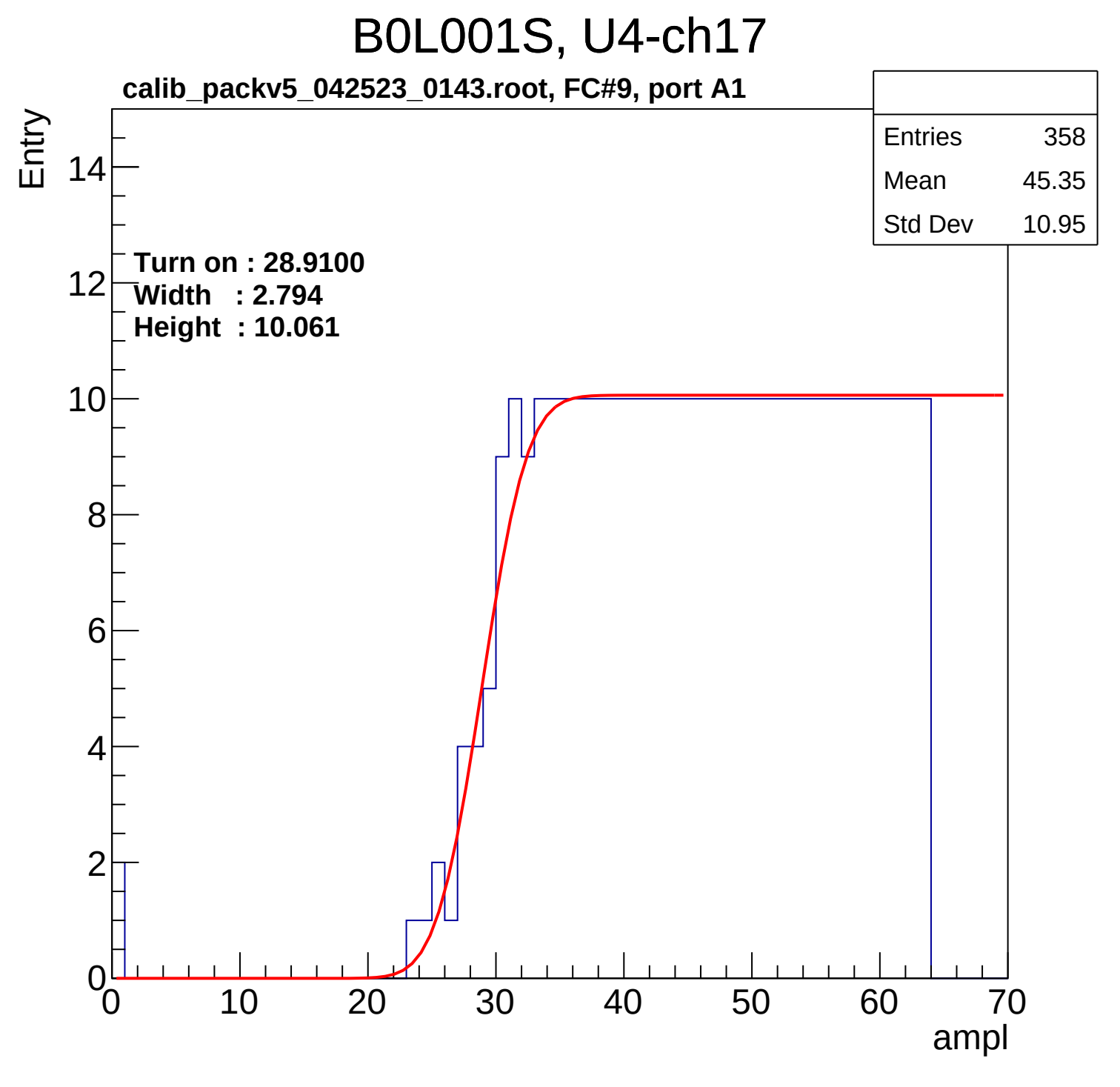
B0L001S, U4-ch17
calib_packv5_042523_0143.root, FC#9, port A1
Entries 358
Mean 45.35
Std Dev 10.95
Turn on : 28.9100
Width : 2.794
Height : 10.061
Entry
ampl
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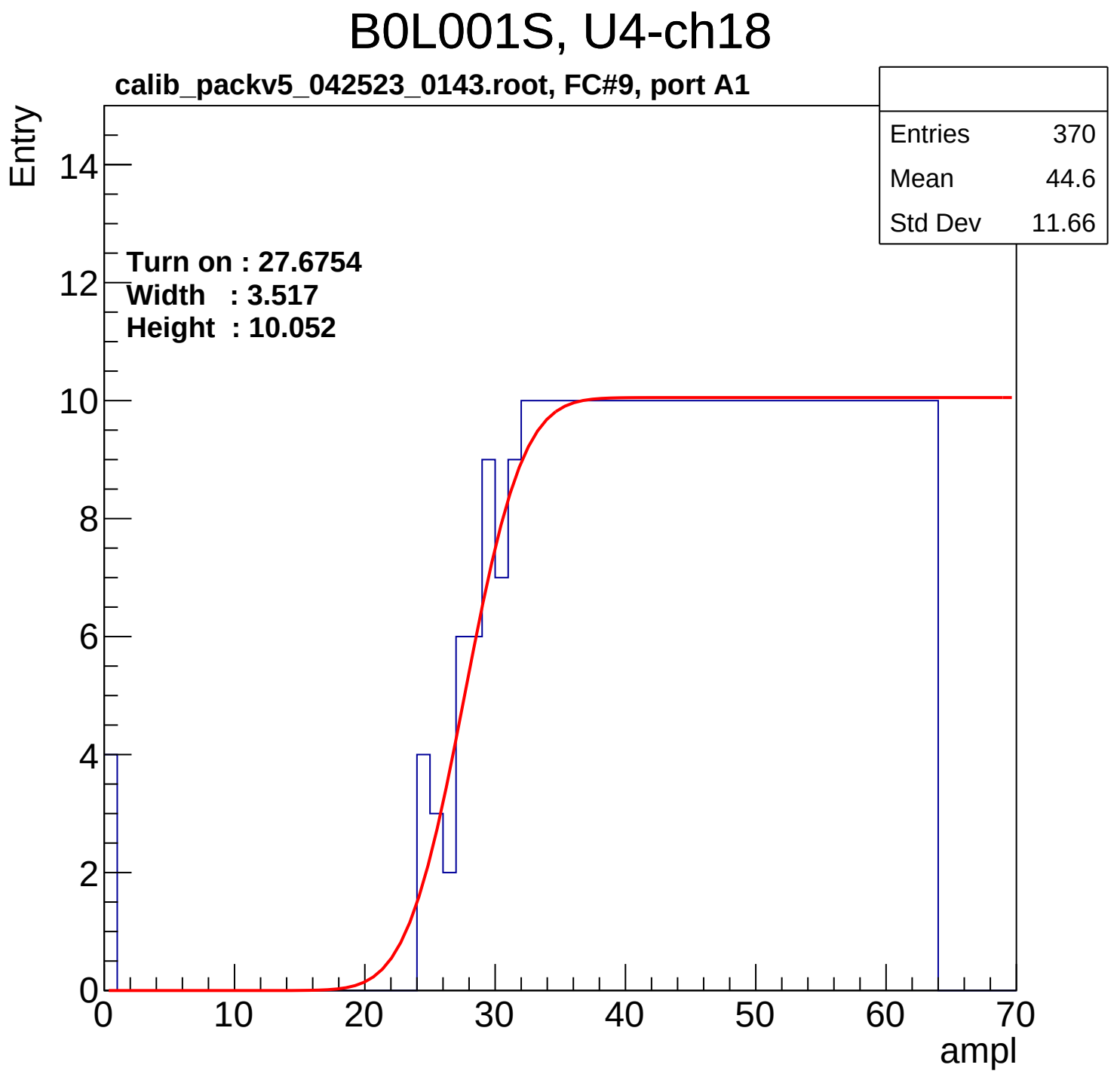
B0L001S, U4-ch18
calib_packv5_042523_0143.root, FC#9, port A1
Entries 370
Mean 44.6
Std Dev 11.66
Turn on : 27.6754
Width : 3.517
Height : 10.052
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ampl
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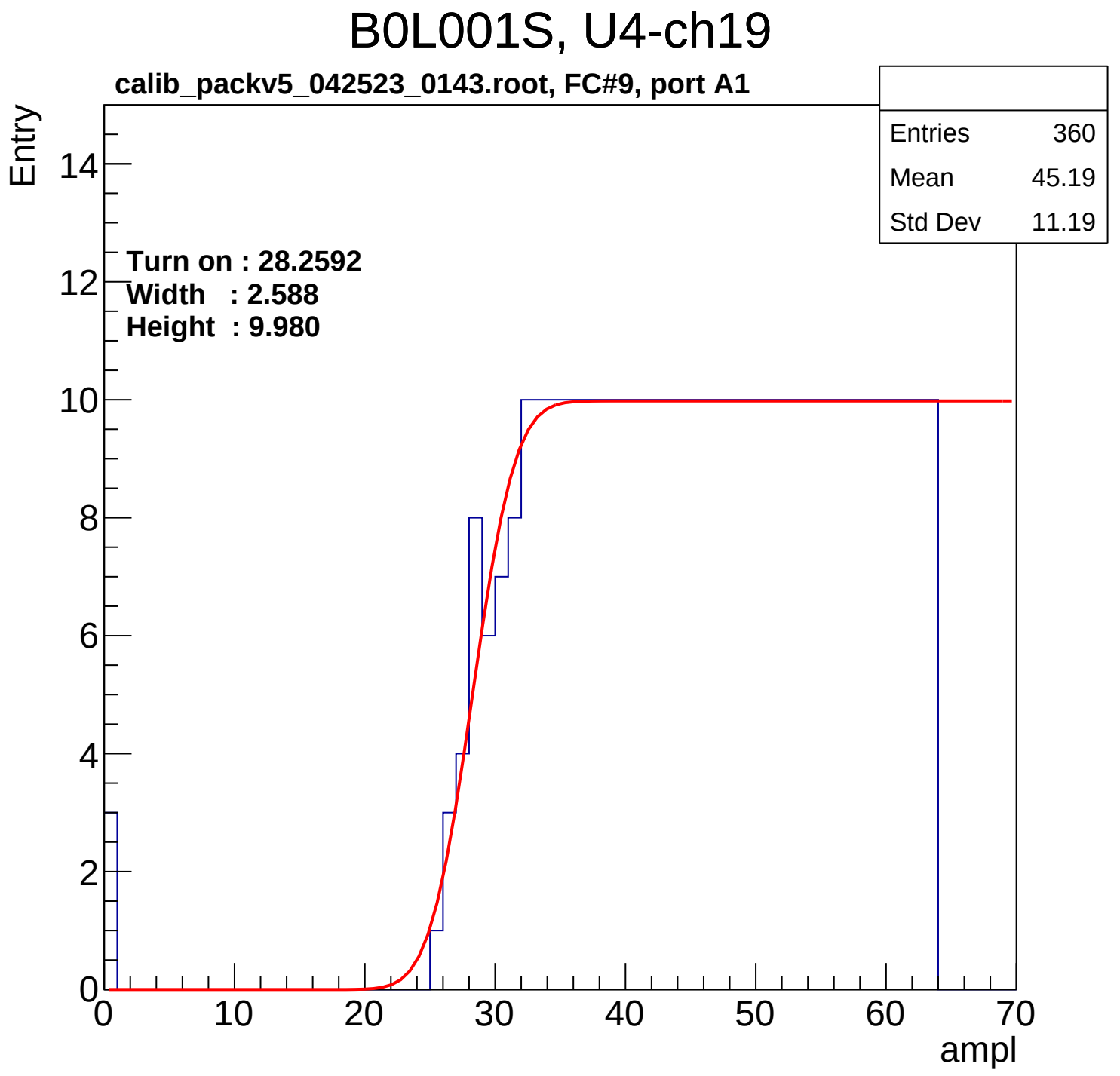
B0L001S, U4-ch19
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 45.19
Std Dev 11.19
Turn on : 28.2592
Width : 2.588
Height : 9.980
Entry
ampl
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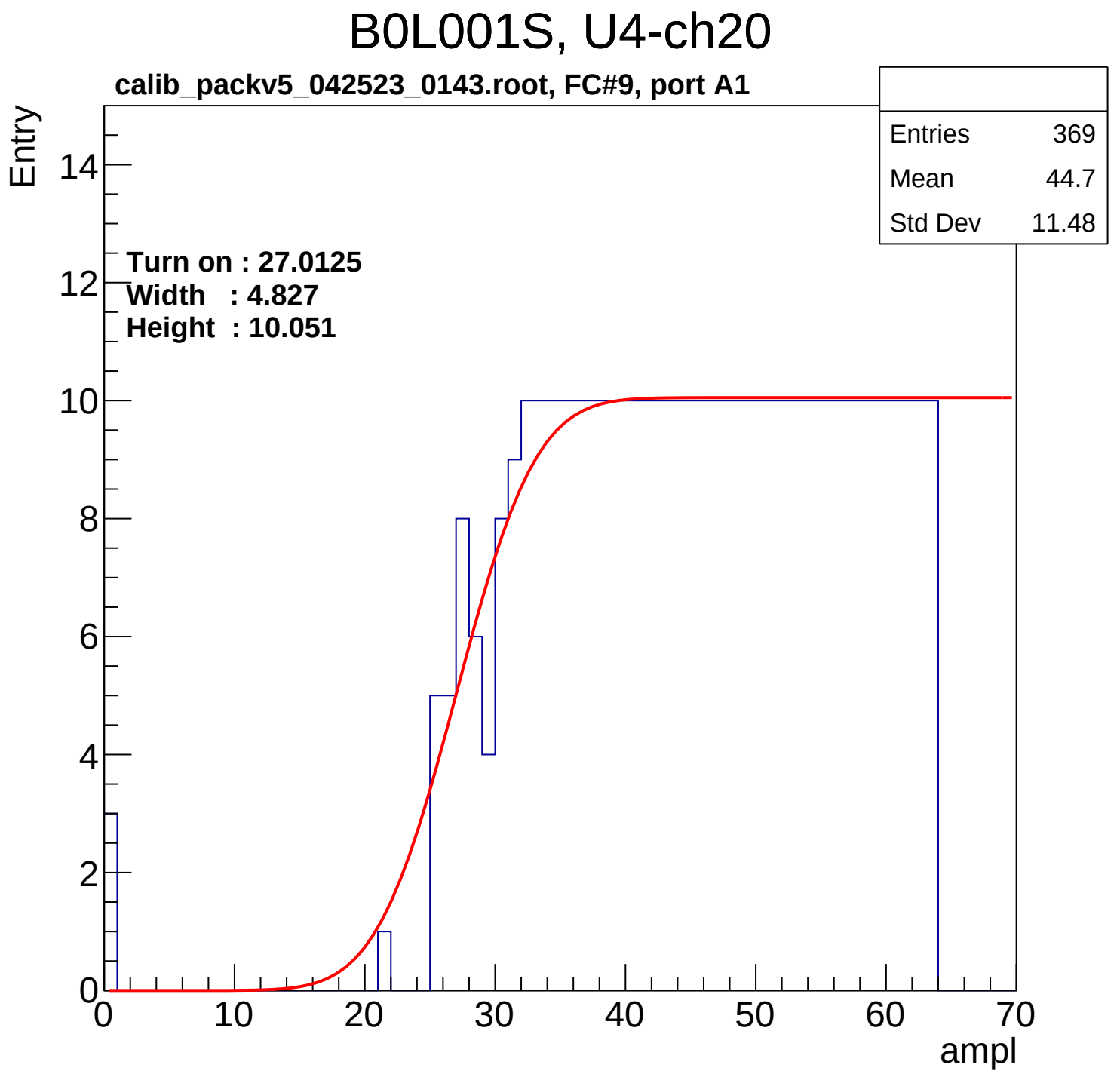
B0L001S, U4-ch20
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.7
Std Dev 11.48
Turn on : 27.0125
Width : 4.827
Height : 10.051
Entry
ampl
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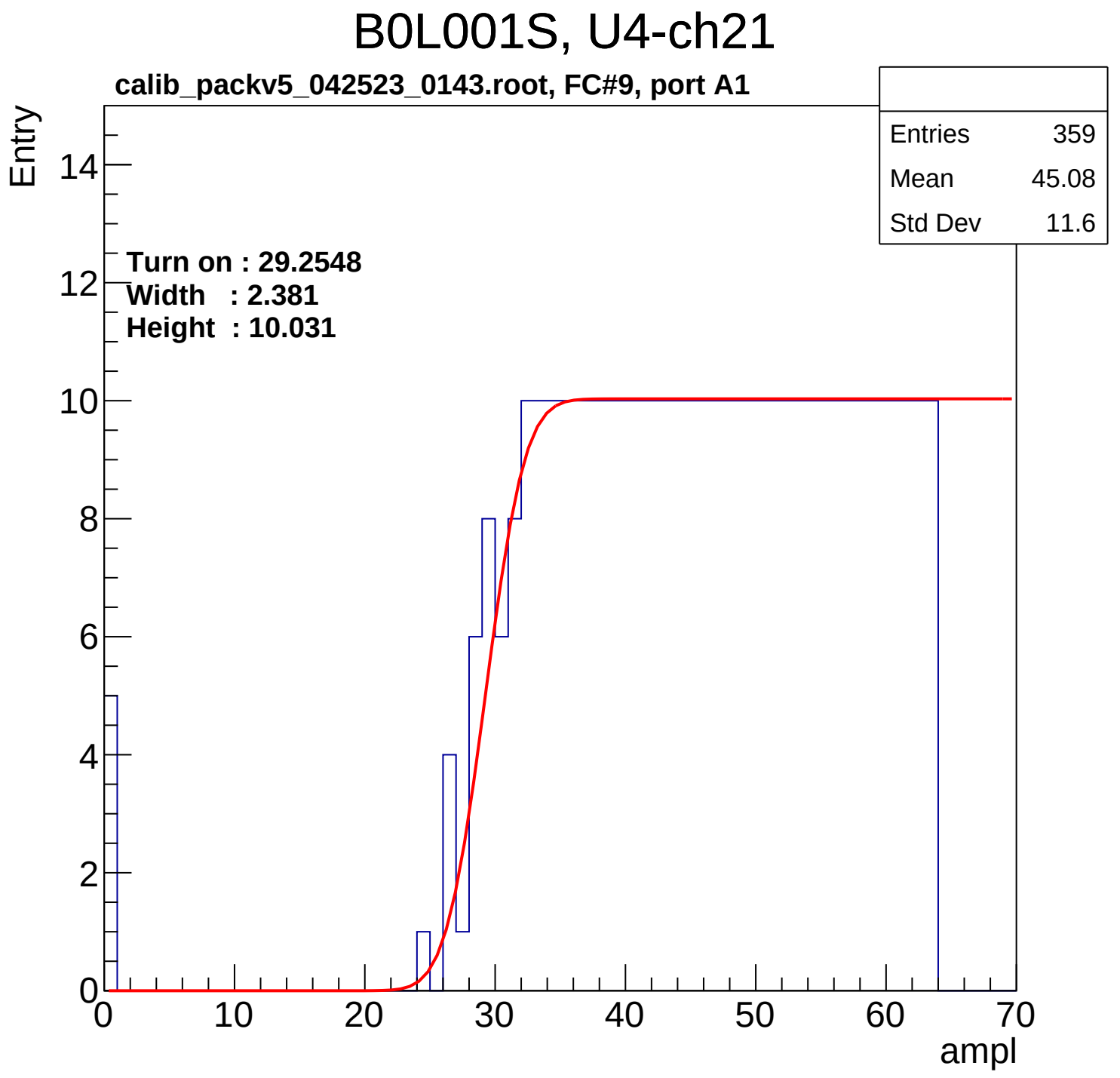
B0L001S, U4-ch21
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 45.08
Std Dev 11.6
Turn on : 29.2548
Width : 2.381
Height : 10.031
Entry
ampl
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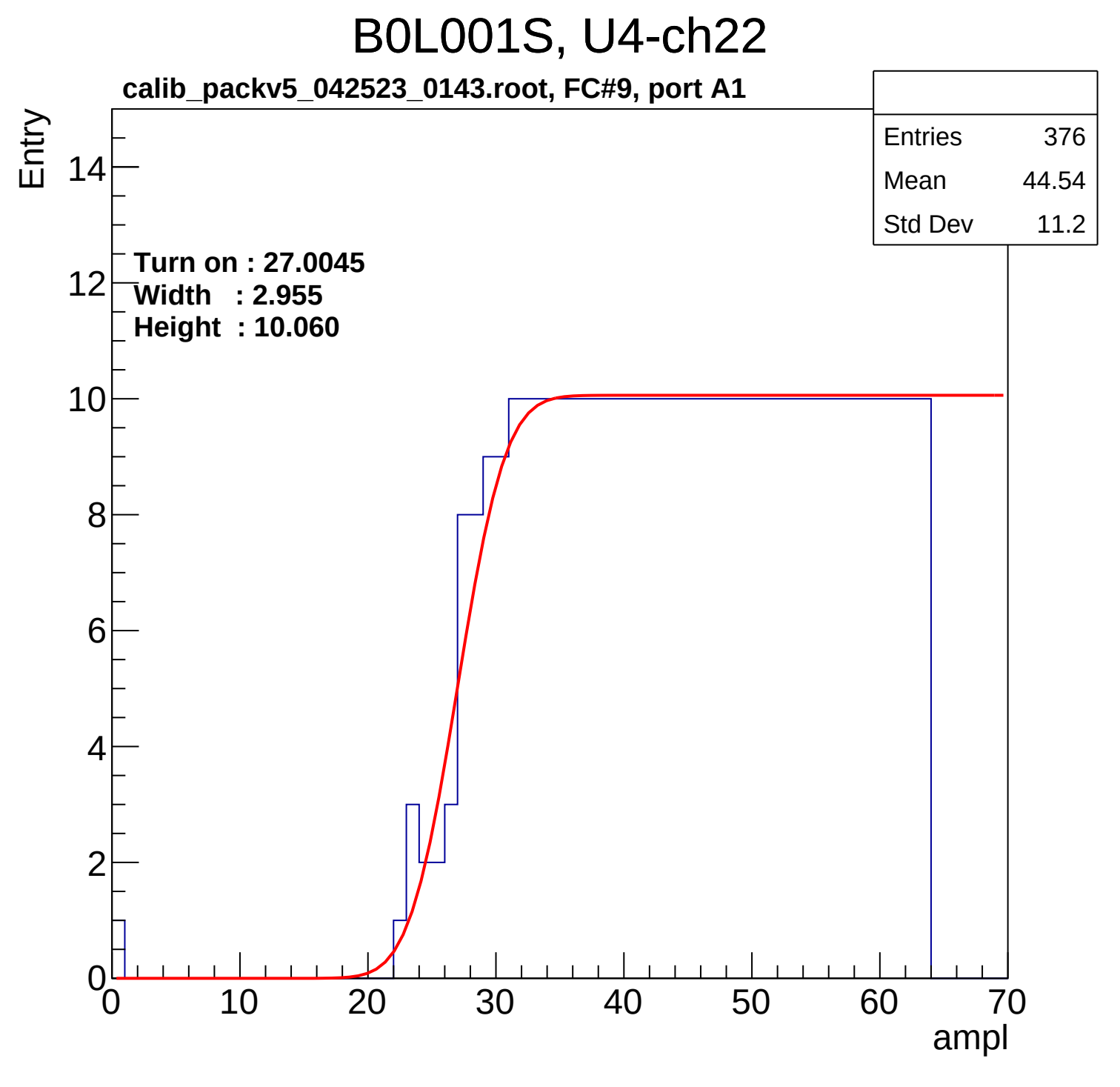
B0L001S, U4-ch22
calib_packv5_042523_0143.root, FC#9, port A1
Entries 376
Mean 44.54
Std Dev 11.2
Turn on : 27.0045
Width : 2.955
Height : 10.060
Entry
ampl
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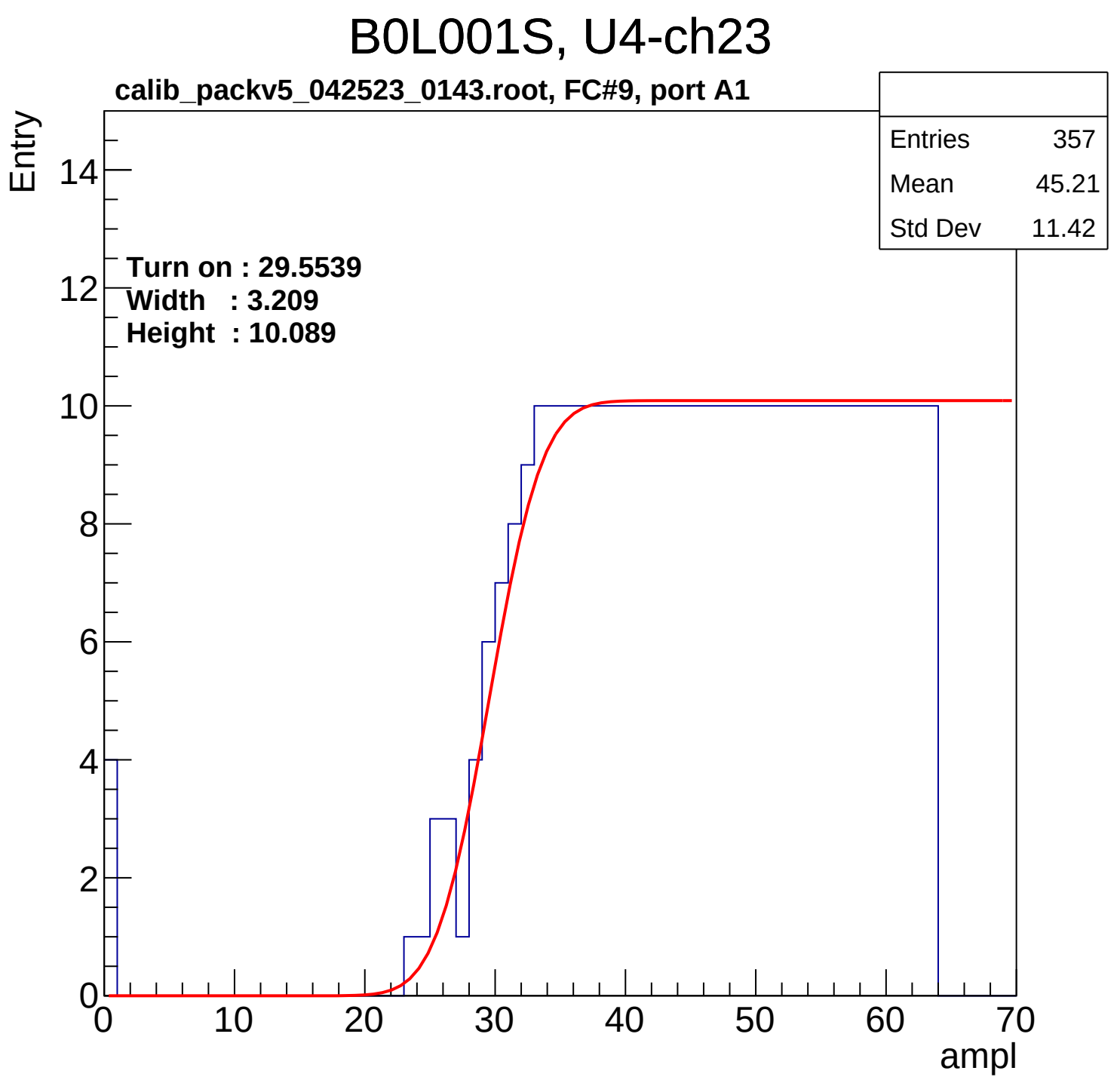
B0L001S, U4-ch23
calib_packv5_042523_0143.root, FC#9, port A1
Entries 357
Mean 45.21
Std Dev 11.42
Turn on : 29.5539
Width : 3.209
Height : 10.089
Entry
ampl
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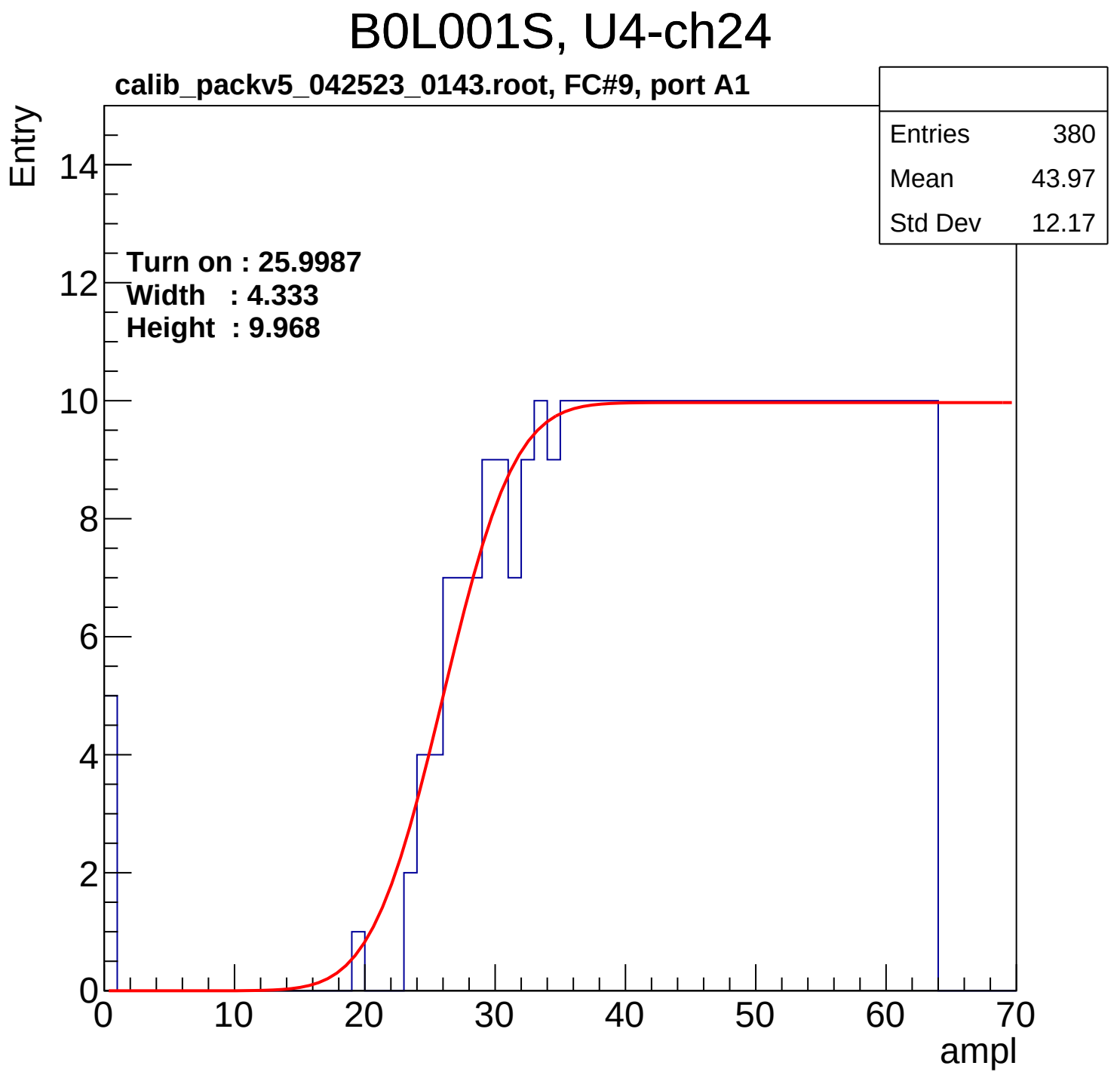
B0L001S, U4-ch24
calib_packv5_042523_0143.root, FC#9, port A1
Entries 380
Mean 43.97
Std Dev 12.17
Turn on : 25.9987
Width : 4.333
Height : 9.968
Entry
ampl
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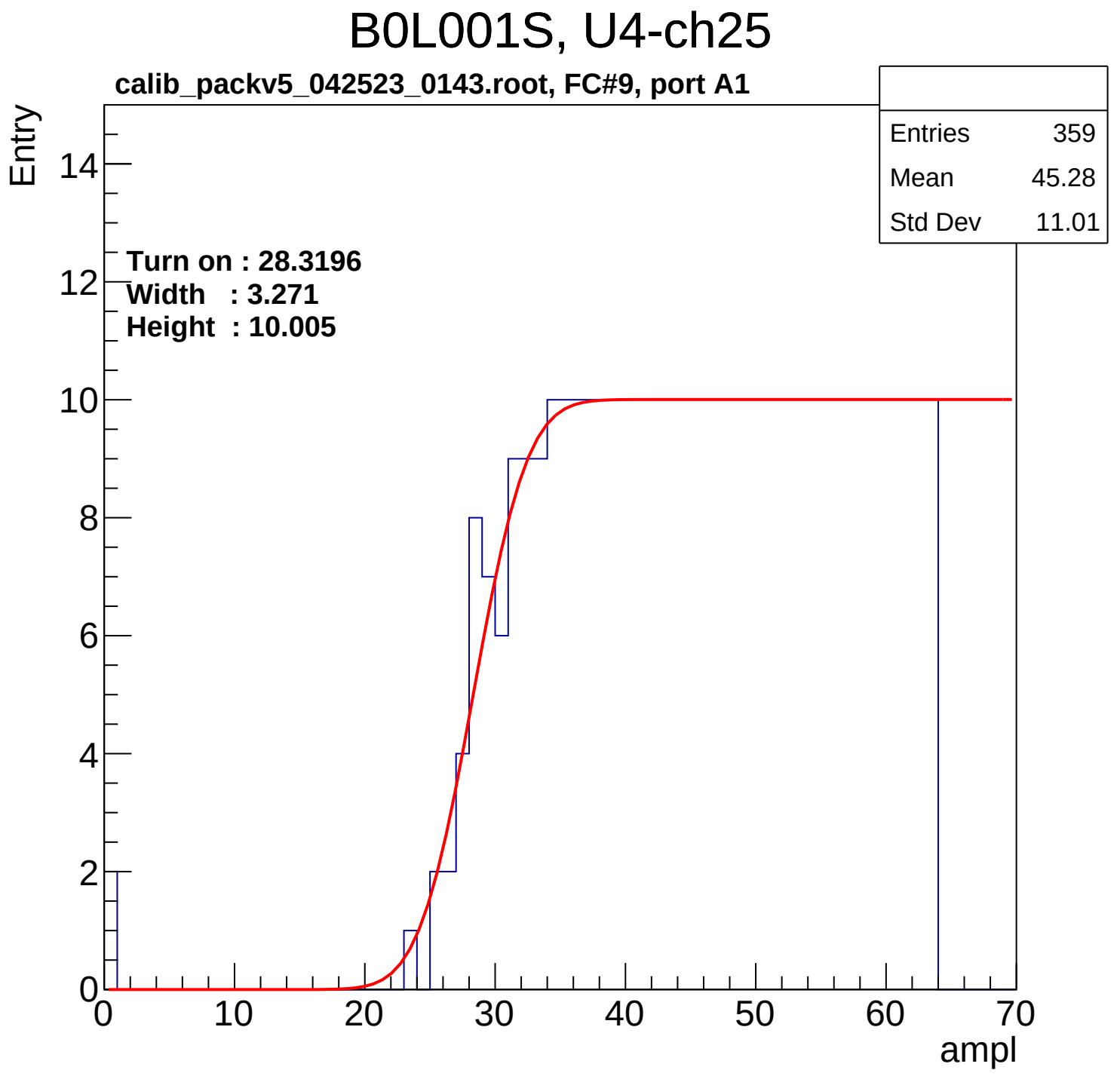
B0L001S, U4-ch25
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 45.28
Std Dev 11.01
Turn on : 28.3196
Width : 3.271
Height : 10.005
Entry
ampl
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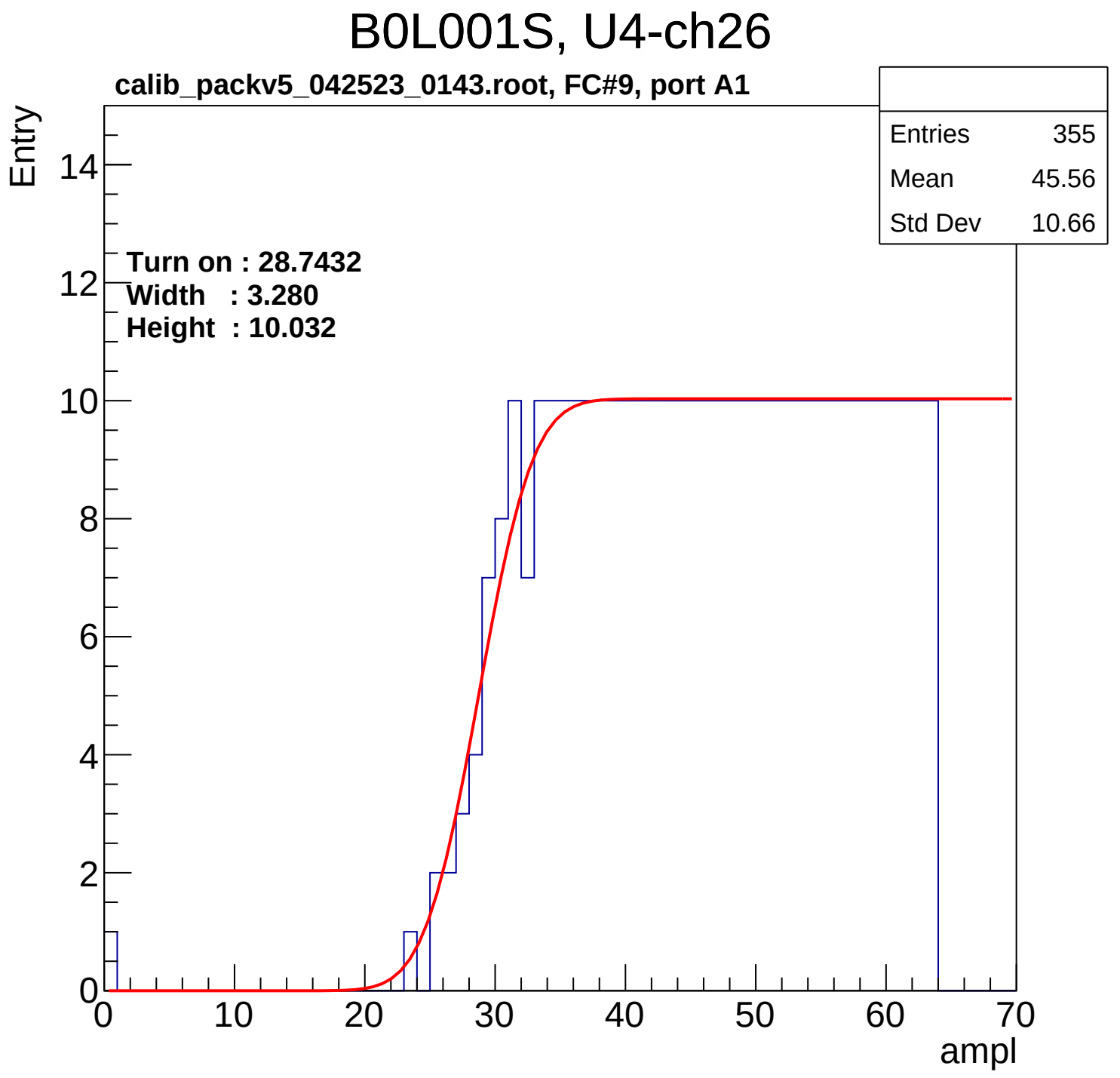
B0L001S, U4-ch26
calib_packv5_042523_0143.root, FC#9, port A1
Entries 355
Mean 45.56
Std Dev 10.66
Turn on : 28.7432
Width : 3.280
Height : 10.032
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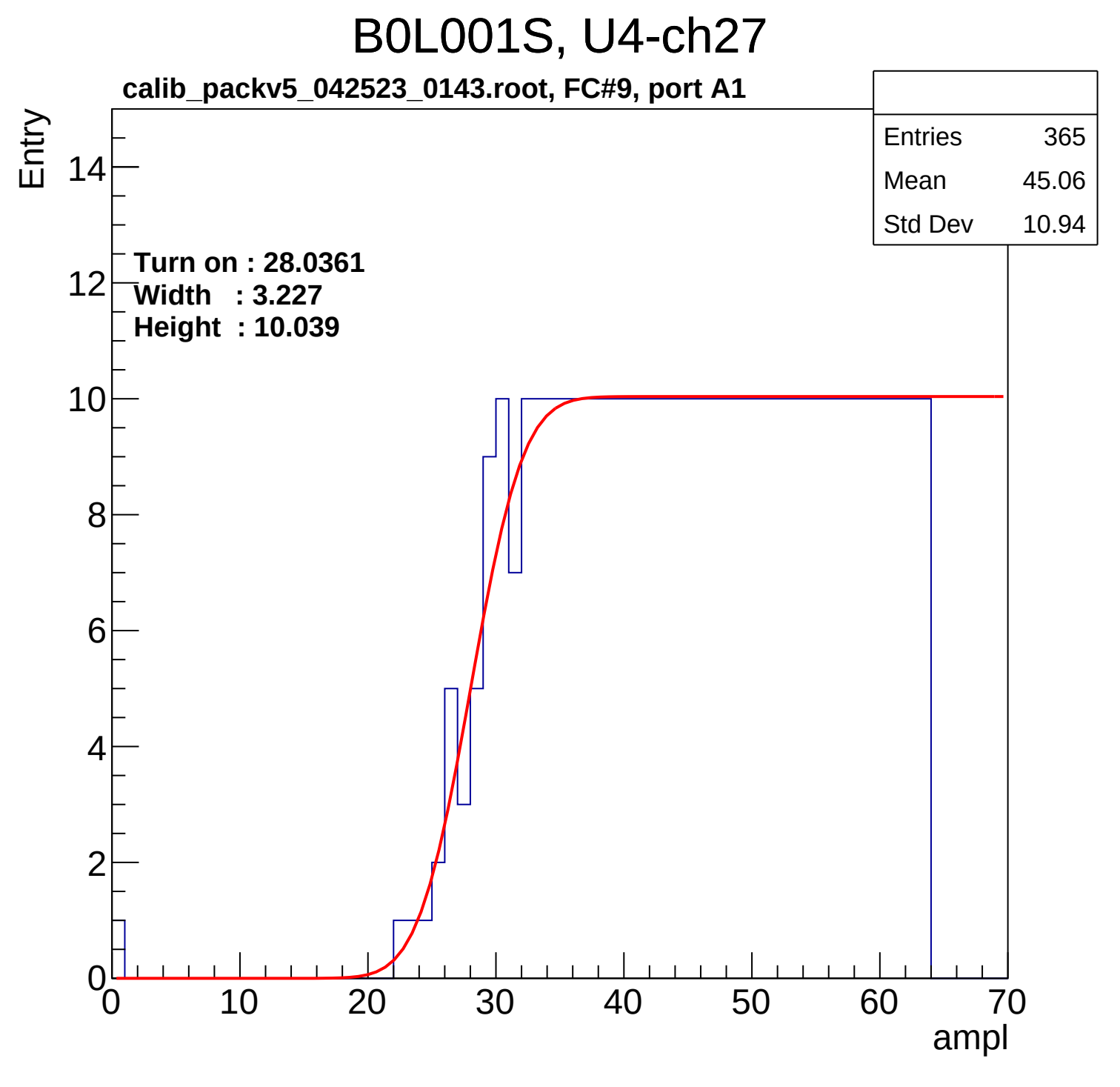
B0L001S, U4-ch27
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 45.06
Std Dev 10.94
Turn on : 28.0361
Width : 3.227
Height : 10.039
Entry
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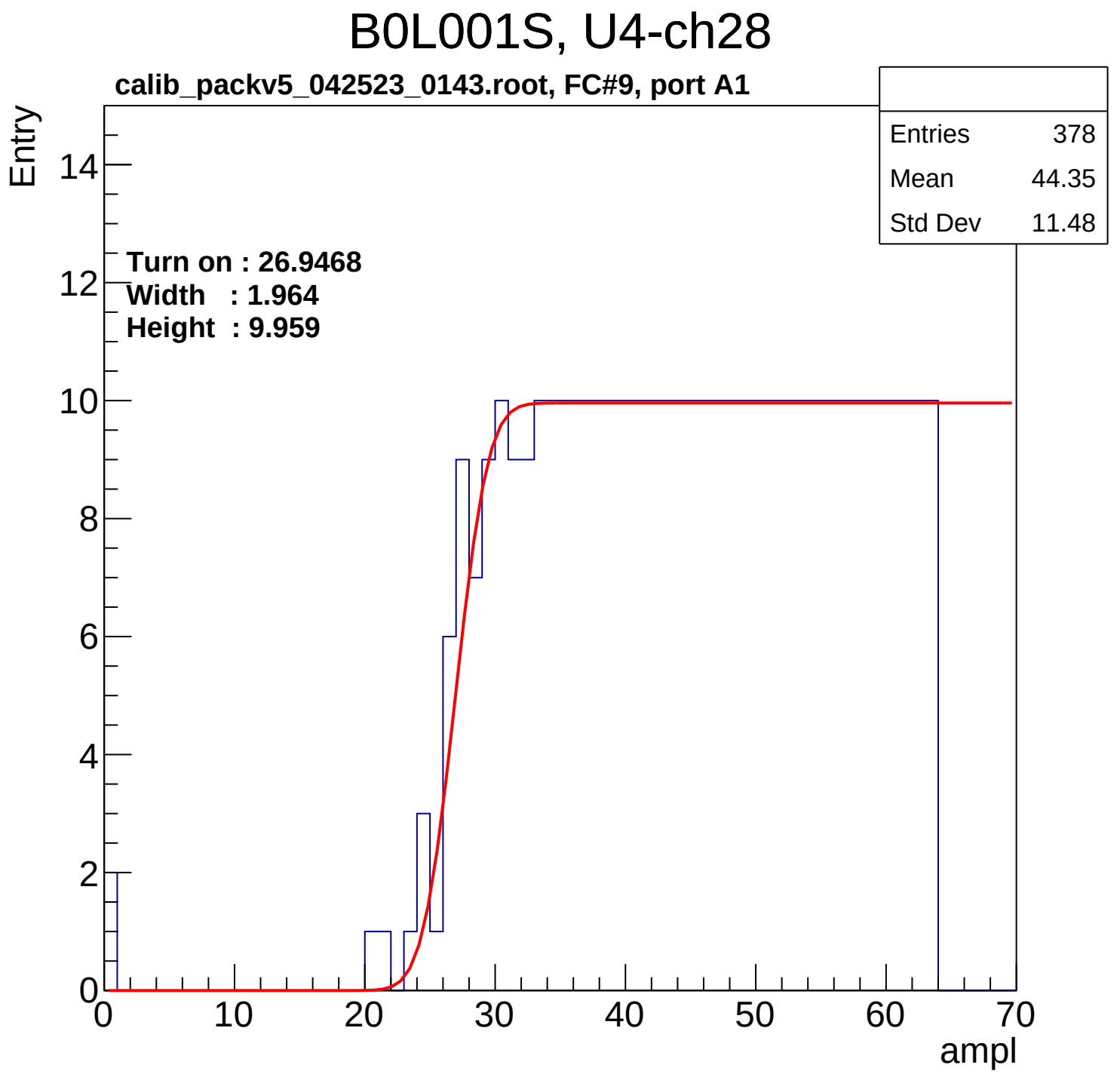
B0L001S, U4-ch28
calib_packv5_042523_0143.root, FC#9, port A1
Entries 378
Mean 44.35
Std Dev 11.48
Turn on : 26.9468
Width : 1.964
Height : 9.959
Entry
ampl
0
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4
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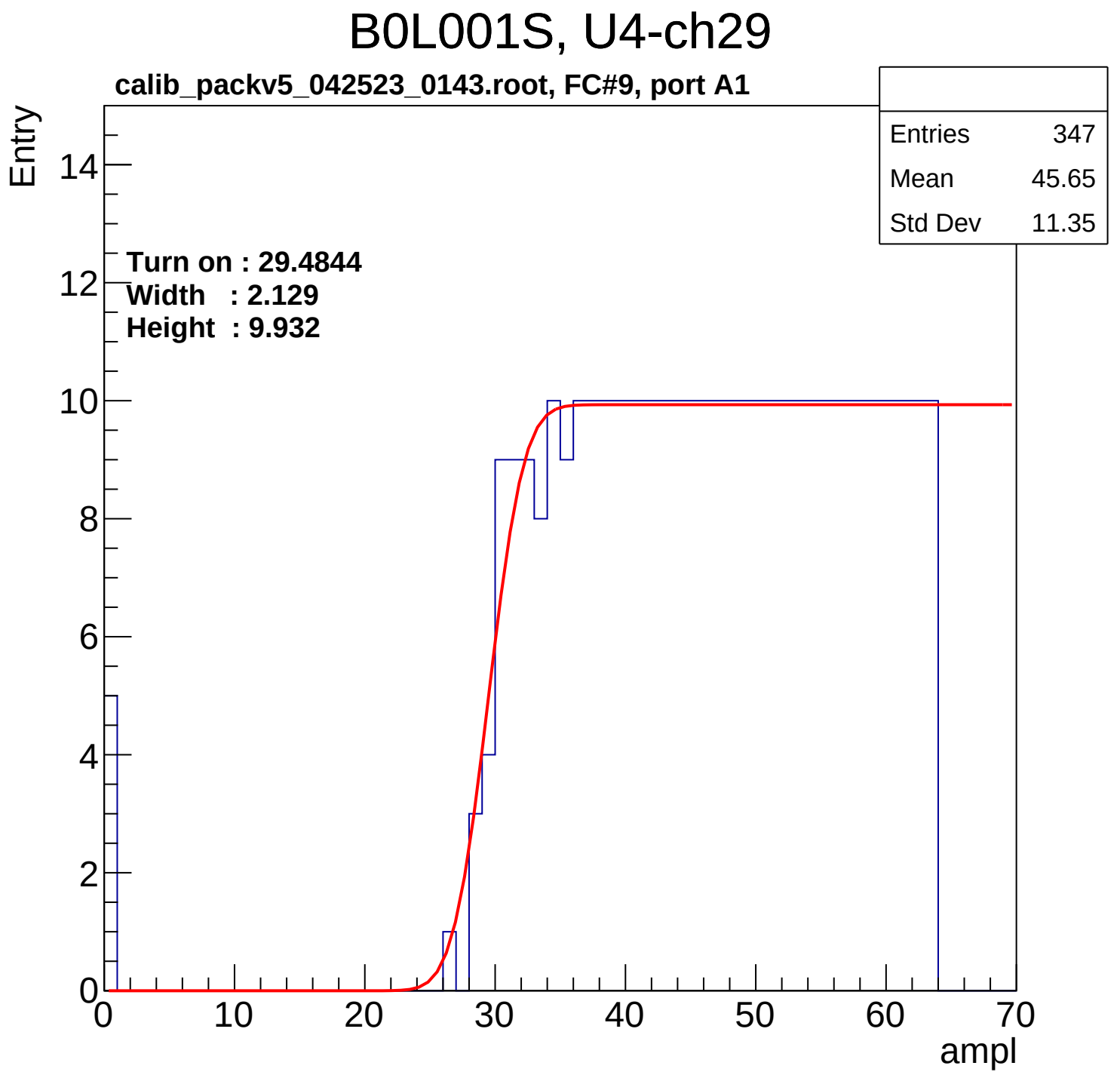
B0L001S, U4-ch29
calib_packv5_042523_0143.root, FC#9, port A1
Entries 347
Mean 45.65
Std Dev 11.35
Turn on : 29.4844
Width : 2.129
Height : 9.932
Entry
ampl
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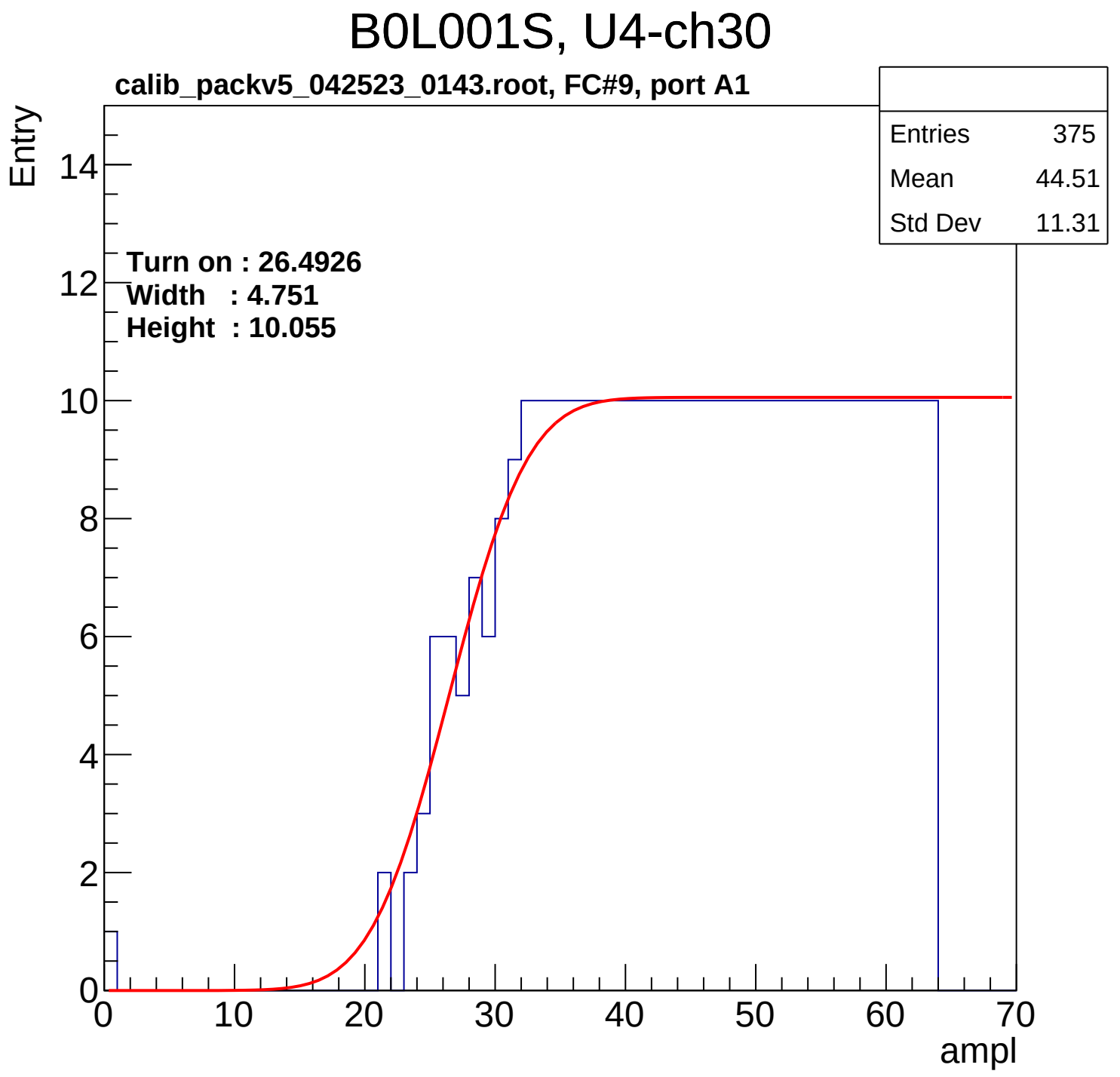
B0L001S, U4-ch30
calib_packv5_042523_0143.root, FC#9, port A1
Entries 375
Mean 44.51
Std Dev 11.31
Turn on : 26.4926
Width : 4.751
Height : 10.055
Entry
ampl
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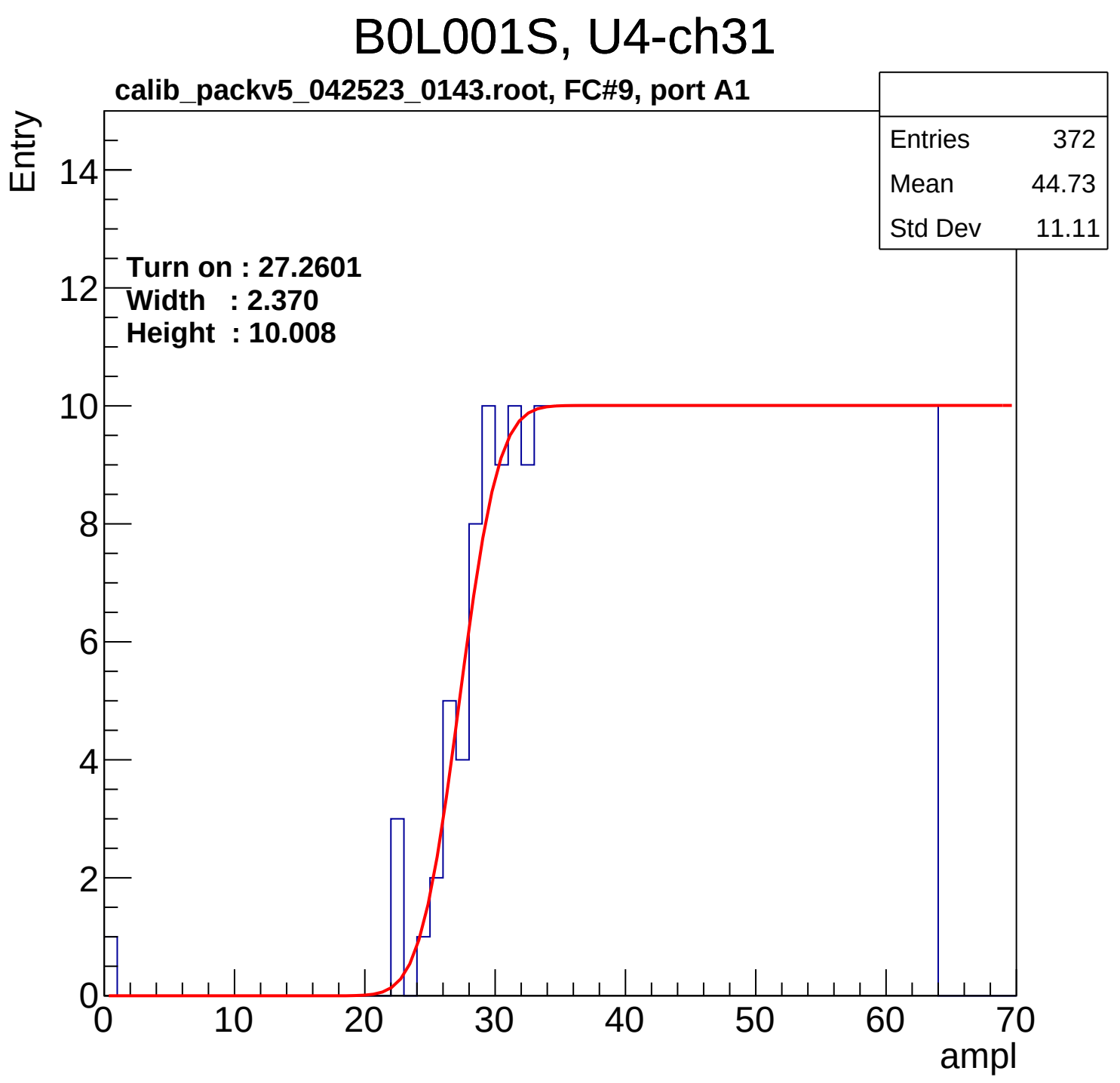
B0L001S, U4-ch31
calib_packv5_042523_0143.root, FC#9, port A1
Entries 372
Mean 44.73
Std Dev 11.11
Turn on : 27.2601
Width : 2.370
Height : 10.008
Entry
ampl
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2
4
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0
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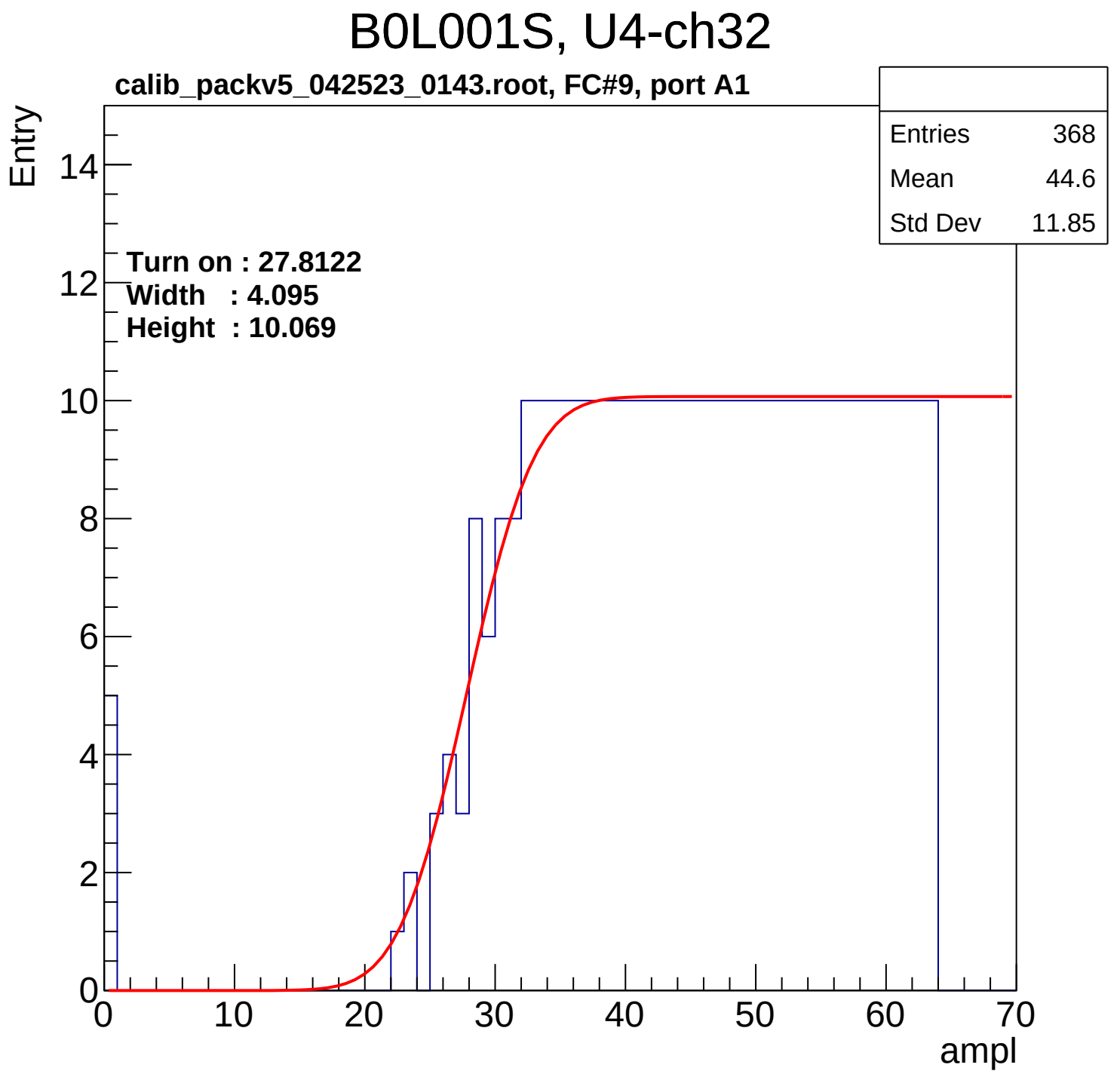
B0L001S, U4-ch32
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.6
Std Dev 11.85
Turn on : 27.8122
Width : 4.095
Height : 10.069
Entry
ampl
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2
4
6
8
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60
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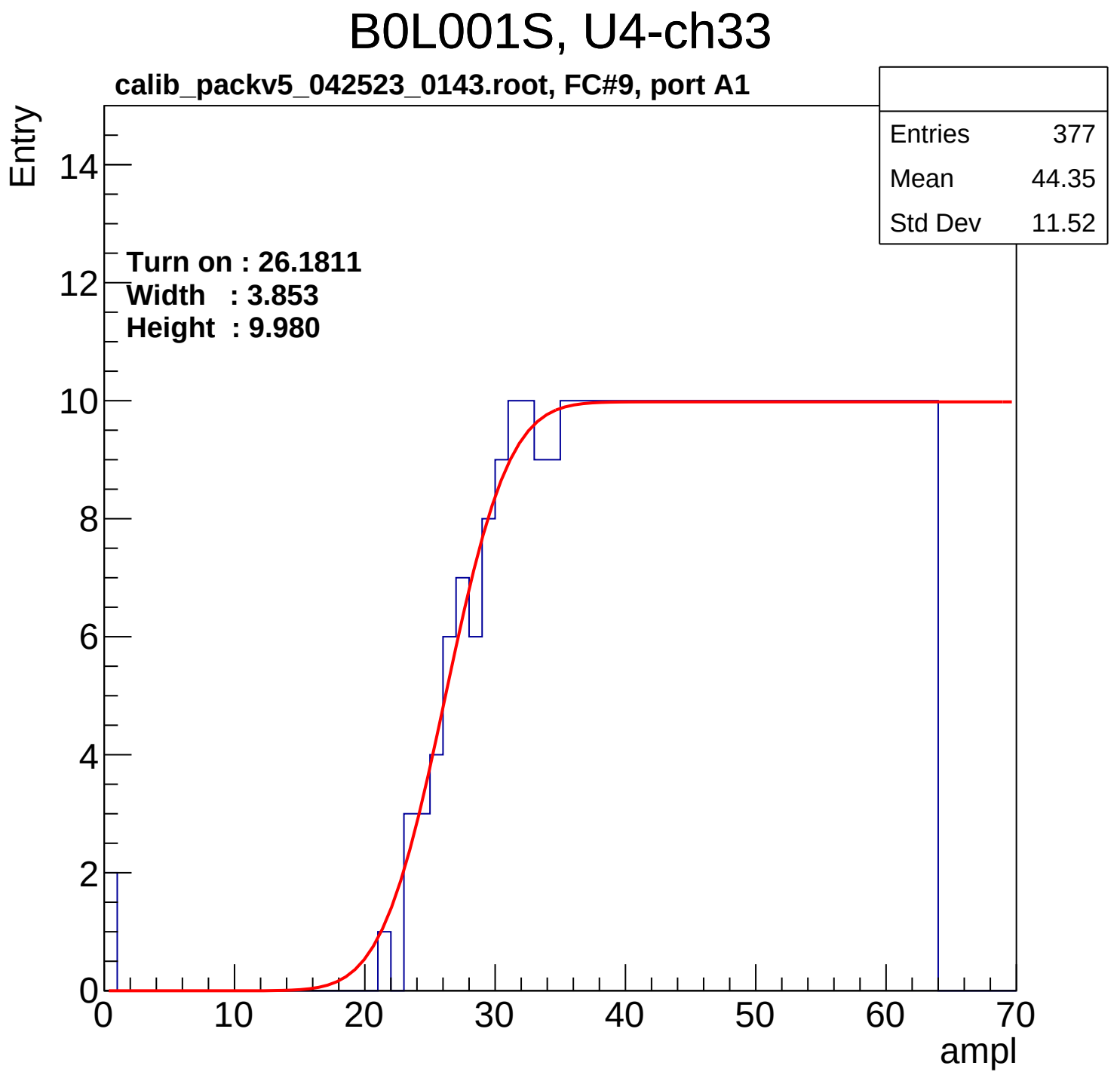
B0L001S, U4-ch33
calib_packv5_042523_0143.root, FC#9, port A1
Entries 377
Mean 44.35
Std Dev 11.52
Turn on : 26.1811
Width : 3.853
Height : 9.980
Entry
ampl
0
2
4
6
8
10
12
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0
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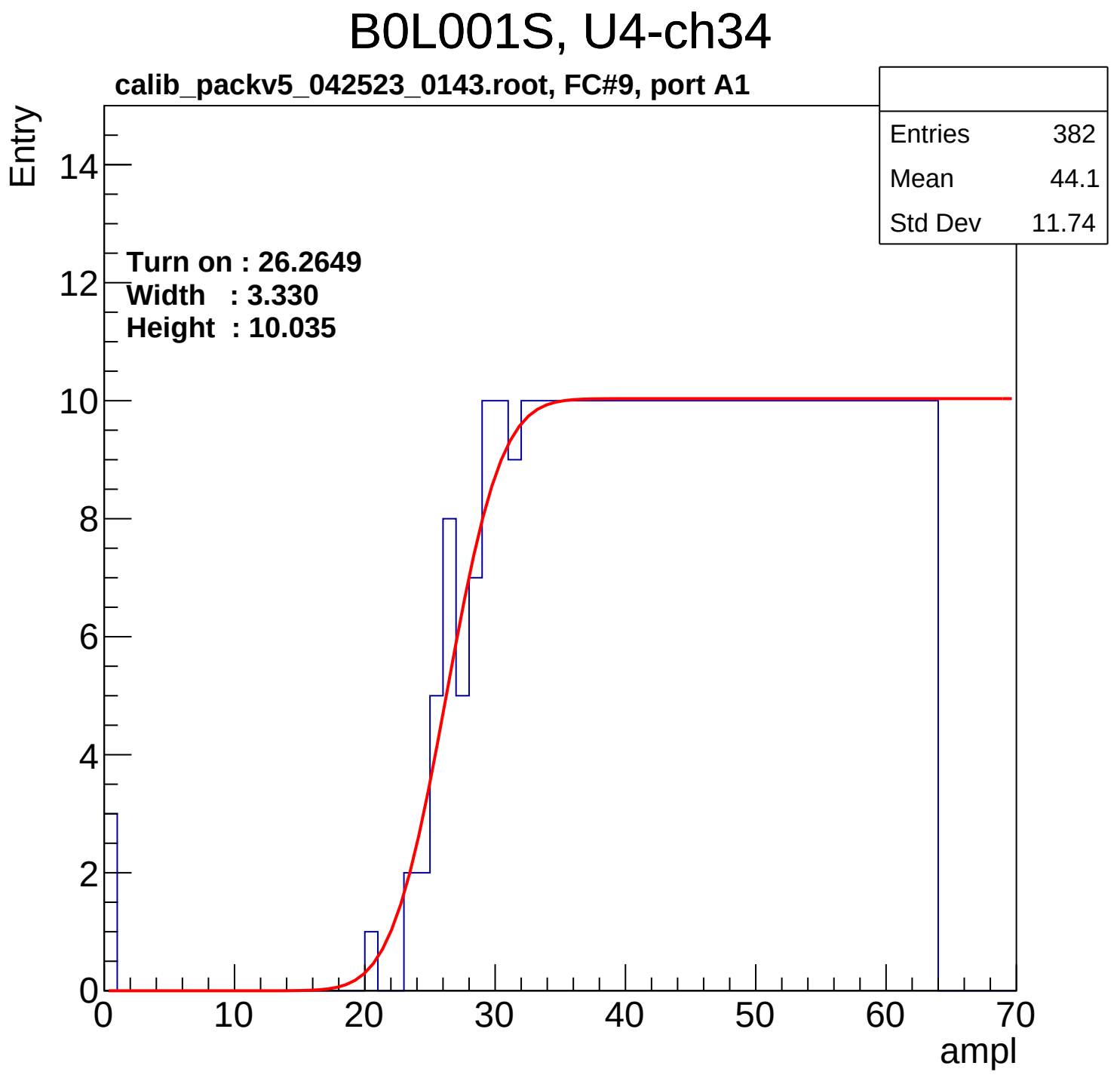
B0L001S, U4-ch34
calib_packv5_042523_0143.root, FC#9, port A1
Entries 382
Mean 44.1
Std Dev 11.74
Turn on : 26.2649
Width : 3.330
Height : 10.035
Entry
ampl
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2
4
6
8
10
12
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0
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60
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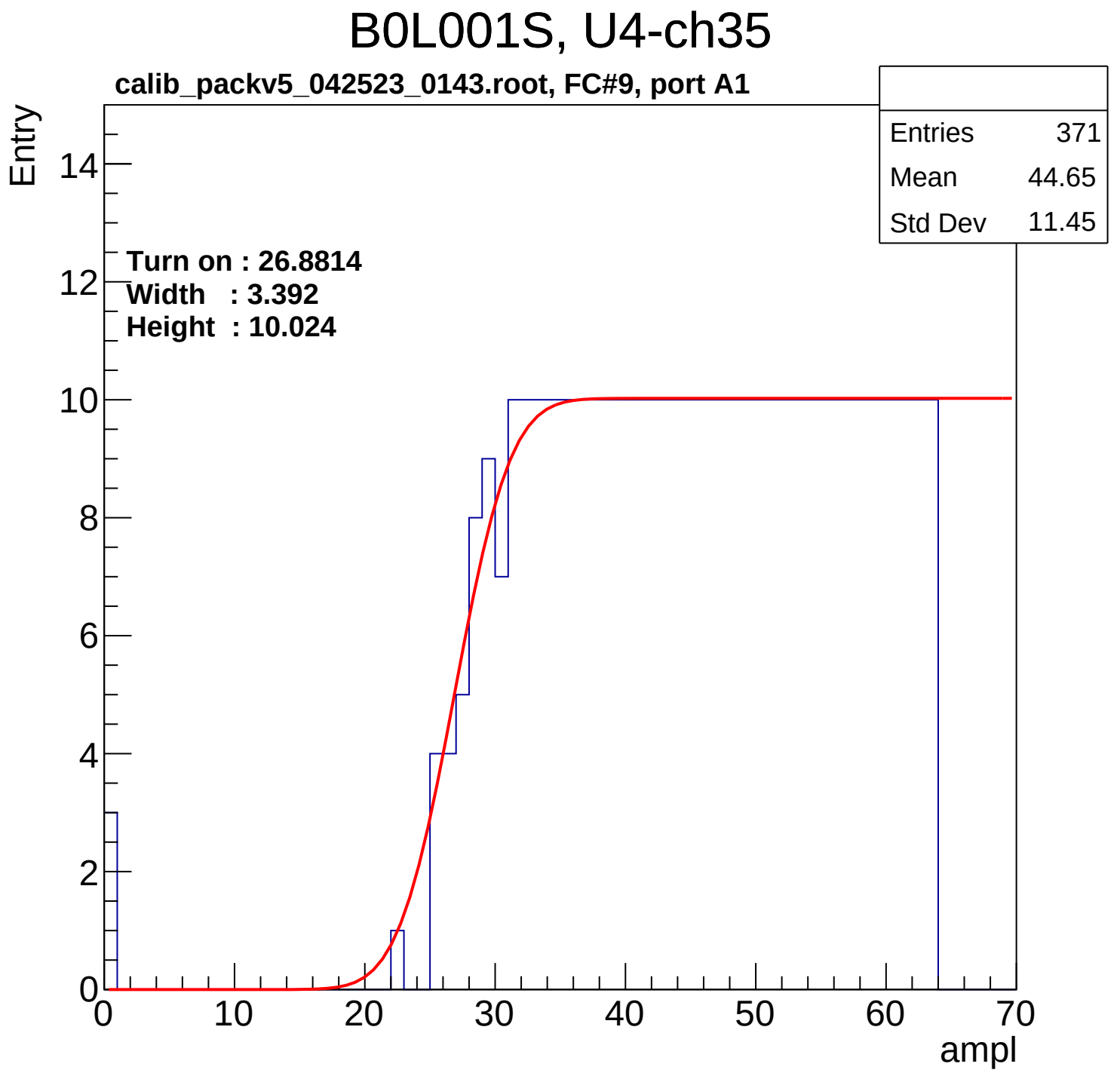
B0L001S, U4-ch35
calib_packv5_042523_0143.root, FC#9, port A1
Entries 371
Mean 44.65
Std Dev 11.45
Turn on : 26.8814
Width : 3.392
Height : 10.024
Entry
ampl
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2
4
6
8
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0
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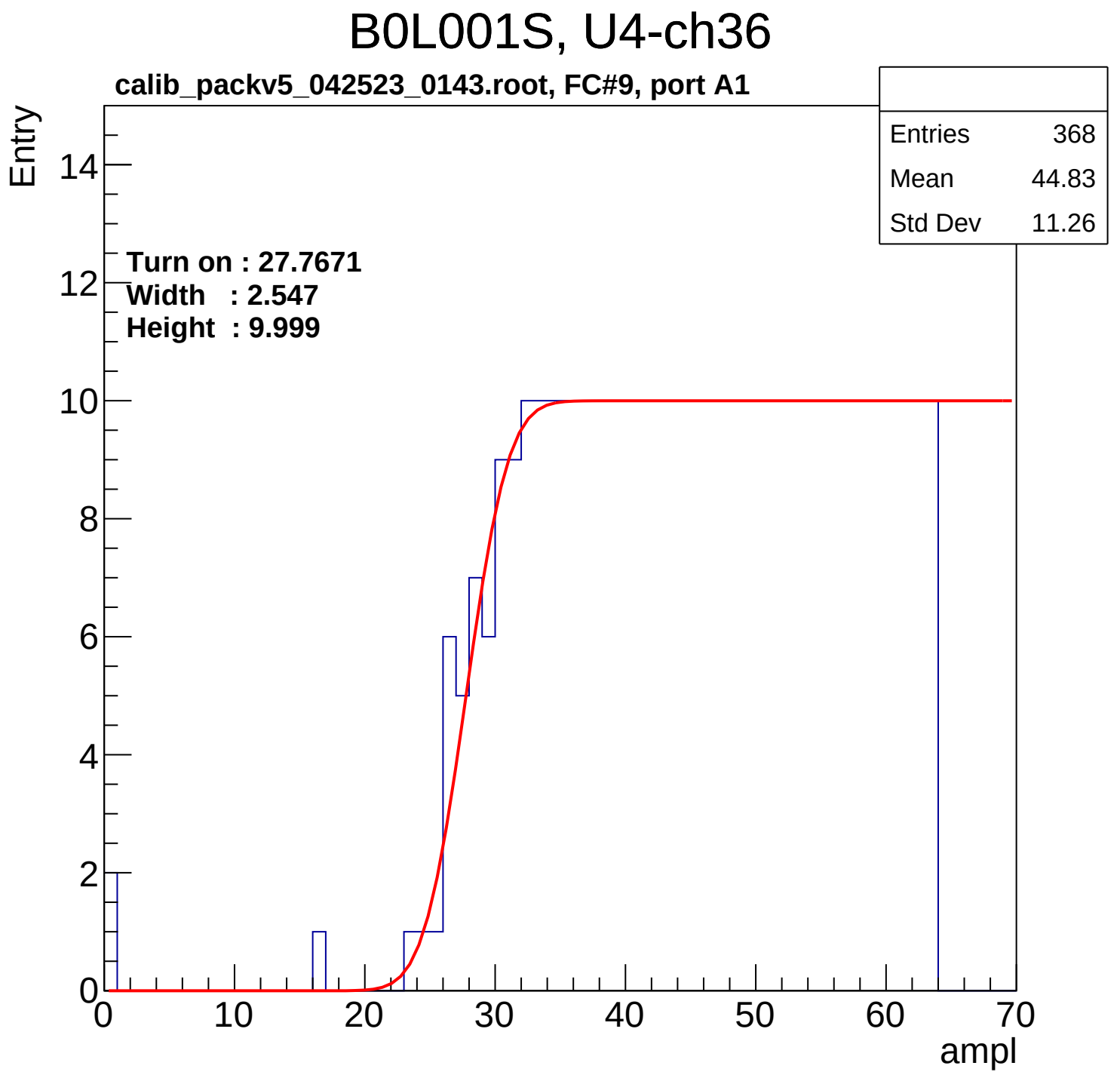
B0L001S, U4-ch36
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.83
Std Dev 11.26
Turn on : 27.7671
Width : 2.547
Height : 9.999
Entry
ampl
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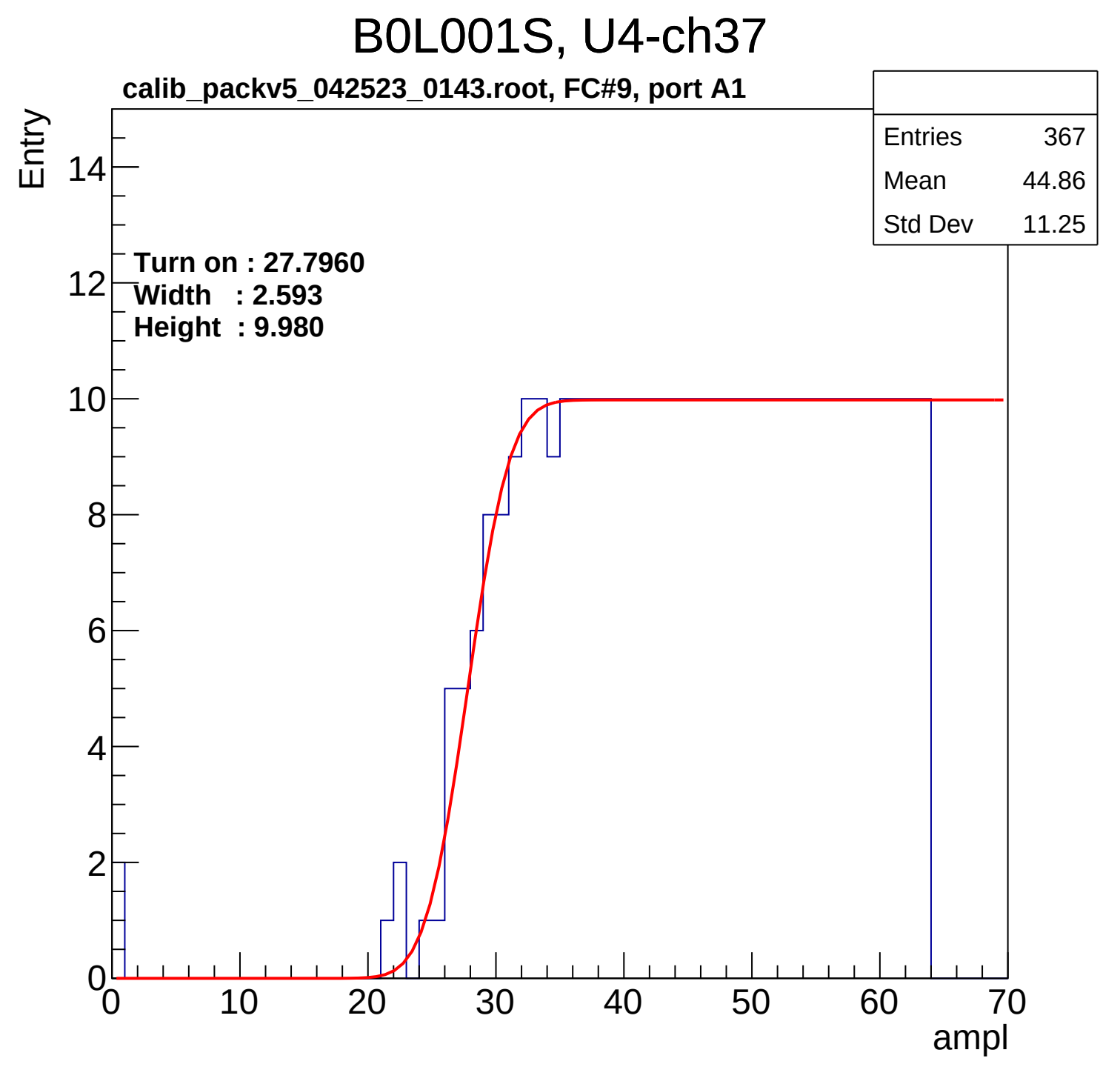
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U4-ch37
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.86
Std Dev 11.25
Turn on : 27.7960
Width : 2.593
Height : 9.980
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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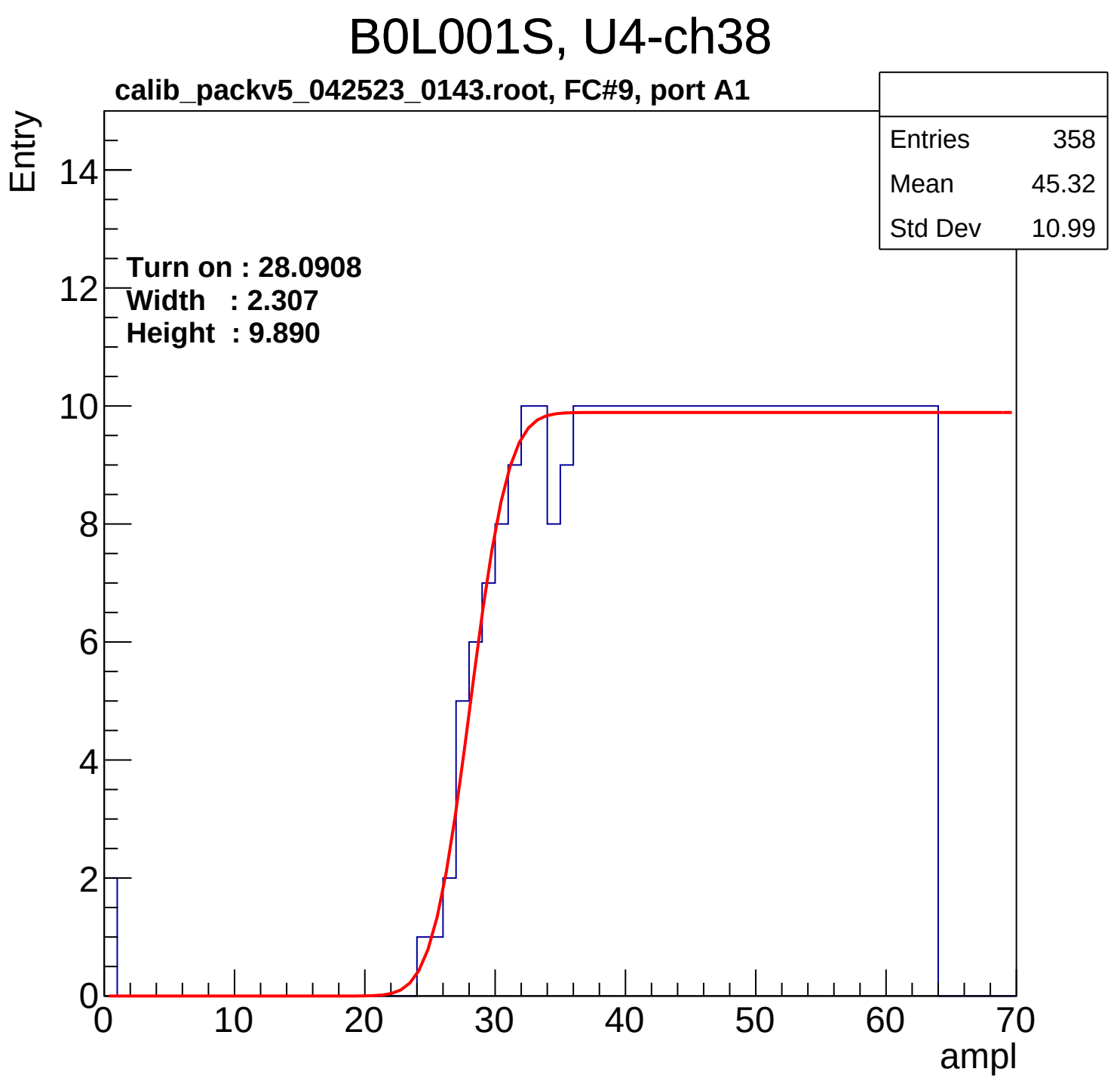
B0L001S, U4-ch38
calib_packv5_042523_0143.root, FC#9, port A1
Entries 358
Mean 45.32
Std Dev 10.99
Turn on : 28.0908
Width : 2.307
Height : 9.890
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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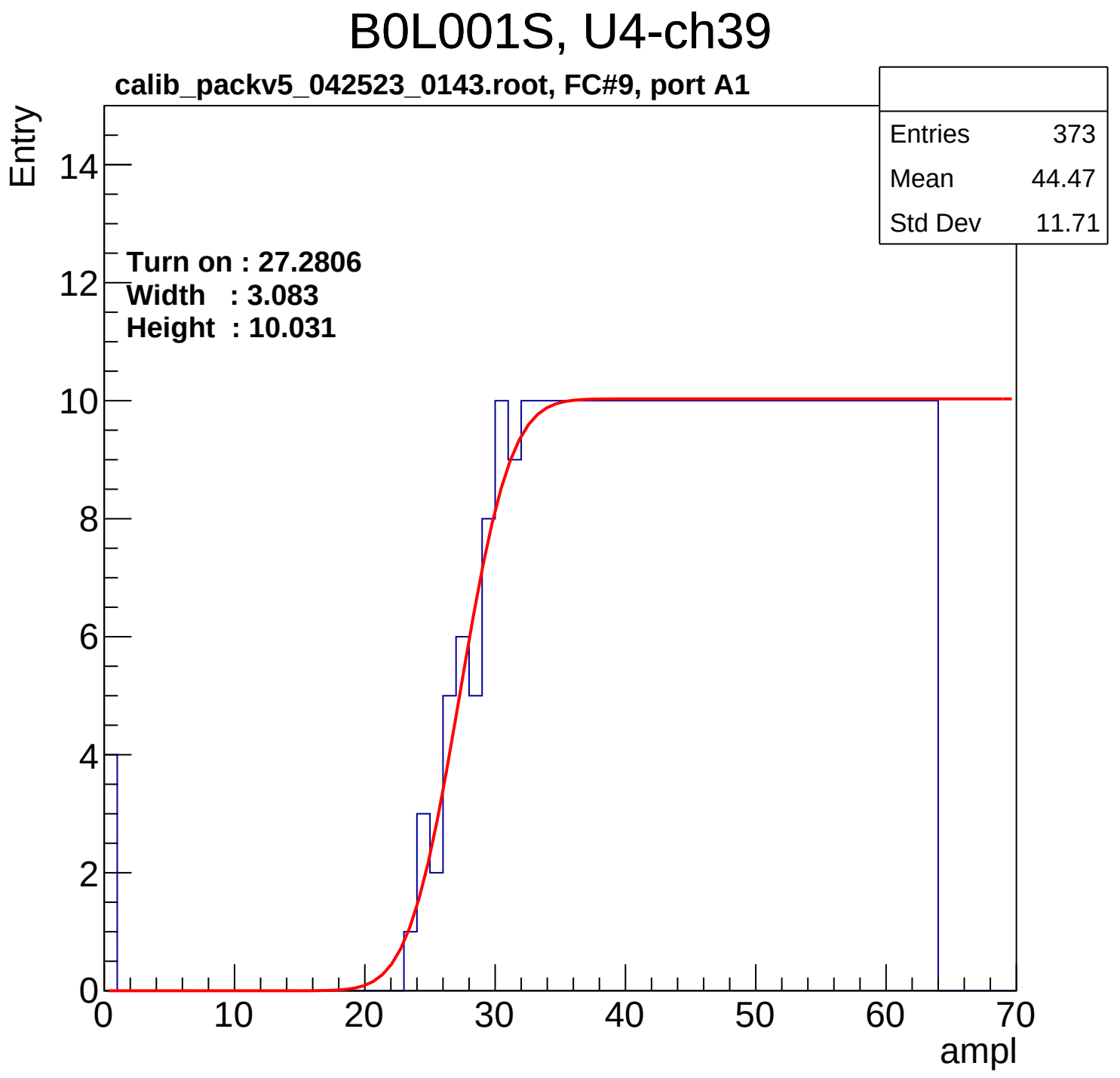
B0L001S, U4-ch39
calib_packv5_042523_0143.root, FC#9, port A1
Entries 373
Mean 44.47
Std Dev 11.71
Turn on : 27.2806
Width : 3.083
Height : 10.031
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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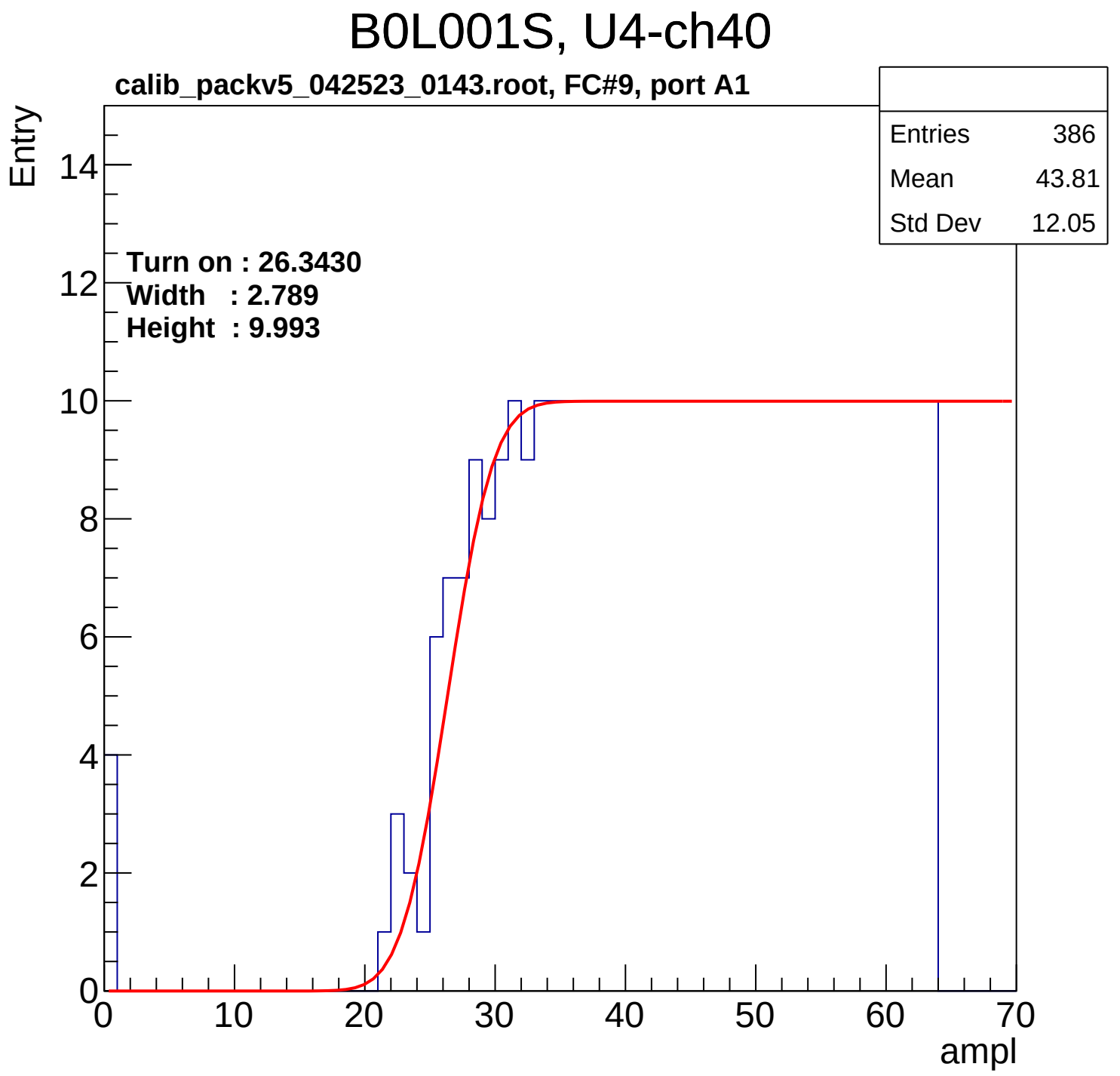
B0L001S, U4-ch40
calib_packv5_042523_0143.root, FC#9, port A1
Entries 386
Mean 43.81
Std Dev 12.05
Turn on : 26.3430
Width : 2.789
Height : 9.993
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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40
50
60
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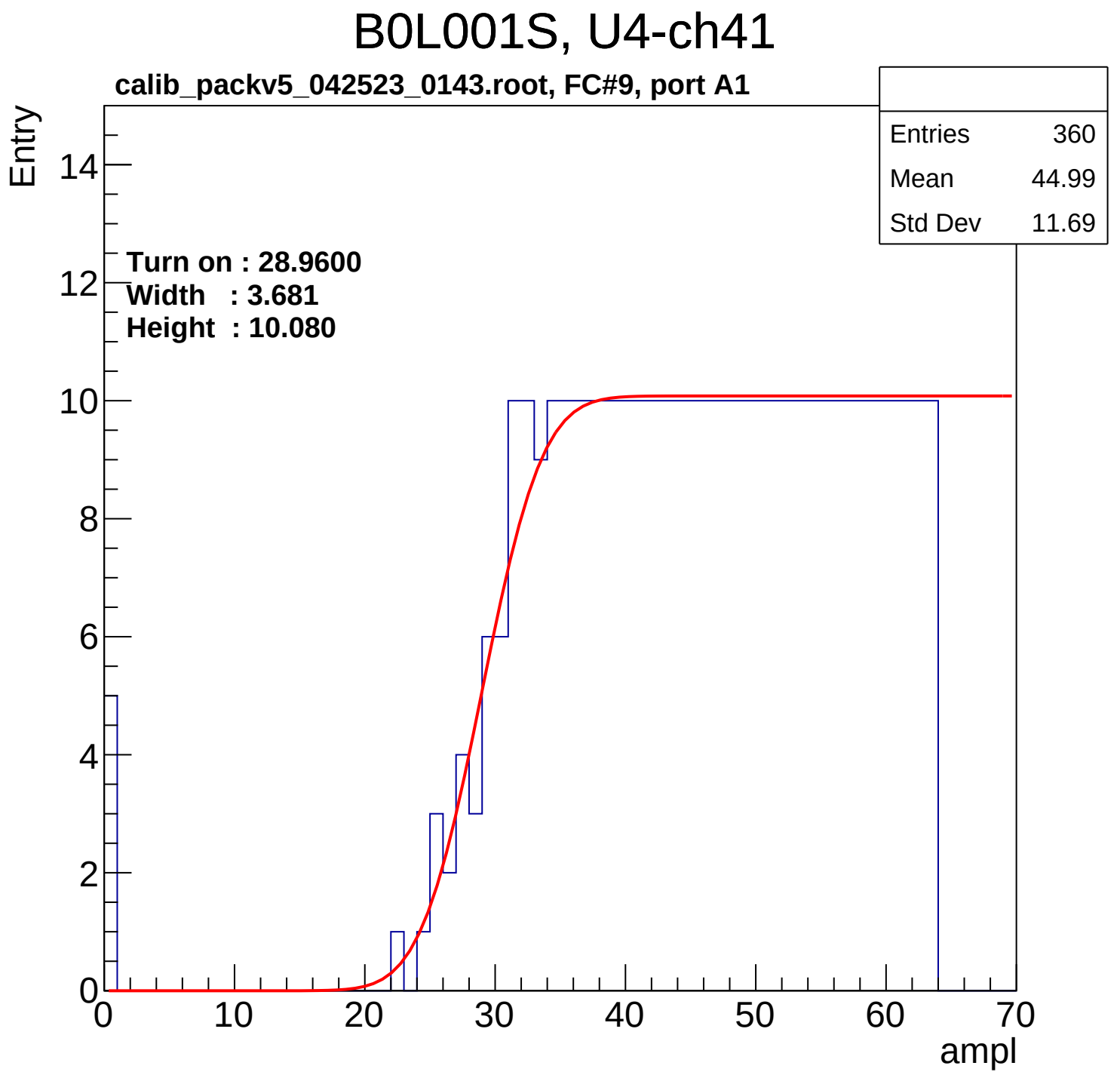
B0L001S, U4-ch41
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 44.99
Std Dev 11.69
Turn on : 28.9600
Width : 3.681
Height : 10.080
Entry
ampl
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6
8
10
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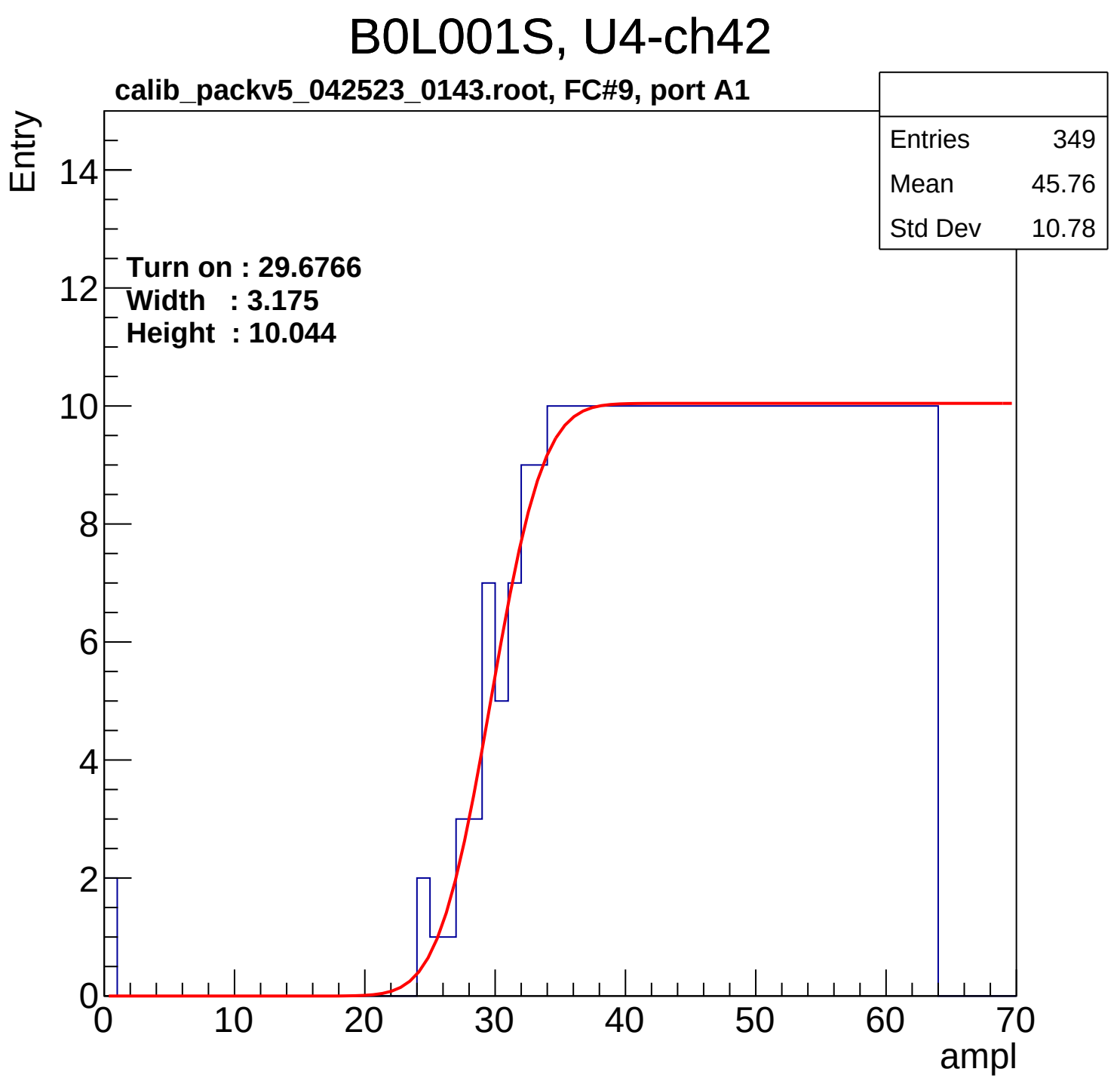
B0L001S, U4-ch42
calib_packv5_042523_0143.root, FC#9, port A1
Entries 349
Mean 45.76
Std Dev 10.78
Turn on : 29.6766
Width : 3.175
Height : 10.044
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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60
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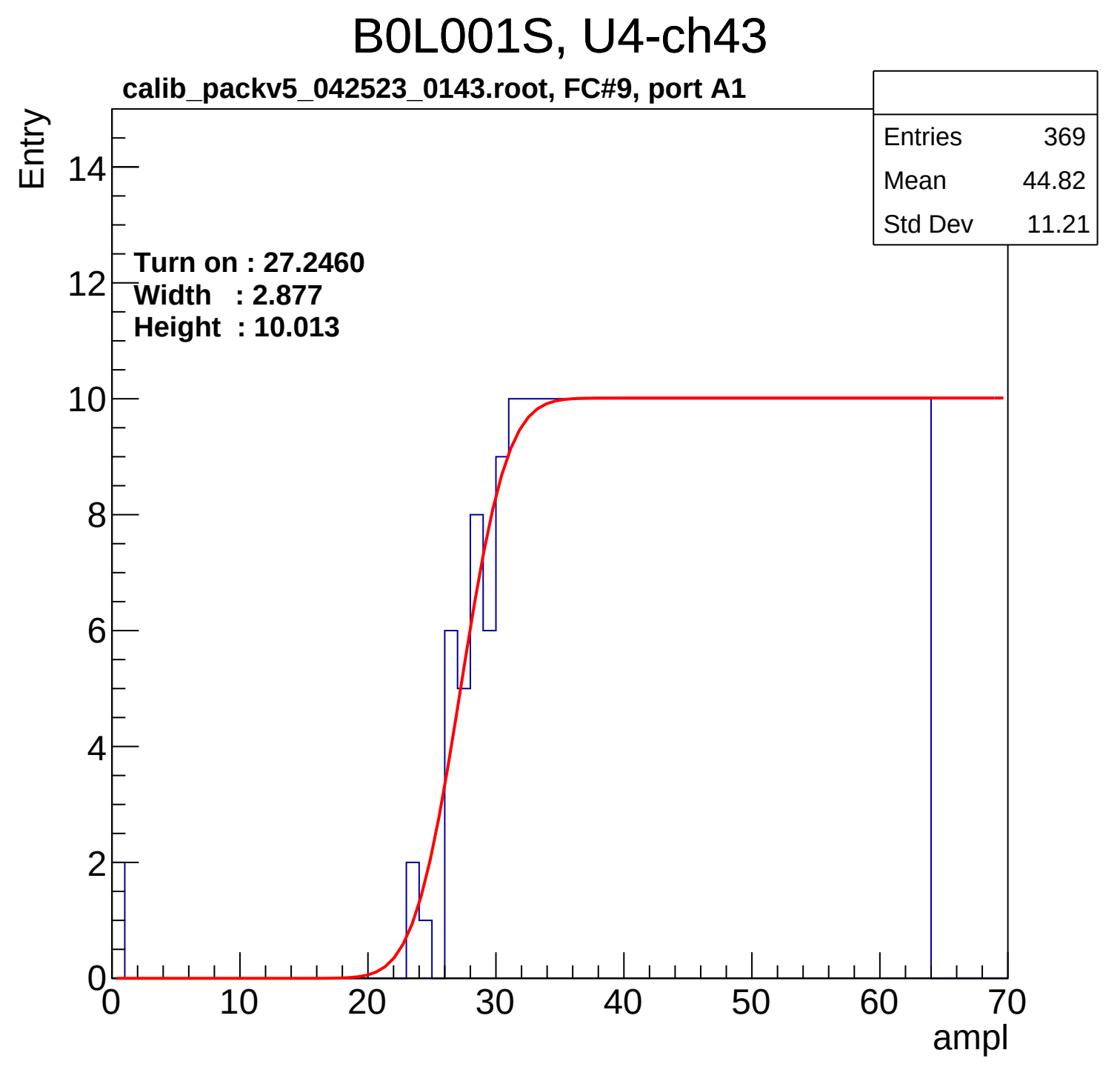
B0L001S, U4-ch43
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.82
Std Dev 11.21
Turn on : 27.2460
Width : 2.877
Height : 10.013
Entry
ampl
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6
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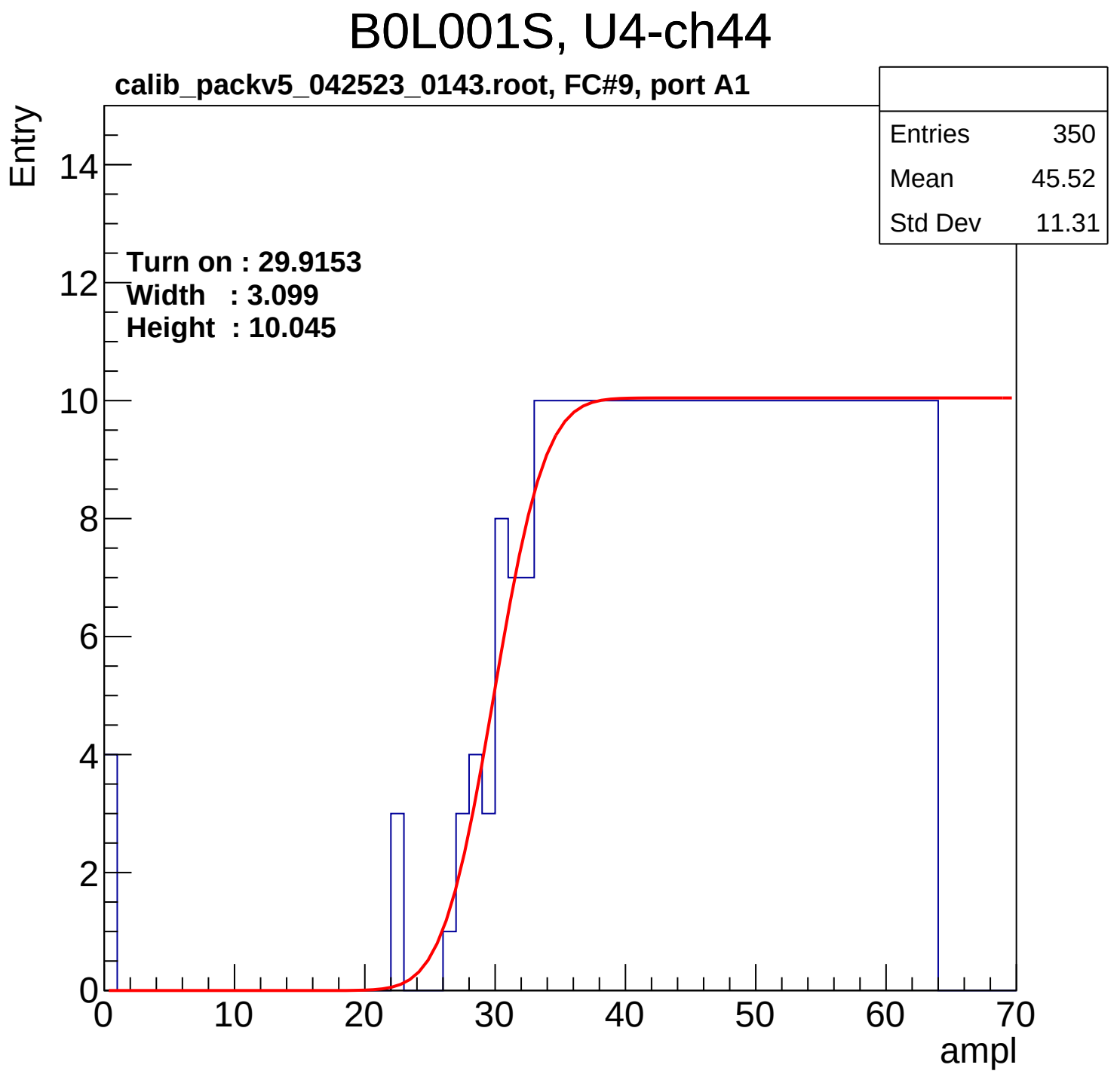
B0L001S, U4-ch44
calib_packv5_042523_0143.root, FC#9, port A1
Entries 350
Mean 45.52
Std Dev 11.31
Turn on : 29.9153
Width : 3.099
Height : 10.045
Entry
ampl
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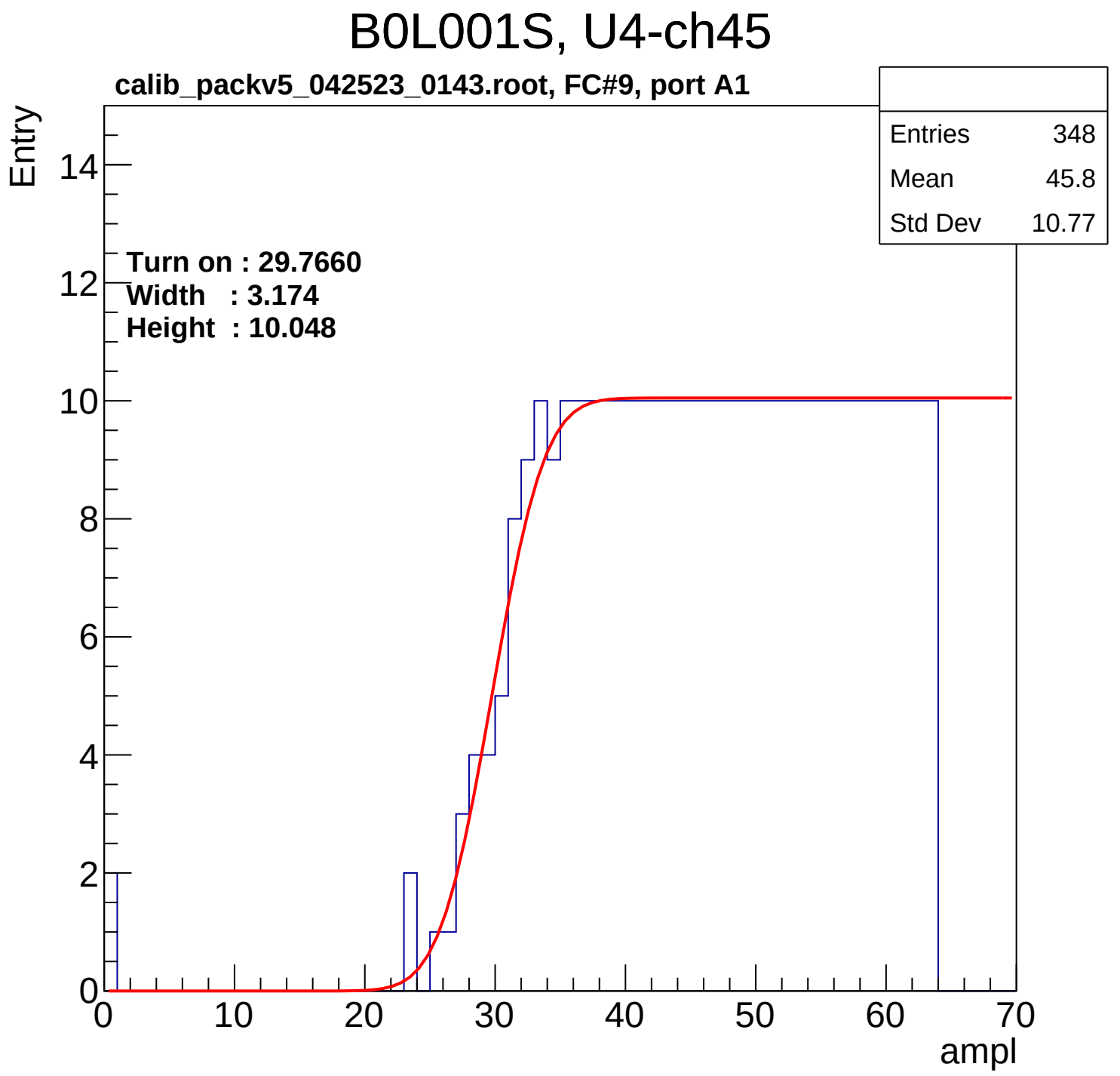
B0L001S, U4-ch45
calib_packv5_042523_0143.root, FC#9, port A1
Entries 348
Mean 45.8
Std Dev 10.77
Turn on : 29.7660
Width : 3.174
Height : 10.048
Entry
ampl
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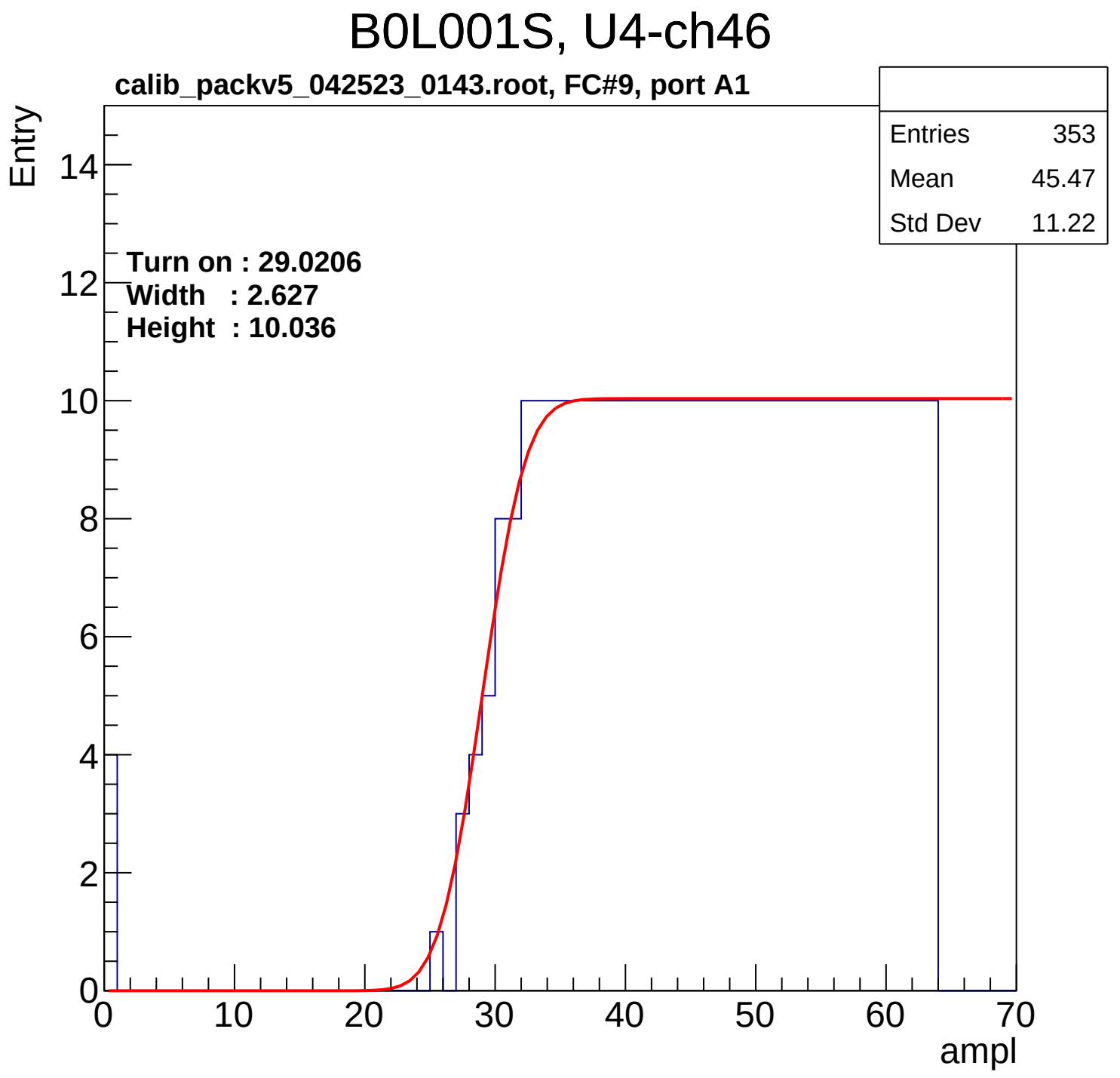
B0L001S, U4-ch46
calib_packv5_042523_0143.root, FC#9, port A1
Entries 353
Mean 45.47
Std Dev 11.22
Turn on : 29.0206
Width : 2.627
Height : 10.036
Entry
ampl
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6
8
10
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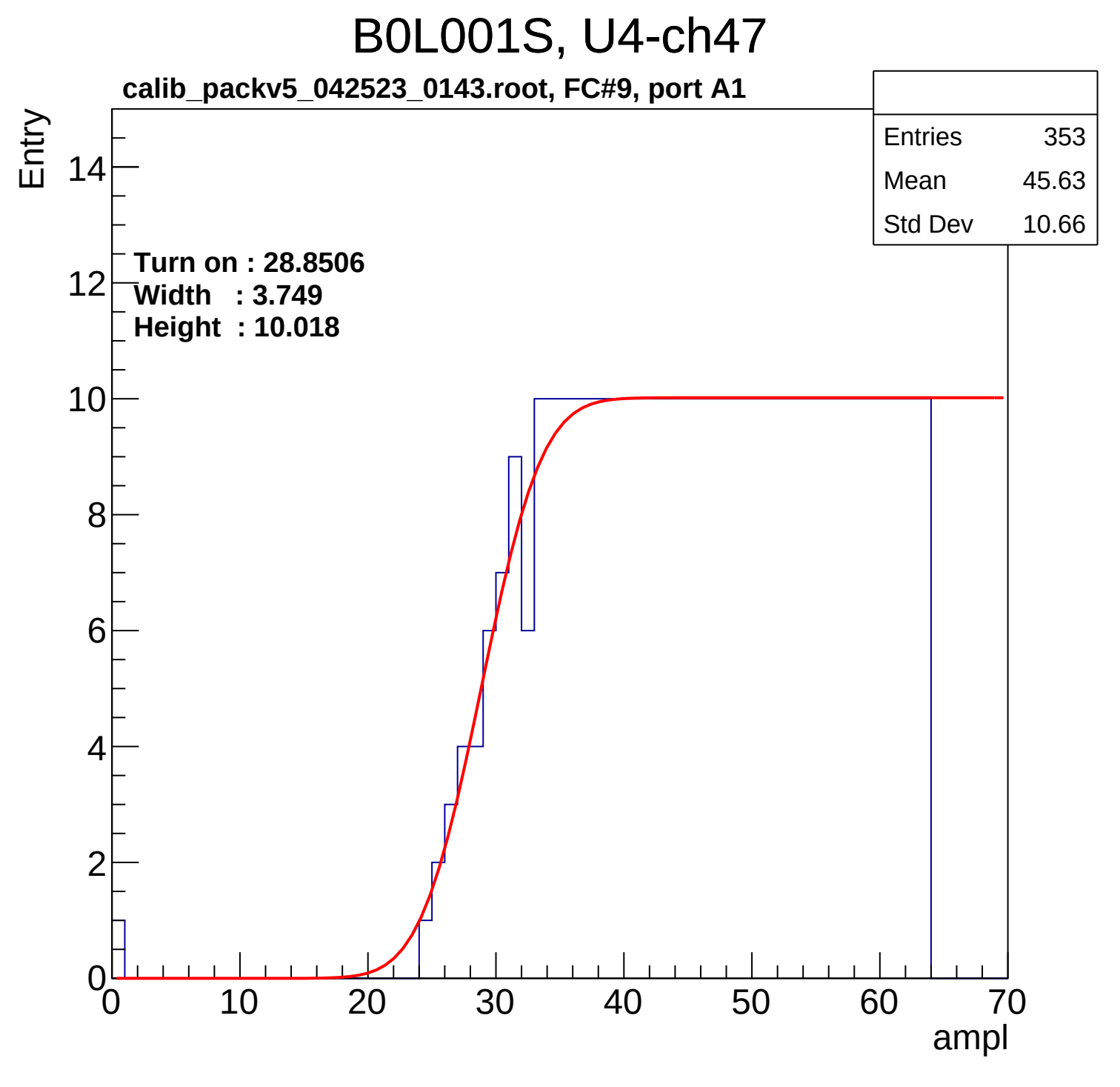
B0L001S, U4-ch47
calib_packv5_042523_0143.root, FC#9, port A1
Entries 353
Mean 45.63
Std Dev 10.66
Turn on : 28.8506
Width : 3.749
Height : 10.018
Entry
ampl
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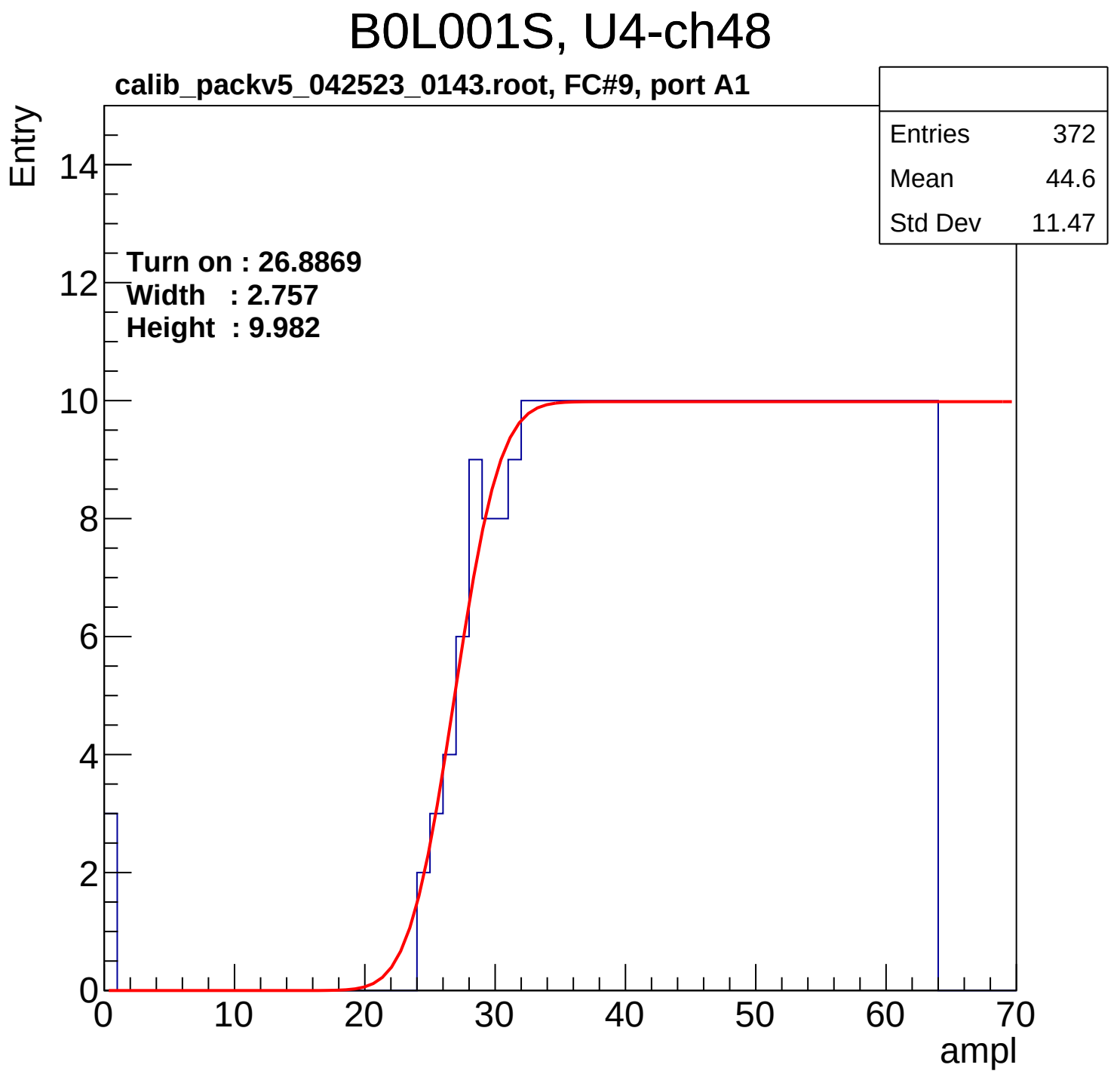
B0L001S, U4-ch48
calib_packv5_042523_0143.root, FC#9, port A1
Entries 372
Mean 44.6
Std Dev 11.47
Turn on : 26.8869
Width : 2.757
Height : 9.982
Entry
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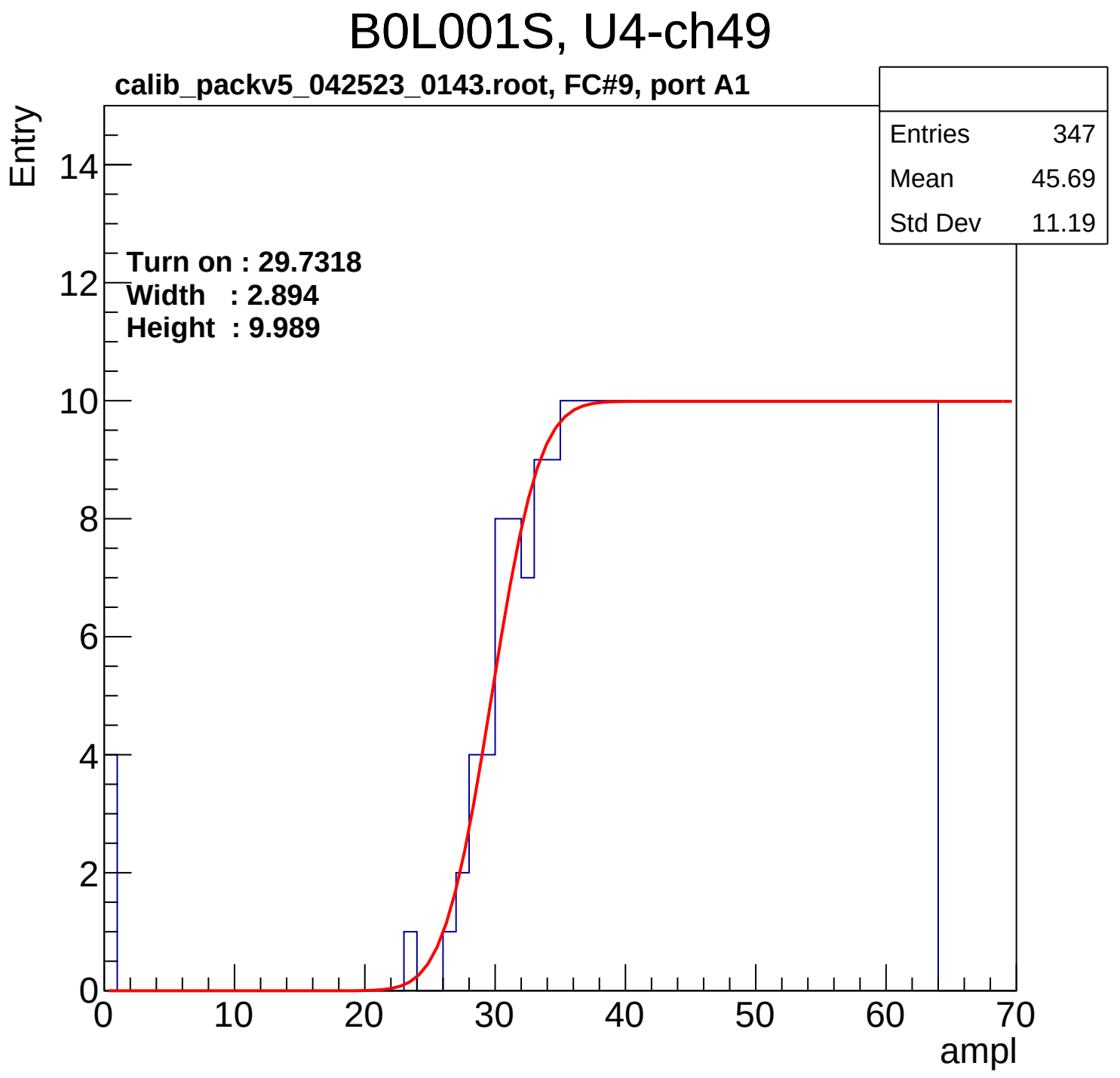
B0L001S, U4-ch49
calib_packv5_042523_0143.root, FC#9, port A1
Entries 347
Mean 45.69
Std Dev 11.19
Turn on : 29.7318
Width : 2.894
Height : 9.989
Entry
ampl
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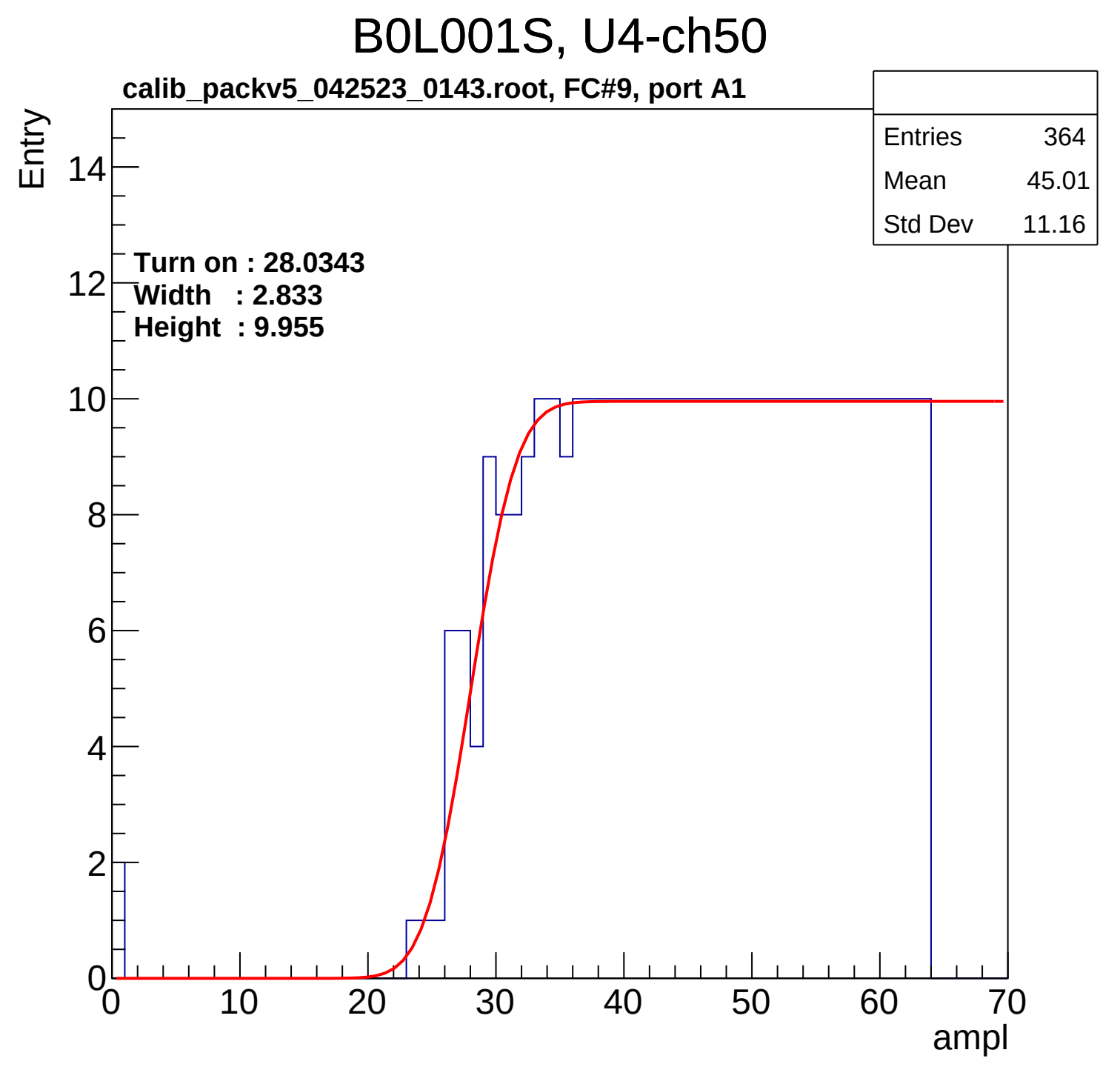
B0L001S, U4-ch50
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 45.01
Std Dev 11.16
Turn on : 28.0343
Width : 2.833
Height : 9.955
Entry
ampl
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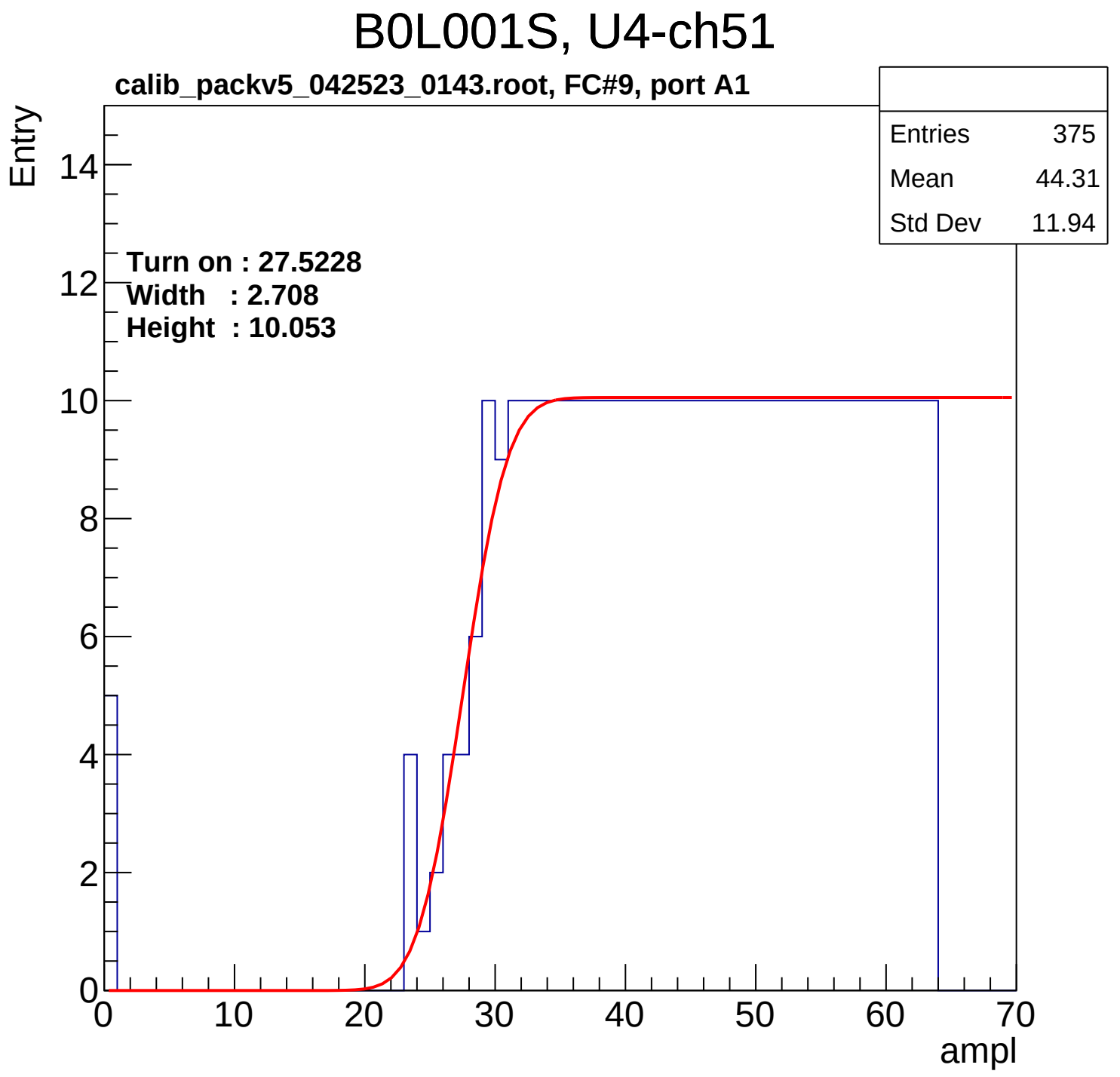
B0L001S, U4-ch51
calib_packv5_042523_0143.root, FC#9, port A1
Entries 375
Mean 44.31
Std Dev 11.94
Turn on : 27.5228
Width : 2.708
Height : 10.053
Entry
ampl
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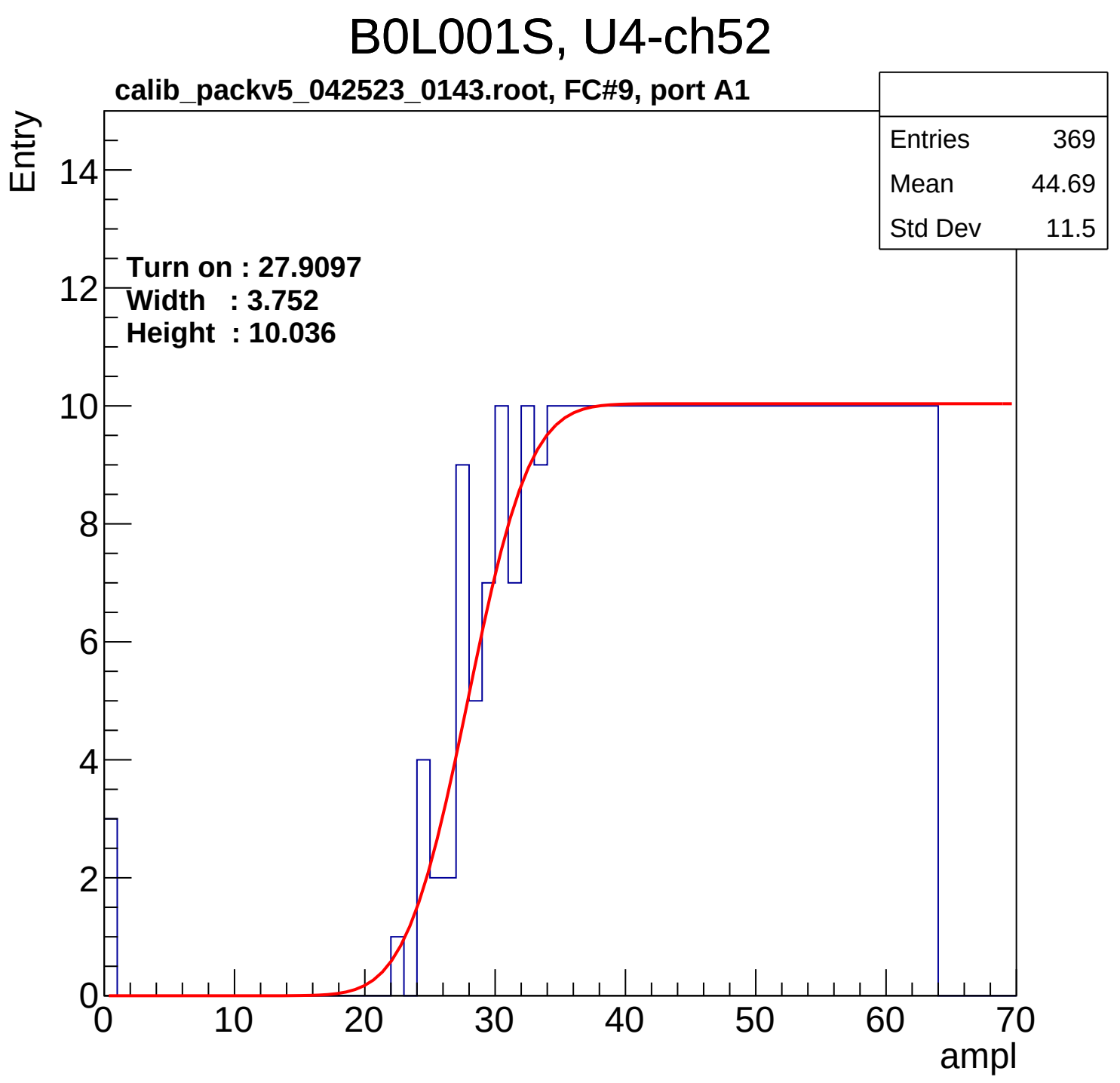
B0L001S, U4-ch52
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.69
Std Dev 11.5
Turn on : 27.9097
Width : 3.752
Height : 10.036
Entry
ampl
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60
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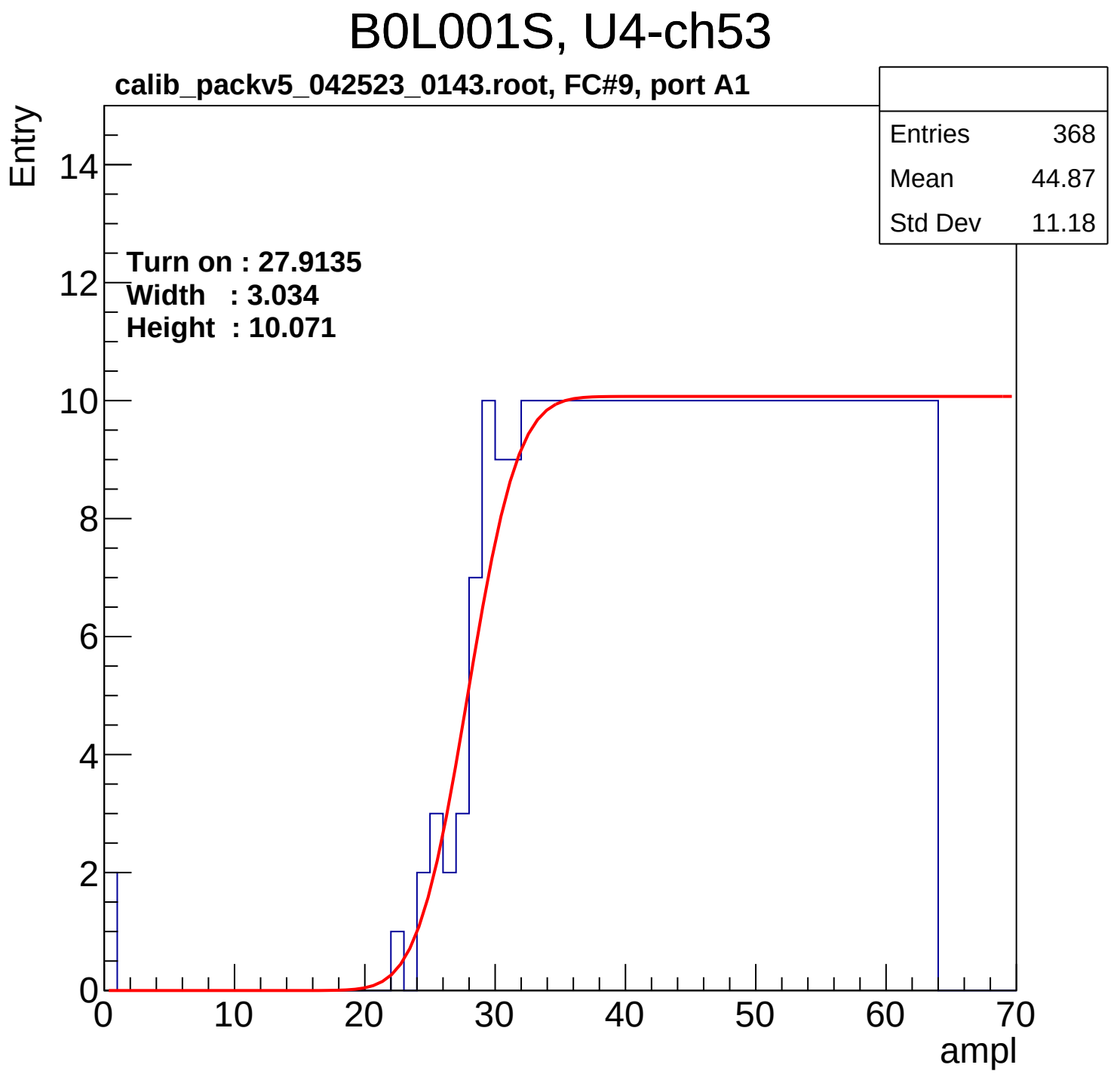
B0L001S, U4-ch53
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.87
Std Dev 11.18
Turn on : 27.9135
Width : 3.034
Height : 10.071
Entry
ampl
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10
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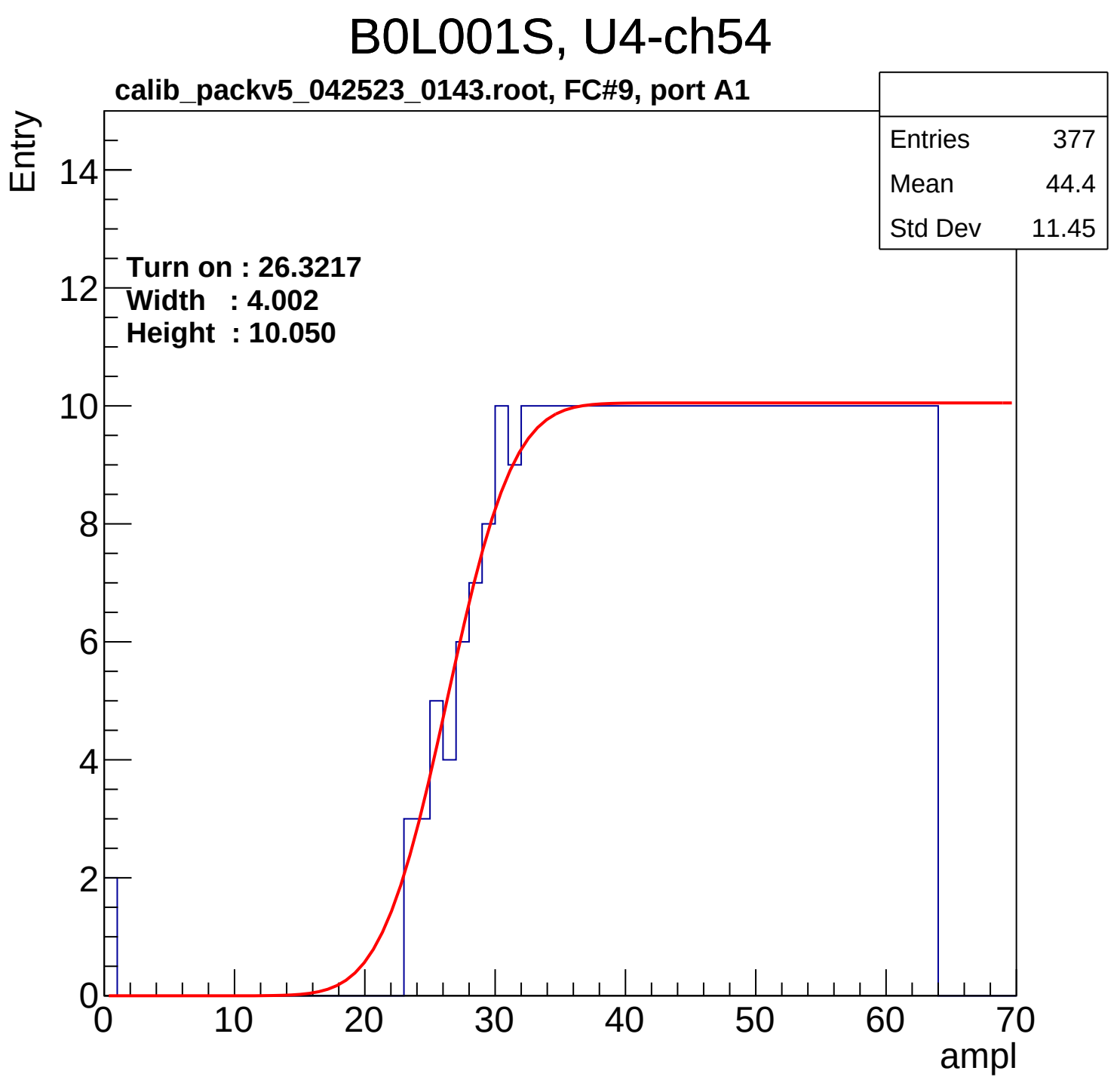
B0L001S, U4-ch54
calib_packv5_042523_0143.root, FC#9, port A1
Entries 377
Mean 44.4
Std Dev 11.45
Turn on : 26.3217
Width : 4.002
Height : 10.050
Entry
ampl
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4
6
8
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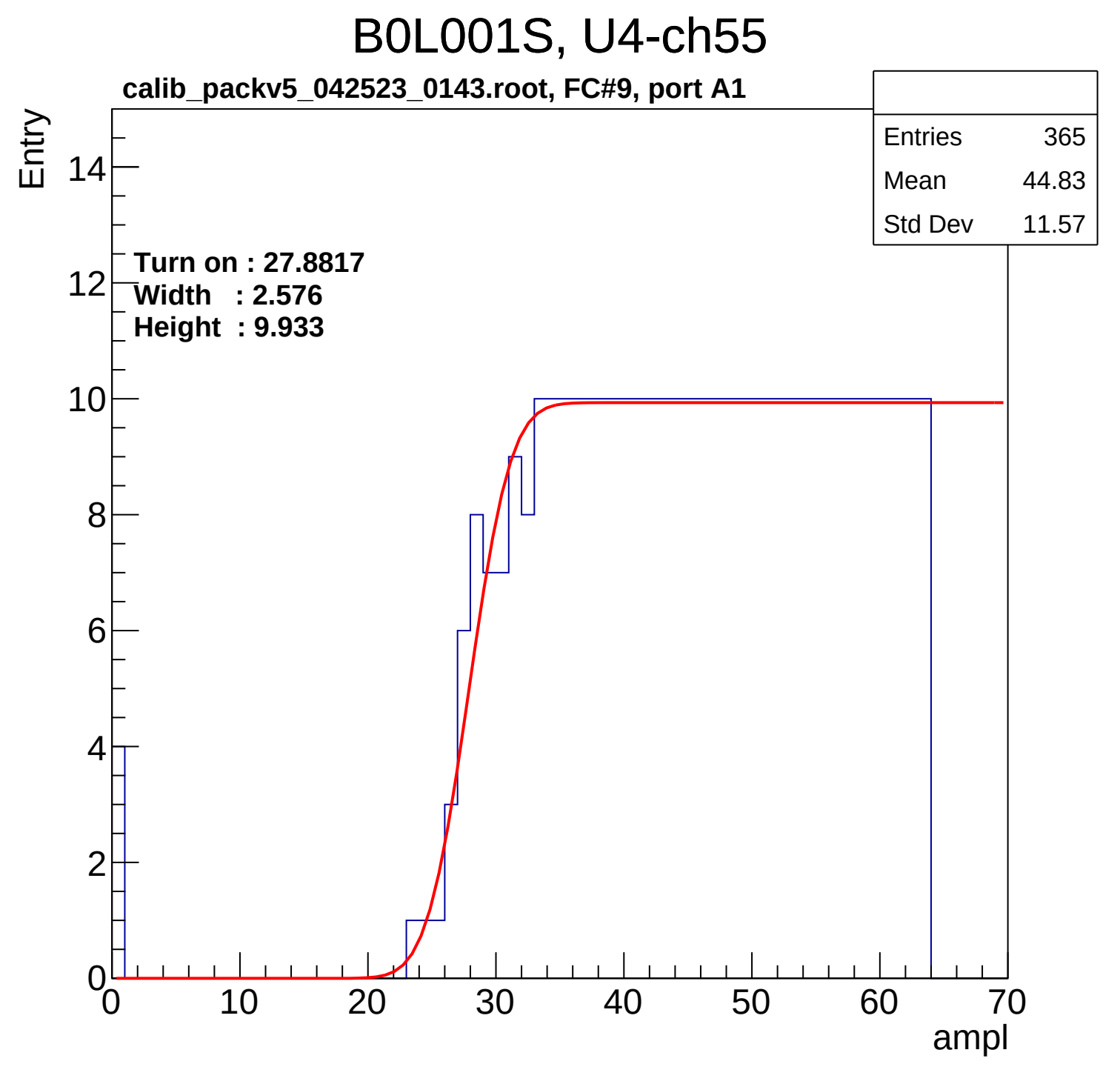
B0L001S, U4-ch55
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 44.83
Std Dev 11.57
Turn on : 27.8817
Width : 2.576
Height : 9.933
Entry
ampl
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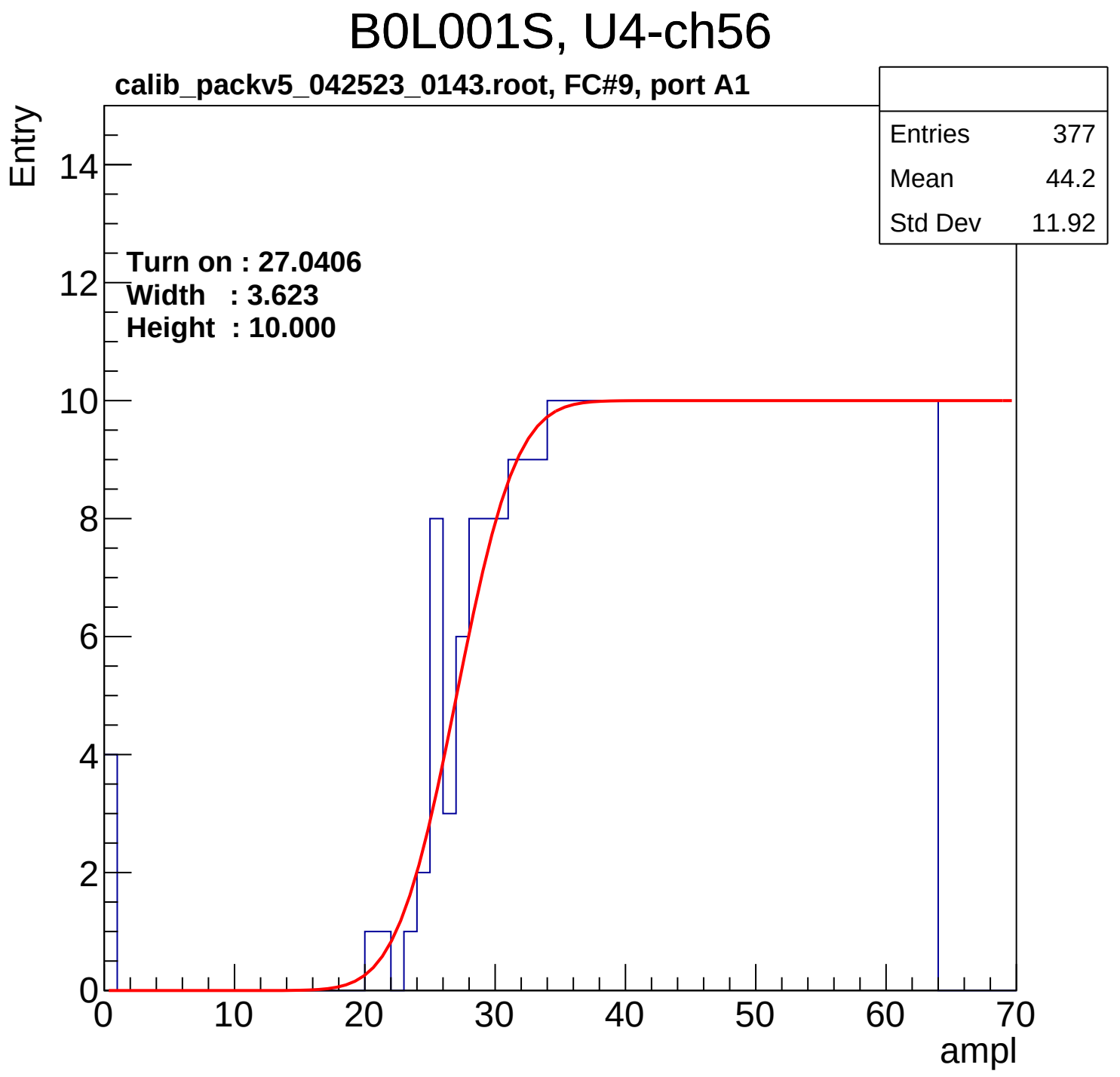
B0L001S, U4-ch56
calib_packv5_042523_0143.root, FC#9, port A1
Entries 377
Mean 44.2
Std Dev 11.92
Turn on : 27.0406
Width : 3.623
Height : 10.000
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ampl
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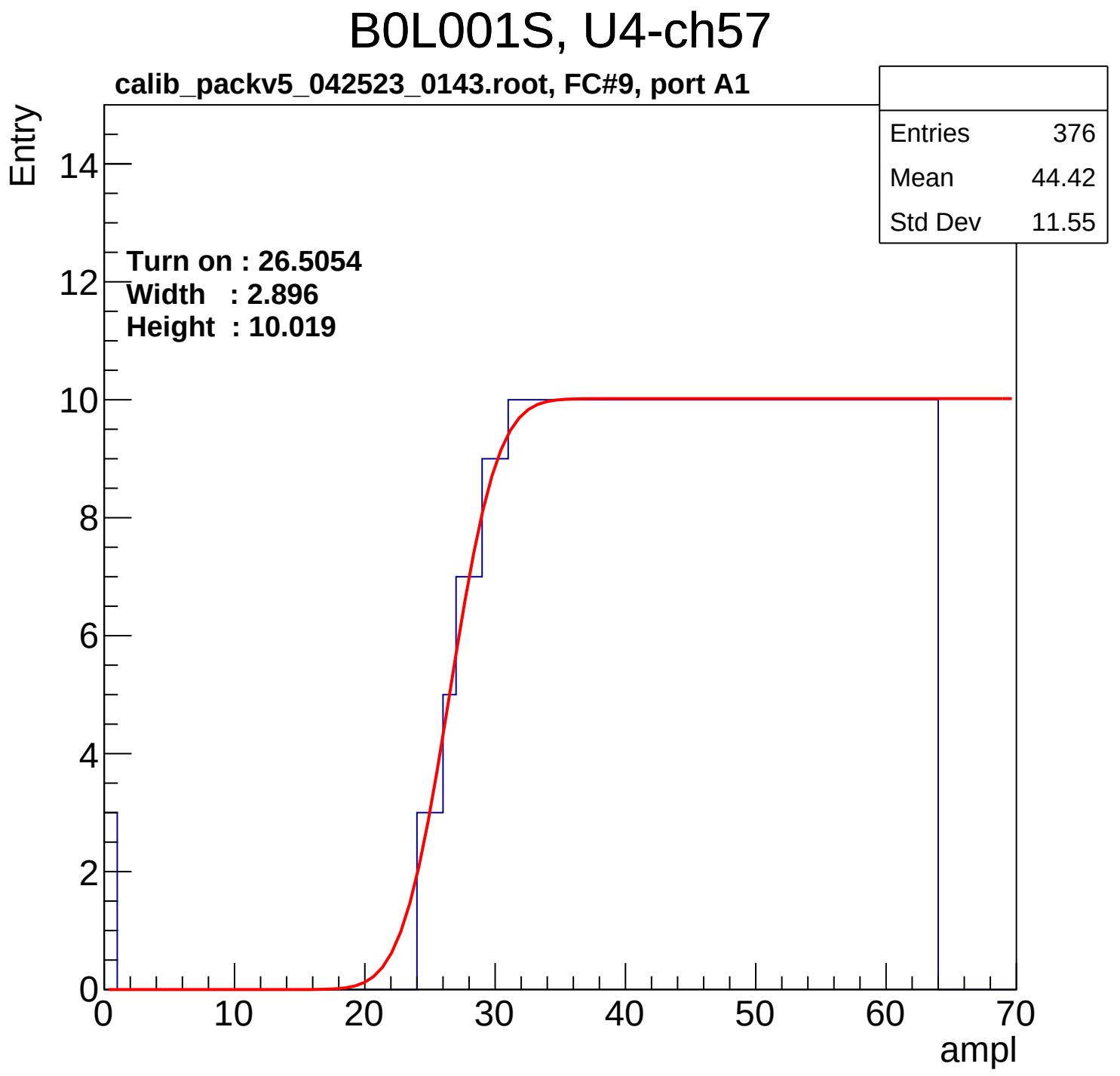
B0L001S, U4-ch57
calib_packv5_042523_0143.root, FC#9, port A1
Entries 376
Mean 44.42
Std Dev 11.55
Turn on : 26.5054
Width : 2.896
Height : 10.019
Entry
ampl
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2
4
6
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12
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20
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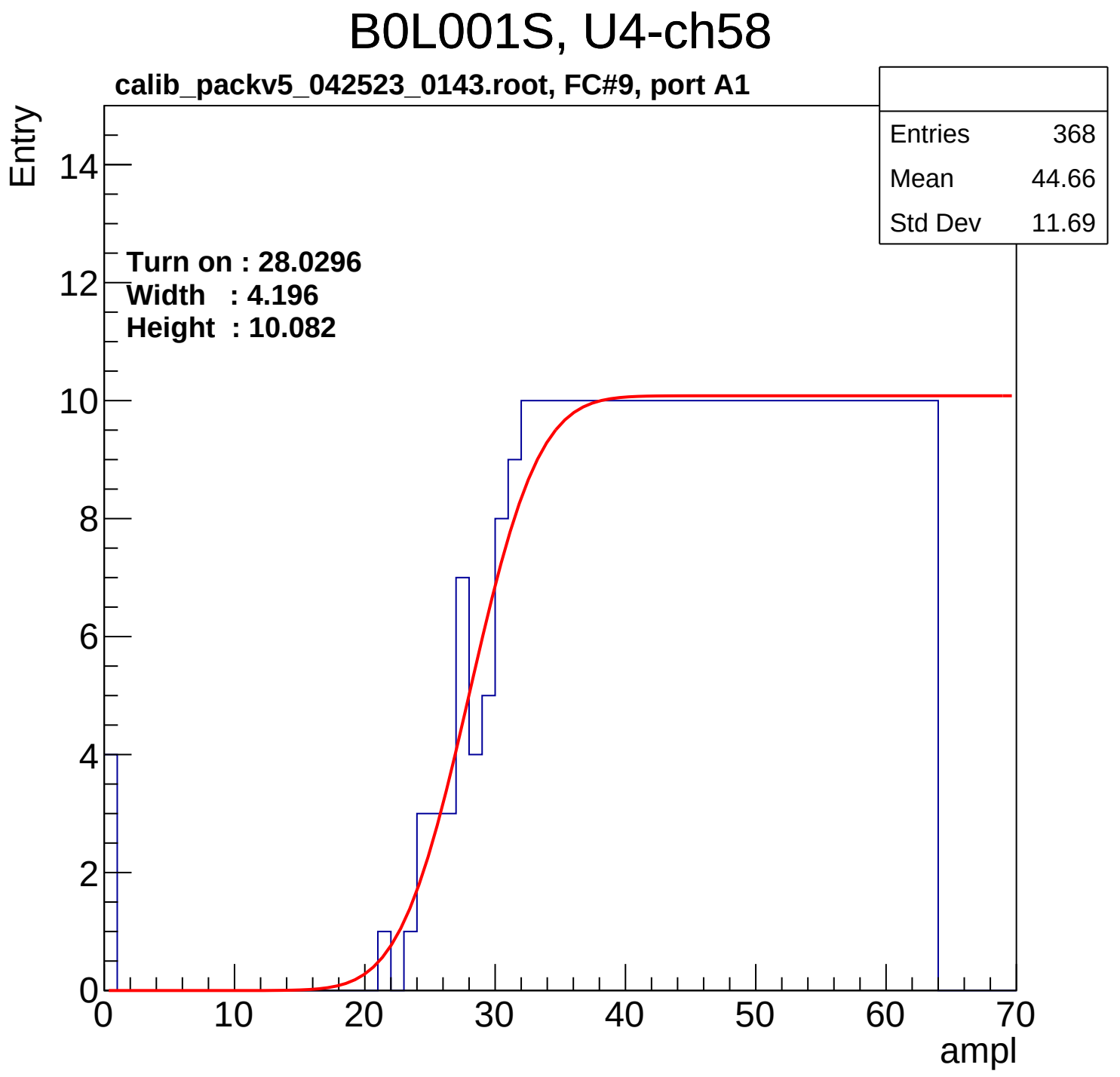
B0L001S, U4-ch58
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.66
Std Dev 11.69
Turn on : 28.0296
Width : 4.196
Height : 10.082
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ampl
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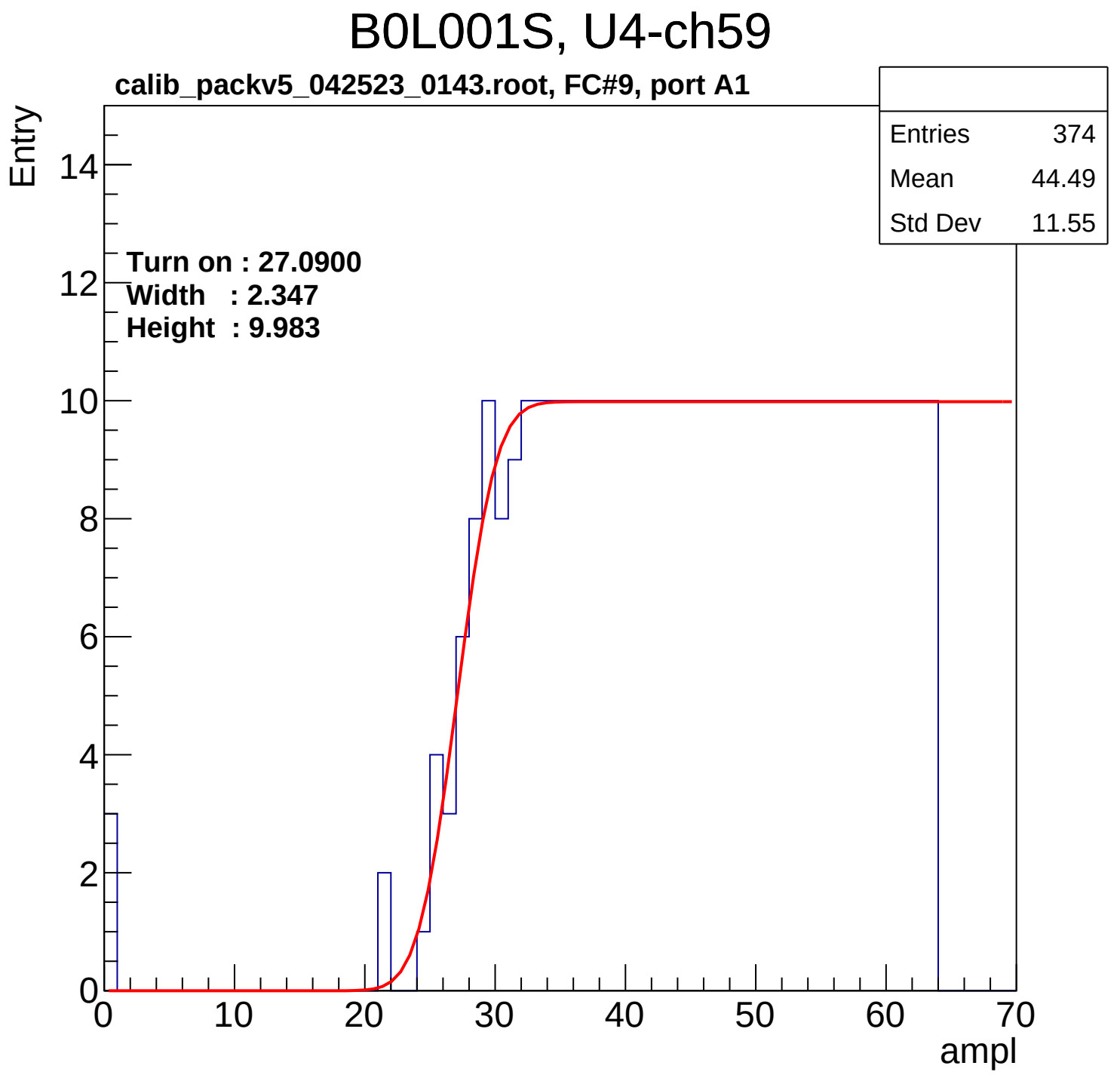
B0L001S, U4-ch59
calib_packv5_042523_0143.root, FC#9, port A1
Entries 374
Mean 44.49
Std Dev 11.55
Turn on : 27.0900
Width : 2.347
Height : 9.983
Entry
ampl
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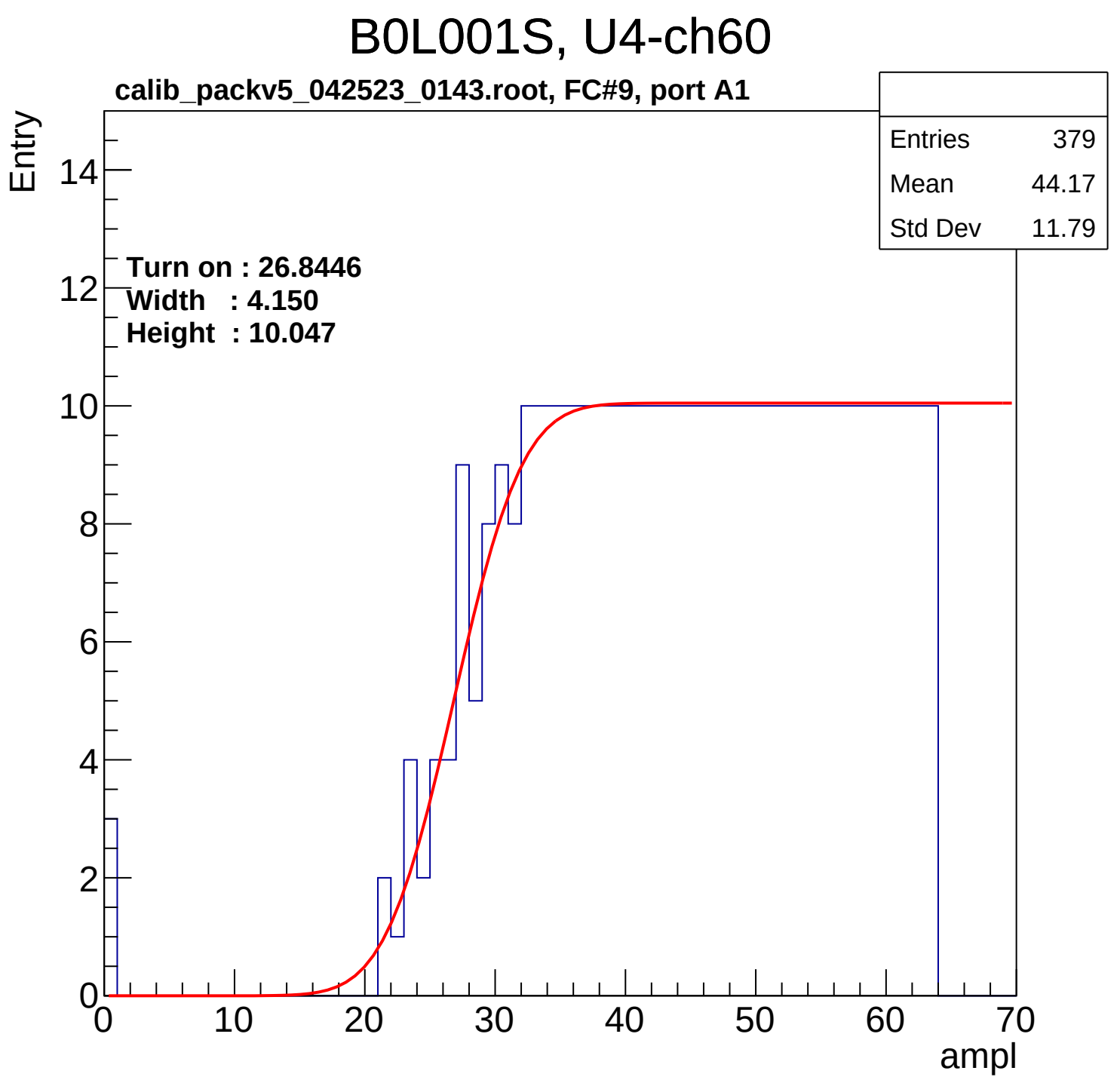
B0L001S, U4-ch60
calib_packv5_042523_0143.root, FC#9, port A1
Entries 379
Mean 44.17
Std Dev 11.79
Turn on : 26.8446
Width : 4.150
Height : 10.047
Entry
ampl
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2
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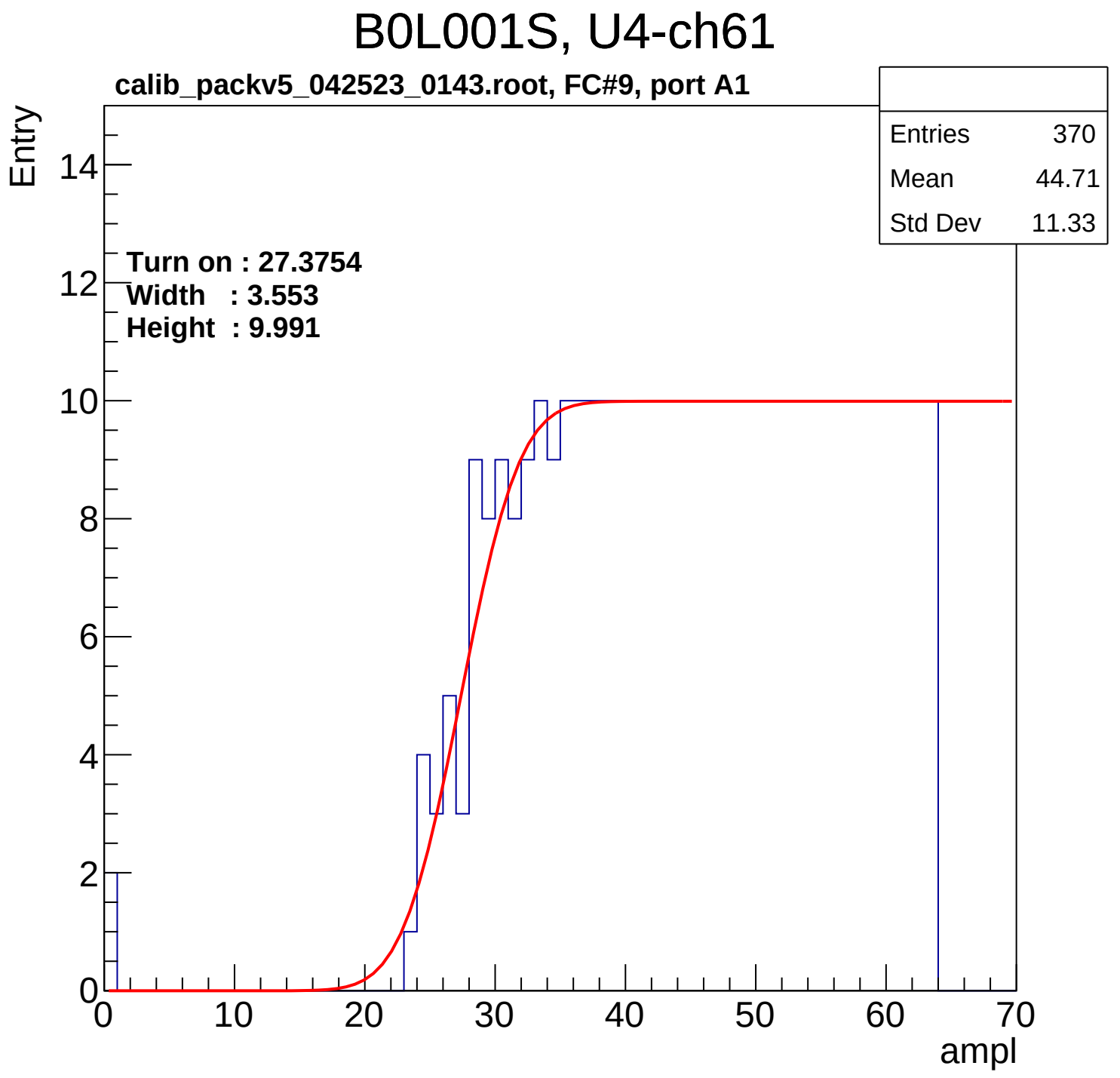
B0L001S, U4-ch61
calib_packv5_042523_0143.root, FC#9, port A1
Entries 370
Mean 44.71
Std Dev 11.33
Turn on : 27.3754
Width : 3.553
Height : 9.991
Entry
ampl
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2
4
6
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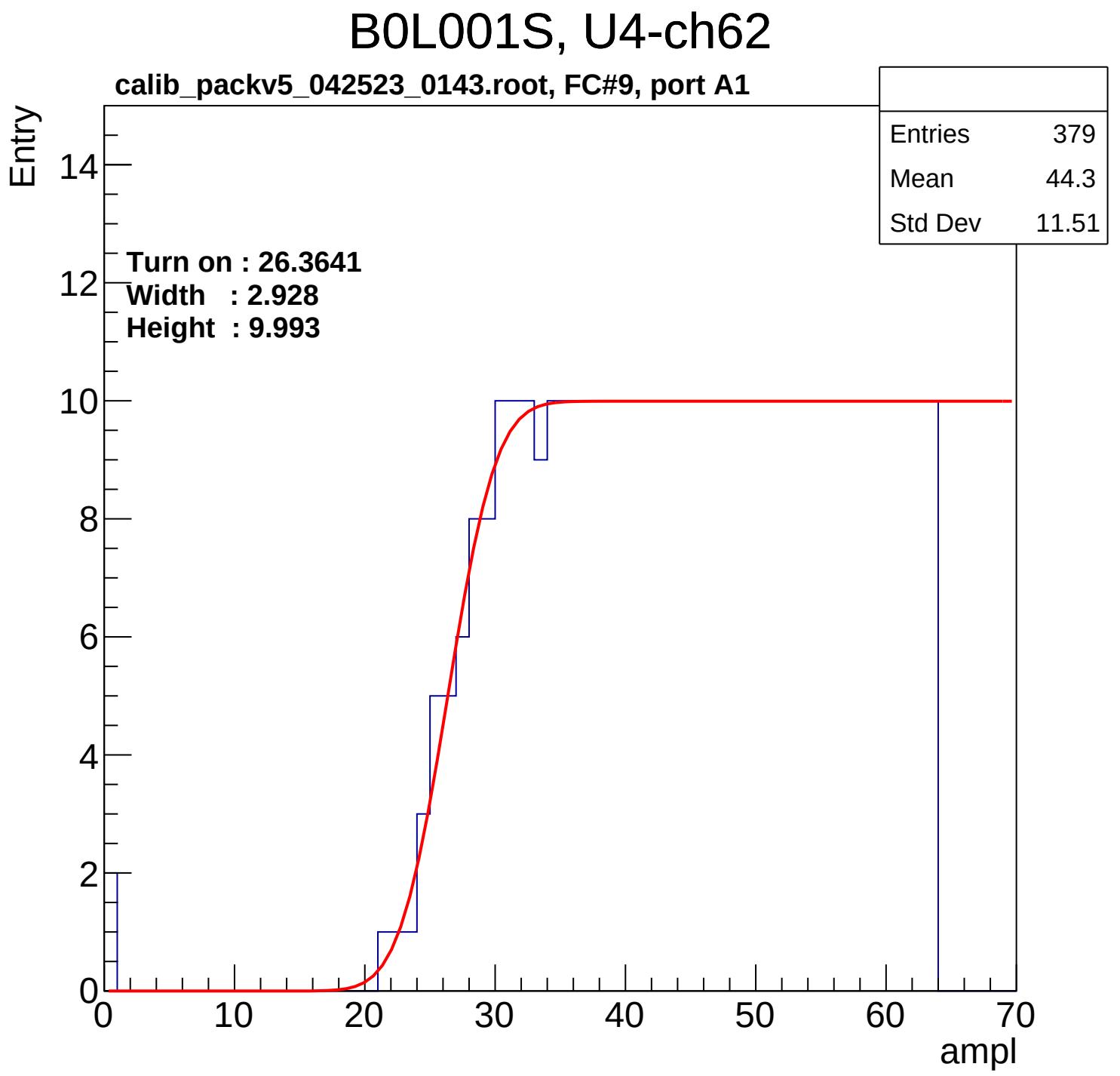
B0L001S, U4-ch62
calib_packv5_042523_0143.root, FC#9, port A1
Entries 379
Mean 44.3
Std Dev 11.51
Turn on : 26.3641
Width : 2.928
Height : 9.993
Entry
ampl
0
2
4
6
8
10
12
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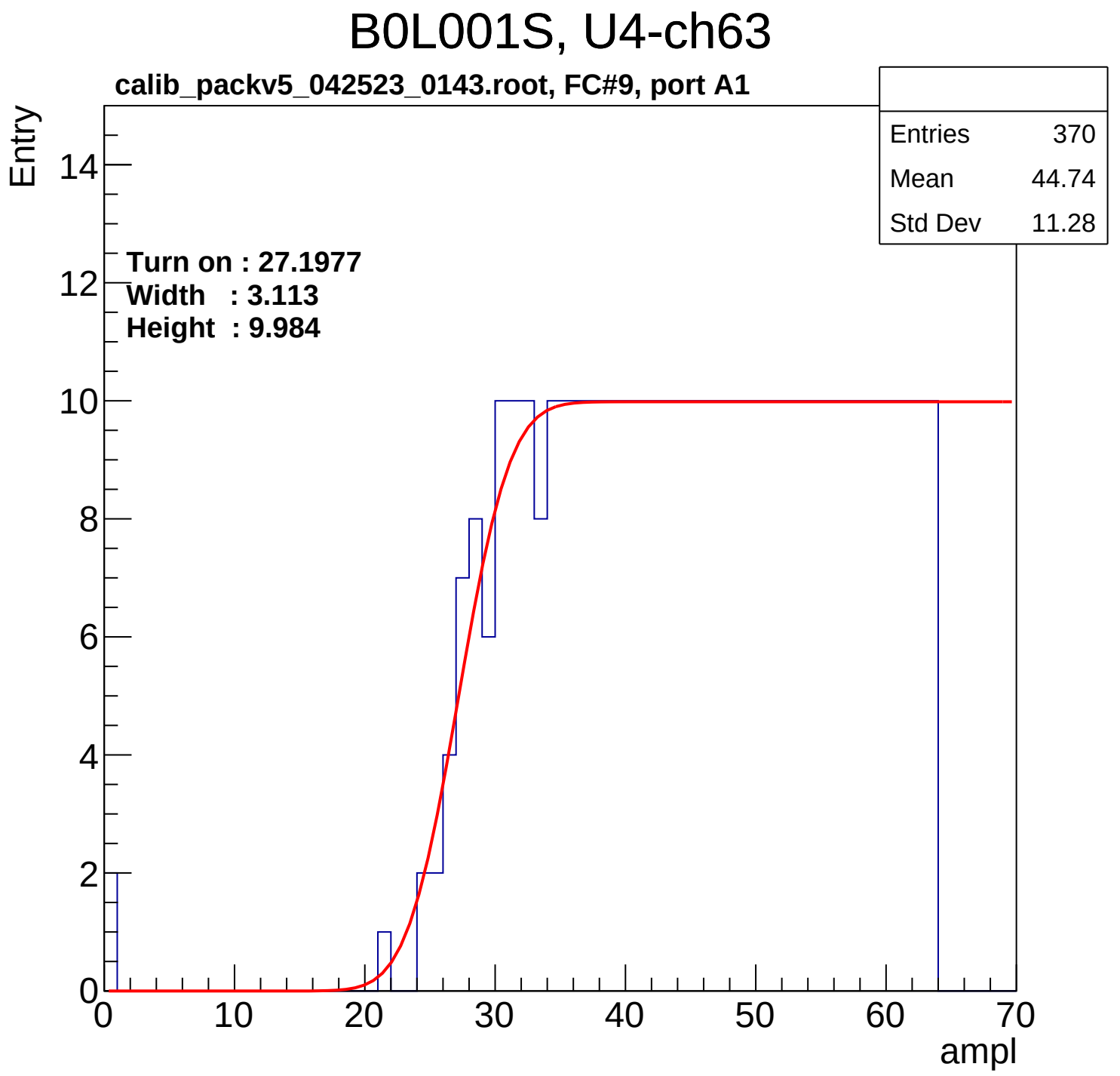
B0L001S, U4-ch63
calib_packv5_042523_0143.root, FC#9, port A1
Entries 370
Mean 44.74
Std Dev 11.28
Turn on : 27.1977
Width : 3.113
Height : 9.984
Entry
ampl
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6
8
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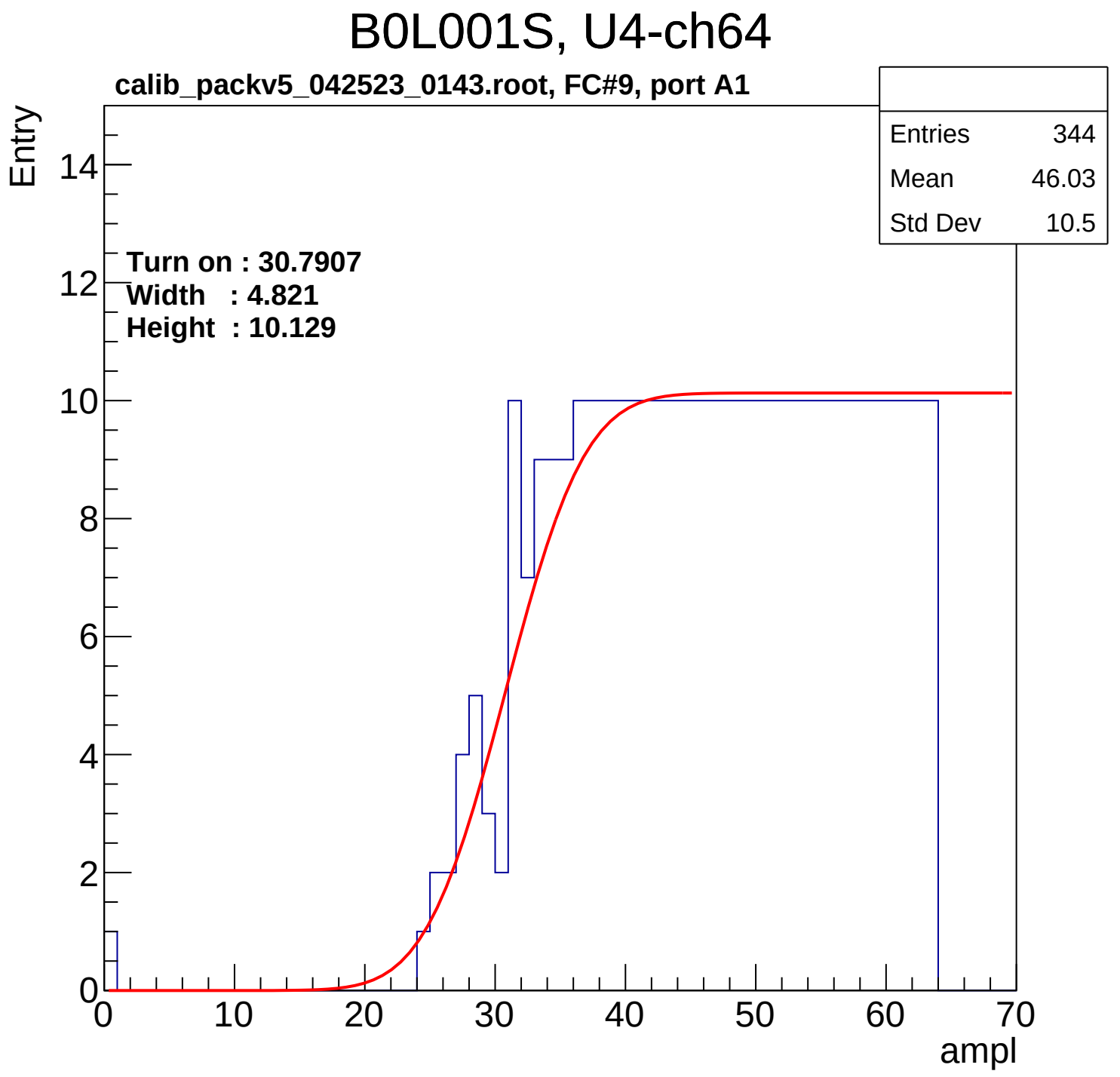
B0L001S, U4-ch64
calib_packv5_042523_0143.root, FC#9, port A1
Entries 344
Mean 46.03
Std Dev 10.5
Turn on : 30.7907
Width : 4.821
Height : 10.129
Entry
ampl
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2
4
6
8
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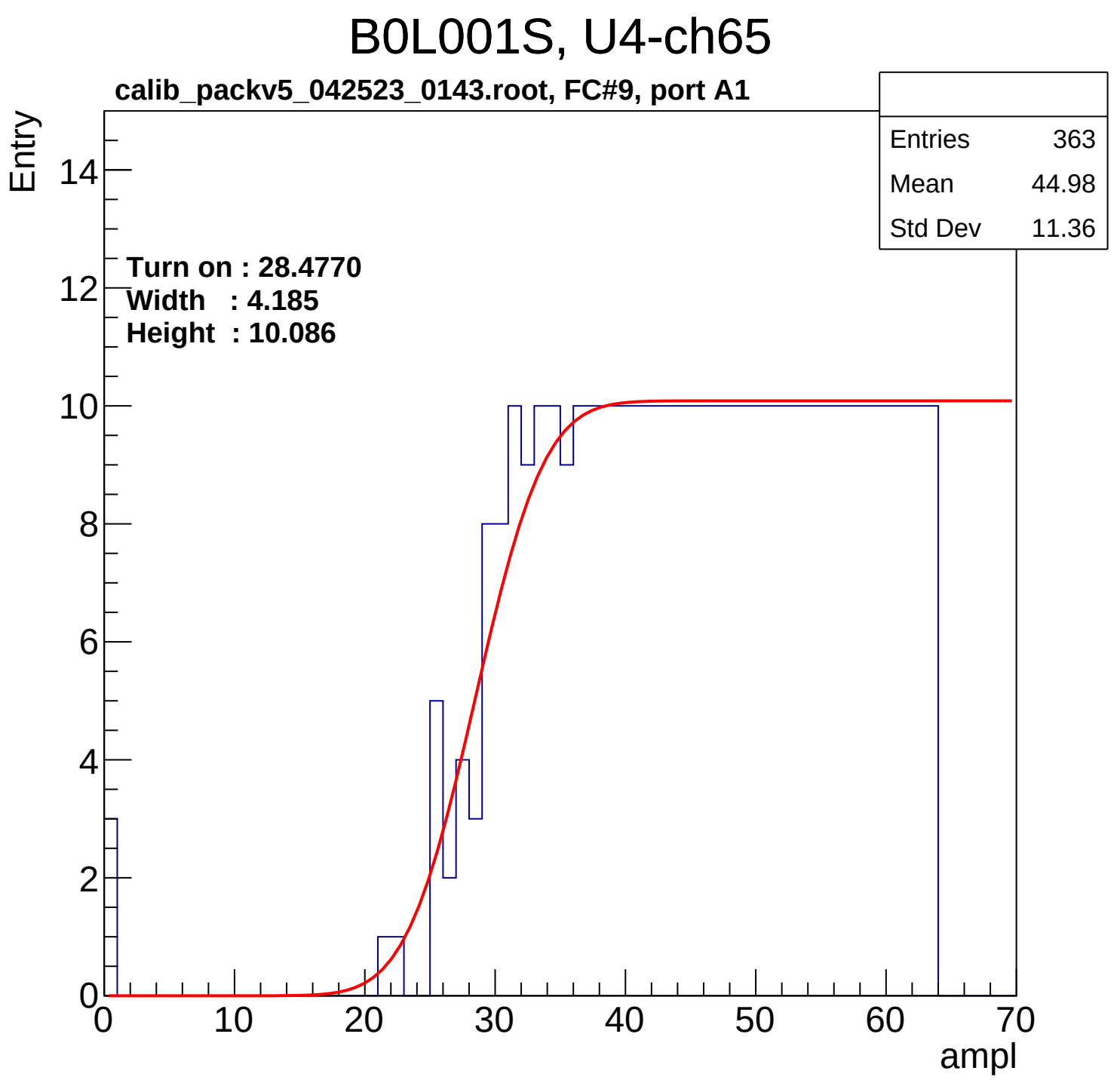
B0L001S, U4-ch65
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 44.98
Std Dev 11.36
Turn on : 28.4770
Width : 4.185
Height : 10.086
Entry
ampl
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2
4
6
8
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12
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40
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60
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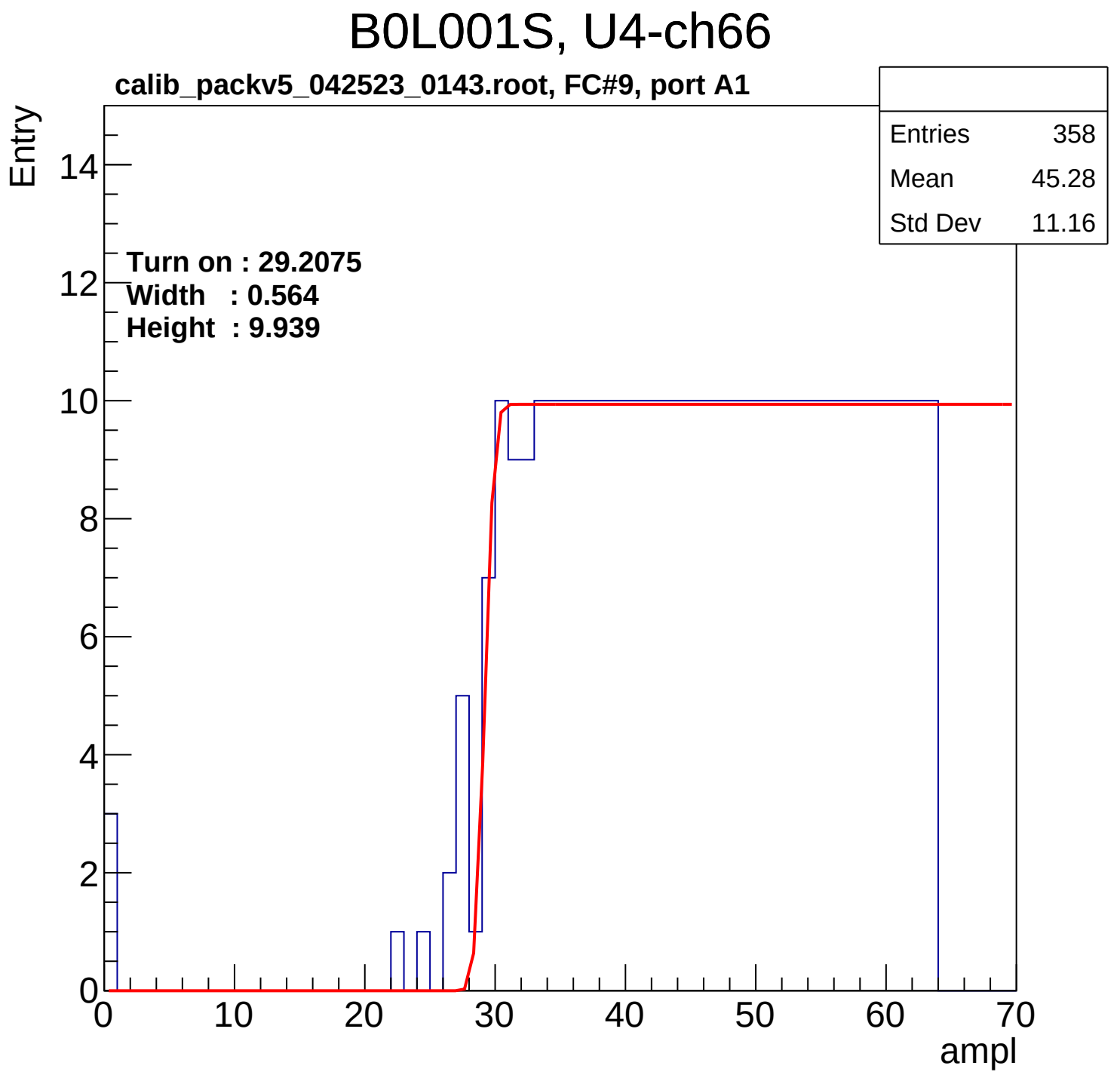
B0L001S, U4-ch66
calib_packv5_042523_0143.root, FC#9, port A1
Entries 358
Mean 45.28
Std Dev 11.16
Turn on : 29.2075
Width : 0.564
Height : 9.939
Entry
ampl
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2
4
6
8
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12
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0
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60
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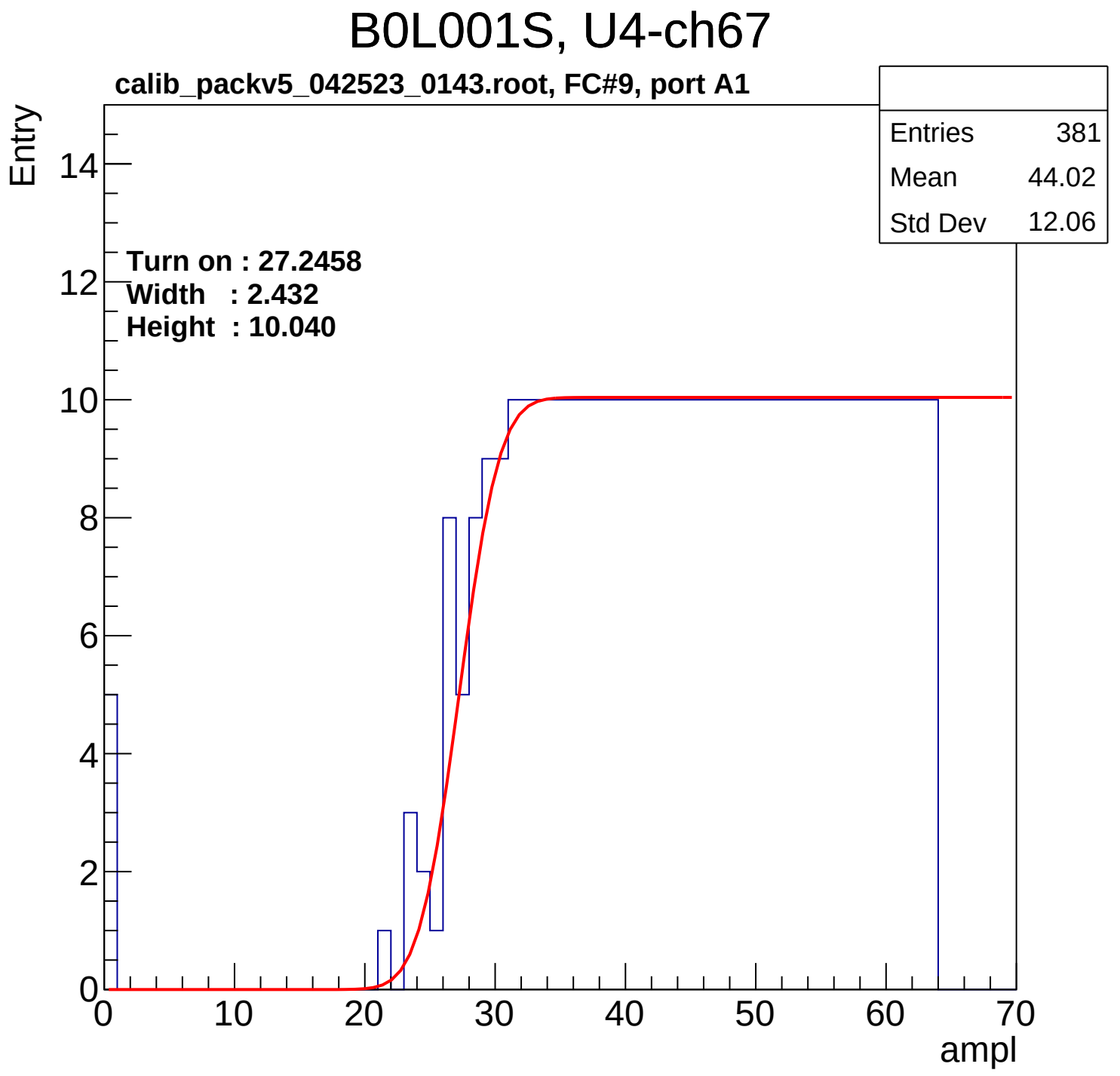
B0L001S, U4-ch67
calib_packv5_042523_0143.root, FC#9, port A1
Entries 381
Mean 44.02
Std Dev 12.06
Turn on : 27.2458
Width : 2.432
Height : 10.040
Entry
ampl
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2
4
6
8
10
12
14
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20
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60
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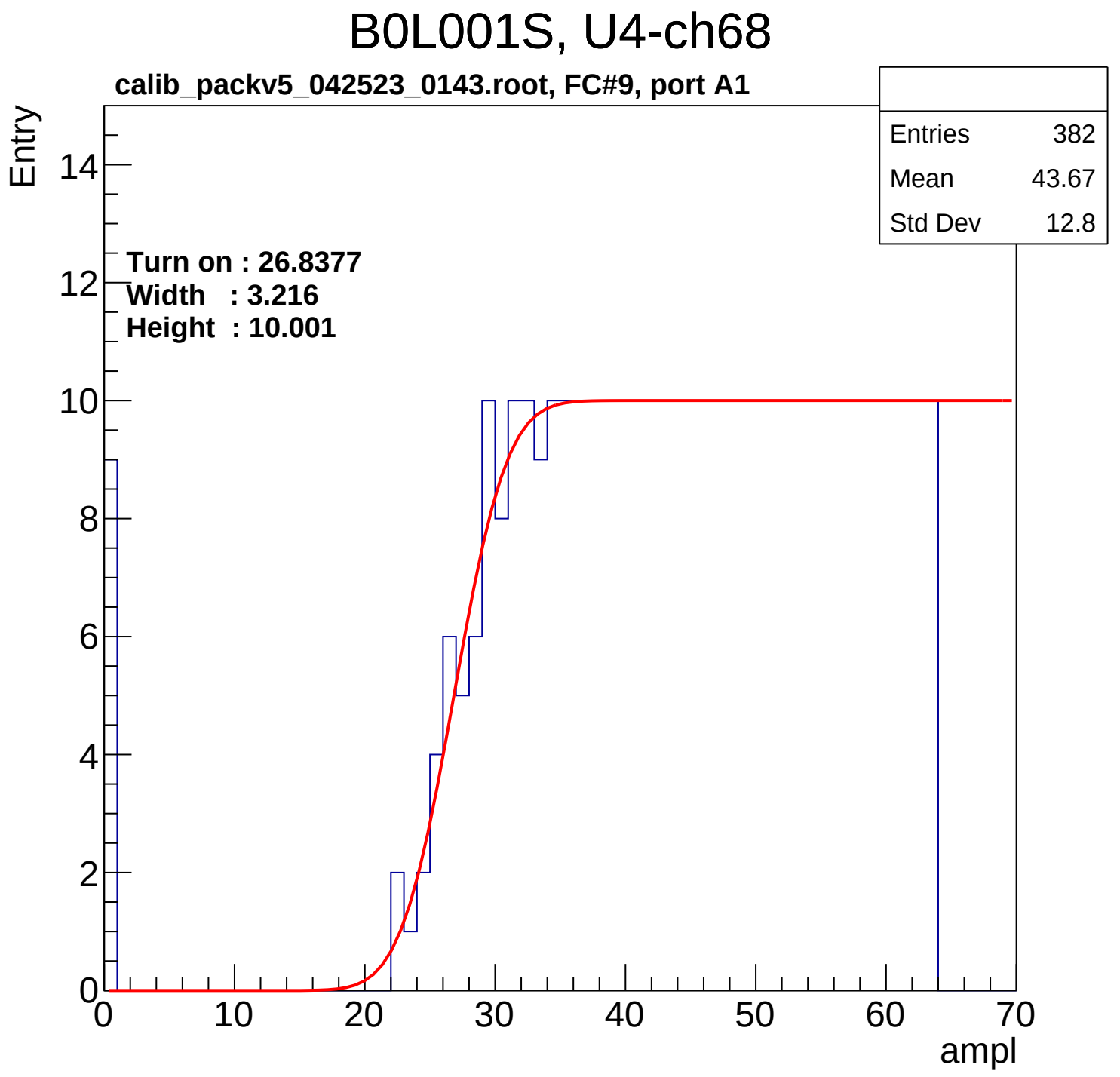
B0L001S, U4-ch68
calib_packv5_042523_0143.root, FC#9, port A1
Entries 382
Mean 43.67
Std Dev 12.8
Turn on : 26.8377
Width : 3.216
Height : 10.001
Entry
ampl
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6
8
10
12
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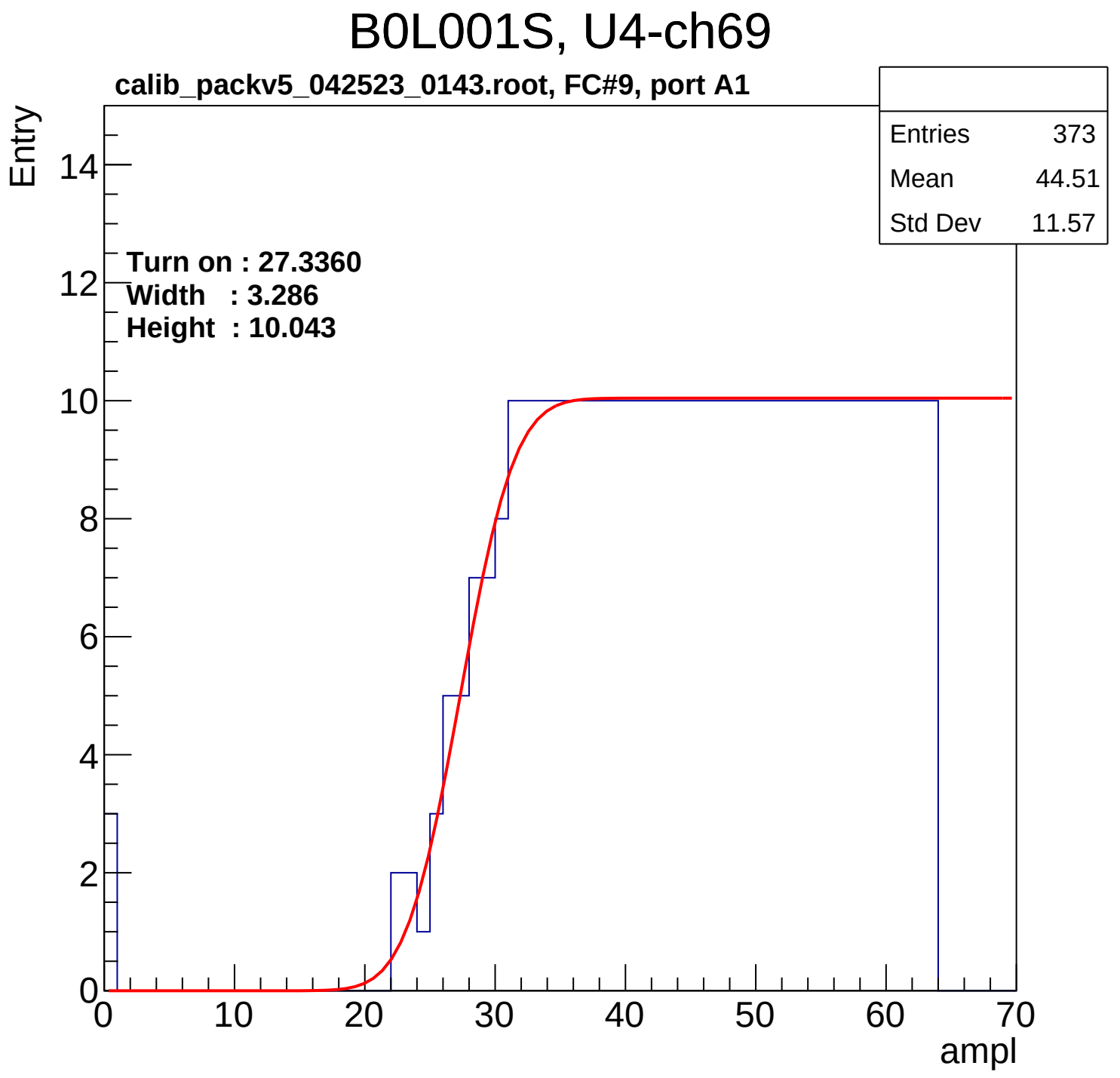
B0L001S, U4-ch69
calib_packv5_042523_0143.root, FC#9, port A1
Entries 373
Mean 44.51
Std Dev 11.57
Turn on : 27.3360
Width : 3.286
Height : 10.043
Entry
ampl
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6
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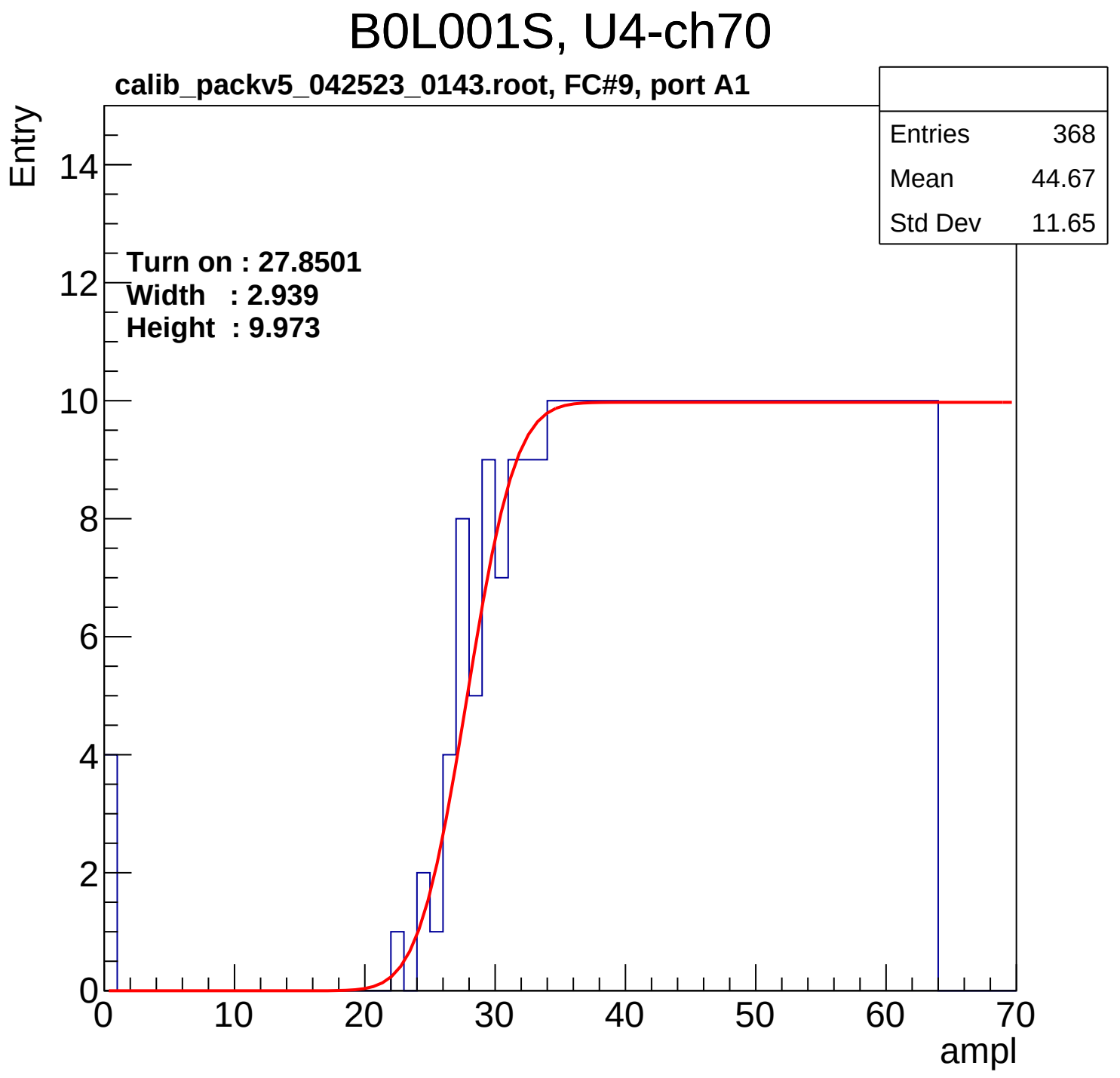
B0L001S, U4-ch70
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.67
Std Dev 11.65
Turn on : 27.8501
Width : 2.939
Height : 9.973
Entry
ampl
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6
8
10
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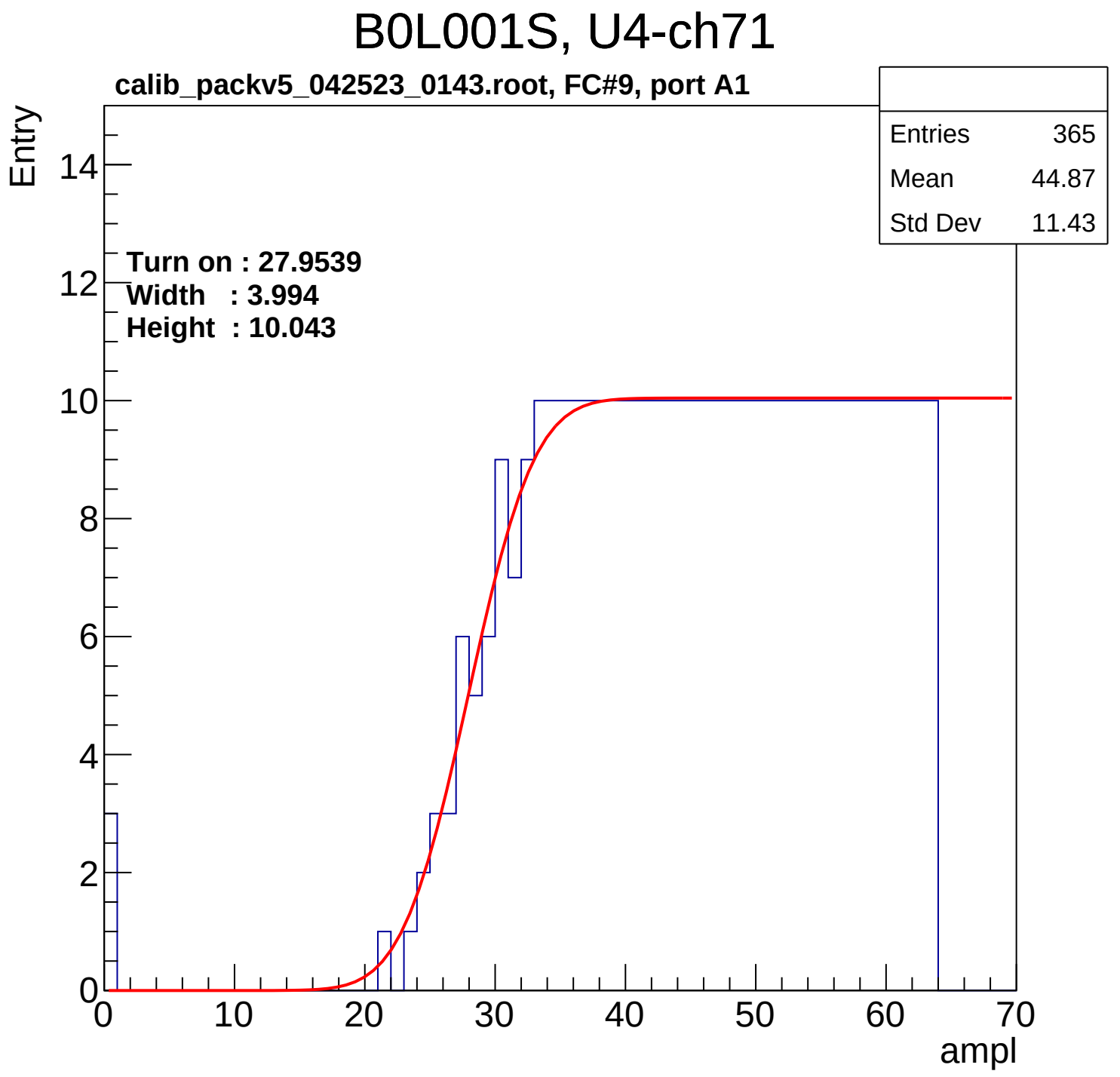
B0L001S, U4-ch71
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 44.87
Std Dev 11.43
Turn on : 27.9539
Width : 3.994
Height : 10.043
Entry
ampl
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6
8
10
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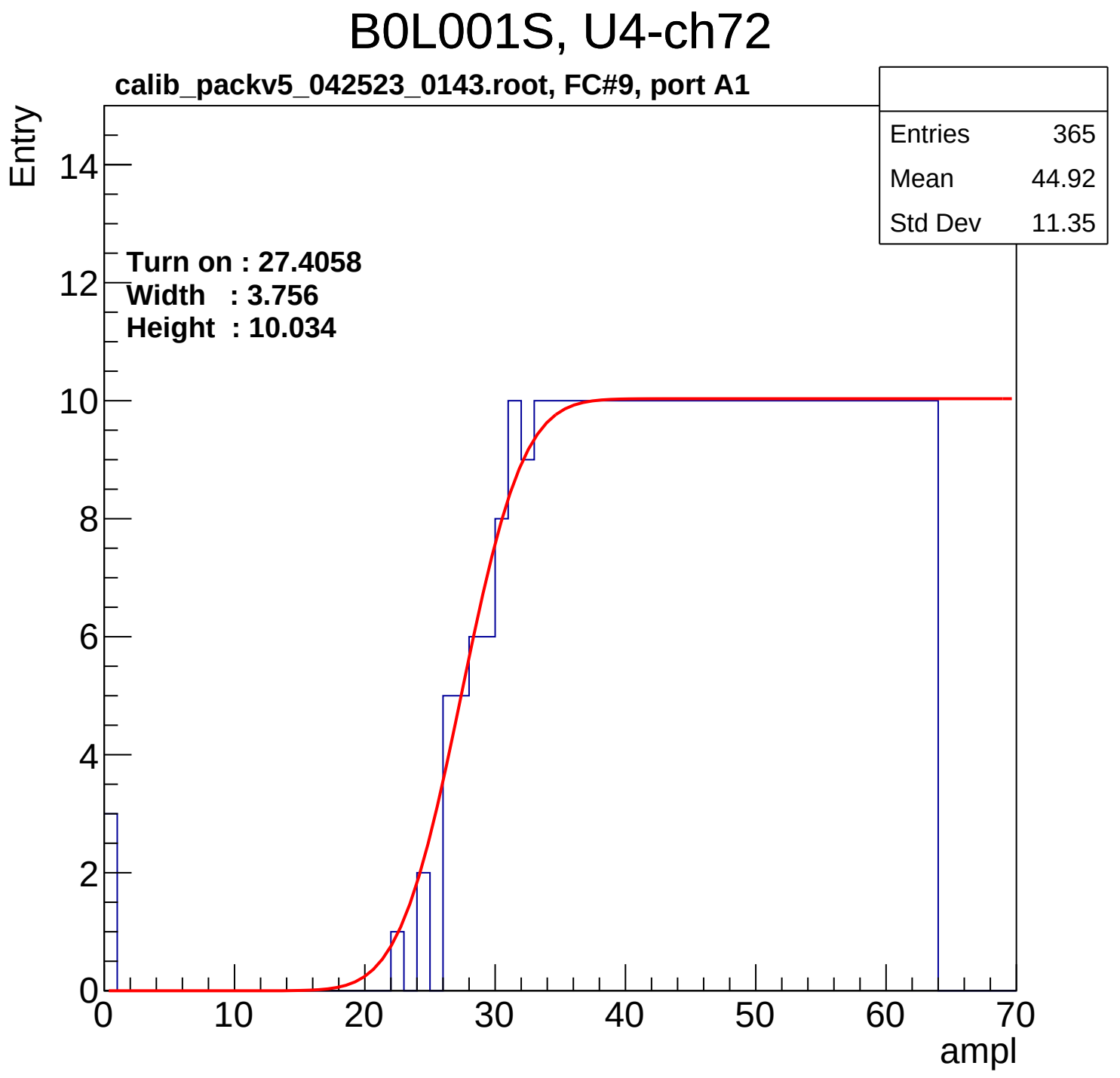
B0L001S, U4-ch72
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 44.92
Std Dev 11.35
Turn on : 27.4058
Width : 3.756
Height : 10.034
Entry
ampl
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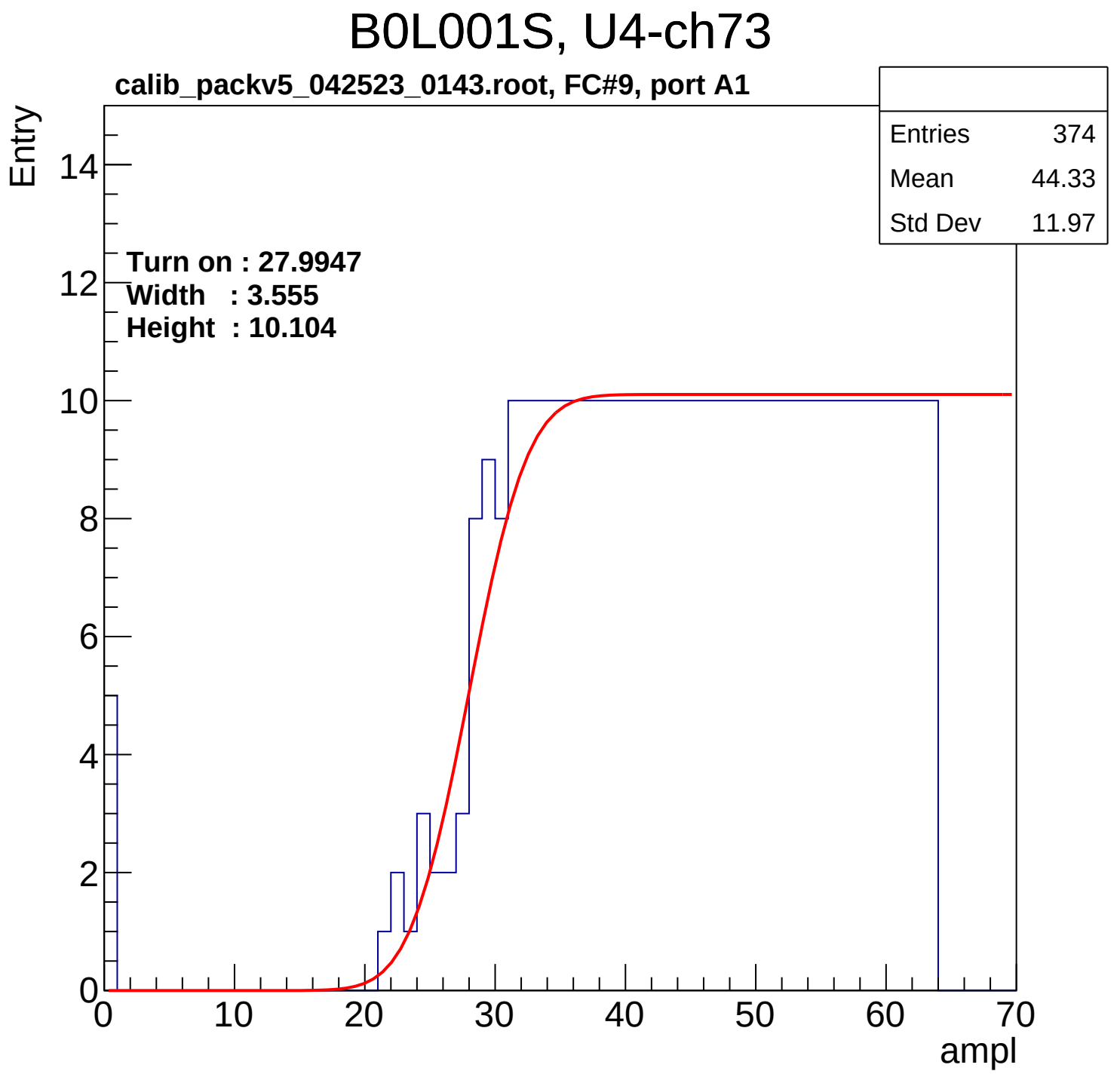
B0L001S, U4-ch73
calib_packv5_042523_0143.root, FC#9, port A1
Entries 374
Mean 44.33
Std Dev 11.97
Turn on : 27.9947
Width : 3.555
Height : 10.104
Entry
ampl
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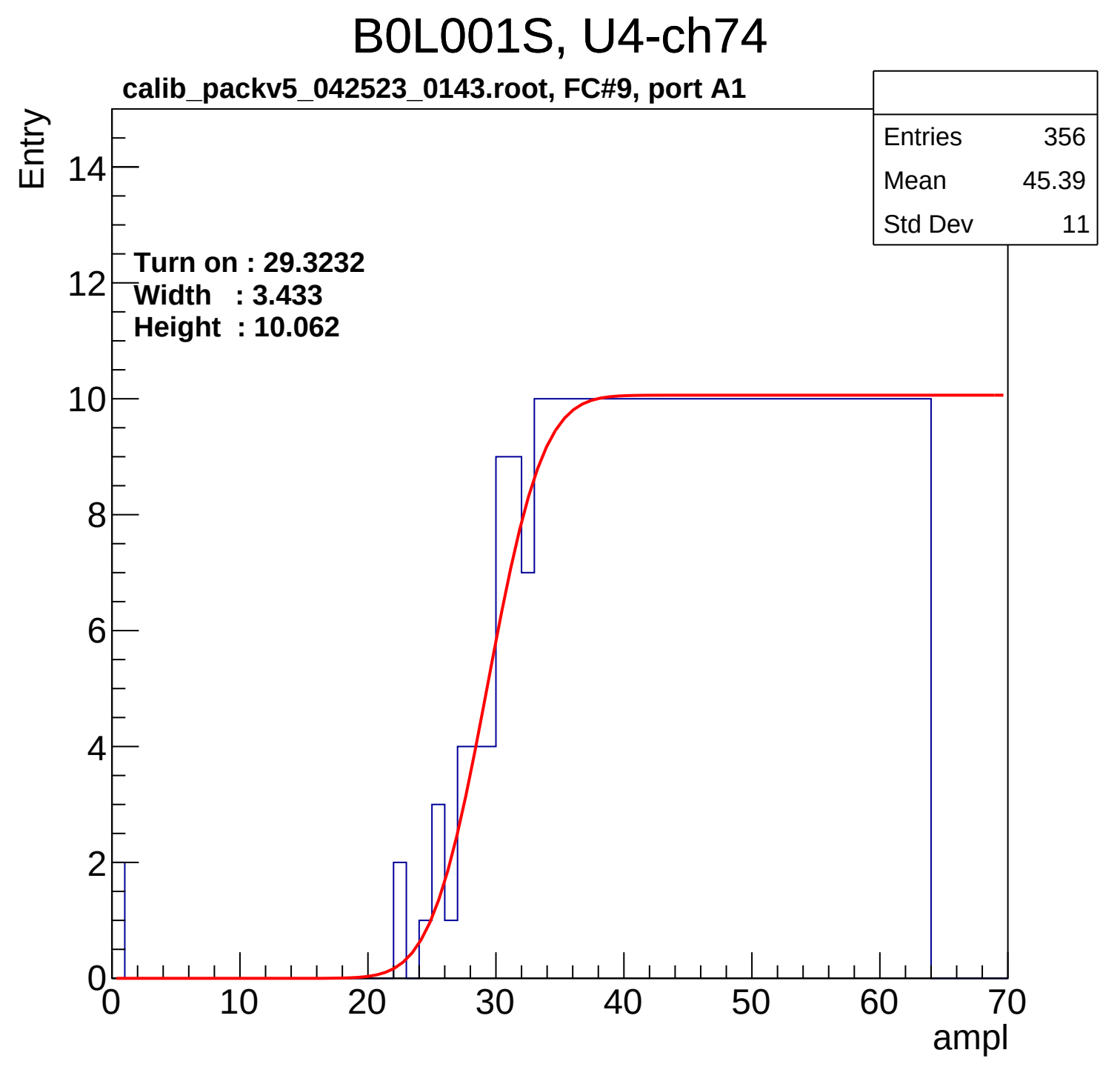
B0L001S, U4-ch74
calib_packv5_042523_0143.root, FC#9, port A1
Entries 356
Mean 45.39
Std Dev 11
Turn on : 29.3232
Width : 3.433
Height : 10.062
Entry
ampl
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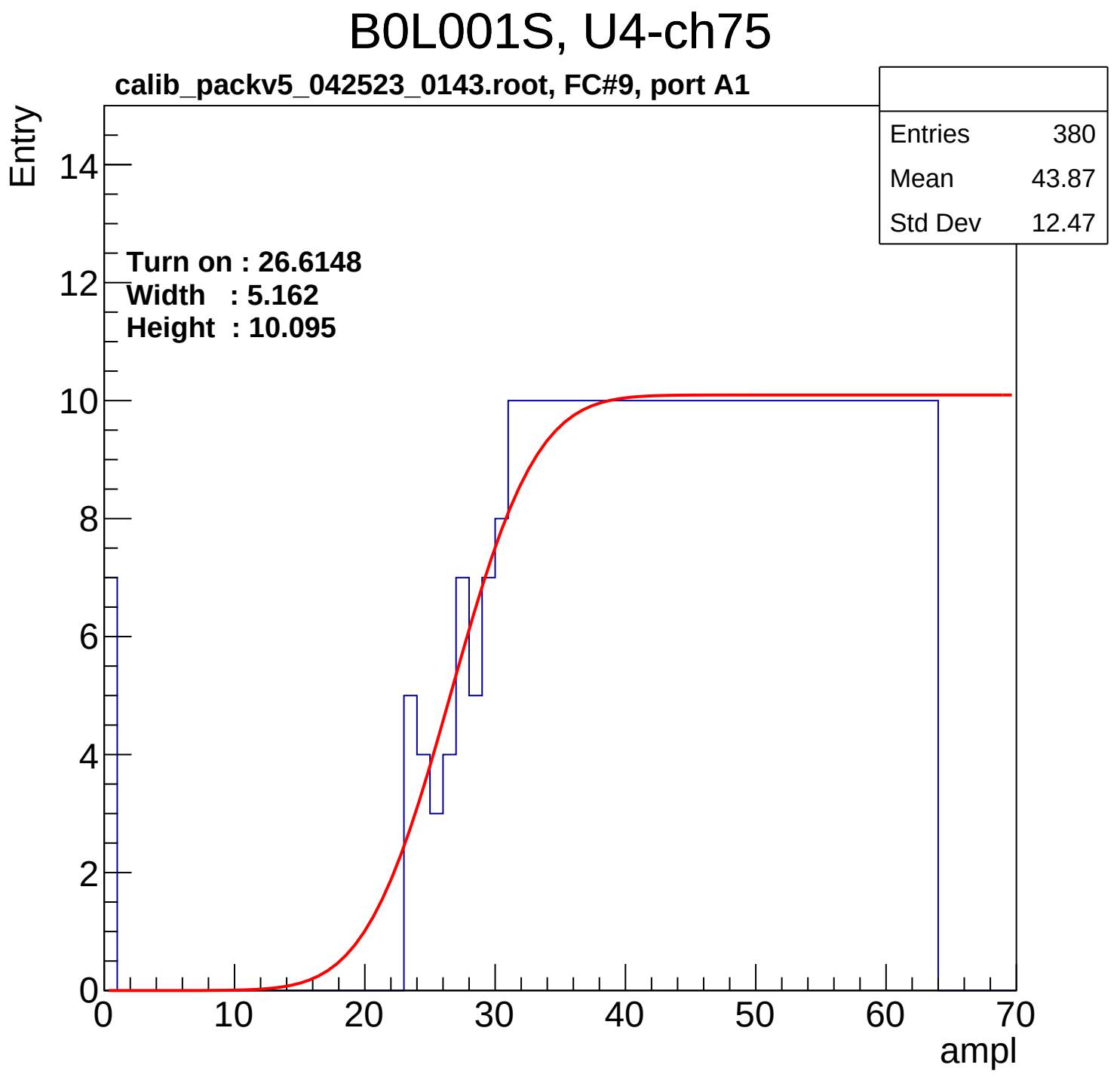
B0L001S, U4-ch75
calib_packv5_042523_0143.root, FC#9, port A1
Entries 380
Mean 43.87
Std Dev 12.47
Turn on : 26.6148
Width : 5.162
Height : 10.095
Entry
ampl
0
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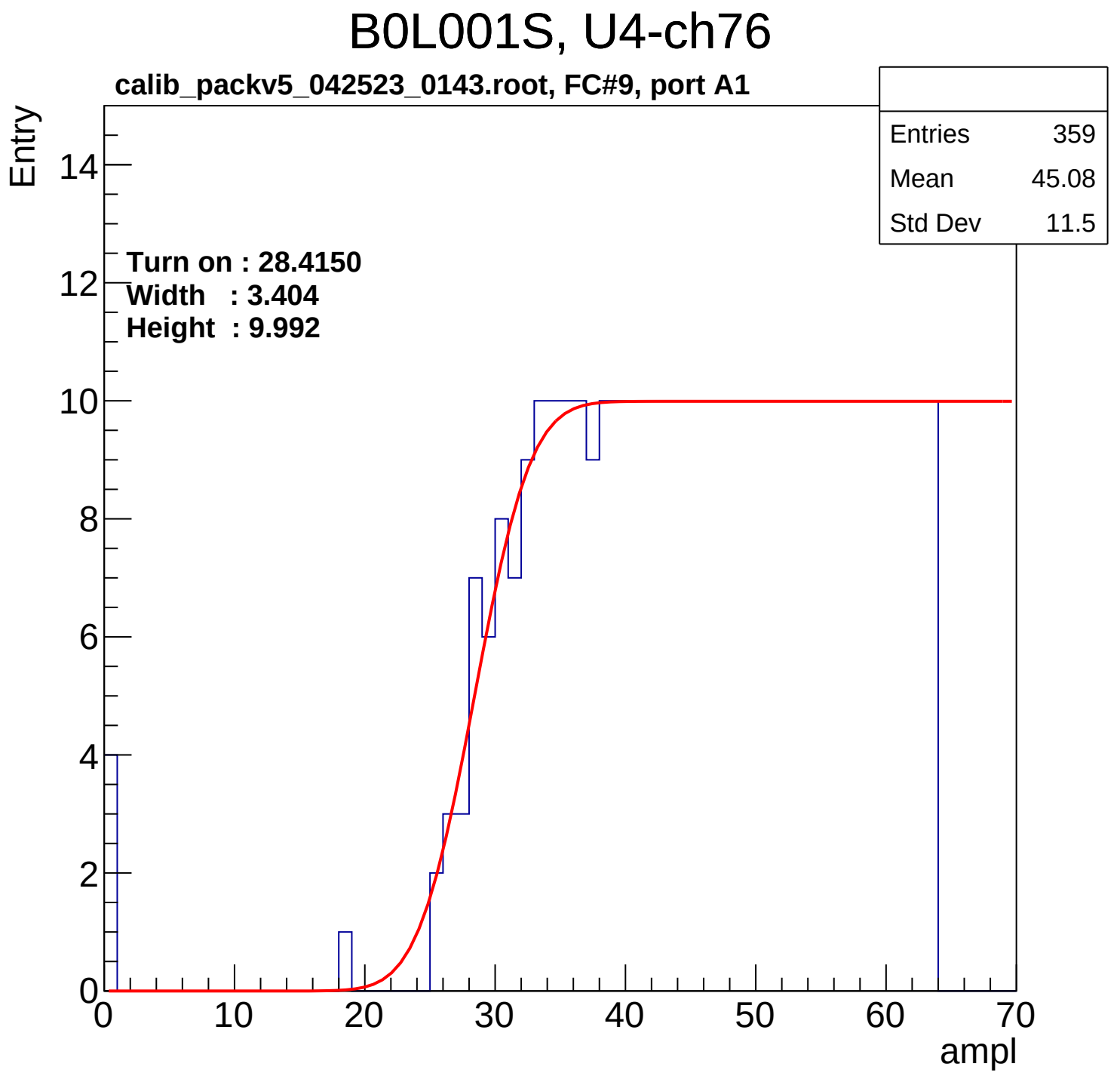
B0L001S, U4-ch76
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 45.08
Std Dev 11.5
Turn on : 28.4150
Width : 3.404
Height : 9.992
Entry
ampl
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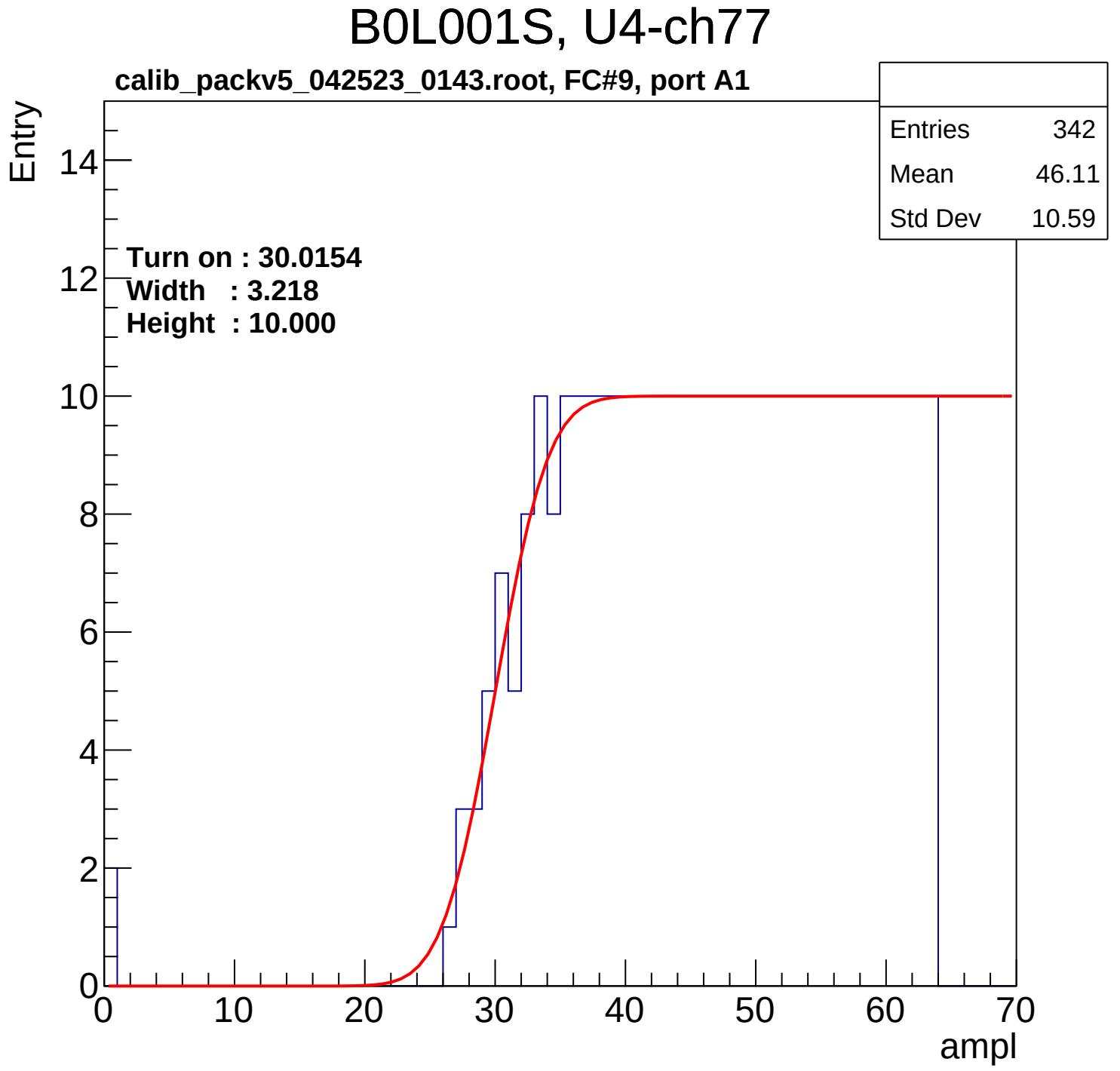
B0L001S, U4-ch77
calib_packv5_042523_0143.root, FC#9, port A1
Entries 342
Mean 46.11
Std Dev 10.59
Turn on : 30.0154
Width : 3.218
Height : 10.000
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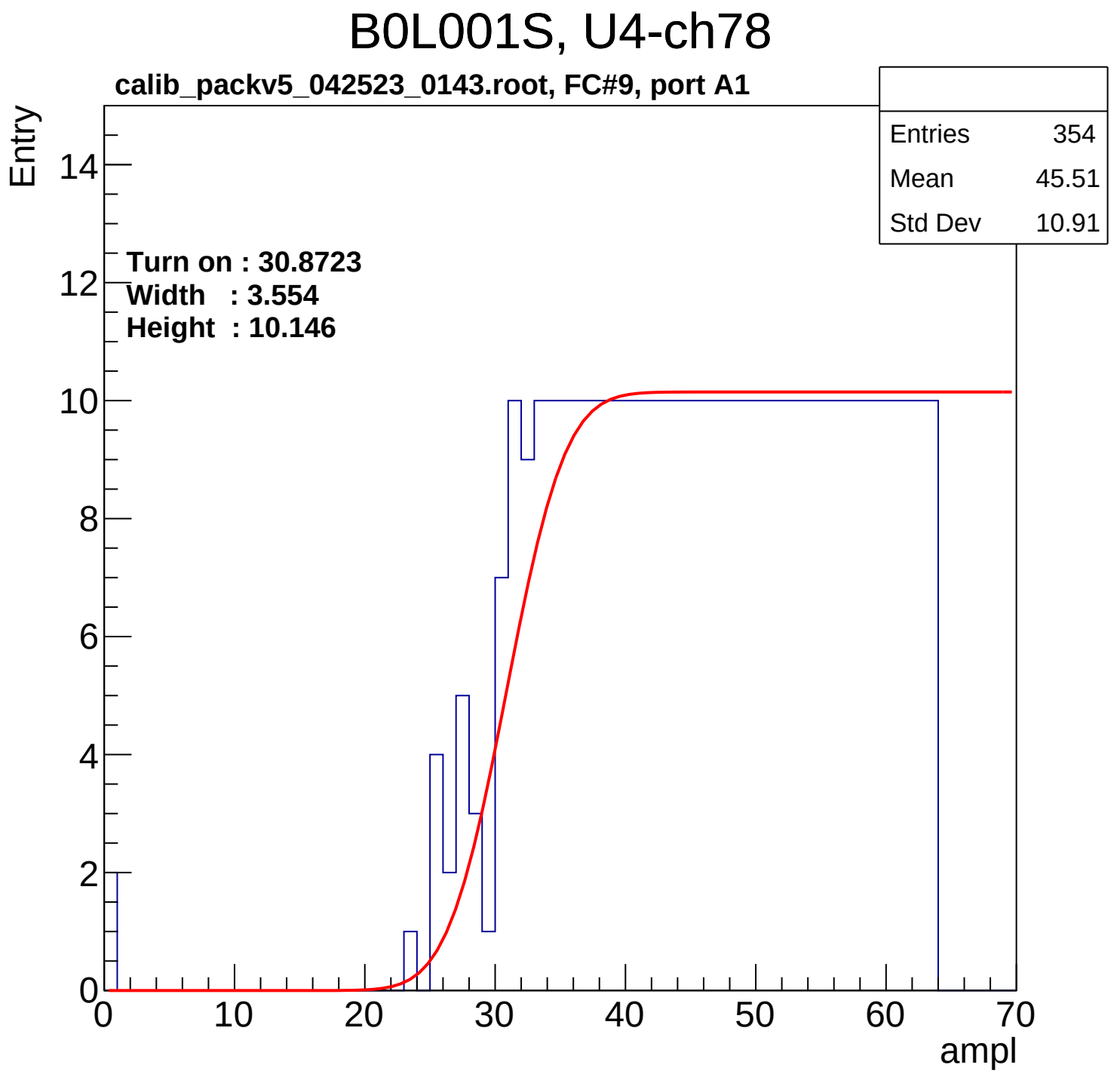
B0L001S, U4-ch78
calib_packv5_042523_0143.root, FC#9, port A1
Entries 354
Mean 45.51
Std Dev 10.91
Turn on : 30.8723
Width : 3.554
Height : 10.146
Entry
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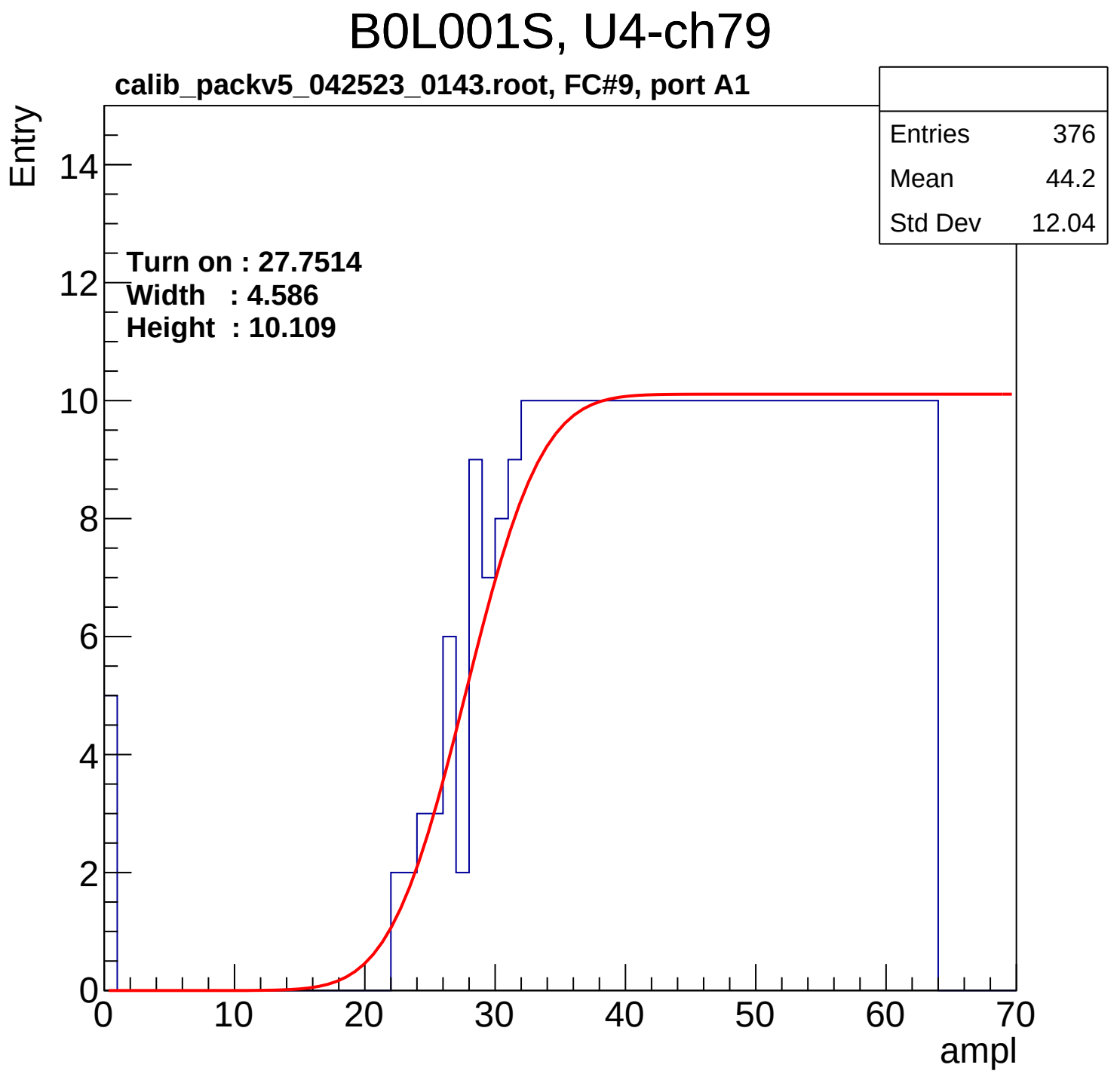
B0L001S, U4-ch79
calib_packv5_042523_0143.root, FC#9, port A1
Entries 376
Mean 44.2
Std Dev 12.04
Turn on : 27.7514
Width : 4.586
Height : 10.109
Entry
ampl
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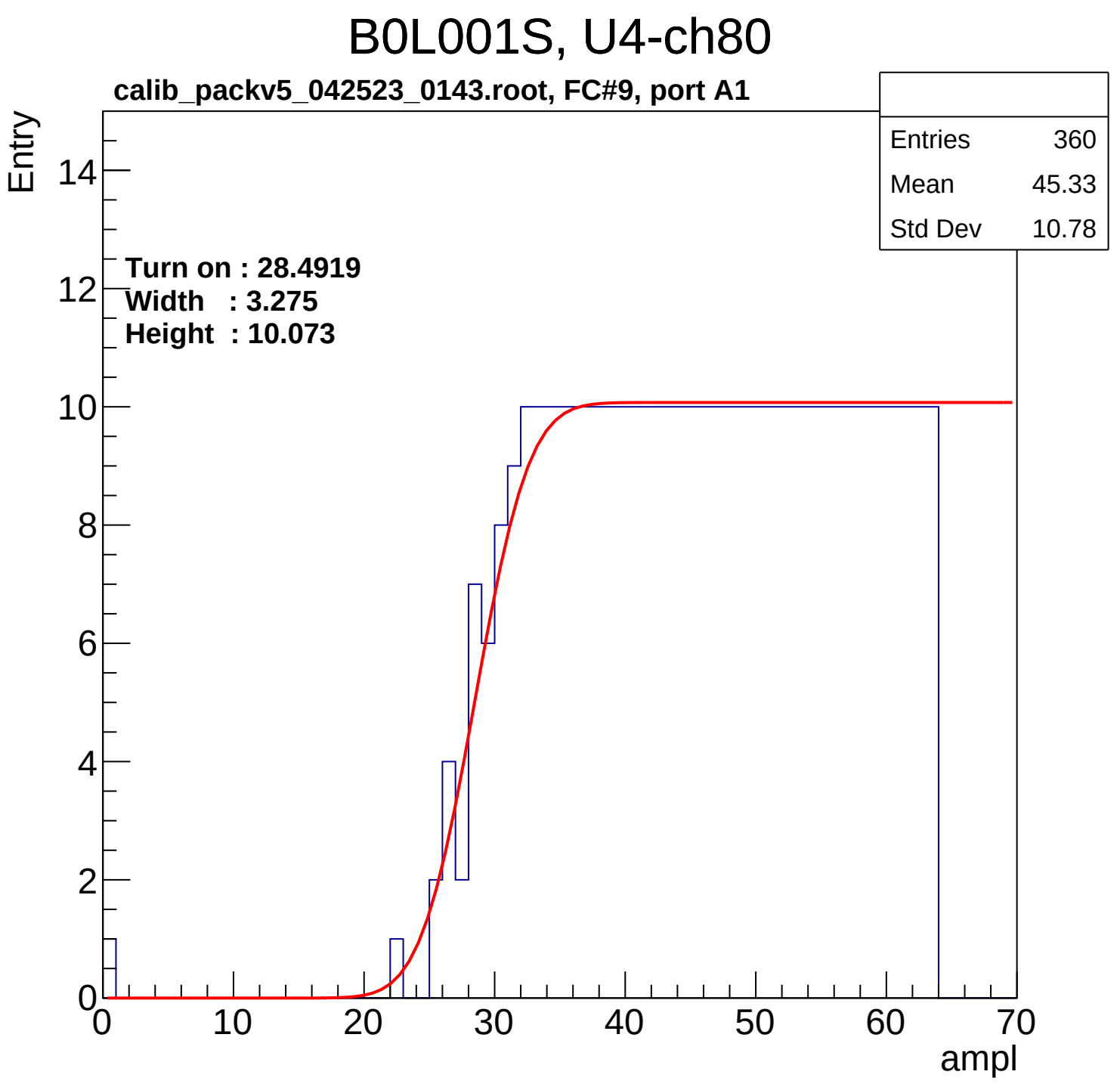
B0L001S, U4-ch80
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 45.33
Std Dev 10.78
Turn on : 28.4919
Width : 3.275
Height : 10.073
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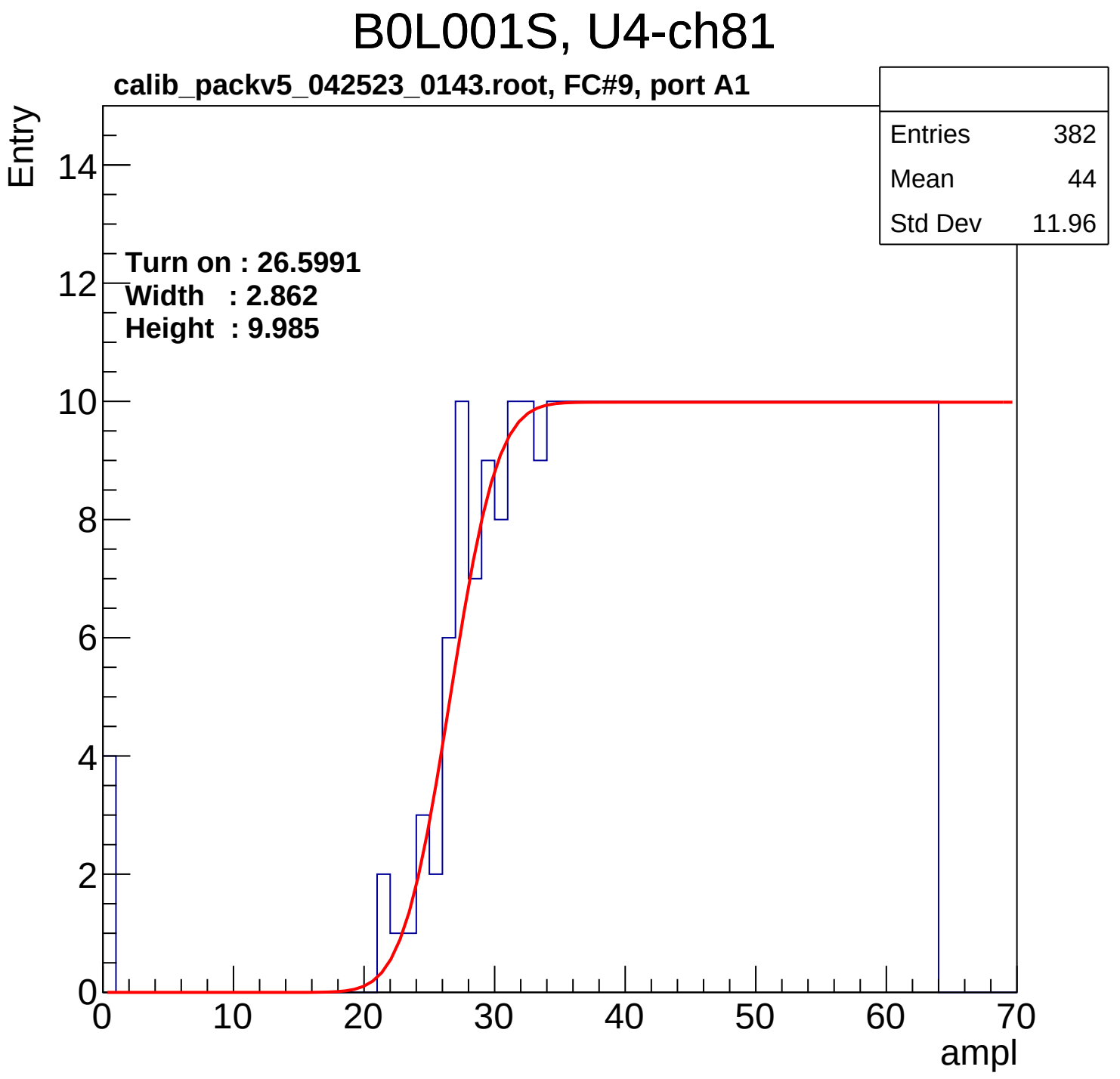
B0L001S, U4-ch81
calib_packv5_042523_0143.root, FC#9, port A1
Entries 382
Mean 44
Std Dev 11.96
Turn on : 26.5991
Width : 2.862
Height : 9.985
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ampl
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6
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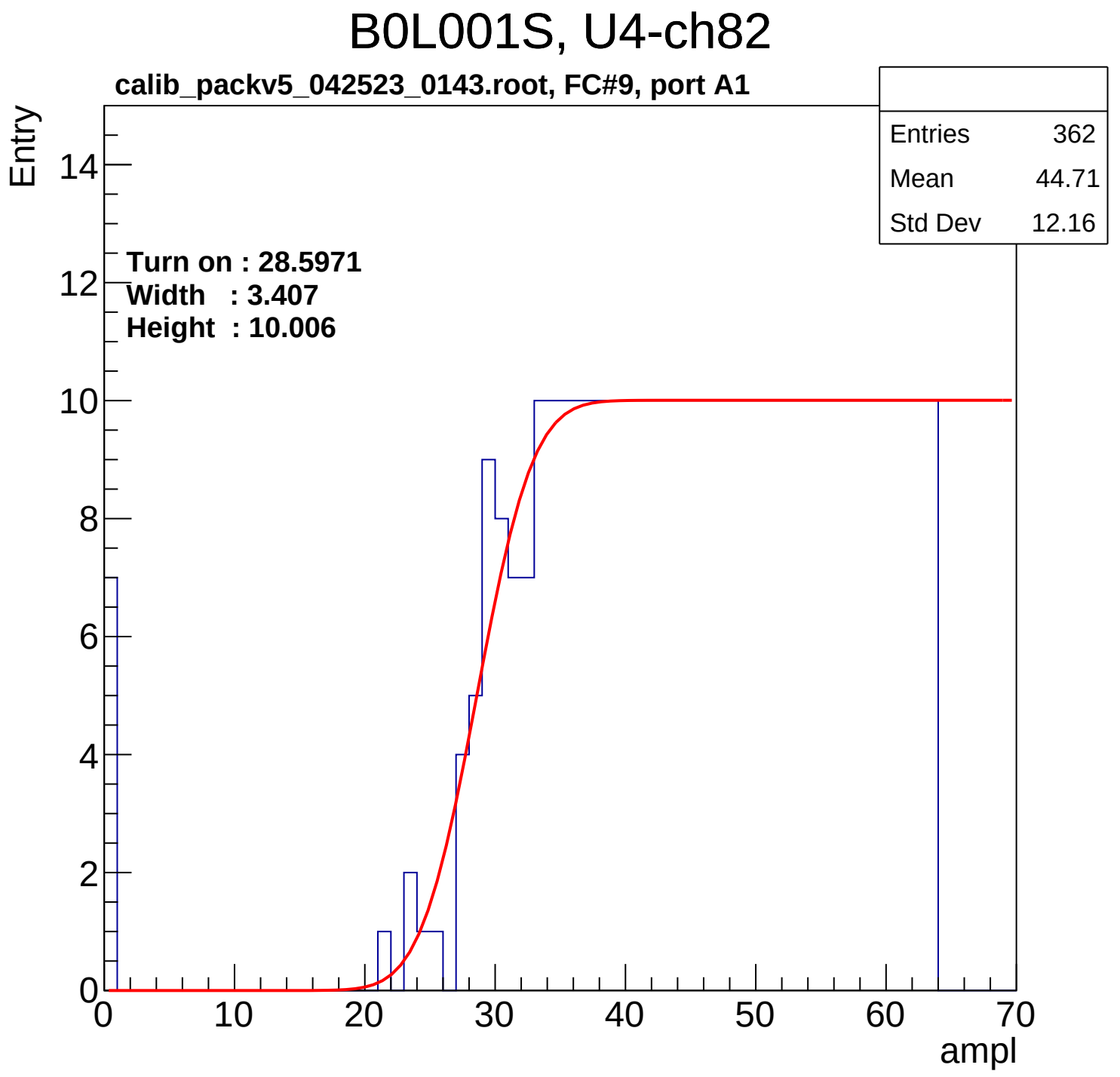
B0L001S, U4-ch82
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 44.71
Std Dev 12.16
Turn on : 28.5971
Width : 3.407
Height : 10.006
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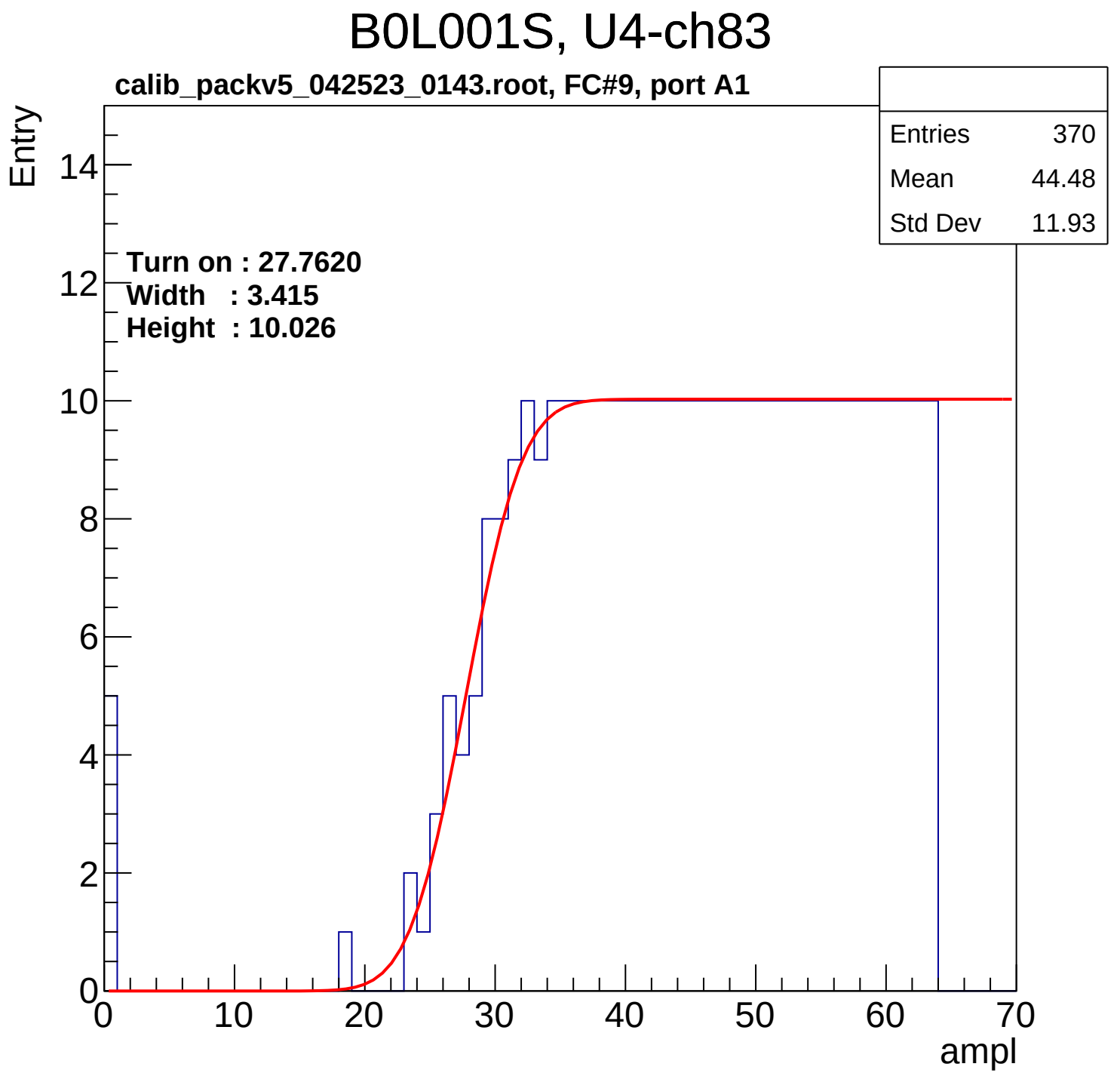
B0L001S, U4-ch83
calib_packv5_042523_0143.root, FC#9, port A1
Entries 370
Mean 44.48
Std Dev 11.93
Turn on : 27.7620
Width : 3.415
Height : 10.026
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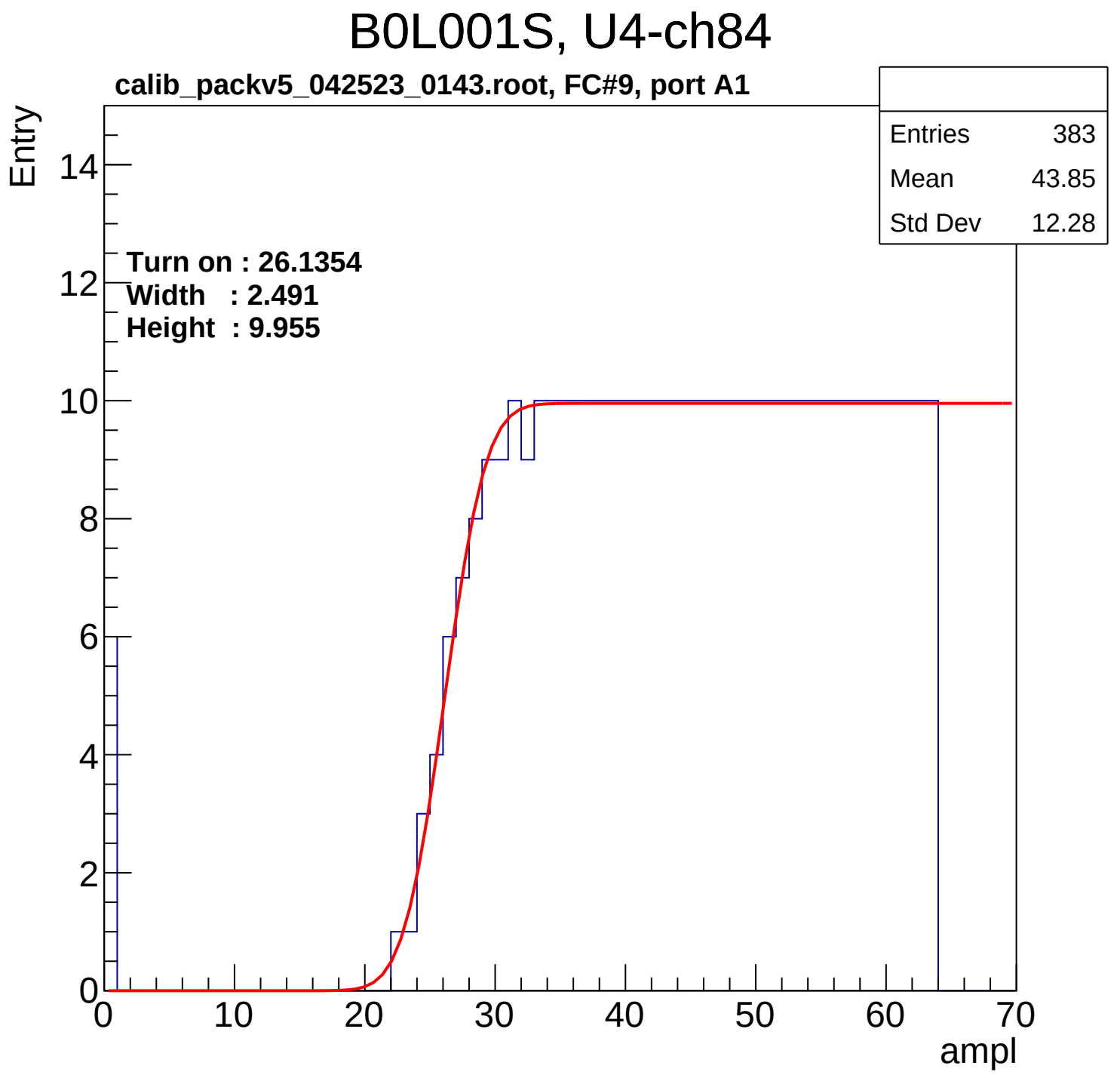
B0L001S, U4-ch84
calib_packv5_042523_0143.root, FC#9, port A1
Entries 383
Mean 43.85
Std Dev 12.28
Turn on : 26.1354
Width : 2.491
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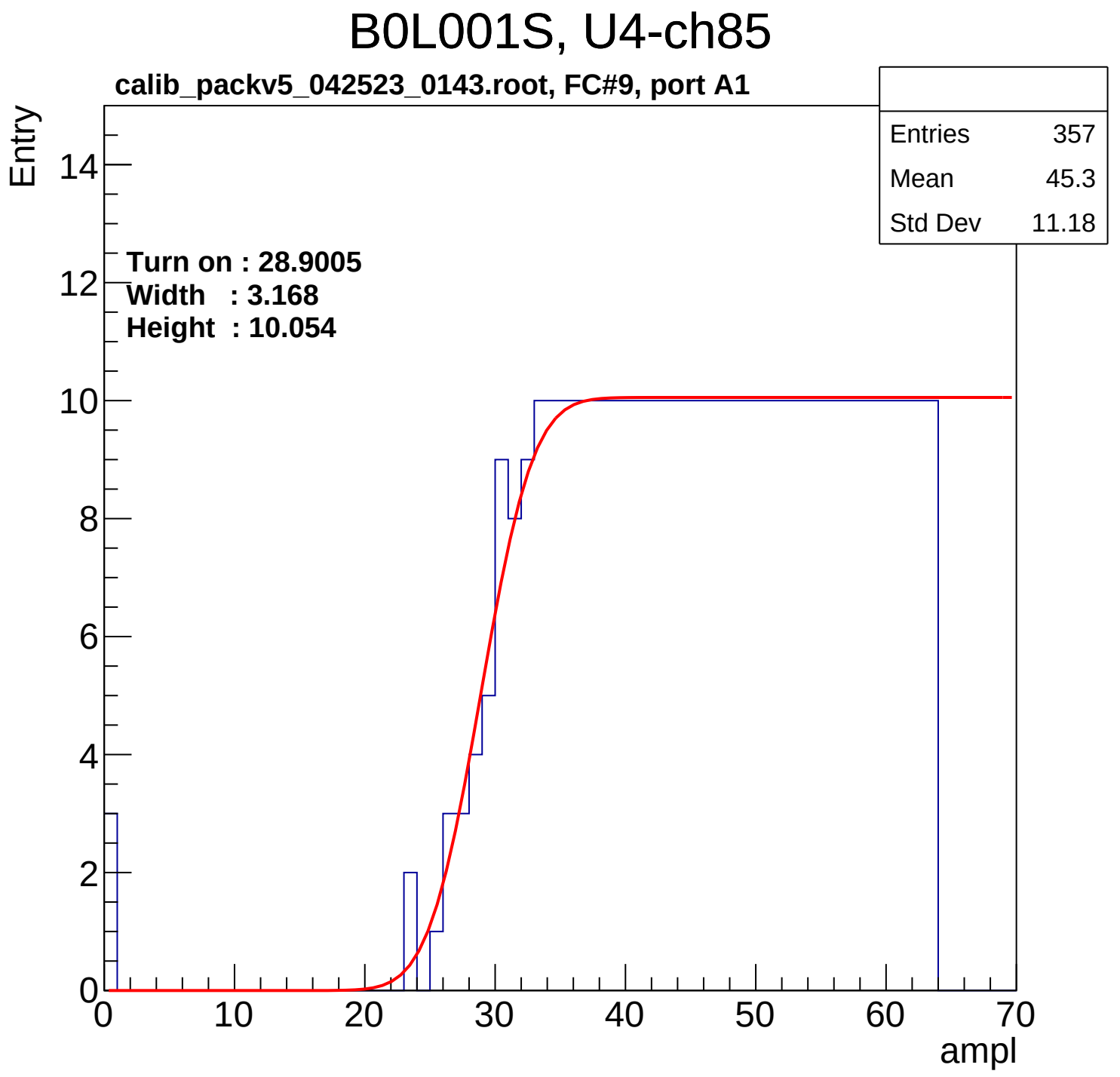
B0L001S, U4-ch85
calib_packv5_042523_0143.root, FC#9, port A1
Entries 357
Mean 45.3
Std Dev 11.18
Turn on : 28.9005
Width : 3.168
Height : 10.054
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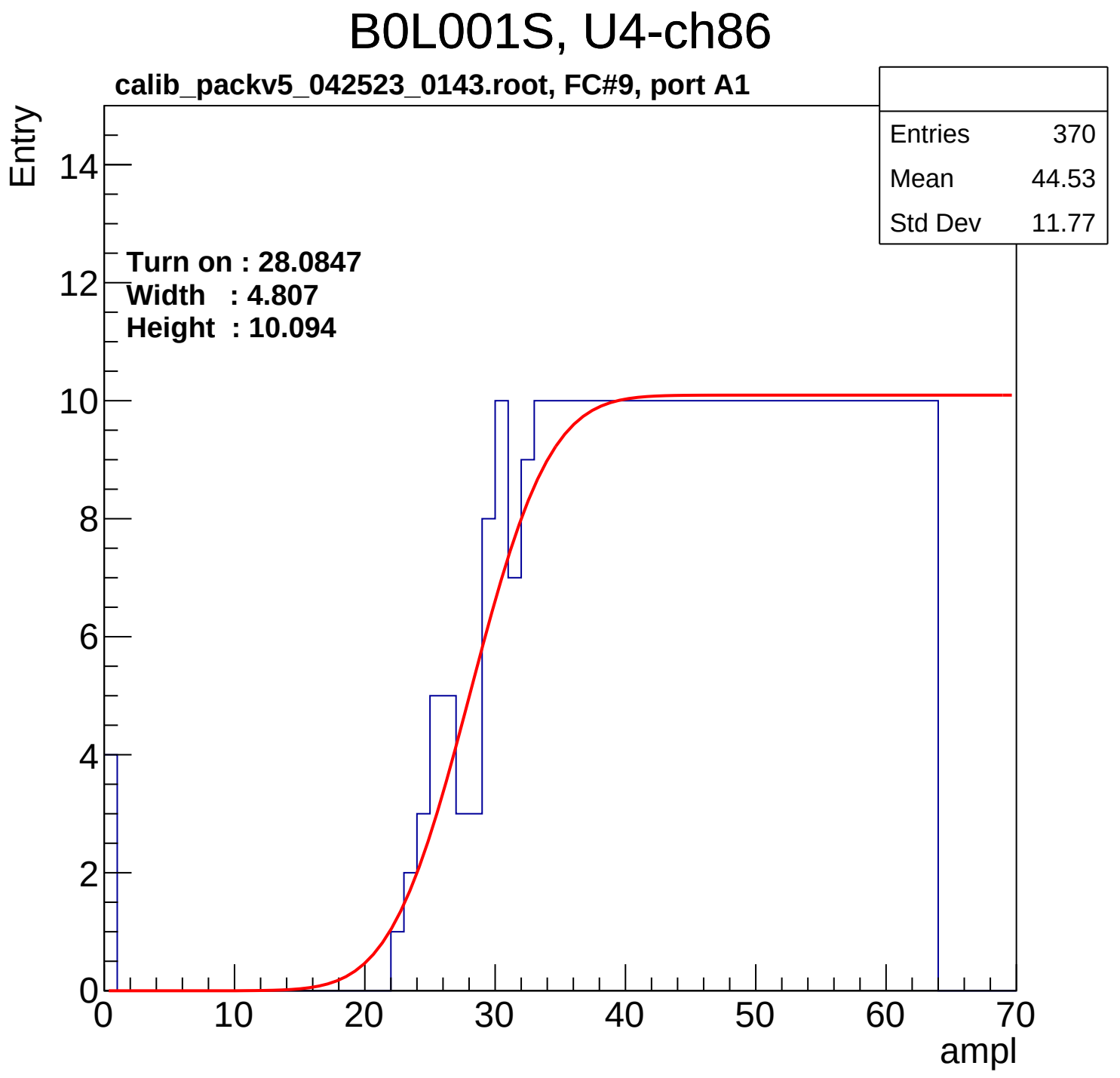
B0L001S, U4-ch86
calib_packv5_042523_0143.root, FC#9, port A1
Entries 370
Mean 44.53
Std Dev 11.77
Turn on : 28.0847
Width : 4.807
Height : 10.094
Entry
ampl
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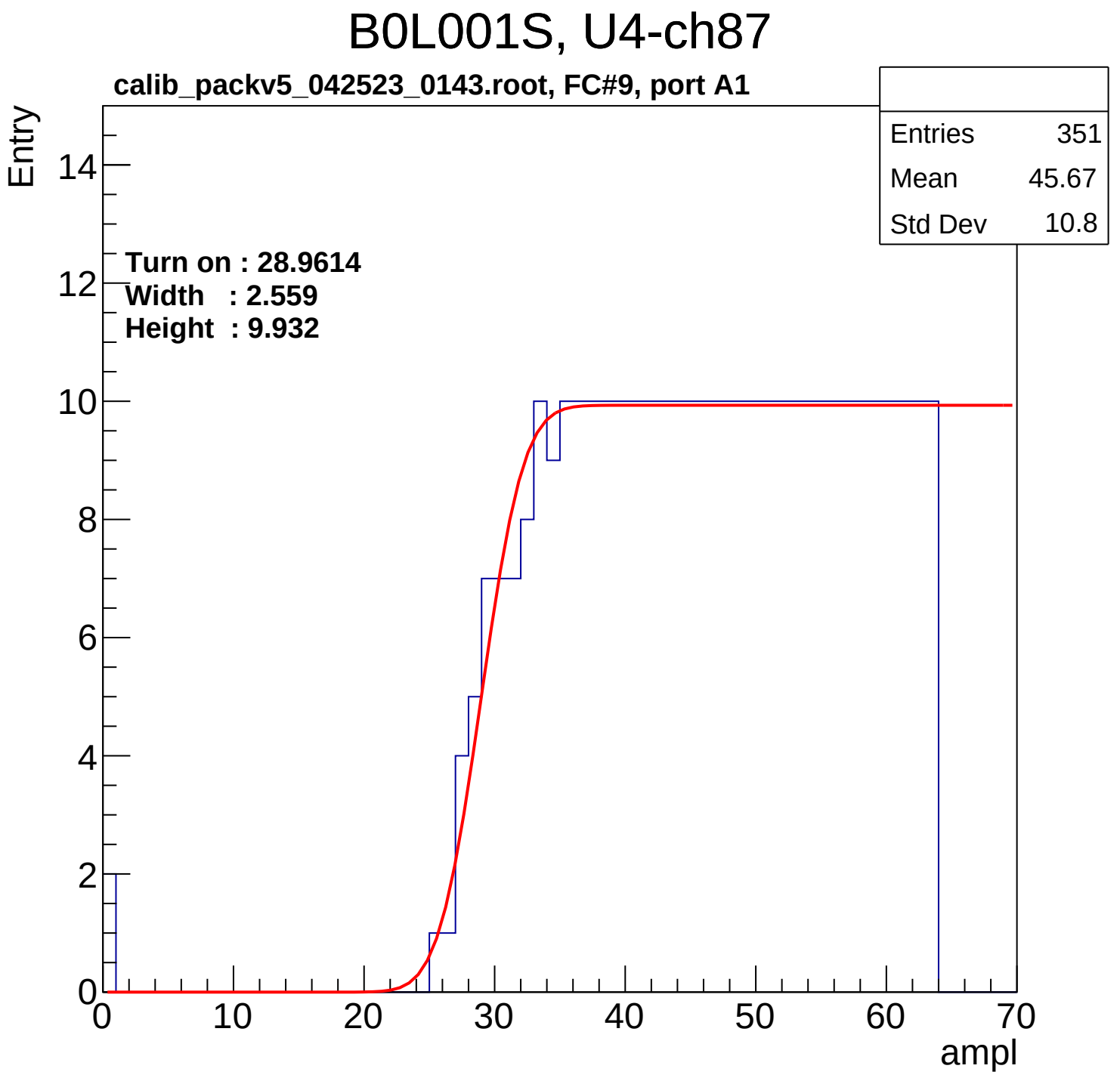
B0L001S, U4-ch87
calib_packv5_042523_0143.root, FC#9, port A1
Entries 351
Mean 45.67
Std Dev 10.8
Turn on : 28.9614
Width : 2.559
Height : 9.932
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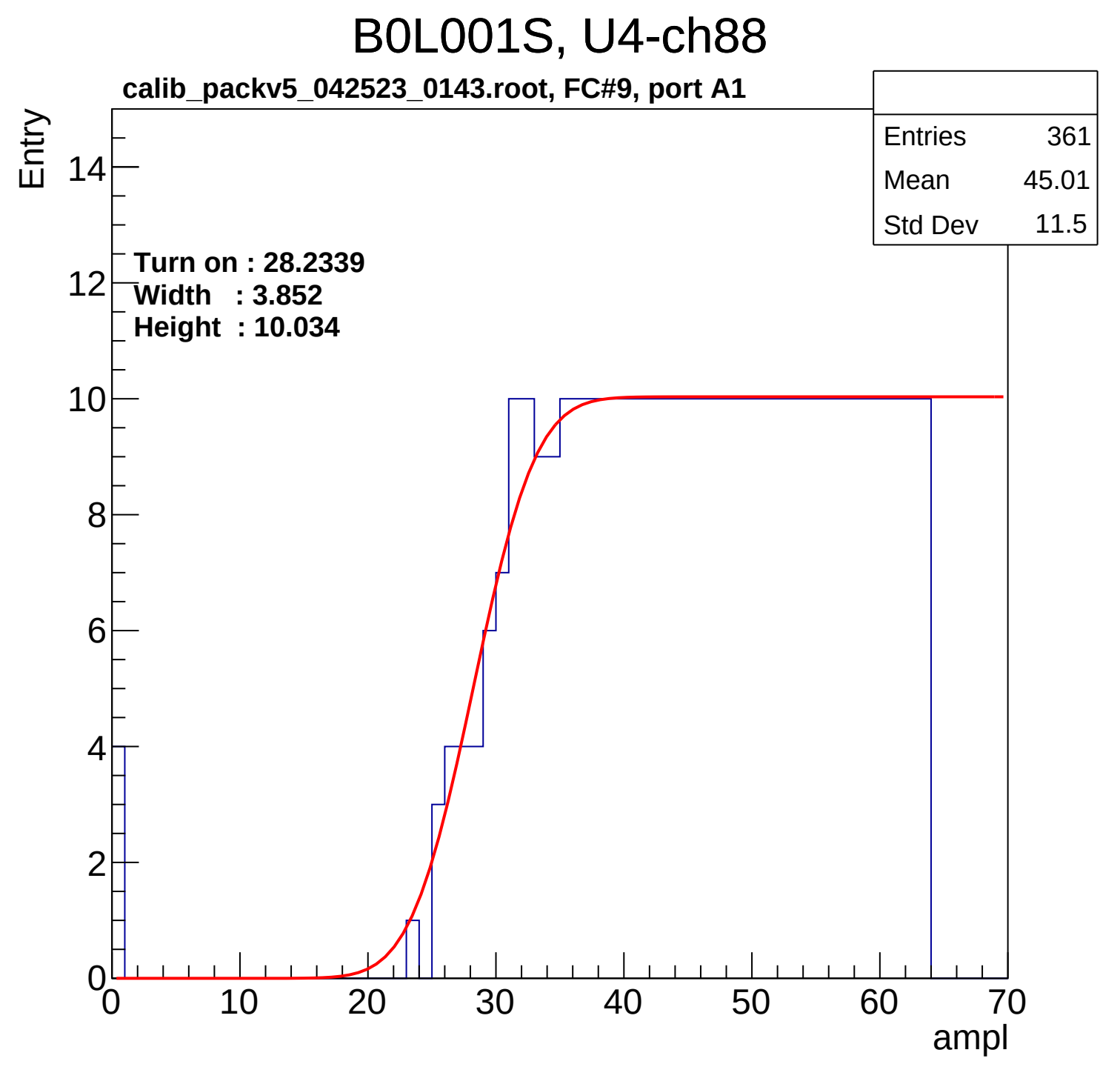
B0L001S, U4-ch88
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 45.01
Std Dev 11.5
Turn on : 28.2339
Width : 3.852
Height : 10.034
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ampl
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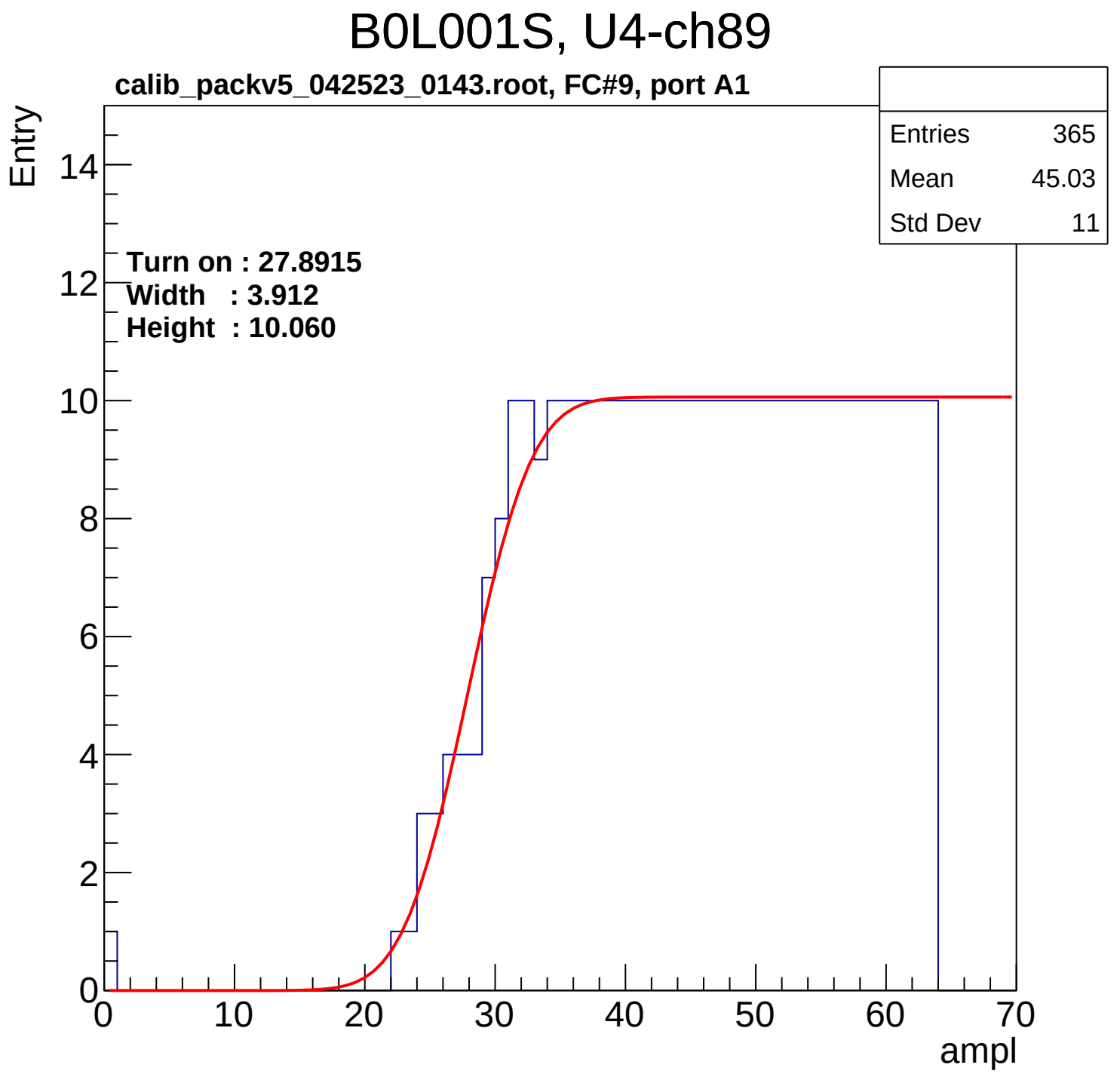
B0L001S, U4-ch89
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 45.03
Std Dev 11
Turn on : 27.8915
Width : 3.912
Height : 10.060
Entry
ampl
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2
4
6
8
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60
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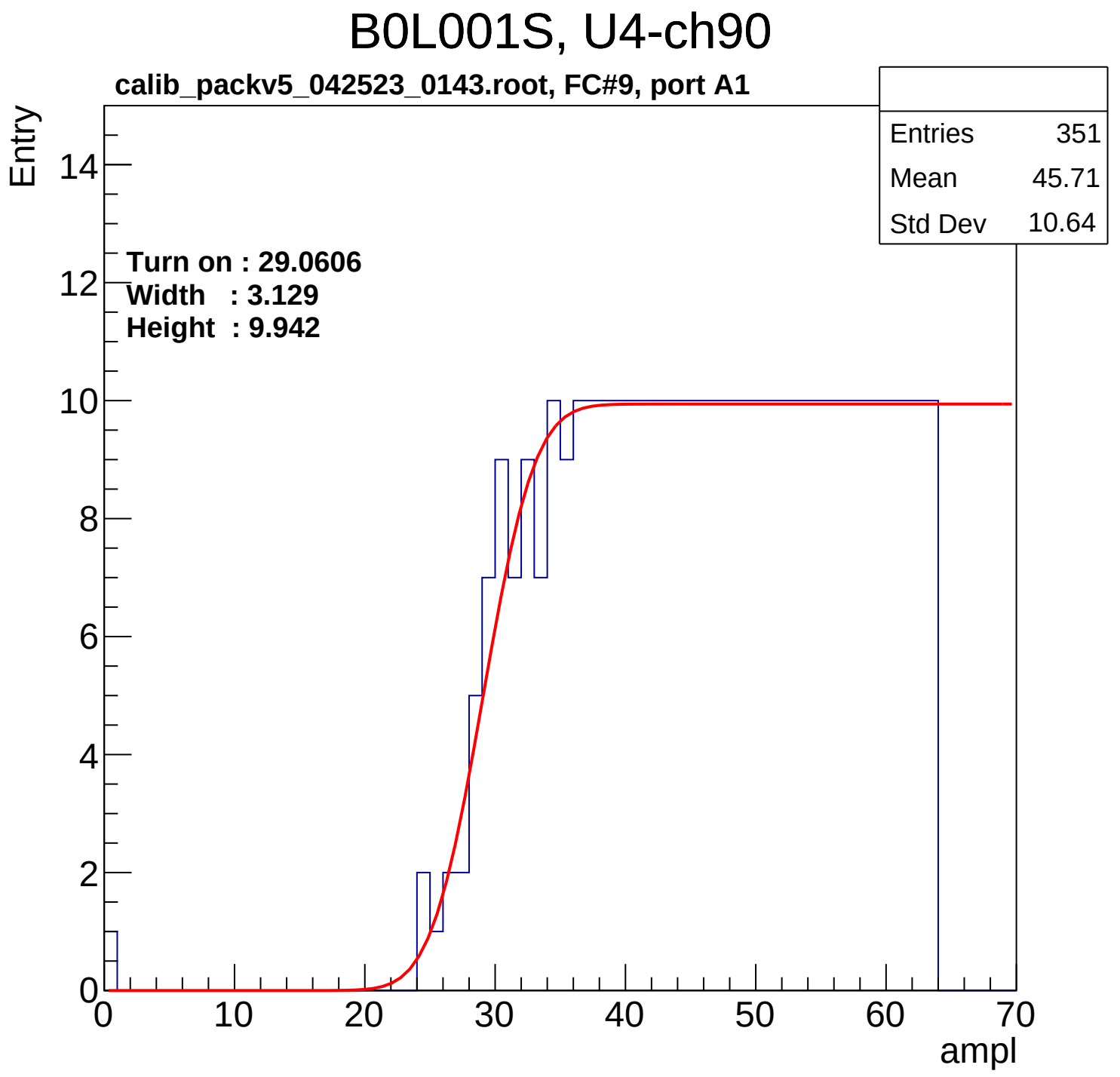
B0L001S, U4-ch90
calib_packv5_042523_0143.root, FC#9, port A1
Entries 351
Mean 45.71
Std Dev 10.64
Turn on : 29.0606
Width : 3.129
Height : 9.942
Entry
ampl
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2
4
6
8
10
12
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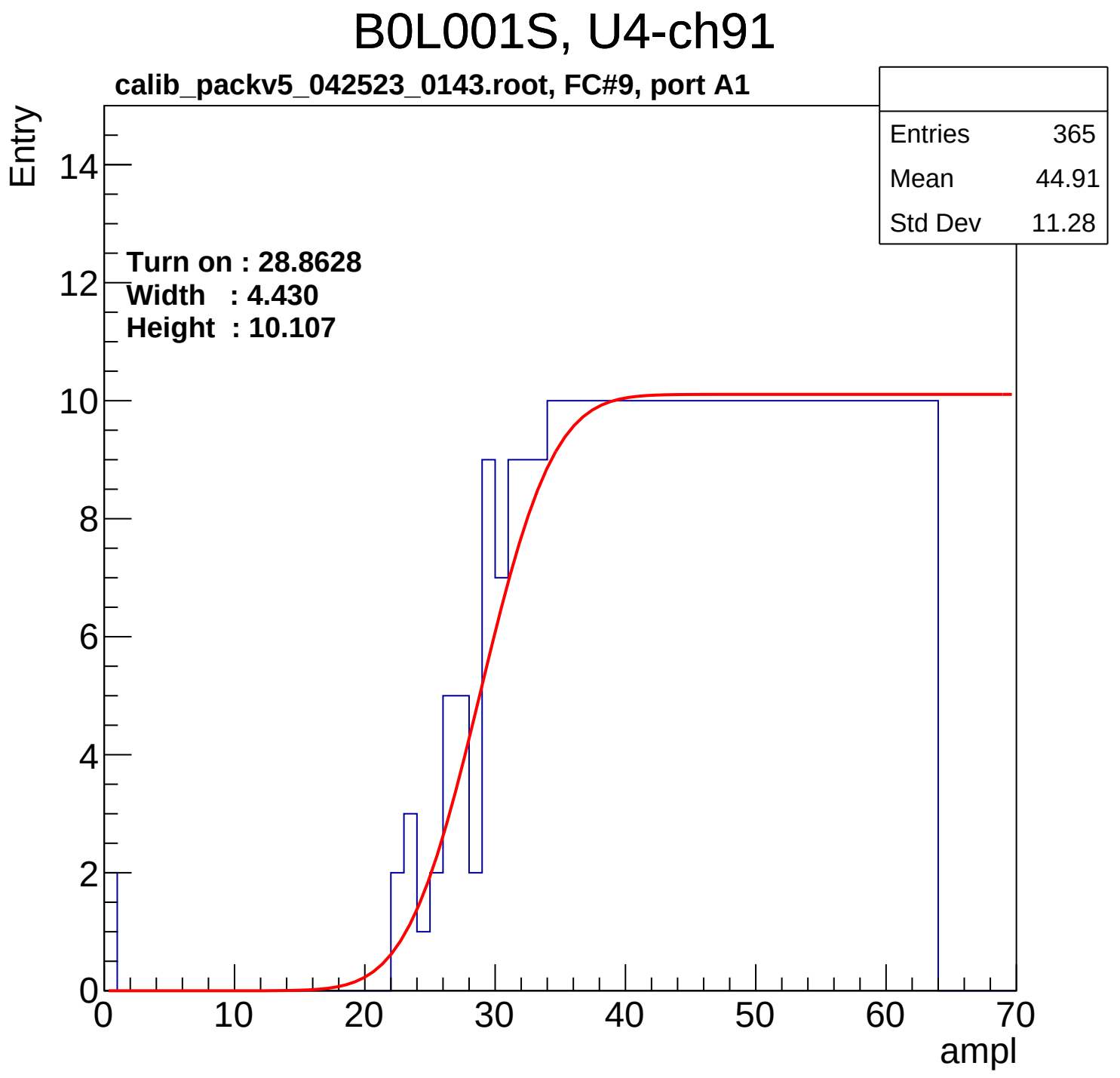
B0L001S, U4-ch91
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 44.91
Std Dev 11.28
Turn on : 28.8628
Width : 4.430
Height : 10.107
Entry
ampl
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2
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6
8
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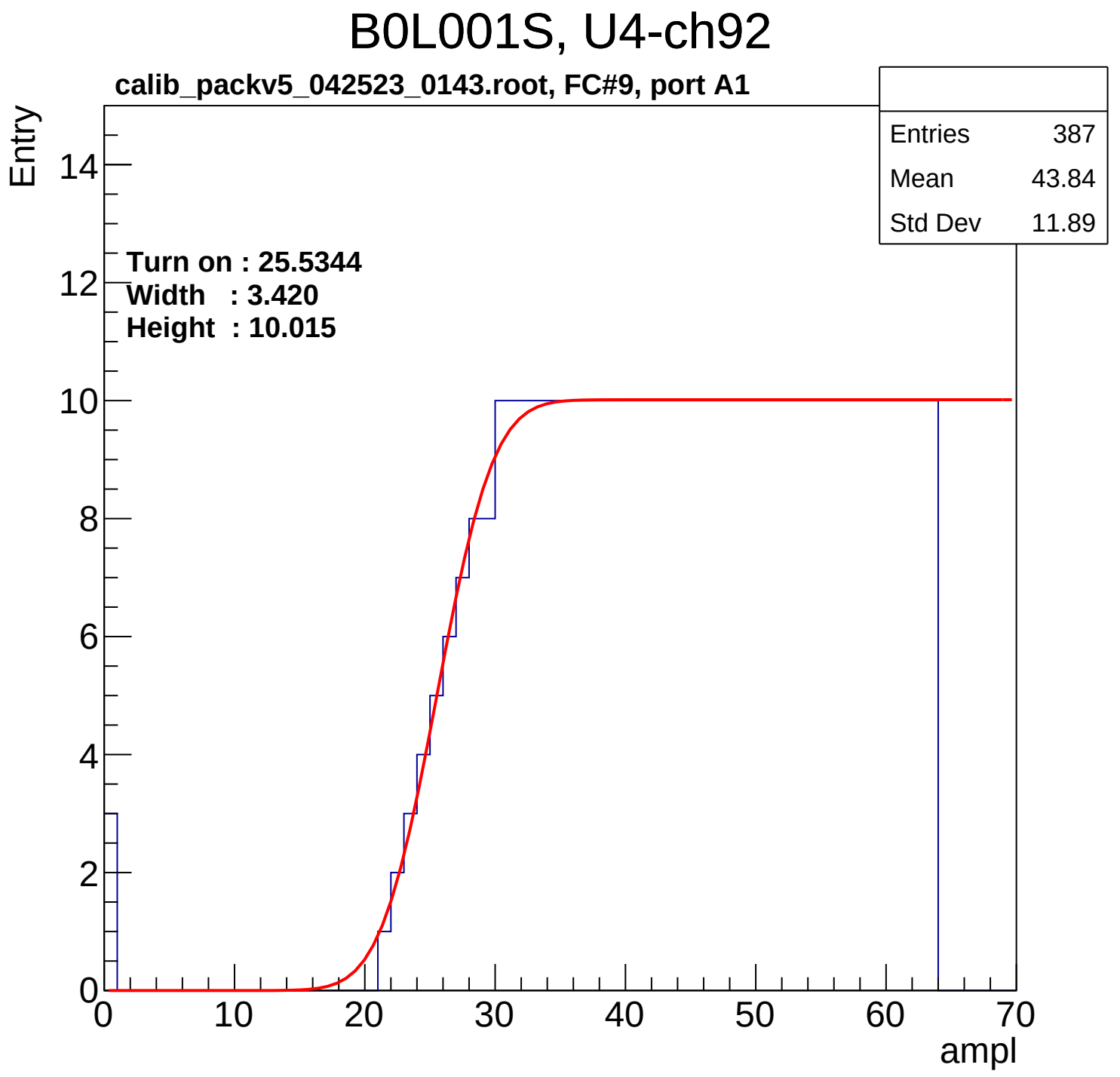
B0L001S, U4-ch92
calib_packv5_042523_0143.root, FC#9, port A1
Entries 387
Mean 43.84
Std Dev 11.89
Turn on : 25.5344
Width : 3.420
Height : 10.015
Entry
ampl
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2
4
6
8
10
12
14
0
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60
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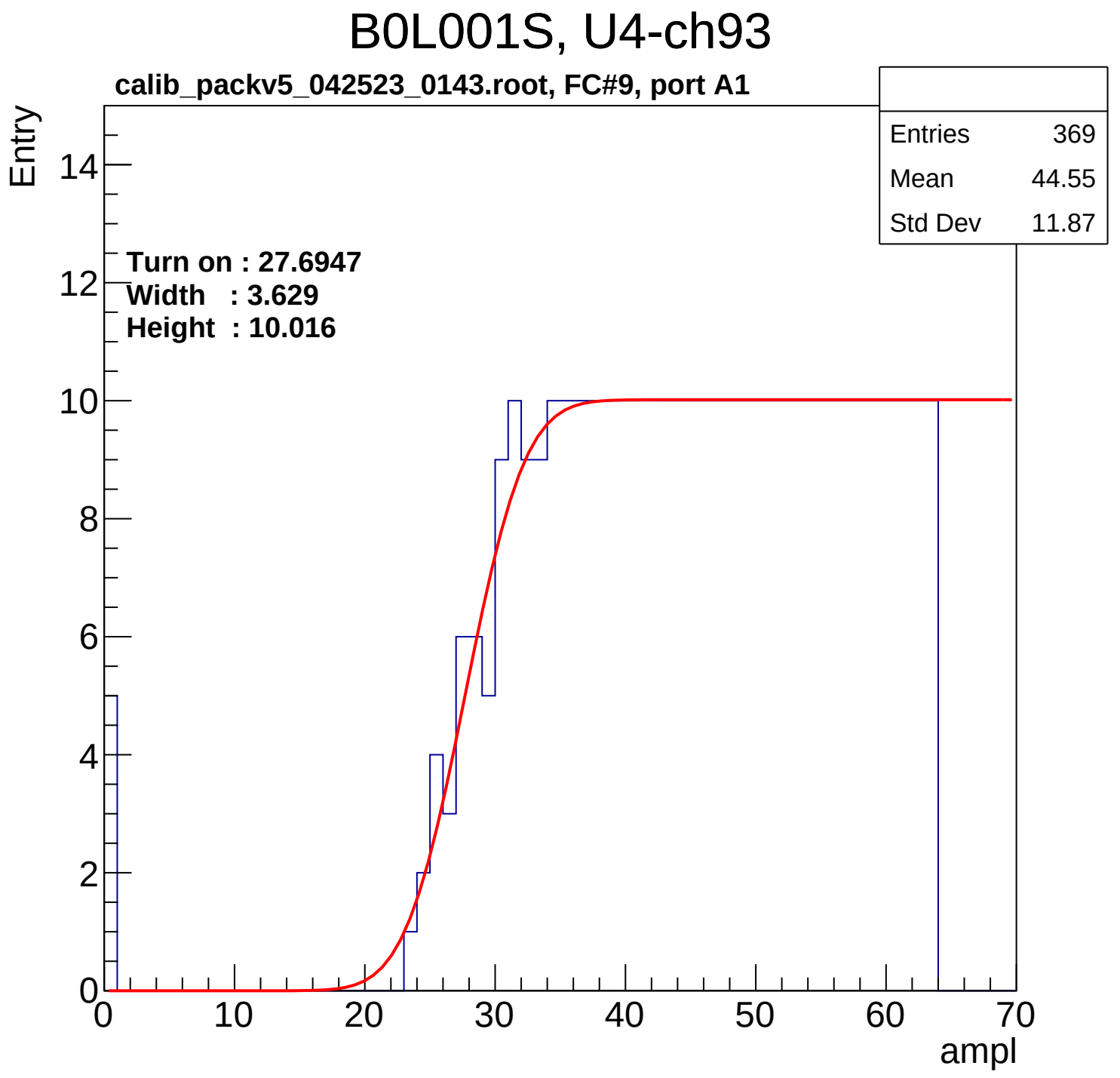
B0L001S, U4-ch93
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.55
Std Dev 11.87
Turn on : 27.6947
Width : 3.629
Height : 10.016
Entry
ampl
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4
6
8
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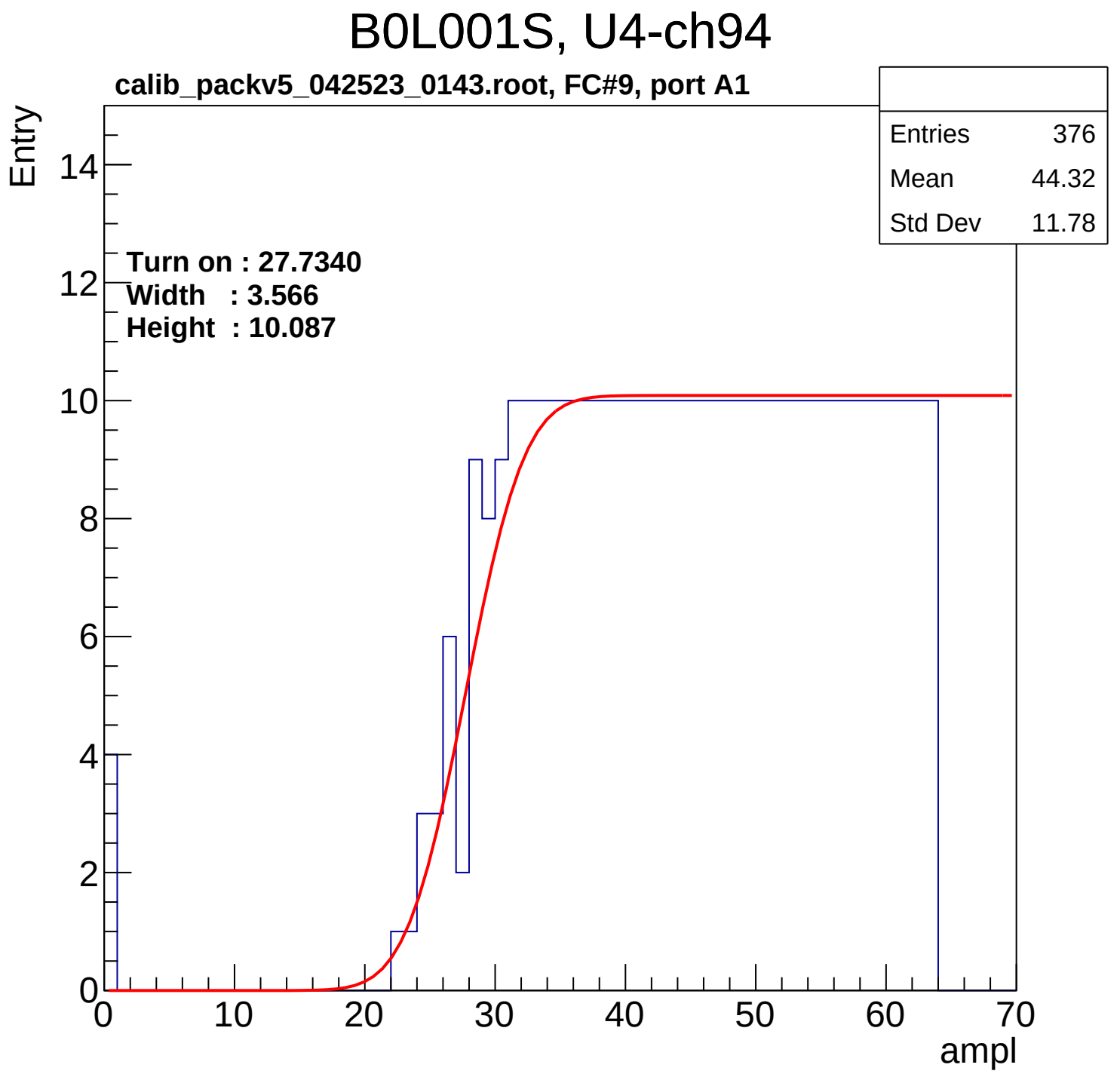
B0L001S, U4-ch94
calib_packv5_042523_0143.root, FC#9, port A1
Entries 376
Mean 44.32
Std Dev 11.78
Turn on : 27.7340
Width : 3.566
Height : 10.087
Entry
ampl
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4
6
8
10
12
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0
10
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40
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60
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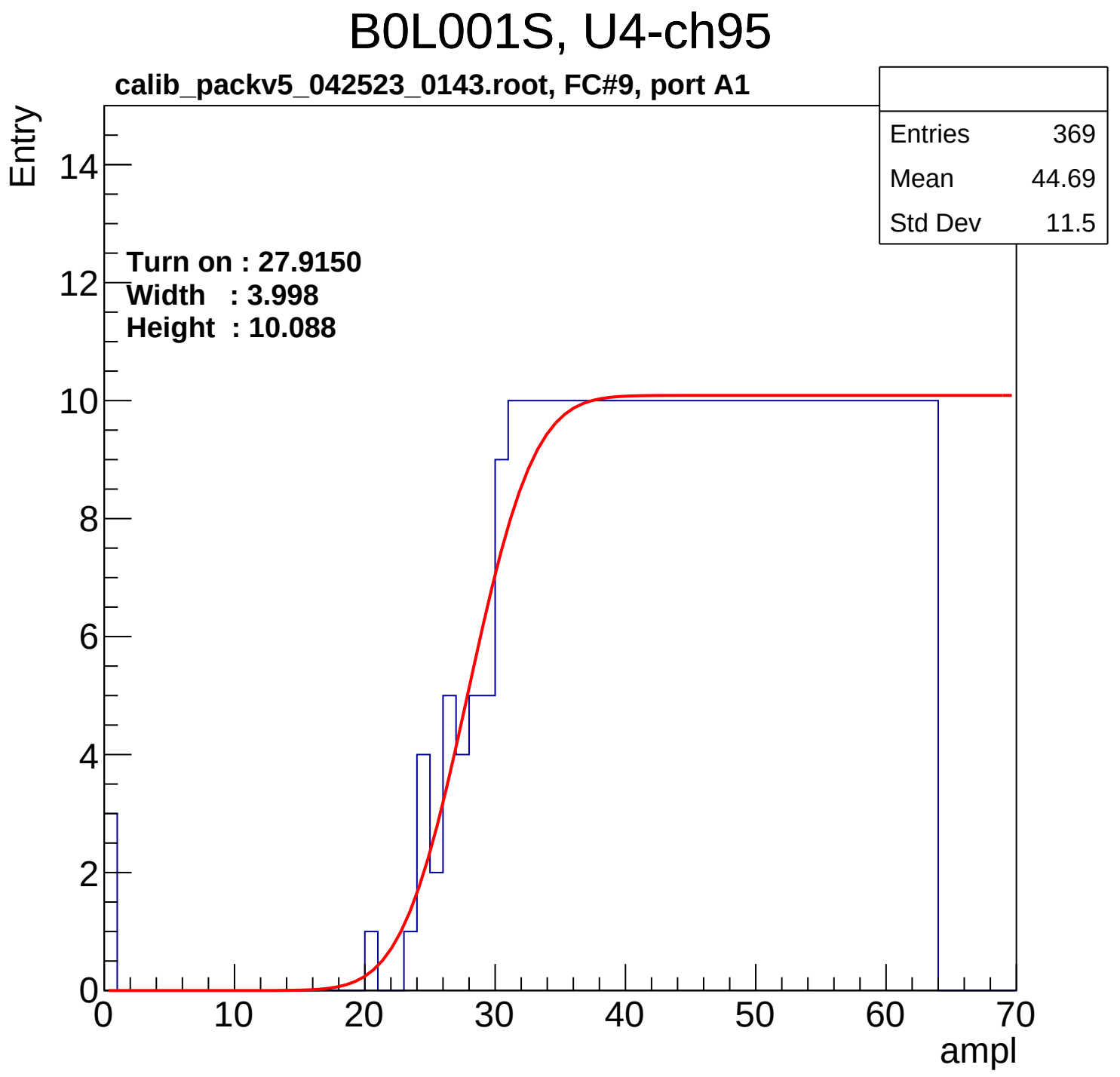
B0L001S, U4-ch95
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.69
Std Dev 11.5
Turn on : 27.9150
Width : 3.998
Height : 10.088
Entry
ampl
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4
6
8
10
12
14
0
10
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40
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60
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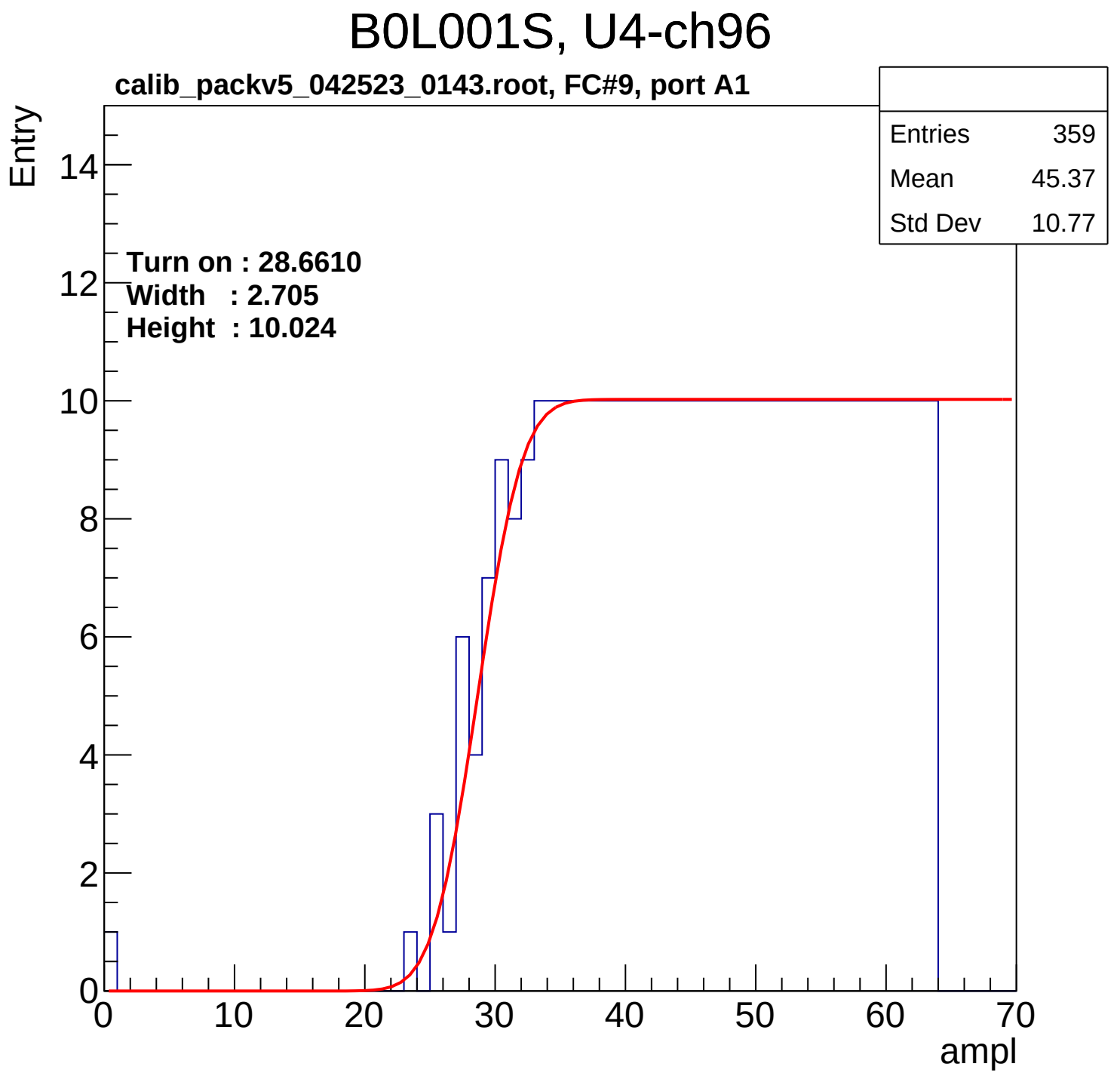
B0L001S, U4-ch96
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 45.37
Std Dev 10.77
Turn on : 28.6610
Width : 2.705
Height : 10.024
Entry
ampl
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6
8
10
12
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60
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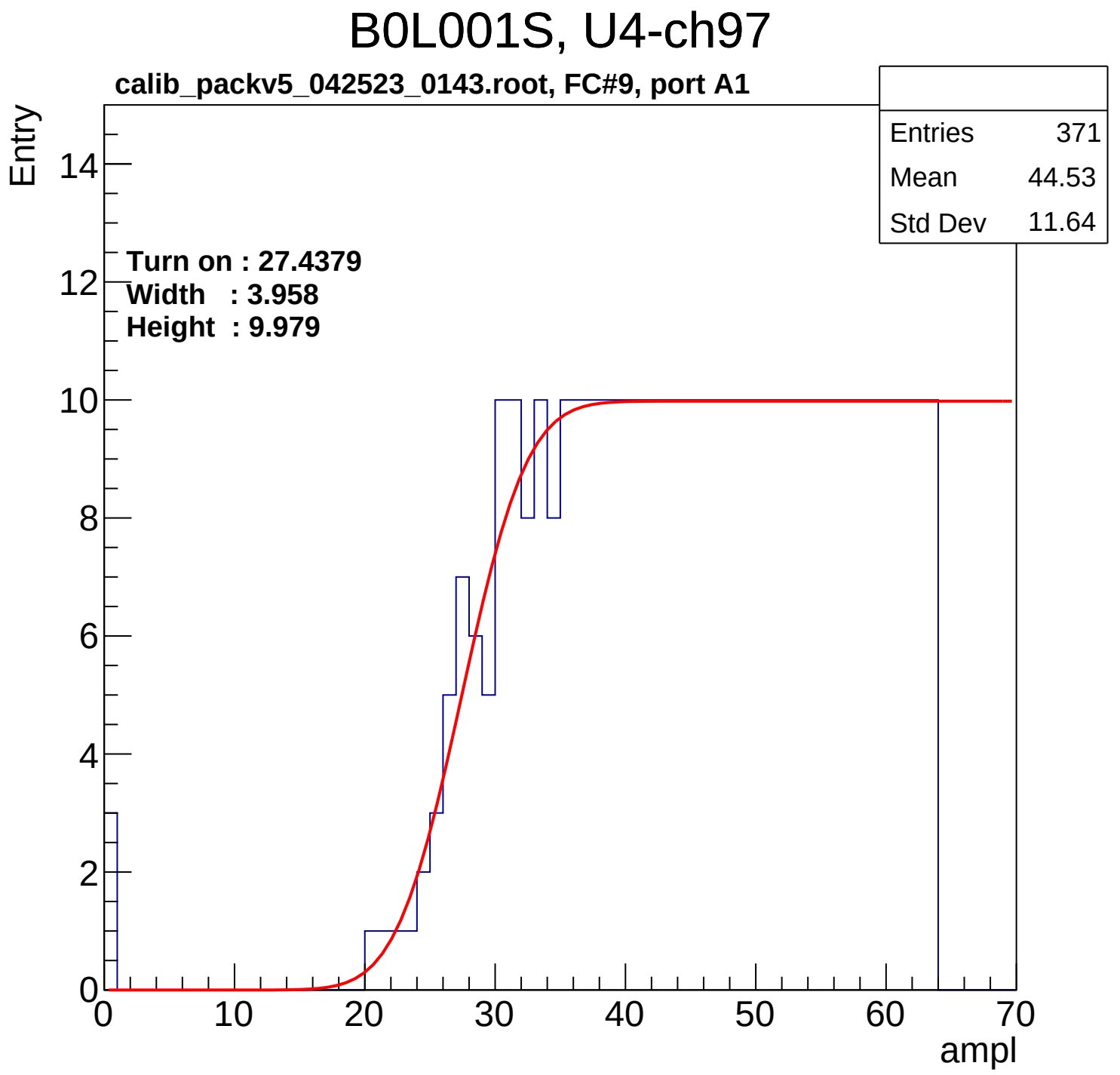
B0L001S, U4-ch97
calib_packv5_042523_0143.root, FC#9, port A1
Entries 371
Mean 44.53
Std Dev 11.64
Turn on : 27.4379
Width : 3.958
Height : 9.979
Entry
ampl
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4
6
8
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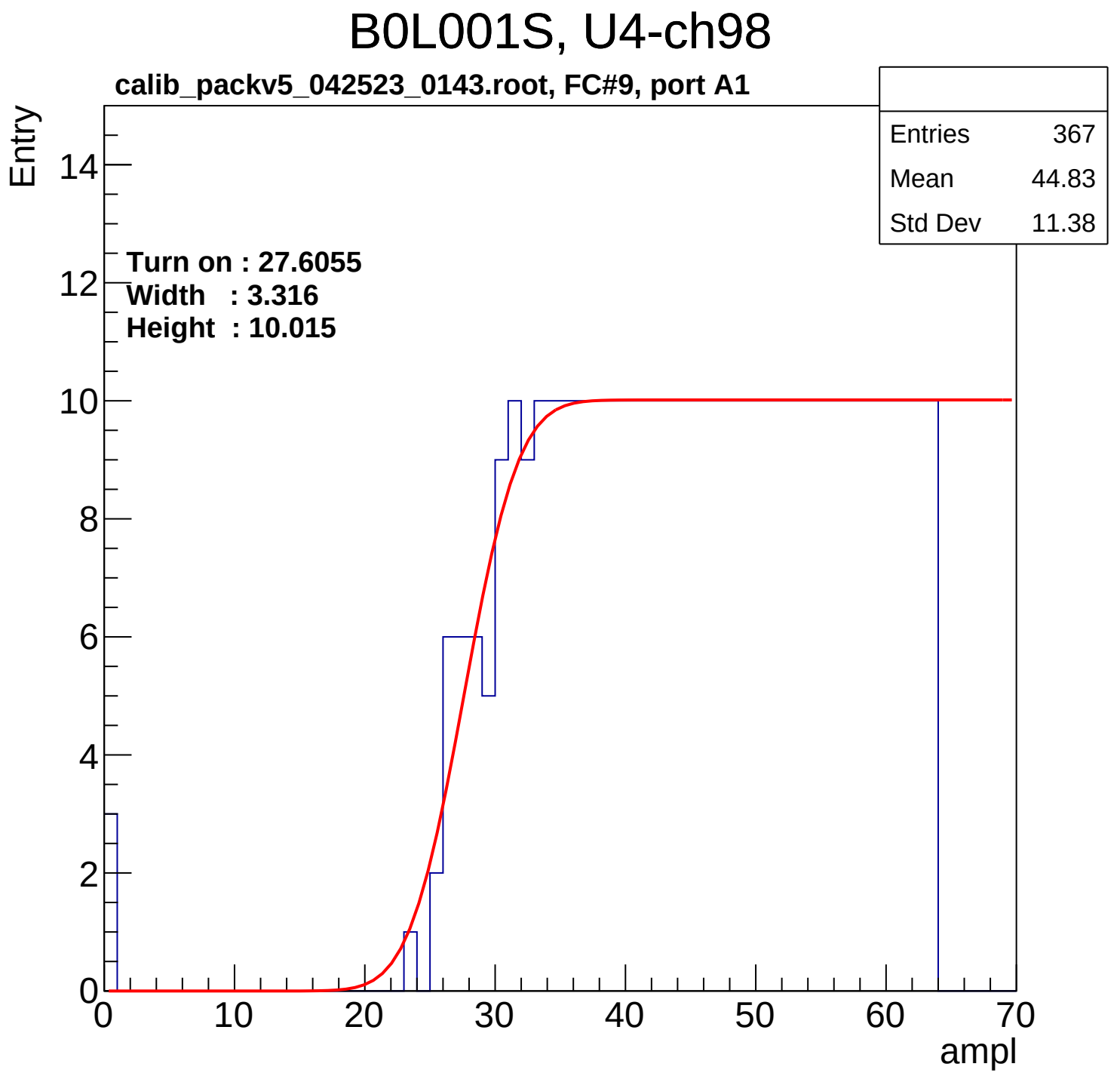
B0L001S, U4-ch98
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.83
Std Dev 11.38
Turn on : 27.6055
Width : 3.316
Height : 10.015
Entry
ampl
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4
6
8
10
12
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60
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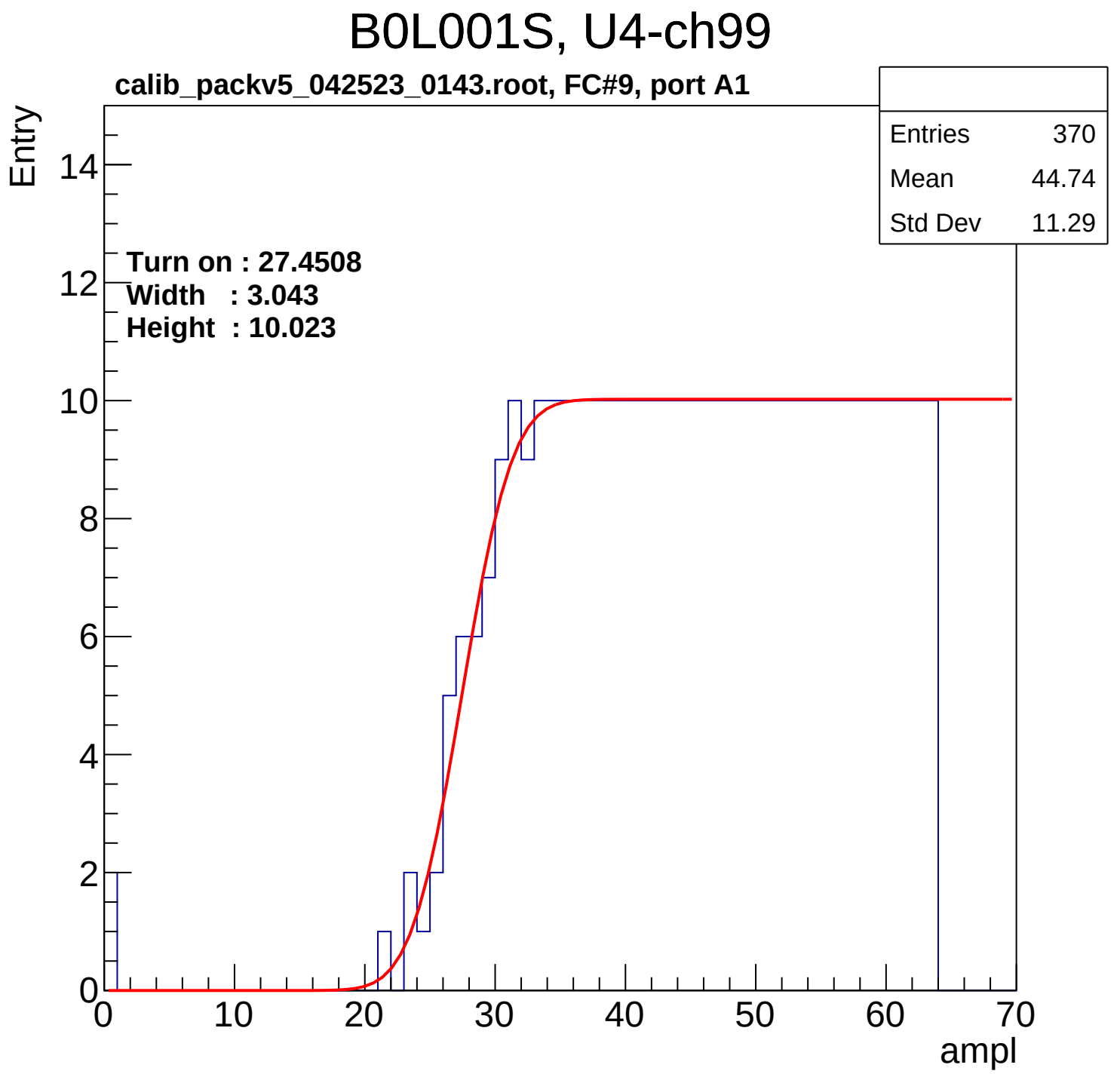
B0L001S, U4-ch99
calib_packv5_042523_0143.root, FC#9, port A1
Entries 370
Mean 44.74
Std Dev 11.29
Turn on : 27.4508
Width : 3.043
Height : 10.023
Entry
ampl
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6
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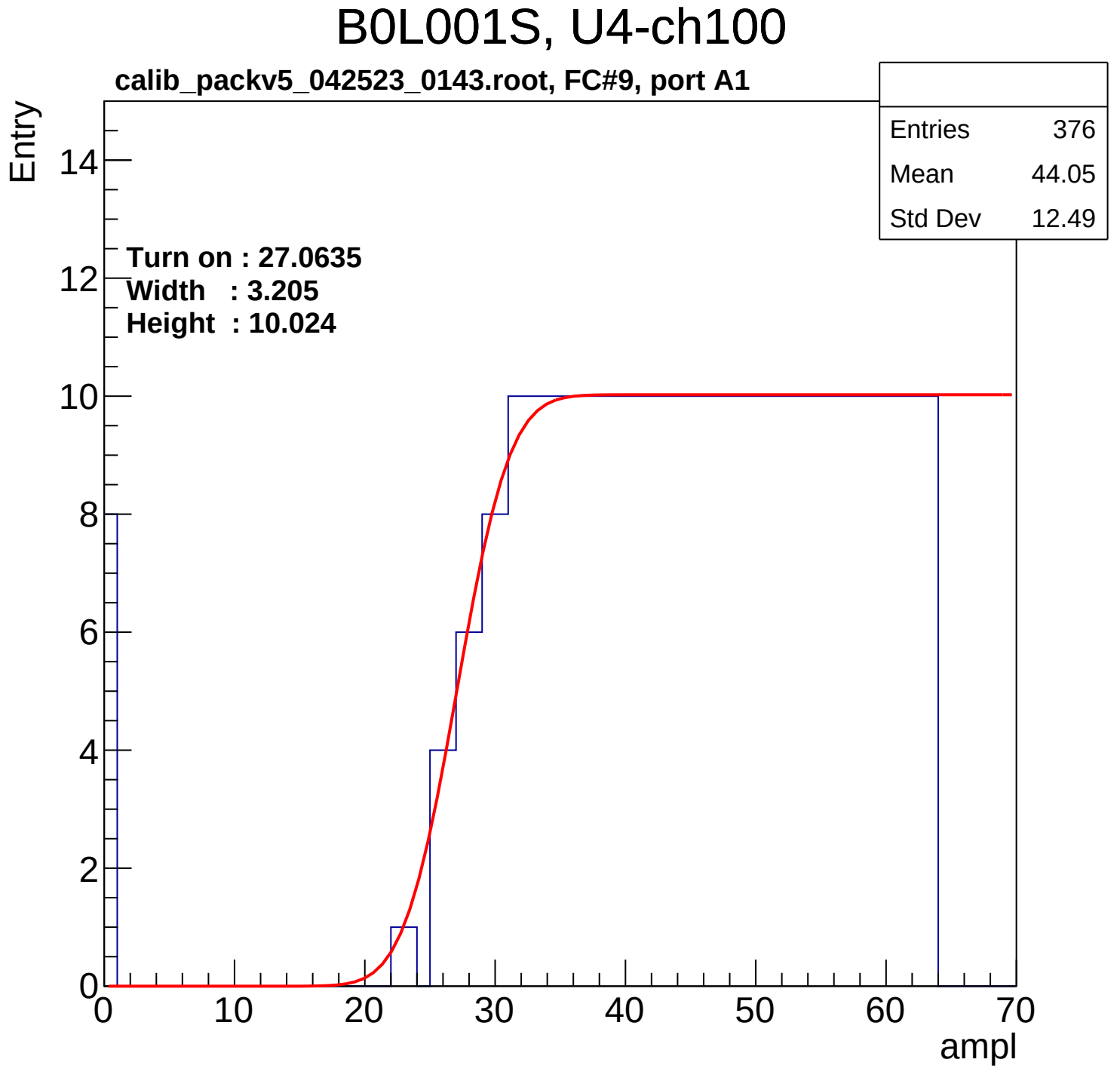
B0L001S, U4-ch100
calib_packv5_042523_0143.root, FC#9, port A1
Entries 376
Mean 44.05
Std Dev 12.49
Turn on : 27.0635
Width : 3.205
Height : 10.024
Entry
ampl
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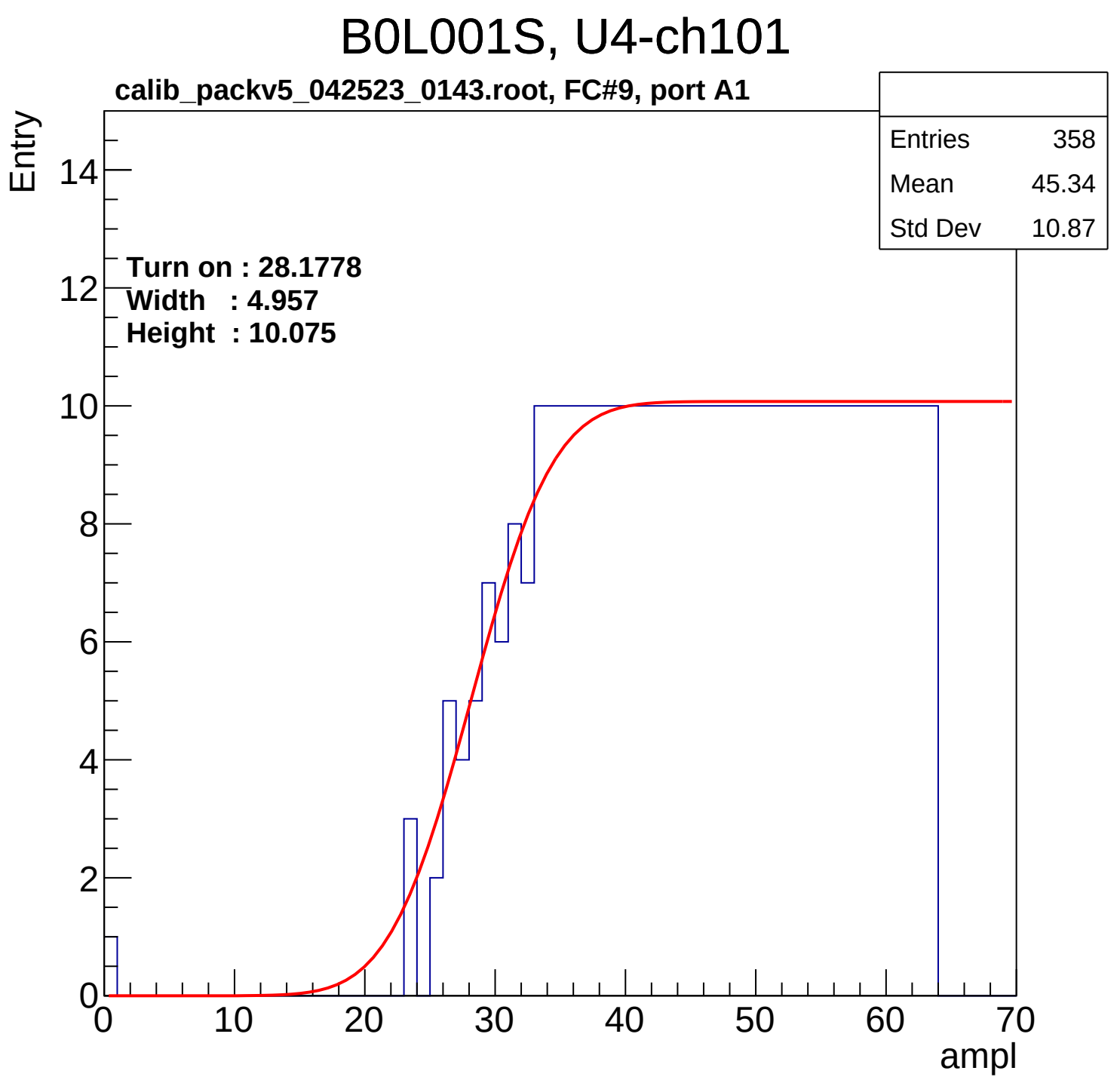
B0L001S, U4-ch101
calib_packv5_042523_0143.root, FC#9, port A1
Entries 358
Mean 45.34
Std Dev 10.87
Turn on : 28.1778
Width : 4.957
Height : 10.075
Entry
ampl
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6
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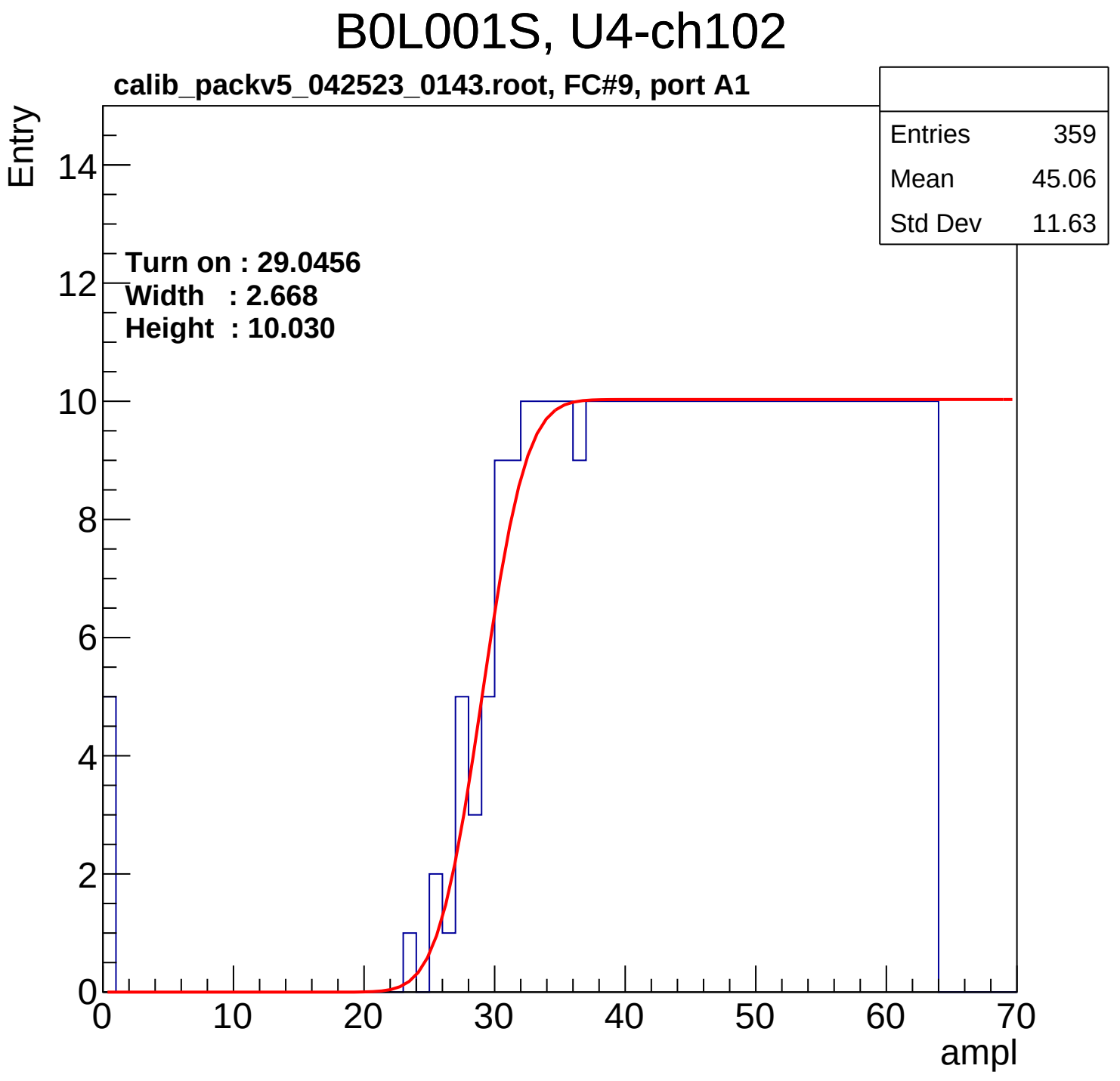
B0L001S, U4-ch102
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 45.06
Std Dev 11.63
Turn on : 29.0456
Width : 2.668
Height : 10.030
Entry
ampl
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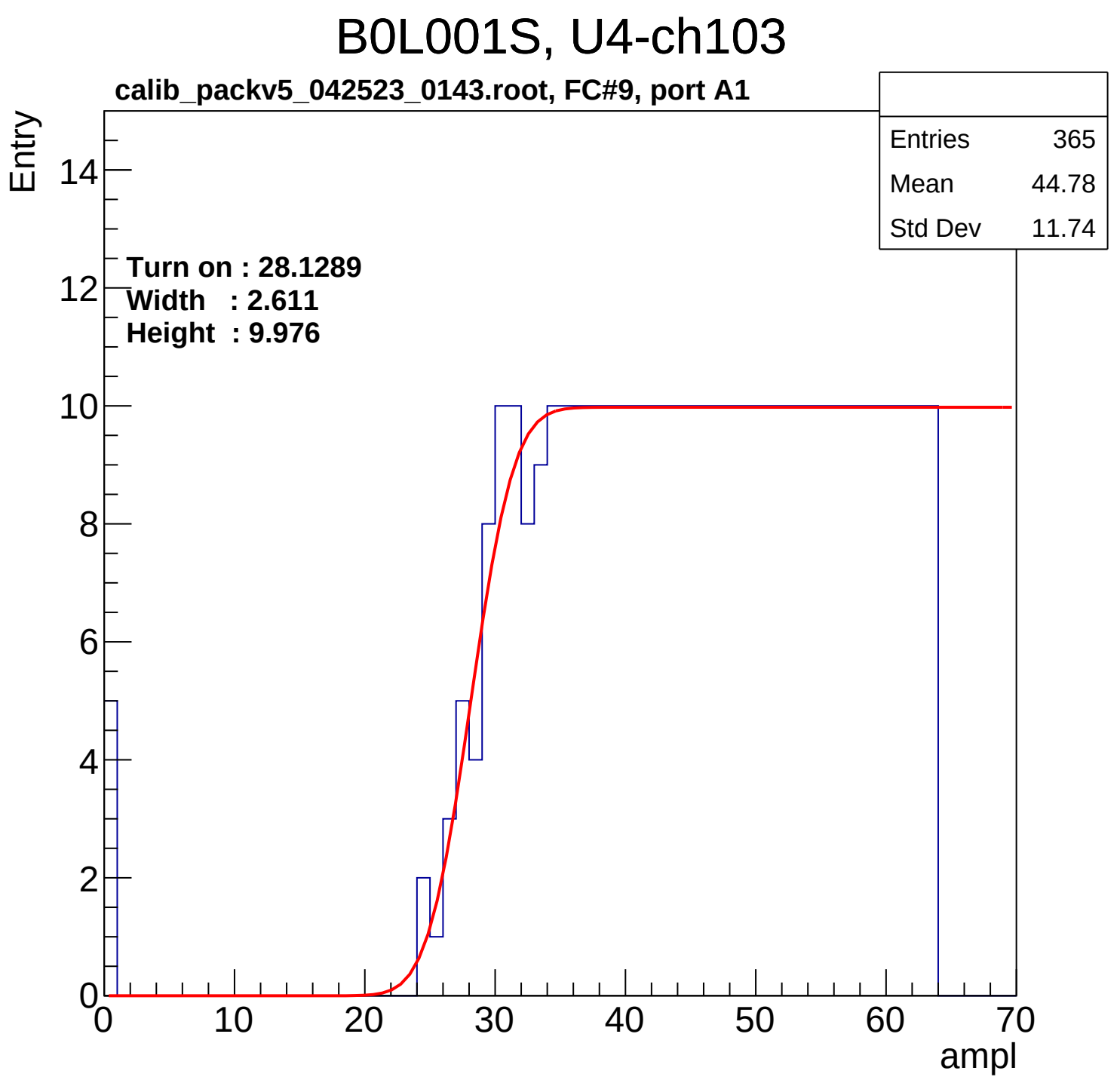
B0L001S, U4-ch103
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 44.78
Std Dev 11.74
Turn on : 28.1289
Width : 2.611
Height : 9.976
Entry
ampl
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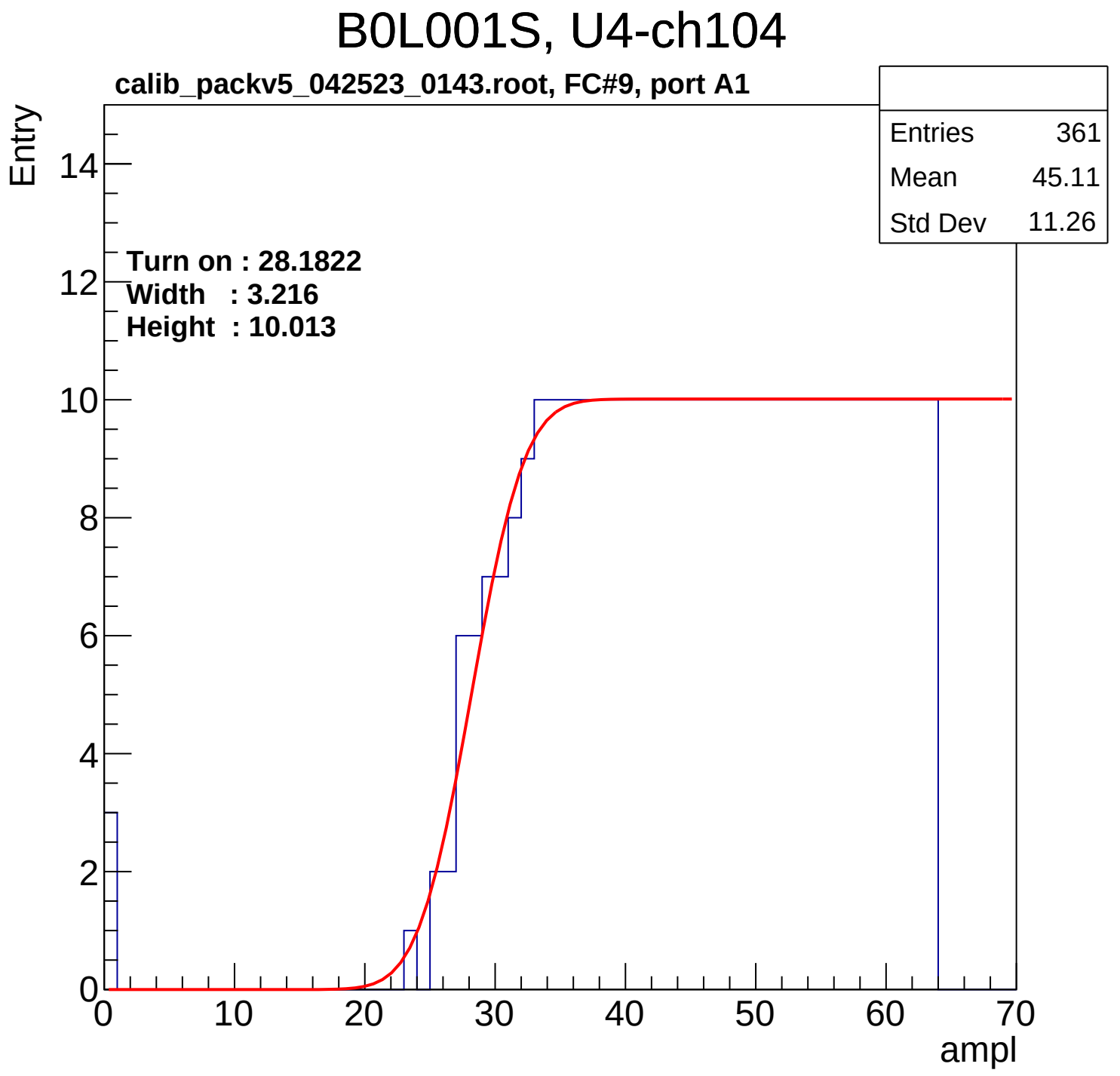
B0L001S, U4-ch104
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 45.11
Std Dev 11.26
Turn on : 28.1822
Width : 3.216
Height : 10.013
Entry
ampl
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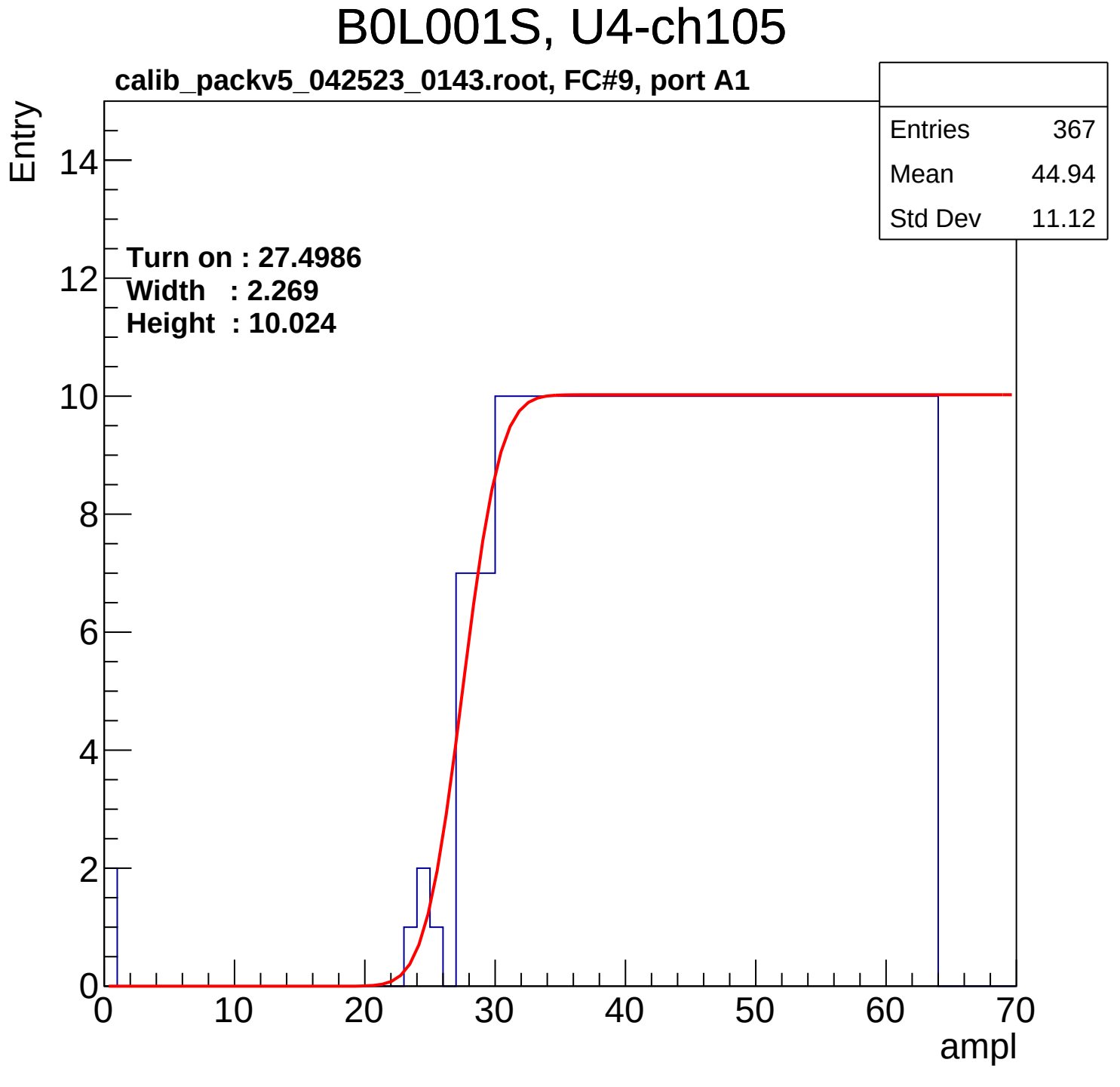
B0L001S, U4-ch105
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.94
Std Dev 11.12
Turn on : 27.4986
Width : 2.269
Height : 10.024
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ampl
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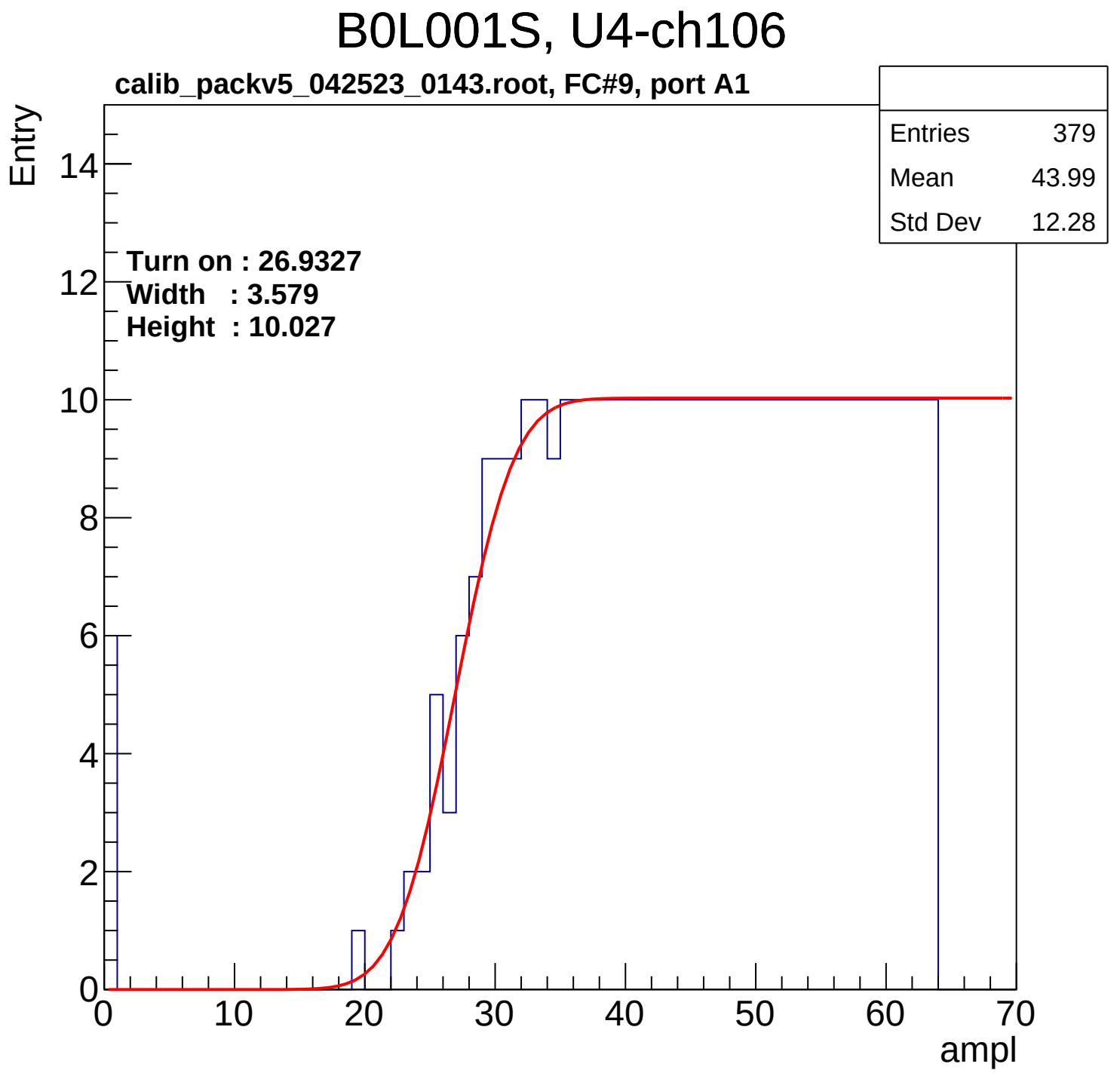
B0L001S, U4-ch106
calib_packv5_042523_0143.root, FC#9, port A1
Entries 379
Mean 43.99
Std Dev 12.28
Turn on : 26.9327
Width : 3.579
Height : 10.027
Entry
ampl
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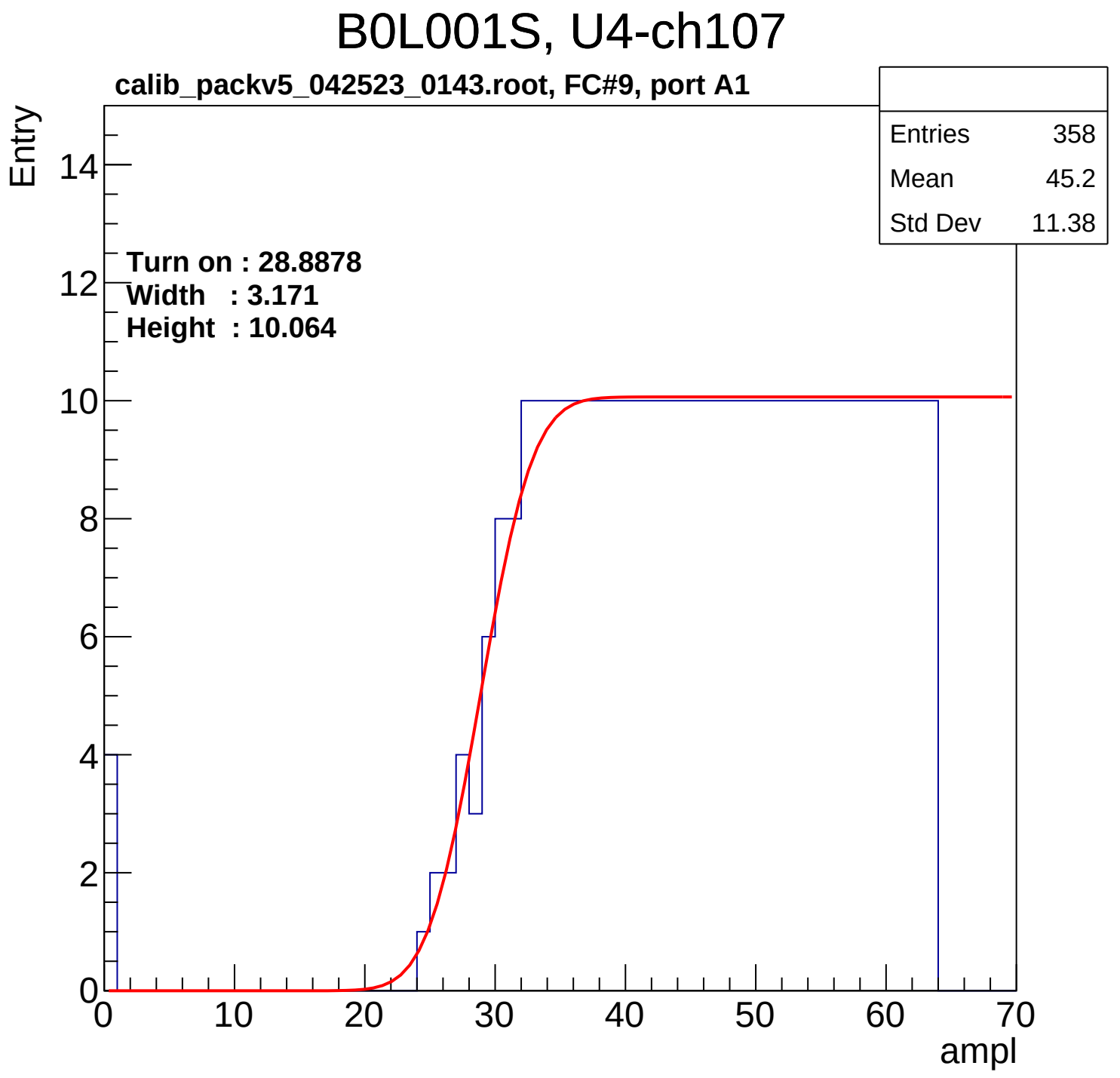
B0L001S, U4-ch107
calib_packv5_042523_0143.root, FC#9, port A1
Entries 358
Mean 45.2
Std Dev 11.38
Turn on : 28.8878
Width : 3.171
Height : 10.064
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ampl
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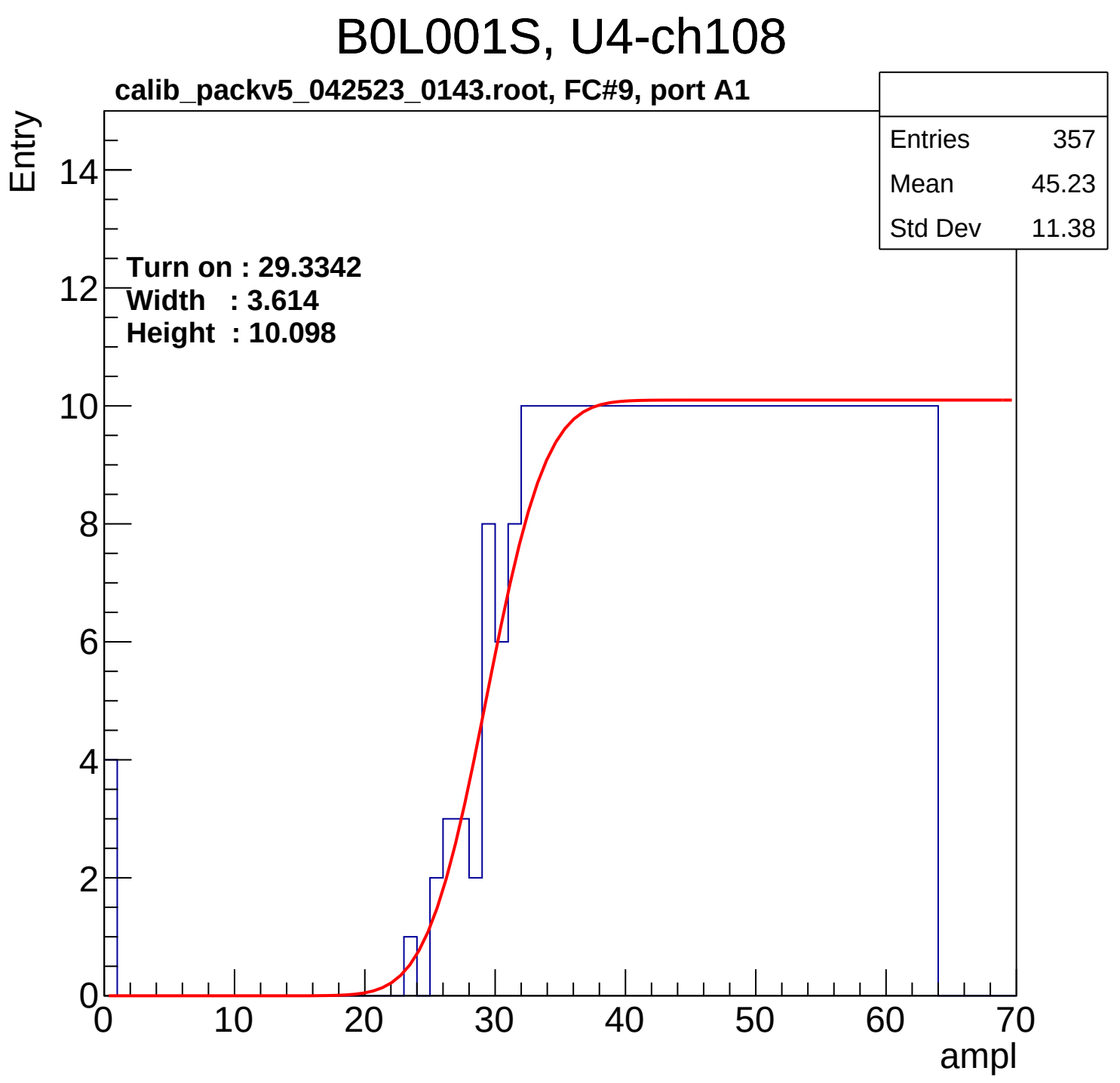
B0L001S, U4-ch108
calib_packv5_042523_0143.root, FC#9, port A1
Entries 357
Mean 45.23
Std Dev 11.38
Turn on : 29.3342
Width : 3.614
Height : 10.098
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ampl
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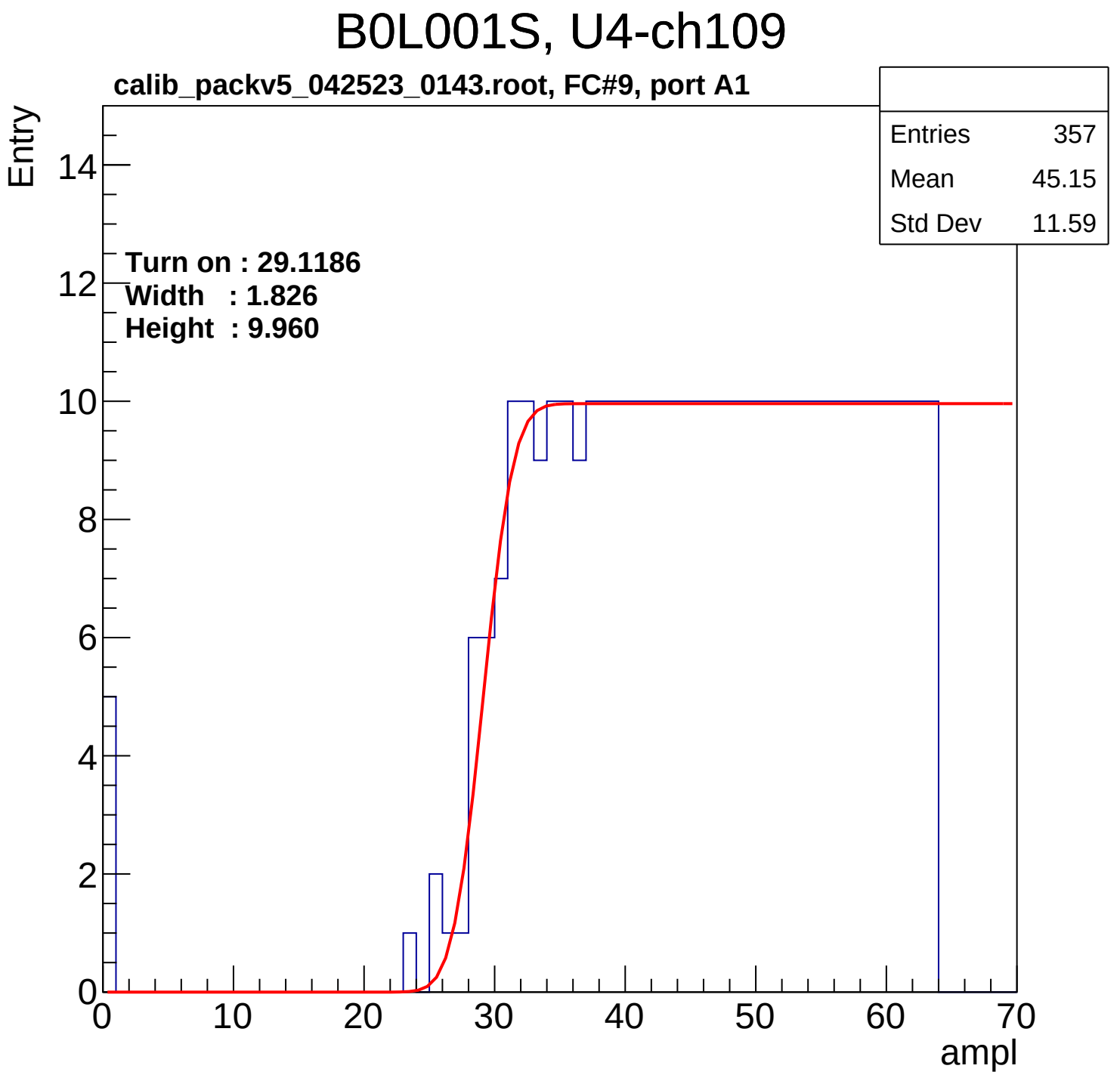
B0L001S, U4-ch109
calib_packv5_042523_0143.root, FC#9, port A1
Entries 357
Mean 45.15
Std Dev 11.59
Turn on : 29.1186
Width : 1.826
Height : 9.960
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ampl
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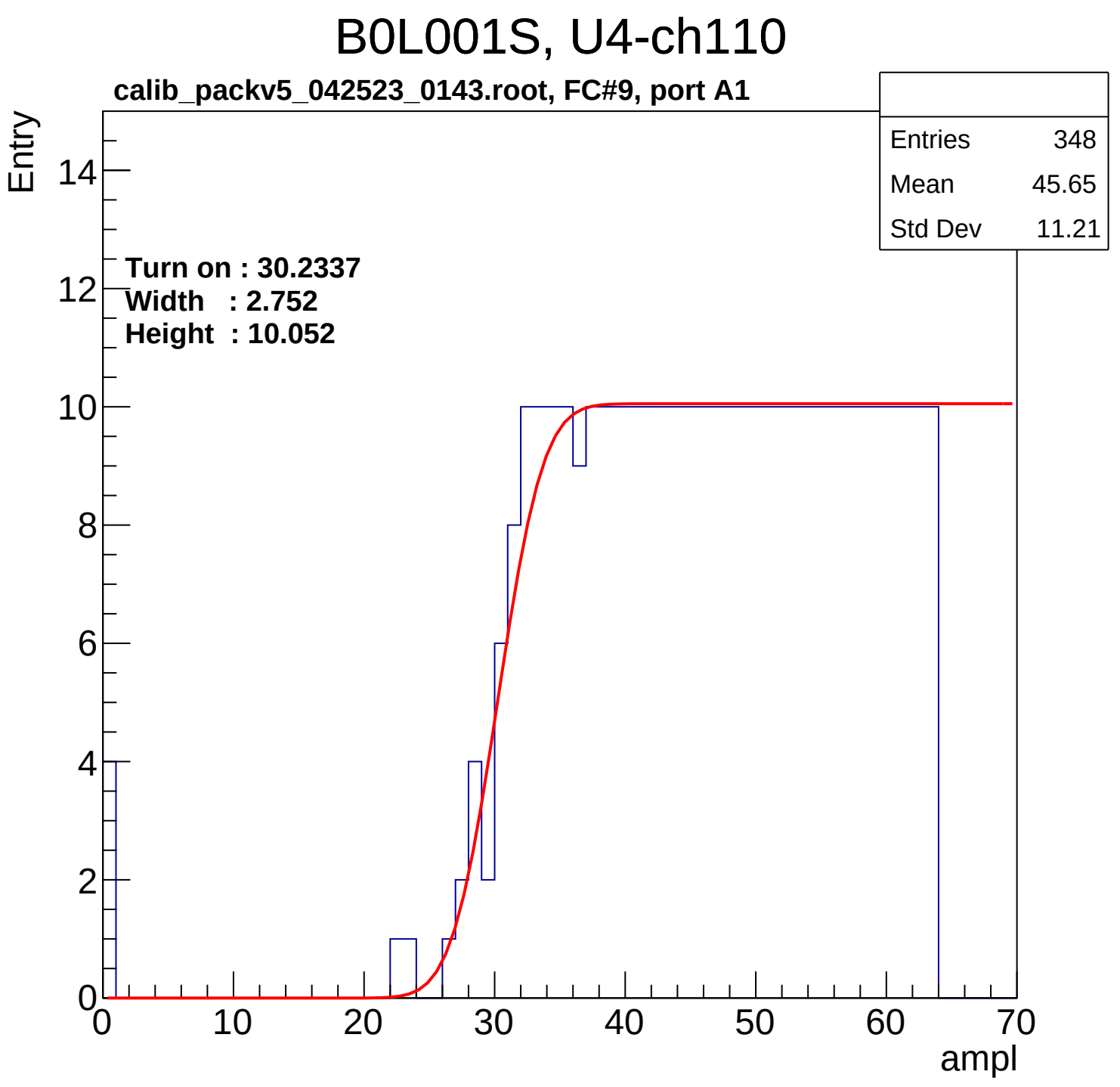
B0L001S, U4-ch110
calib_packv5_042523_0143.root, FC#9, port A1
Entries 348
Mean 45.65
Std Dev 11.21
Turn on : 30.2337
Width : 2.752
Height : 10.052
Entry
ampl
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8
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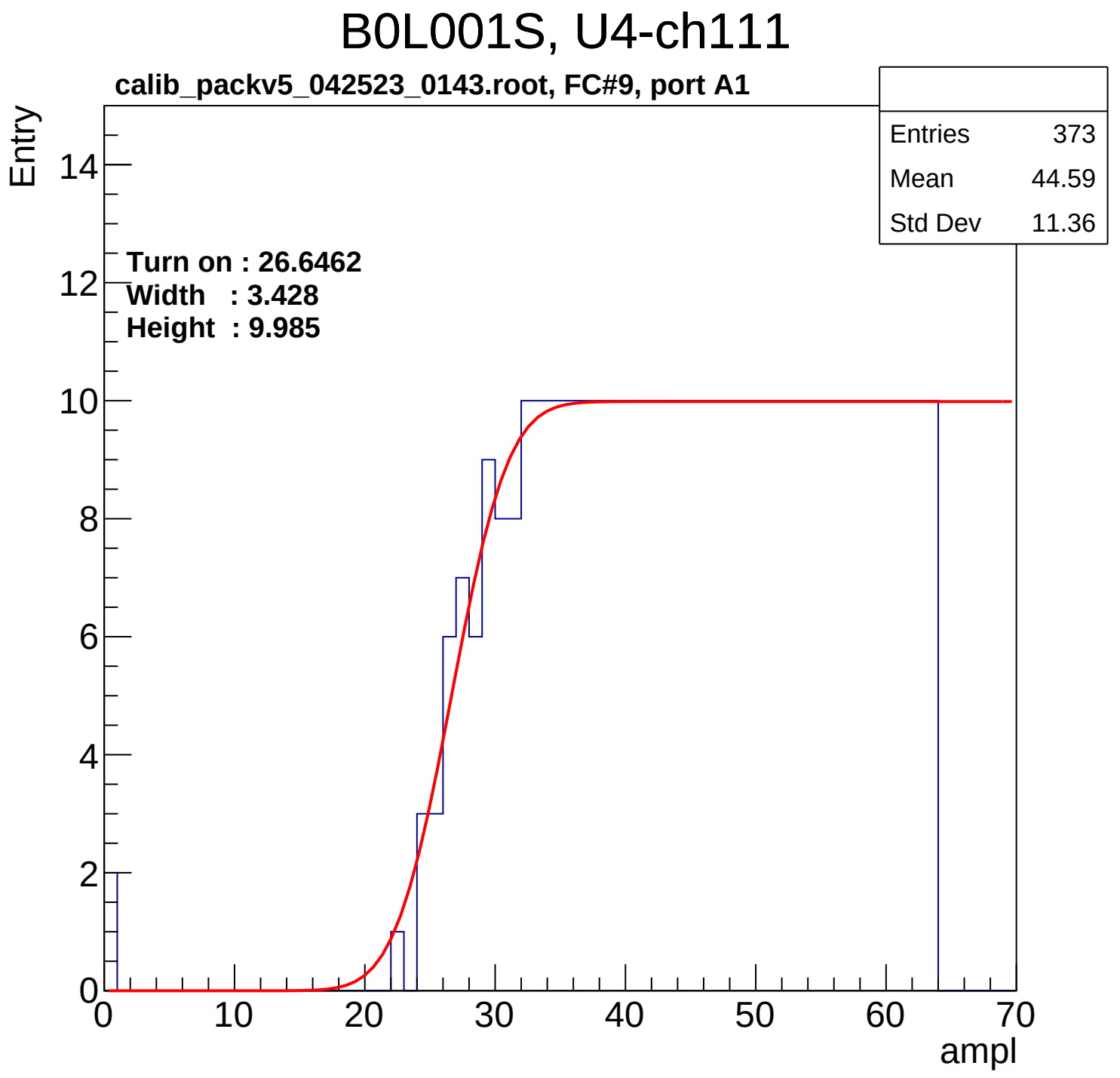
B0L001S, U4-ch111
calib_packv5_042523_0143.root, FC#9, port A1
Entries 373
Mean 44.59
Std Dev 11.36
Turn on : 26.6462
Width : 3.428
Height : 9.985
Entry
ampl
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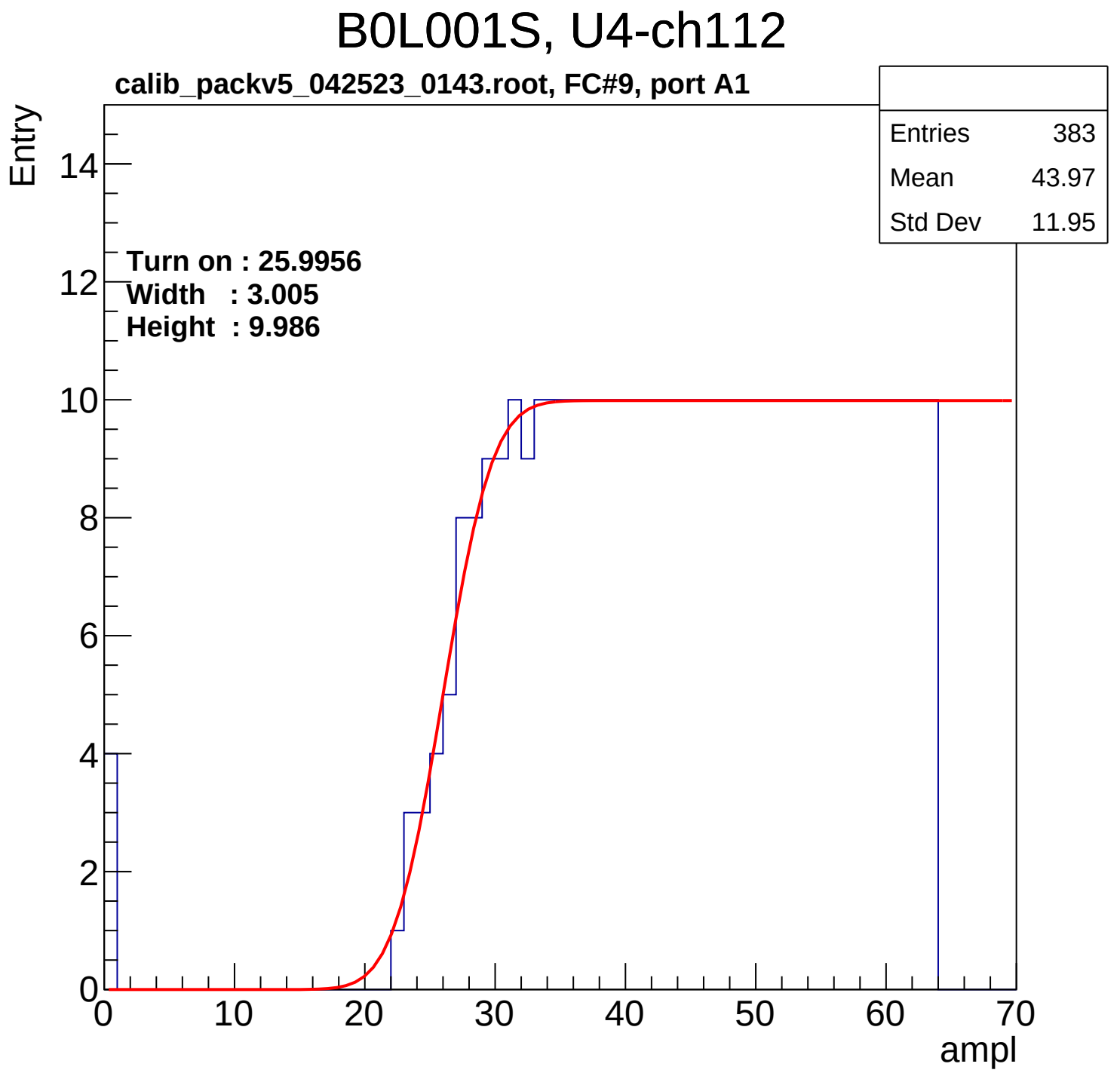
B0L001S, U4-ch112
calib_packv5_042523_0143.root, FC#9, port A1
Entries 383
Mean 43.97
Std Dev 11.95
Turn on : 25.9956
Width : 3.005
Height : 9.986
Entry
ampl
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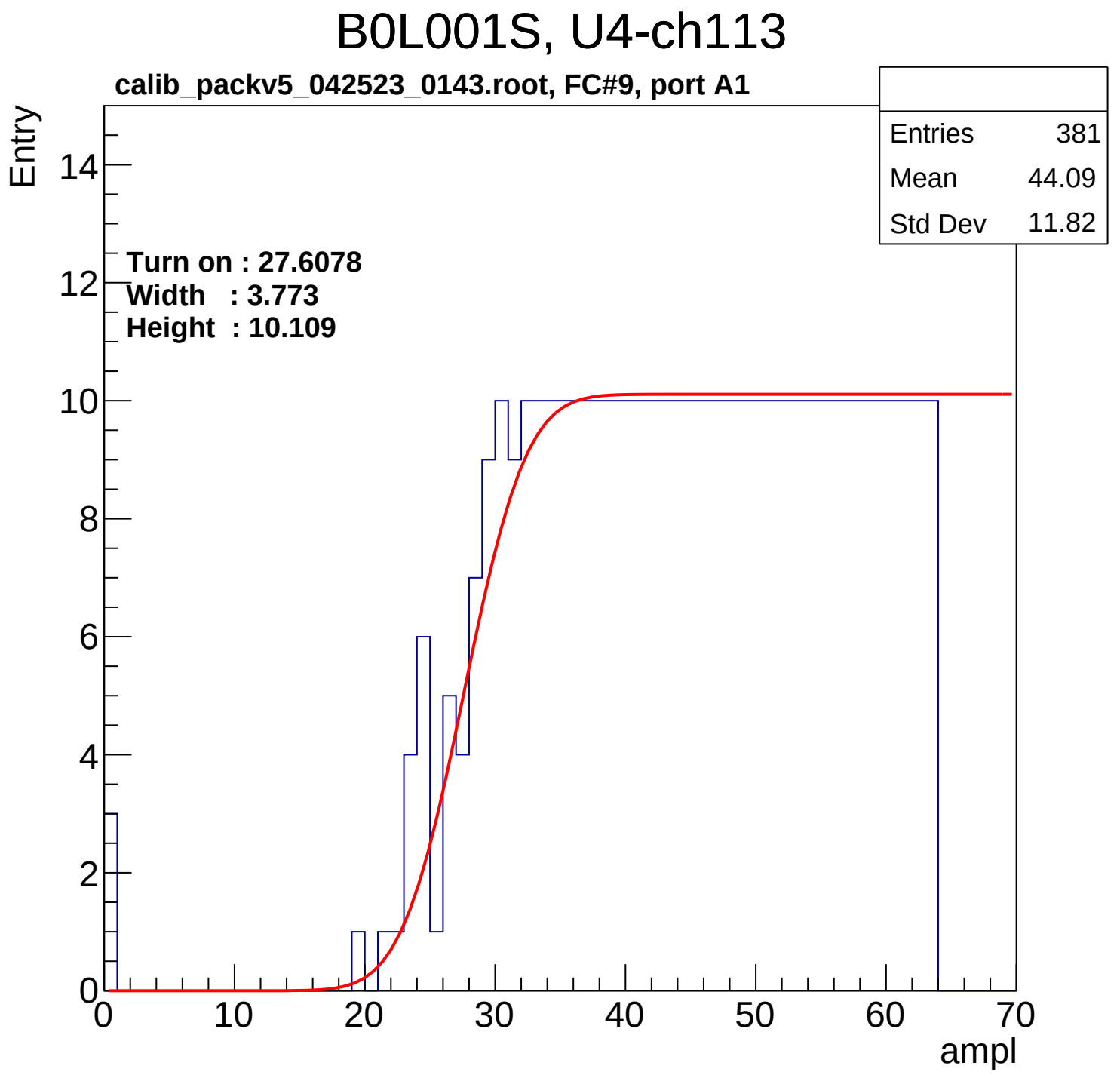
B0L001S, U4-ch113
calib_packv5_042523_0143.root, FC#9, port A1
Entries 381
Mean 44.09
Std Dev 11.82
Turn on : 27.6078
Width : 3.773
Height : 10.109
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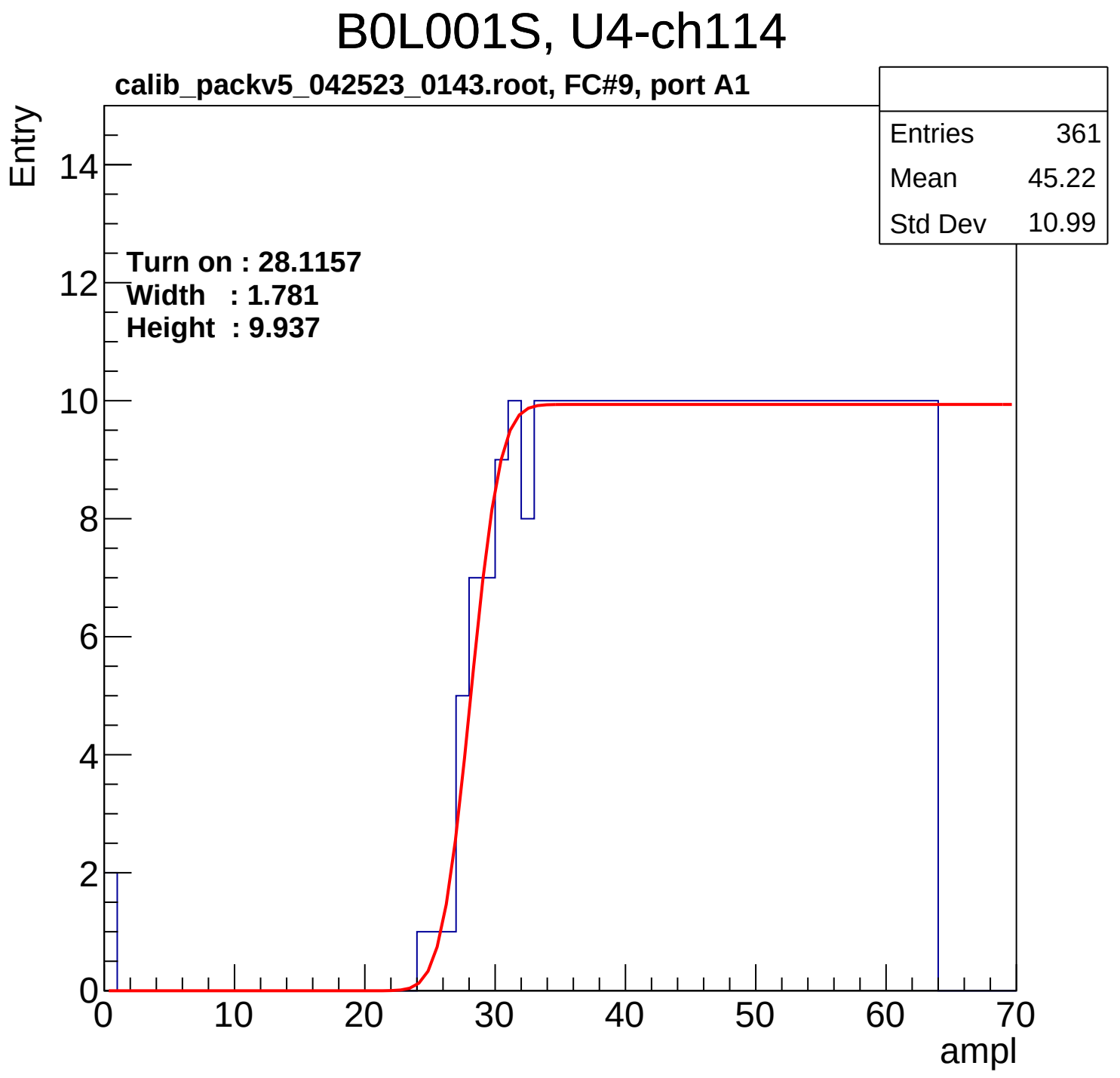
B0L001S, U4-ch114
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 45.22
Std Dev 10.99
Turn on : 28.1157
Width : 1.781
Height : 9.937
Entry
ampl
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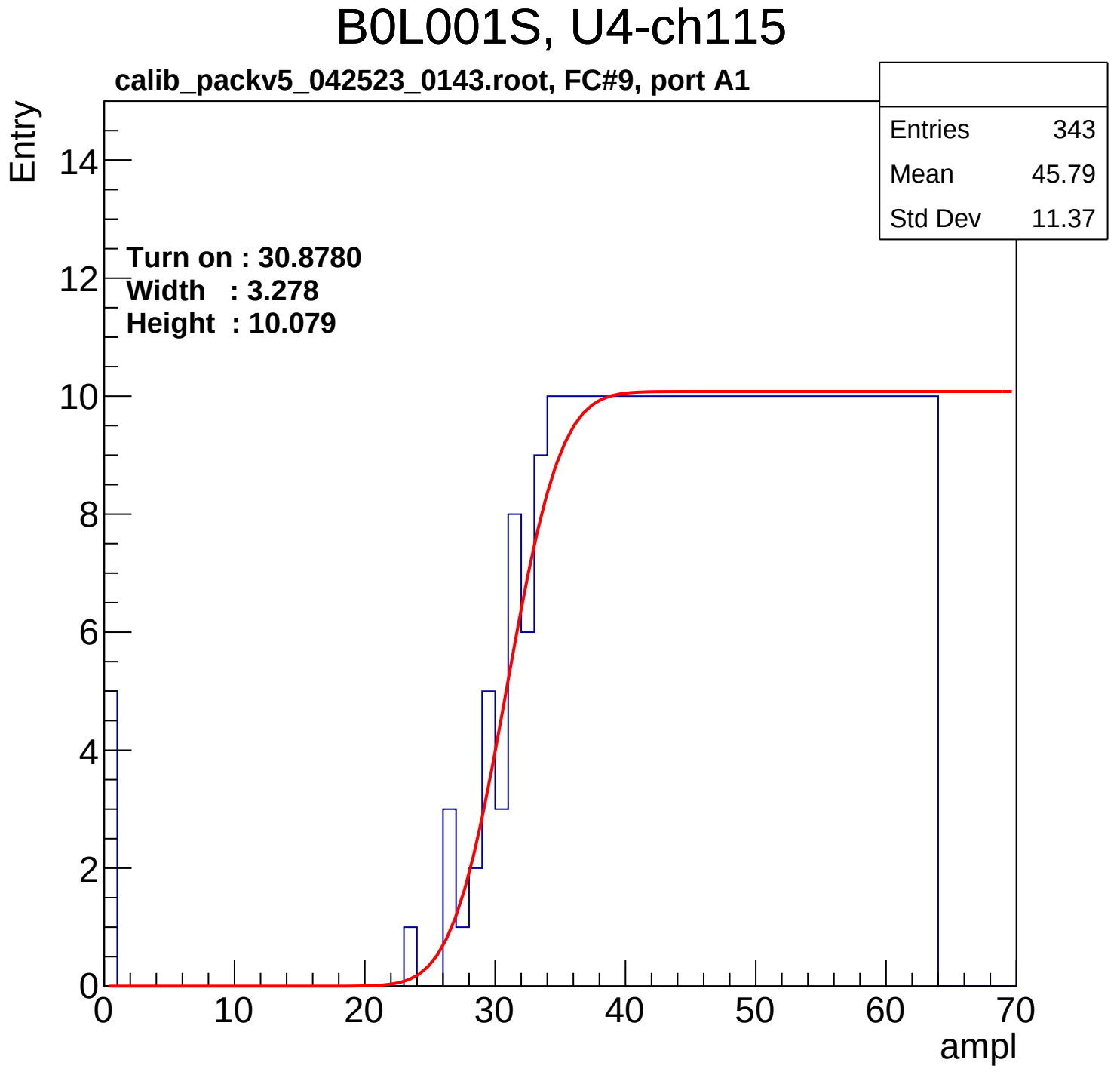
B0L001S, U4-ch115
calib_packv5_042523_0143.root, FC#9, port A1
Entries 343
Mean 45.79
Std Dev 11.37
Turn on : 30.8780
Width : 3.278
Height : 10.079
Entry
ampl
0
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4
6
8
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12
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10
20
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40
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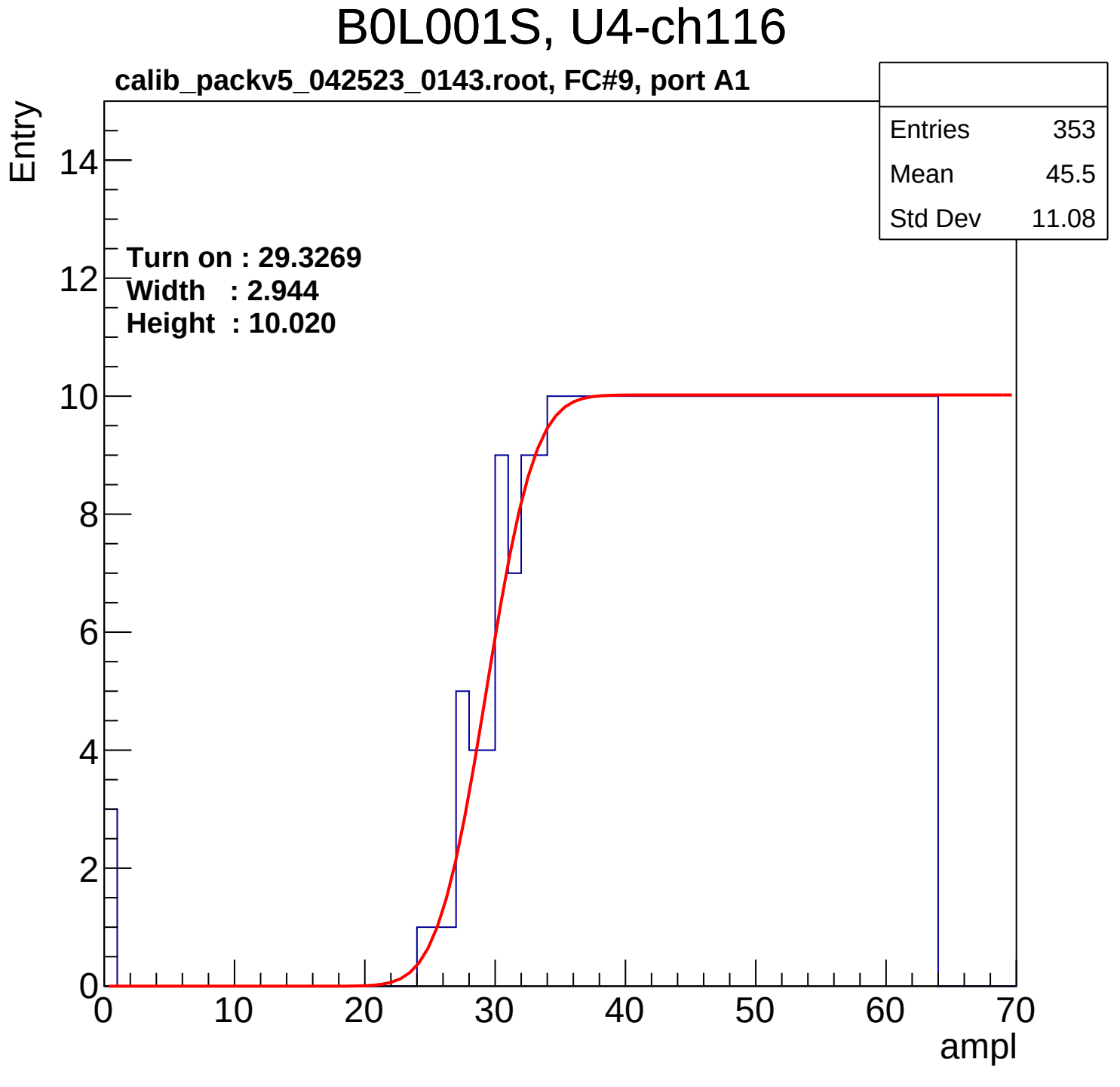
B0L001S, U4-ch116
calib_packv5_042523_0143.root, FC#9, port A1
Entries 353
Mean 45.5
Std Dev 11.08
Turn on : 29.3269
Width : 2.944
Height : 10.020
Entry
ampl
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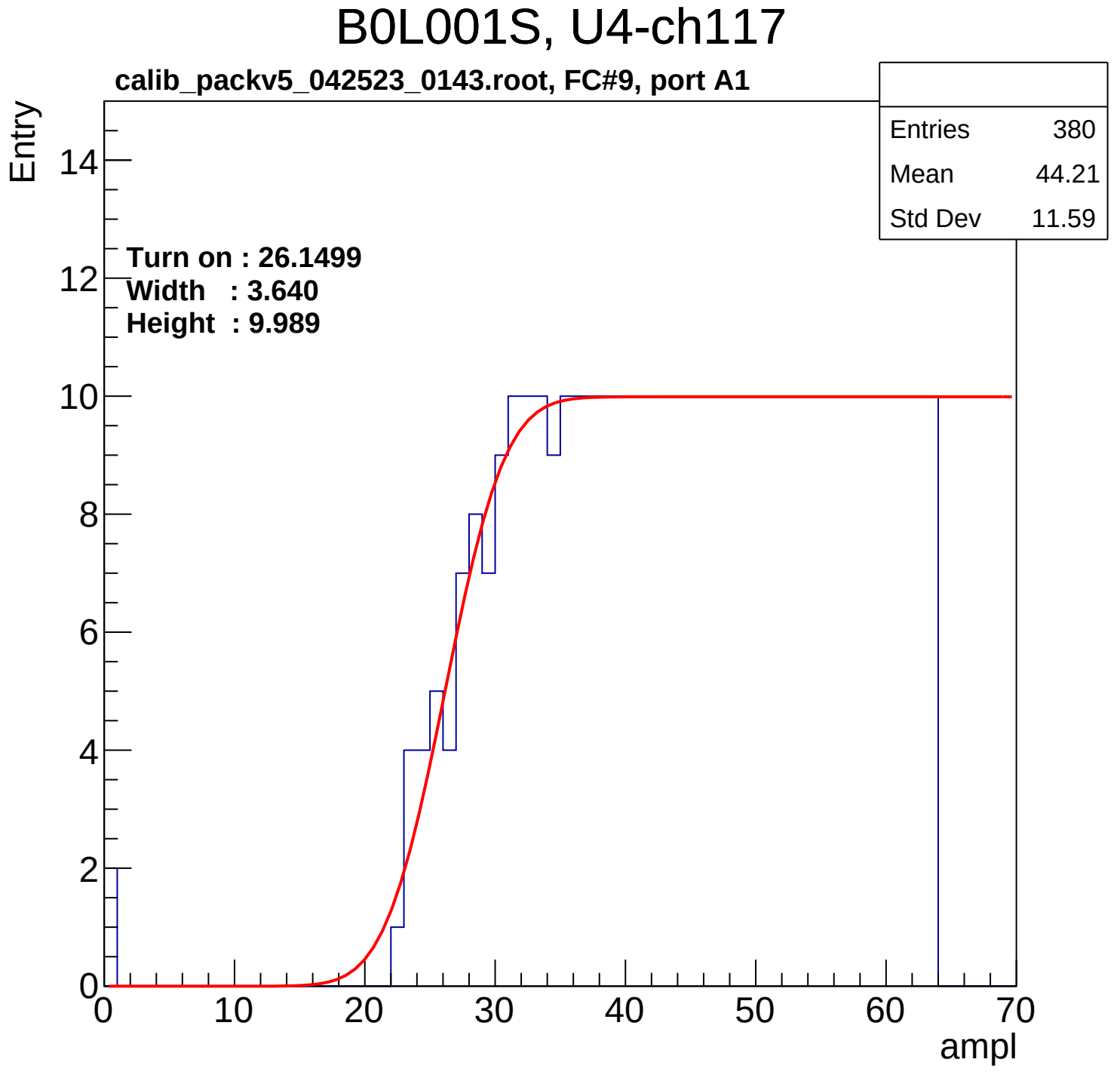
B0L001S, U4-ch117
calib_packv5_042523_0143.root, FC#9, port A1
Entries 380
Mean 44.21
Std Dev 11.59
Turn on : 26.1499
Width : 3.640
Height : 9.989
Entry
ampl
0
2
4
6
8
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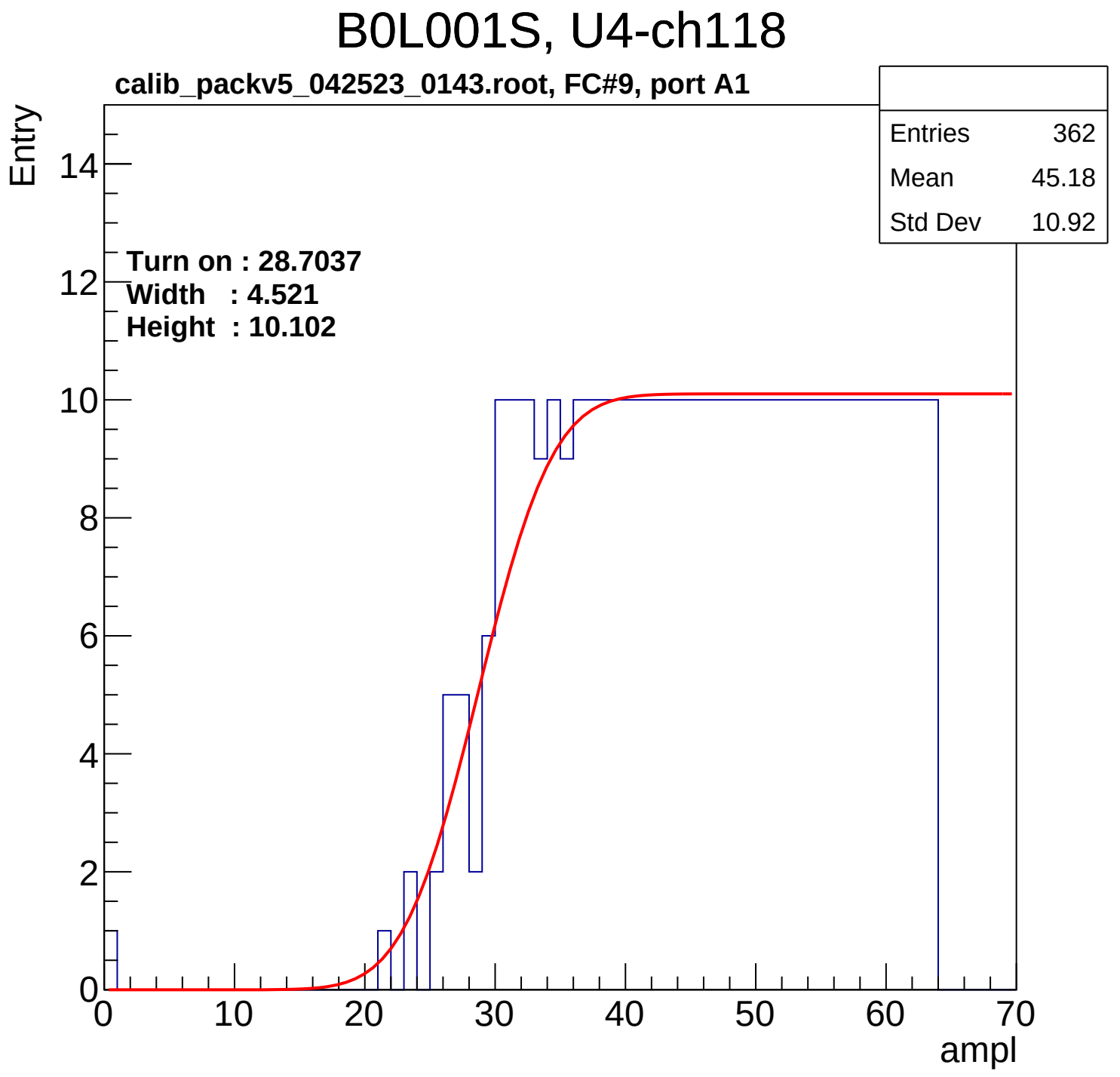
B0L001S, U4-ch118
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 45.18
Std Dev 10.92
Turn on : 28.7037
Width : 4.521
Height : 10.102
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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60
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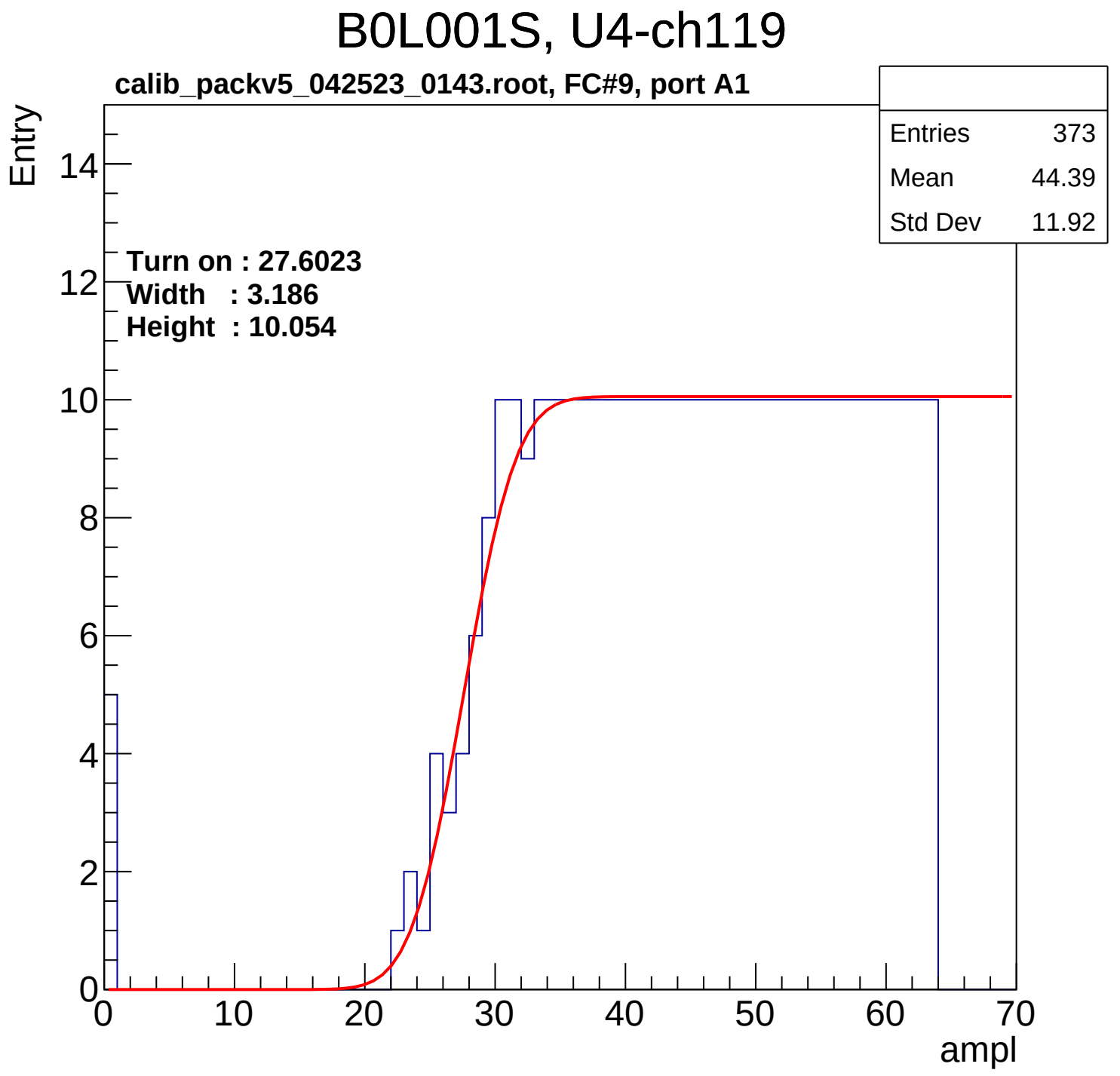
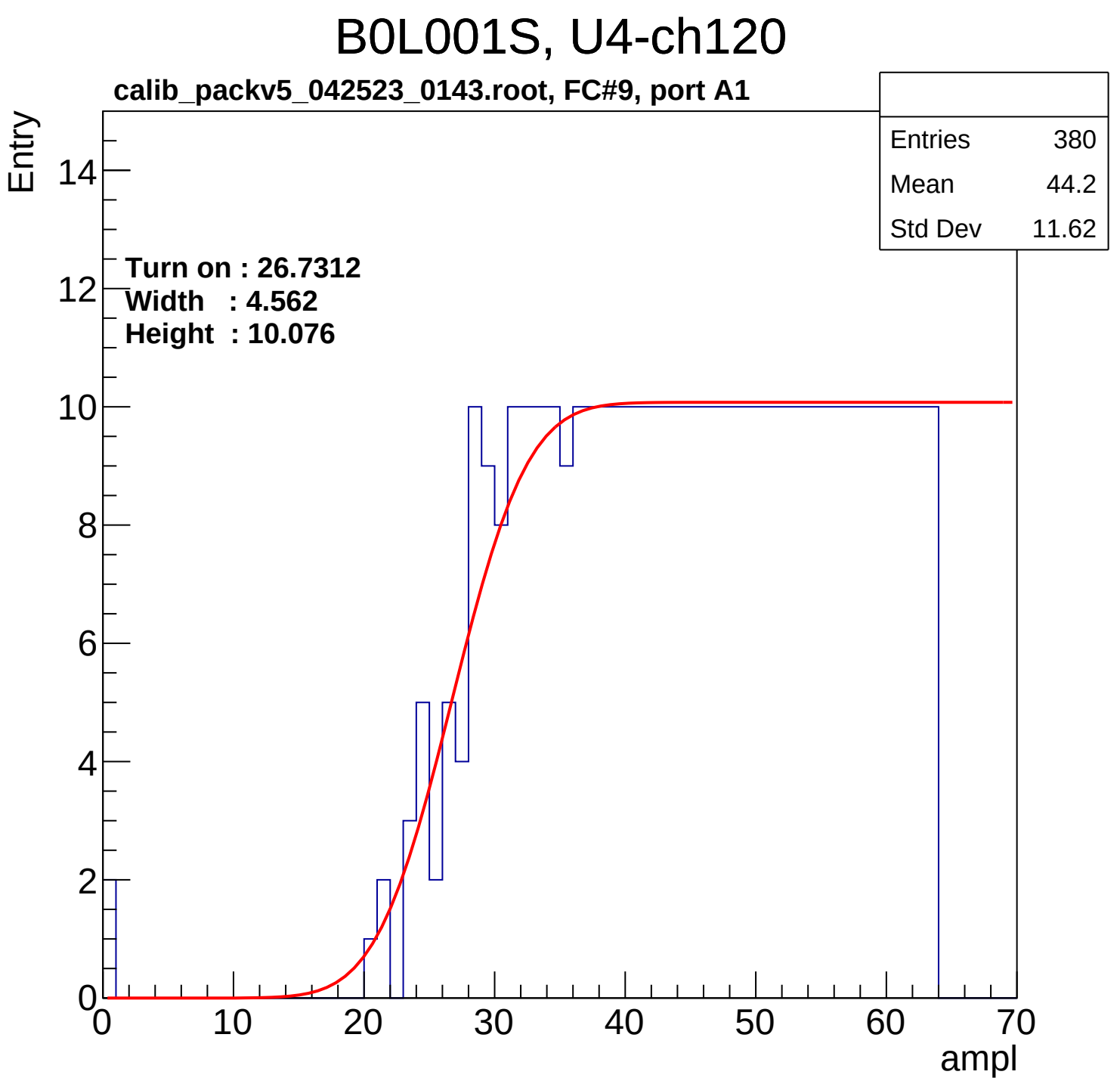

B0L001S, U4-ch119
calib_packv5_042523_0143.root, FC#9, port A1
Entries 373
Mean 44.39
Std Dev 11.92
Turn on : 27.6023
Width : 3.186
Height : 10.054
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U4-ch120
calib_packv5_042523_0143.root, FC#9, port A1
Entries 380
Mean 44.2
Std Dev 11.62
Turn on : 26.7312
Width : 4.562
Height : 10.076
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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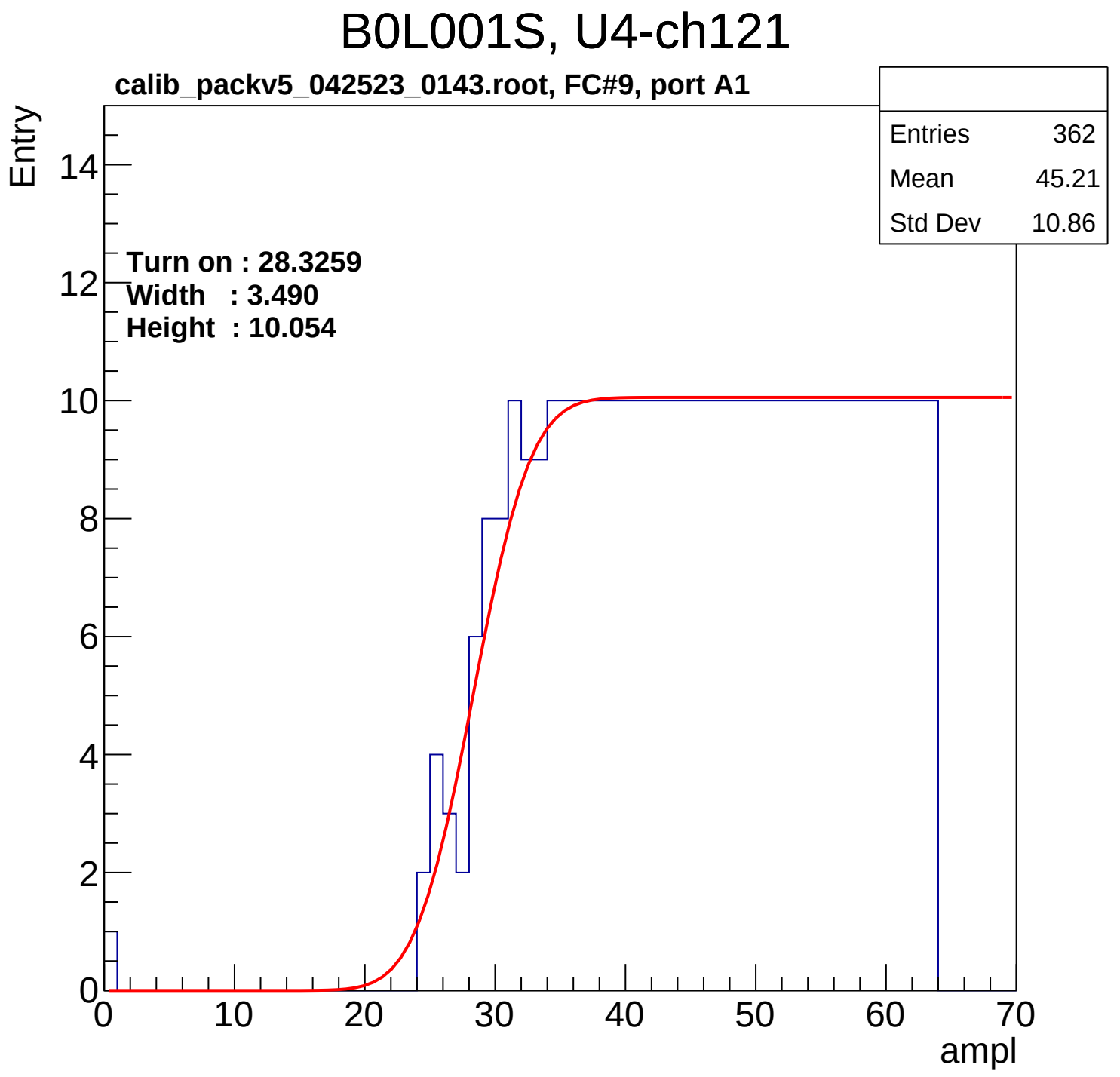
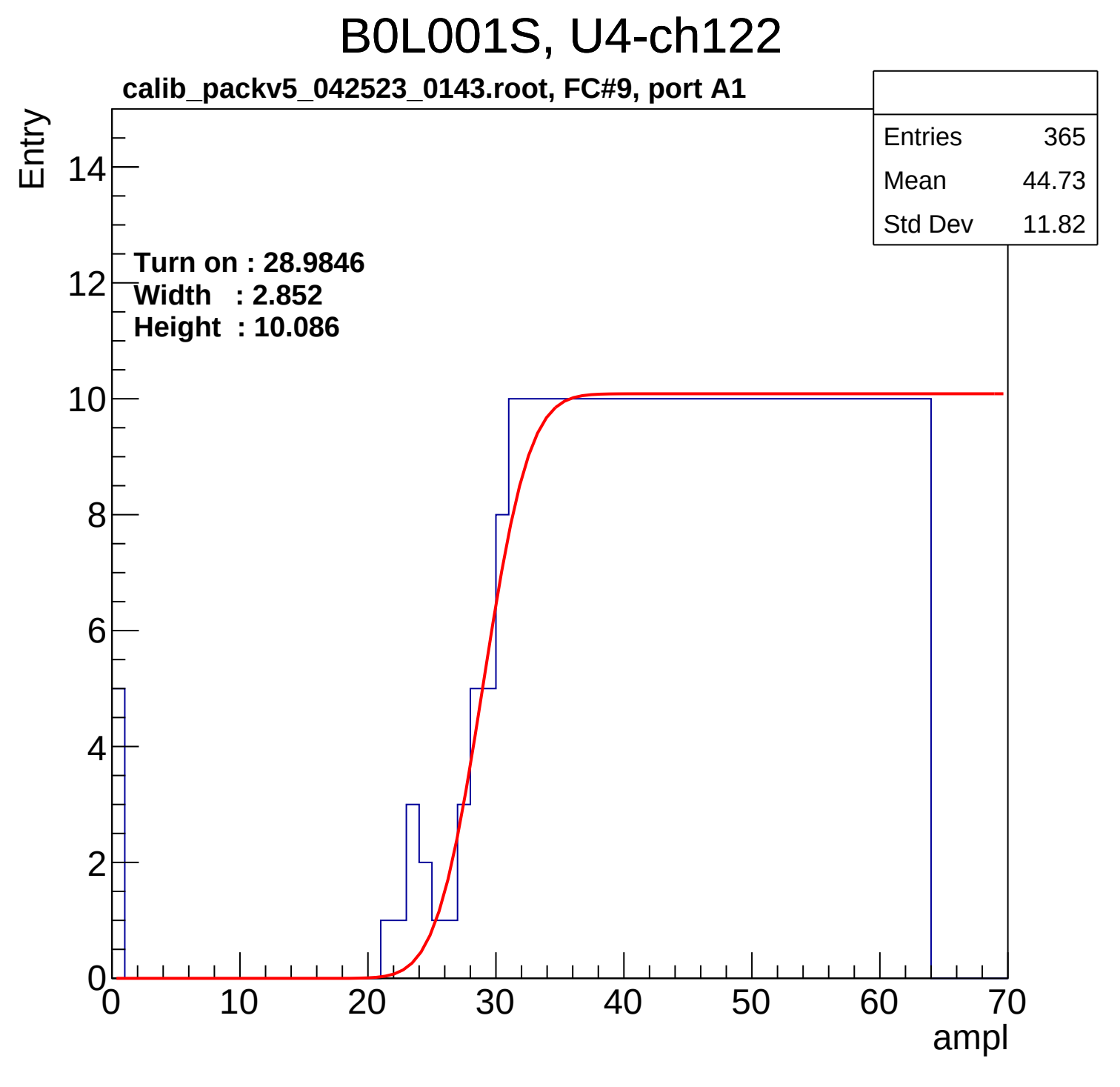

B0L001S, U4-ch121
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 45.21
Std Dev 10.86
Turn on : 28.3259
Width : 3.490
Height : 10.054
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U4-ch122
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 44.73
Std Dev 11.82
Turn on : 28.9846
Width : 2.852
Height : 10.086
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
30
40
50
60
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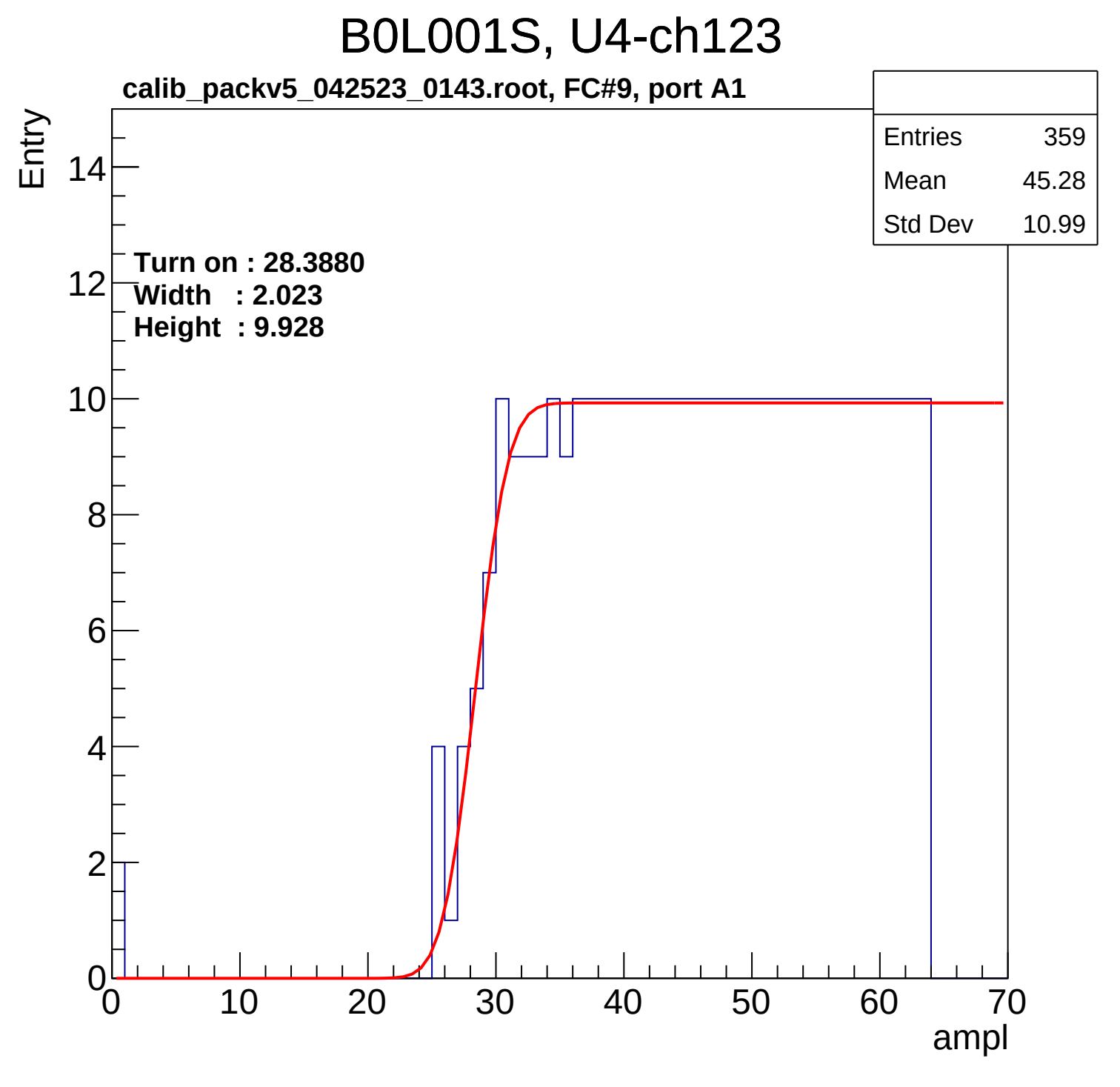
B0L001S, U4-ch123
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 45.28
Std Dev 10.99
Turn on : 28.3880
Width : 2.023
Height : 9.928
Entry
ampl
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2
4
6
8
10
12
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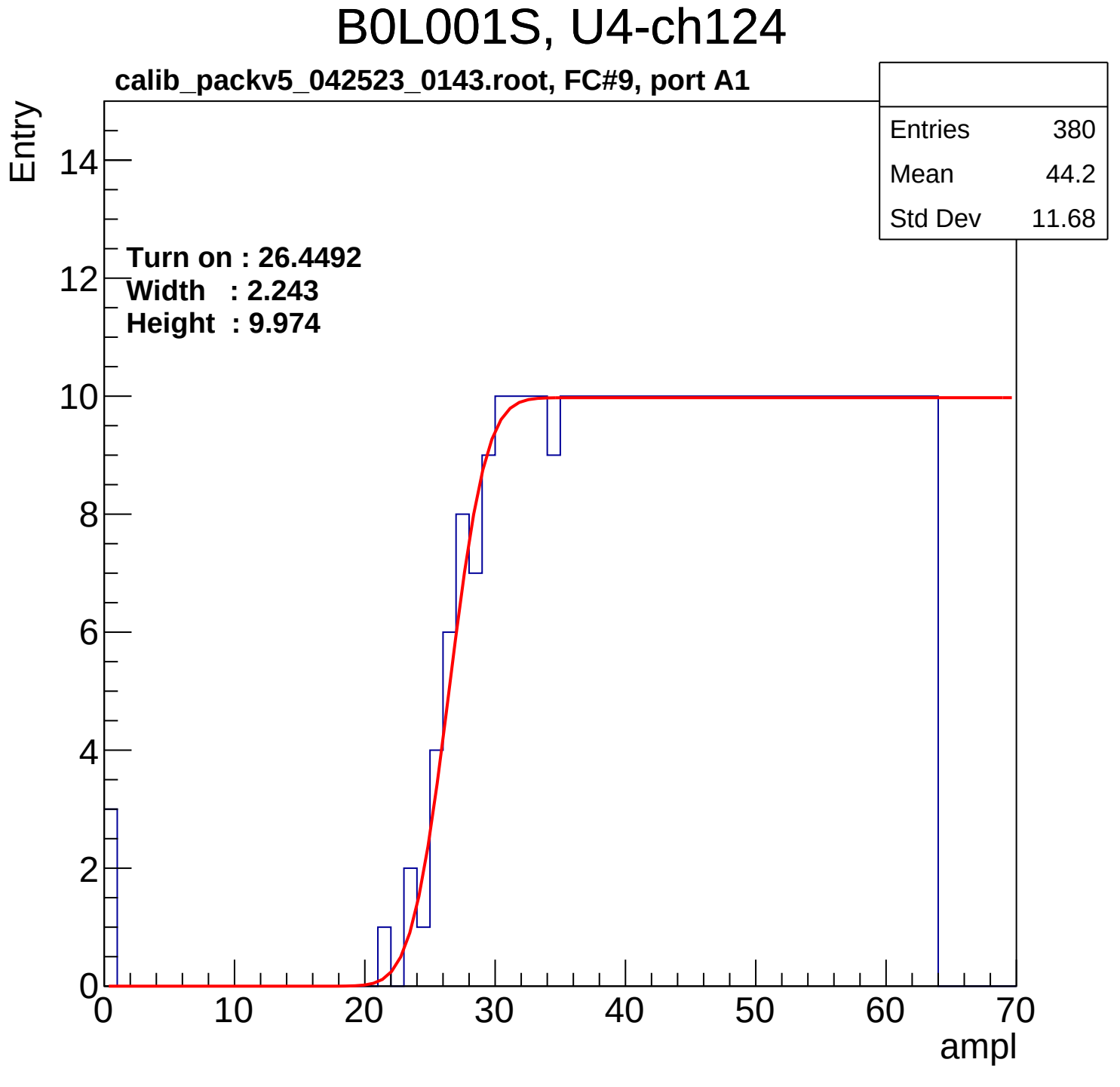
0
10
20
30
40
50
60
70


B0L001S, U4-ch124
calib_packv5_042523_0143.root, FC#9, port A1
Entries 380
Mean 44.2
Std Dev 11.68
Turn on : 26.4492
Width : 2.243
Height : 9.974
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
30
40
50
60
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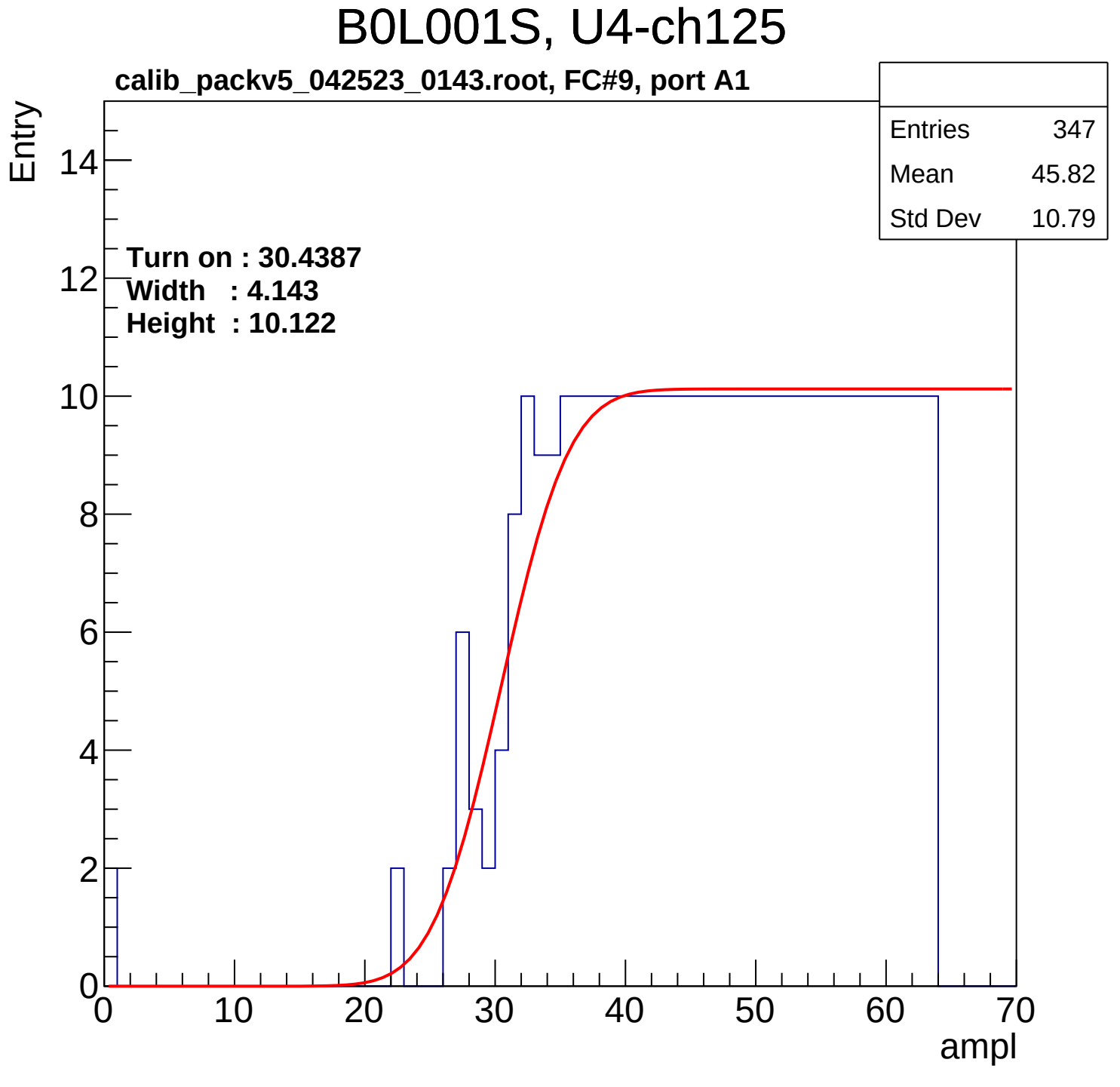
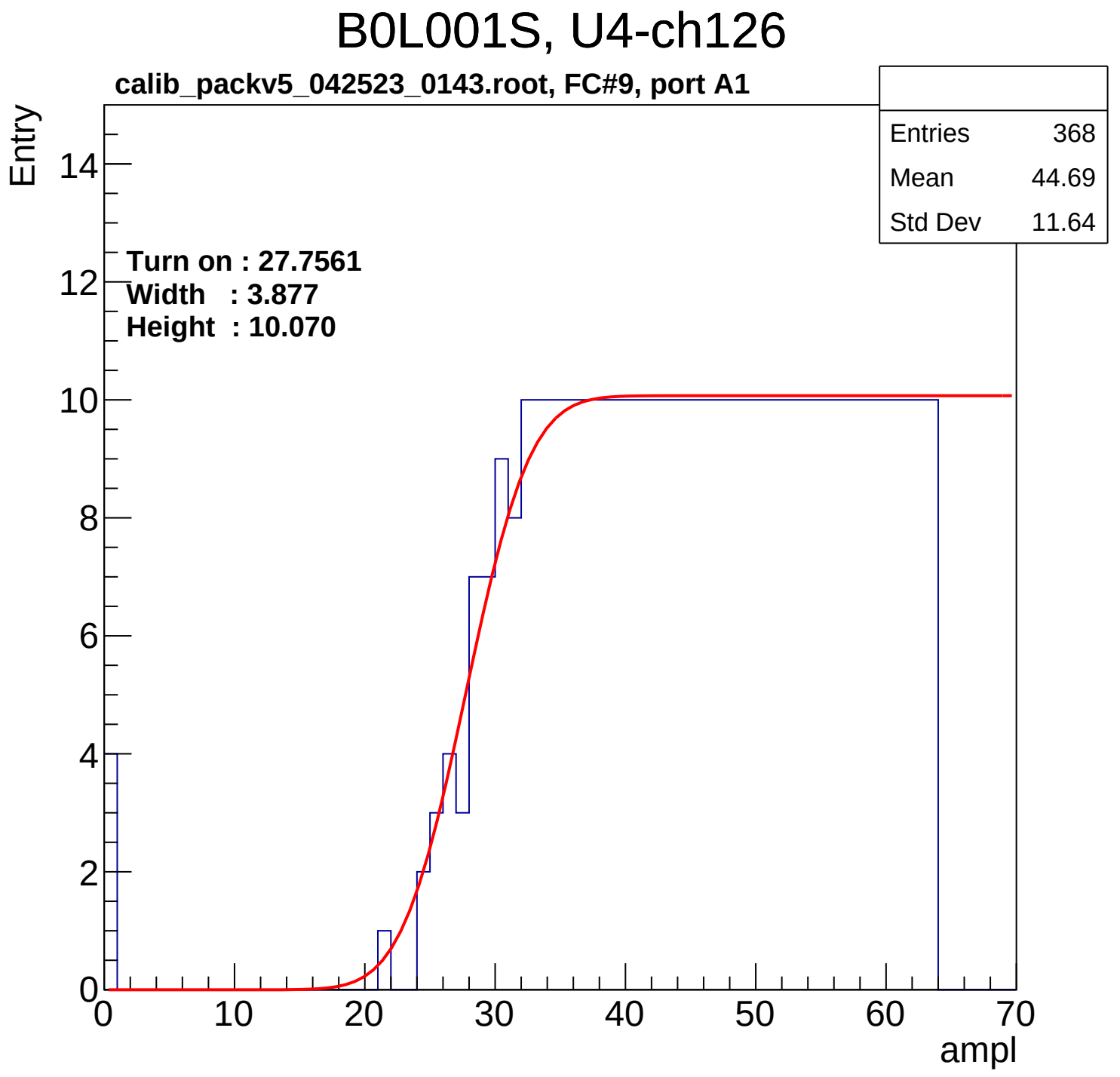

B0L001S, U4-ch125
calib_packv5_042523_0143.root, FC#9, port A1
Entries 347
Mean 45.82
Std Dev 10.79
Turn on : 30.4387
Width : 4.143
Height : 10.122
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U4-ch126
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.69
Std Dev 11.64
Turn on : 27.7561
Width : 3.877
Height : 10.070
Entry
ampl
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4
6
8
10
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0
10
20
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60
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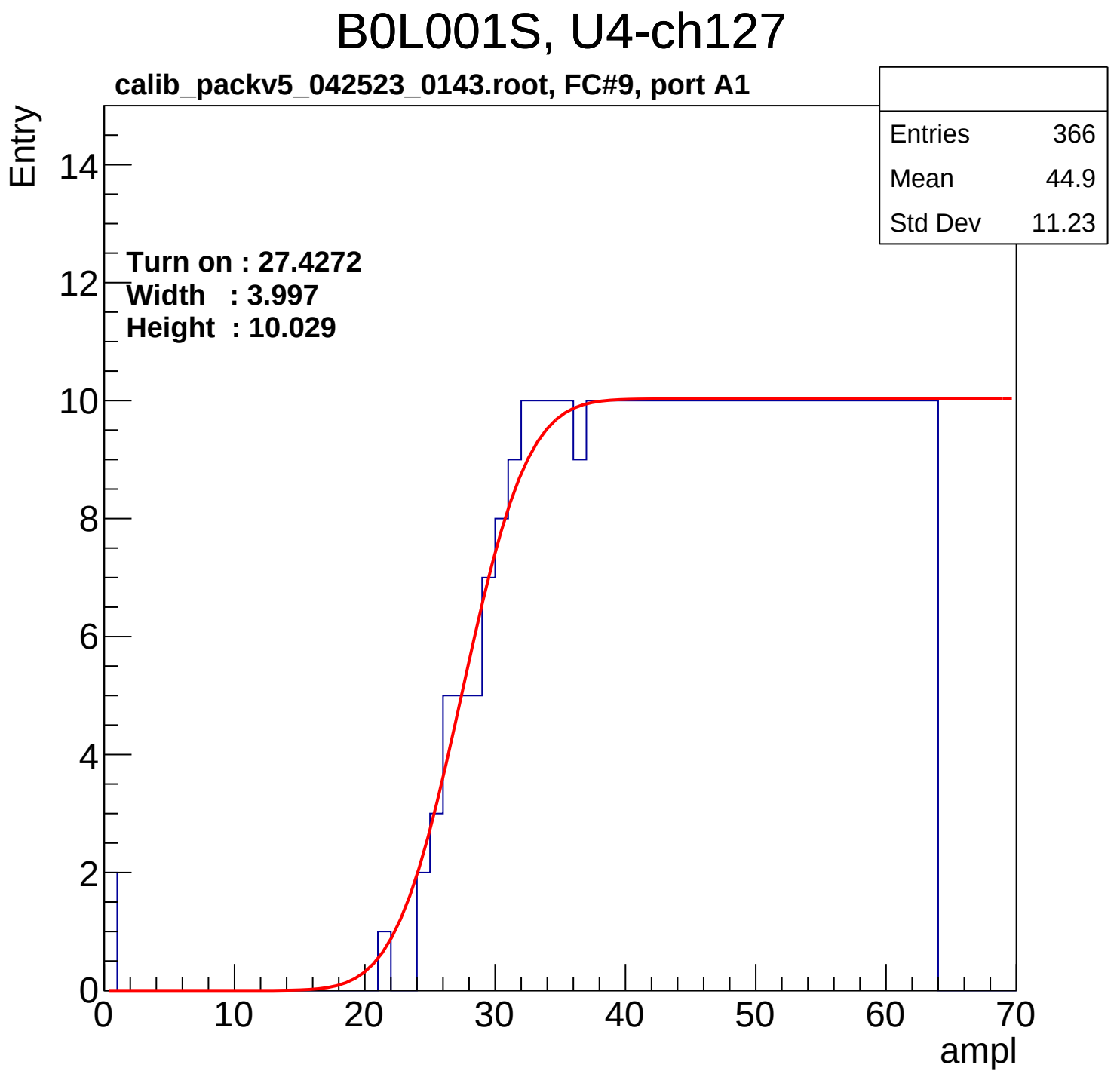
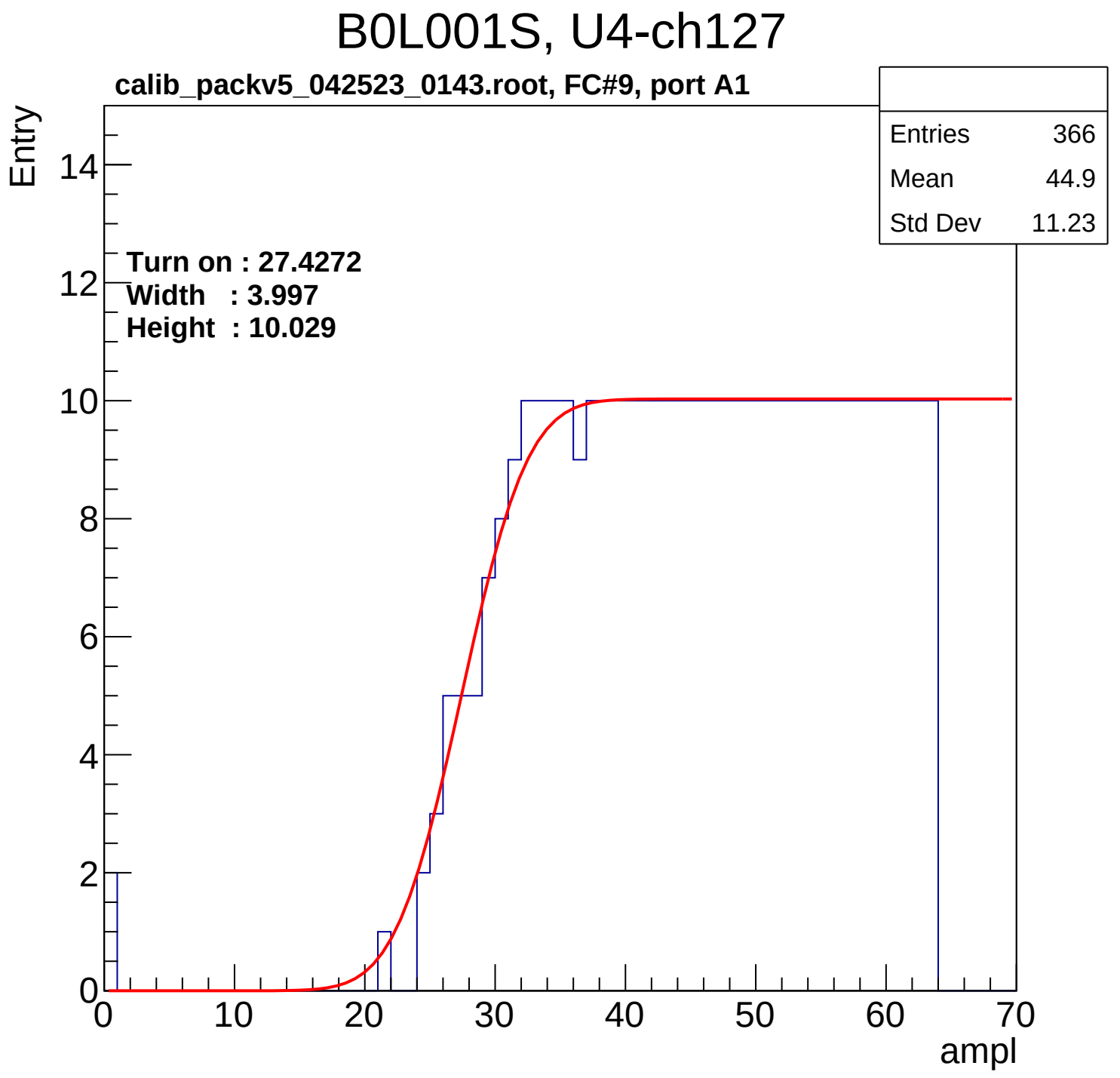

B0L001S, U4-ch127
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.9
Std Dev 11.23
Turn on : 27.4272
Width : 3.997
Height : 10.029
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U4-ch127
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.9
Std Dev 11.23
Turn on : 27.4272
Width : 3.997
Height : 10.029
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
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70