

B0L001S, U17-ch0

calib_packv5_042523_0143.root, FC#9, port A1

Entries	364
Mean	45.12
Std Dev	10.91

Turn on : 28.1707

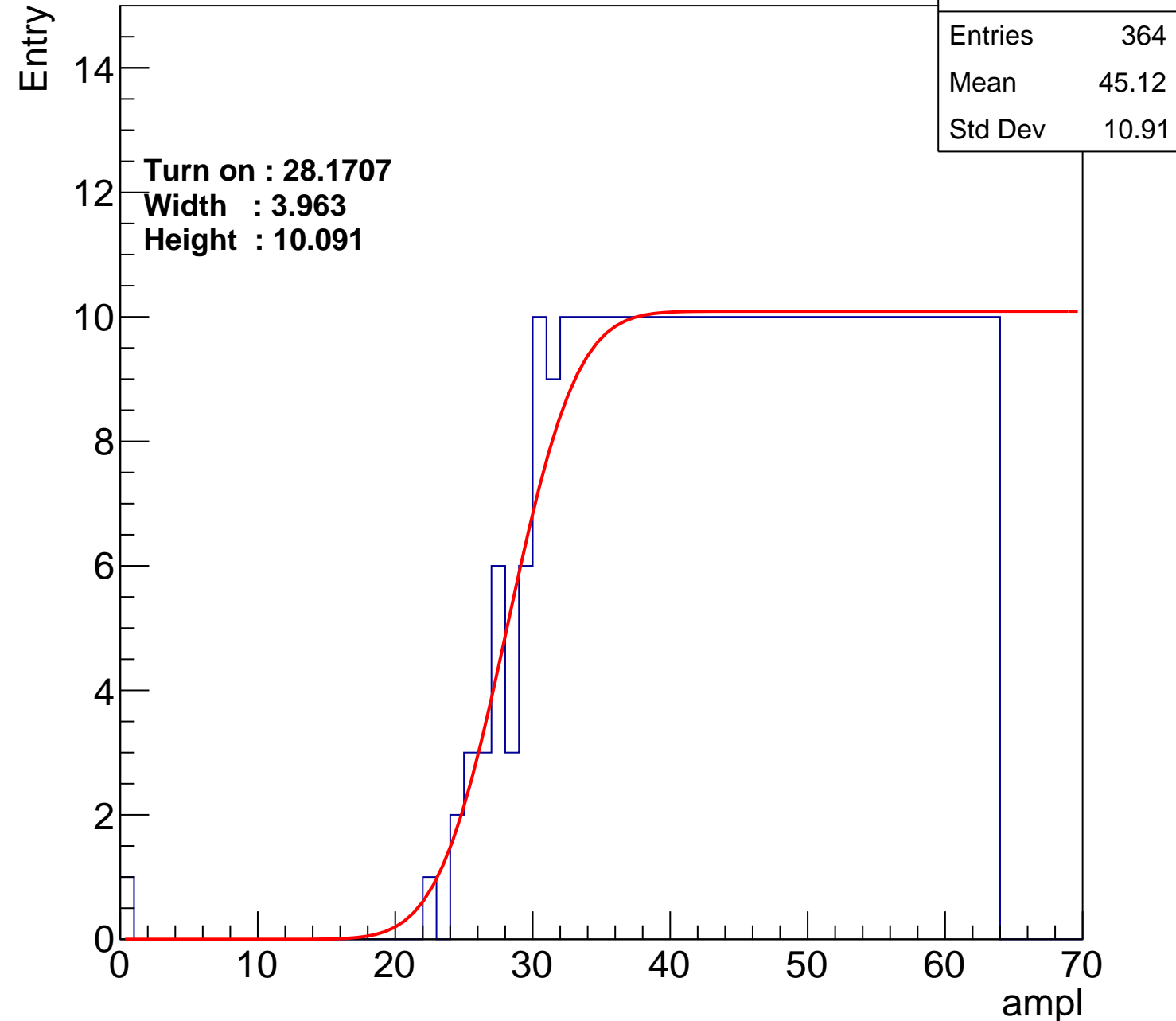
Width : 3.963

Height : 10.091

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch1

calib_packv5_042523_0143.root, FC#9, port A1

Entries	373
Mean	44.66
Std Dev	11.25

Turn on : 26.9100

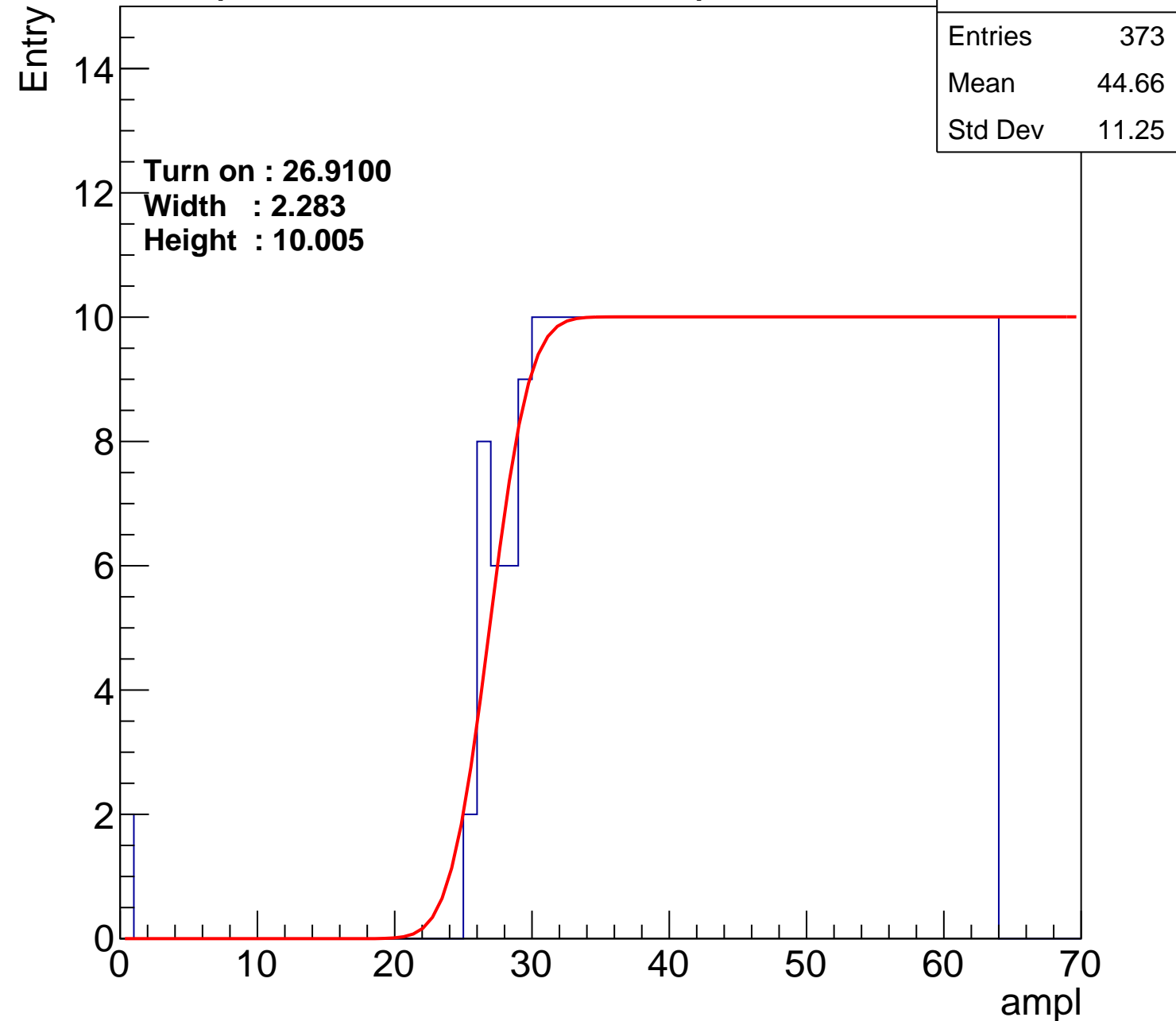
Width : 2.283

Height : 10.005

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch2

calib_packv5_042523_0143.root, FC#9, port A1

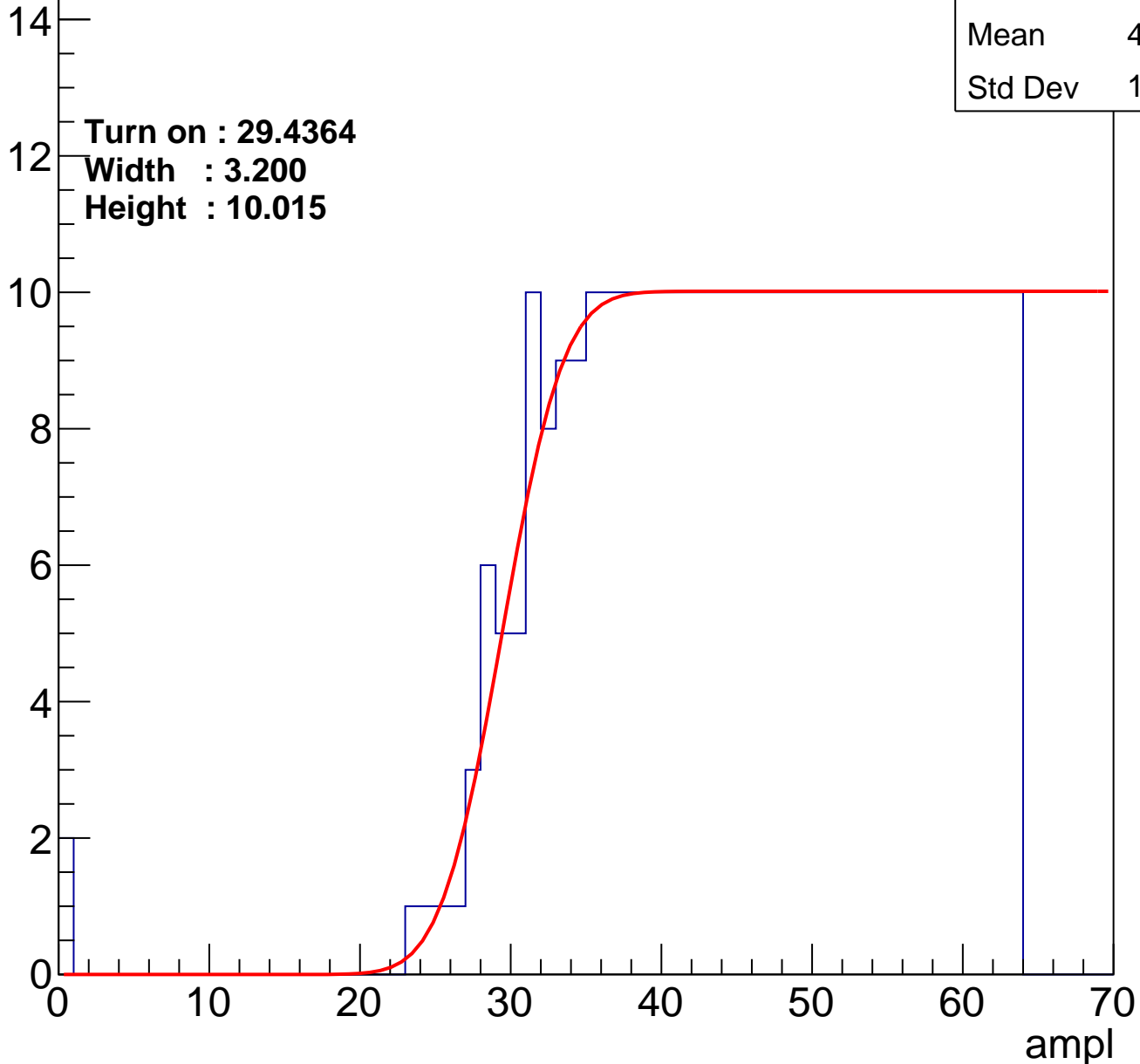
Entries	351
Mean	45.64
Std Dev	10.85

Turn on : 29.4364

Width : 3.200

Height : 10.015

Entry



B0L001S, U17-ch3

calib_packv5_042523_0143.root, FC#9, port A1

Entries	355
Mean	45.39
Std Dev	11.05

Turn on : 29.3811

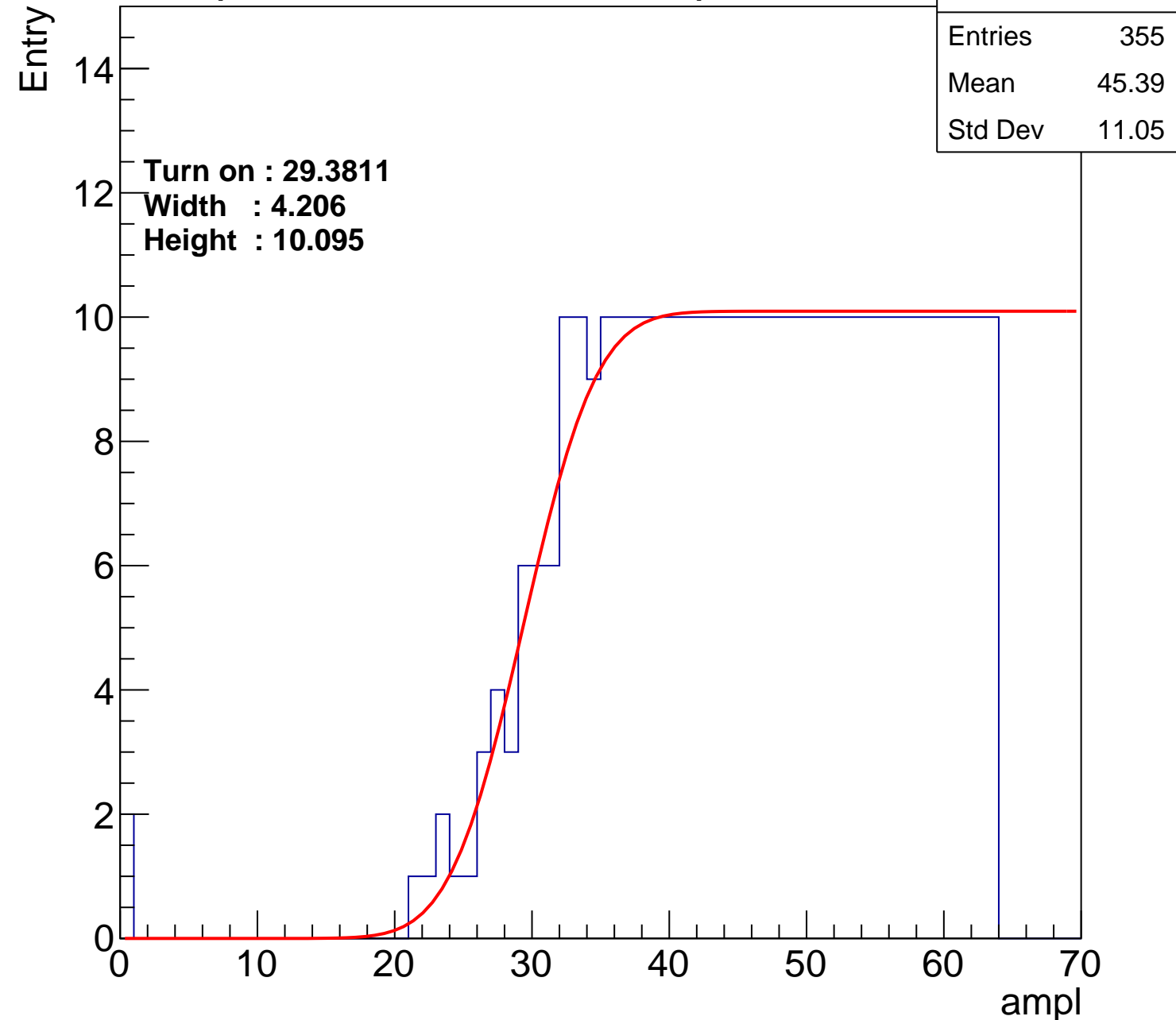
Width : 4.206

Height : 10.095

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch4

calib_packv5_042523_0143.root, FC#9, port A1

Entries	375
Mean	44.54
Std Dev	11.25

Turn on : 26.9249

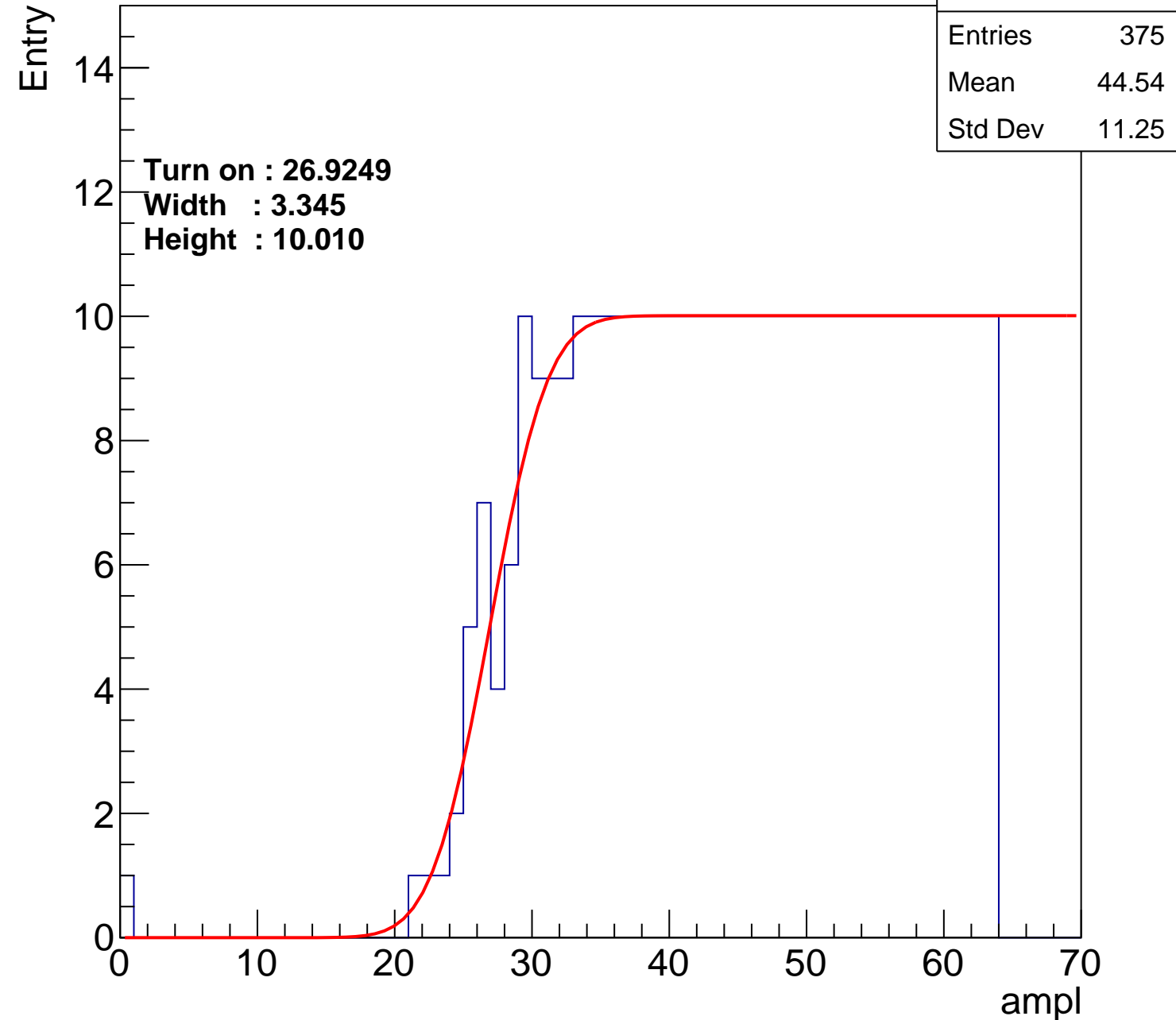
Width : 3.345

Height : 10.010

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch5

calib_packv5_042523_0143.root, FC#9, port A1

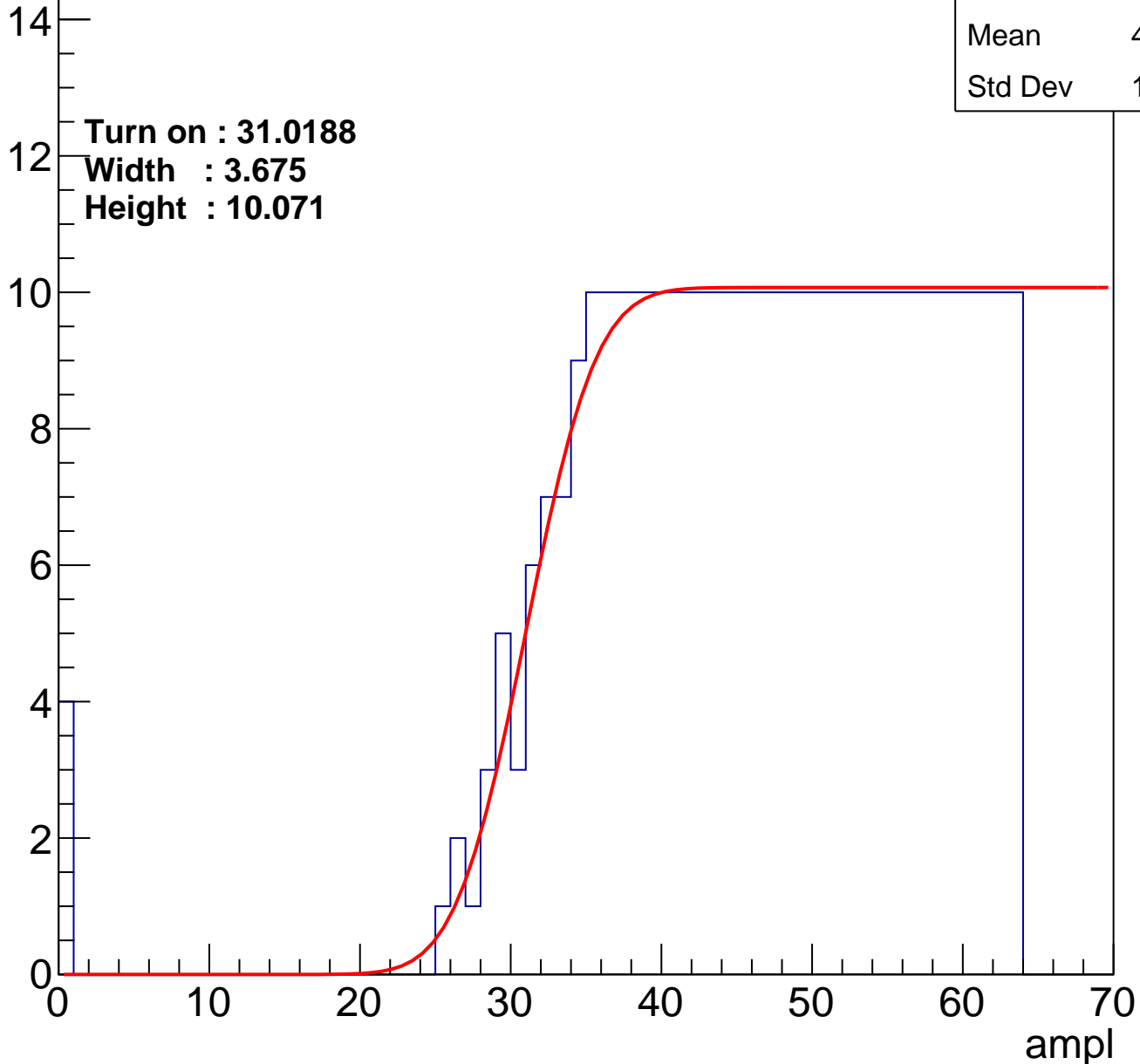
Entries	338
Mean	46.09
Std Dev	11.06

Turn on : 31.0188

Width : 3.675

Height : 10.071

Entry



B0L001S, U17-ch6

calib_packv5_042523_0143.root, FC#9, port A1

Entries	365
Mean	45.06
Std Dev	10.95

Turn on : 27.7310

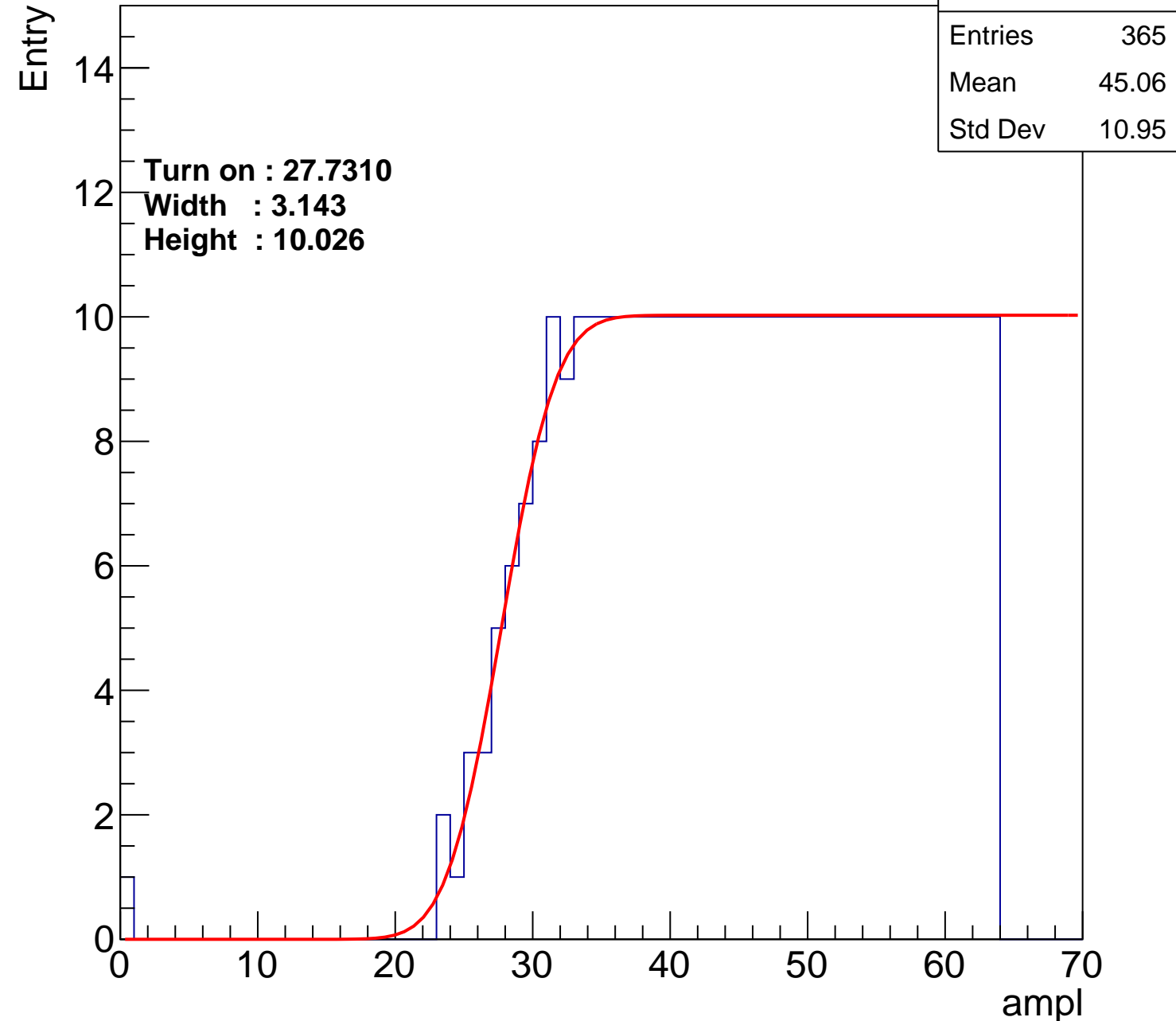
Width : 3.143

Height : 10.026

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch7

calib_packv5_042523_0143.root, FC#9, port A1

Entries	346
Mean	45.91
Std Dev	10.69

Turn on : 29.6981

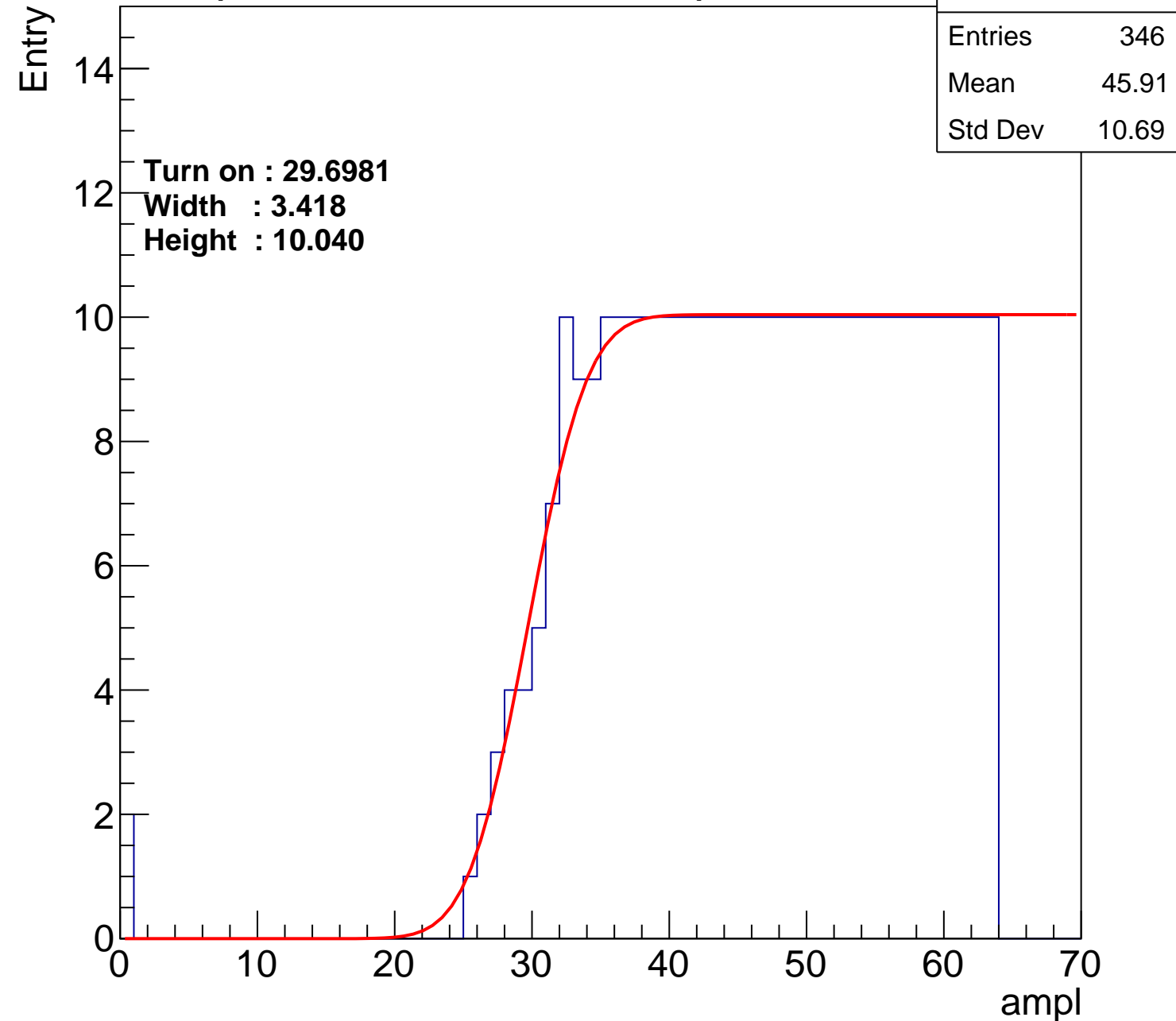
Width : 3.418

Height : 10.040

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch8

calib_packv5_042523_0143.root, FC#9, port A1

Entries	377
Mean	44.41
Std Dev	11.44

Turn on : 26.6938

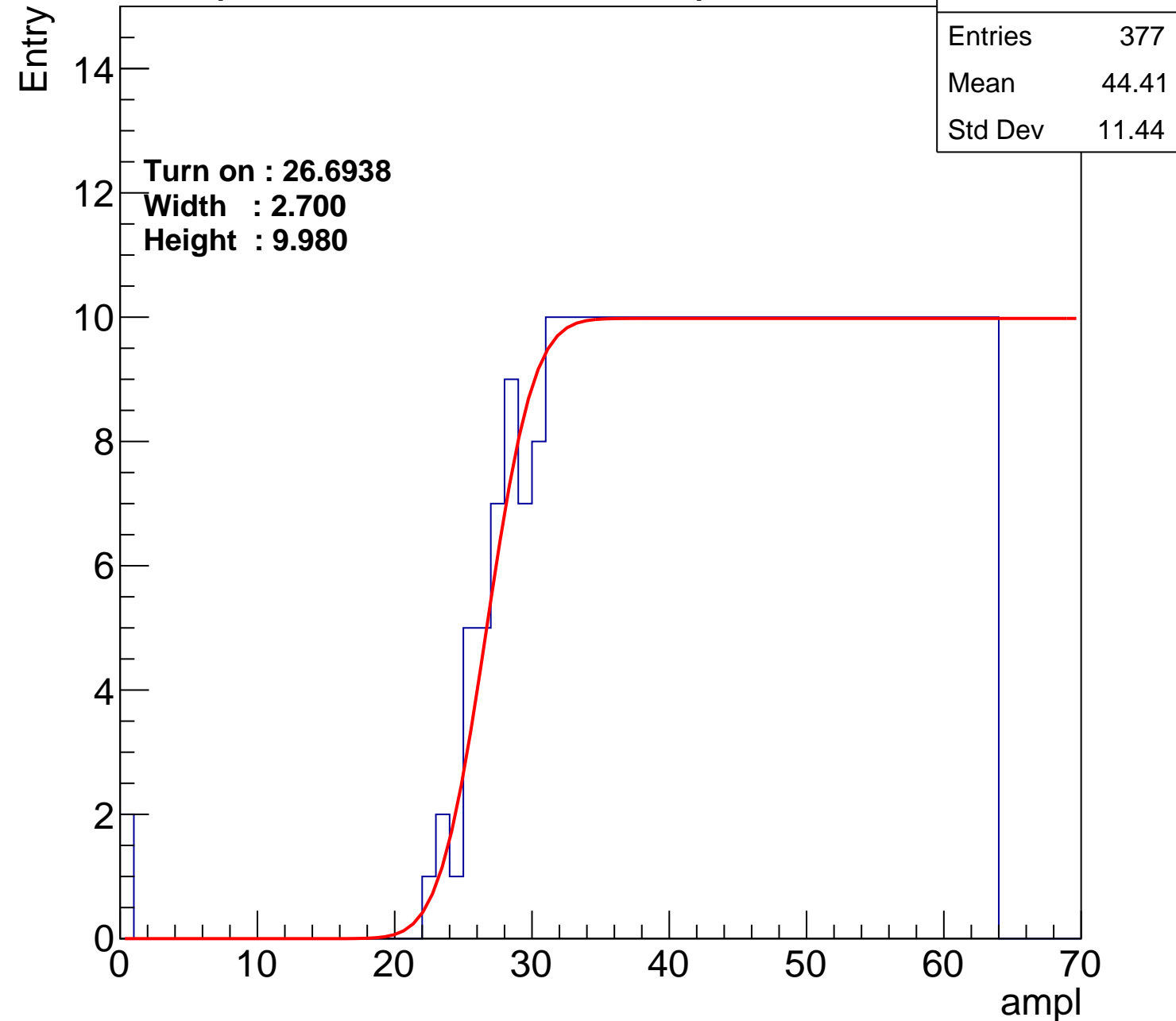
Width : 2.700

Height : 9.980

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch9

calib_packv5_042523_0143.root, FC#9, port A1

Entries	366
Mean	44.94
Std Dev	11.17

Turn on : 28.0940

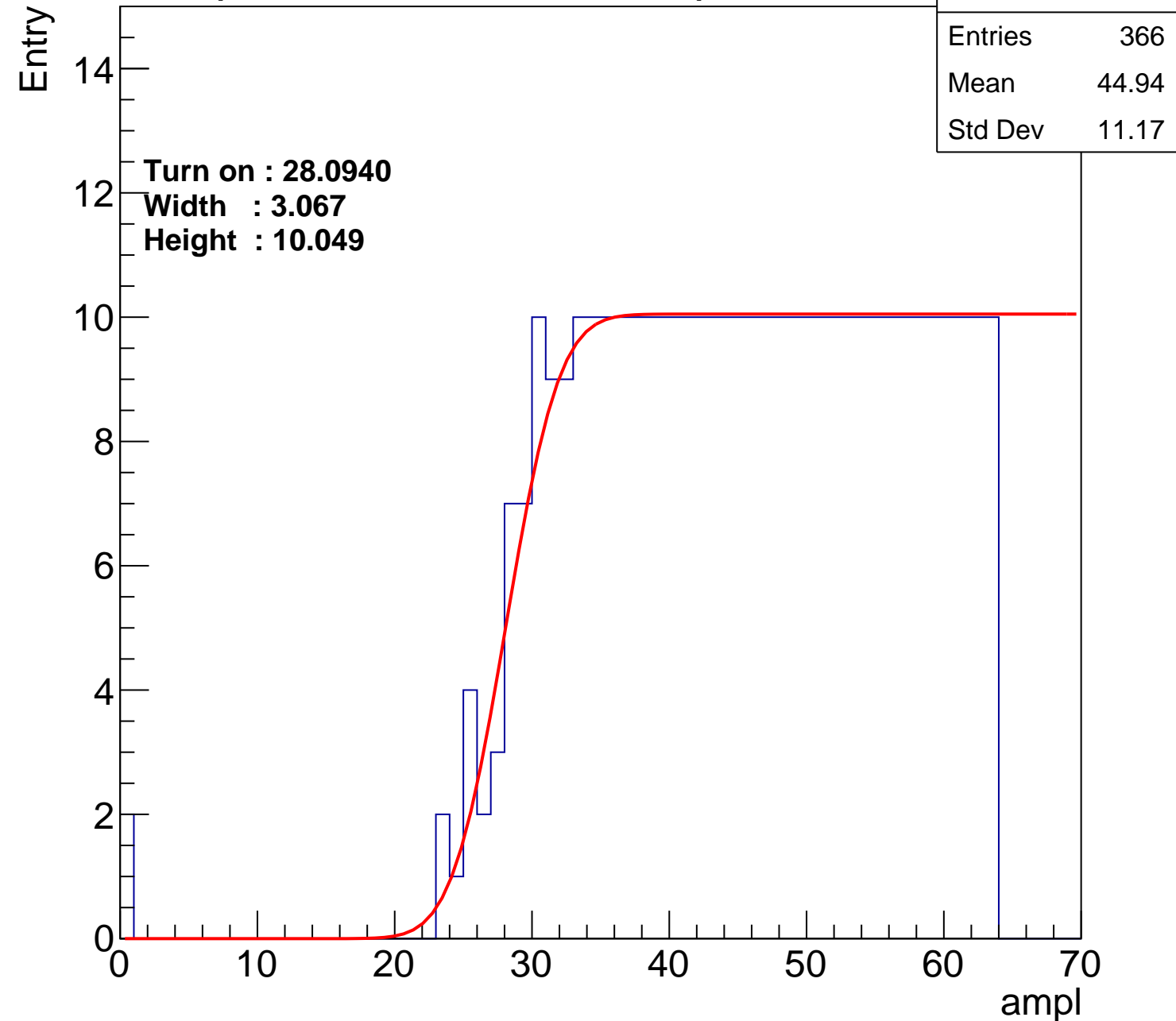
Width : 3.067

Height : 10.049

Entry

14
12
10
8
6
4
2
0

ampl



calib_packv5_042523_0143.root, FC#9, port A1

Entries	348
Mean	45.83
Std Dev	10.71

Mean	45.83
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Std Dev	10.71
---------	-------

Width : 2.121

Height : 9.929



B0L001S, U17-ch11

calib_packv5_042523_0143.root, FC#9, port A1

Entries	371
Mean	44.64
Std Dev	11.38

Turn on : 27.1599

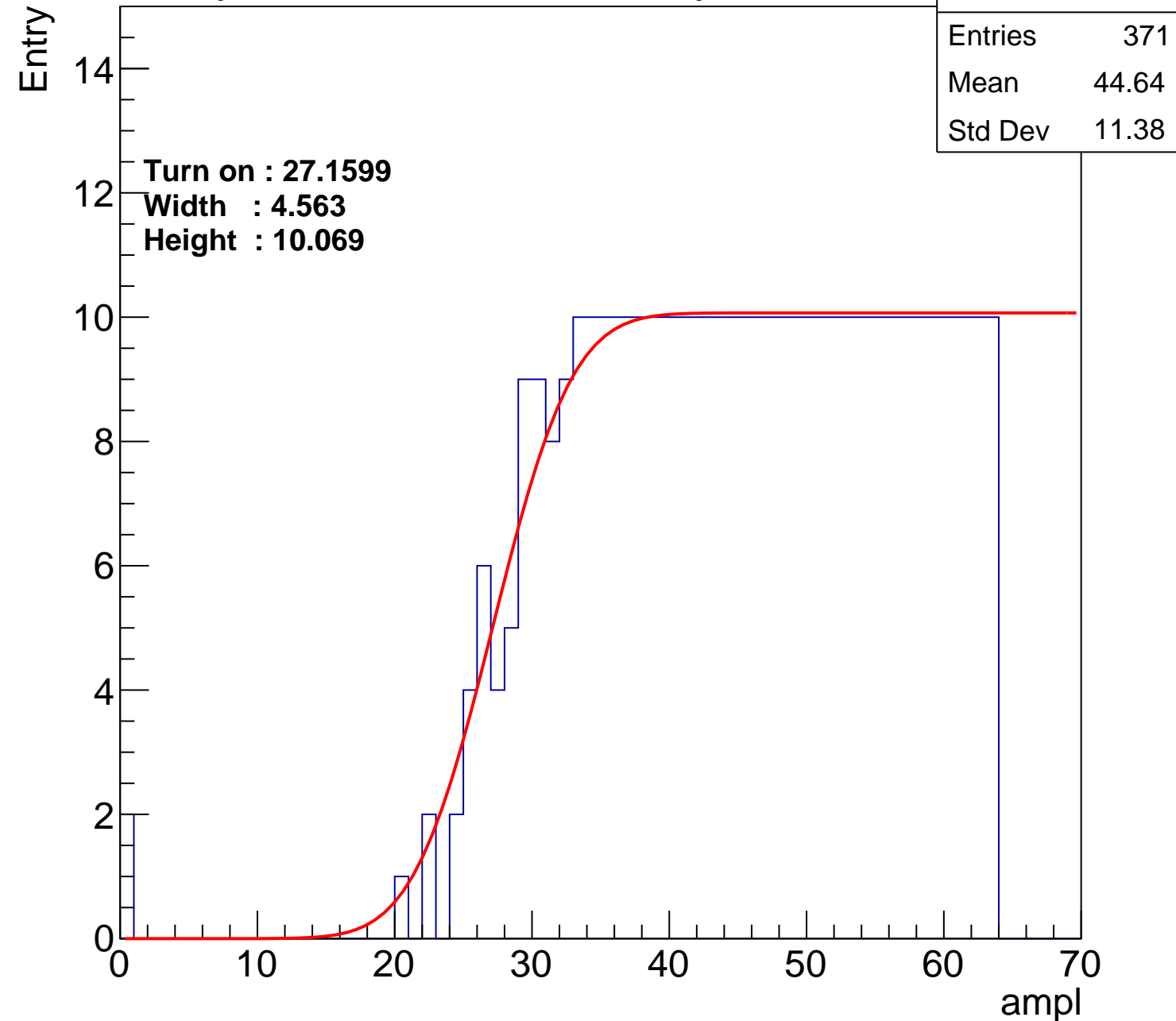
Width : 4.563

Height : 10.069

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch12

calib_packv5_042523_0143.root, FC#9, port A1

Entries	367
Mean	44.96
Std Dev	11.01

Turn on : 27.2273

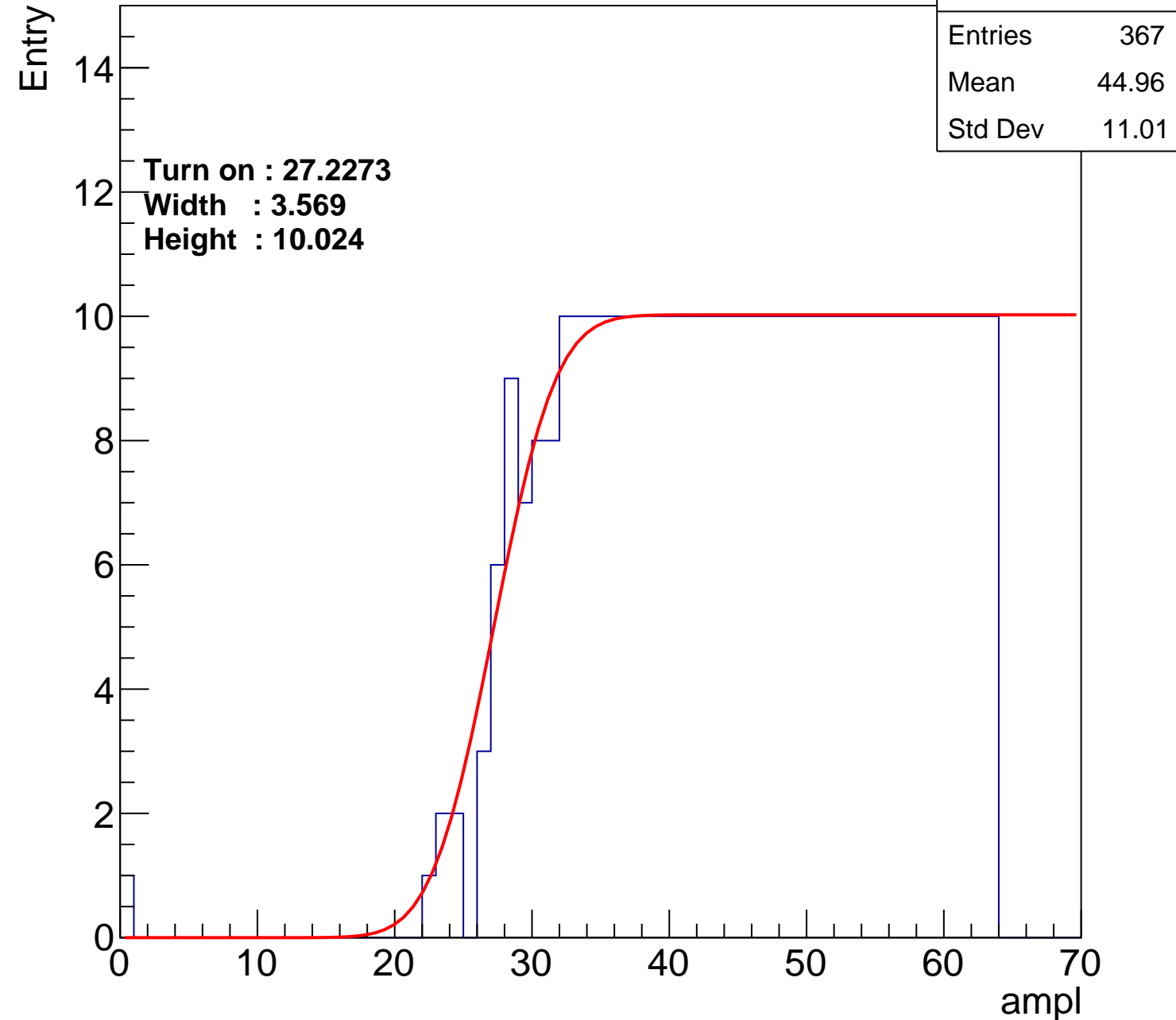
Width : 3.569

Height : 10.024

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch13

calib_packv5_042523_0143.root, FC#9, port A1

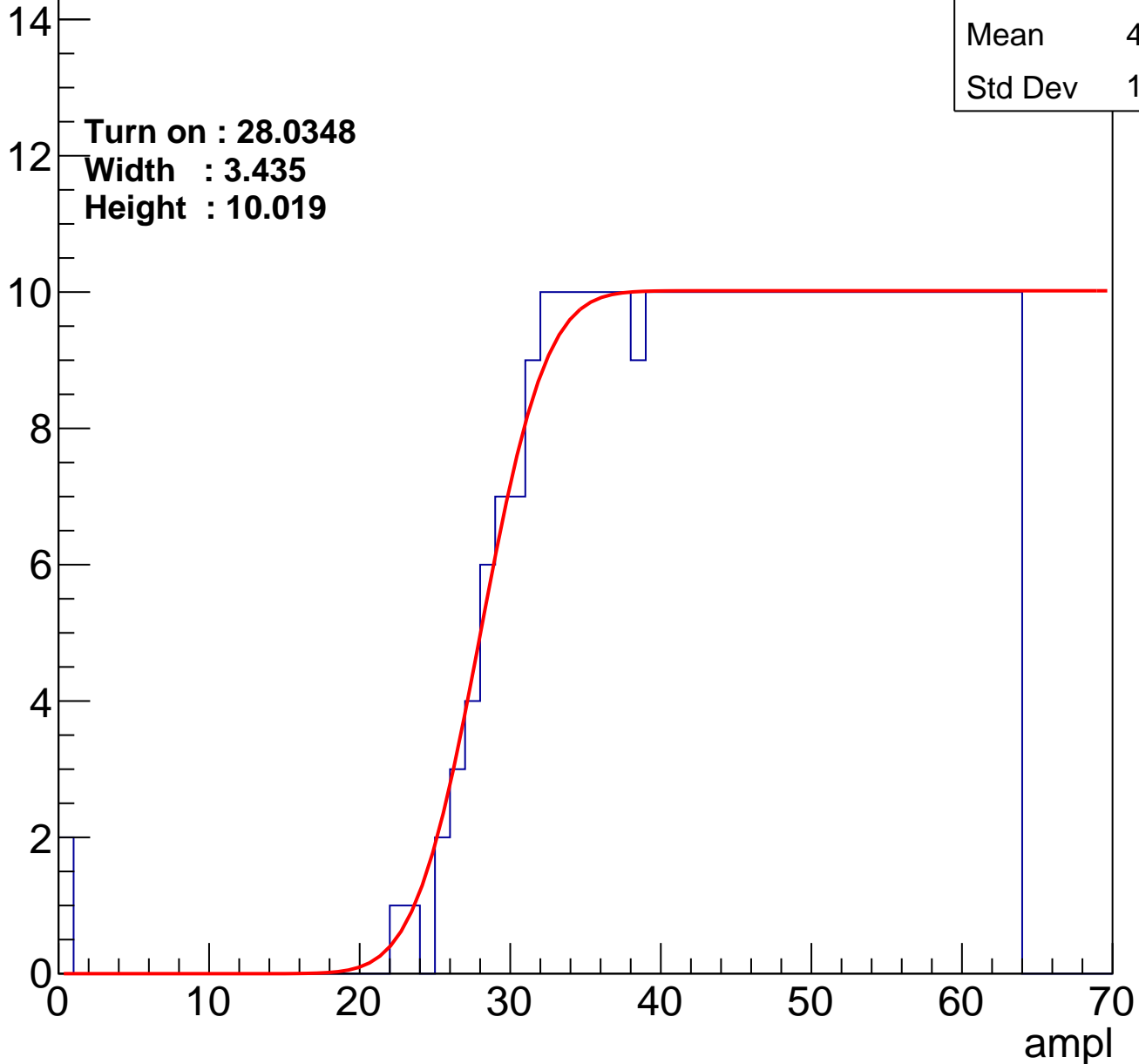
Entries	361
Mean	45.16
Std Dev	11.08

Turn on : 28.0348

Width : 3.435

Height : 10.019

Entry



B0L001S, U17-ch14

calib_packv5_042523_0143.root, FC#9, port A1

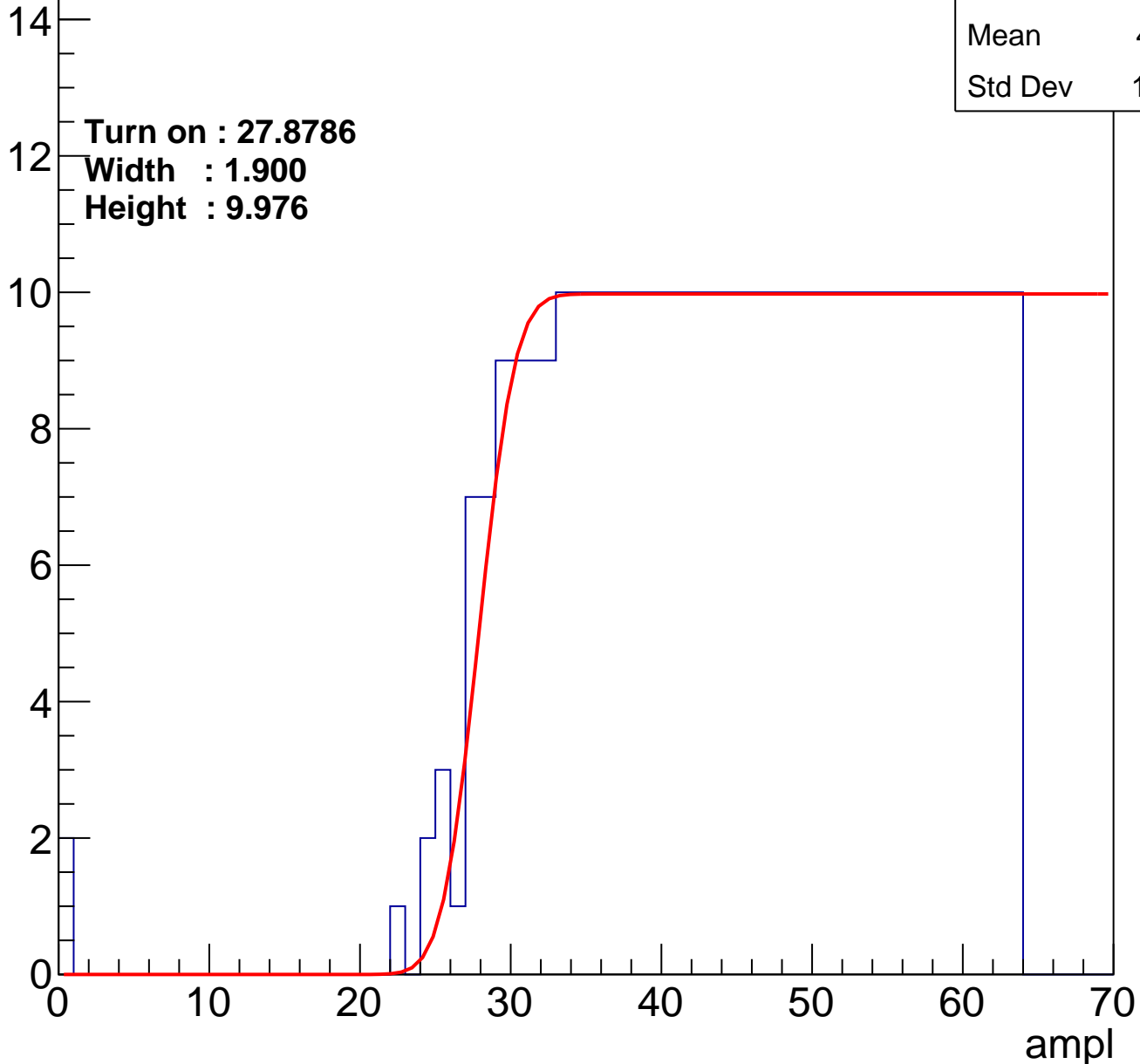
Entries	369
Mean	44.81
Std Dev	11.23

Turn on : 27.8786

Width : 1.900

Height : 9.976

Entry



B0L001S, U17-ch15

calib_packv5_042523_0143.root, FC#9, port A1

Entries	375
Mean	44.4
Std Dev	11.72

Turn on : 26.7506

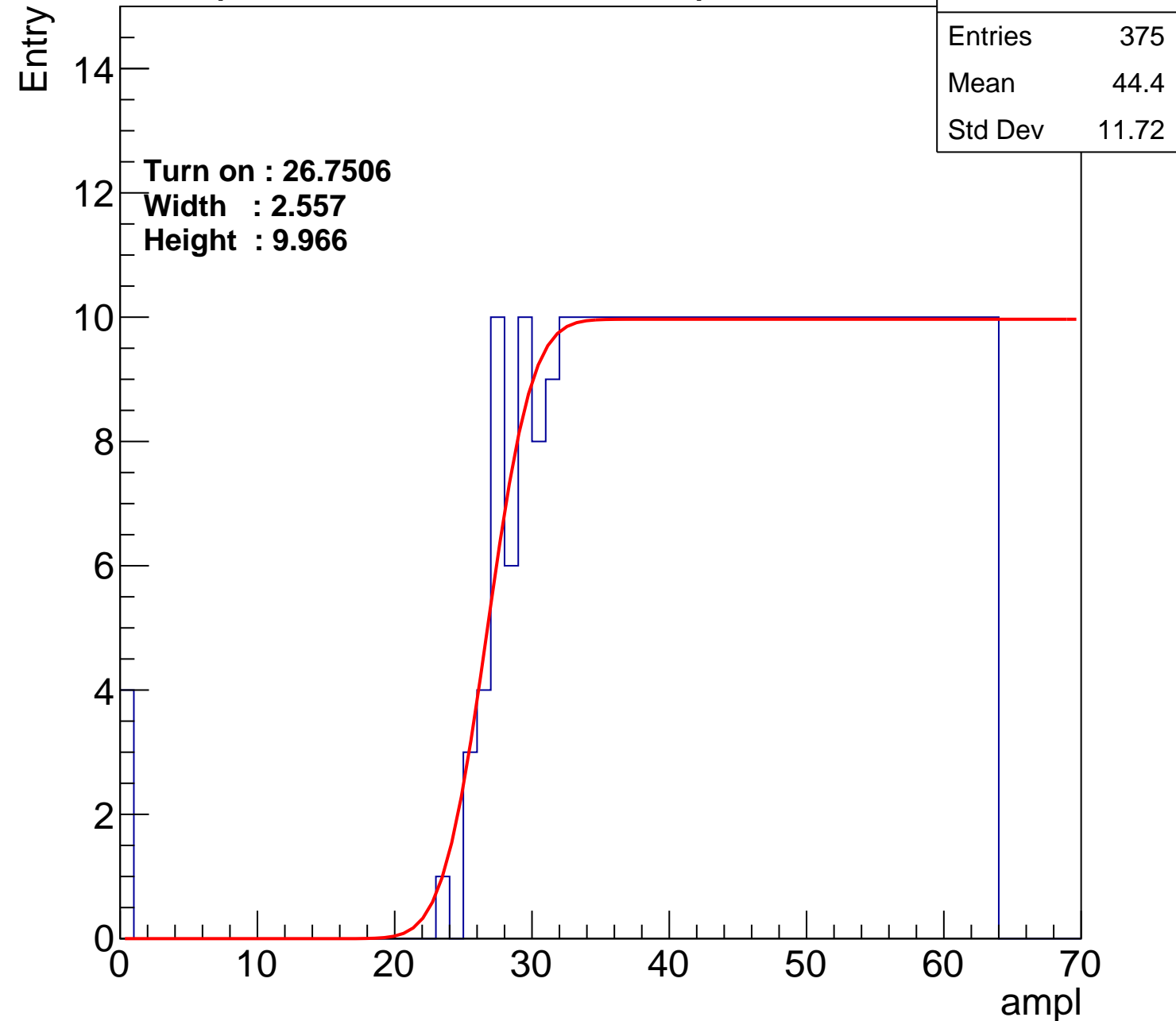
Width : 2.557

Height : 9.966

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch16

calib_packv5_042523_0143.root, FC#9, port A1

Entries	389
Mean	43.65
Std Dev	12.21

Turn on : 25.4489

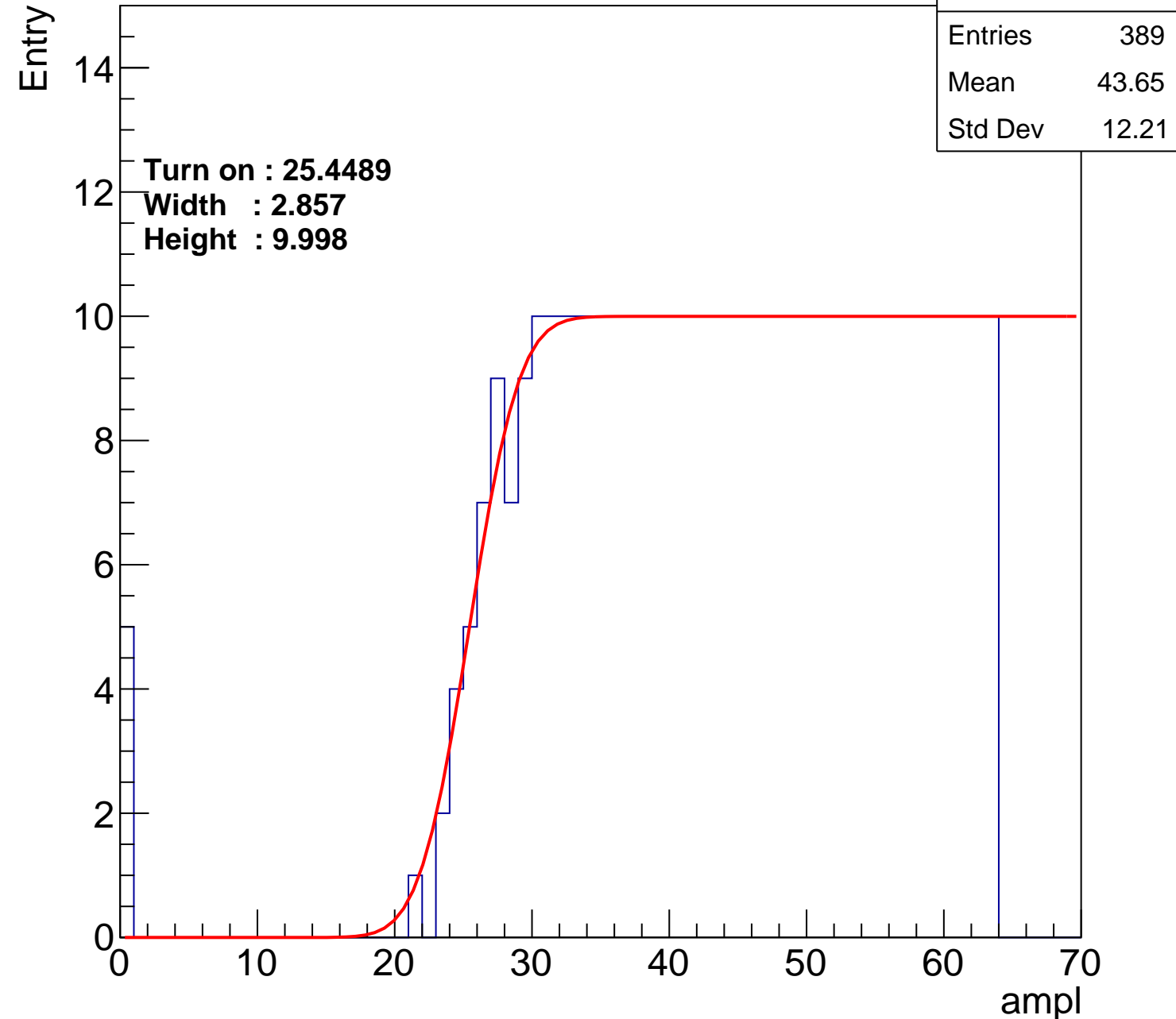
Width : 2.857

Height : 9.998

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch17

calib_packv5_042523_0143.root, FC#9, port A1

Entries	370
Mean	44.7
Std Dev	11.42

Turn on : 27.0810

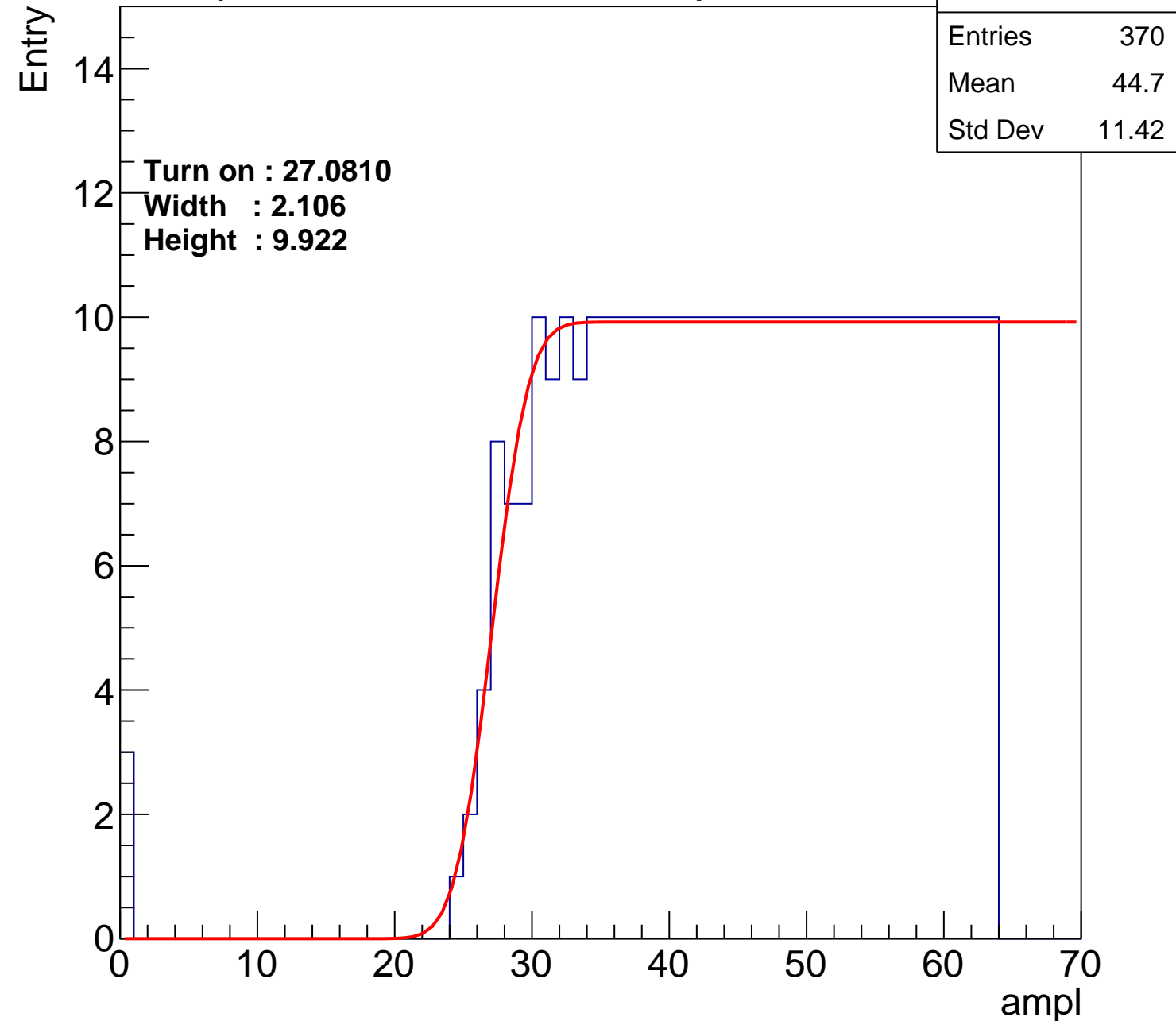
Width : 2.106

Height : 9.922

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch18

calib_packv5_042523_0143.root, FC#9, port A1

Entries	372
Mean	44.56
Std Dev	11.55

Turn on : 28.2204

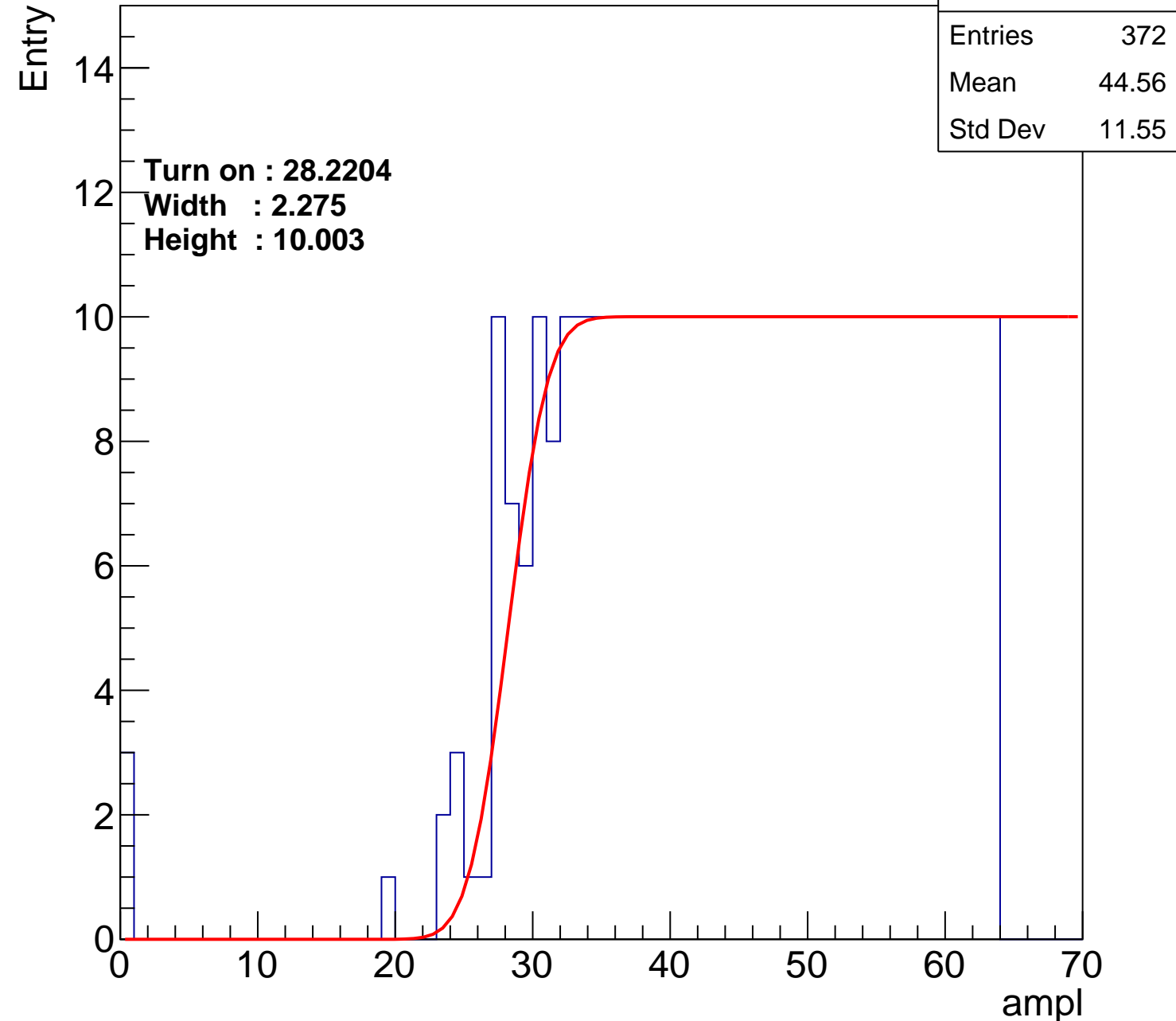
Width : 2.275

Height : 10.003

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch19

calib_packv5_042523_0143.root, FC#9, port A1

Entries	370
Mean	44.46
Std Dev	12.04

Turn on : 27.9547

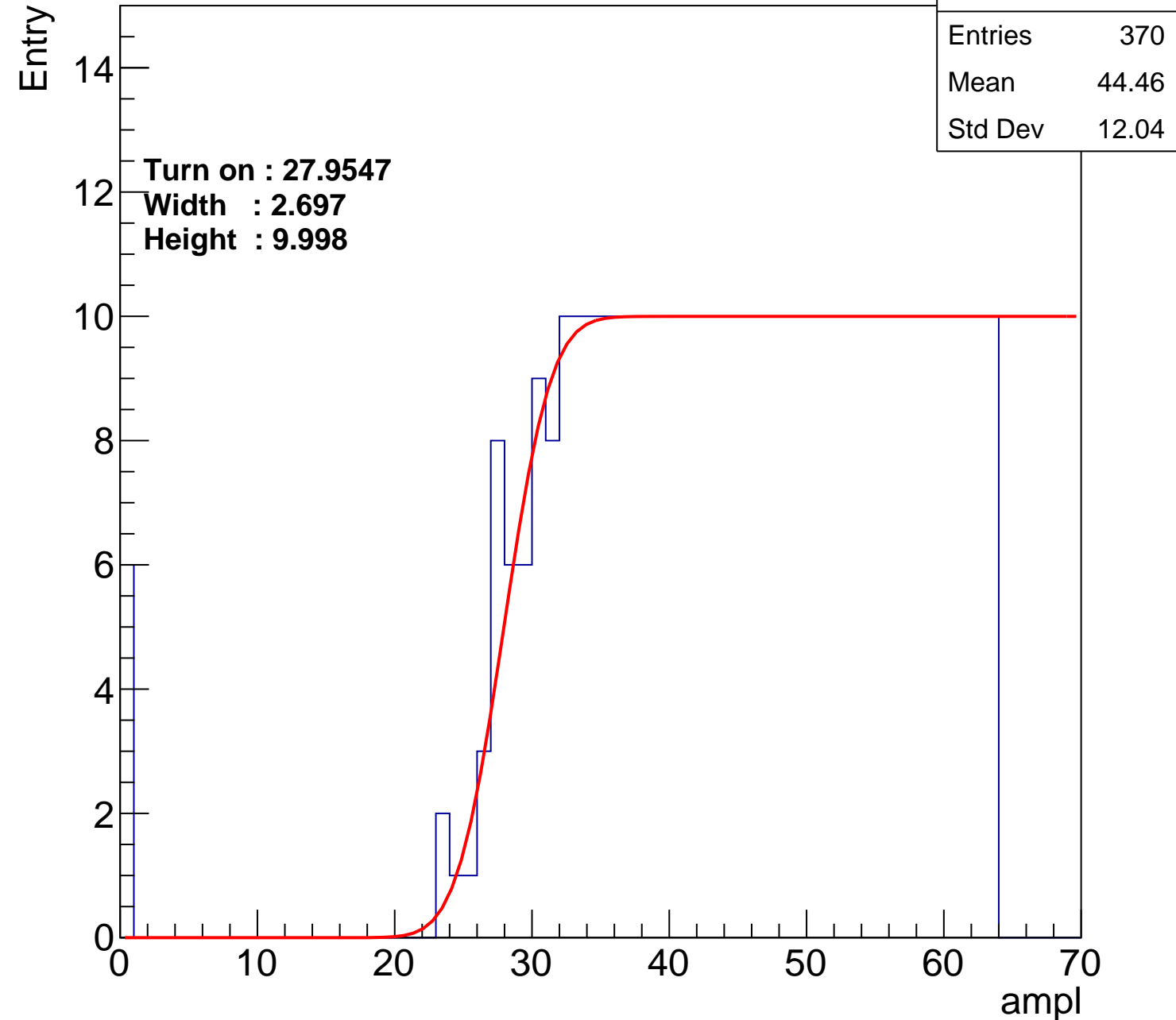
Width : 2.697

Height : 9.998

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch20

calib_packv5_042523_0143.root, FC#9, port A1

Entries	354
Mean	45.42
Std Dev	11.15

Turn on : 29.4467

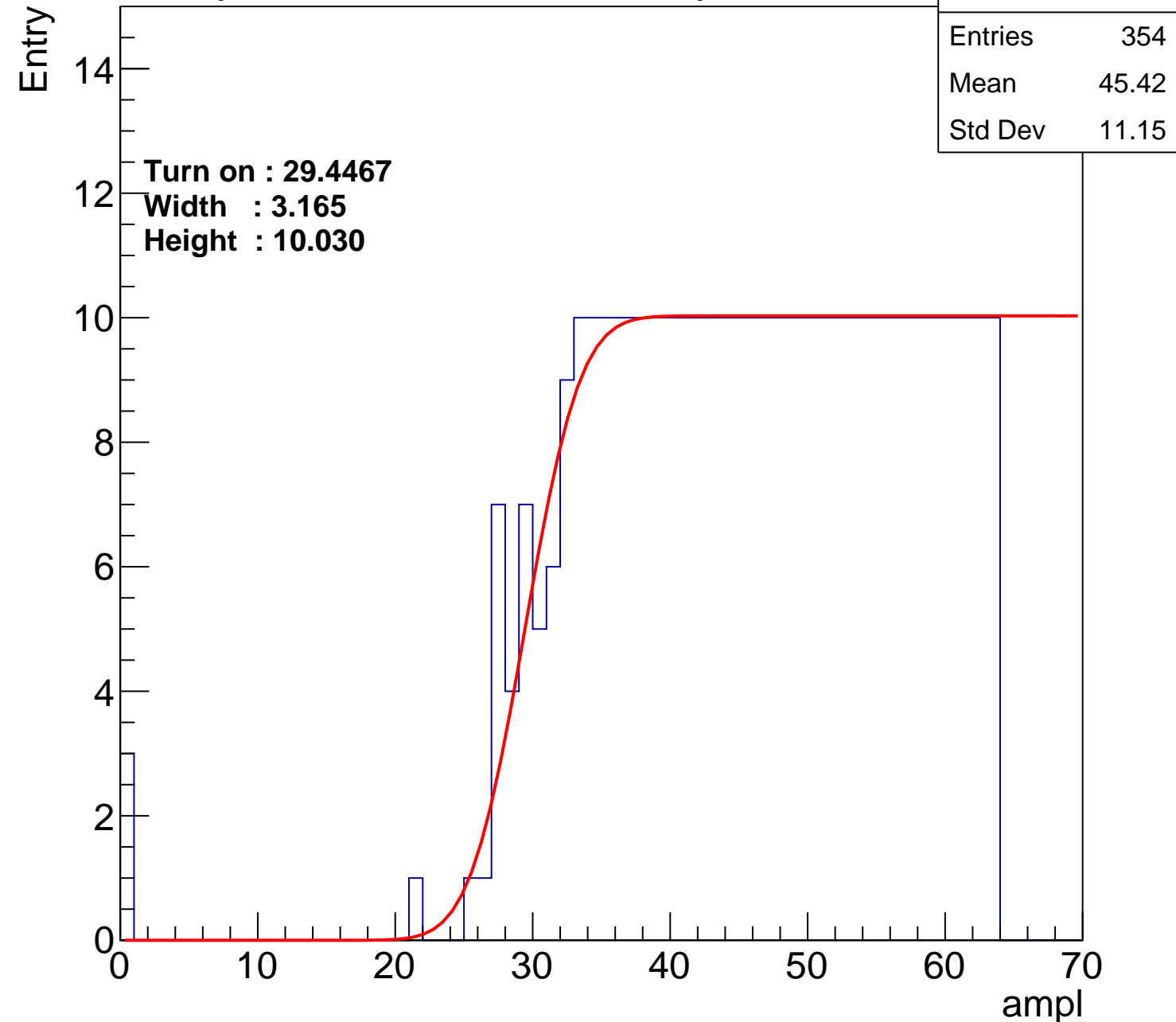
Width : 3.165

Height : 10.030

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch21

calib_packv5_042523_0143.root, FC#9, port A1

Entries	360
Mean	45.25
Std Dev	11

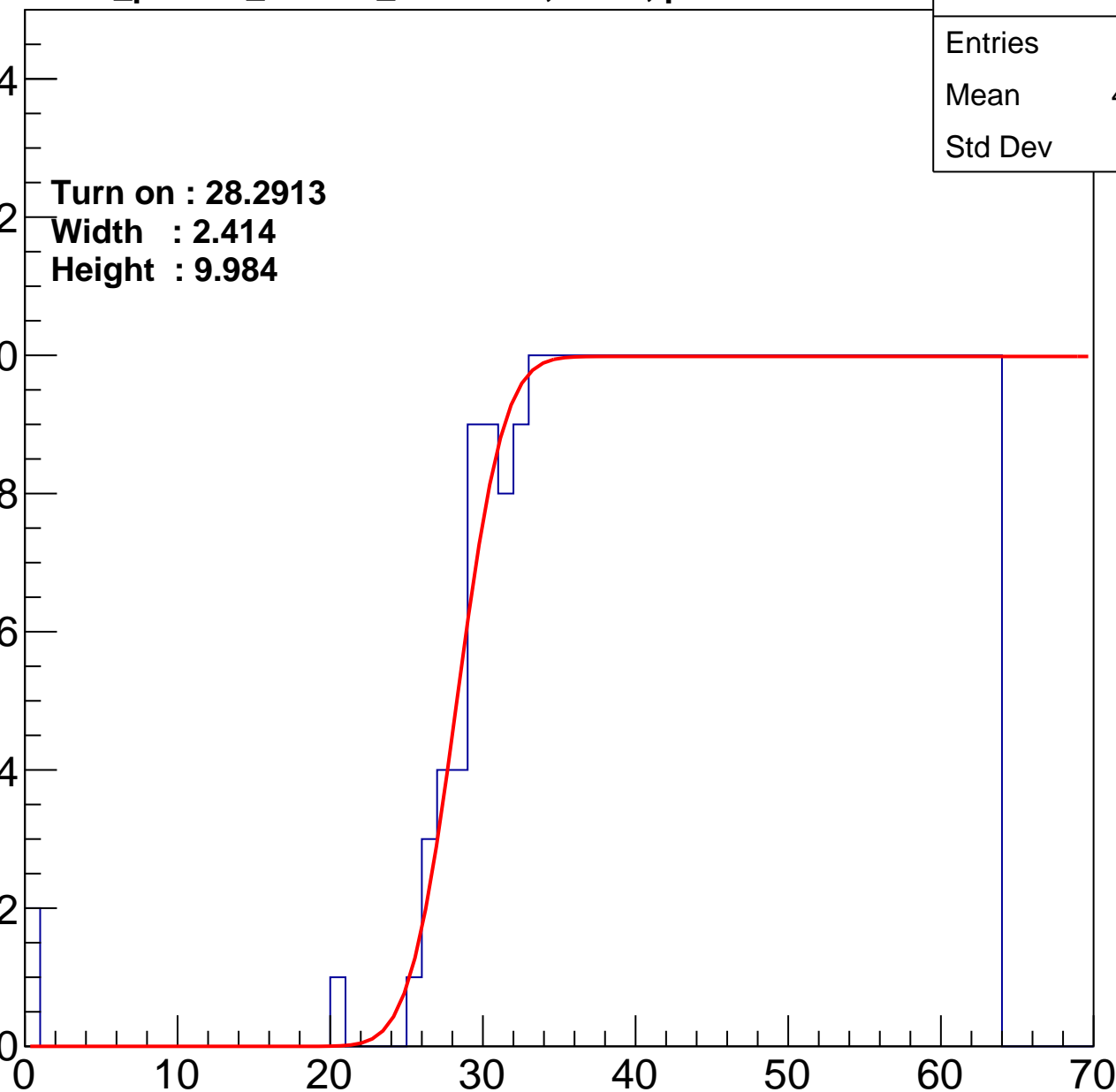
Turn on : 28.2913

Width : 2.414

Height : 9.984

Entry

14
12
10
8
6
4
2
0



ampl

B0L001S, U17-ch22

calib_packv5_042523_0143.root, FC#9, port A1

Entries	383
Mean	44.13
Std Dev	11.58

Turn on : 25.8143

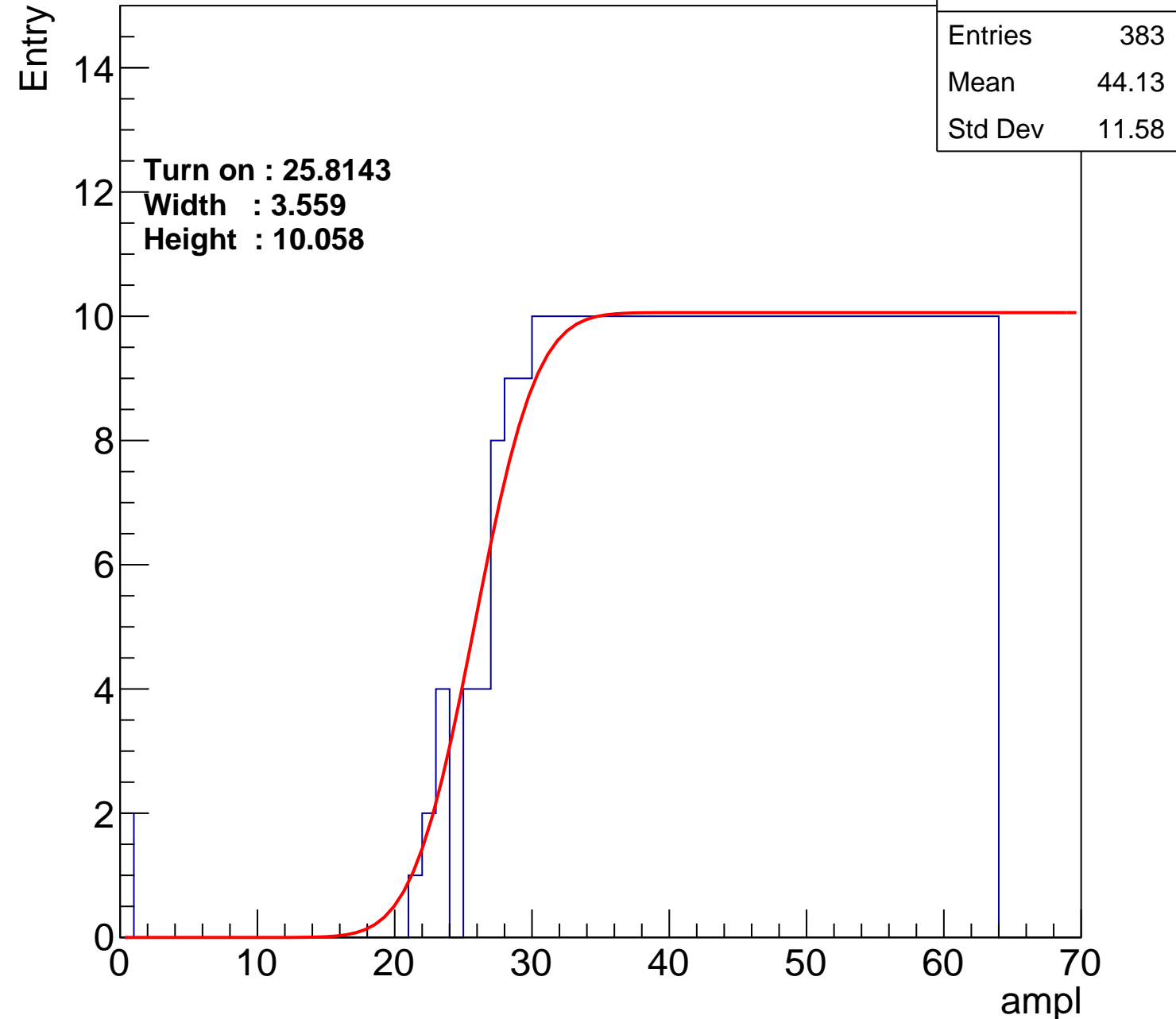
Width : 3.559

Height : 10.058

Entry

14
12
10
8
6
4
2
0

ampl

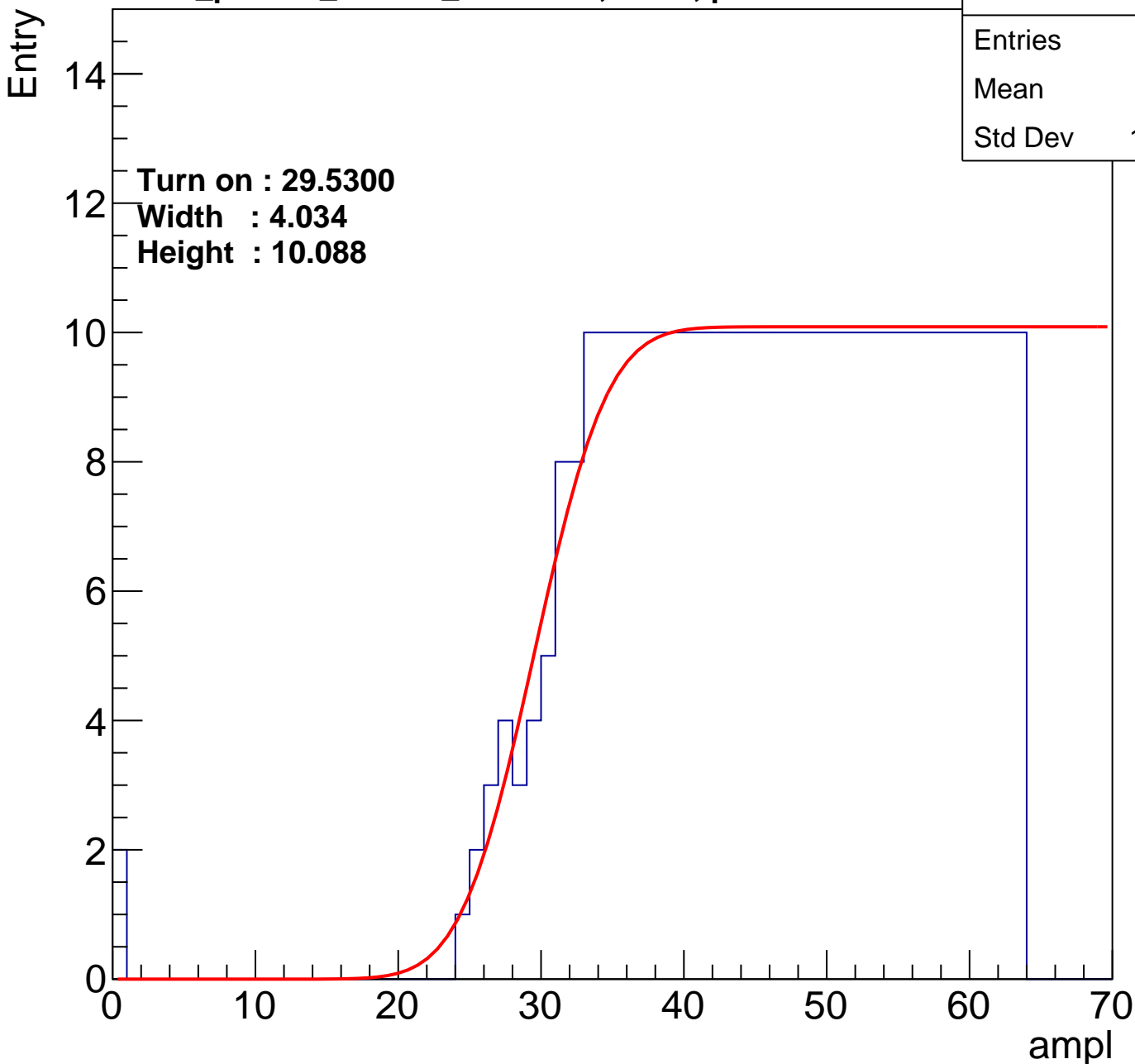


calib_packv5_042523_0143.root, FC#9, port A1

calib_packv5_042523_0143.root, FC#9, port A1

Entries	350
Mean	45.7
Std Dev	10.83

Height : 10.088



B0L001S, U17-ch24

calib_packv5_042523_0143.root, FC#9, port A1

Entries	364
Mean	45.12
Std Dev	10.9

Turn on : 27.8534

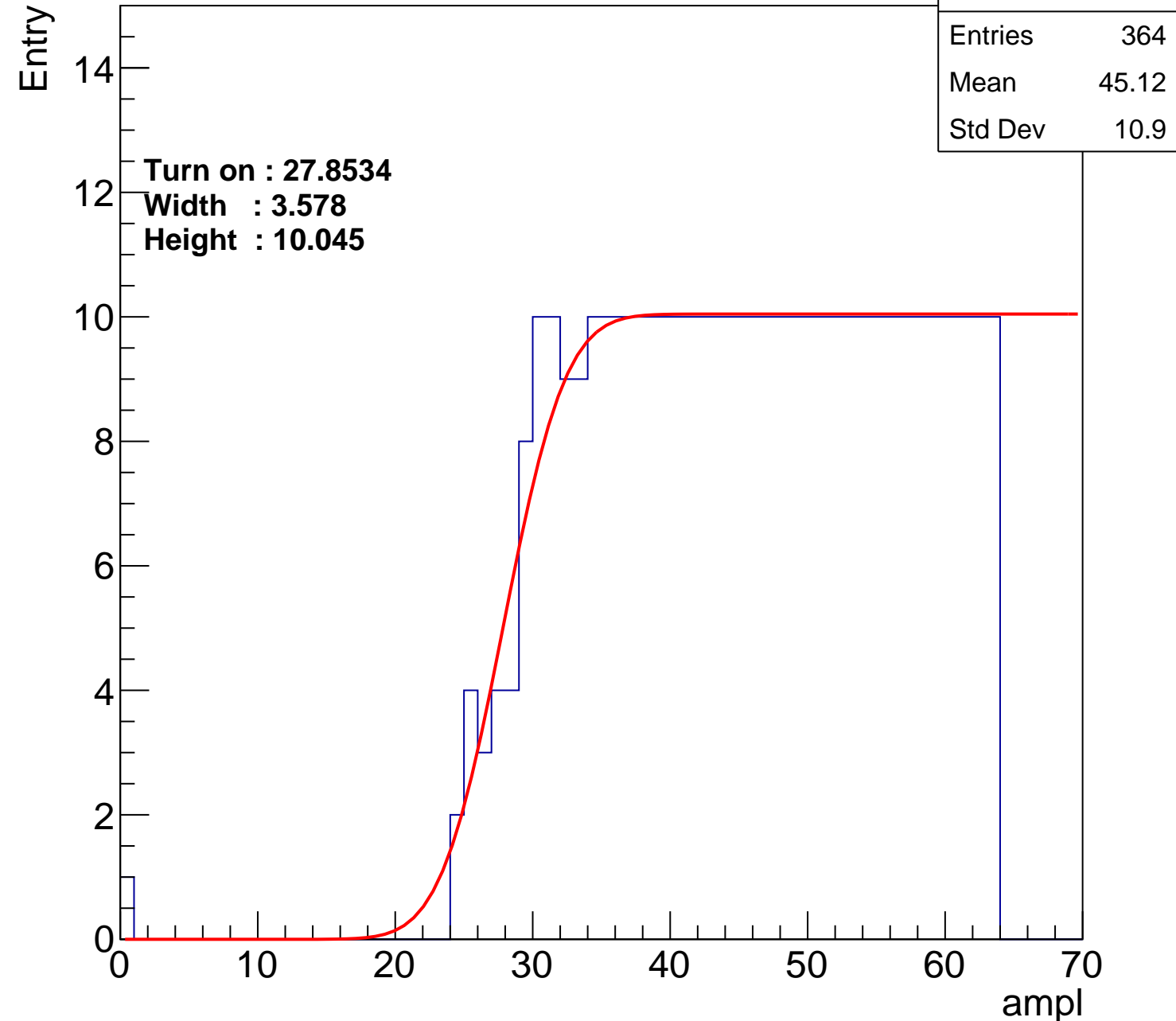
Width : 3.578

Height : 10.045

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch25

calib_packv5_042523_0143.root, FC#9, port A1

Entries	363
Mean	44.87
Std Dev	11.71

Turn on : 28.4246

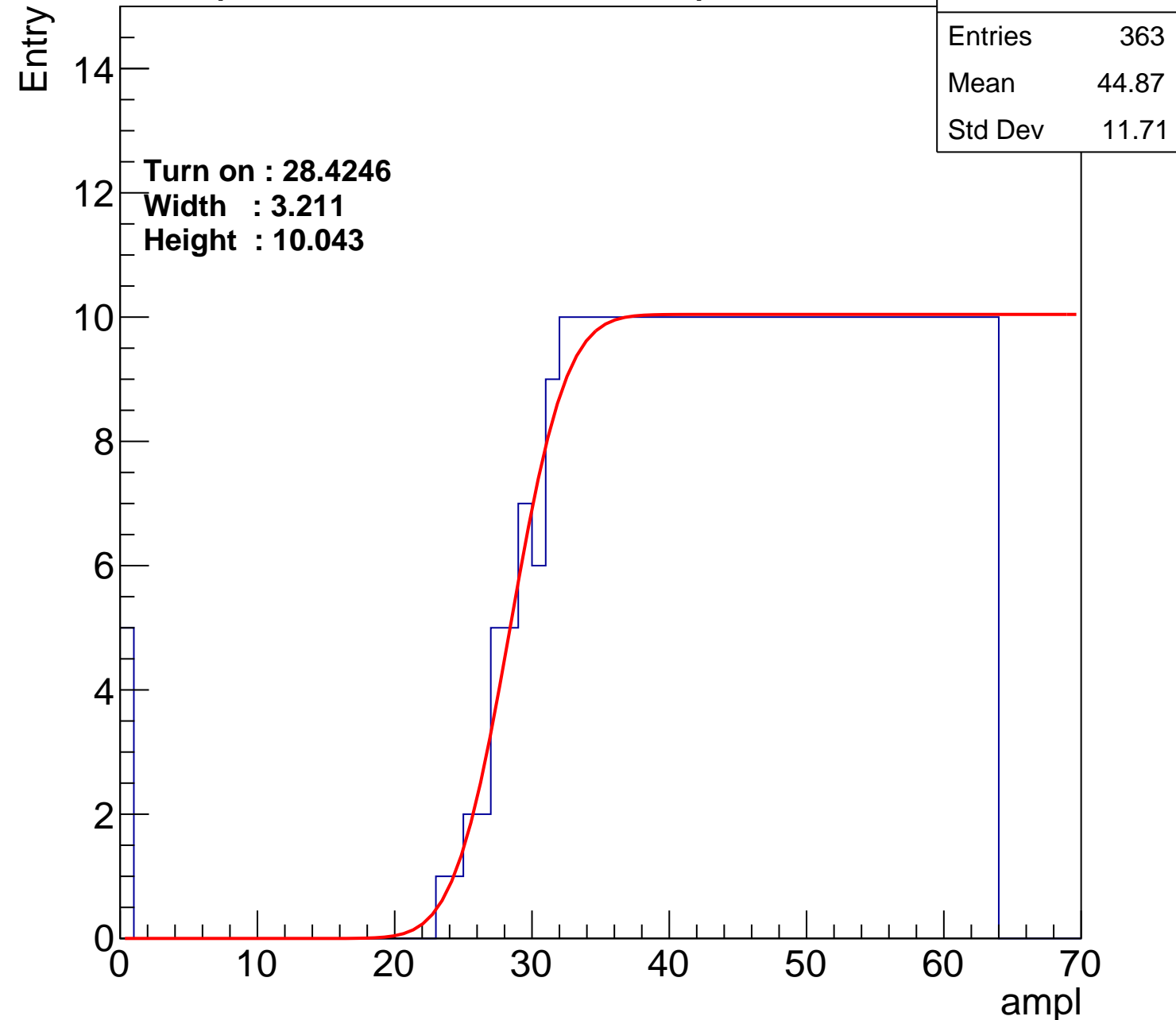
Width : 3.211

Height : 10.043

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch26

calib_packv5_042523_0143.root, FC#9, port A1

Entries	377
Mean	44.27
Std Dev	11.81

Turn on : 26.6779

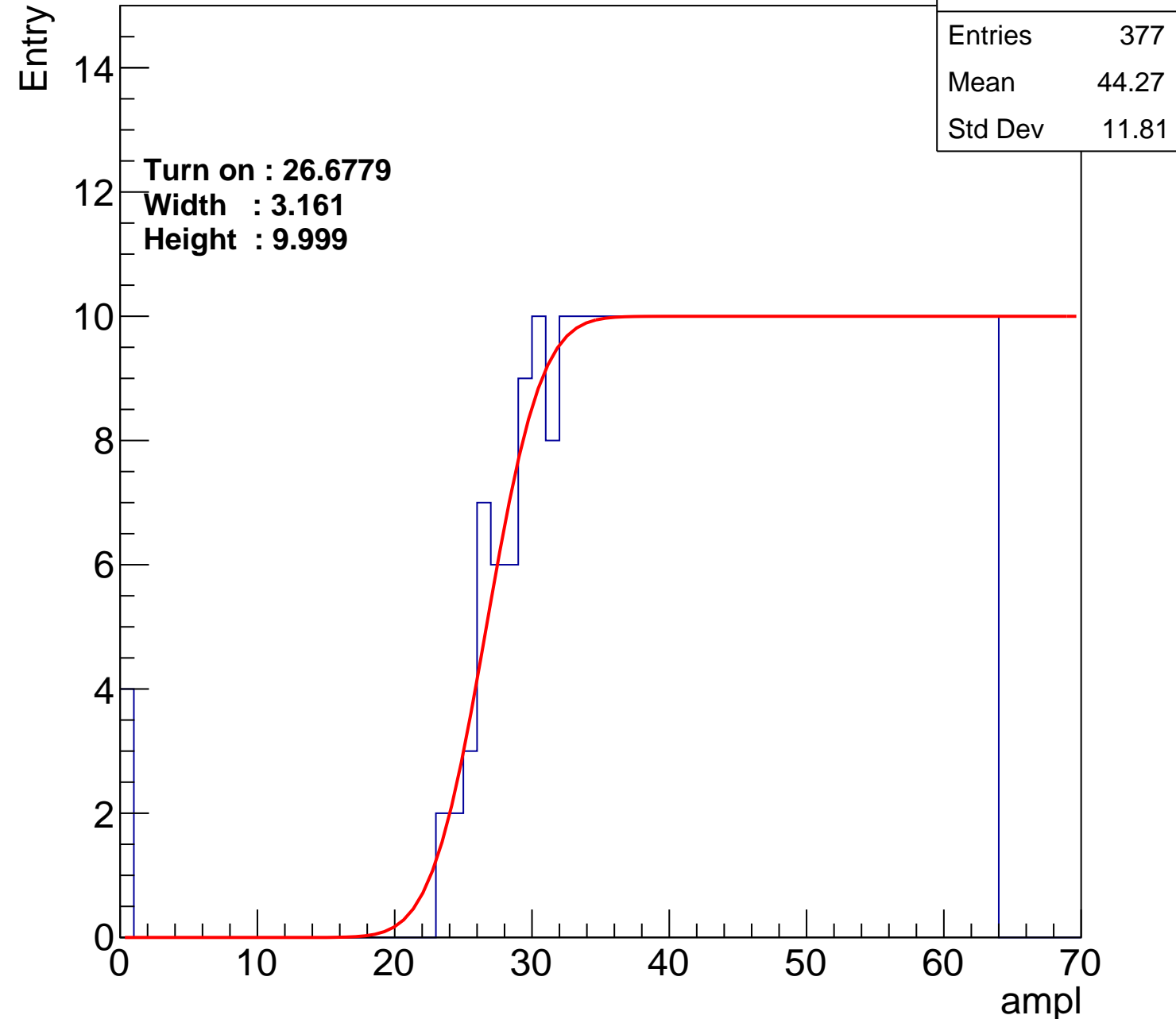
Width : 3.161

Height : 9.999

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch27

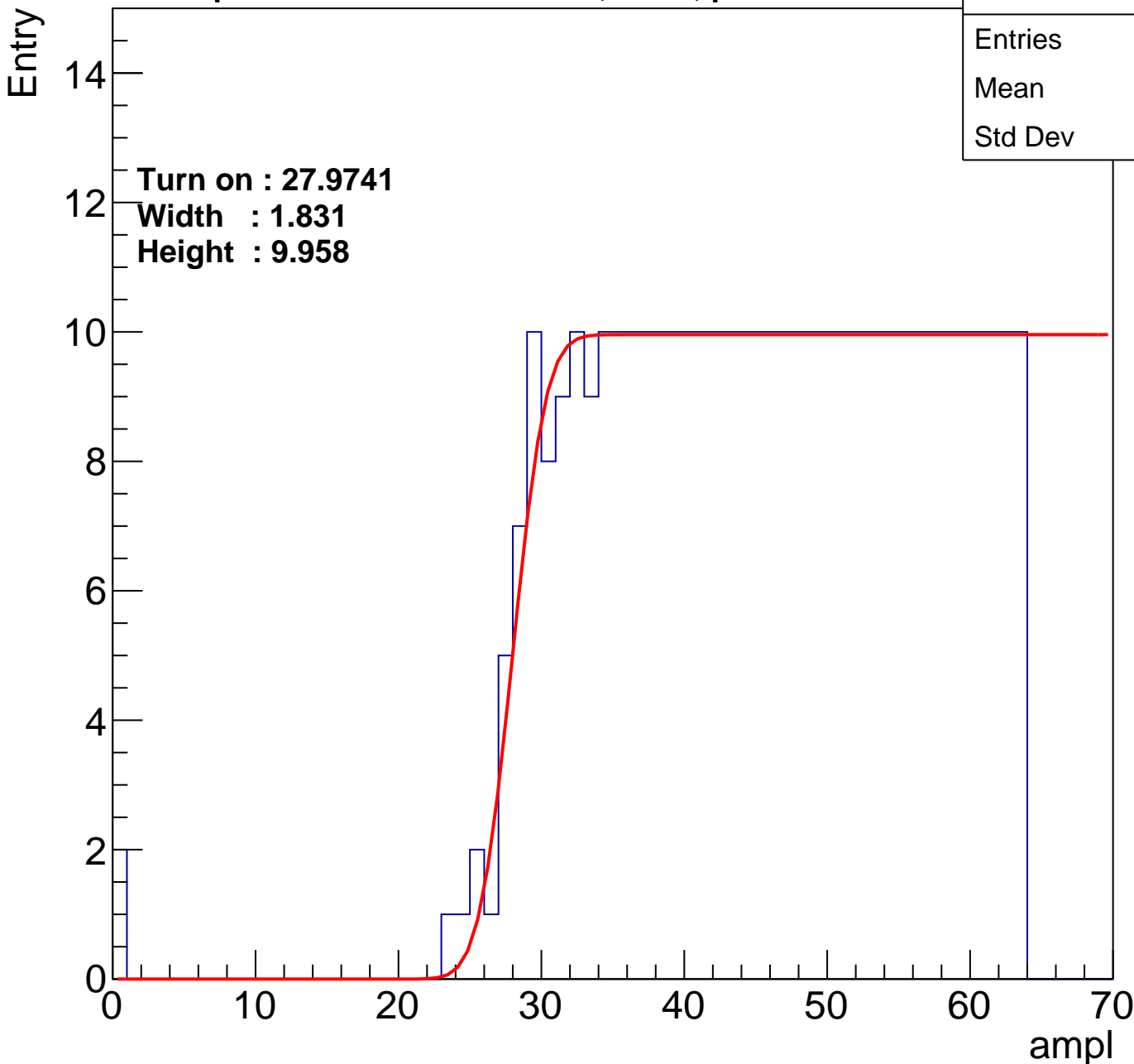
calib_packv5_042523_0143.root, FC#9, port A1

Entries	365
Mean	45.01
Std Dev	11.11

Turn on : 27.9741

Width : 1.831

Height : 9.958



B0L001S, U17-ch28

calib_packv5_042523_0143.root, FC#9, port A1

Entries	375
Mean	44.44
Std Dev	11.58

Turn on : 26.5594

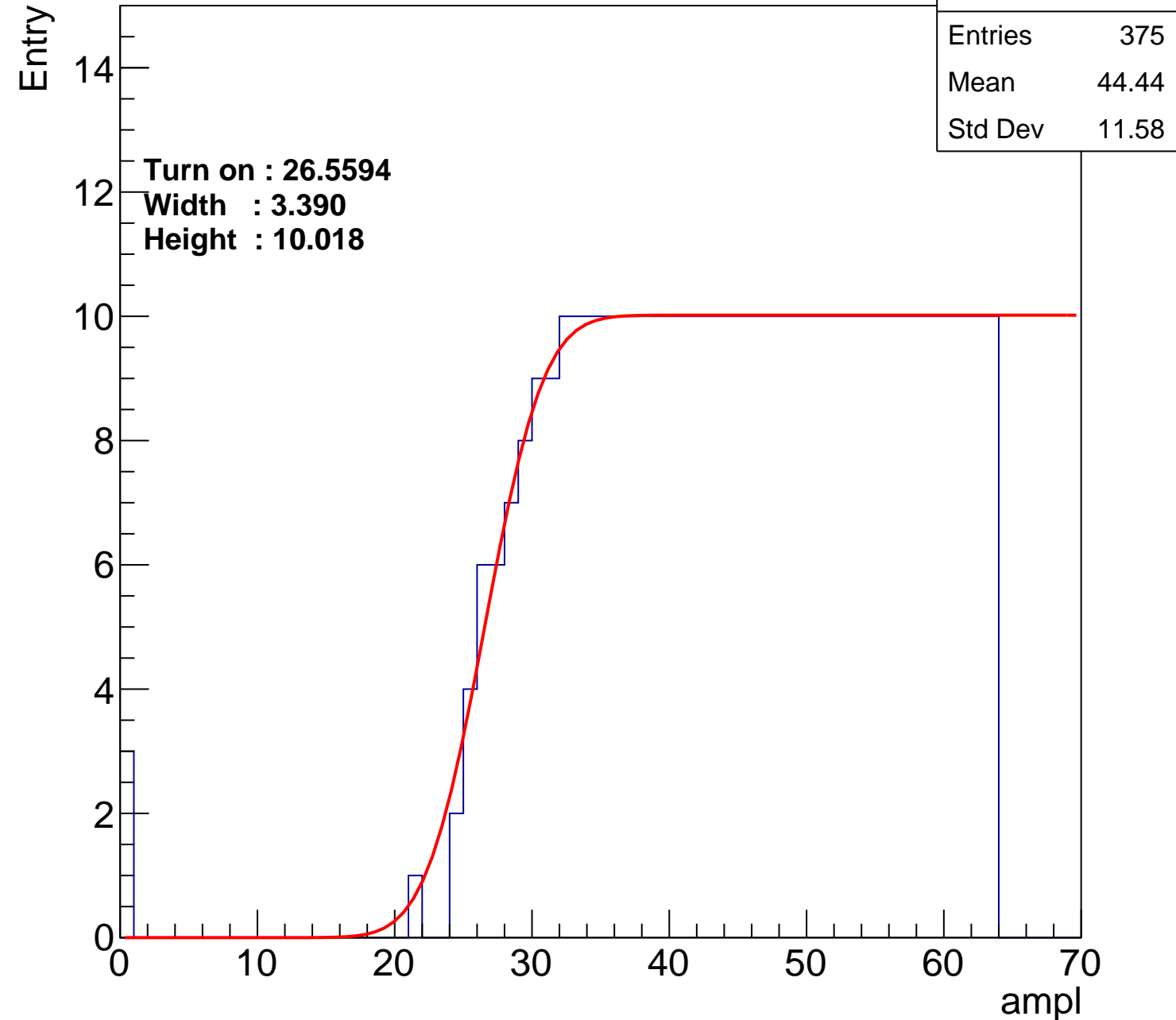
Width : 3.390

Height : 10.018

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch29

calib_packv5_042523_0143.root, FC#9, port A1

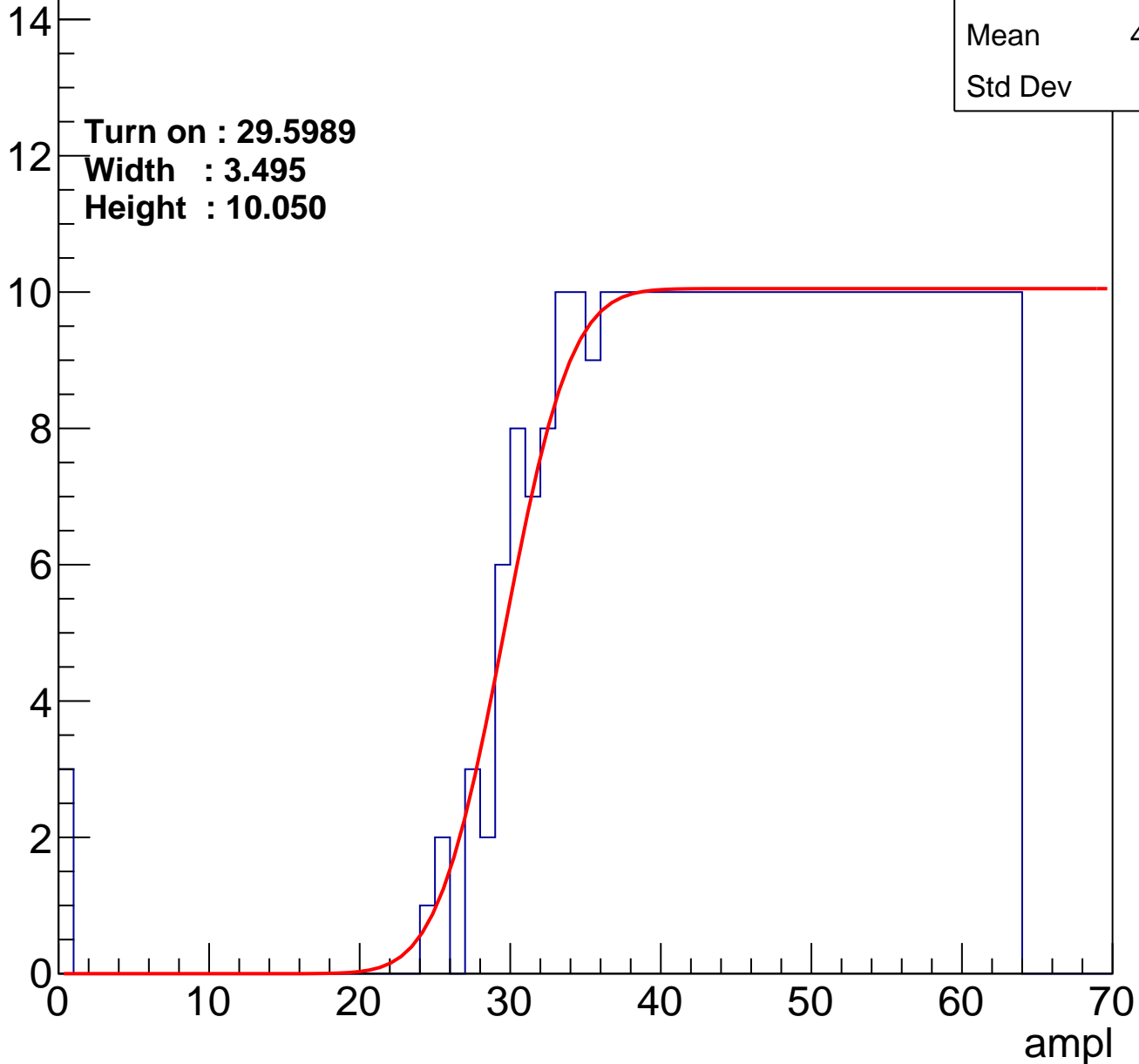
Entries	349
Mean	45.68
Std Dev	11

Turn on : 29.5989

Width : 3.495

Height : 10.050

Entry



B0L001S, U17-ch30

calib_packv5_042523_0143.root, FC#9, port A1

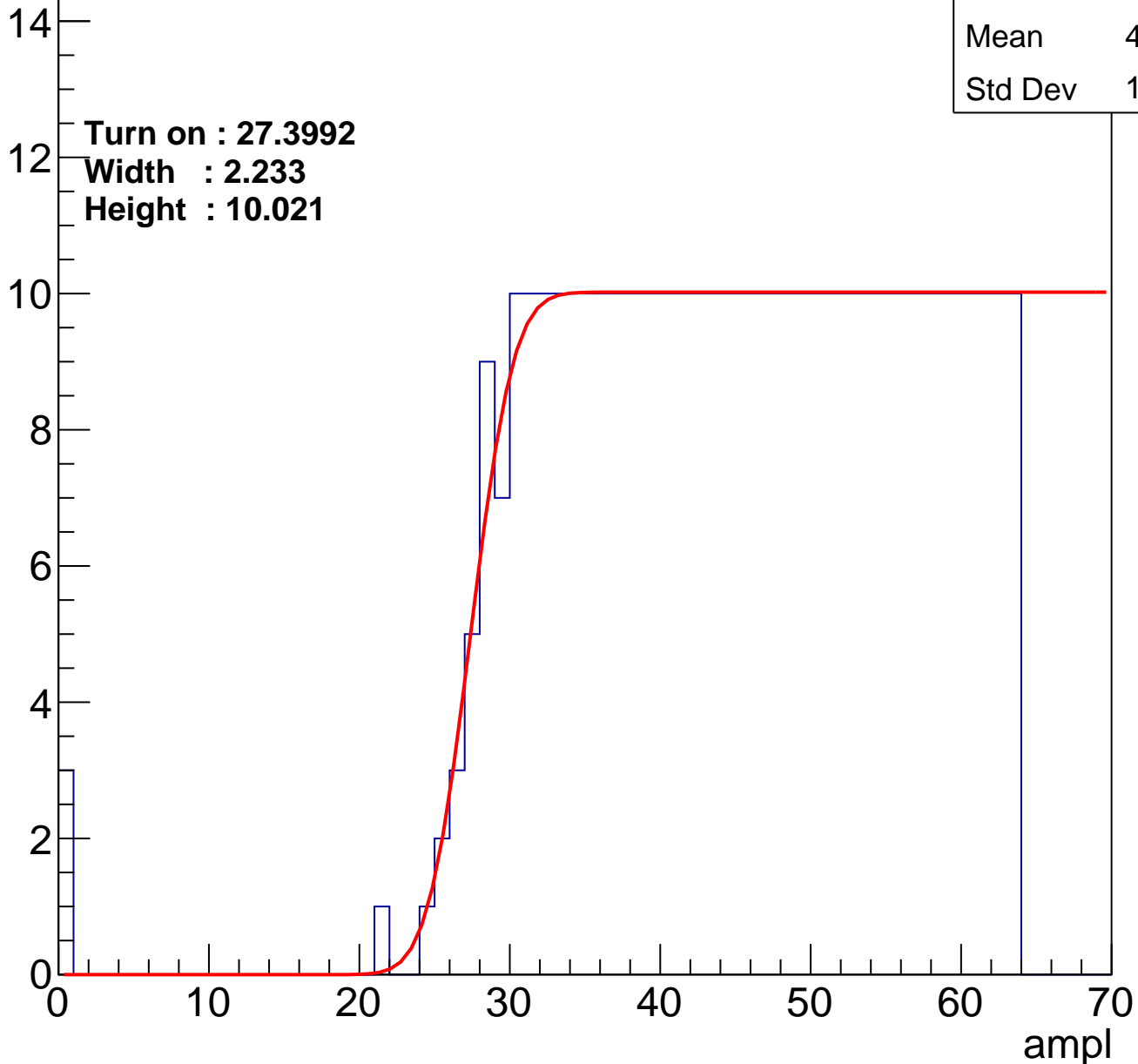
Entries	371
Mean	44.67
Std Dev	11.43

Turn on : 27.3992

Width : 2.233

Height : 10.021

Entry



B0L001S, U17-ch31

calib_packv5_042523_0143.root, FC#9, port A1

Entries	351
Mean	45.68
Std Dev	10.81

Turn on : 29.7331

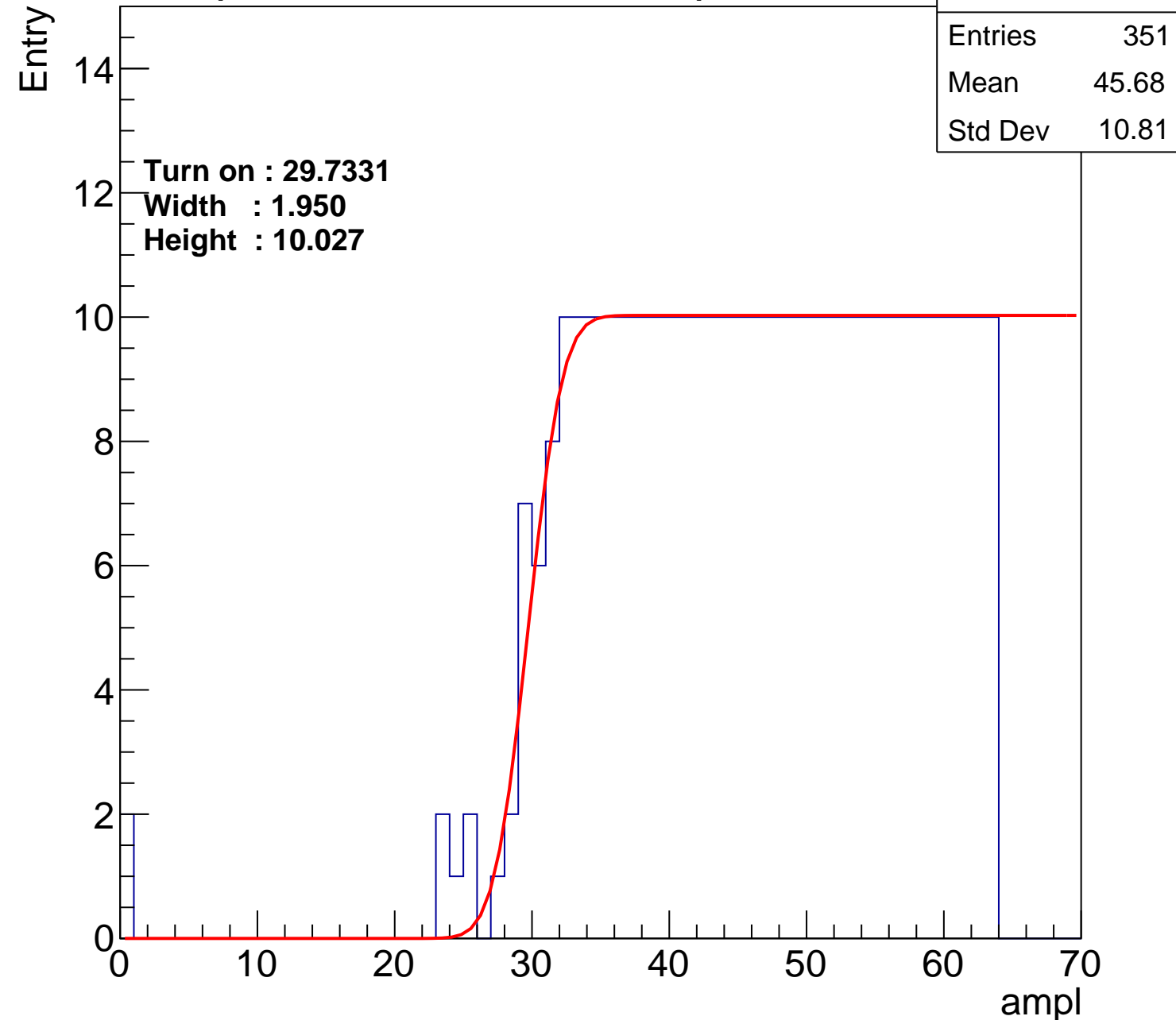
Width : 1.950

Height : 10.027

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch32

calib_packv5_042523_0143.root, FC#9, port A1

Entries	373
Mean	44.47
Std Dev	11.64

Turn on : 27.7317

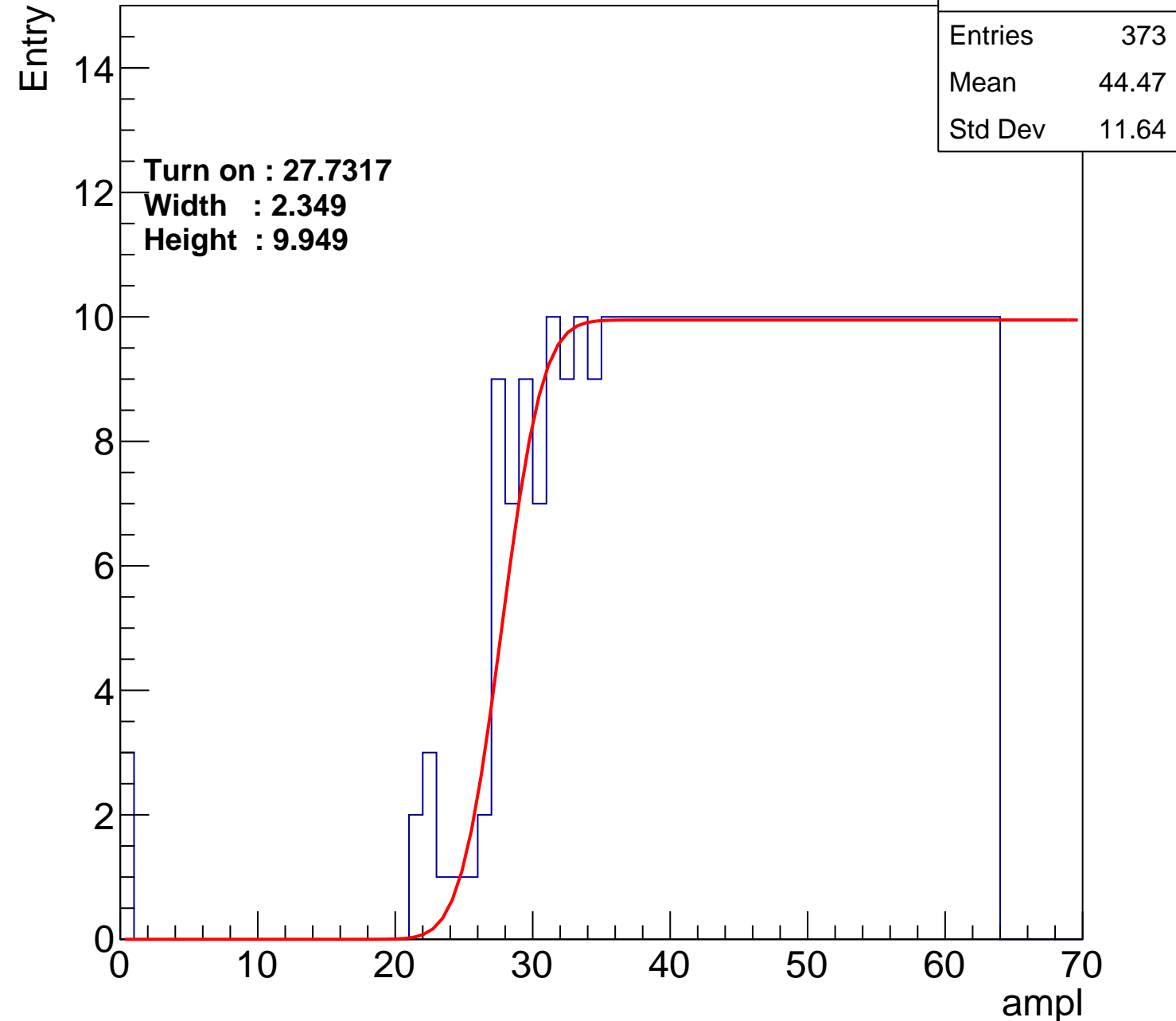
Width : 2.349

Height : 9.949

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch33

calib_packv5_042523_0143.root, FC#9, port A1

Entries	363
Mean	44.94
Std Dev	11.51

Turn on : 28.3243

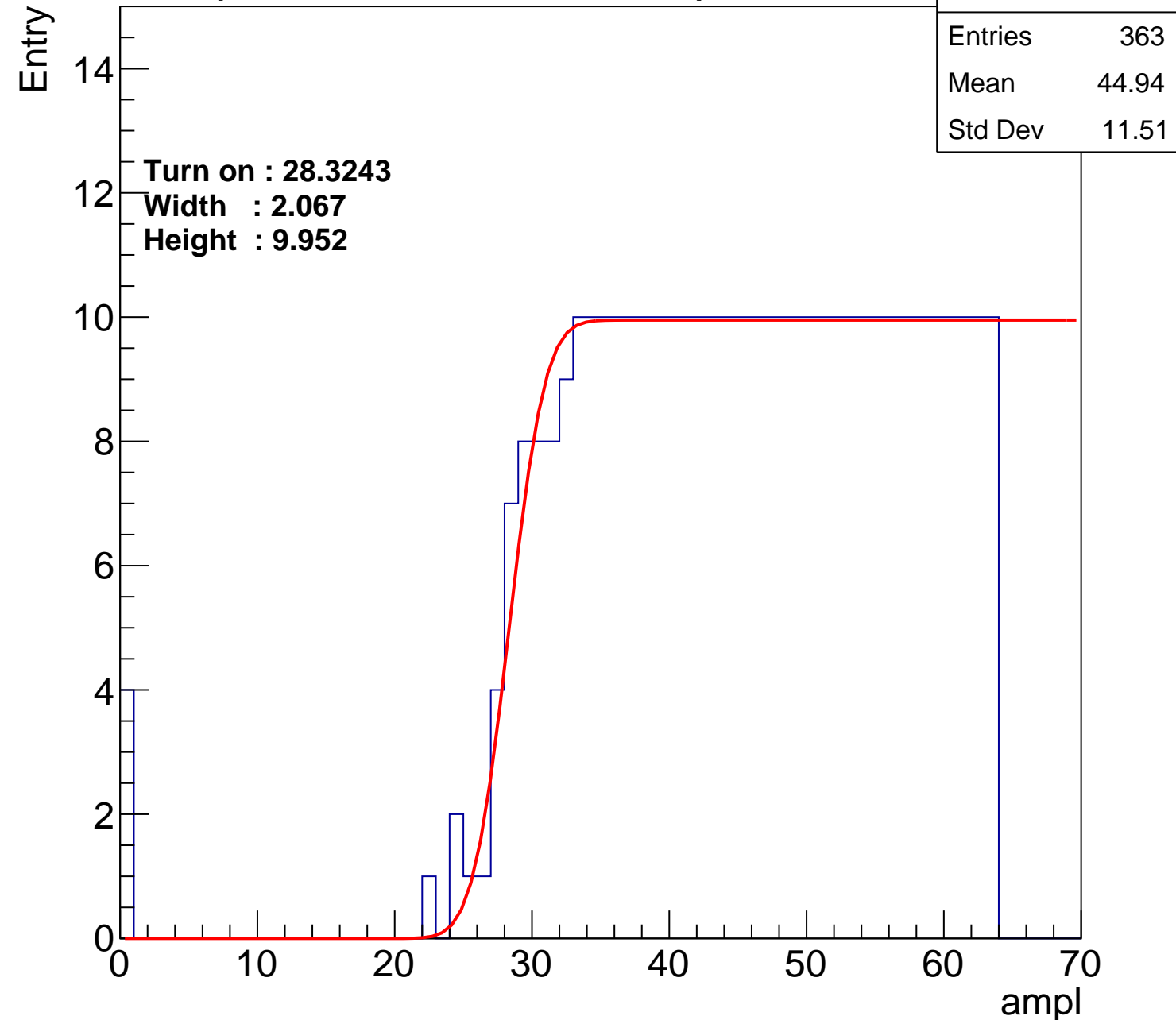
Width : 2.067

Height : 9.952

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch34

calib_packv5_042523_0143.root, FC#9, port A1

Entries	367
Mean	44.88
Std Dev	11.21

Turn on : 27.4888

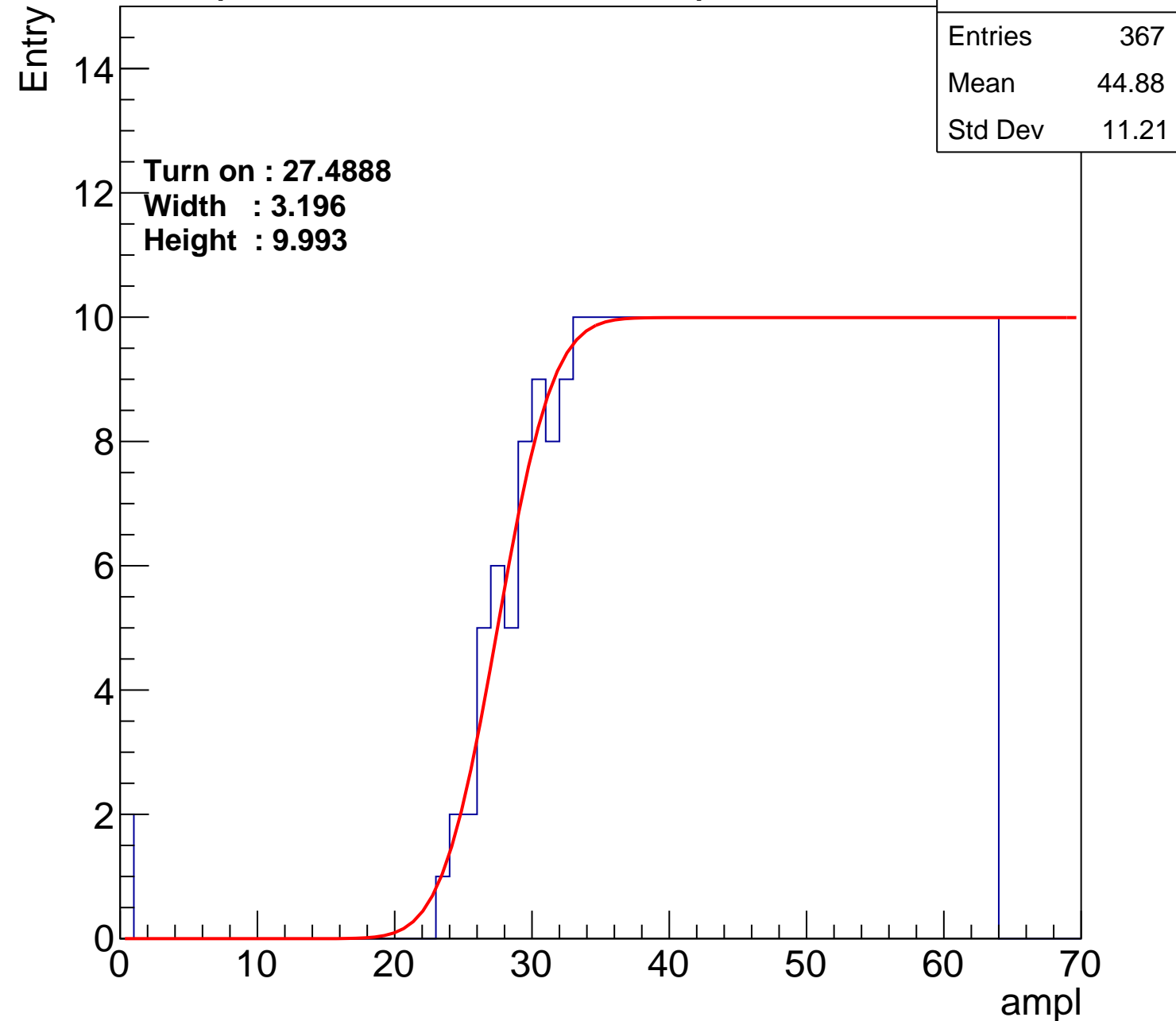
Width : 3.196

Height : 9.993

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch35

calib_packv5_042523_0143.root, FC#9, port A1

Entries	349
Mean	45.68
Std Dev	11.02

Turn on : 30.0974

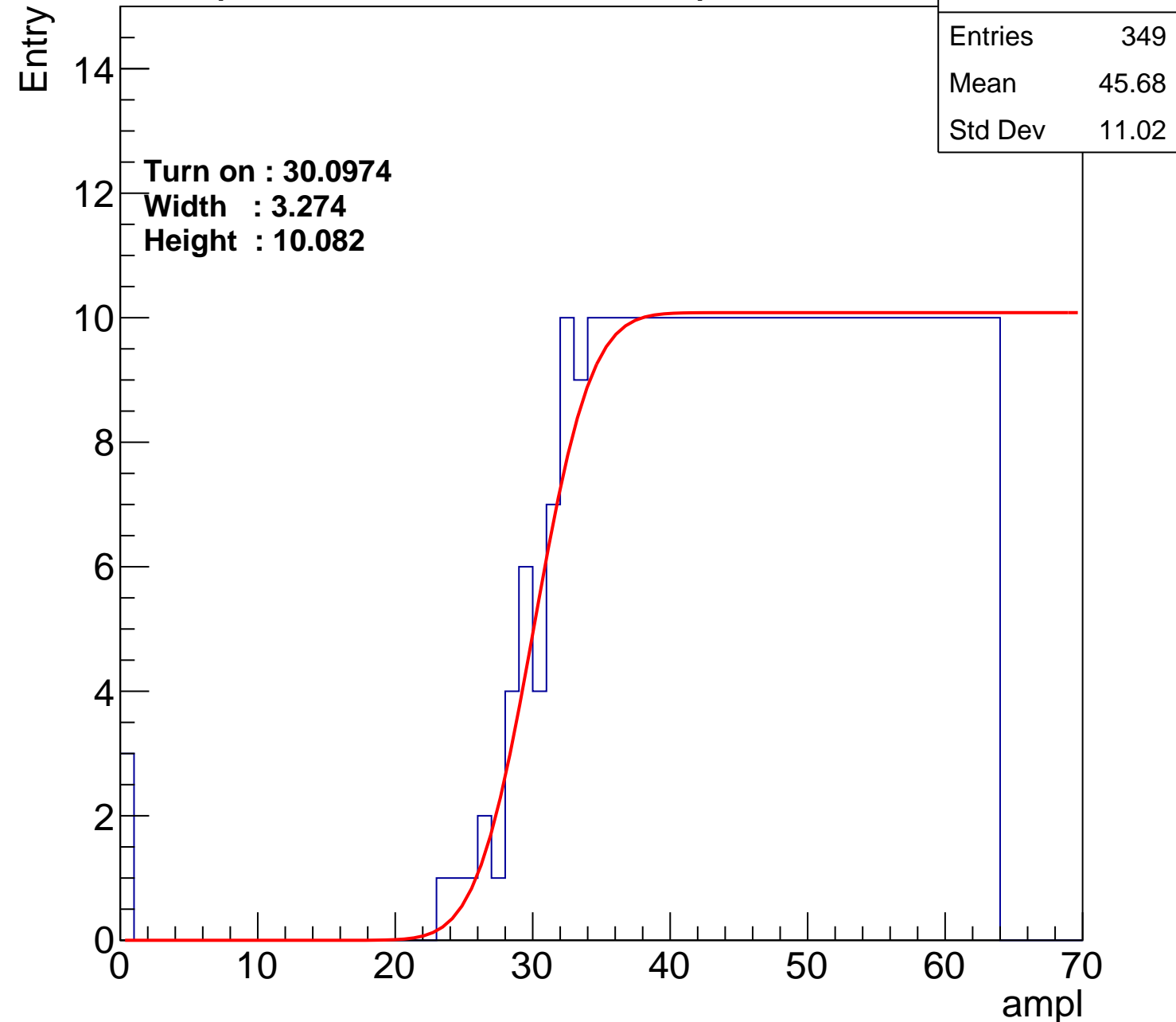
Width : 3.274

Height : 10.082

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch36

calib_packv5_042523_0143.root, FC#9, port A1

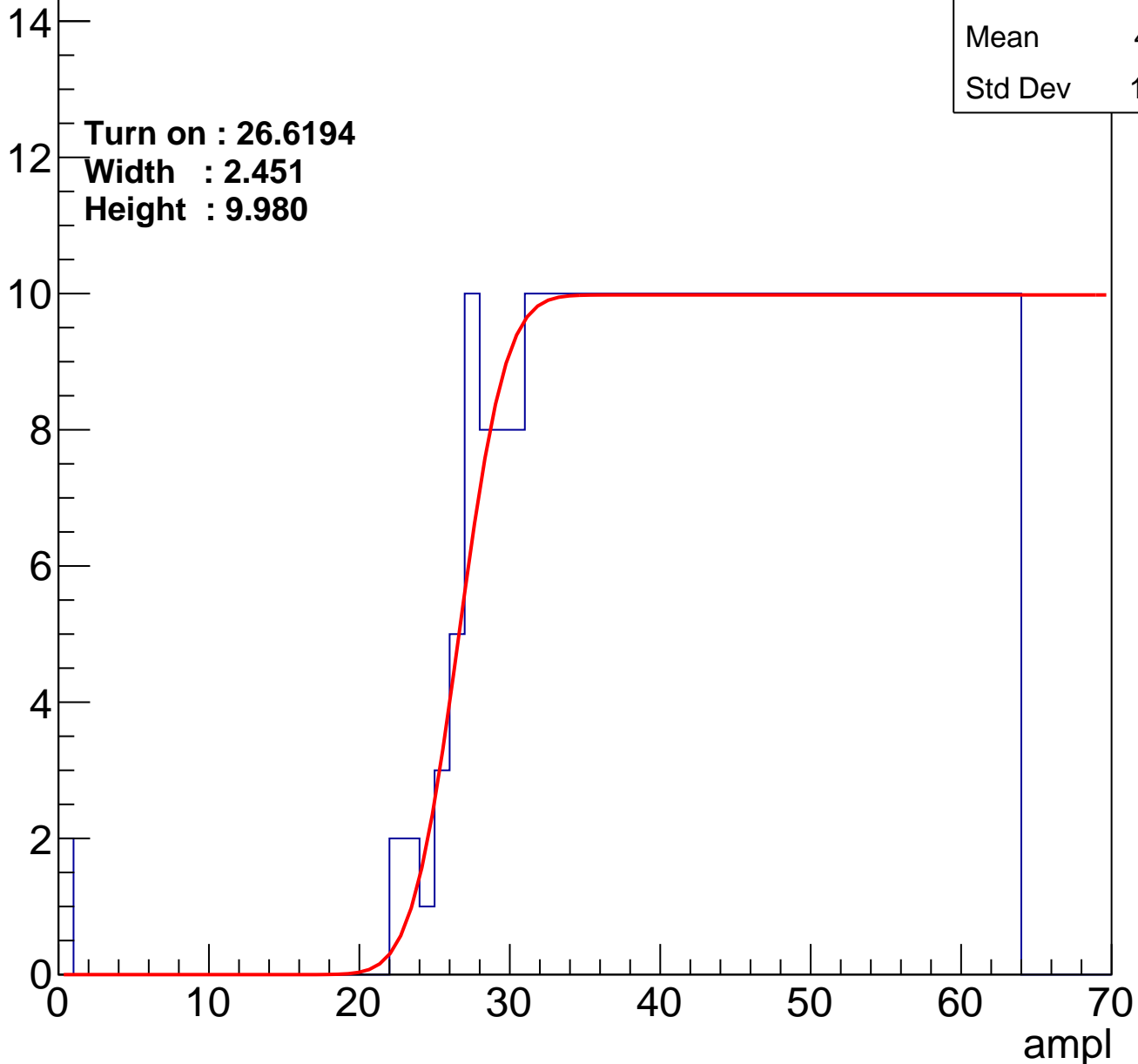
Entries	379
Mean	44.31
Std Dev	11.48

Turn on : 26.6194

Width : 2.451

Height : 9.980

Entry



B0L001S, U17-ch37

calib_packv5_042523_0143.root, FC#9, port A1

Entries	366
Mean	44.95
Std Dev	11.17

Turn on : 27.5298

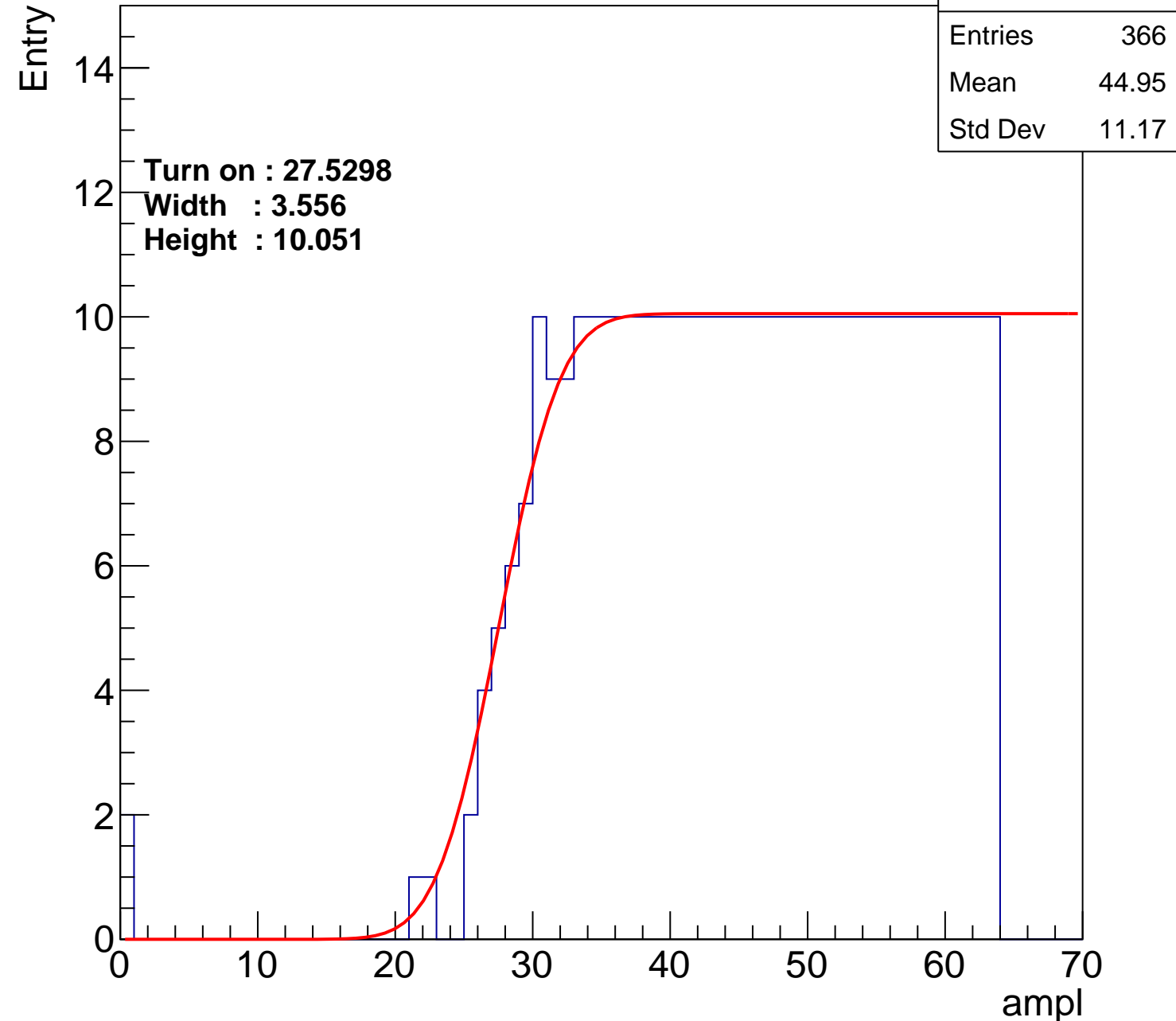
Width : 3.556

Height : 10.051

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch38

calib_packv5_042523_0143.root, FC#9, port A1

Entries	362
Mean	45.12
Std Dev	11.2

Turn on : 28.2153

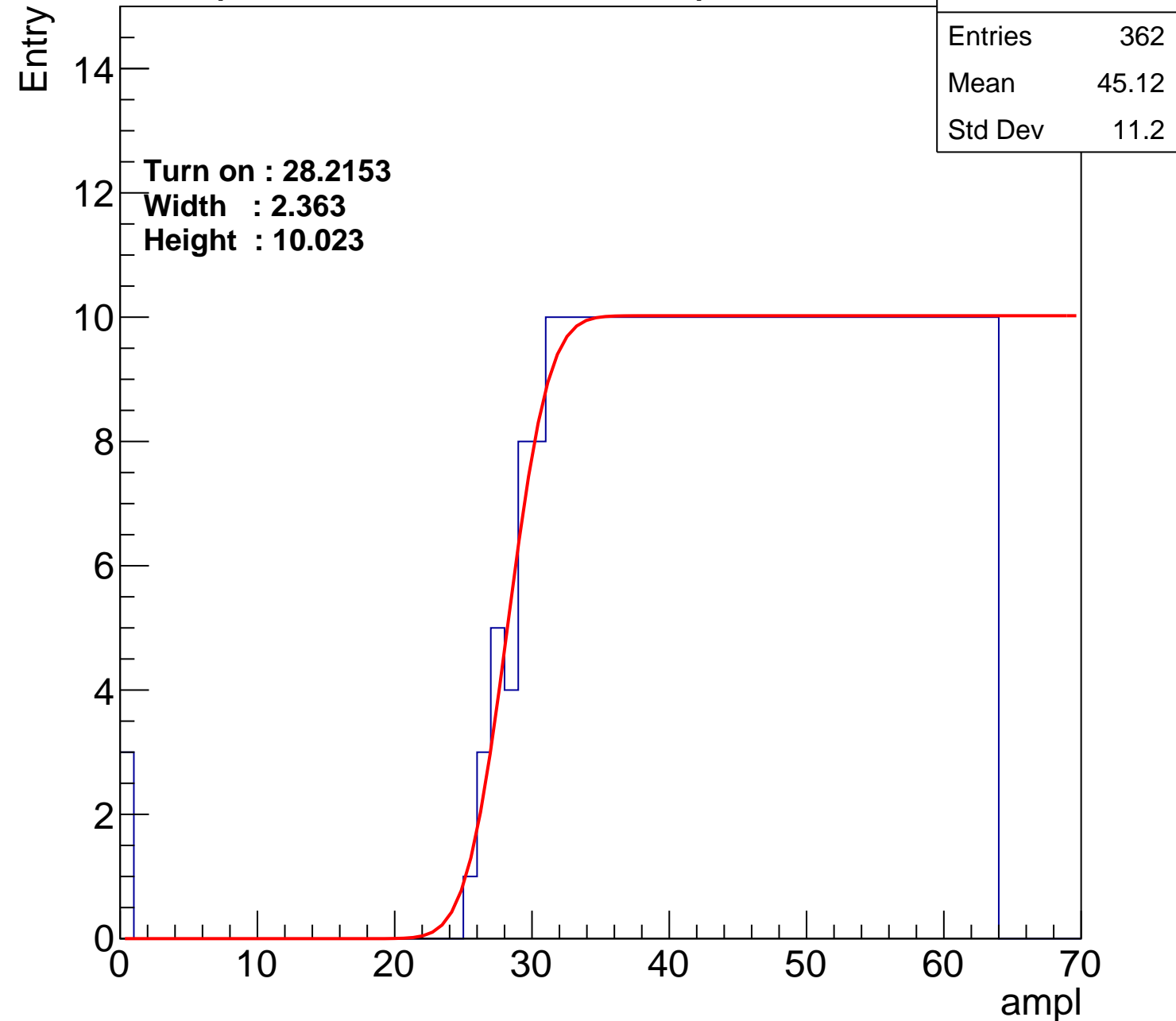
Width : 2.363

Height : 10.023

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch39

calib_packv5_042523_0143.root, FC#9, port A1

Entries	369
Mean	44.59
Std Dev	11.72

Turn on : 27.3895

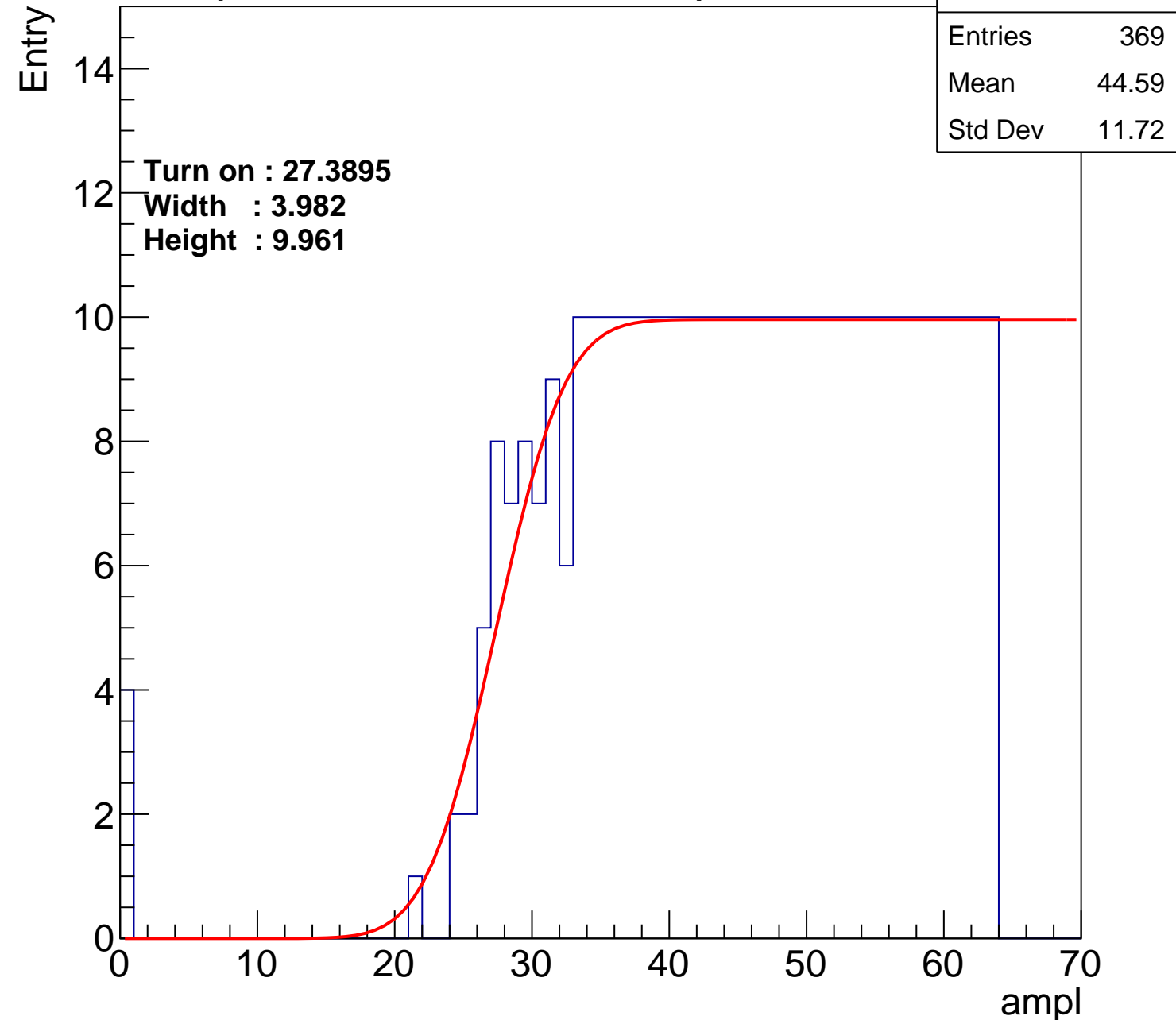
Width : 3.982

Height : 9.961

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch40

calib_packv5_042523_0143.root, FC#9, port A1

Entries	352
Mean	45.55
Std Dev	11.05

Turn on : 29.3810

Width : 2.812

Height : 10.008

Entry

14

12

10

8

6

4

2

0

0

10

20

30

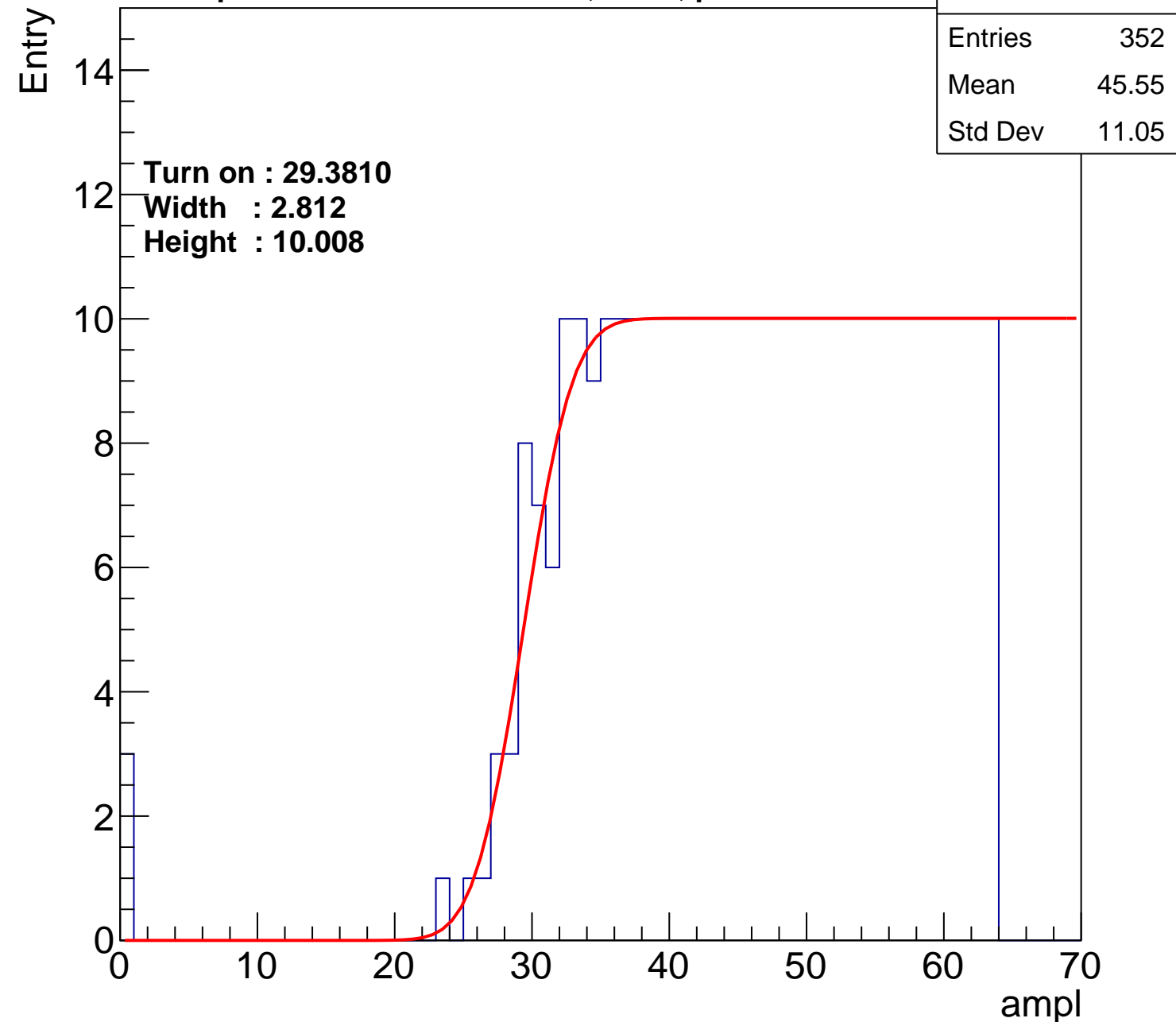
40

50

60

70

ampl



B0L001S, U17-ch41

calib_packv5_042523_0143.root, FC#9, port A1

Entries	358
Mean	45.14
Std Dev	11.46

Turn on : 28.3871

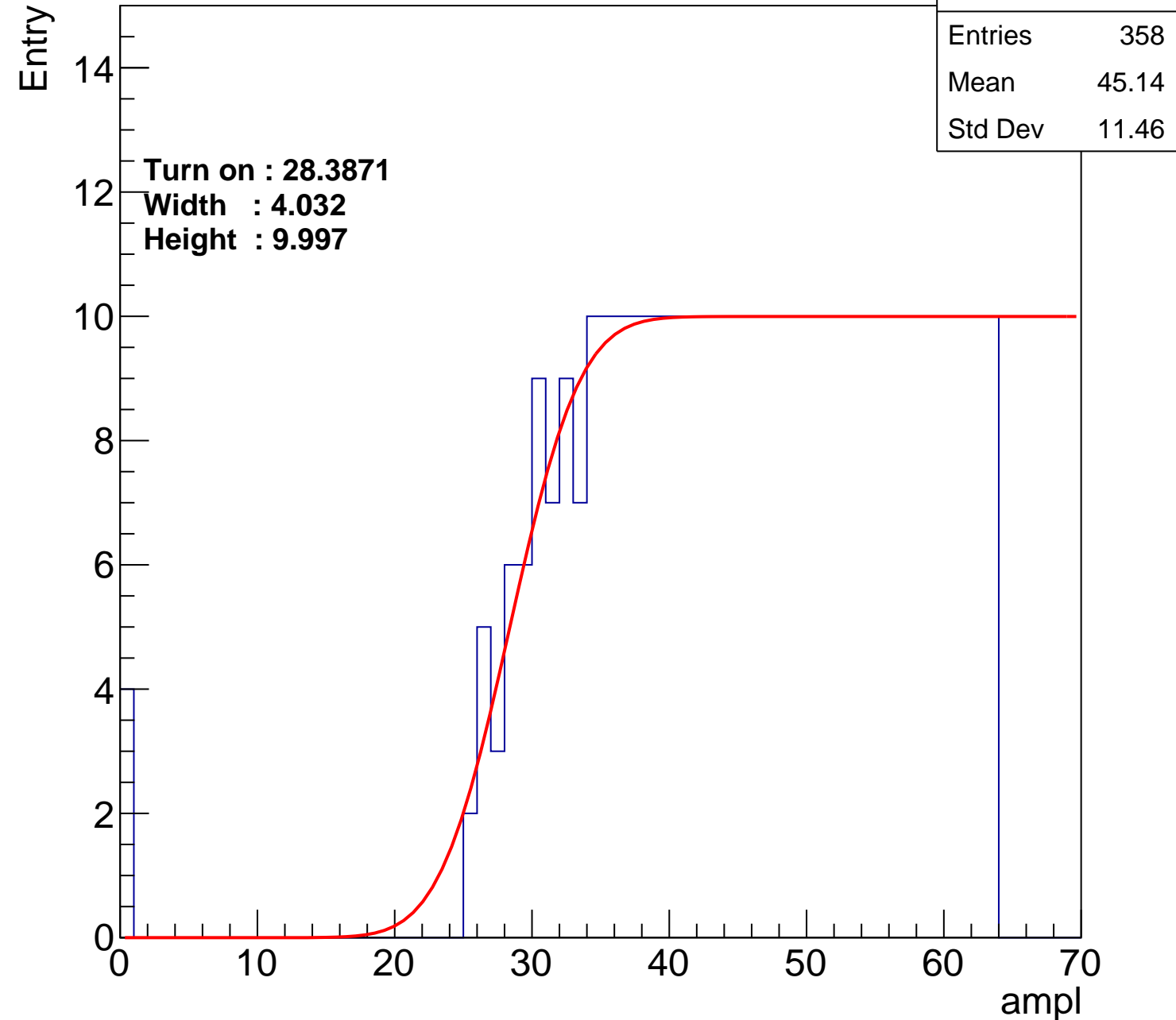
Width : 4.032

Height : 9.997

Entry

14
12
10
8
6
4
2
0

ampl



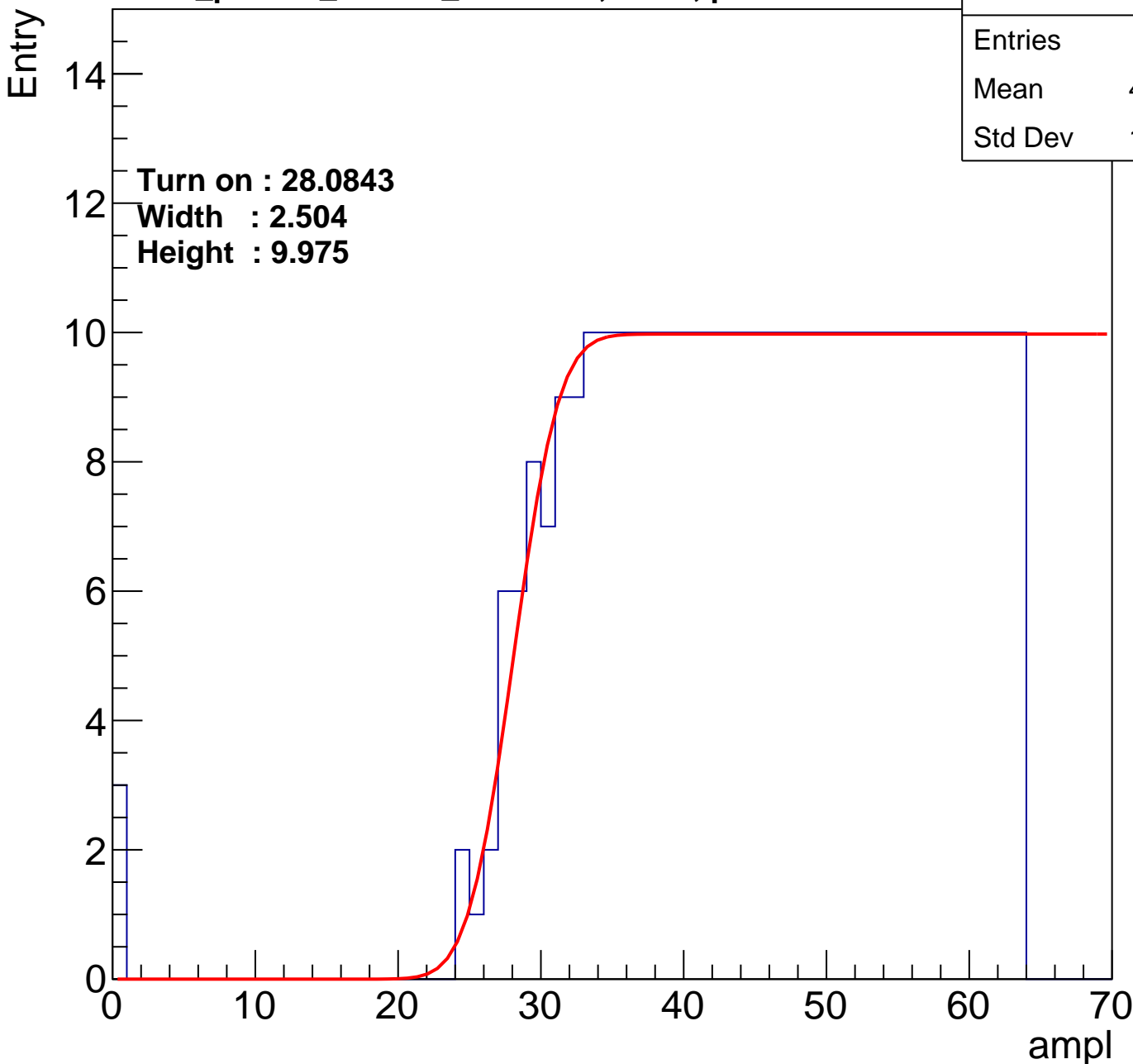
calib_packv5_042523_0143.root, FC#9, port A1

calib_packv5_042523_0143.root, FC#9, port A1

Entries	363
Mean	45.02
Std Dev	11.29

Width : 2.504

Height : 9.975



B0L001S, U17-ch43

calib_packv5_042523_0143.root, FC#9, port A1

Entries	358
Mean	45.07
Std Dev	11.65

Turn on : 28.7379

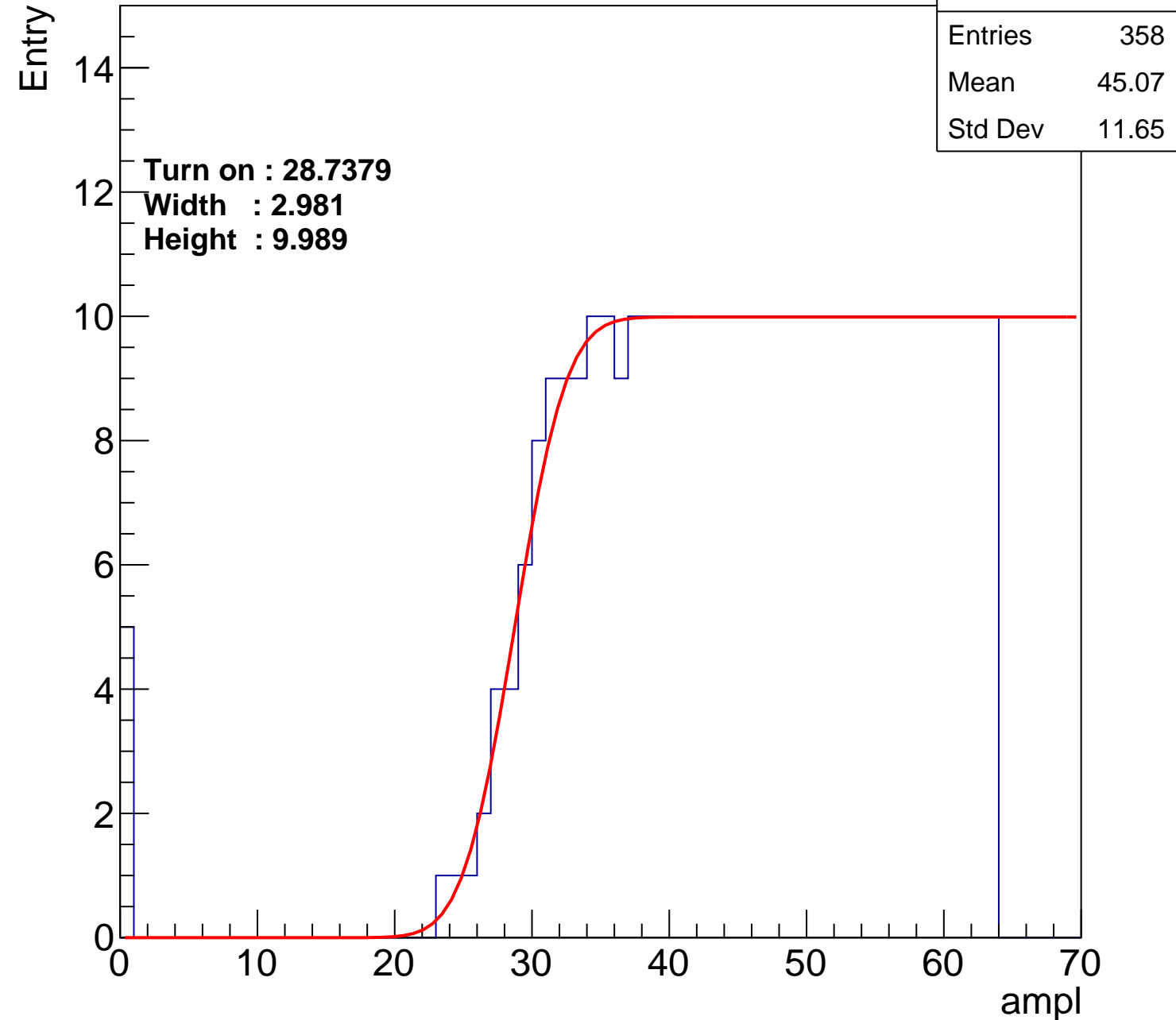
Width : 2.981

Height : 9.989

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch44

calib_packv5_042523_0143.root, FC#9, port A1

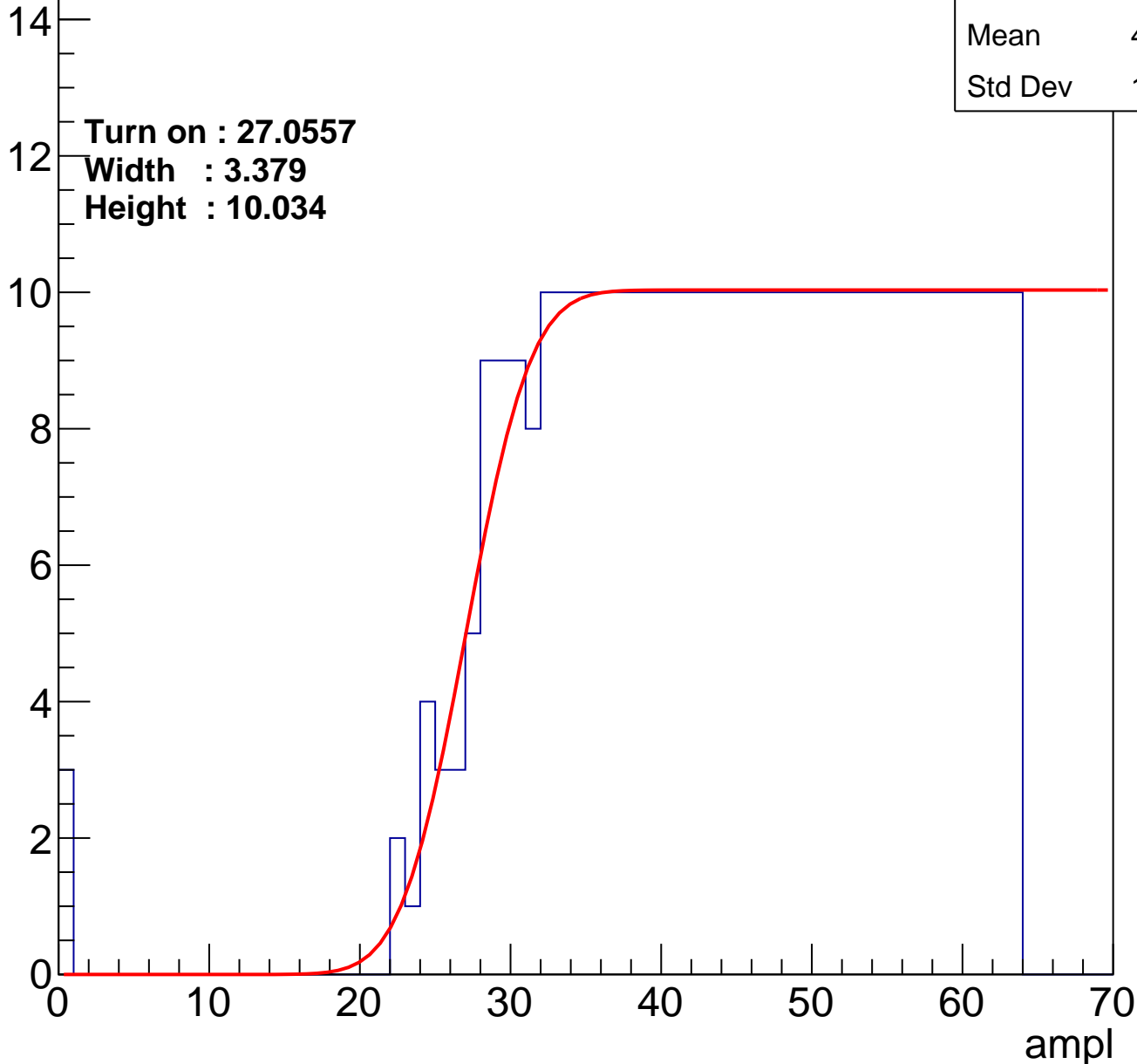
Entries	376
Mean	44.37
Std Dev	11.64

Turn on : 27.0557

Width : 3.379

Height : 10.034

Entry



B0L001S, U17-ch45

calib_packv5_042523_0143.root, FC#9, port A1

Entries	357
Mean	45.22
Std Dev	11.38

Turn on : 28.6020

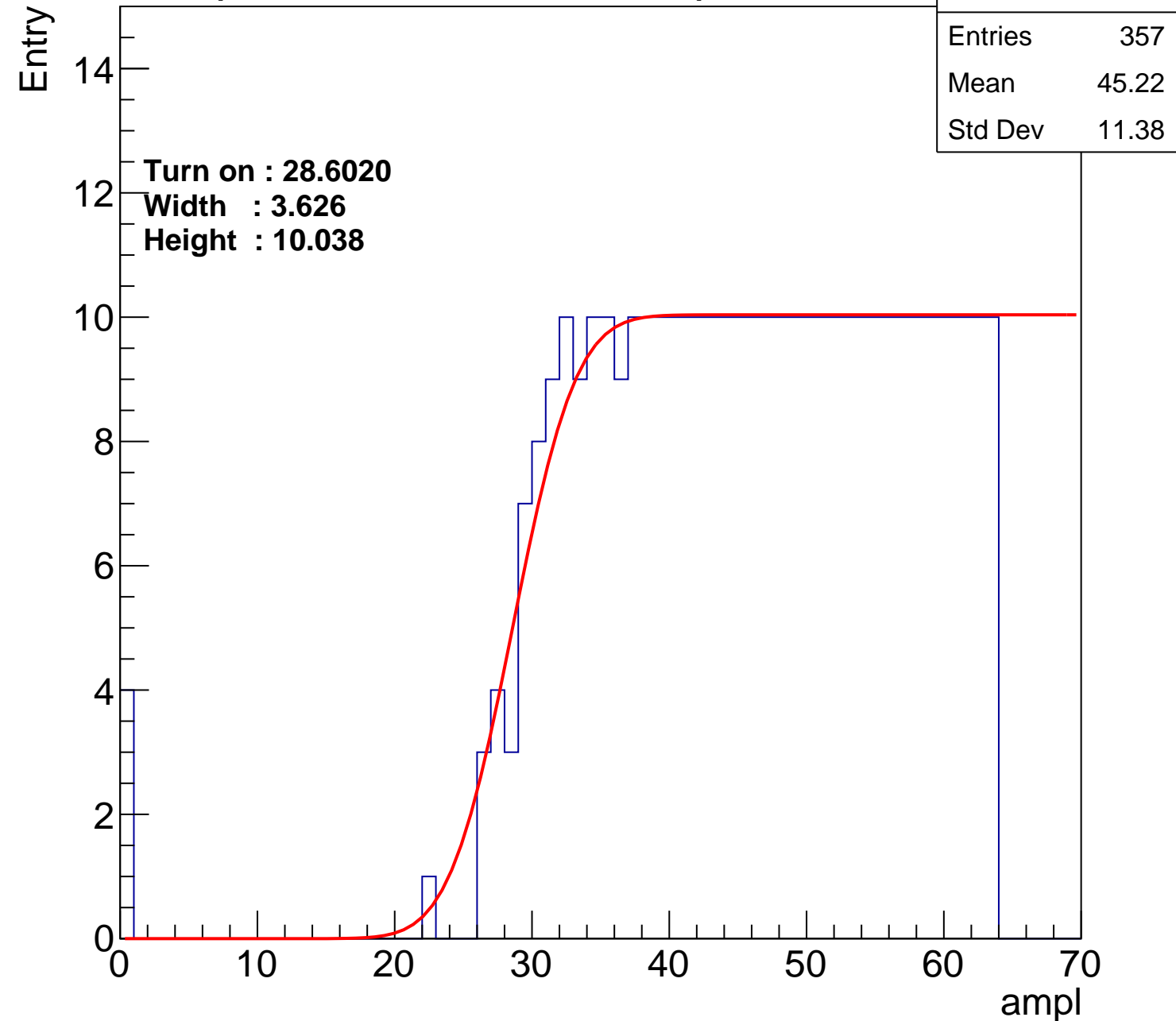
Width : 3.626

Height : 10.038

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch46

calib_packv5_042523_0143.root, FC#9, port A1

Entries	354
Mean	45.18
Std Dev	11.81

Turn on : 29.6811

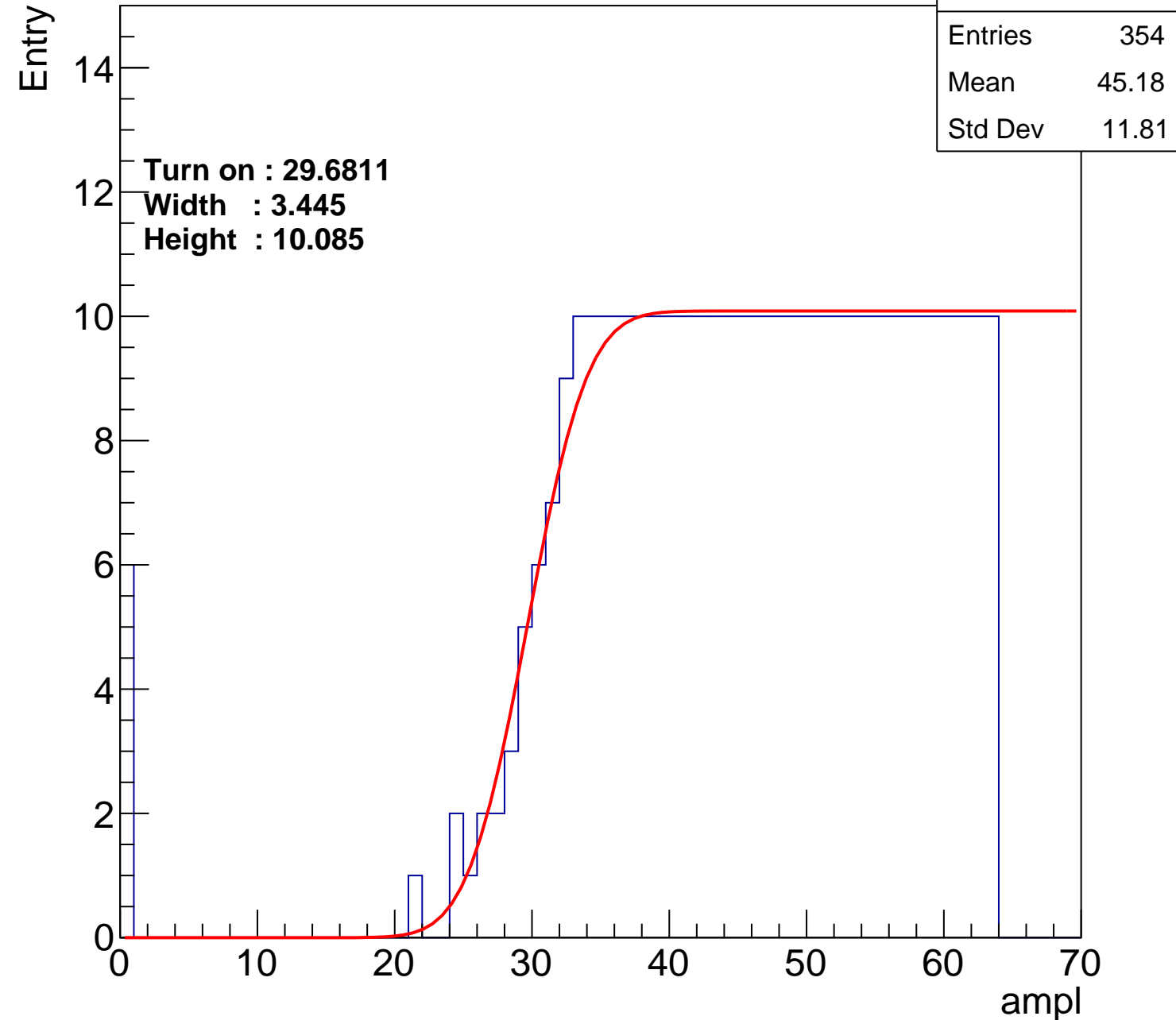
Width : 3.445

Height : 10.085

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch47

calib_packv5_042523_0143.root, FC#9, port A1

Entries	366
Mean	44.9
Std Dev	11.32

Turn on : 27.5093

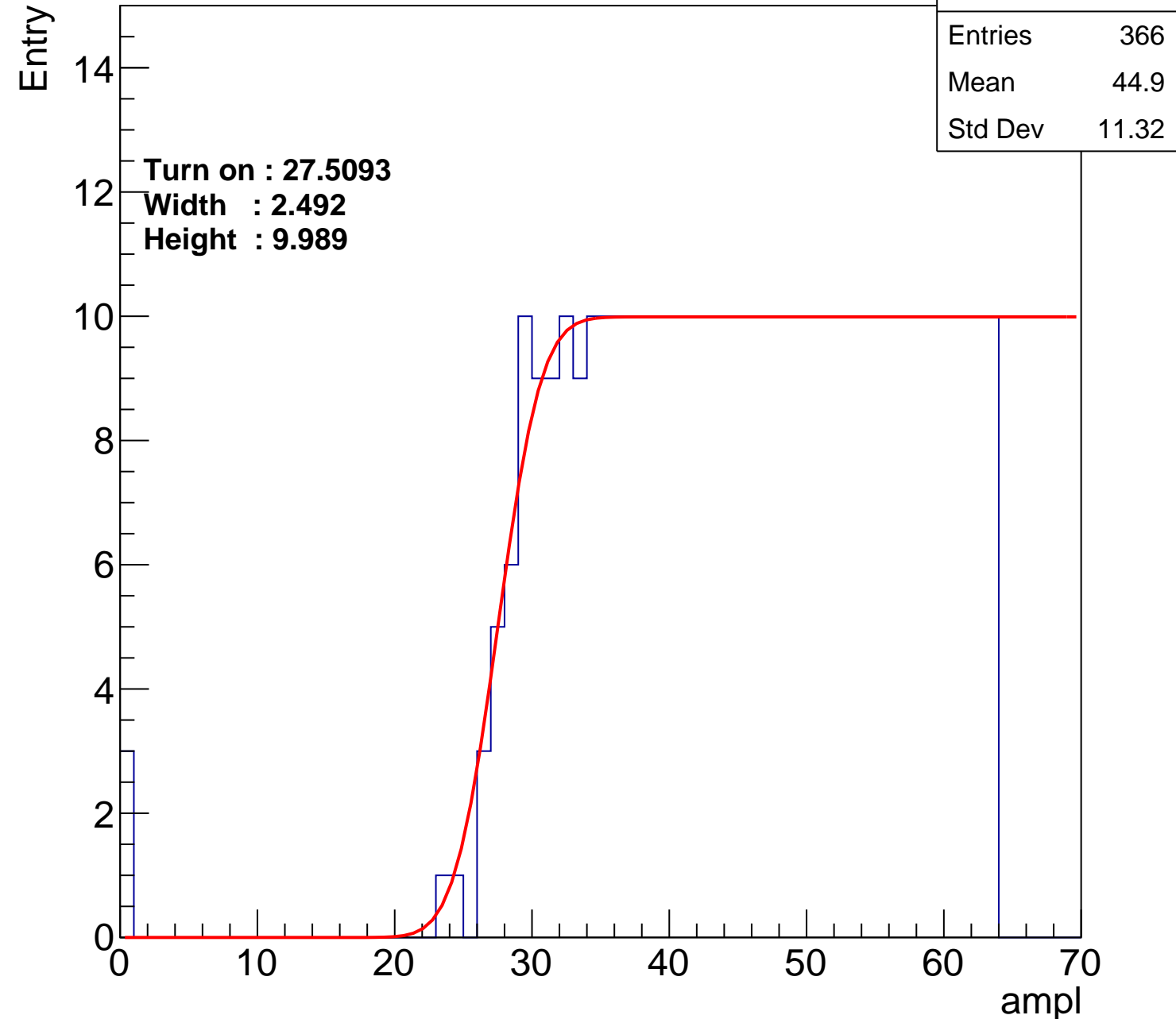
Width : 2.492

Height : 9.989

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch48

calib_packv5_042523_0143.root, FC#9, port A1

Entries	360
Mean	45.25
Std Dev	11

Turn on : 28.5901

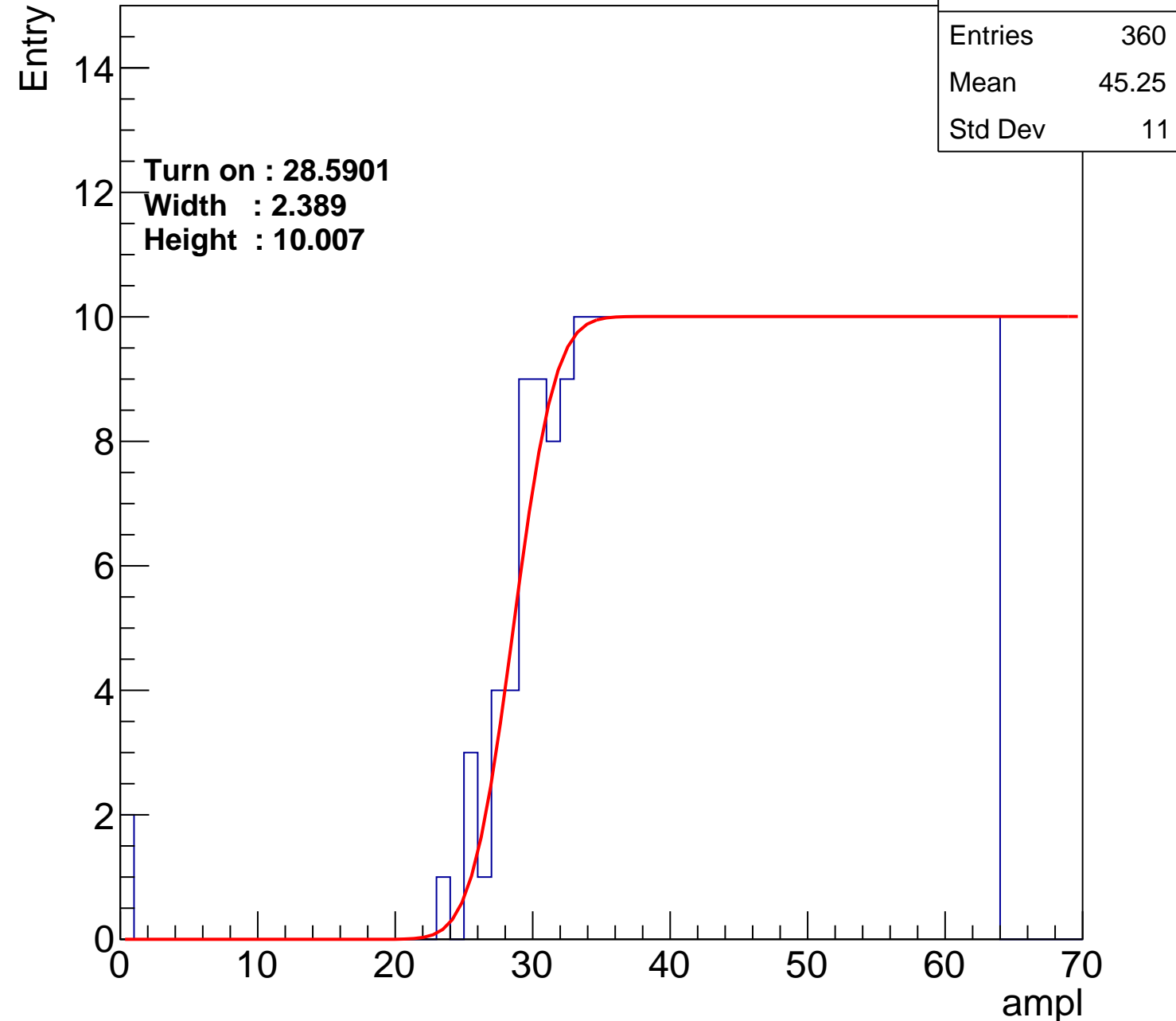
Width : 2.389

Height : 10.007

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch49

calib_packv5_042523_0143.root, FC#9, port A1

Entries	376
Mean	44.11
Std Dev	12.33

Turn on : 27.2508

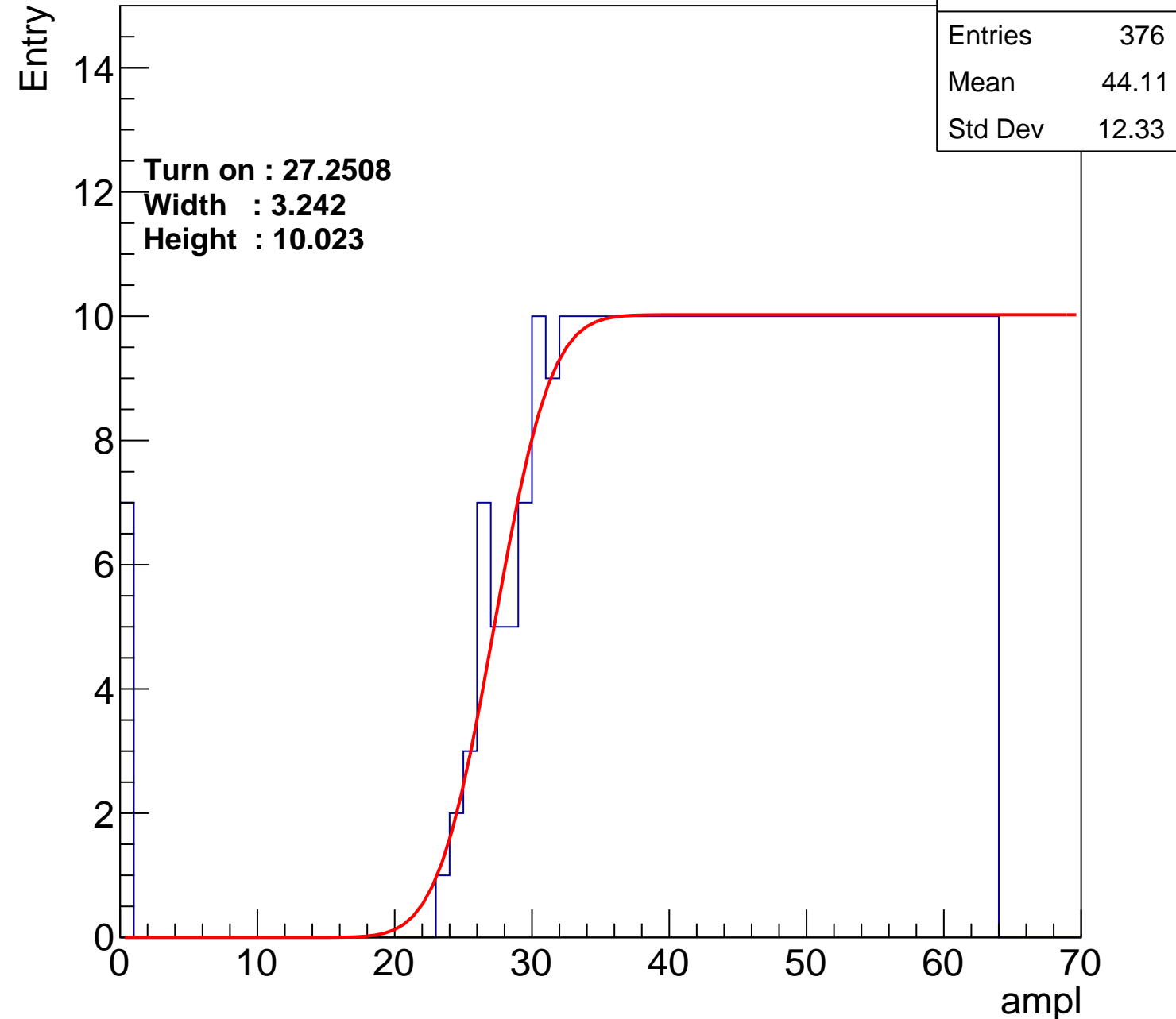
Width : 3.242

Height : 10.023

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch50

calib_packv5_042523_0143.root, FC#9, port A1

Entries	369
Mean	44.61
Std Dev	11.71

Turn on : 27.9329

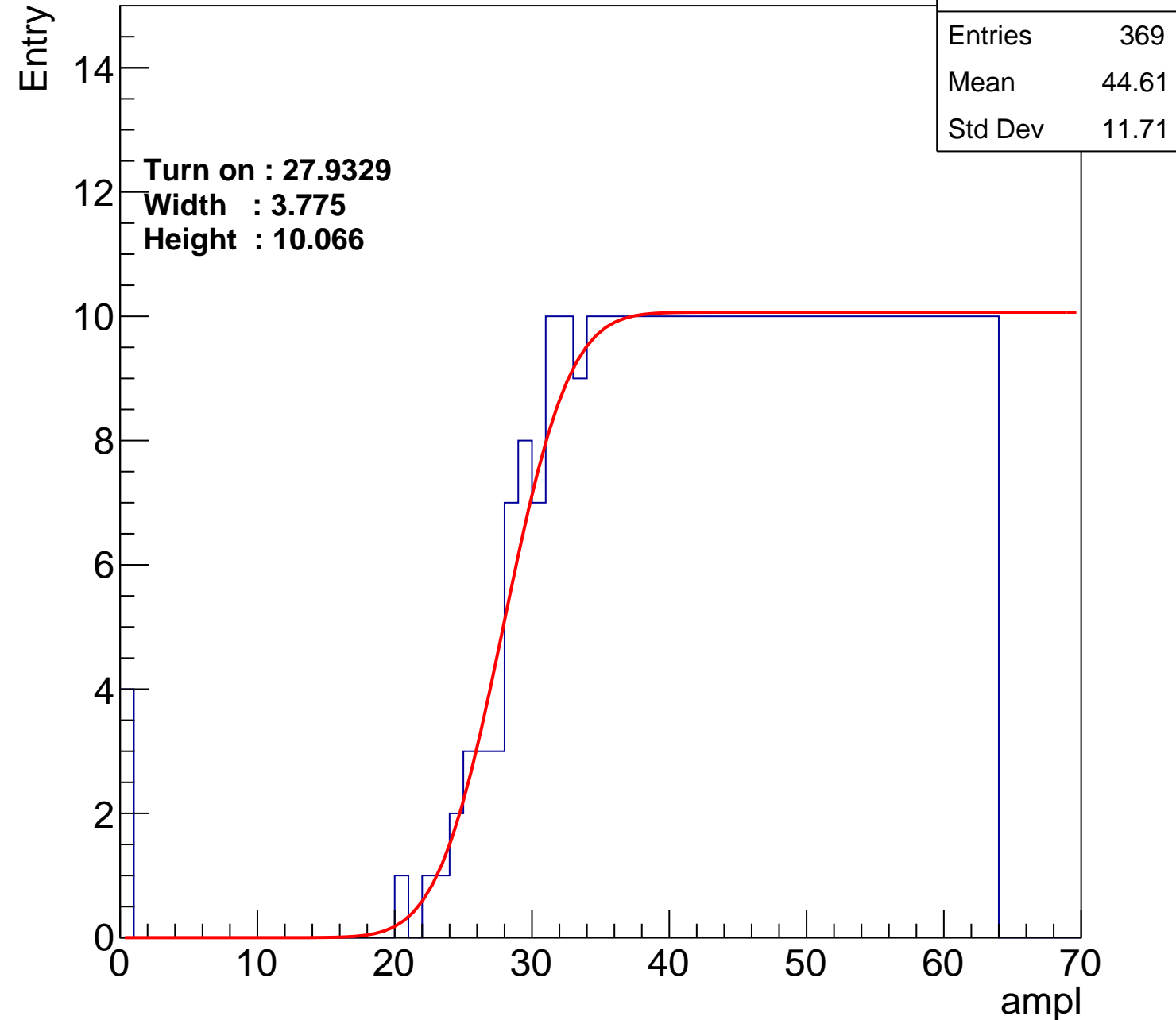
Width : 3.775

Height : 10.066

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch51

calib_packv5_042523_0143.root, FC#9, port A1

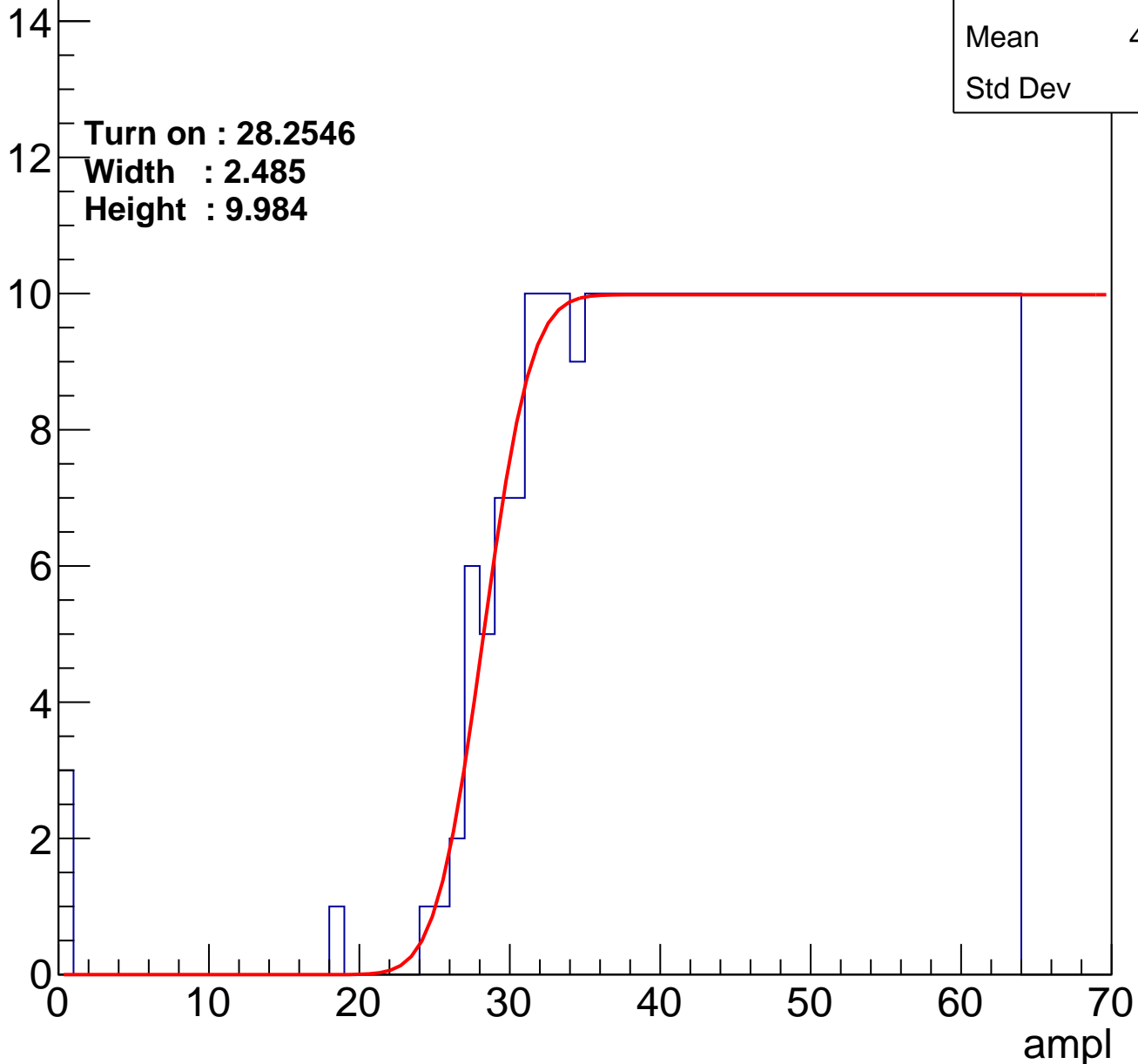
Entries	362
Mean	45.06
Std Dev	11.3

Turn on : 28.2546

Width : 2.485

Height : 9.984

Entry



B0L001S, U17-ch52

calib_packv5_042523_0143.root, FC#9, port A1

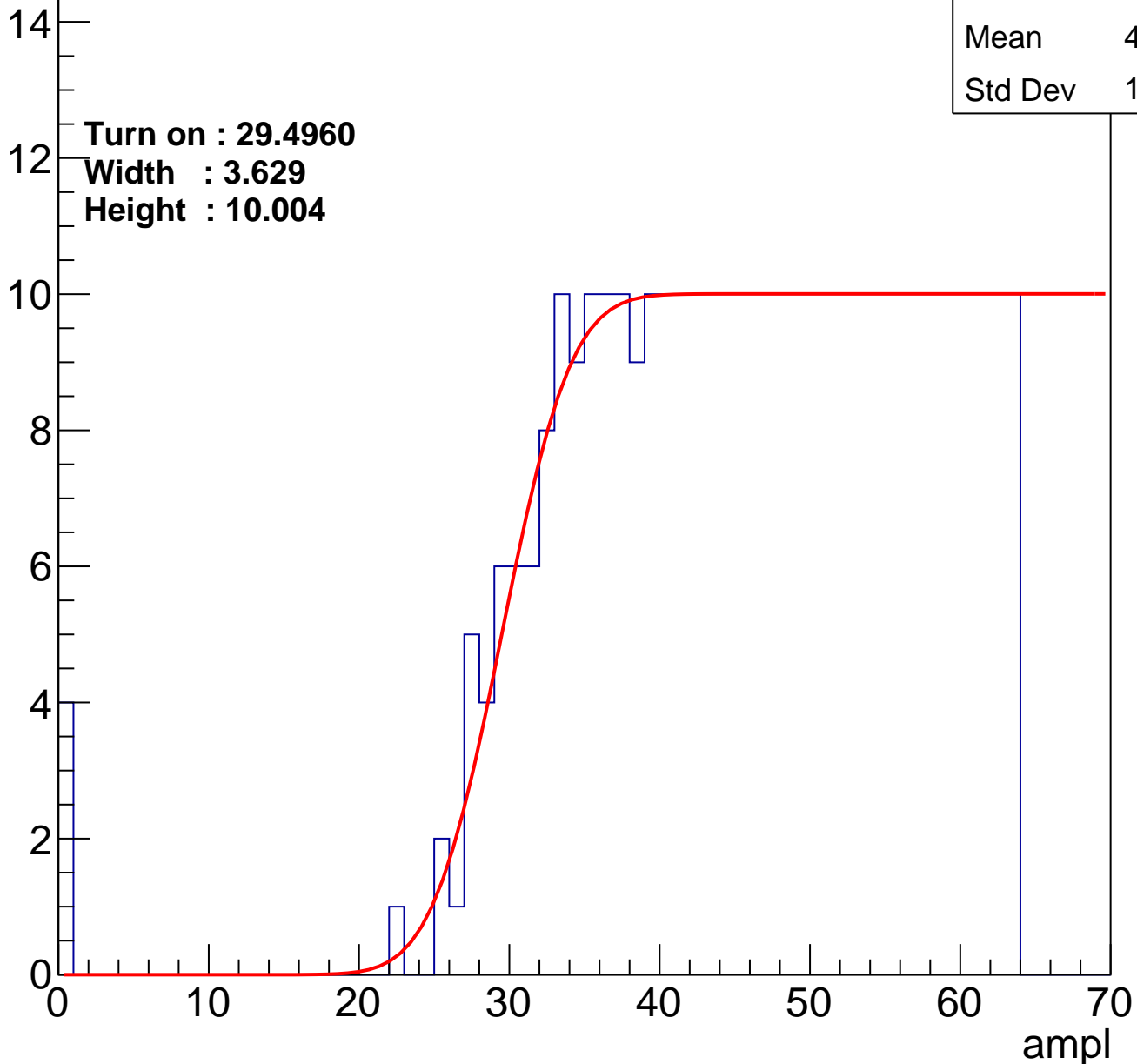
Entries	351
Mean	45.44
Std Dev	11.36

Turn on : 29.4960

Width : 3.629

Height : 10.004

Entry



B0L001S, U17-ch53

calib_packv5_042523_0143.root, FC#9, port A1

Entries	355
Mean	45.39
Std Dev	11.15

Turn on : 29.1442

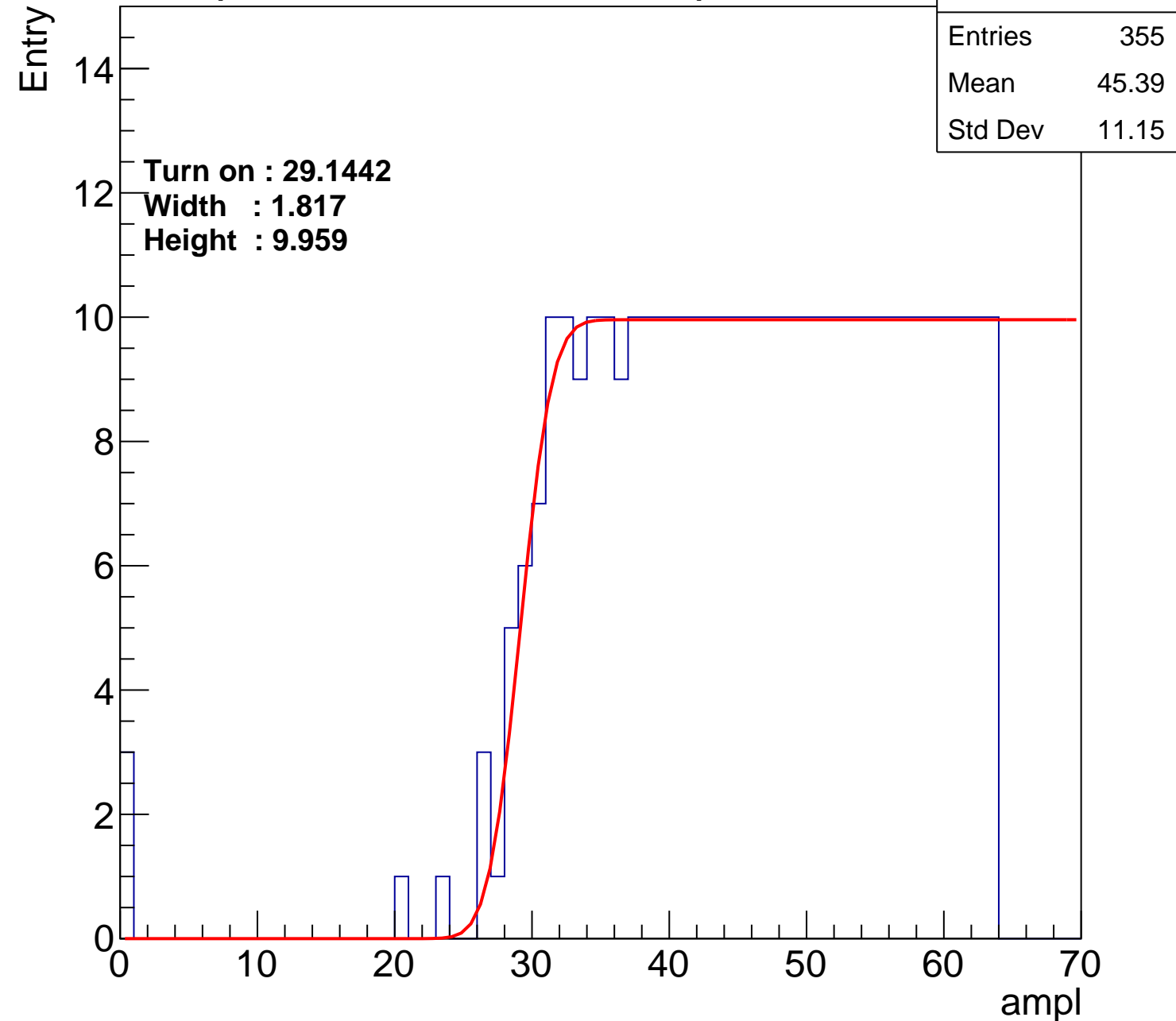
Width : 1.817

Height : 9.959

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch54

calib_packv5_042523_0143.root, FC#9, port A1

Entries	364
Mean	45.05
Std Dev	11.1

Turn on : 27.7619

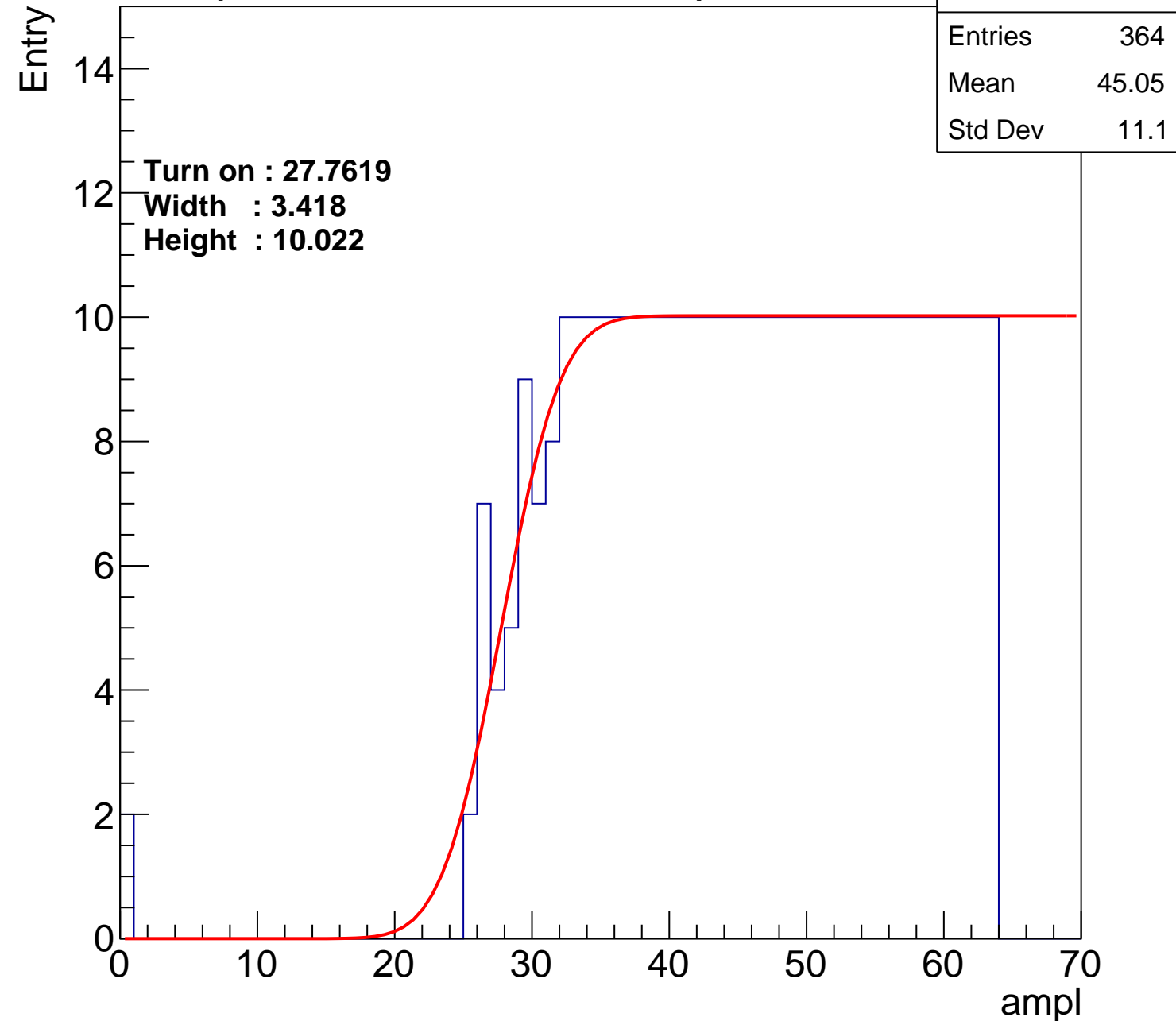
Width : 3.418

Height : 10.022

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch55

calib_packv5_042523_0143.root, FC#9, port A1

Entries	357
Mean	45.16
Std Dev	11.59

Turn on : 29.2181

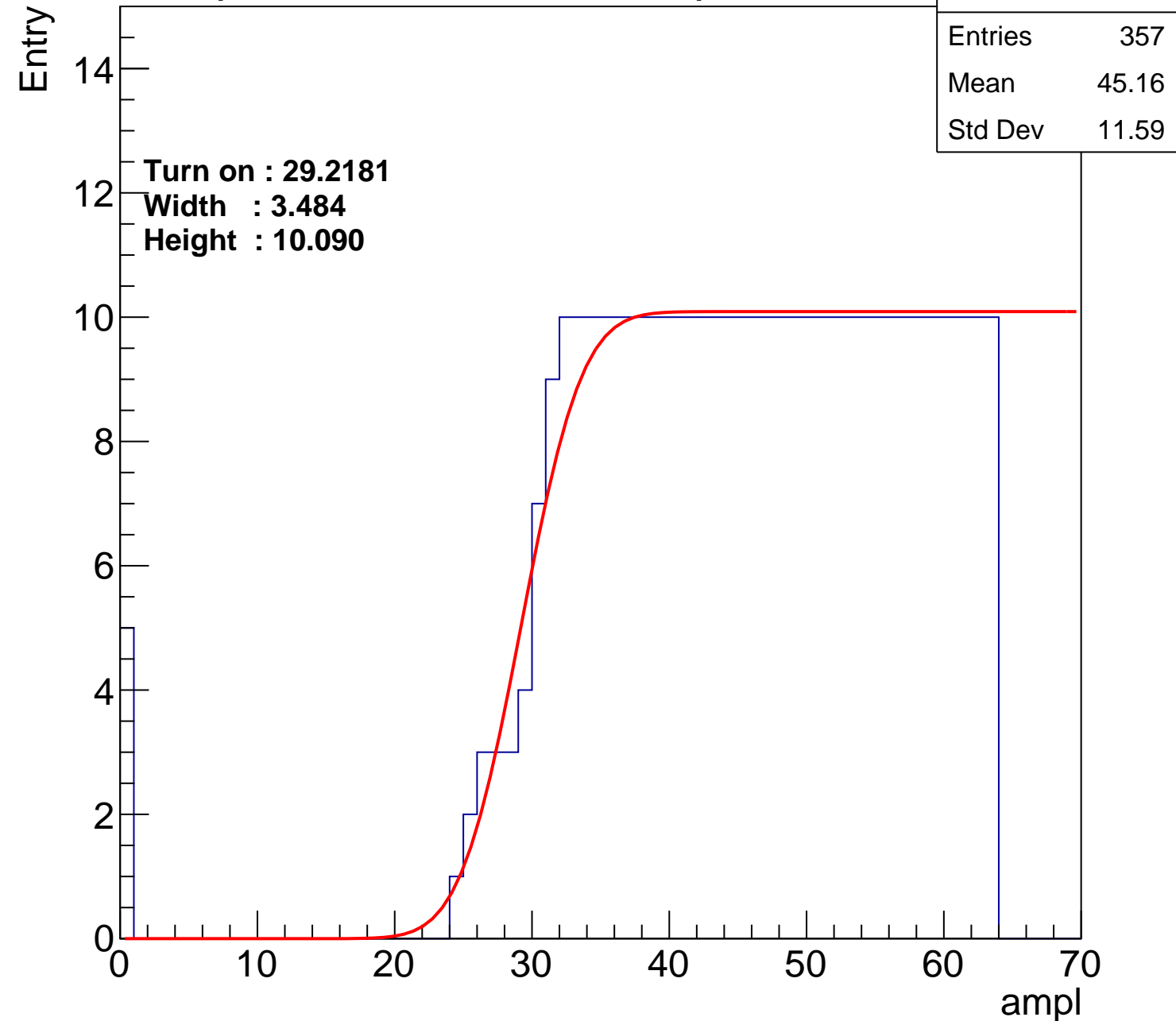
Width : 3.484

Height : 10.090

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch56

calib_packv5_042523_0143.root, FC#9, port A1

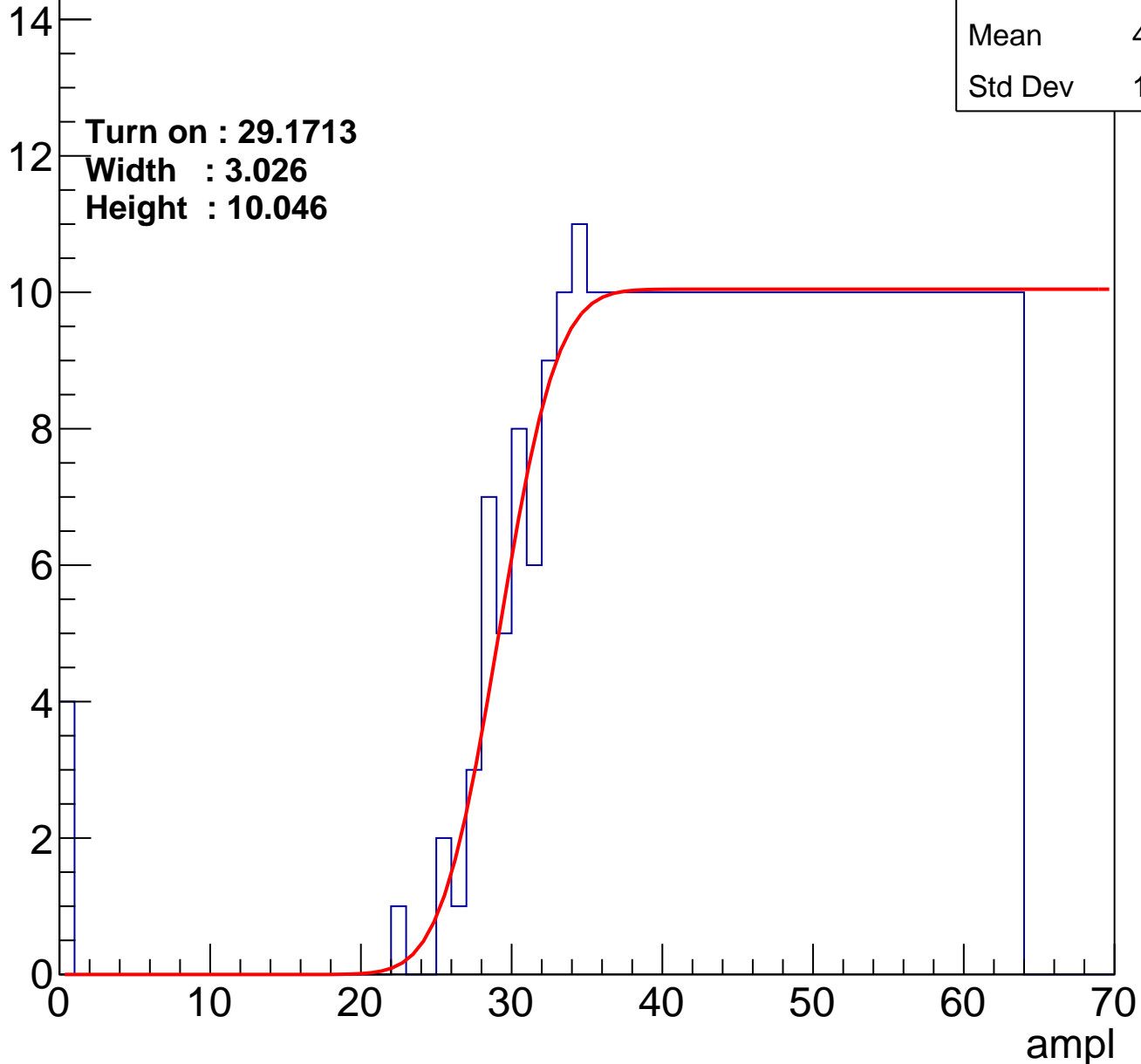
Entries	357
Mean	45.23
Std Dev	11.38

Turn on : 29.1713

Width : 3.026

Height : 10.046

Entry



B0L001S, U17-ch57

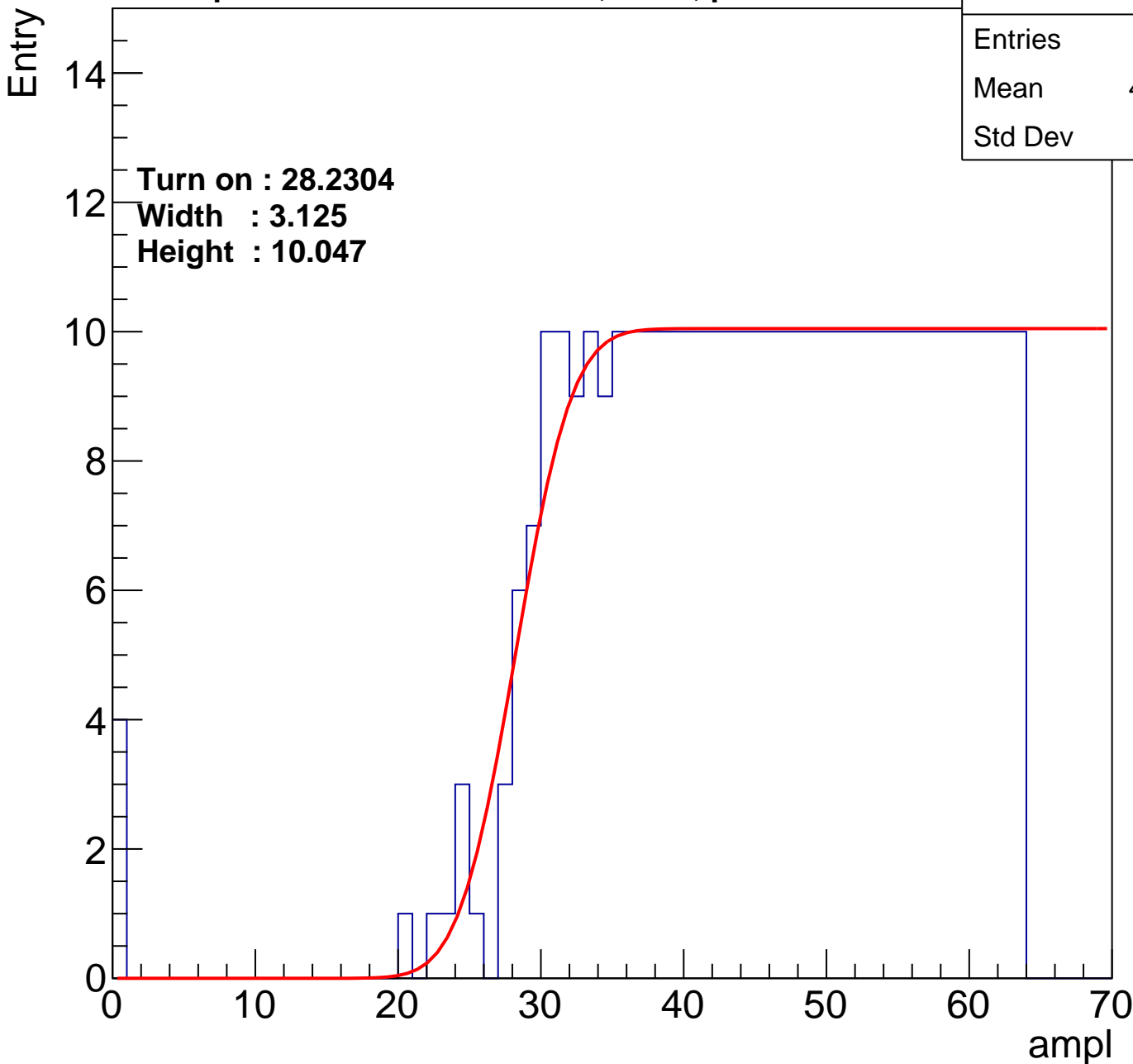
calib_packv5_042523_0143.root, FC#9, port A1

Entries	365
Mean	44.82
Std Dev	11.6

Turn on : 28.2304

Width : 3.125

Height : 10.047



B0L001S, U17-ch58

calib_packv5_042523_0143.root, FC#9, port A1

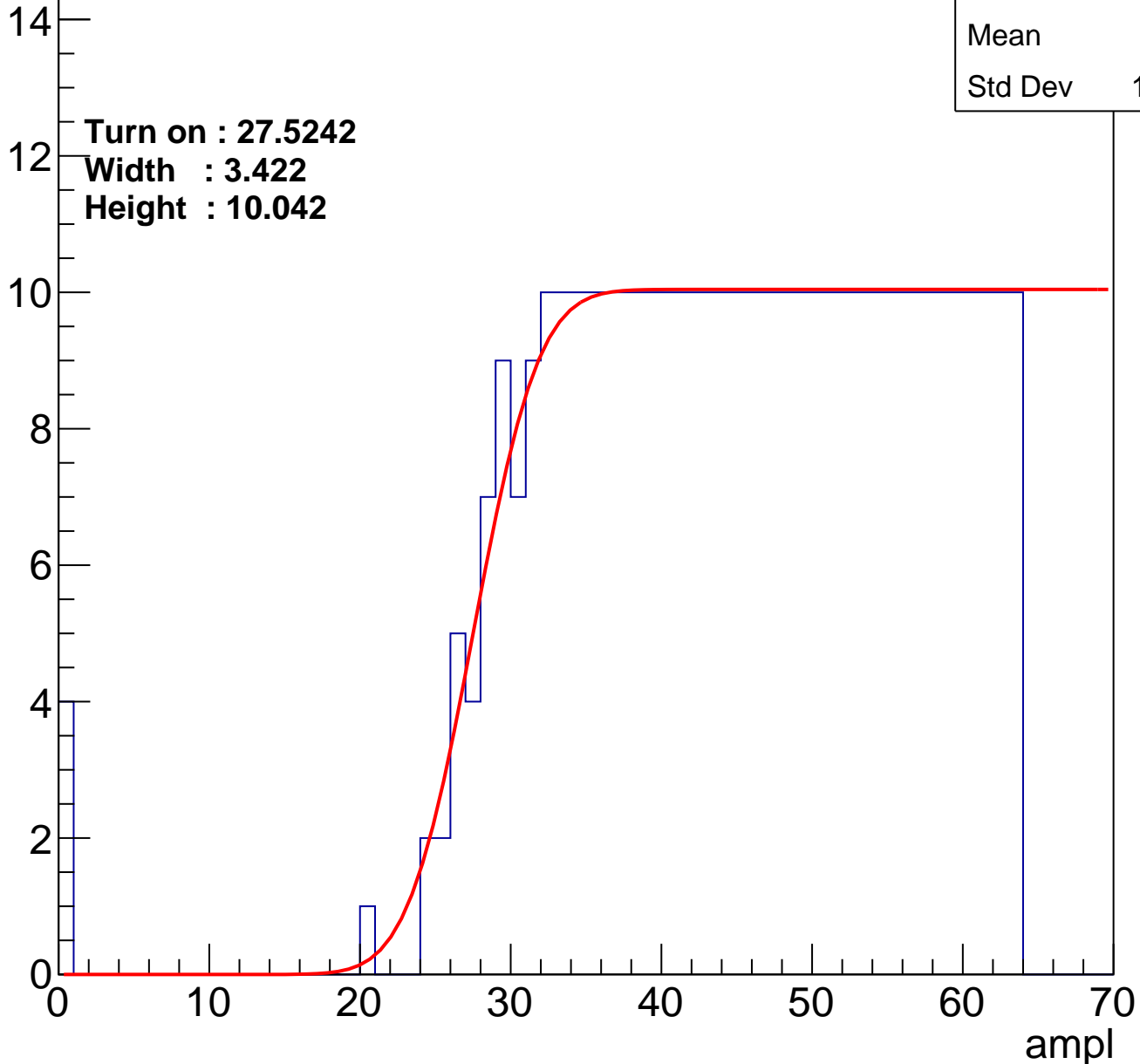
Entries	370
Mean	44.6
Std Dev	11.67

Turn on : 27.5242

Width : 3.422

Height : 10.042

Entry



B0L001S, U17-ch59

calib_packv5_042523_0143.root, FC#9, port A1

Entries	381
Mean	44.11
Std Dev	11.78

Turn on : 26.7034

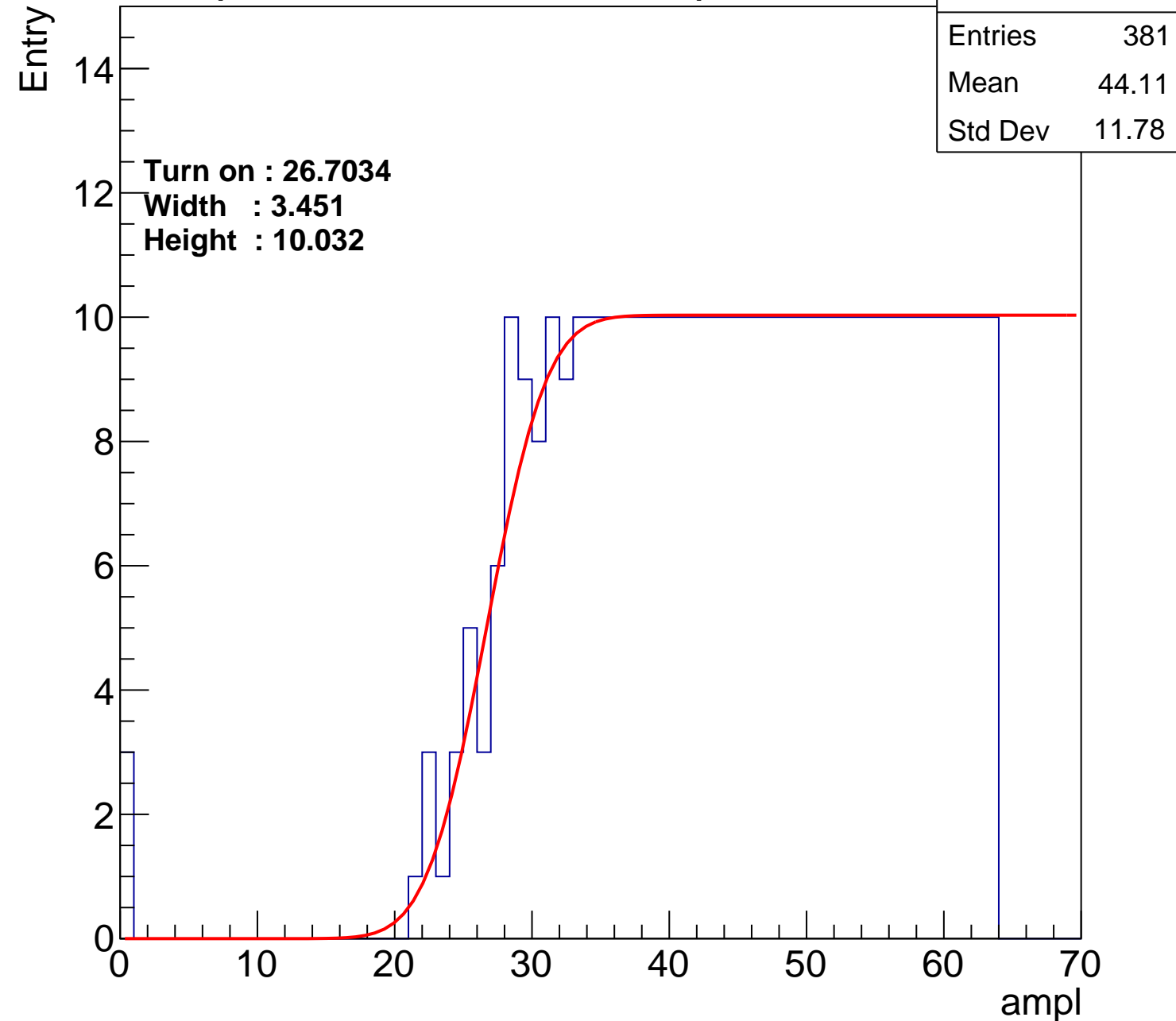
Width : 3.451

Height : 10.032

Entry

14
12
10
8
6
4
2
0

ampl



calib_packv5_042523_0143.root, FC#9, port A1

calib_packv5_042523_0143.root, FC#9, port A1

Turn on : 27.7427
Width : 3.496
Height : 10.035



B0L001S, U17-ch61

calib_packv5_042523_0143.root, FC#9, port A1

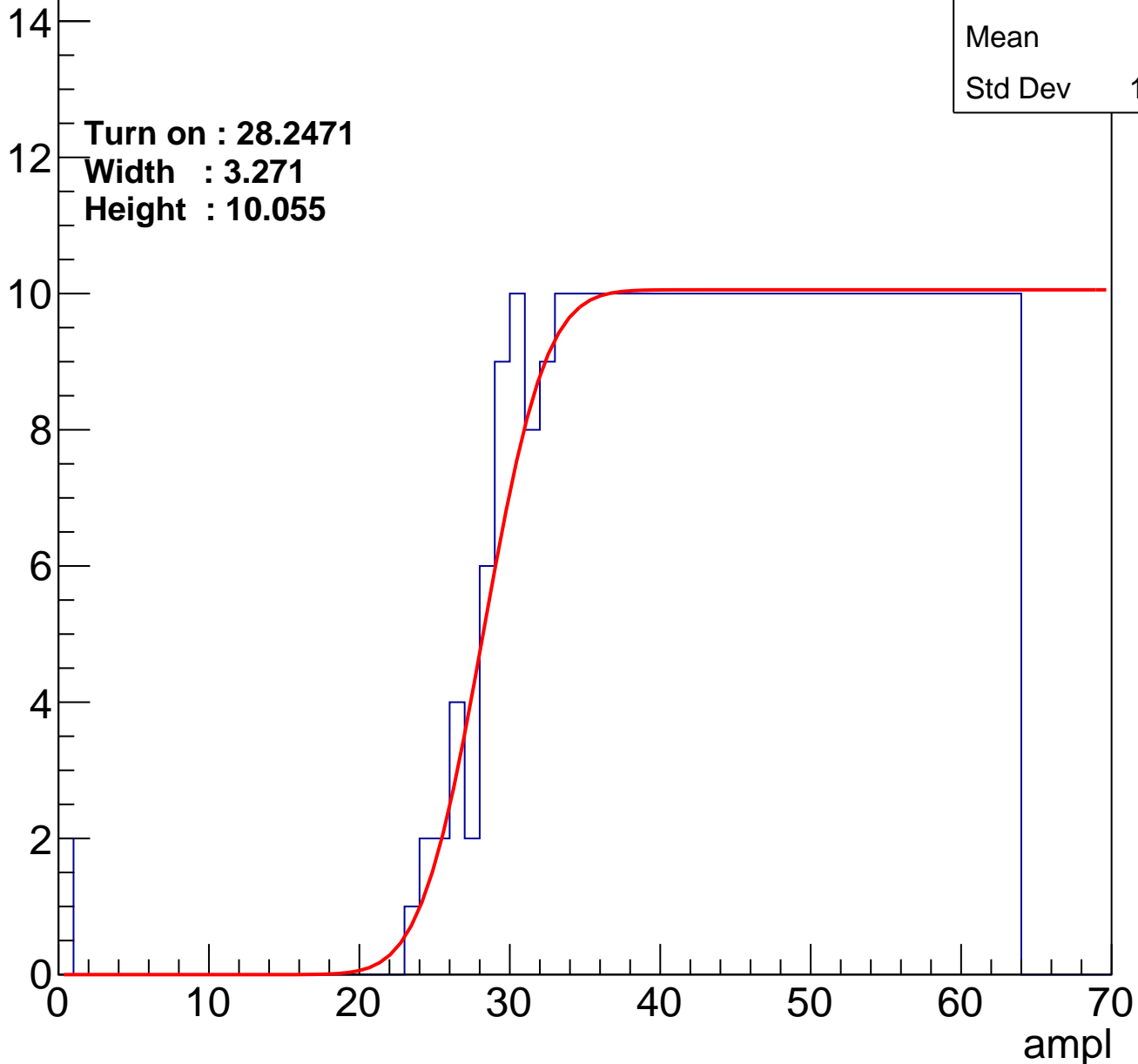
Entries	365
Mean	45
Std Dev	11.14

Turn on : 28.2471

Width : 3.271

Height : 10.055

Entry



B0L001S, U17-ch62

calib_packv5_042523_0143.root, FC#9, port A1

Entries	370
Mean	44.65
Std Dev	11.51

Turn on : 27.1112

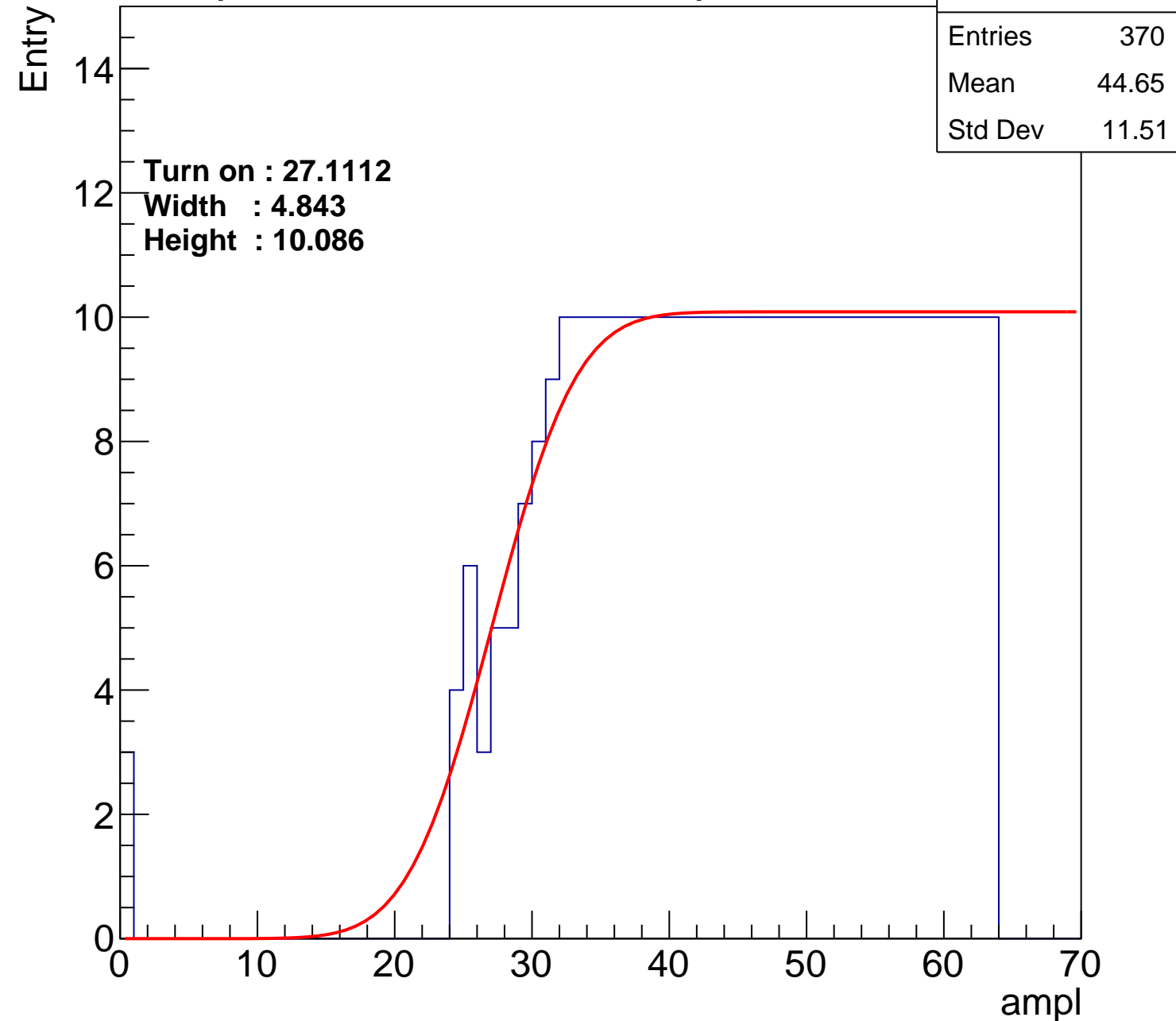
Width : 4.843

Height : 10.086

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch63

calib_packv5_042523_0143.root, FC#9, port A1

Entries	375
Mean	44.35
Std Dev	11.78

Turn on : 27.1497

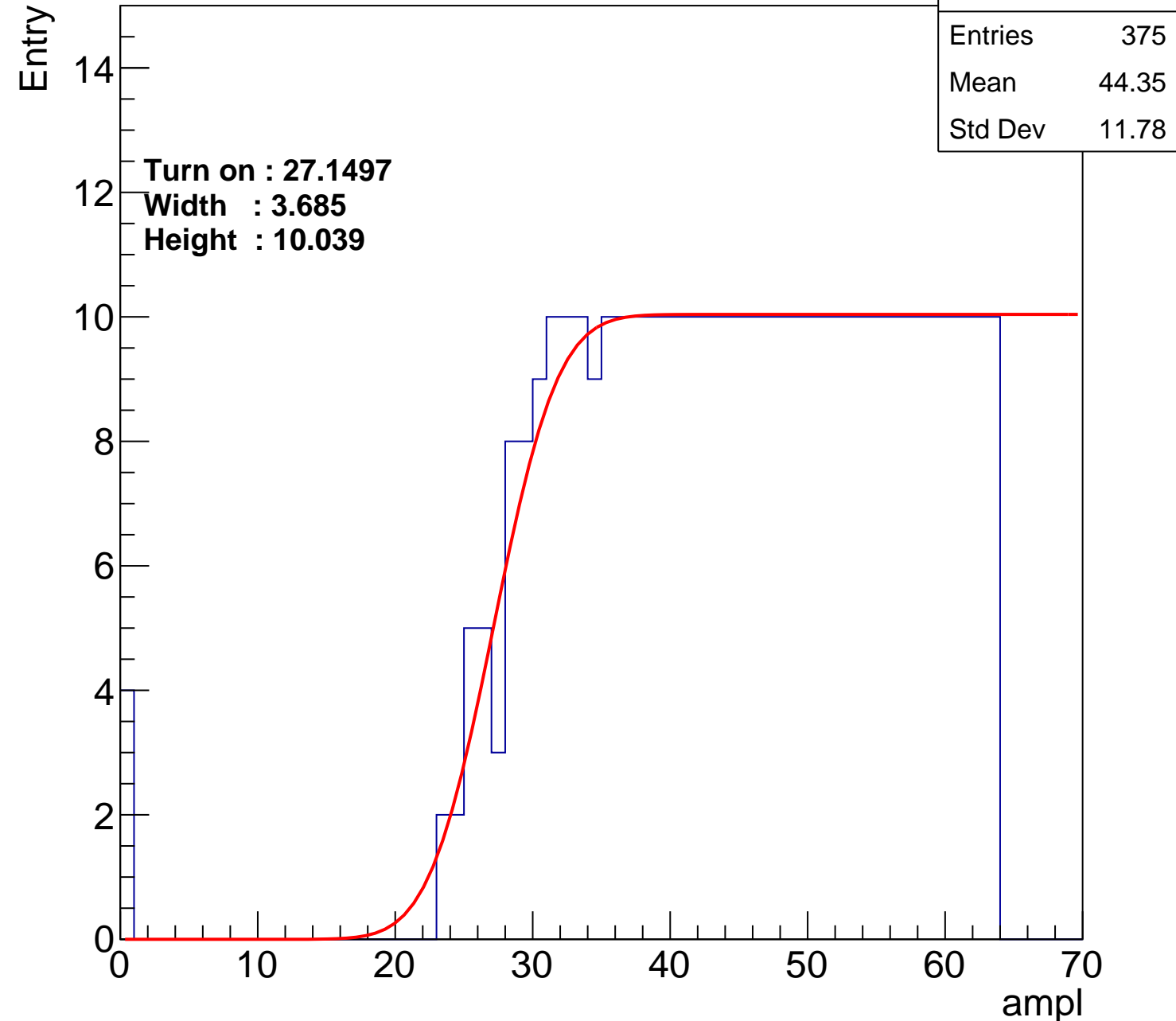
Width : 3.685

Height : 10.039

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch64

calib_packv5_042523_0143.root, FC#9, port A1

Entries	378
Mean	44.17
Std Dev	11.91

Turn on : 27.2369

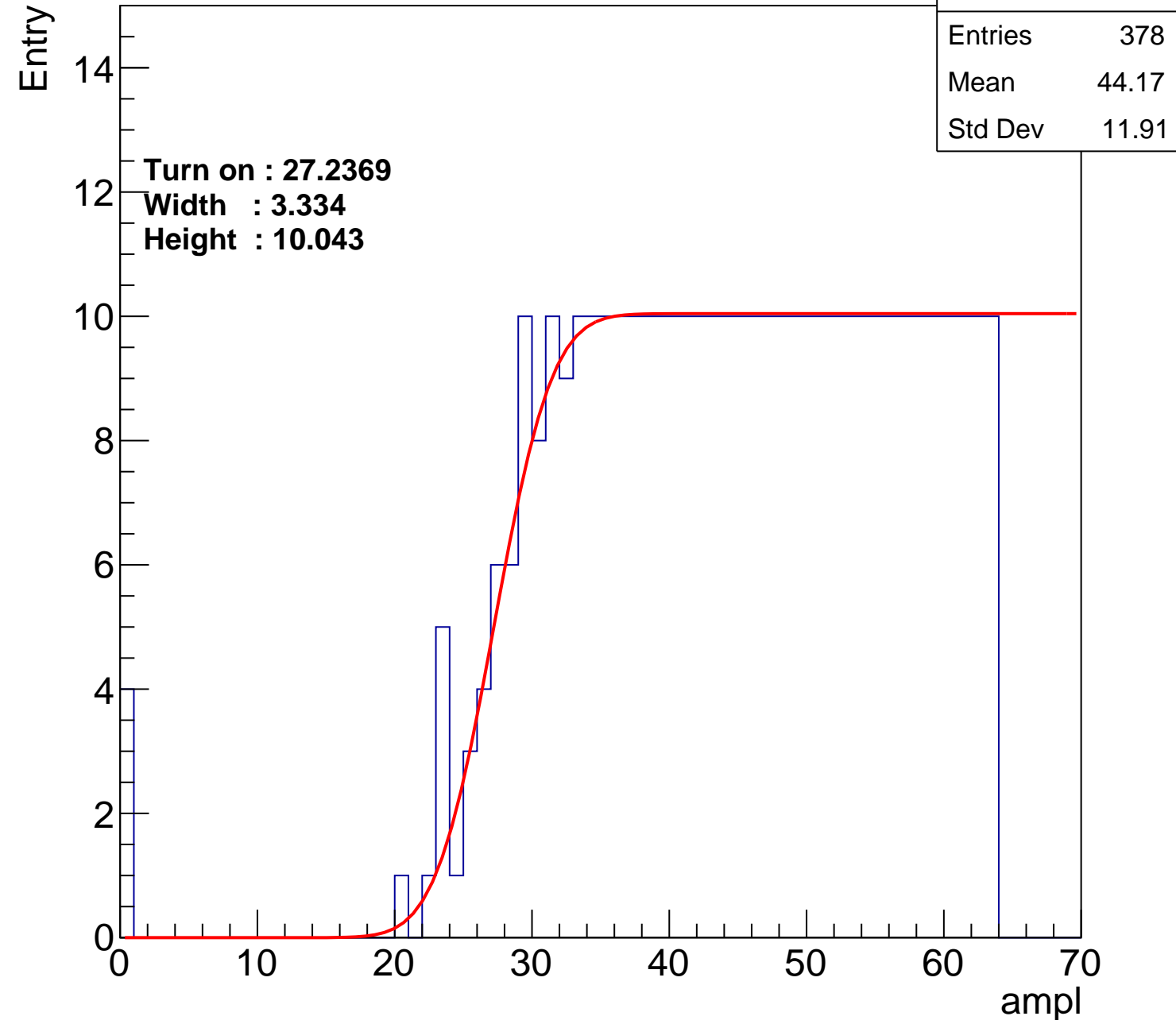
Width : 3.334

Height : 10.043

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch65

calib_packv5_042523_0143.root, FC#9, port A1

Entries	364
Mean	44.89
Std Dev	11.54

Turn on : 28.6741

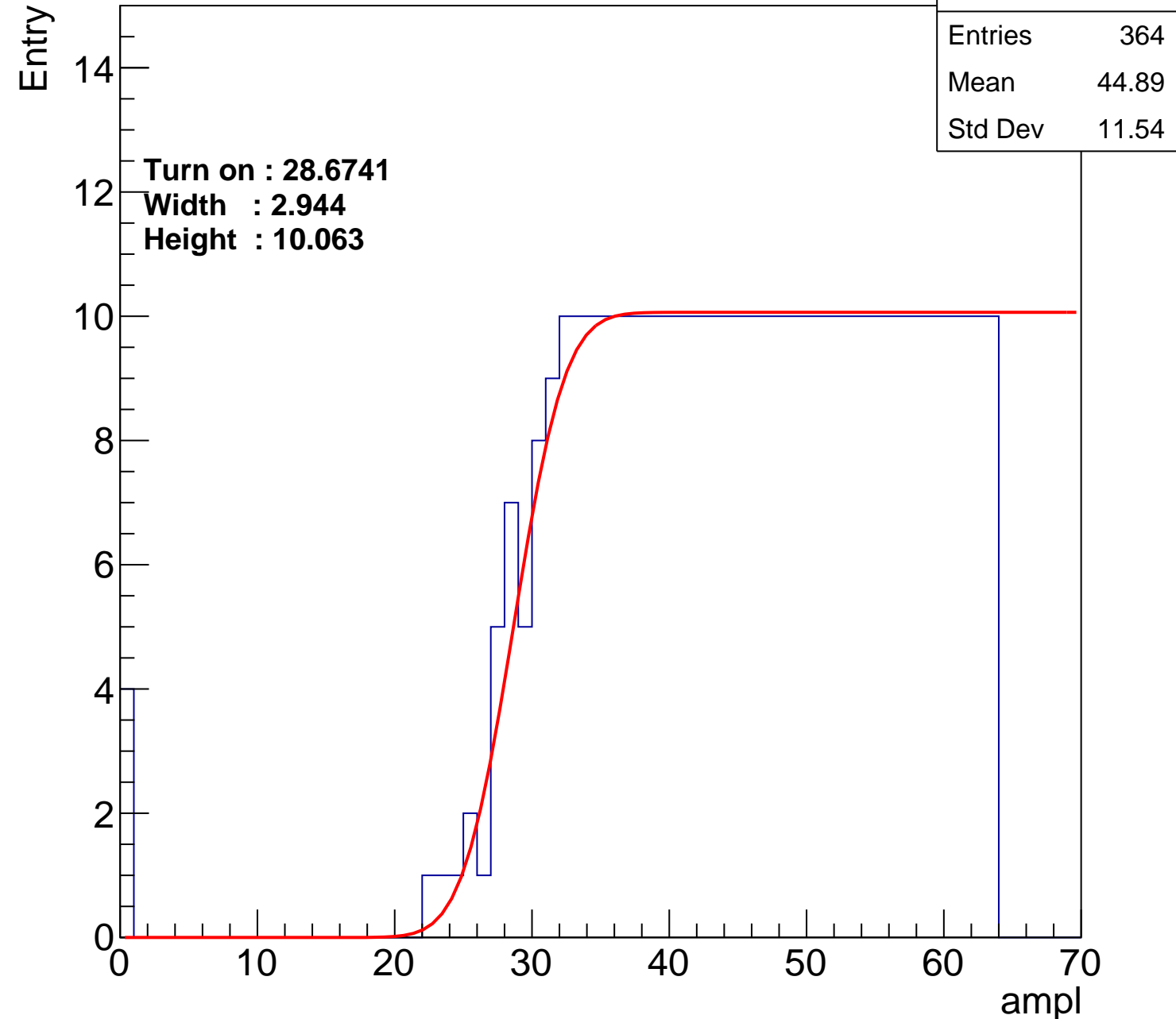
Width : 2.944

Height : 10.063

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch66

calib_packv5_042523_0143.root, FC#9, port A1

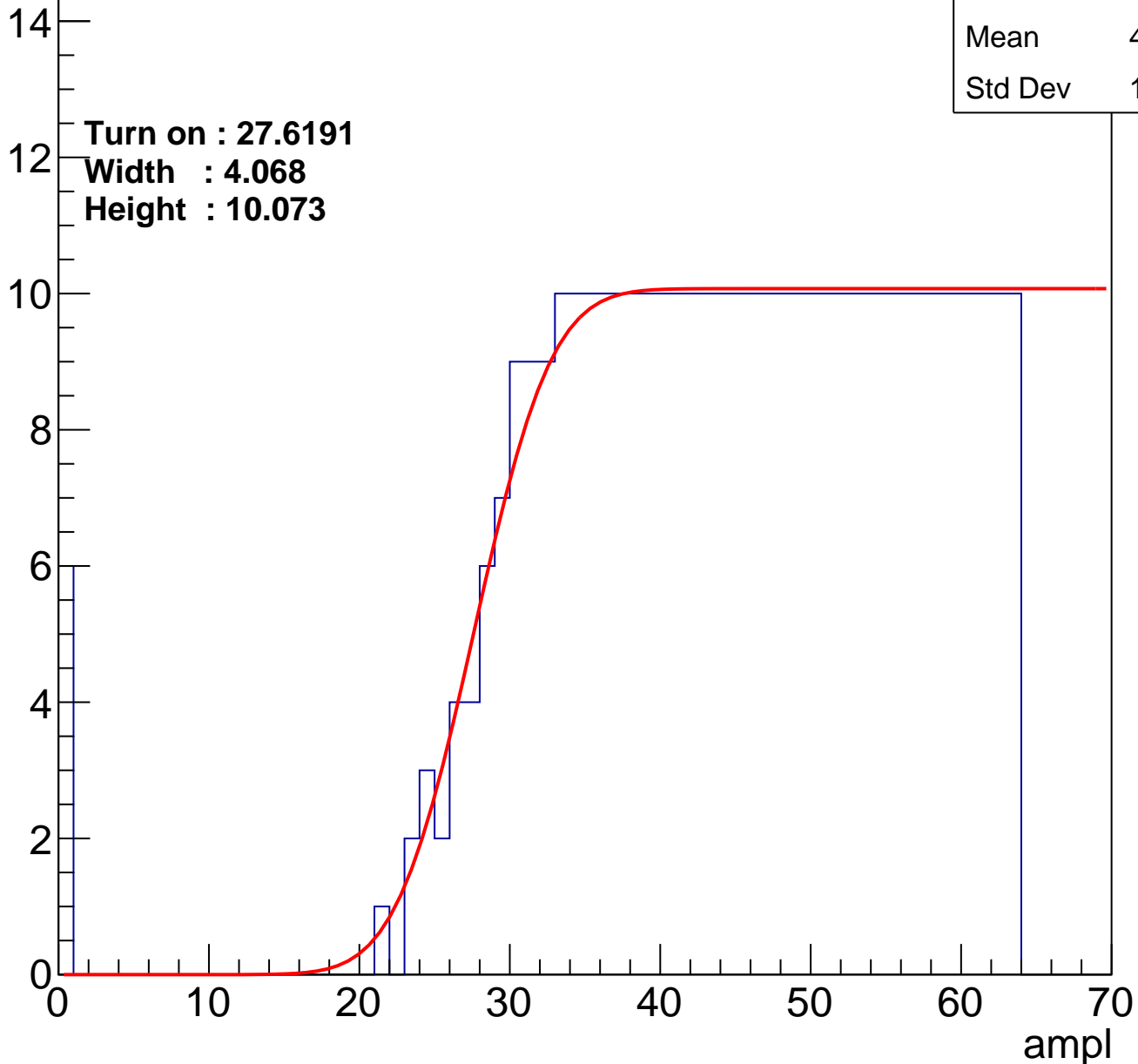
Entries	372
Mean	44.33
Std Dev	12.14

Turn on : 27.6191

Width : 4.068

Height : 10.073

Entry



B0L001S, U17-ch67

calib_packv5_042523_0143.root, FC#9, port A1

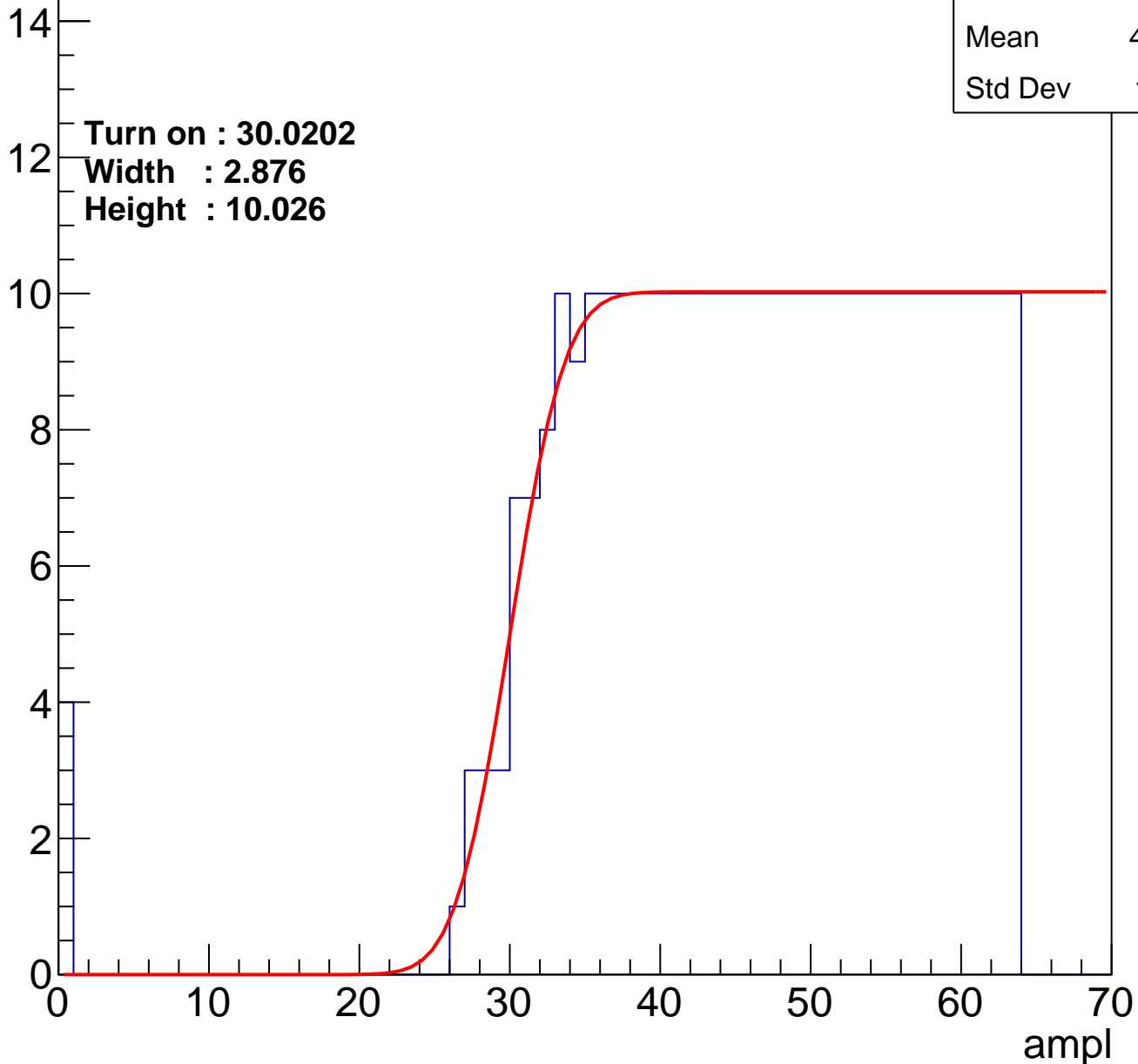
Entries	345
Mean	45.82
Std Dev	11.11

Turn on : 30.0202

Width : 2.876

Height : 10.026

Entry



B0L001S, U17-ch68

calib_packv5_042523_0143.root, FC#9, port A1

Entries	368
Mean	44.76
Std Dev	11.44

Turn on : 27.4850

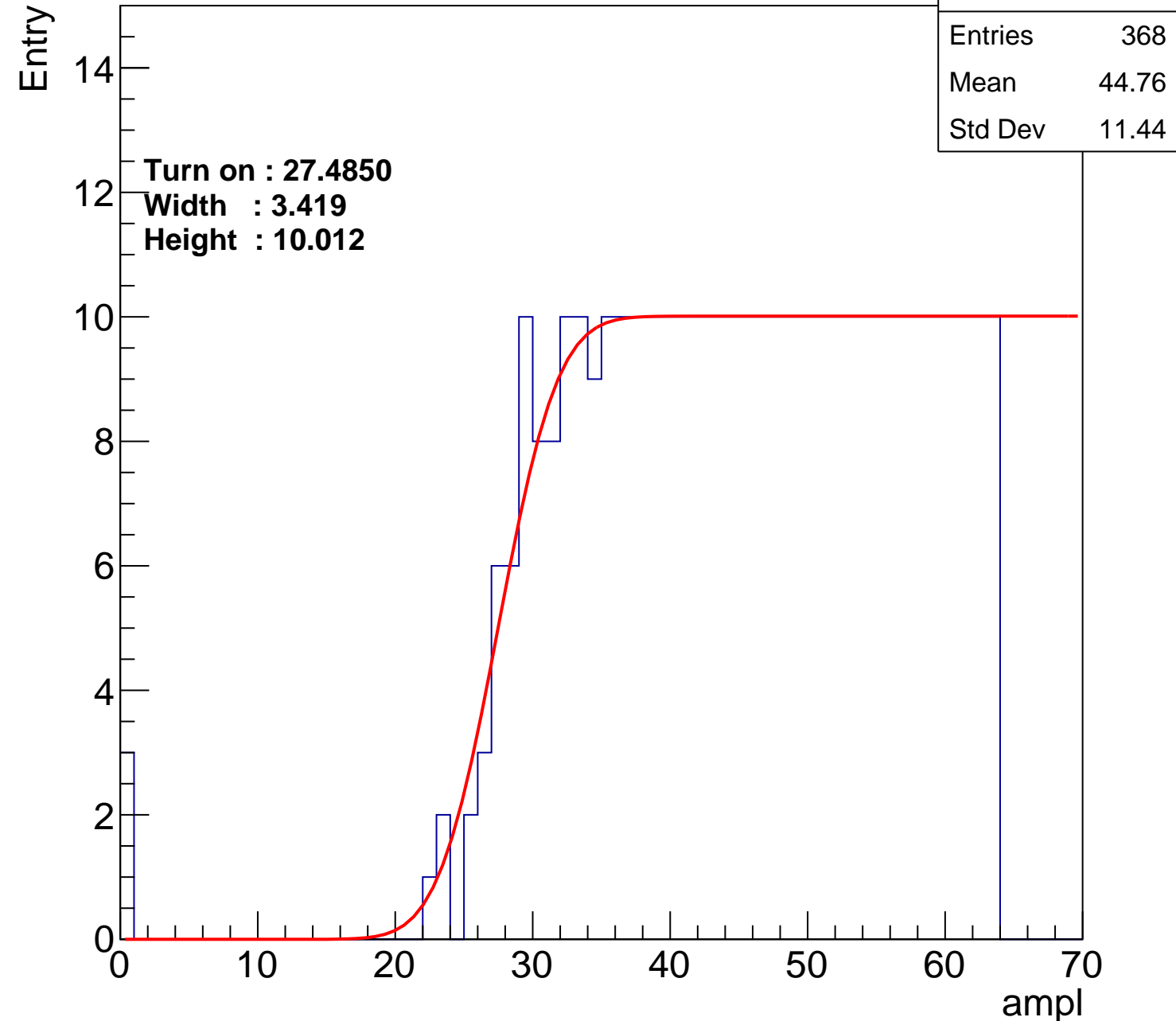
Width : 3.419

Height : 10.012

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch69

calib_packv5_042523_0143.root, FC#9, port A1

Entries	348
Mean	45.73
Std Dev	10.98

Turn on : 30.6373

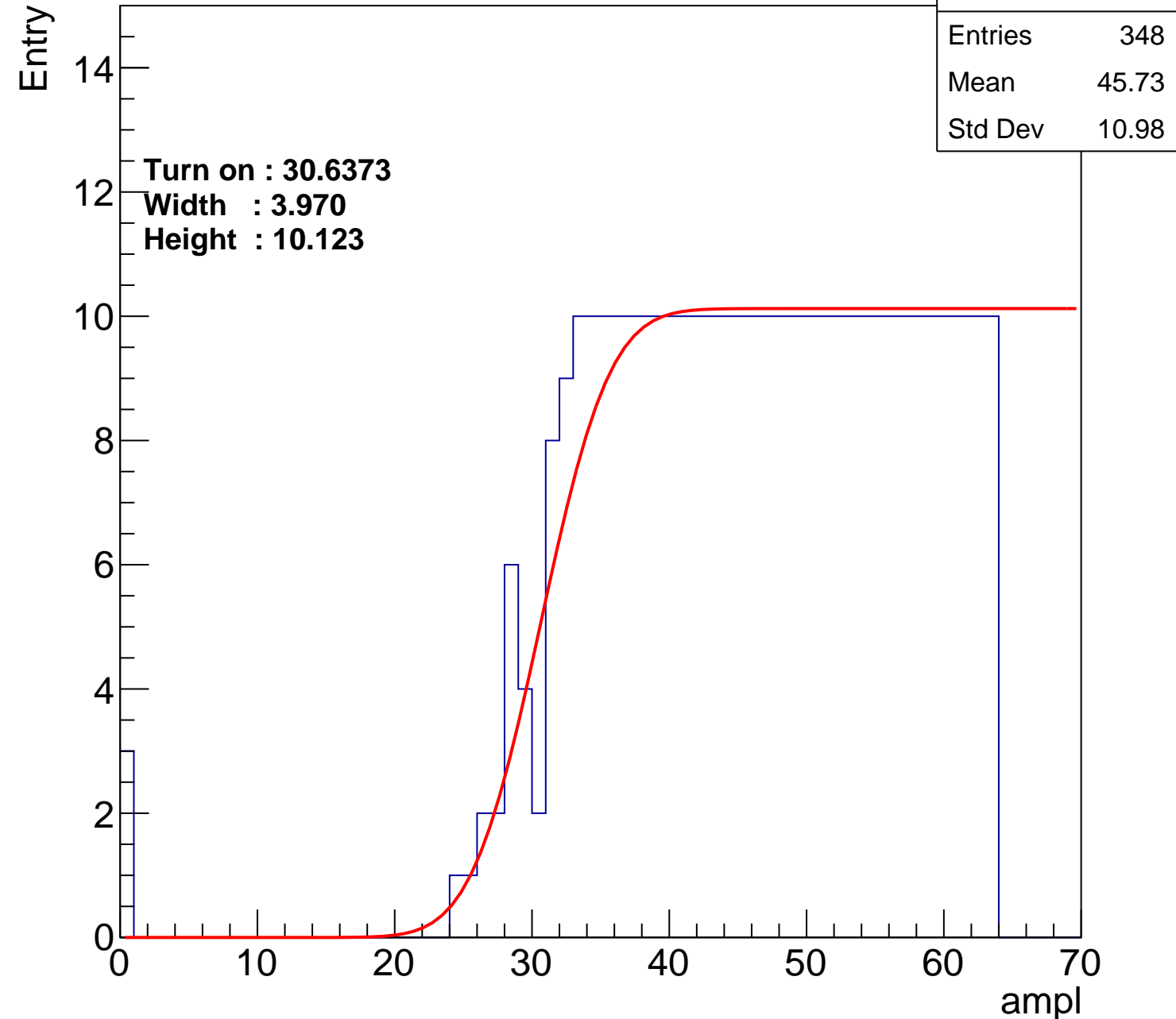
Width : 3.970

Height : 10.123

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch70

calib_packv5_042523_0143.root, FC#9, port A1

Entries	383
Mean	44.05
Std Dev	11.69

Turn on : 25.7656

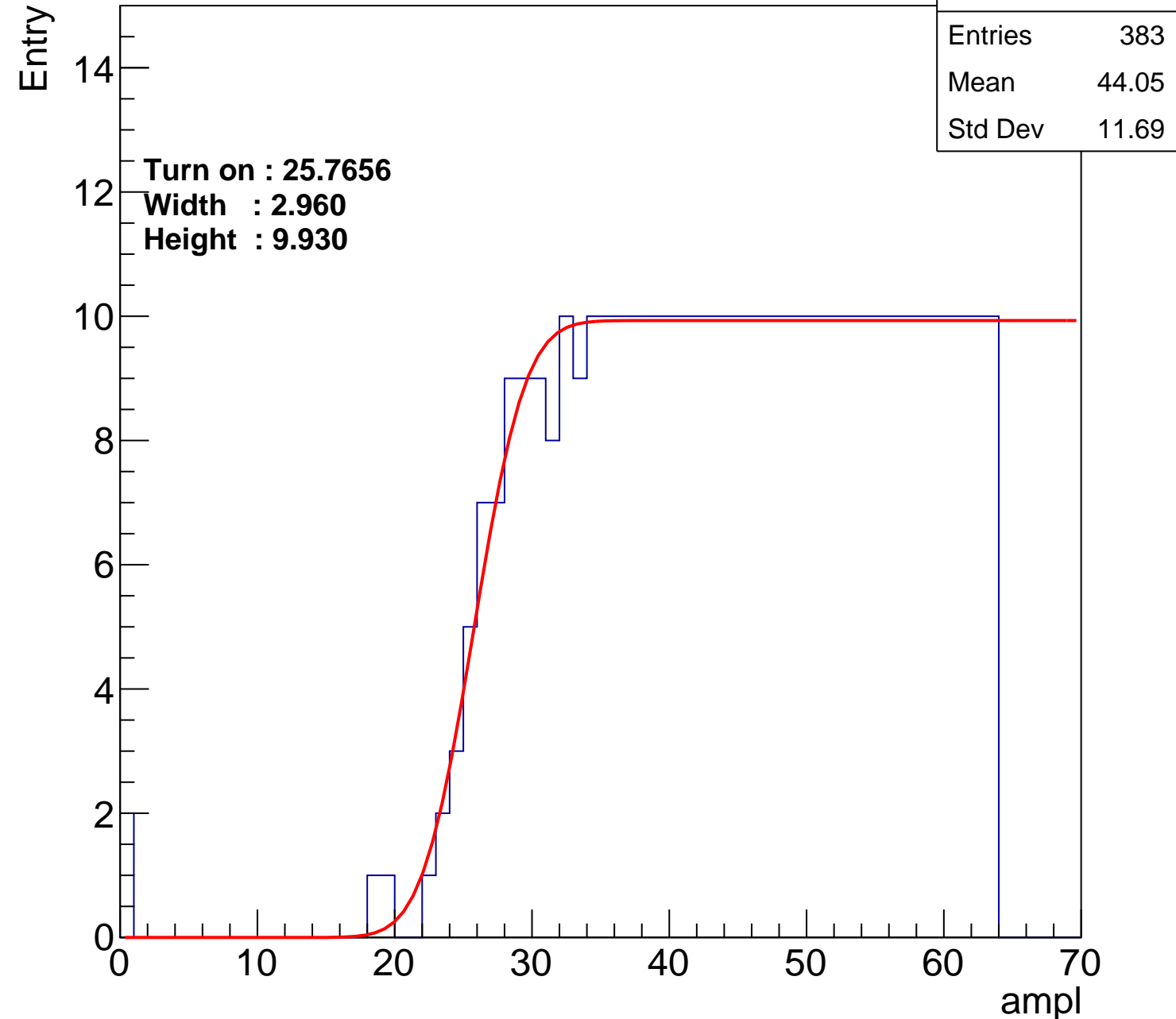
Width : 2.960

Height : 9.930

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch71

calib_packv5_042523_0143.root, FC#9, port A1

Entries	365
Mean	44.9
Std Dev	11.38

Turn on : 28.3046

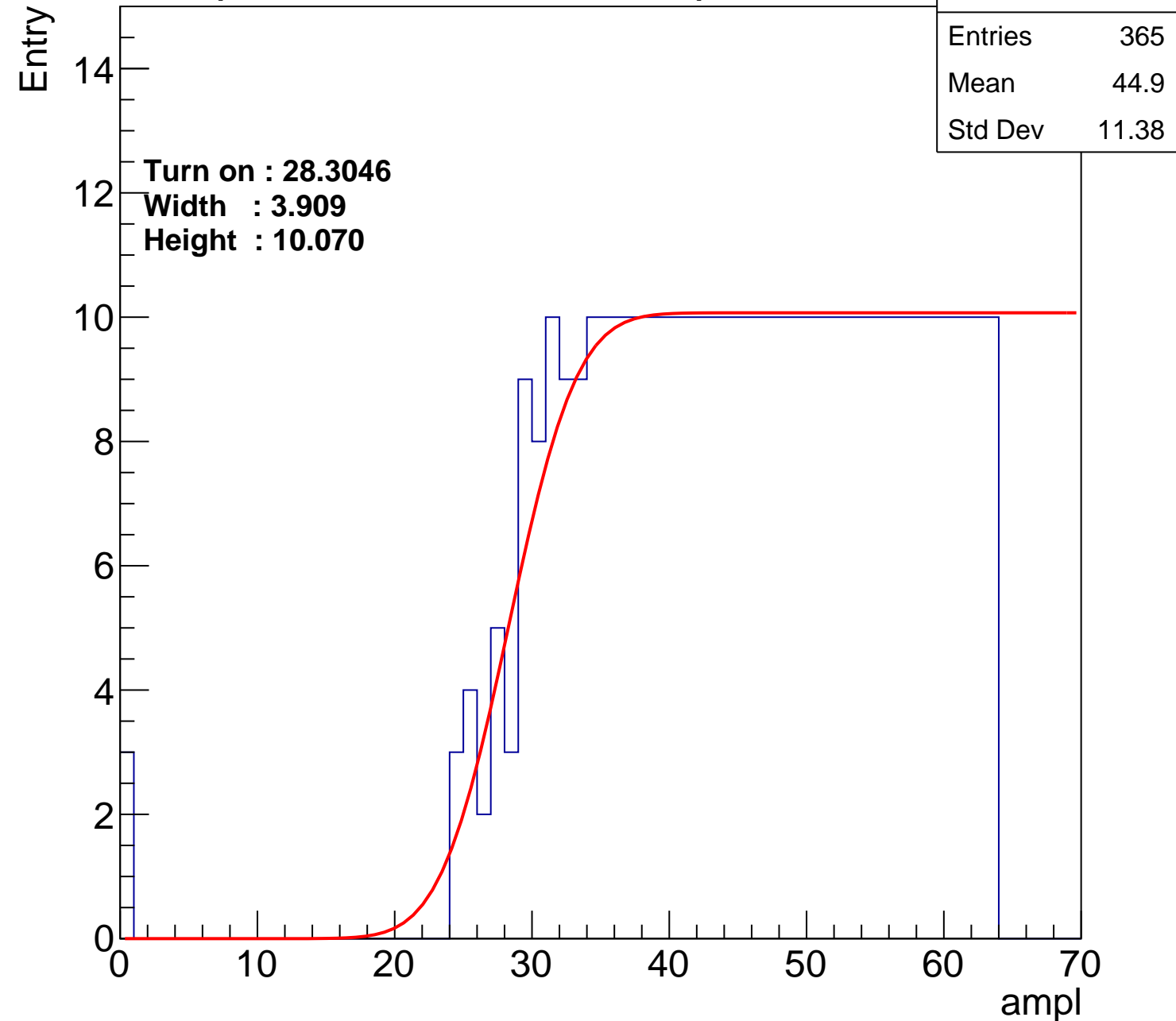
Width : 3.909

Height : 10.070

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch72

calib_packv5_042523_0143.root, FC#9, port A1

Entries	377
Mean	44.31
Std Dev	11.75

Turn on : 26.5526

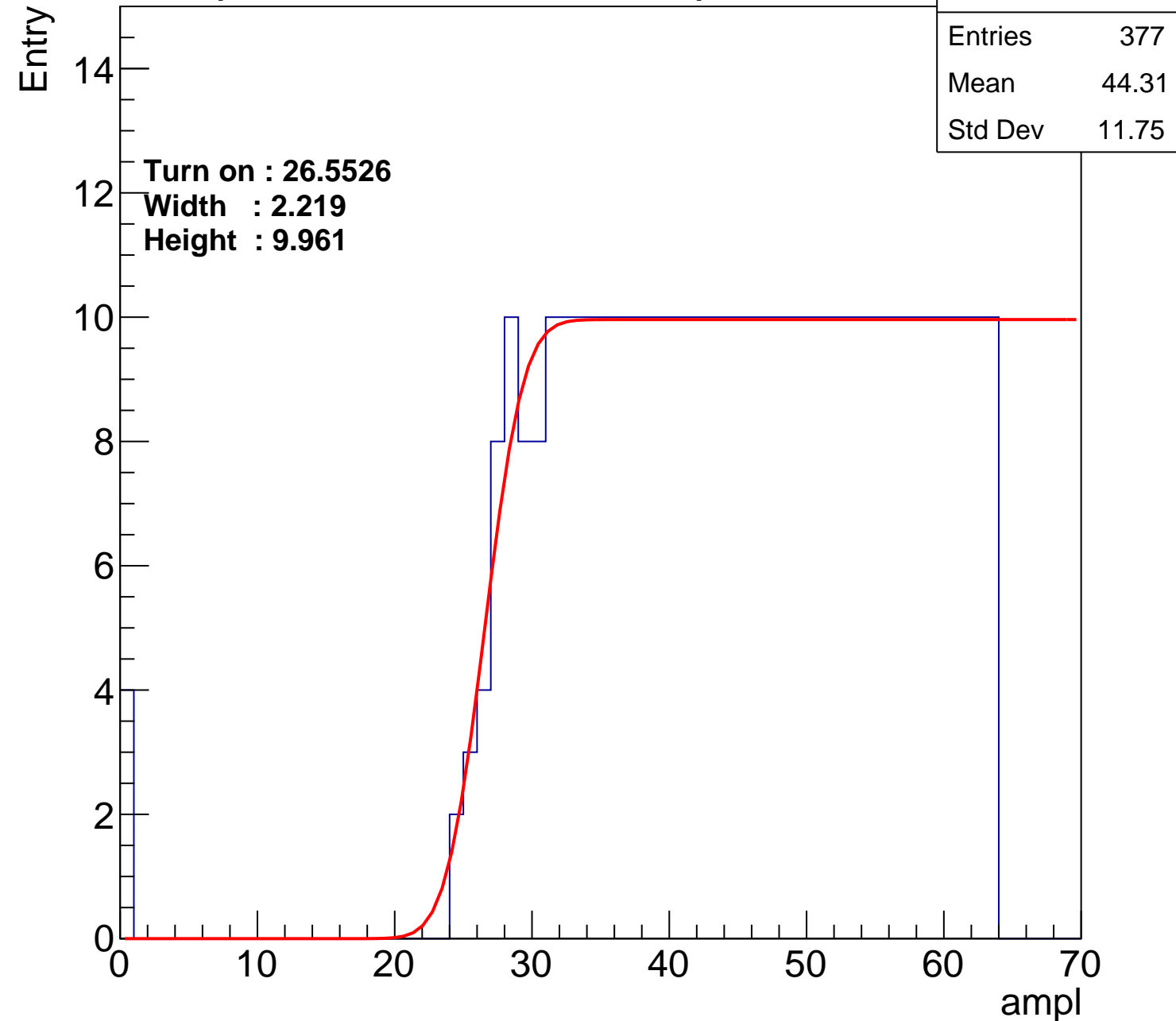
Width : 2.219

Height : 9.961

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch73

calib_packv5_042523_0143.root, FC#9, port A1

Entries	377
Mean	44.34
Std Dev	11.63

Turn on : 26.7210

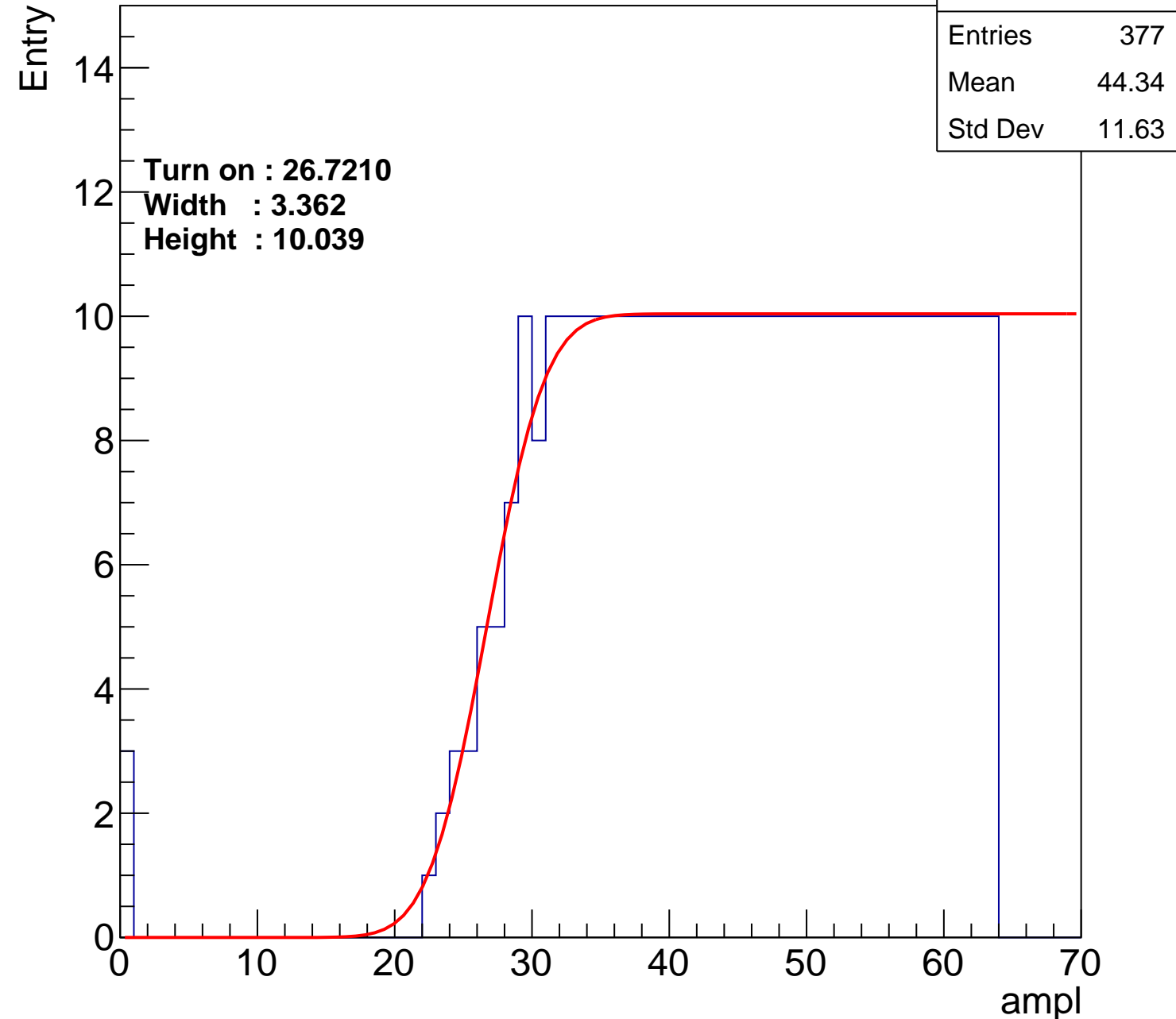
Width : 3.362

Height : 10.039

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch74

calib_packv5_042523_0143.root, FC#9, port A1

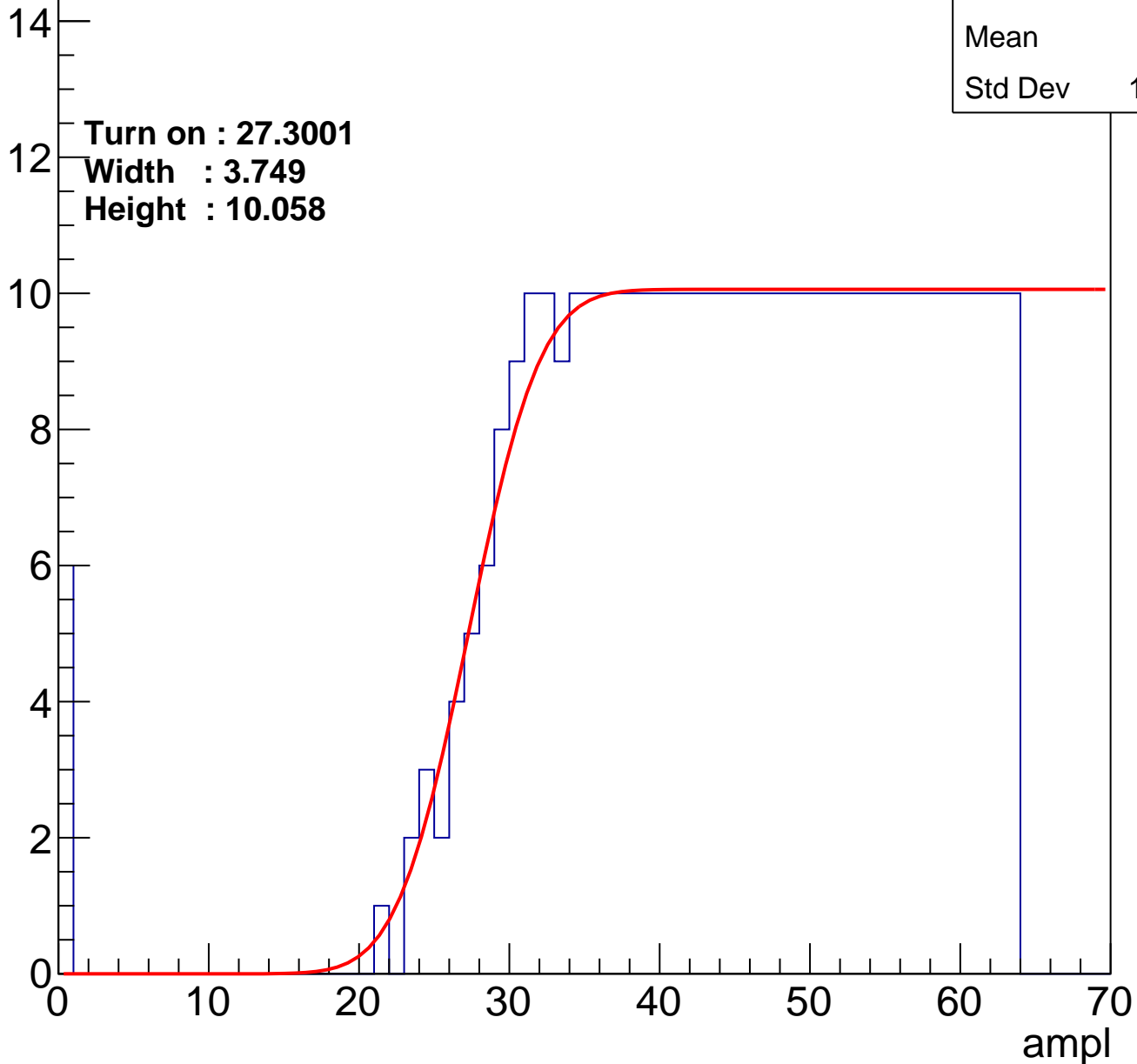
Entries	375
Mean	44.2
Std Dev	12.17

Turn on : 27.3001

Width : 3.749

Height : 10.058

Entry



B0L001S, U17-ch75

calib_packv5_042523_0143.root, FC#9, port A1

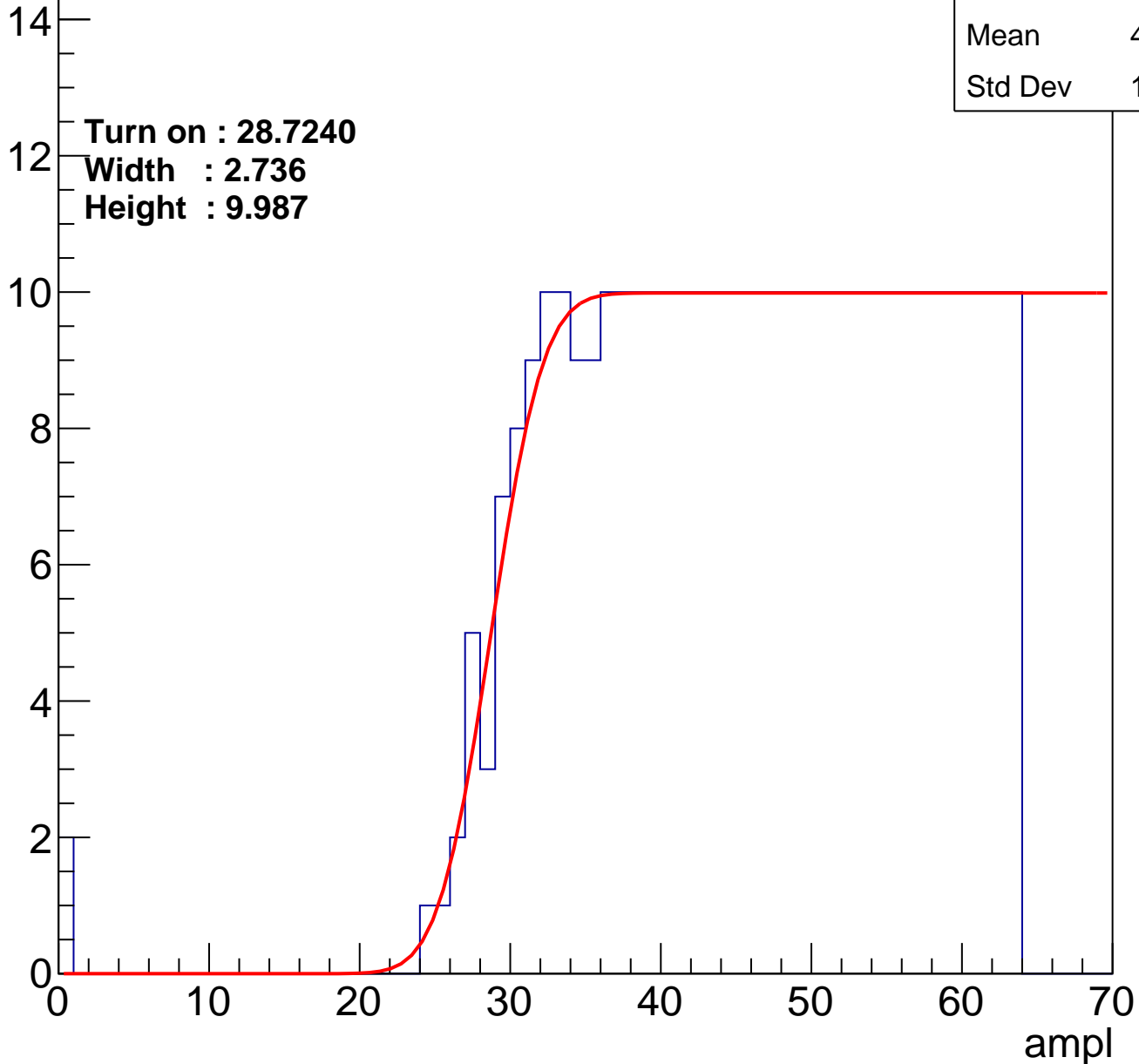
Entries	356
Mean	45.43
Std Dev	10.92

Turn on : 28.7240

Width : 2.736

Height : 9.987

Entry



B0L001S, U17-ch76

calib_packv5_042523_0143.root, FC#9, port A1

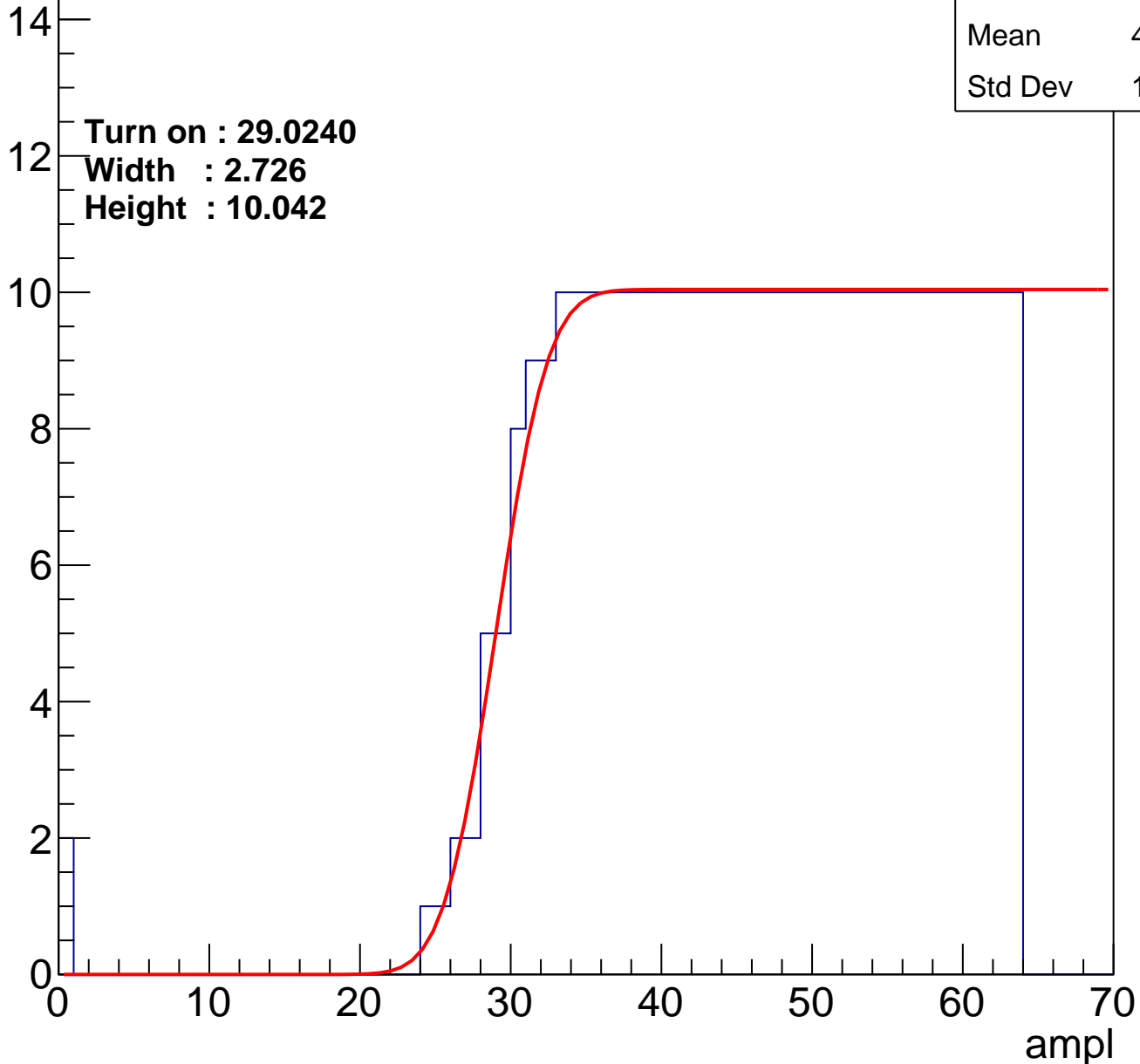
Entries	354
Mean	45.56
Std Dev	10.83

Turn on : 29.0240

Width : 2.726

Height : 10.042

Entry



B0L001S, U17-ch77

calib_packv5_042523_0143.root, FC#9, port A1

Entries	363
Mean	44.94
Std Dev	11.52

Turn on : 28.9316

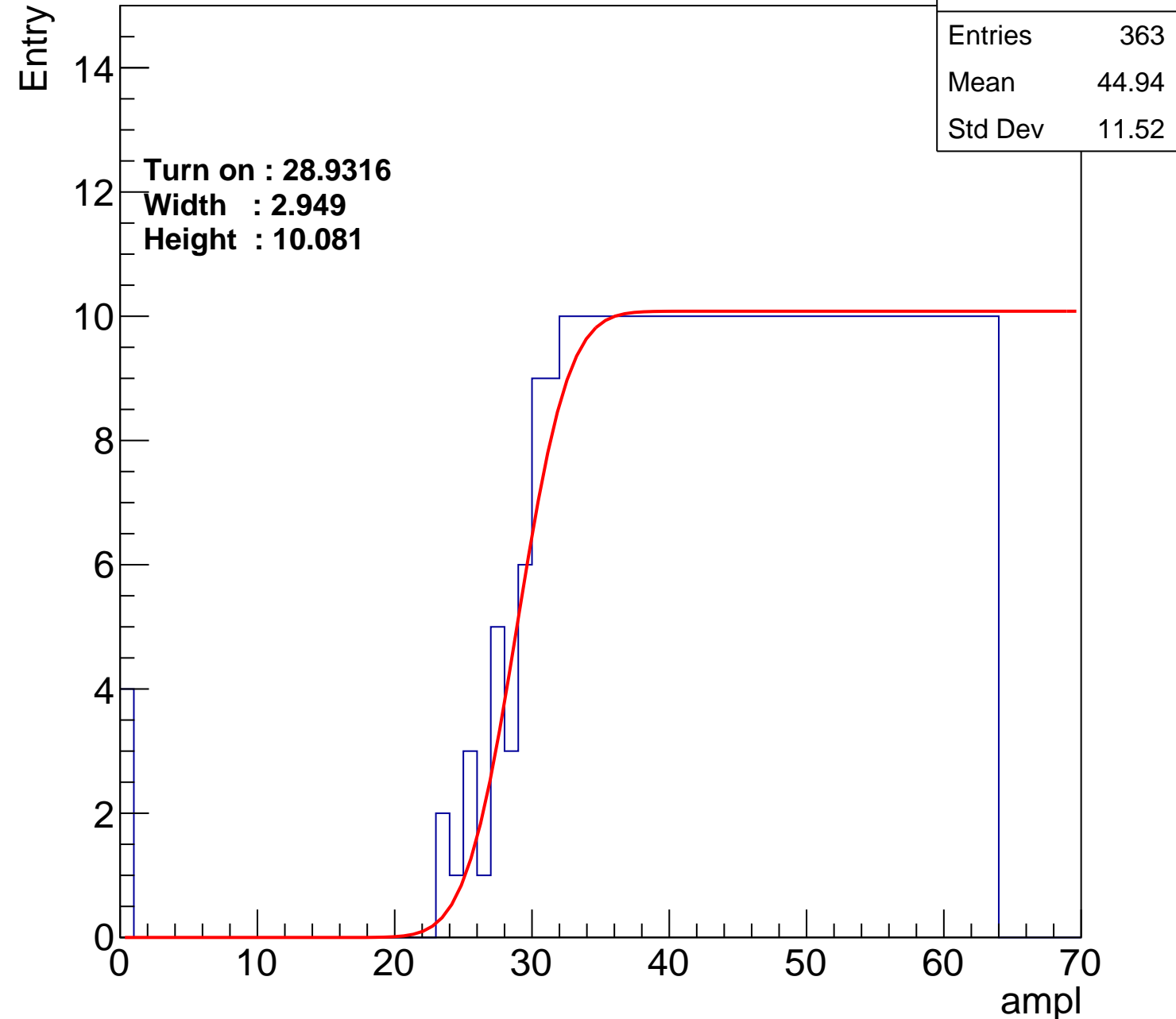
Width : 2.949

Height : 10.081

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch78

calib_packv5_042523_0143.root, FC#9, port A1

Entries	354
Mean	45.22
Std Dev	11.73

Turn on : 29.2129

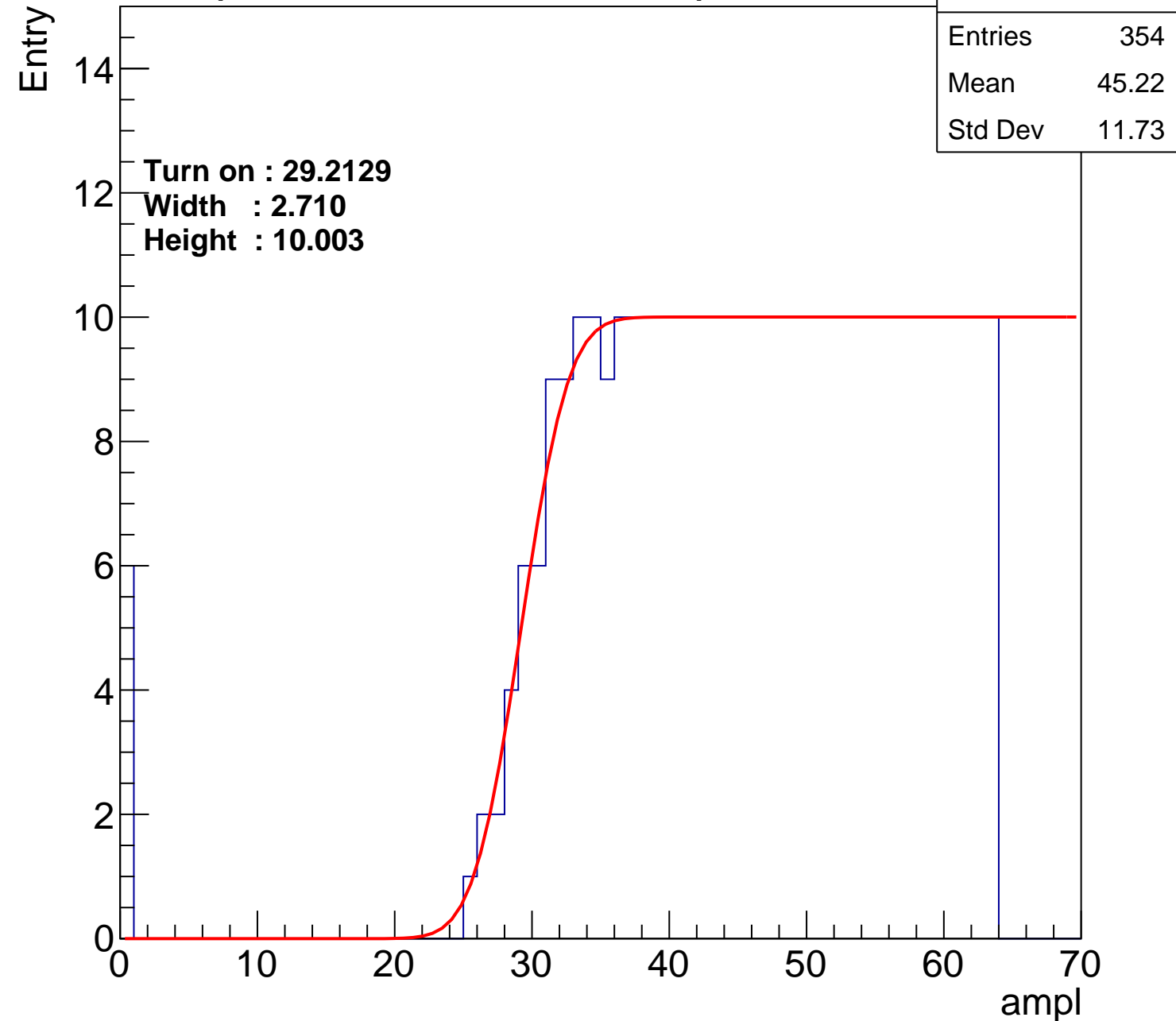
Width : 2.710

Height : 10.003

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch79

calib_packv5_042523_0143.root, FC#9, port A1

Entries	364
Mean	44.93
Std Dev	11.38

Turn on : 27.8741

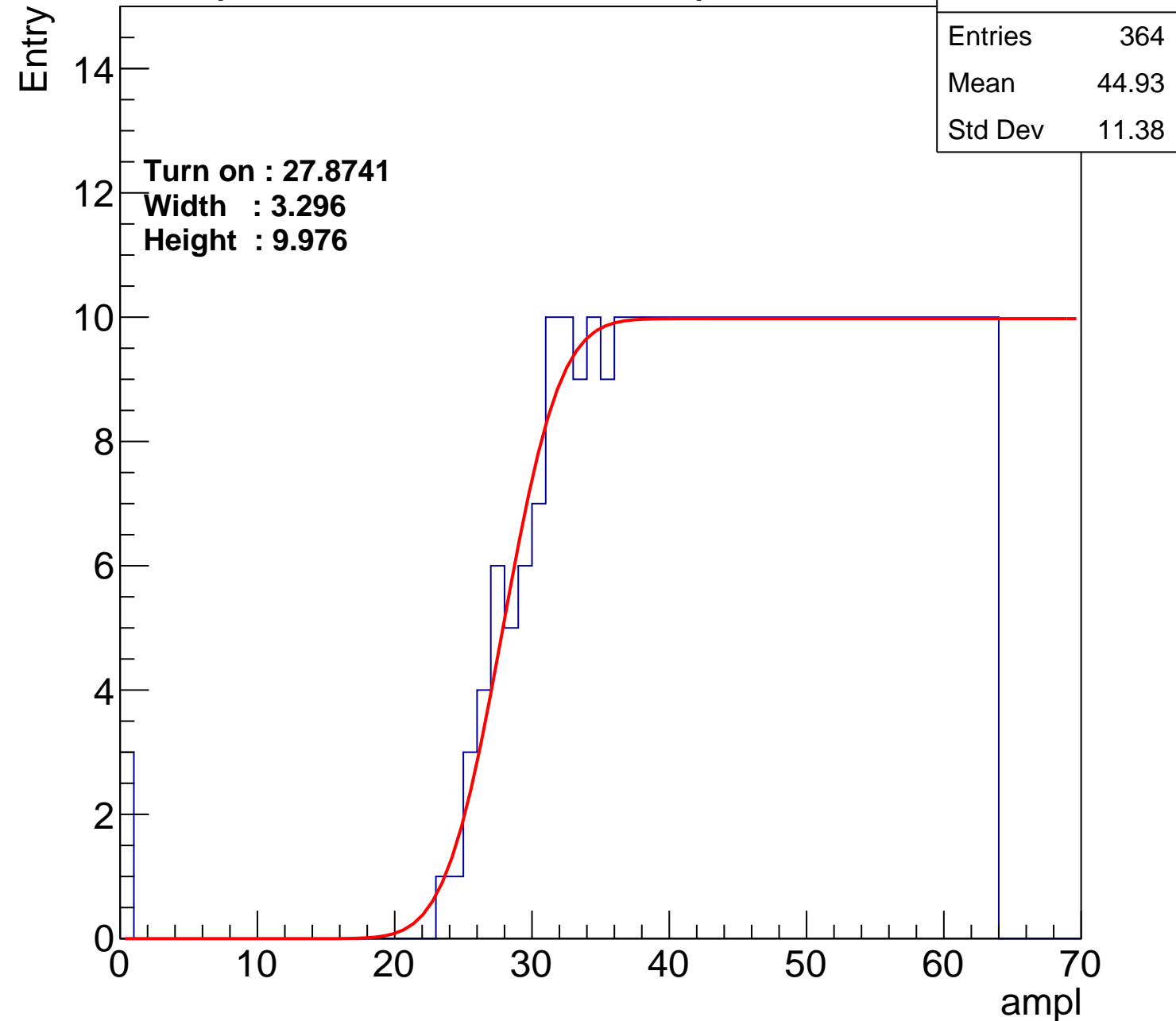
Width : 3.296

Height : 9.976

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch80

calib_packv5_042523_0143.root, FC#9, port A1

Entries	363
Mean	44.88
Std Dev	11.7

Turn on : 28.8088

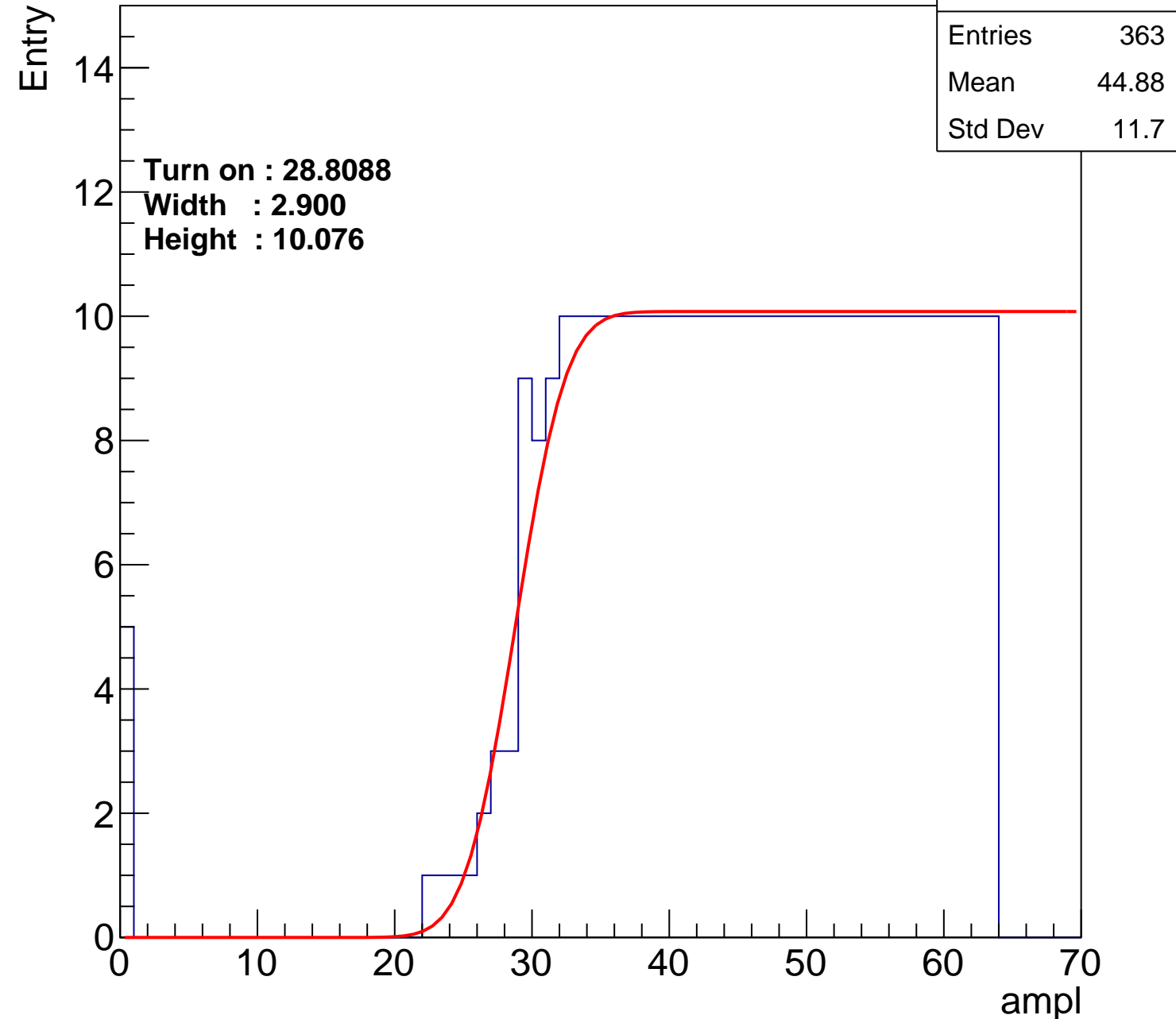
Width : 2.900

Height : 10.076

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch81

calib_packv5_042523_0143.root, FC#9, port A1

Entries	373
Mean	44.27
Std Dev	12.24

Turn on : 27.3839

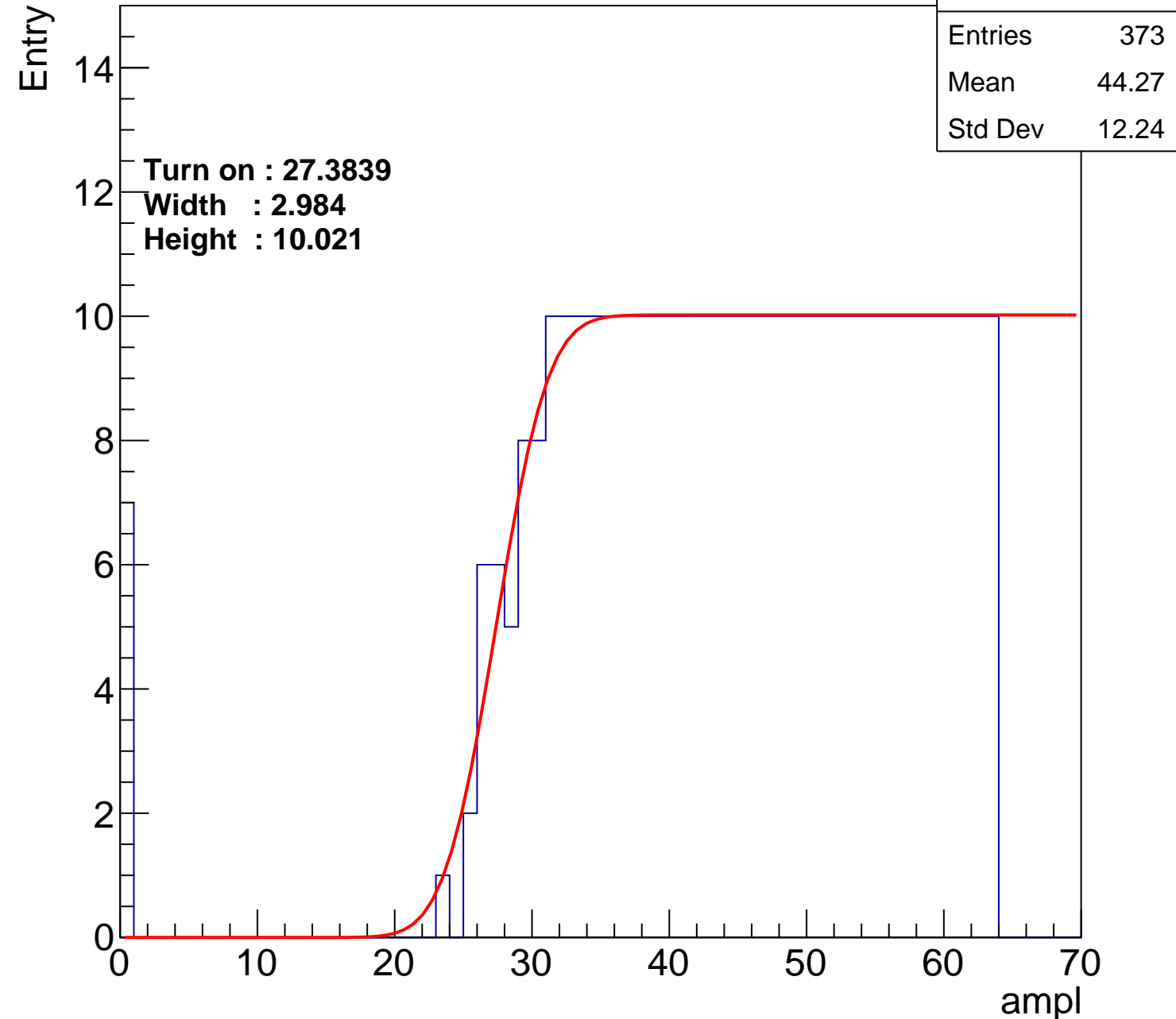
Width : 2.984

Height : 10.021

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch82

calib_packv5_042523_0143.root, FC#9, port A1

Entries	368
Mean	44.89
Std Dev	11.15

Turn on : 27.4078

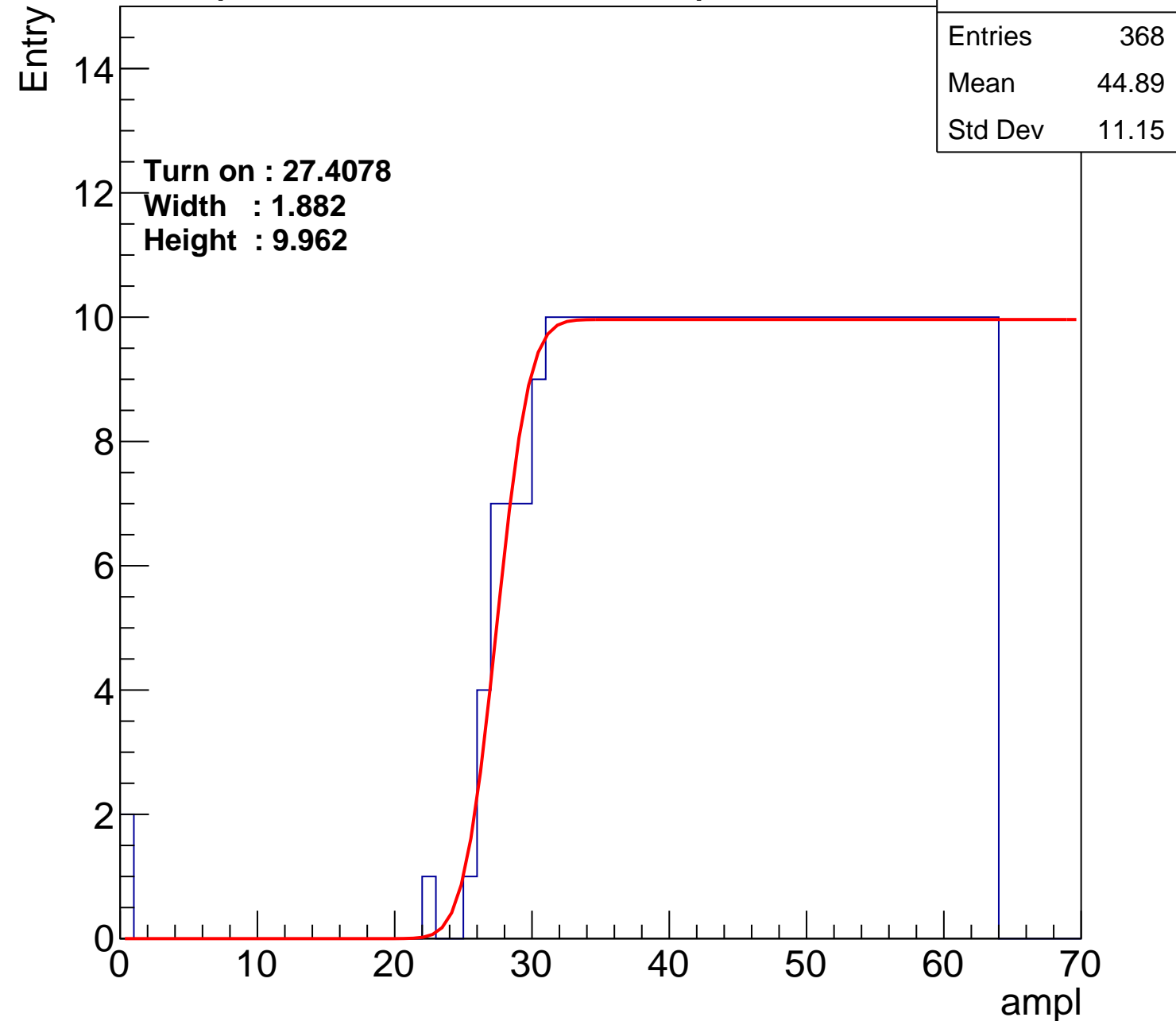
Width : 1.882

Height : 9.962

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch83

calib_packv5_042523_0143.root, FC#9, port A1

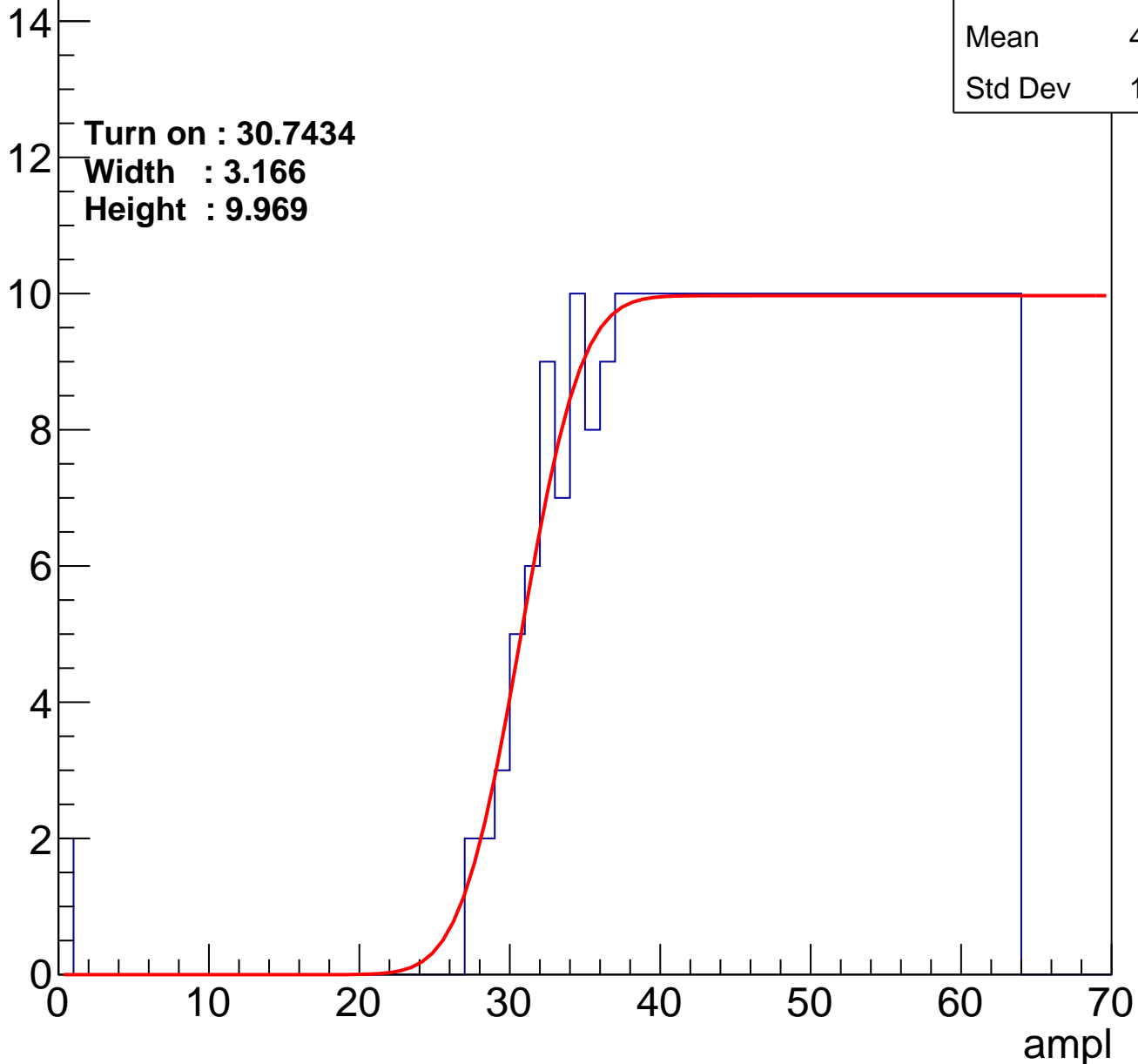
Entries	333
Mean	46.53
Std Dev	10.39

Turn on : 30.7434

Width : 3.166

Height : 9.969

Entry



B0L001S, U17-ch84

calib_packv5_042523_0143.root, FC#9, port A1

Entries	352
Mean	45.65
Std Dev	10.8

Turn on : 28.9471

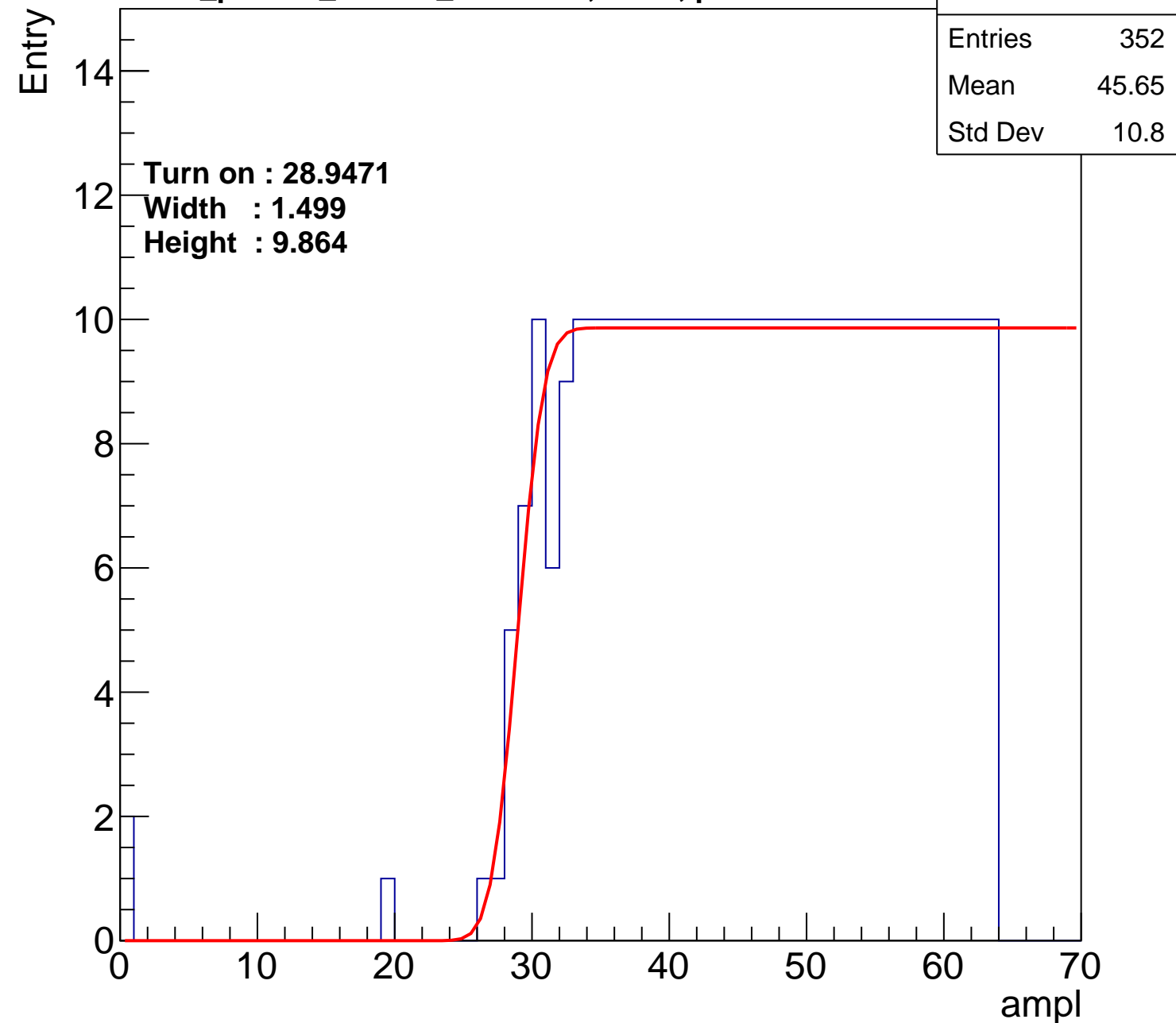
Width : 1.499

Height : 9.864

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch85

calib_packv5_042523_0143.root, FC#9, port A1

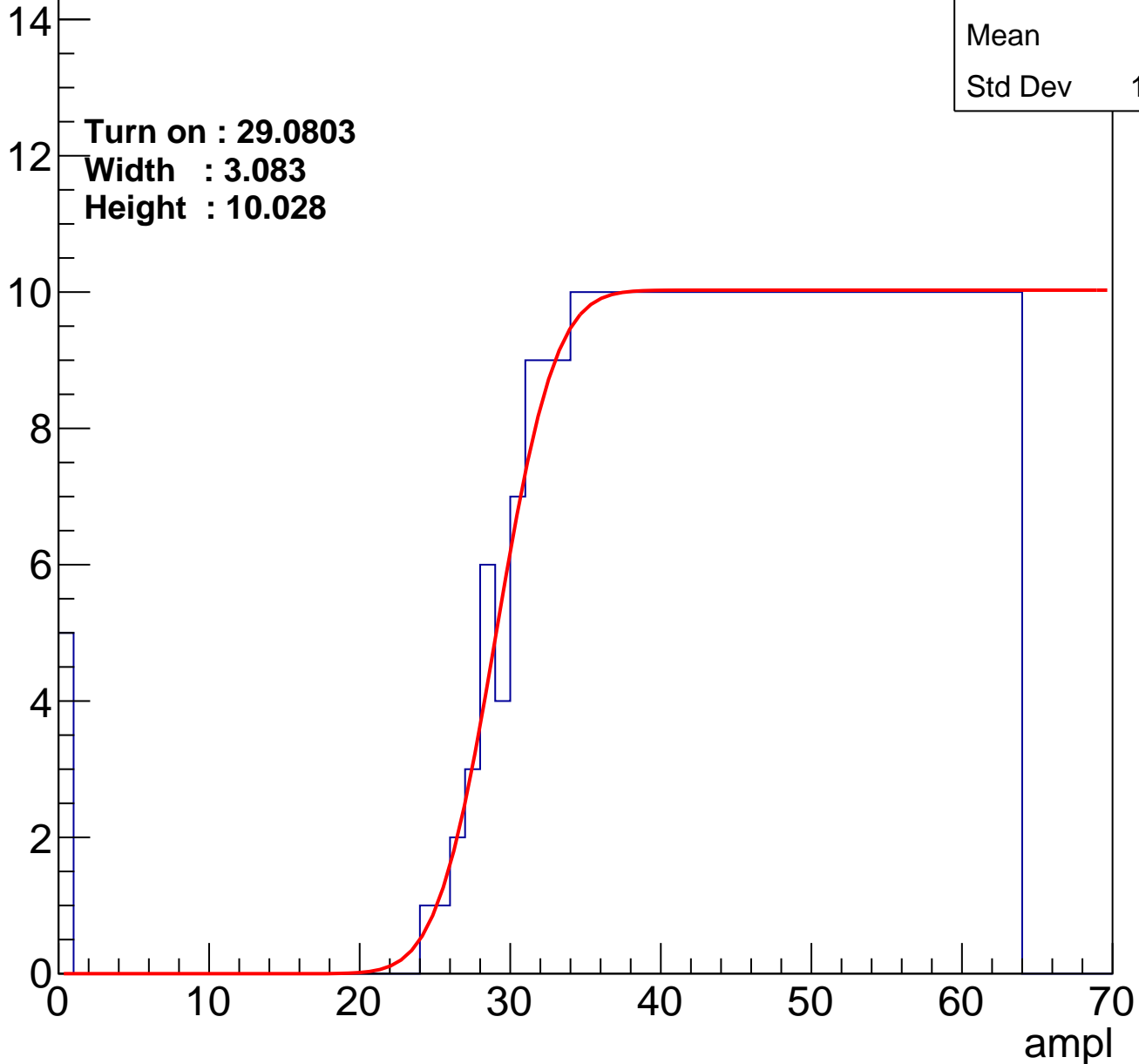
Entries	356
Mean	45.2
Std Dev	11.58

Turn on : 29.0803

Width : 3.083

Height : 10.028

Entry



B0L001S, U17-ch86

calib_packv5_042523_0143.root, FC#9, port A1

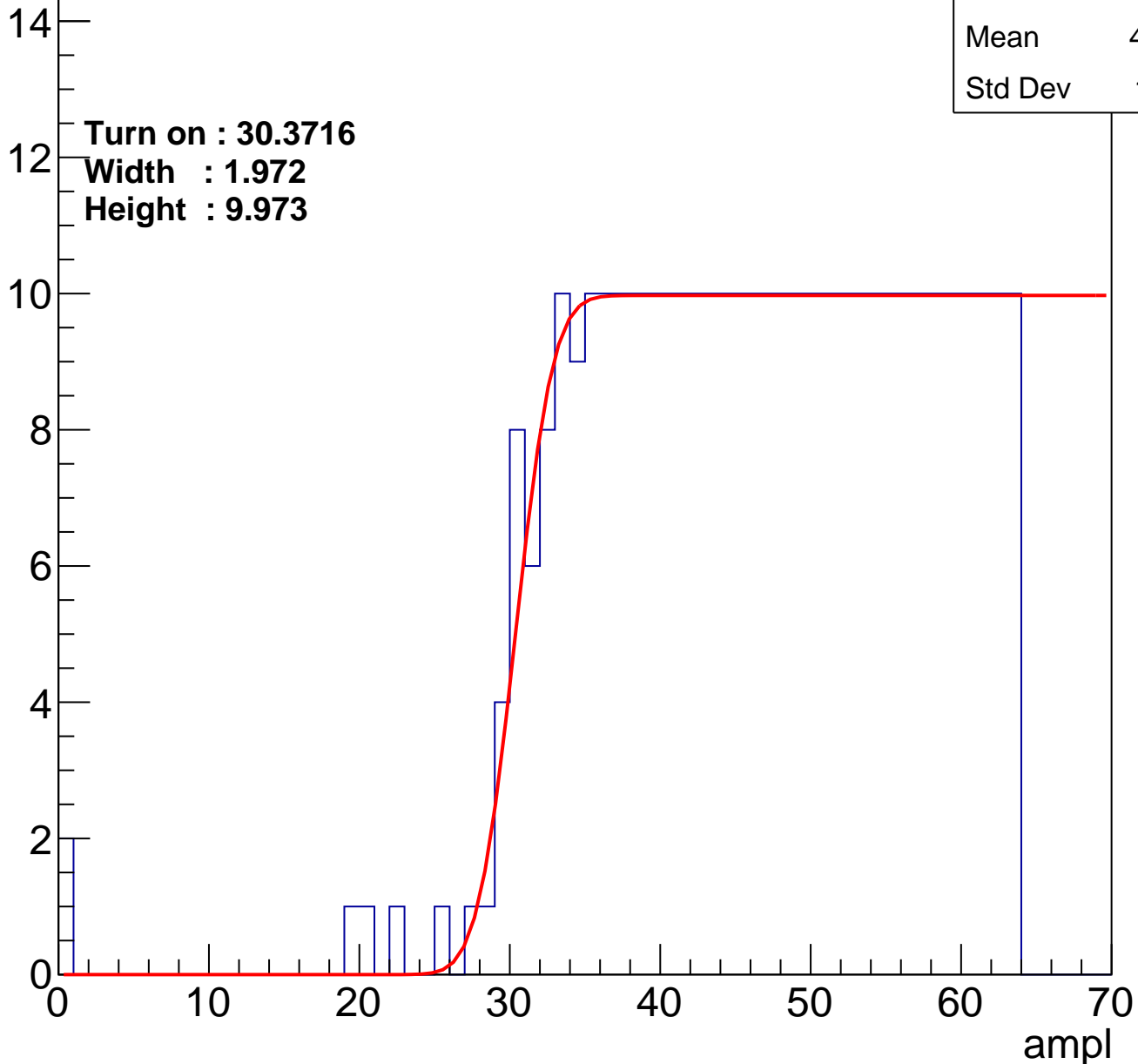
Entries	343
Mean	46.02
Std Dev	10.71

Turn on : 30.3716

Width : 1.972

Height : 9.973

Entry



B0L001S, U17-ch87

calib_packv5_042523_0143.root, FC#9, port A1

Entries	375
Mean	44.53
Std Dev	11.36

Turn on : 26.8629

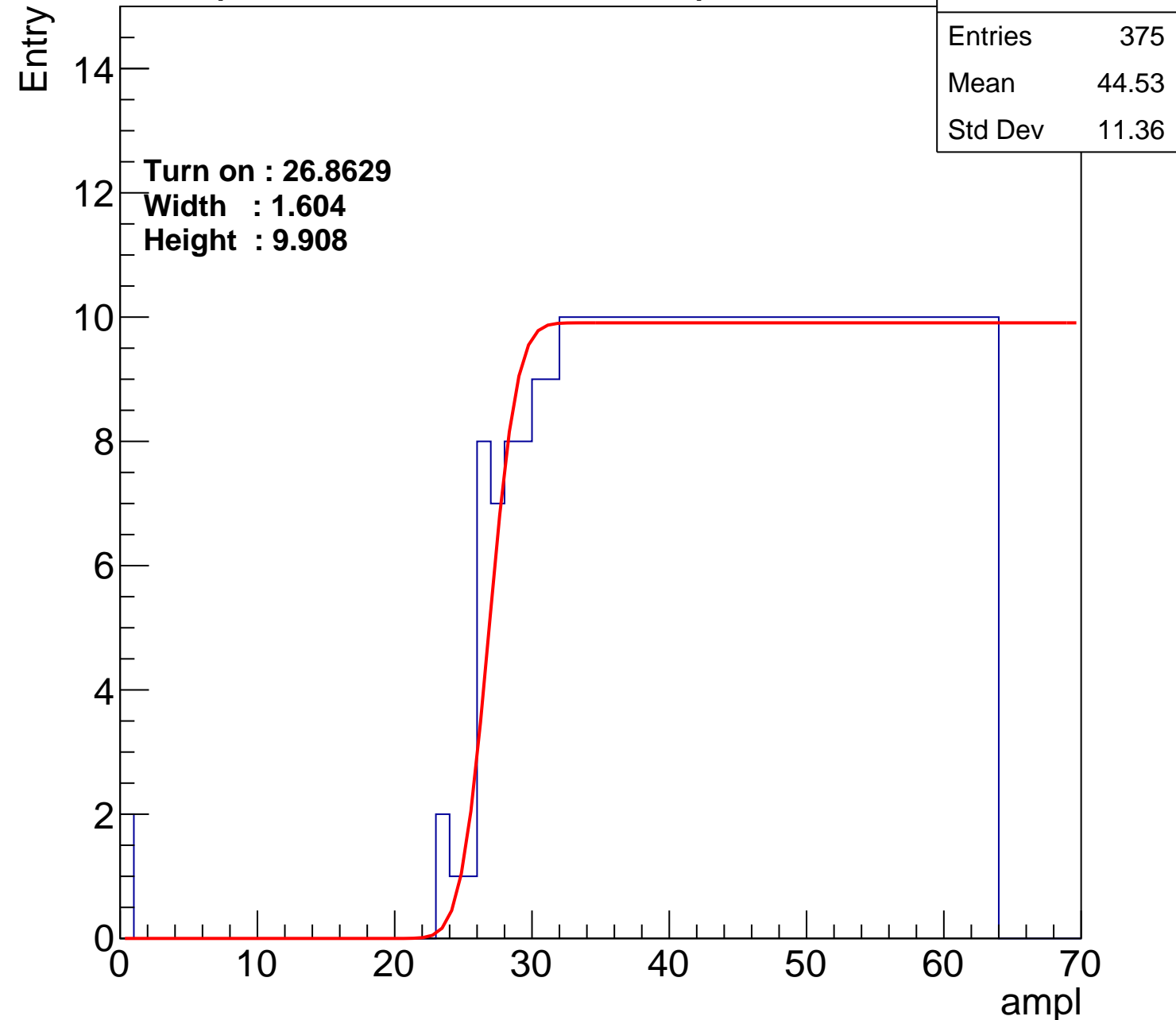
Width : 1.604

Height : 9.908

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch88

calib_packv5_042523_0143.root, FC#9, port A1

Entries	366
Mean	44.89
Std Dev	11.34

Turn on : 27.4704

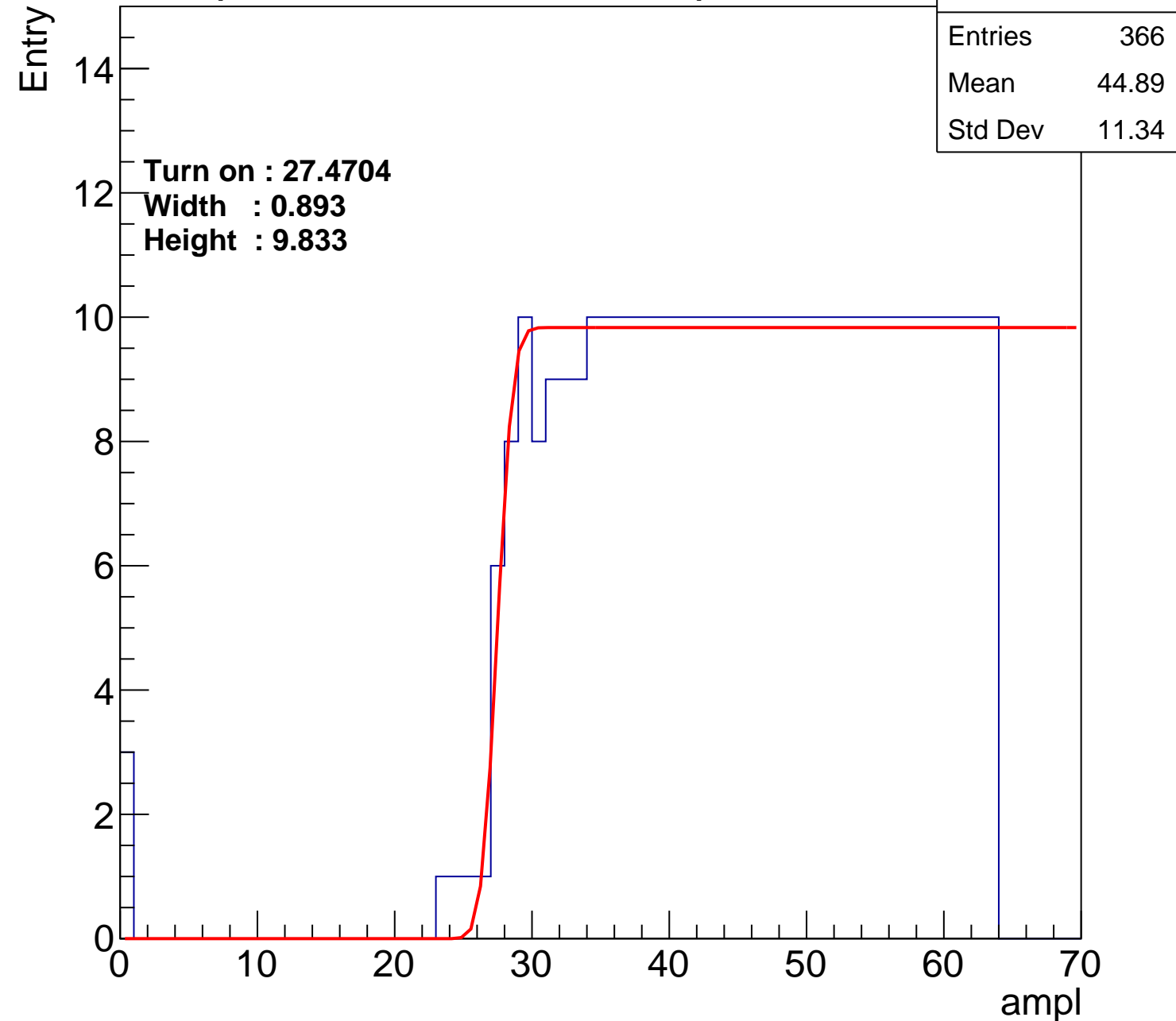
Width : 0.893

Height : 9.833

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch89

calib_packv5_042523_0143.root, FC#9, port A1

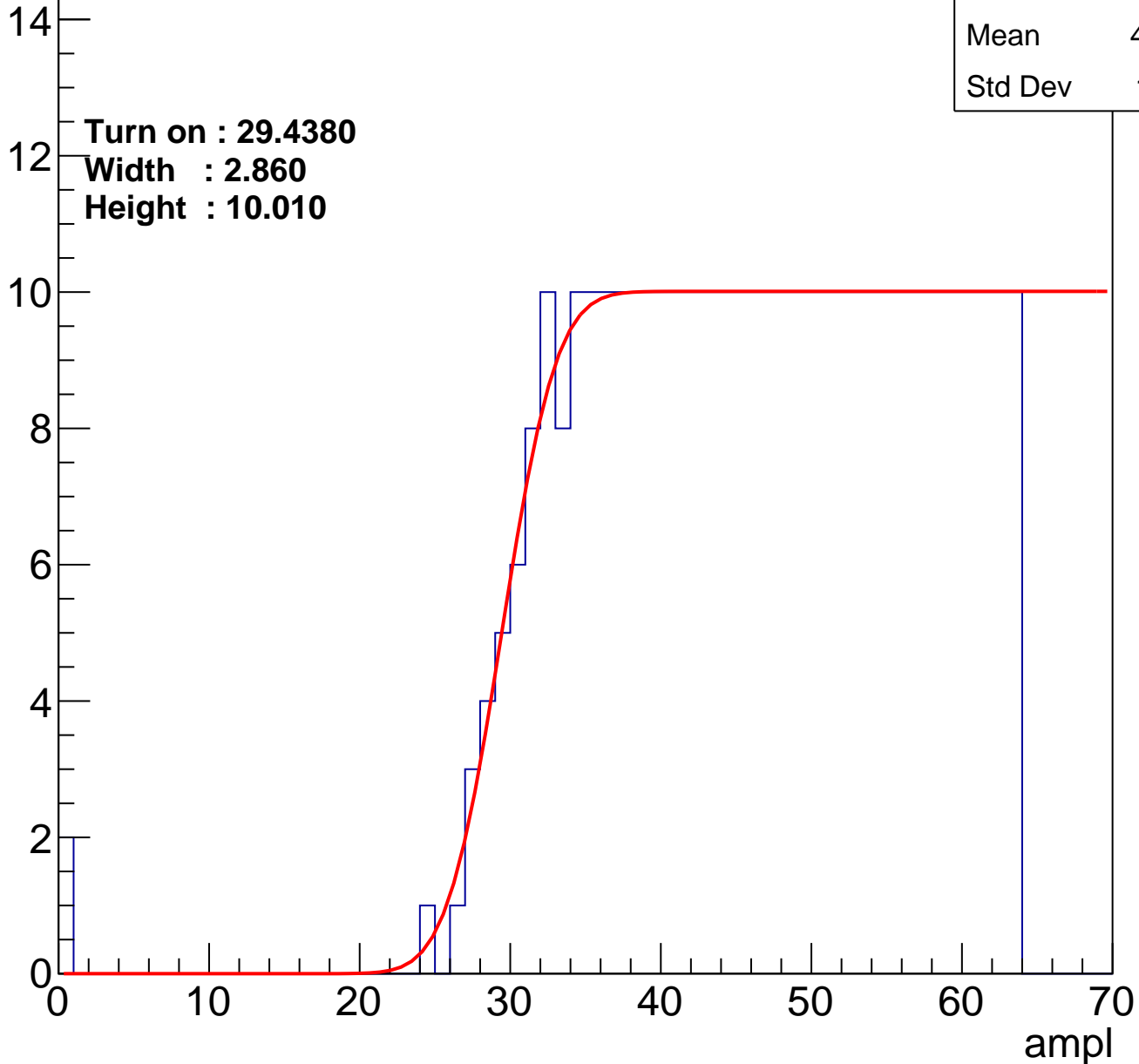
Entries	348
Mean	45.83
Std Dev	10.71

Turn on : 29.4380

Width : 2.860

Height : 10.010

Entry



B0L001S, U17-ch90

calib_packv5_042523_0143.root, FC#9, port A1

Entries	348
Mean	45.62
Std Dev	11.26

Turn on : 29.6813

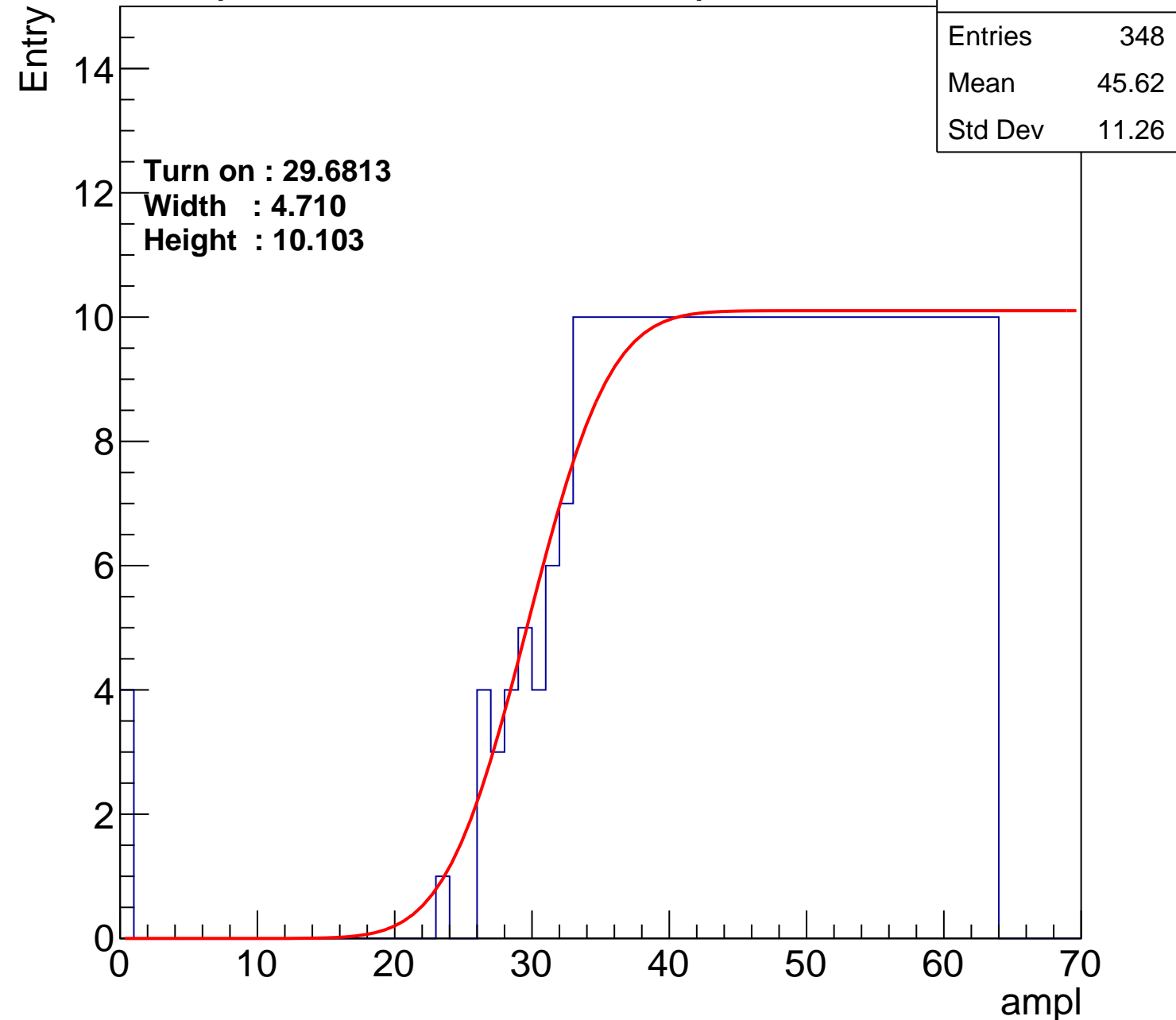
Width : 4.710

Height : 10.103

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch91

calib_packv5_042523_0143.root, FC#9, port A1

Entries	375
Mean	44.47
Std Dev	11.44

Turn on : 26.9165

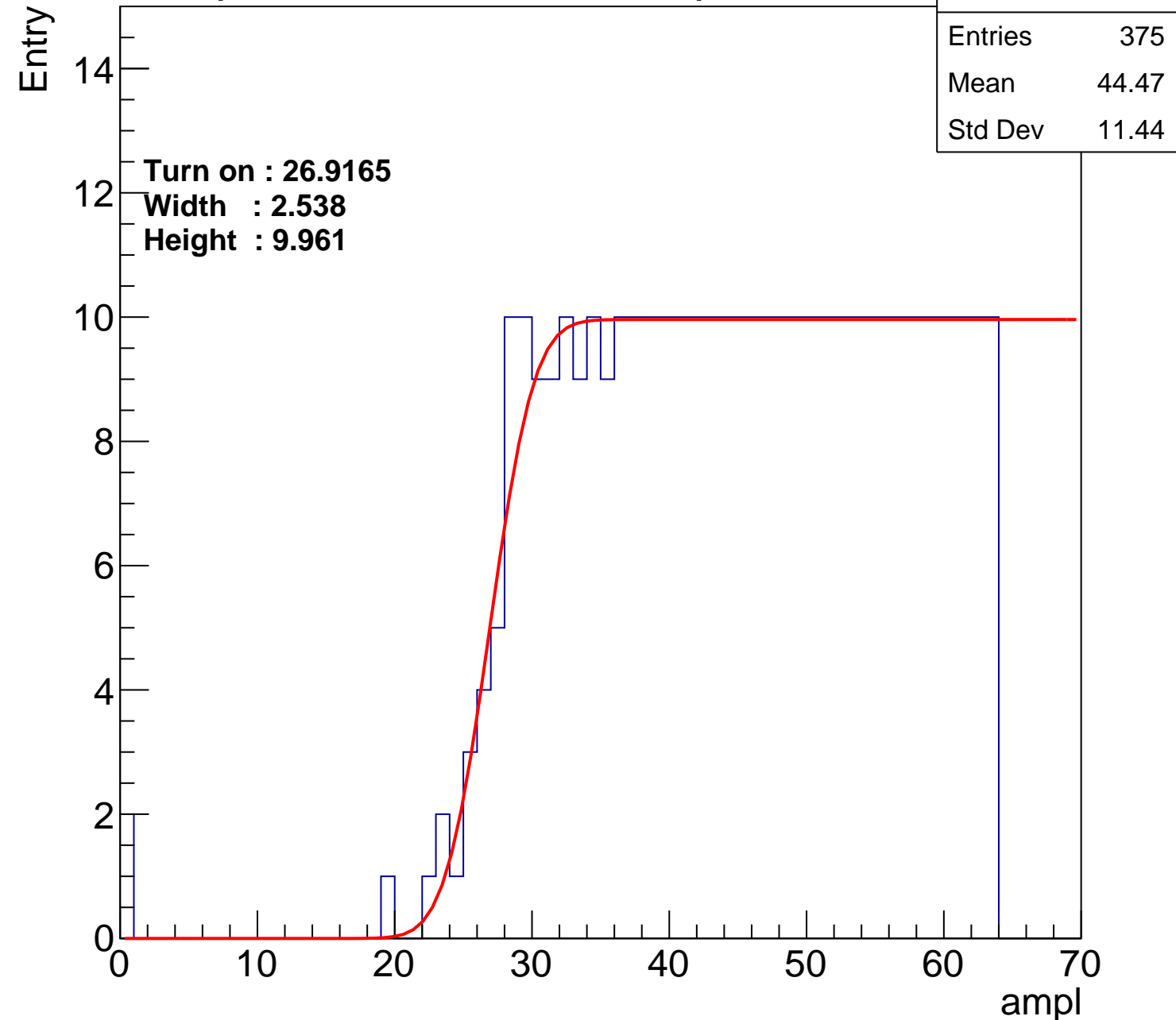
Width : 2.538

Height : 9.961

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch92

calib_packv5_042523_0143.root, FC#9, port A1

Entries	362
Mean	45.17
Std Dev	11.02

Turn on : 27.9529

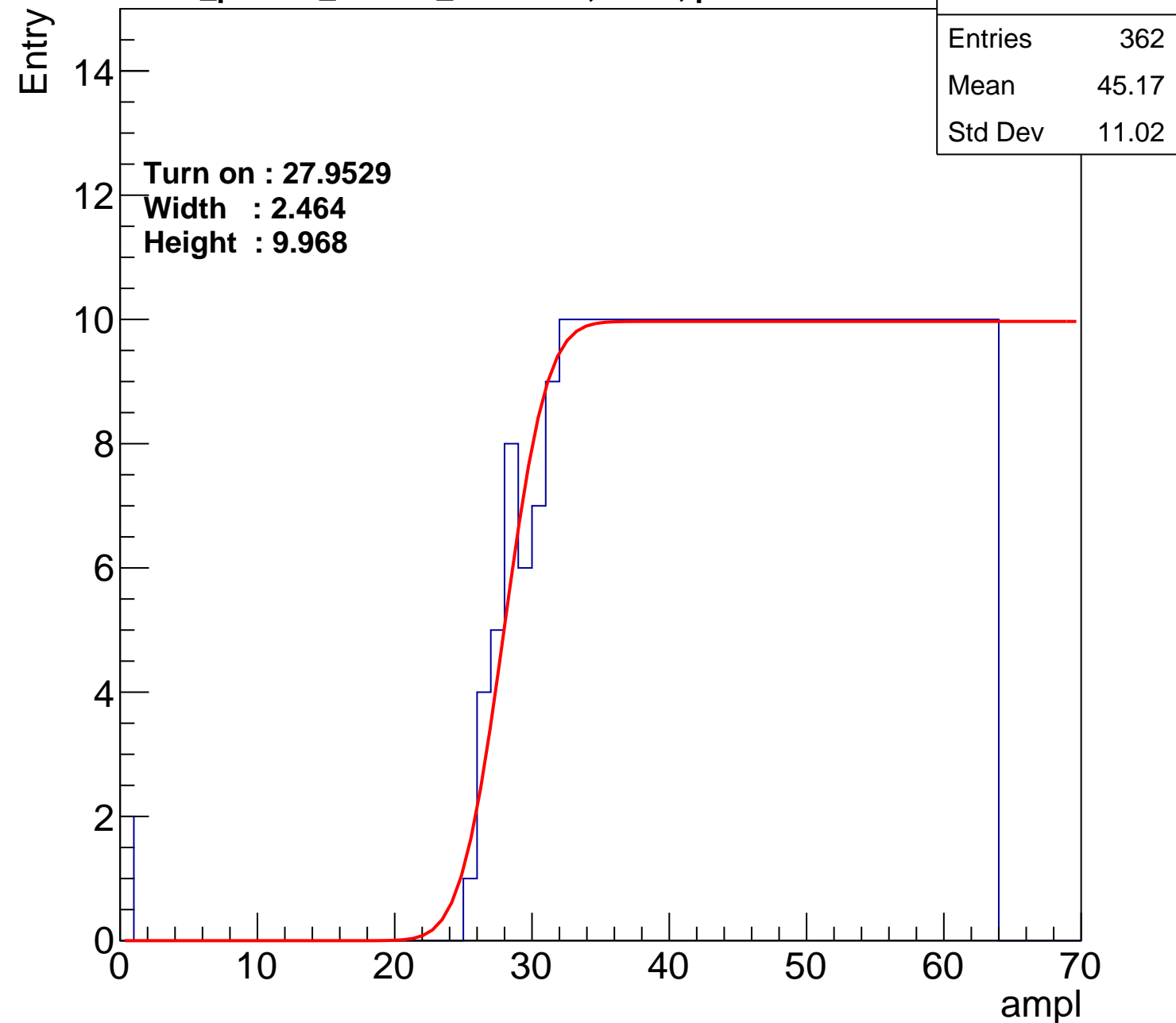
Width : 2.464

Height : 9.968

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch93

calib_packv5_042523_0143.root, FC#9, port A1

Entries	365
Mean	44.99
Std Dev	11.14

Turn on : 28.0369

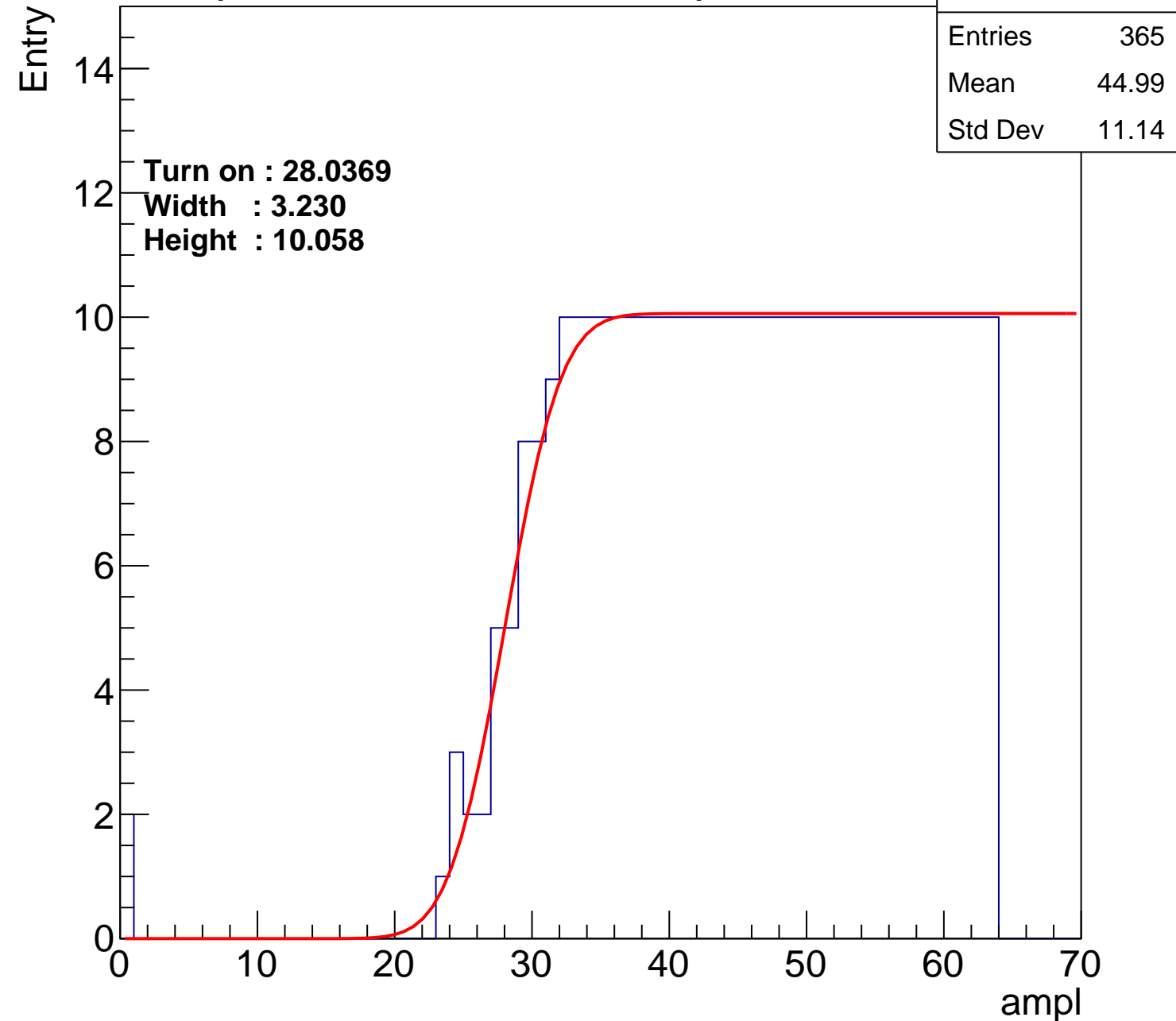
Width : 3.230

Height : 10.058

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch94

calib_packv5_042523_0143.root, FC#9, port A1

Entries	365
Mean	44.99
Std Dev	11.15

Turn on : 27.5410

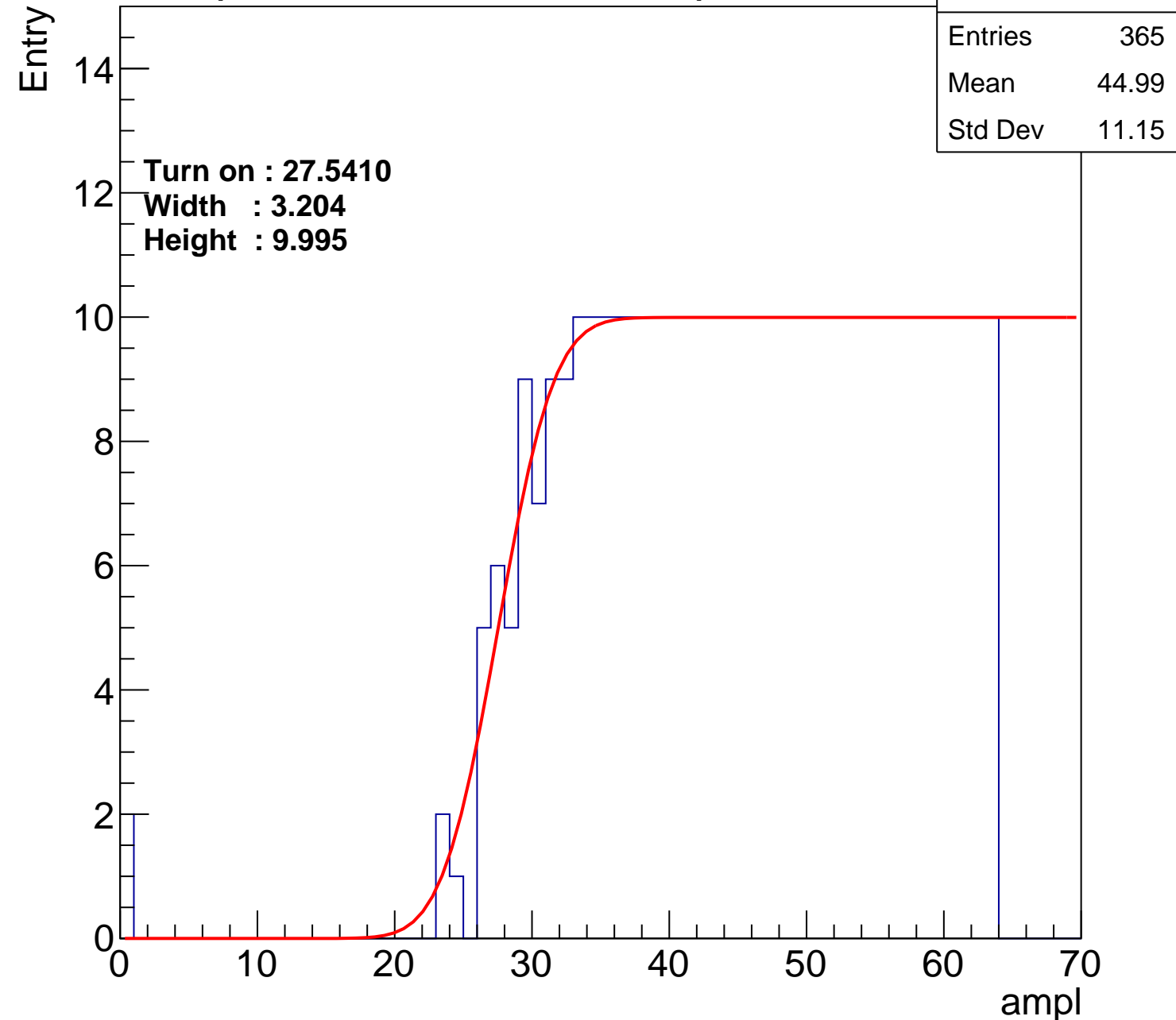
Width : 3.204

Height : 9.995

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch95

calib_packv5_042523_0143.root, FC#9, port A1

Entries	362
Mean	45.01
Std Dev	11.38

Turn on : 29.4021

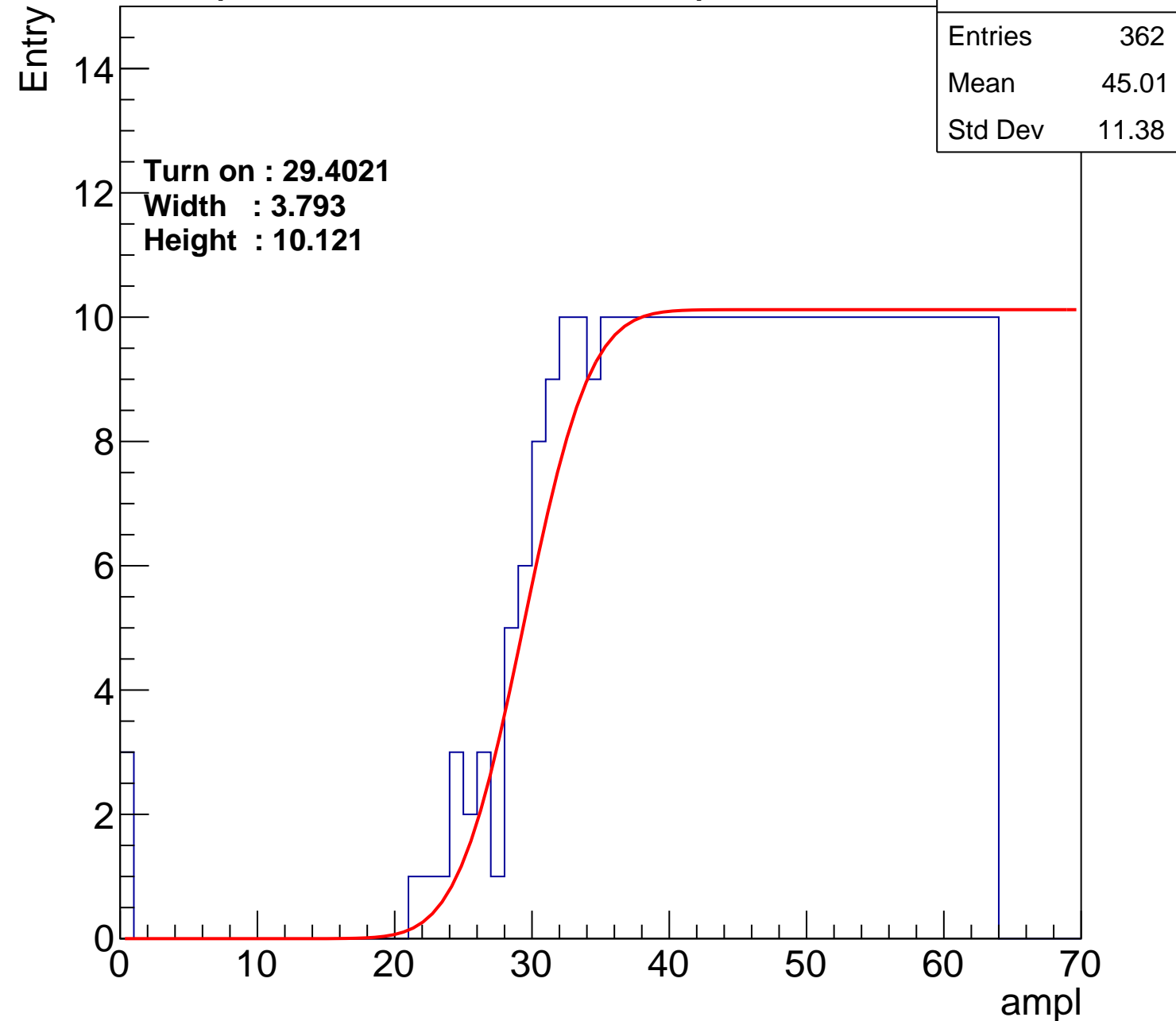
Width : 3.793

Height : 10.121

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch96

calib_packv5_042523_0143.root, FC#9, port A1

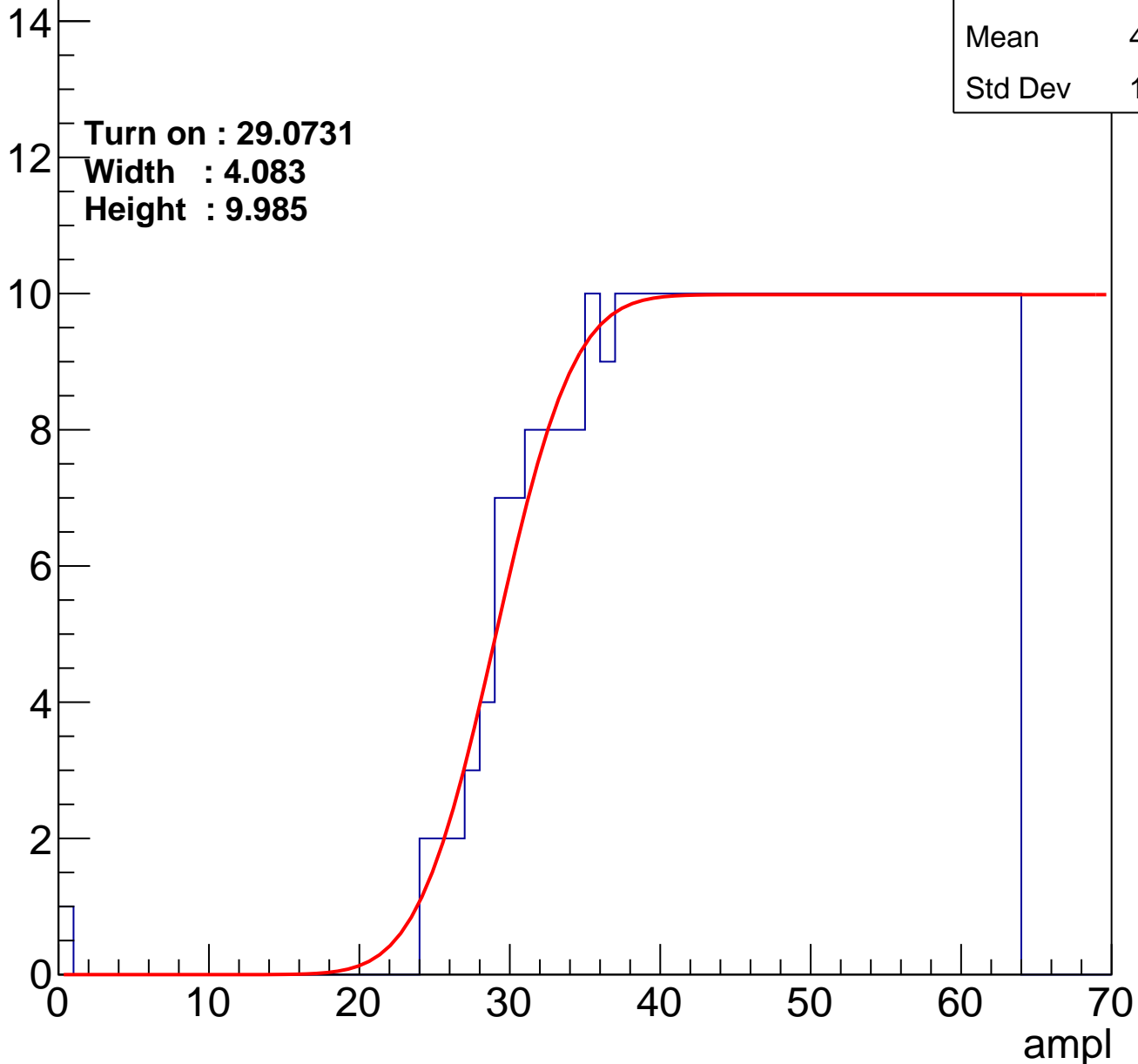
Entries	349
Mean	45.76
Std Dev	10.66

Turn on : 29.0731

Width : 4.083

Height : 9.985

Entry



B0L001S, U17-ch97

calib_packv5_042523_0143.root, FC#9, port A1

Entries	348
Mean	45.66
Std Dev	11.07

Turn on : 29.2530

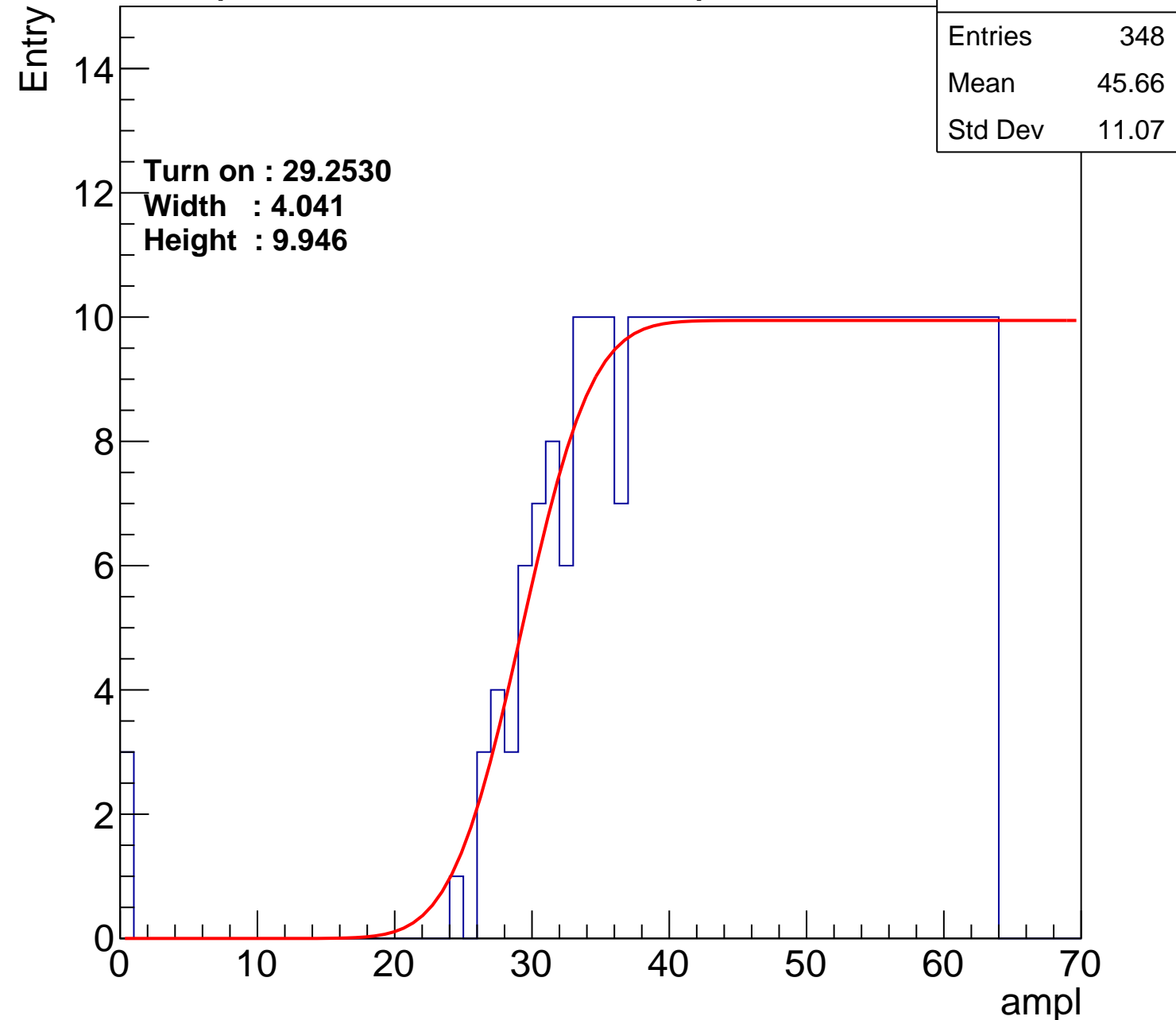
Width : 4.041

Height : 9.946

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch98

calib_packv5_042523_0143.root, FC#9, port A1

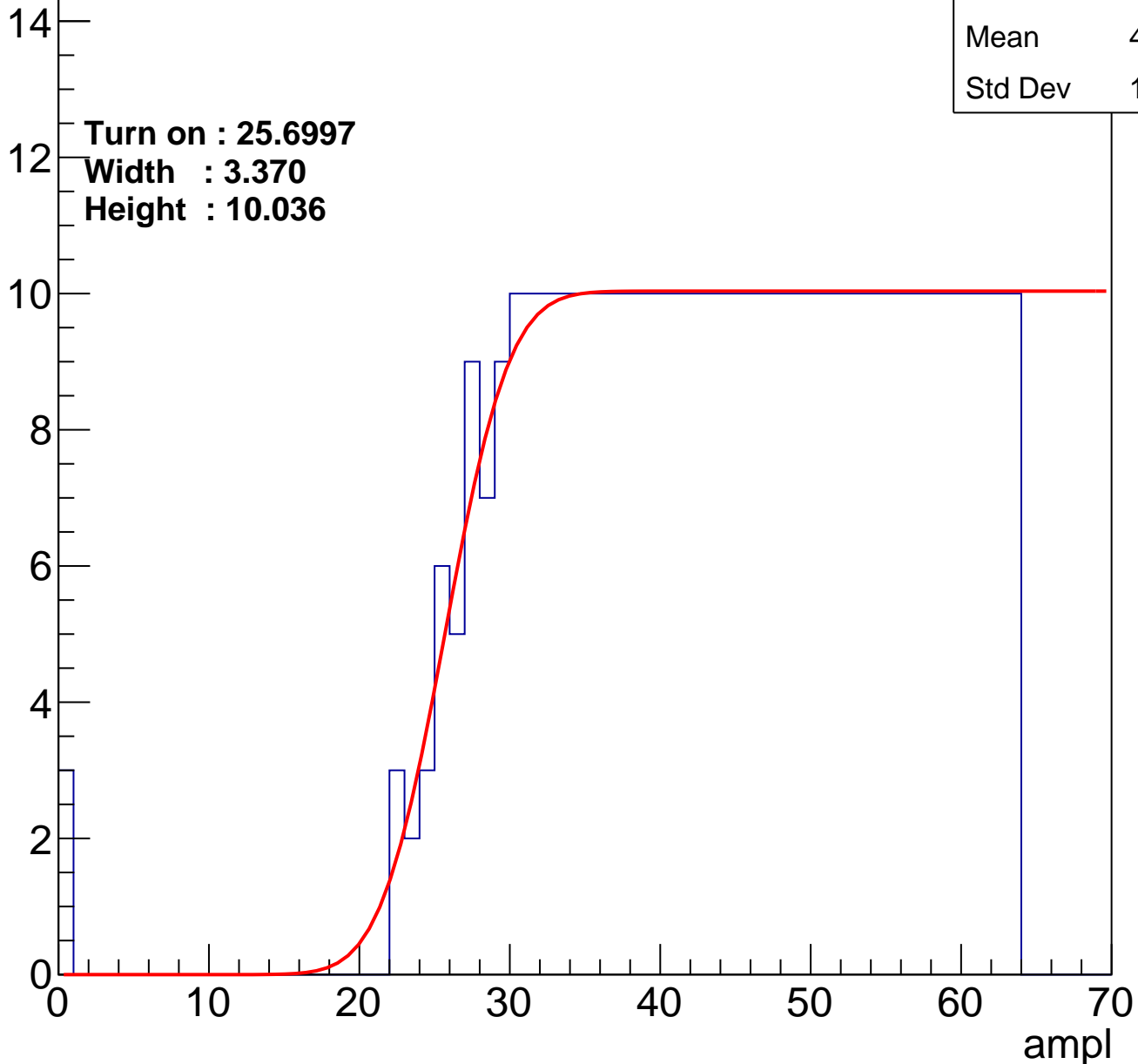
Entries	387
Mean	43.86
Std Dev	11.85

Turn on : 25.6997

Width : 3.370

Height : 10.036

Entry



B0L001S, U17-ch99

calib_packv5_042523_0143.root, FC#9, port A1

Entries	360
Mean	44.97
Std Dev	11.72

Turn on : 28.9985

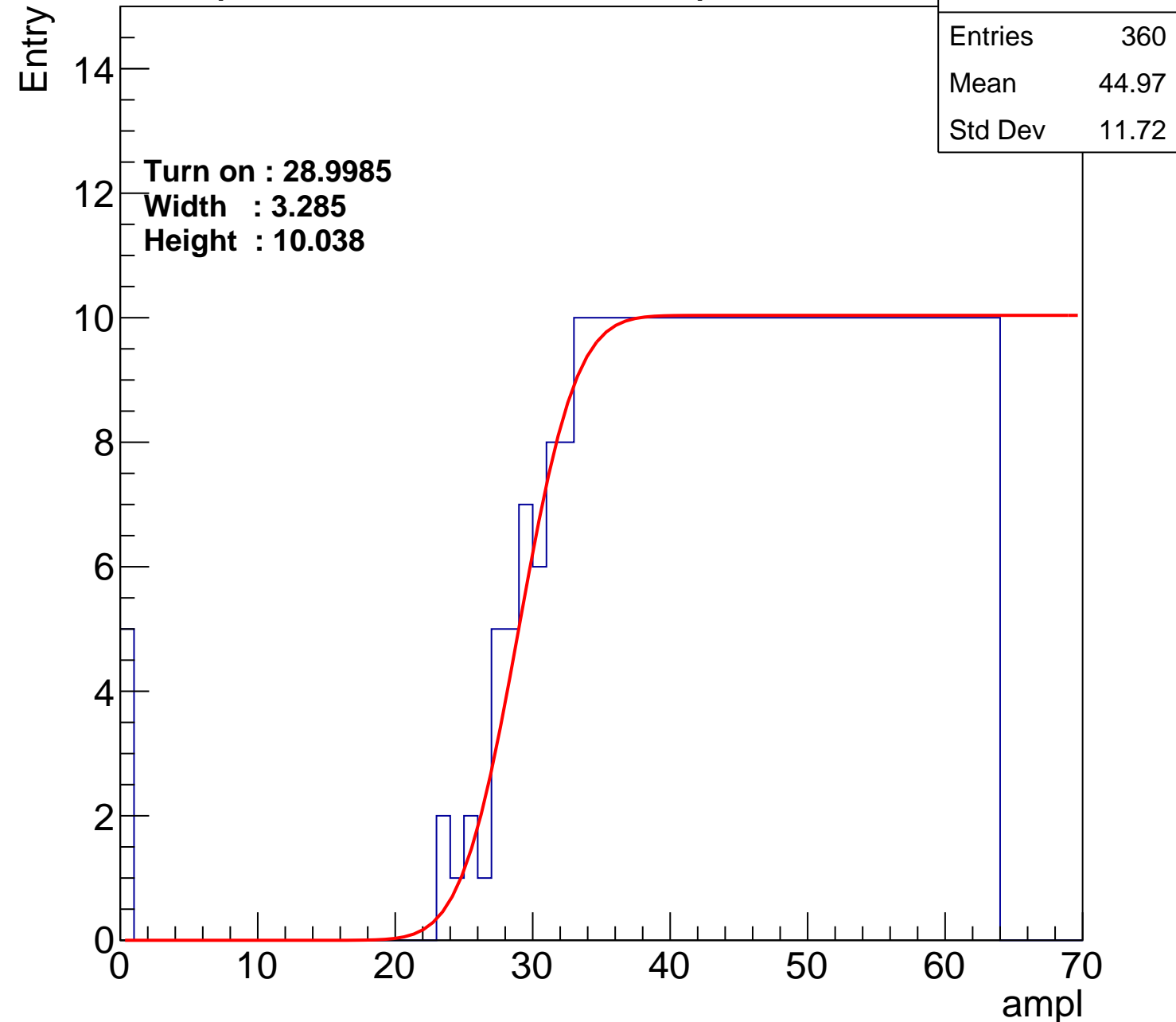
Width : 3.285

Height : 10.038

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch100

calib_packv5_042523_0143.root, FC#9, port A1

Entries	357
Mean	45.37
Std Dev	10.97

Turn on : 28.5971

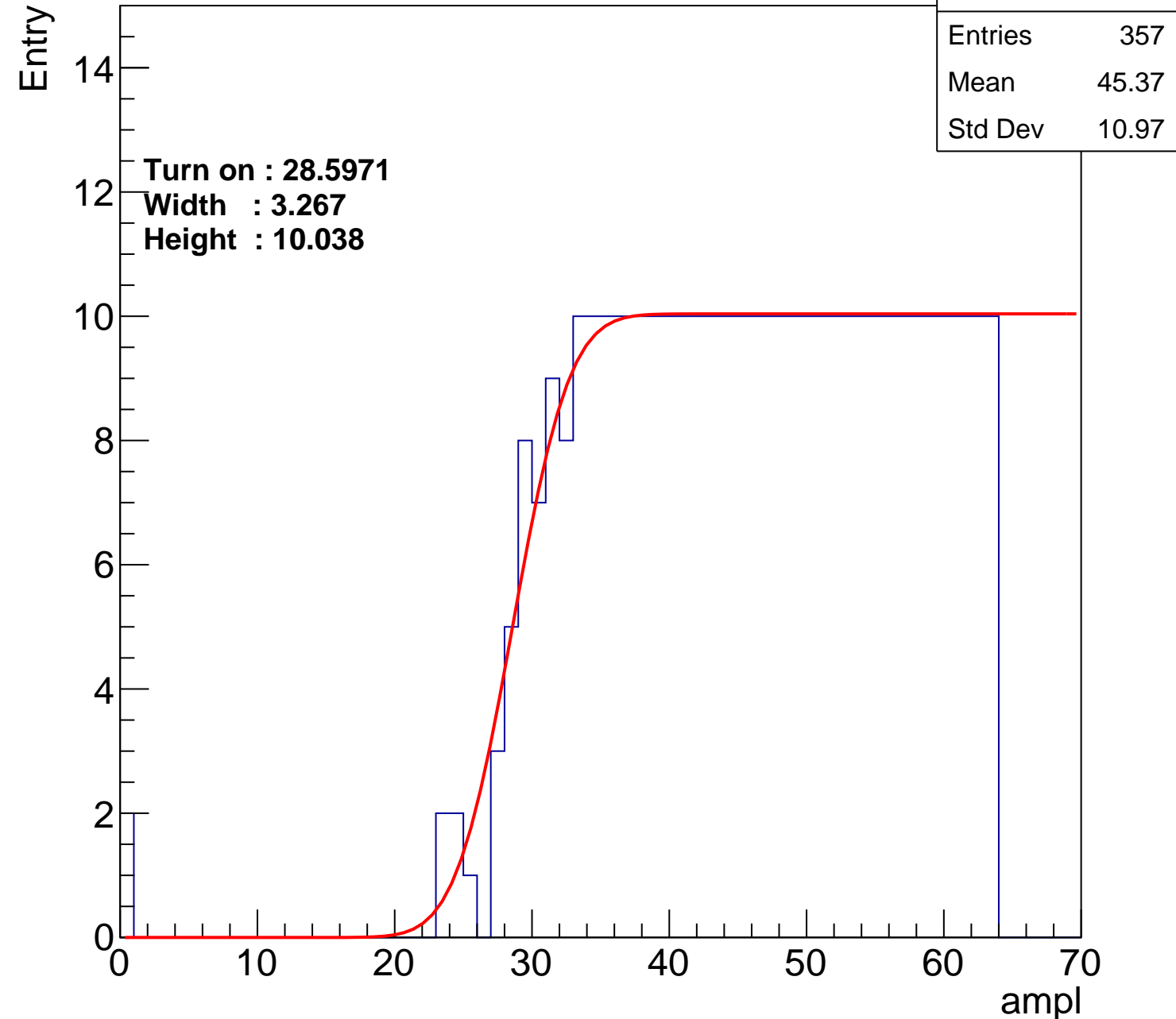
Width : 3.267

Height : 10.038

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch101

calib_packv5_042523_0143.root, FC#9, port A1

Entries	382
Mean	44.06
Std Dev	11.87

Turn on : 26.3135

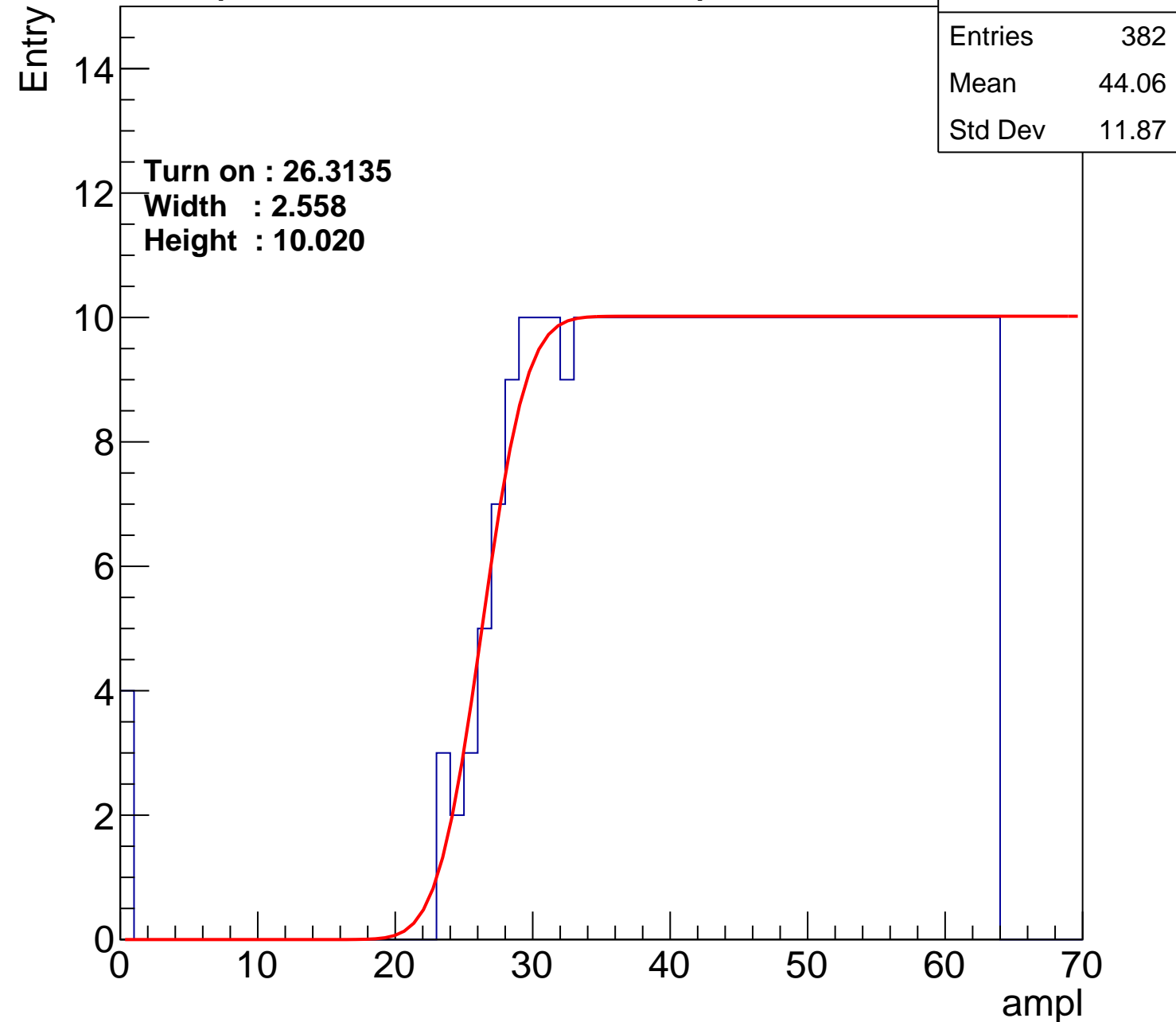
Width : 2.558

Height : 10.020

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch102

calib_packv5_042523_0143.root, FC#9, port A1

Entries	371
Mean	44.48
Std Dev	11.89

Turn on : 27.8725

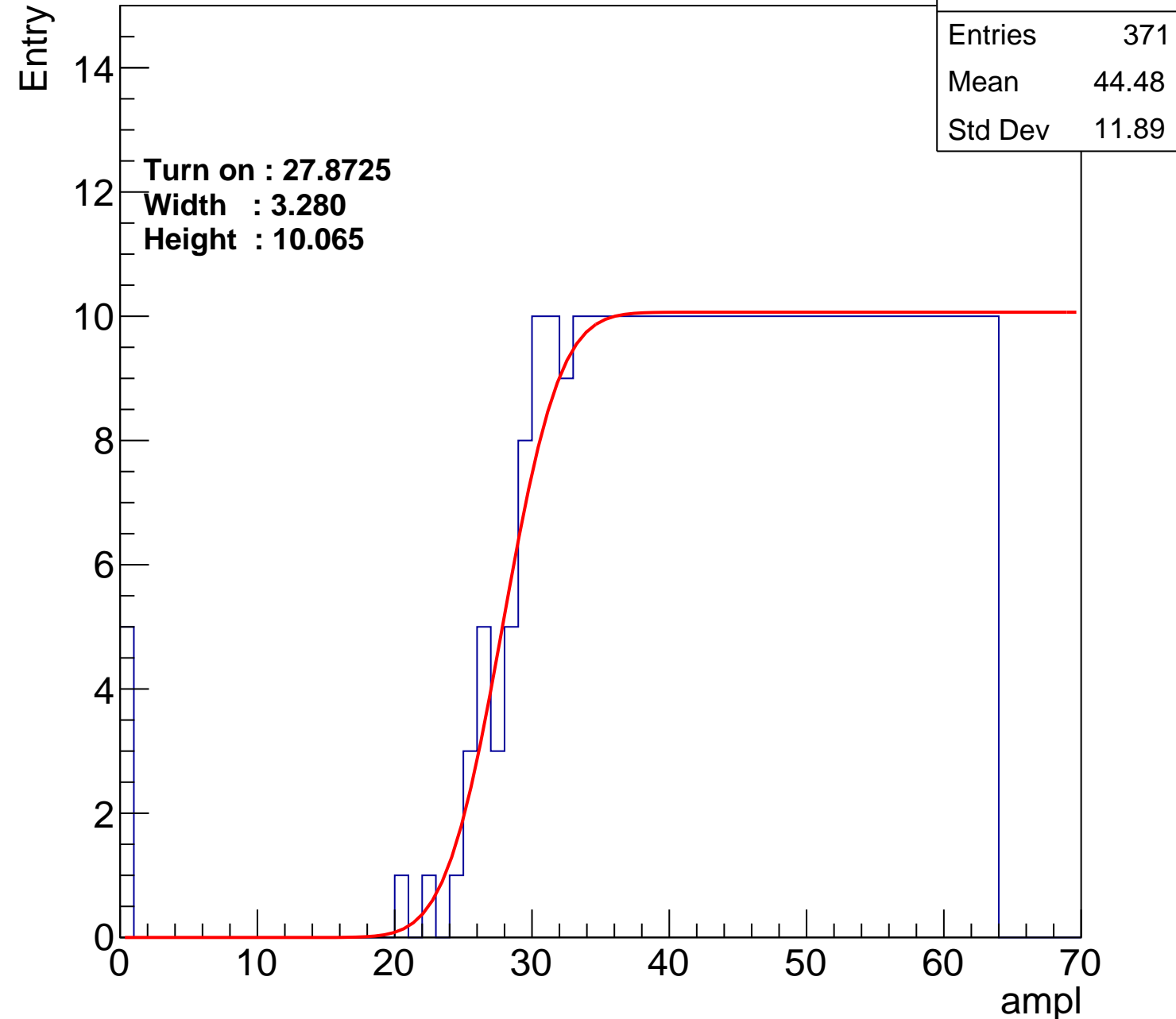
Width : 3.280

Height : 10.065

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch103

calib_packv5_042523_0143.root, FC#9, port A1

Entries	362
Mean	44.96
Std Dev	11.54

Turn on : 28.6039

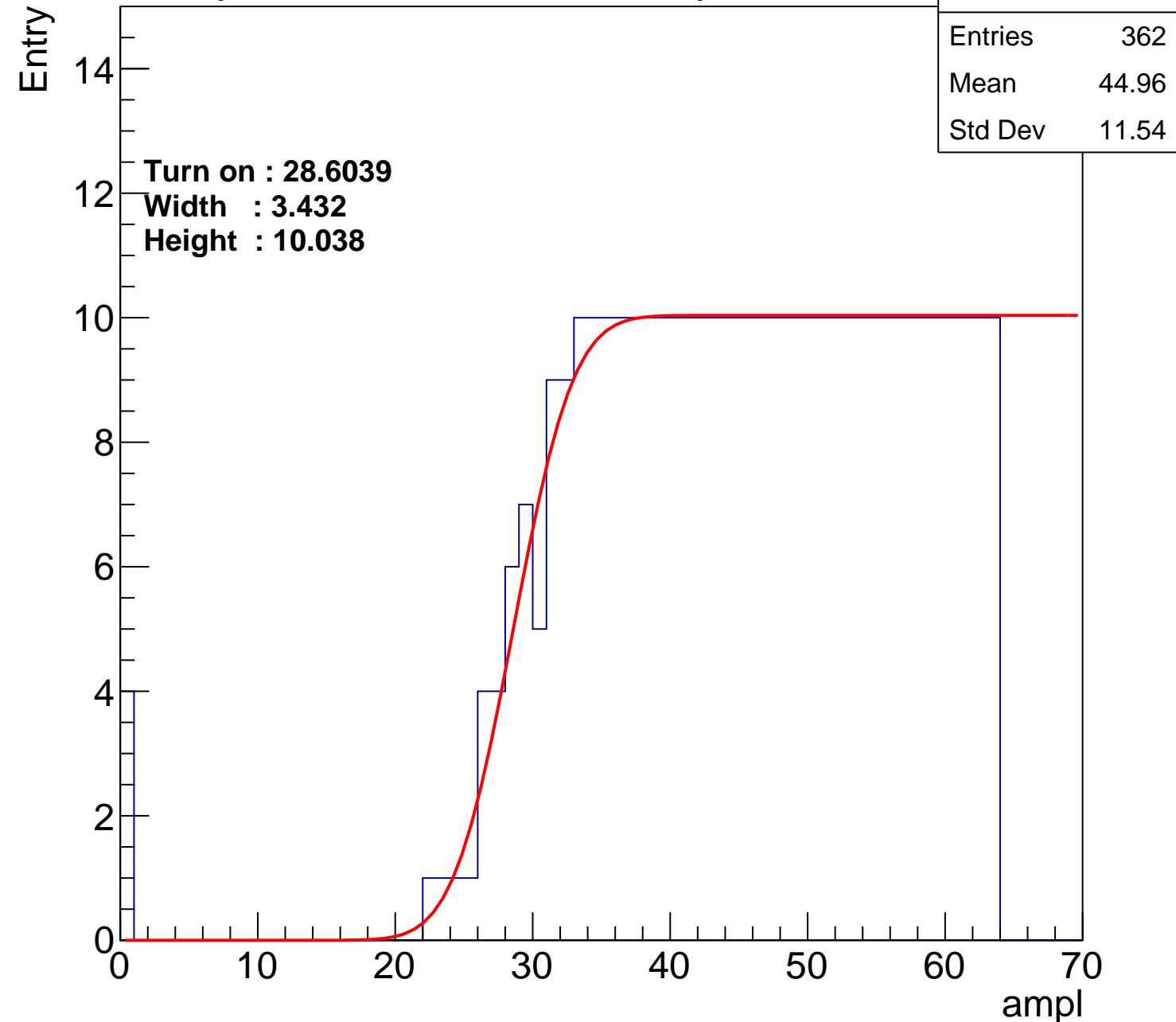
Width : 3.432

Height : 10.038

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch104

calib_packv5_042523_0143.root, FC#9, port A1

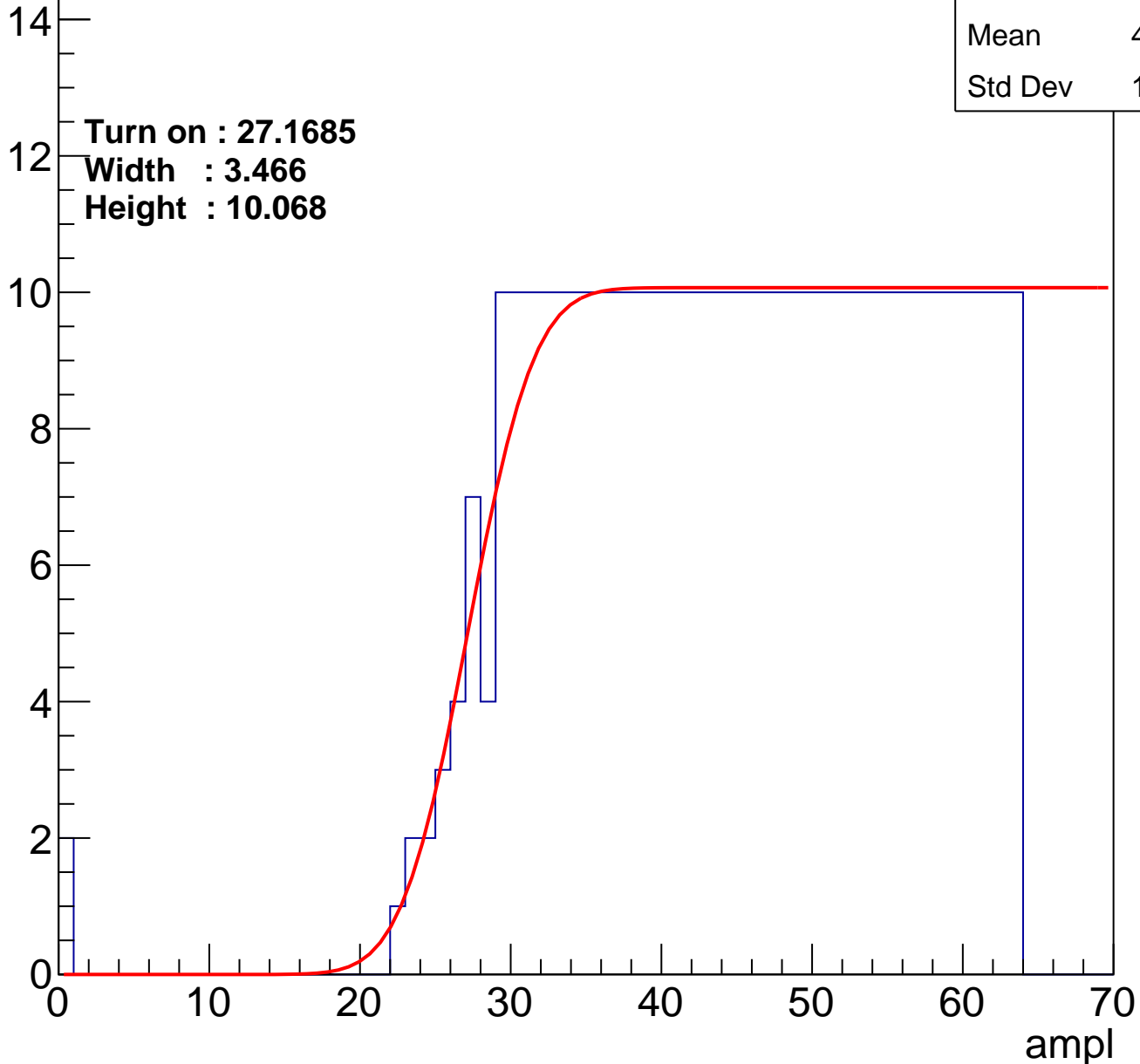
Entries	375
Mean	44.52
Std Dev	11.37

Turn on : 27.1685

Width : 3.466

Height : 10.068

Entry



B0L001S, U17-ch105

calib_packv5_042523_0143.root, FC#9, port A1

Entries	383
Mean	44.04
Std Dev	11.78

Turn on : 25.9388

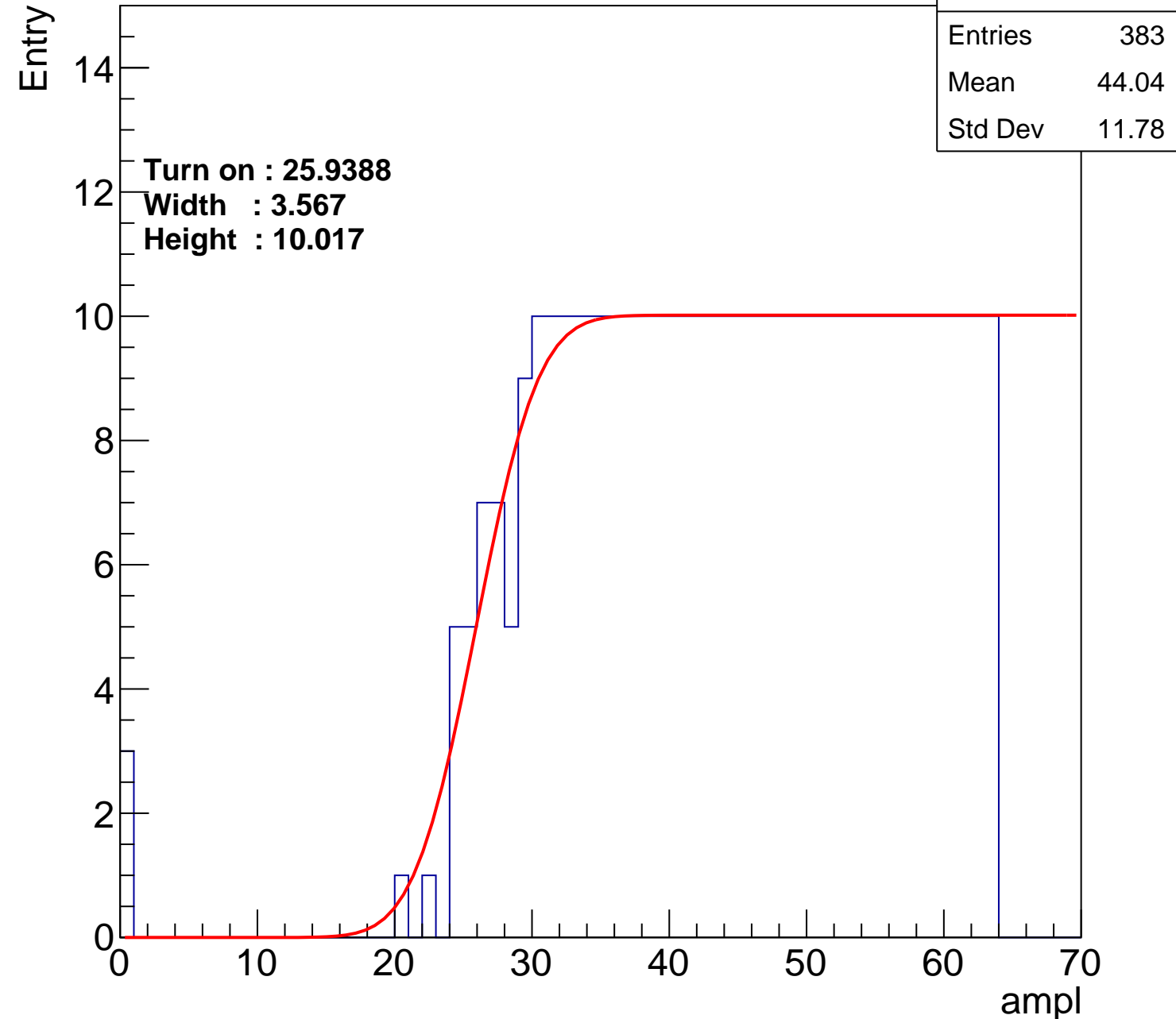
Width : 3.567

Height : 10.017

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch106

calib_packv5_042523_0143.root, FC#9, port A1

Entries	357
Mean	45.39
Std Dev	10.93

Turn on : 28.5221

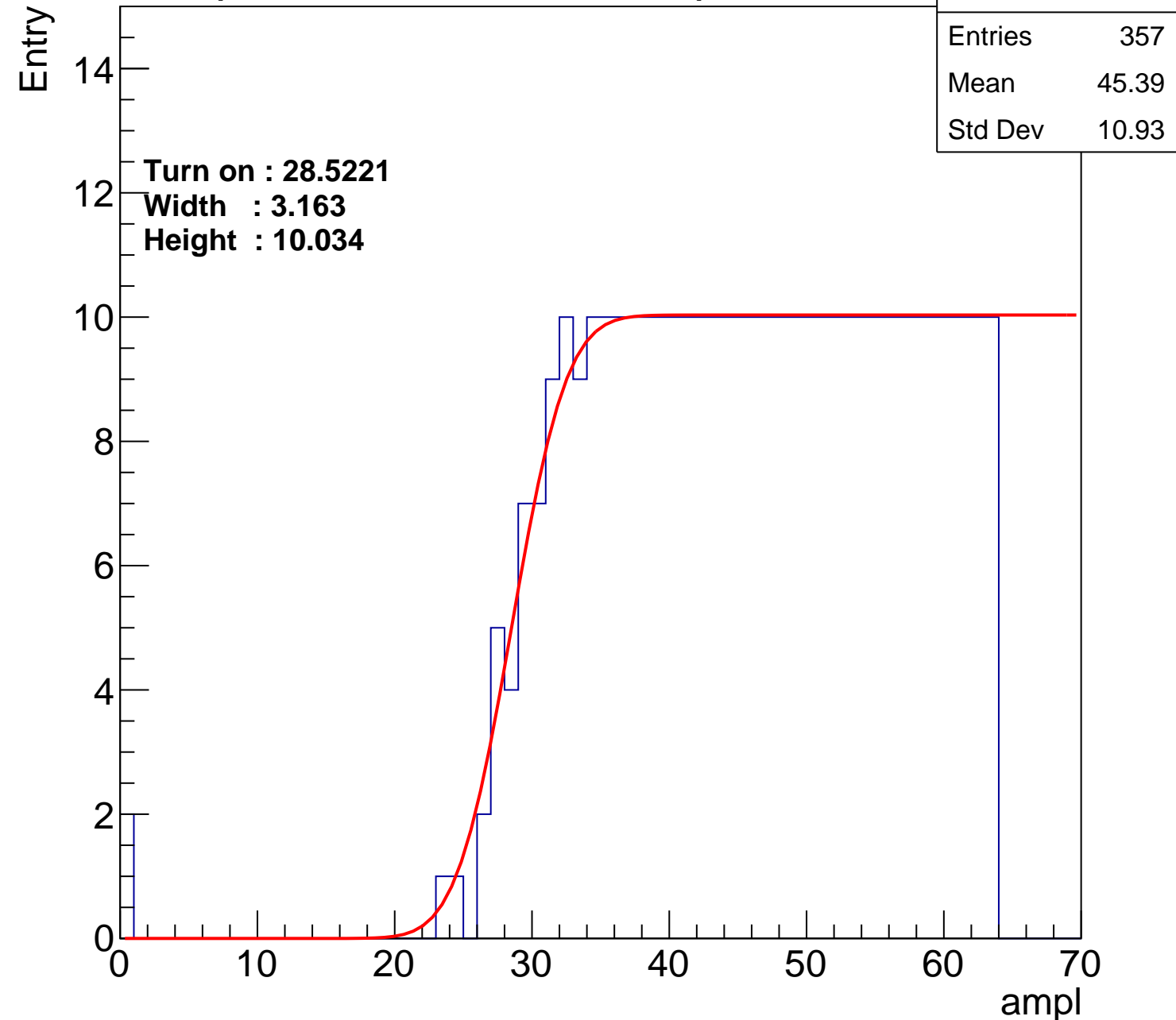
Width : 3.163

Height : 10.034

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch107

calib_packv5_042523_0143.root, FC#9, port A1

Entries	359
Mean	45.08
Std Dev	11.51

Turn on : 28.4512

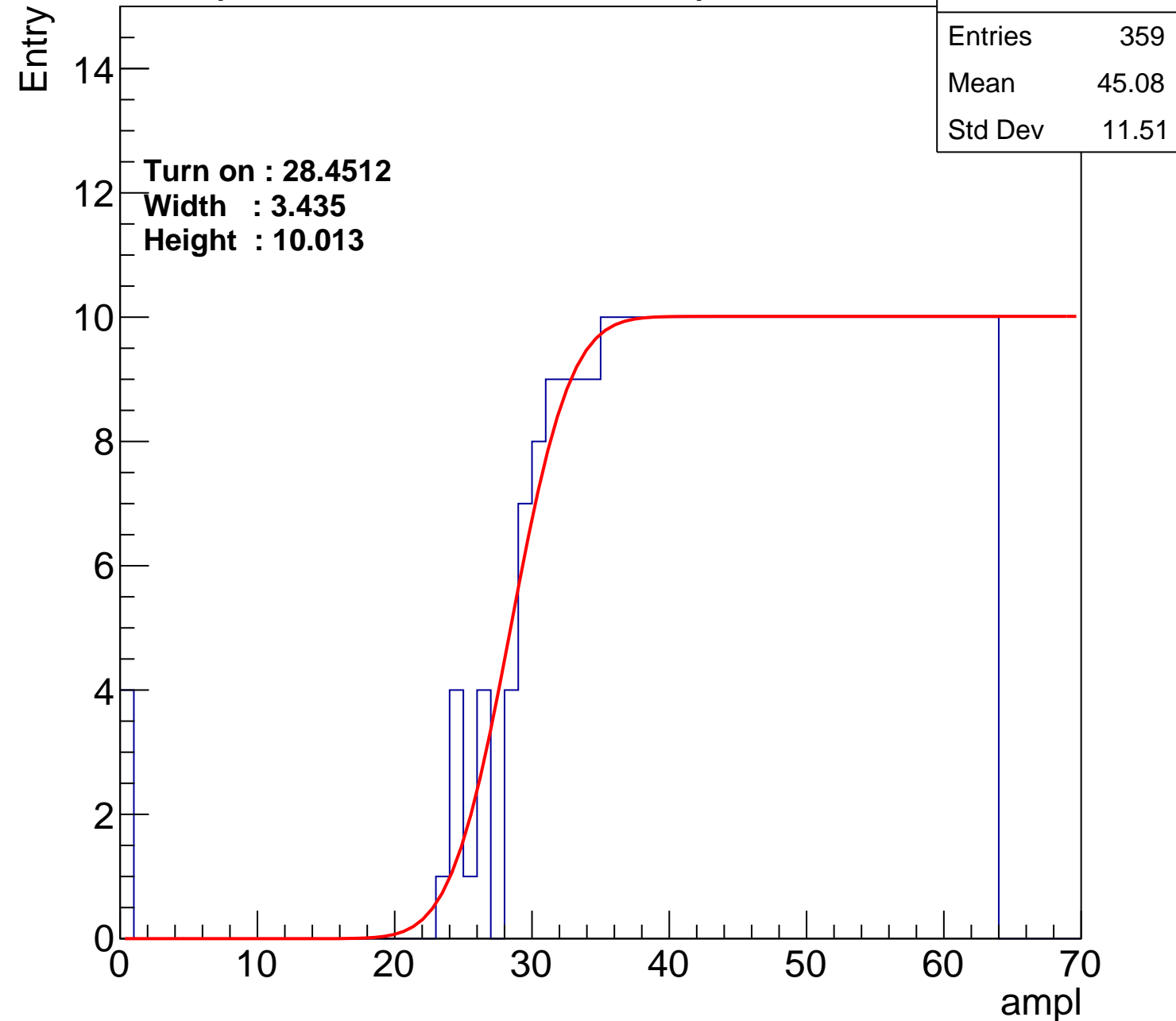
Width : 3.435

Height : 10.013

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch108

calib_packv5_042523_0143.root, FC#9, port A1

Entries	384
Mean	43.98
Std Dev	11.83

Turn on : 26.6048

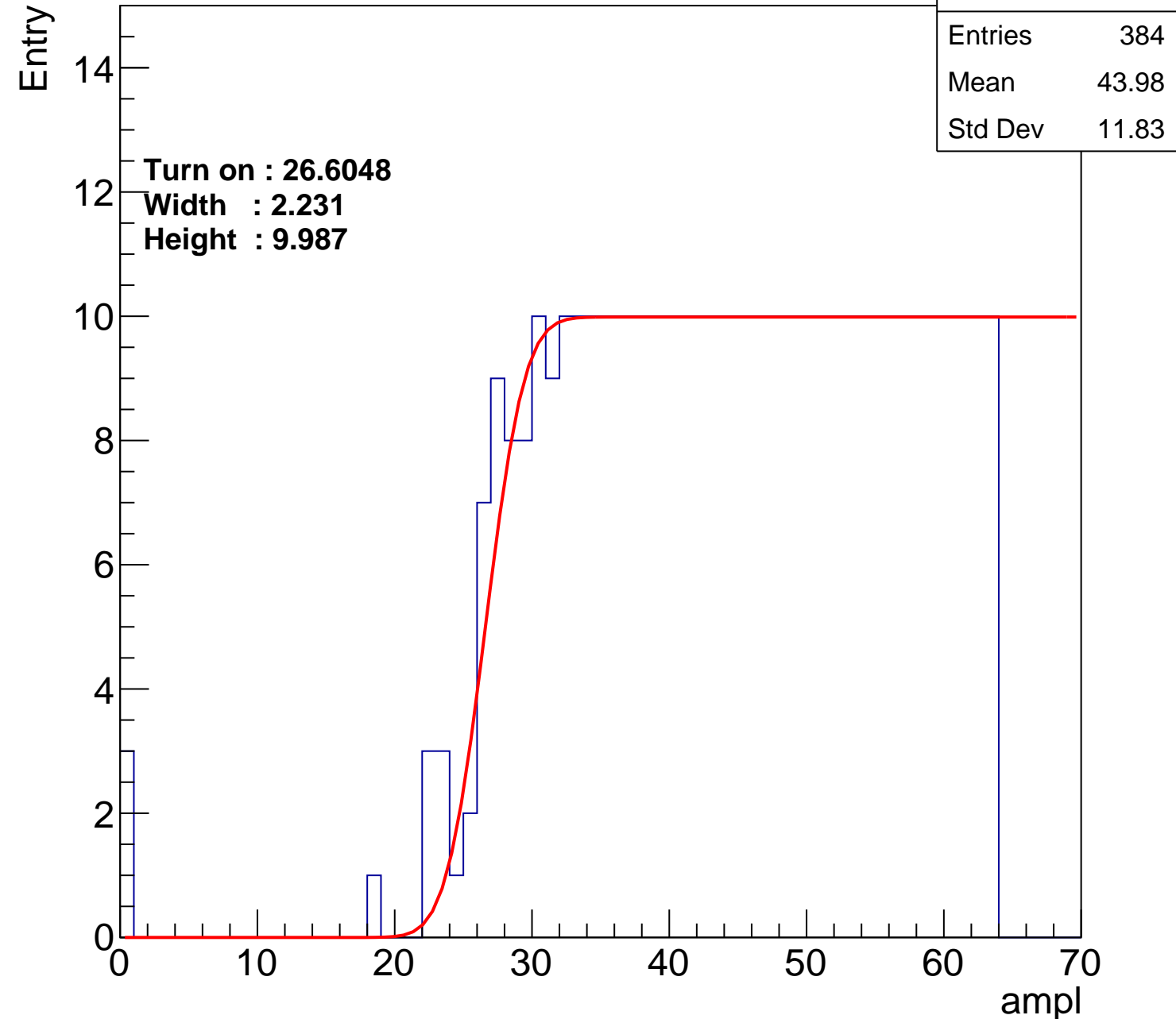
Width : 2.231

Height : 9.987

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch109

calib_packv5_042523_0143.root, FC#9, port A1

Entries	353
Mean	45.47
Std Dev	11.13

Turn on : 29.7403

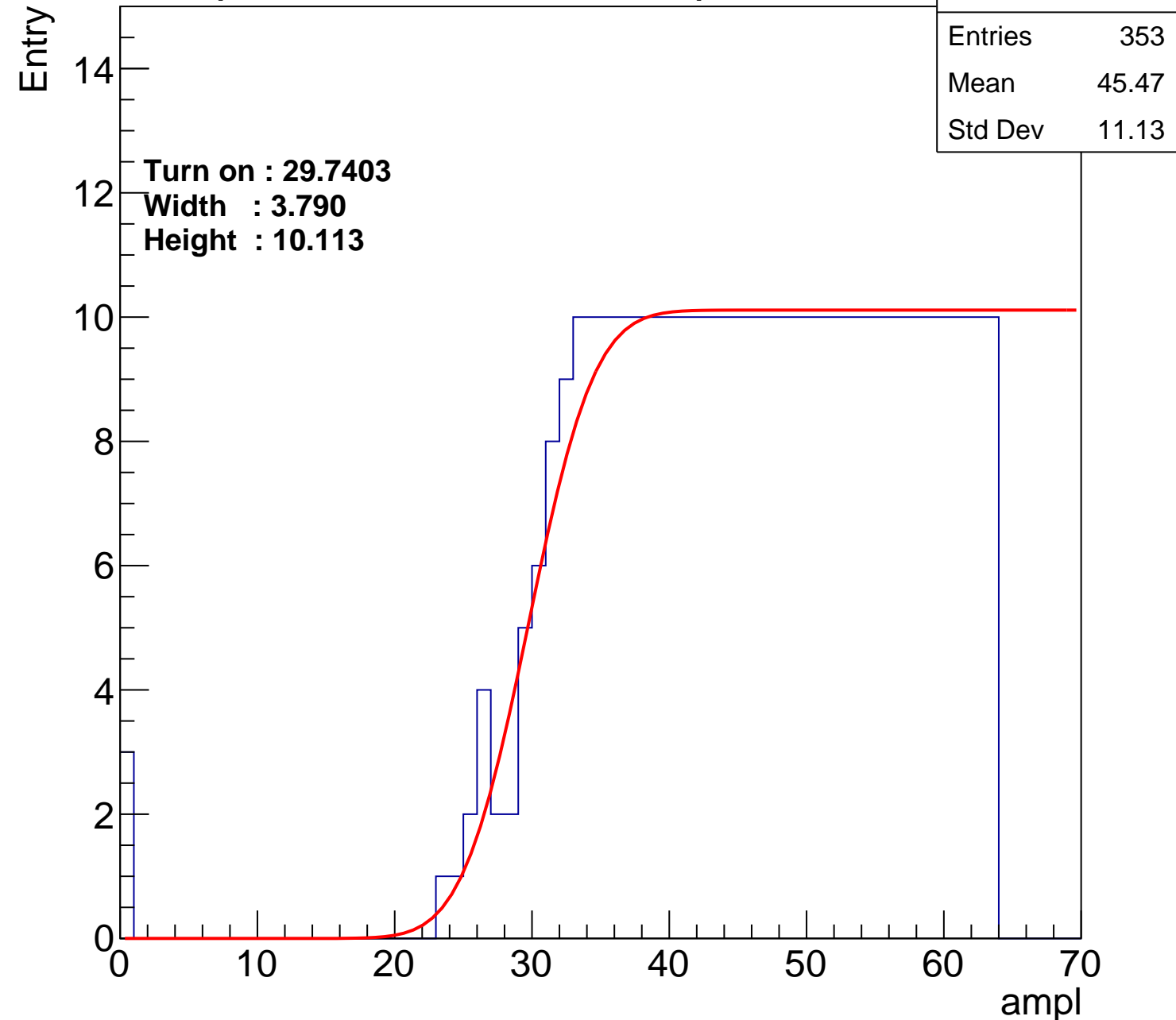
Width : 3.790

Height : 10.113

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch110

calib_packv5_042523_0143.root, FC#9, port A1

Entries	370
Mean	44.59
Std Dev	11.77

Turn on : 28.0768

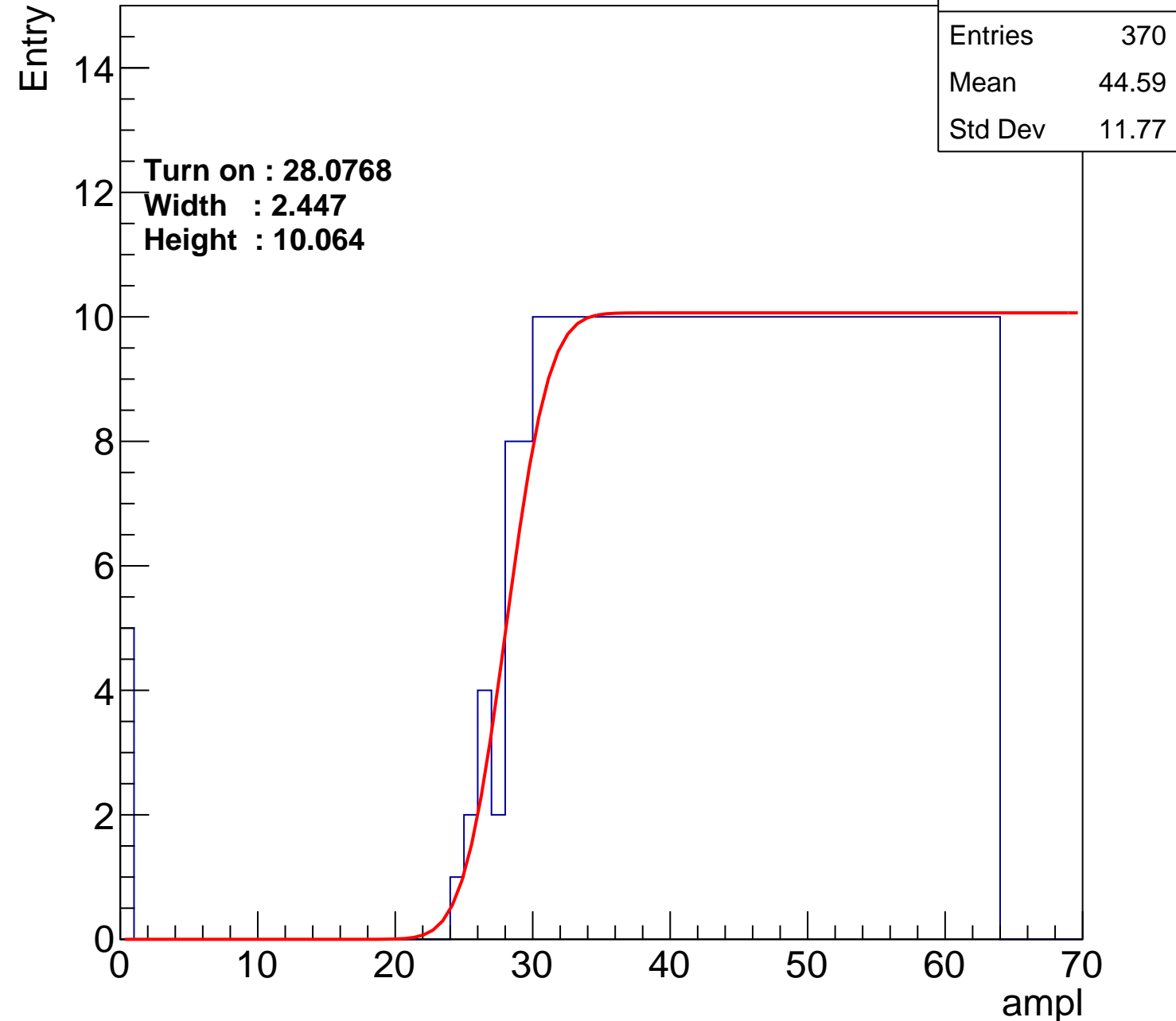
Width : 2.447

Height : 10.064

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch111

calib_packv5_042523_0143.root, FC#9, port A1

Entries	357
Mean	45.21
Std Dev	11.42

Turn on : 30.3204

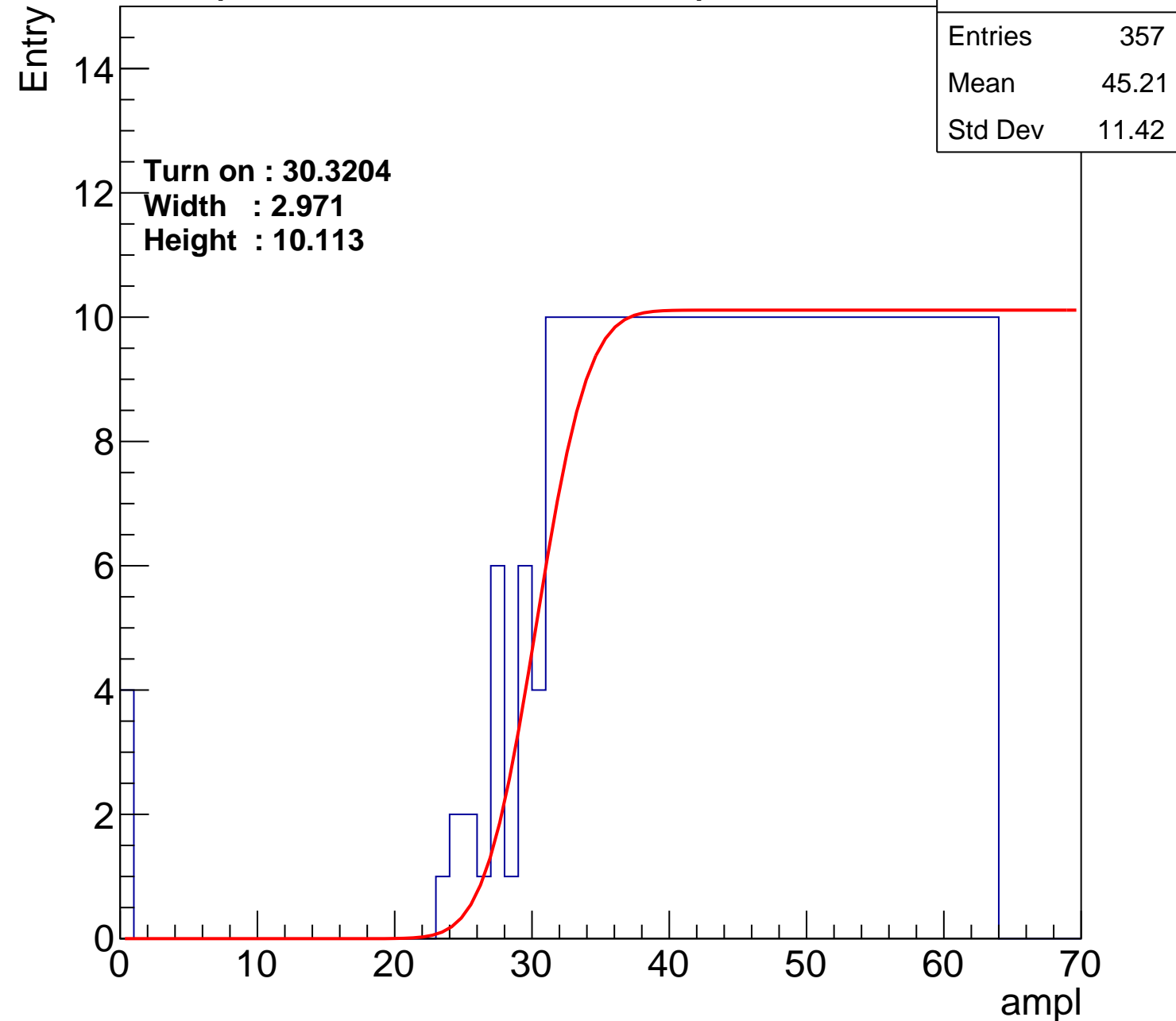
Width : 2.971

Height : 10.113

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch112

calib_packv5_042523_0143.root, FC#9, port A1

Entries	374
Mean	44.32
Std Dev	11.96

Turn on : 26.4590

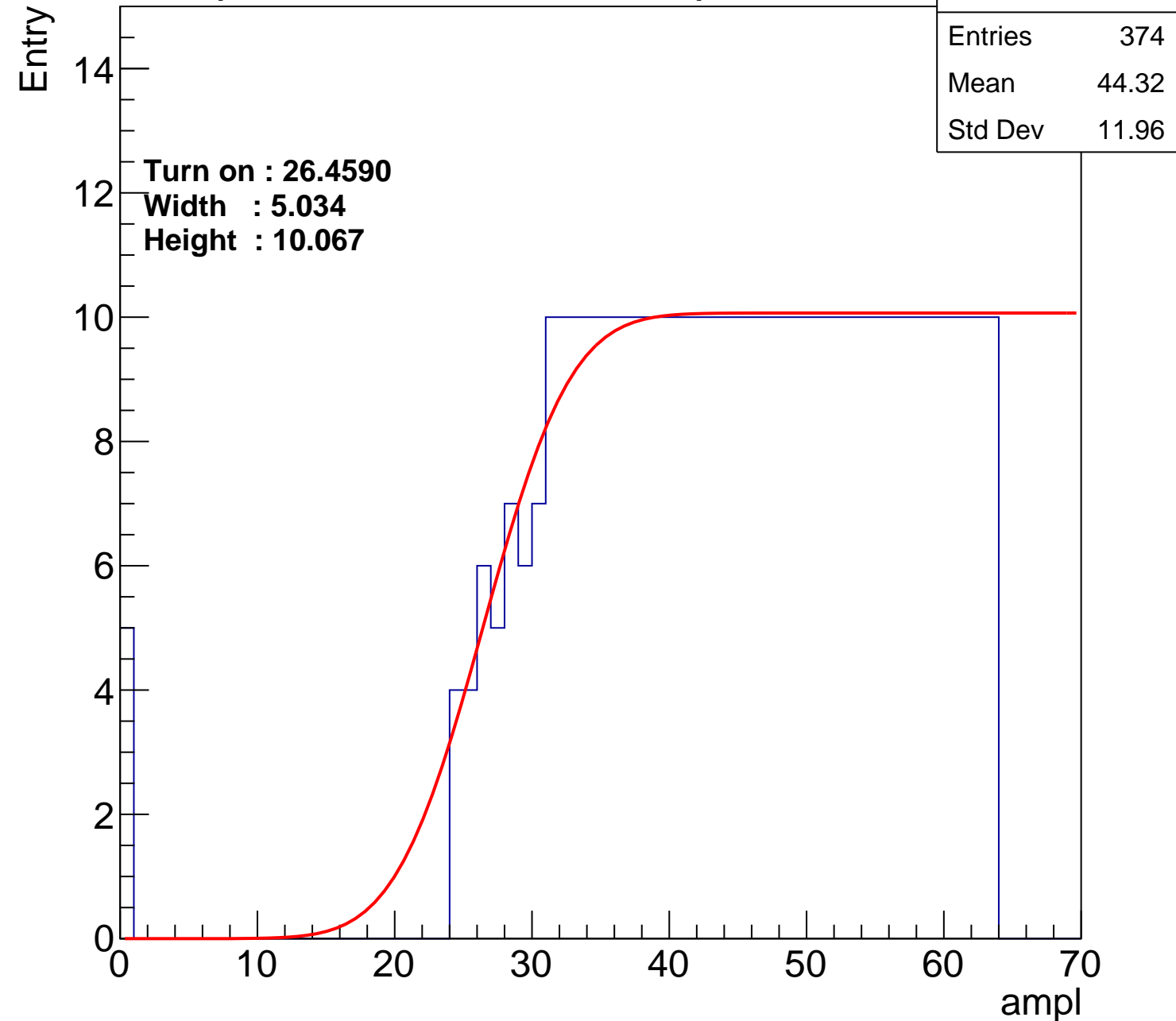
Width : 5.034

Height : 10.067

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch113

calib_packv5_042523_0143.root, FC#9, port A1

Entries	351
Mean	45.58
Std Dev	11.06

Turn on : 29.7519

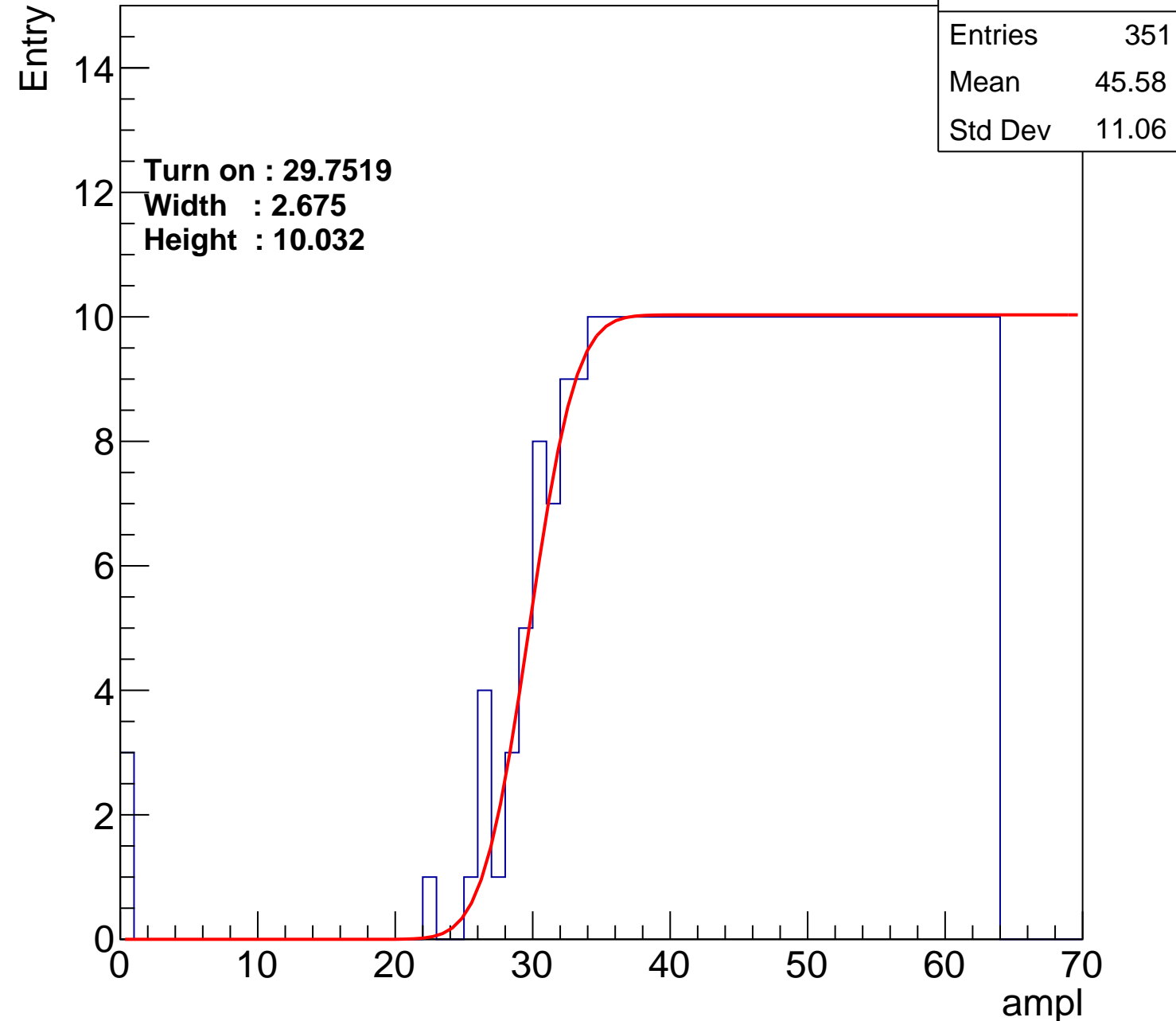
Width : 2.675

Height : 10.032

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch114

calib_packv5_042523_0143.root, FC#9, port A1

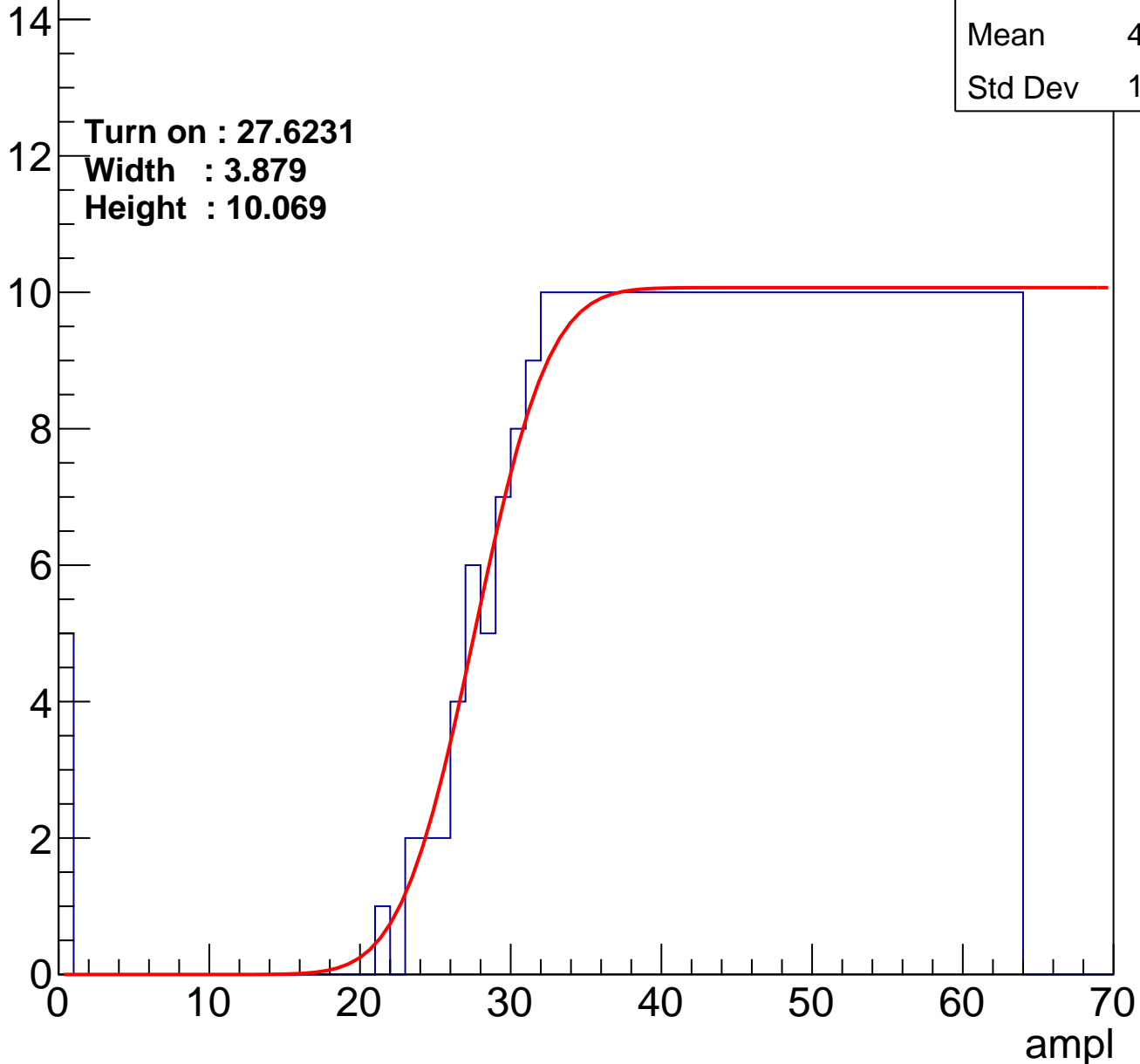
Entries	371
Mean	44.46
Std Dev	11.92

Turn on : 27.6231

Width : 3.879

Height : 10.069

Entry



B0L001S, U17-ch115

calib_packv5_042523_0143.root, FC#9, port A1

Entries	362
Mean	45.09
Std Dev	11.16

Turn on : 28.3025

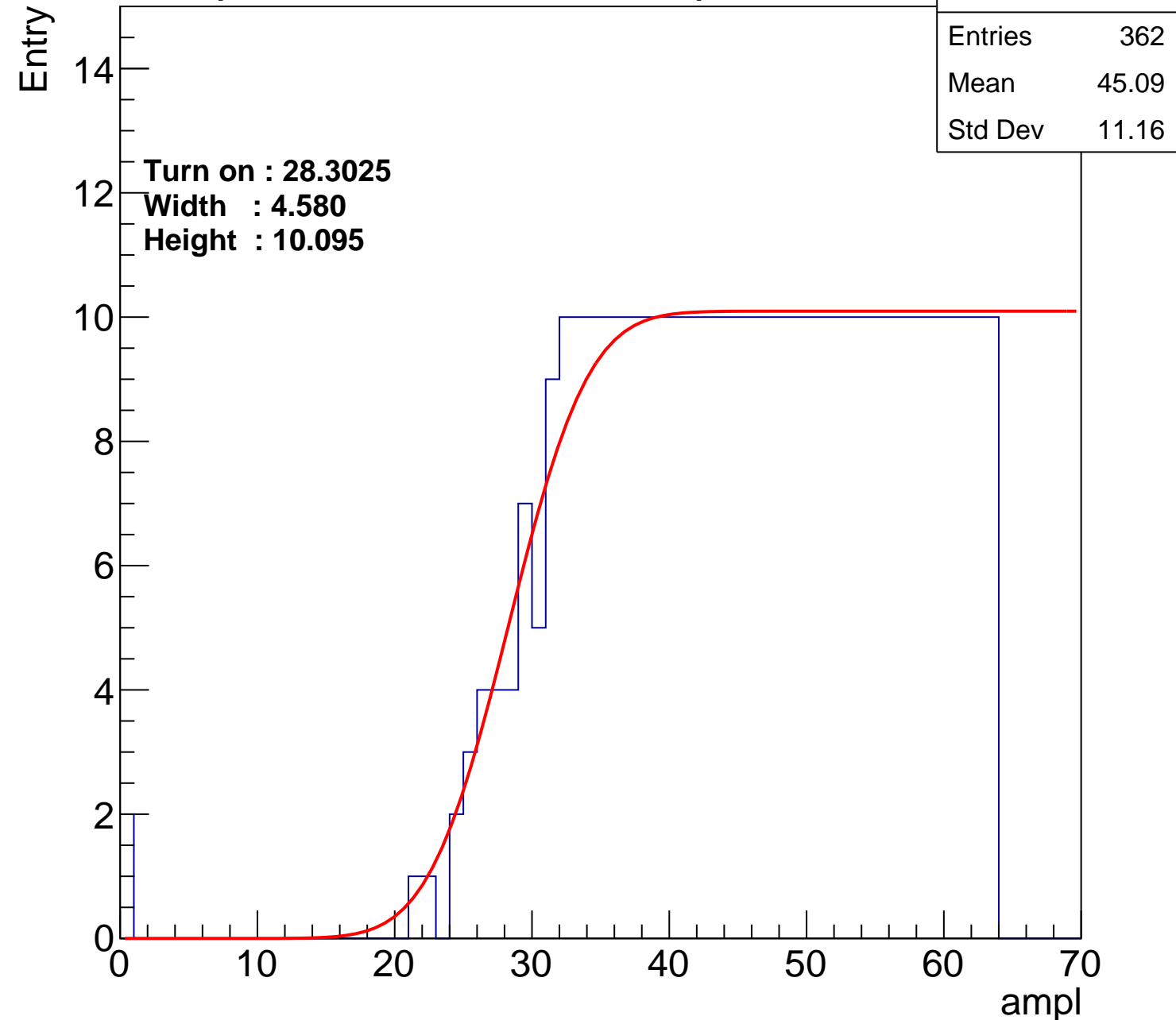
Width : 4.580

Height : 10.095

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch116

calib_packv5_042523_0143.root, FC#9, port A1

Entries	381
Mean	44.31
Std Dev	11.3

Turn on : 25.6387

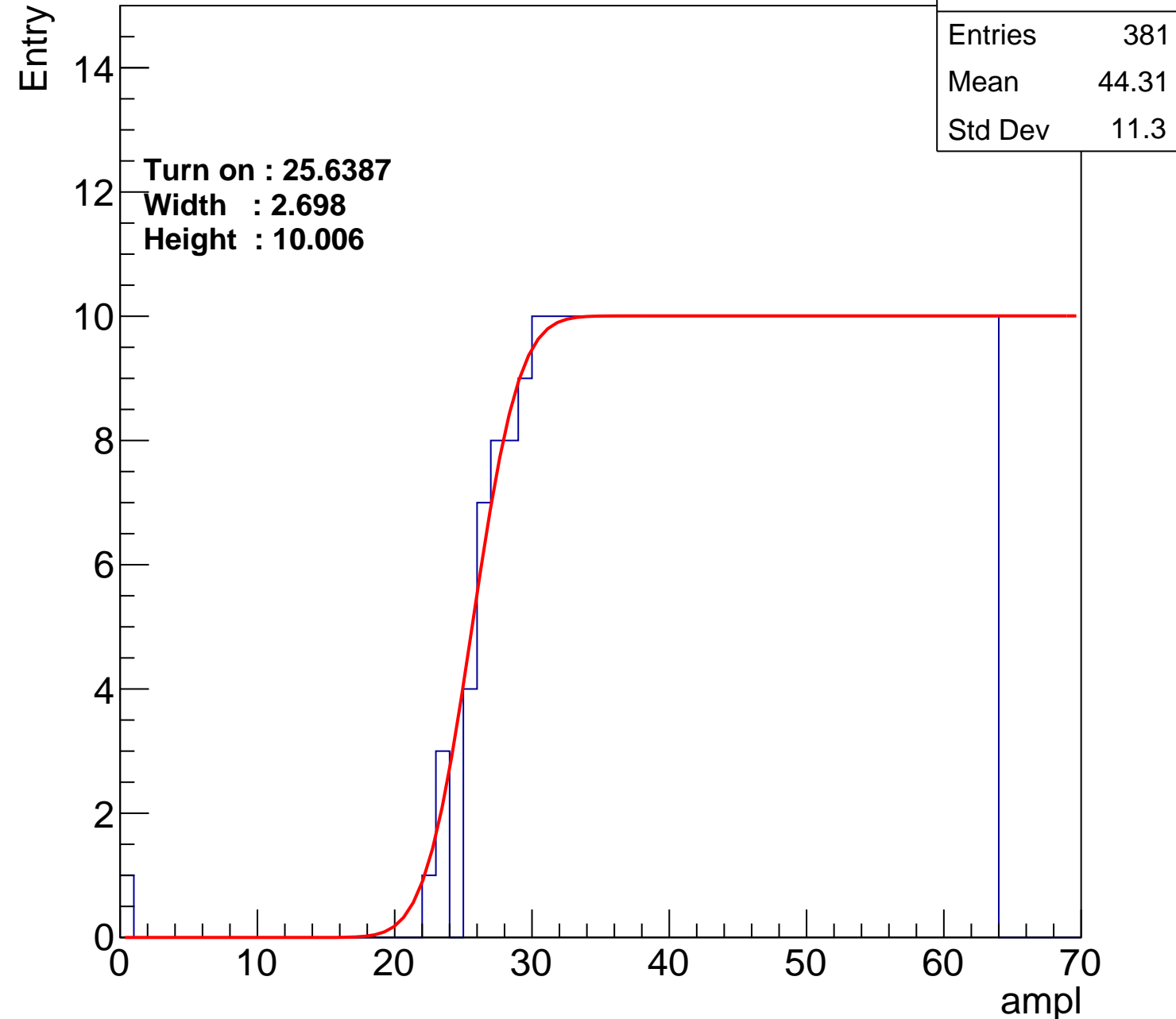
Width : 2.698

Height : 10.006

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch117

calib_packv5_042523_0143.root, FC#9, port A1

Entries	366
Mean	44.88
Std Dev	11.36

Turn on : 28.1933

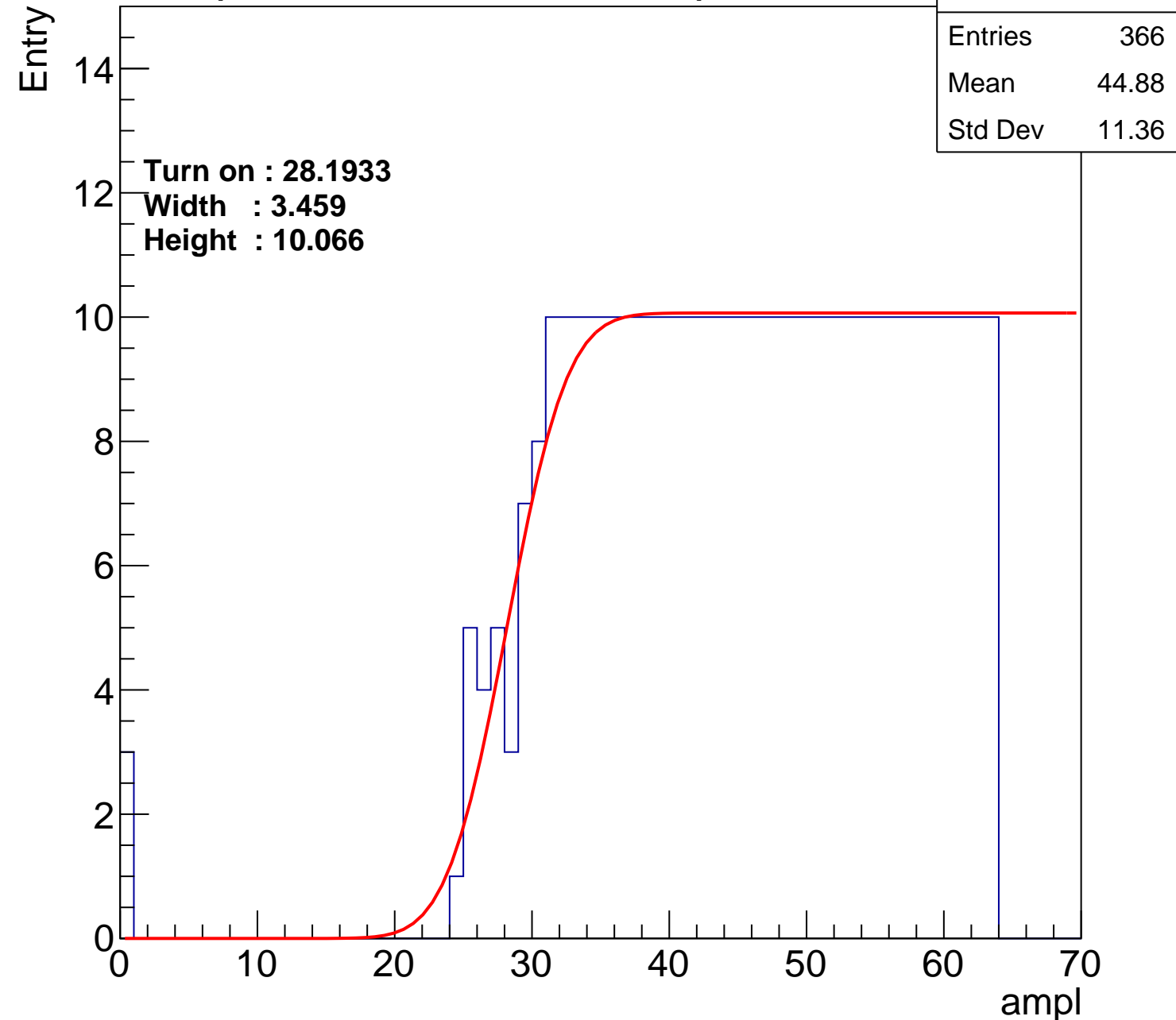
Width : 3.459

Height : 10.066

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch118

calib_packv5_042523_0143.root, FC#9, port A1

Entries	364
Mean	44.9
Std Dev	11.43

Turn on : 28.3195

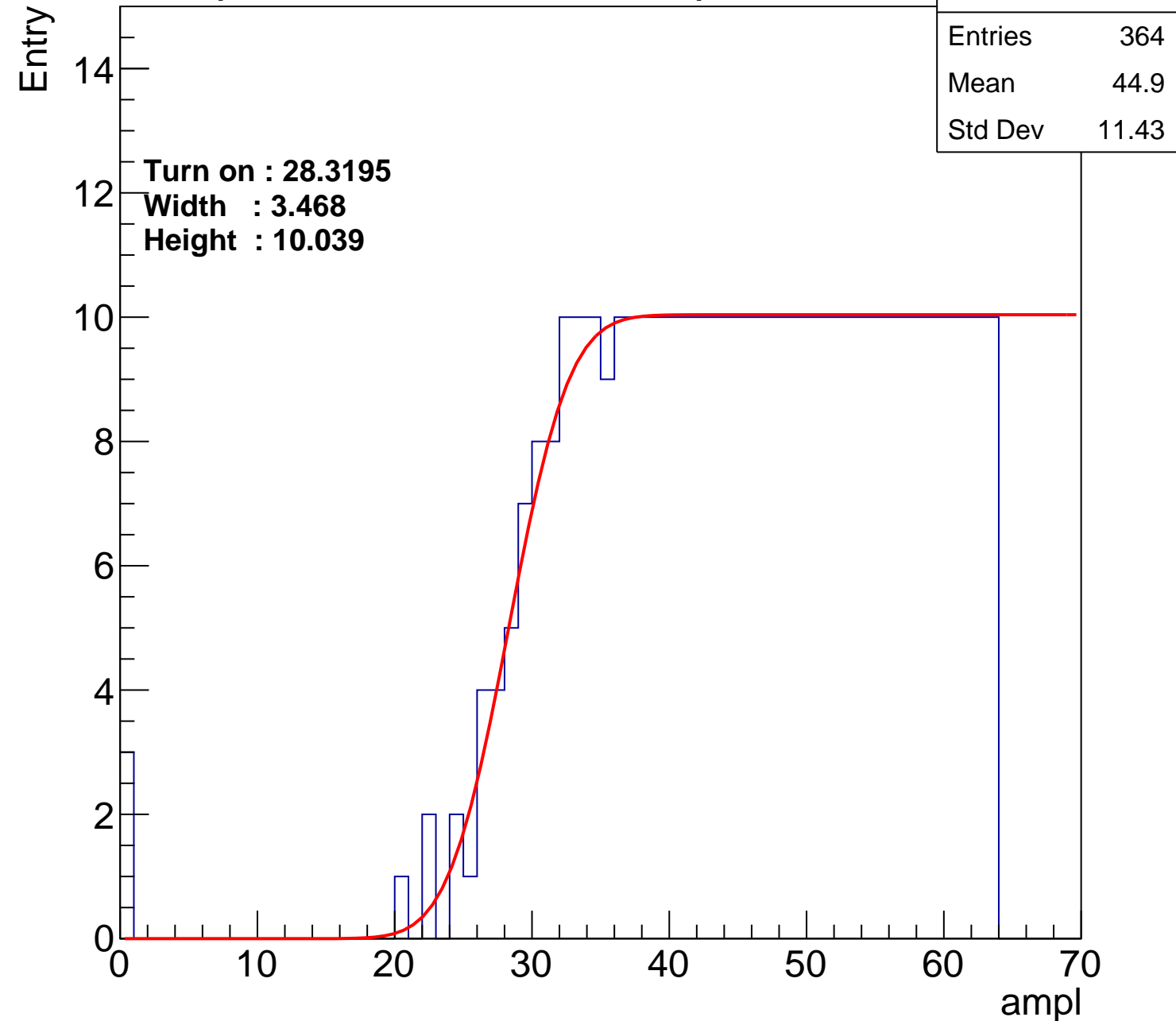
Width : 3.468

Height : 10.039

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch119

calib_packv5_042523_0143.root, FC#9, port A1

Entries	351
Mean	45.47
Std Dev	11.32

Turn on : 29.3339

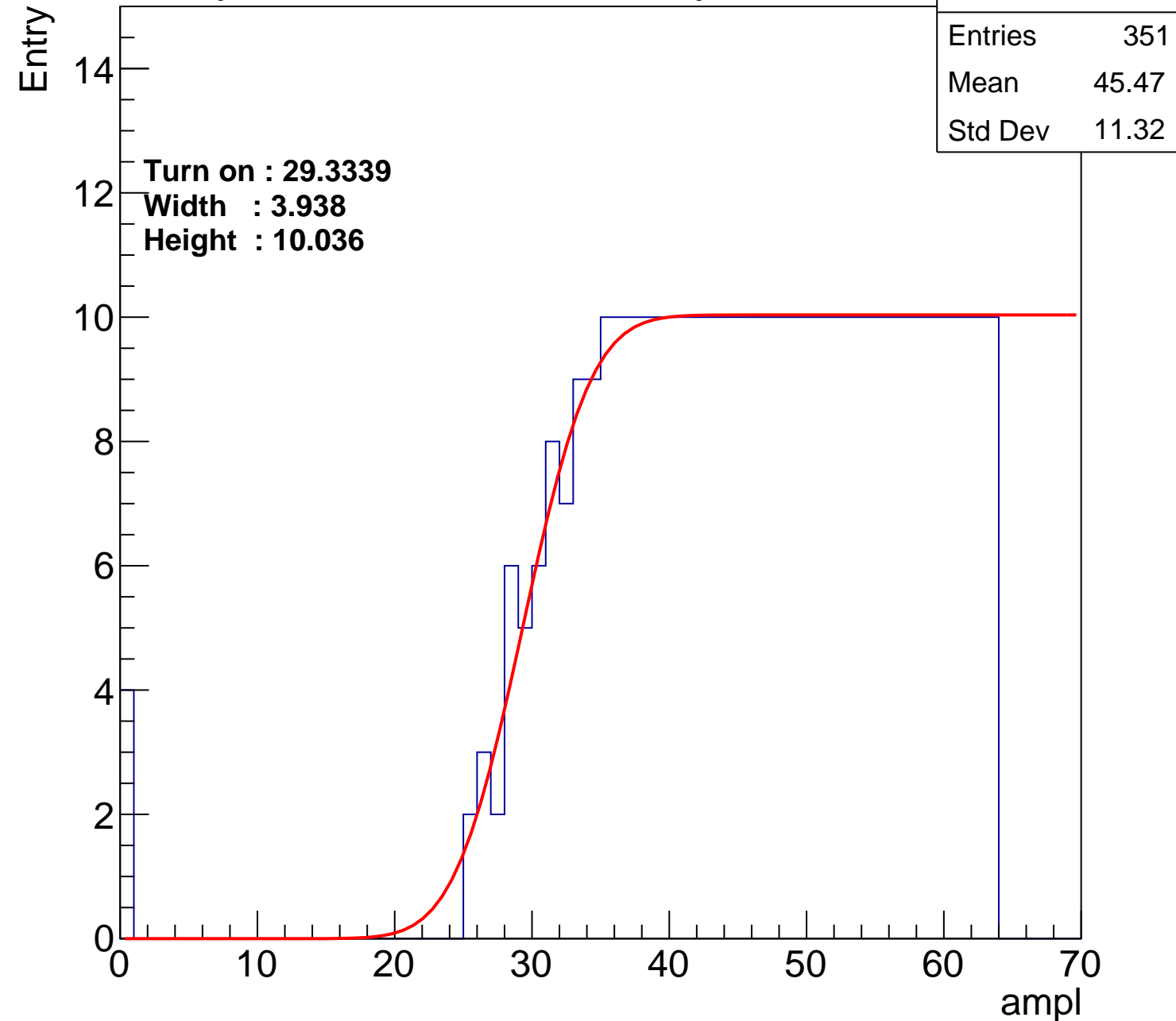
Width : 3.938

Height : 10.036

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch120

calib_packv5_042523_0143.root, FC#9, port A1

Entries	389
Mean	43.52
Std Dev	12.47

Turn on : 25.8905

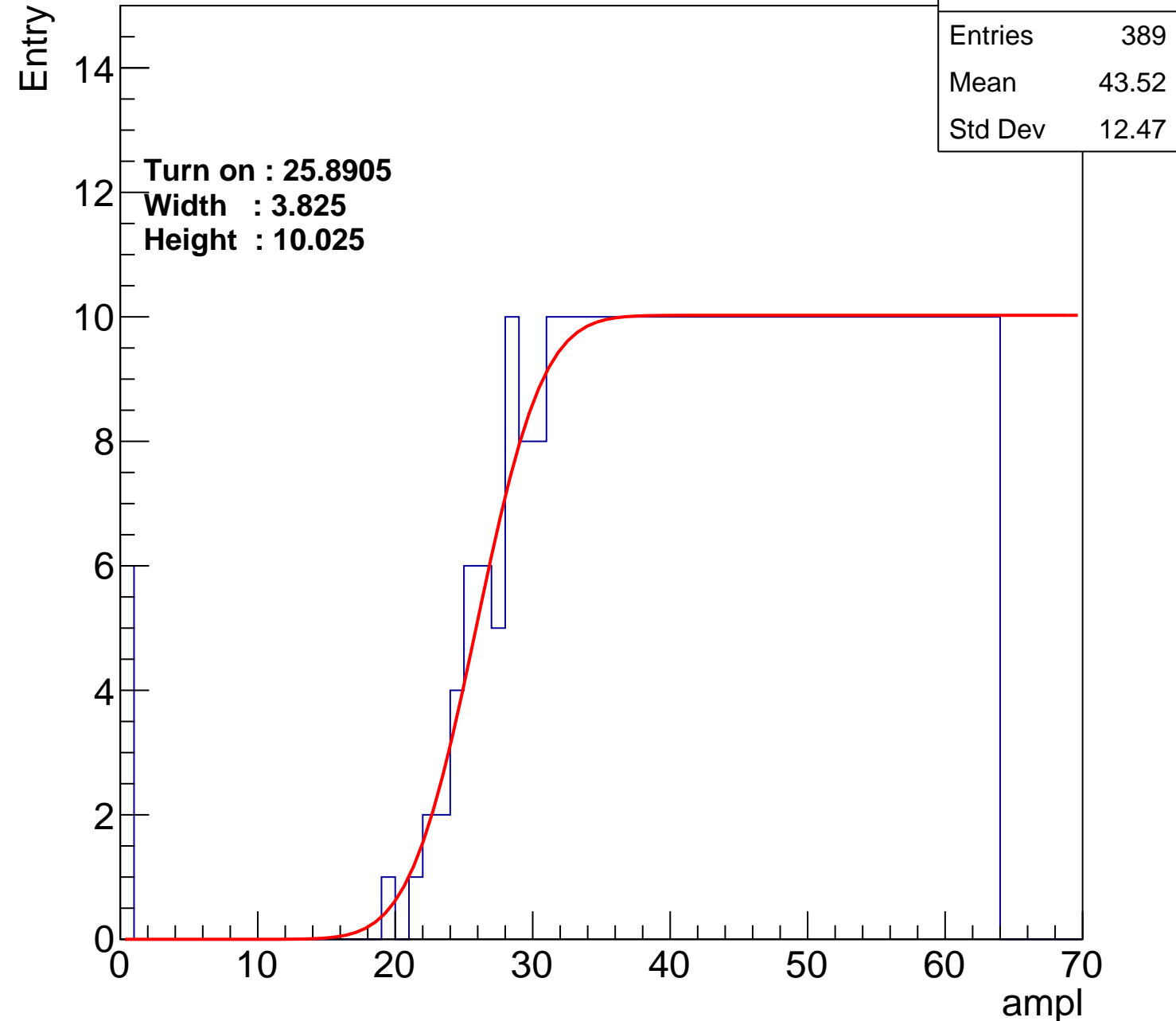
Width : 3.825

Height : 10.025

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch121

calib_packv5_042523_0143.root, FC#9, port A1

Entries	372
Mean	44.36
Std Dev	12.01

Turn on : 27.8223

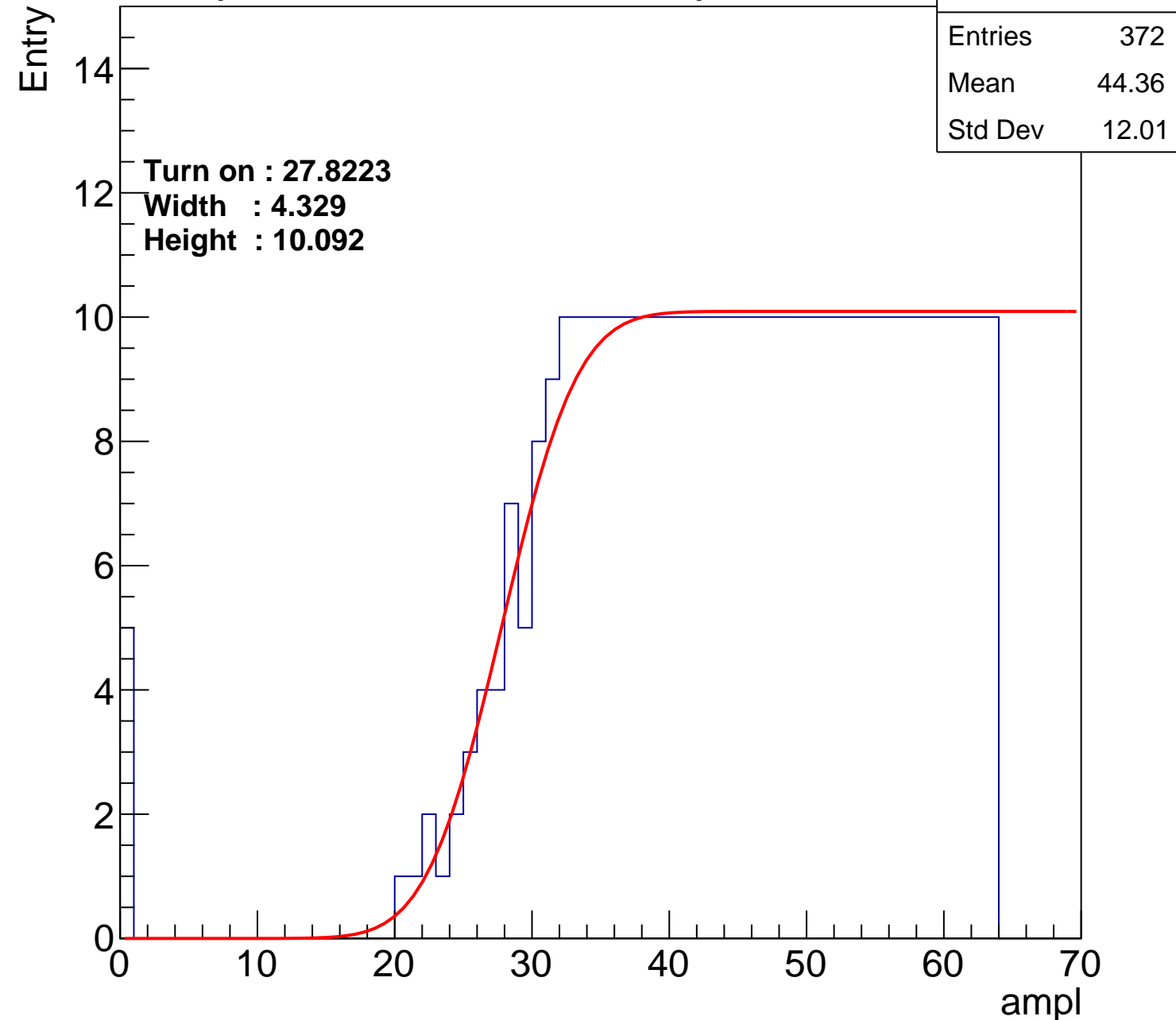
Width : 4.329

Height : 10.092

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch122

calib_packv5_042523_0143.root, FC#9, port A1

Entries	367
Mean	44.73
Std Dev	11.63

Turn on : 27.9797

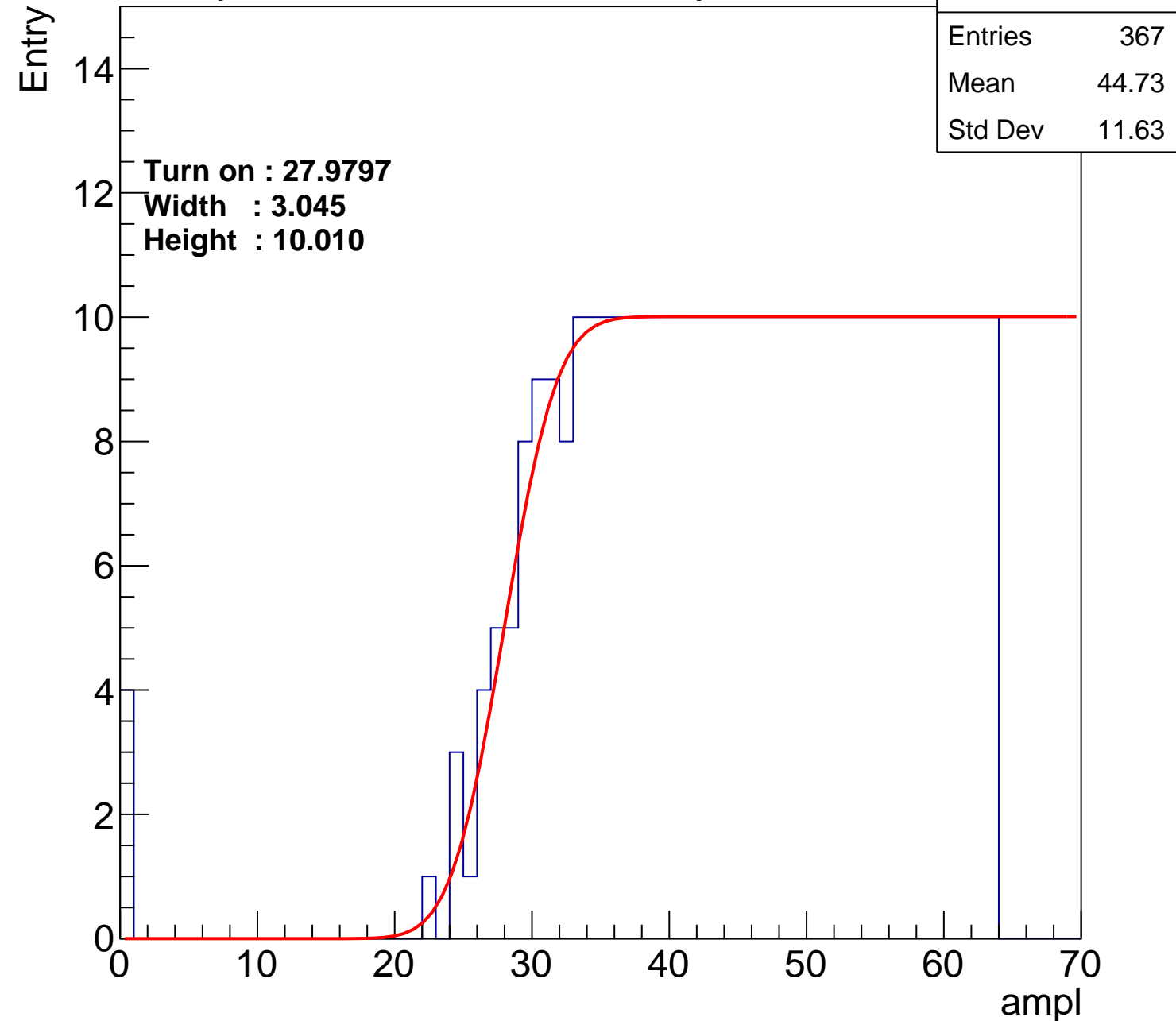
Width : 3.045

Height : 10.010

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch123

calib_packv5_042523_0143.root, FC#9, port A1

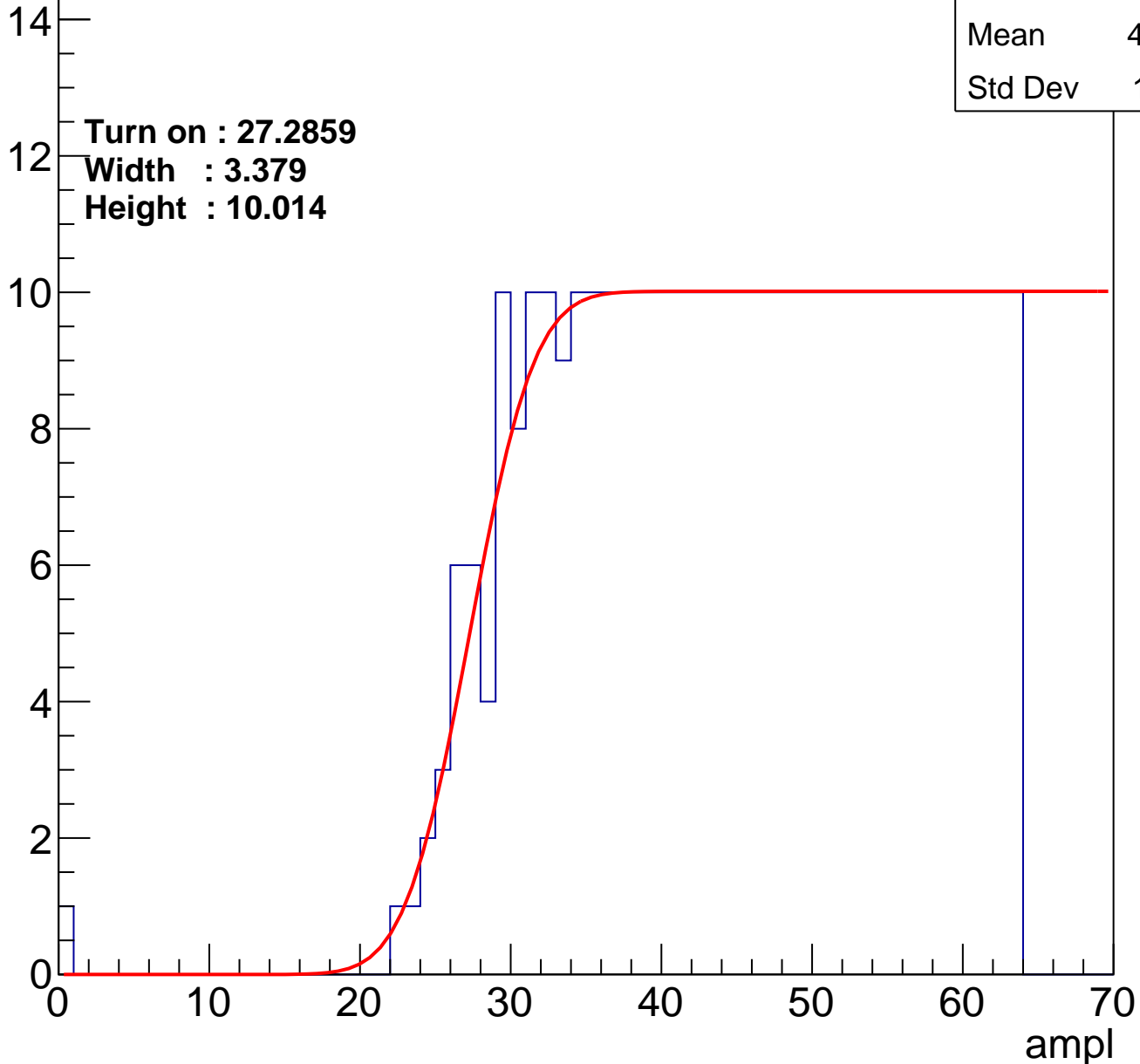
Entries	371
Mean	44.76
Std Dev	11.11

Turn on : 27.2859

Width : 3.379

Height : 10.014

Entry



B0L001S, U17-ch124

calib_packv5_042523_0143.root, FC#9, port A1

Entries	351
Mean	45.54
Std Dev	11.12

Turn on : 29.7715

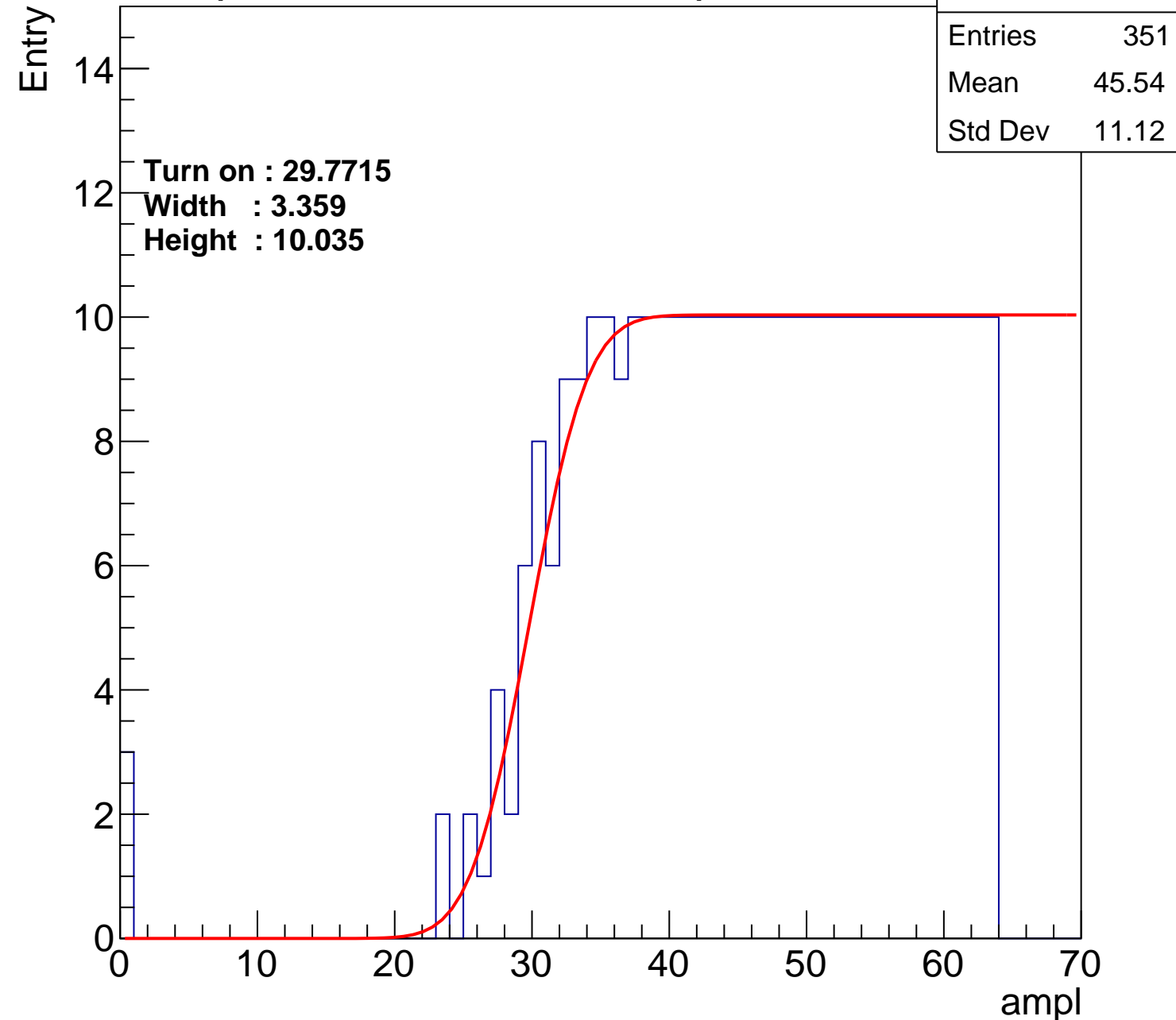
Width : 3.359

Height : 10.035

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch125

calib_packv5_042523_0143.root, FC#9, port A1

Entries	385
Mean	43.9
Std Dev	11.97

Turn on : 25.9811

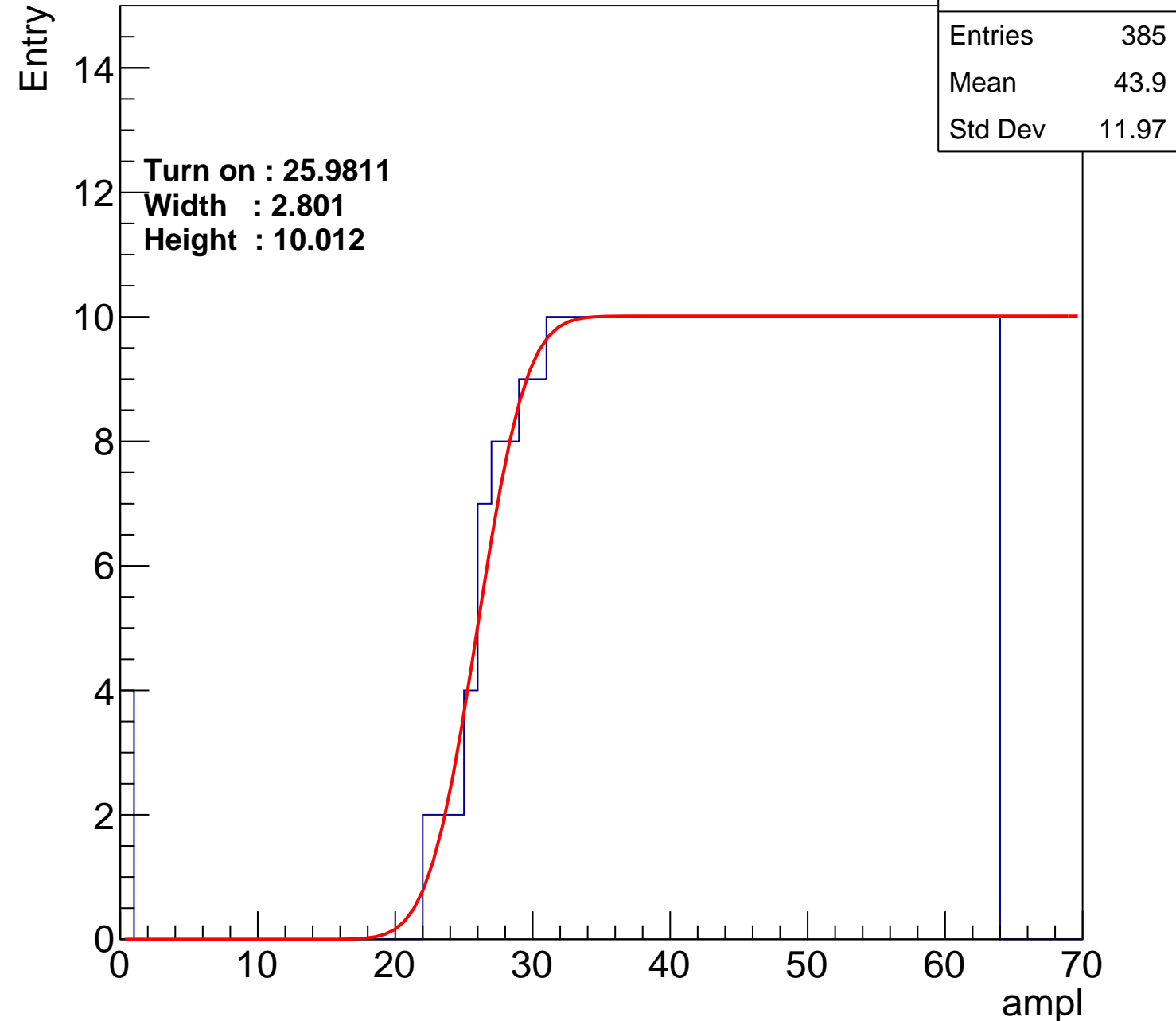
Width : 2.801

Height : 10.012

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch126

calib_packv5_042523_0143.root, FC#9, port A1

Entries	382
Mean	44.1
Std Dev	11.74

Turn on : 26.4688

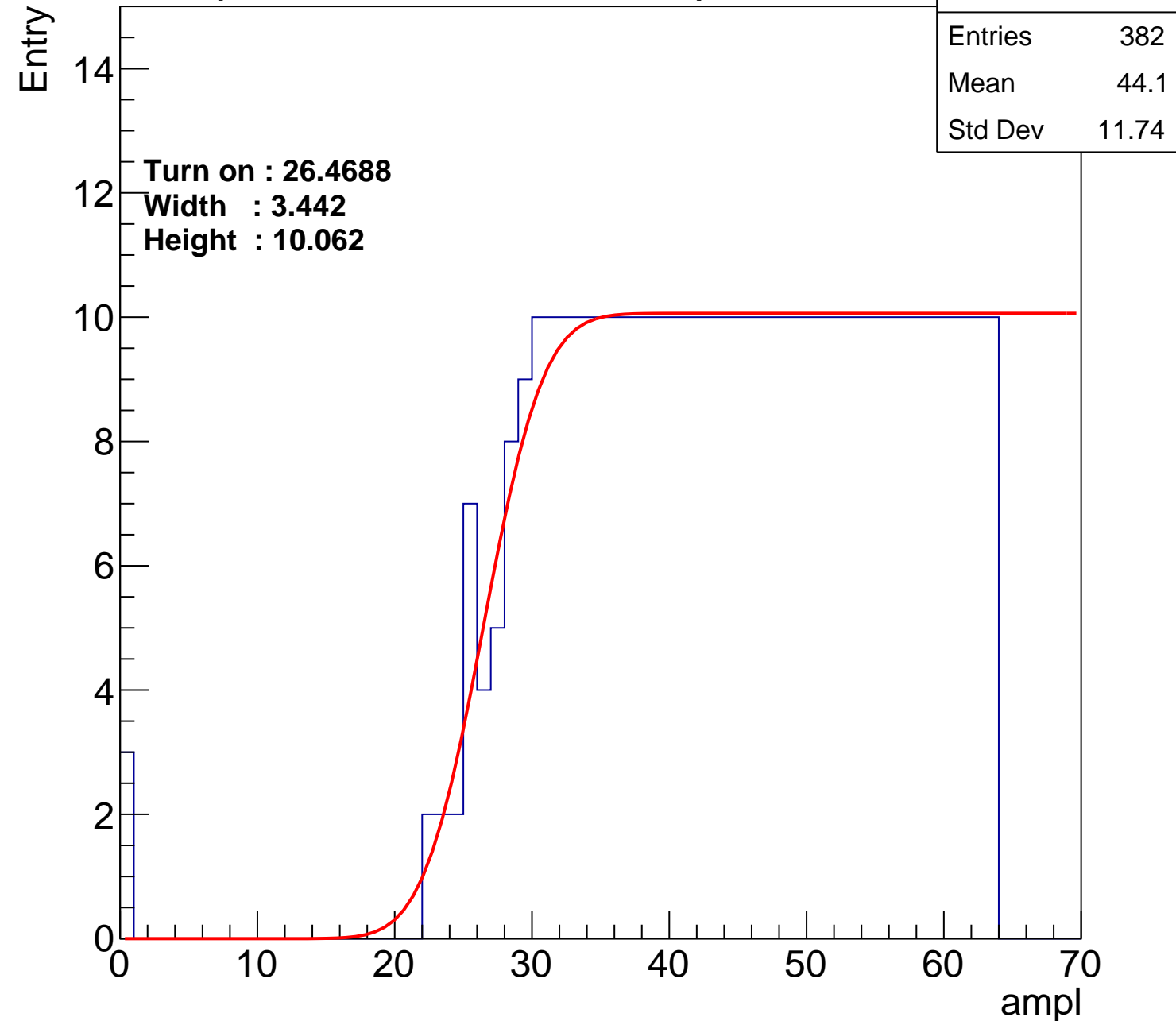
Width : 3.442

Height : 10.062

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch127

calib_packv5_042523_0143.root, FC#9, port A1

Entries	360
Mean	45.19
Std Dev	11.19

Turn on : 28.2871

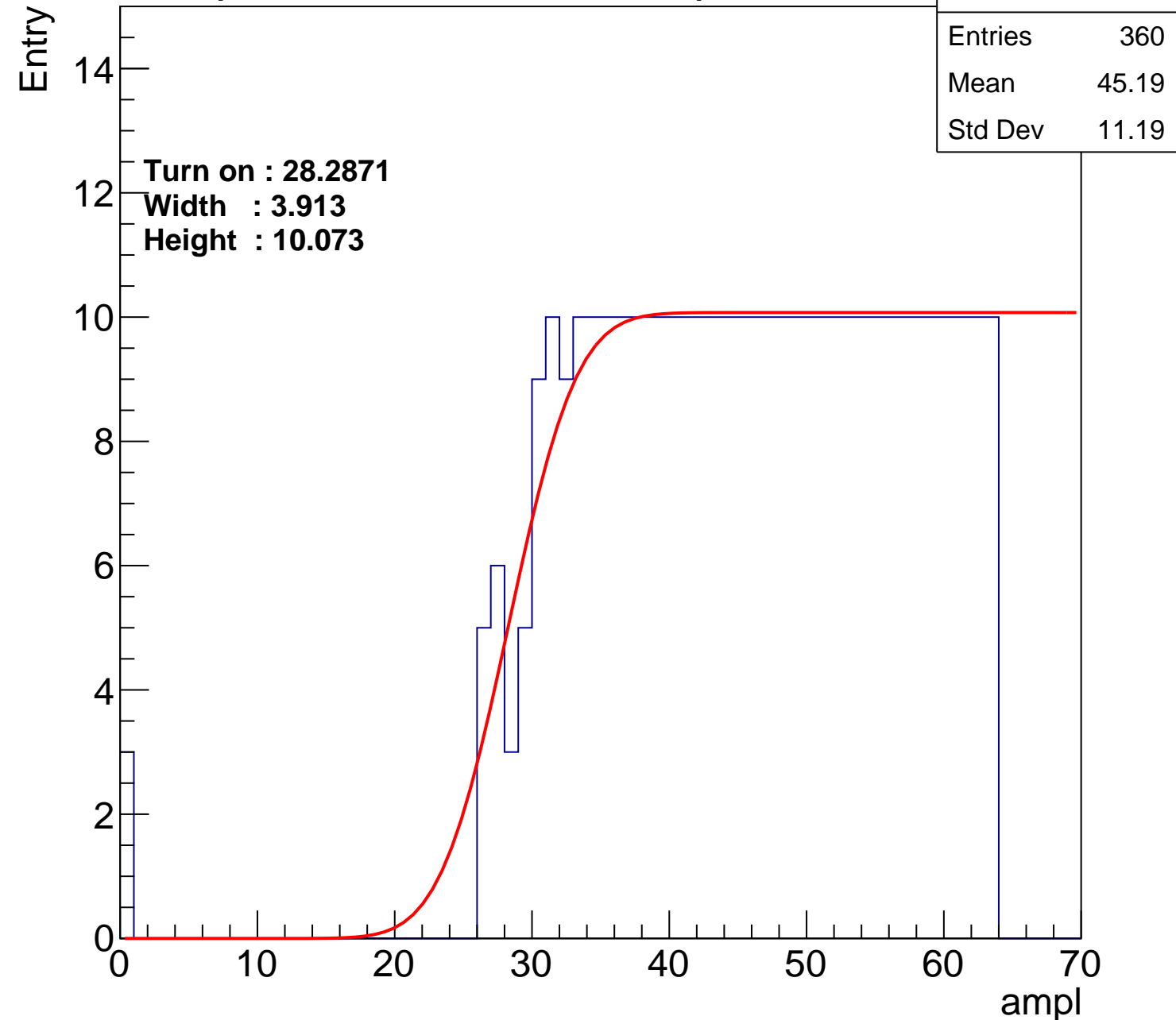
Width : 3.913

Height : 10.073

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U17-ch127

calib_packv5_042523_0143.root, FC#9, port A1

Entries	360
Mean	45.19
Std Dev	11.19

Turn on : 28.2871

Width : 3.913

Height : 10.073

Entry

14
12
10
8
6
4
2
0

ampl

