



# B1L103S, U2-ch0, adc0

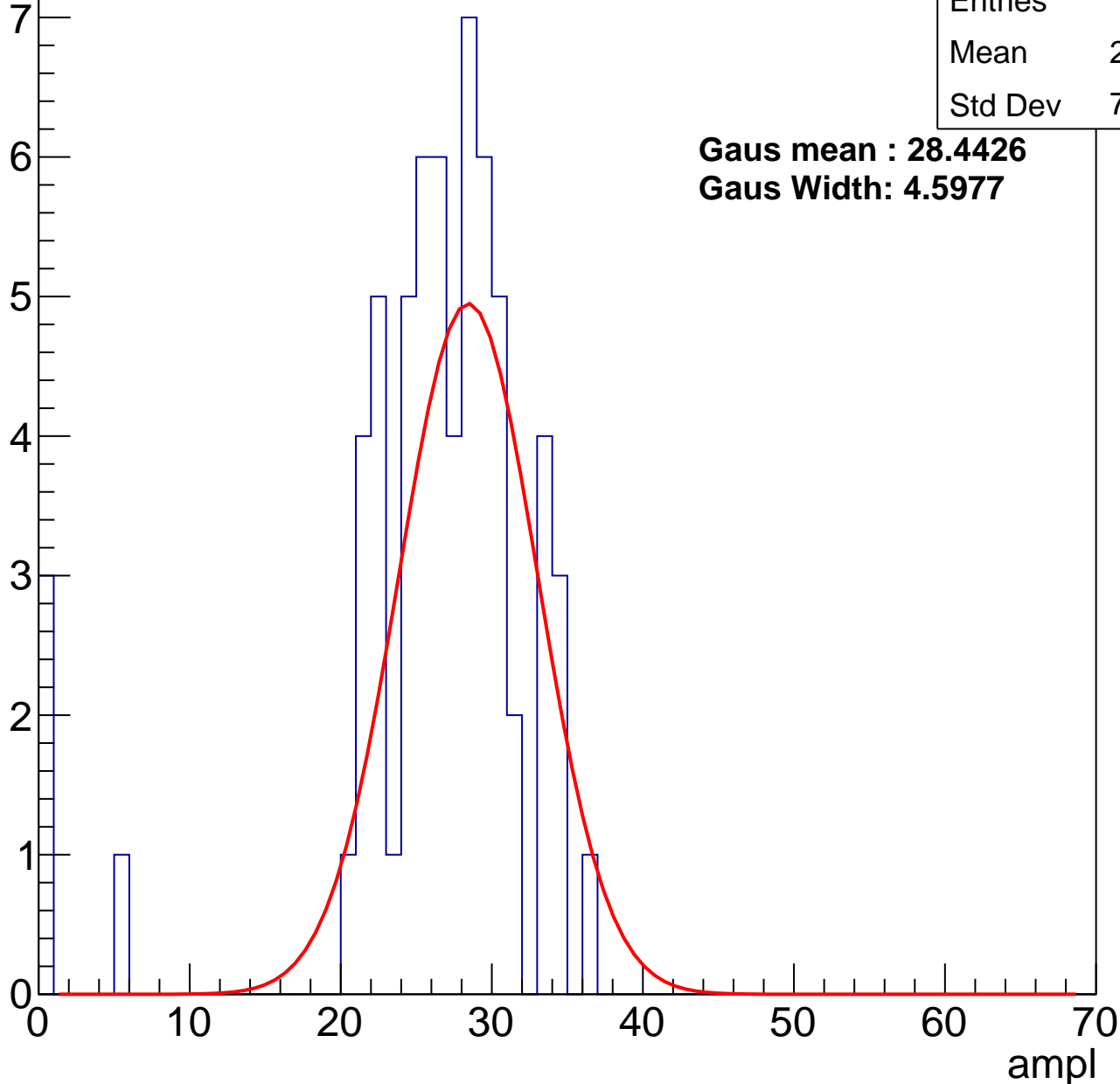
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	25.44
Std Dev	7.293

**Gaus mean : 28.4426**

**Gaus Width: 4.5977**



# B1L103S, U2-ch0, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	80
Mean	32.67
Std Dev	5.164

**Gaus mean : 33.7320**

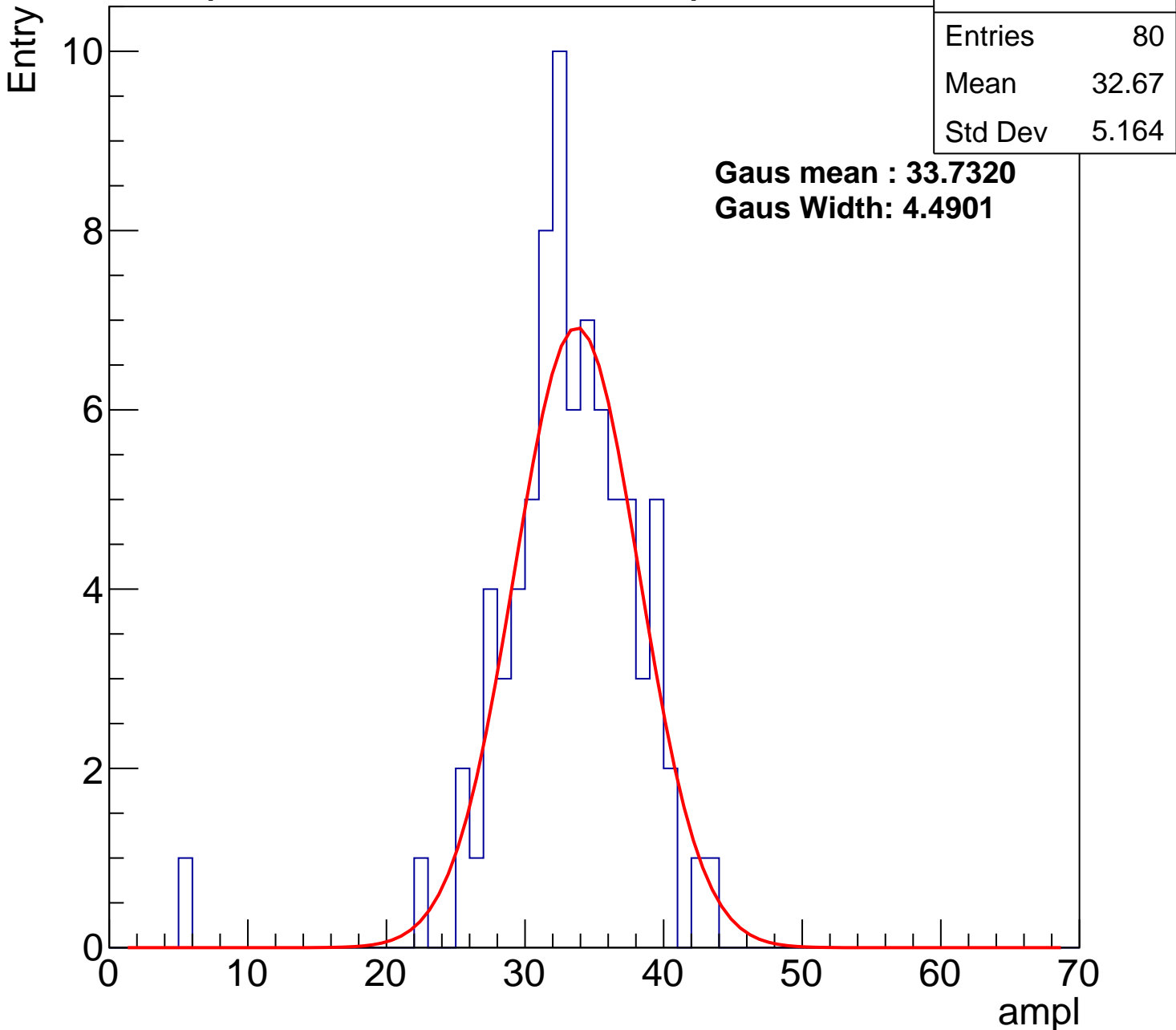
**Gaus Width: 4.4901**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U2-ch0, adc2

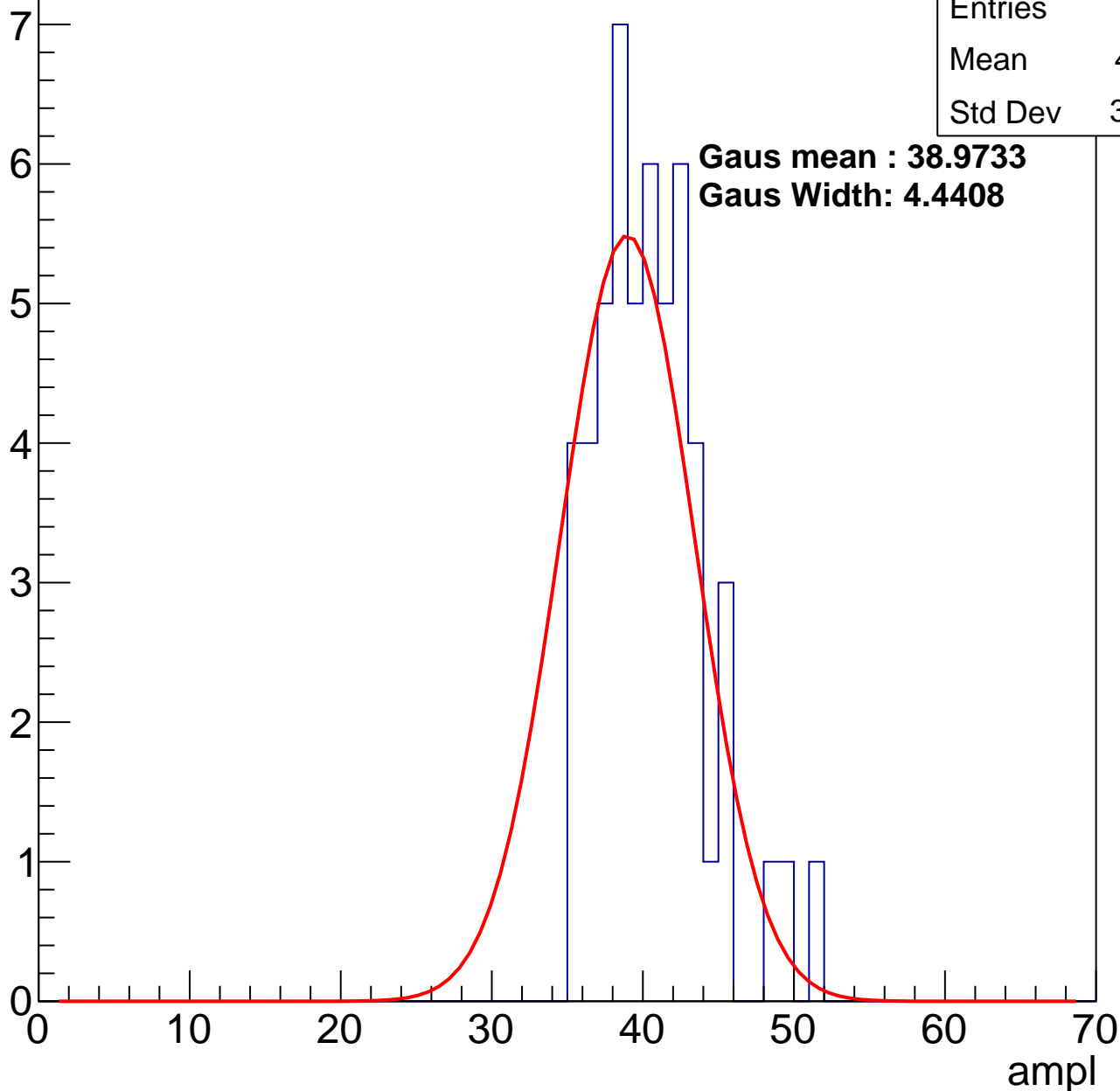
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	40.11
Std Dev	3.538

**Gaus mean : 38.9733**

**Gaus Width: 4.4408**

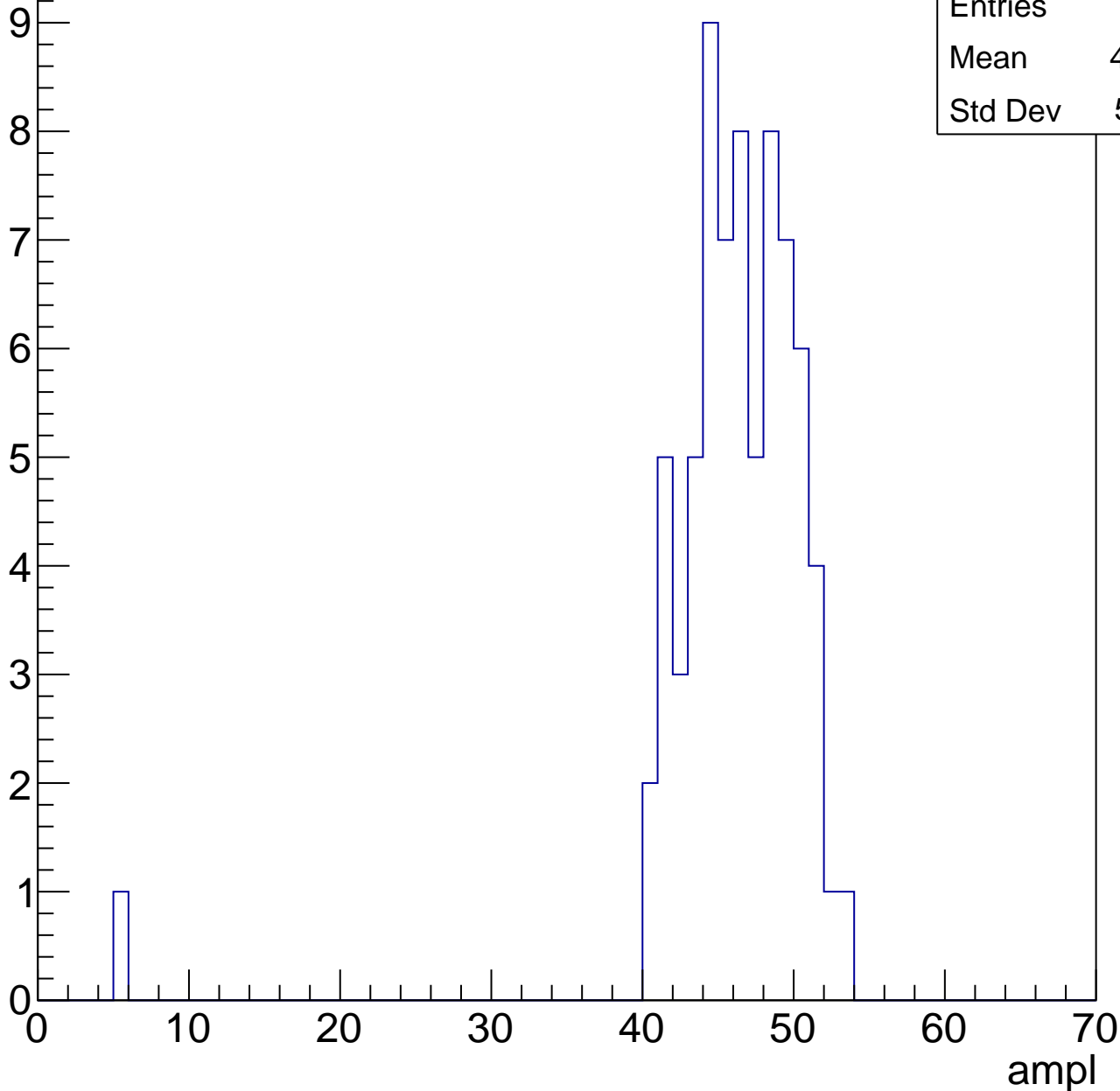


# B1L103S, U2-ch0, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	45.57
Std Dev	5.751

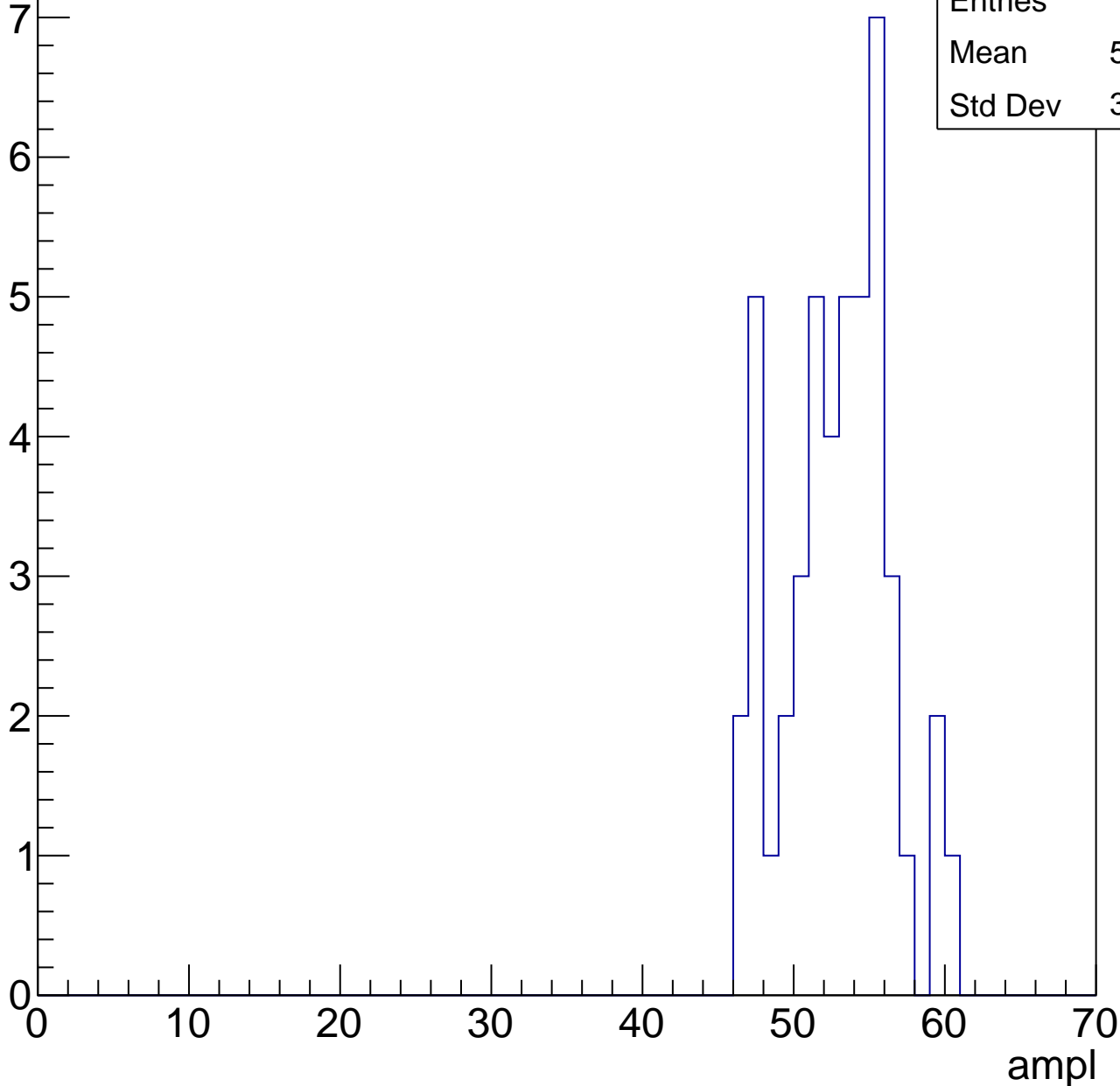


# B1L103S, U2-ch0, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	46
Mean	52.37
Std Dev	3.504

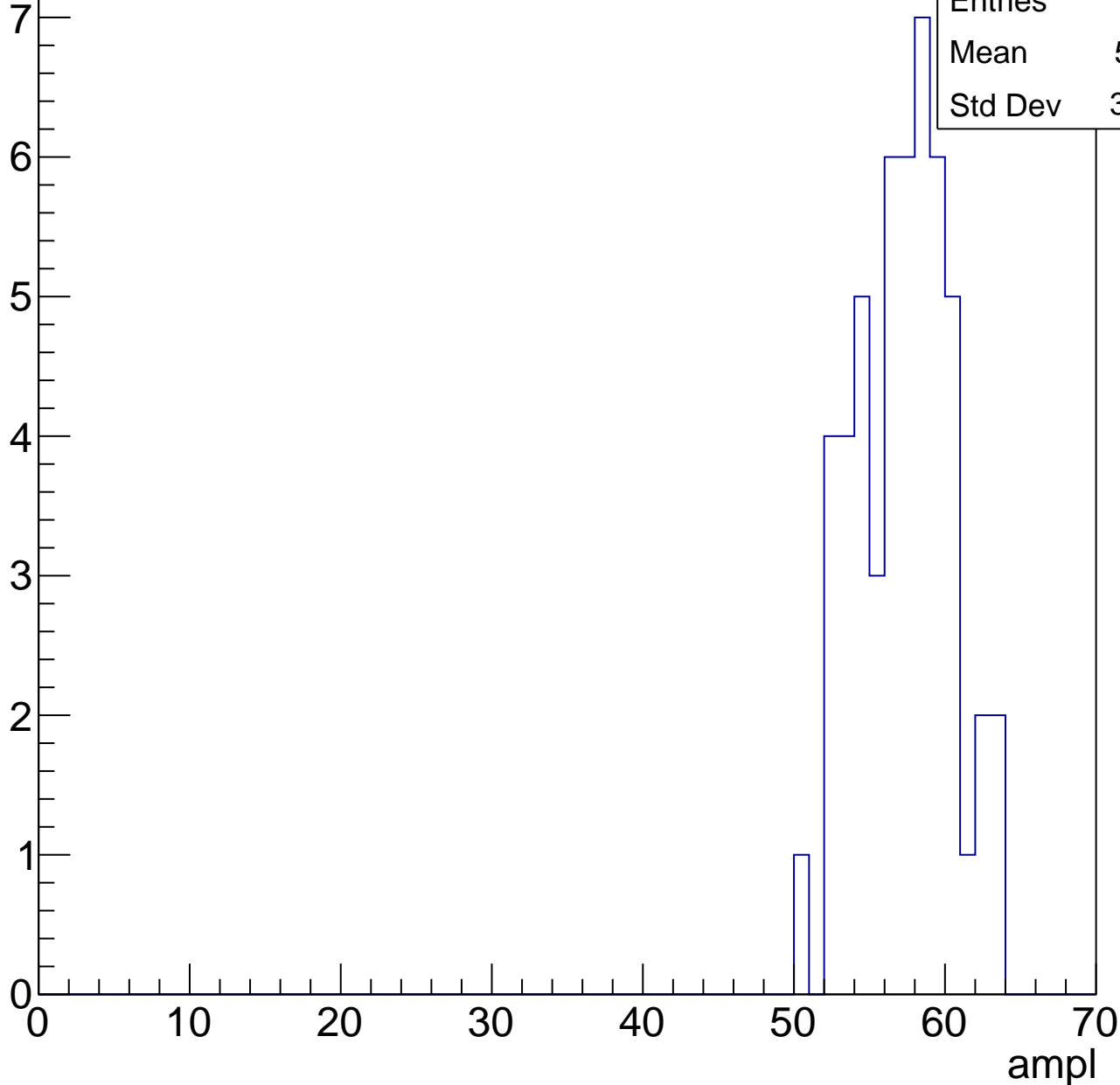


# B1L103S, U2-ch0, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	56.81
Std Dev	3.064

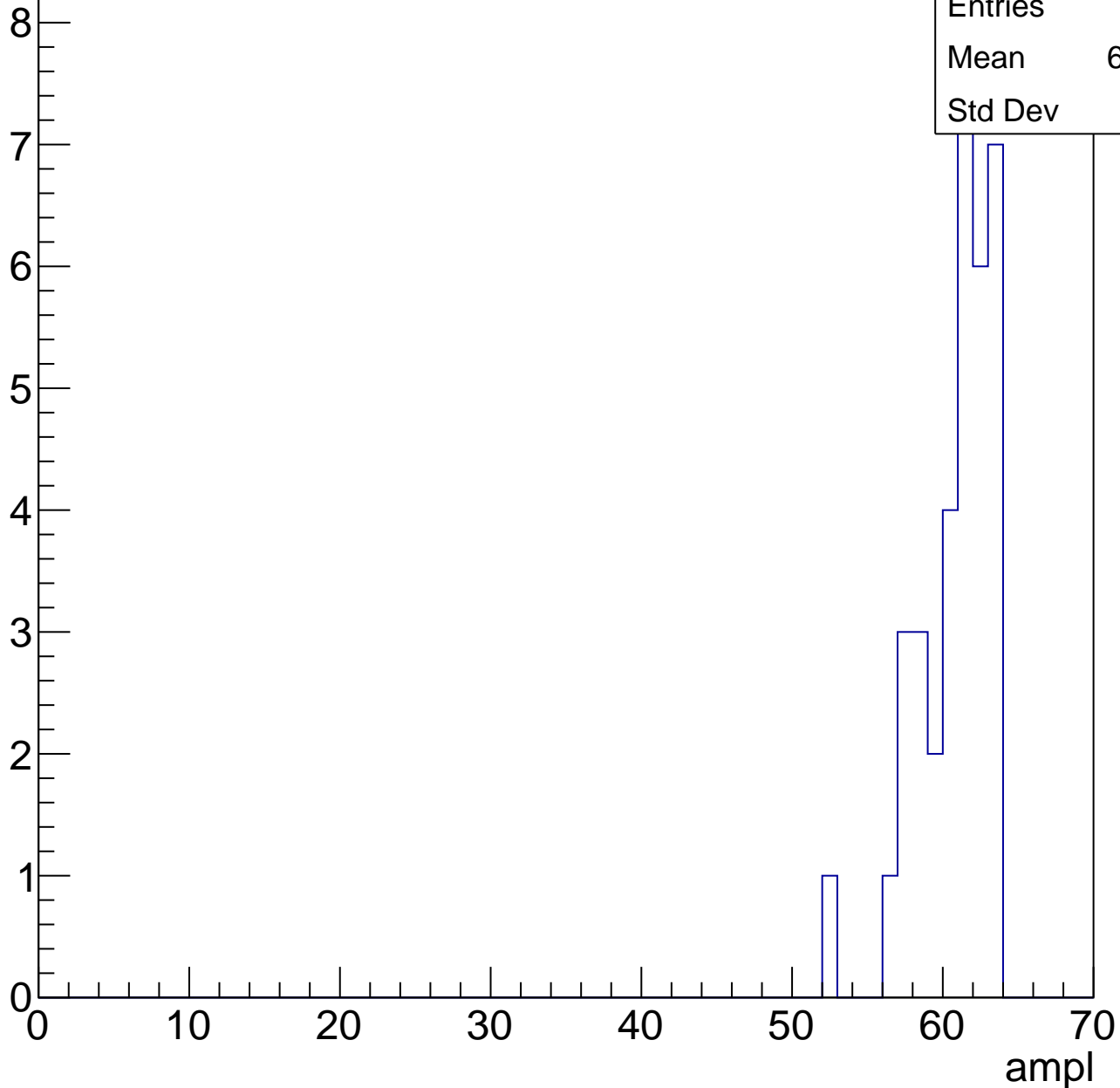


# B1L103S, U2-ch0, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	35
Mean	60.34
Std Dev	2.46

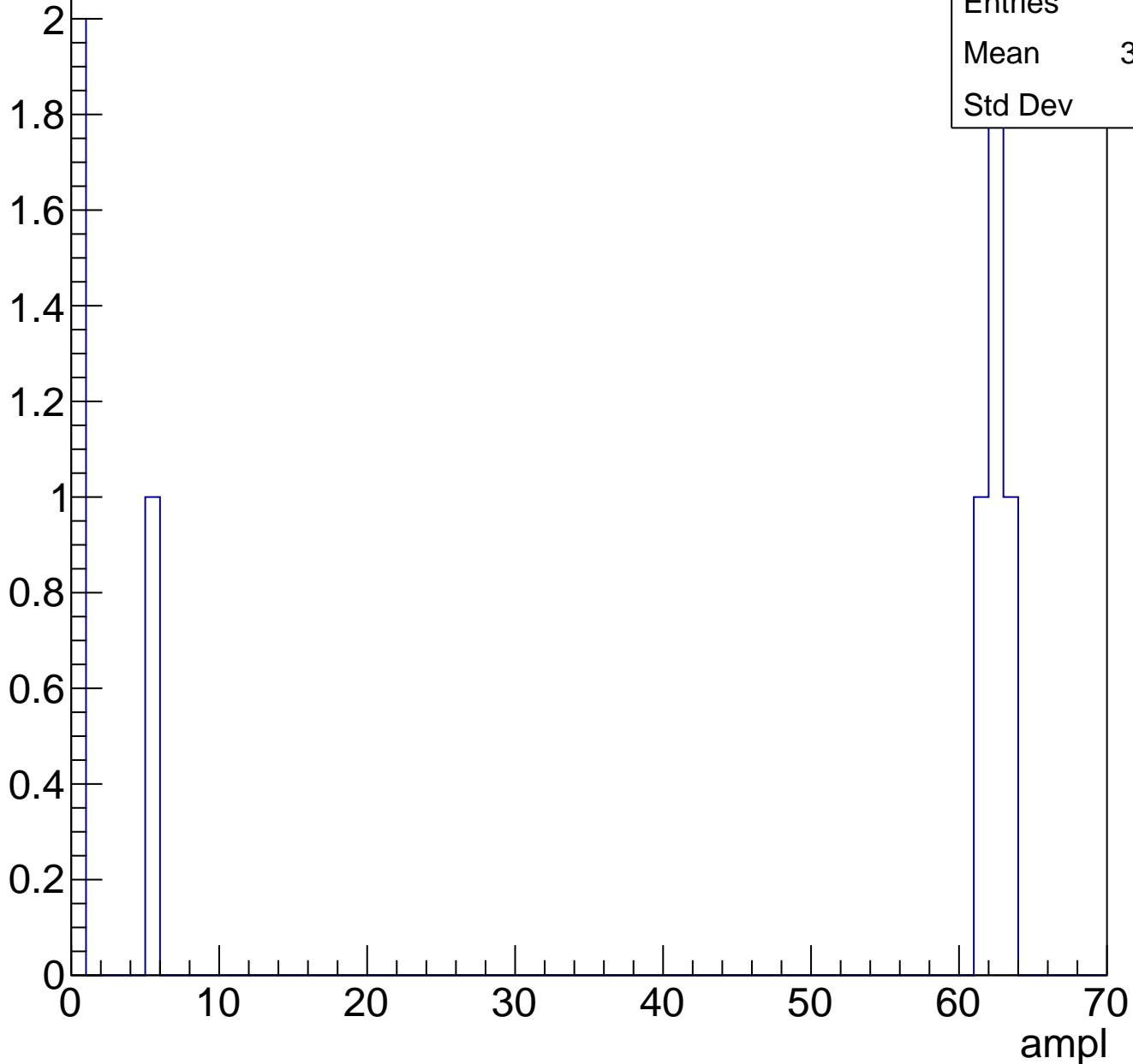




# B1L103S, U2-ch0, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	7
Mean	36.14
Std Dev	29.9

# B1L103S, U2-ch1, adc0

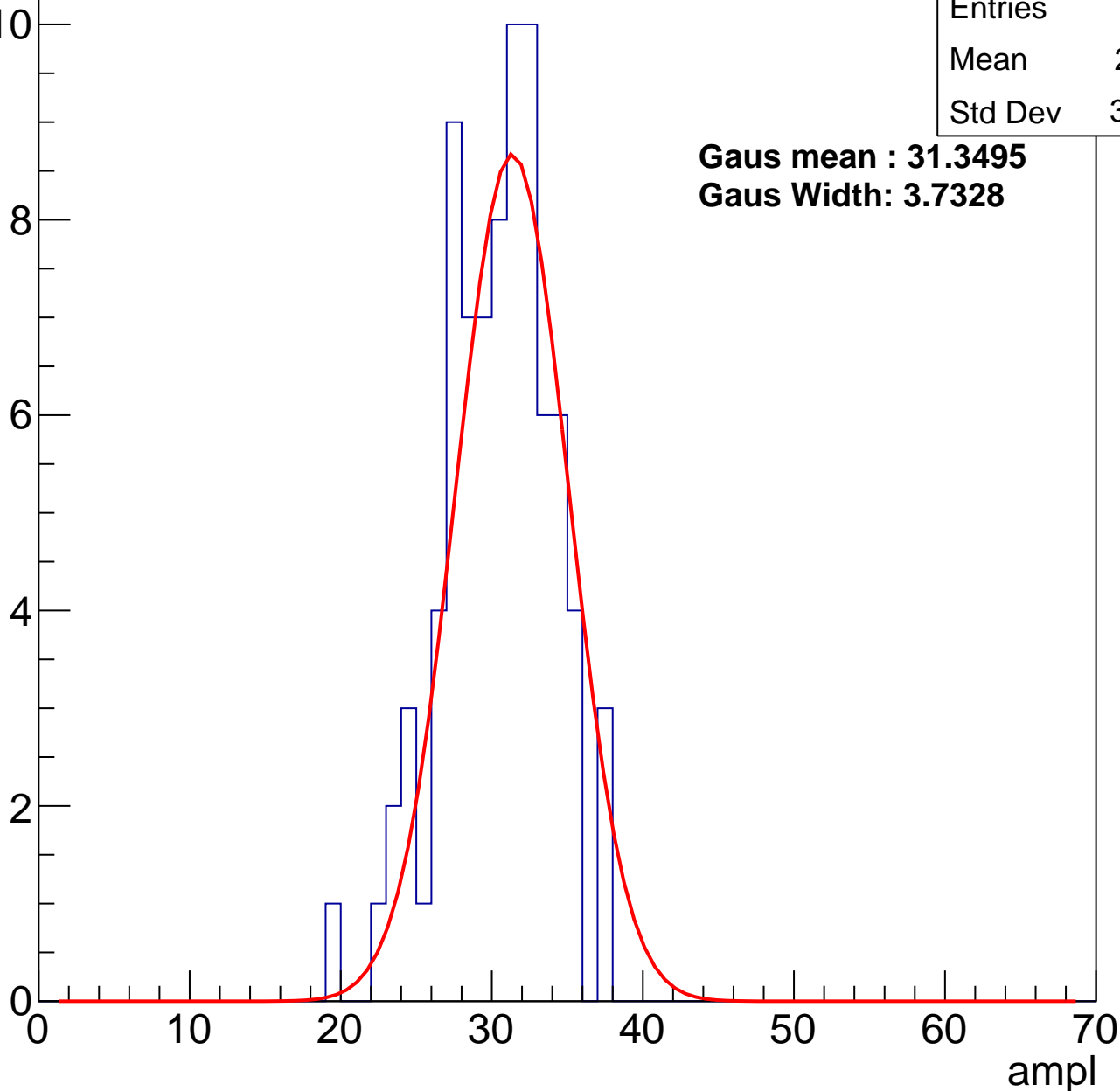
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	82
Mean	29.91
Std Dev	3.565

**Gaus mean : 31.3495**

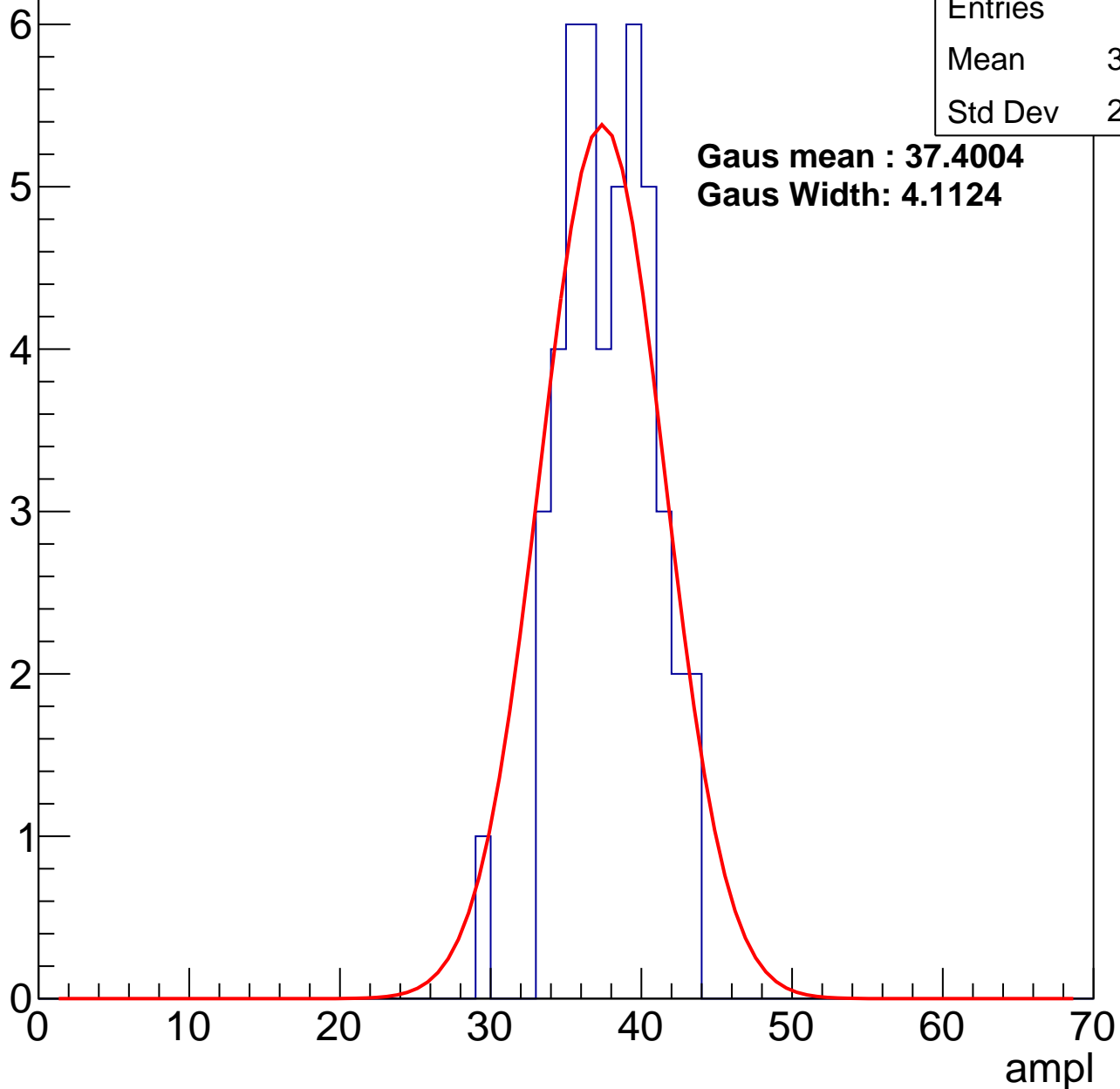
**Gaus Width: 3.7328**



# B1L103S, U2-ch1, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch1, adc2

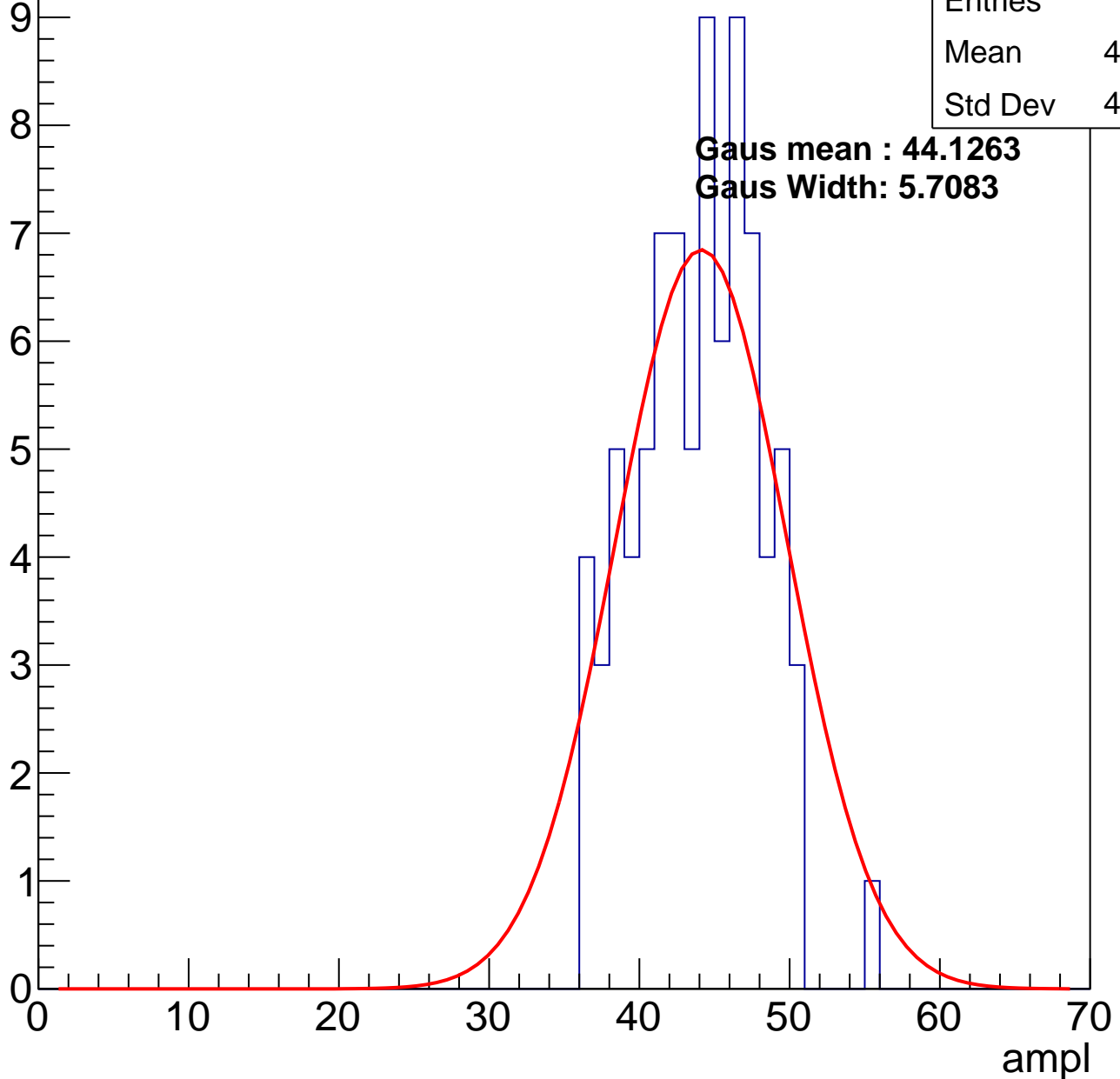
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	84
Mean	43.43
Std Dev	4.016

**Gaus mean : 44.1263**

**Gaus Width: 5.7083**

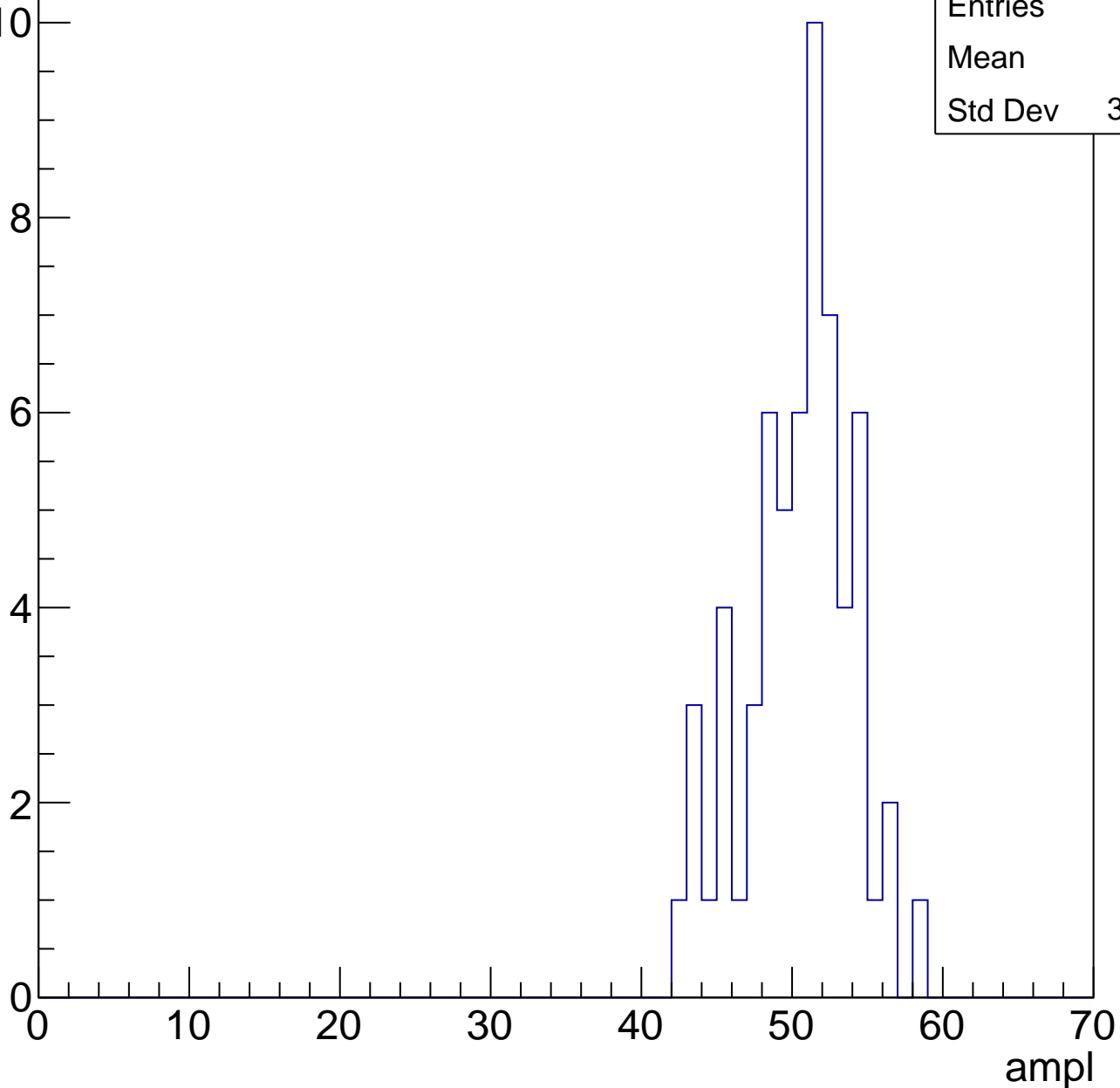


# B1L103S, U2-ch1, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	50
Std Dev	3.506



# B1L103S, U2-ch1, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

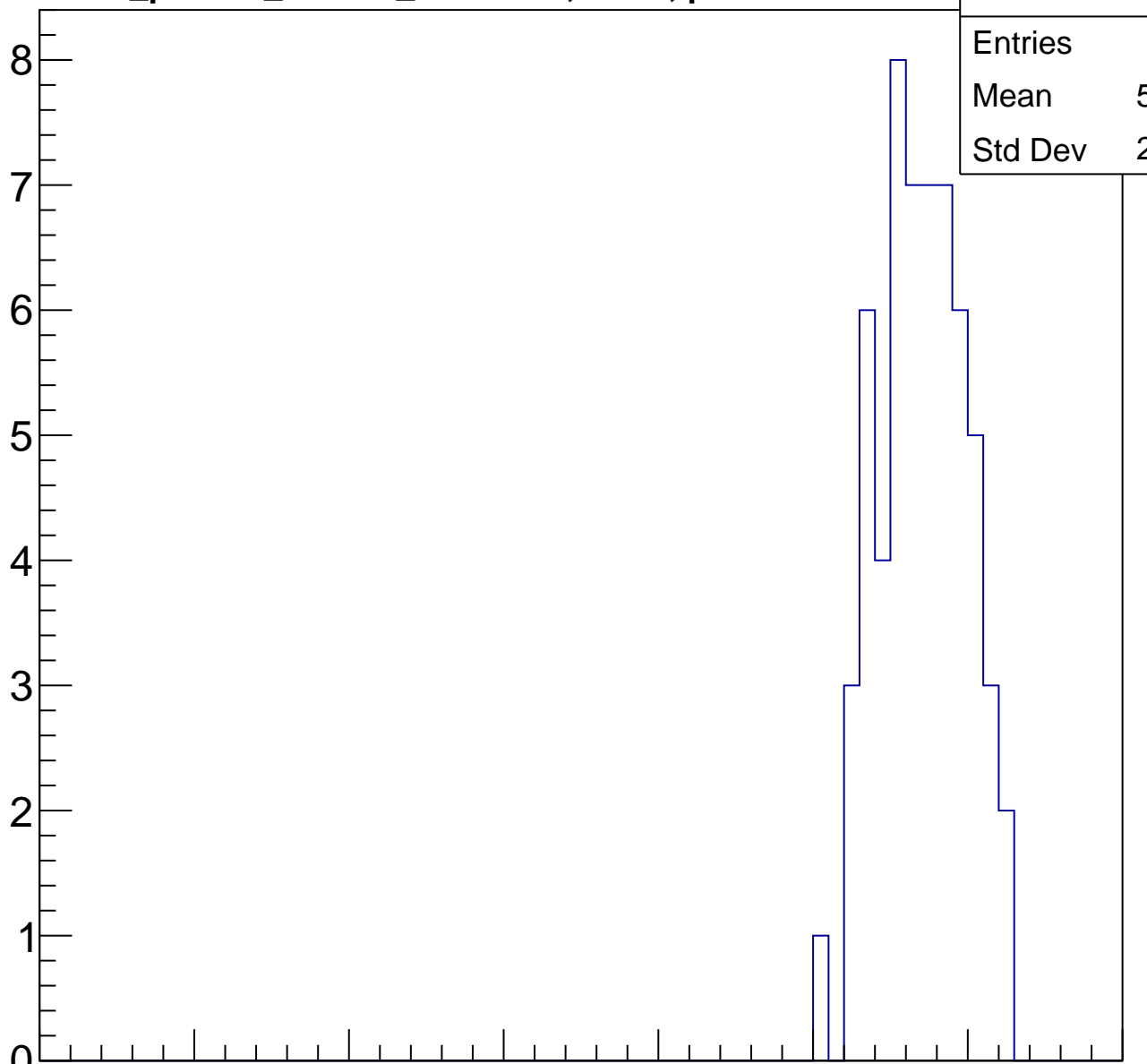
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	59
Mean	56.58
Std Dev	2.787

ampl

0 10 20 30 40 50 60 70

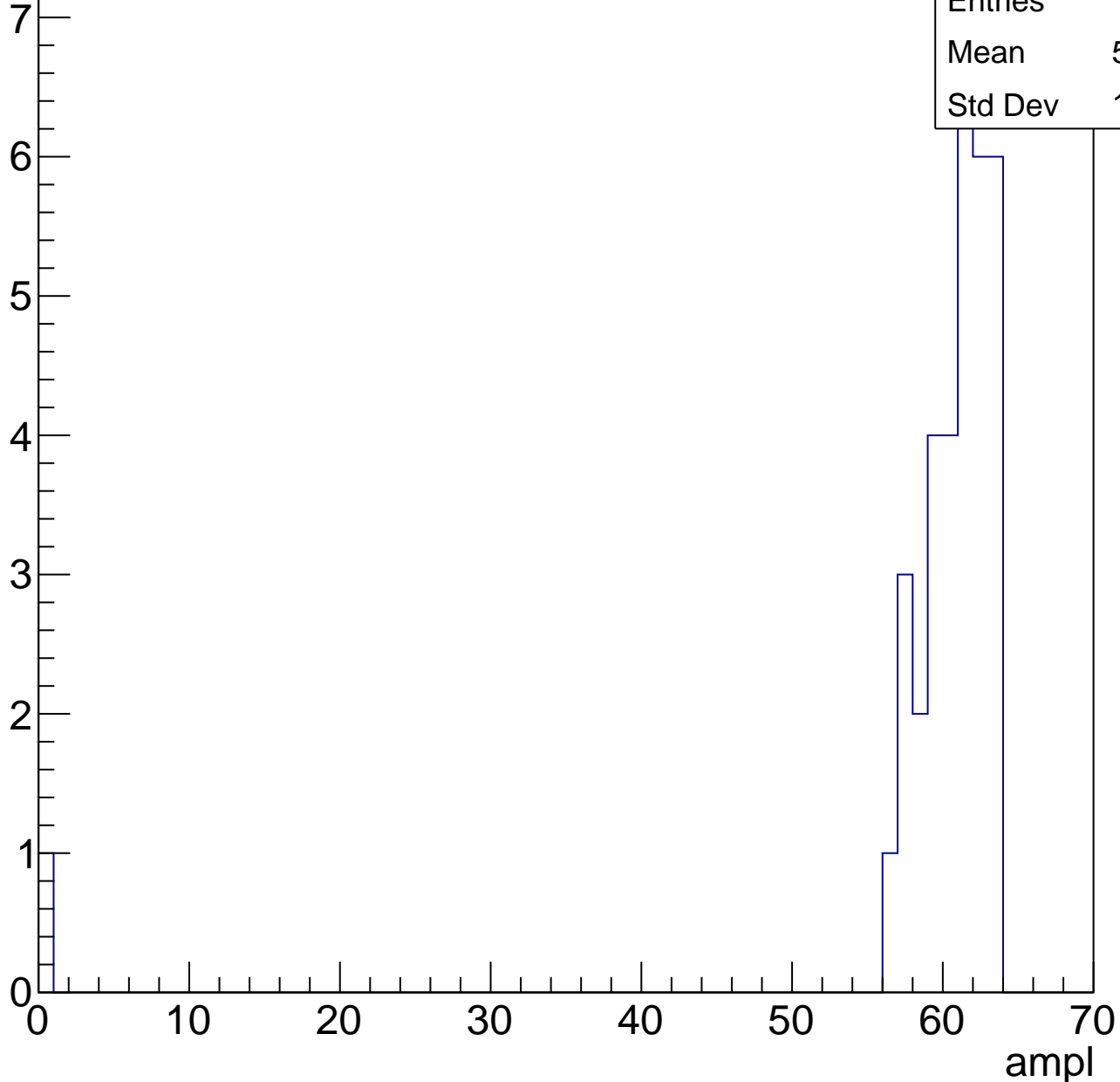


# B1L103S, U2-ch1, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	34
Mean	58.71
Std Dev	10.41



# B1L103S, U2-ch1, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U2-ch1, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch2, adc0

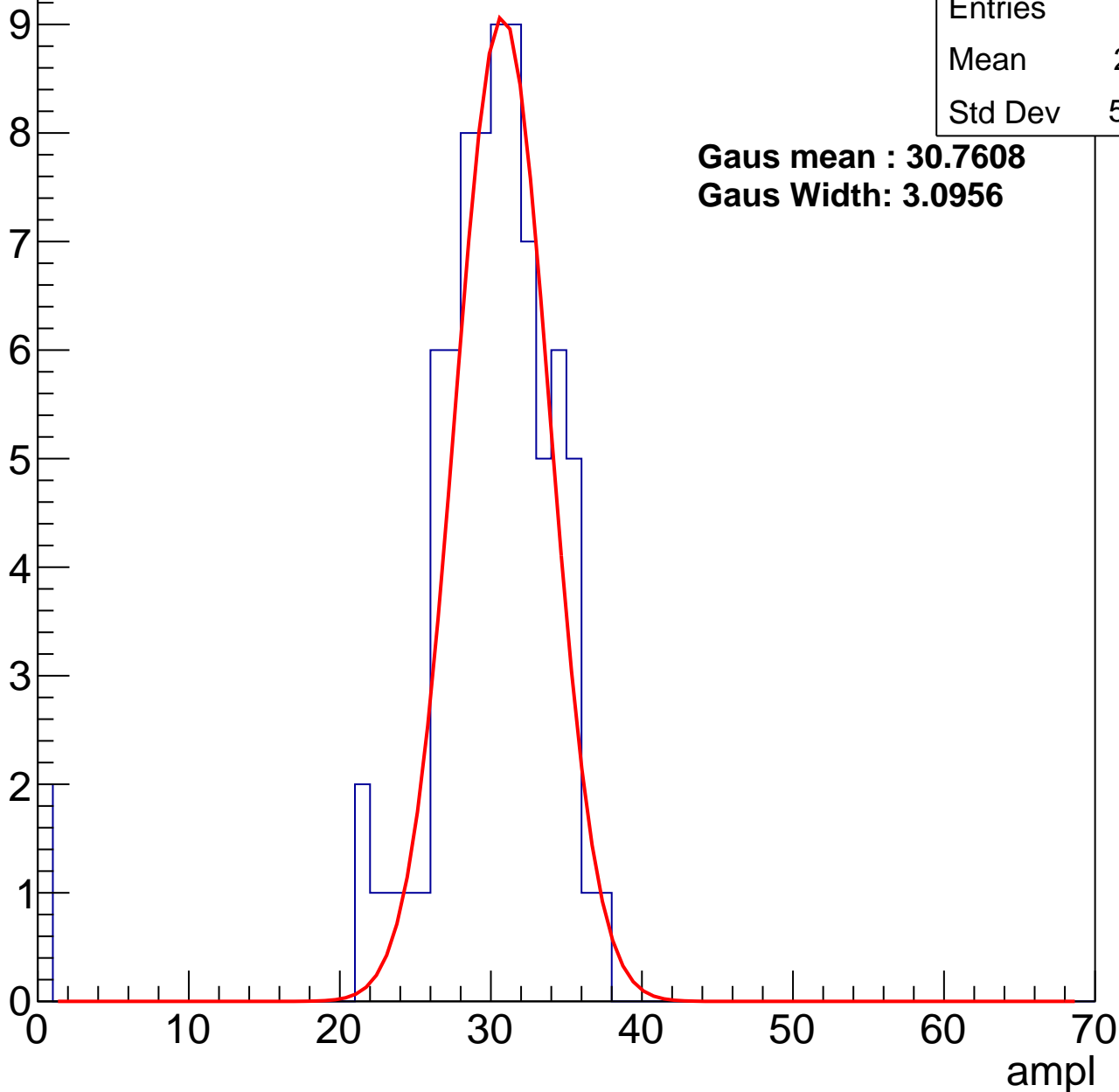
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	79
Mean	29.11
Std Dev	5.794

**Gaus mean : 30.7608**

**Gaus Width: 3.0956**



# B1L103S, U2-ch2, adc1

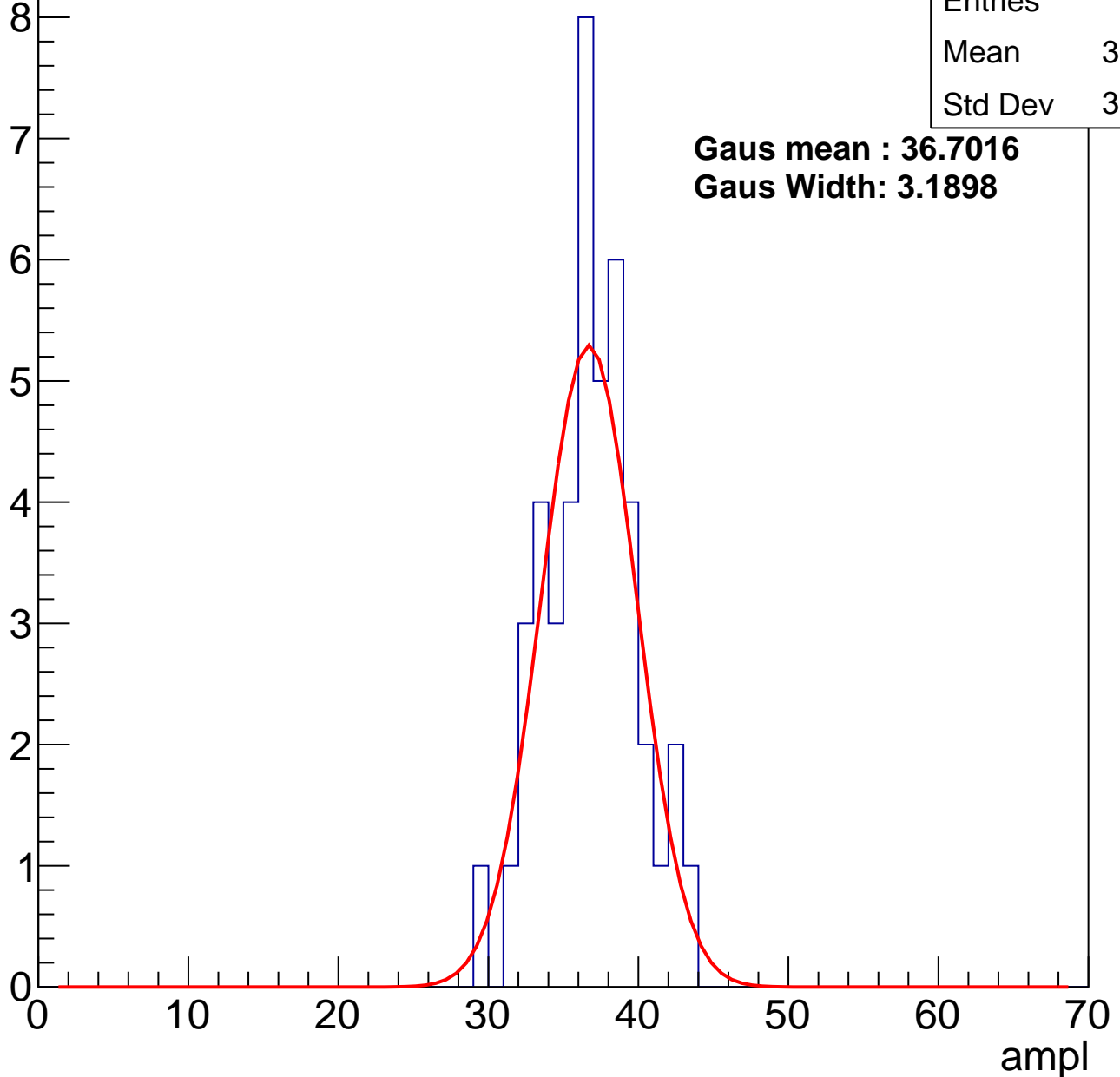
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	45
Mean	36.33
Std Dev	3.026

**Gaus mean : 36.7016**

**Gaus Width: 3.1898**



# B1L103S, U2-ch2, adc2

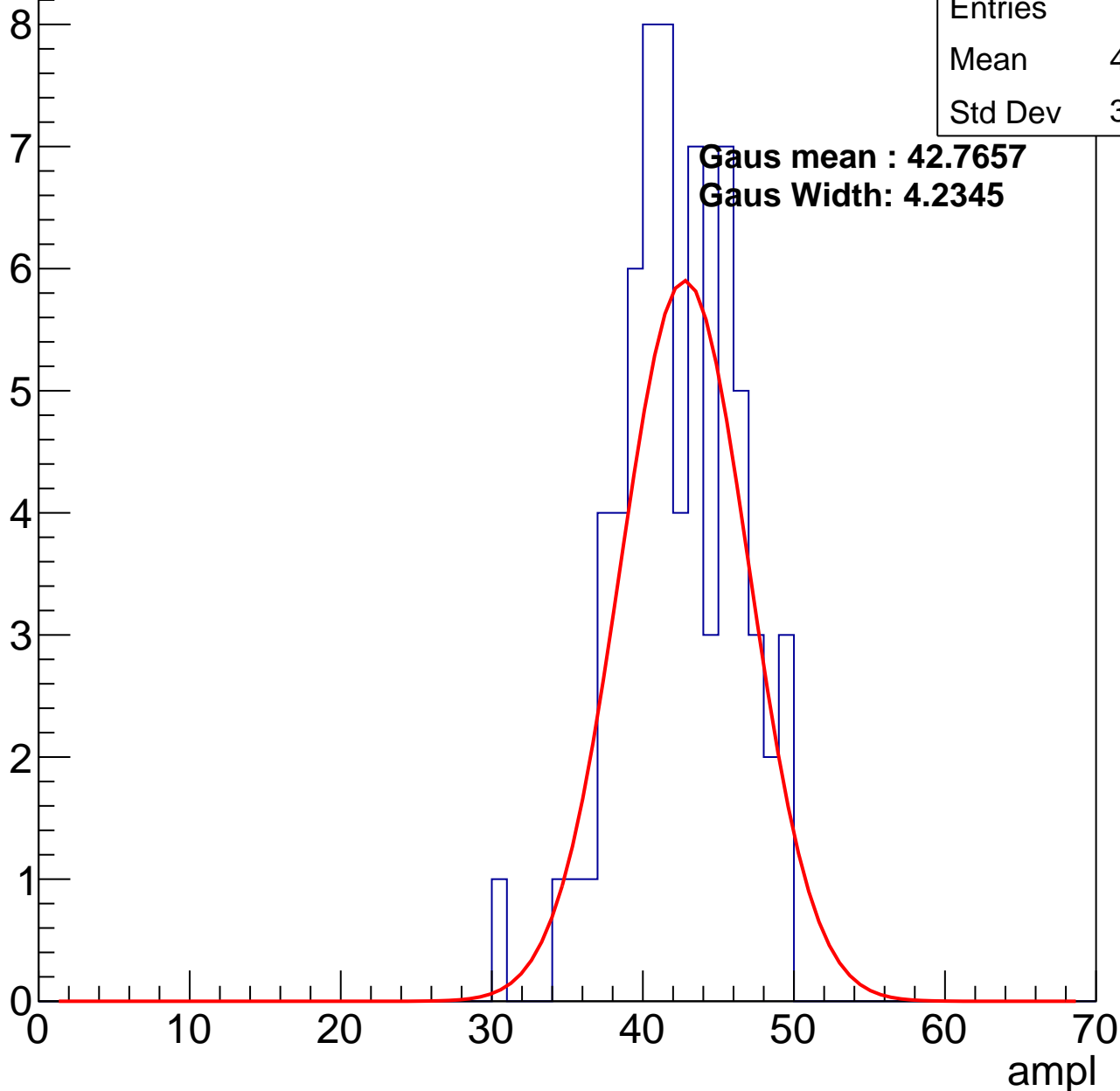
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	41.87
Std Dev	3.846

**Gaus mean : 42.7657**

**Gaus Width: 4.2345**

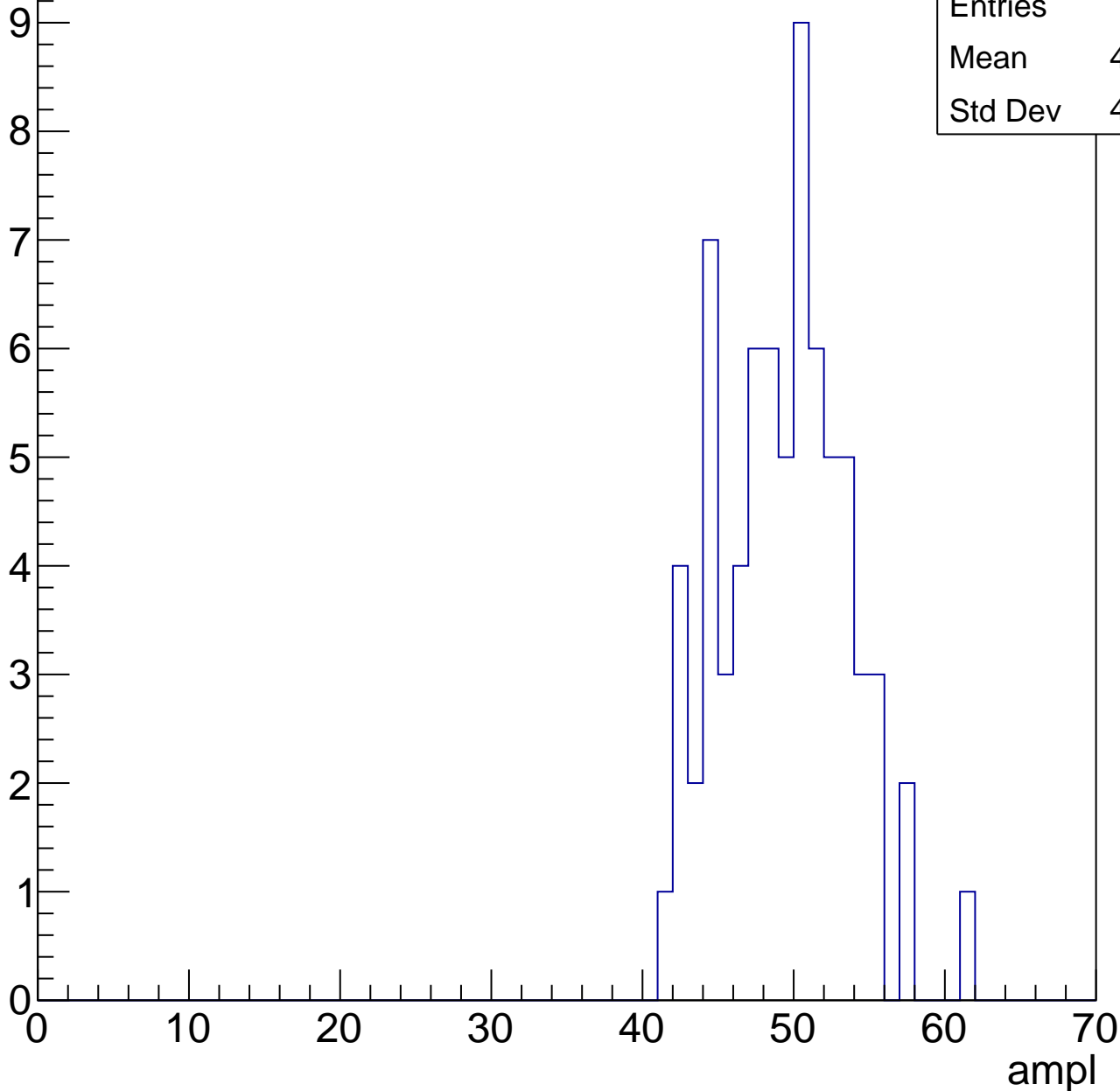


# B1L103S, U2-ch2, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	48.89
Std Dev	4.138

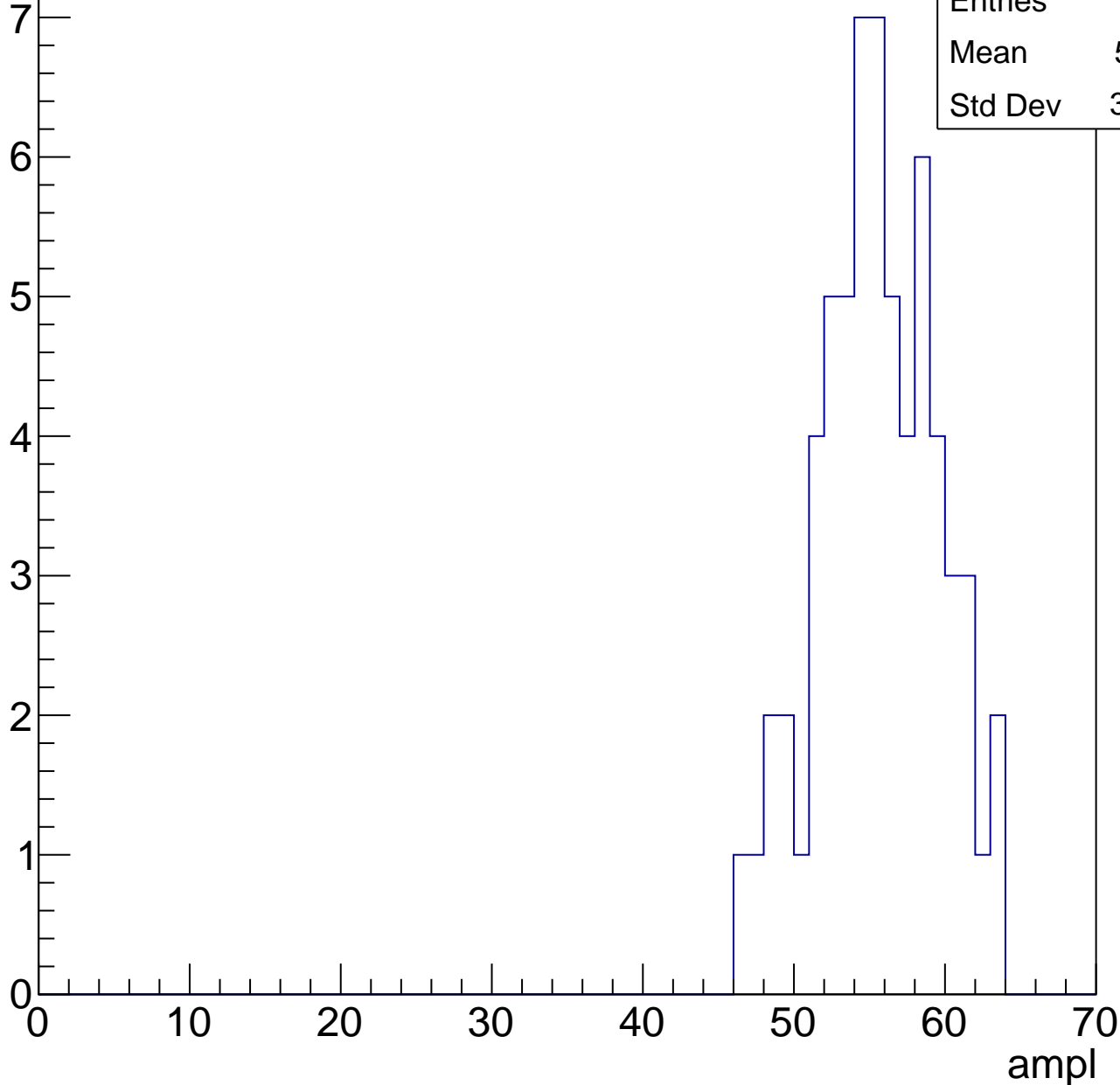


# B1L103S, U2-ch2, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

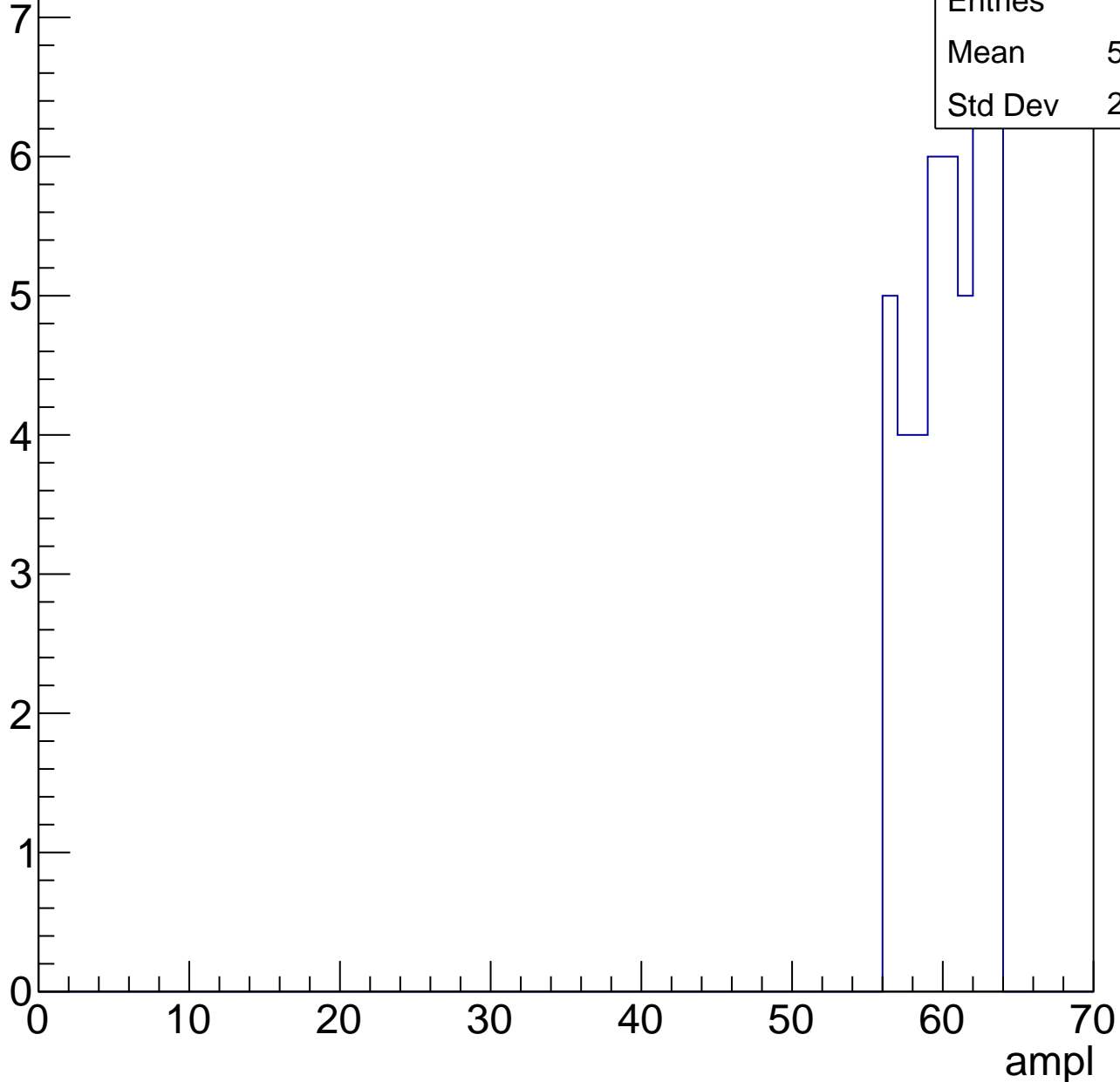
Entries	63
Mean	55.11
Std Dev	3.932



# B1L103S, U2-ch2, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	44
Mean	59.86
Std Dev	2.302

# B1L103S, U2-ch2, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

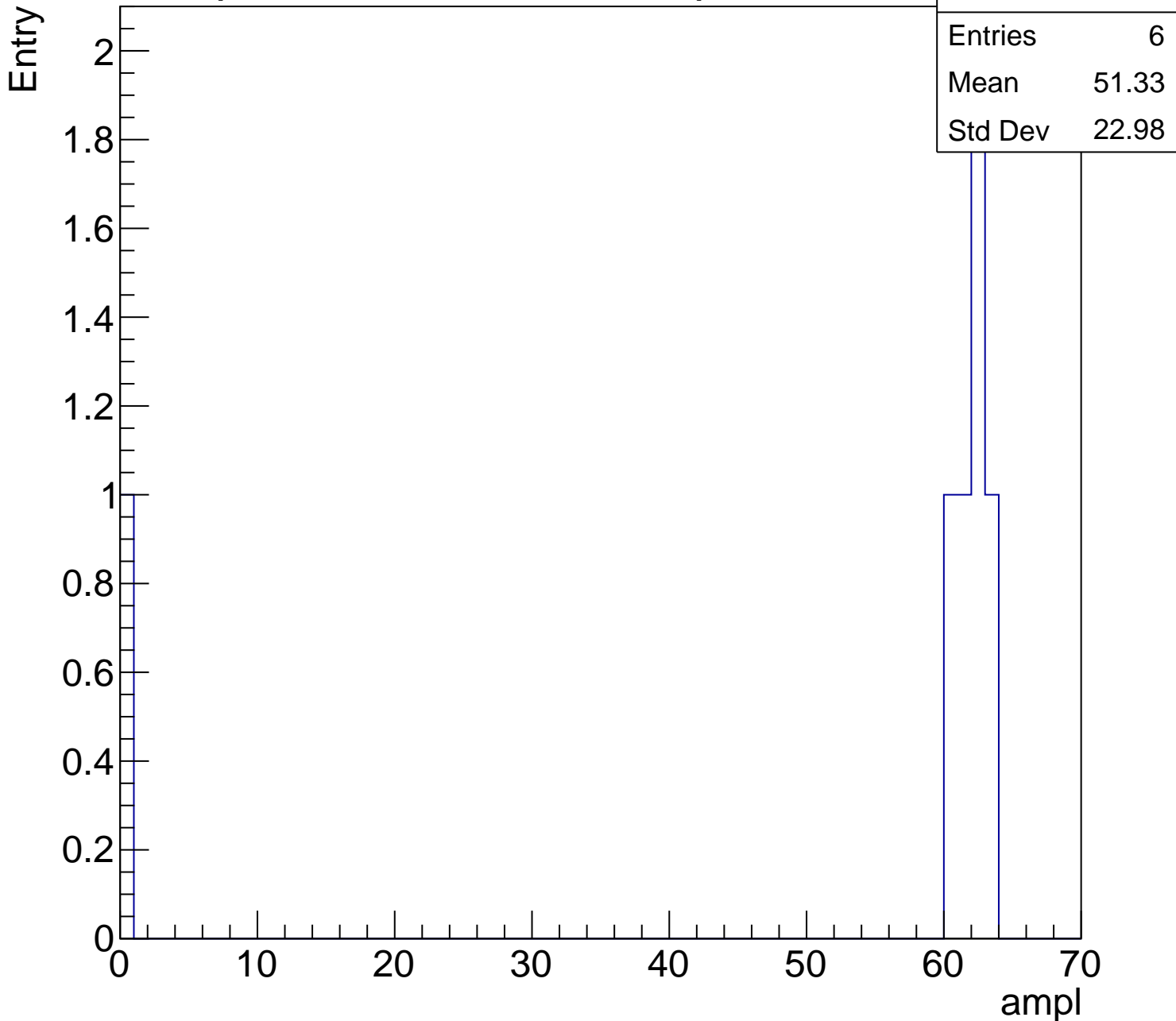
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	51.33
Std Dev	22.98

0 10 20 30 40 50 60 70

ampl





# B1L103S, U2-ch2, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U2-ch3, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	71
Mean	27.97
Std Dev	3.113

**Gaus mean : 28.6749**

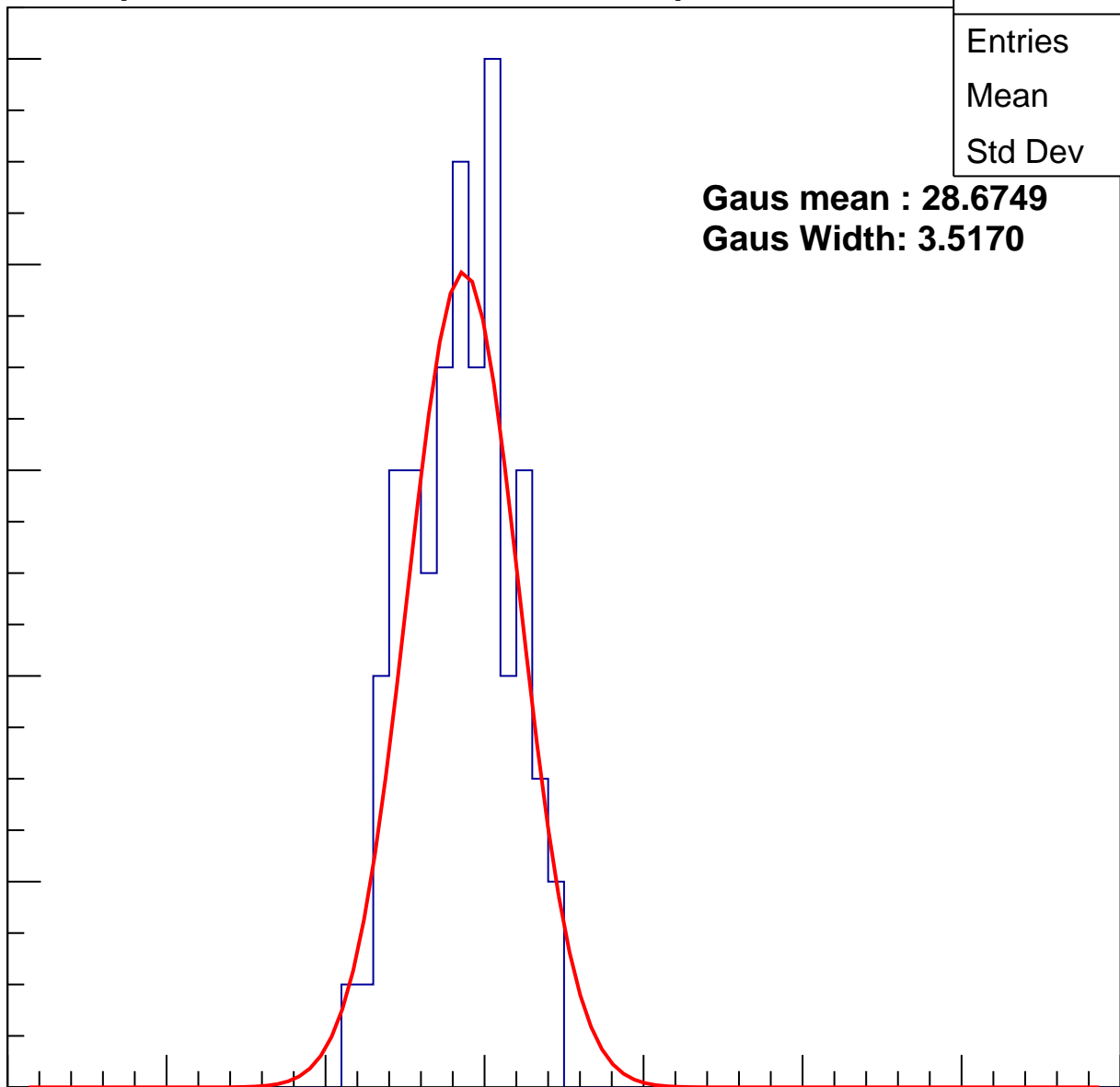
**Gaus Width: 3.5170**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U2-ch3, adc1

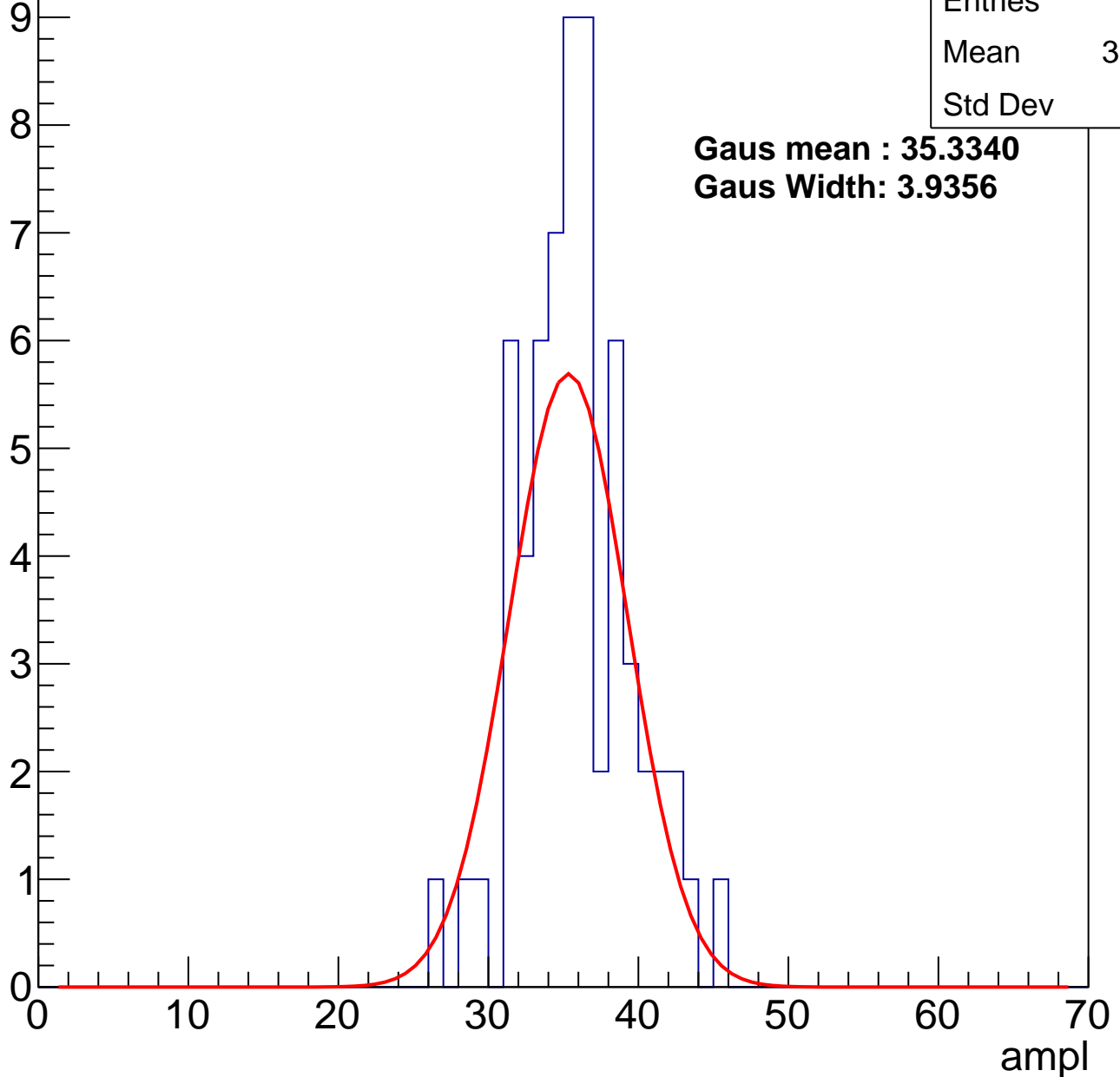
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	35.32
Std Dev	3.62

**Gaus mean : 35.3340**

**Gaus Width: 3.9356**



# B1L103S, U2-ch3, adc2

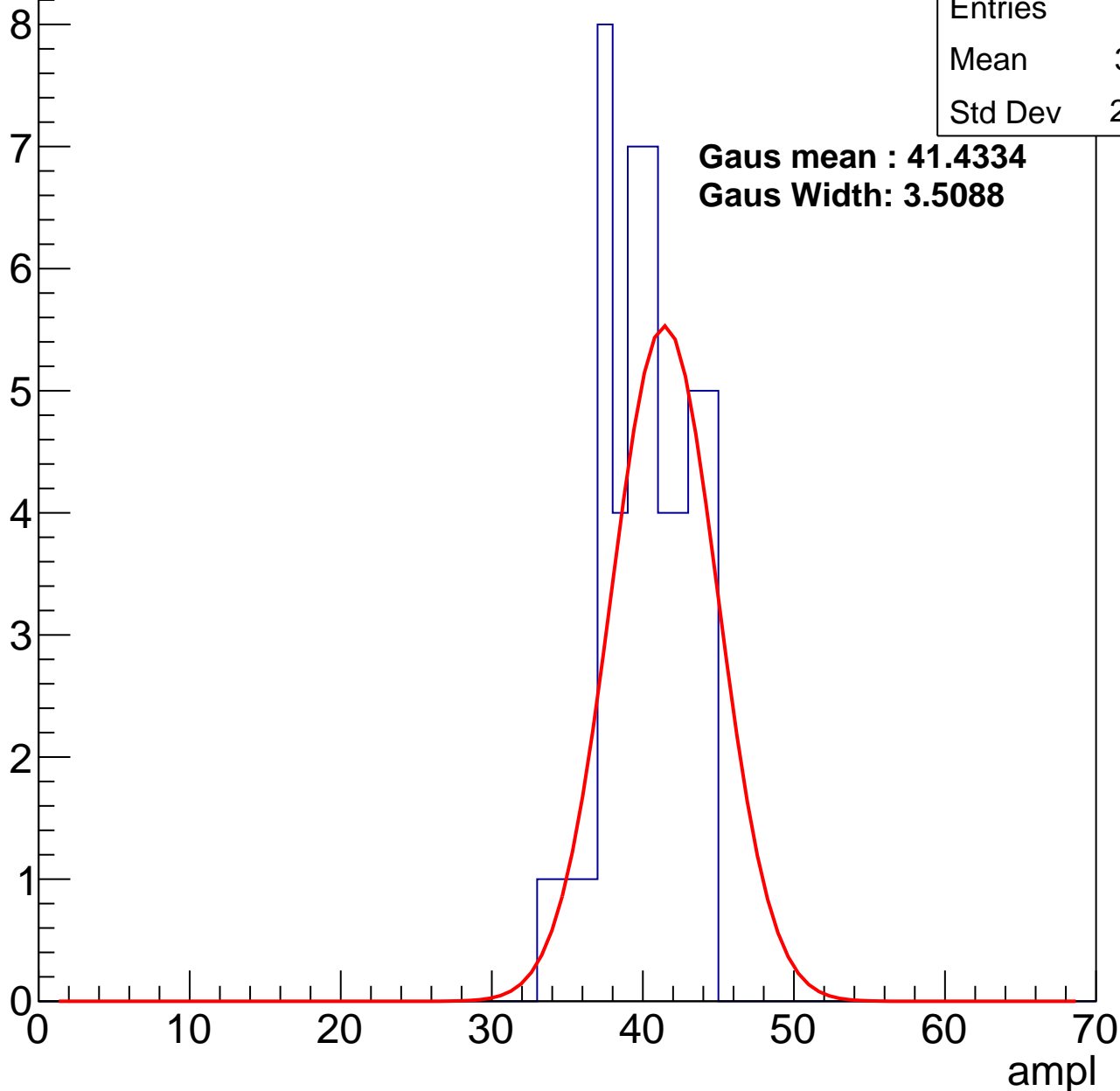
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	48
Mean	39.71
Std Dev	2.746

**Gaus mean : 41.4334**

**Gaus Width: 3.5088**

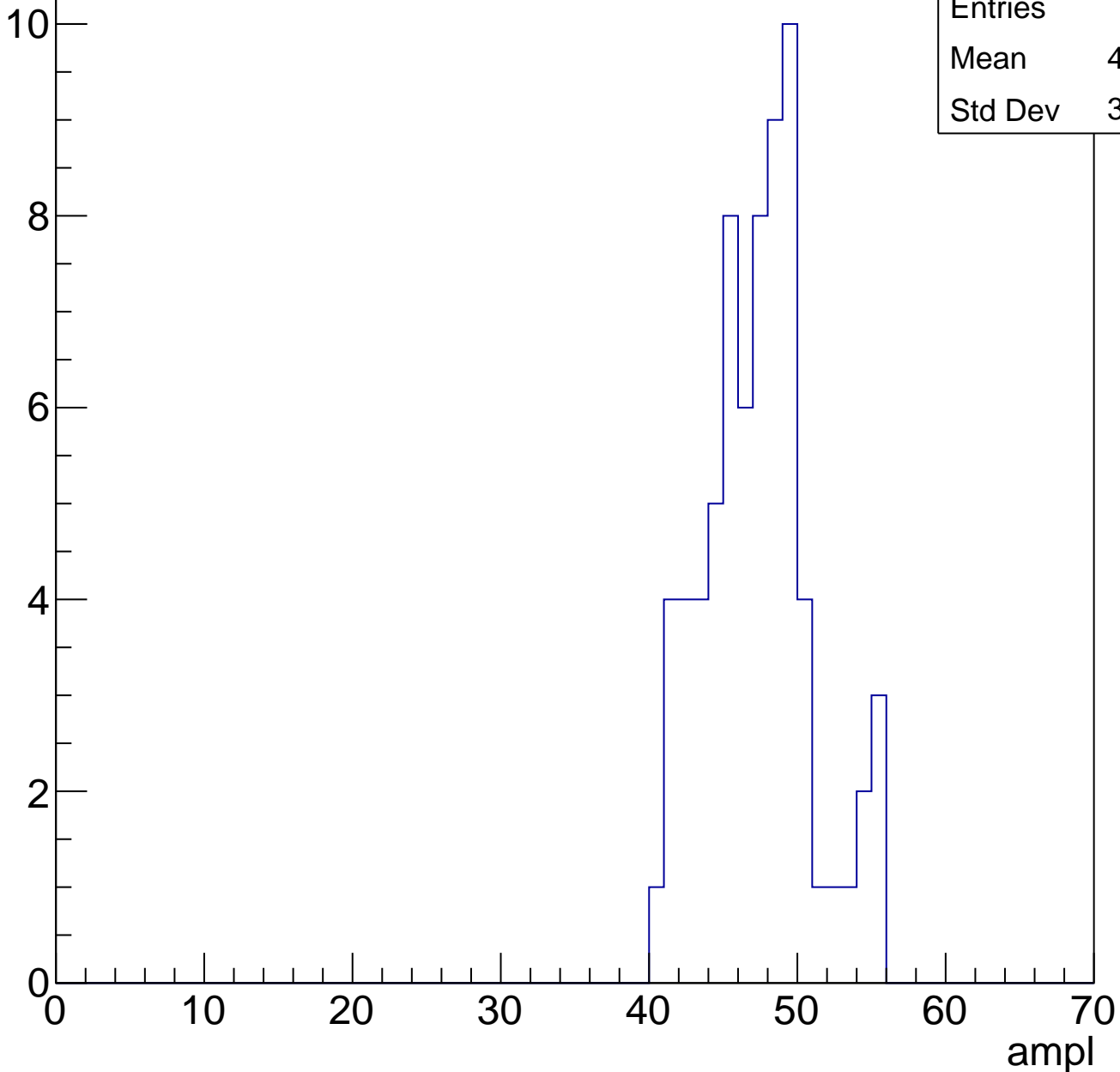


# B1L103S, U2-ch3, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	71
Mean	46.86
Std Dev	3.542

Entry

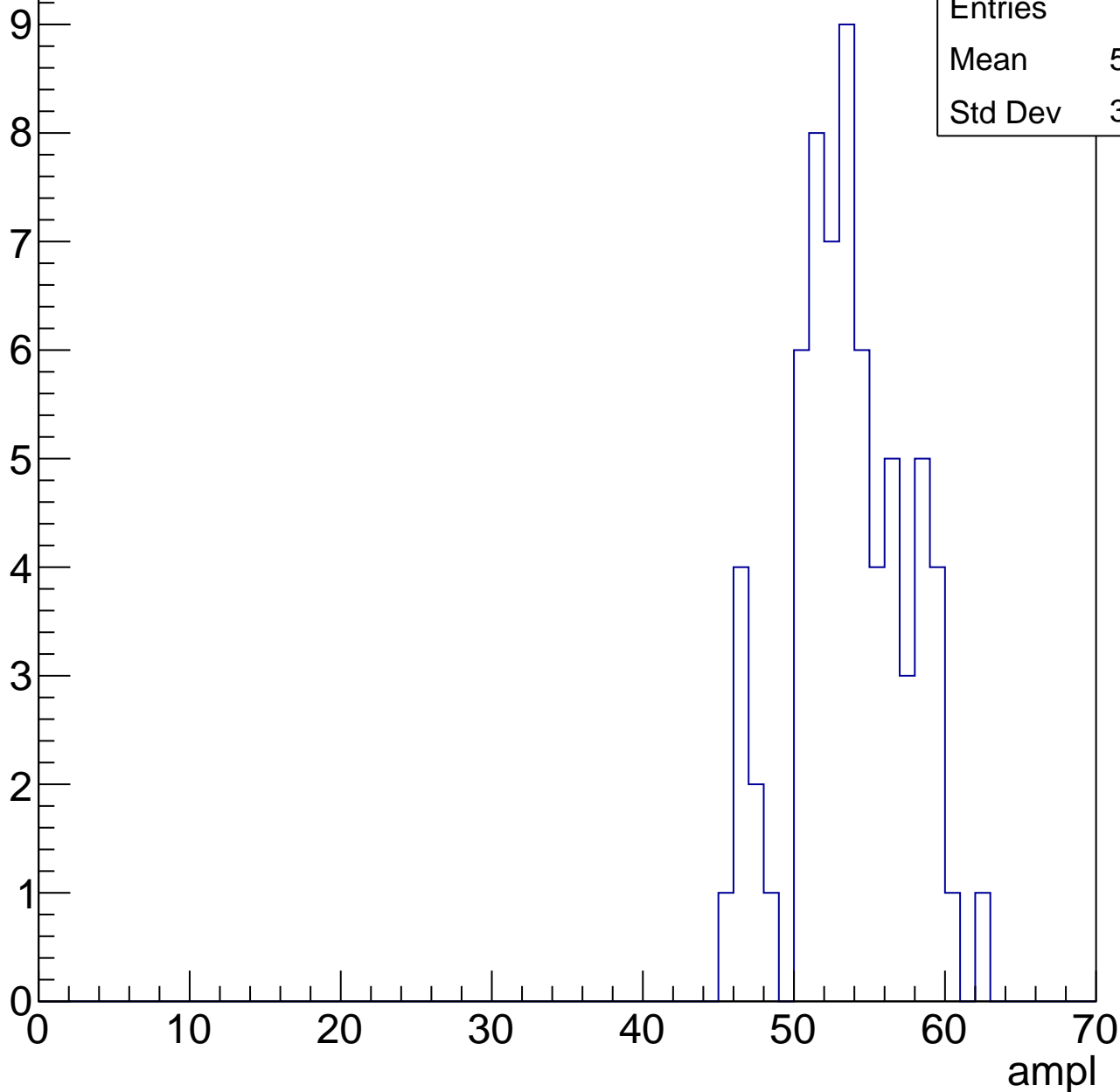


# B1L103S, U2-ch3, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	53.18
Std Dev	3.789

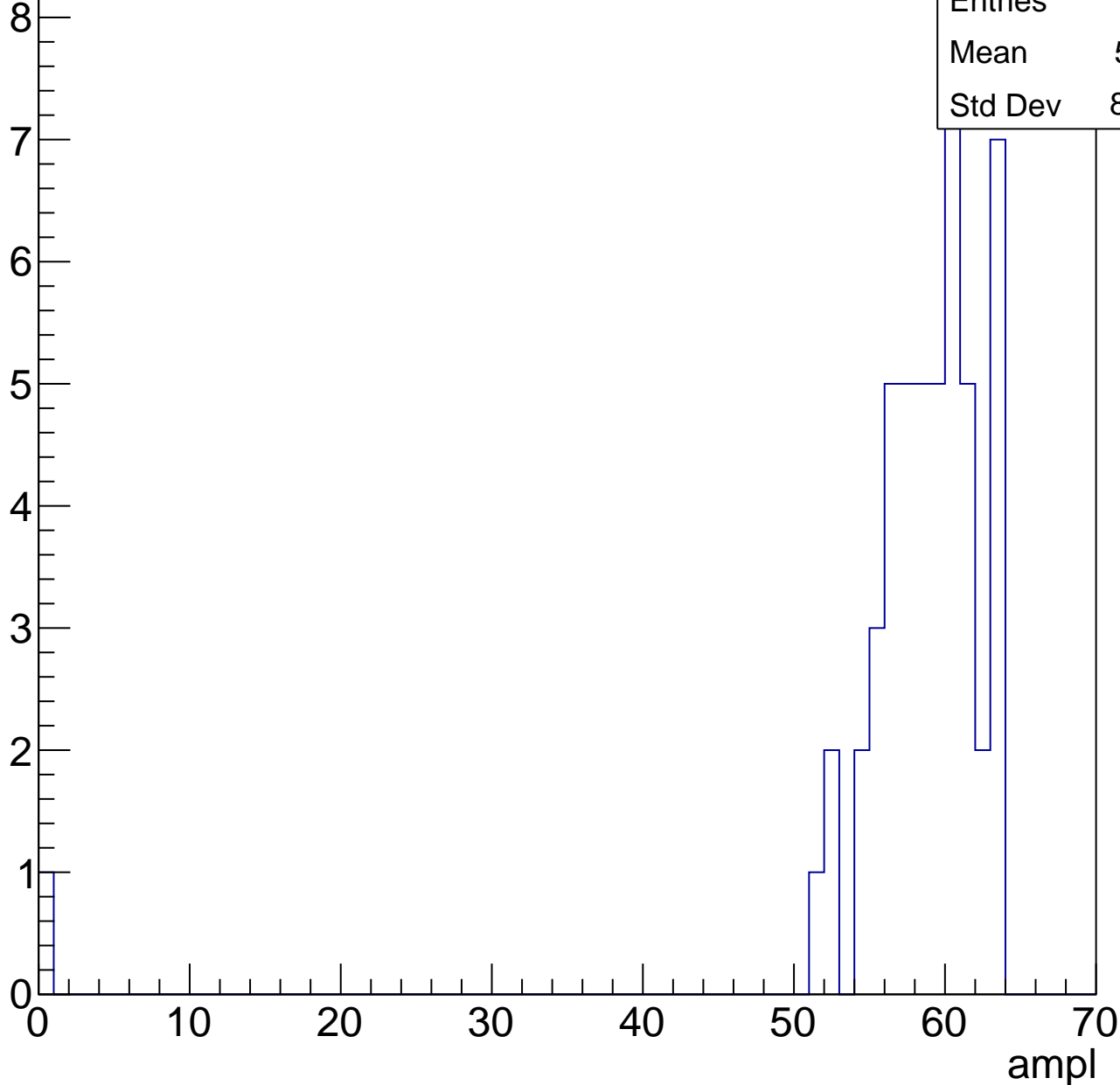


# B1L103S, U2-ch3, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	57.41
Std Dev	8.678

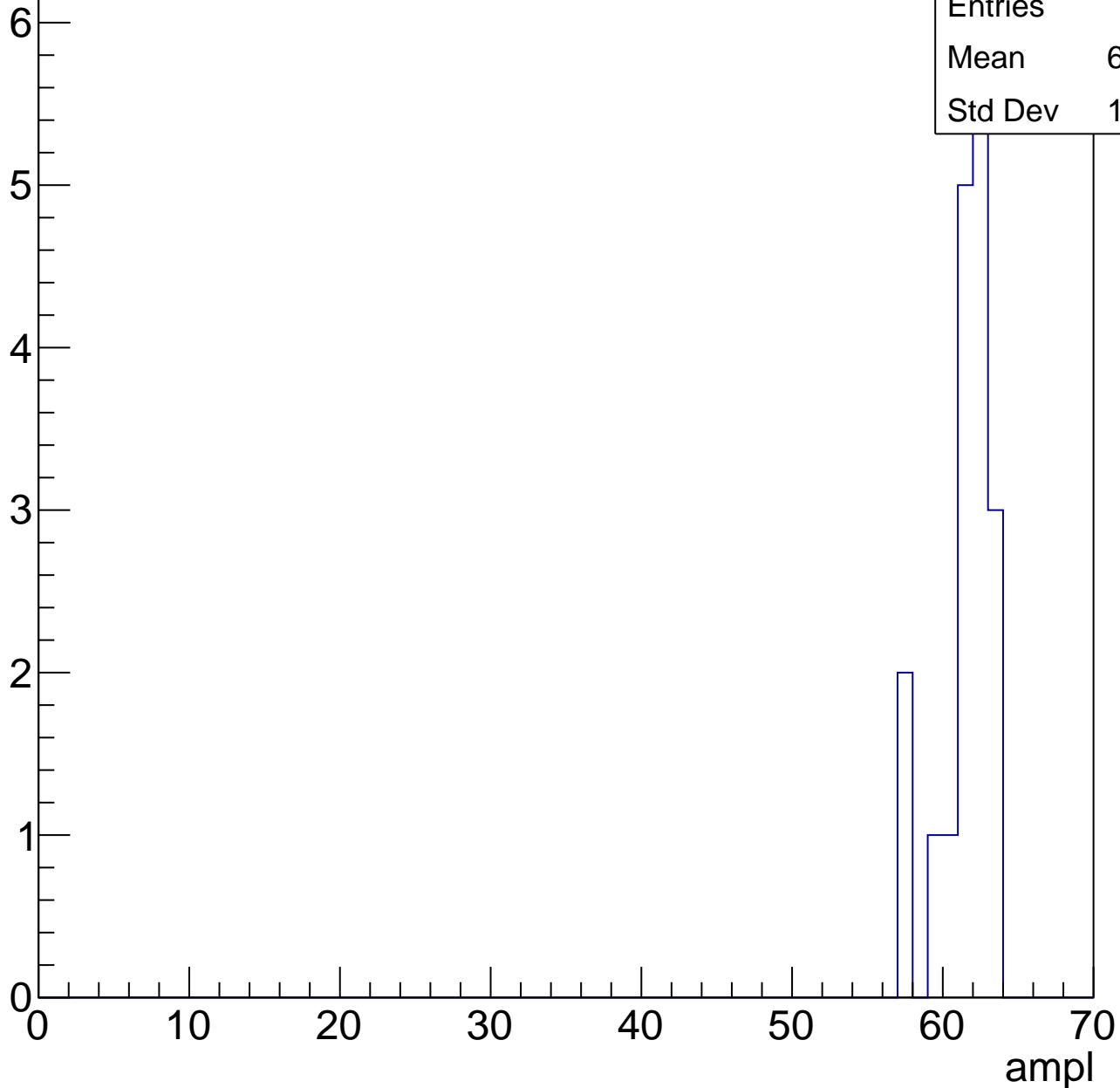


# B1L103S, U2-ch3, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	18
Mean	61.06
Std Dev	1.747

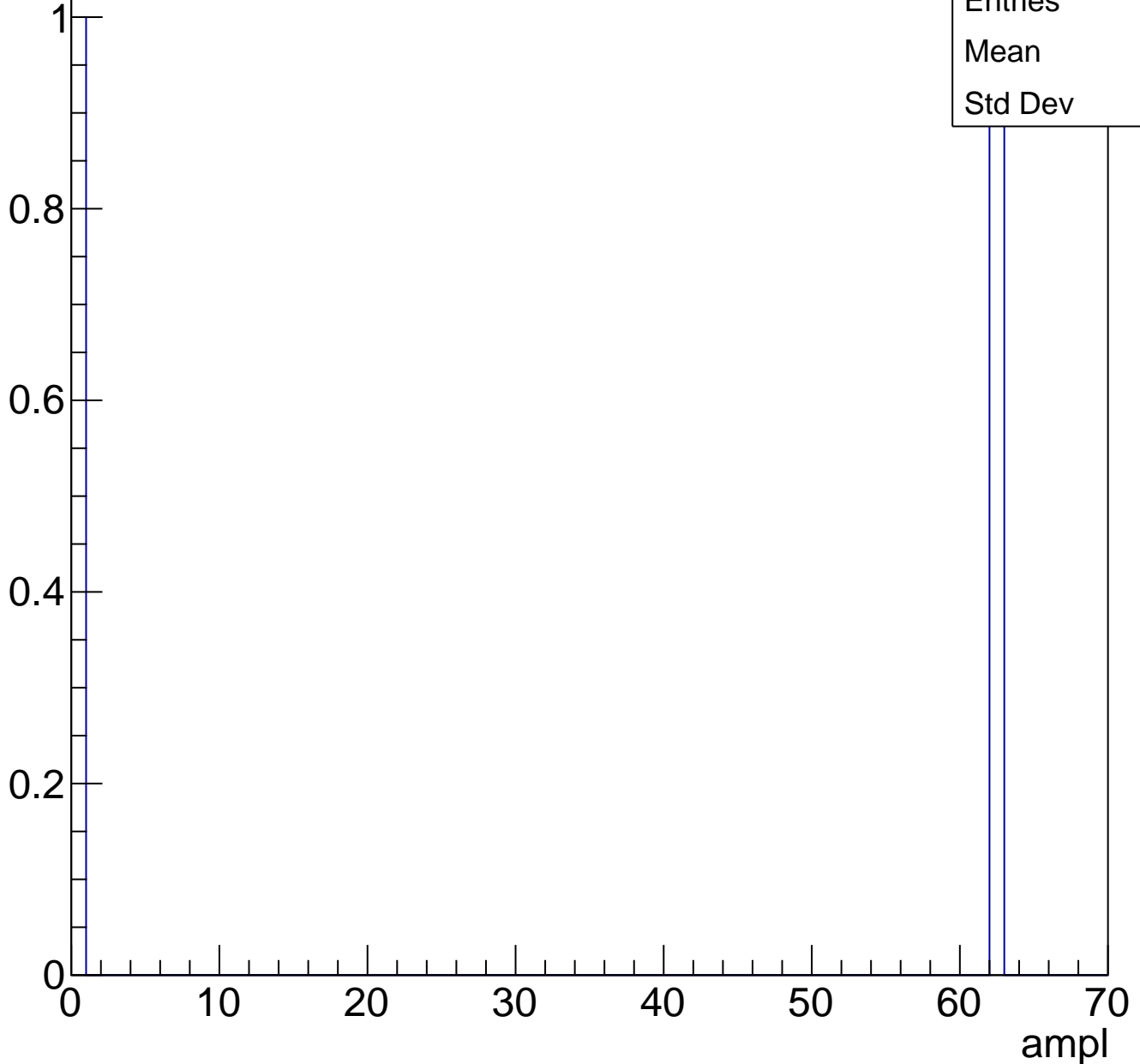




# B1L103S, U2-ch3, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch4, adc0

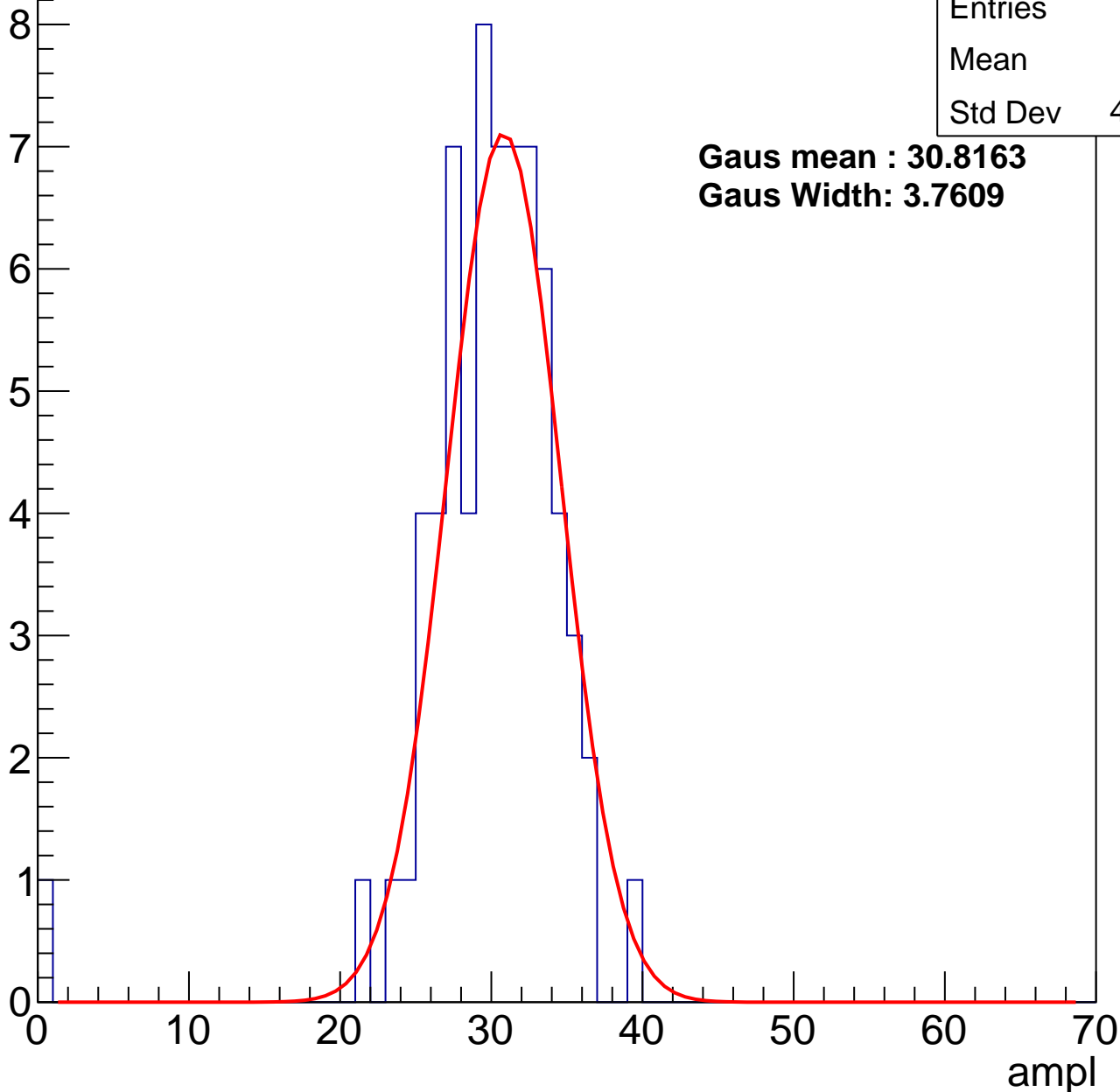
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	29.5
Std Dev	4.972

**Gaus mean : 30.8163**

**Gaus Width: 3.7609**



# B1L103S, U2-ch4, adc1

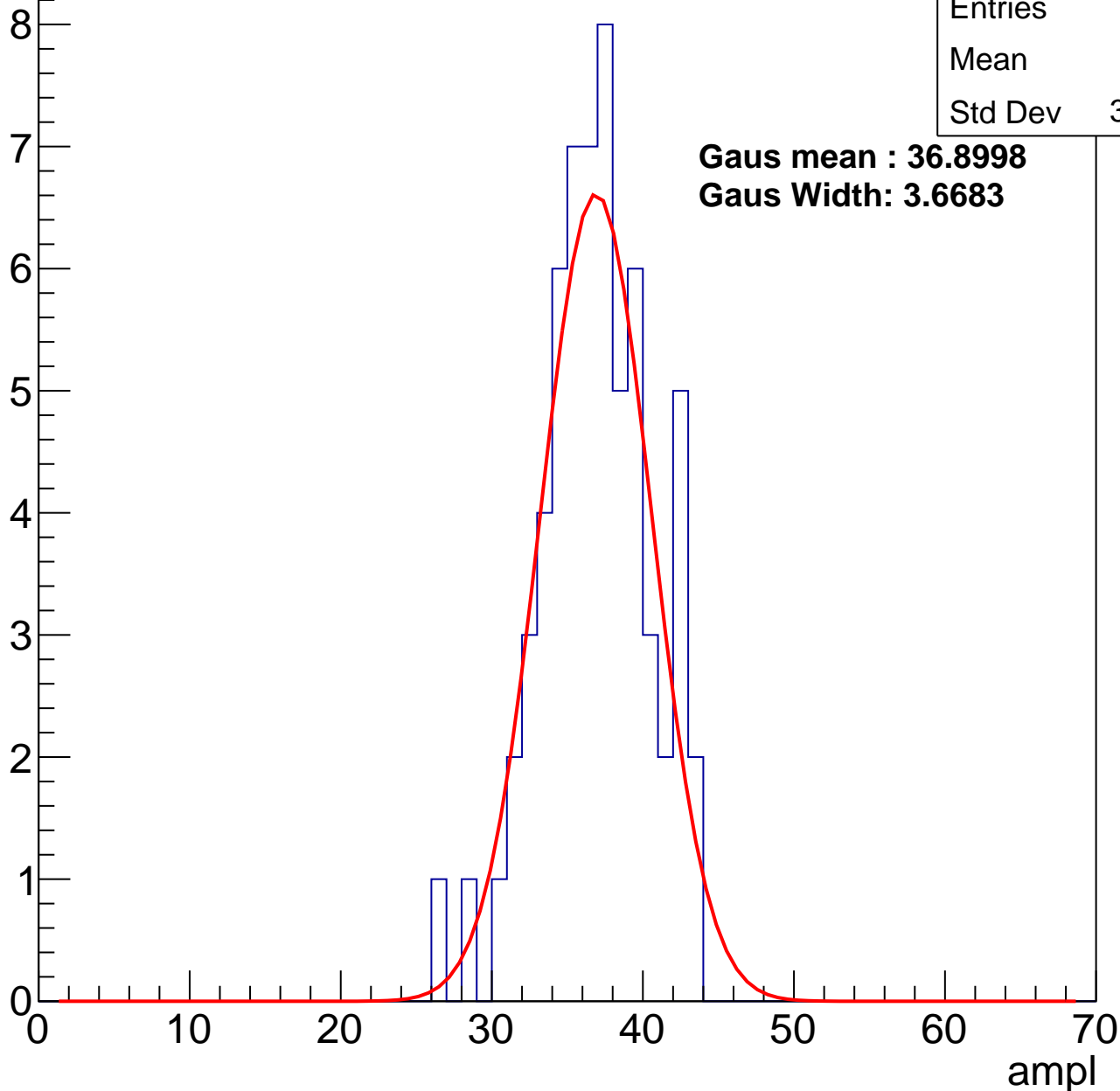
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	36.4
Std Dev	3.592

**Gaus mean : 36.8998**

**Gaus Width: 3.6683**



# B1L103S, U2-ch4, adc2

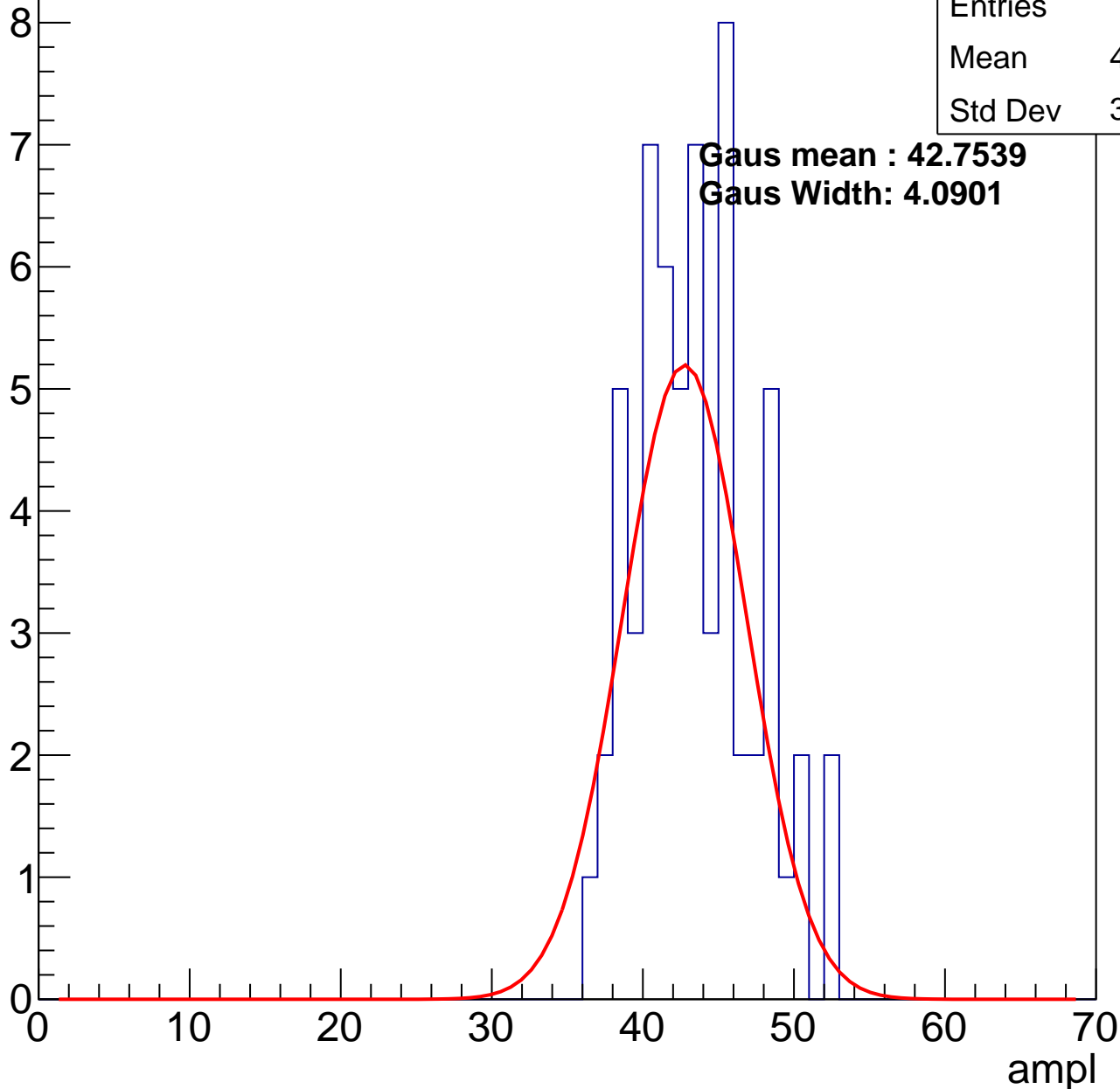
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	43.03
Std Dev	3.824

**Gaus mean : 42.7539**

**Gaus Width: 4.0901**

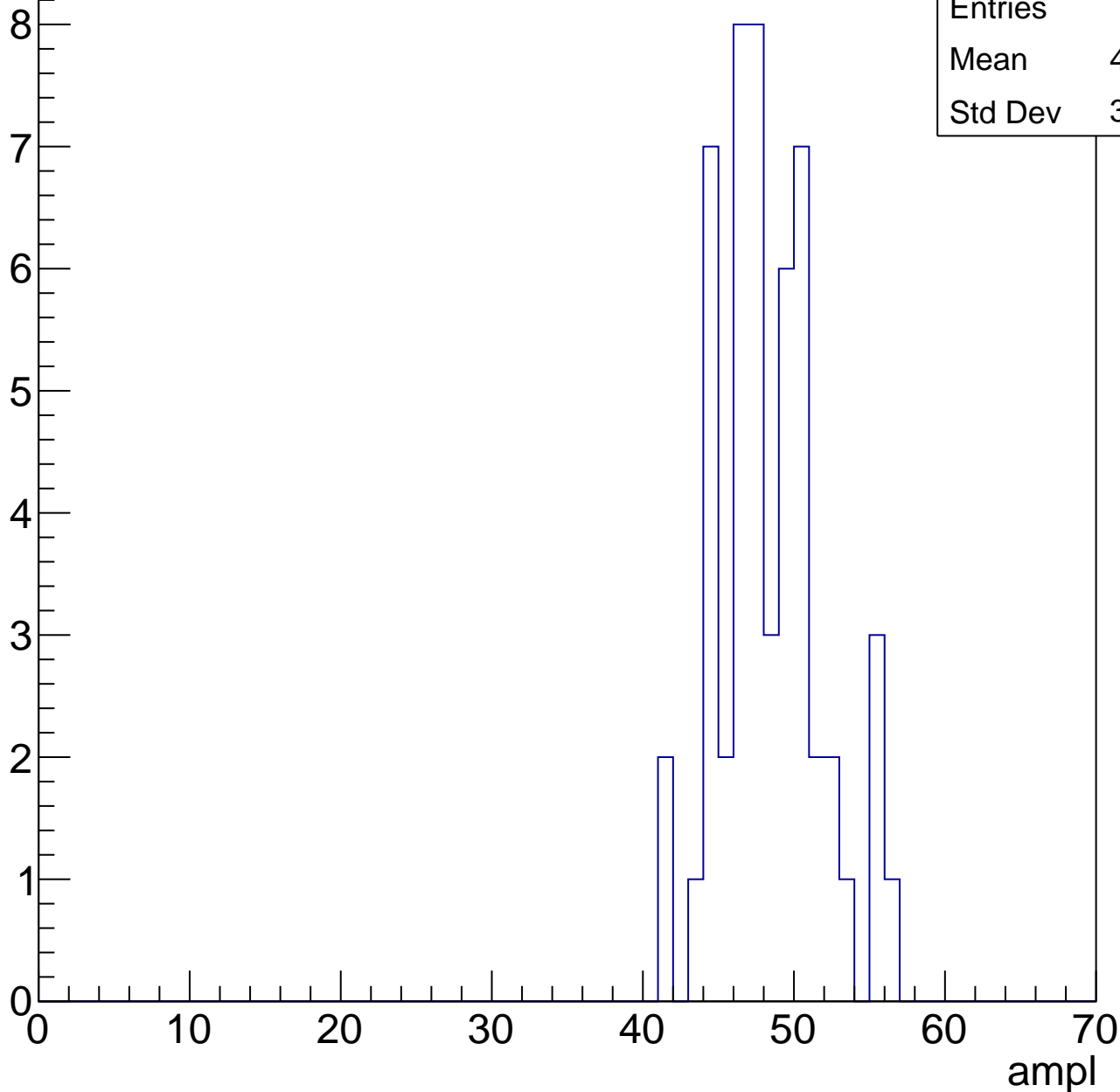


# B1L103S, U2-ch4, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	47.83
Std Dev	3.397



# B1L103S, U2-ch4, adc4

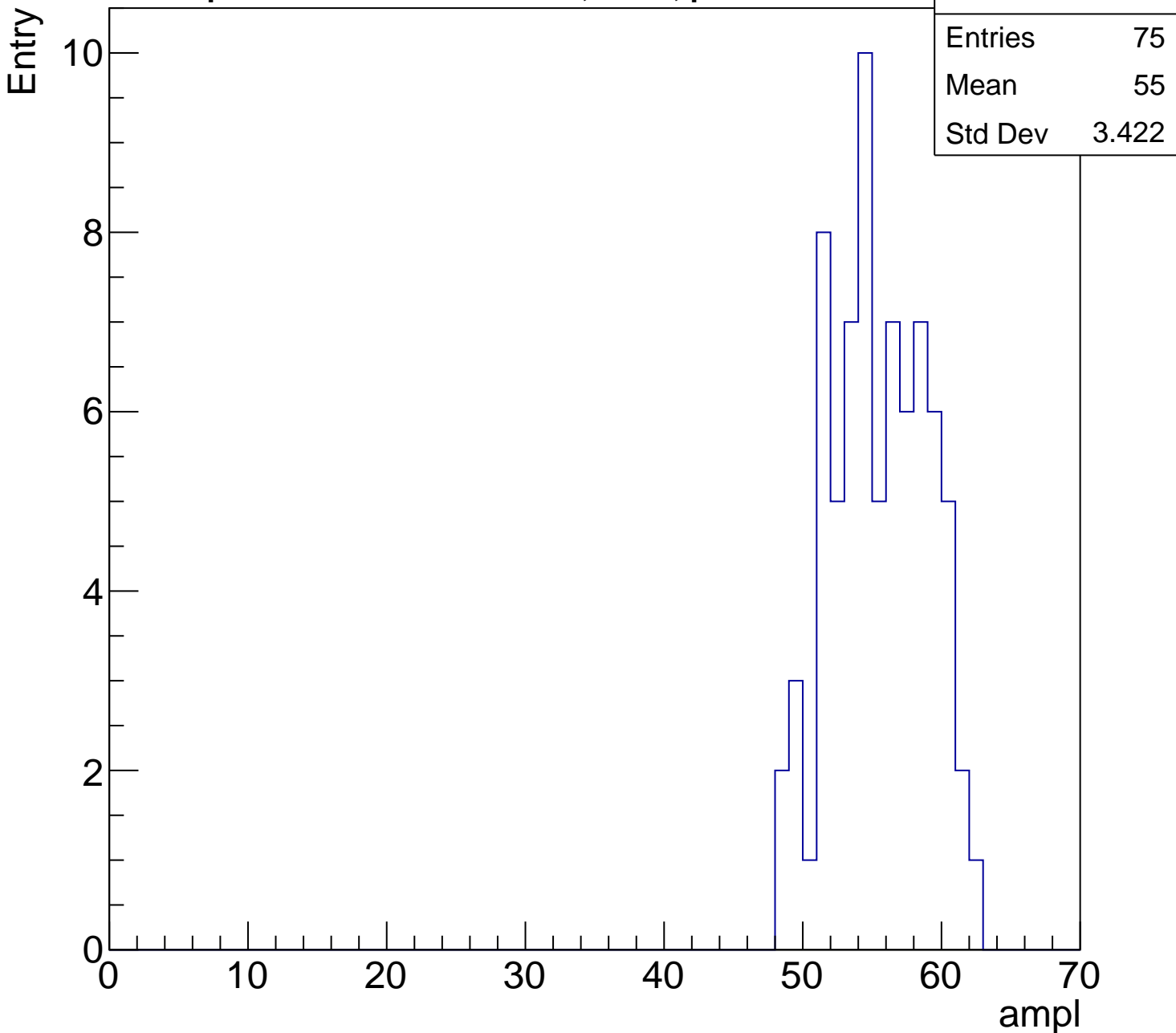
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	75
Mean	55
Std Dev	3.422

Entry

10  
8  
6  
4  
2  
0

ampl

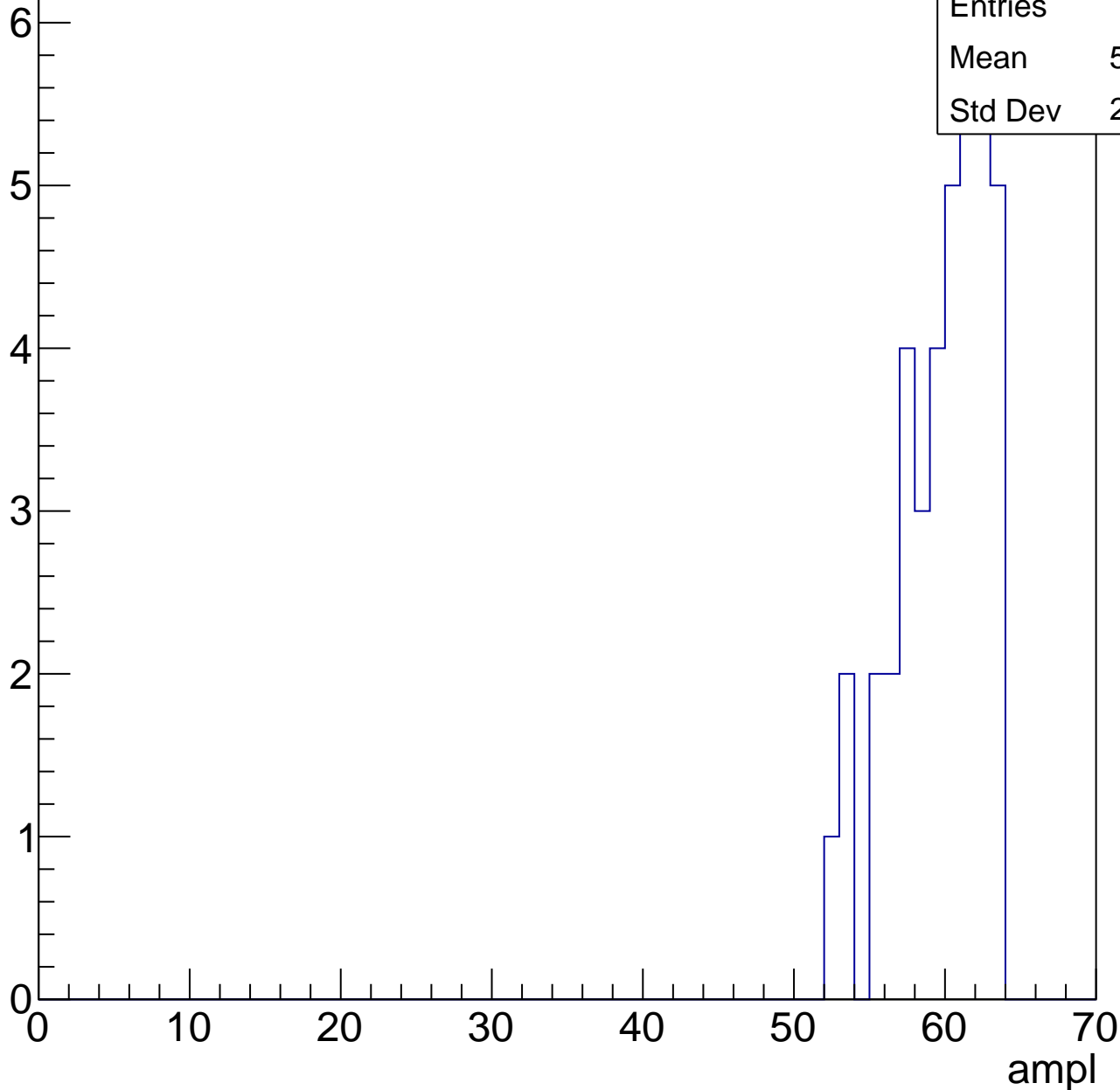


# B1L103S, U2-ch4, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

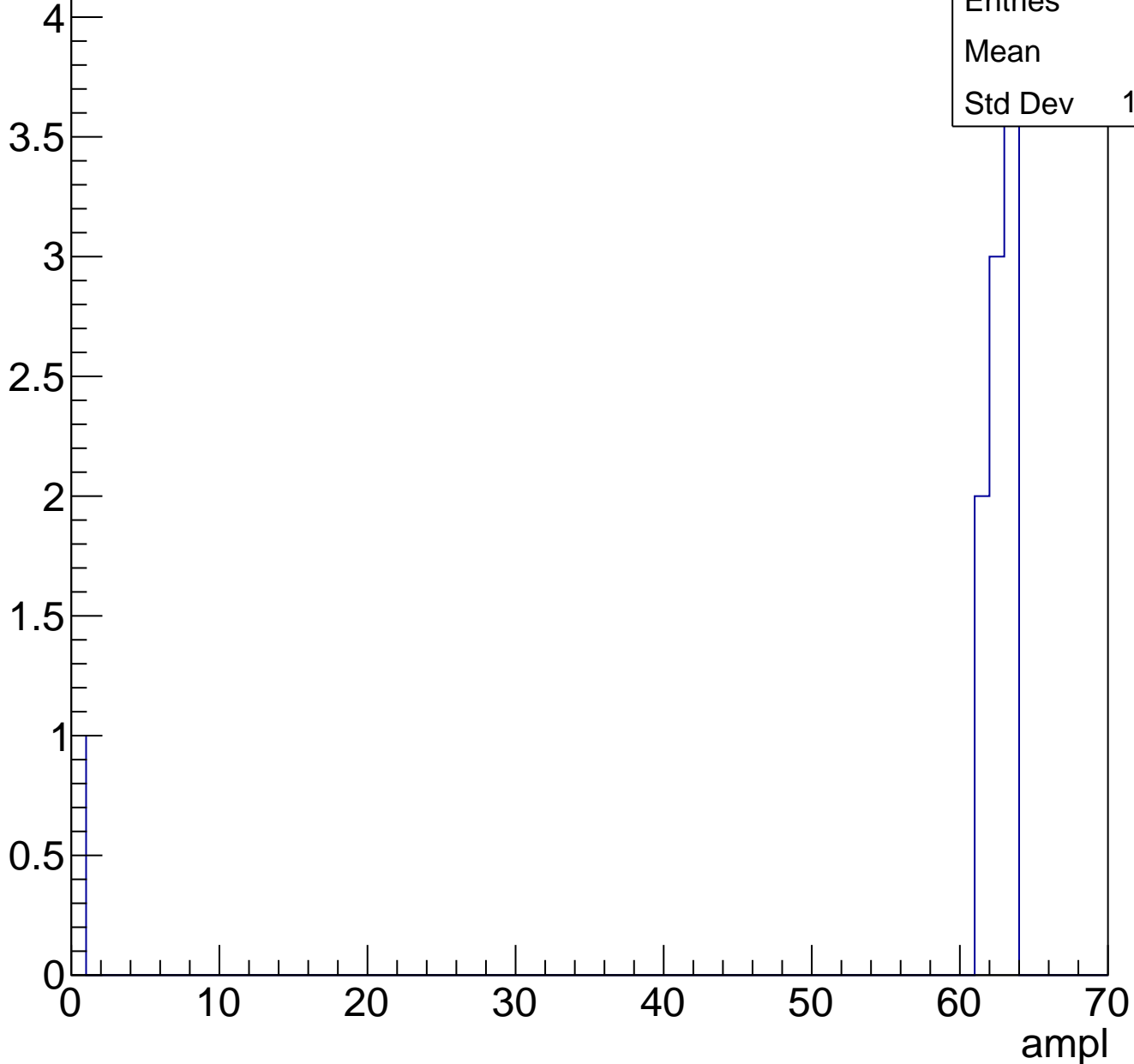
Entries	40
Mean	59.27
Std Dev	2.958



# B1L103S, U2-ch4, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U2-ch4, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch5, adc0

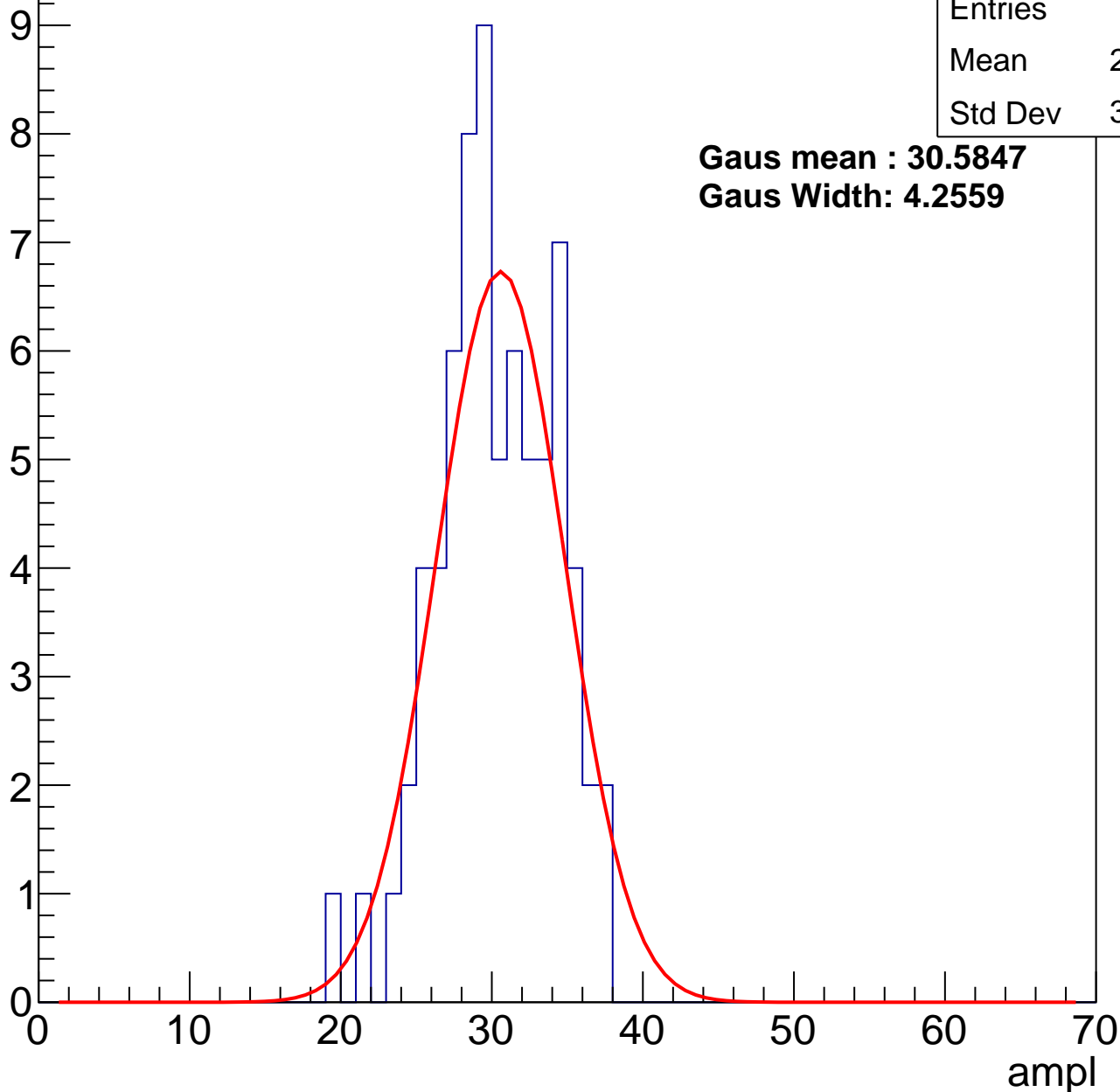
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	29.82
Std Dev	3.787

**Gaus mean : 30.5847**

**Gaus Width: 4.2559**



# B1L103S, U2-ch5, adc1

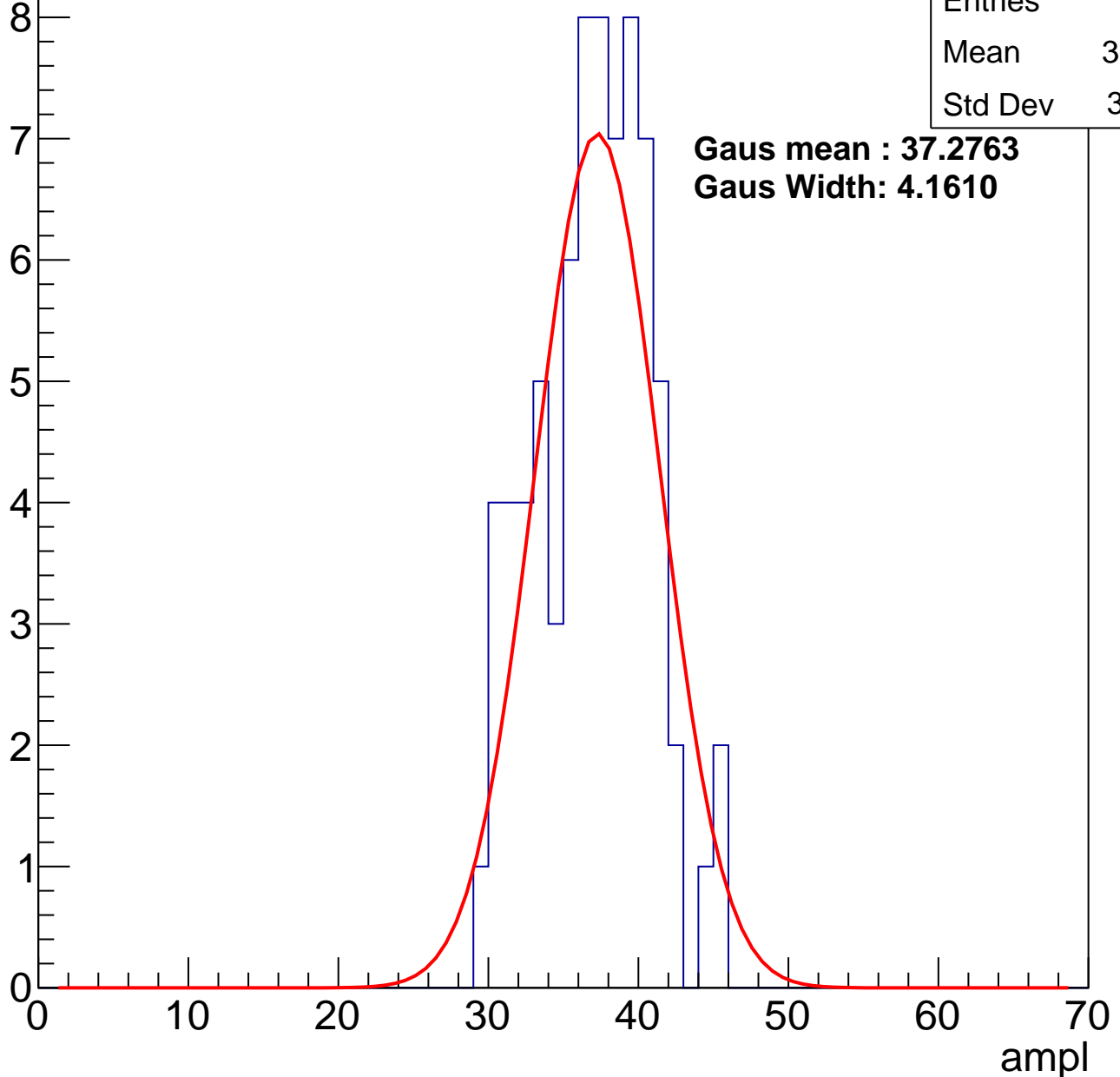
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	36.57
Std Dev	3.721

**Gaus mean : 37.2763**

**Gaus Width: 4.1610**



# B1L103S, U2-ch5, adc2

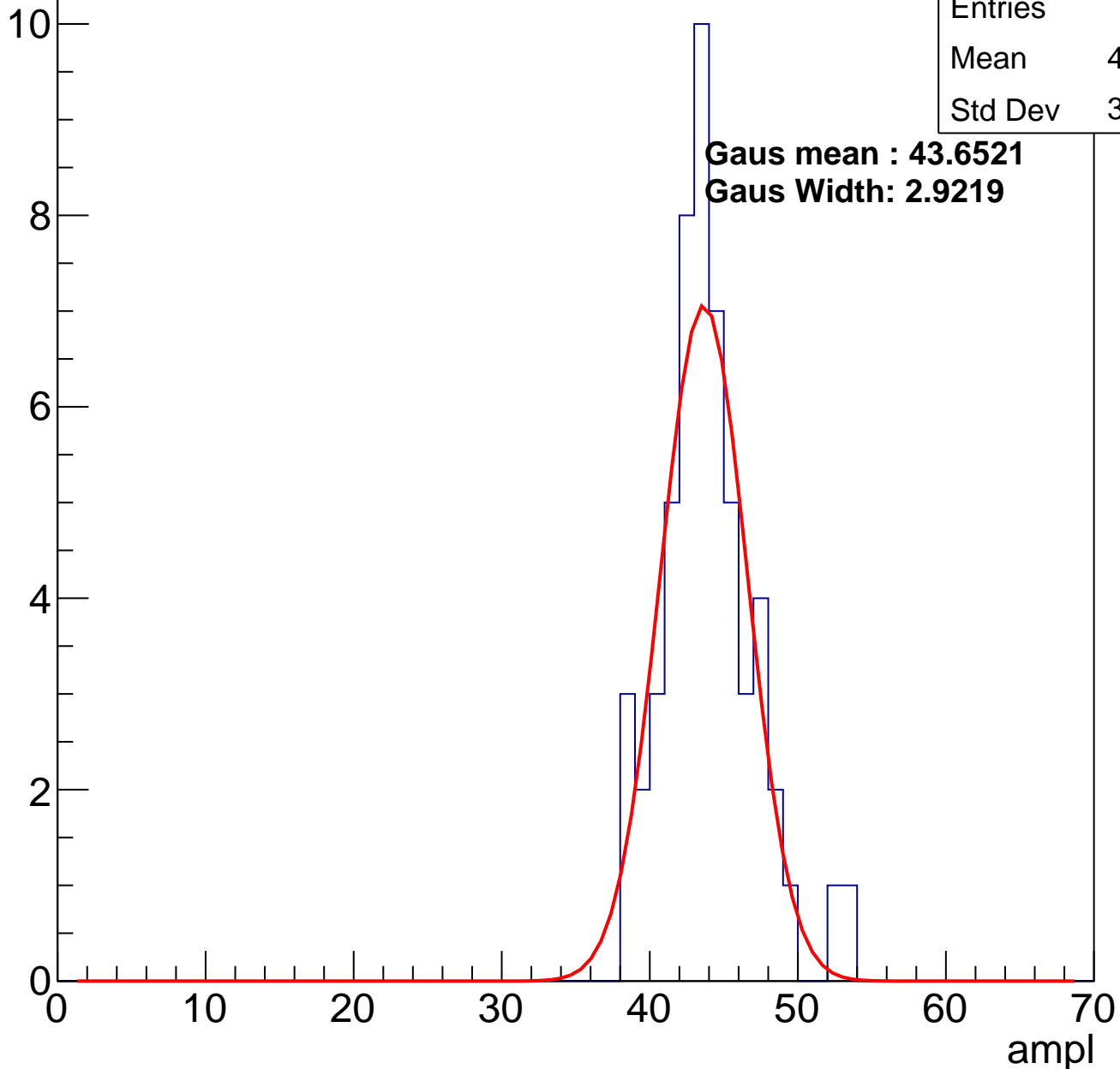
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	55
Mean	43.49
Std Dev	3.115

**Gaus mean : 43.6521**

**Gaus Width: 2.9219**

Entry

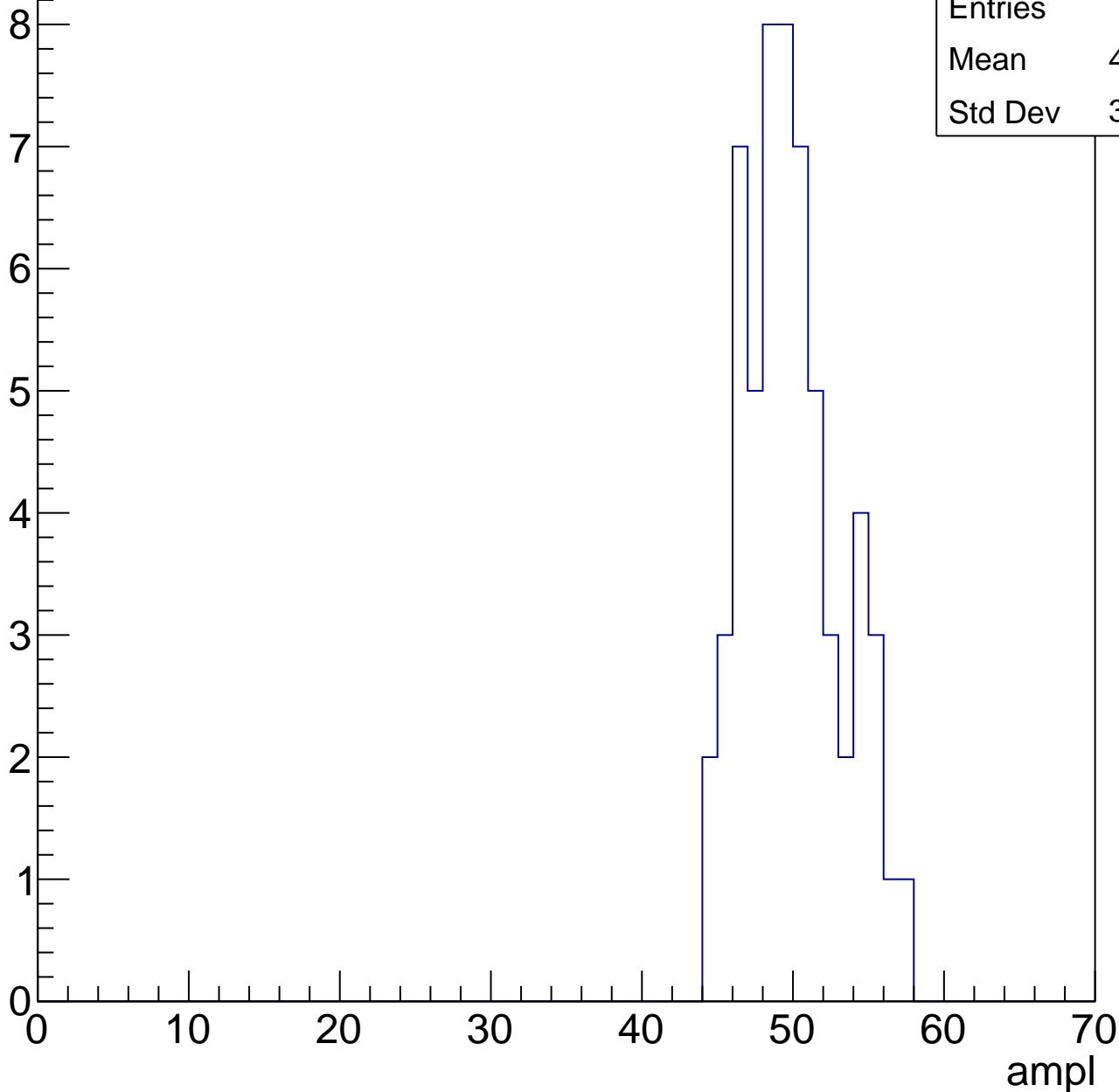


# B1L103S, U2-ch5, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	49.44
Std Dev	3.148

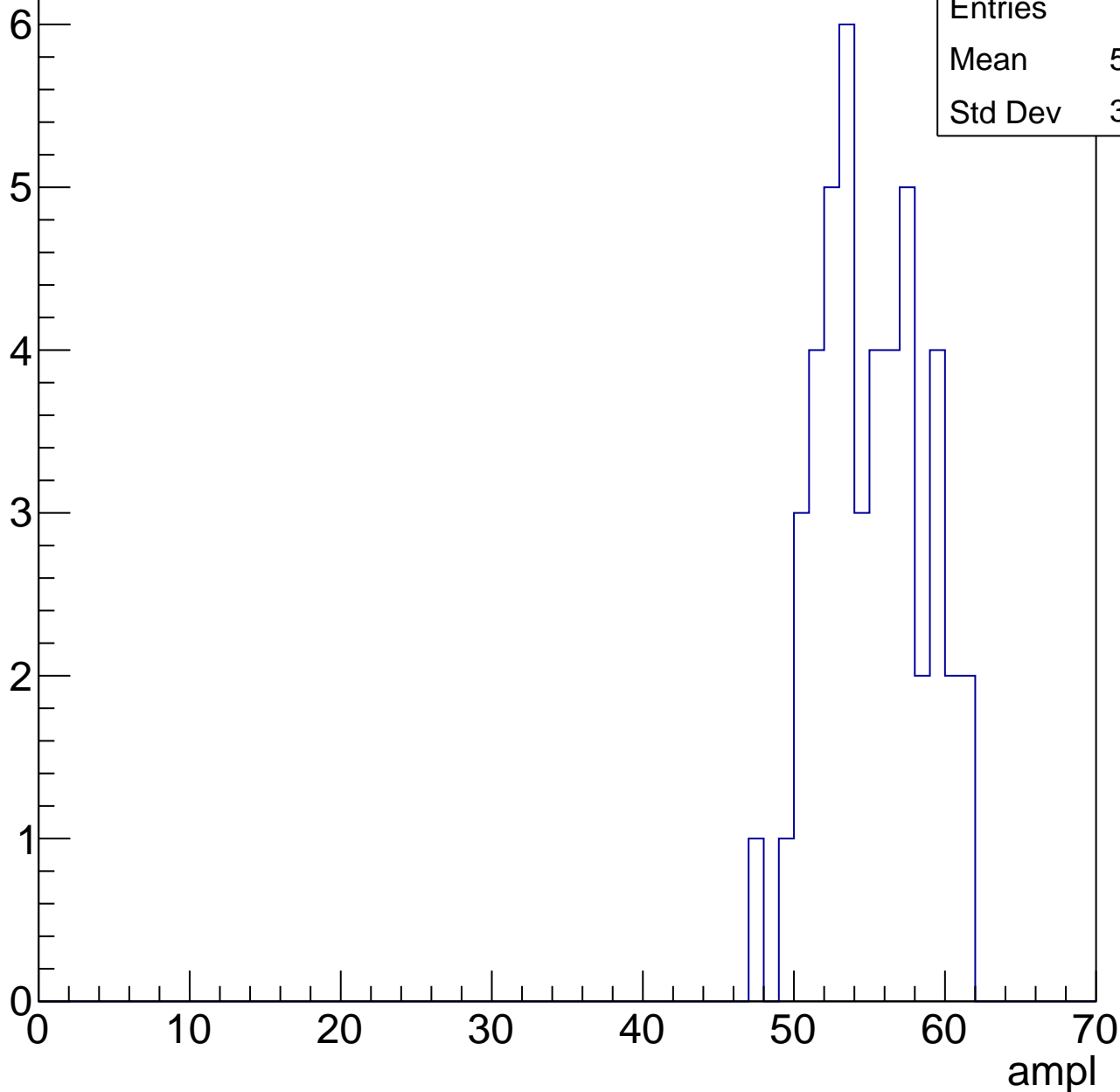


# B1L103S, U2-ch5, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	46
Mean	54.63
Std Dev	3.403



# B1L103S, U2-ch5, adc5

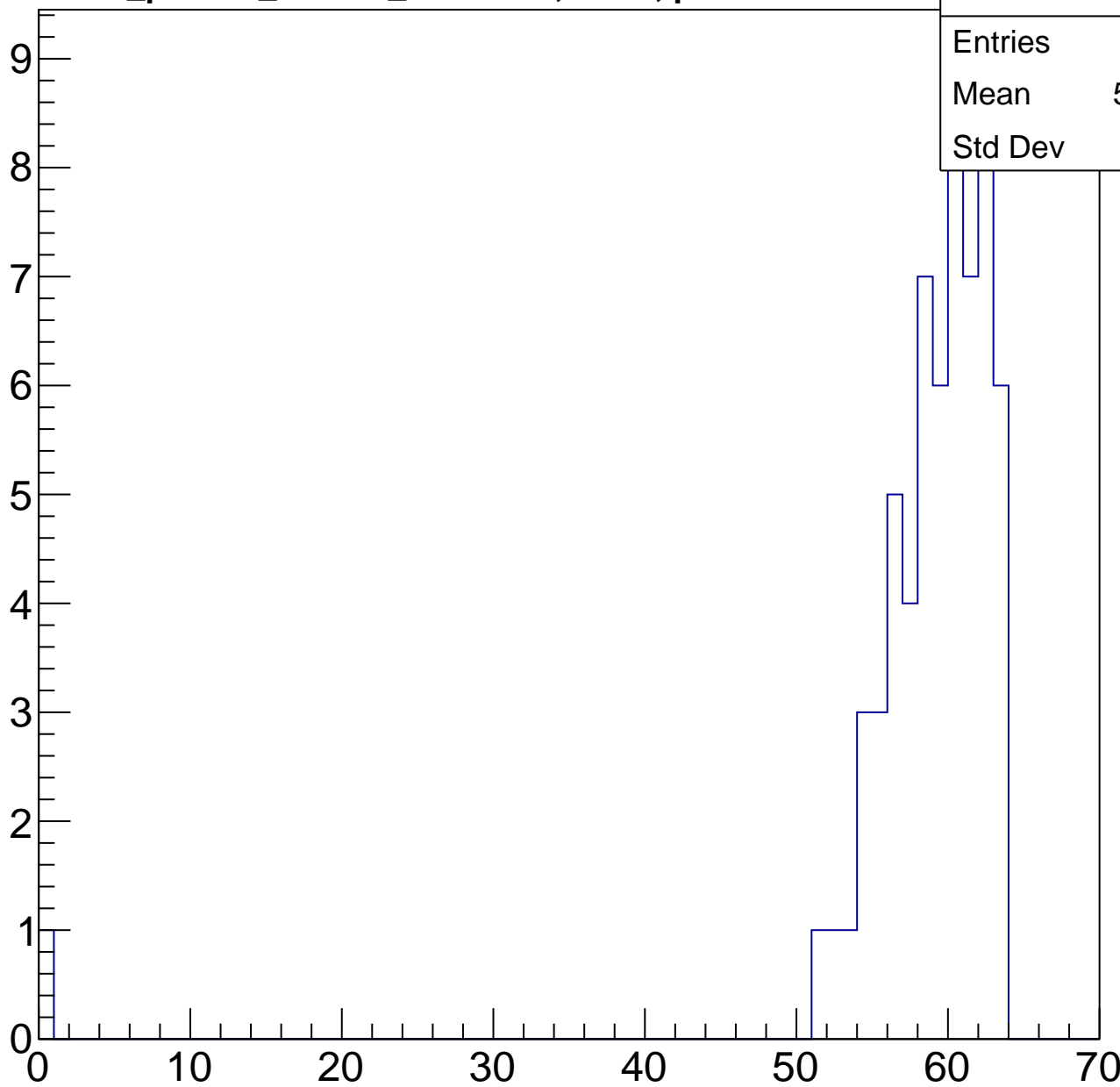
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	62
Mean	57.97
Std Dev	8

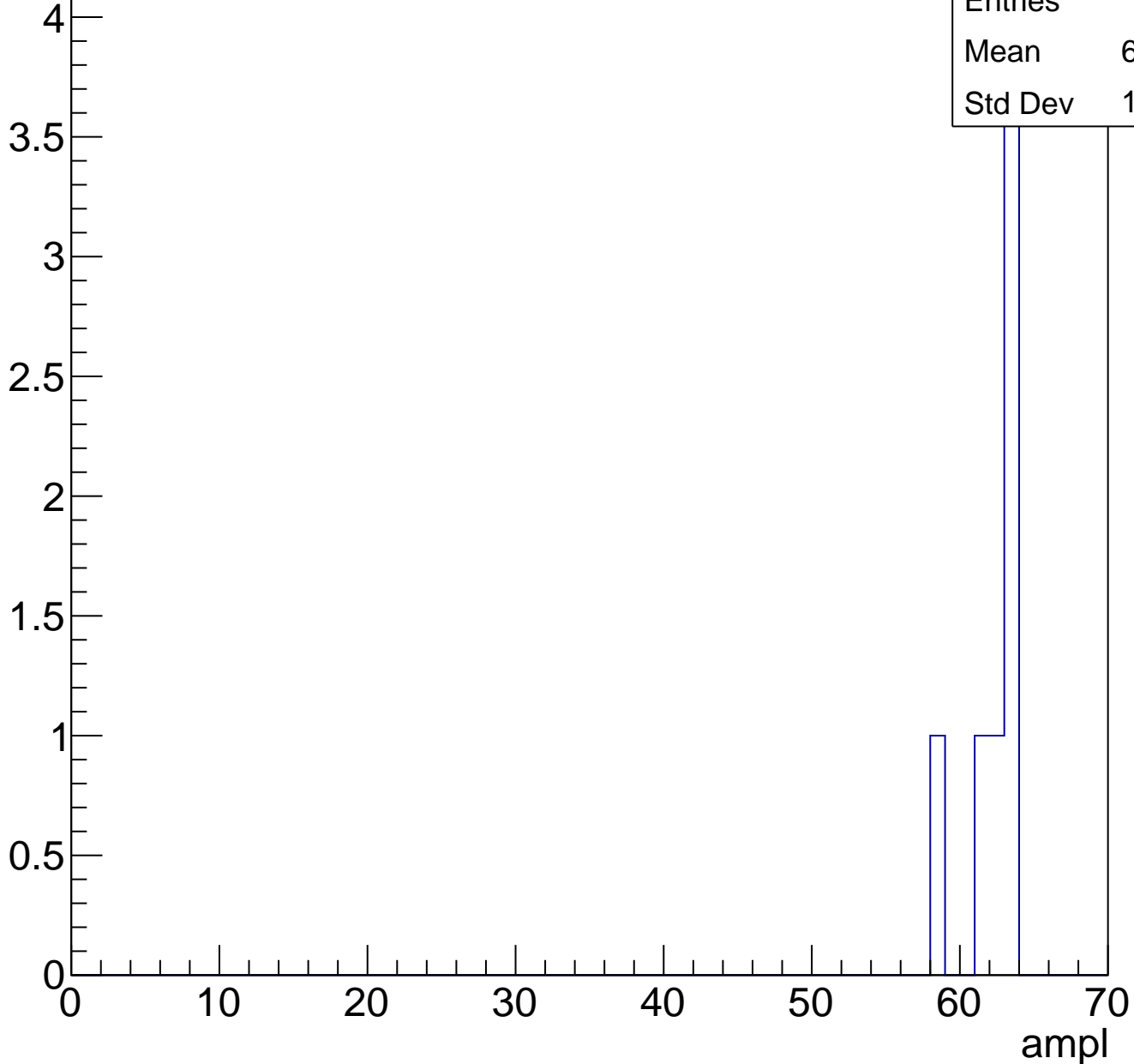
ampl



# B1L103S, U2-ch5, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U2-ch5, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch6, adc0

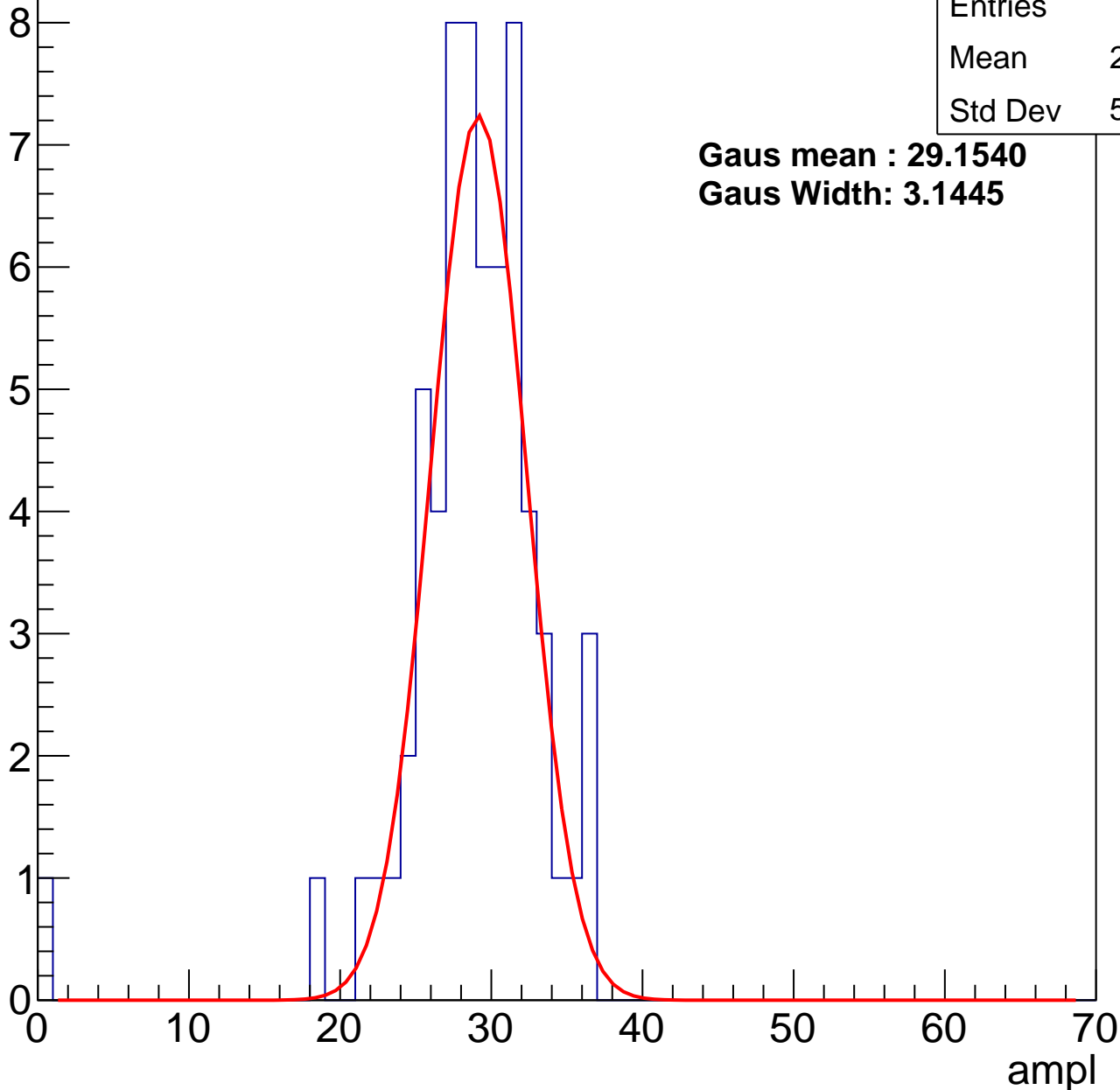
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	28.23
Std Dev	5.015

**Gaus mean : 29.1540**

**Gaus Width: 3.1445**



# B1L103S, U2-ch6, adc1

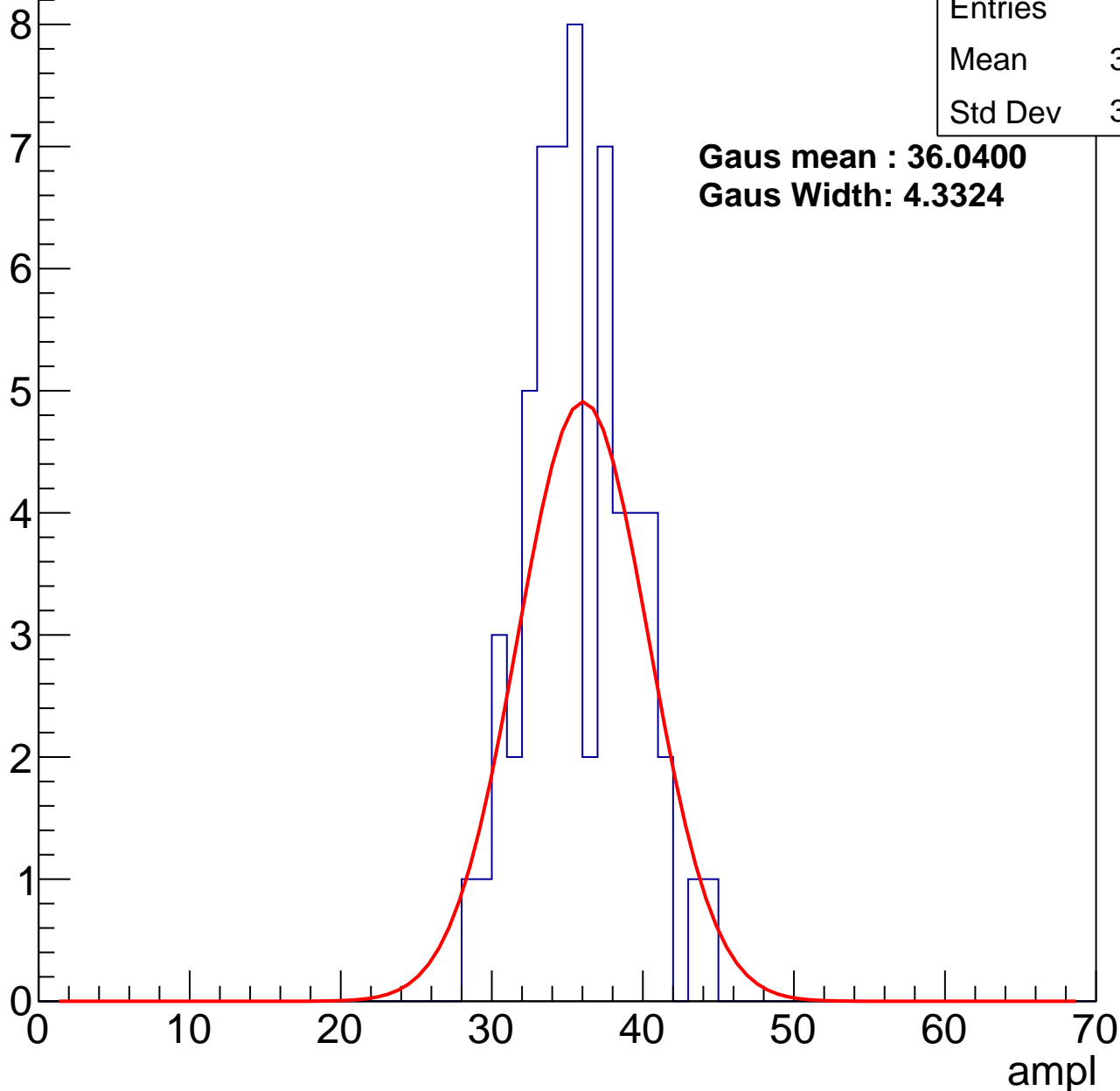
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	35.36
Std Dev	3.473

**Gaus mean : 36.0400**

**Gaus Width: 4.3324**



# B1L103S, U2-ch6, adc2

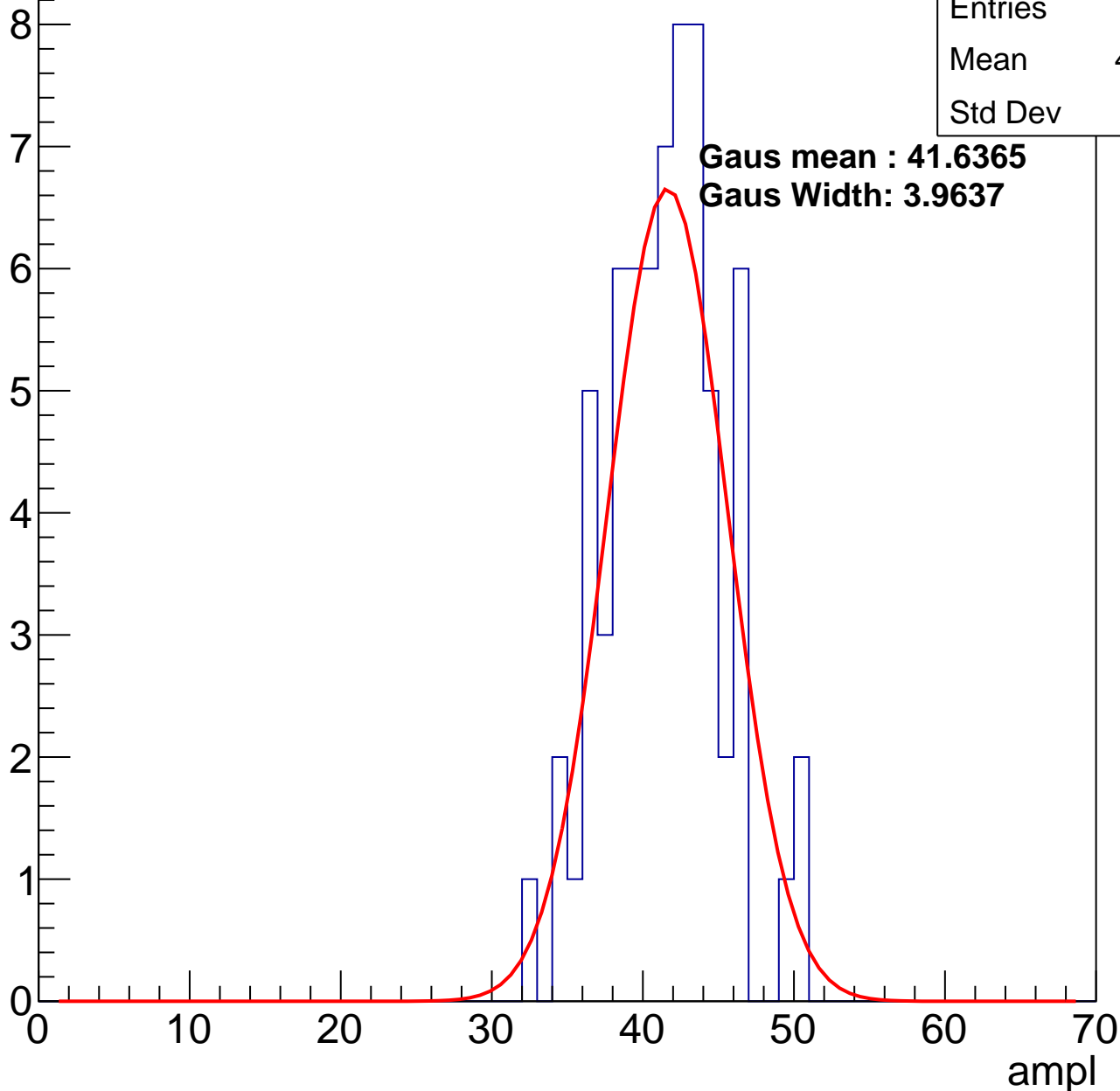
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	41.01
Std Dev	3.74

**Gaus mean : 41.6365**

**Gaus Width: 3.9637**

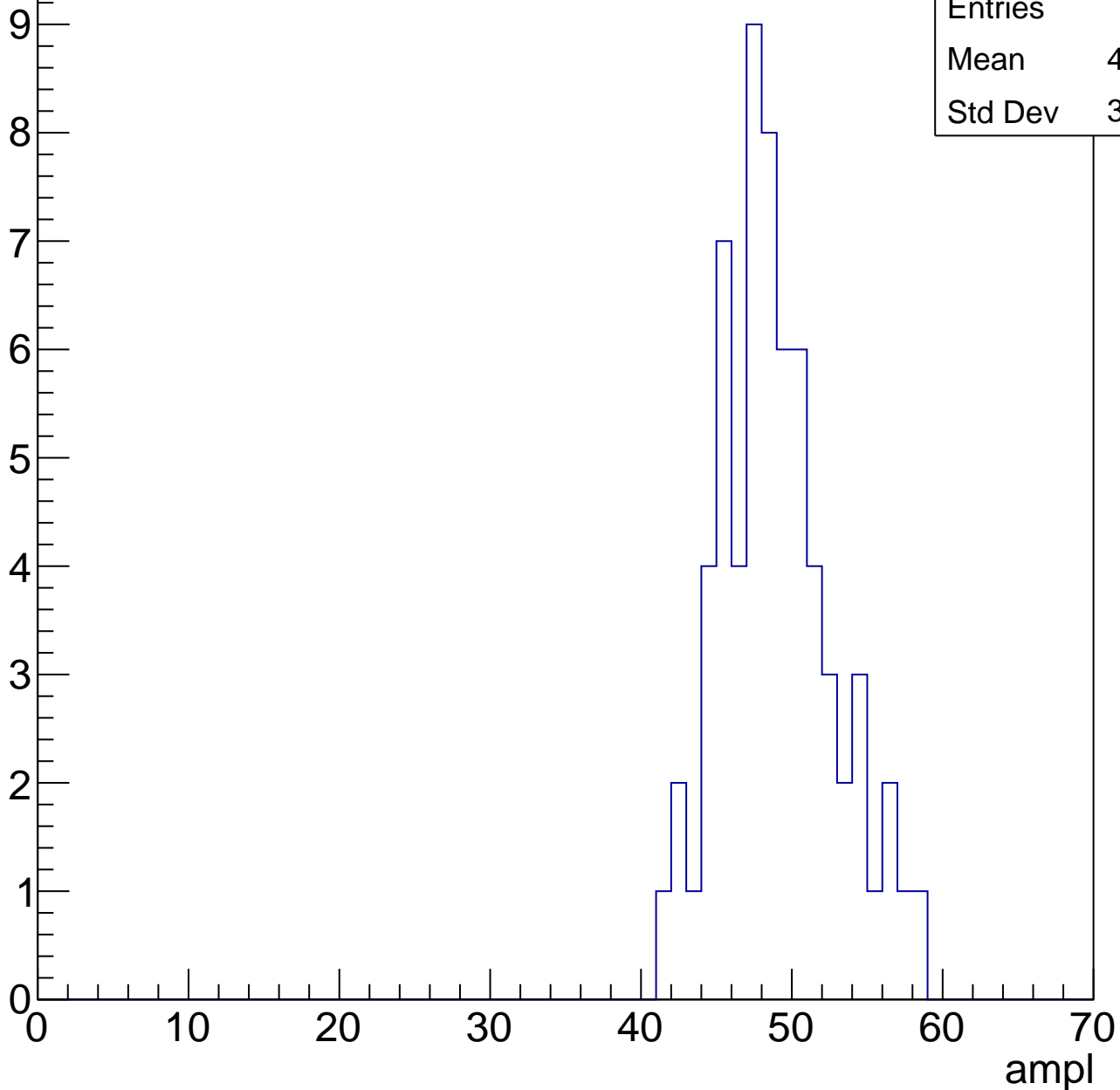


# B1L103S, U2-ch6, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	48.52
Std Dev	3.742

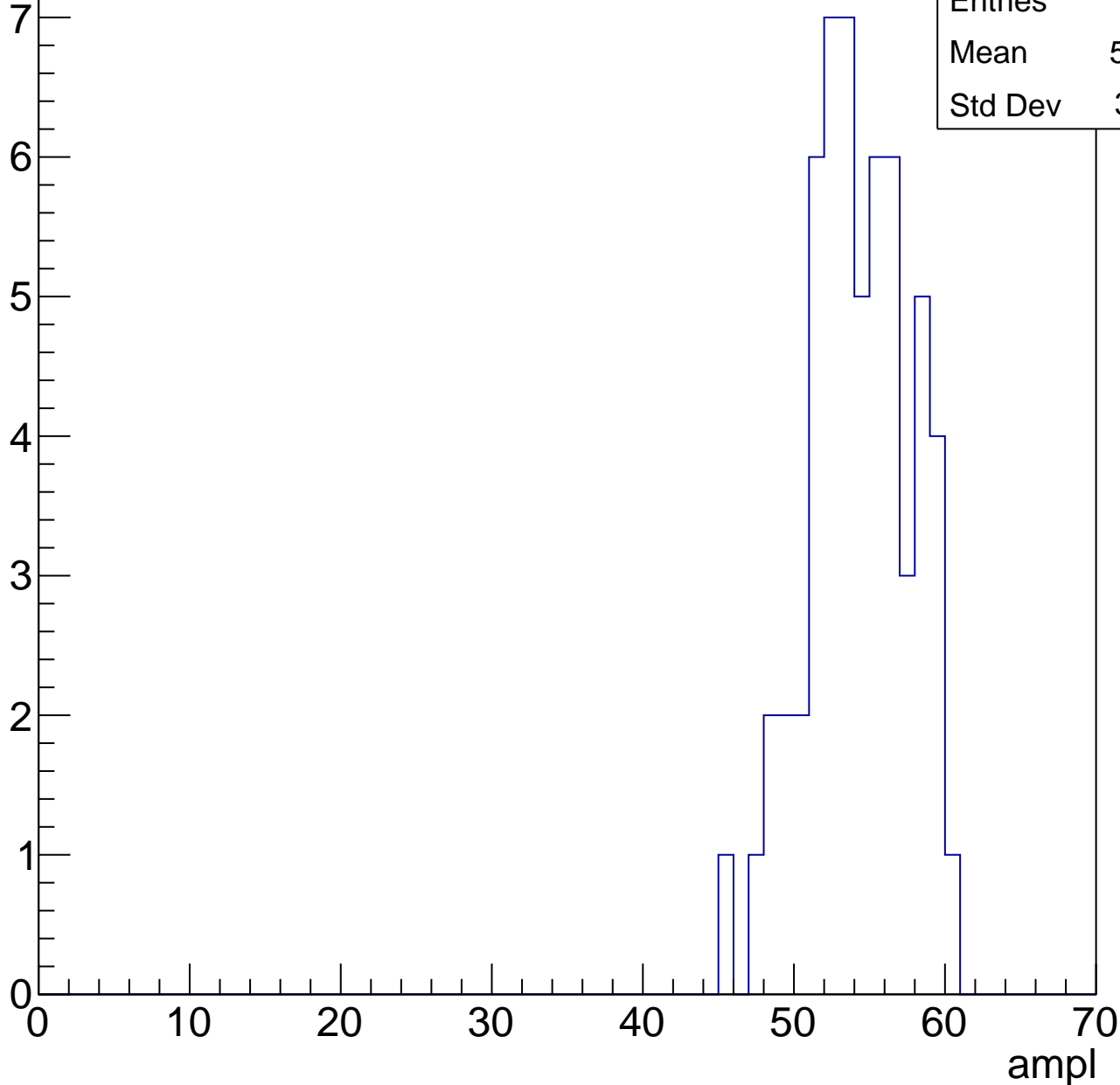


# B1L103S, U2-ch6, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	53.79
Std Dev	3.331



# B1L103S, U2-ch6, adc5

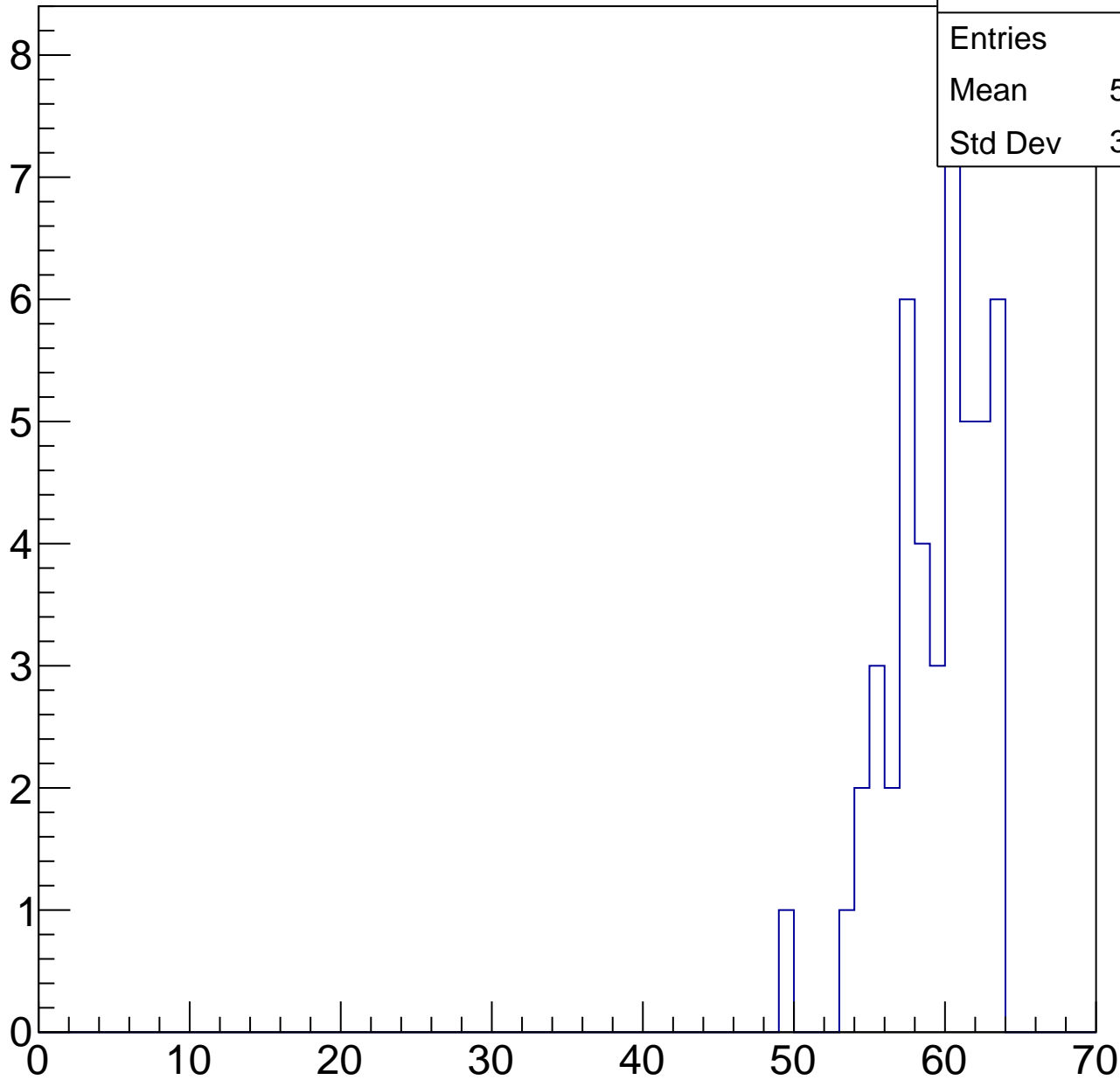
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	46
Mean	58.93
Std Dev	3.124

ampl

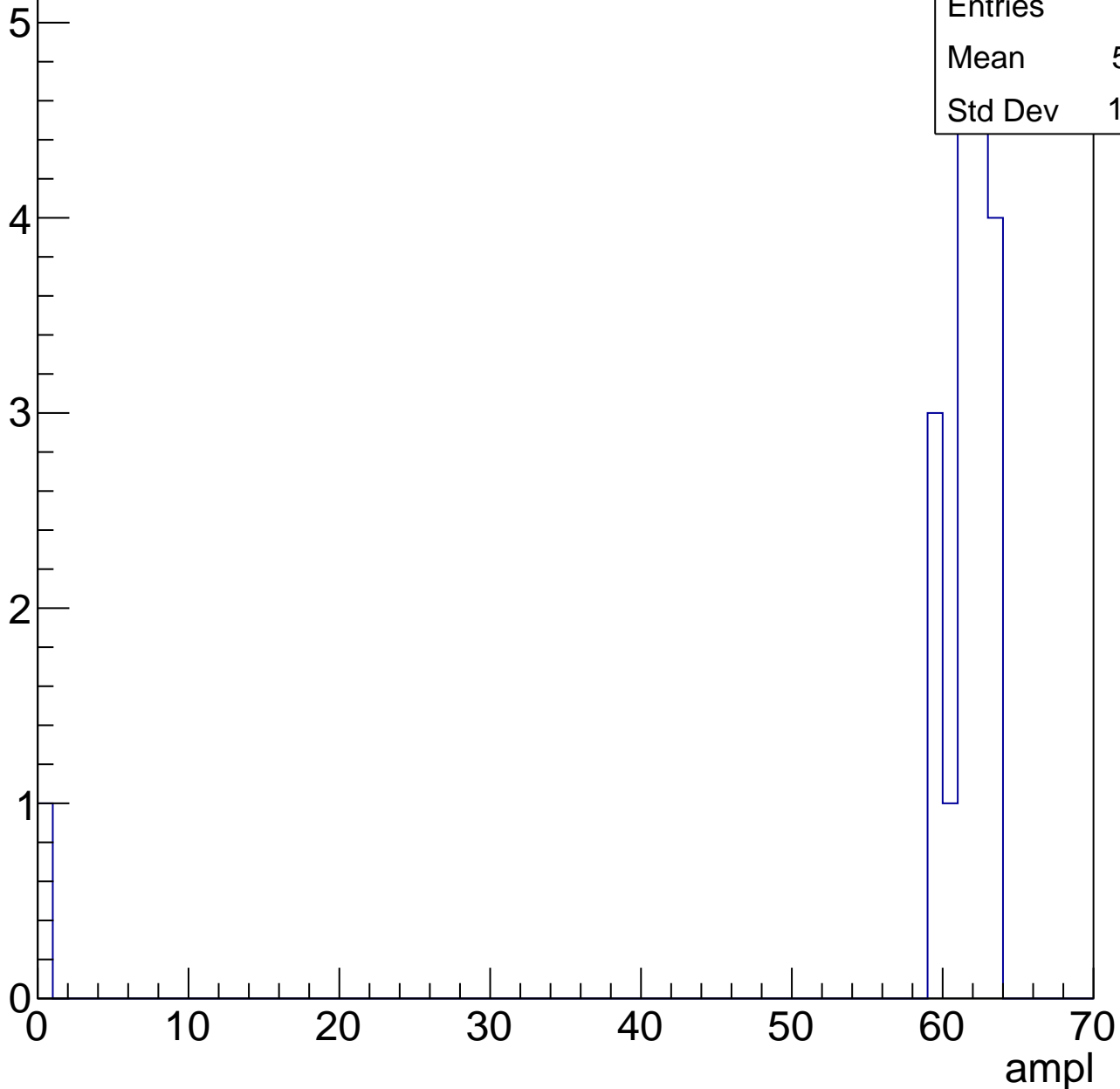


# B1L103S, U2-ch6, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	19
Mean	58.11
Std Dev	13.76





# B1L103S, U2-ch6, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U2-ch7, adc0

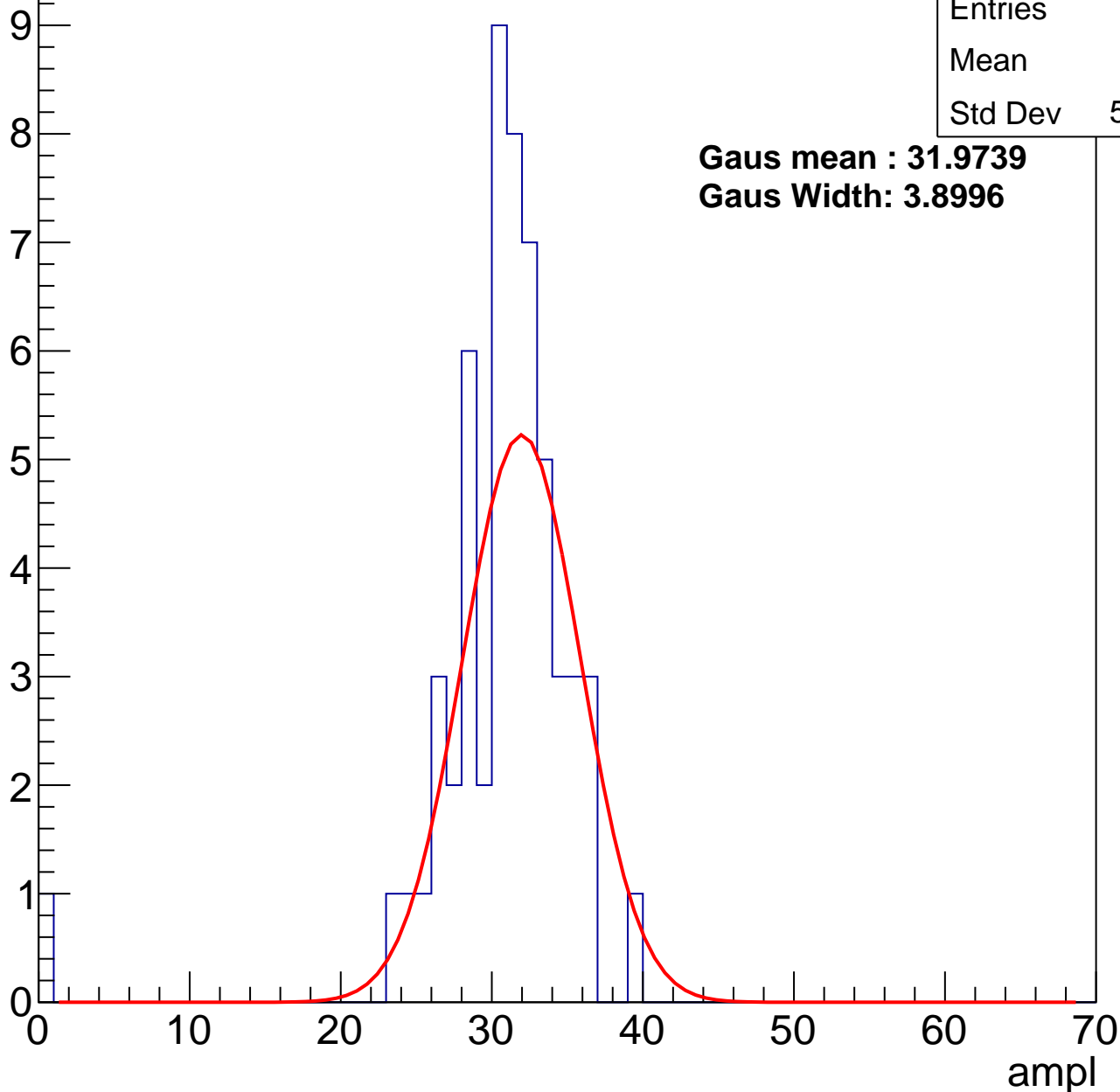
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	30.2
Std Dev	5.163

**Gaus mean : 31.9739**

**Gaus Width: 3.8996**



# B1L103S, U2-ch7, adc1

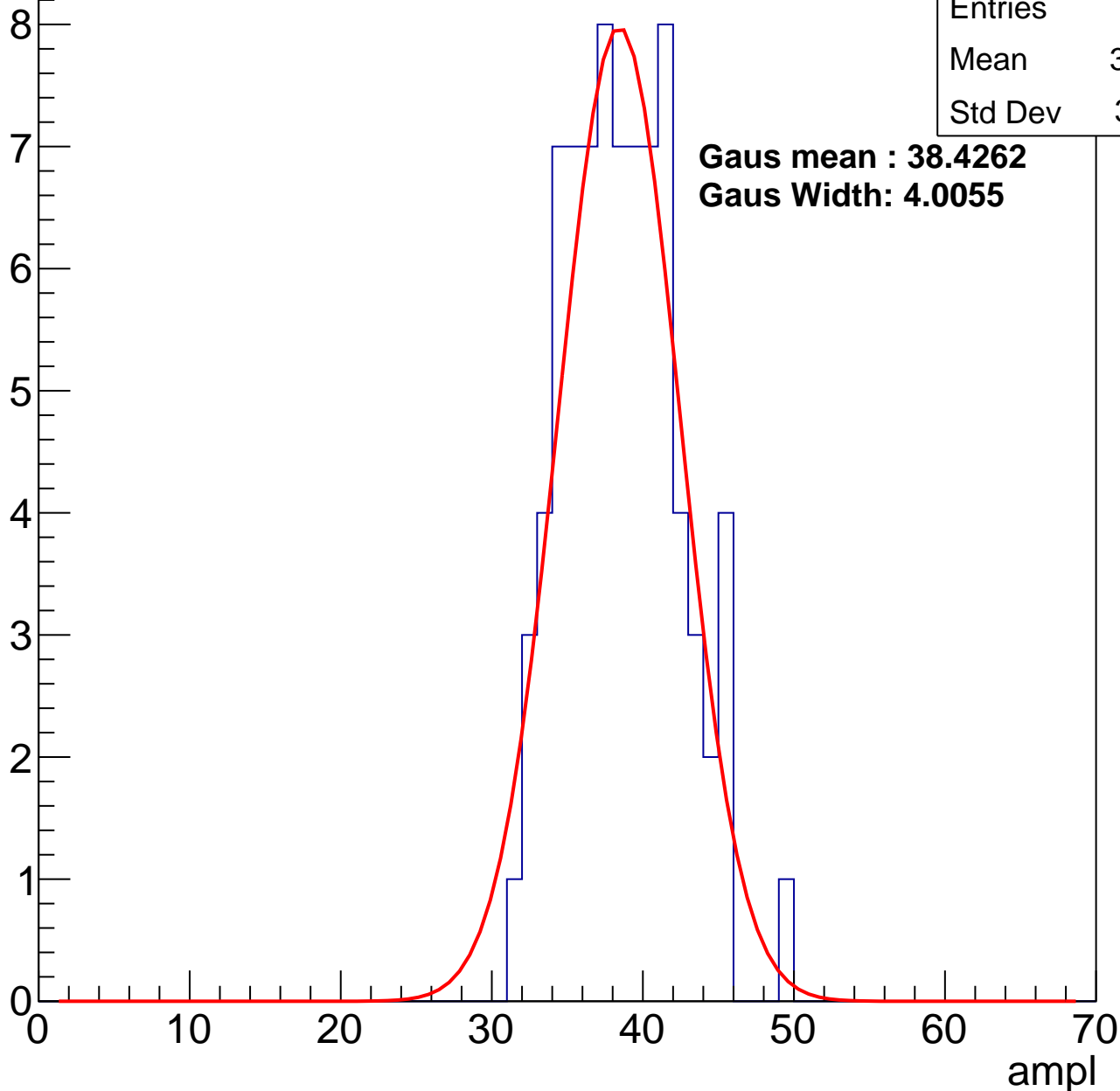
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	80
Mean	38.14
Std Dev	3.711

**Gaus mean : 38.4262**

**Gaus Width: 4.0055**



# B1L103S, U2-ch7, adc2

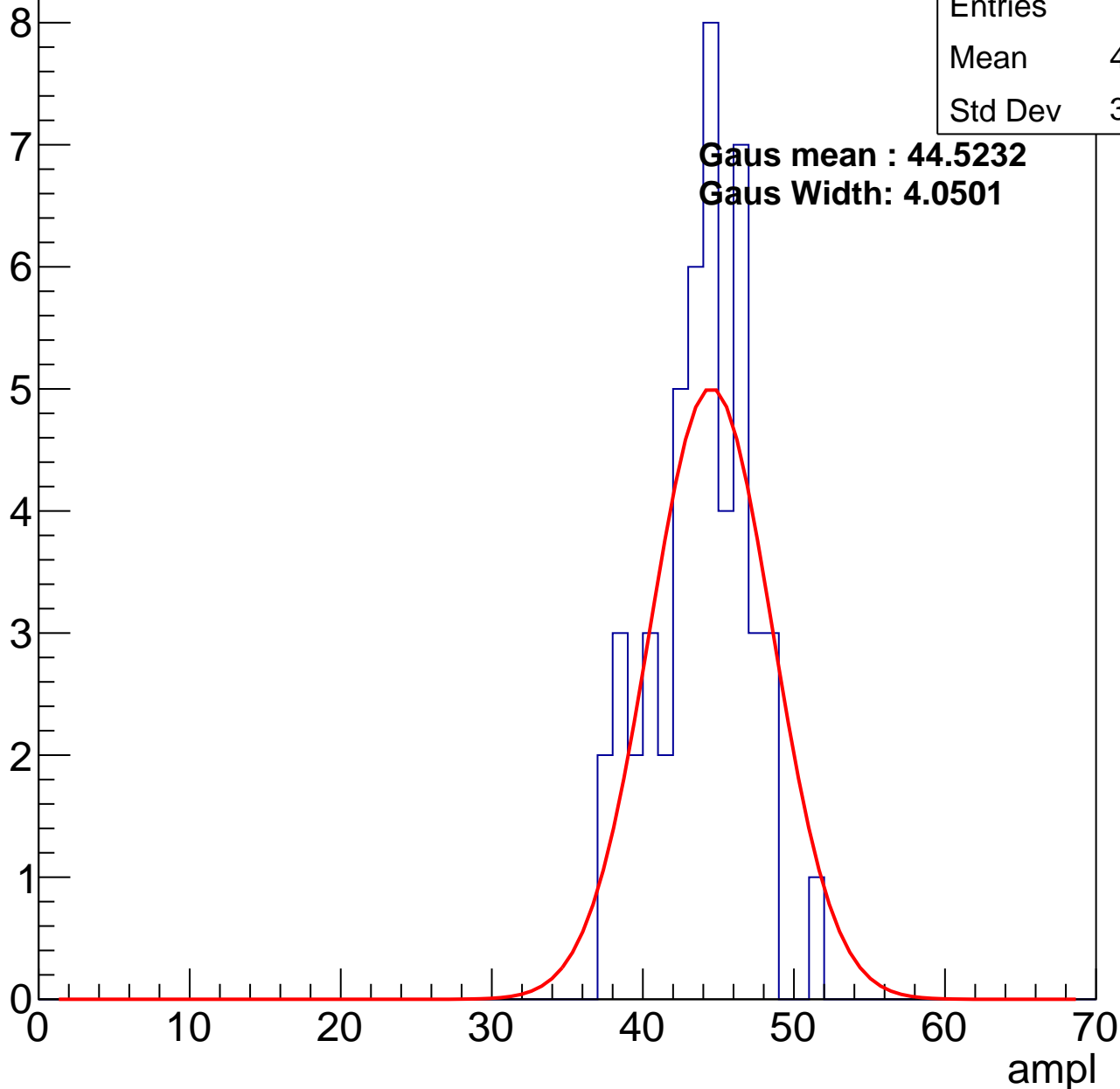
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	43.39
Std Dev	3.148

**Gaus mean : 44.5232**

**Gaus Width: 4.0501**

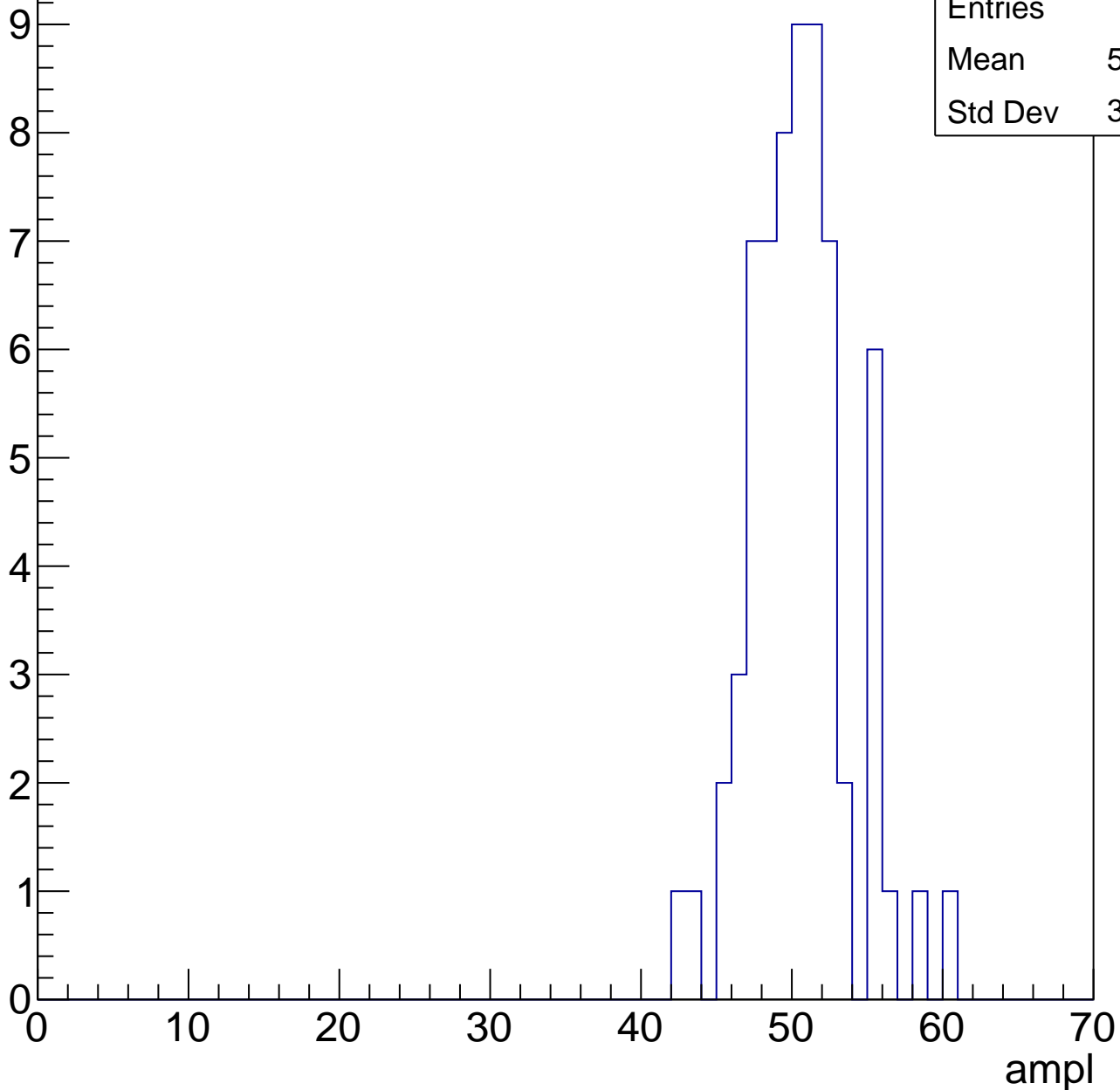


# B1L103S, U2-ch7, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	50.05
Std Dev	3.316



# B1L103S, U2-ch7, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

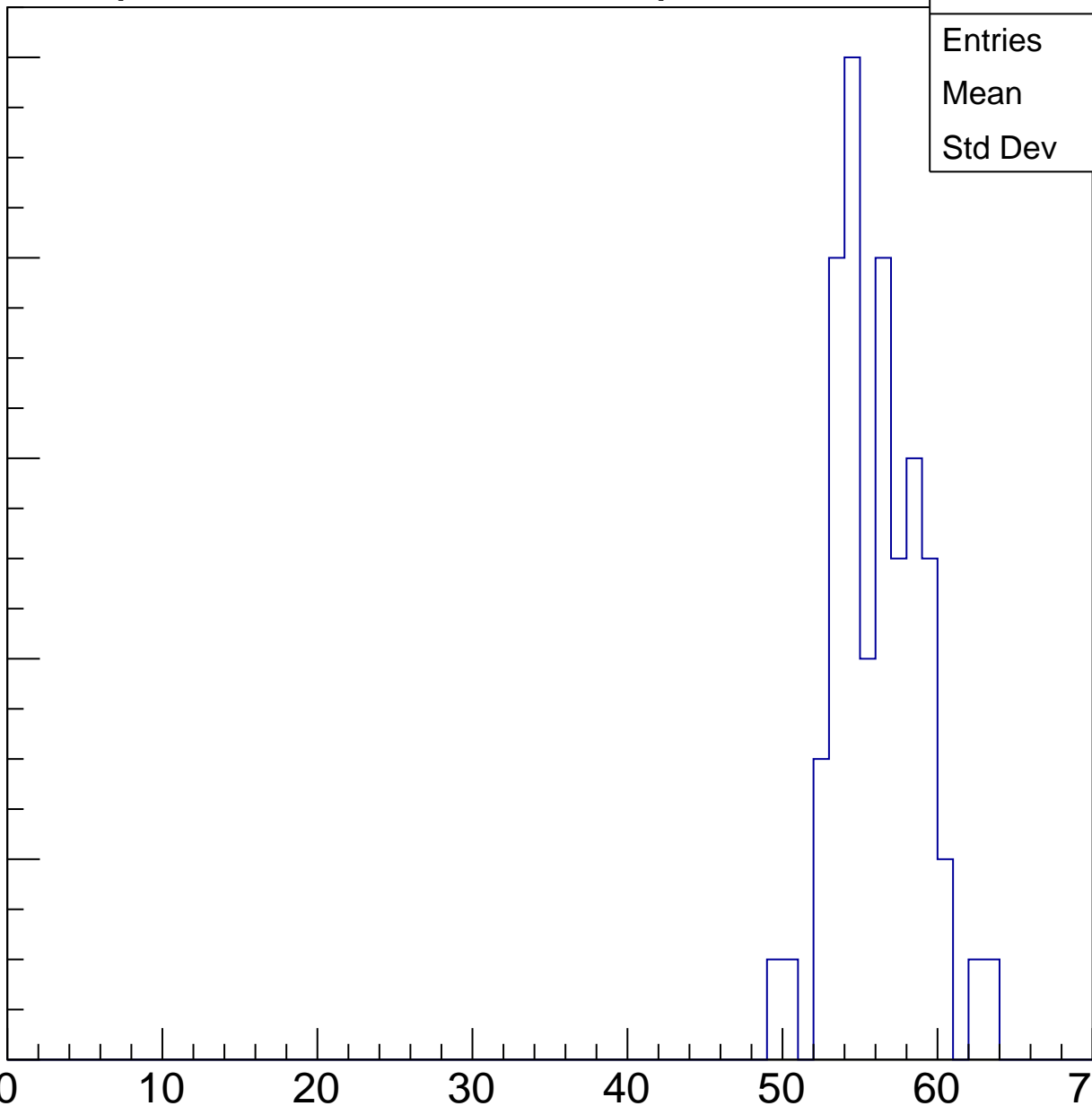
Entries	55
Mean	55.64
Std Dev	2.805

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

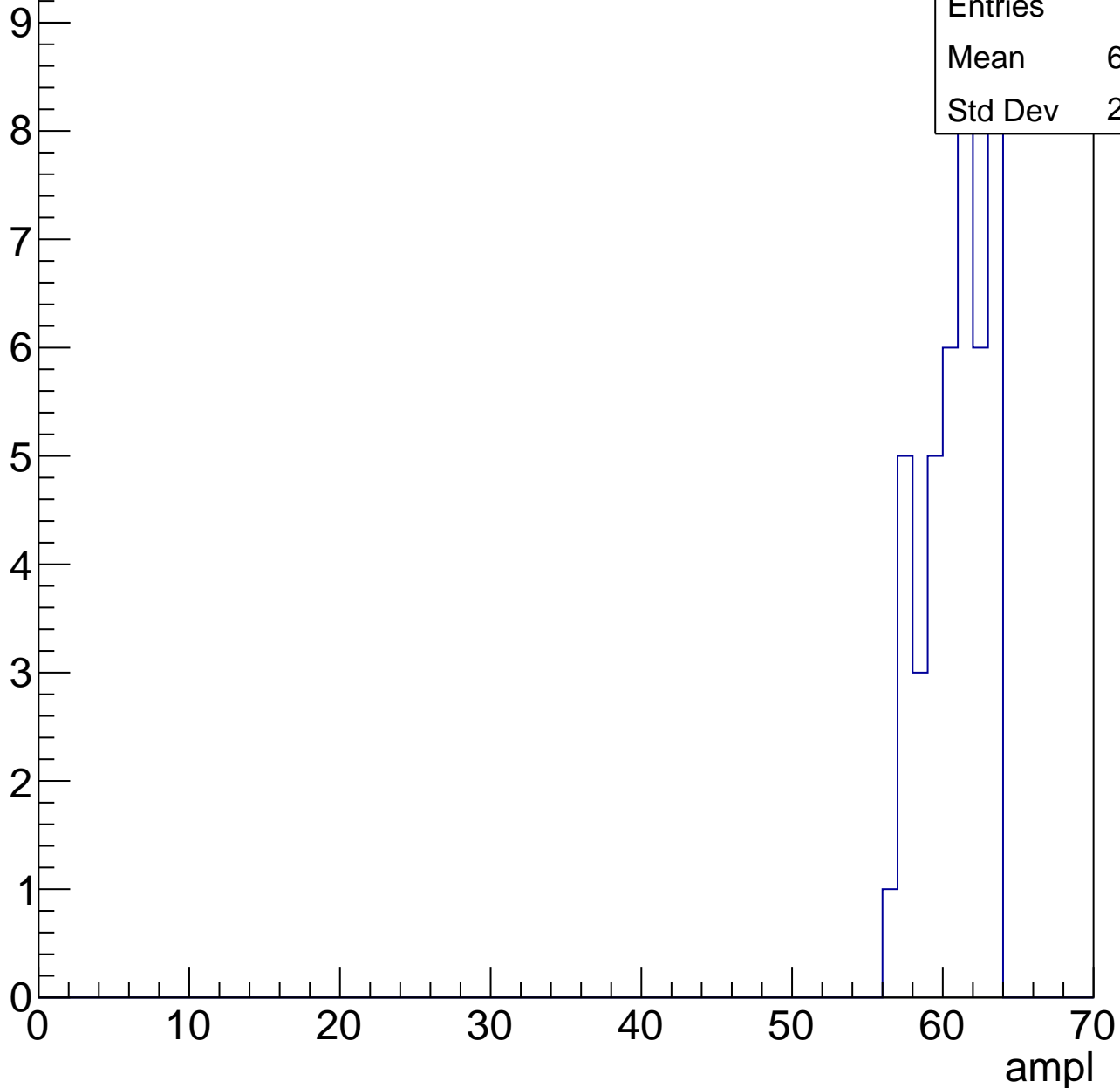
ampl



# B1L103S, U2-ch7, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

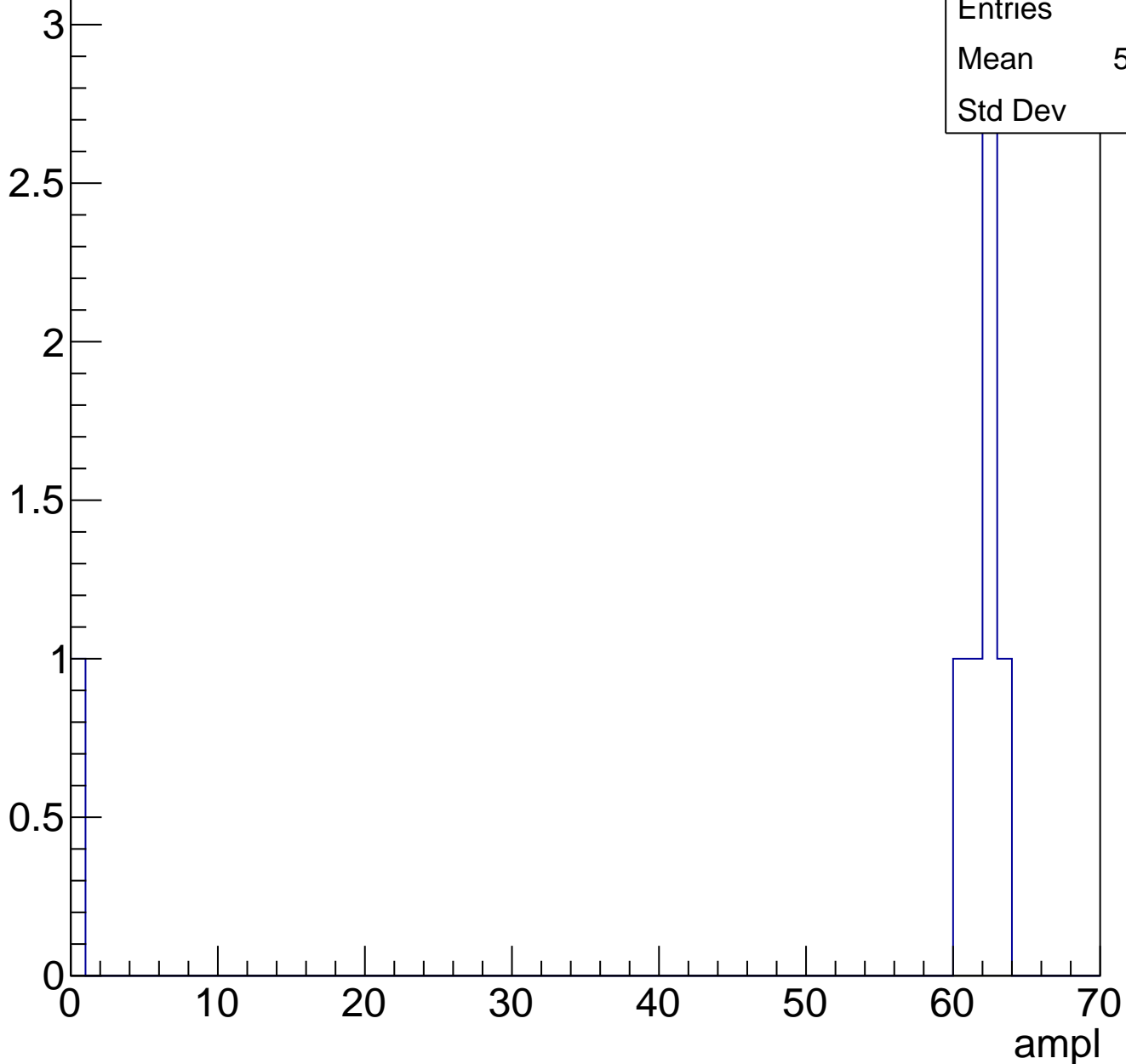
Entry



# B1L103S, U2-ch7, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U2-ch7, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U2-ch8, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	77
Mean	30.3
Std Dev	3.618

**Gaus mean : 30.8935**

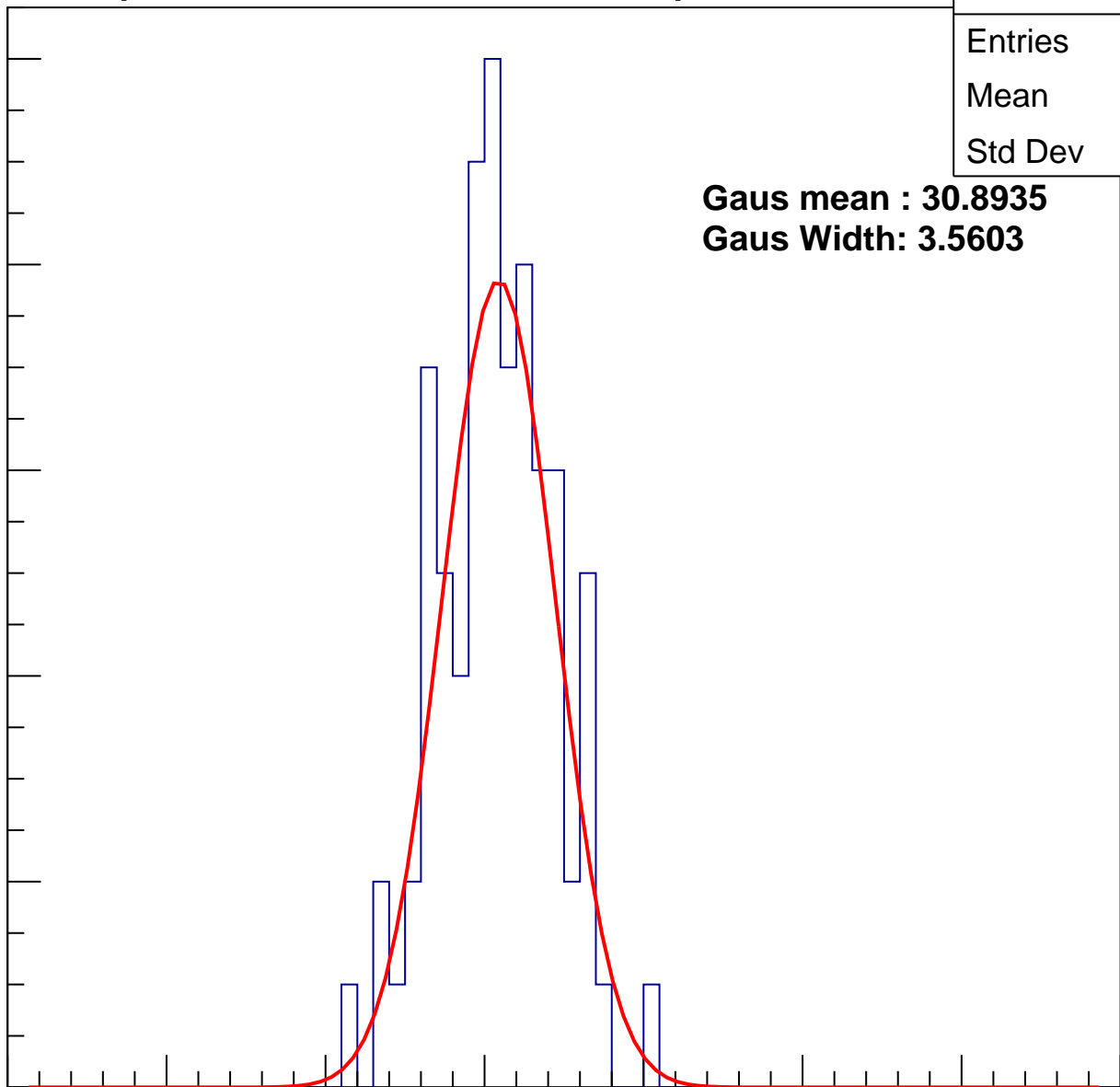
**Gaus Width: 3.5603**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U2-ch8, adc1

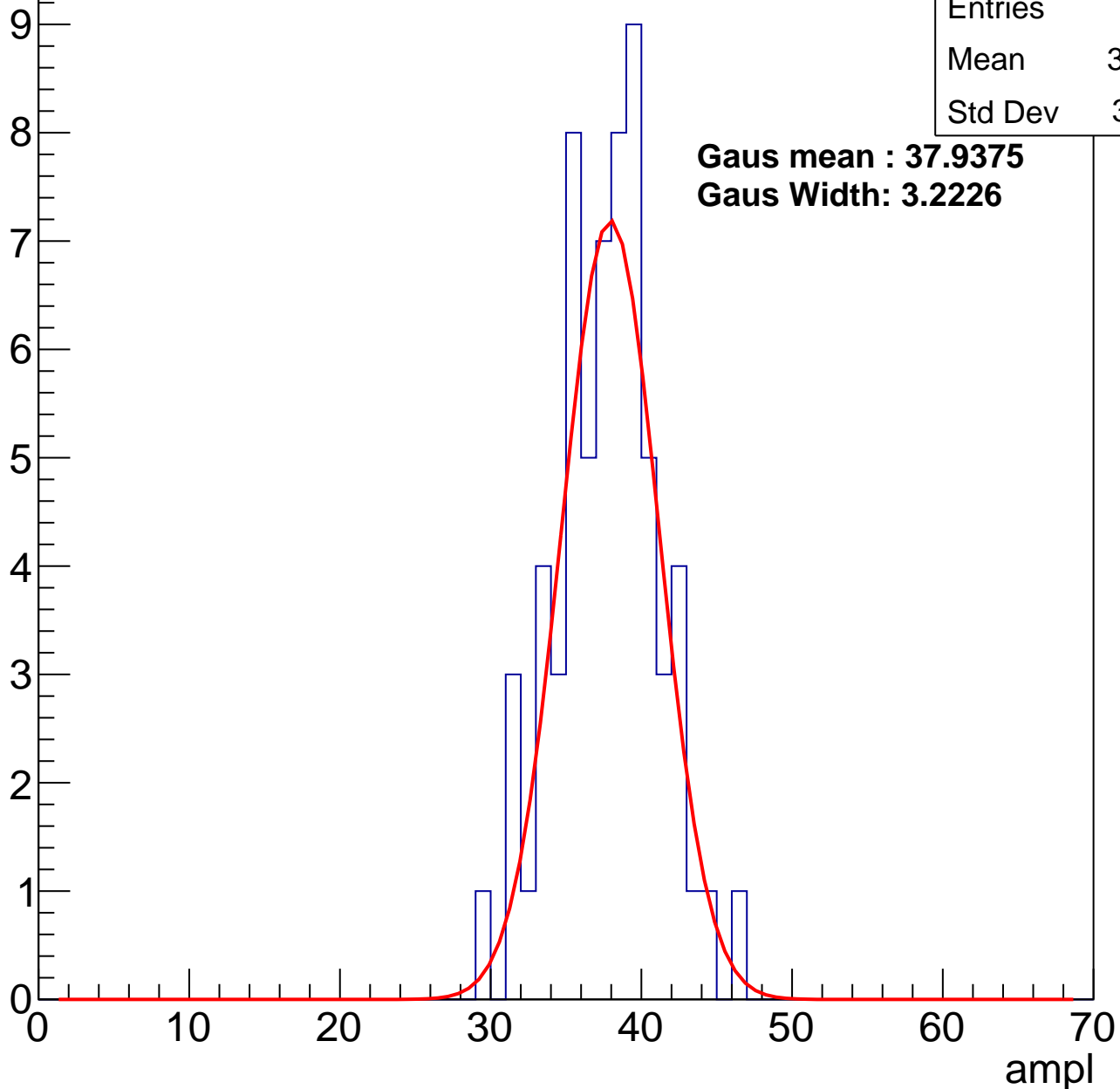
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	37.28
Std Dev	3.361

**Gaus mean : 37.9375**

**Gaus Width: 3.2226**



# B1L103S, U2-ch8, adc2

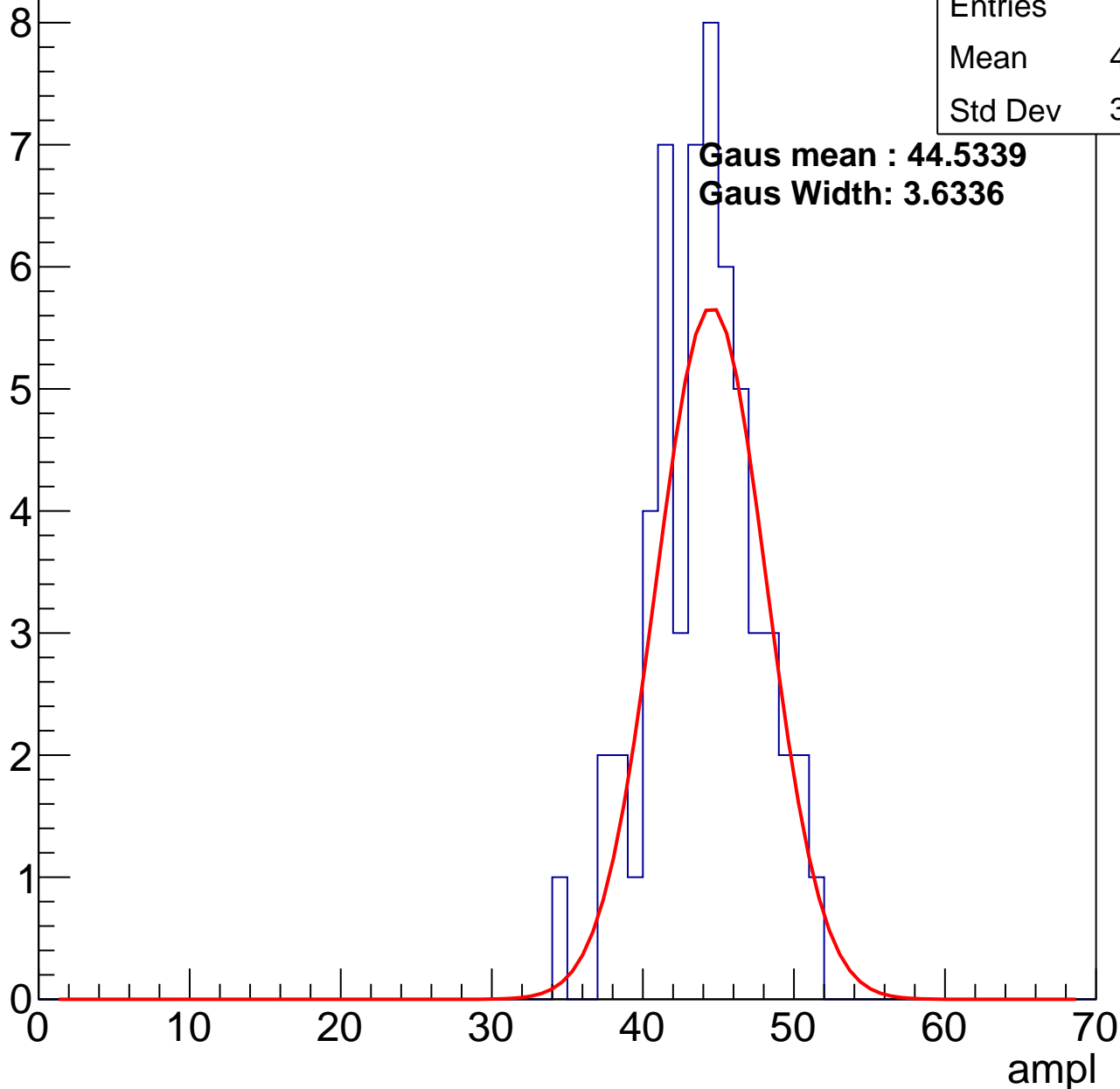
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	43.56
Std Dev	3.509

**Gaus mean : 44.5339**

**Gaus Width: 3.6336**

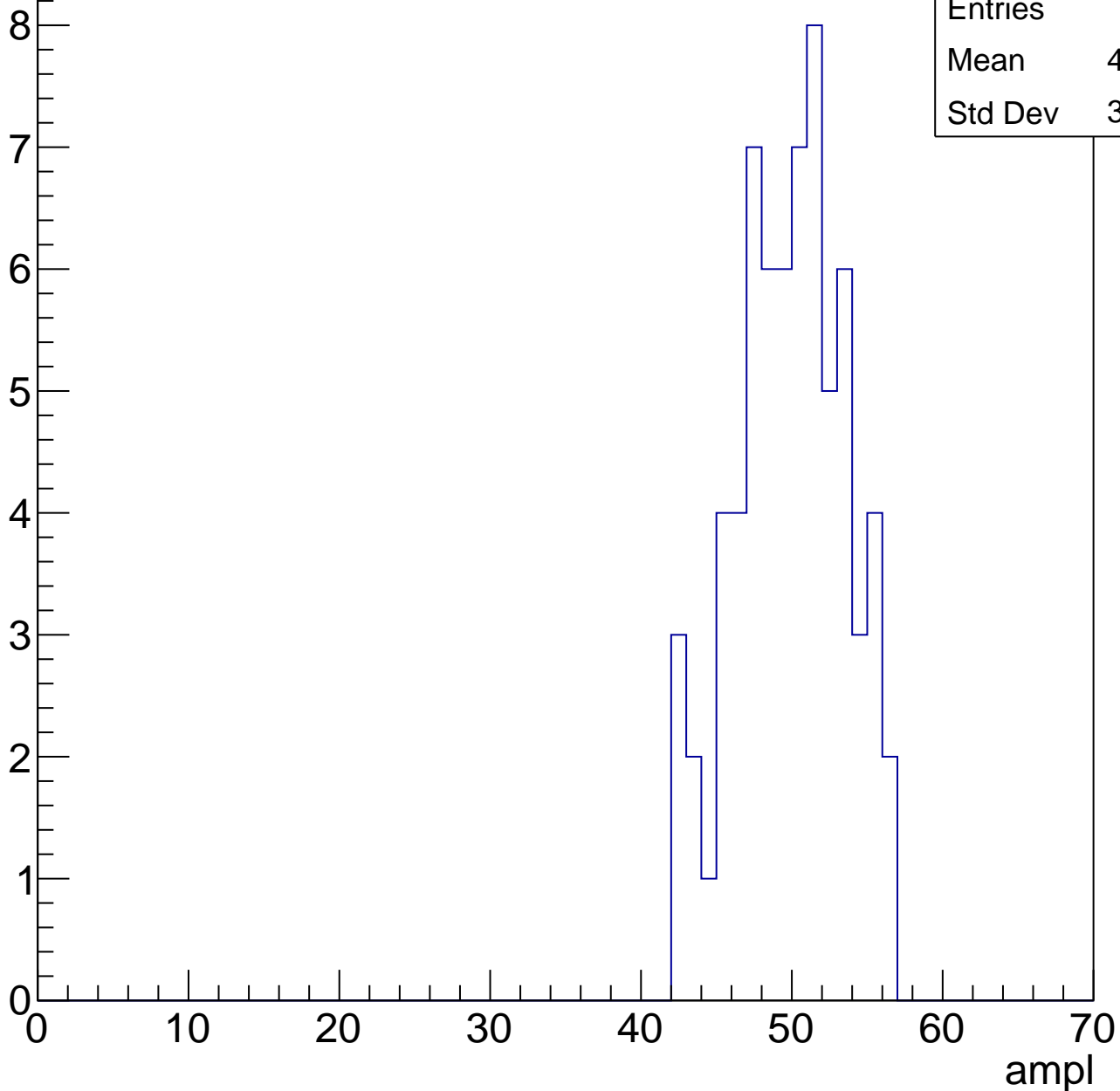


# B1L103S, U2-ch8, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	49.43
Std Dev	3.562

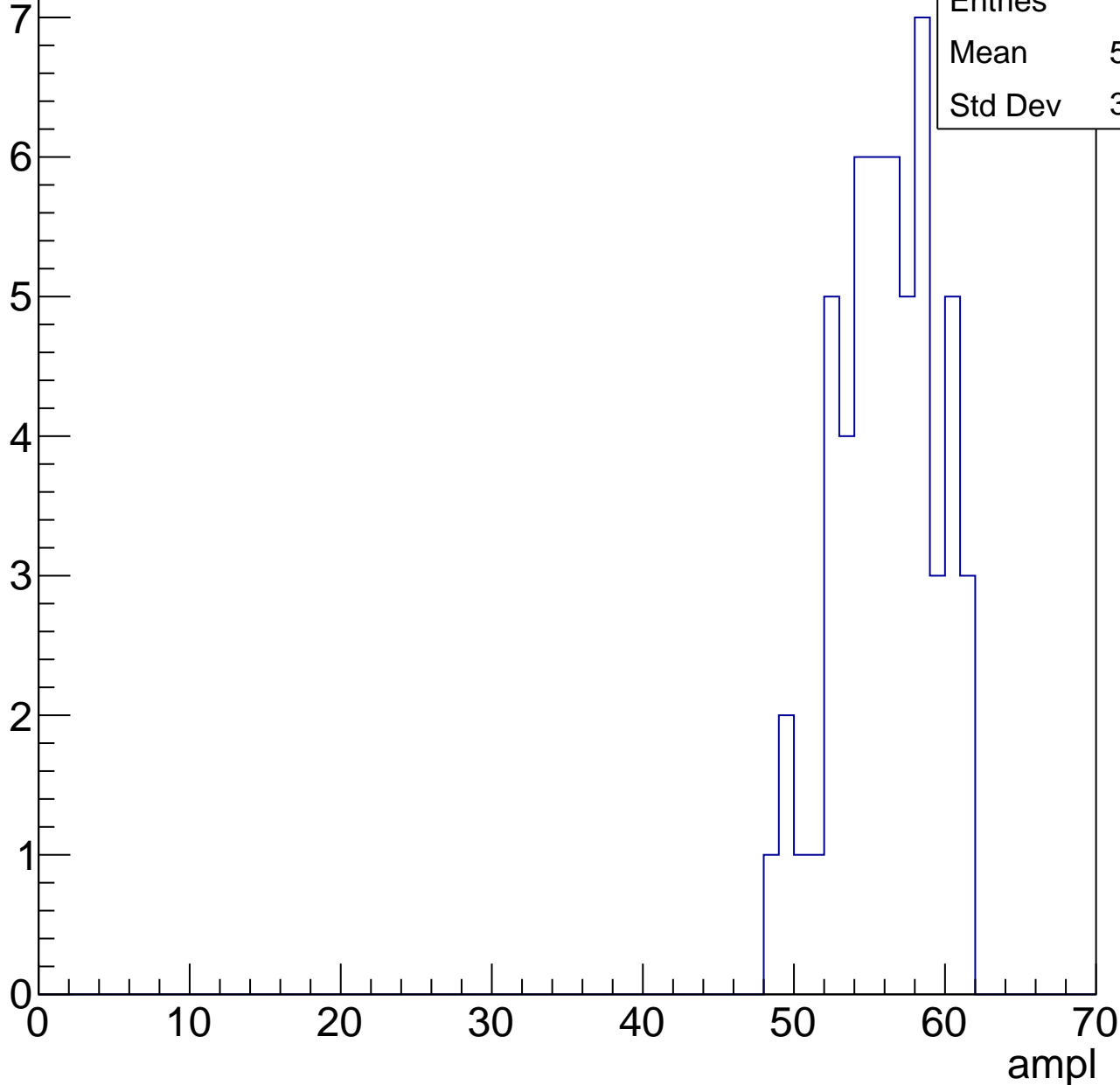


# B1L103S, U2-ch8, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	55.64
Std Dev	3.238



# B1L103S, U2-ch8, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	44
Mean	58.61
Std Dev	9.22

ampl

0

10

20

30

40

50

60

70

# B1L103S, U2-ch8, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U2-ch8, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L103S, U2-ch9, adc0

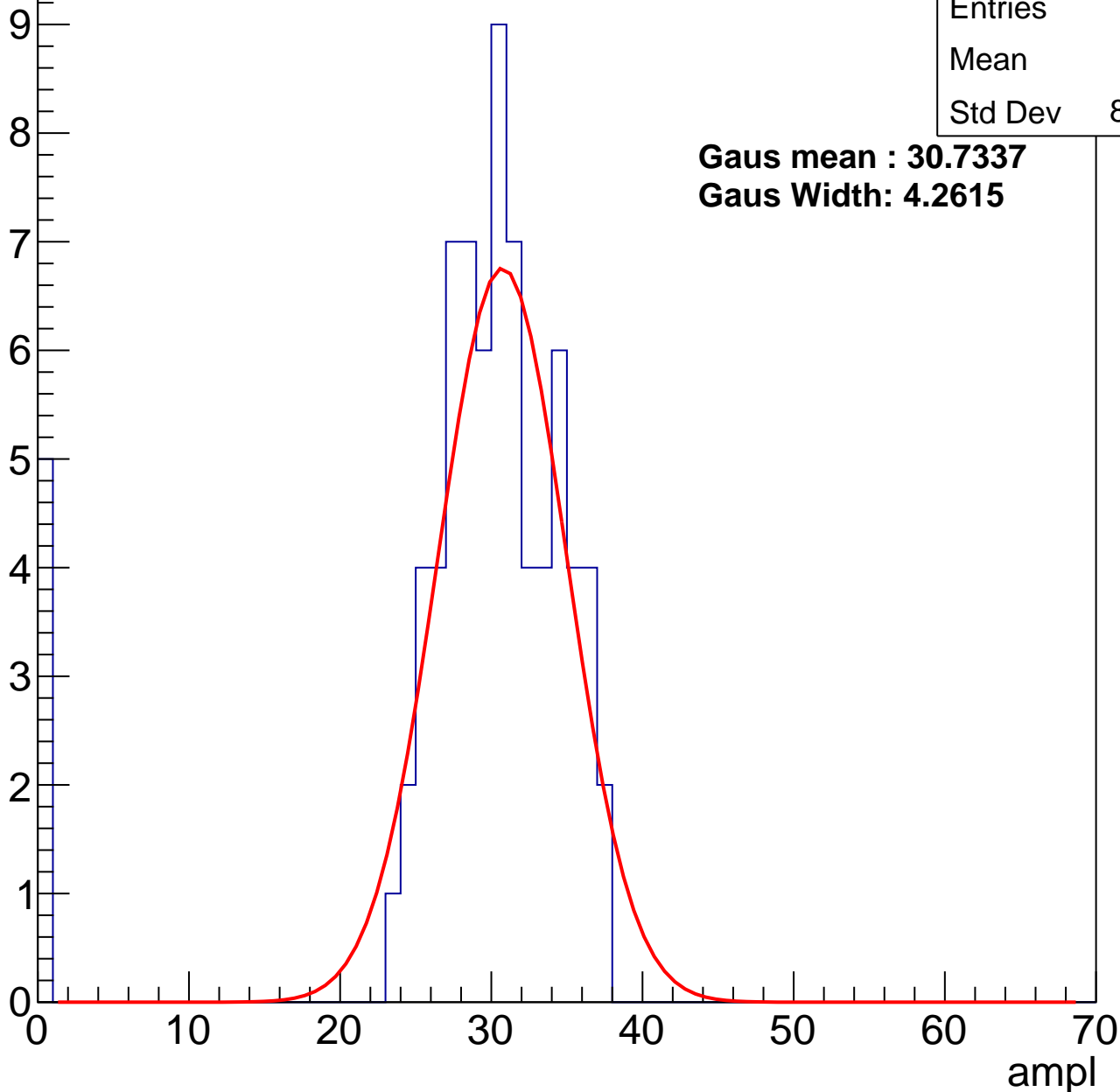
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	28.2
Std Dev	8.217

**Gaus mean : 30.7337**

**Gaus Width: 4.2615**



# B1L103S, U2-ch9, adc1

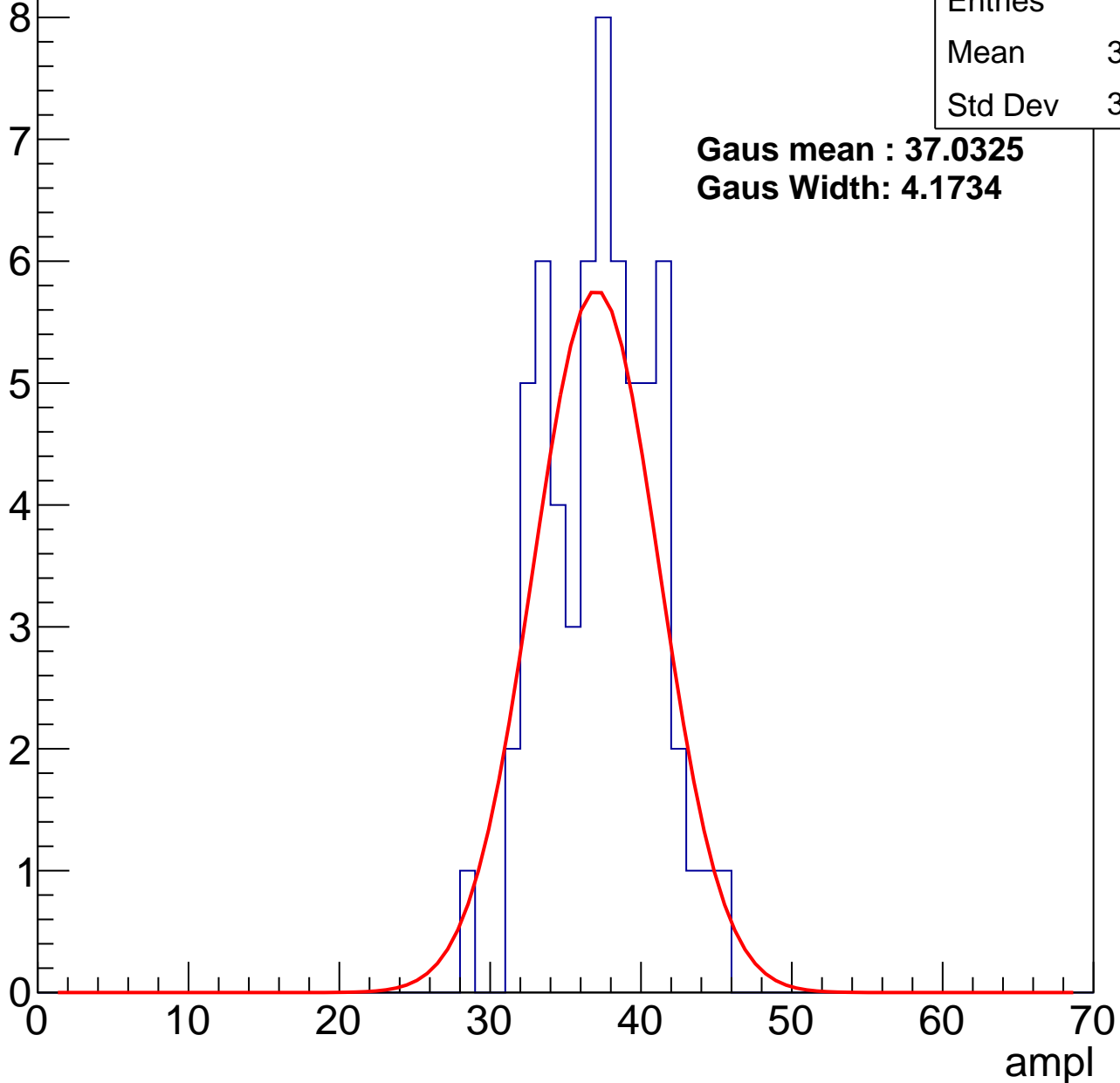
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	36.87
Std Dev	3.576

**Gaus mean : 37.0325**

**Gaus Width: 4.1734**



# B1L103S, U2-ch9, adc2

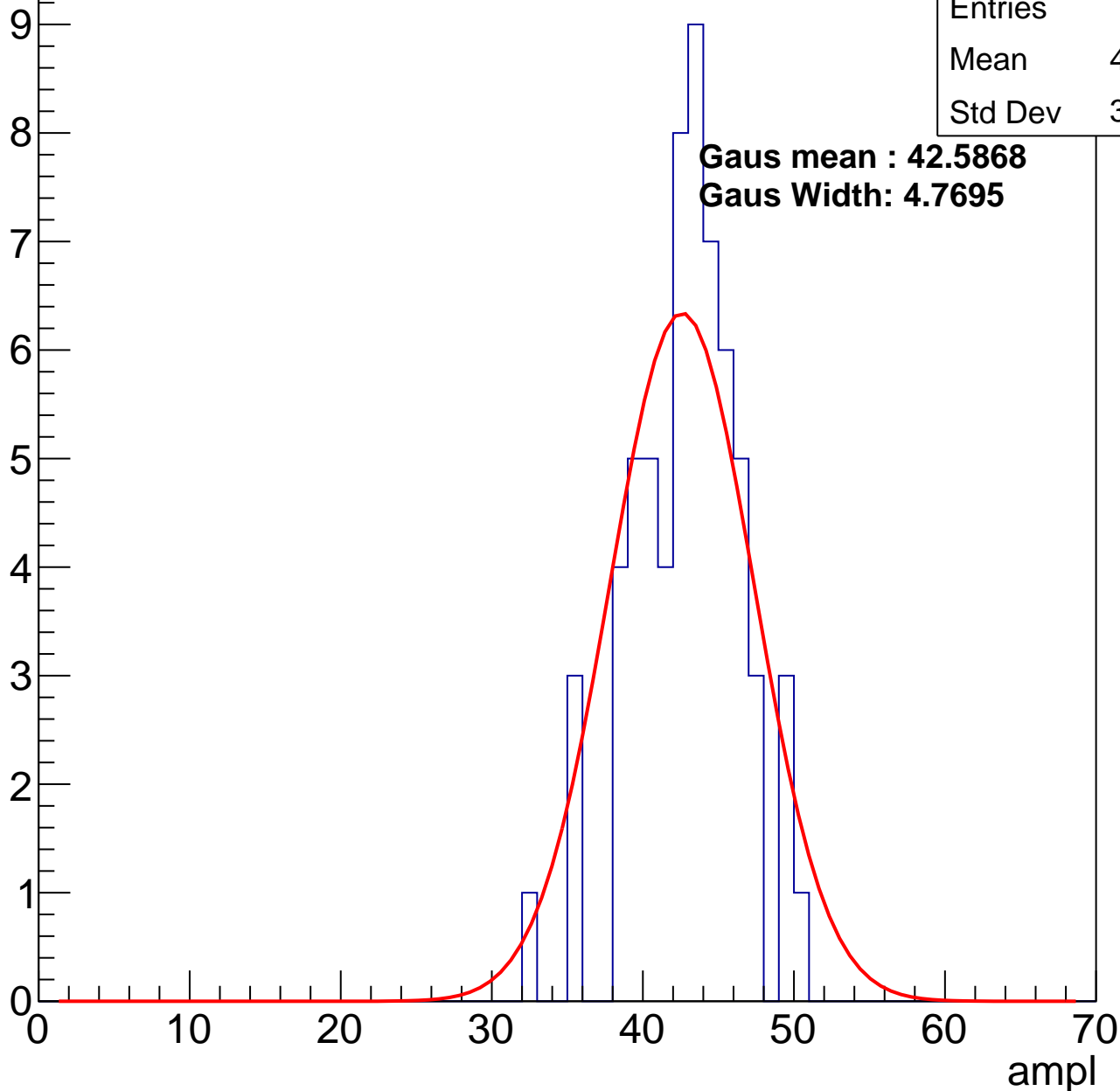
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	42.45
Std Dev	3.588

**Gaus mean : 42.5868**

**Gaus Width: 4.7695**

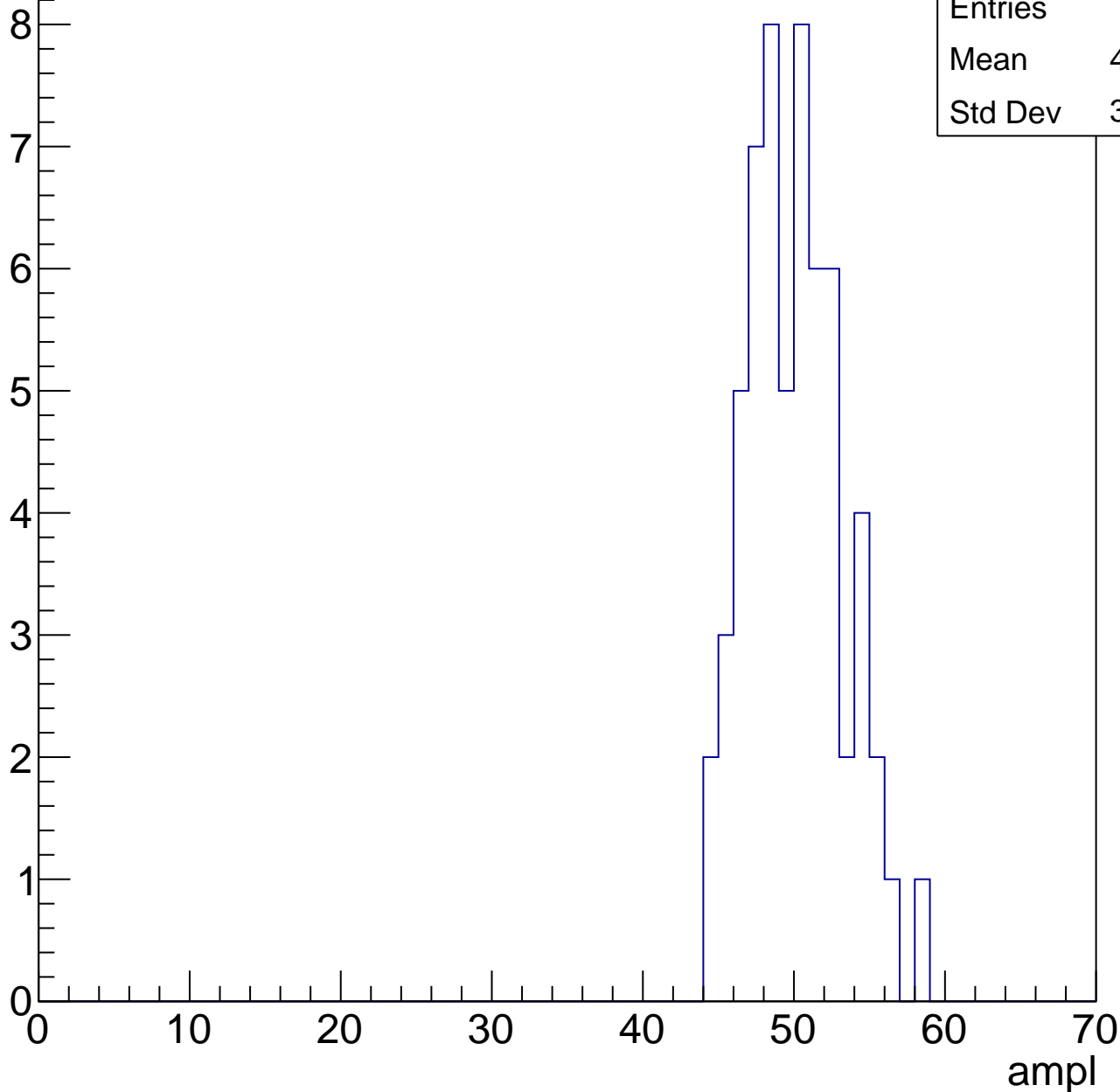


# B1L103S, U2-ch9, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	49.58
Std Dev	3.105

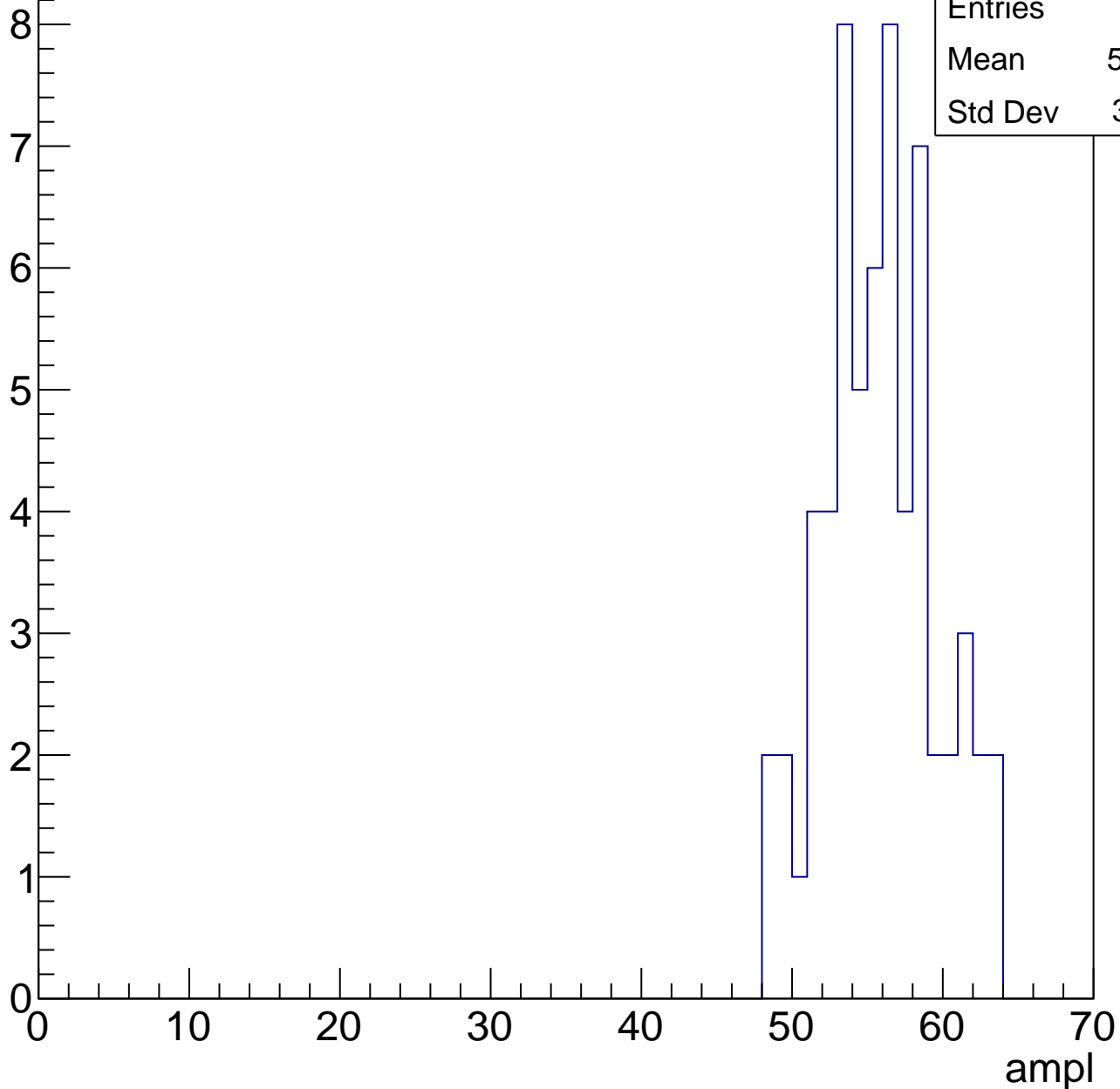


# B1L103S, U2-ch9, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	55.37
Std Dev	3.651

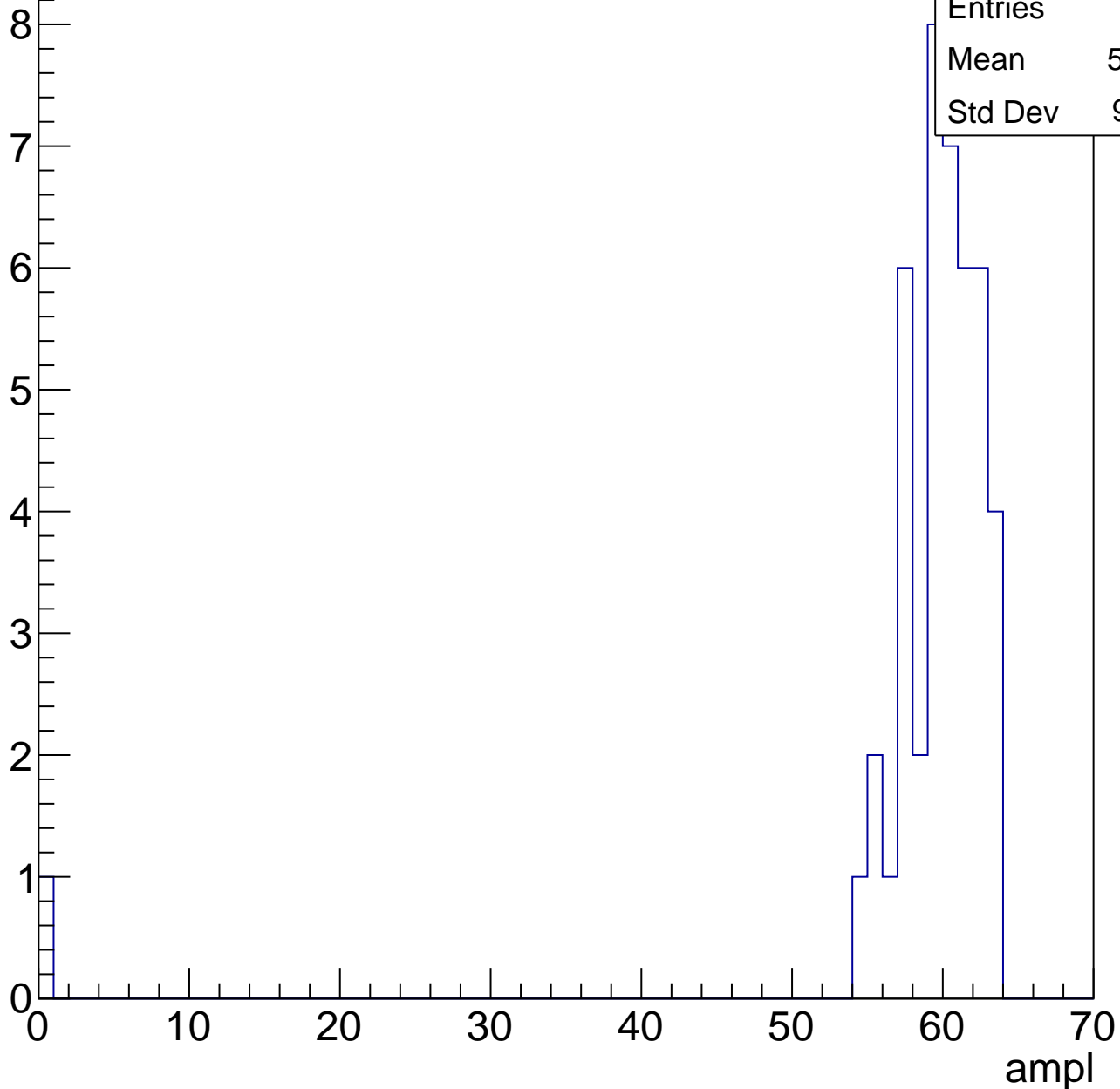


# B1L103S, U2-ch9, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	44
Mean	58.18
Std Dev	9.161



# B1L103S, U2-ch9, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U2-ch9, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U2-ch10, adc0

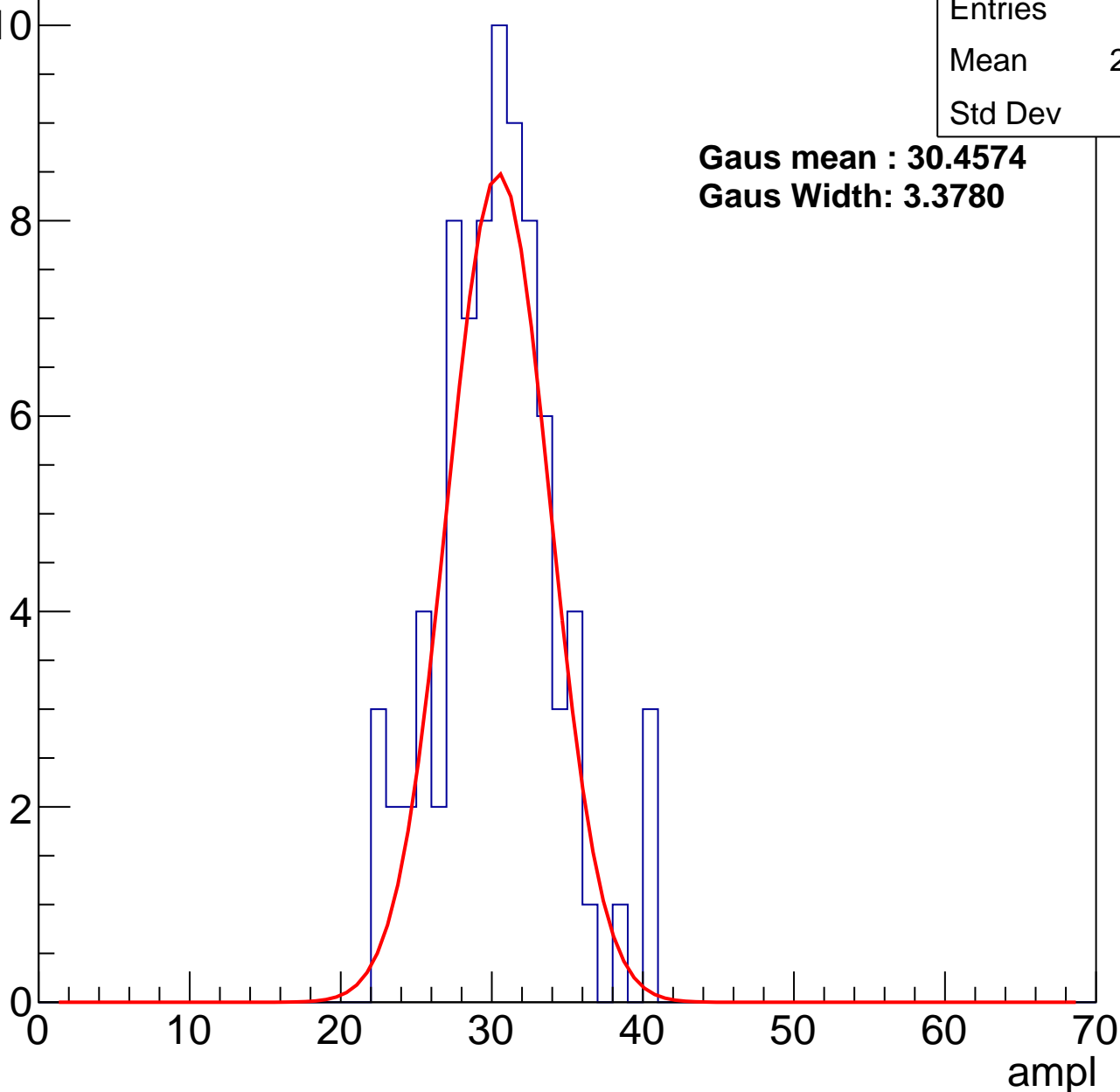
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	81
Mean	29.94
Std Dev	3.92

**Gaus mean : 30.4574**

**Gaus Width: 3.3780**



# B1L103S, U2-ch10, adc1

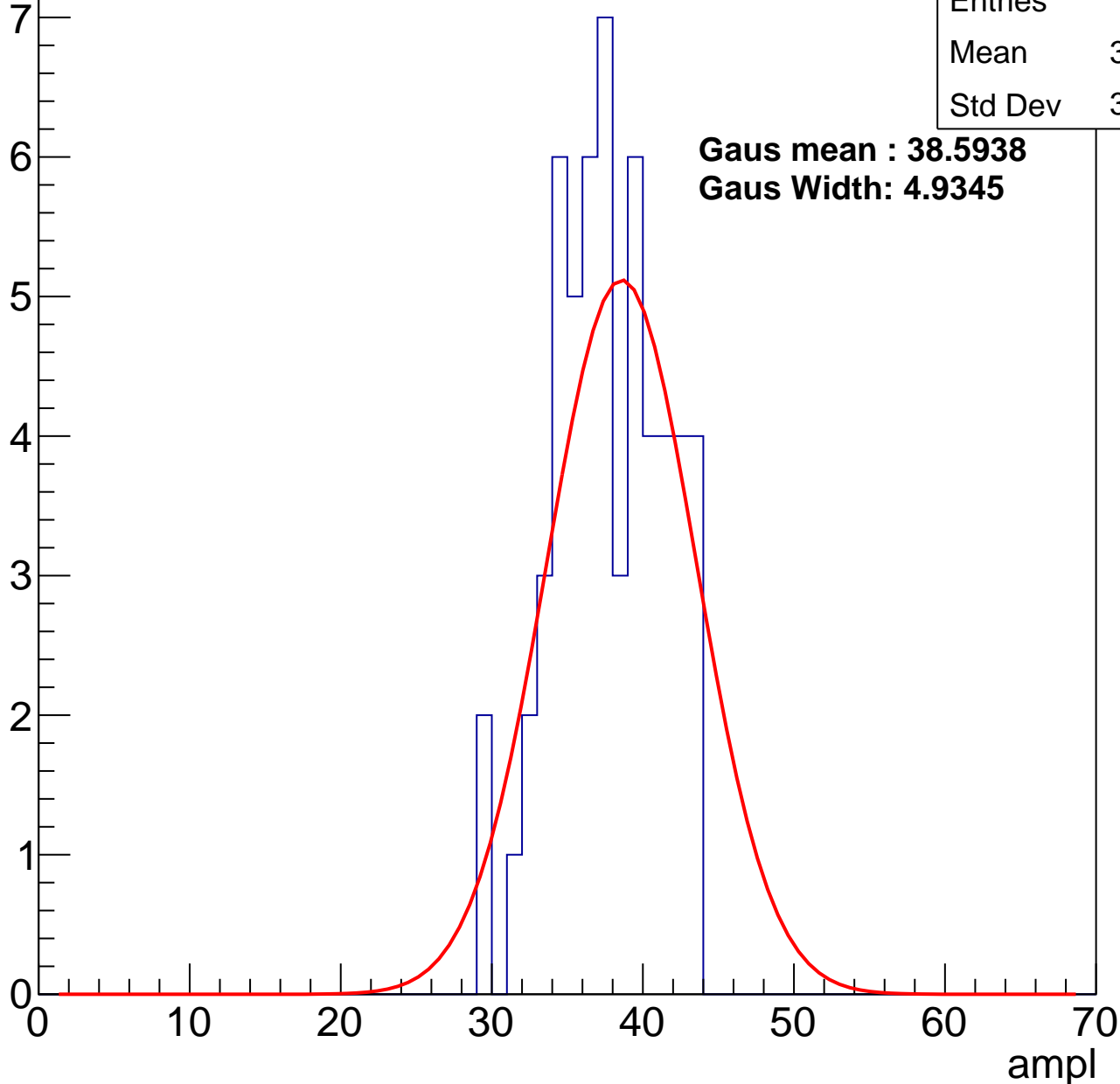
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	37.16
Std Dev	3.533

**Gaus mean : 38.5938**

**Gaus Width: 4.9345**



# B1L103S, U2-ch10, adc2

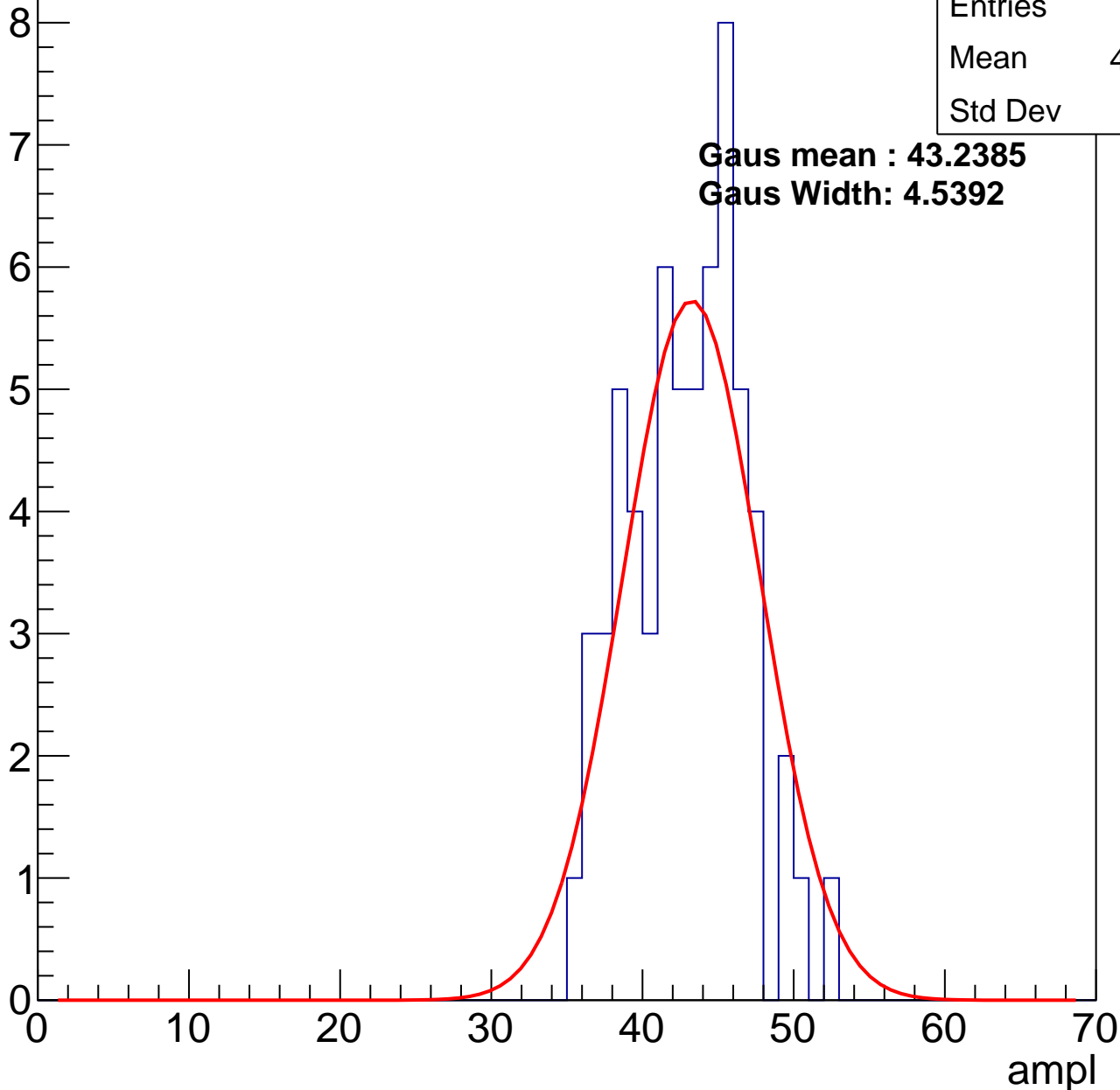
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	42.47
Std Dev	3.8

**Gaus mean : 43.2385**

**Gaus Width: 4.5392**

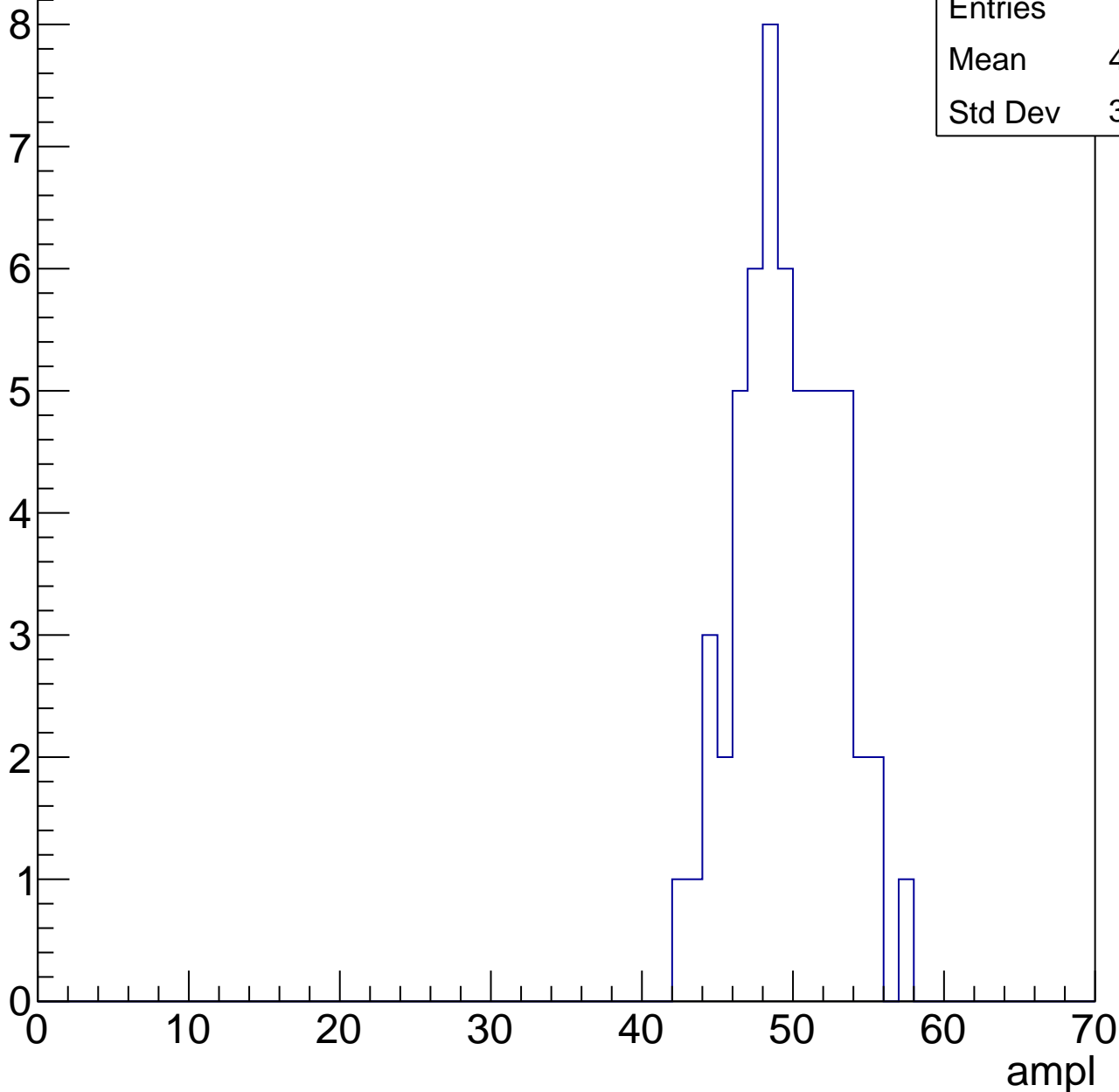


# B1L103S, U2-ch10, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

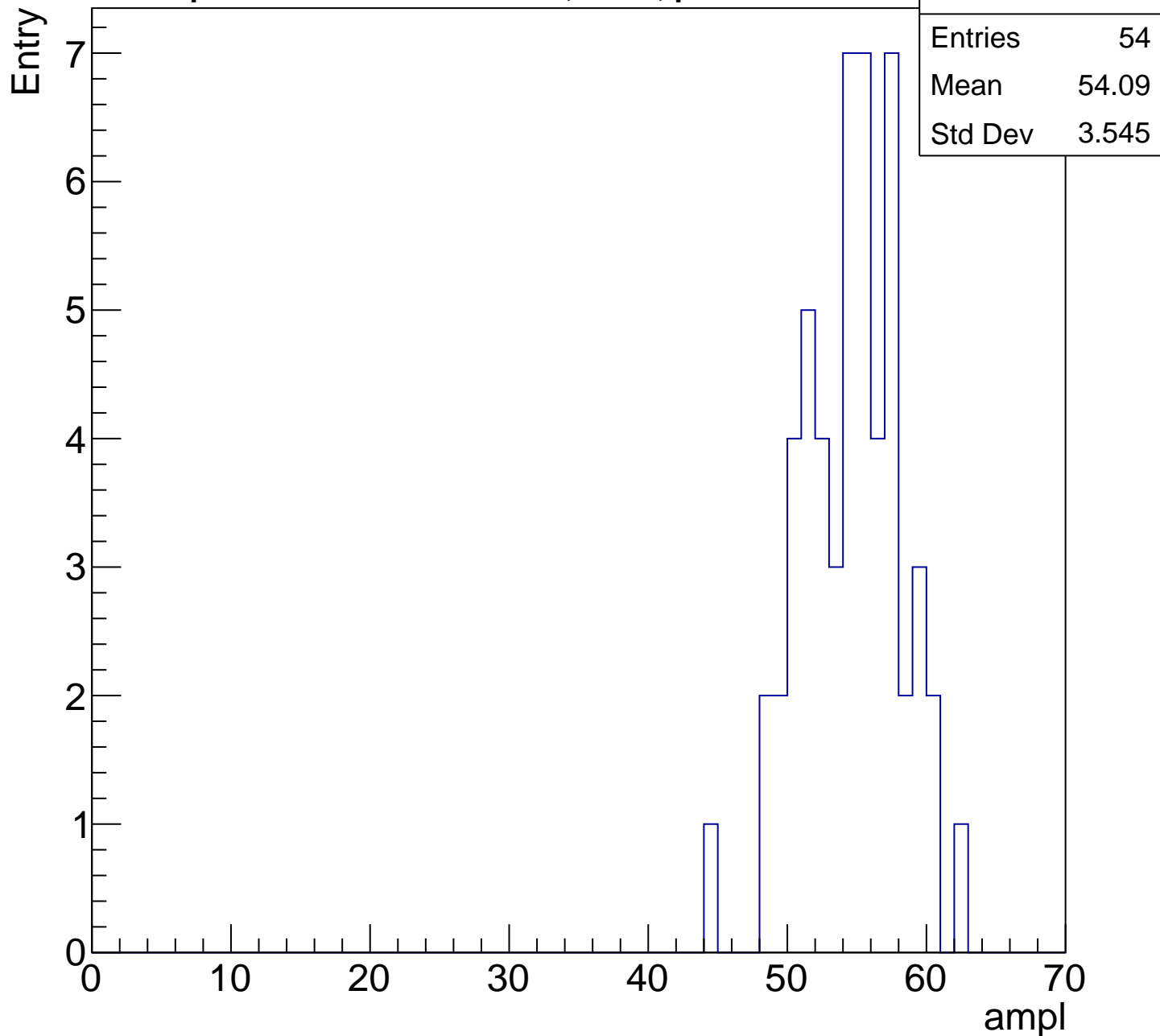
Entry

Entries	57
Mean	49.16
Std Dev	3.254



# B1L103S, U2-ch10, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

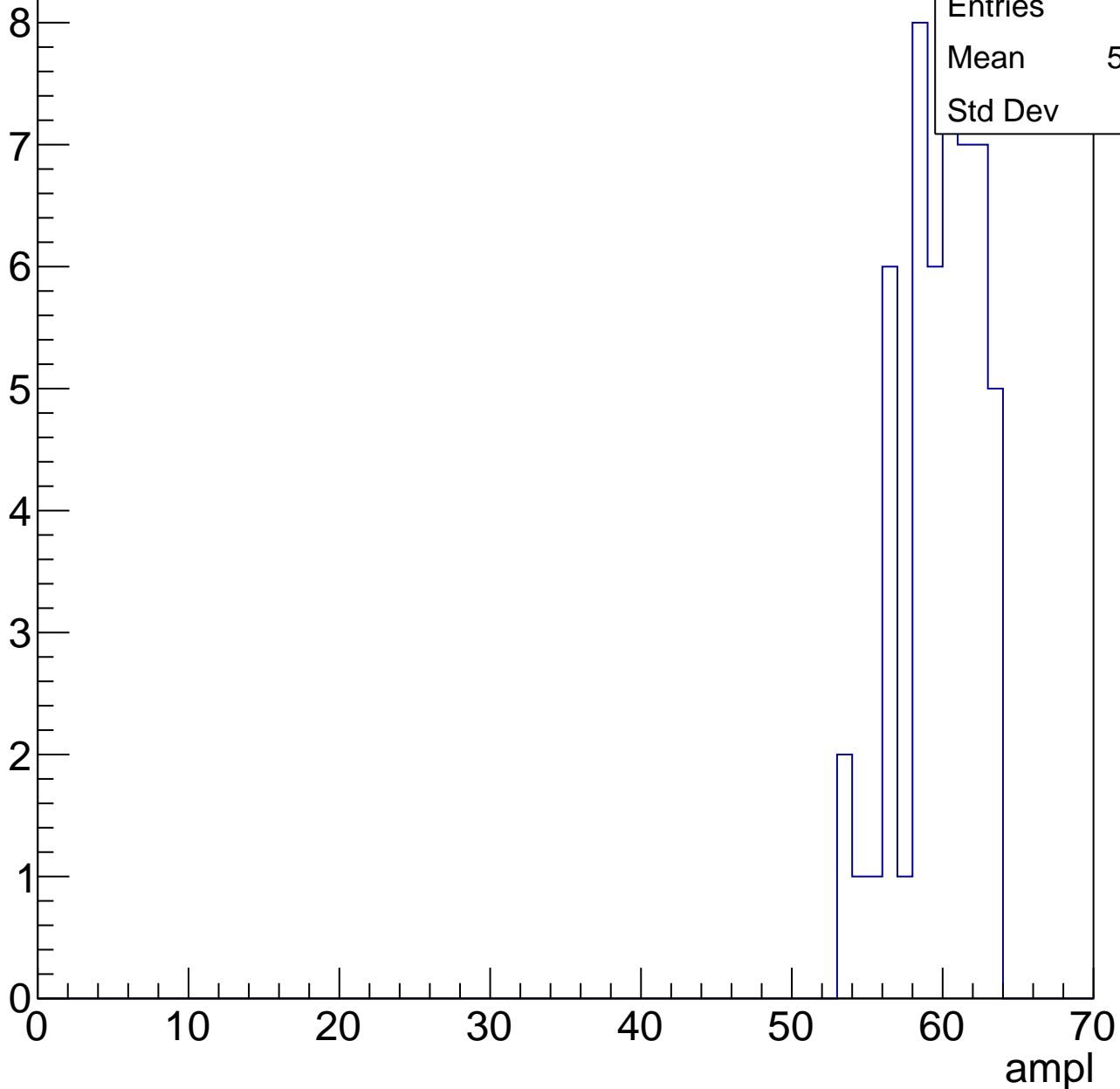


# B1L103S, U2-ch10, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

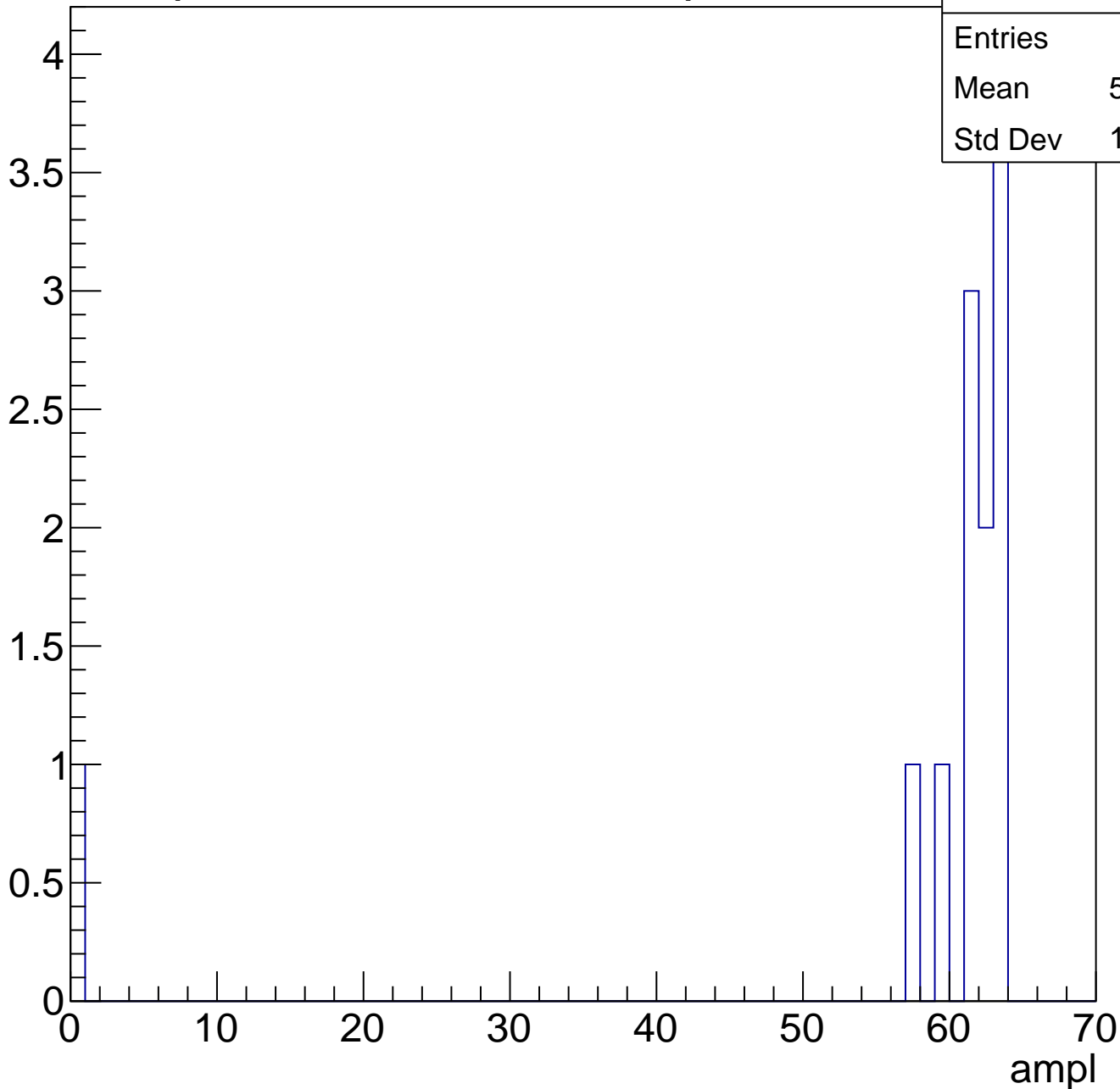
Entries	52
Mean	59.27
Std Dev	2.61



# B1L103S, U2-ch10, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U2-ch10, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch11, adc0

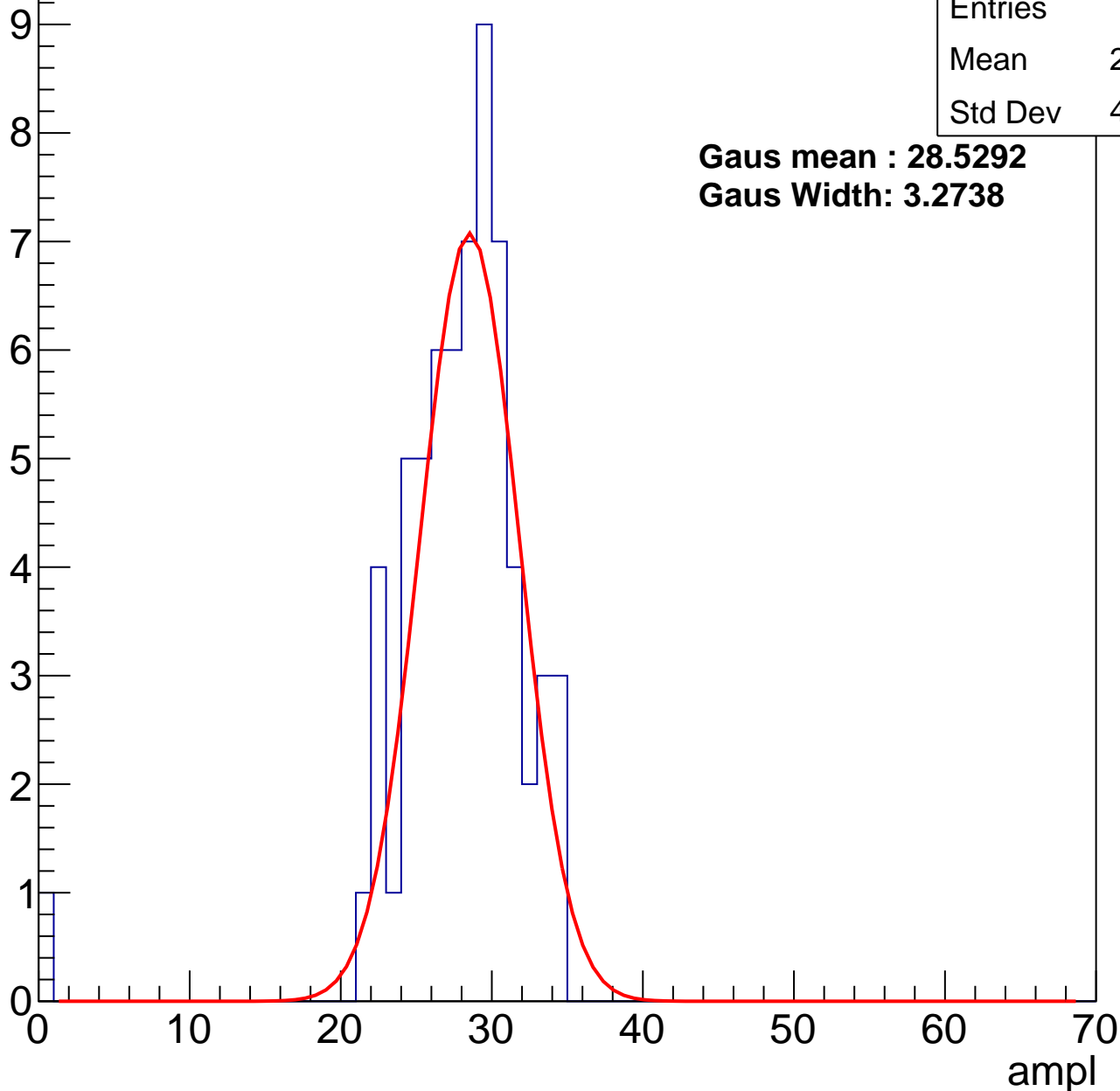
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	27.36
Std Dev	4.708

**Gaus mean : 28.5292**

**Gaus Width: 3.2738**



# B1L103S, U2-ch11, adc1

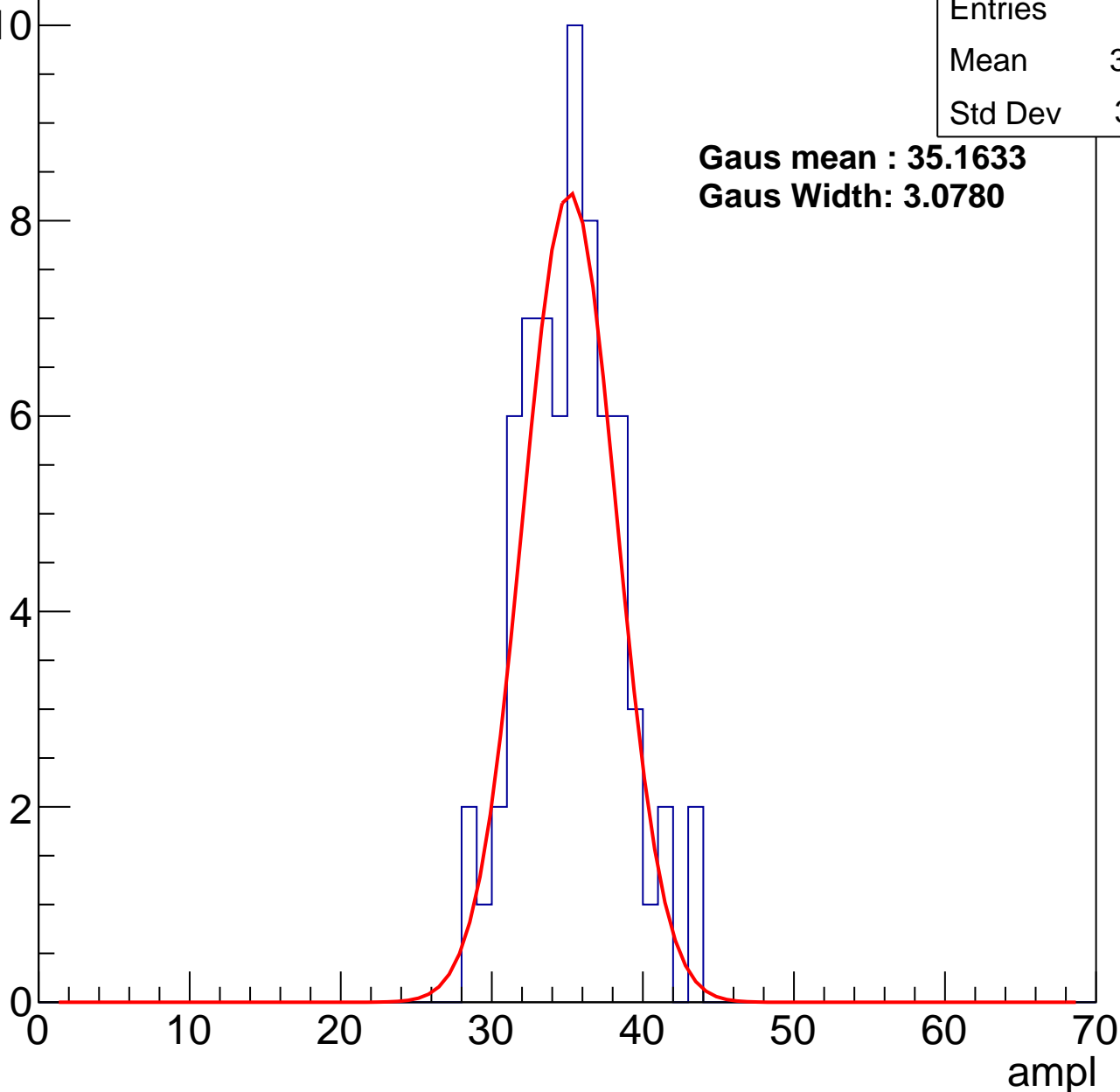
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	34.83
Std Dev	3.261

**Gaus mean : 35.1633**

**Gaus Width: 3.0780**



# B1L103S, U2-ch11, adc2

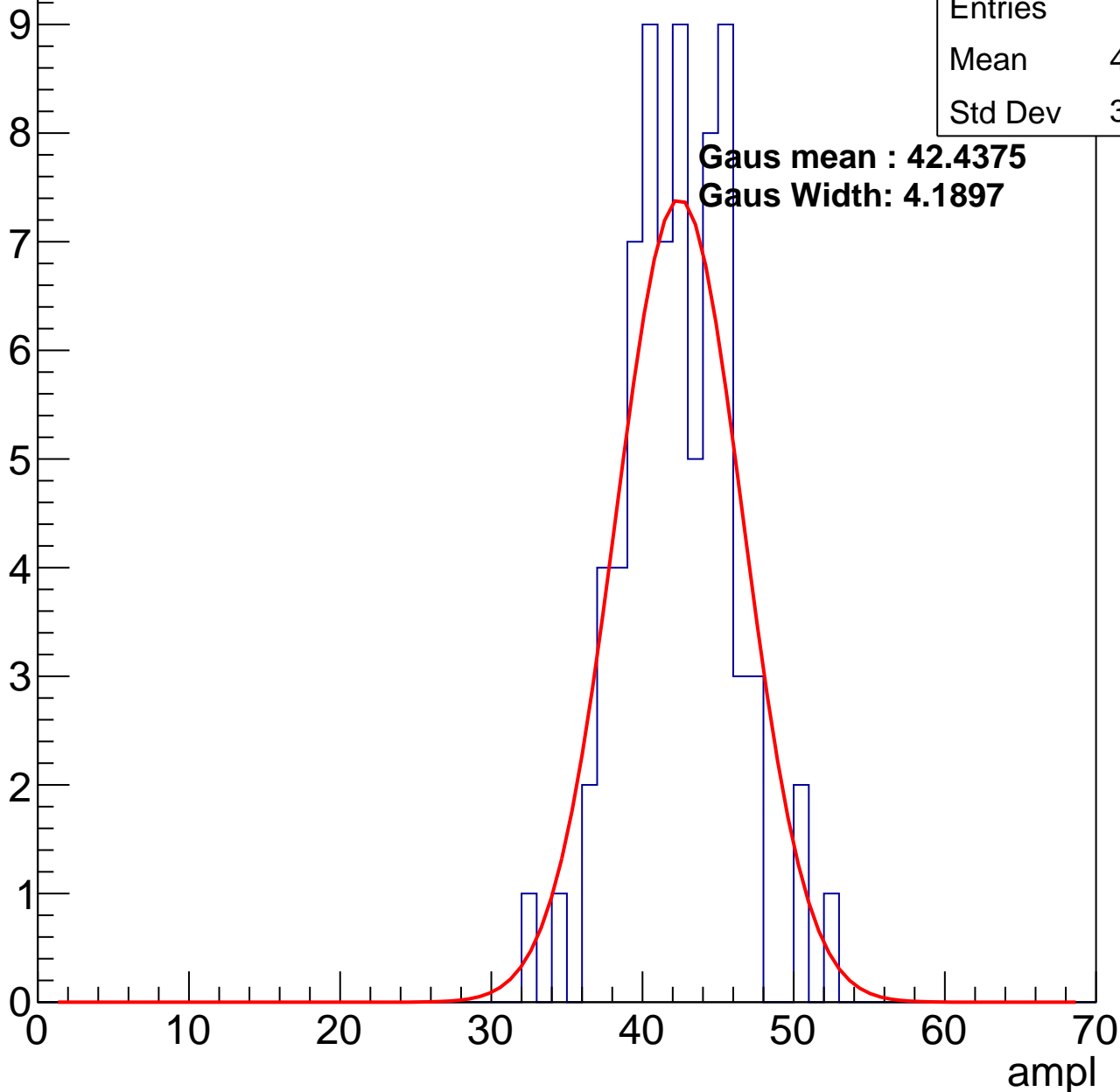
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	41.85
Std Dev	3.603

**Gaus mean : 42.4375**

**Gaus Width: 4.1897**

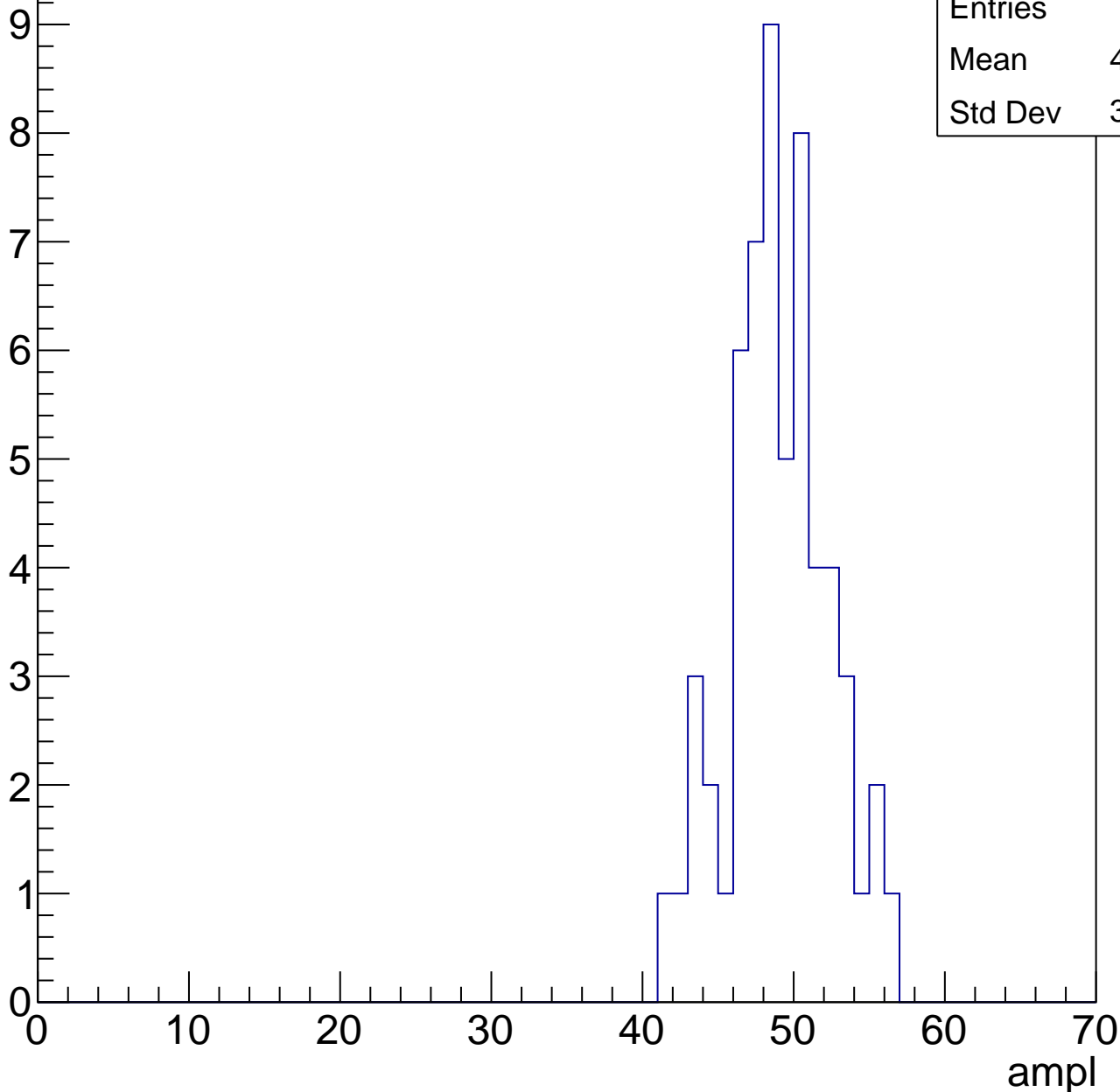


# B1L103S, U2-ch11, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

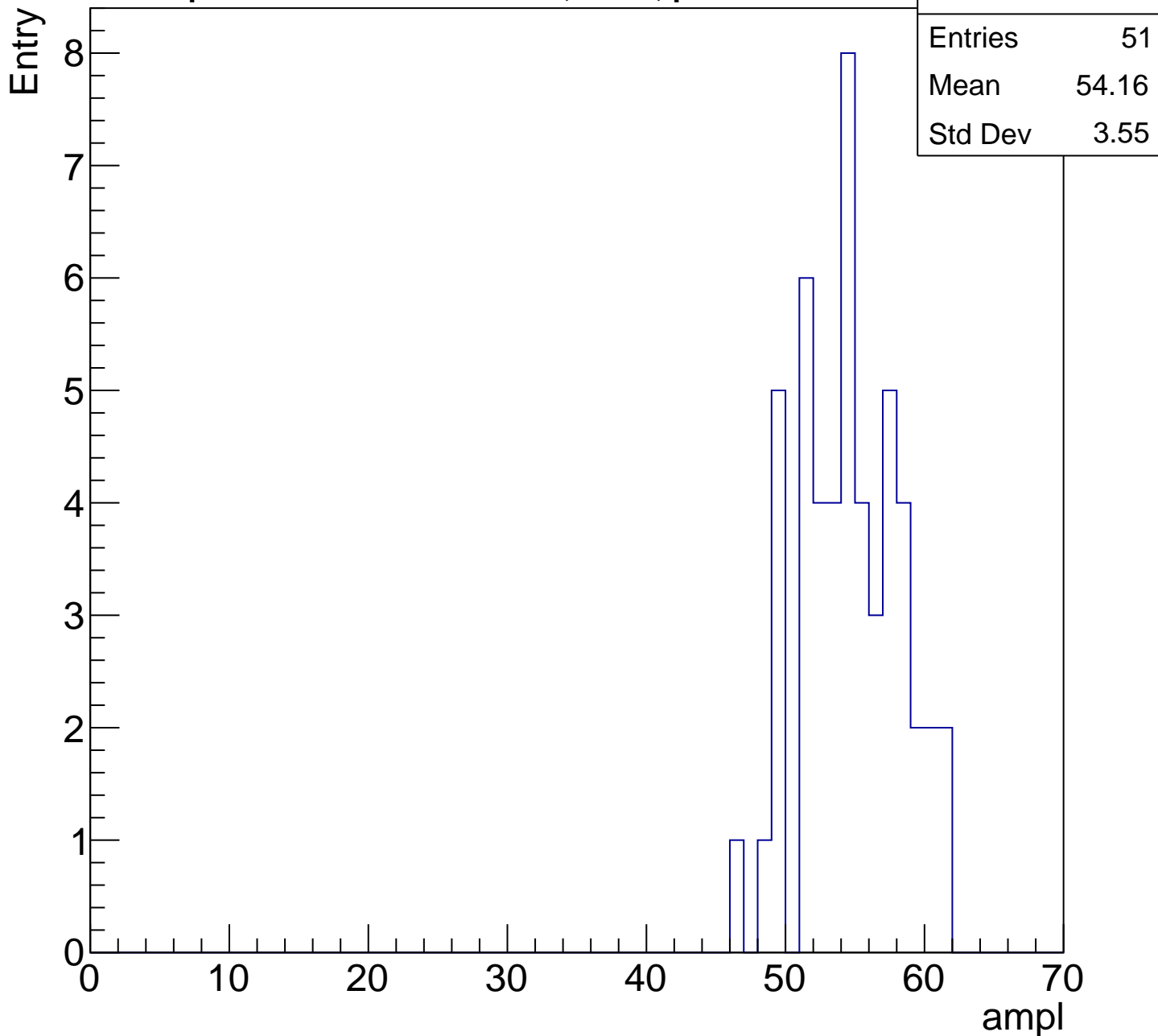
Entry

Entries	58
Mean	48.59
Std Dev	3.275



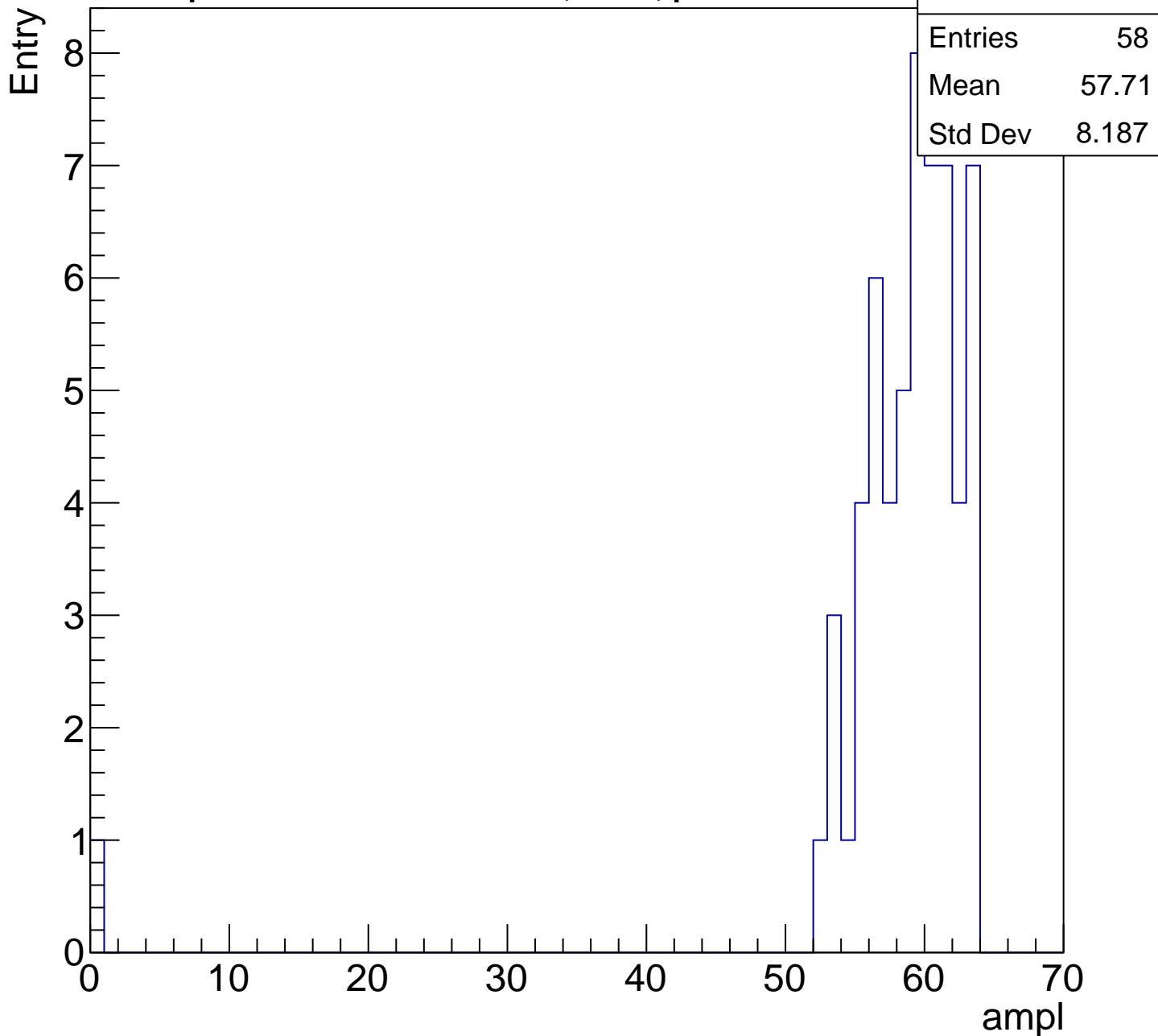
# B1L103S, U2-ch11, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U2-ch11, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

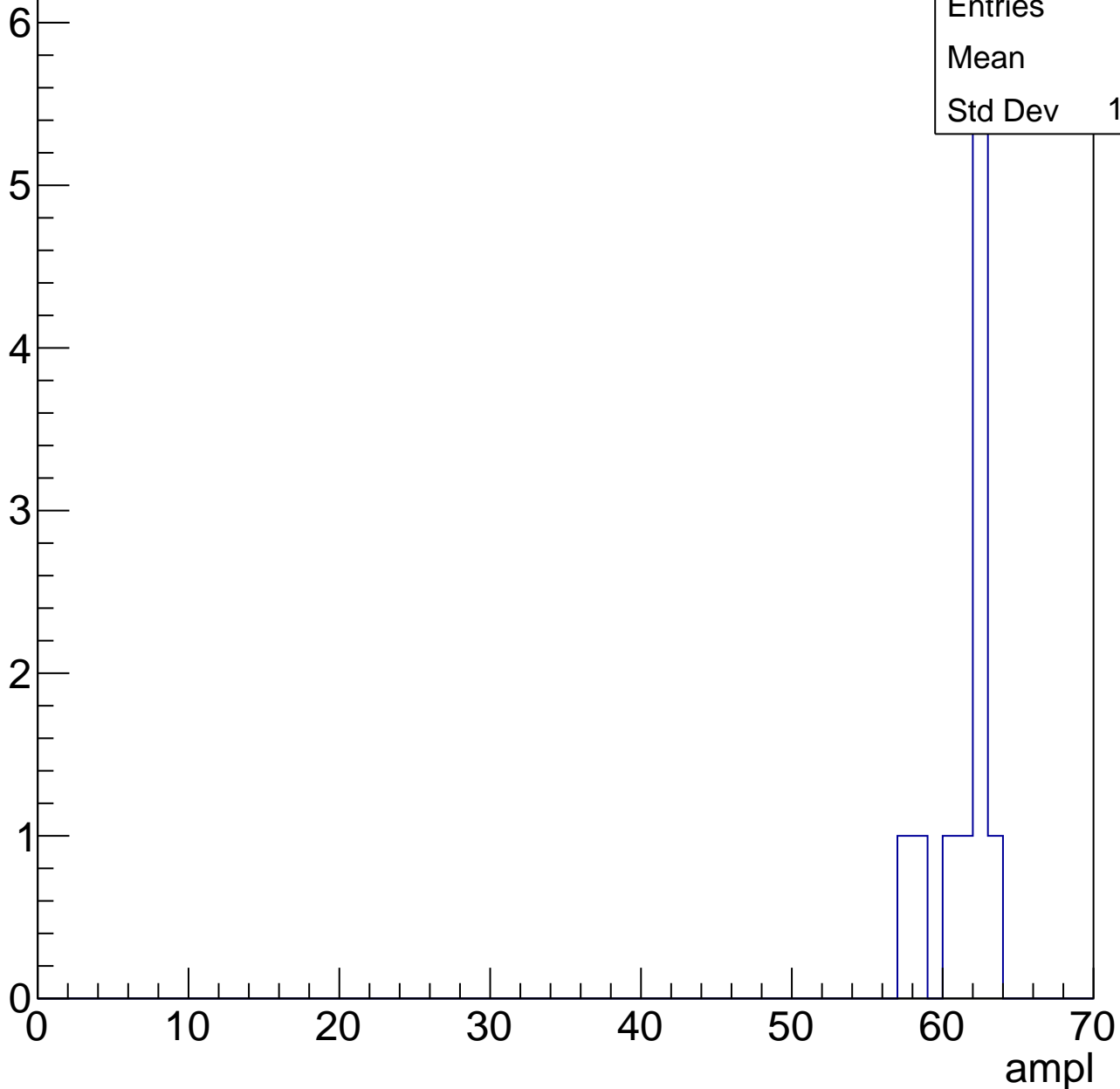


# B1L103S, U2-ch11, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	11
Mean	61
Std Dev	1.809





# B1L103S, U2-ch11, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch12, adc0

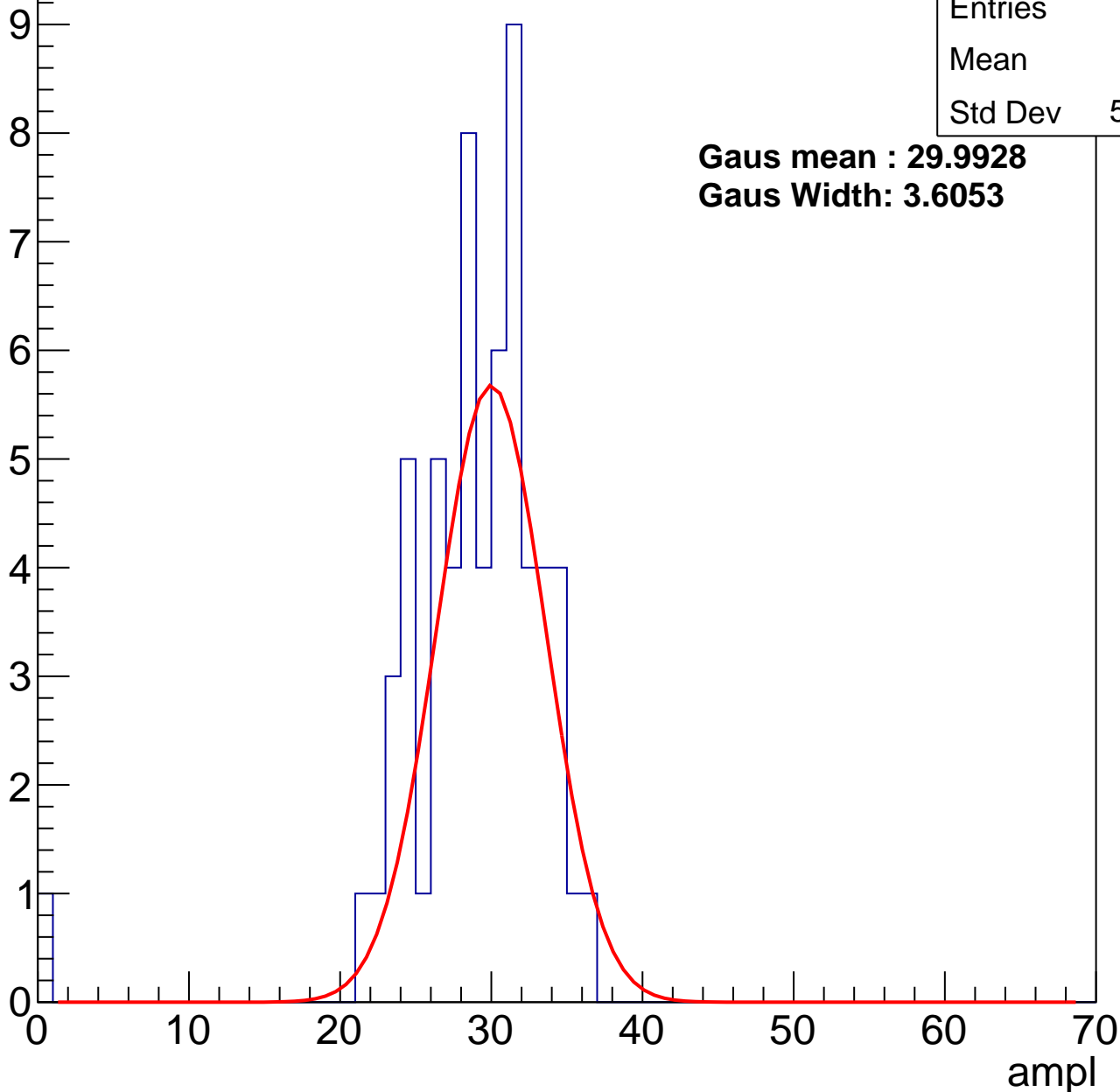
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	28.4
Std Dev	5.043

**Gaus mean : 29.9928**

**Gaus Width: 3.6053**



# B1L103S, U2-ch12, adc1

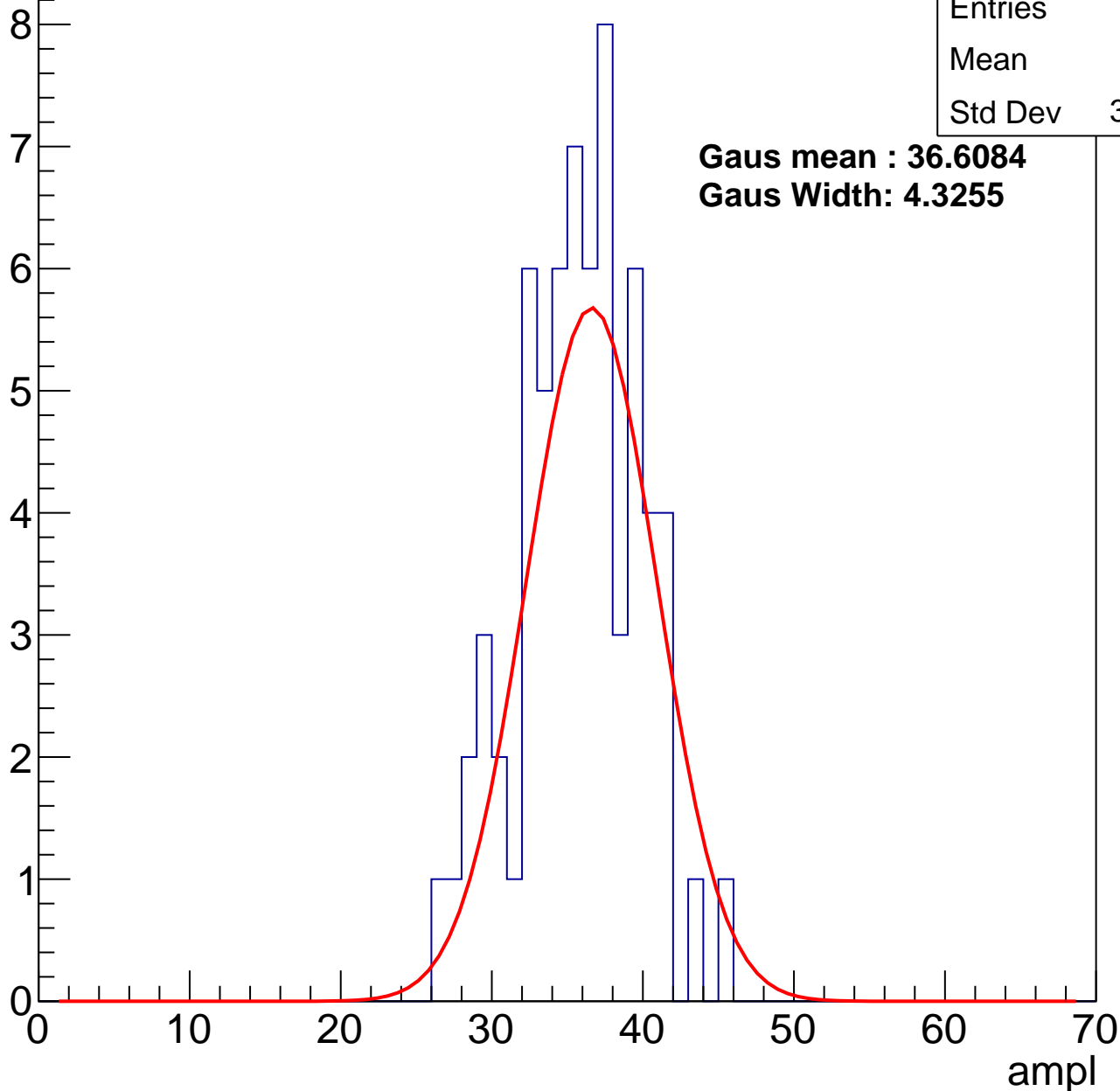
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	35.3
Std Dev	3.978

**Gaus mean : 36.6084**

**Gaus Width: 4.3255**



# B1L103S, U2-ch12, adc2

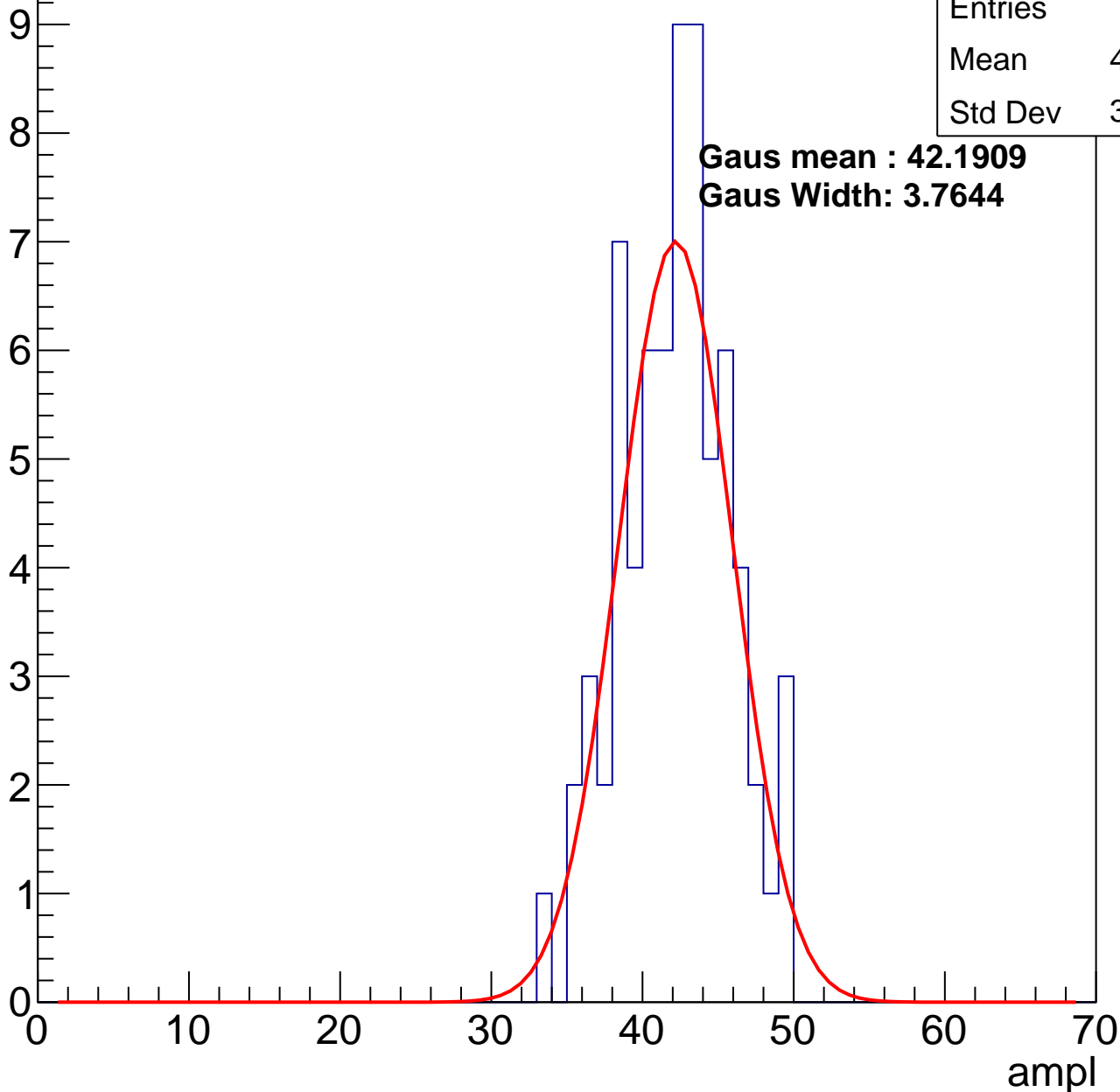
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	41.73
Std Dev	3.565

**Gaus mean : 42.1909**

**Gaus Width: 3.7644**

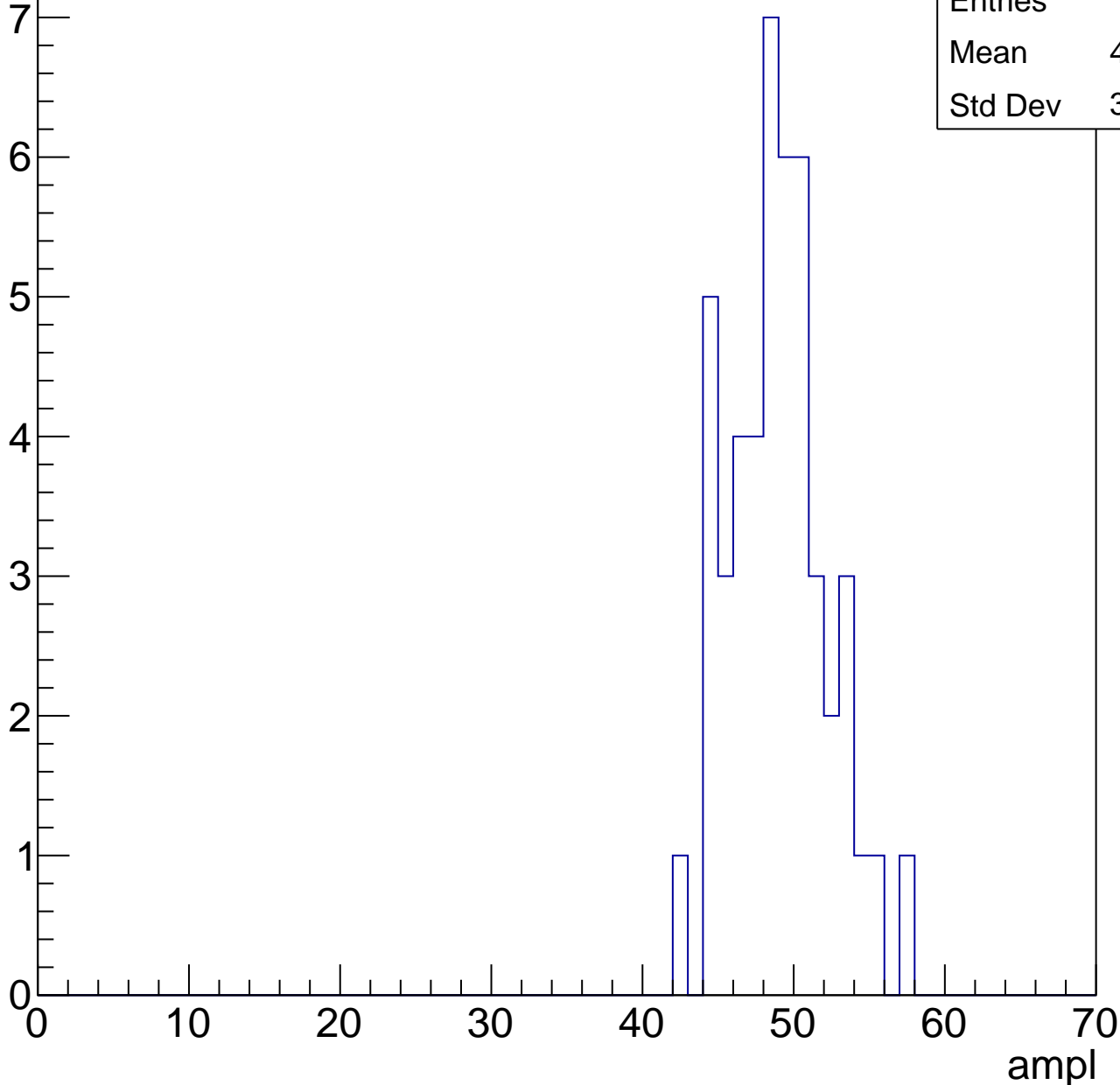


# B1L103S, U2-ch12, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

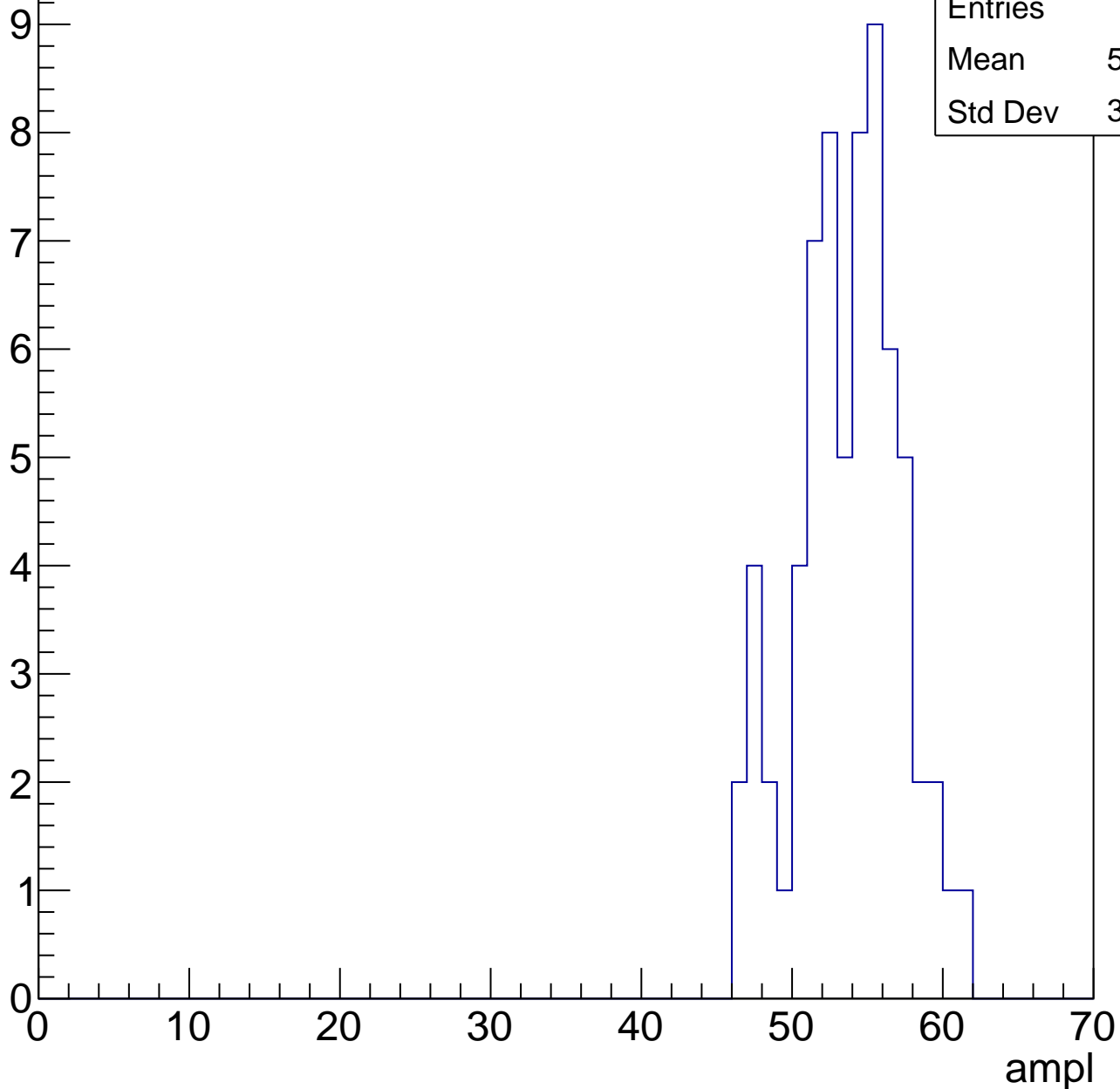
Entries	47
Mean	48.53
Std Dev	3.195



# B1L103S, U2-ch12, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

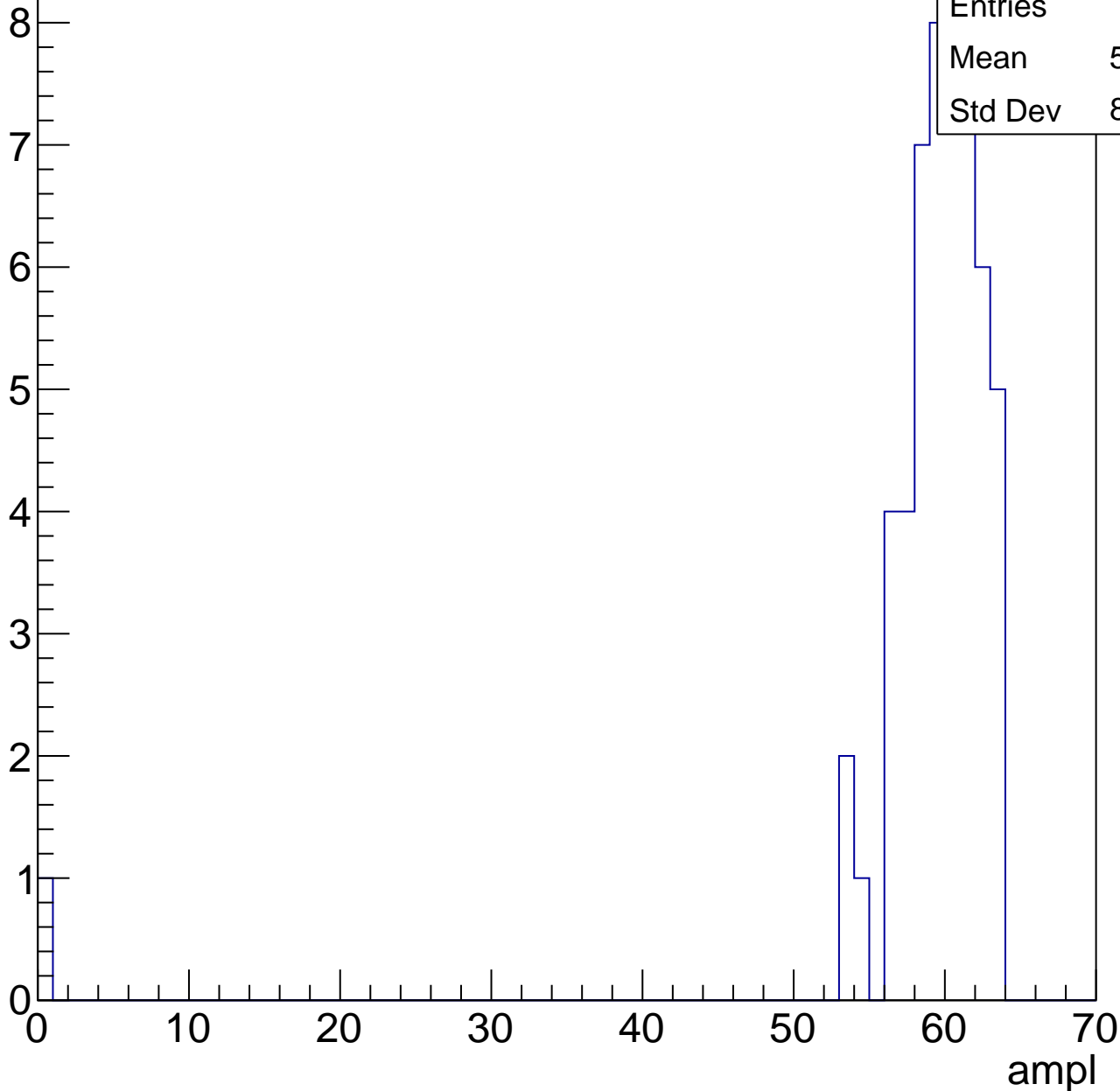


# B1L103S, U2-ch12, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	58.24
Std Dev	8.366

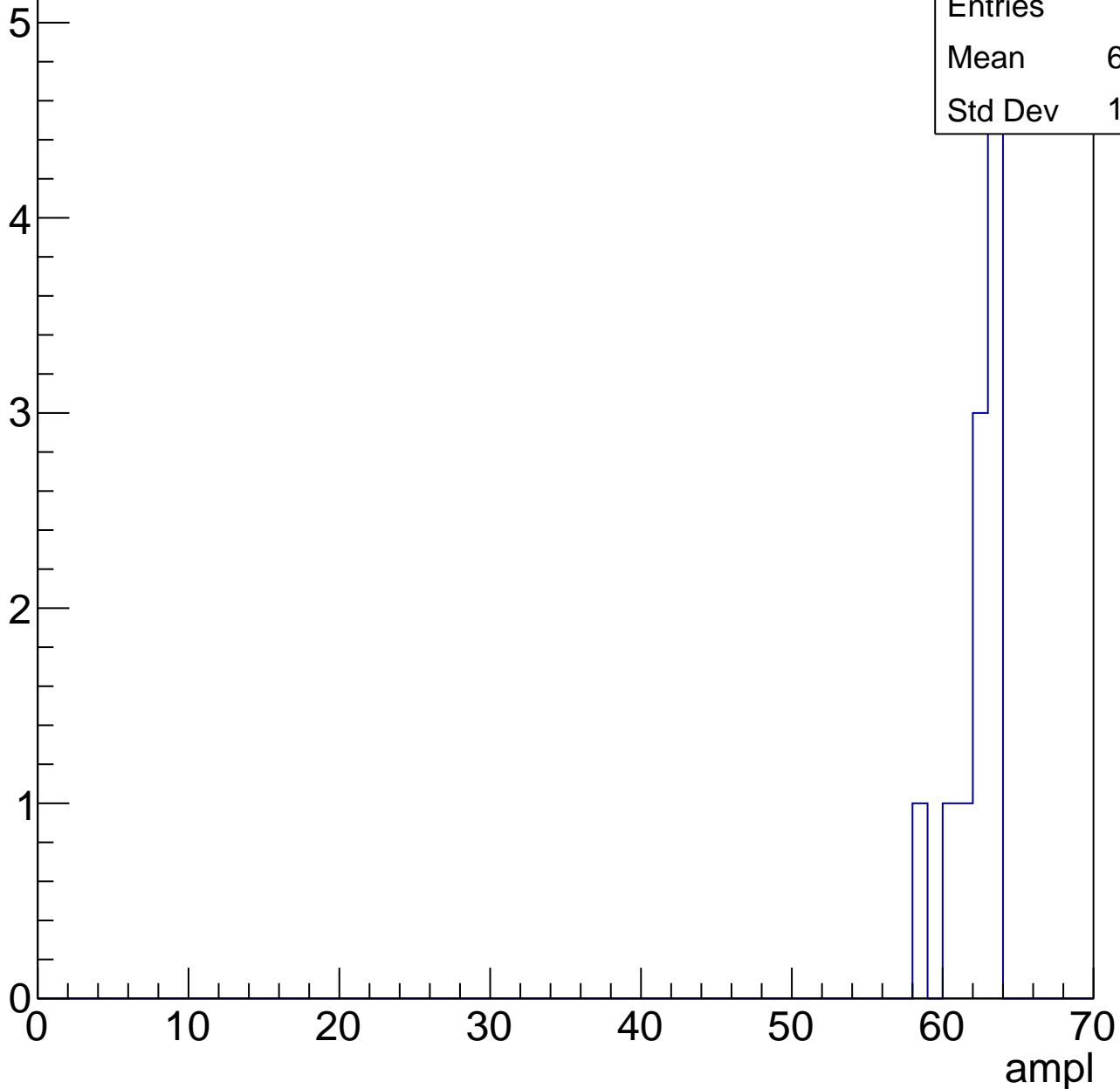


# B1L103S, U2-ch12, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	11
Mean	61.82
Std Dev	1.527





# B1L103S, U2-ch12, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch13, adc0

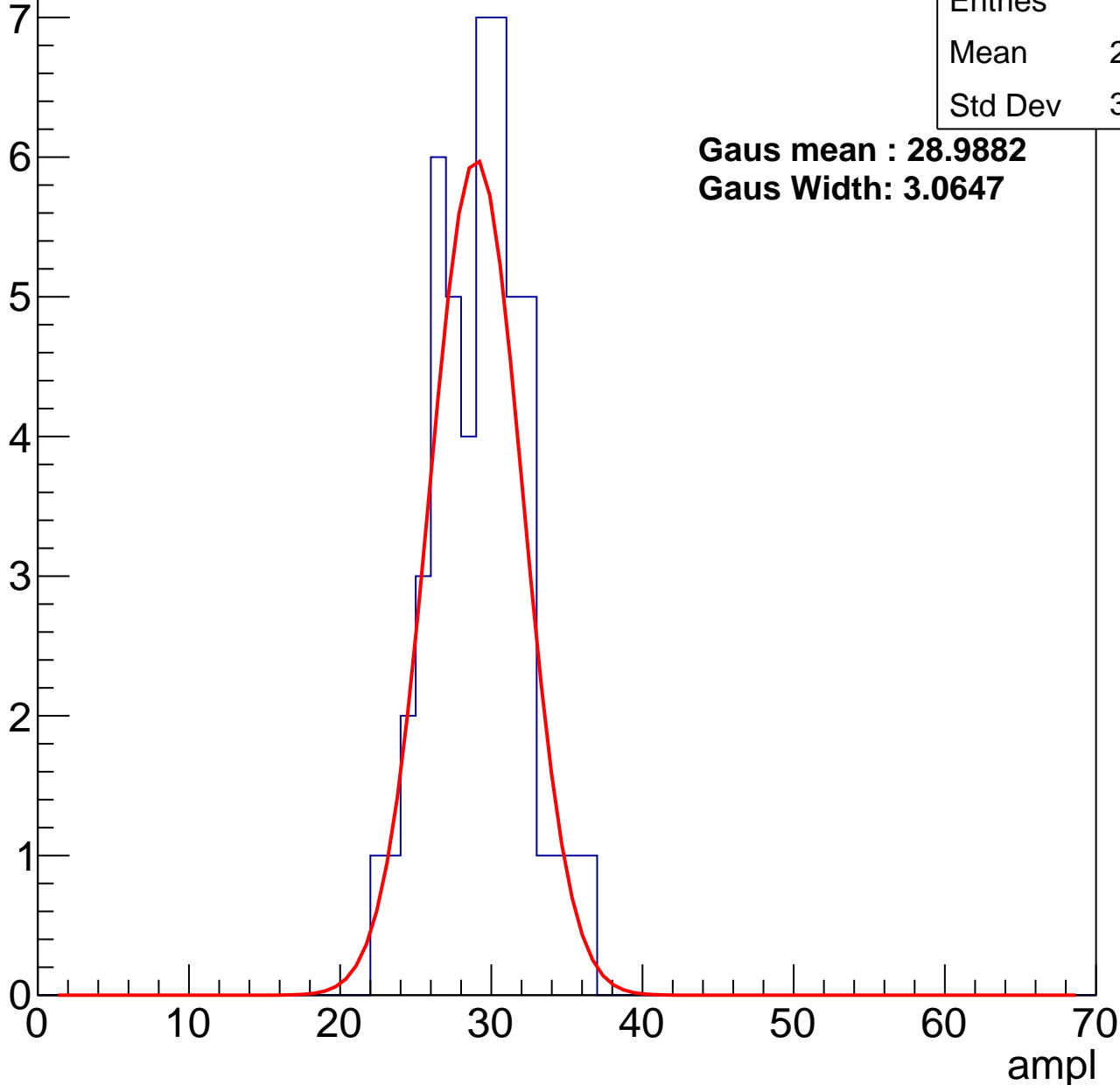
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	28.74
Std Dev	3.019

**Gaus mean : 28.9882**

**Gaus Width: 3.0647**



# B1L103S, U2-ch13, adc1

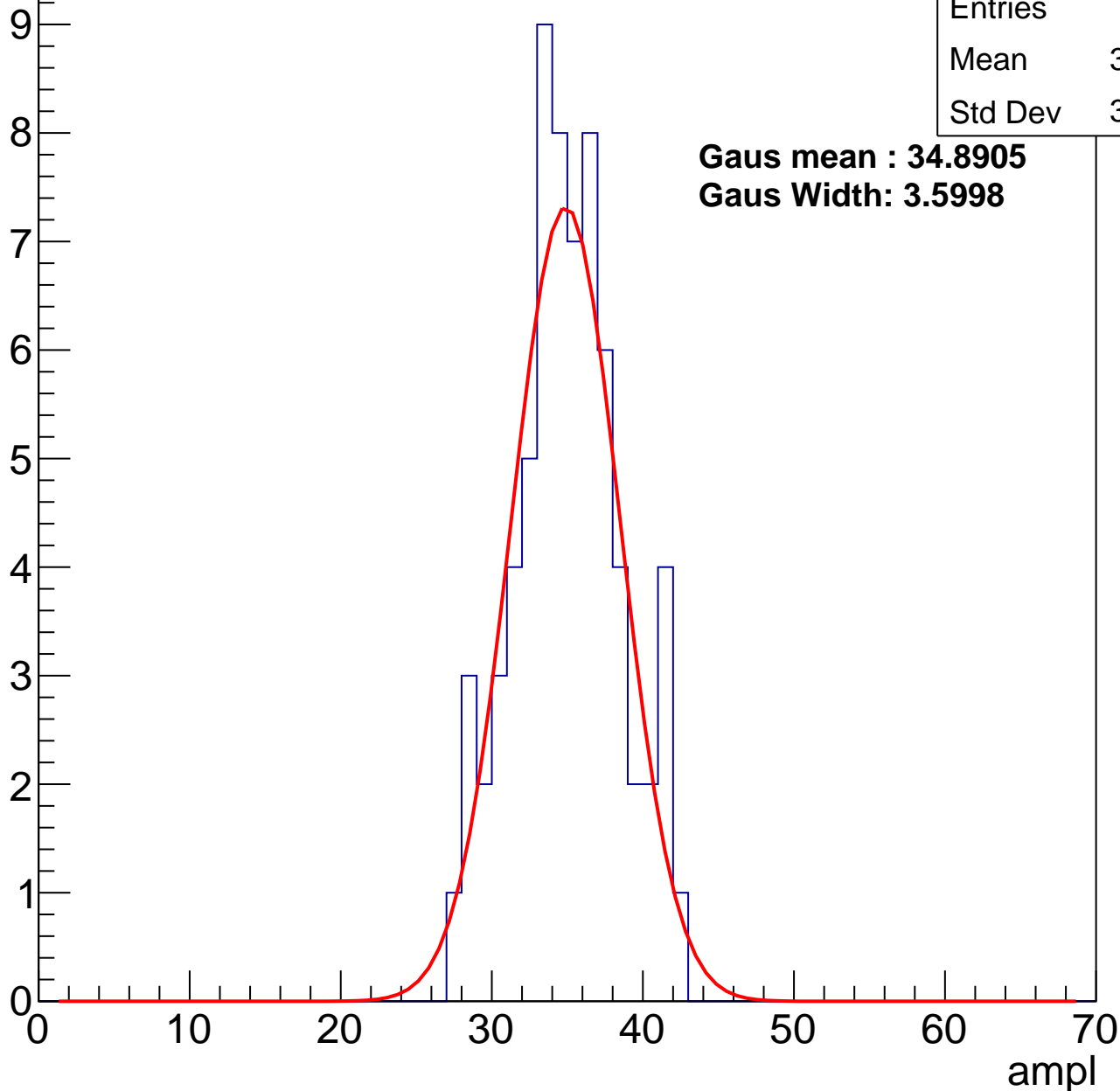
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	34.54
Std Dev	3.487

**Gaus mean : 34.8905**

**Gaus Width: 3.5998**



# B1L103S, U2-ch13, adc2

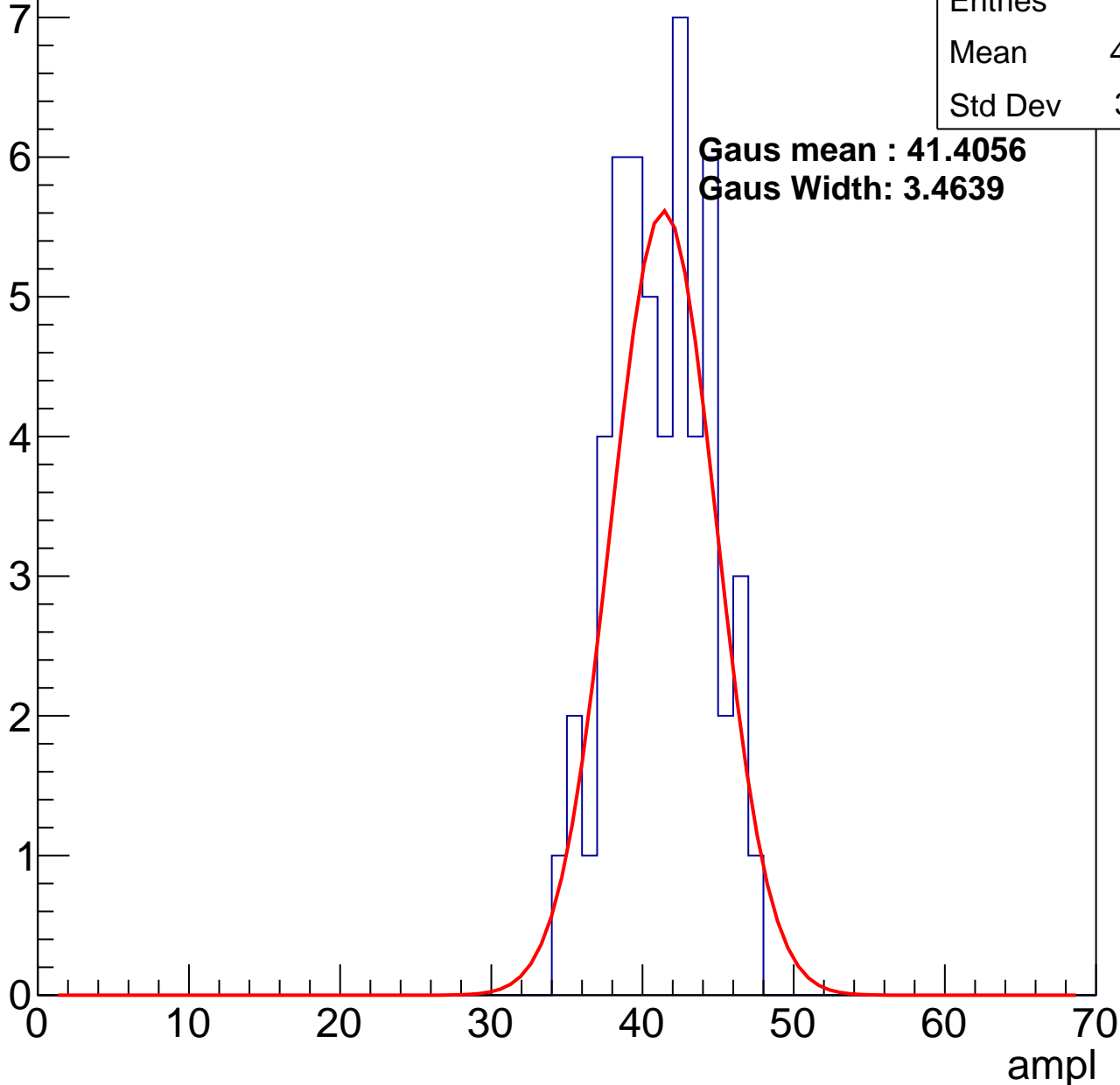
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	40.75
Std Dev	3.131

**Gaus mean : 41.4056**

**Gaus Width: 3.4639**

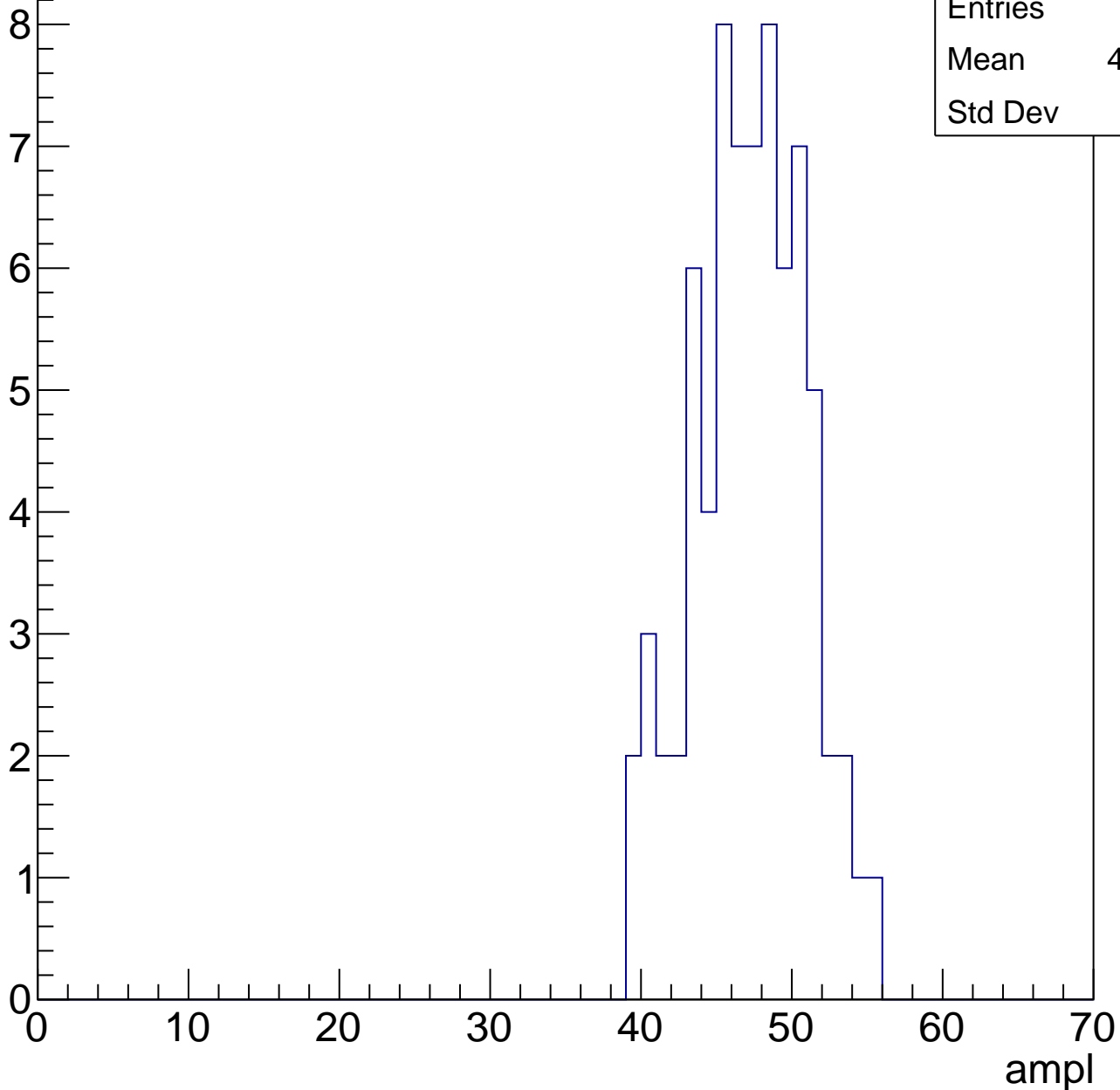


# B1L103S, U2-ch13, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

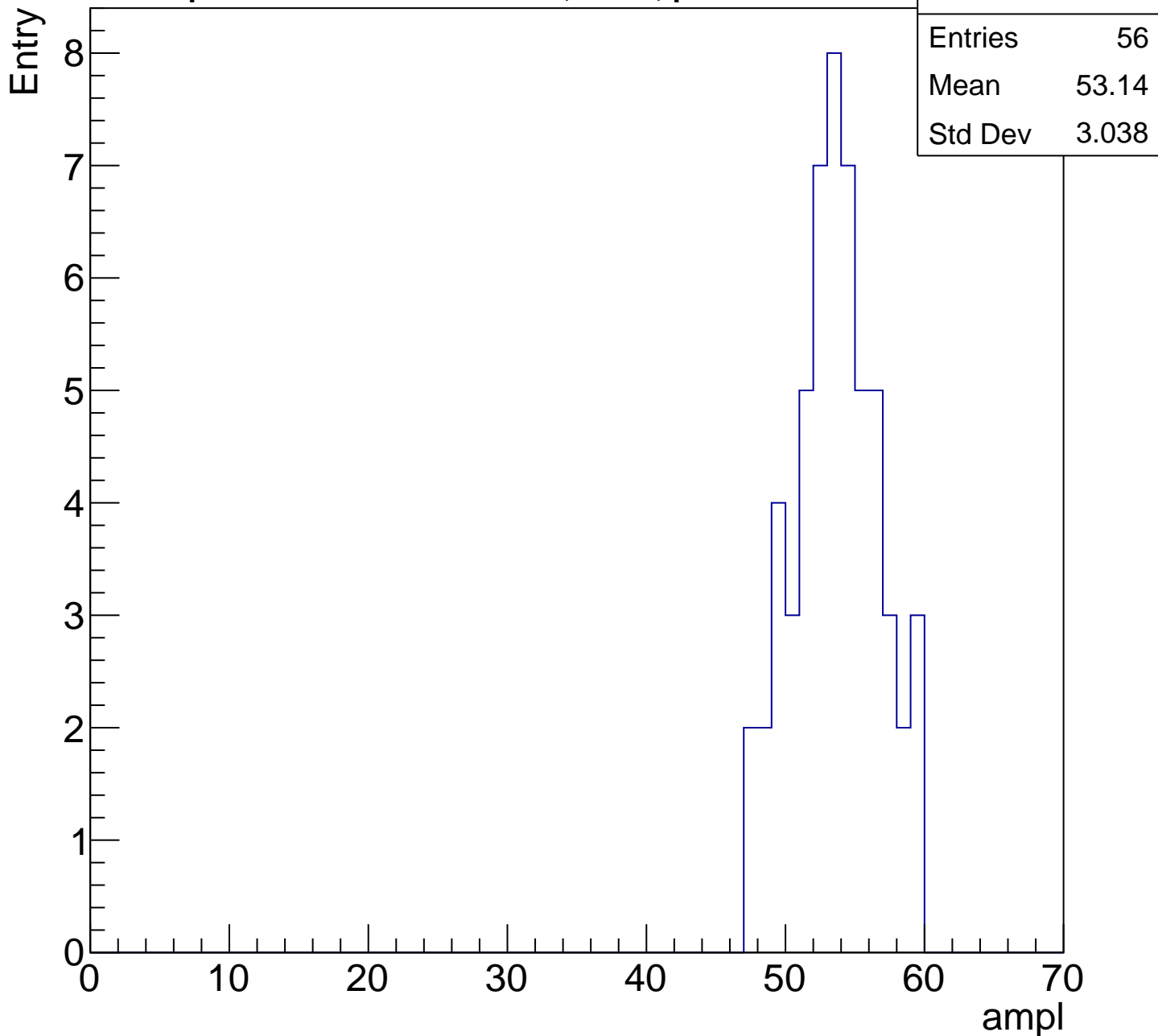
Entry

Entries	73
Mean	46.73
Std Dev	3.65



# B1L103S, U2-ch13, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

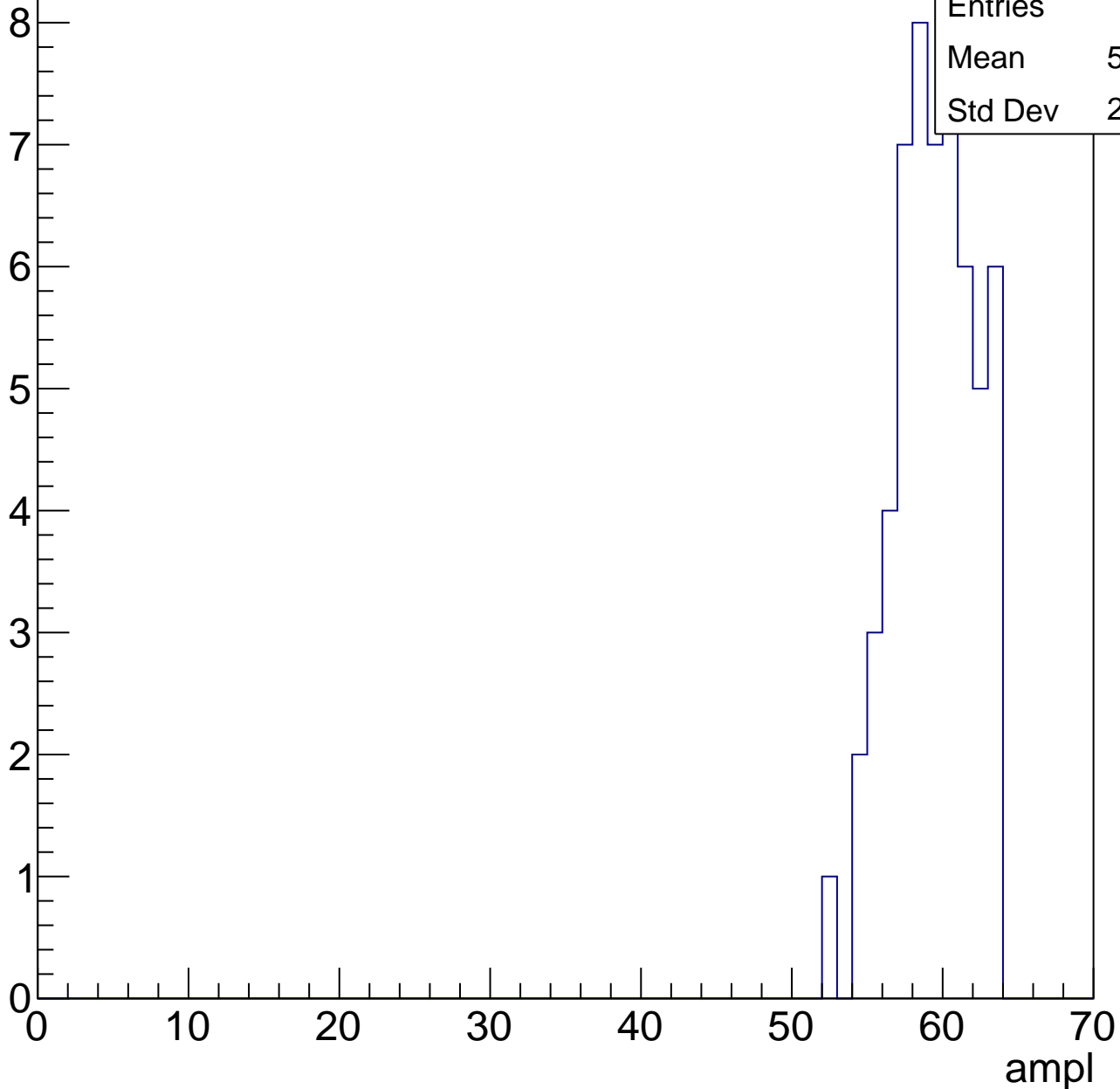


# B1L103S, U2-ch13, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	58.93
Std Dev	2.622

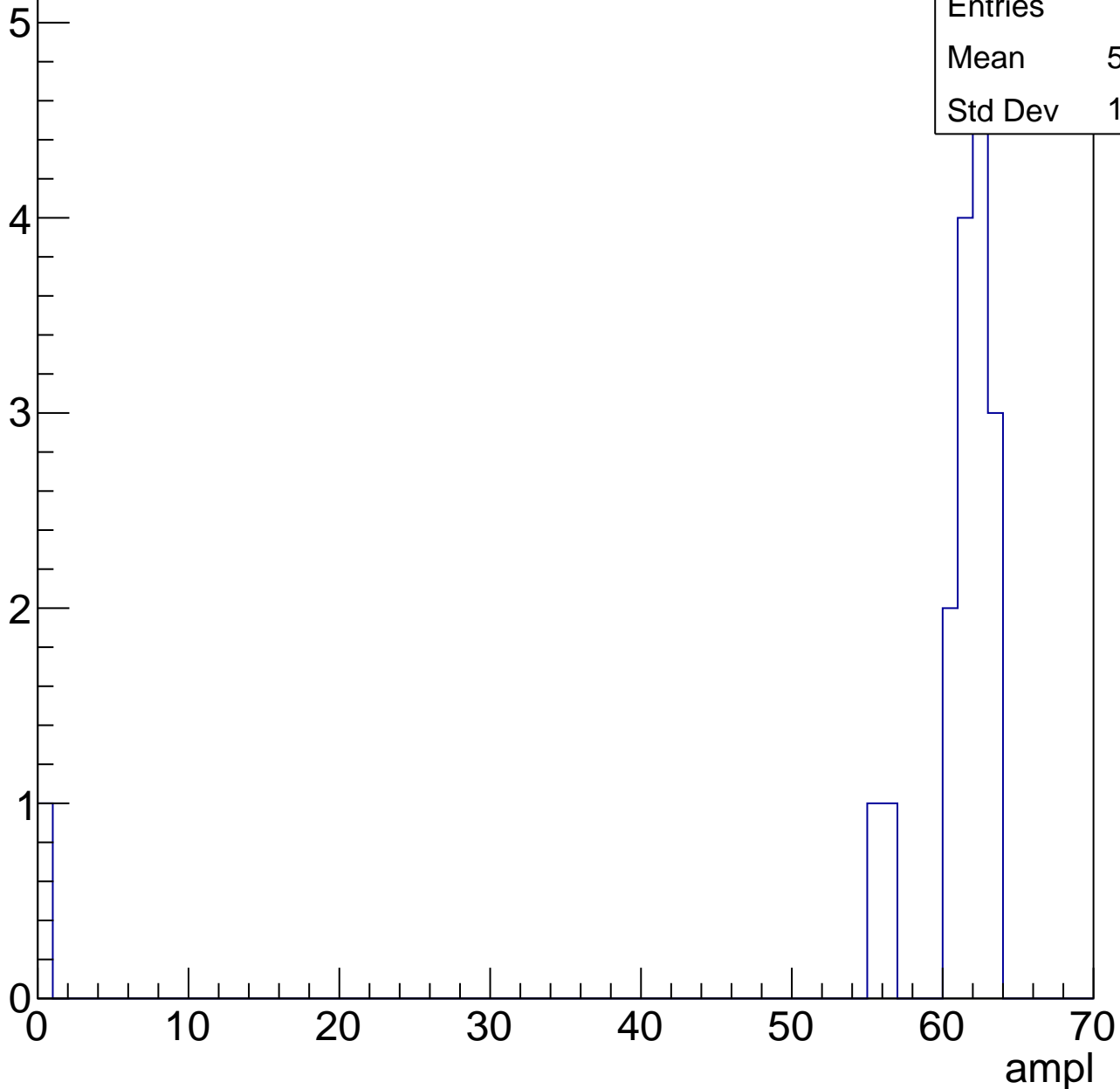


# B1L103S, U2-ch13, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	17
Mean	57.29
Std Dev	14.49





# B1L103S, U2-ch13, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch14, adc0

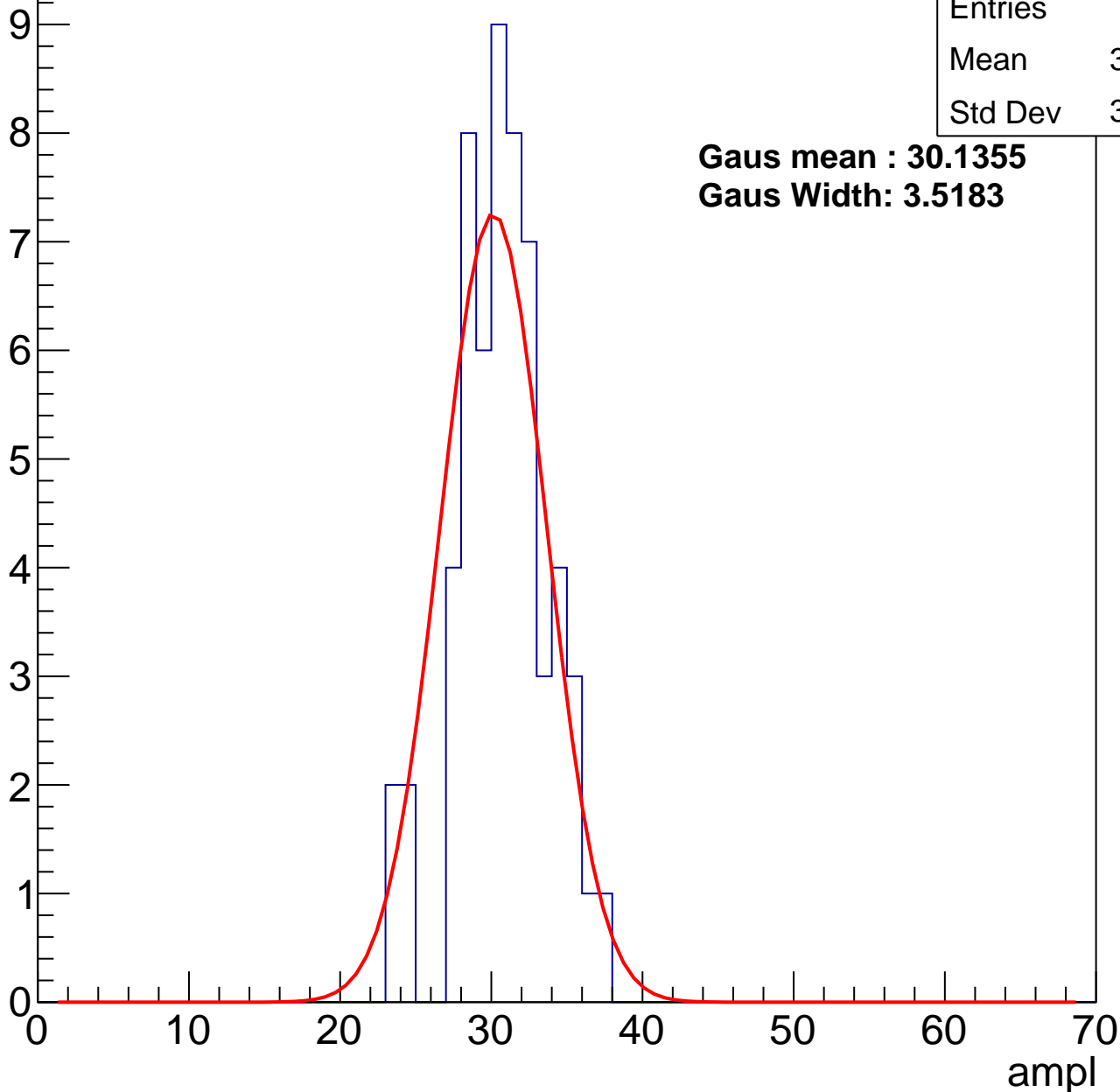
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	30.26
Std Dev	3.015

**Gaus mean : 30.1355**

**Gaus Width: 3.5183**



# B1L103S, U2-ch14, adc1

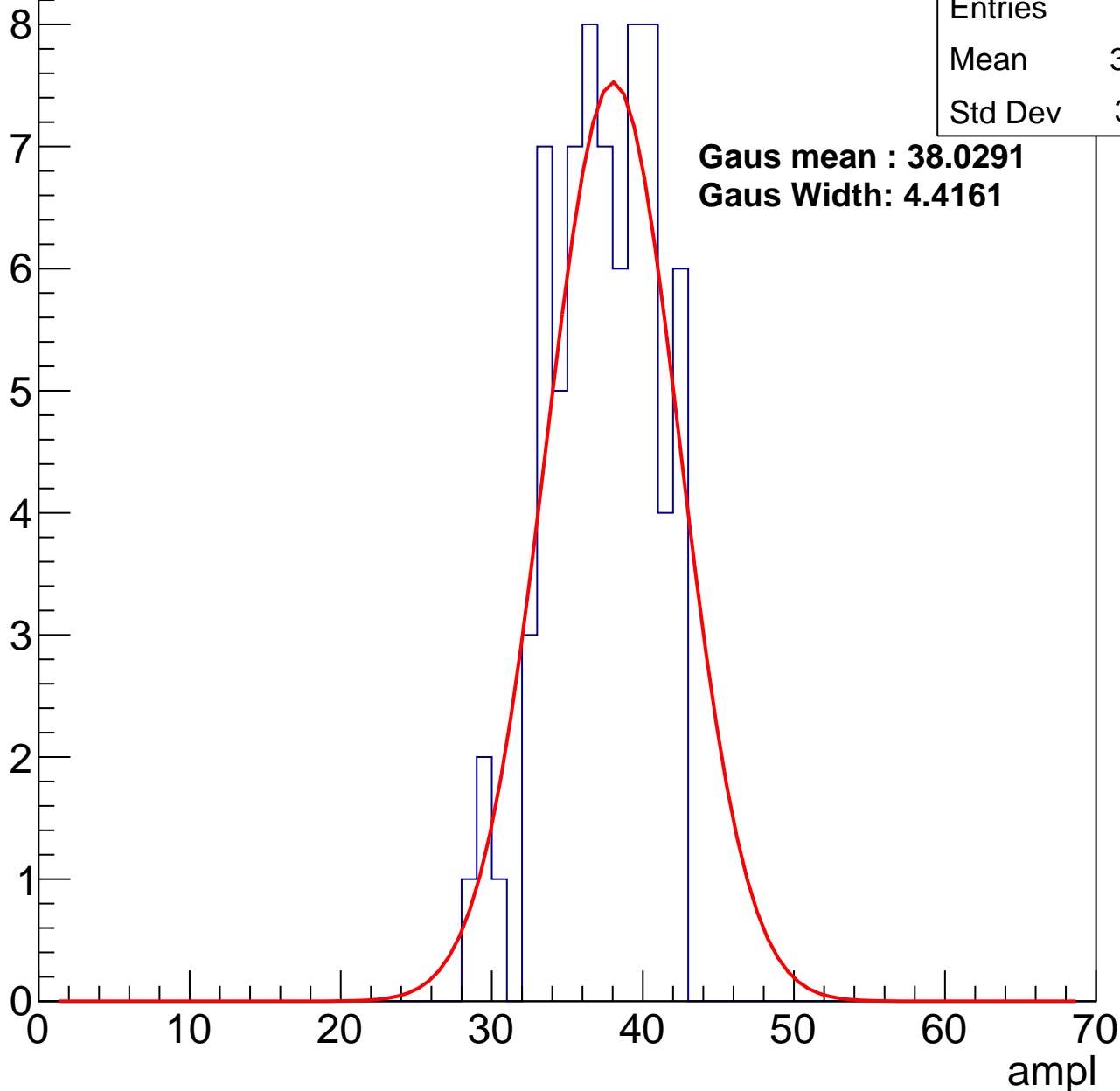
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	36.73
Std Dev	3.401

**Gaus mean : 38.0291**

**Gaus Width: 4.4161**



# B1L103S, U2-ch14, adc2

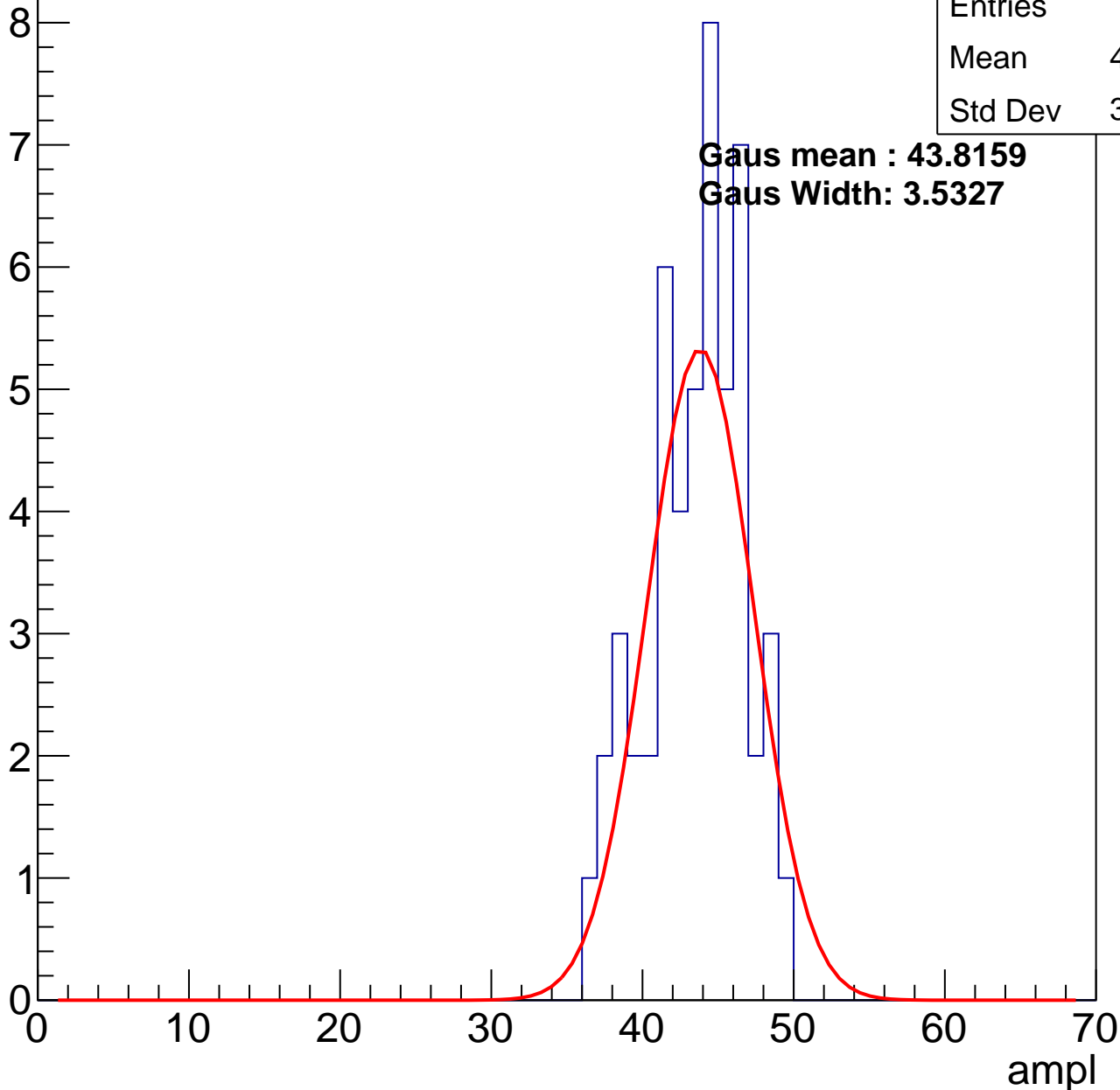
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	43.08
Std Dev	3.155

**Gaus mean : 43.8159**

**Gaus Width: 3.5327**

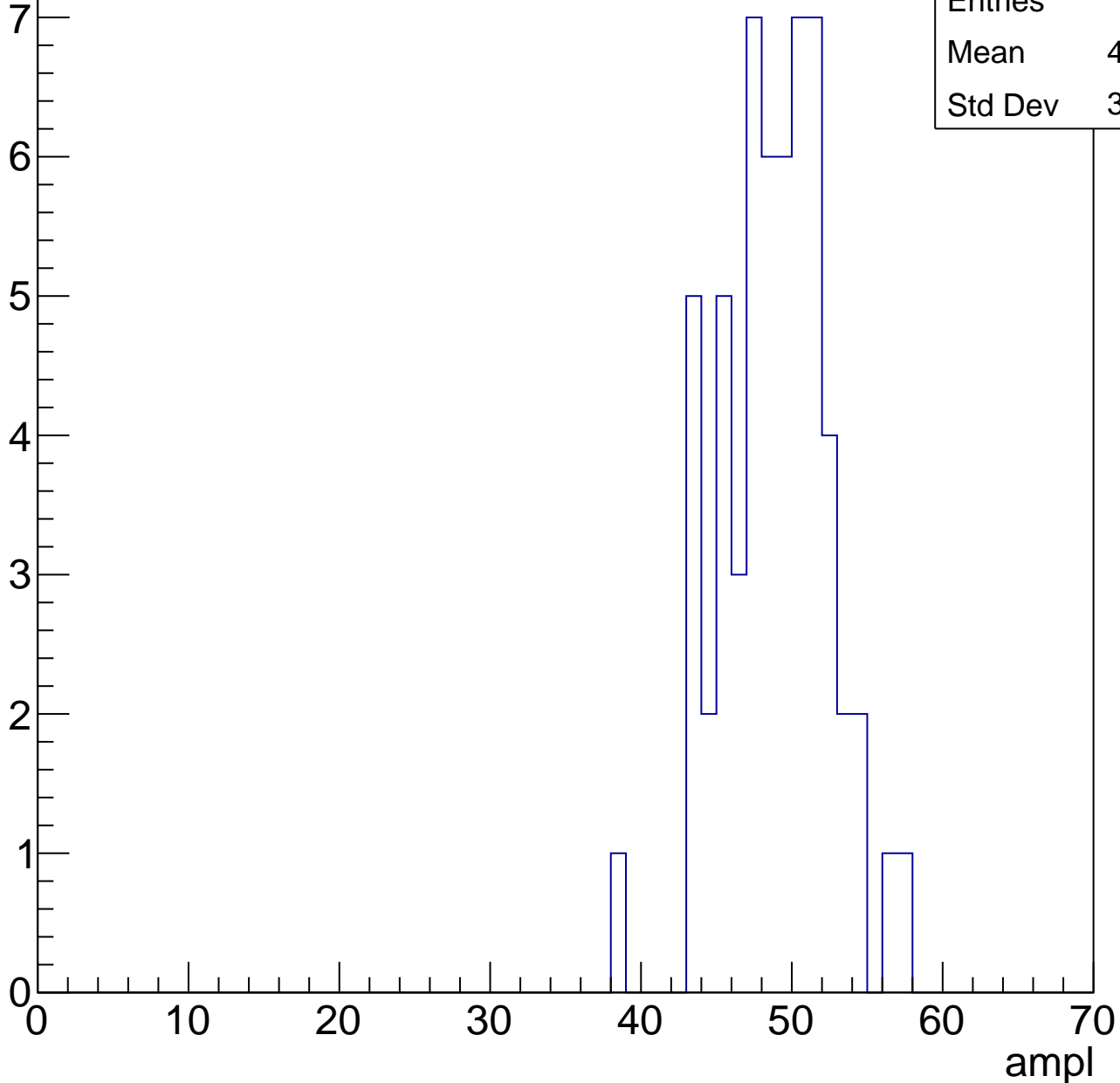


# B1L103S, U2-ch14, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	48.42
Std Dev	3.538

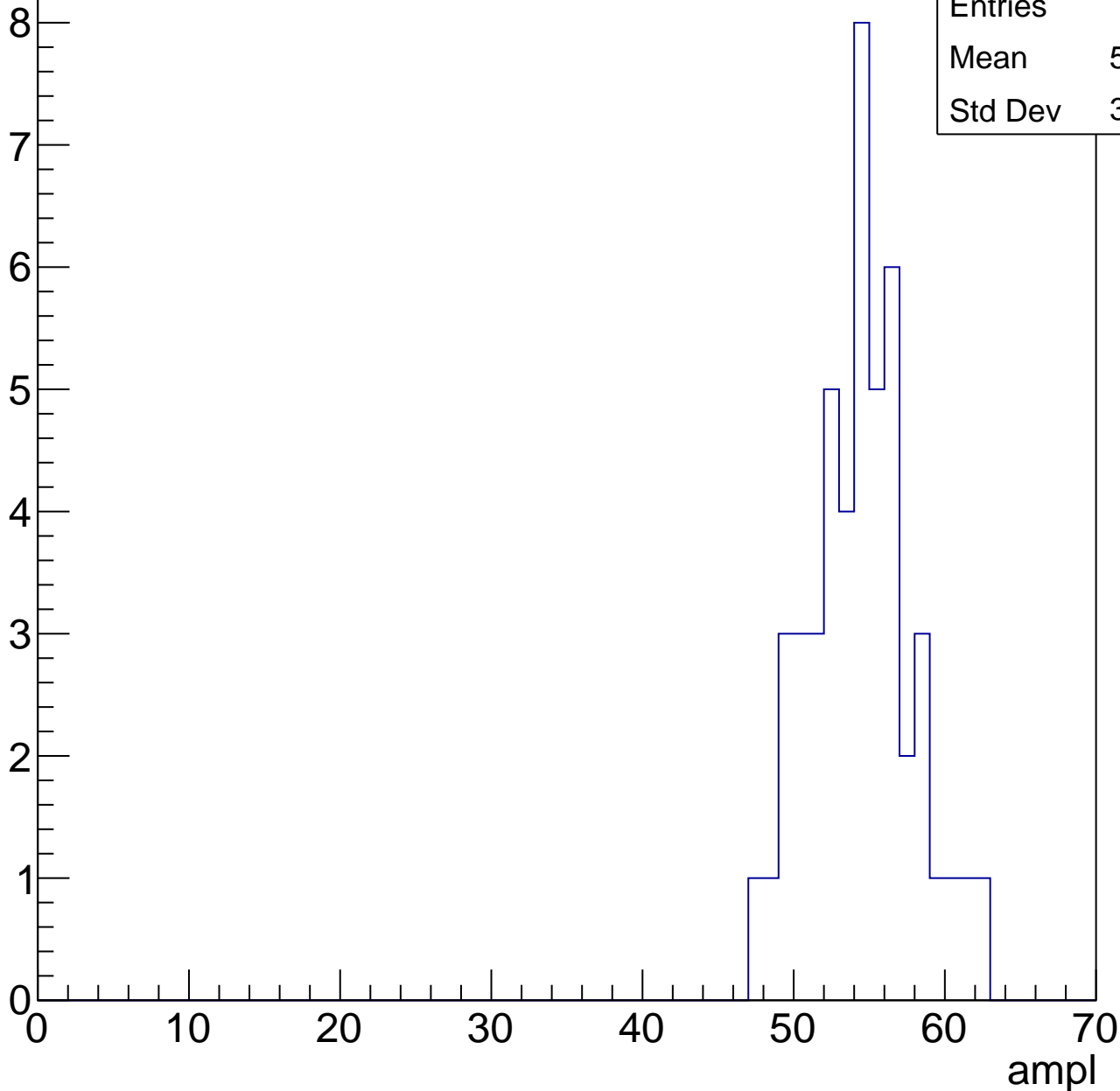


# B1L103S, U2-ch14, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	48
Mean	53.96
Std Dev	3.316



# B1L103S, U2-ch14, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	62
Mean	57.77
Std Dev	7.928

ampl

0

10

20

30

40

50

60

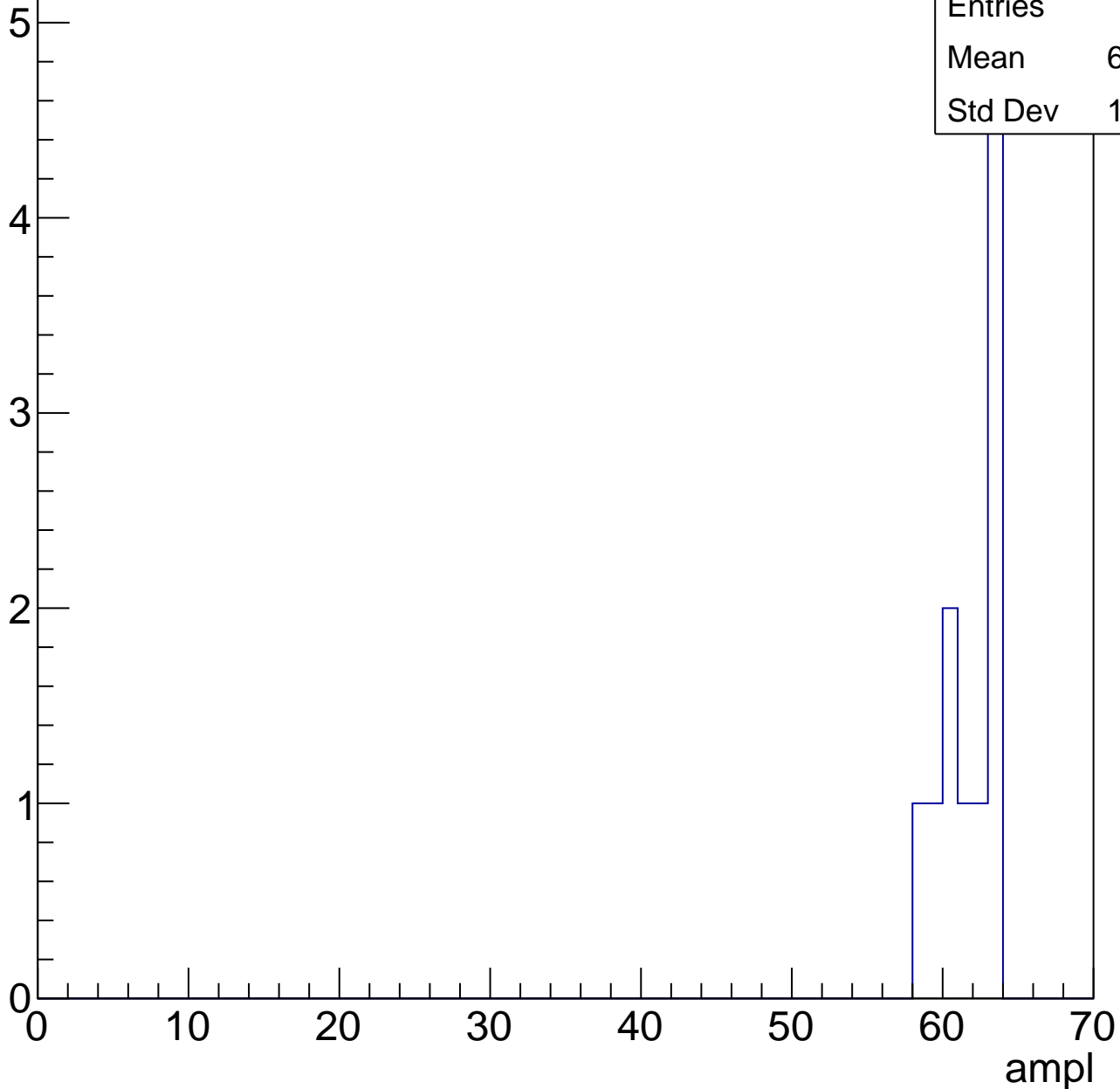
70

# B1L103S, U2-ch14, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	11
Mean	61.36
Std Dev	1.772

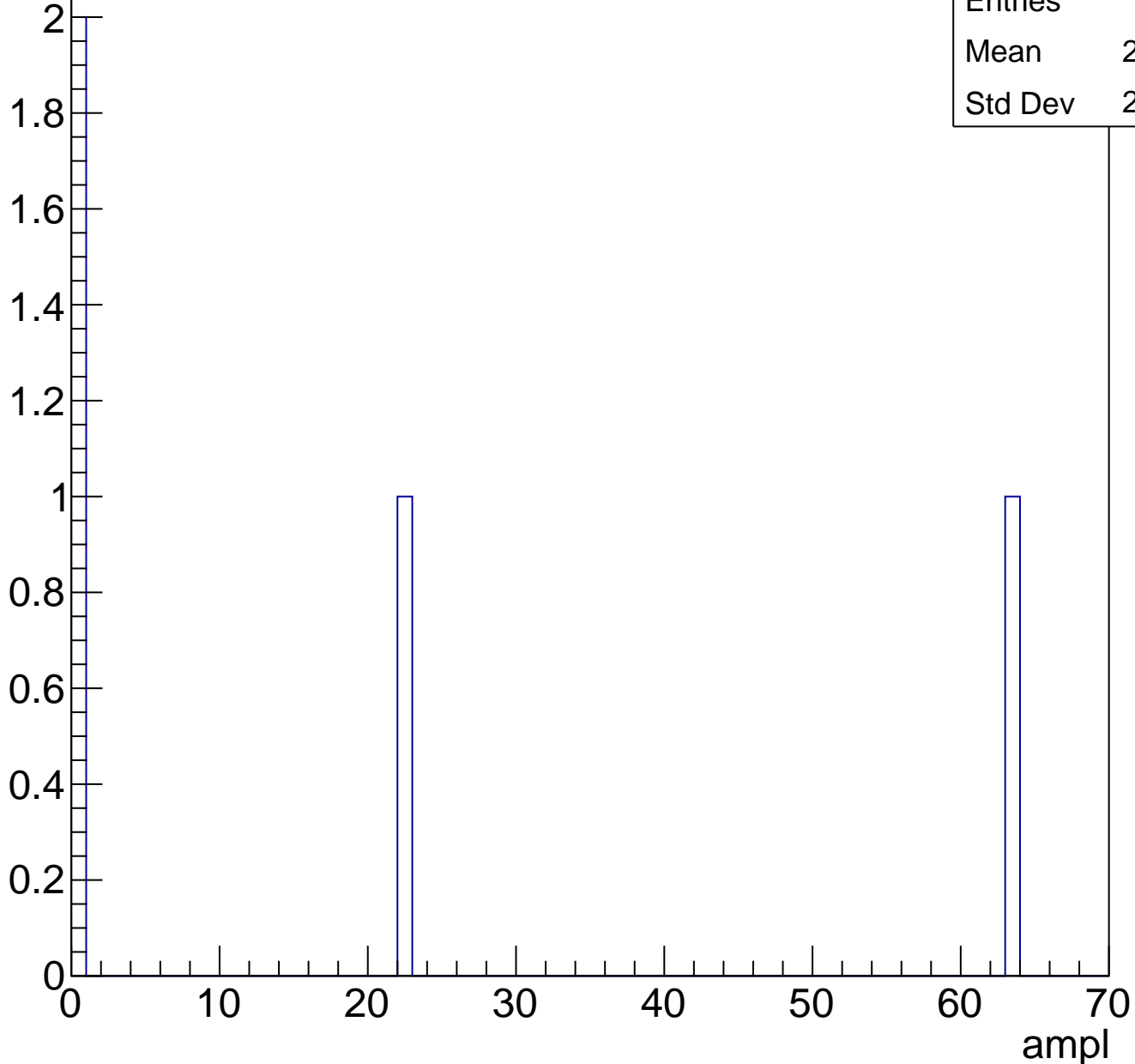




# B1L103S, U2-ch14, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	4
Mean	21.25
Std Dev	25.72

# B1L103S, U2-ch15, adc0

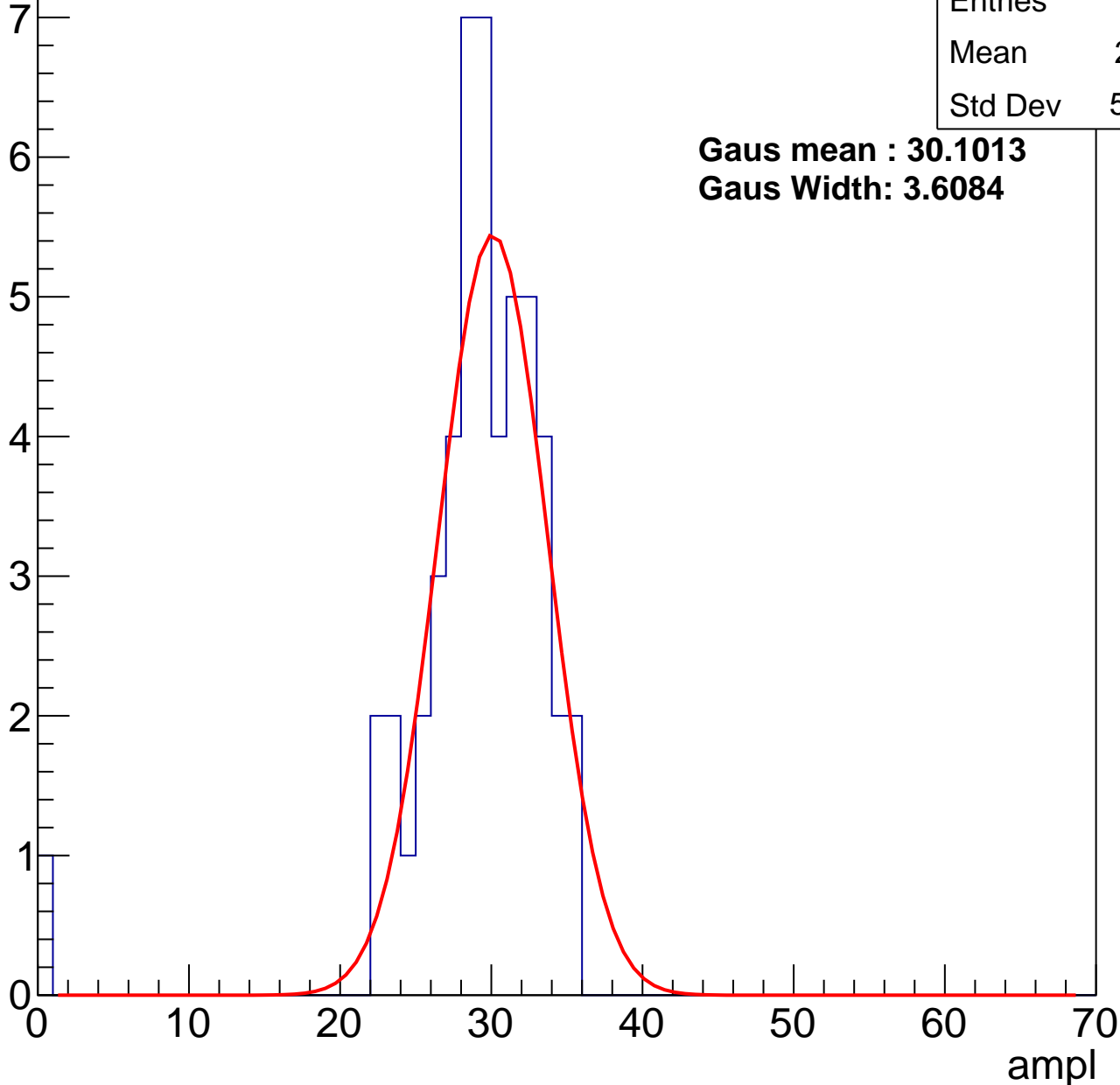
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	28.51
Std Dev	5.165

**Gaus mean : 30.1013**

**Gaus Width: 3.6084**



# B1L103S, U2-ch15, adc1

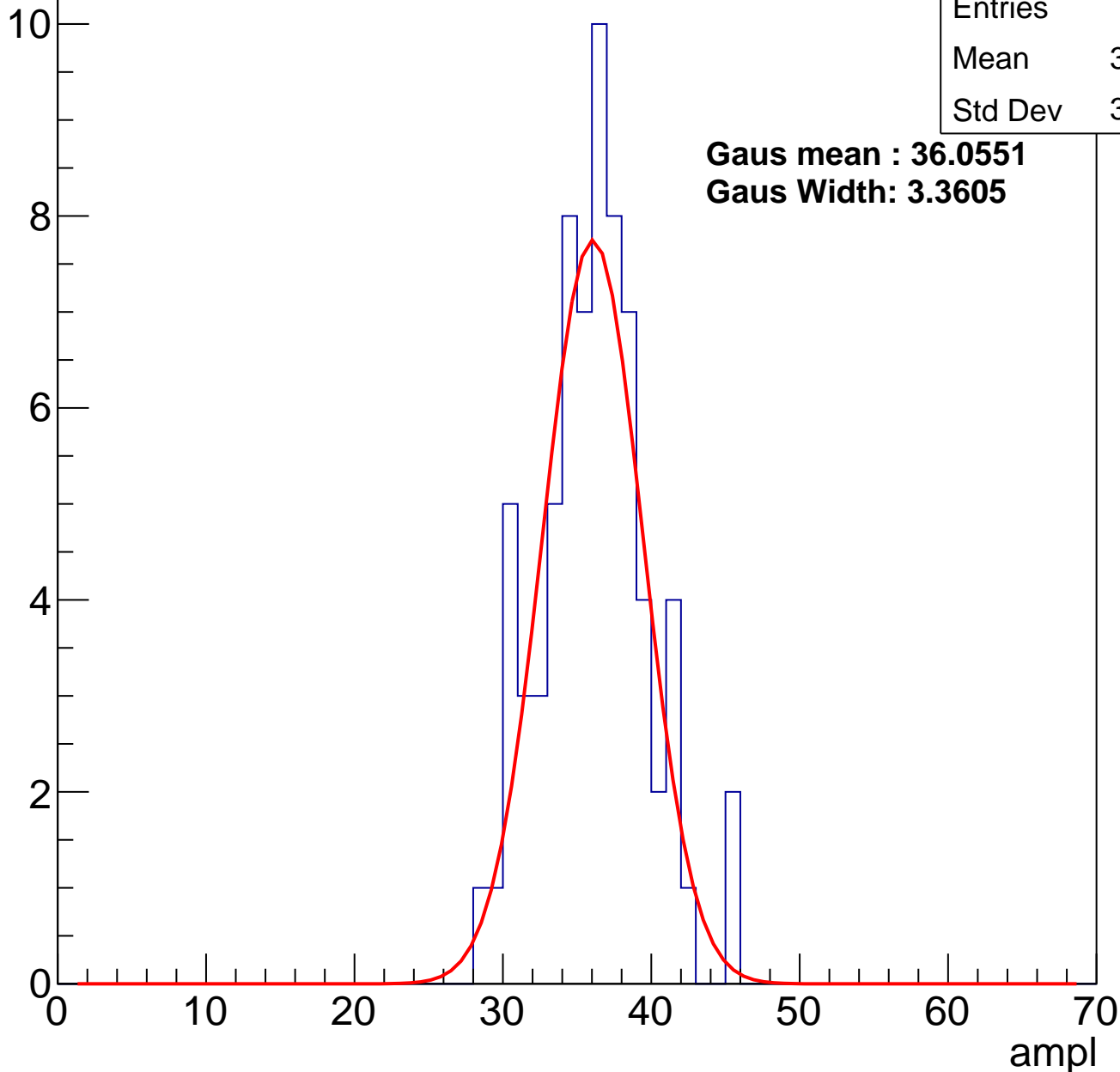
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	71
Mean	35.66
Std Dev	3.548

**Gaus mean : 36.0551**

**Gaus Width: 3.3605**

Entry



# B1L103S, U2-ch15, adc2

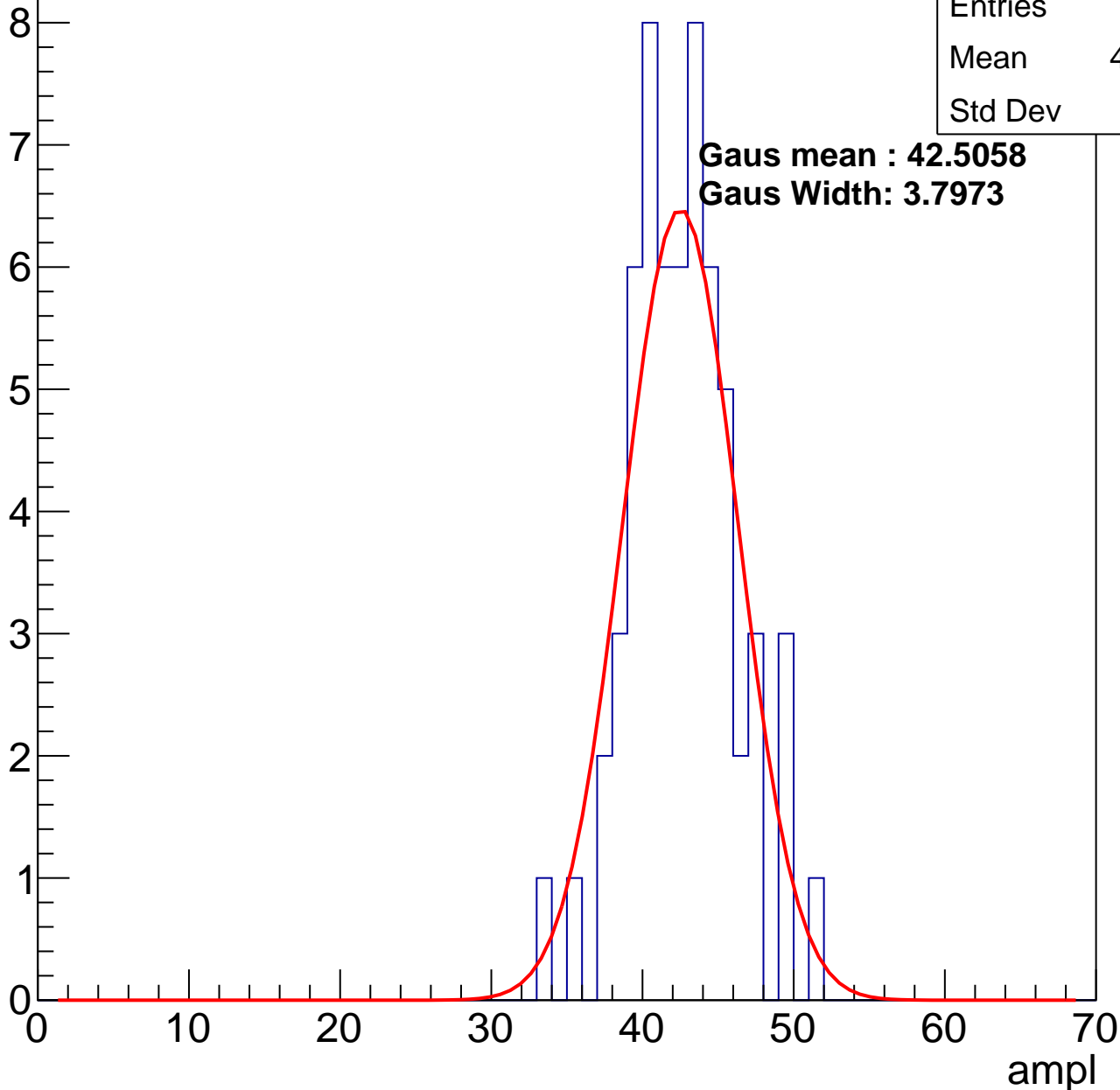
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	42.16
Std Dev	3.46

**Gaus mean : 42.5058**

**Gaus Width: 3.7973**



# B1L103S, U2-ch15, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

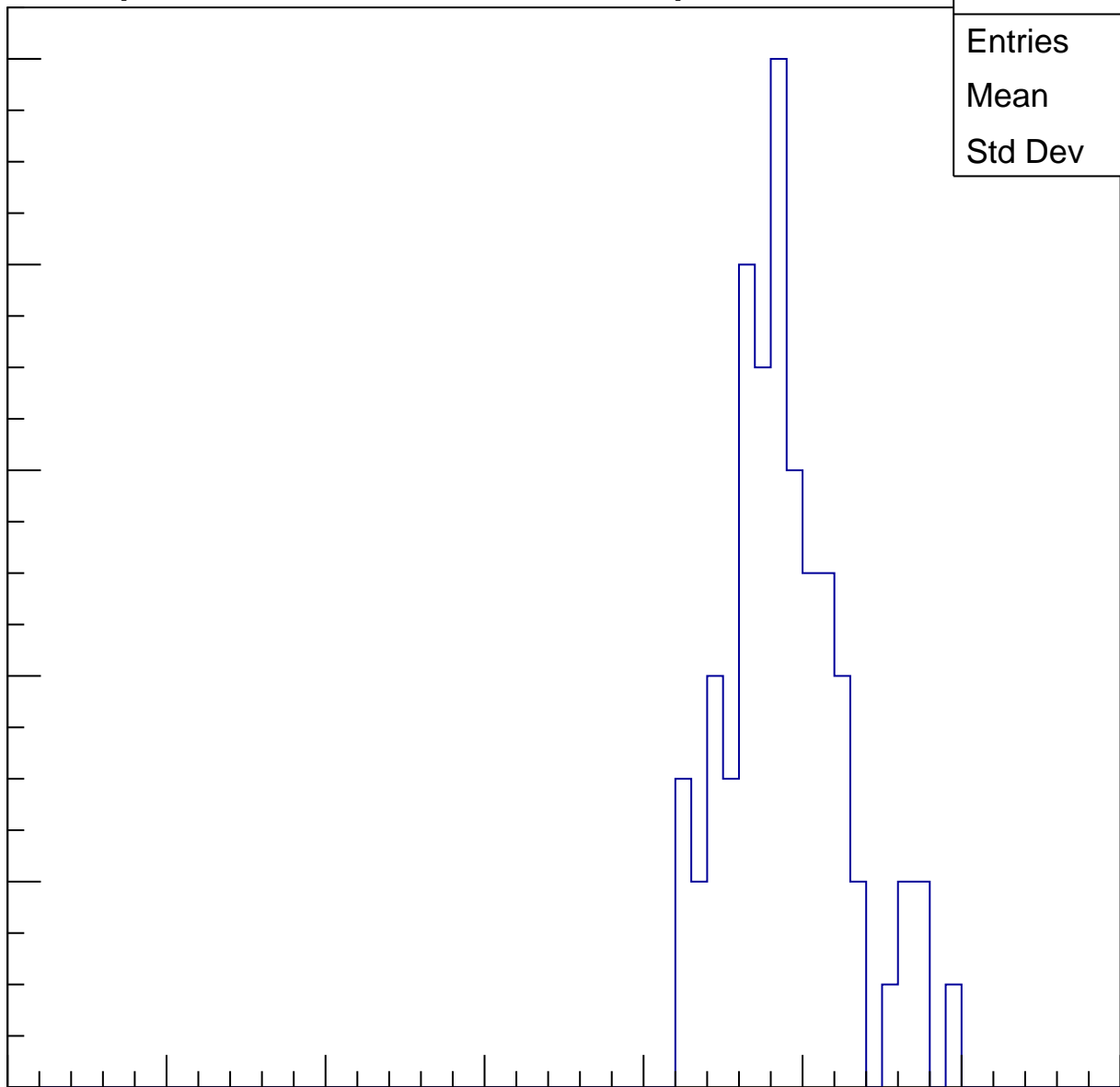
Entries	65
Mean	48.51
Std Dev	3.754

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

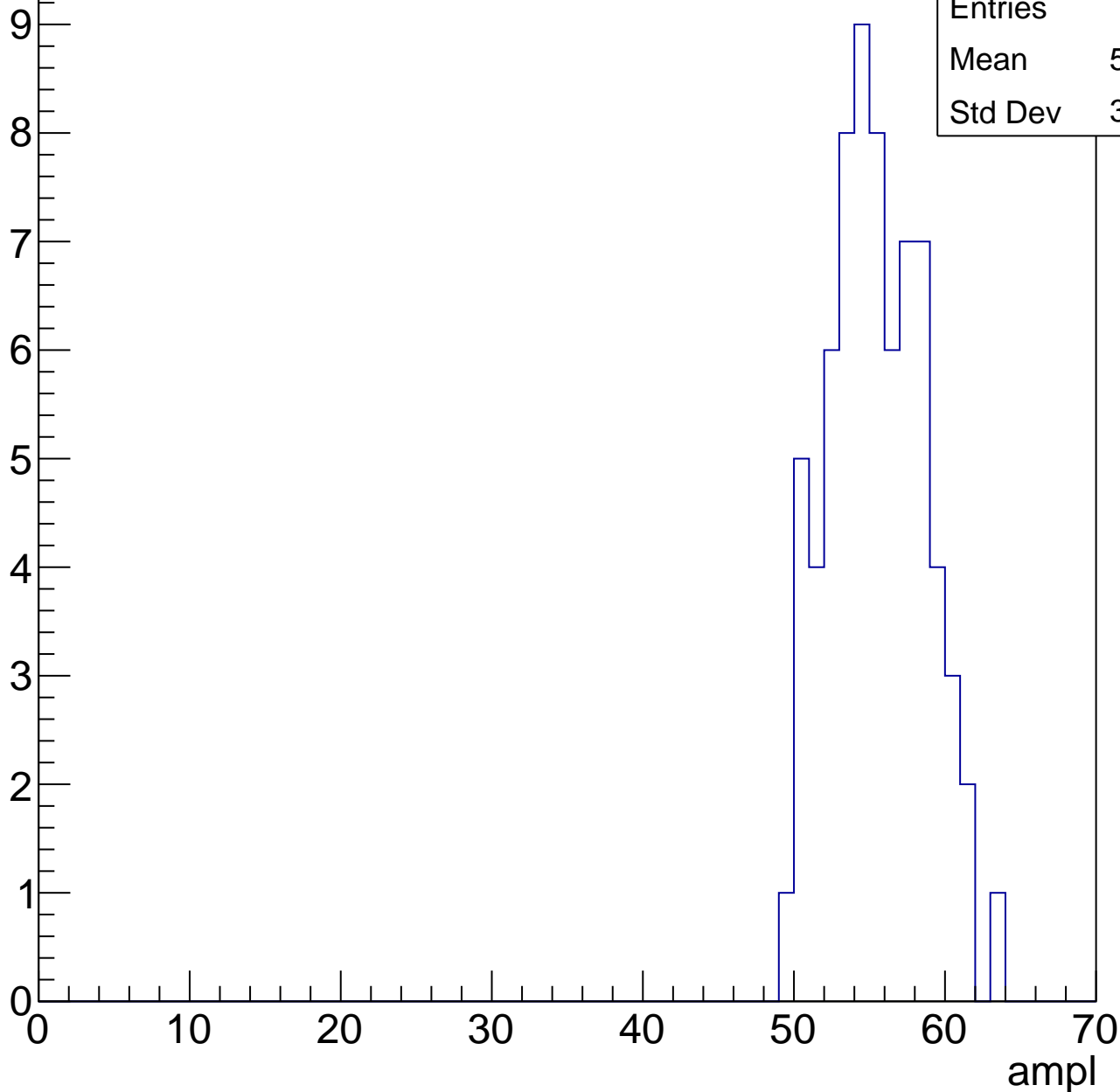


# B1L103S, U2-ch15, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	55.03
Std Dev	3.122

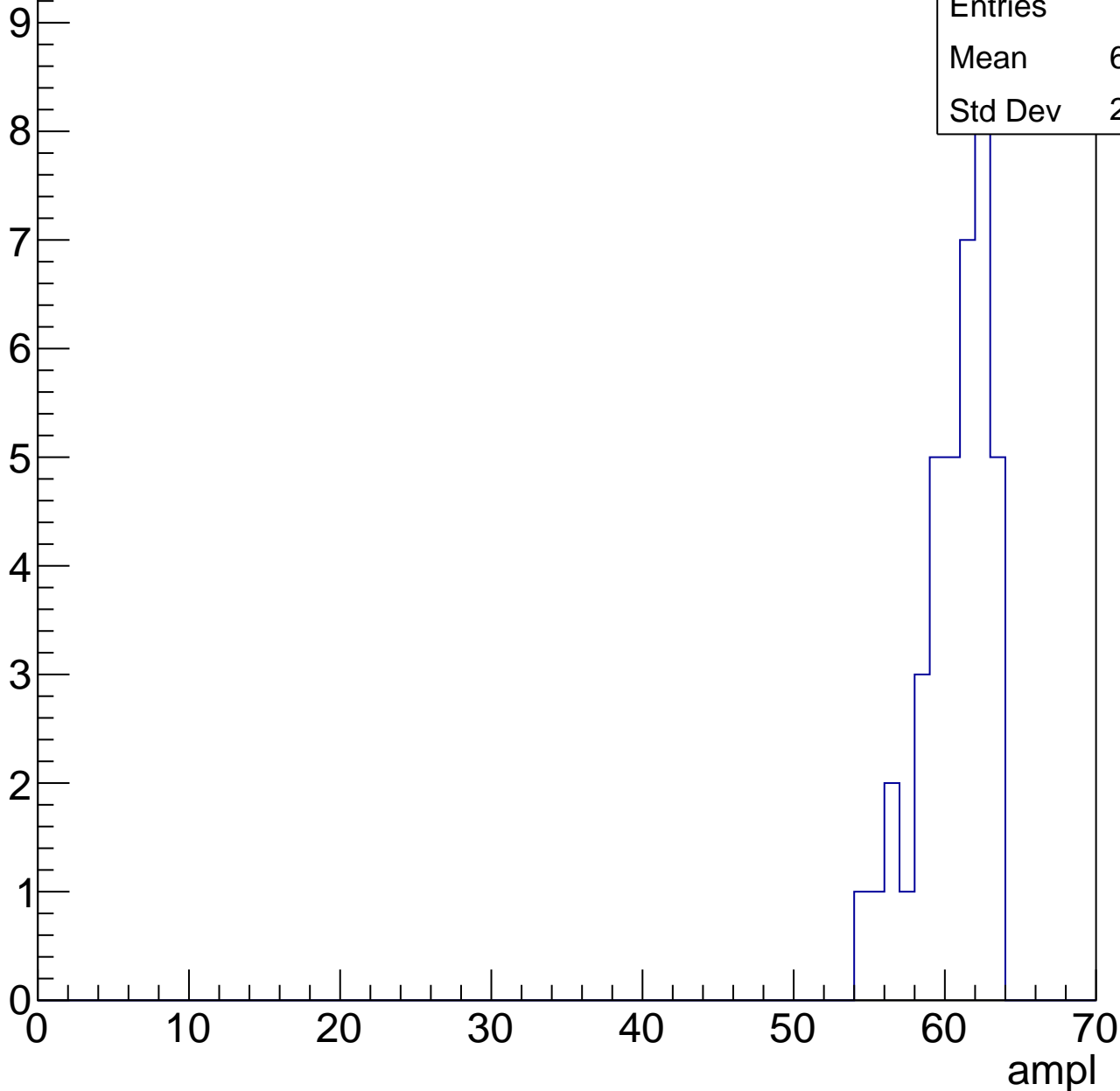


# B1L103S, U2-ch15, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

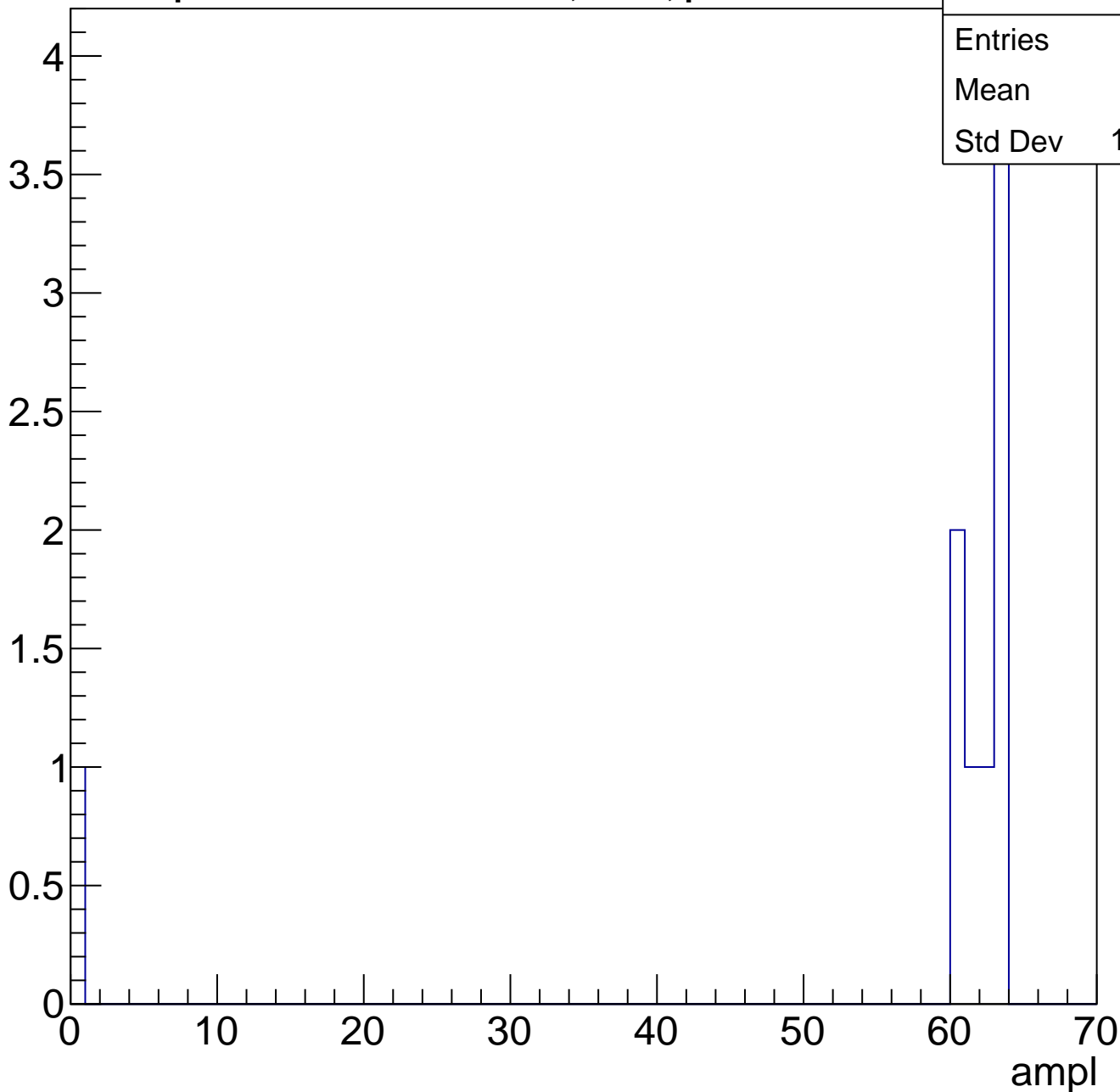
Entries	39
Mean	60.18
Std Dev	2.297



# B1L103S, U2-ch15, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U2-ch15, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U2-ch16, adc0

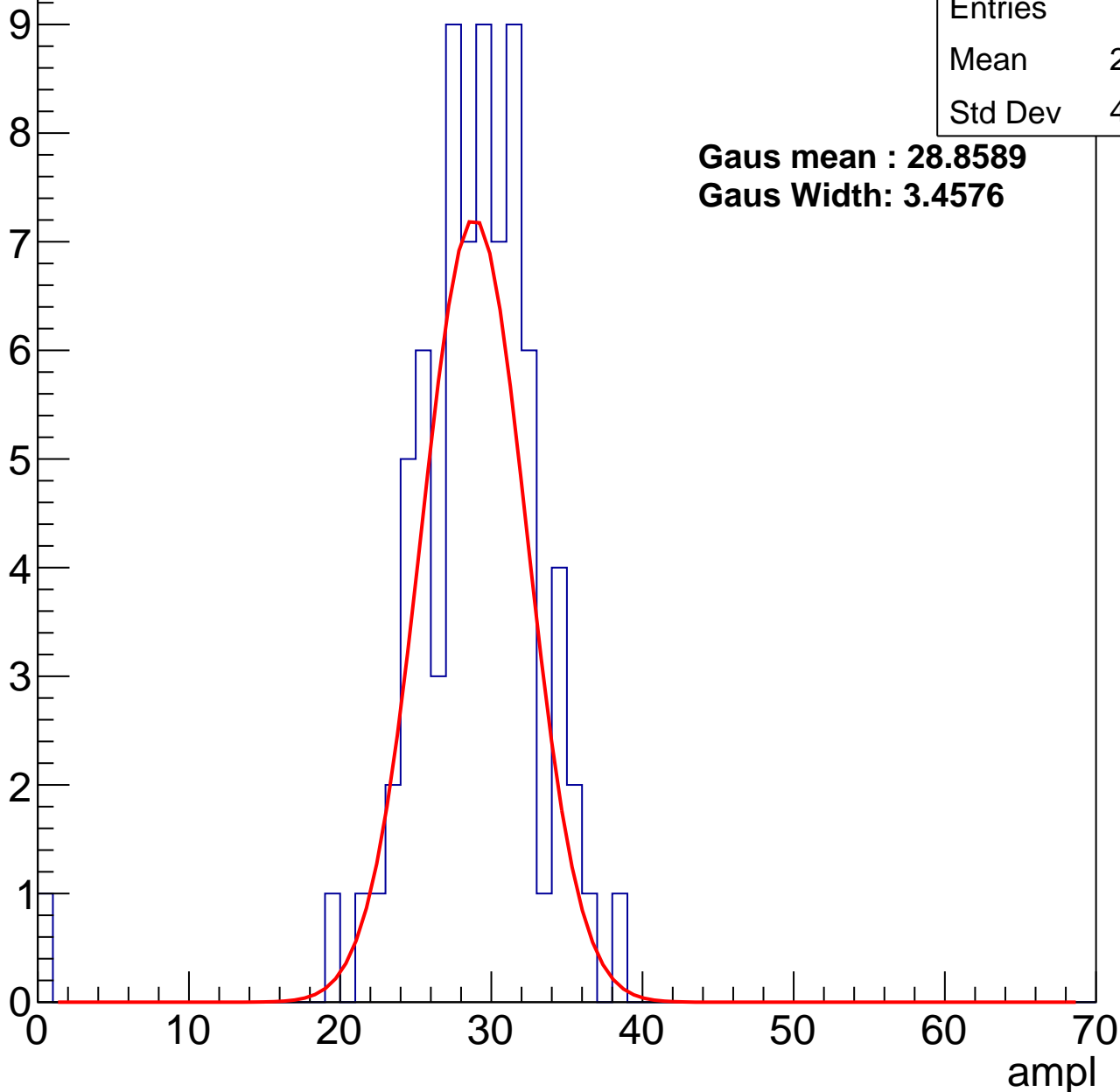
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	28.29
Std Dev	4.858

**Gaus mean : 28.8589**

**Gaus Width: 3.4576**



# B1L103S, U2-ch16, adc1

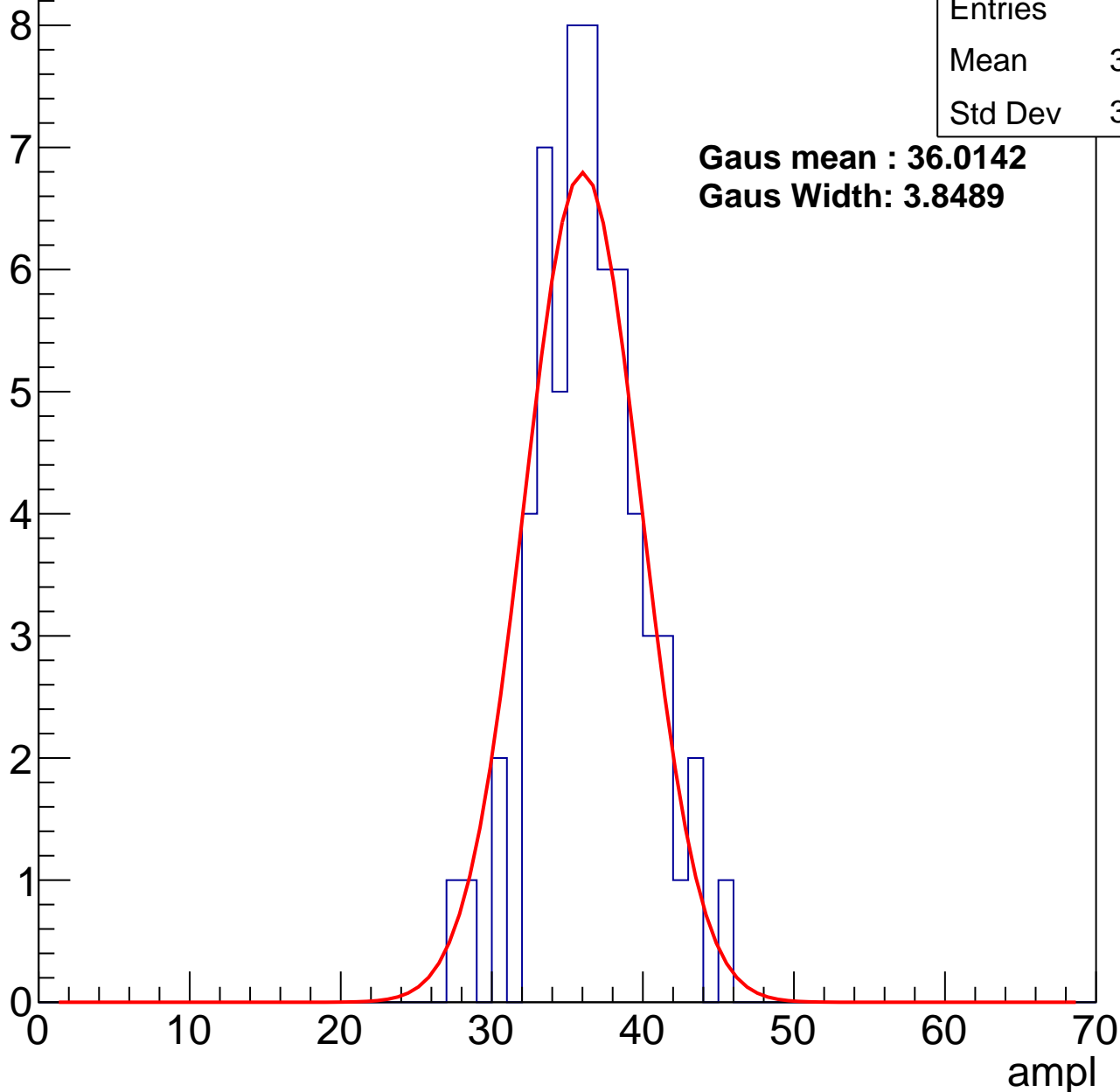
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	36.03
Std Dev	3.538

**Gaus mean : 36.0142**

**Gaus Width: 3.8489**



# B1L103S, U2-ch16, adc2

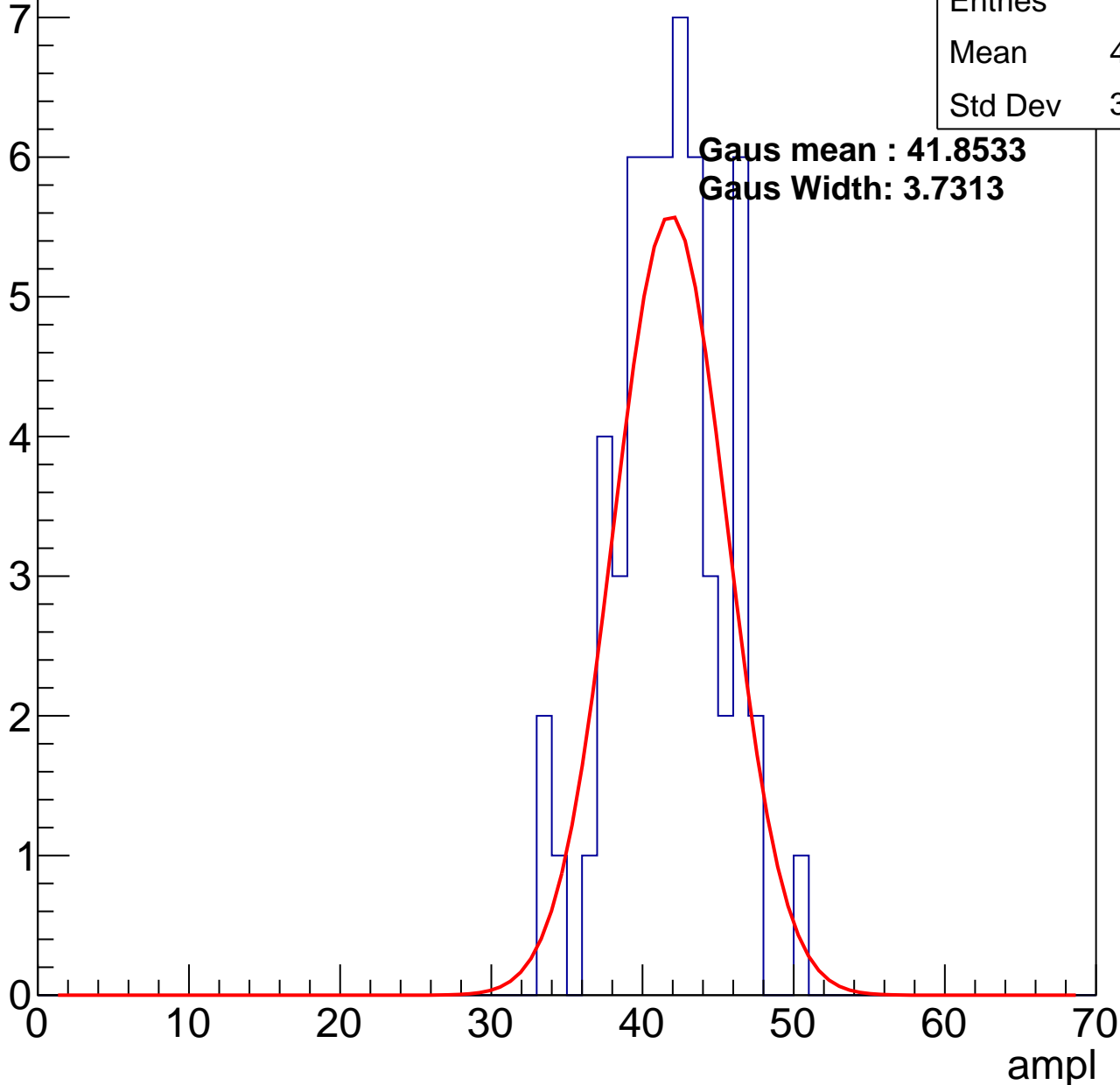
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	41.29
Std Dev	3.564

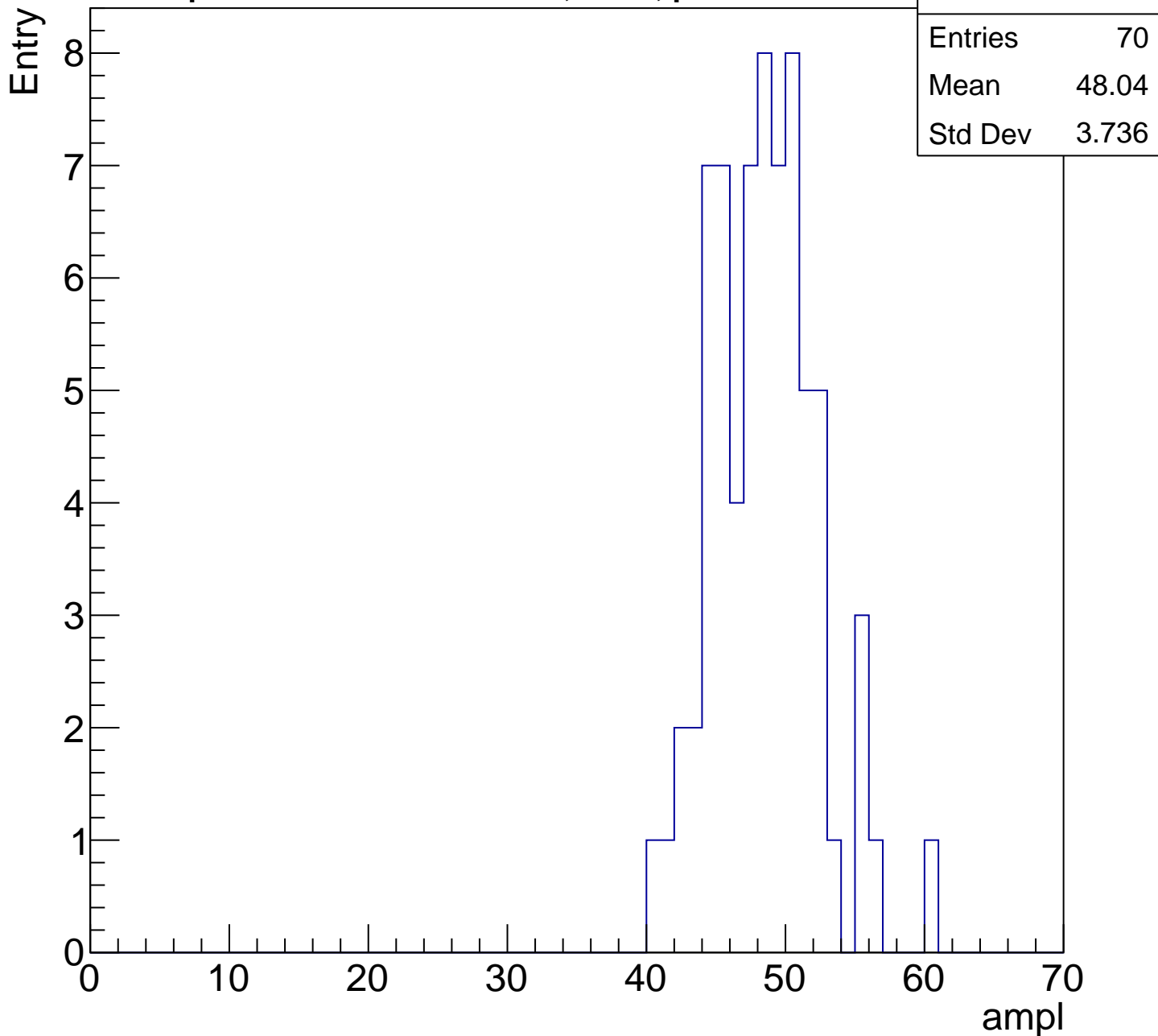
**Gaus mean : 41.8533**

**Gaus Width: 3.7313**



# B1L103S, U2-ch16, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

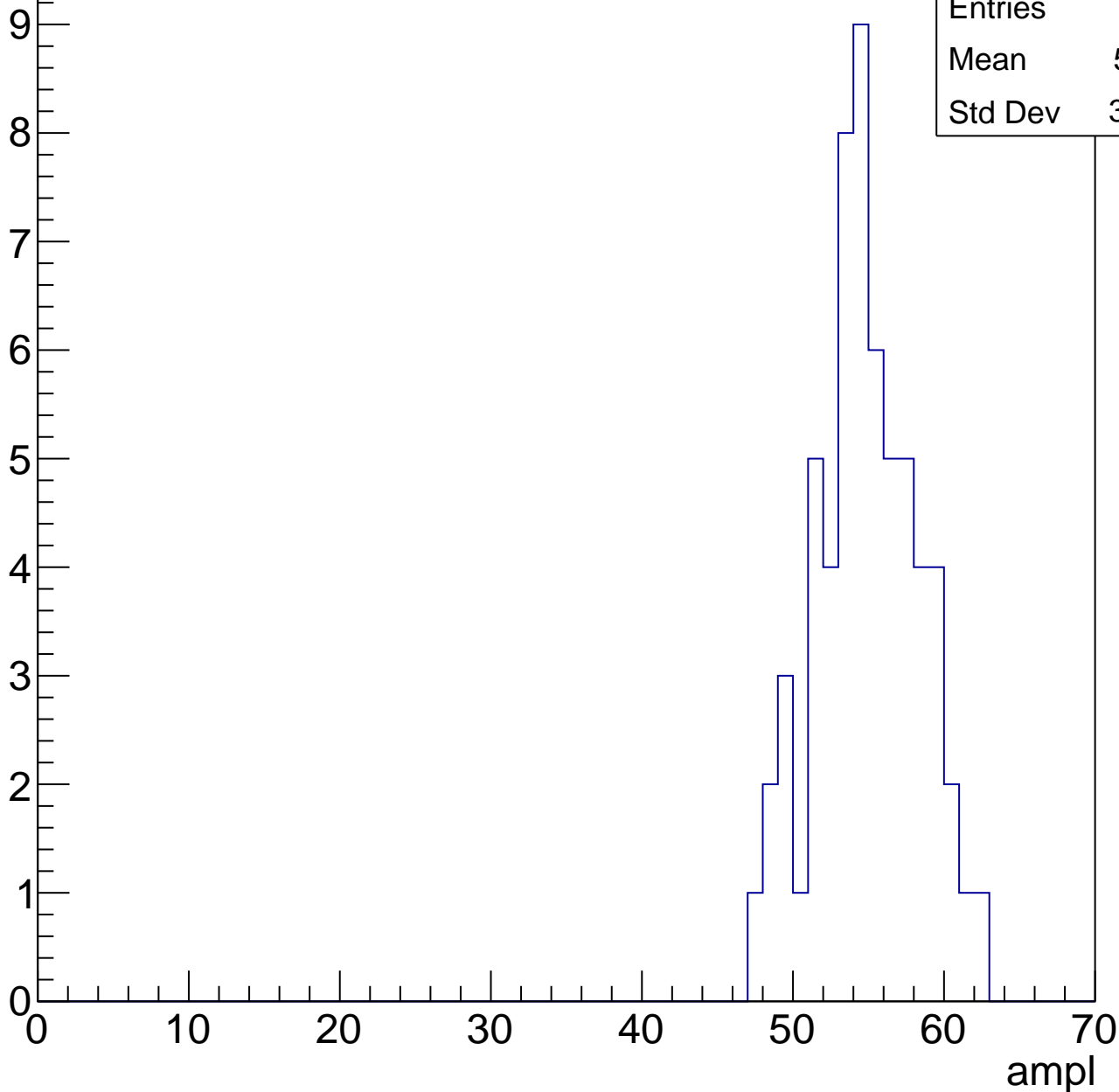


# B1L103S, U2-ch16, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	54.41
Std Dev	3.365

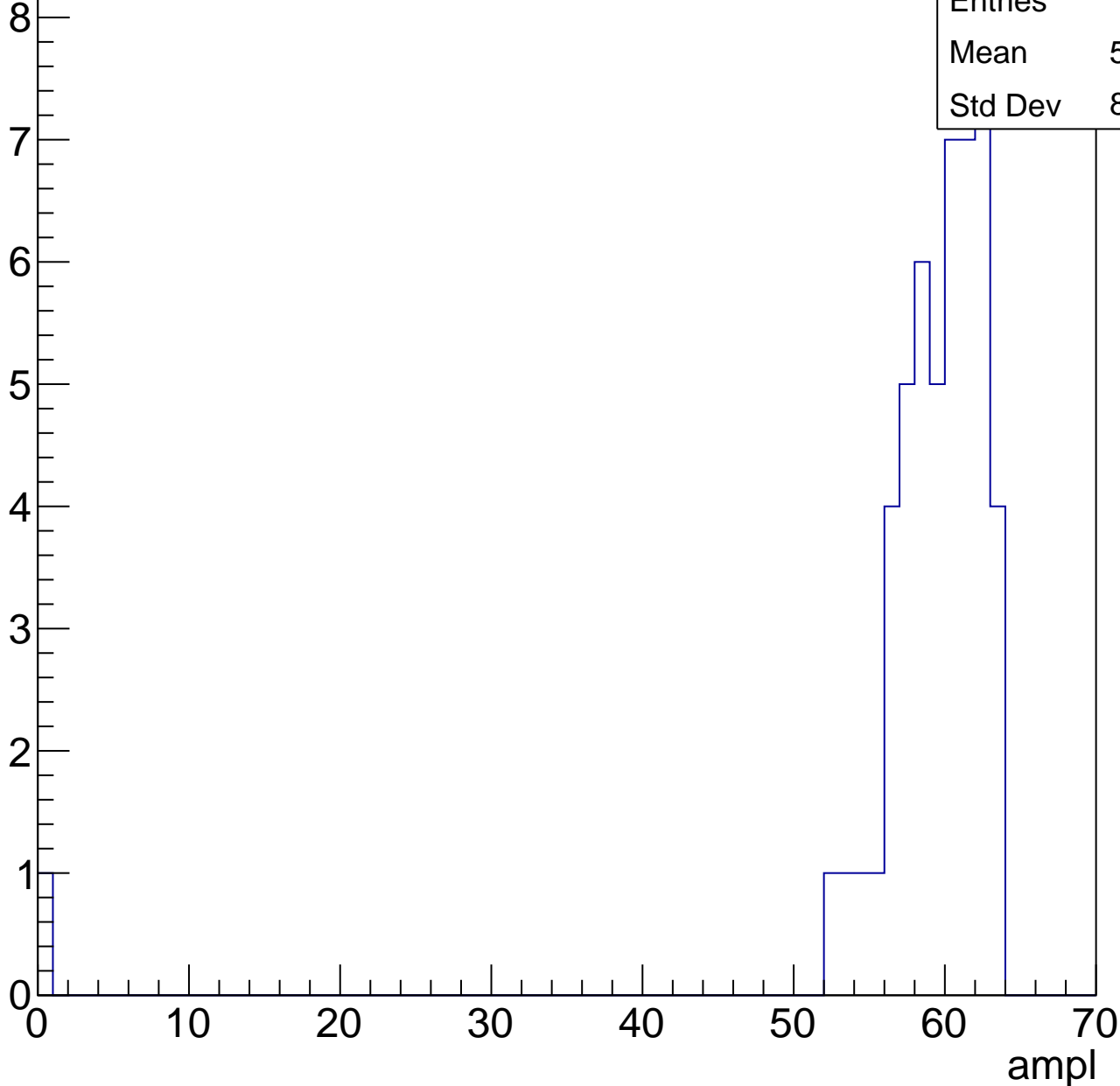


# B1L103S, U2-ch16, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	58.06
Std Dev	8.626

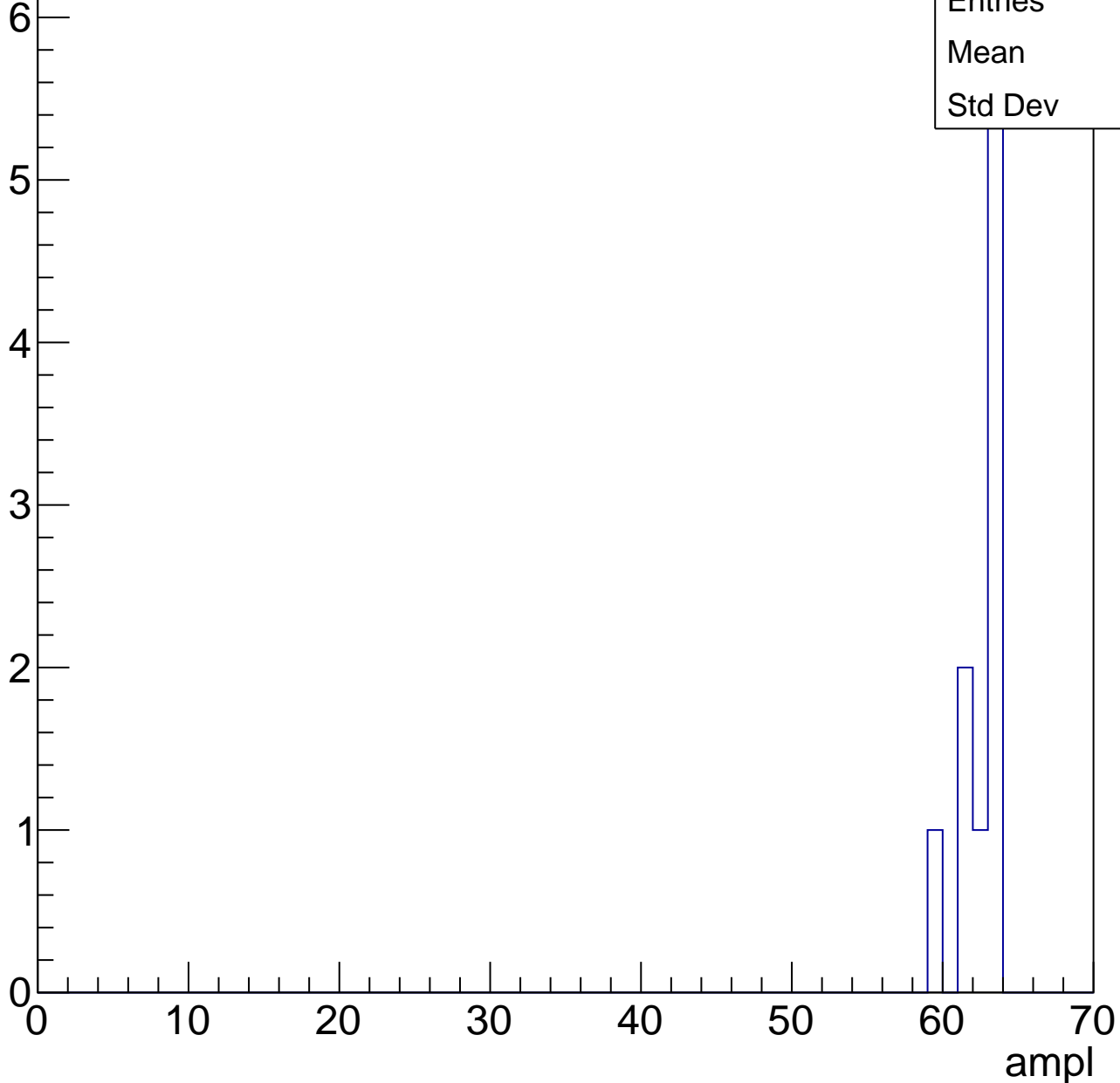


# B1L103S, U2-ch16, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	10
Mean	62.1
Std Dev	1.3





# B1L103S, U2-ch16, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L103S, U2-ch17, adc0

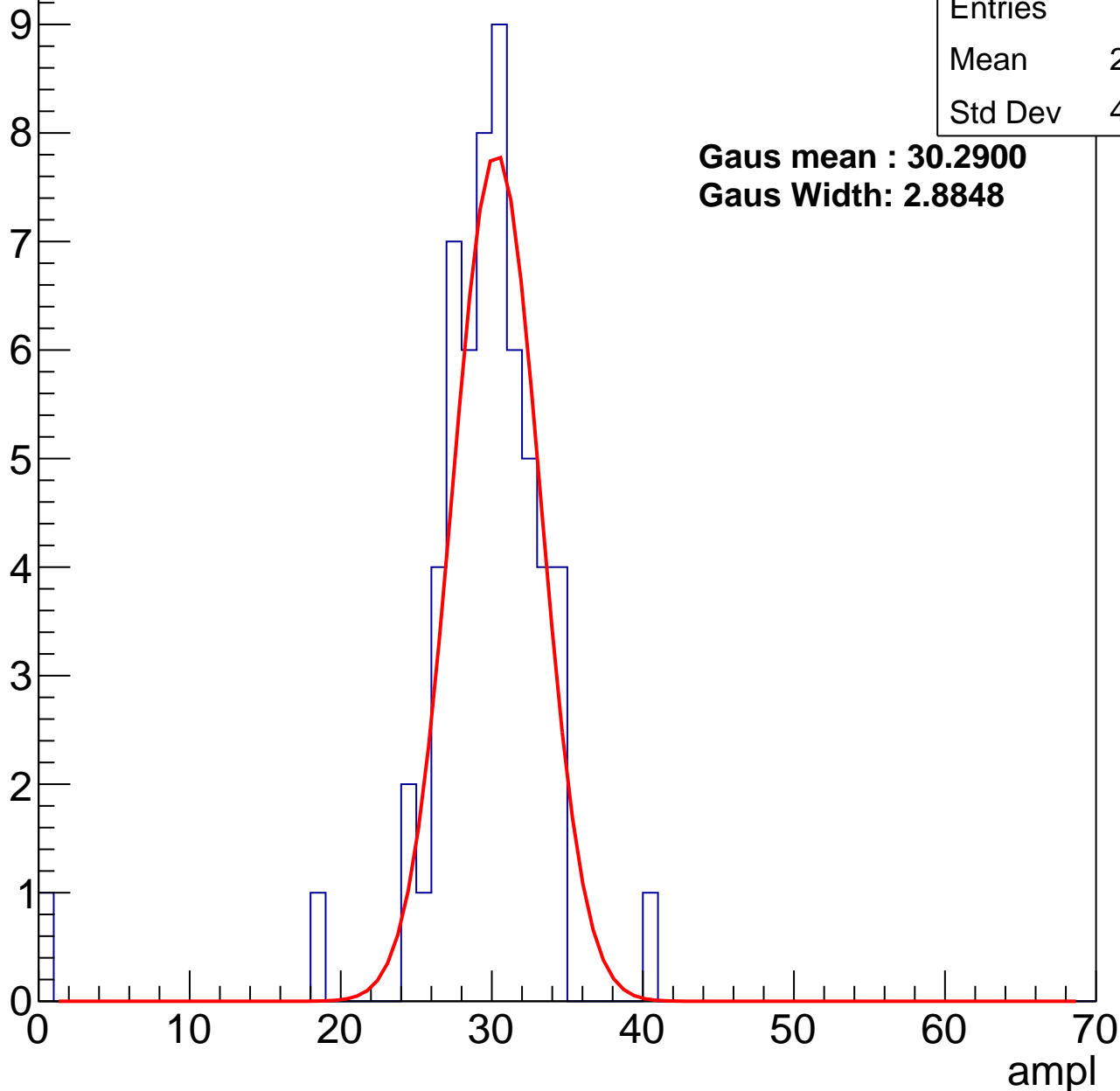
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	28.95
Std Dev	4.976

**Gaus mean : 30.2900**

**Gaus Width: 2.8848**



# B1L103S, U2-ch17, adc1

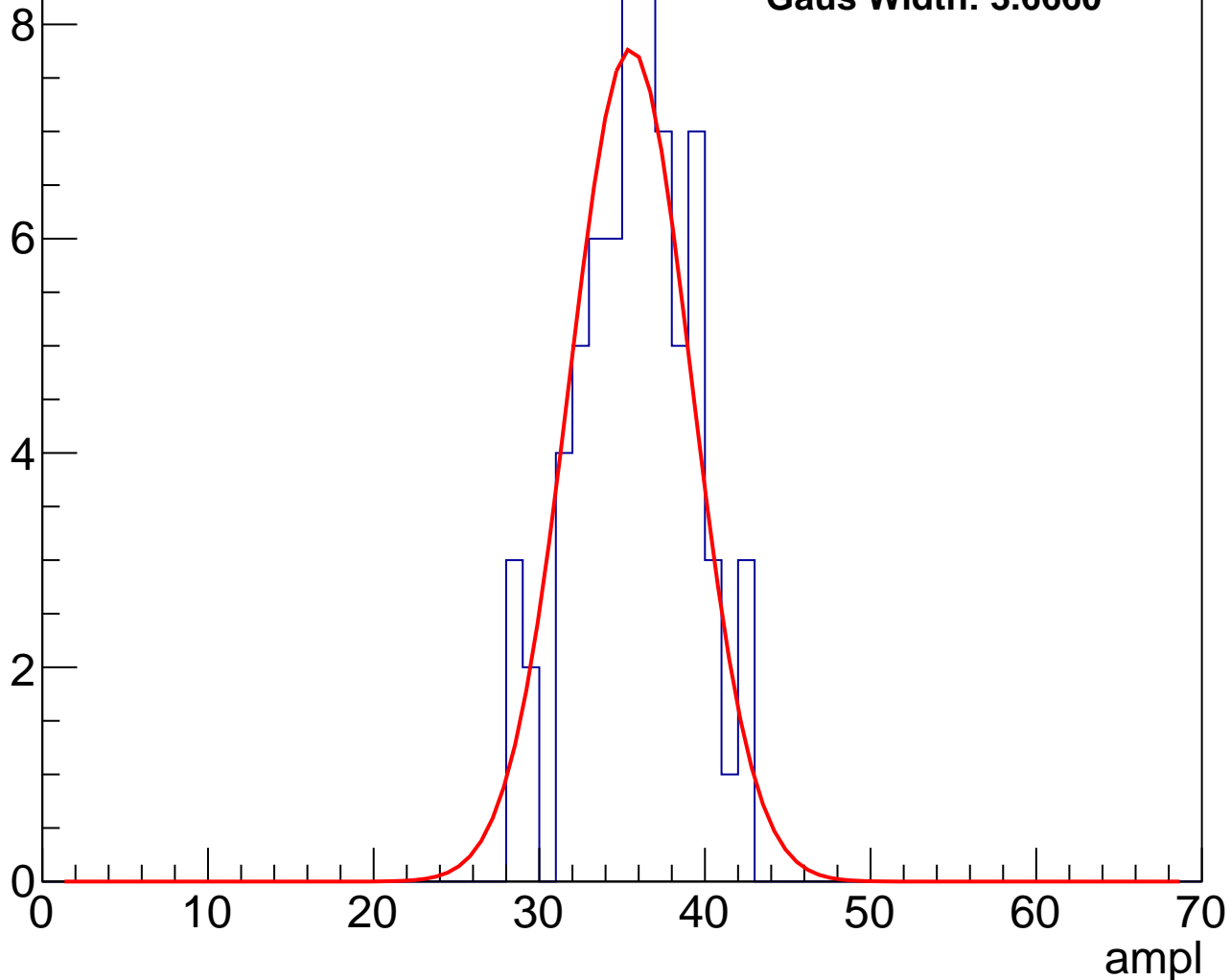
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	35.37
Std Dev	3.358

**Gaus mean : 35.5072**

**Gaus Width: 3.6660**



# B1L103S, U2-ch17, adc2

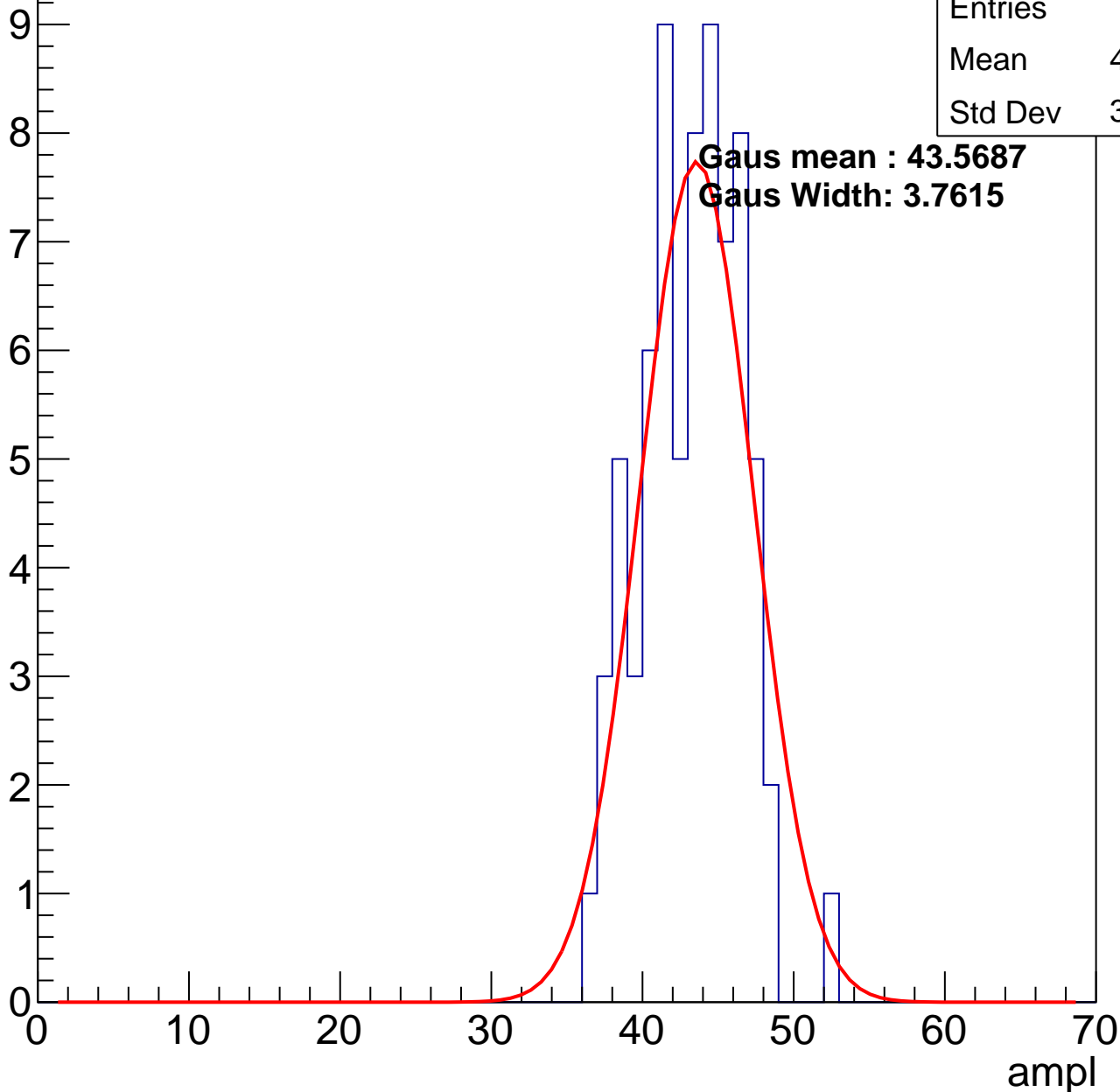
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	42.76
Std Dev	3.208

**Gaus mean : 43.5687**

**Gaus Width: 3.7615**



# B1L103S, U2-ch17, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	65
Mean	49.65
Std Dev	3.51

Entry

10

8

6

4

2

0

0

10

20

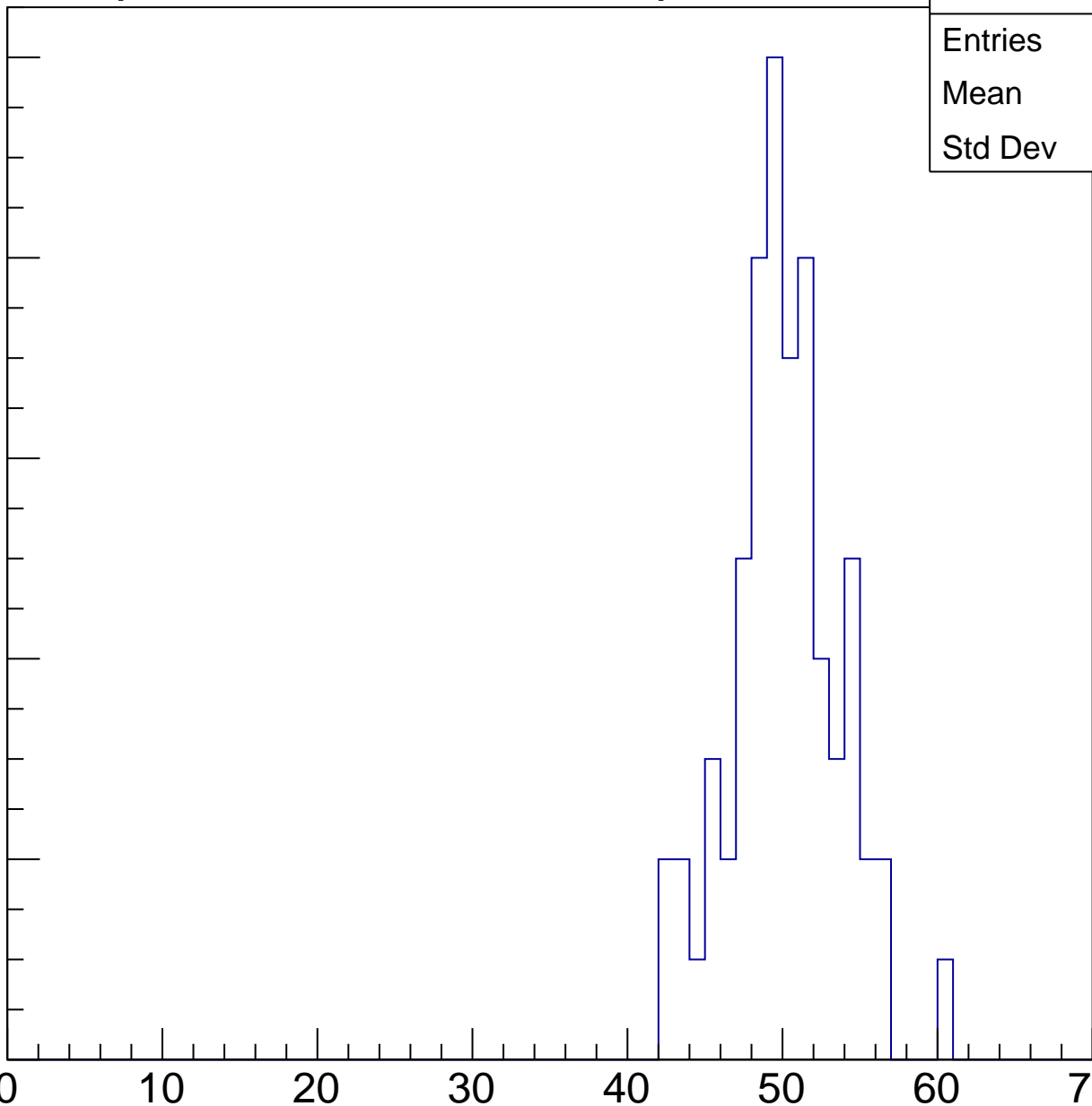
30

40

50

60

ampl

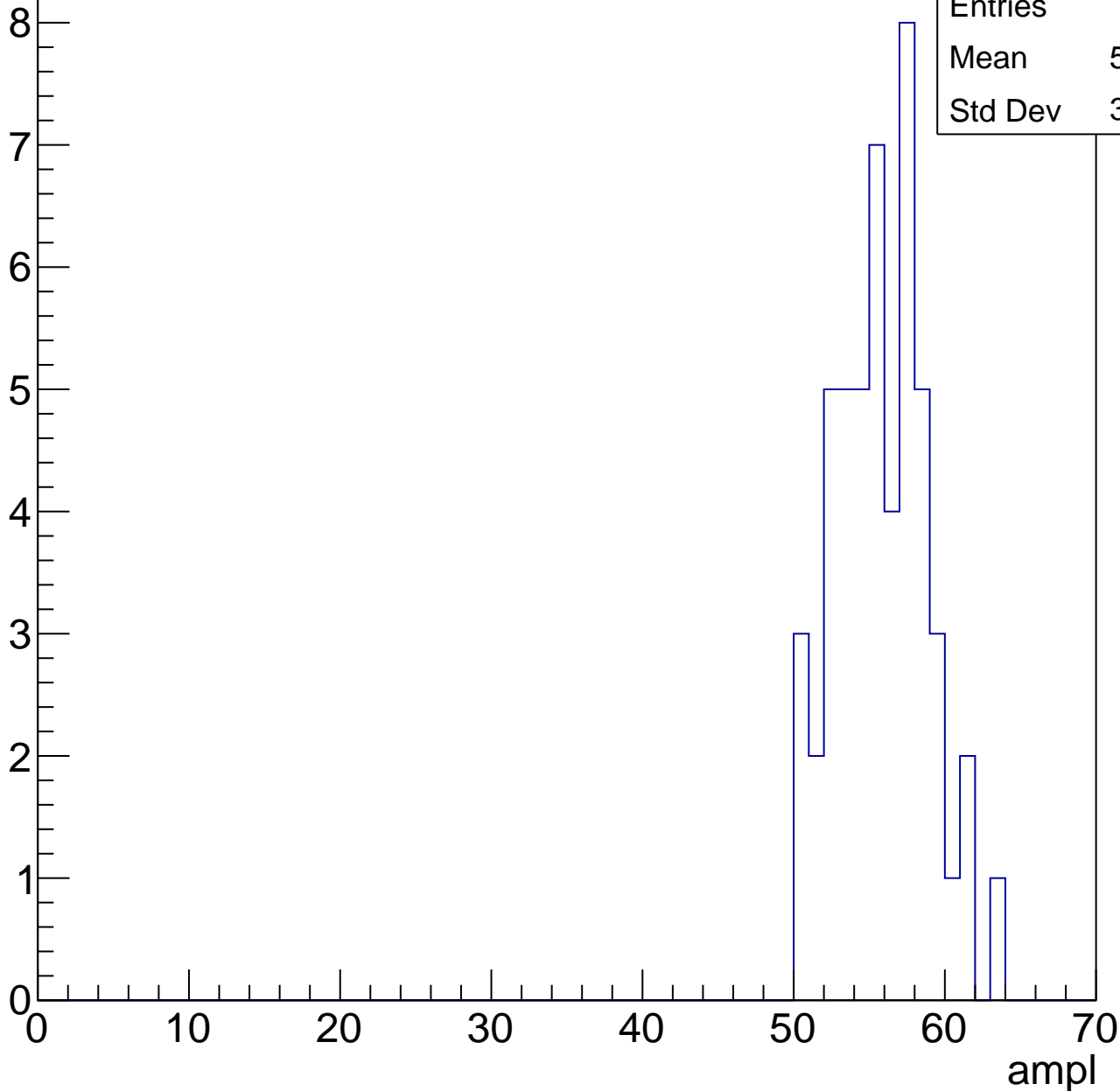


# B1L103S, U2-ch17, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	55.37
Std Dev	3.003

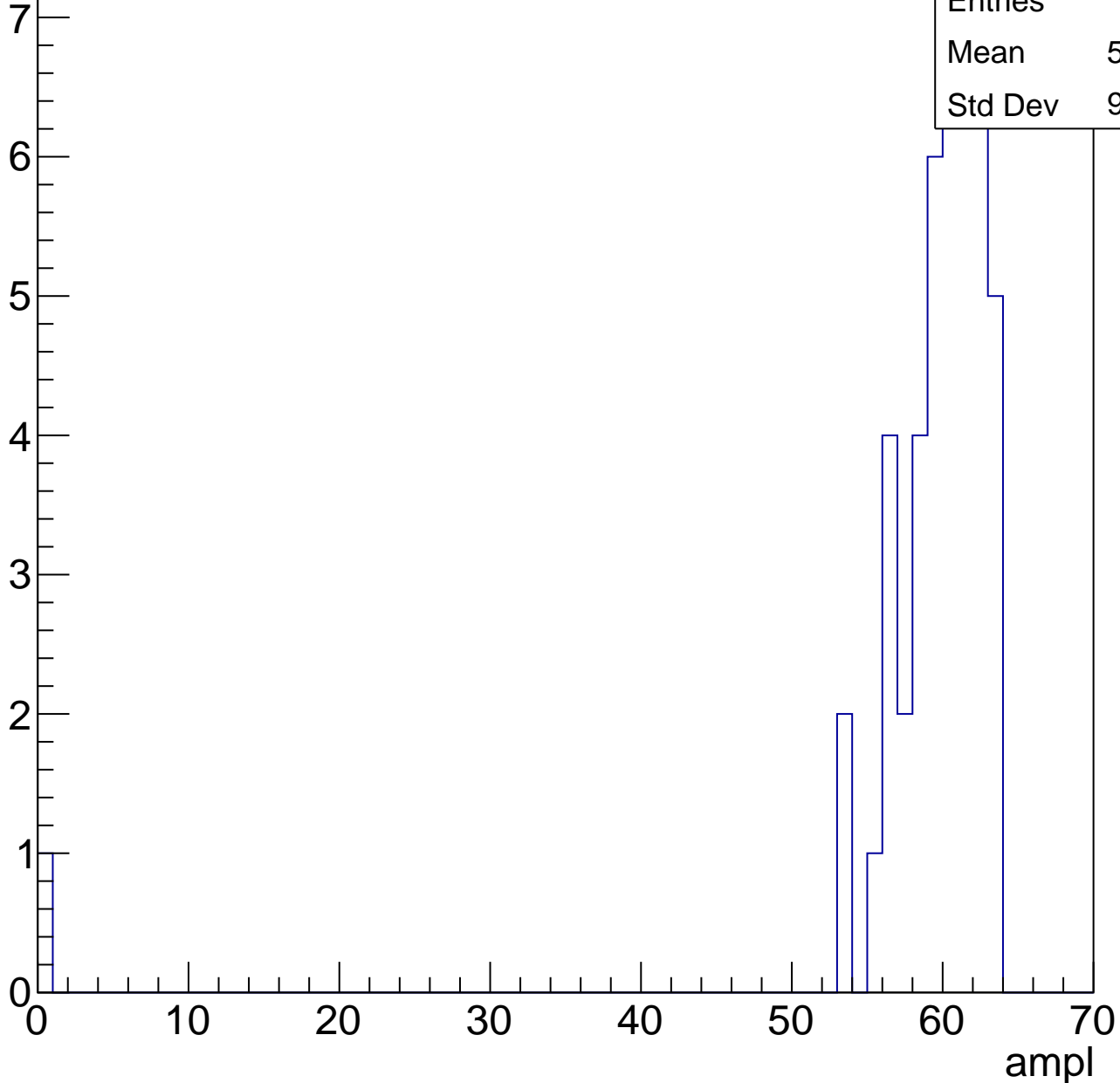


# B1L103S, U2-ch17, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

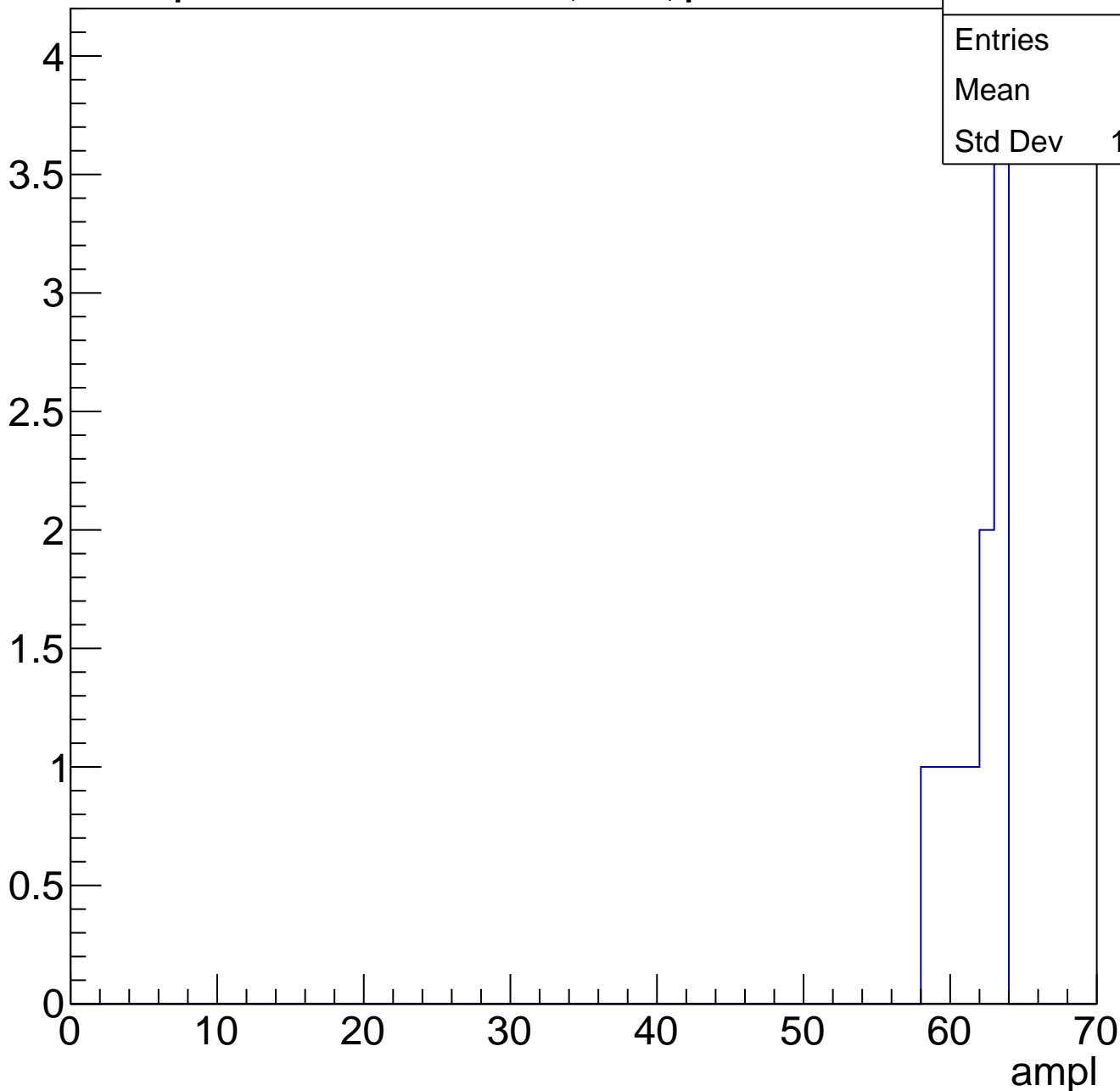
Entries	46
Mean	58.28
Std Dev	9.055



# B1L103S, U2-ch17, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	10
Mean	61.4
Std Dev	1.744



# B1L103S, U2-ch17, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch18, adc0

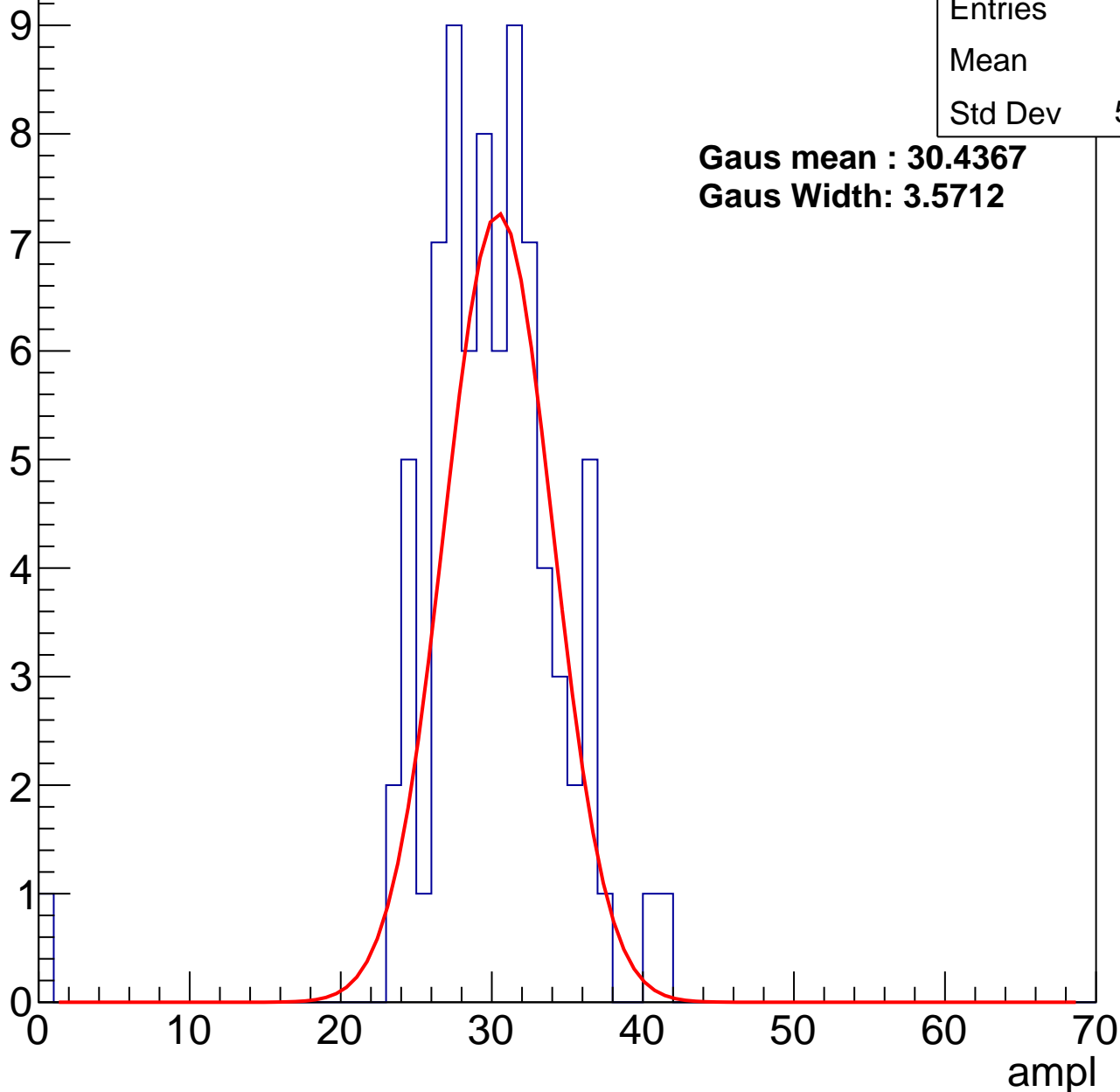
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	29.5
Std Dev	5.101

**Gaus mean : 30.4367**

**Gaus Width: 3.5712**



# B1L103S, U2-ch18, adc1

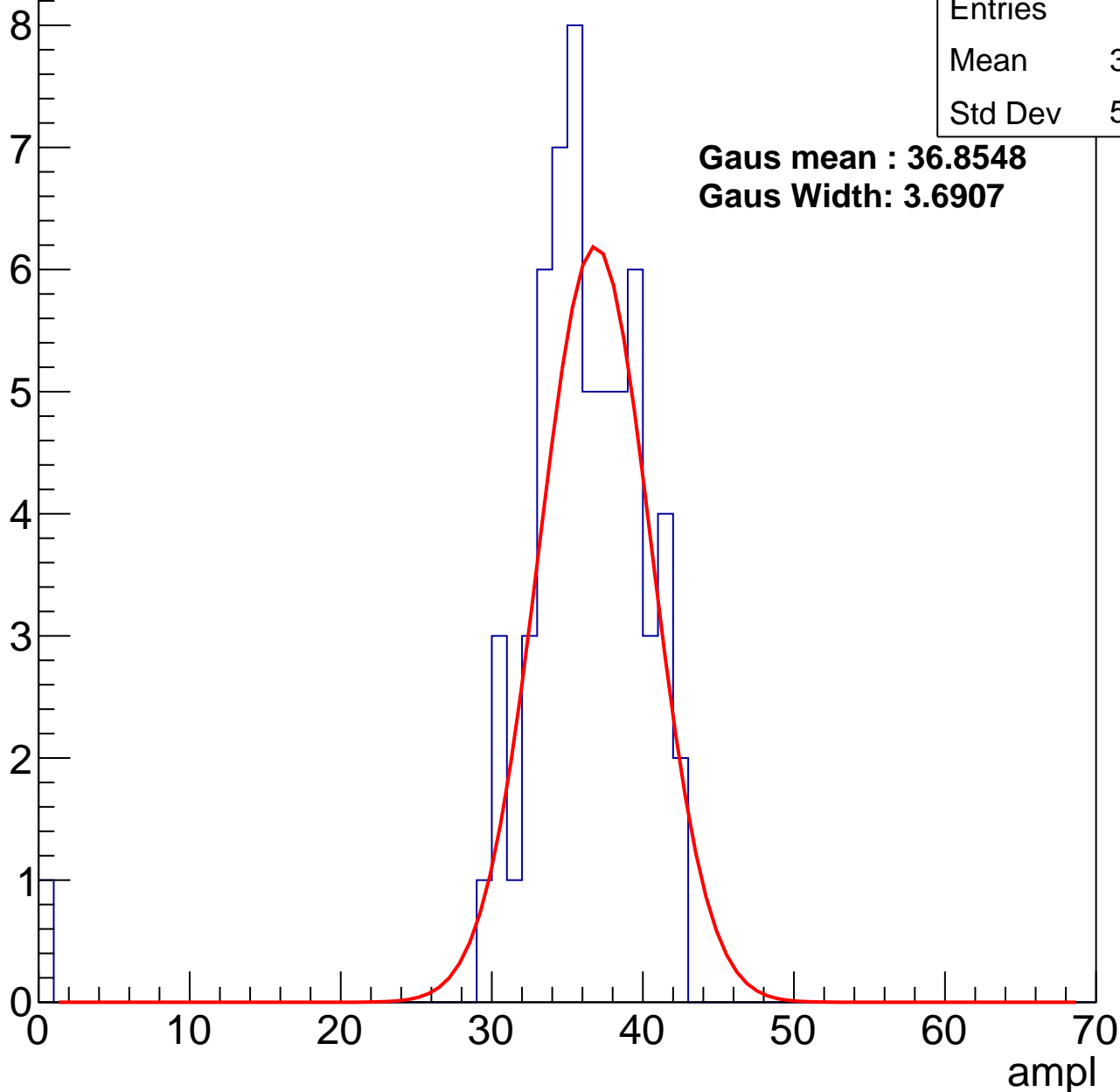
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	35.32
Std Dev	5.608

**Gaus mean : 36.8548**

**Gaus Width: 3.6907**



# B1L103S, U2-ch18, adc2

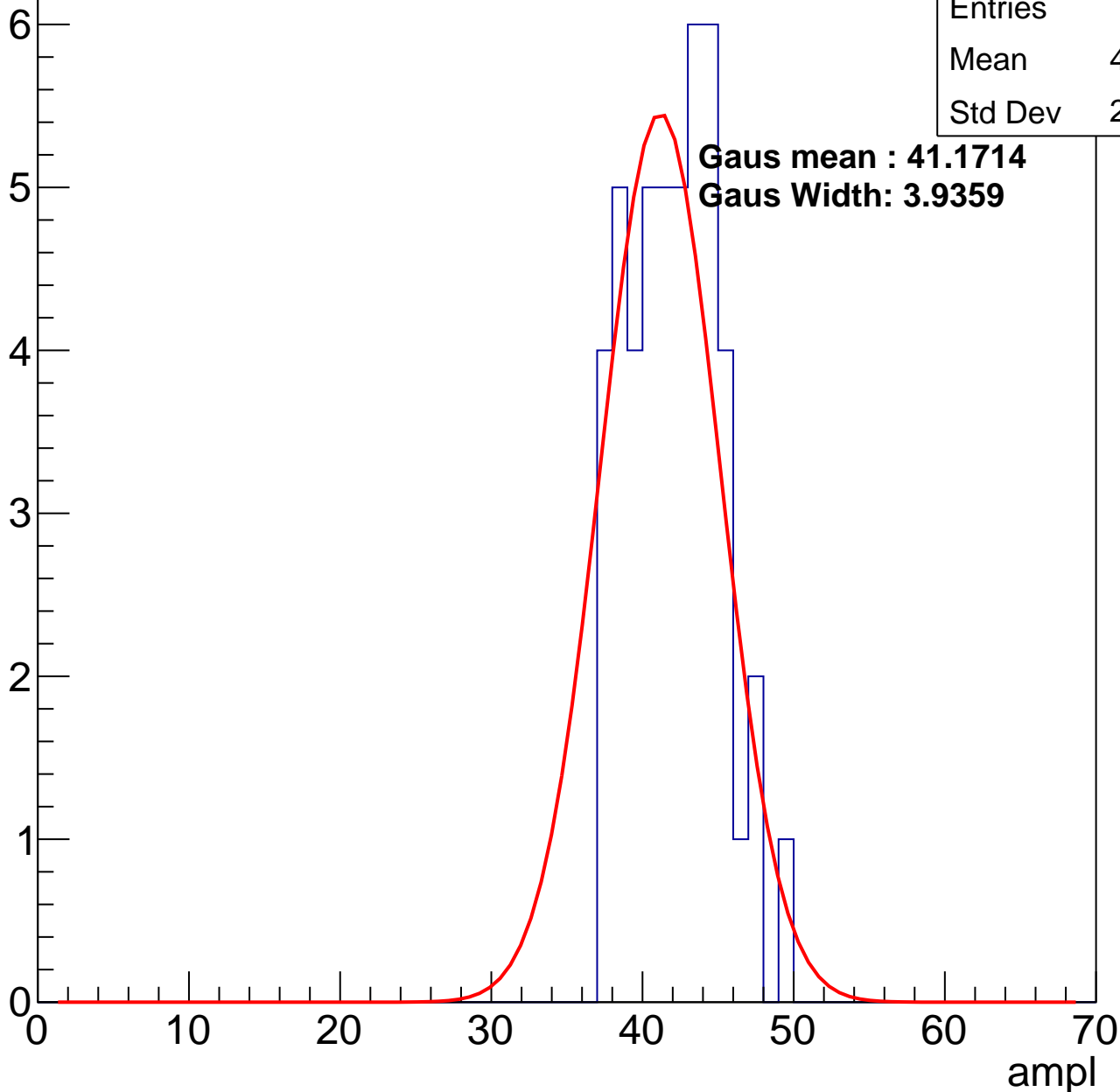
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	48
Mean	41.67
Std Dev	2.946

**Gaus mean : 41.1714**

**Gaus Width: 3.9359**

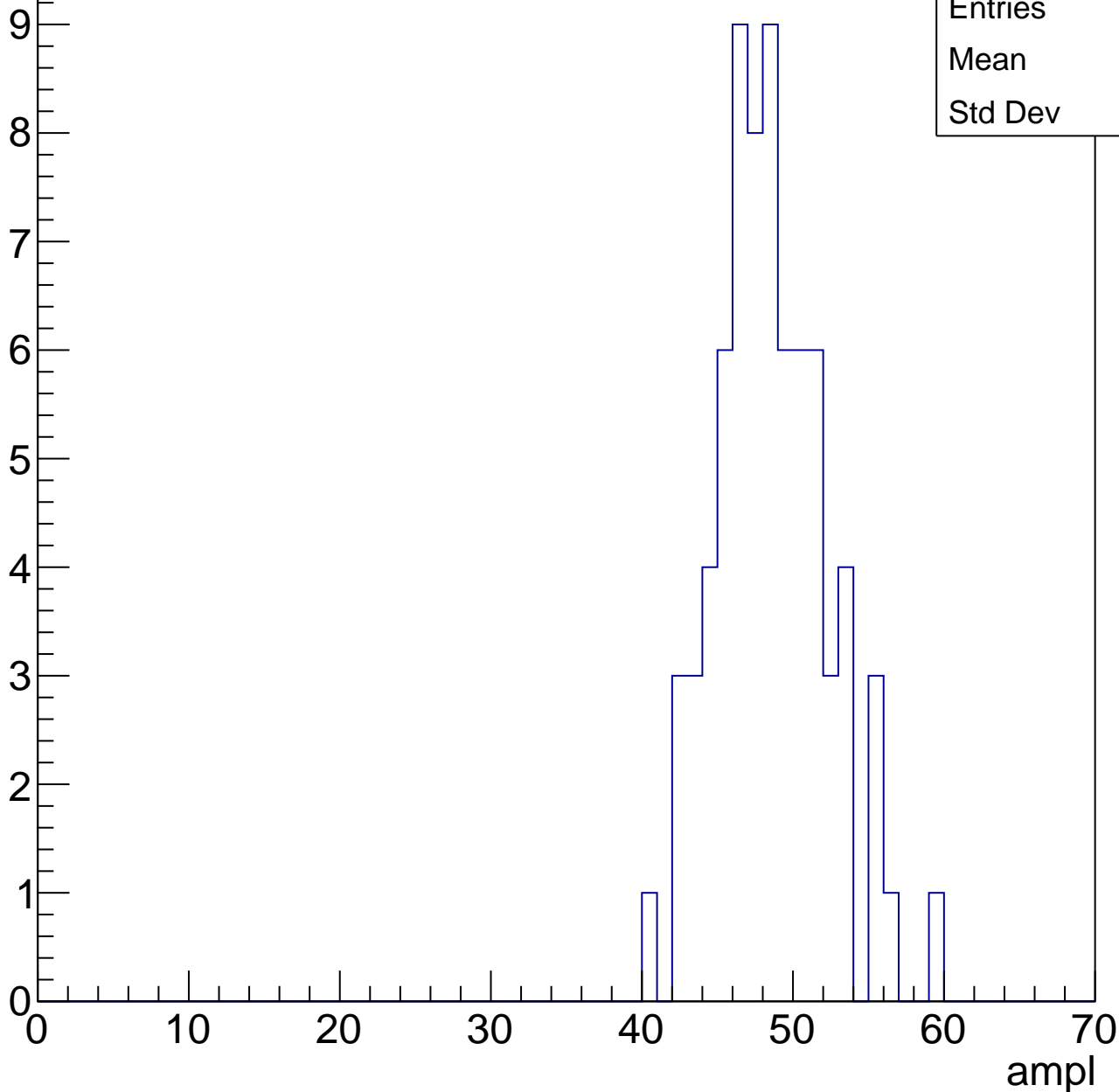


# B1L103S, U2-ch18, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	48.1
Std Dev	3.65

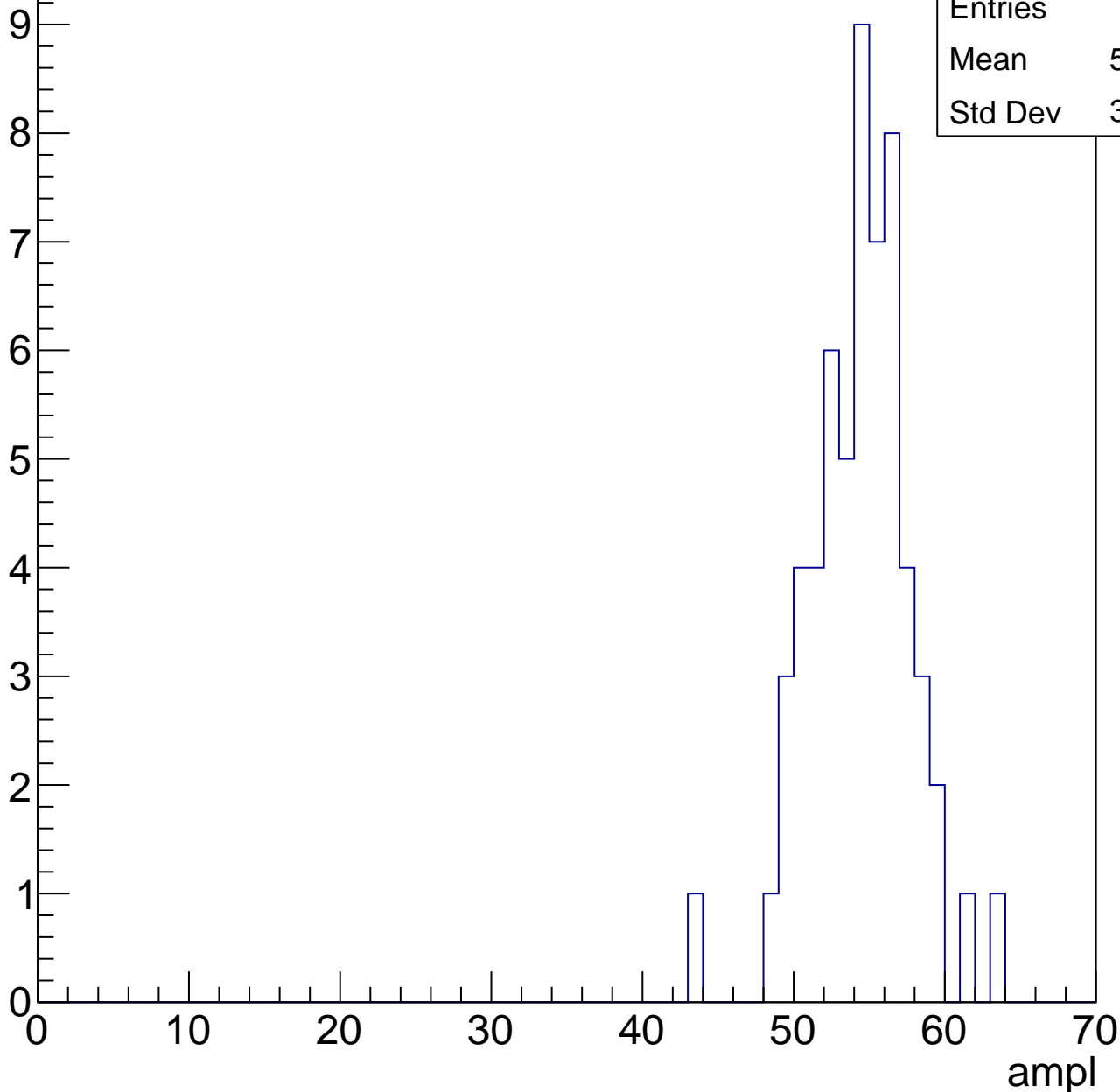


# B1L103S, U2-ch18, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	53.93
Std Dev	3.354

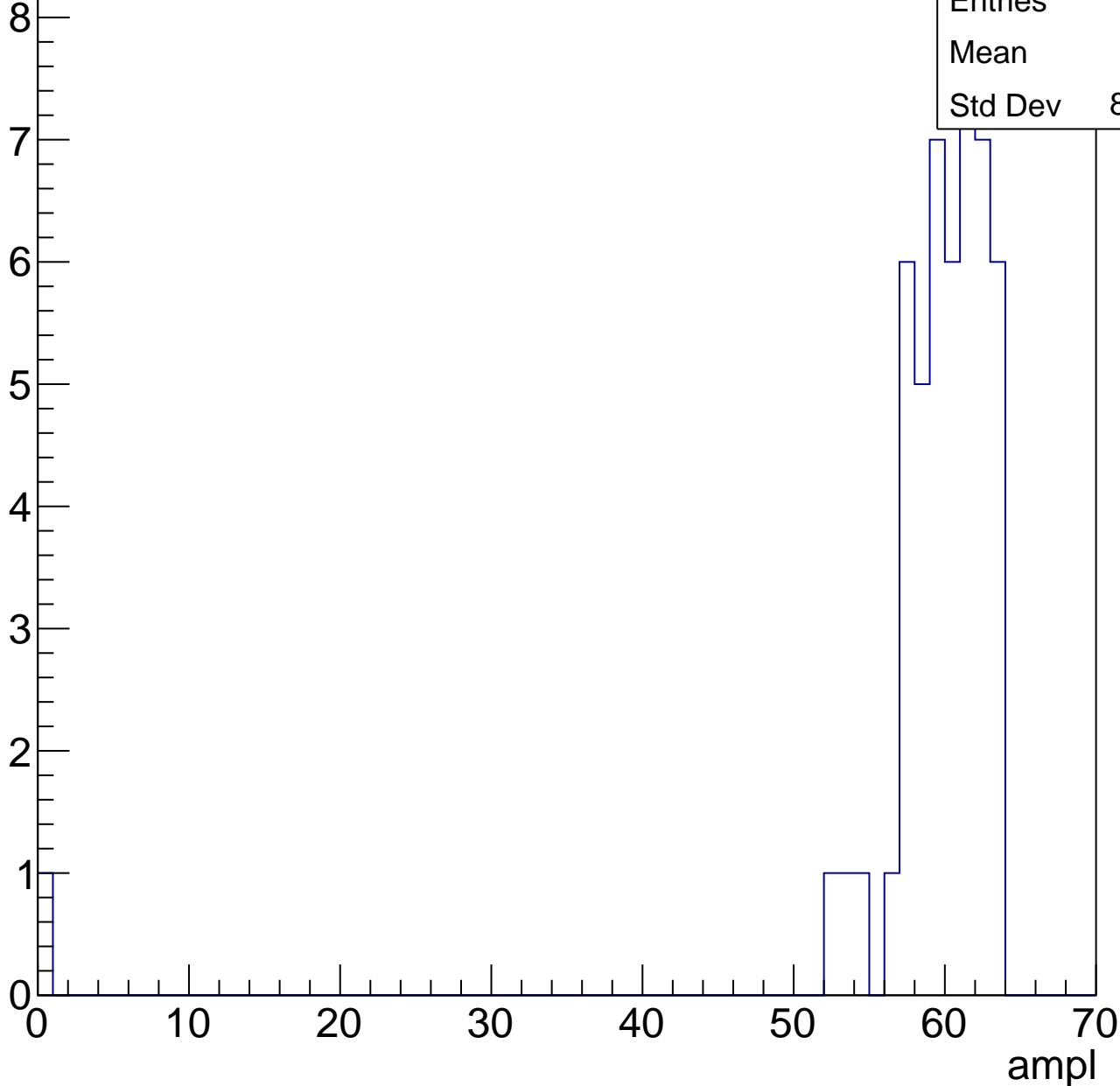


# B1L103S, U2-ch18, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

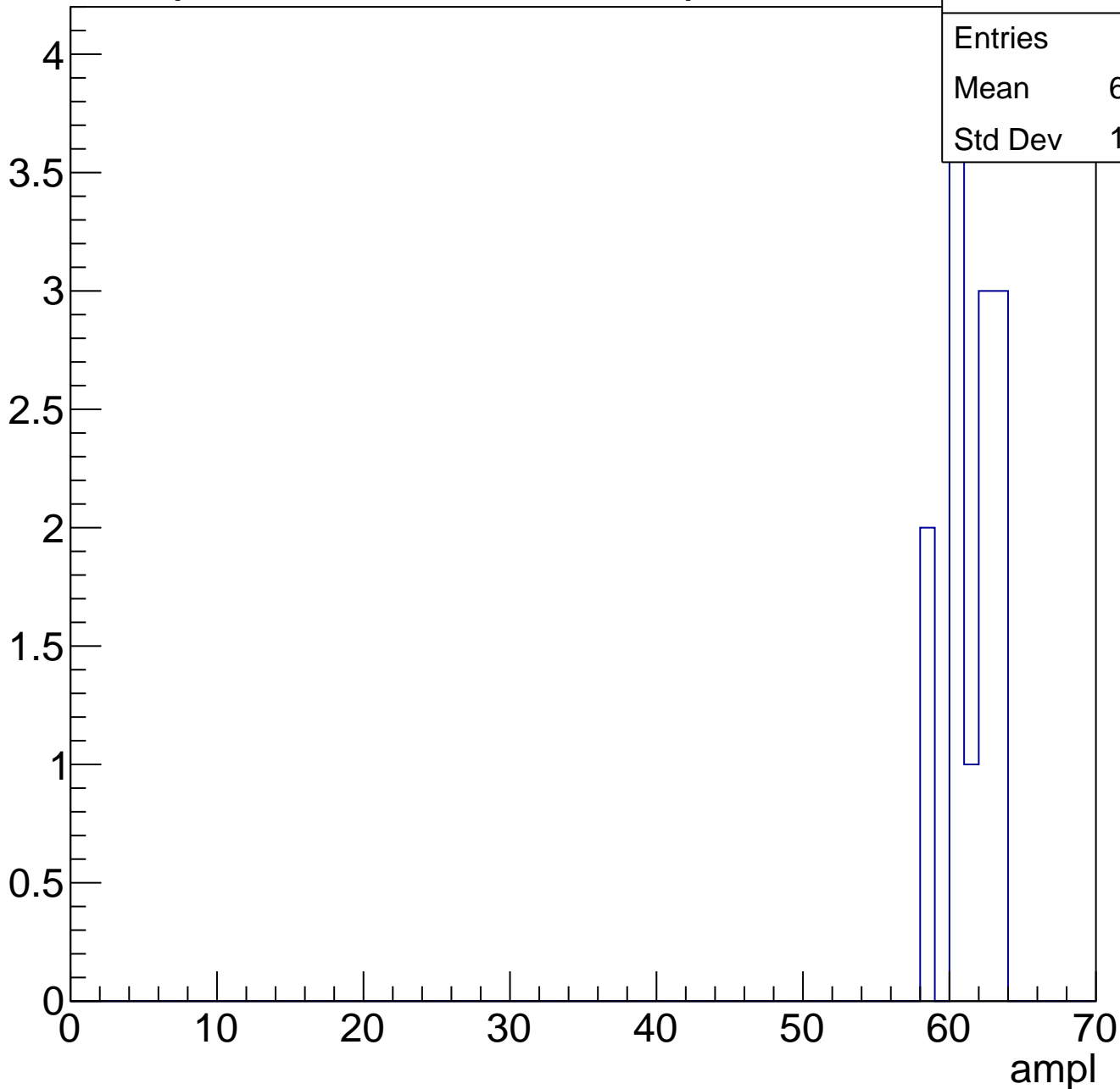
Entries	50
Mean	58.4
Std Dev	8.727



# B1L103S, U2-ch18, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	13
Mean	60.92
Std Dev	1.685



# B1L103S, U2-ch18, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	10.5
Std Dev	10.5

# B1L103S, U2-ch19, adc0

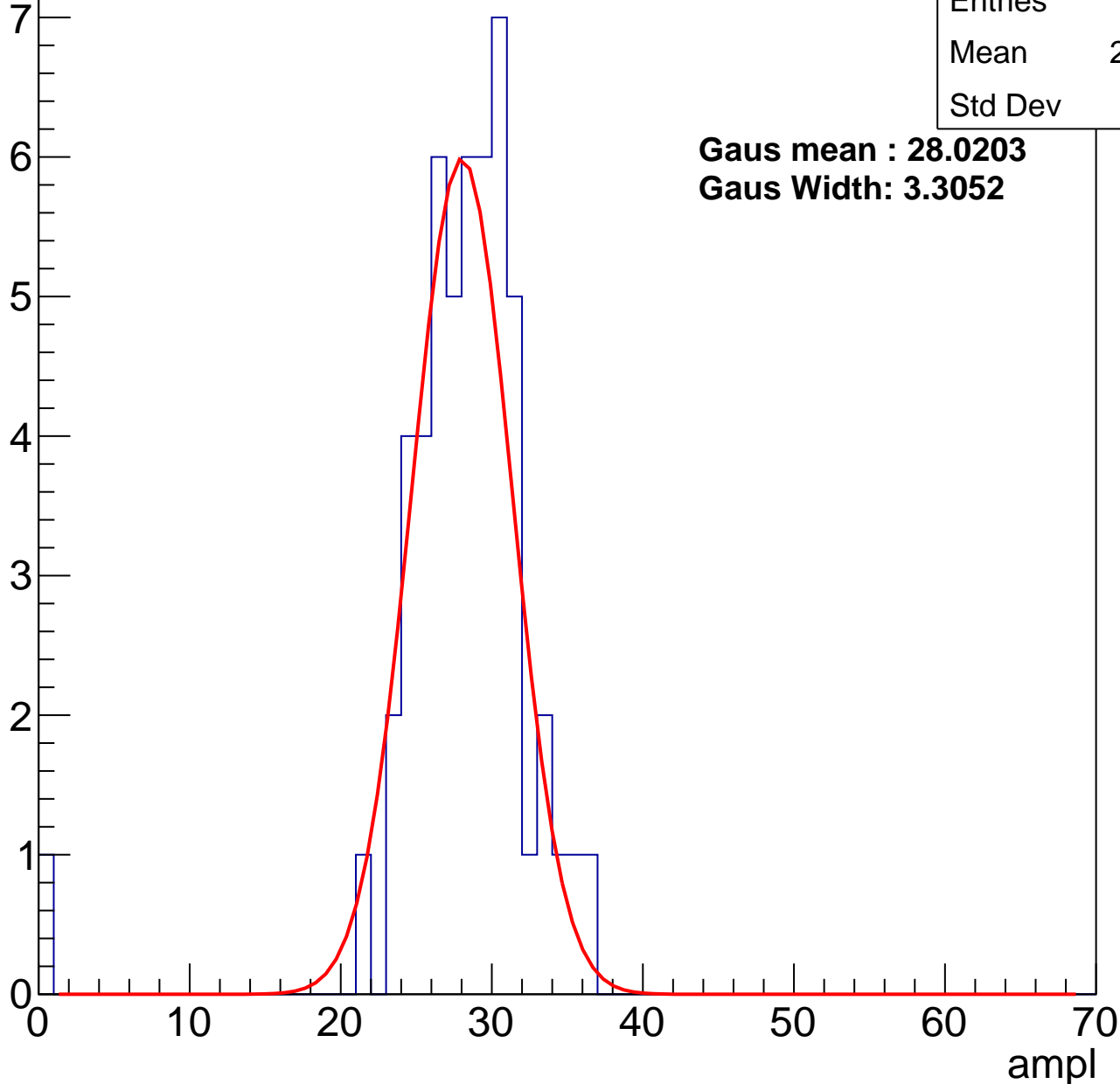
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	27.62
Std Dev	4.95

**Gaus mean : 28.0203**

**Gaus Width: 3.3052**



# B1L103S, U2-ch19, adc1

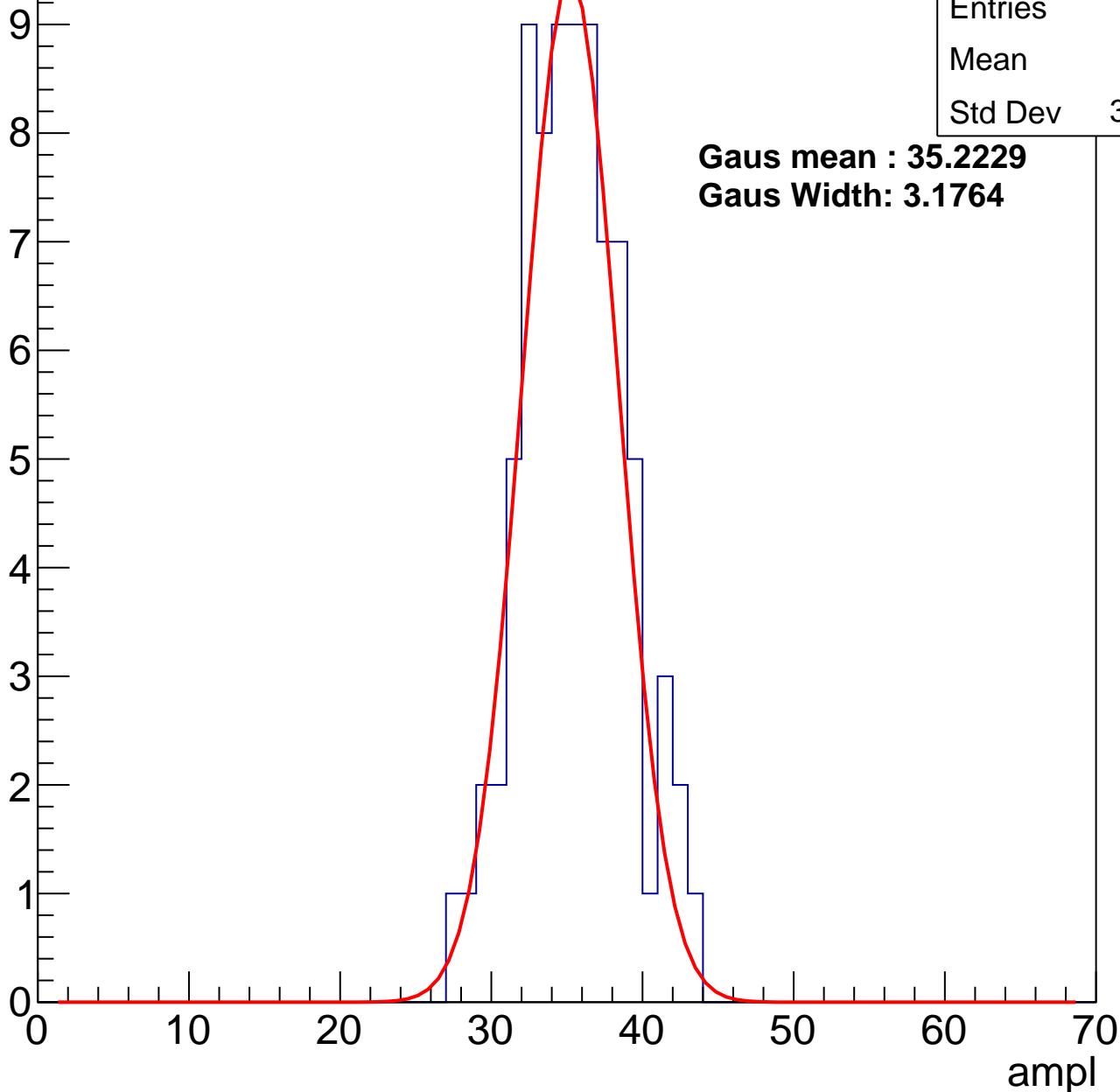
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	81
Mean	35
Std Dev	3.355

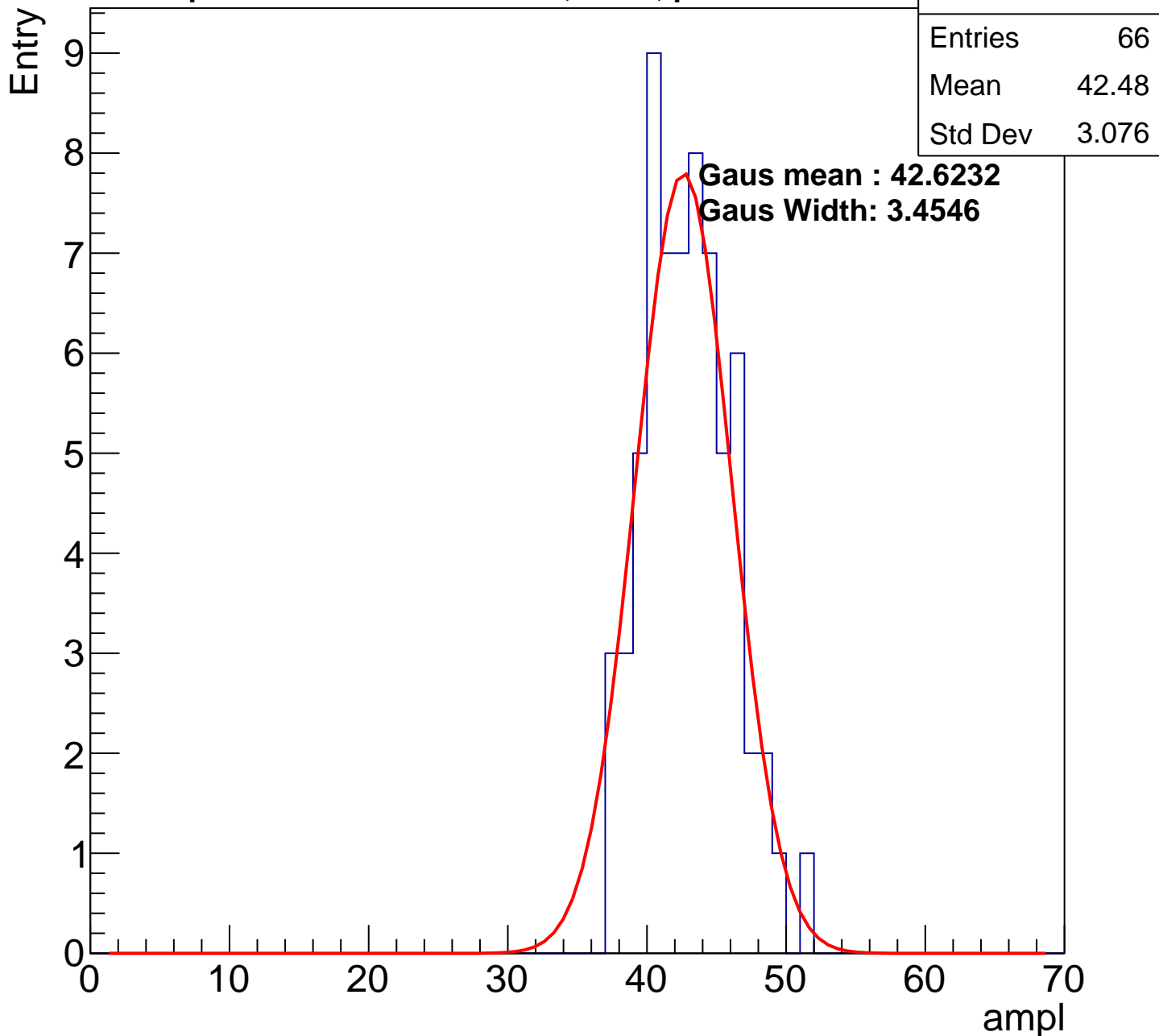
**Gaus mean : 35.2229**

**Gaus Width: 3.1764**



# B1L103S, U2-ch19, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

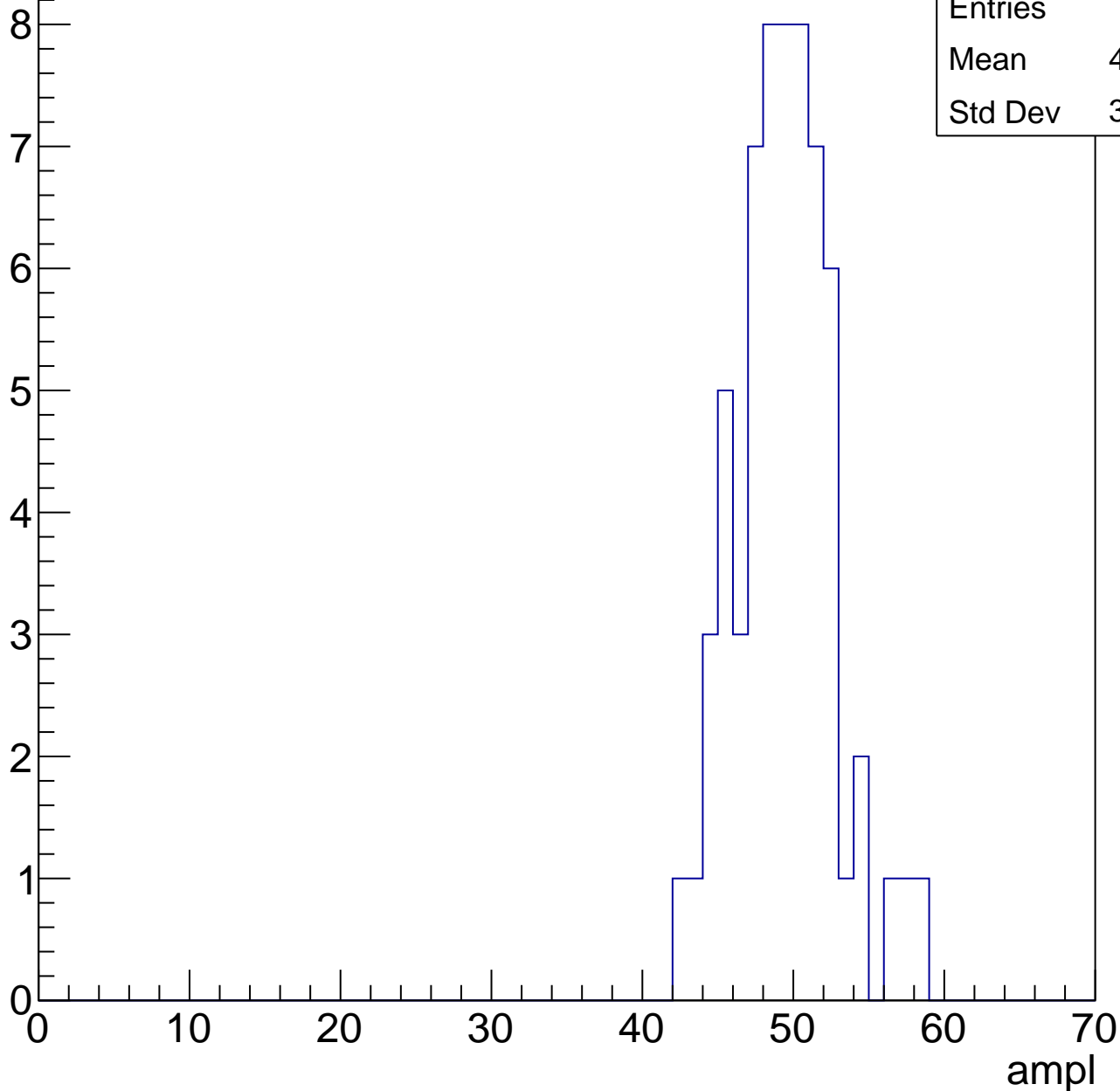


# B1L103S, U2-ch19, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

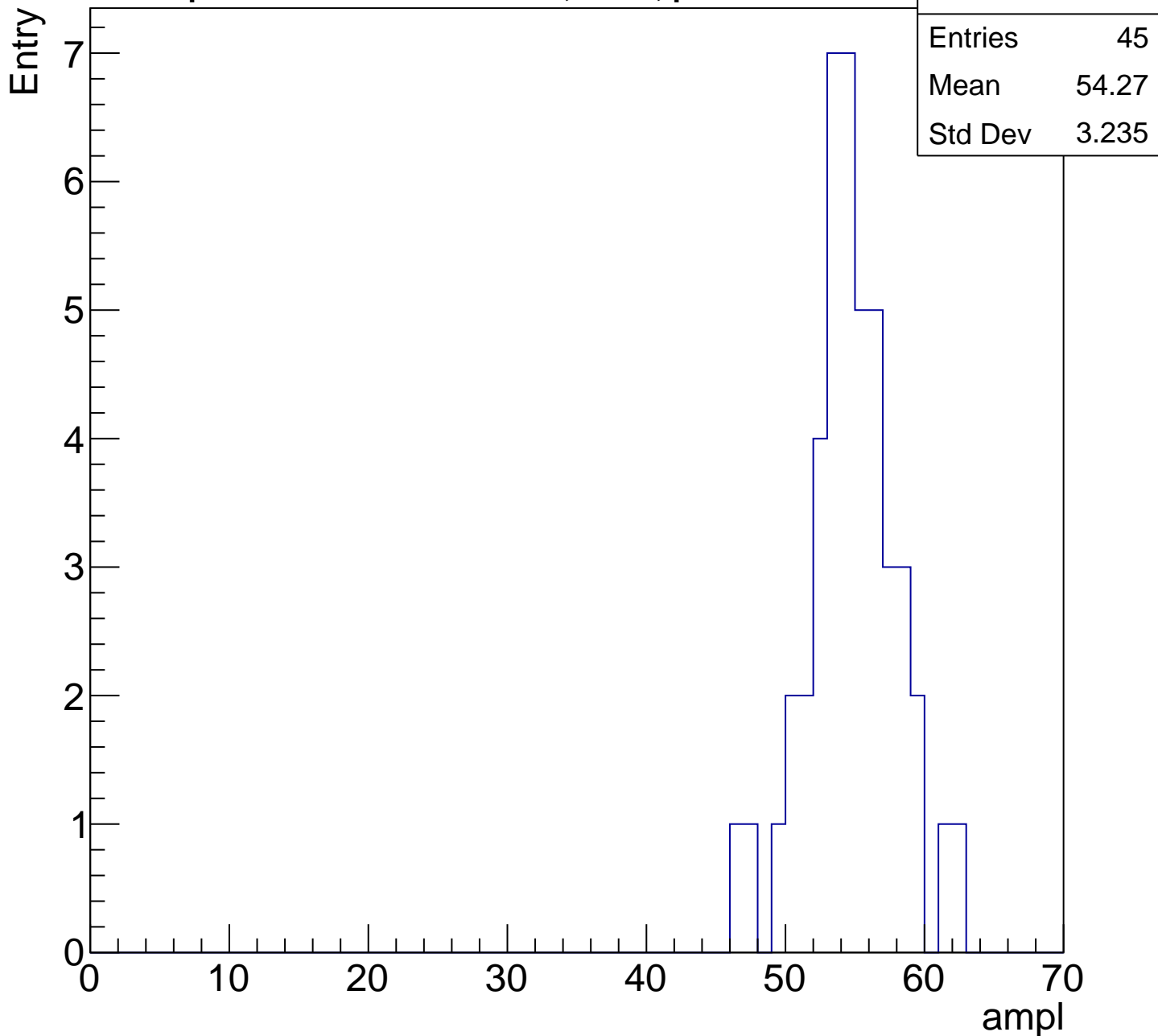
Entry

Entries	63
Mean	48.98
Std Dev	3.219



# B1L103S, U2-ch19, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

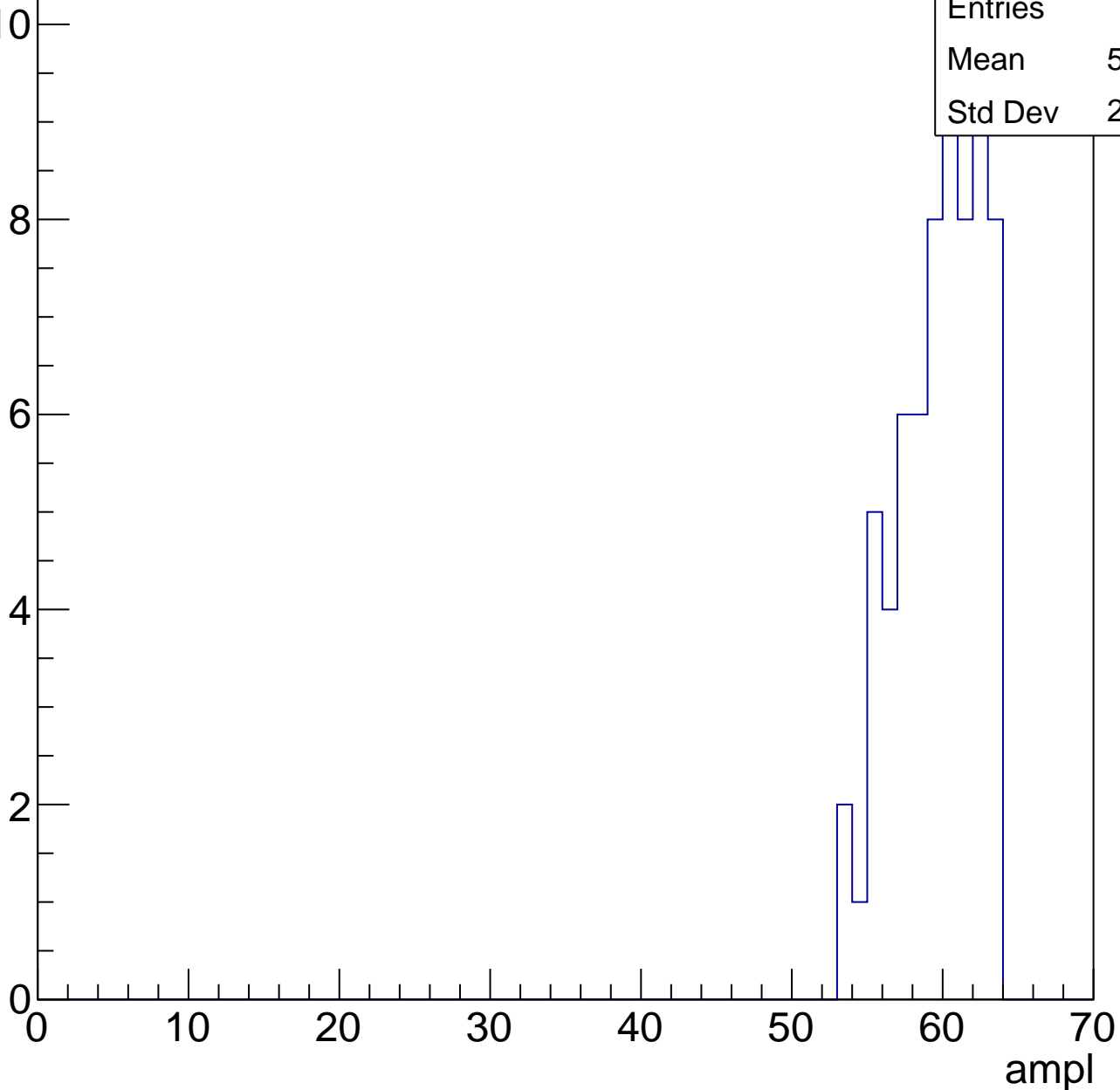


# B1L103S, U2-ch19, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

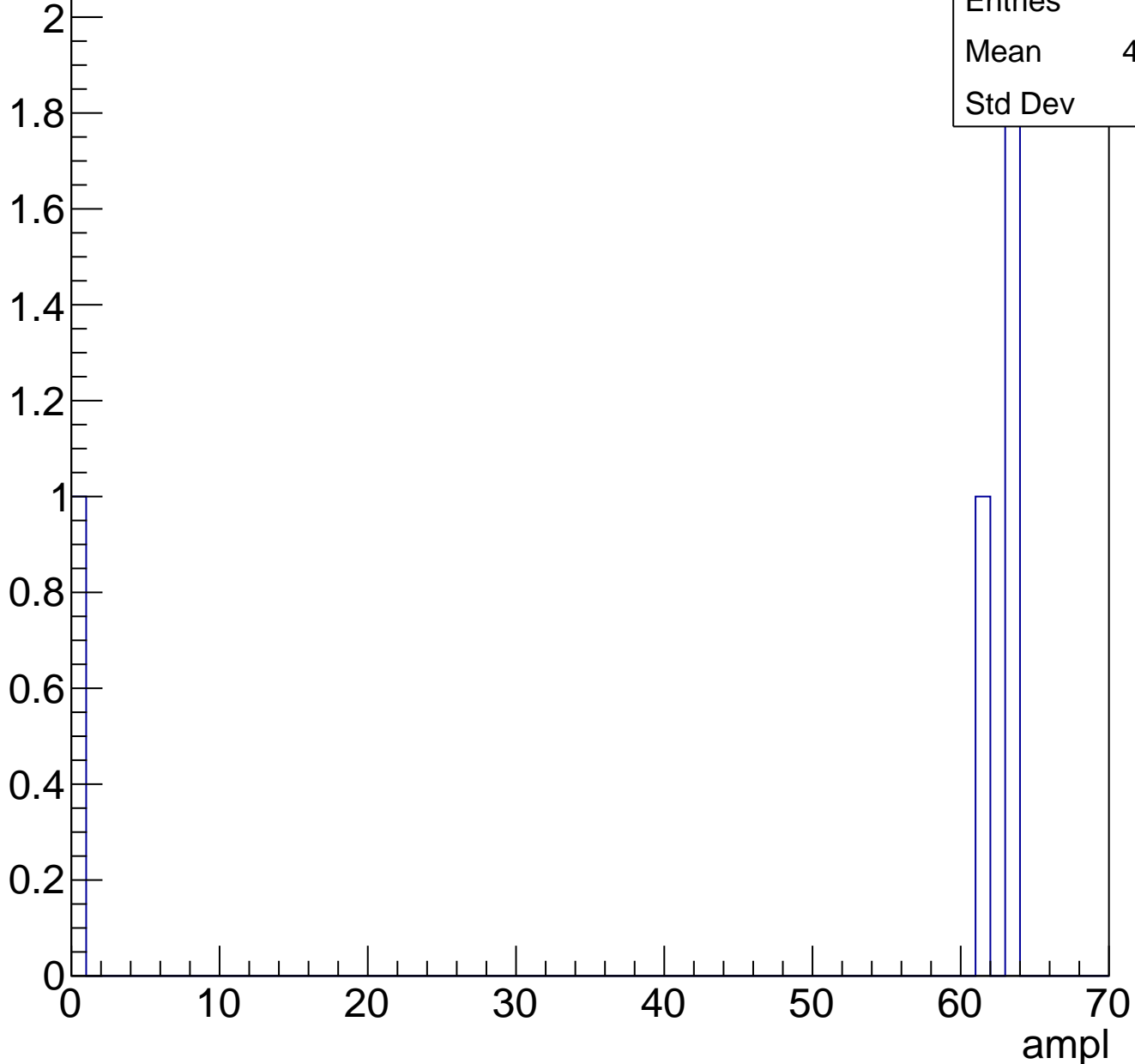
Entries	67
Mean	59.27
Std Dev	2.702



# B1L103S, U2-ch19, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	4
Mean	46.75
Std Dev	27



# B1L103S, U2-ch19, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L103S, U2-ch20, adc0

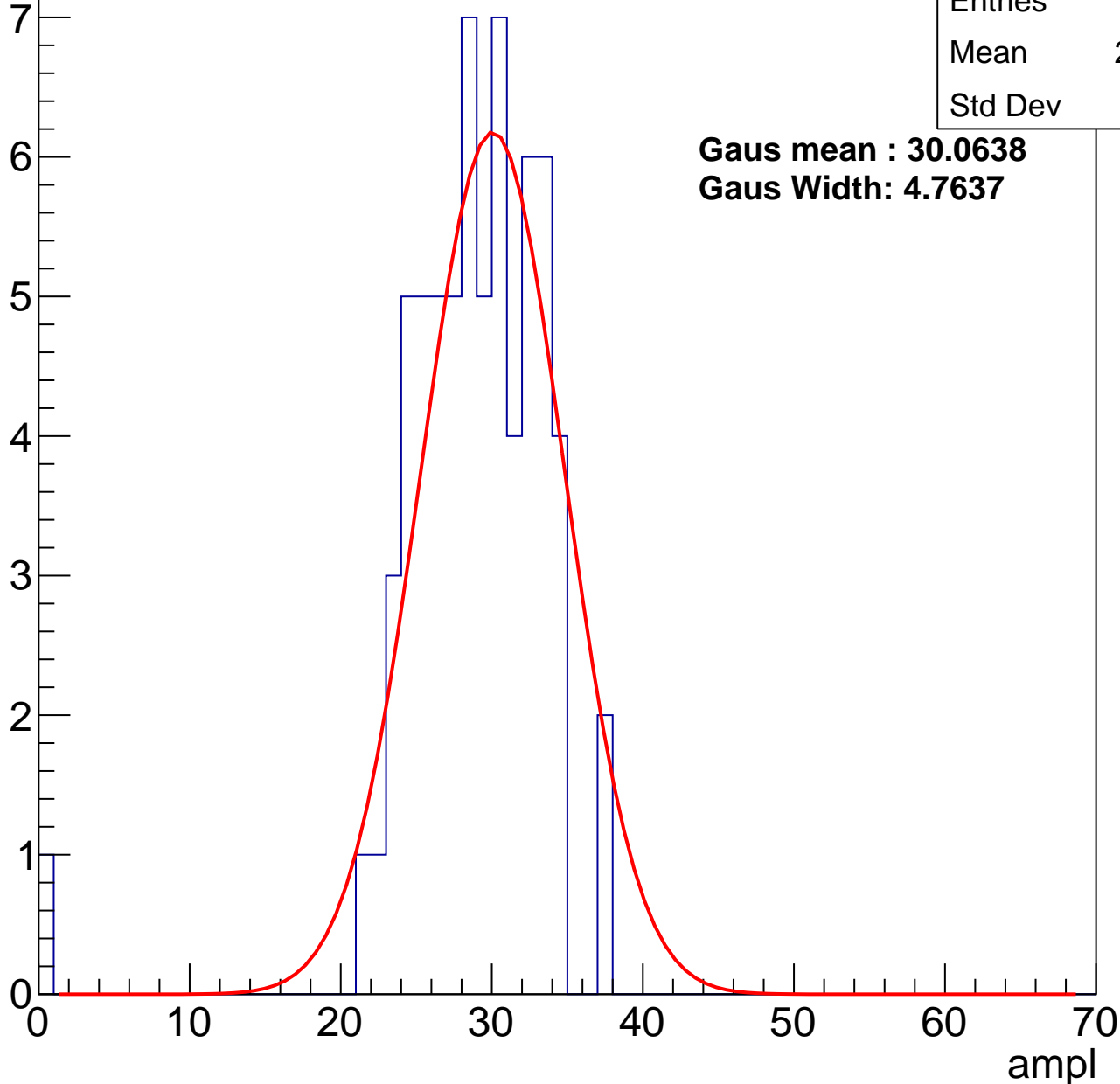
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	28.31
Std Dev	5.05

**Gaus mean : 30.0638**

**Gaus Width: 4.7637**



# B1L103S, U2-ch20, adc1

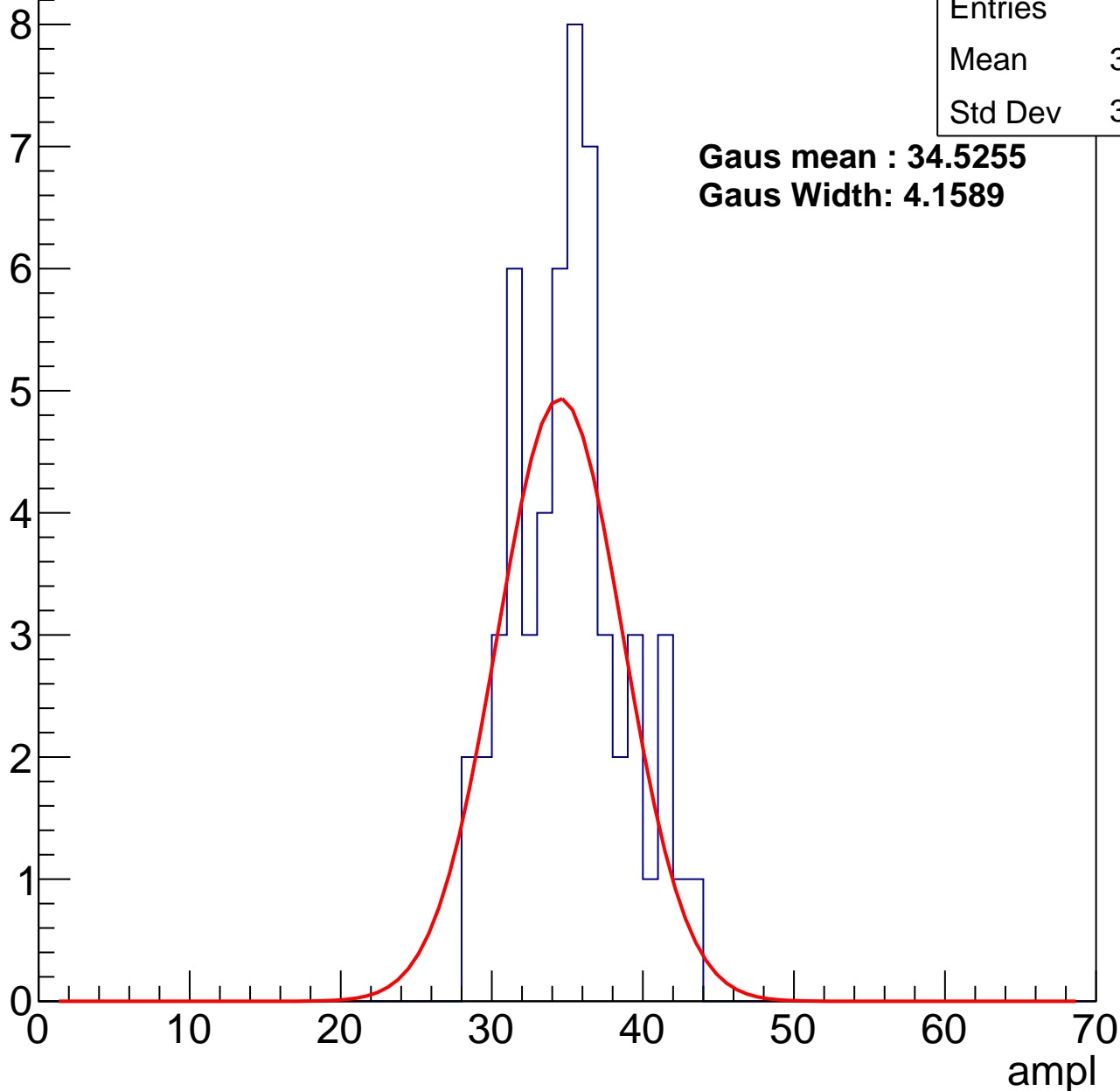
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	34.65
Std Dev	3.604

**Gaus mean : 34.5255**

**Gaus Width: 4.1589**



# B1L103S, U2-ch20, adc2

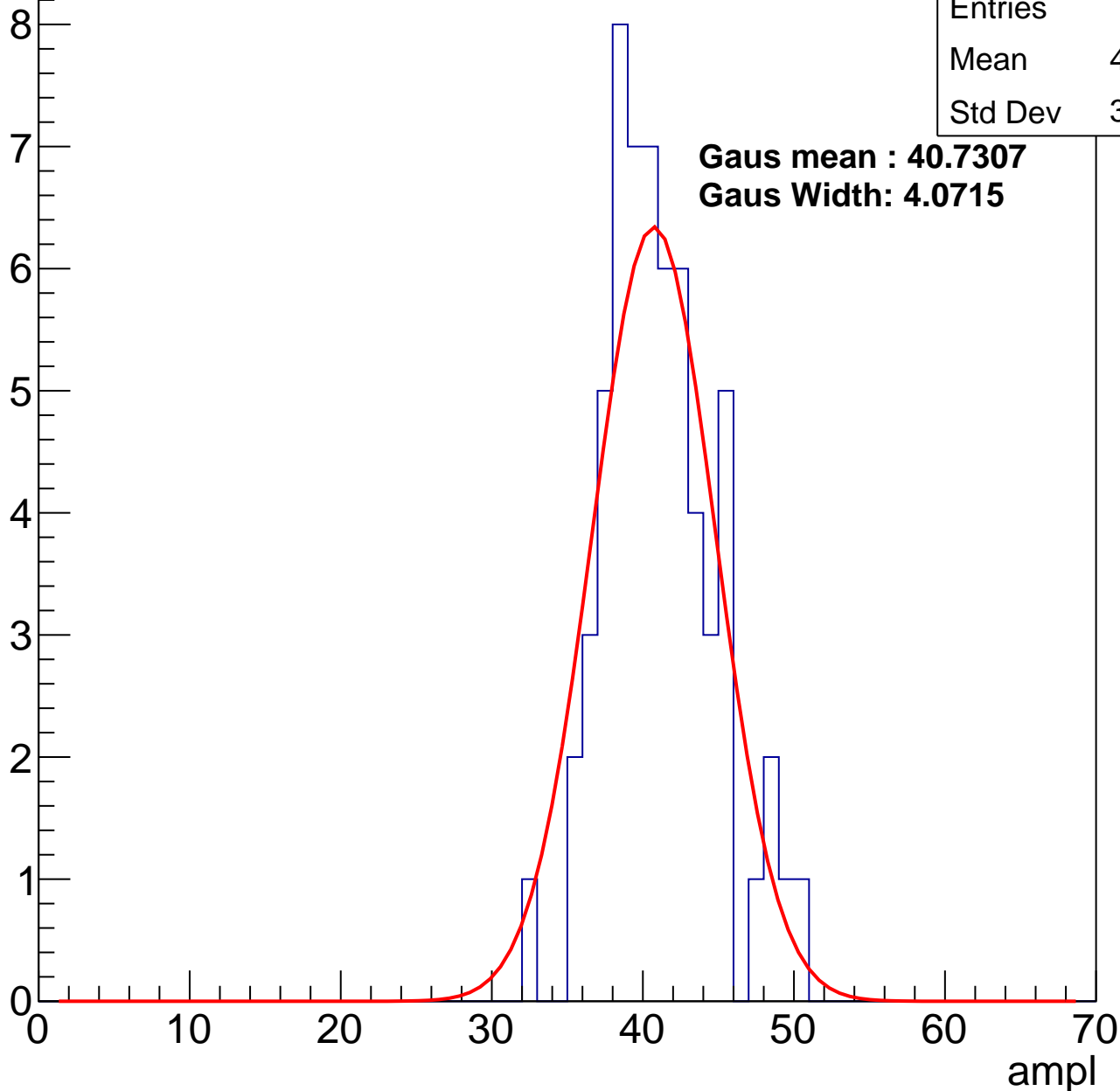
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	40.66
Std Dev	3.628

**Gaus mean : 40.7307**

**Gaus Width: 4.0715**

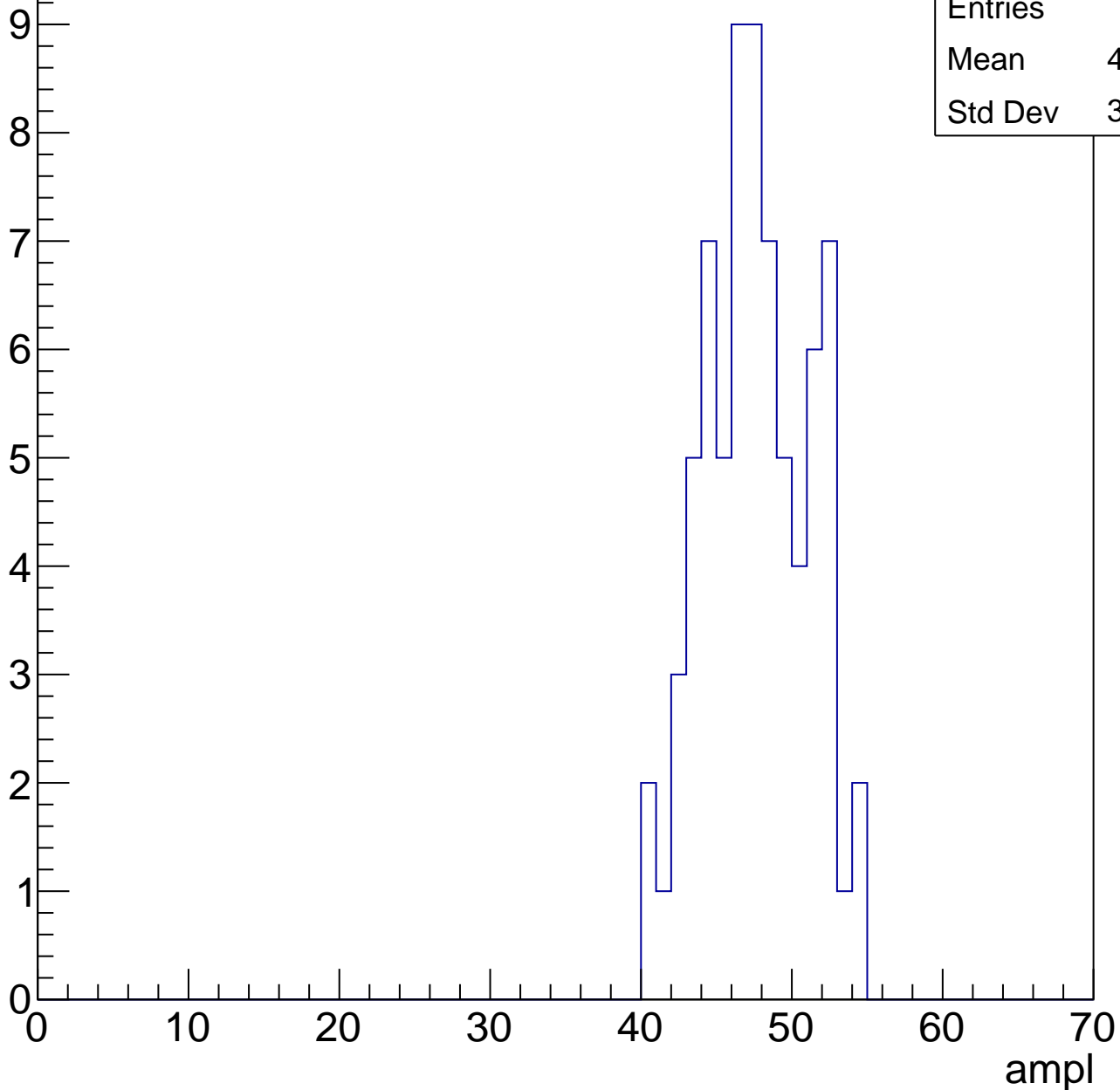


# B1L103S, U2-ch20, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	47.18
Std Dev	3.406

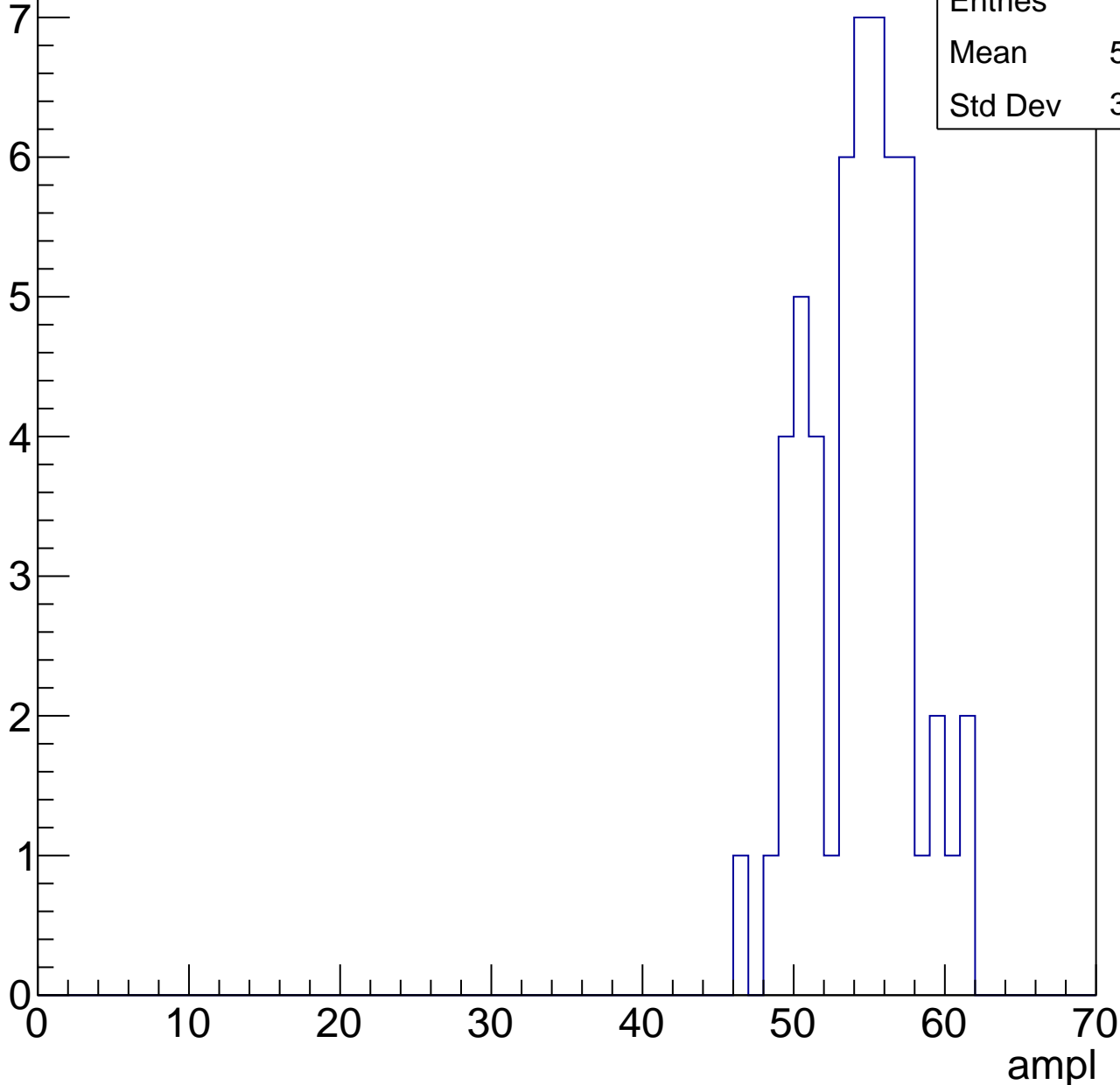


# B1L103S, U2-ch20, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	53.94
Std Dev	3.363

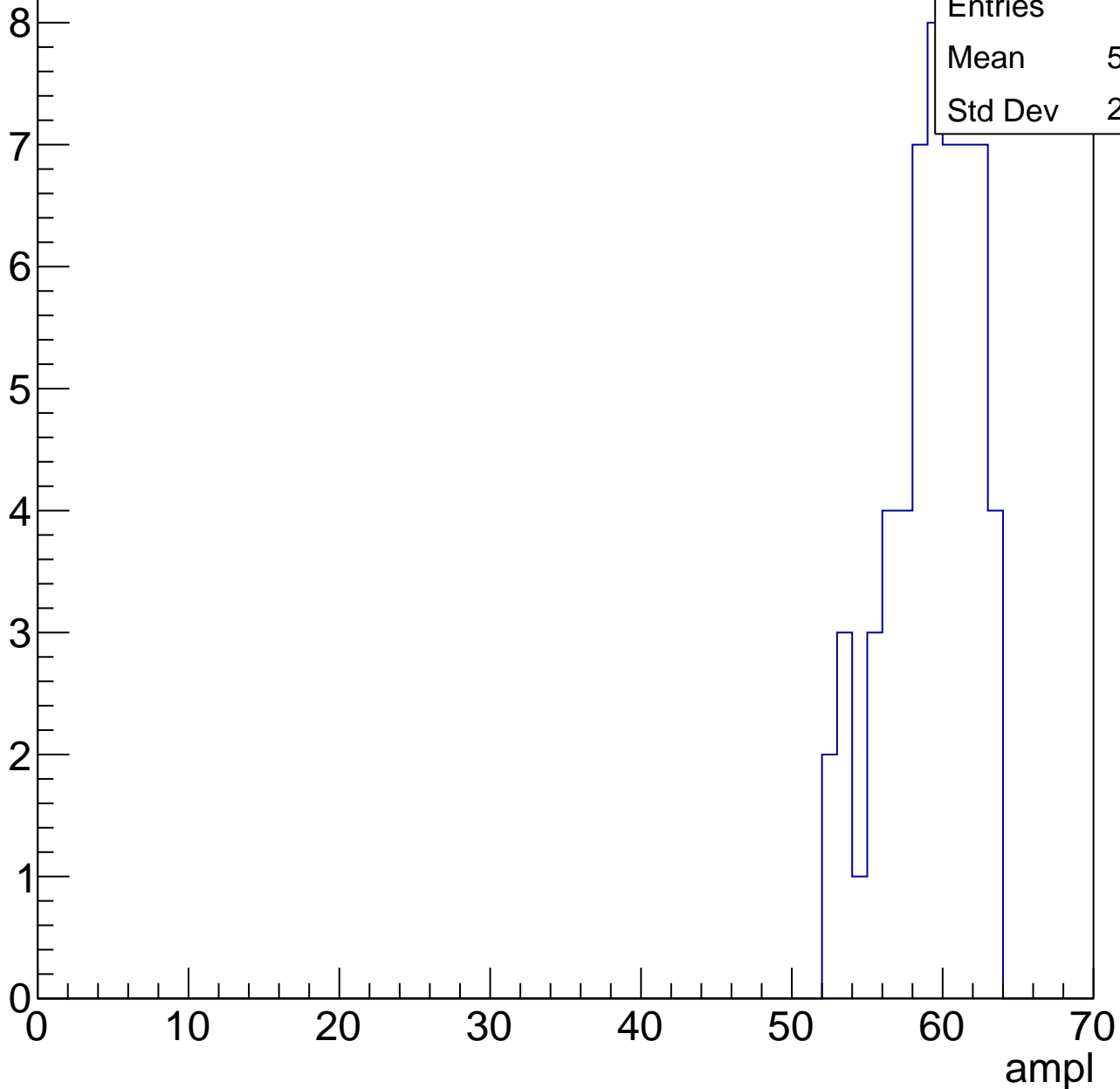


# B1L103S, U2-ch20, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	58.68
Std Dev	2.945

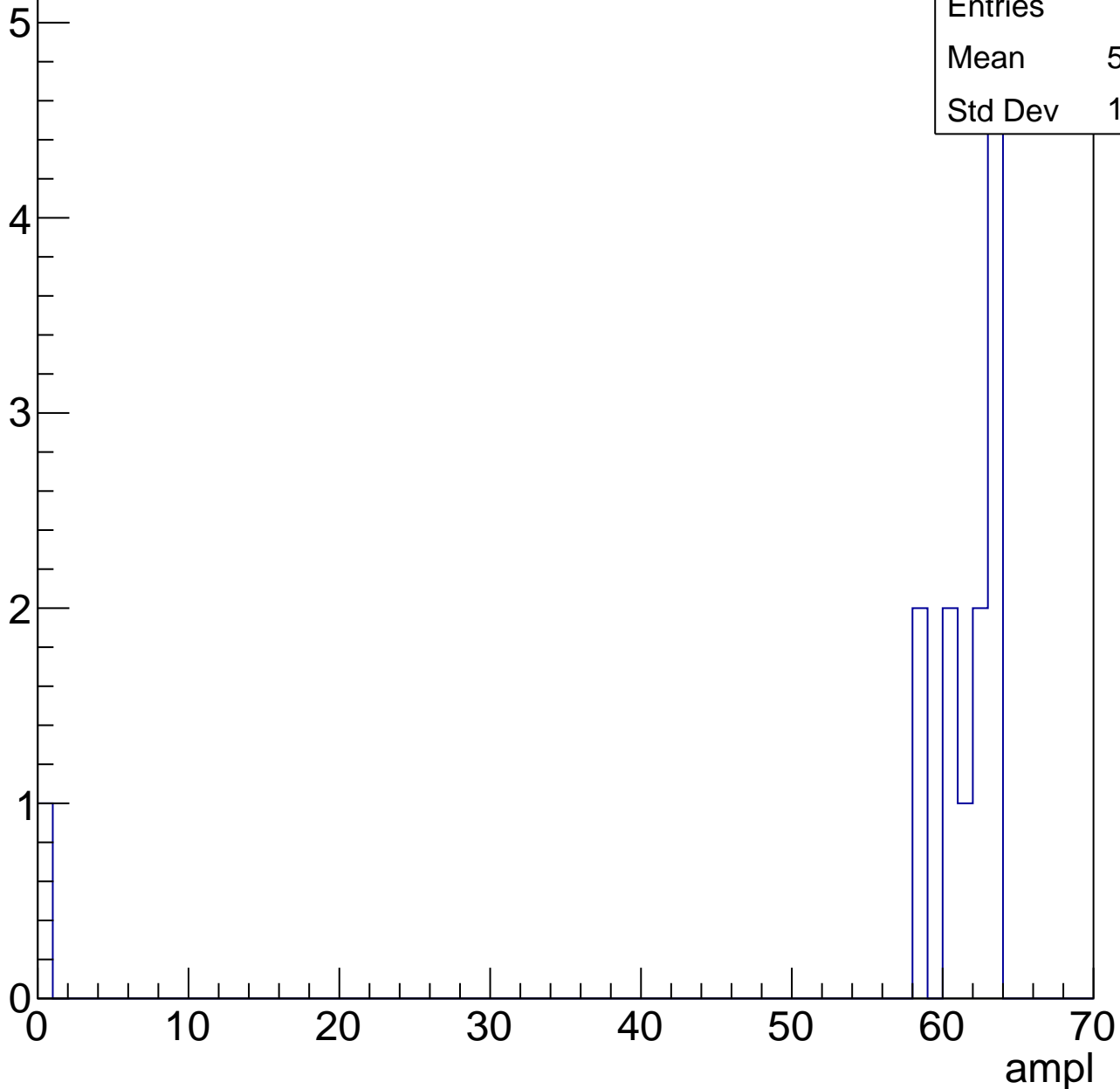


# B1L103S, U2-ch20, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	13
Mean	56.62
Std Dev	16.44

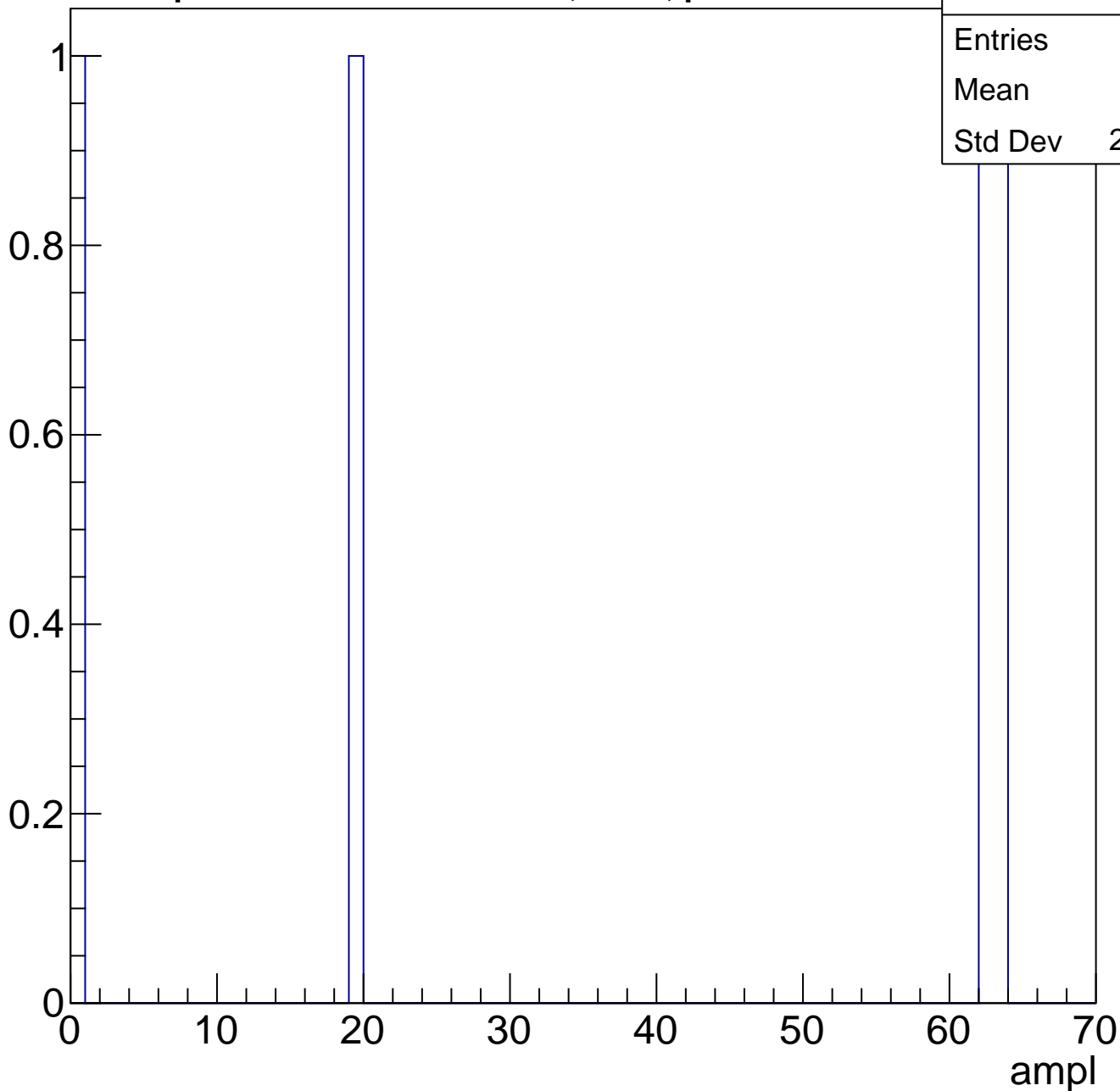




# B1L103S, U2-ch20, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch21, adc0

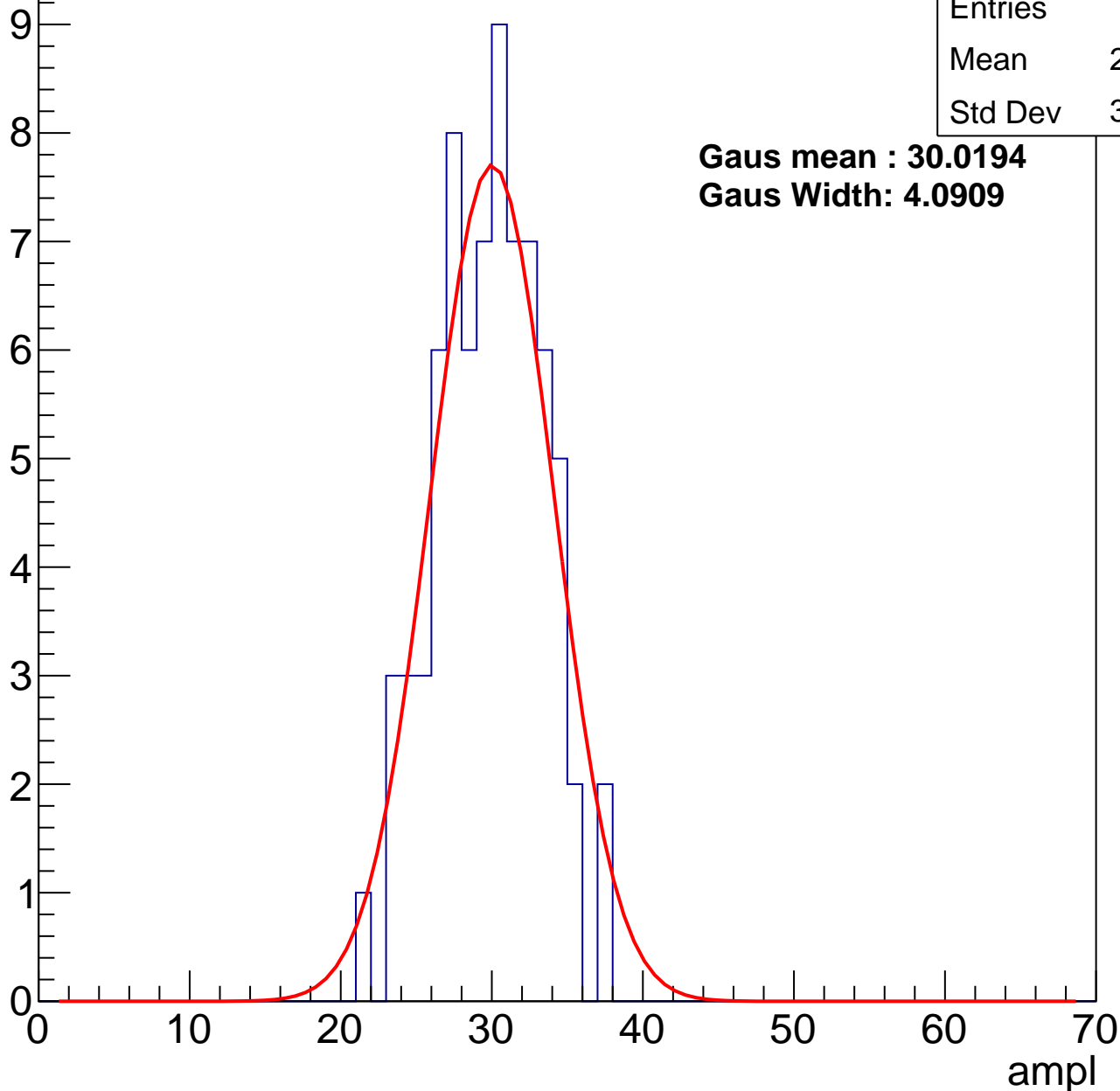
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	29.37
Std Dev	3.459

**Gaus mean : 30.0194**

**Gaus Width: 4.0909**



# B1L103S, U2-ch21, adc1

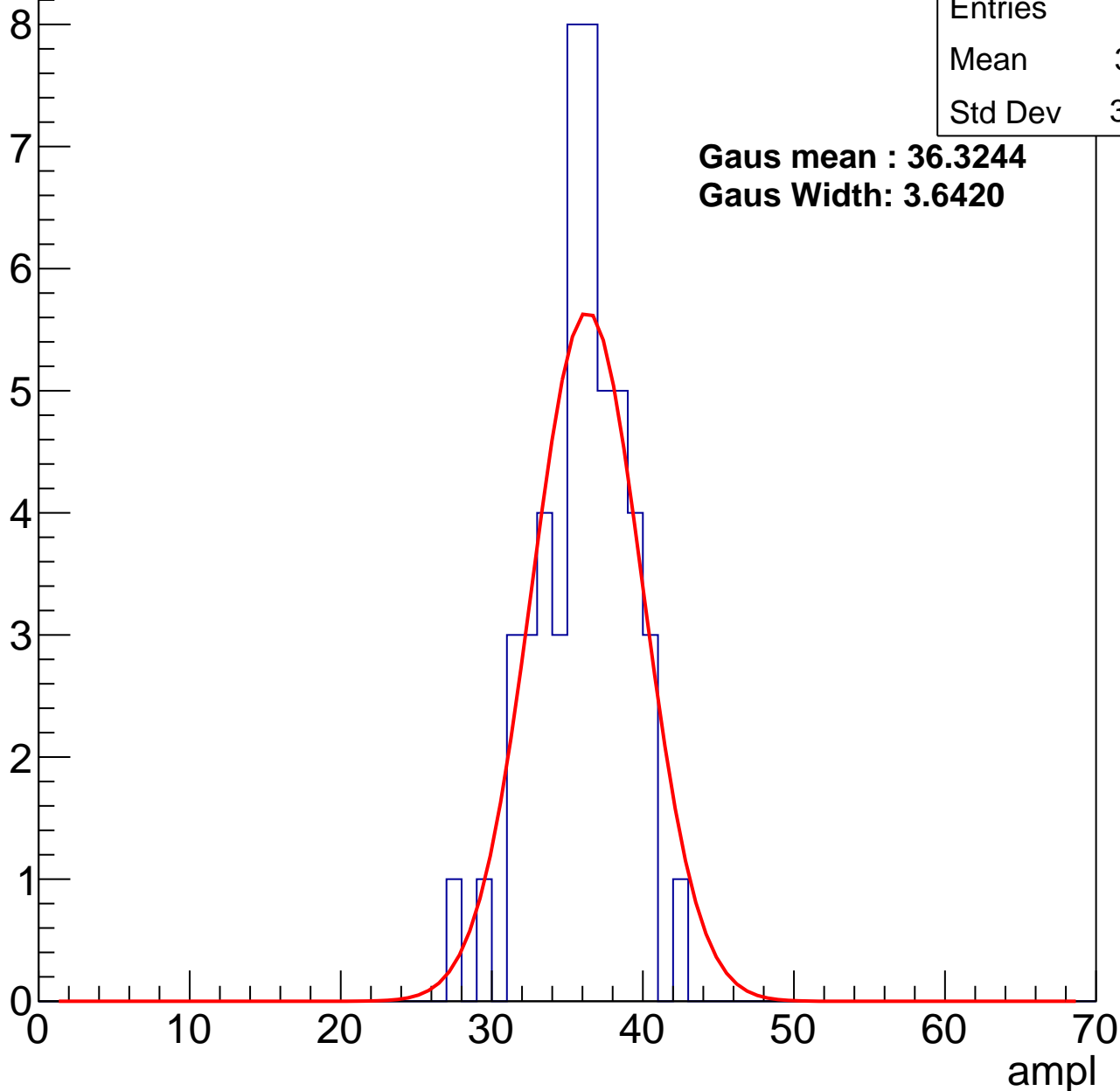
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	35.51
Std Dev	3.004

**Gaus mean : 36.3244**

**Gaus Width: 3.6420**



# B1L103S, U2-ch21, adc2

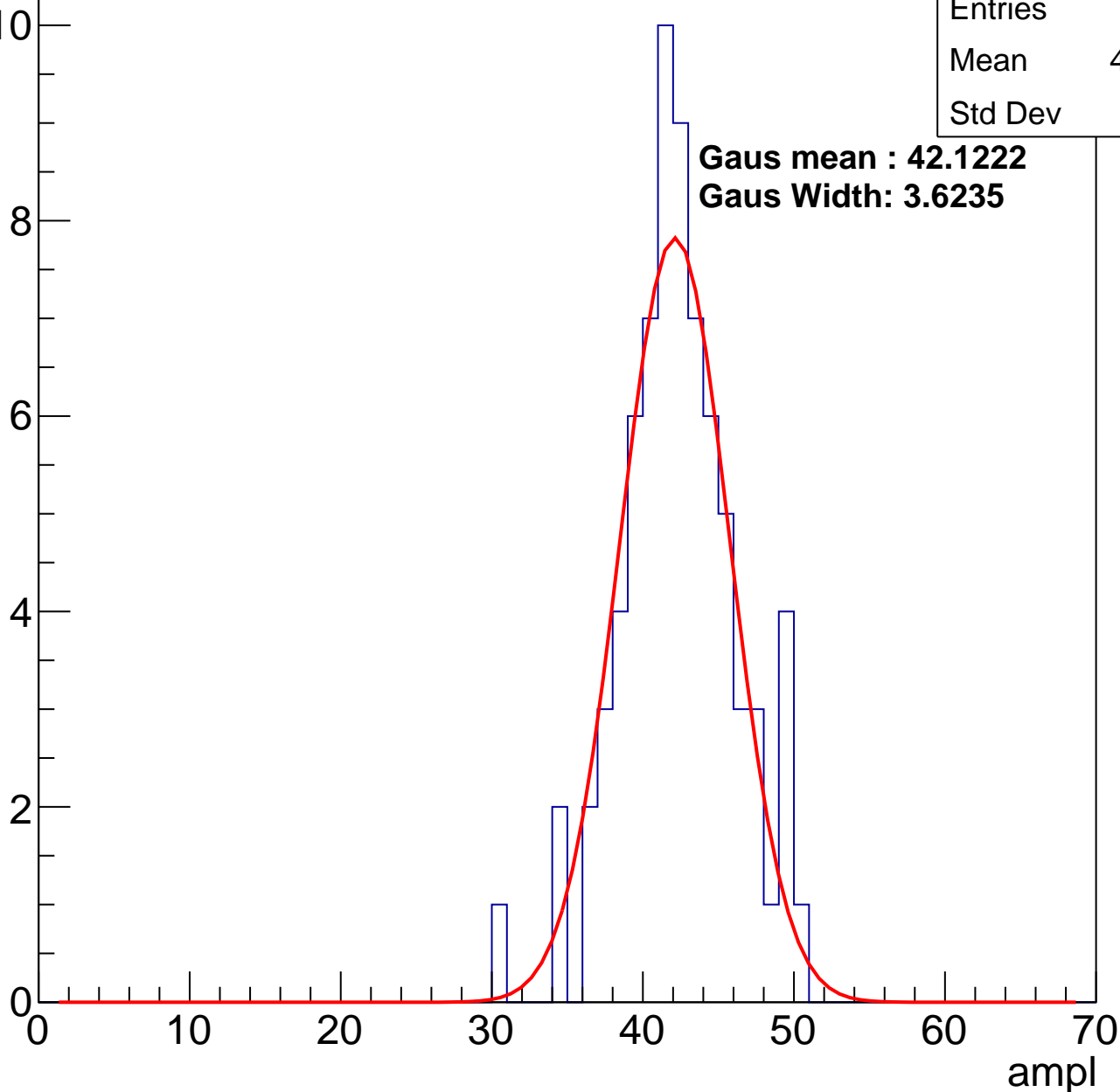
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	41.86
Std Dev	3.8

**Gaus mean : 42.1222**

**Gaus Width: 3.6235**

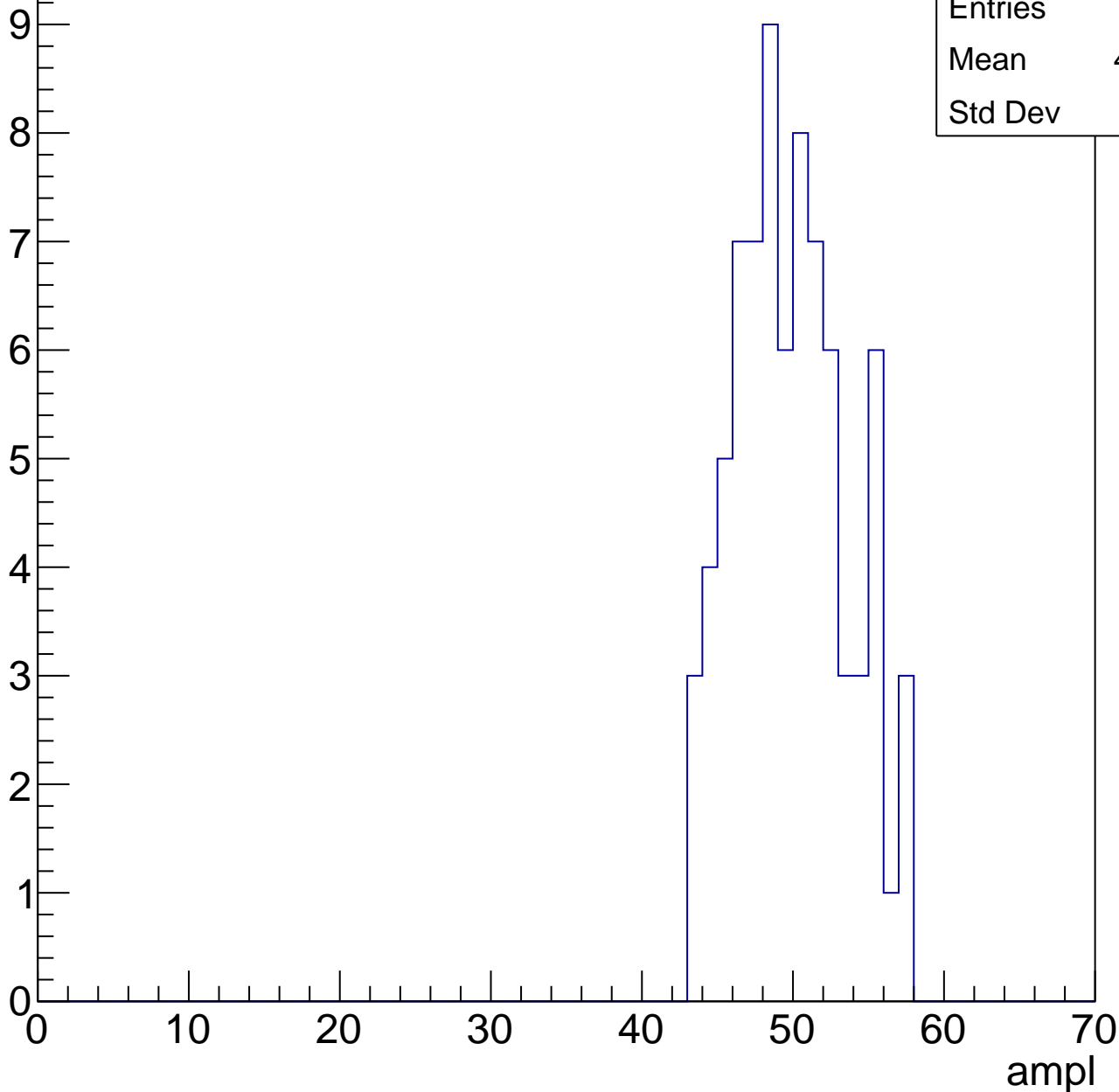


# B1L103S, U2-ch21, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	49.41
Std Dev	3.66

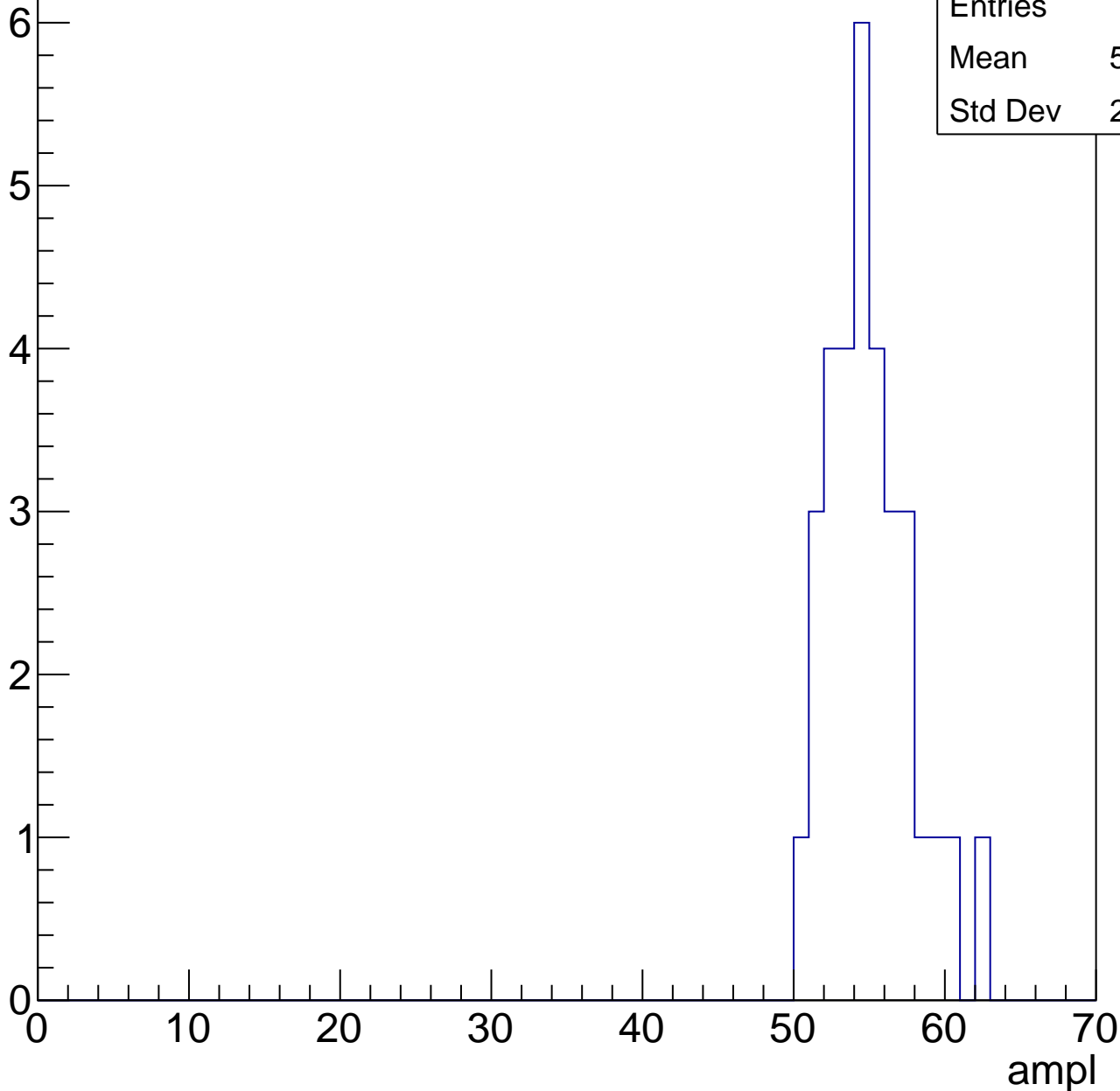


# B1L103S, U2-ch21, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	32
Mean	54.53
Std Dev	2.727

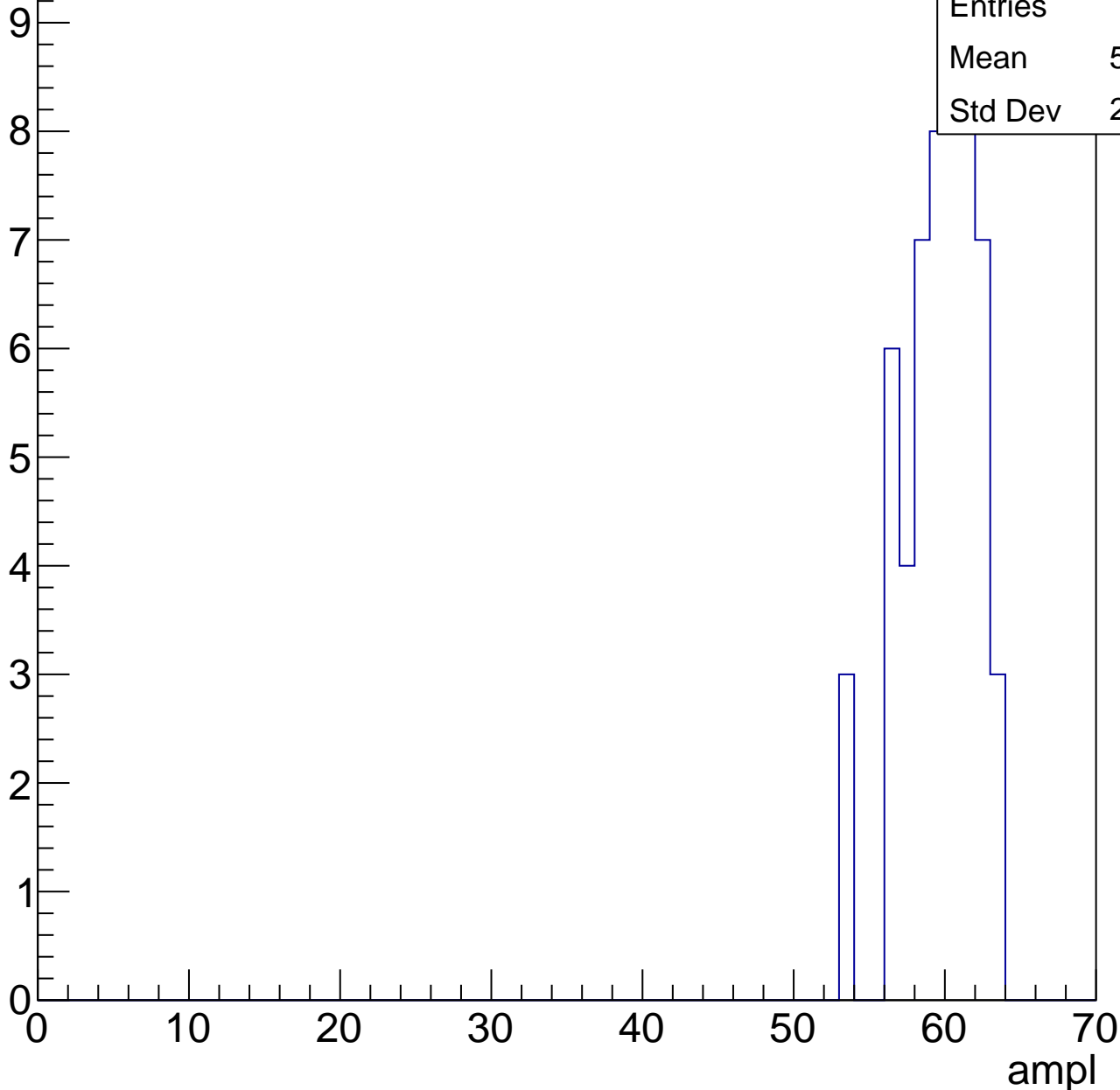


# B1L103S, U2-ch21, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	59.15
Std Dev	2.482

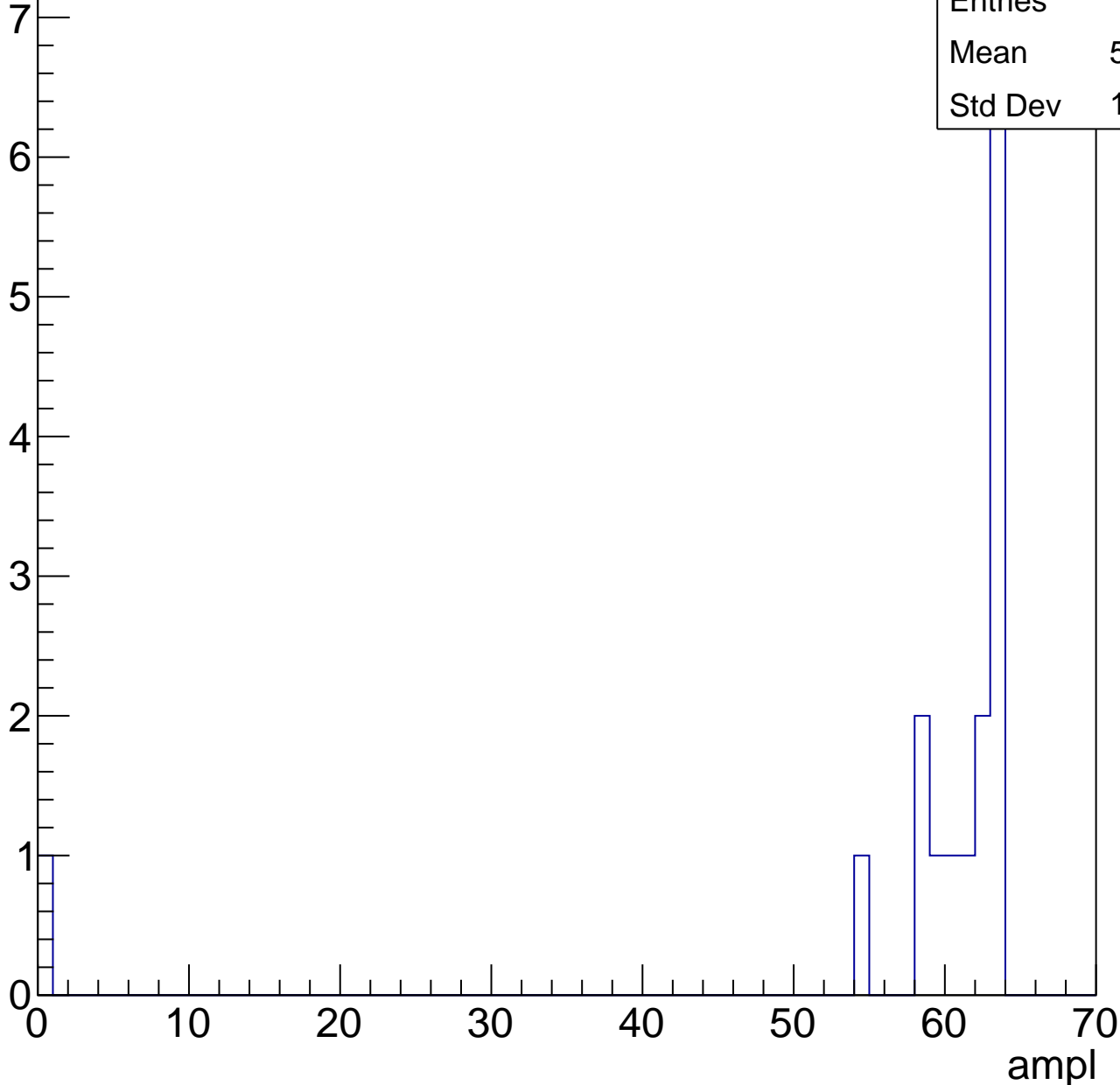


# B1L103S, U2-ch21, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	16
Mean	57.19
Std Dev	14.98





# B1L103S, U2-ch21, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U2-ch22, adc0

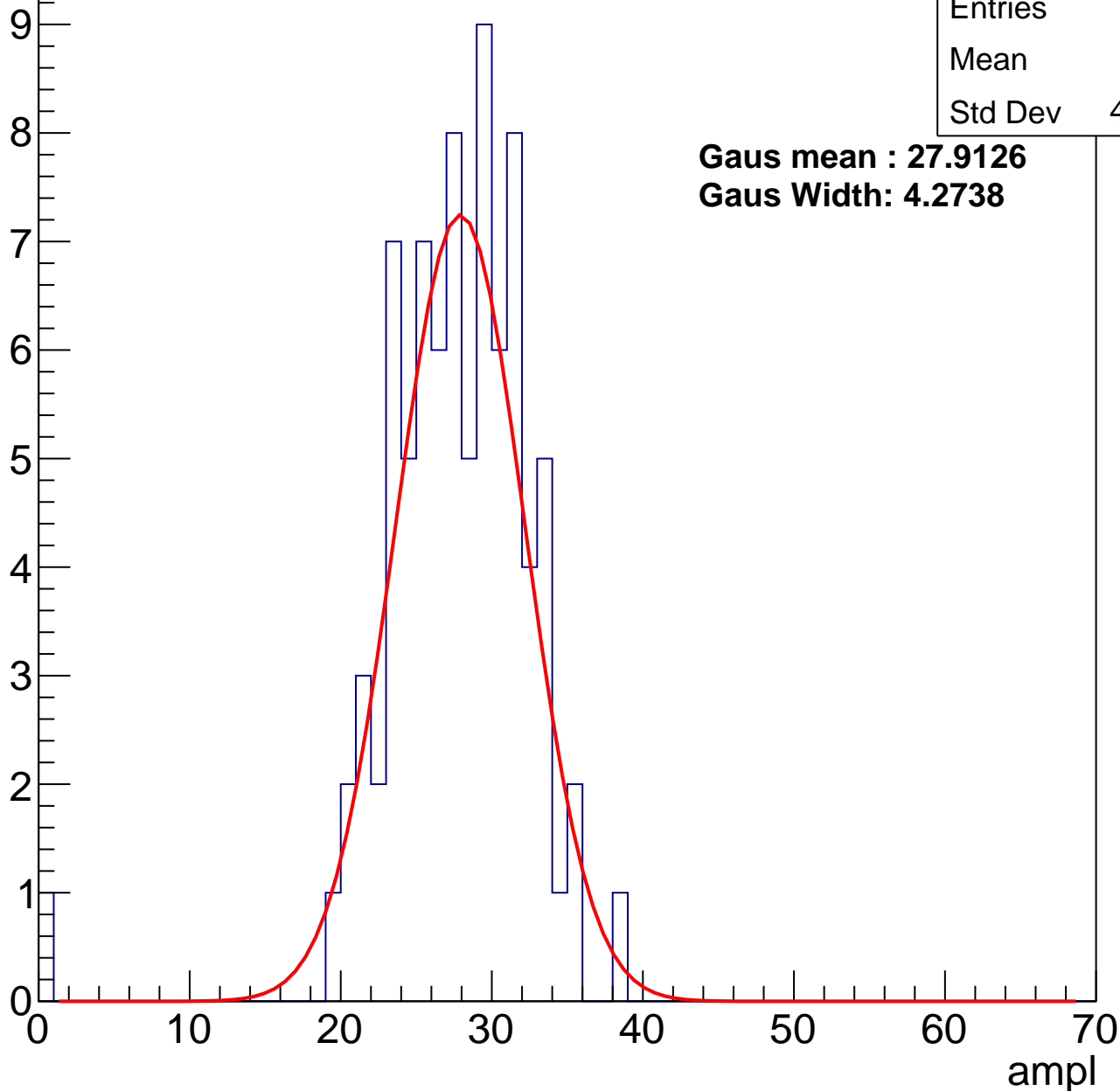
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	83
Mean	27.2
Std Dev	4.955

**Gaus mean : 27.9126**

**Gaus Width: 4.2738**



# B1L103S, U2-ch22, adc1

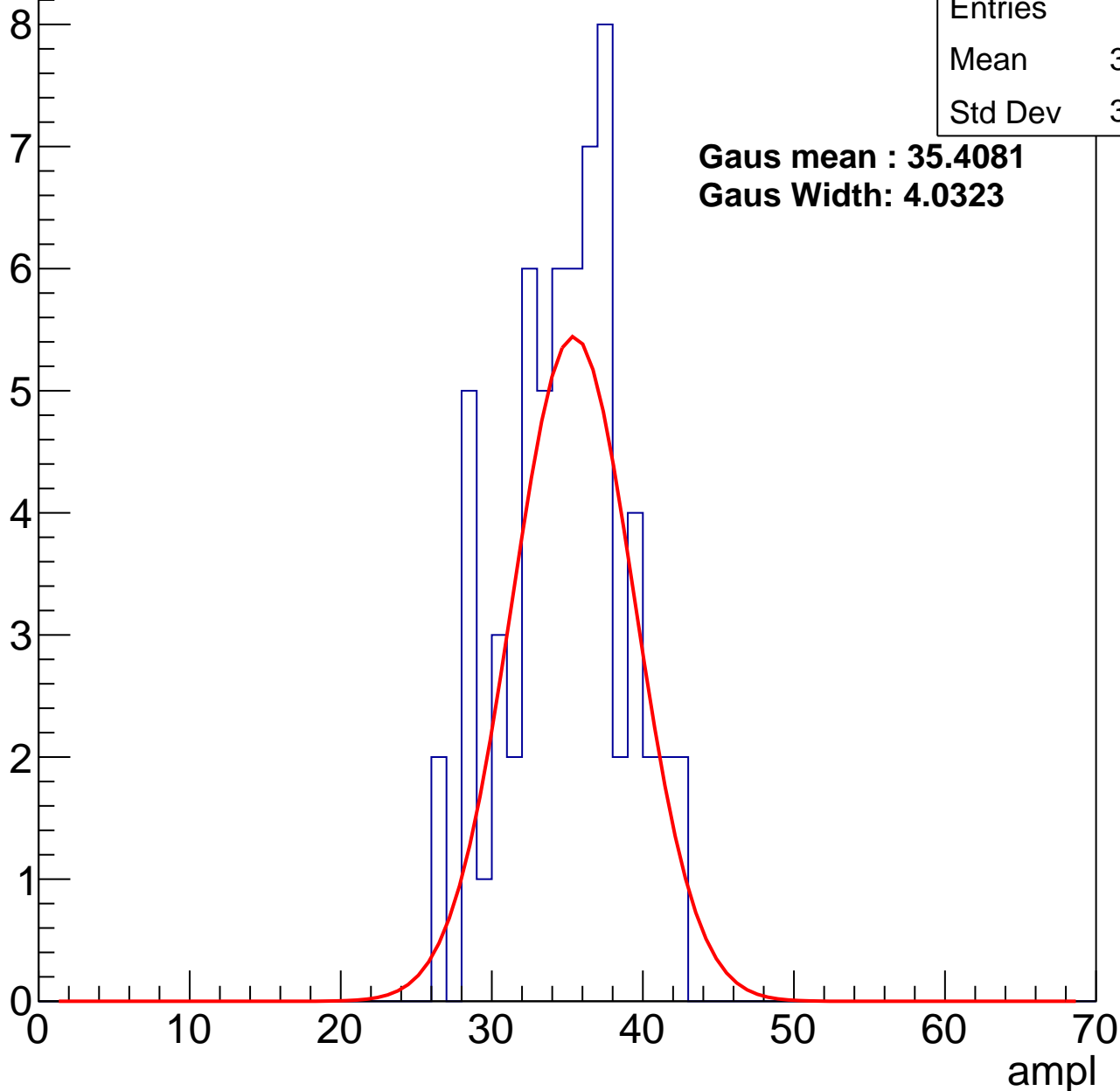
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	34.44
Std Dev	3.886

**Gaus mean : 35.4081**

**Gaus Width: 4.0323**



# B1L103S, U2-ch22, adc2

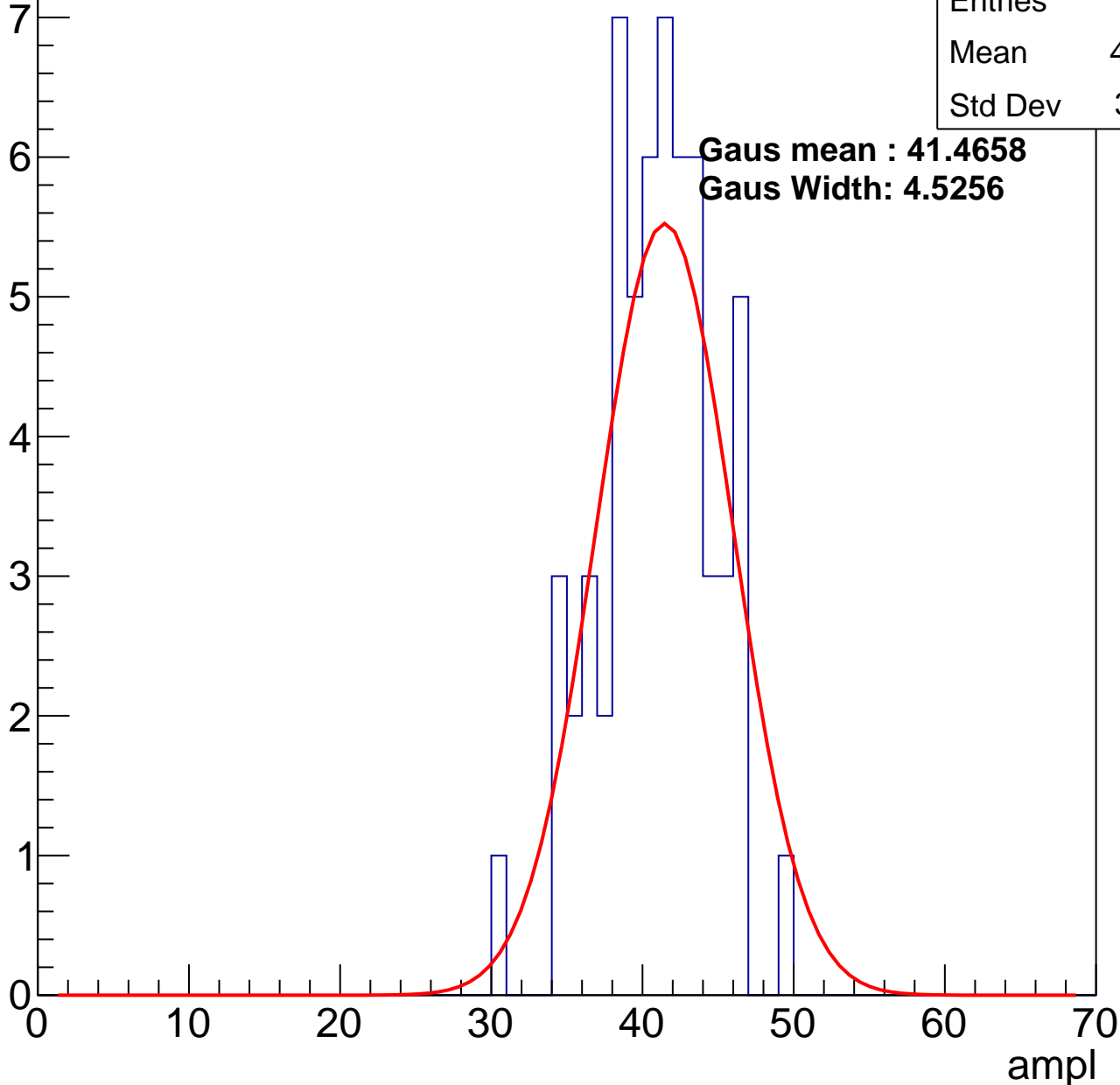
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	40.47
Std Dev	3.681

**Gaus mean : 41.4658**

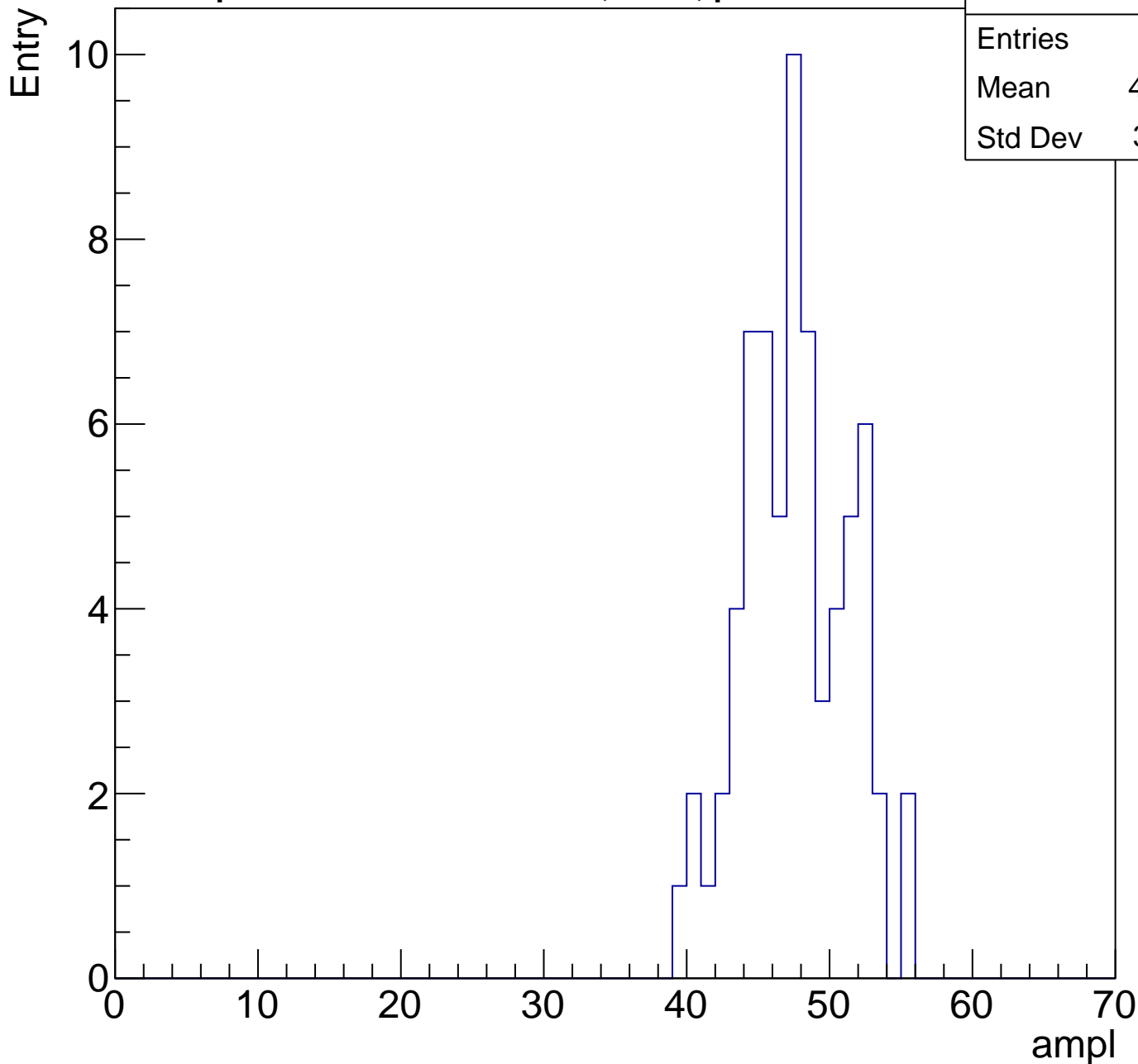
**Gaus Width: 4.5256**



# B1L103S, U2-ch22, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	68
Mean	47.13
Std Dev	3.621

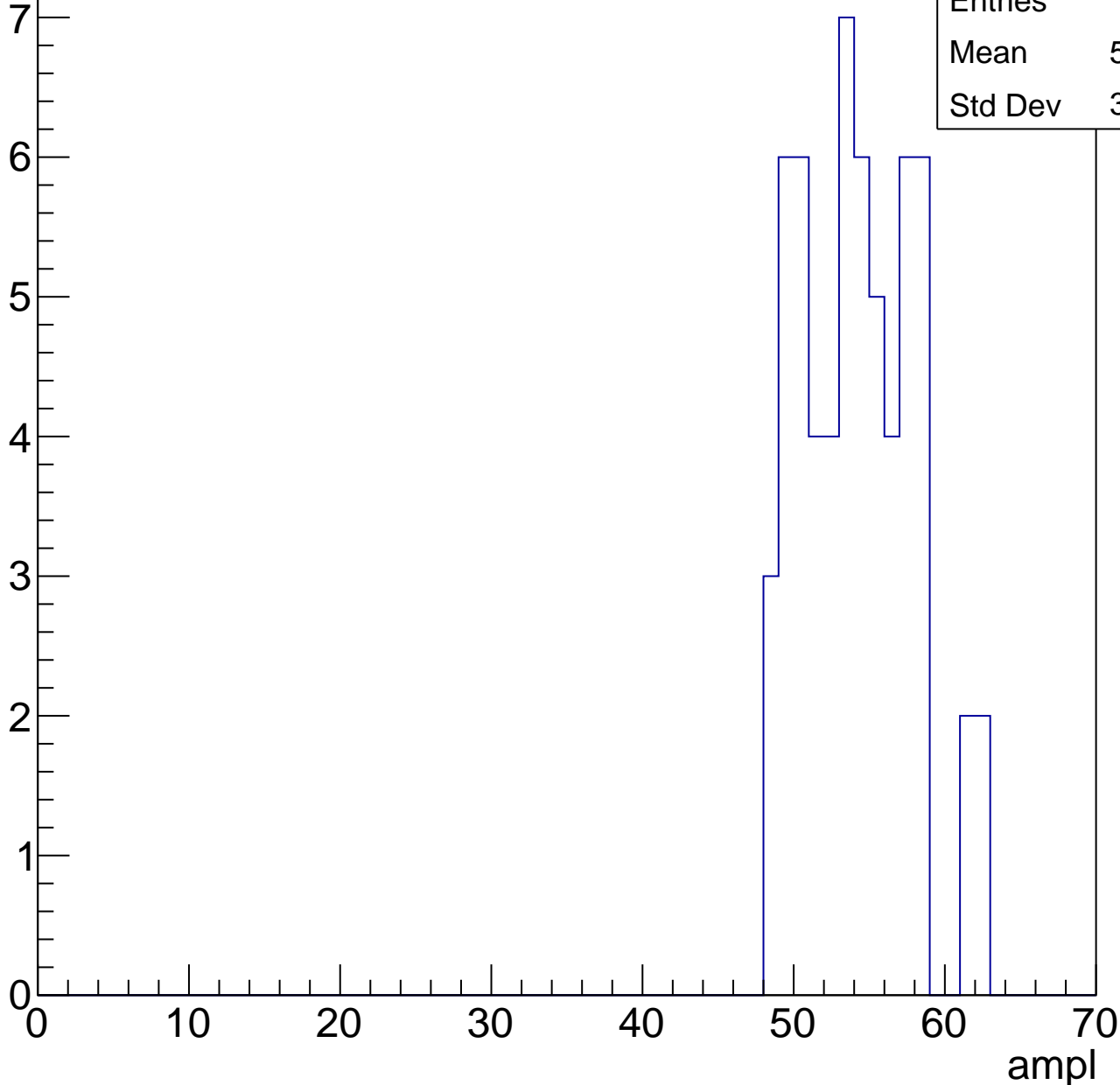


# B1L103S, U2-ch22, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	53.77
Std Dev	3.637

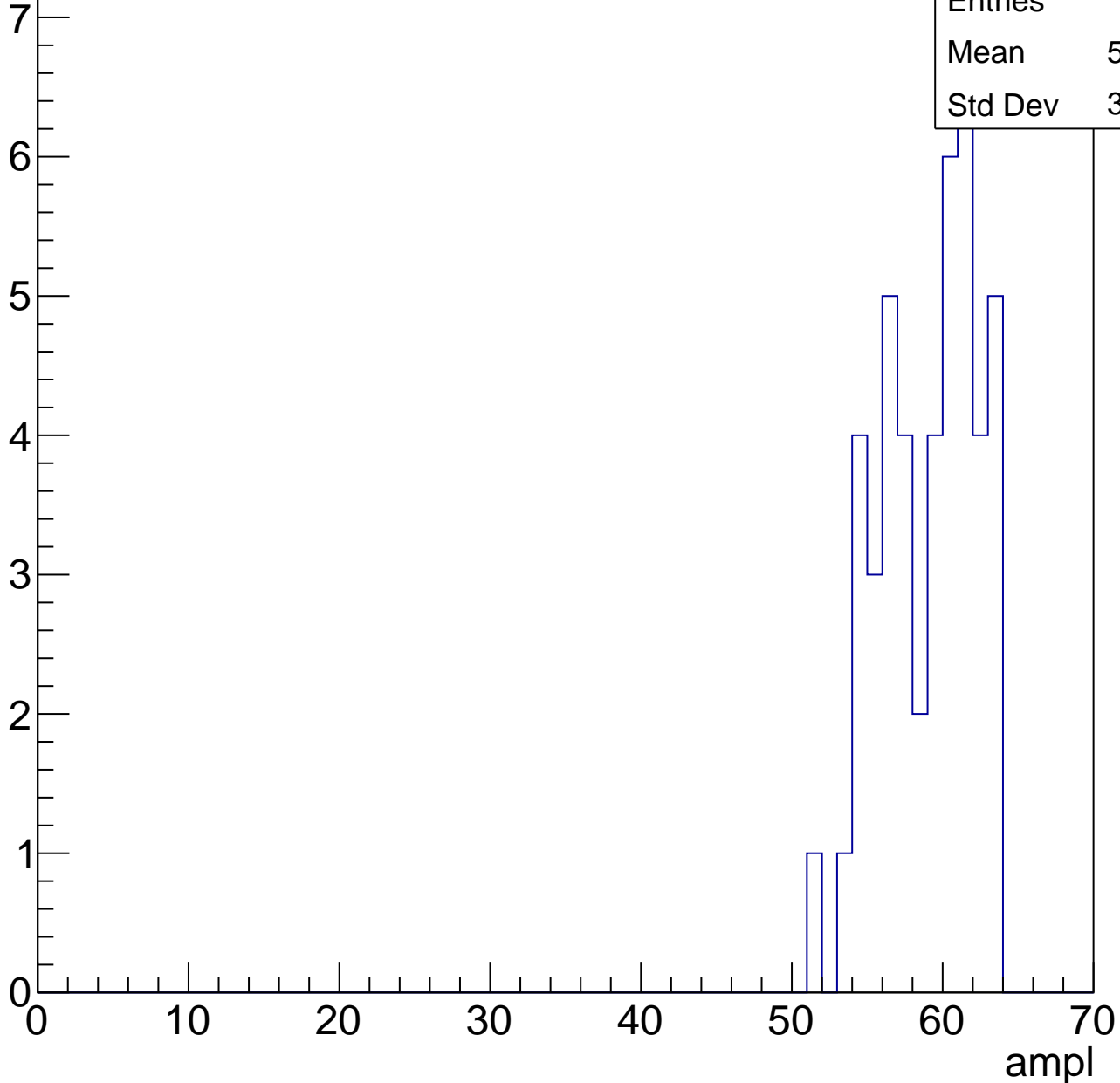


# B1L103S, U2-ch22, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	46
Mean	58.59
Std Dev	3.139

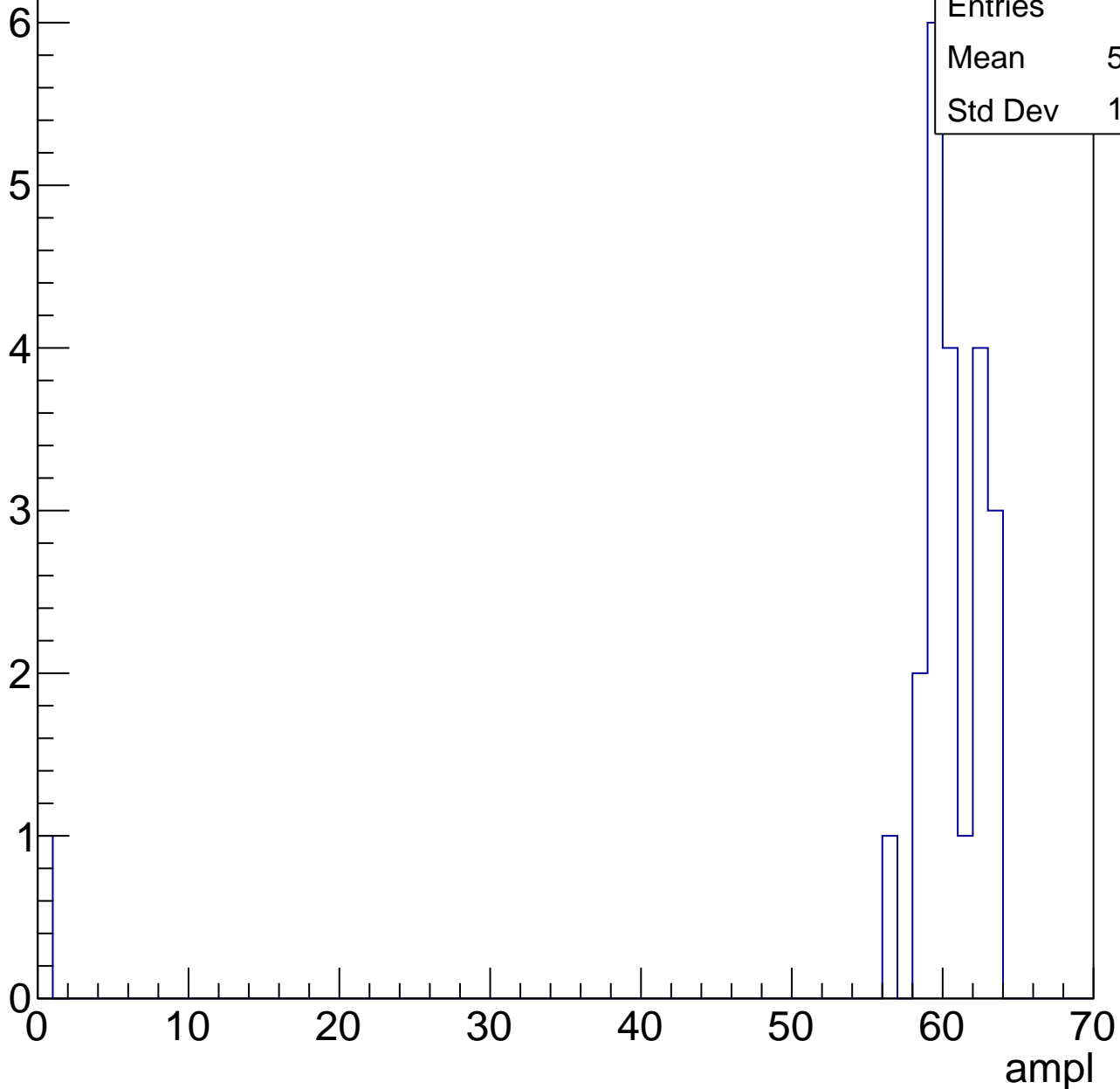


# B1L103S, U2-ch22, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	22
Mean	57.45
Std Dev	12.67





# B1L103S, U2-ch22, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch23, adc0

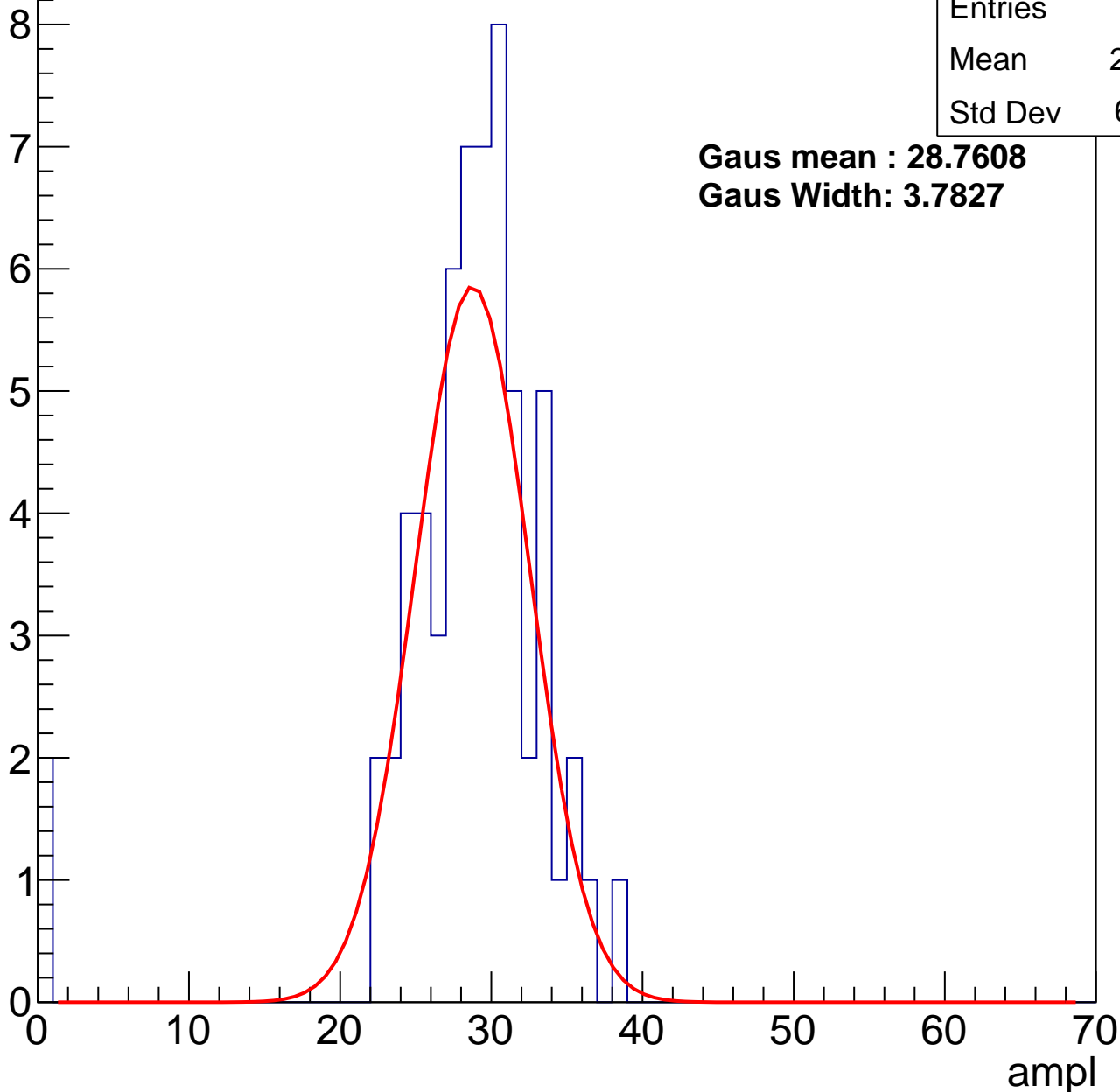
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	27.85
Std Dev	6.151

**Gaus mean : 28.7608**

**Gaus Width: 3.7827**



# B1L103S, U2-ch23, adc1

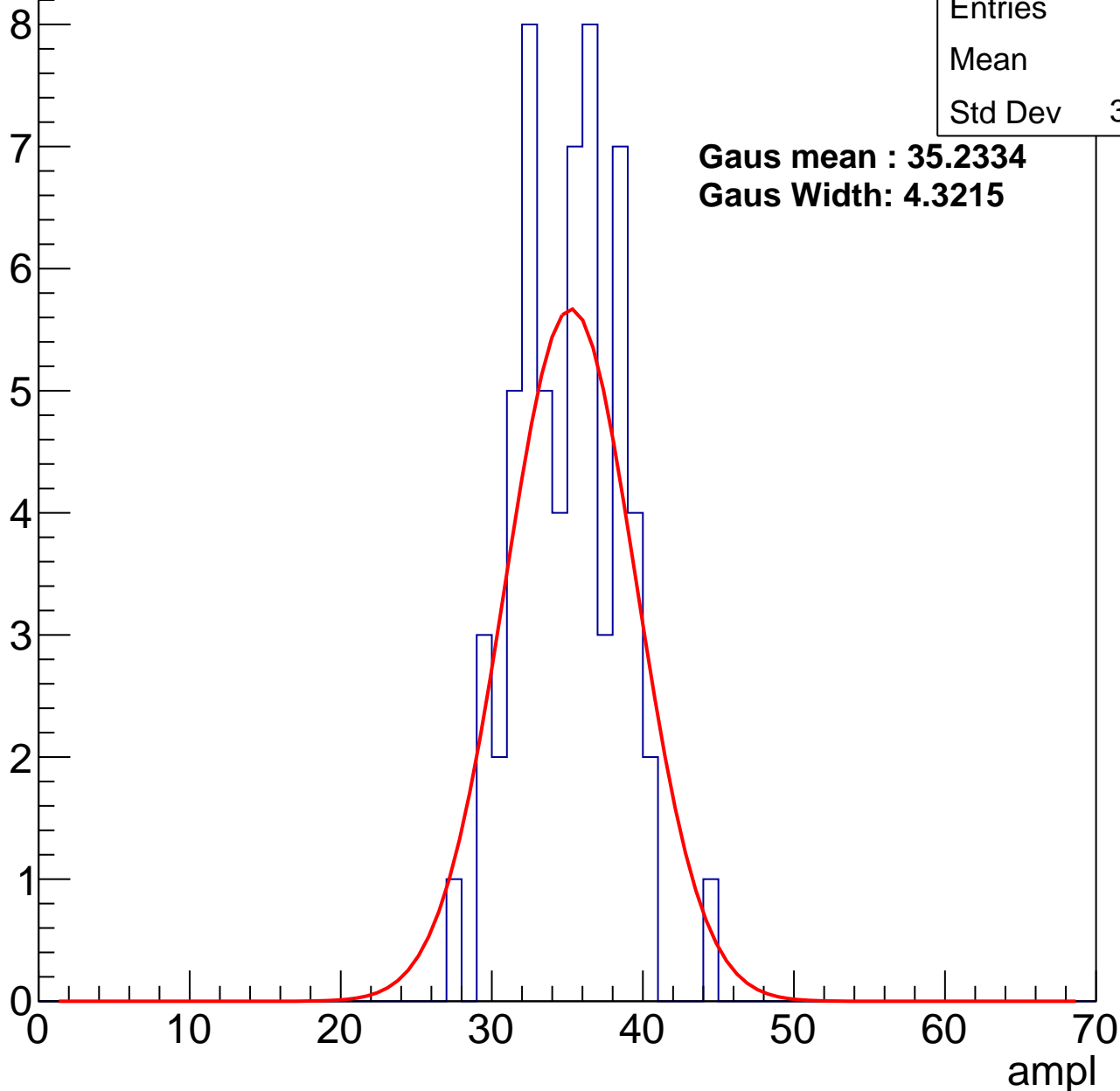
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	34.6
Std Dev	3.333

**Gaus mean : 35.2334**

**Gaus Width: 4.3215**



# B1L103S, U2-ch23, adc2

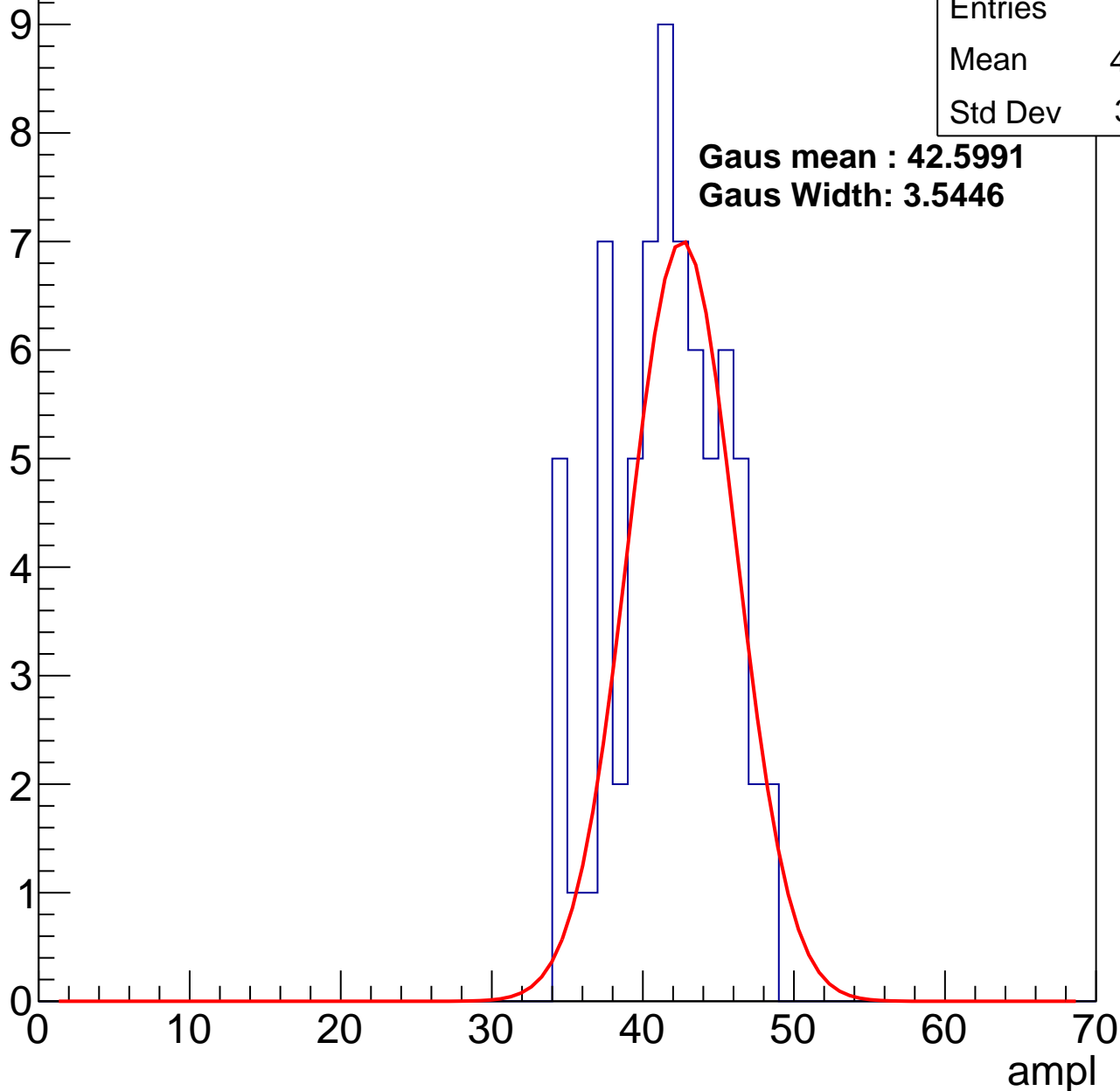
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	41.17
Std Dev	3.641

**Gaus mean : 42.5991**

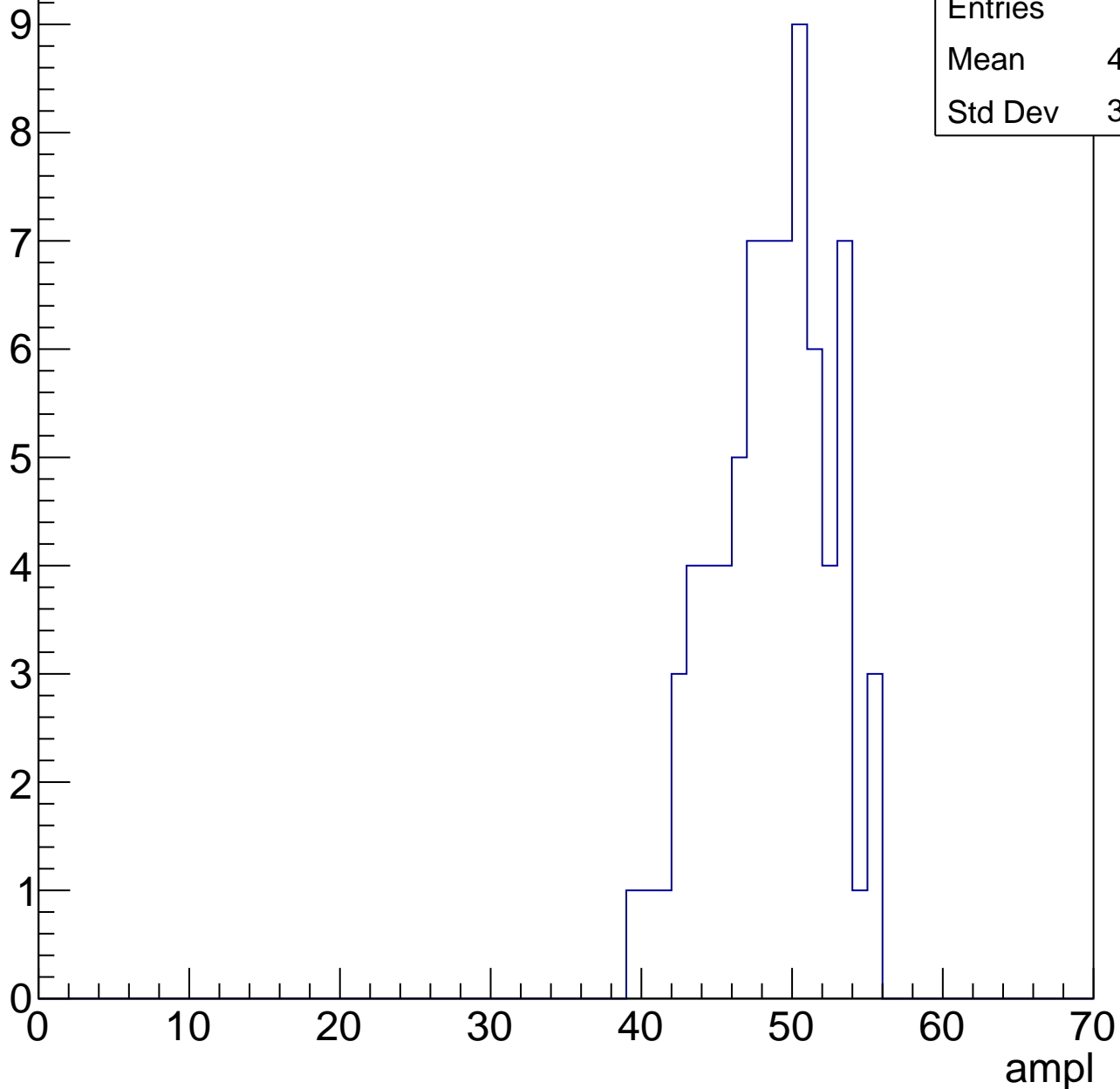
**Gaus Width: 3.5446**



# B1L103S, U2-ch23, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

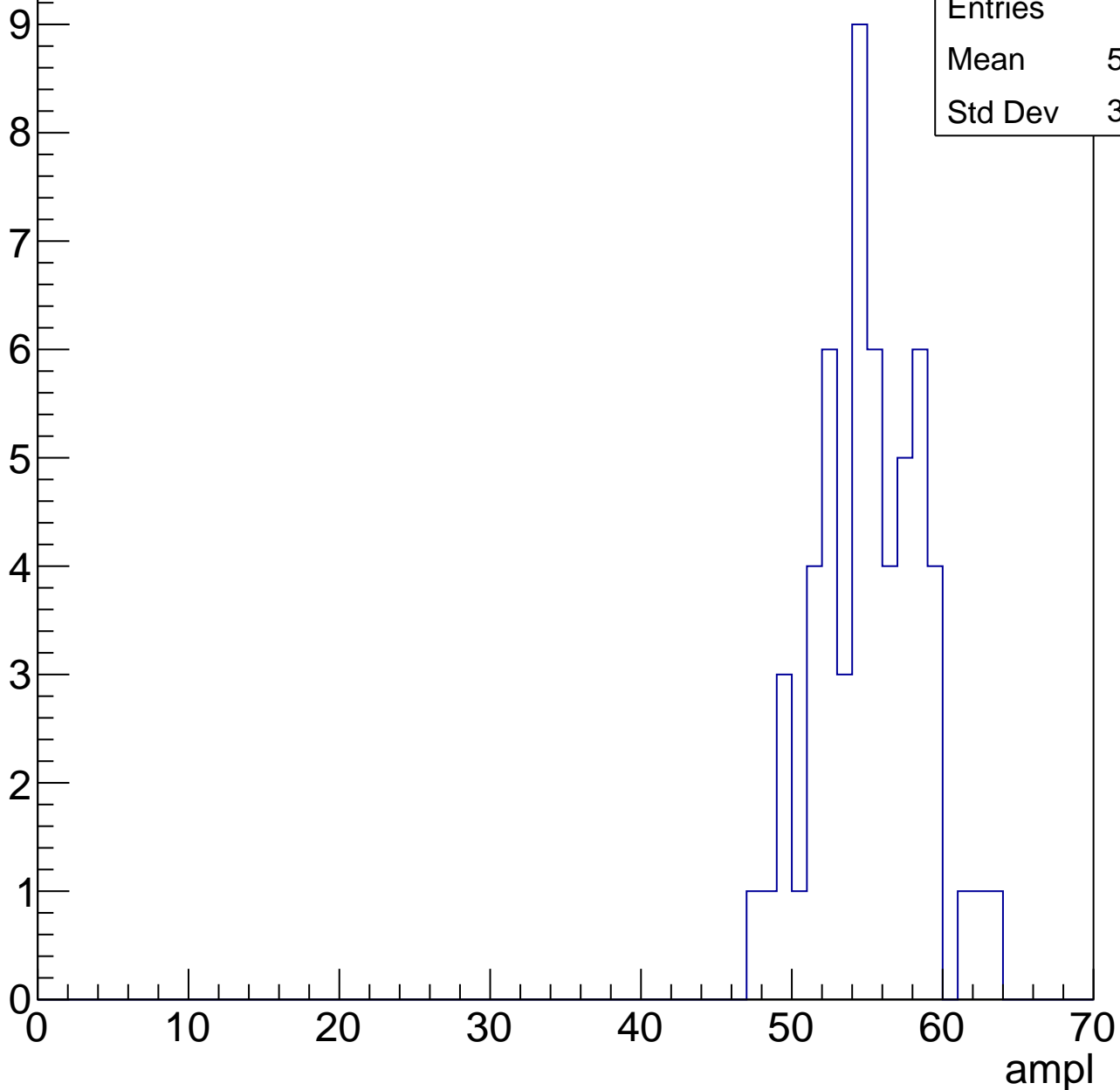


# B1L103S, U2-ch23, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

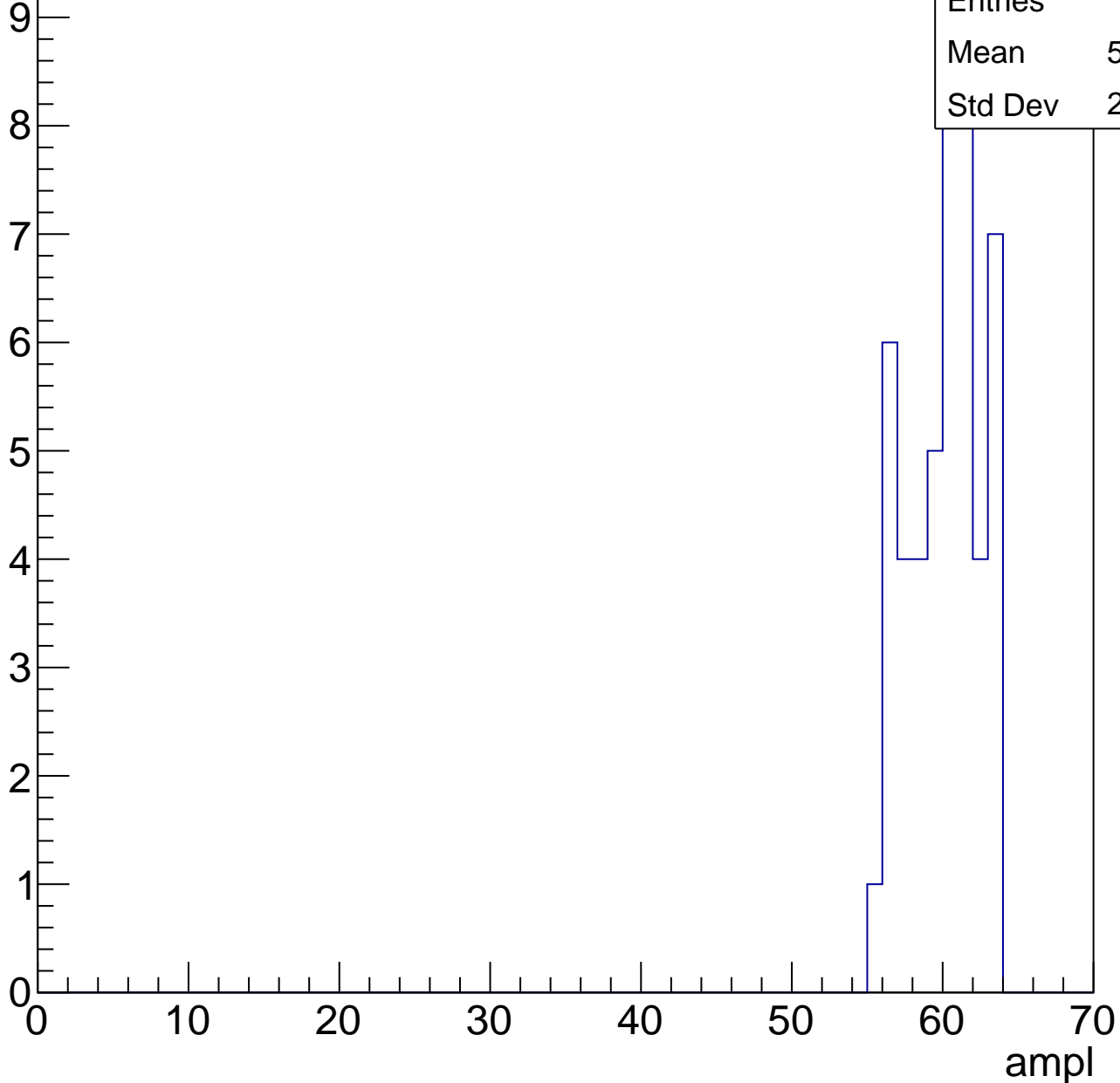
Entries	56
Mean	54.68
Std Dev	3.459



# B1L103S, U2-ch23, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

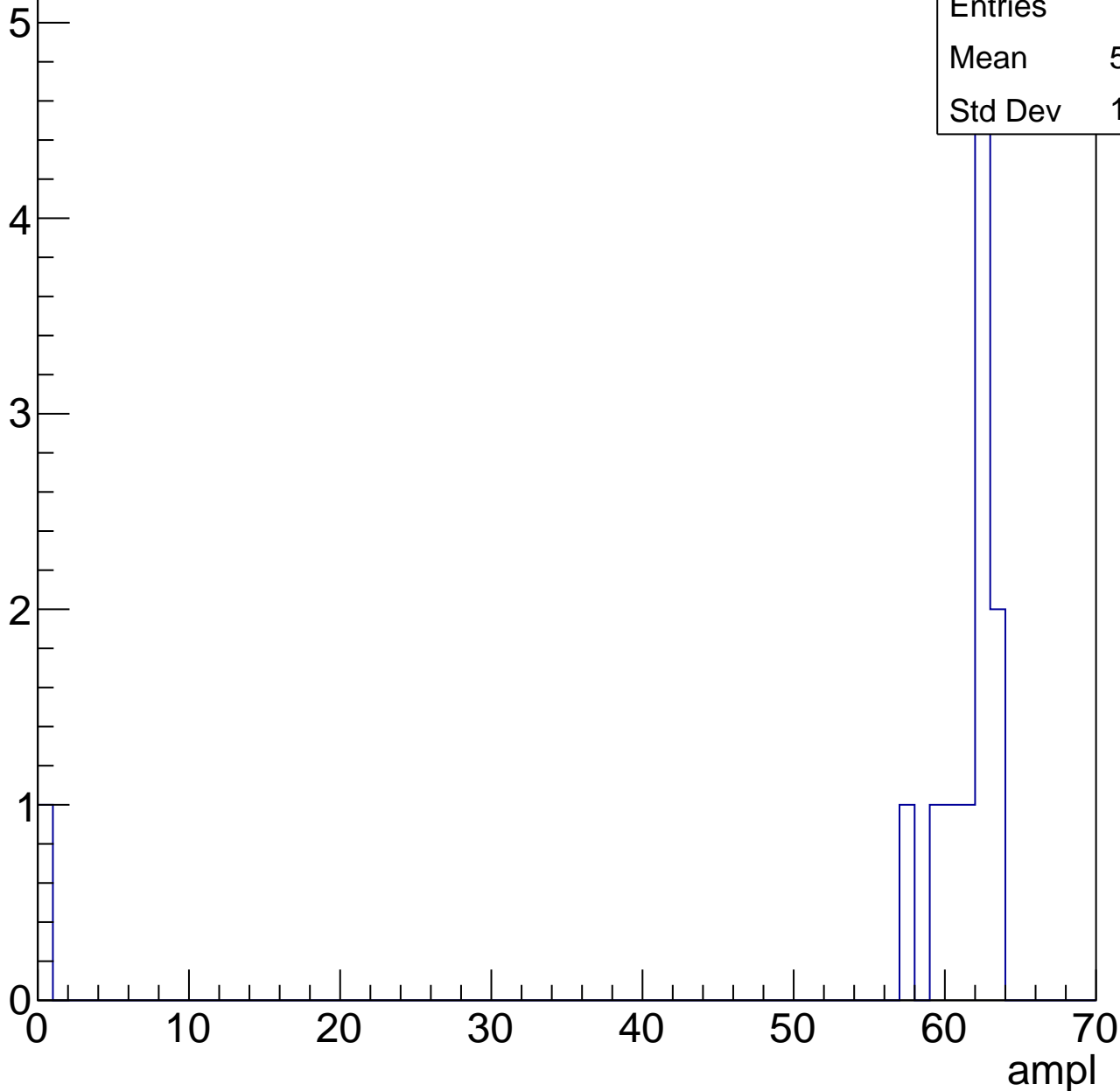


# B1L103S, U2-ch23, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	12
Mean	56.08
Std Dev	16.99





# B1L103S, U2-ch23, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	10.5
Std Dev	10.5

# B1L103S, U2-ch24, adc0

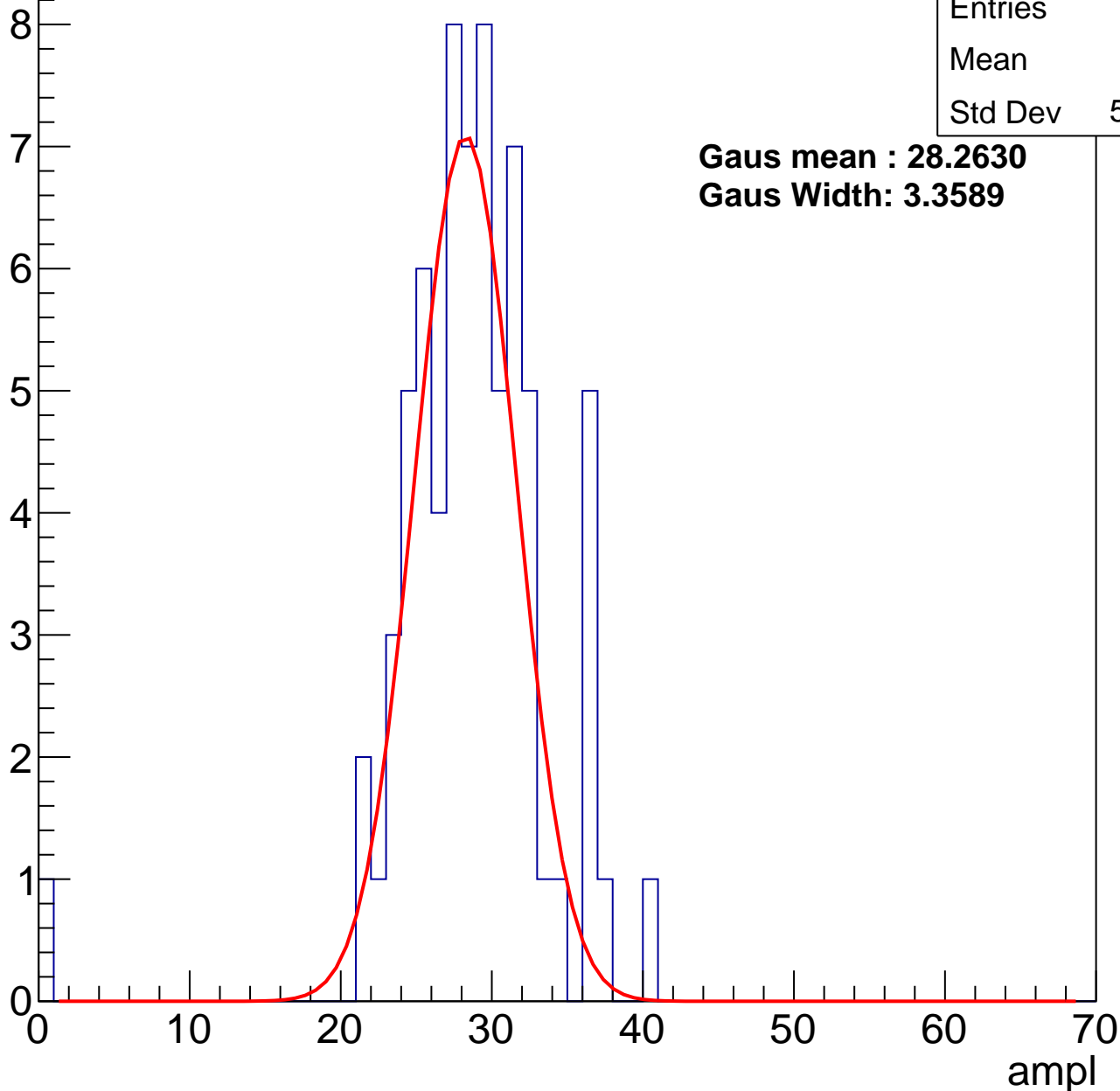
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	28.2
Std Dev	5.207

**Gaus mean : 28.2630**

**Gaus Width: 3.3589**



# B1L103S, U2-ch24, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	82
Mean	35.87
Std Dev	3.678

**Gaus mean : 36.4713**

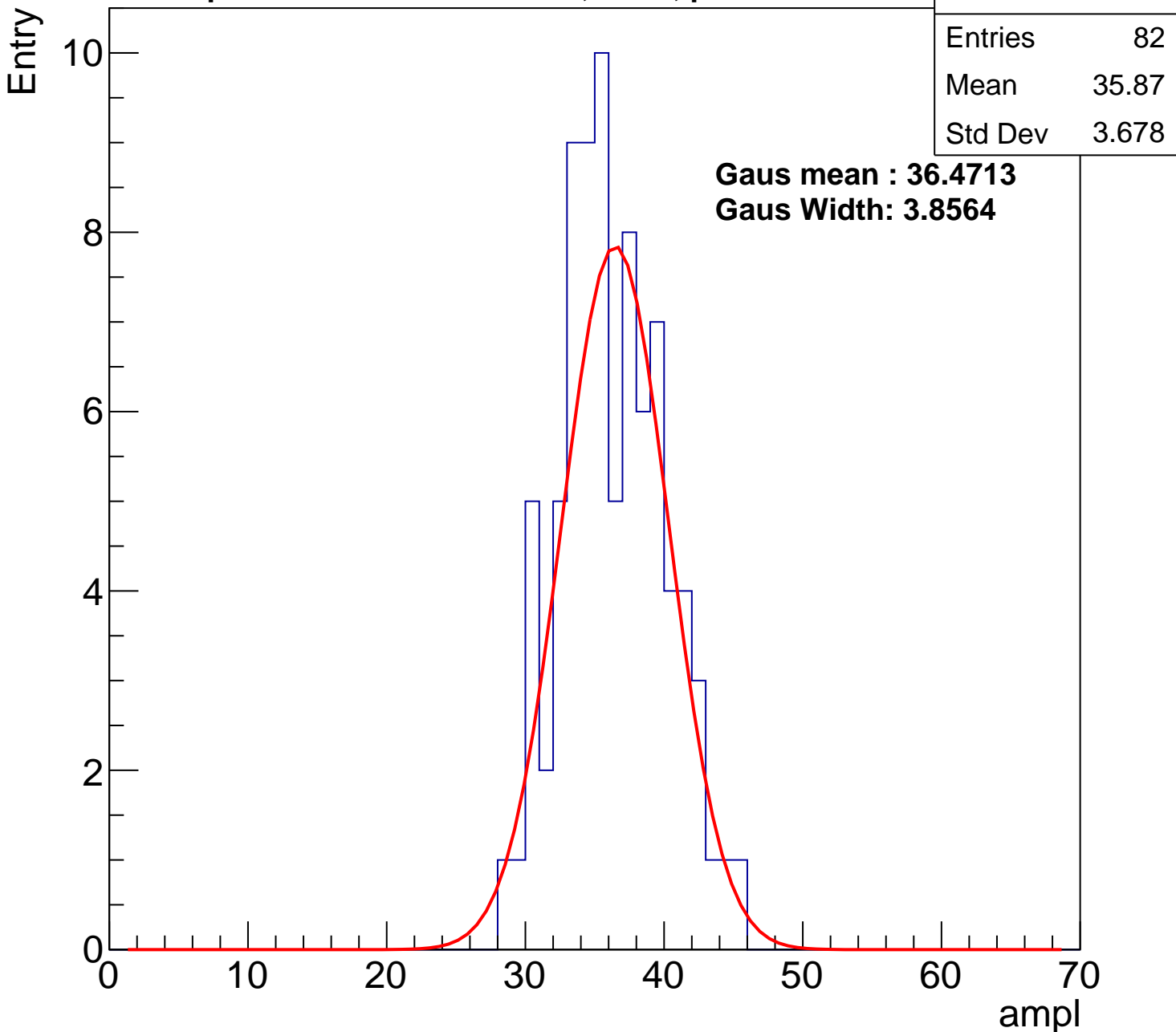
**Gaus Width: 3.8564**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L103S, U2-ch24, adc2

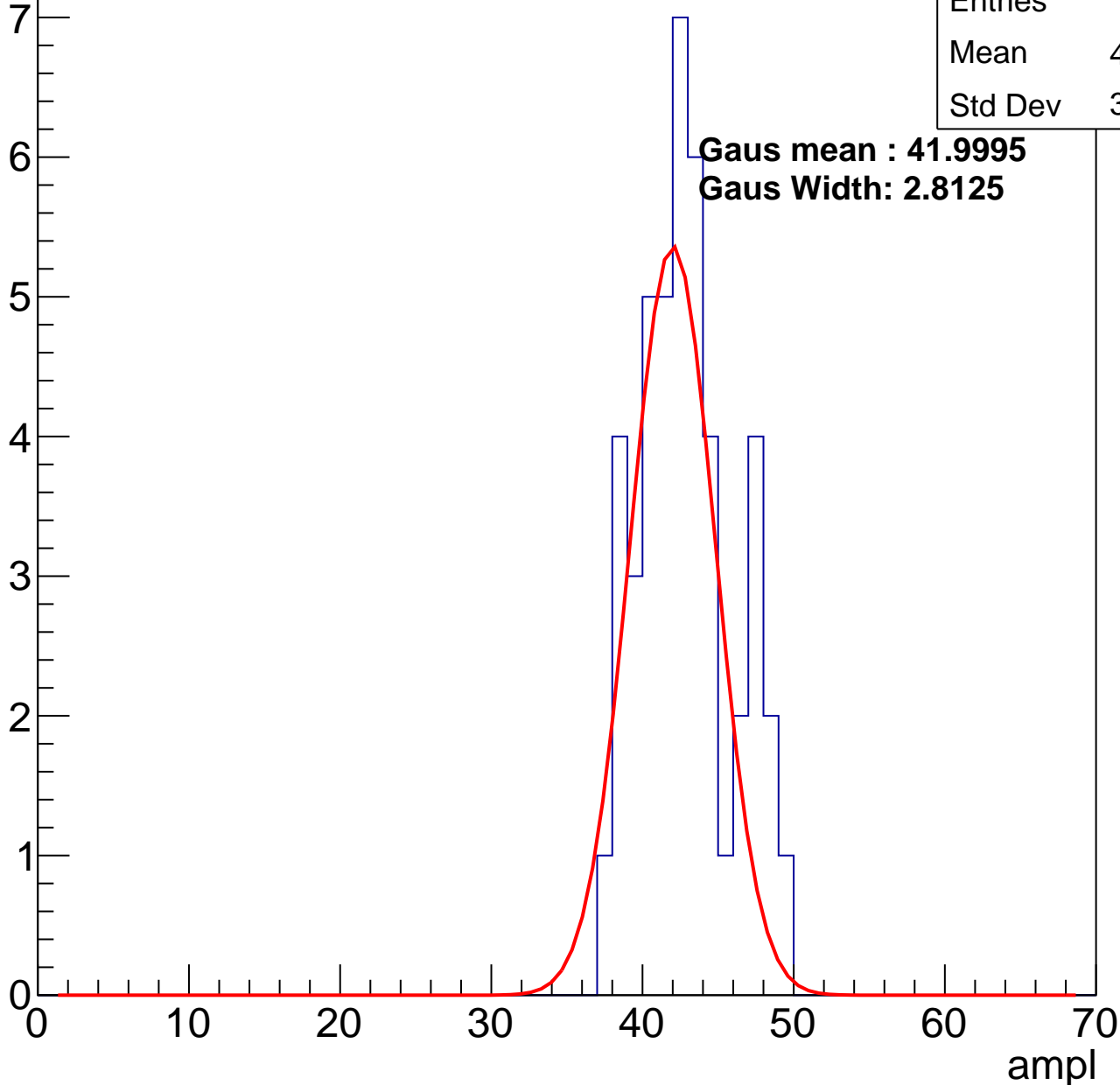
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	45
Mean	42.42
Std Dev	3.044

**Gaus mean : 41.9995**

**Gaus Width: 2.8125**

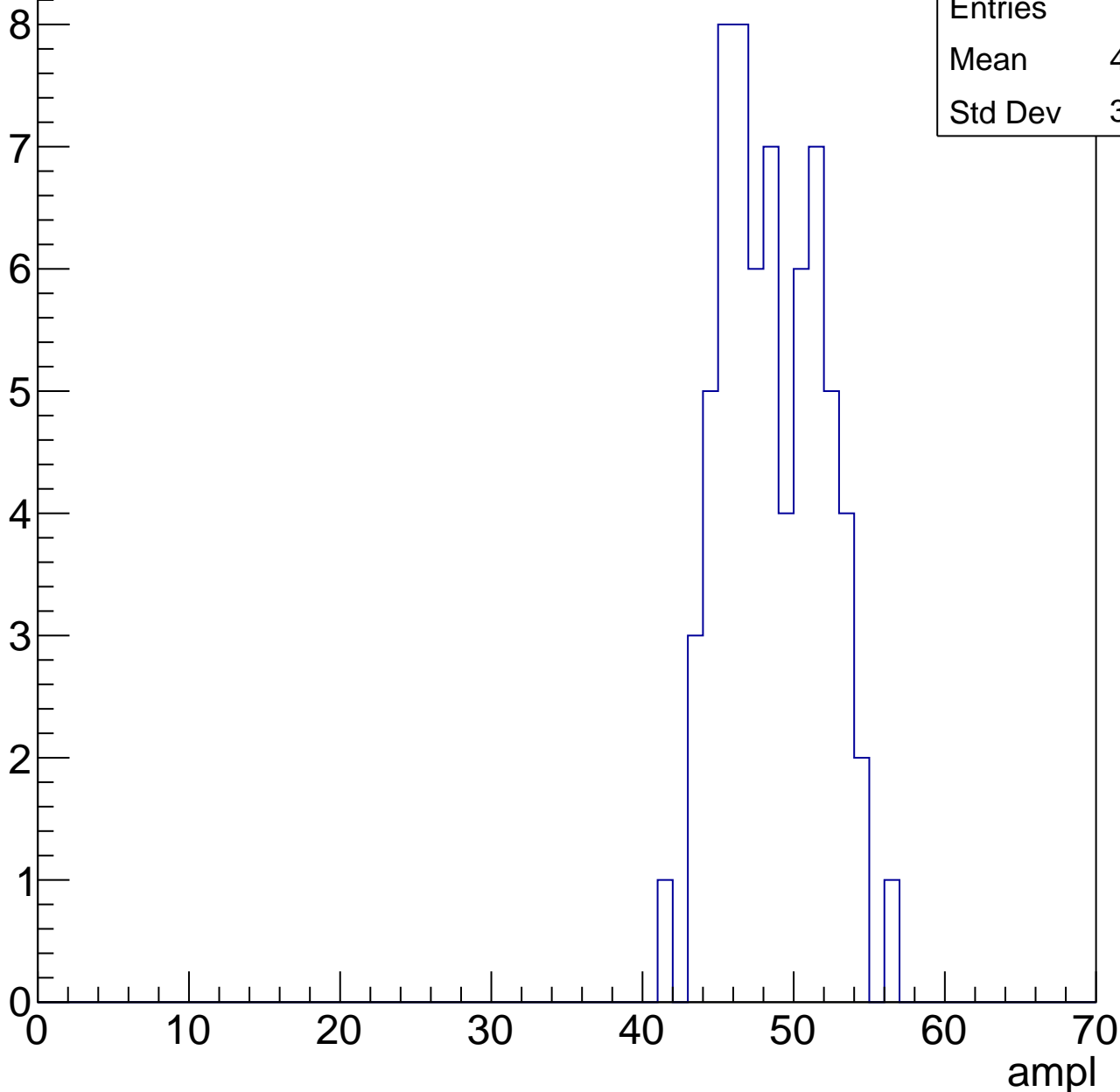


# B1L103S, U2-ch24, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

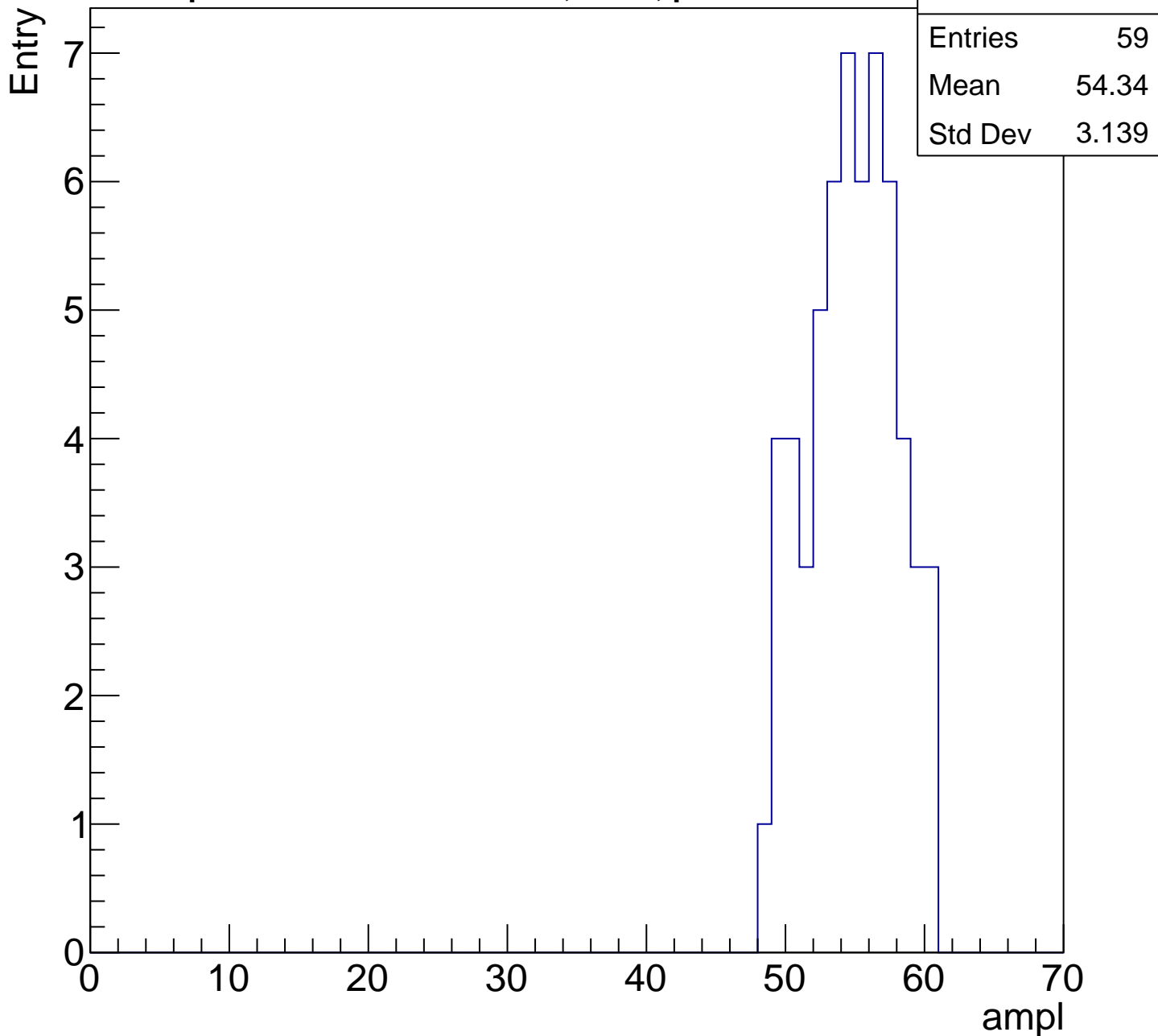
Entry

Entries	67
Mean	48.13
Std Dev	3.278



# B1L103S, U2-ch24, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

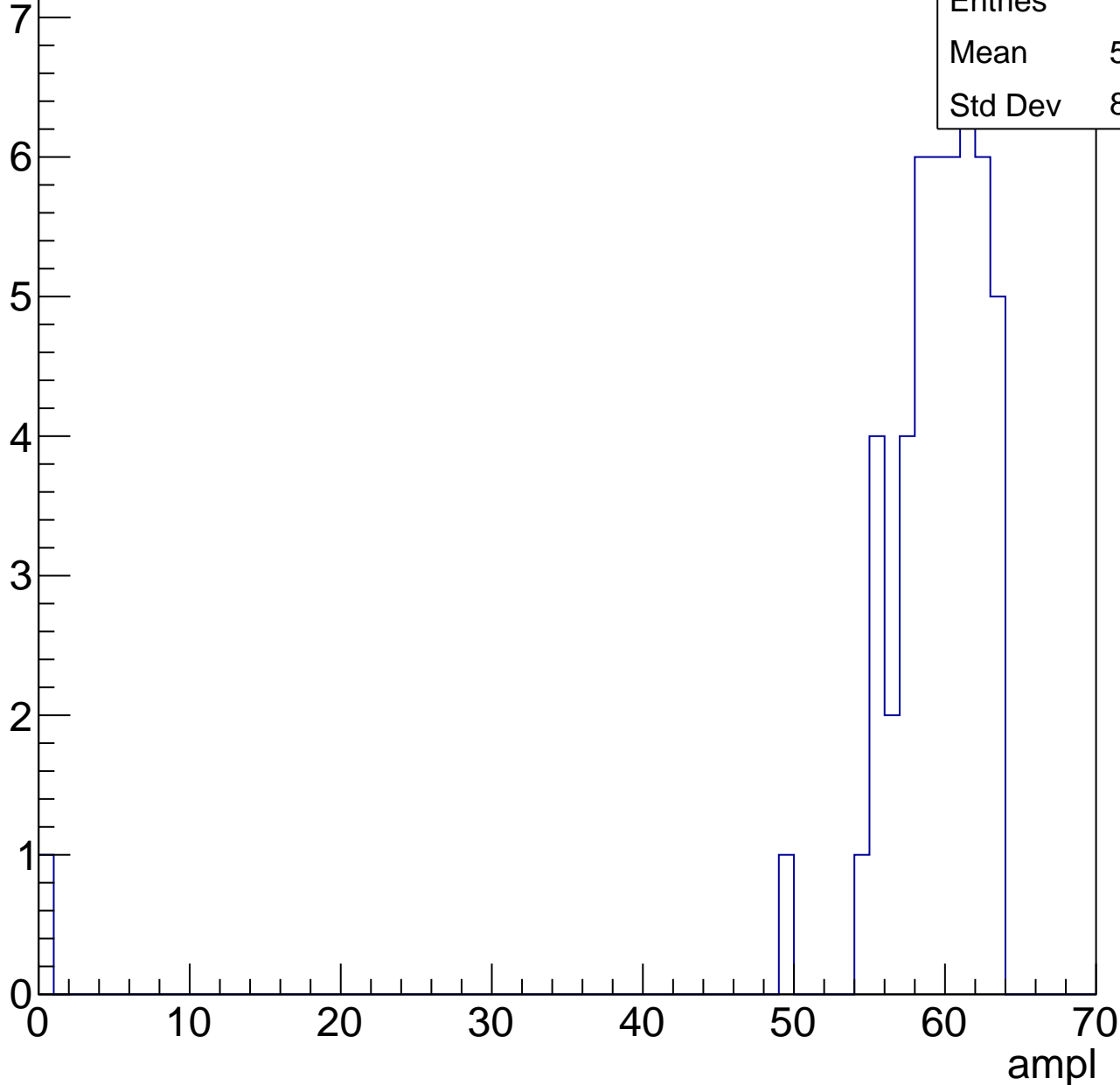


# B1L103S, U2-ch24, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	57.94
Std Dev	8.833

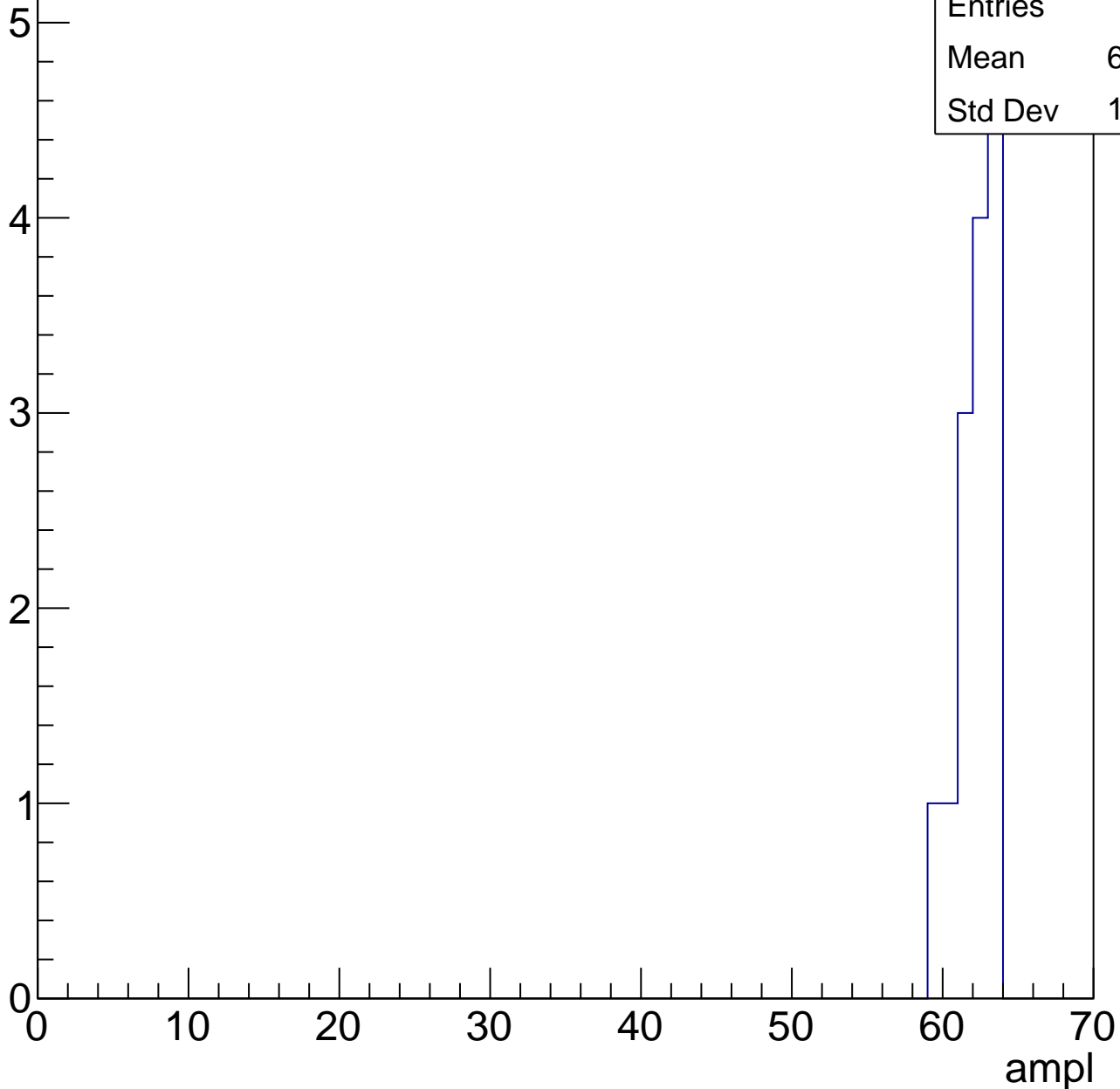


# B1L103S, U2-ch24, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	14
Mean	61.79
Std Dev	1.206





# B1L103S, U2-ch24, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch25, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	93
Mean	29.23
Std Dev	3.719

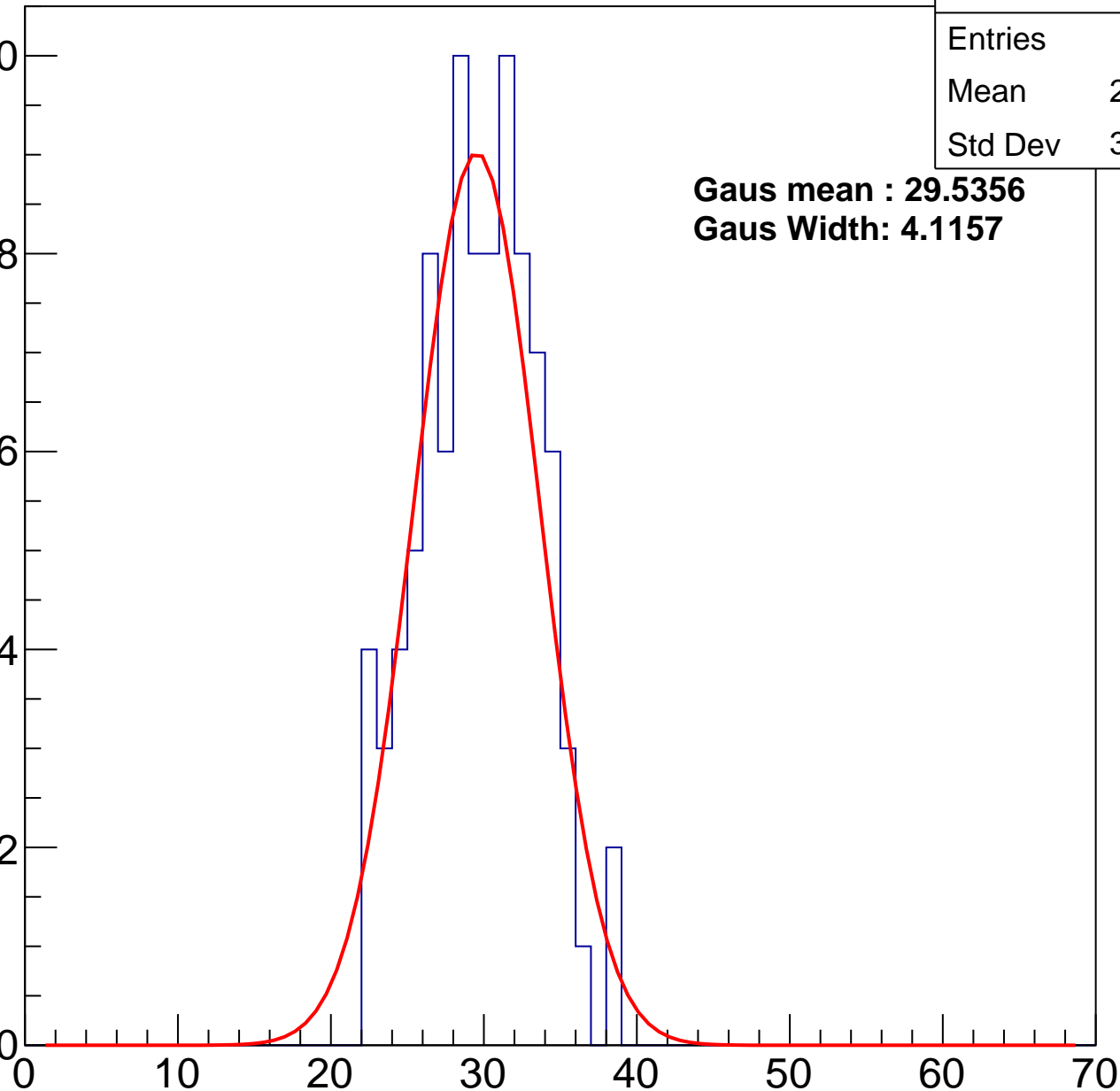
**Gaus mean : 29.5356**

**Gaus Width: 4.1157**

Entry

10  
8  
6  
4  
2  
0

ampl



# B1L103S, U2-ch25, adc1

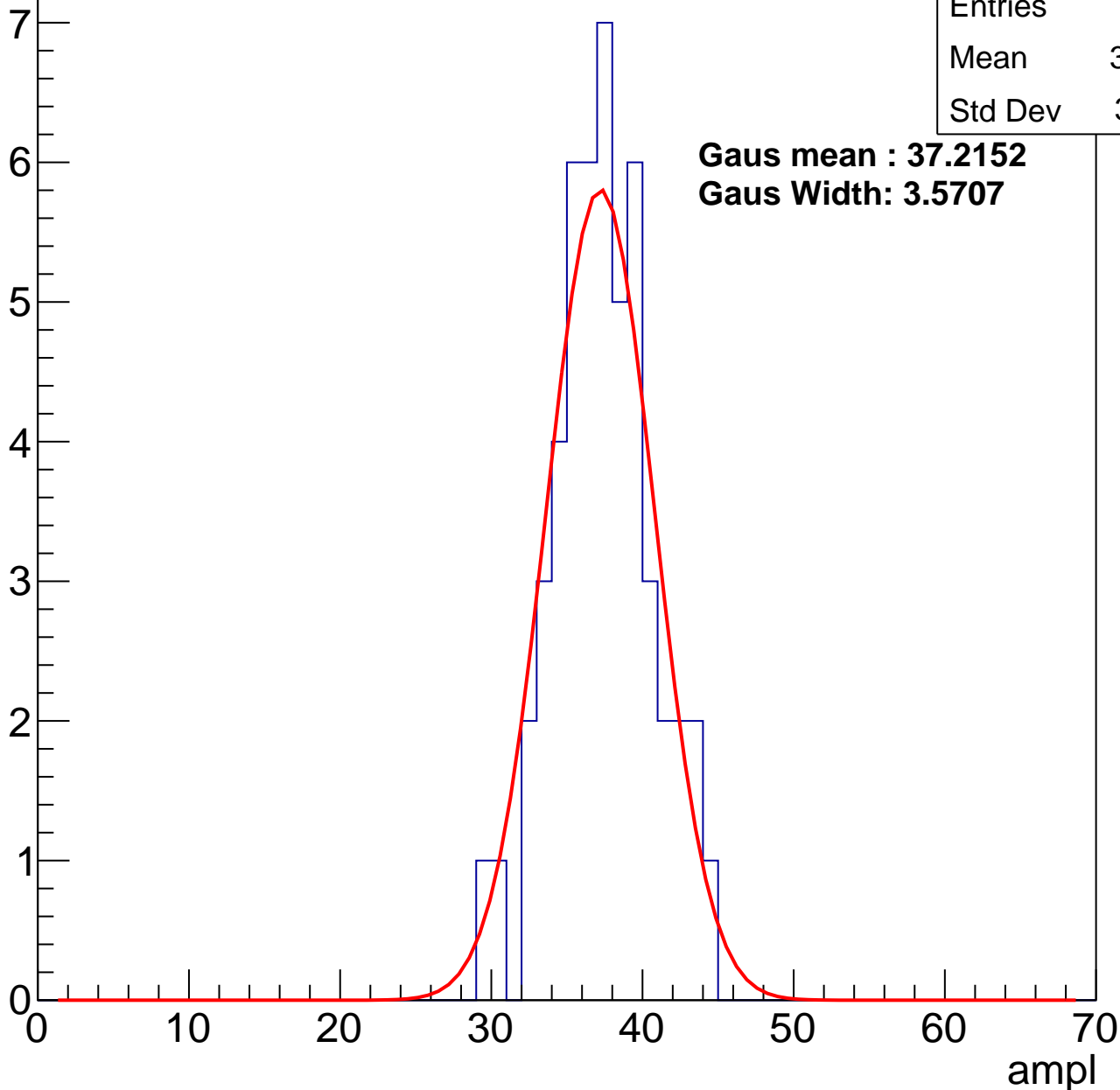
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	36.92
Std Dev	3.241

**Gaus mean : 37.2152**

**Gaus Width: 3.5707**



# B1L103S, U2-ch25, adc2

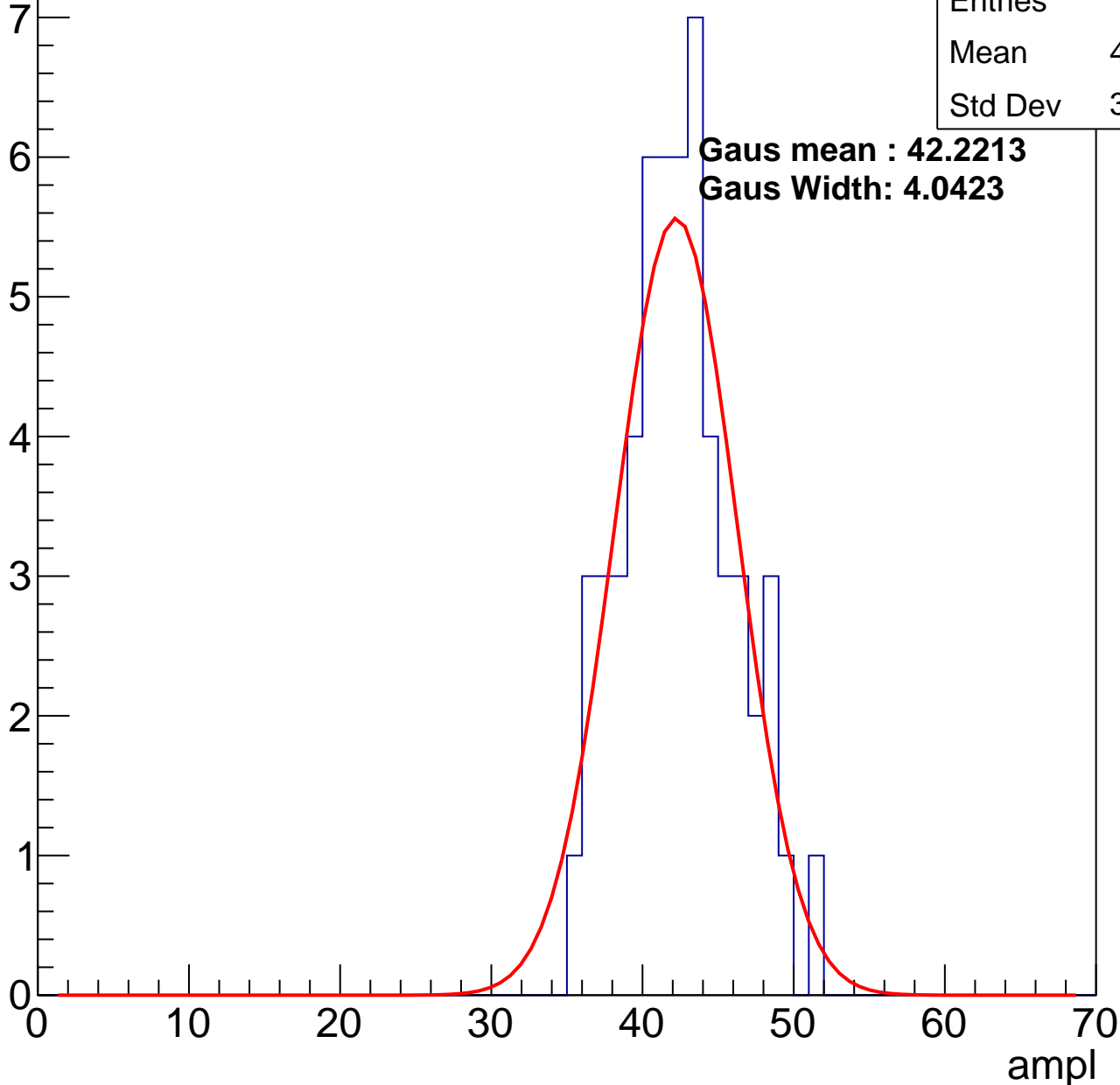
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	41.96
Std Dev	3.615

**Gaus mean : 42.2213**

**Gaus Width: 4.0423**

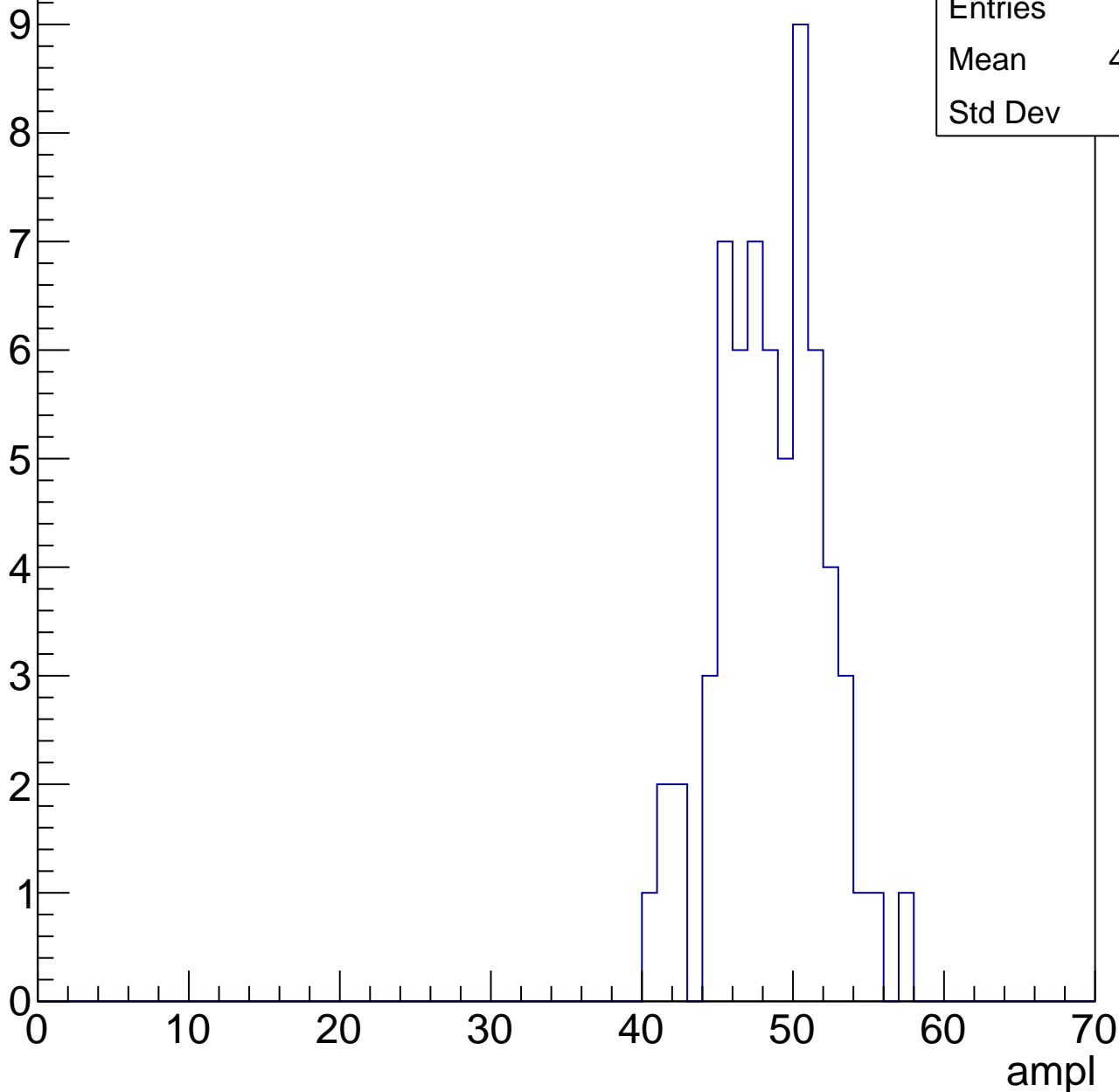


# B1L103S, U2-ch25, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

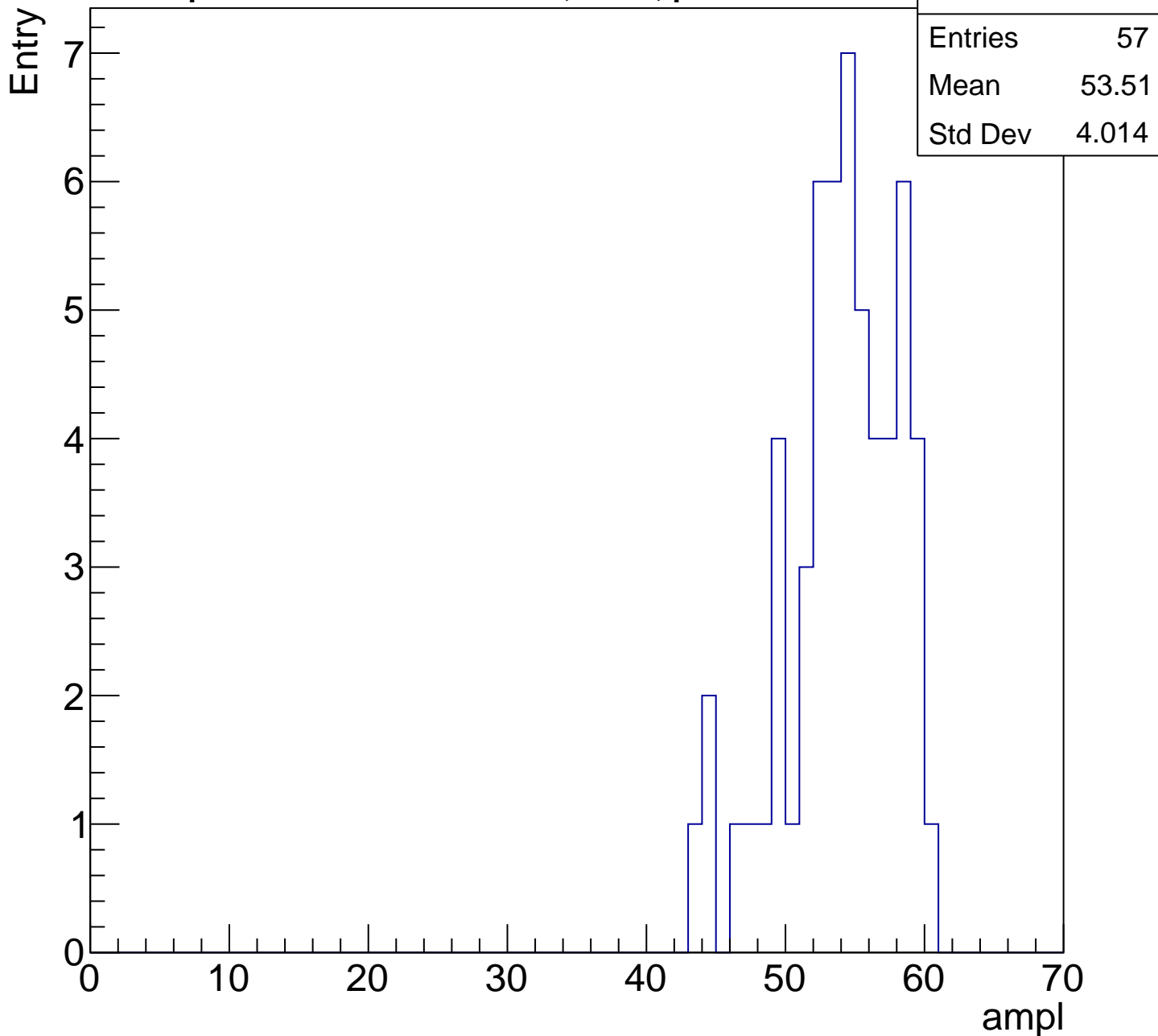
Entry

Entries	64
Mean	48.12
Std Dev	3.48



# B1L103S, U2-ch25, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U2-ch25, adc5

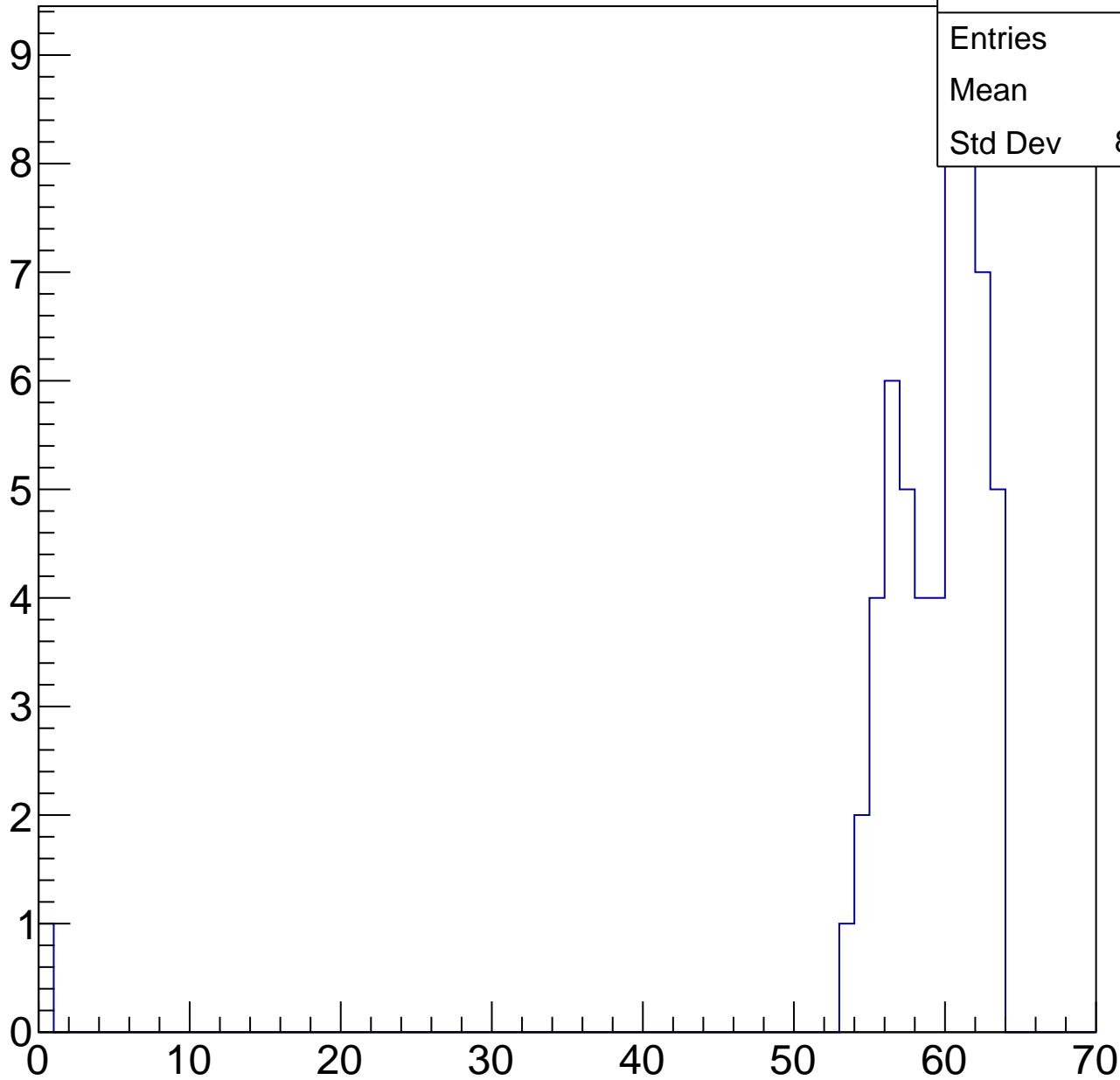
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	56
Mean	58
Std Dev	8.281

ampl

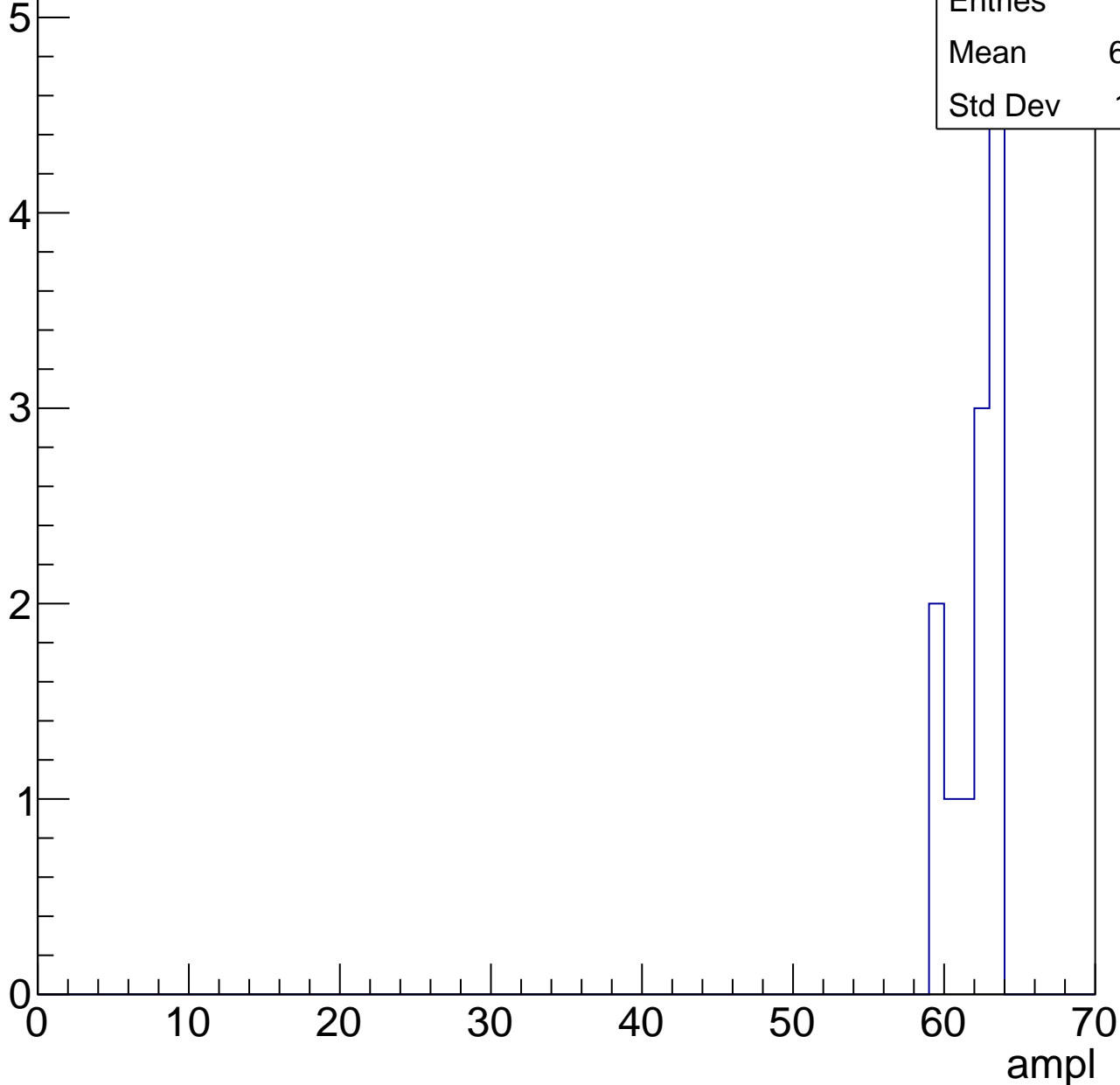


# B1L103S, U2-ch25, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	12
Mean	61.67
Std Dev	1.491





# B1L103S, U2-ch25, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U2-ch26, adc0

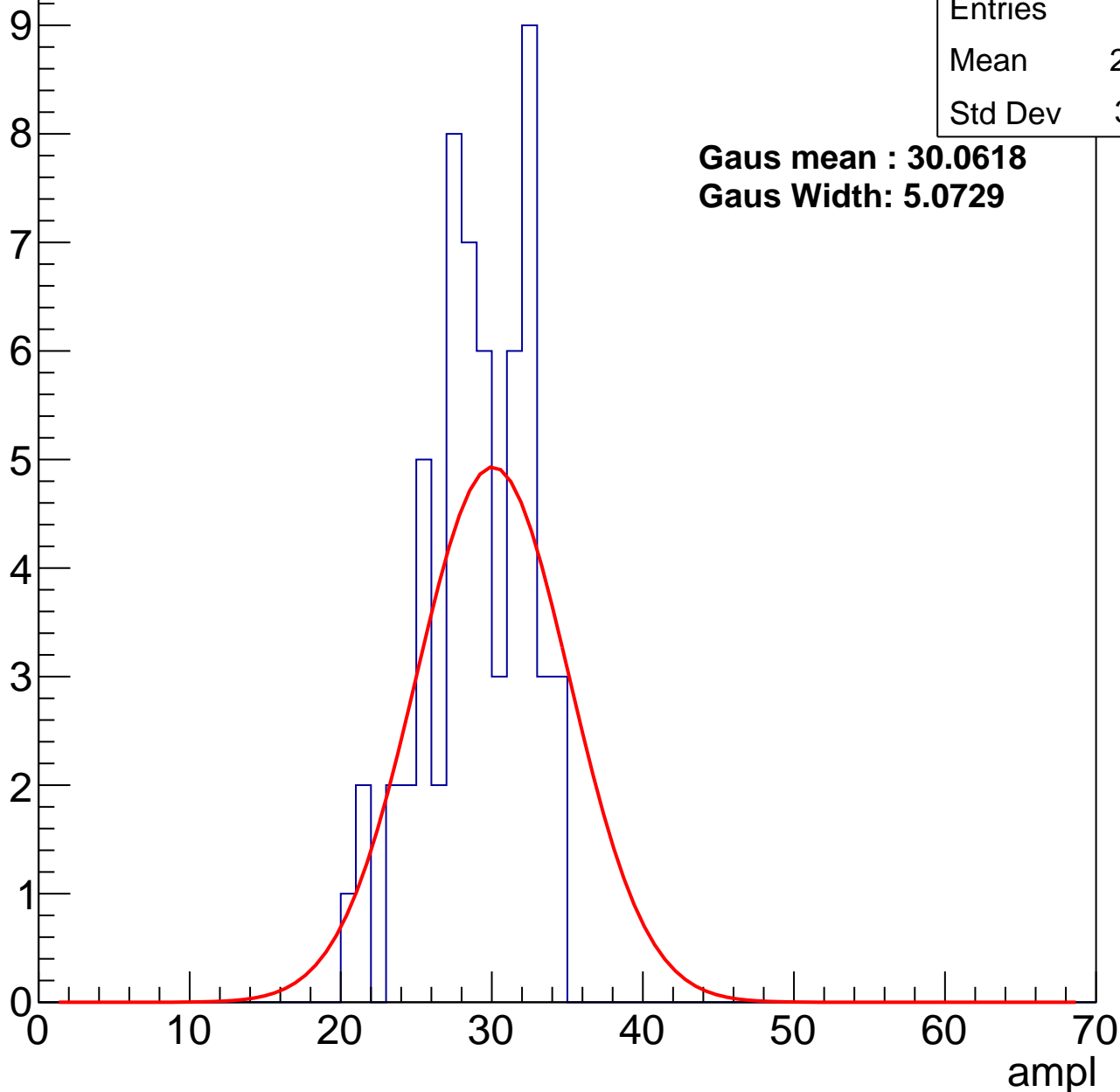
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	28.54
Std Dev	3.411

**Gaus mean : 30.0618**

**Gaus Width: 5.0729**



# B1L103S, U2-ch26, adc1

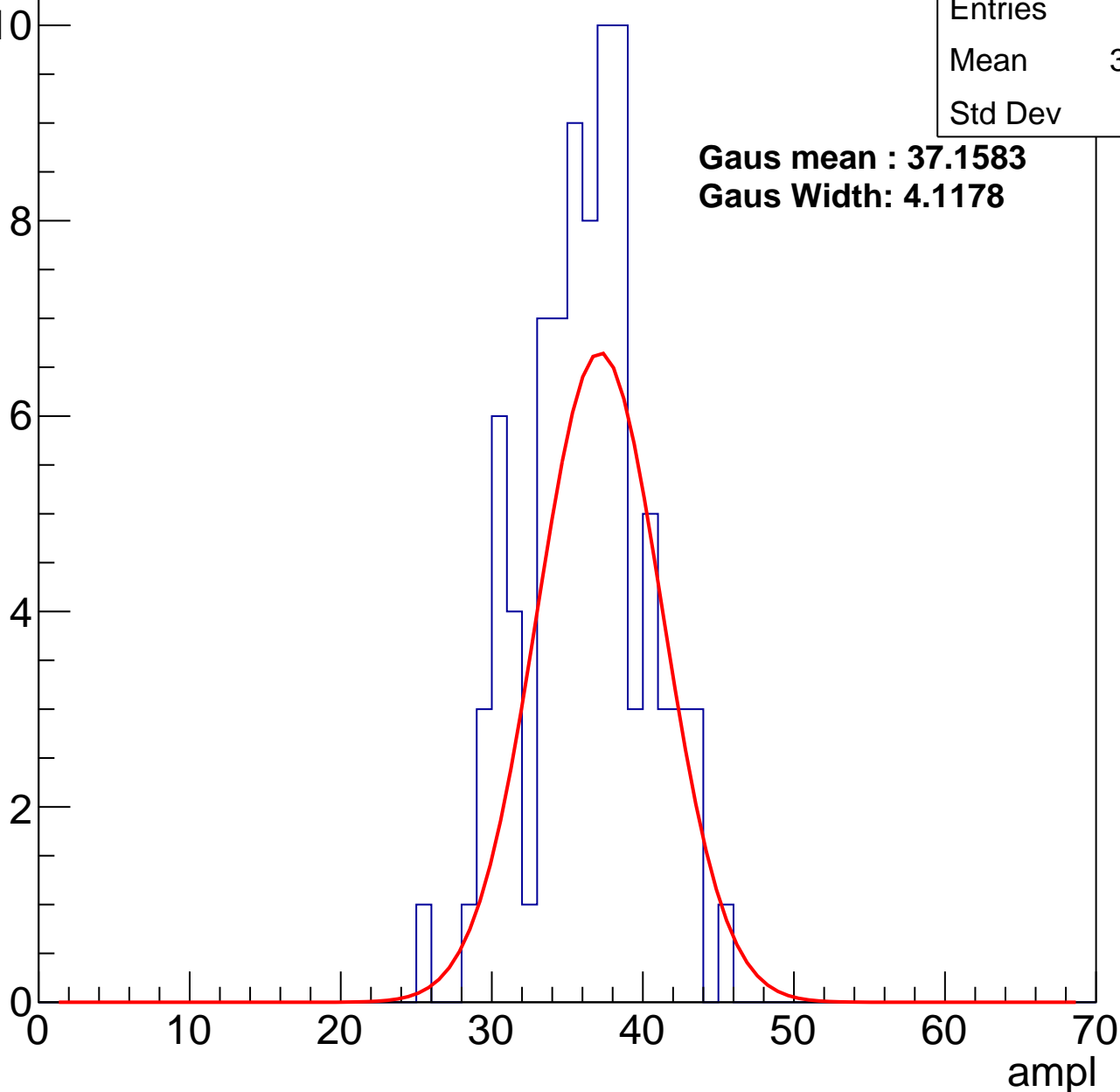
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	85
Mean	35.74
Std Dev	3.95

**Gaus mean : 37.1583**

**Gaus Width: 4.1178**



# B1L103S, U2-ch26, adc2

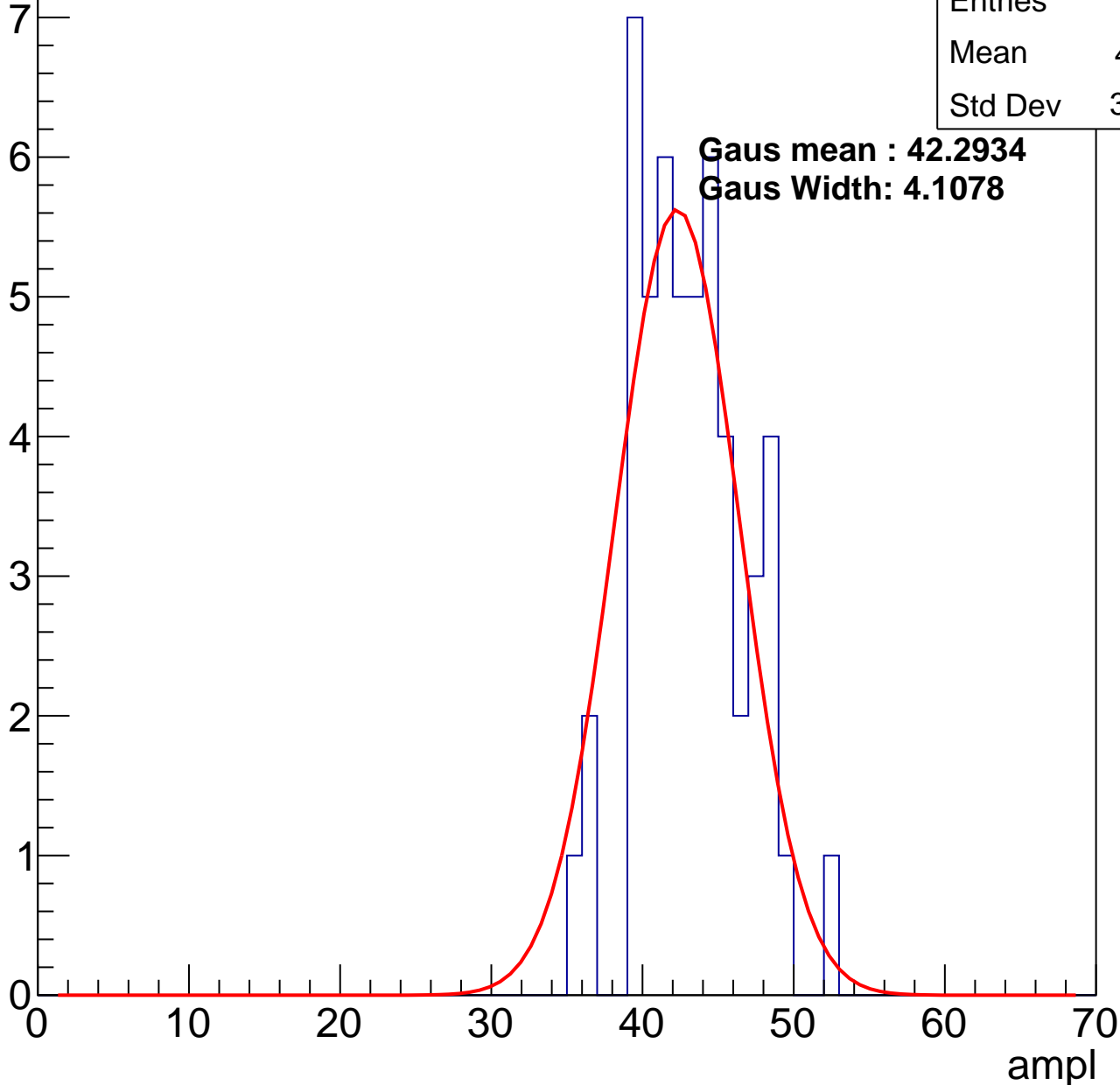
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	42.71
Std Dev	3.532

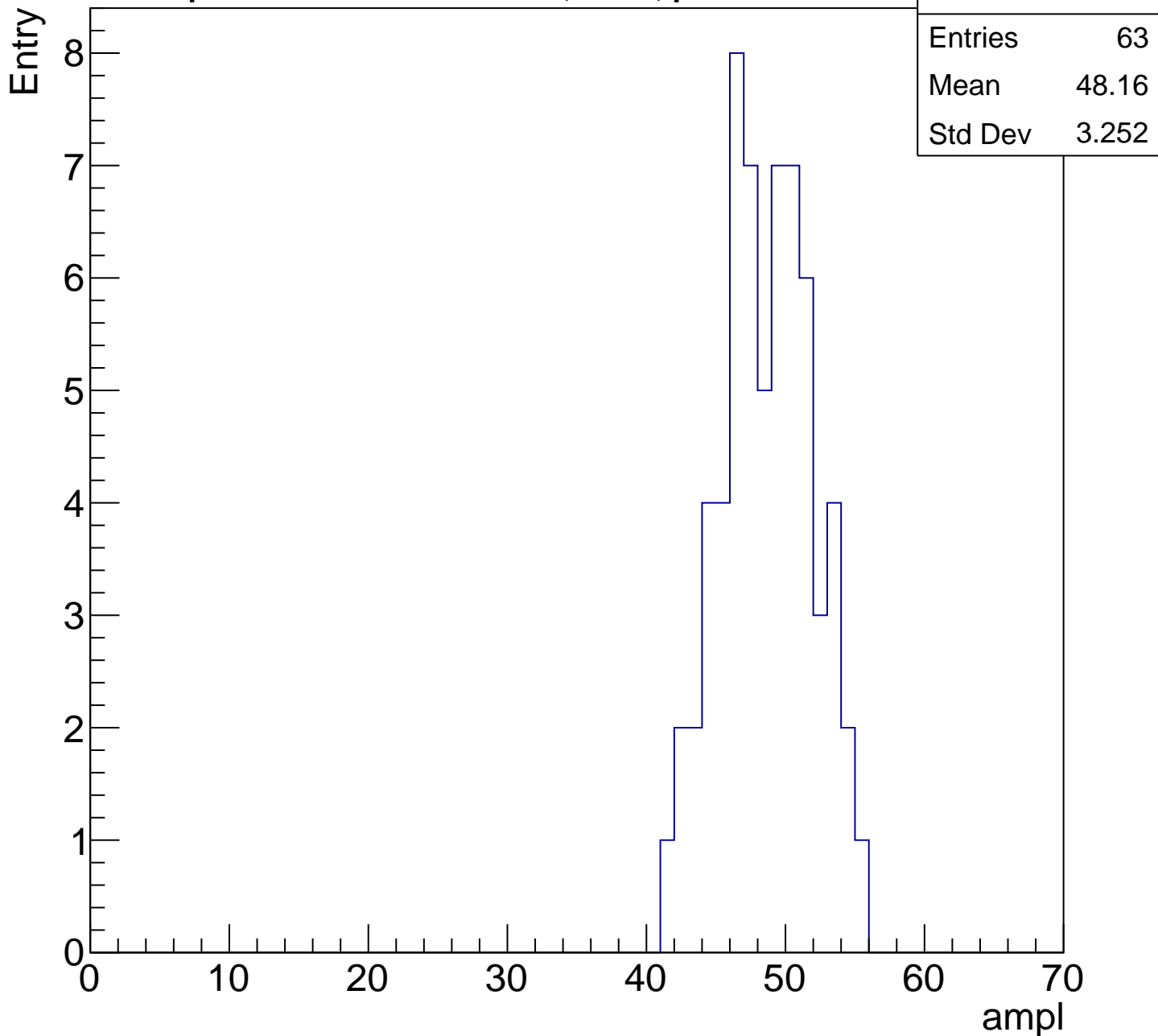
**Gaus mean : 42.2934**

**Gaus Width: 4.1078**



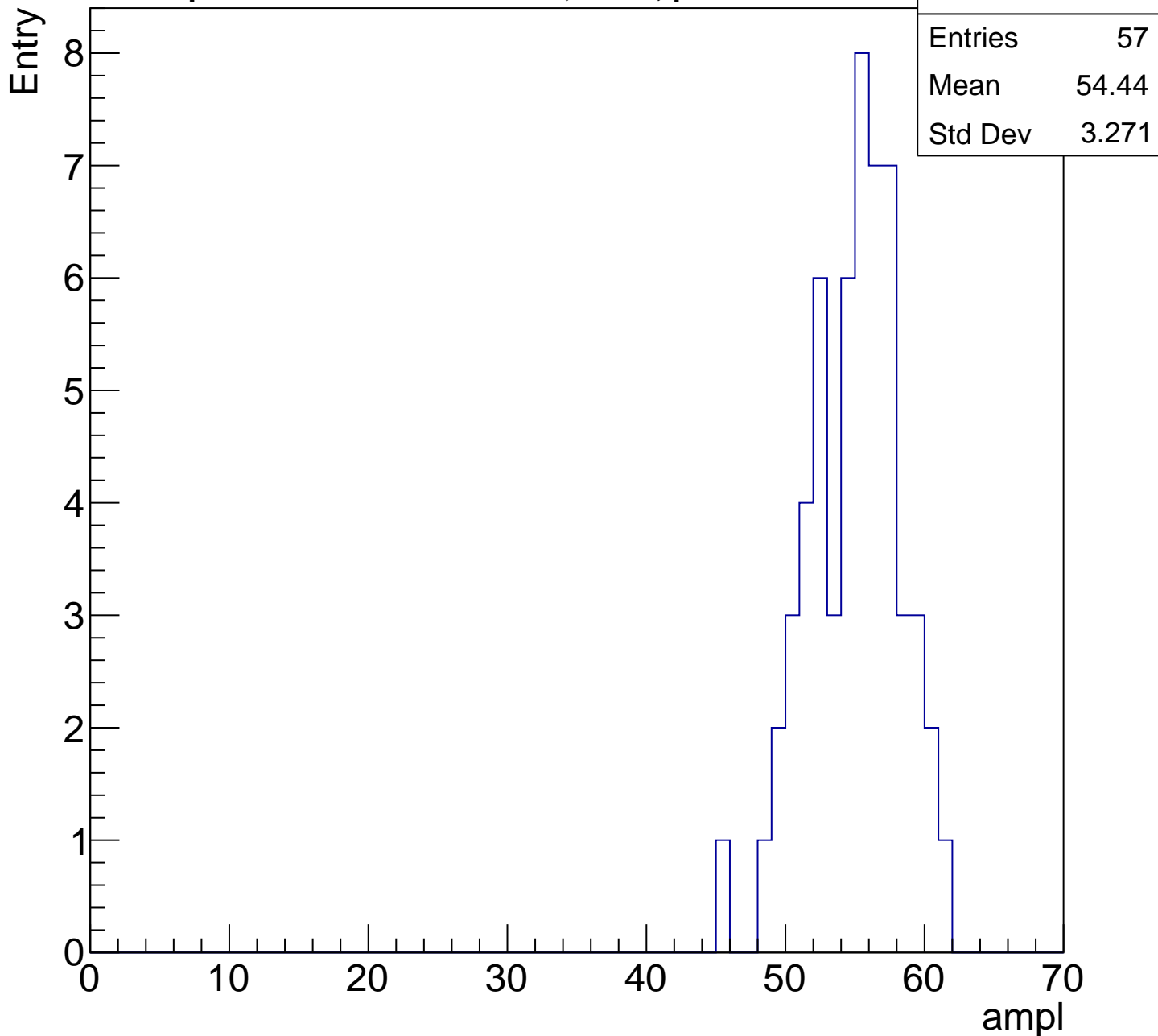
# B1L103S, U2-ch26, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U2-ch26, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

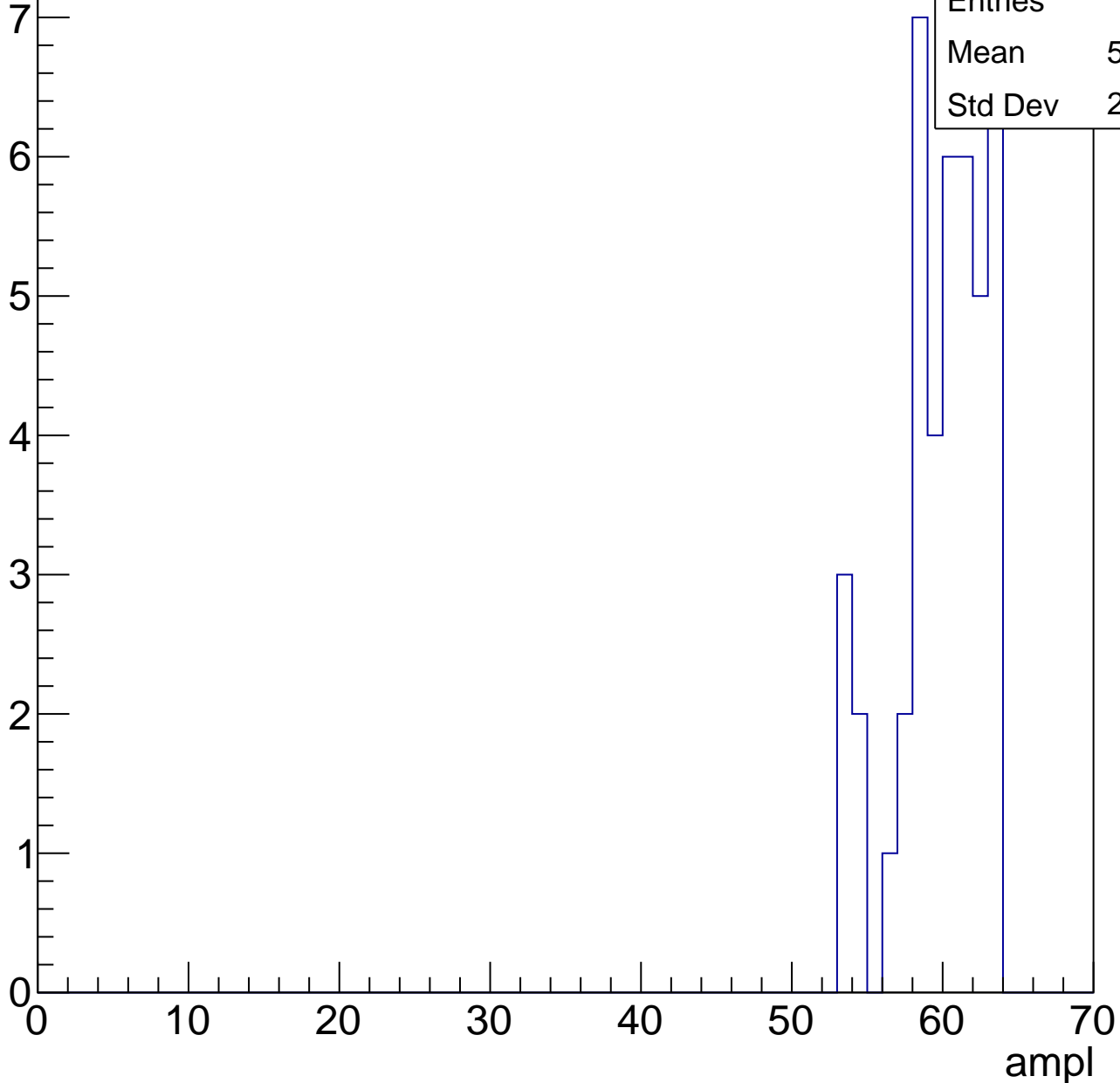


# B1L103S, U2-ch26, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	43
Mean	59.44
Std Dev	2.896

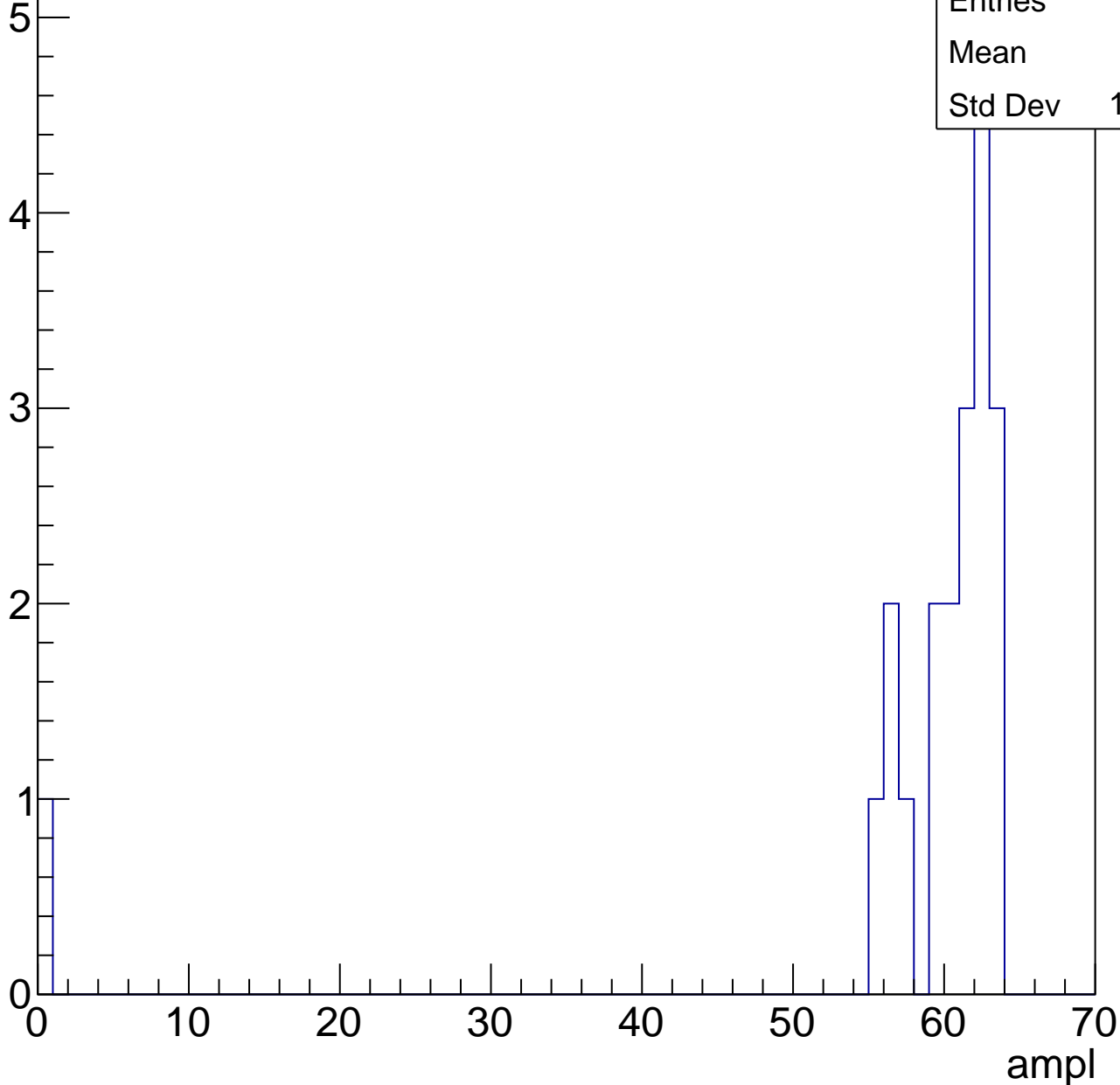


# B1L103S, U2-ch26, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	20
Mean	57.2
Std Dev	13.34

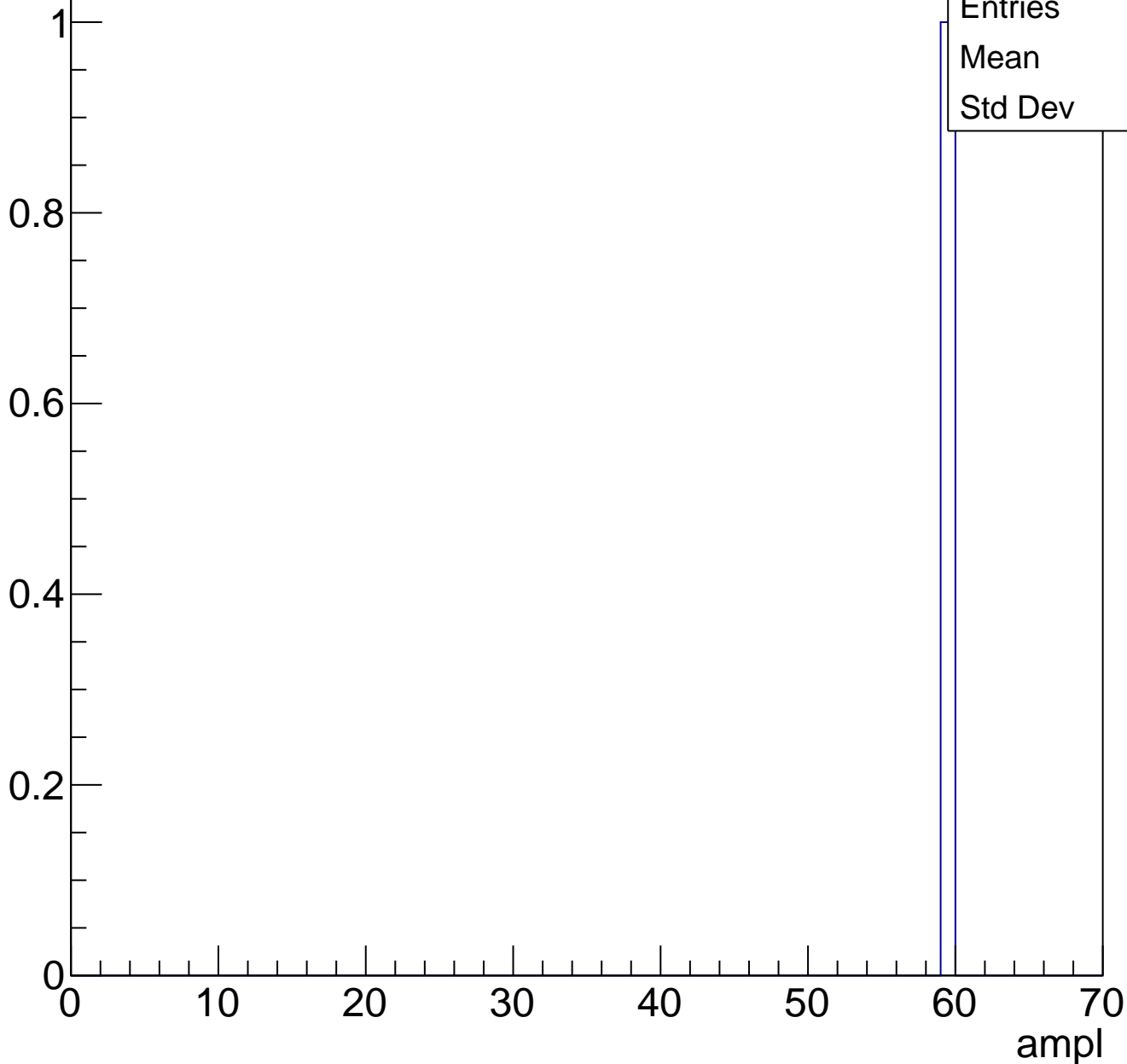




# B1L103S, U2-ch26, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



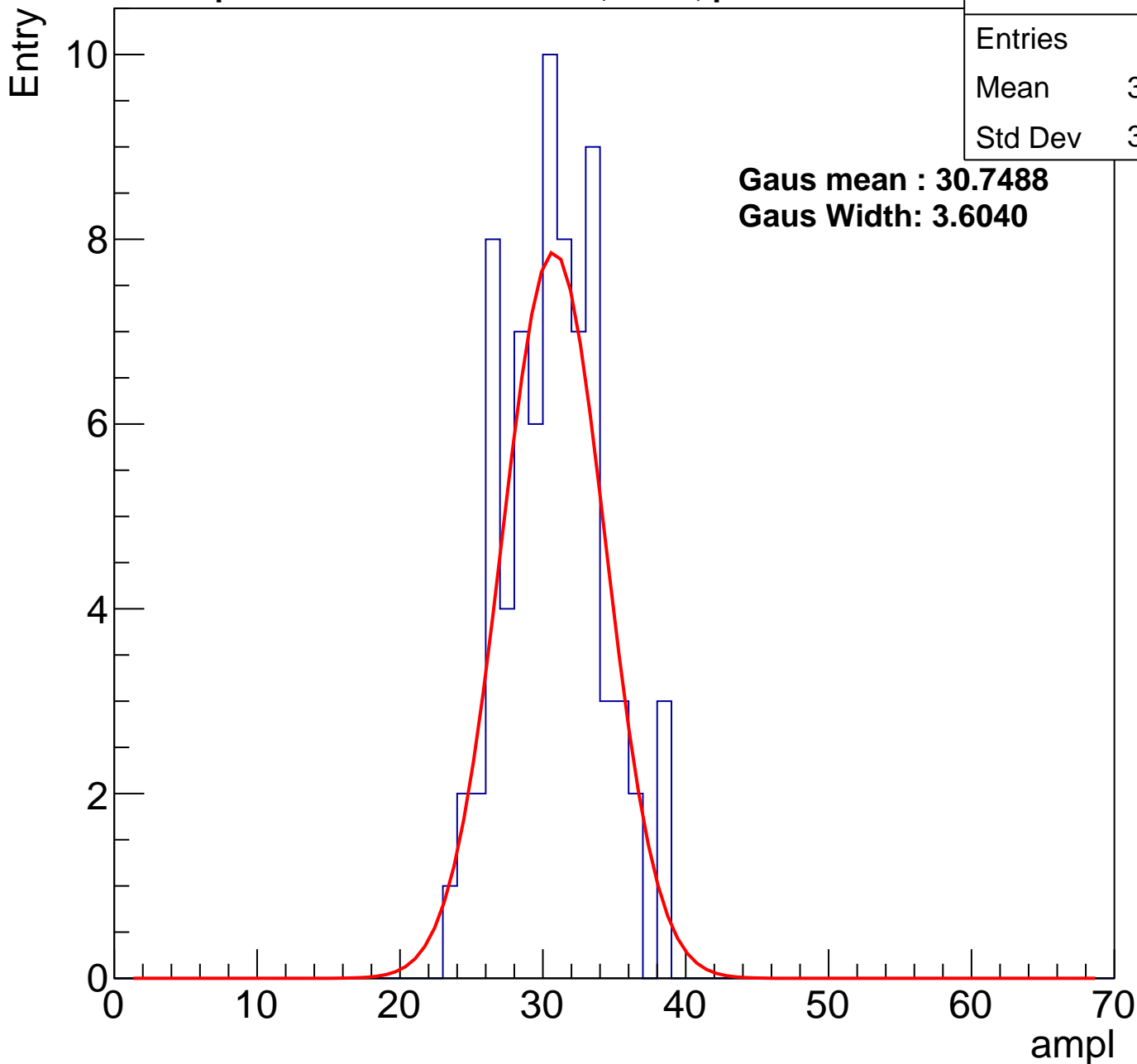
# B1L103S, U2-ch27, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	75
Mean	30.25
Std Dev	3.402

**Gaus mean : 30.7488**

**Gaus Width: 3.6040**



# B1L103S, U2-ch27, adc1

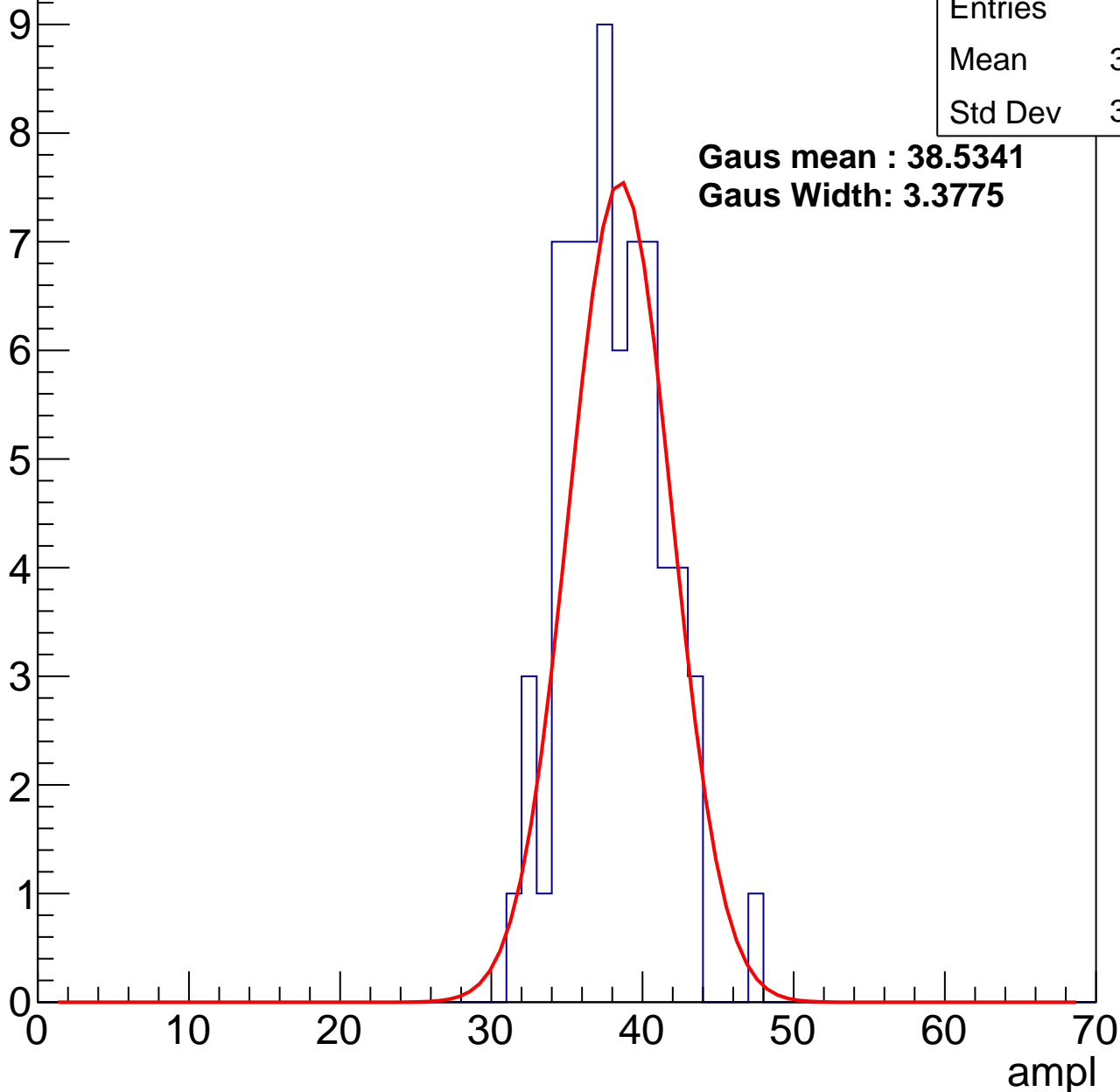
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	37.57
Std Dev	3.168

**Gaus mean : 38.5341**

**Gaus Width: 3.3775**

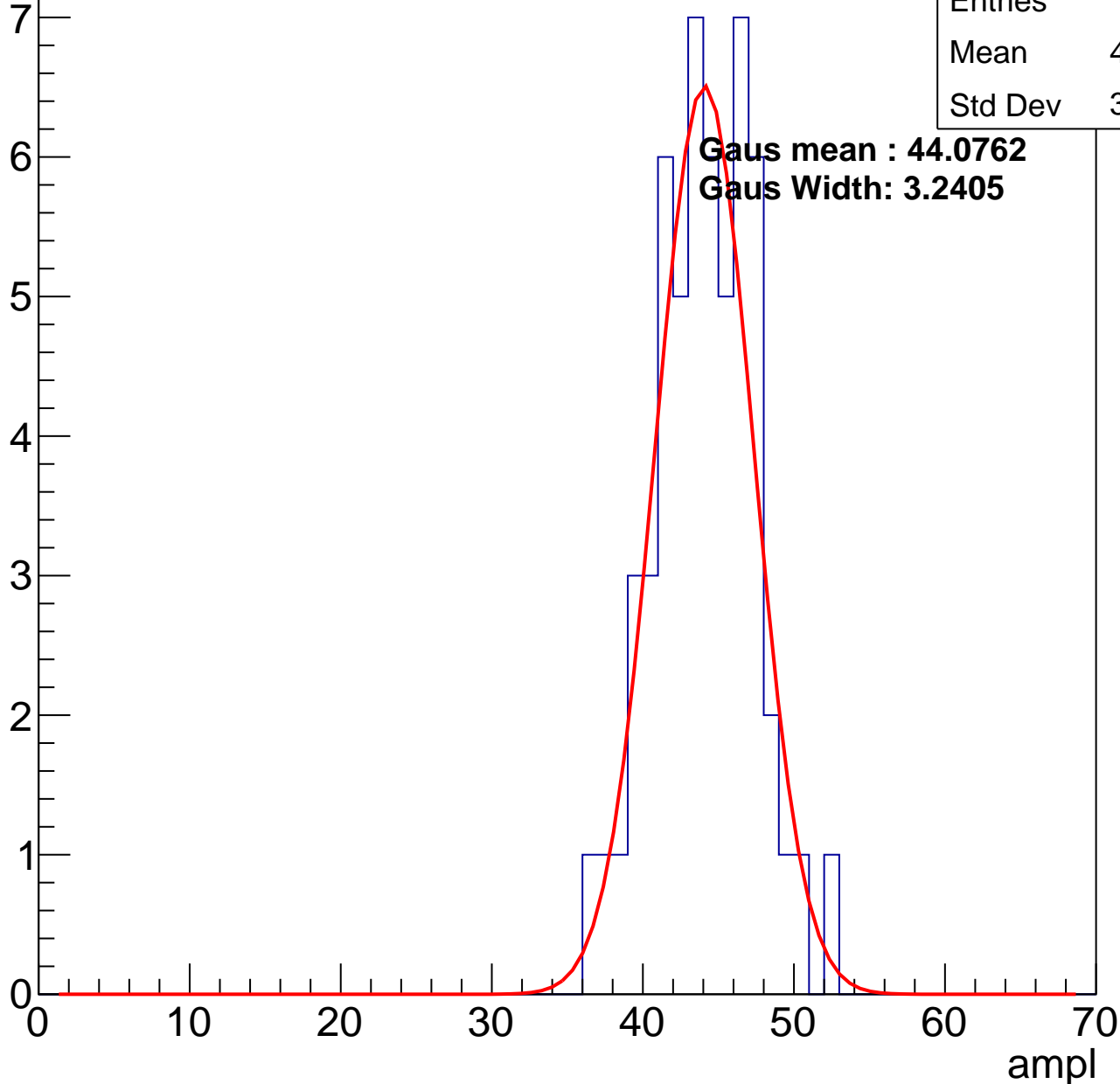


# B1L103S, U2-ch27, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	43.66
Std Dev	3.247

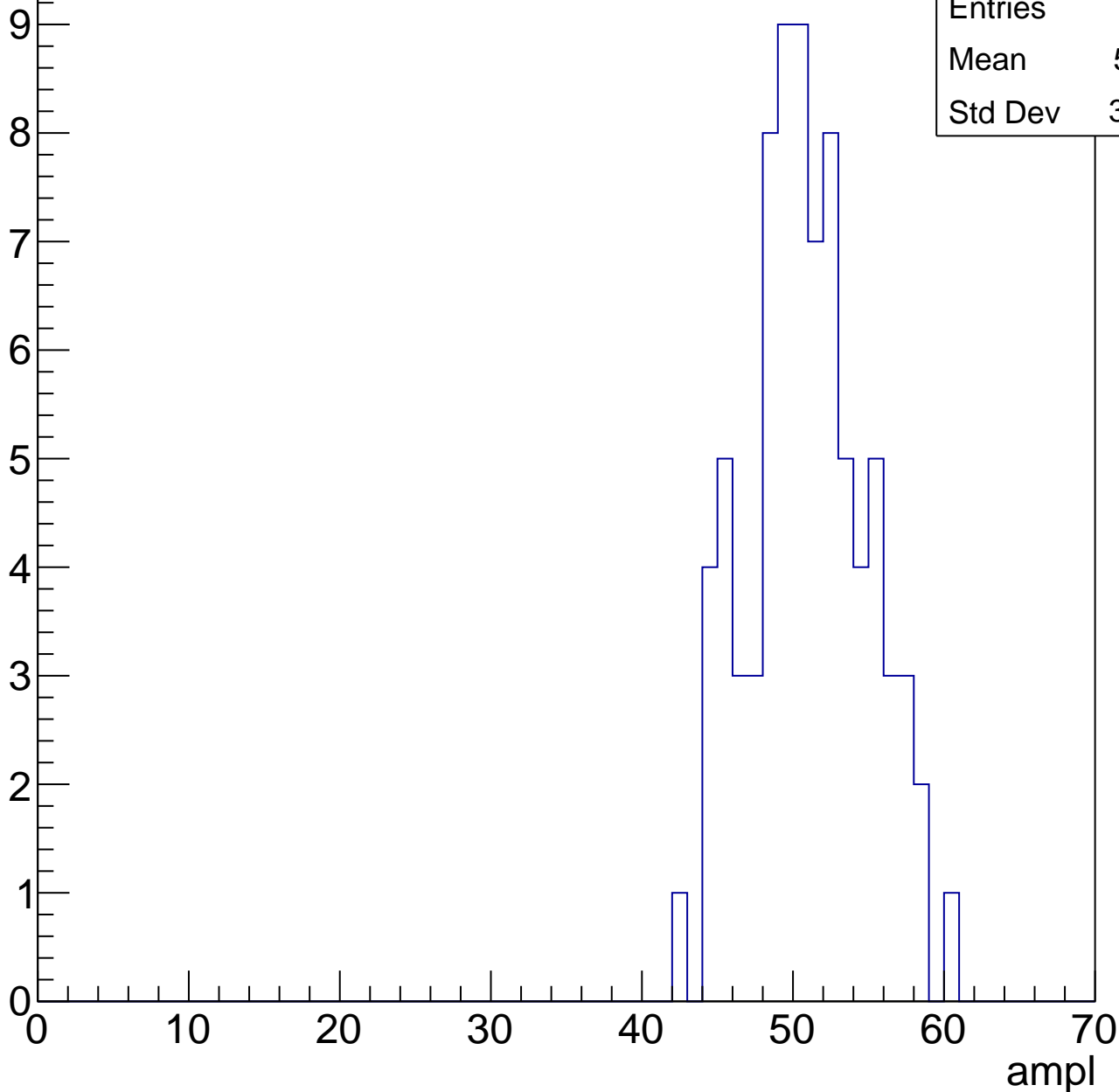


# B1L103S, U2-ch27, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	80
Mean	50.51
Std Dev	3.847

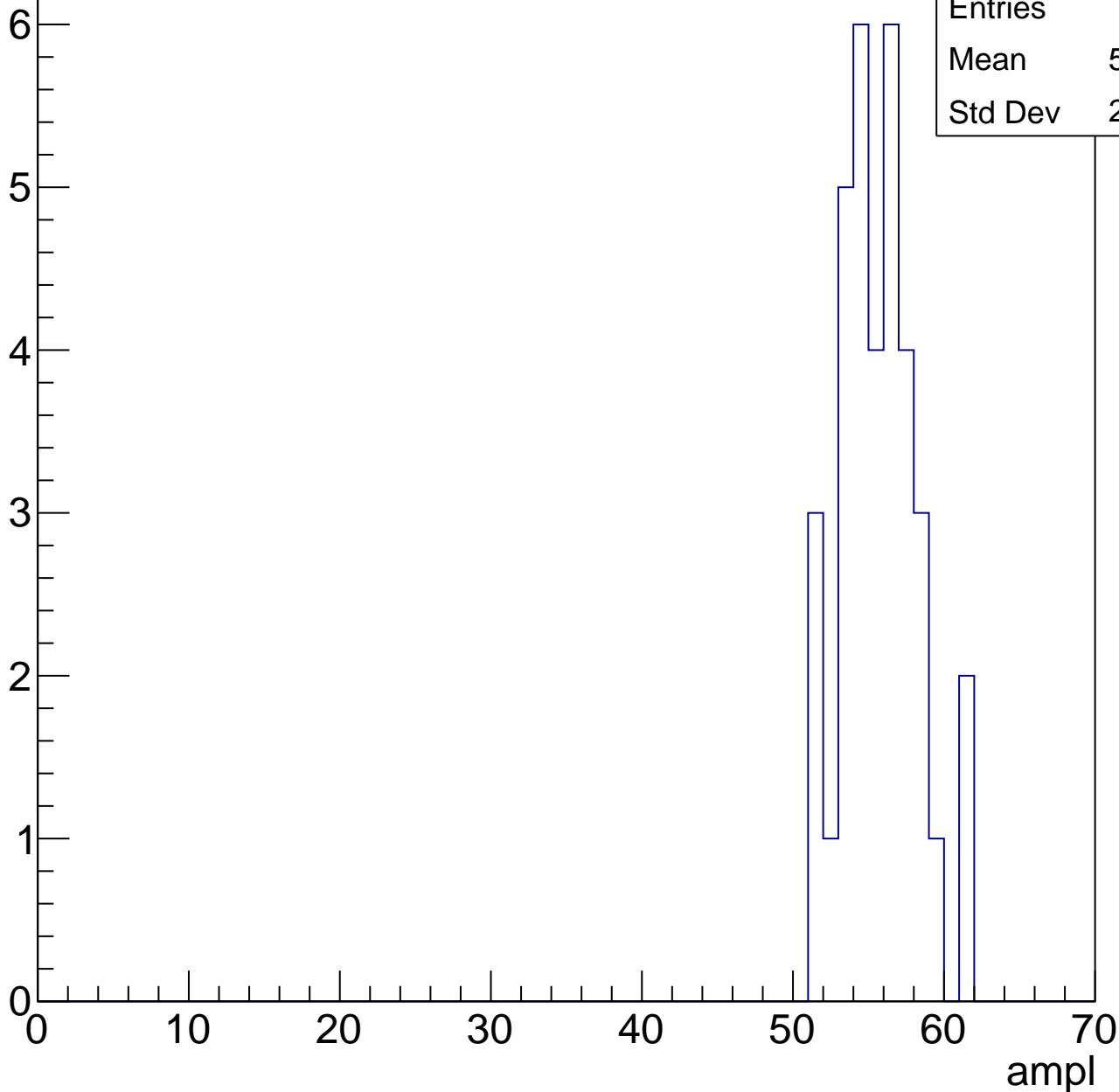


# B1L103S, U2-ch27, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	35
Mean	55.23
Std Dev	2.497

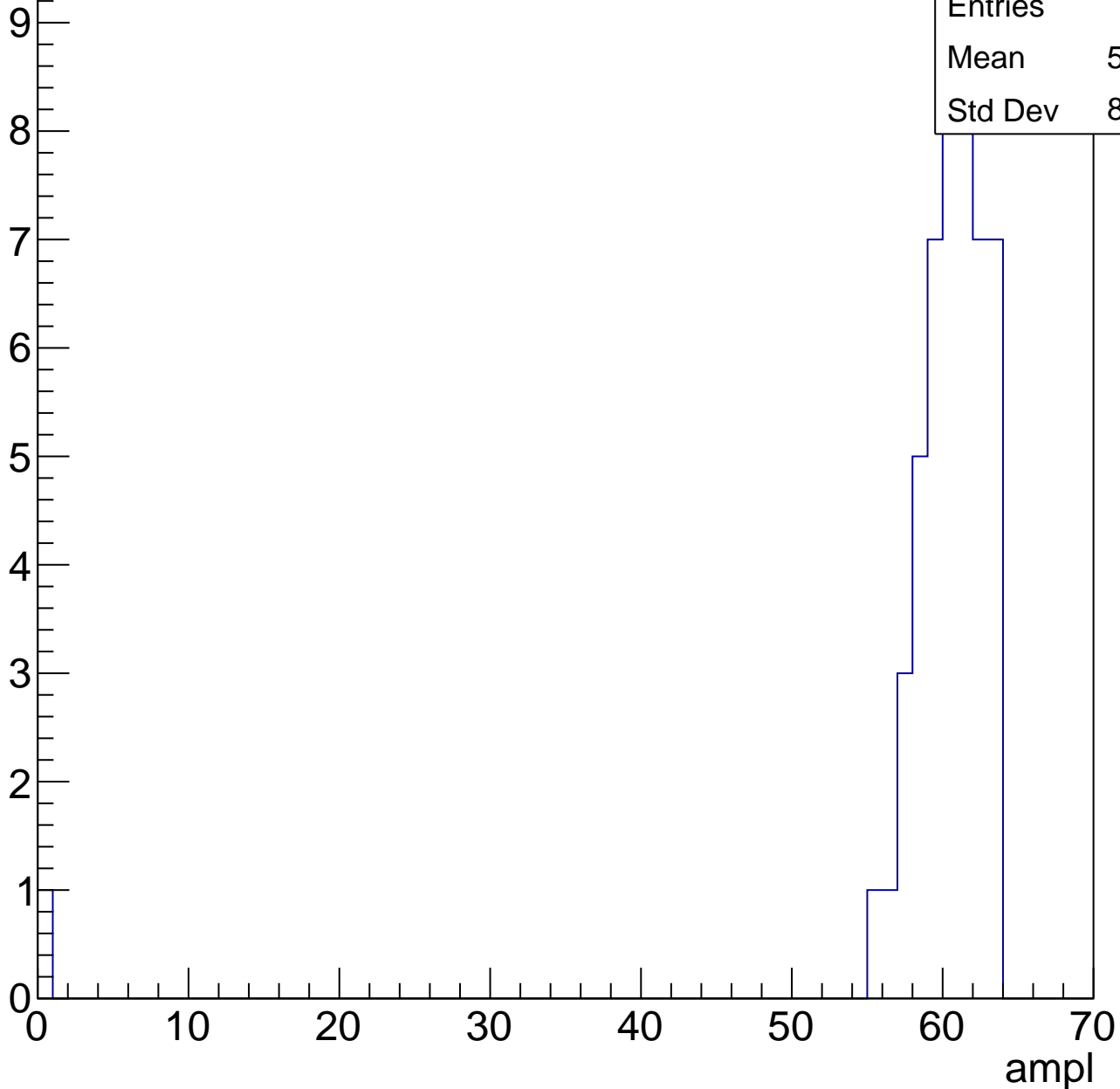


# B1L103S, U2-ch27, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

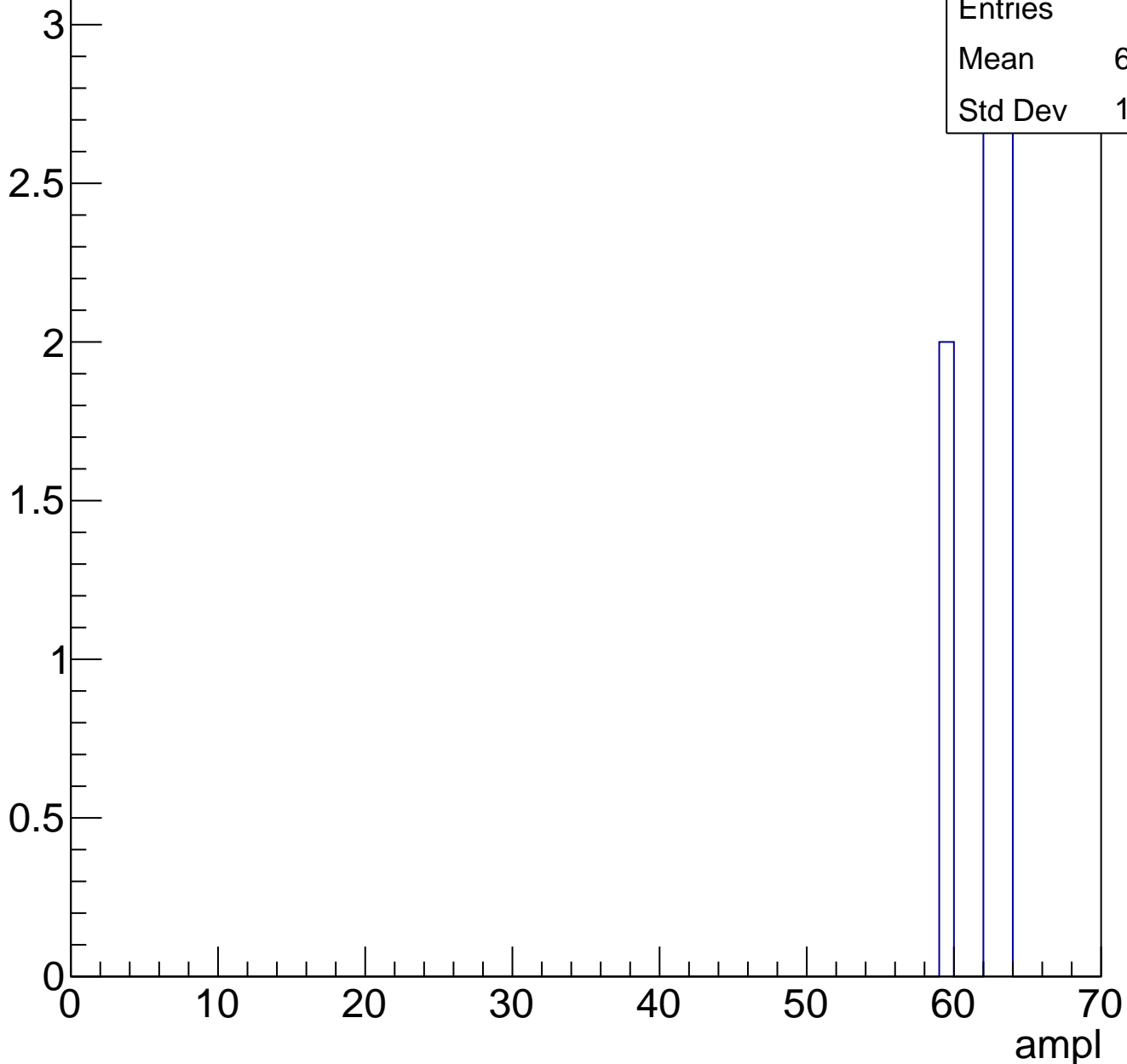
Entries	49
Mean	58.94
Std Dev	8.735



# B1L103S, U2-ch27, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U2-ch27, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch28, adc0

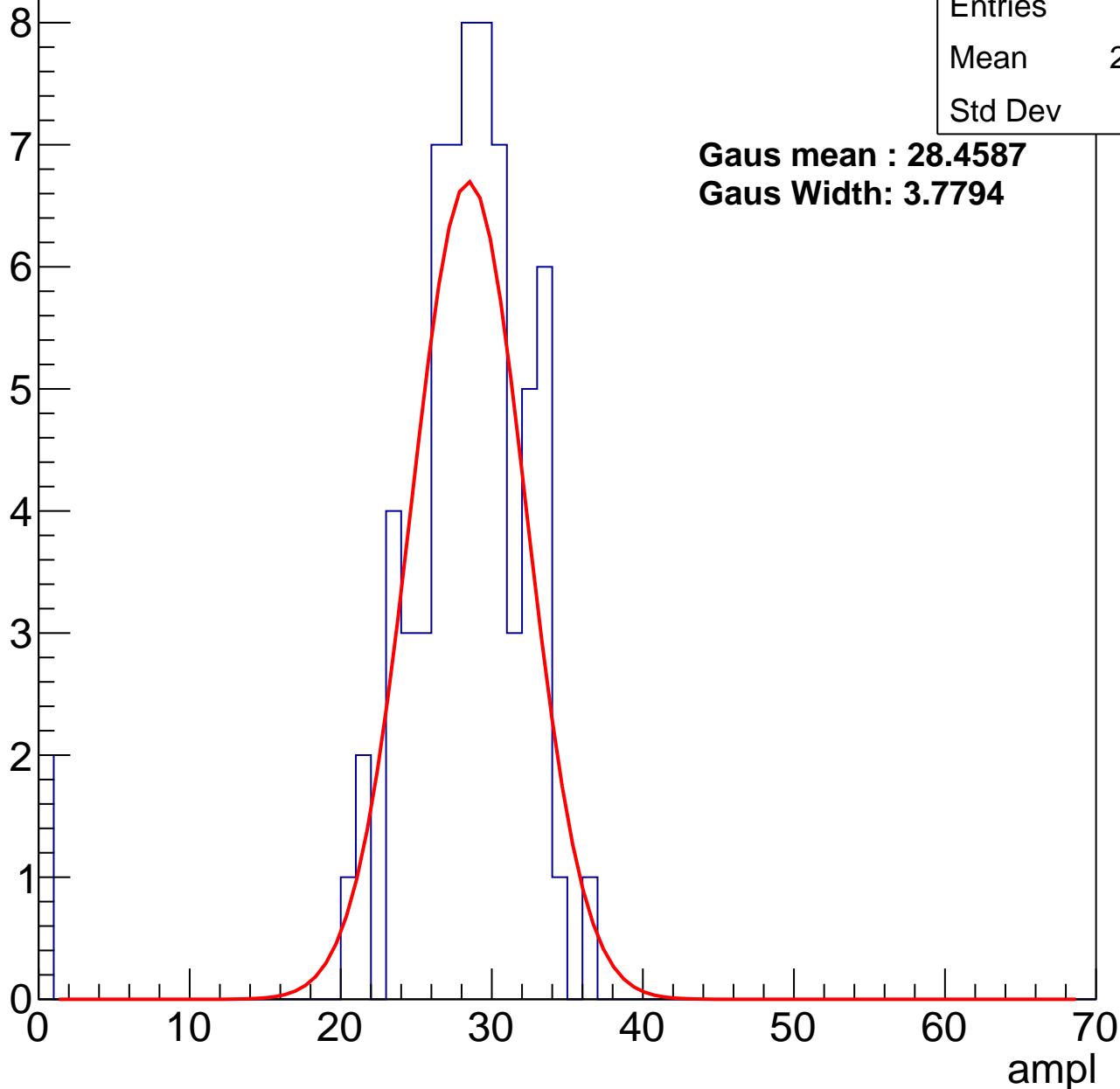
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	27.34
Std Dev	5.82

**Gaus mean : 28.4587**

**Gaus Width: 3.7794**



# B1L103S, U2-ch28, adc1

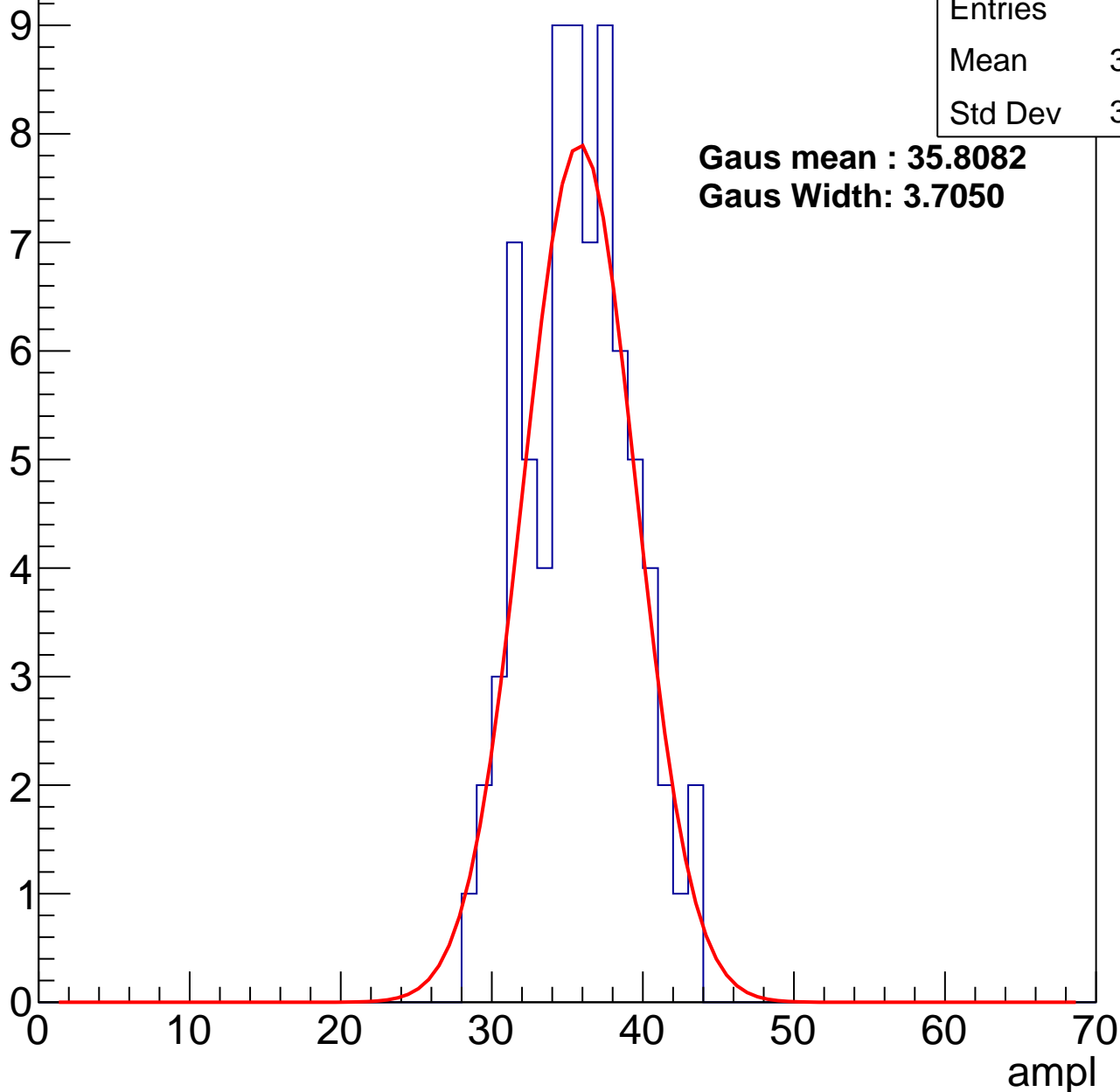
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	35.32
Std Dev	3.434

**Gaus mean : 35.8082**

**Gaus Width: 3.7050**



# B1L103S, U2-ch28, adc2

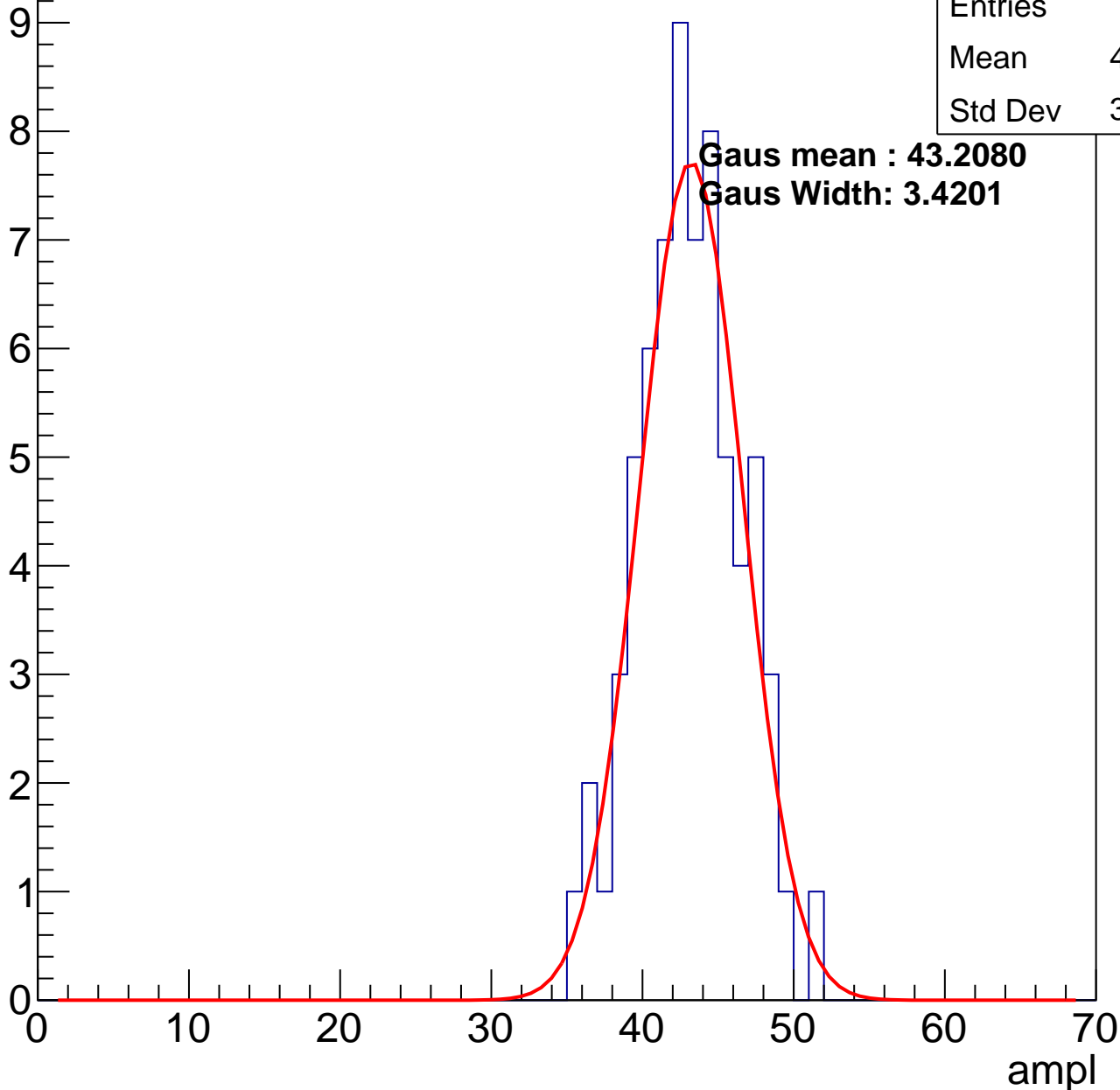
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	42.63
Std Dev	3.329

**Gaus mean : 43.2080**

**Gaus Width: 3.4201**

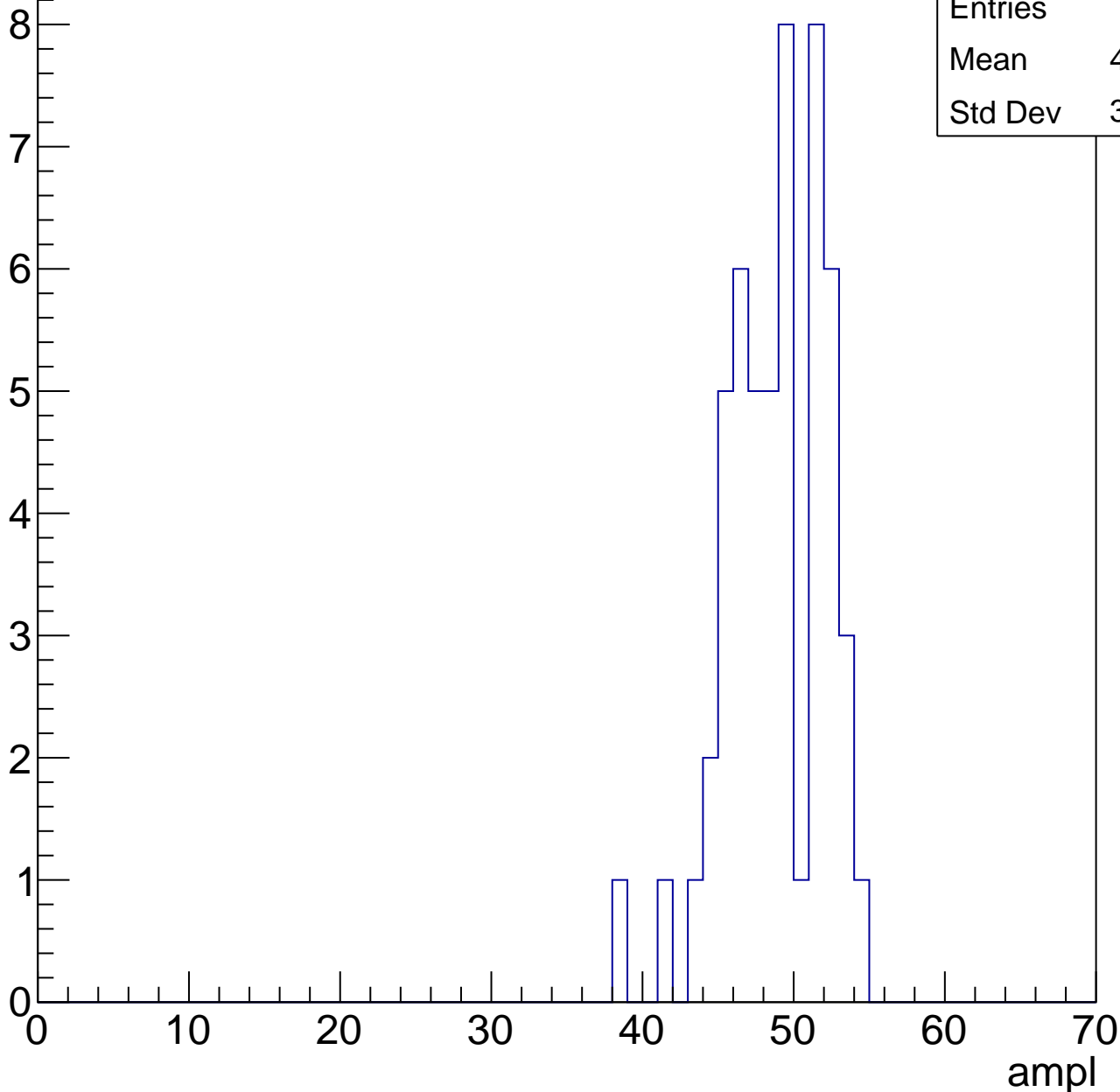


# B1L103S, U2-ch28, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	48.32
Std Dev	3.267

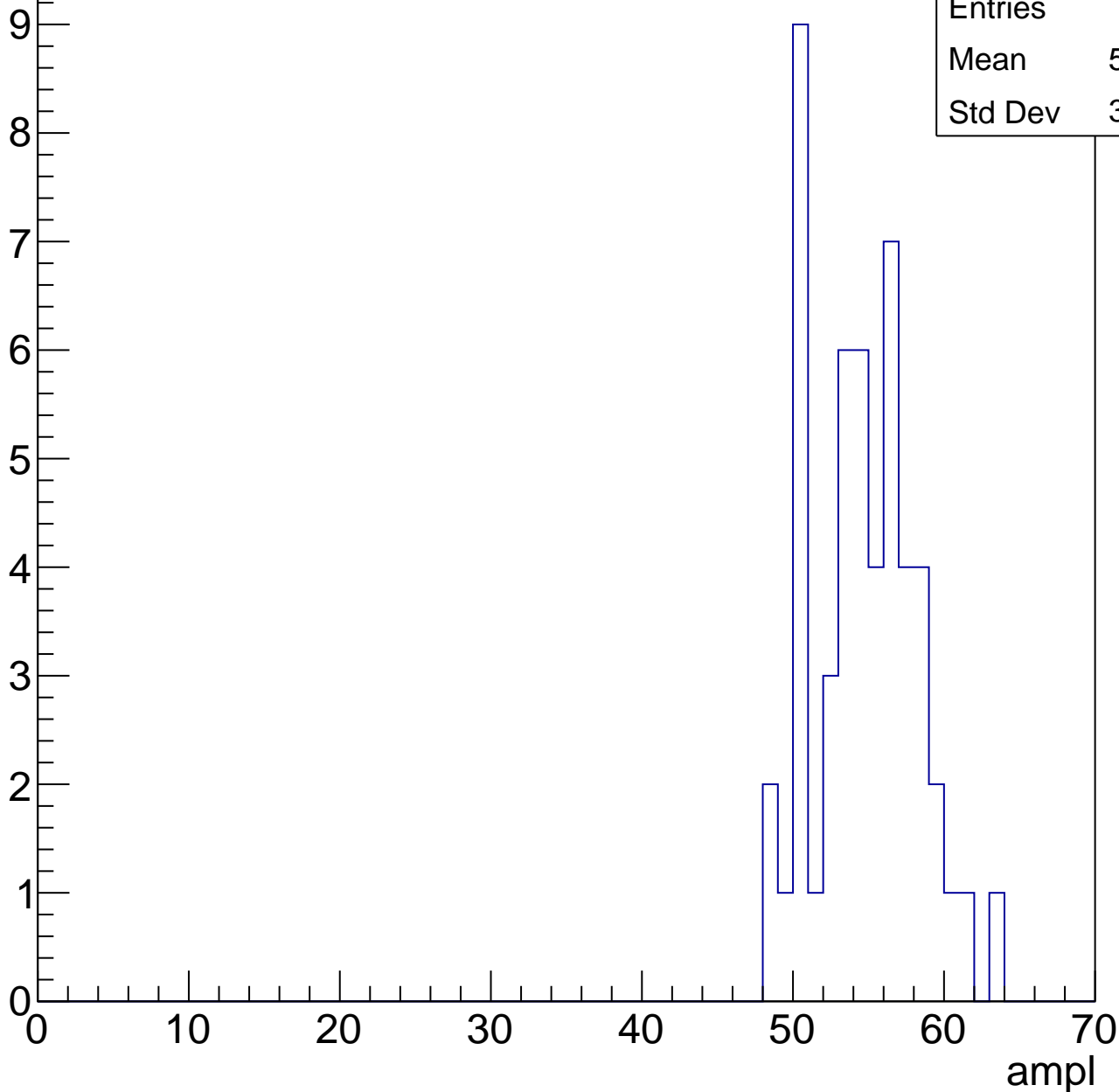


# B1L103S, U2-ch28, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

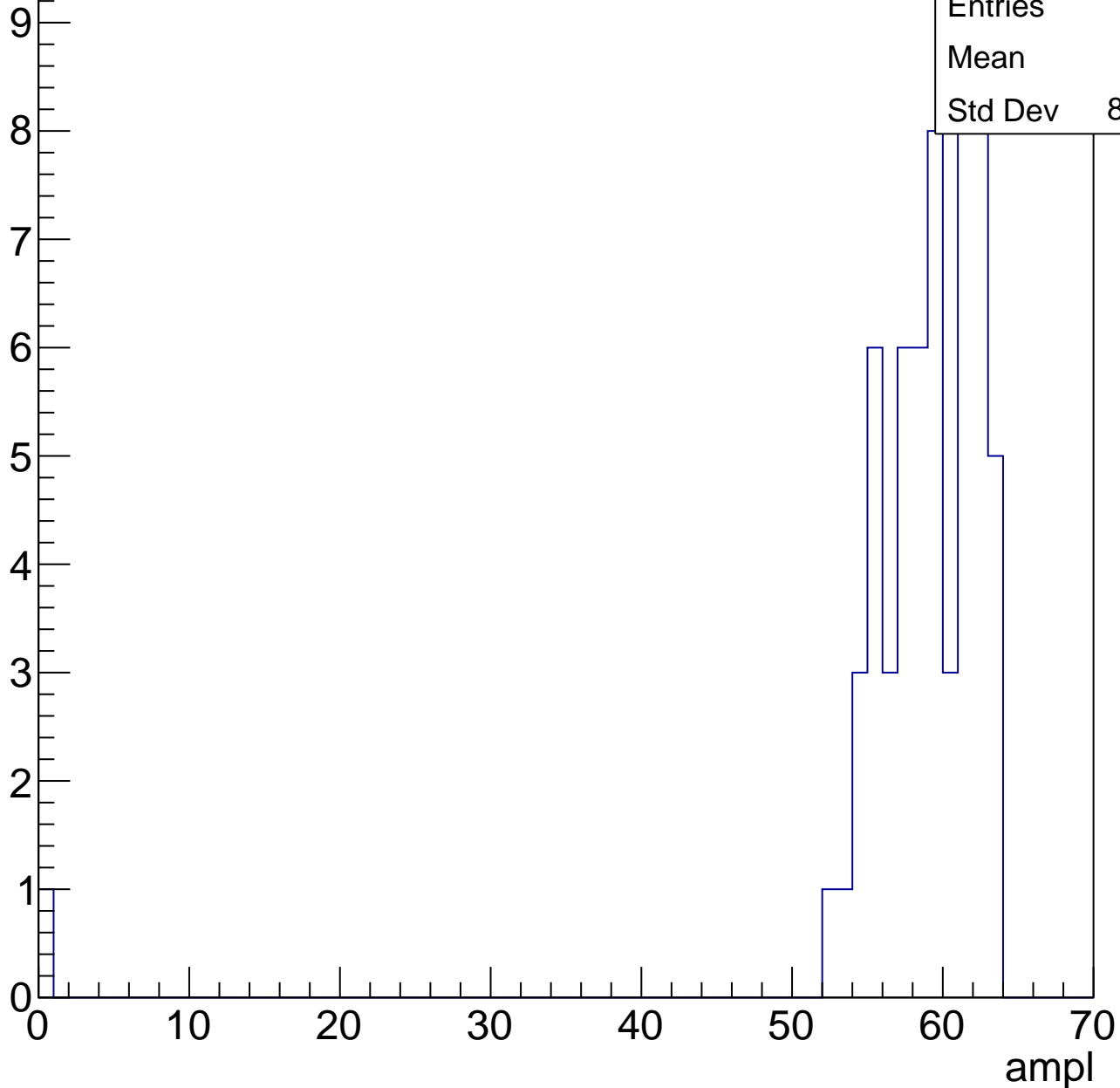
Entries	52
Mean	54.19
Std Dev	3.436



# B1L103S, U2-ch28, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

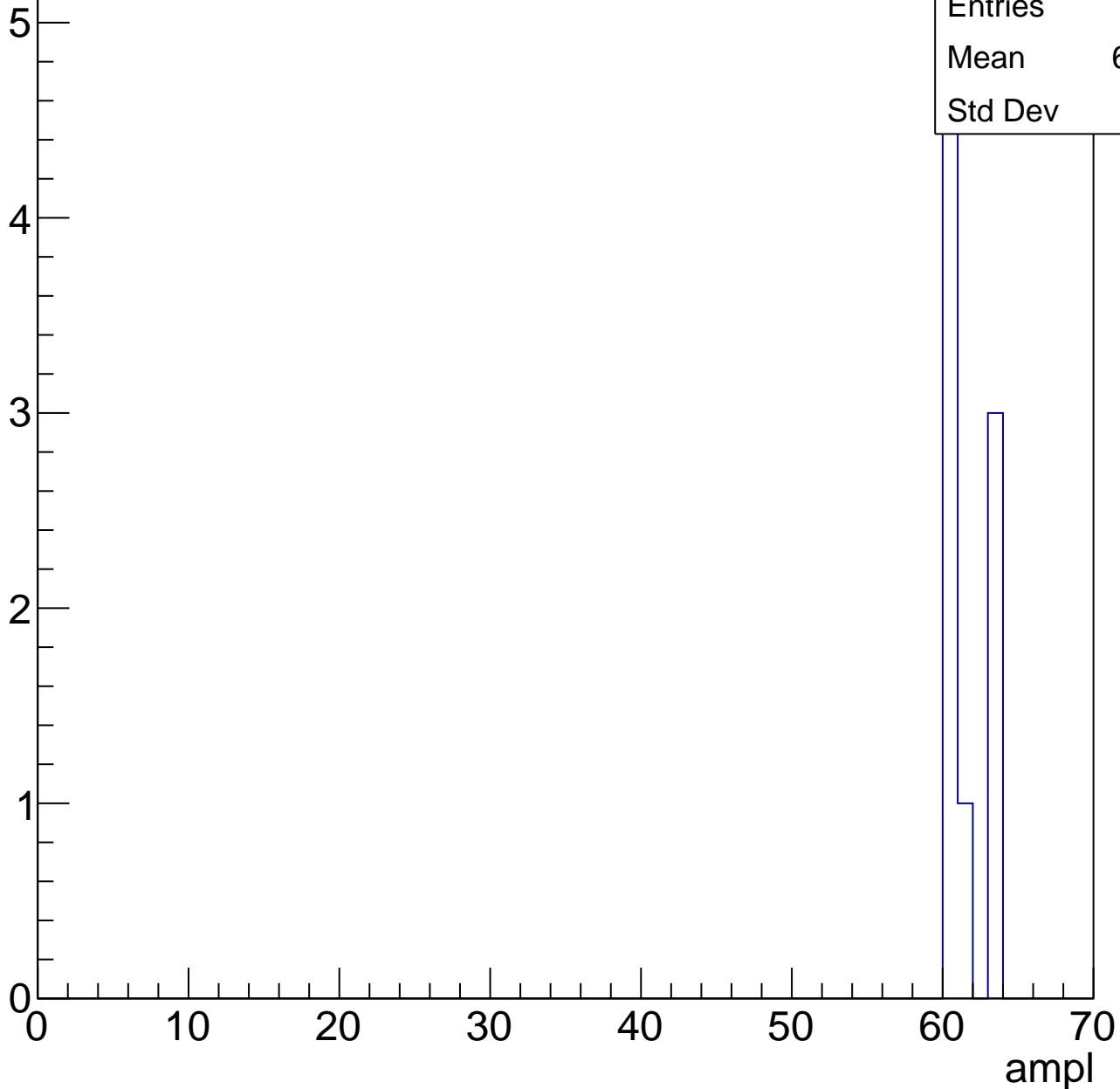


# B1L103S, U2-ch28, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	9
Mean	61.11
Std Dev	1.37

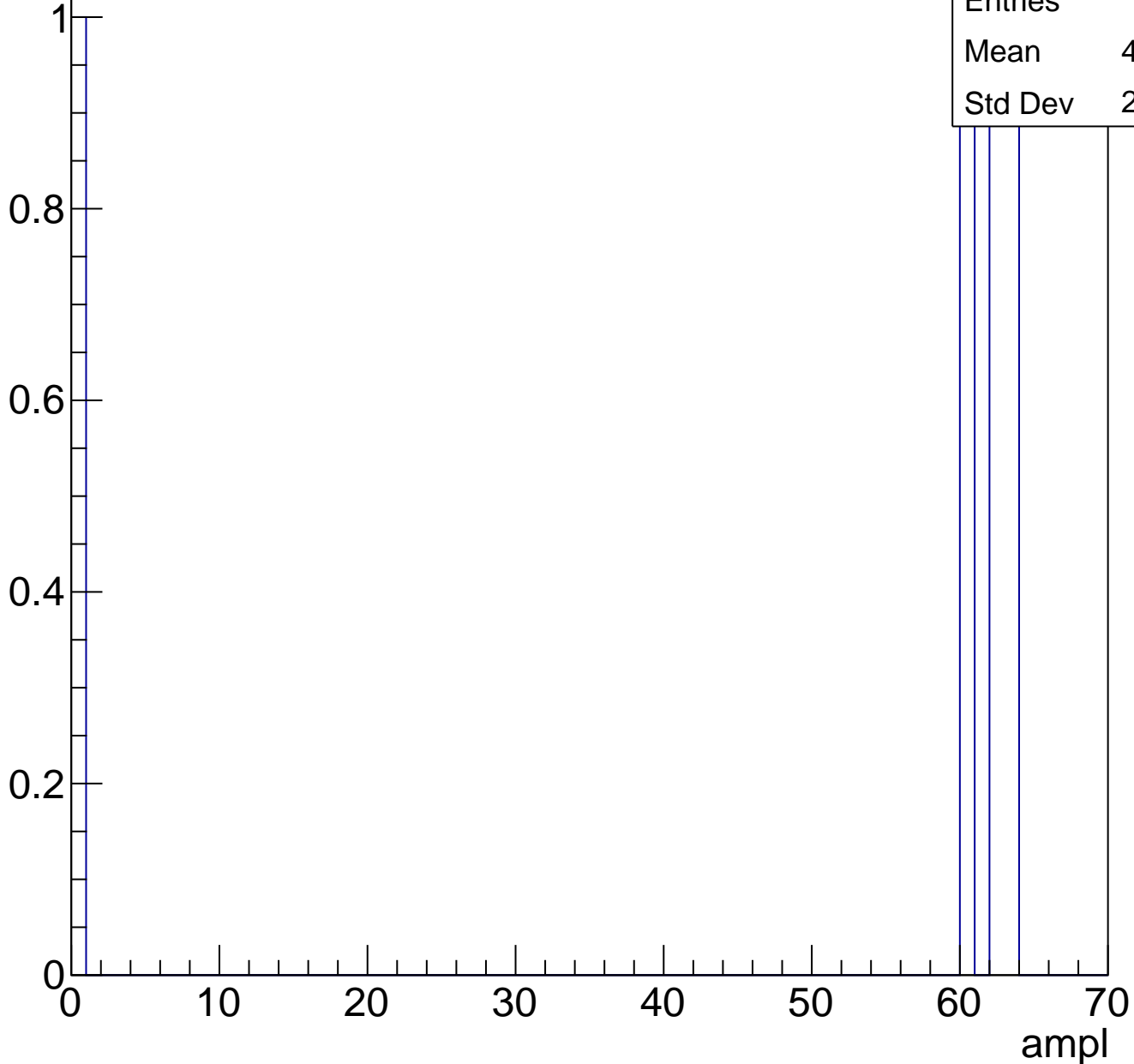




# B1L103S, U2-ch28, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch29, adc0

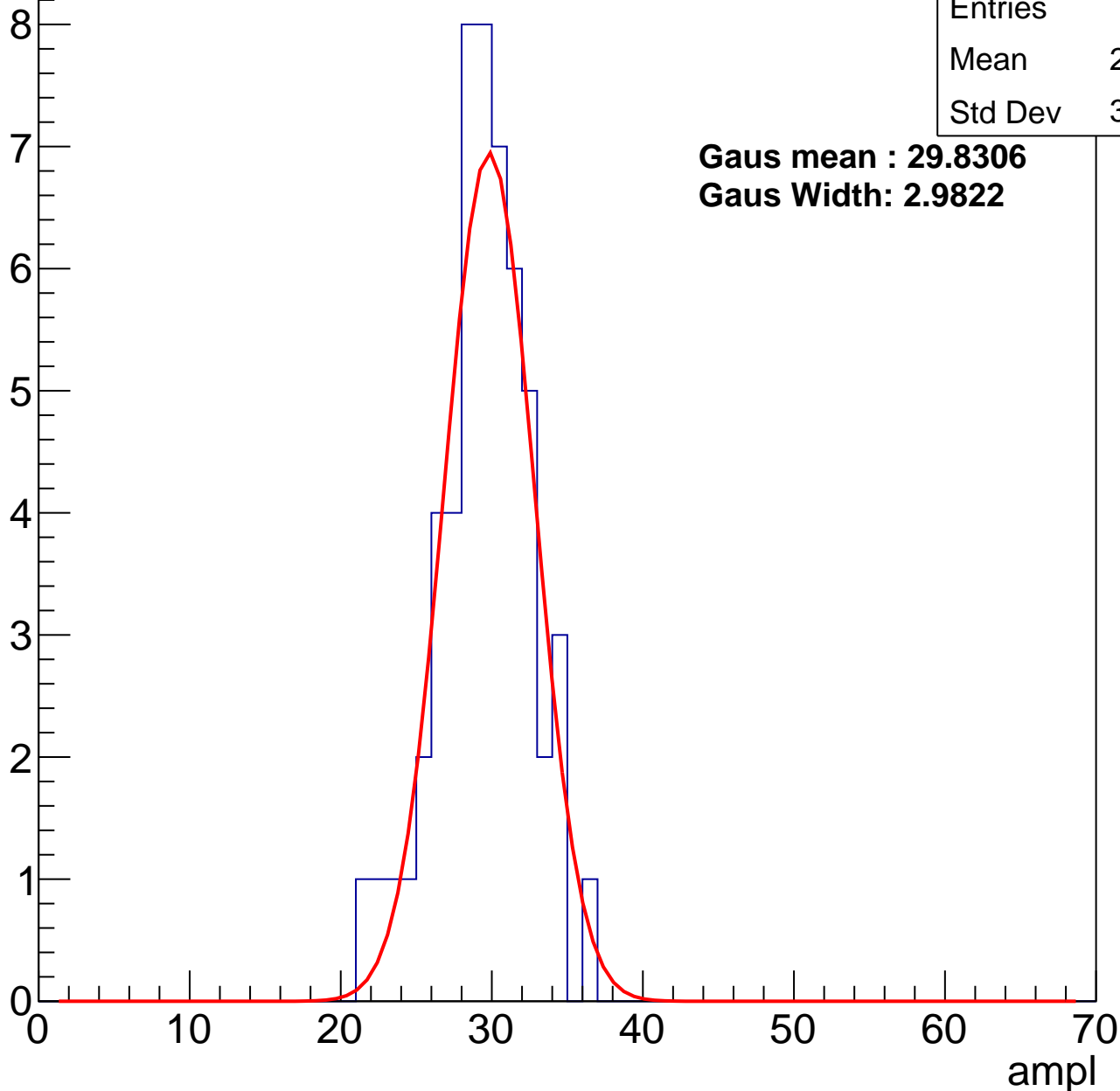
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	29.04
Std Dev	3.037

**Gaus mean : 29.8306**

**Gaus Width: 2.9822**



# B1L103S, U2-ch29, adc1

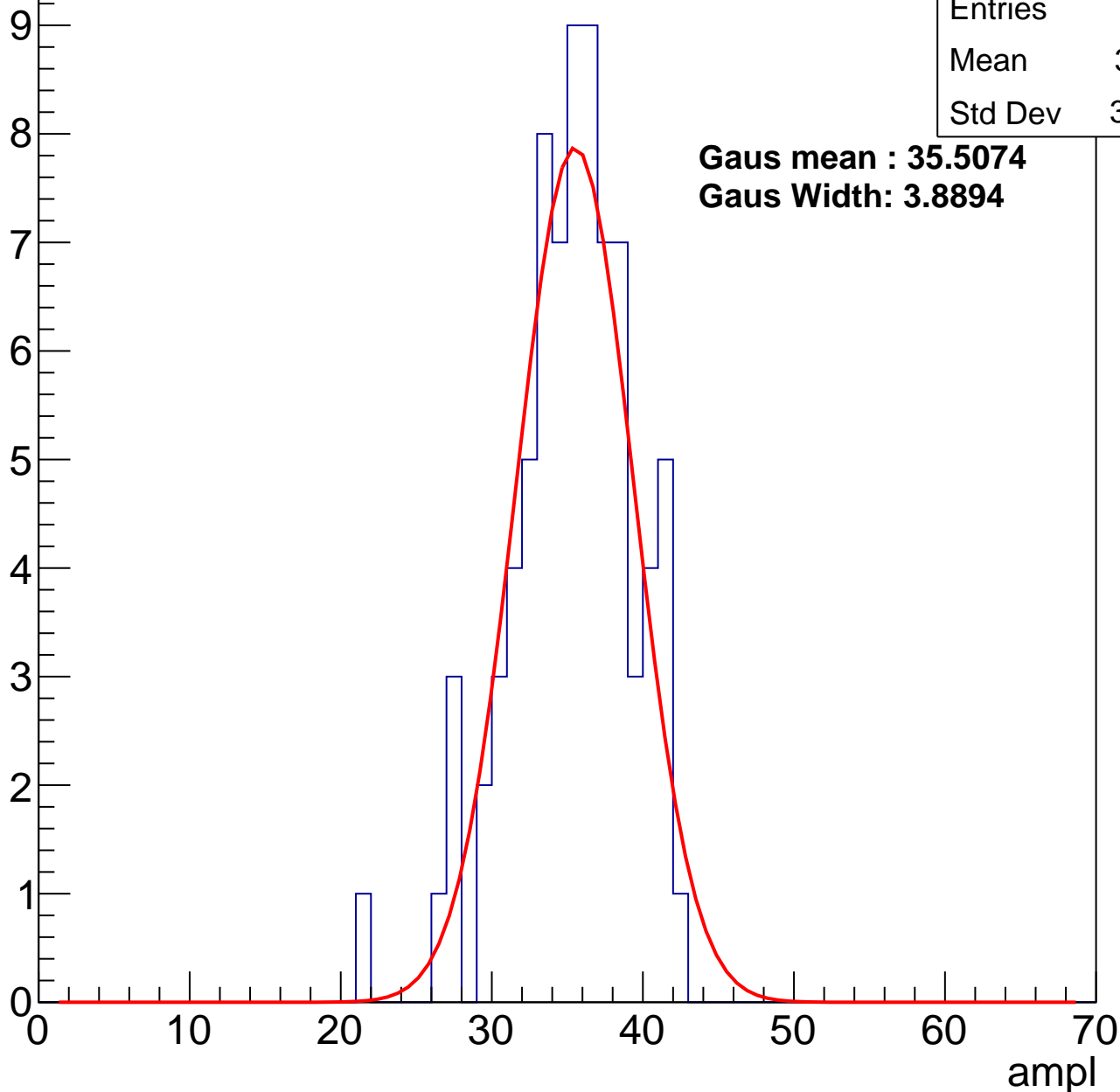
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	79
Mean	34.81
Std Dev	3.959

**Gaus mean : 35.5074**

**Gaus Width: 3.8894**



# B1L103S, U2-ch29, adc2

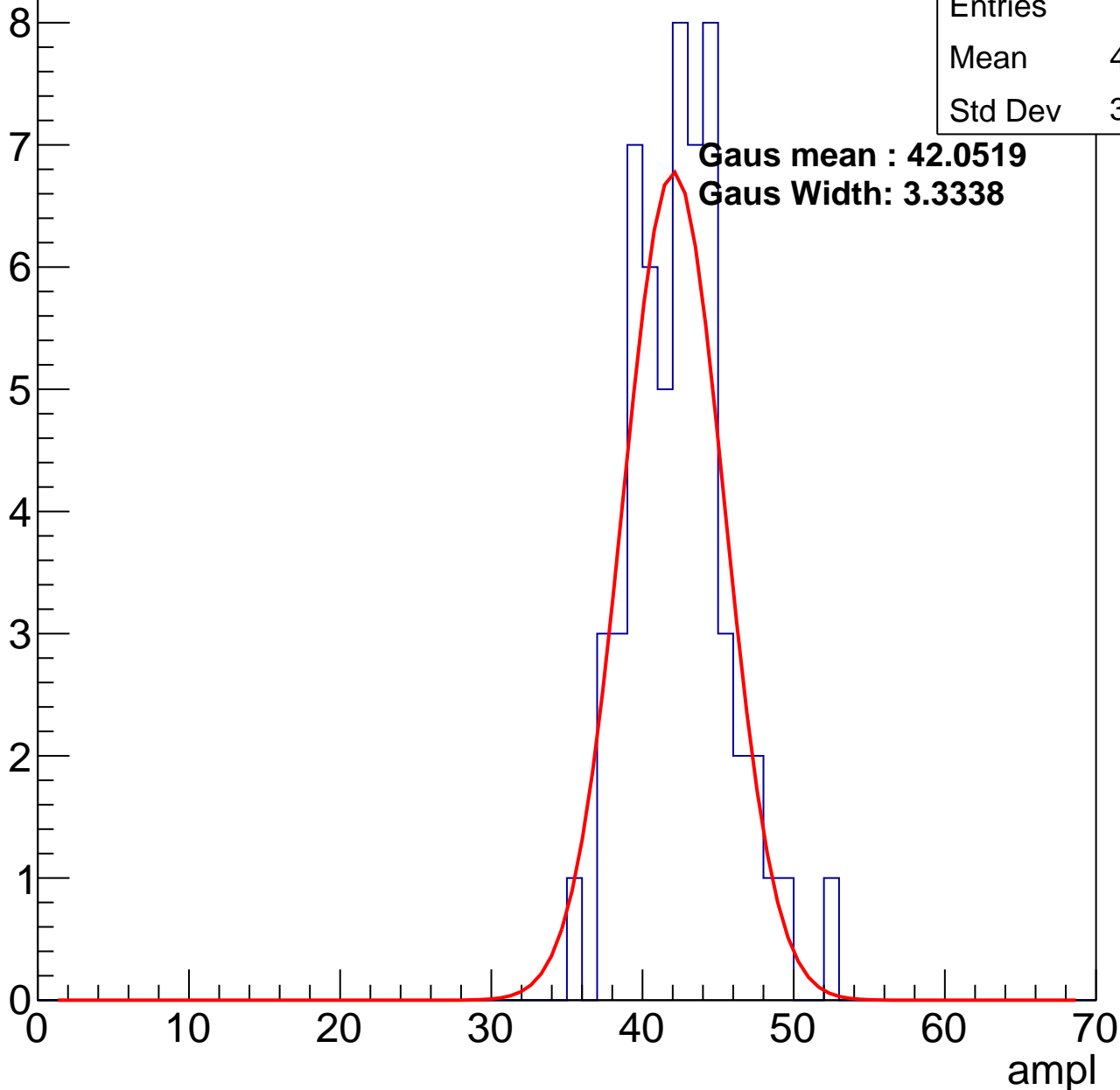
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	42.02
Std Dev	3.208

**Gaus mean : 42.0519**

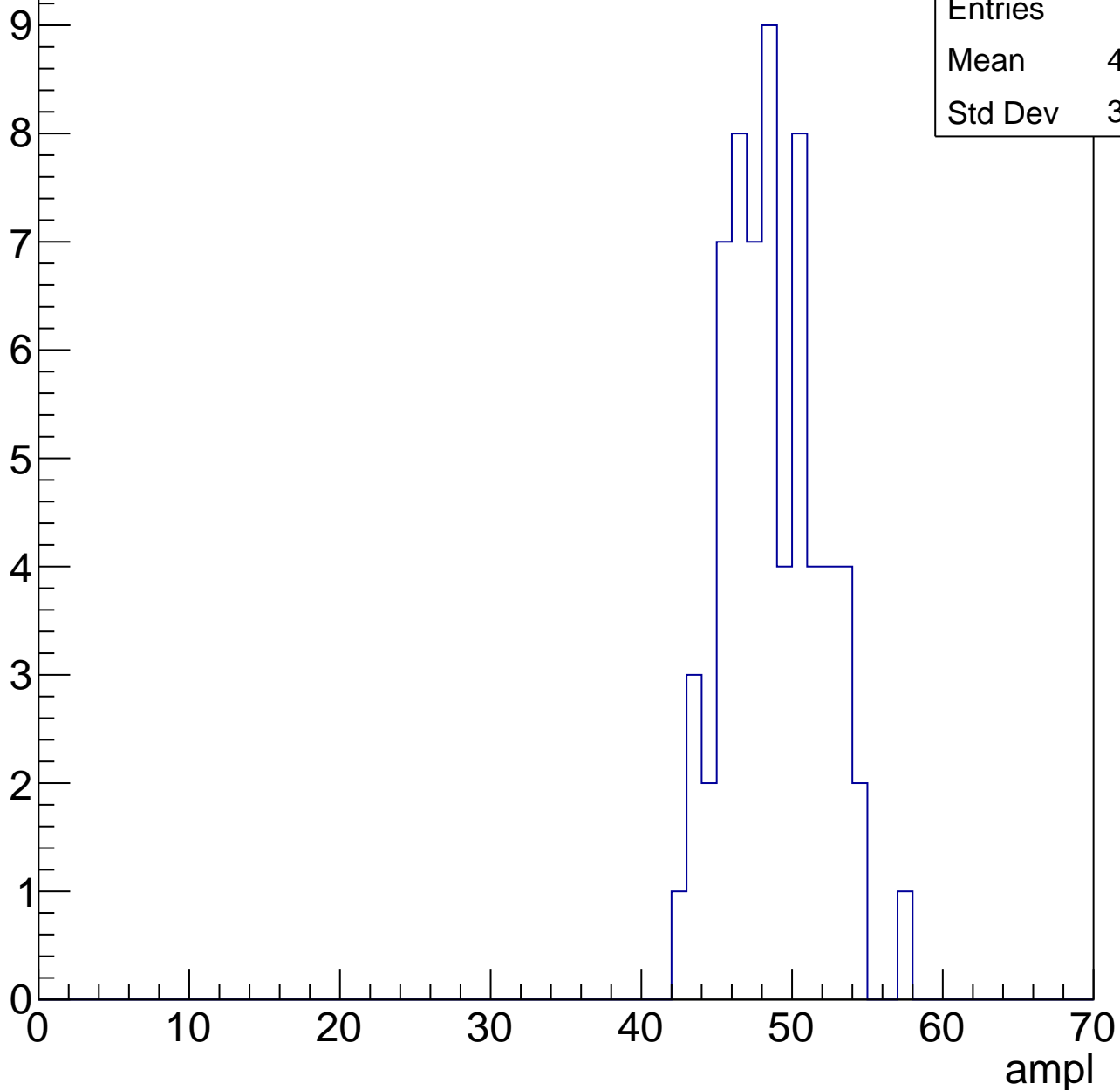
**Gaus Width: 3.3338**



# B1L103S, U2-ch29, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



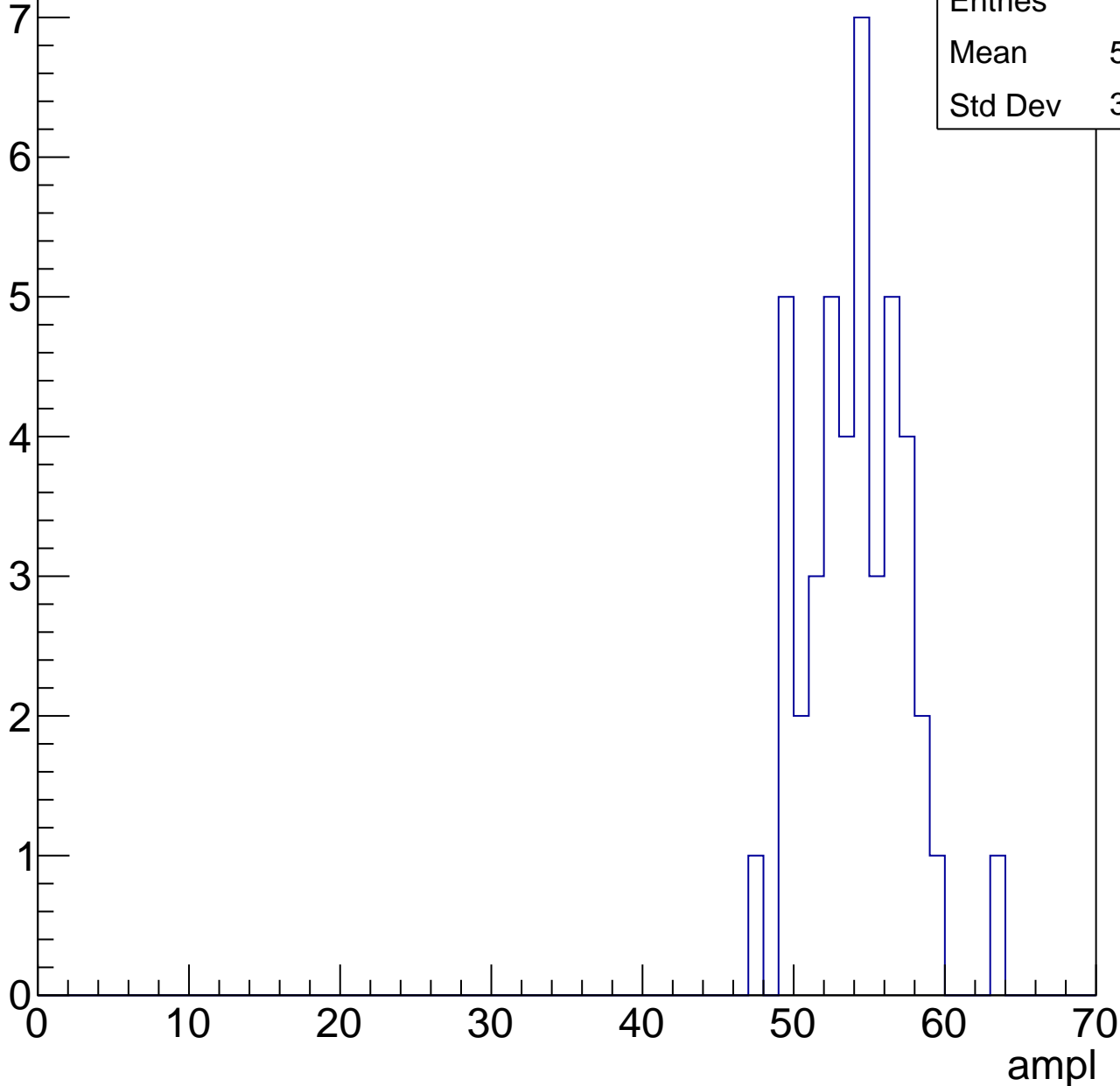
Entries	64
Mean	48.25
Std Dev	3.137

# B1L103S, U2-ch29, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

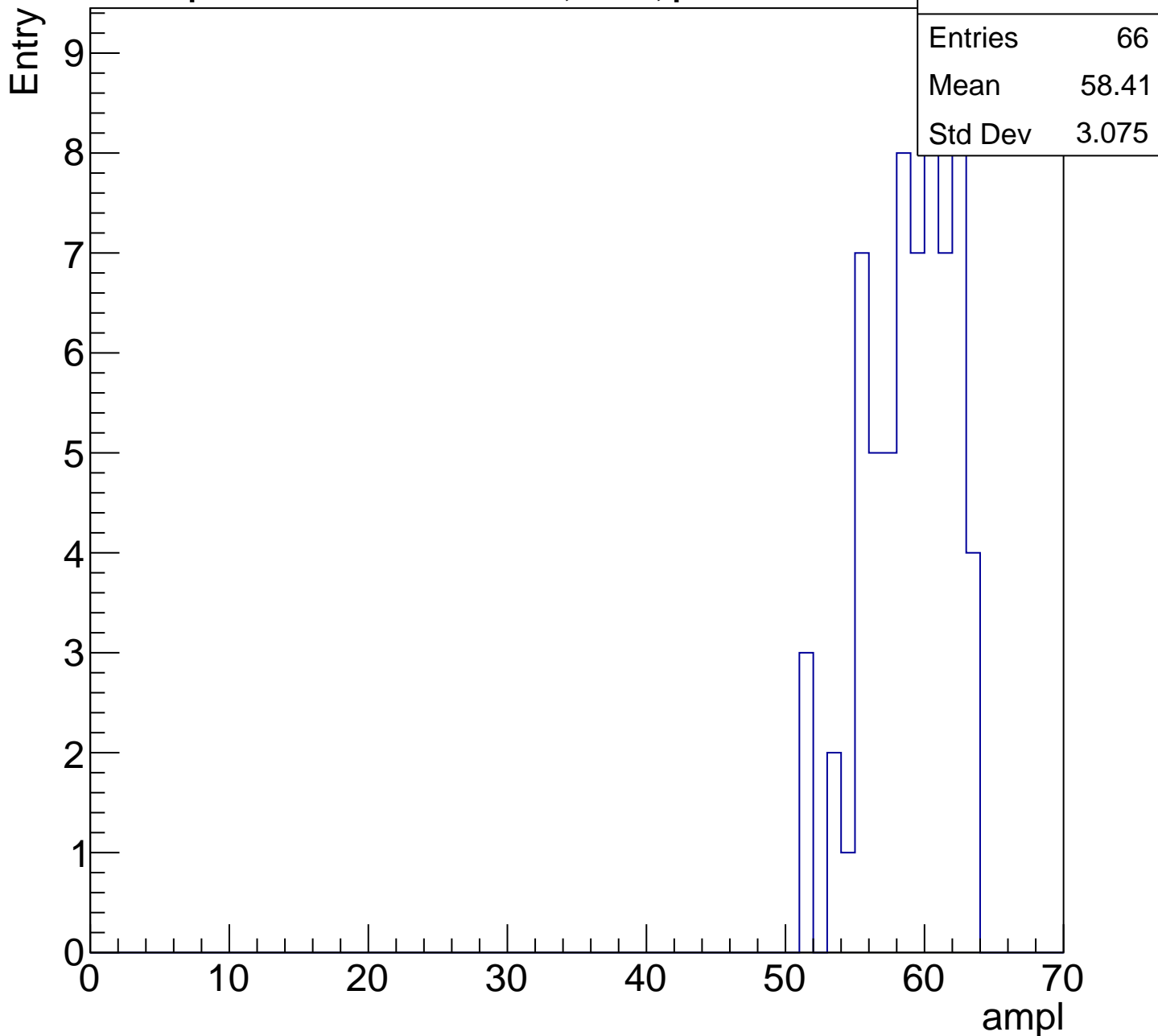
Entry

Entries	43
Mean	53.63
Std Dev	3.228



# B1L103S, U2-ch29, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

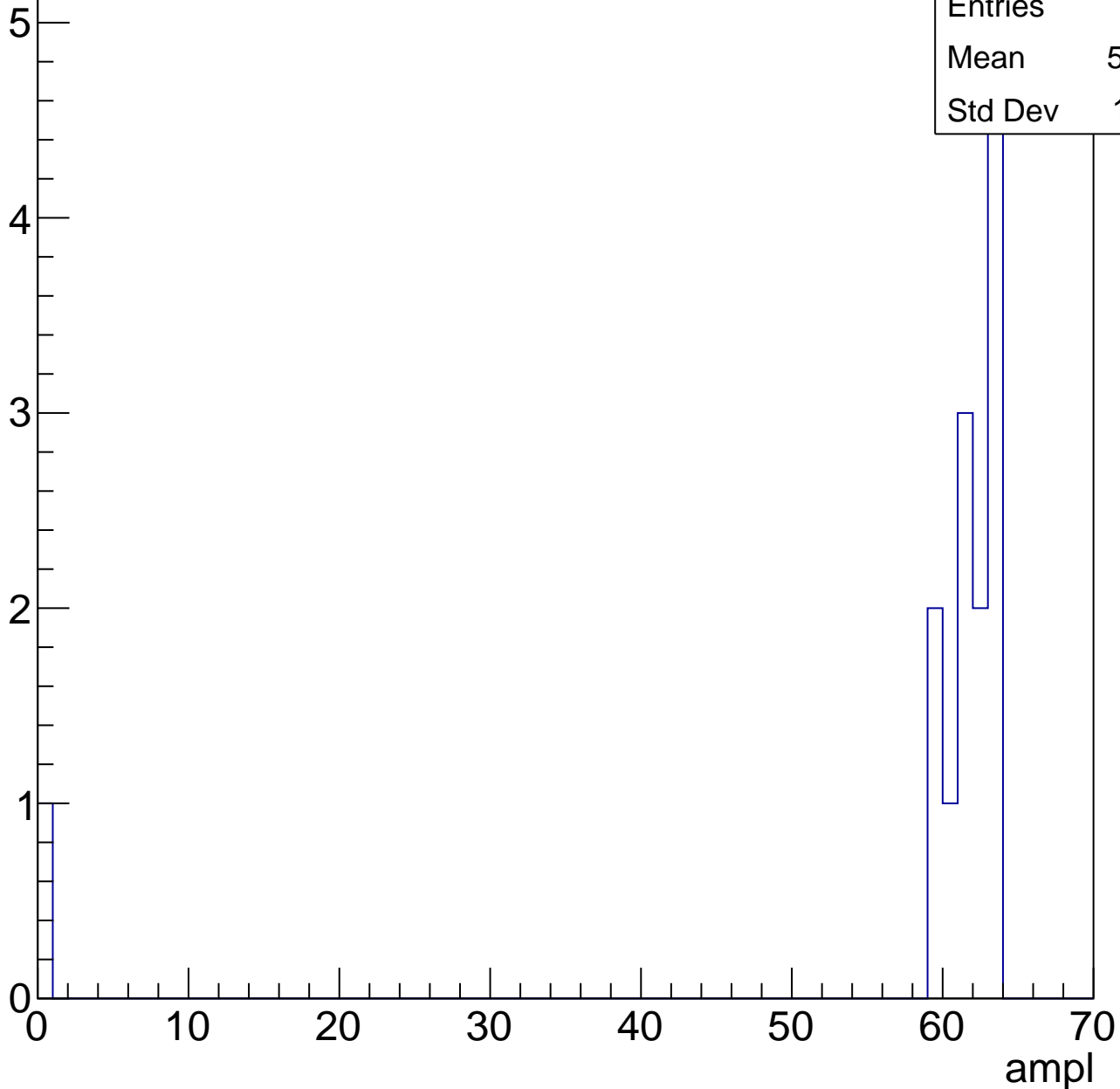


# B1L103S, U2-ch29, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	14
Mean	57.14
Std Dev	15.91





# B1L103S, U2-ch29, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U2-ch30, adc0

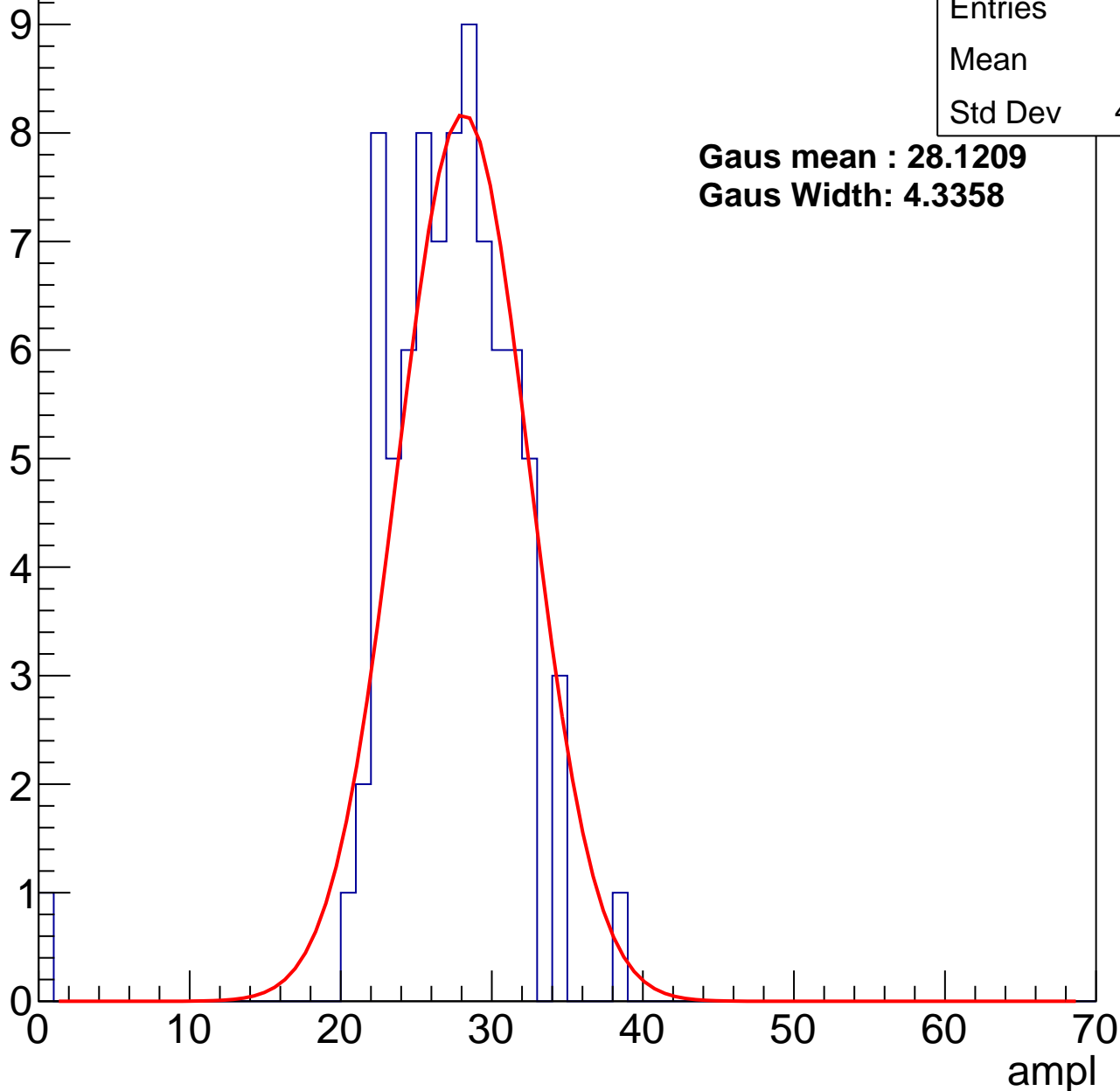
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	83
Mean	26.7
Std Dev	4.651

**Gaus mean : 28.1209**

**Gaus Width: 4.3358**



# B1L103S, U2-ch30, adc1

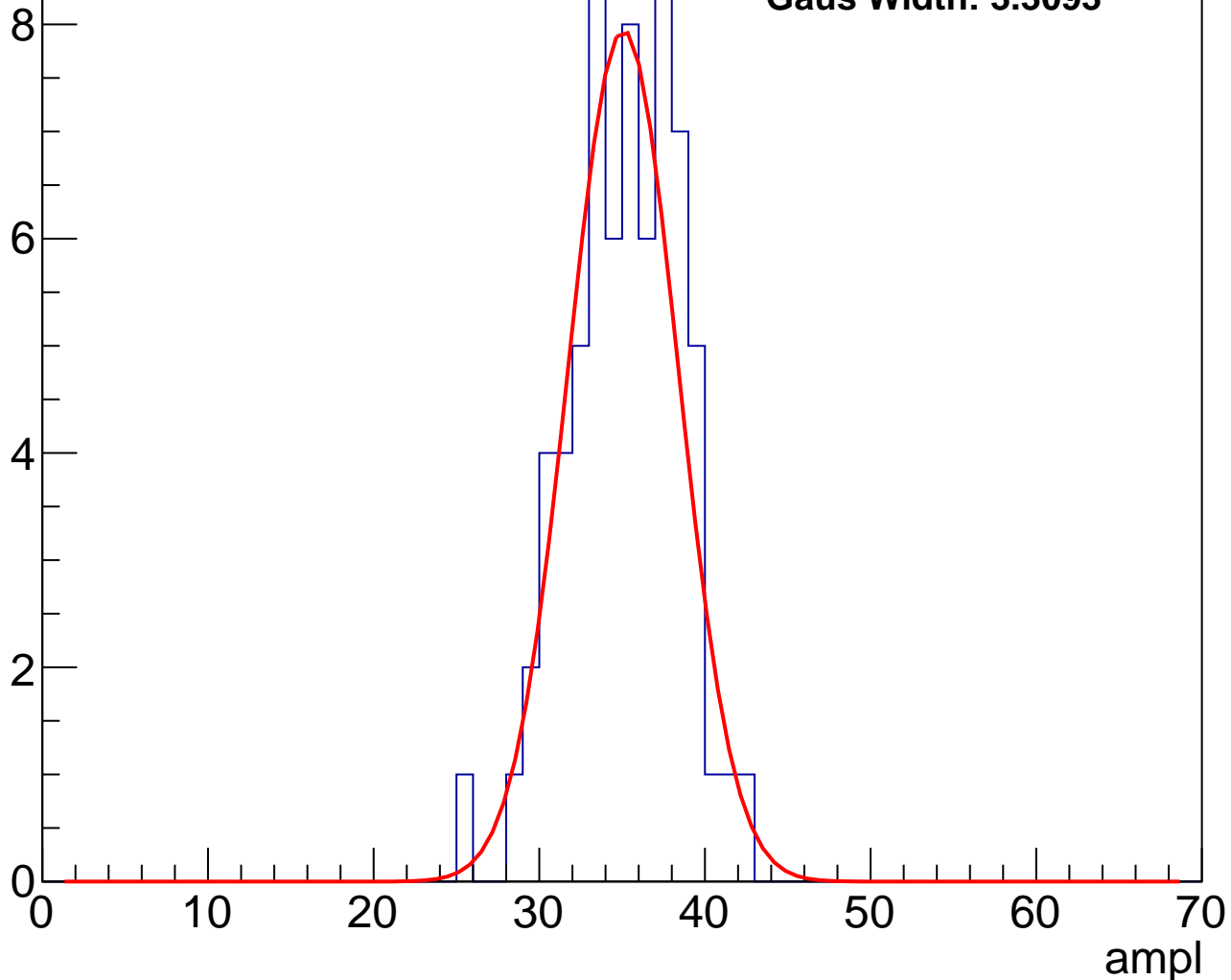
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	34.68
Std Dev	3.279

**Gaus mean : 35.0683**

**Gaus Width: 3.3093**



# B1L103S, U2-ch30, adc2

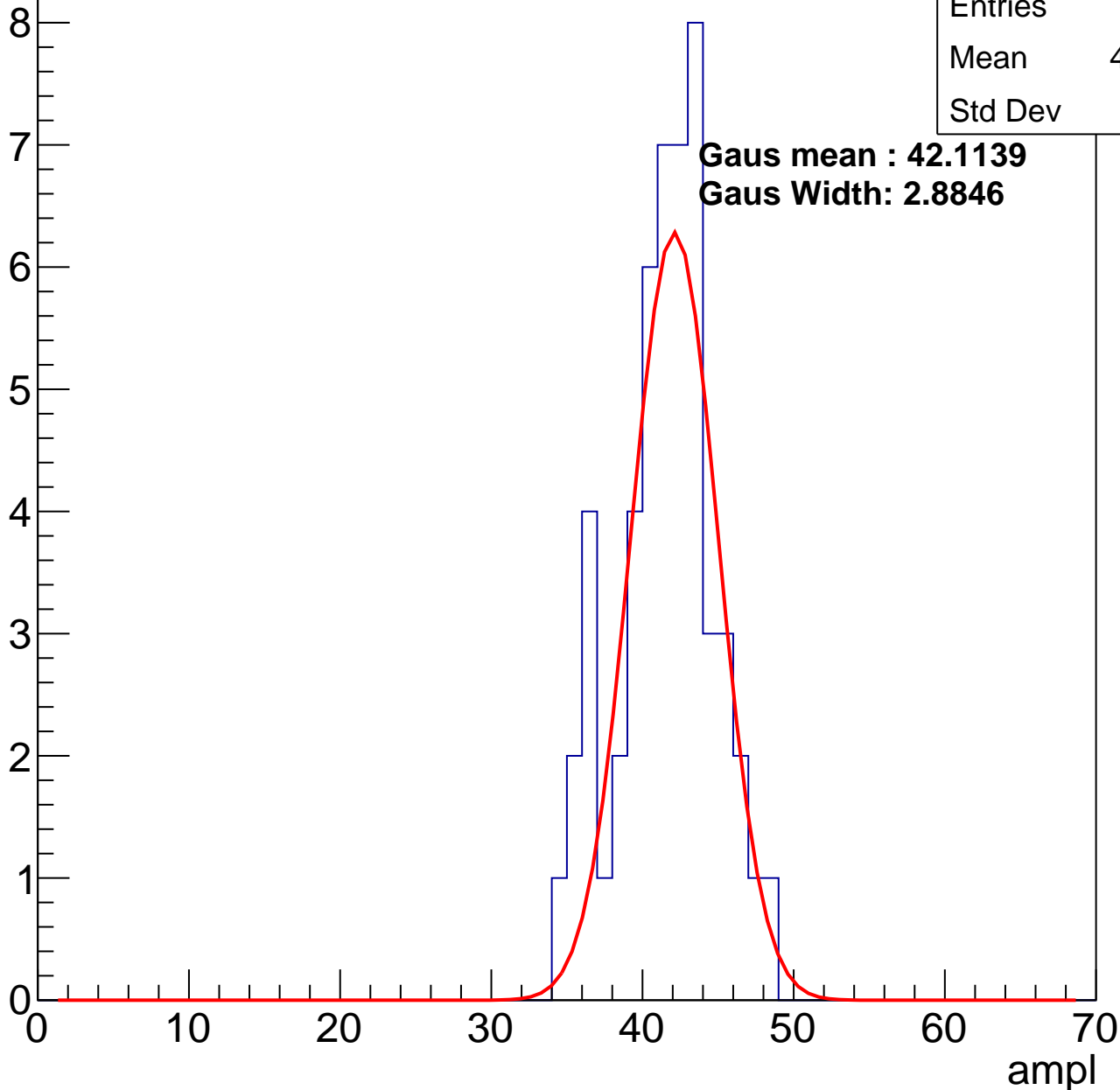
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	41.08
Std Dev	3.18

**Gaus mean : 42.1139**

**Gaus Width: 2.8846**

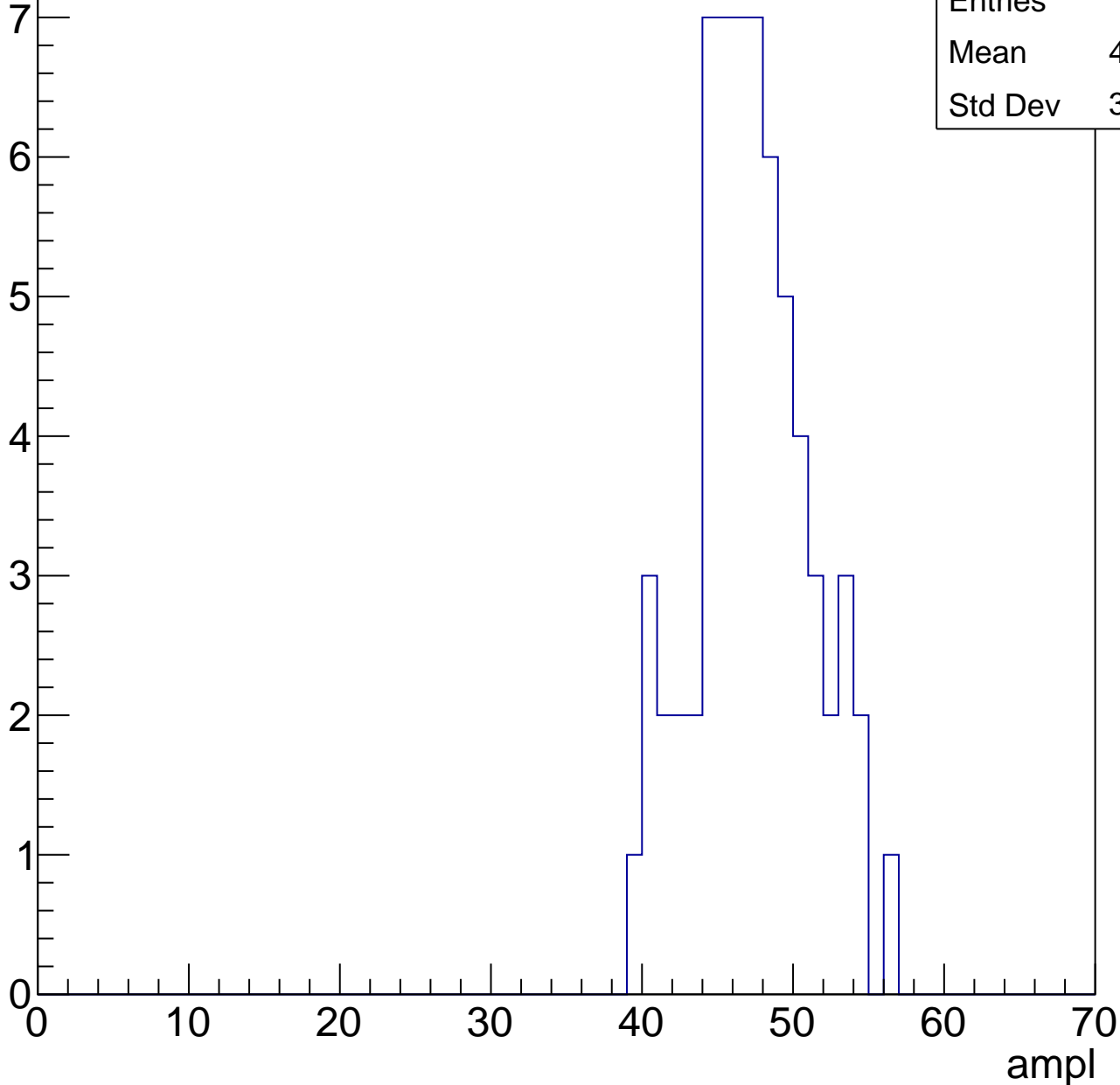


# B1L103S, U2-ch30, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	46.84
Std Dev	3.768

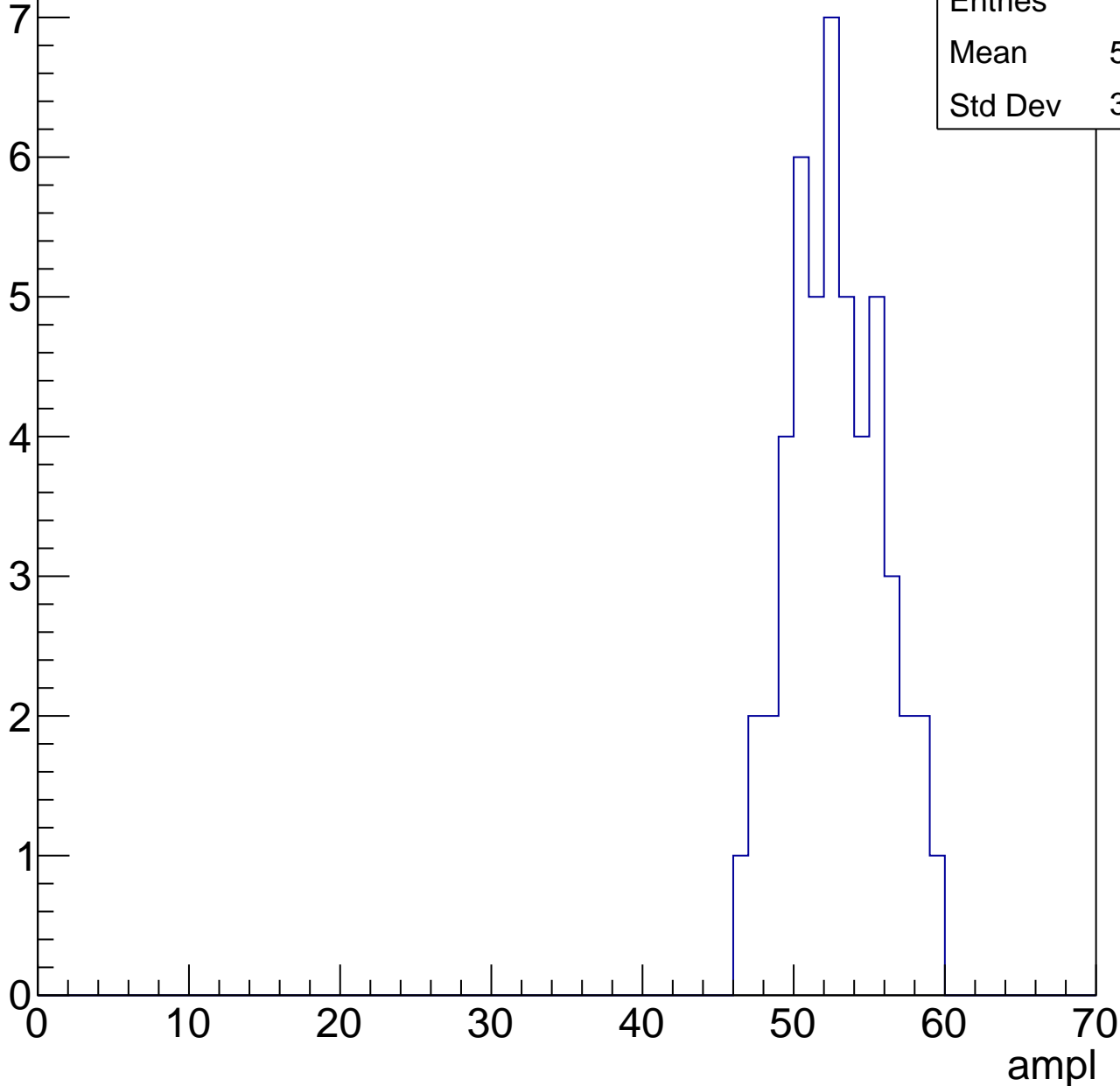


# B1L103S, U2-ch30, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	52.33
Std Dev	3.073

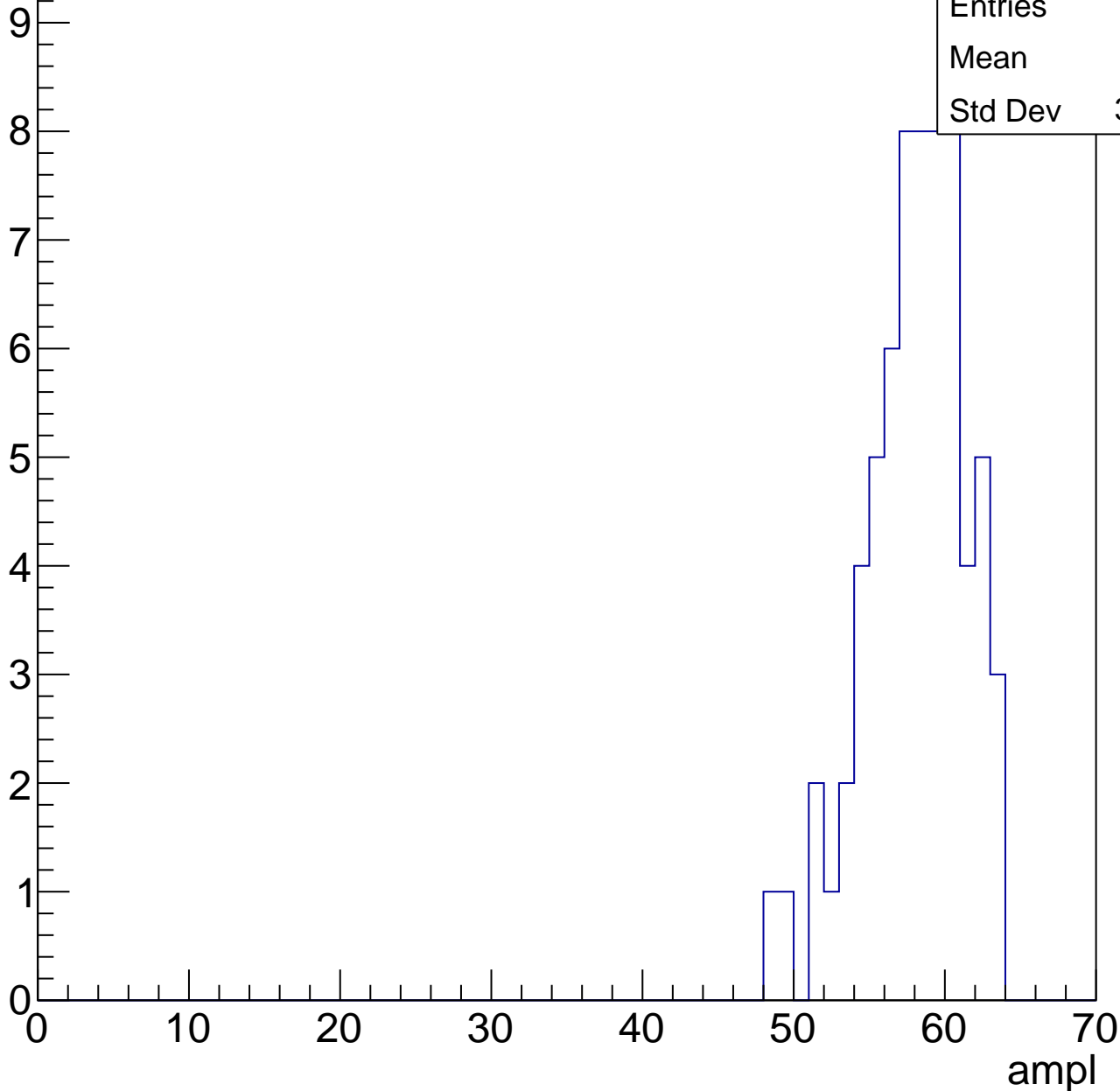


# B1L103S, U2-ch30, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	57.6
Std Dev	3.301

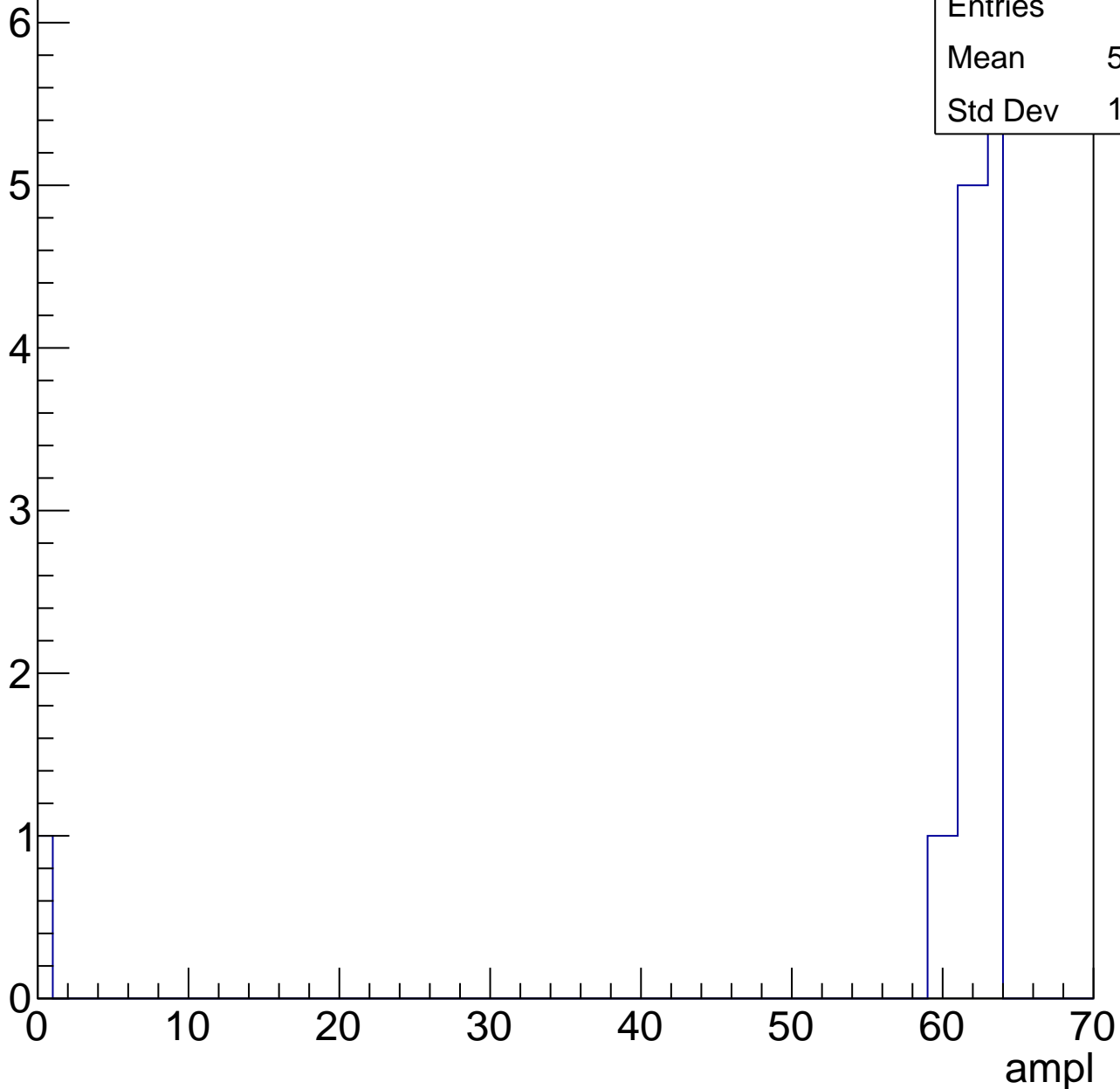


# B1L103S, U2-ch30, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	19
Mean	58.53
Std Dev	13.84

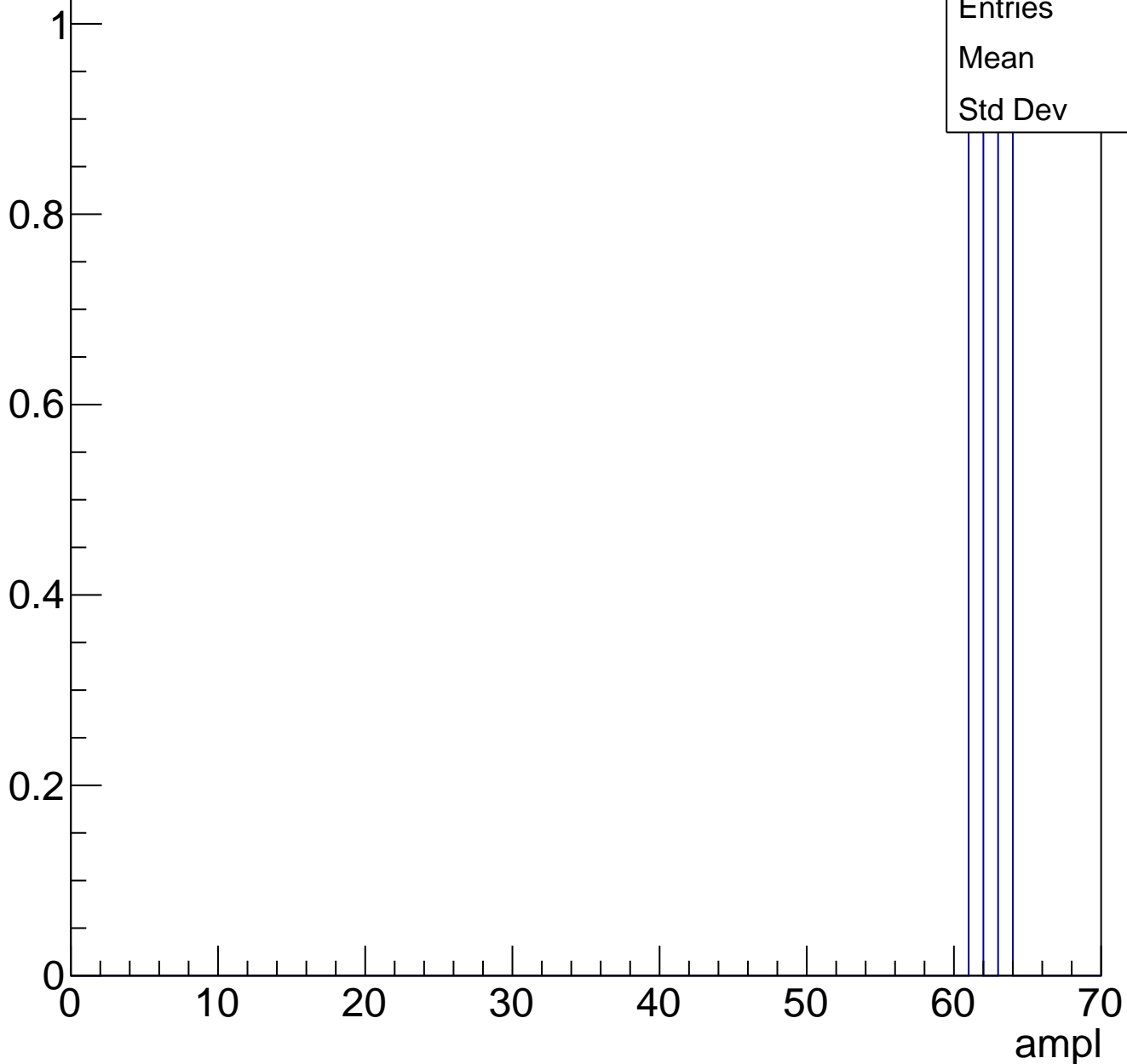




# B1L103S, U2-ch30, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch31, adc0

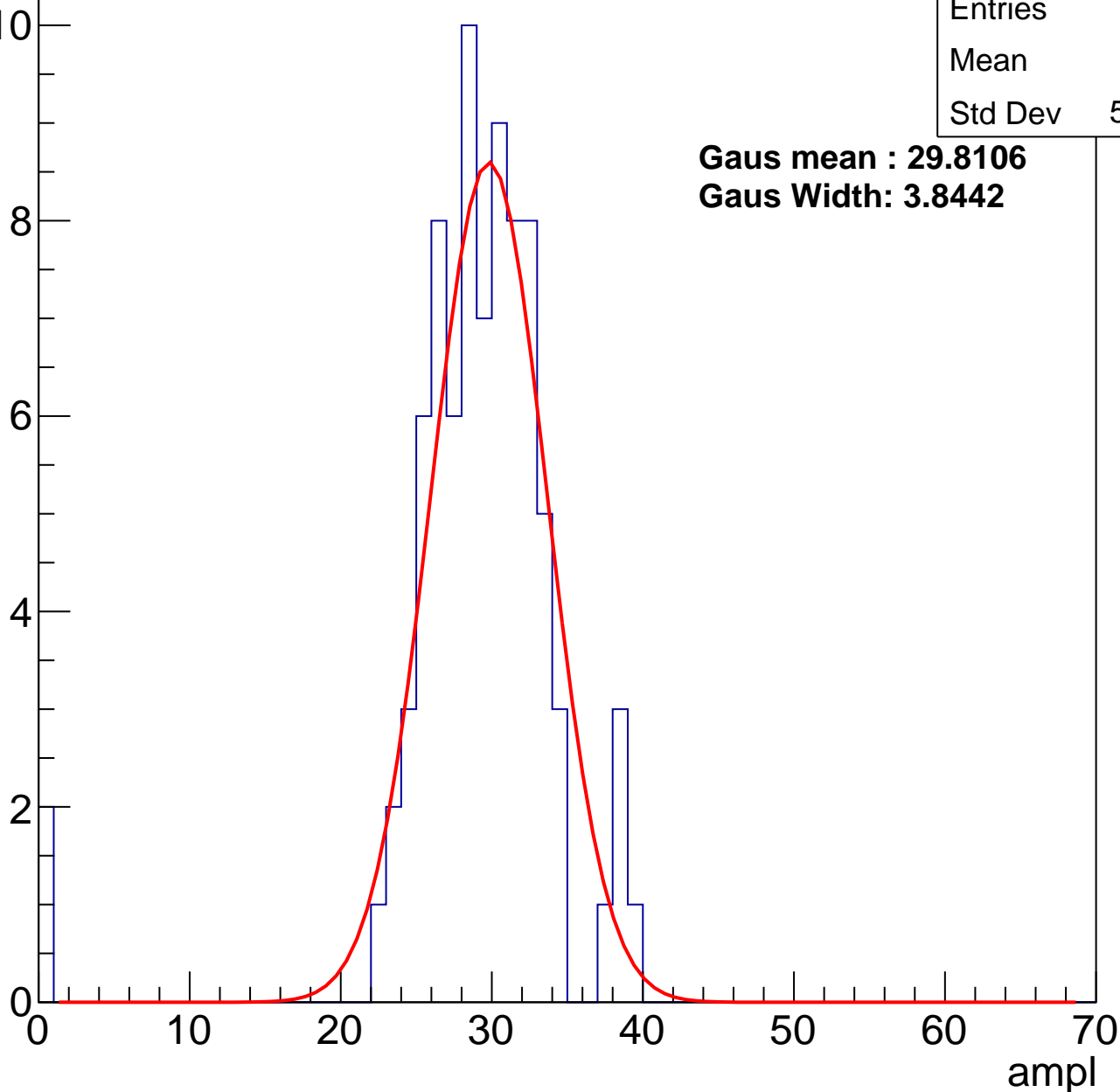
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	83
Mean	28.6
Std Dev	5.748

**Gaus mean : 29.8106**

**Gaus Width: 3.8442**



# B1L103S, U2-ch31, adc1

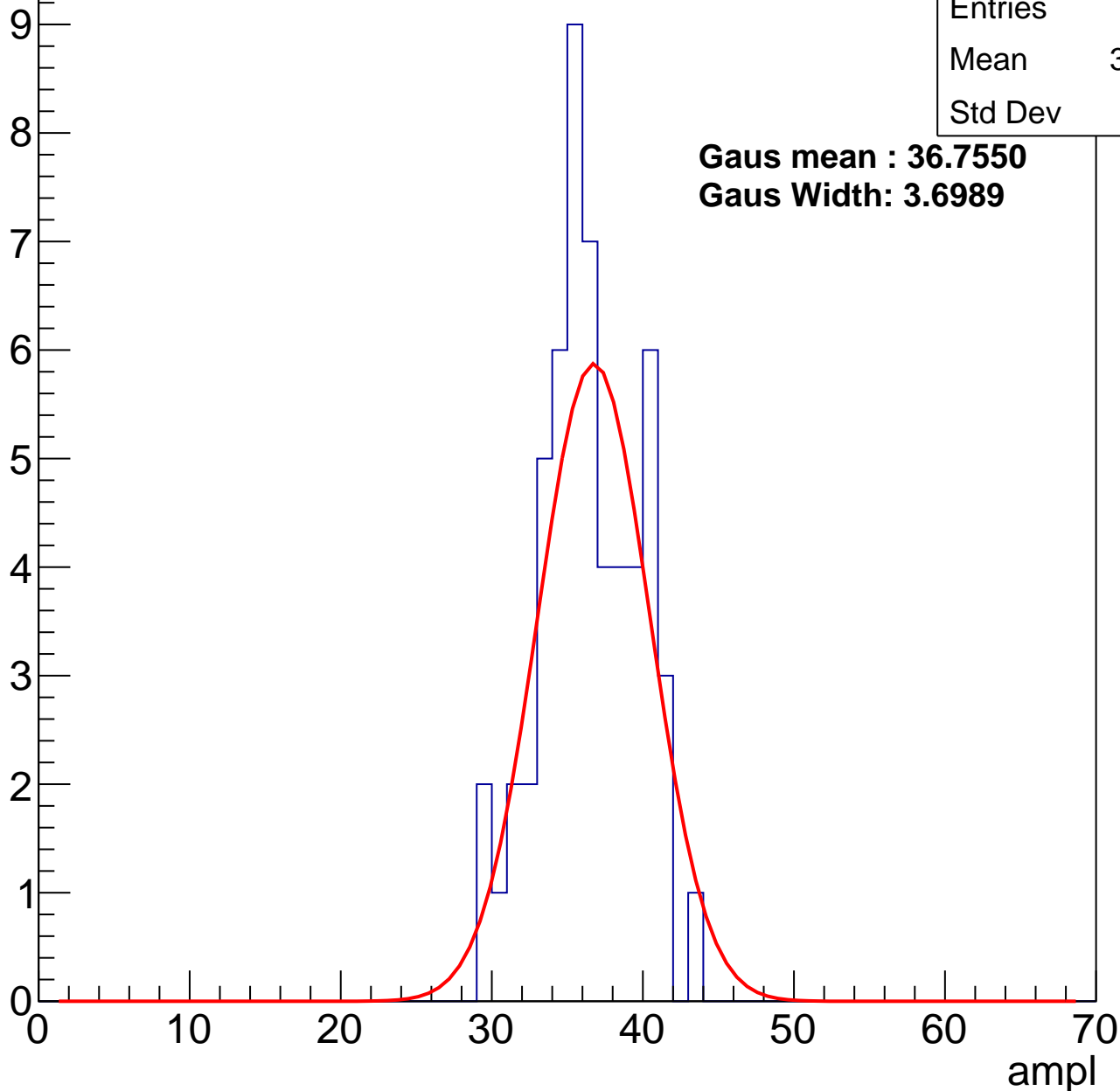
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	35.93
Std Dev	3.19

**Gaus mean : 36.7550**

**Gaus Width: 3.6989**



# B1L103S, U2-ch31, adc2

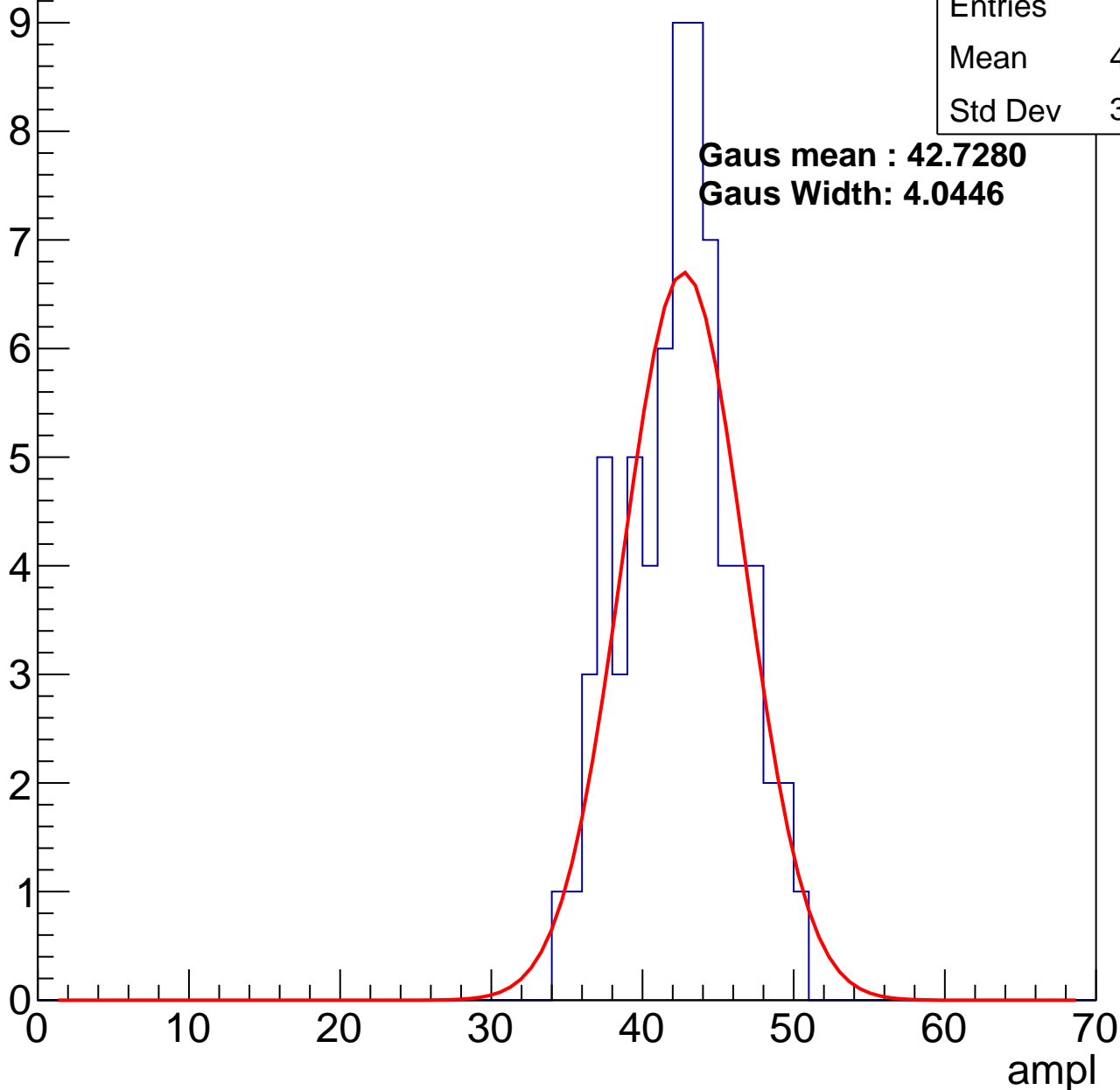
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	42.09
Std Dev	3.648

**Gaus mean : 42.7280**

**Gaus Width: 4.0446**

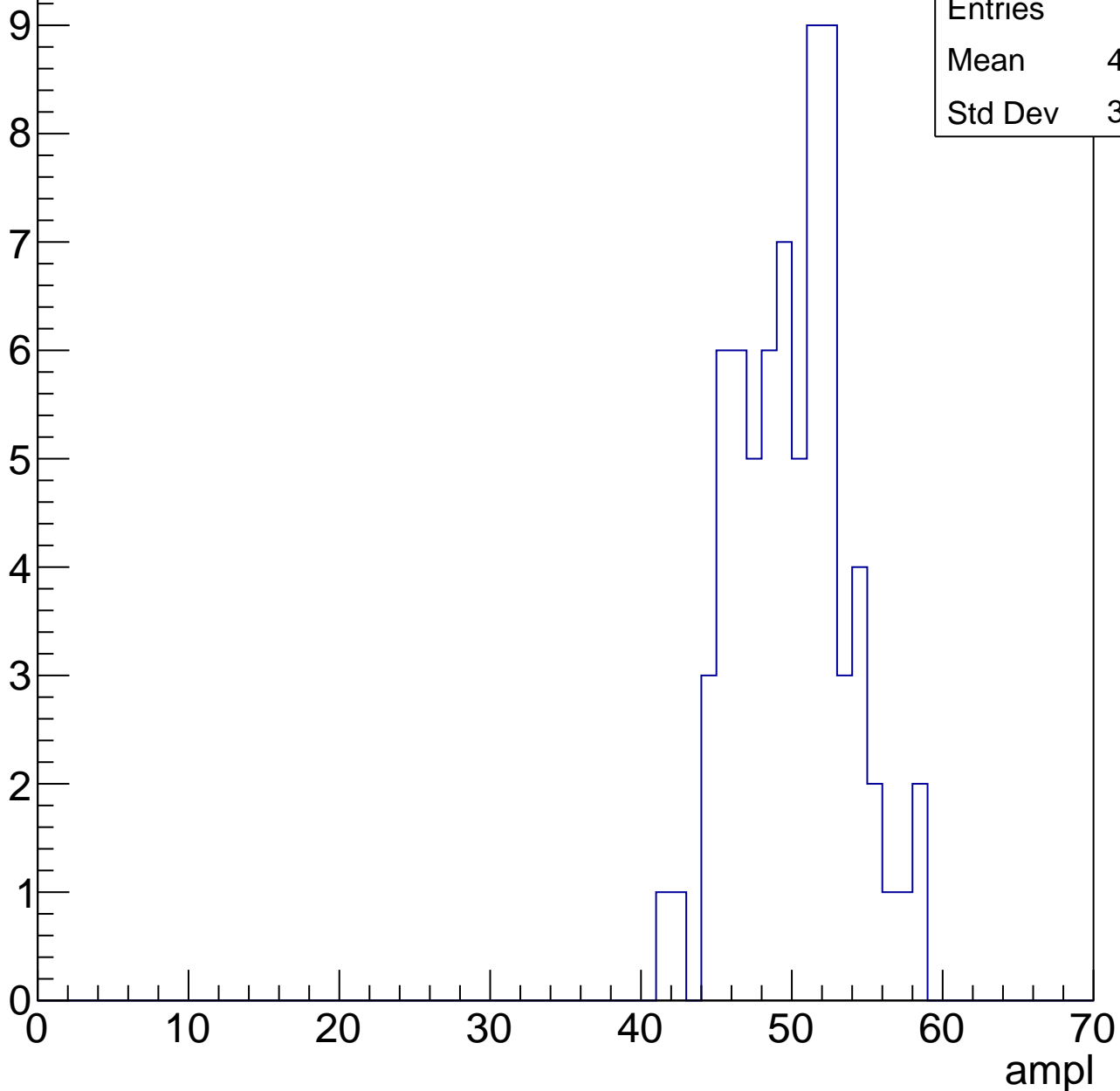


# B1L103S, U2-ch31, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	49.55
Std Dev	3.676

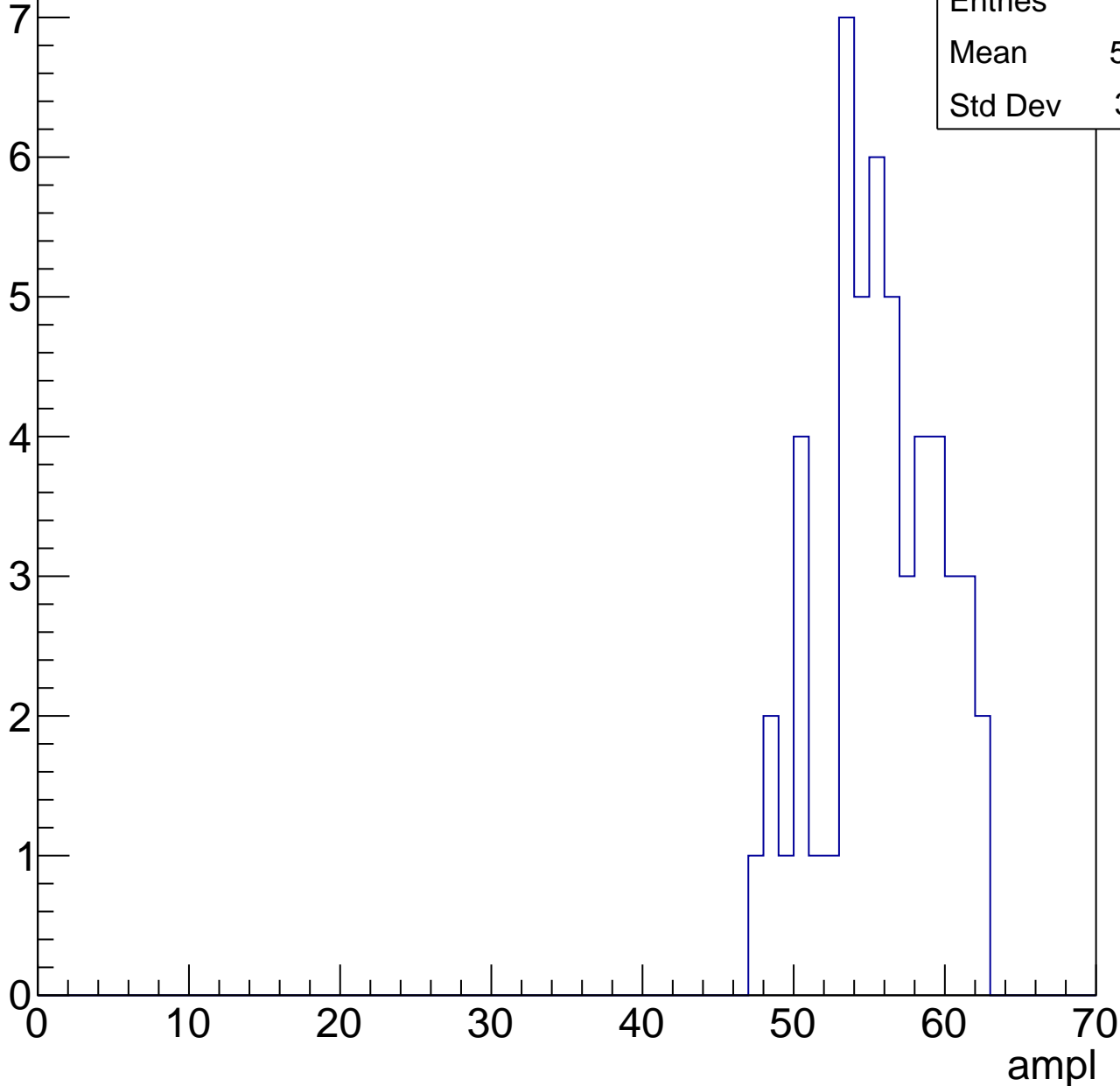


# B1L103S, U2-ch31, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	55.23
Std Dev	3.801

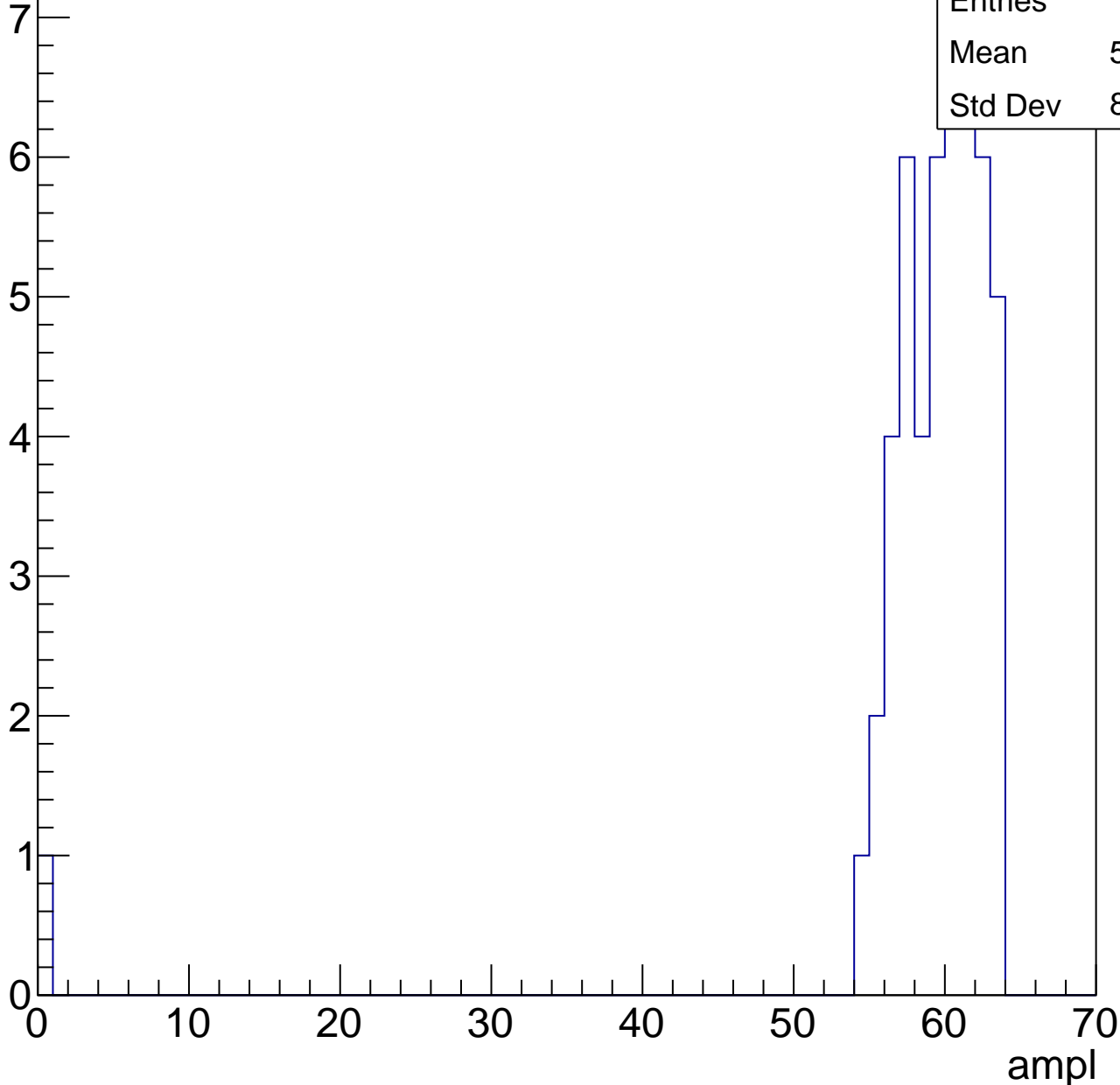


# B1L103S, U2-ch31, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	58.16
Std Dev	8.733



# B1L103S, U2-ch31, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U2-ch31, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch32, adc0

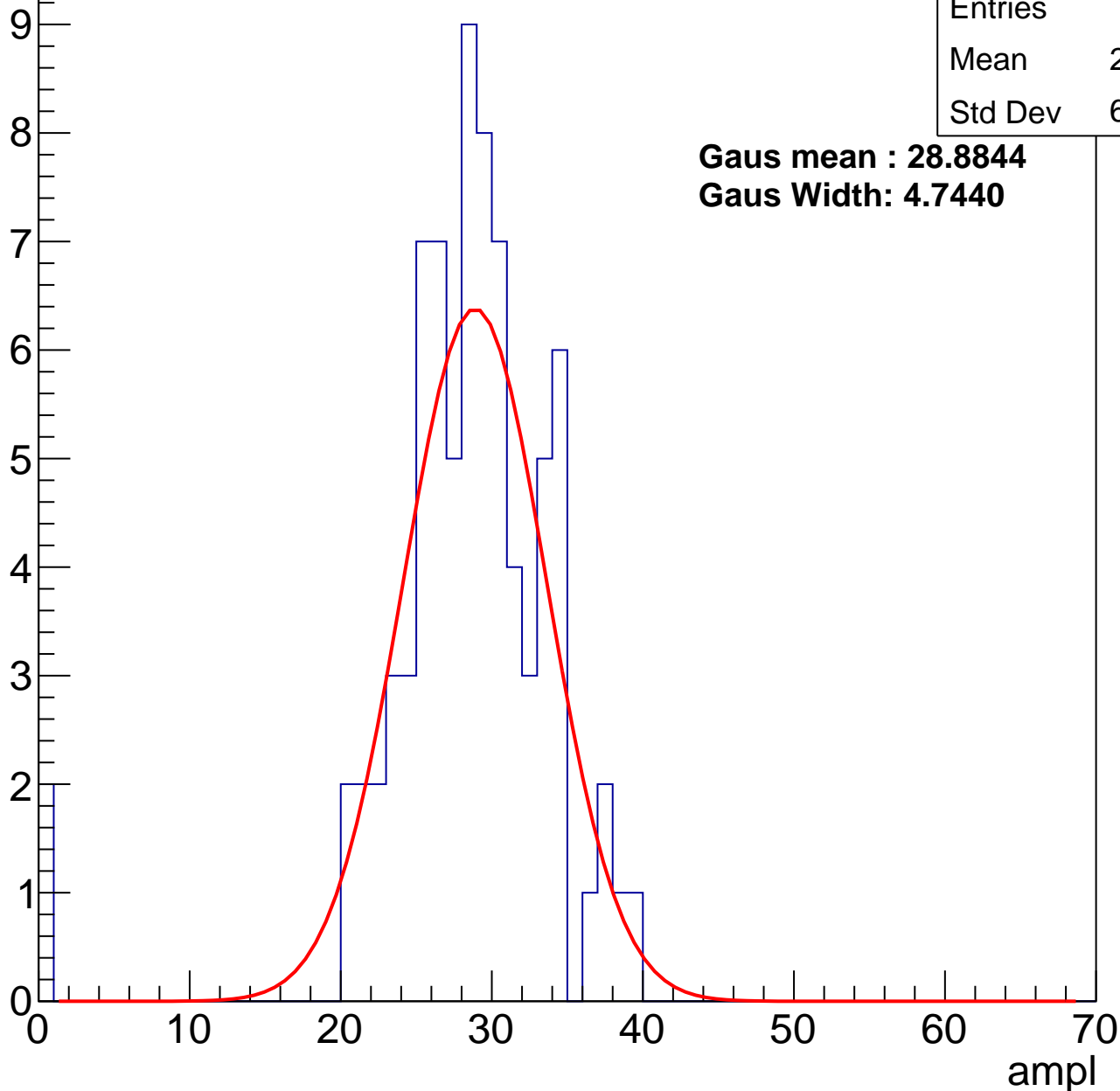
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	80
Mean	27.86
Std Dev	6.115

**Gaus mean : 28.8844**

**Gaus Width: 4.7440**



# B1L103S, U2-ch32, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	60
Mean	34.57
Std Dev	3.603

**Gaus mean : 34.5196**

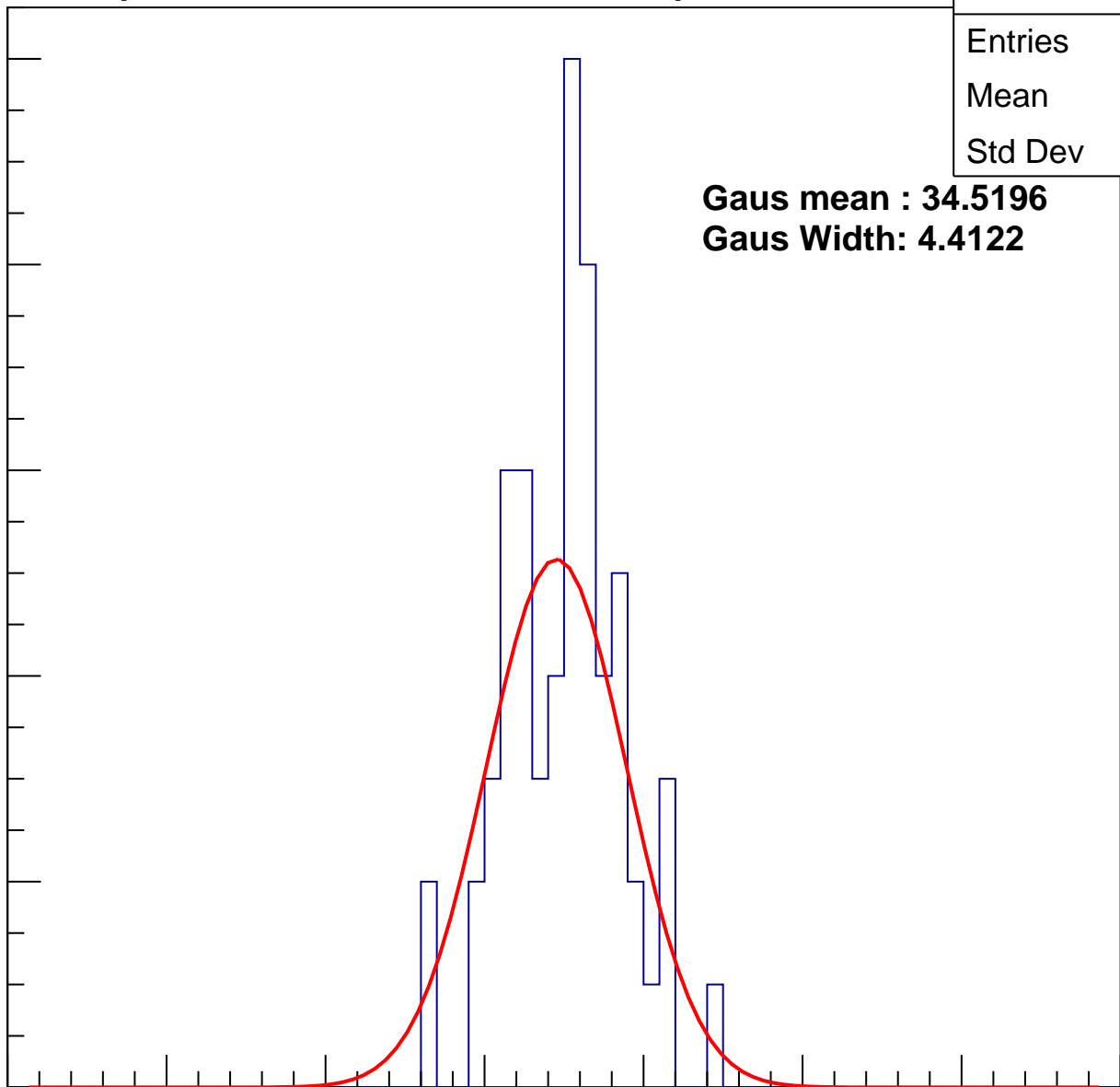
**Gaus Width: 4.4122**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U2-ch32, adc2

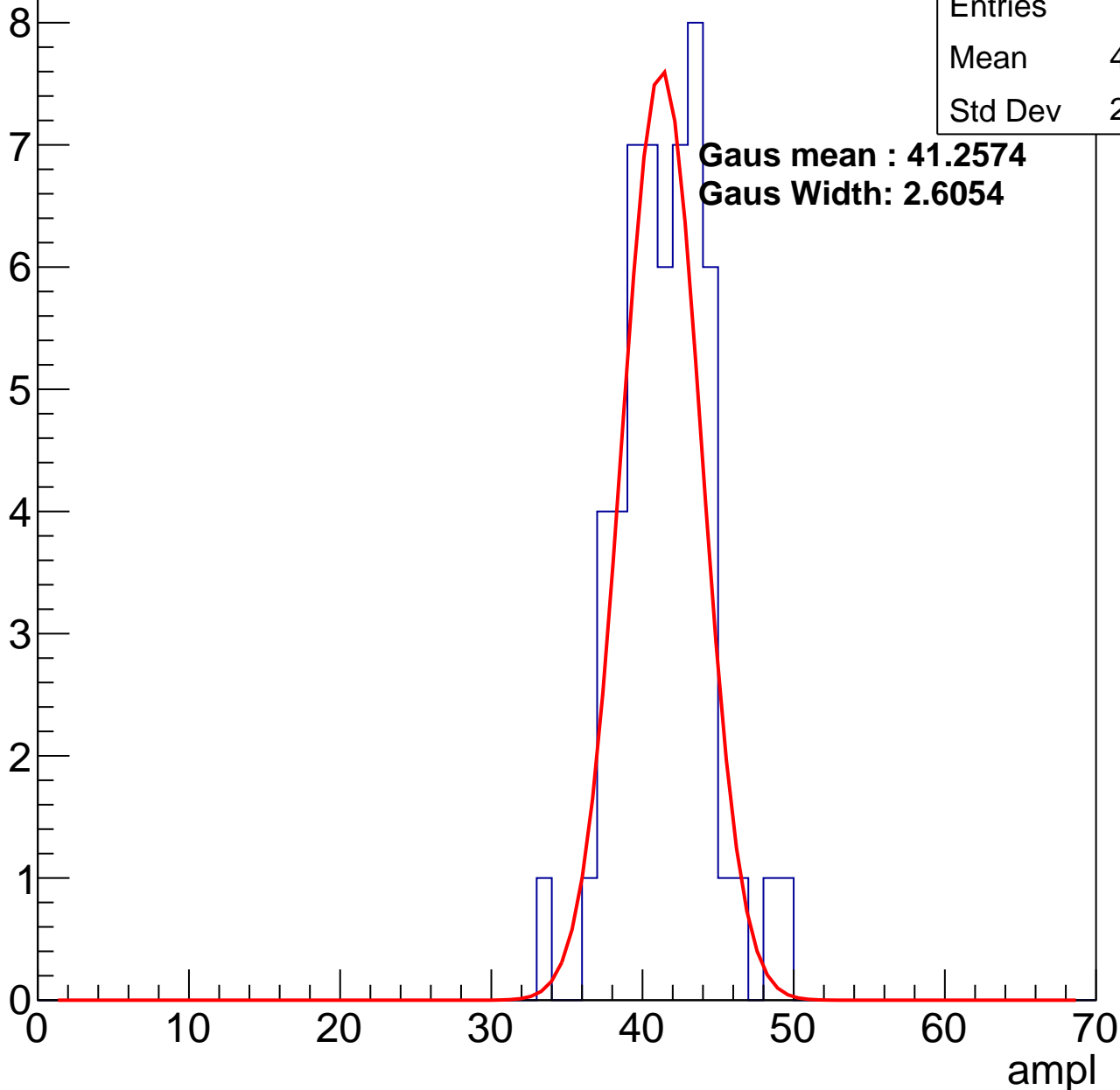
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	41.05
Std Dev	2.926

**Gaus mean : 41.2574**

**Gaus Width: 2.6054**

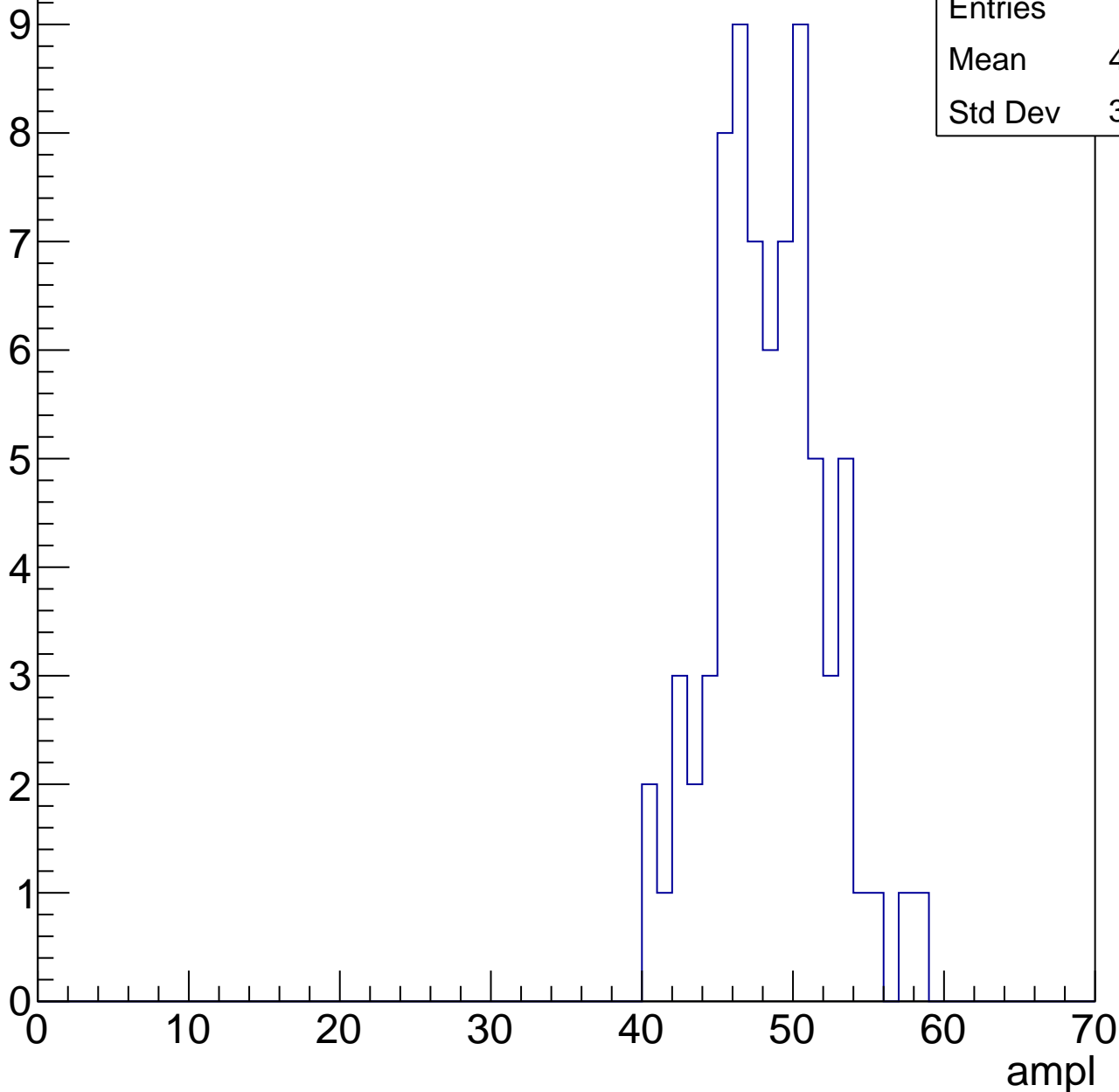


# B1L103S, U2-ch32, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

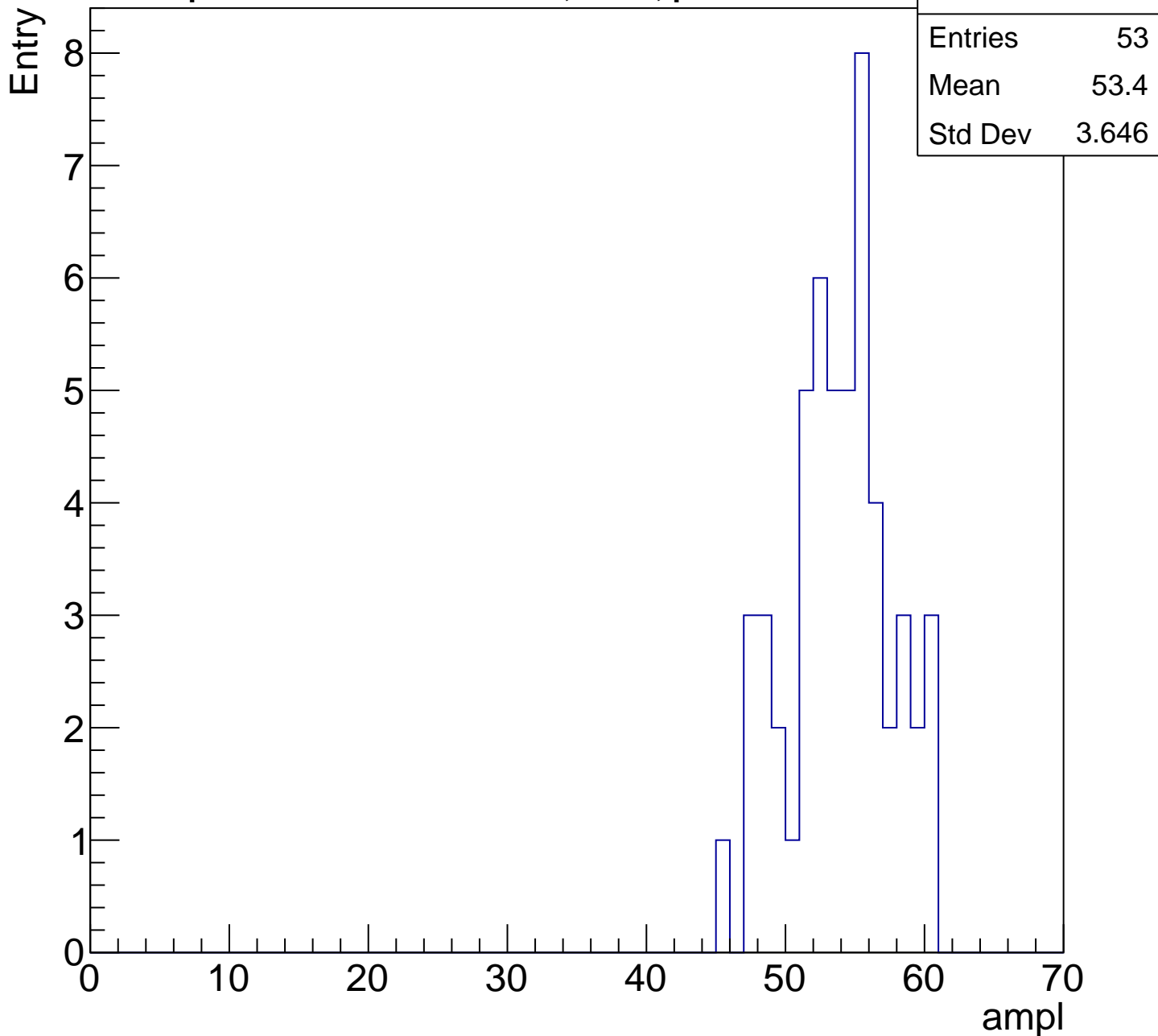
Entry

Entries	74
Mean	47.96
Std Dev	3.722



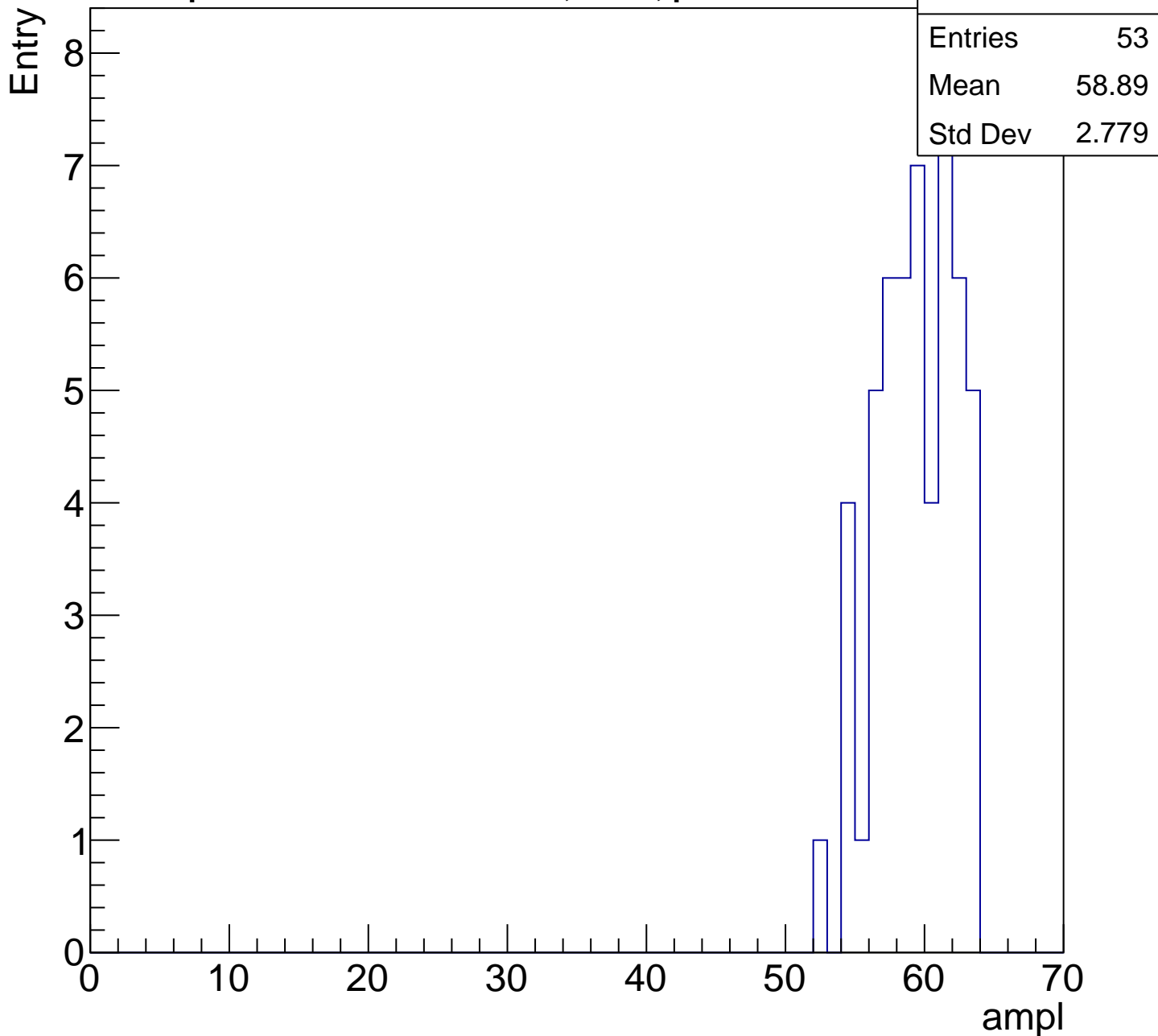
# B1L103S, U2-ch32, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U2-ch32, adc5

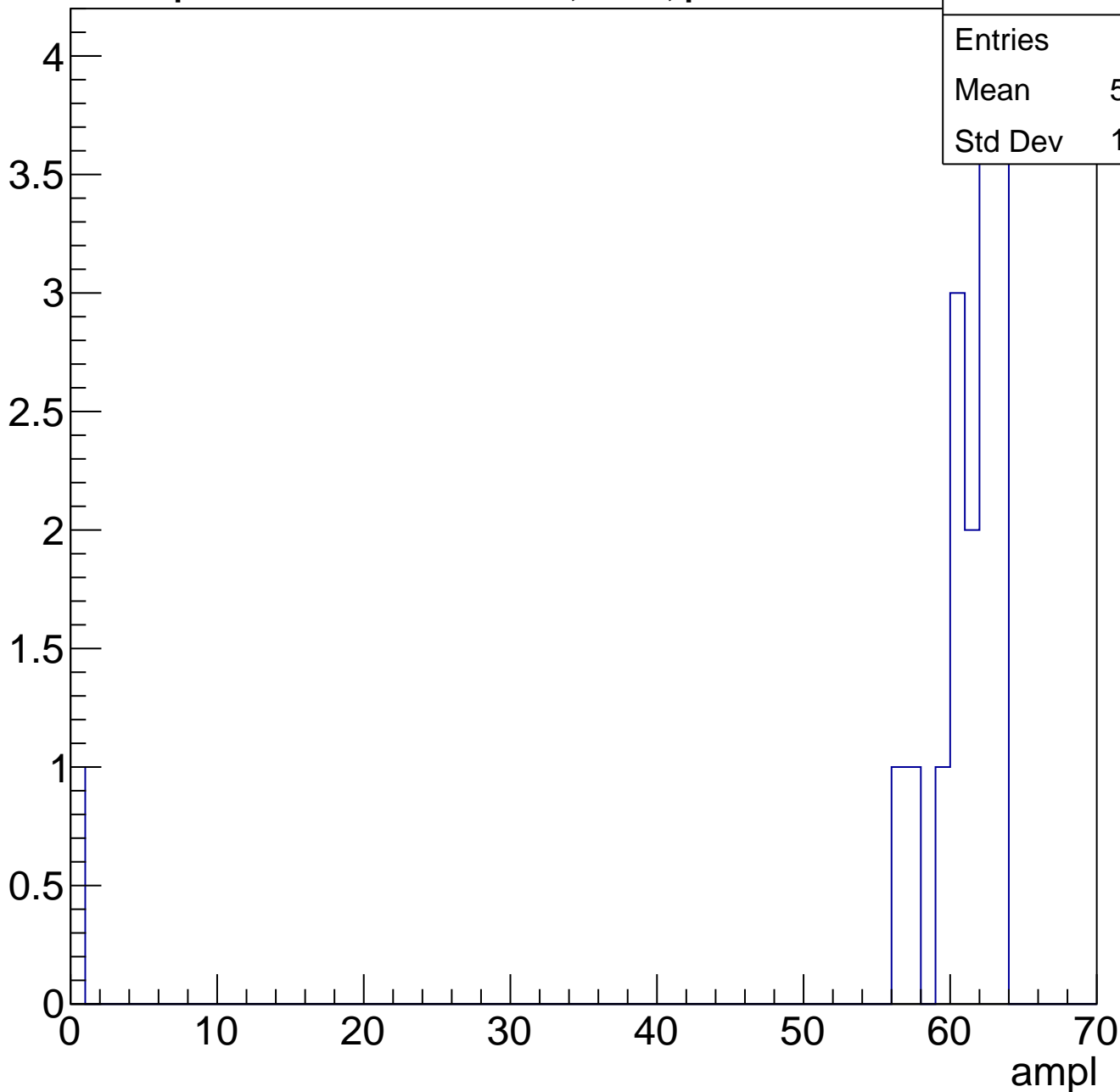
calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U2-ch32, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U2-ch32, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch33, adc0

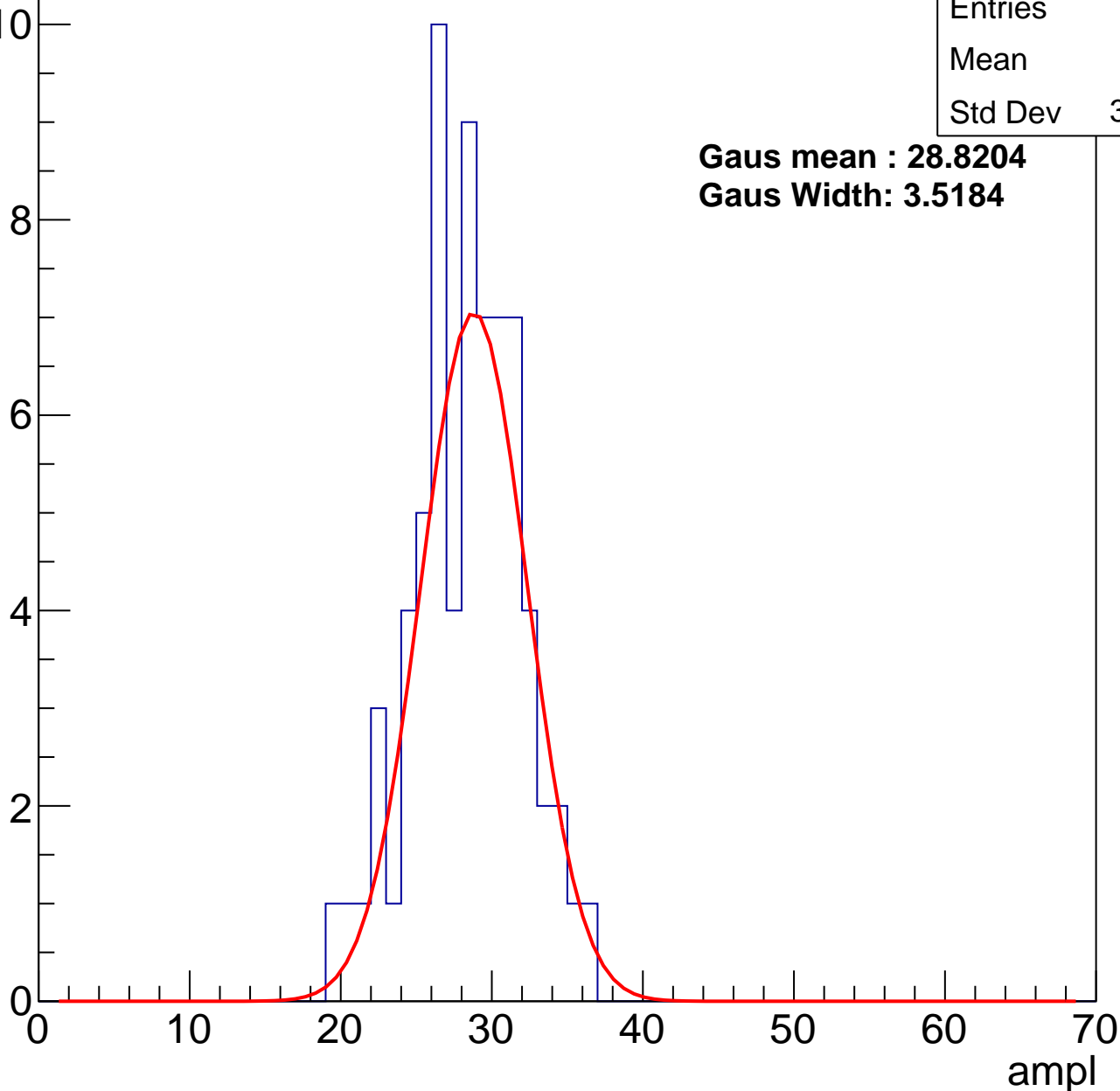
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	27.9
Std Dev	3.538

**Gaus mean : 28.8204**

**Gaus Width: 3.5184**



# B1L103S, U2-ch33, adc1

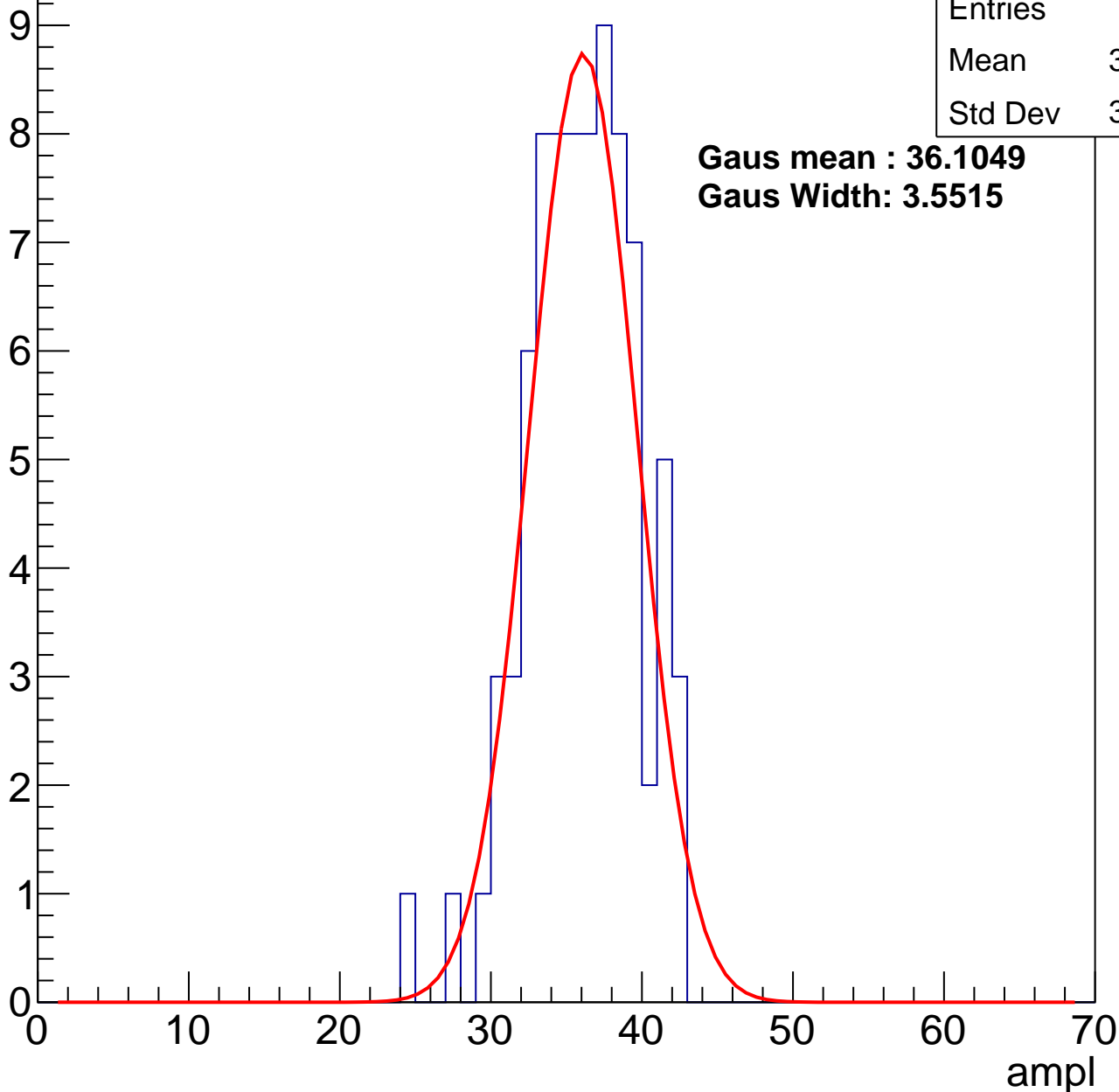
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	81
Mean	35.56
Std Dev	3.545

**Gaus mean : 36.1049**

**Gaus Width: 3.5515**

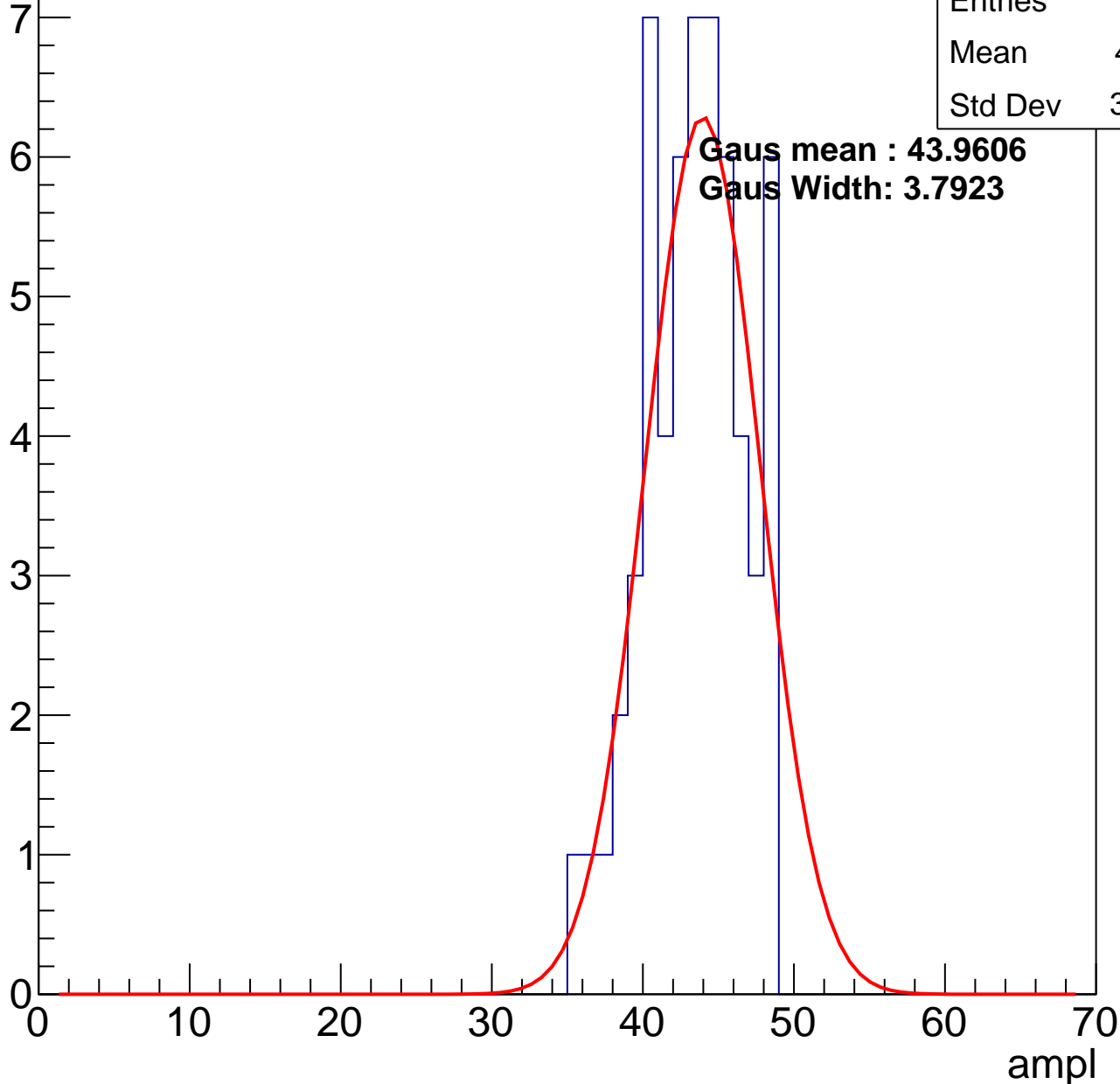


# B1L103S, U2-ch33, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	42.91
Std Dev	3.207

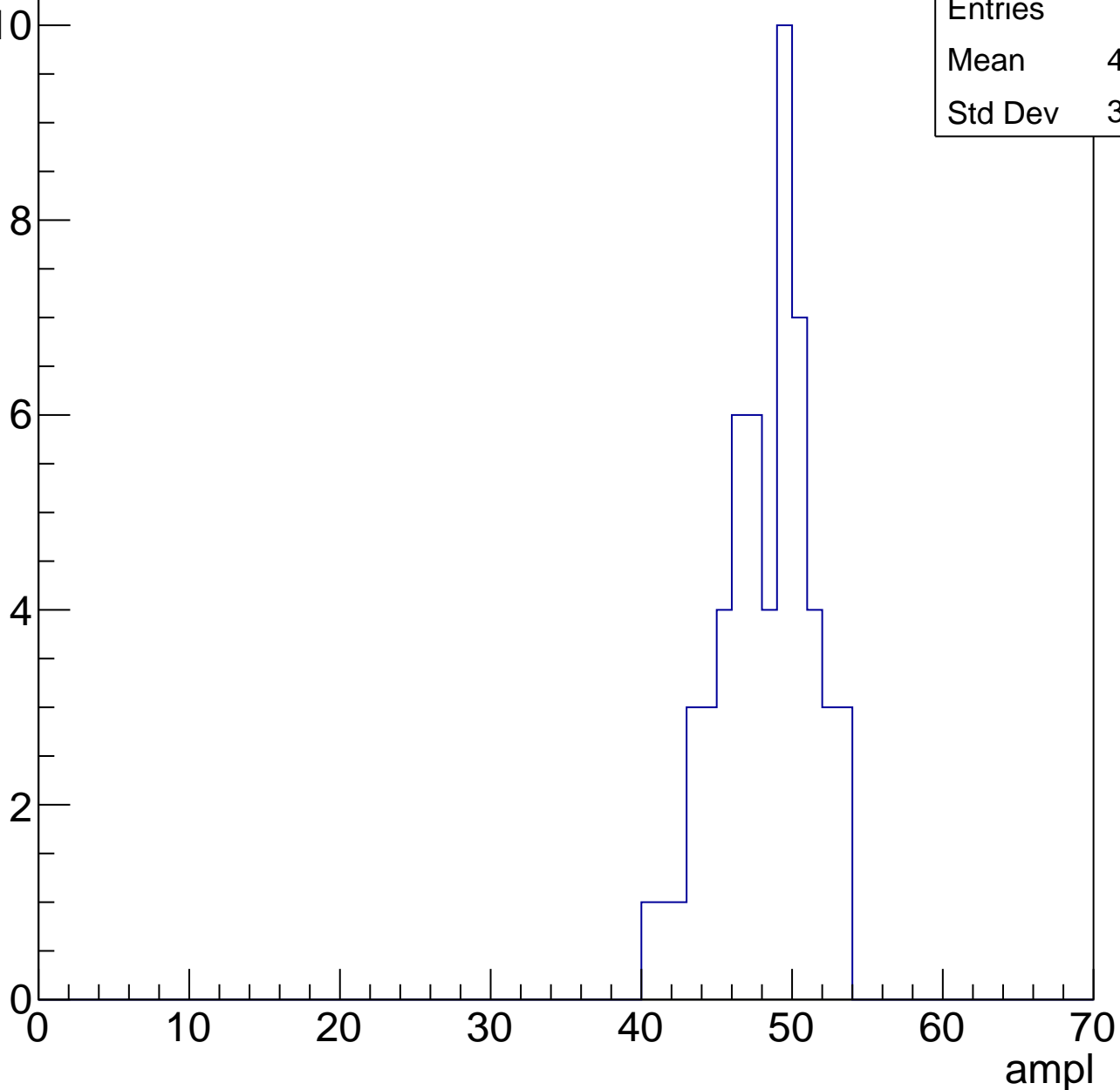


# B1L103S, U2-ch33, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	47.73
Std Dev	3.079

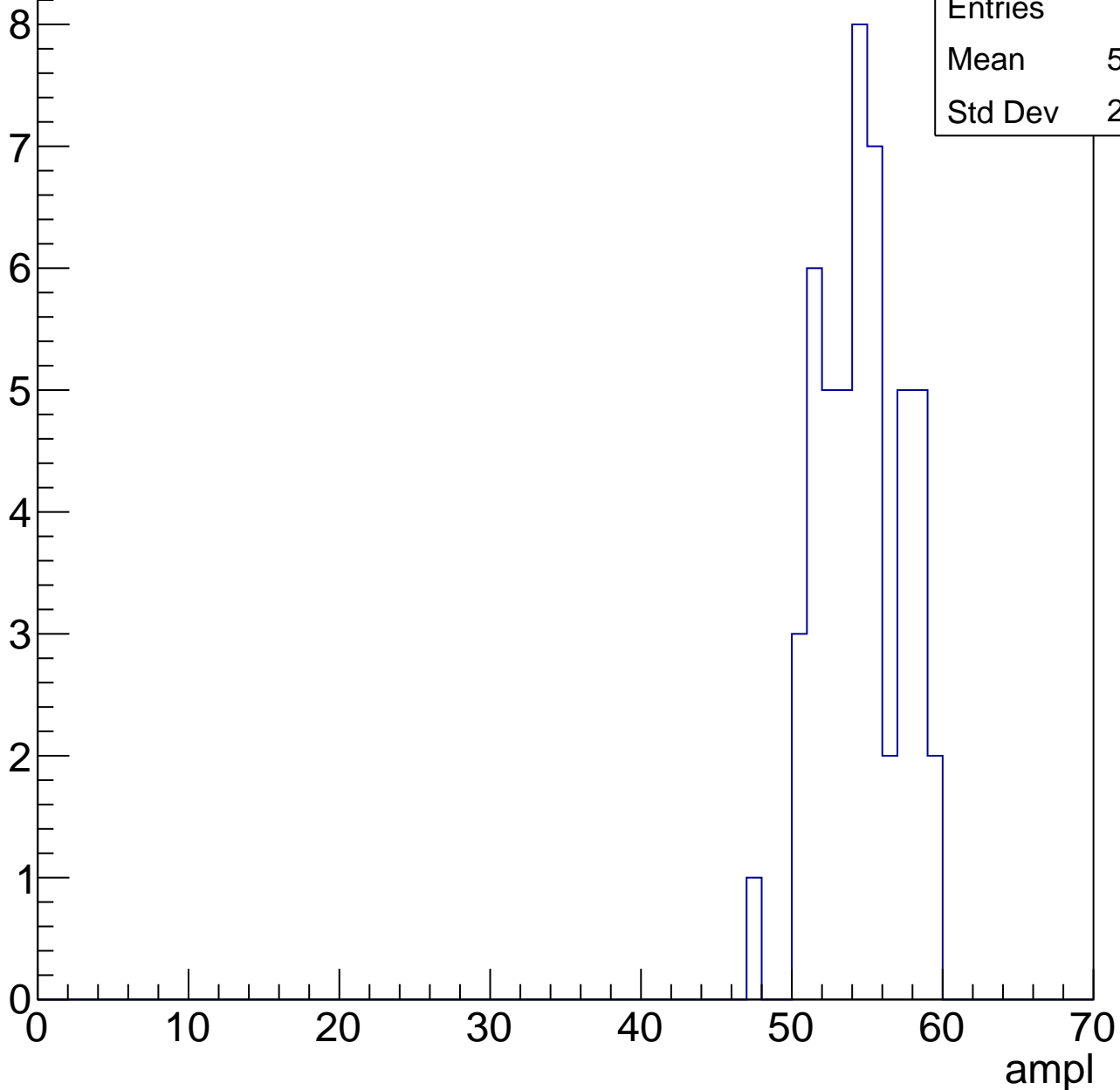


# B1L103S, U2-ch33, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	54.08
Std Dev	2.732

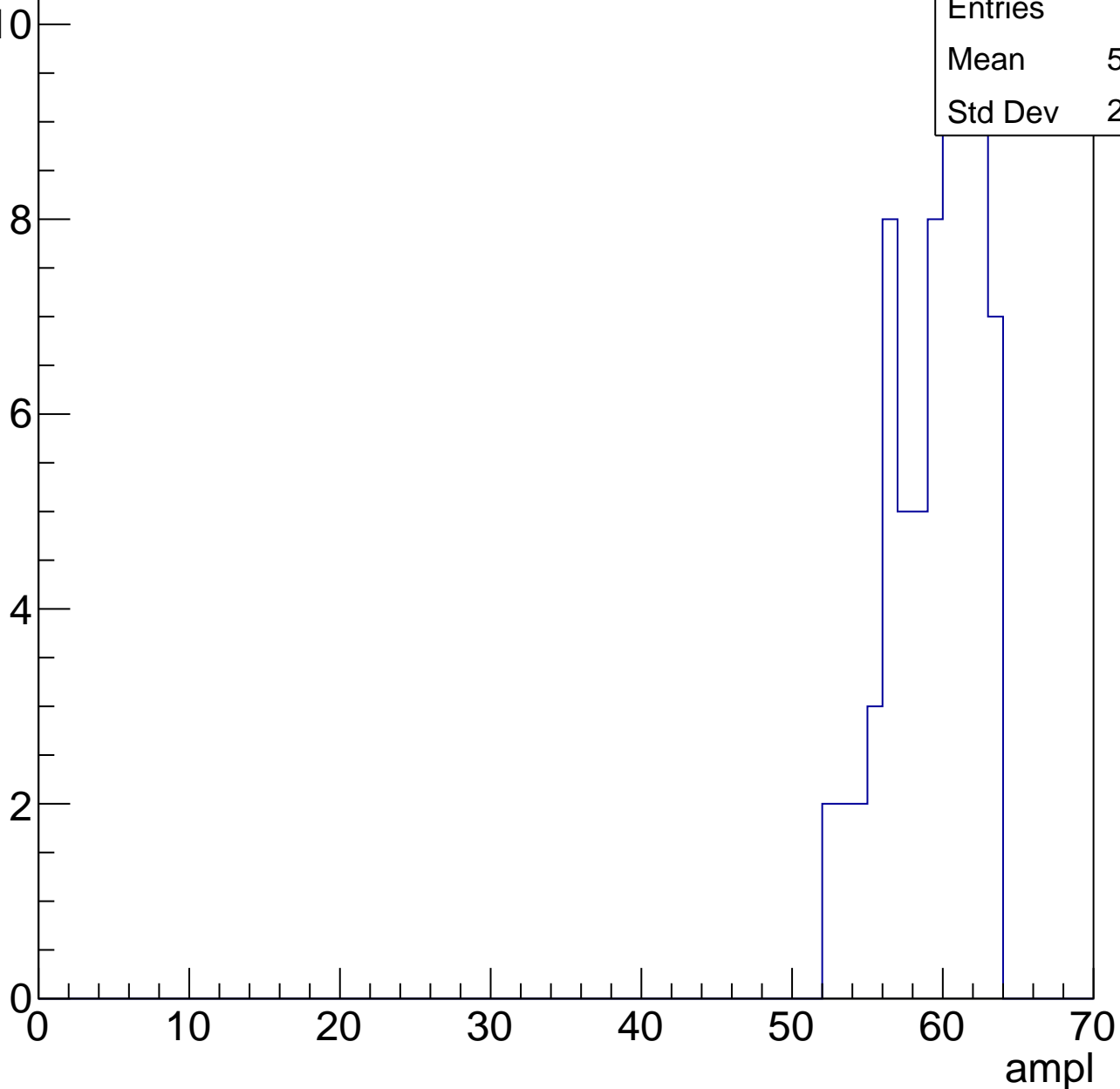


# B1L103S, U2-ch33, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

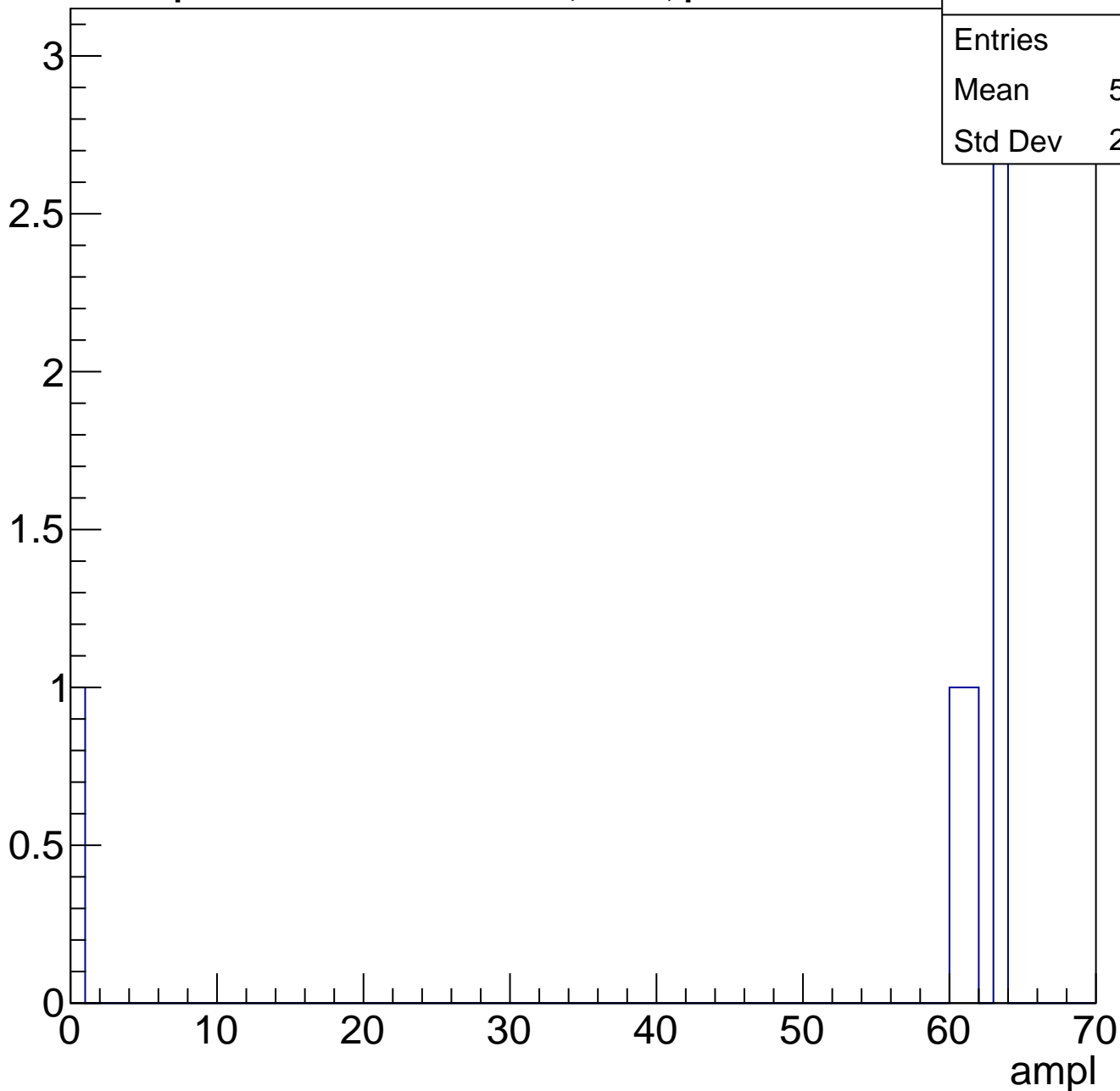
Entries	70
Mean	58.97
Std Dev	2.957



# B1L103S, U2-ch33, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U2-ch33, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U2-ch34, adc0

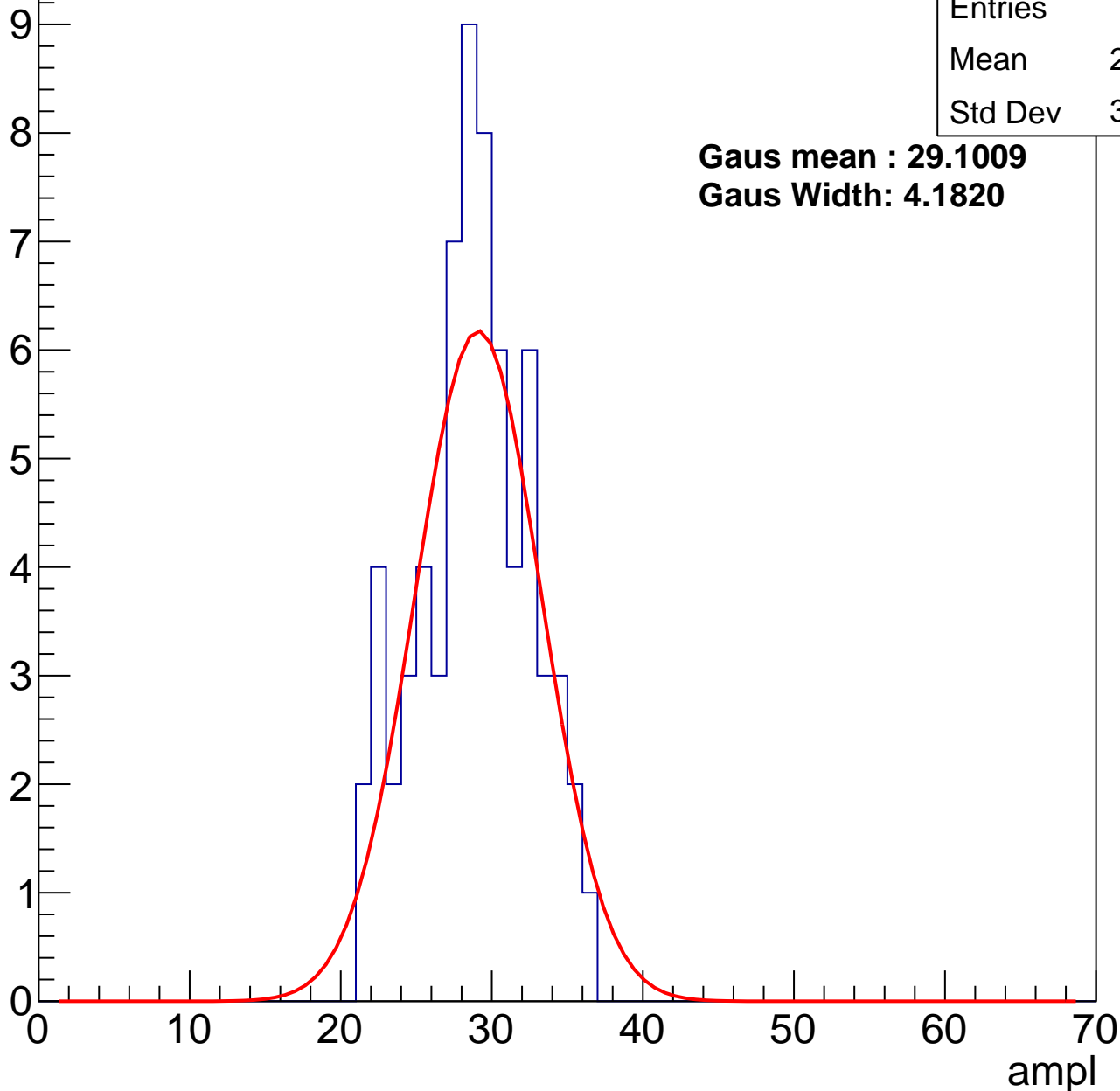
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	28.39
Std Dev	3.653

**Gaus mean : 29.1009**

**Gaus Width: 4.1820**



# B1L103S, U2-ch34, adc1

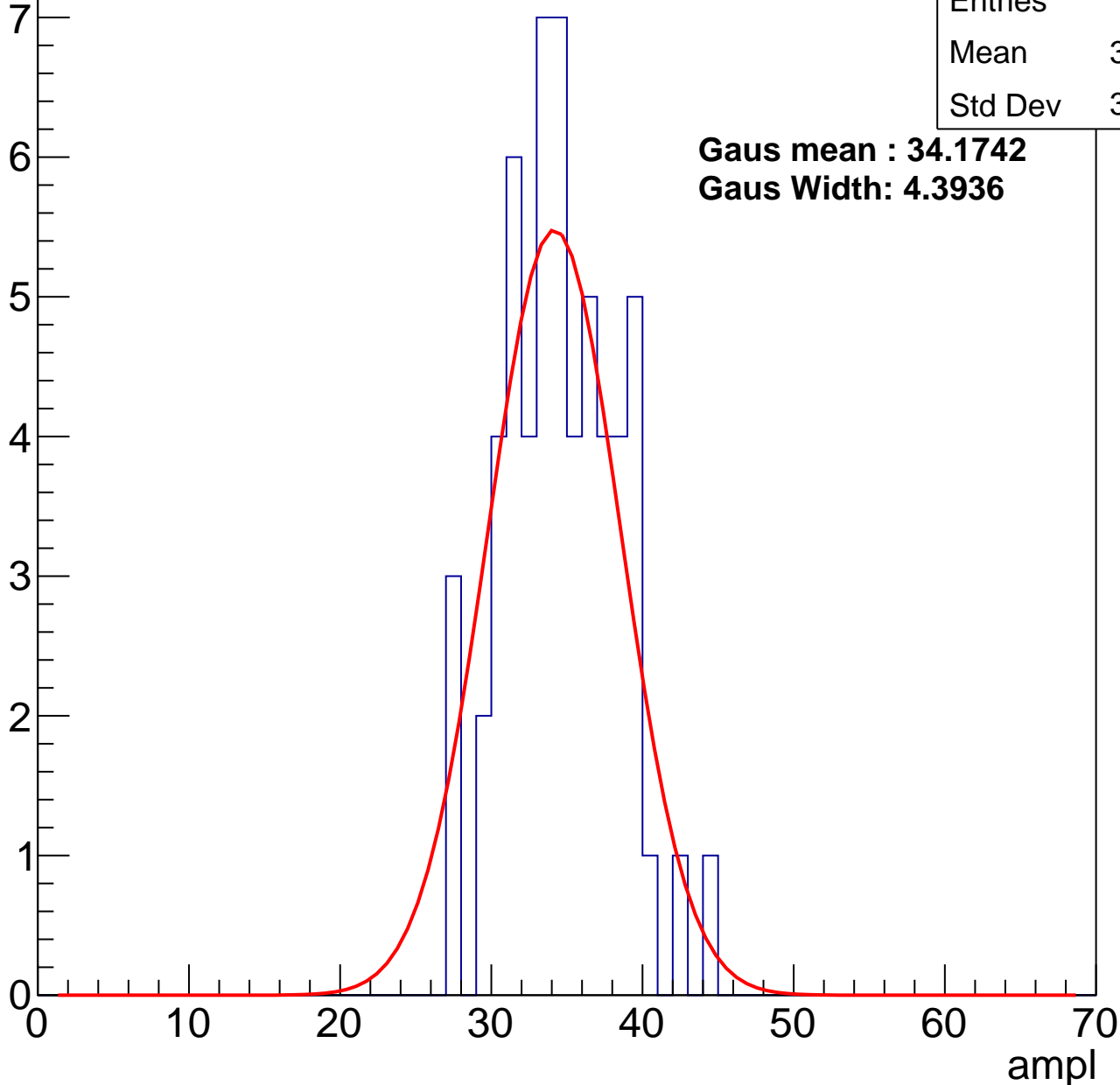
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	34.19
Std Dev	3.679

**Gaus mean : 34.1742**

**Gaus Width: 4.3936**



# B1L103S, U2-ch34, adc2

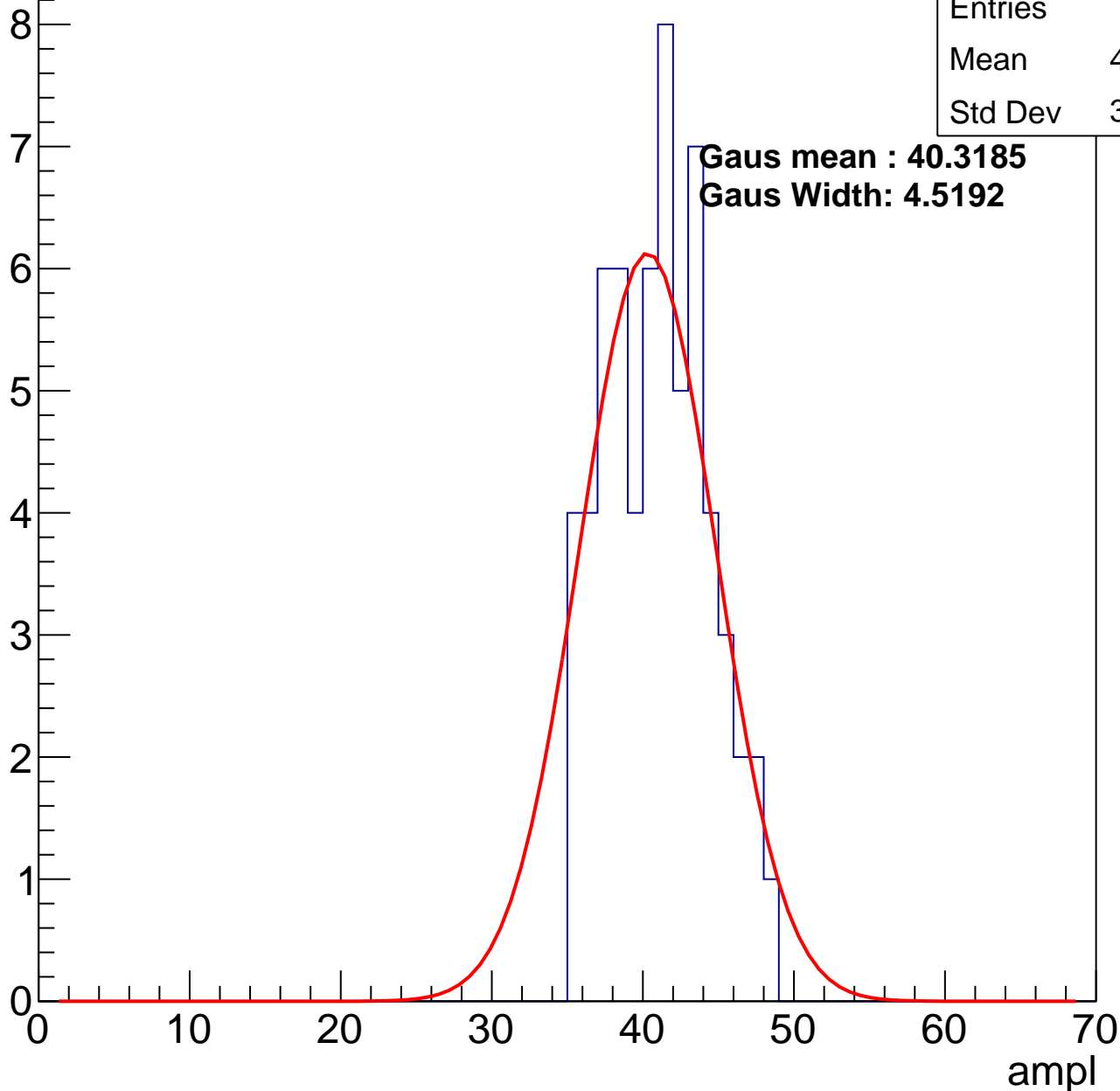
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	40.55
Std Dev	3.339

**Gaus mean : 40.3185**

**Gaus Width: 4.5192**

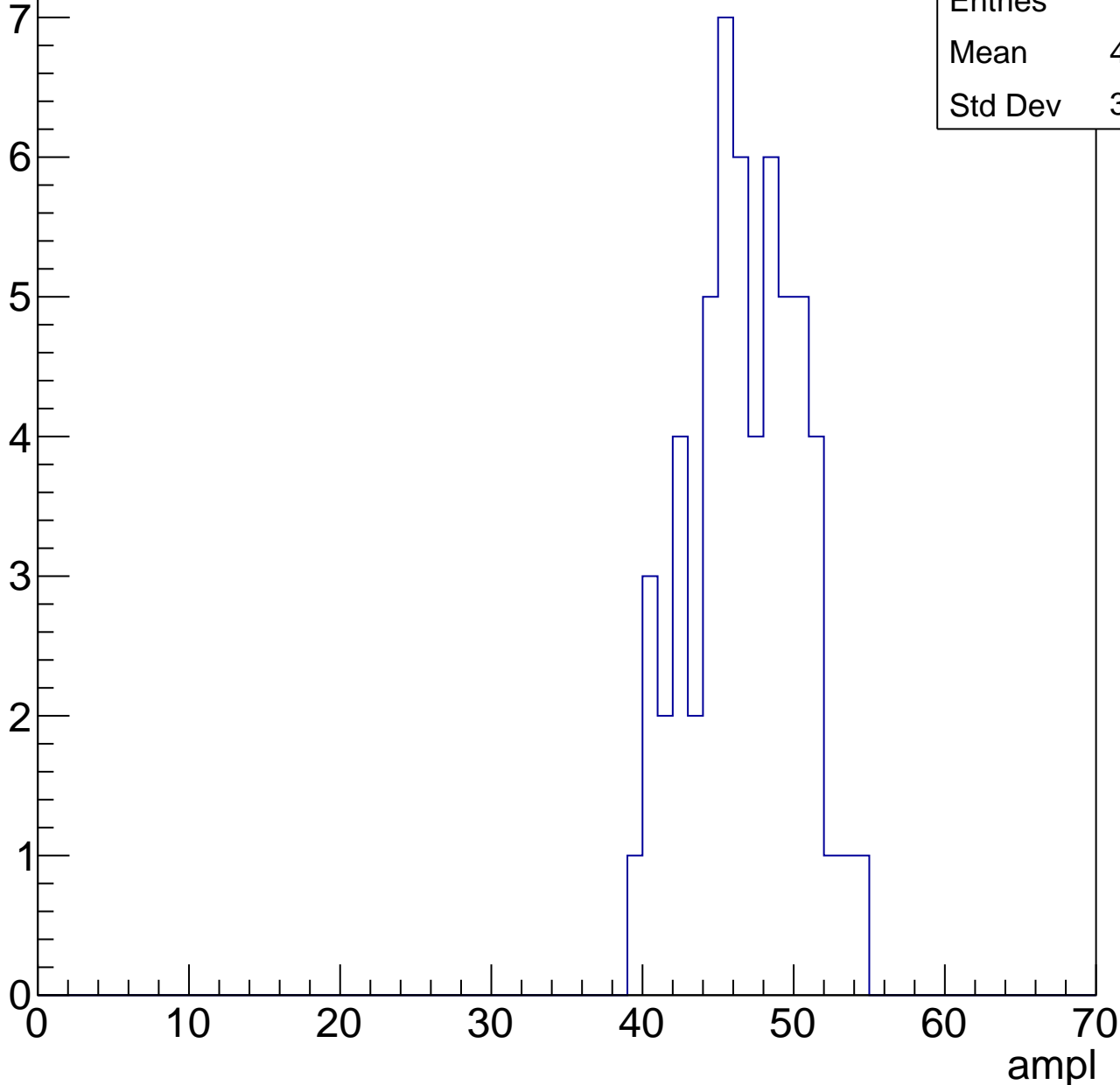


# B1L103S, U2-ch34, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	46.32
Std Dev	3.535

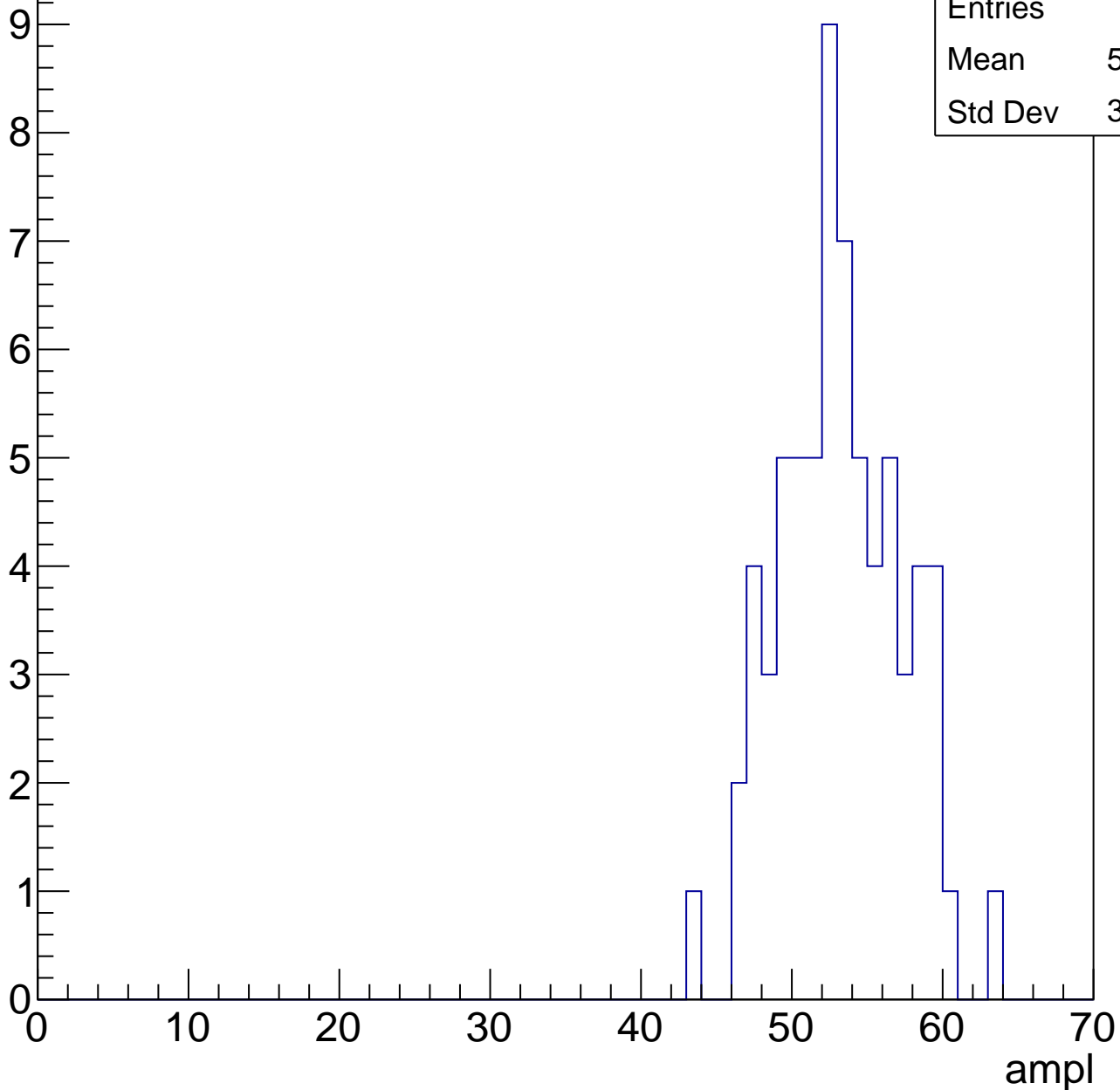


# B1L103S, U2-ch34, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

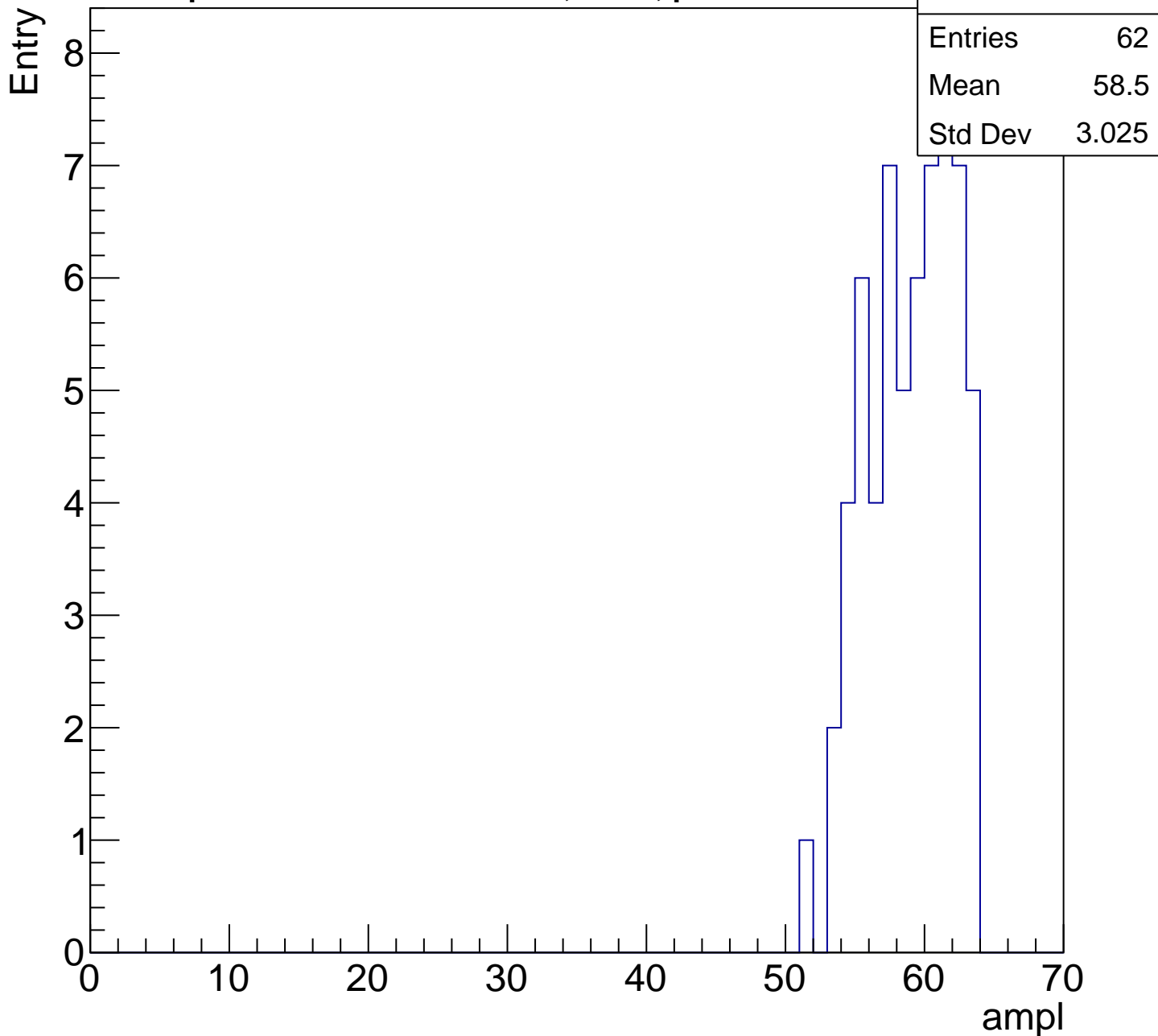
Entry

Entries	68
Mean	52.76
Std Dev	3.975



# B1L103S, U2-ch34, adc5

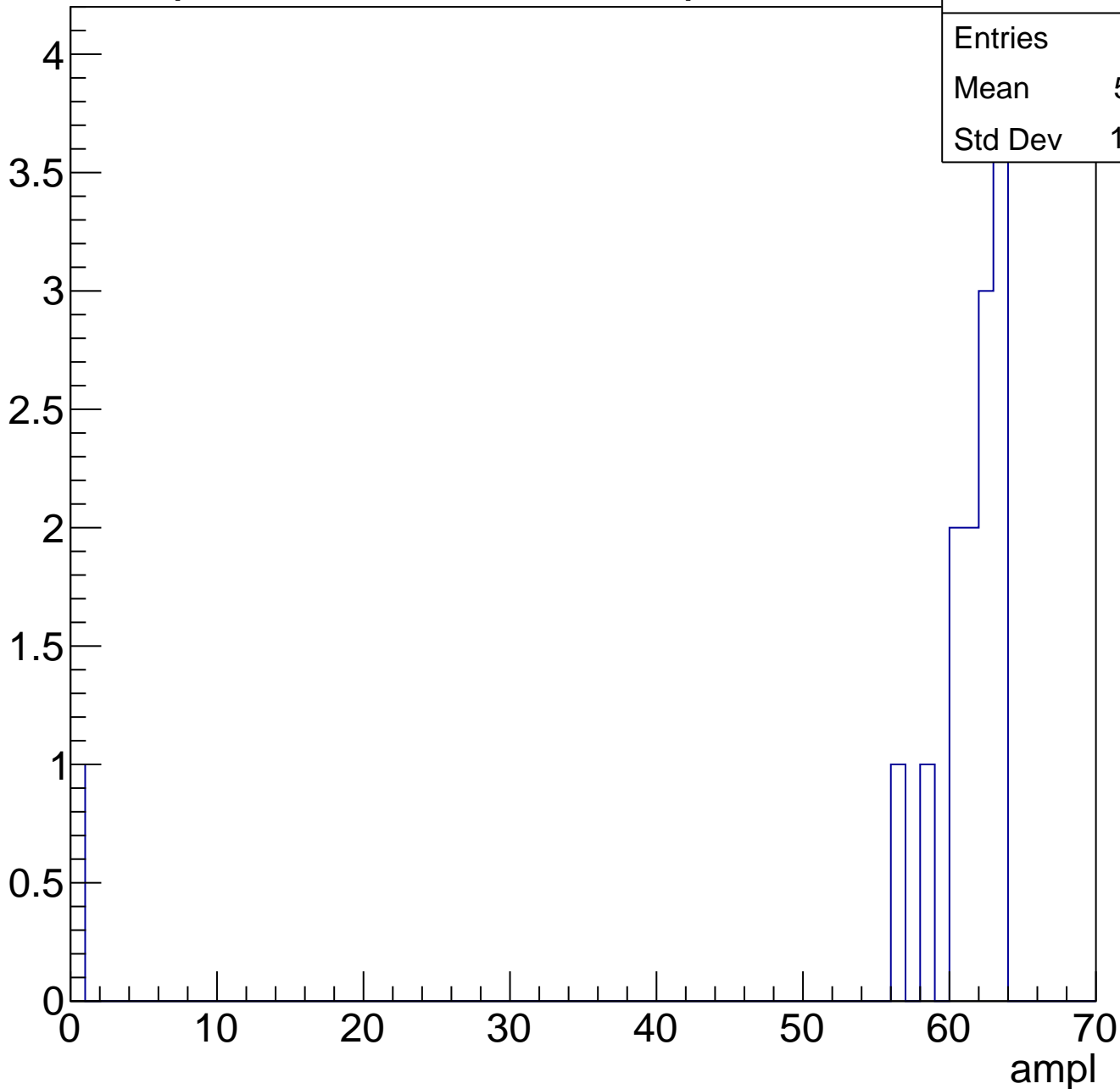
calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U2-ch34, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U2-ch34, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	9.5
Std Dev	9.5

# B1L103S, U2-ch35, adc0

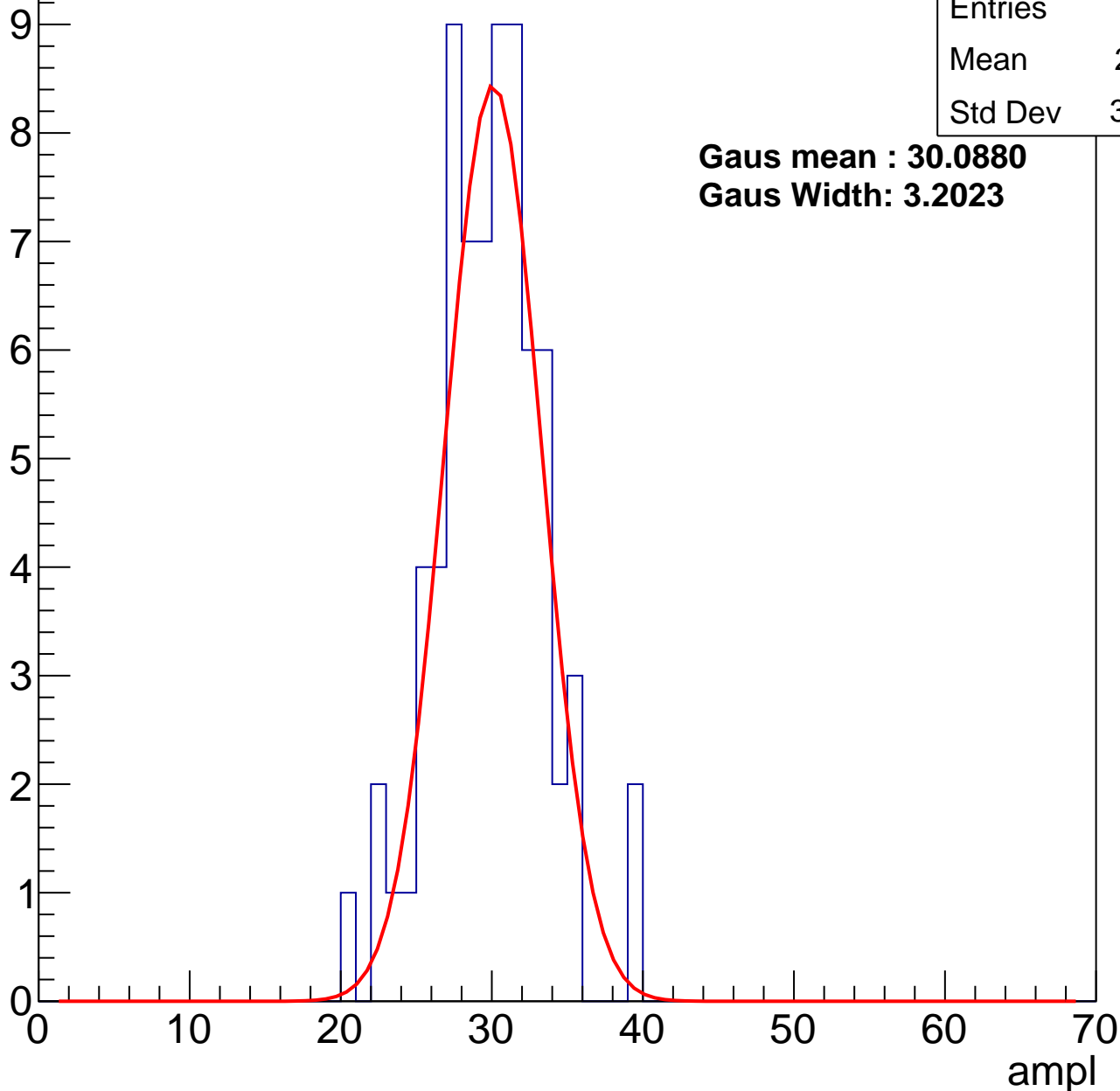
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	29.41
Std Dev	3.557

**Gaus mean : 30.0880**

**Gaus Width: 3.2023**



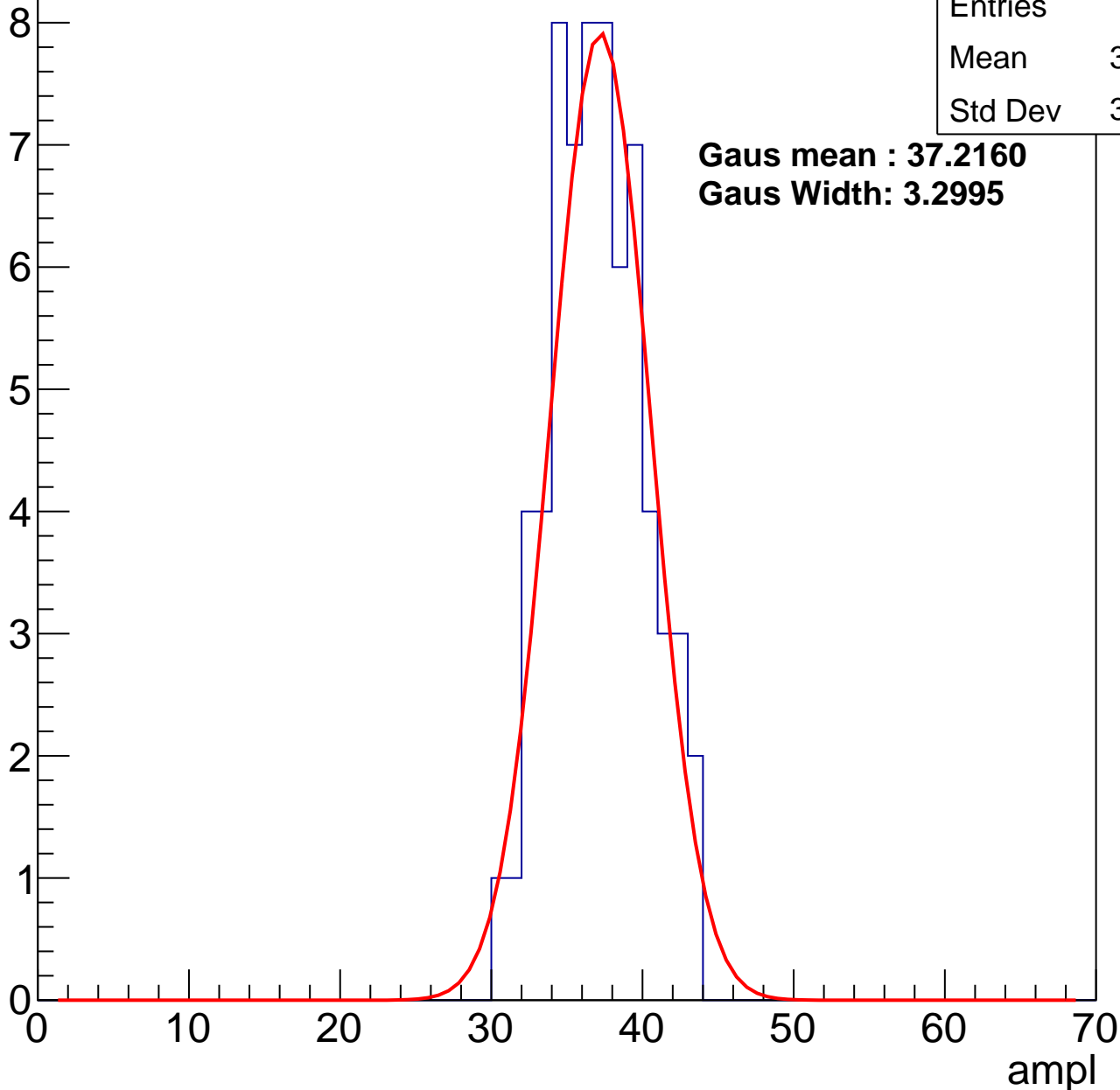
# B1L103S, U2-ch35, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	36.64
Std Dev	3.048

**Gaus mean : 37.2160**  
**Gaus Width: 3.2995**



# B1L103S, U2-ch35, adc2

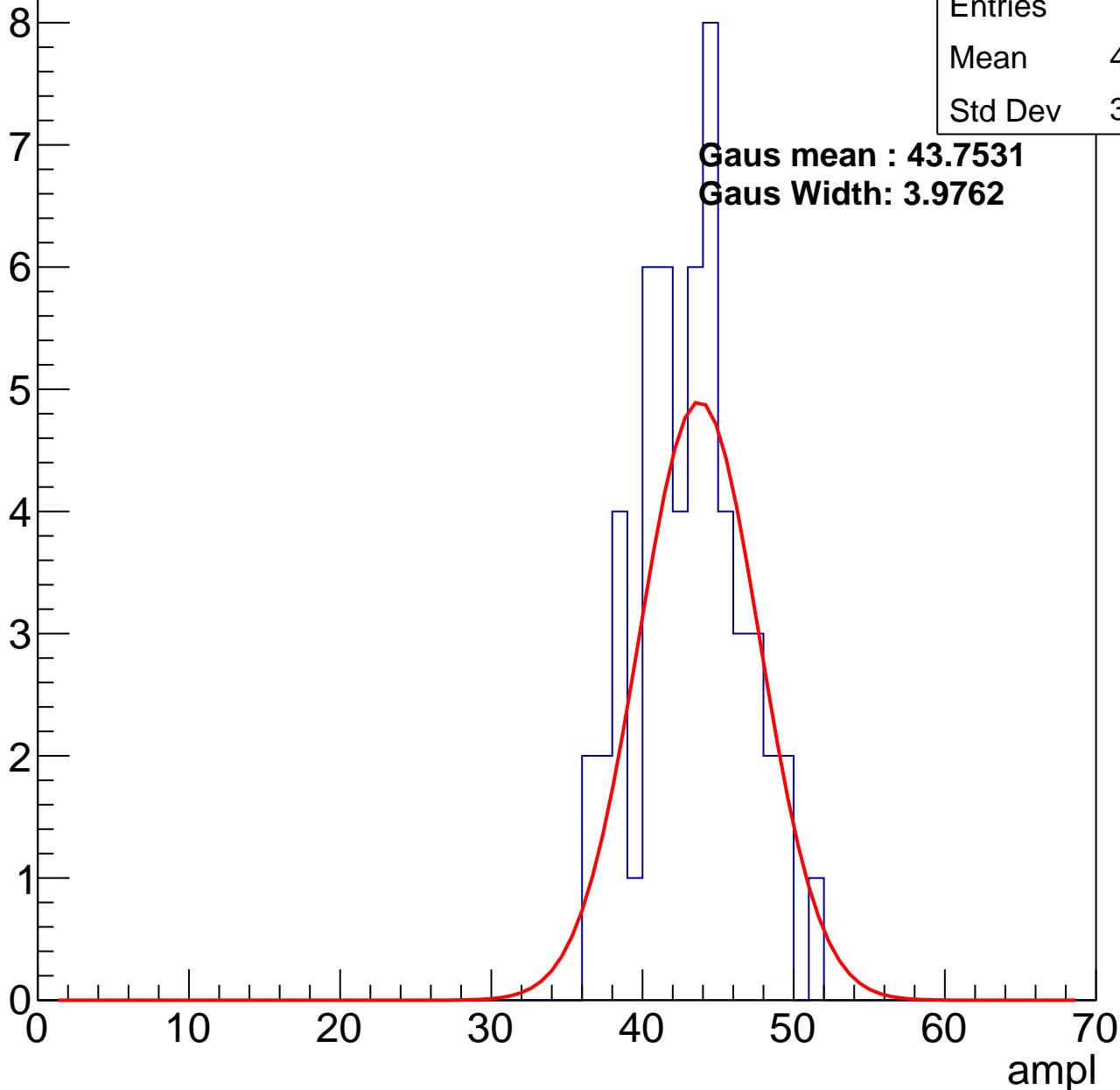
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	42.69
Std Dev	3.463

**Gaus mean : 43.7531**

**Gaus Width: 3.9762**

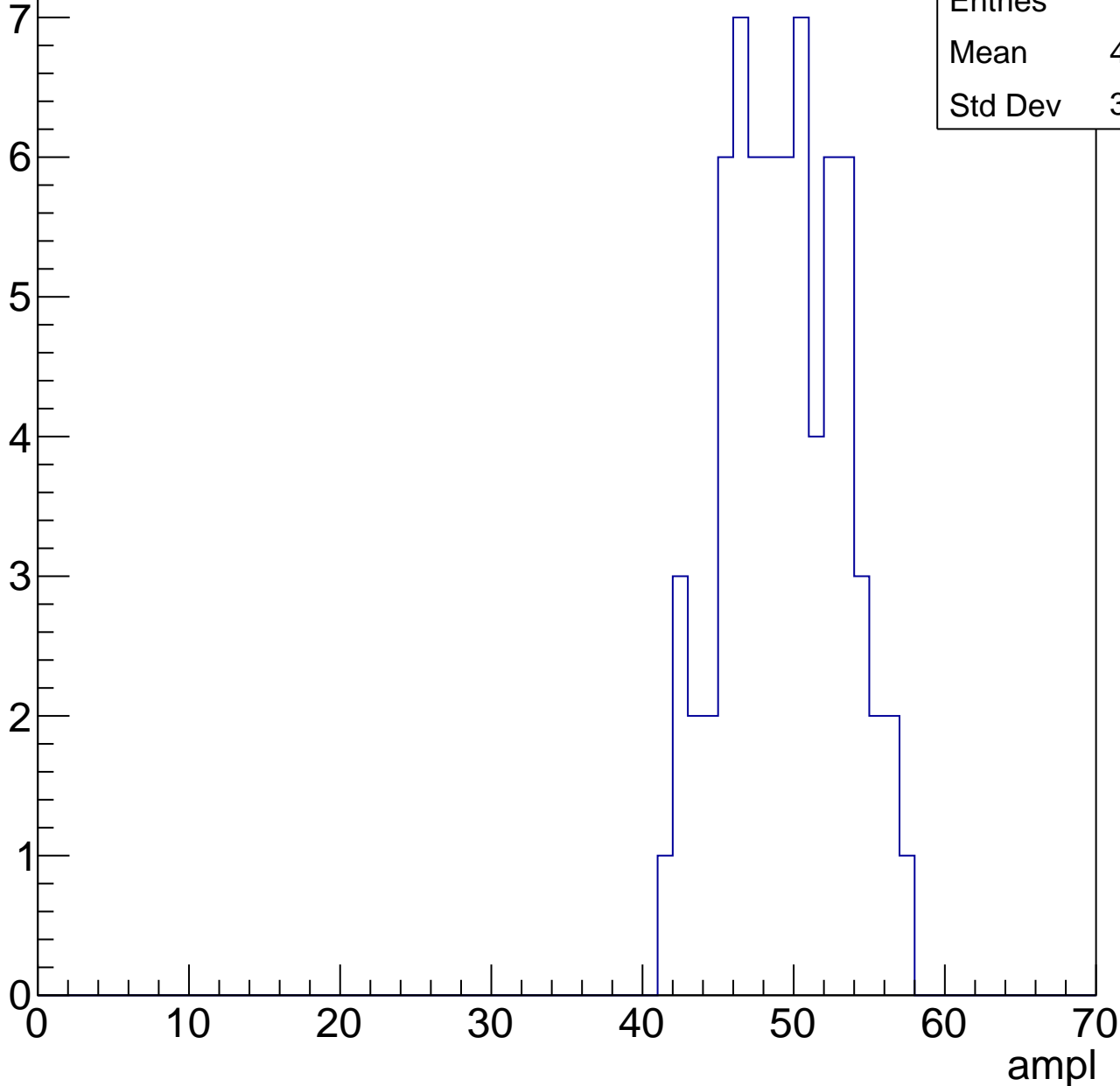


# B1L103S, U2-ch35, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	48.89
Std Dev	3.785

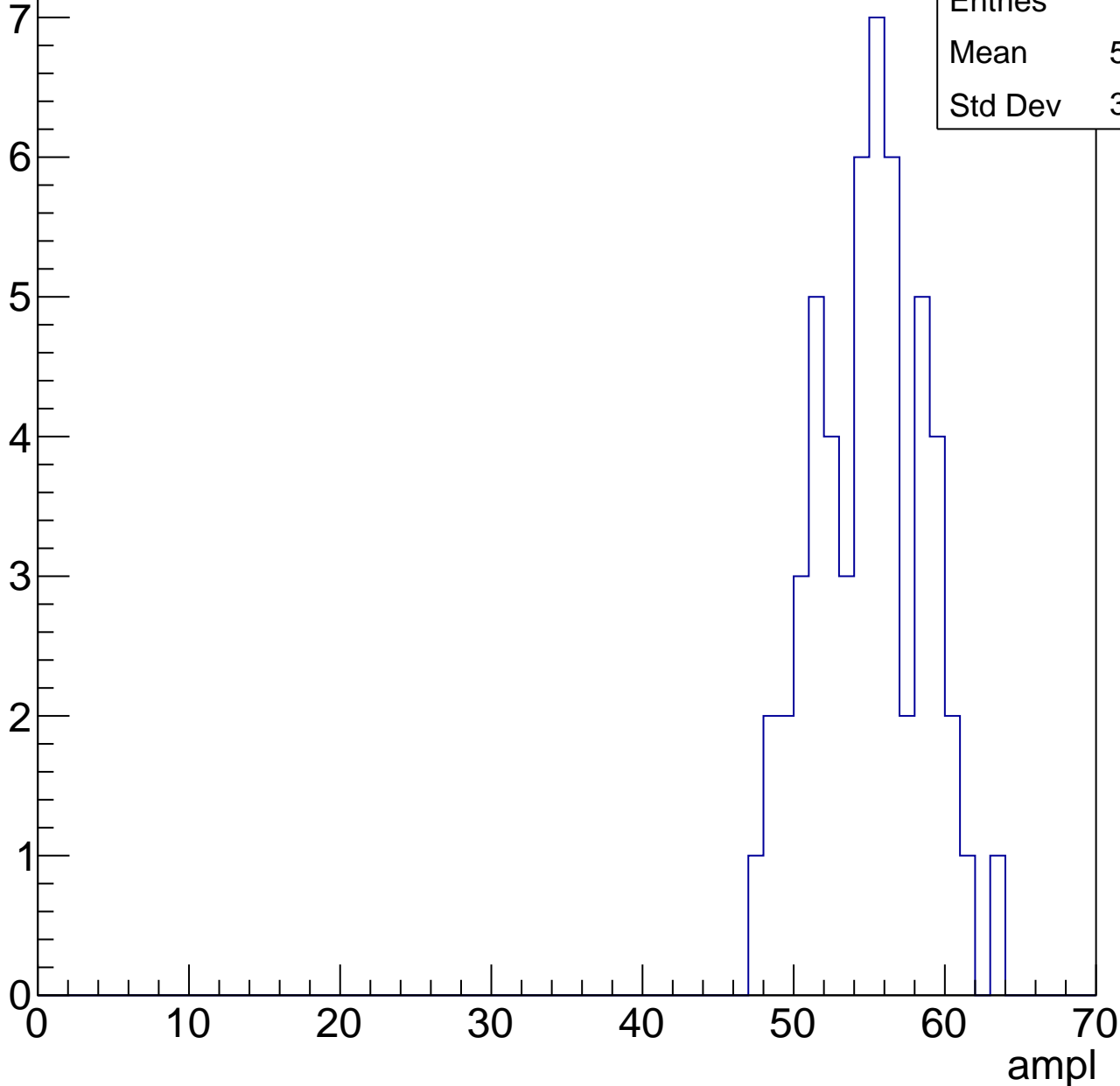


# B1L103S, U2-ch35, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

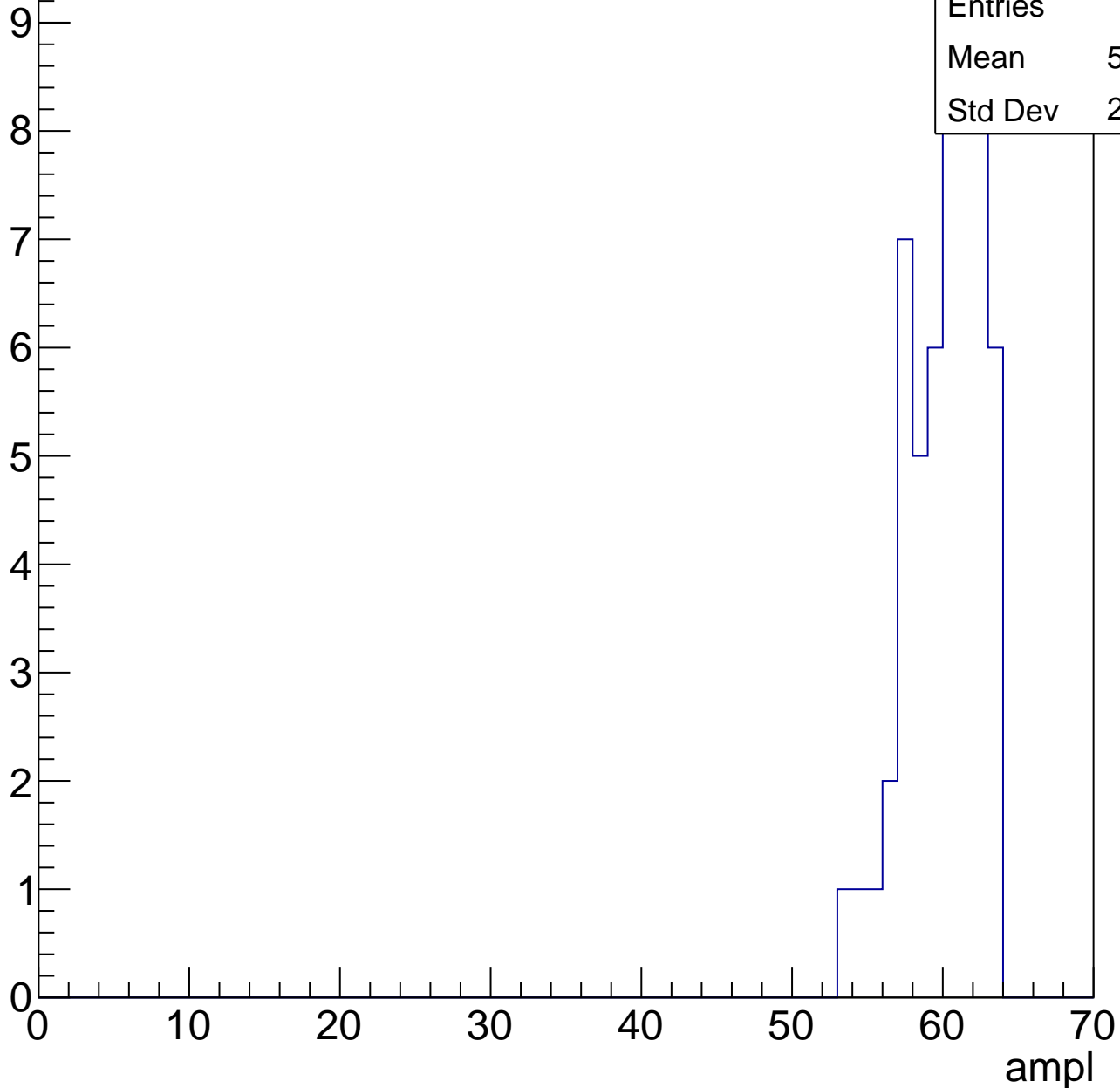
Entries	54
Mean	54.48
Std Dev	3.604



# B1L103S, U2-ch35, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

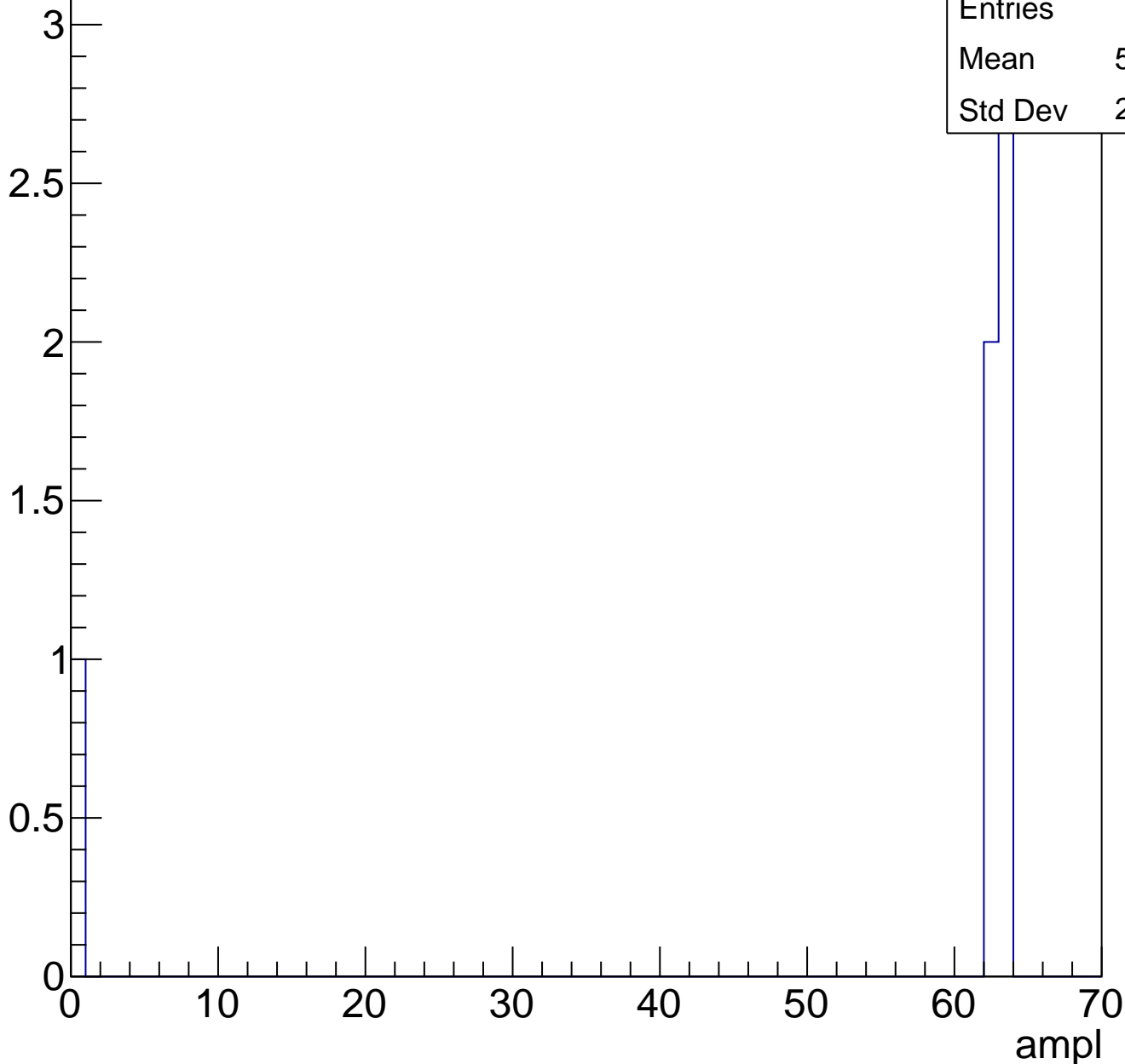


Entries	54
Mean	59.63
Std Dev	2.429

# B1L103S, U2-ch35, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U2-ch35, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch36, adc0

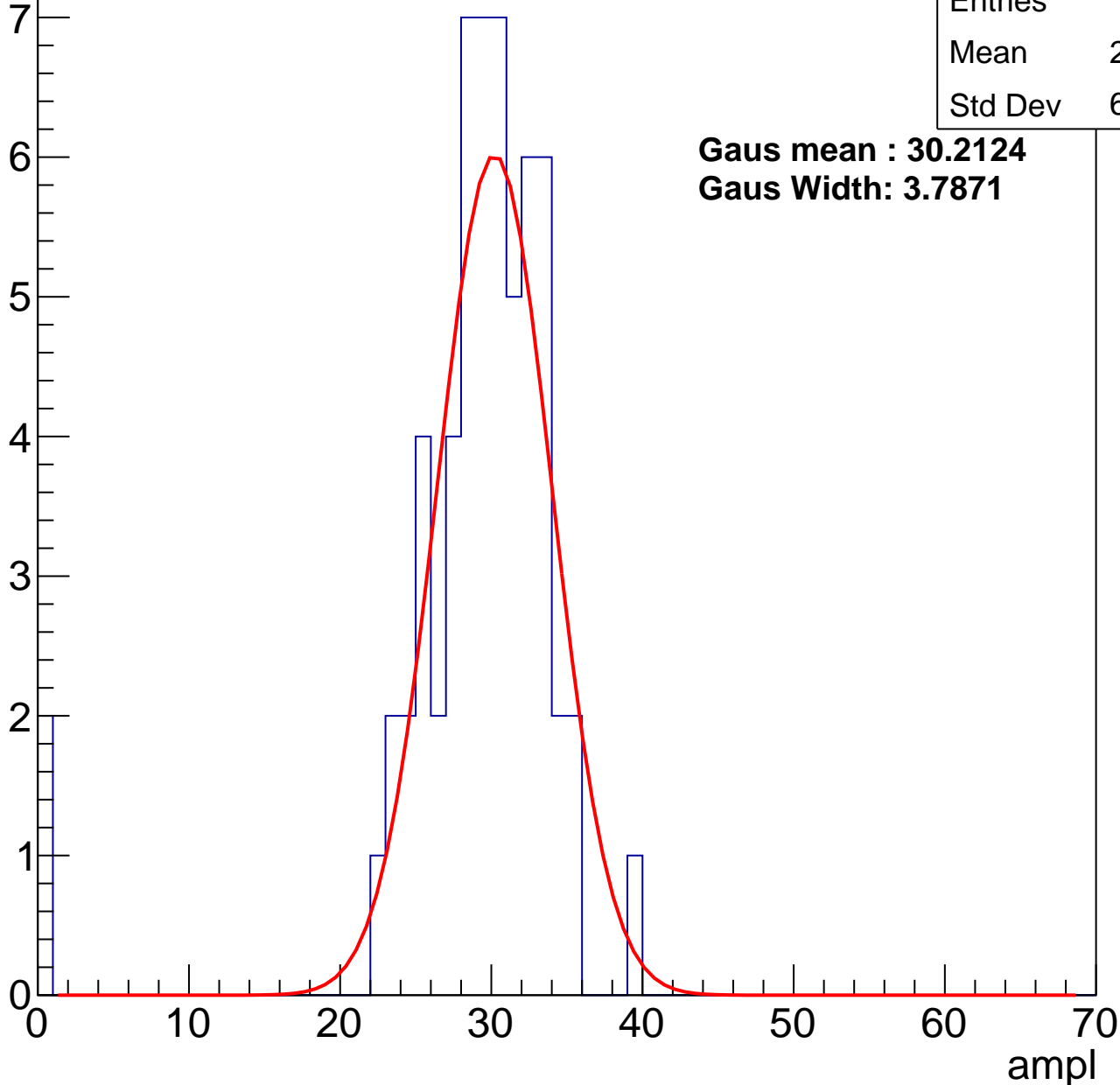
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	28.45
Std Dev	6.243

**Gaus mean : 30.2124**

**Gaus Width: 3.7871**



# B1L103S, U2-ch36, adc1

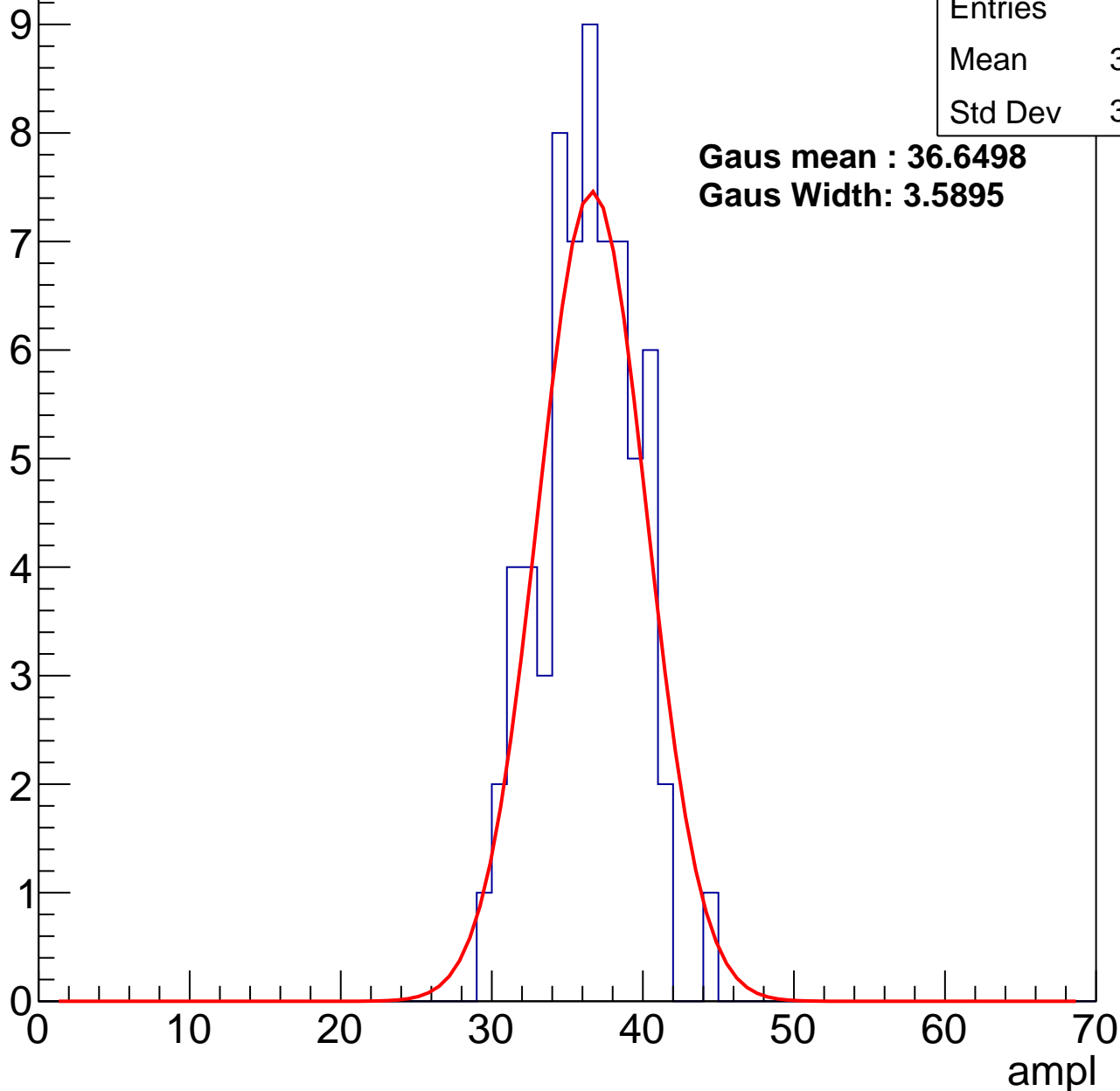
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	35.86
Std Dev	3.113

**Gaus mean : 36.6498**

**Gaus Width: 3.5895**



# B1L103S, U2-ch36, adc2

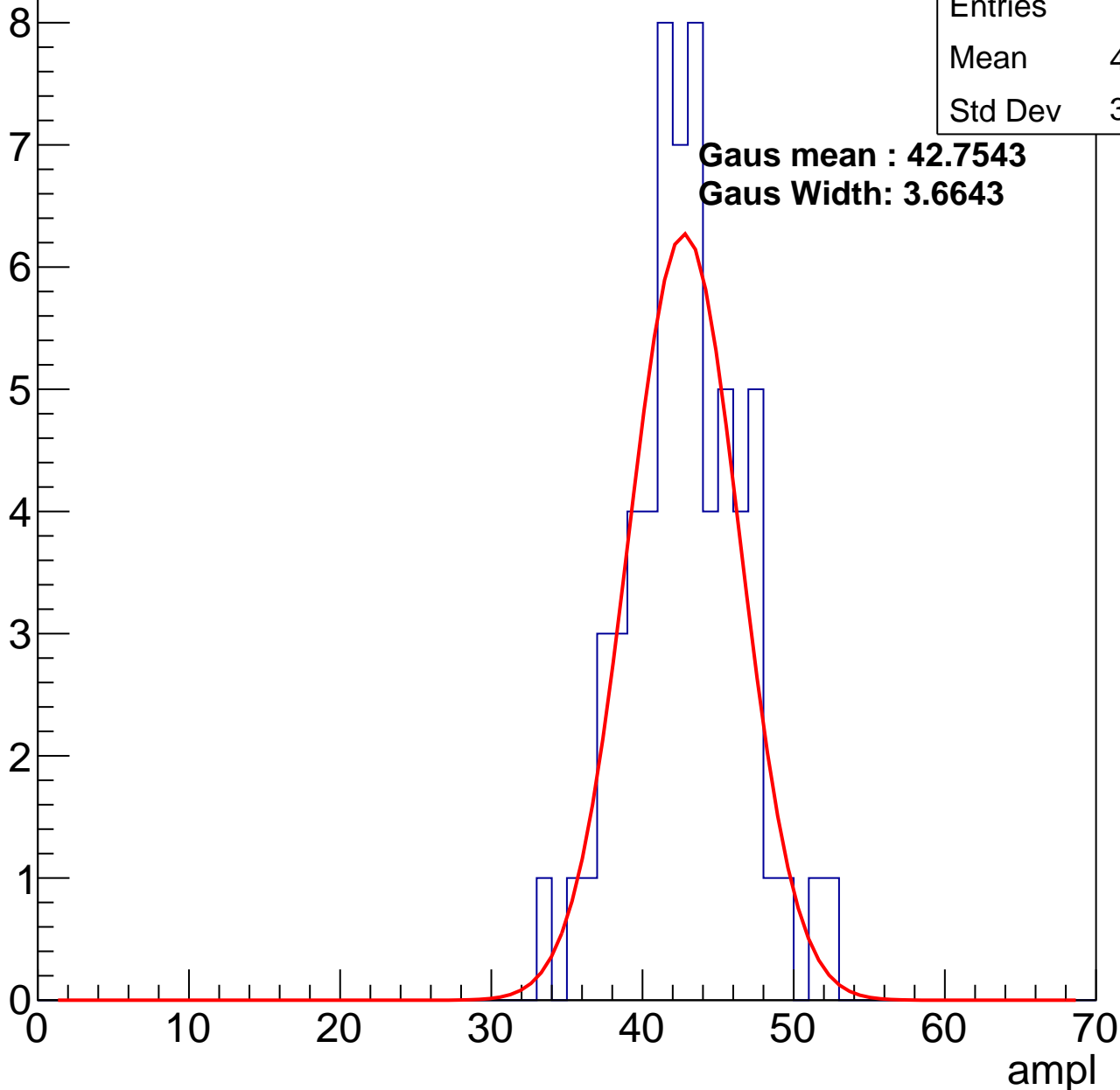
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	42.44
Std Dev	3.727

**Gaus mean : 42.7543**

**Gaus Width: 3.6643**

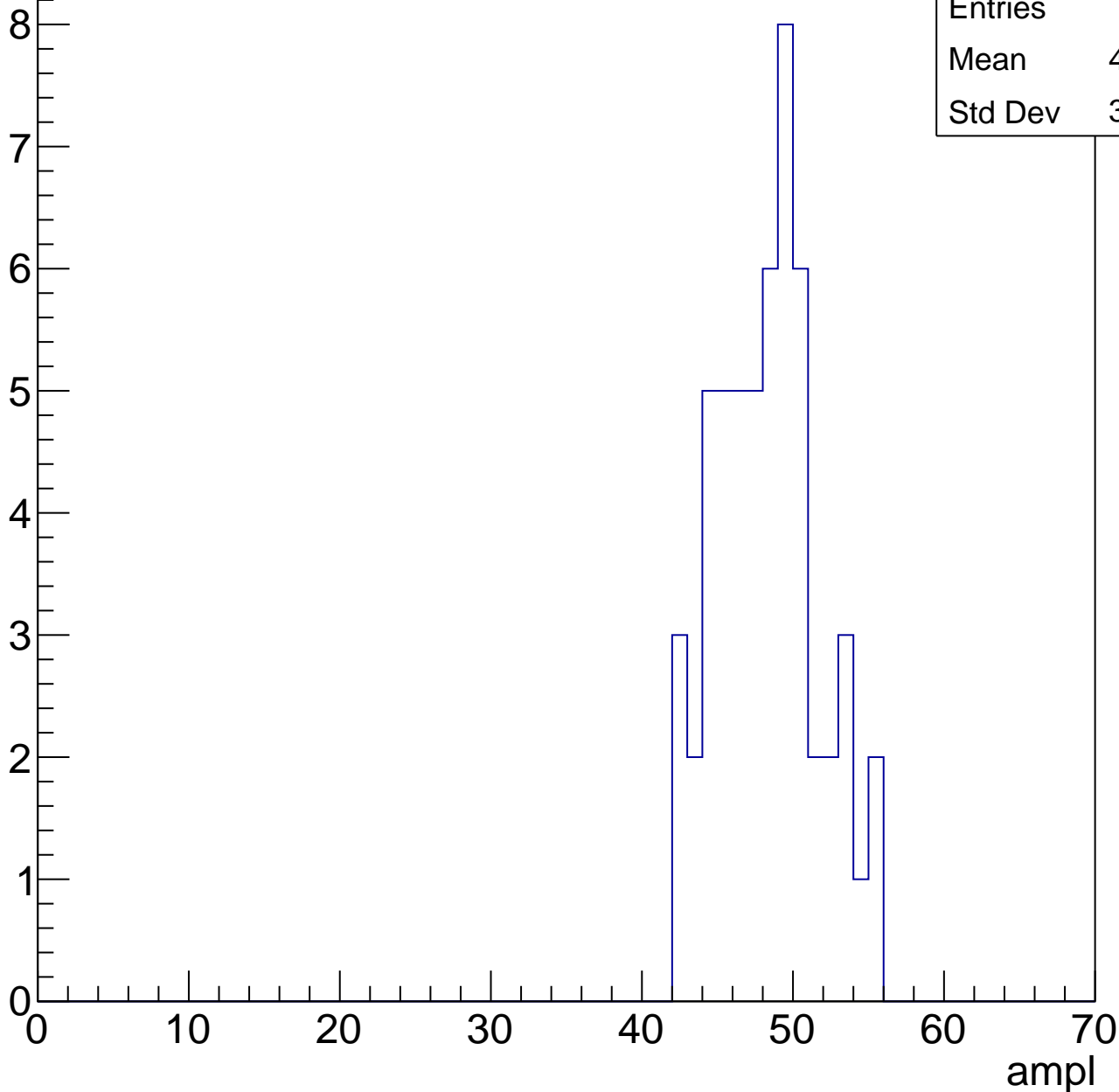


# B1L103S, U2-ch36, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	47.84
Std Dev	3.296

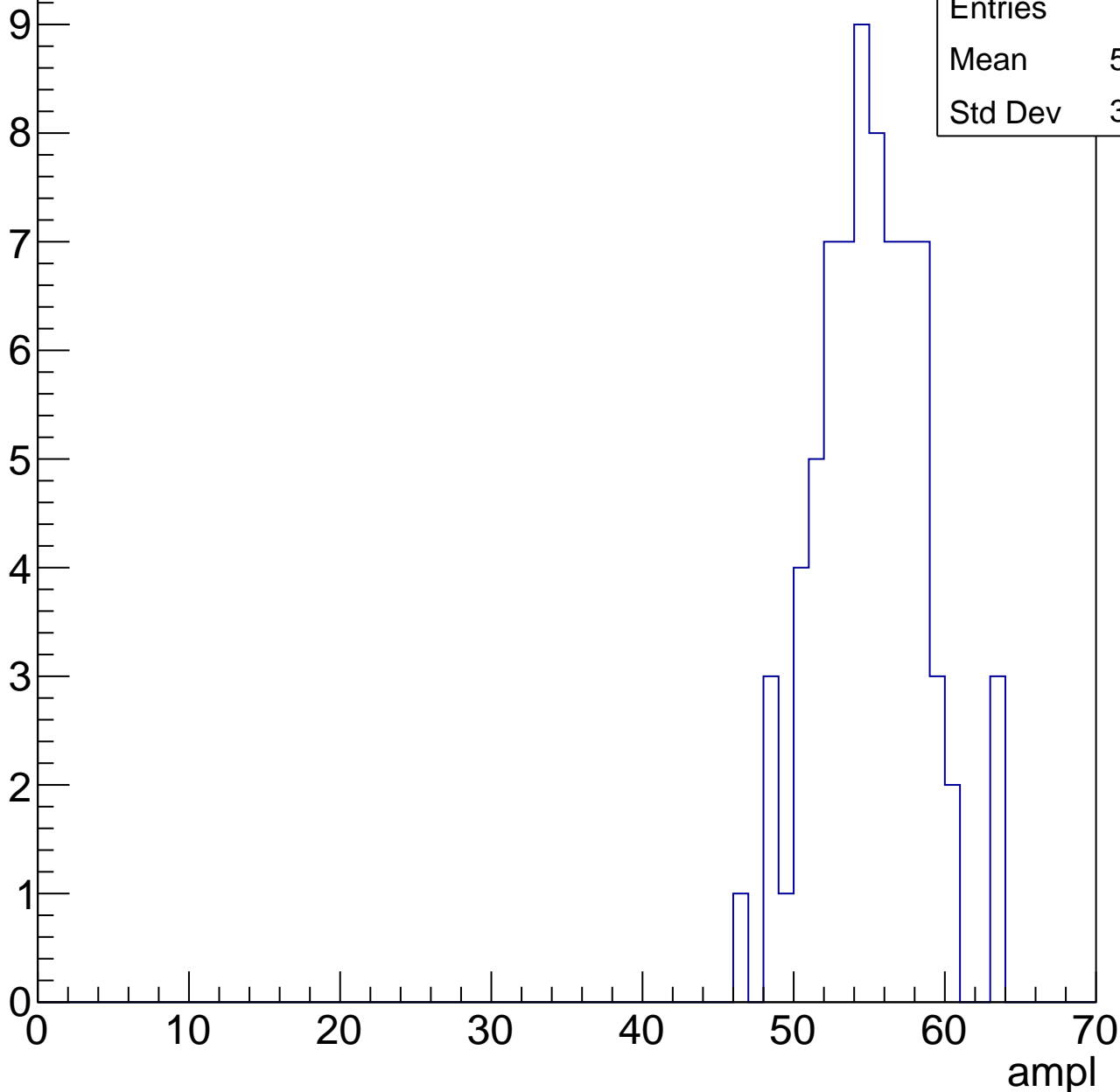


# B1L103S, U2-ch36, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

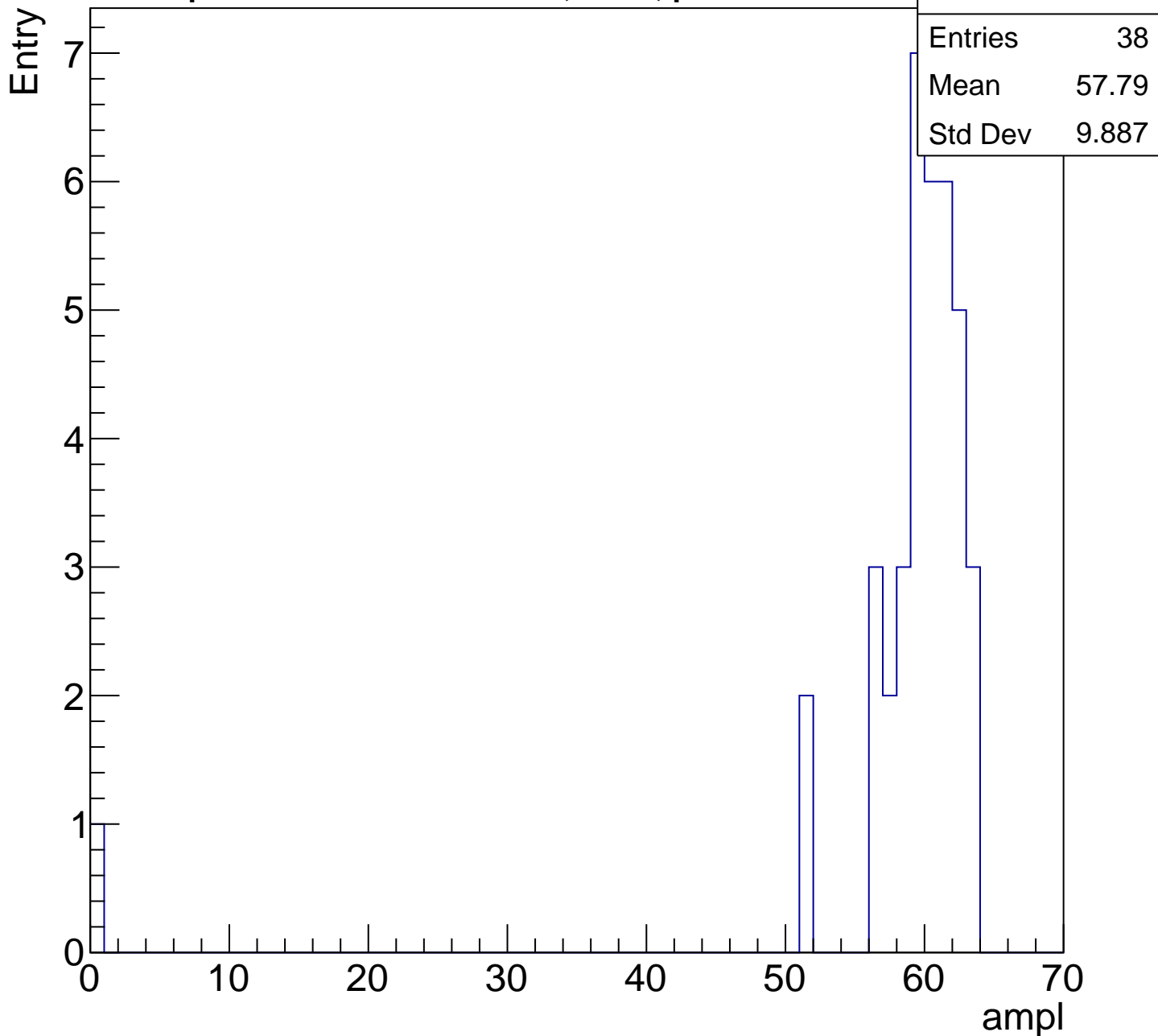
Entry

Entries	74
Mean	54.57
Std Dev	3.522



# B1L103S, U2-ch36, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

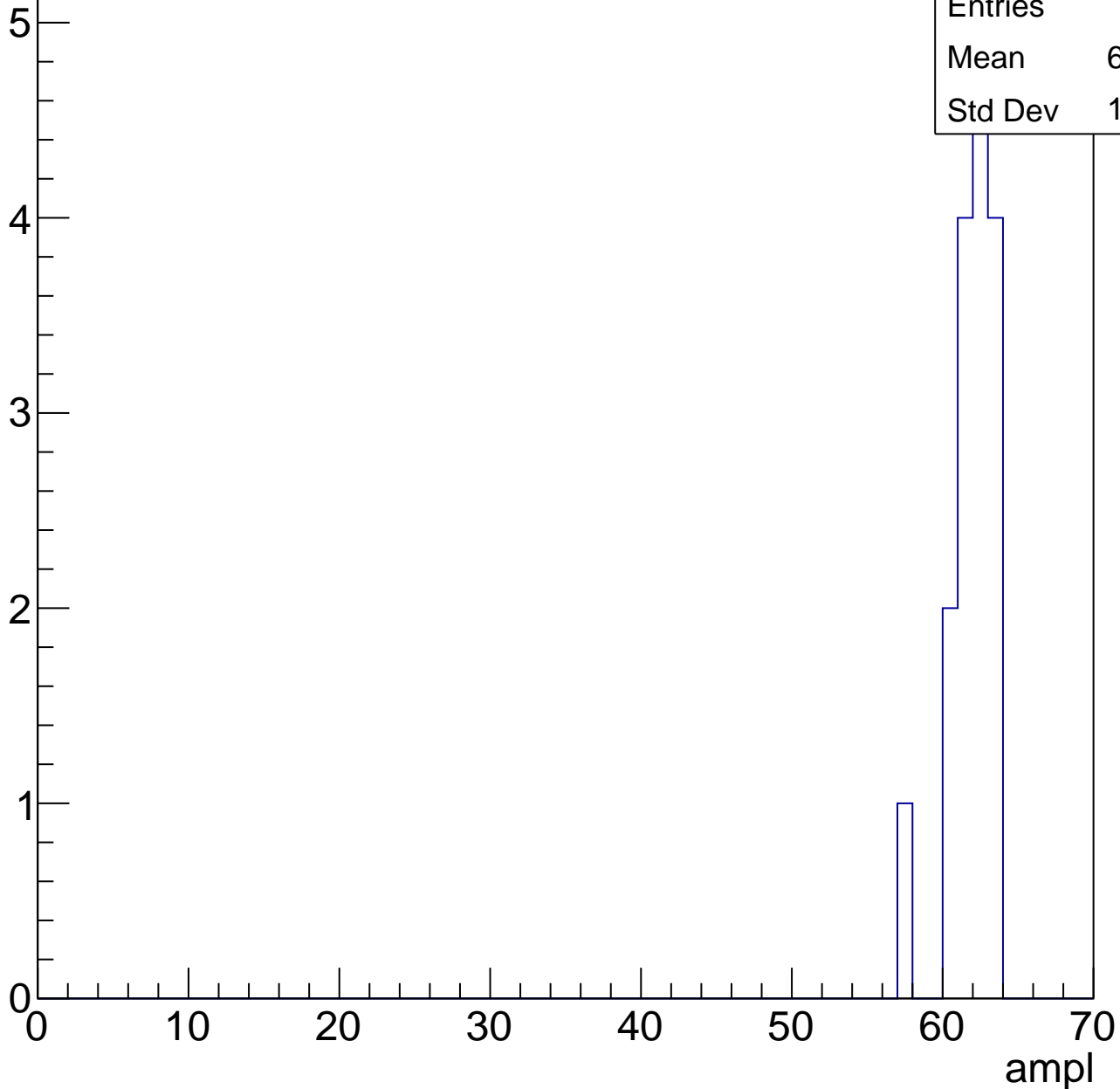


# B1L103S, U2-ch36, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	16
Mean	61.44
Std Dev	1.499





# B1L103S, U2-ch36, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U2-ch37, adc0

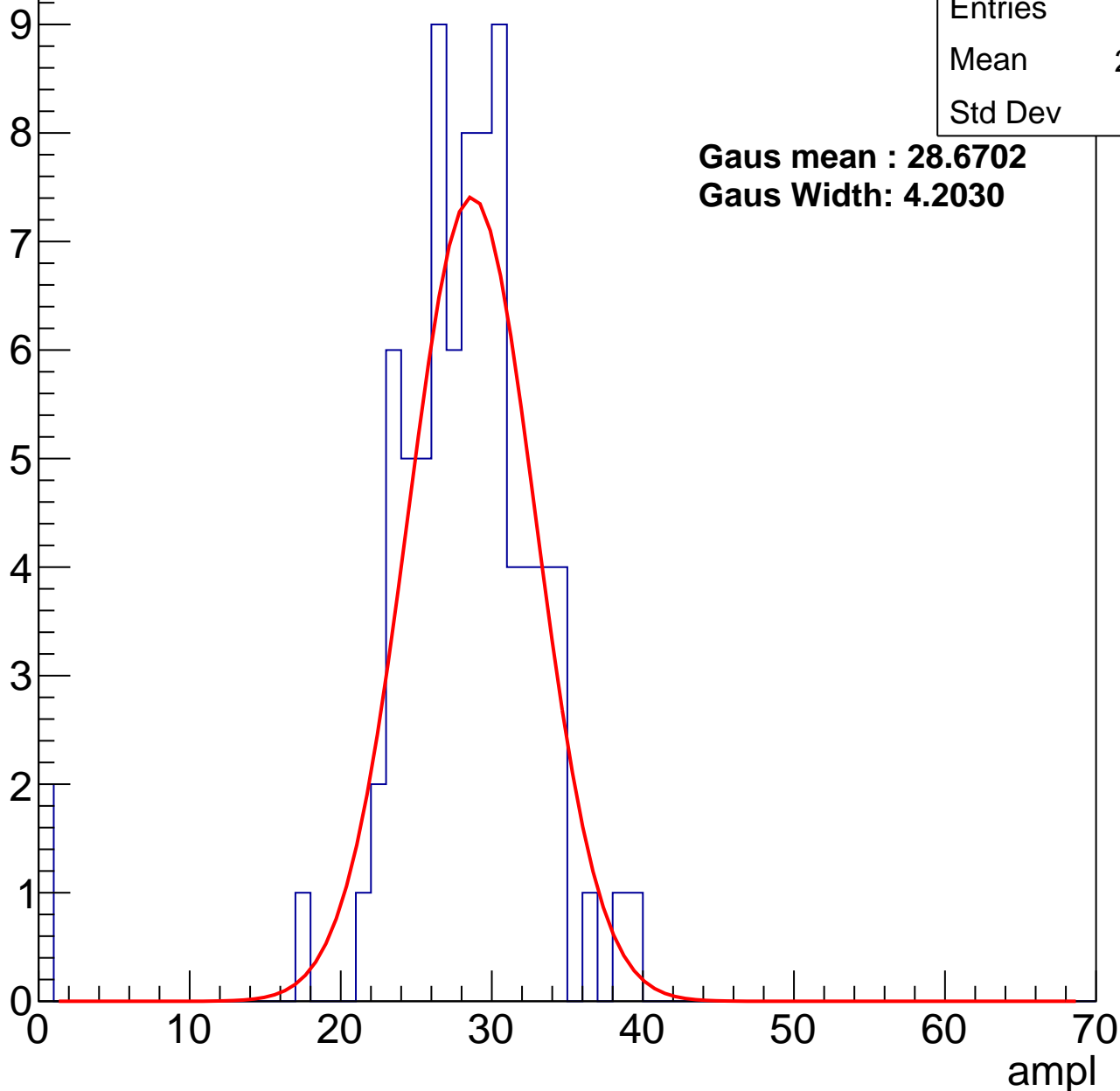
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	81
Mean	27.41
Std Dev	5.85

**Gaus mean : 28.6702**

**Gaus Width: 4.2030**



# B1L103S, U2-ch37, adc1

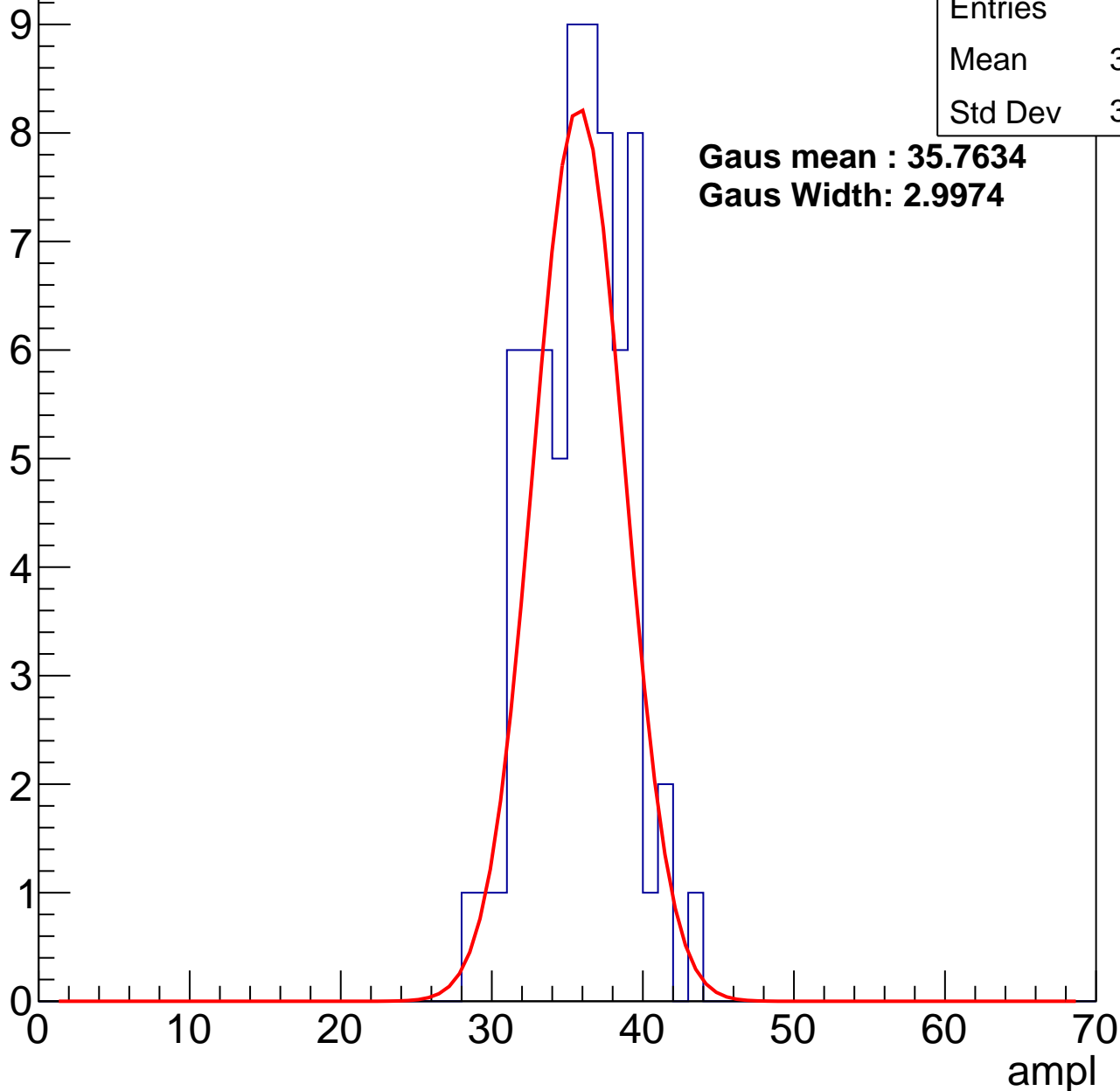
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	35.33
Std Dev	3.083

**Gaus mean : 35.7634**

**Gaus Width: 2.9974**



# B1L103S, U2-ch37, adc2

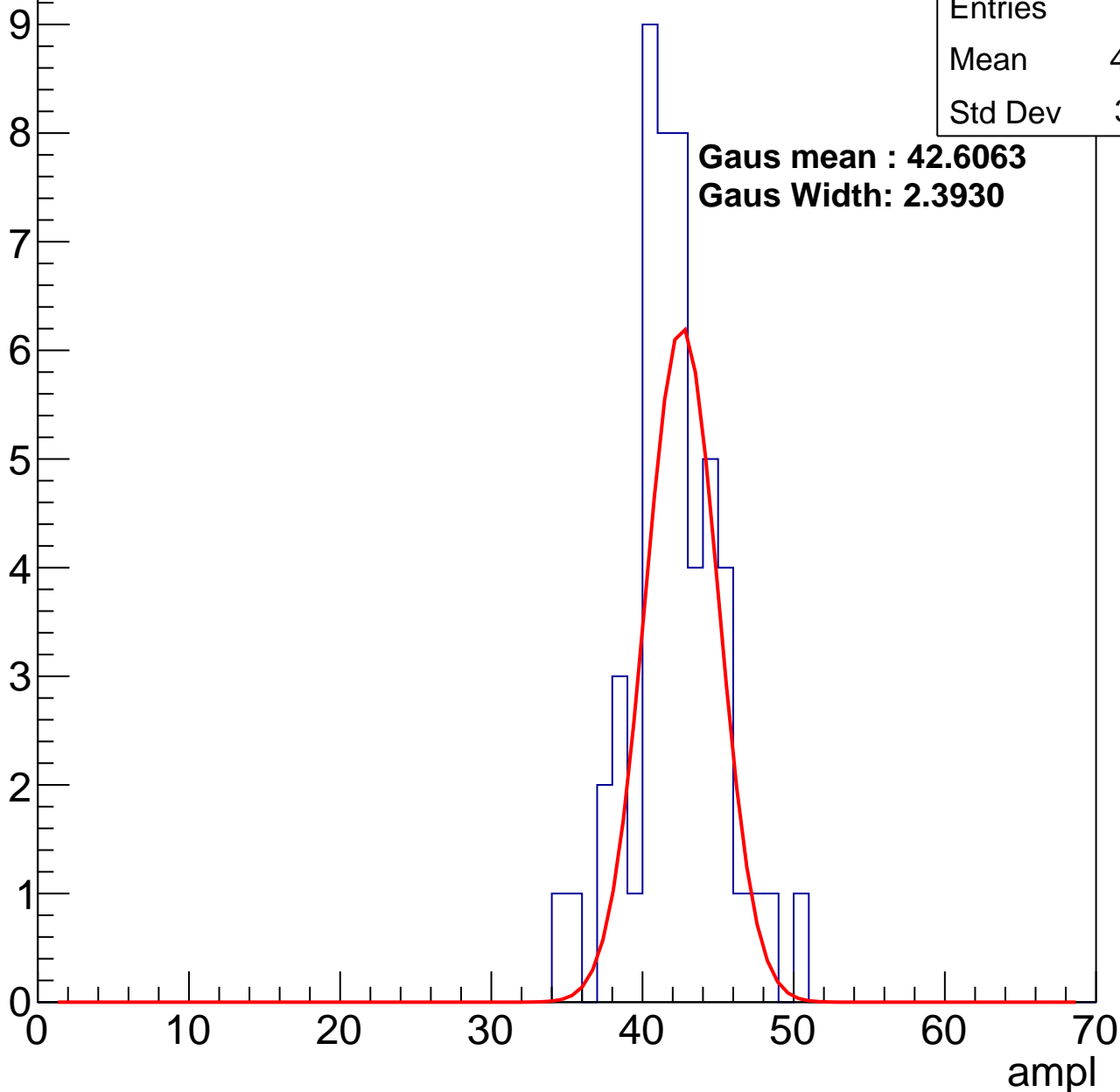
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	41.66
Std Dev	3.031

**Gaus mean : 42.6063**

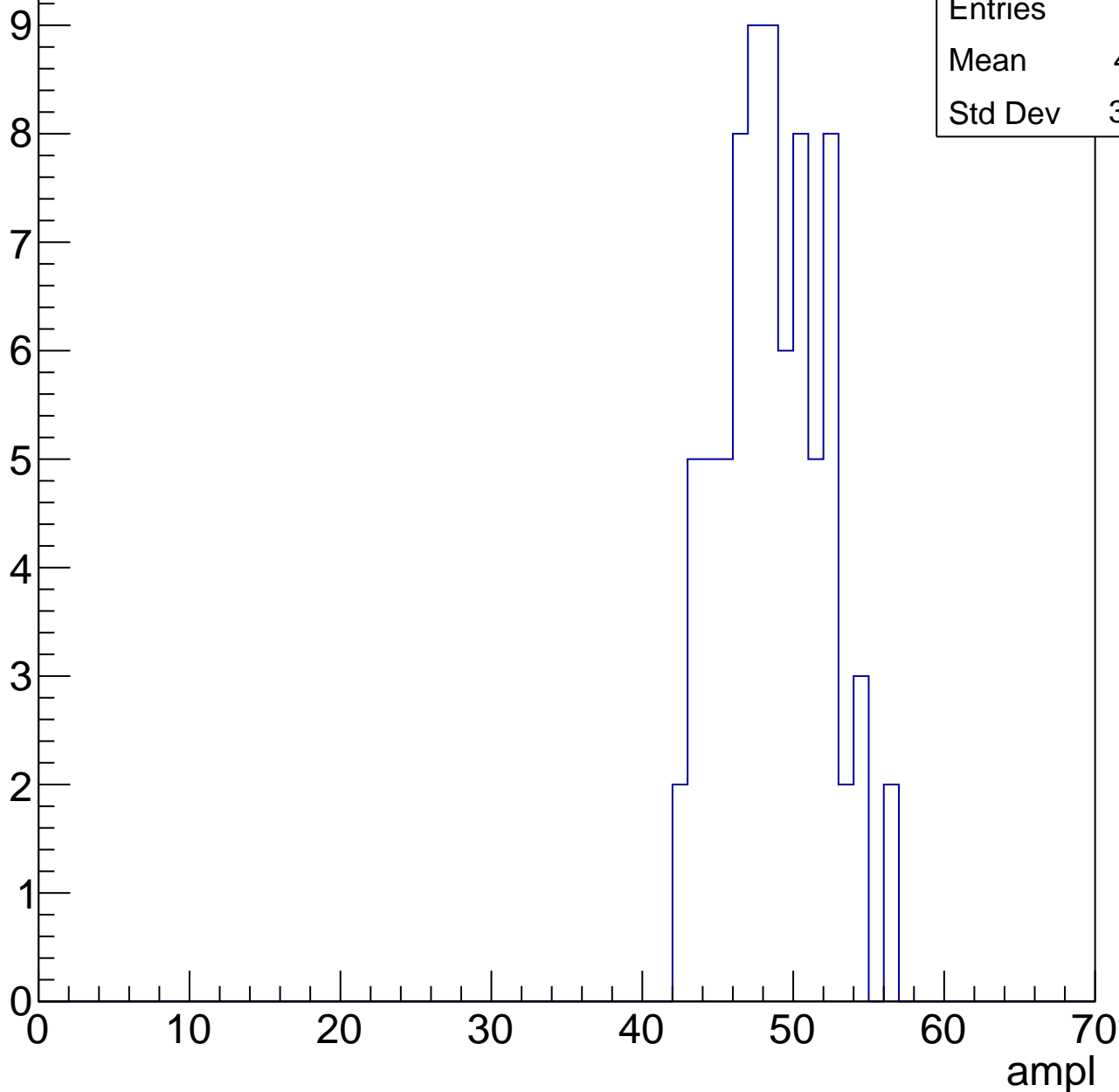
**Gaus Width: 2.3930**



# B1L103S, U2-ch37, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

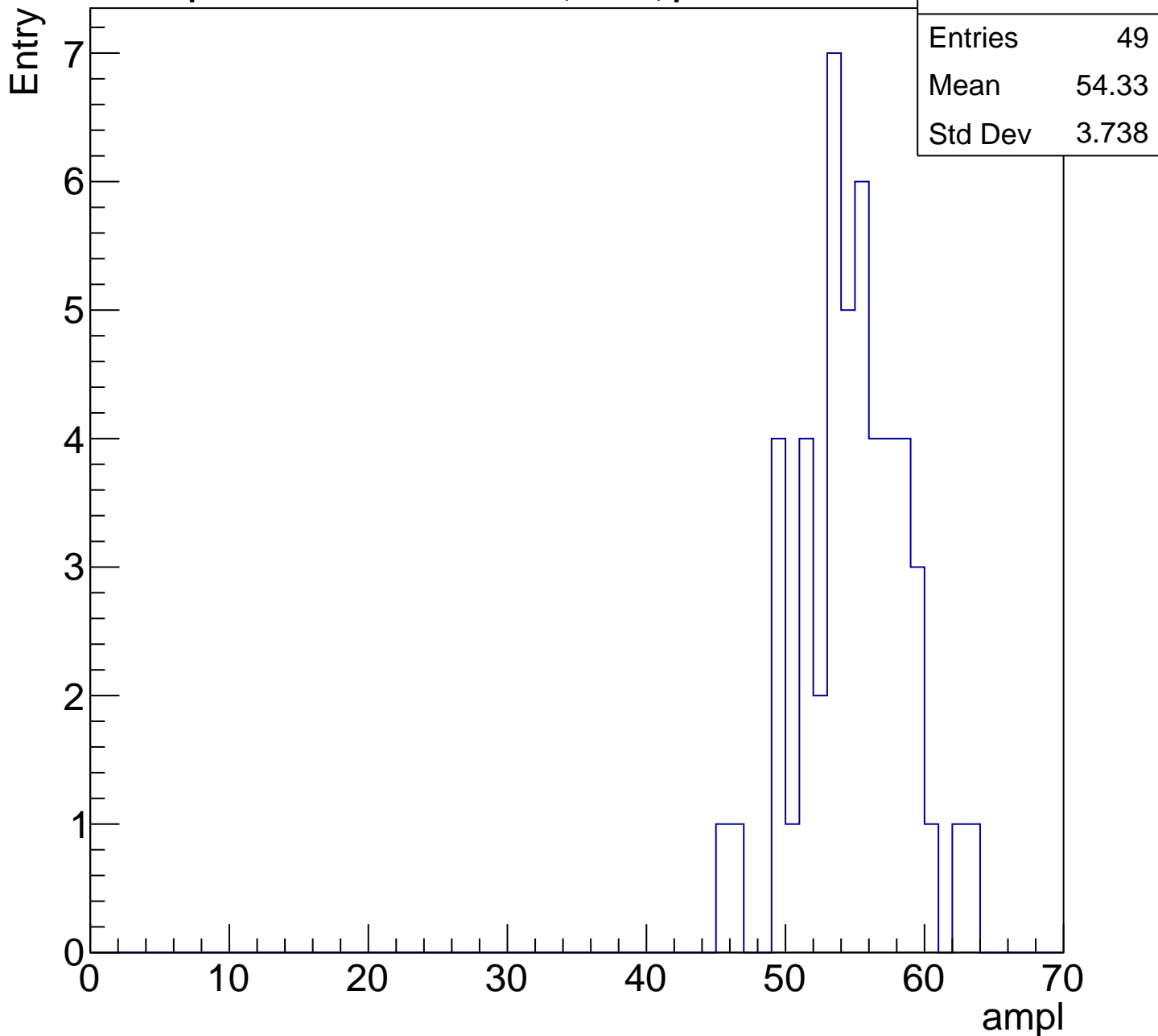
Entry



Entries	77
Mean	48.21
Std Dev	3.336

# B1L103S, U2-ch37, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

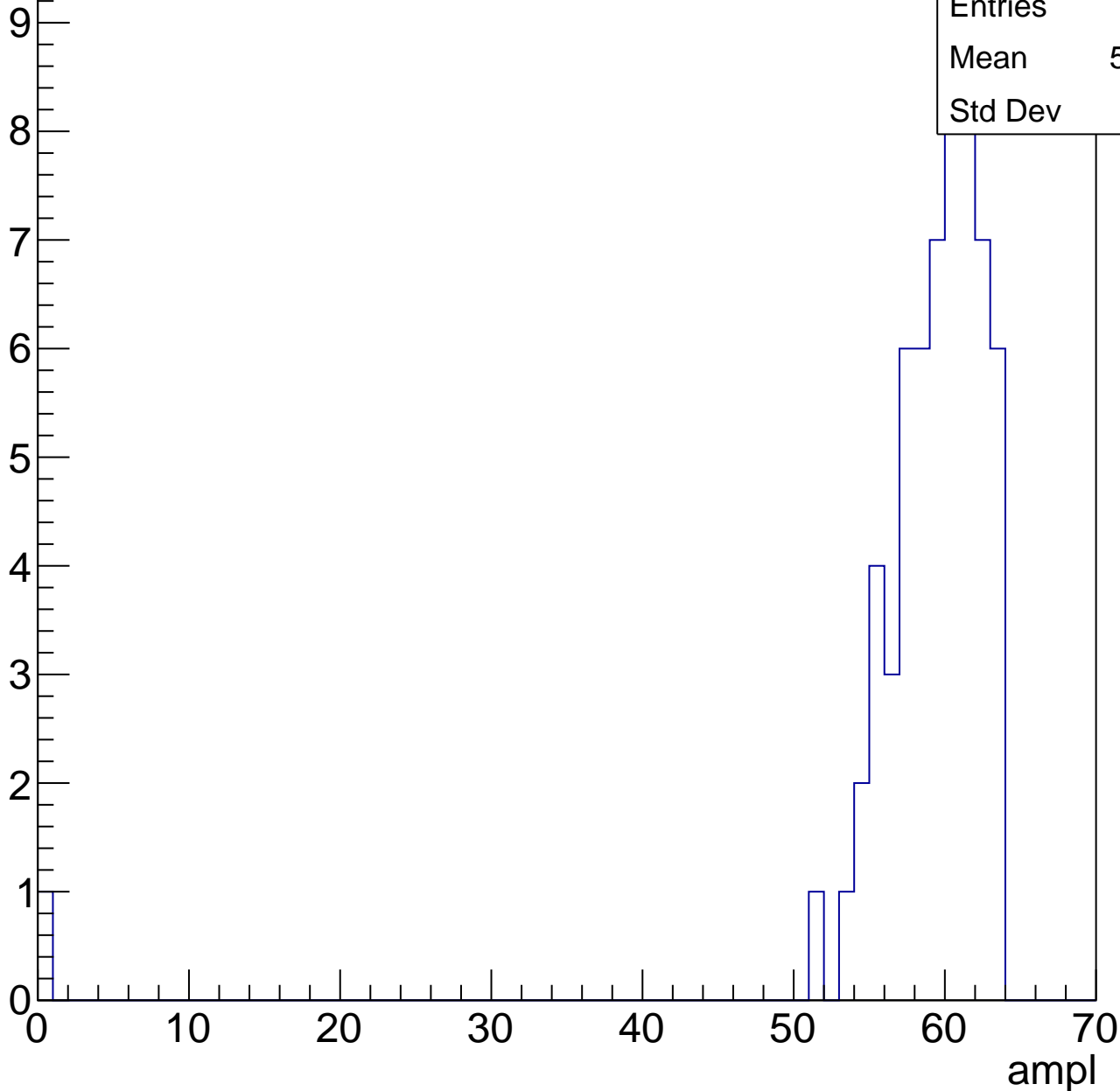


# B1L103S, U2-ch37, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

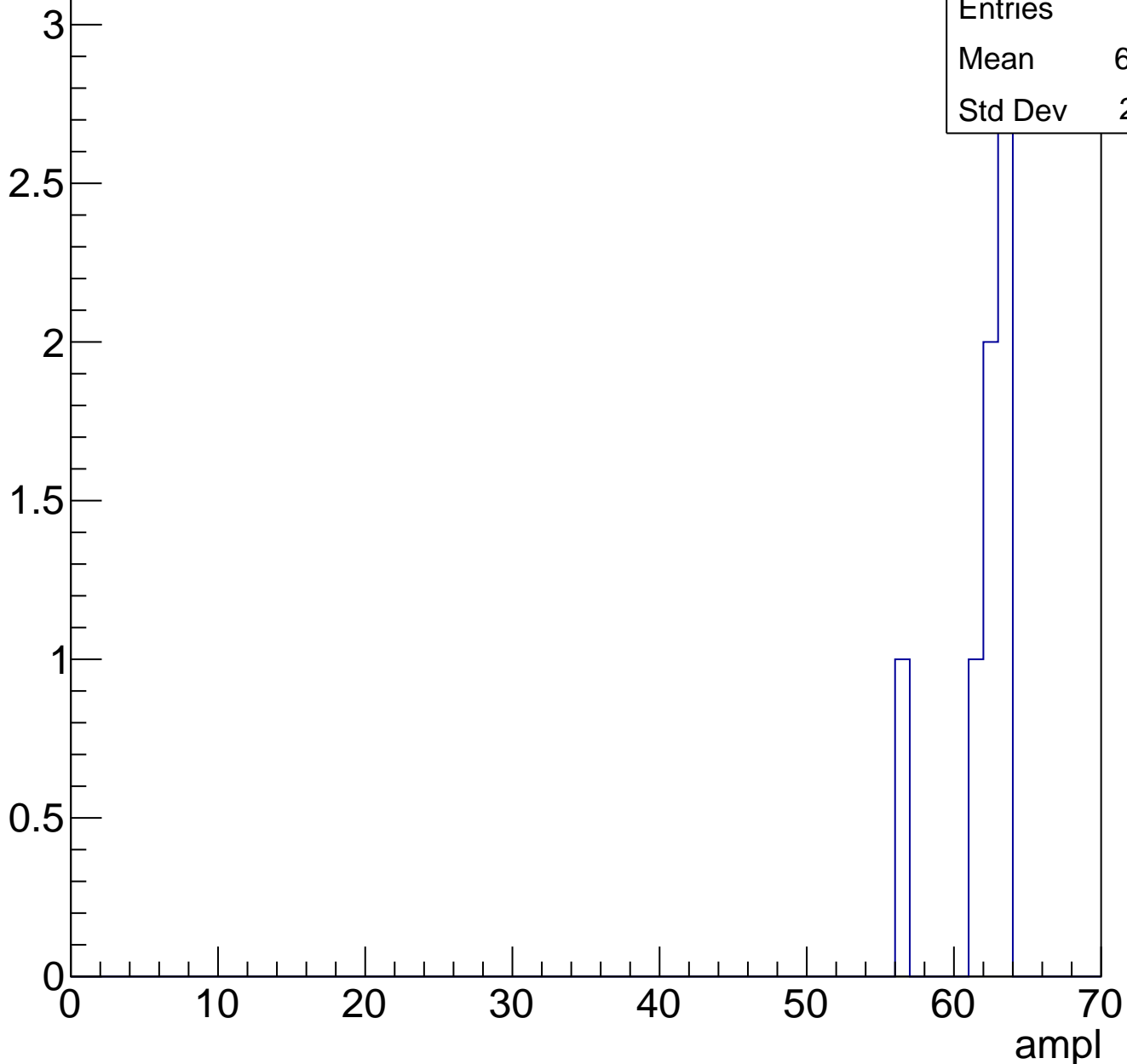
Entries	62
Mean	58.13
Std Dev	7.94



# B1L103S, U2-ch37, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U2-ch37, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U2-ch38, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	67
Mean	29.13
Std Dev	3.729

**Gaus mean : 29.9671**

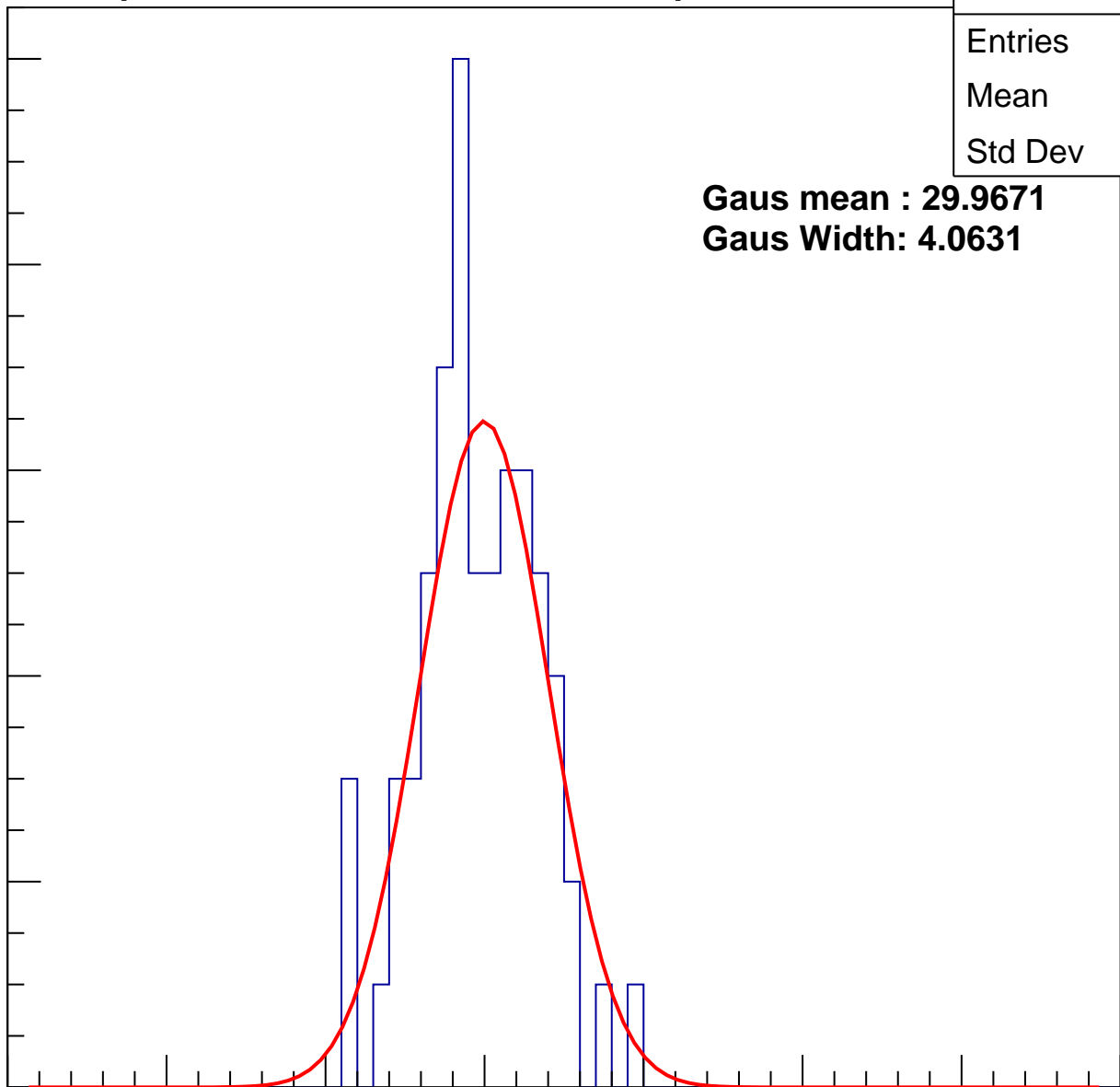
**Gaus Width: 4.0631**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U2-ch38, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	73
Mean	36.05
Std Dev	3.384

**Gaus mean : 36.5499**

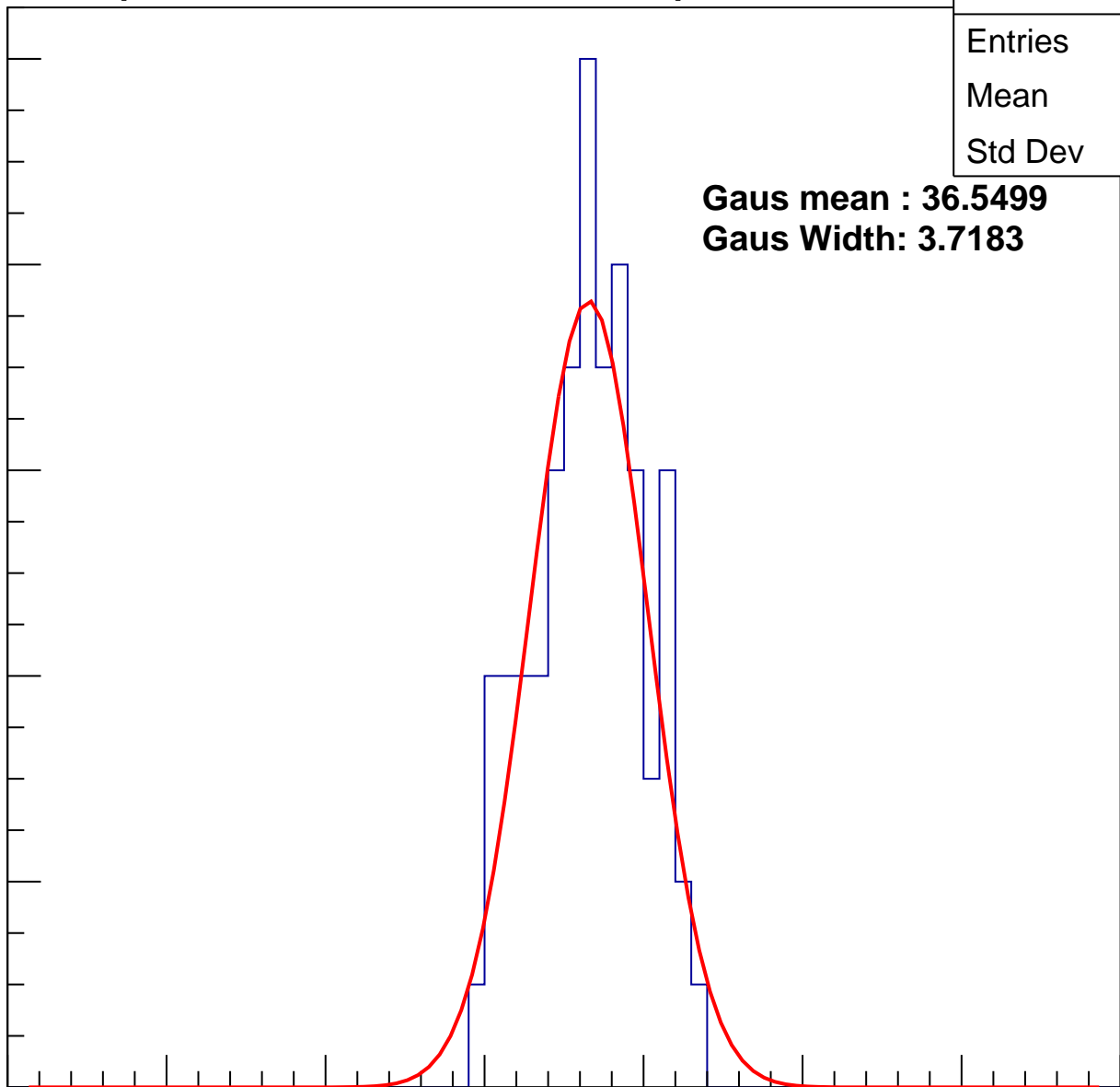
**Gaus Width: 3.7183**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L103S, U2-ch38, adc2

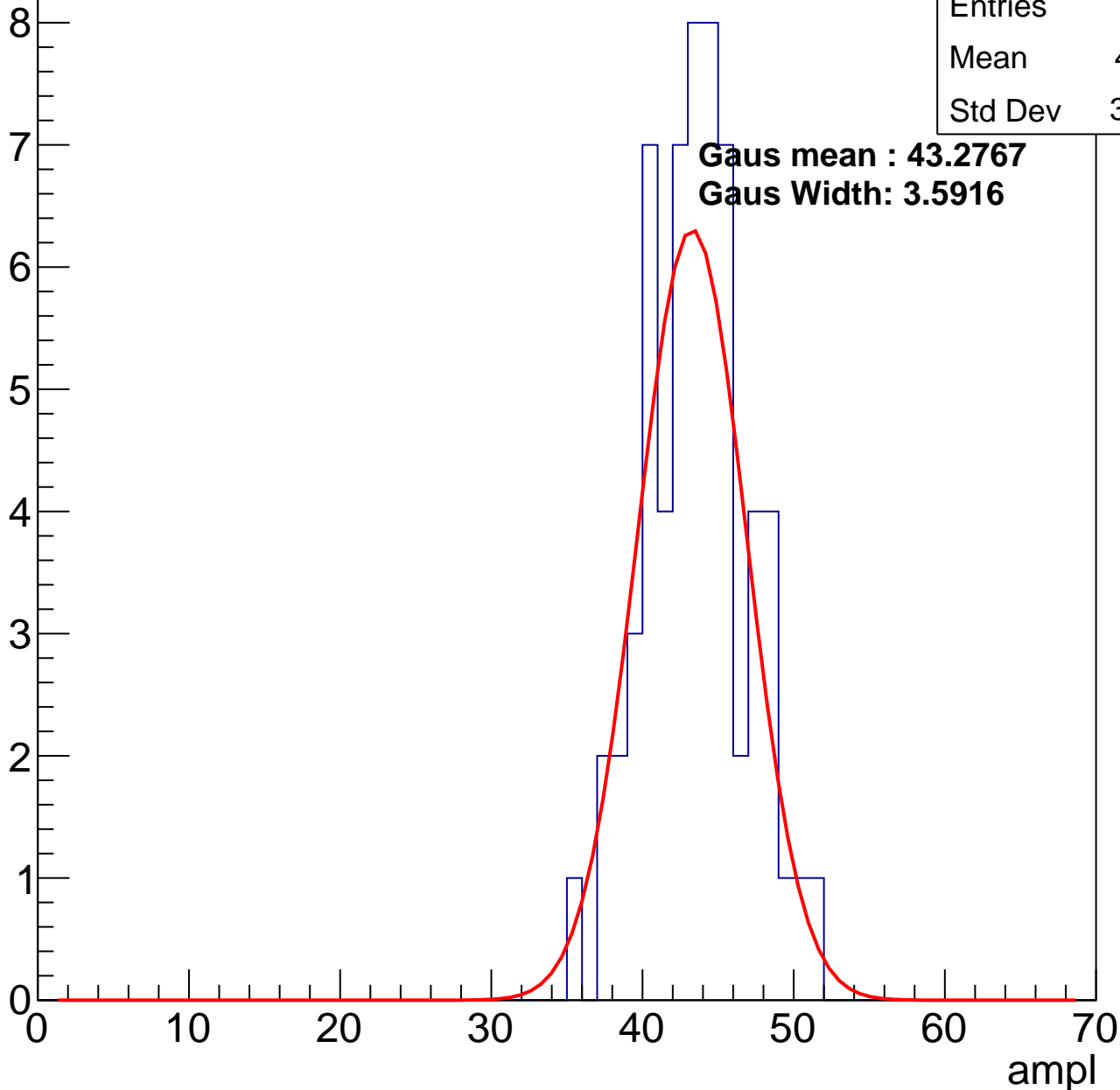
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	43.11
Std Dev	3.327

**Gaus mean : 43.2767**

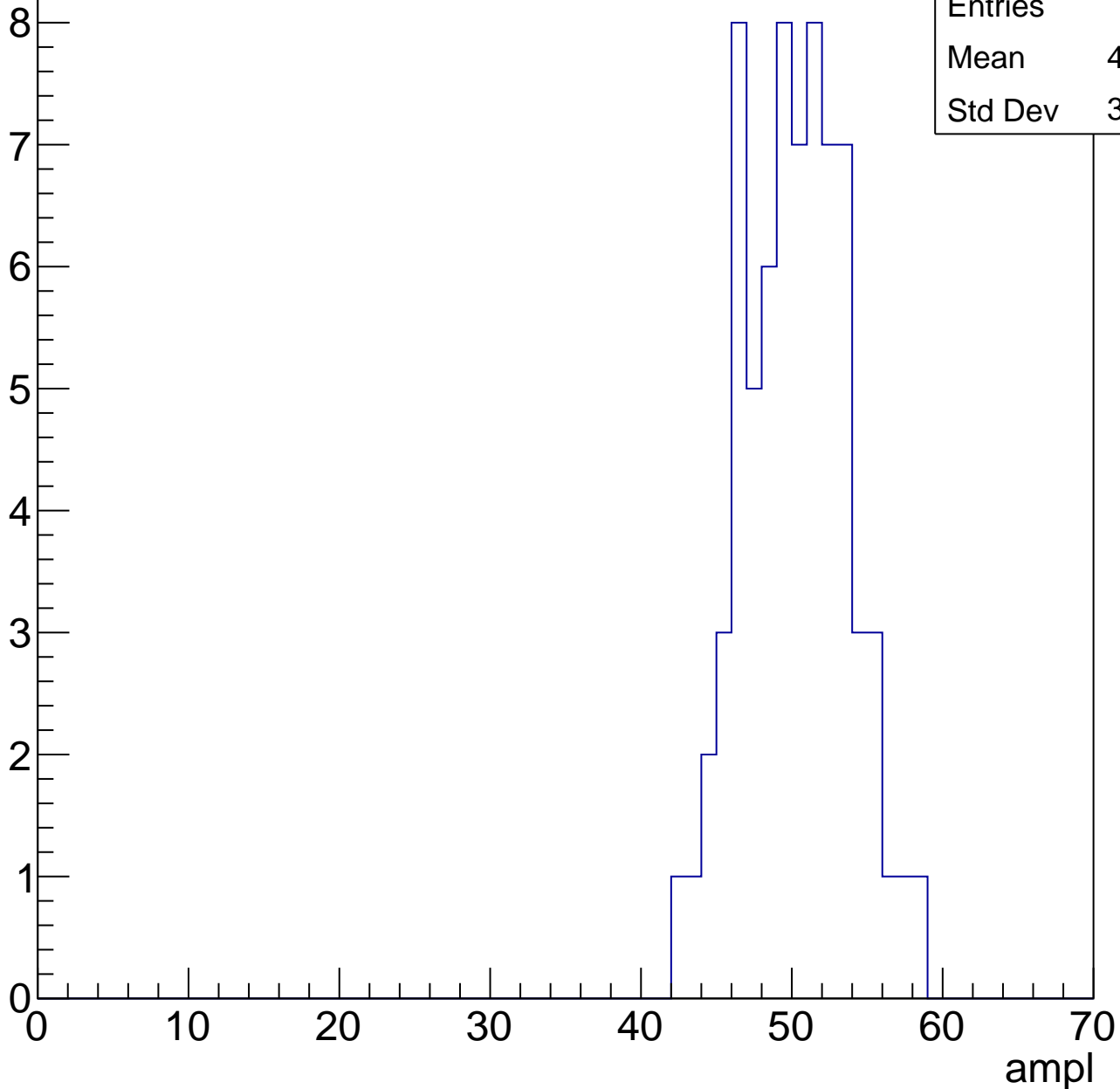
**Gaus Width: 3.5916**



# B1L103S, U2-ch38, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

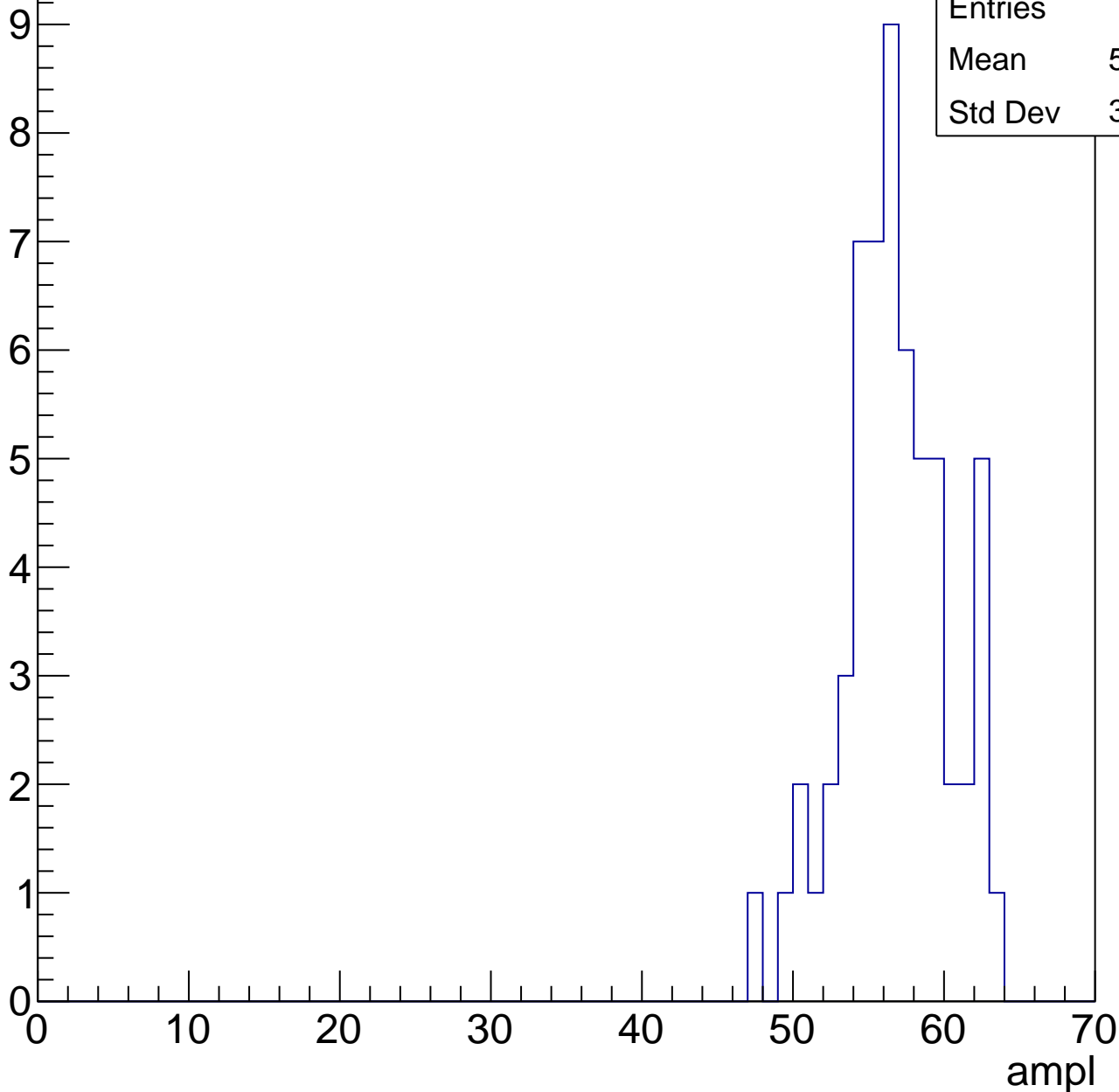


# B1L103S, U2-ch38, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	56.25
Std Dev	3.442

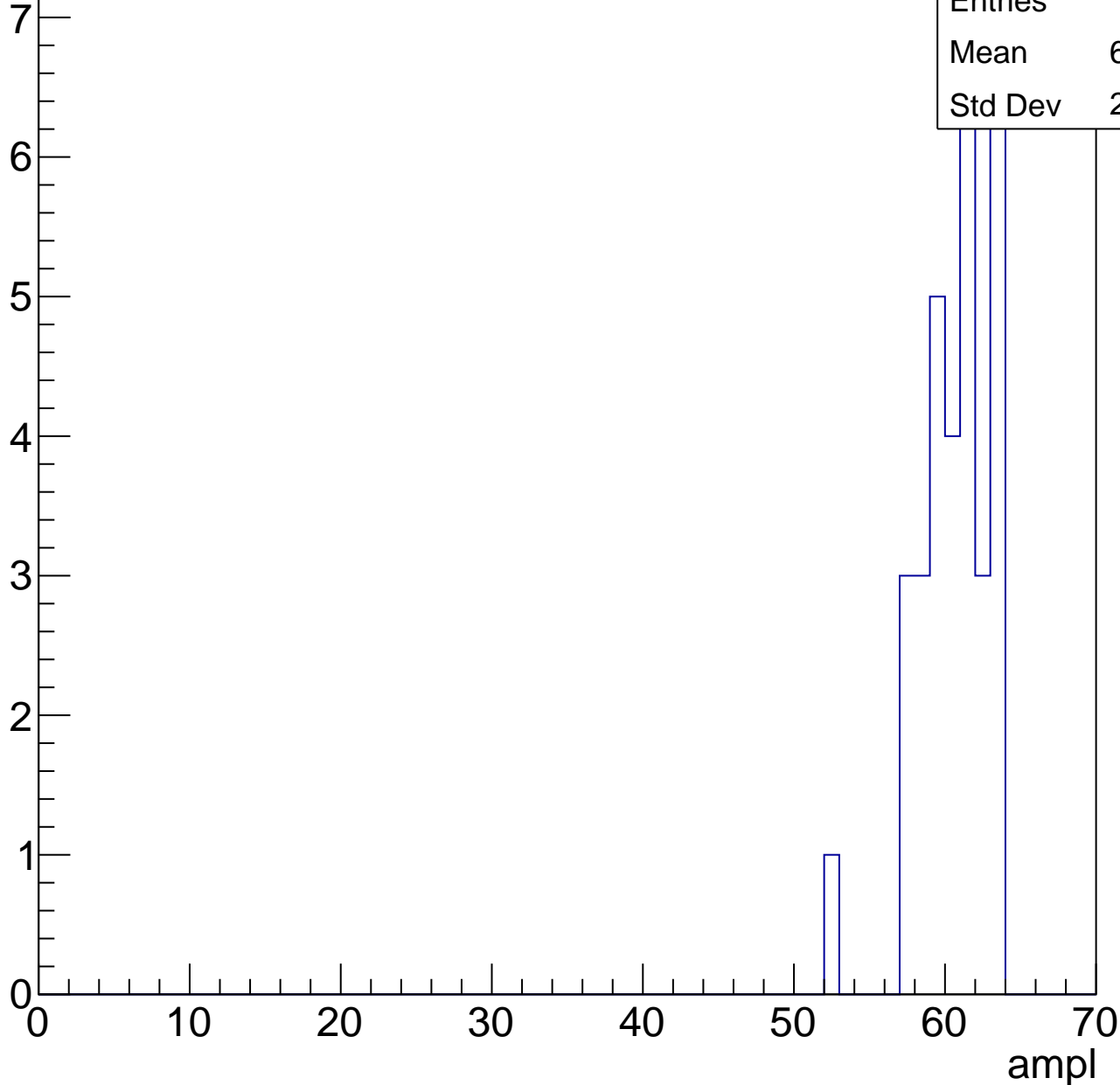


# B1L103S, U2-ch38, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

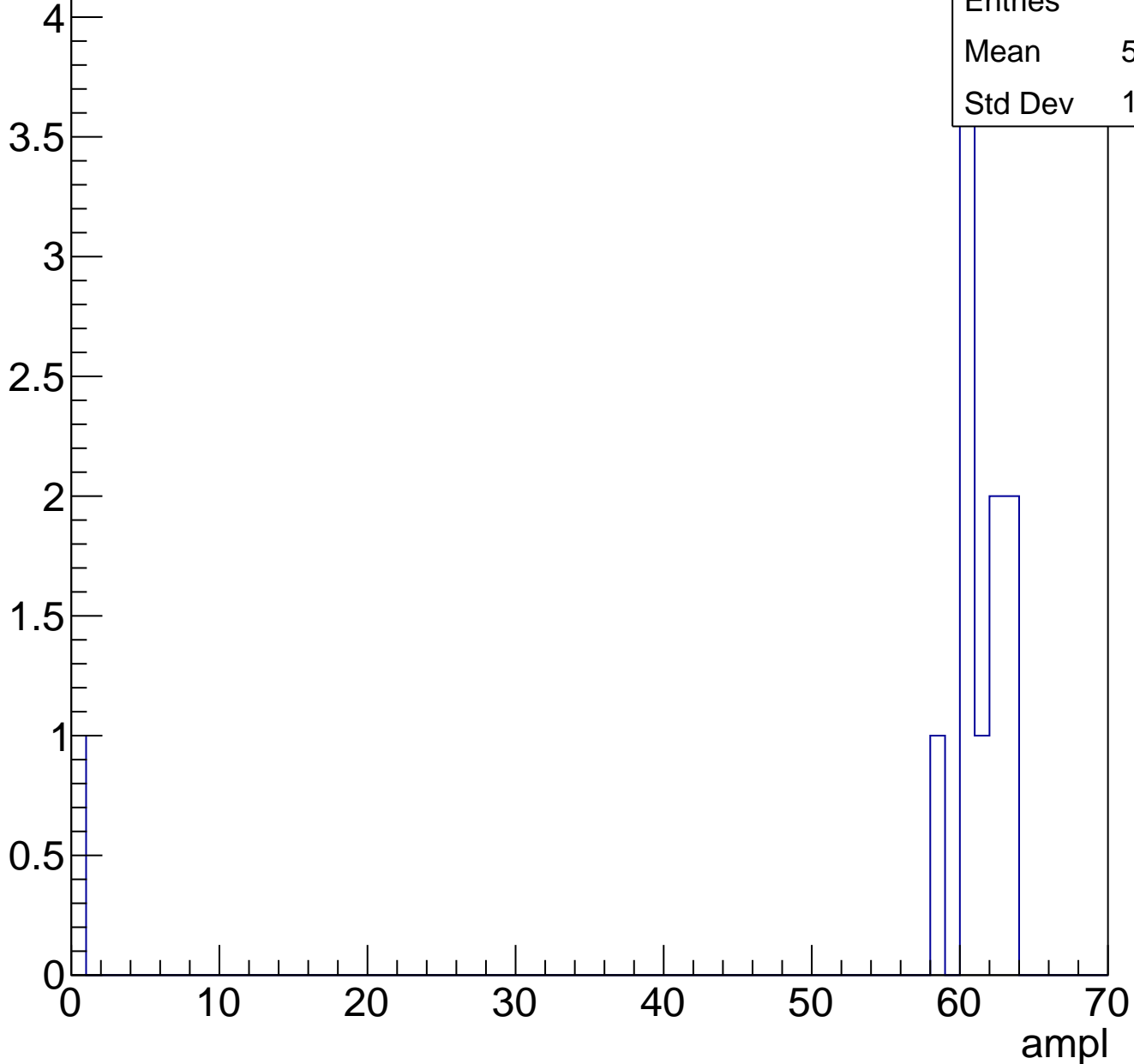
Entries	33
Mean	60.18
Std Dev	2.393



# B1L103S, U2-ch38, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U2-ch38, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

0

Mean

0

Std Dev

0

# B1L103S, U2-ch39, adc0

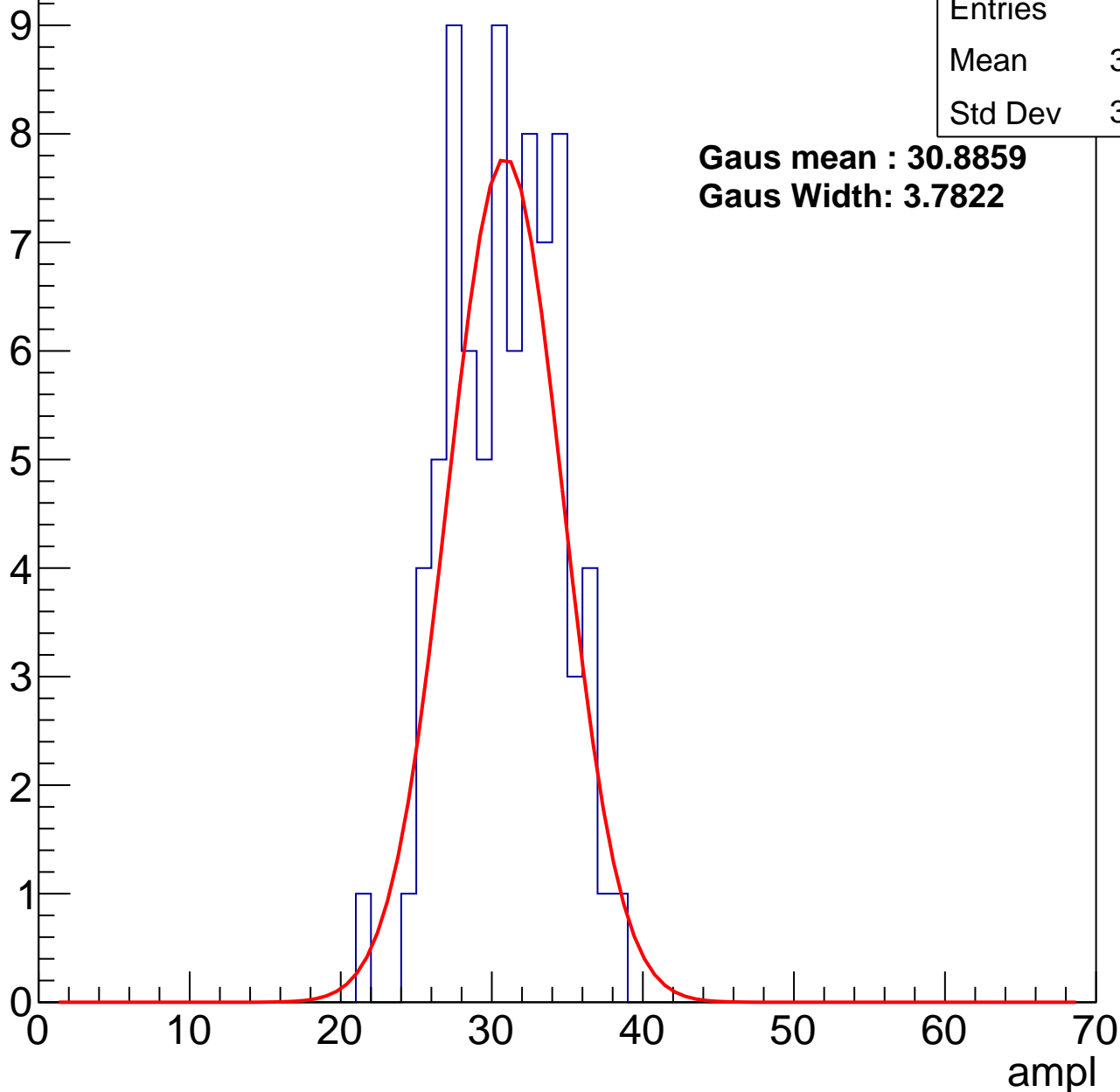
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	30.38
Std Dev	3.502

**Gaus mean : 30.8859**

**Gaus Width: 3.7822**



# B1L103S, U2-ch39, adc1

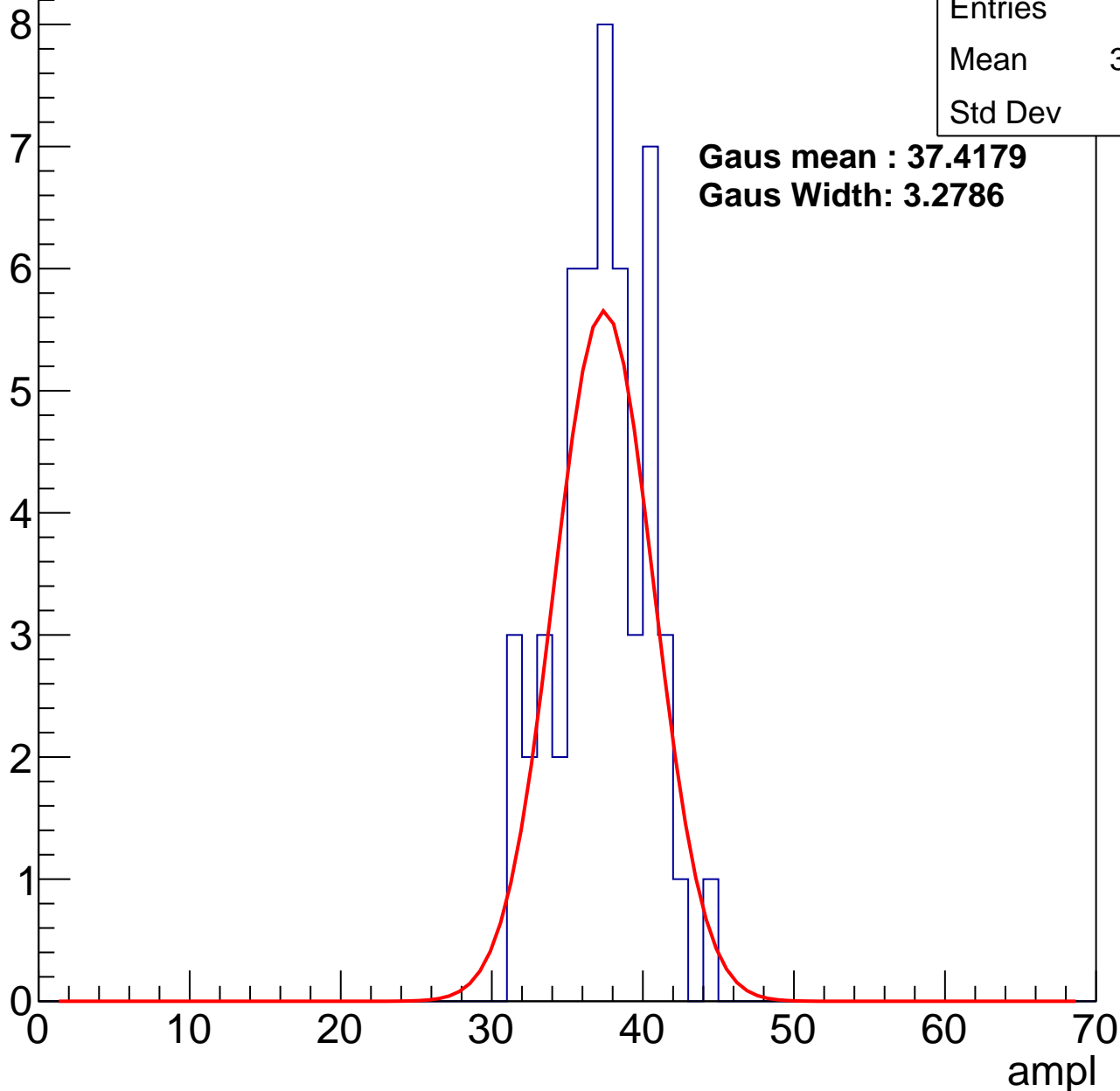
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	36.86
Std Dev	2.99

**Gaus mean : 37.4179**

**Gaus Width: 3.2786**

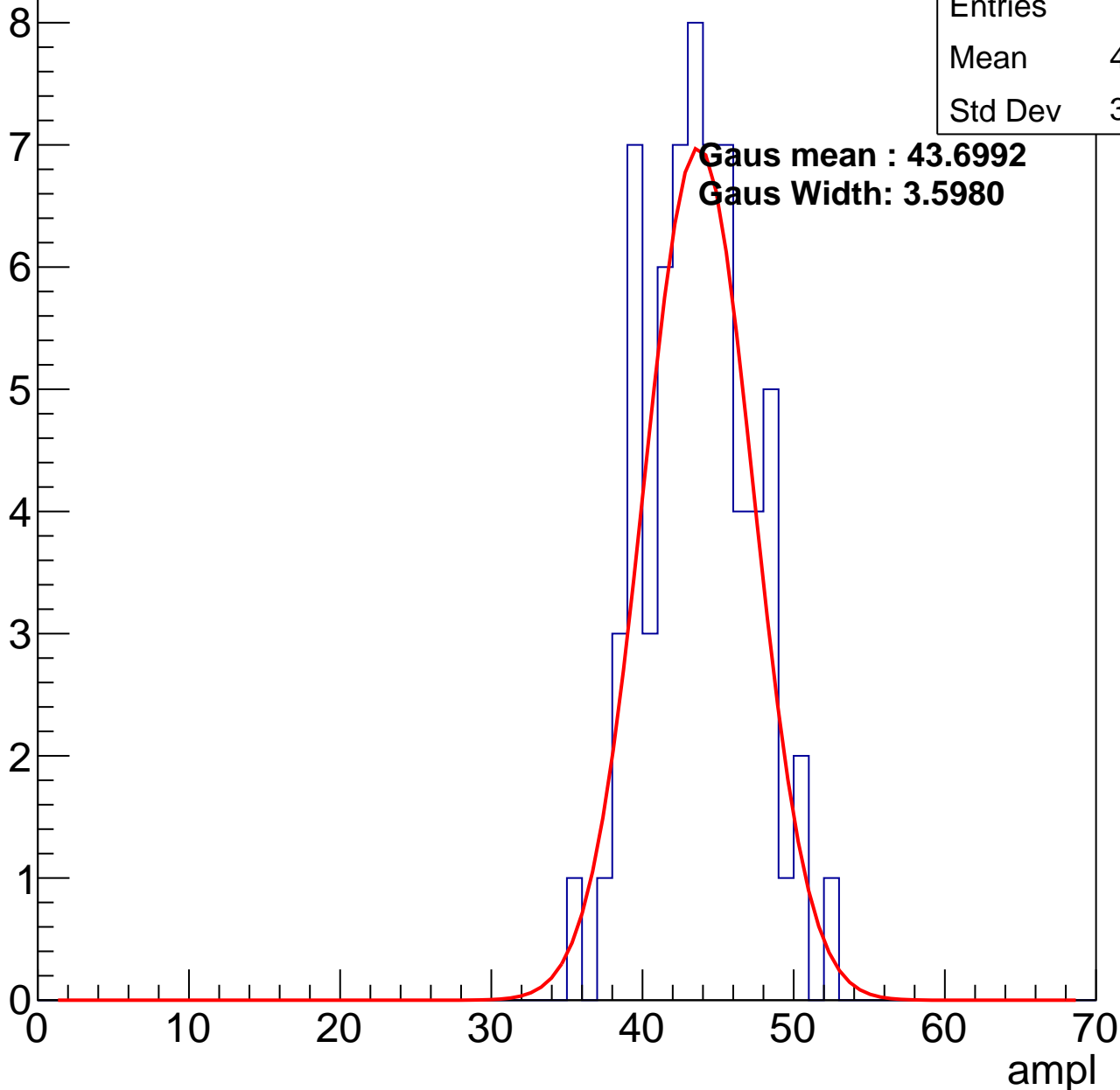


# B1L103S, U2-ch39, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

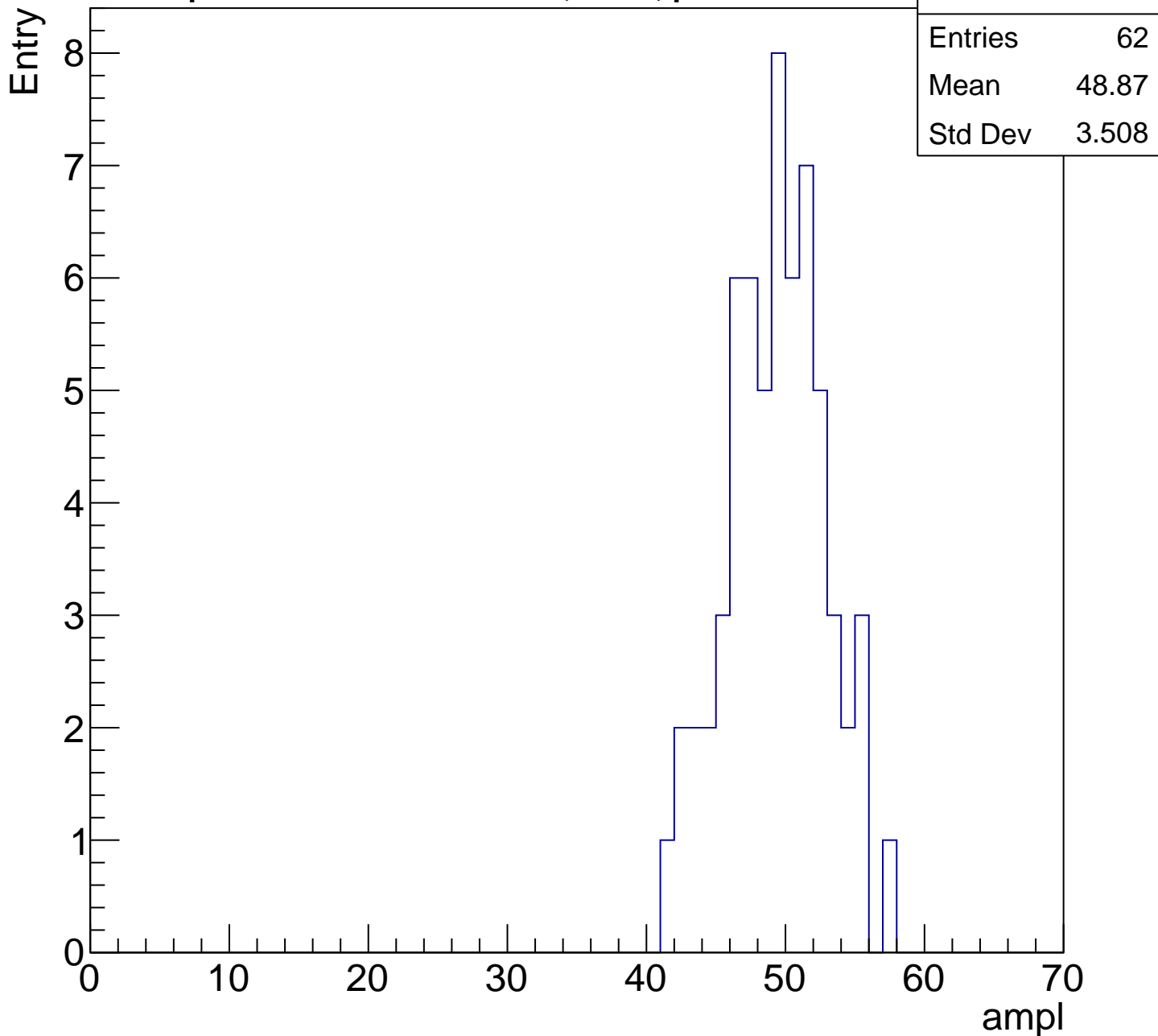
Entry

Entries	67
Mean	43.27
Std Dev	3.488



# B1L103S, U2-ch39, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

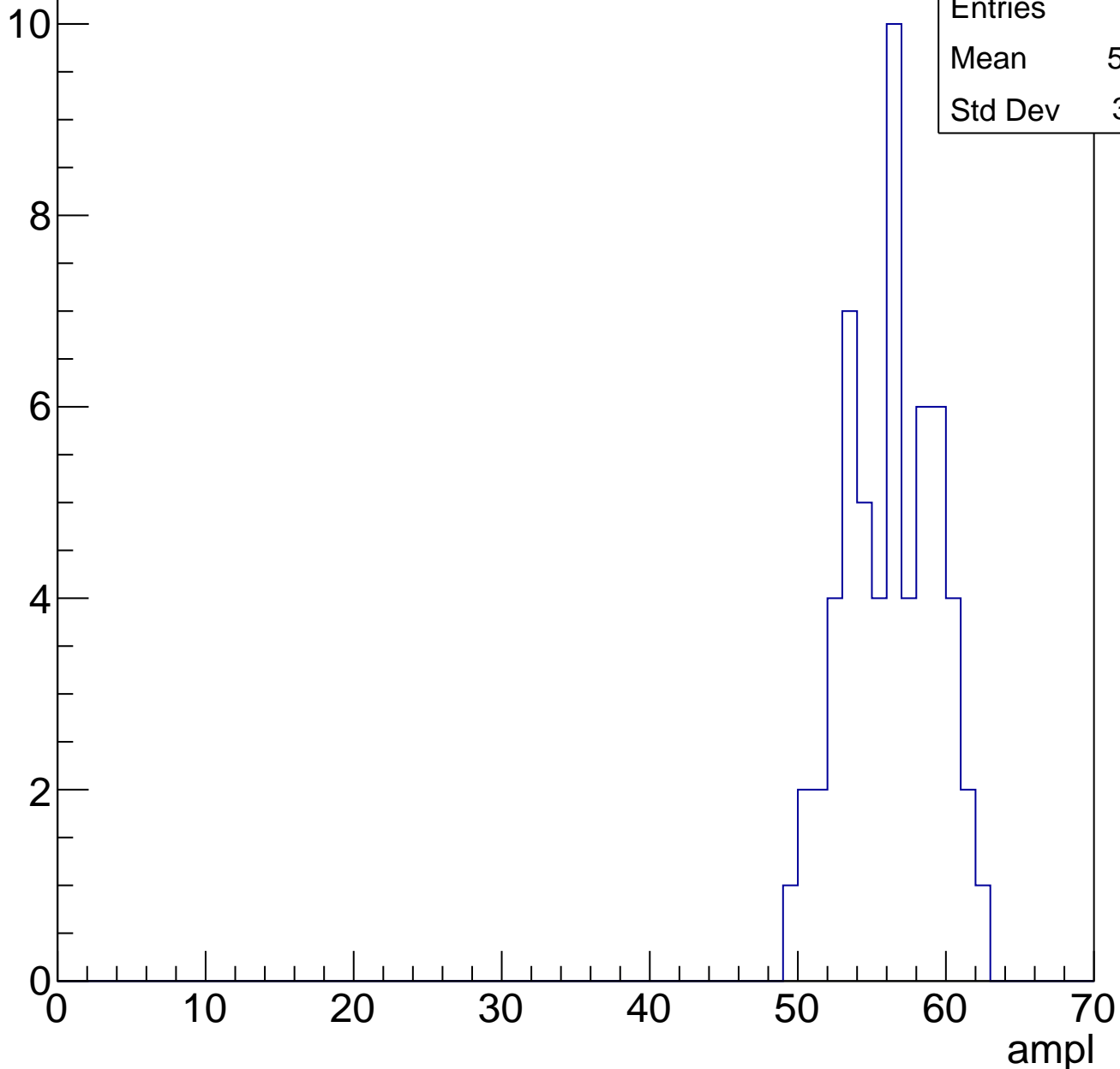


# B1L103S, U2-ch39, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	58
Mean	55.76
Std Dev	3.081

Entry

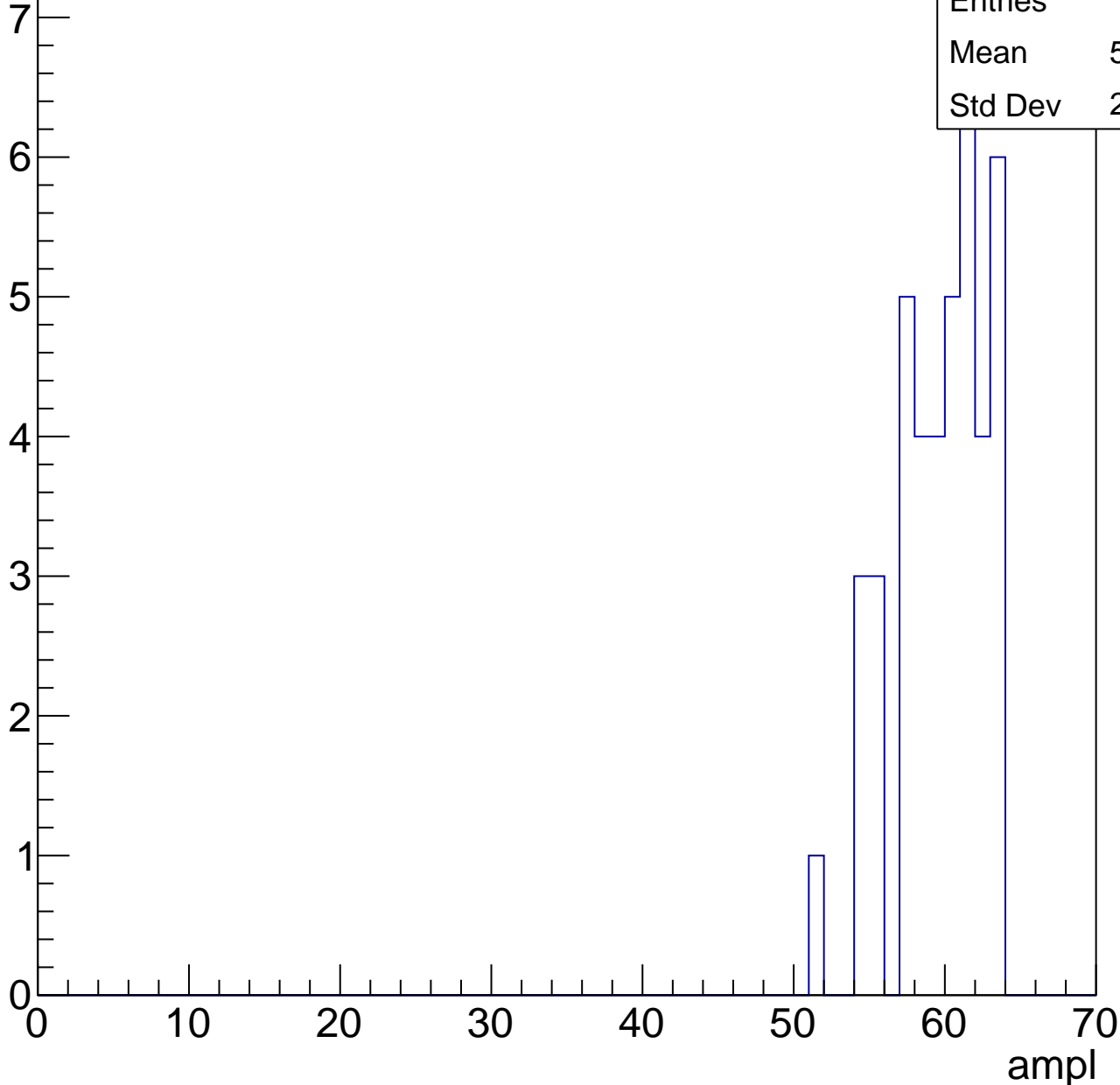


# B1L103S, U2-ch39, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	42
Mean	59.14
Std Dev	2.989

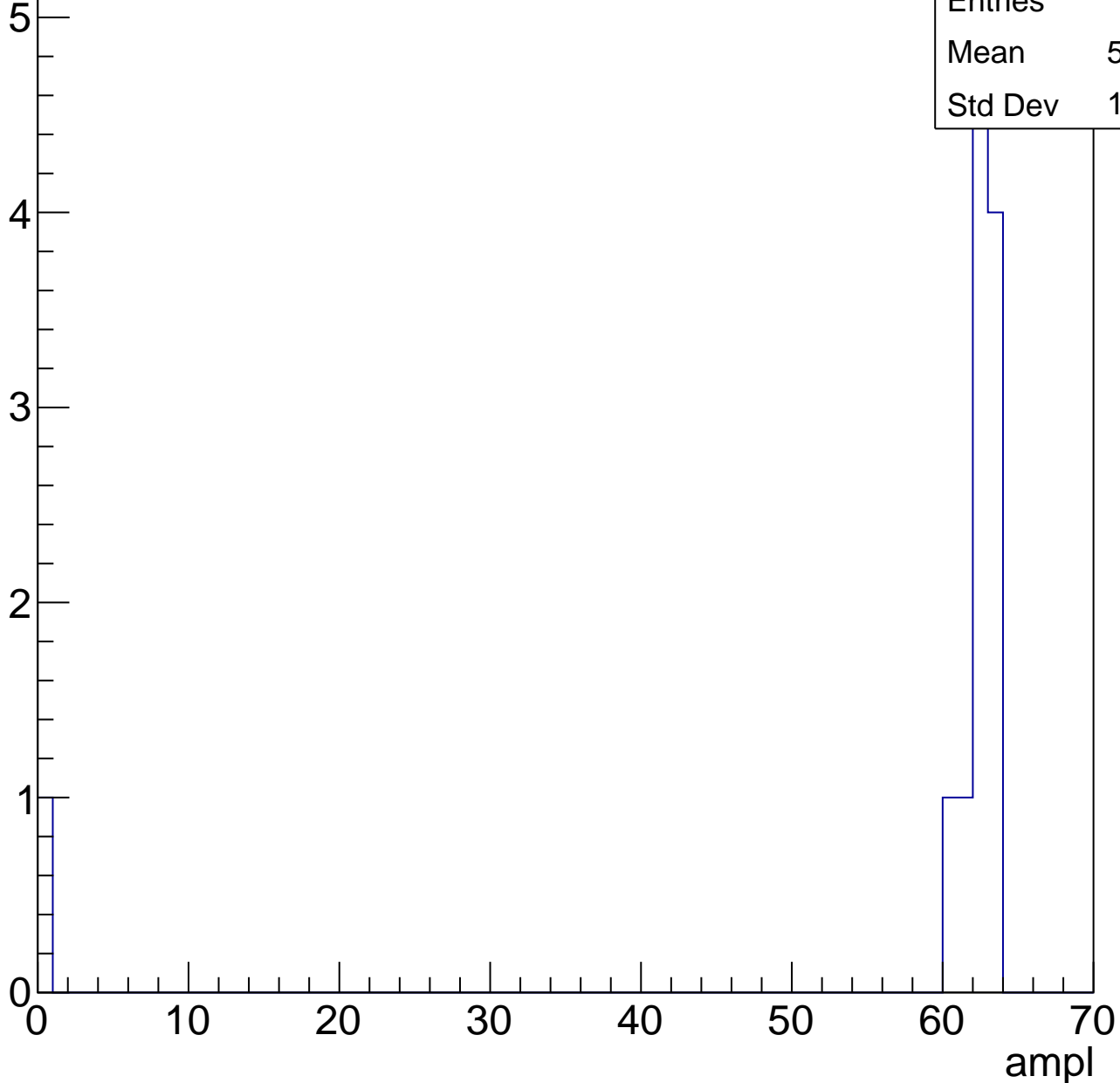


# B1L103S, U2-ch39, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	12
Mean	56.92
Std Dev	17.18





# B1L103S, U2-ch39, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U2-ch40, adc0

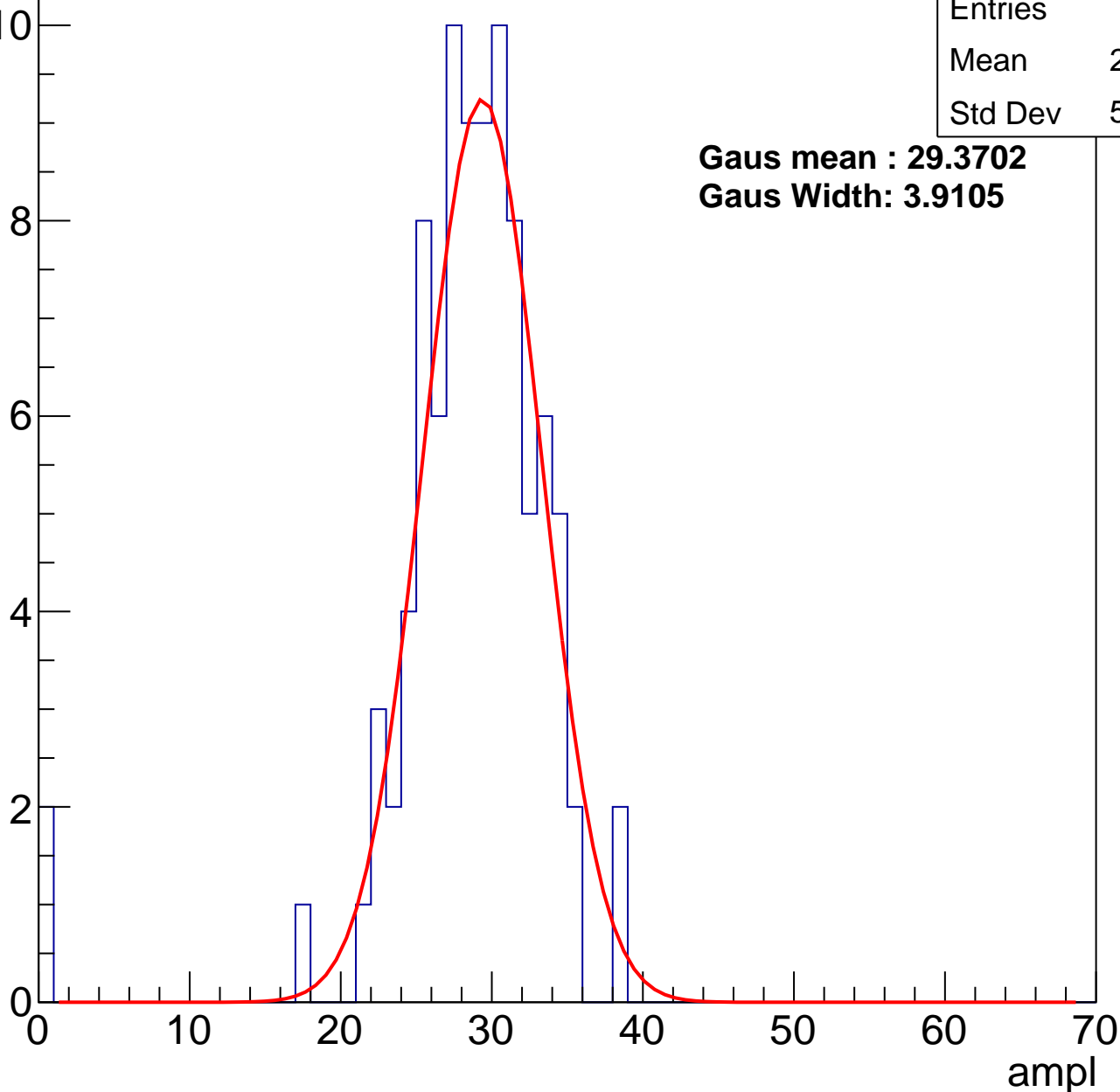
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	93
Mean	28.03
Std Dev	5.579

**Gaus mean : 29.3702**

**Gaus Width: 3.9105**



# B1L103S, U2-ch40, adc1

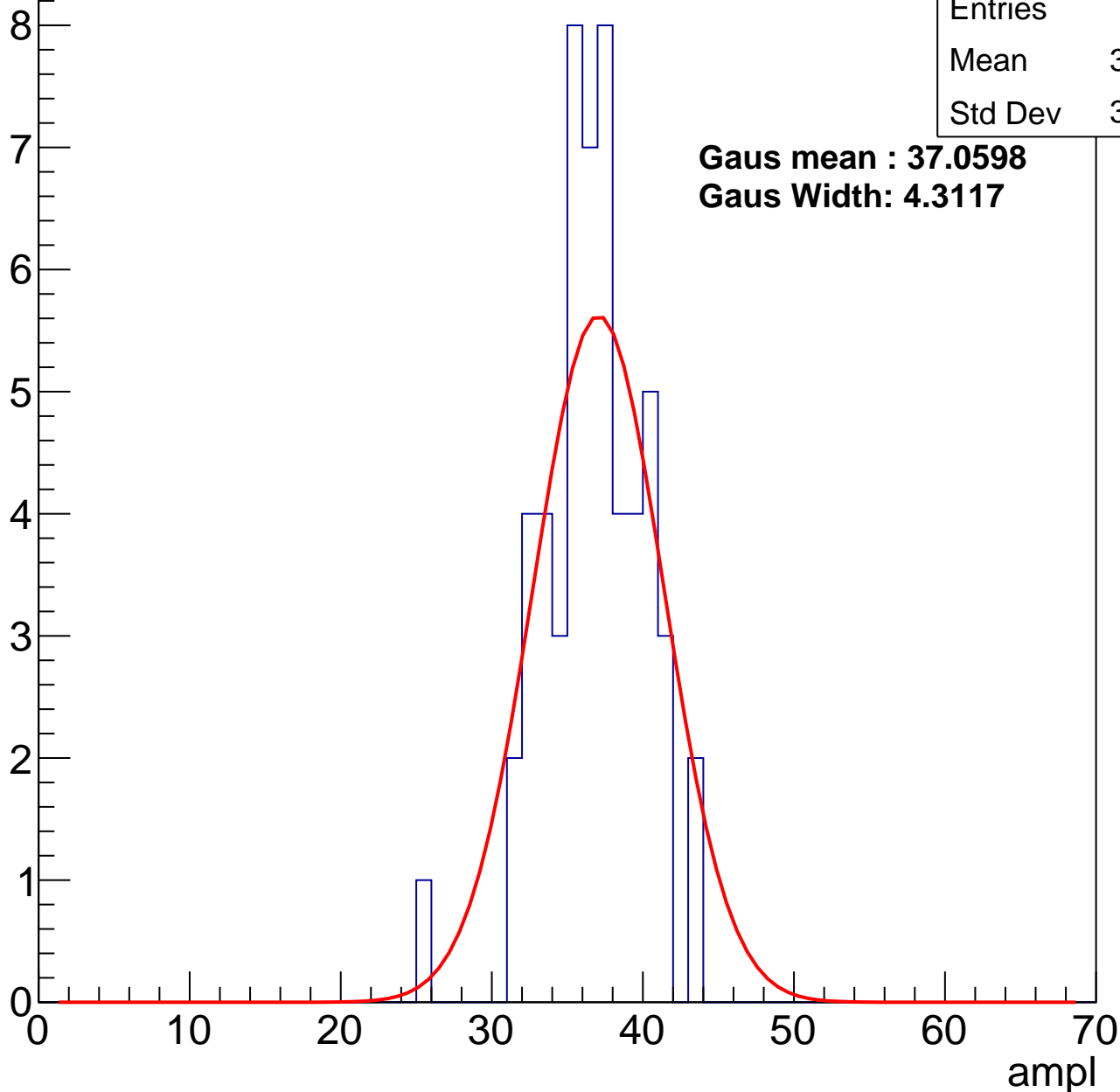
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	36.25
Std Dev	3.304

**Gaus mean : 37.0598**

**Gaus Width: 4.3117**



# B1L103S, U2-ch40, adc2

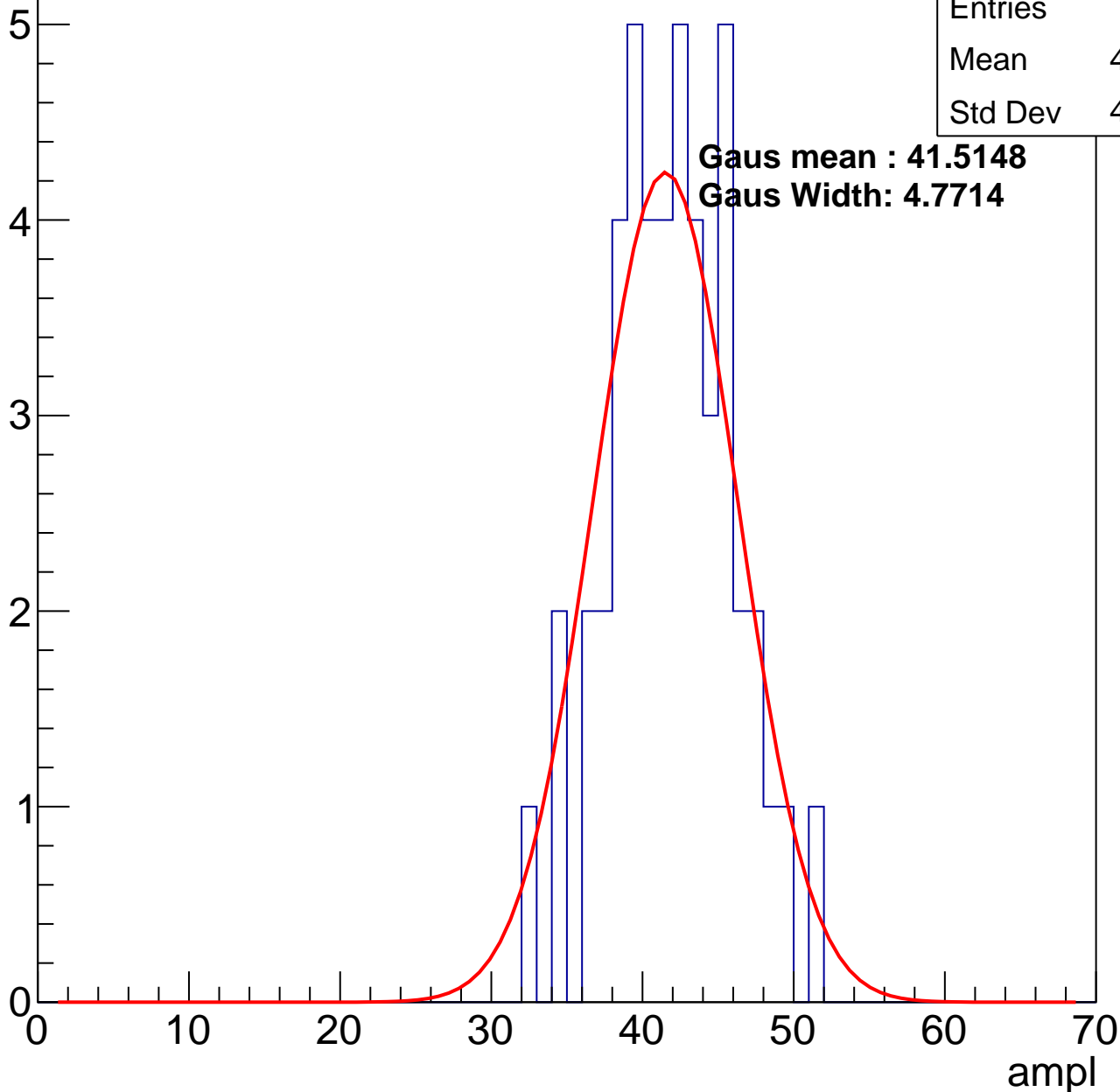
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	48
Mean	41.46
Std Dev	4.015

**Gaus mean : 41.5148**

**Gaus Width: 4.7714**

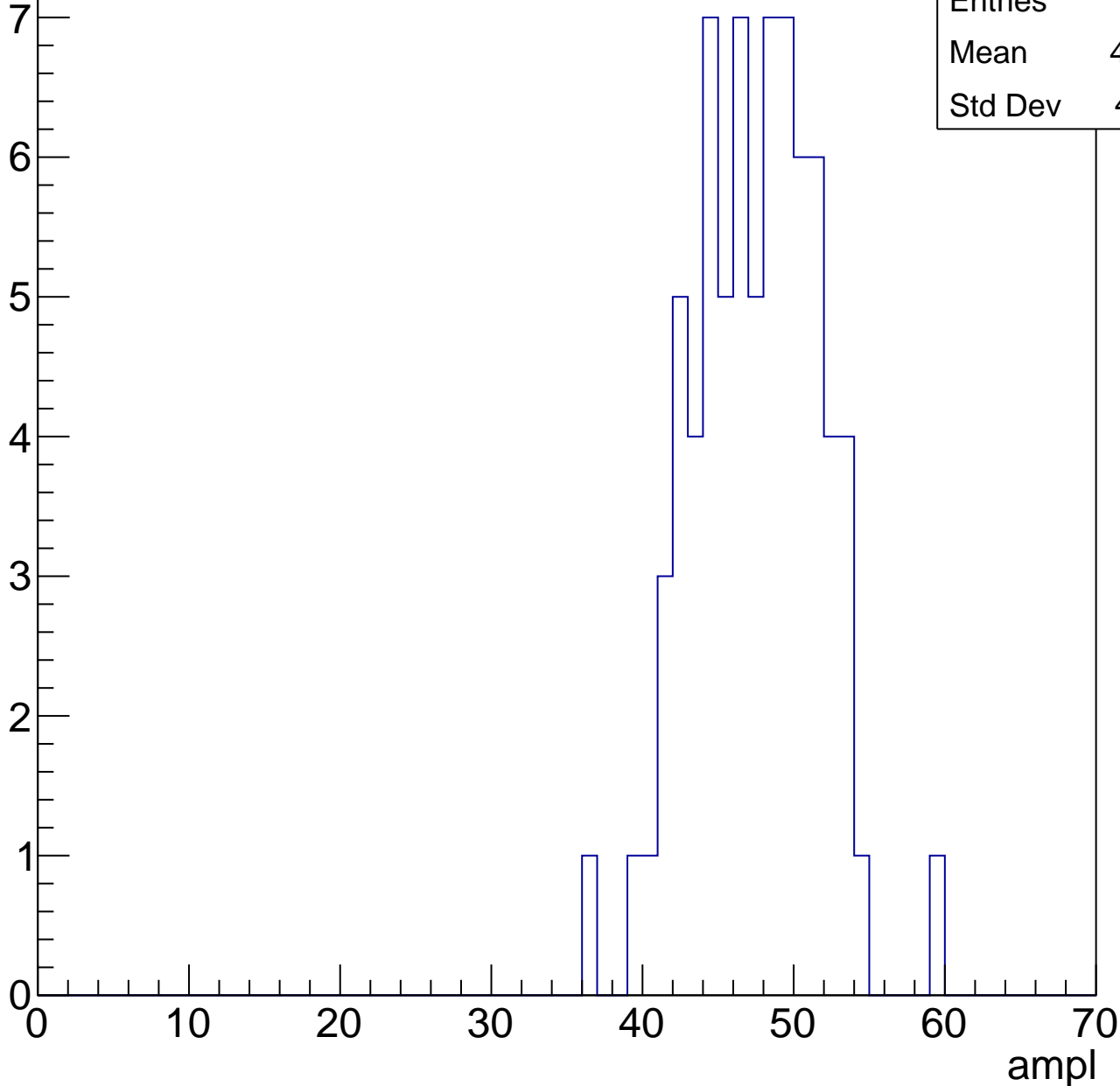


# B1L103S, U2-ch40, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	47.04
Std Dev	4.071

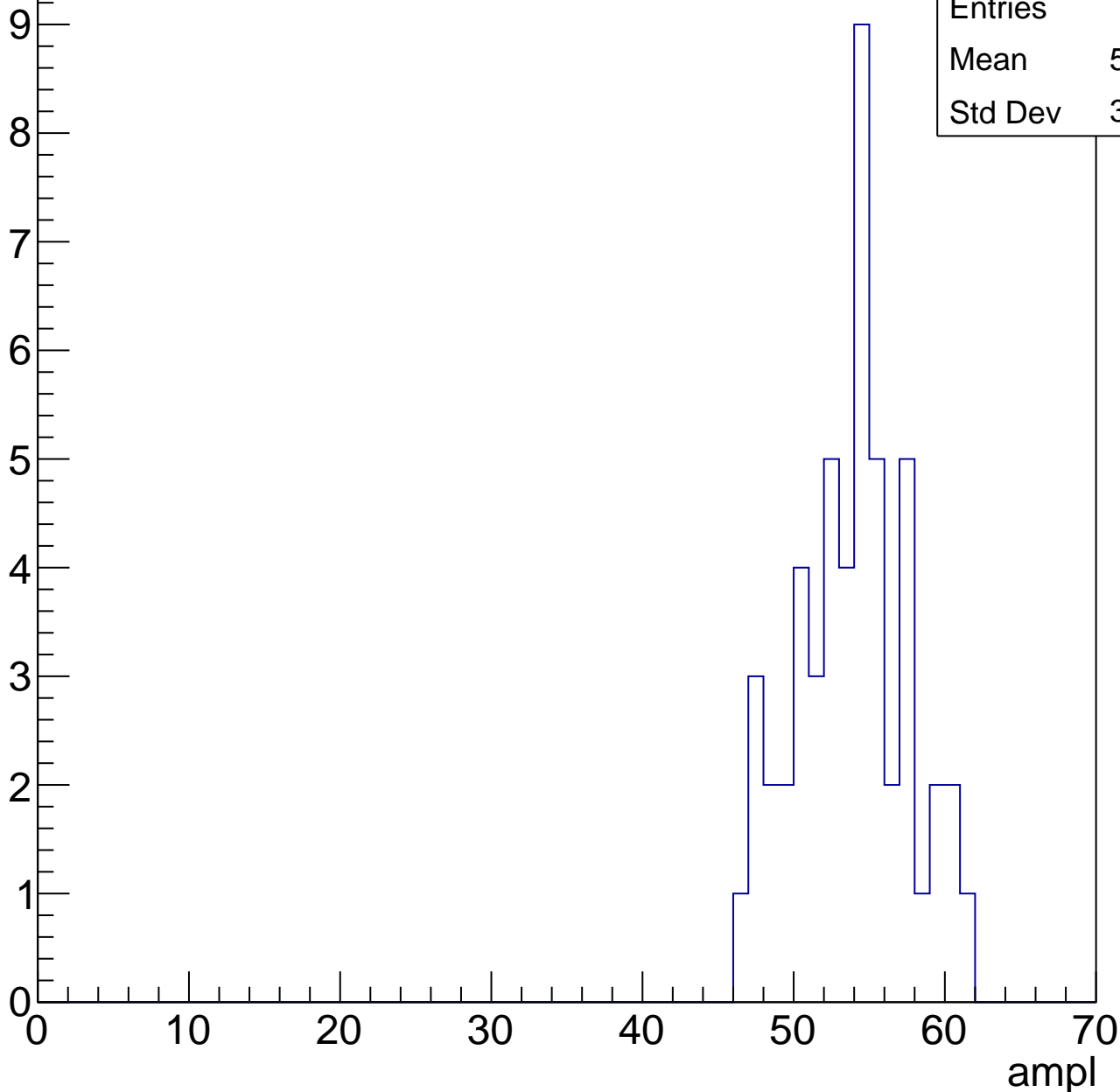


# B1L103S, U2-ch40, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

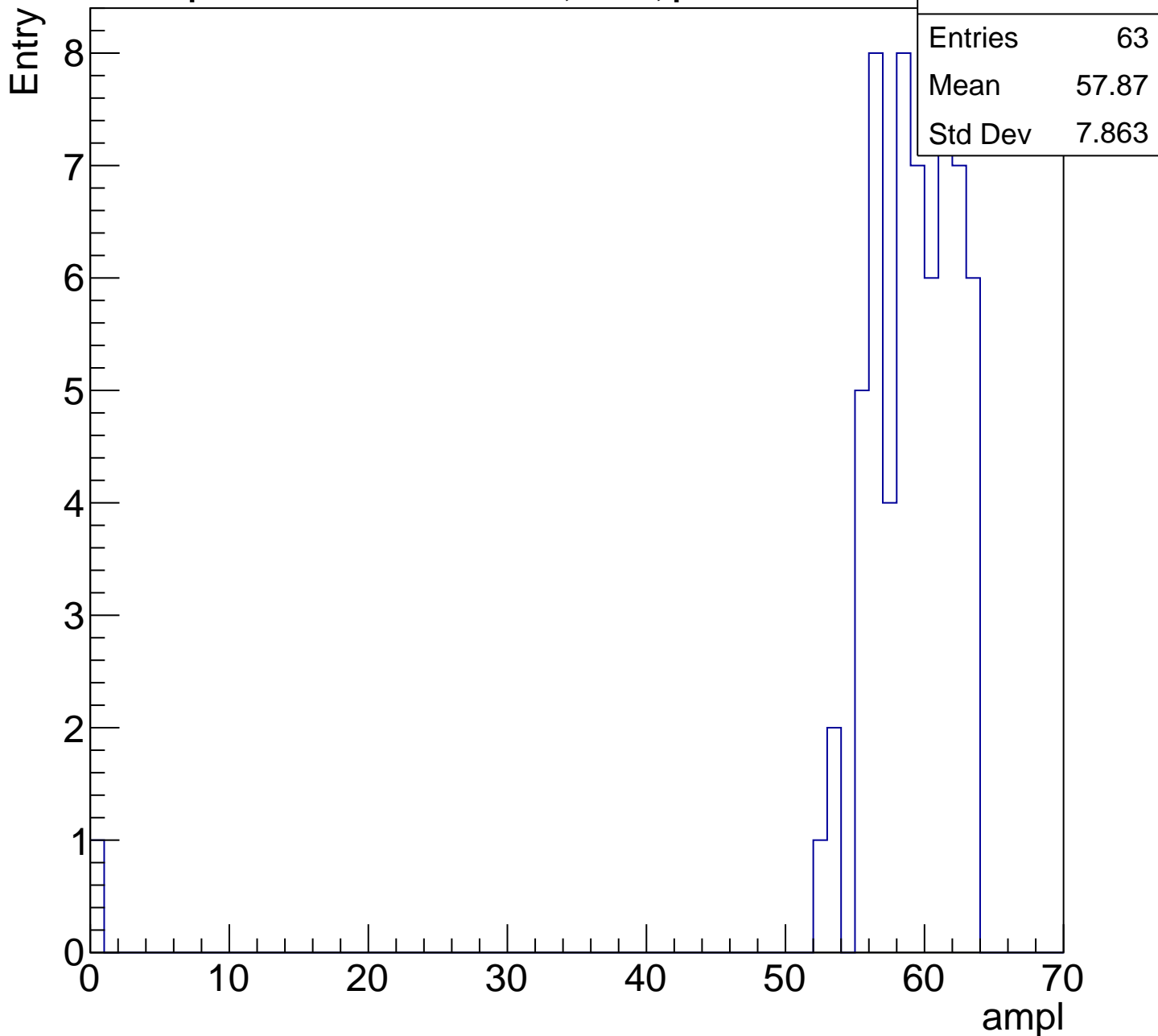
Entry

Entries	51
Mean	53.35
Std Dev	3.629



# B1L103S, U2-ch40, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U2-ch40, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries

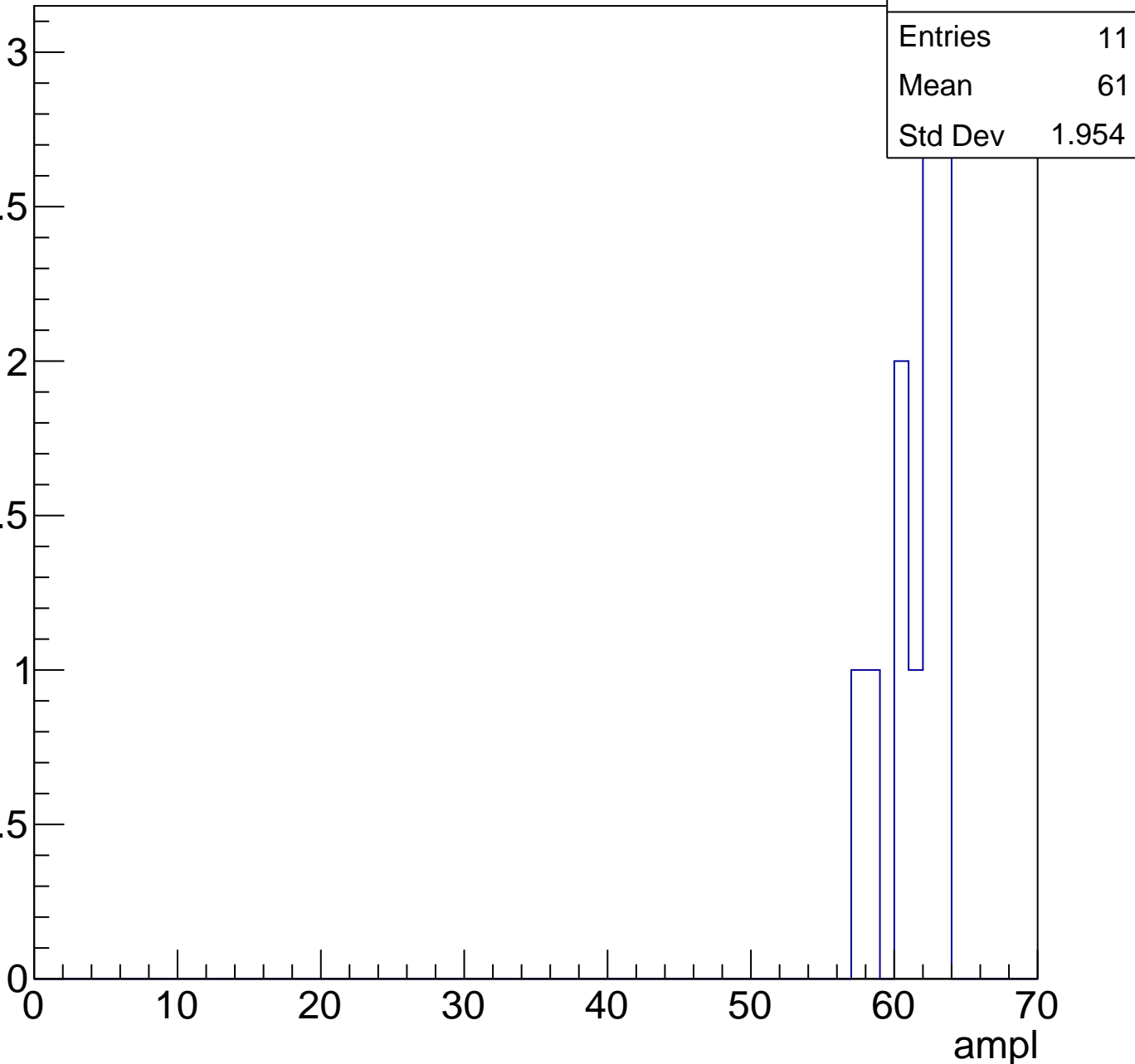
11

Mean

61

Std Dev

1.954





# B1L103S, U2-ch40, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch41, adc0

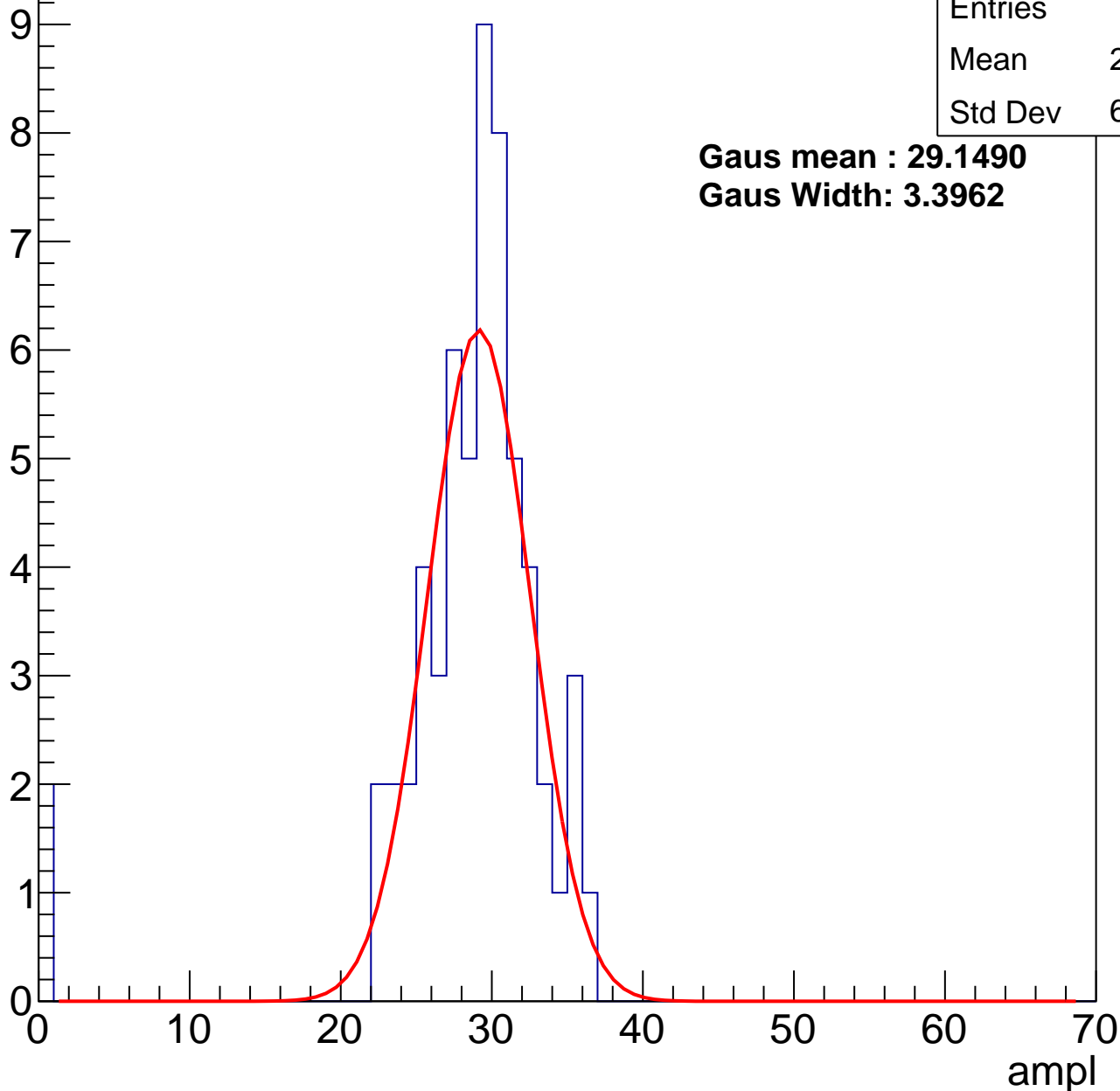
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	27.85
Std Dev	6.136

**Gaus mean : 29.1490**

**Gaus Width: 3.3962**



# B1L103S, U2-ch41, adc1

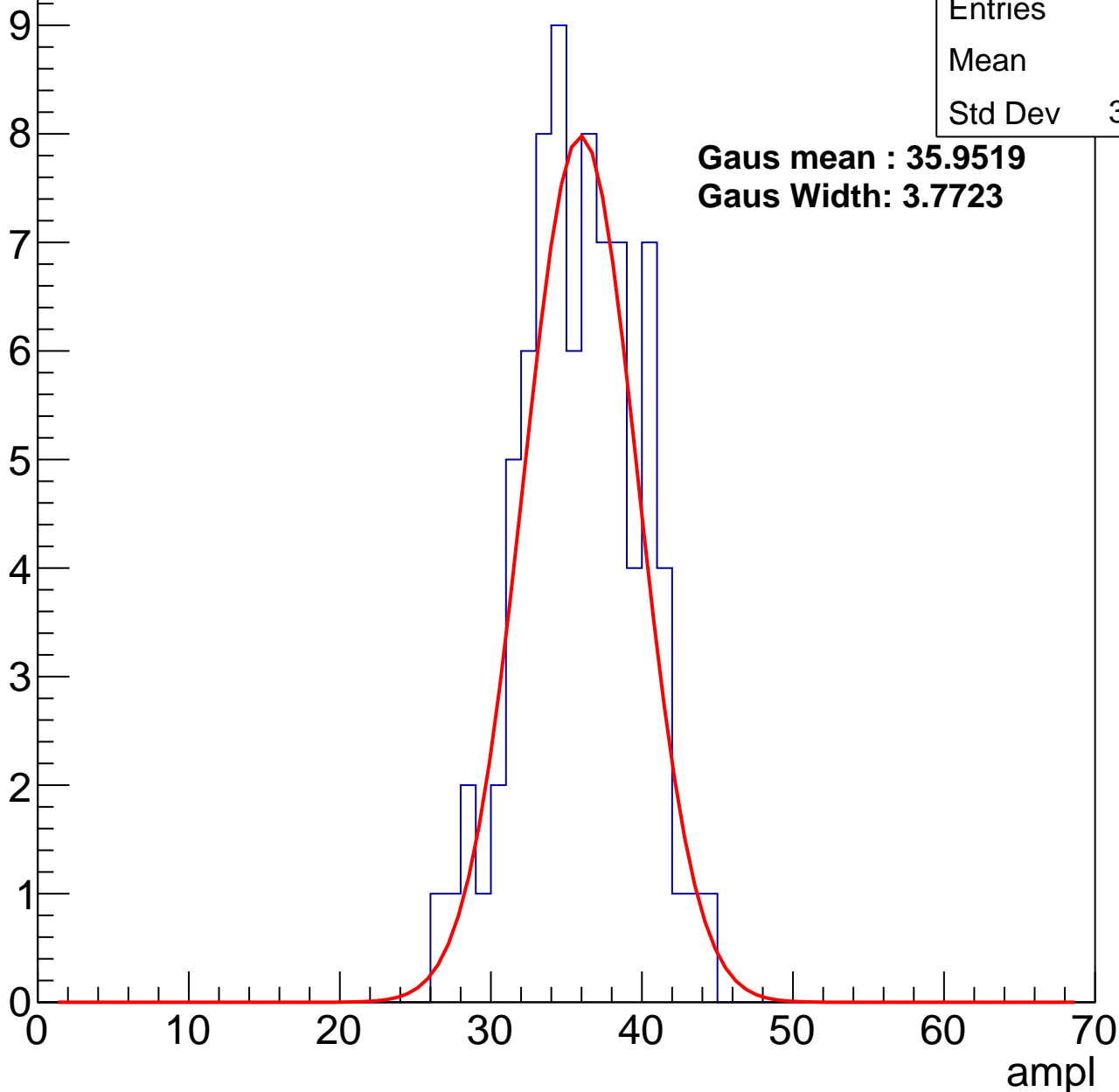
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	81
Mean	35.4
Std Dev	3.796

**Gaus mean : 35.9519**

**Gaus Width: 3.7723**



# B1L103S, U2-ch41, adc2

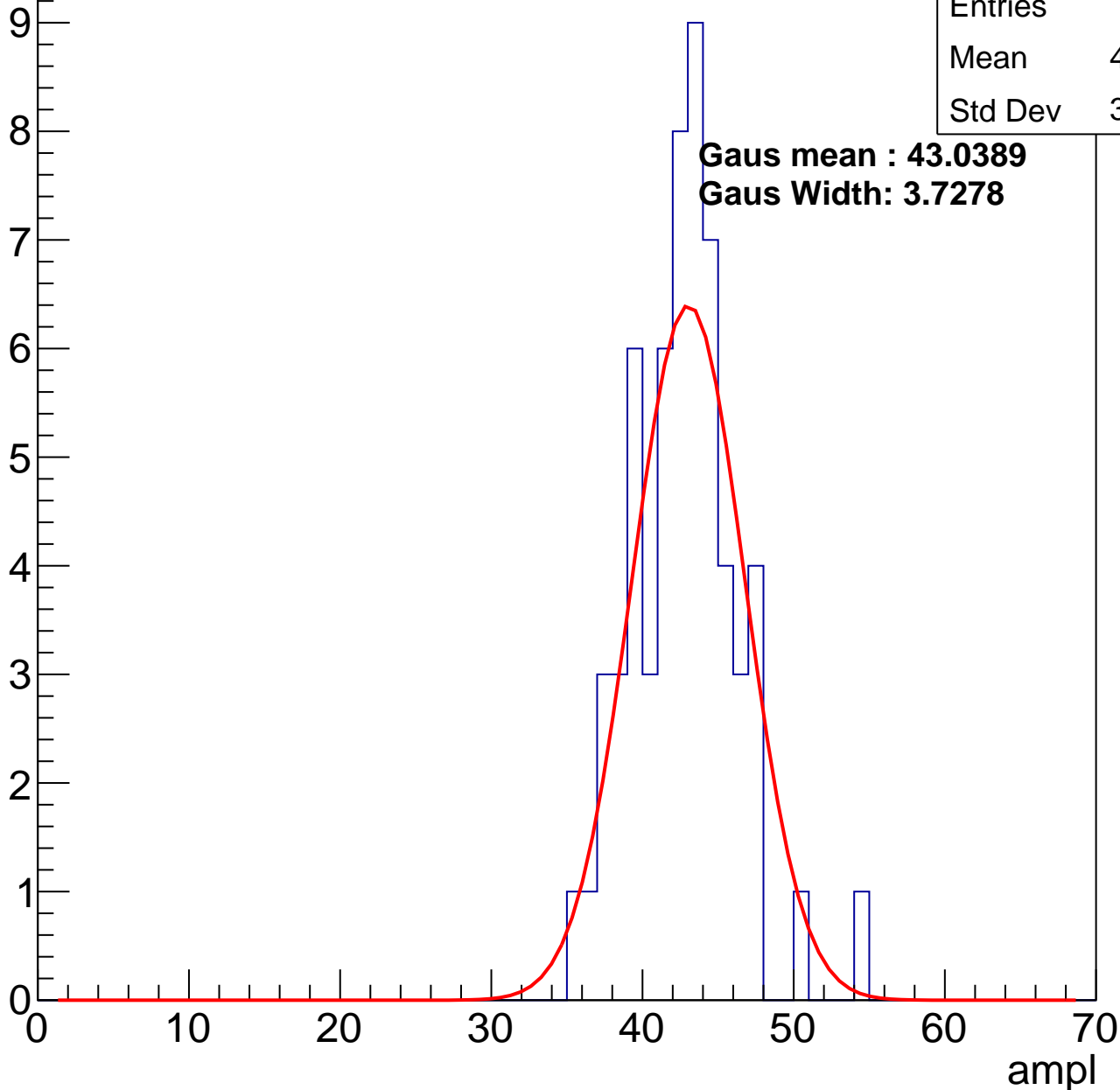
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	42.28
Std Dev	3.426

**Gaus mean : 43.0389**

**Gaus Width: 3.7278**



# B1L103S, U2-ch41, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

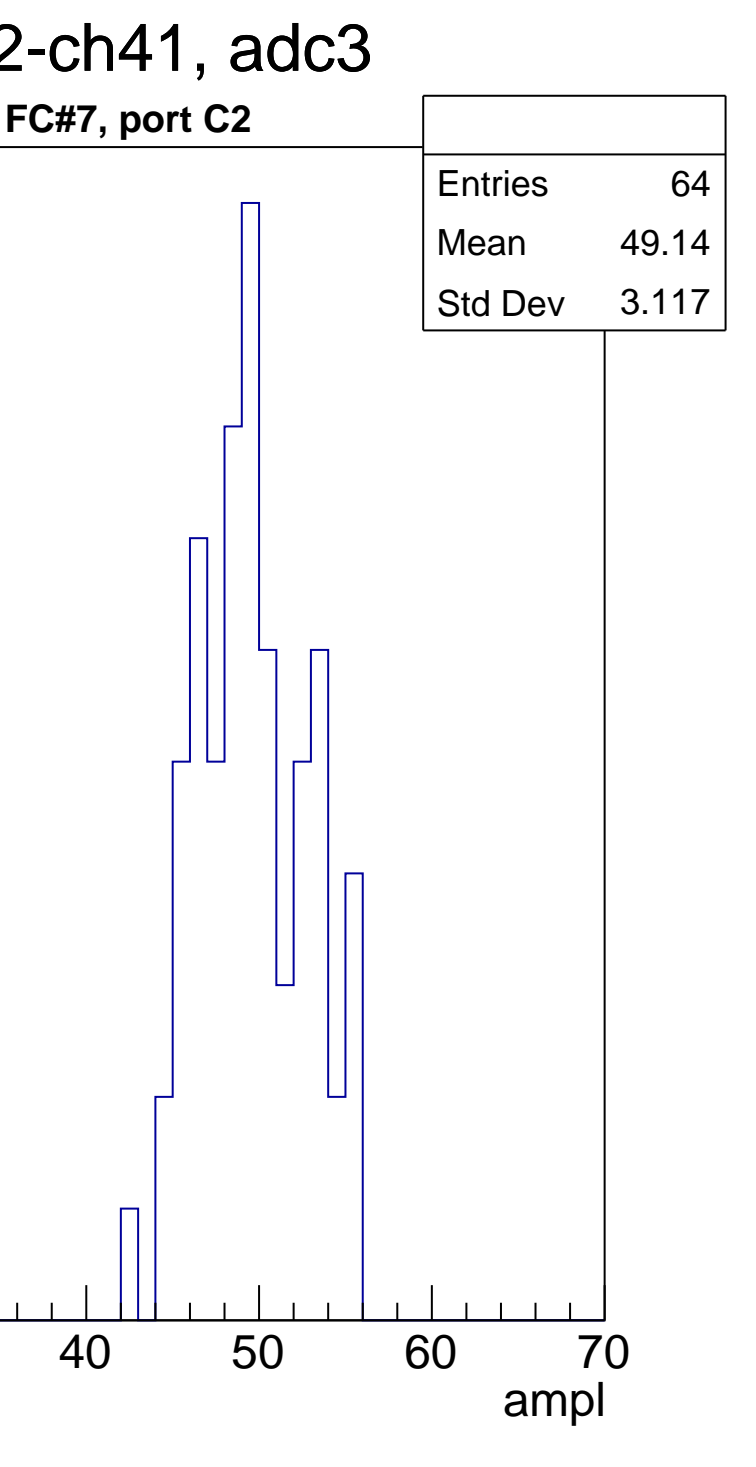
Entries	64
Mean	49.14
Std Dev	3.117

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

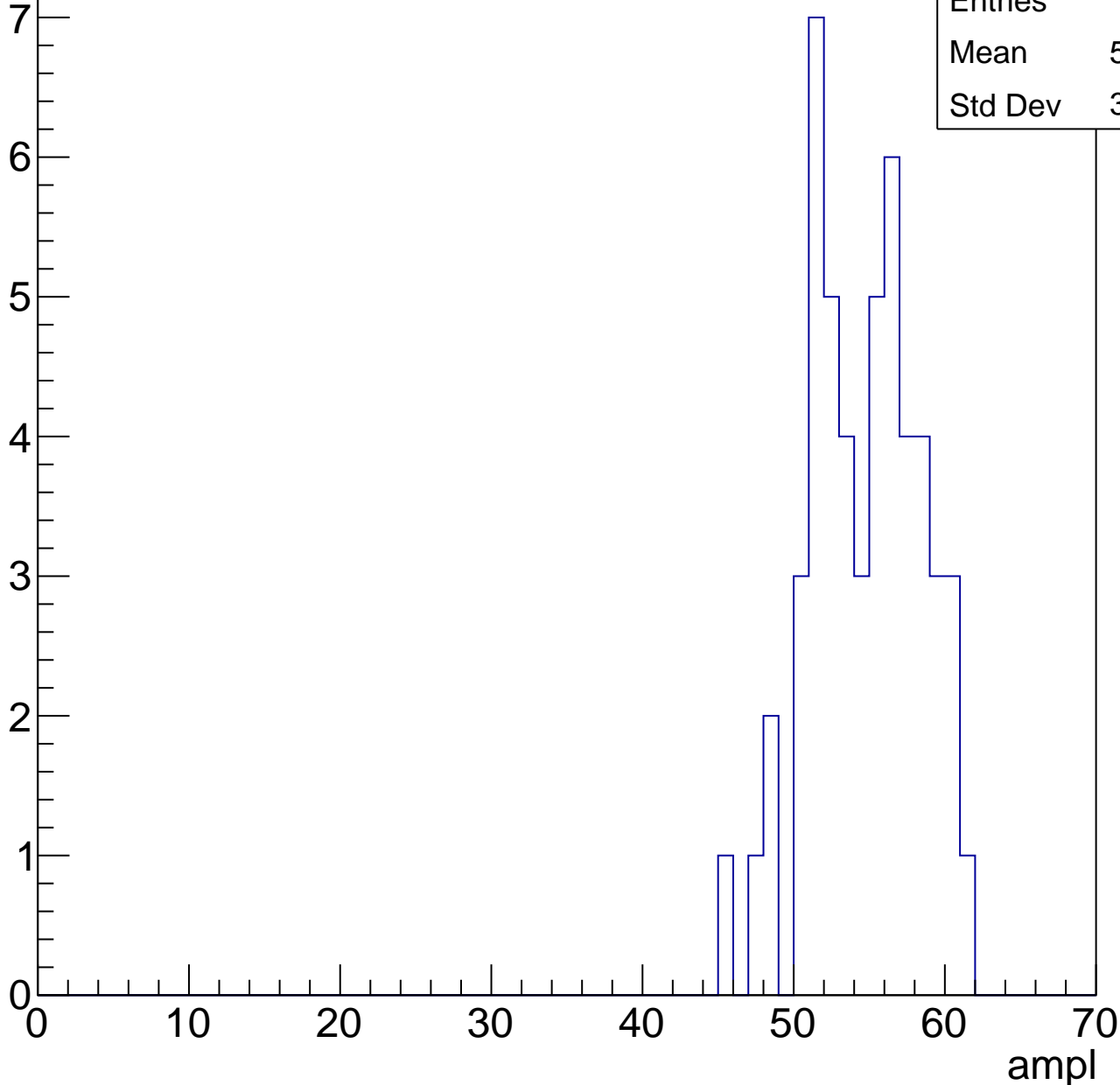


# B1L103S, U2-ch41, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	54.19
Std Dev	3.659

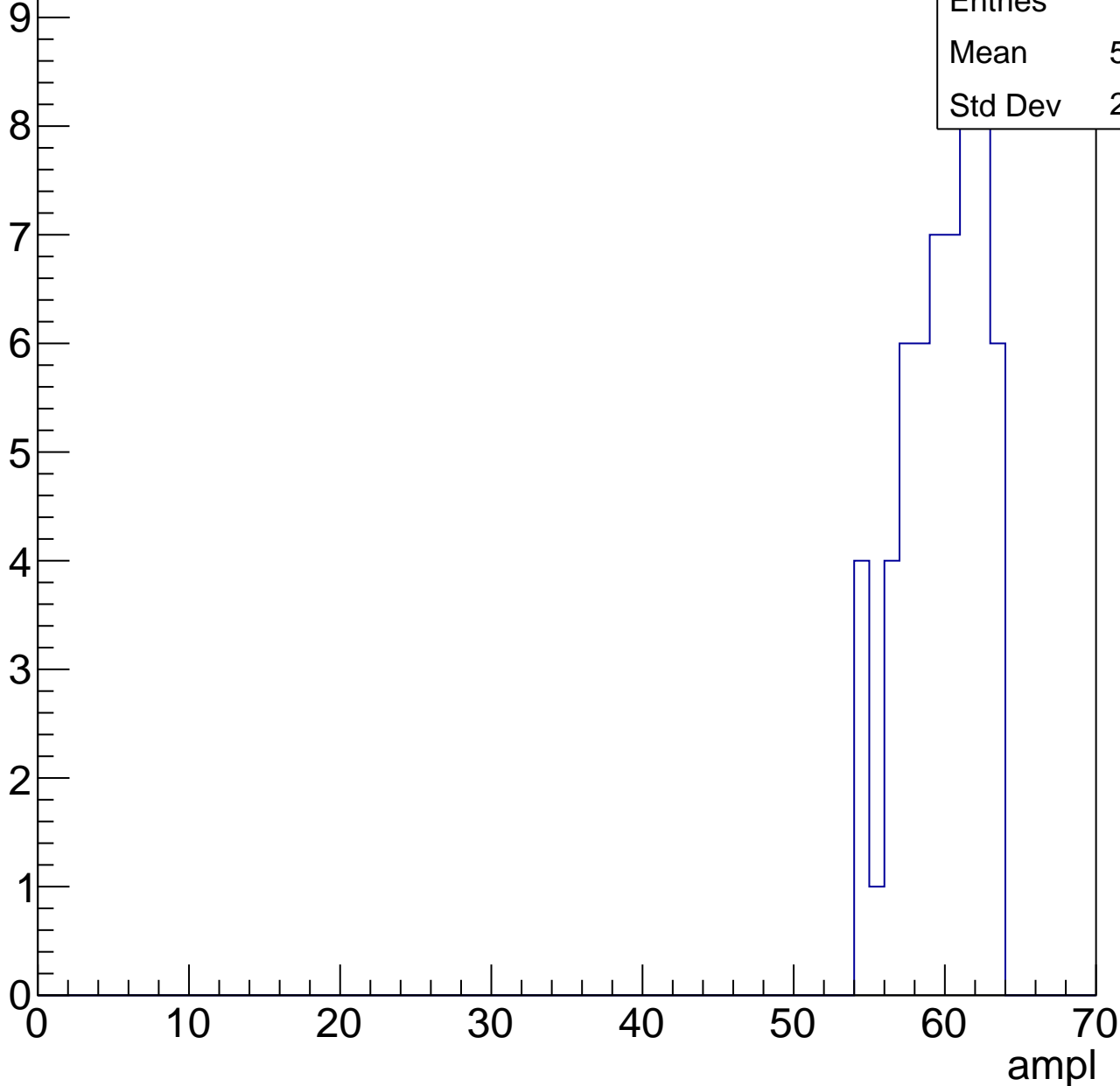


# B1L103S, U2-ch41, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

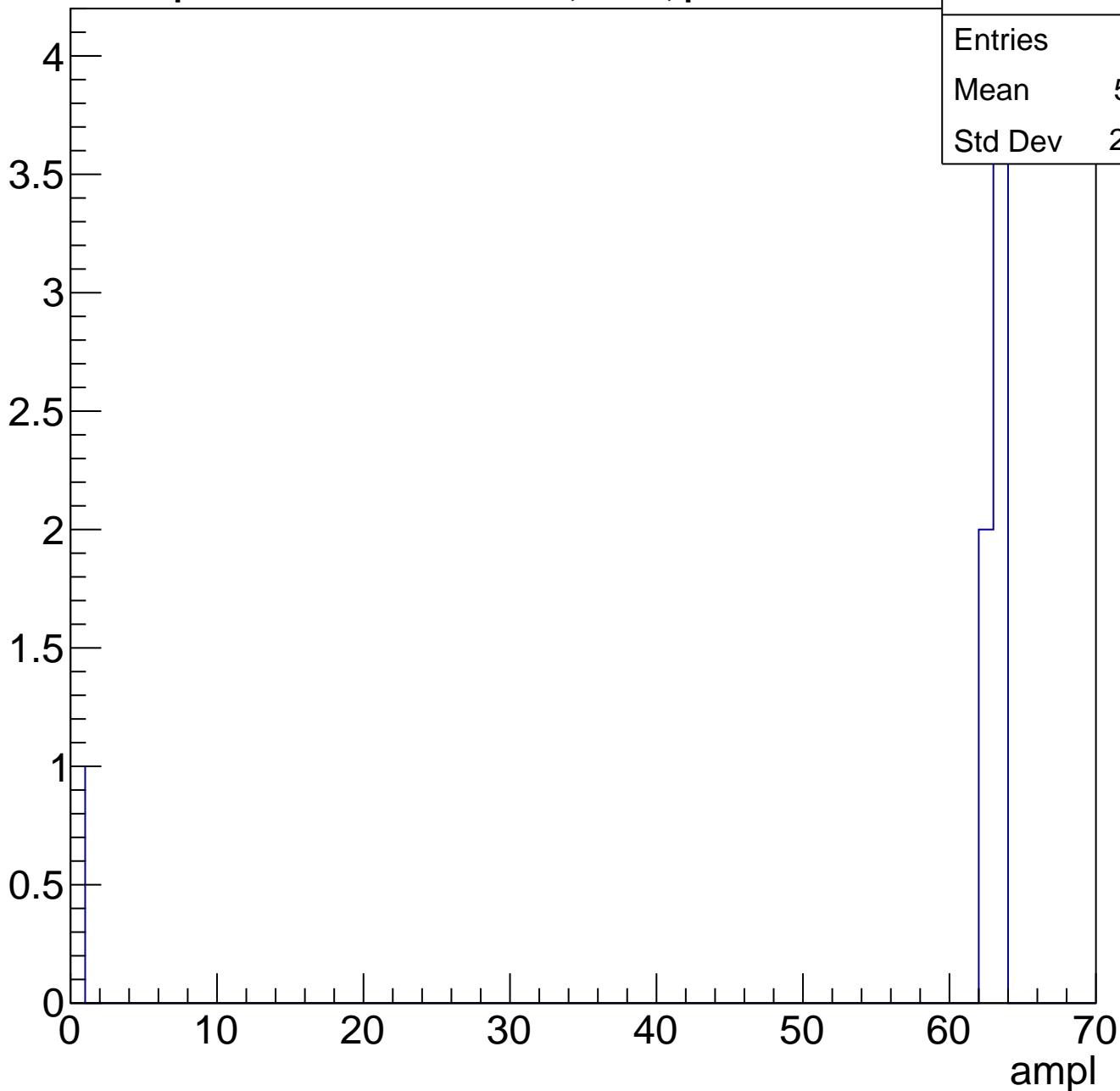
Entries	58
Mean	59.33
Std Dev	2.582



# B1L103S, U2-ch41, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U2-ch41, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U2-ch42, adc0

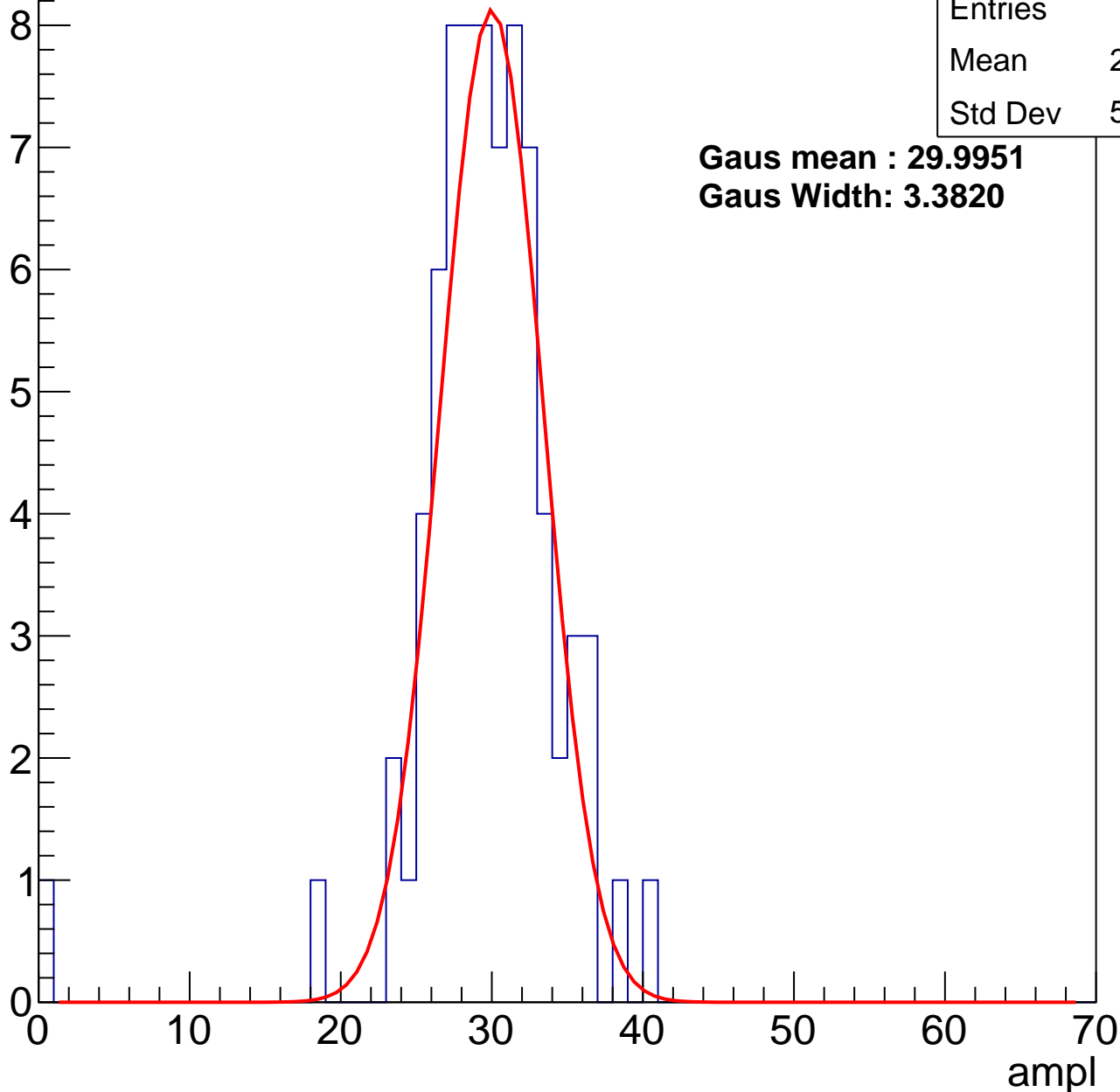
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	29.19
Std Dev	5.016

**Gaus mean : 29.9951**

**Gaus Width: 3.3820**



# B1L103S, U2-ch42, adc1

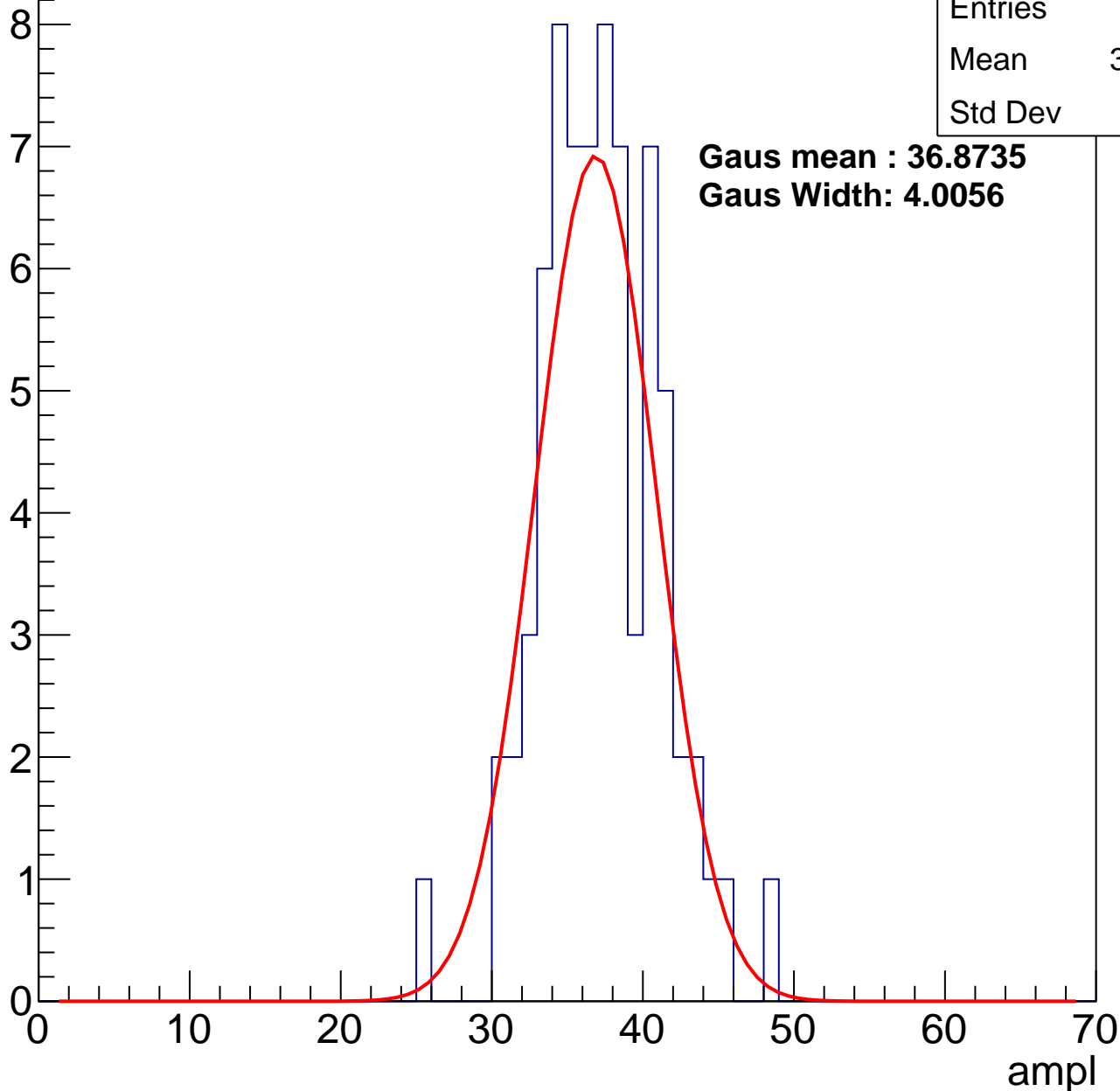
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	36.73
Std Dev	3.89

**Gaus mean : 36.8735**

**Gaus Width: 4.0056**



# B1L103S, U2-ch42, adc2

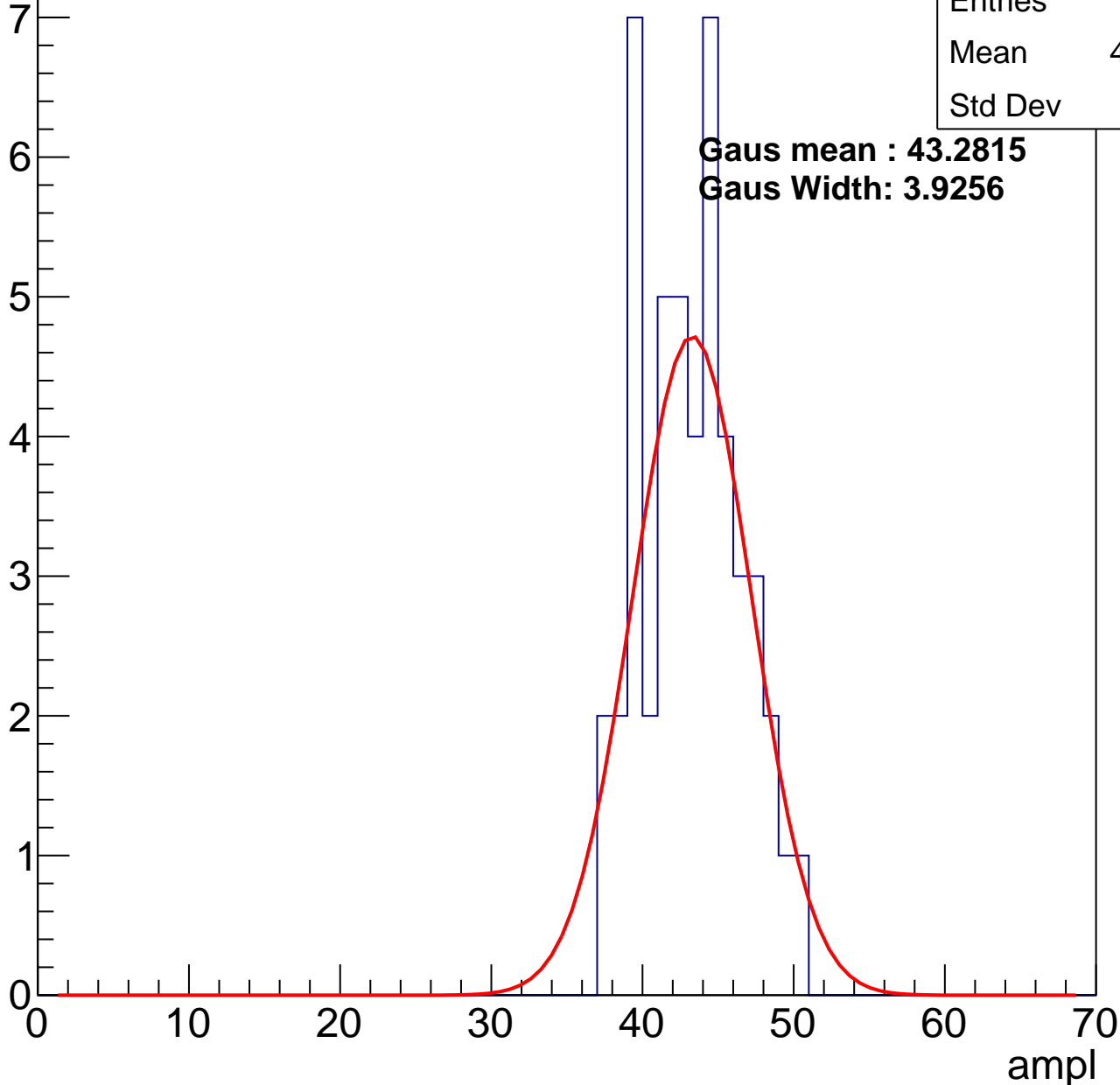
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	48
Mean	42.75
Std Dev	3.25

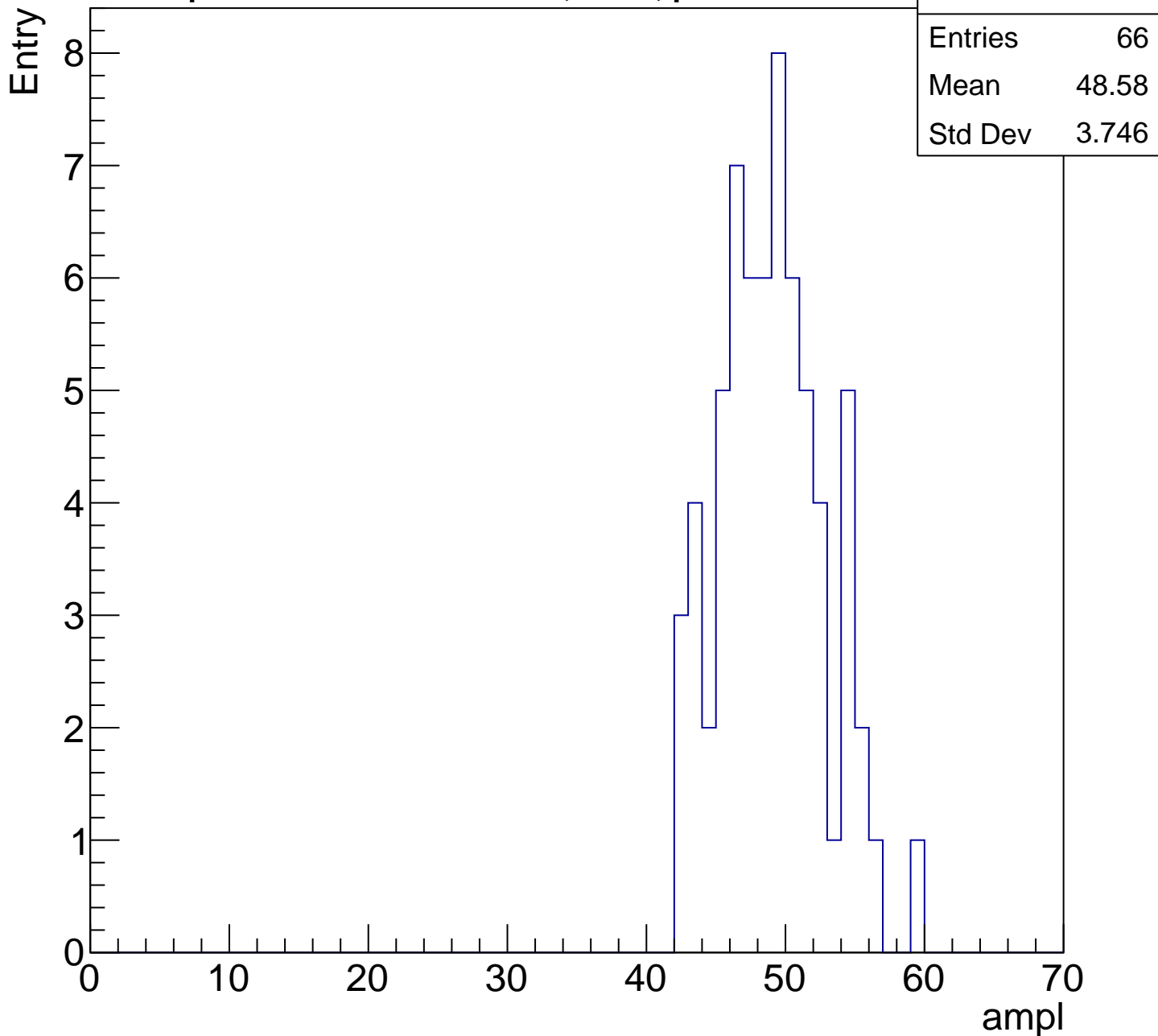
**Gaus mean : 43.2815**

**Gaus Width: 3.9256**



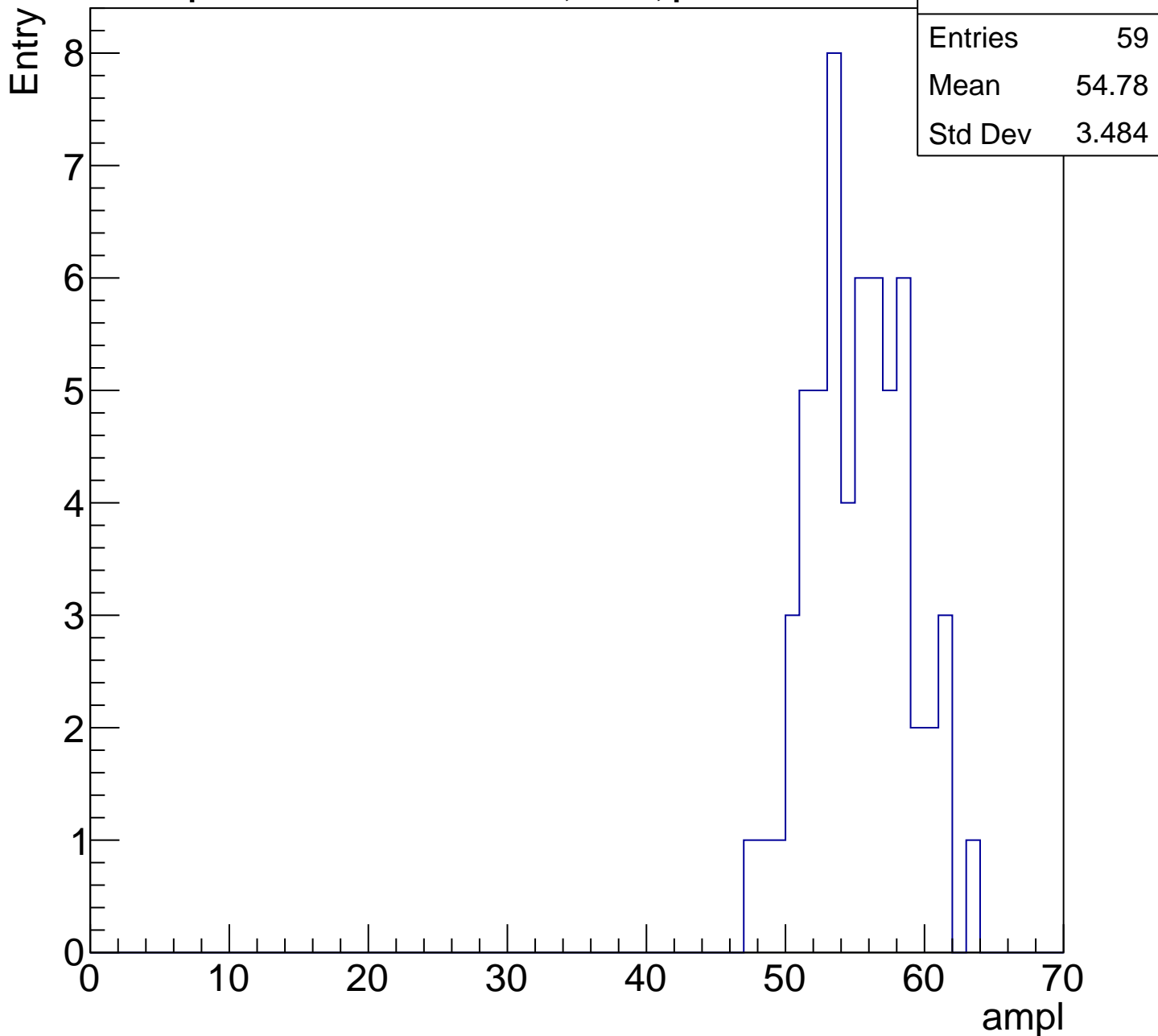
# B1L103S, U2-ch42, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2



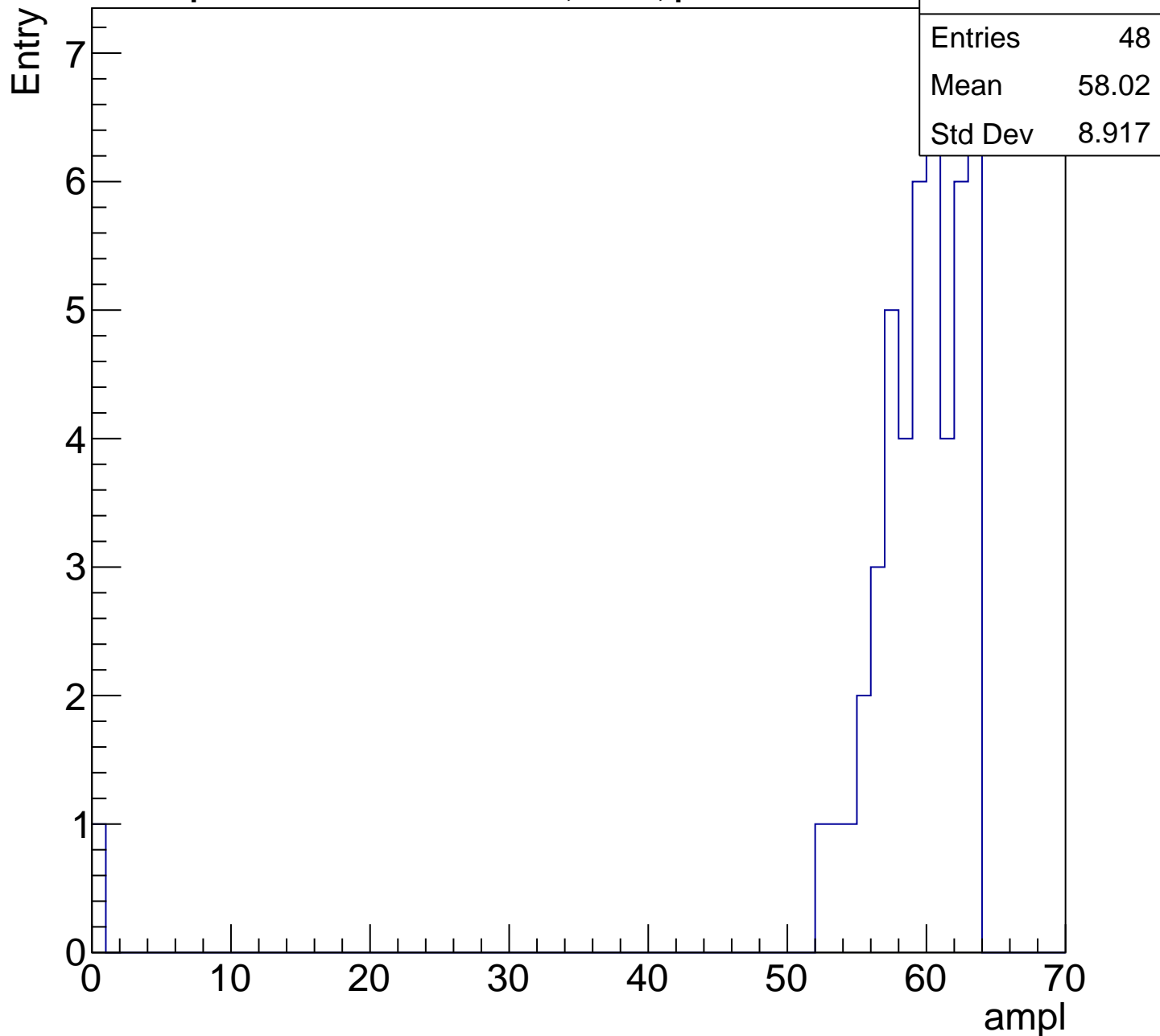
# B1L103S, U2-ch42, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U2-ch42, adc5

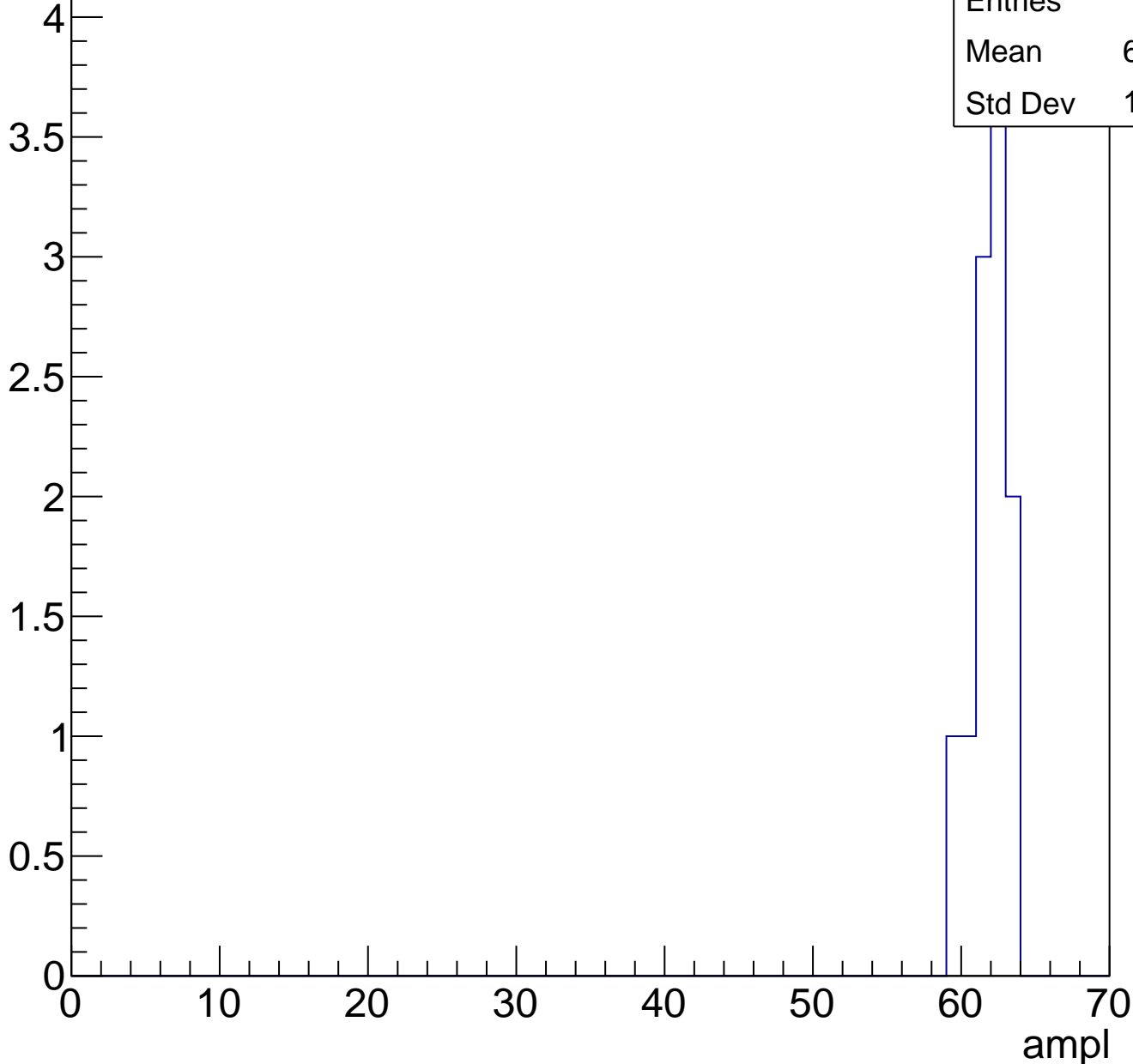
calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U2-ch42, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U2-ch42, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

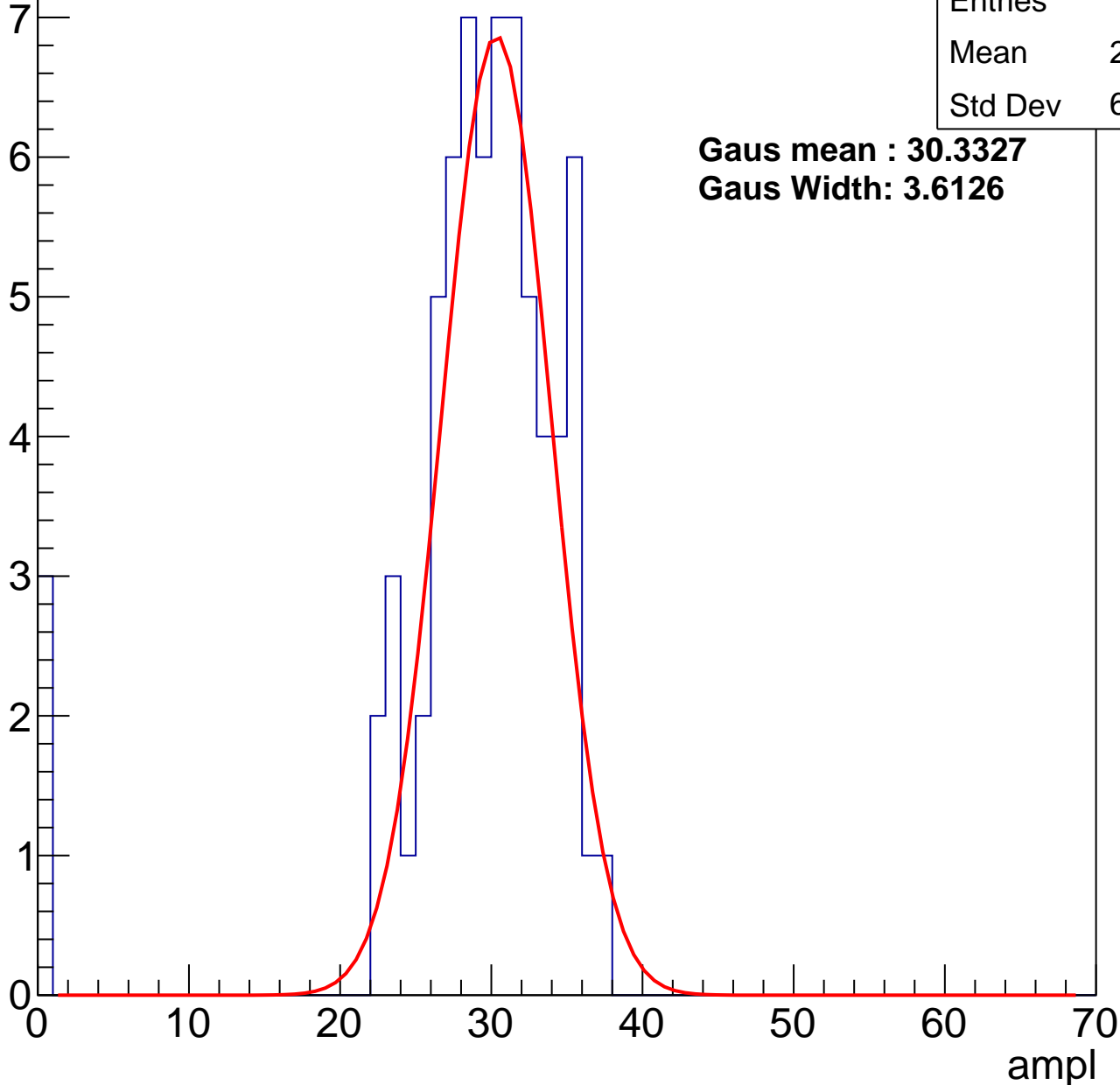
# B1L103S, U2-ch43, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	28.39
Std Dev	6.978

**Gaus mean : 30.3327**  
**Gaus Width: 3.6126**



# B1L103S, U2-ch43, adc1

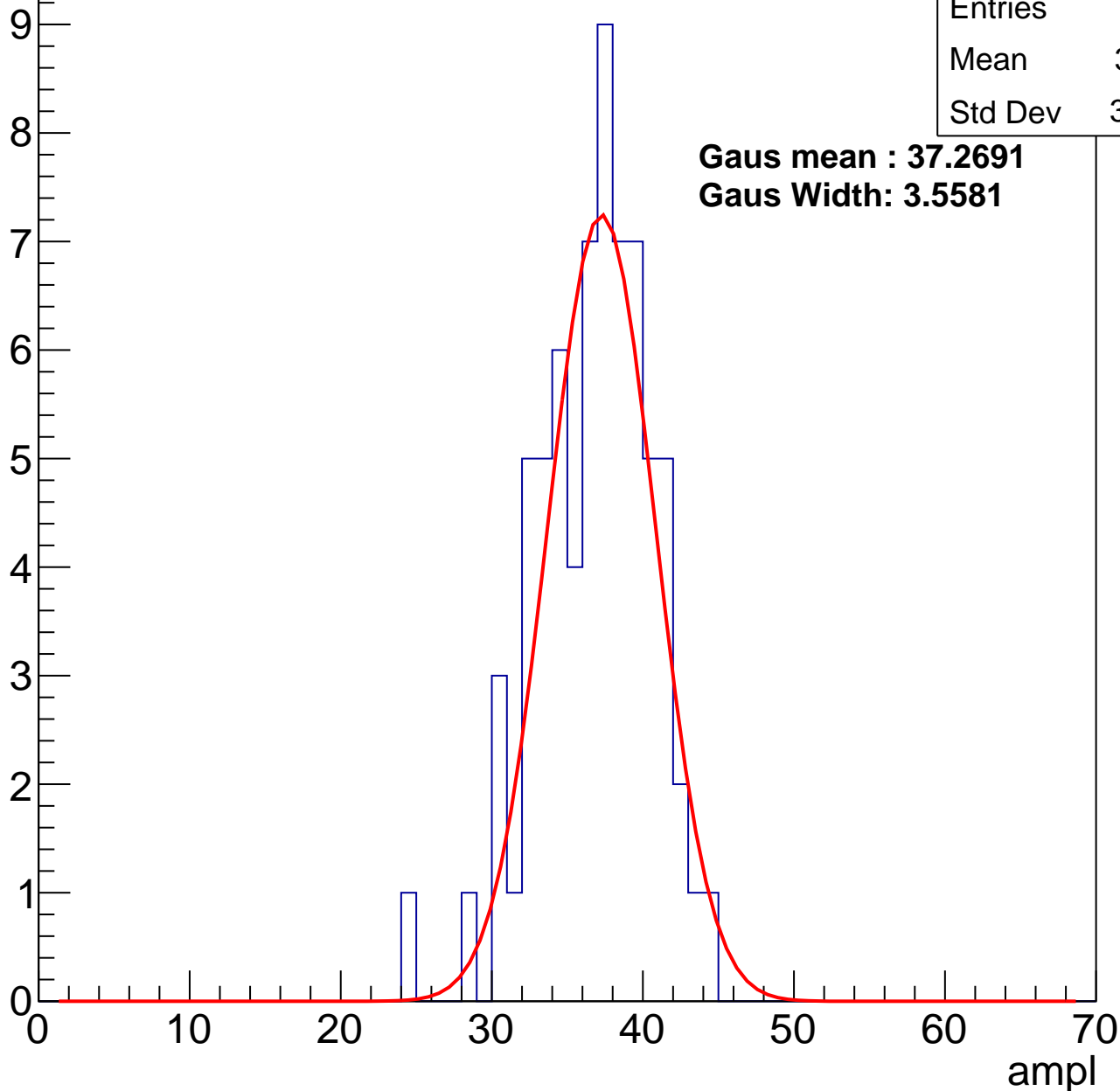
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	36.31
Std Dev	3.736

**Gaus mean : 37.2691**

**Gaus Width: 3.5581**



# B1L103S, U2-ch43, adc2

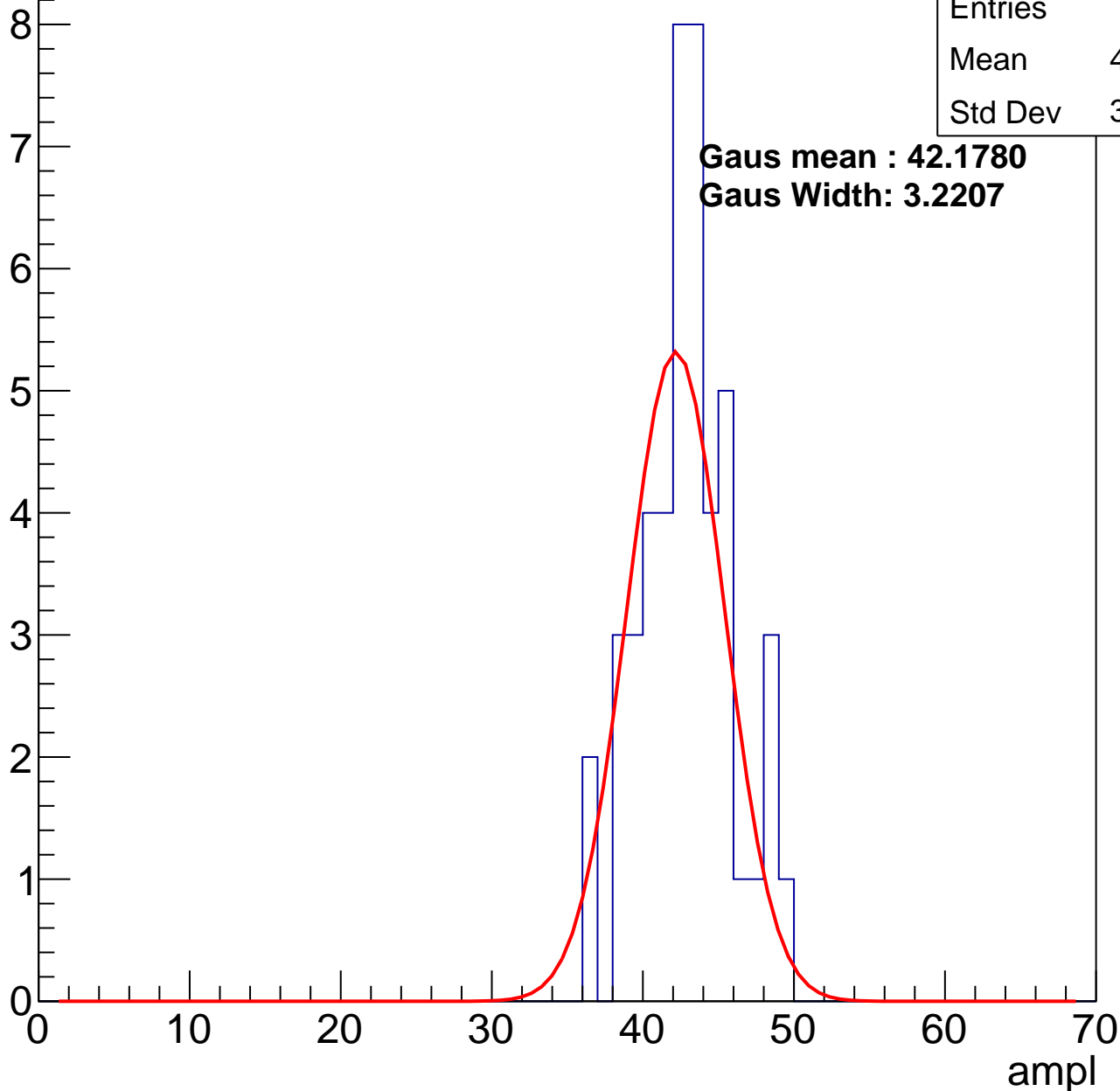
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	47
Mean	42.43
Std Dev	3.009

**Gaus mean : 42.1780**

**Gaus Width: 3.2207**

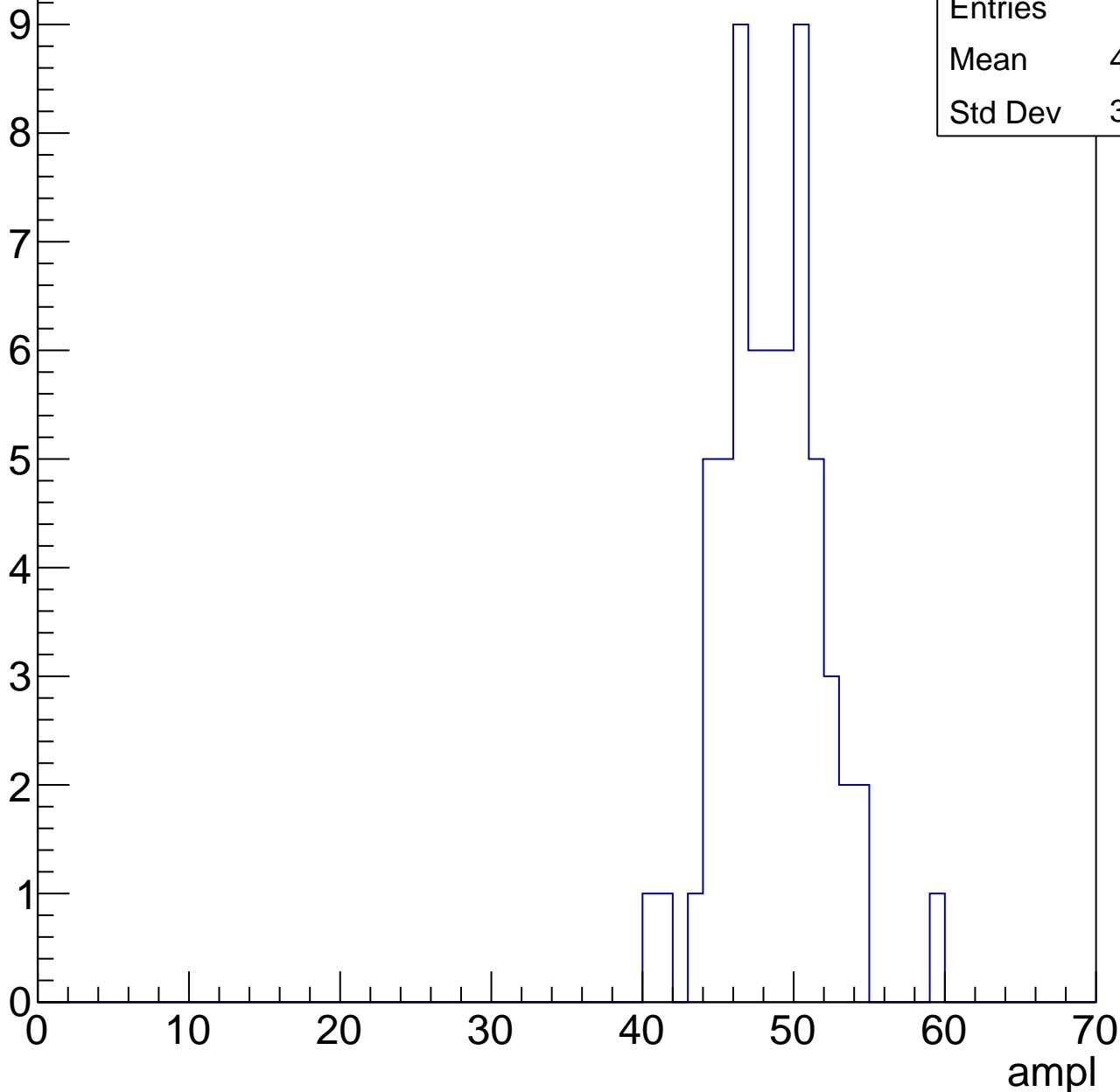


# B1L103S, U2-ch43, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

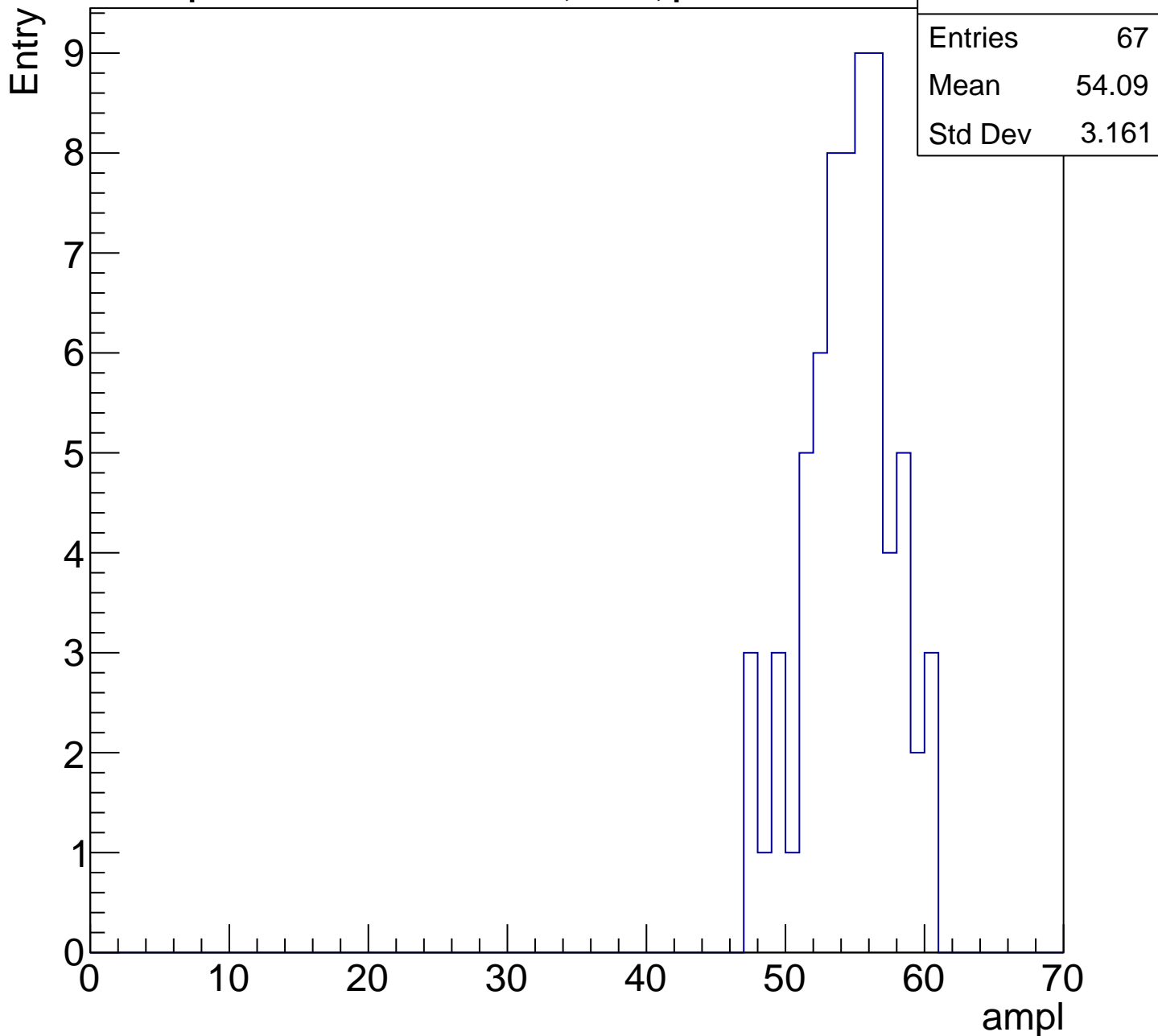
Entry

Entries	62
Mean	48.08
Std Dev	3.318



# B1L103S, U2-ch43, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

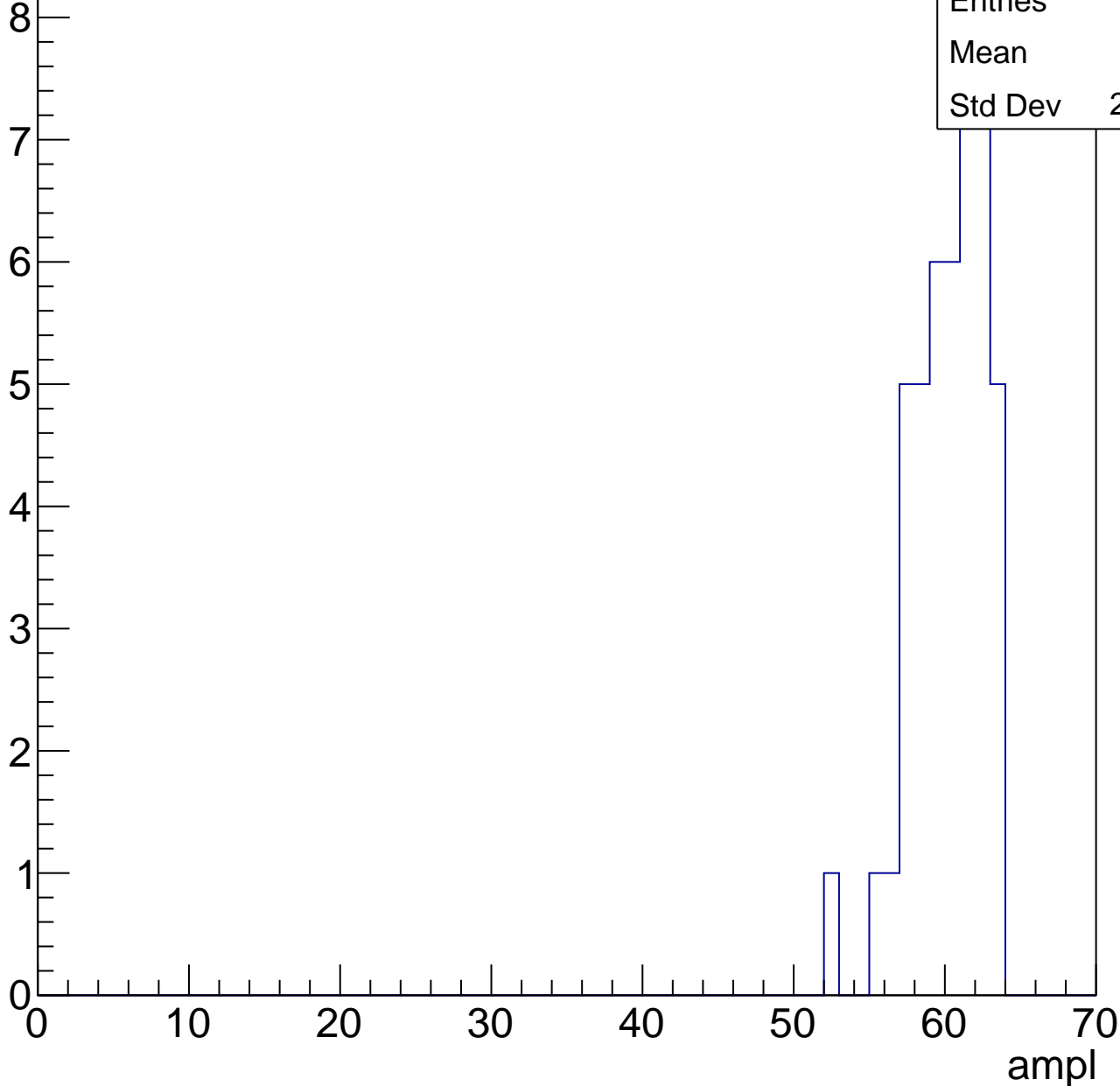


# B1L103S, U2-ch43, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

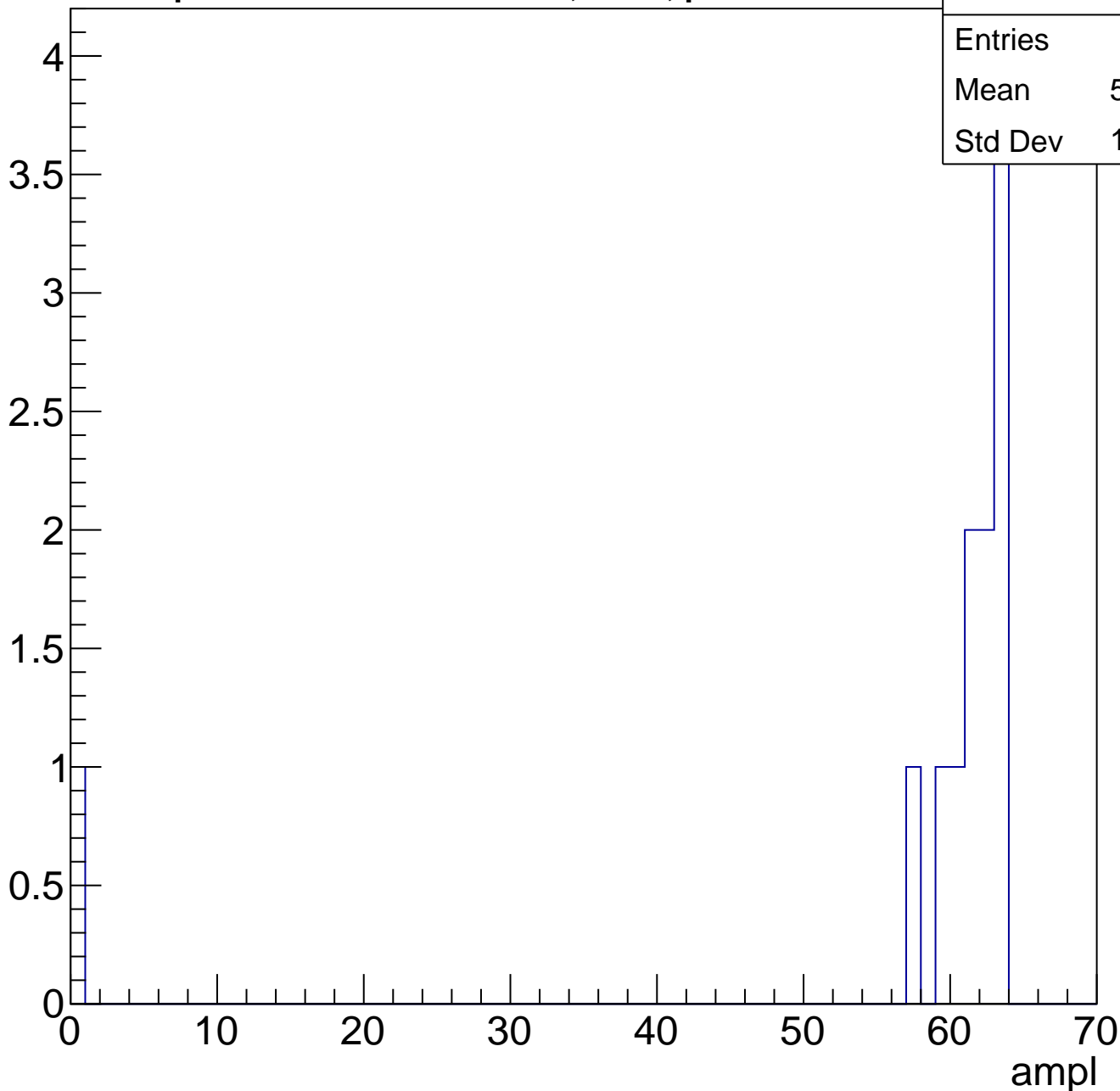
Entries	46
Mean	59.8
Std Dev	2.374



# B1L103S, U2-ch43, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



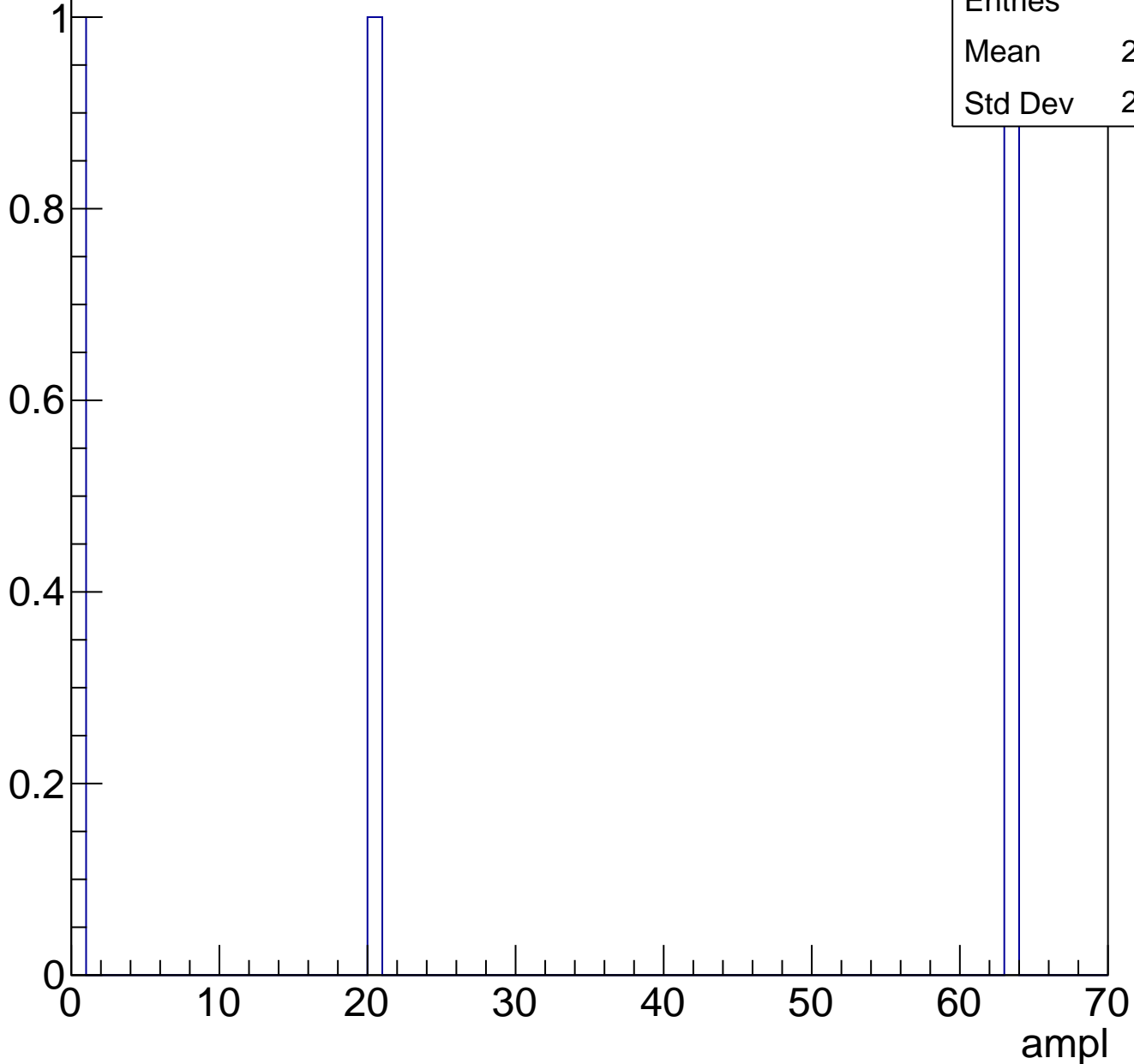
Entries	12
Mean	56.17
Std Dev	17.03



# B1L103S, U2-ch43, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	3
Mean	27.67
Std Dev	26.28

# B1L103S, U2-ch44, adc0

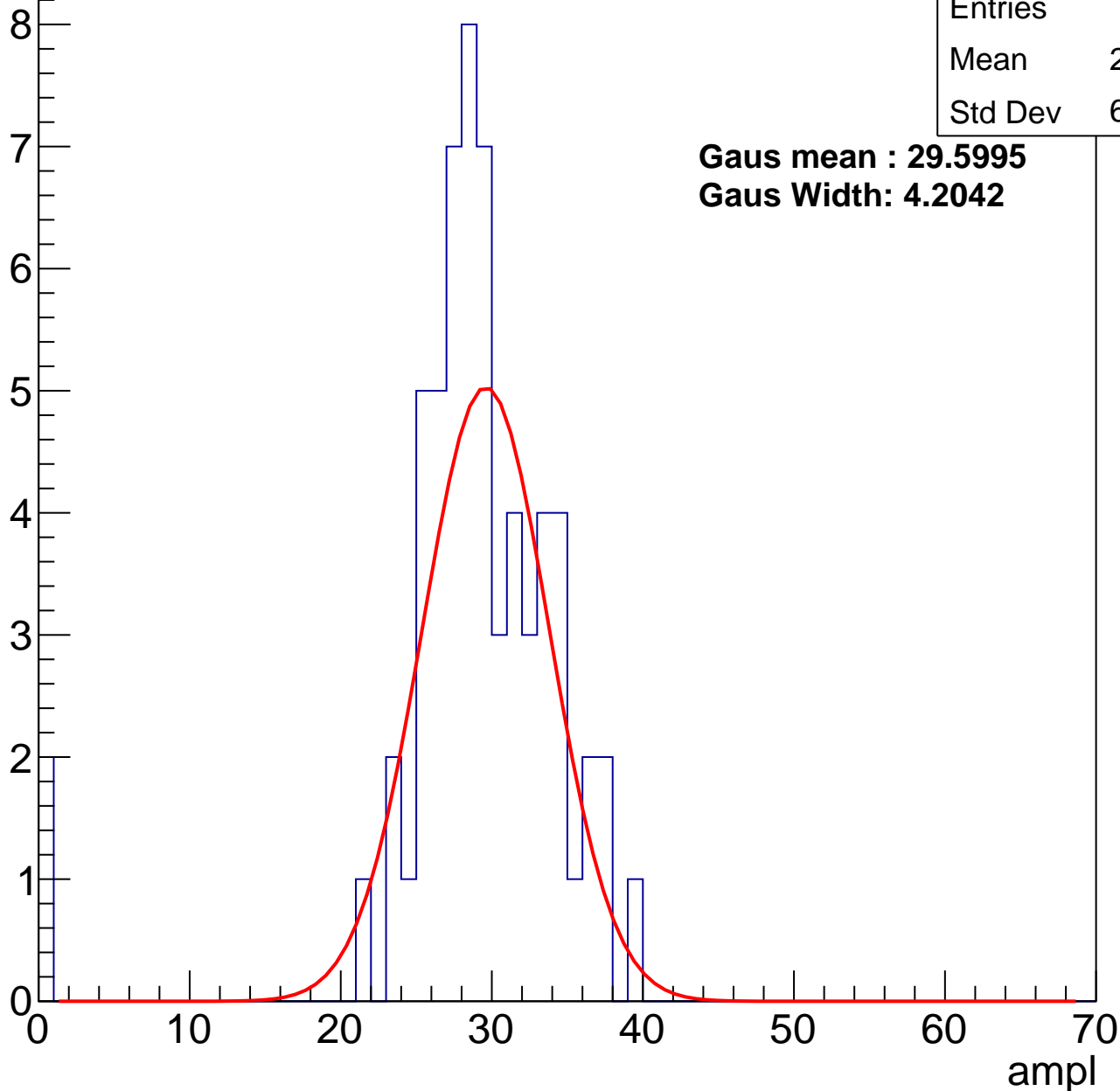
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	28.39
Std Dev	6.417

**Gaus mean : 29.5995**

**Gaus Width: 4.2042**



# B1L103S, U2-ch44, adc1

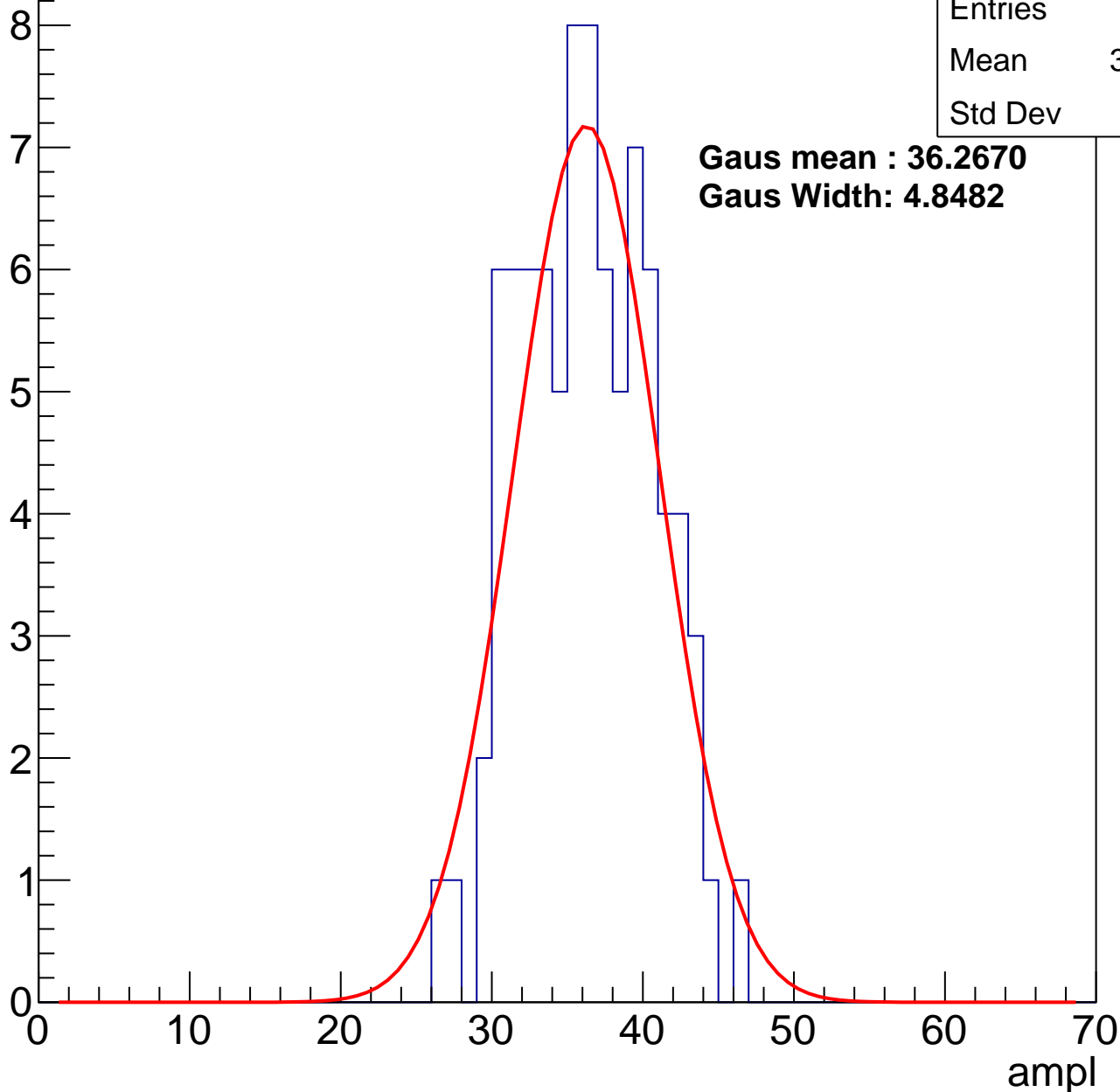
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	86
Mean	35.83
Std Dev	4.26

**Gaus mean : 36.2670**

**Gaus Width: 4.8482**



# B1L103S, U2-ch44, adc2

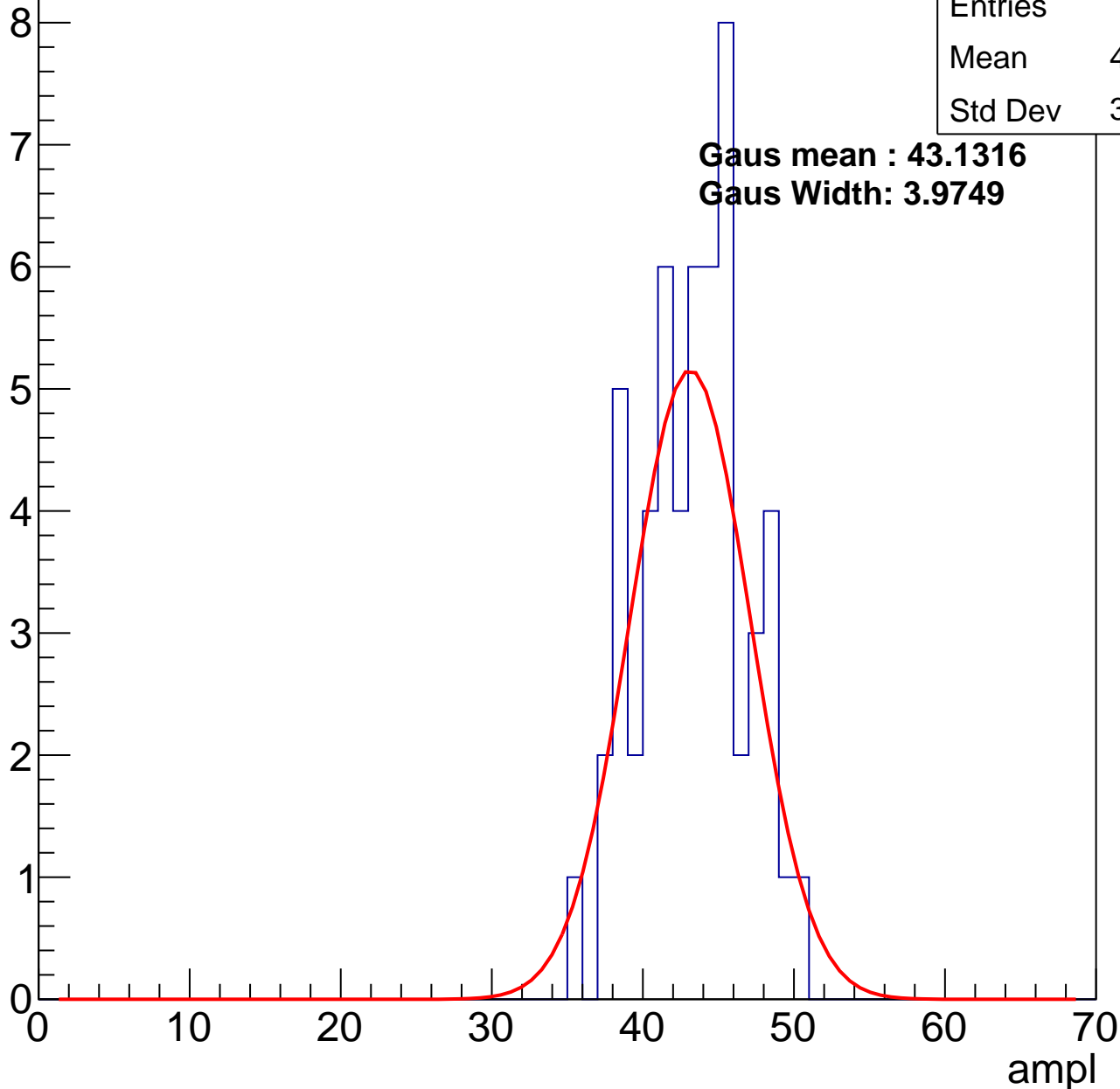
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	42.85
Std Dev	3.424

**Gaus mean : 43.1316**

**Gaus Width: 3.9749**

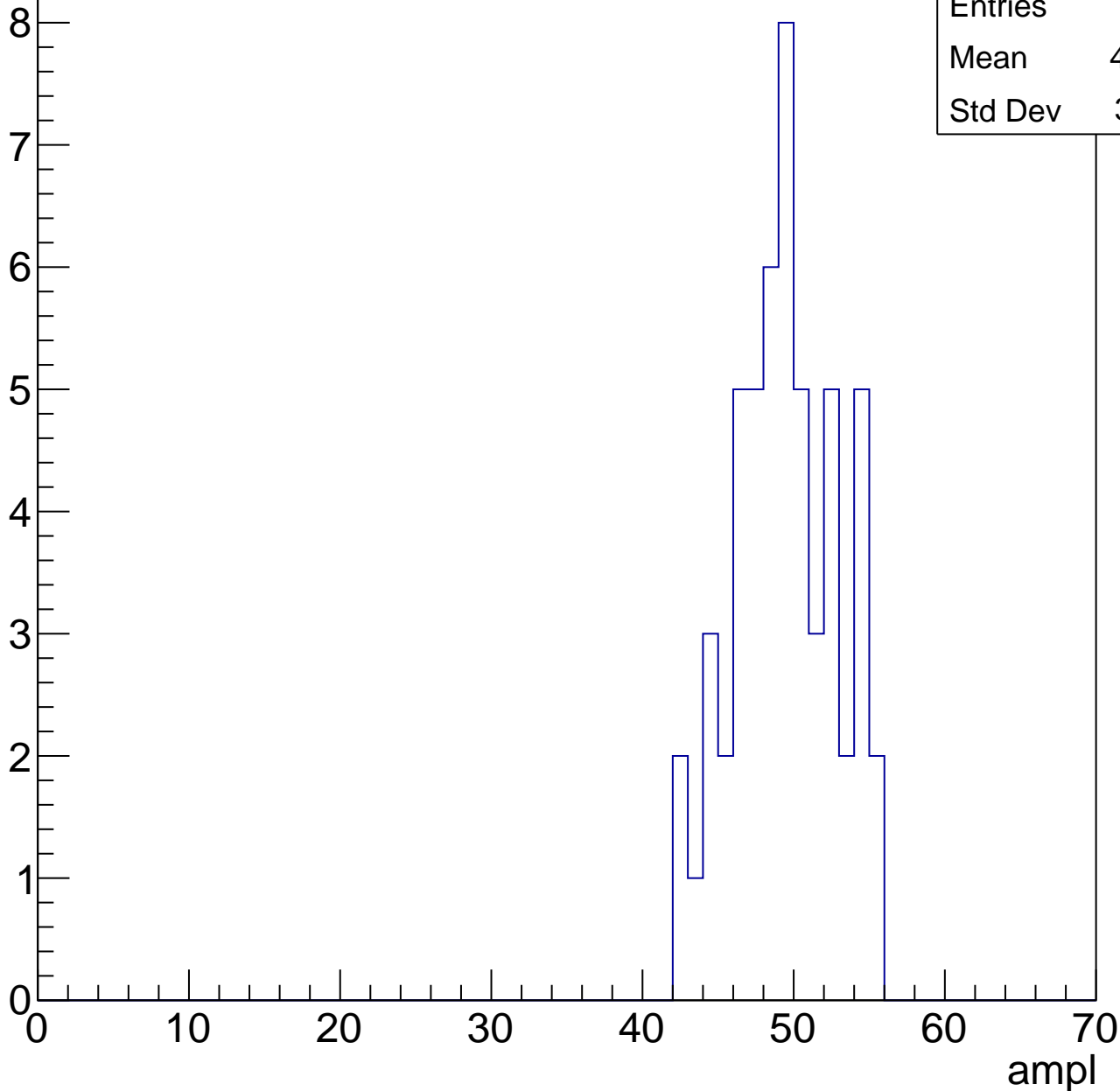


# B1L103S, U2-ch44, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

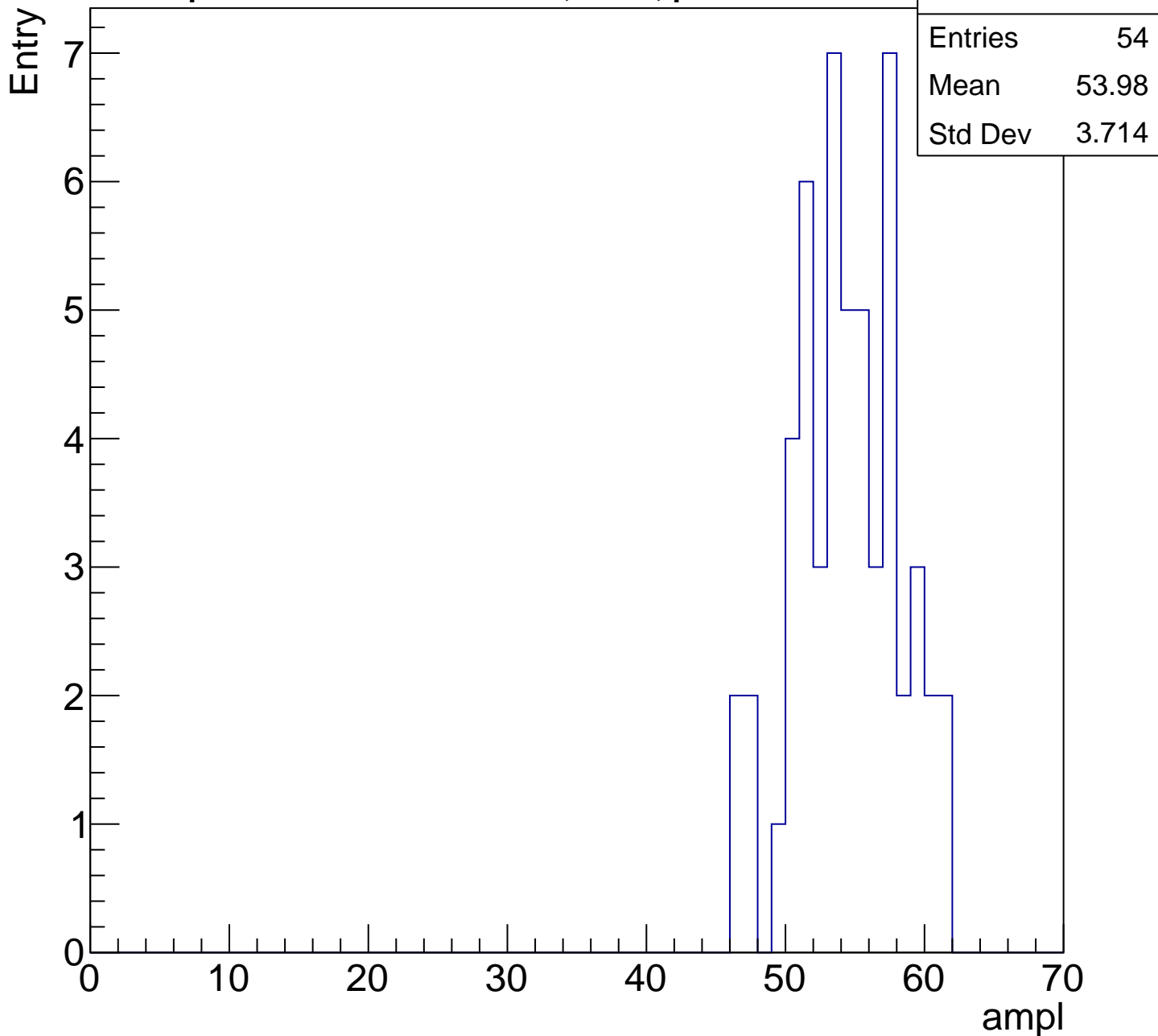
Entry

Entries	54
Mean	48.94
Std Dev	3.341



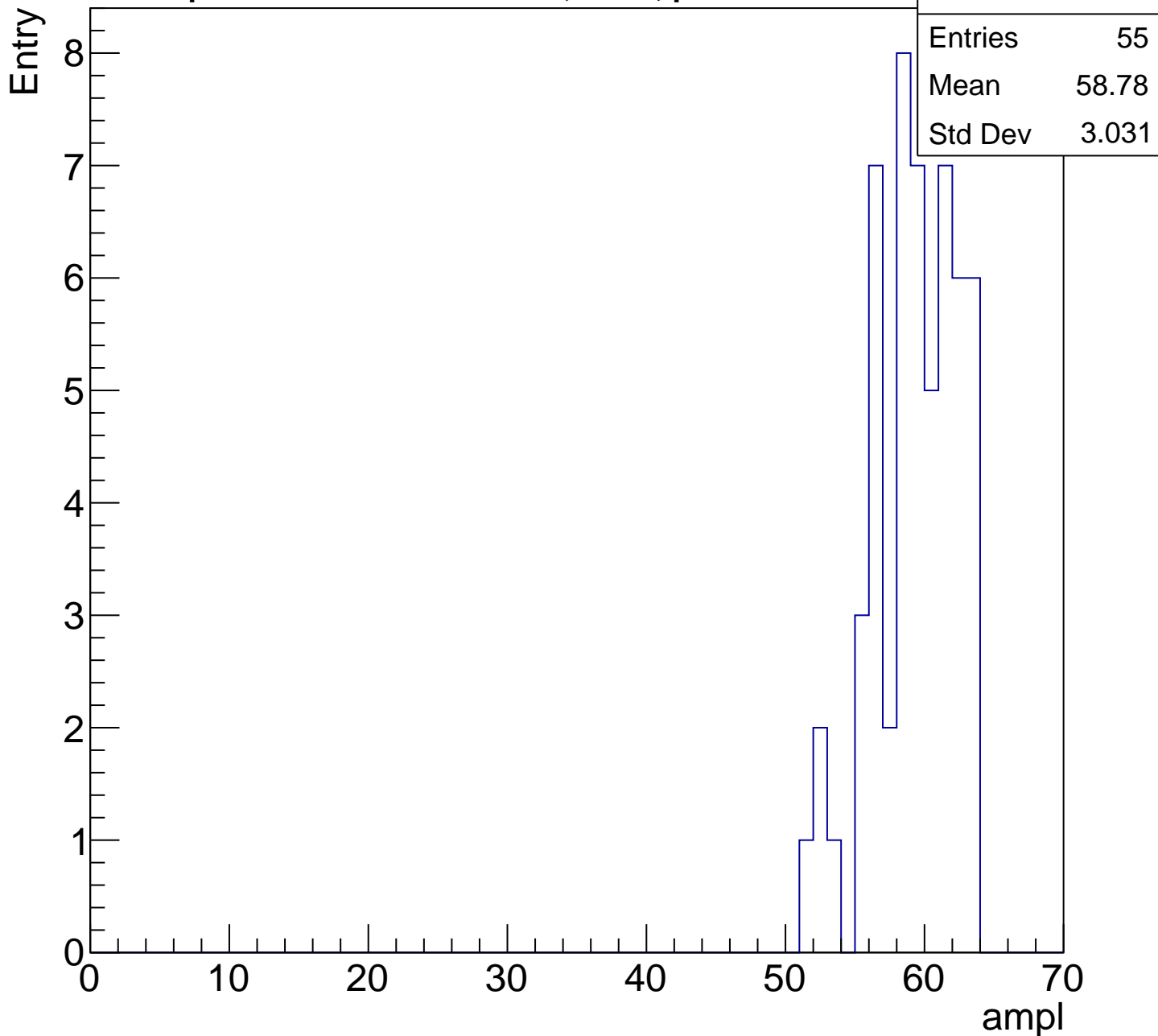
# B1L103S, U2-ch44, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U2-ch44, adc5

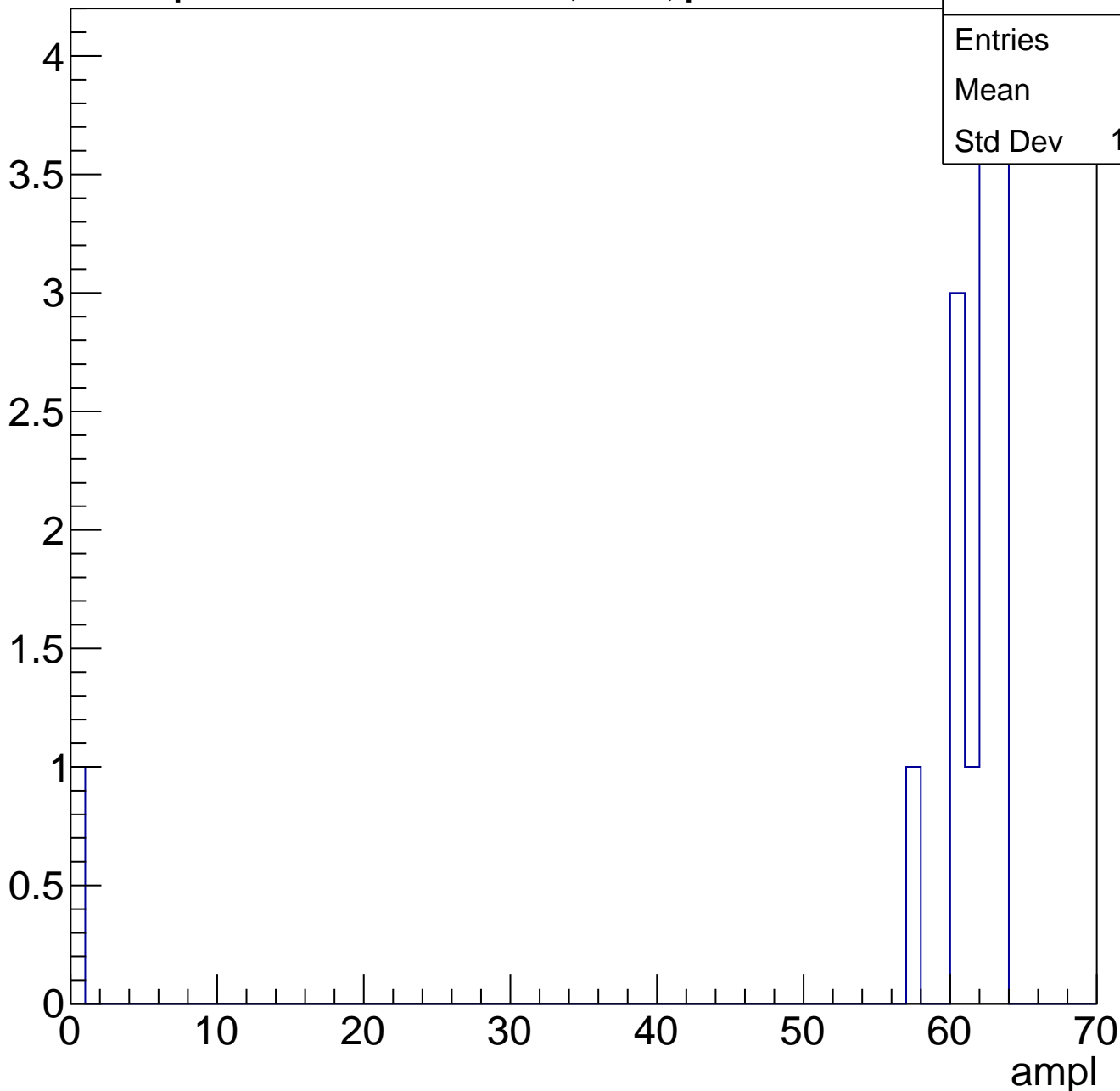
calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U2-ch44, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U2-ch44, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

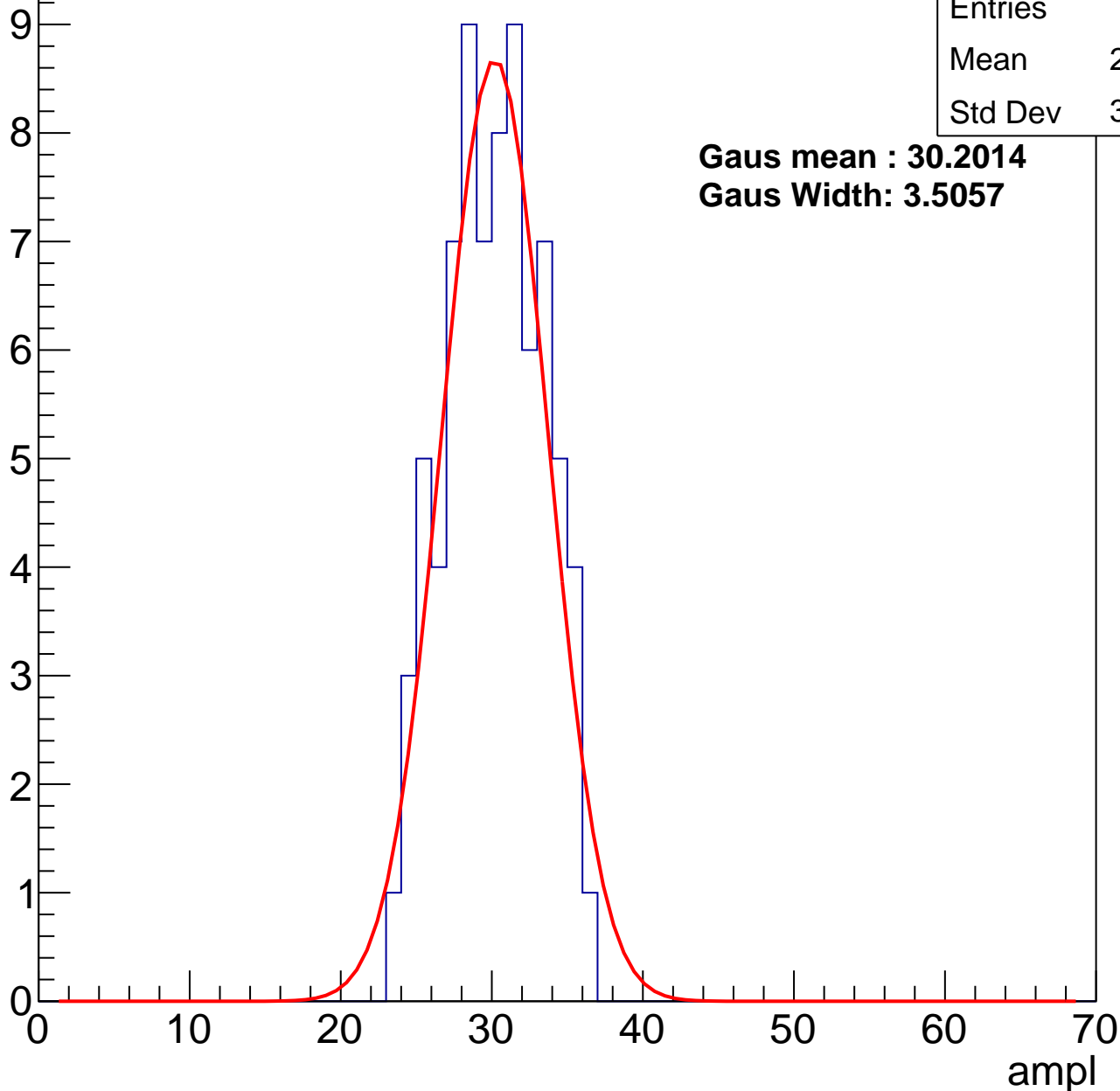
Entry



# B1L103S, U2-ch45, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch45, adc1

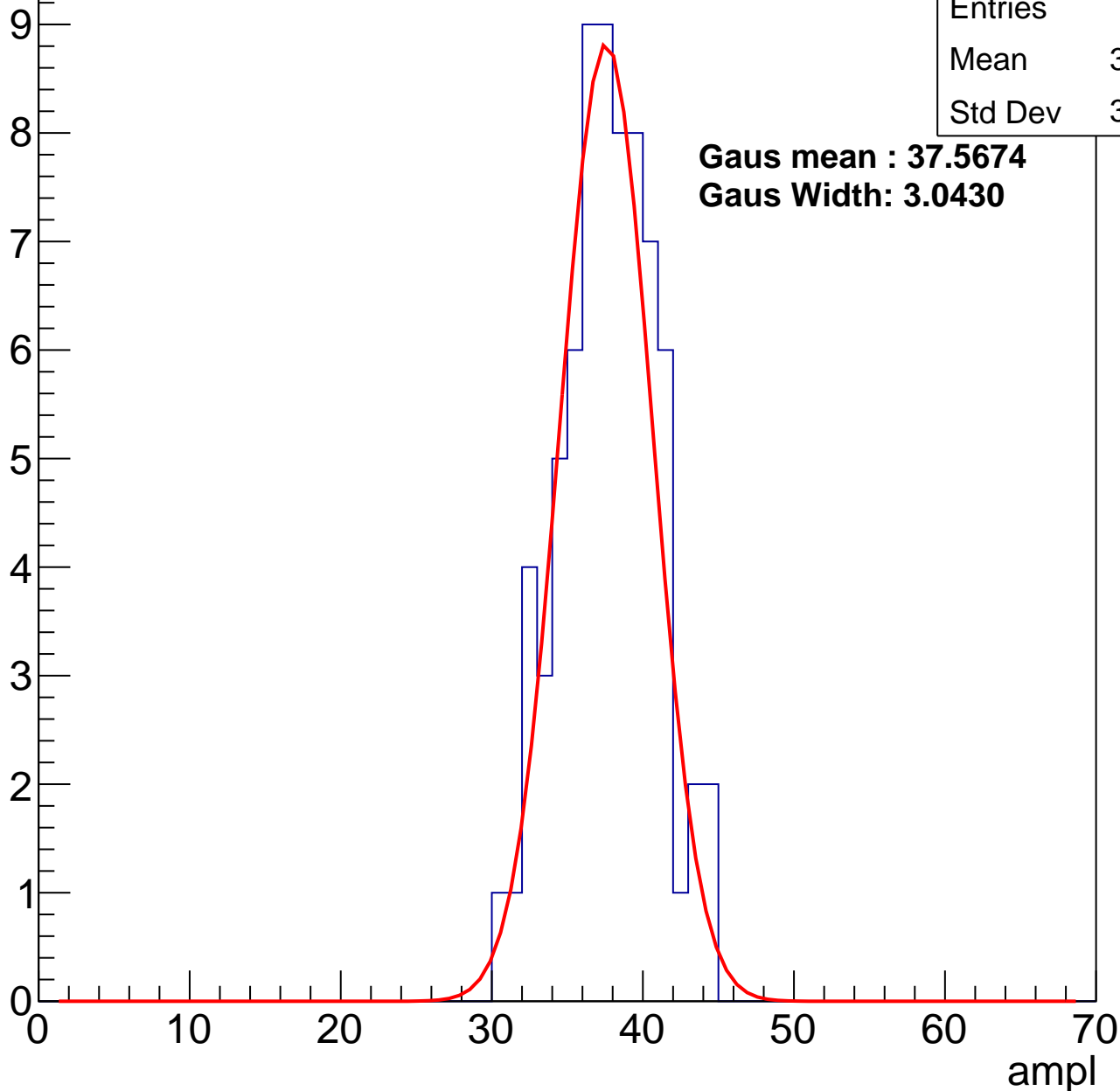
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	37.26
Std Dev	3.118

**Gaus mean : 37.5674**

**Gaus Width: 3.0430**



# B1L103S, U2-ch45, adc2

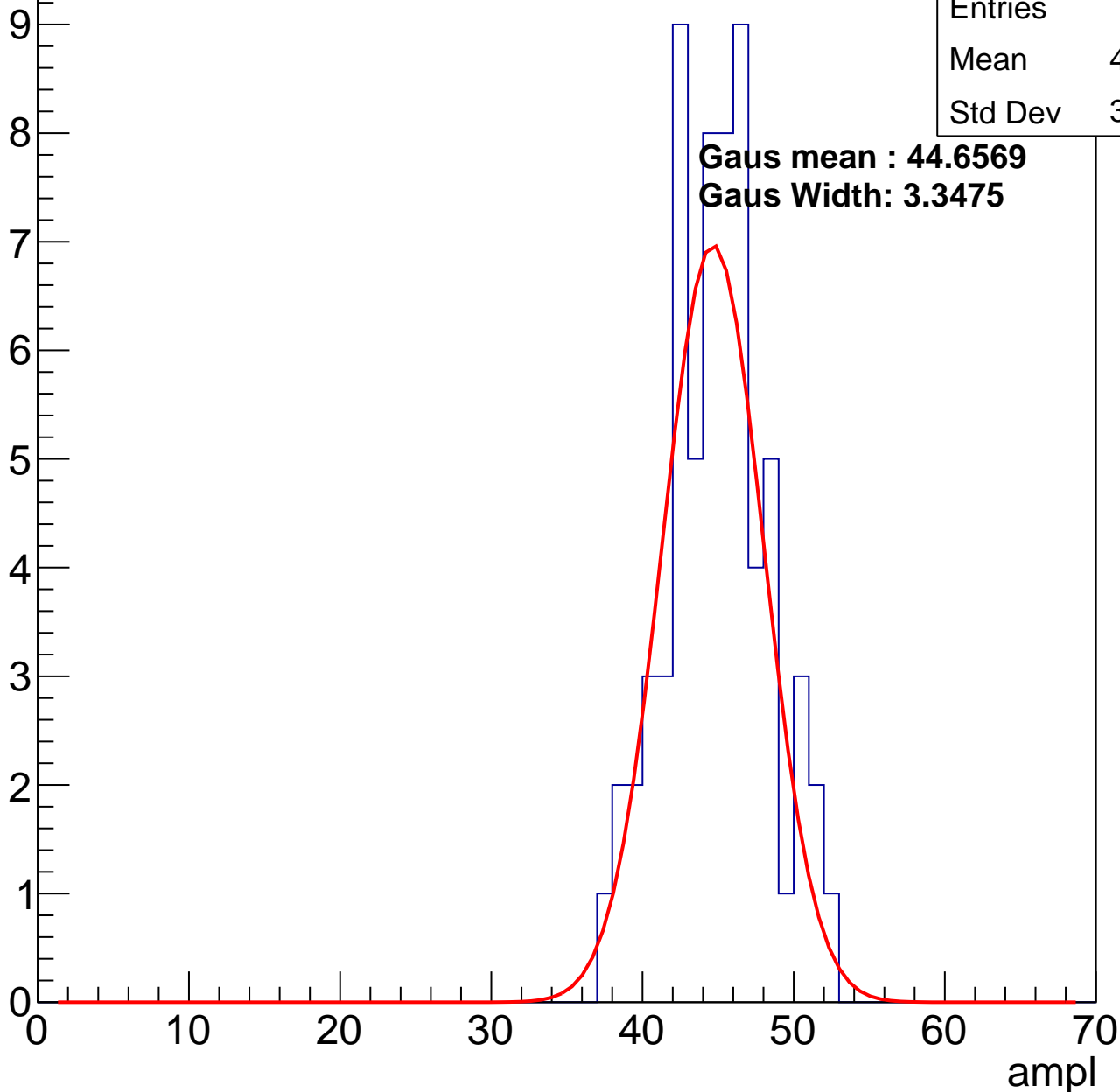
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	44.45
Std Dev	3.322

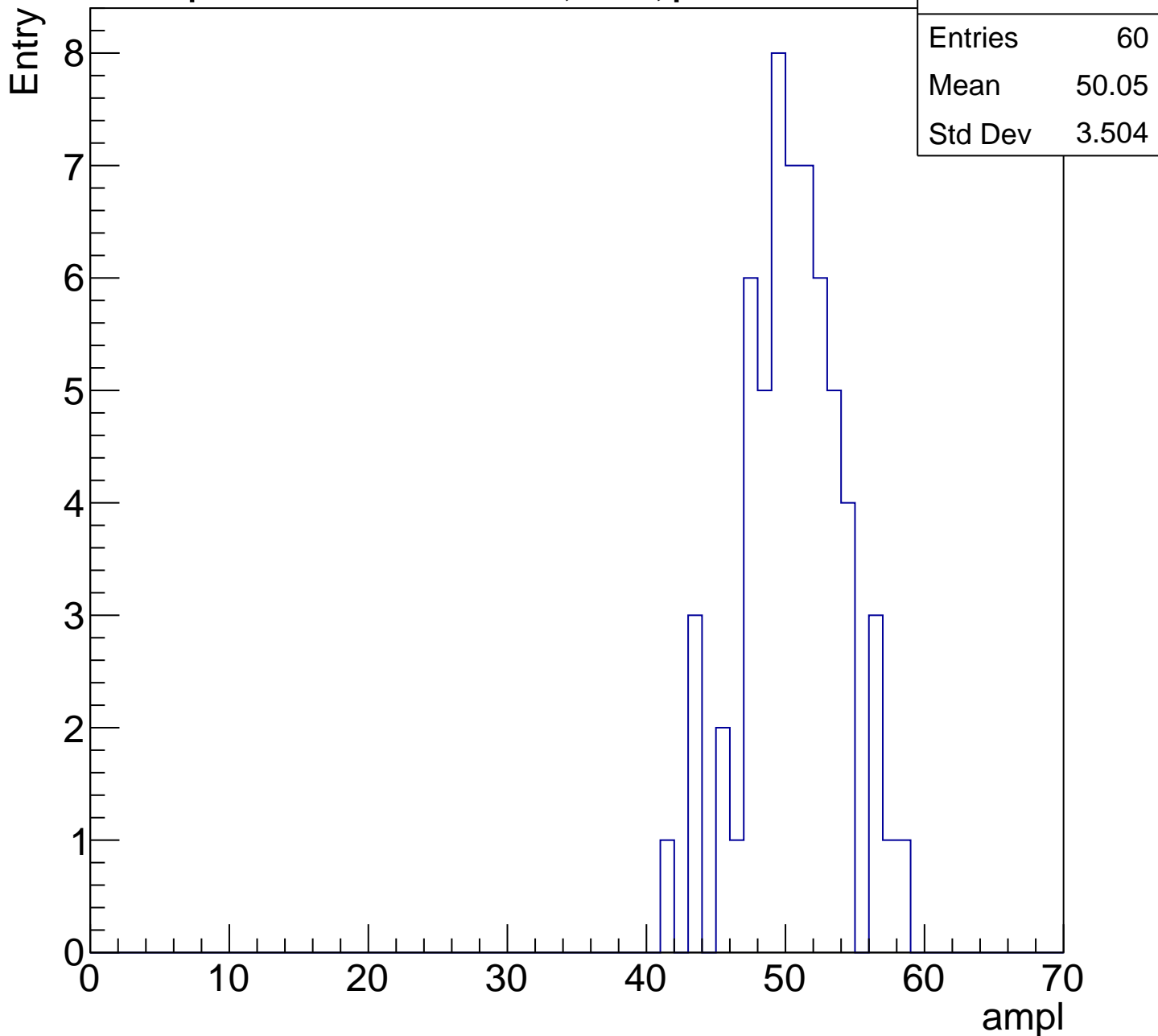
**Gaus mean : 44.6569**

**Gaus Width: 3.3475**



# B1L103S, U2-ch45, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

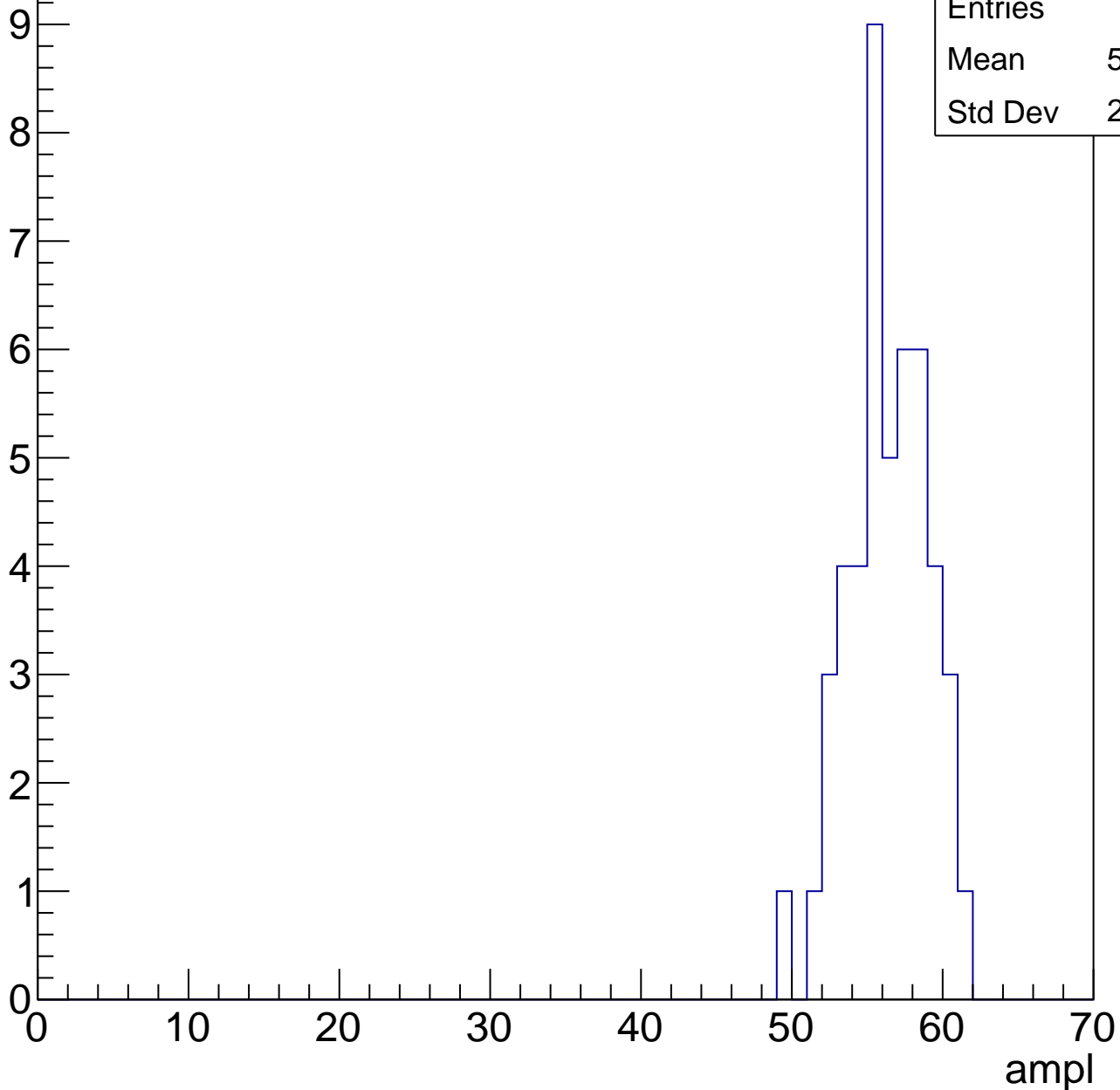


# B1L103S, U2-ch45, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	47
Mean	55.87
Std Dev	2.614

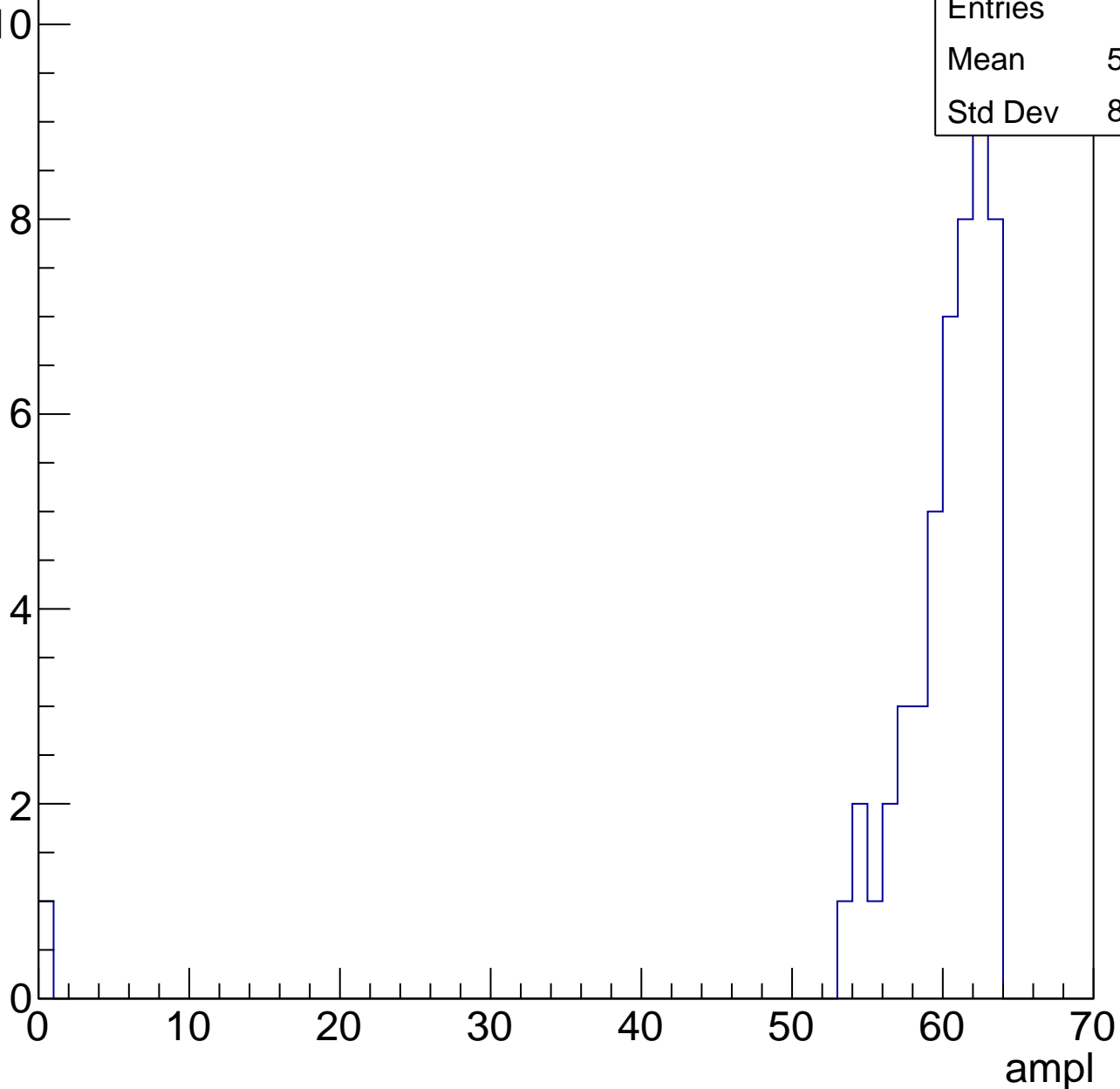


# B1L103S, U2-ch45, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

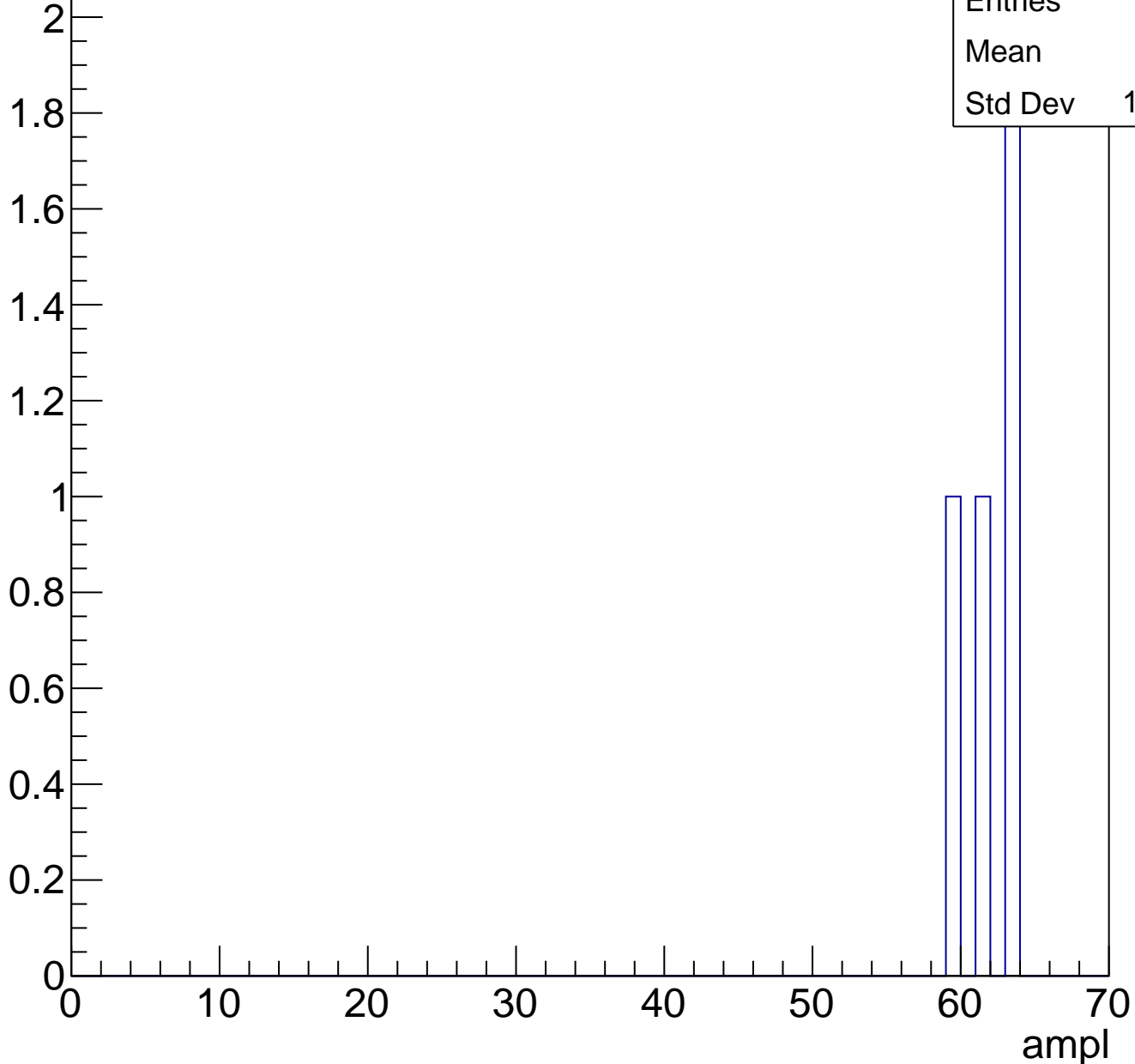
Entries	51
Mean	58.82
Std Dev	8.713



# B1L103S, U2-ch45, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U2-ch45, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch46, adc0

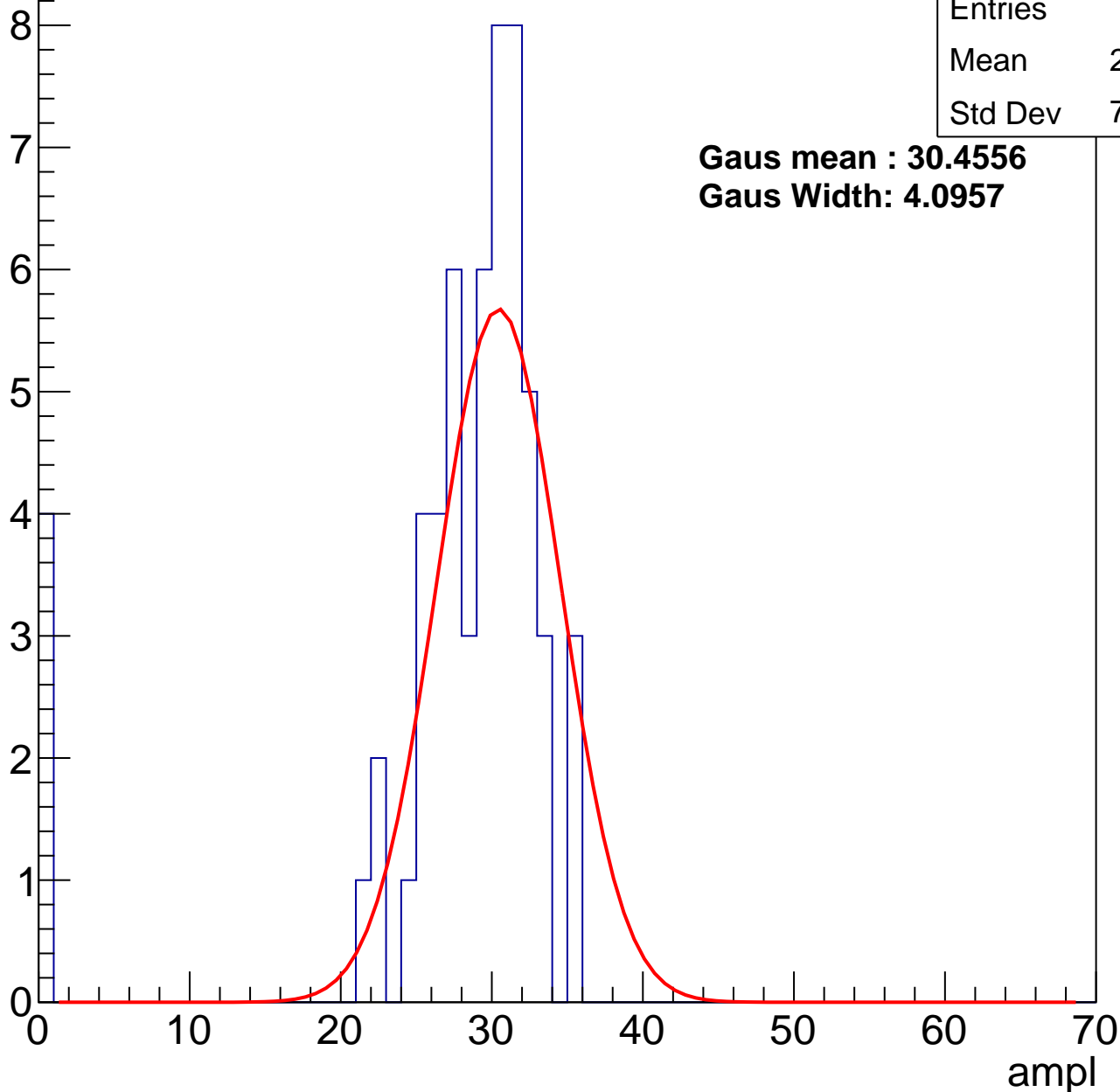
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	26.98
Std Dev	7.969

**Gaus mean : 30.4556**

**Gaus Width: 4.0957**



# B1L103S, U2-ch46, adc1

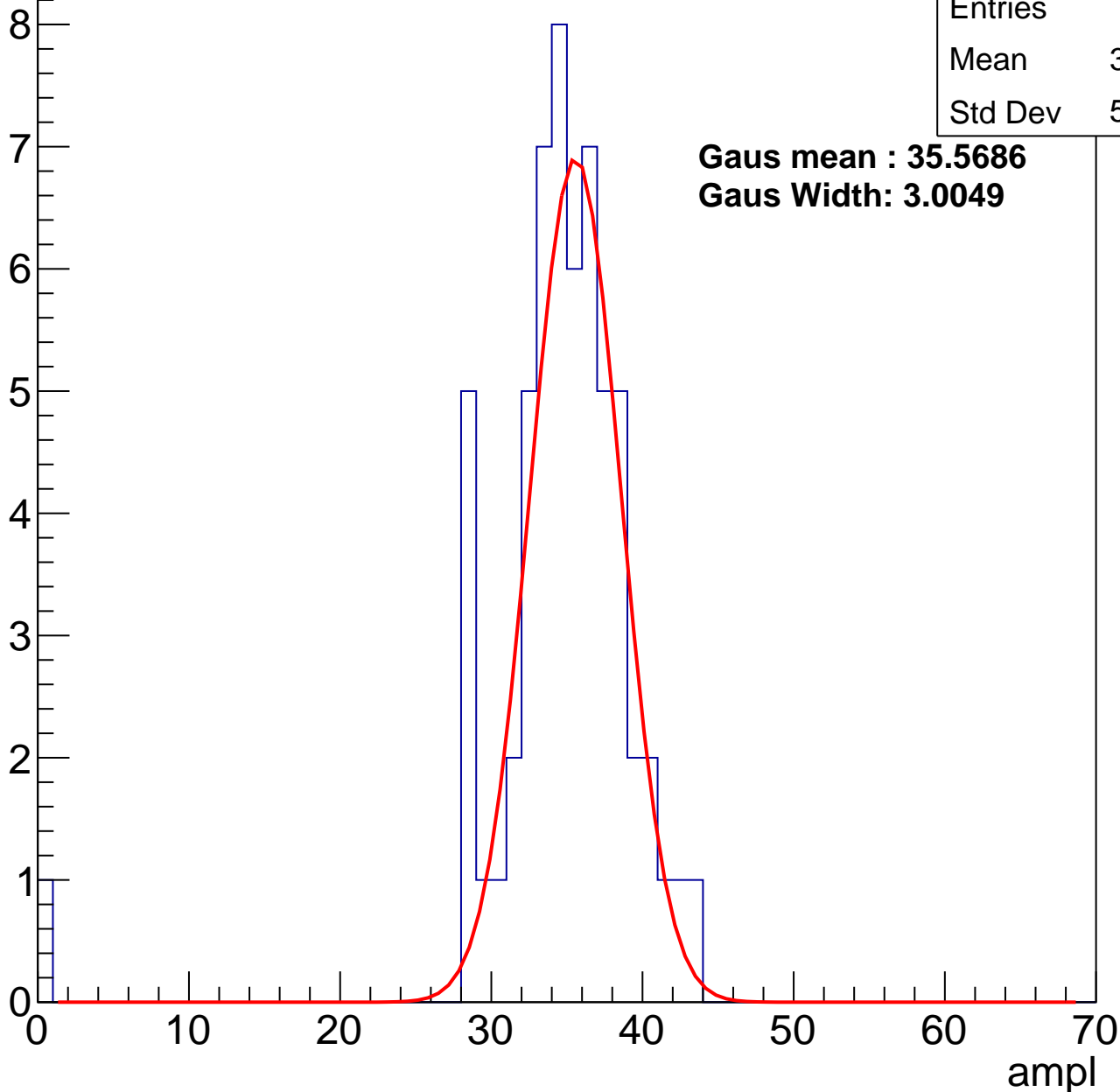
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	34.08
Std Dev	5.622

**Gaus mean : 35.5686**

**Gaus Width: 3.0049**



# B1L103S, U2-ch46, adc2

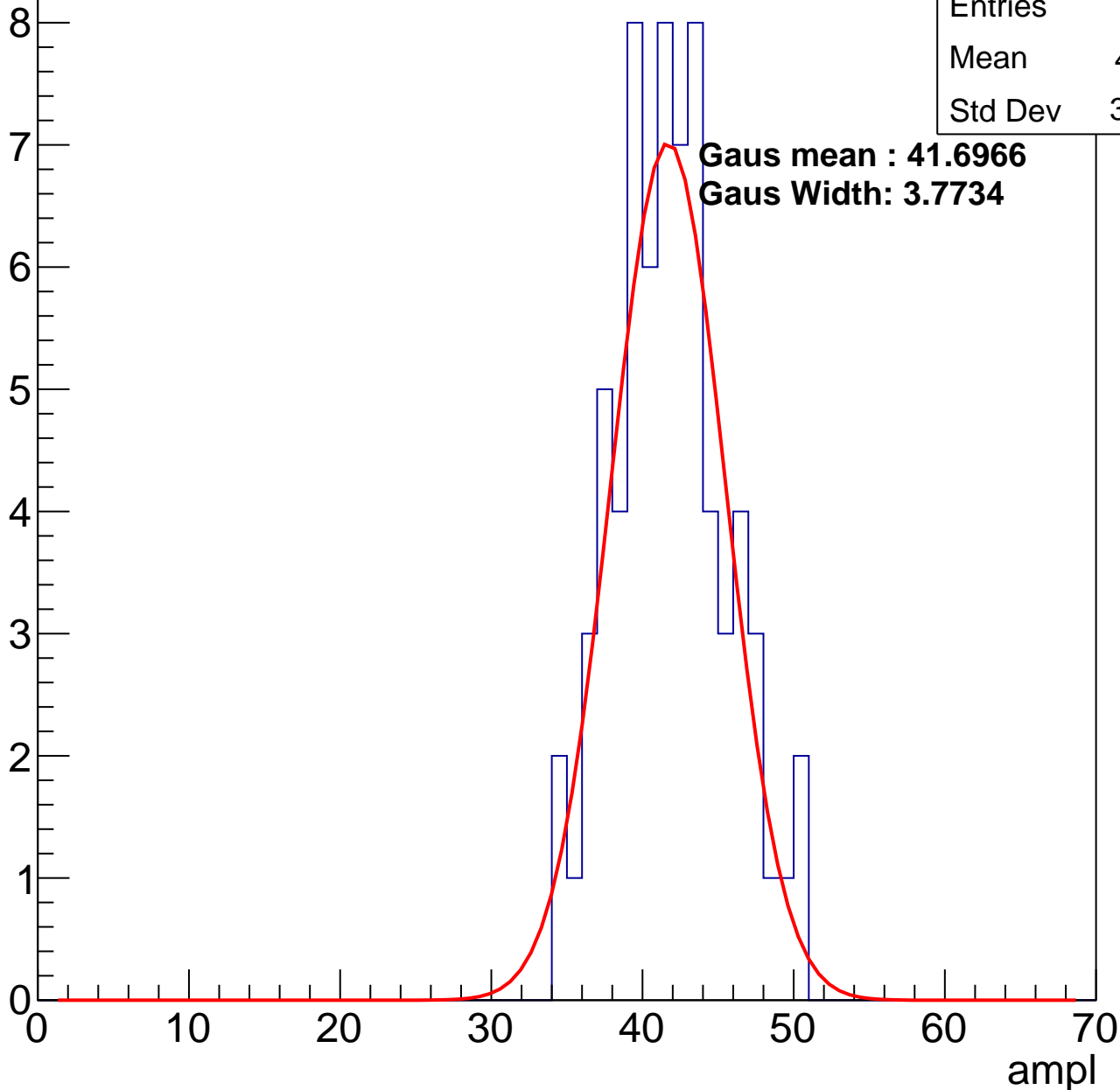
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	41.41
Std Dev	3.697

**Gaus mean : 41.6966**

**Gaus Width: 3.7734**

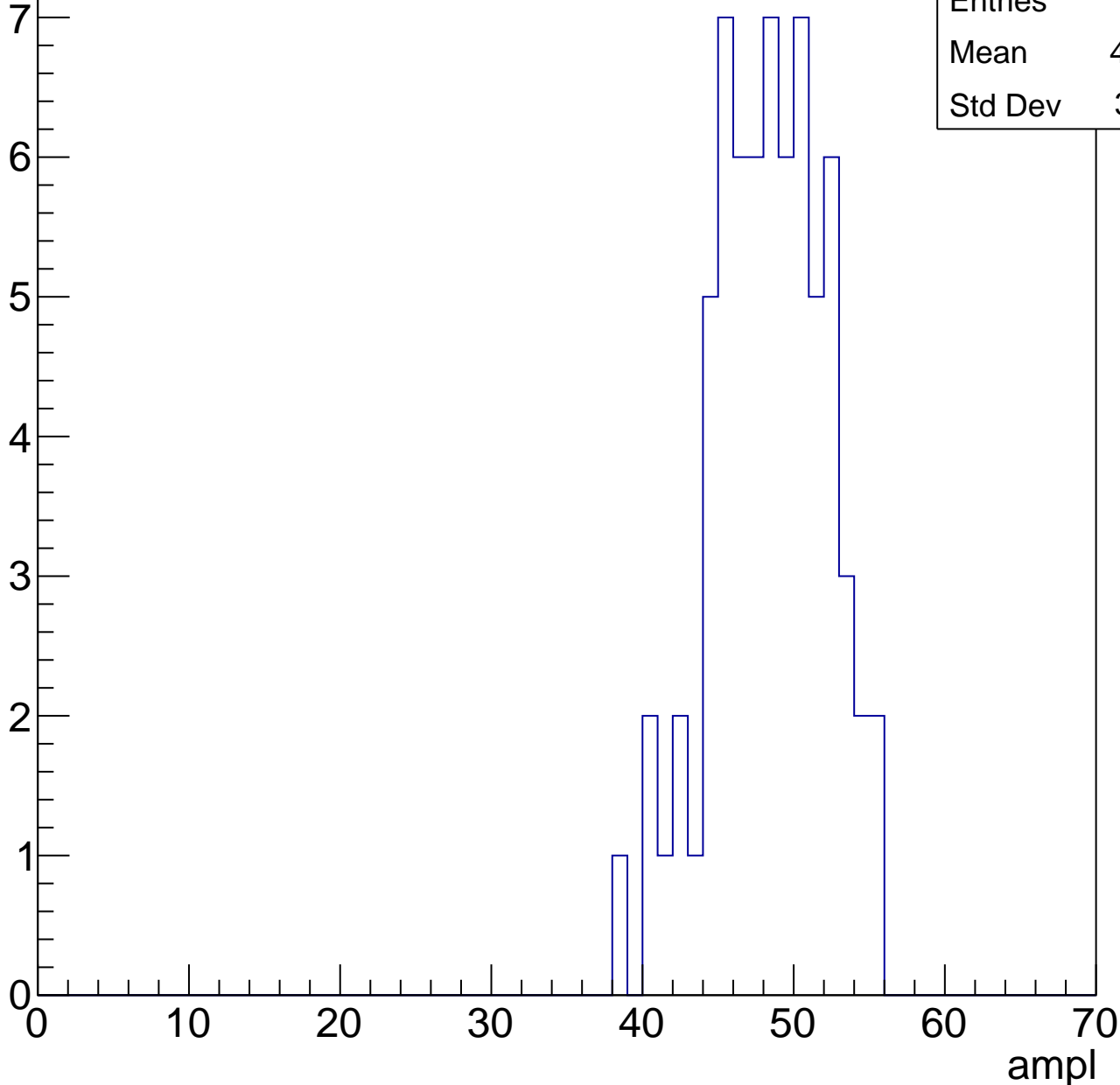


# B1L103S, U2-ch46, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

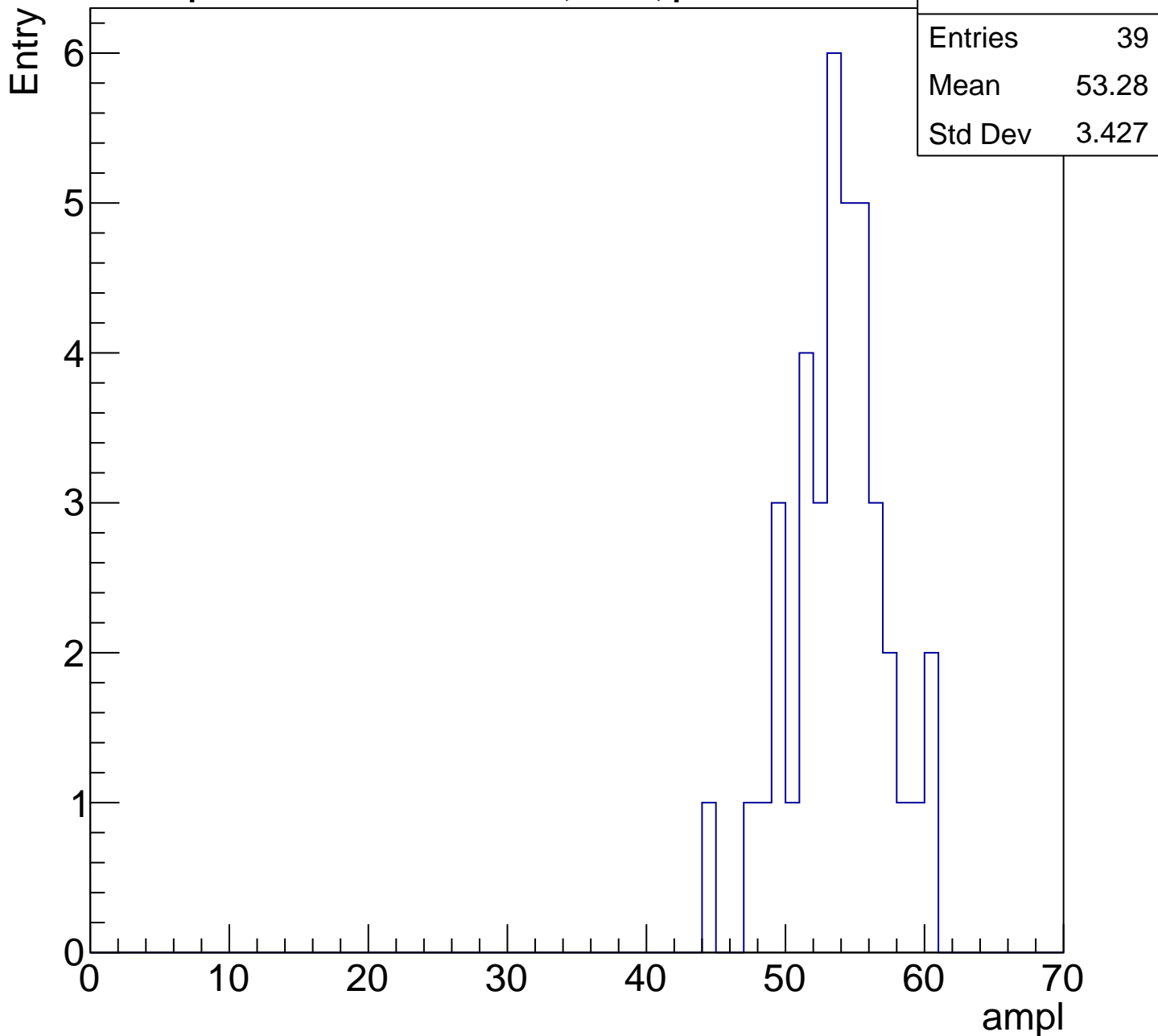
Entry

Entries	69
Mean	47.87
Std Dev	3.741



# B1L103S, U2-ch46, adc4

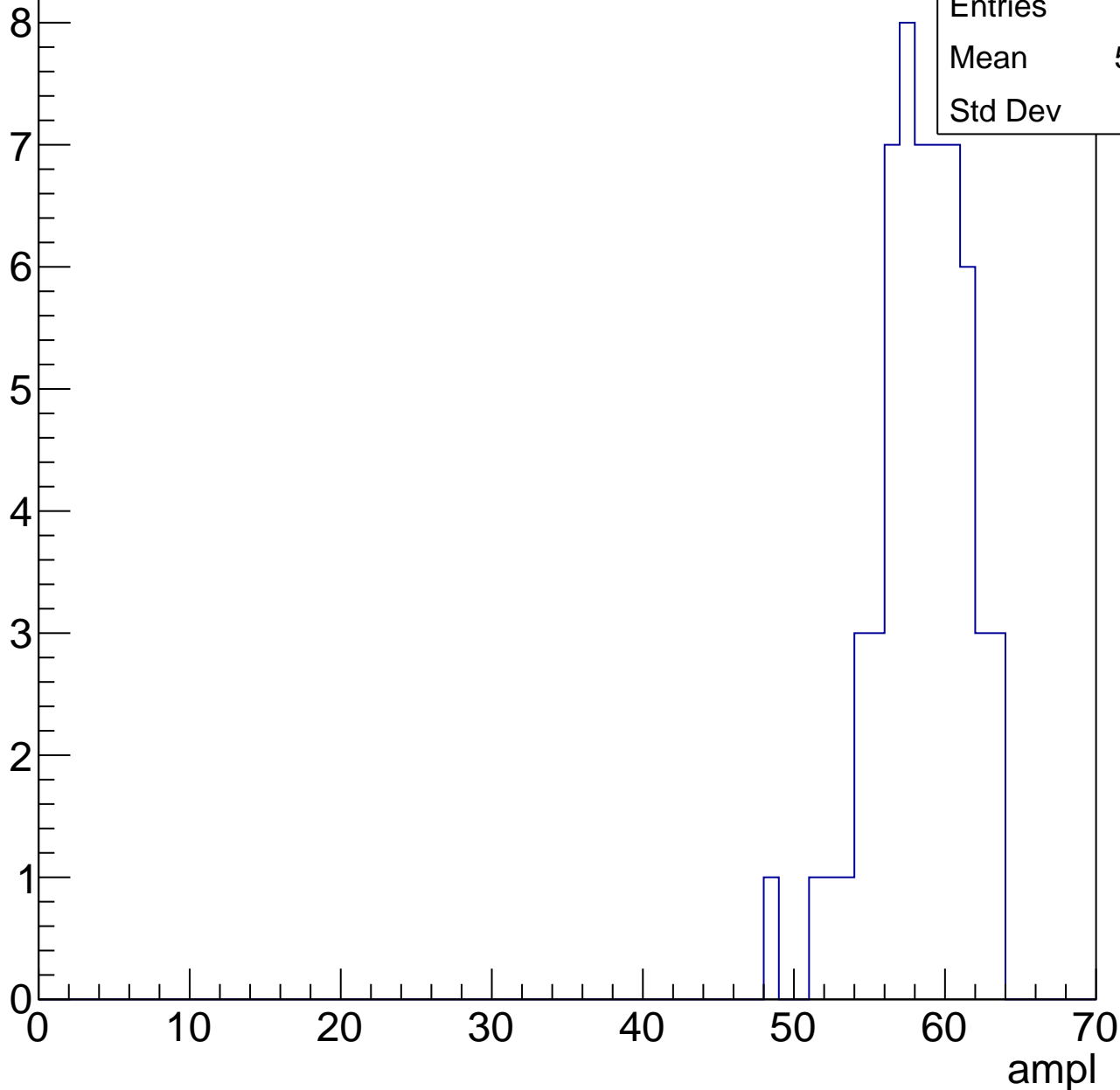
calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U2-ch46, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

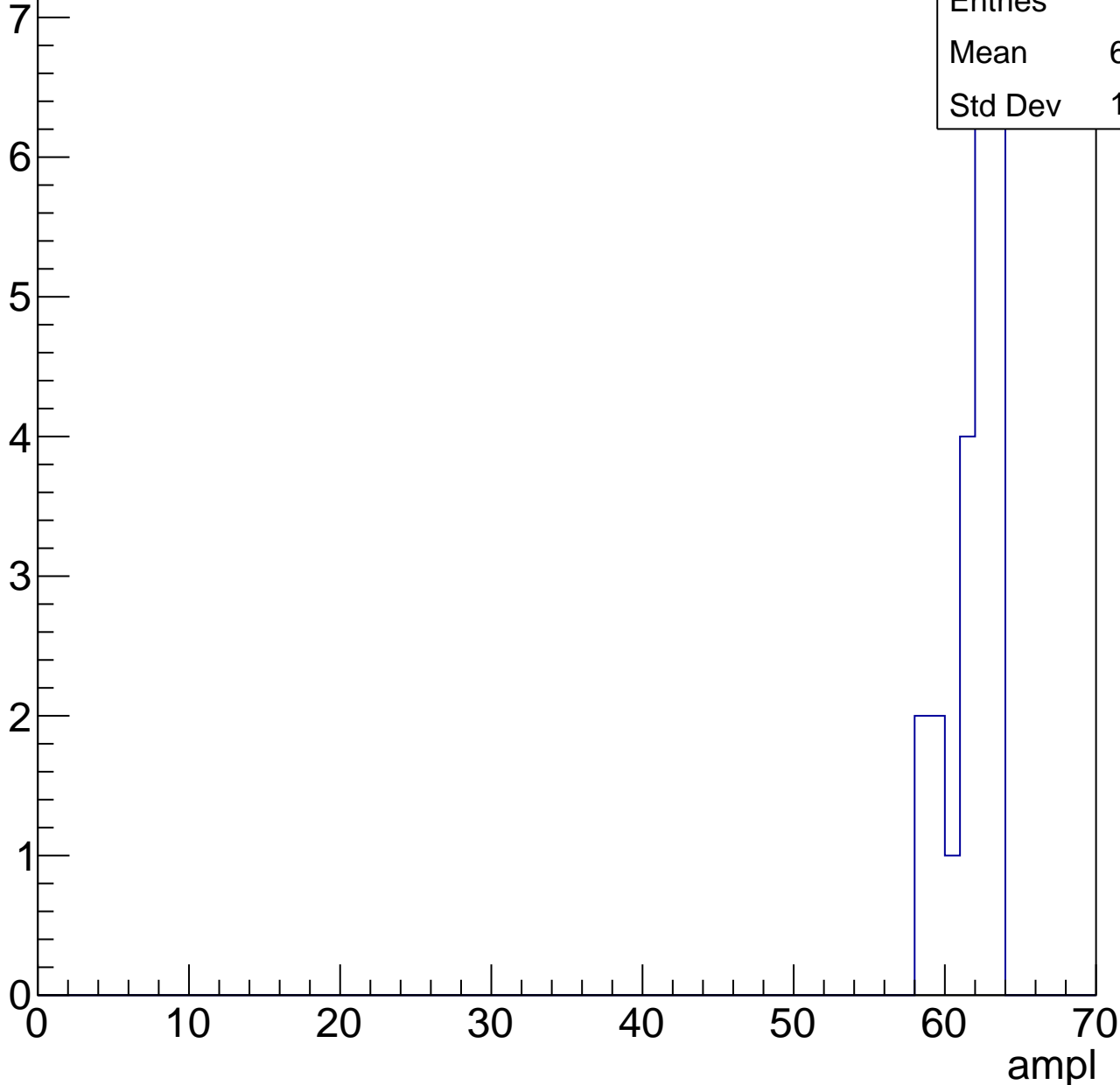


# B1L103S, U2-ch46, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	23
Mean	61.43
Std Dev	1.583





# B1L103S, U2-ch46, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch47, adc0

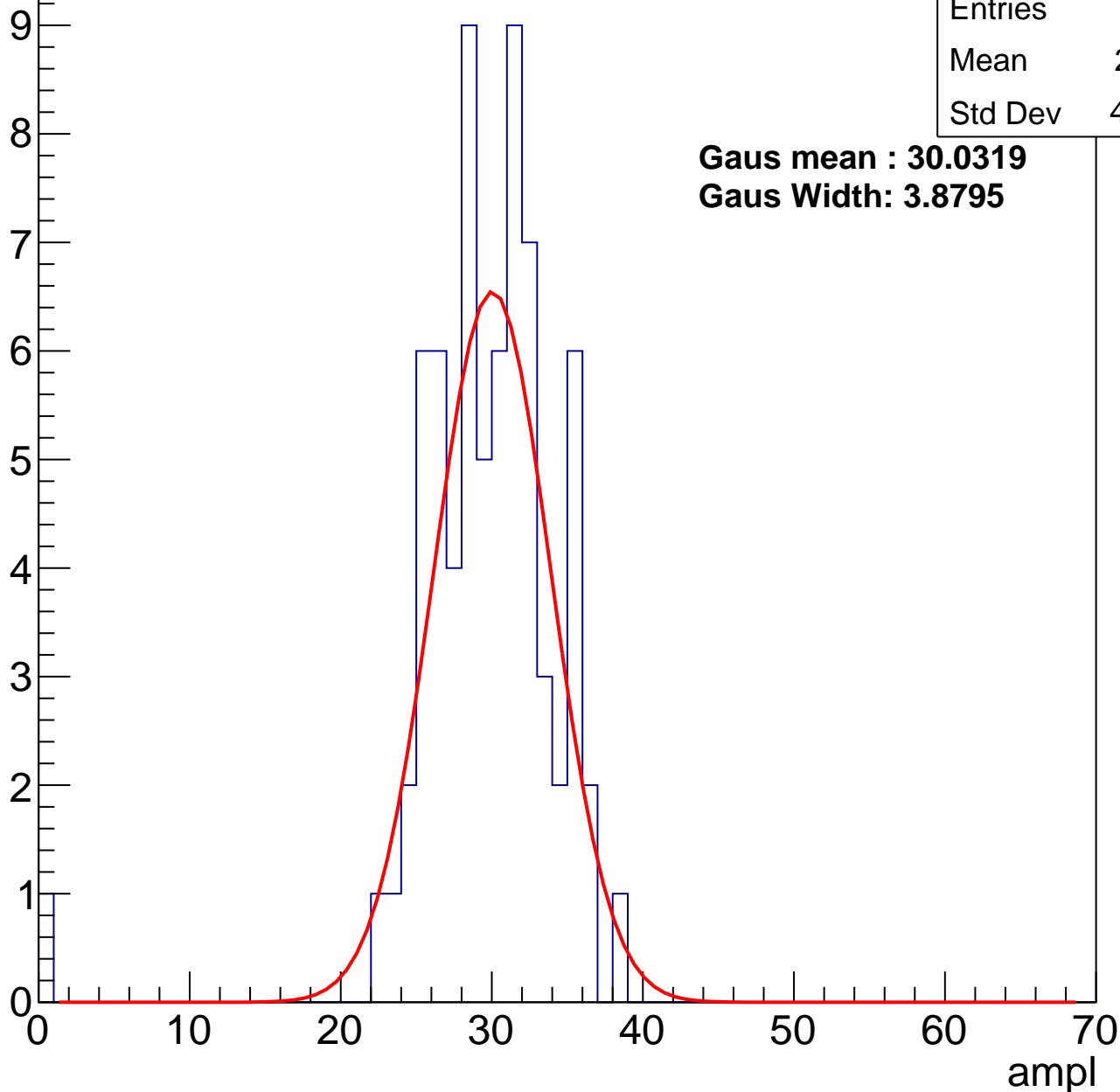
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	29.21
Std Dev	4.959

**Gaus mean : 30.0319**

**Gaus Width: 3.8795**



# B1L103S, U2-ch47, adc1

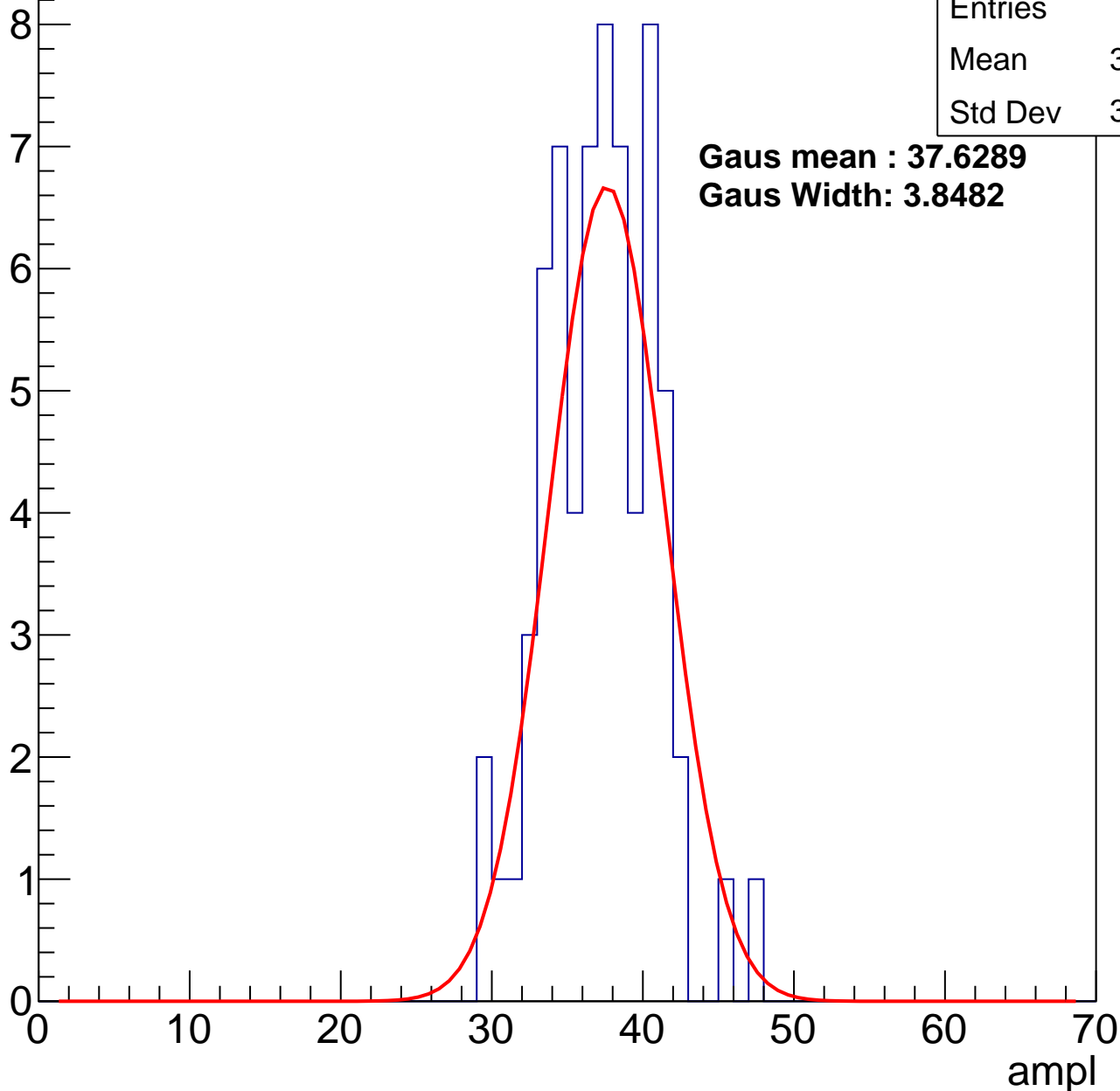
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	36.75
Std Dev	3.572

**Gaus mean : 37.6289**

**Gaus Width: 3.8482**



# B1L103S, U2-ch47, adc2

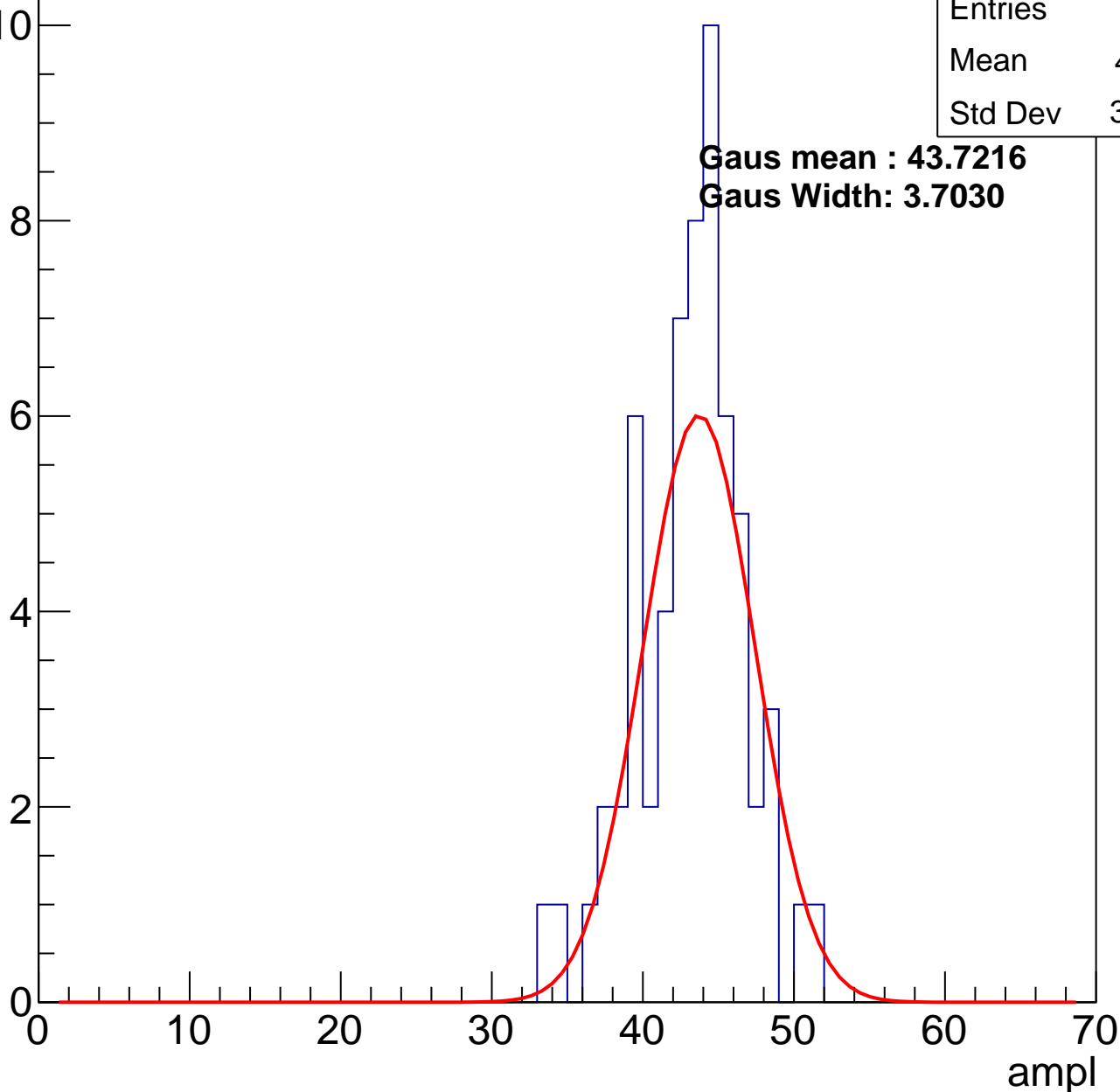
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	42.71
Std Dev	3.553

**Gaus mean : 43.7216**

**Gaus Width: 3.7030**

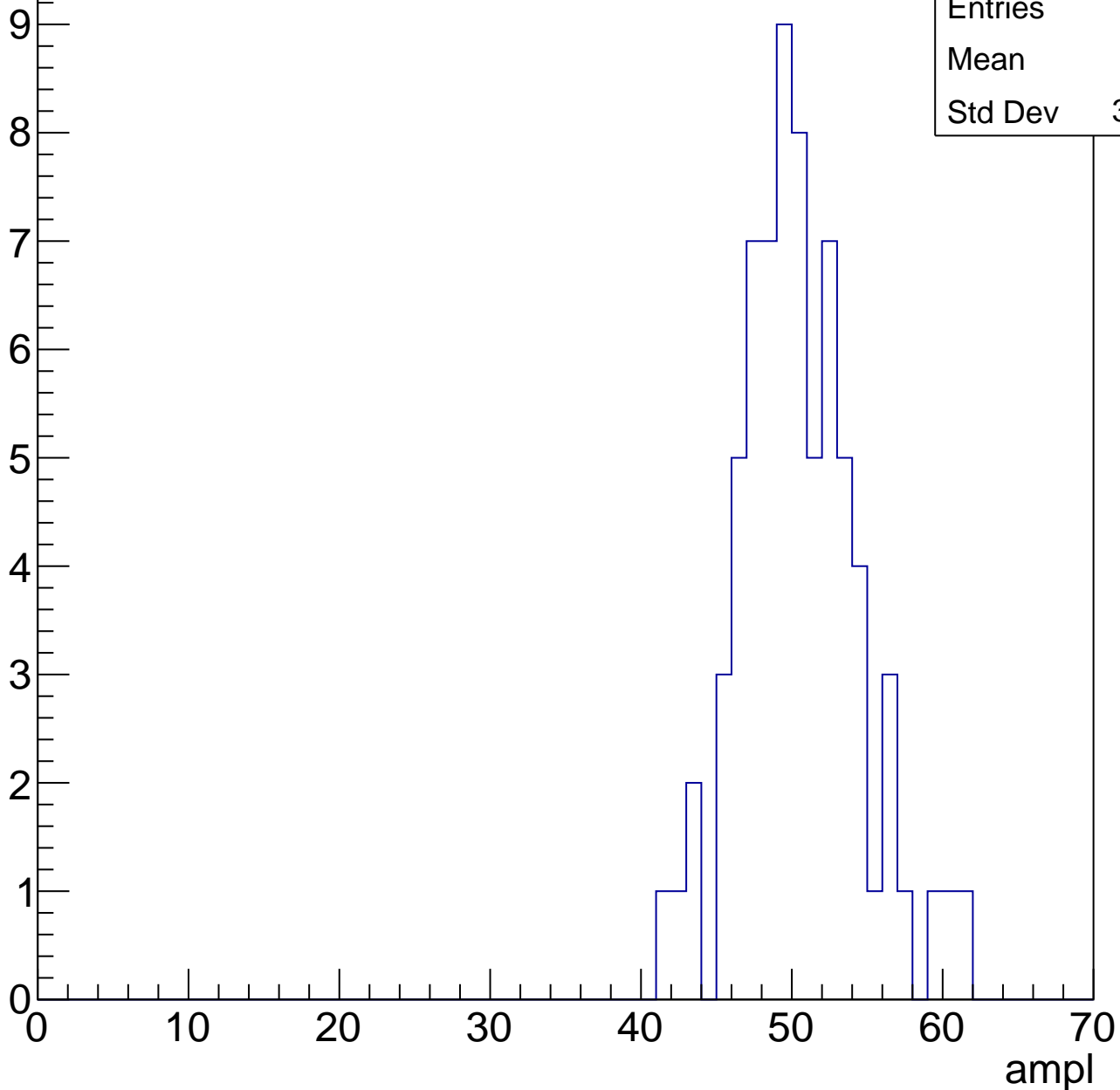


# B1L103S, U2-ch47, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

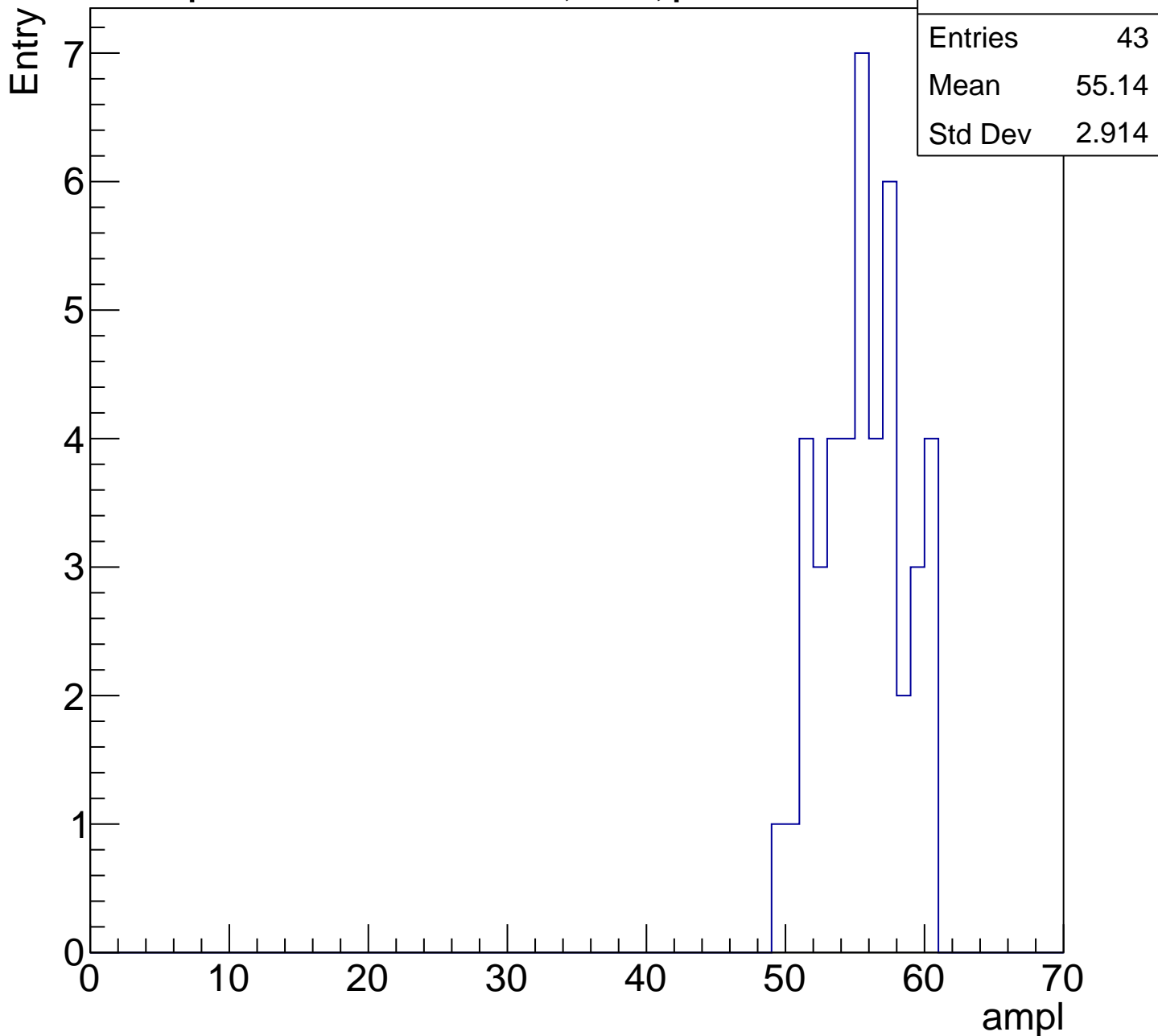
Entry

Entries	72
Mean	50
Std Dev	3.951



# B1L103S, U2-ch47, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U2-ch47, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

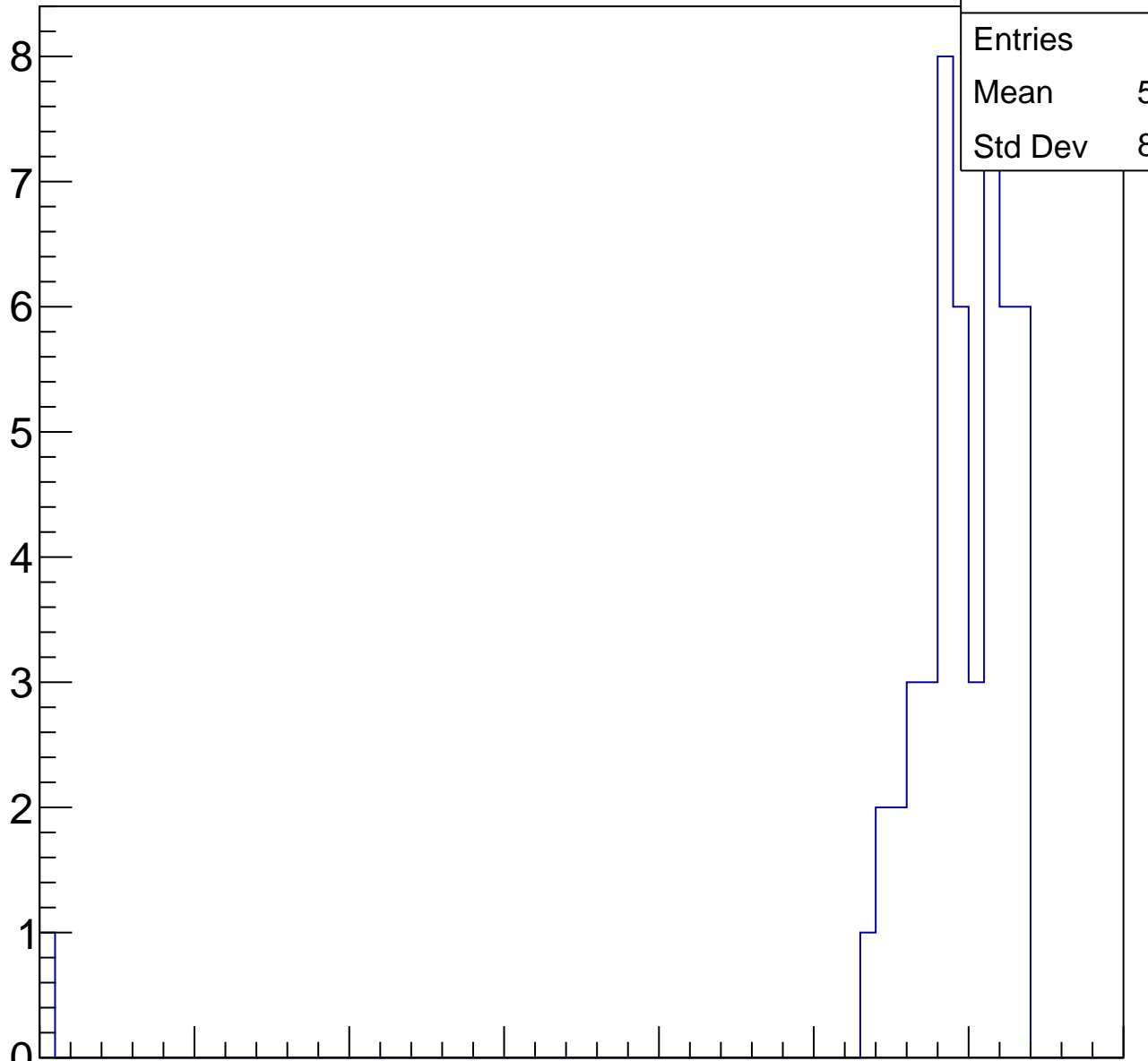
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	49
Mean	58.08
Std Dev	8.794

ampl

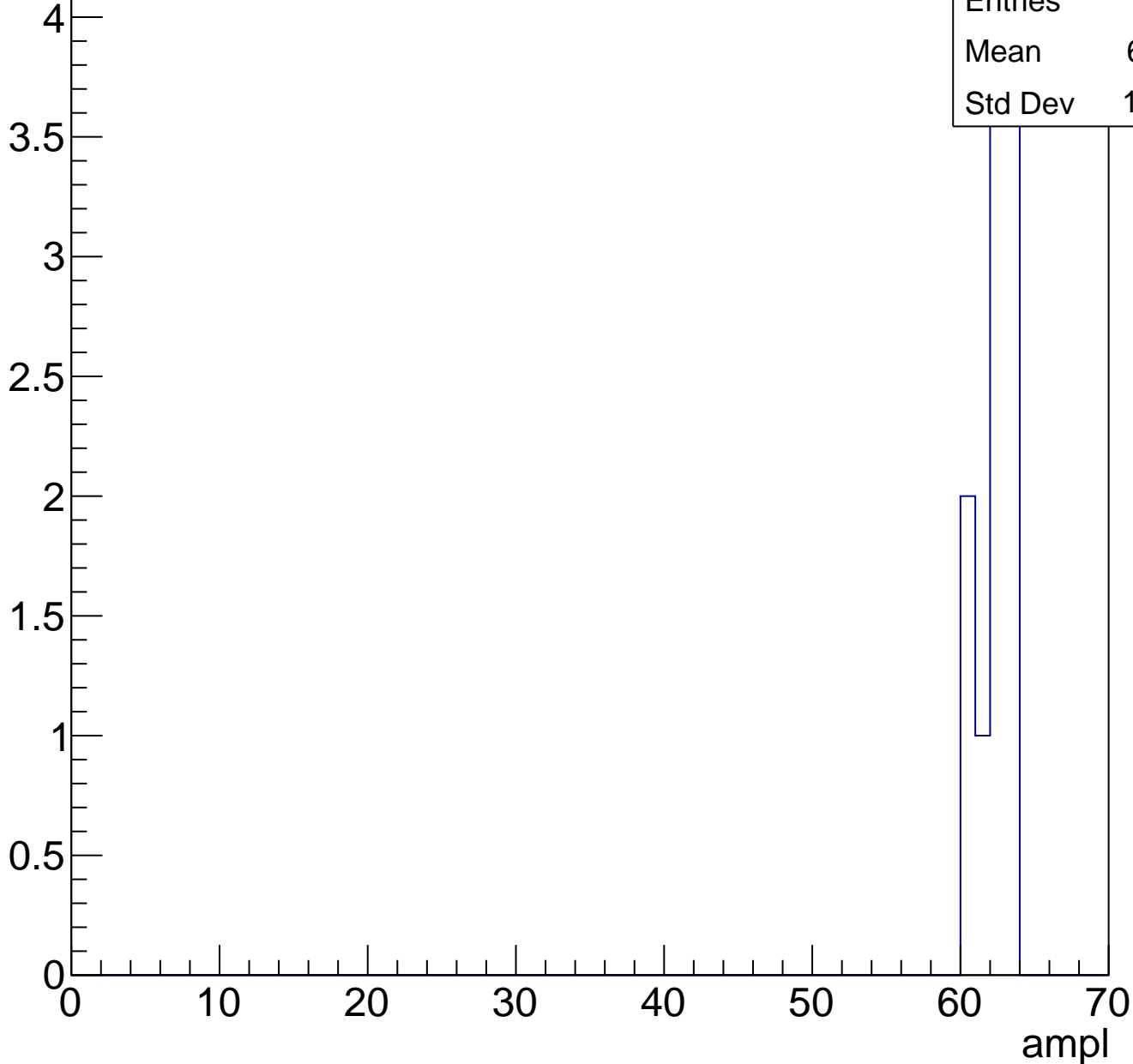
0 10 20 30 40 50 60 70



# B1L103S, U2-ch47, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U2-ch47, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	11
Std Dev	11

# B1L103S, U2-ch48, adc0

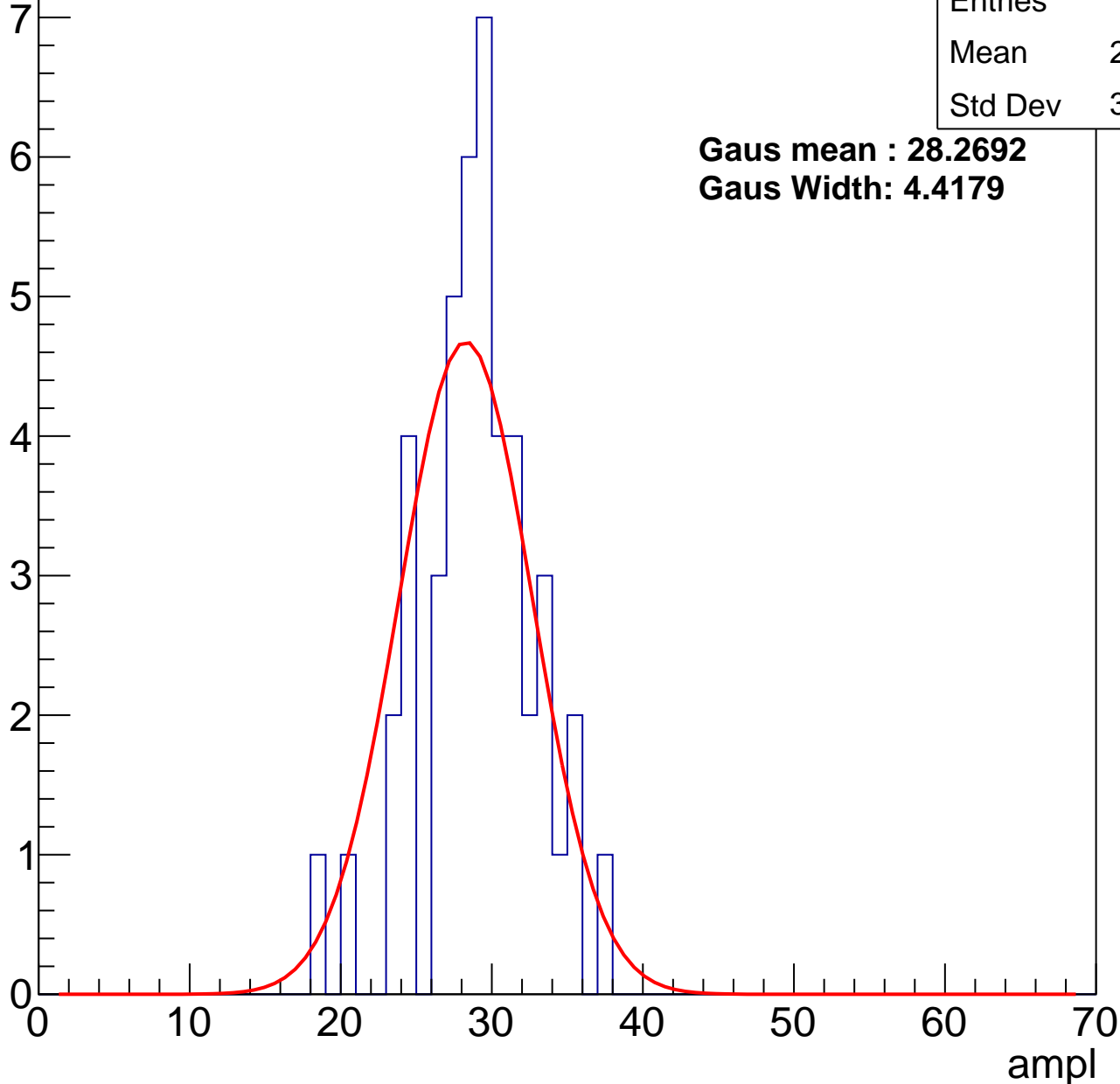
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	46
Mean	28.52
Std Dev	3.798

**Gaus mean : 28.2692**

**Gaus Width: 4.4179**



# B1L103S, U2-ch48, adc1

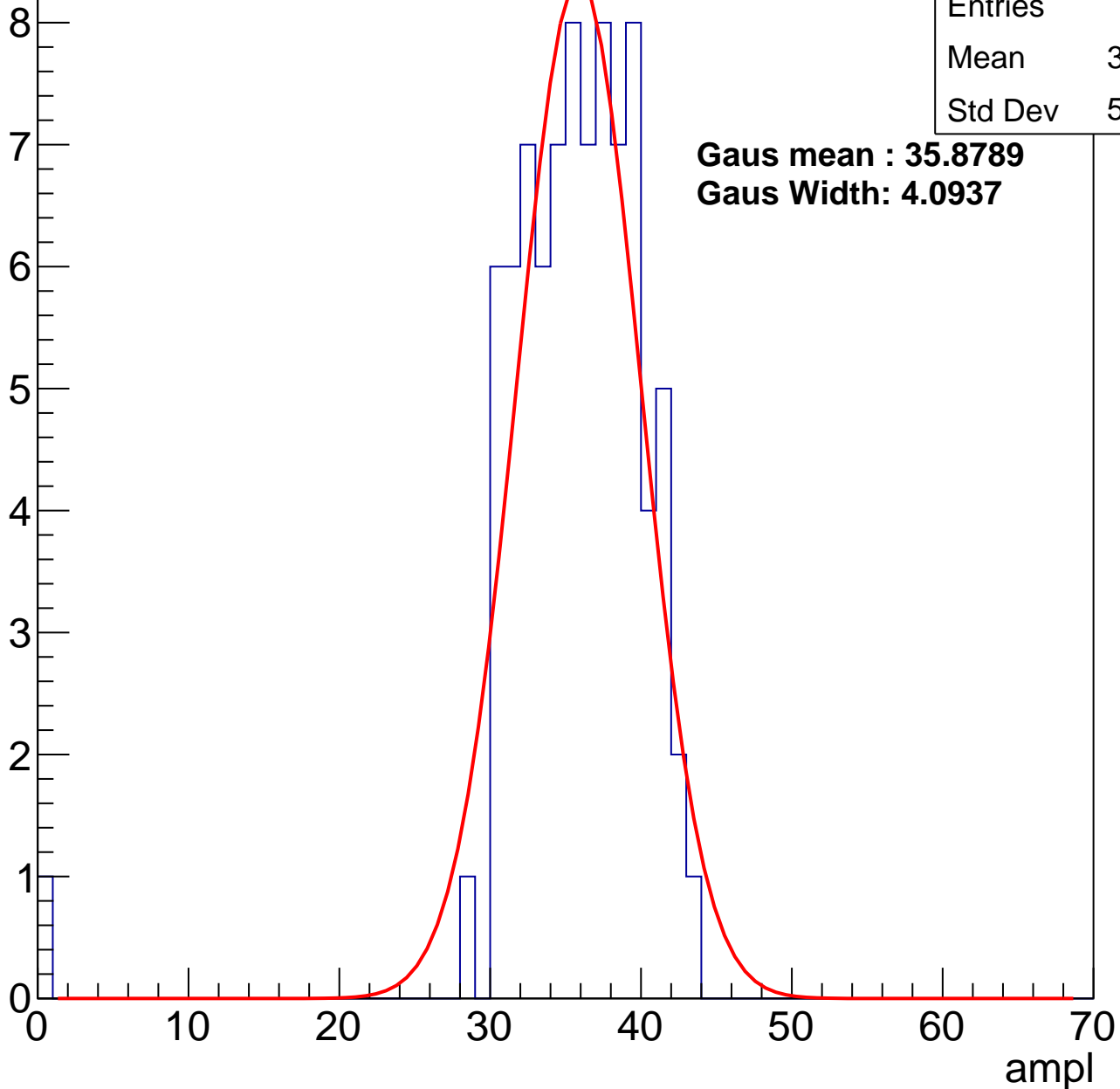
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	84
Mean	35.14
Std Dev	5.215

**Gaus mean : 35.8789**

**Gaus Width: 4.0937**



# B1L103S, U2-ch48, adc2

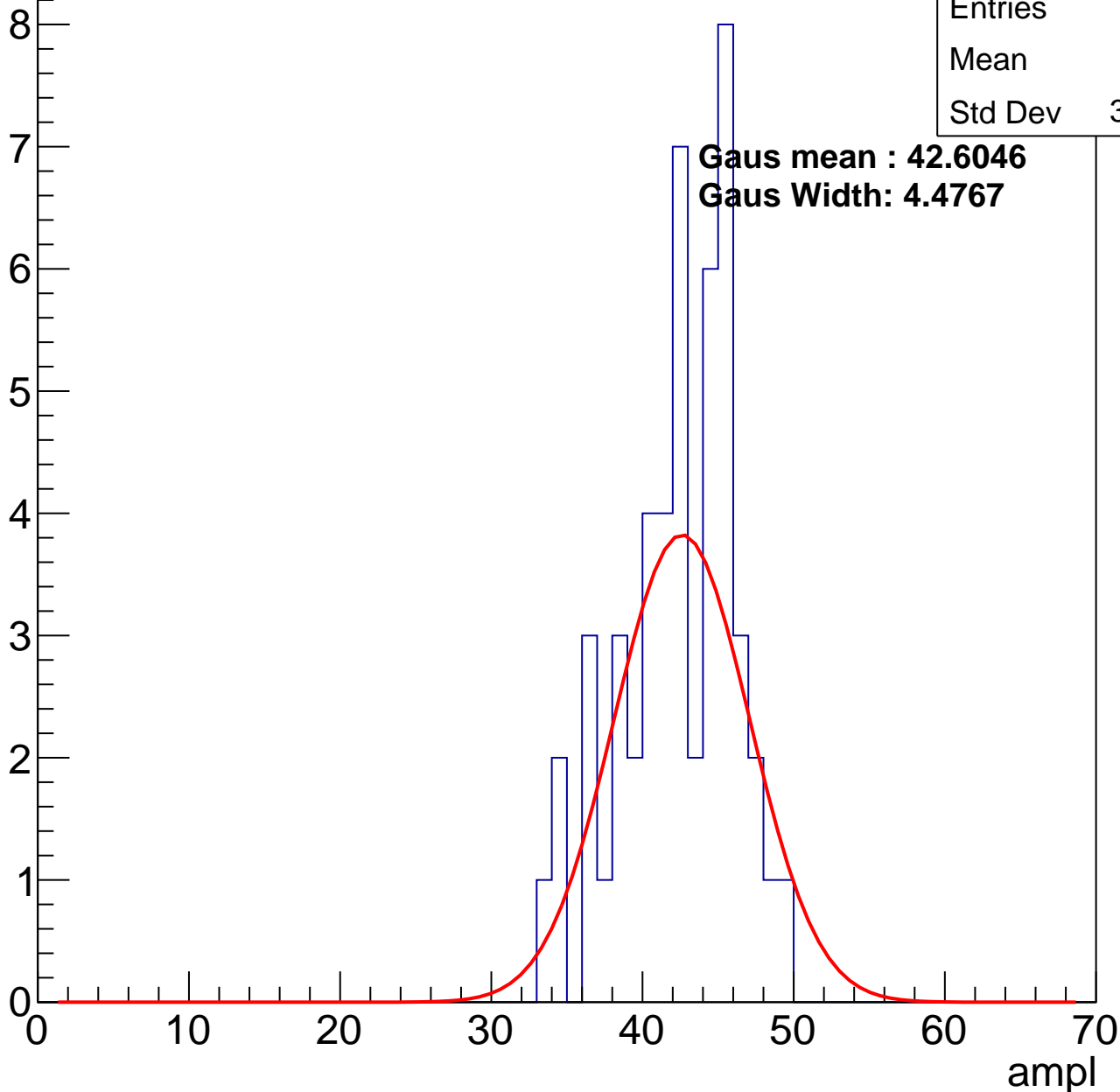
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	41.9
Std Dev	3.764

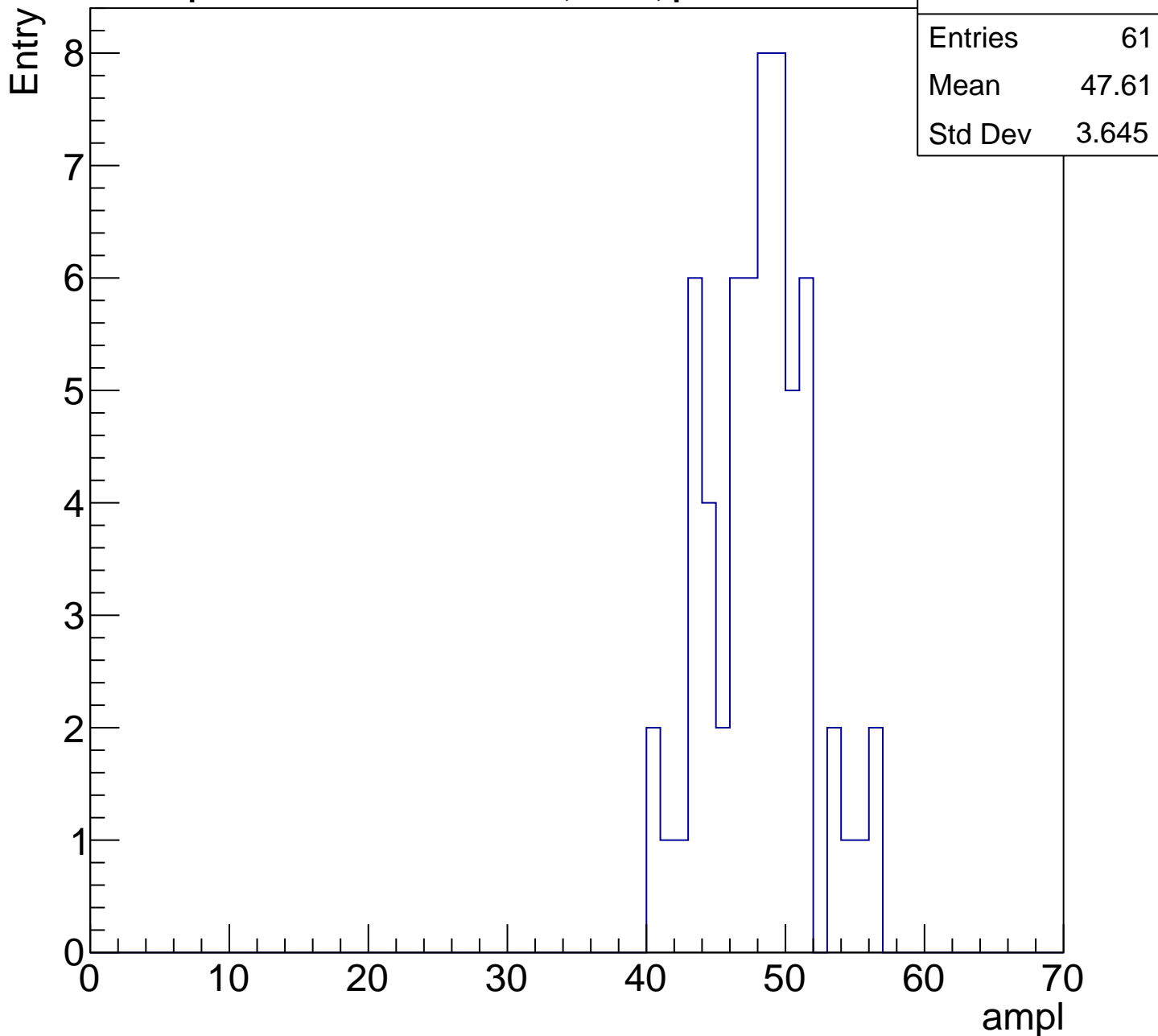
**Gaus mean : 42.6046**

**Gaus Width: 4.4767**



# B1L103S, U2-ch48, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

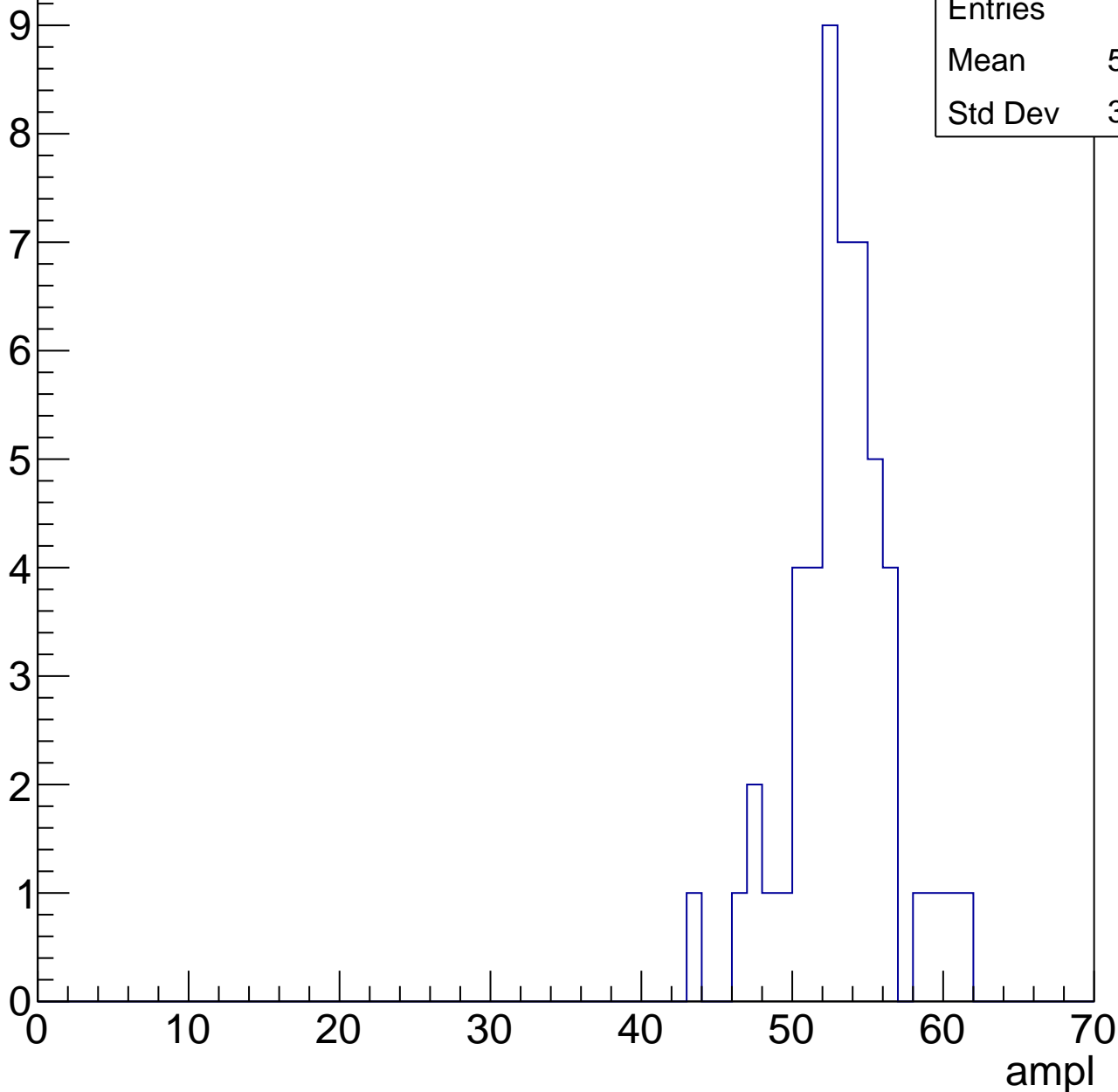


# B1L103S, U2-ch48, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	52.76
Std Dev	3.338



# B1L103S, U2-ch48, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	62
Mean	57.42
Std Dev	7.842

ampl

0

10

20

30

40

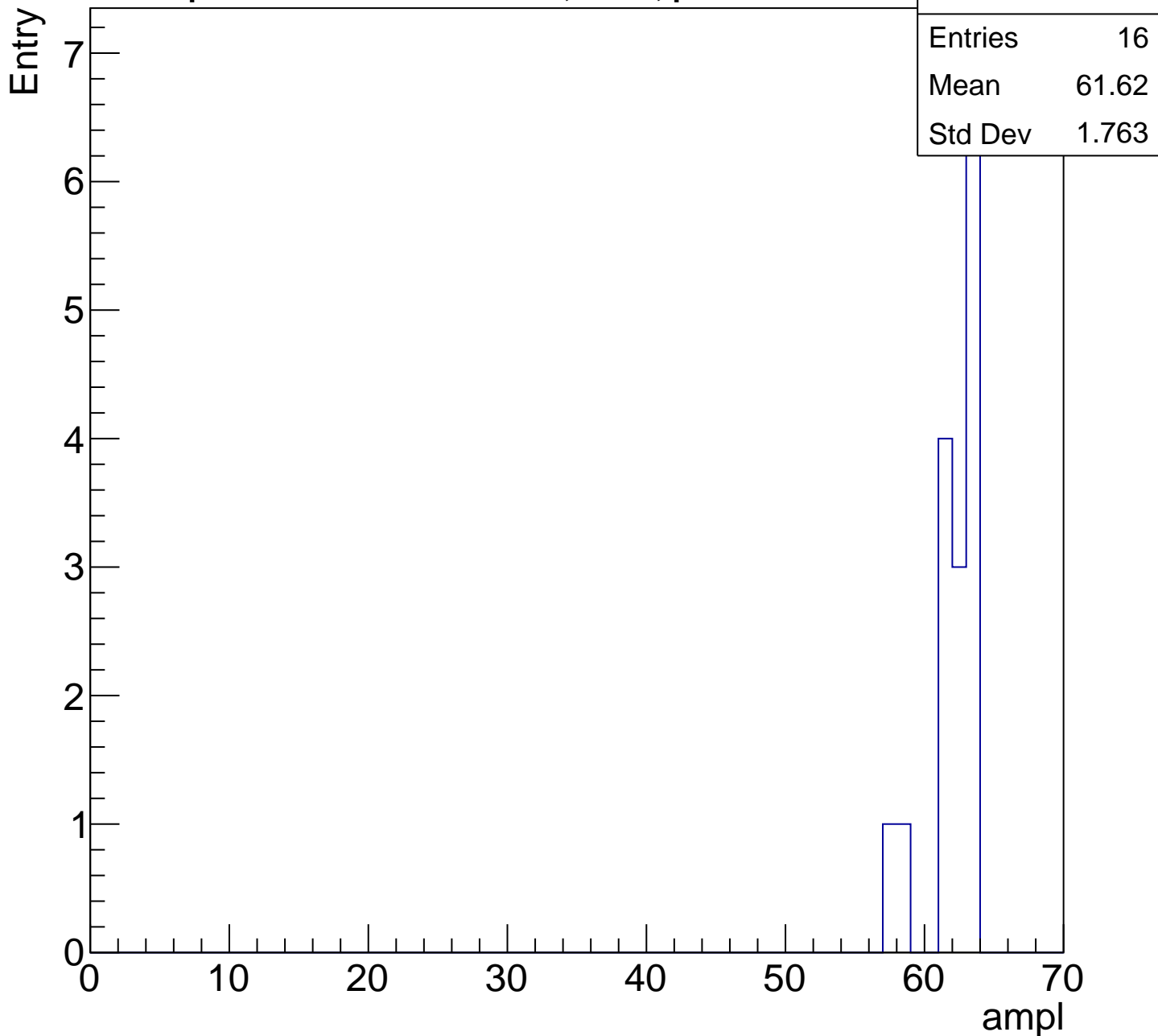
50

60

70

# B1L103S, U2-ch48, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

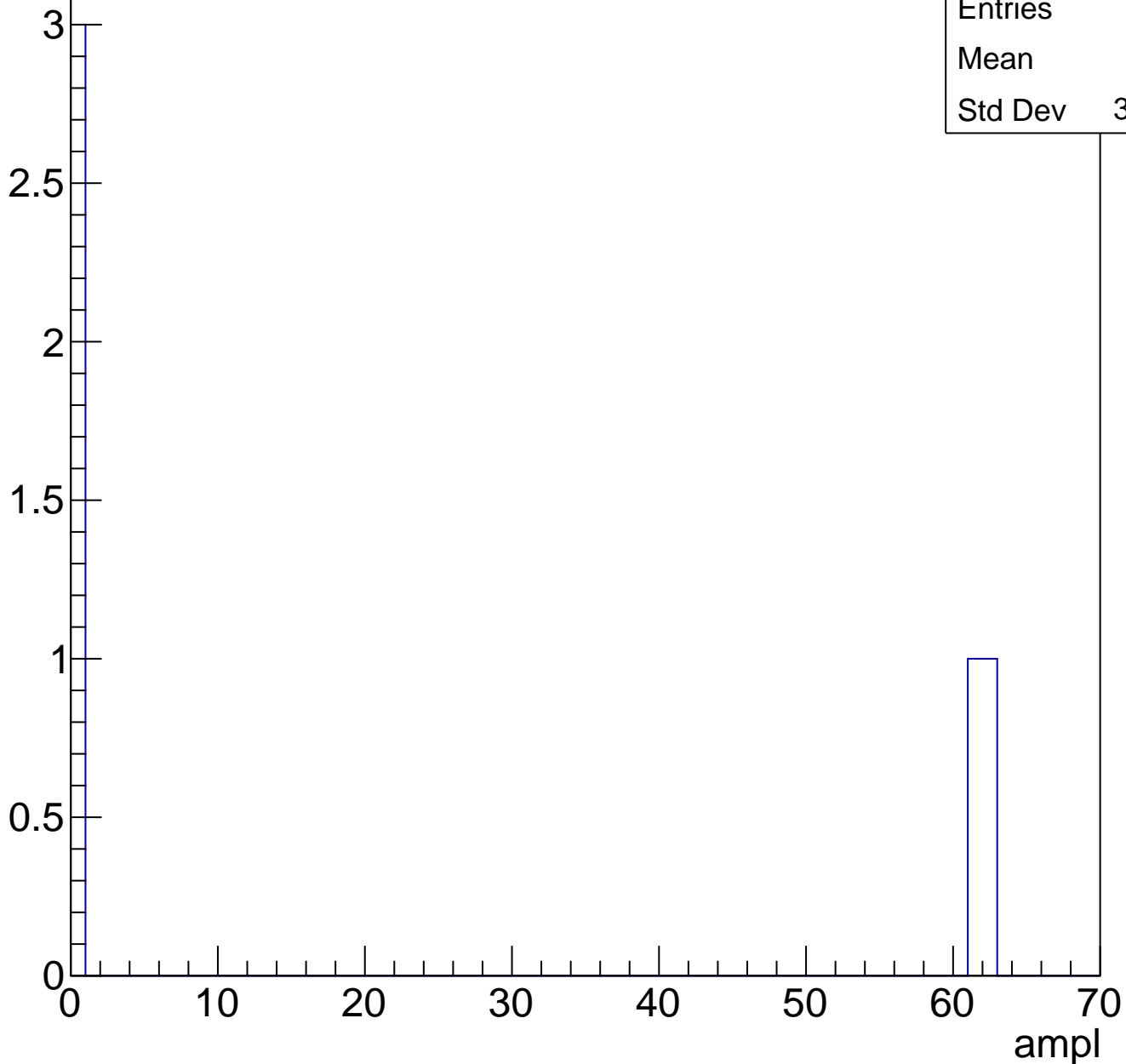




# B1L103S, U2-ch48, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch49, adc0

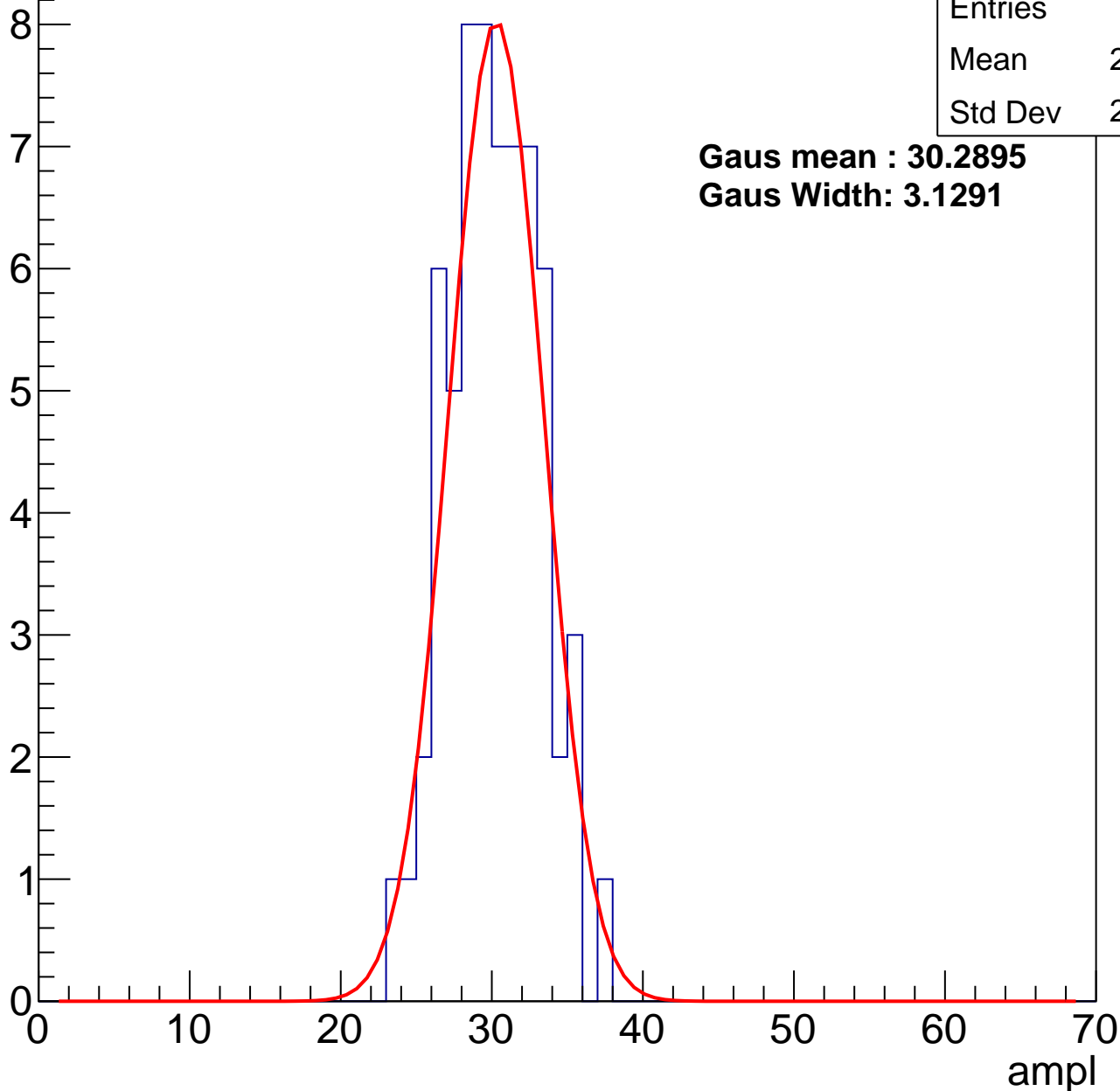
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	29.73
Std Dev	2.949

**Gaus mean : 30.2895**

**Gaus Width: 3.1291**



# B1L103S, U2-ch49, adc1

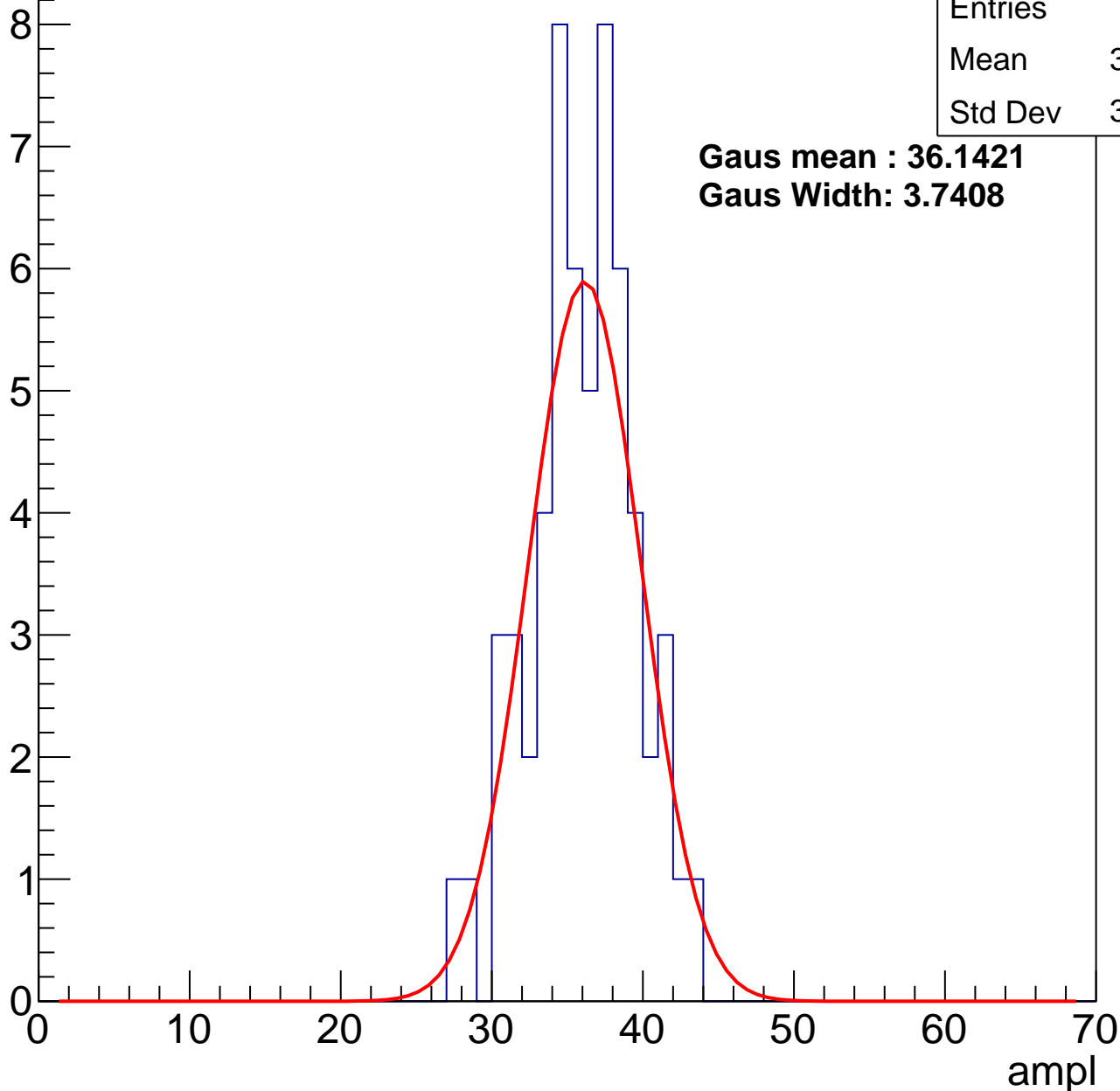
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	35.59
Std Dev	3.434

**Gaus mean : 36.1421**

**Gaus Width: 3.7408**



# B1L103S, U2-ch49, adc2

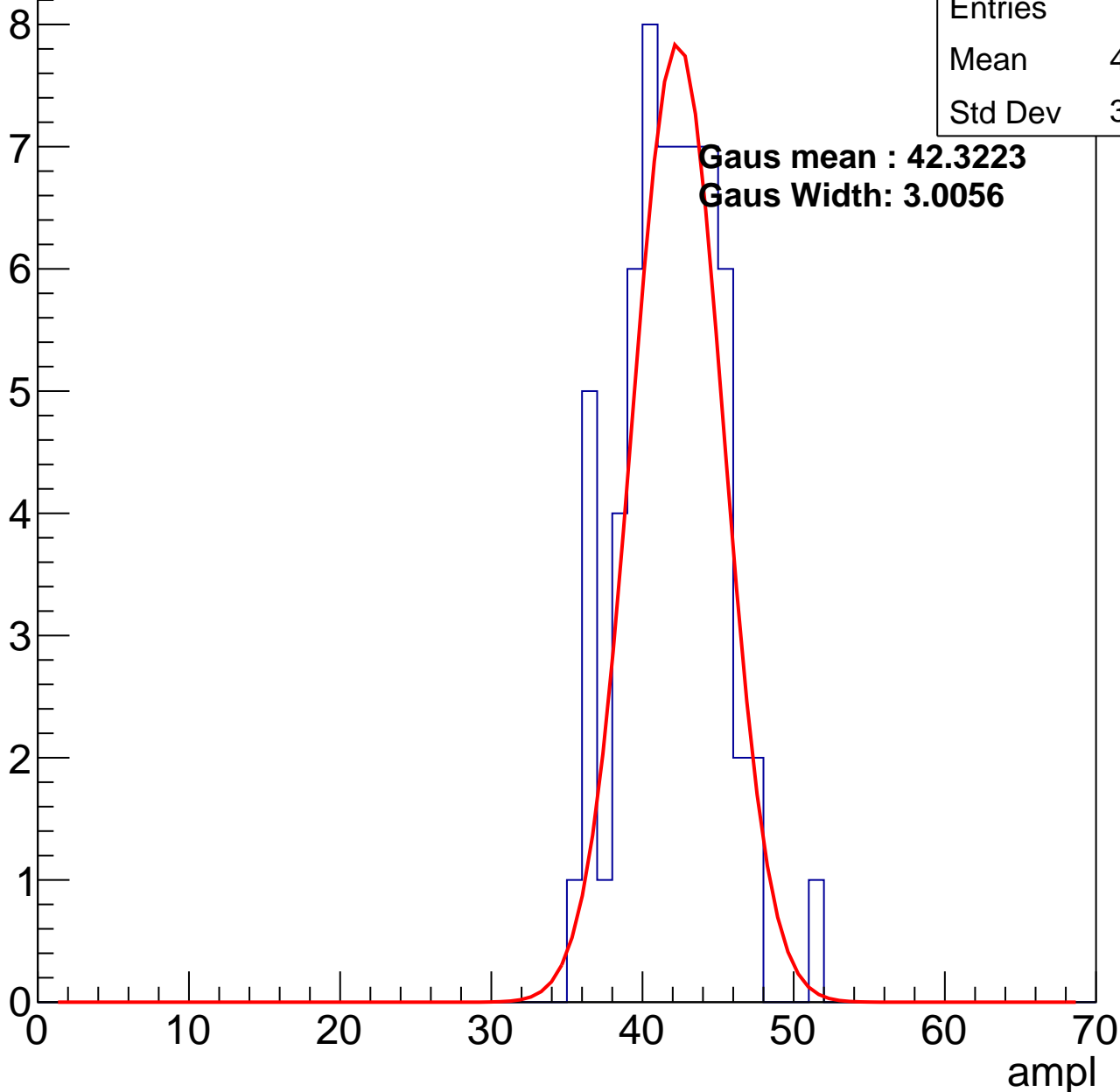
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	41.48
Std Dev	3.177

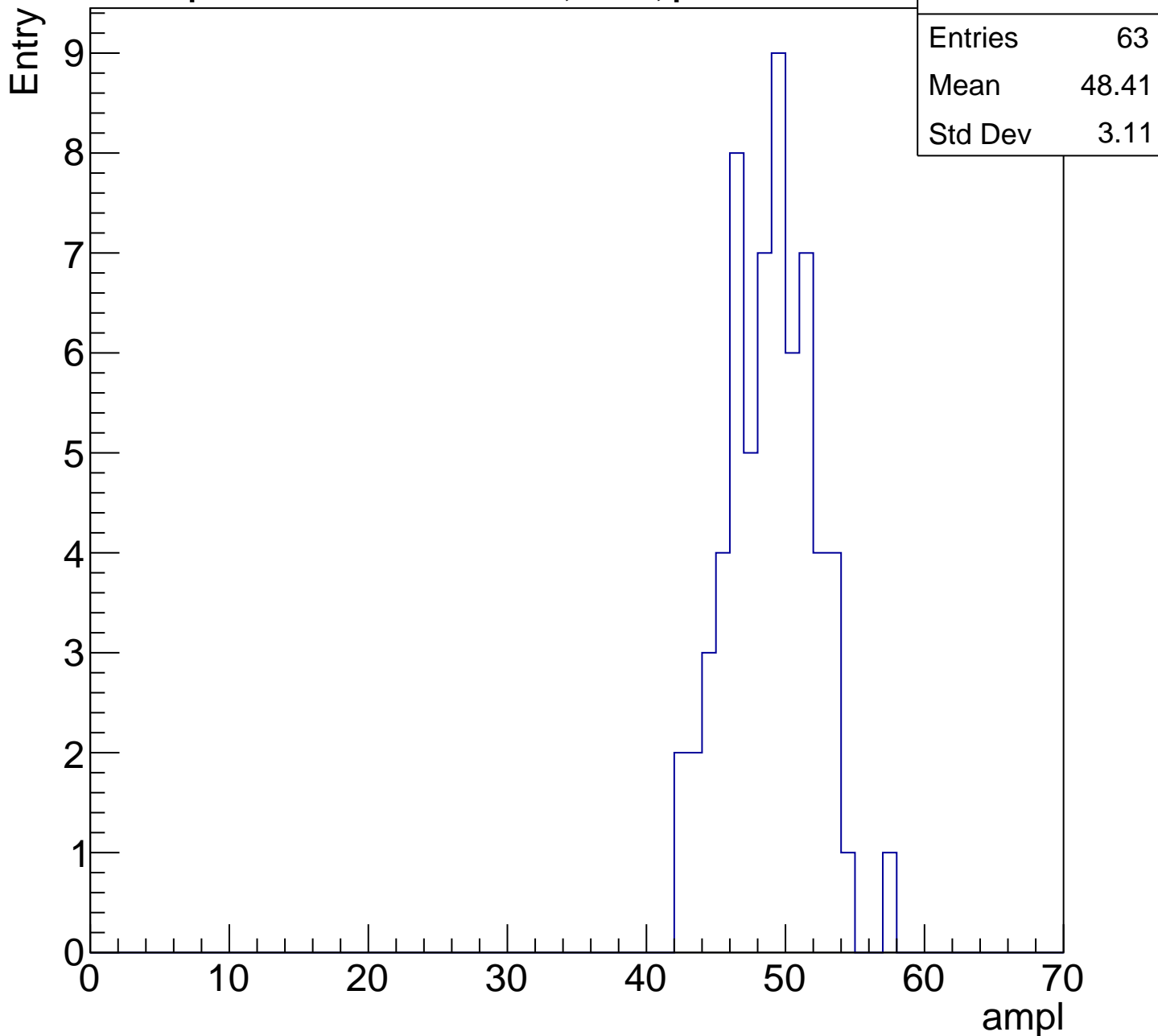
Gaus mean : 42.3223

Gaus Width: 3.0056



# B1L103S, U2-ch49, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

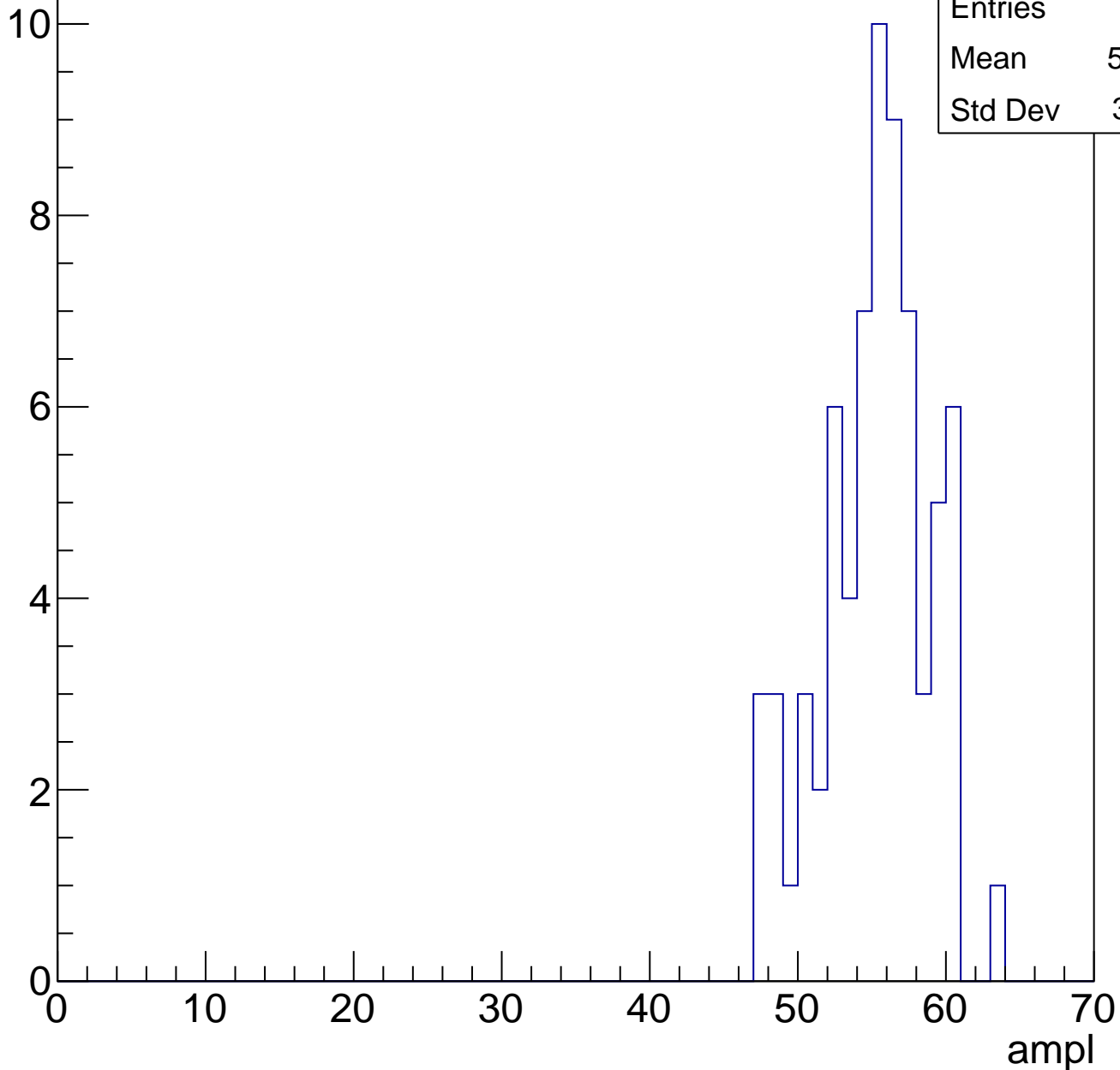


# B1L103S, U2-ch49, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

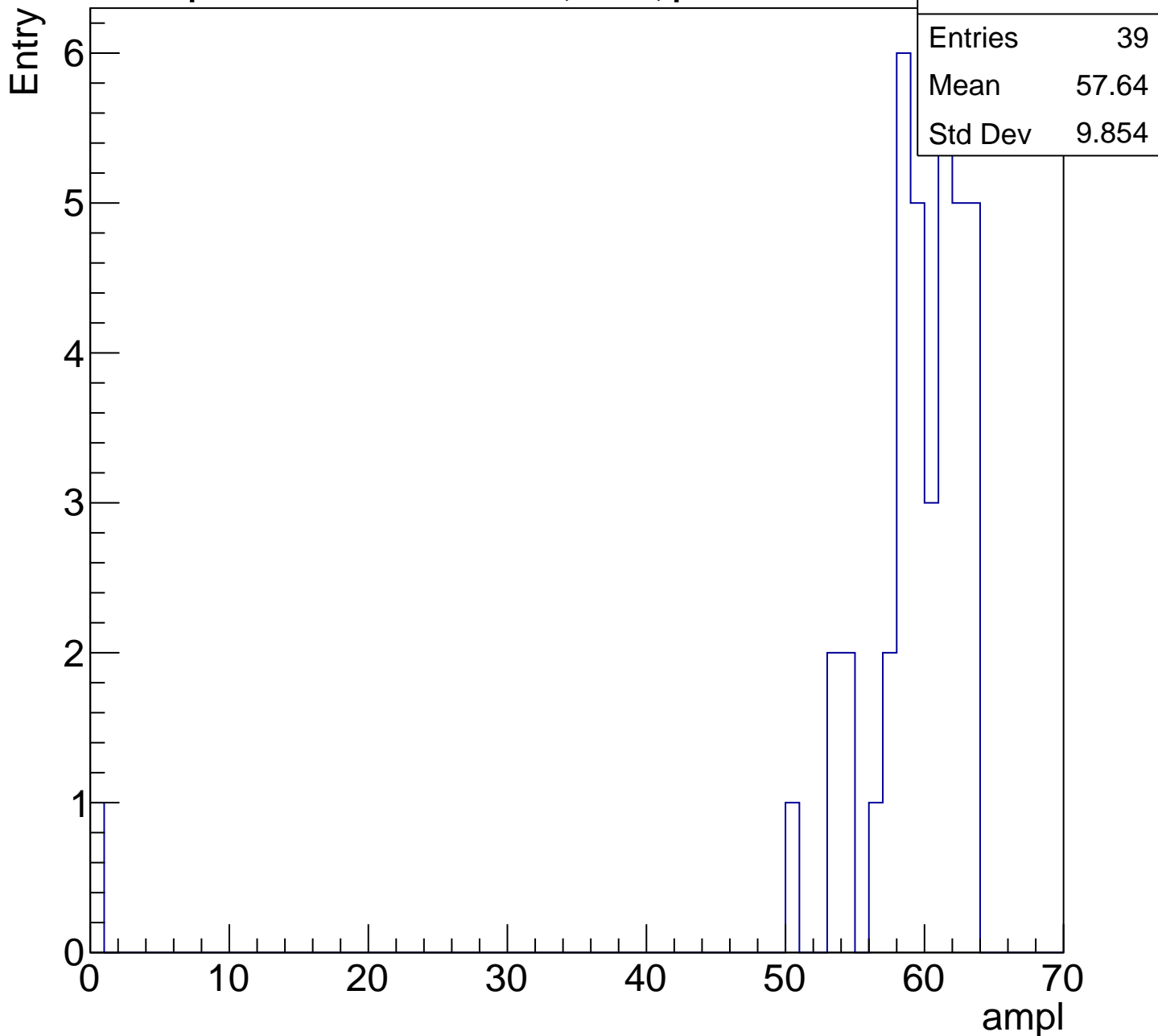
Entries	70
Mean	54.76
Std Dev	3.611

Entry



# B1L103S, U2-ch49, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

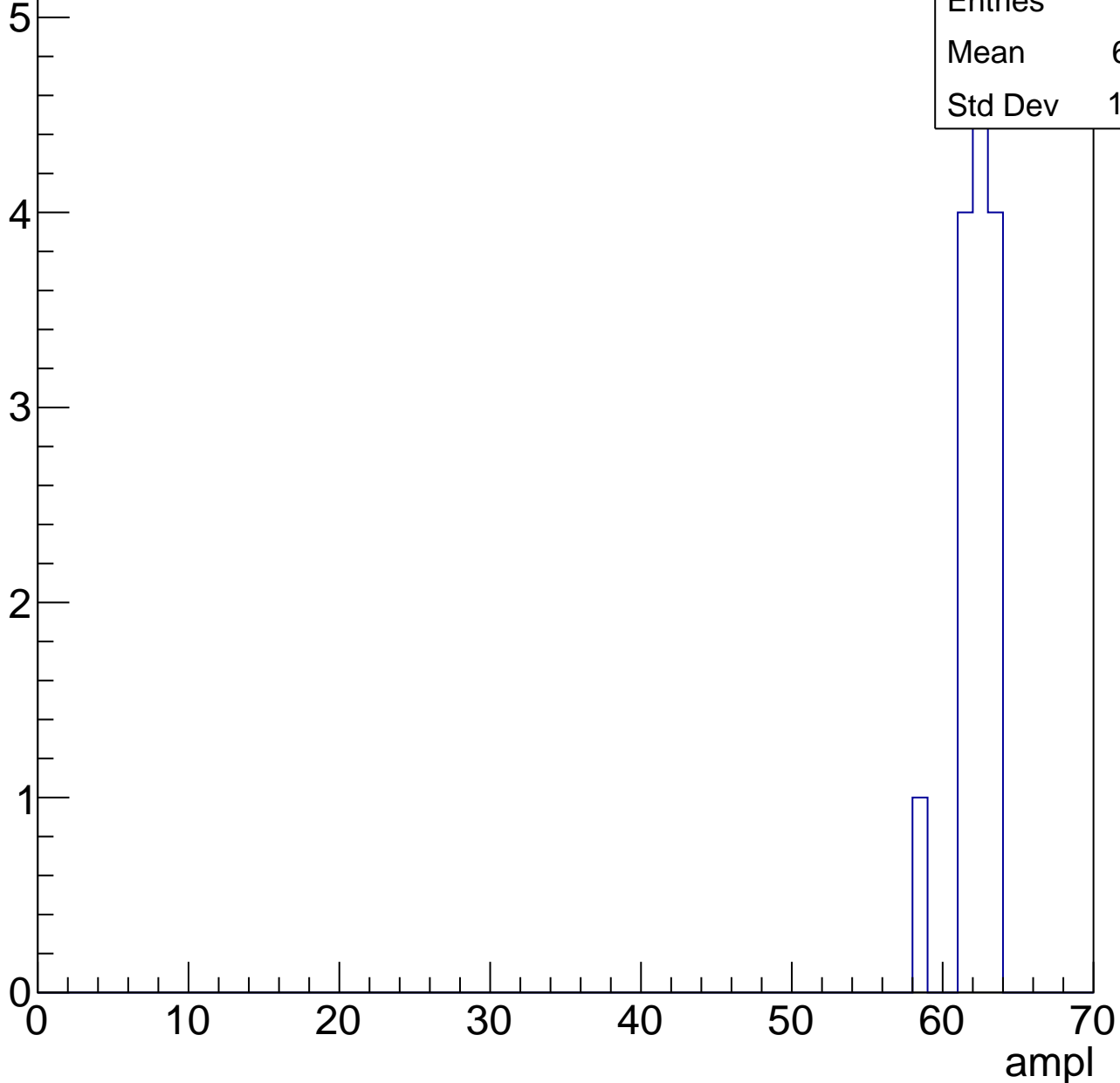


# B1L103S, U2-ch49, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	14
Mean	61.71
Std Dev	1.278

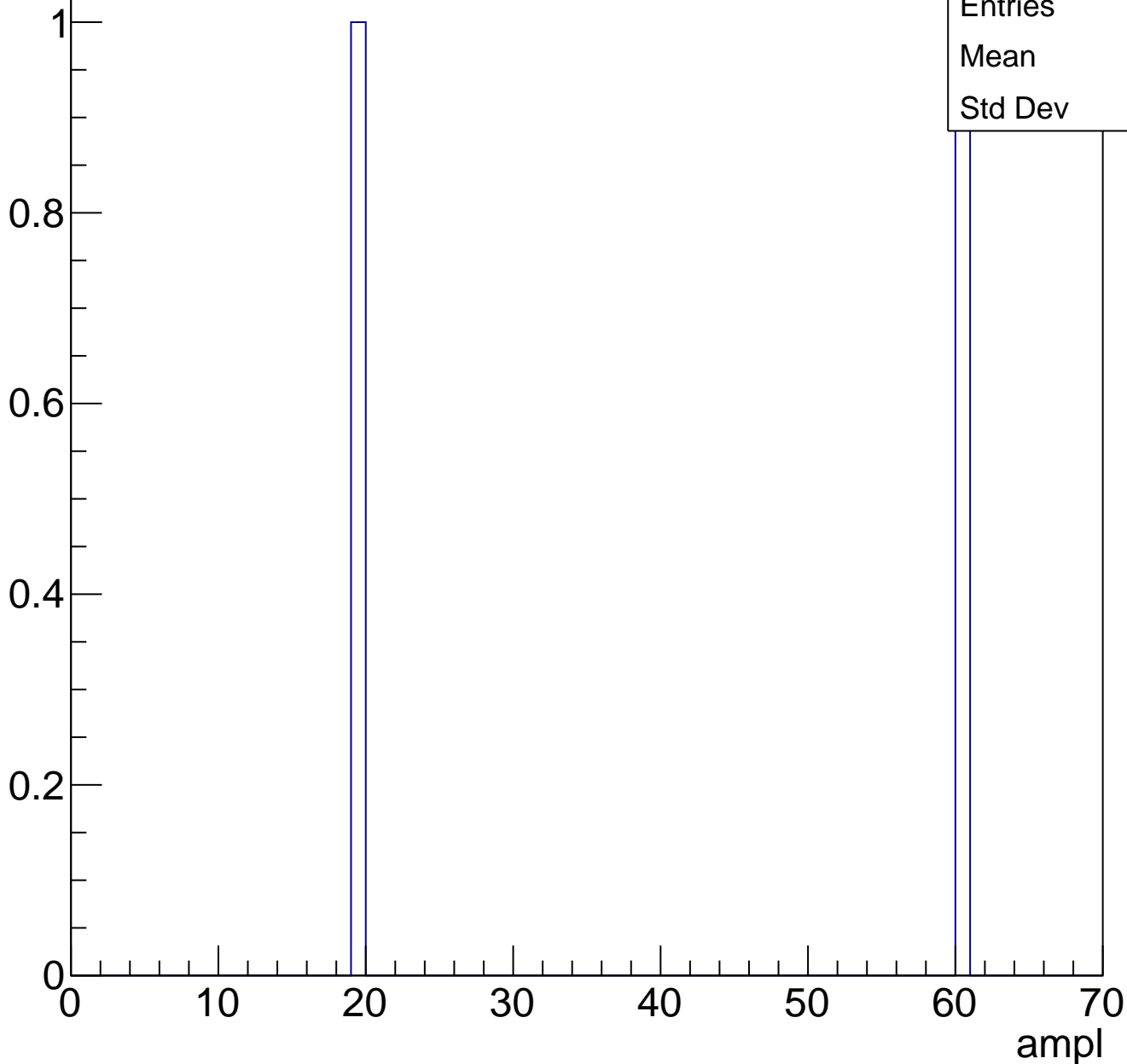




# B1L103S, U2-ch49, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch50, adc0

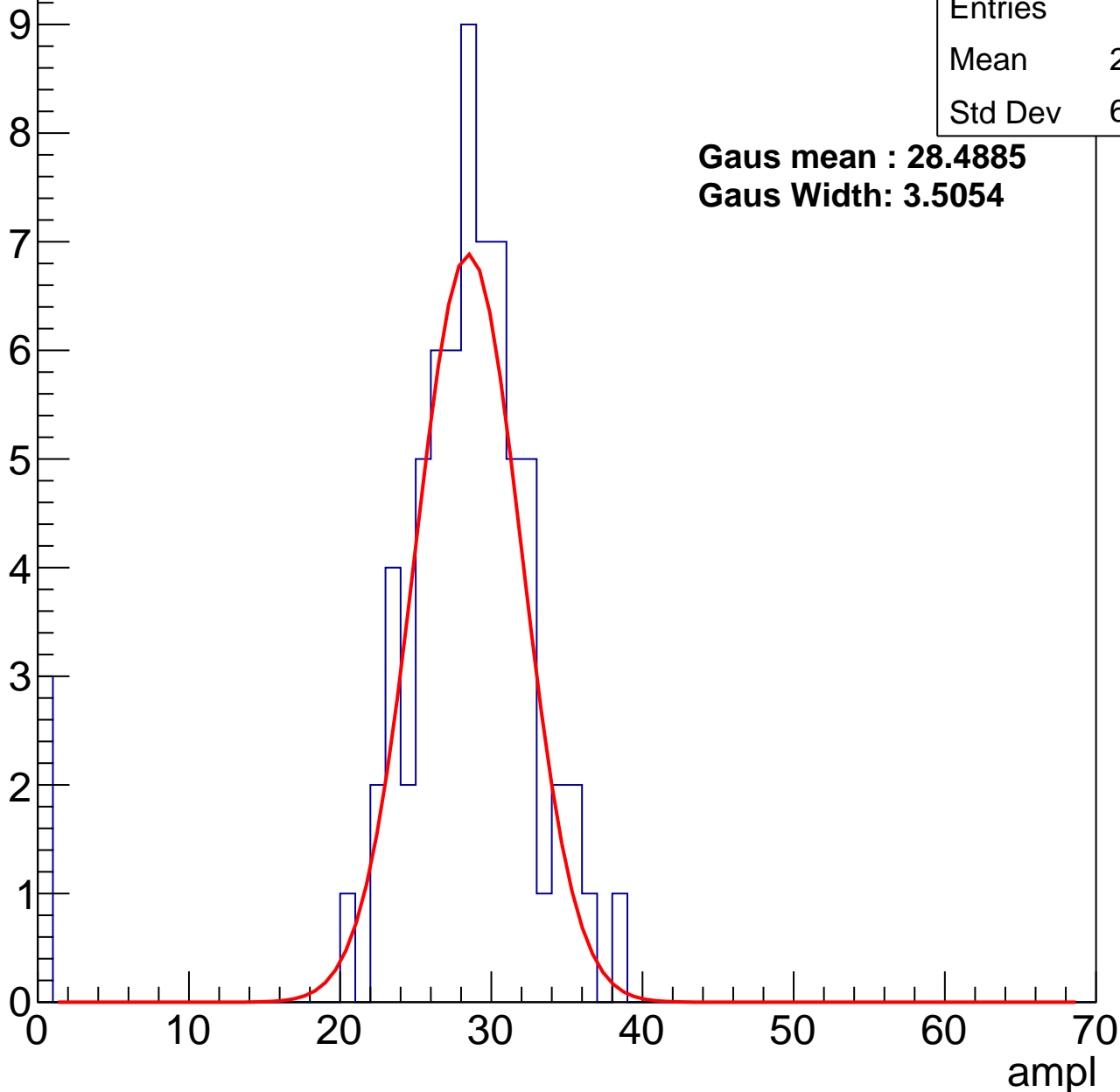
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	27.13
Std Dev	6.769

**Gaus mean : 28.4885**

**Gaus Width: 3.5054**



# B1L103S, U2-ch50, adc1

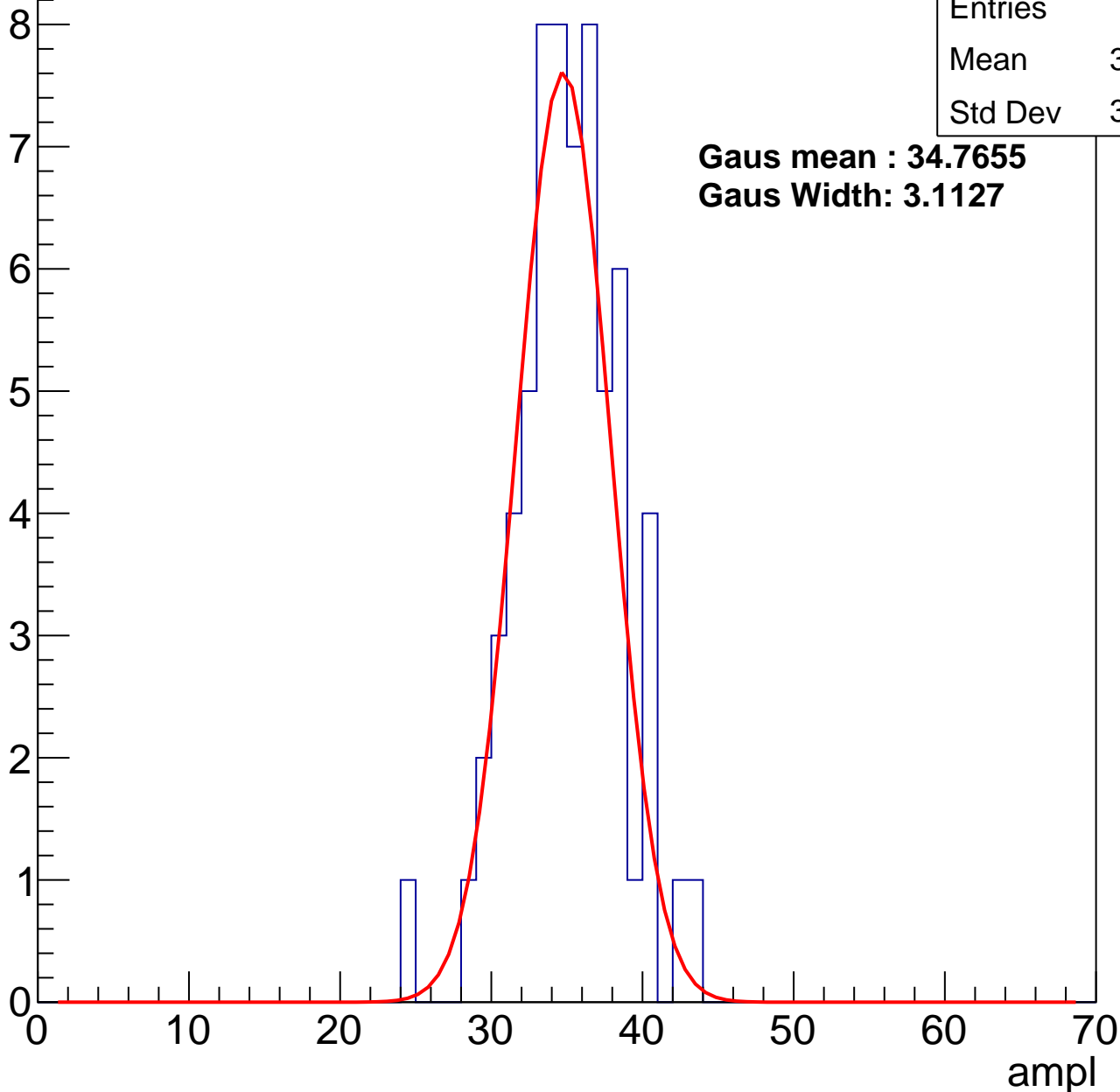
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	34.62
Std Dev	3.436

**Gaus mean : 34.7655**

**Gaus Width: 3.1127**



# B1L103S, U2-ch50, adc2

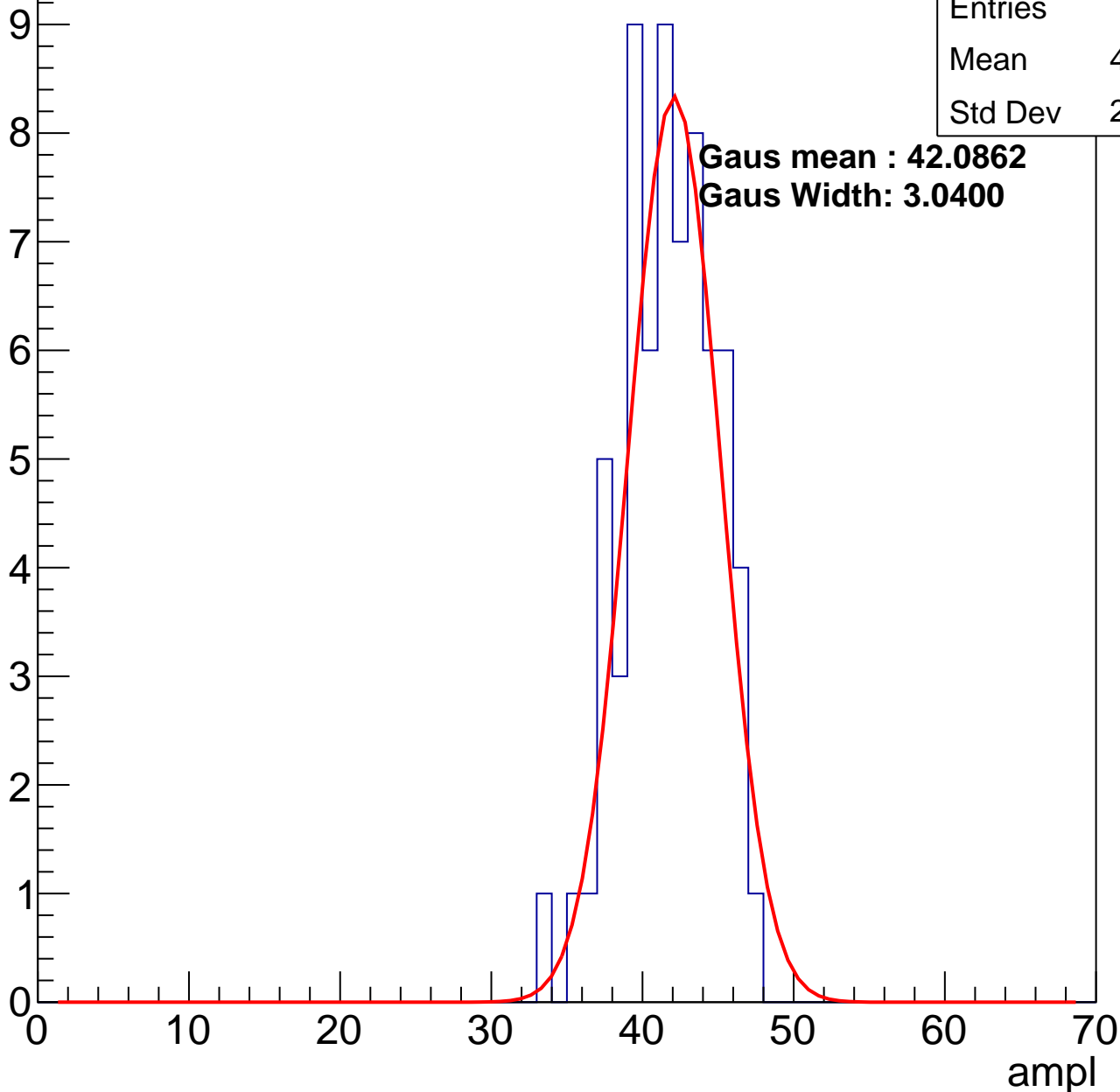
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	41.28
Std Dev	2.977

**Gaus mean : 42.0862**

**Gaus Width: 3.0400**

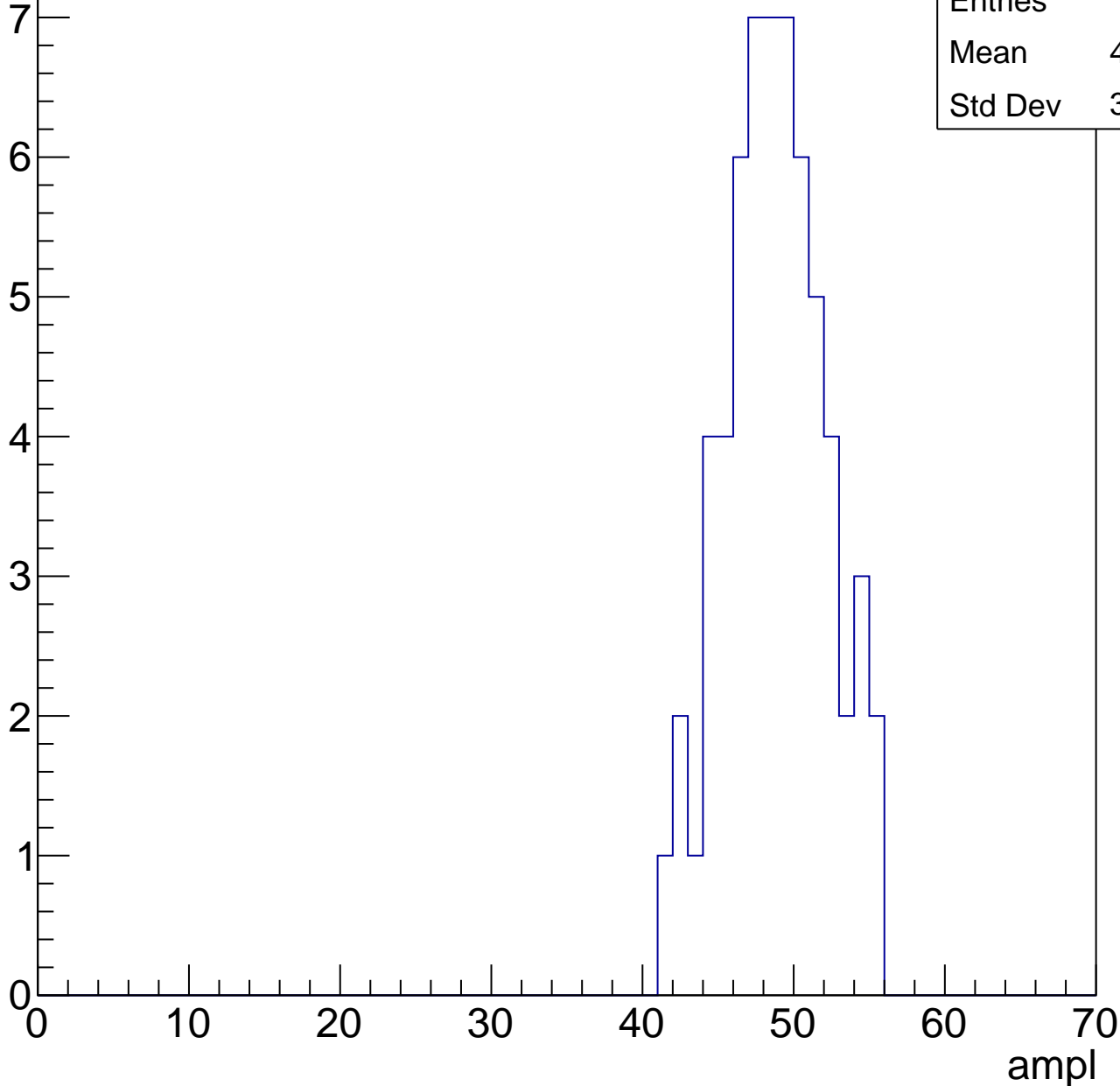


# B1L103S, U2-ch50, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

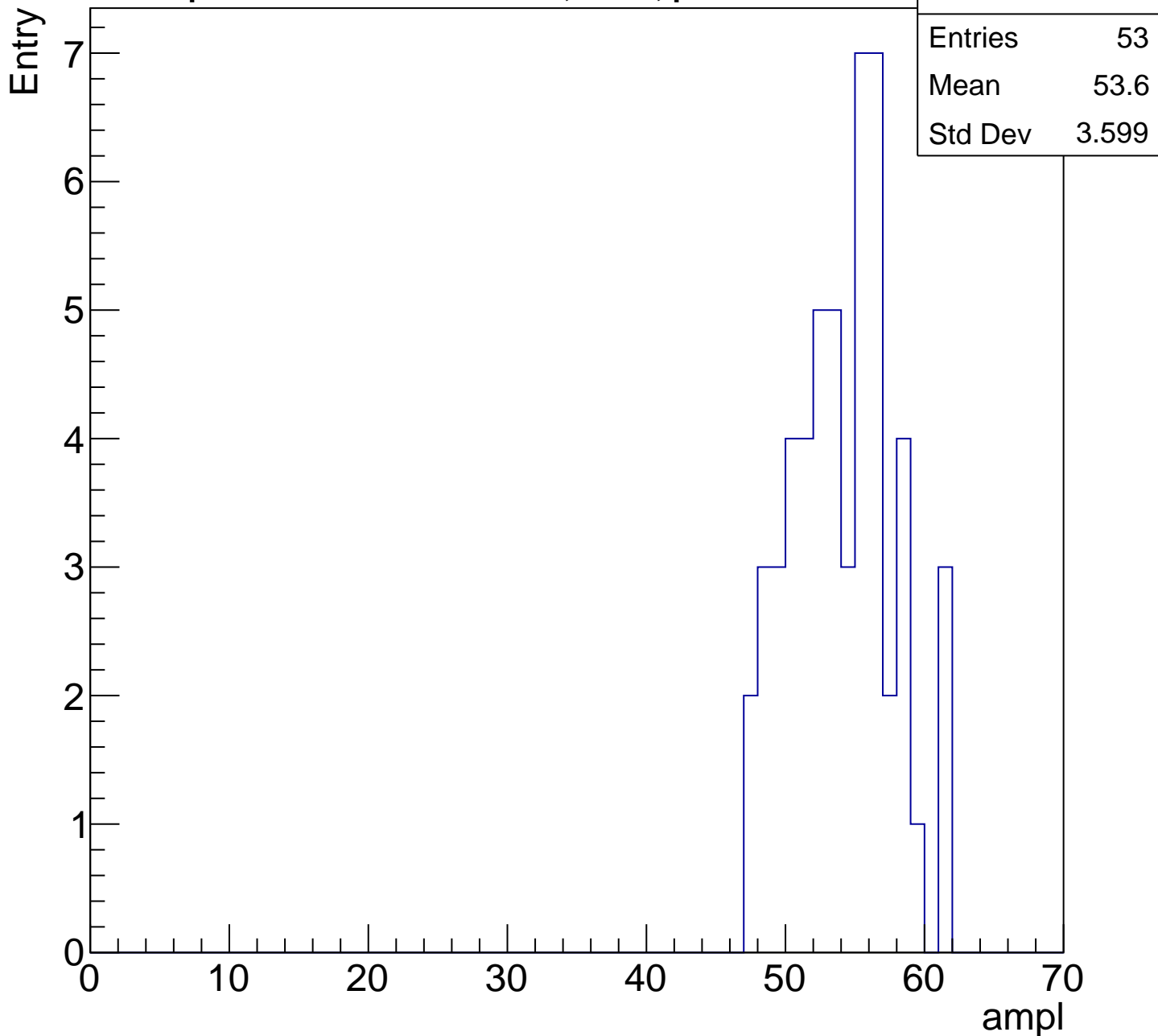
Entry

Entries	61
Mean	48.34
Std Dev	3.304



# B1L103S, U2-ch50, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

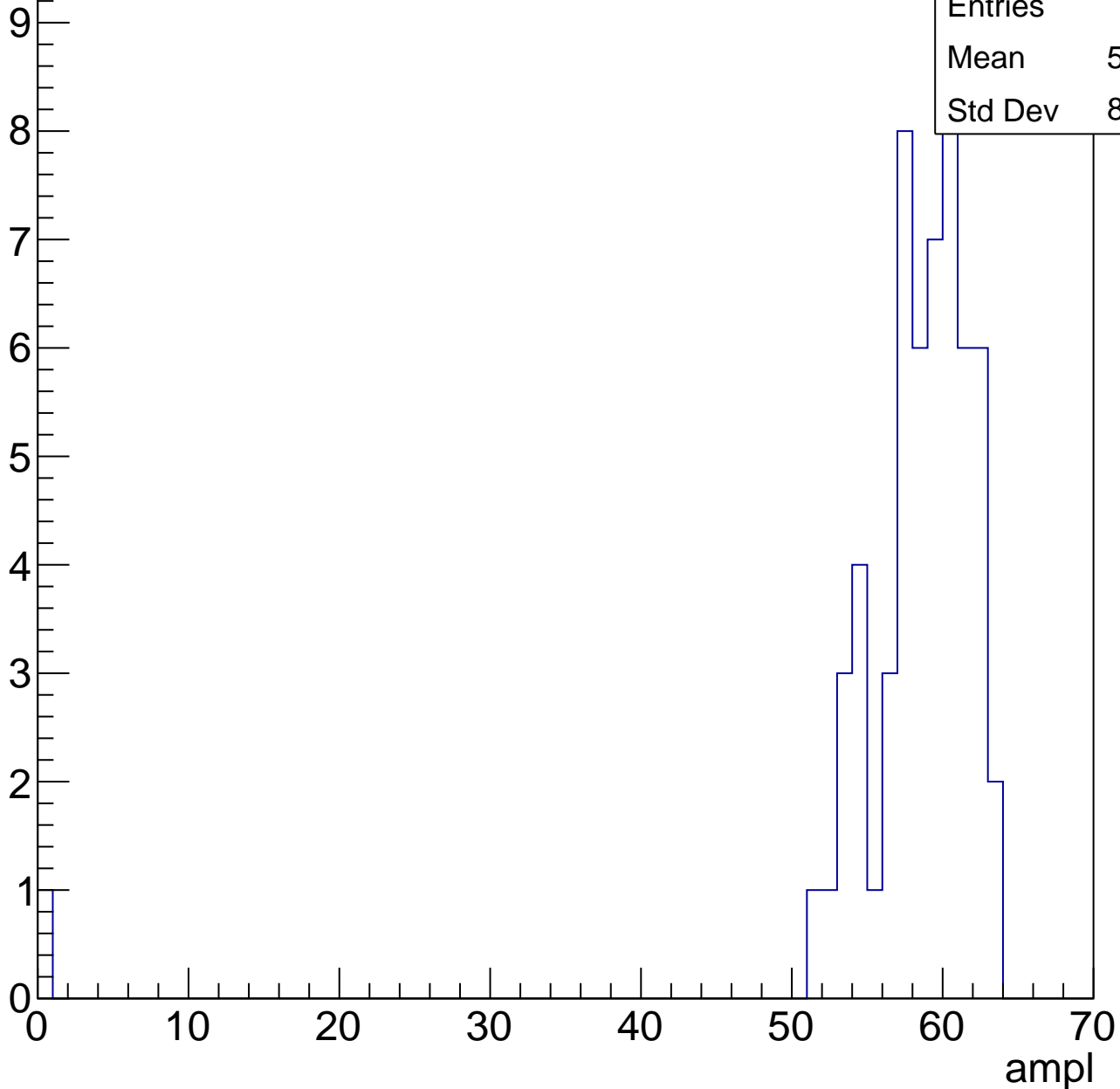


# B1L103S, U2-ch50, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	57.28
Std Dev	8.126



# B1L103S, U2-ch50, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

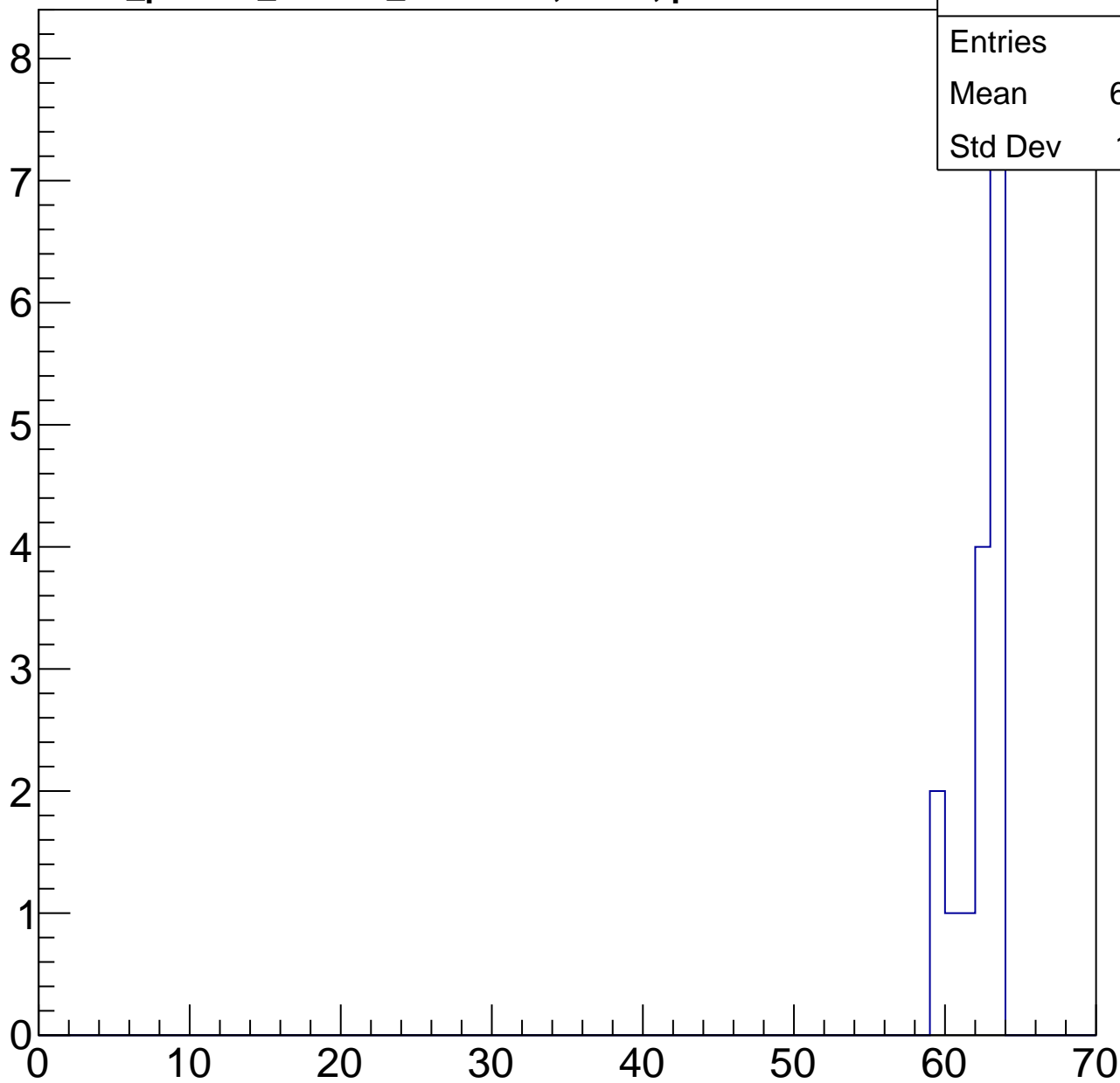
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	16
Mean	61.94
Std Dev	1.391

ampl

0 10 20 30 40 50 60 70





# B1L103S, U2-ch50, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U2-ch51, adc0

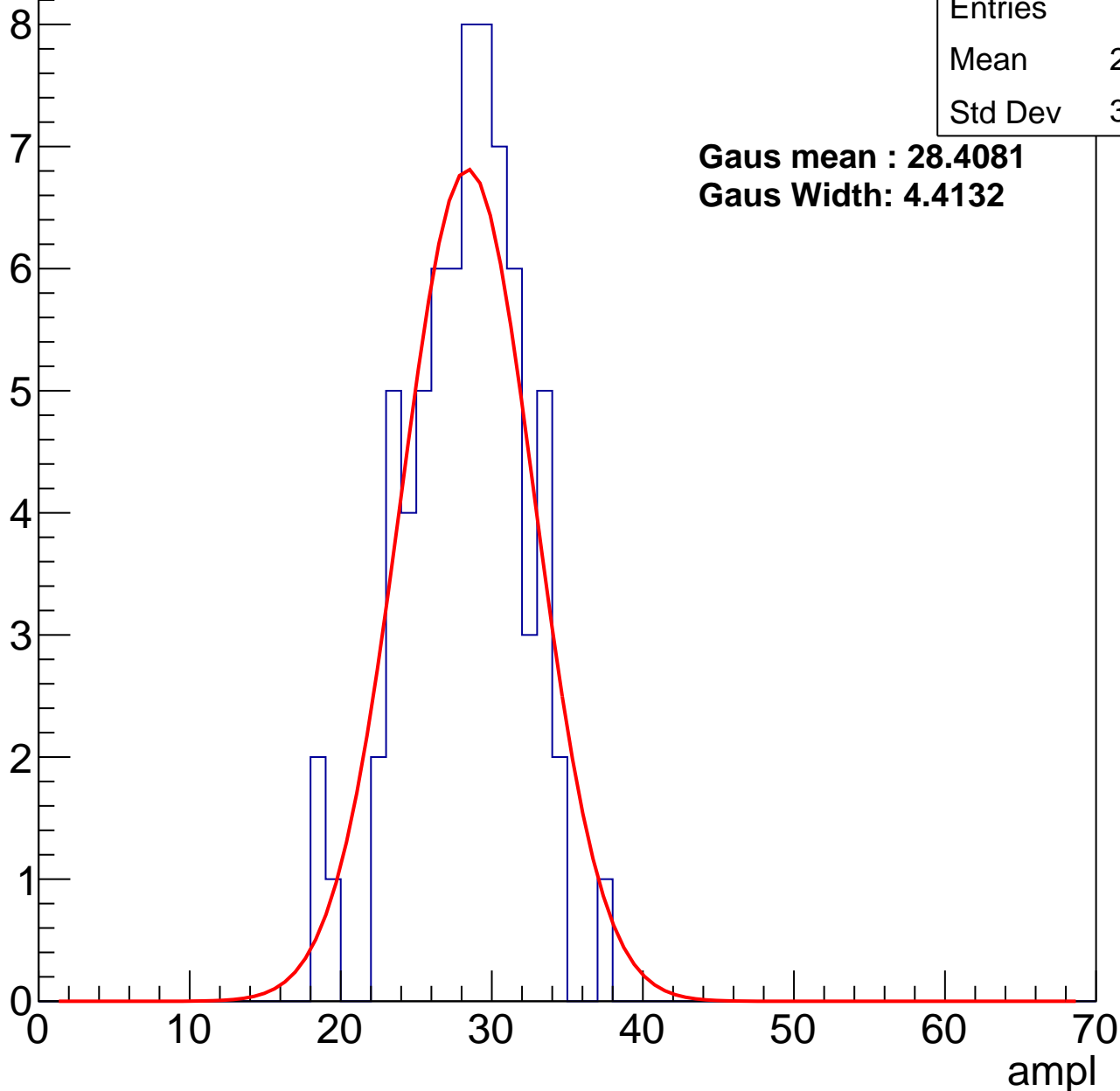
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	27.76
Std Dev	3.807

**Gaus mean : 28.4081**

**Gaus Width: 4.4132**



# B1L103S, U2-ch51, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	74
Mean	35.86
Std Dev	3.028

**Gaus mean : 36.1158**

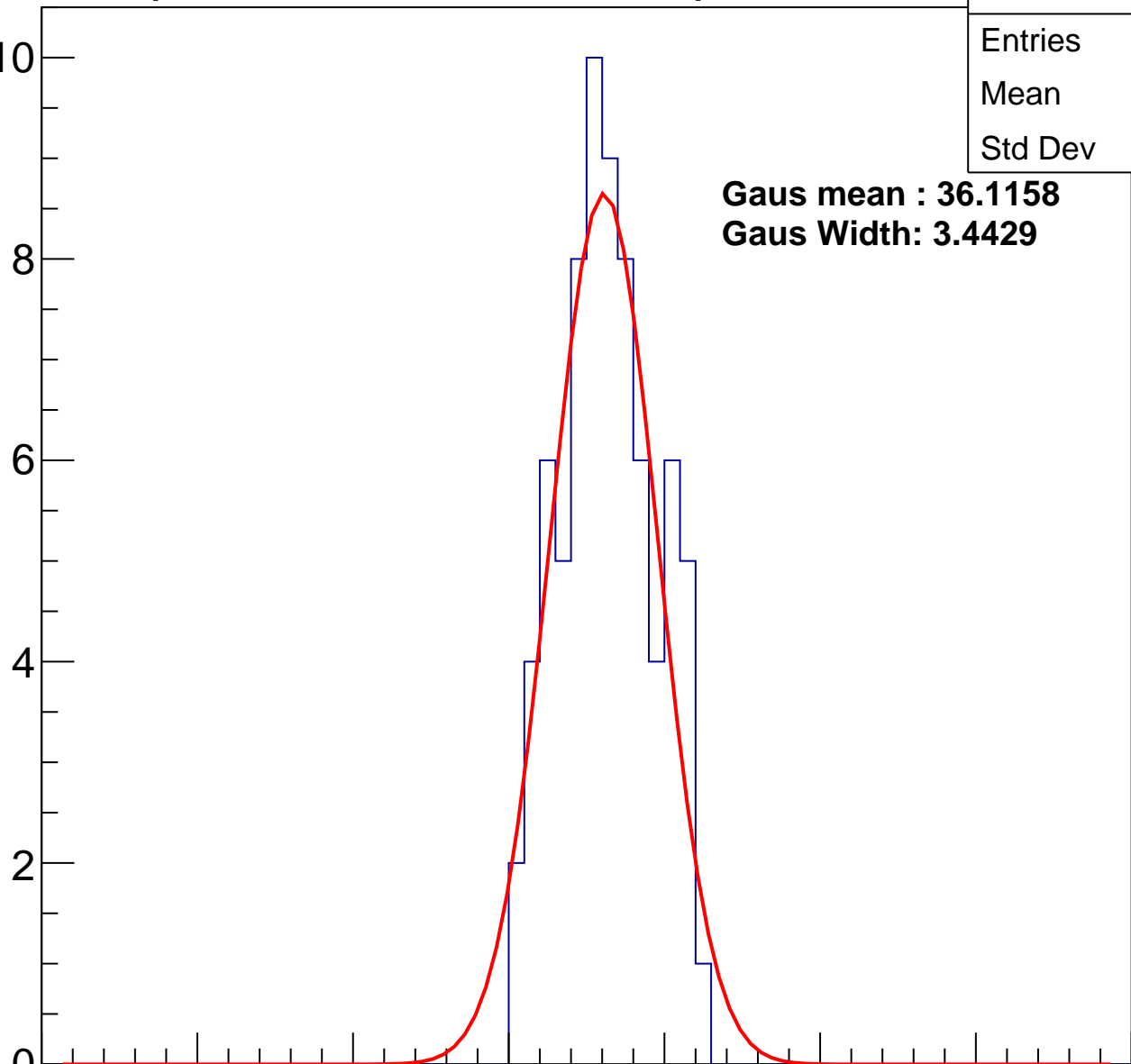
**Gaus Width: 3.4429**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

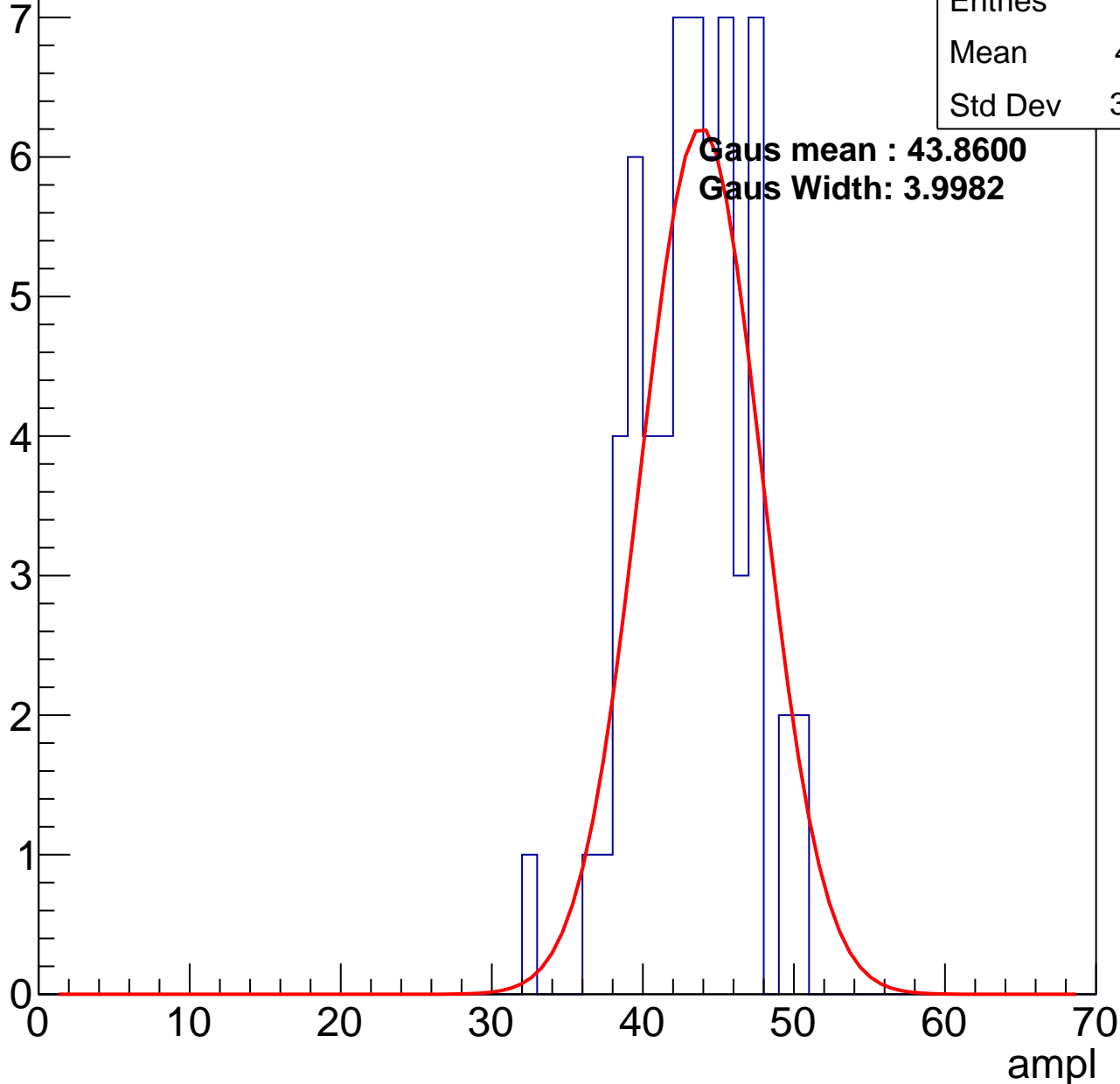


# B1L103S, U2-ch51, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	42.81
Std Dev	3.596

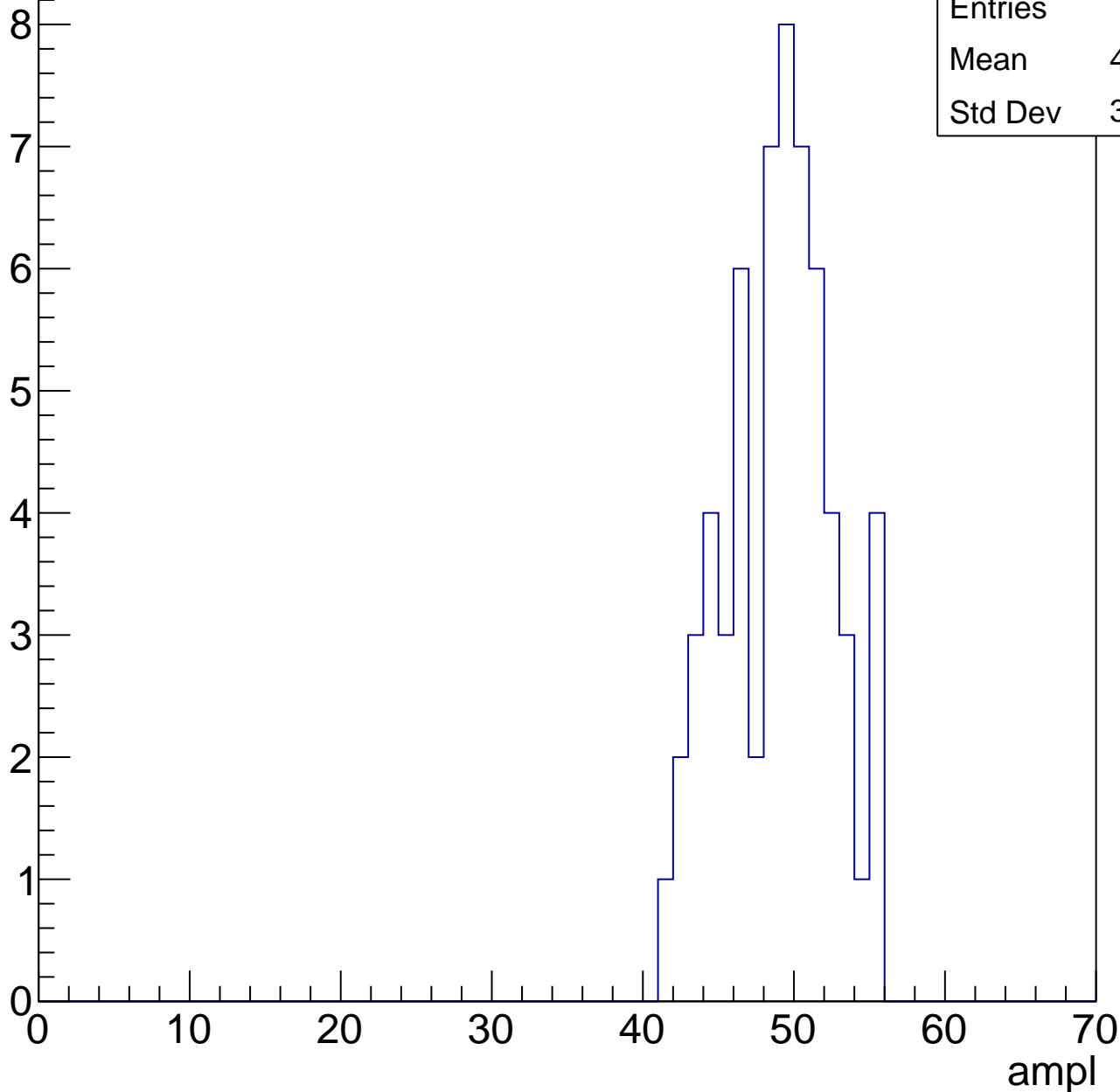


# B1L103S, U2-ch51, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

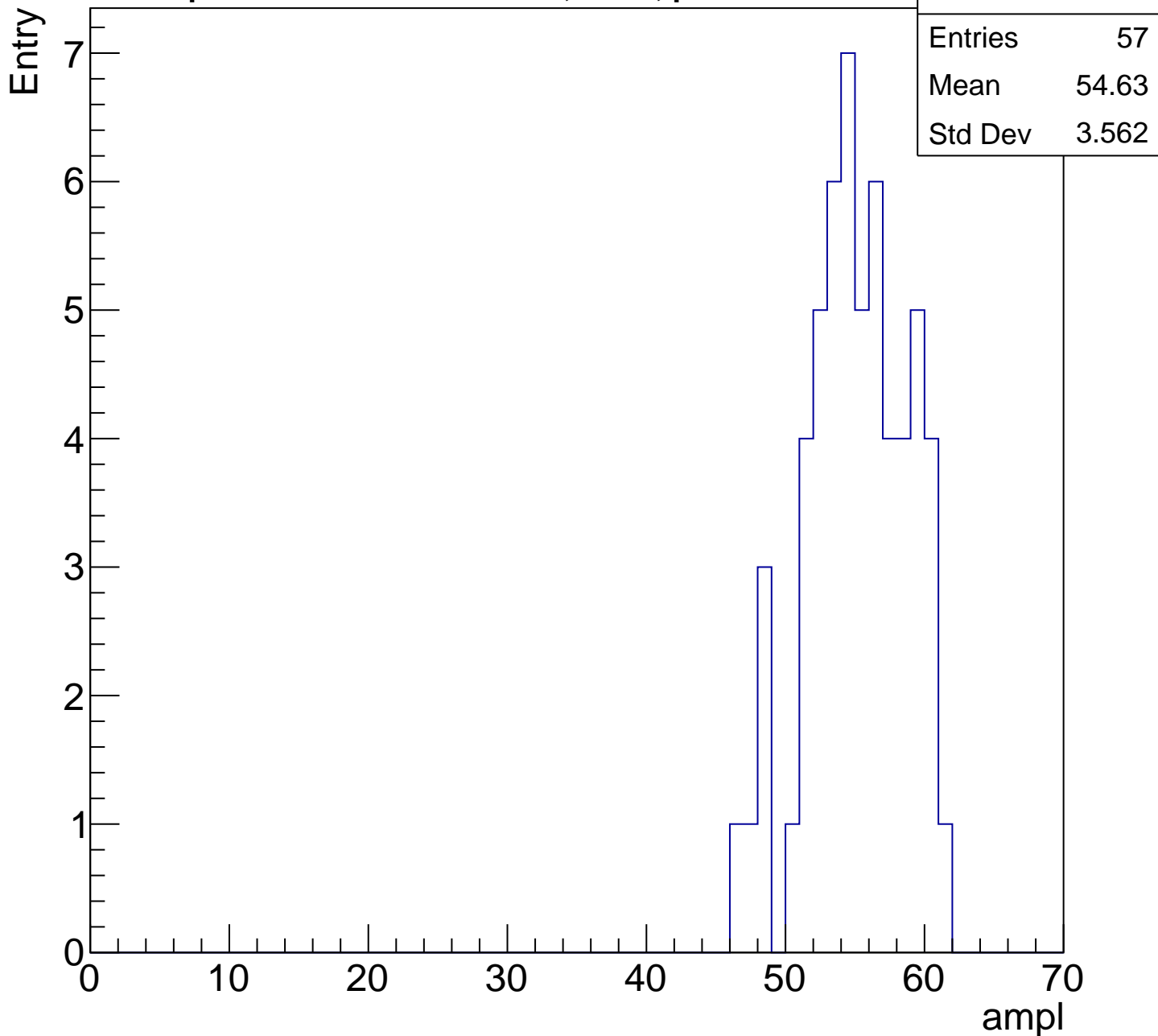
Entry

Entries	61
Mean	48.52
Std Dev	3.523



# B1L103S, U2-ch51, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

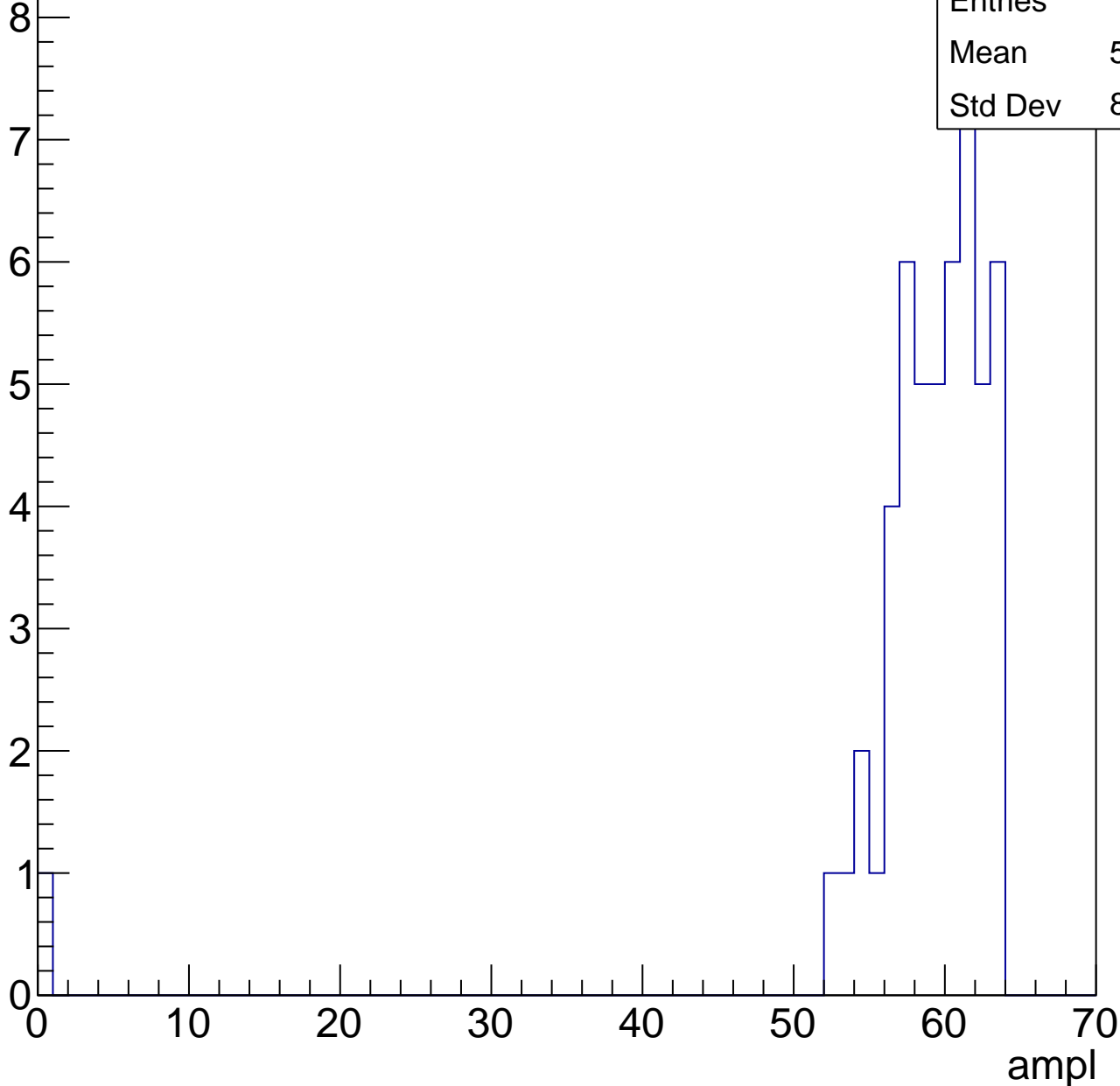


# B1L103S, U2-ch51, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	57.94
Std Dev	8.653

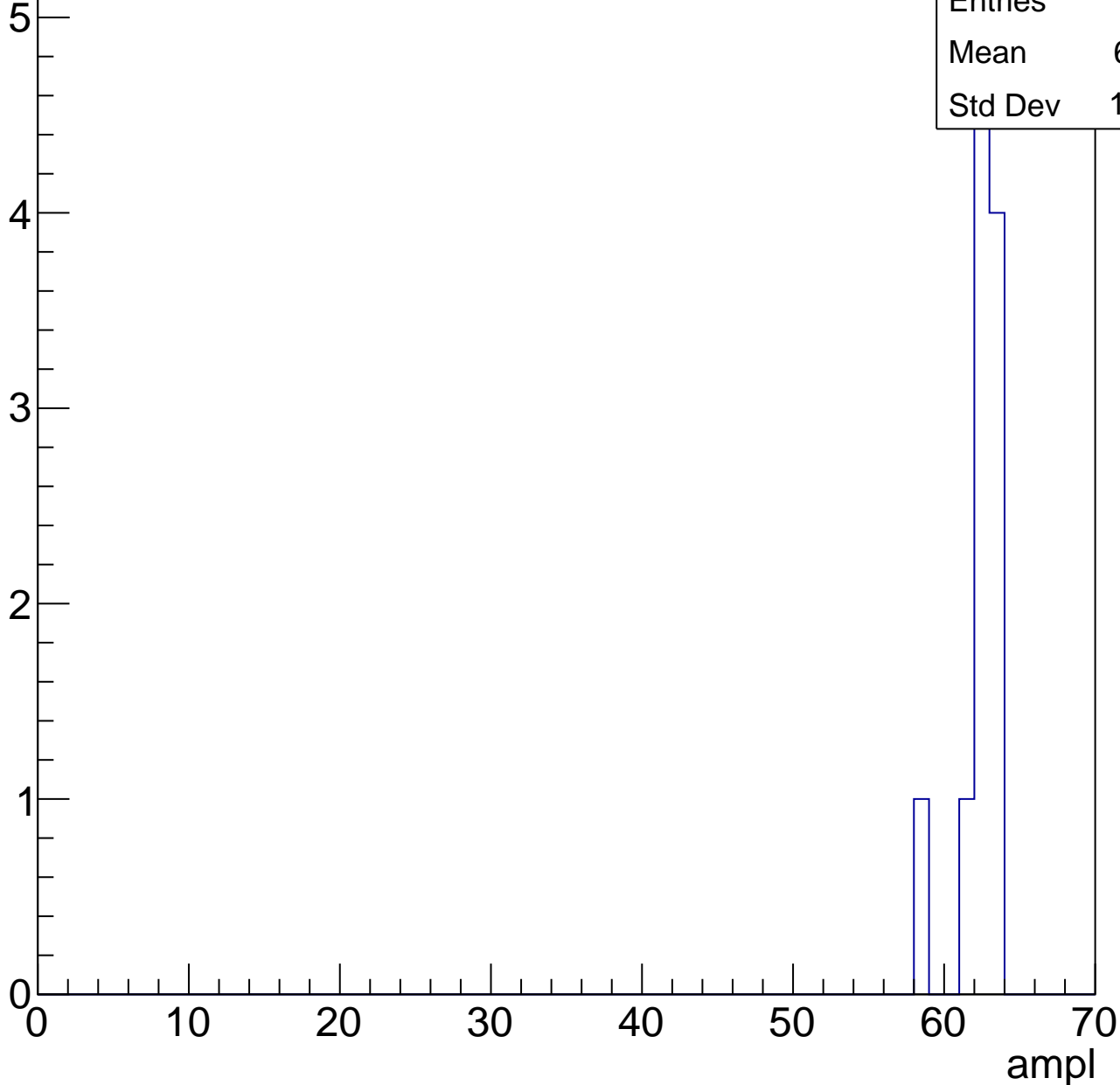


# B1L103S, U2-ch51, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	11
Mean	61.91
Std Dev	1.379





# B1L103S, U2-ch51, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U2-ch52, adc0

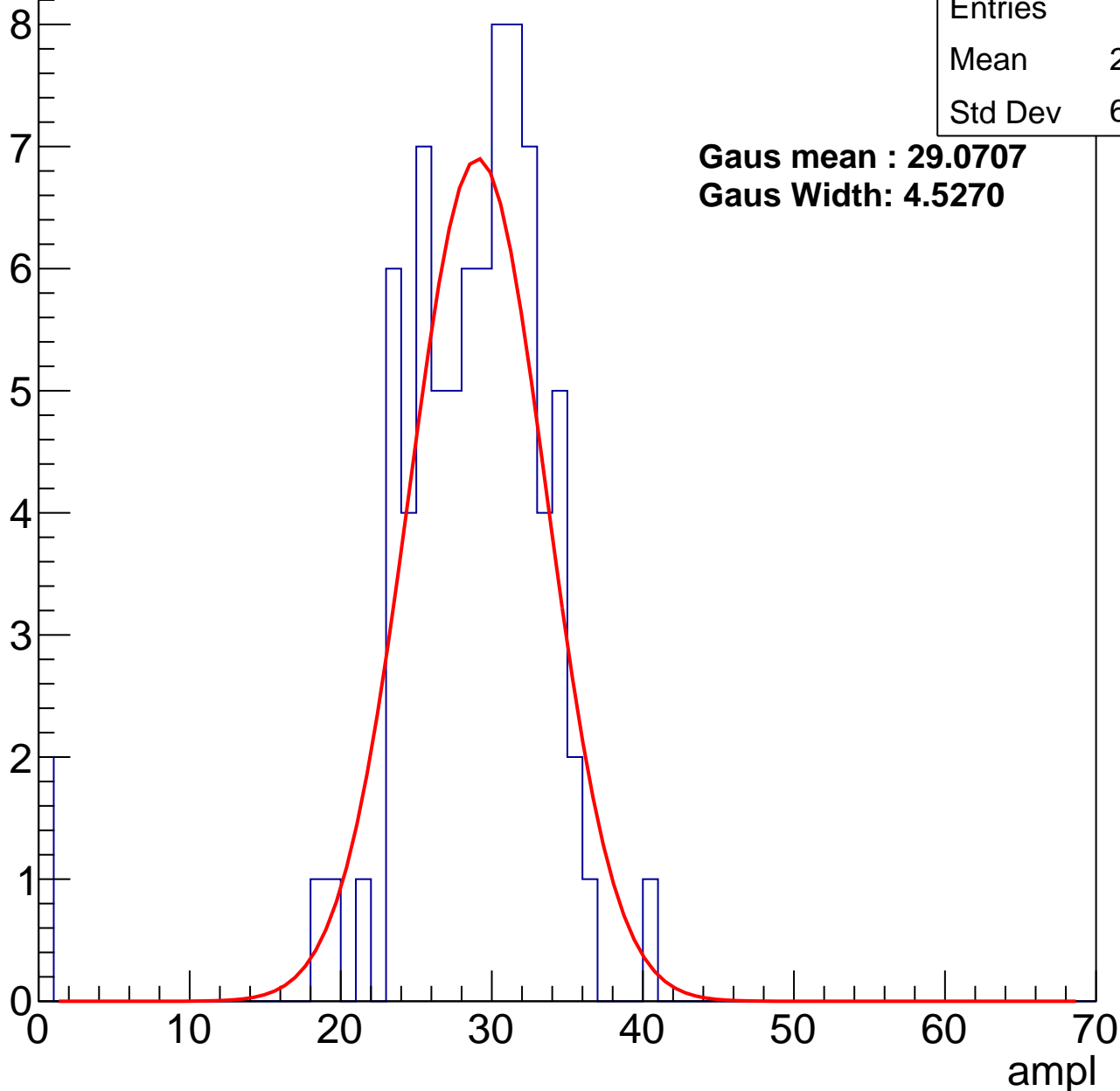
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	80
Mean	27.93
Std Dev	6.029

**Gaus mean : 29.0707**

**Gaus Width: 4.5270**



# B1L103S, U2-ch52, adc1

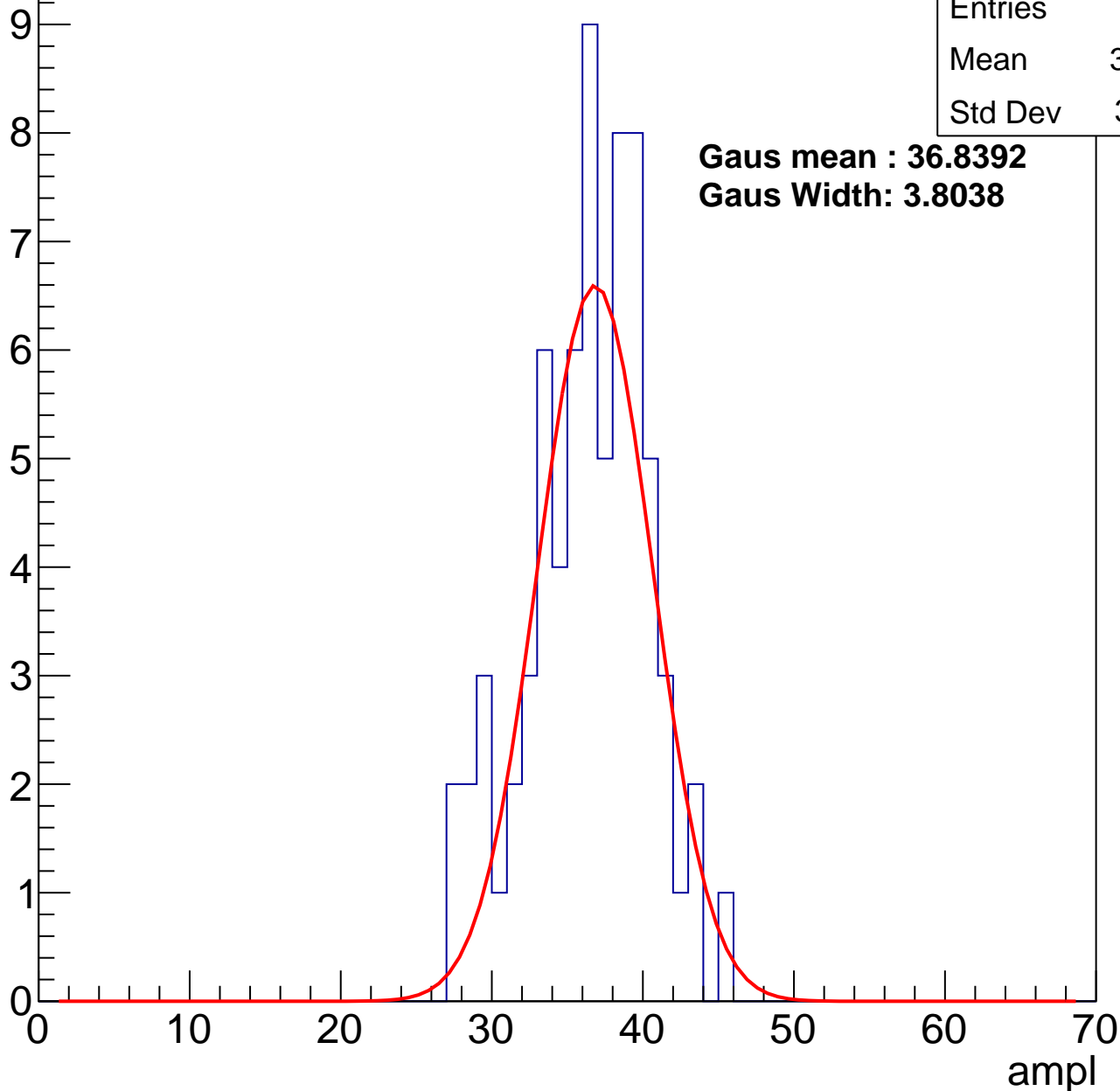
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	35.92
Std Dev	3.981

**Gaus mean : 36.8392**

**Gaus Width: 3.8038**



# B1L103S, U2-ch52, adc2

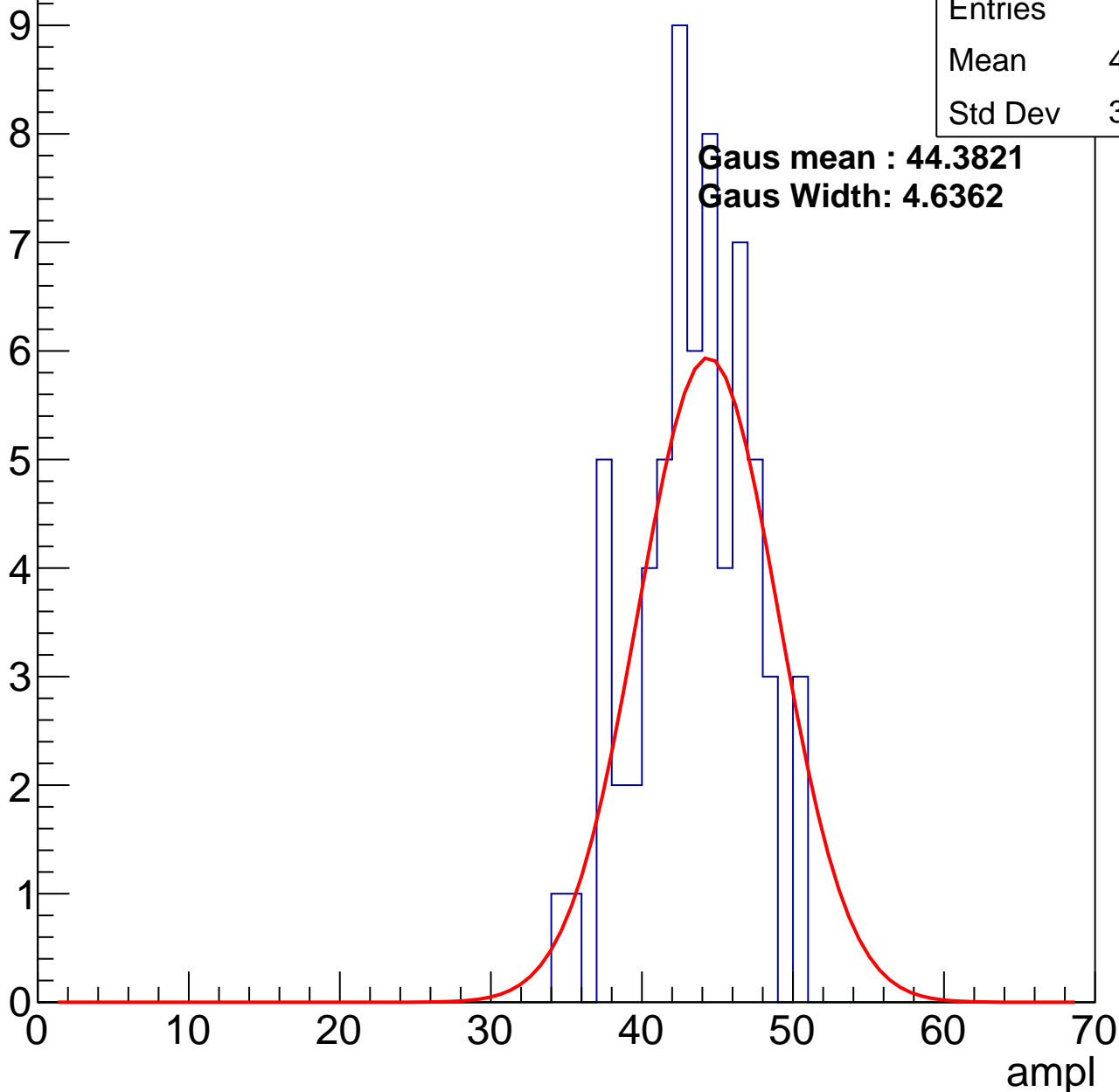
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	42.95
Std Dev	3.639

**Gaus mean : 44.3821**

**Gaus Width: 4.6362**

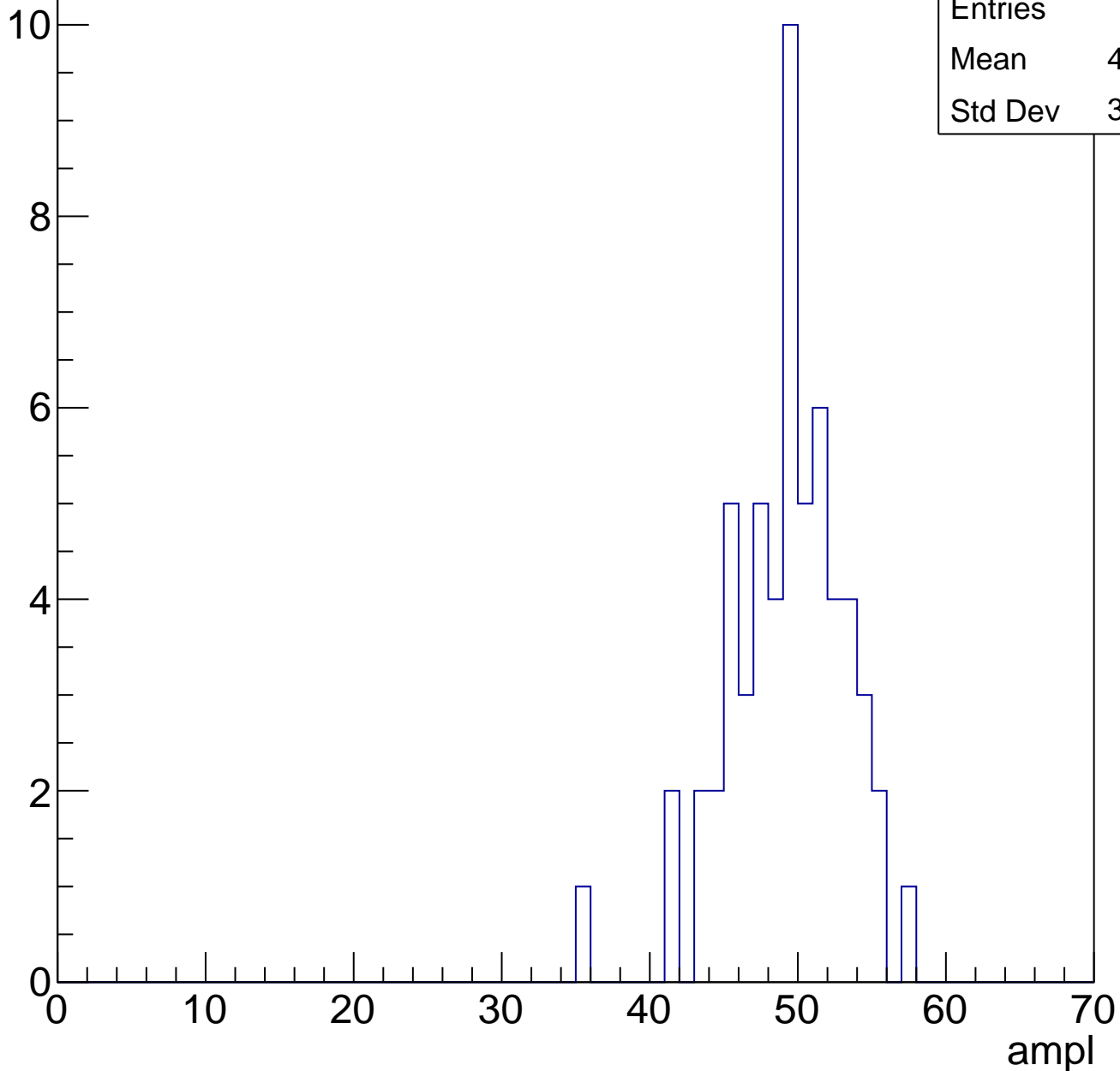


# B1L103S, U2-ch52, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

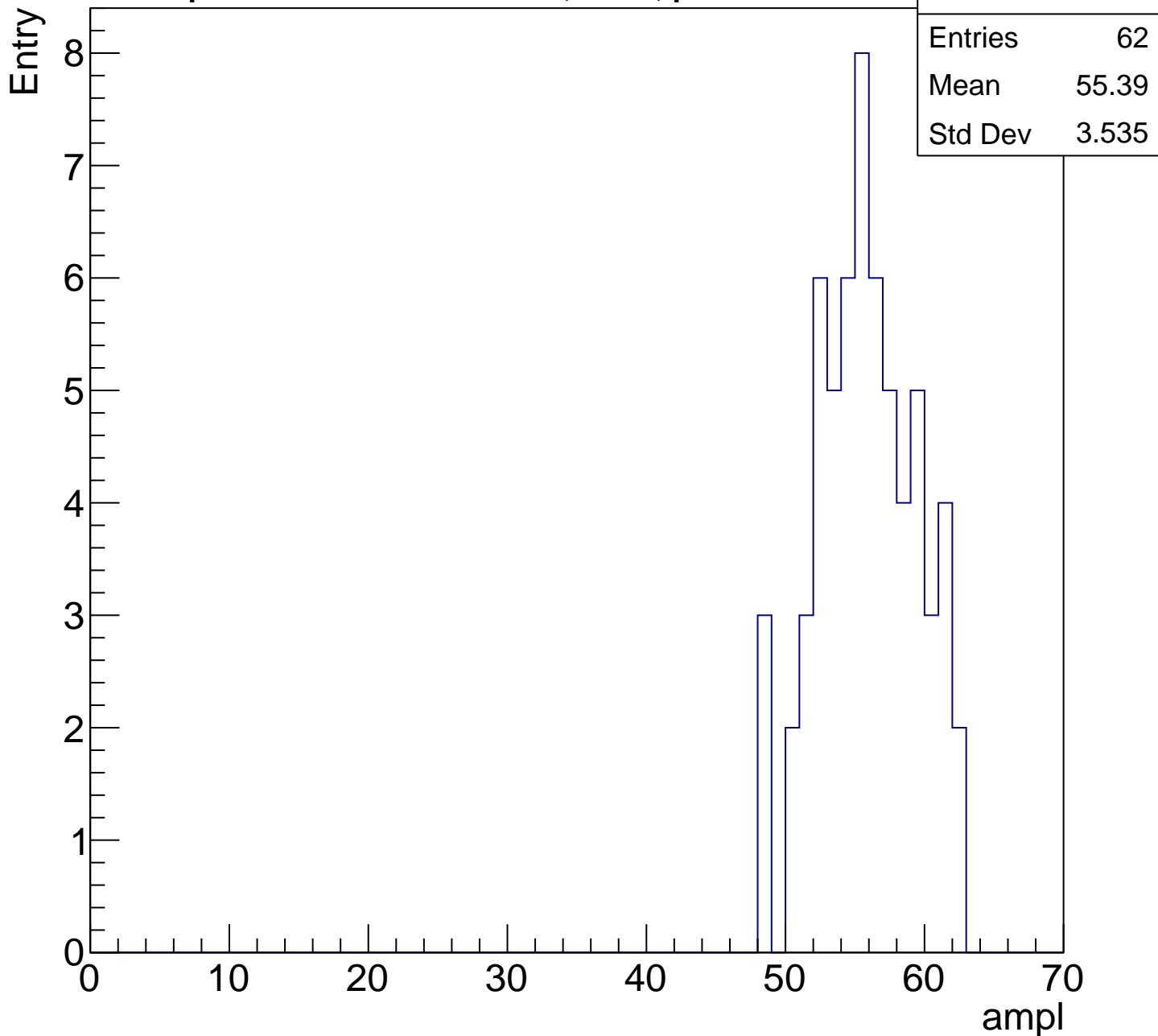
Entries	59
Mean	48.75
Std Dev	3.934

Entry



# B1L103S, U2-ch52, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

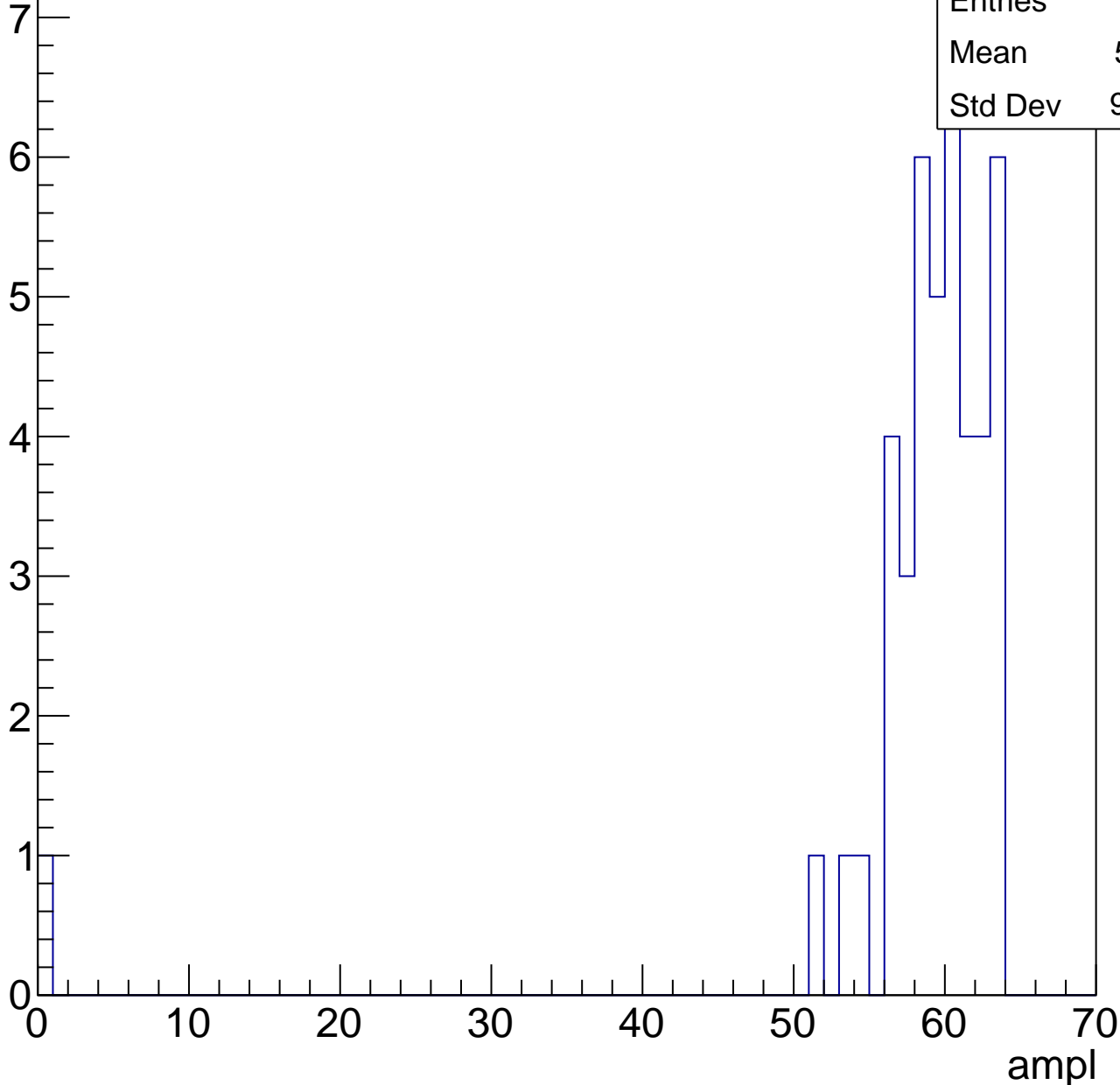


# B1L103S, U2-ch52, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

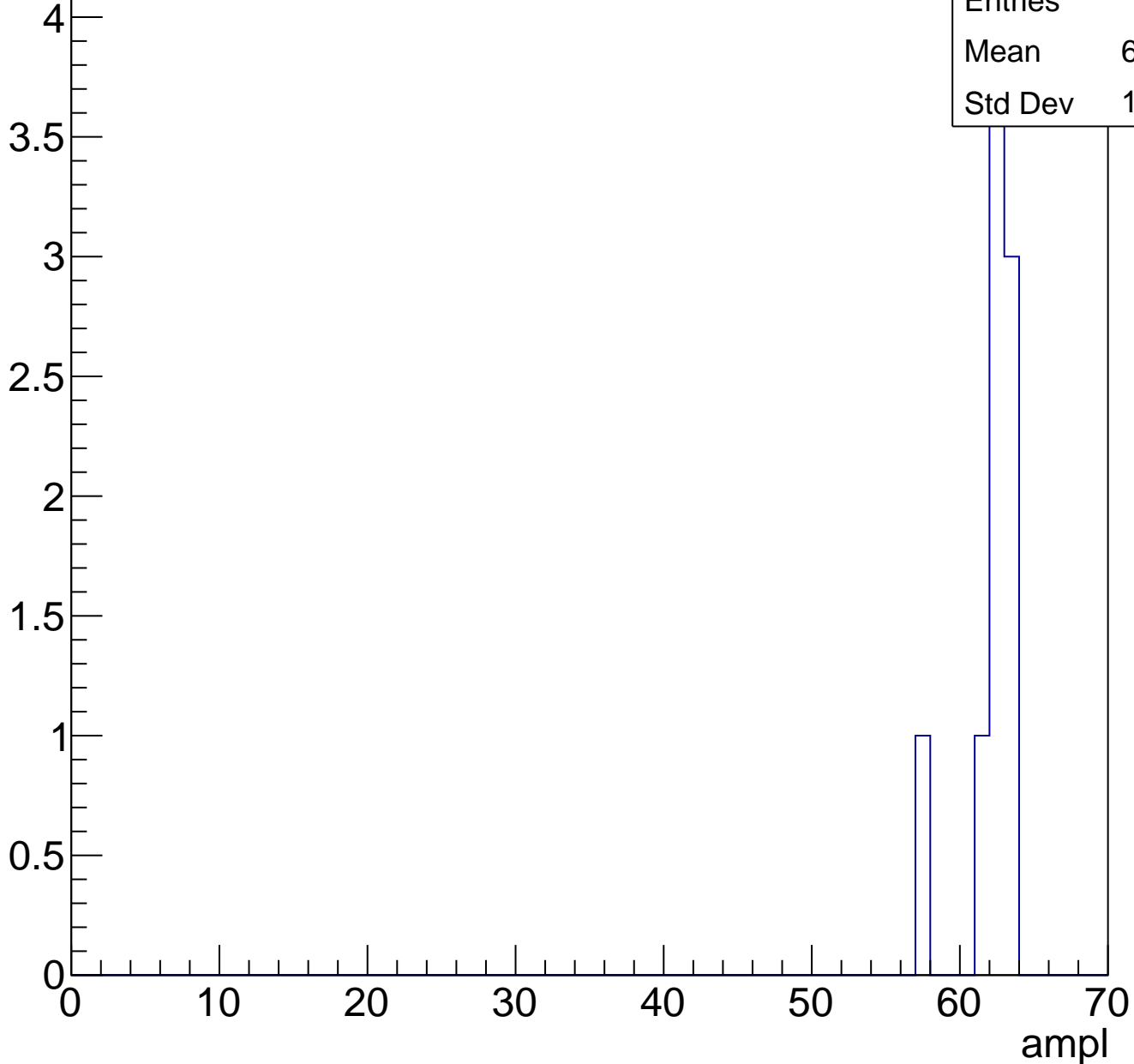
Entries	43
Mean	57.81
Std Dev	9.344



# B1L103S, U2-ch52, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

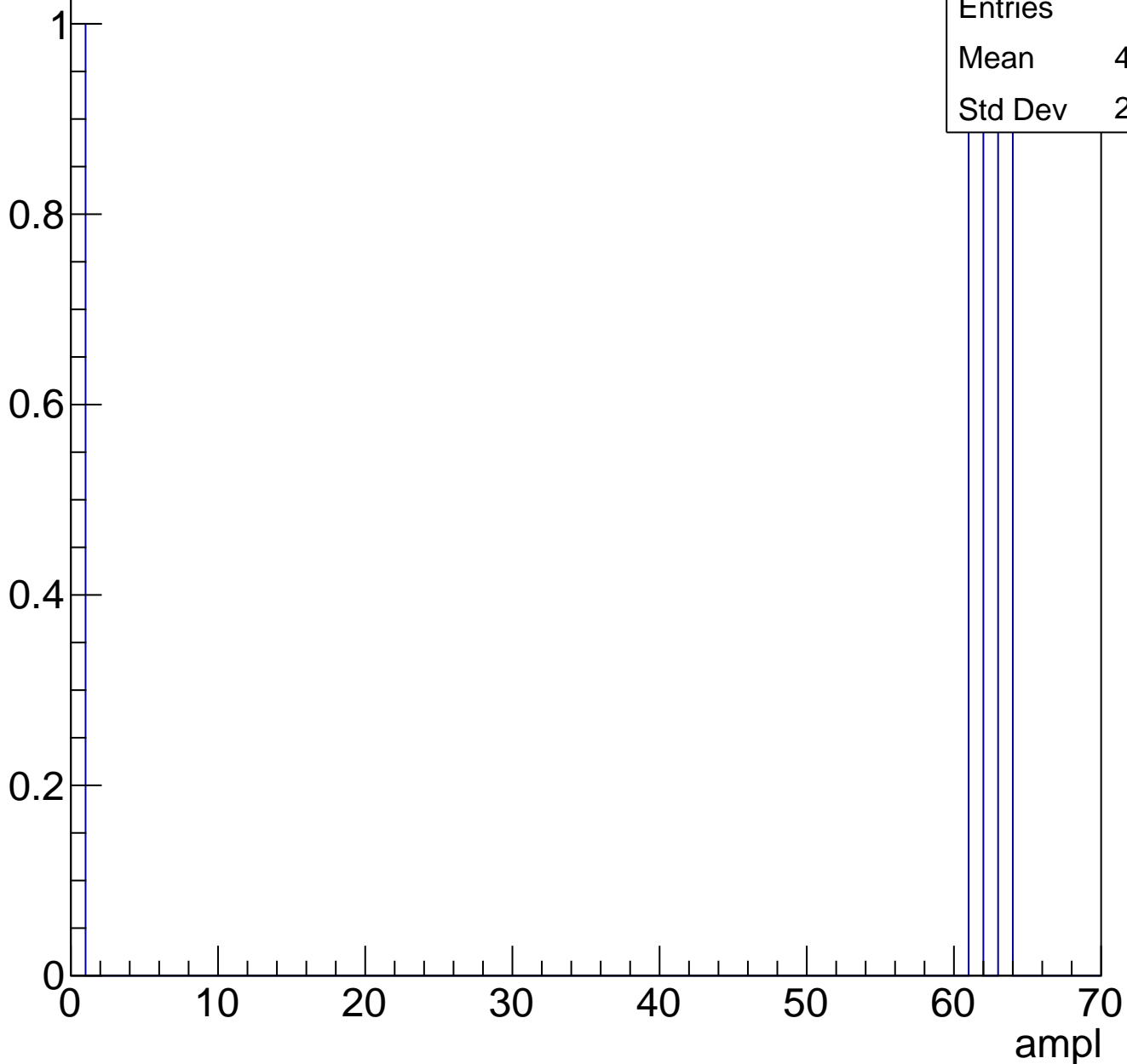




# B1L103S, U2-ch52, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch53, adc0

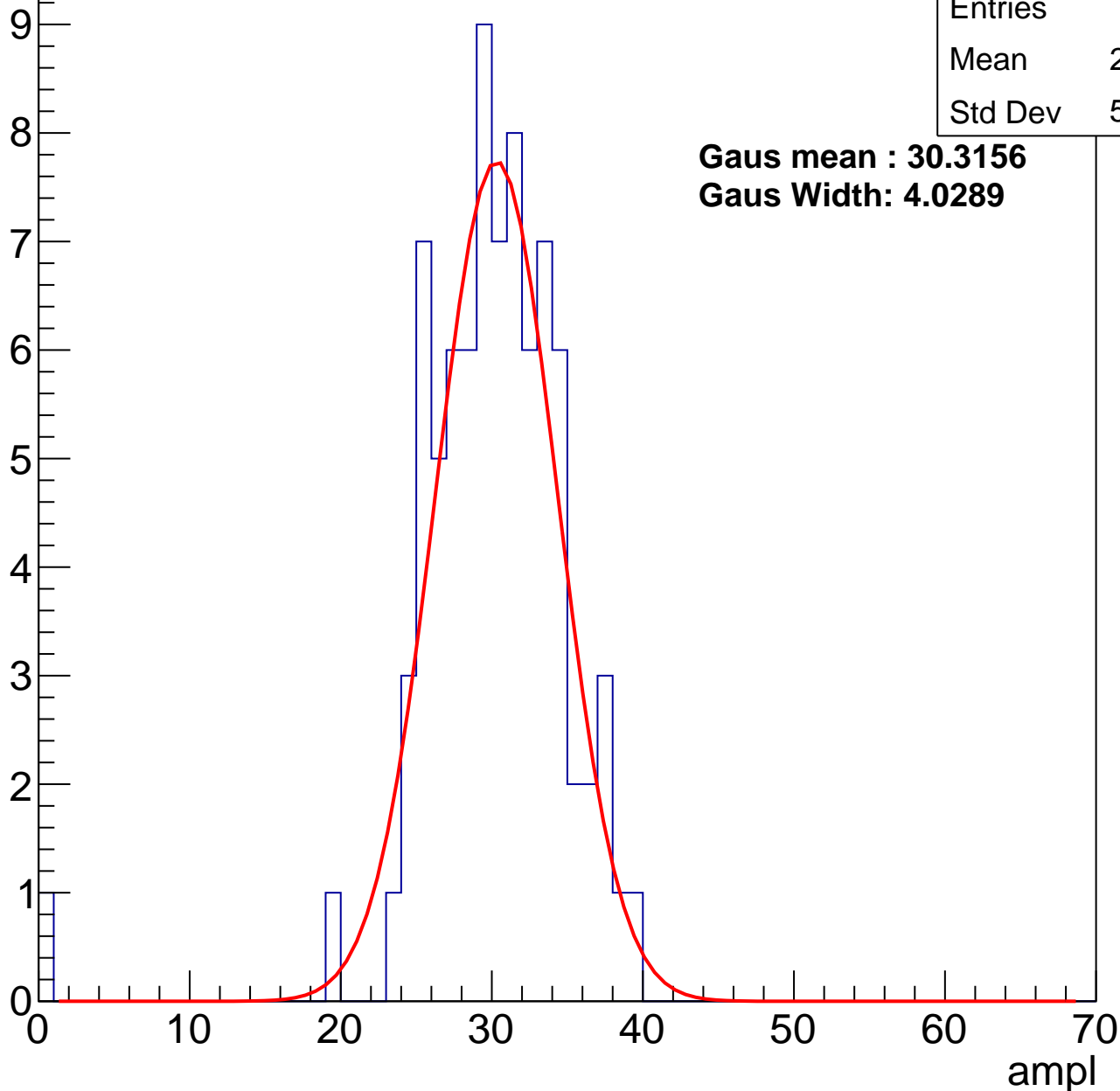
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	82
Mean	29.57
Std Dev	5.073

**Gaus mean : 30.3156**

**Gaus Width: 4.0289**



# B1L103S, U2-ch53, adc1

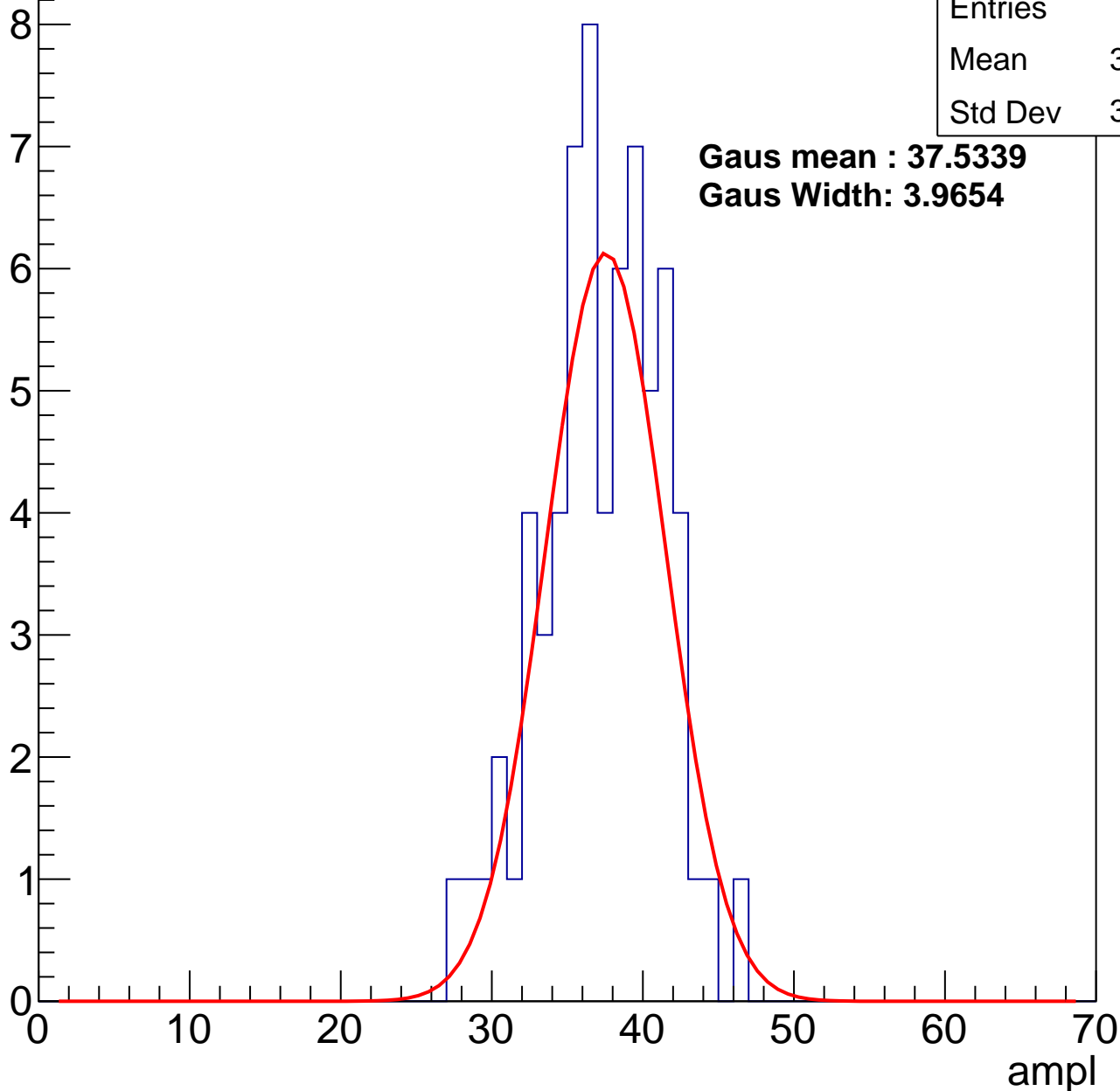
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	36.82
Std Dev	3.936

**Gaus mean : 37.5339**

**Gaus Width: 3.9654**



# B1L103S, U2-ch53, adc2

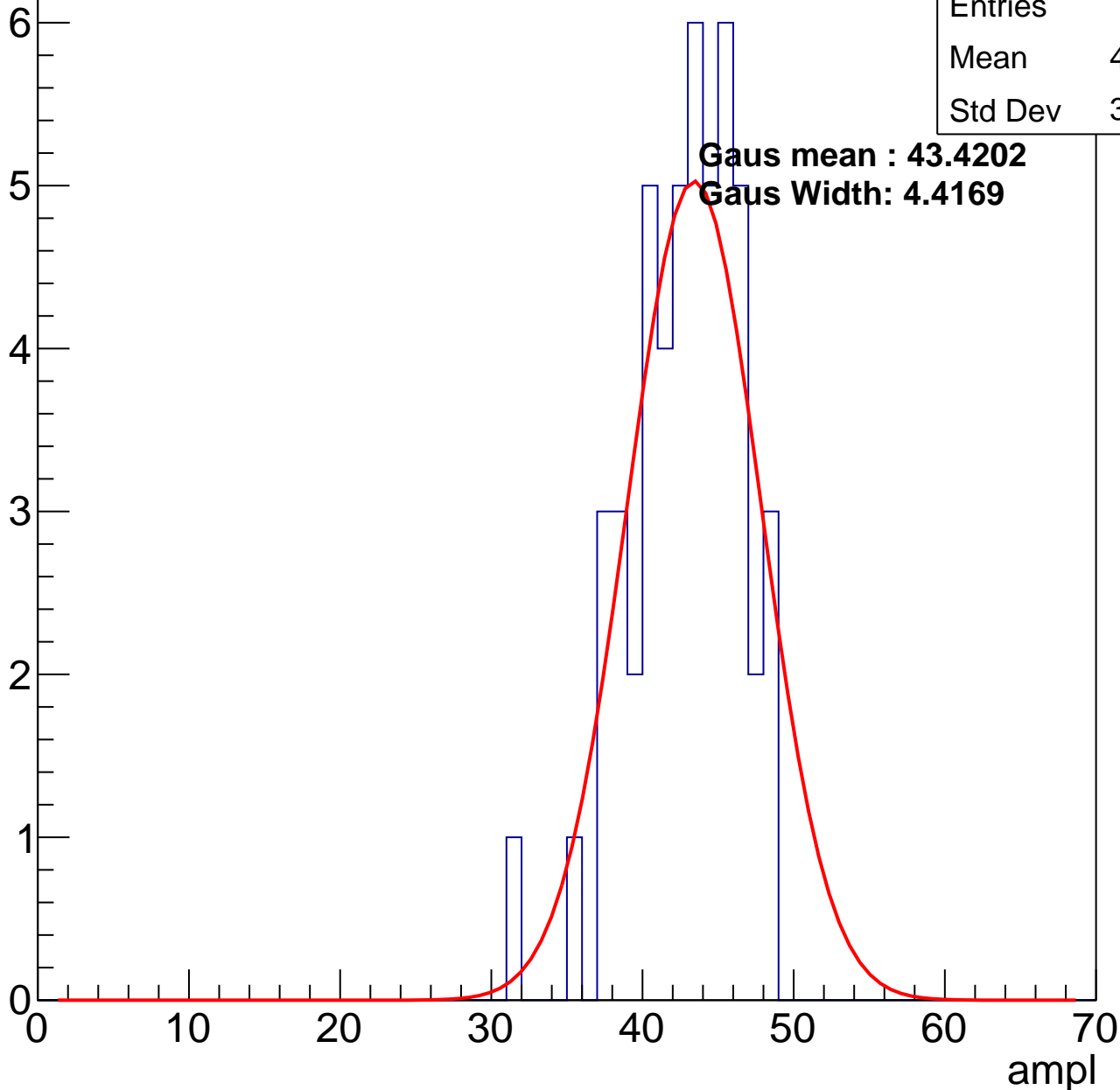
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	42.33
Std Dev	3.563

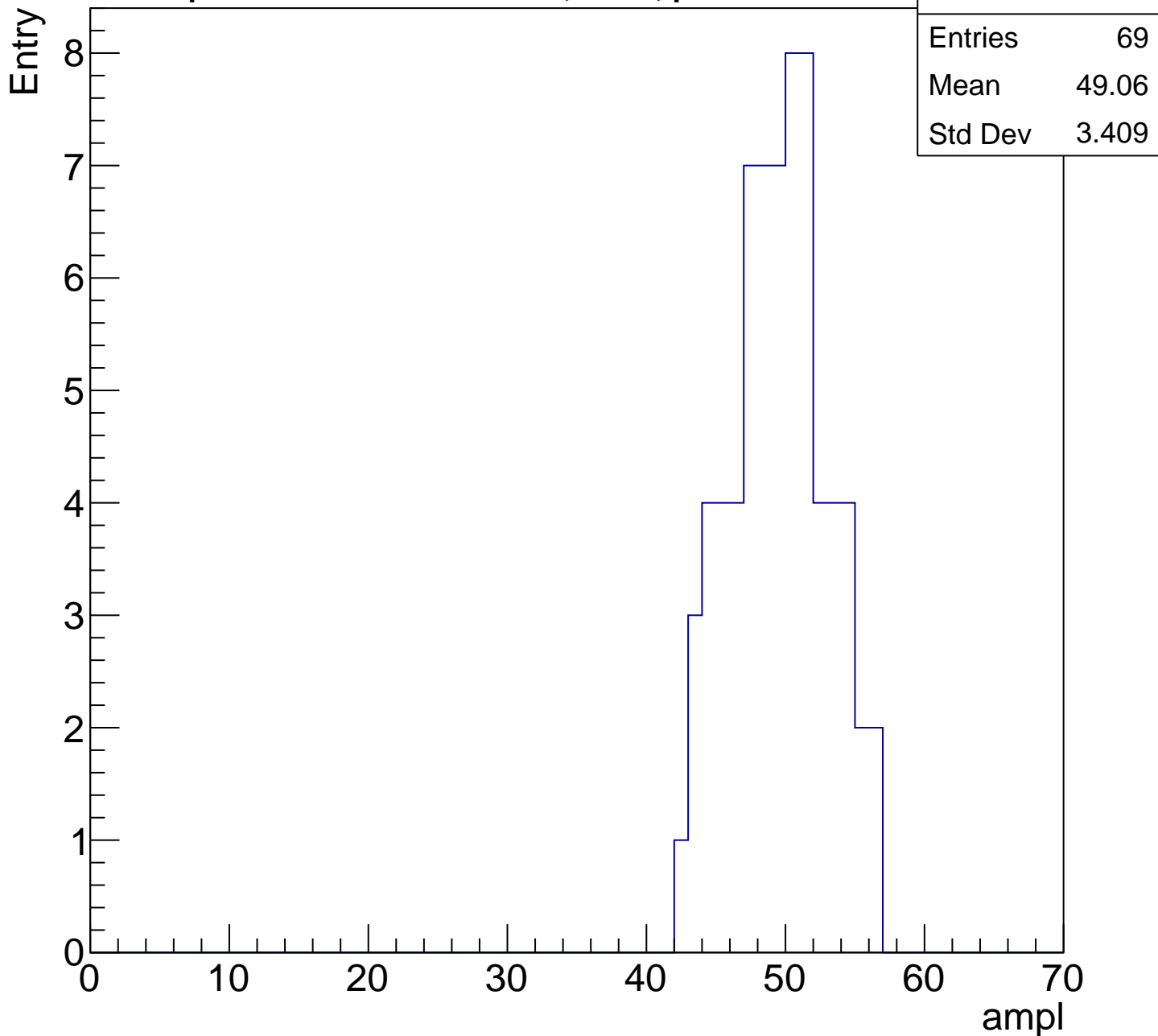
**Gaus mean : 43.4202**

**Gaus Width: 4.4169**



# B1L103S, U2-ch53, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

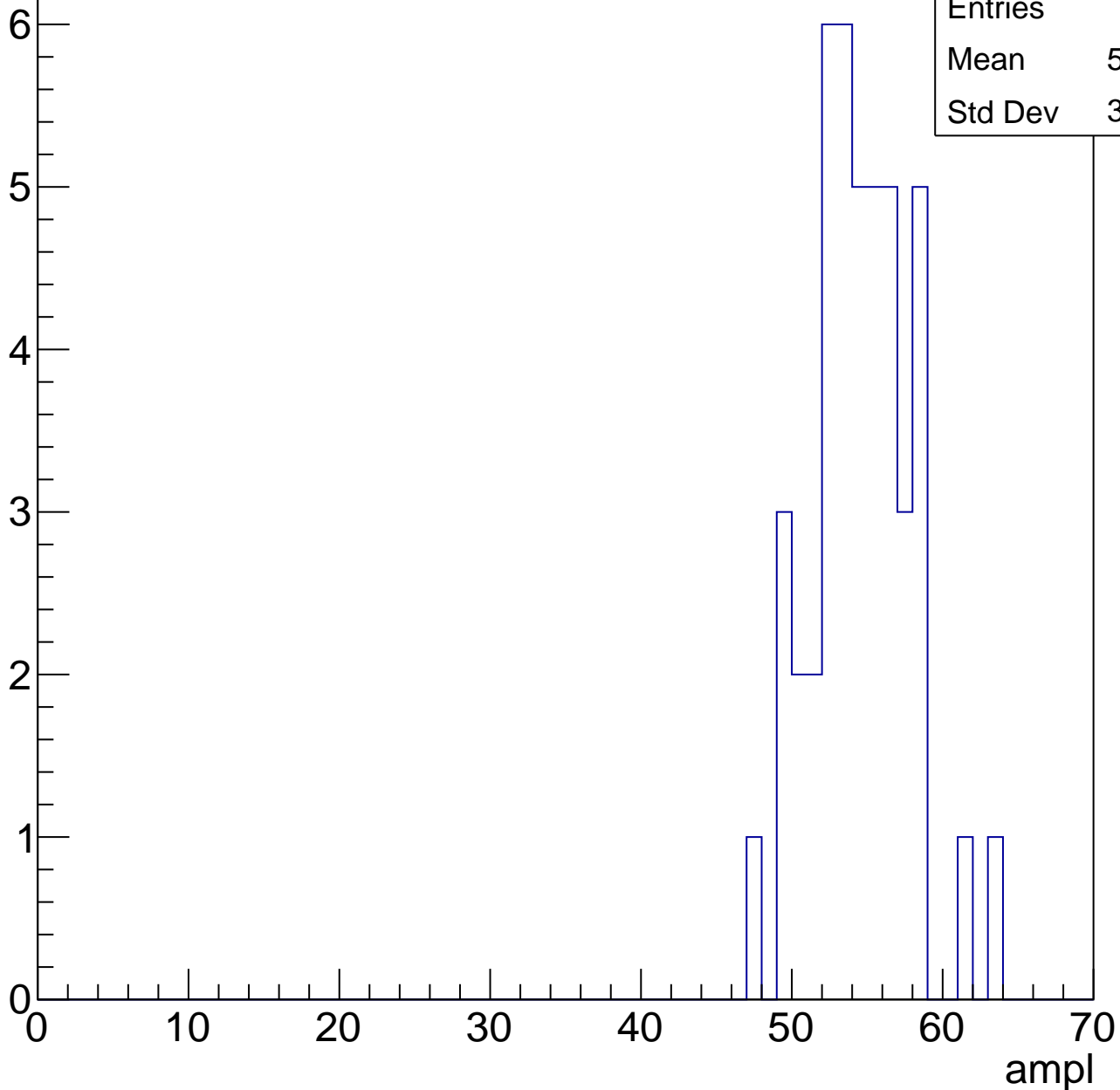


# B1L103S, U2-ch53, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	45
Mean	54.13
Std Dev	3.215

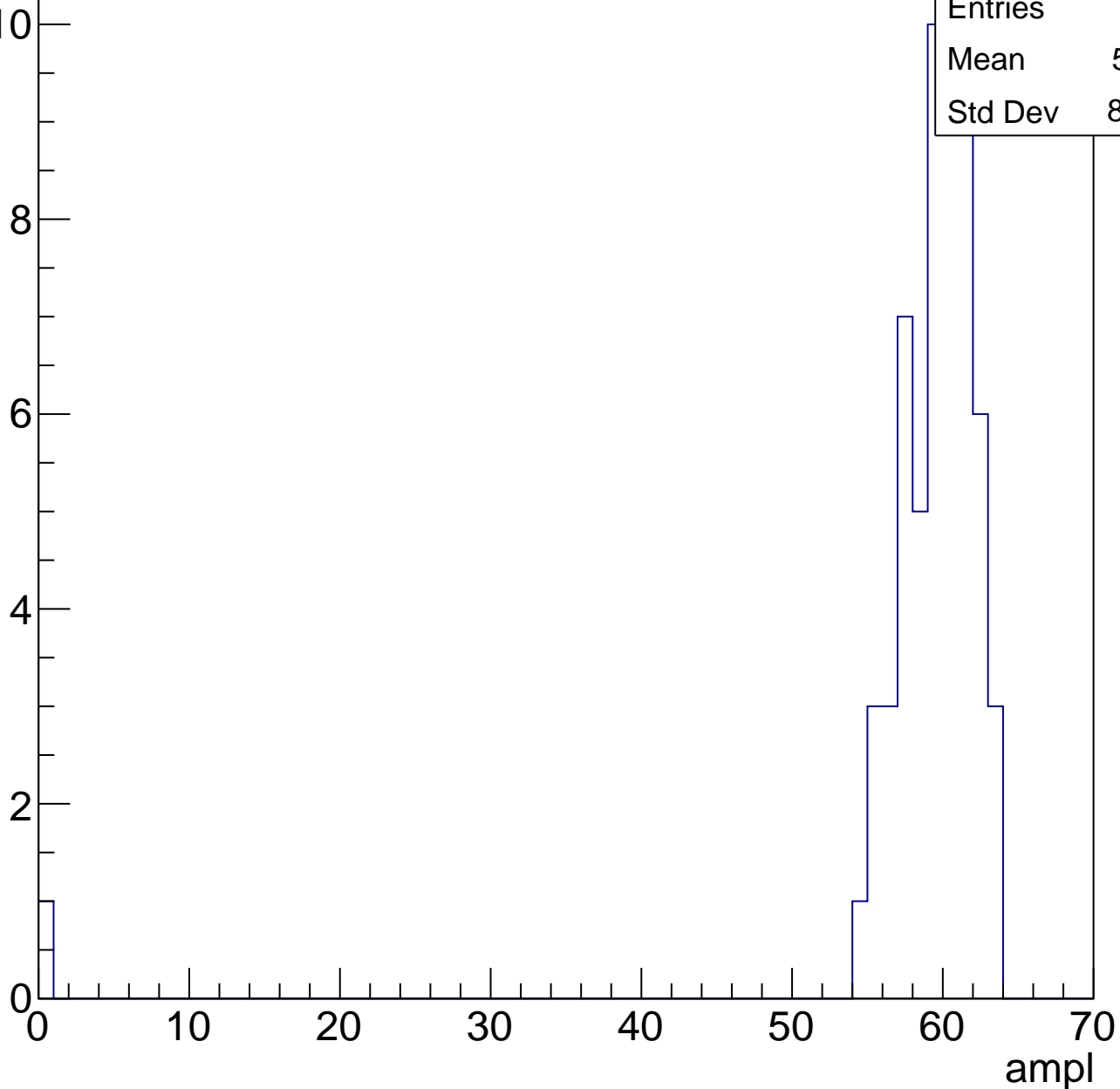


# B1L103S, U2-ch53, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	58.21
Std Dev	8.015

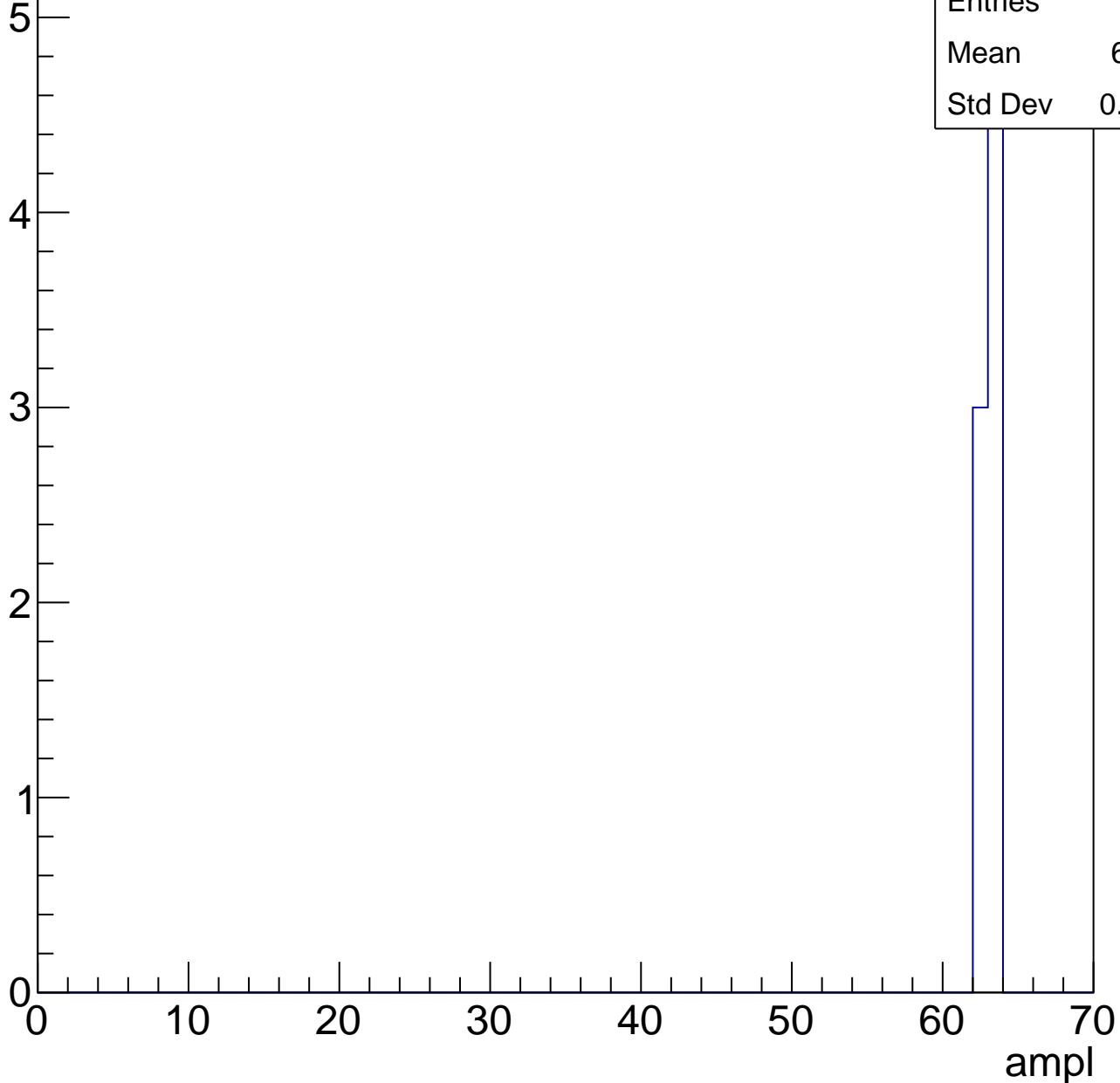


# B1L103S, U2-ch53, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	8
Mean	62.62
Std Dev	0.4841

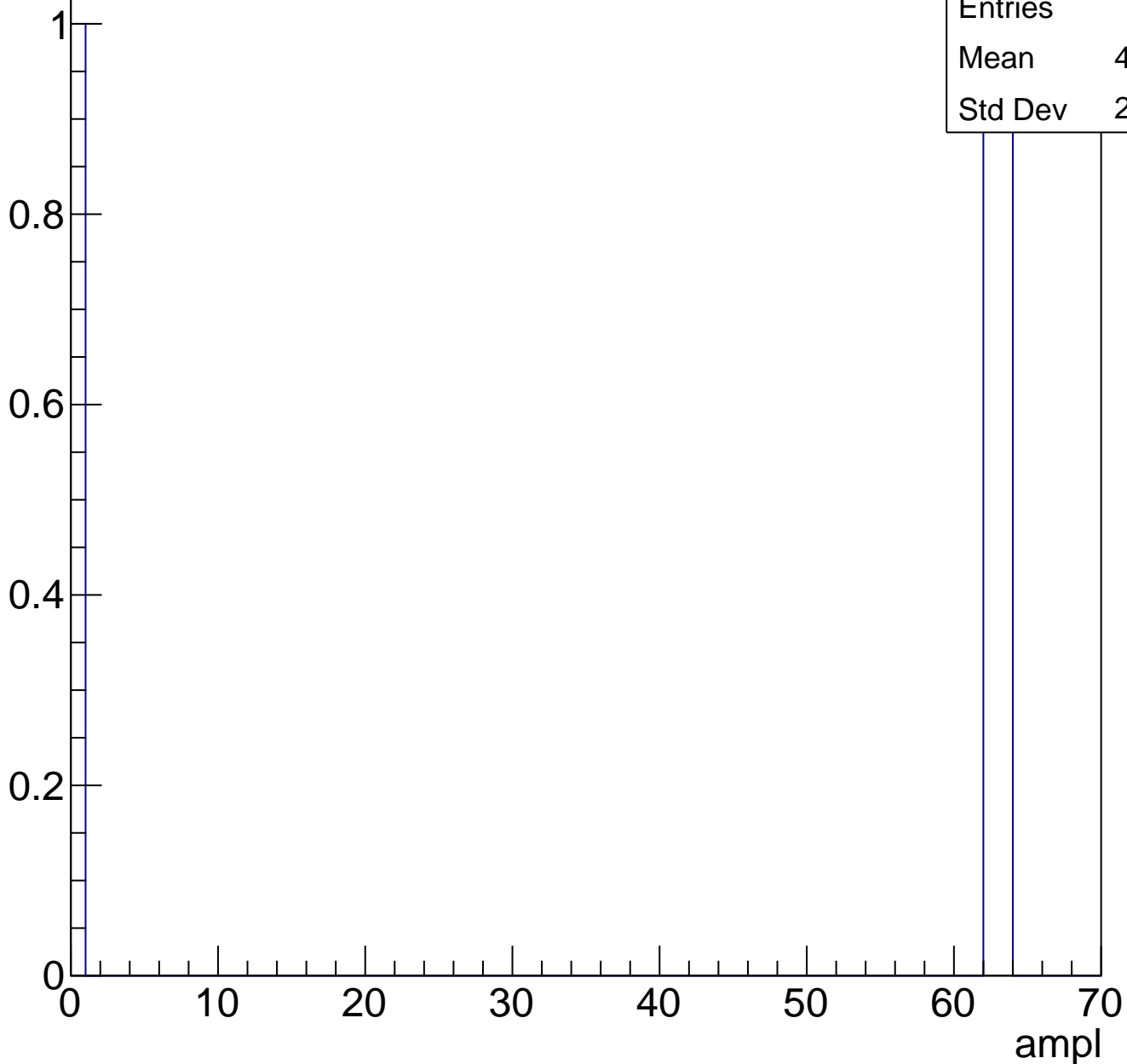




# B1L103S, U2-ch53, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch54, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	79
Mean	29.43
Std Dev	3.961

**Gaus mean : 29.4731**

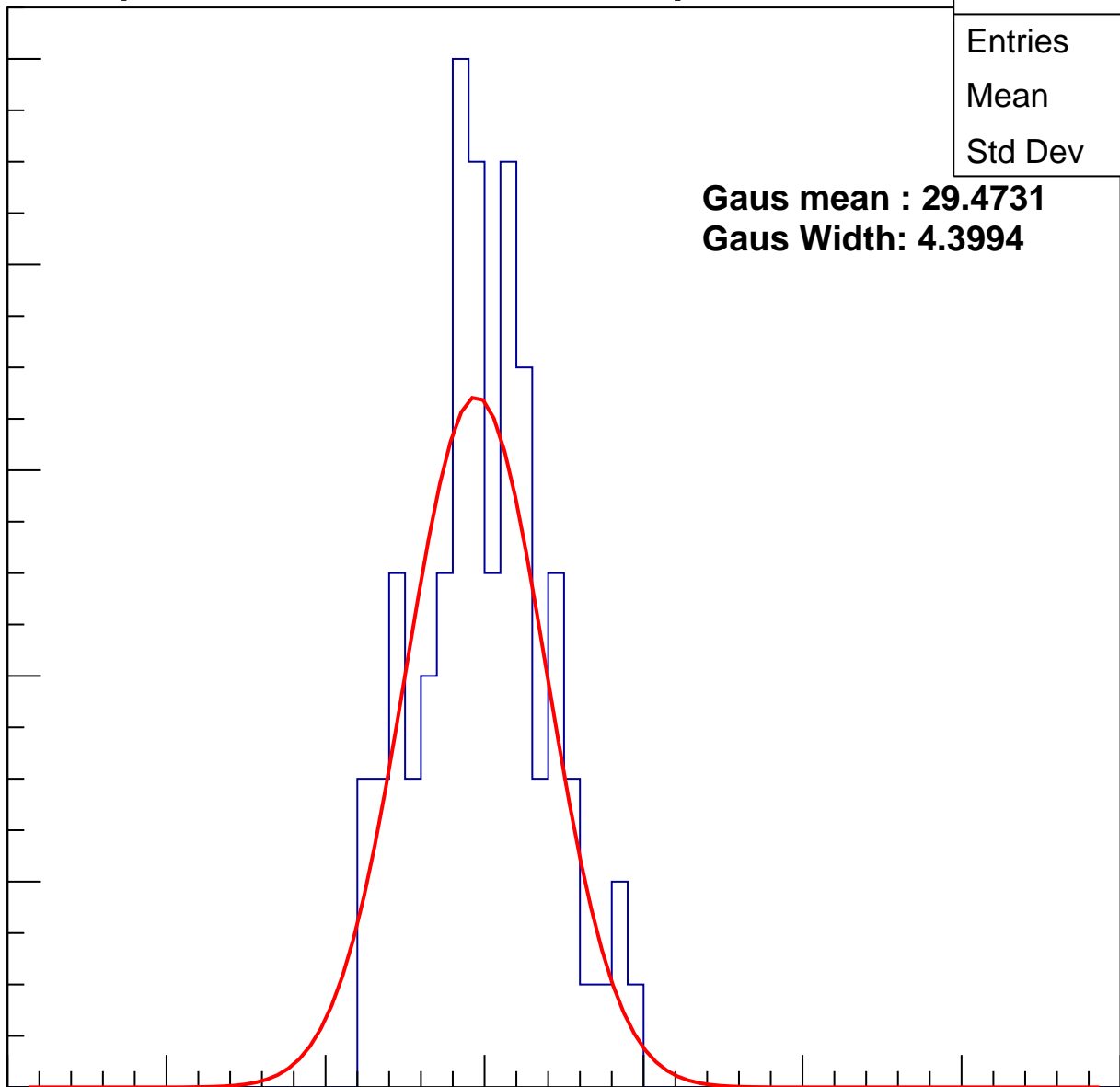
**Gaus Width: 4.3994**

Entry

10  
8  
6  
4  
2  
0

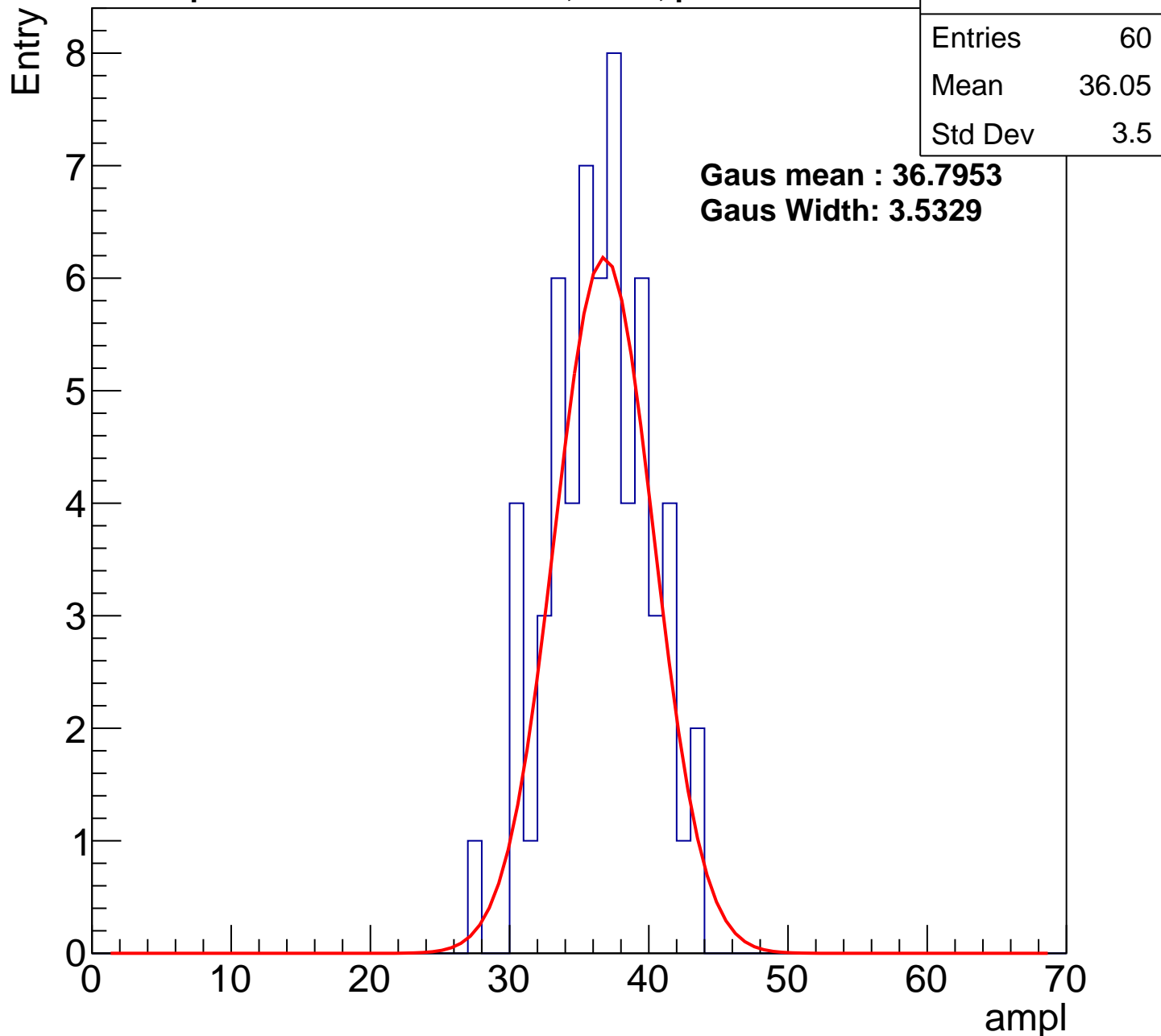
ampl

0 10 20 30 40 50 60 70



# B1L103S, U2-ch54, adc1

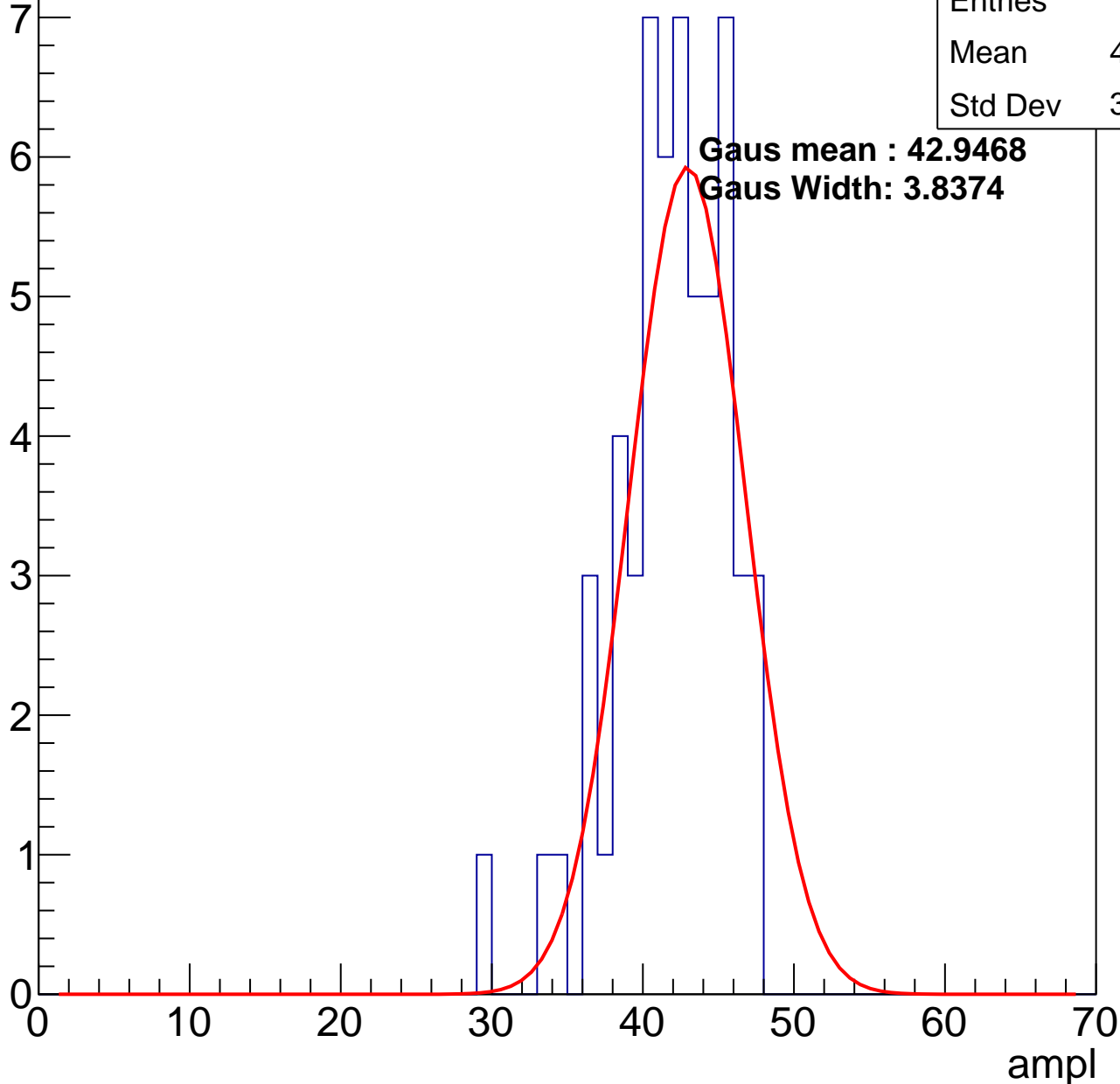
calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U2-ch54, adc2

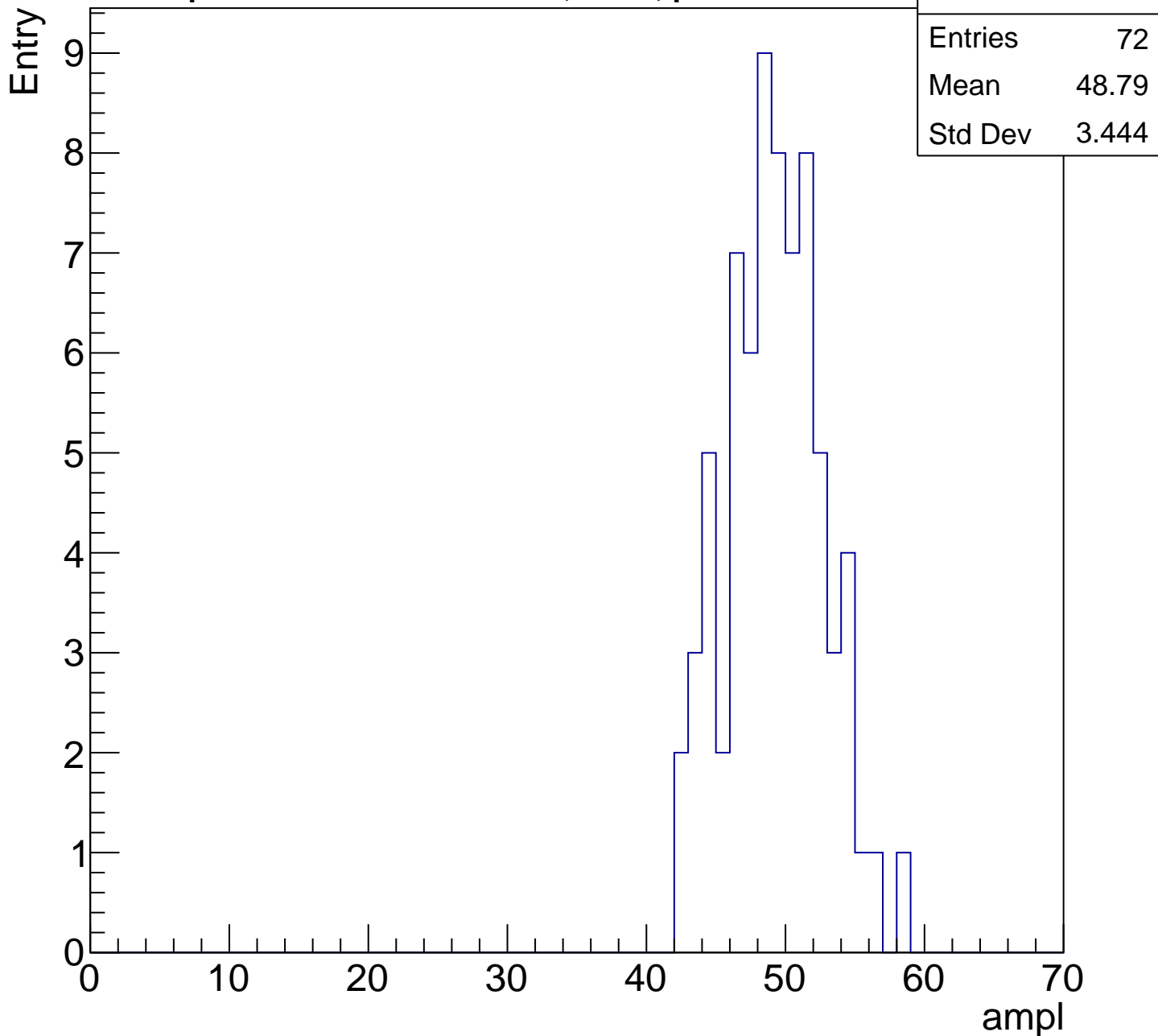
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



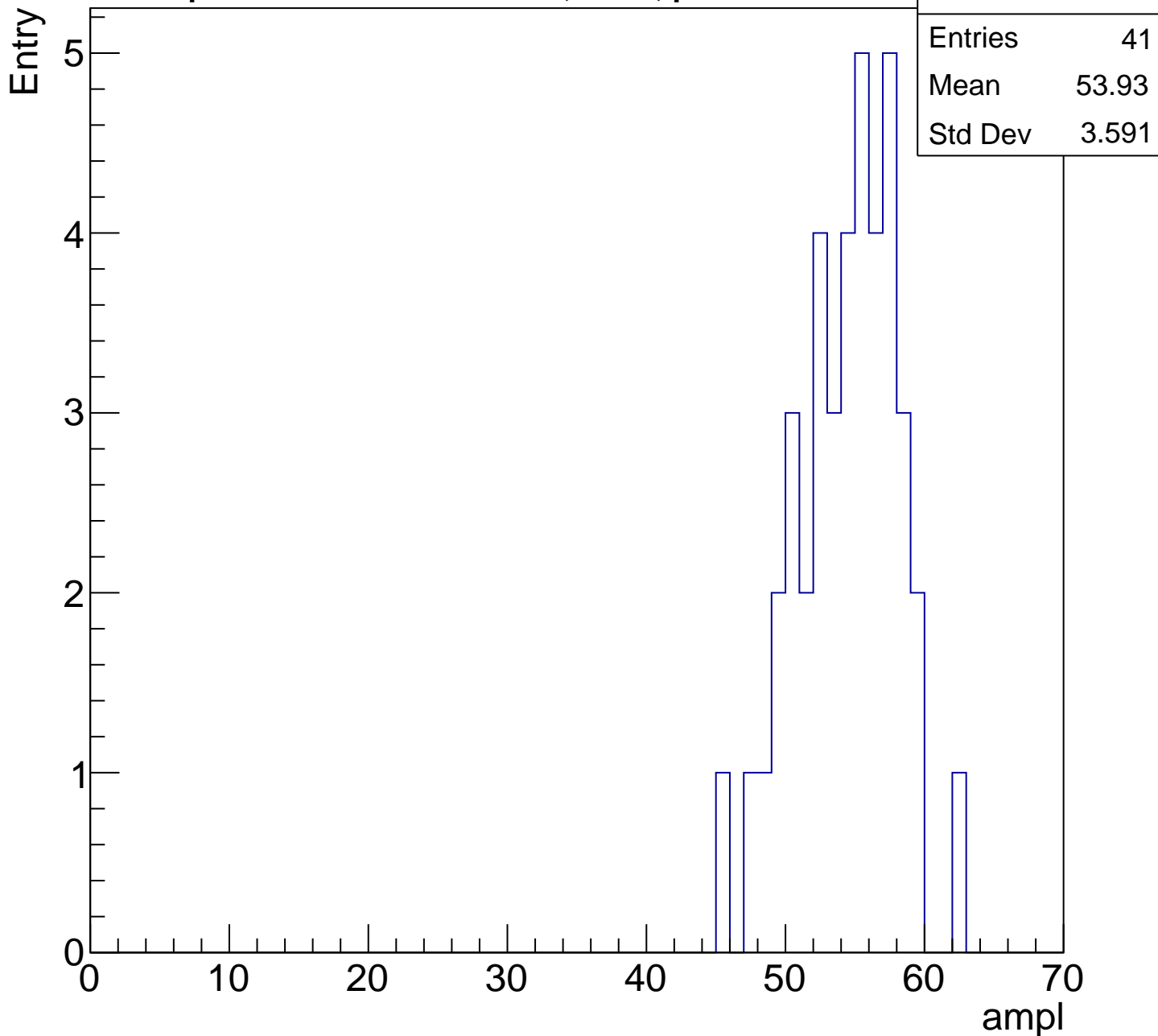
# B1L103S, U2-ch54, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U2-ch54, adc4

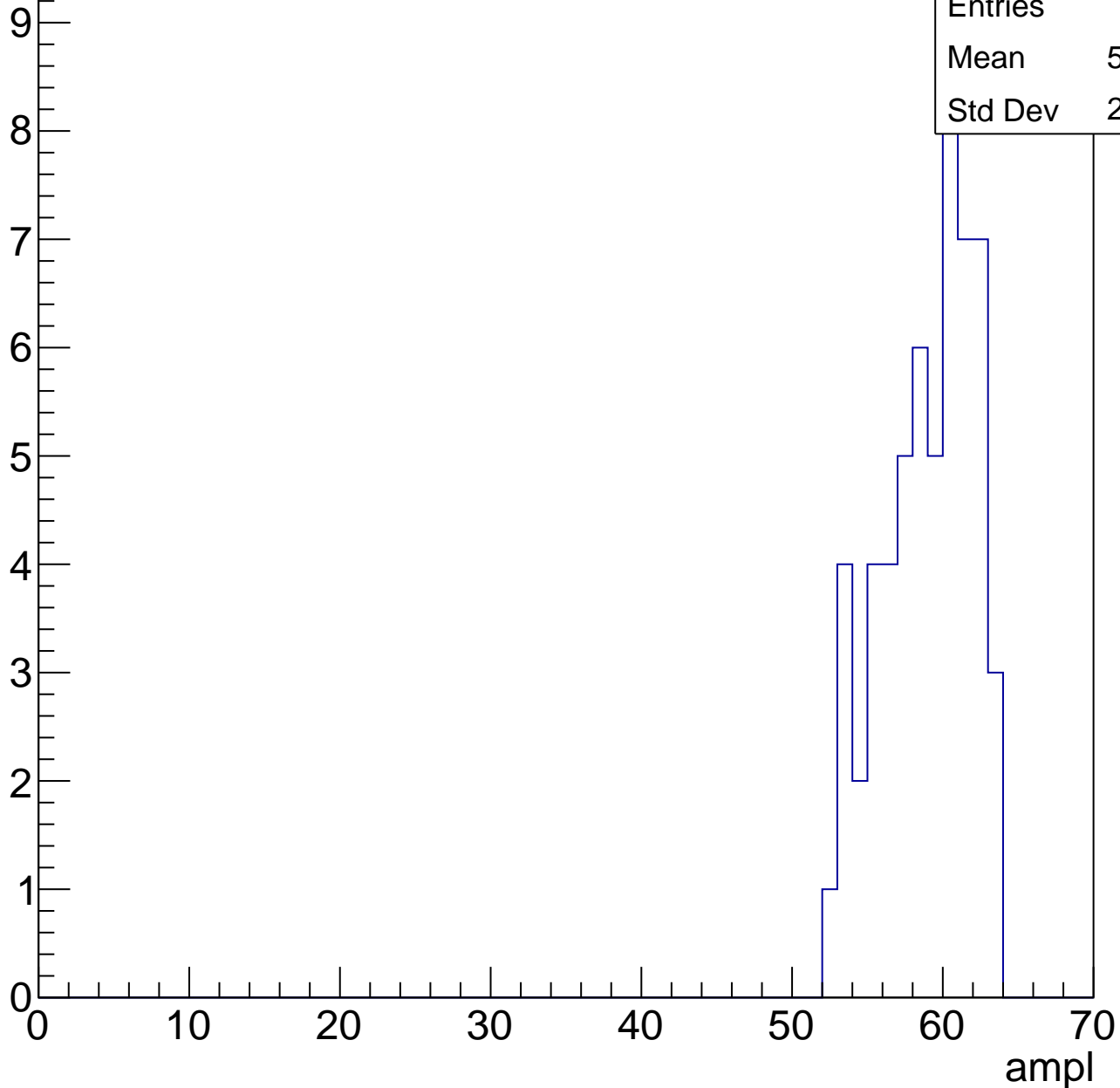
calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U2-ch54, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

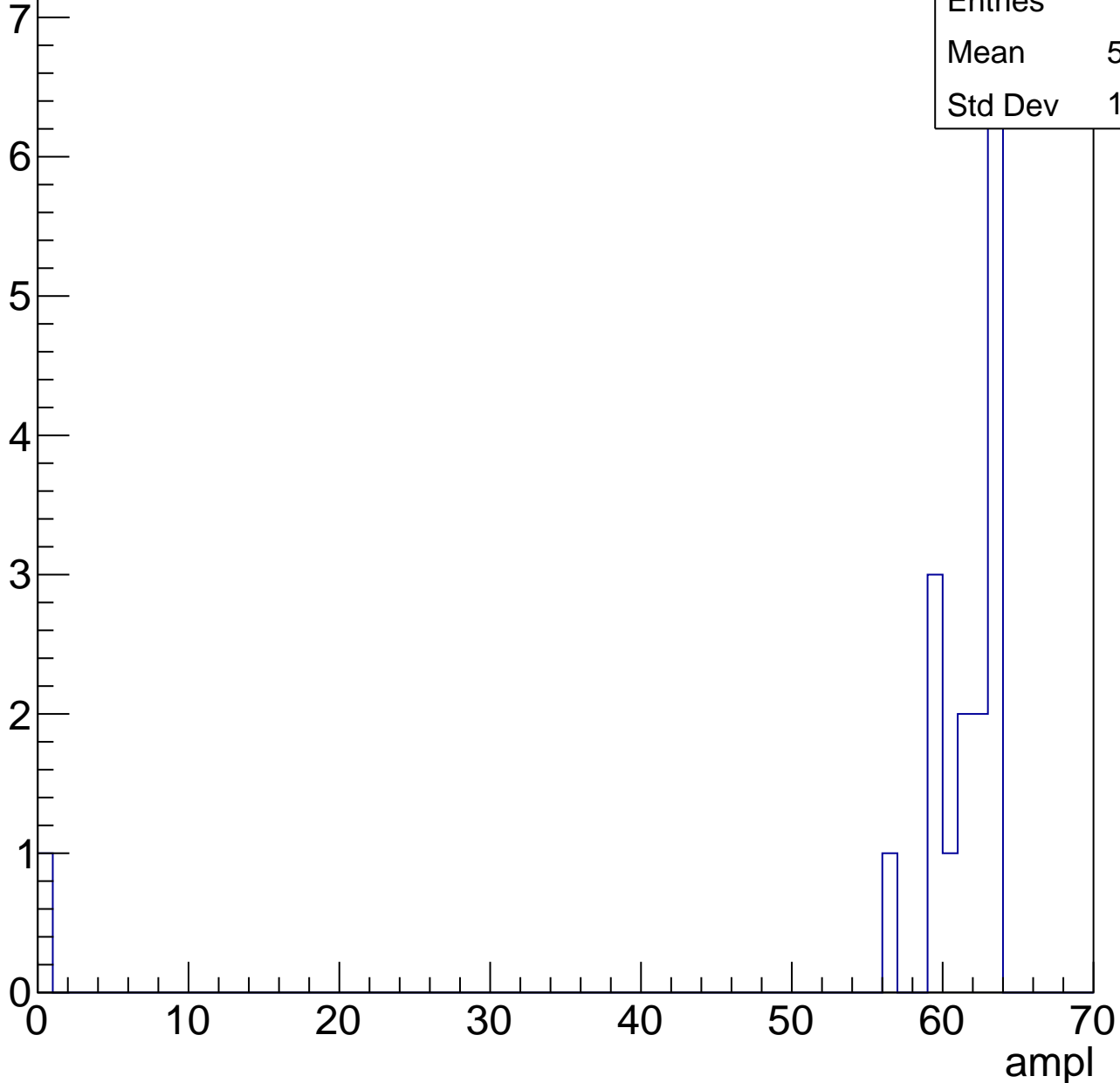


# B1L103S, U2-ch54, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	17
Mean	57.65
Std Dev	14.55

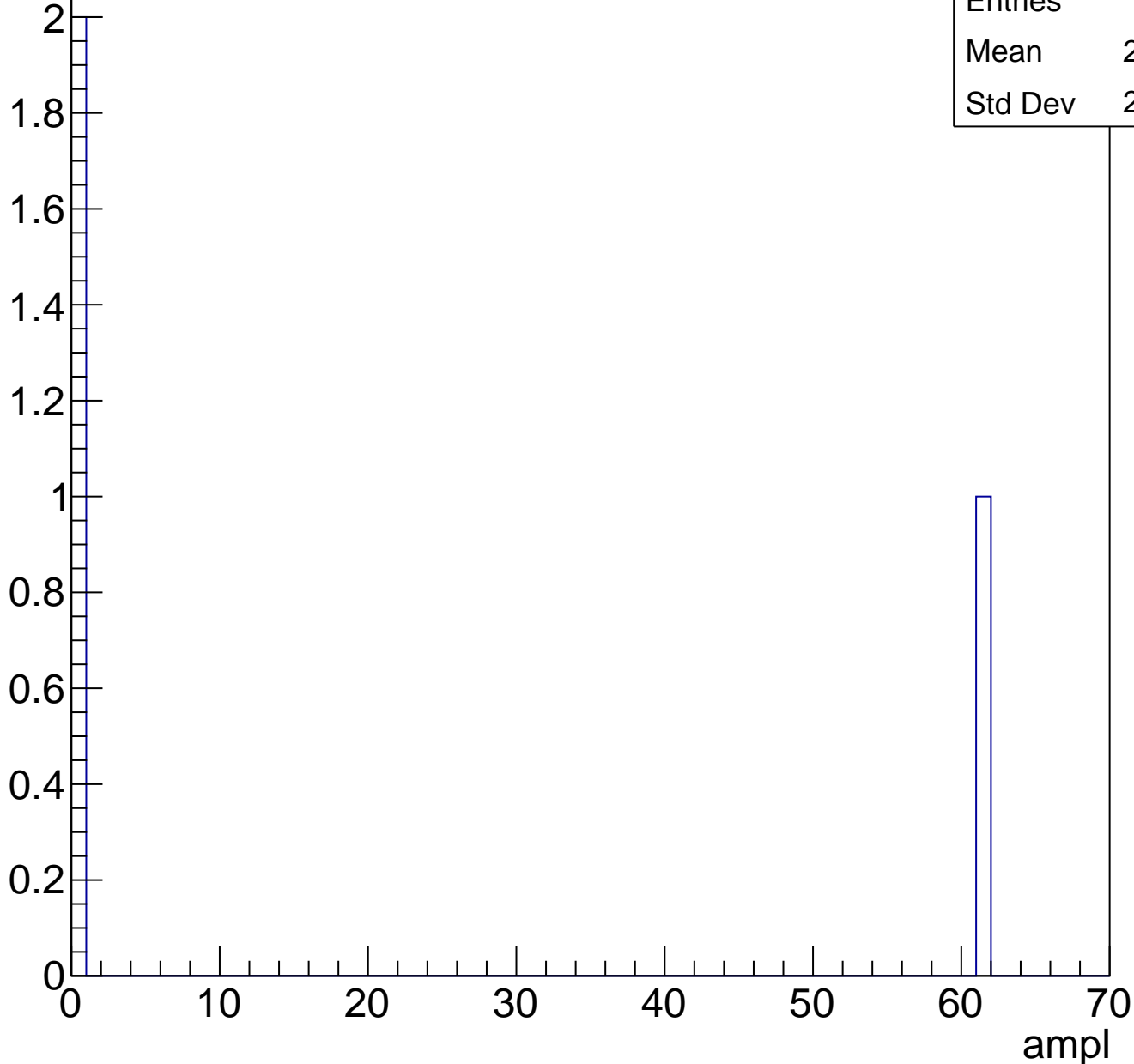




# B1L103S, U2-ch54, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch55, adc0

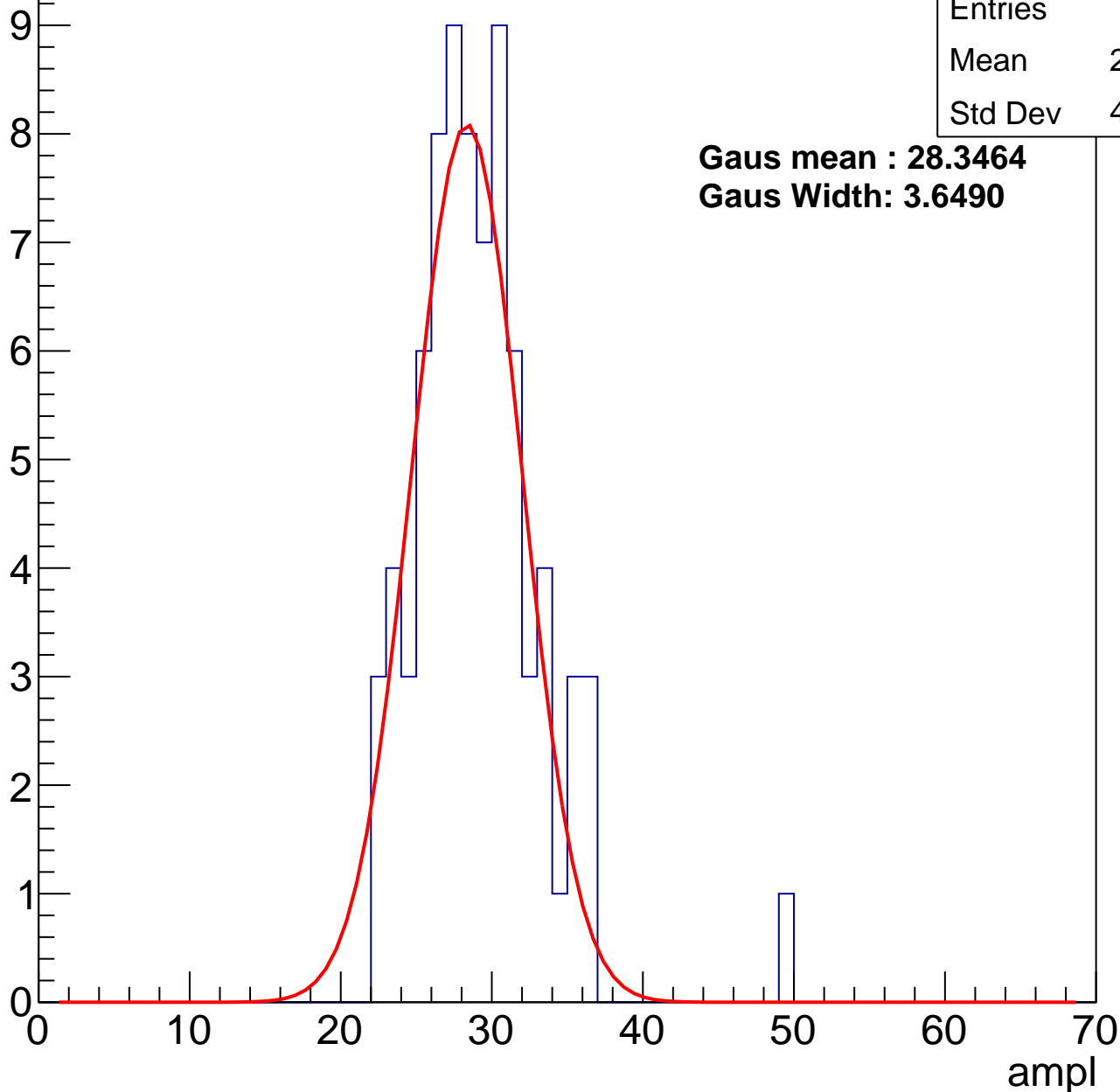
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	28.69
Std Dev	4.198

**Gaus mean : 28.3464**

**Gaus Width: 3.6490**



# B1L103S, U2-ch55, adc1

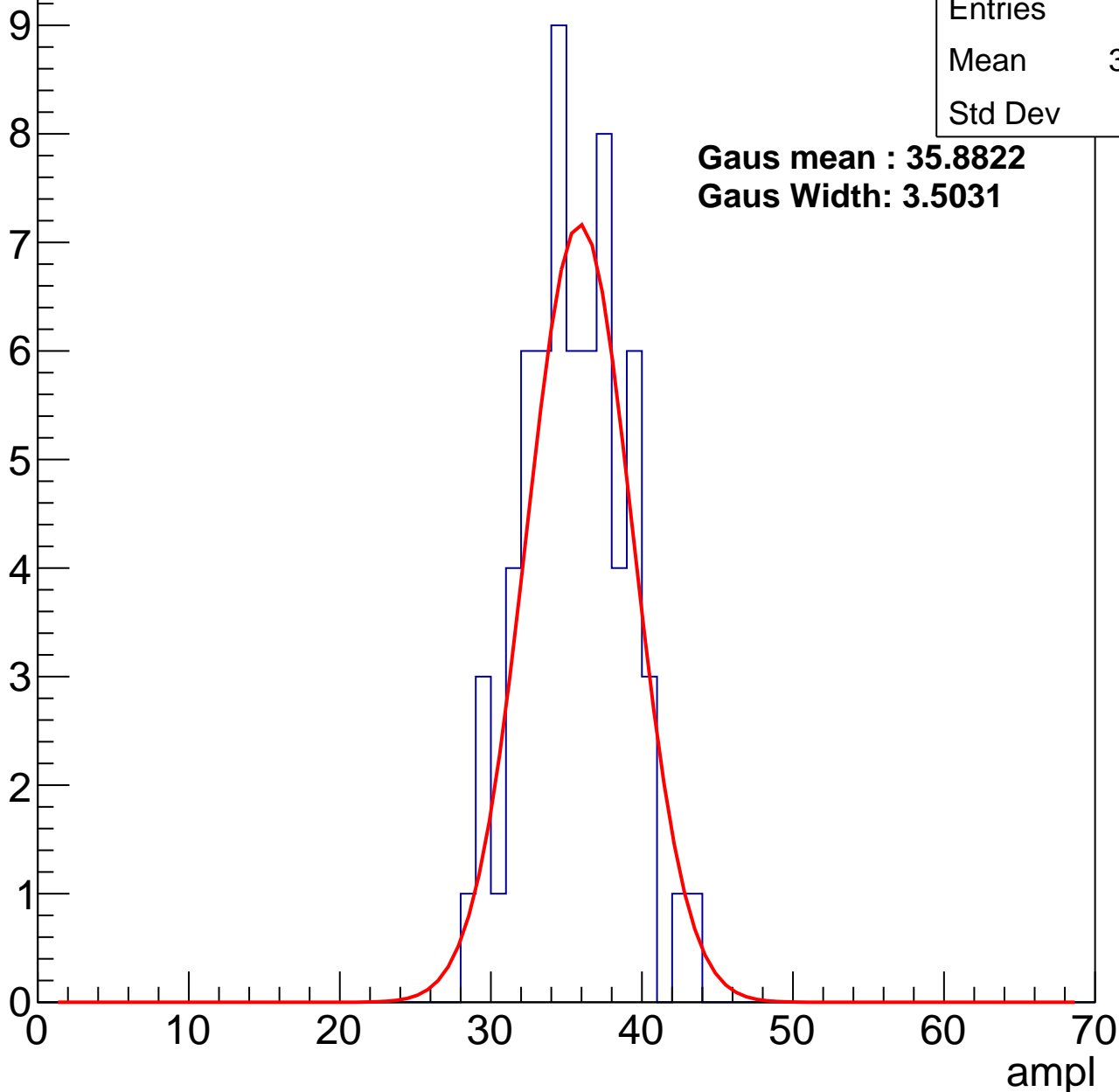
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	35.05
Std Dev	3.26

**Gaus mean : 35.8822**

**Gaus Width: 3.5031**



# B1L103S, U2-ch55, adc2

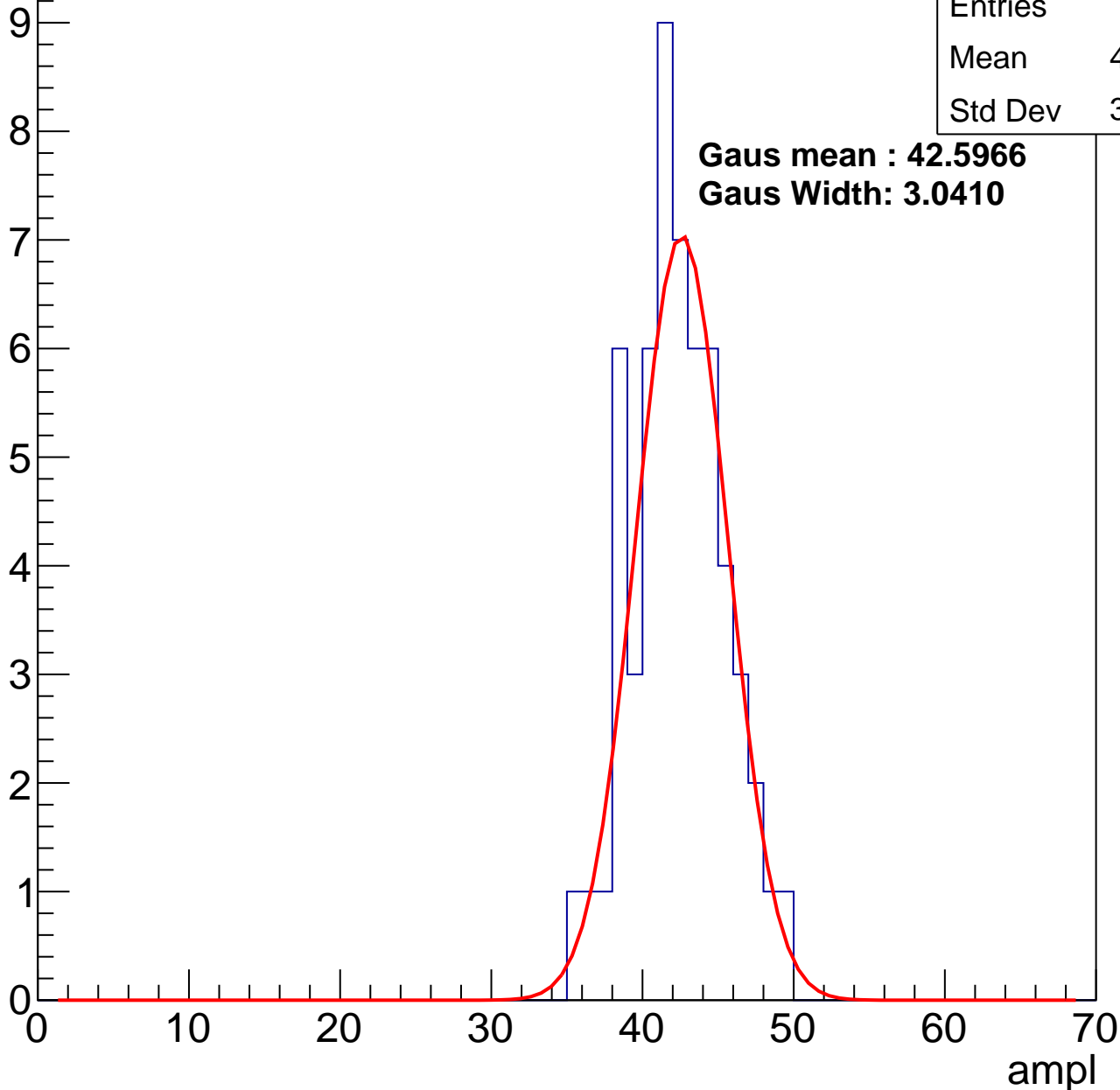
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	41.88
Std Dev	3.003

**Gaus mean : 42.5966**

**Gaus Width: 3.0410**

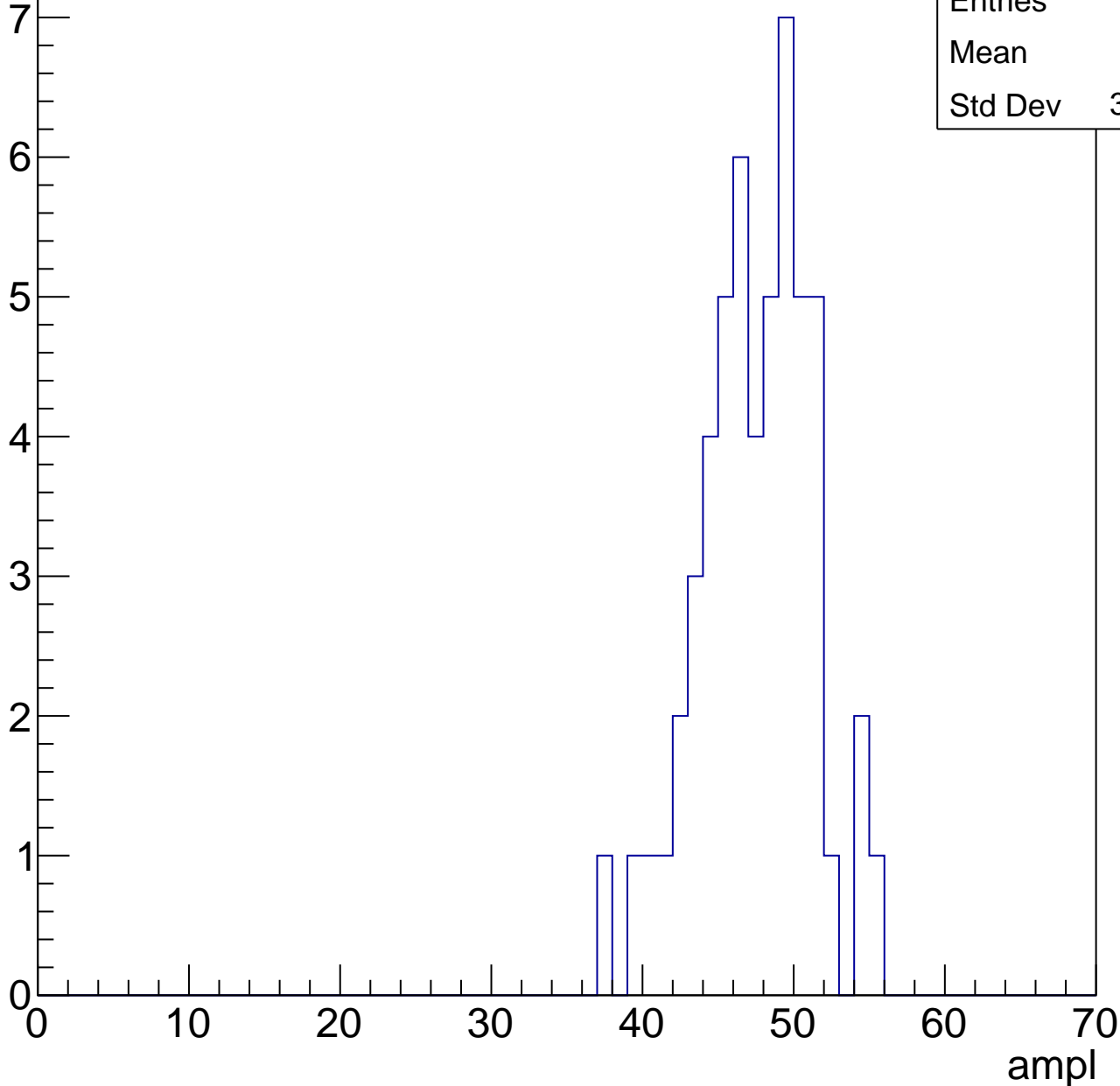


# B1L103S, U2-ch55, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

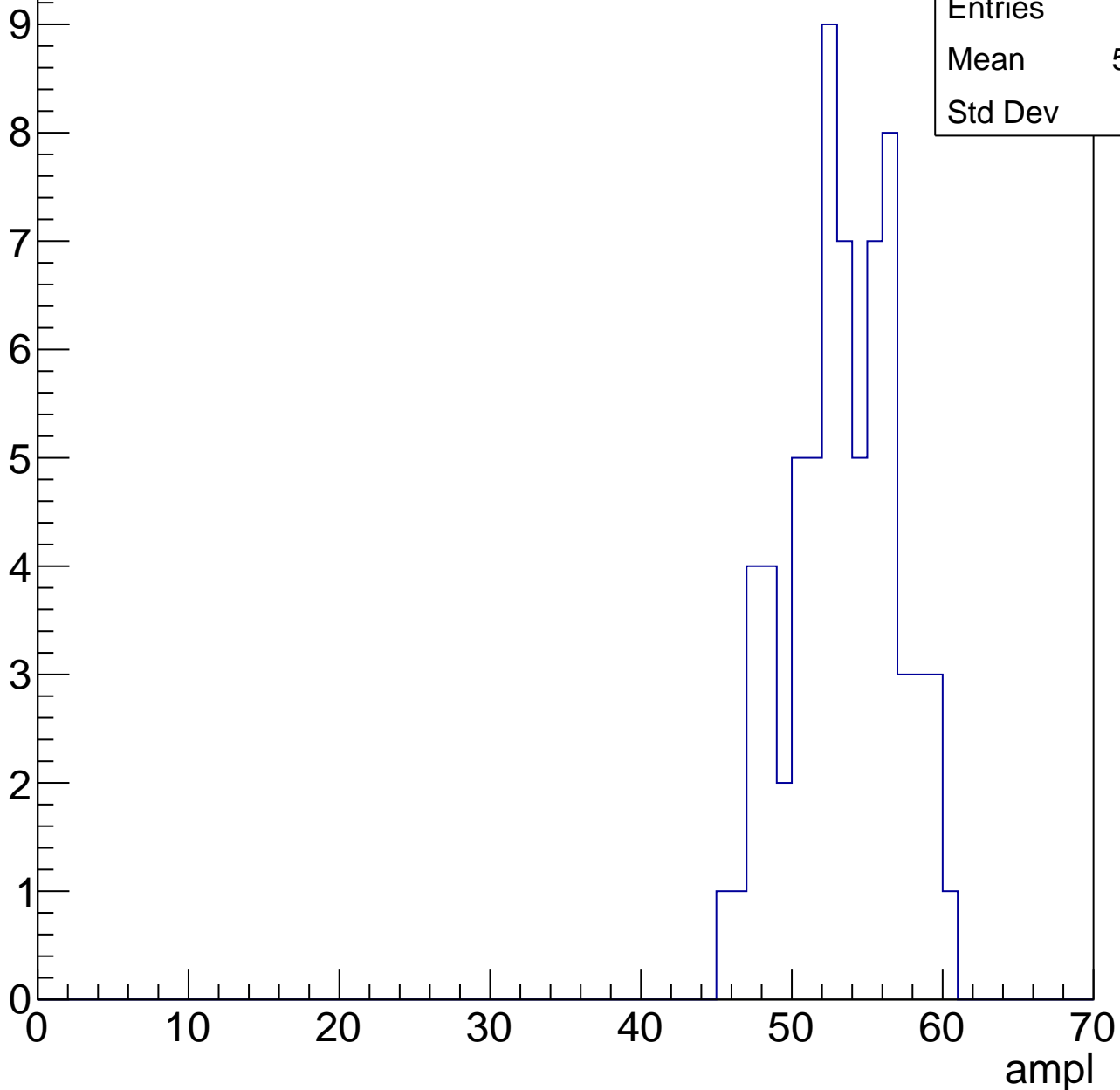
Entries	54
Mean	47
Std Dev	3.737



# B1L103S, U2-ch55, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



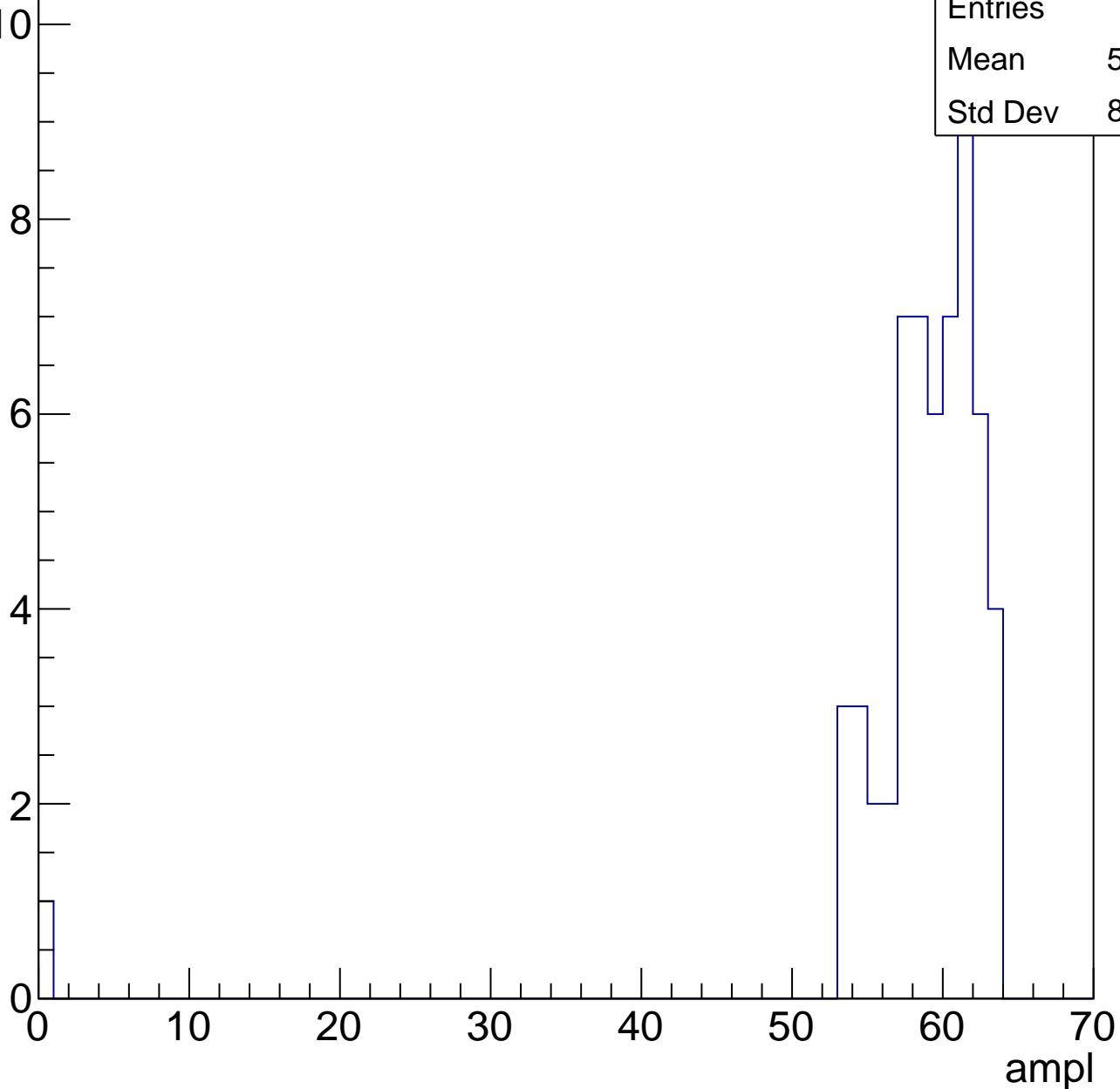
Entries	68
Mean	52.91
Std Dev	3.53

# B1L103S, U2-ch55, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	57.86
Std Dev	8.136

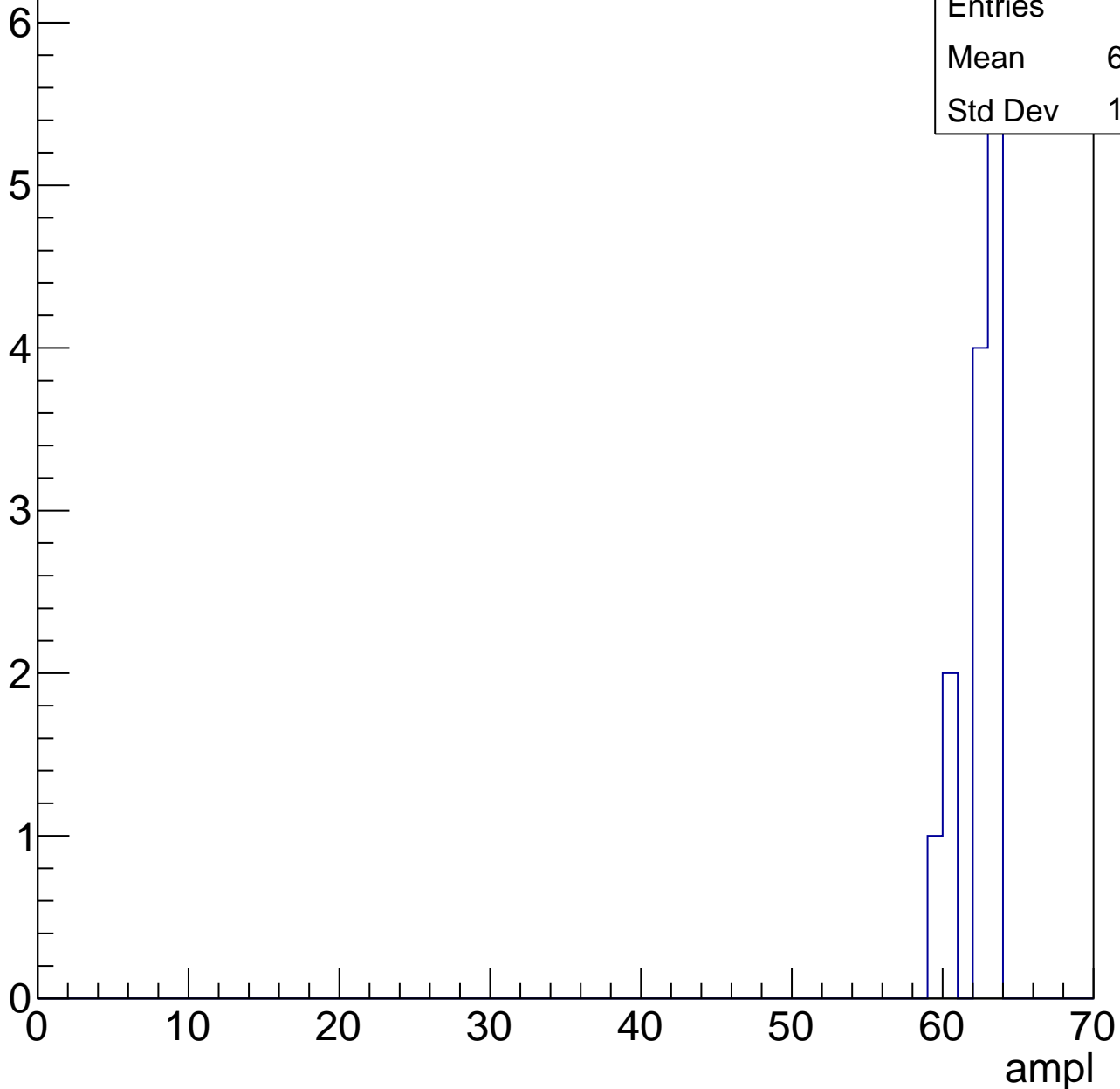


# B1L103S, U2-ch55, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	13
Mean	61.92
Std Dev	1.328





# B1L103S, U2-ch55, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	11
Std Dev	11

# B1L103S, U2-ch56, adc0

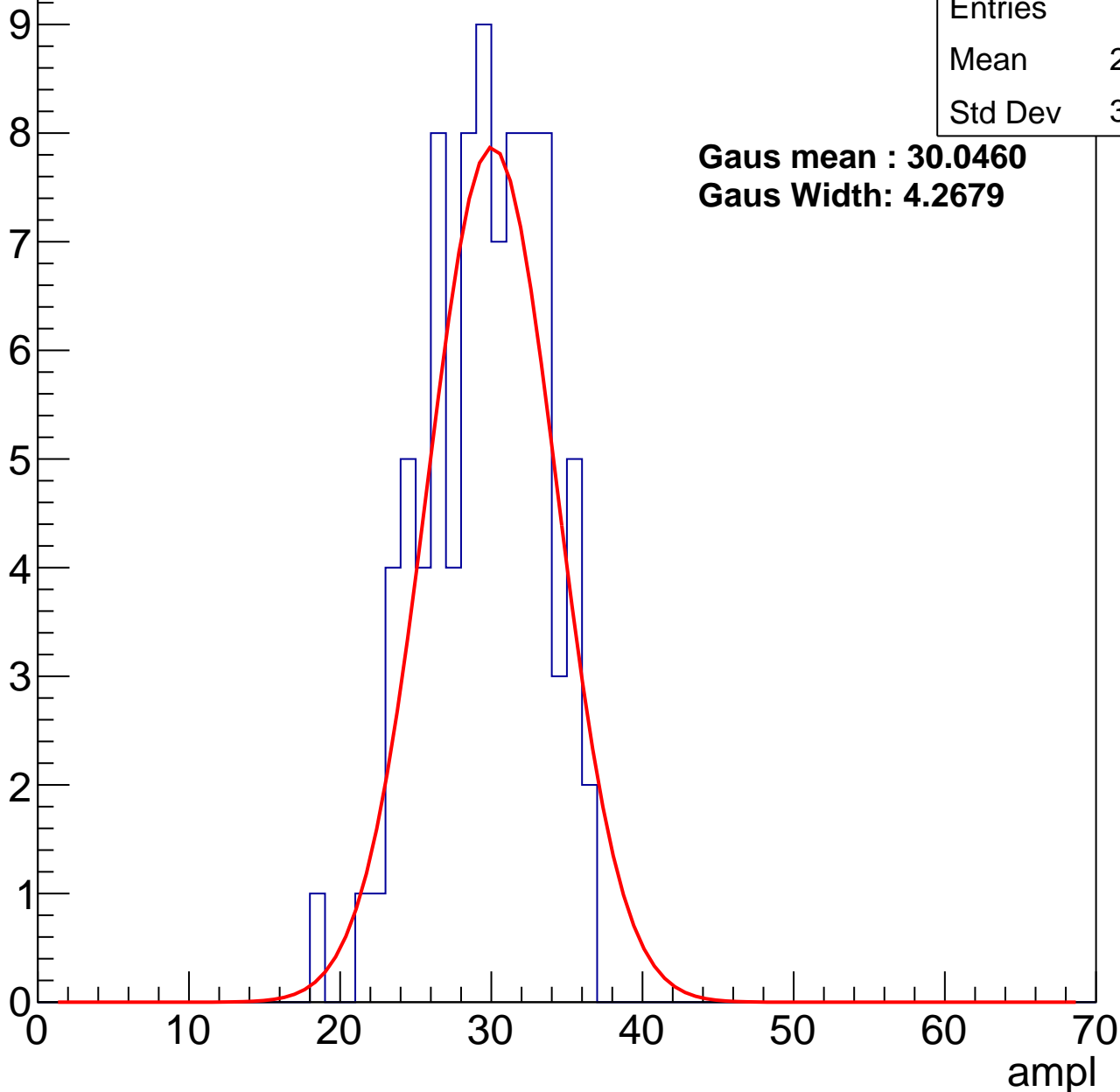
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	86
Mean	29.08
Std Dev	3.819

**Gaus mean : 30.0460**

**Gaus Width: 4.2679**



# B1L103S, U2-ch56, adc1

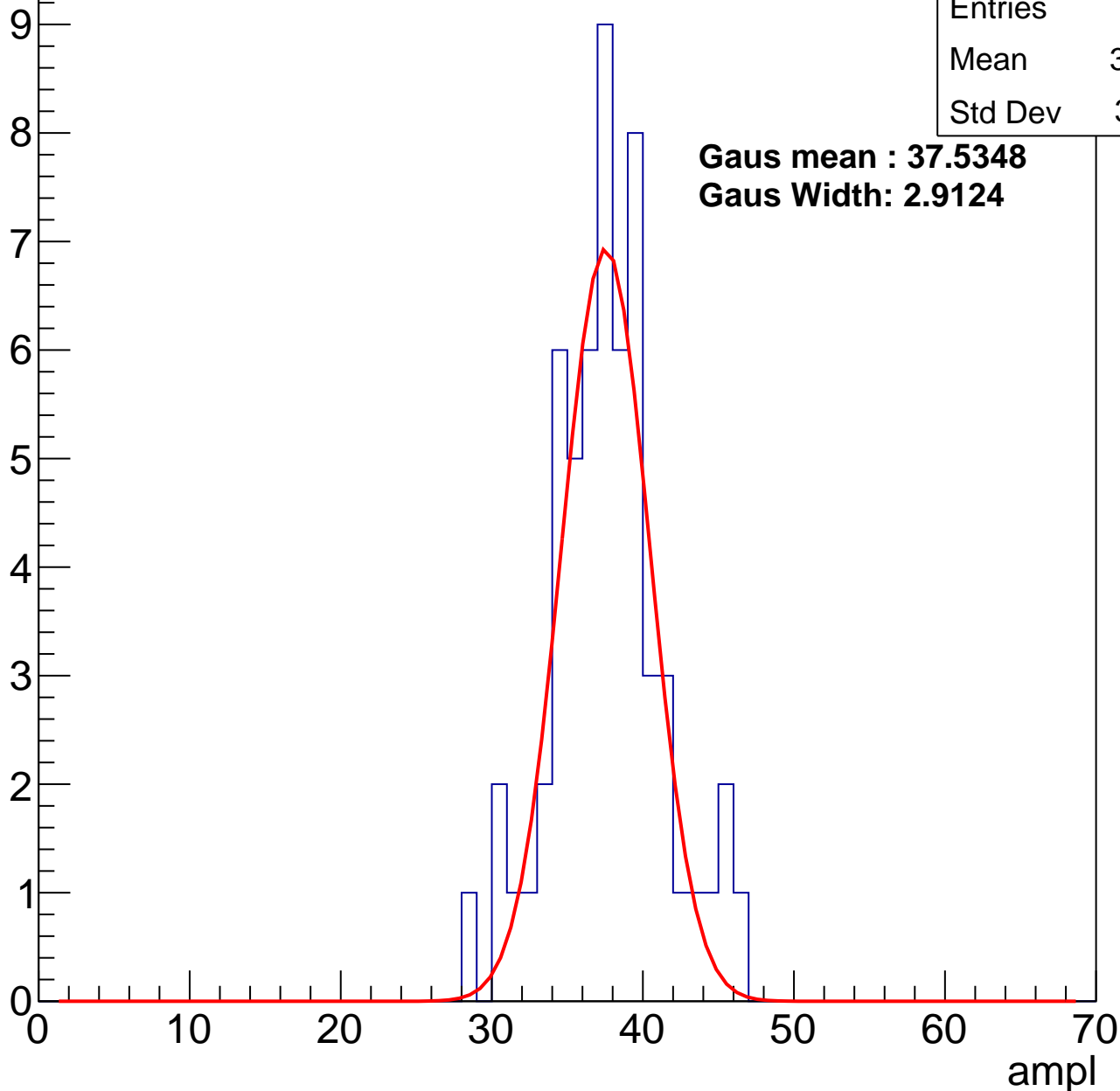
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	37.17
Std Dev	3.641

**Gaus mean : 37.5348**

**Gaus Width: 2.9124**



# B1L103S, U2-ch56, adc2

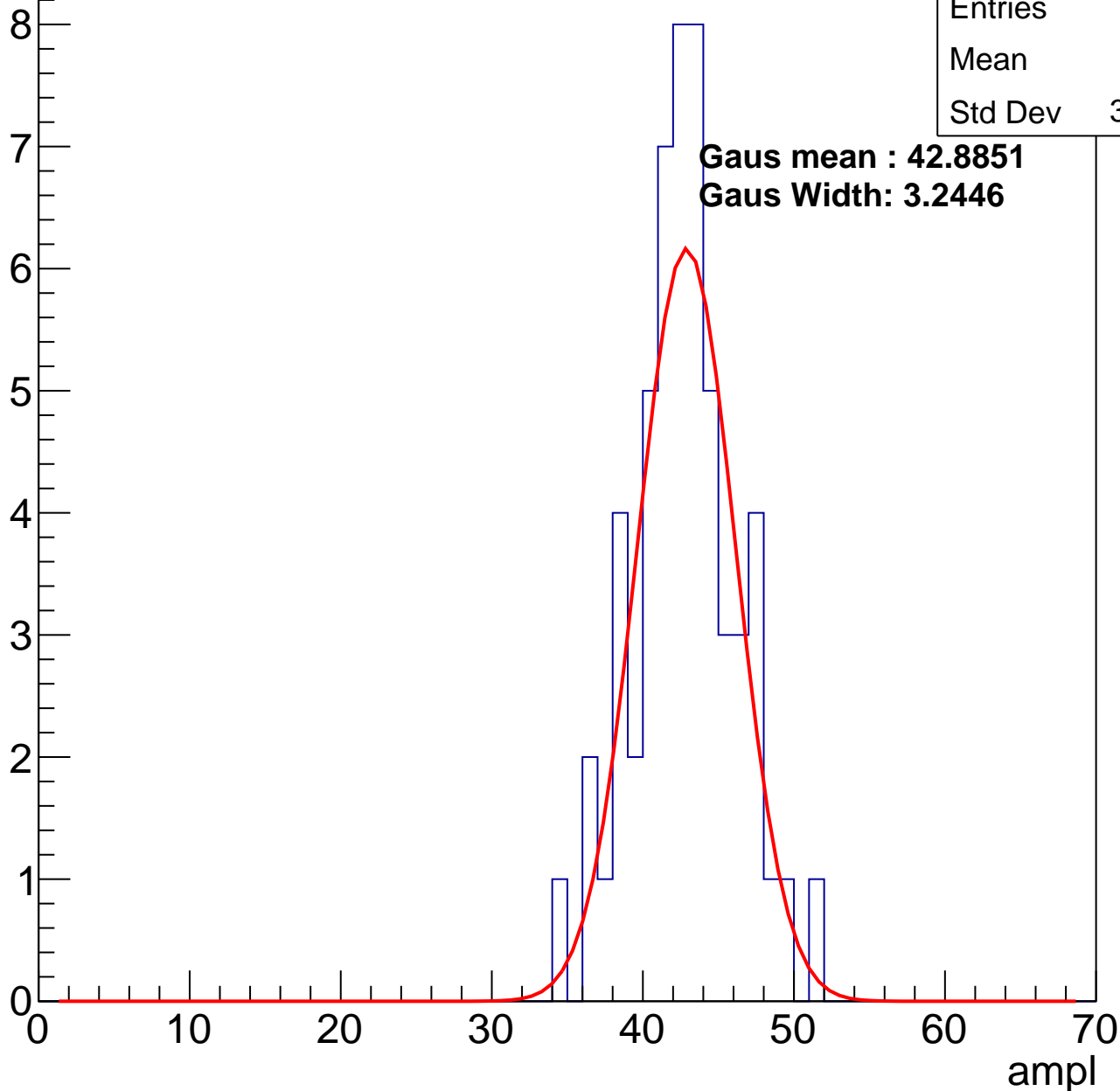
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	42.3
Std Dev	3.364

**Gaus mean : 42.8851**

**Gaus Width: 3.2446**



# B1L103S, U2-ch56, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

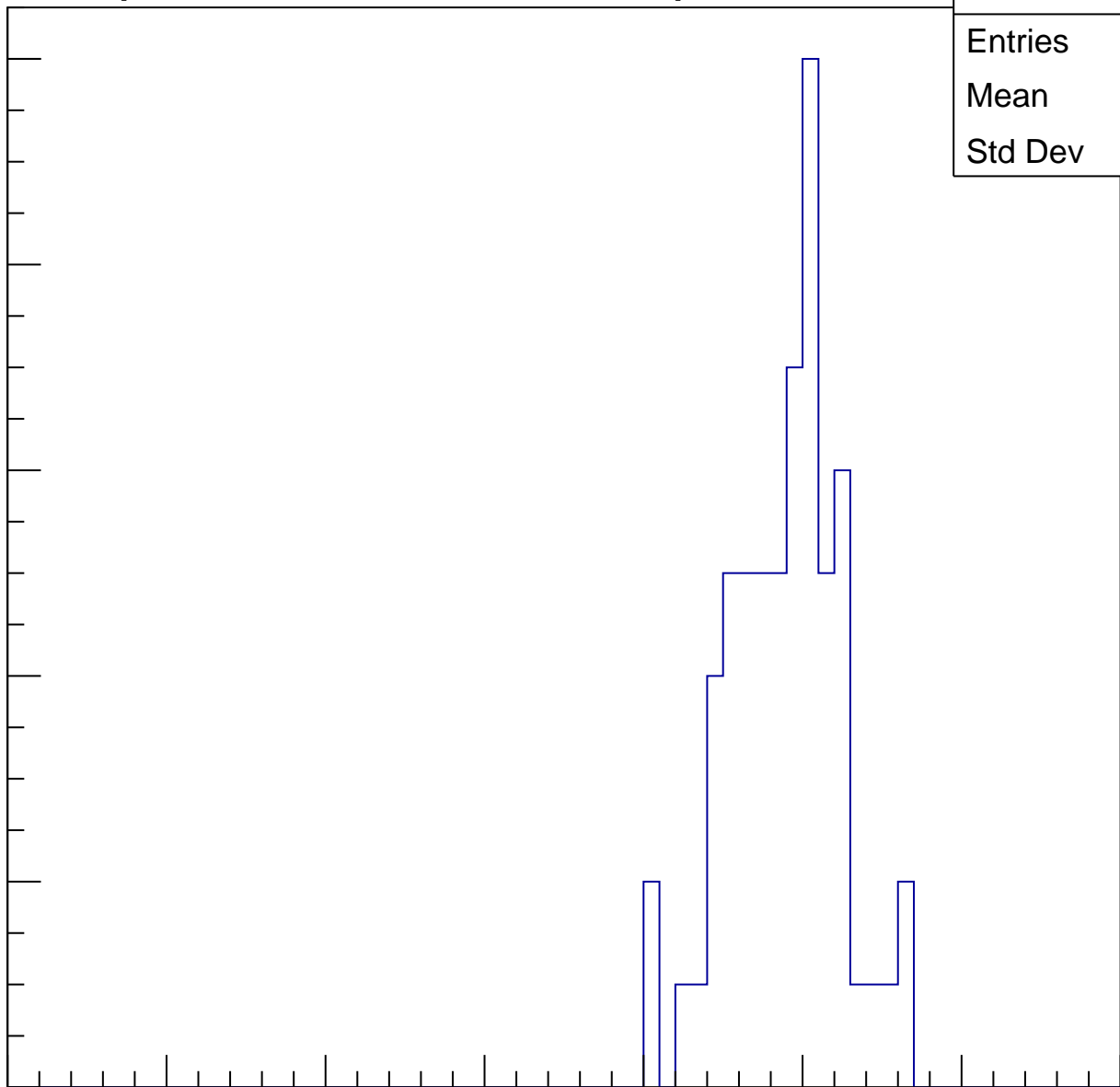
Entries	61
Mean	48.44
Std Dev	3.476

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

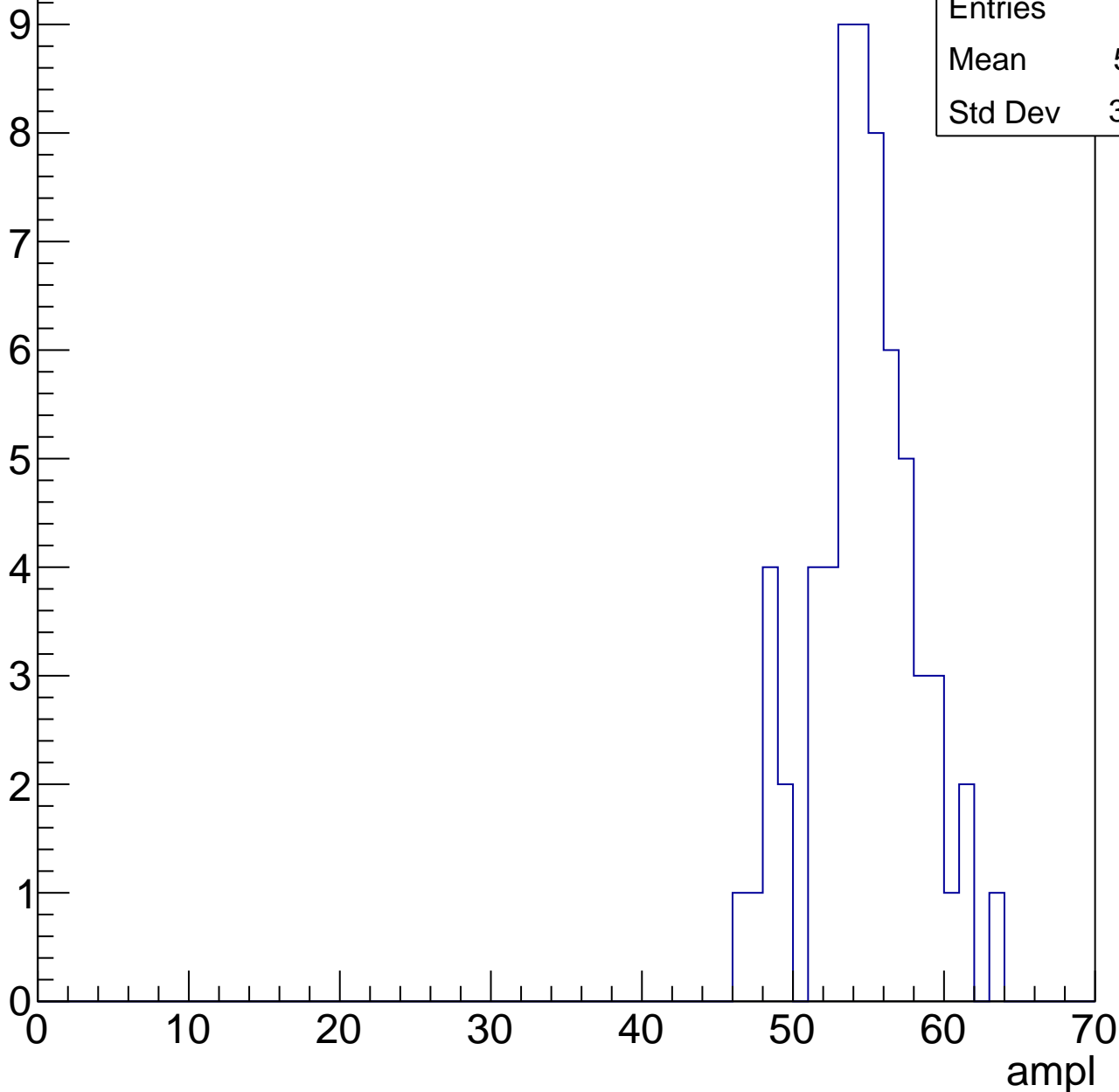


# B1L103S, U2-ch56, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

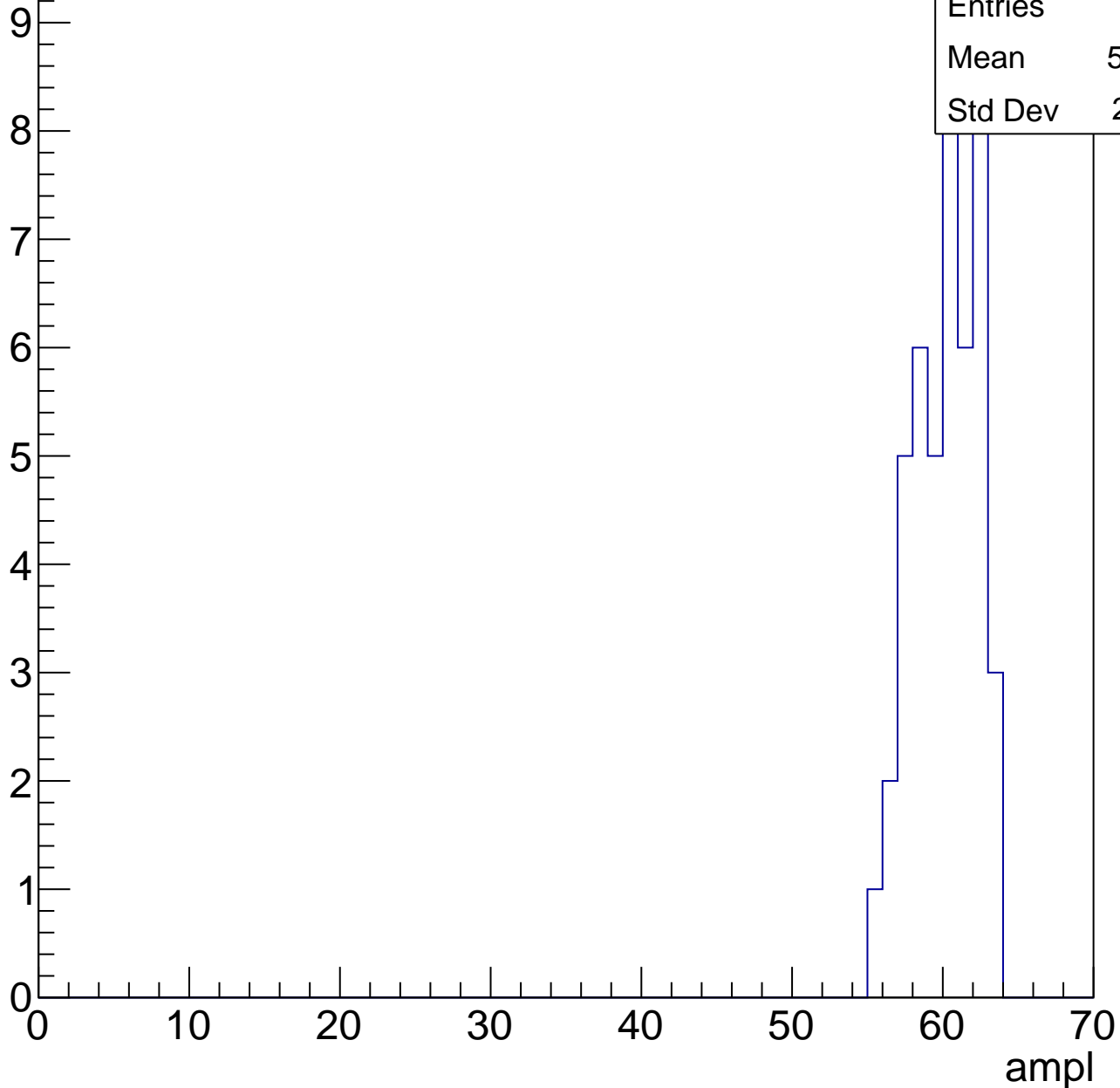
Entries	63
Mean	54.21
Std Dev	3.519



# B1L103S, U2-ch56, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



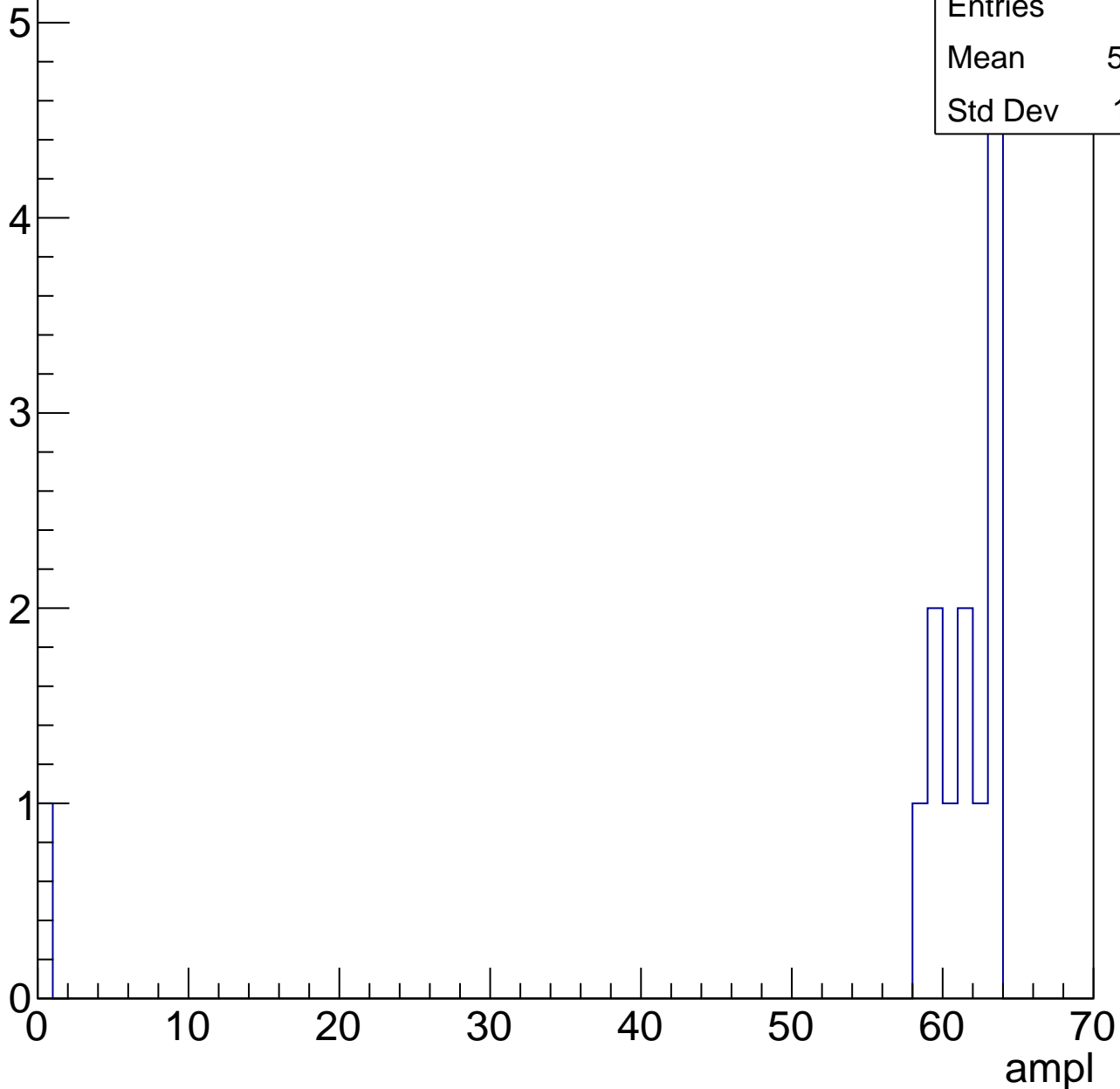
Entries	45
Mean	59.73
Std Dev	2.091

# B1L103S, U2-ch56, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	13
Mean	56.54
Std Dev	16.41





# B1L103S, U2-ch56, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	3
Mean	21
Std Dev	29.7

# B1L103S, U2-ch57, adc0

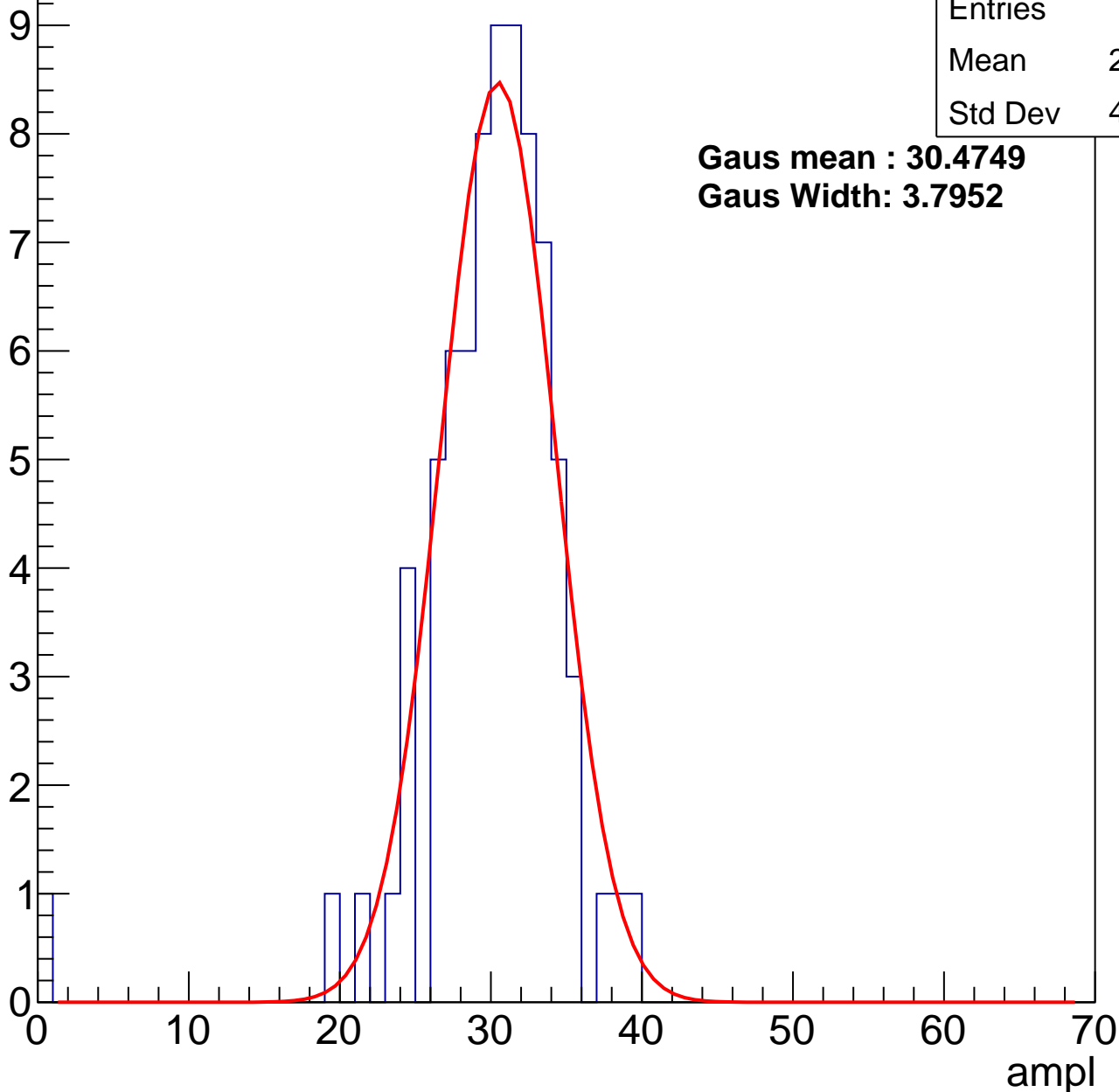
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	29.56
Std Dev	4.966

**Gaus mean : 30.4749**

**Gaus Width: 3.7952**



# B1L103S, U2-ch57, adc1

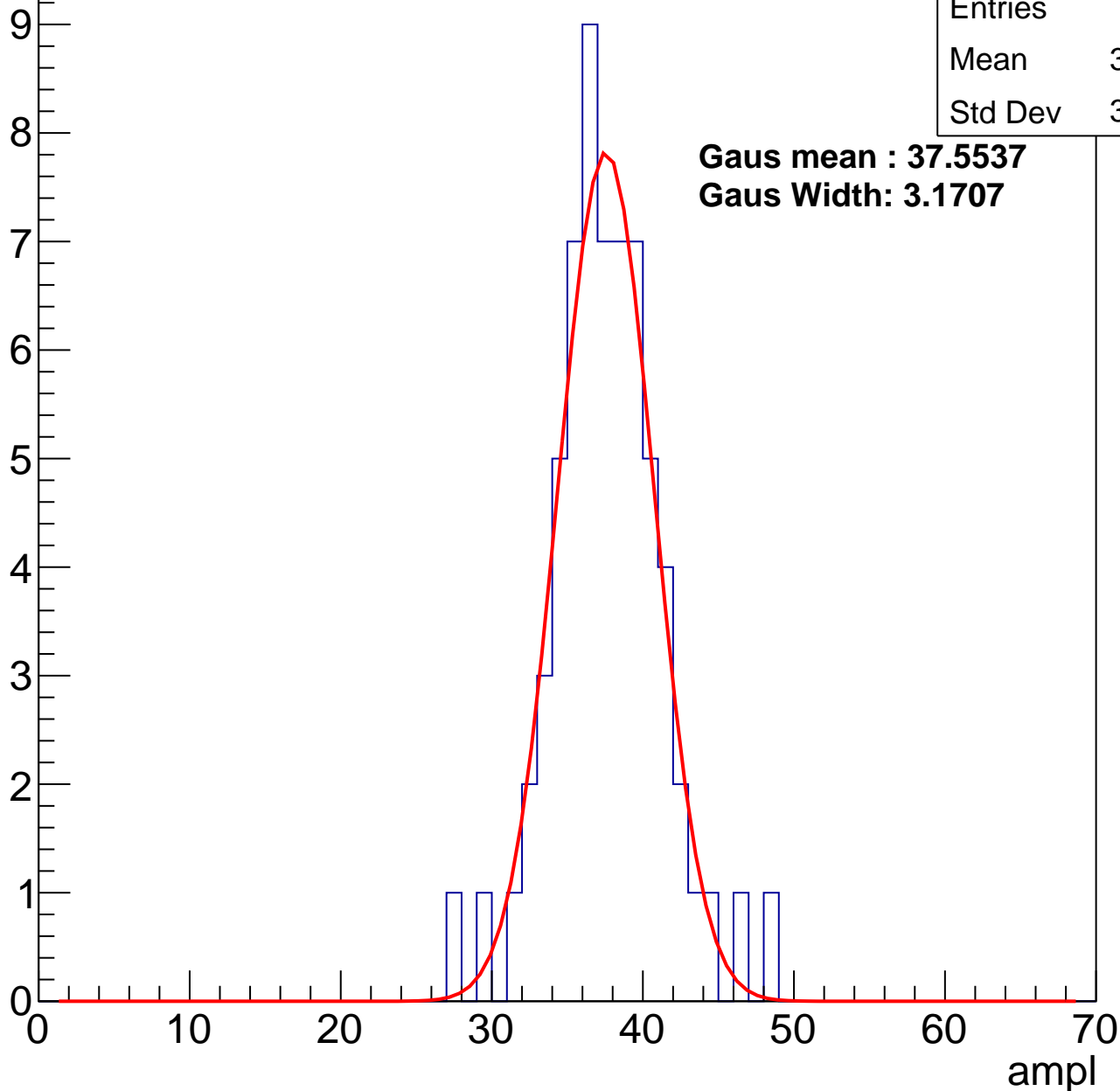
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	37.17
Std Dev	3.636

**Gaus mean : 37.5537**

**Gaus Width: 3.1707**



# B1L103S, U2-ch57, adc2

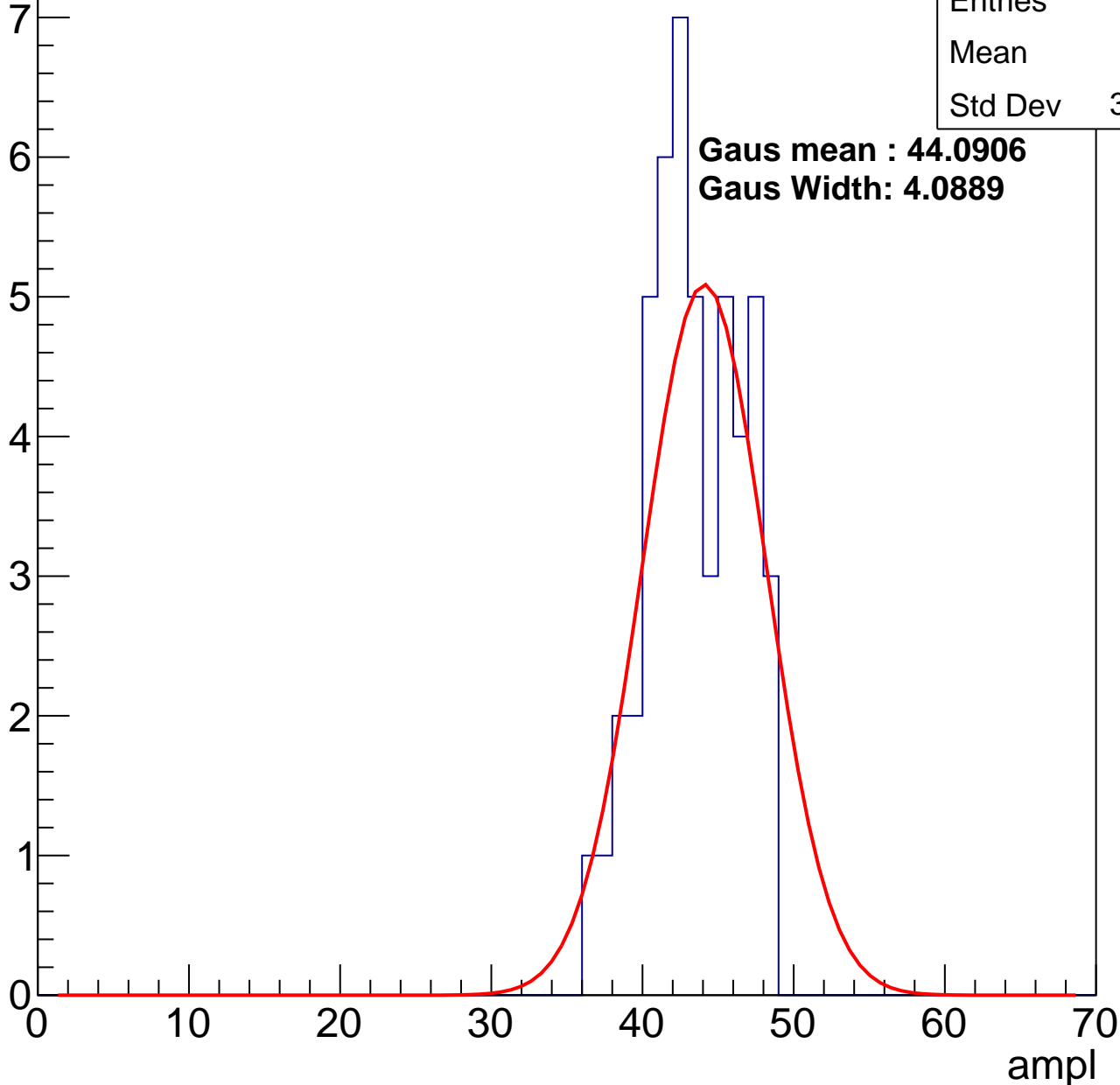
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	42.9
Std Dev	3.052

**Gaus mean : 44.0906**

**Gaus Width: 4.0889**

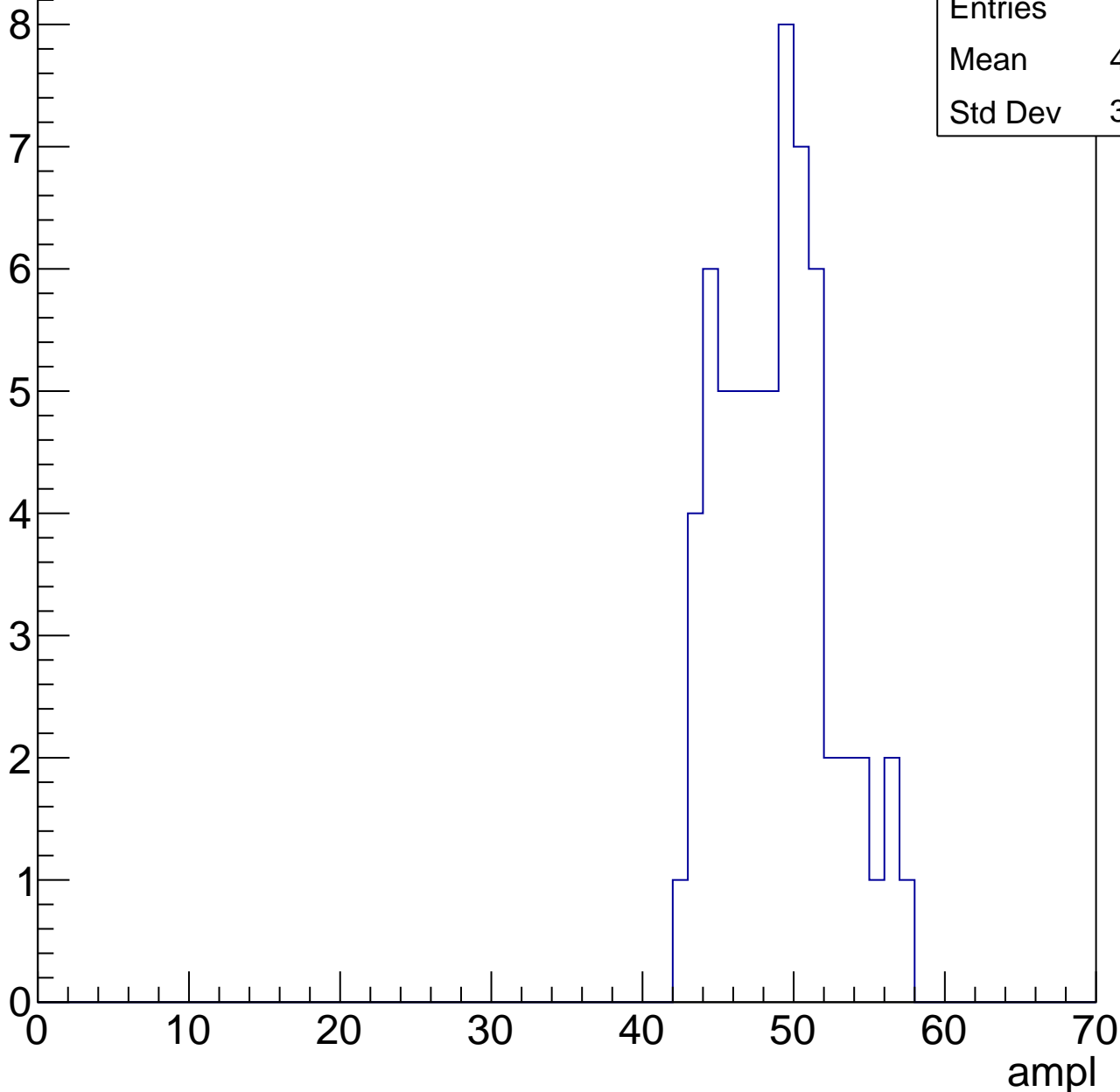


# B1L103S, U2-ch57, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

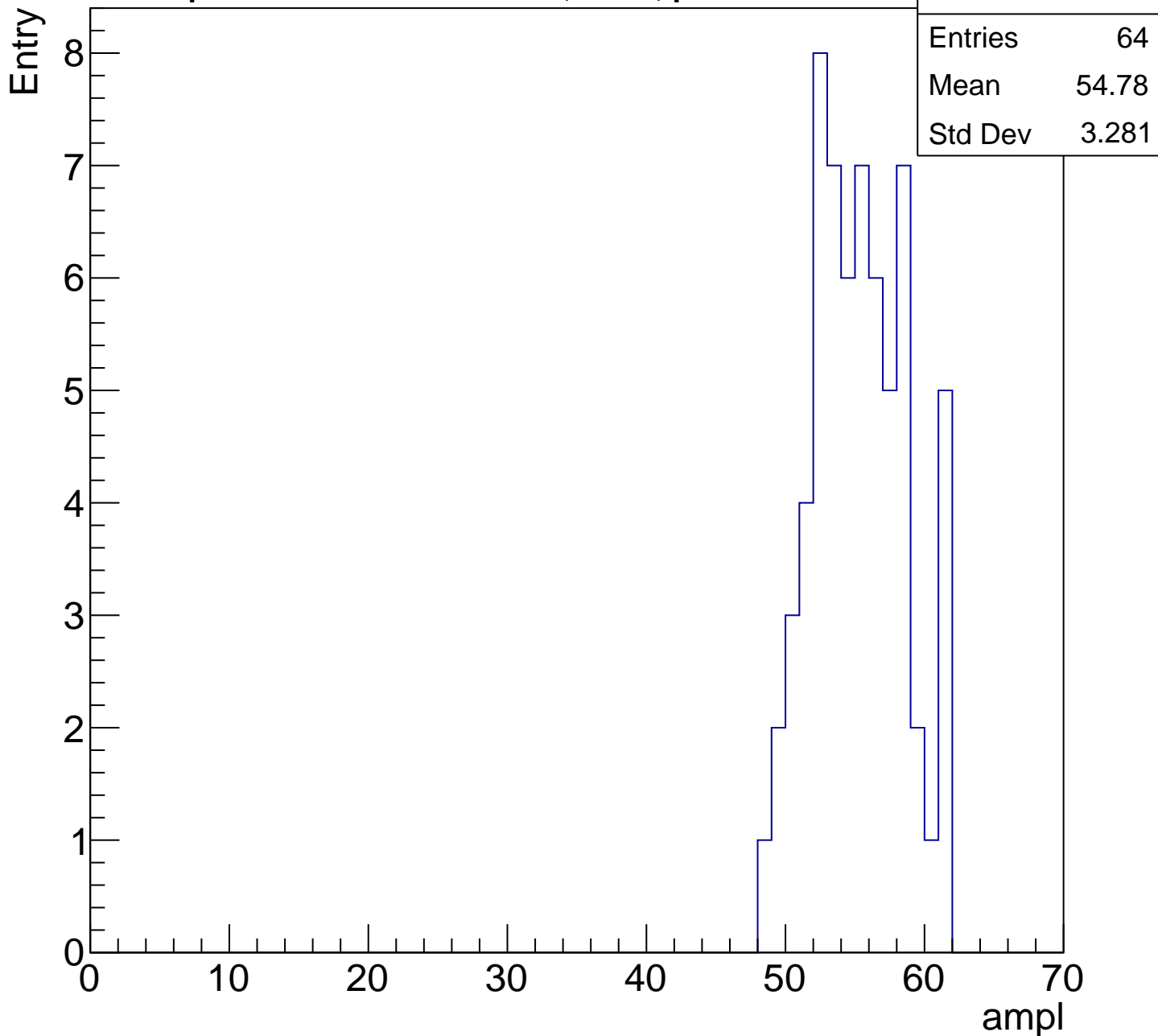
Entry

Entries	62
Mean	48.35
Std Dev	3.584



# B1L103S, U2-ch57, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U2-ch57, adc5

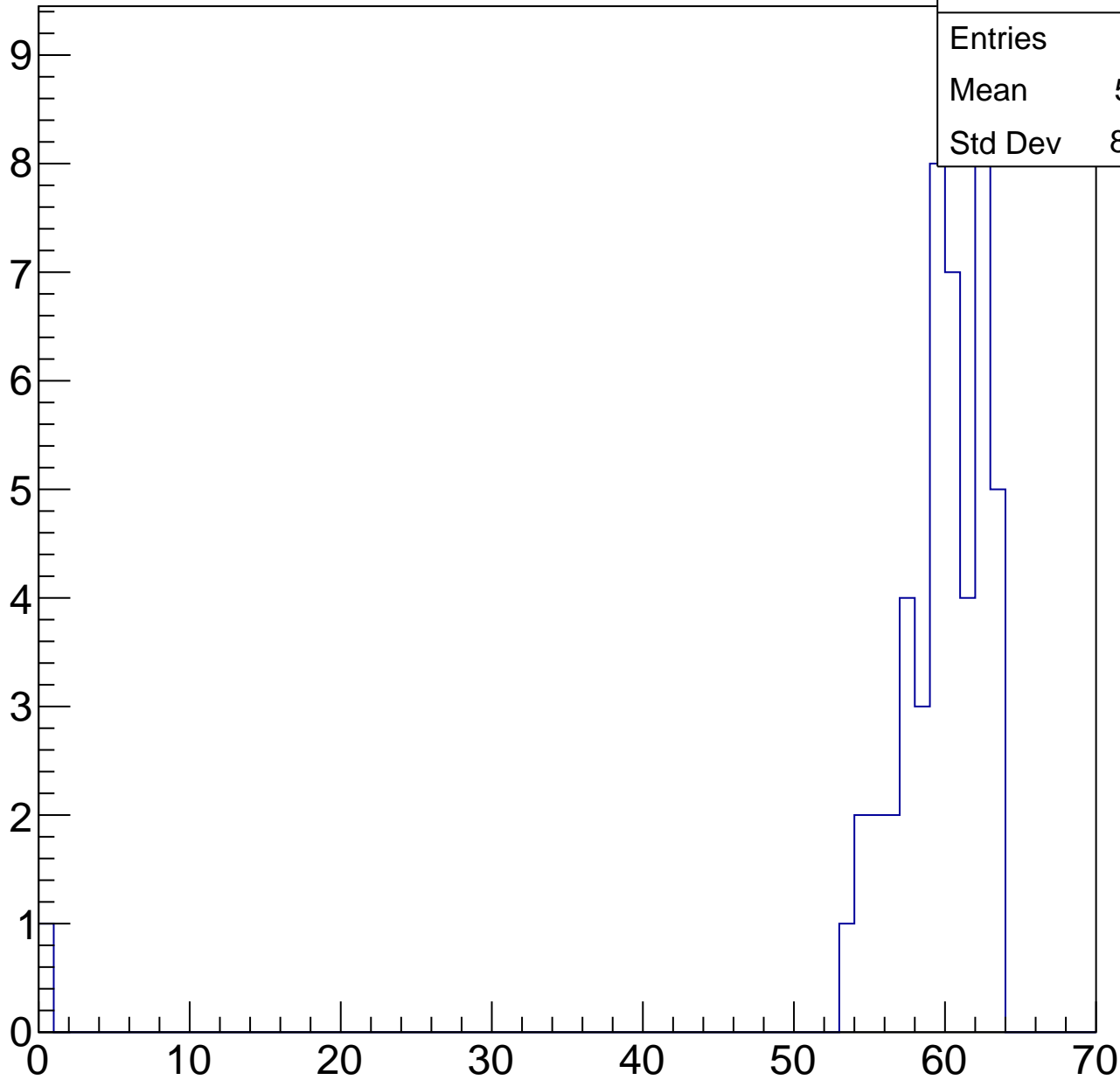
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	48
Mean	58.21
Std Dev	8.886

ampl

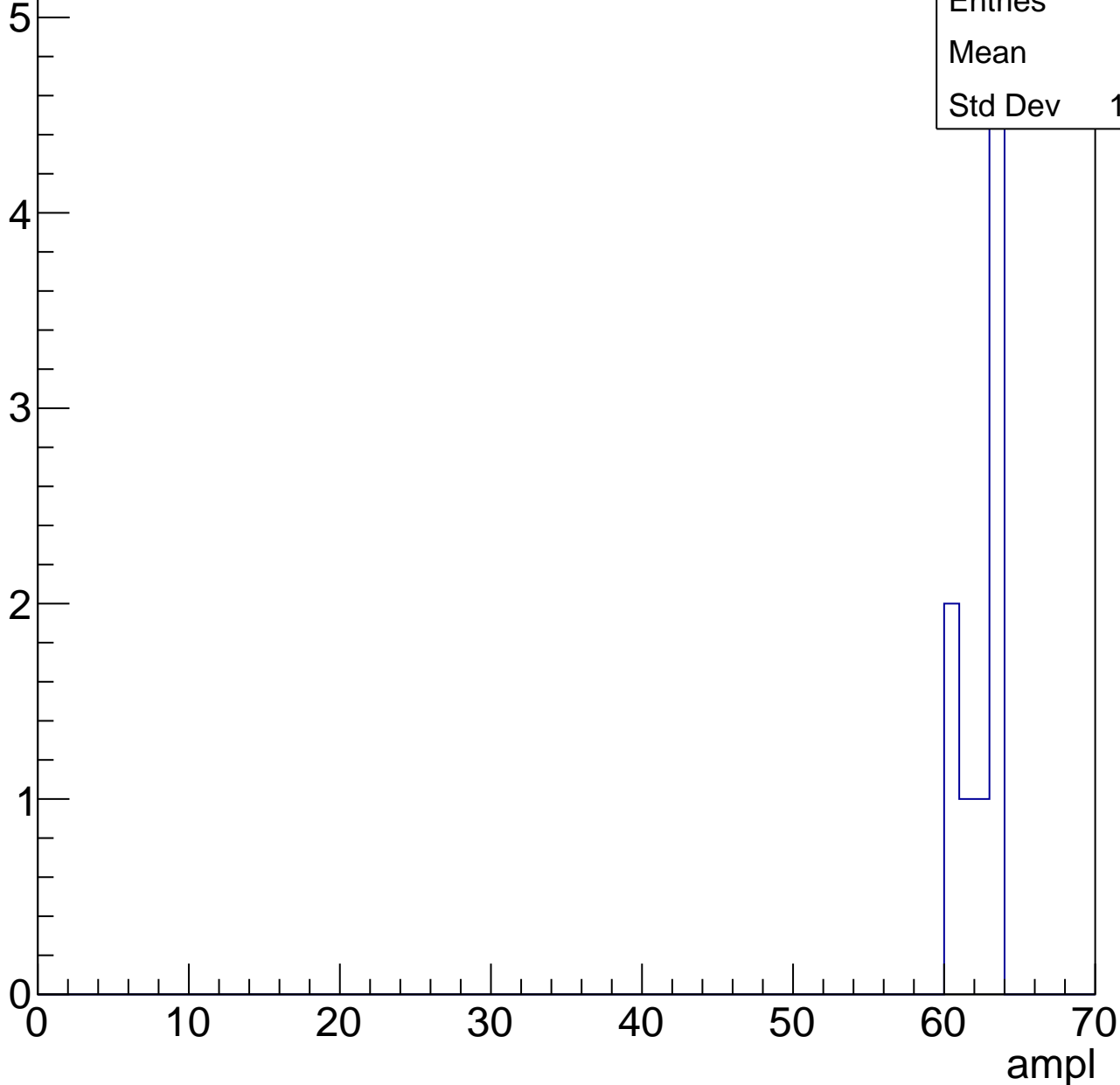


# B1L103S, U2-ch57, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	9
Mean	62
Std Dev	1.247





# B1L103S, U2-ch57, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L103S, U2-ch58, adc0

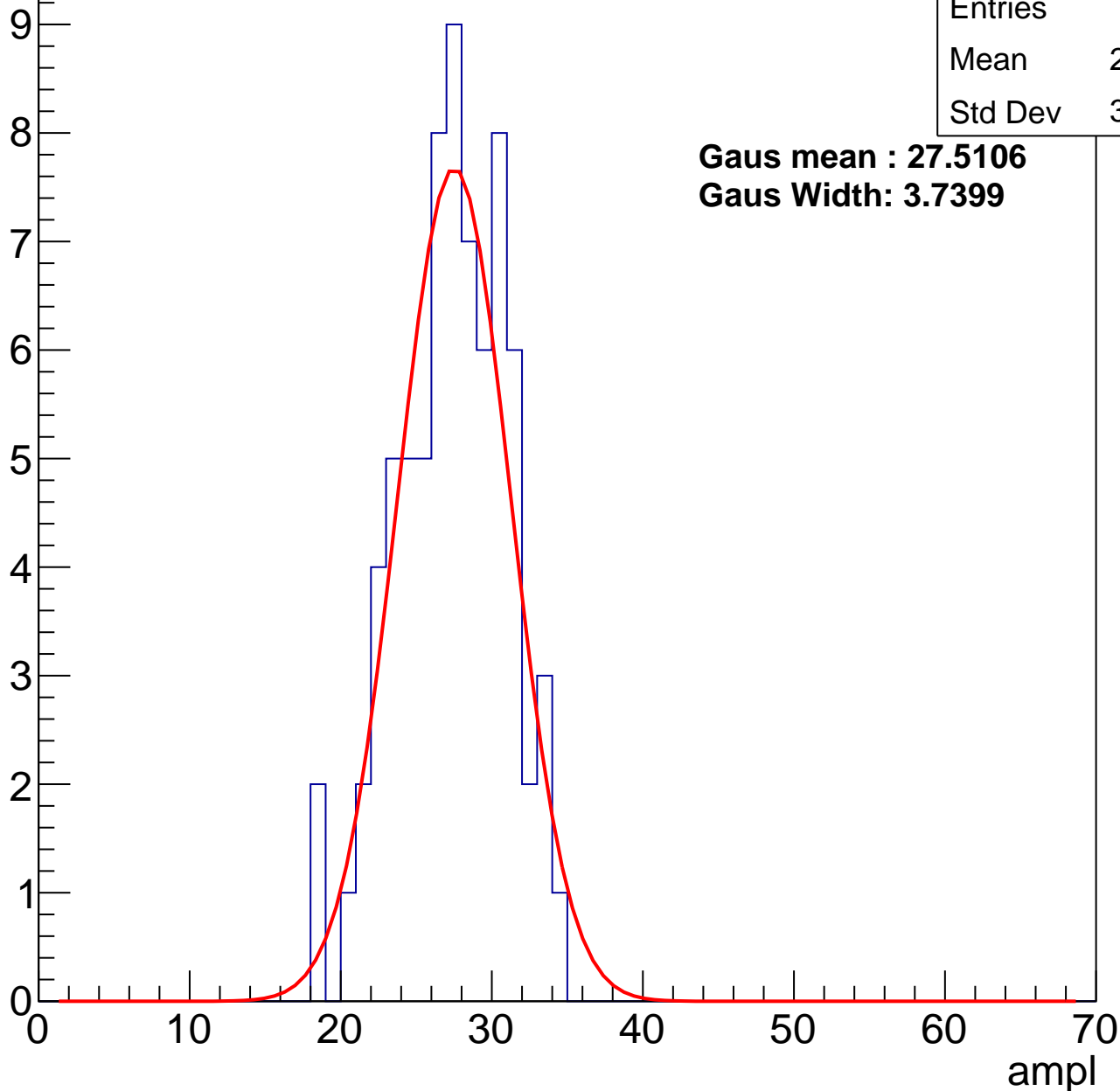
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	26.89
Std Dev	3.566

**Gaus mean : 27.5106**

**Gaus Width: 3.7399**



# B1L103S, U2-ch58, adc1

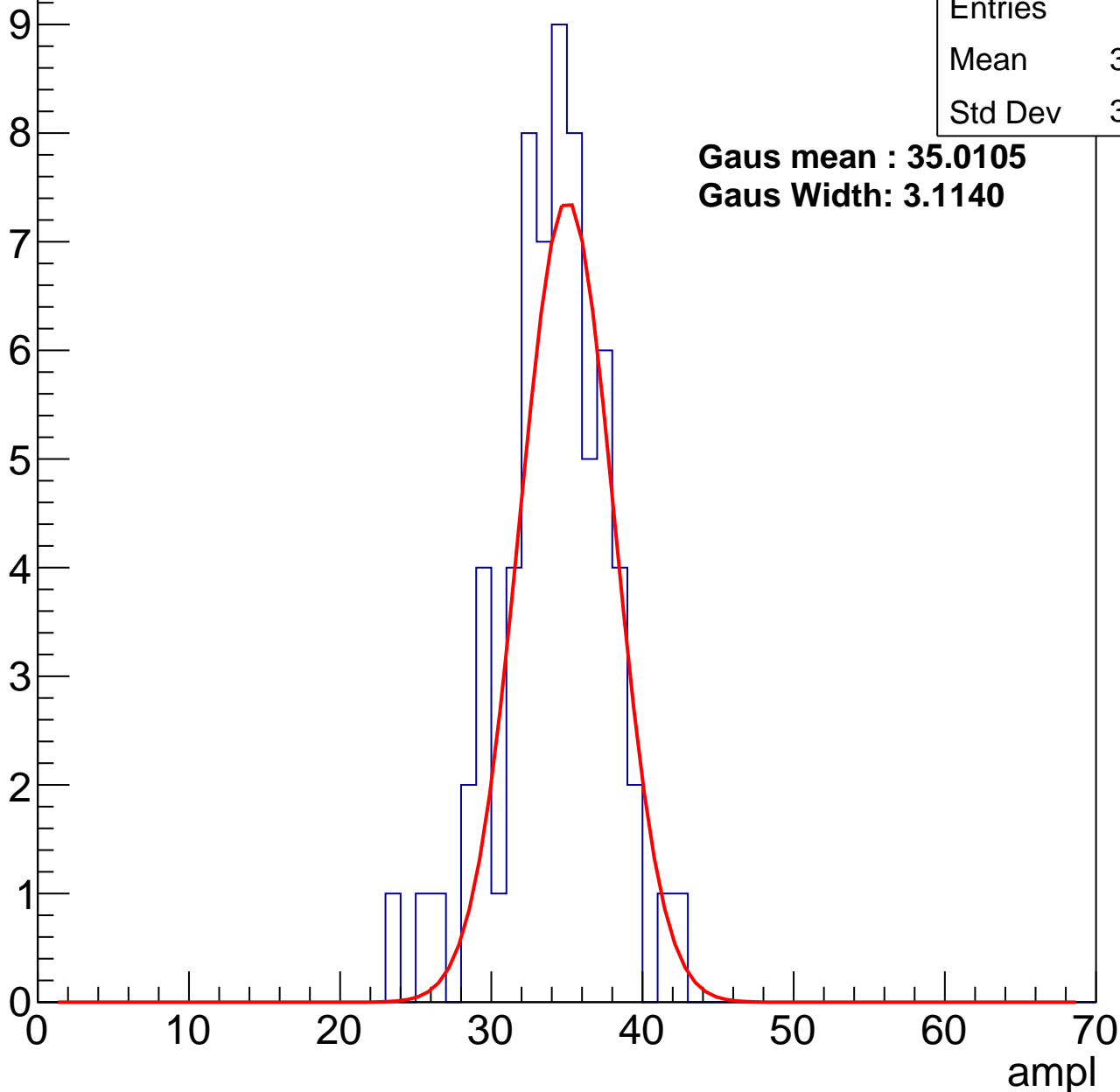
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	33.66
Std Dev	3.575

**Gaus mean : 35.0105**

**Gaus Width: 3.1140**



# B1L103S, U2-ch58, adc2

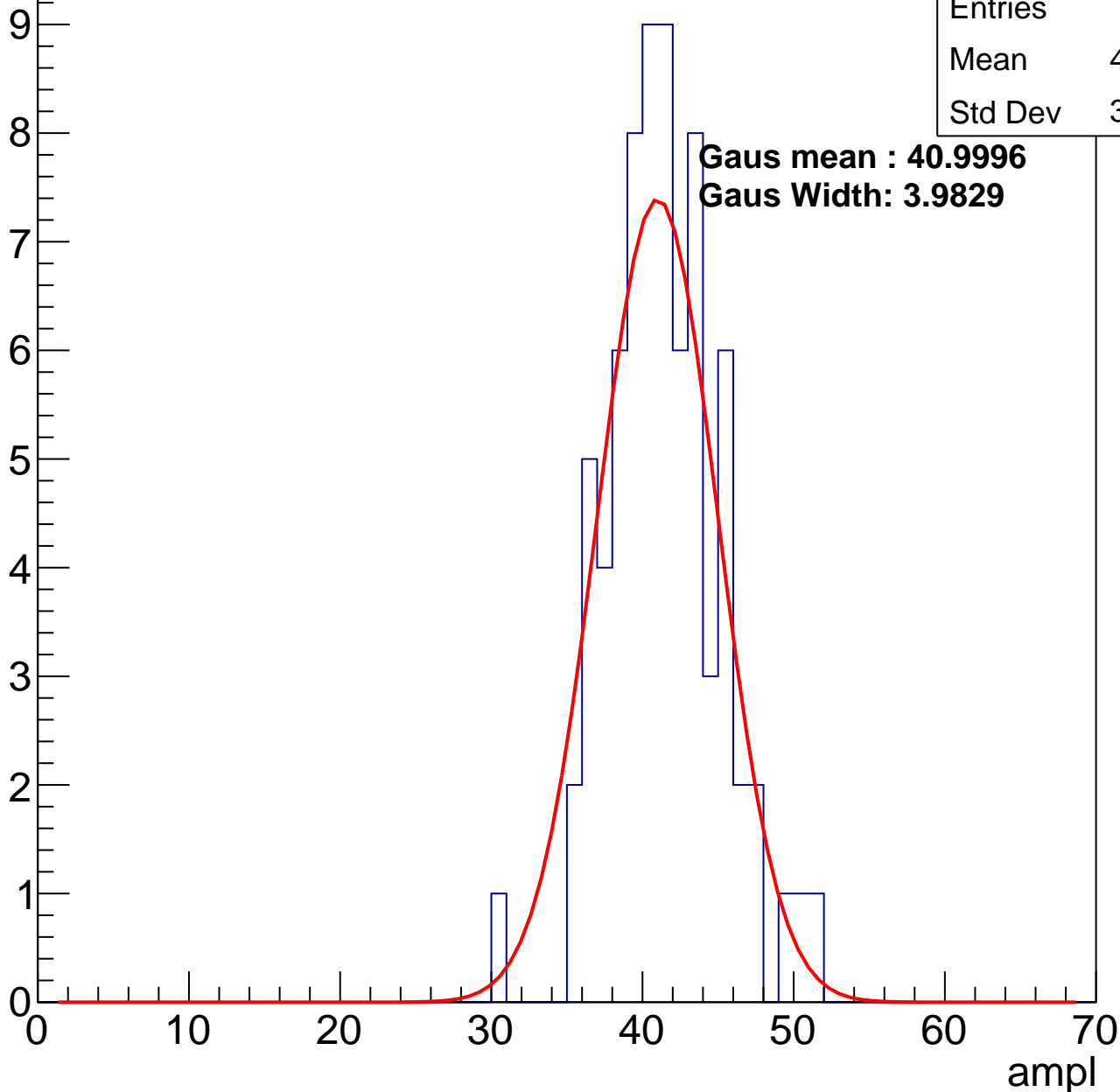
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	40.96
Std Dev	3.685

**Gaus mean : 40.9996**

**Gaus Width: 3.9829**

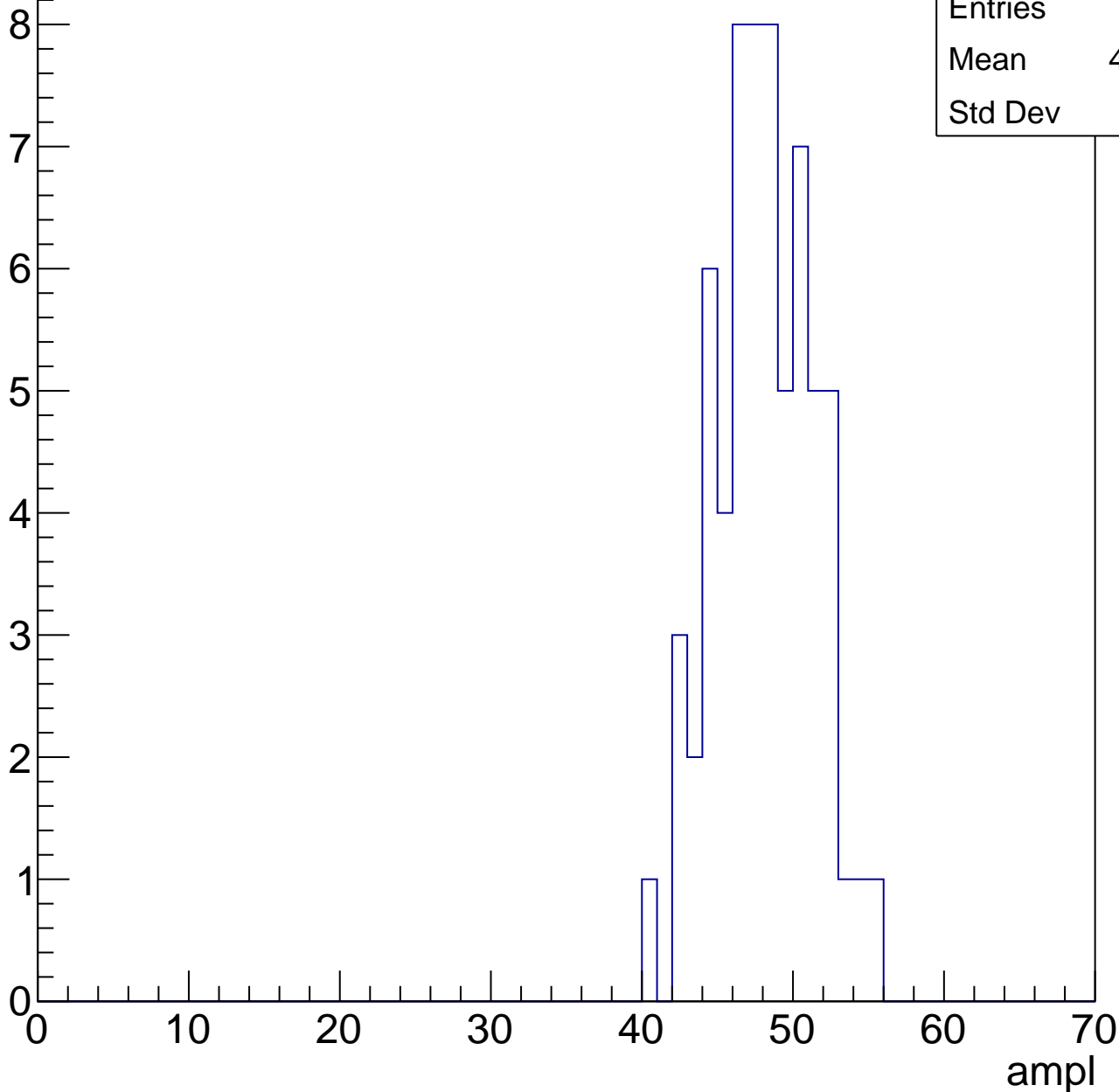


# B1L103S, U2-ch58, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	47.63
Std Dev	3.17

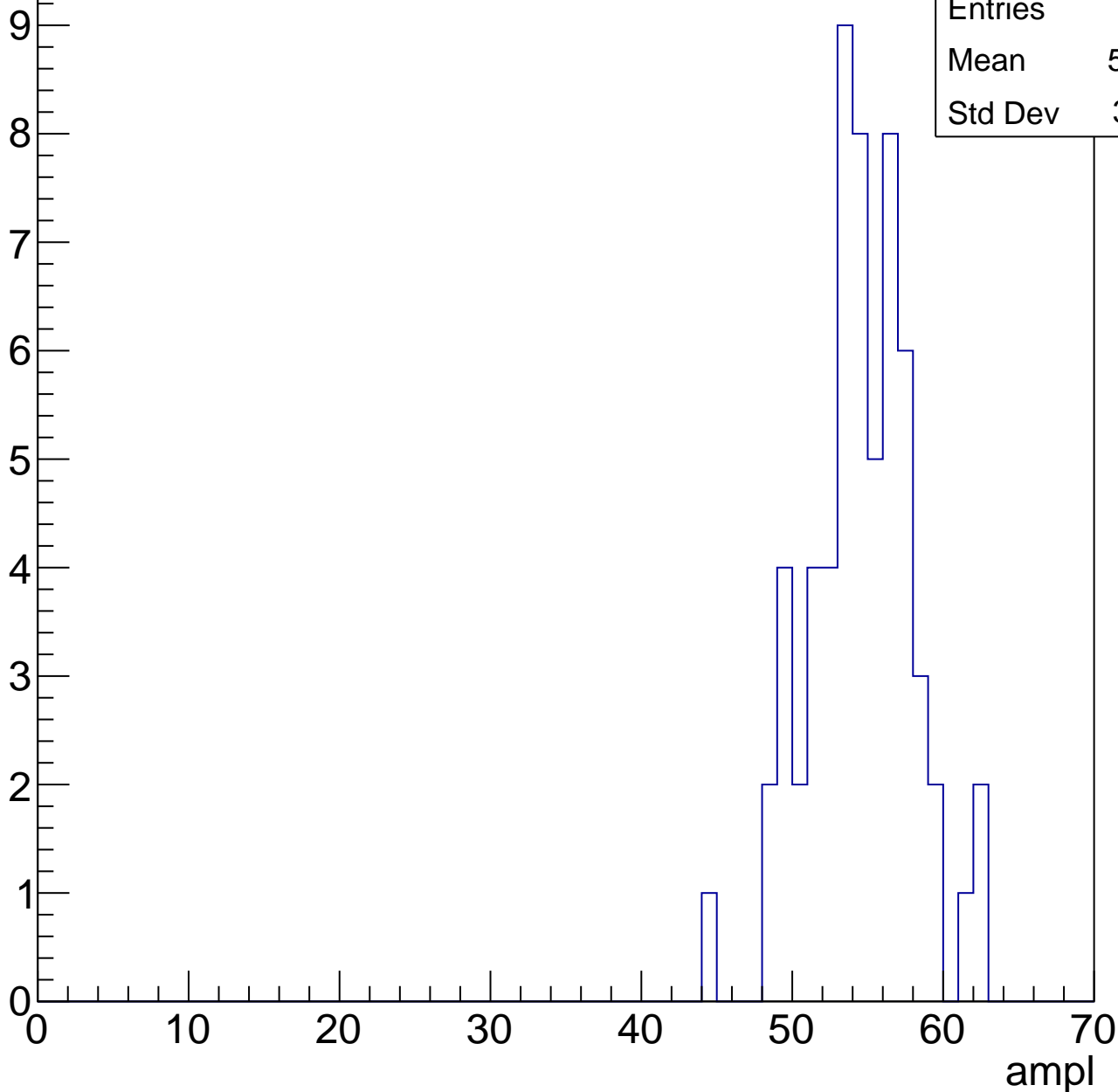


# B1L103S, U2-ch58, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	54.08
Std Dev	3.461

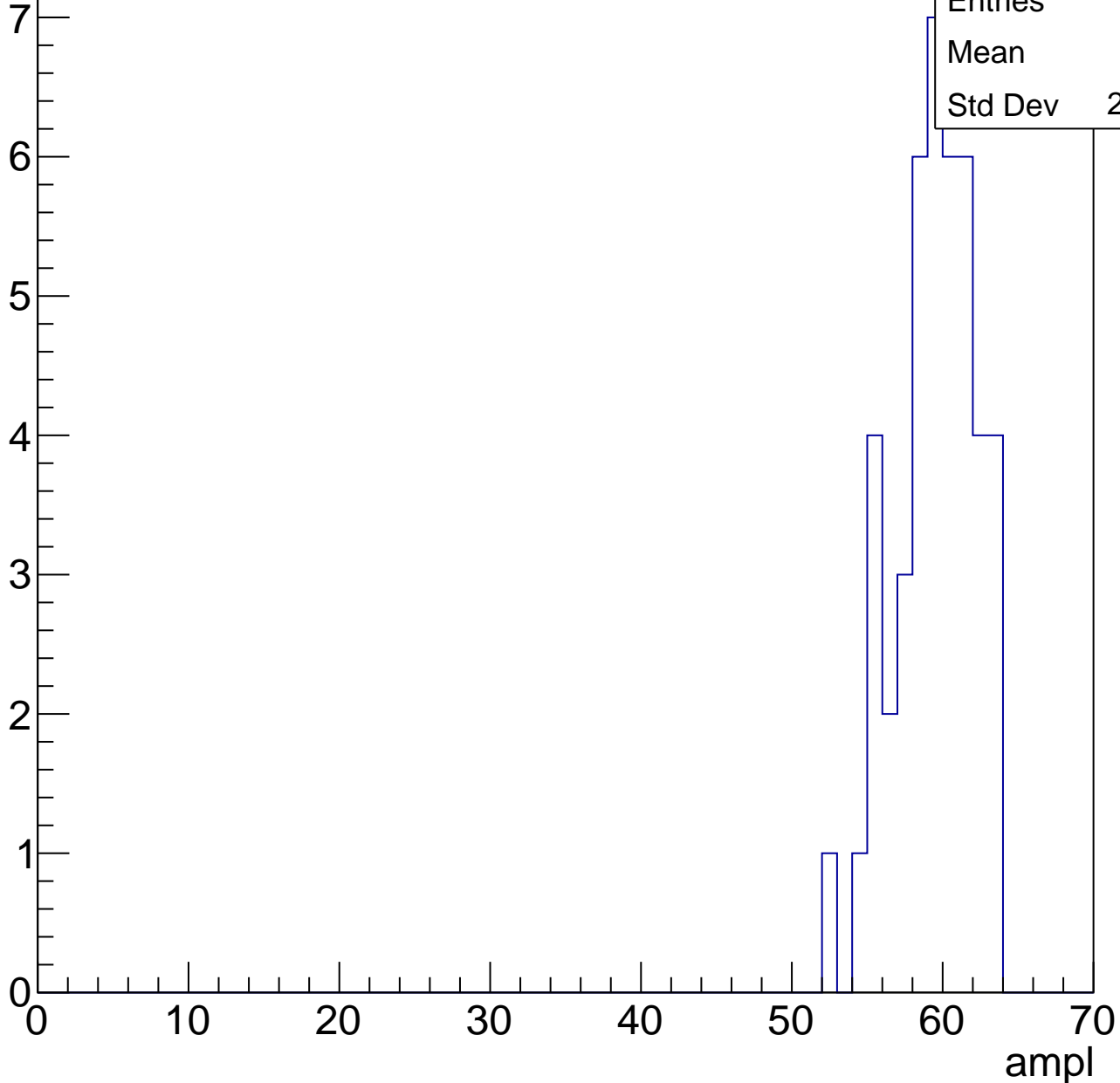


# B1L103S, U2-ch58, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	44
Mean	59
Std Dev	2.629

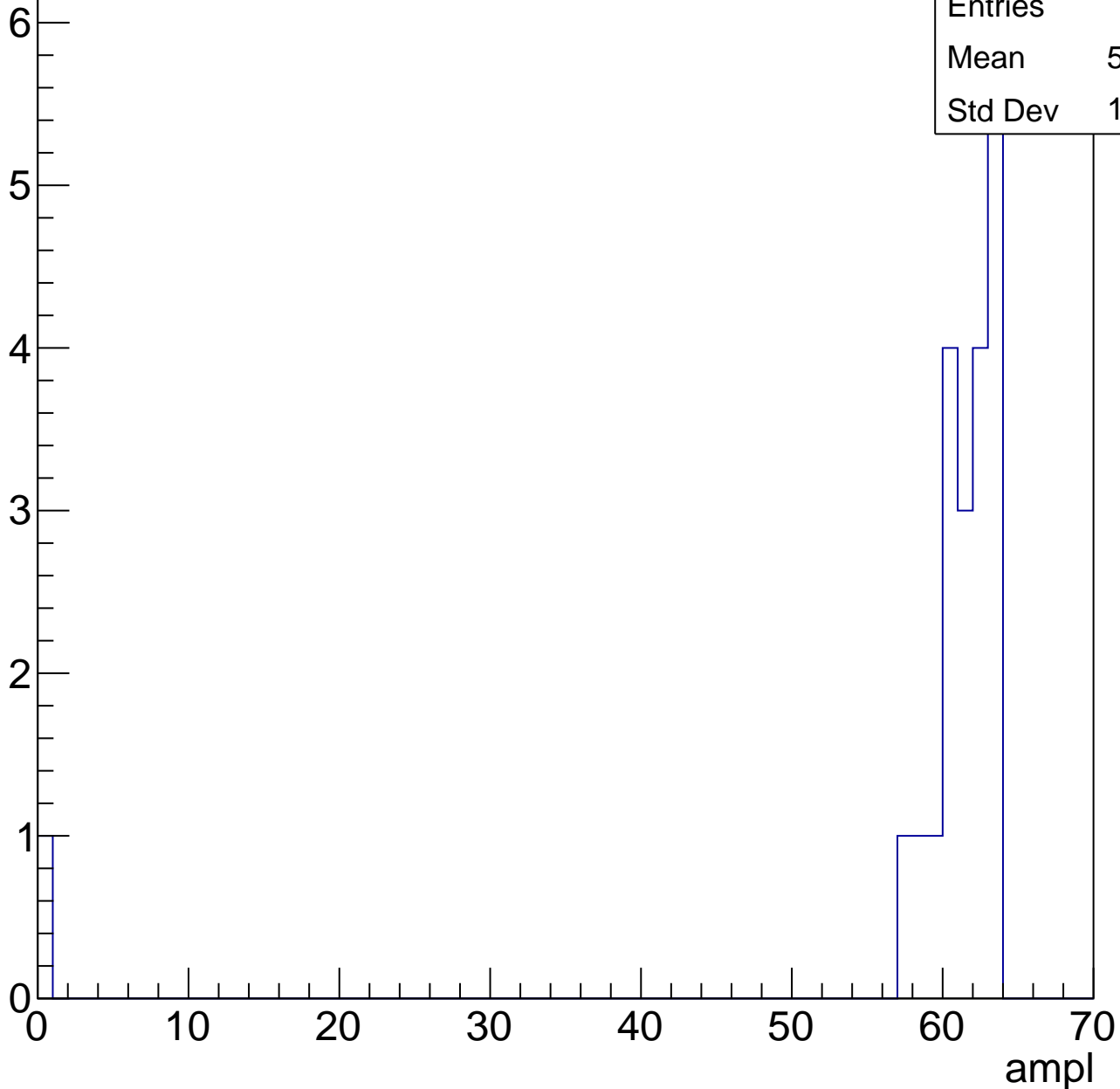


# B1L103S, U2-ch58, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	21
Mean	58.24
Std Dev	13.13





# B1L103S, U2-ch58, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U2-ch59, adc0

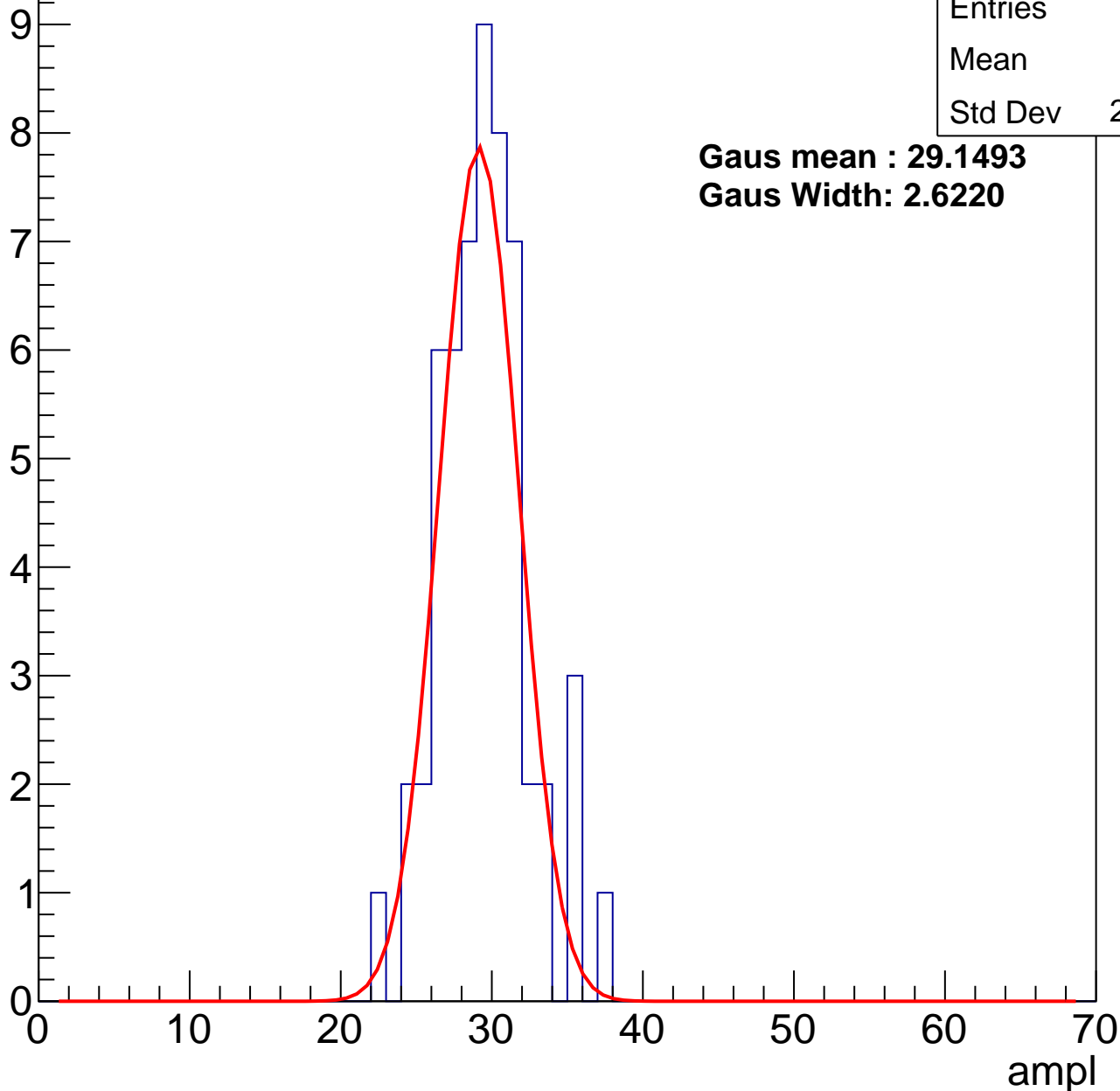
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	29
Std Dev	2.909

**Gaus mean : 29.1493**

**Gaus Width: 2.6220**



# B1L103S, U2-ch59, adc1

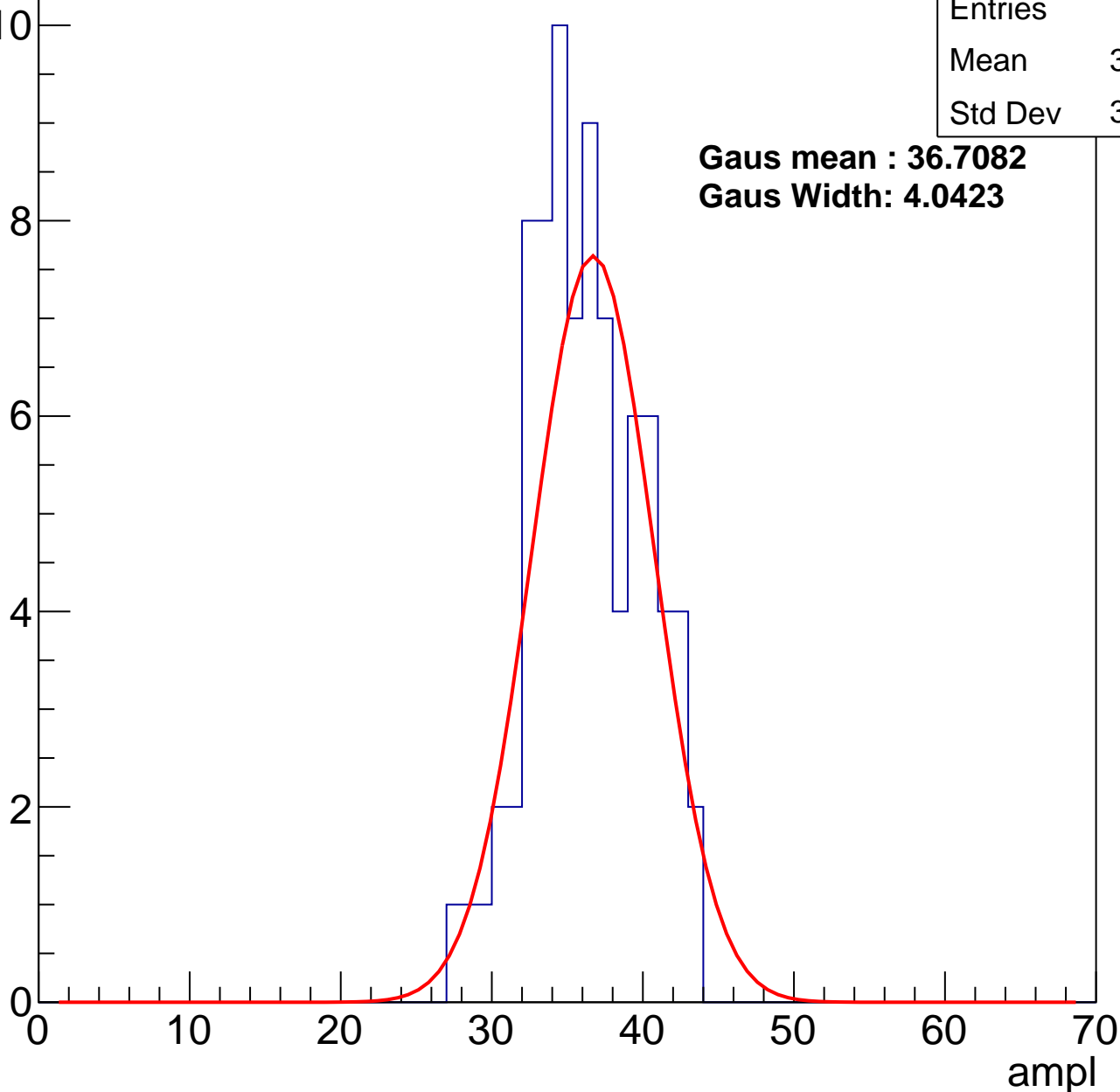
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	82
Mean	35.83
Std Dev	3.622

**Gaus mean : 36.7082**

**Gaus Width: 4.0423**



# B1L103S, U2-ch59, adc2

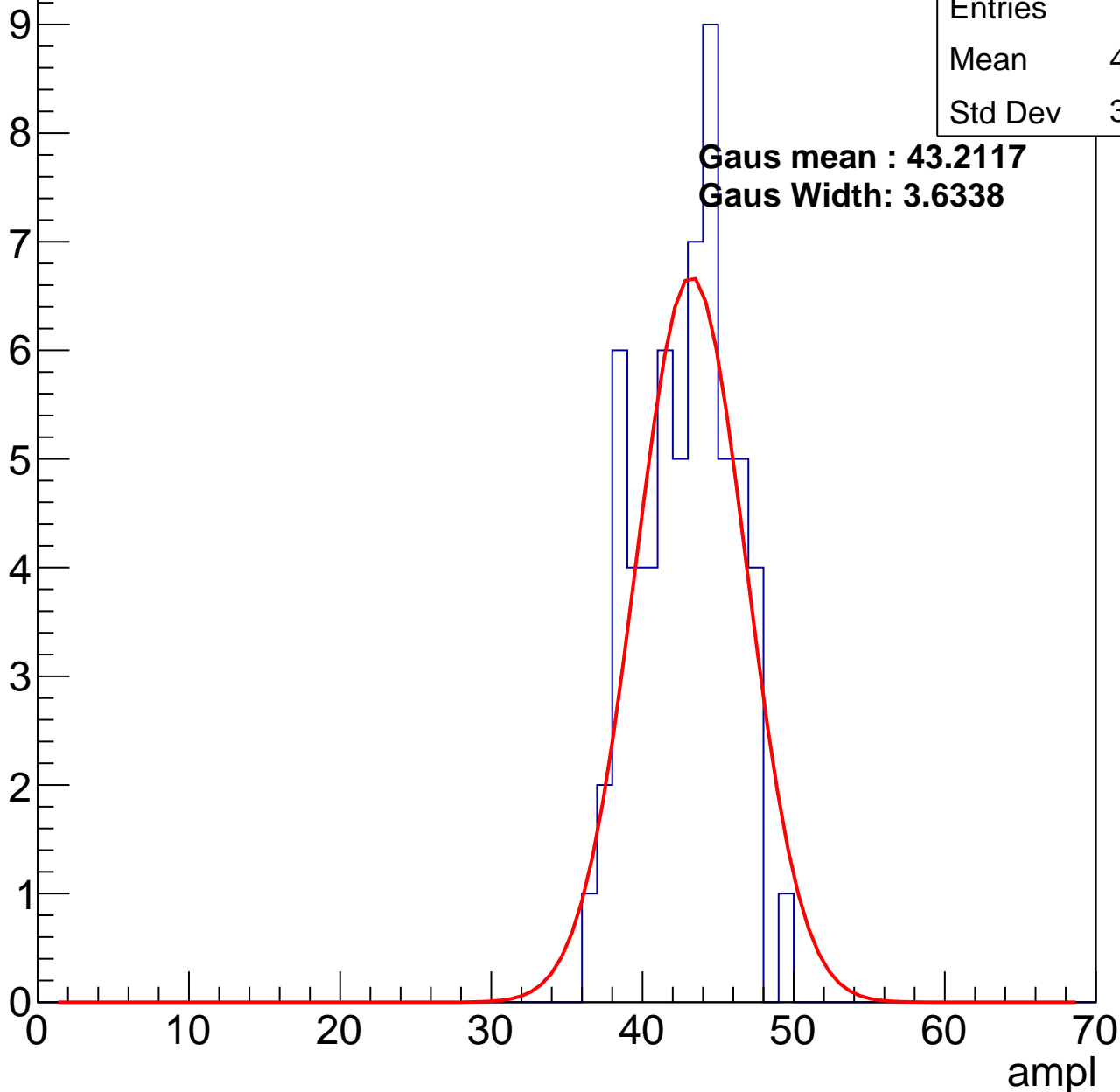
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	42.36
Std Dev	3.052

**Gaus mean : 43.2117**

**Gaus Width: 3.6338**

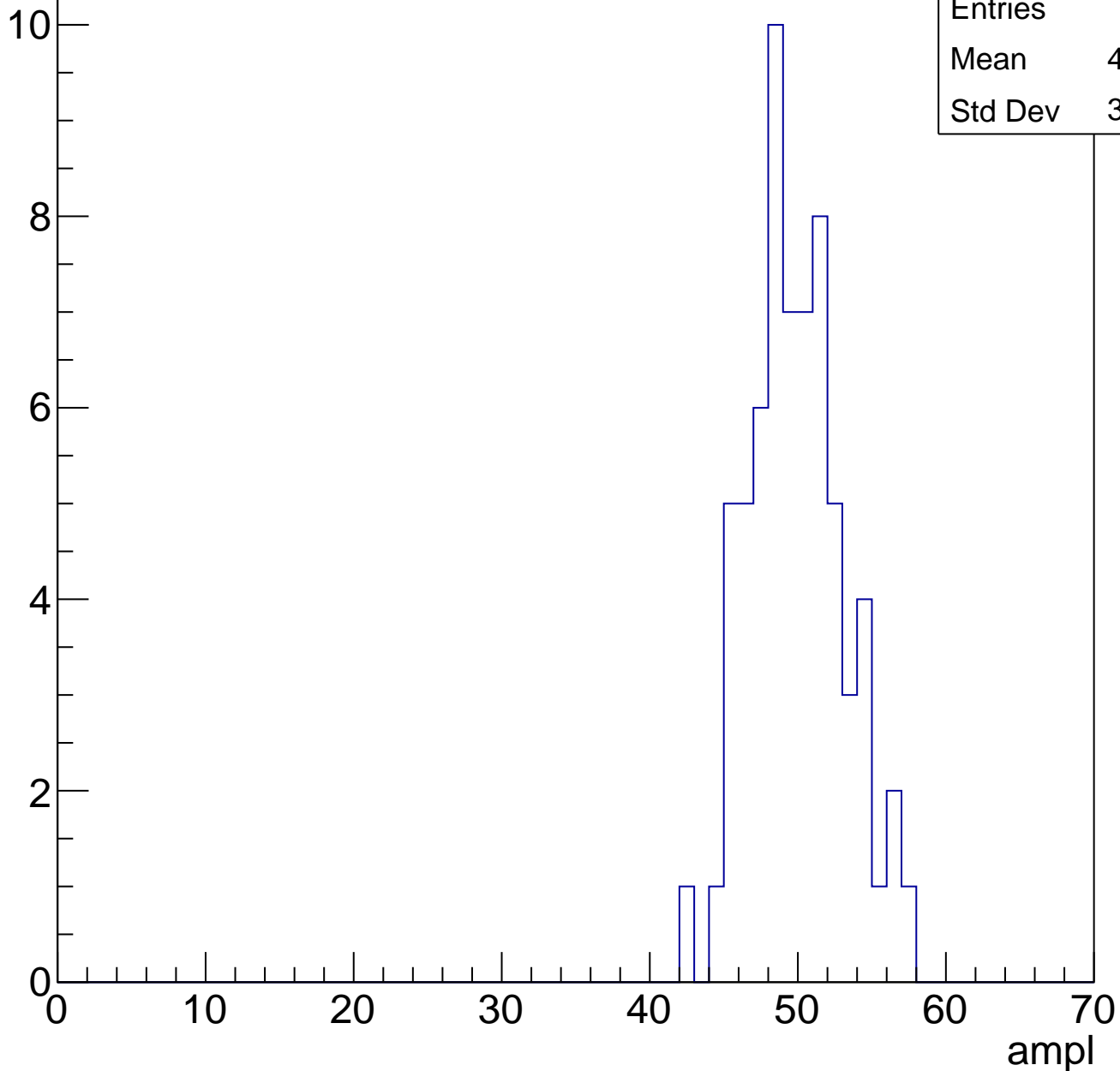


# B1L103S, U2-ch59, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

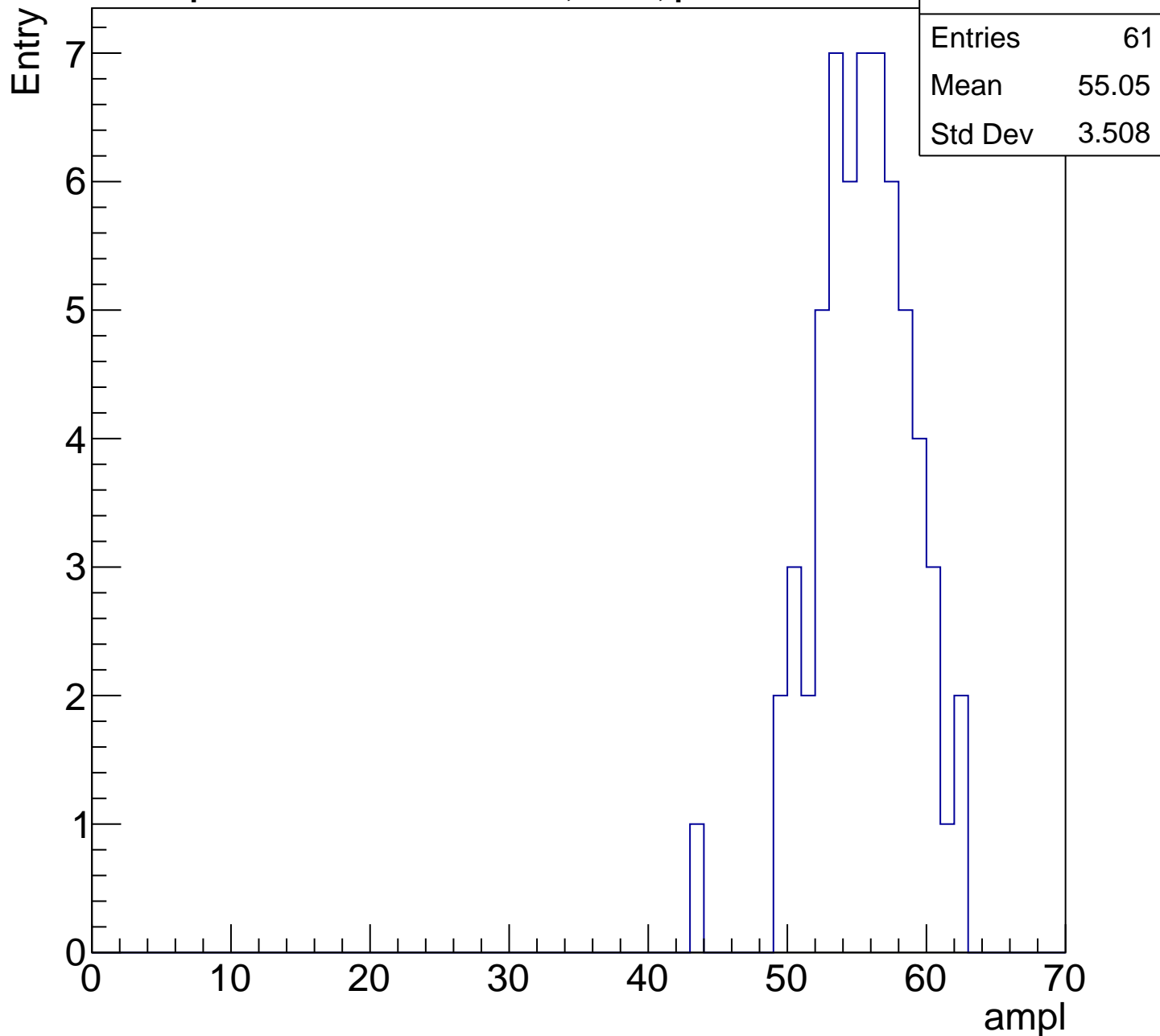
Entries	66
Mean	49.44
Std Dev	3.139

Entry



# B1L103S, U2-ch59, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U2-ch59, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

7

6

5

4

3

2

1

0

Entries

41

Mean

60.12

Std Dev

2.2

ampl

0

10

20

30

40

50

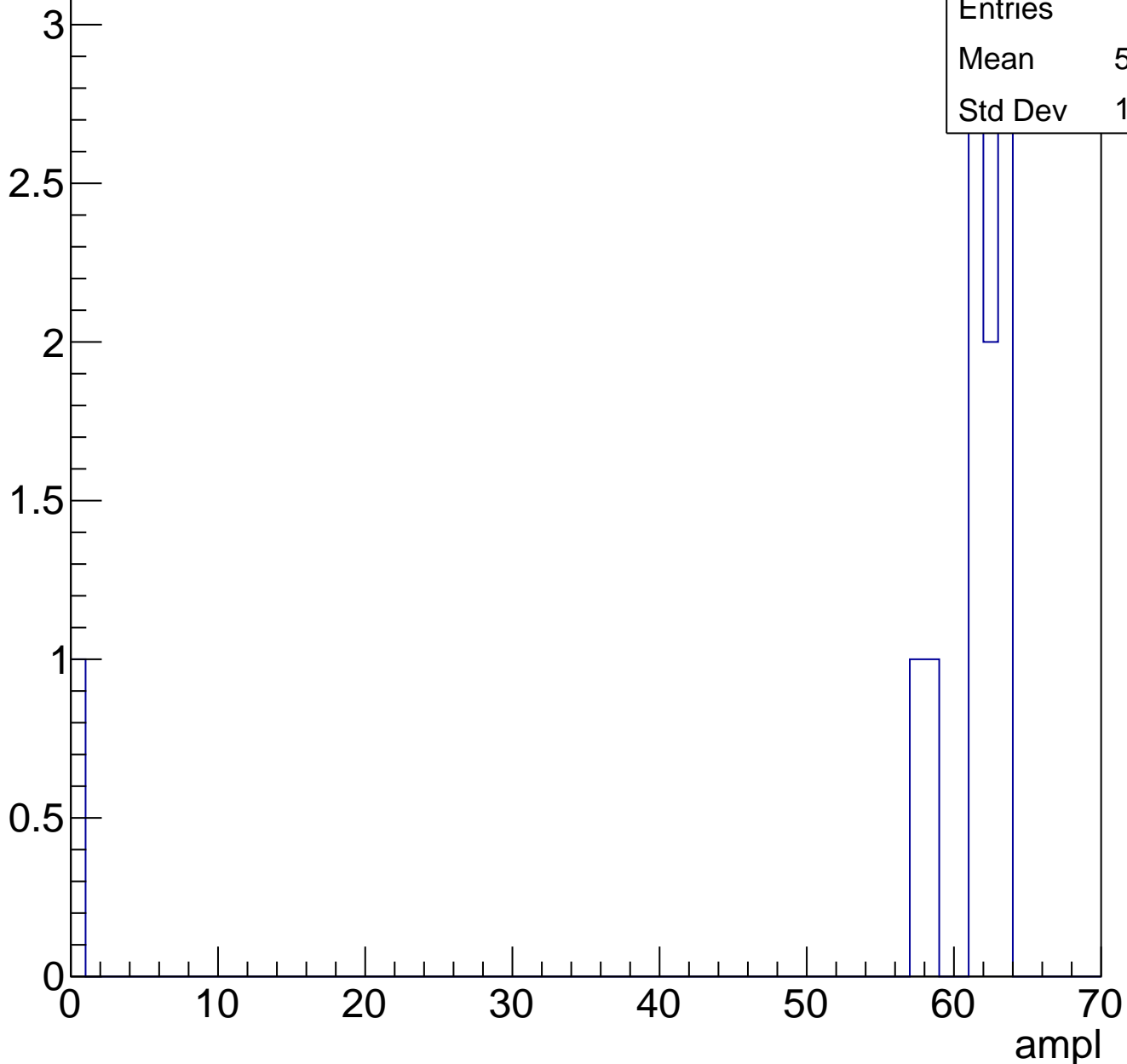
60

70

# B1L103S, U2-ch59, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U2-ch59, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch60, adc0

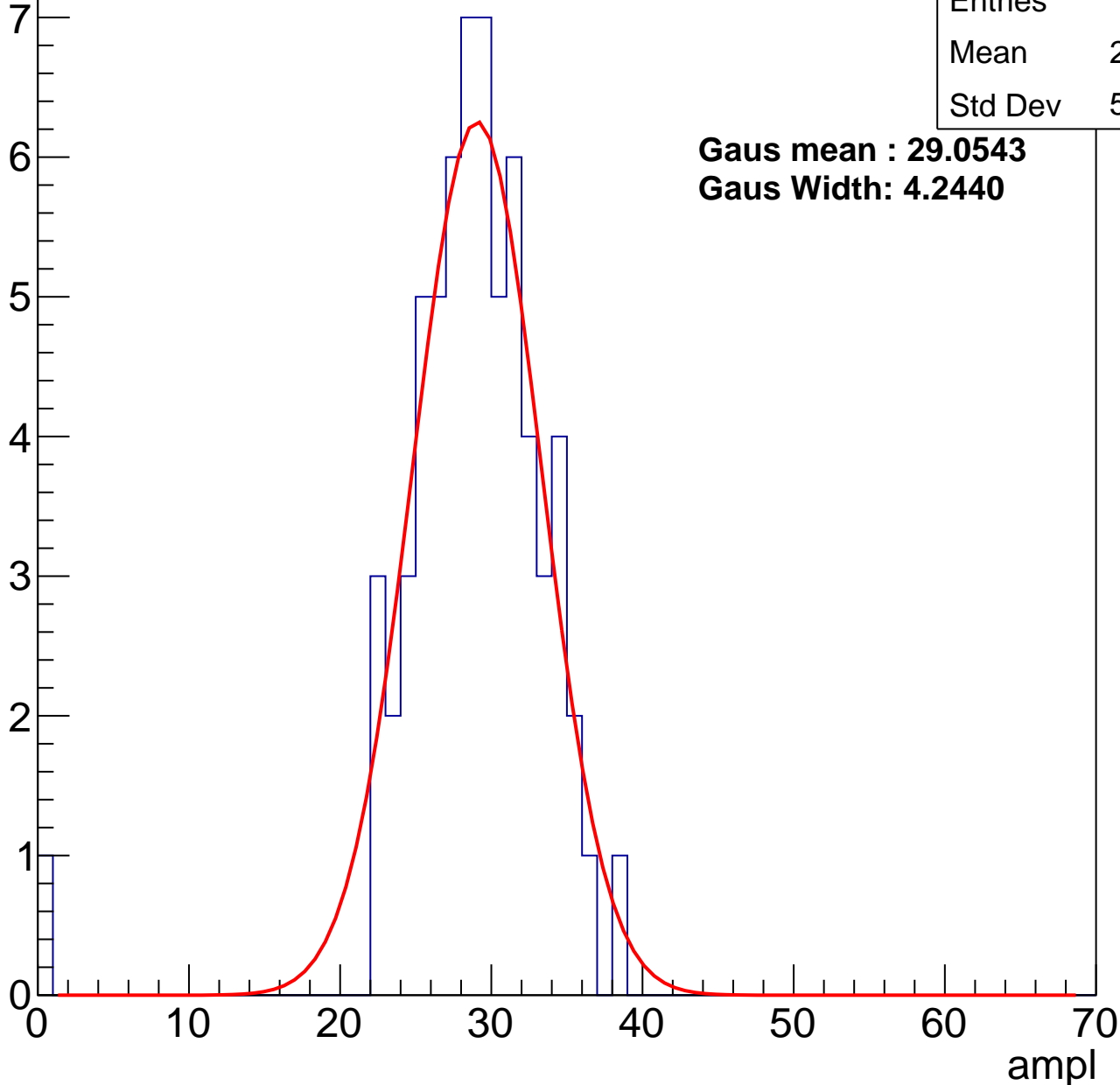
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	28.35
Std Dev	5.082

**Gaus mean : 29.0543**

**Gaus Width: 4.2440**



# B1L103S, U2-ch60, adc1

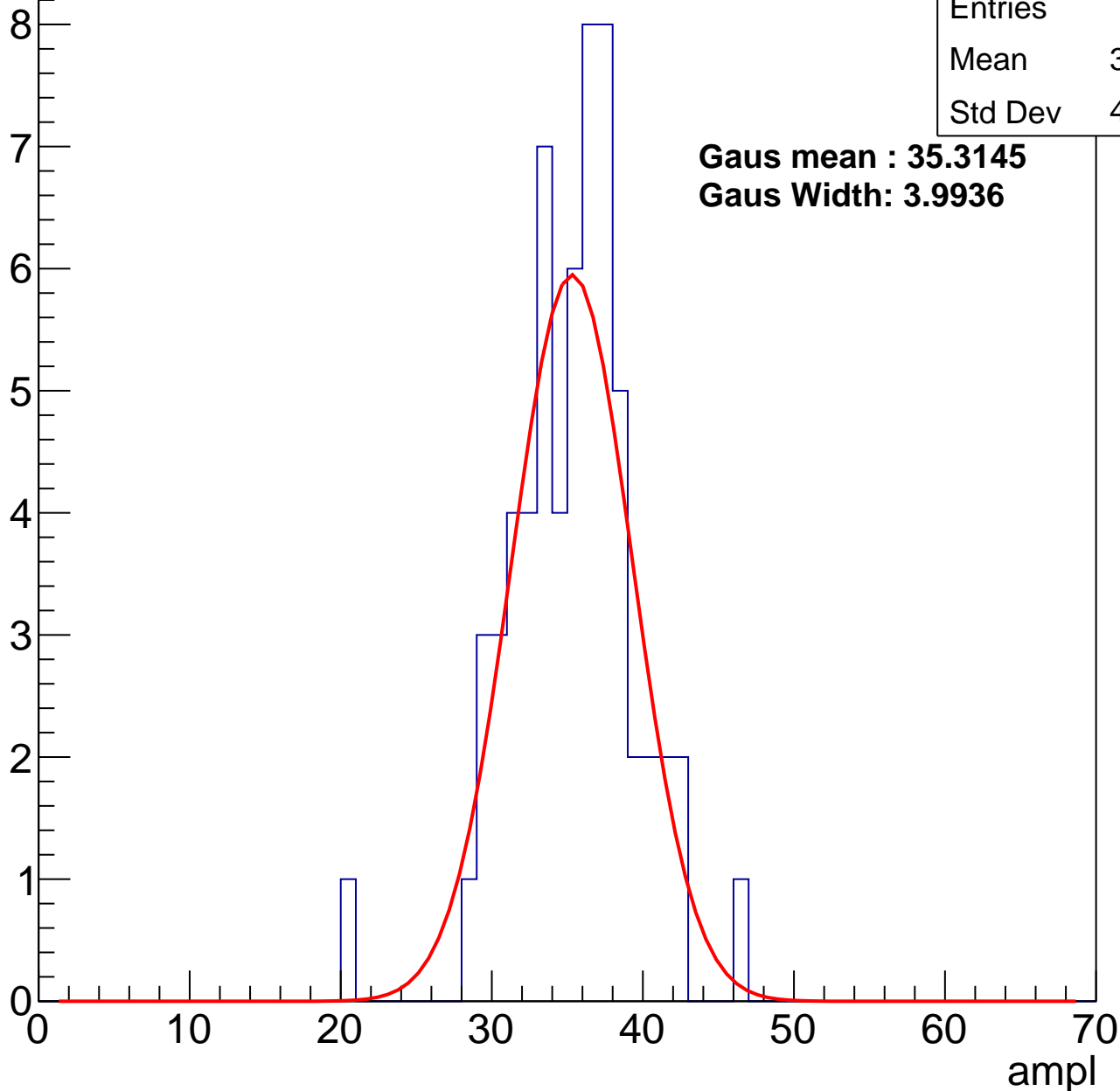
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	34.89
Std Dev	4.075

**Gaus mean : 35.3145**

**Gaus Width: 3.9936**



# B1L103S, U2-ch60, adc2

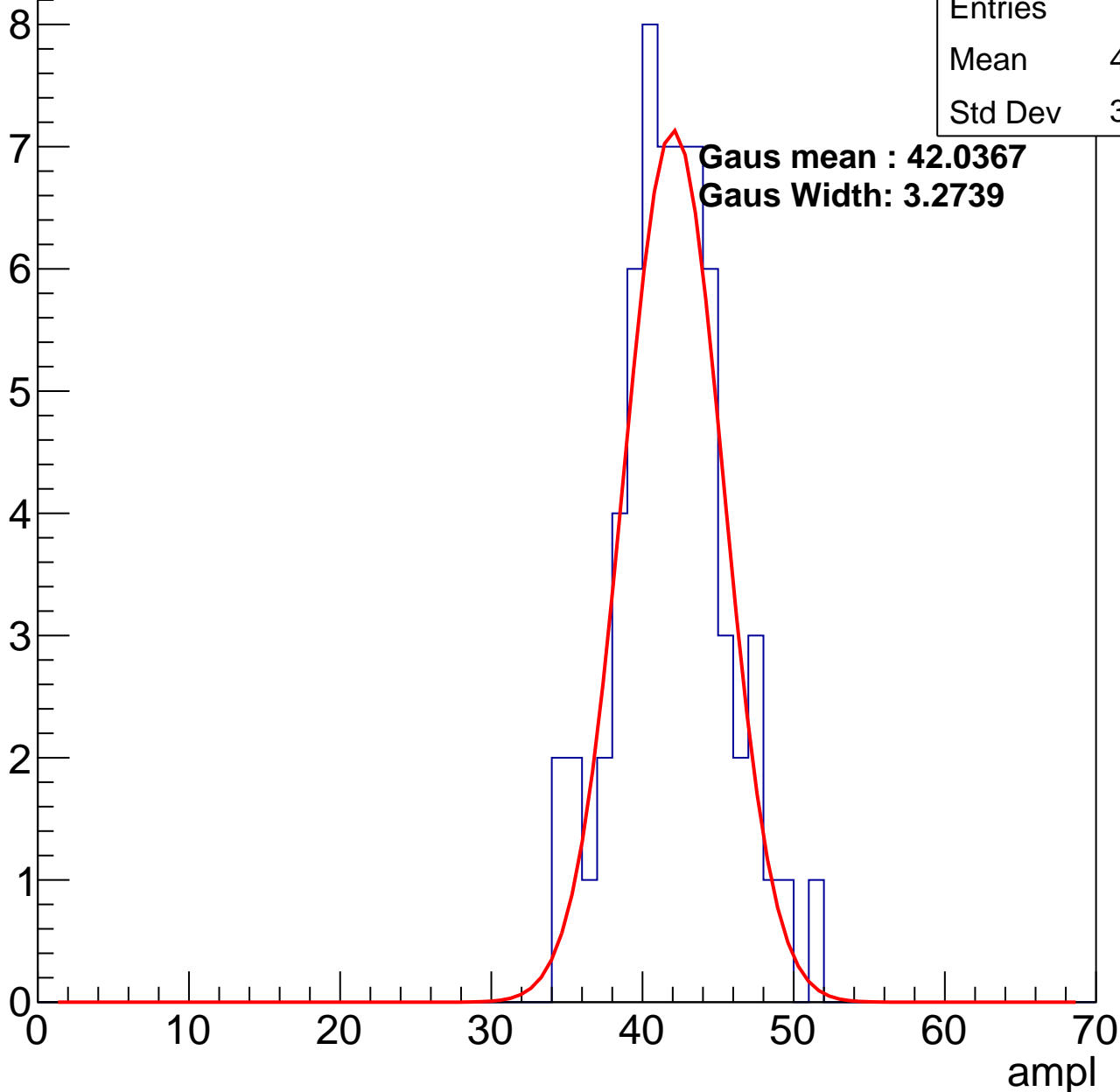
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	41.52
Std Dev	3.532

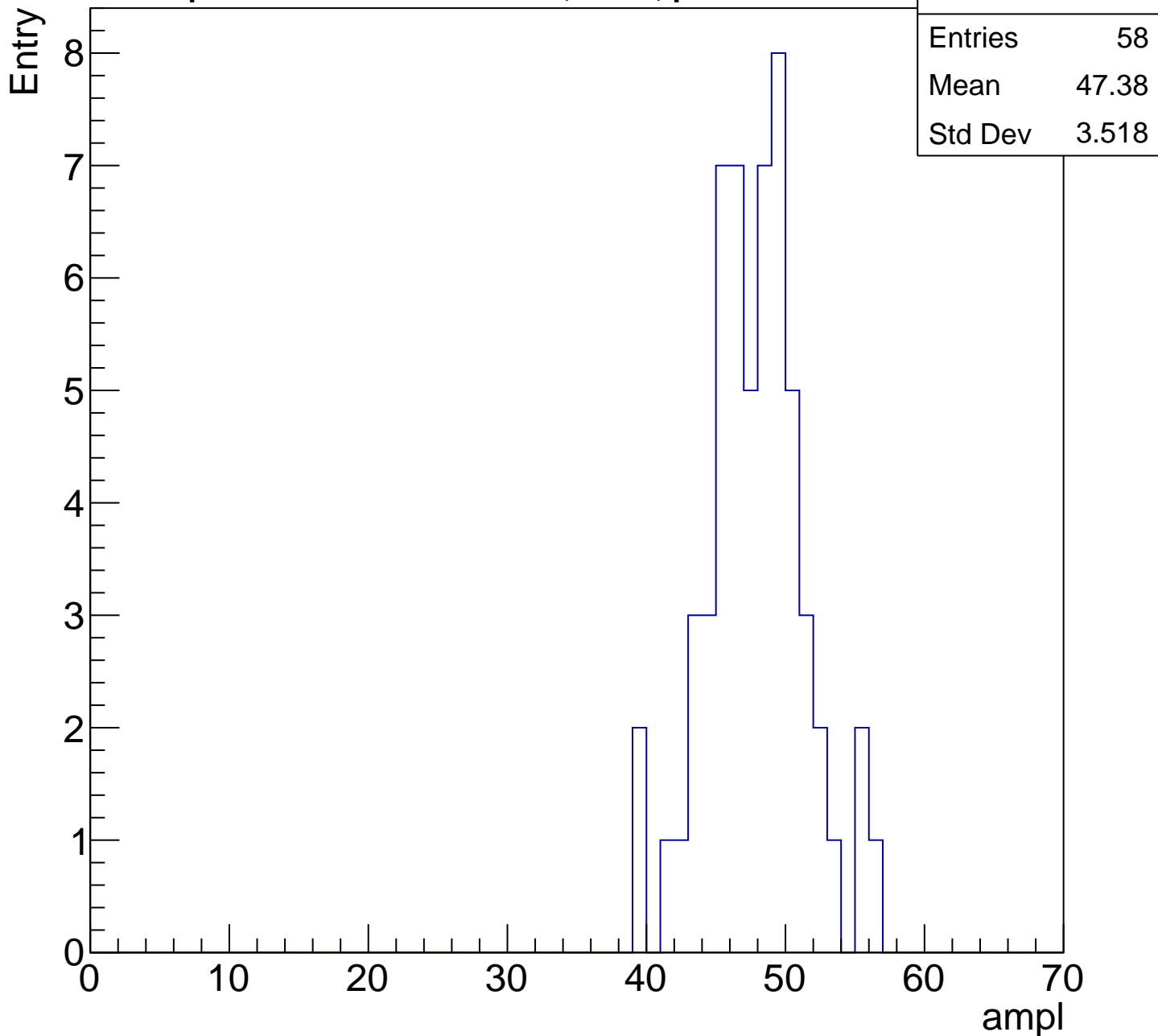
**Gaus mean : 42.0367**

**Gaus Width: 3.2739**



# B1L103S, U2-ch60, adc3

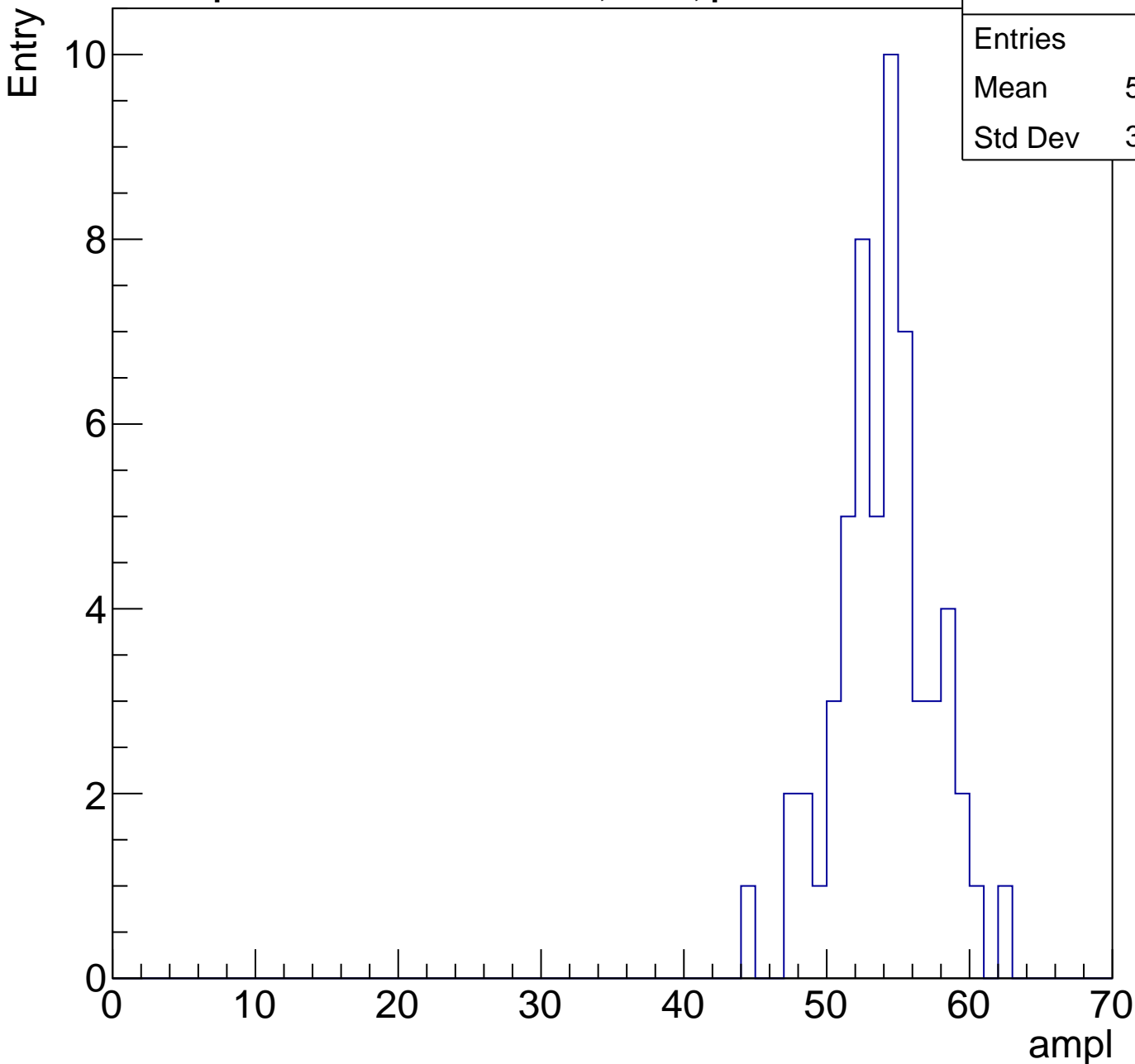
calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U2-ch60, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	58
Mean	53.53
Std Dev	3.405

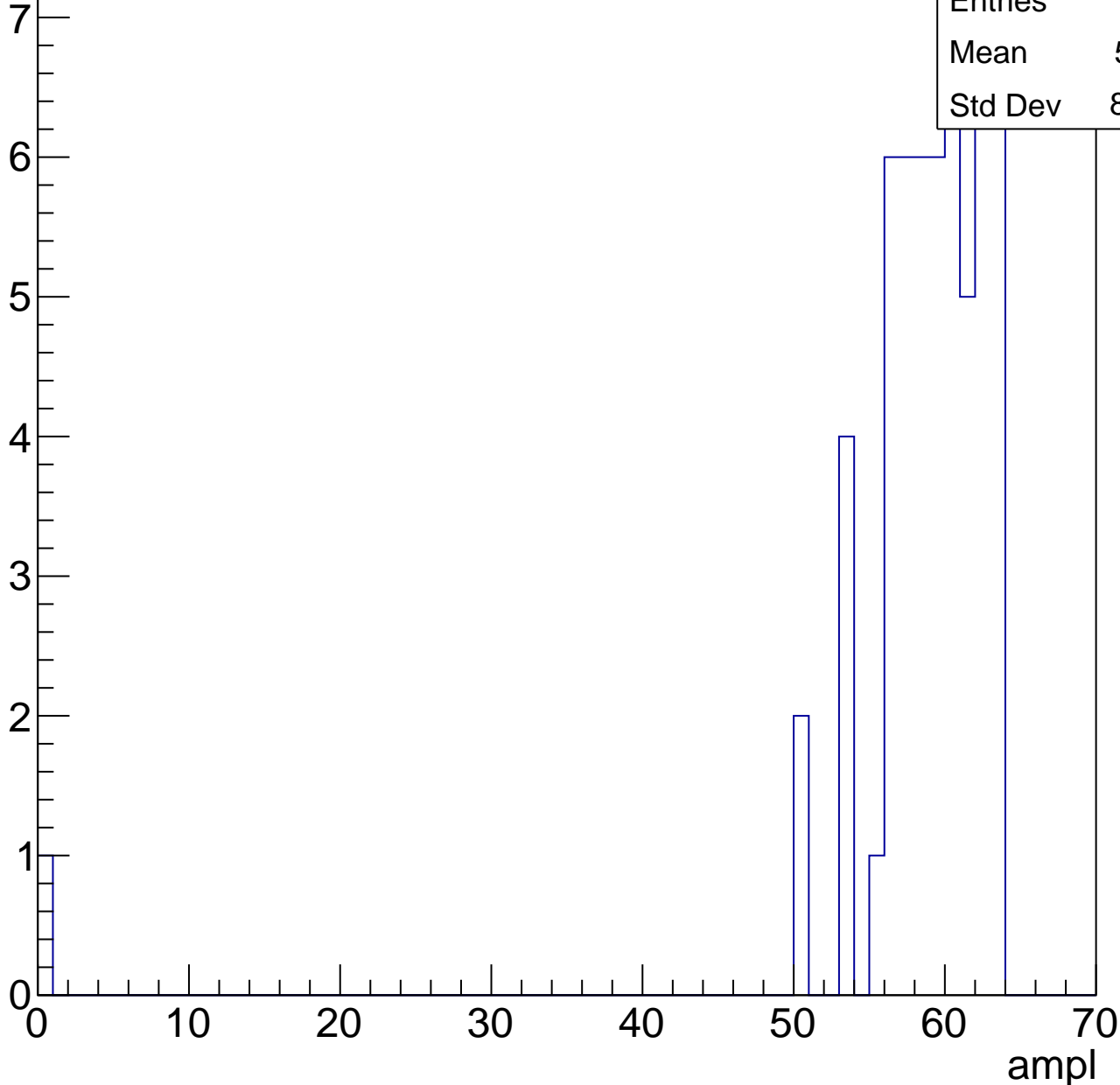


# B1L103S, U2-ch60, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	57.71
Std Dev	8.296

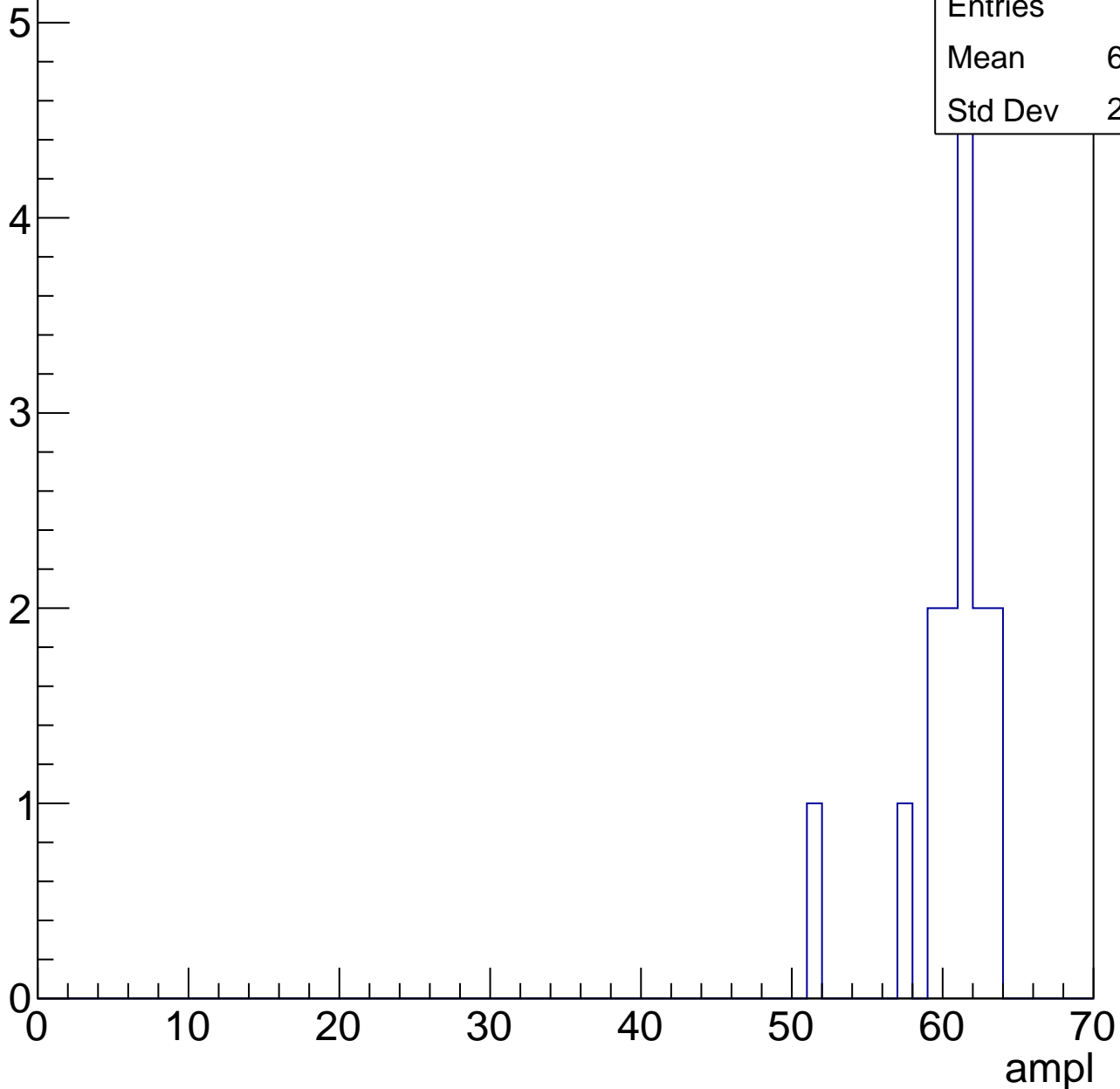


# B1L103S, U2-ch60, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	15
Mean	60.07
Std Dev	2.863





# B1L103S, U2-ch60, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	3
Mean	21
Std Dev	29.7

# B1L103S, U2-ch61, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	74
Mean	29.46
Std Dev	4.725

**Gaus mean : 30.4083**

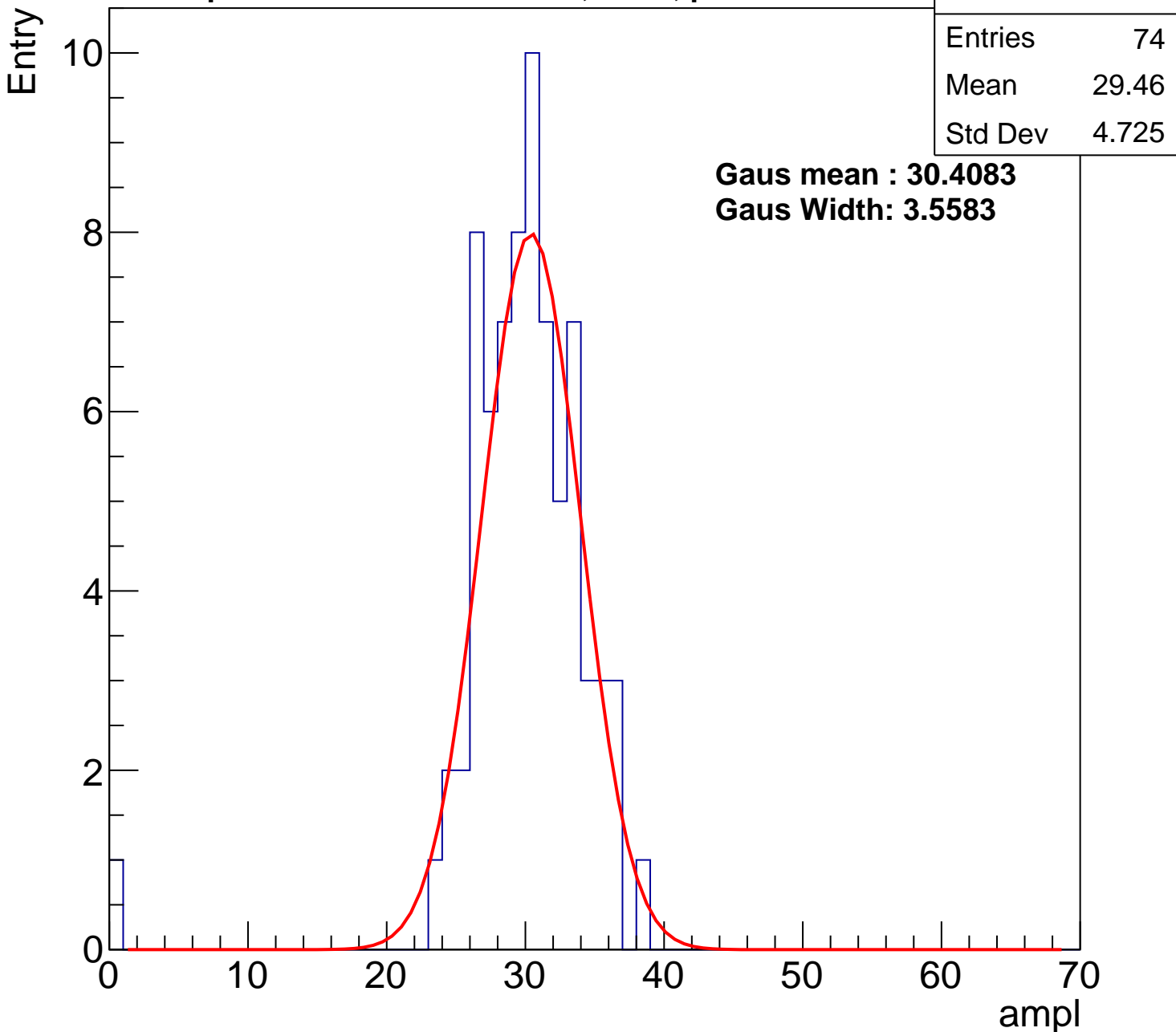
**Gaus Width: 3.5583**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U2-ch61, adc1

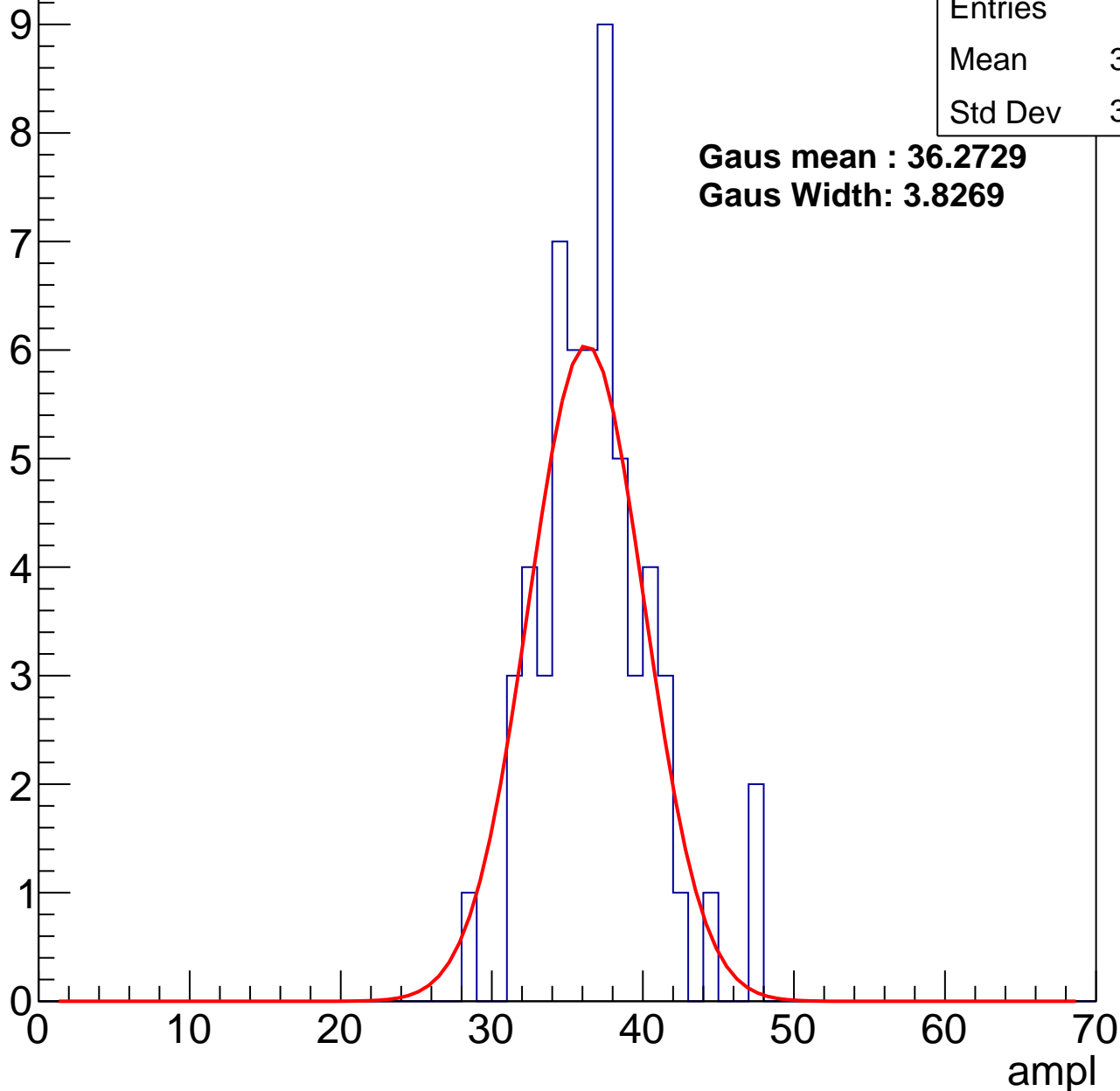
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	36.47
Std Dev	3.687

**Gaus mean : 36.2729**

**Gaus Width: 3.8269**



# B1L103S, U2-ch61, adc2

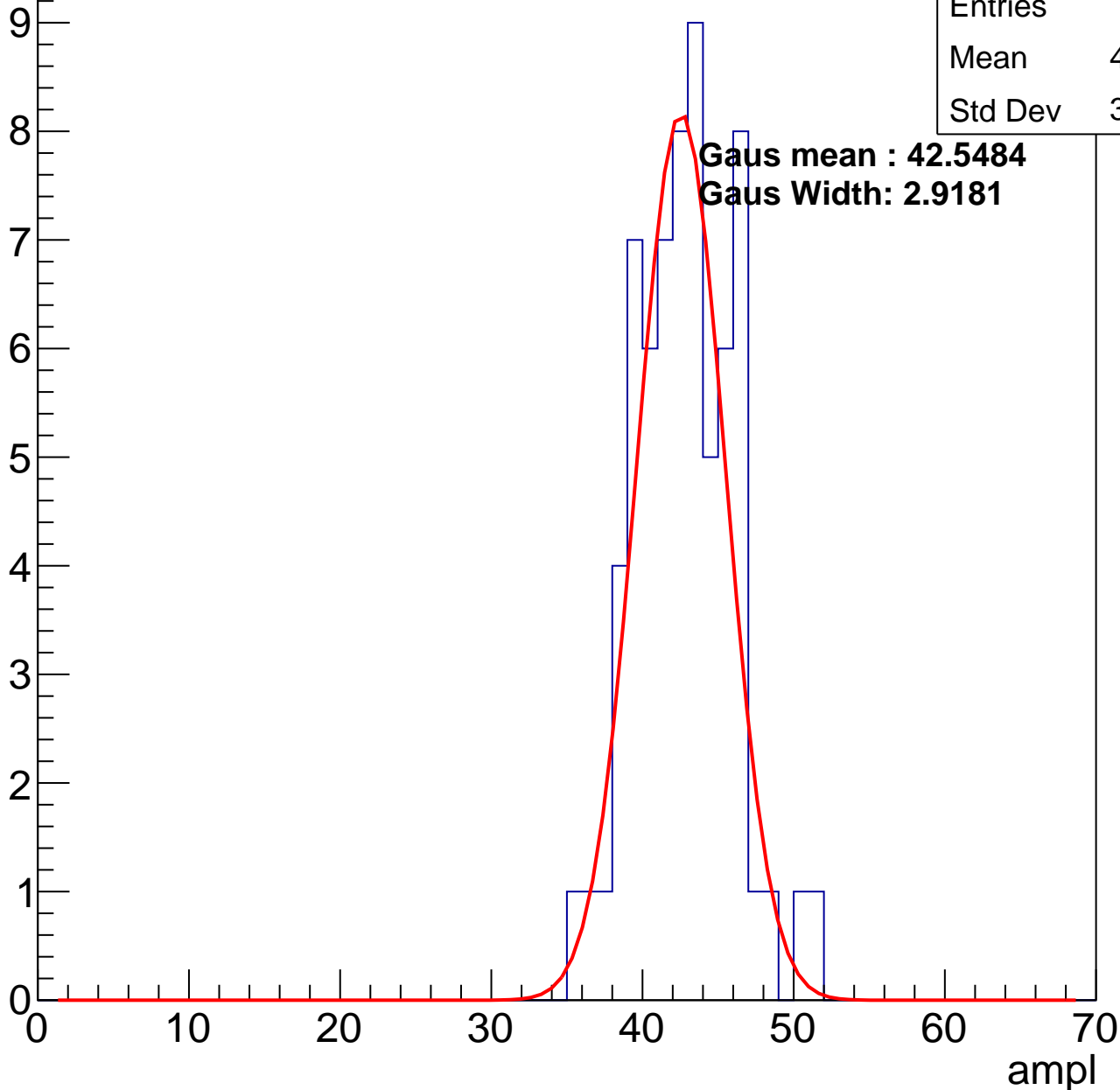
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	42.34
Std Dev	3.179

**Gaus mean : 42.5484**

**Gaus Width: 2.9181**

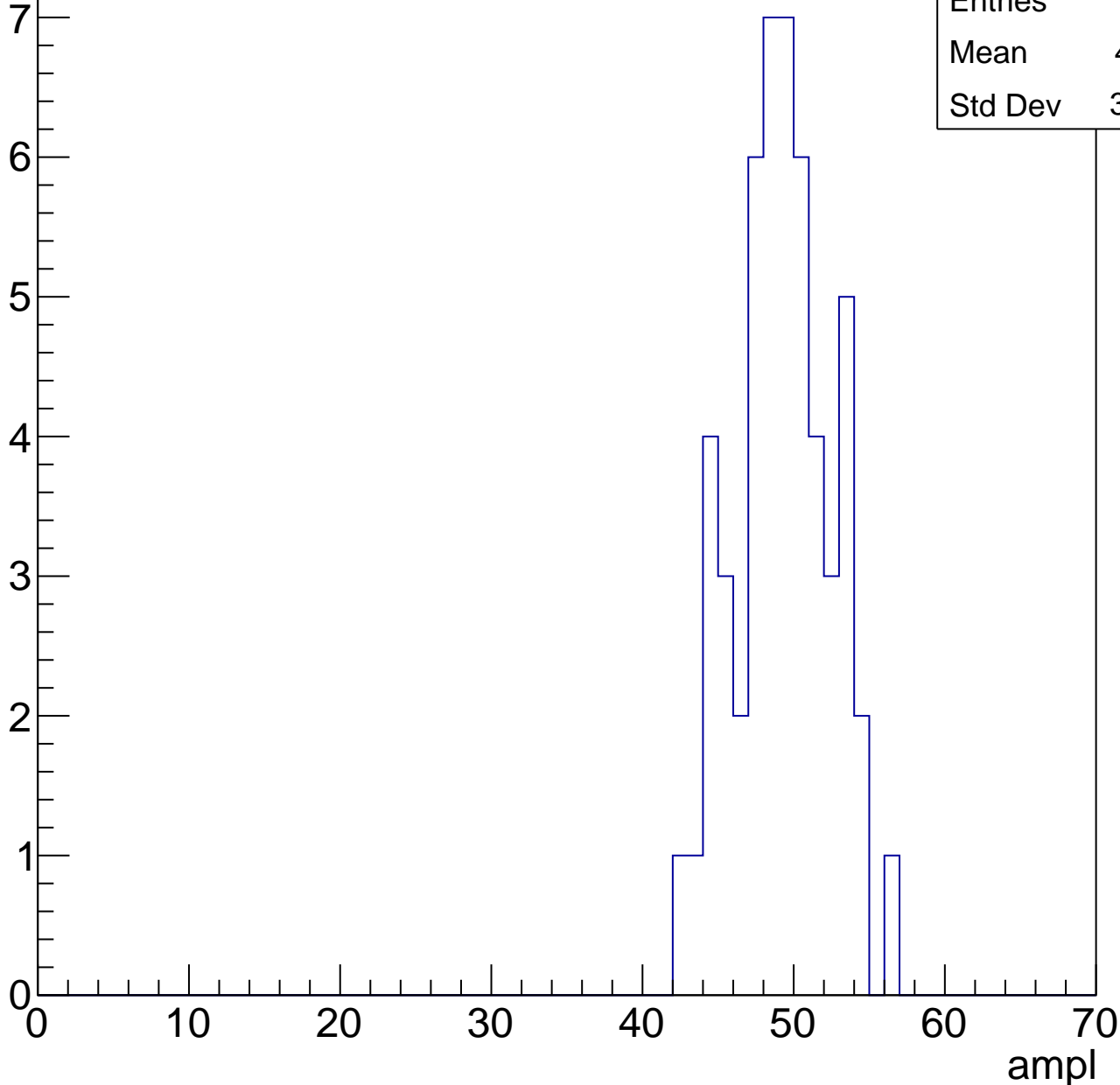


# B1L103S, U2-ch61, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	48.81
Std Dev	3.126

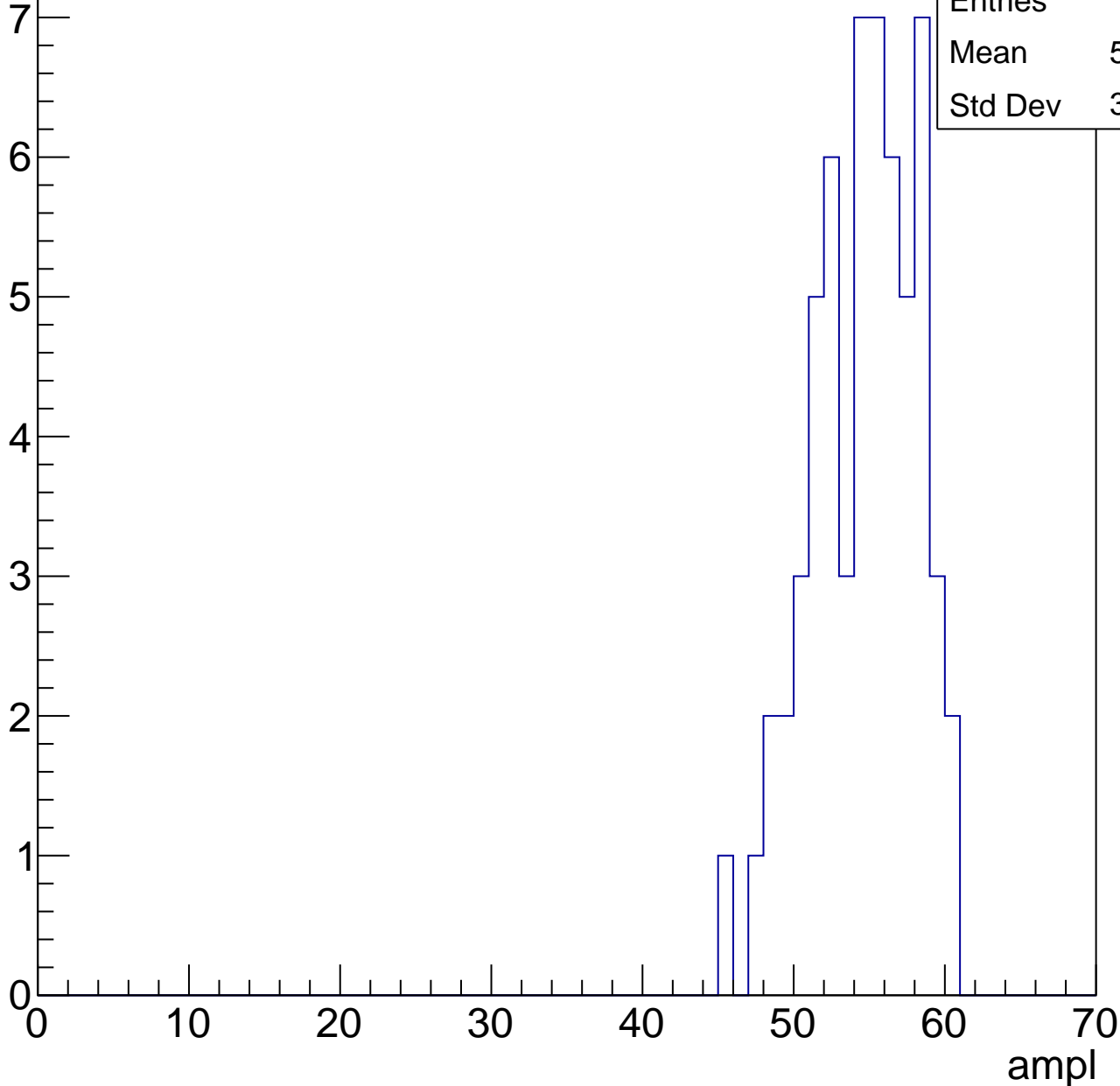


# B1L103S, U2-ch61, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	54.15
Std Dev	3.429



# B1L103S, U2-ch61, adc5

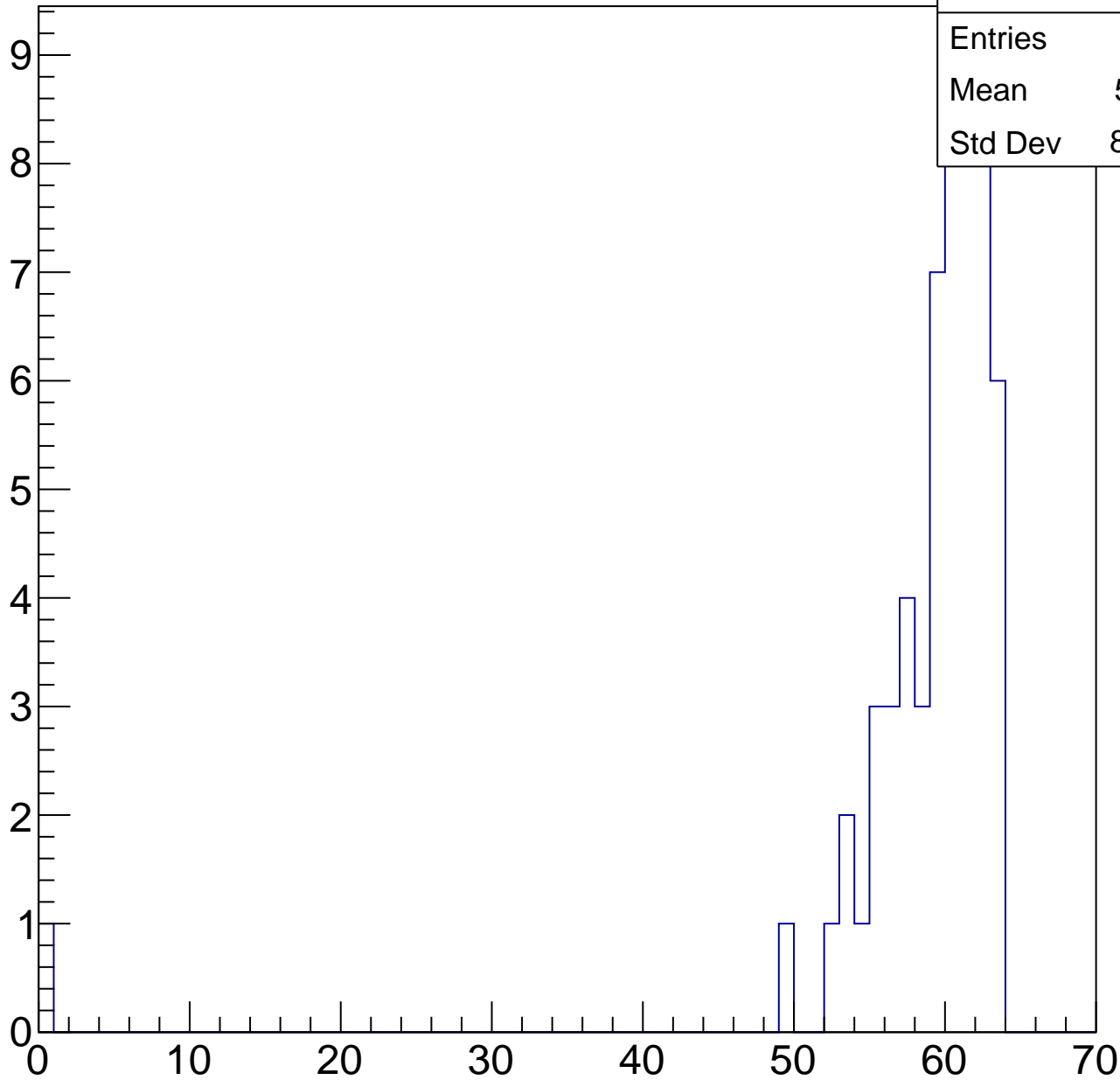
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	57
Mean	58.11
Std Dev	8.364

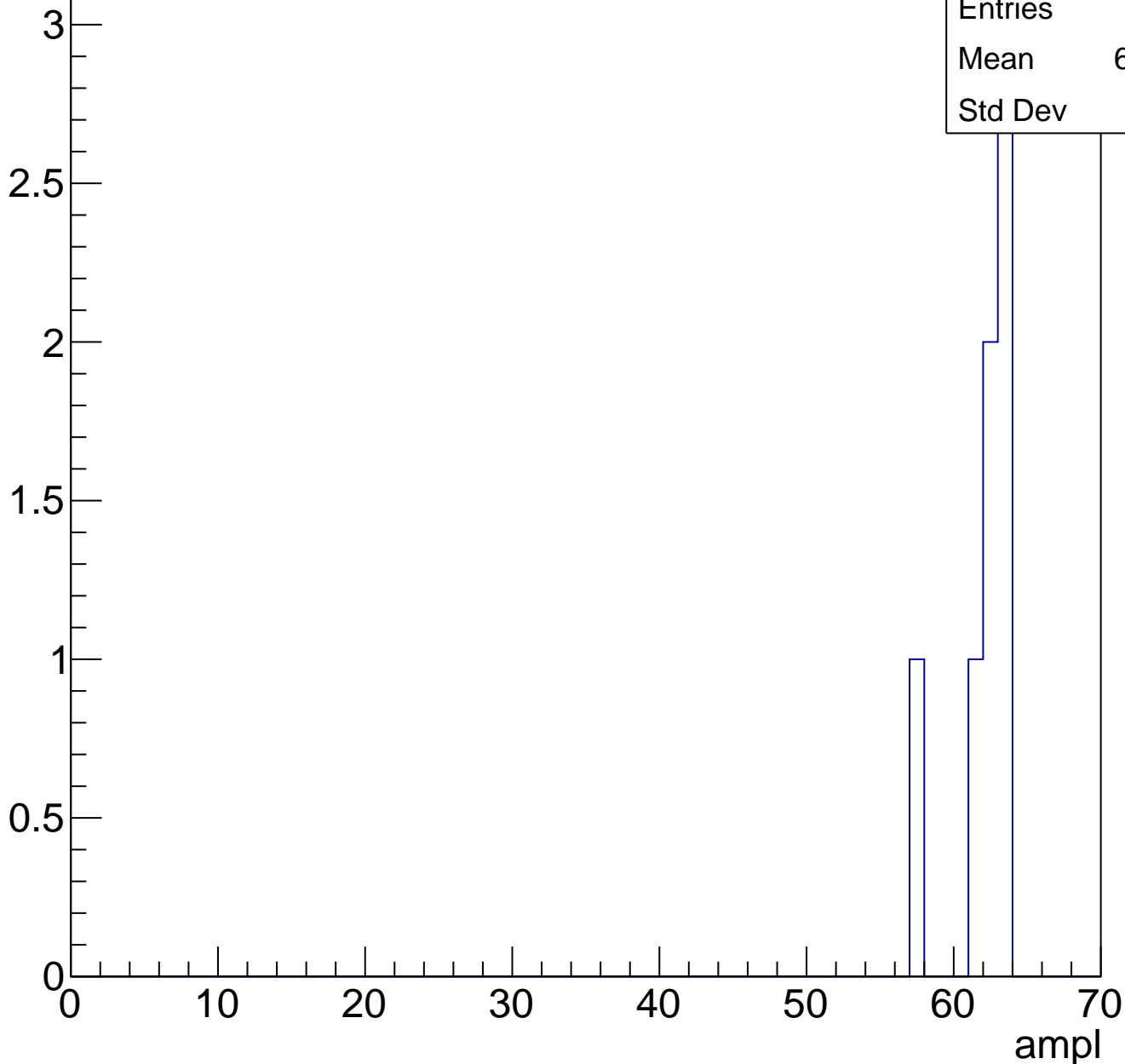
ampl



# B1L103S, U2-ch61, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U2-ch61, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch62, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	80
Mean	26.36
Std Dev	7.063

**Gaus mean : 28.2139**

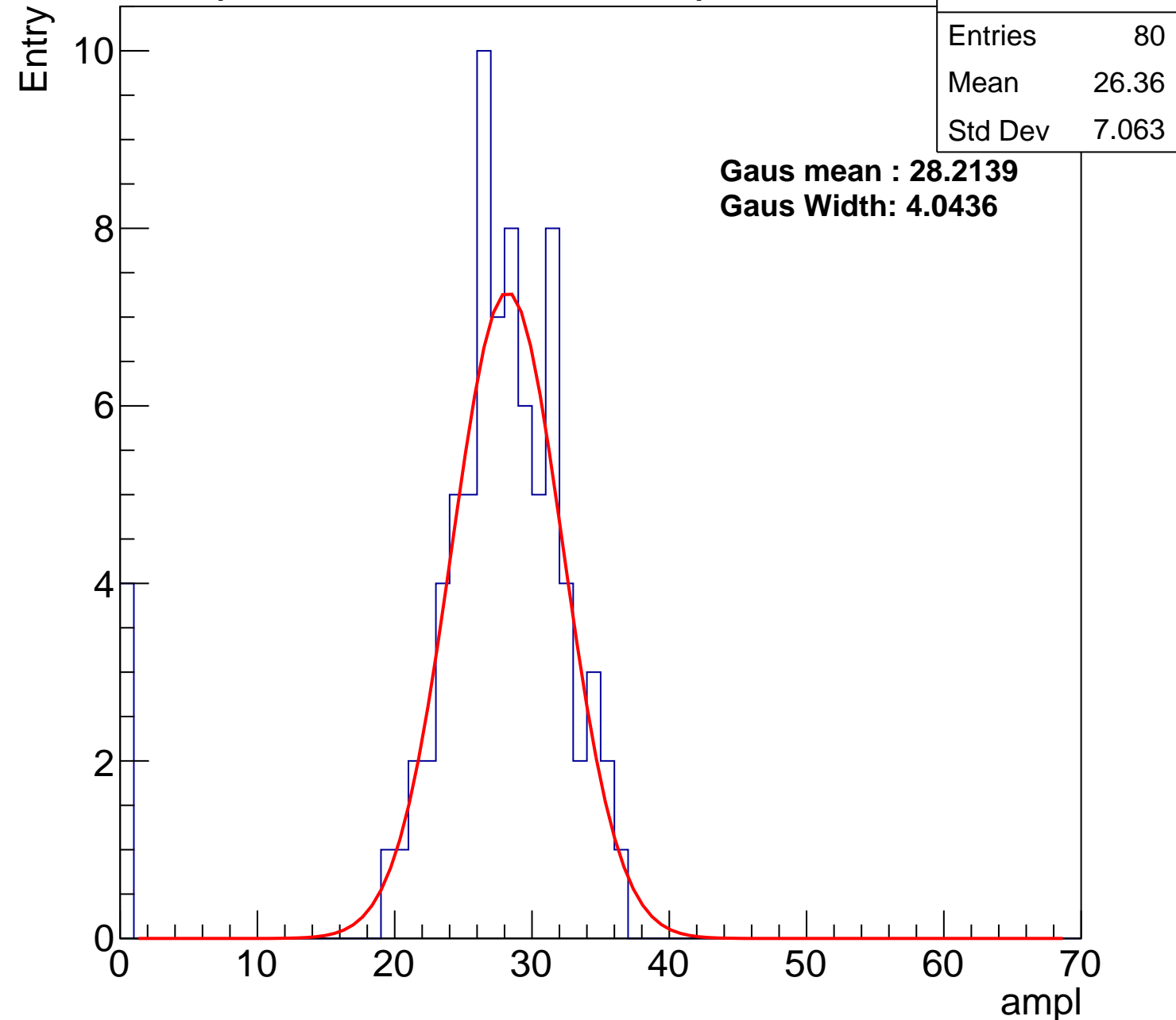
**Gaus Width: 4.0436**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U2-ch62, adc1

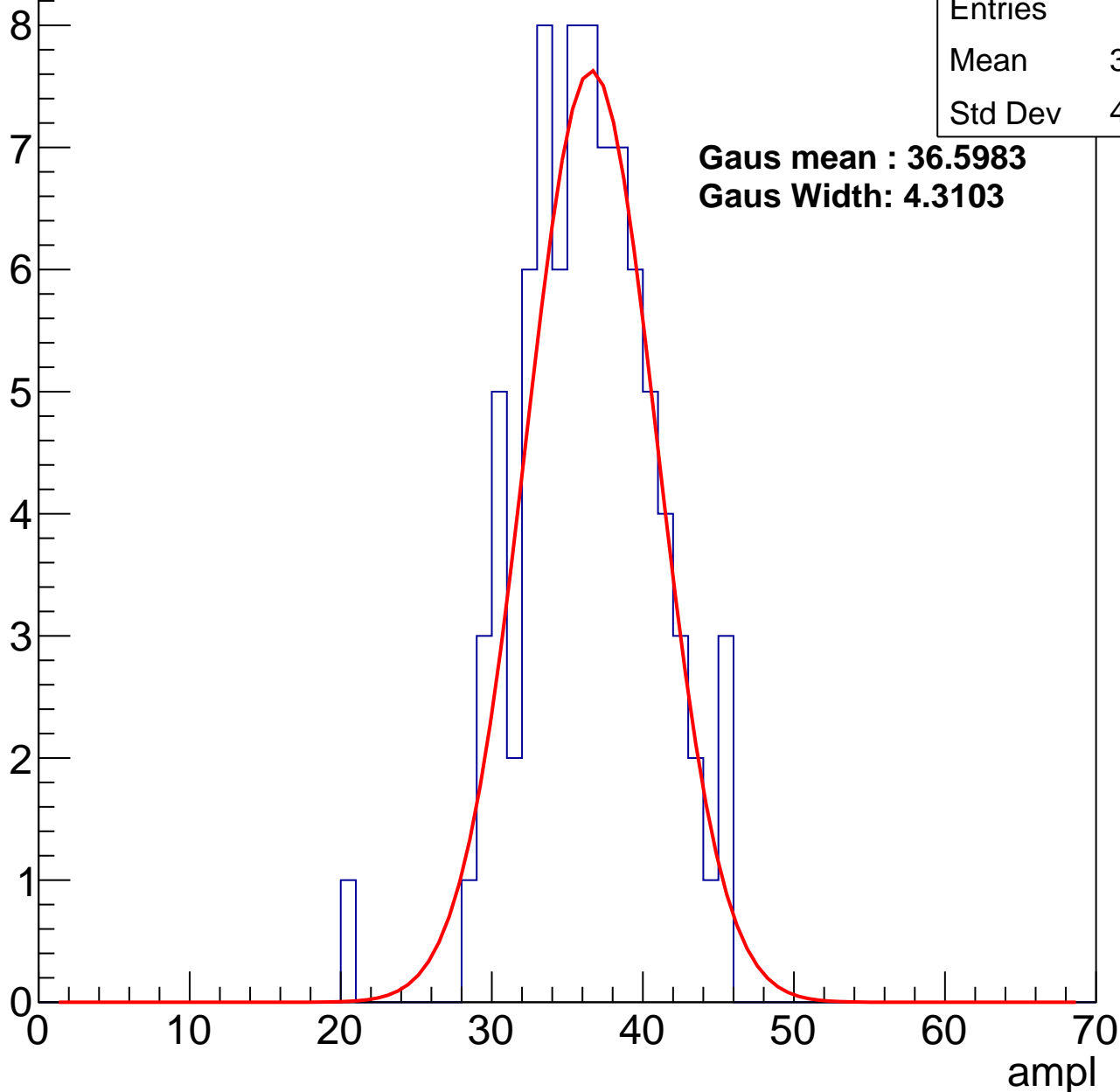
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	86
Mean	35.92
Std Dev	4.418

**Gaus mean : 36.5983**

**Gaus Width: 4.3103**



# B1L103S, U2-ch62, adc2

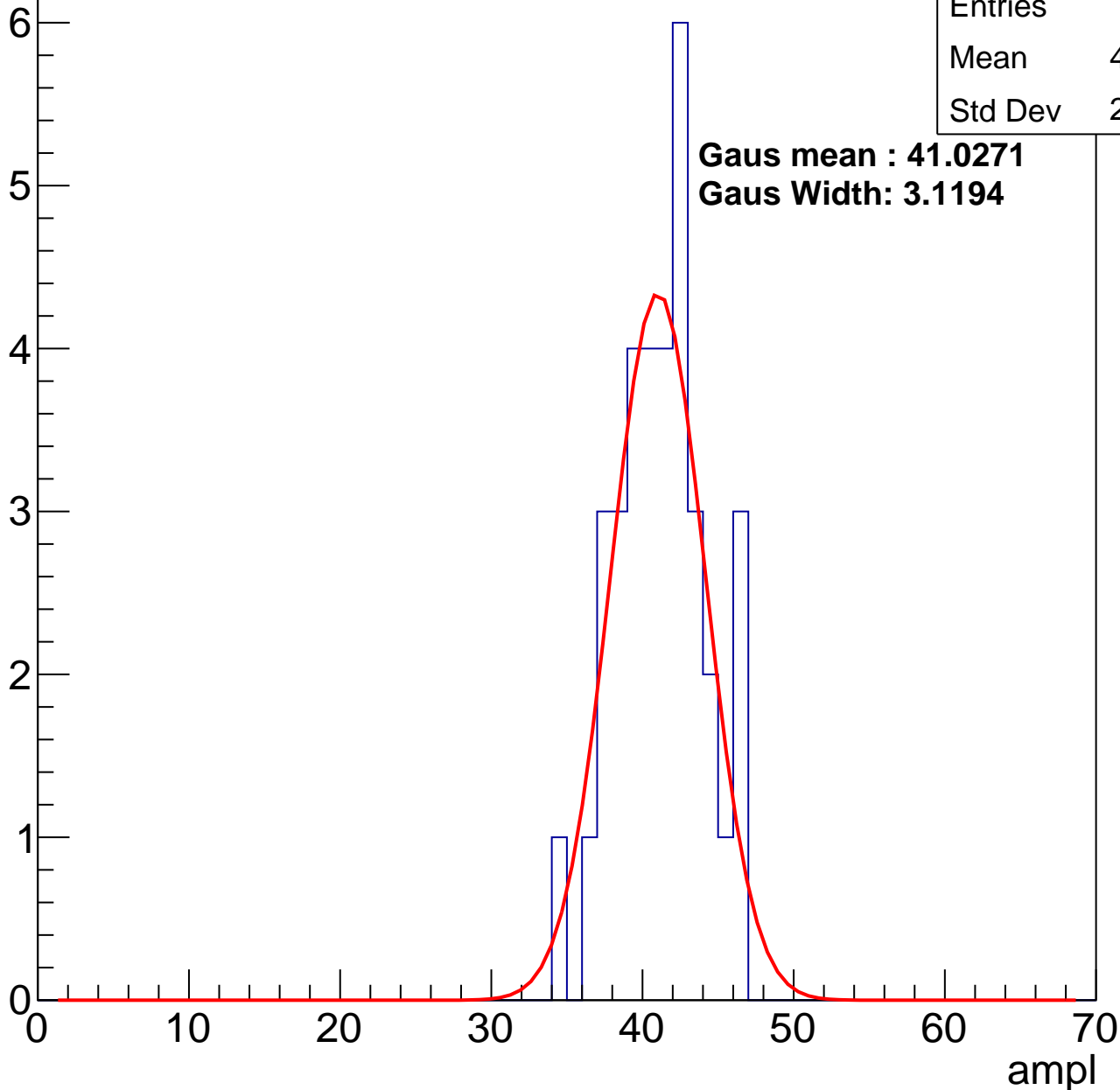
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	35
Mean	40.77
Std Dev	2.899

**Gaus mean : 41.0271**

**Gaus Width: 3.1194**

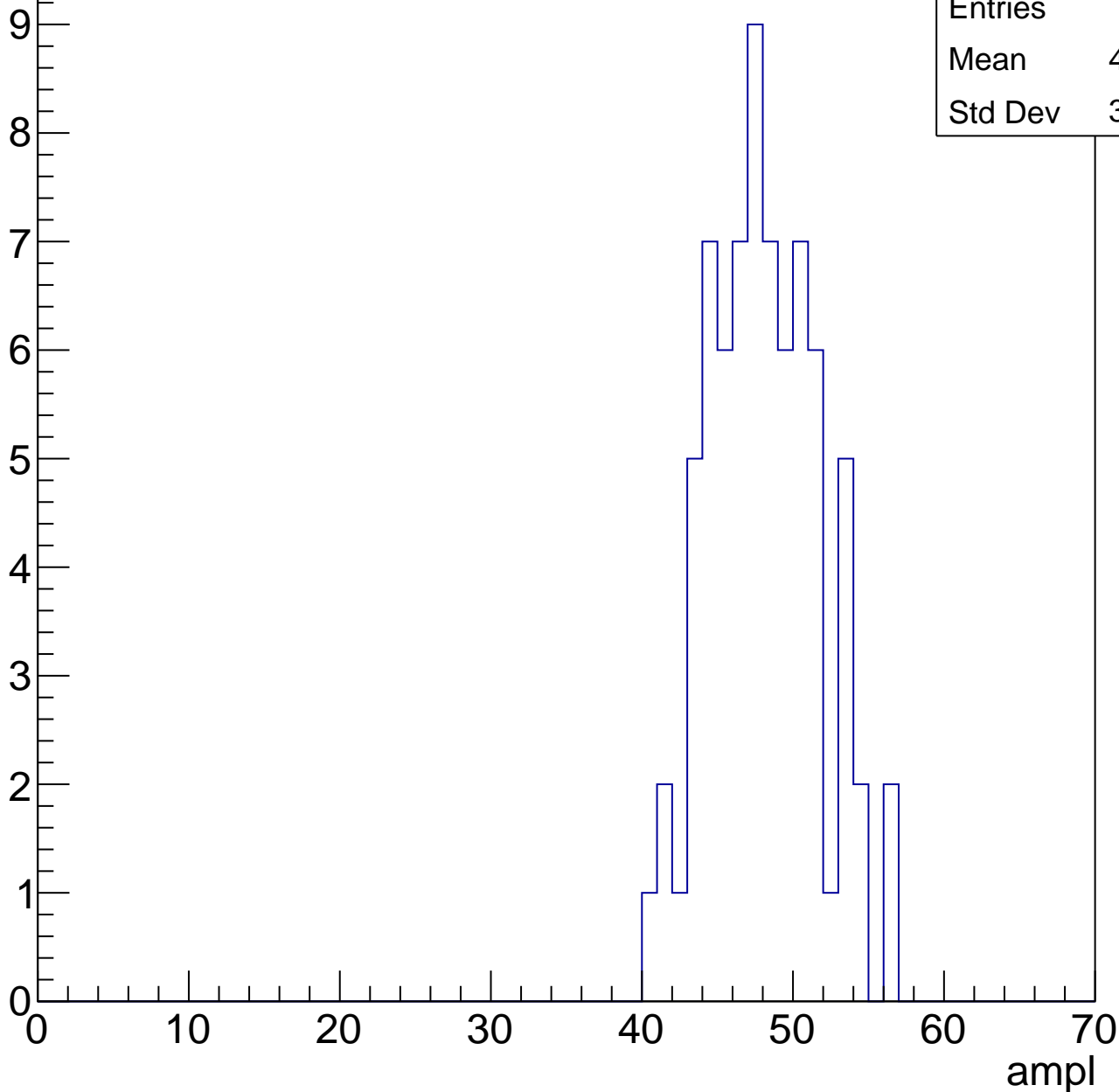


# B1L103S, U2-ch62, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	47.64
Std Dev	3.574

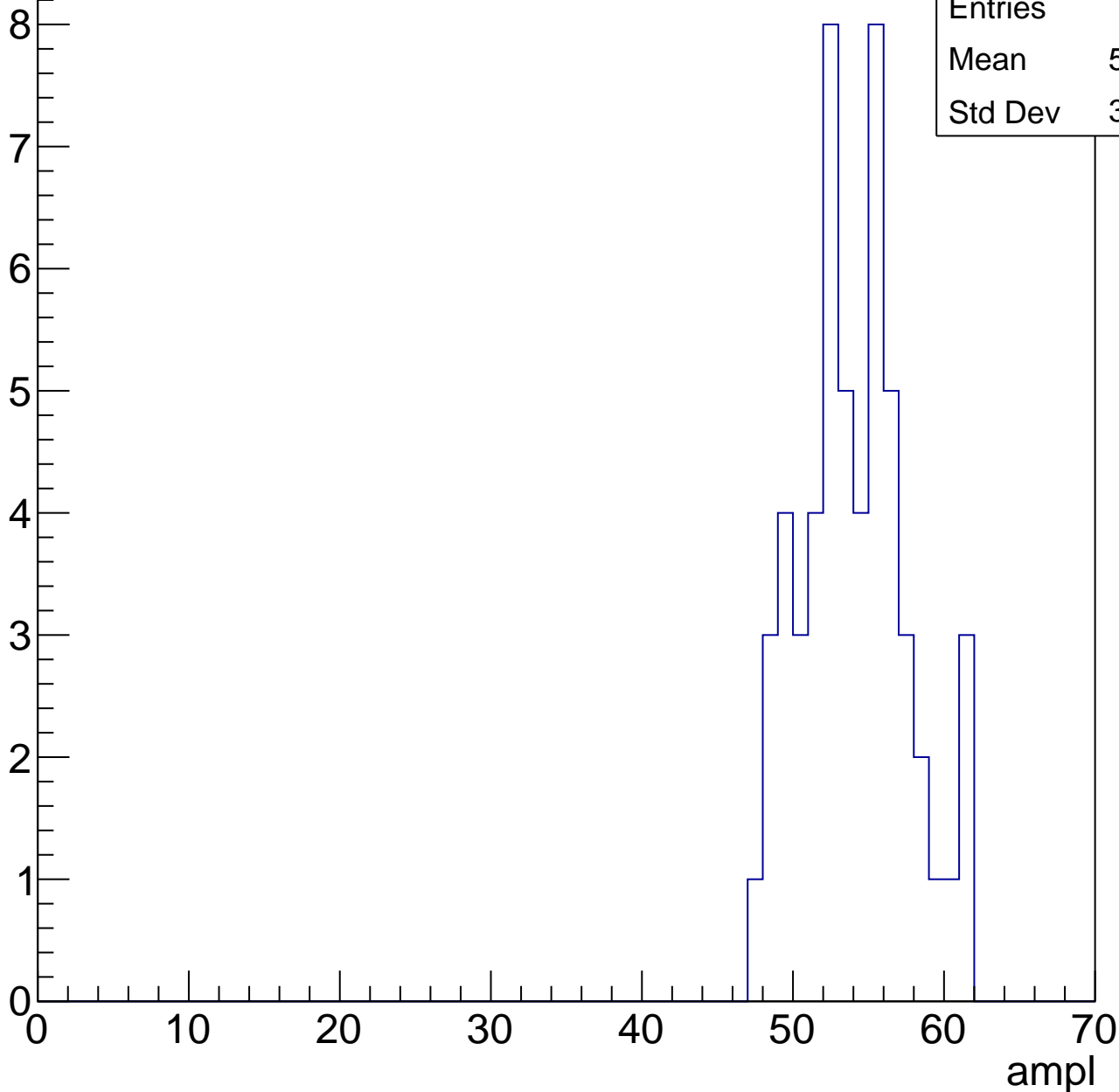


# B1L103S, U2-ch62, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

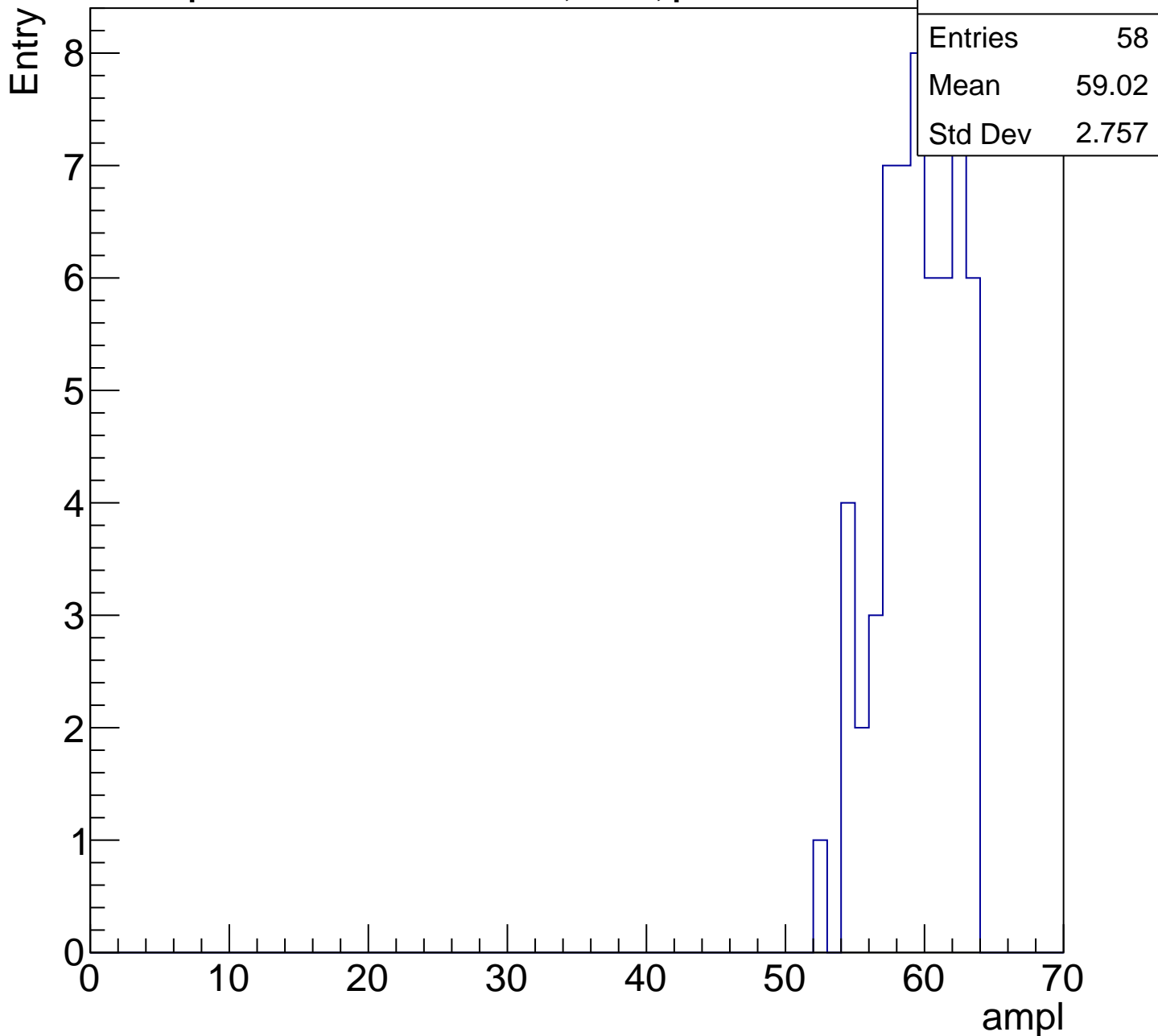
Entry

Entries	55
Mean	53.58
Std Dev	3.473



# B1L103S, U2-ch62, adc5

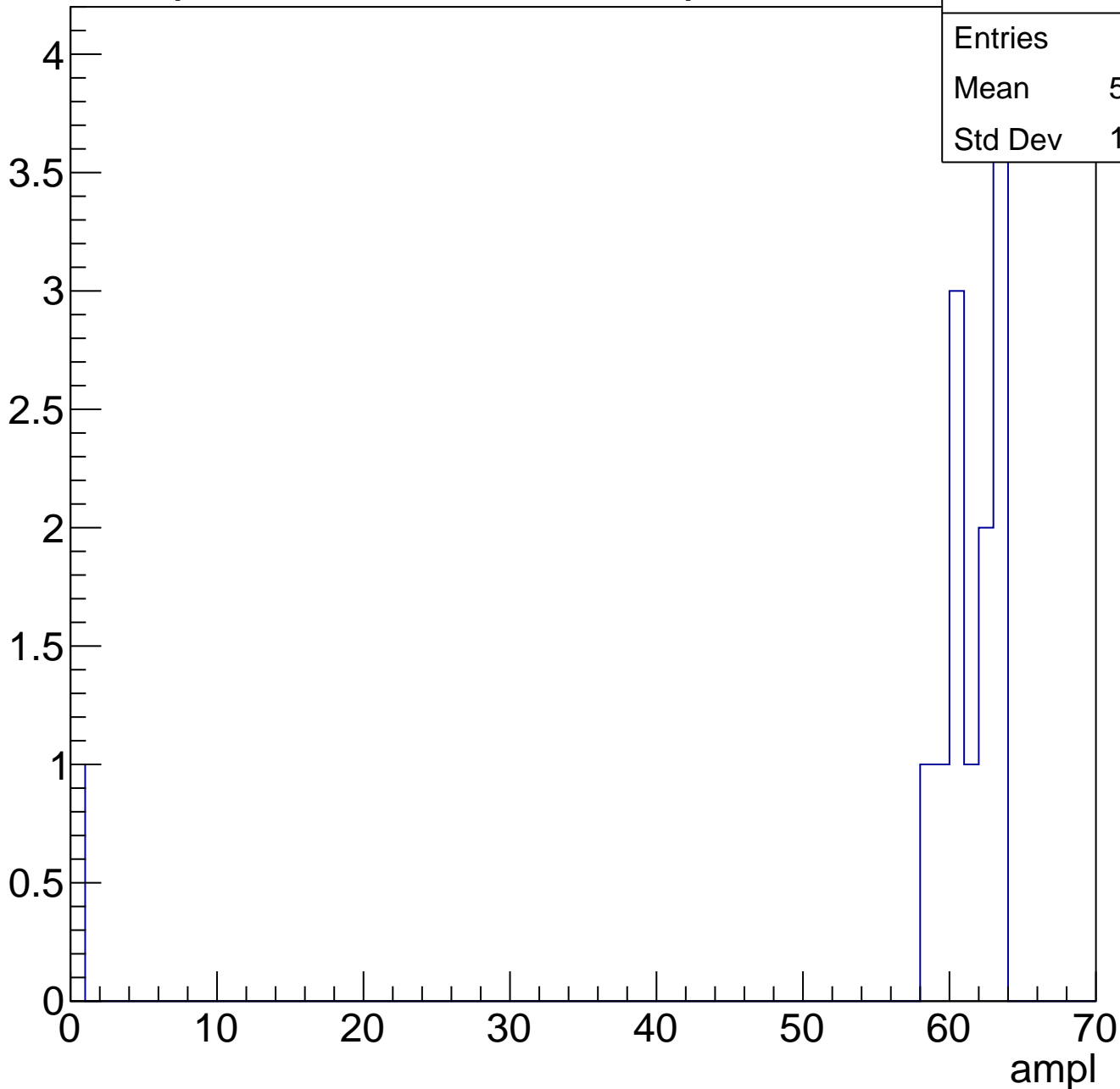
calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U2-ch62, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U2-ch62, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

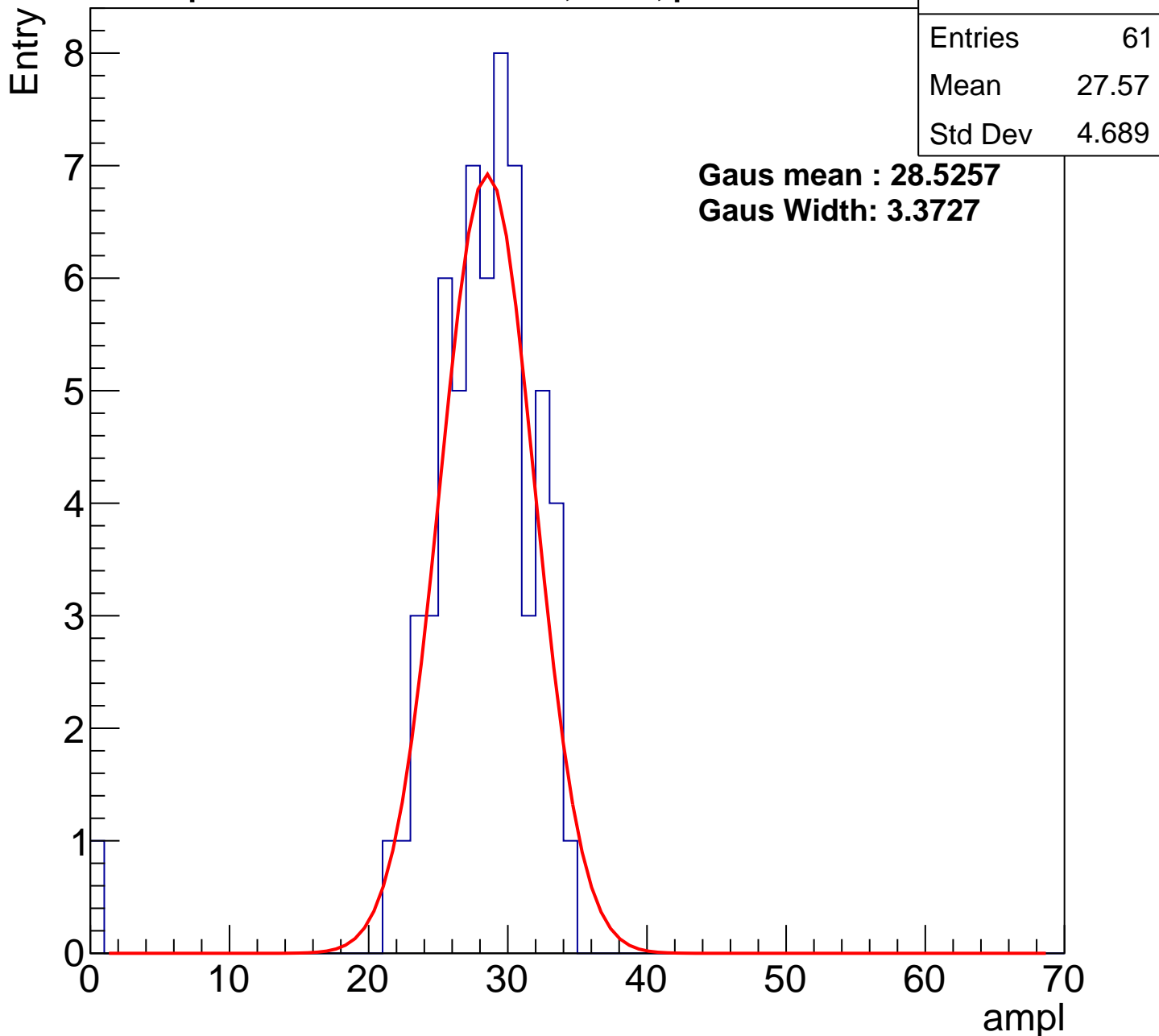
Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U2-ch63, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U2-ch63, adc1

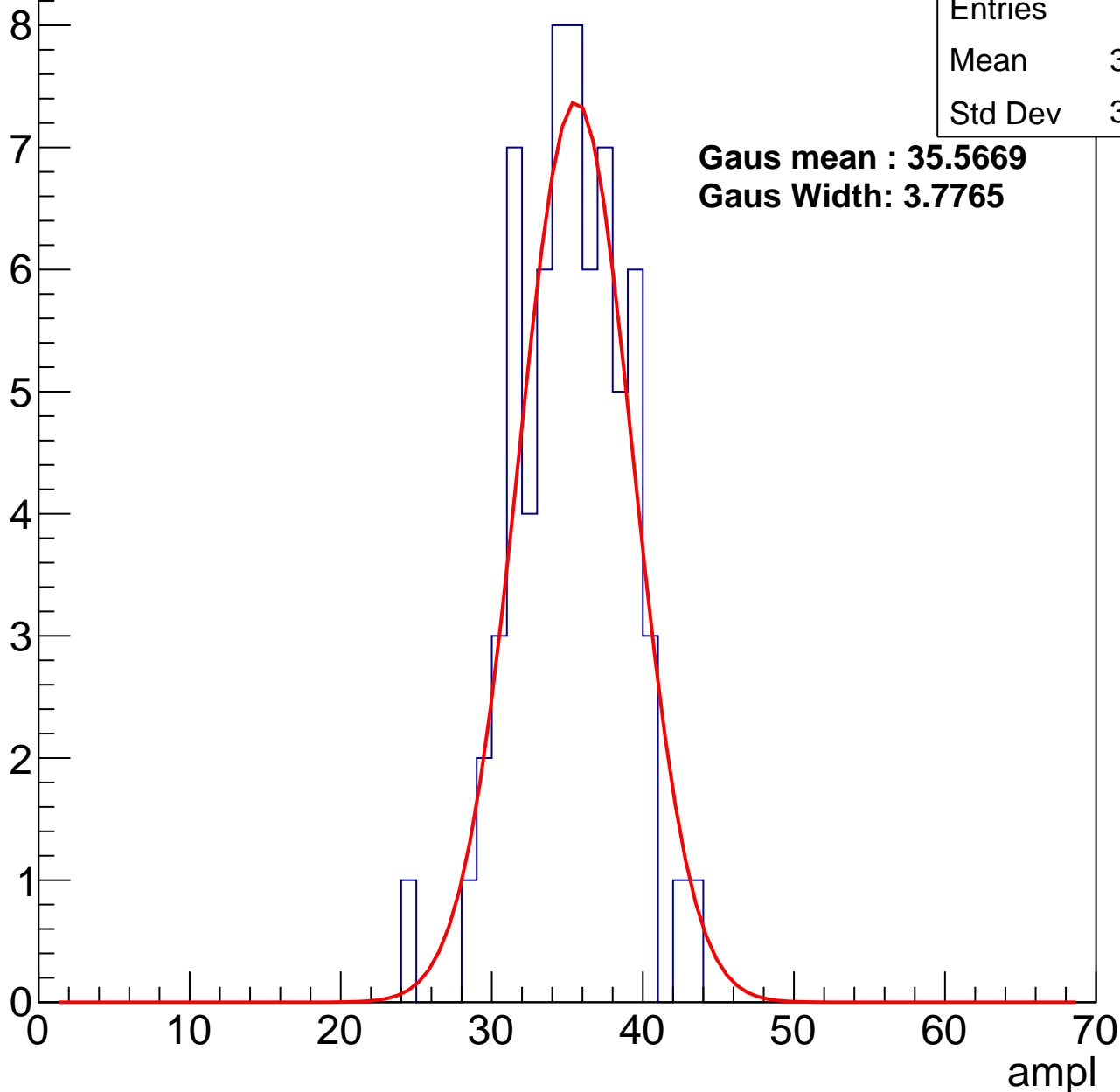
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	34.77
Std Dev	3.523

**Gaus mean : 35.5669**

**Gaus Width: 3.7765**



# B1L103S, U2-ch63, adc2

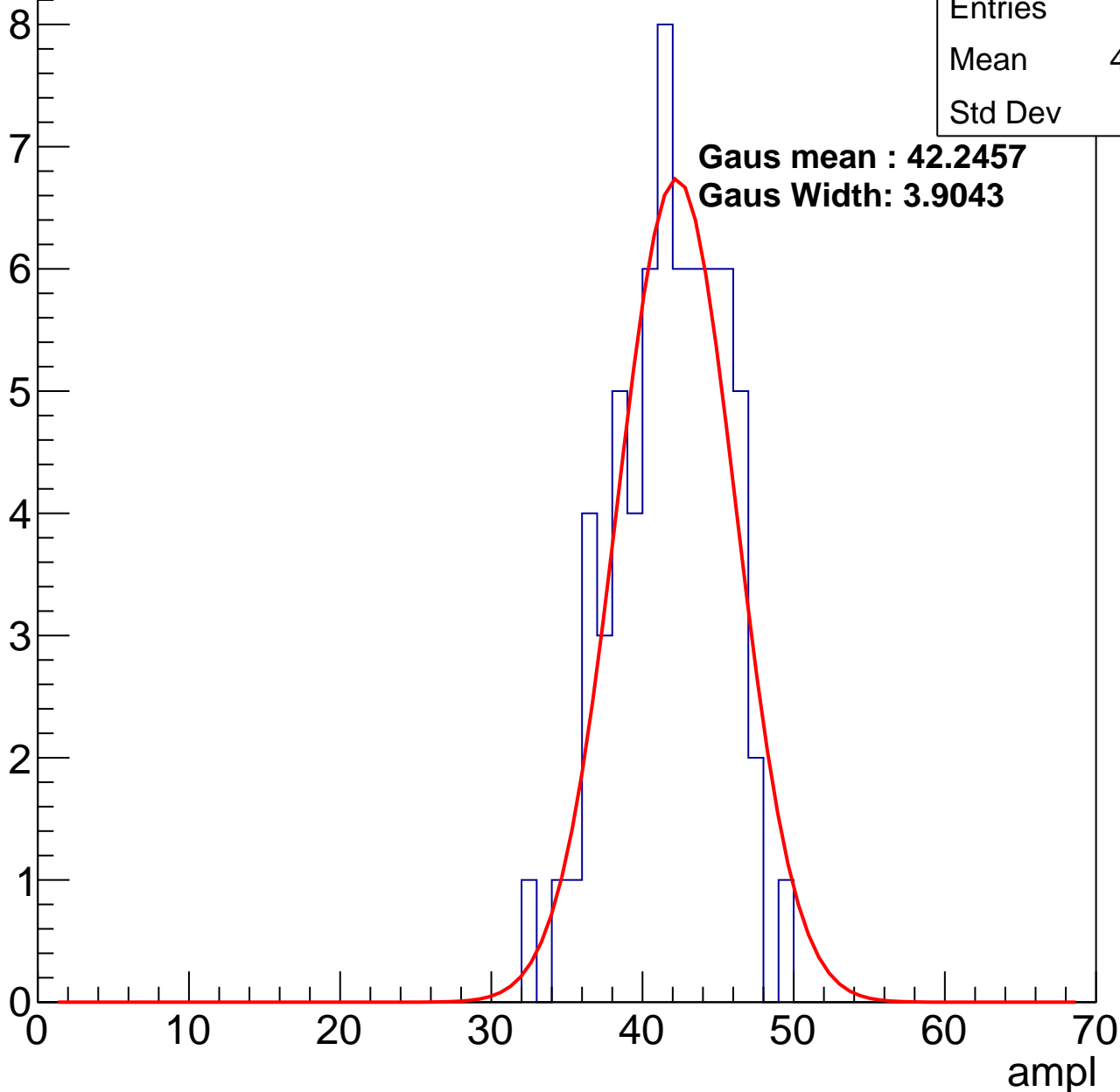
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	41.34
Std Dev	3.54

**Gaus mean : 42.2457**

**Gaus Width: 3.9043**

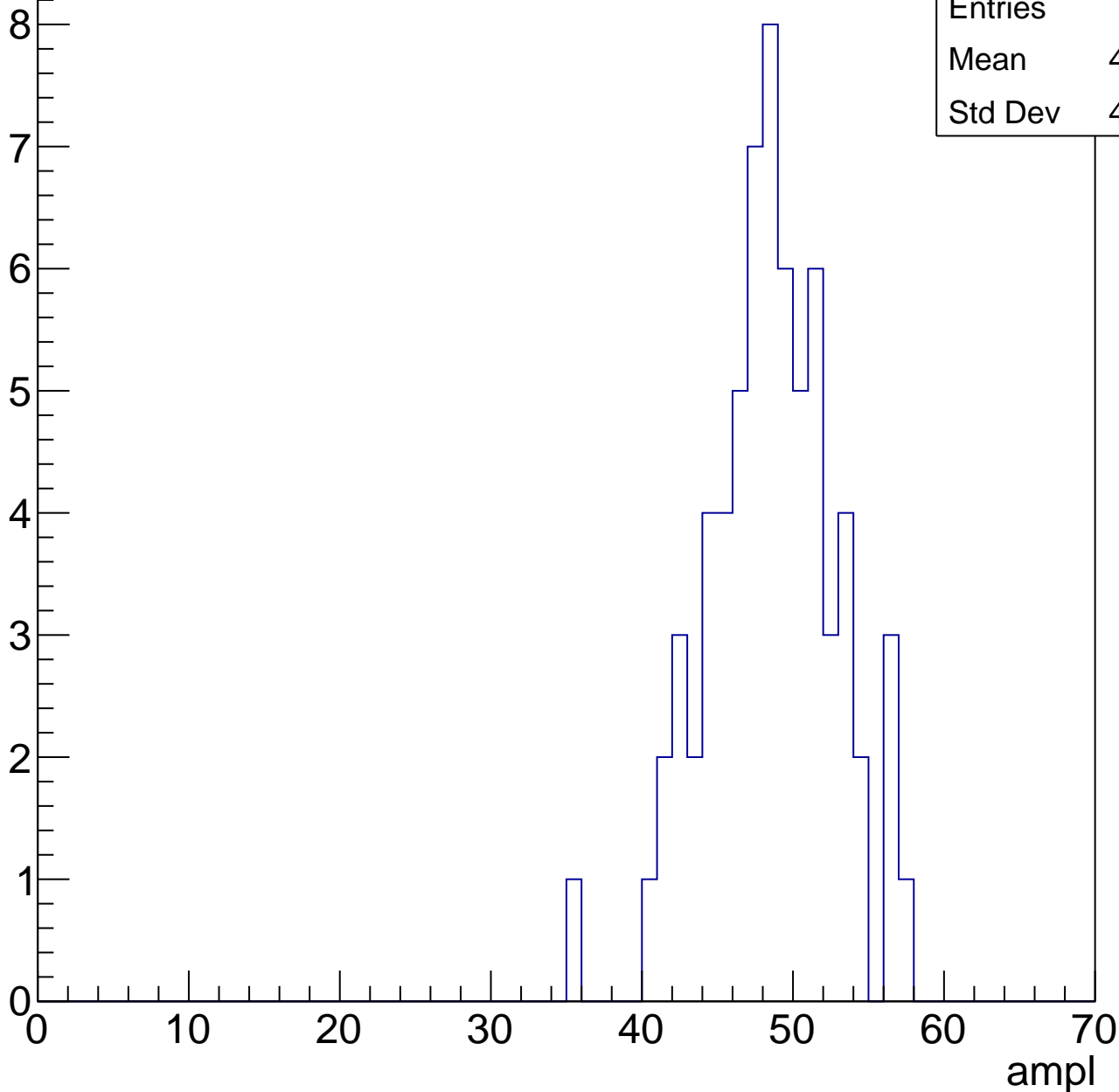


# B1L103S, U2-ch63, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

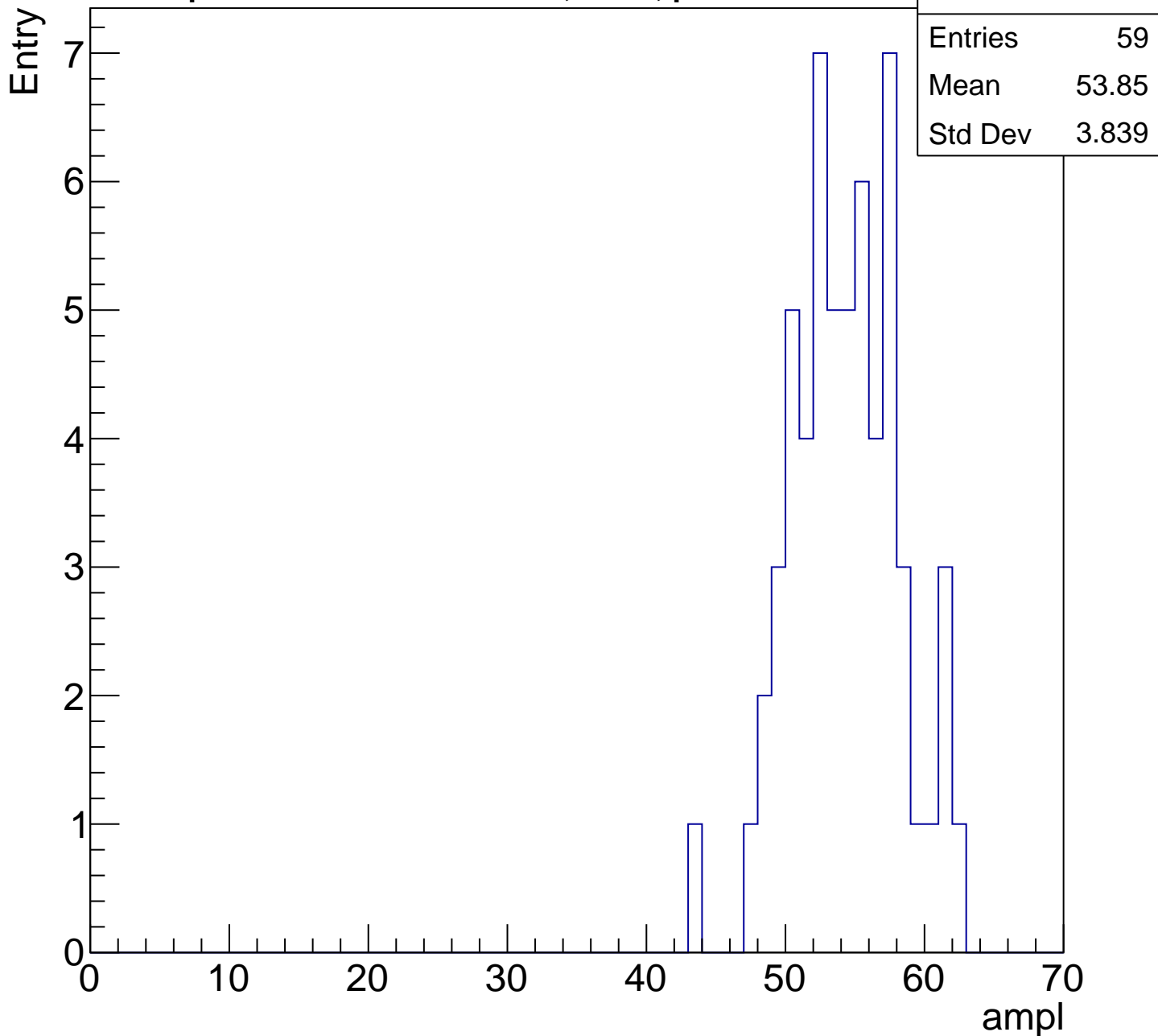
Entry

Entries	67
Mean	48.04
Std Dev	4.212



# B1L103S, U2-ch63, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

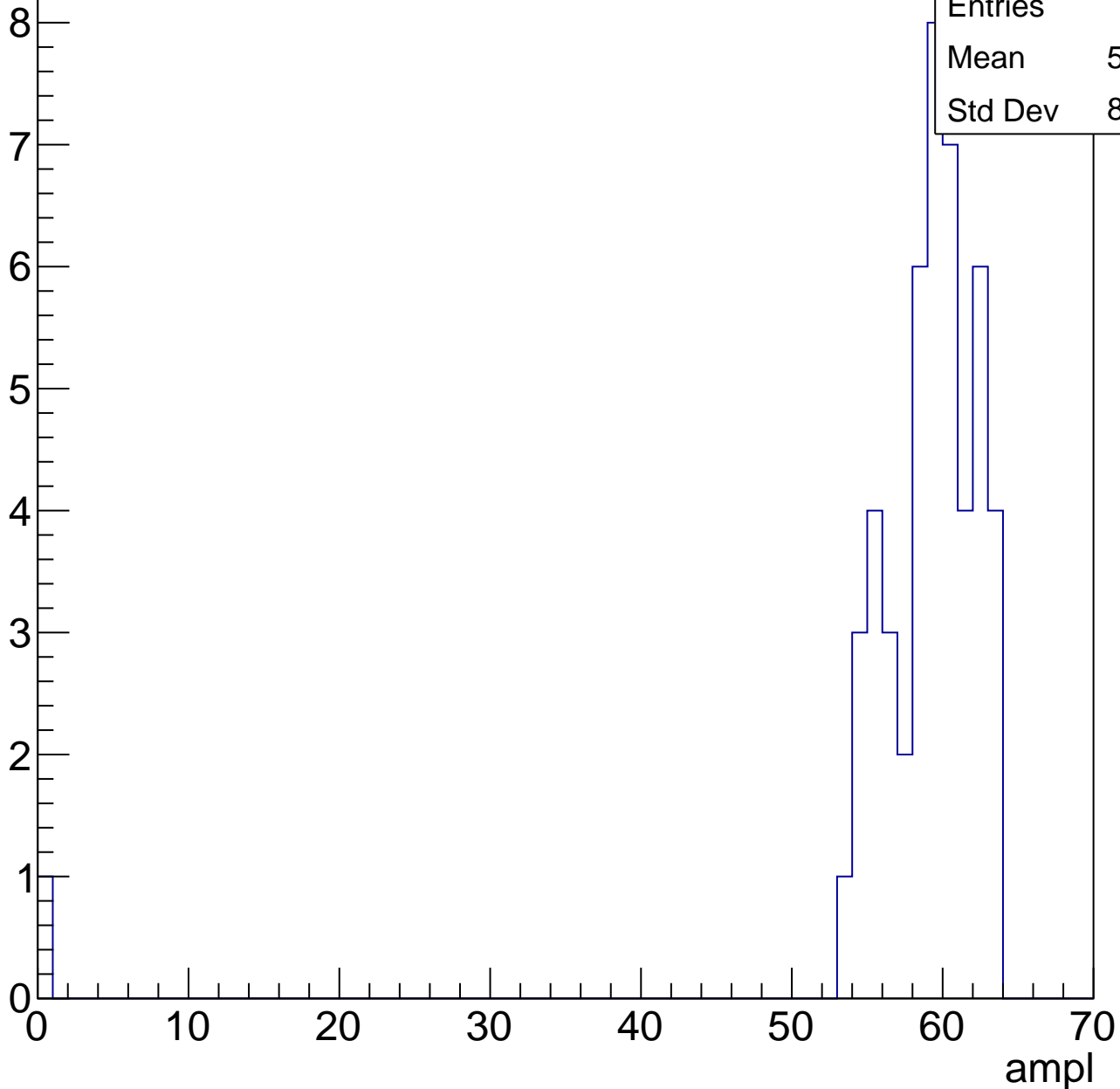


# B1L103S, U2-ch63, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	57.65
Std Dev	8.747

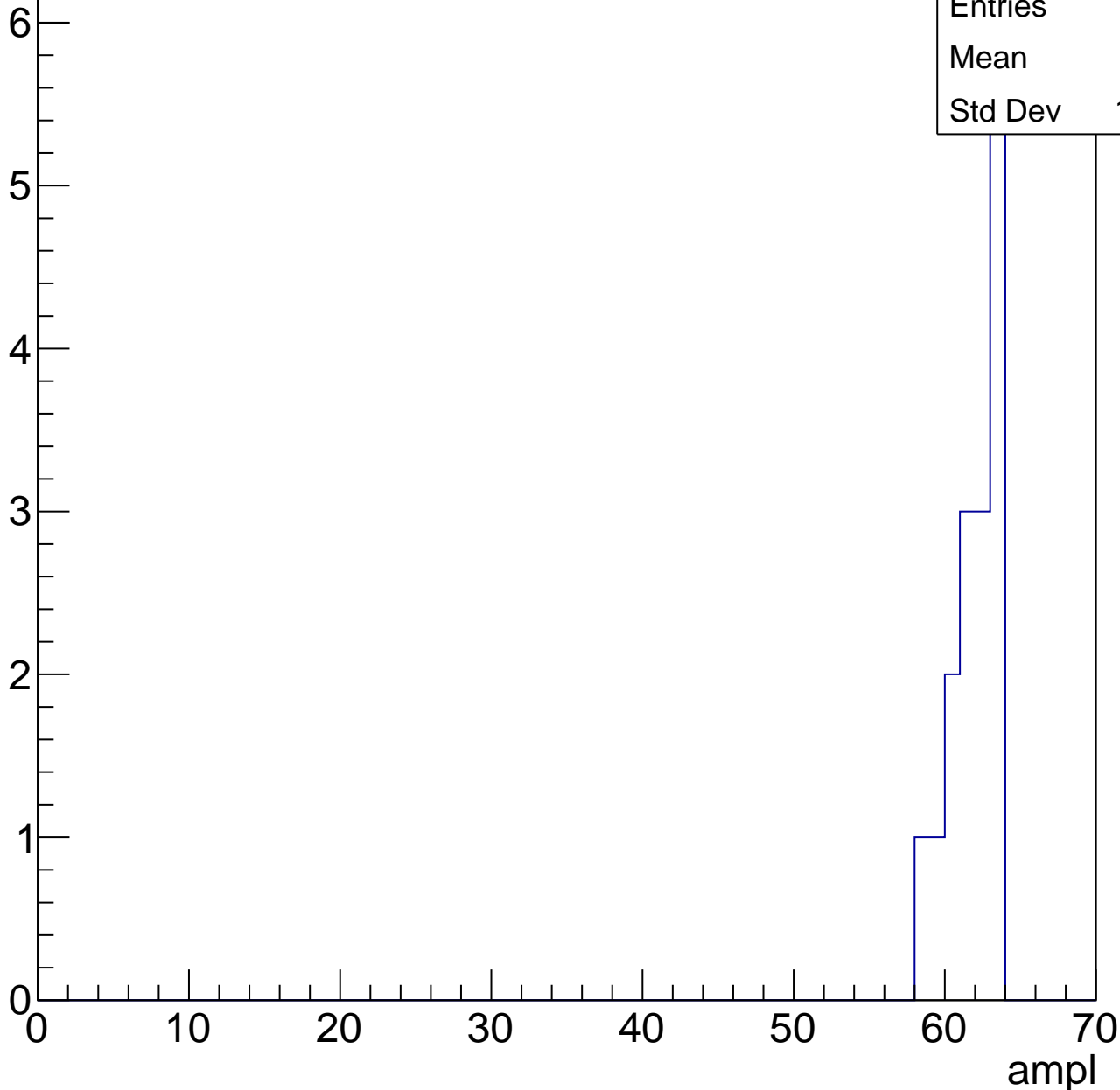


# B1L103S, U2-ch63, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	16
Mean	61.5
Std Dev	1.541





# B1L103S, U2-ch63, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U2-ch64, adc0

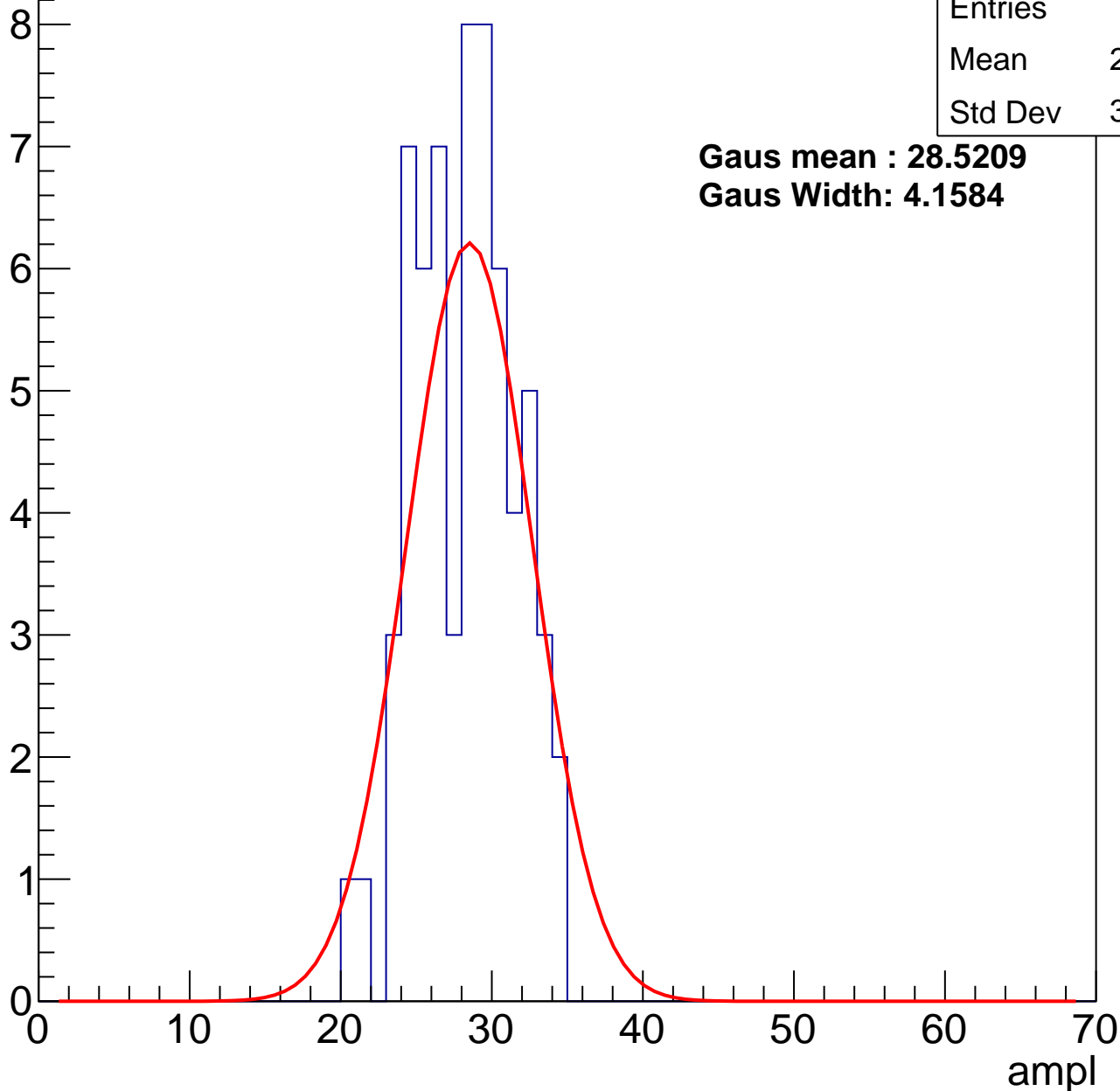
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	27.78
Std Dev	3.252

**Gaus mean : 28.5209**

**Gaus Width: 4.1584**



# B1L103S, U2-ch64, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	71
Mean	34.96
Std Dev	3.546

**Gaus mean : 35.0220**

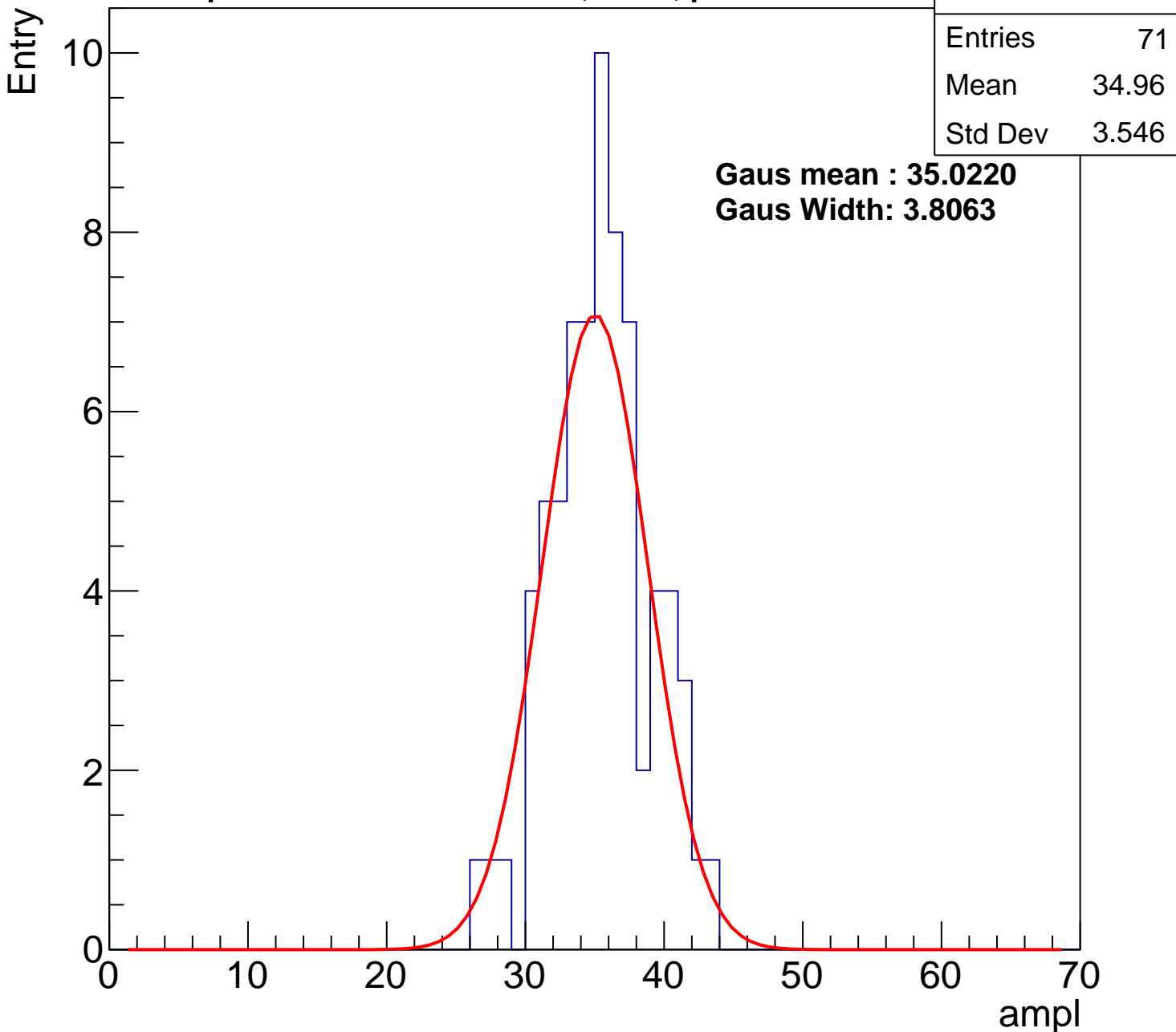
**Gaus Width: 3.8063**

Entry

10  
8  
6  
4  
2  
0

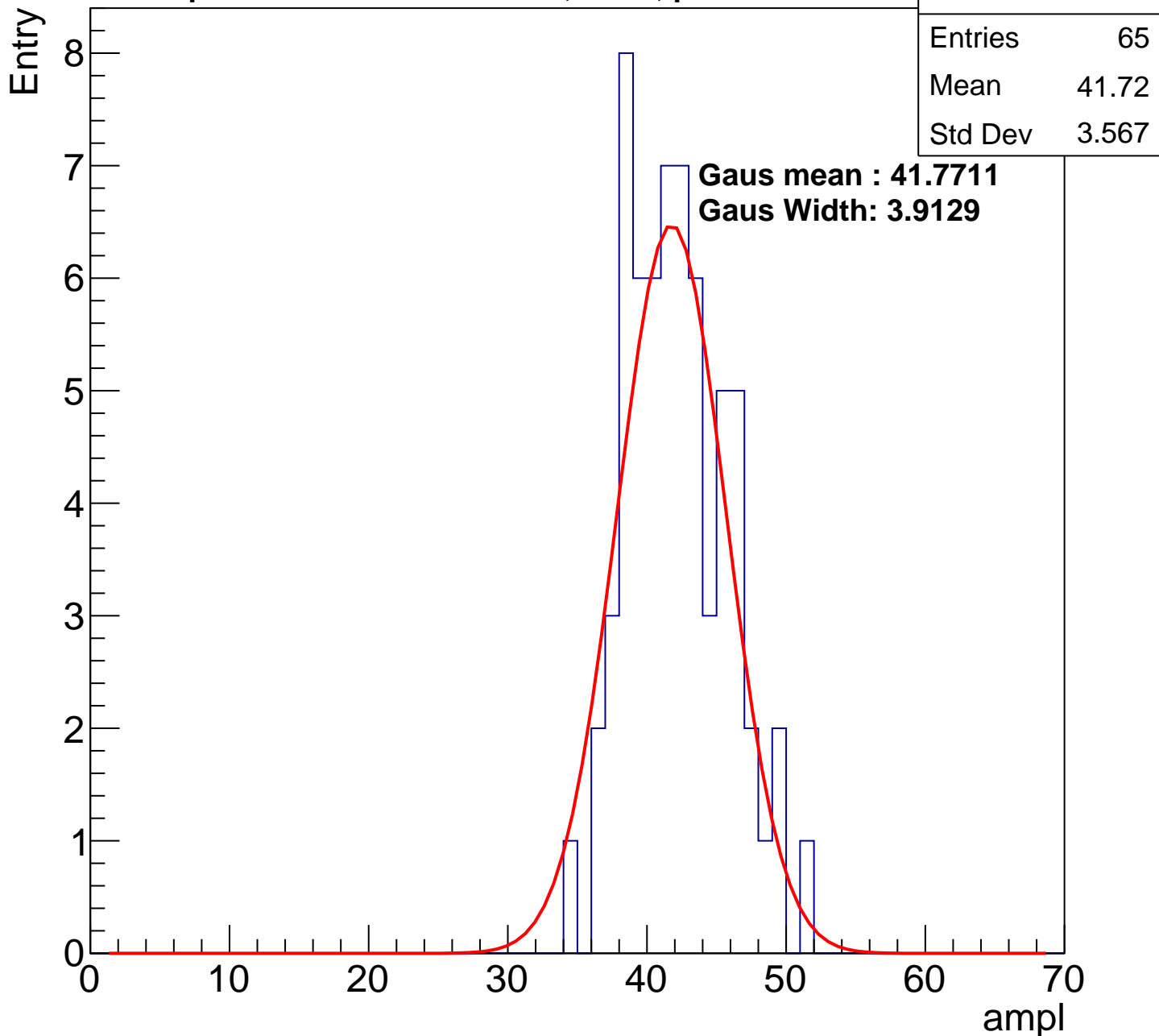
ampl

0 10 20 30 40 50 60 70



# B1L103S, U2-ch64, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

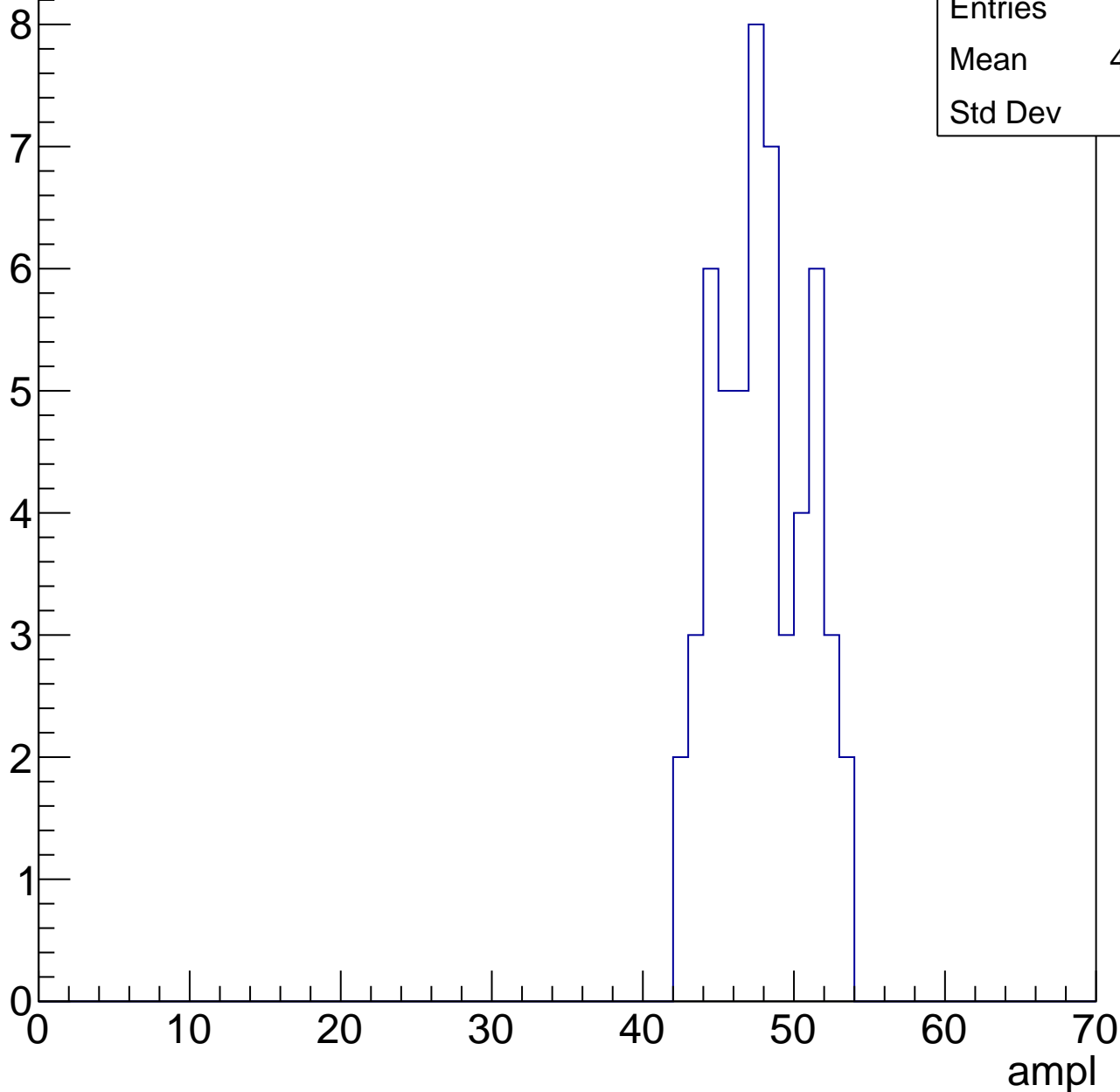


# B1L103S, U2-ch64, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

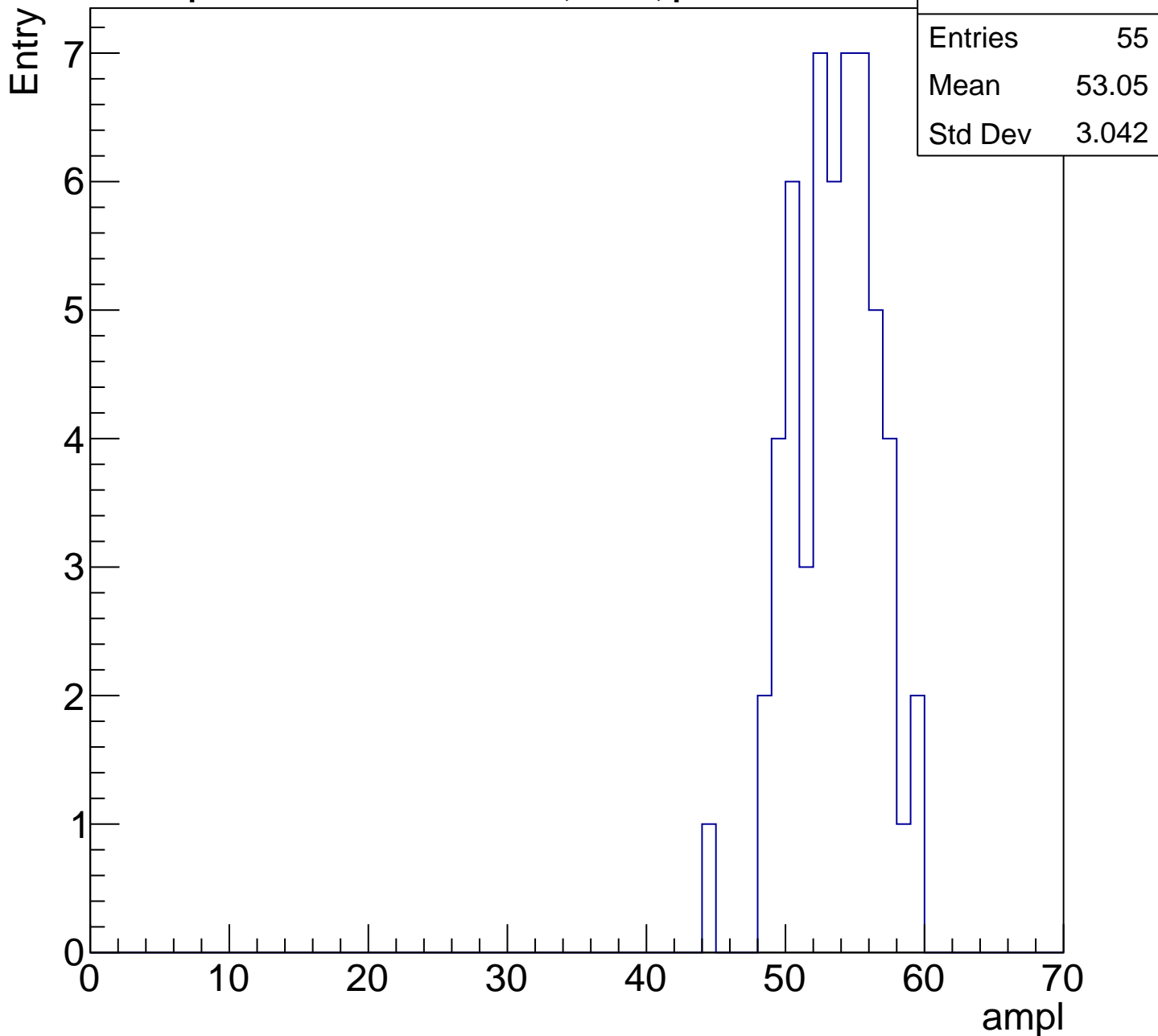
Entry

Entries	54
Mean	47.39
Std Dev	2.94



# B1L103S, U2-ch64, adc4

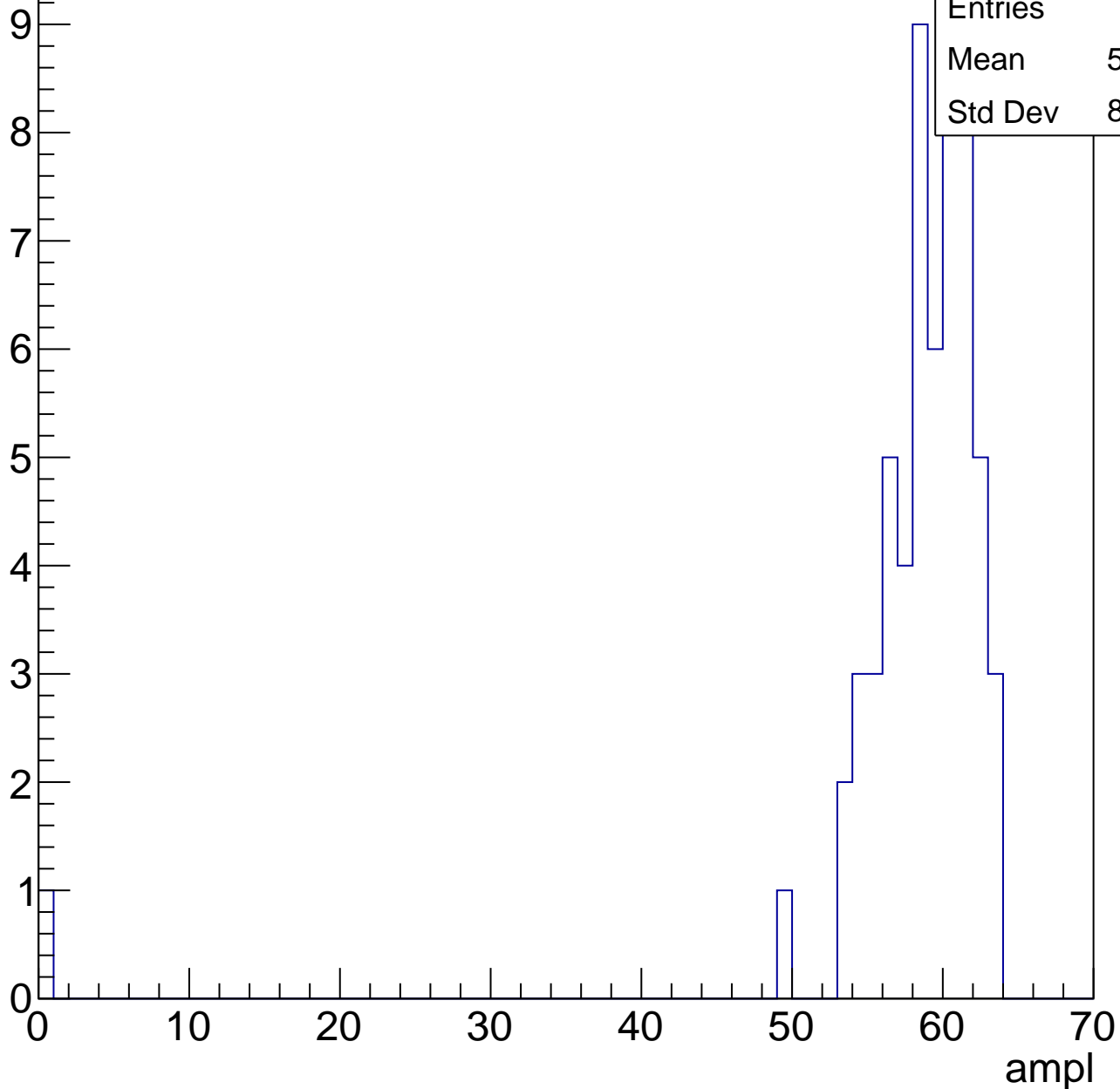
calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U2-ch64, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

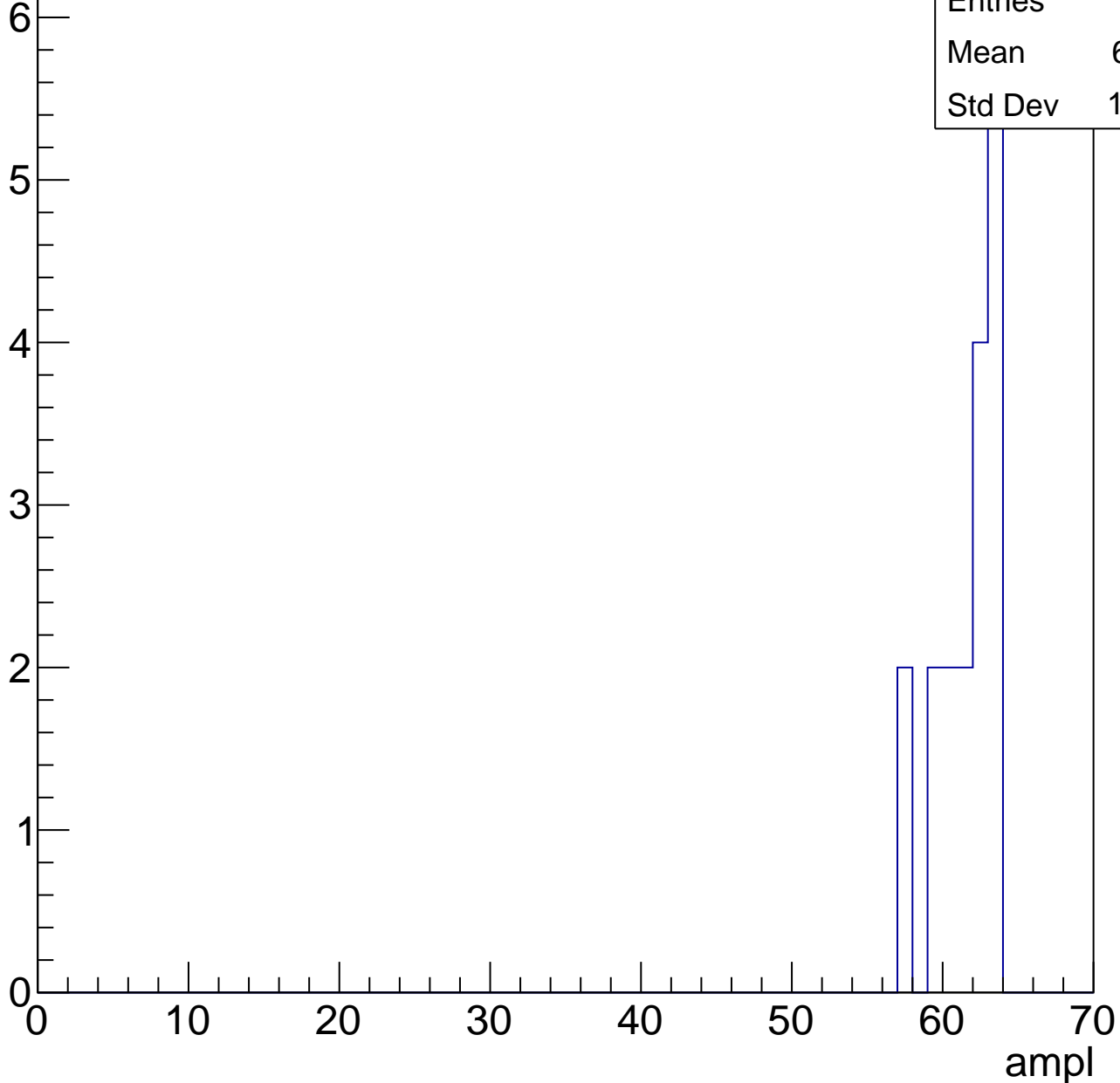


# B1L103S, U2-ch64, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	18
Mean	61.11
Std Dev	1.969





# B1L103S, U2-ch64, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch65, adc0

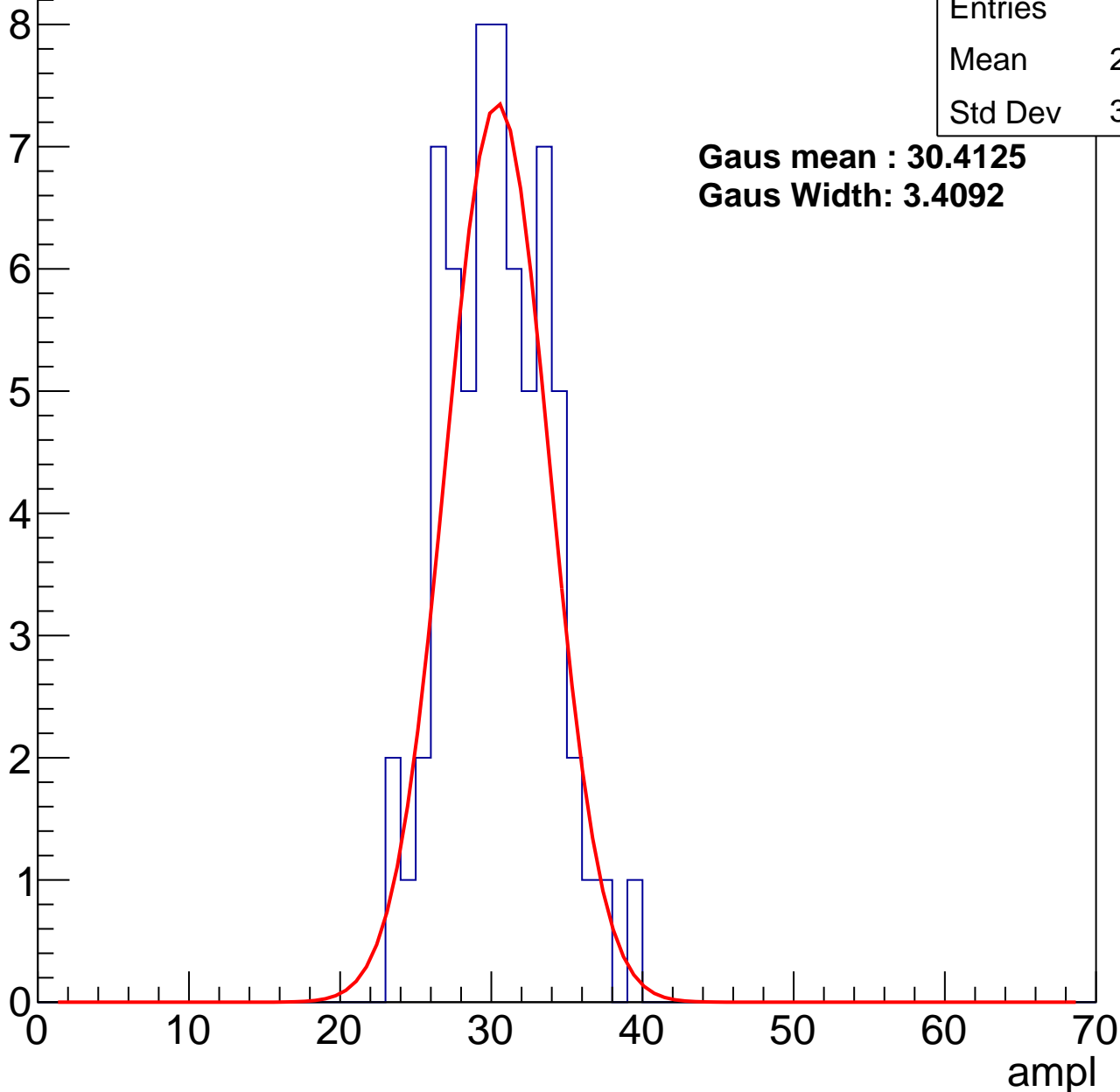
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	29.93
Std Dev	3.374

**Gaus mean : 30.4125**

**Gaus Width: 3.4092**



# B1L103S, U2-ch65, adc1

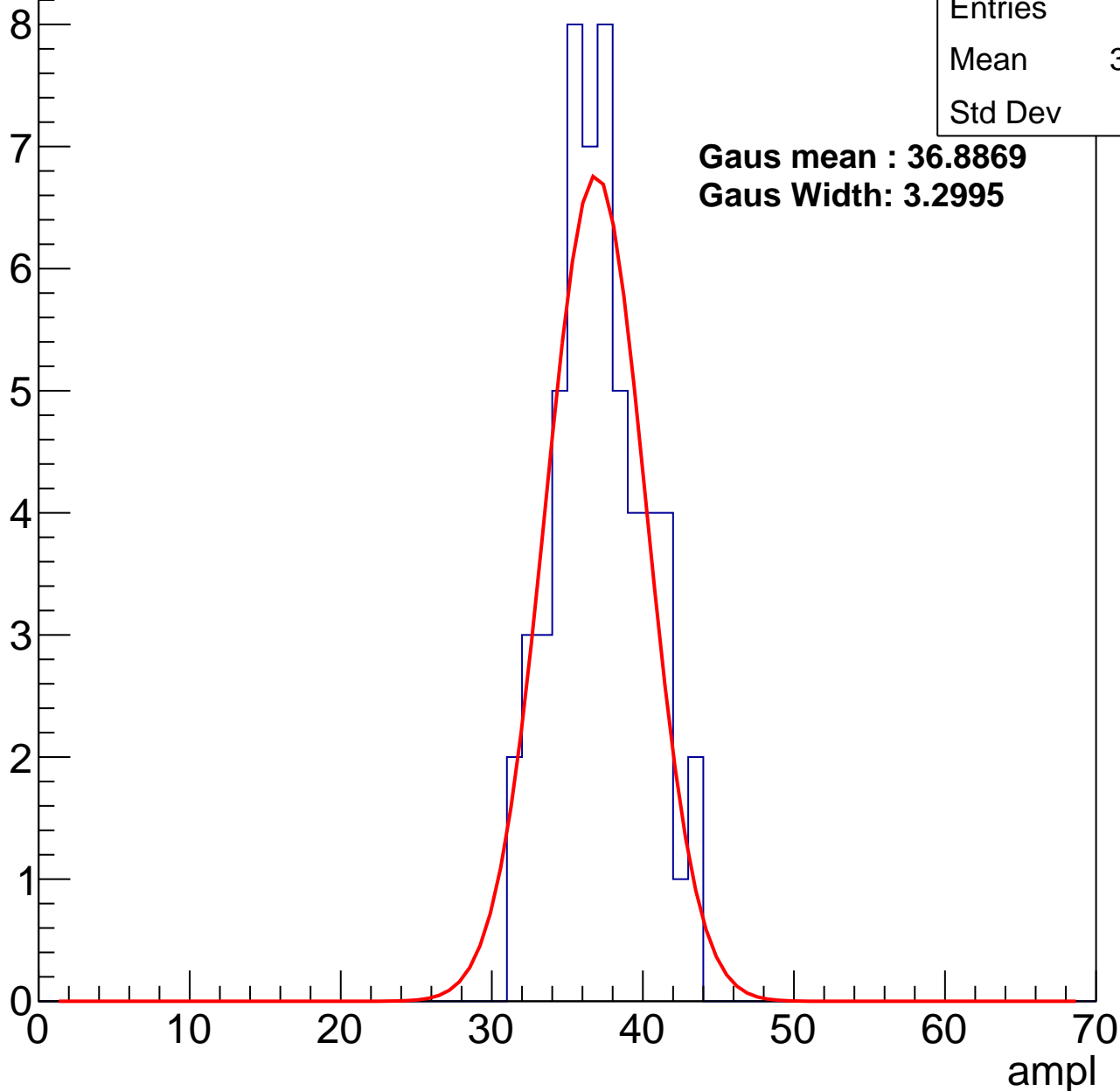
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	36.66
Std Dev	2.96

**Gaus mean : 36.8869**

**Gaus Width: 3.2995**



# B1L103S, U2-ch65, adc2

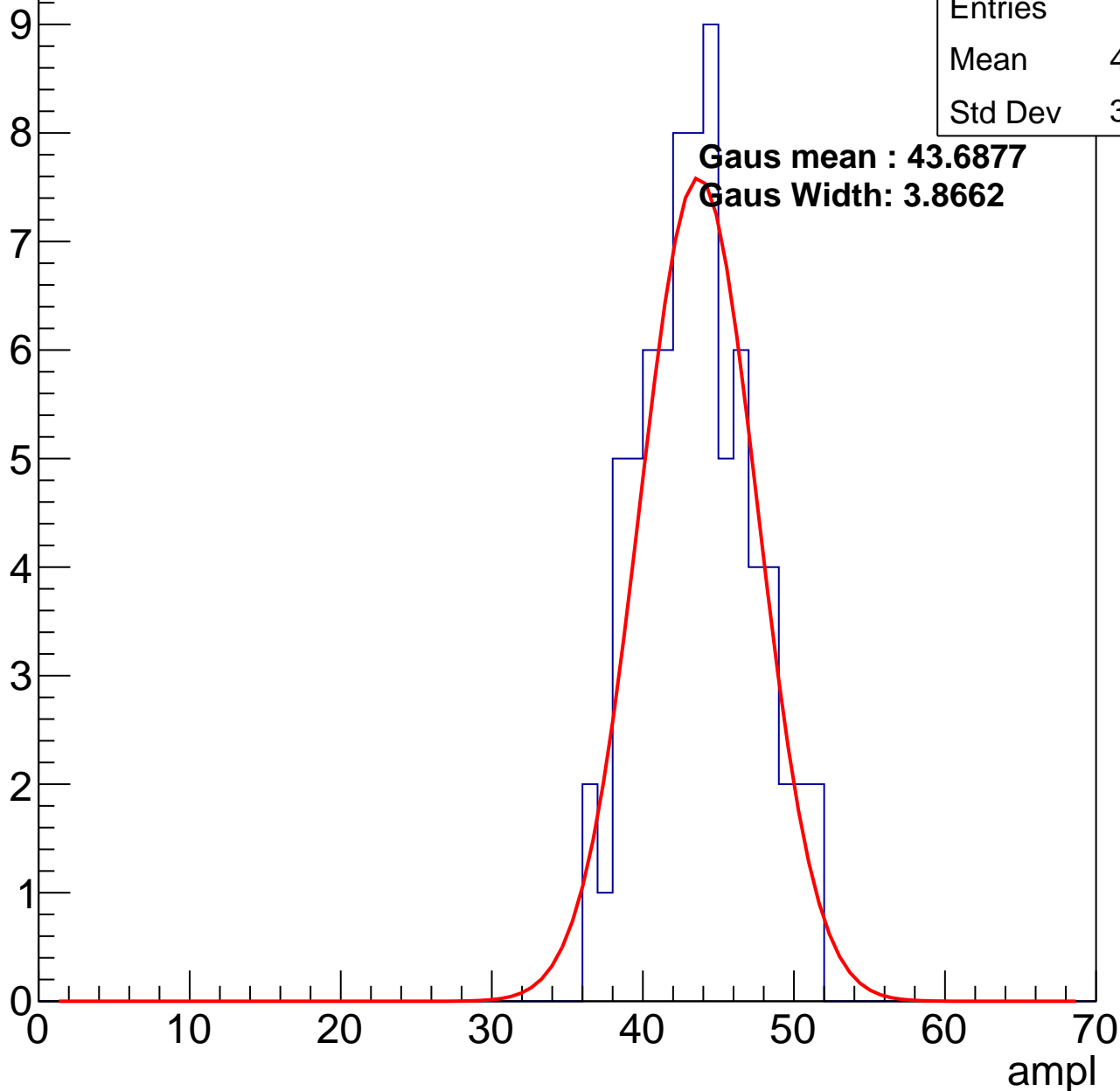
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	43.16
Std Dev	3.593

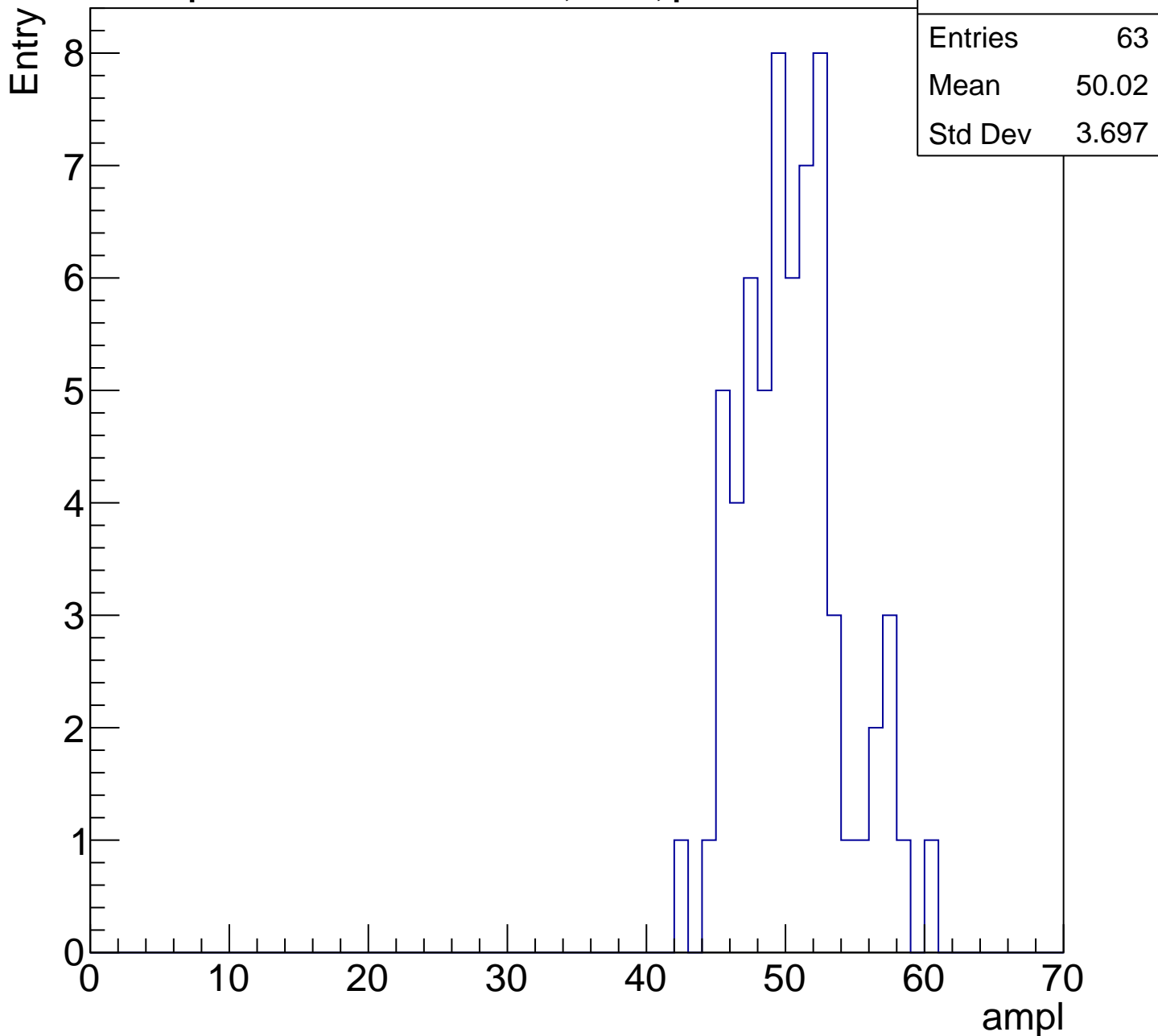
**Gaus mean : 43.6877**

**Gaus Width: 3.8662**



# B1L103S, U2-ch65, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

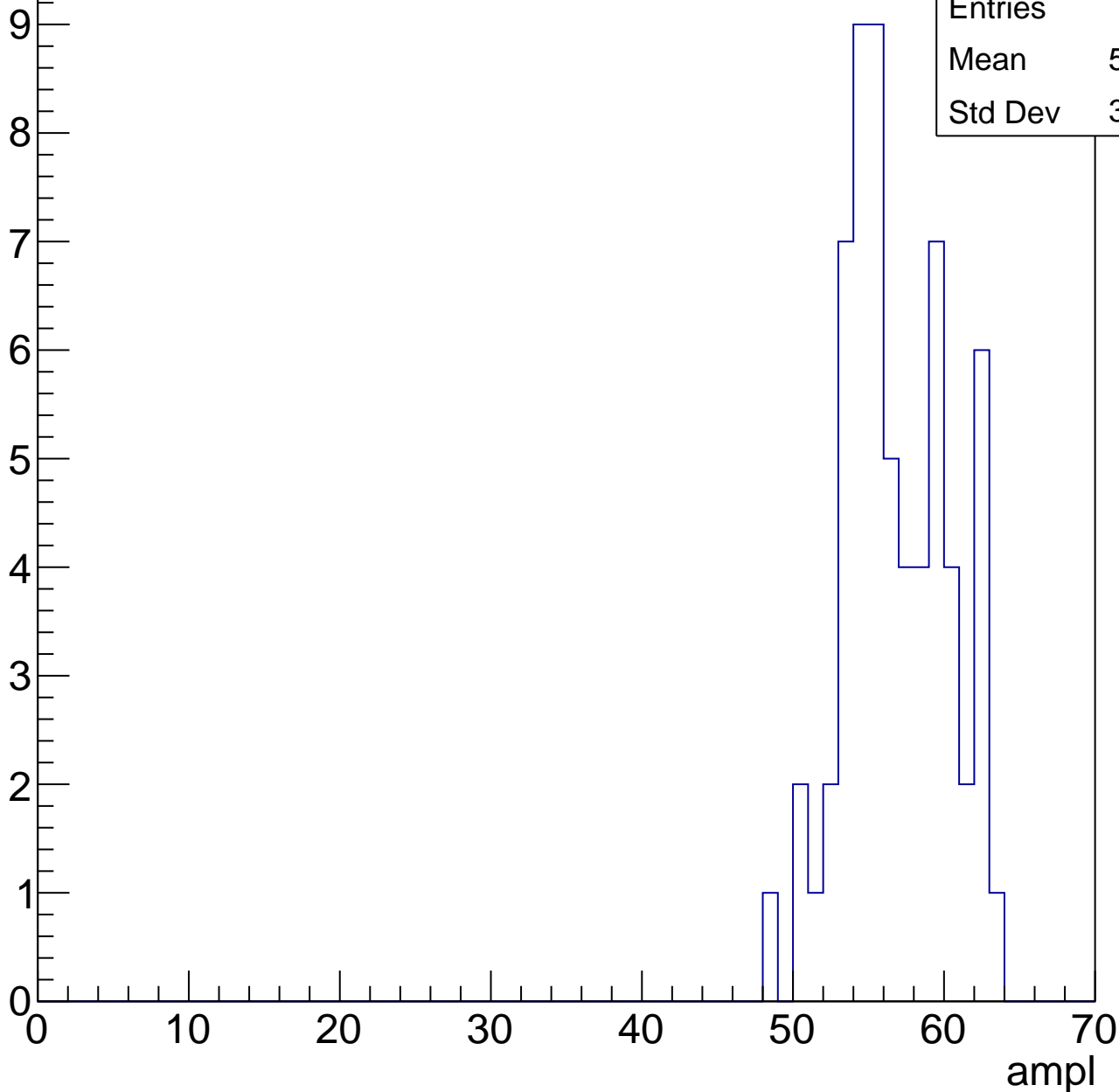


# B1L103S, U2-ch65, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	56.33
Std Dev	3.437

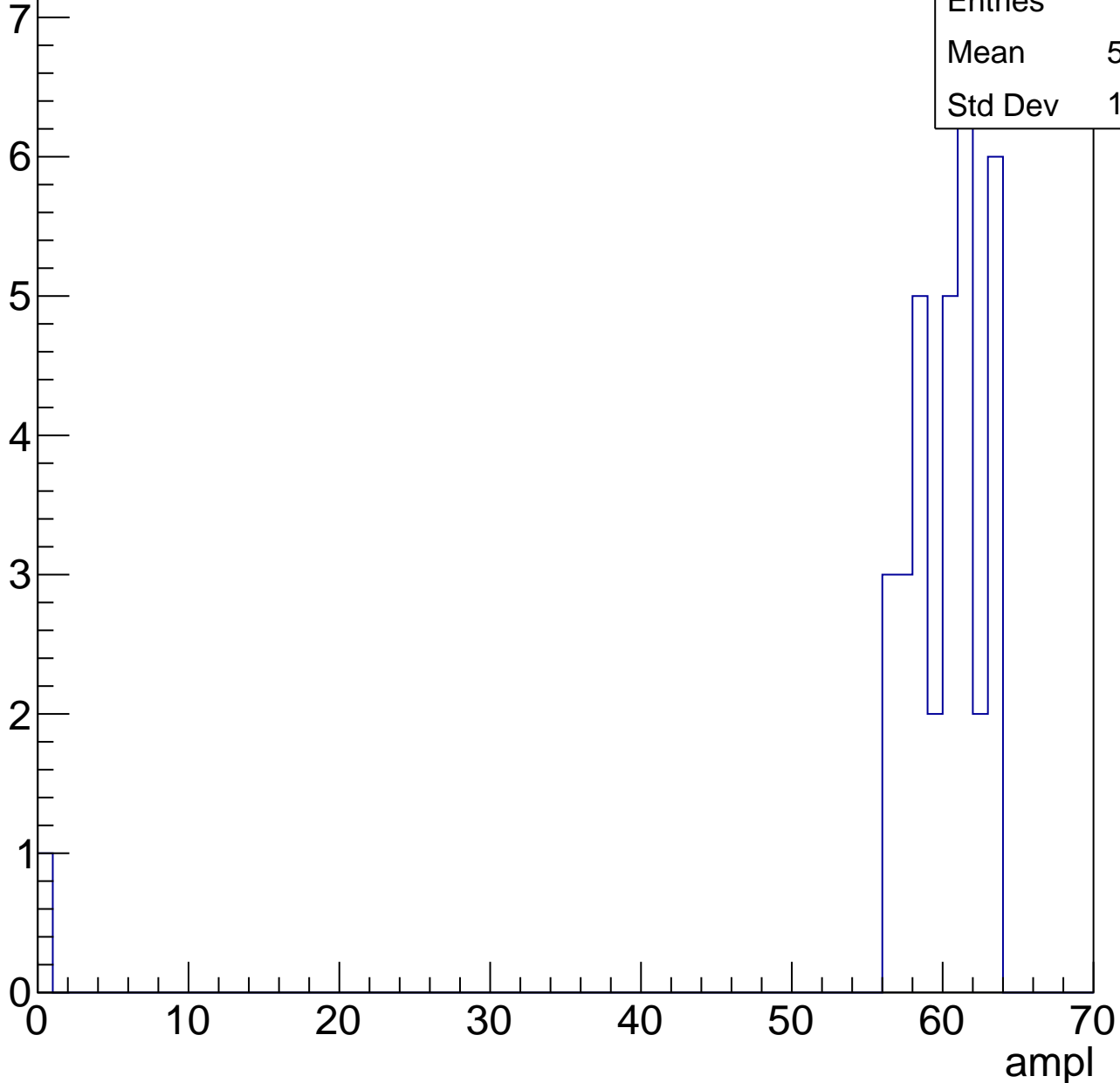


# B1L103S, U2-ch65, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

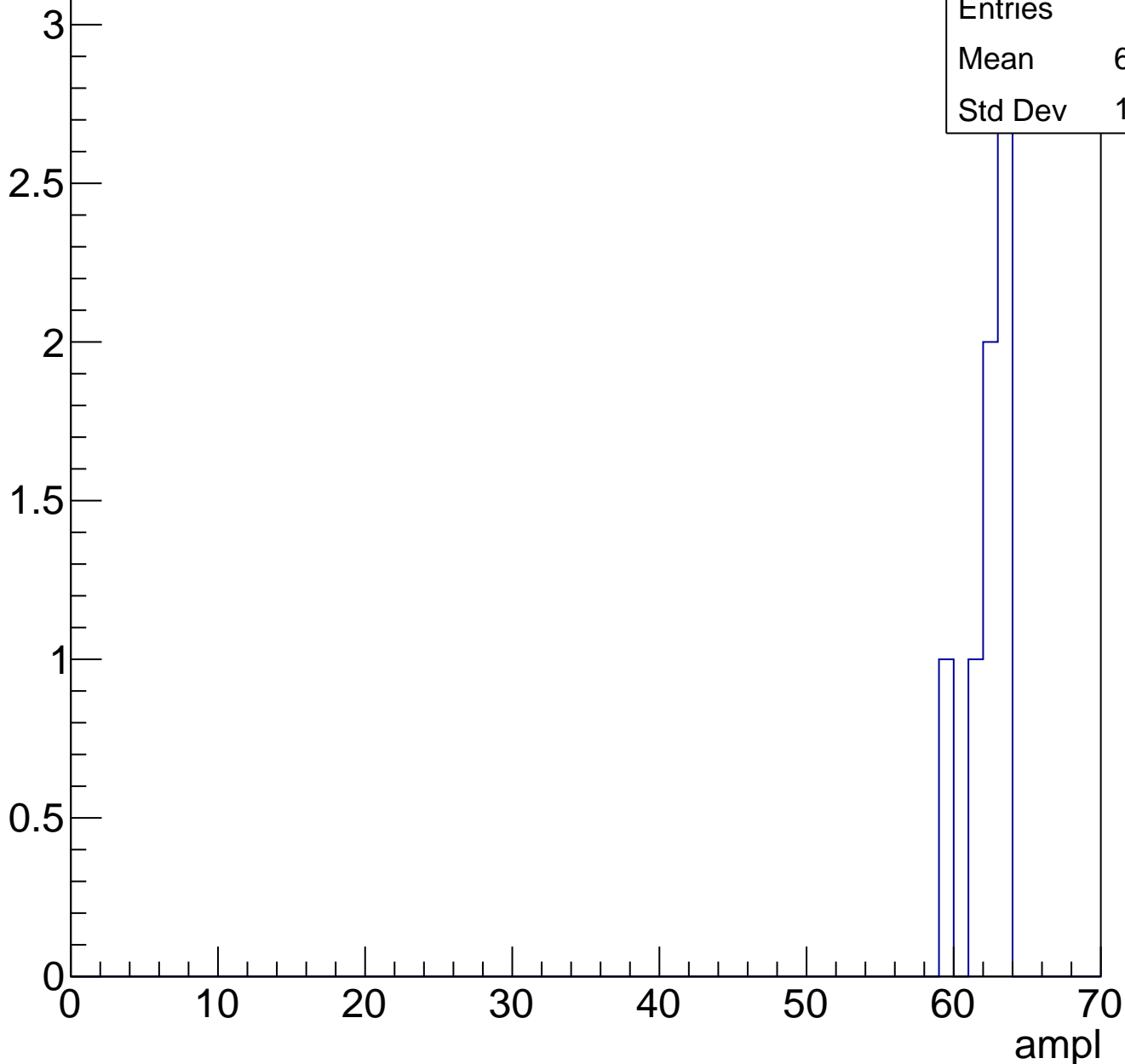
Entries	34
Mean	58.12
Std Dev	10.35



# B1L103S, U2-ch65, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

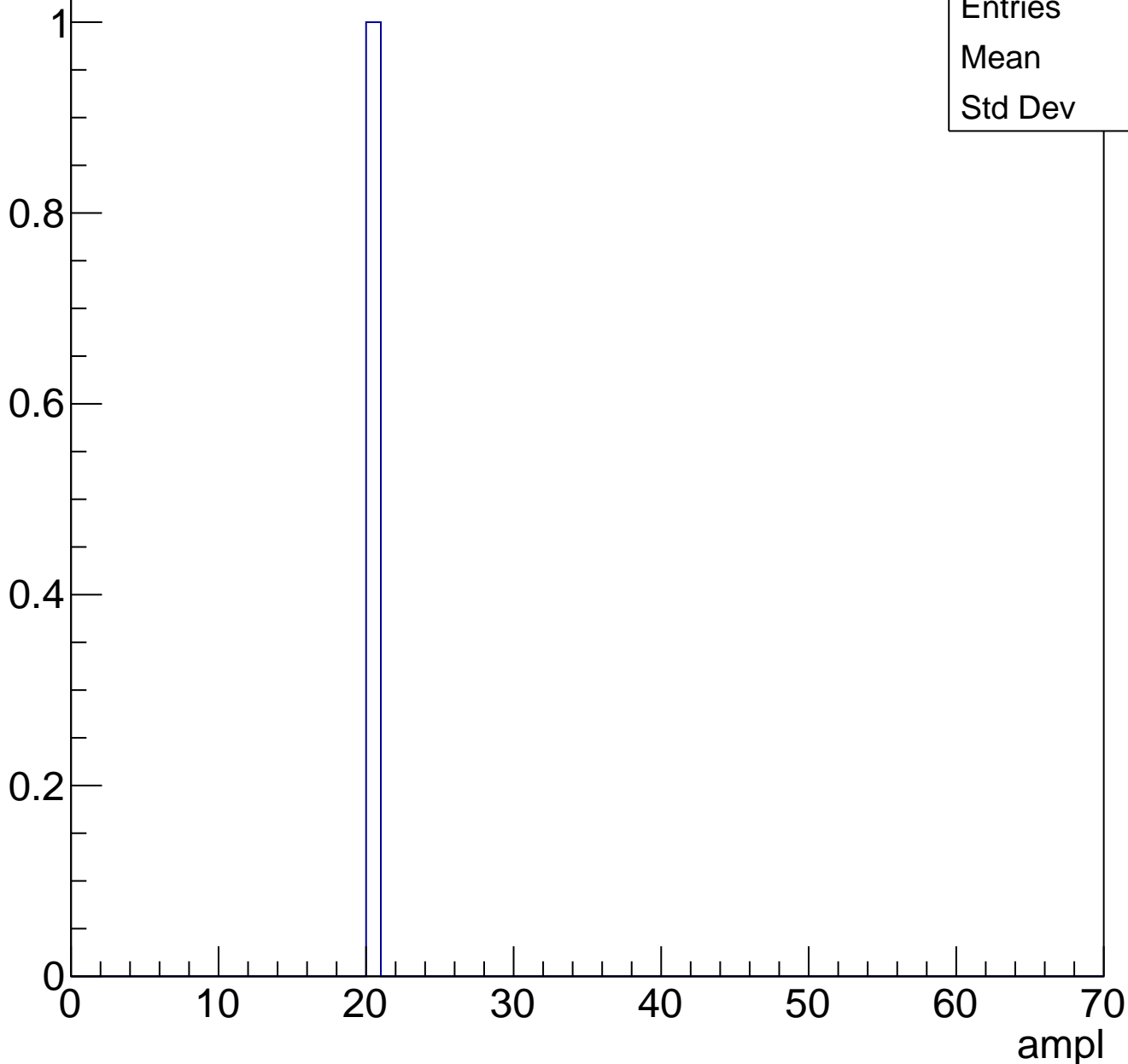




# B1L103S, U2-ch65, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	20
Std Dev	0

# B1L103S, U2-ch66, adc0

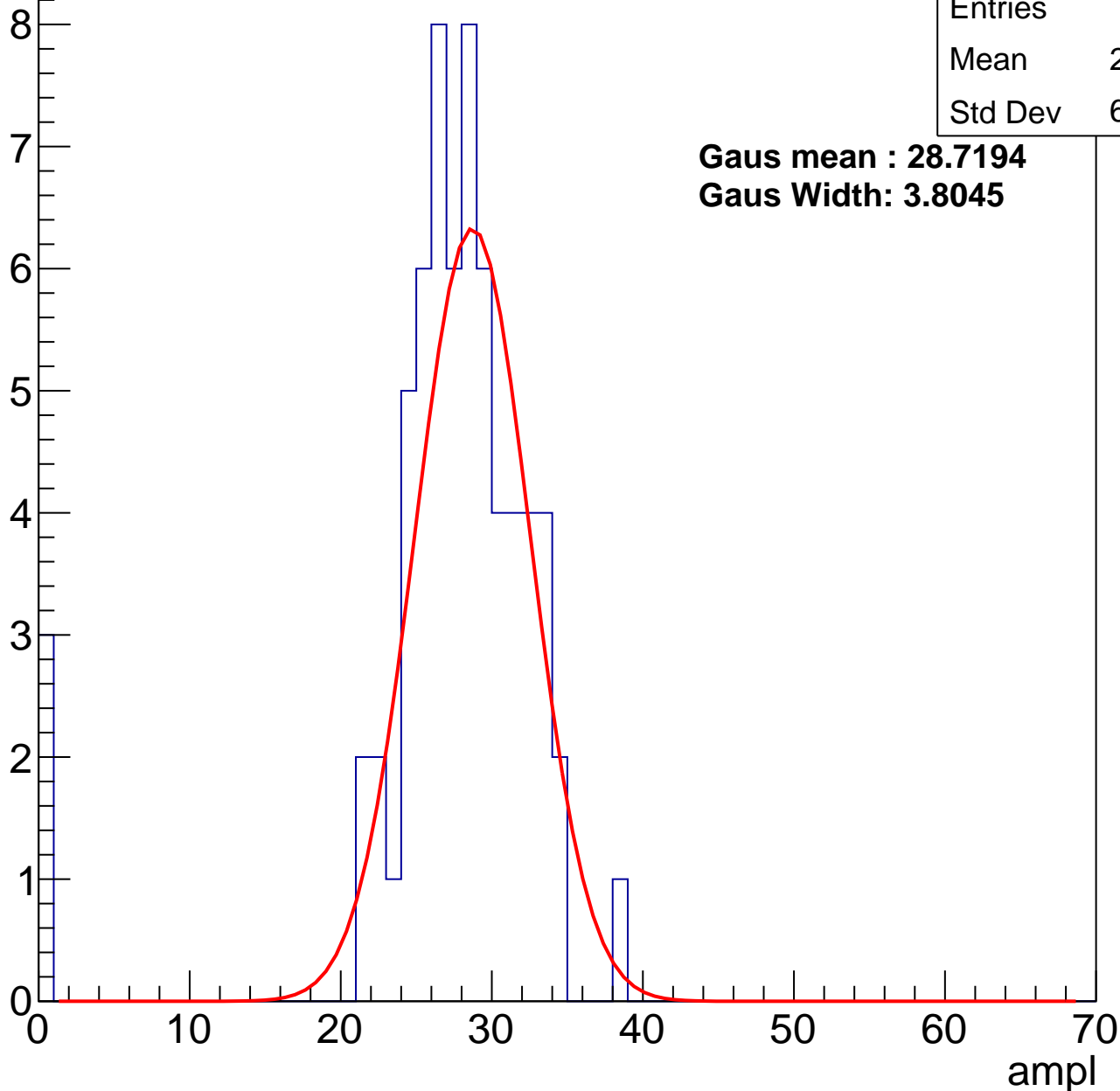
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	26.62
Std Dev	6.728

**Gaus mean : 28.7194**

**Gaus Width: 3.8045**



# B1L103S, U2-ch66, adc1

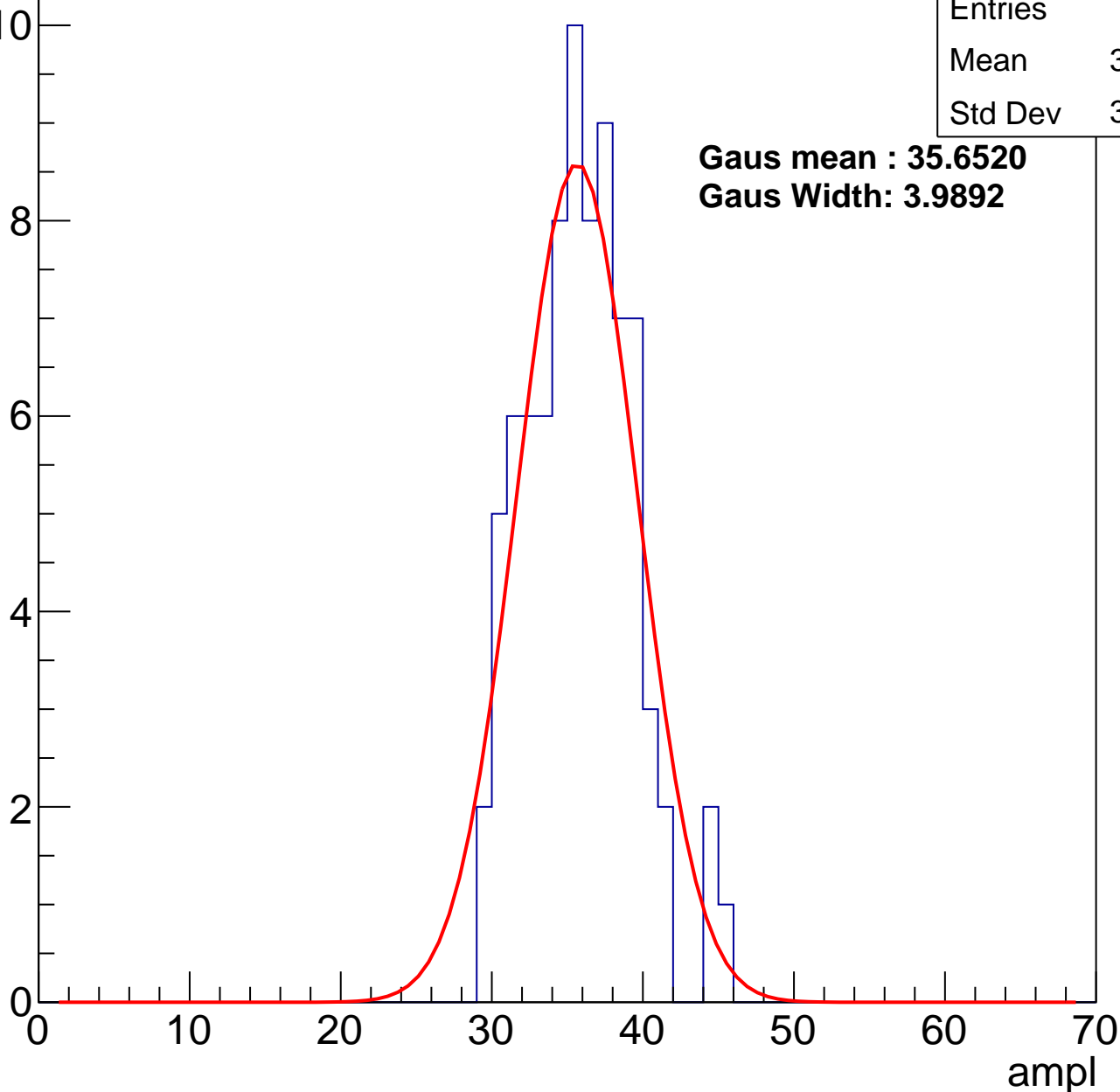
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	82
Mean	35.38
Std Dev	3.484

**Gaus mean : 35.6520**

**Gaus Width: 3.9892**



# B1L103S, U2-ch66, adc2

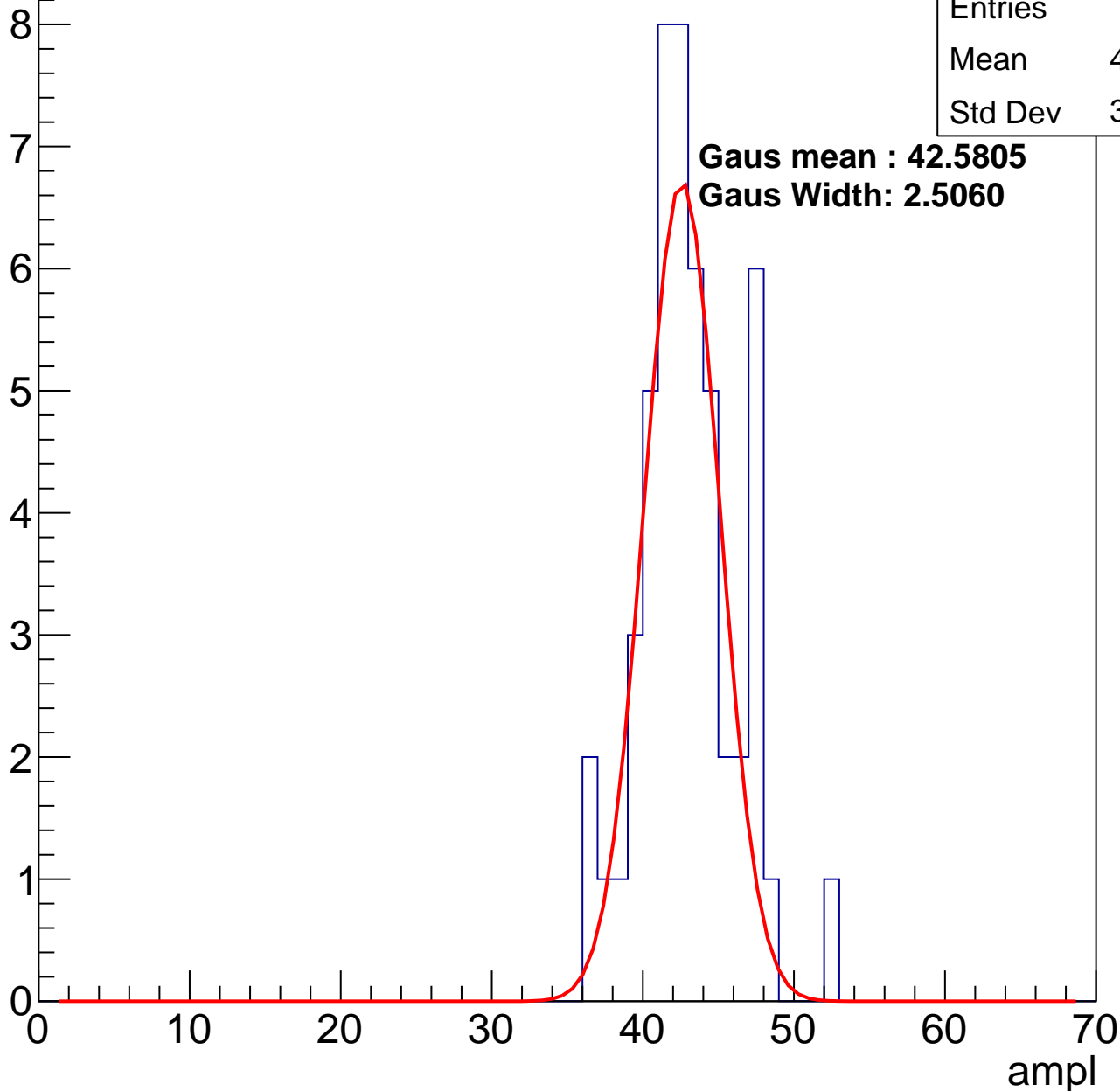
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	42.55
Std Dev	3.177

**Gaus mean : 42.5805**

**Gaus Width: 2.5060**

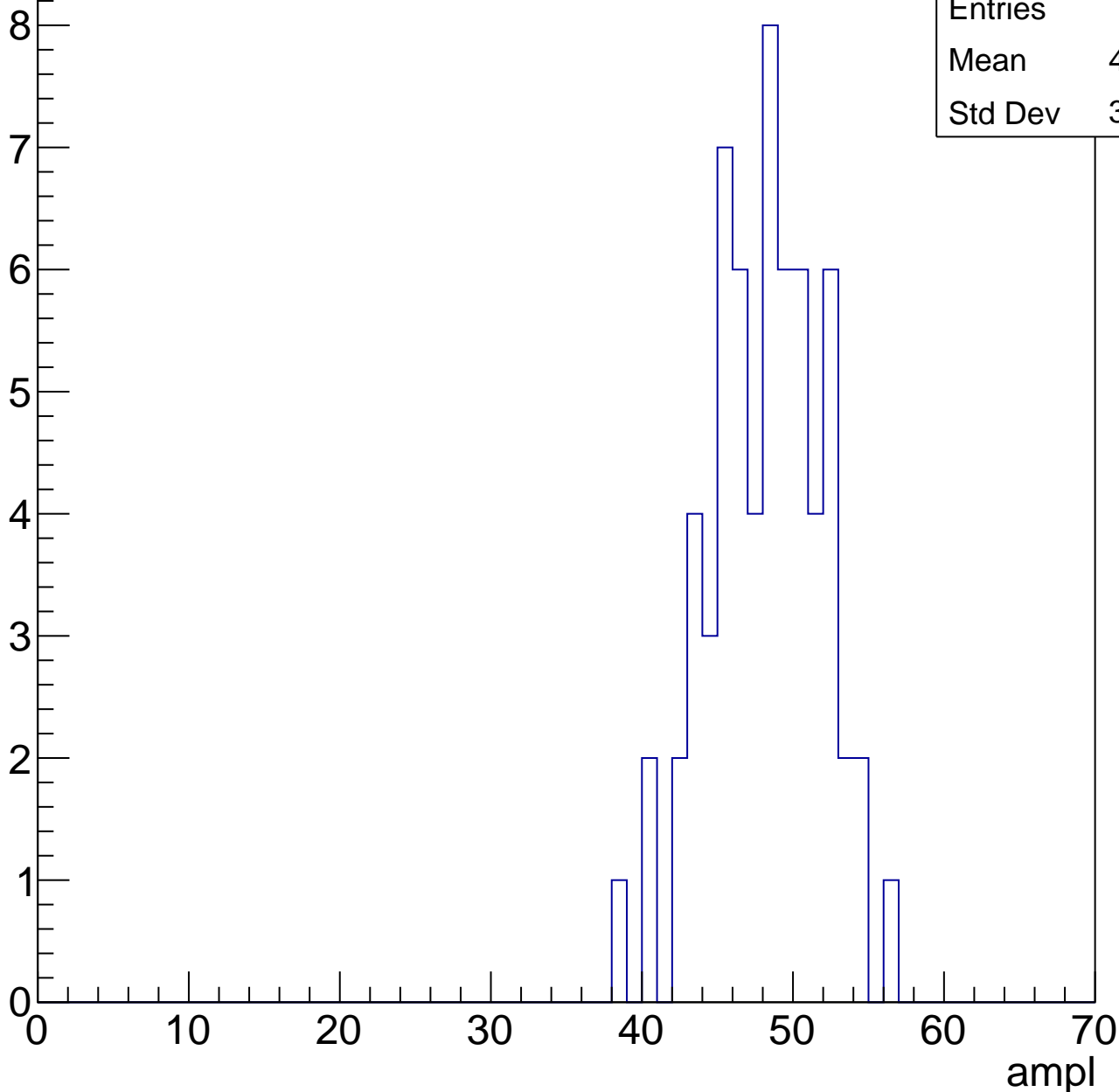


# B1L103S, U2-ch66, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	47.64
Std Dev	3.705

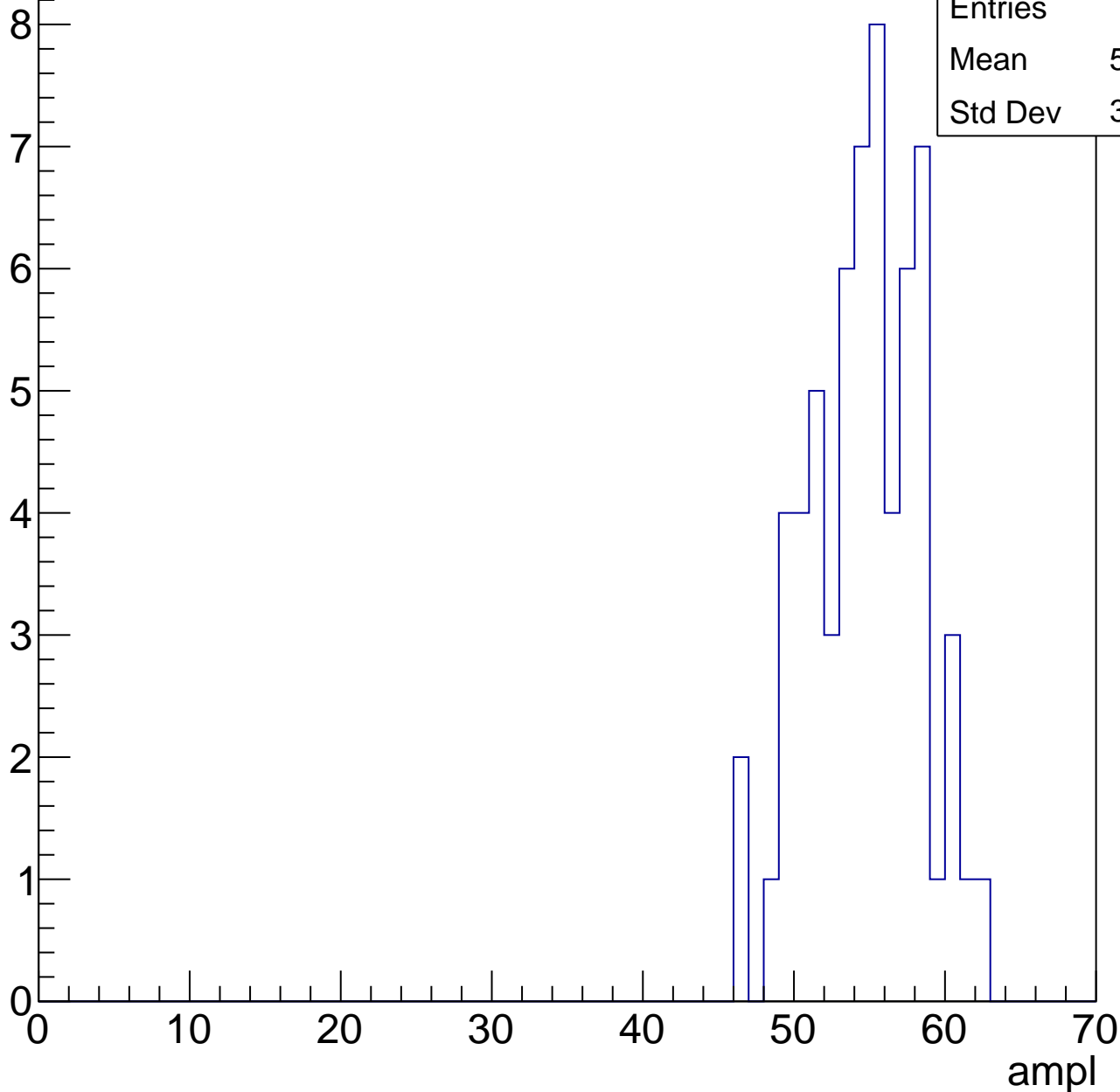


# B1L103S, U2-ch66, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

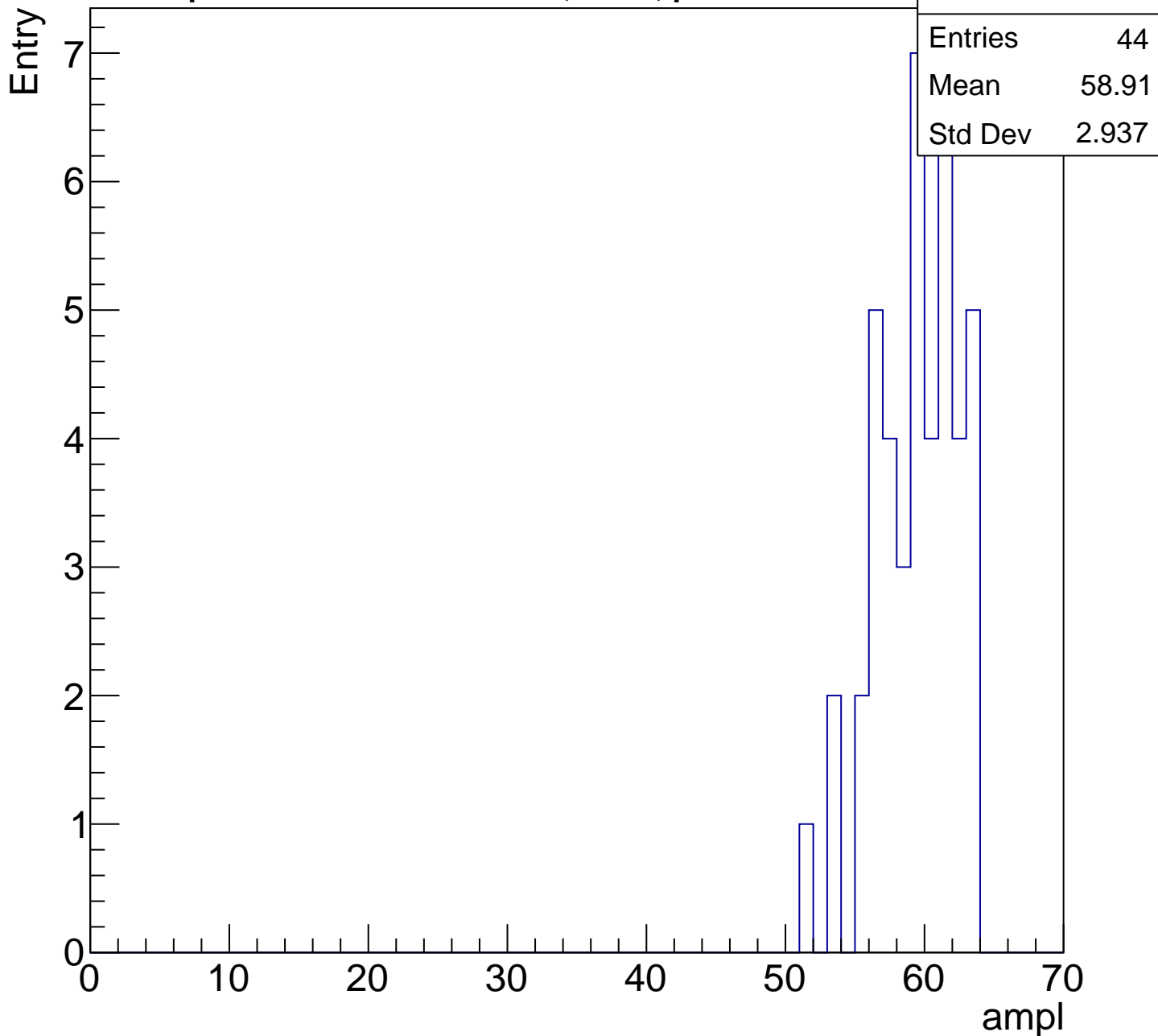
Entry

Entries	63
Mean	54.24
Std Dev	3.615



# B1L103S, U2-ch66, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

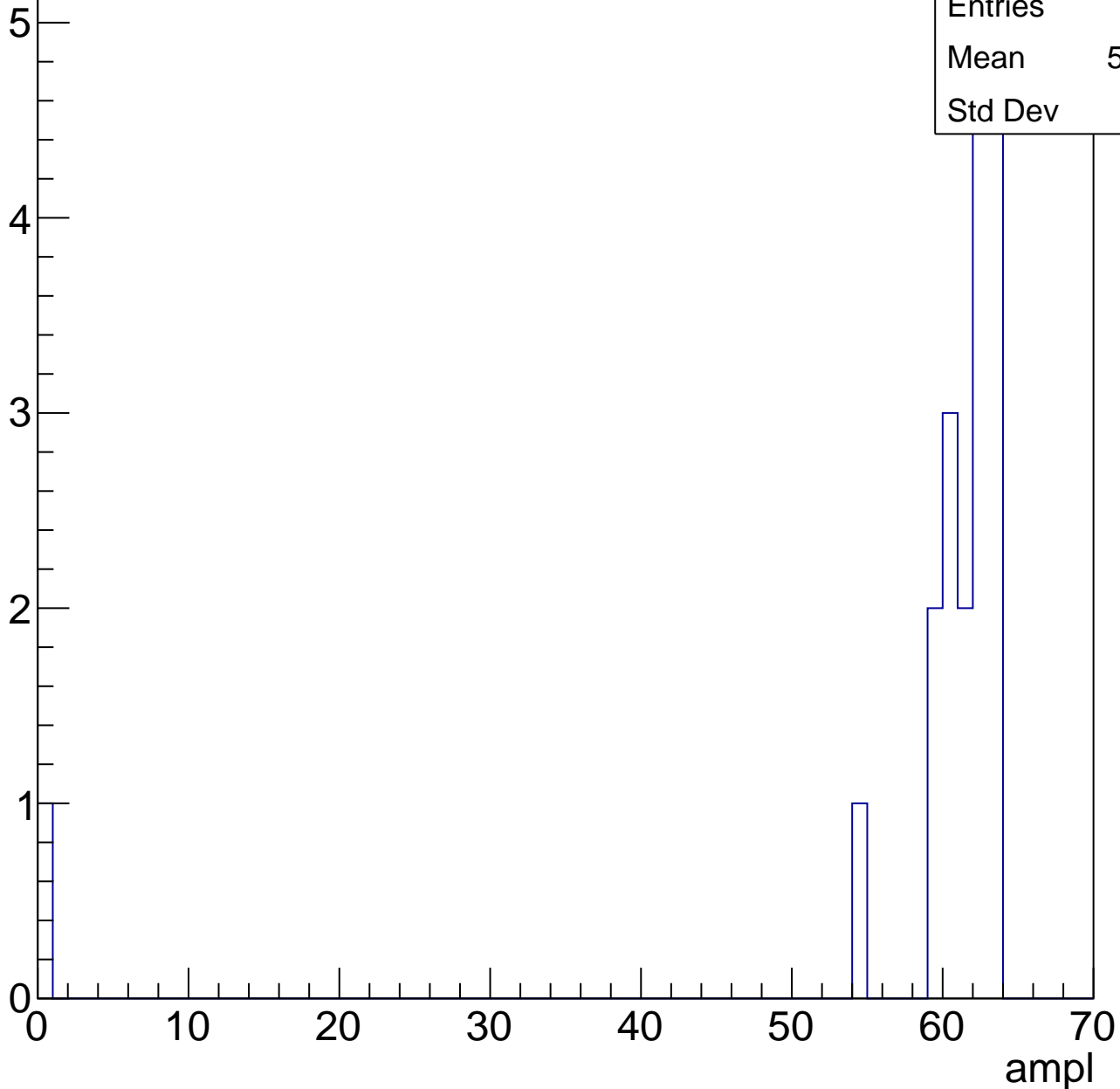


# B1L103S, U2-ch66, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	19
Mean	57.84
Std Dev	13.8





# B1L103S, U2-ch66, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U2-ch67, adc0

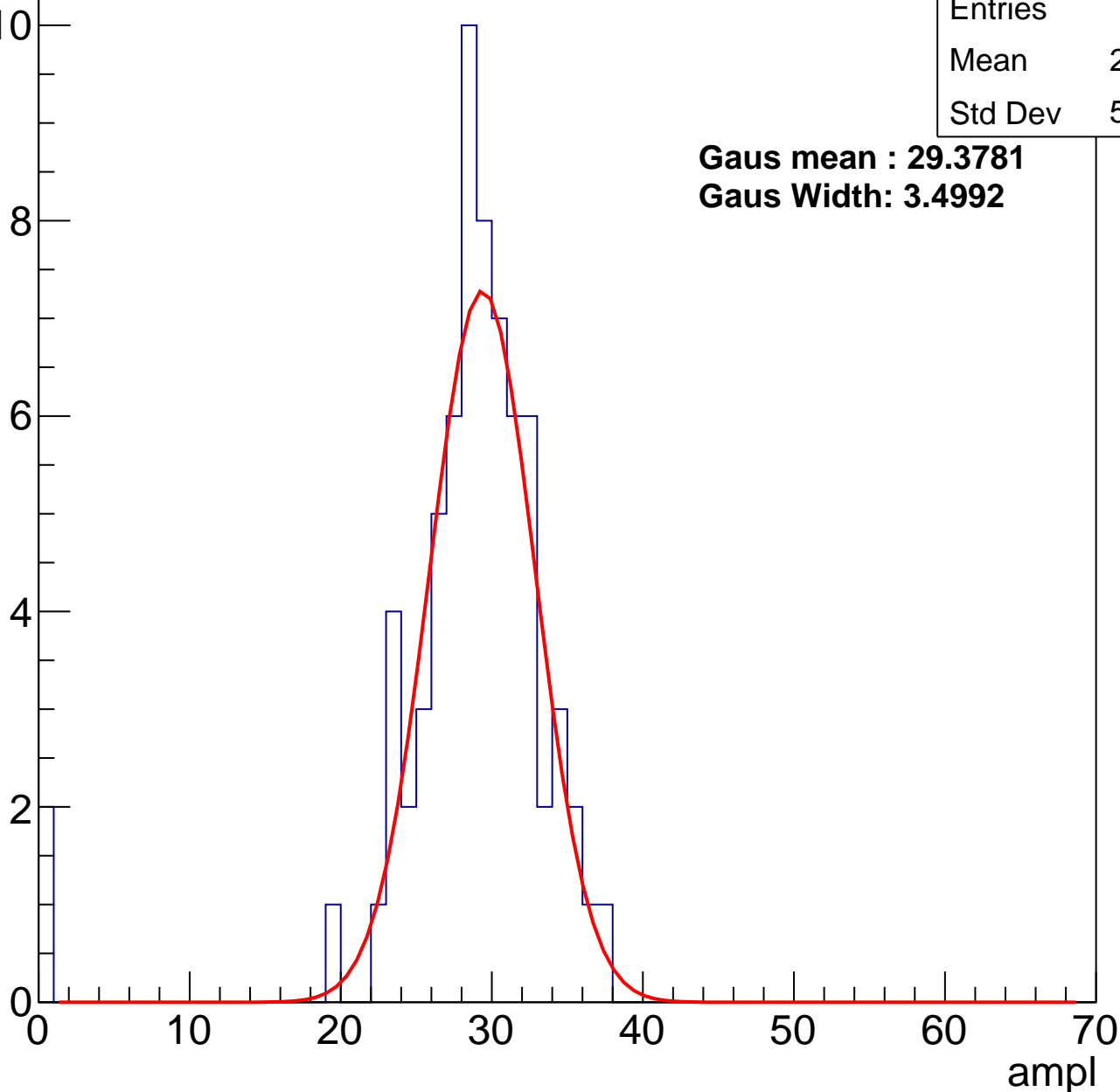
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	27.99
Std Dev	5.925

**Gaus mean : 29.3781**

**Gaus Width: 3.4992**



# B1L103S, U2-ch67, adc1

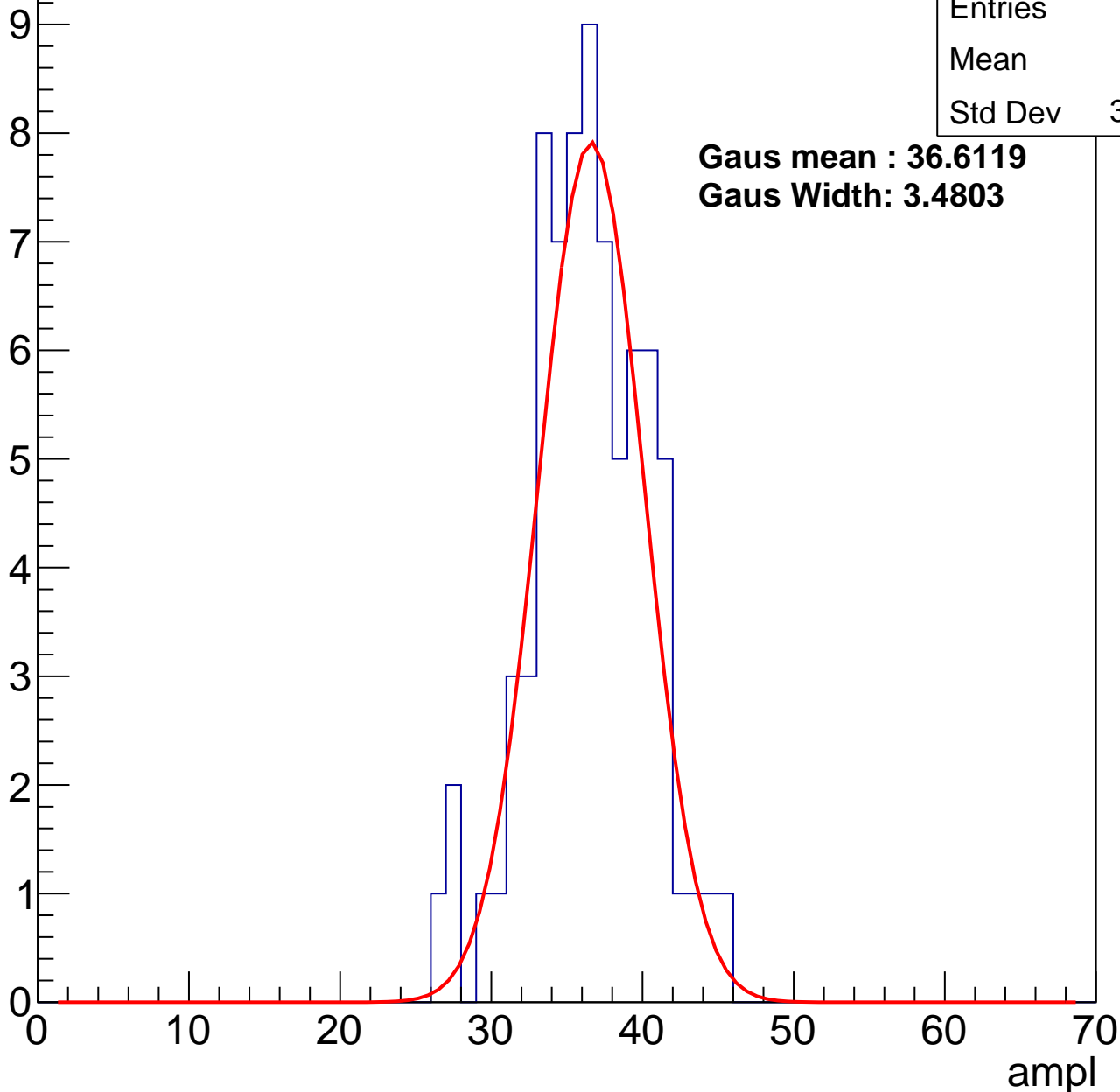
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	36
Std Dev	3.822

**Gaus mean : 36.6119**

**Gaus Width: 3.4803**



# B1L103S, U2-ch67, adc2

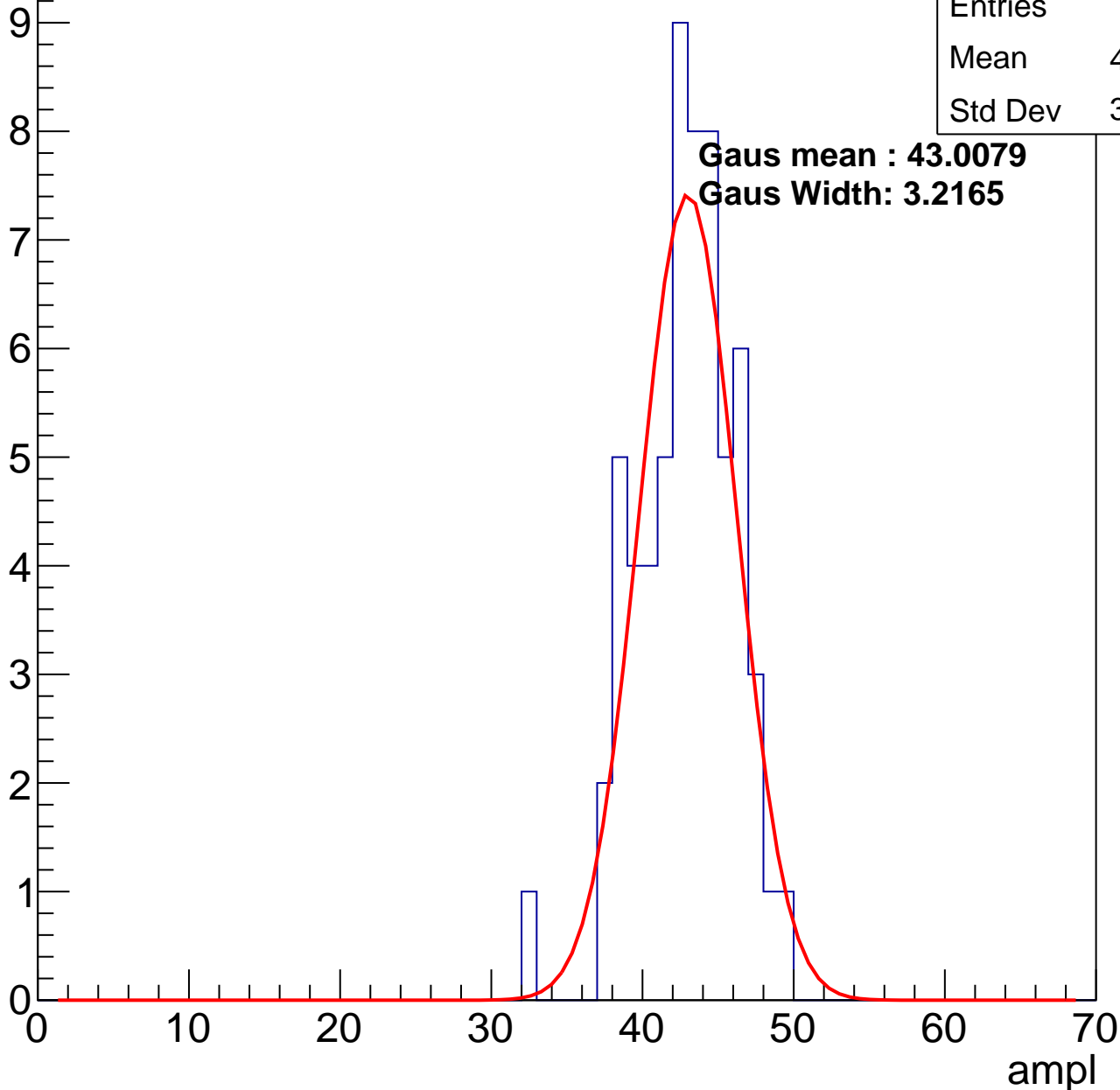
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	42.42
Std Dev	3.155

**Gaus mean : 43.0079**

**Gaus Width: 3.2165**

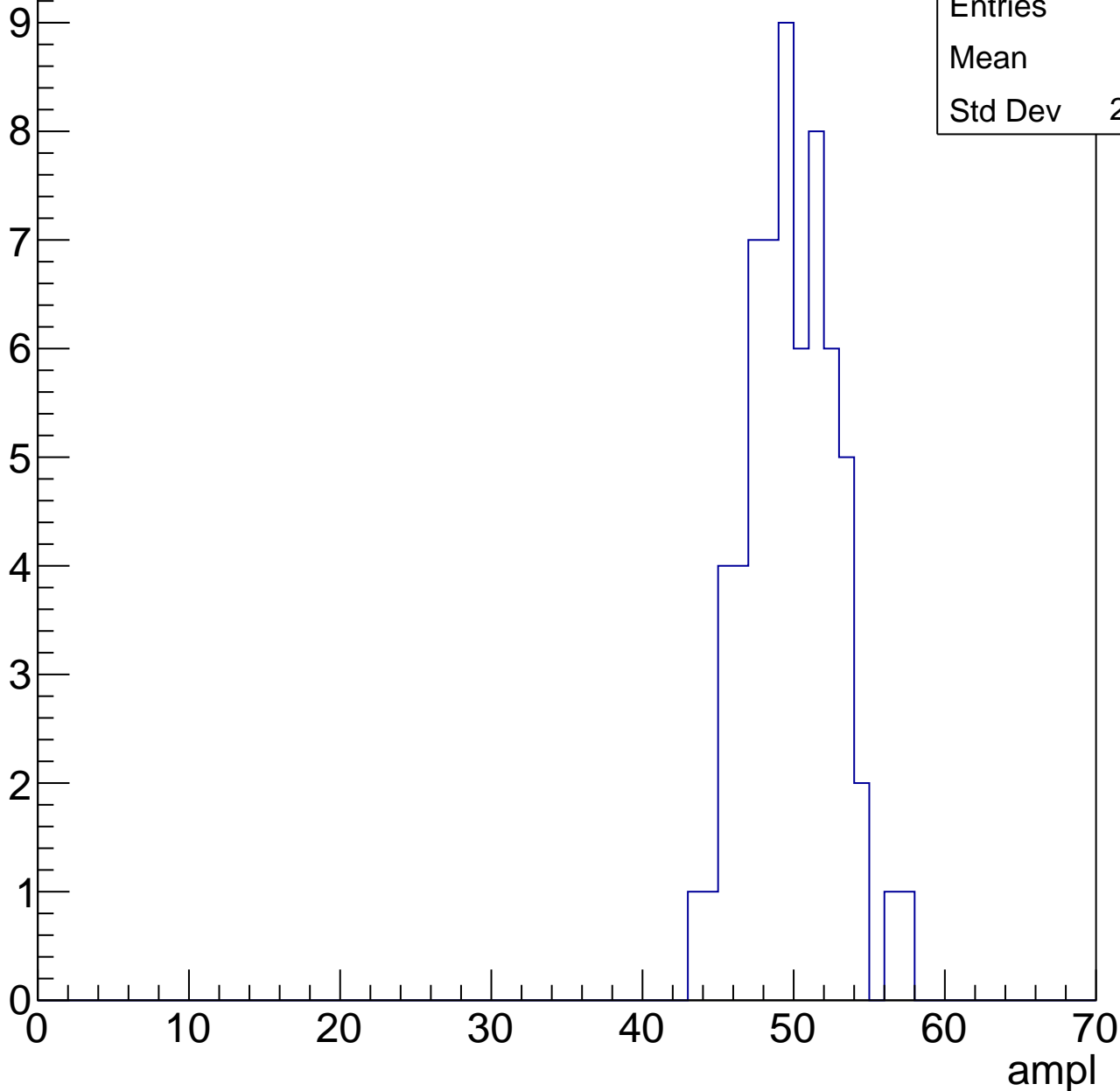


# B1L103S, U2-ch67, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	49.4
Std Dev	2.899

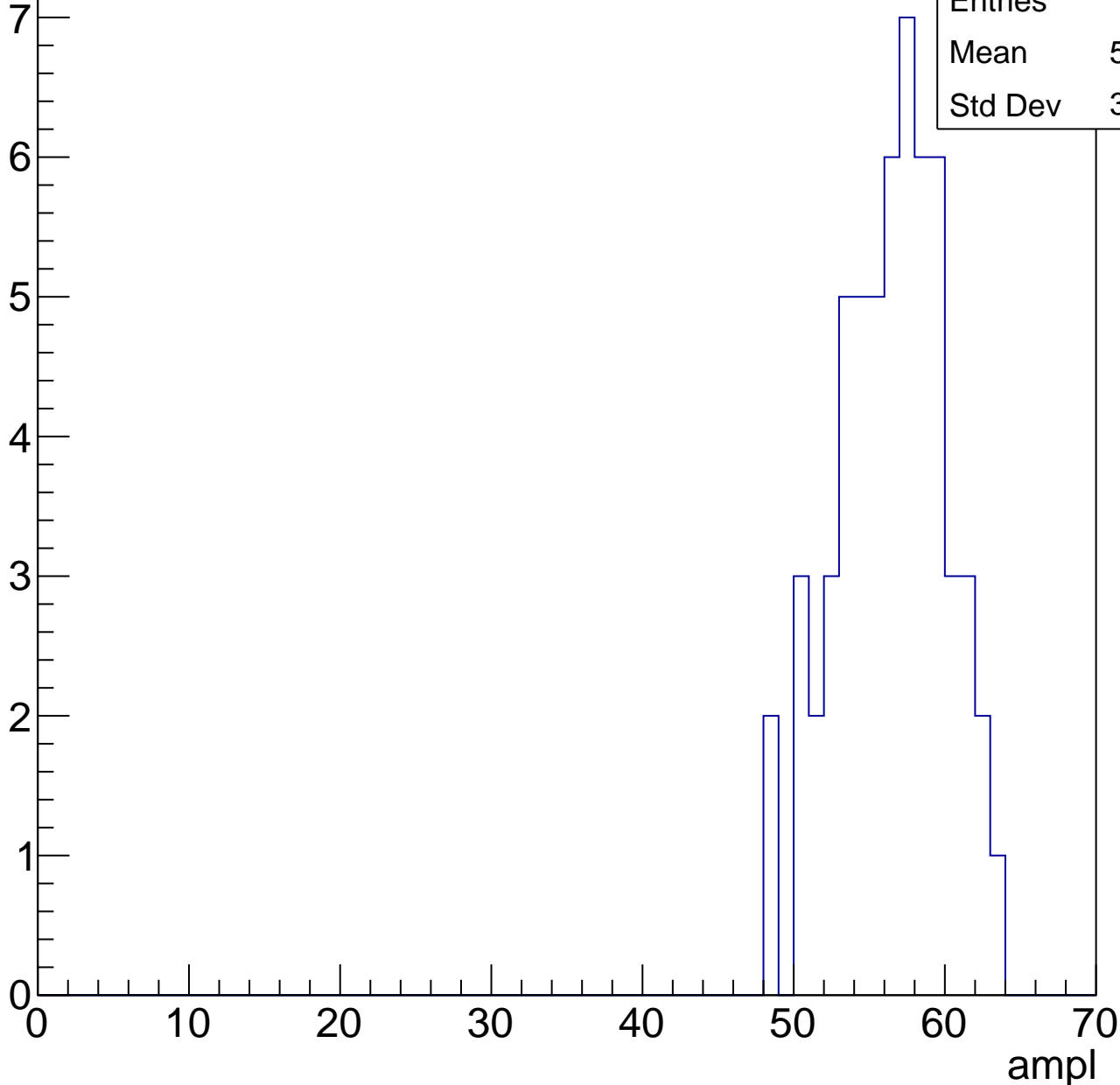


# B1L103S, U2-ch67, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	55.95
Std Dev	3.524

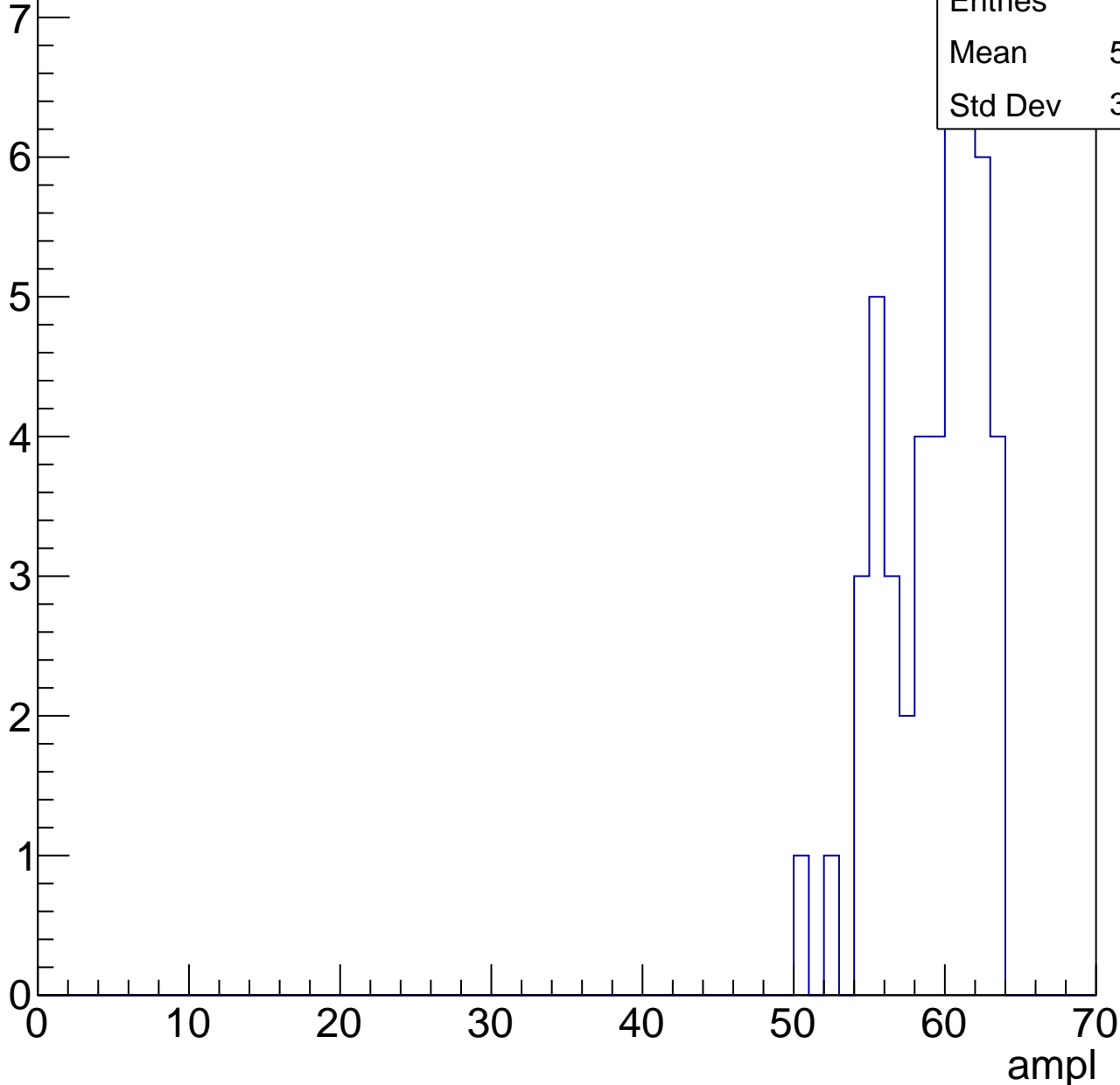


# B1L103S, U2-ch67, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	47
Mean	58.72
Std Dev	3.174

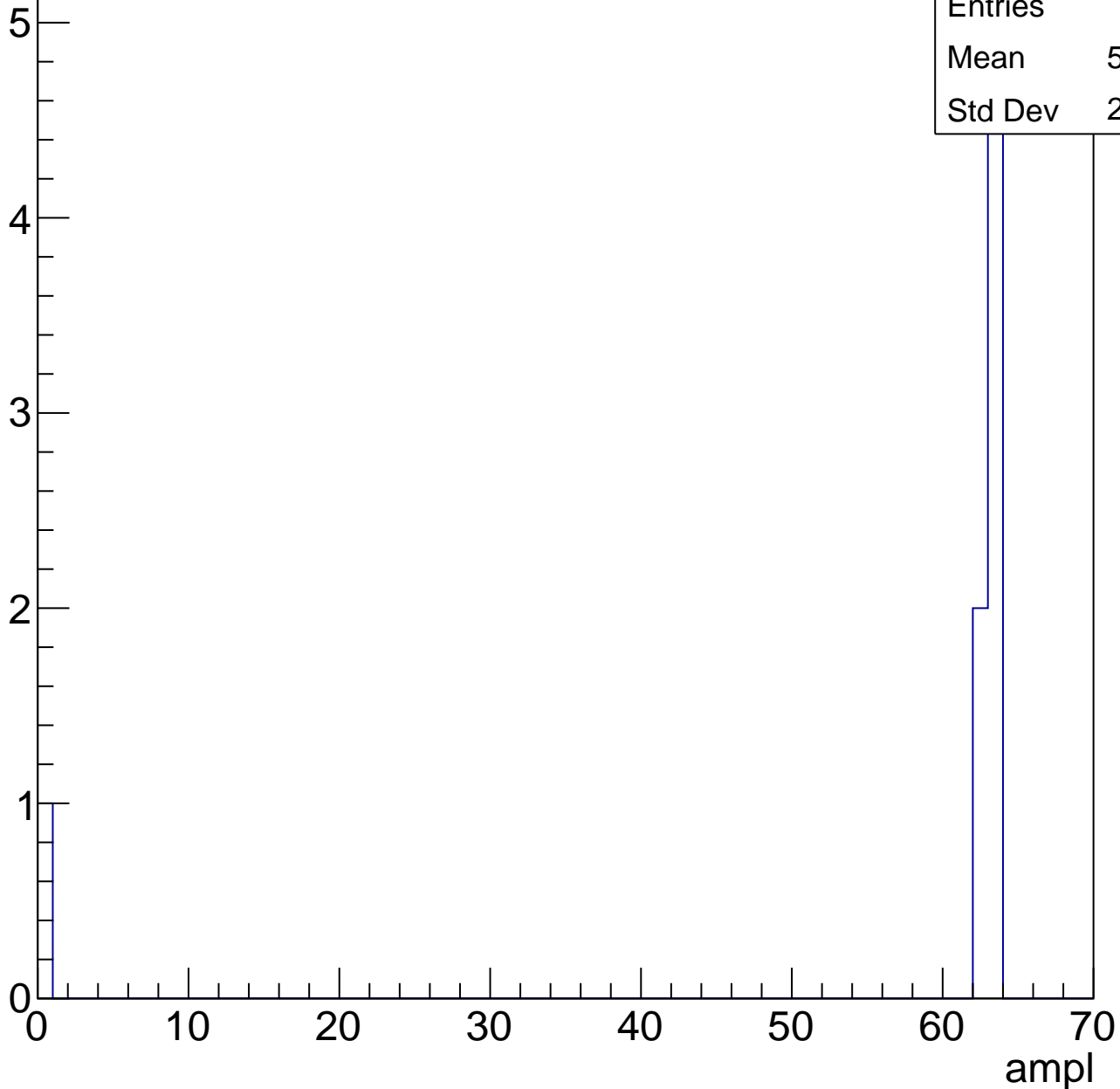


# B1L103S, U2-ch67, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	8
Mean	54.88
Std Dev	20.75





# B1L103S, U2-ch67, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U2-ch68, adc0

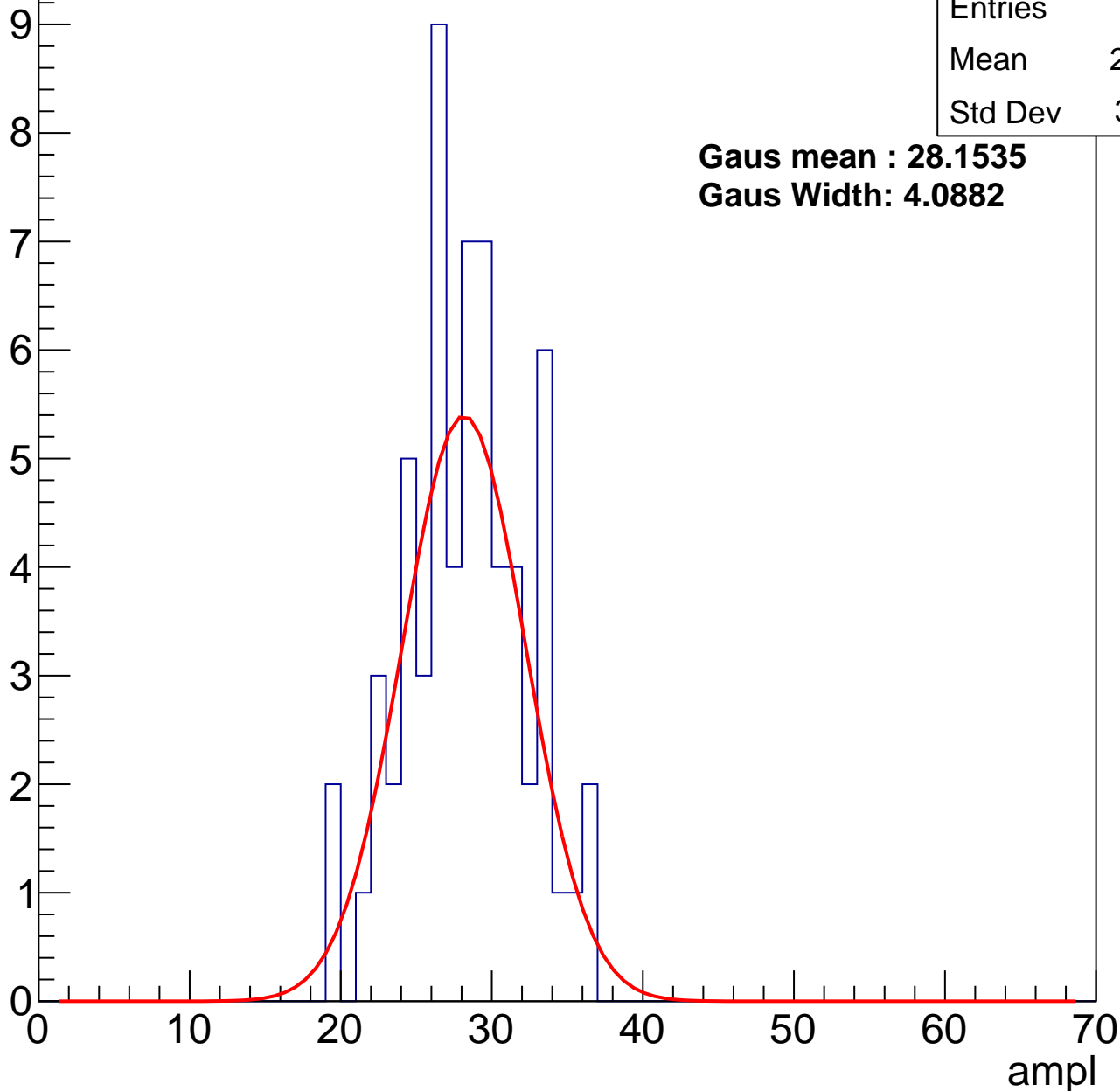
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	27.84
Std Dev	3.921

**Gaus mean : 28.1535**

**Gaus Width: 4.0882**



# B1L103S, U2-ch68, adc1

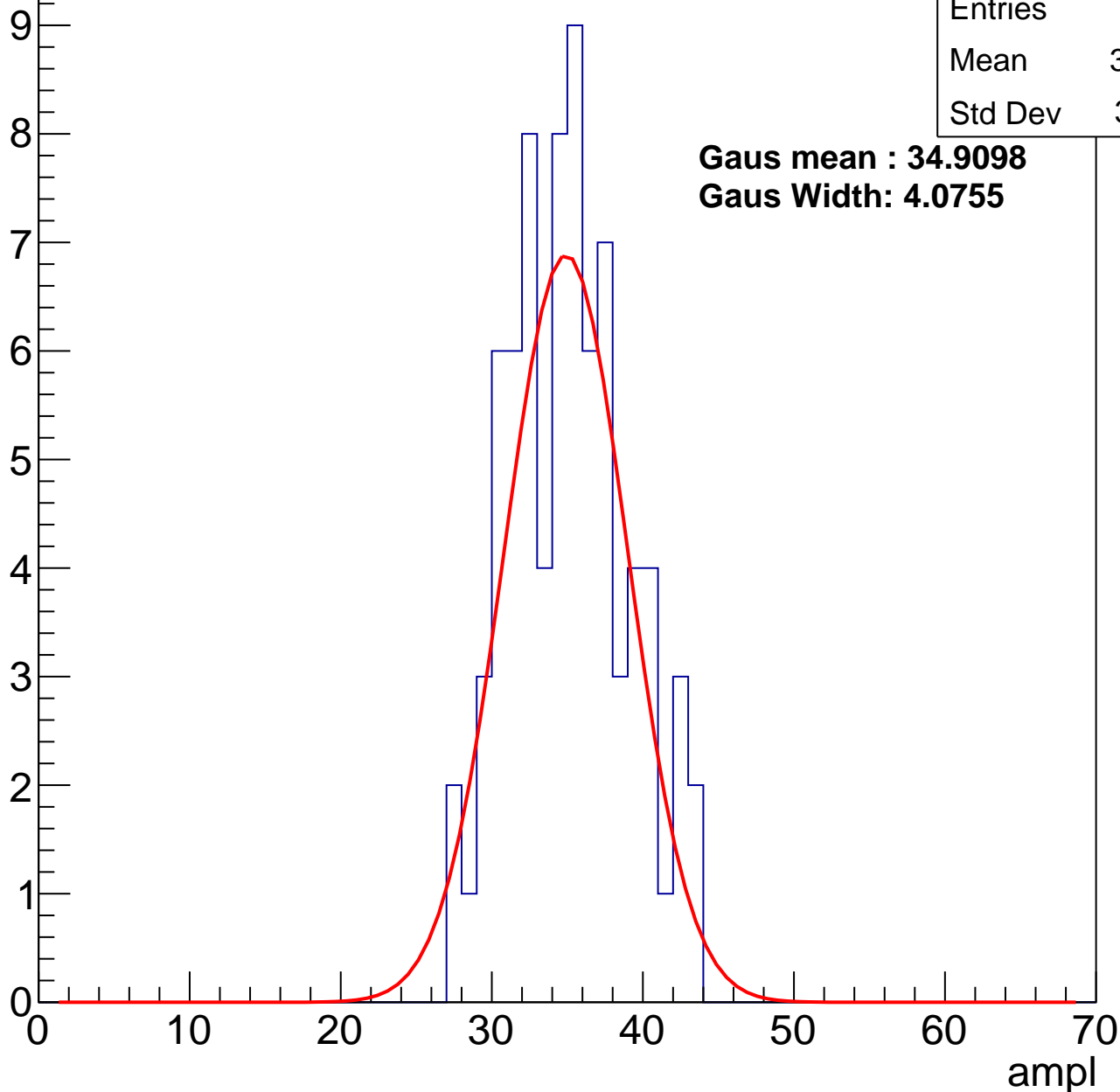
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	34.65
Std Dev	3.871

**Gaus mean : 34.9098**

**Gaus Width: 4.0755**

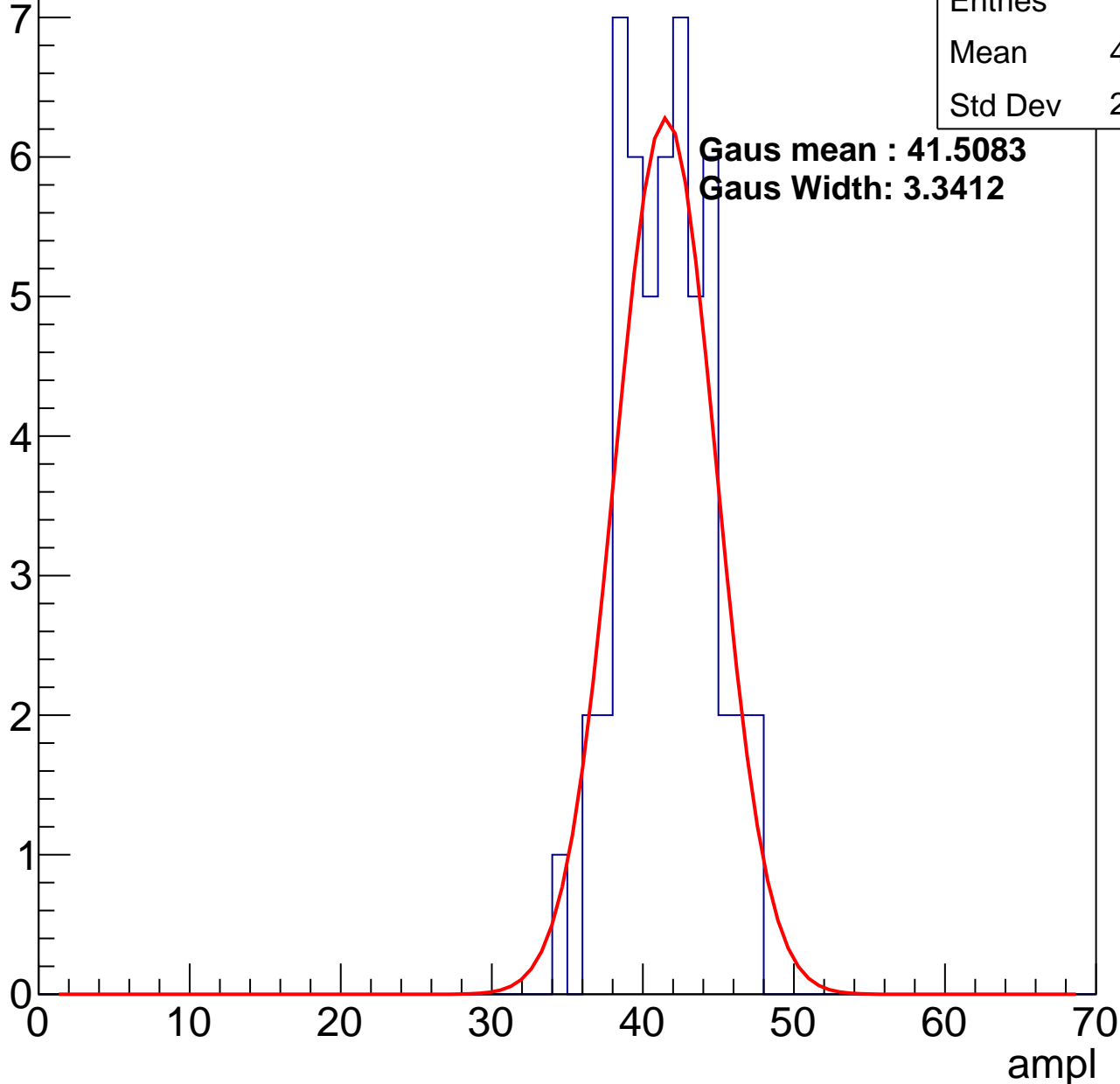


# B1L103S, U2-ch68, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	41.04
Std Dev	2.939

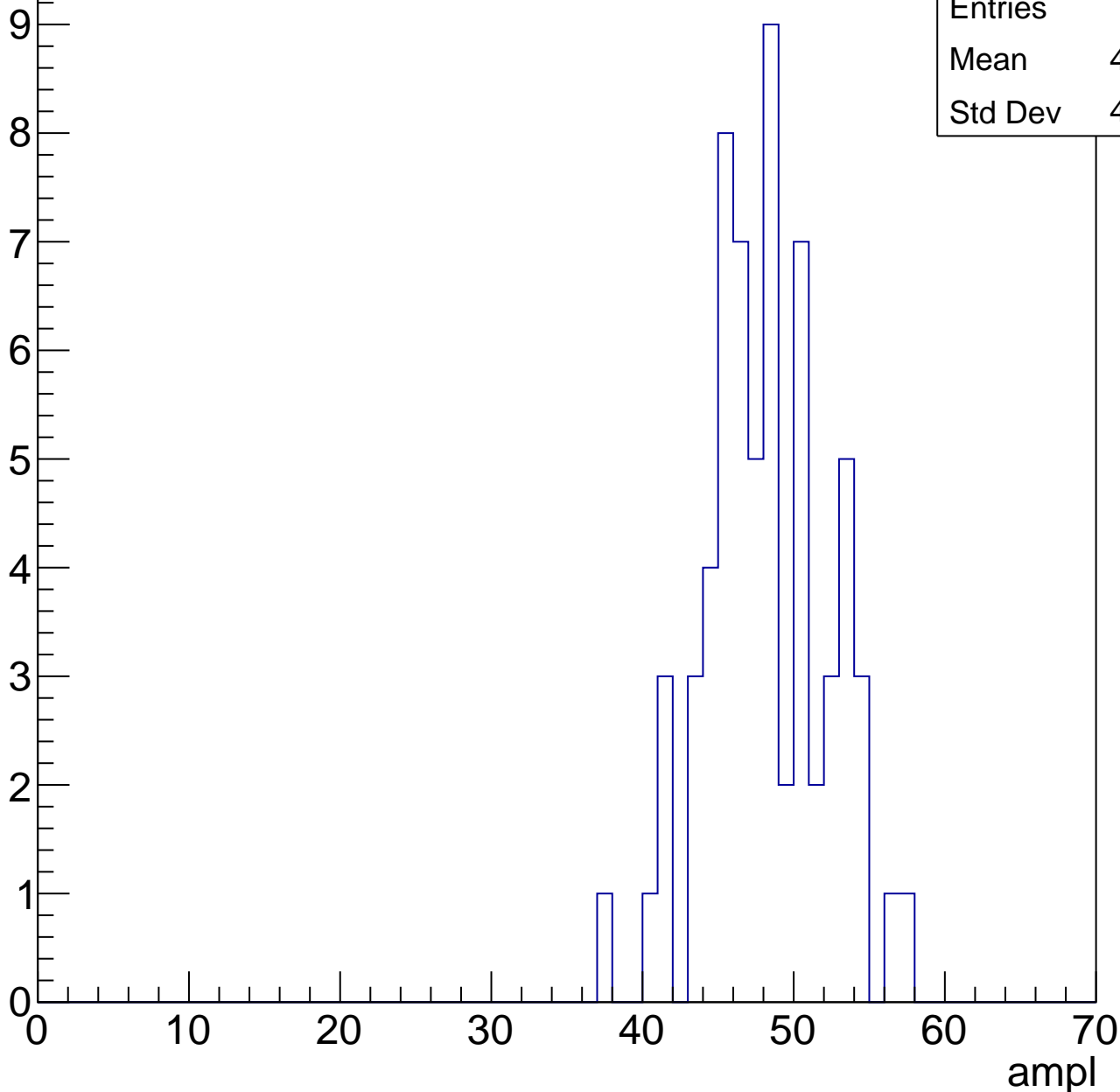


# B1L103S, U2-ch68, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

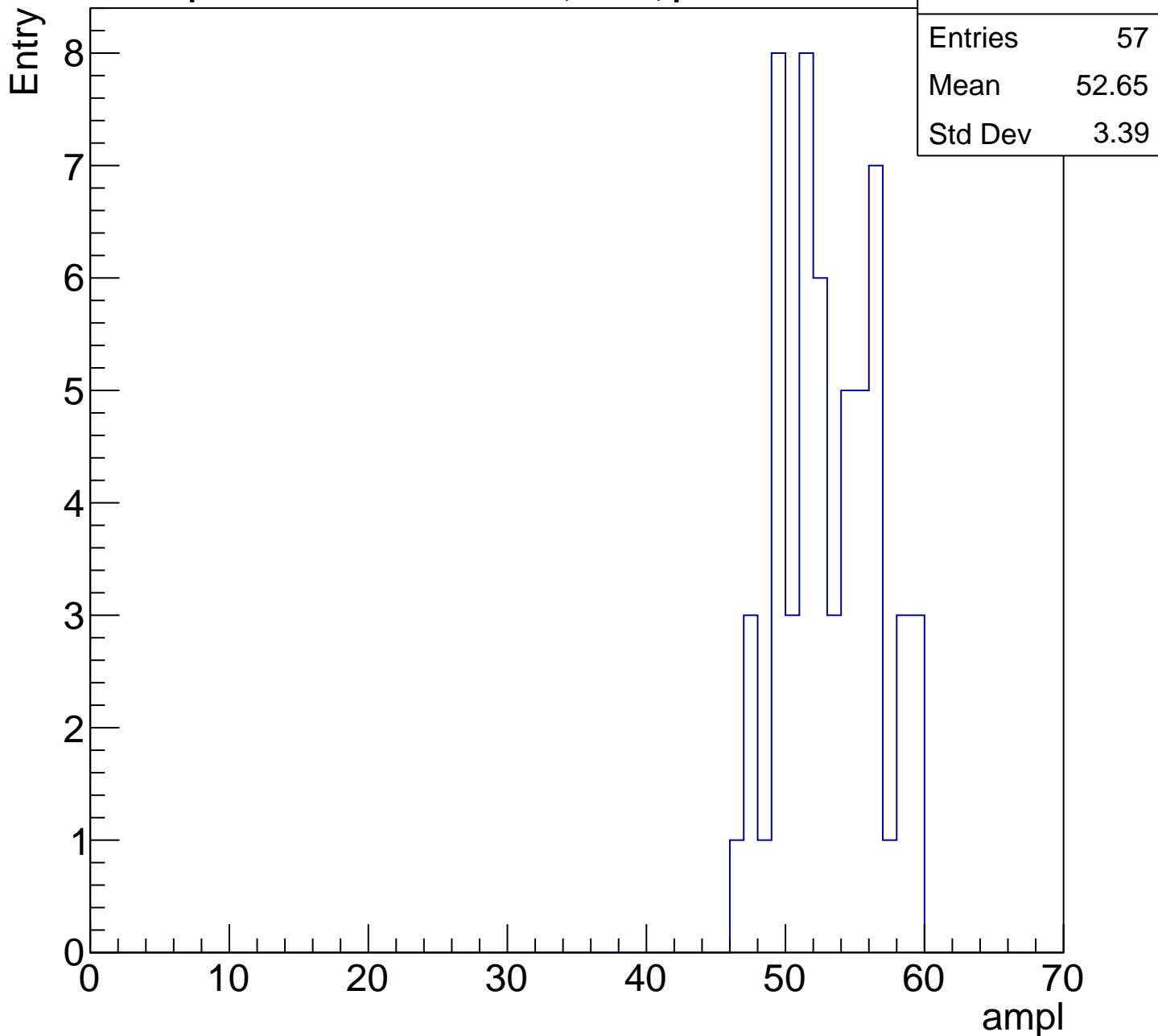
Entry

Entries	65
Mean	47.69
Std Dev	4.007



# B1L103S, U2-ch68, adc4

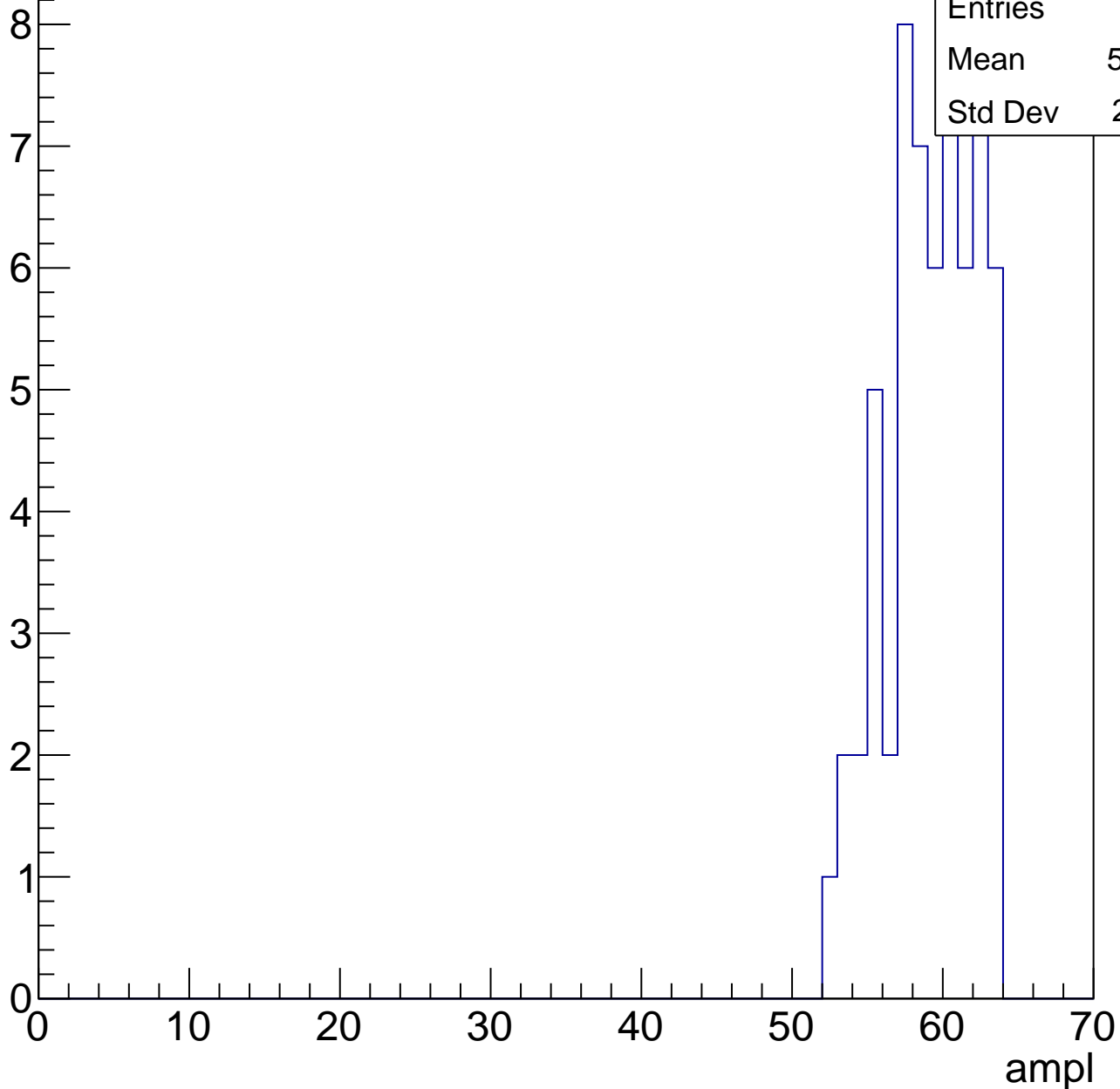
calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U2-ch68, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

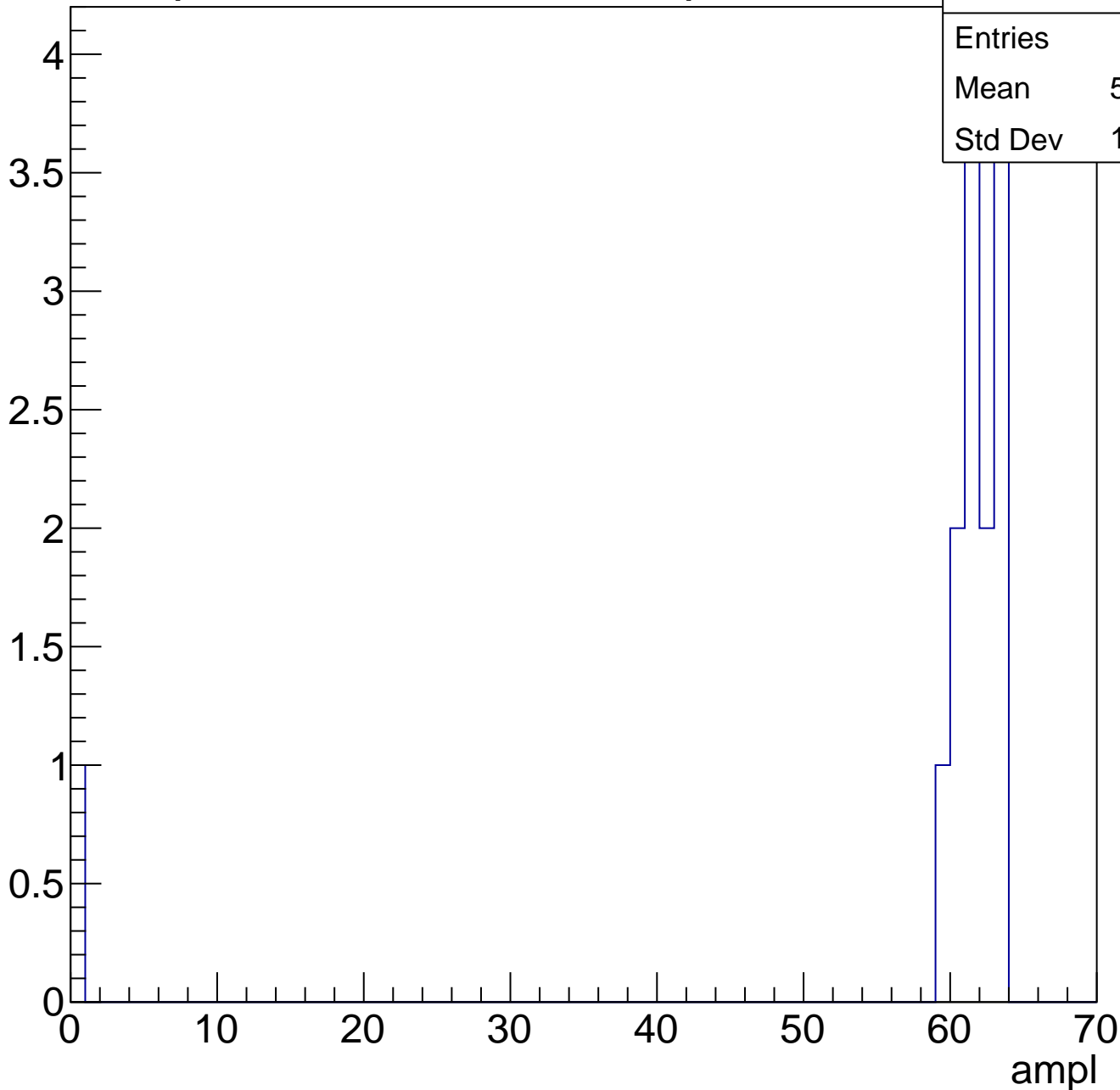


Entries	61
Mean	58.84
Std Dev	2.881

# B1L103S, U2-ch68, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

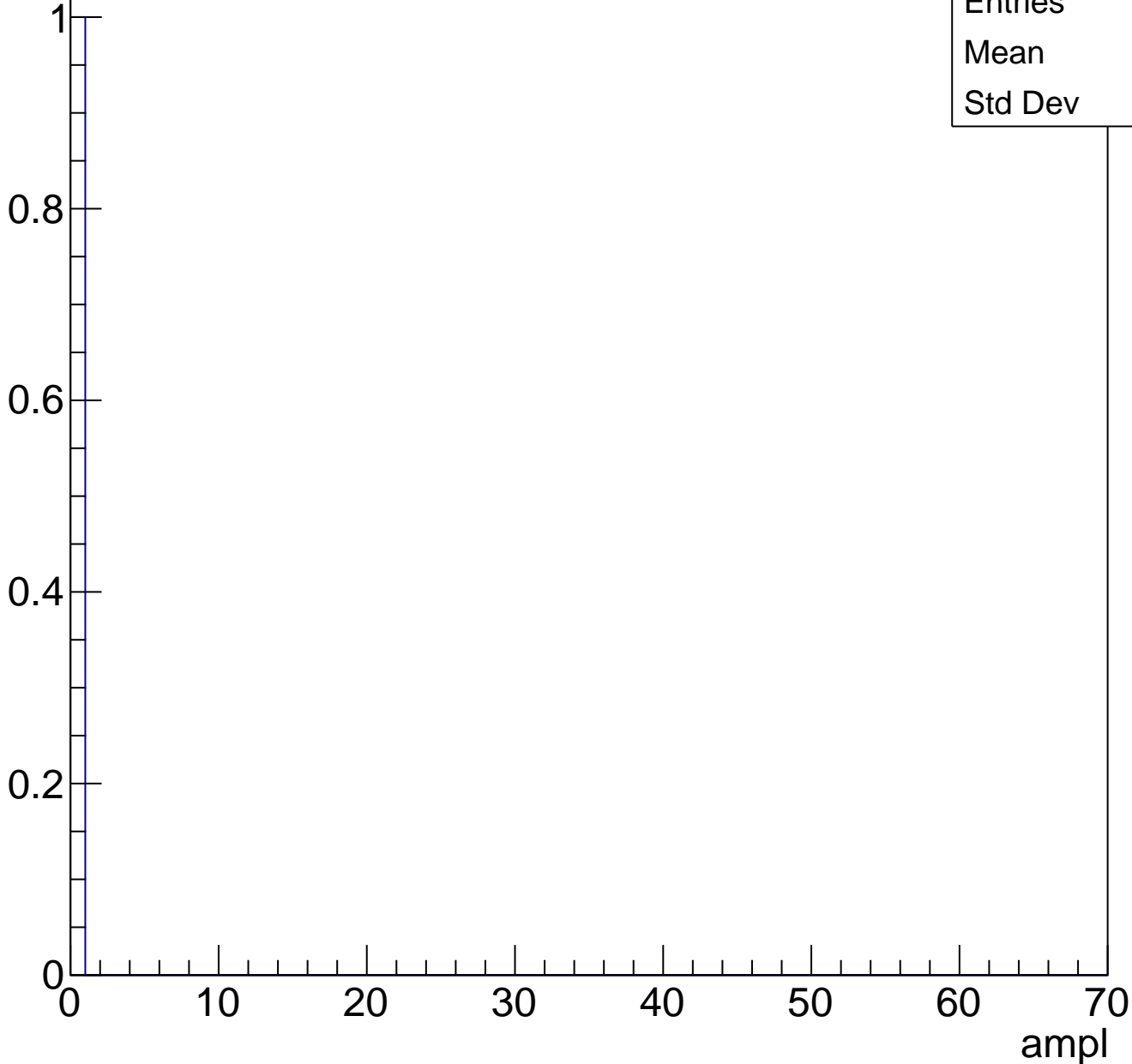




# B1L103S, U2-ch68, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U2-ch69, adc0

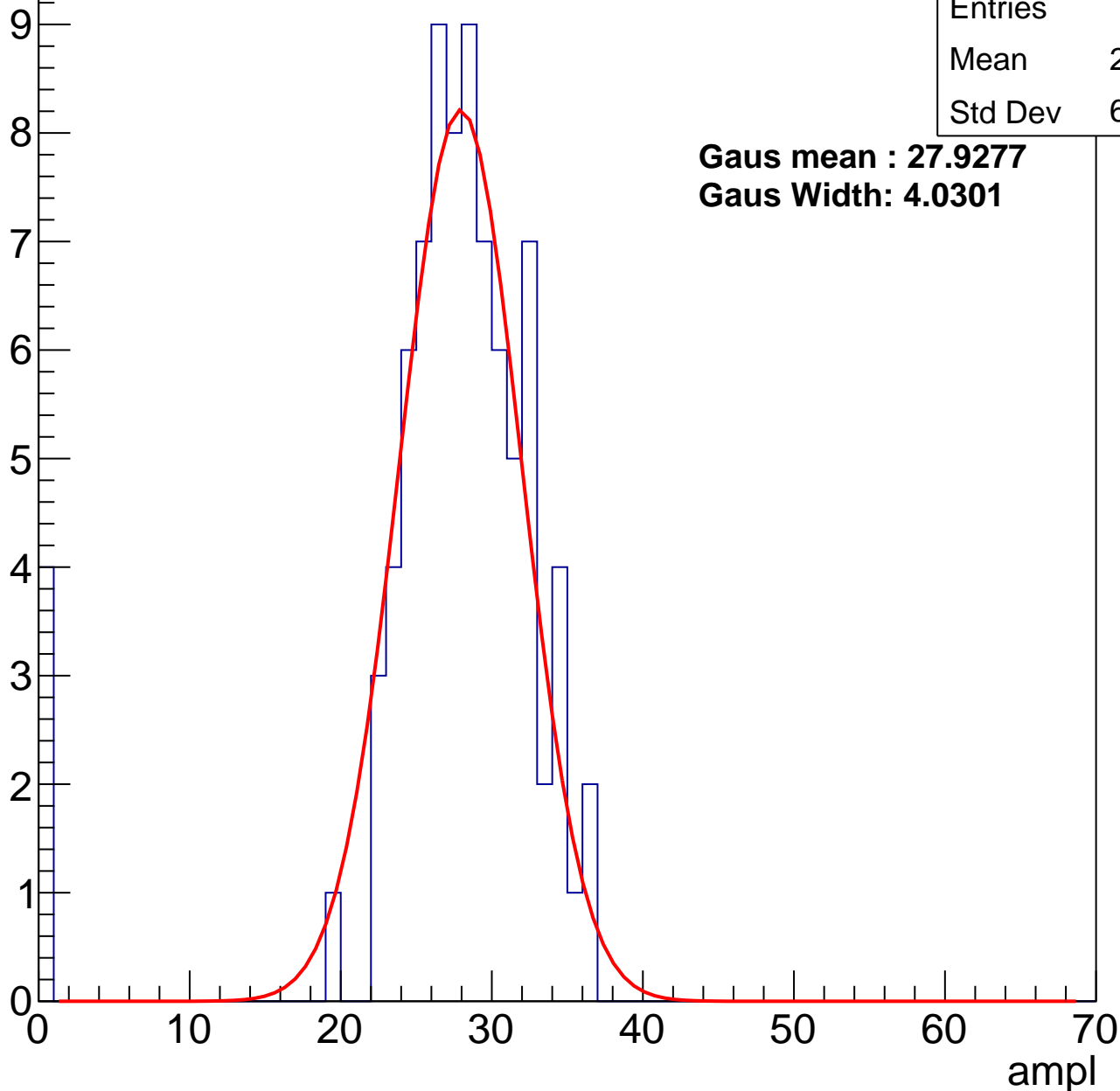
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	85
Mean	26.69
Std Dev	6.896

**Gaus mean : 27.9277**

**Gaus Width: 4.0301**



# B1L103S, U2-ch69, adc1

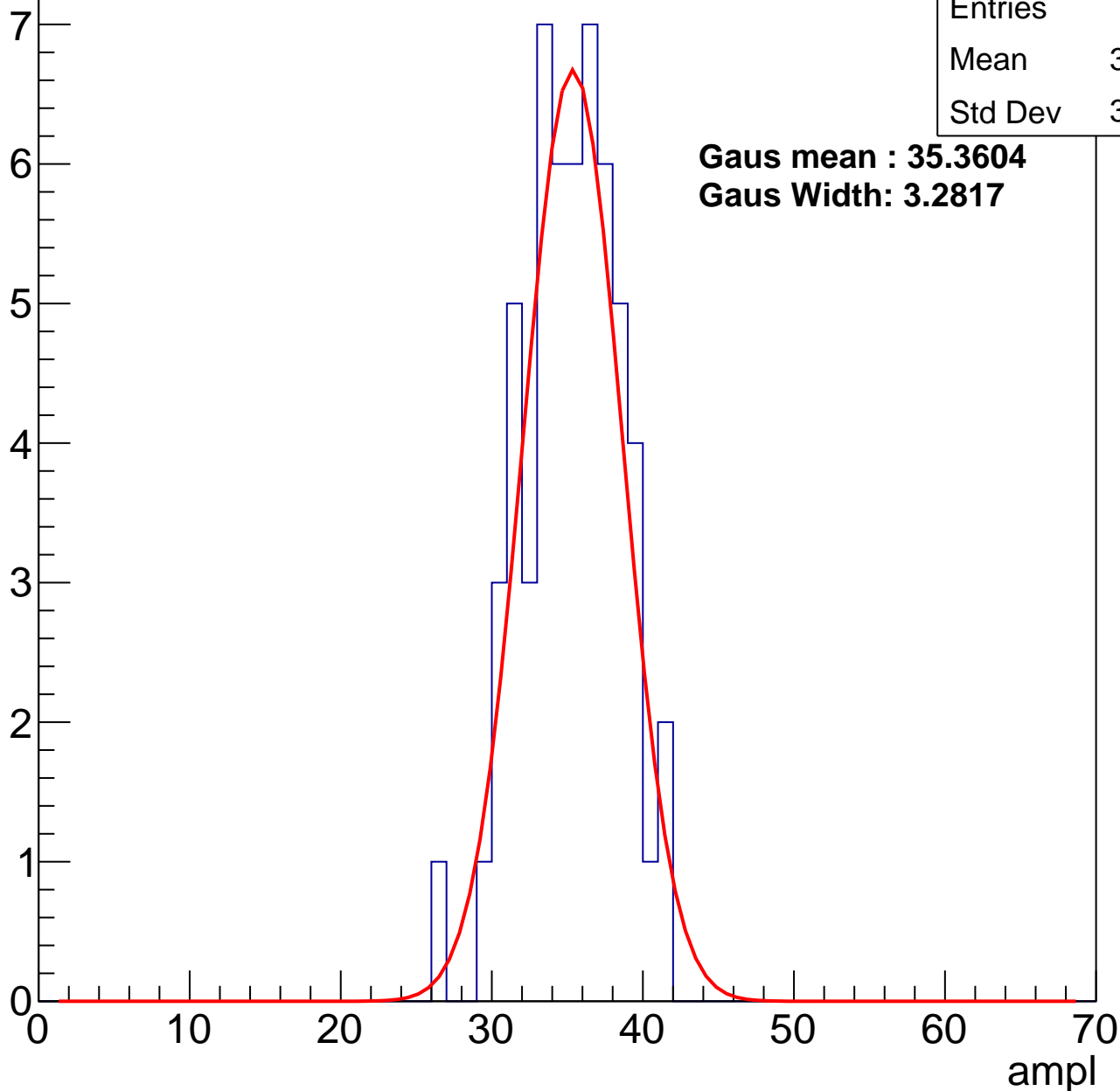
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	34.79
Std Dev	3.155

**Gaus mean : 35.3604**

**Gaus Width: 3.2817**



# B1L103S, U2-ch69, adc2

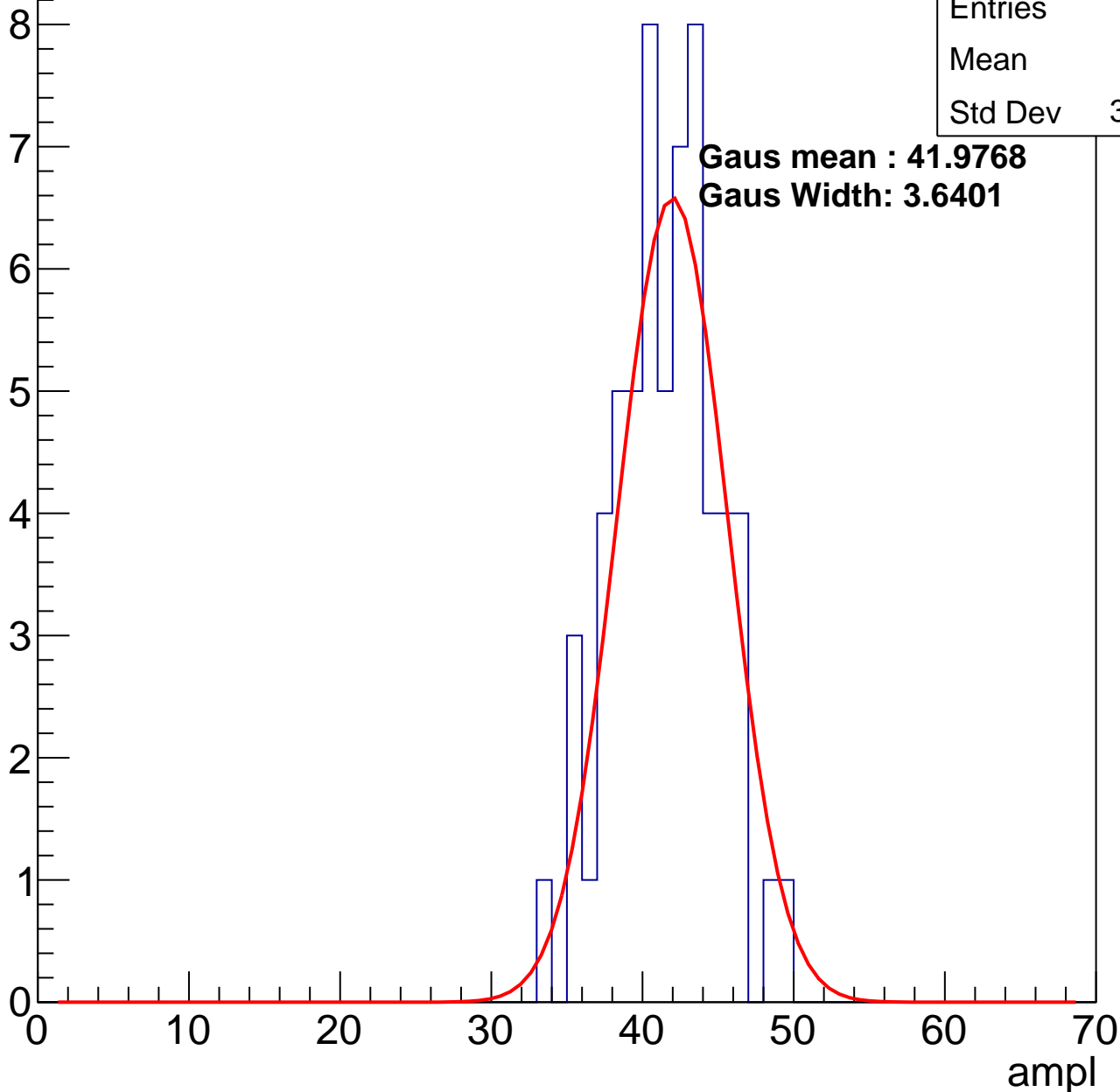
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	41.1
Std Dev	3.352

**Gaus mean : 41.9768**

**Gaus Width: 3.6401**



# B1L103S, U2-ch69, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

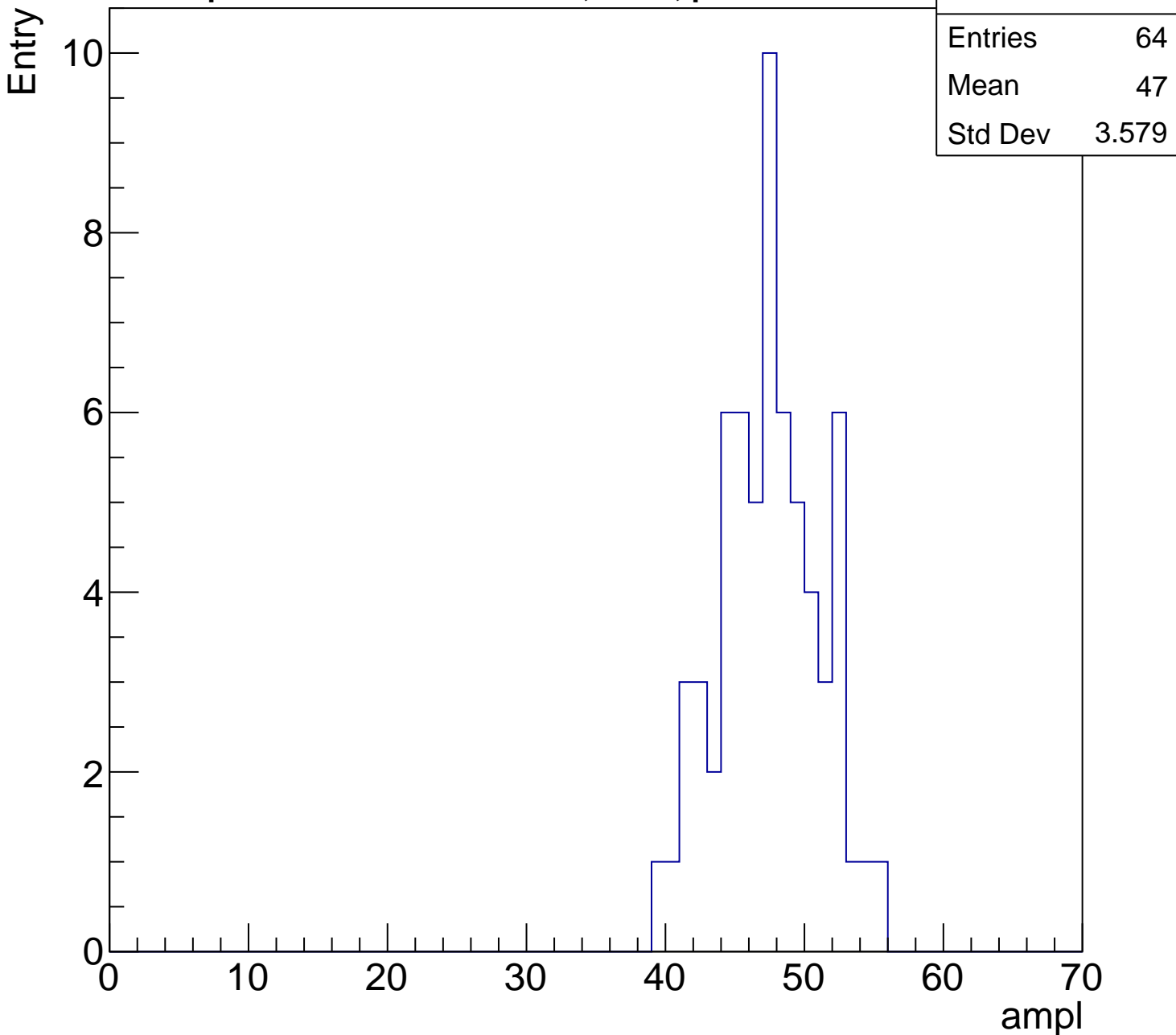
Entries	64
Mean	47
Std Dev	3.579

Entry

10  
8  
6  
4  
2  
0

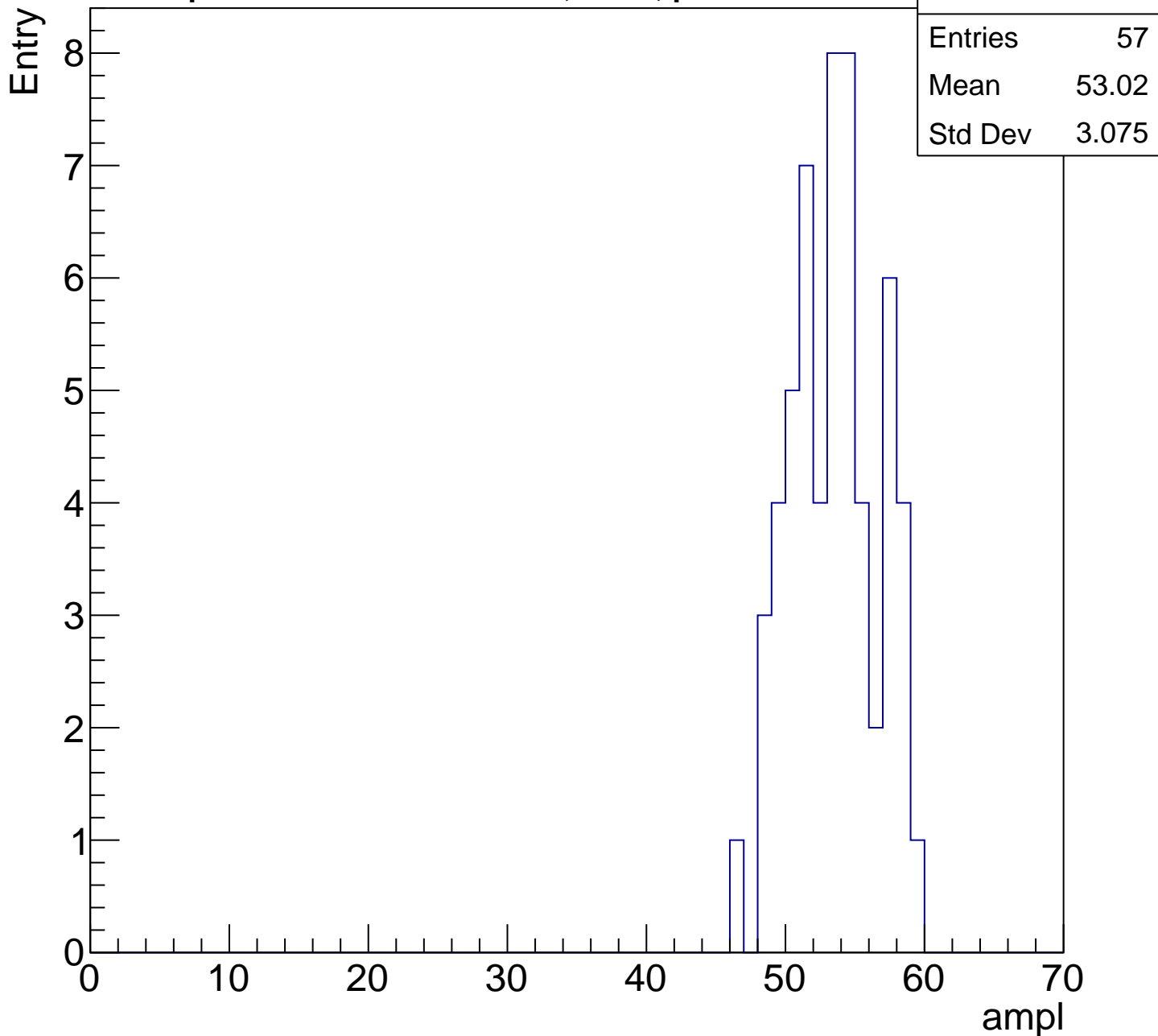
0 10 20 30 40 50 60 70

ampl



# B1L103S, U2-ch69, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

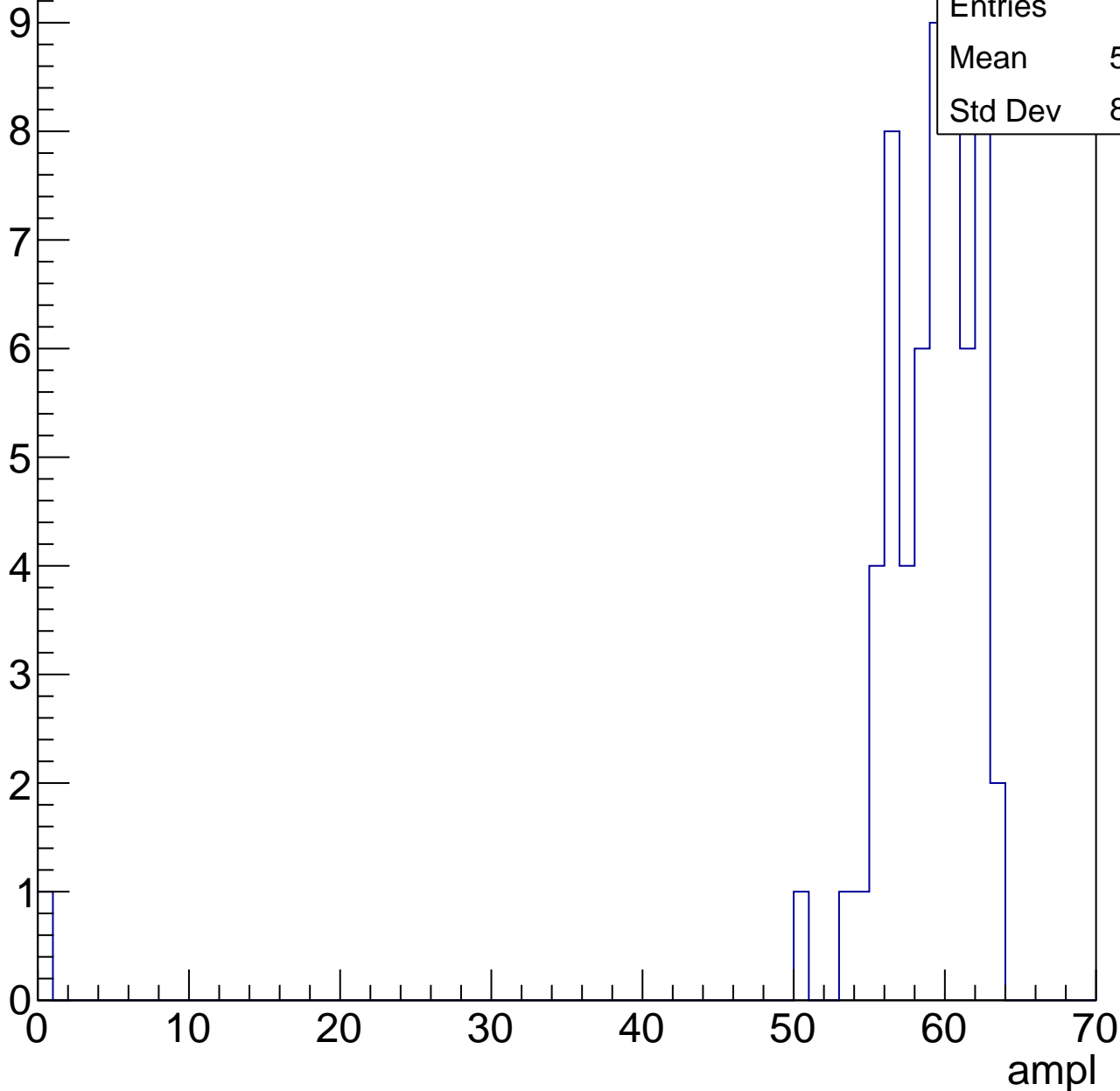


# B1L103S, U2-ch69, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	57.63
Std Dev	8.032

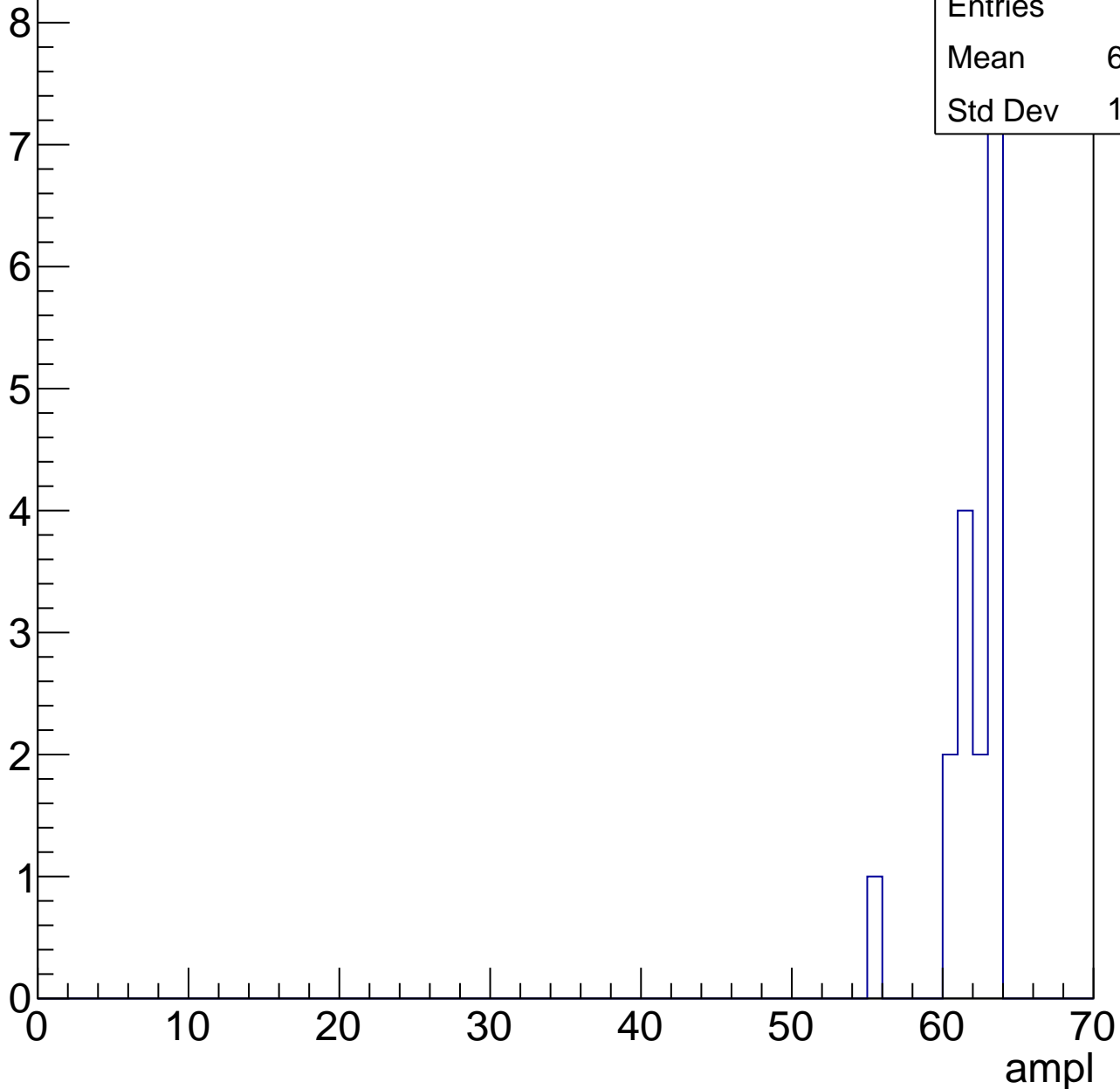


# B1L103S, U2-ch69, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	17
Mean	61.59
Std Dev	1.972

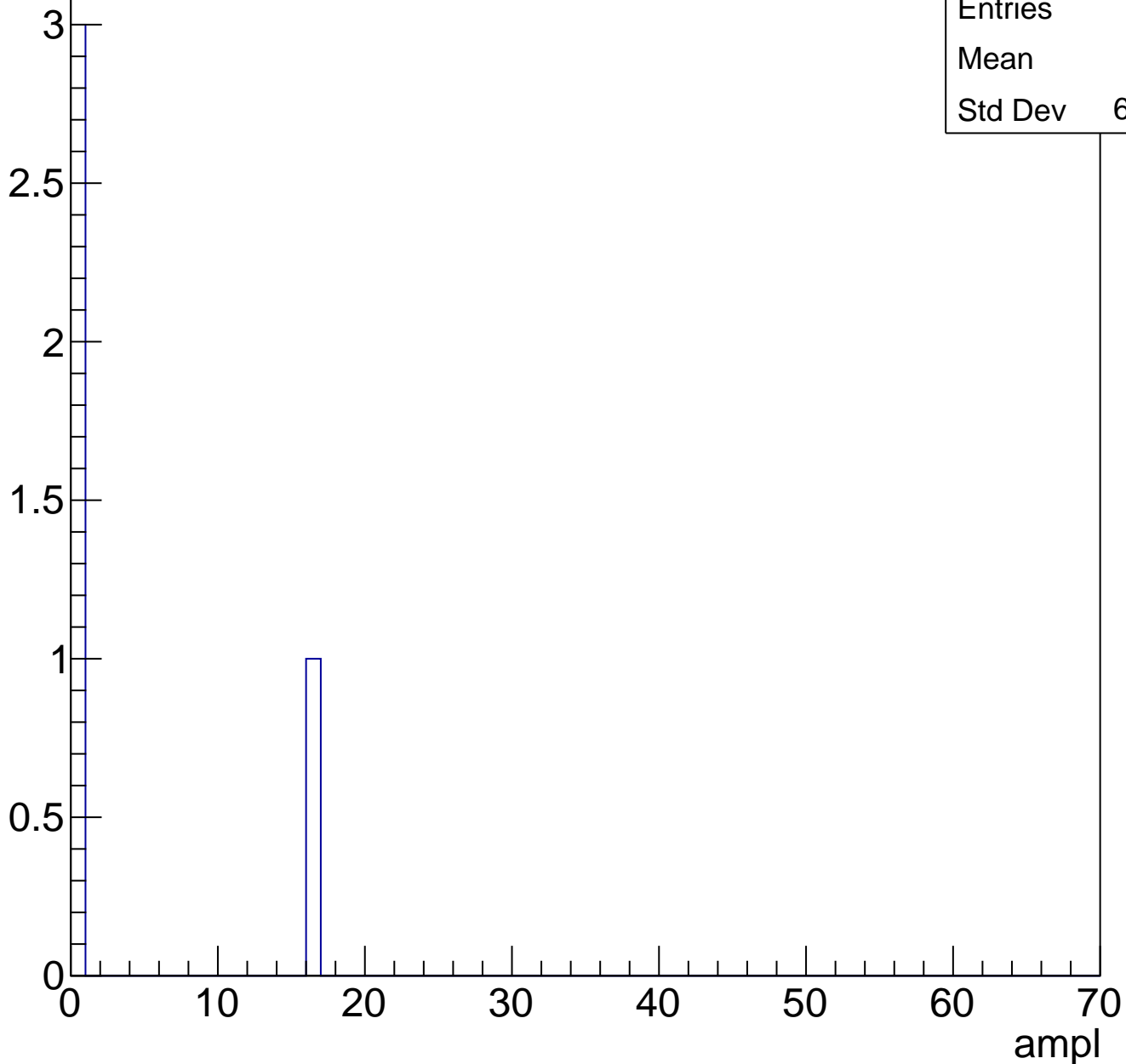




# B1L103S, U2-ch69, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch70, adc0

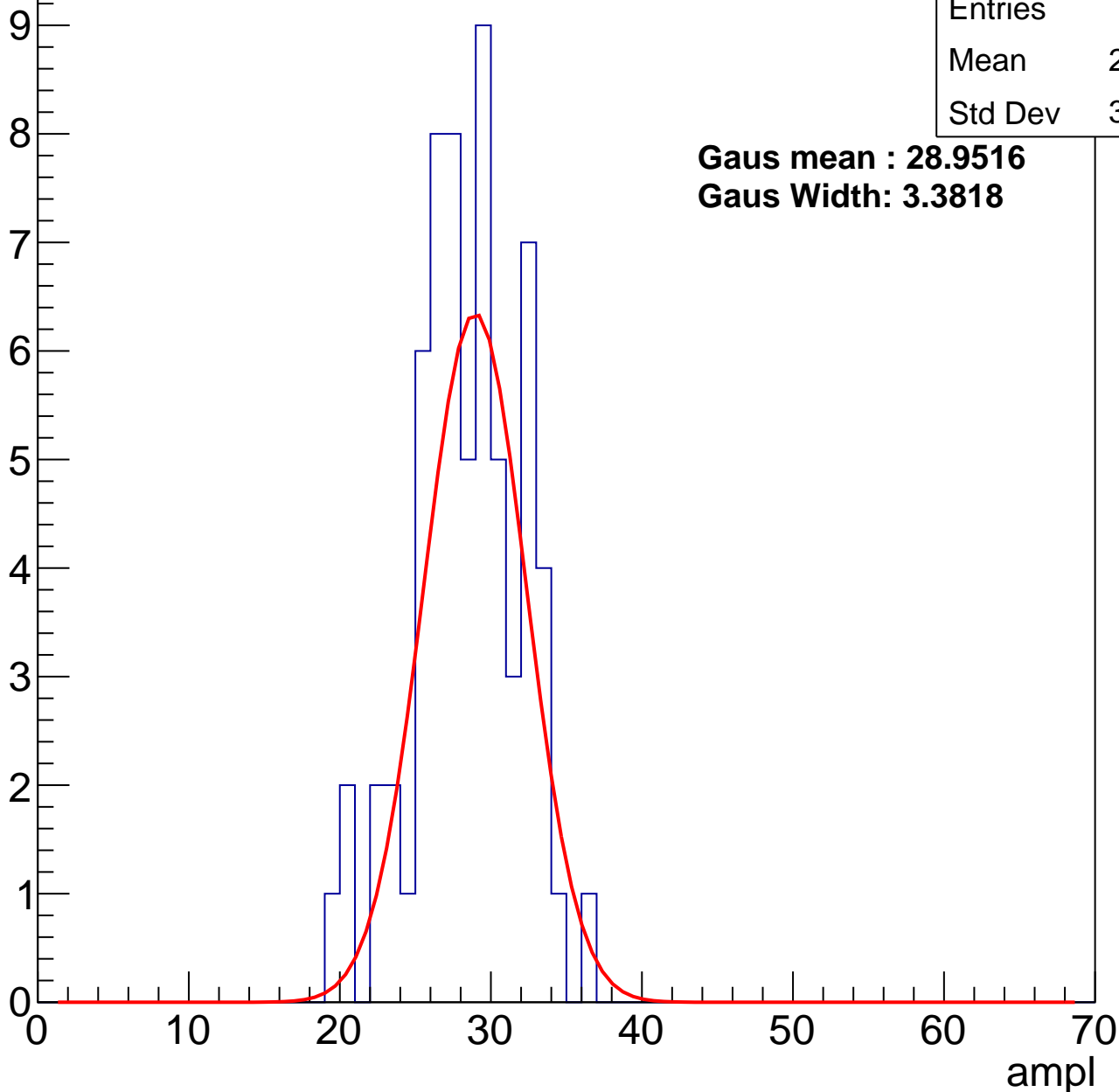
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	27.95
Std Dev	3.528

**Gaus mean : 28.9516**

**Gaus Width: 3.3818**



# B1L103S, U2-ch70, adc1

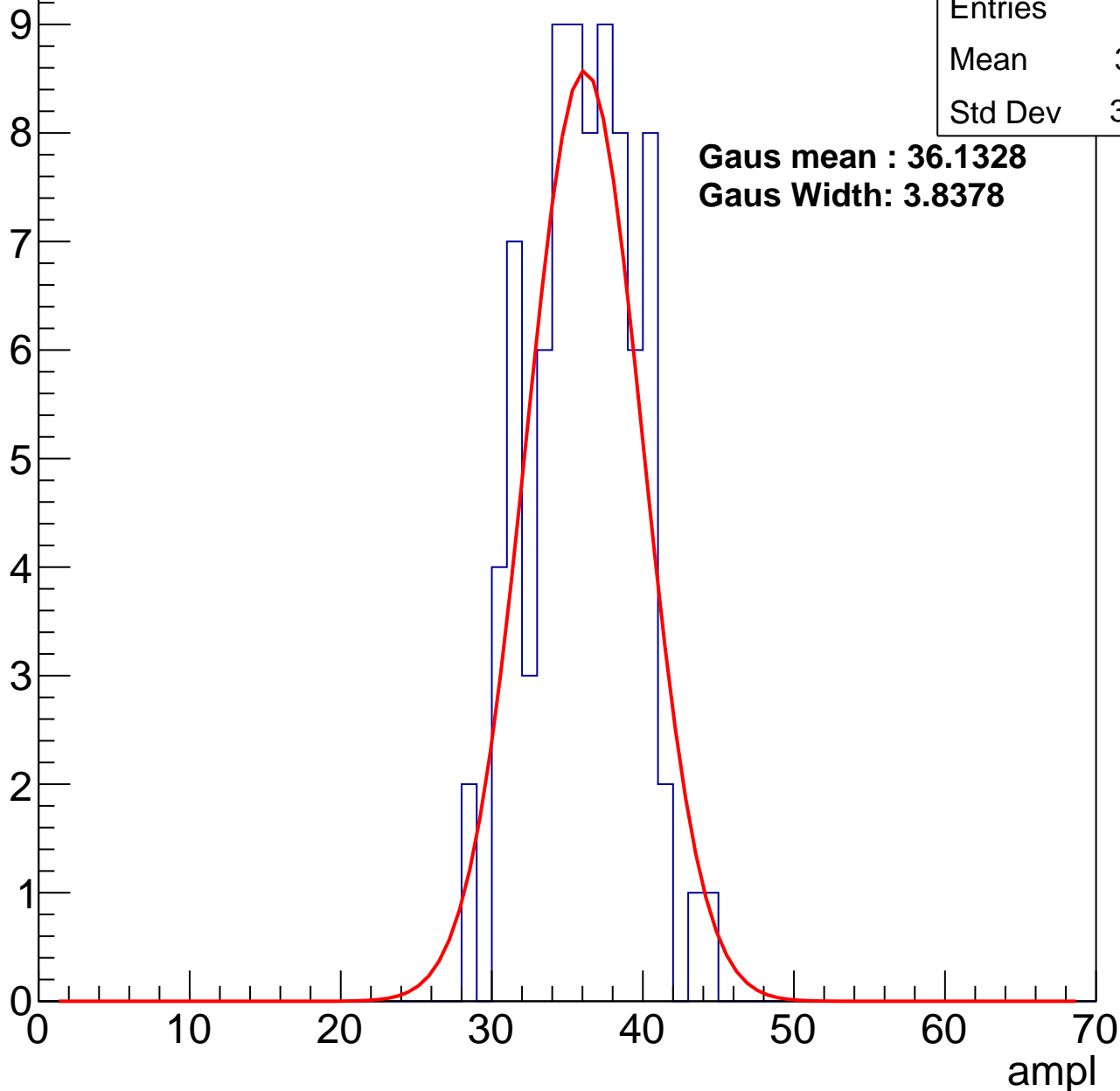
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	83
Mean	35.61
Std Dev	3.414

**Gaus mean : 36.1328**

**Gaus Width: 3.8378**



# B1L103S, U2-ch70, adc2

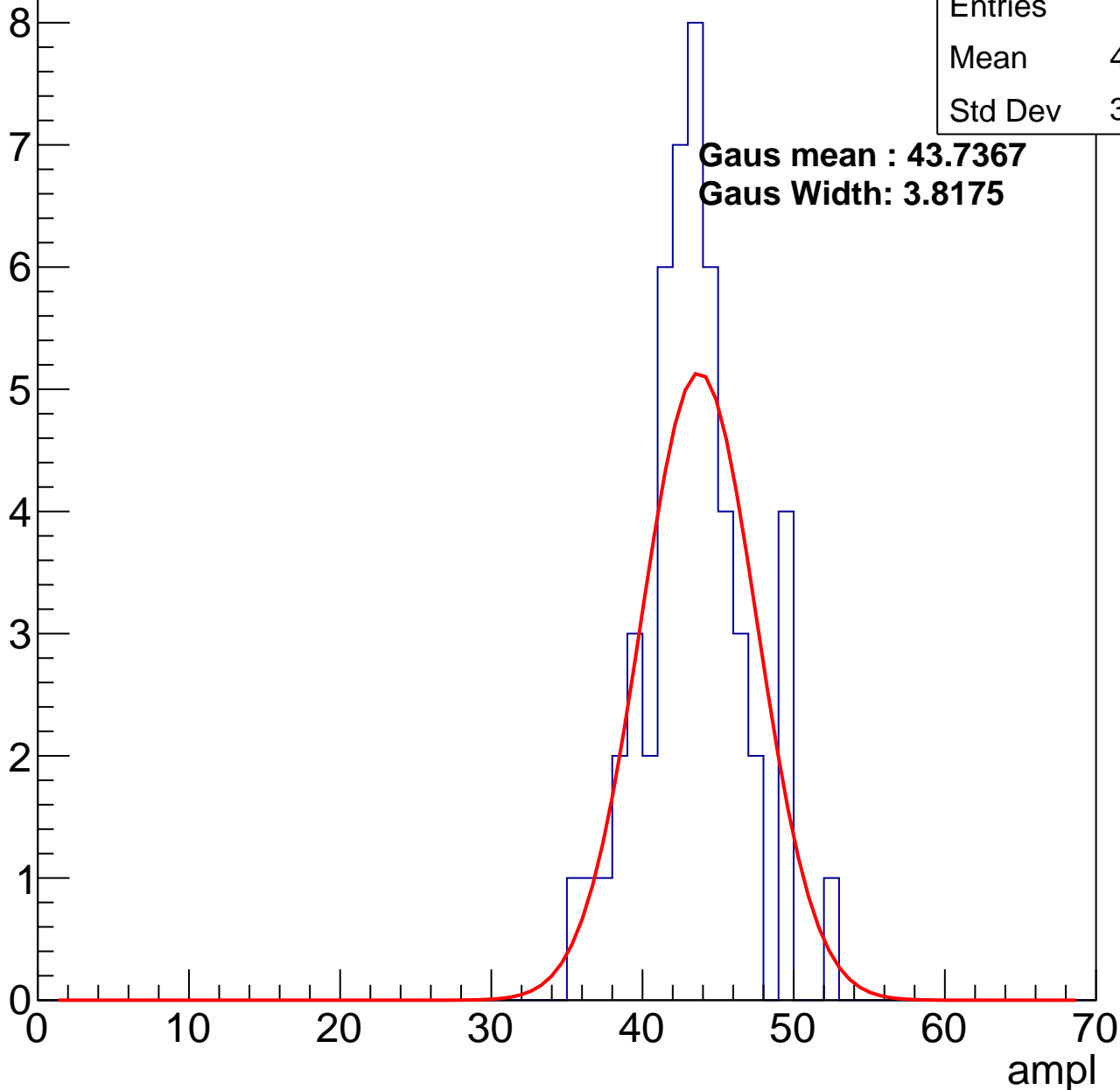
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	42.92
Std Dev	3.435

**Gaus mean : 43.7367**

**Gaus Width: 3.8175**



# B1L103S, U2-ch70, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

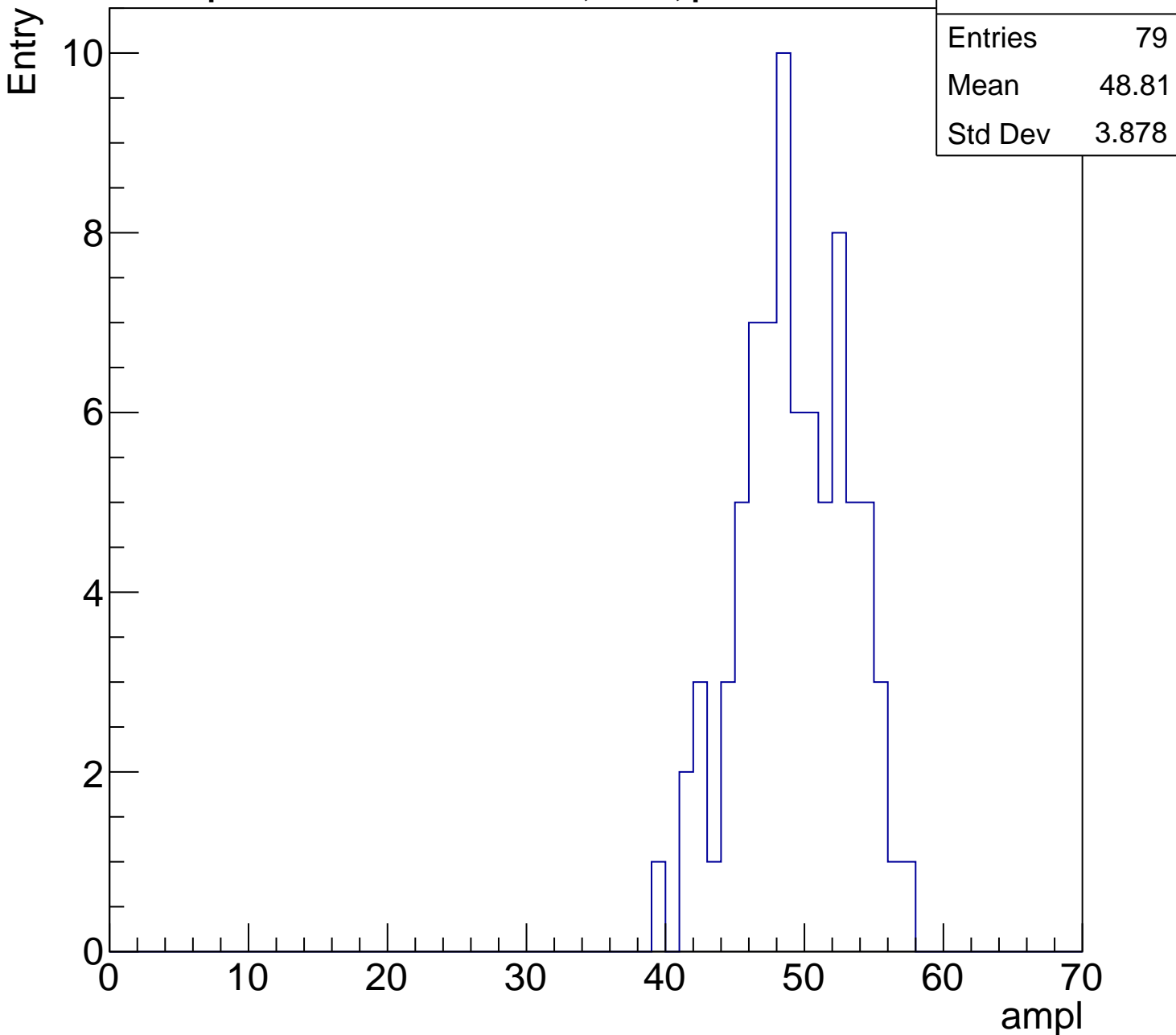
Entries	79
Mean	48.81
Std Dev	3.878

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

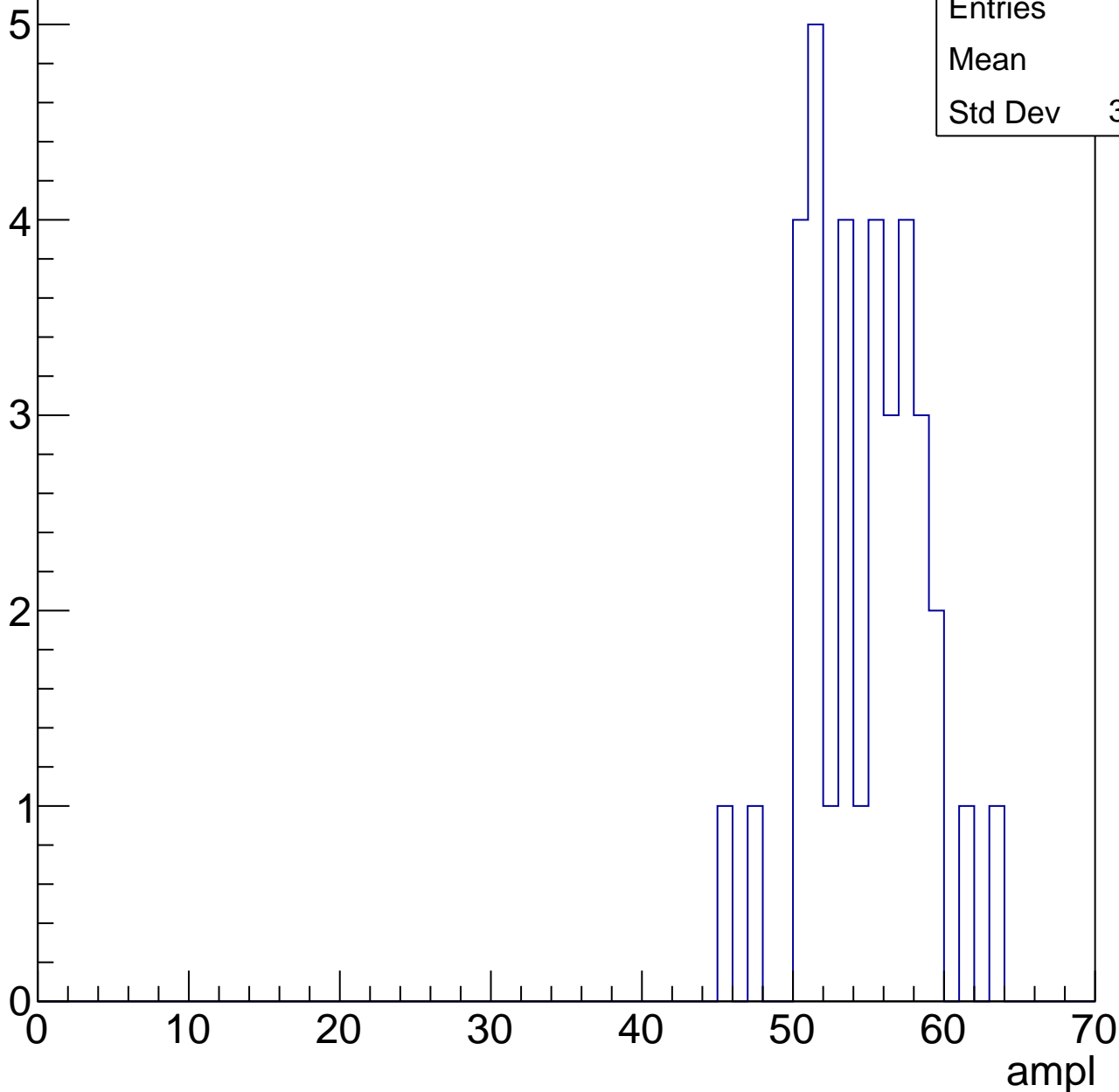


# B1L103S, U2-ch70, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	35
Mean	54.2
Std Dev	3.875



# B1L103S, U2-ch70, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

70

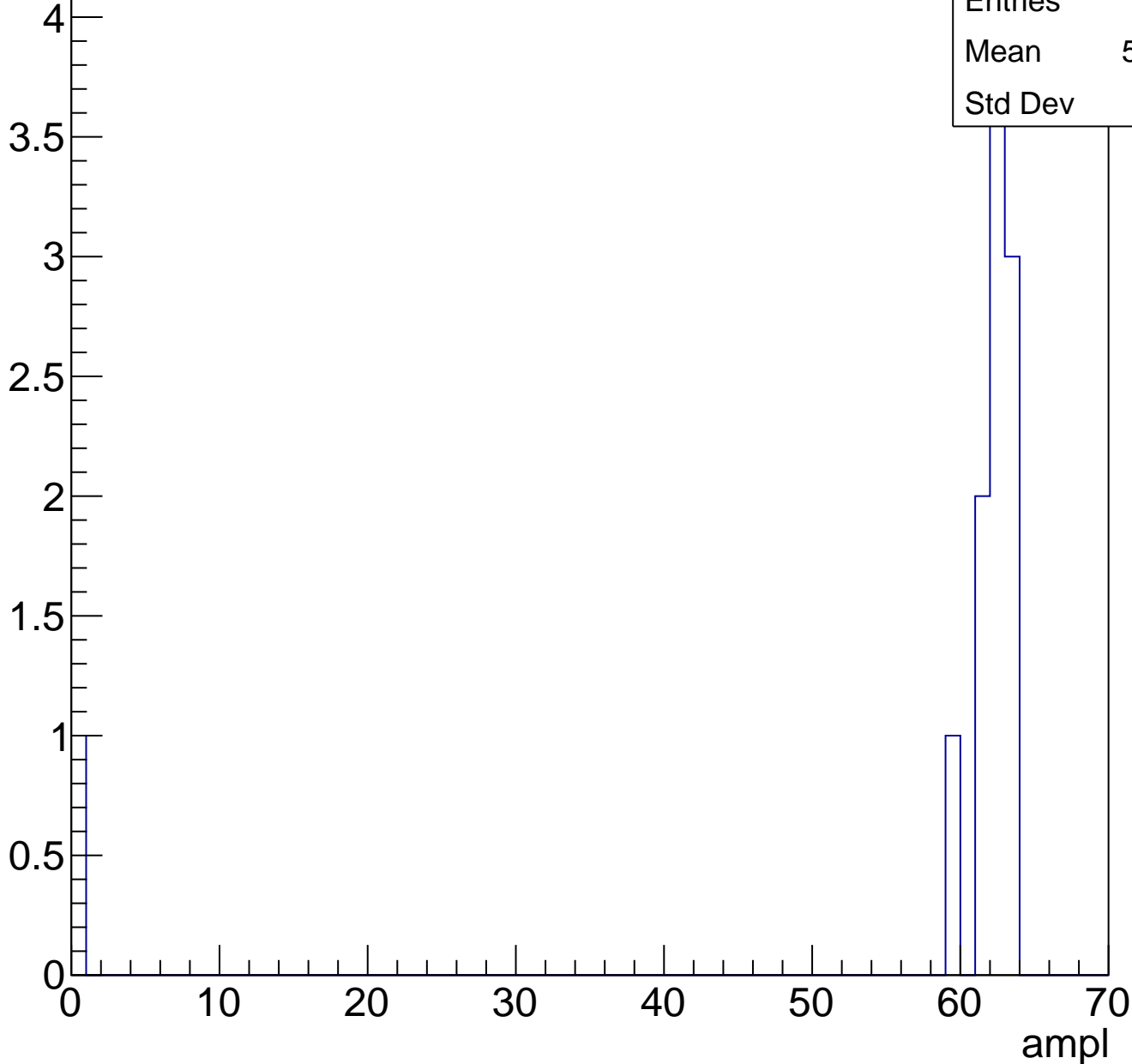
ampl

Entries	62
Mean	58.89
Std Dev	2.701

# B1L103S, U2-ch70, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U2-ch70, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U2-ch71, adc0

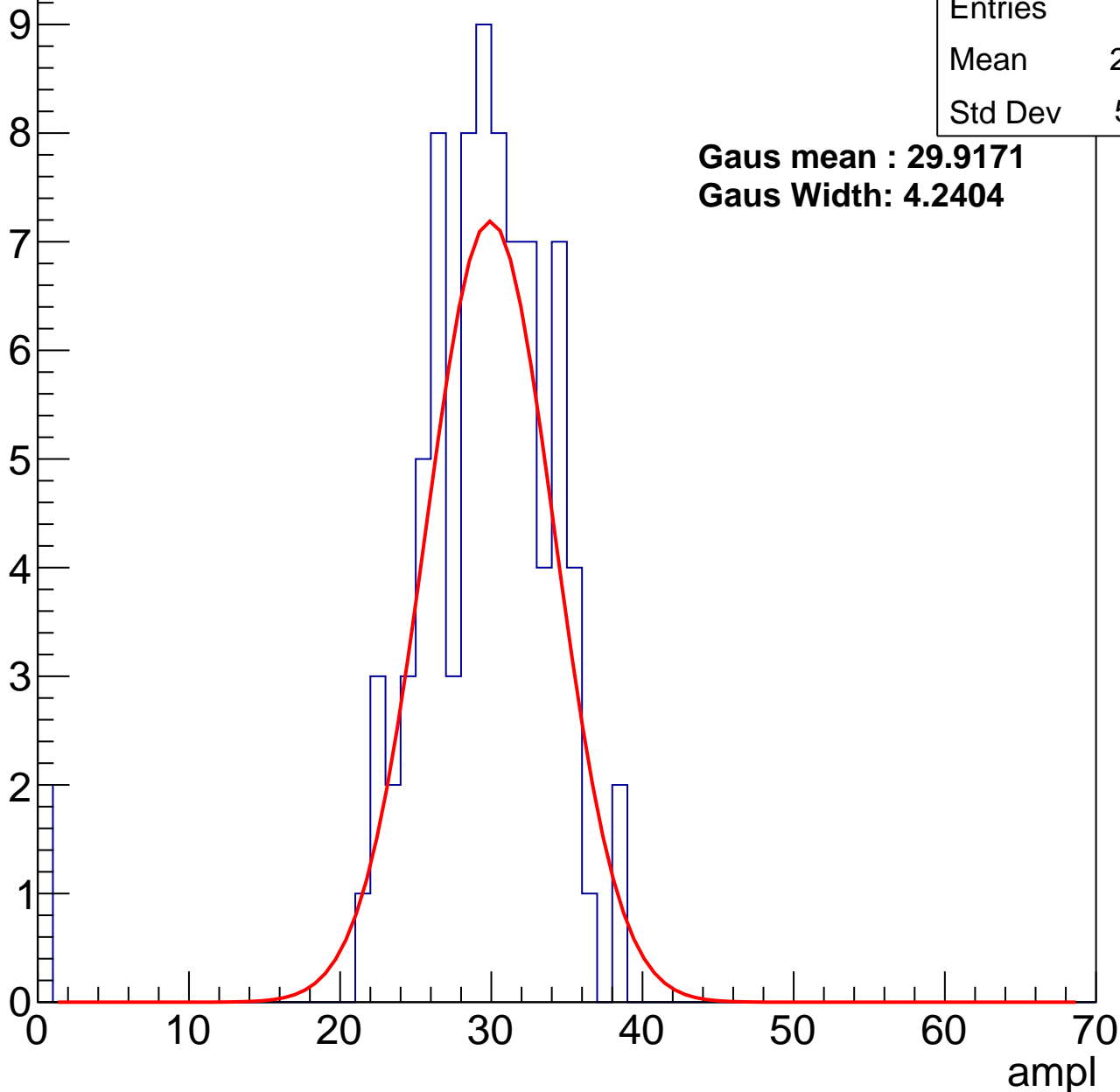
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	84
Mean	28.65
Std Dev	5.871

**Gaus mean : 29.9171**

**Gaus Width: 4.2404**



# B1L103S, U2-ch71, adc1

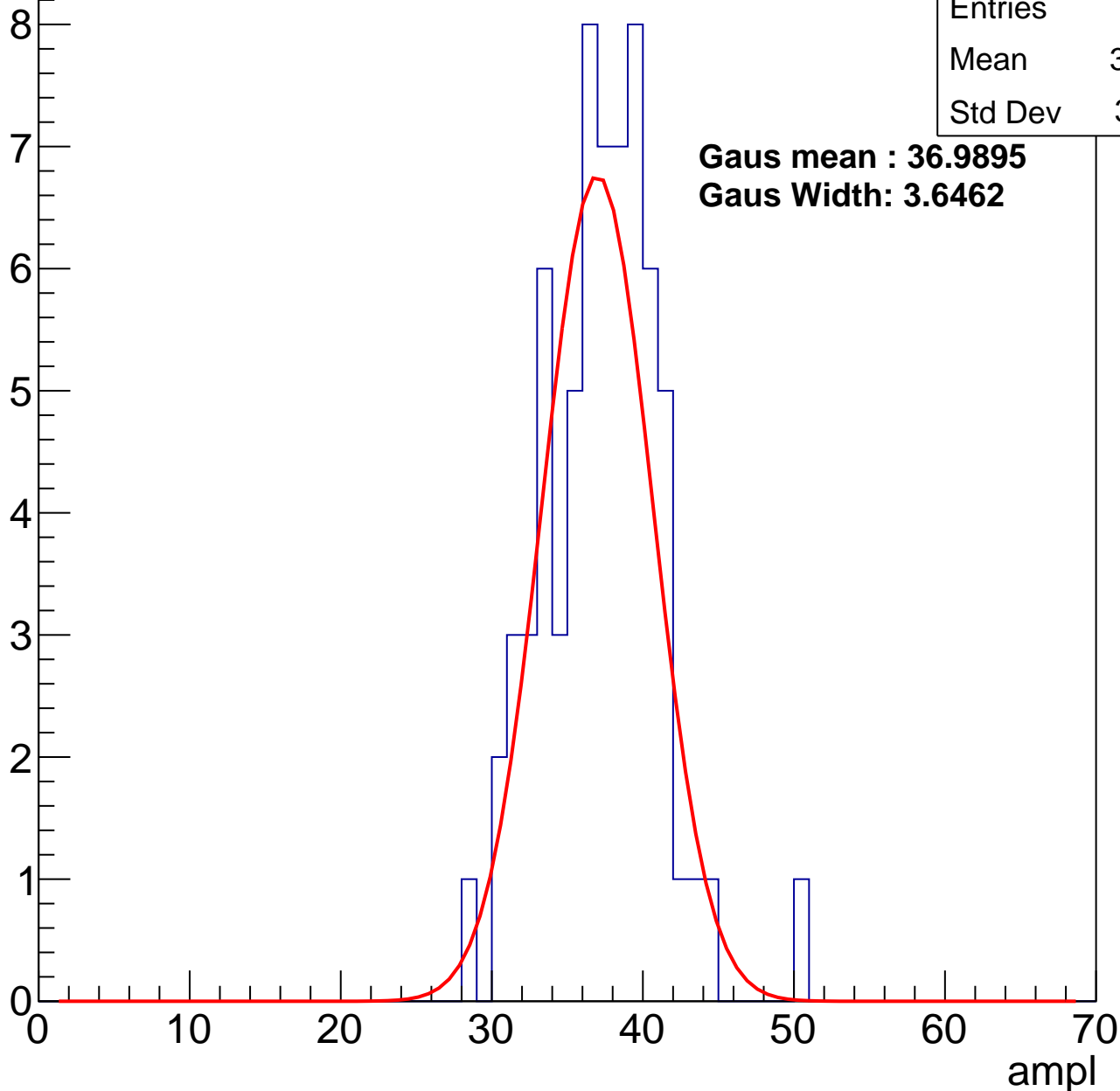
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	36.78
Std Dev	3.761

**Gaus mean : 36.9895**

**Gaus Width: 3.6462**



# B1L103S, U2-ch71, adc2

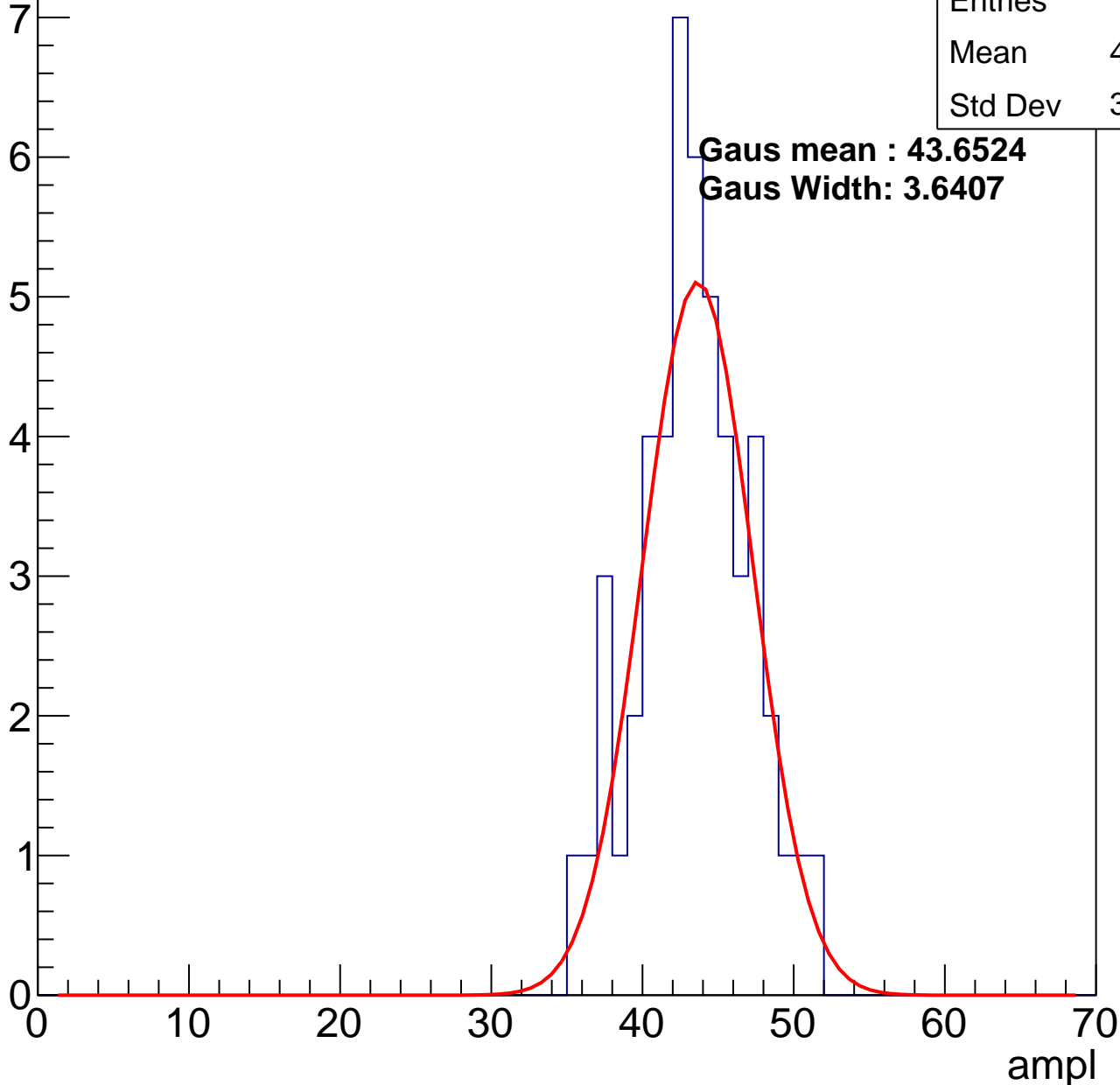
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	42.92
Std Dev	3.599

**Gaus mean : 43.6524**

**Gaus Width: 3.6407**

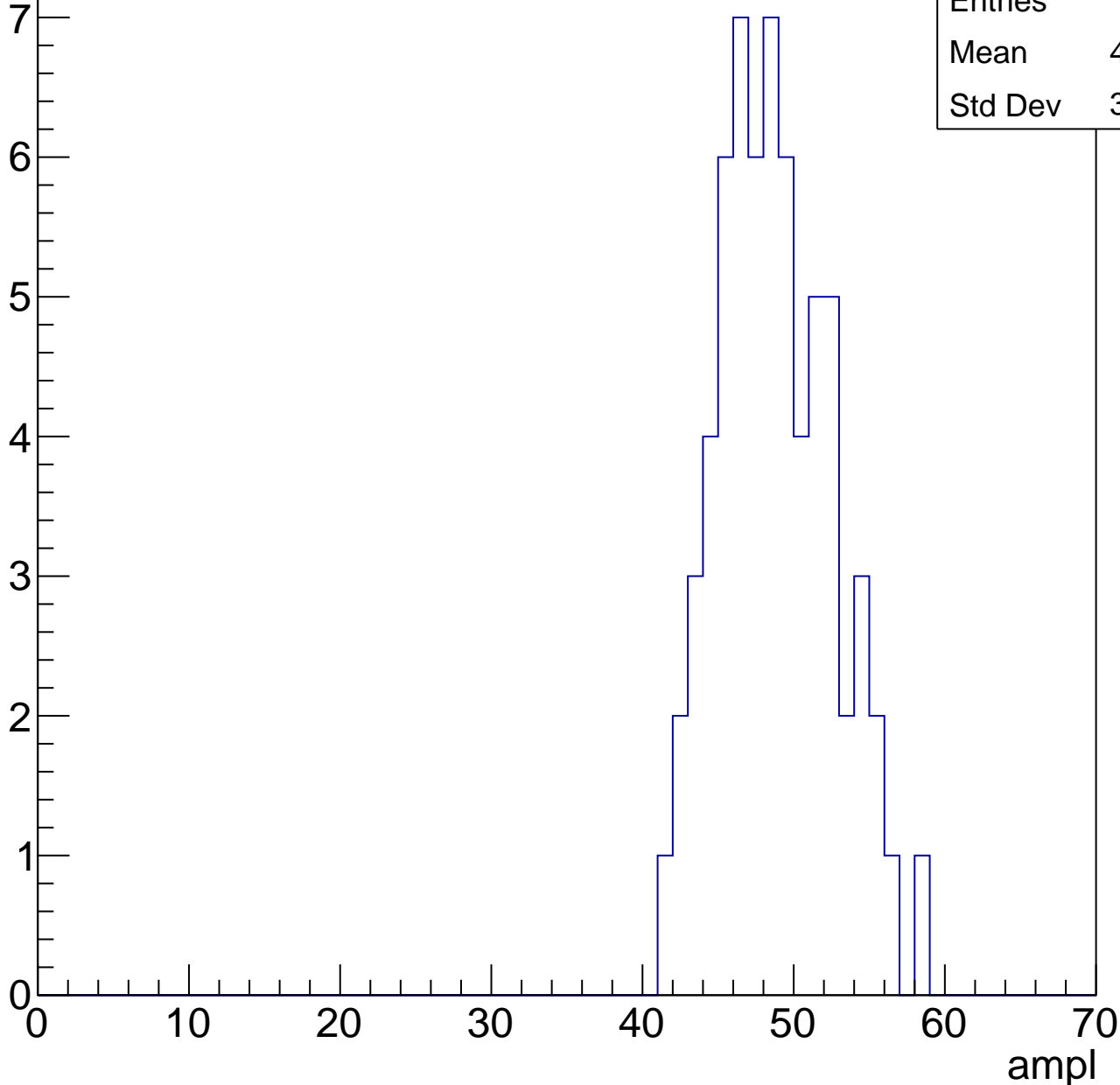


# B1L103S, U2-ch71, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

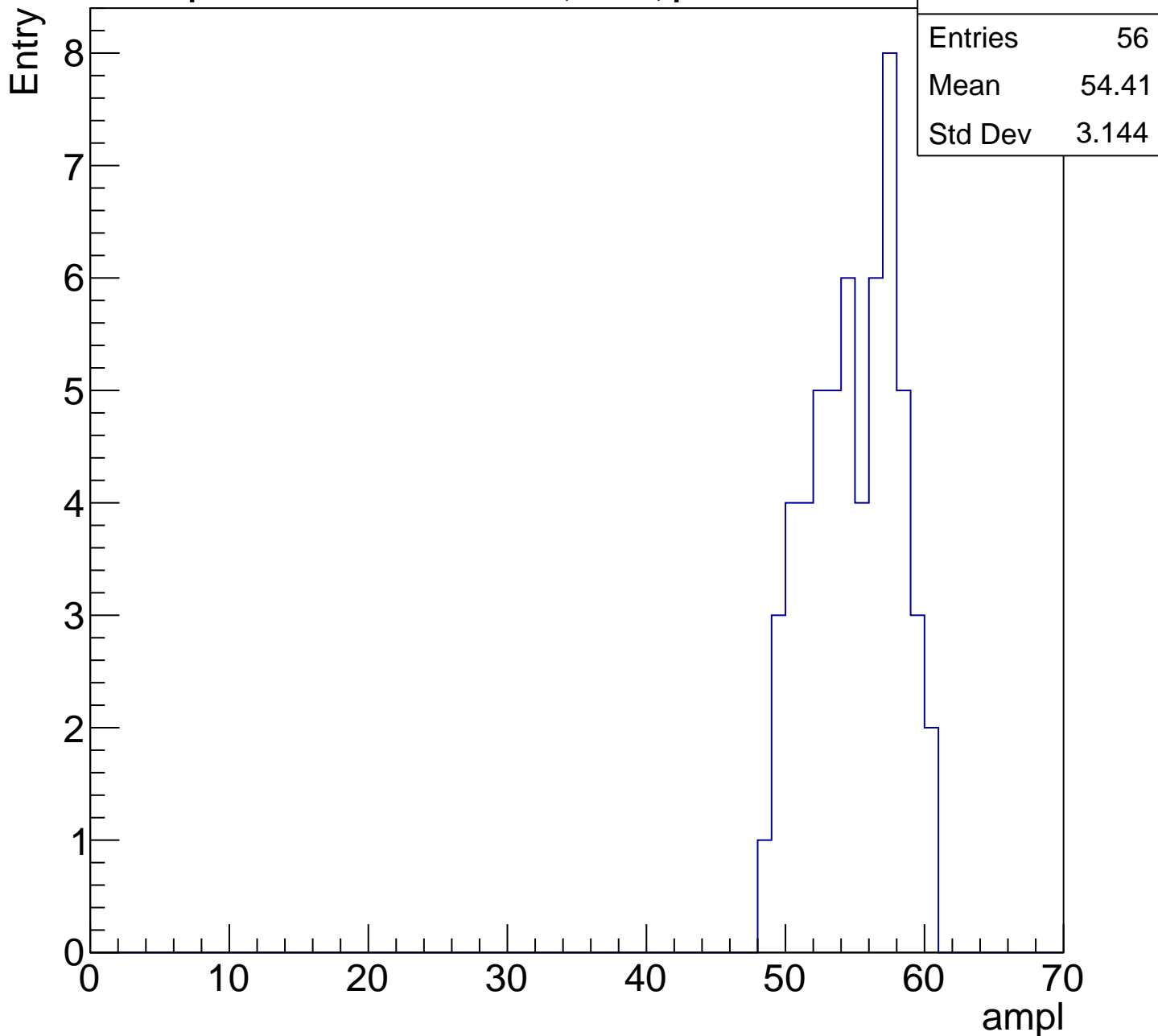
Entry

Entries	65
Mean	48.32
Std Dev	3.738



# B1L103S, U2-ch71, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

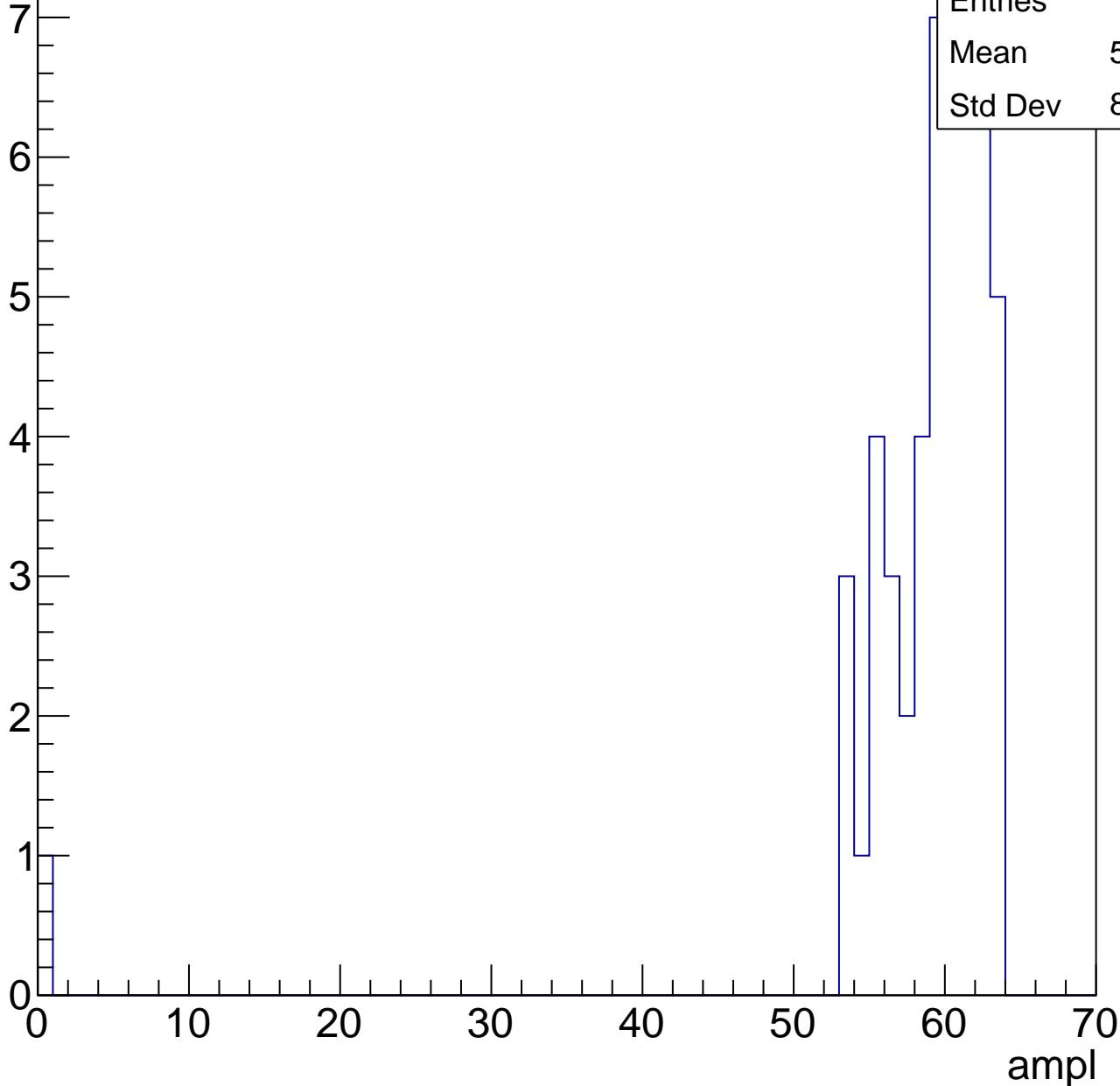


# B1L103S, U2-ch71, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	57.96
Std Dev	8.677

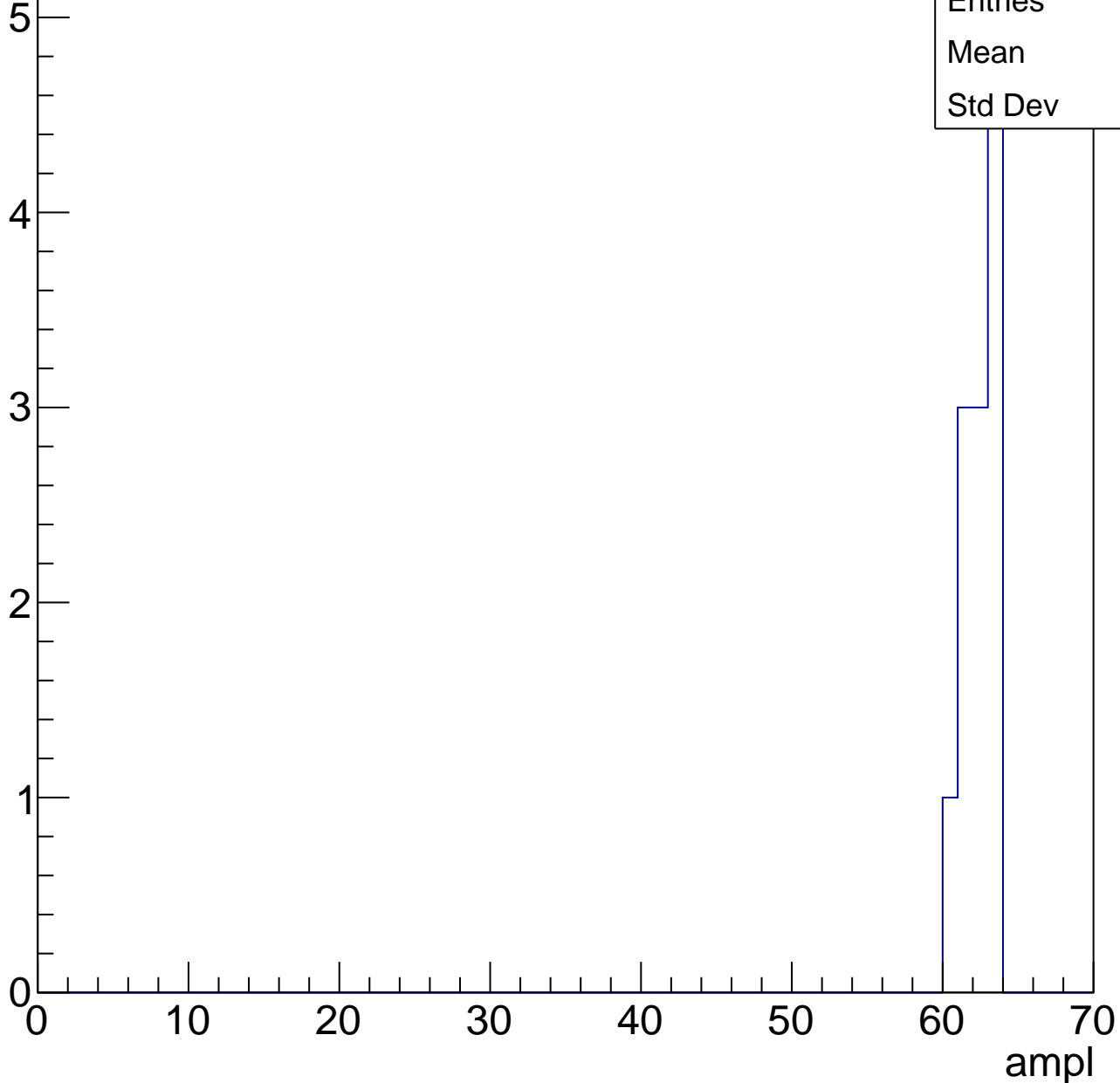


# B1L103S, U2-ch71, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	12
Mean	62
Std Dev	1





# B1L103S, U2-ch71, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L103S, U2-ch72, adc0

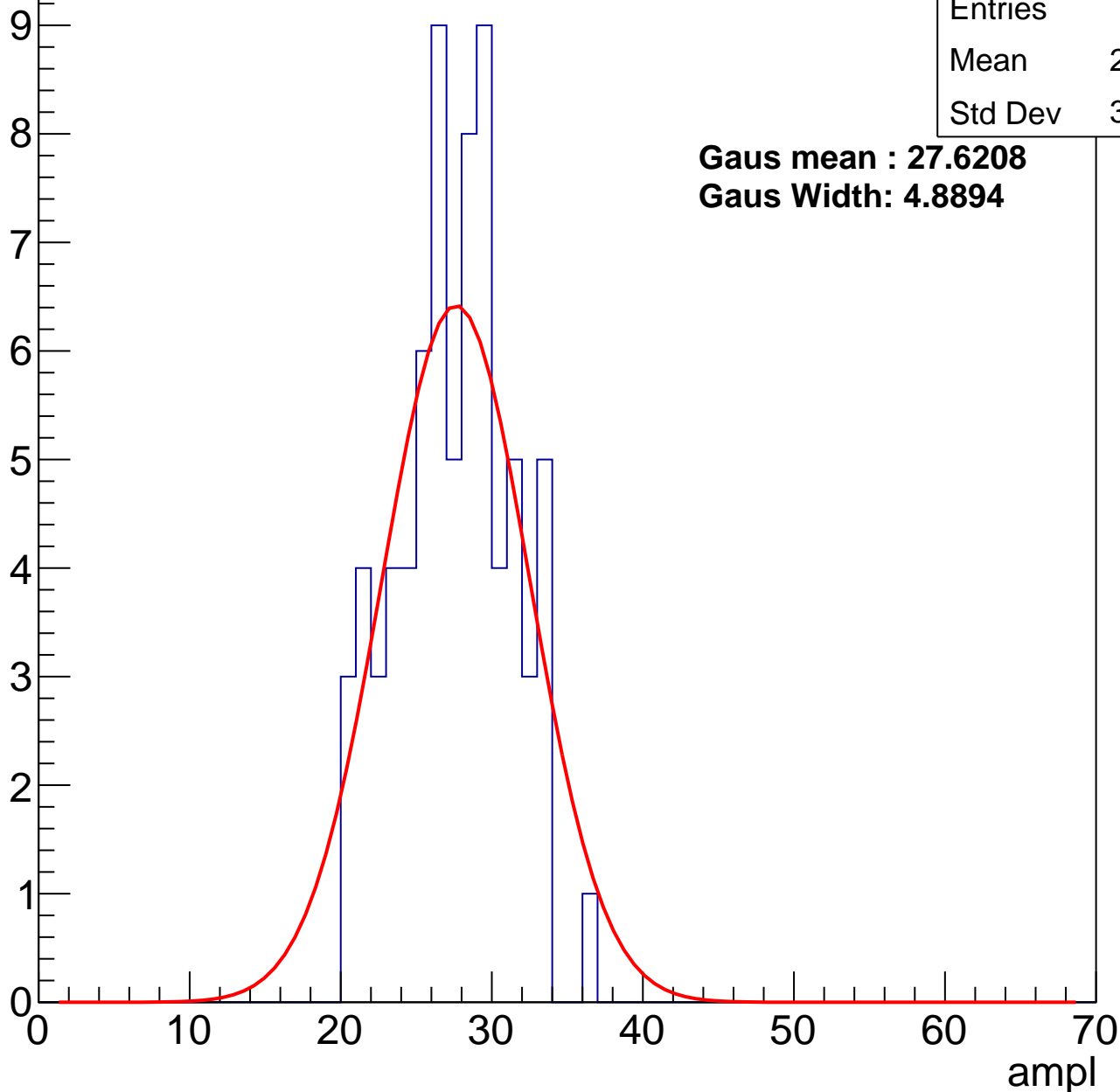
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	27.04
Std Dev	3.692

**Gaus mean : 27.6208**

**Gaus Width: 4.8894**



# B1L103S, U2-ch72, adc1

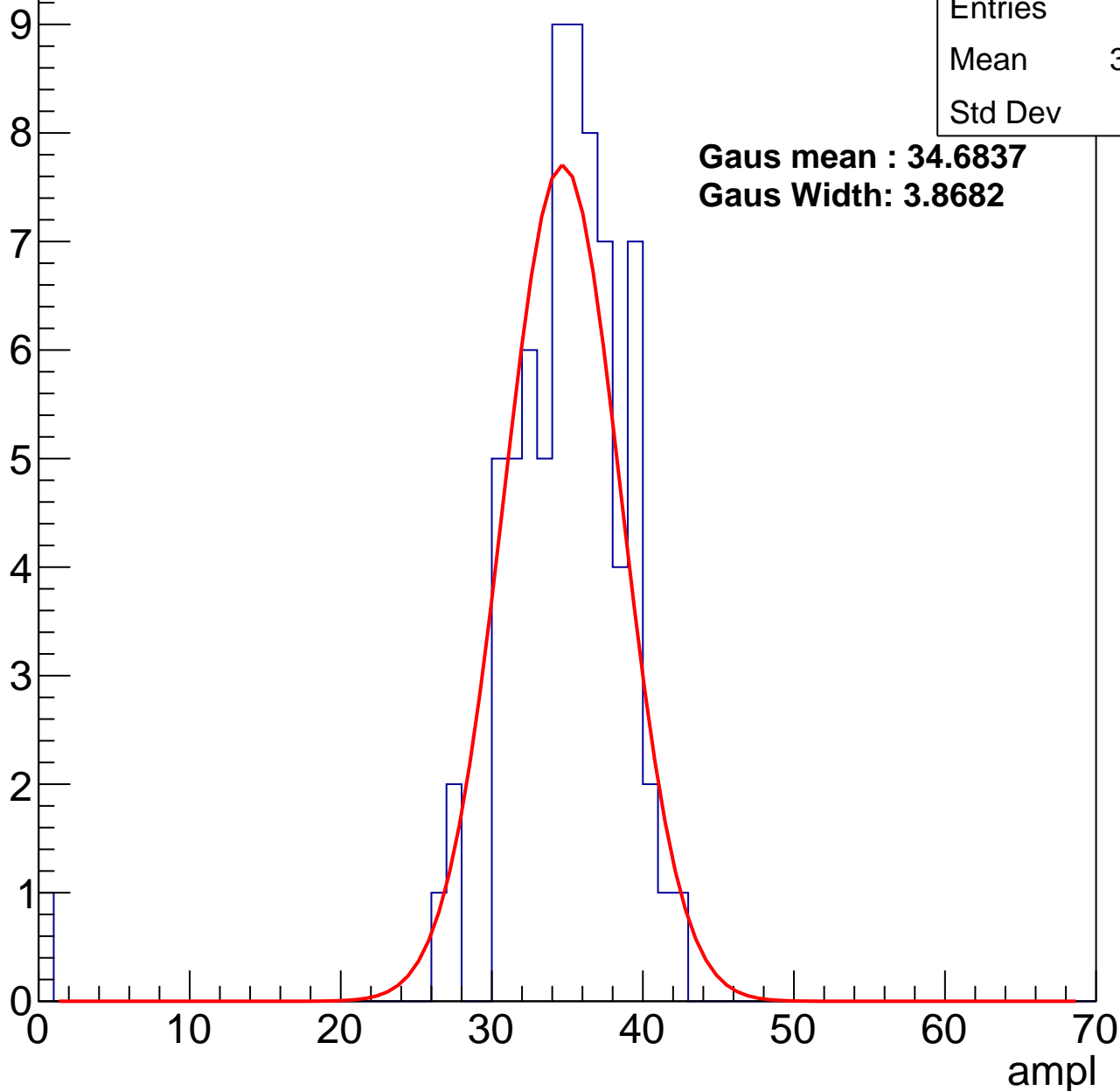
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	34.22
Std Dev	5.23

**Gaus mean : 34.6837**

**Gaus Width: 3.8682**



# B1L103S, U2-ch72, adc2

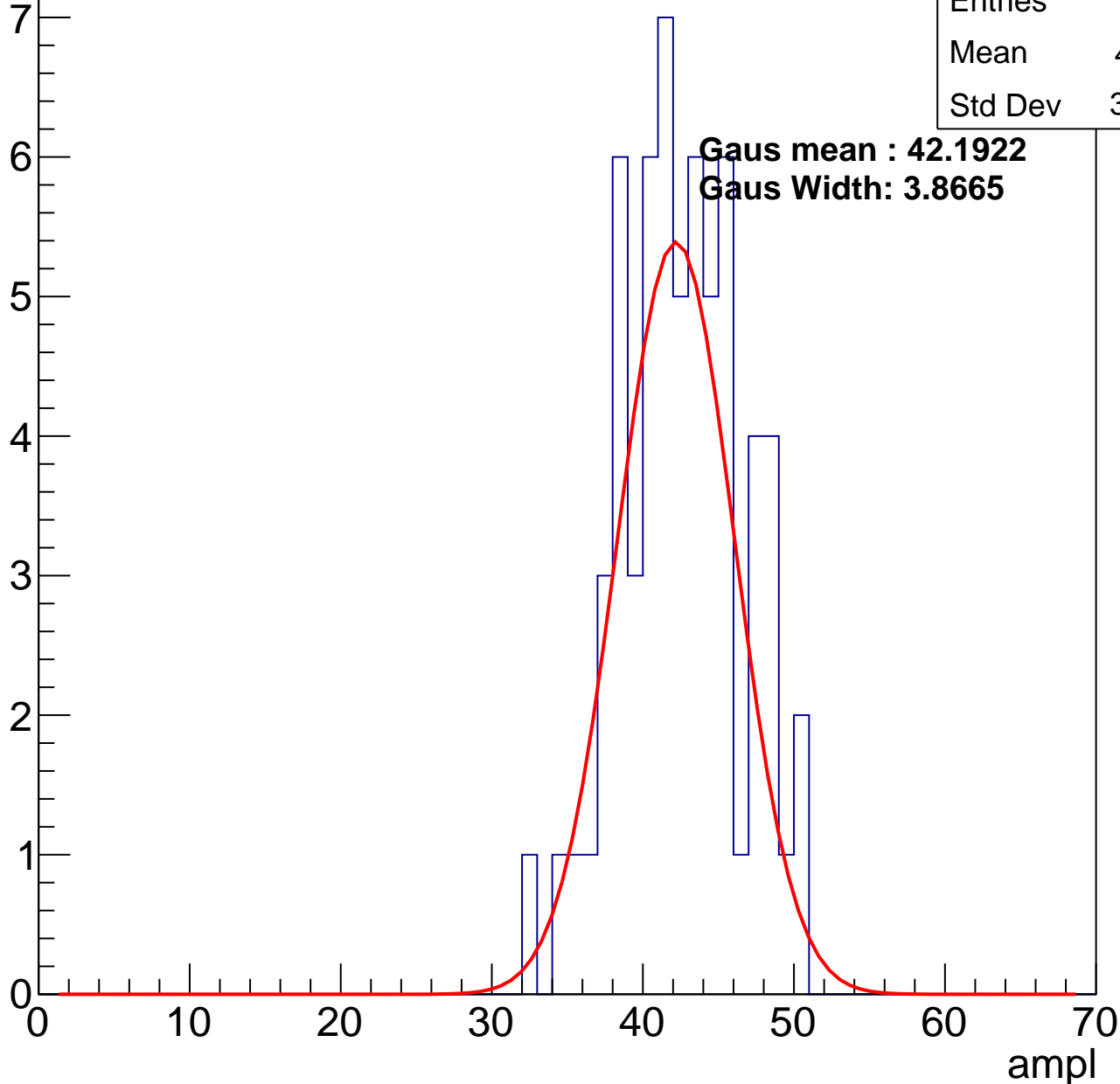
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	42.11
Std Dev	3.973

**Gaus mean : 42.1922**

**Gaus Width: 3.8665**



# B1L103S, U2-ch72, adc3

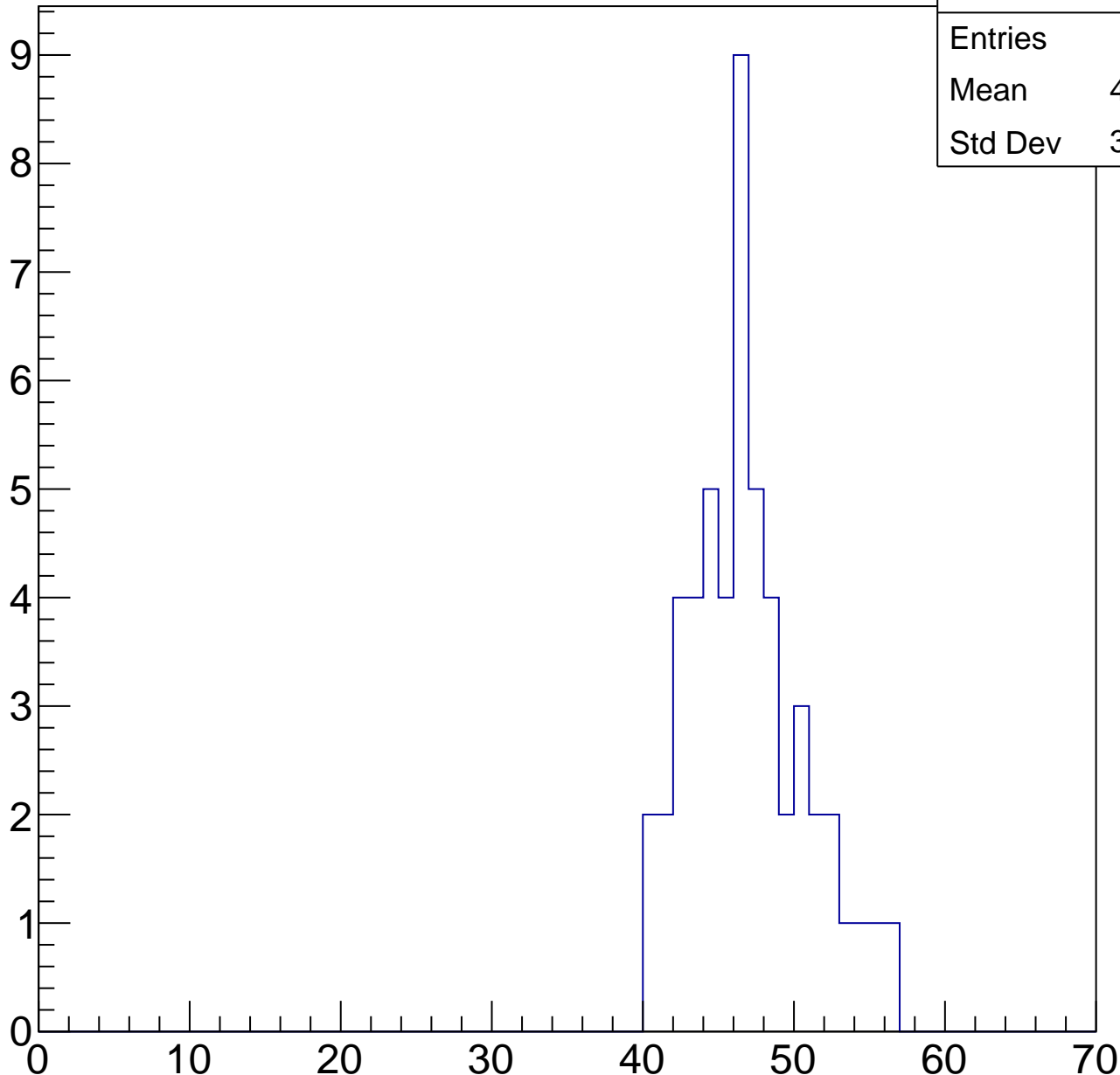
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	52
Mean	46.44
Std Dev	3.769

ampl

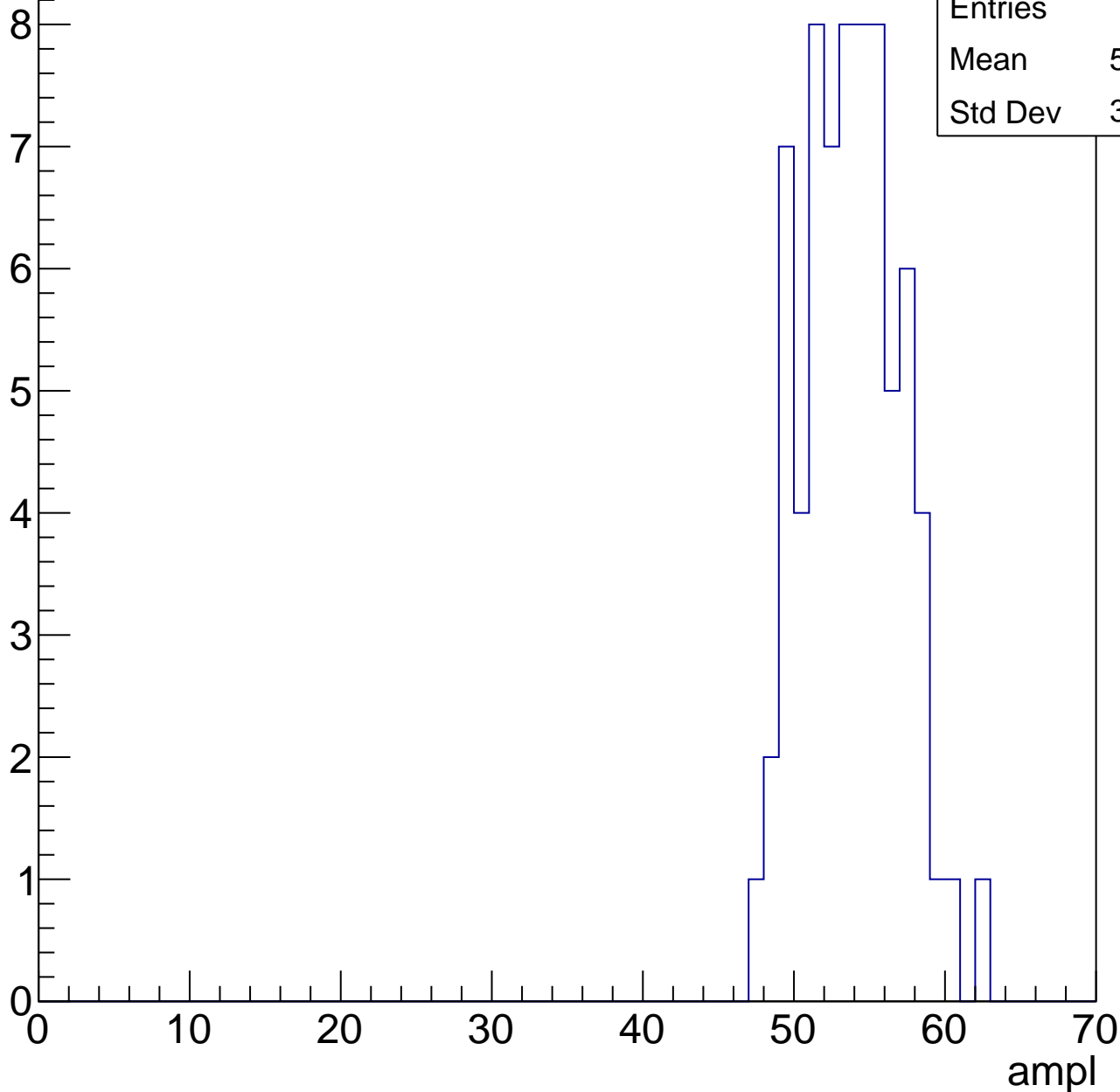


# B1L103S, U2-ch72, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	53.37
Std Dev	3.163



# B1L103S, U2-ch72, adc5

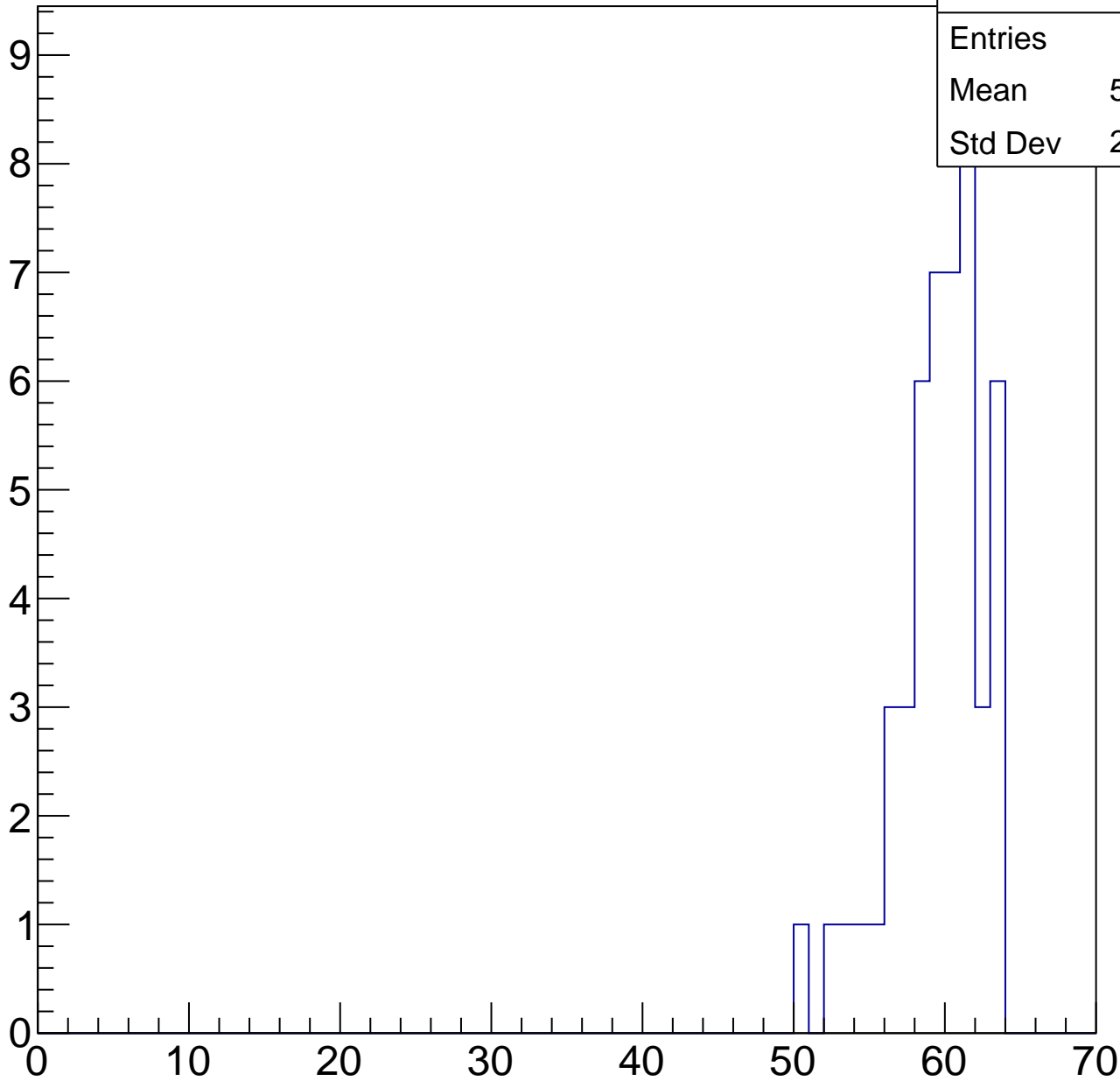
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	49
Mean	59.12
Std Dev	2.918

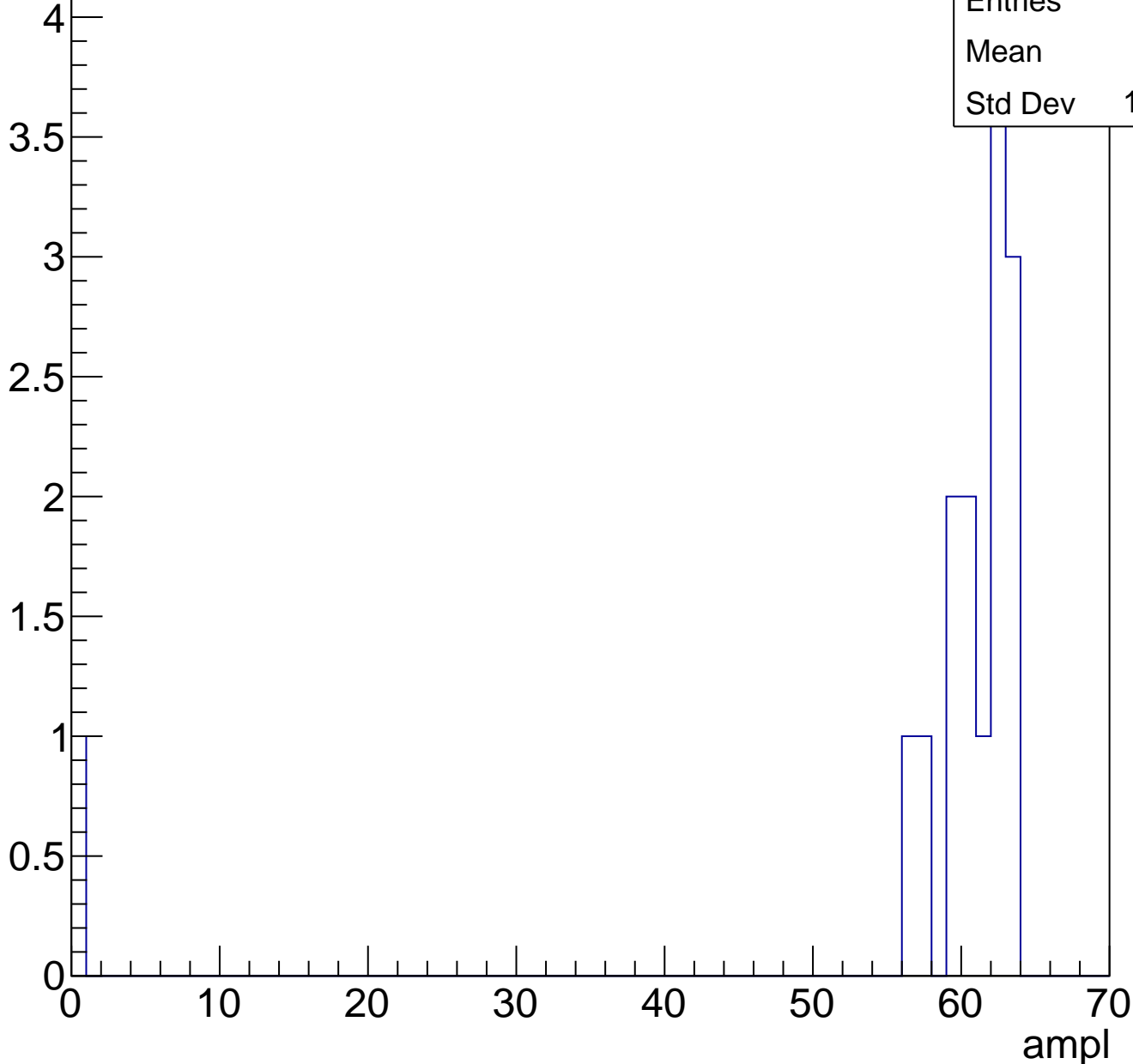
ampl



# B1L103S, U2-ch72, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

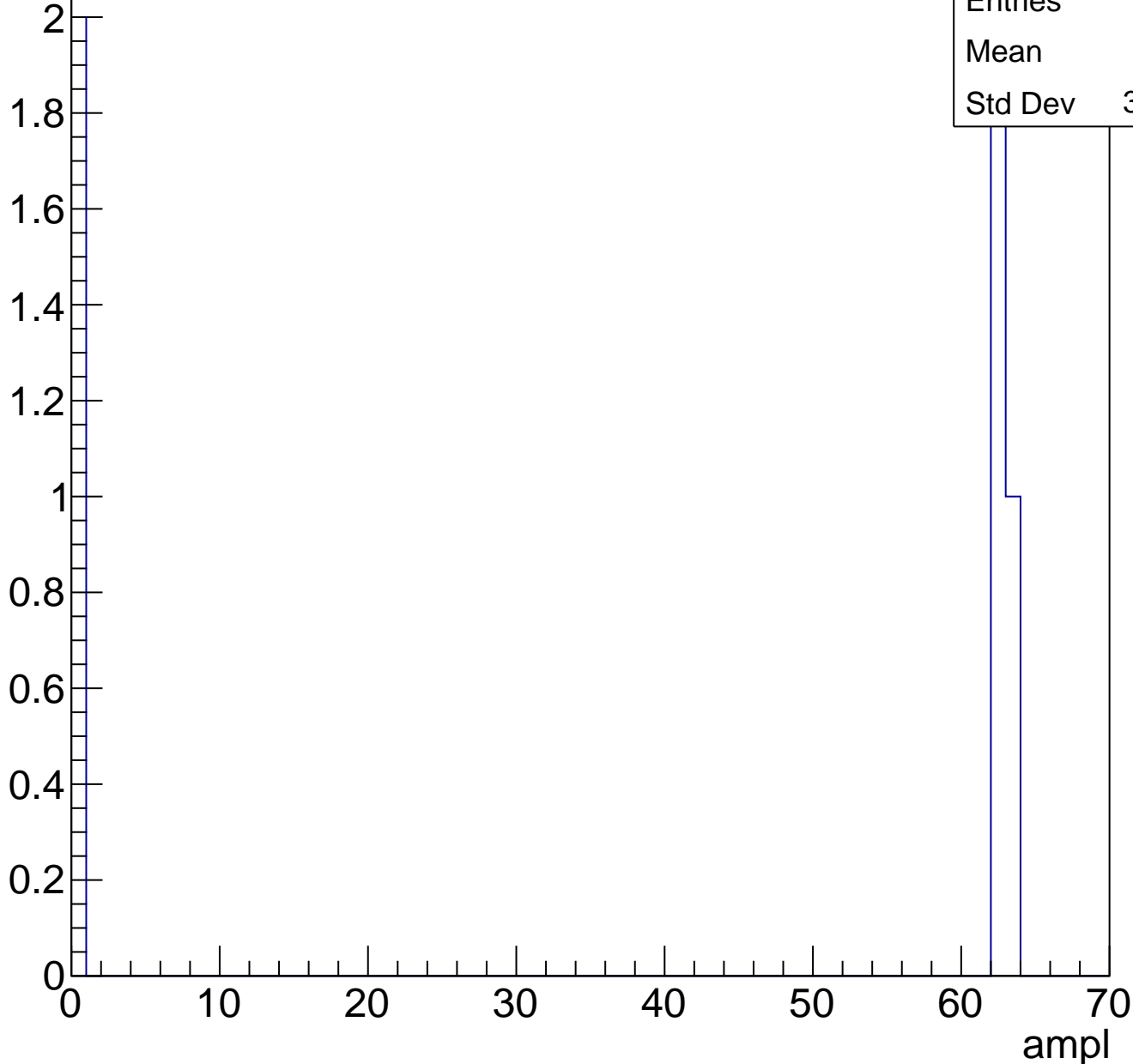




# B1L103S, U2-ch72, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch73, adc0

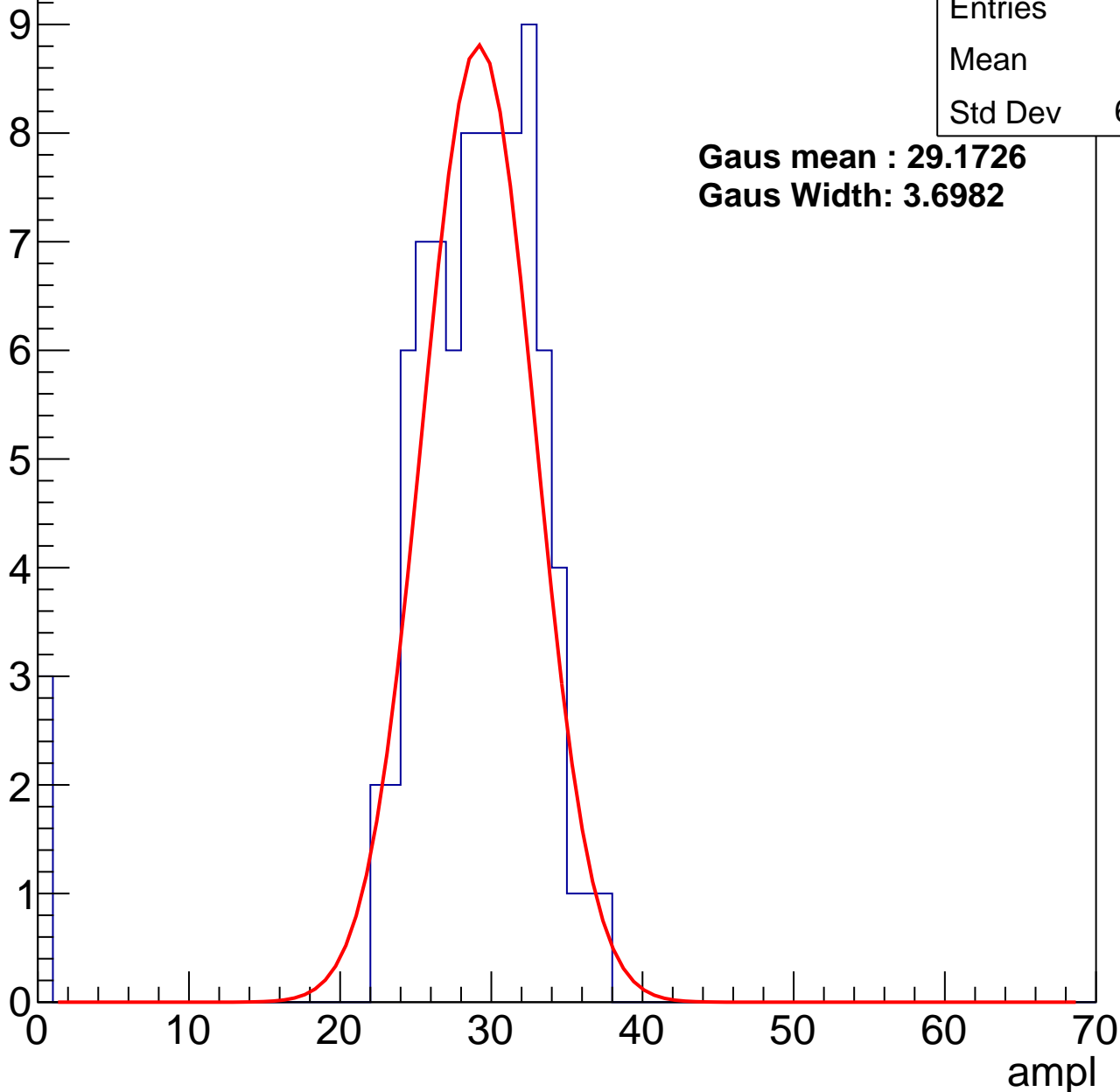
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	87
Mean	27.9
Std Dev	6.261

**Gaus mean : 29.1726**

**Gaus Width: 3.6982**



# B1L103S, U2-ch73, adc1

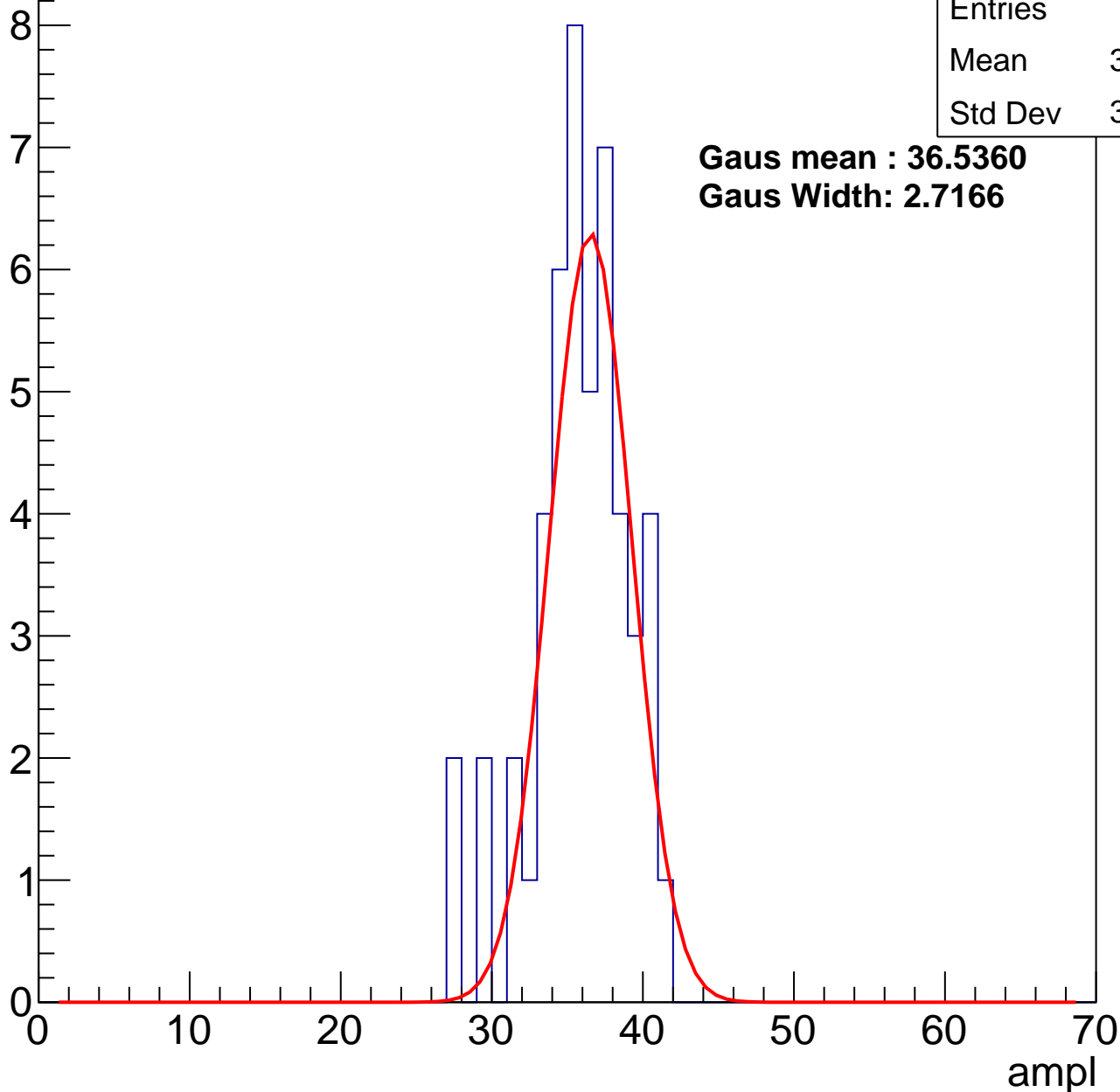
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	35.33
Std Dev	3.229

**Gaus mean : 36.5360**

**Gaus Width: 2.7166**



# B1L103S, U2-ch73, adc2

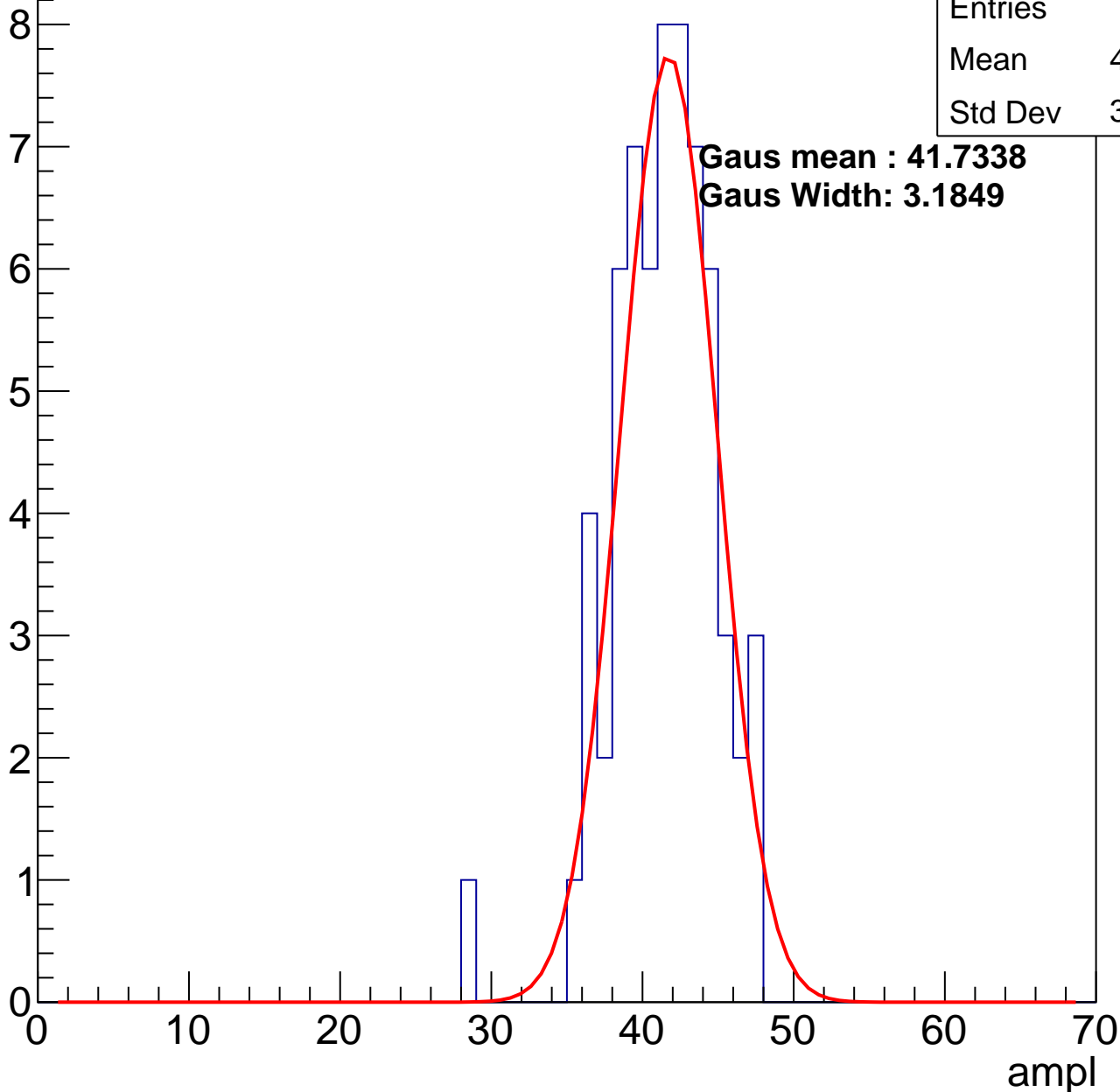
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	40.92
Std Dev	3.356

**Gaus mean : 41.7338**

**Gaus Width: 3.1849**

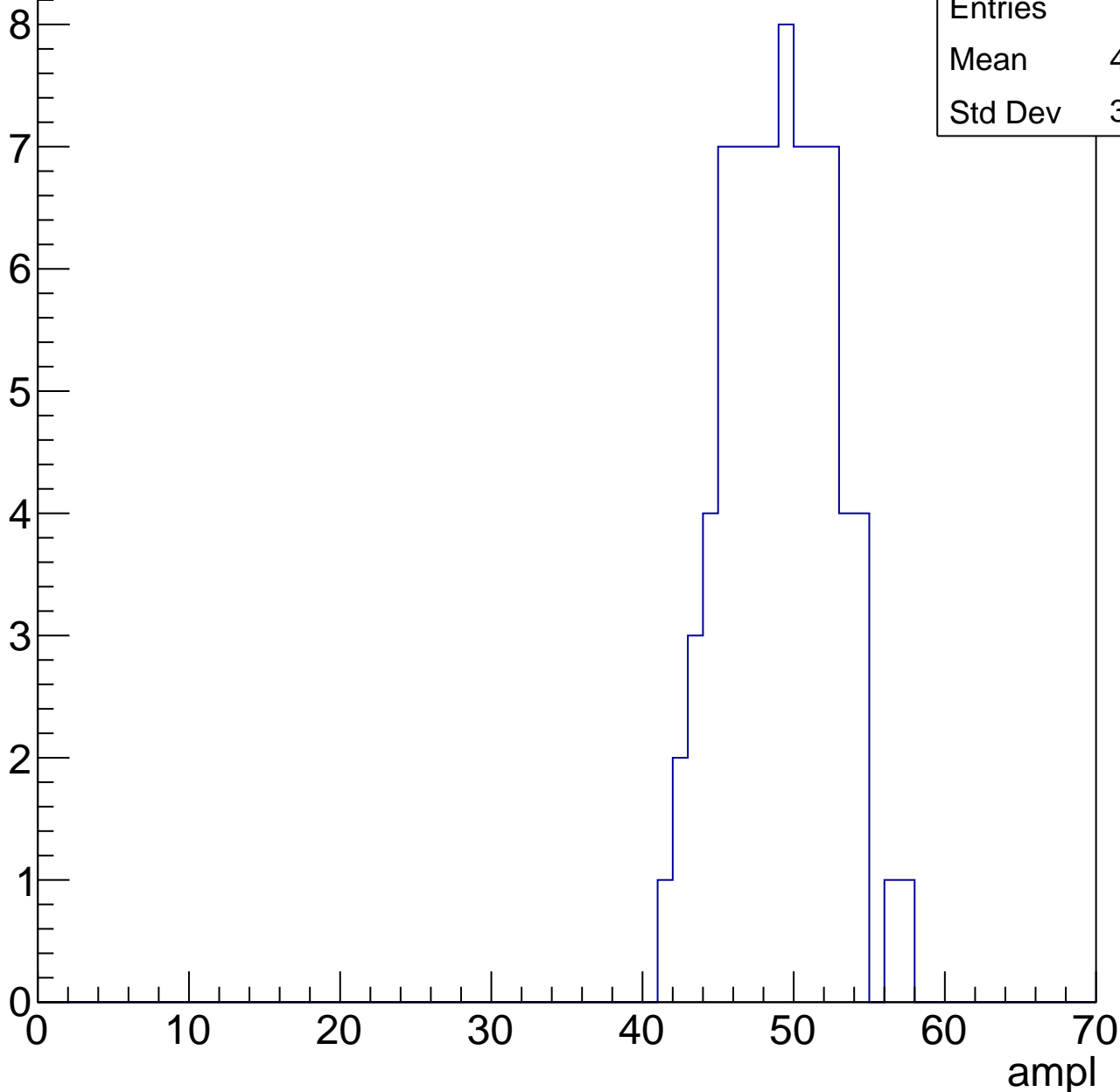


# B1L103S, U2-ch73, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	48.52
Std Dev	3.489

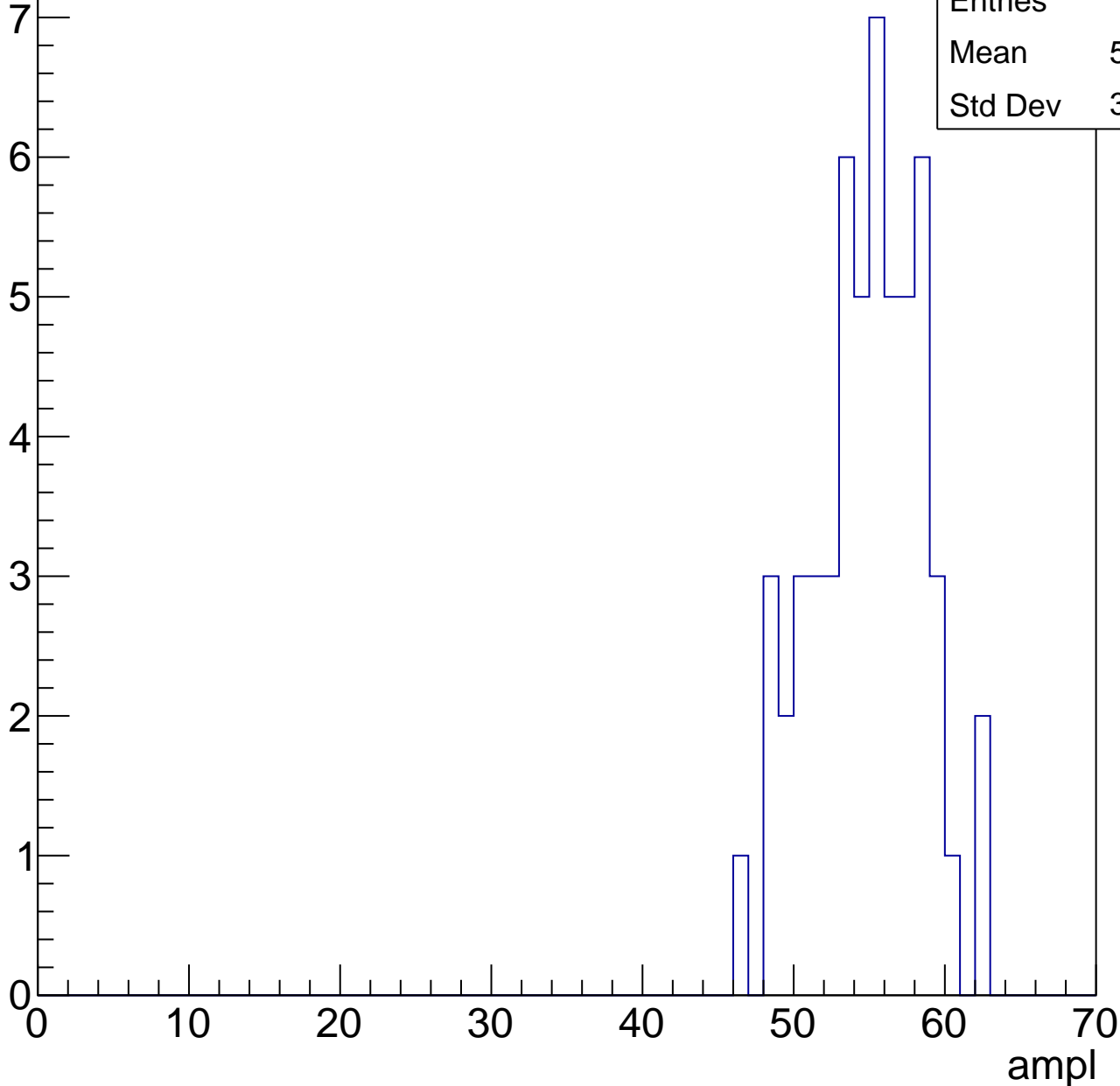


# B1L103S, U2-ch73, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

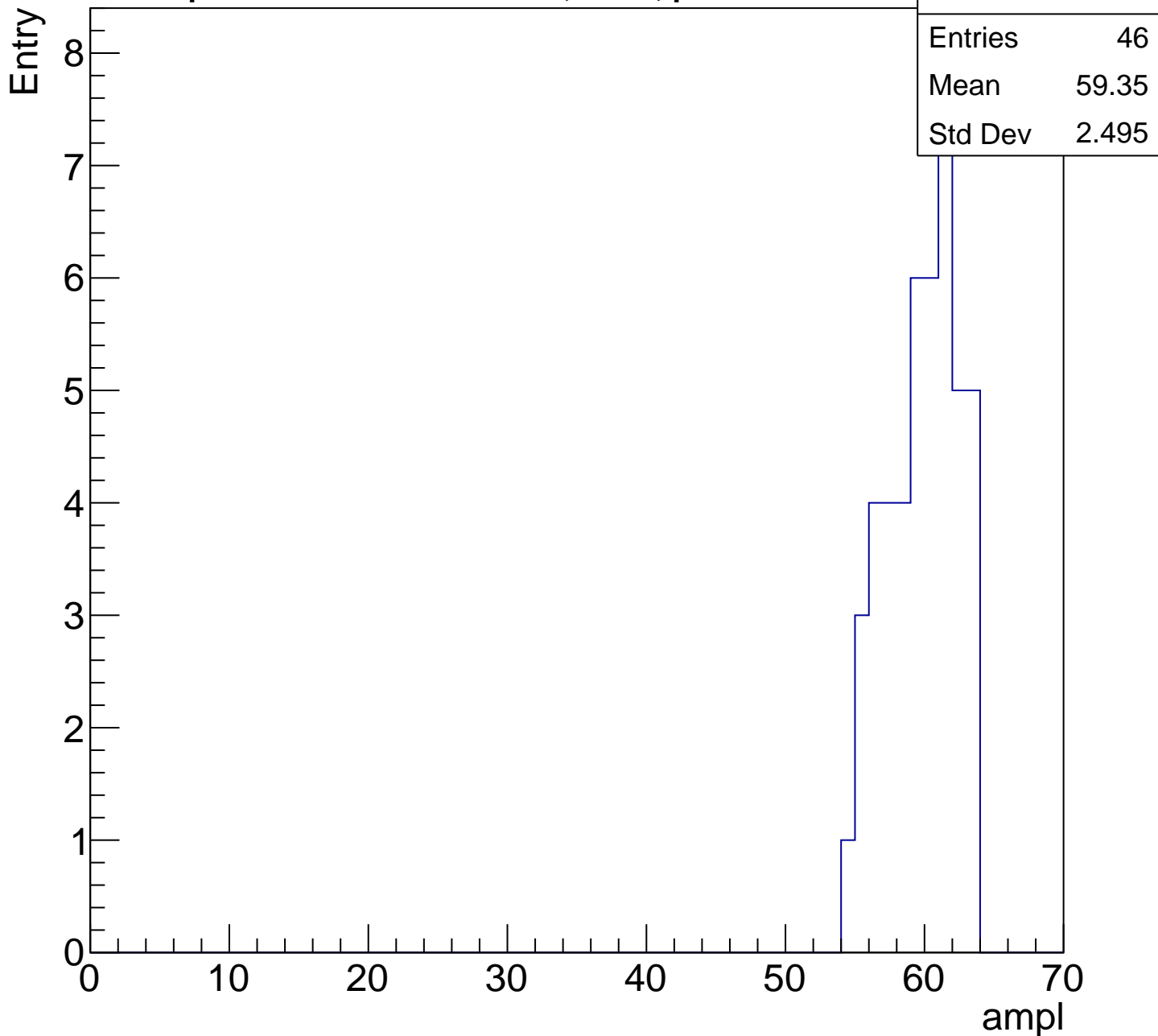
Entry

Entries	55
Mean	54.44
Std Dev	3.597



# B1L103S, U2-ch73, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

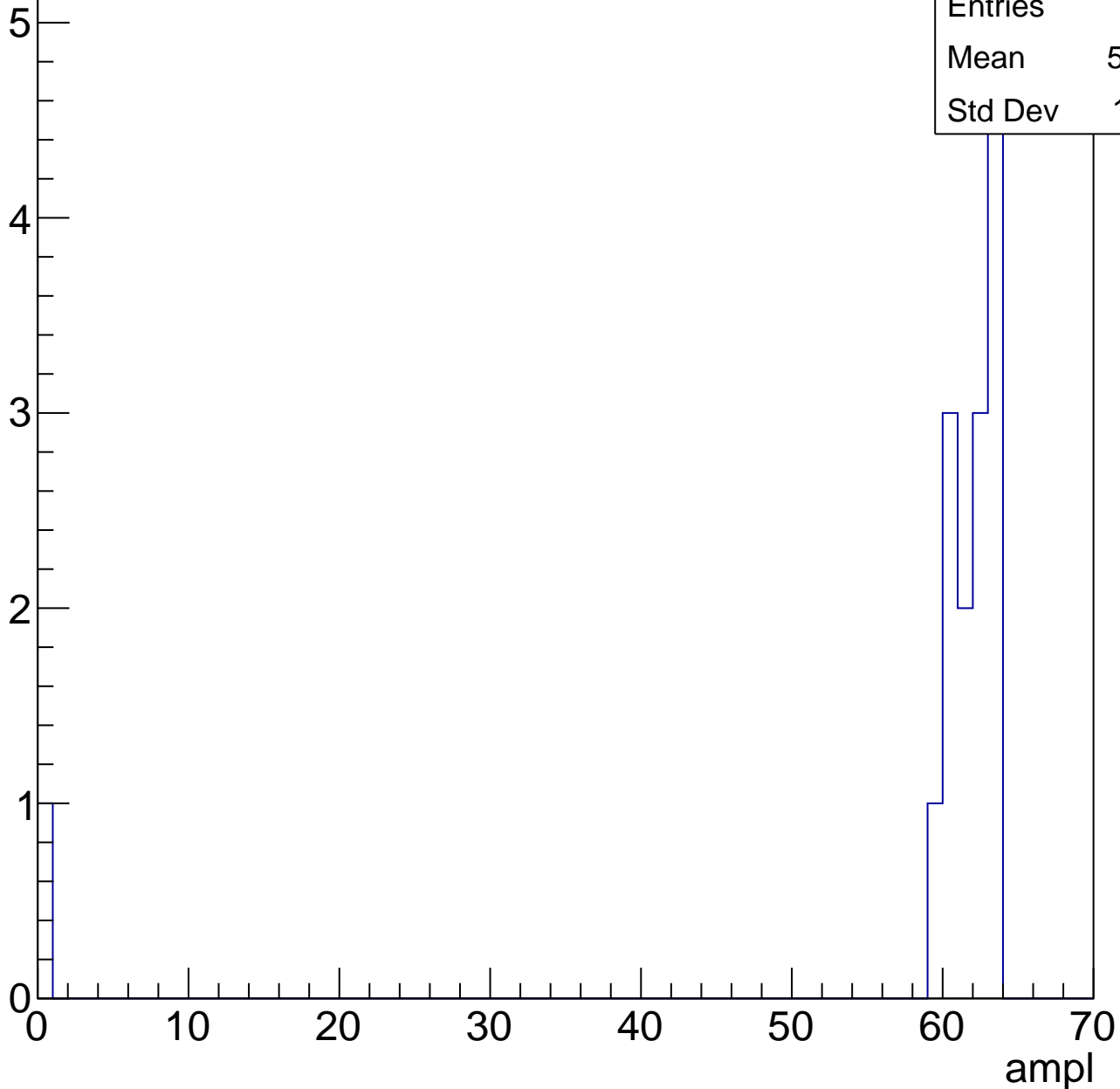


# B1L103S, U2-ch73, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	15
Mean	57.47
Std Dev	15.41





# B1L103S, U2-ch73, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U2-ch74, adc0

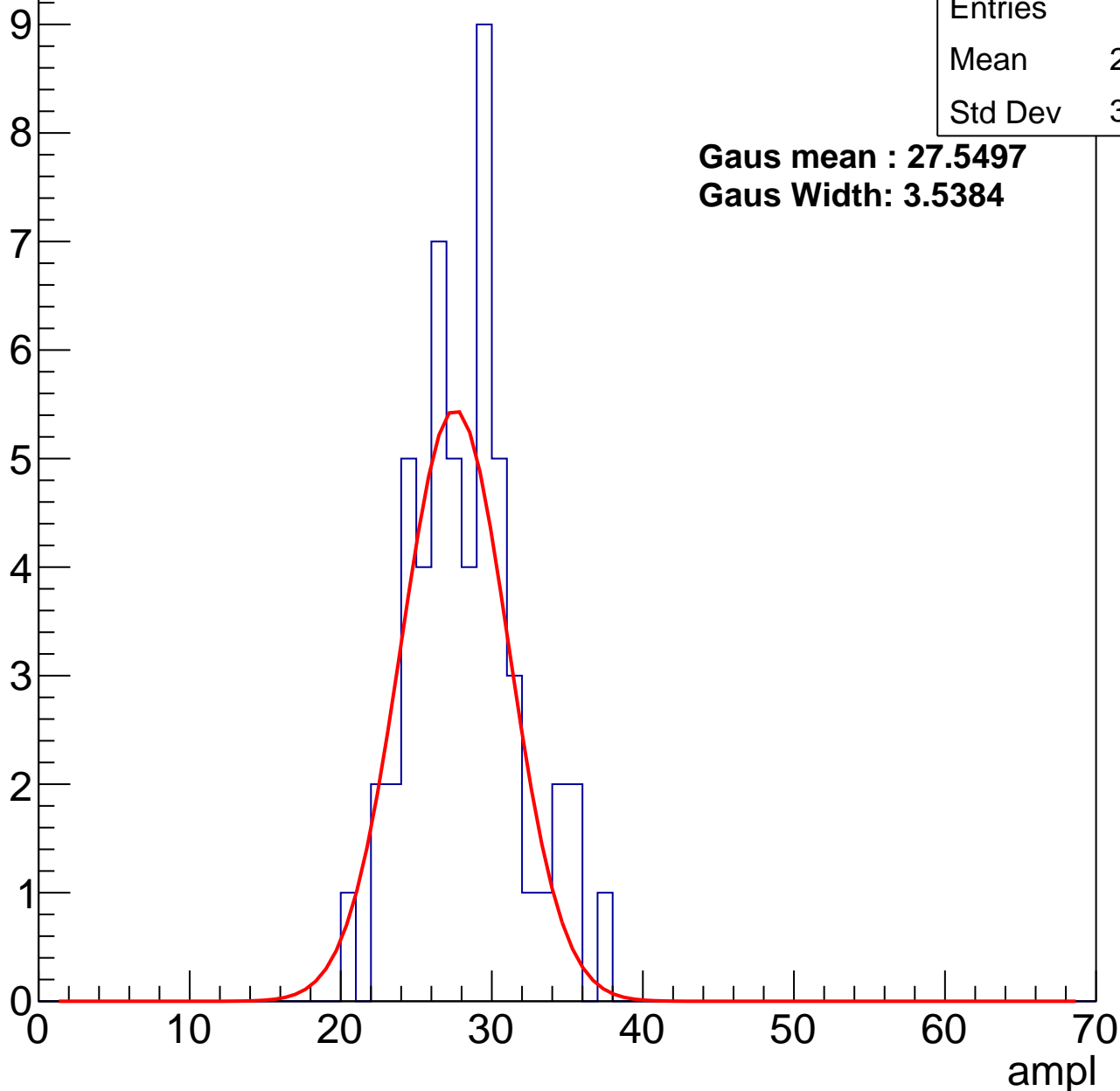
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	27.83
Std Dev	3.553

**Gaus mean : 27.5497**

**Gaus Width: 3.5384**



# B1L103S, U2-ch74, adc1

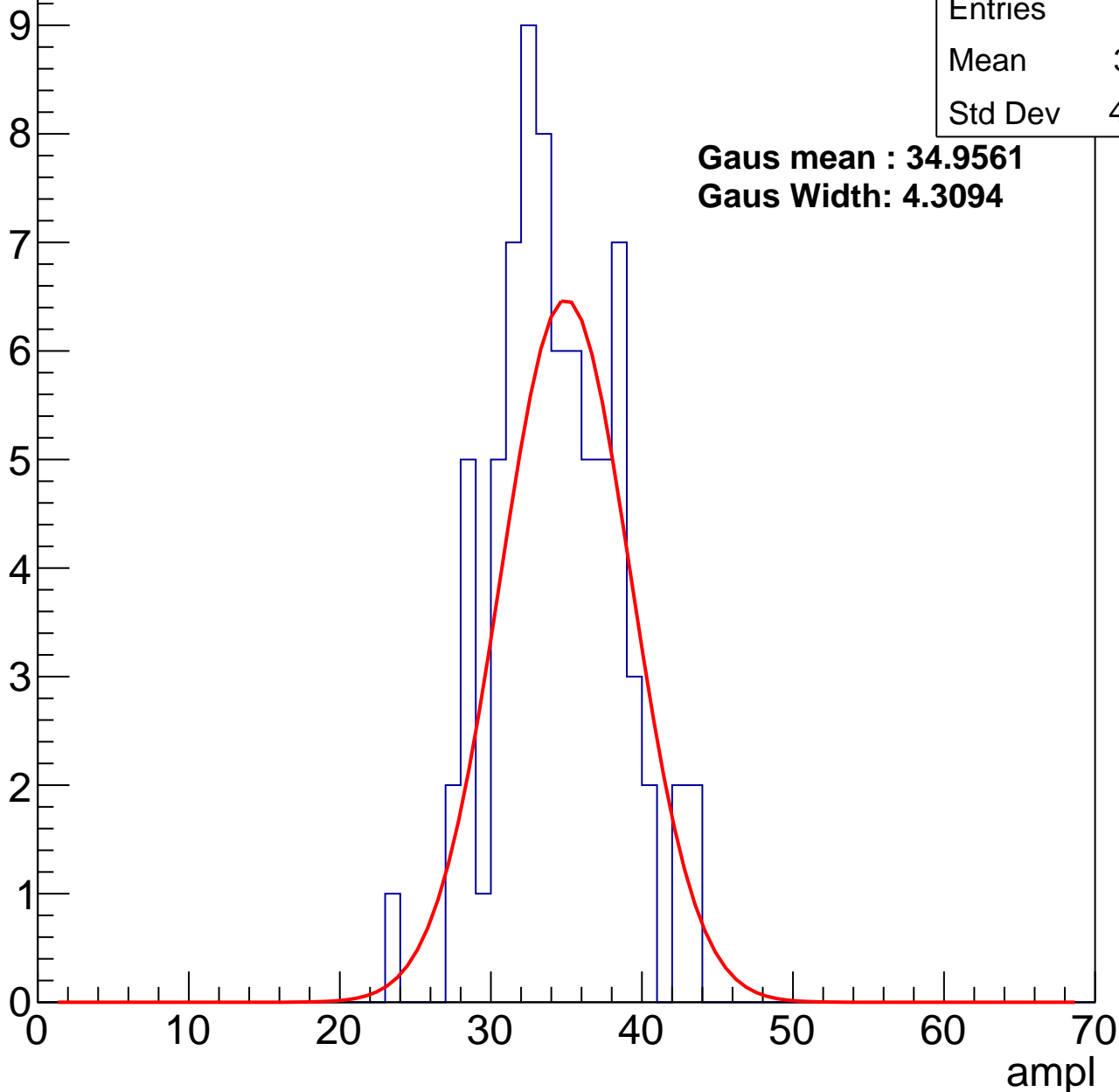
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	33.91
Std Dev	4.024

**Gaus mean : 34.9561**

**Gaus Width: 4.3094**



# B1L103S, U2-ch74, adc2

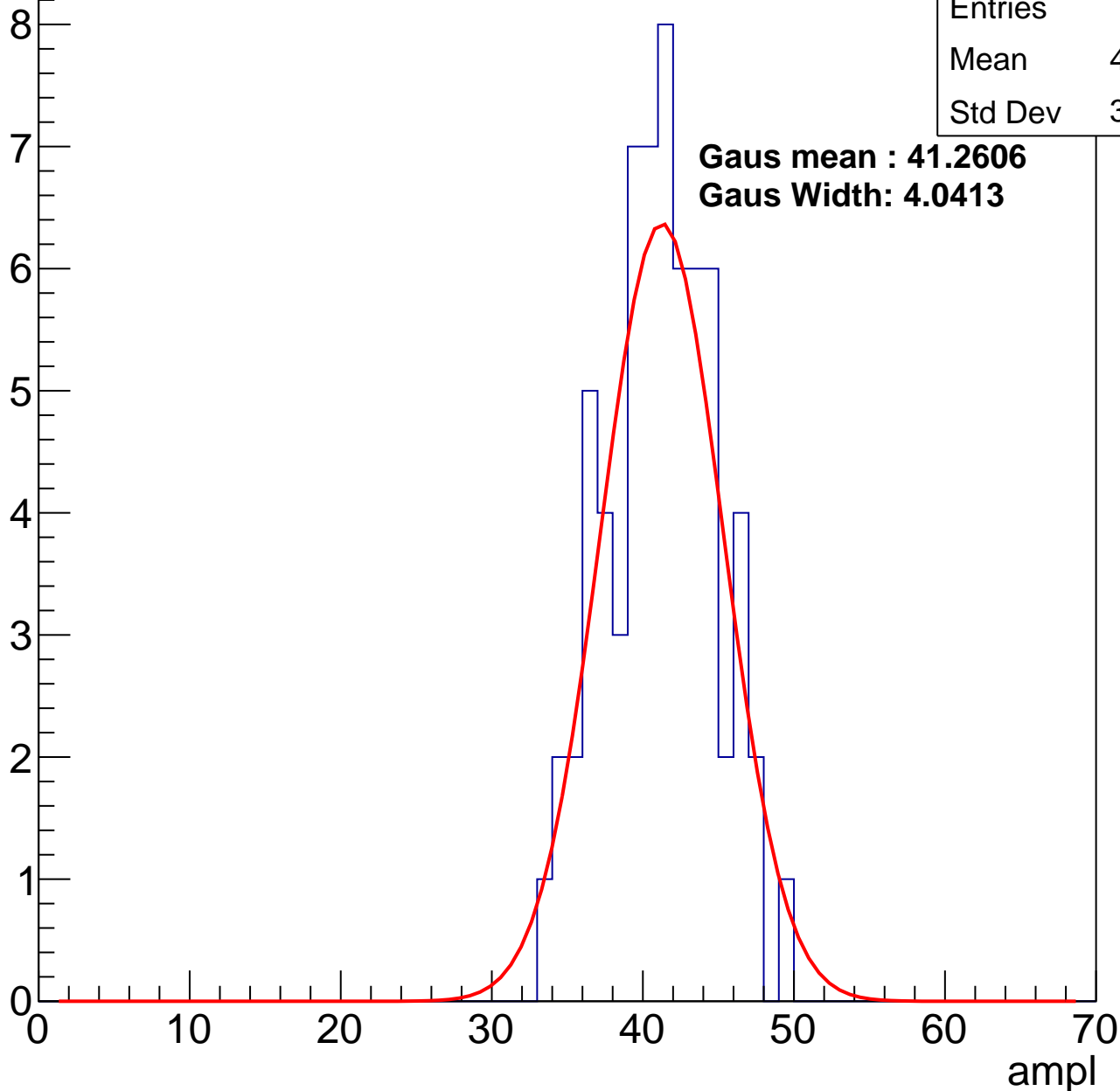
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	40.68
Std Dev	3.547

**Gaus mean : 41.2606**

**Gaus Width: 4.0413**

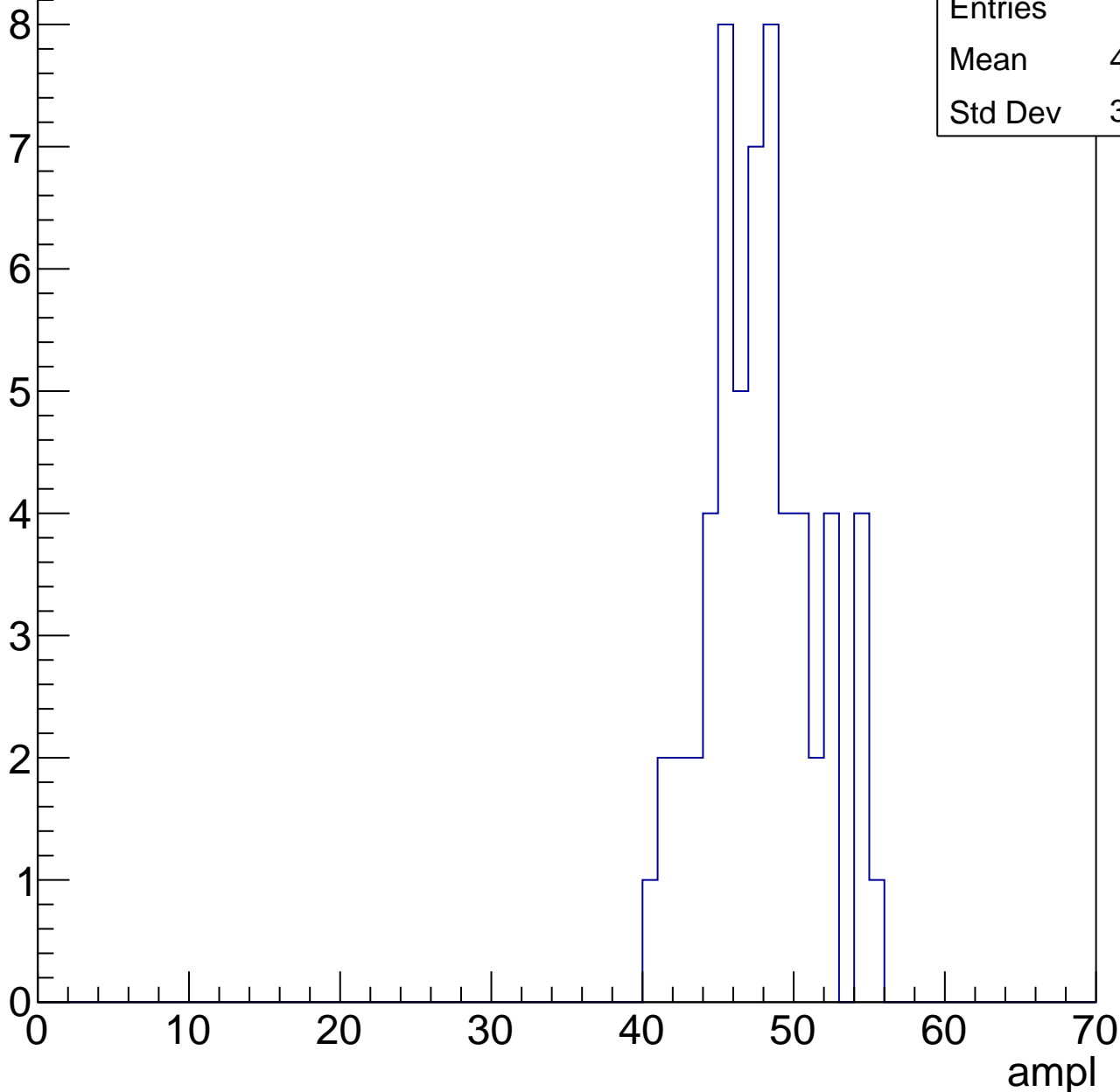


# B1L103S, U2-ch74, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	47.38
Std Dev	3.522



# B1L103S, U2-ch74, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	55
Mean	52.49
Std Dev	2.904

Entry

10

8

6

4

2

0

0

10

20

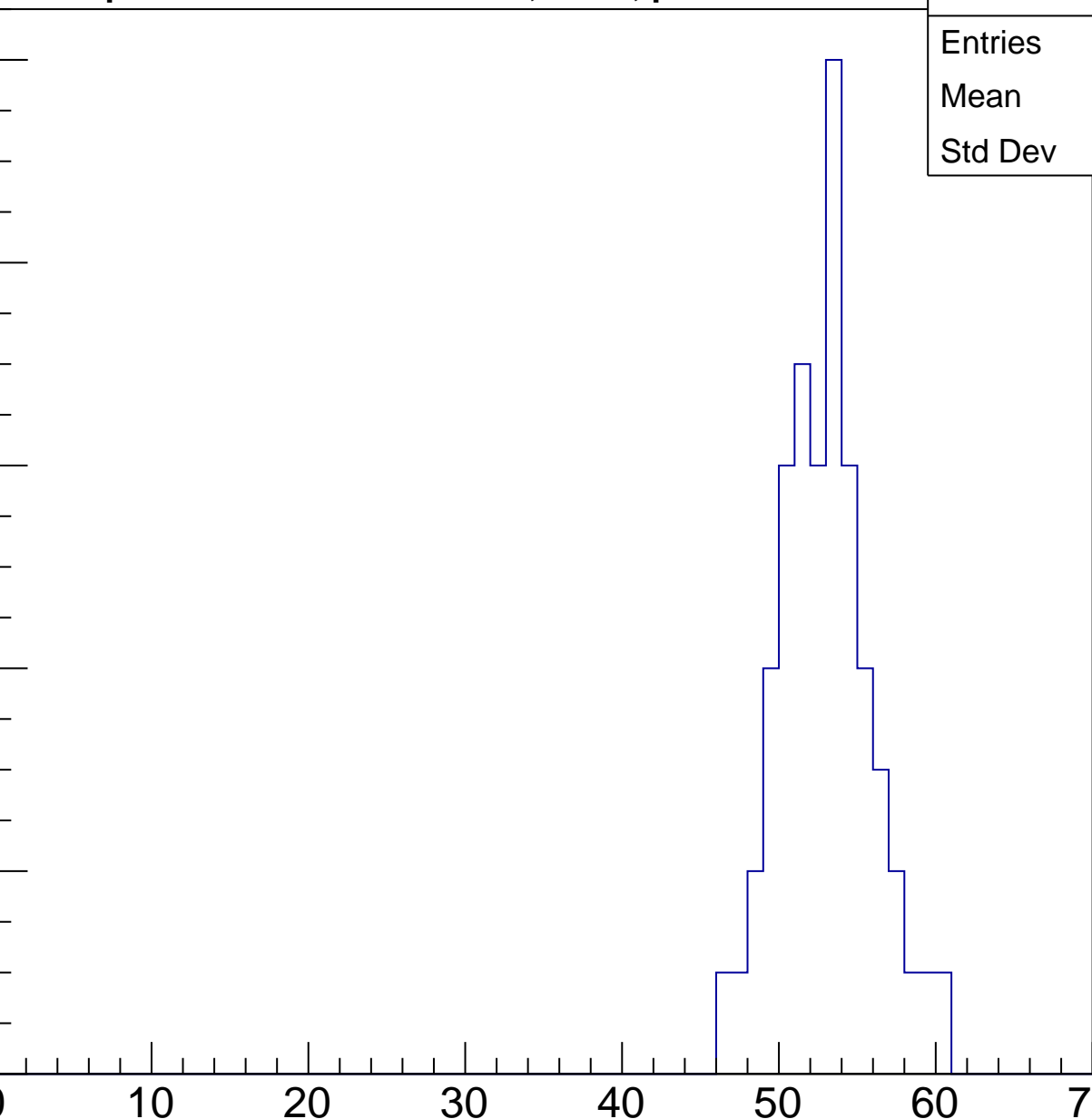
30

40

50

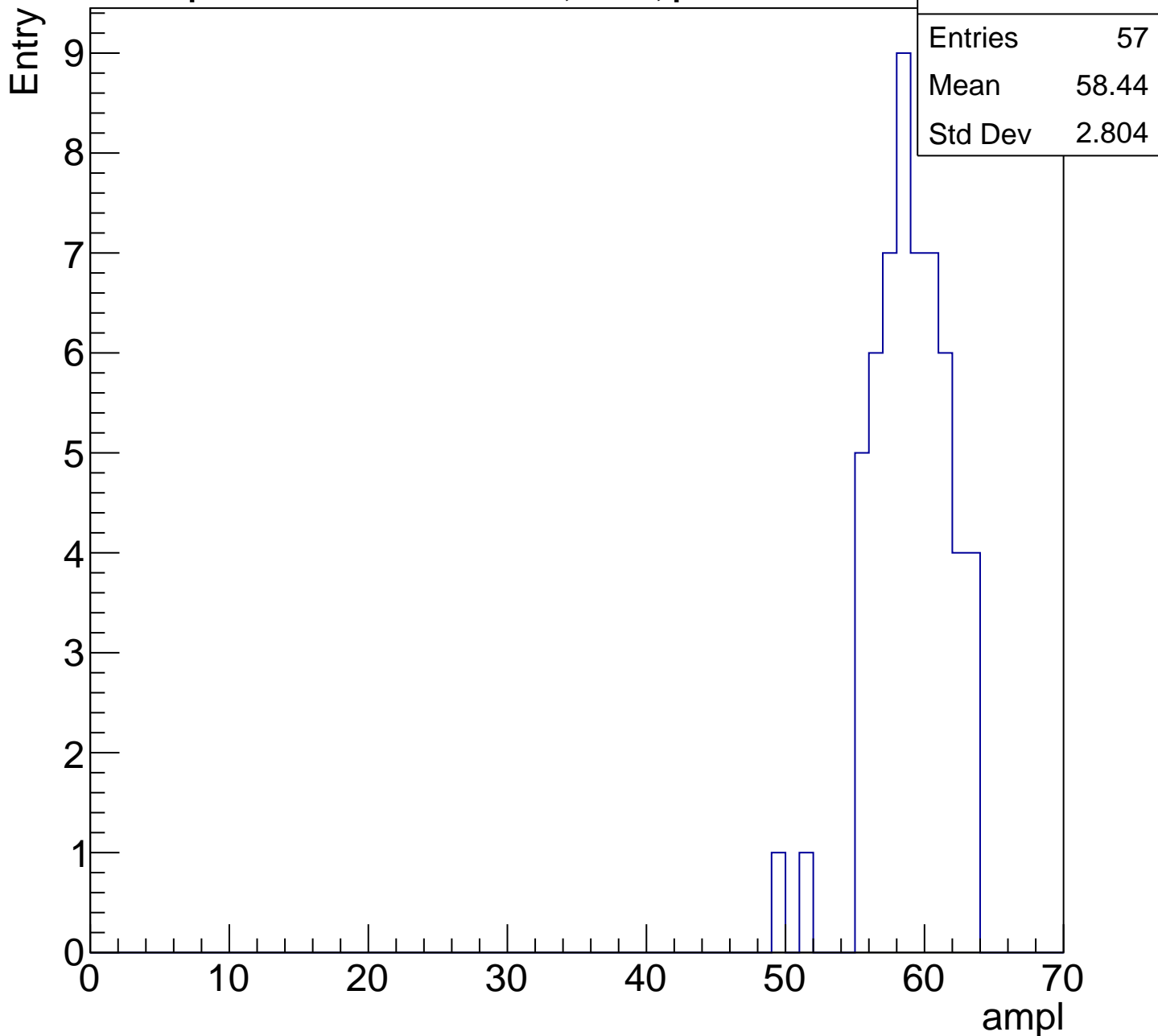
60

ampl



# B1L103S, U2-ch74, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

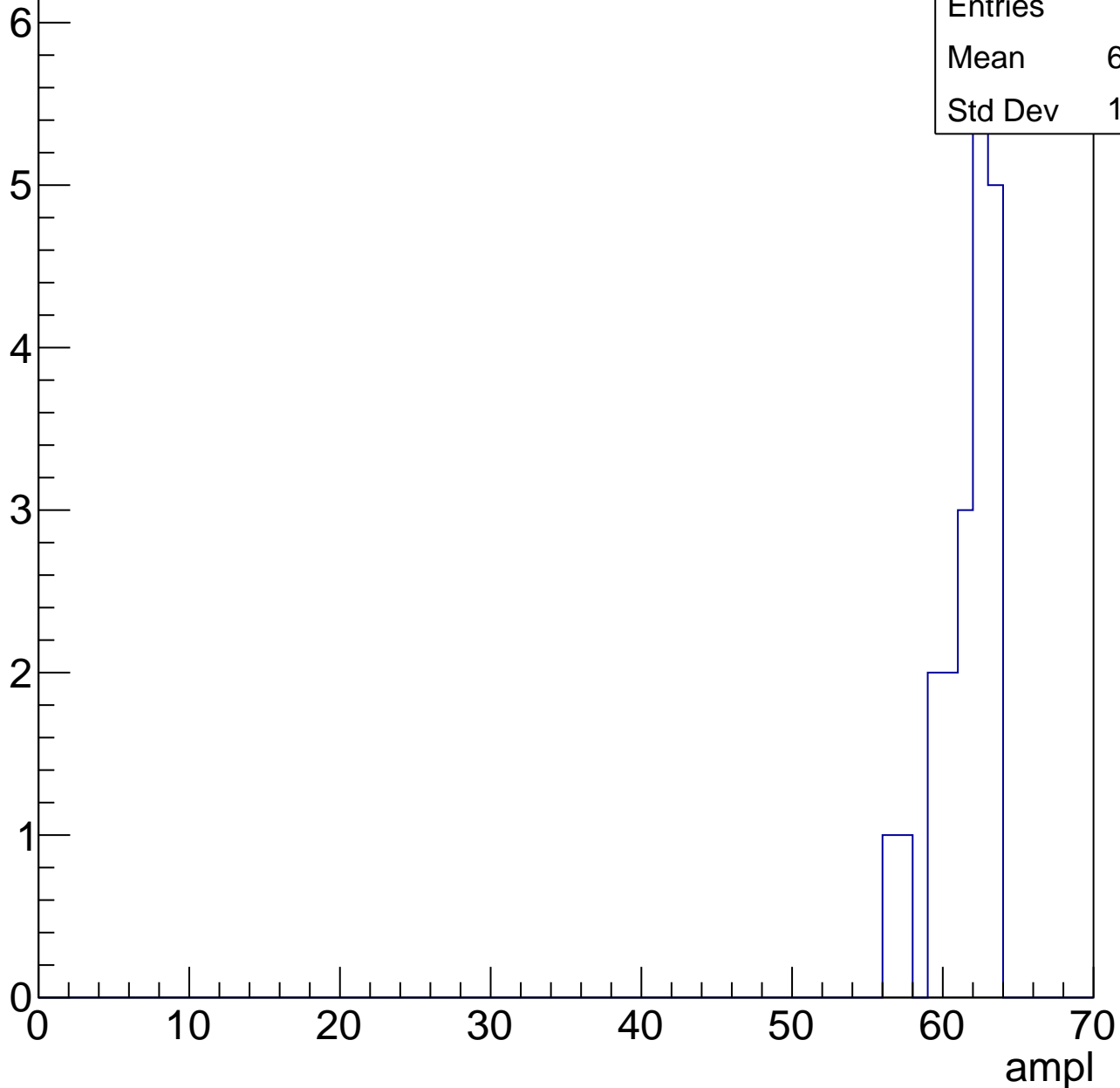


# B1L103S, U2-ch74, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	20
Mean	61.05
Std Dev	1.962





# B1L103S, U2-ch74, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch75, adc0

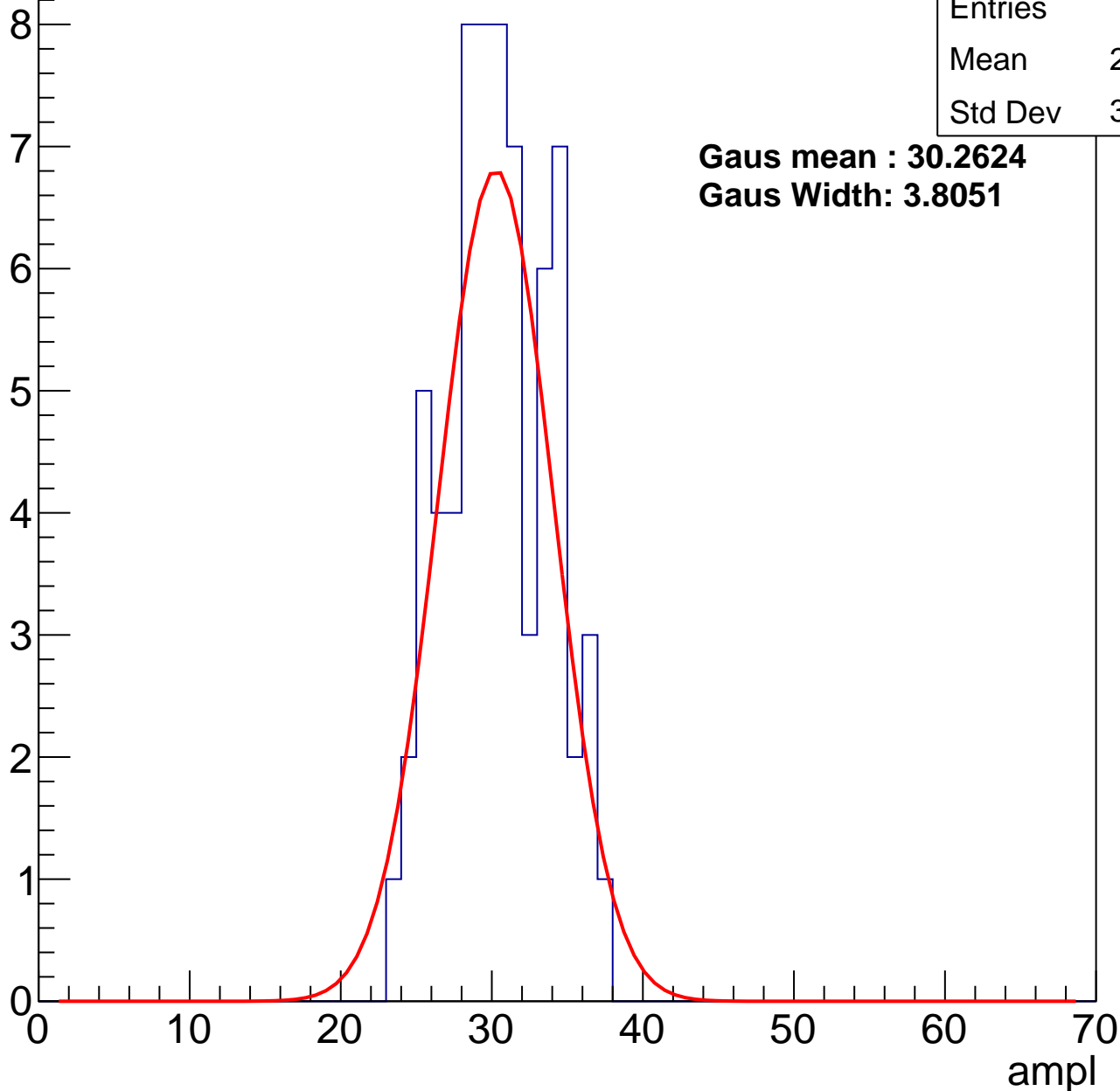
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	29.97
Std Dev	3.358

**Gaus mean : 30.2624**

**Gaus Width: 3.8051**



# B1L103S, U2-ch75, adc1

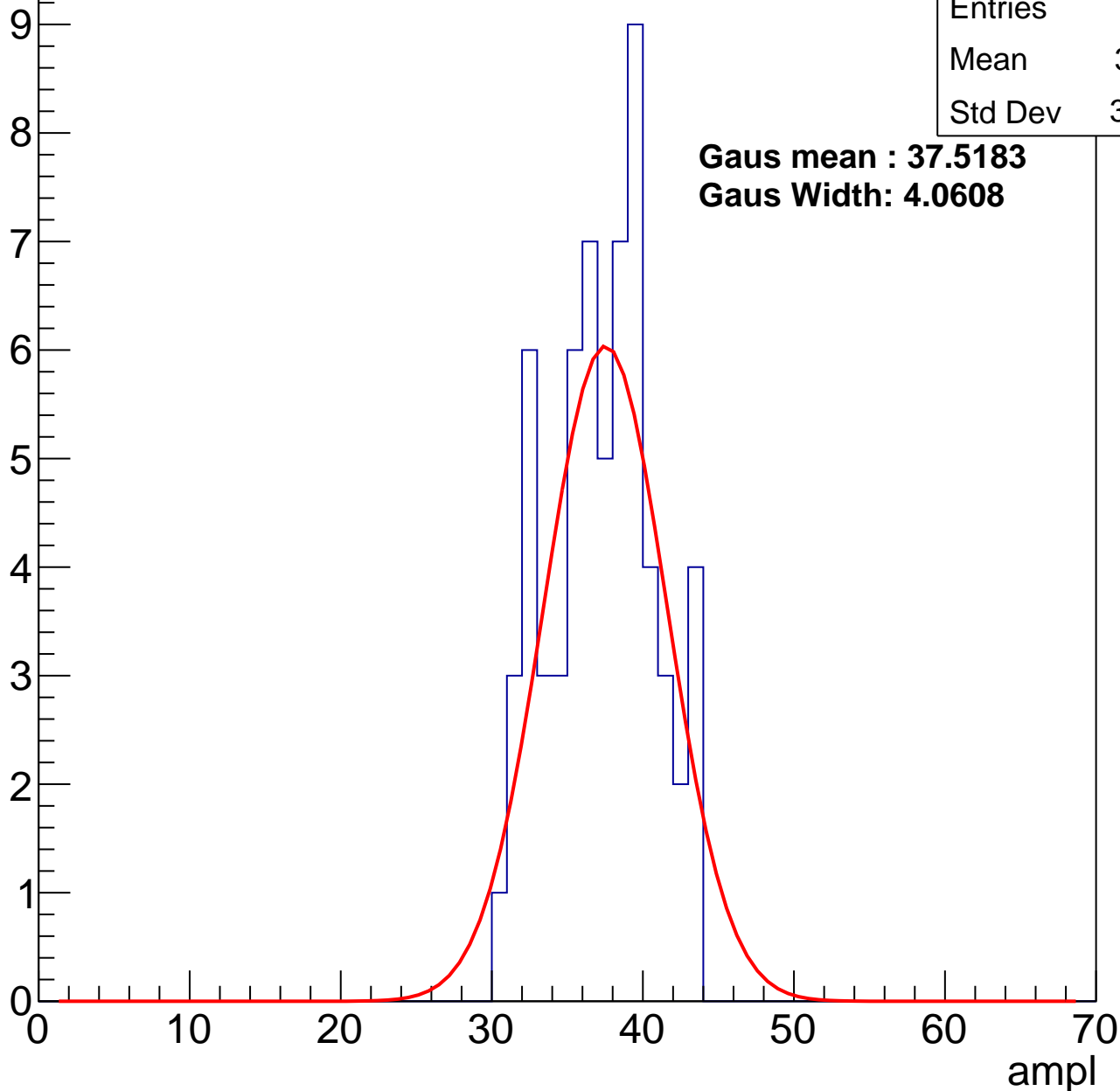
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	36.81
Std Dev	3.408

**Gaus mean : 37.5183**

**Gaus Width: 4.0608**



# B1L103S, U2-ch75, adc2

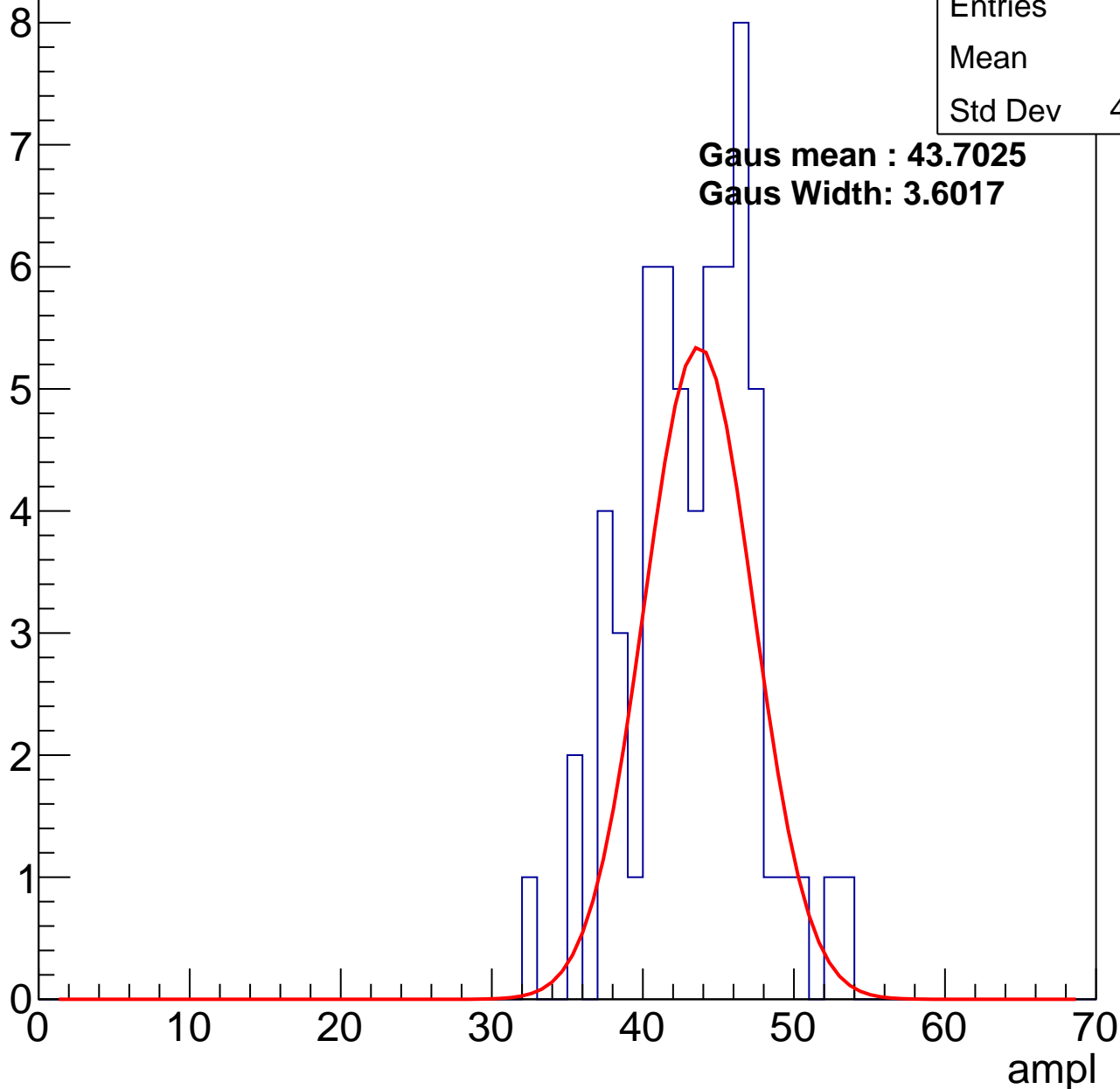
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	42.9
Std Dev	4.094

**Gaus mean : 43.7025**

**Gaus Width: 3.6017**

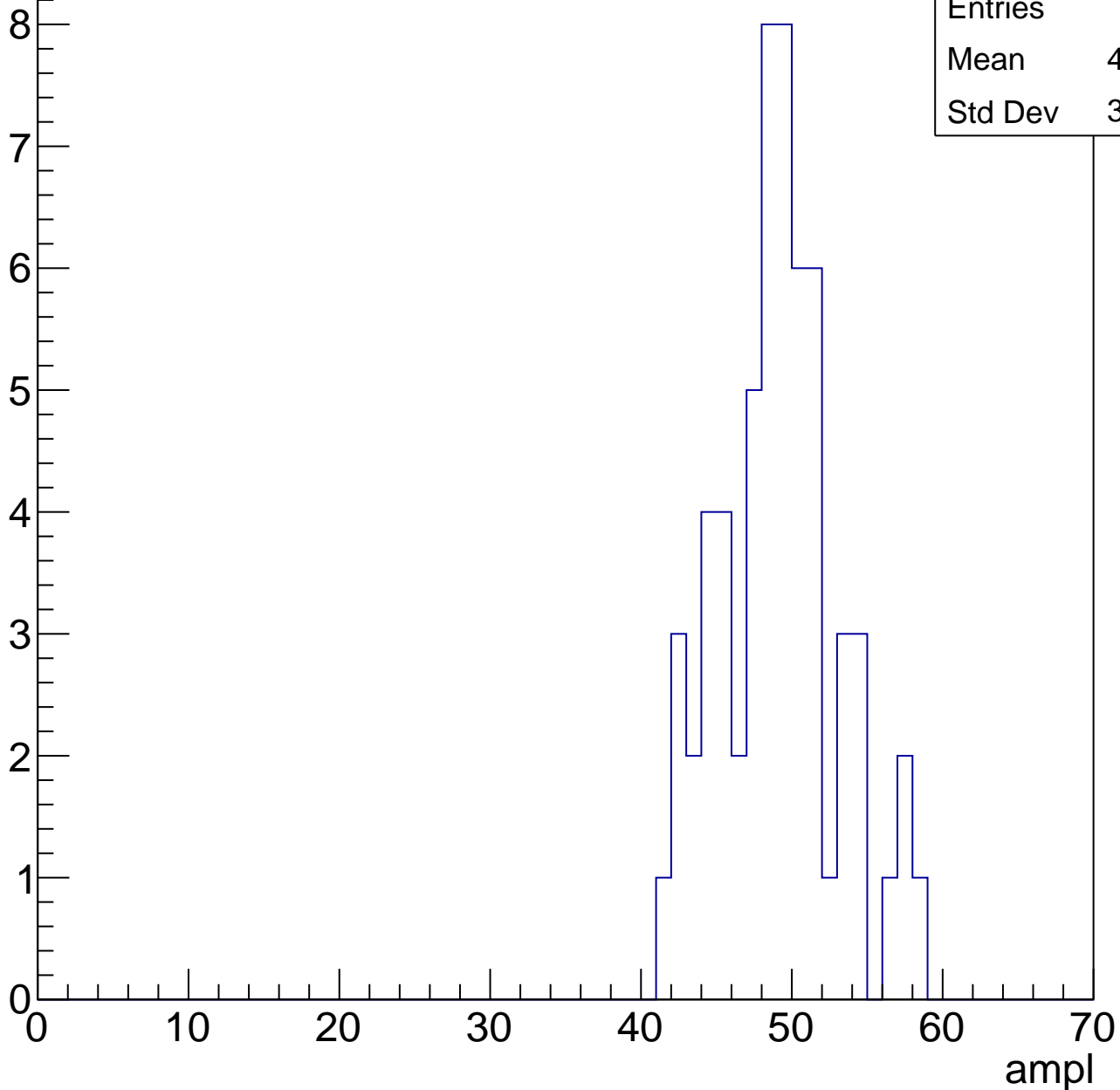


# B1L103S, U2-ch75, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

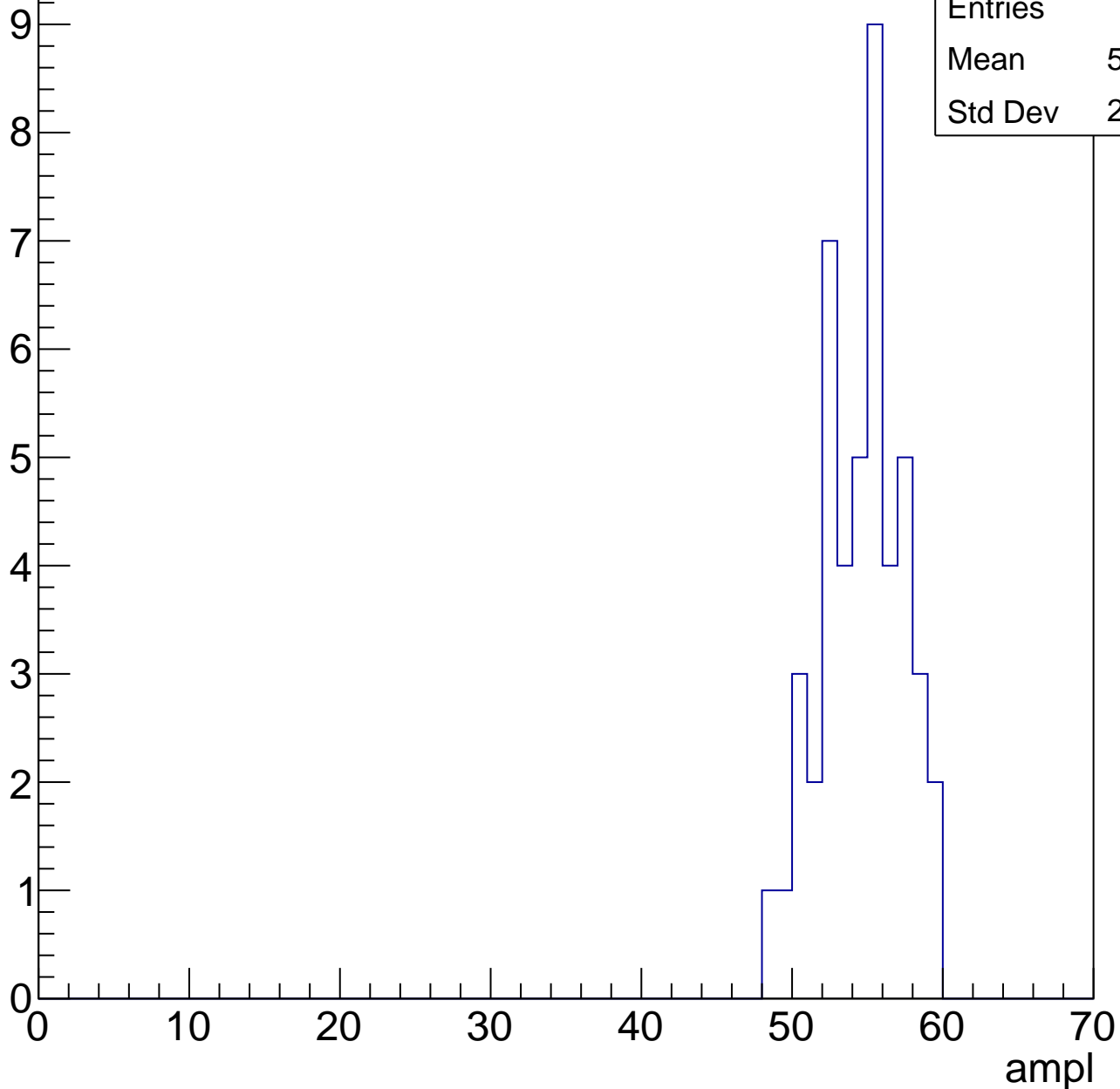
Entries	60
Mean	48.65
Std Dev	3.885



# B1L103S, U2-ch75, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch75, adc5

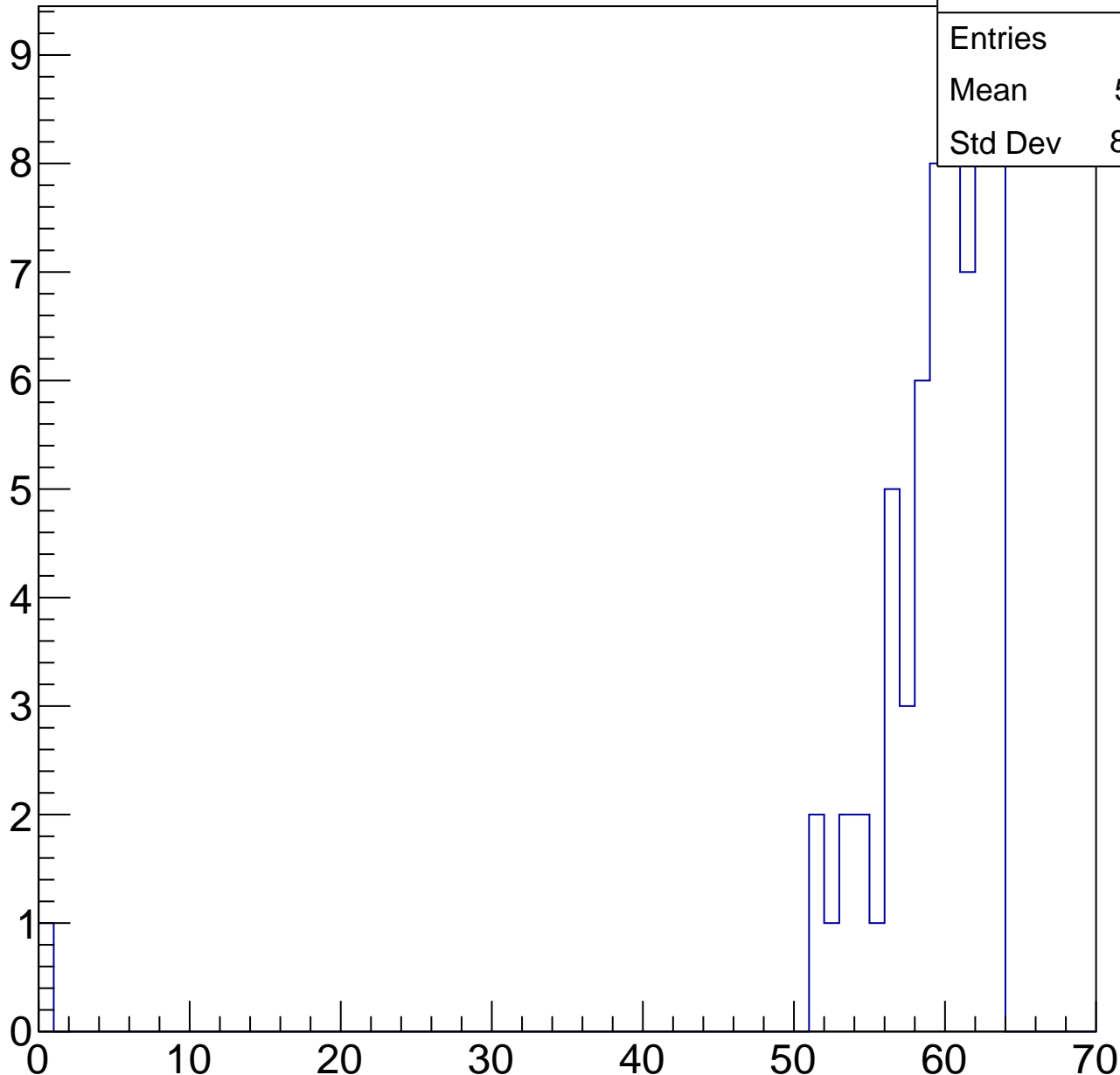
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	63
Mean	58.11
Std Dev	8.014

ampl



# B1L103S, U2-ch75, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

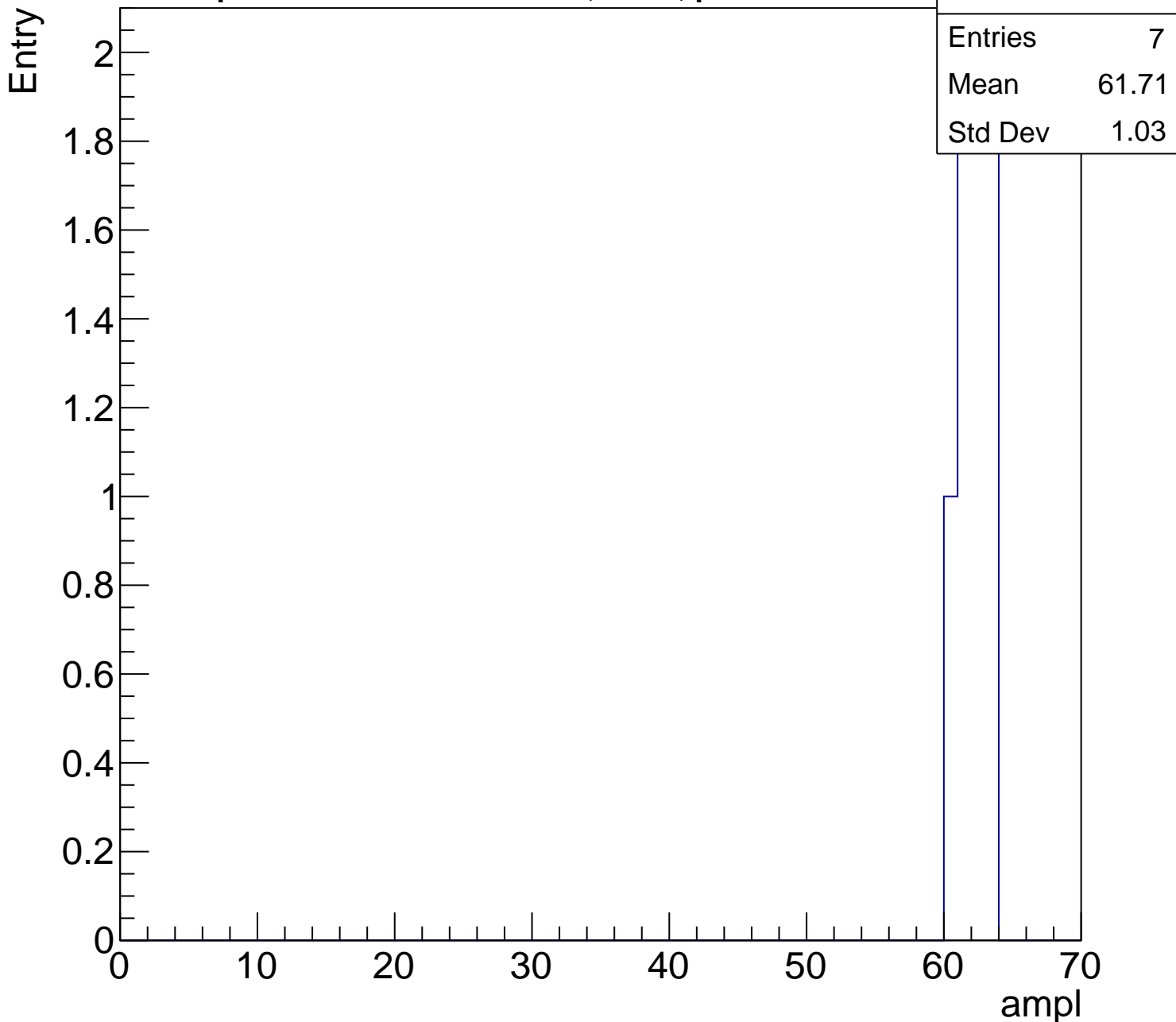
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	7
Mean	61.71
Std Dev	1.03

0 10 20 30 40 50 60 70

ampl





# B1L103S, U2-ch75, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch76, adc0

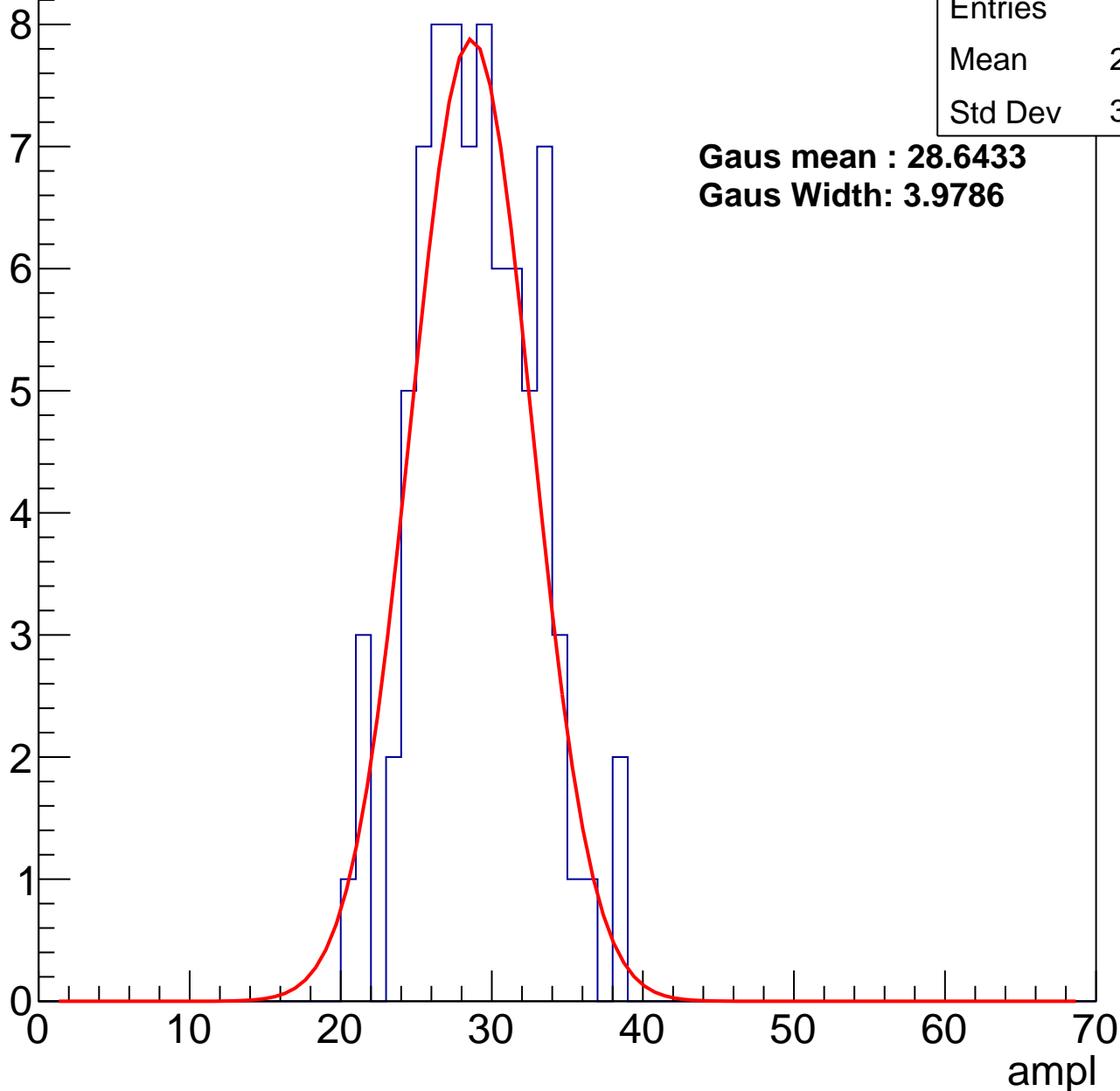
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	80
Mean	28.52
Std Dev	3.847

**Gaus mean : 28.6433**

**Gaus Width: 3.9786**



# B1L103S, U2-ch76, adc1

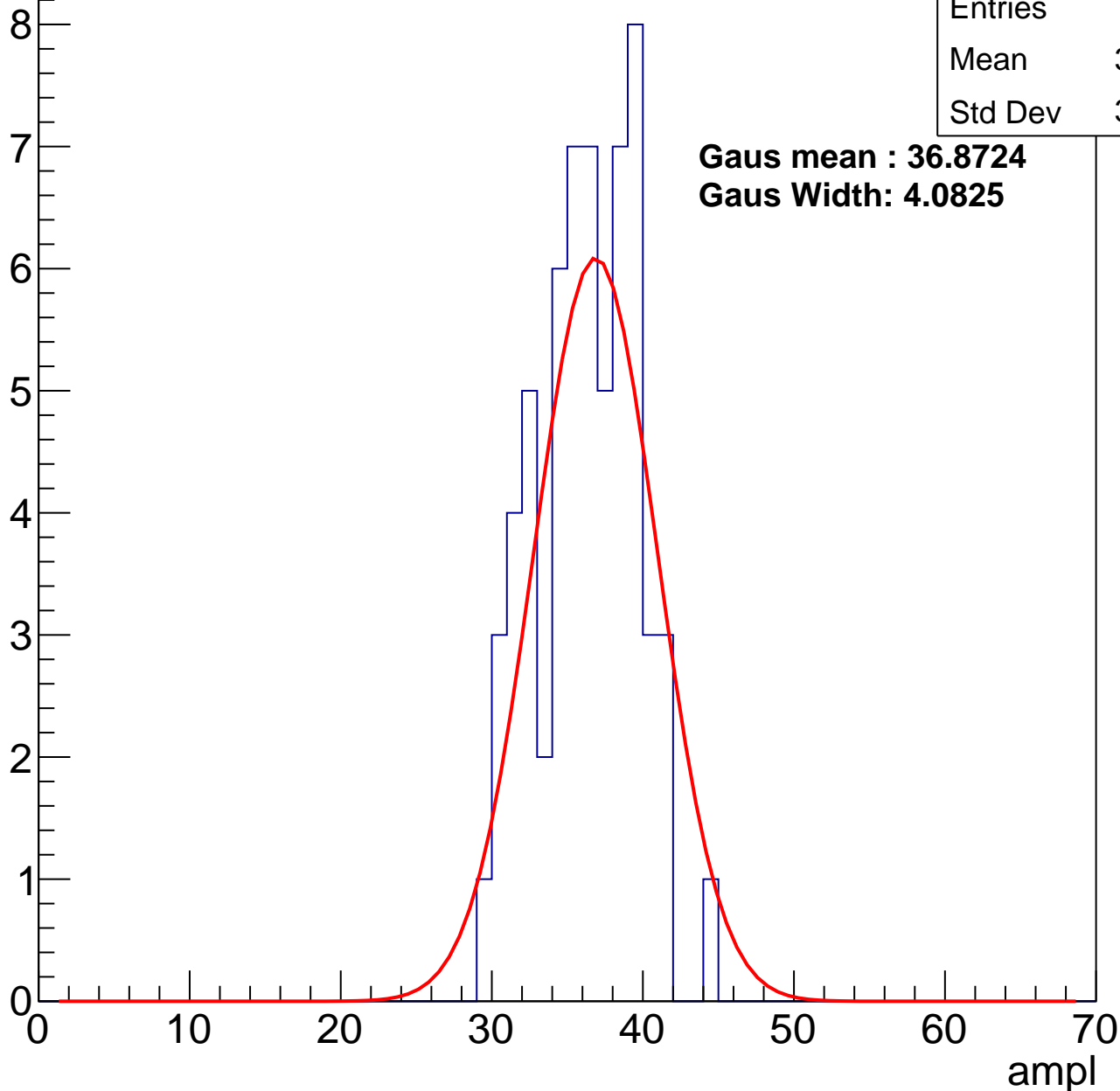
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	35.81
Std Dev	3.301

**Gaus mean : 36.8724**

**Gaus Width: 4.0825**



# B1L103S, U2-ch76, adc2

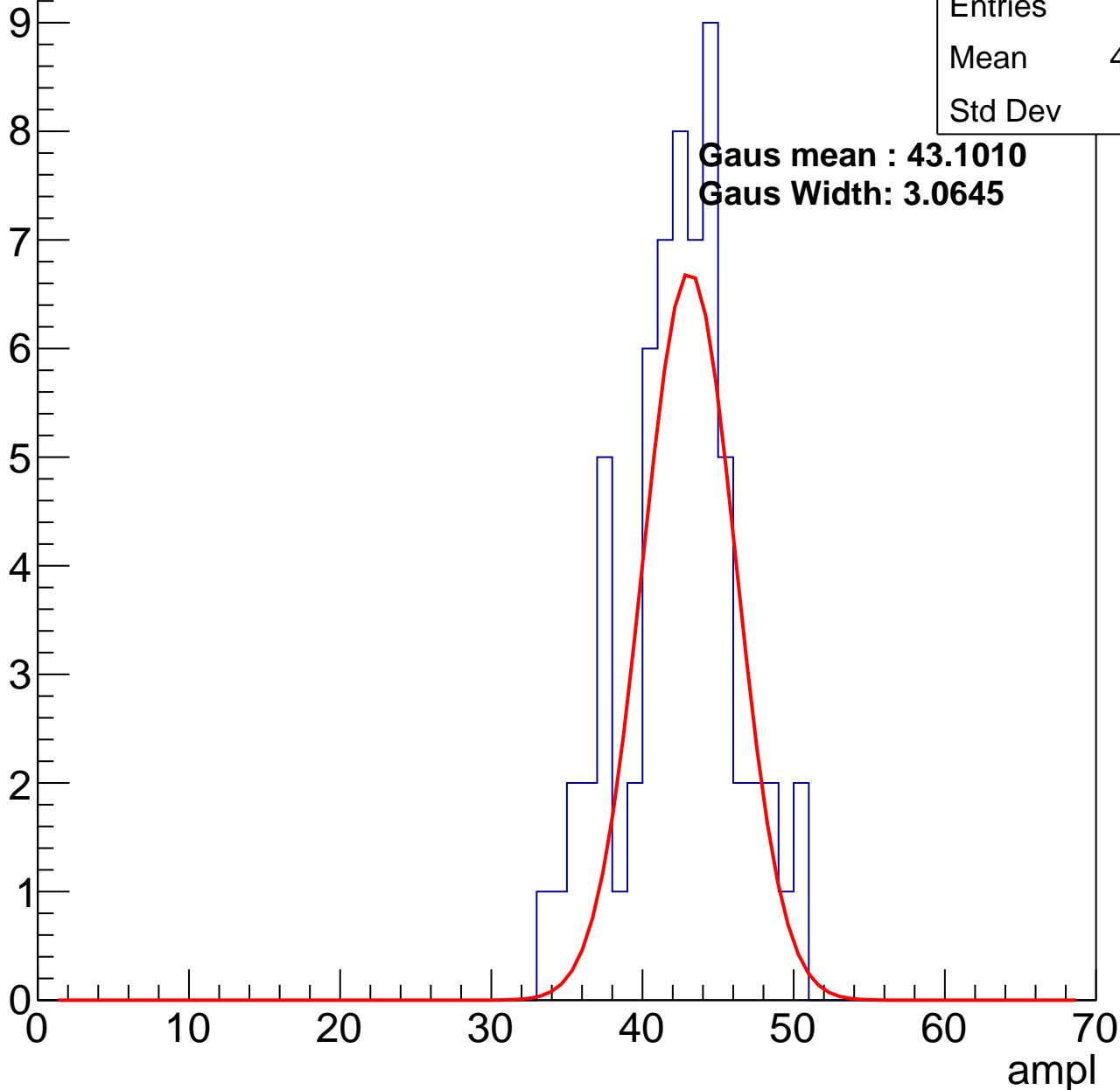
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	41.94
Std Dev	3.77

**Gaus mean : 43.1010**

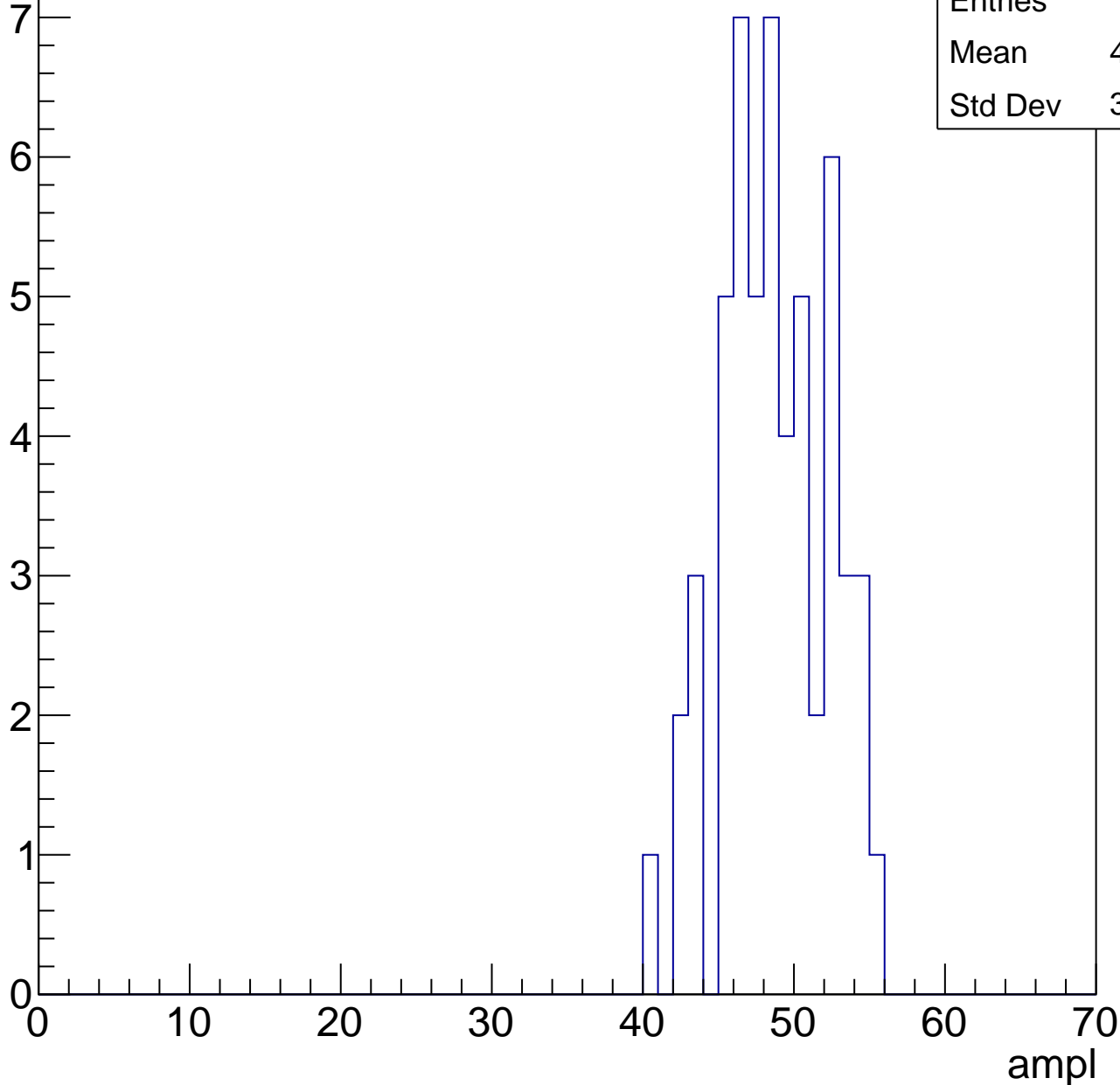
**Gaus Width: 3.0645**



# B1L103S, U2-ch76, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

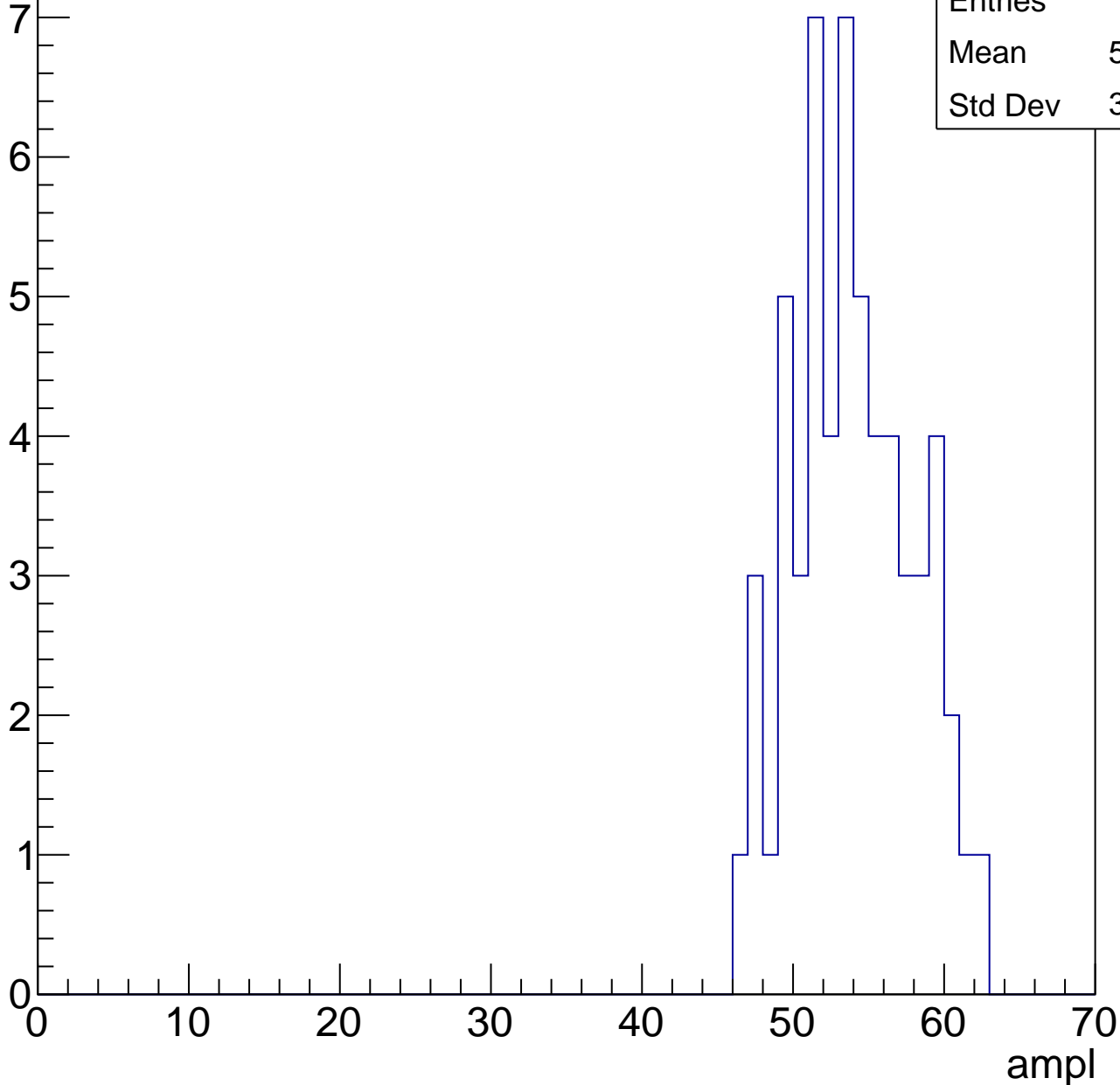


# B1L103S, U2-ch76, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	53.52
Std Dev	3.879

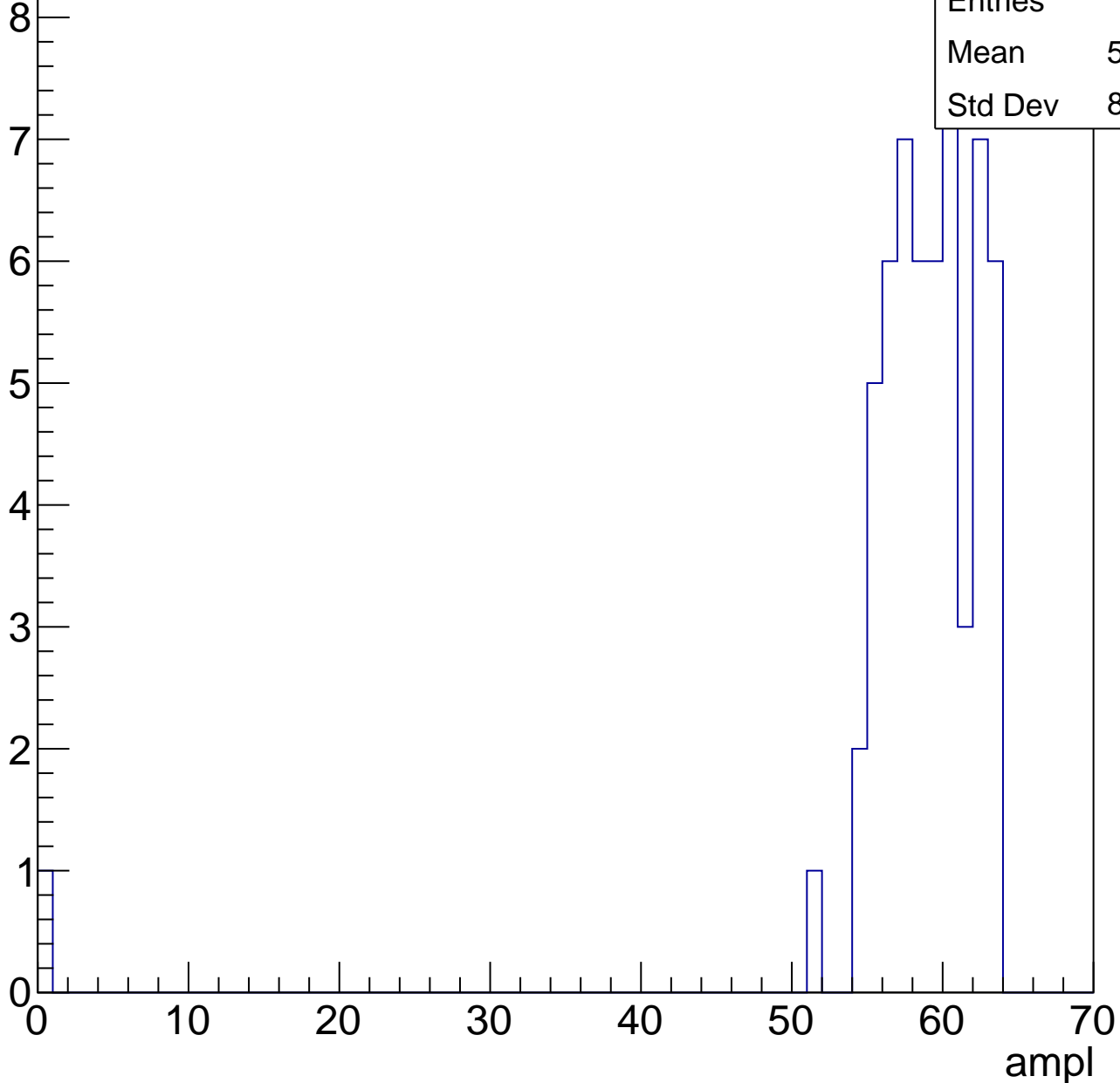


# B1L103S, U2-ch76, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	57.69
Std Dev	8.139

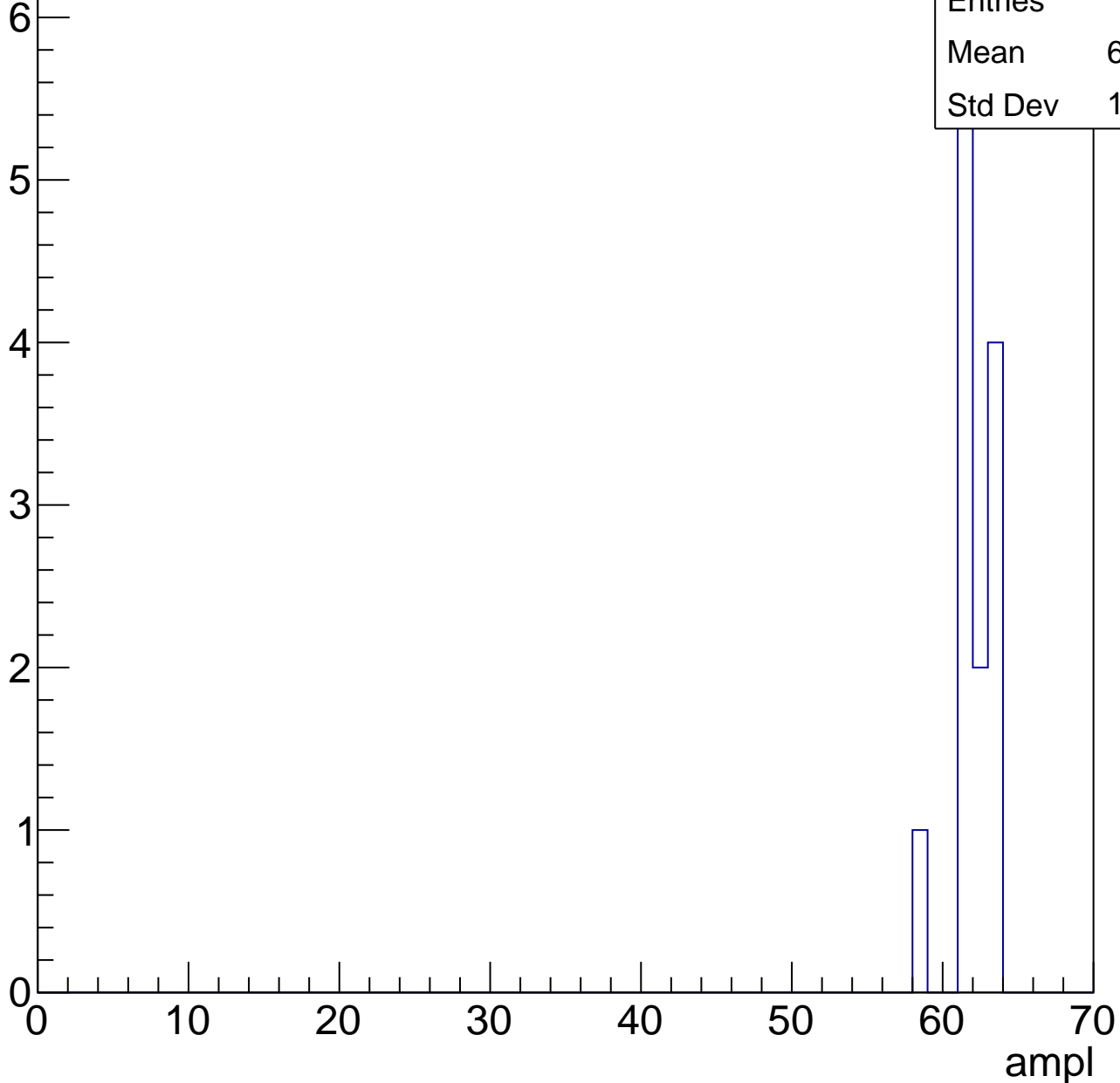


# B1L103S, U2-ch76, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	13
Mean	61.54
Std Dev	1.337





# B1L103S, U2-ch76, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U2-ch77, adc0

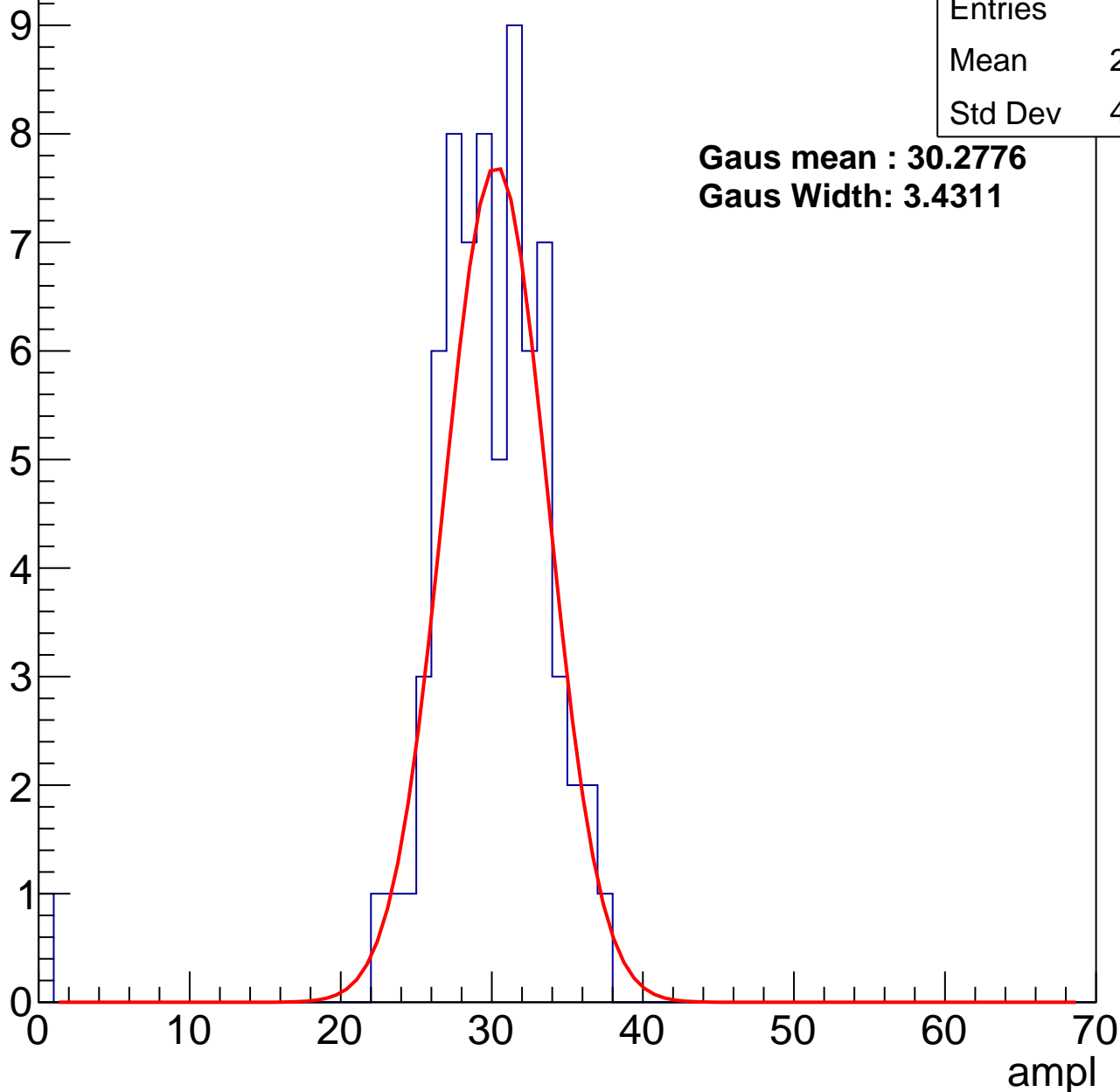
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	29.25
Std Dev	4.752

**Gaus mean : 30.2776**

**Gaus Width: 3.4311**



# B1L103S, U2-ch77, adc1

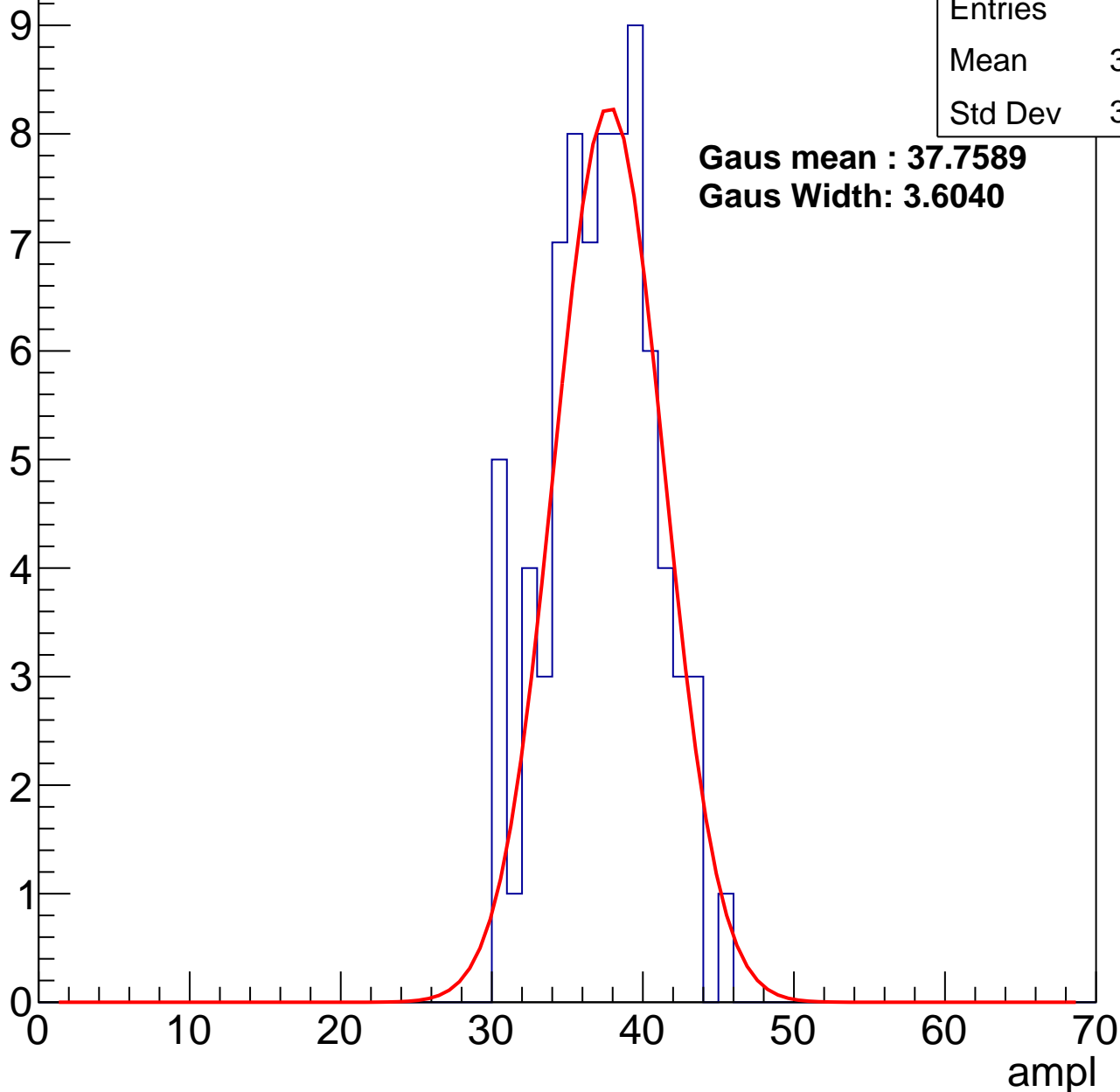
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	36.79
Std Dev	3.488

**Gaus mean : 37.7589**

**Gaus Width: 3.6040**



# B1L103S, U2-ch77, adc2

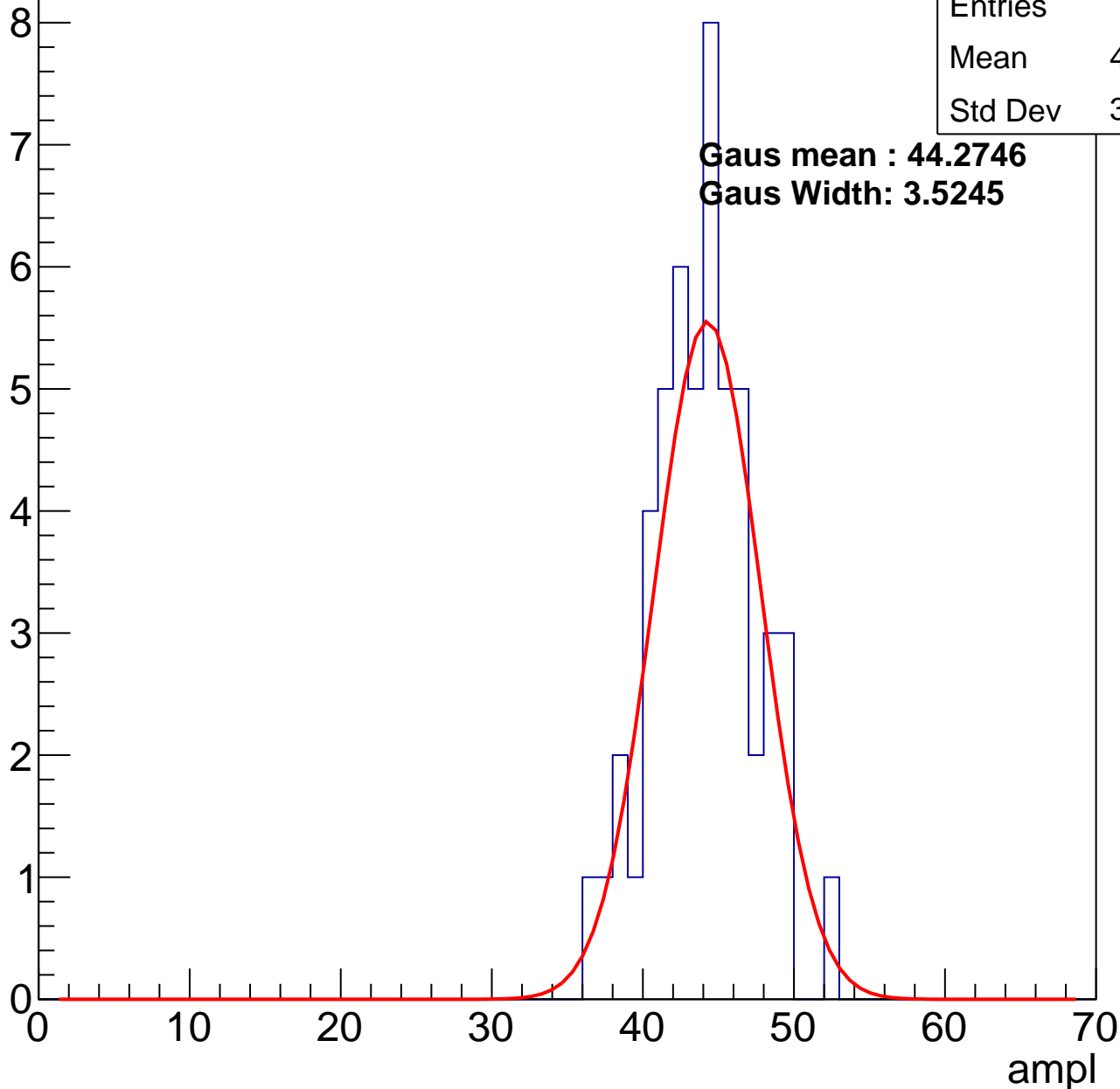
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	43.54
Std Dev	3.302

**Gaus mean : 44.2746**

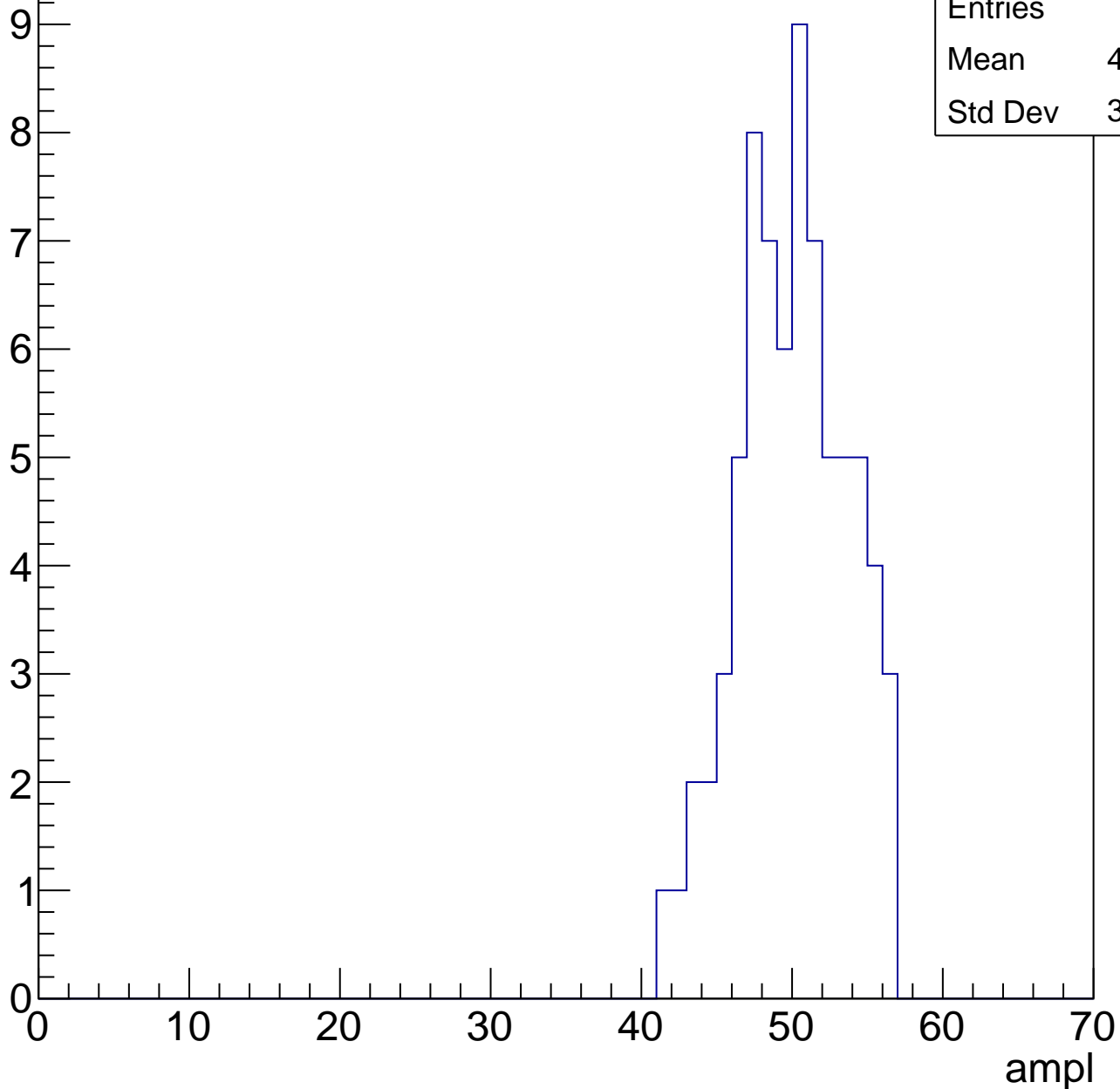
**Gaus Width: 3.5245**



# B1L103S, U2-ch77, adc3

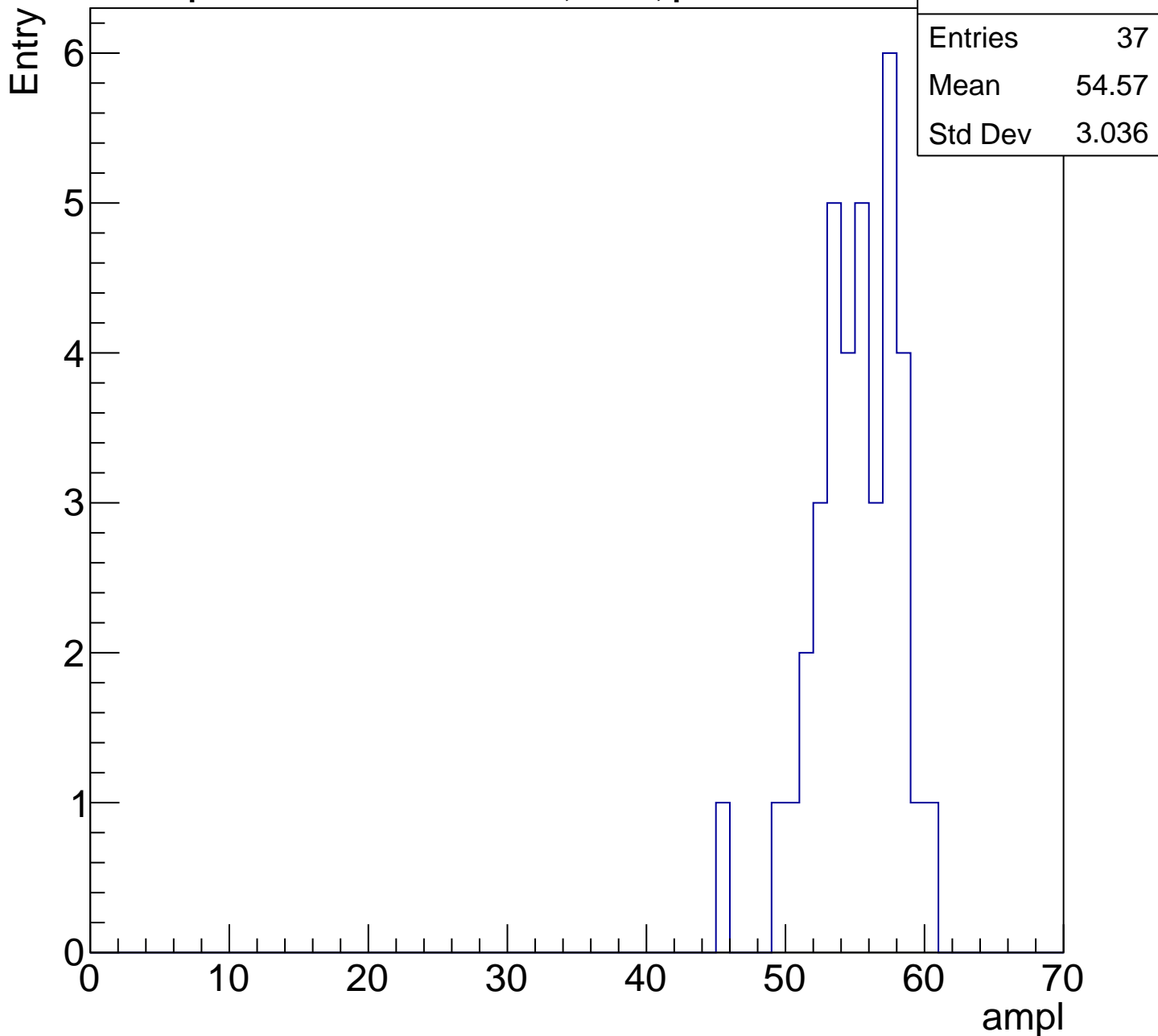
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch77, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

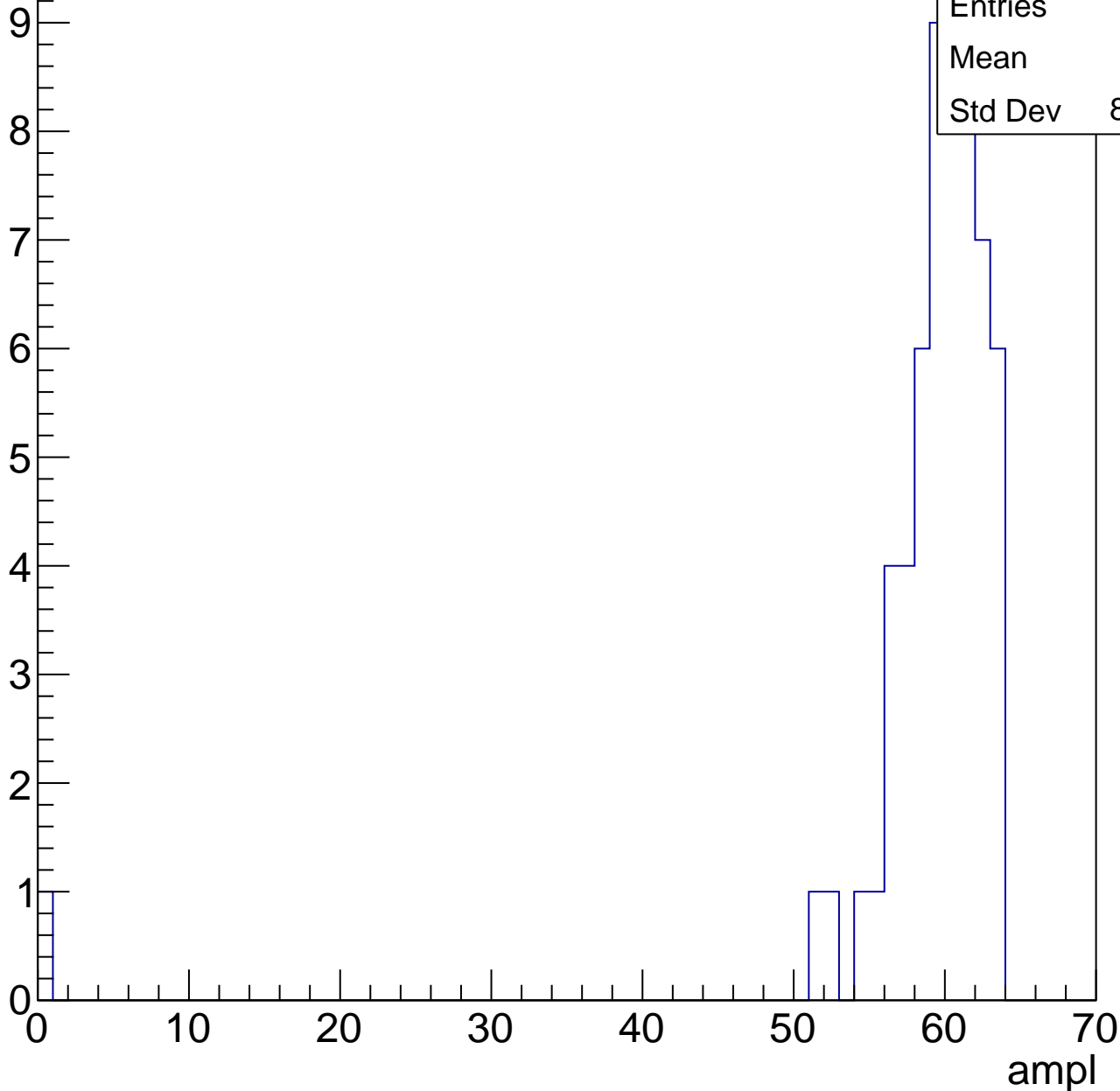


# B1L103S, U2-ch77, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

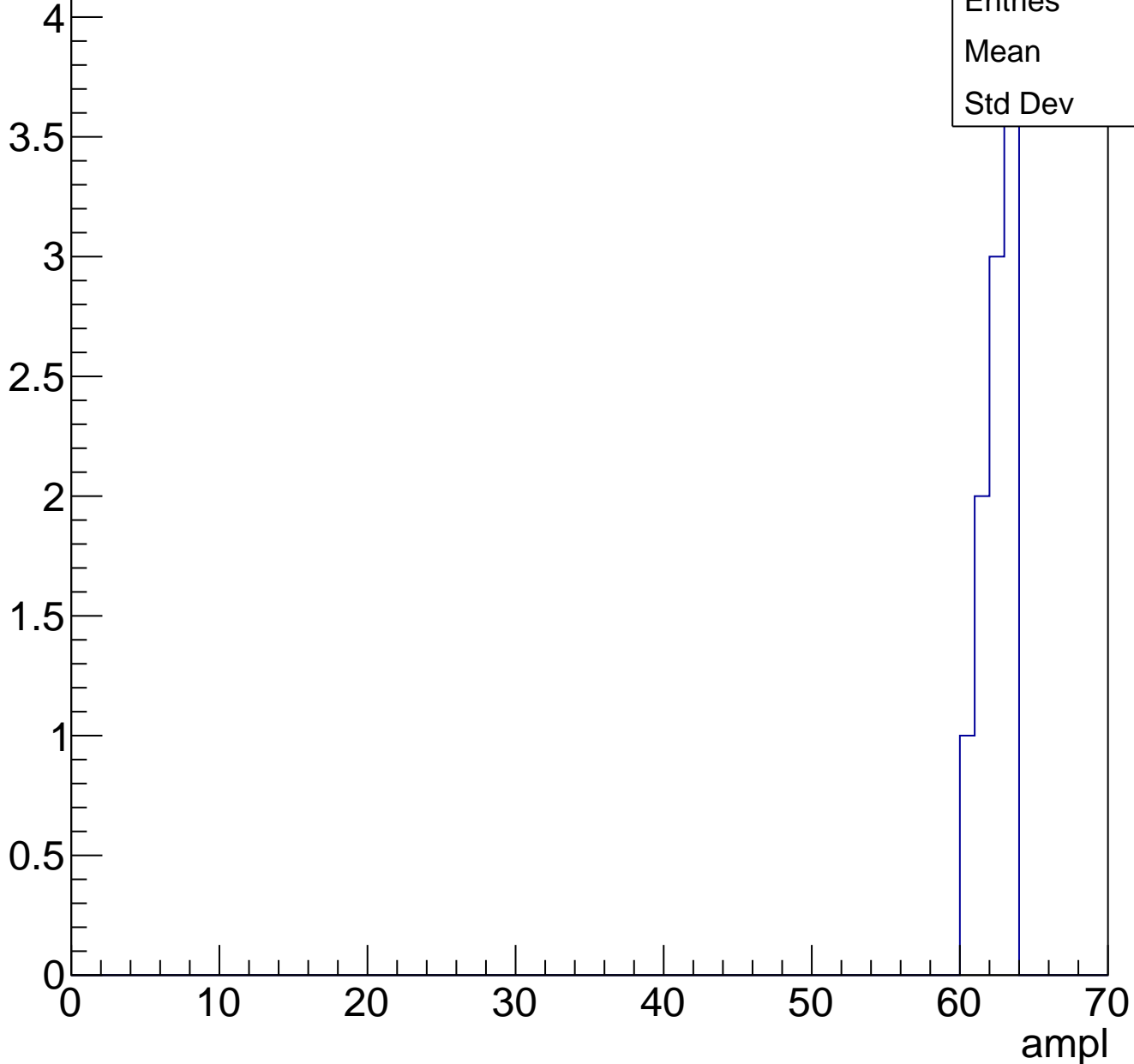
Entries	57
Mean	58.3
Std Dev	8.233



# B1L103S, U2-ch77, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U2-ch77, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	10.5
Std Dev	10.5

# B1L103S, U2-ch78, adc0

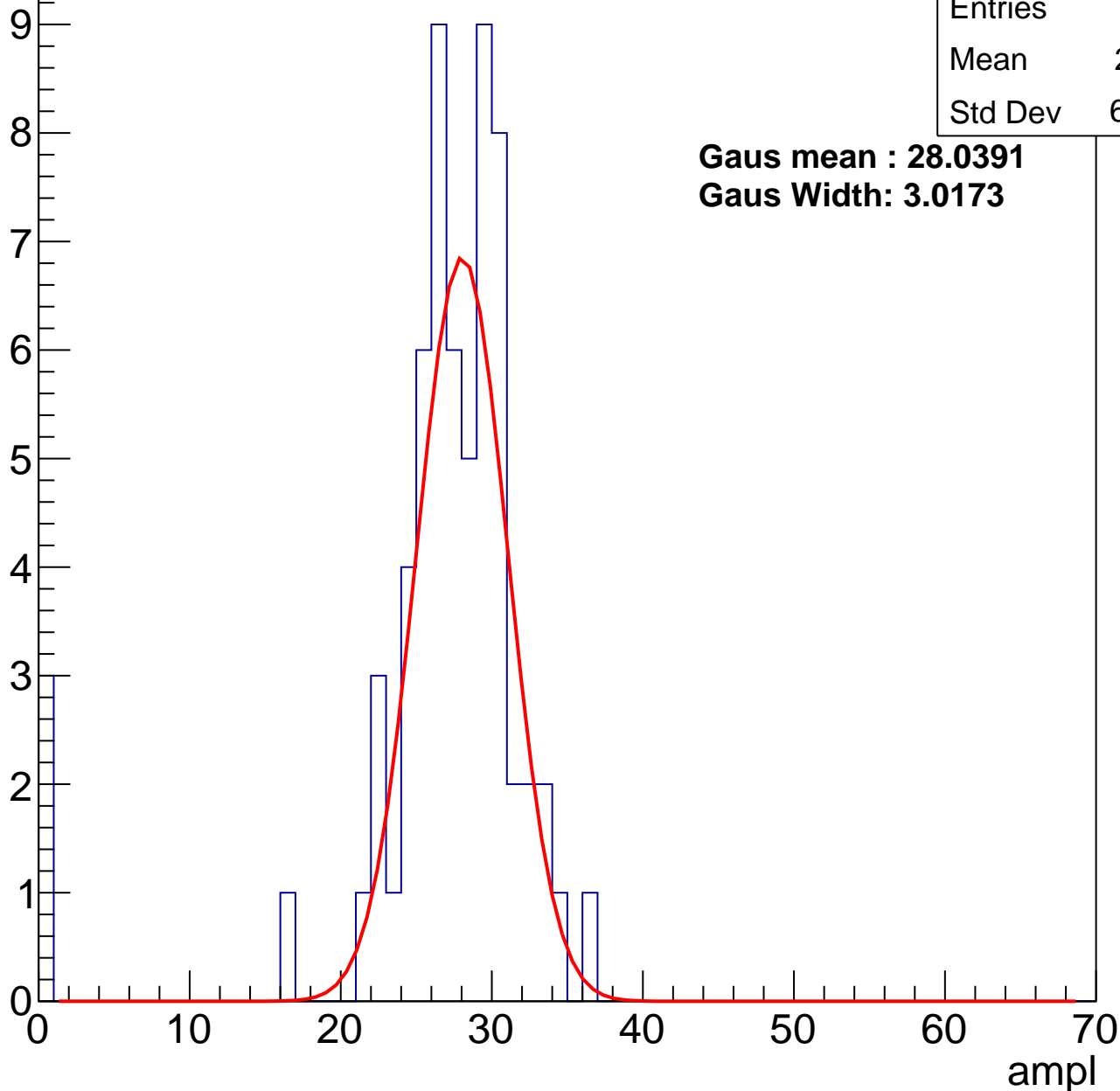
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	26.11
Std Dev	6.673

**Gaus mean : 28.0391**

**Gaus Width: 3.0173**



# B1L103S, U2-ch78, adc1

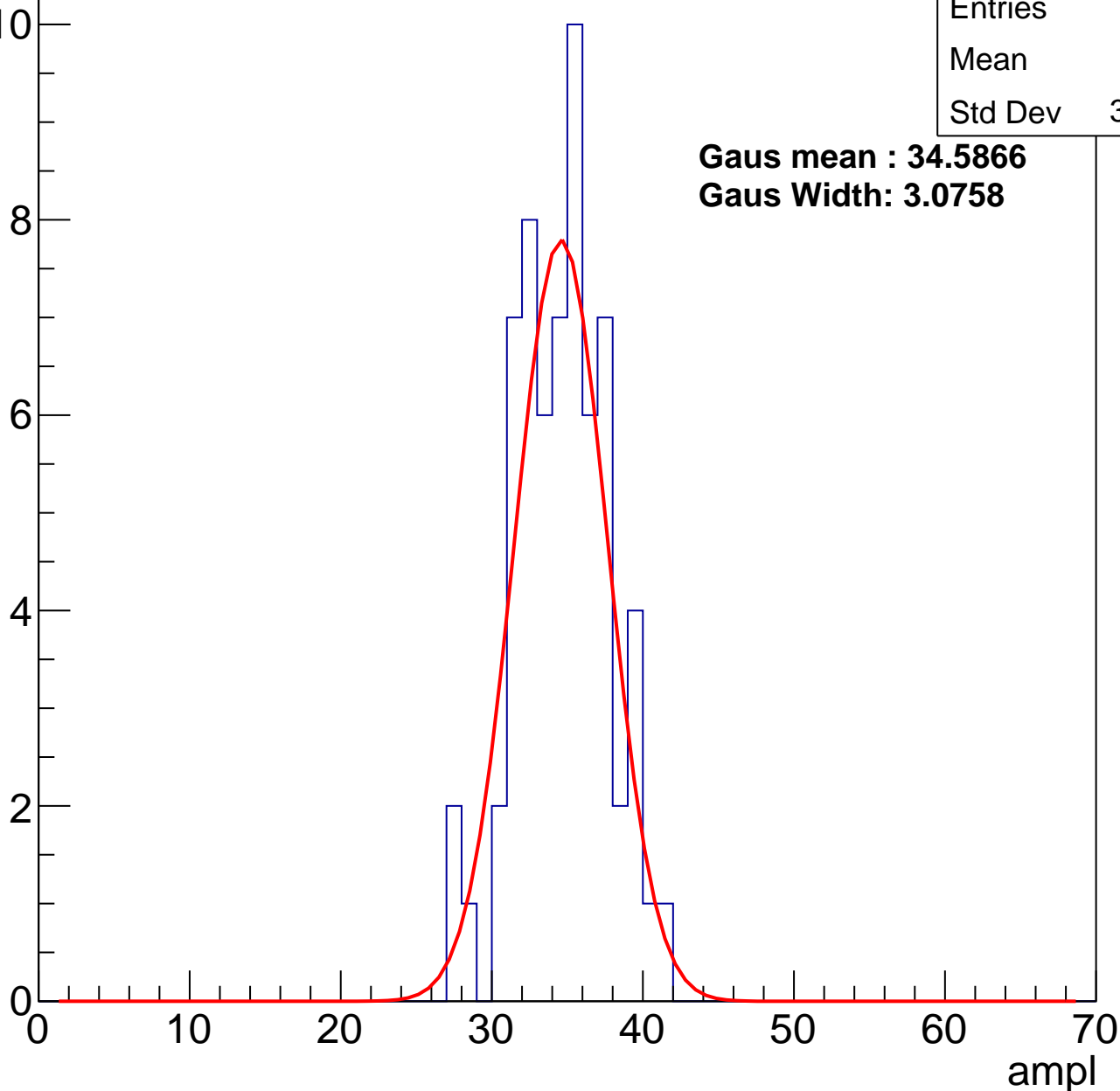
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	34.2
Std Dev	3.006

**Gaus mean : 34.5866**

**Gaus Width: 3.0758**



# B1L103S, U2-ch78, adc2

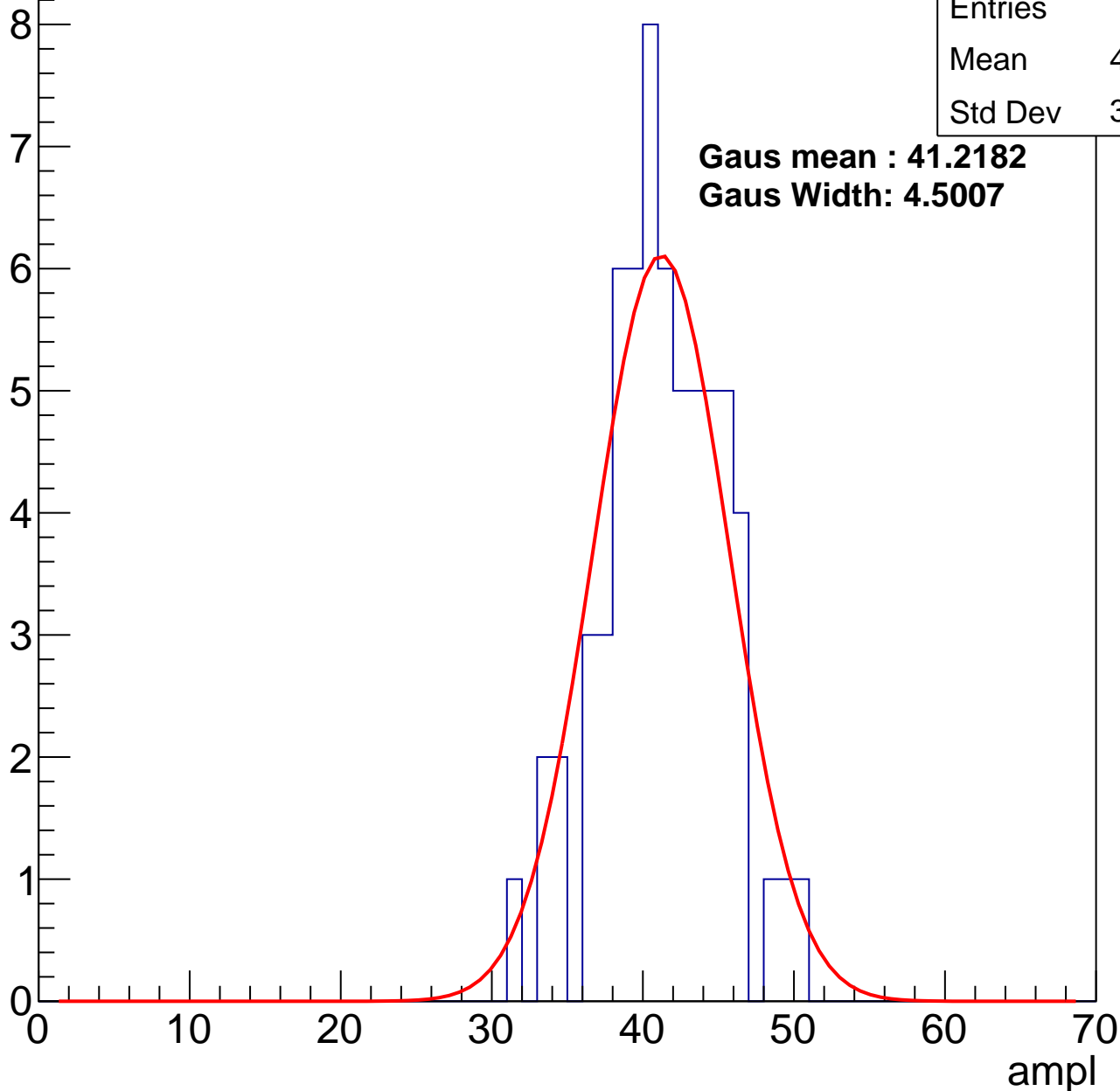
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	40.83
Std Dev	3.907

**Gaus mean : 41.2182**

**Gaus Width: 4.5007**

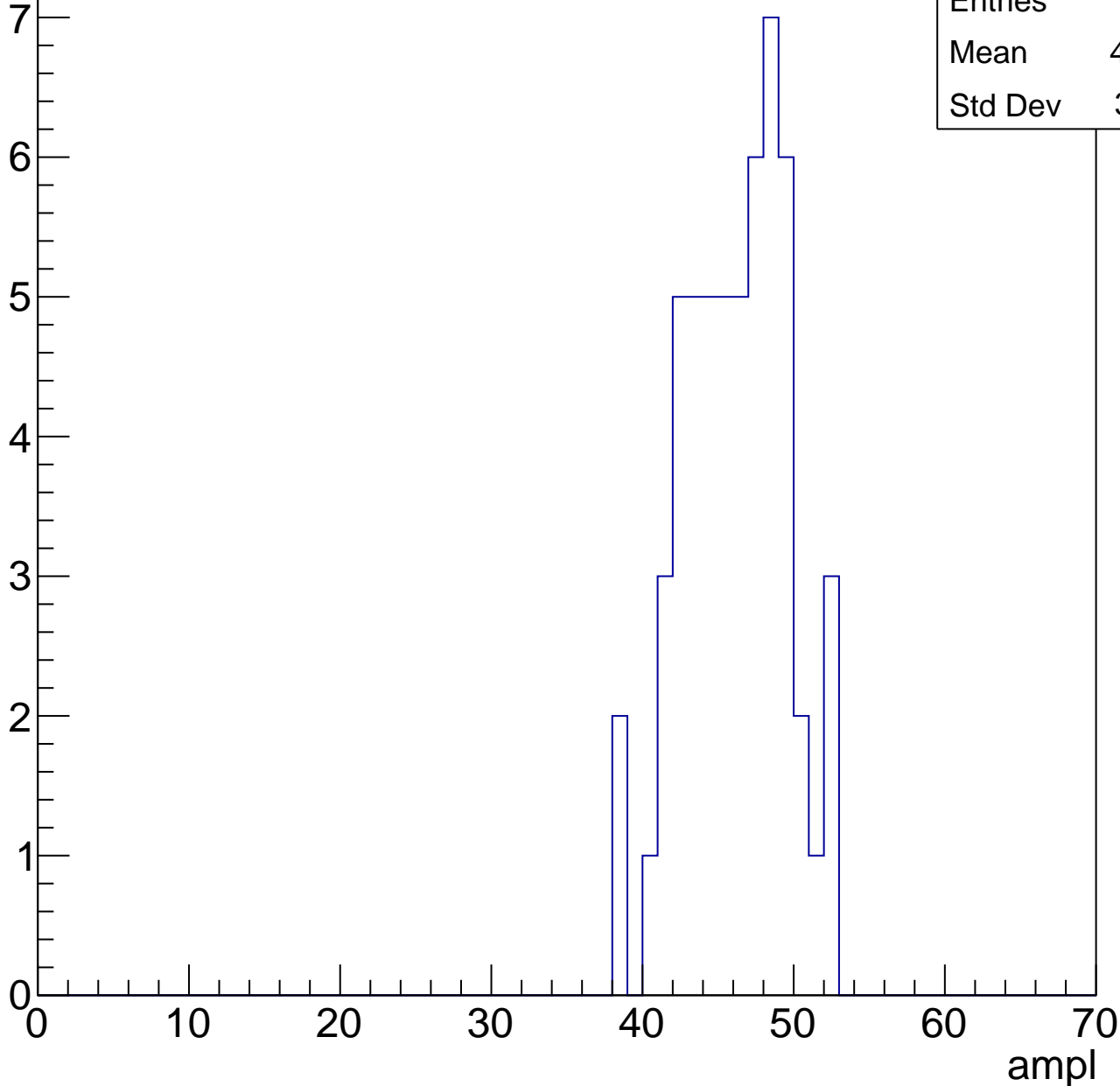


# B1L103S, U2-ch78, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	45.68
Std Dev	3.371

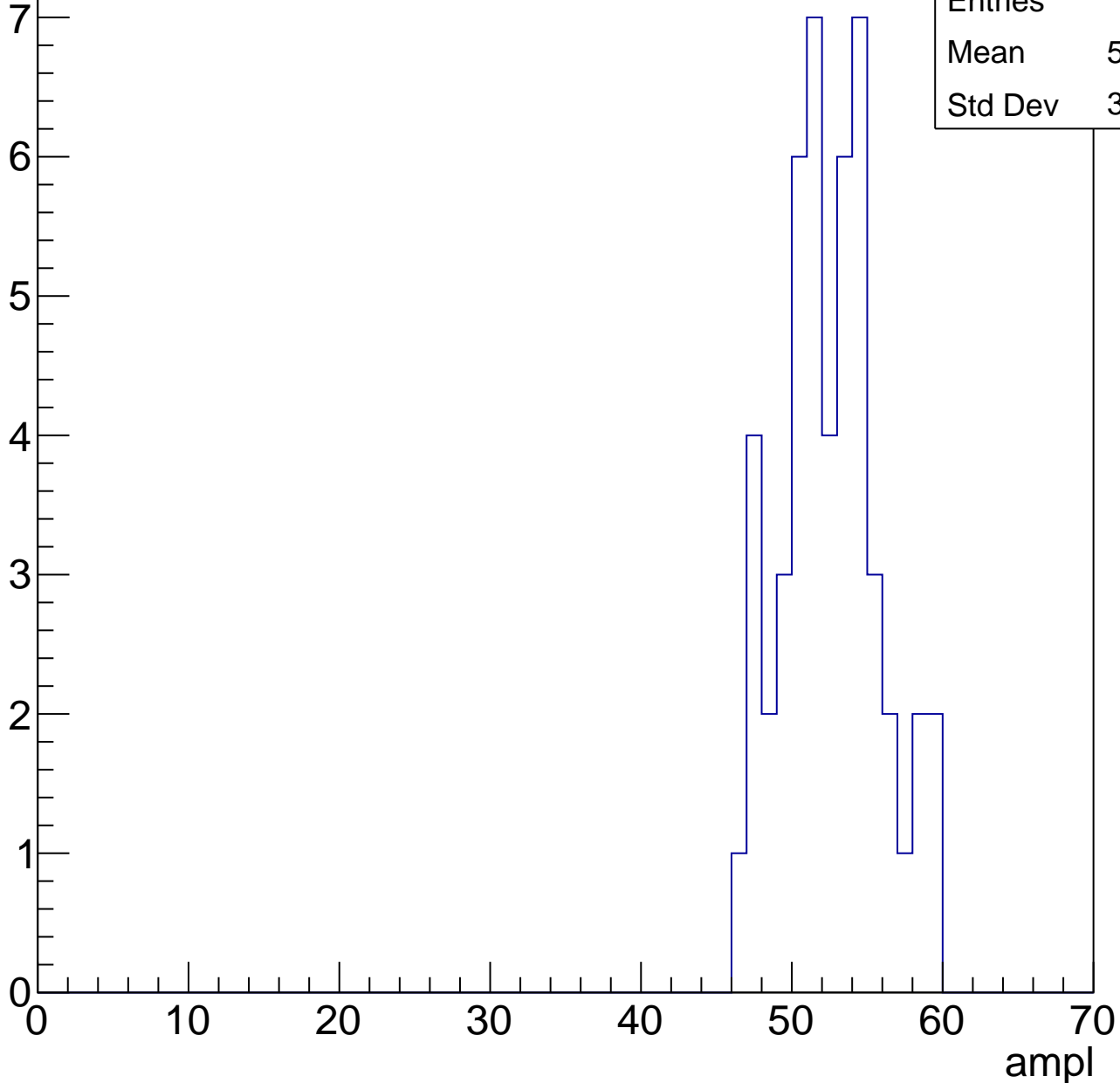


# B1L103S, U2-ch78, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	52.12
Std Dev	3.204

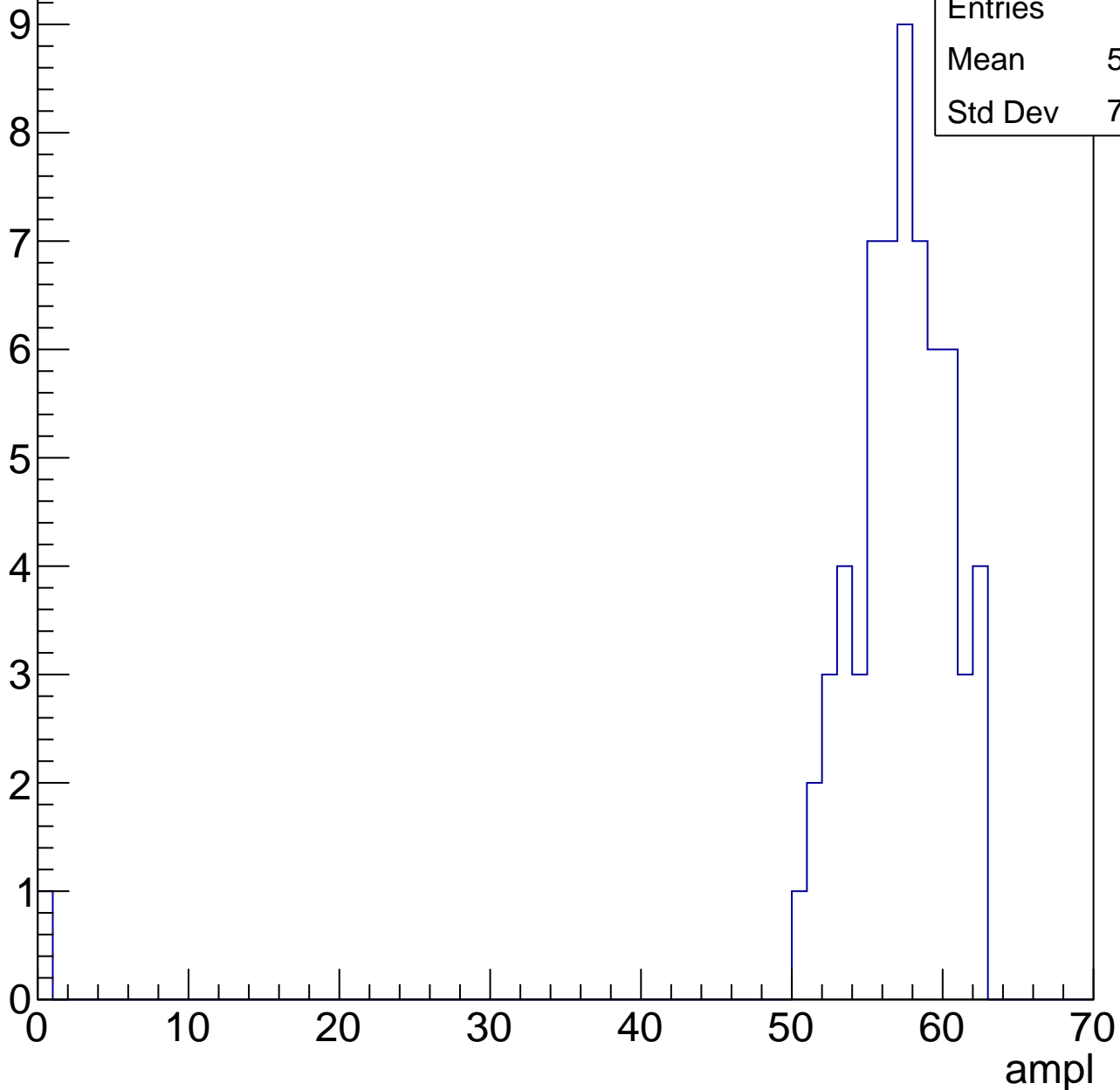


# B1L103S, U2-ch78, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	55.92
Std Dev	7.695

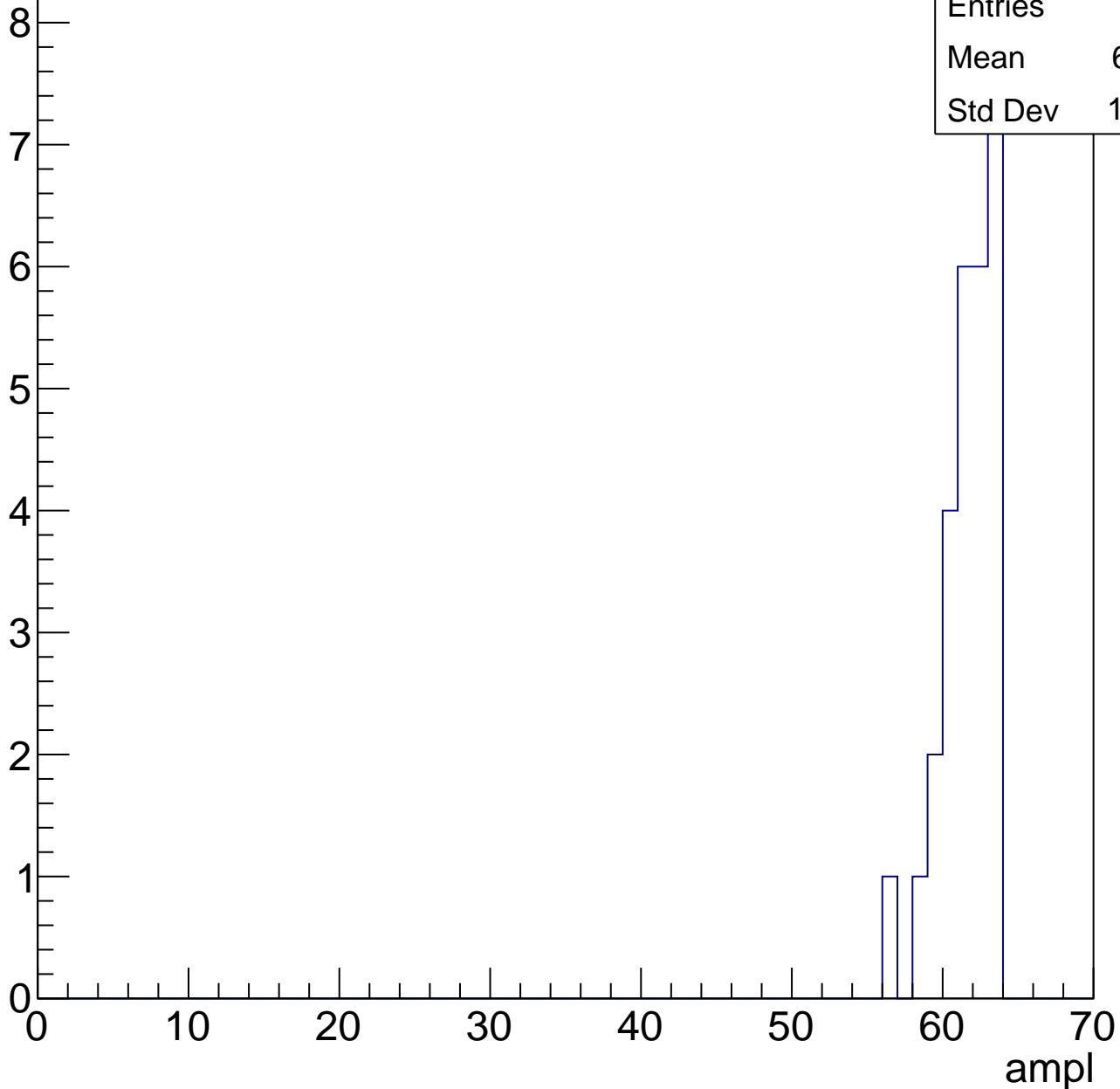


# B1L103S, U2-ch78, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	28
Mean	61.21
Std Dev	1.719





# B1L103S, U2-ch78, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch79, adc0

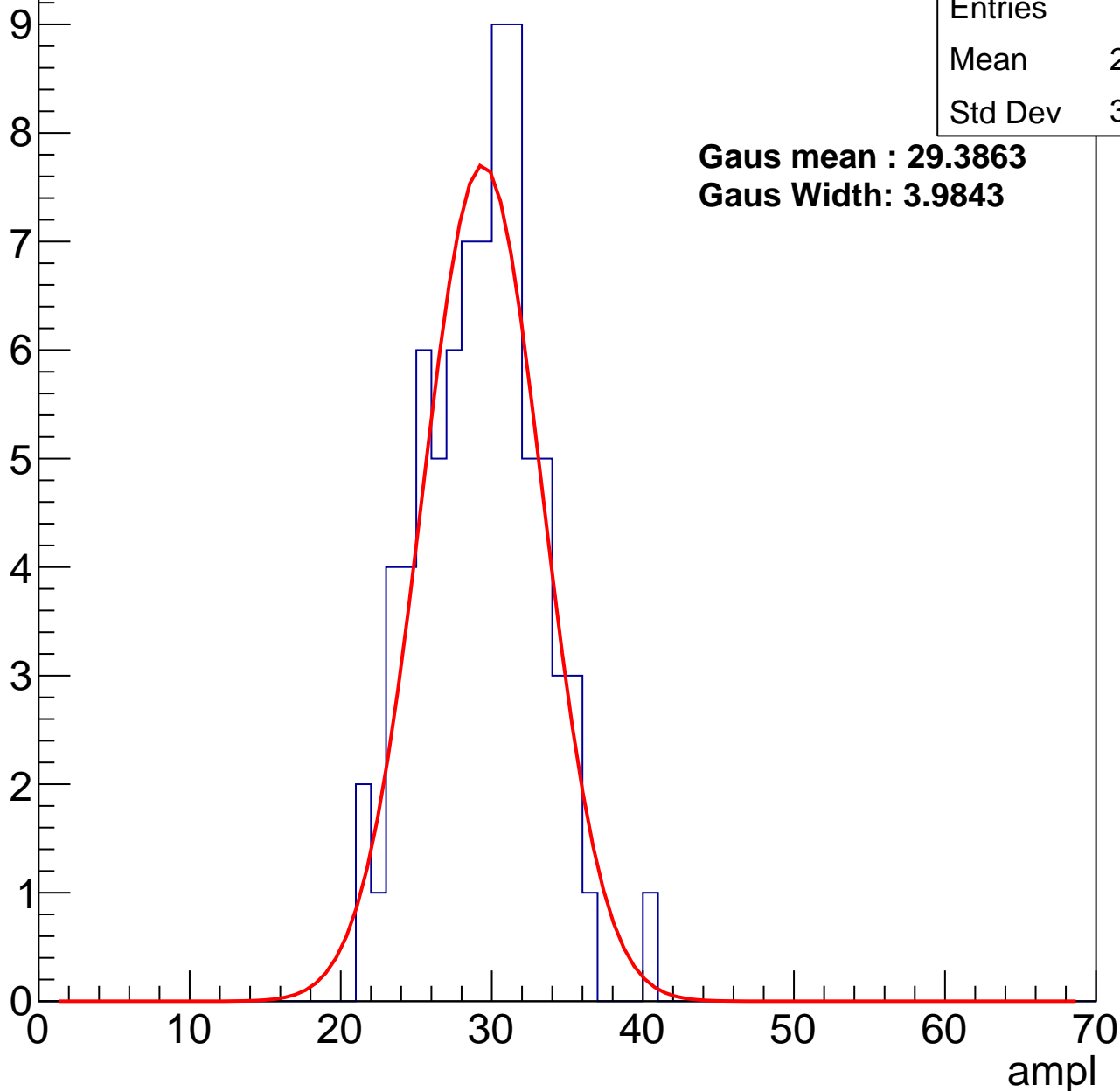
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	28.85
Std Dev	3.779

**Gaus mean : 29.3863**

**Gaus Width: 3.9843**



# B1L103S, U2-ch79, adc1

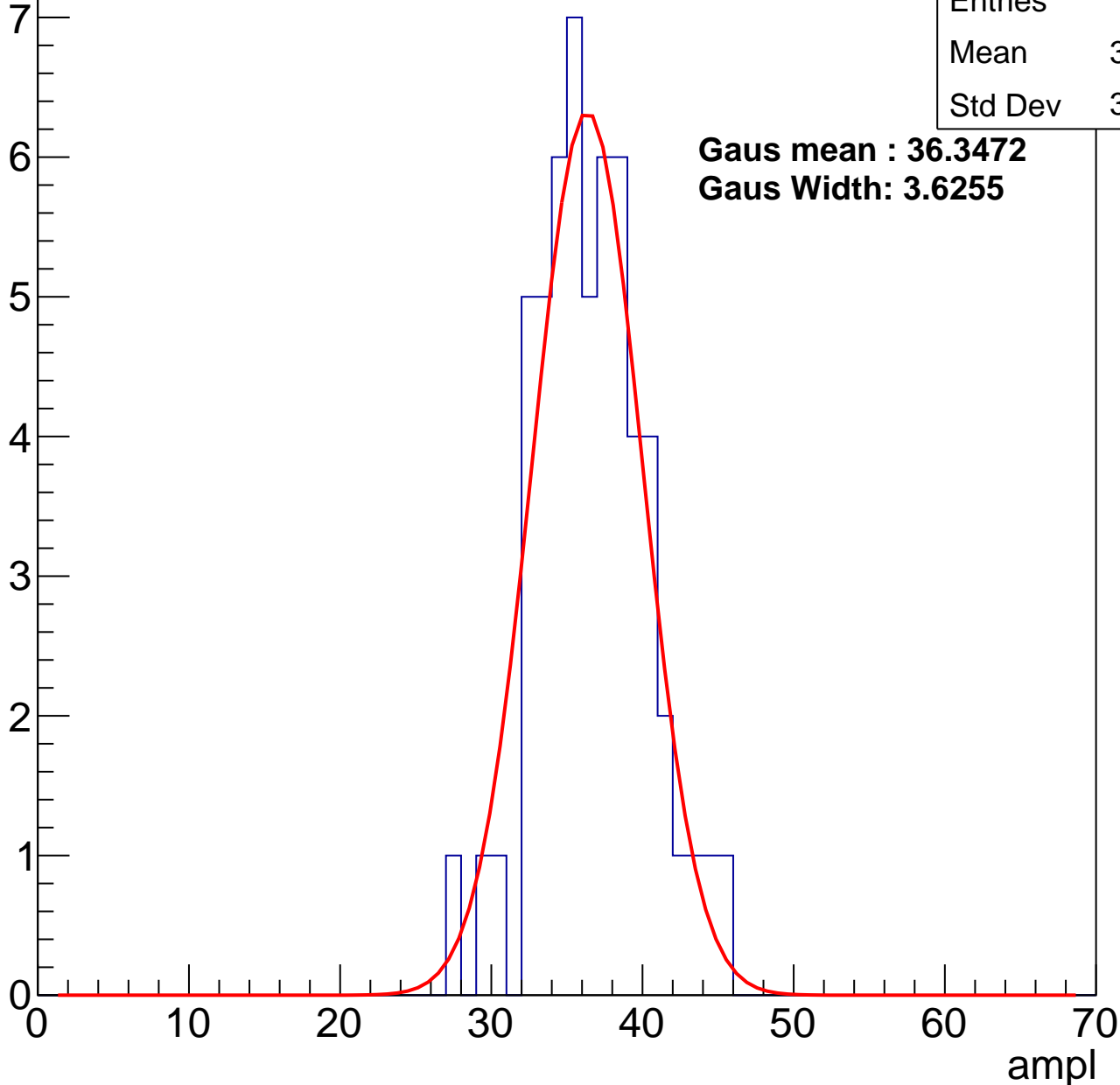
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	36.18
Std Dev	3.579

**Gaus mean : 36.3472**

**Gaus Width: 3.6255**

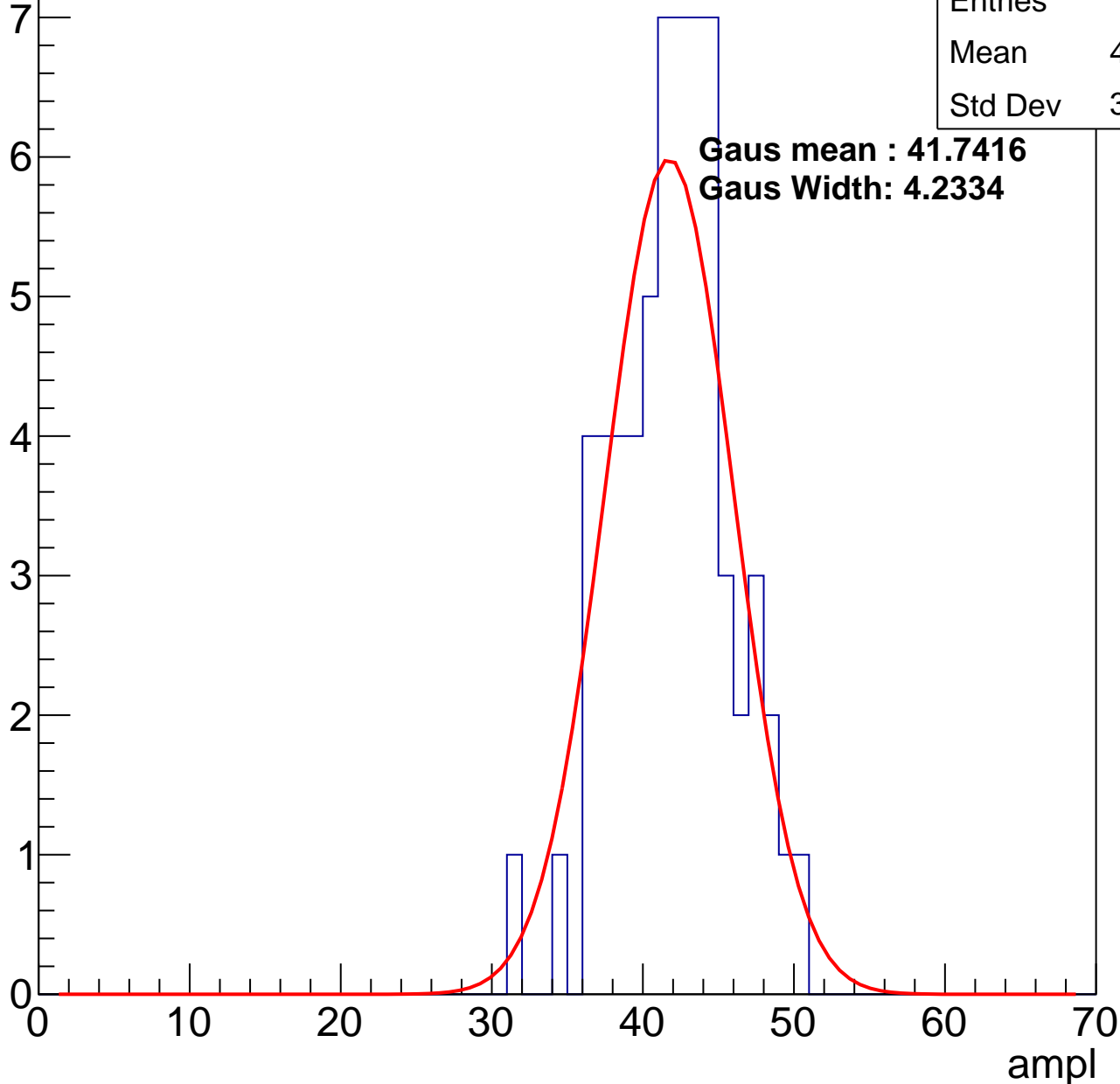


# B1L103S, U2-ch79, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	41.56
Std Dev	3.775

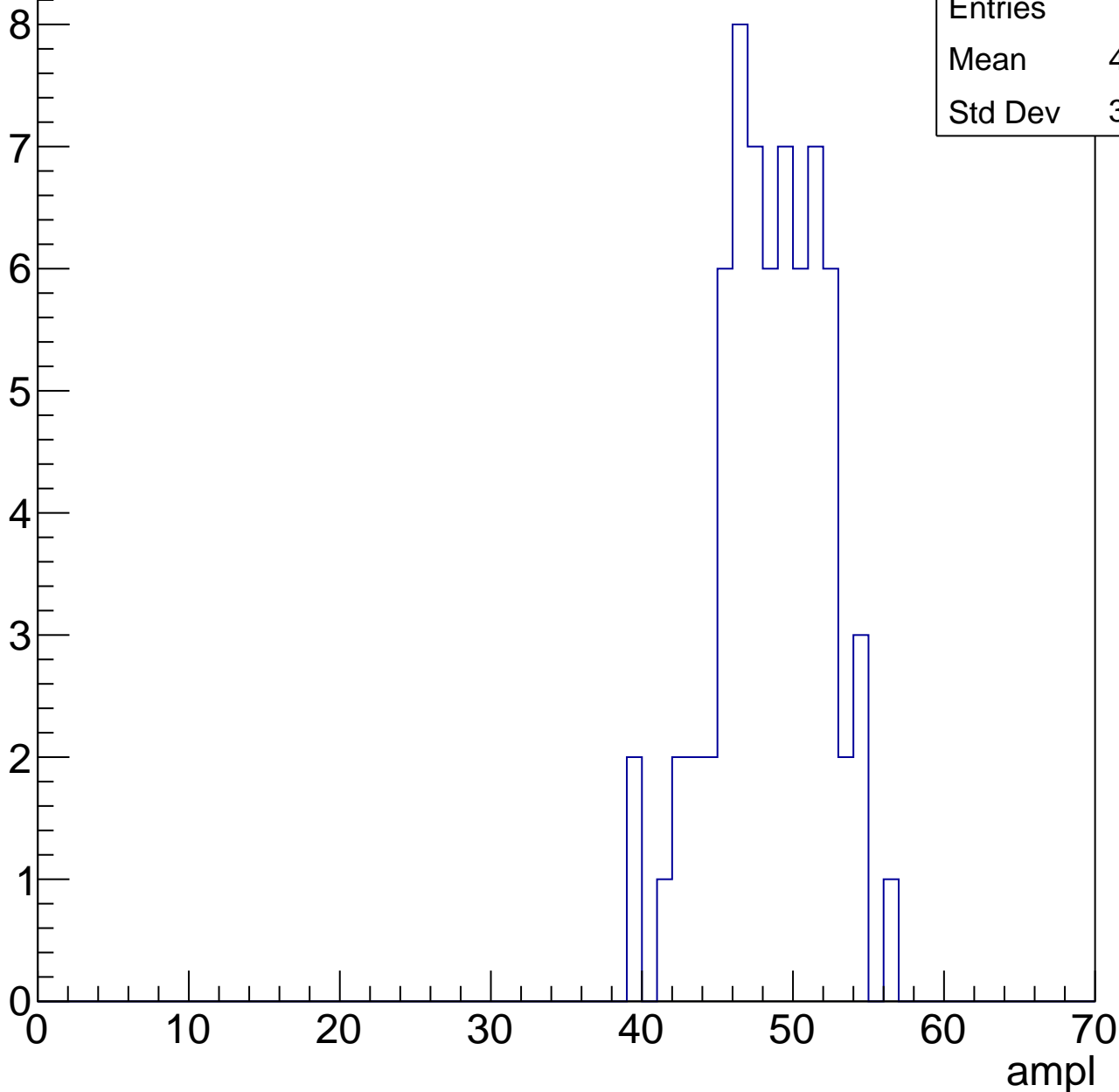


# B1L103S, U2-ch79, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	48.06
Std Dev	3.576

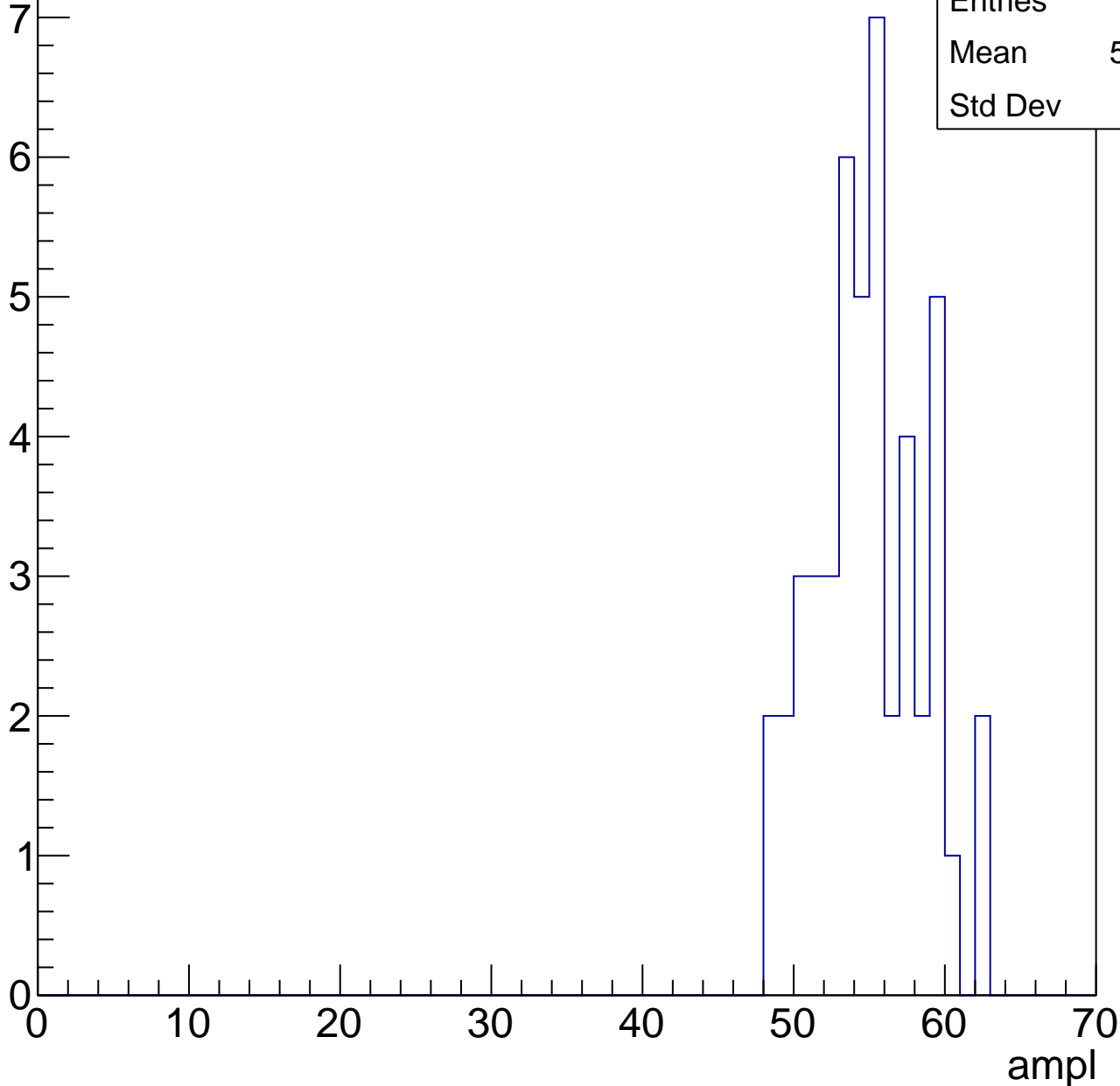


# B1L103S, U2-ch79, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

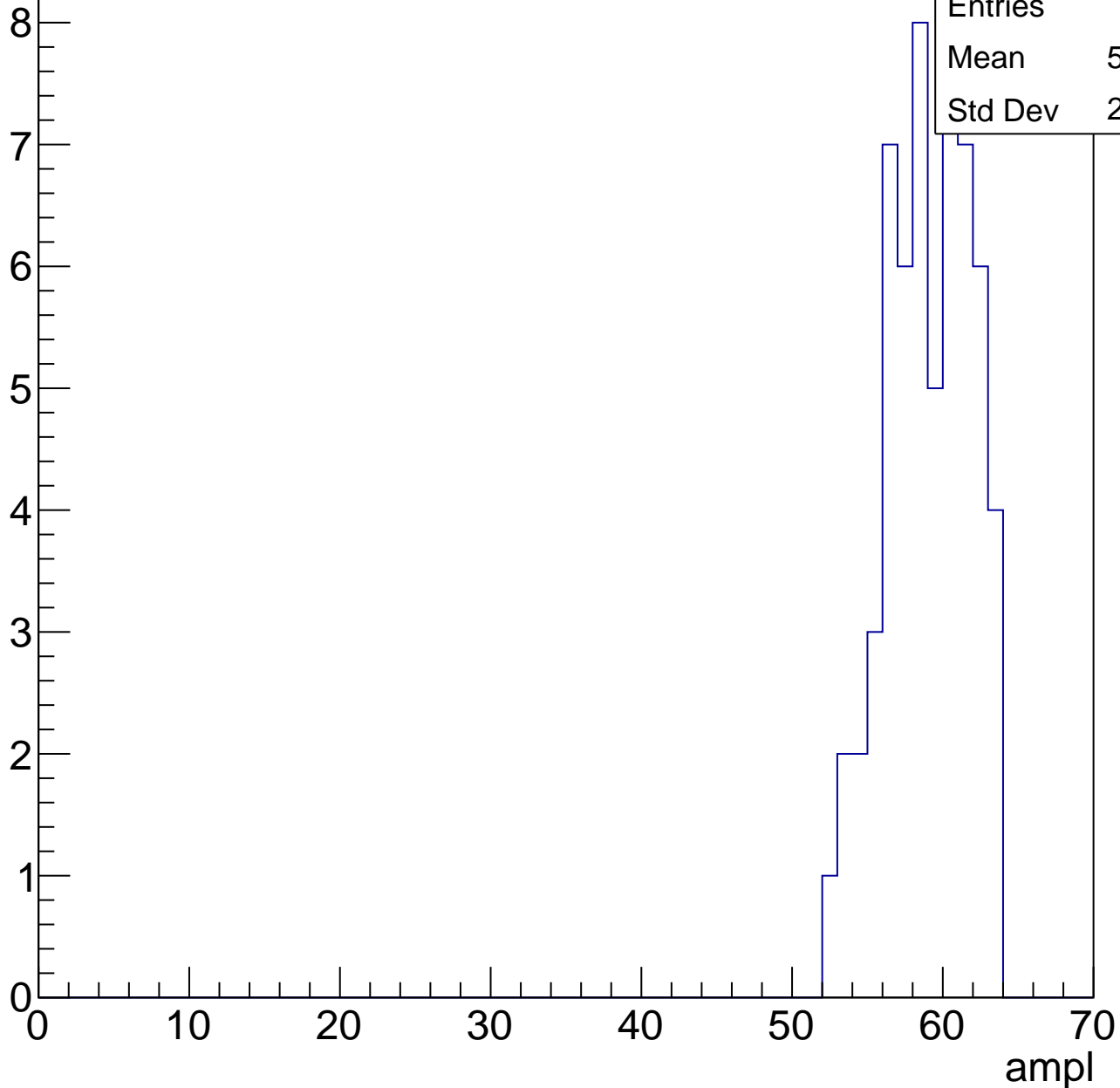
Entries	47
Mean	54.49
Std Dev	3.5



# B1L103S, U2-ch79, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



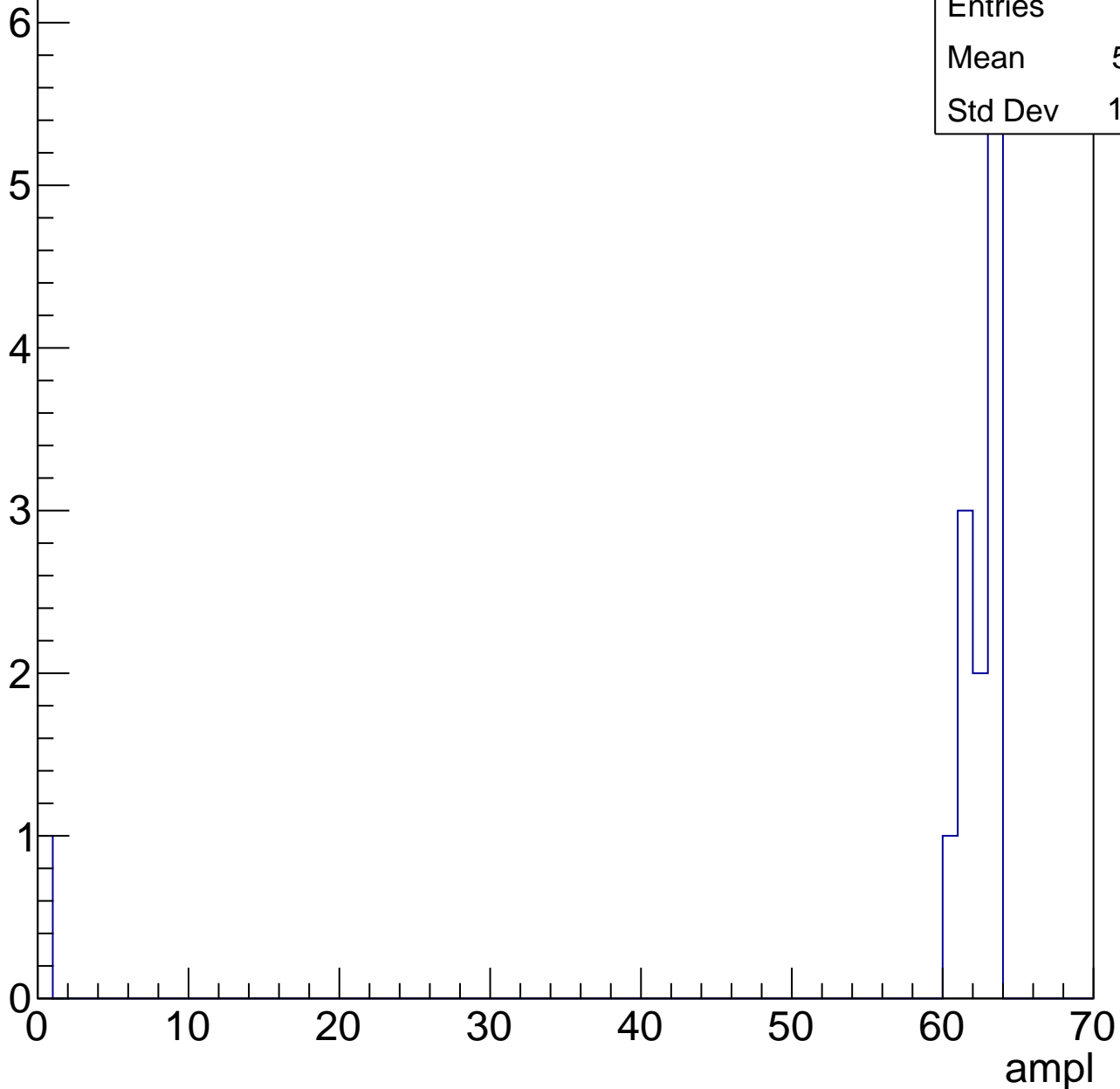
Entries	59
Mean	58.56
Std Dev	2.782

# B1L103S, U2-ch79, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	13
Mean	57.31
Std Dev	16.57





# B1L103S, U2-ch79, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch80, adc0

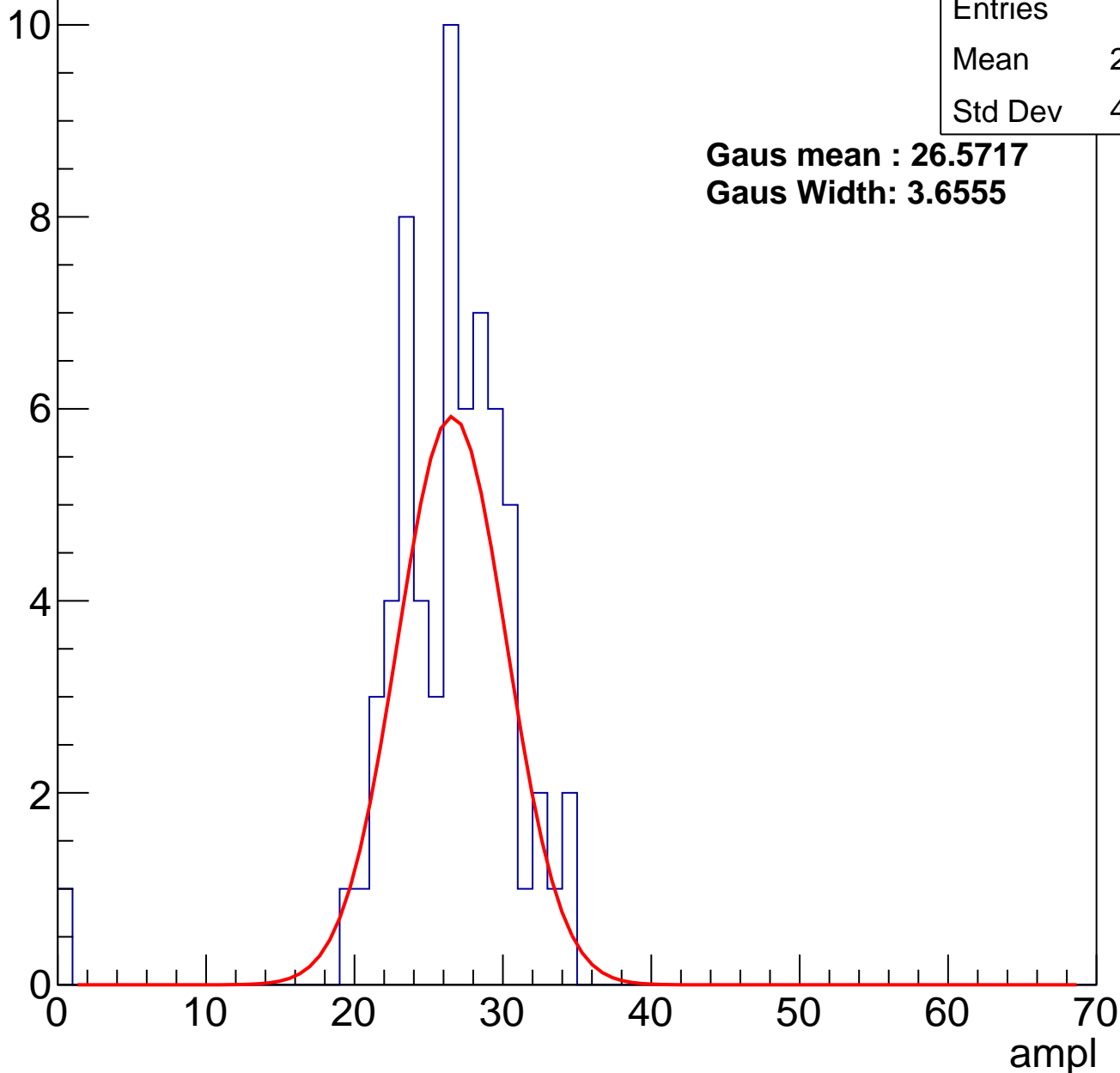
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	65
Mean	25.89
Std Dev	4.694

**Gaus mean : 26.5717**

**Gaus Width: 3.6555**

Entry



# B1L103S, U2-ch80, adc1

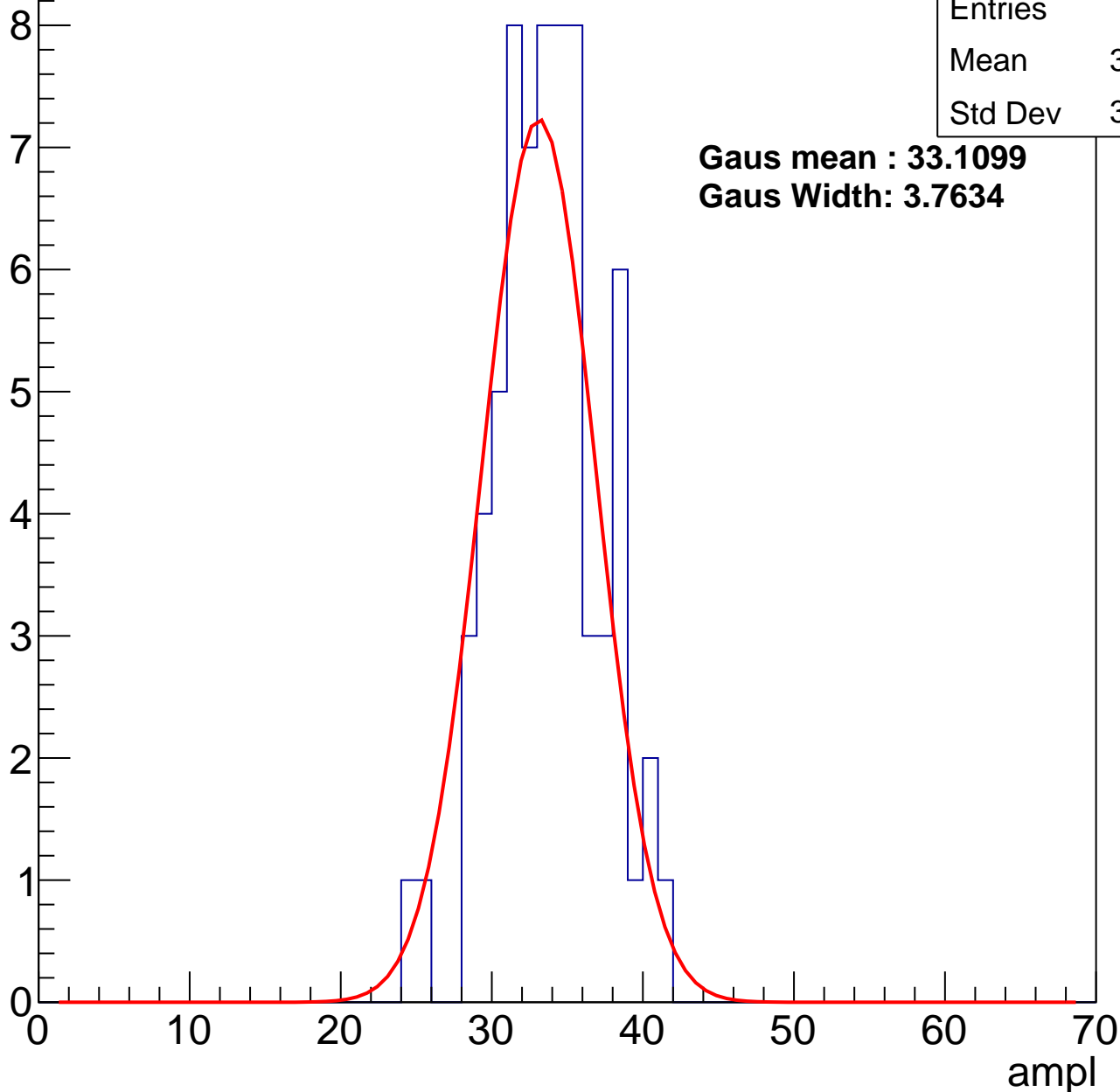
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	33.25
Std Dev	3.462

**Gaus mean : 33.1099**

**Gaus Width: 3.7634**



# B1L103S, U2-ch80, adc2

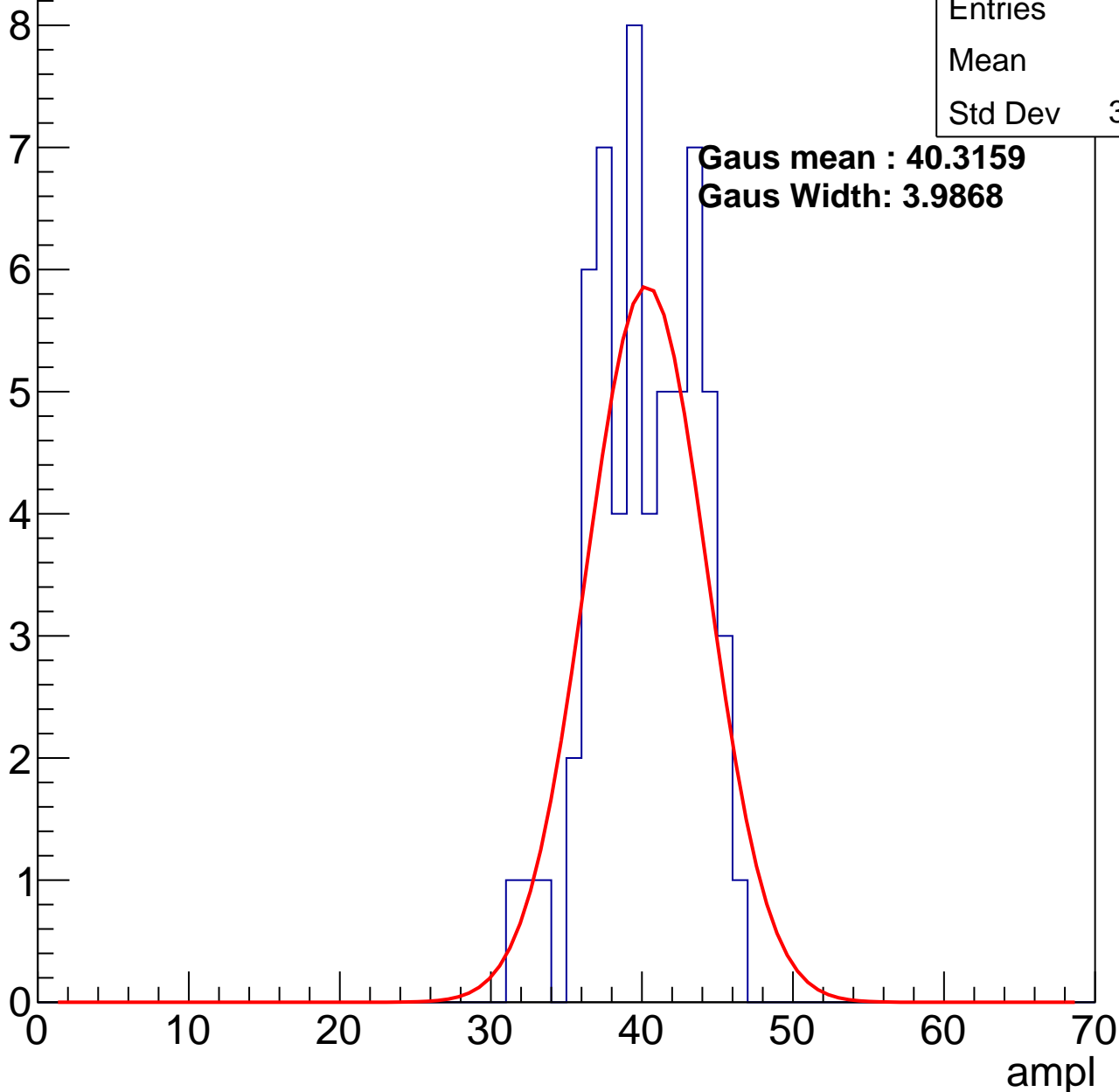
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	39.7
Std Dev	3.417

**Gaus mean : 40.3159**

**Gaus Width: 3.9868**

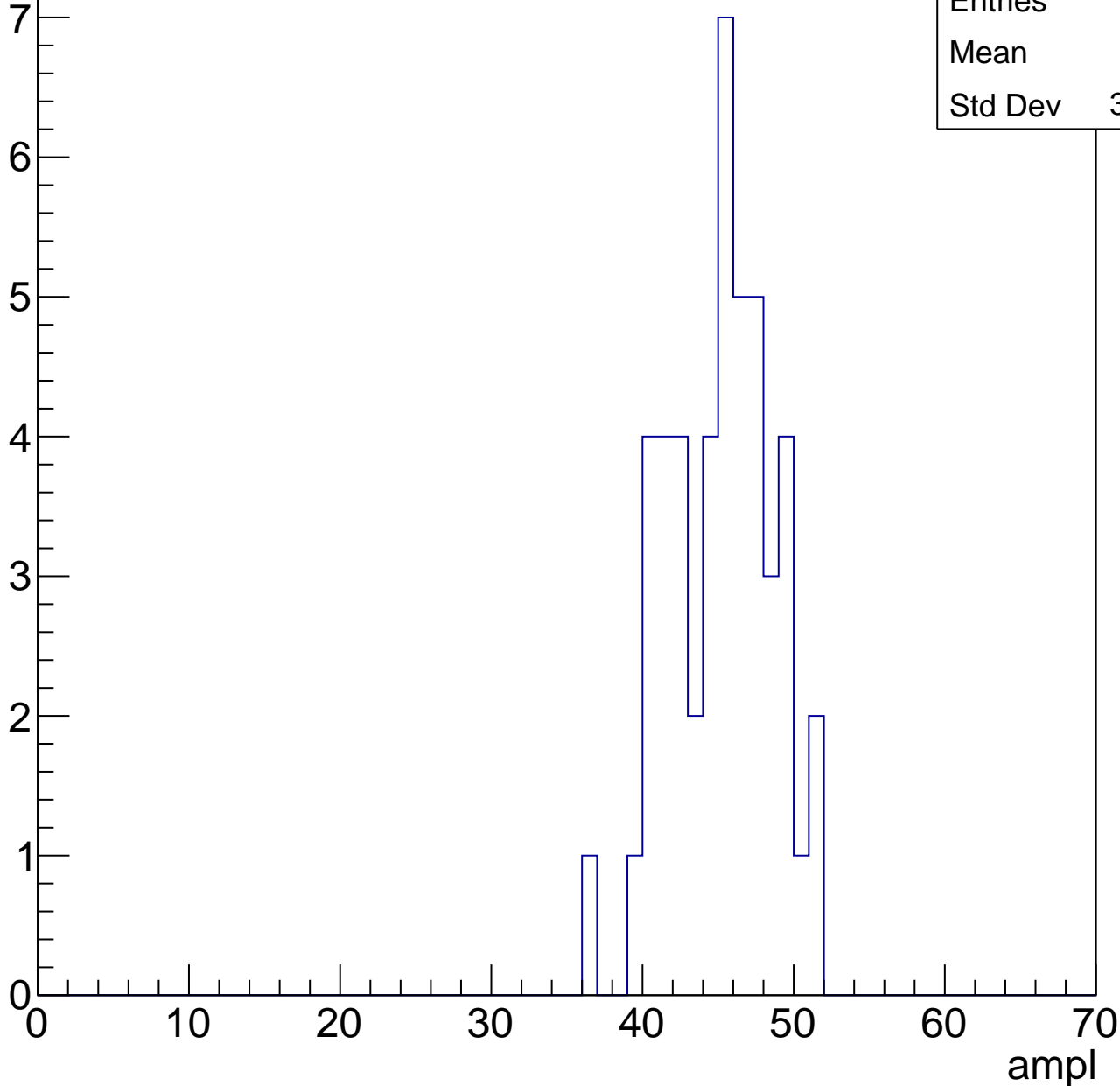


# B1L103S, U2-ch80, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	47
Mean	44.7
Std Dev	3.383

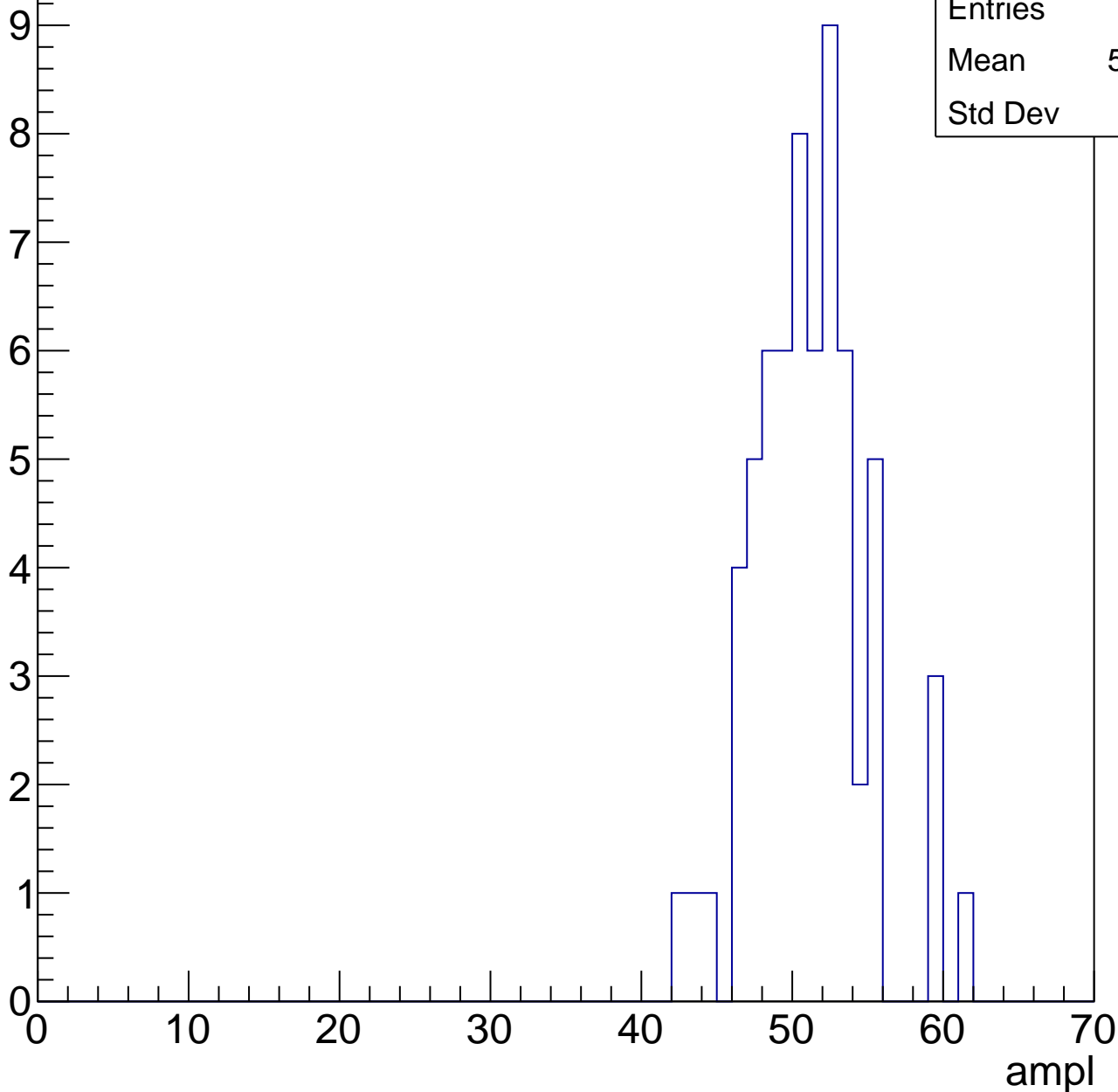


# B1L103S, U2-ch80, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	50.67
Std Dev	3.7

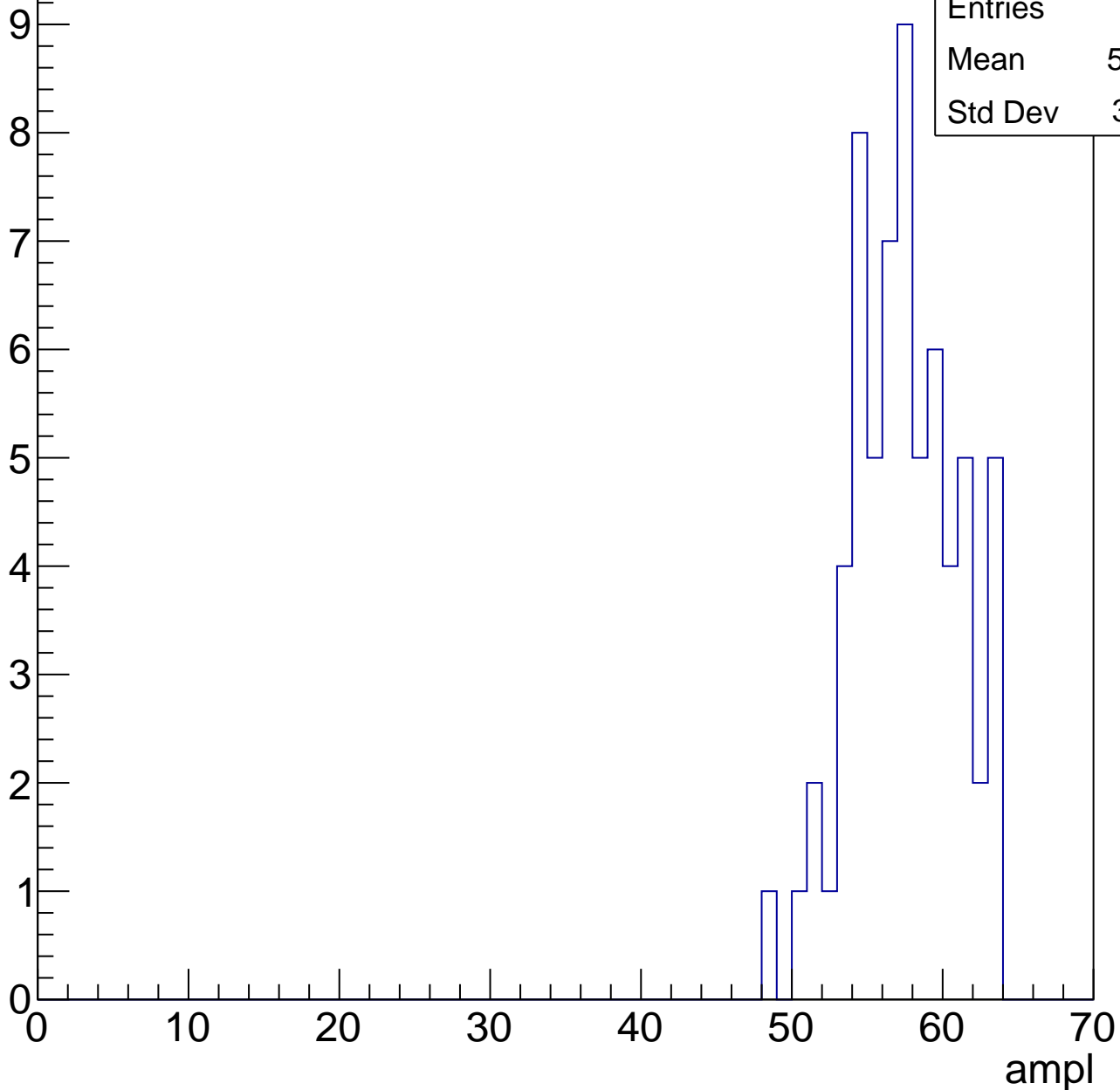


# B1L103S, U2-ch80, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	56.98
Std Dev	3.431

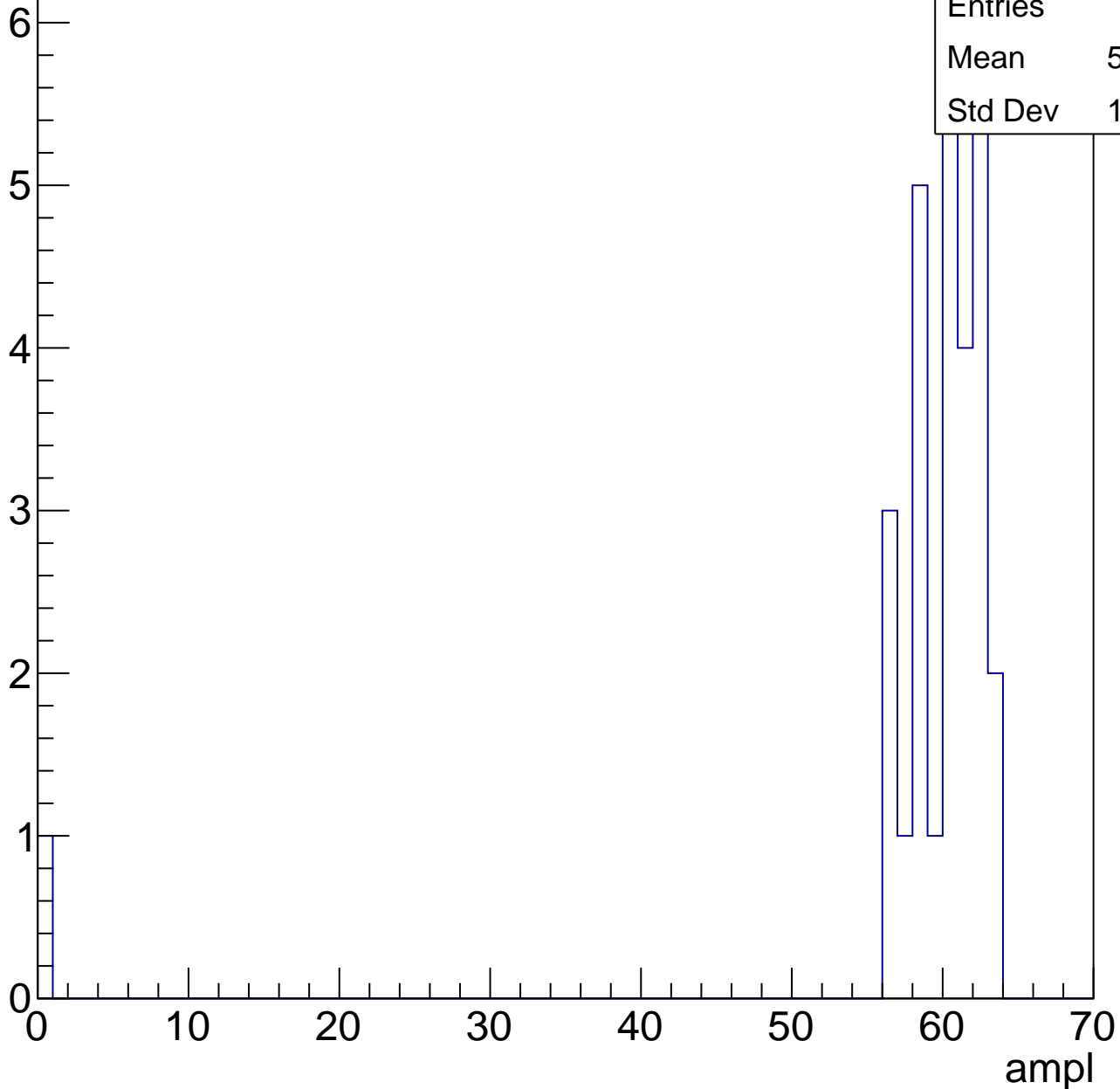


# B1L103S, U2-ch80, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	29
Mean	57.79
Std Dev	11.12

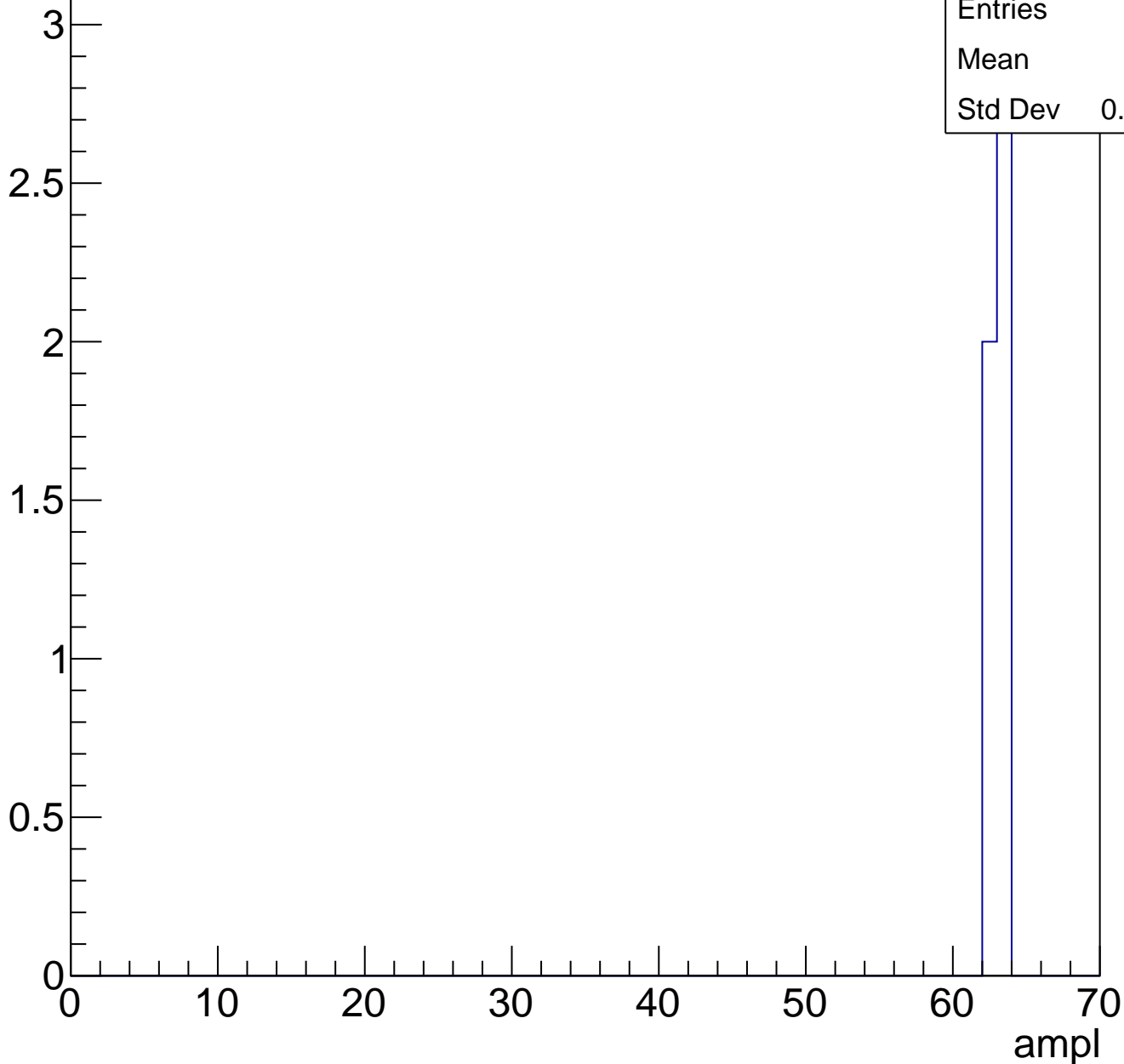




# B1L103S, U2-ch80, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch81, adc0

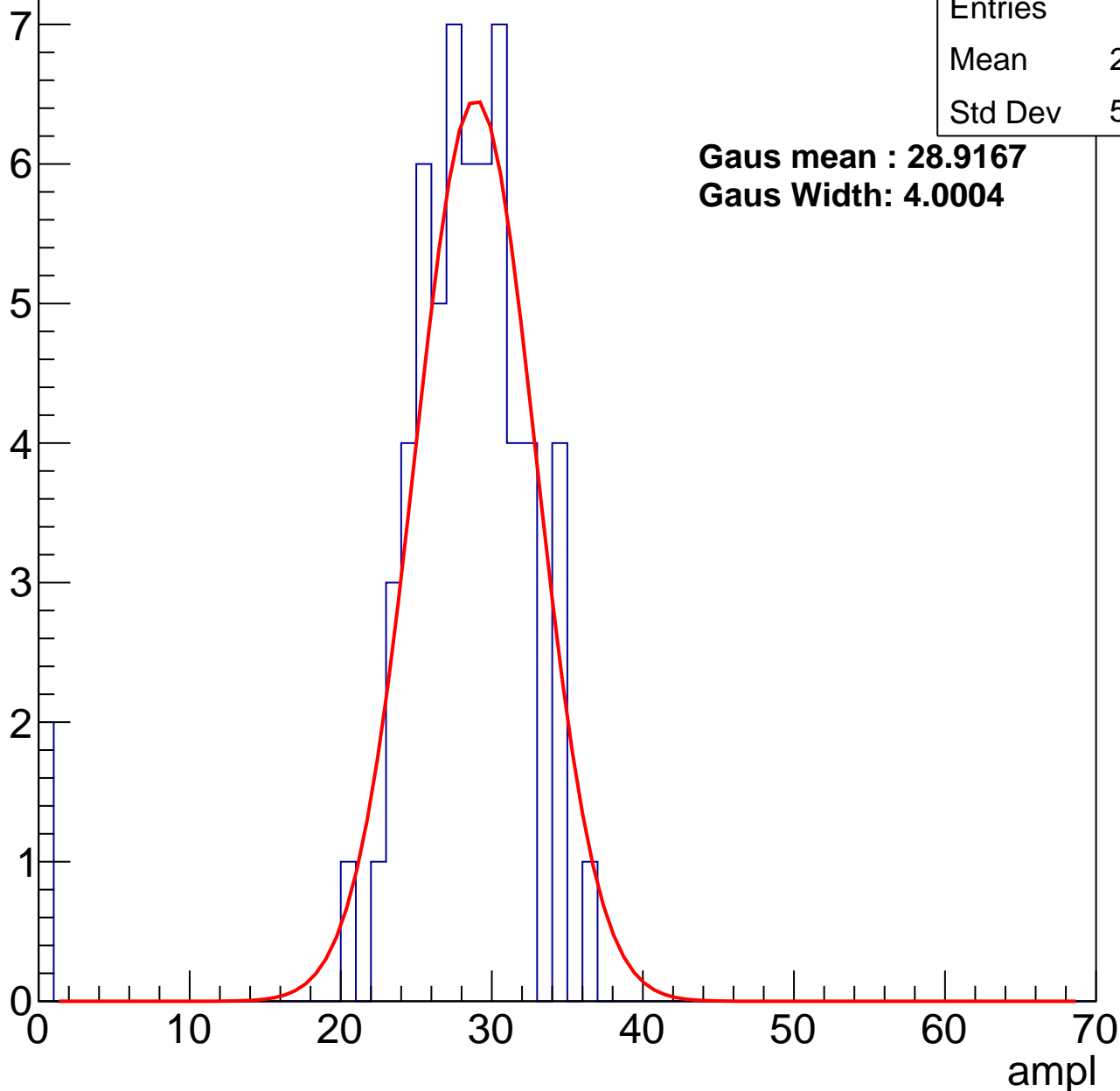
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	27.08
Std Dev	5.976

**Gaus mean : 28.9167**

**Gaus Width: 4.0004**



# B1L103S, U2-ch81, adc1

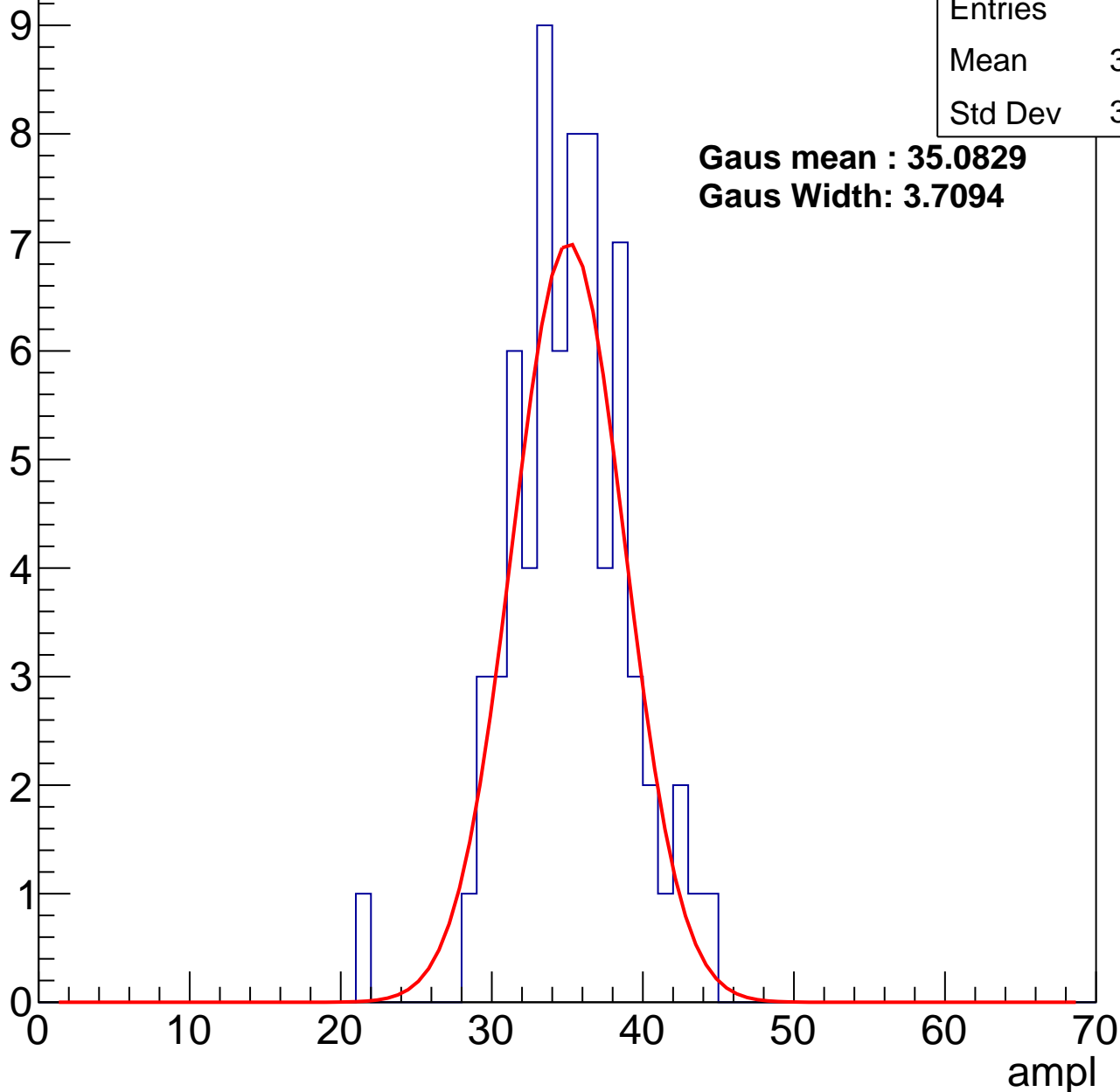
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	34.74
Std Dev	3.894

**Gaus mean : 35.0829**

**Gaus Width: 3.7094**



# B1L103S, U2-ch81, adc2

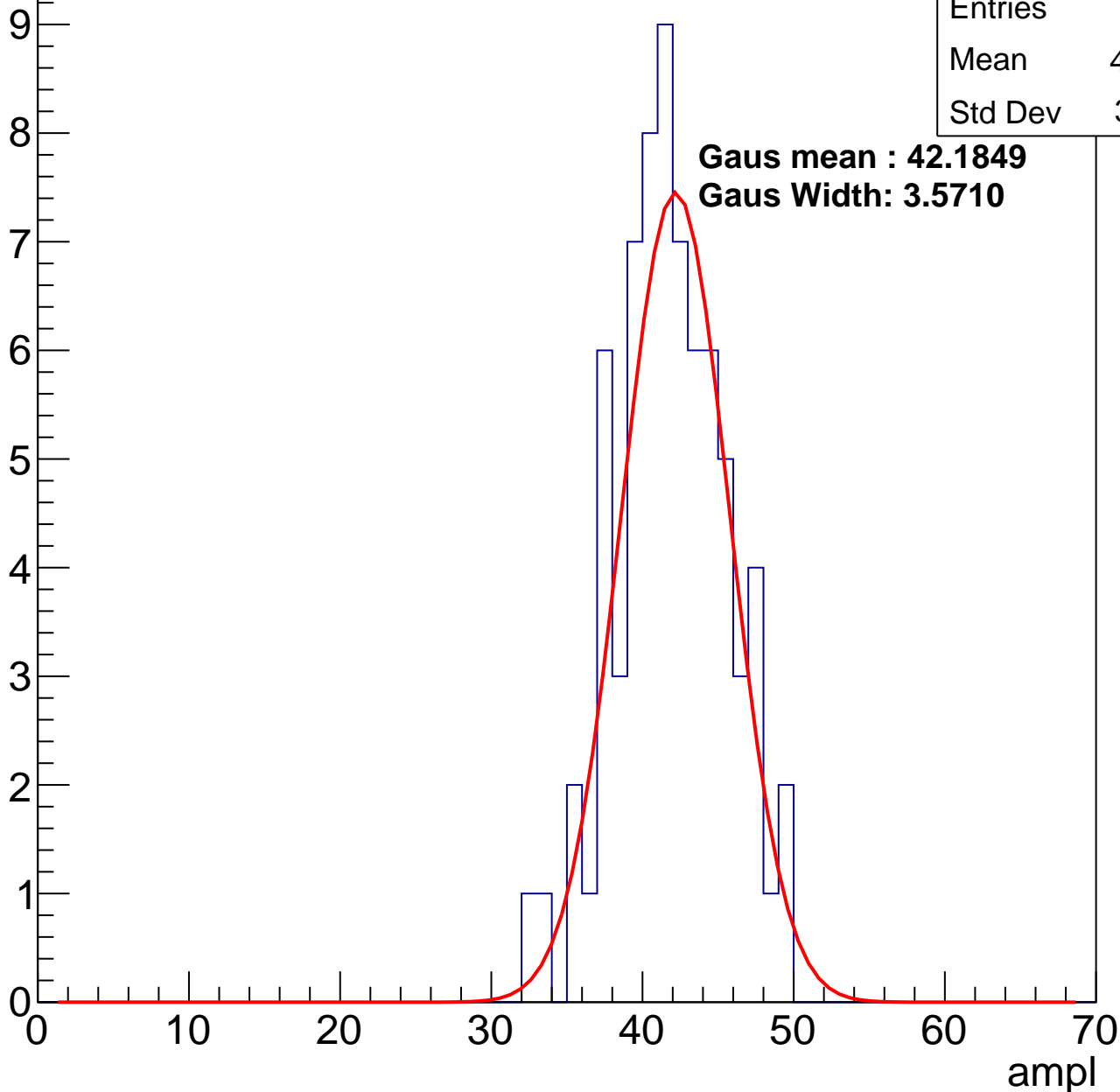
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	41.42
Std Dev	3.631

**Gaus mean : 42.1849**

**Gaus Width: 3.5710**

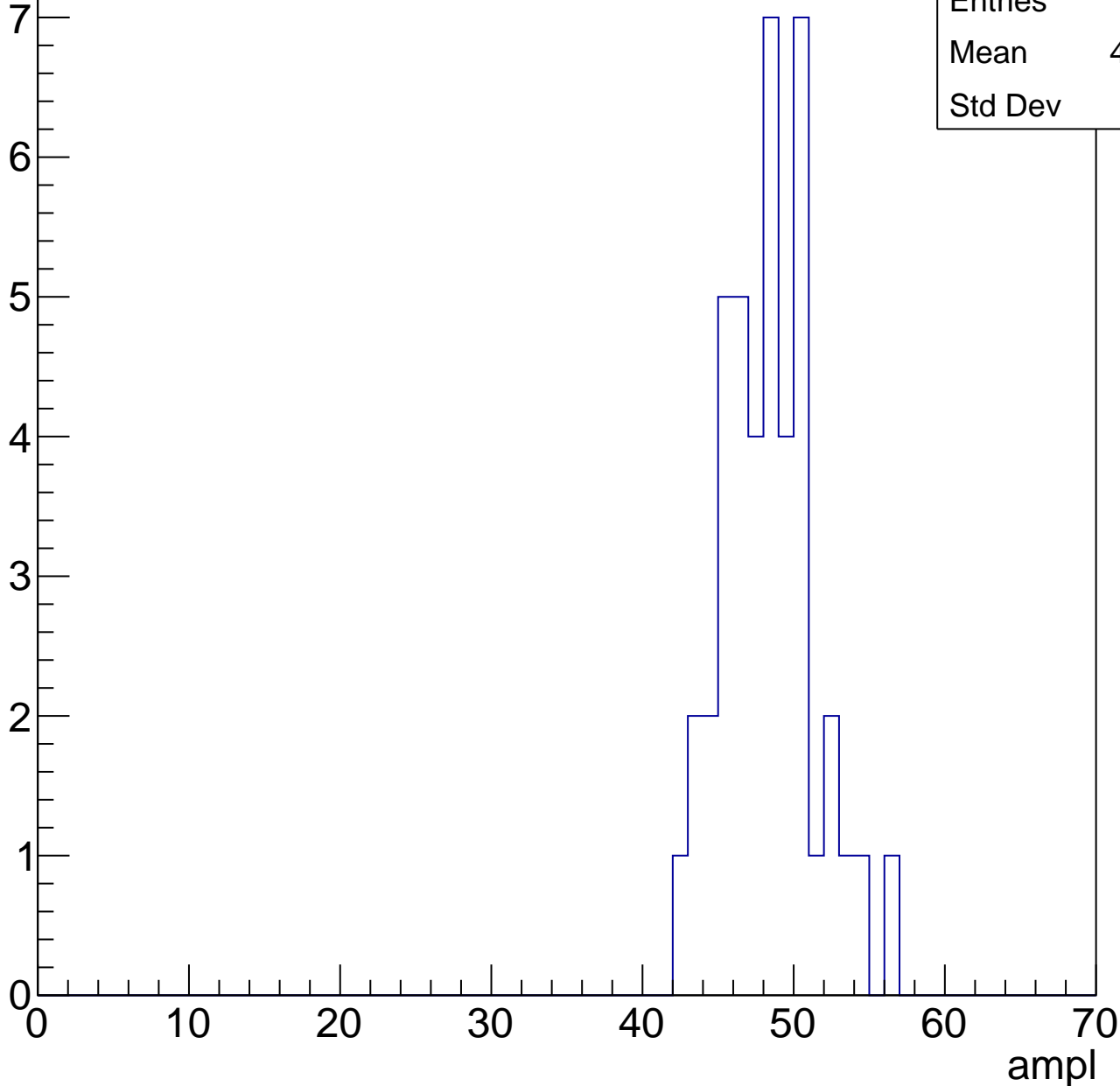


# B1L103S, U2-ch81, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

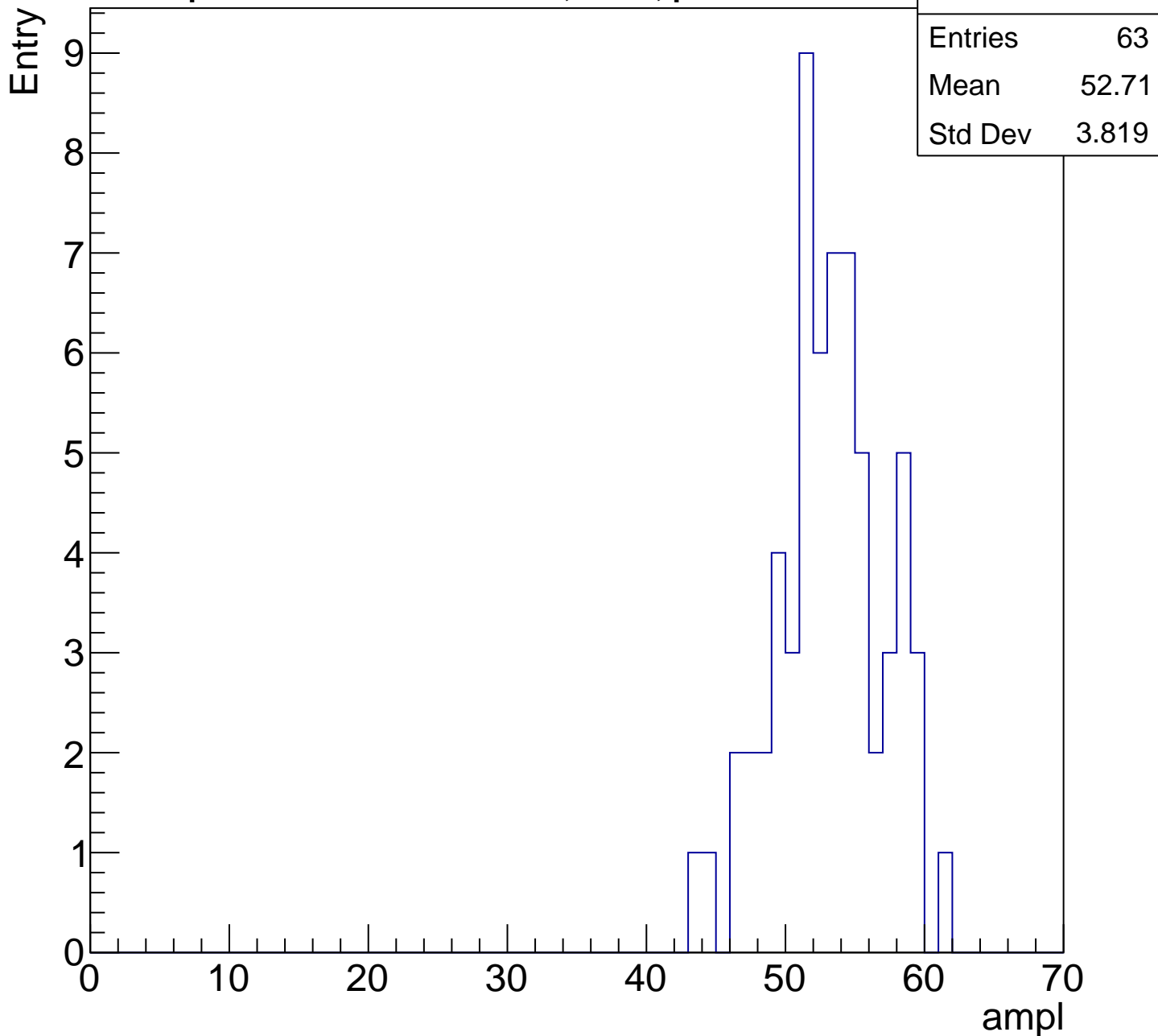
Entry

Entries	43
Mean	47.88
Std Dev	2.99



# B1L103S, U2-ch81, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

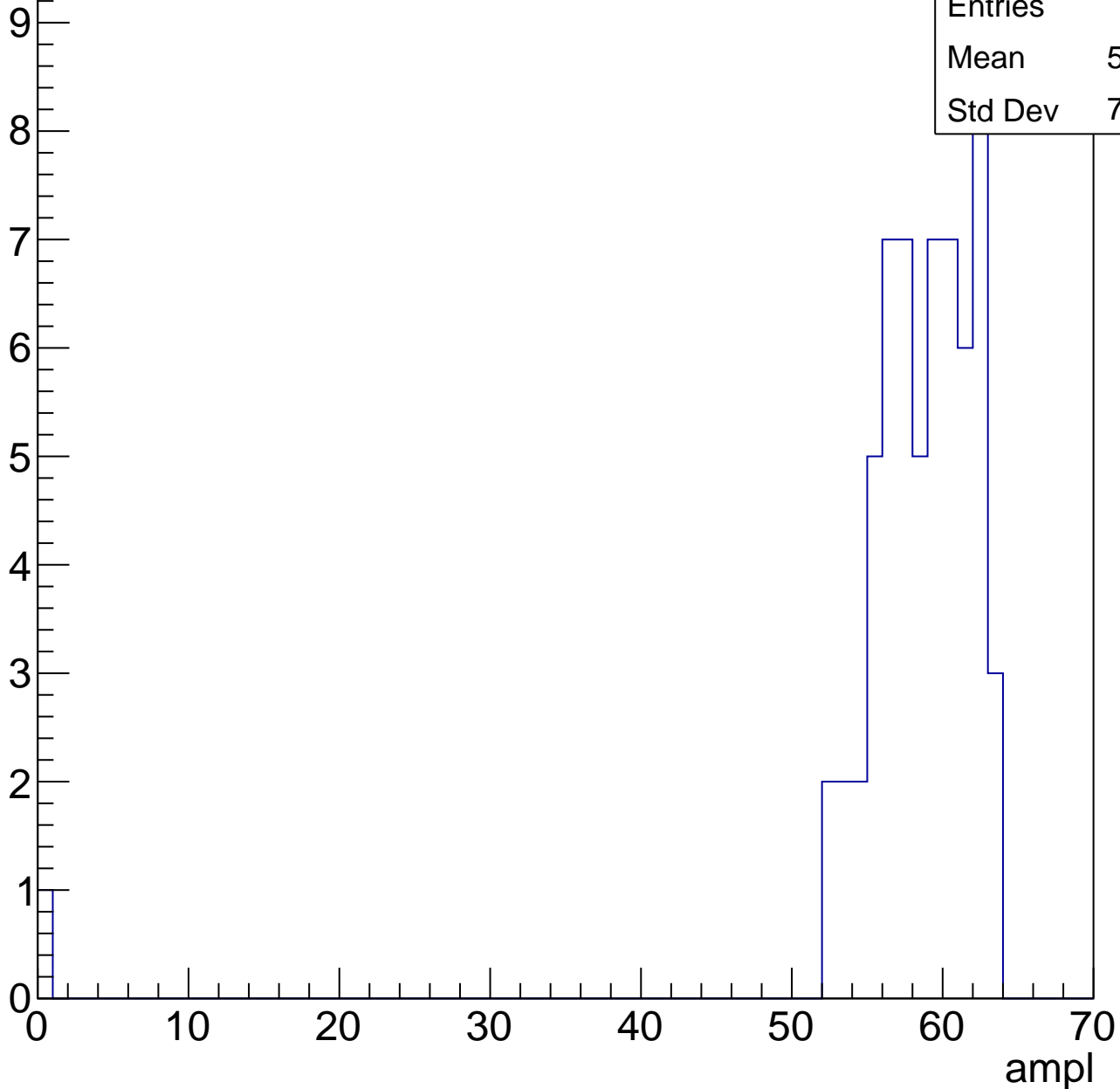


# B1L103S, U2-ch81, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

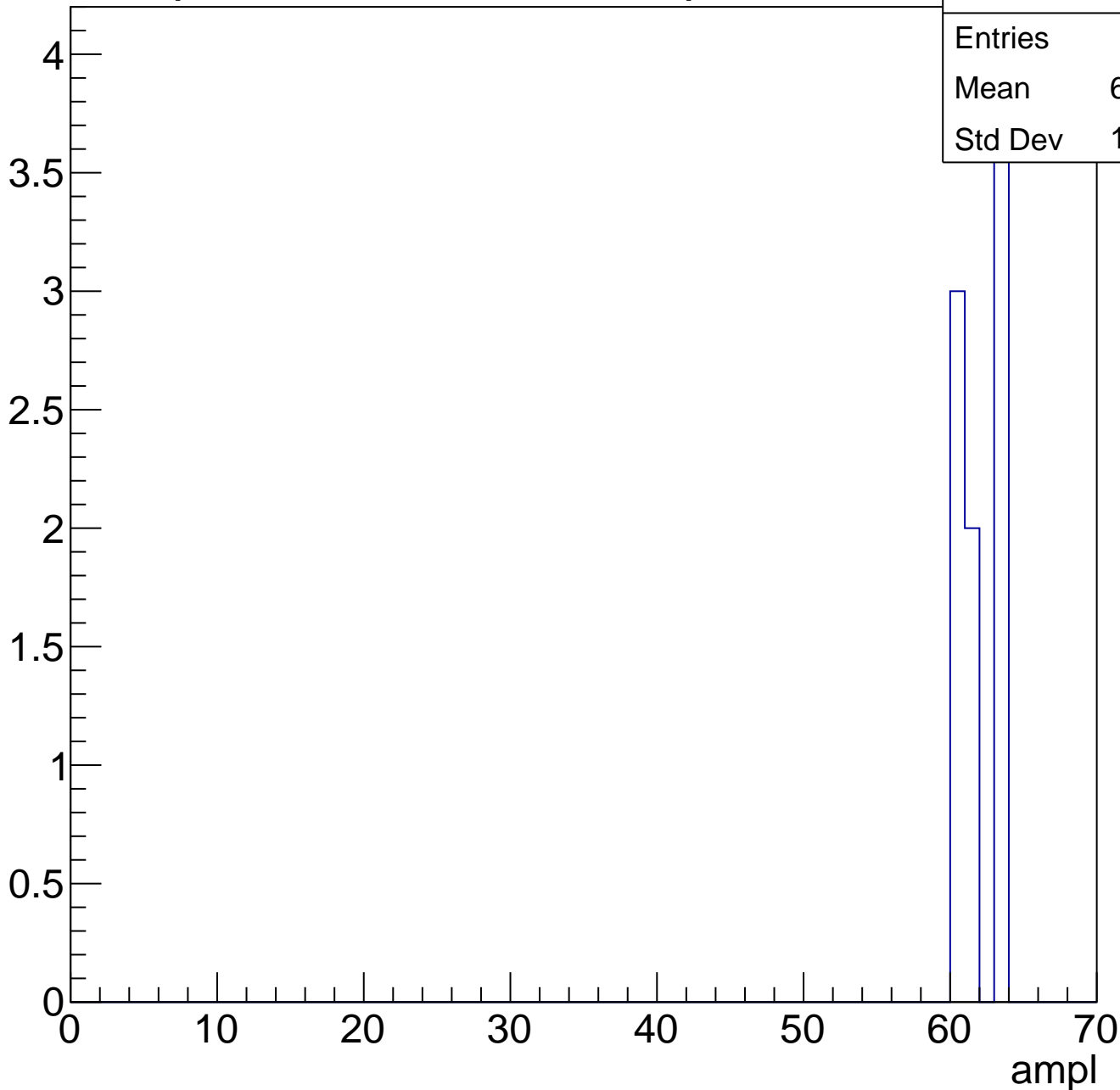
Entries	63
Mean	57.46
Std Dev	7.855



# B1L103S, U2-ch81, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

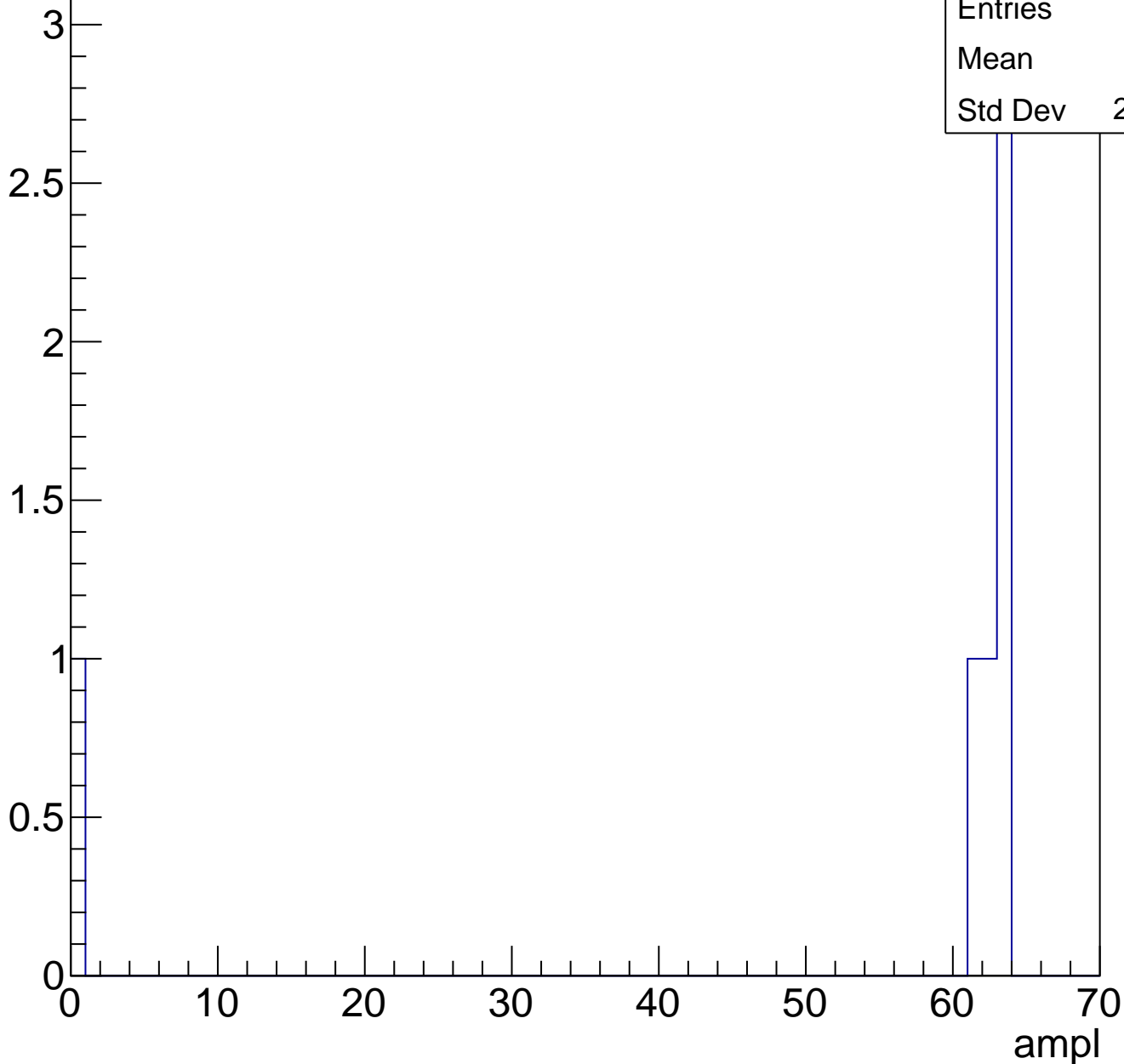




# B1L103S, U2-ch81, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch82, adc0

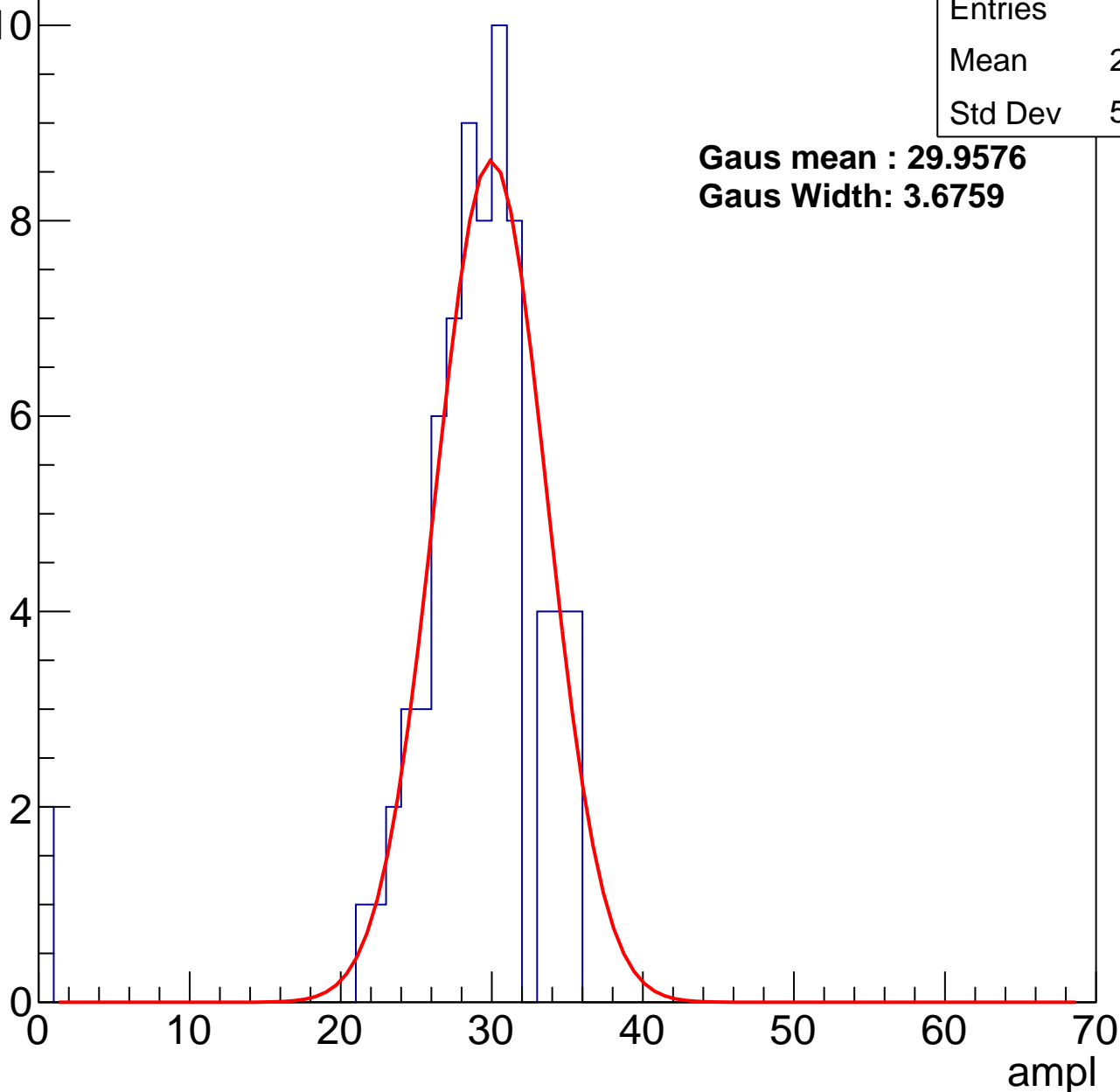
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	28.07
Std Dev	5.736

**Gaus mean : 29.9576**

**Gaus Width: 3.6759**



# B1L103S, U2-ch82, adc1

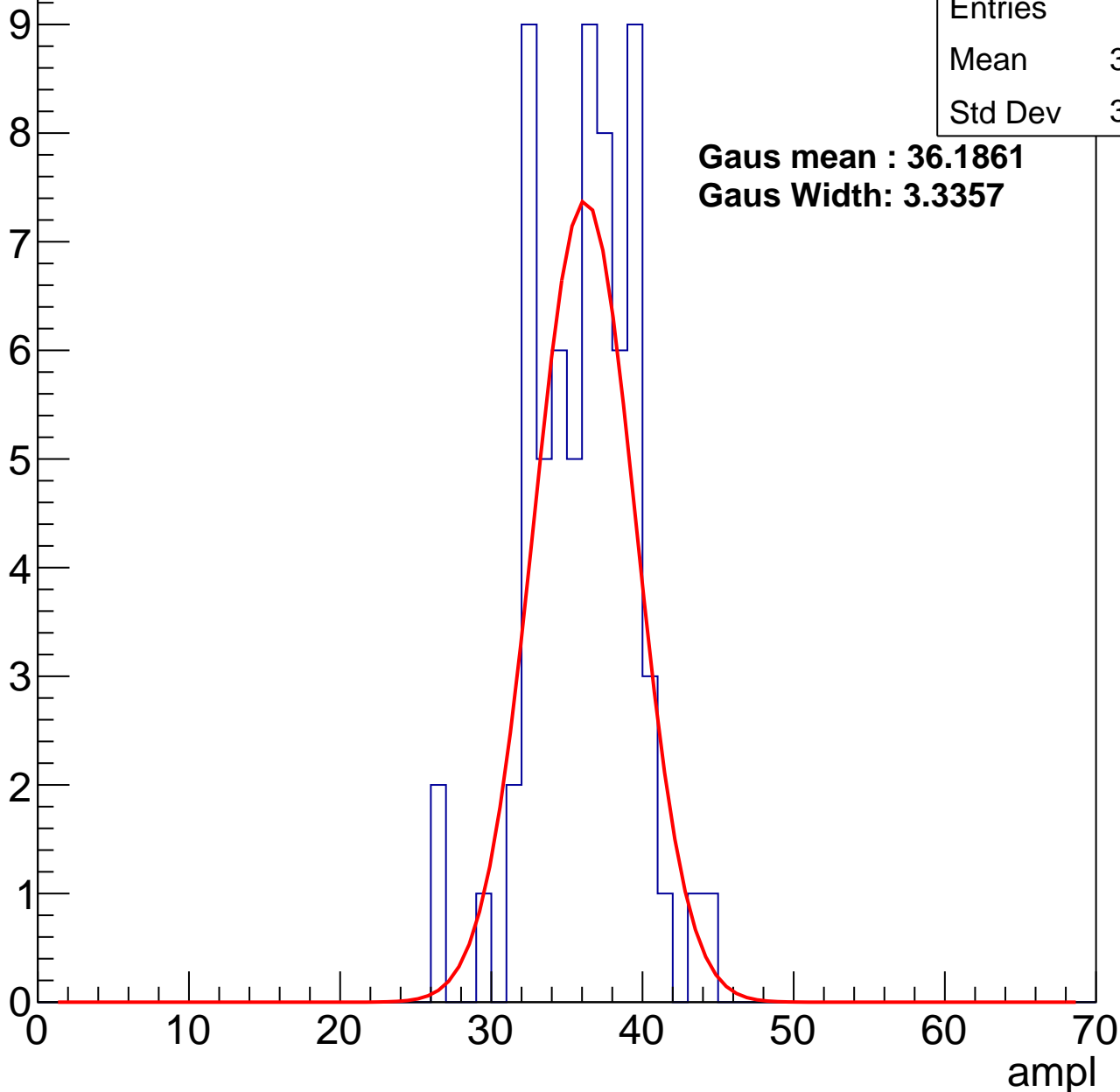
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	35.62
Std Dev	3.443

**Gaus mean : 36.1861**

**Gaus Width: 3.3357**



# B1L103S, U2-ch82, adc2

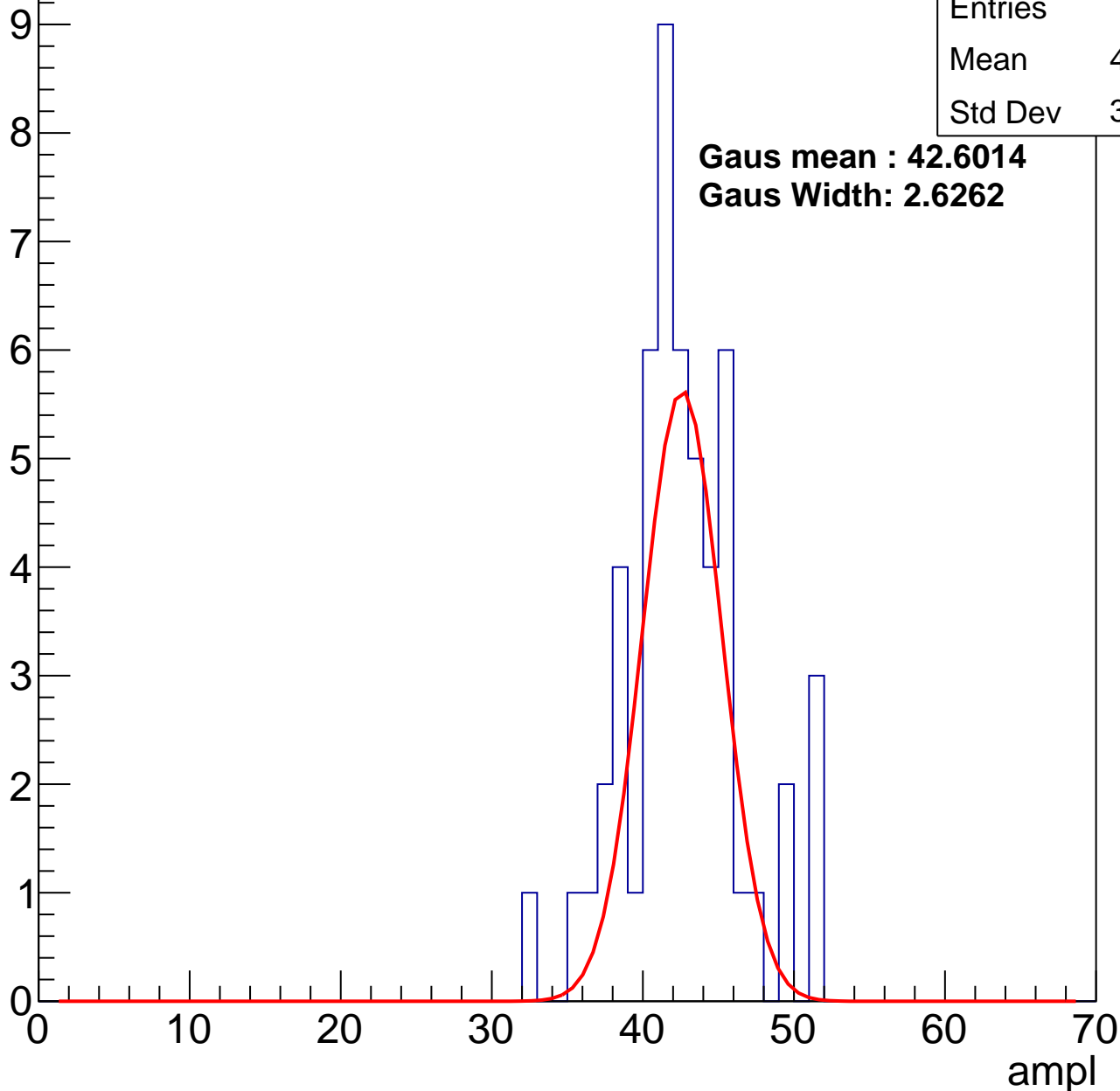
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	42.15
Std Dev	3.877

**Gaus mean : 42.6014**

**Gaus Width: 2.6262**

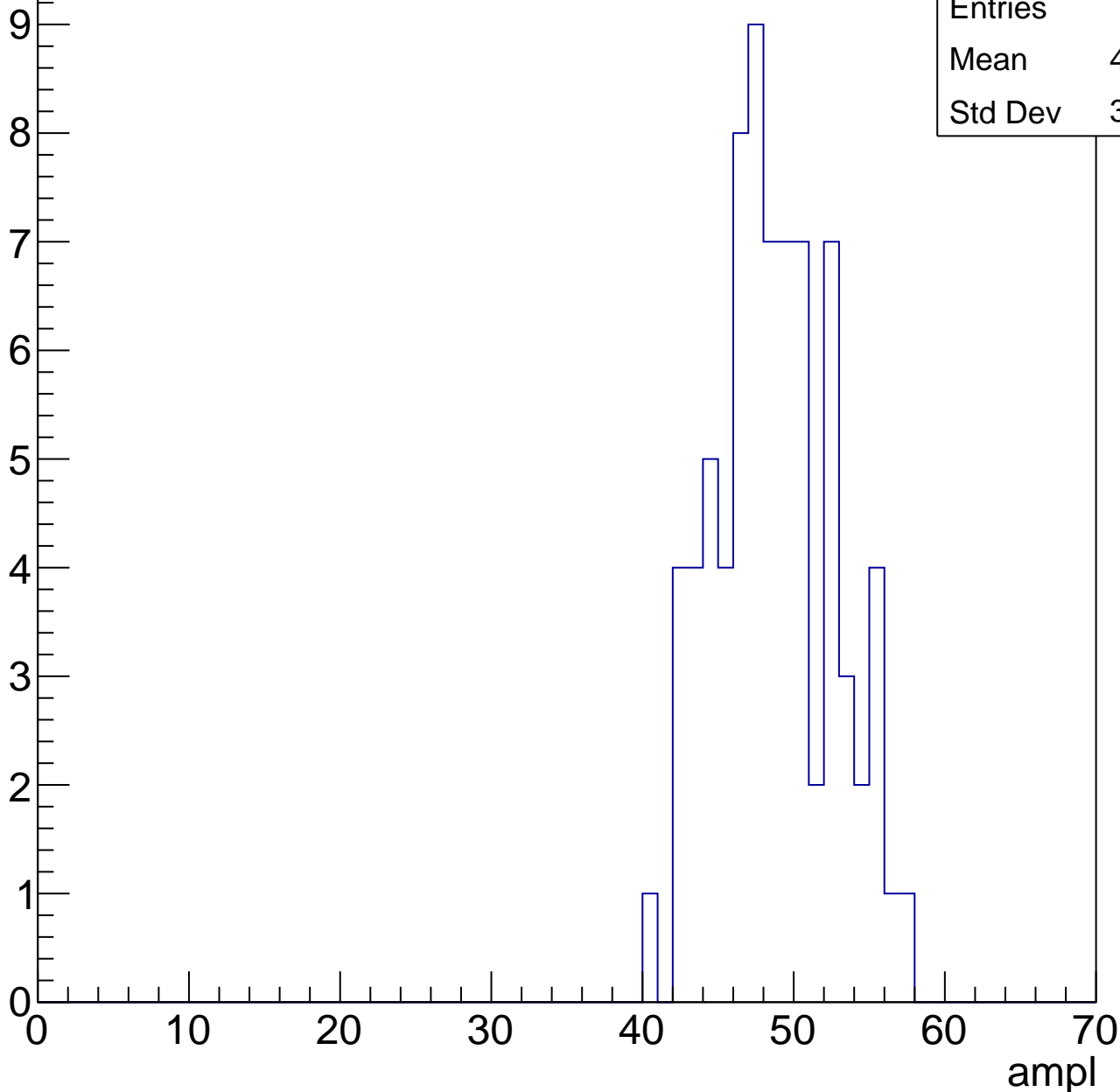


# B1L103S, U2-ch82, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	48.24
Std Dev	3.828

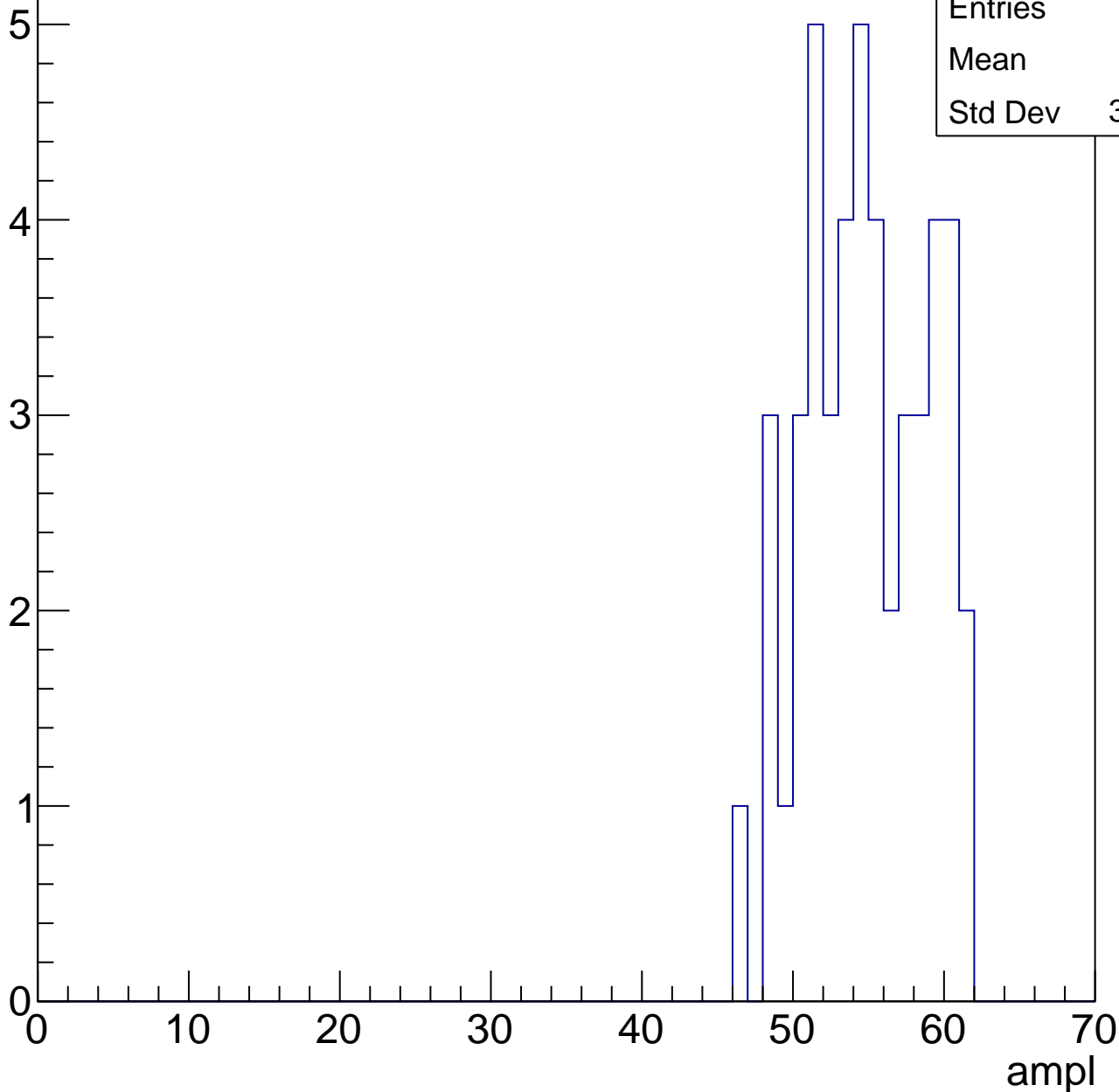


# B1L103S, U2-ch82, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	47
Mean	54.4
Std Dev	3.934

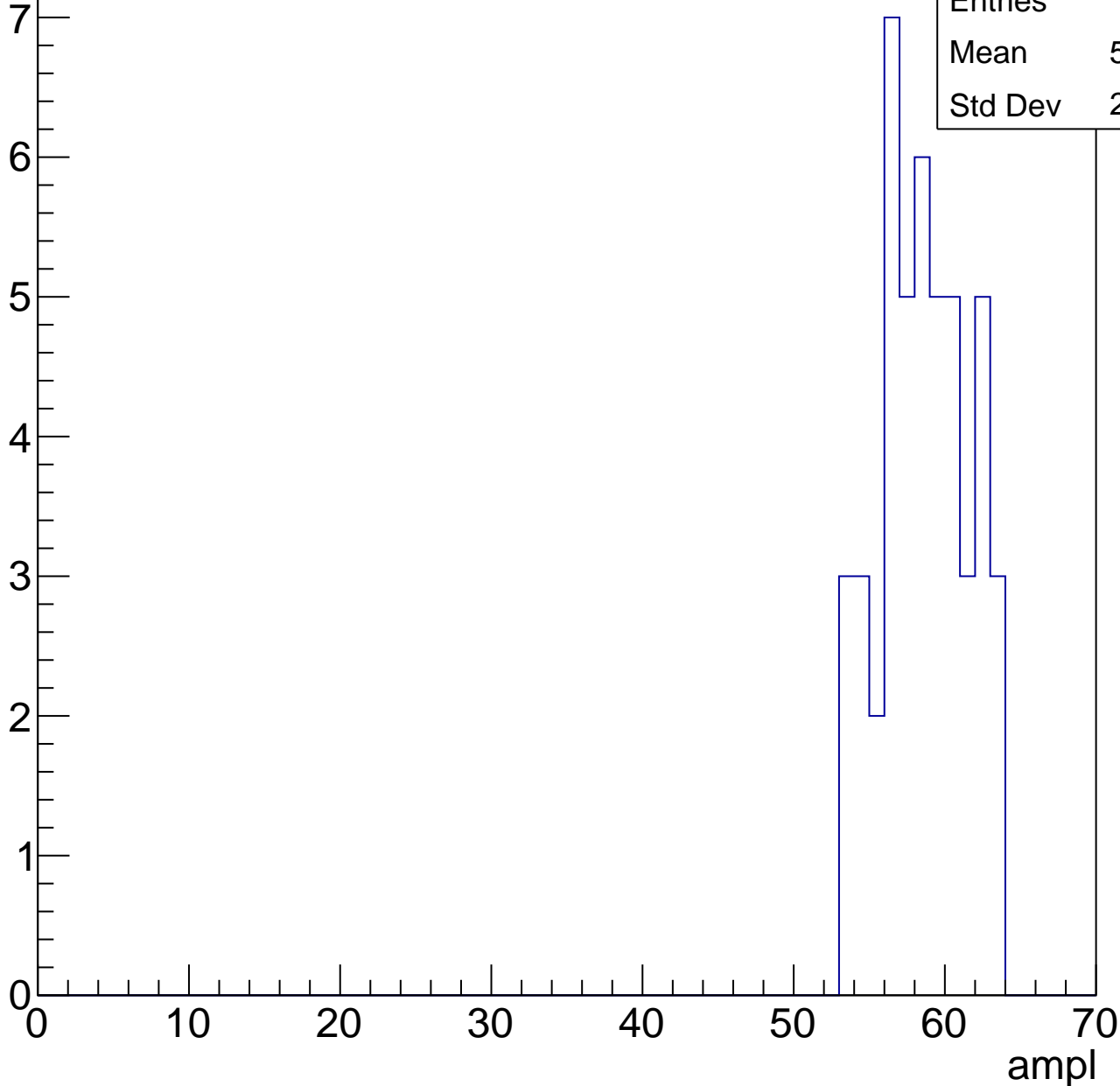


# B1L103S, U2-ch82, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	47
Mean	58.15
Std Dev	2.843

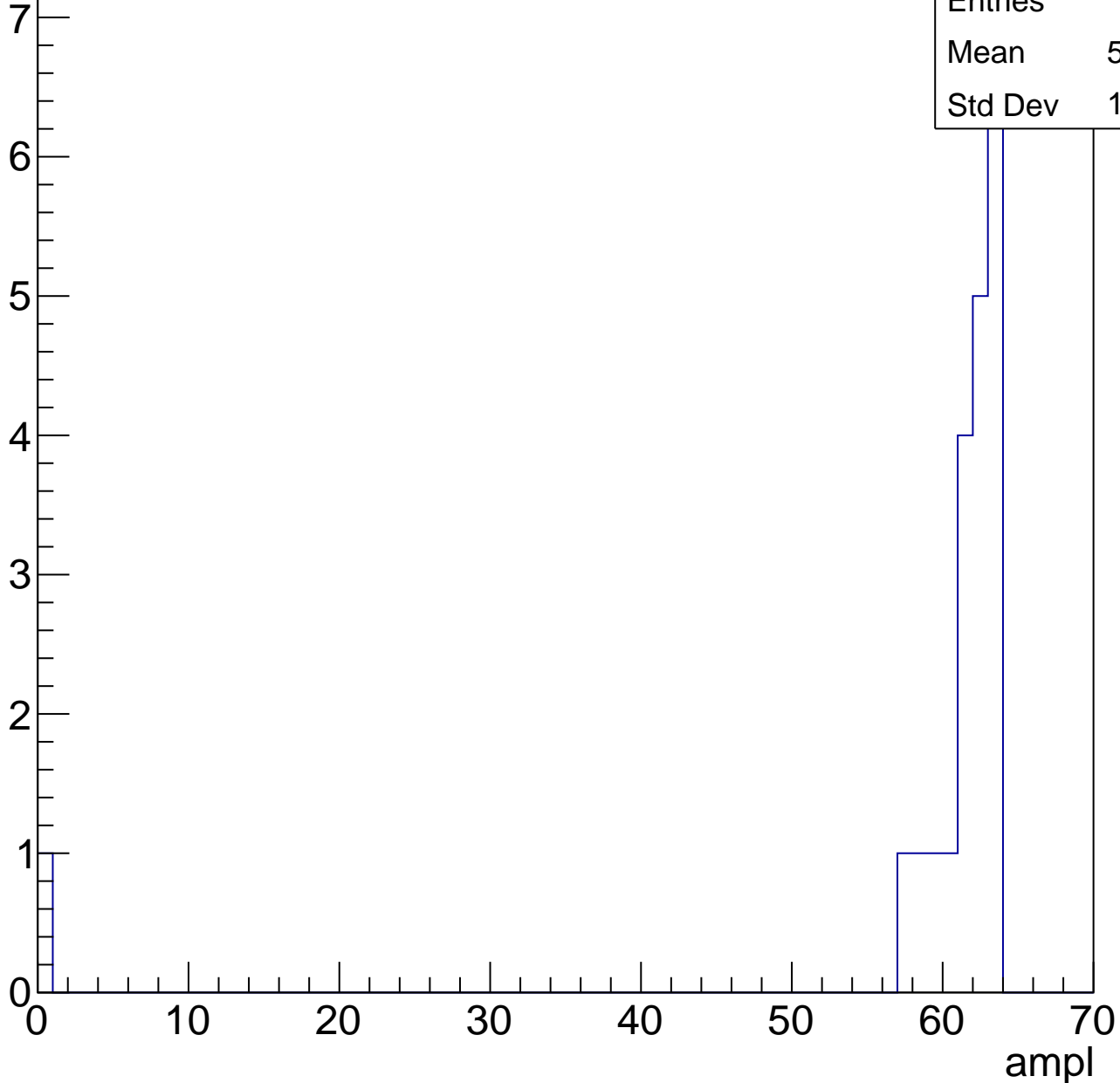


# B1L103S, U2-ch82, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	21
Mean	58.52
Std Dev	13.19





# B1L103S, U2-ch82, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch83, adc0

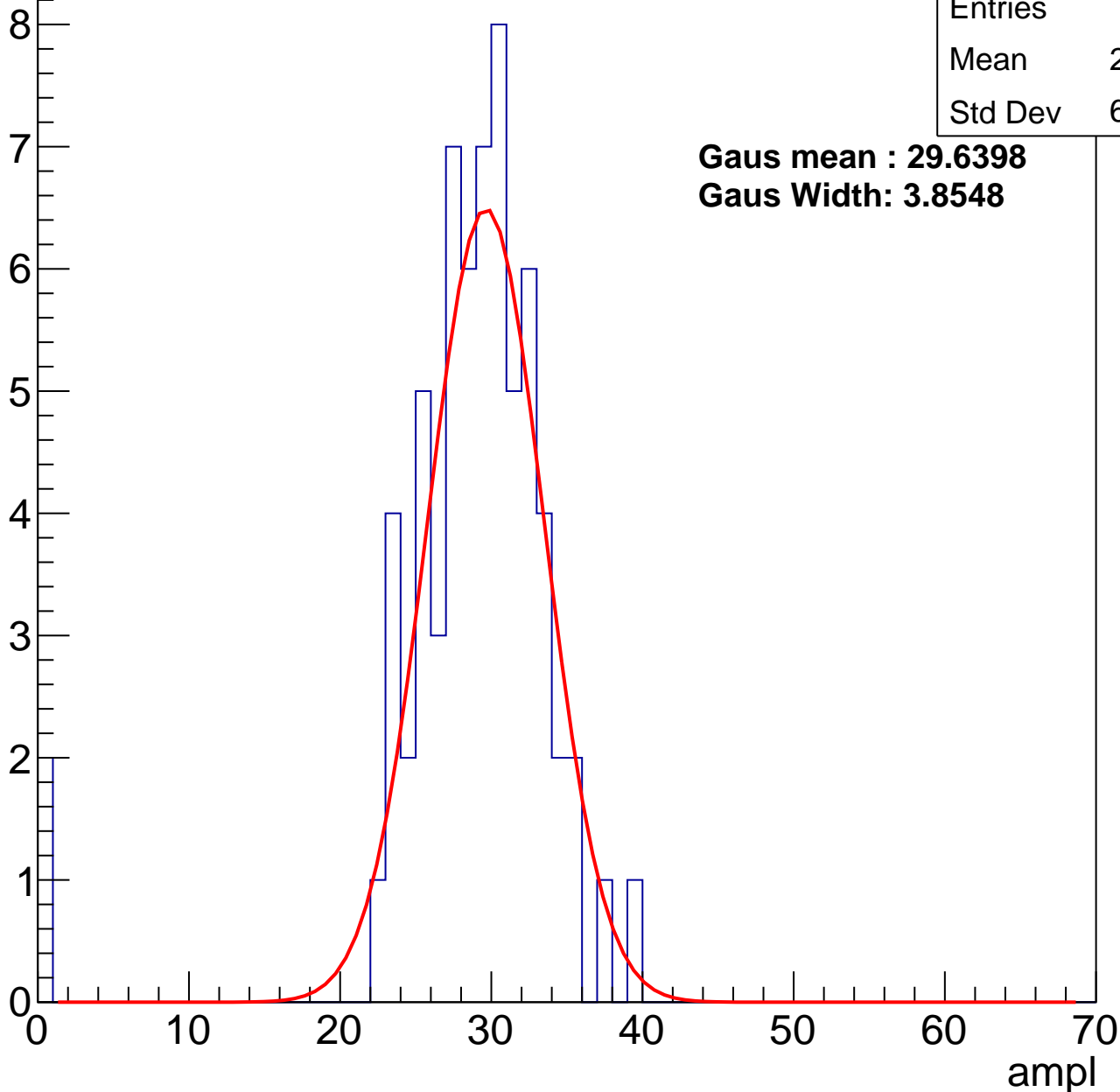
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	28.15
Std Dev	6.093

**Gaus mean : 29.6398**

**Gaus Width: 3.8548**



# B1L103S, U2-ch83, adc1

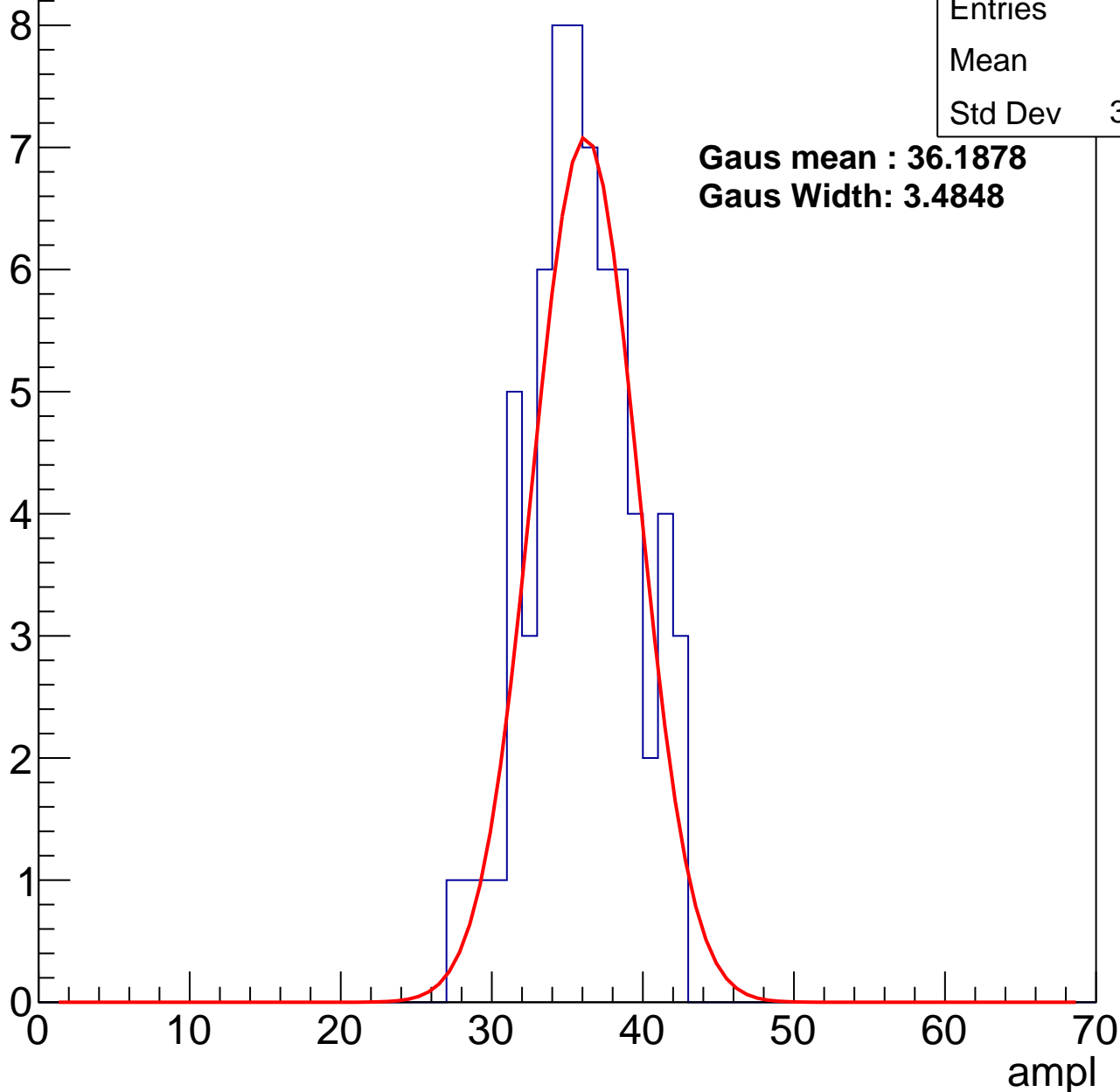
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	35.5
Std Dev	3.452

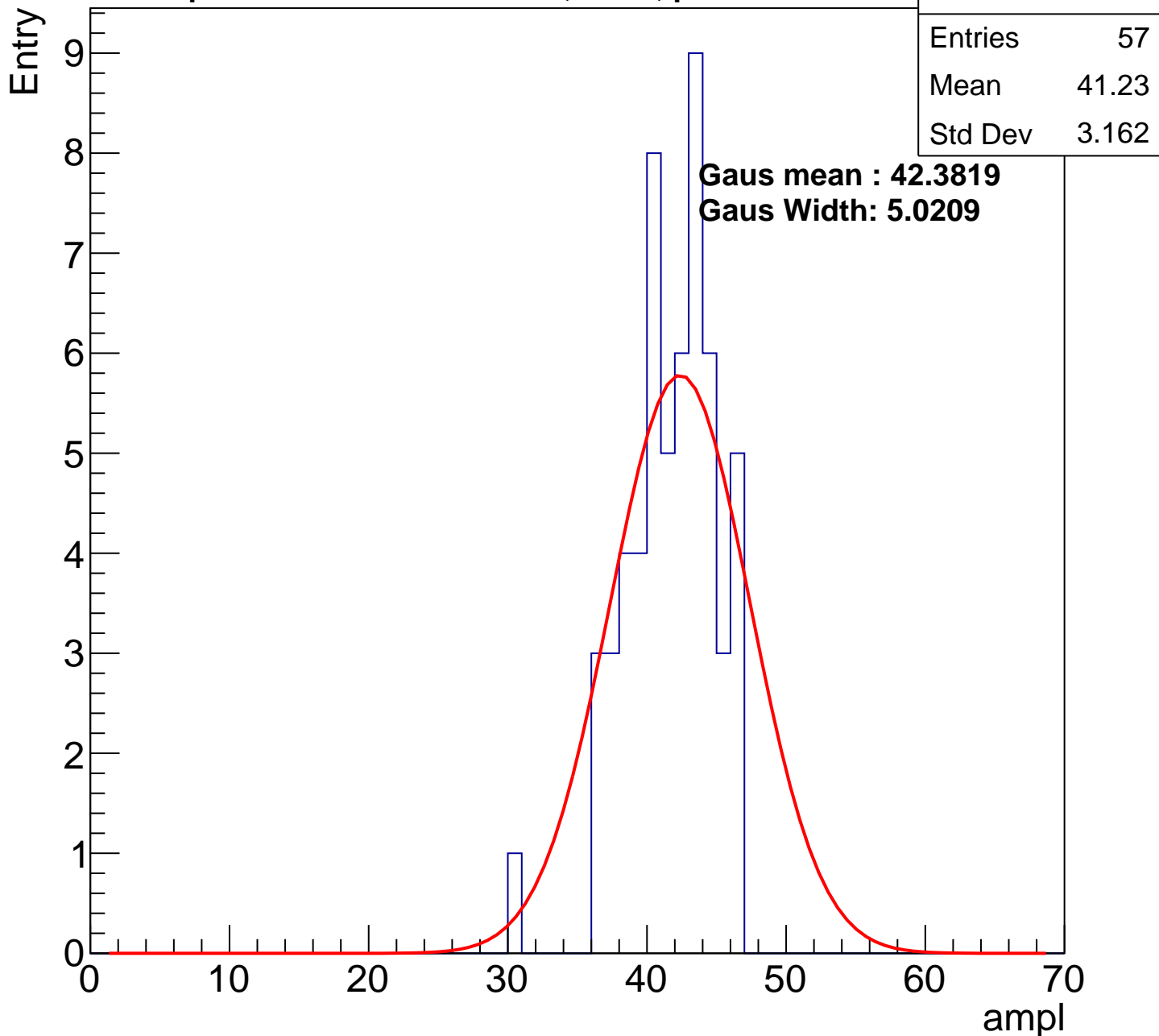
**Gaus mean : 36.1878**

**Gaus Width: 3.4848**



# B1L103S, U2-ch83, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U2-ch83, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

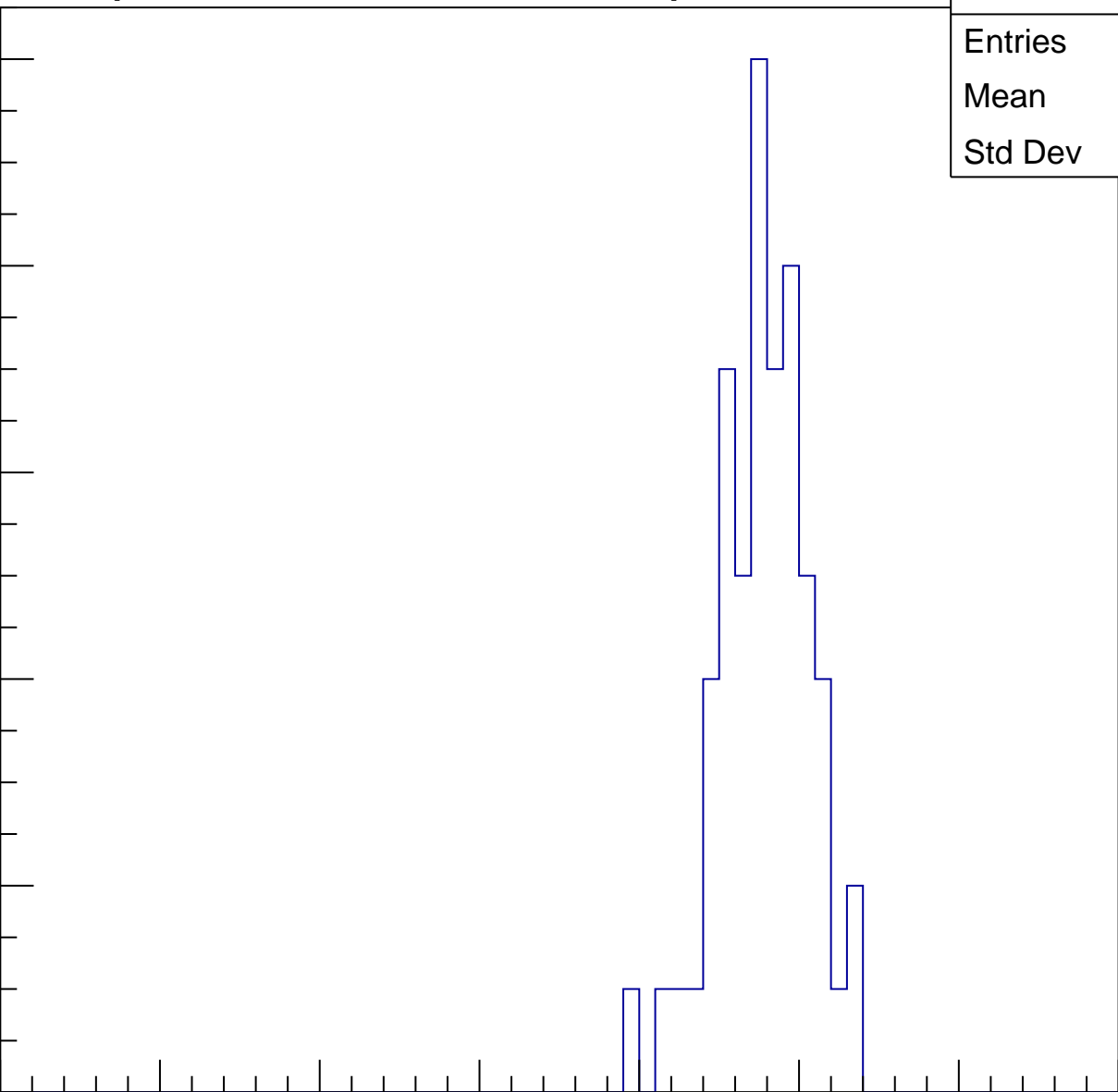
Entries	57
Mean	47.3
Std Dev	2.81

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

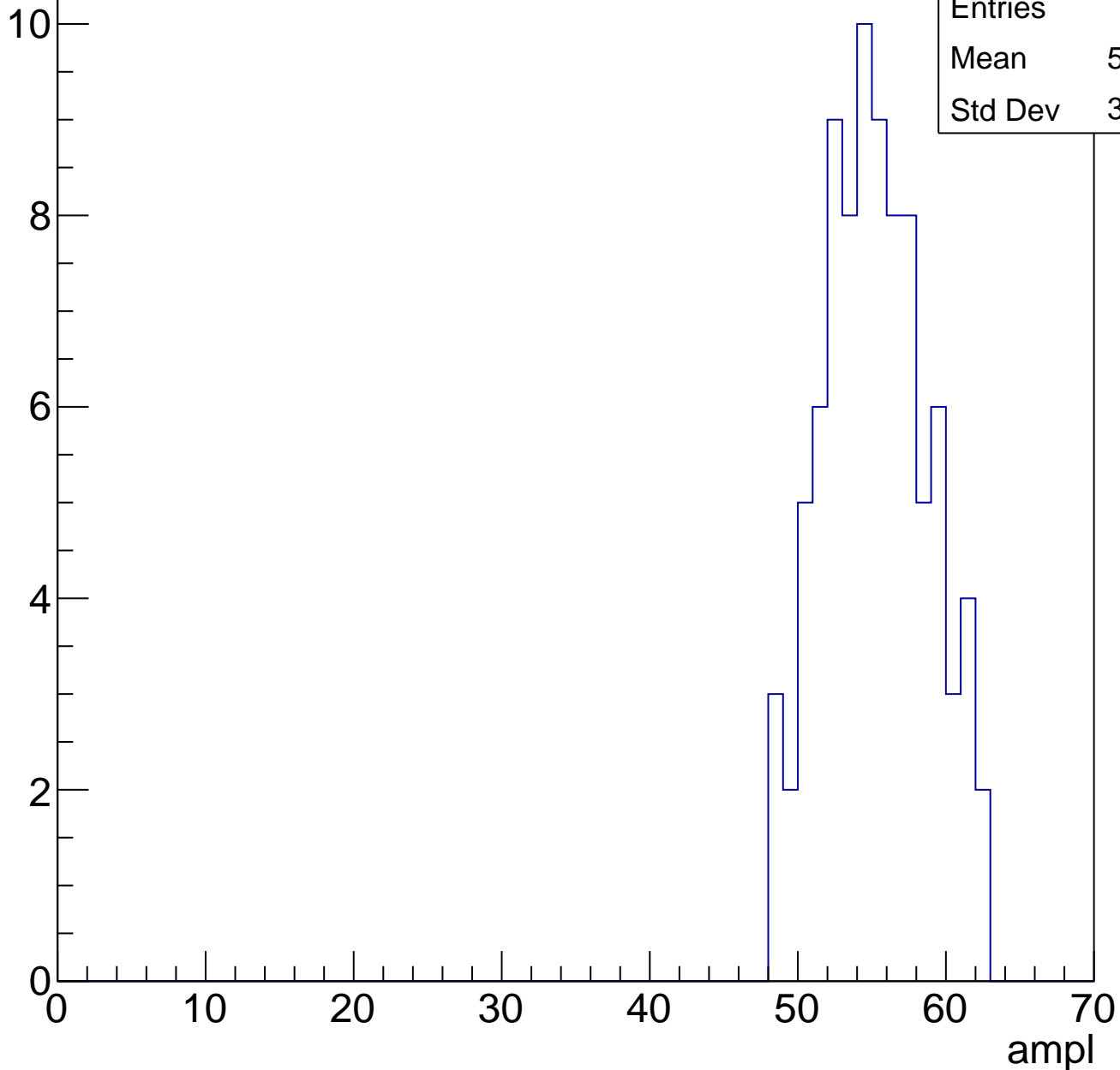


# B1L103S, U2-ch83, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	88
Mean	54.78
Std Dev	3.466

Entry

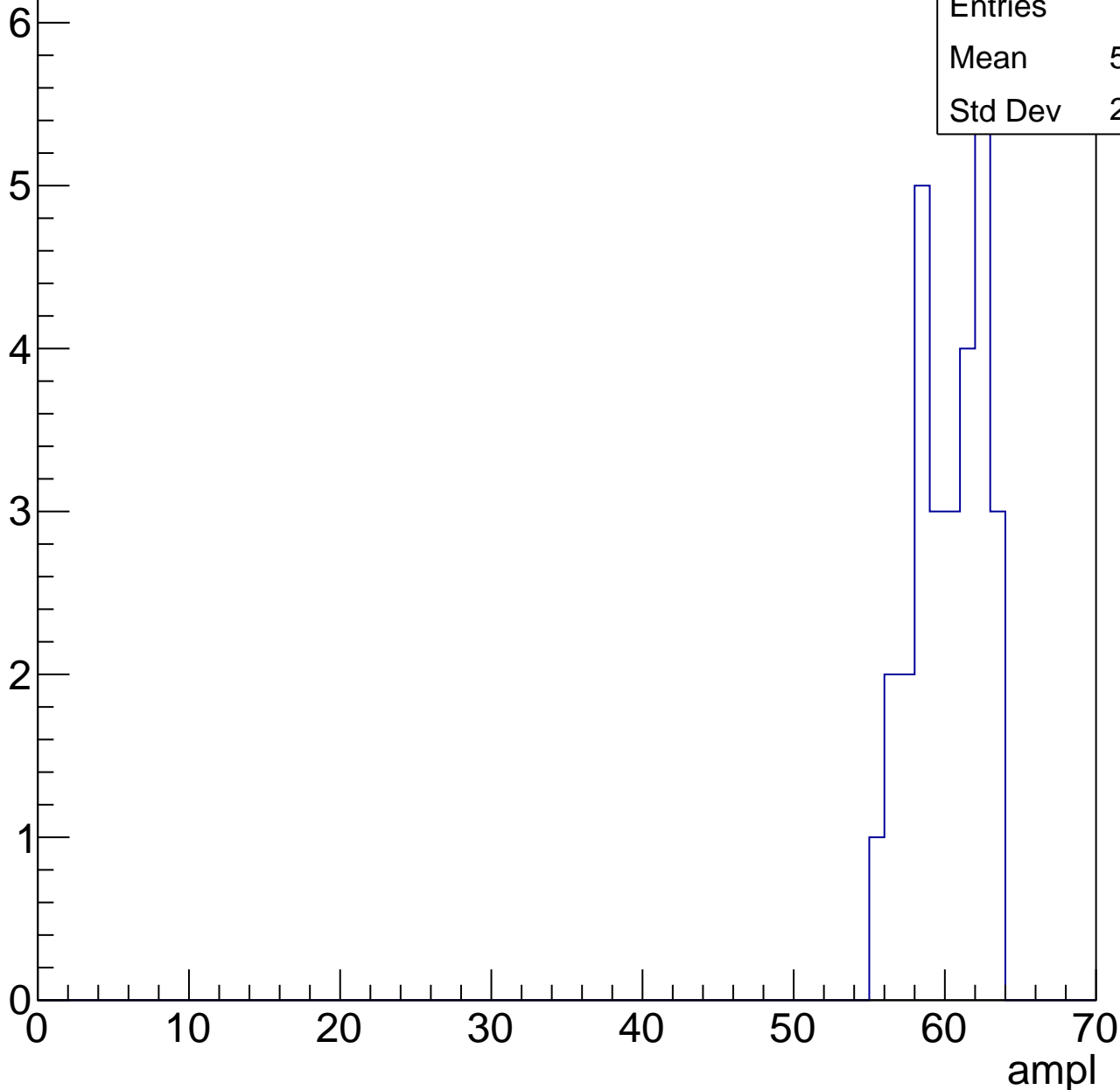


# B1L103S, U2-ch83, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	29
Mean	59.76
Std Dev	2.284

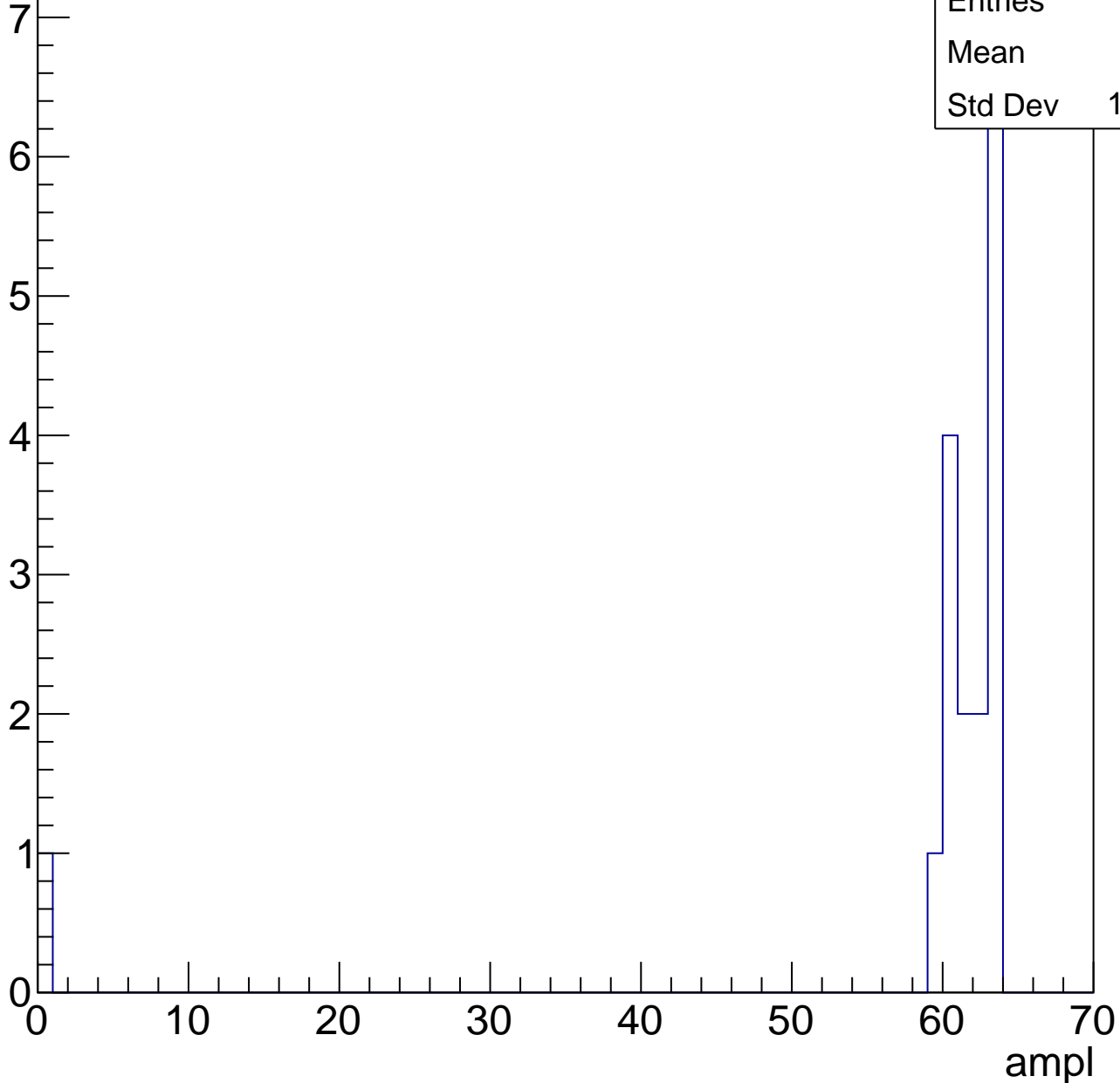


# B1L103S, U2-ch83, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	17
Mean	58
Std Dev	14.56





# B1L103S, U2-ch83, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch84, adc0

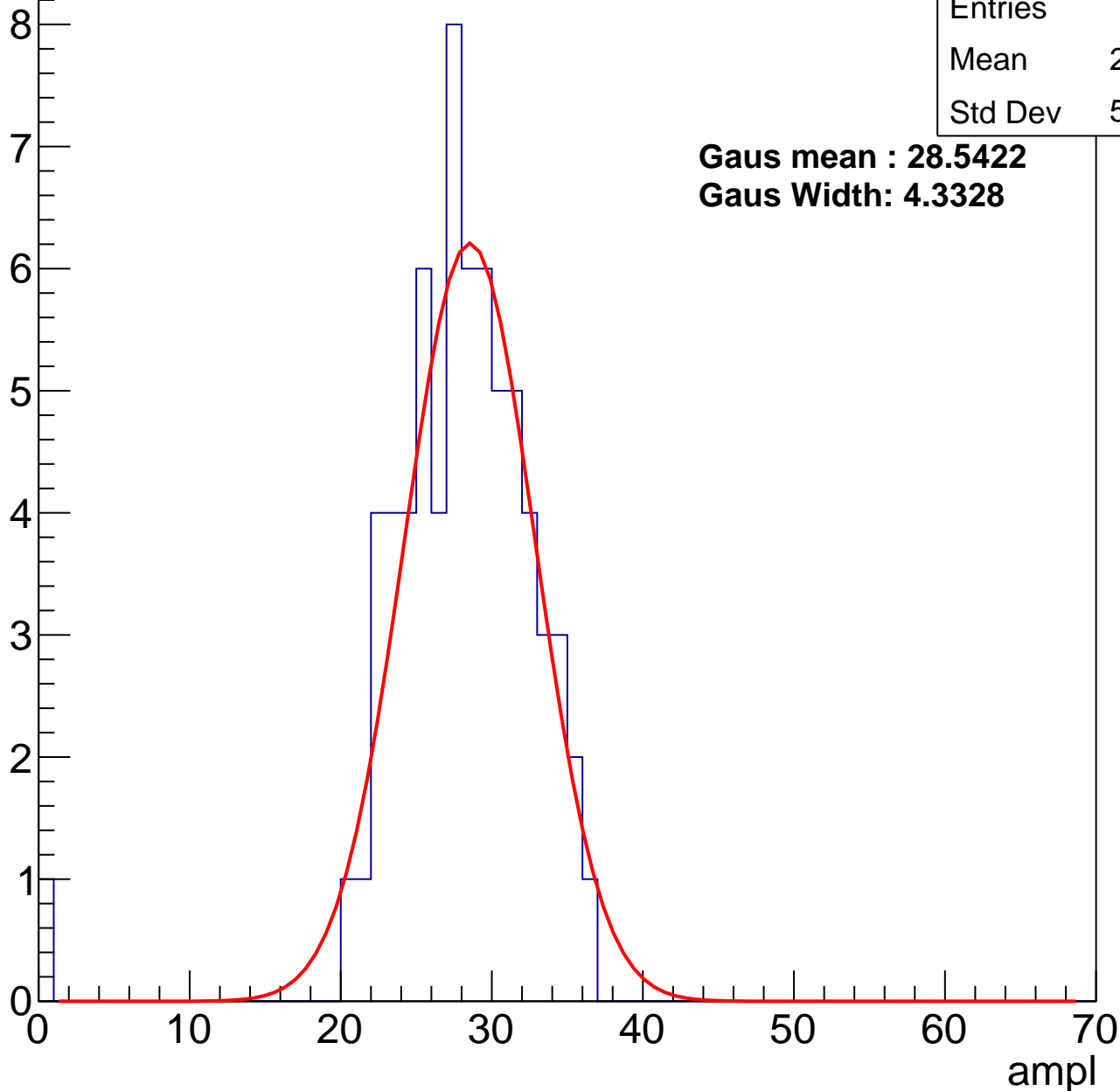
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	27.49
Std Dev	5.066

**Gaus mean : 28.5422**

**Gaus Width: 4.3328**



# B1L103S, U2-ch84, adc1

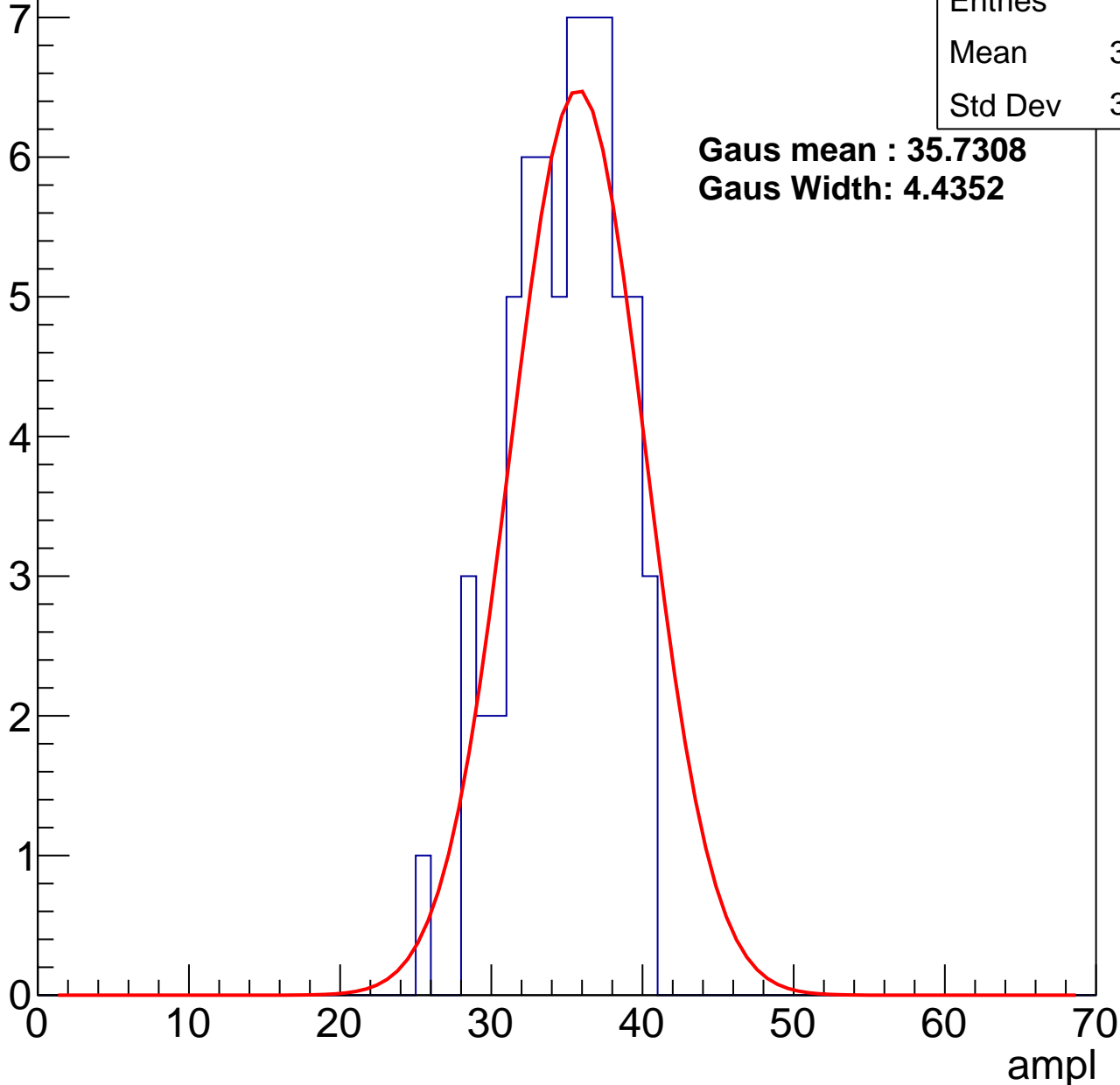
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	34.42
Std Dev	3.413

**Gaus mean : 35.7308**

**Gaus Width: 4.4352**



# B1L103S, U2-ch84, adc2

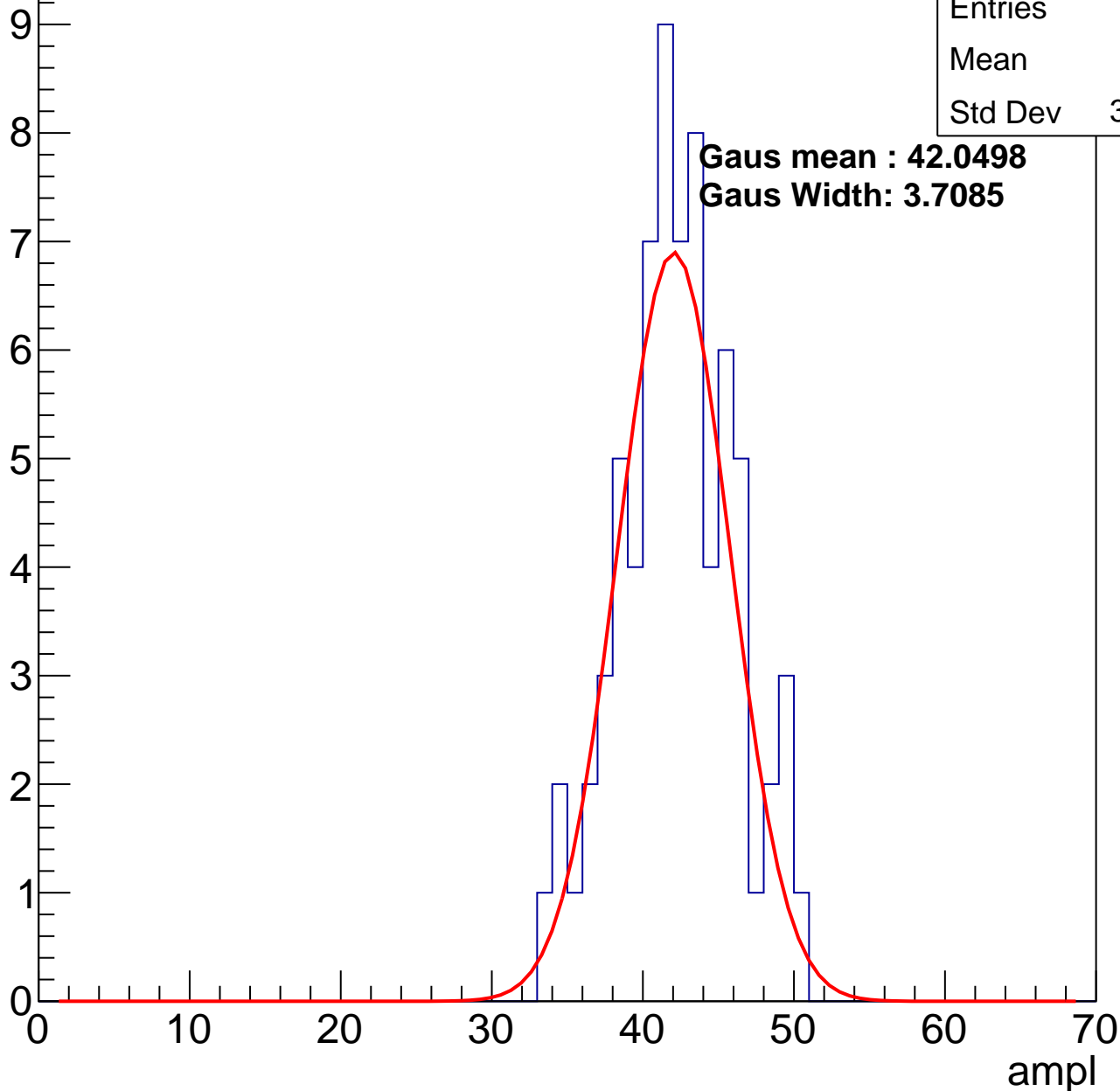
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	41.8
Std Dev	3.793

**Gaus mean : 42.0498**

**Gaus Width: 3.7085**

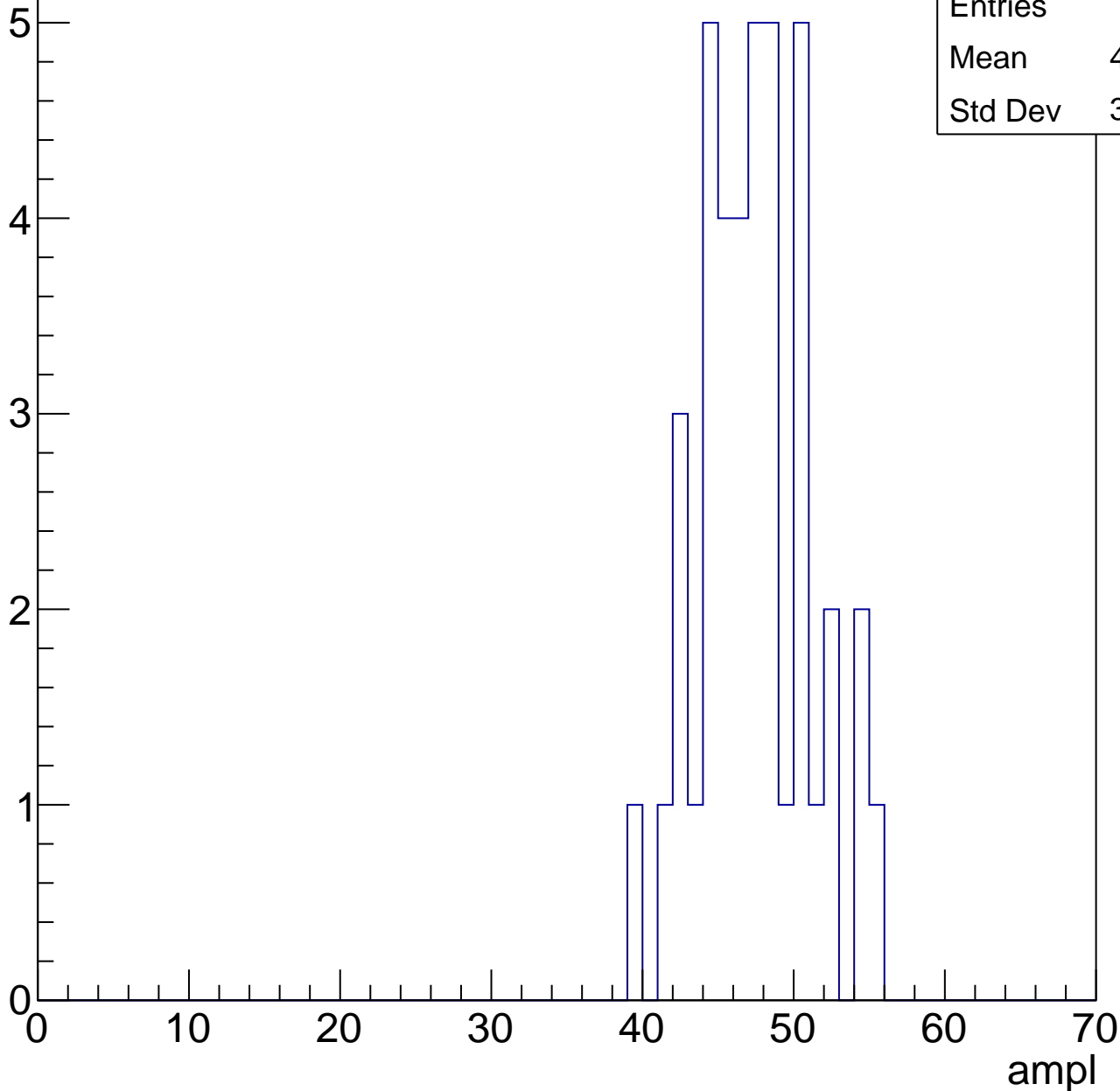


# B1L103S, U2-ch84, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	41
Mean	46.95
Std Dev	3.622

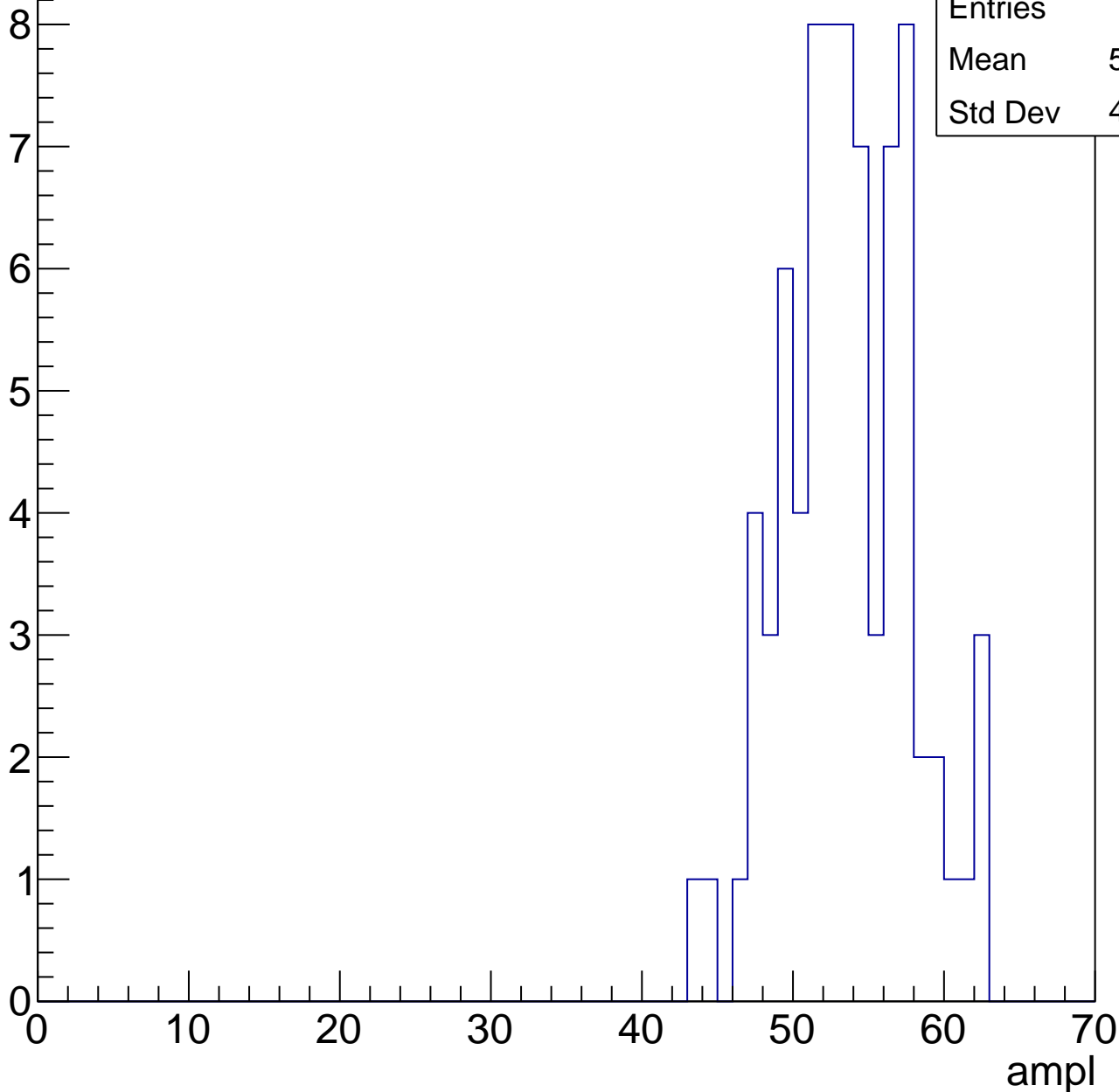


# B1L103S, U2-ch84, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	53.06
Std Dev	4.096

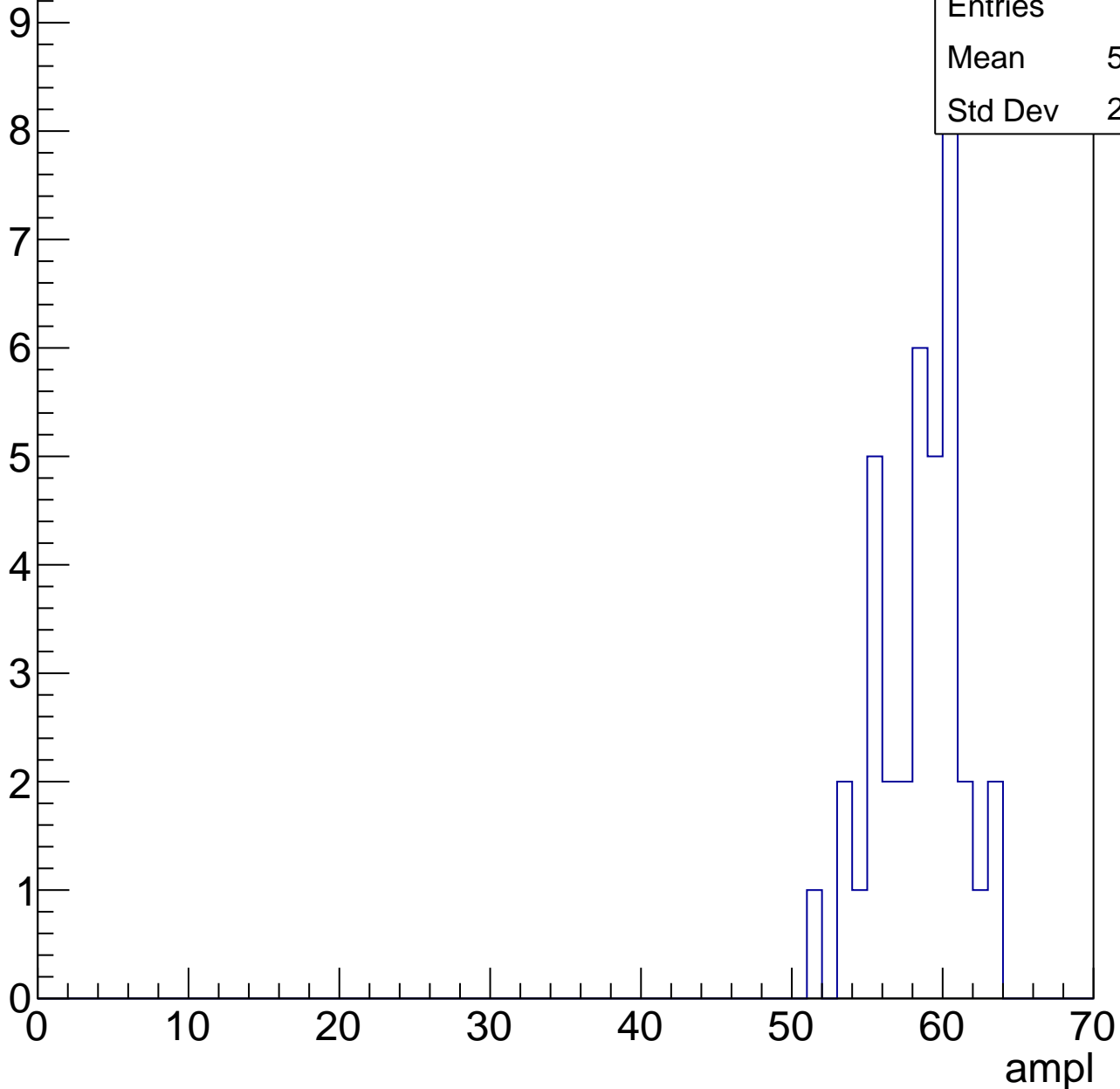


# B1L103S, U2-ch84, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	38
Mean	58.03
Std Dev	2.786

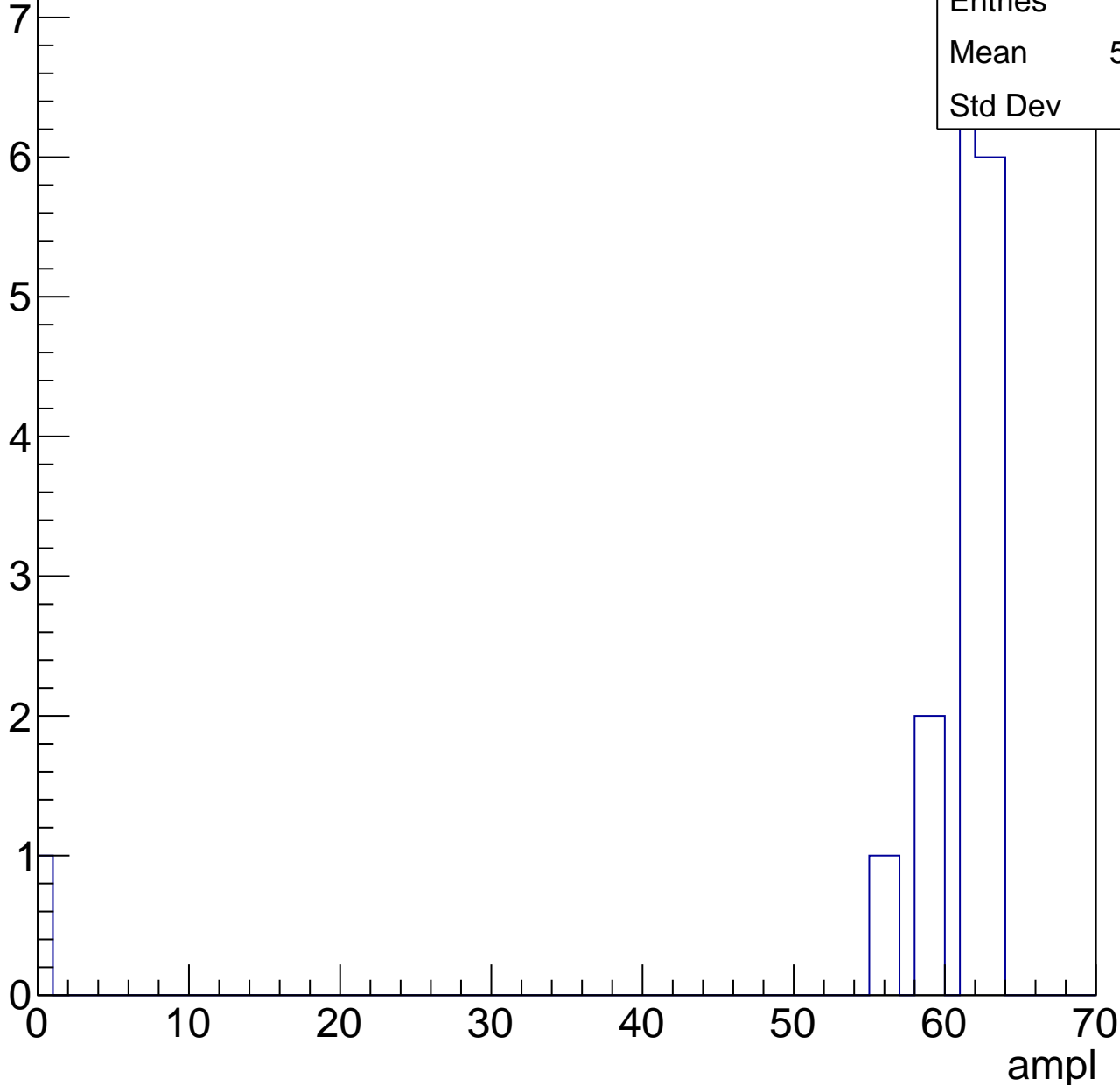


# B1L103S, U2-ch84, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	26
Mean	58.54
Std Dev	11.9

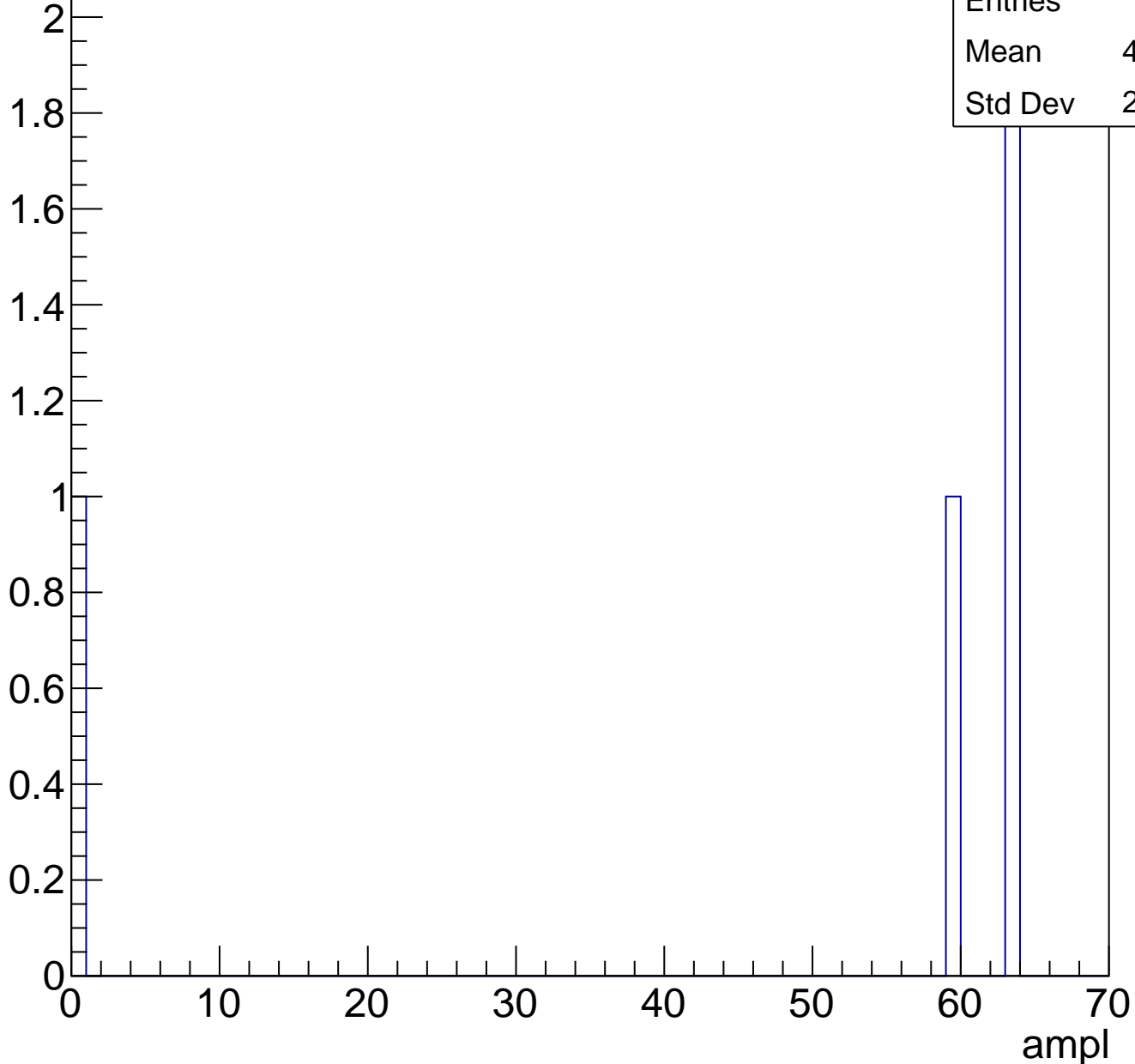




# B1L103S, U2-ch84, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch85, adc0

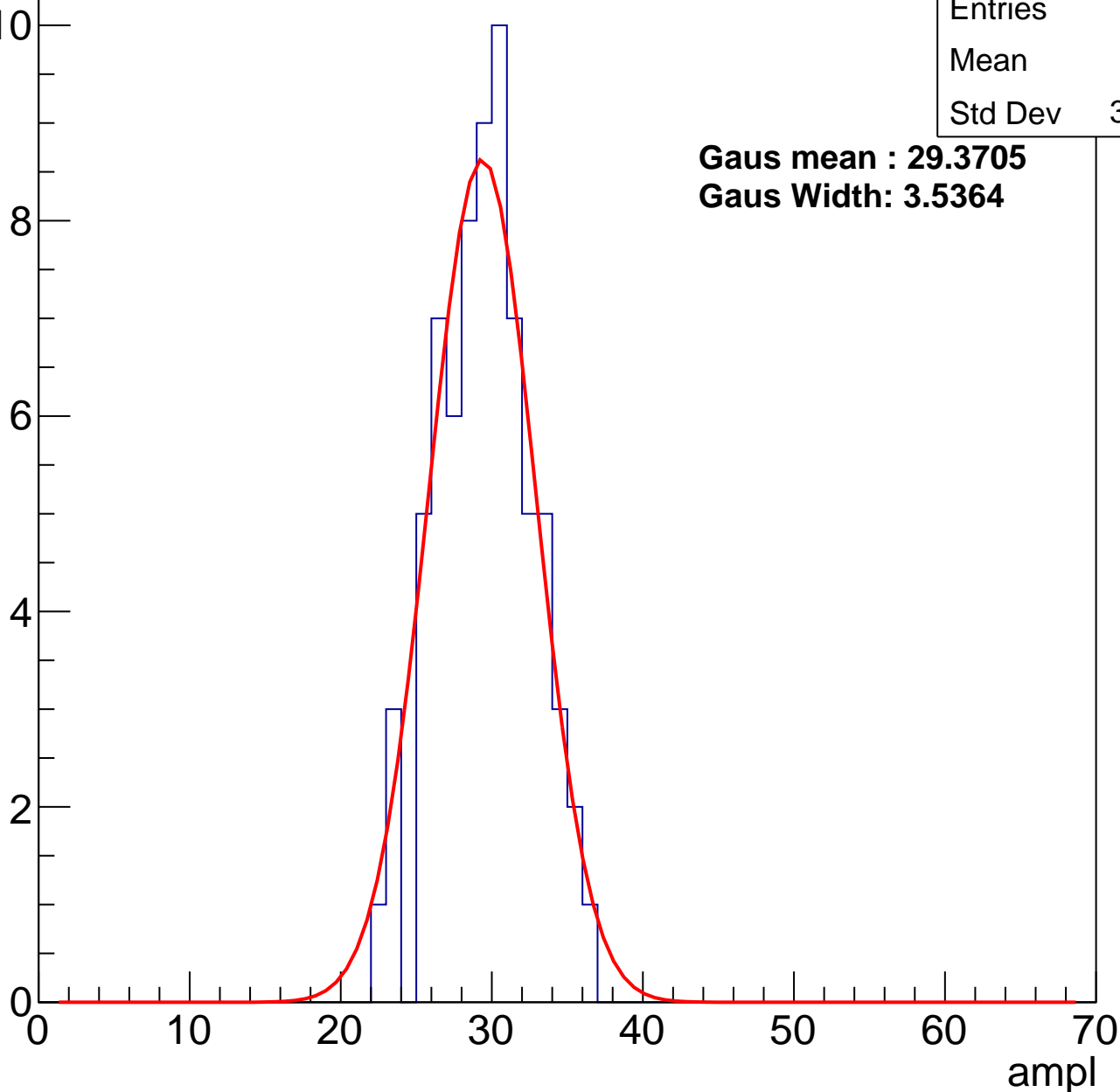
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	29.1
Std Dev	3.096

**Gaus mean : 29.3705**

**Gaus Width: 3.5364**



# B1L103S, U2-ch85, adc1

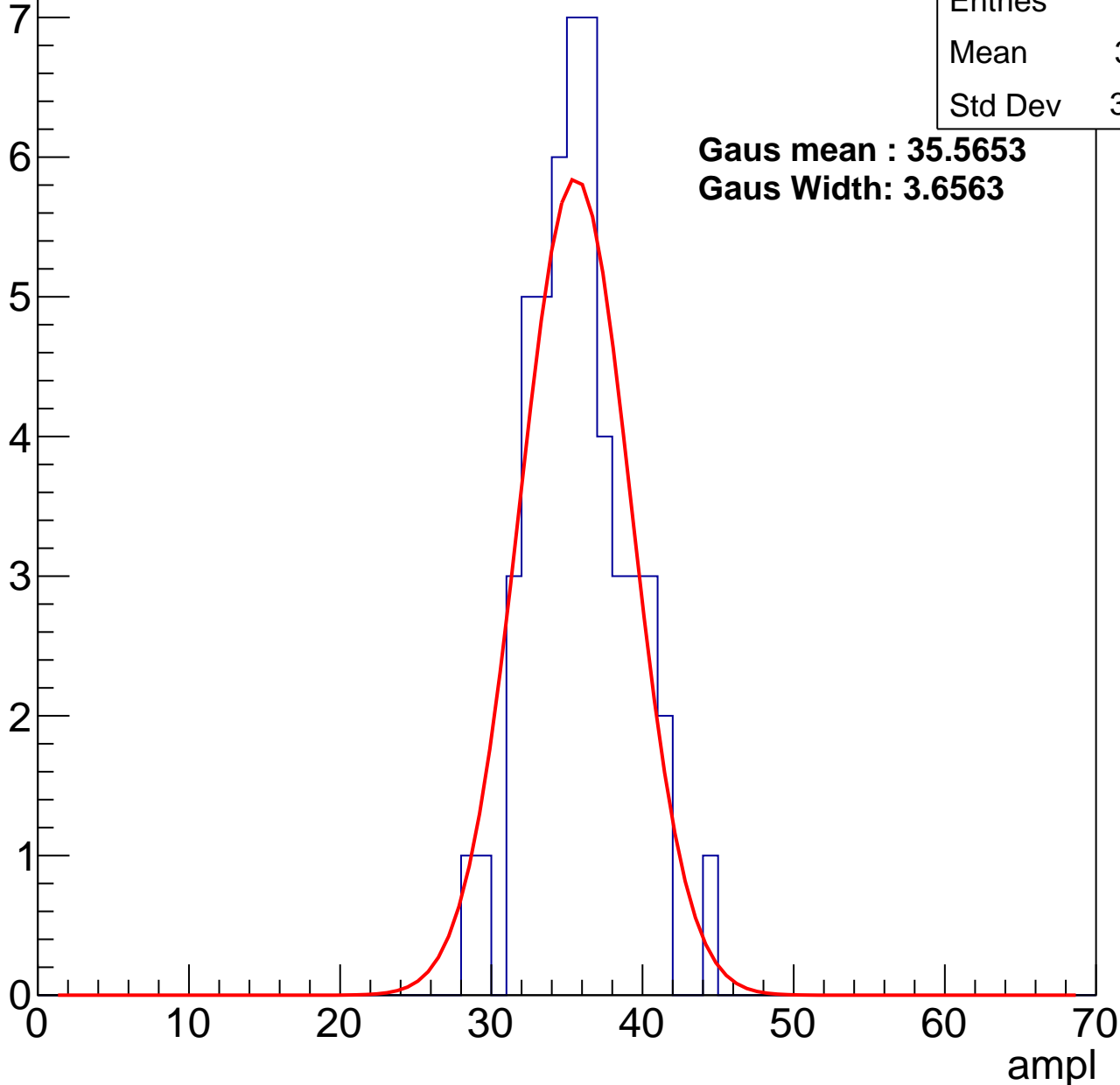
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	35.31
Std Dev	3.208

**Gaus mean : 35.5653**

**Gaus Width: 3.6563**



# B1L103S, U2-ch85, adc2

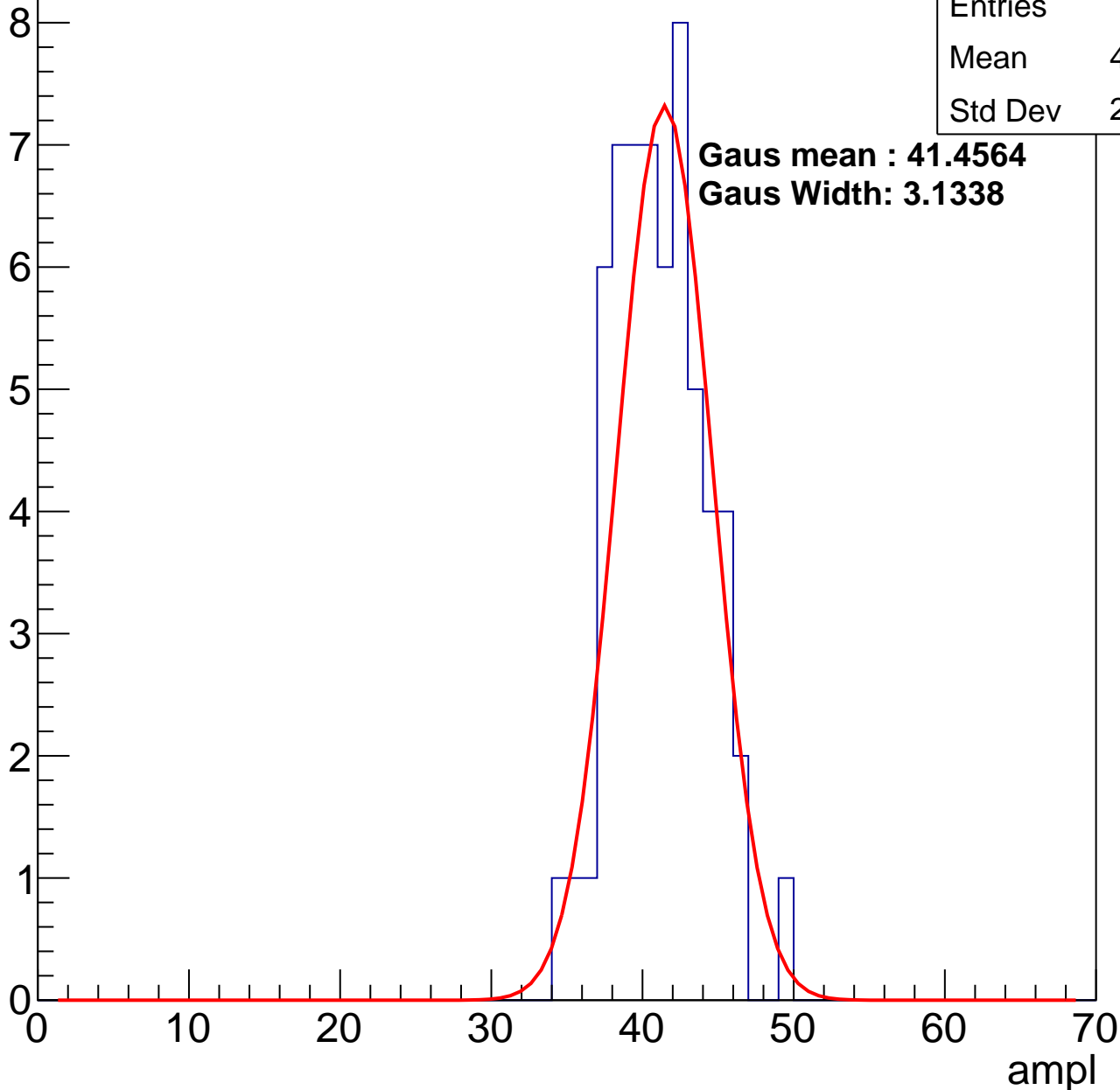
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	40.67
Std Dev	2.998

**Gaus mean : 41.4564**

**Gaus Width: 3.1338**

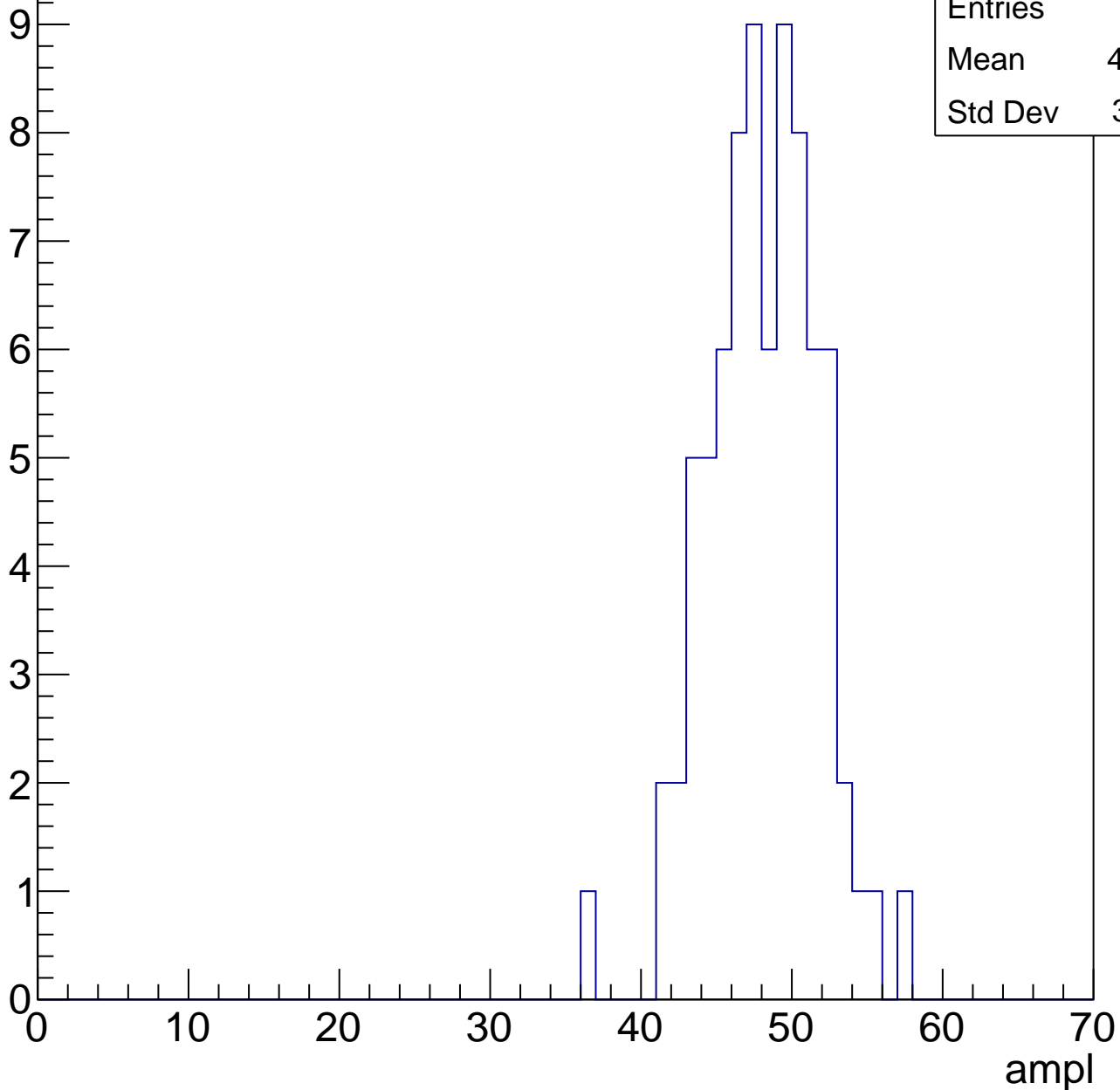


# B1L103S, U2-ch85, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	47.65
Std Dev	3.601

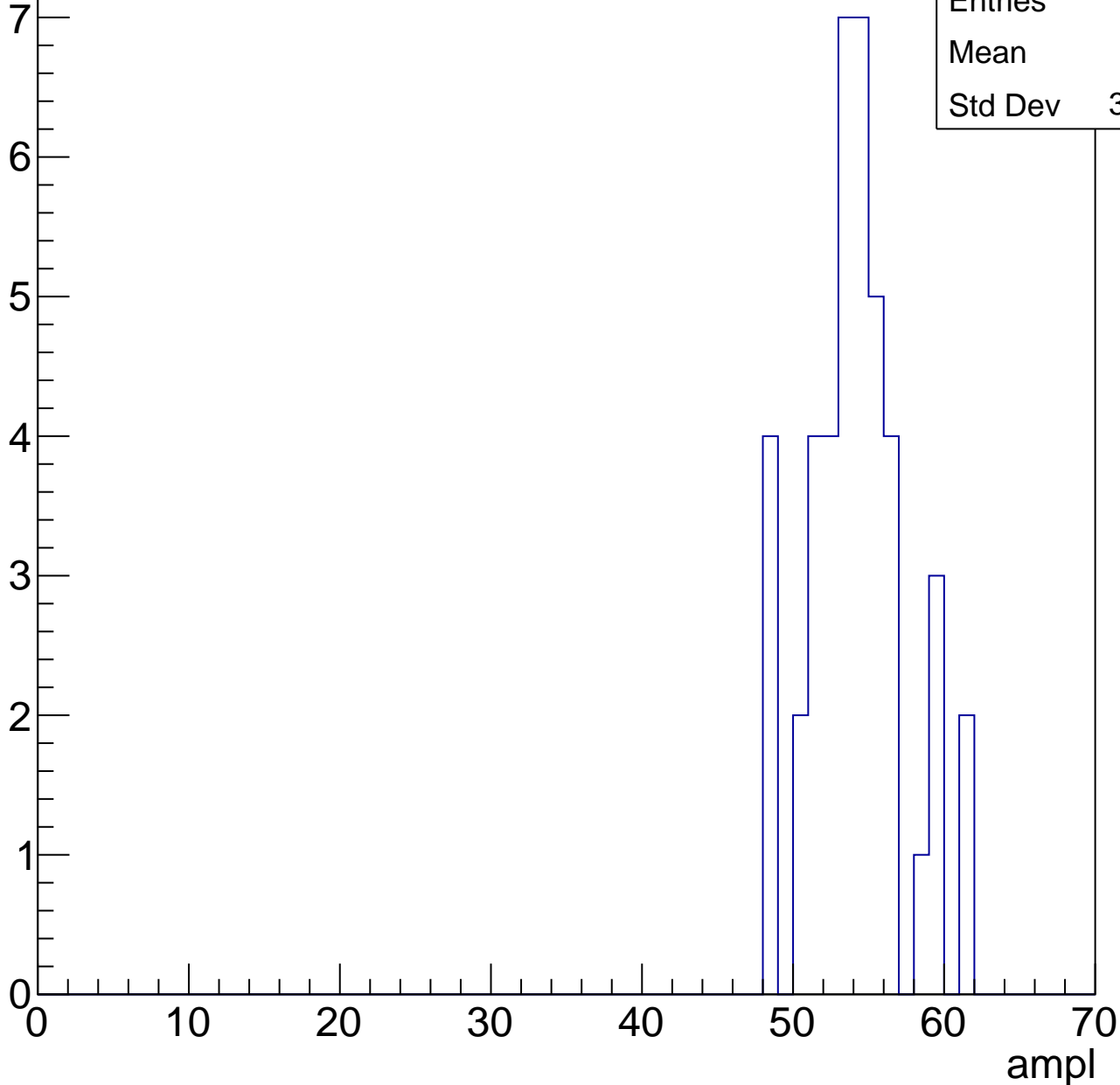


# B1L103S, U2-ch85, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	43
Mean	53.7
Std Dev	3.203

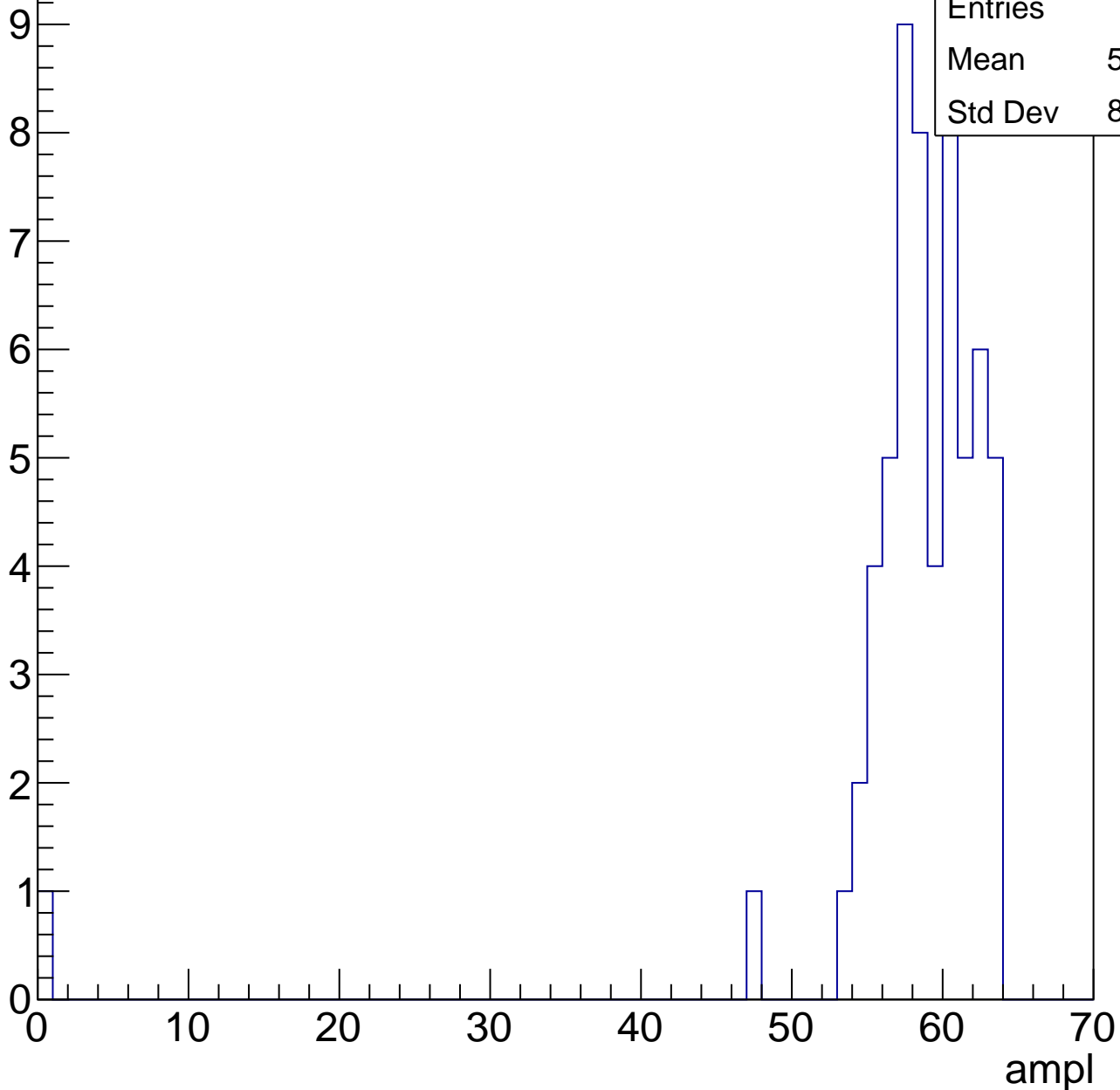


# B1L103S, U2-ch85, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	57.55
Std Dev	8.063

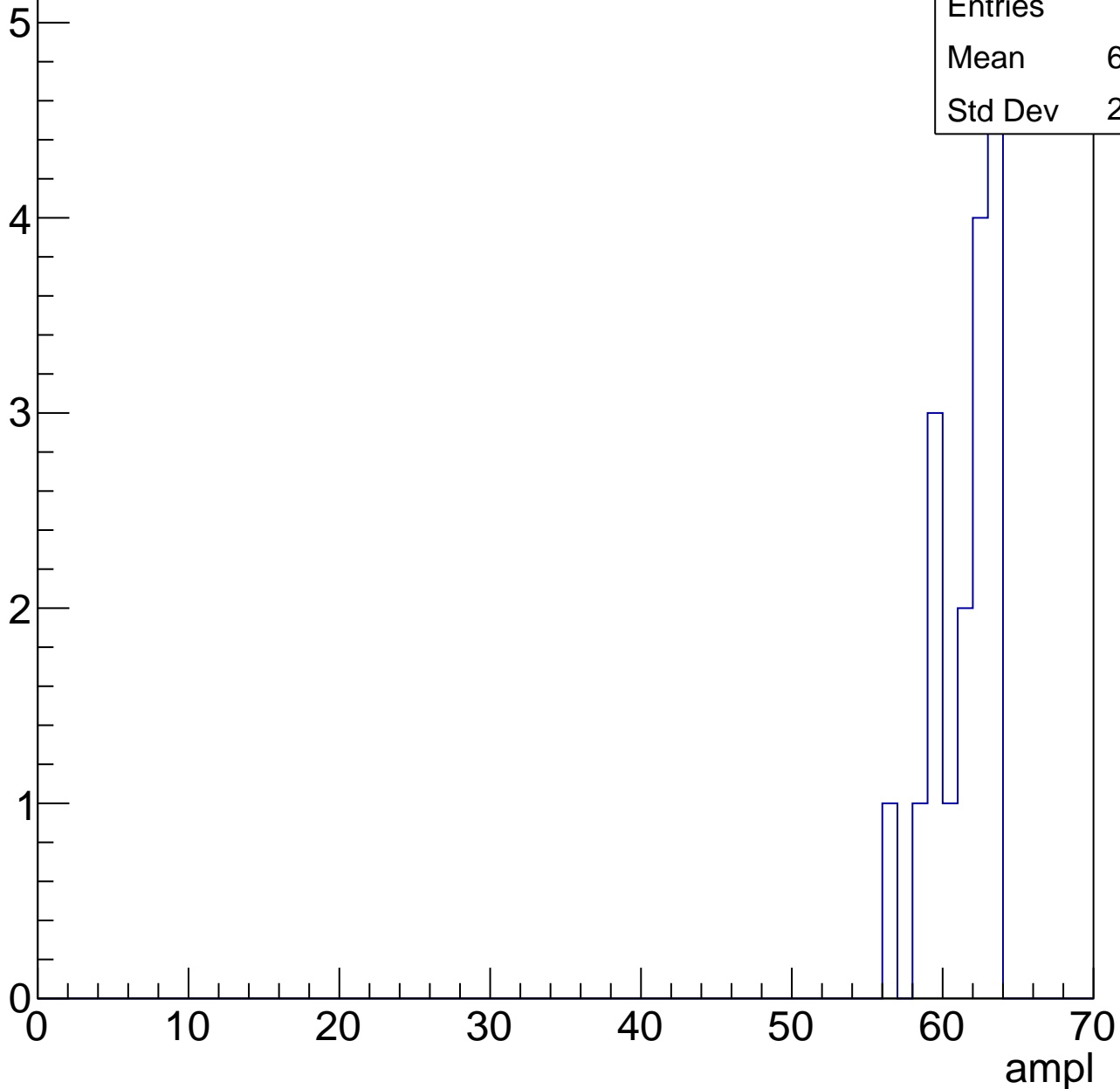


# B1L103S, U2-ch85, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	17
Mean	60.94
Std Dev	2.043

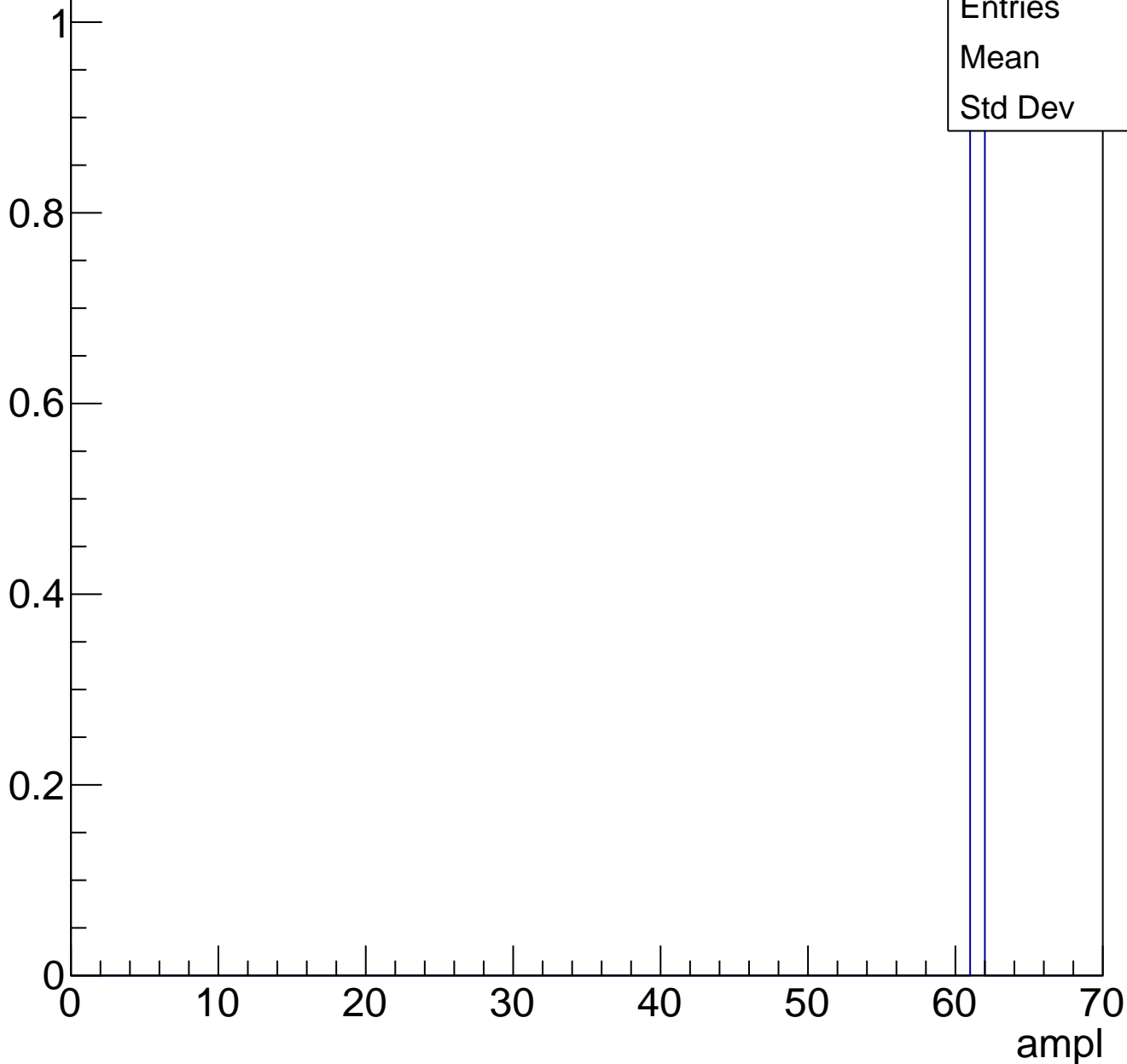




# B1L103S, U2-ch85, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch86, adc0

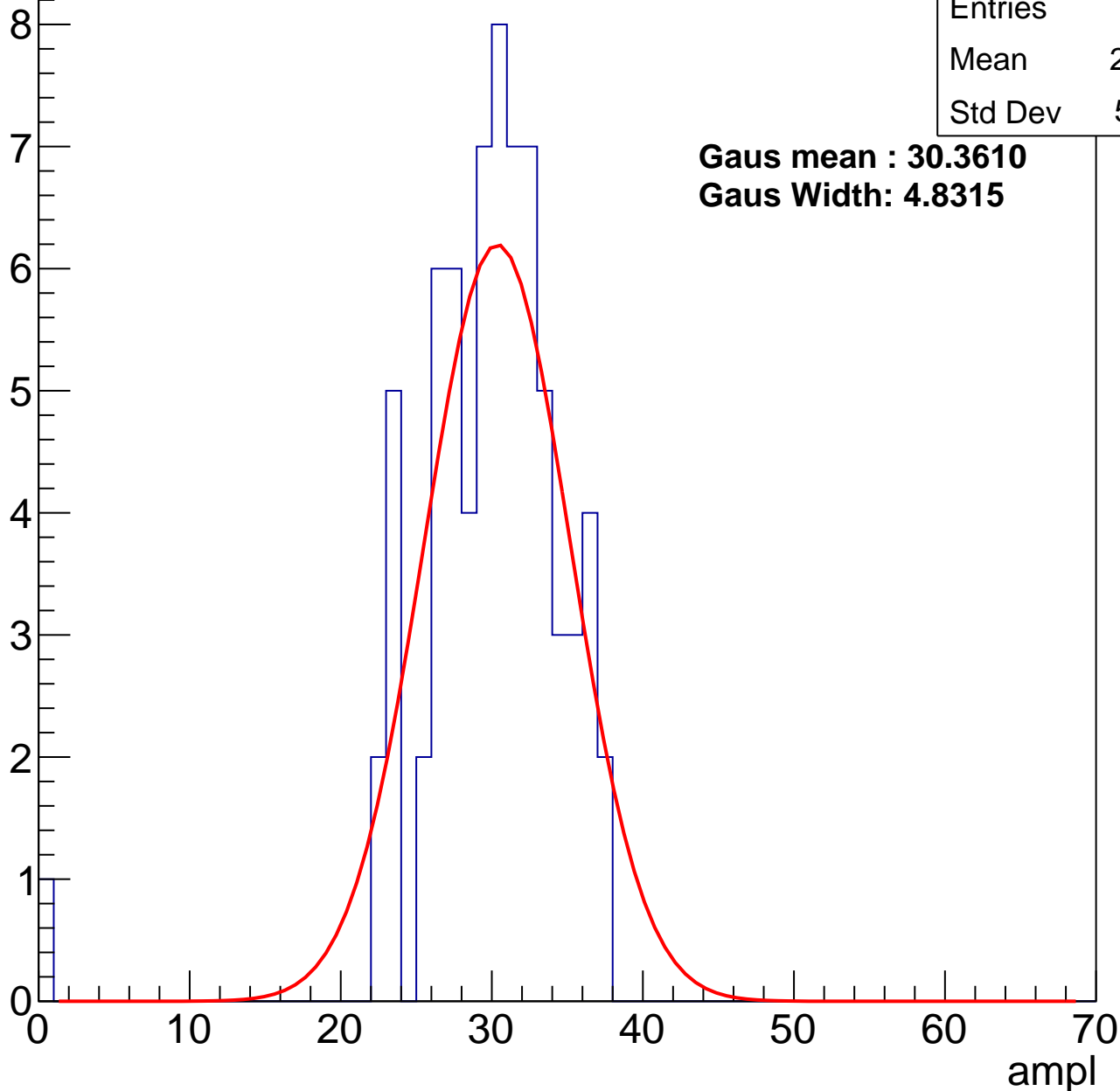
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	29.35
Std Dev	5.151

**Gaus mean : 30.3610**

**Gaus Width: 4.8315**



# B1L103S, U2-ch86, adc1

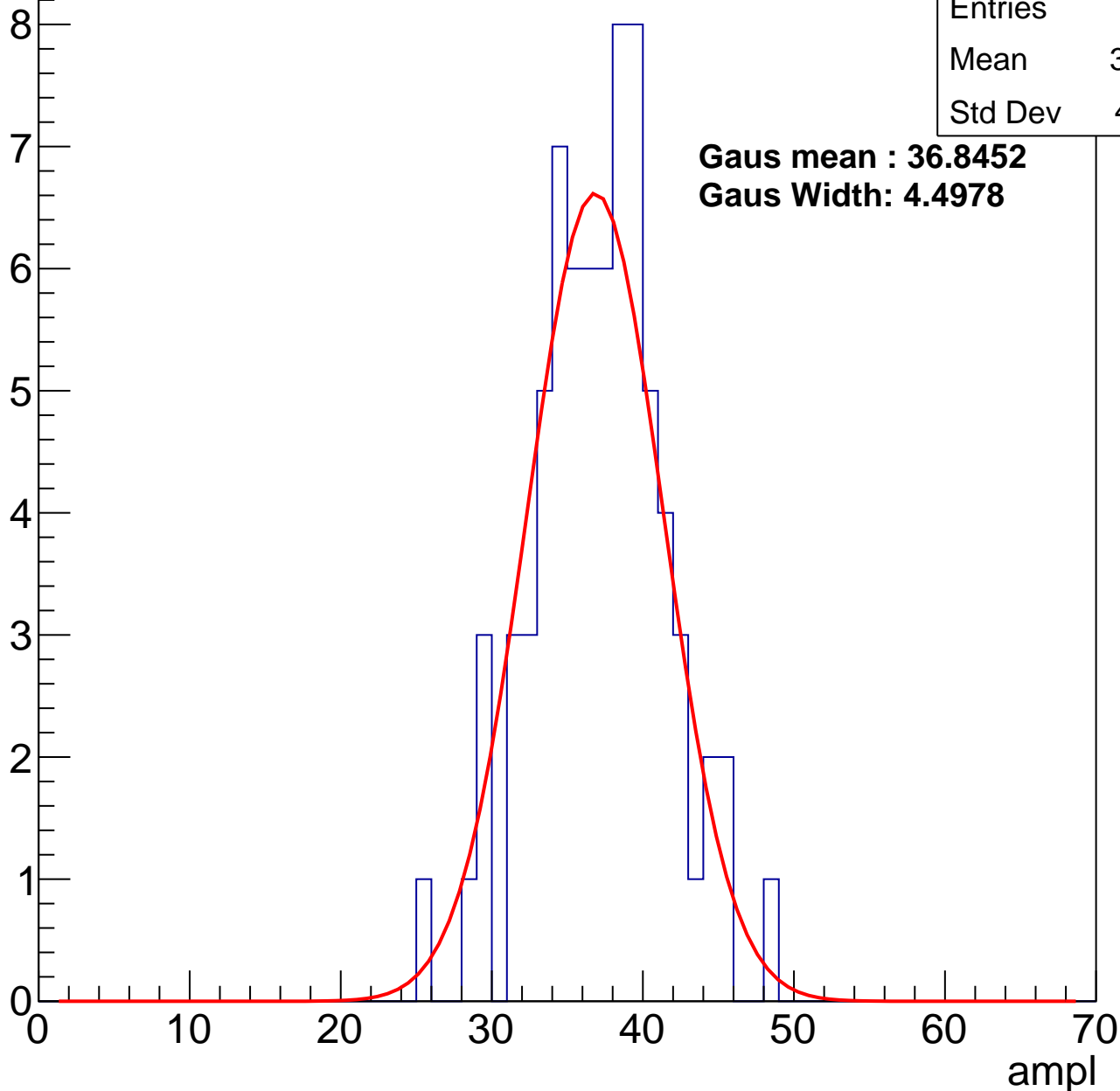
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	36.73
Std Dev	4.281

**Gaus mean : 36.8452**

**Gaus Width: 4.4978**



# B1L103S, U2-ch86, adc2

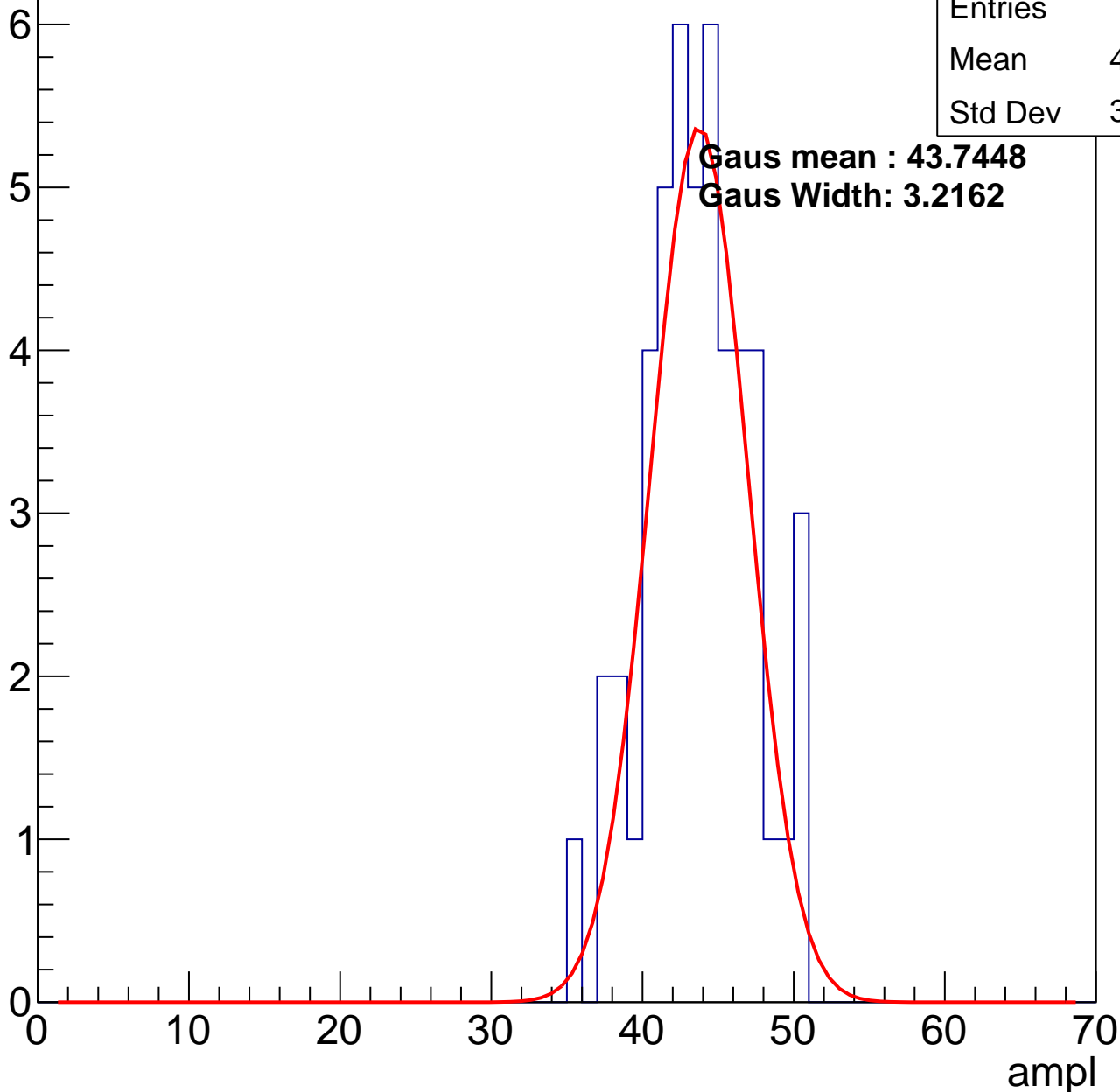
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	43.24
Std Dev	3.473

**Gaus mean : 43.7448**

**Gaus Width: 3.2162**

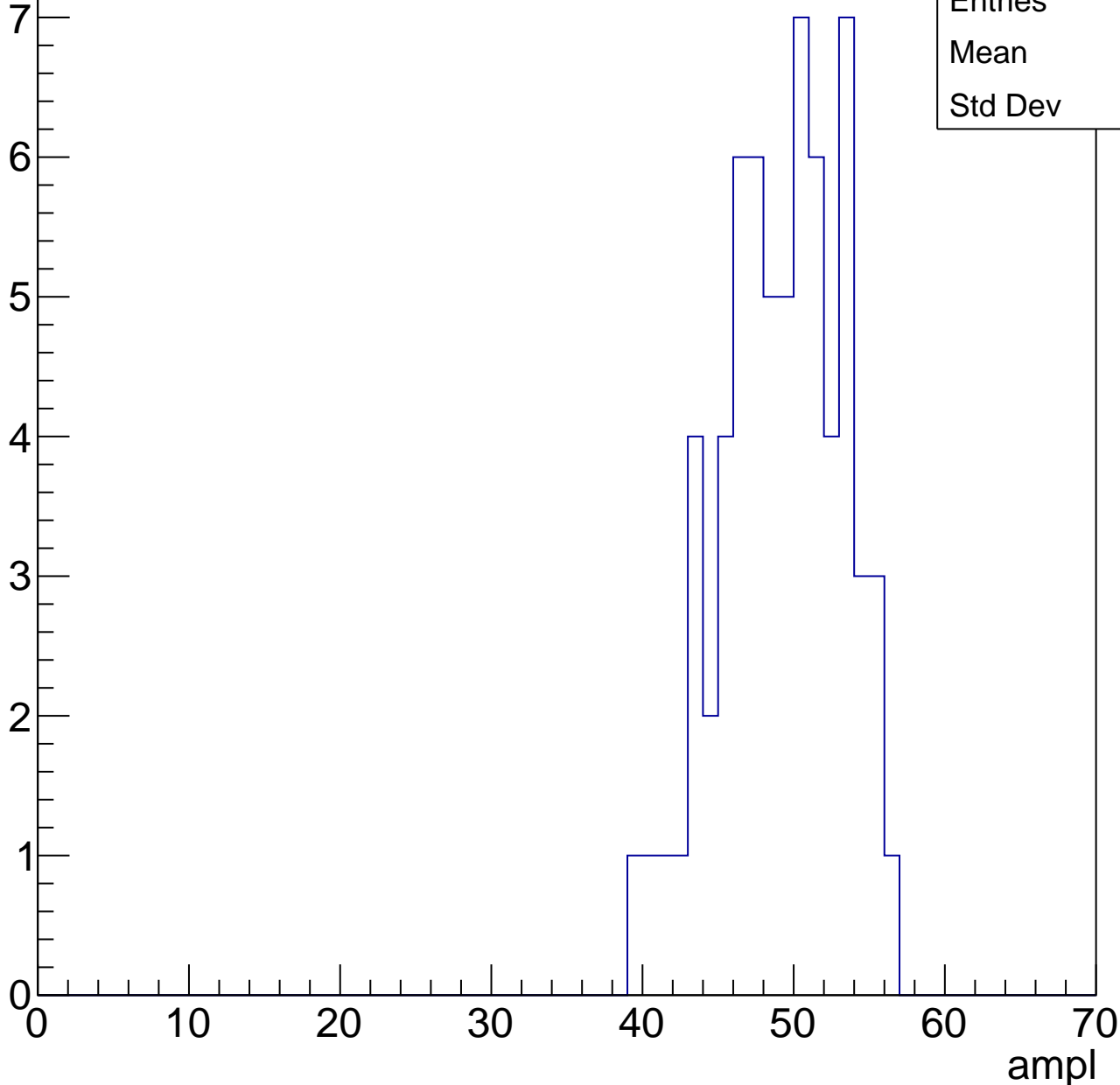


# B1L103S, U2-ch86, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	48.7
Std Dev	3.94

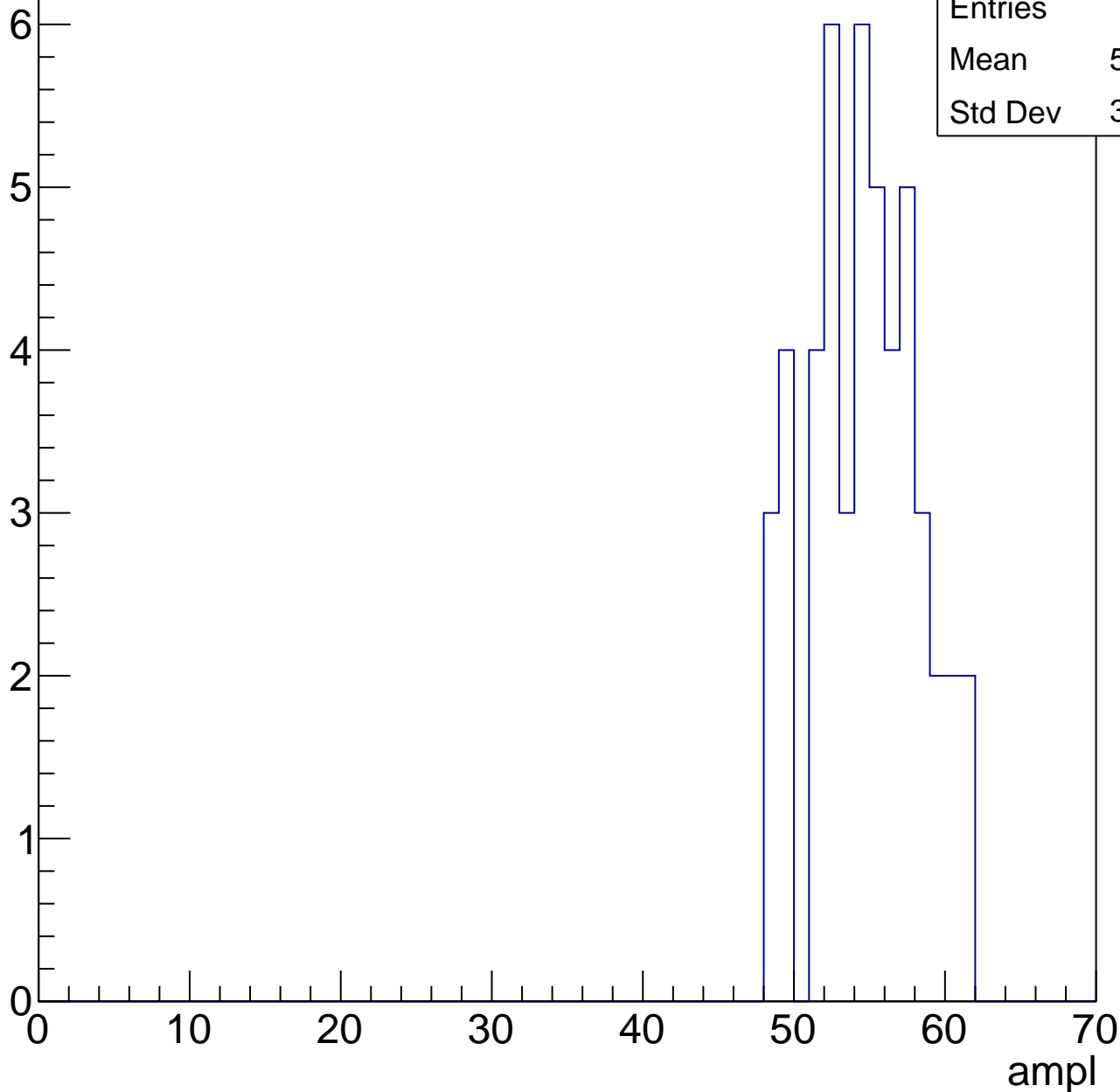


# B1L103S, U2-ch86, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	54.22
Std Dev	3.507

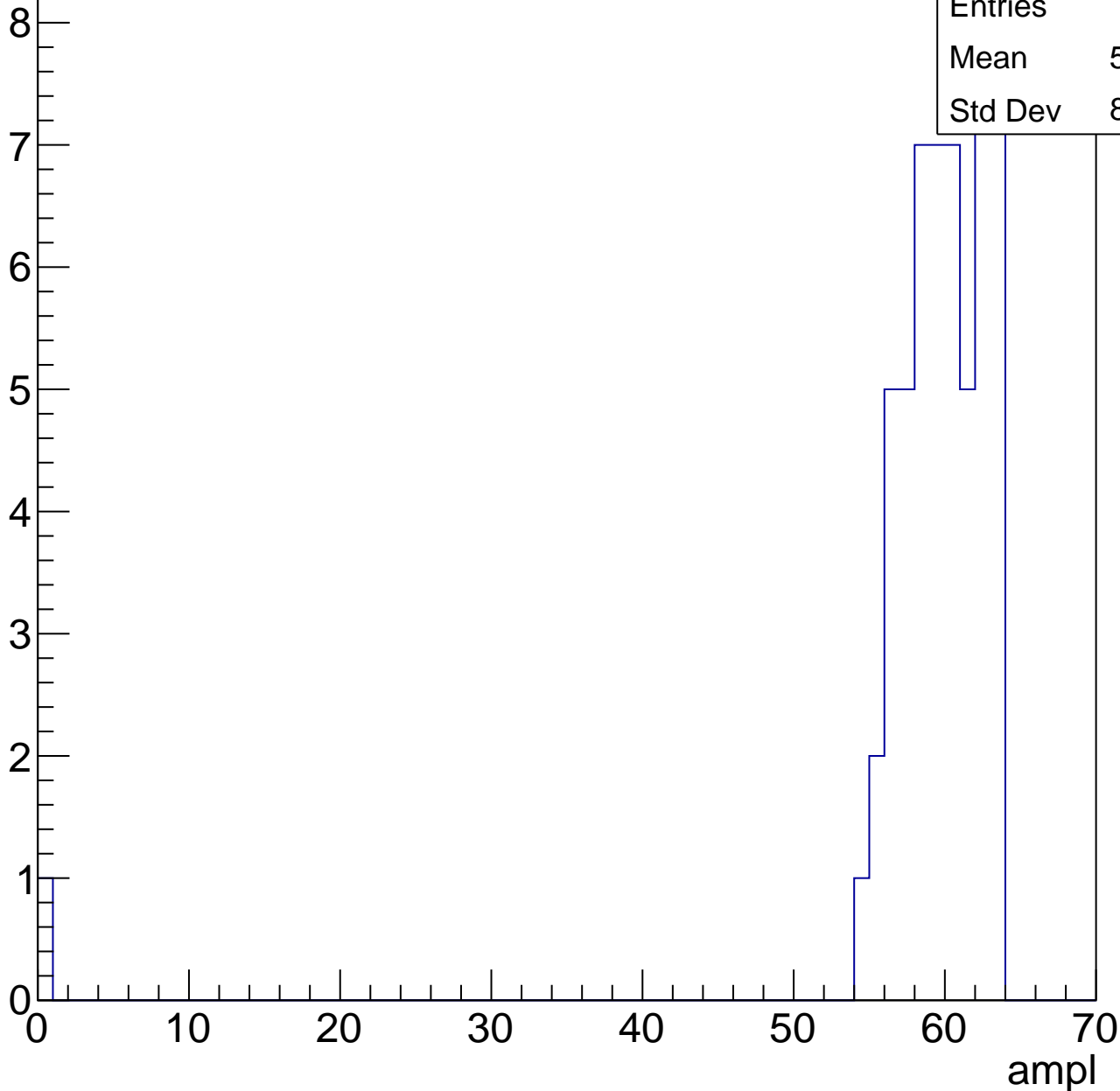


# B1L103S, U2-ch86, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

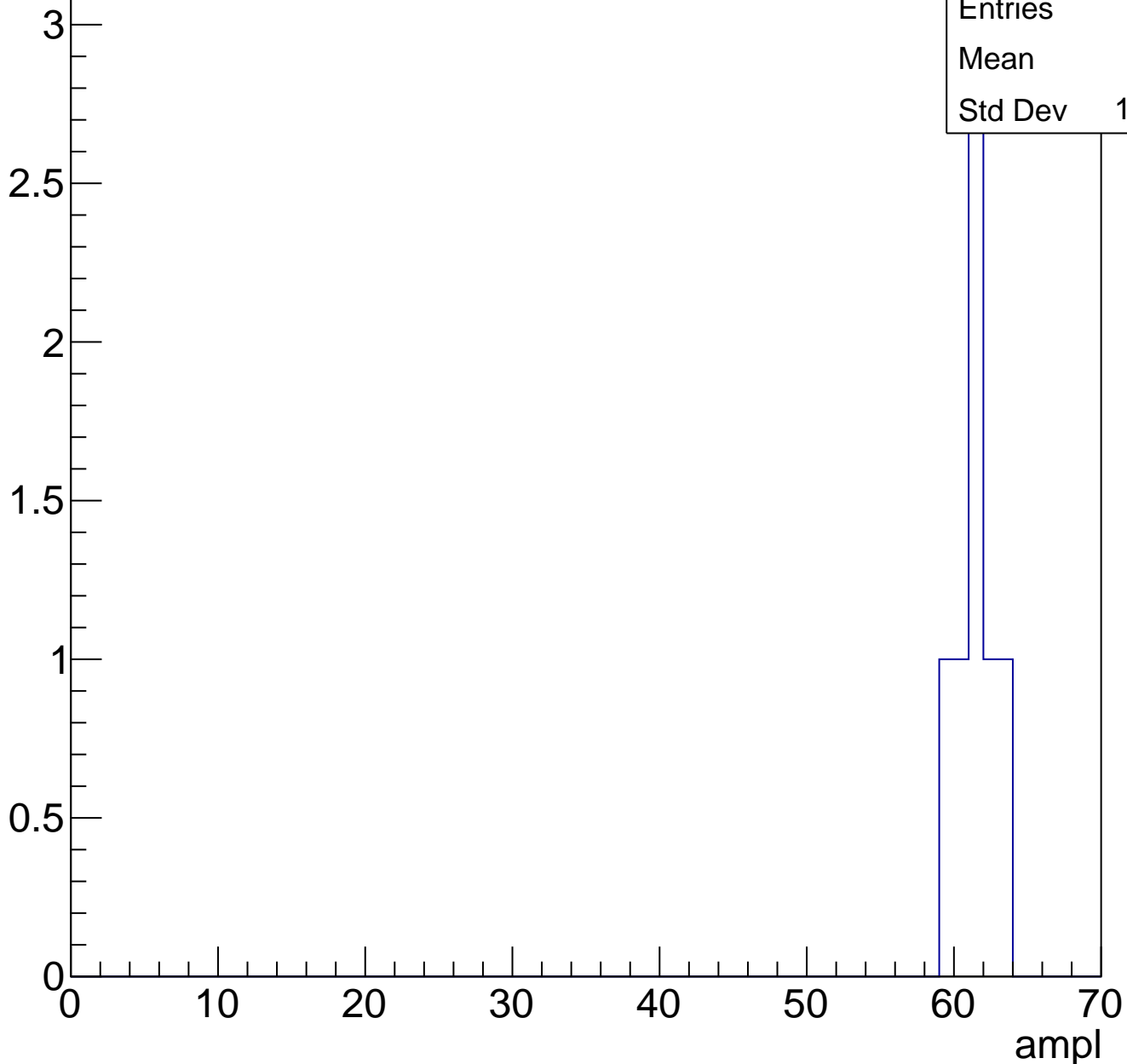
Entries	56
Mean	58.45
Std Dev	8.259



# B1L103S, U2-ch86, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

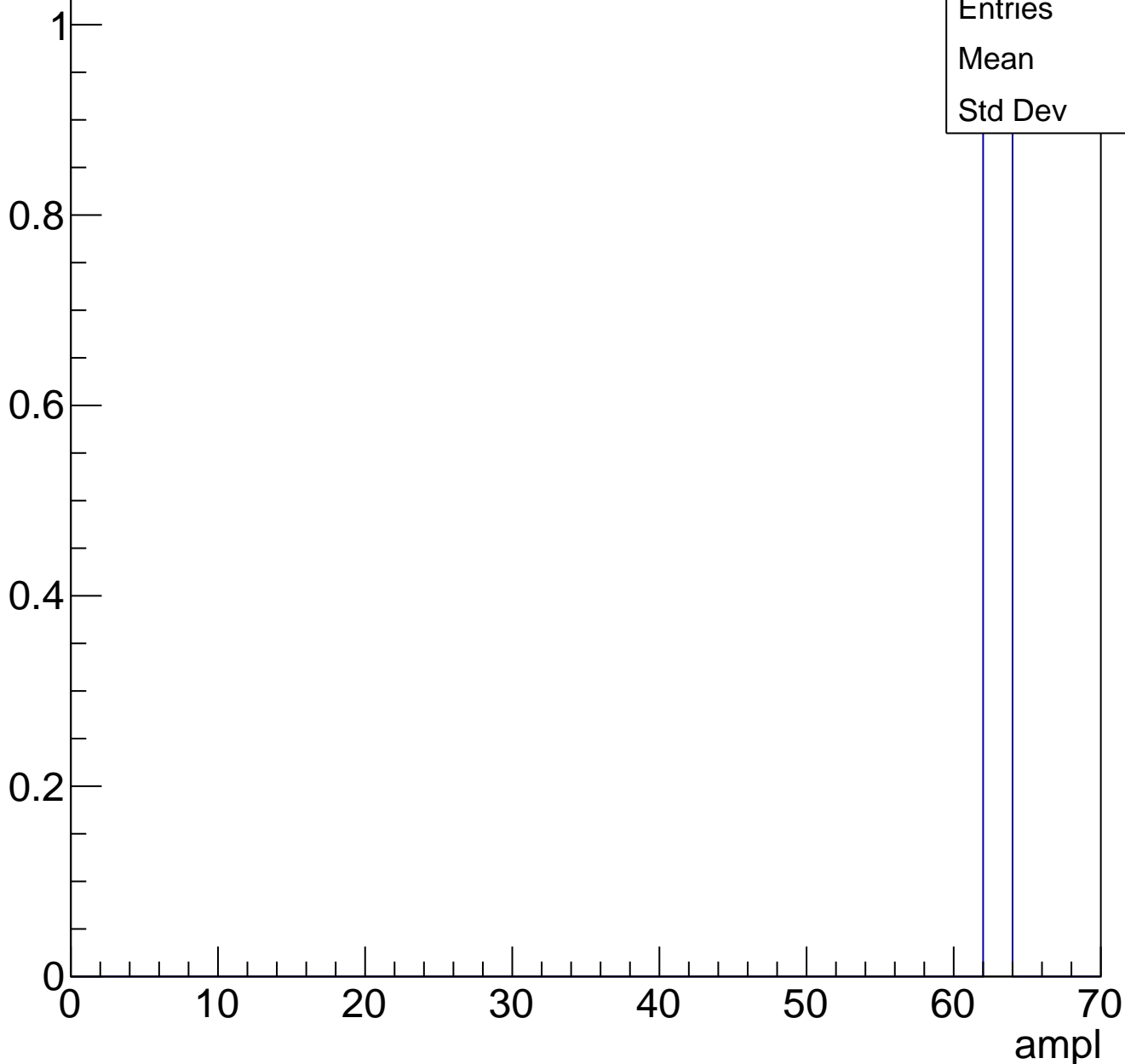




# B1L103S, U2-ch86, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch87, adc0

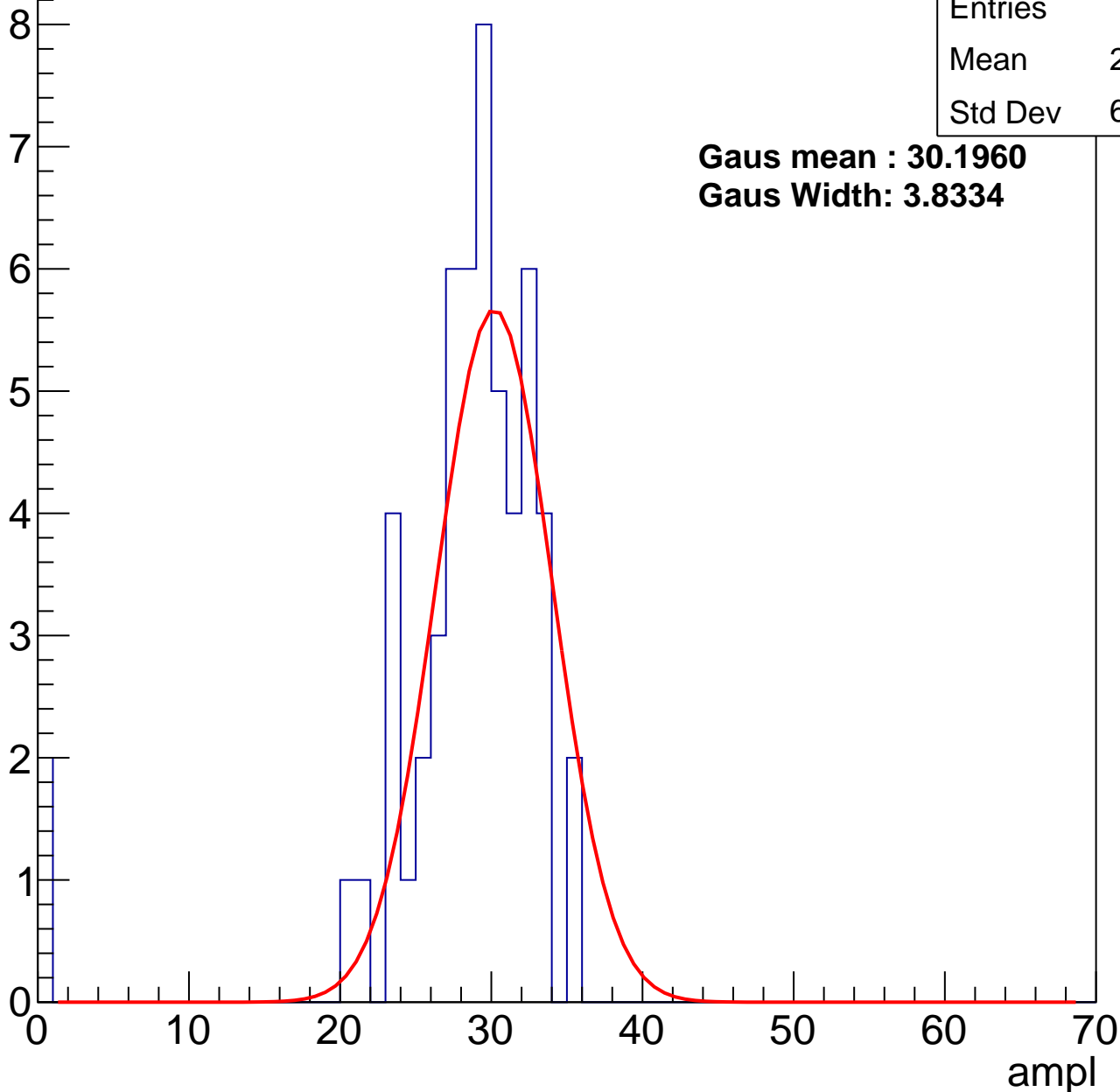
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	27.55
Std Dev	6.295

**Gaus mean : 30.160**

**Gaus Width: 3.8334**



# B1L103S, U2-ch87, adc1

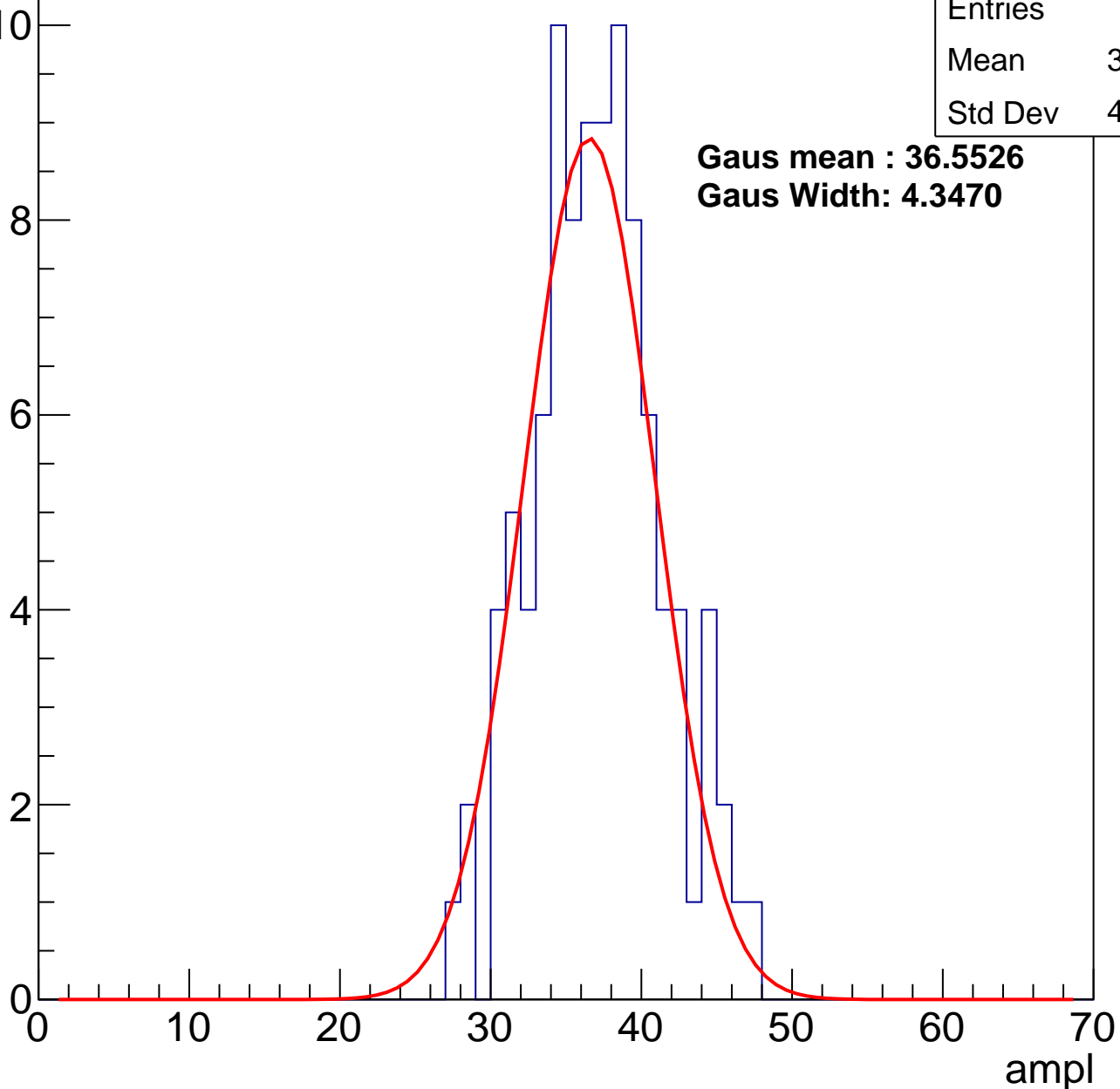
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	99
Mean	36.64
Std Dev	4.208

**Gaus mean : 36.5526**

**Gaus Width: 4.3470**



# B1L103S, U2-ch87, adc2

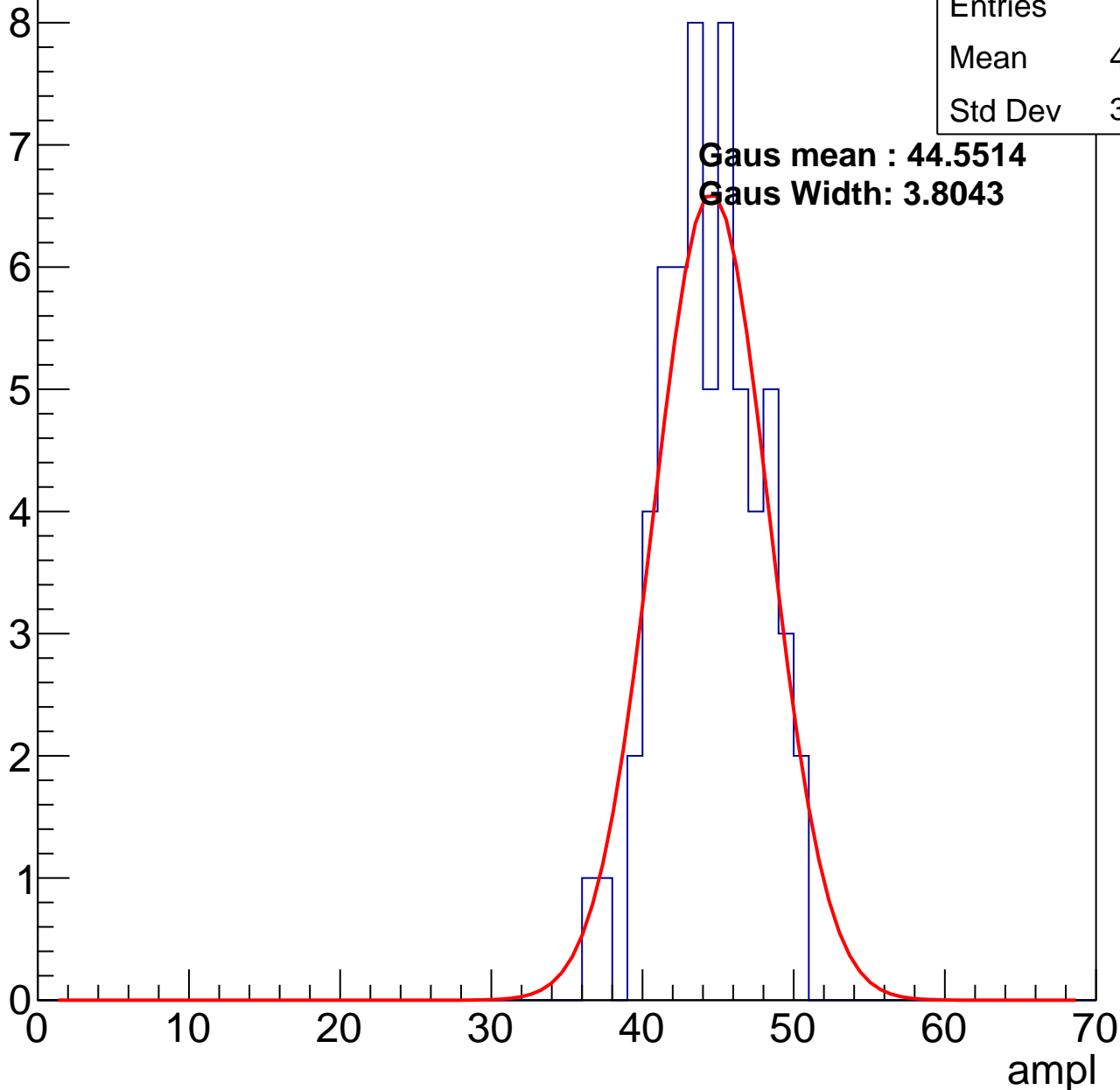
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	43.97
Std Dev	3.173

**Gaus mean : 44.5514**

**Gaus Width: 3.8043**

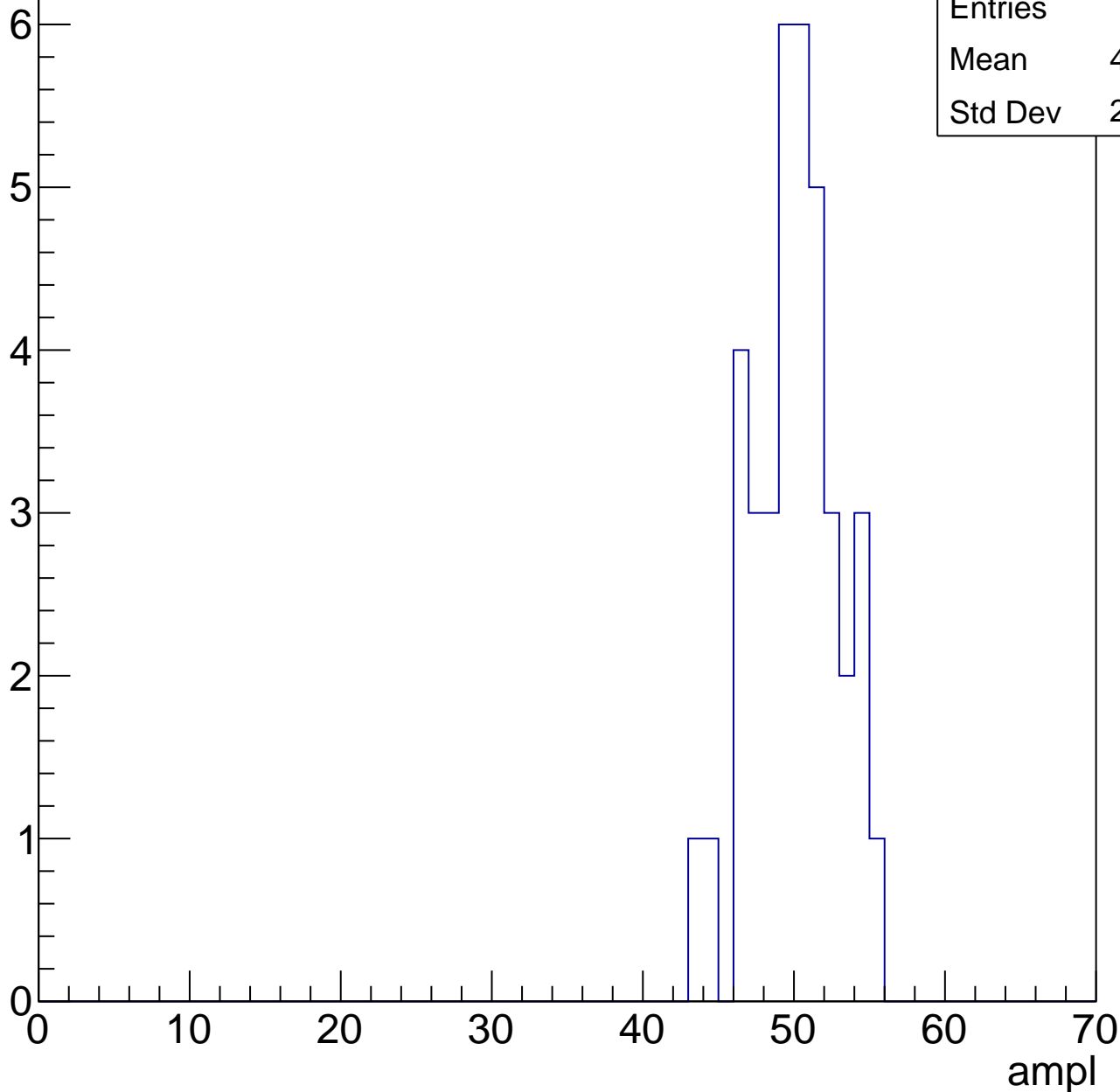


# B1L103S, U2-ch87, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	38
Mean	49.58
Std Dev	2.787

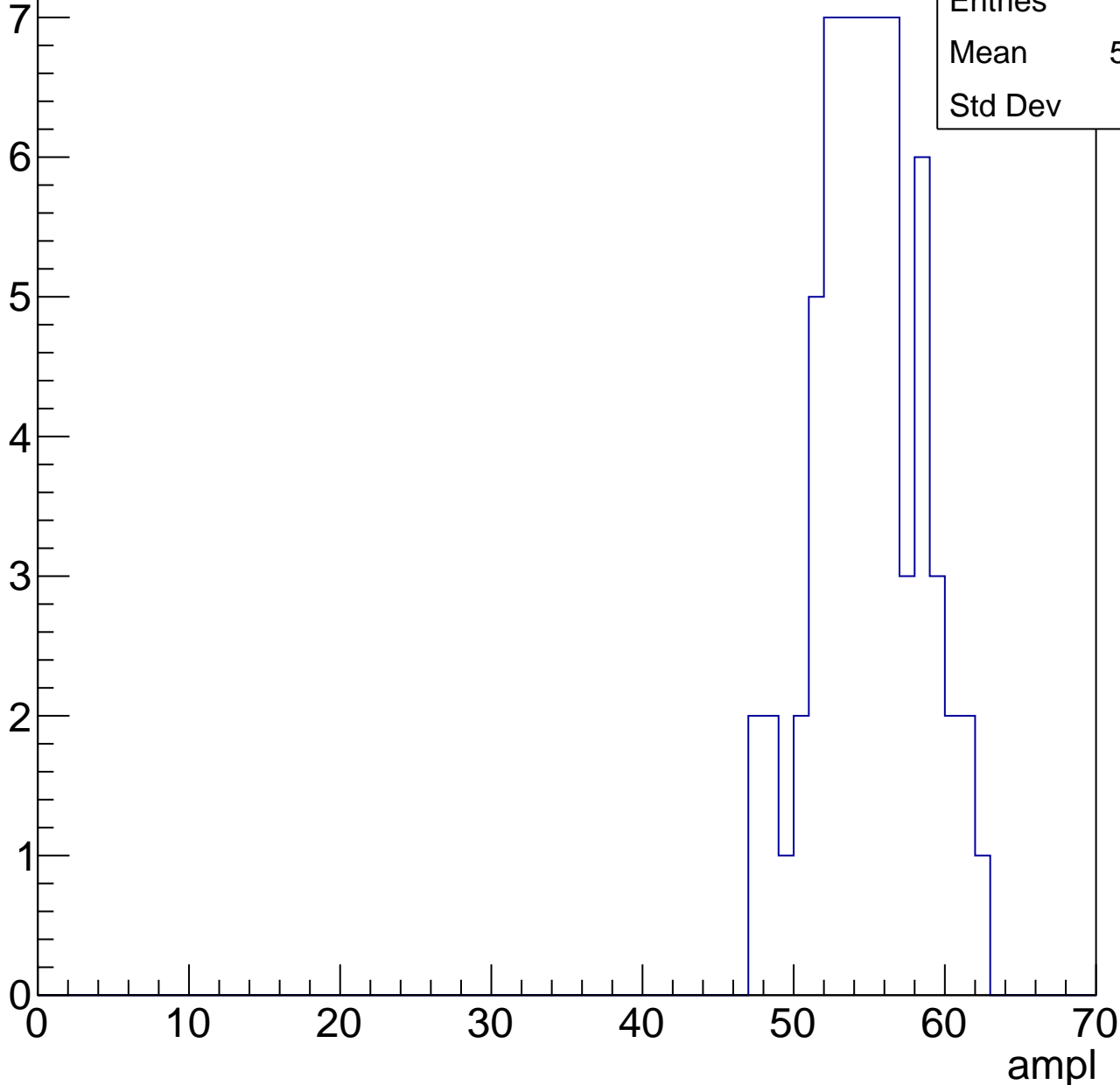


# B1L103S, U2-ch87, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	54.44
Std Dev	3.45

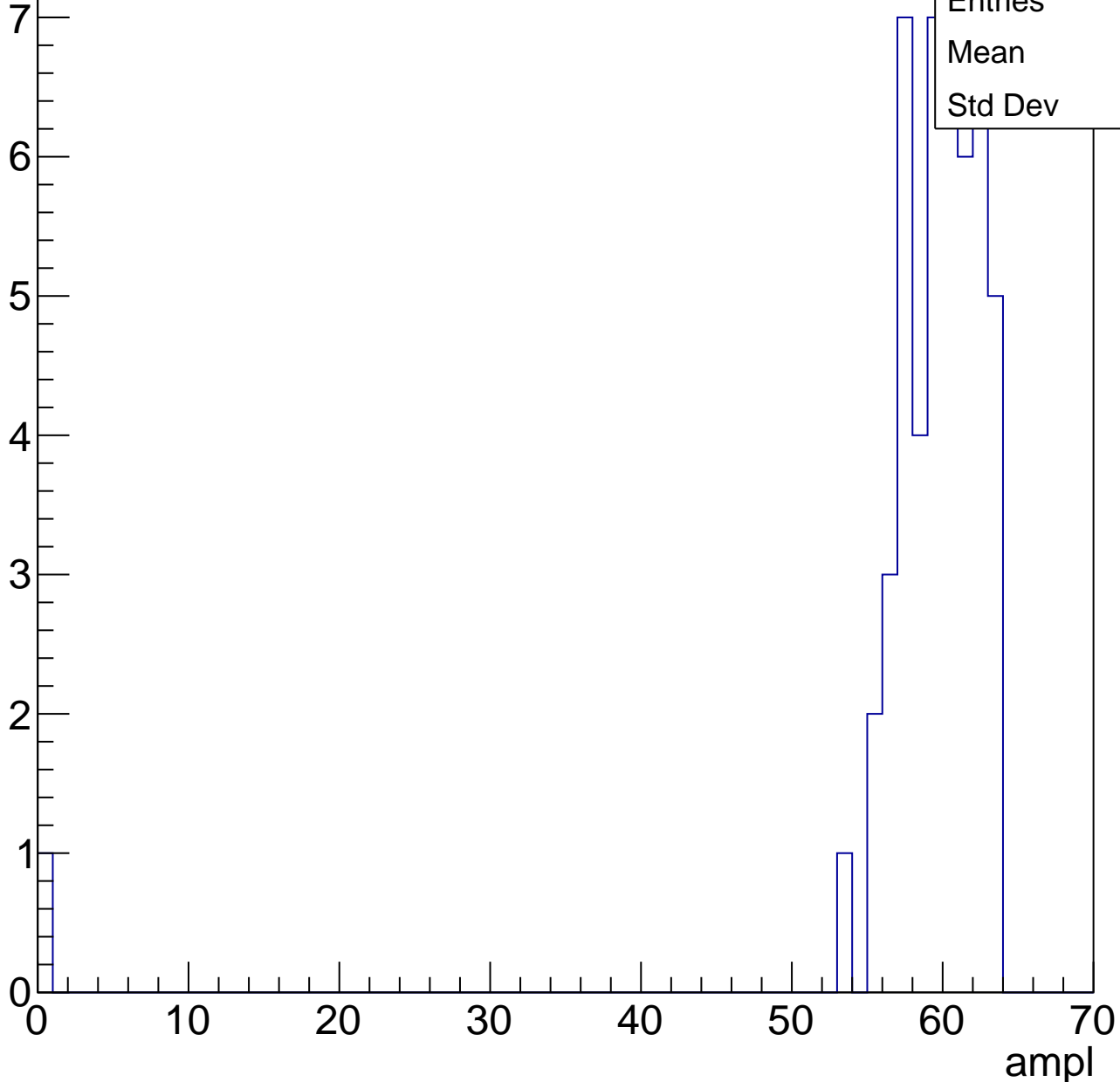


# B1L103S, U2-ch87, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	58.2
Std Dev	8.66

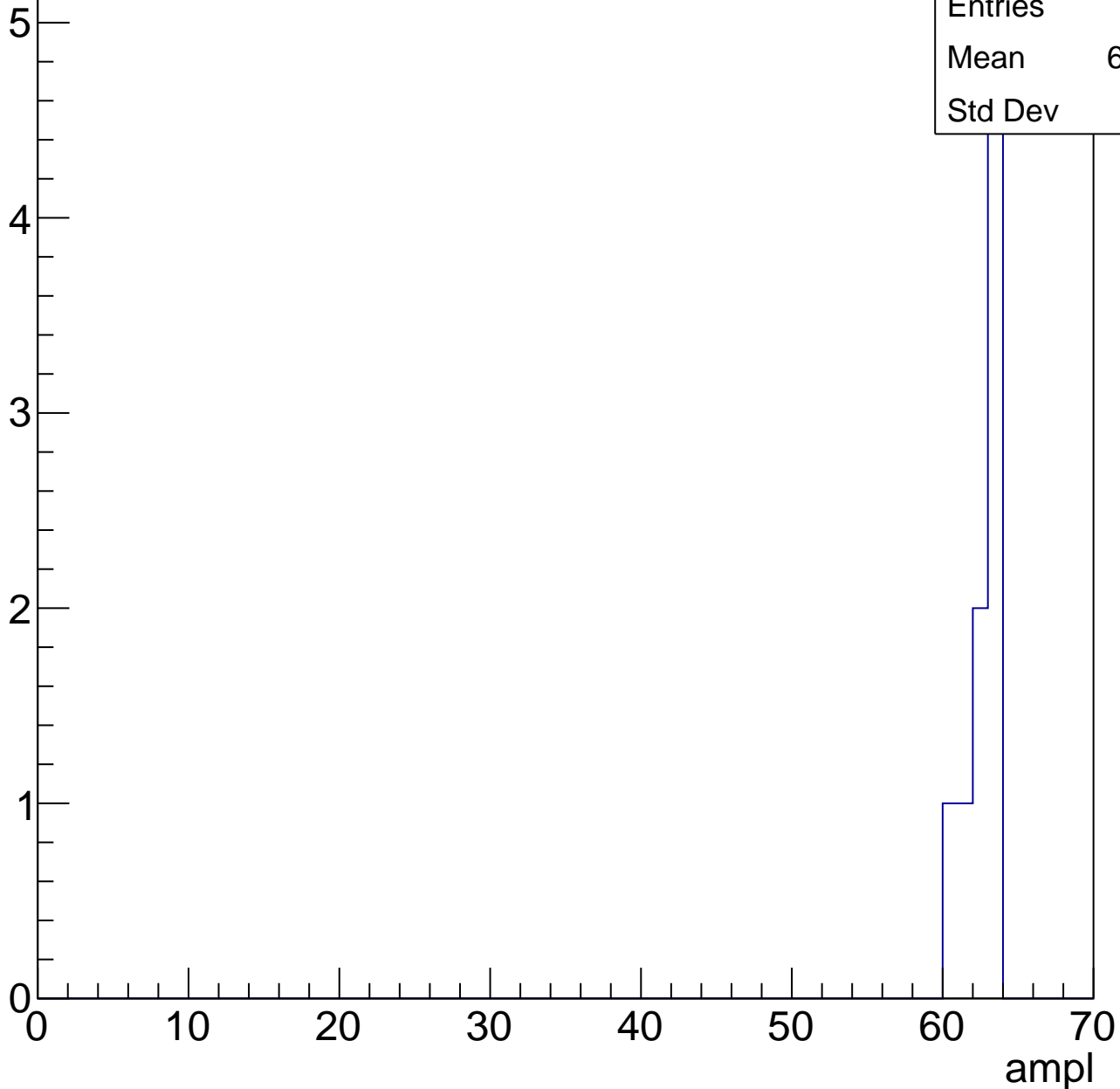


# B1L103S, U2-ch87, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	9
Mean	62.22
Std Dev	1.03

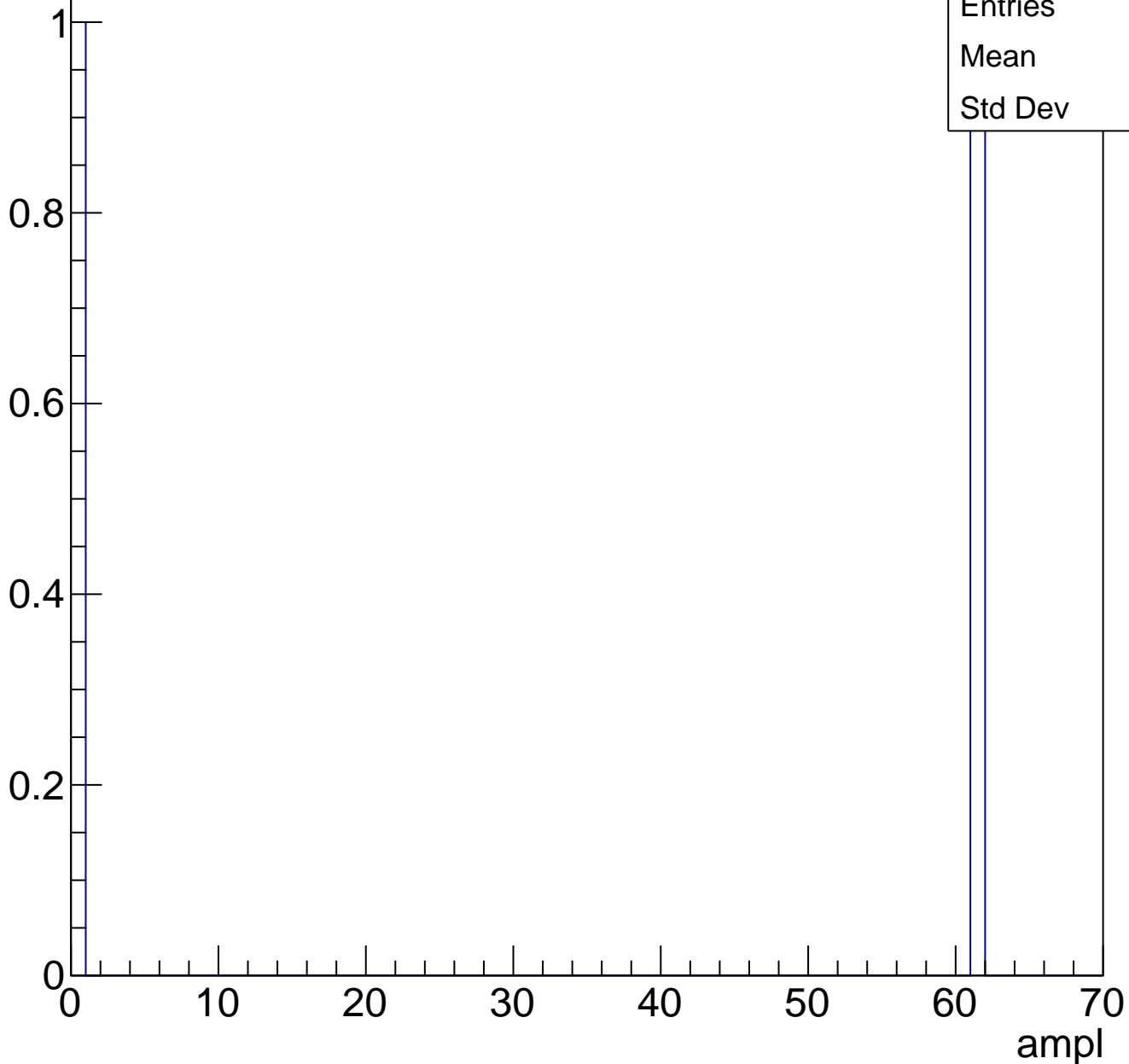




# B1L103S, U2-ch87, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch88, adc0

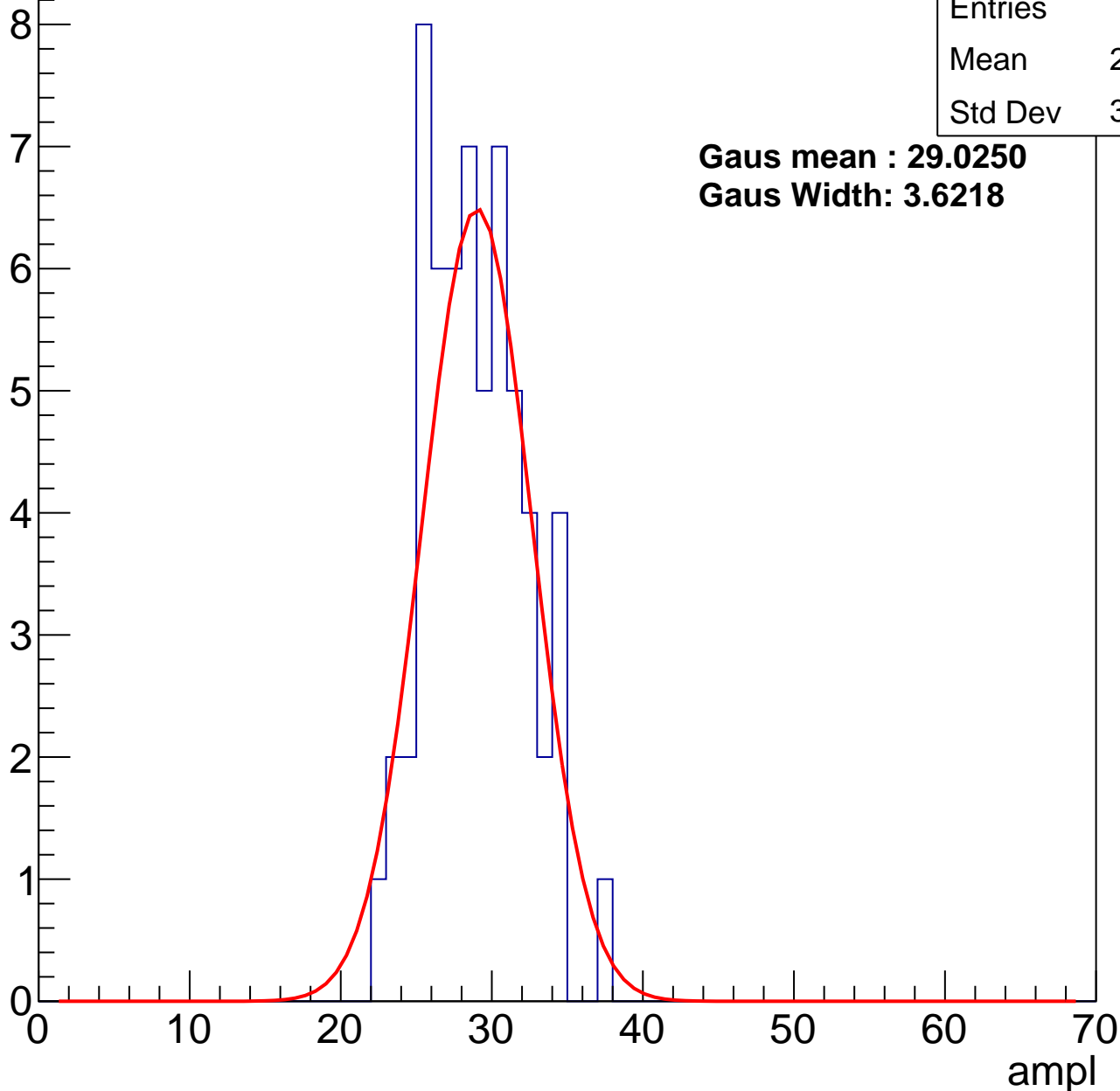
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	28.45
Std Dev	3.227

**Gaus mean : 29.0250**

**Gaus Width: 3.6218**



# B1L103S, U2-ch88, adc1

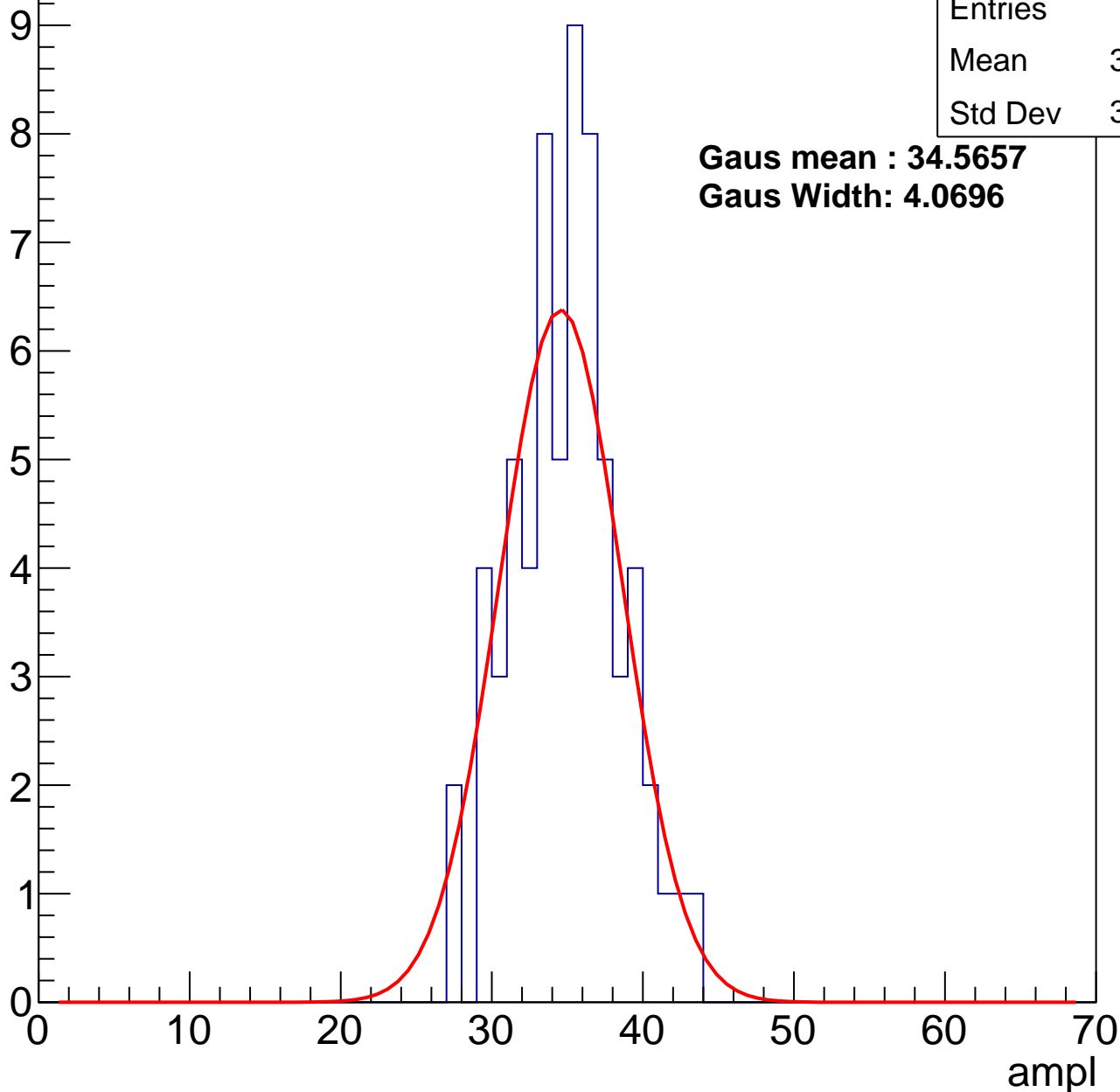
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	34.48
Std Dev	3.509

**Gaus mean : 34.5657**

**Gaus Width: 4.0696**



# B1L103S, U2-ch88, adc2

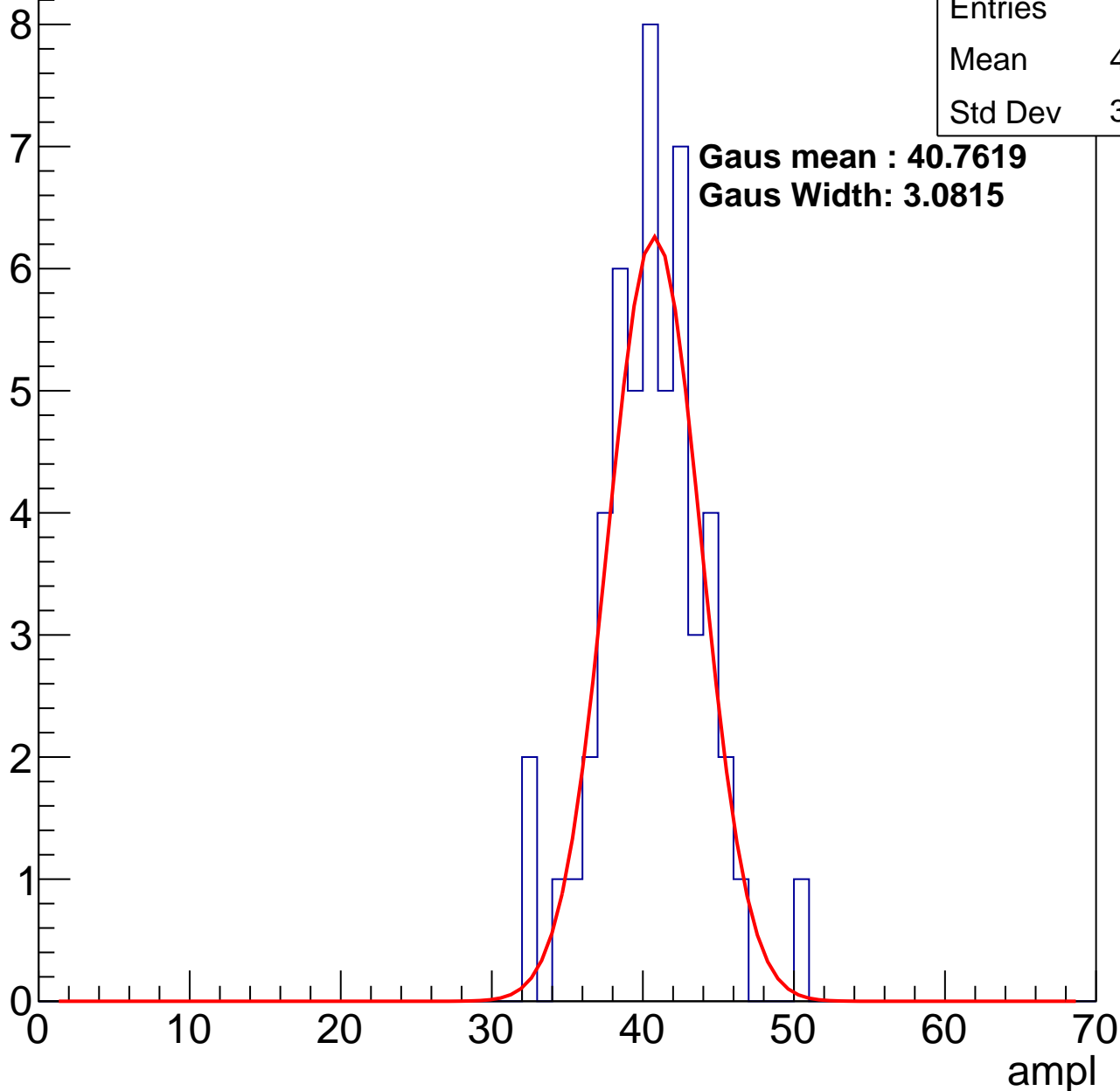
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	40.12
Std Dev	3.384

**Gaus mean : 40.7619**

**Gaus Width: 3.0815**

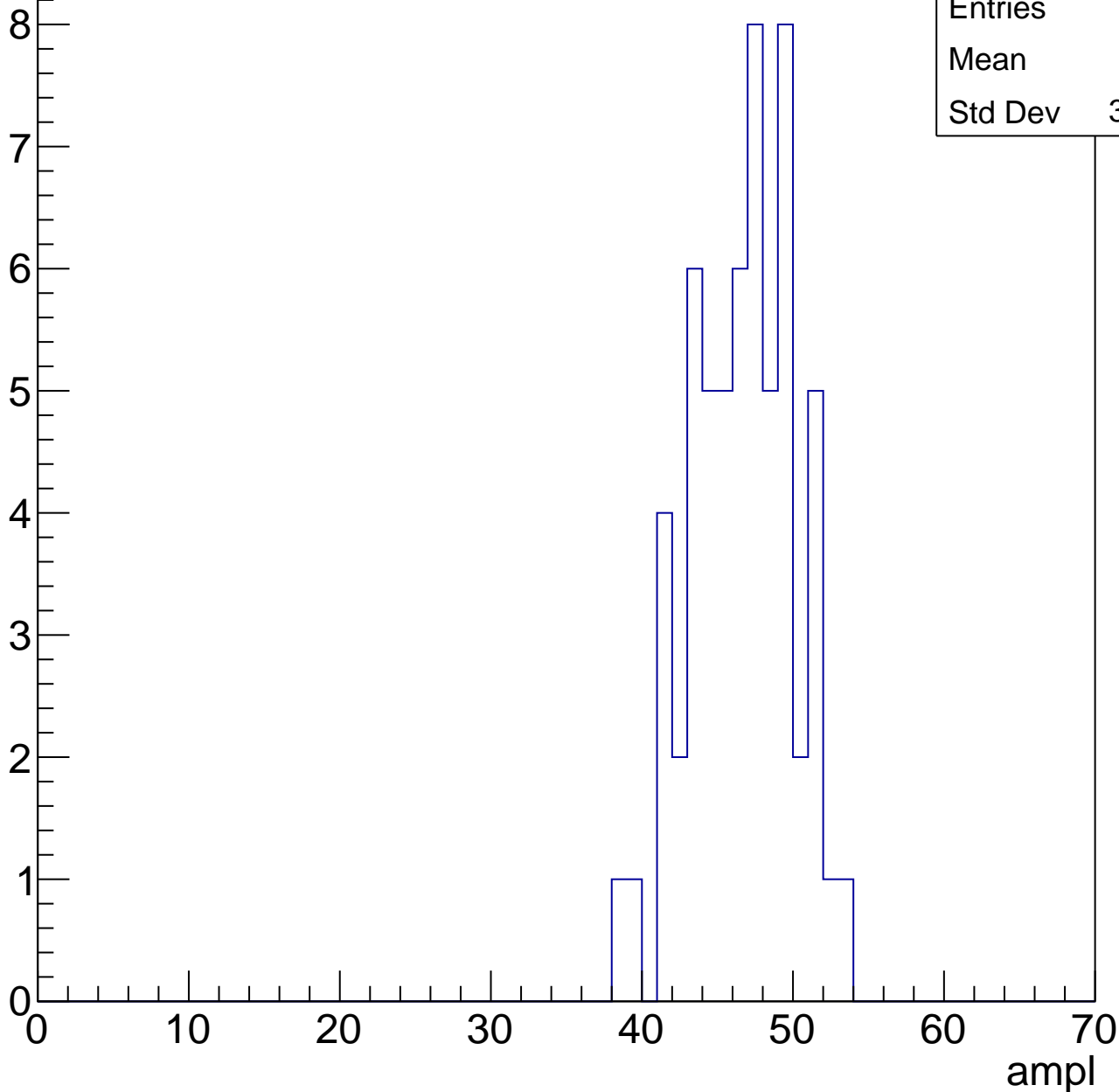


# B1L103S, U2-ch88, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

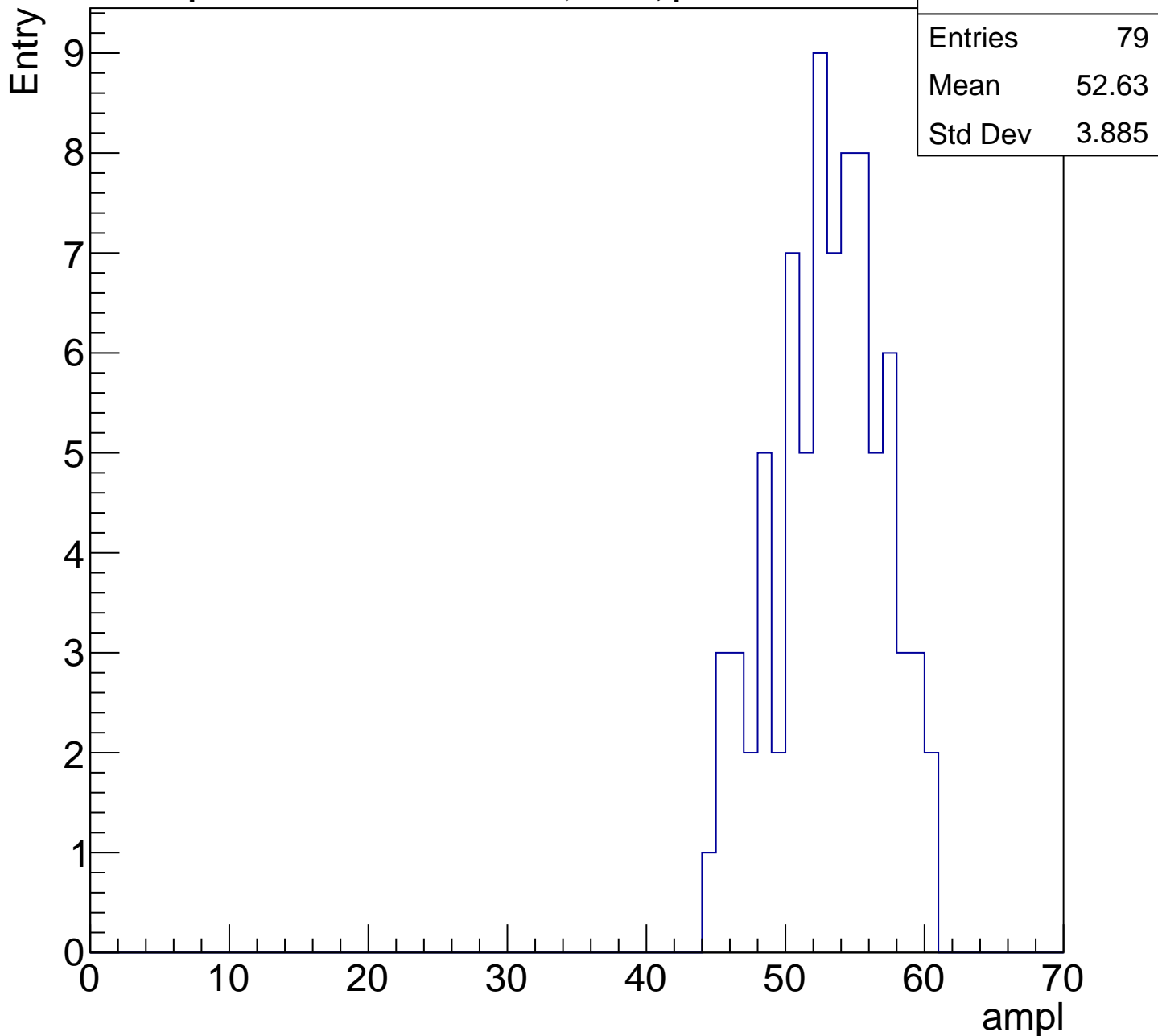
Entry

Entries	60
Mean	46.2
Std Dev	3.326



# B1L103S, U2-ch88, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

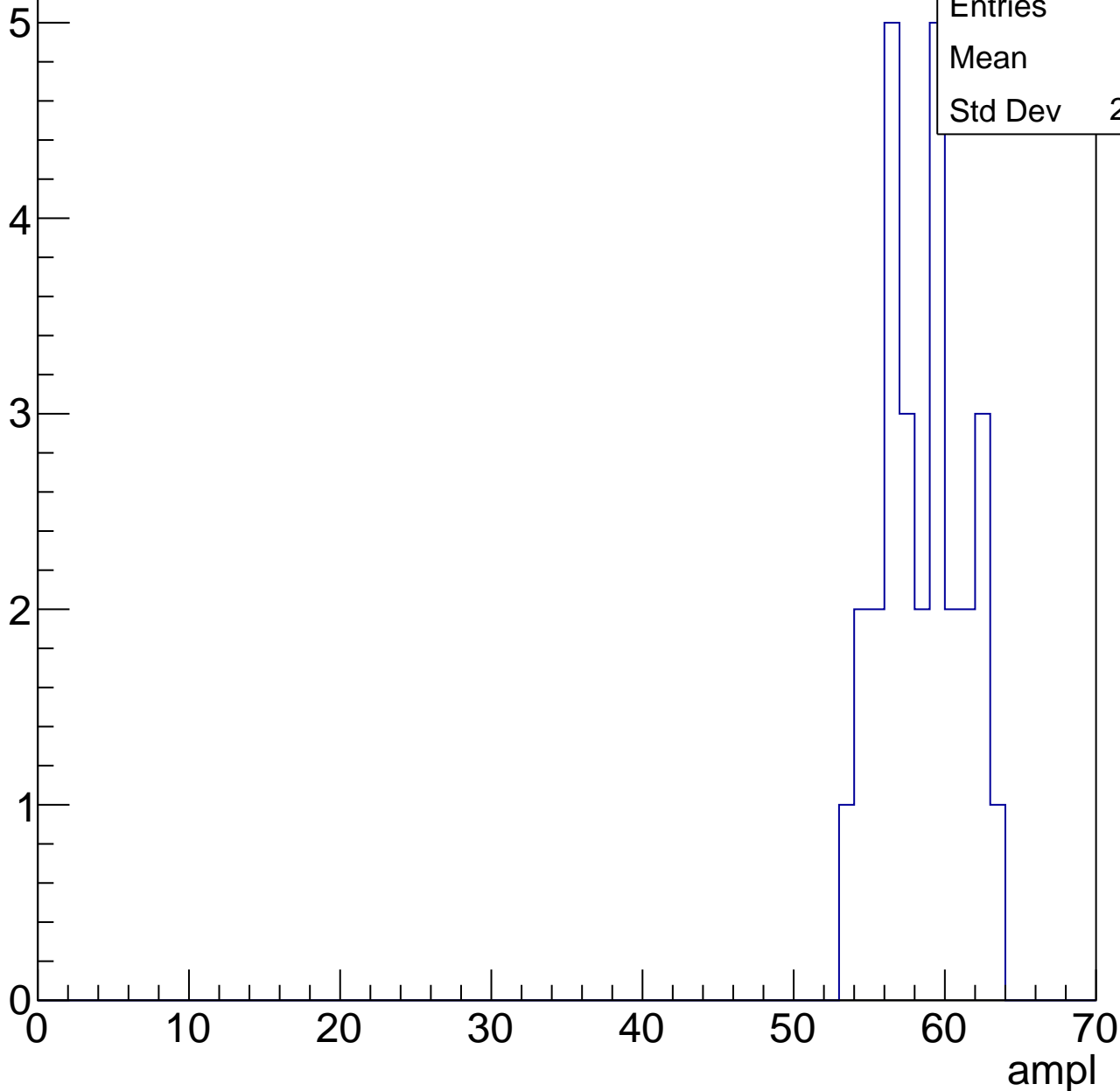


# B1L103S, U2-ch88, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	28
Mean	58
Std Dev	2.686

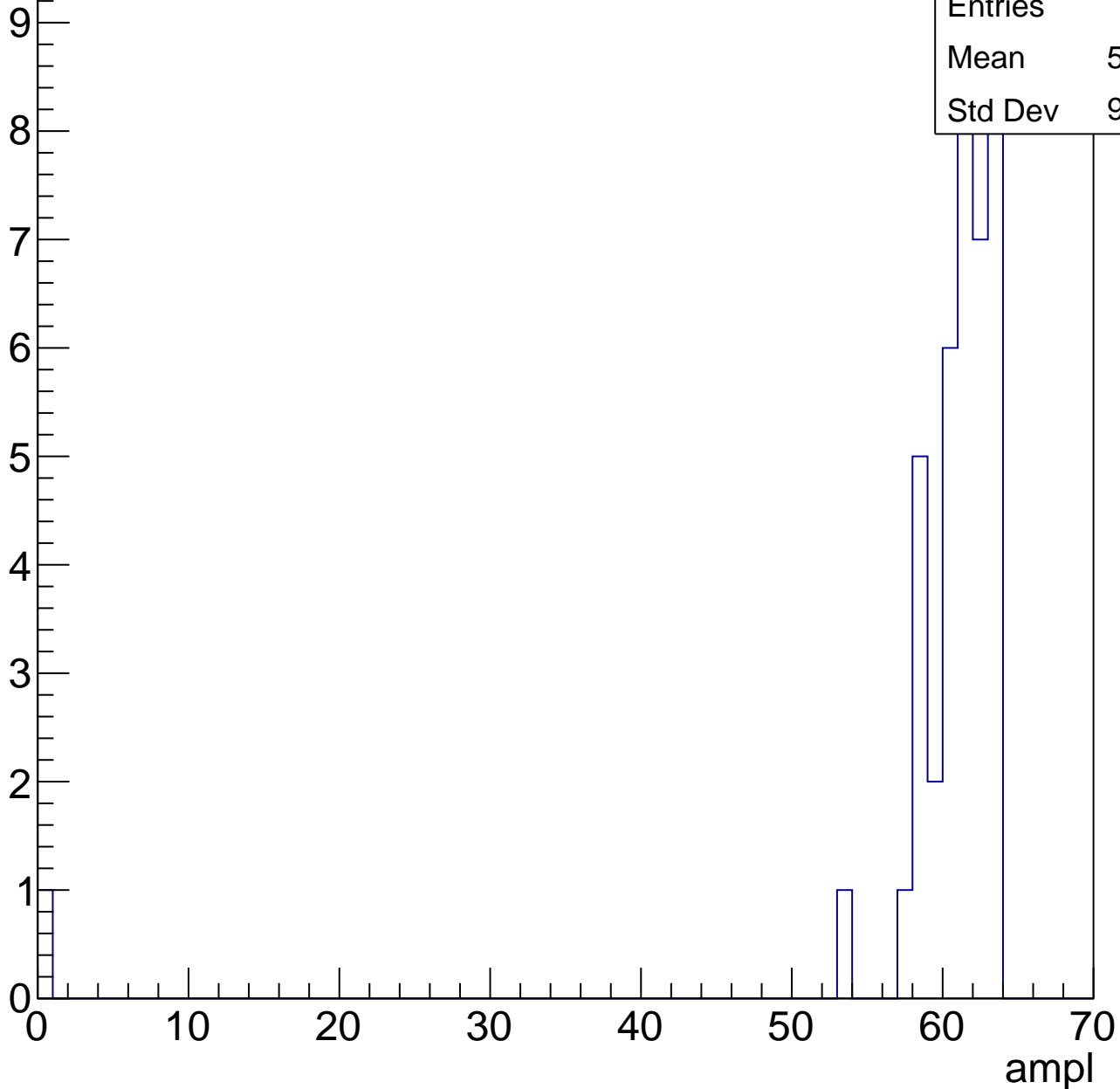


# B1L103S, U2-ch88, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	40
Mean	59.17
Std Dev	9.708

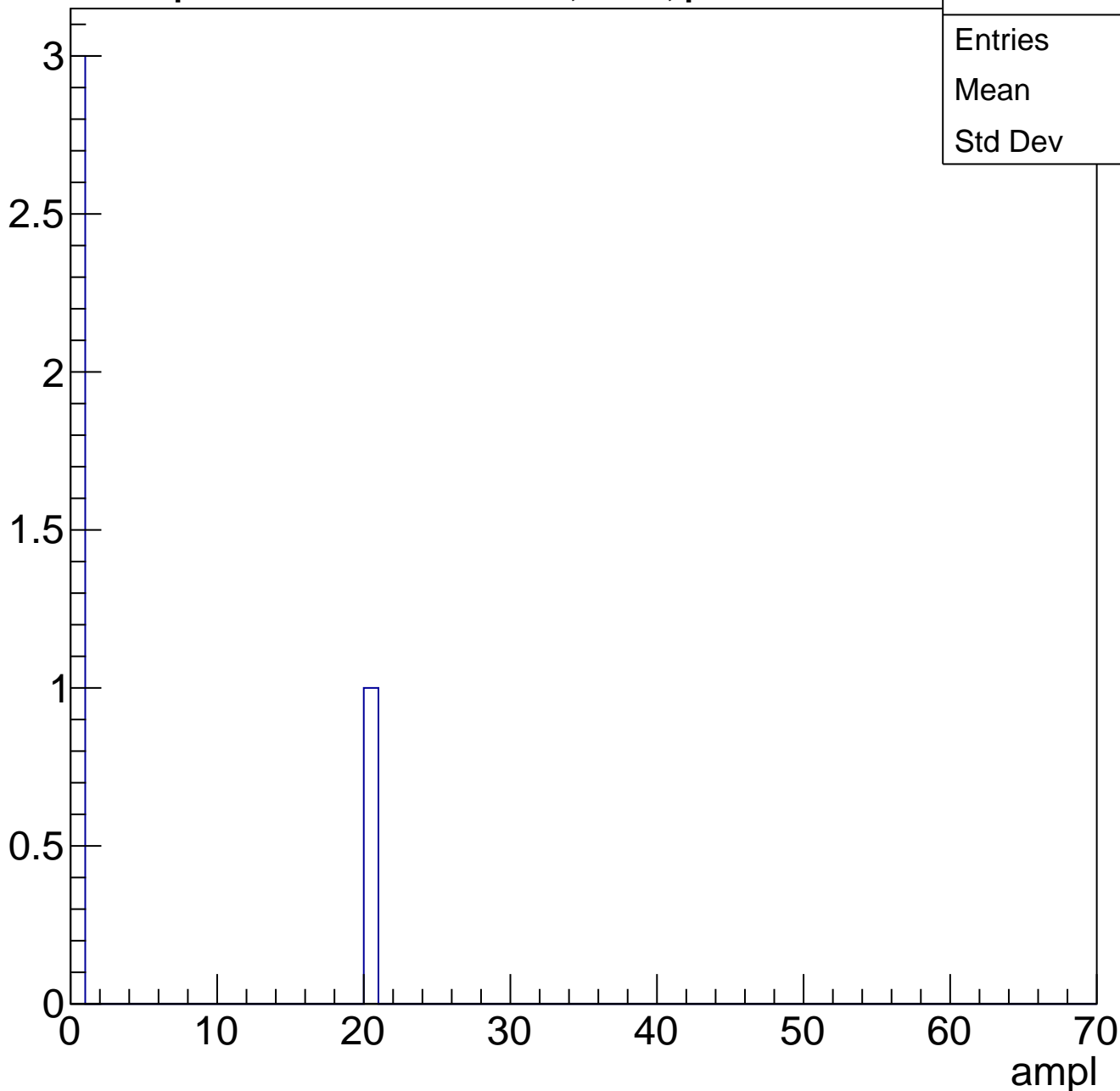




# B1L103S, U2-ch88, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	4
Mean	5
Std Dev	8.66

# B1L103S, U2-ch89, adc0

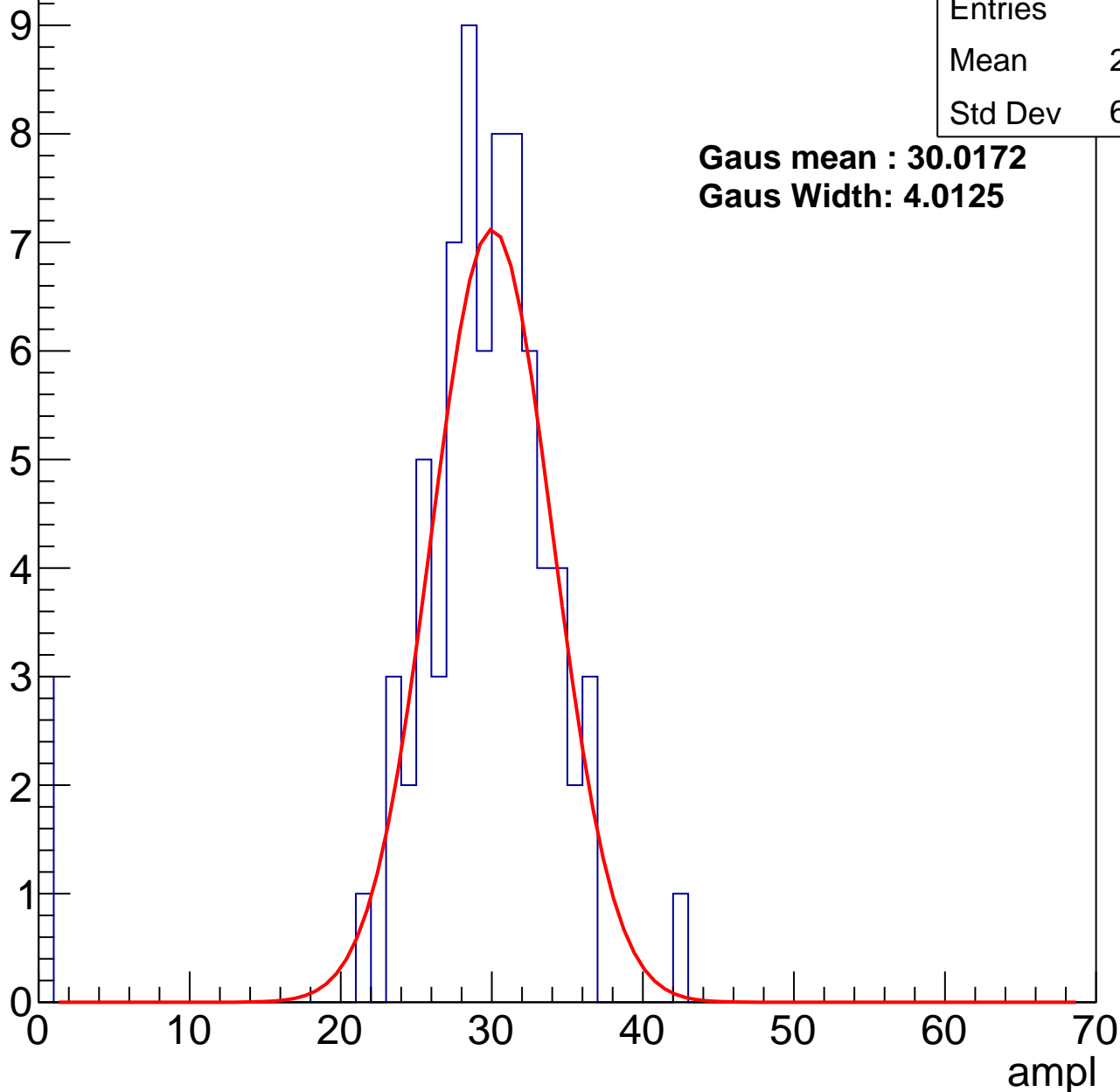
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	28.32
Std Dev	6.832

**Gaus mean : 30.0172**

**Gaus Width: 4.0125**



# B1L103S, U2-ch89, adc1

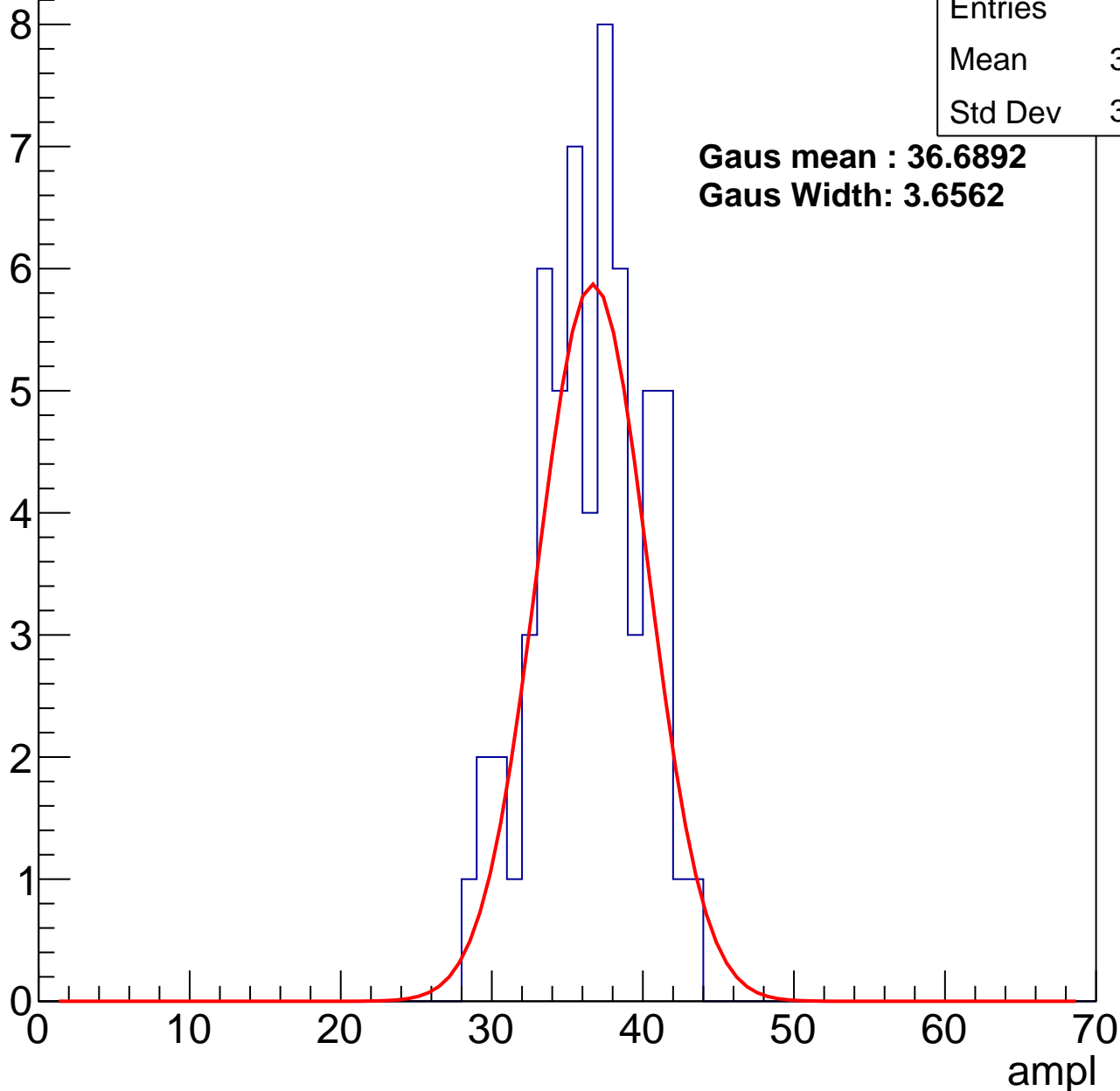
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	36.02
Std Dev	3.505

**Gaus mean : 36.6892**

**Gaus Width: 3.6562**



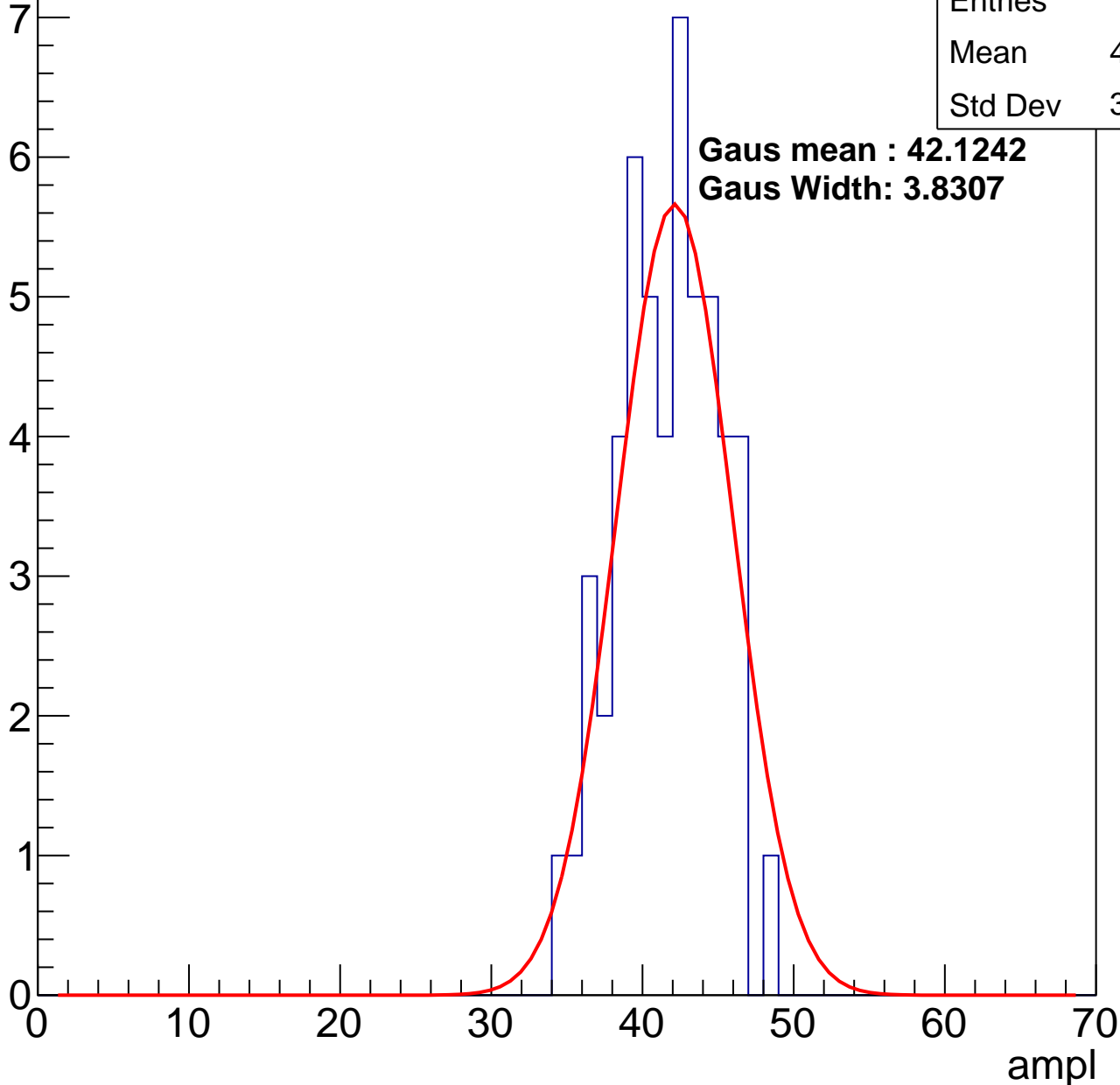
# B1L103S, U2-ch89, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	41.19
Std Dev	3.223

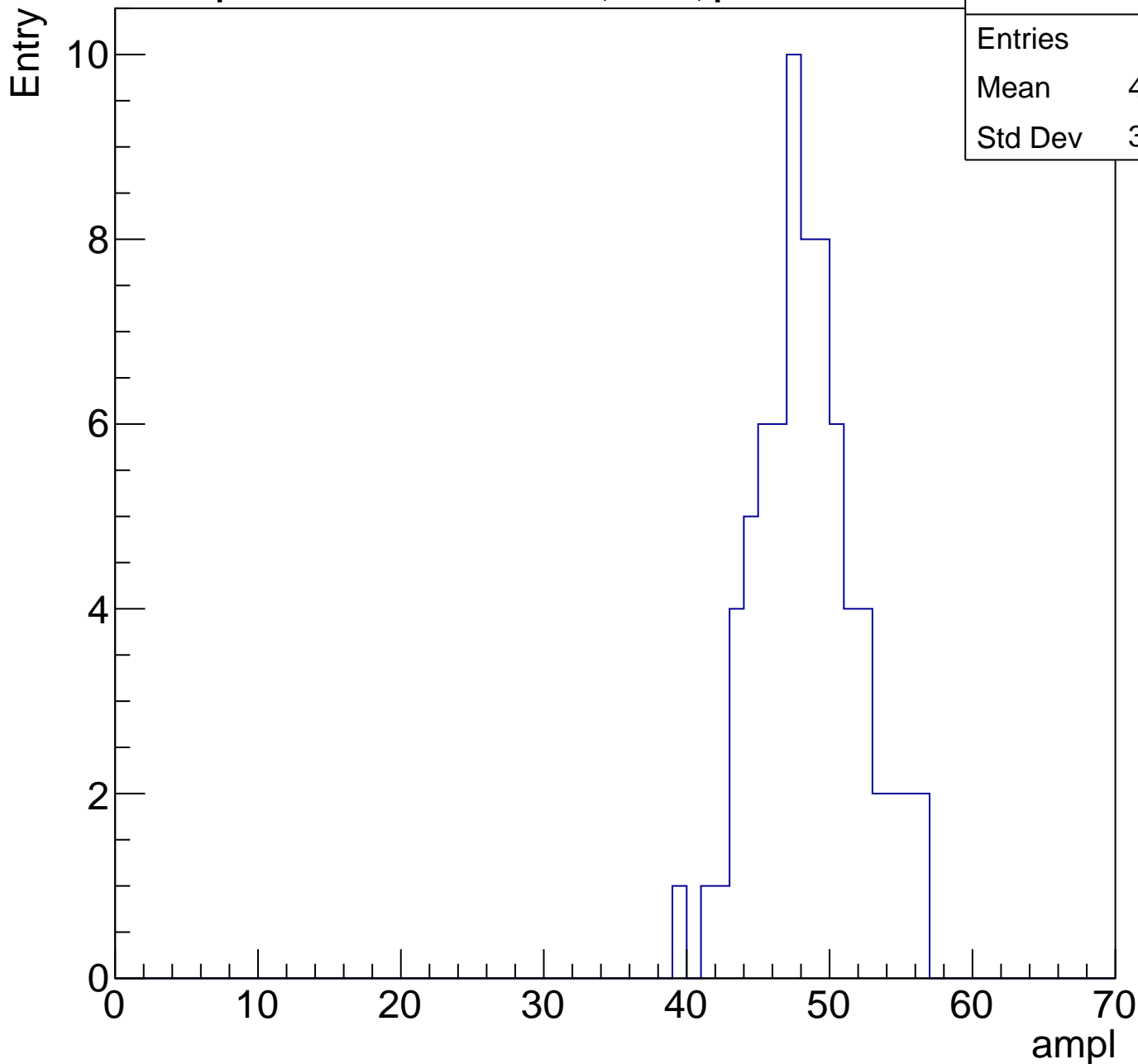
**Gaus mean : 42.1242**  
**Gaus Width: 3.8307**



# B1L103S, U2-ch89, adc3

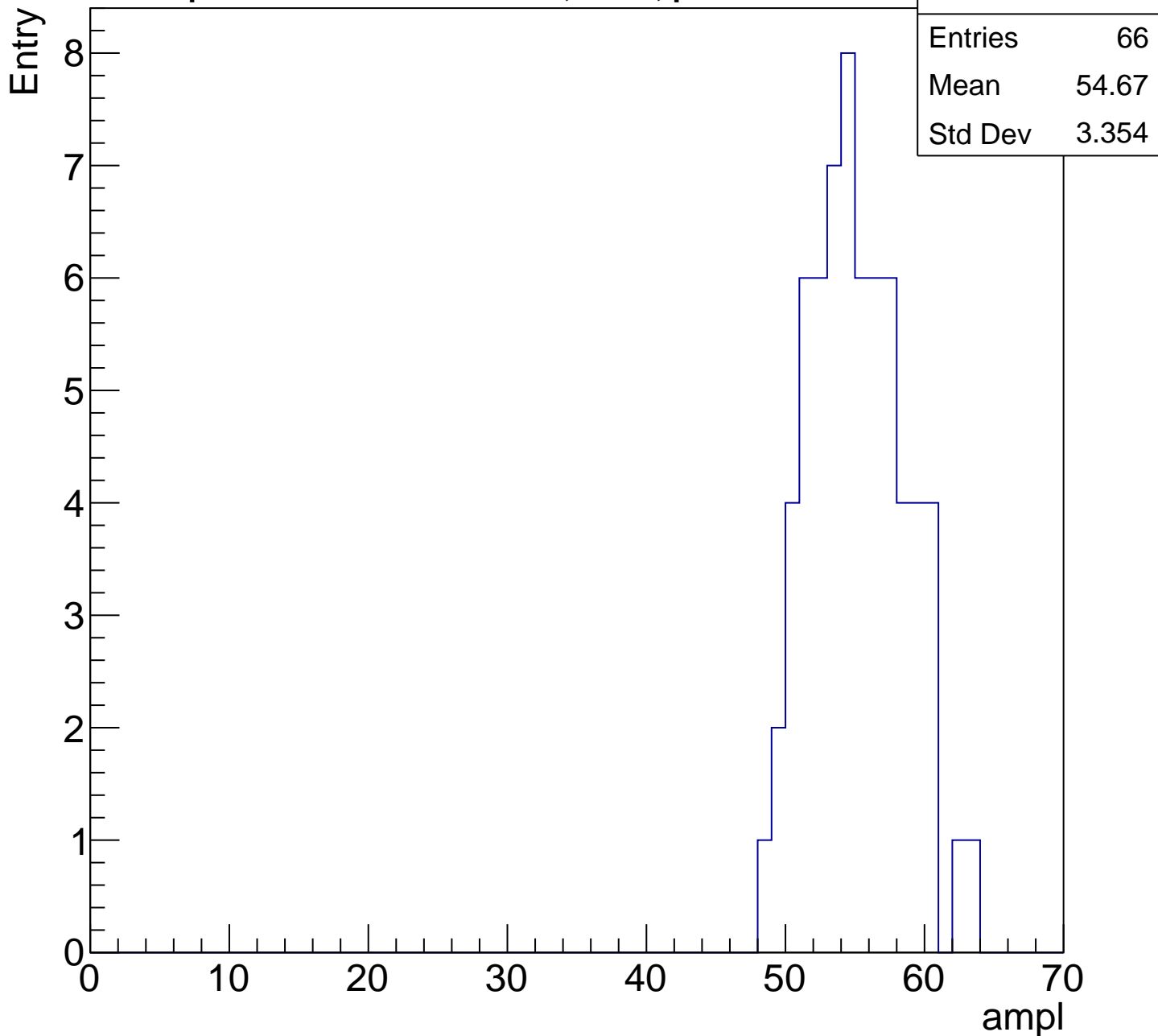
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	72
Mean	47.97
Std Dev	3.563



# B1L103S, U2-ch89, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

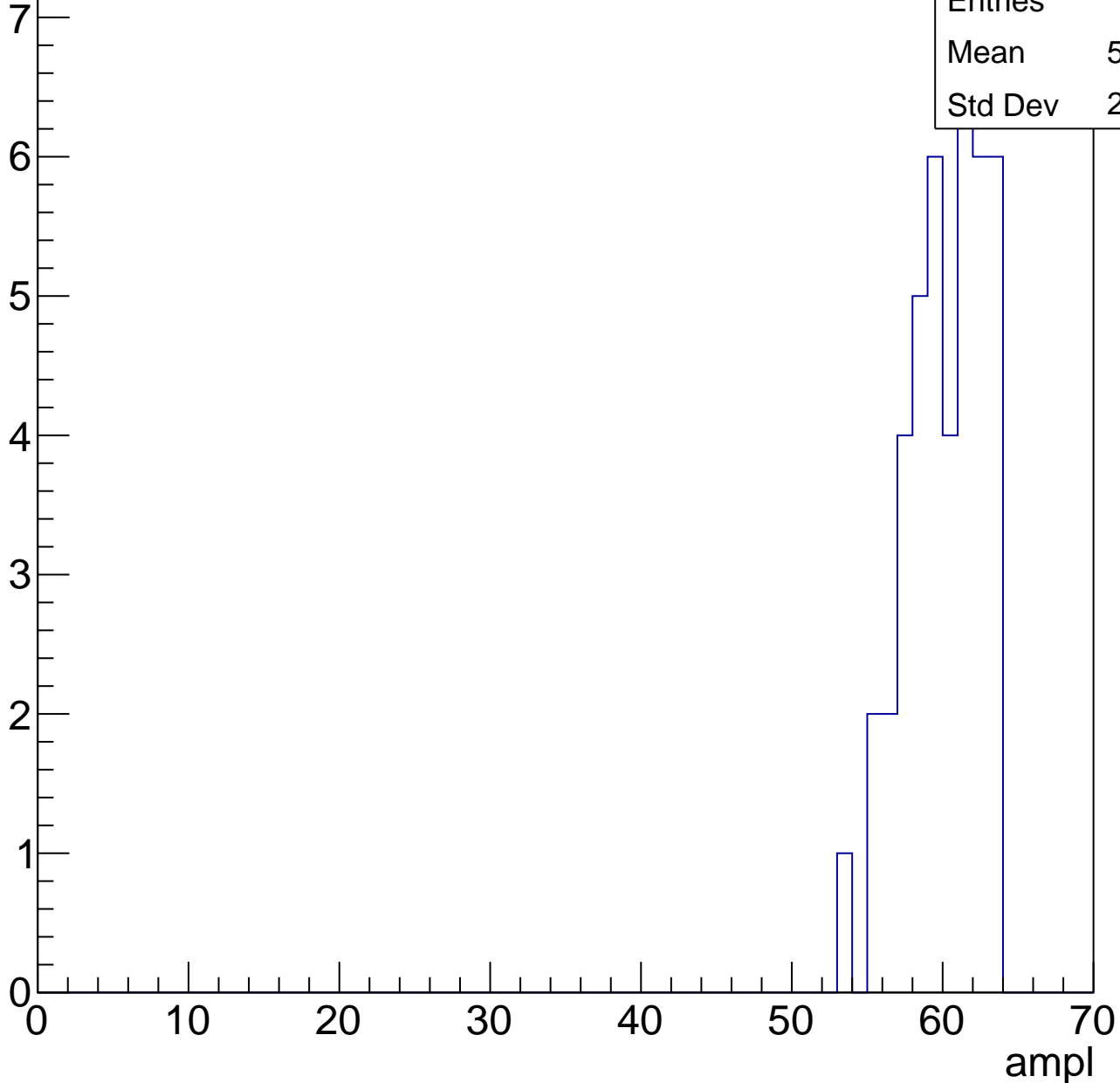


# B1L103S, U2-ch89, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

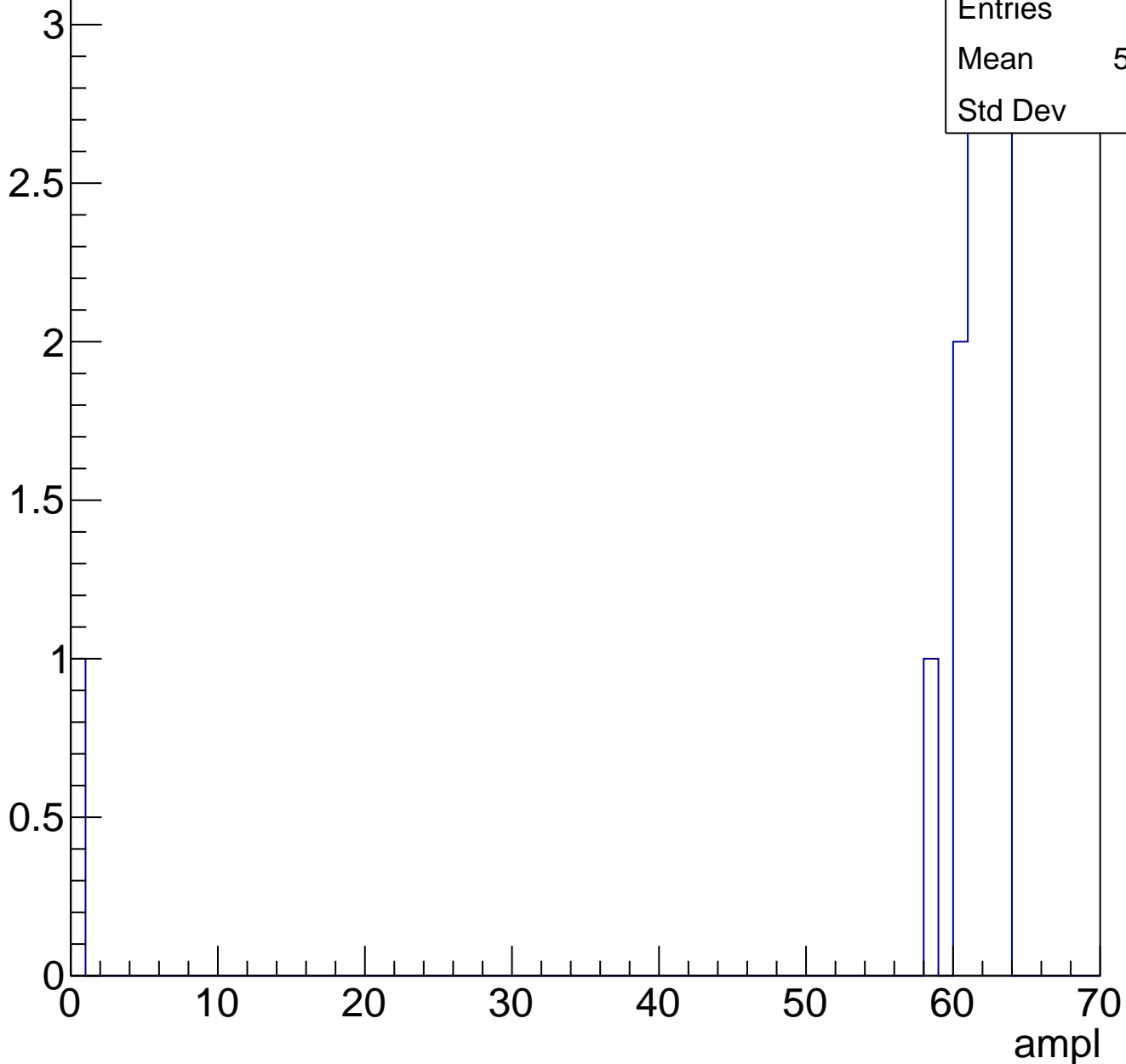
Entries	43
Mean	59.63
Std Dev	2.515



# B1L103S, U2-ch89, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U2-ch89, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U2-ch90, adc0

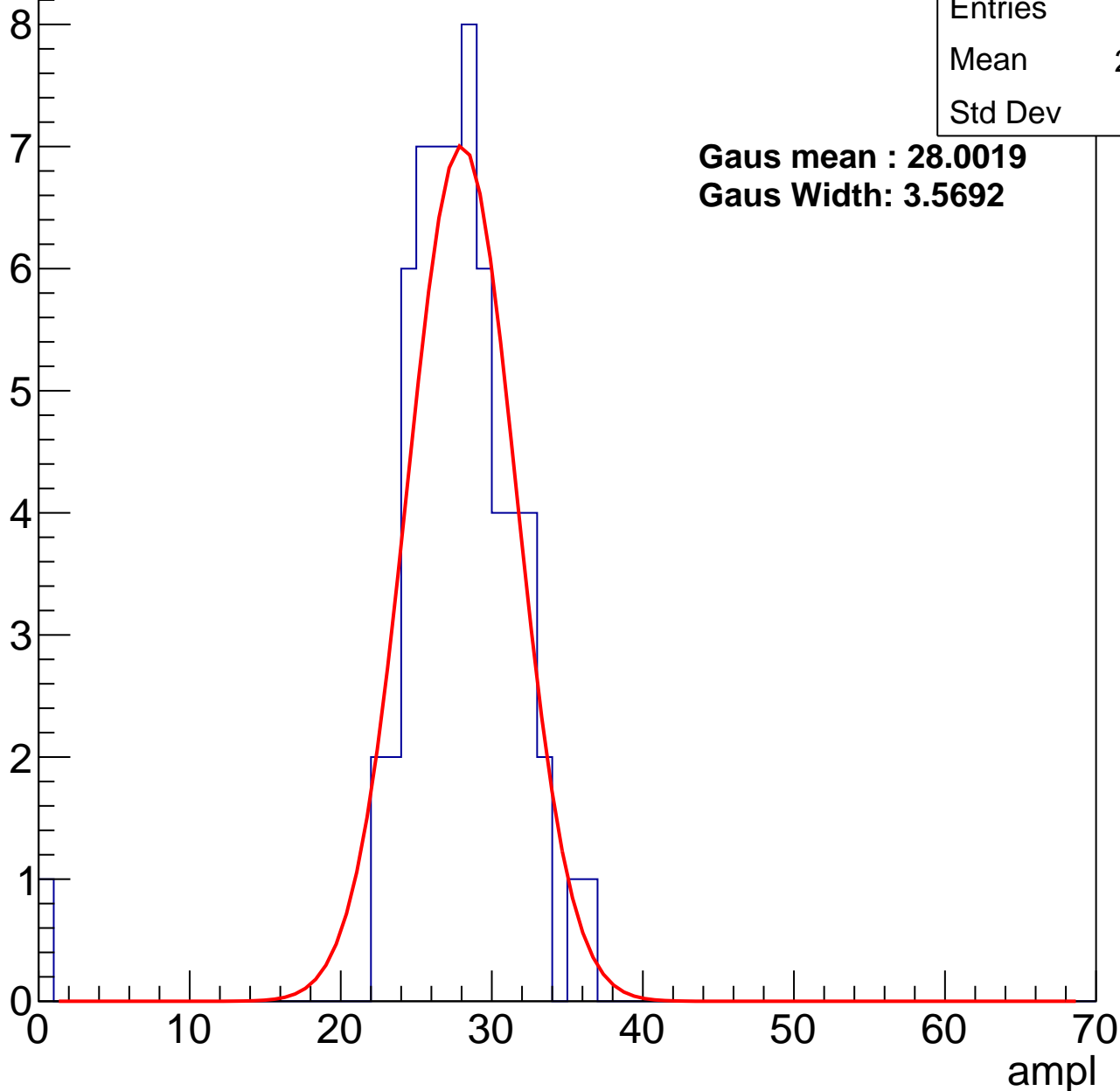
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	27.21
Std Dev	4.66

**Gaus mean : 28.0019**

**Gaus Width: 3.5692**



# B1L103S, U2-ch90, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	70
Mean	33.93
Std Dev	3.275

**Gaus mean : 34.4653**

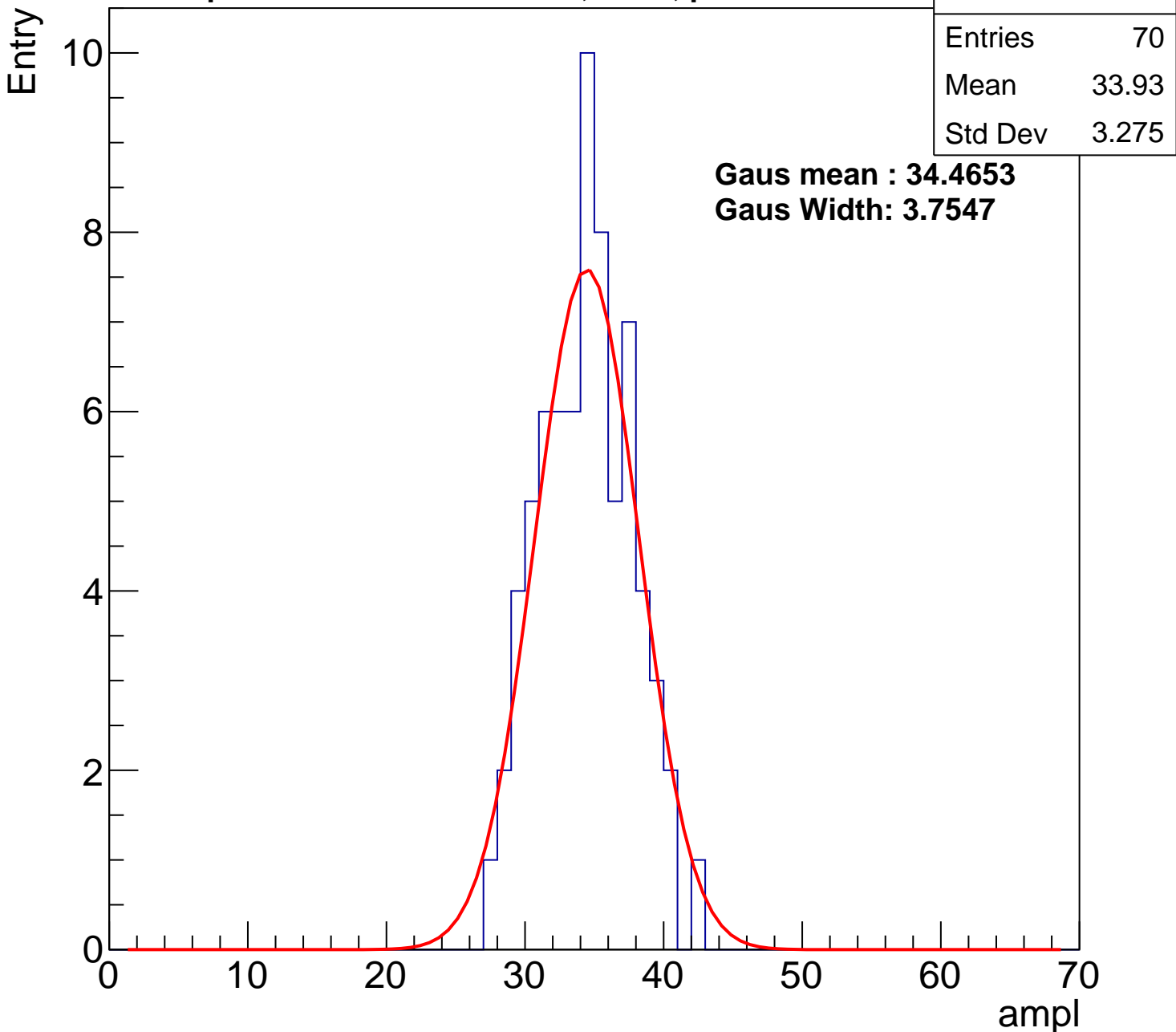
**Gaus Width: 3.7547**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U2-ch90, adc2

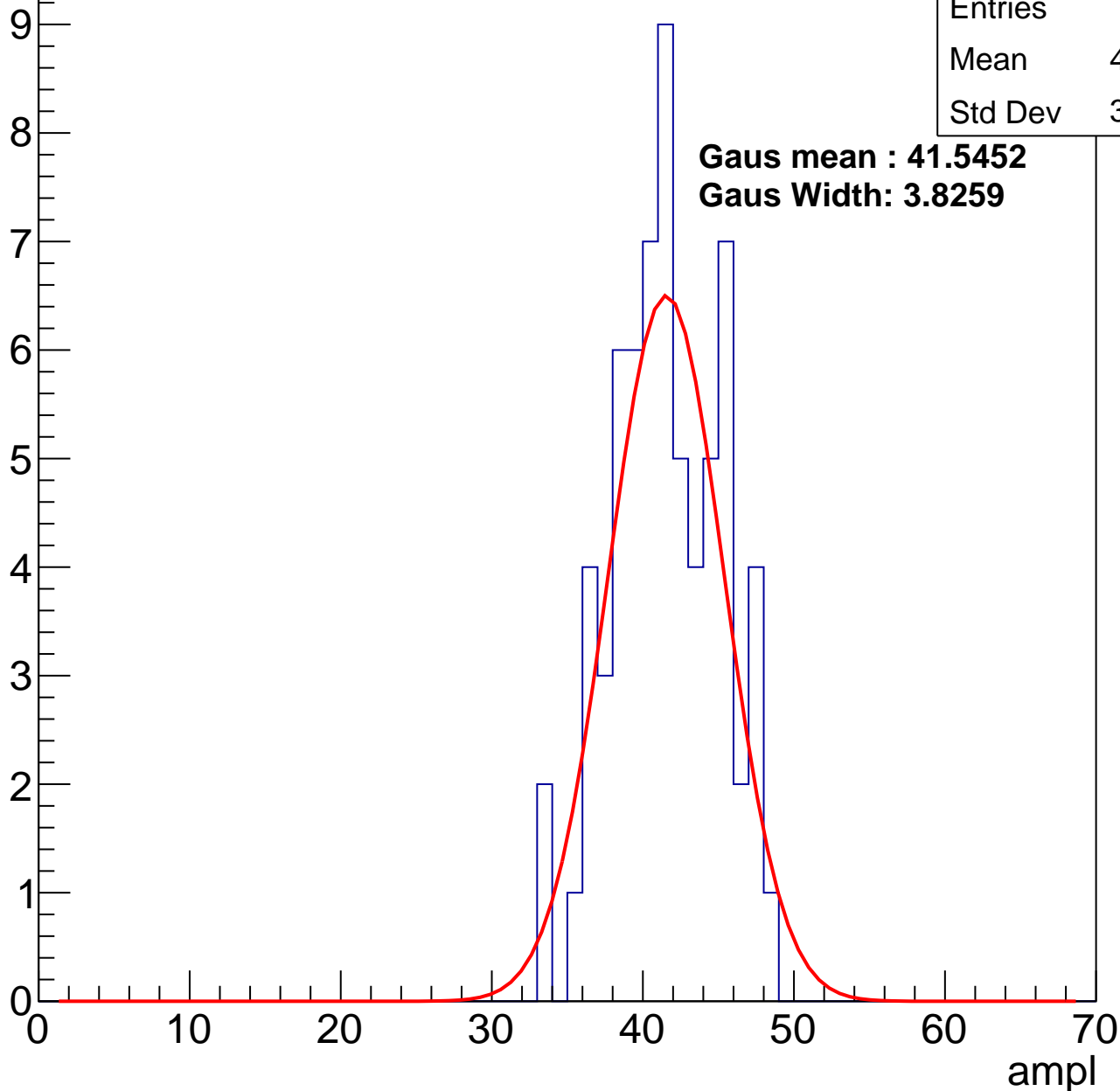
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	41.09
Std Dev	3.519

**Gaus mean : 41.5452**

**Gaus Width: 3.8259**

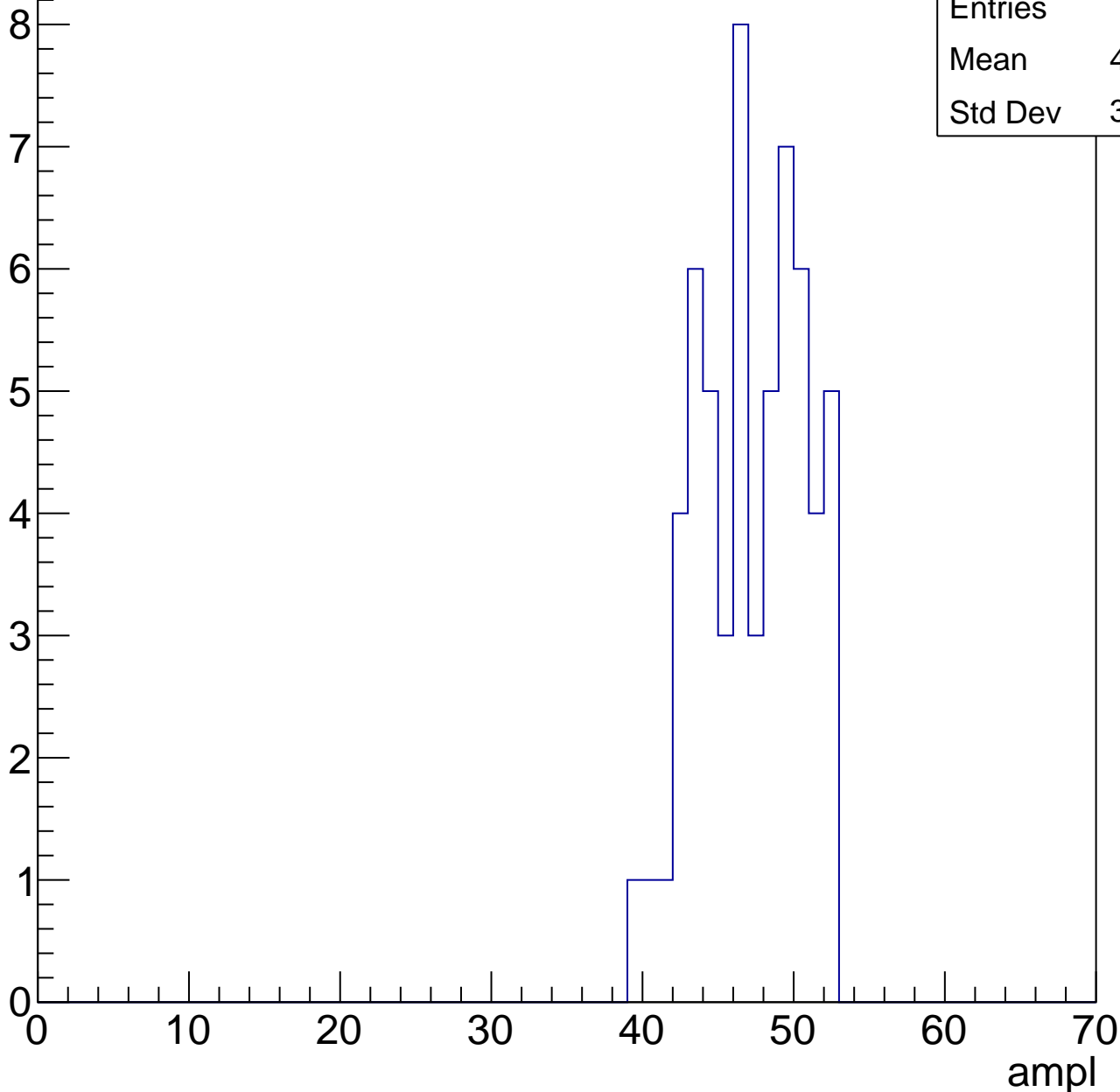


# B1L103S, U2-ch90, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	46.73
Std Dev	3.399

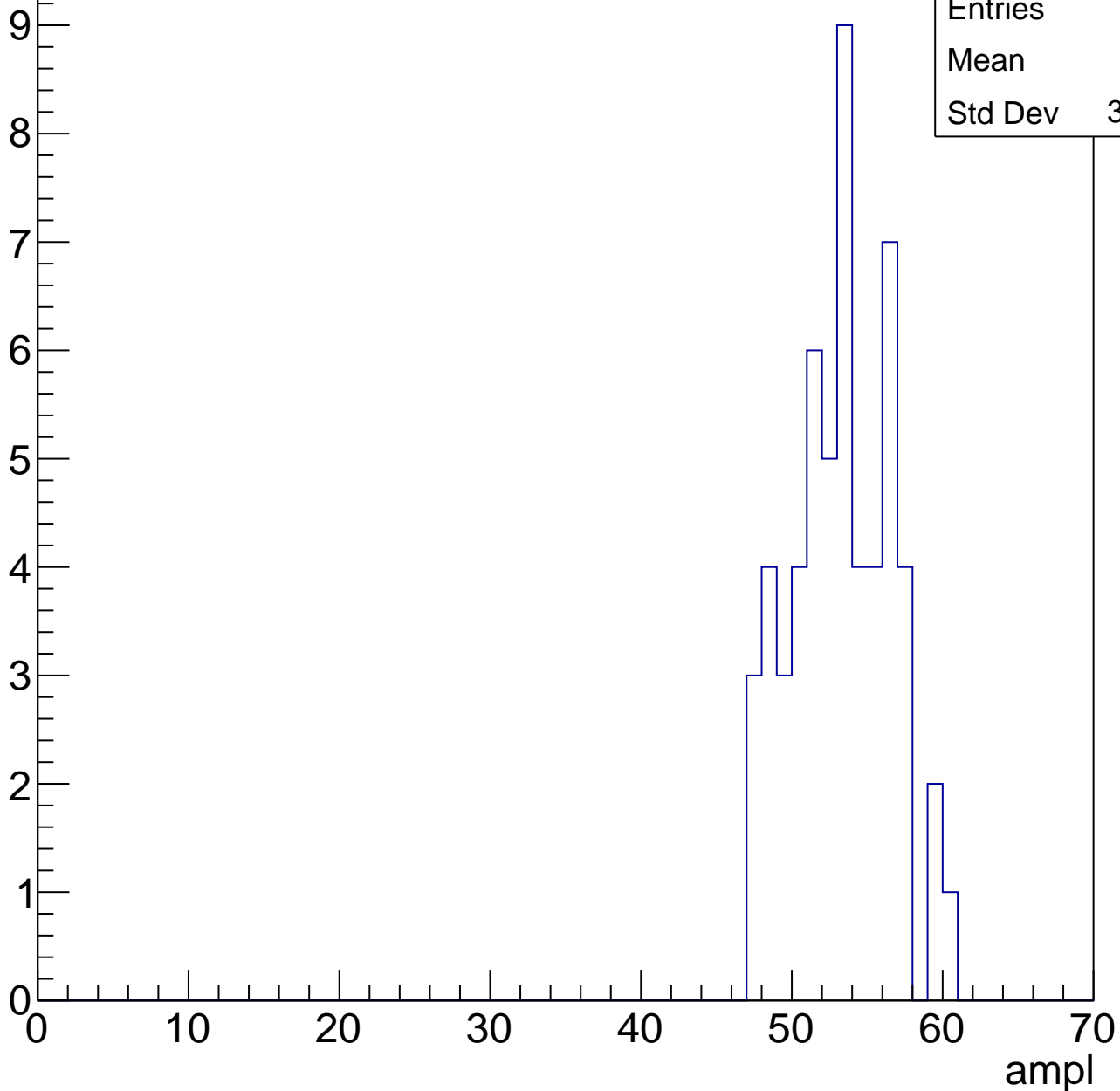


# B1L103S, U2-ch90, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

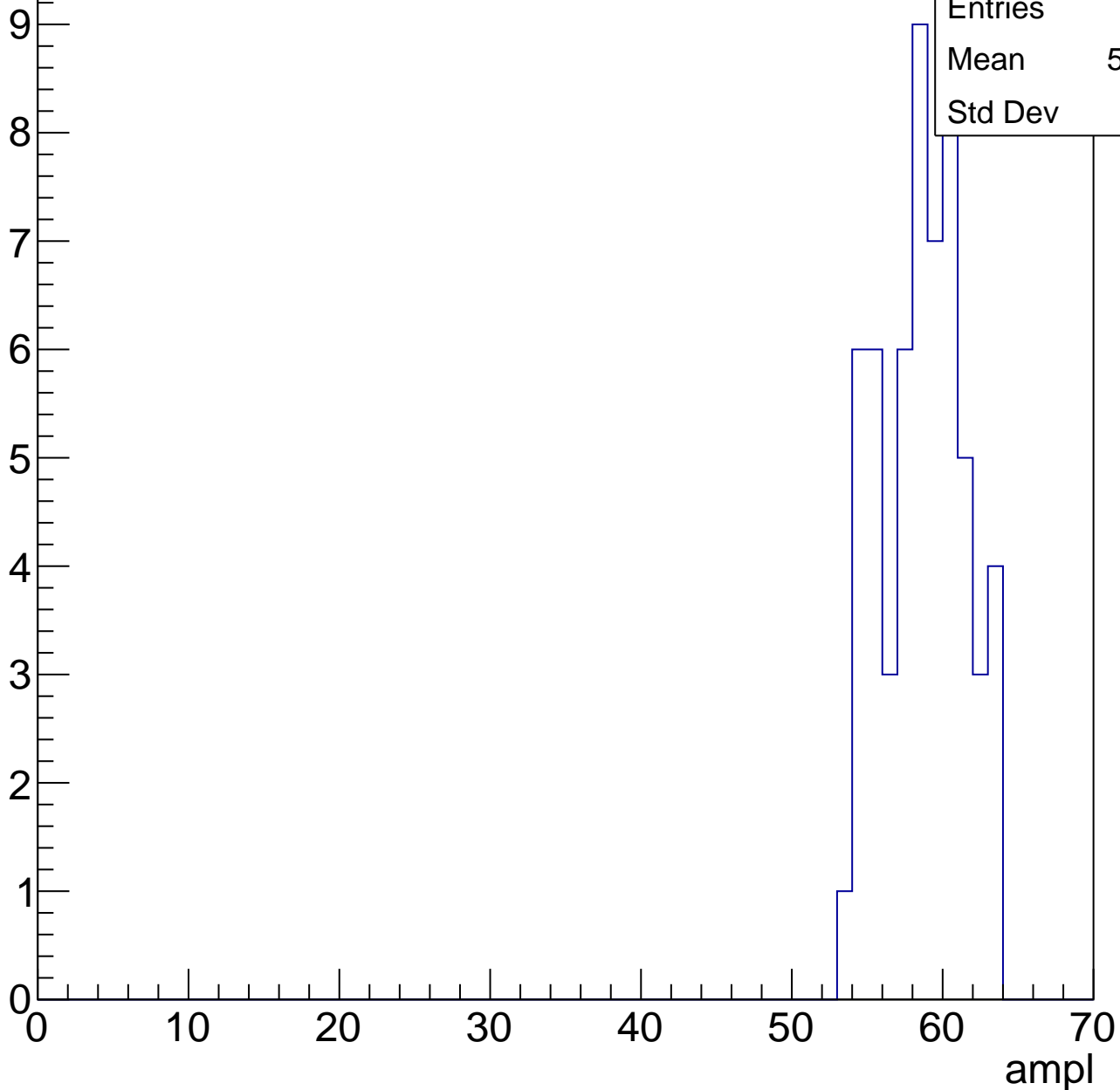
Entries	56
Mean	52.8
Std Dev	3.237



# B1L103S, U2-ch90, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



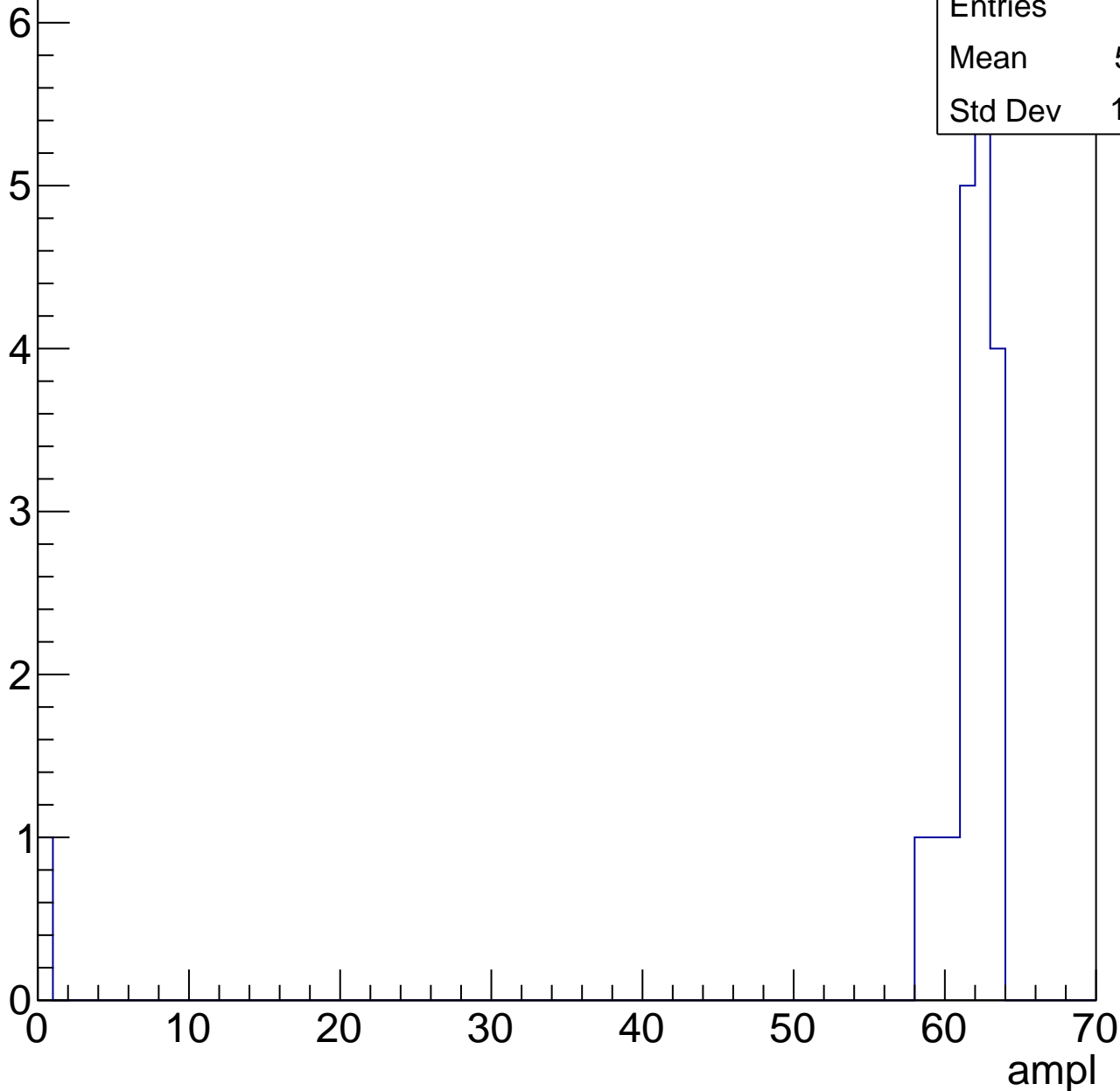
Entries	58
Mean	58.19
Std Dev	2.7

# B1L103S, U2-ch90, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	19
Mean	58.21
Std Dev	13.78

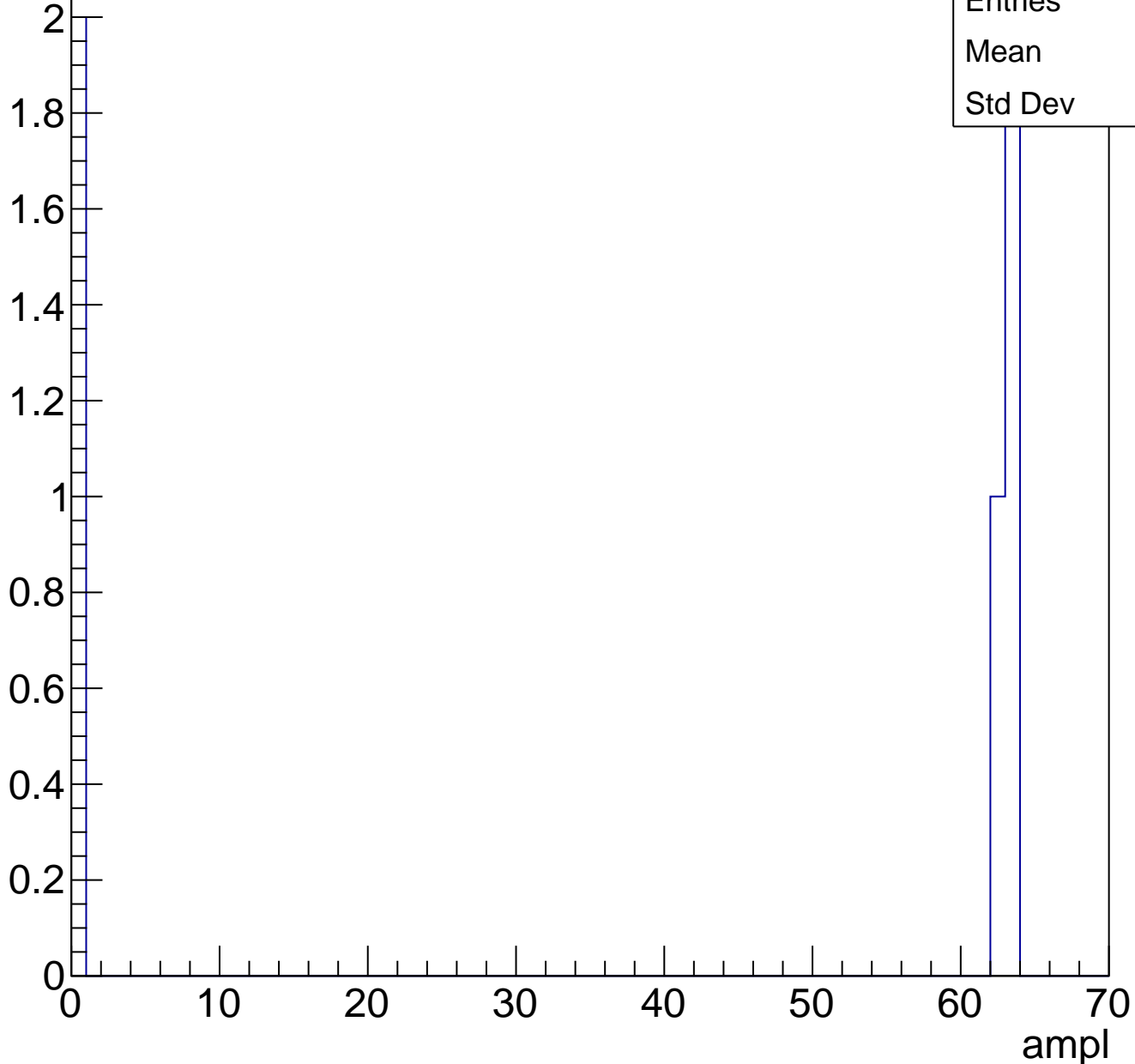




# B1L103S, U2-ch90, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch91, adc0

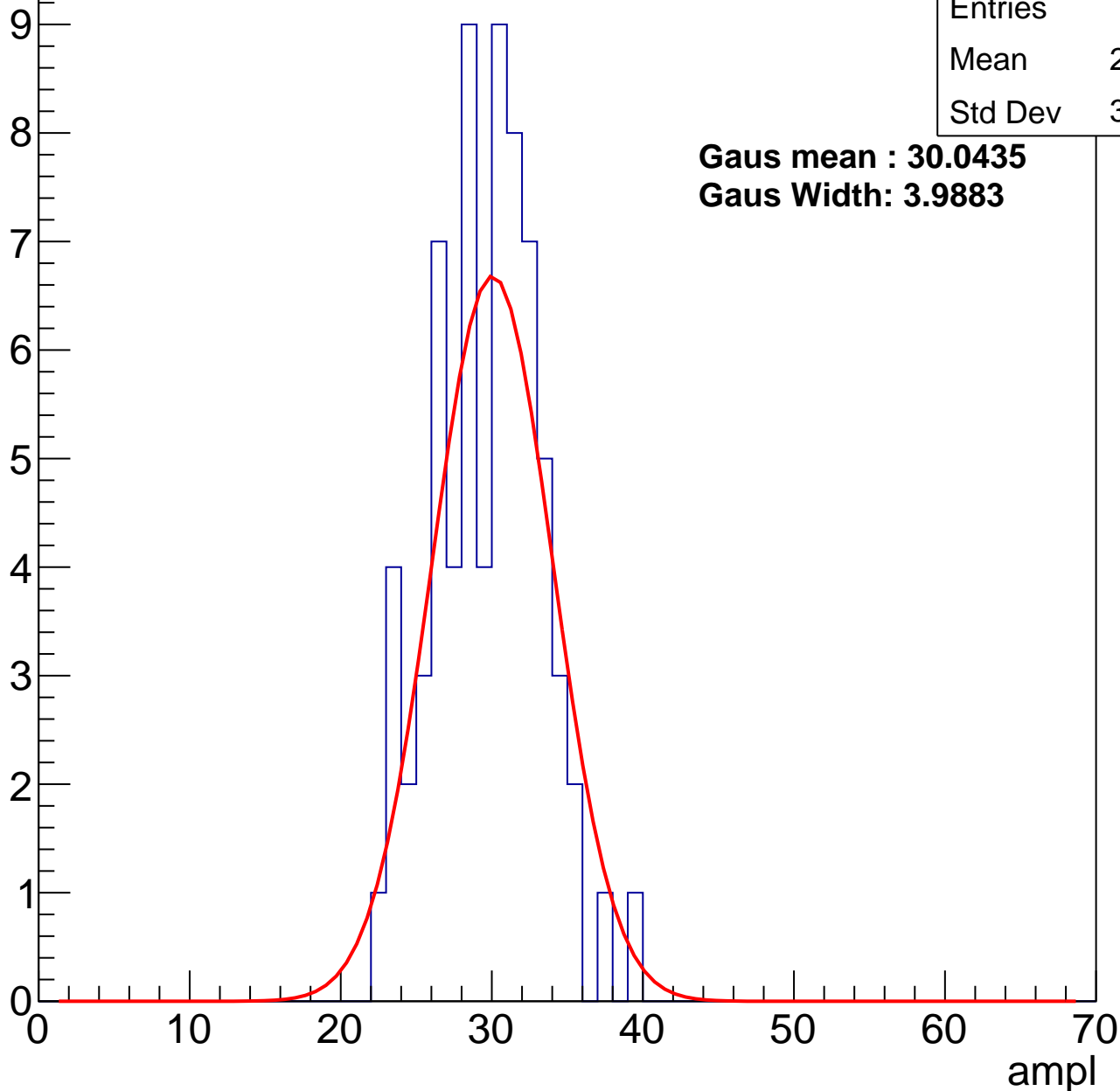
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	29.29
Std Dev	3.522

**Gaus mean : 30.0435**

**Gaus Width: 3.9883**



# B1L103S, U2-ch91, adc1

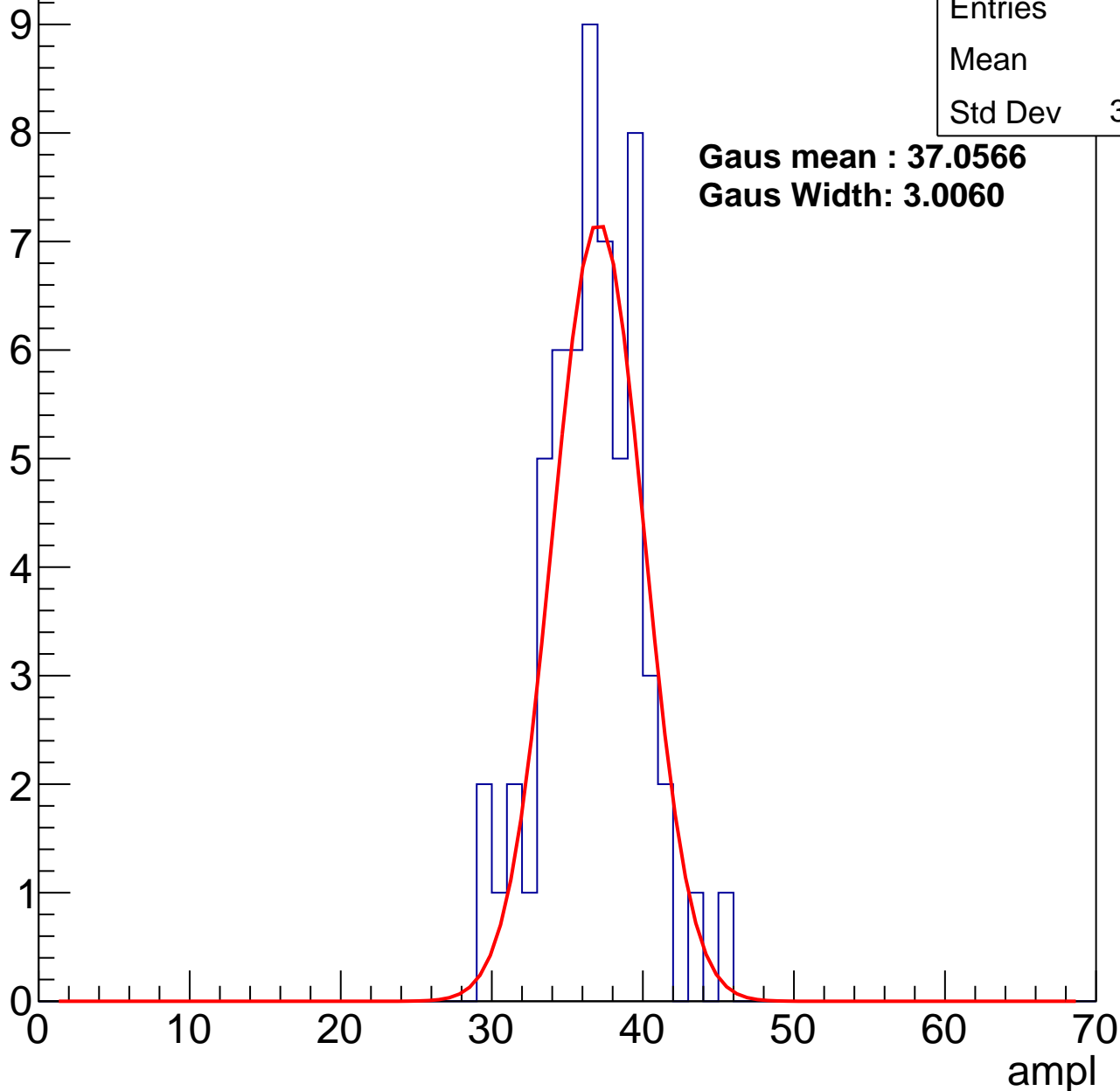
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	36.2
Std Dev	3.188

**Gaus mean : 37.0566**

**Gaus Width: 3.0060**



# B1L103S, U2-ch91, adc2

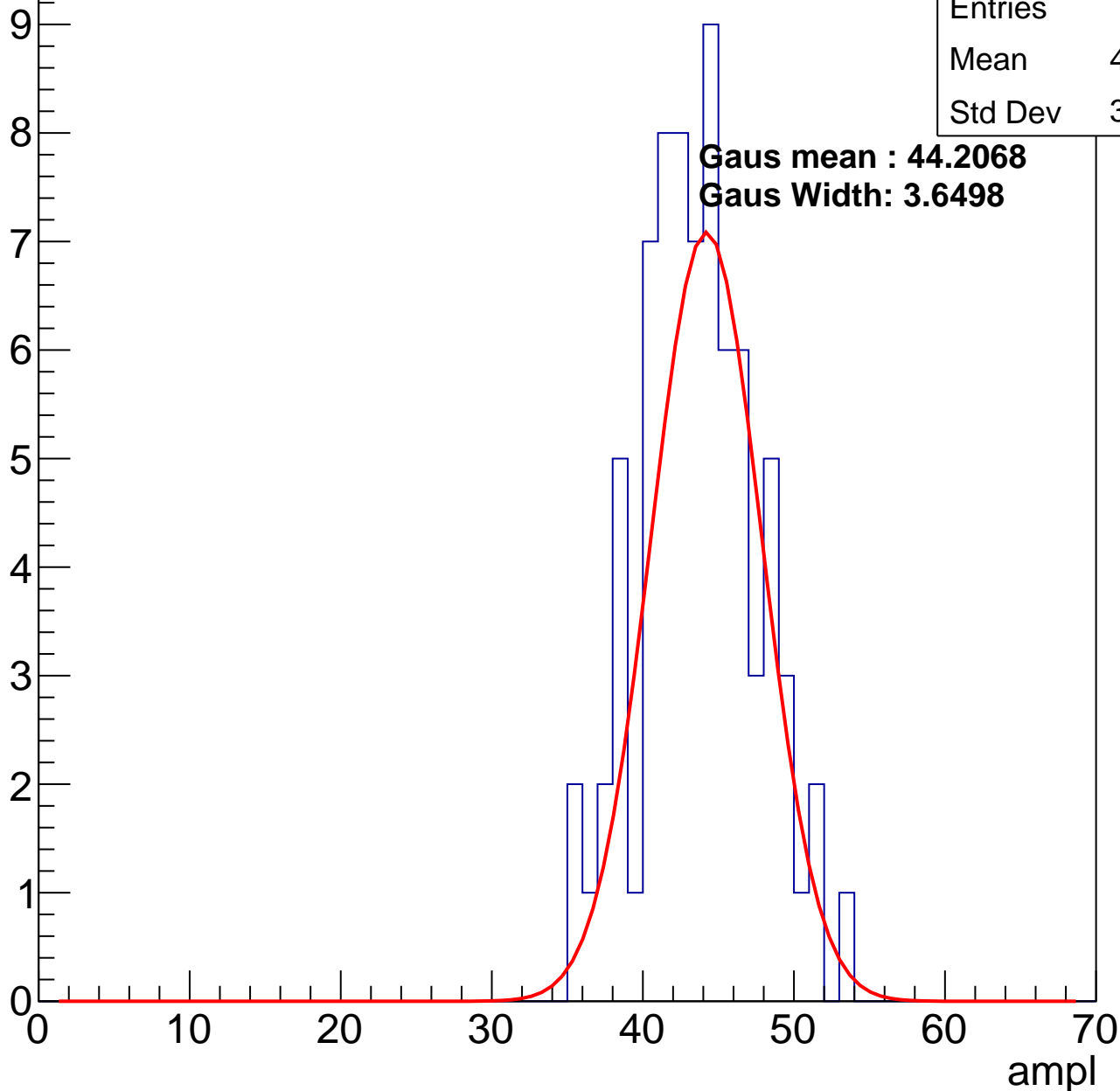
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	43.23
Std Dev	3.837

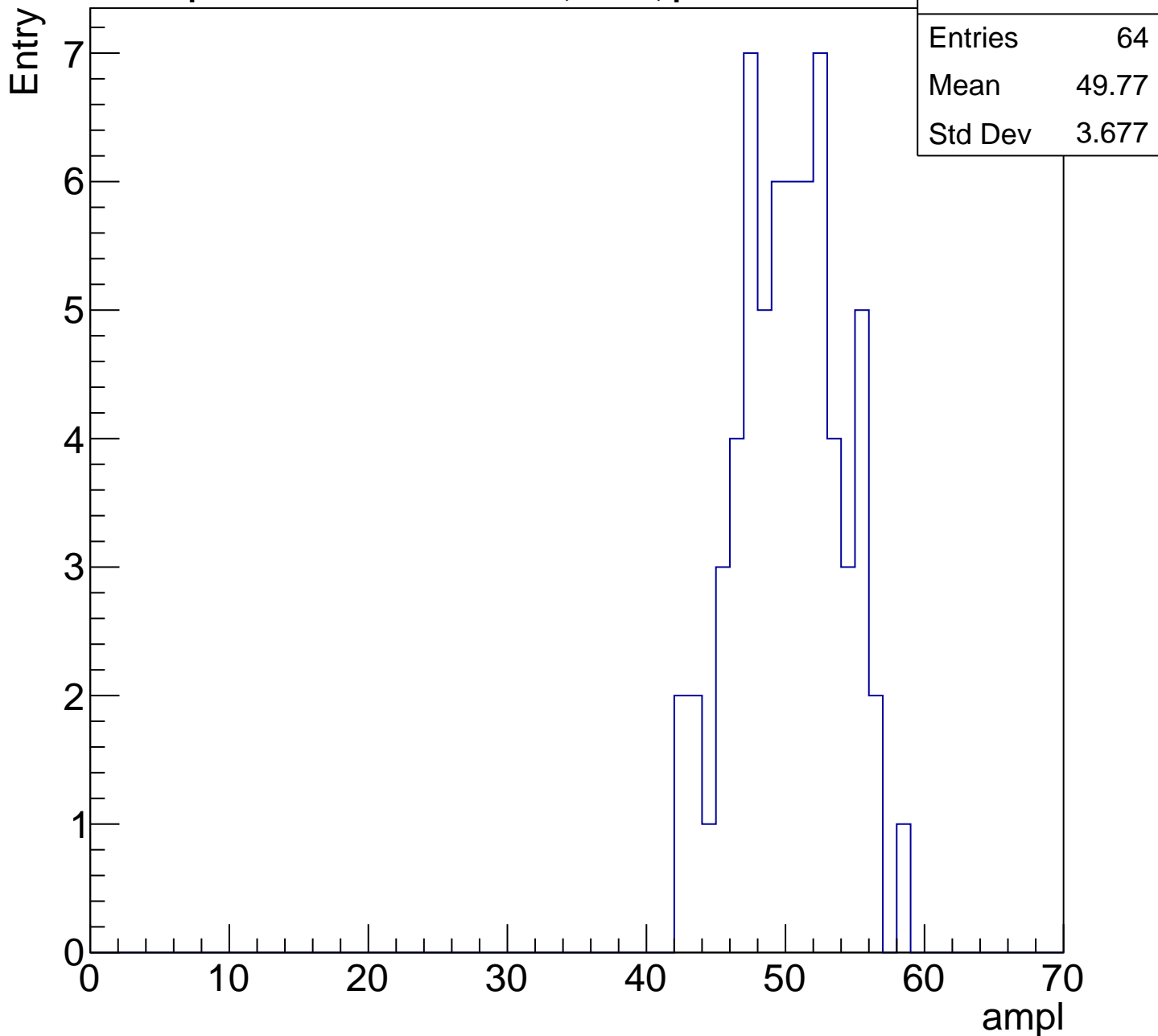
**Gaus mean : 44.2068**

**Gaus Width: 3.6498**



# B1L103S, U2-ch91, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

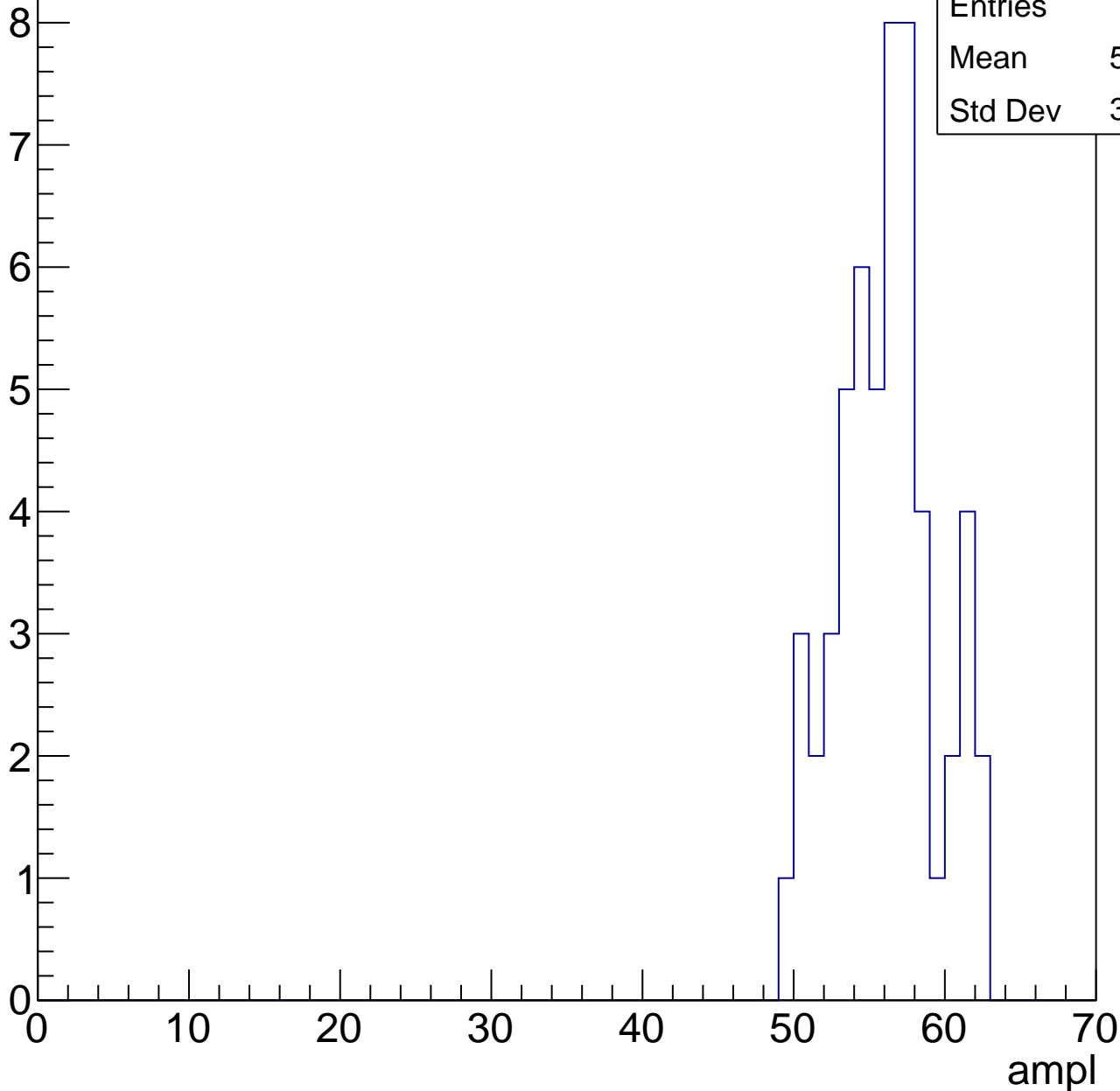


# B1L103S, U2-ch91, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

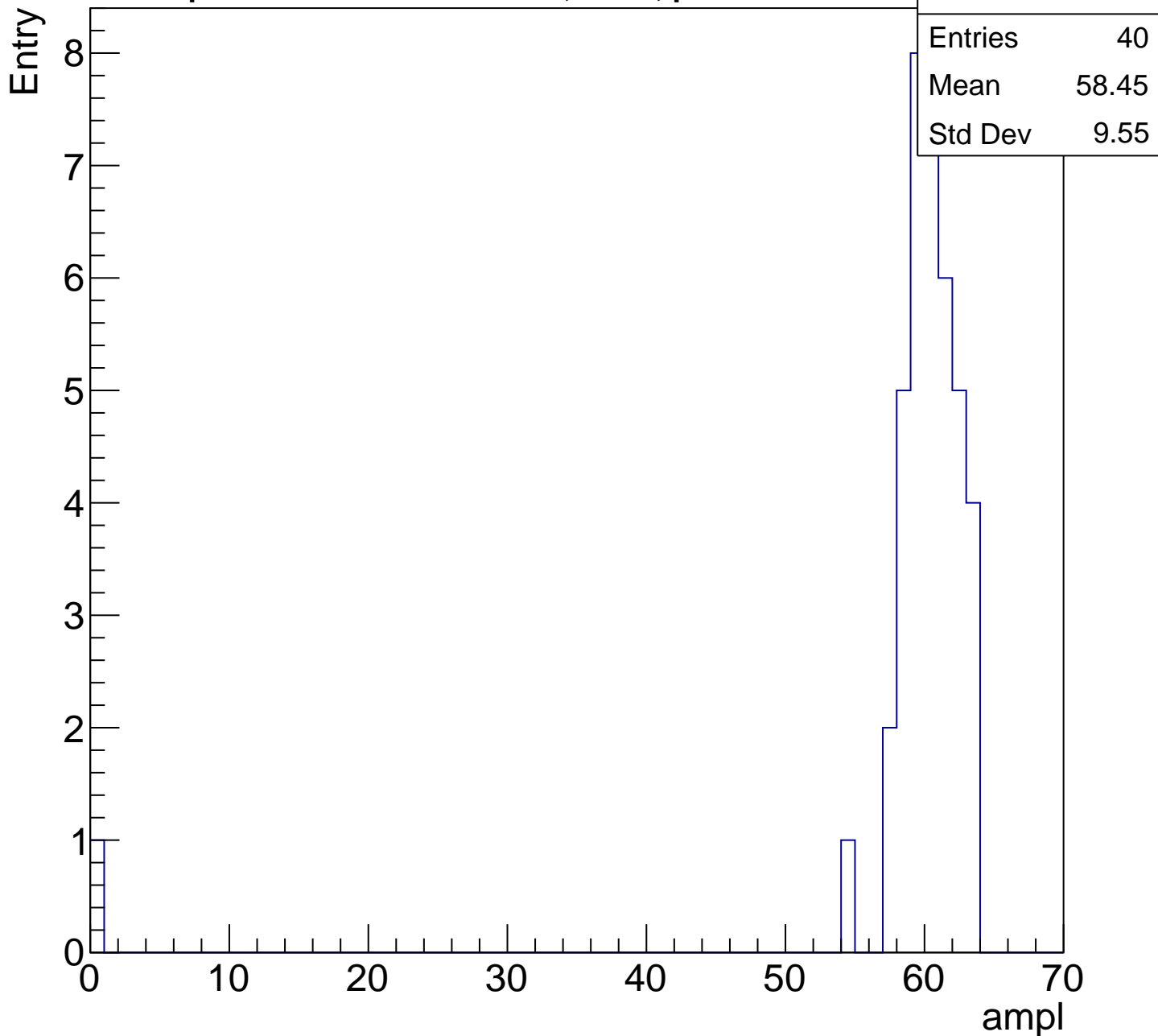
Entry

Entries	54
Mean	55.63
Std Dev	3.216



# B1L103S, U2-ch91, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

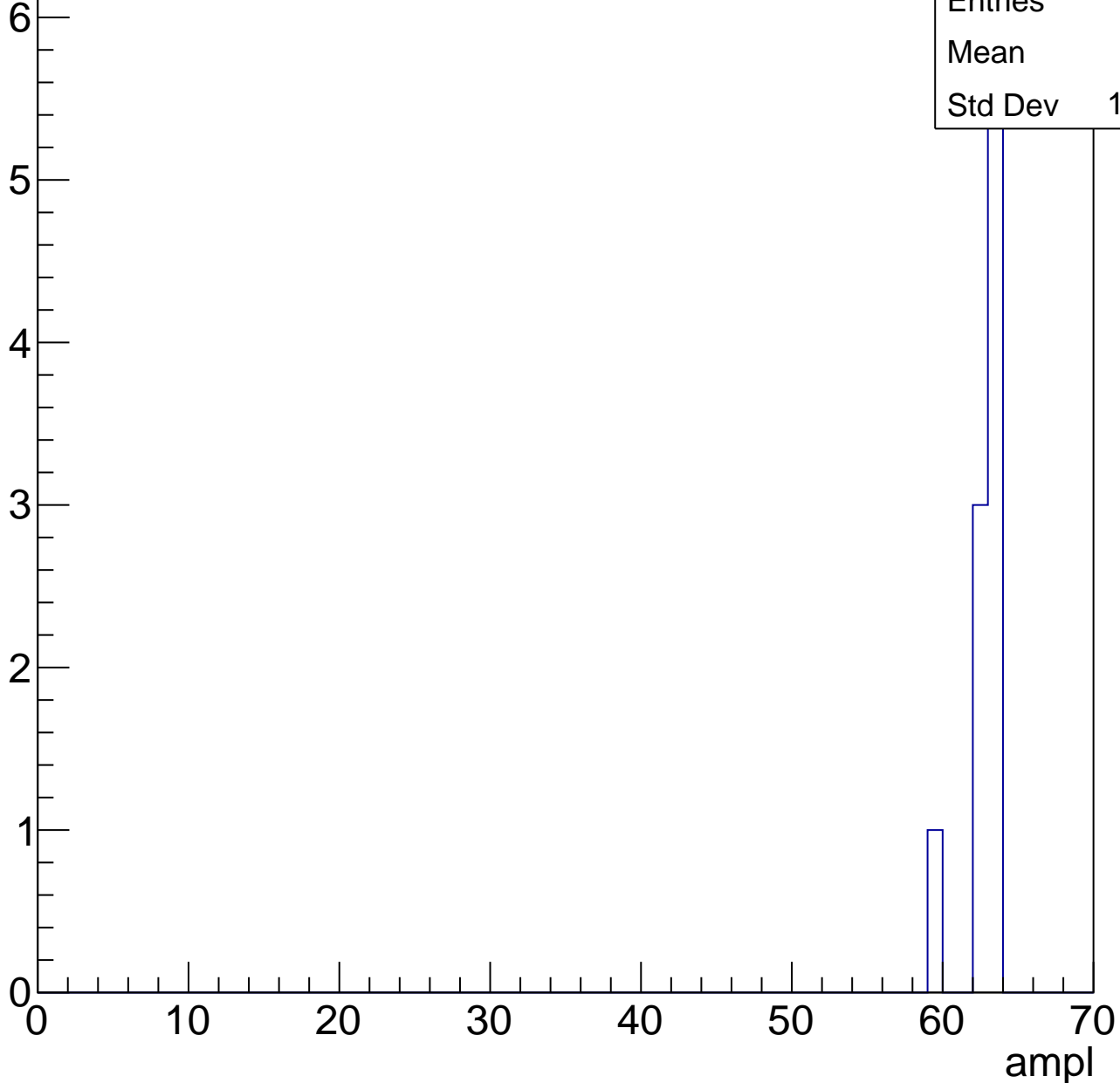


# B1L103S, U2-ch91, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	10
Mean	62.3
Std Dev	1.187

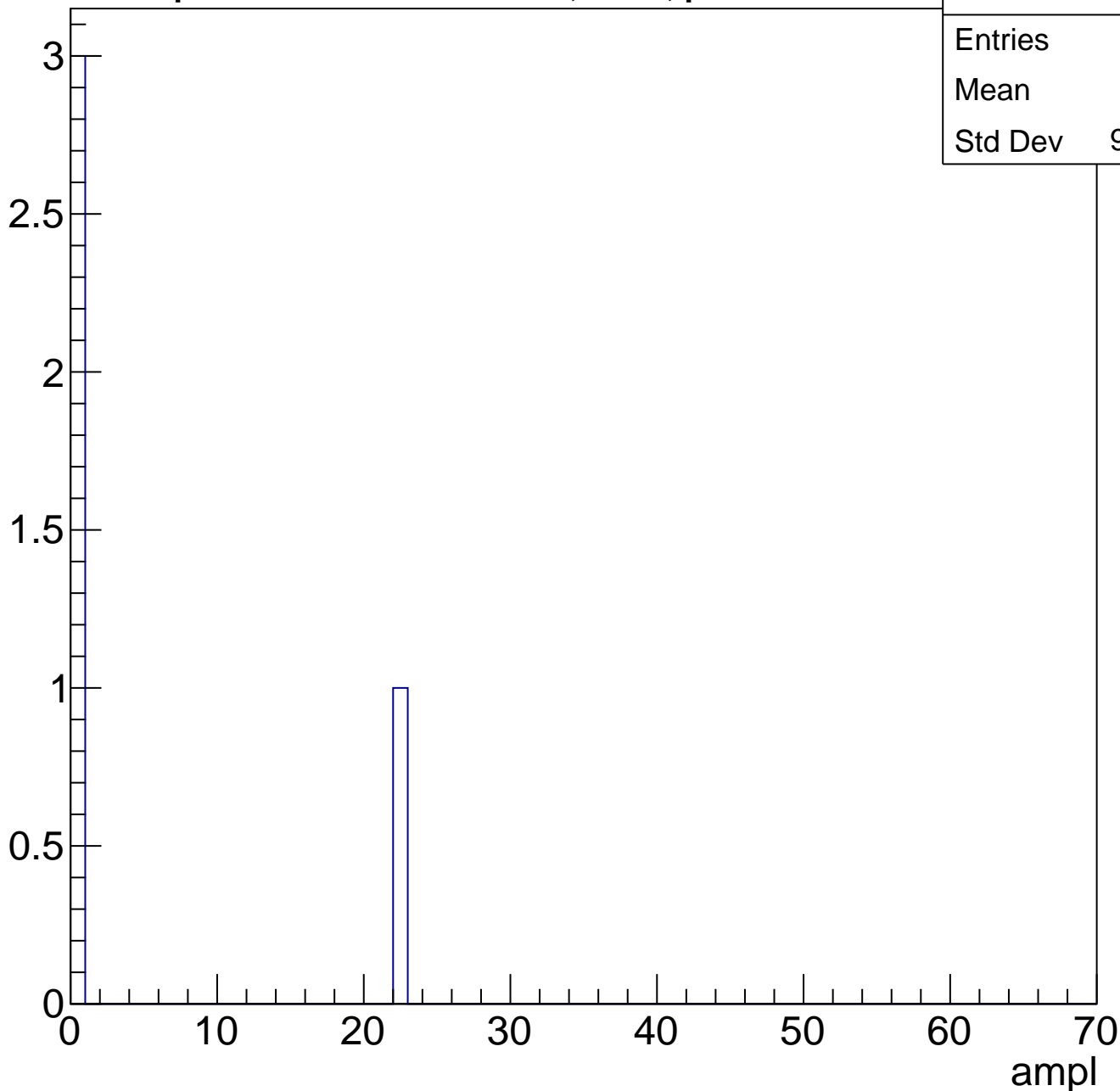




# B1L103S, U2-ch91, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	4
Mean	5.5
Std Dev	9.526

# B1L103S, U2-ch92, adc0

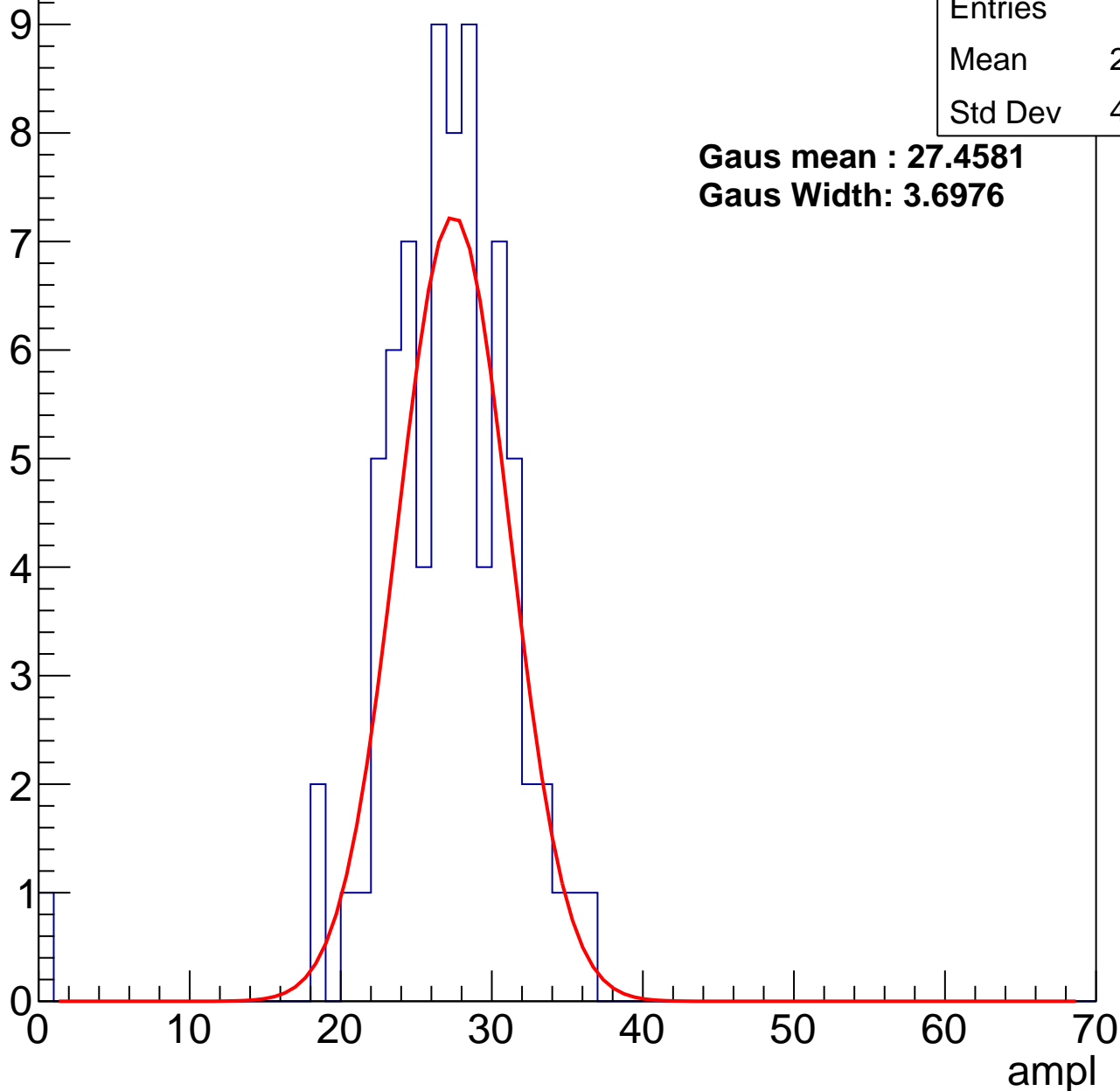
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	26.46
Std Dev	4.794

**Gaus mean : 27.4581**

**Gaus Width: 3.6976**



# B1L103S, U2-ch92, adc1

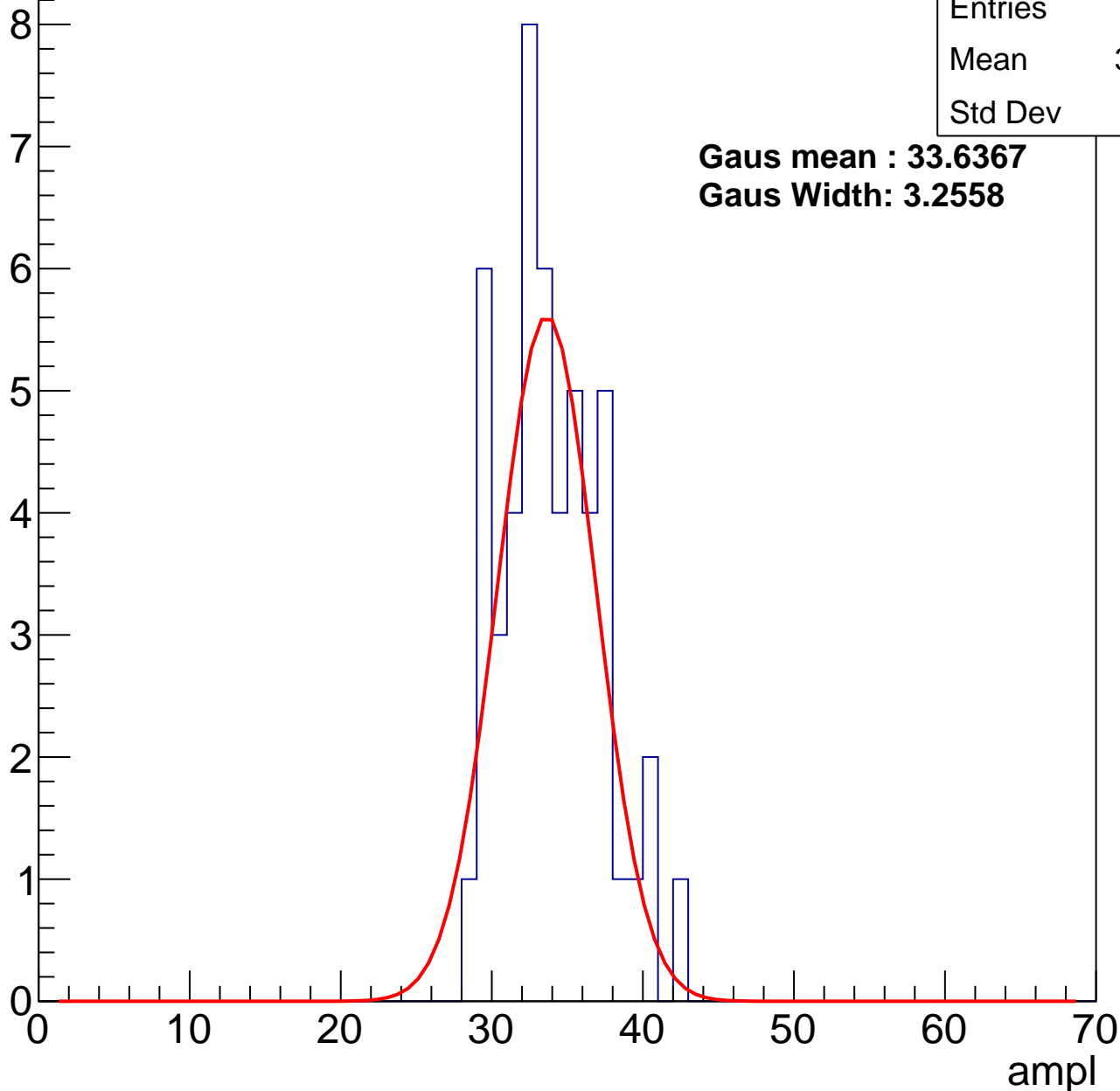
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	33.51
Std Dev	3.25

**Gaus mean : 33.6367**

**Gaus Width: 3.2558**



# B1L103S, U2-ch92, adc2

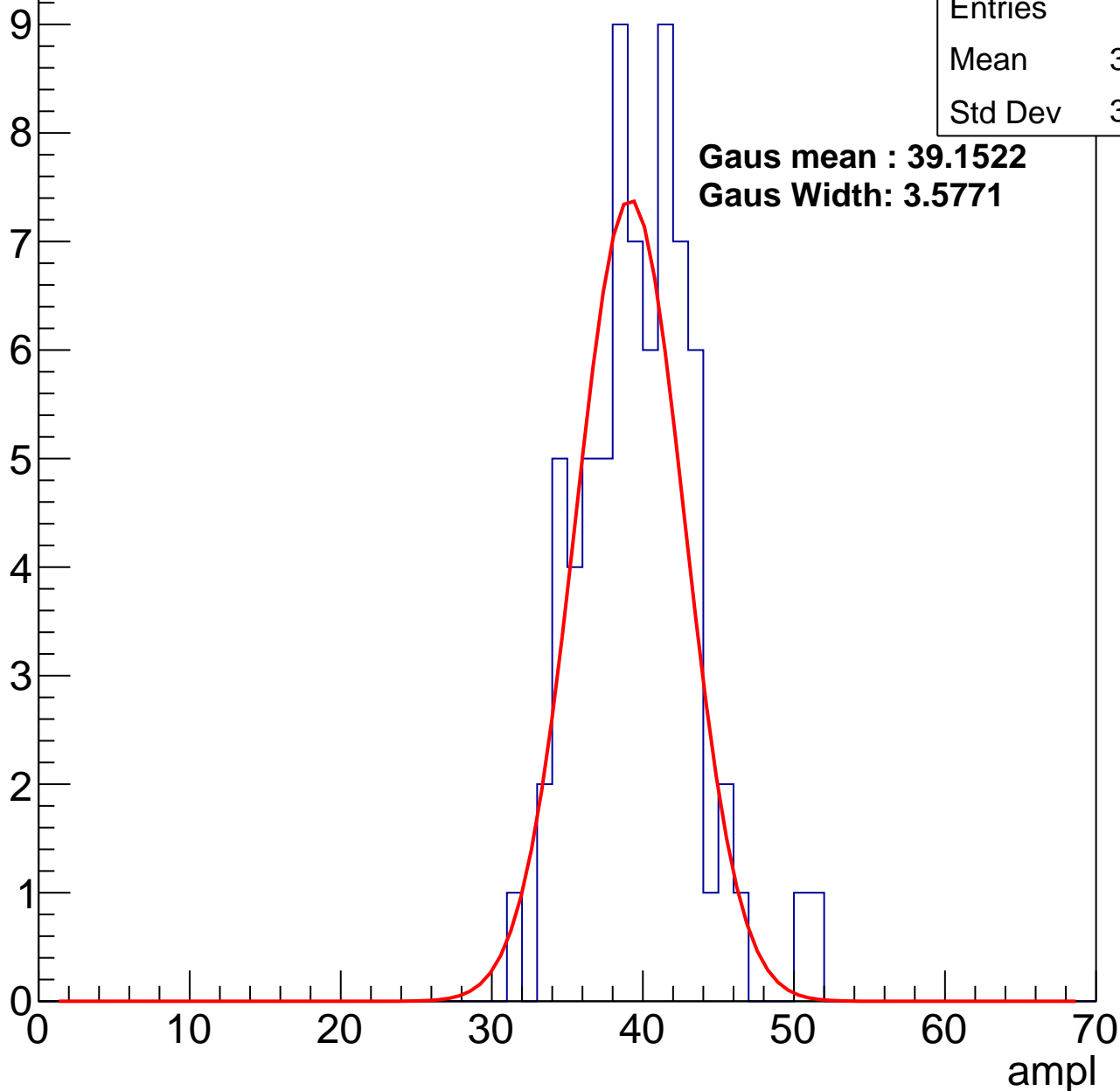
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	39.29
Std Dev	3.736

**Gaus mean : 39.1522**

**Gaus Width: 3.5771**

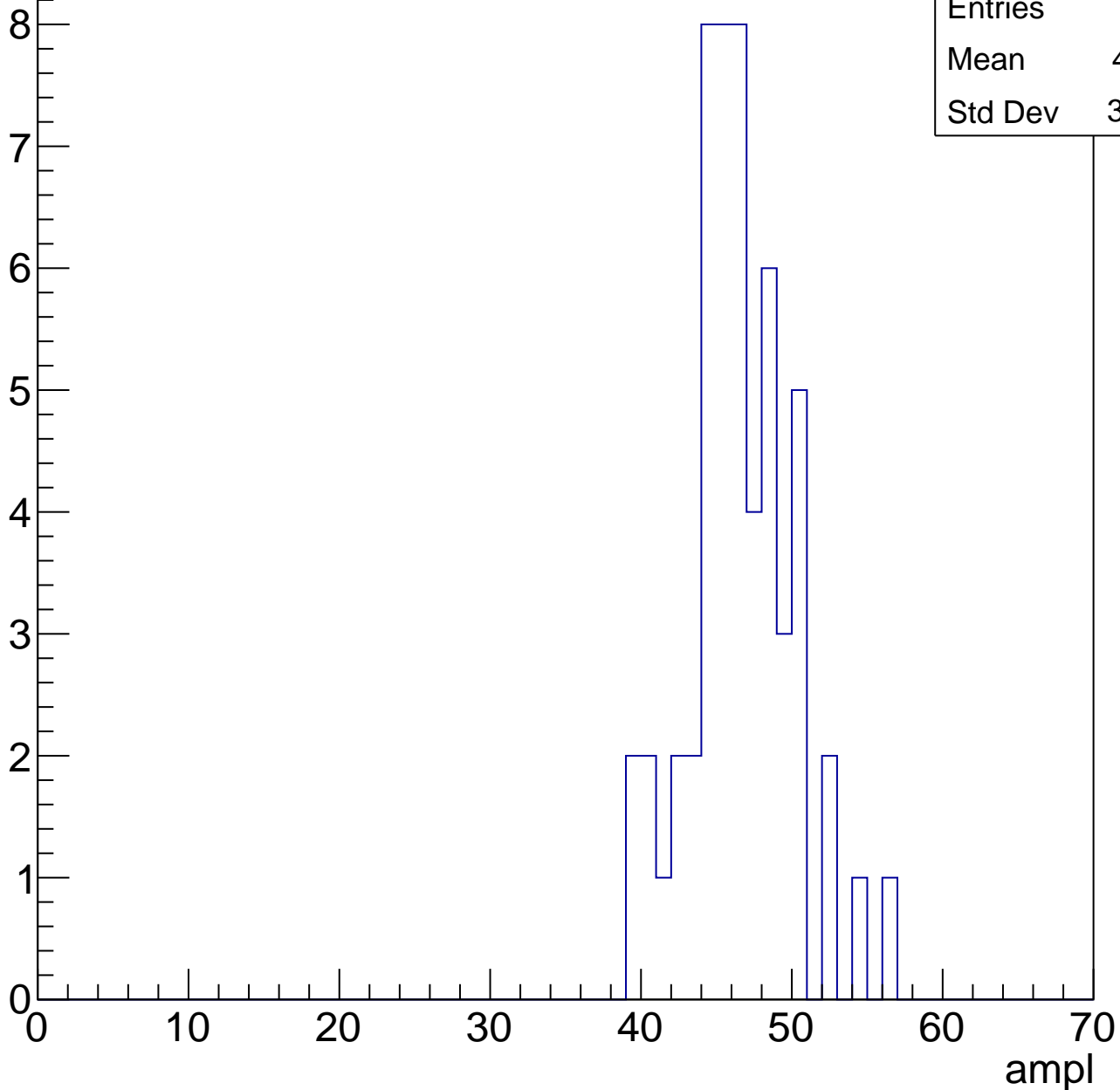


# B1L103S, U2-ch92, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	46.11
Std Dev	3.452

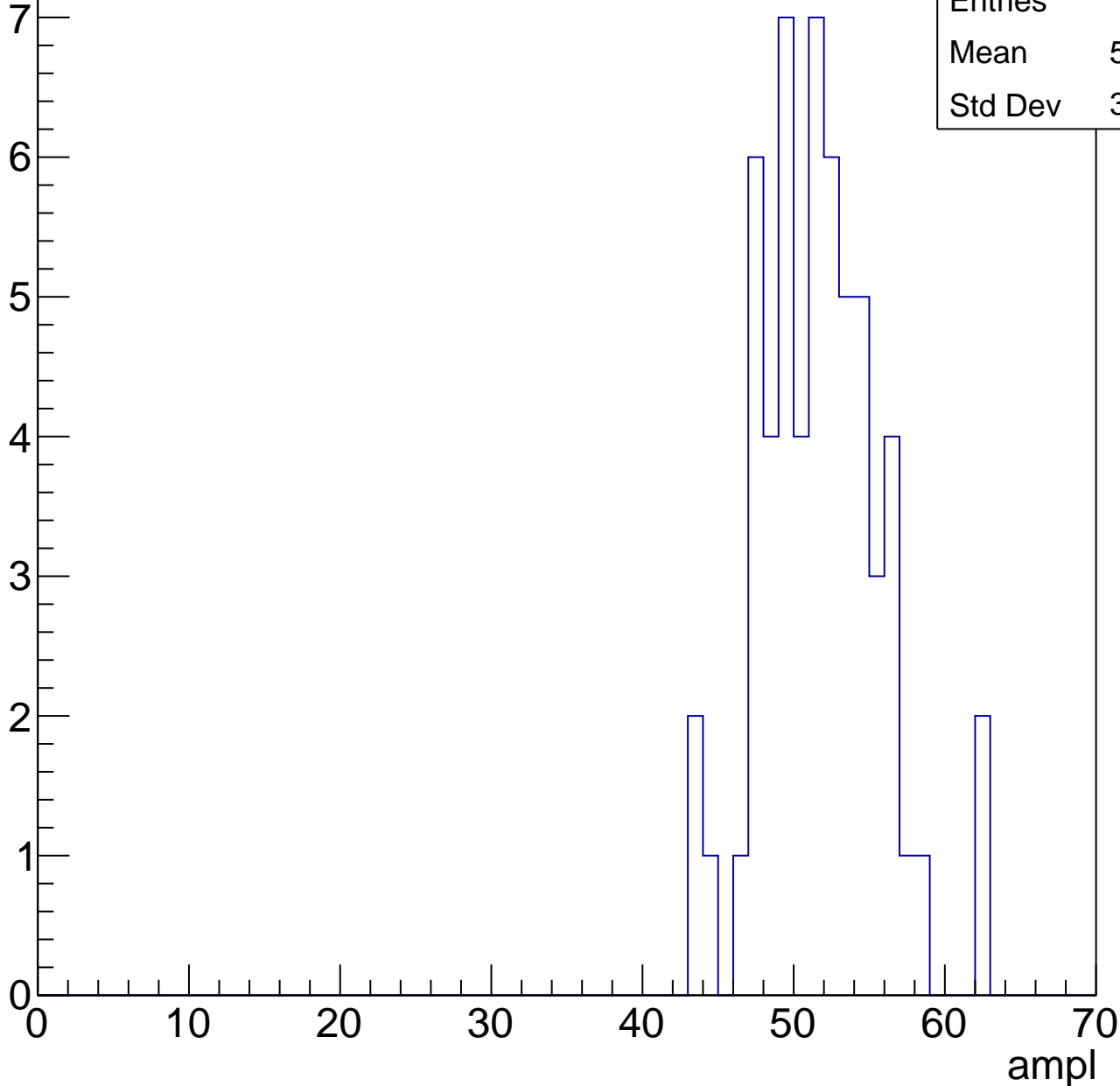


# B1L103S, U2-ch92, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

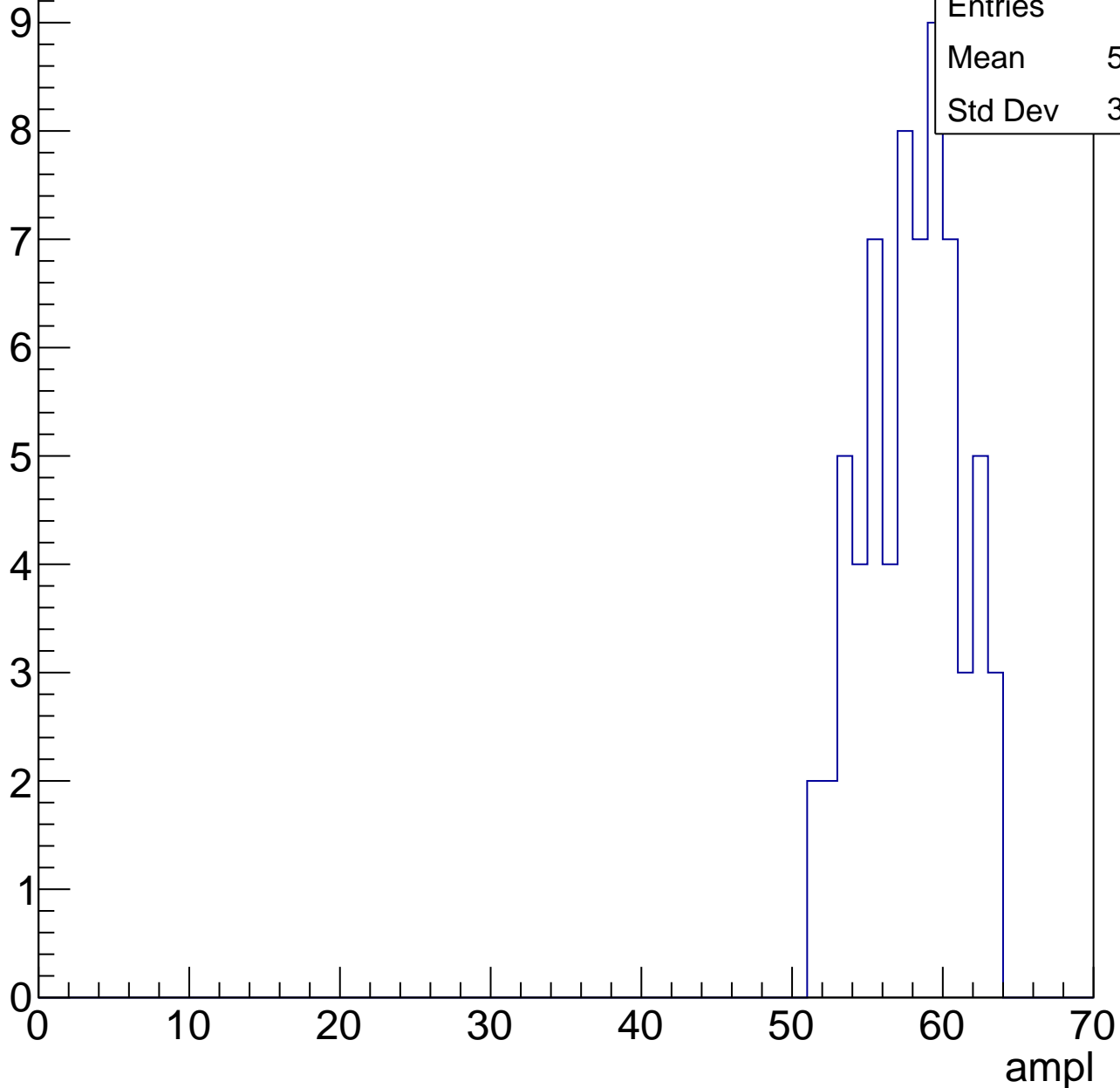
Entries	59
Mean	51.27
Std Dev	3.922



# B1L103S, U2-ch92, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



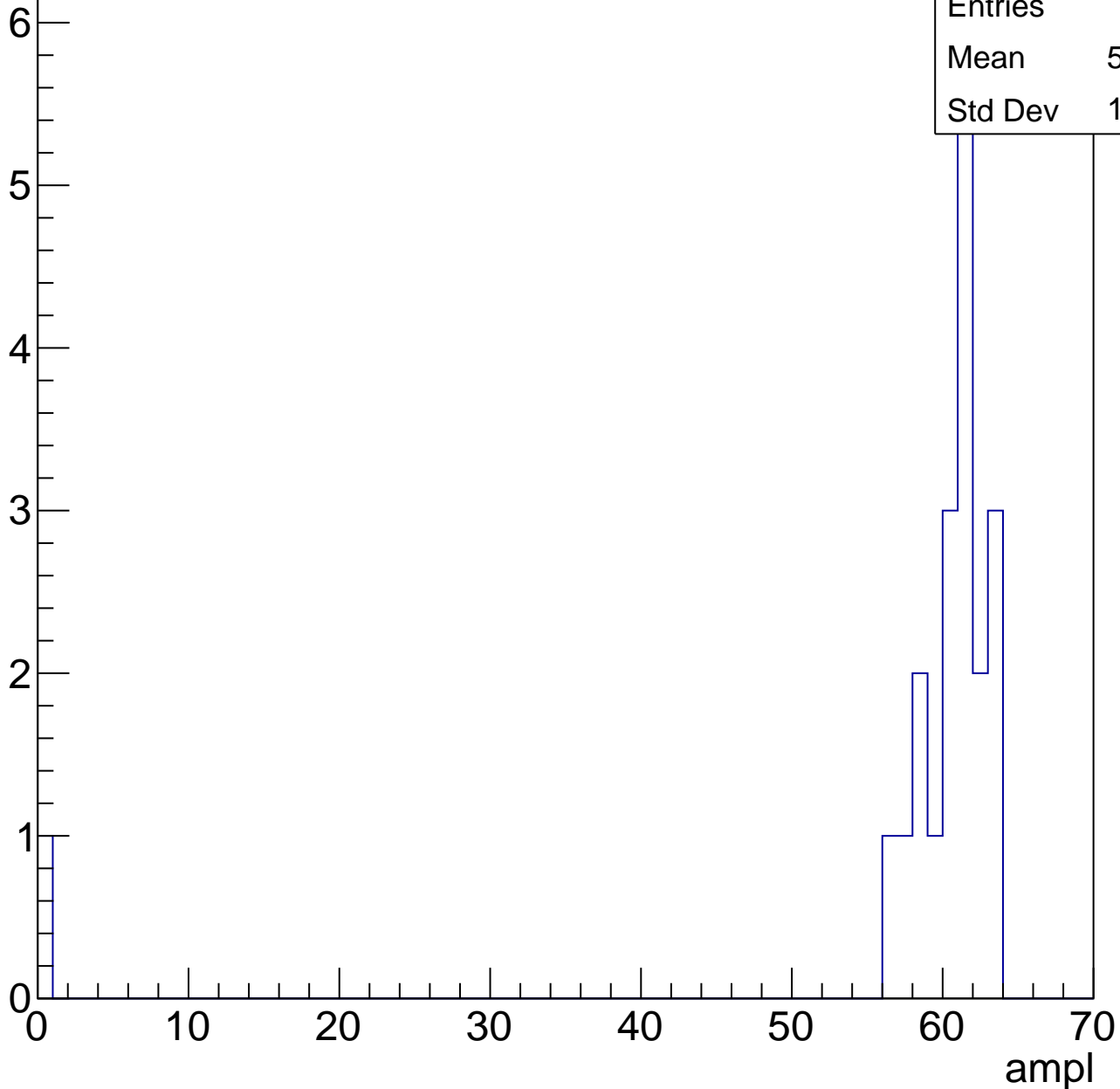
Entries	66
Mean	57.44
Std Dev	3.124

# B1L103S, U2-ch92, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	20
Mean	57.35
Std Dev	13.29

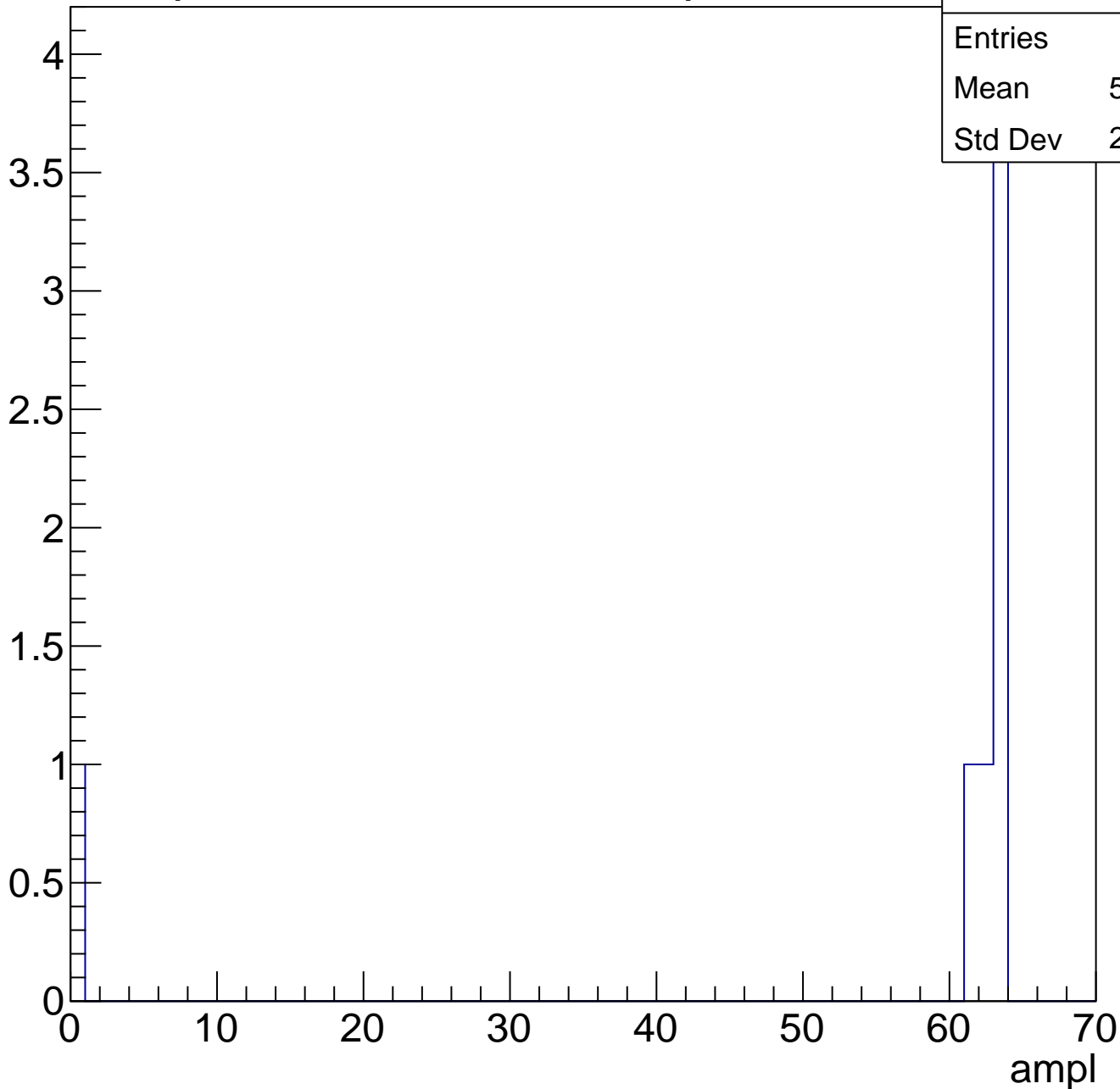




# B1L103S, U2-ch92, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch93, adc0

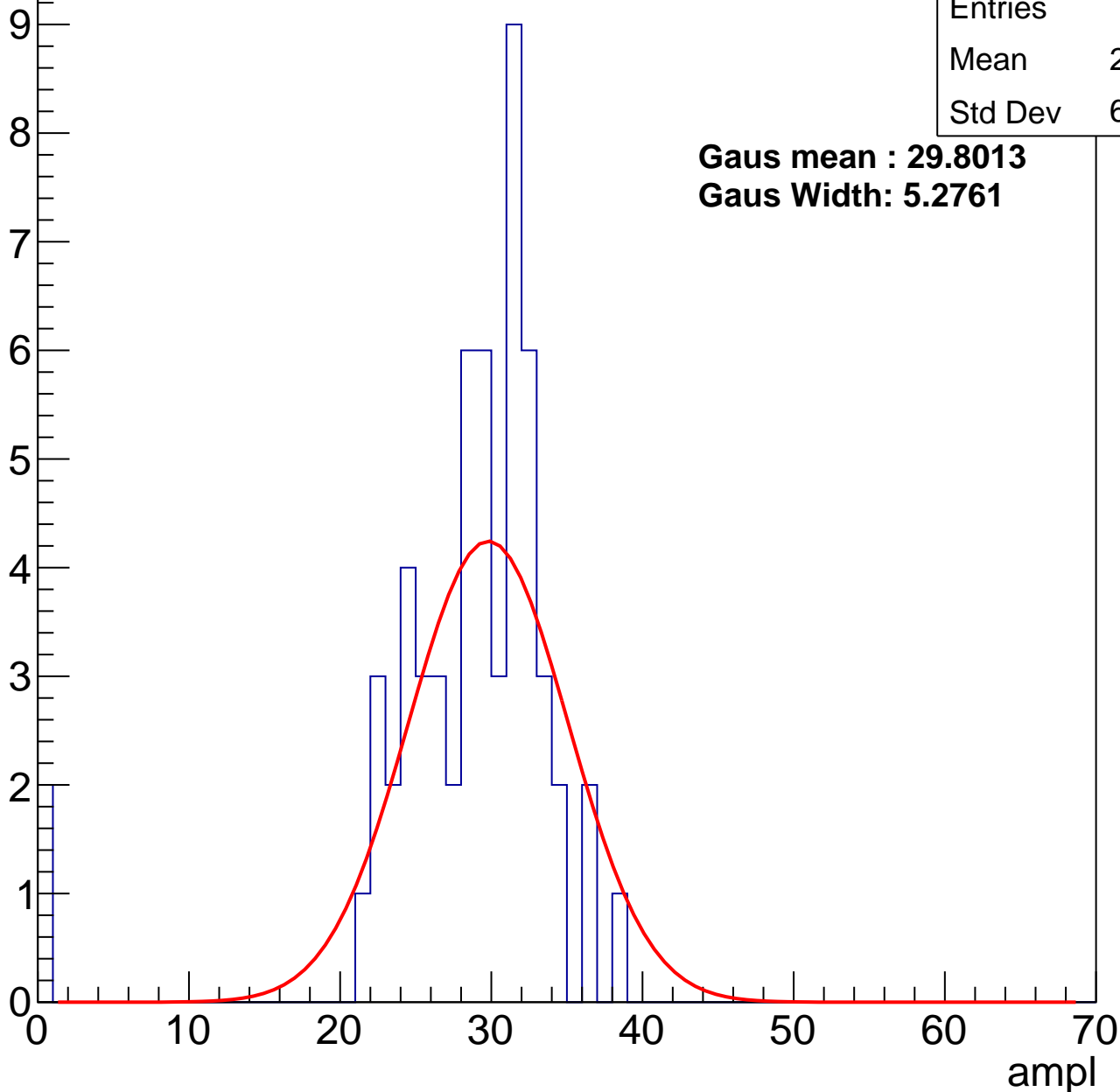
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	27.86
Std Dev	6.498

**Gaus mean : 29.8013**

**Gaus Width: 5.2761**



# B1L103S, U2-ch93, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	72
Mean	35.64
Std Dev	3.203

**Gaus mean : 36.0432**

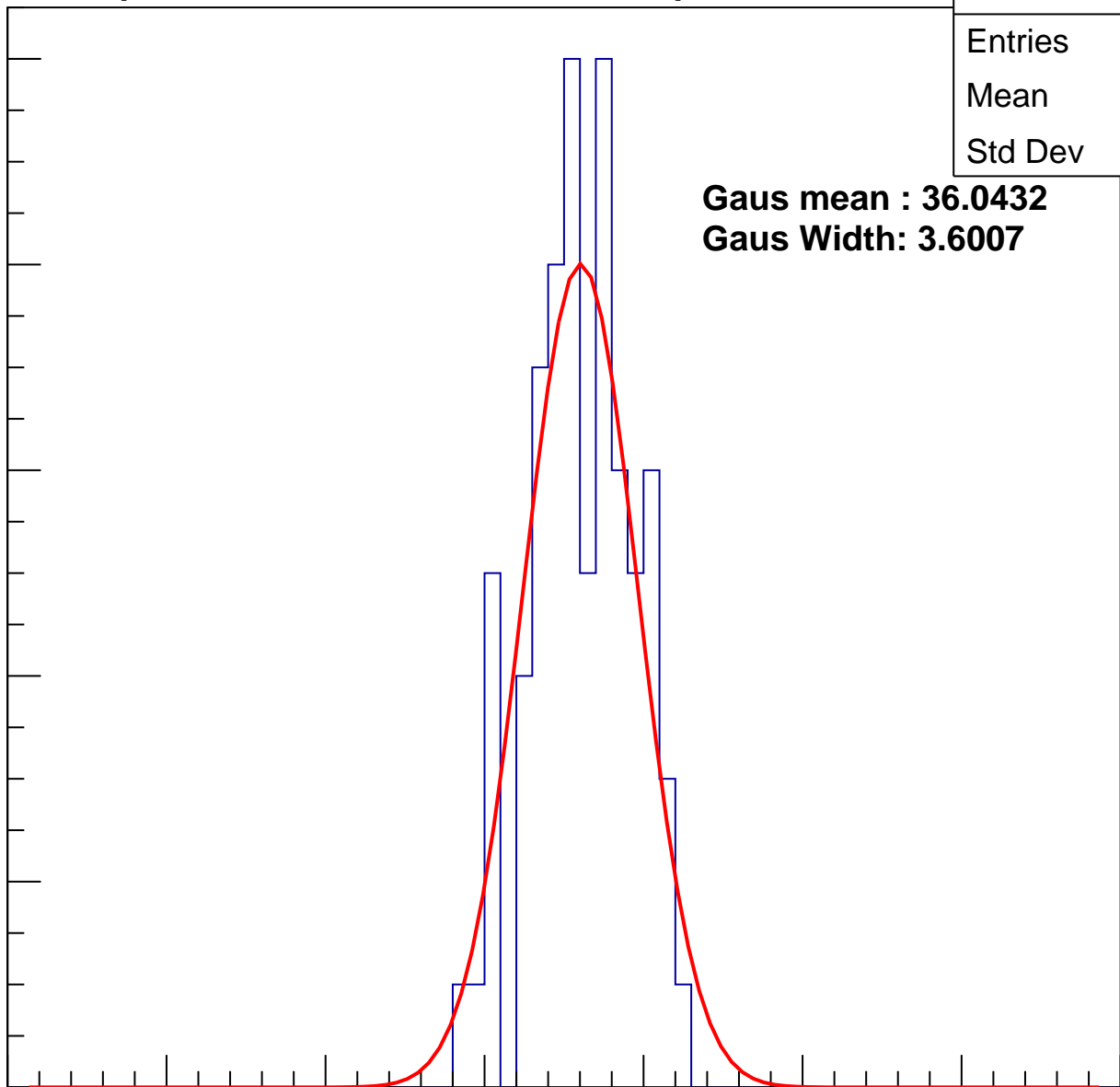
**Gaus Width: 3.6007**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U2-ch93, adc2

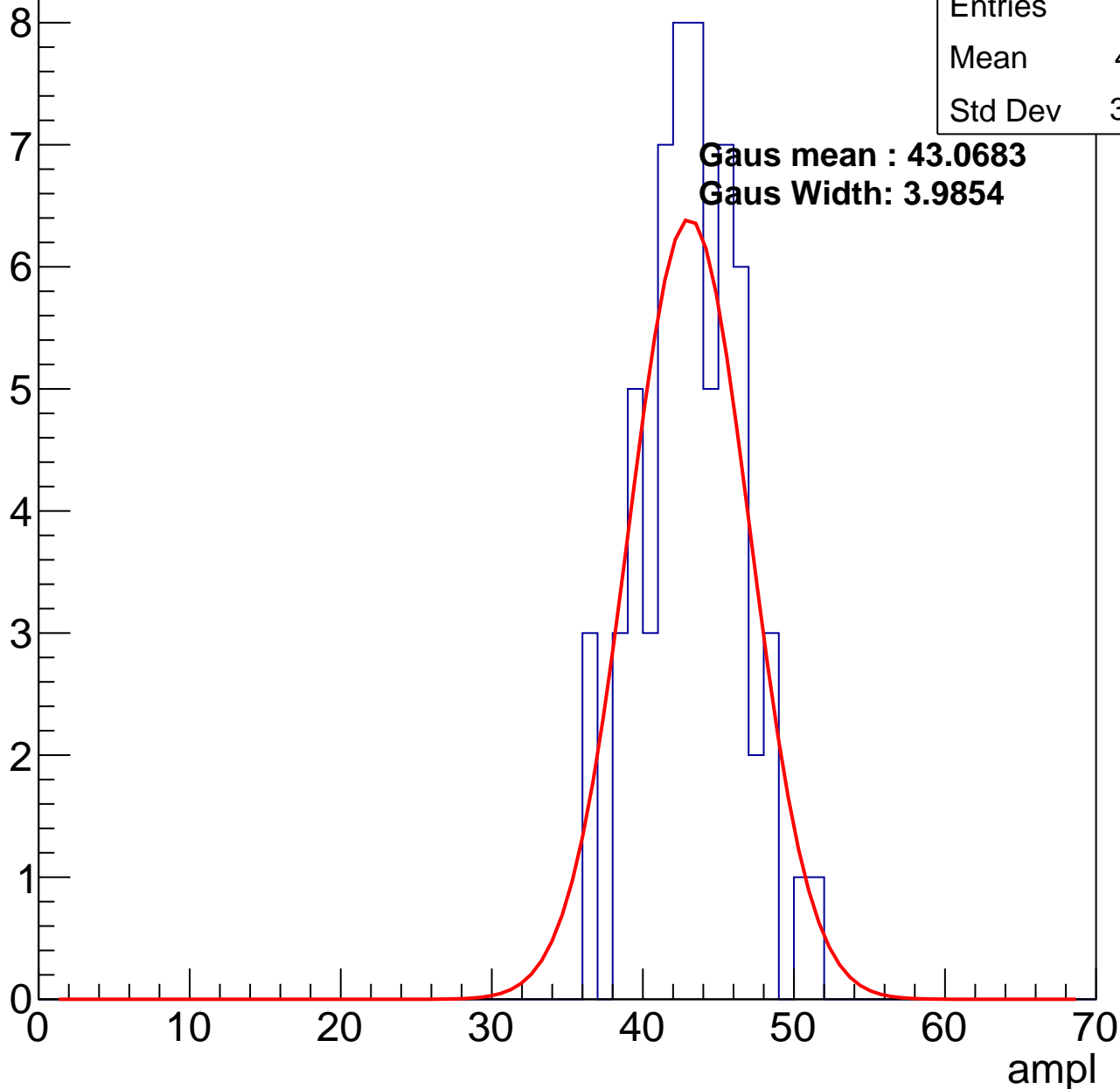
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	42.81
Std Dev	3.287

**Gaus mean : 43.0683**

**Gaus Width: 3.9854**

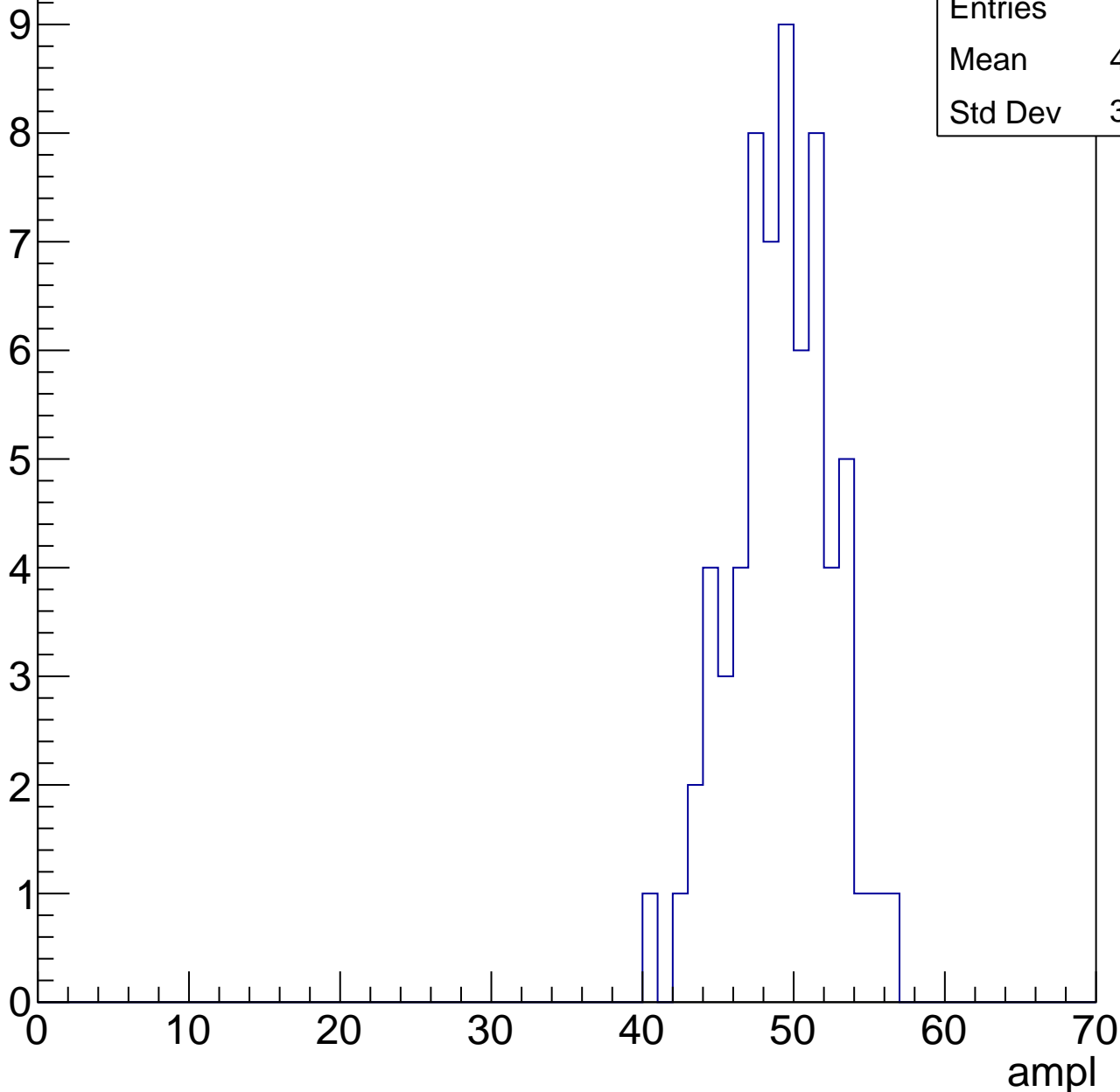


# B1L103S, U2-ch93, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

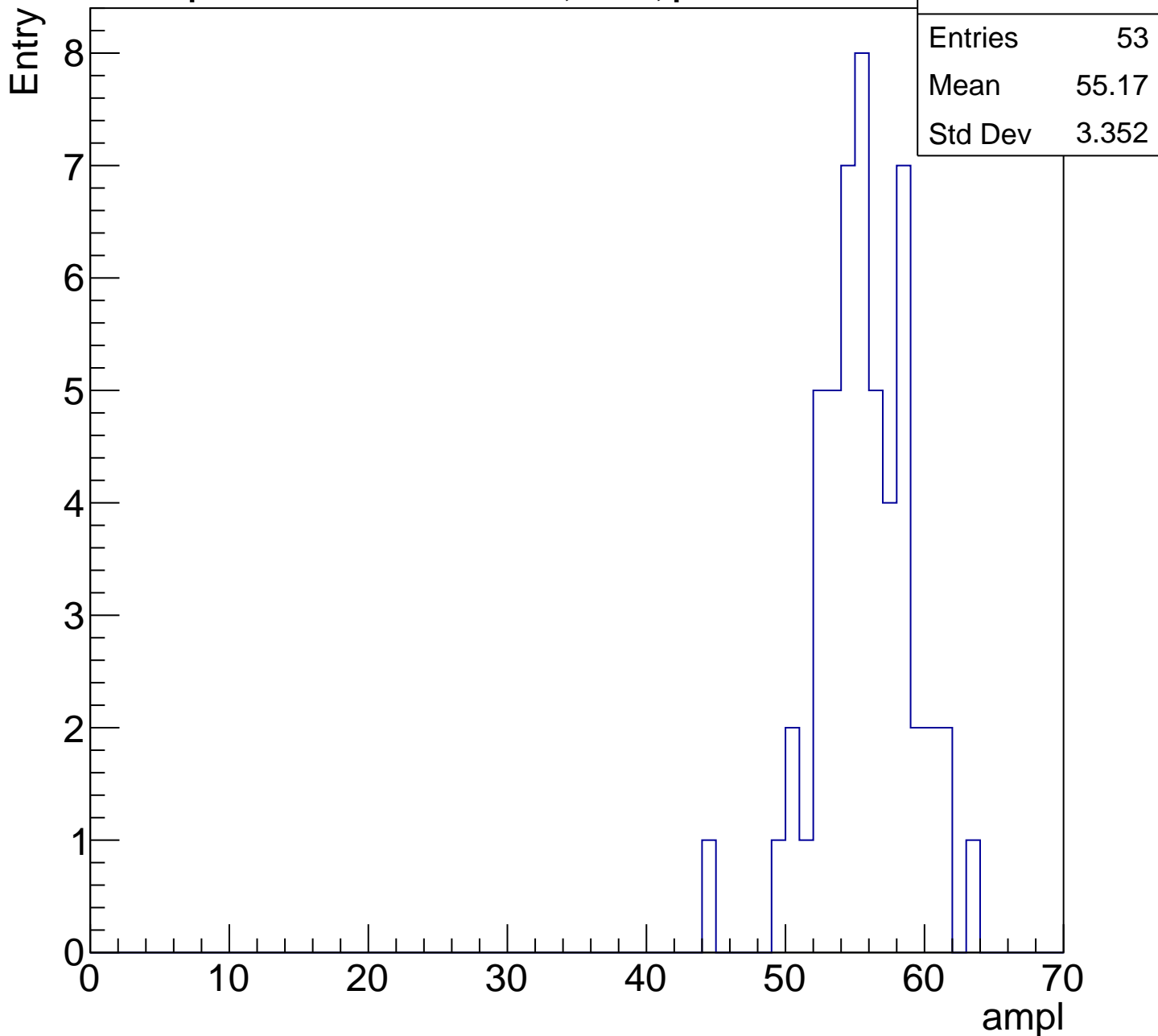
Entry

Entries	65
Mean	48.65
Std Dev	3.236



# B1L103S, U2-ch93, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

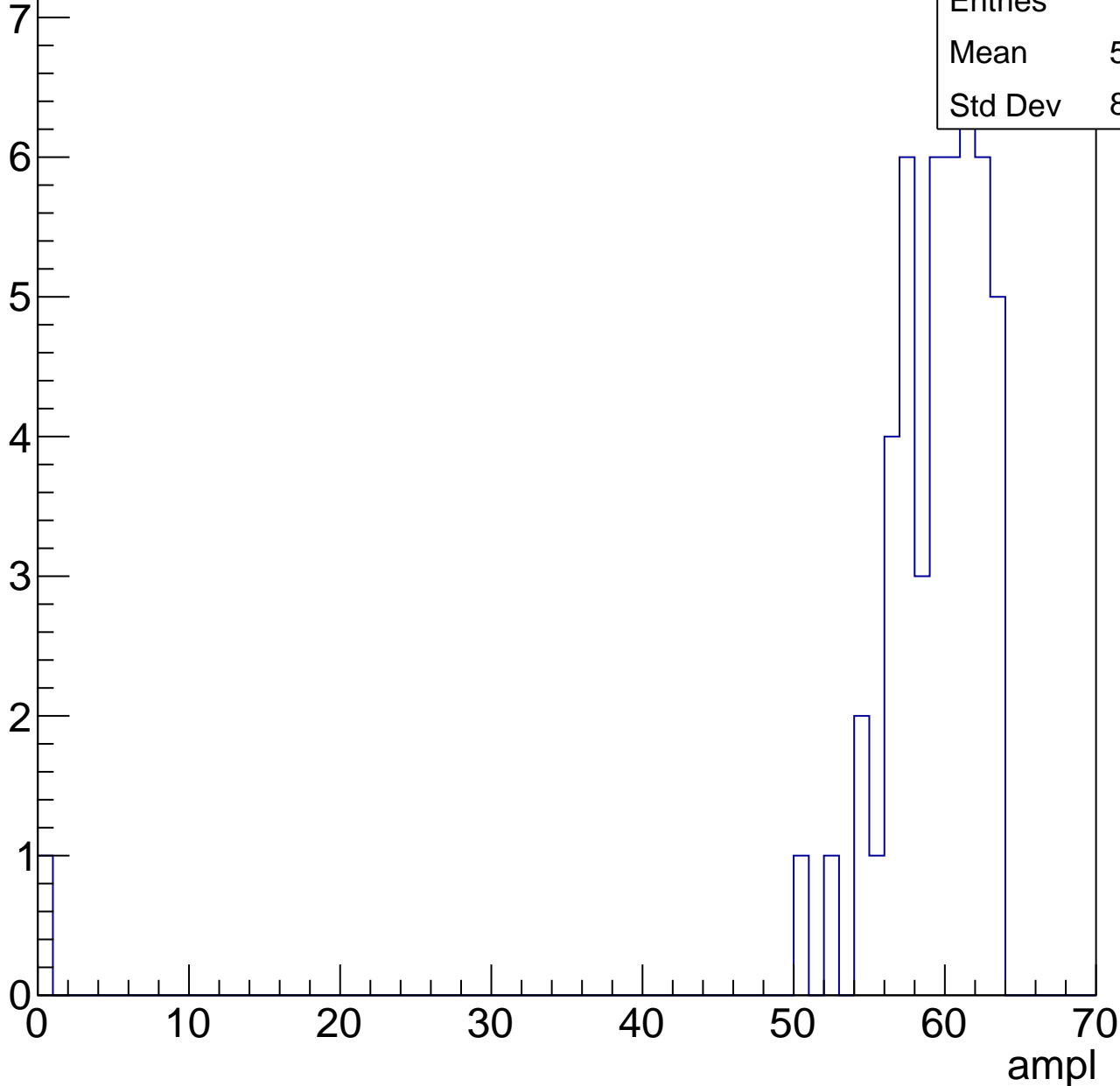


# B1L103S, U2-ch93, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

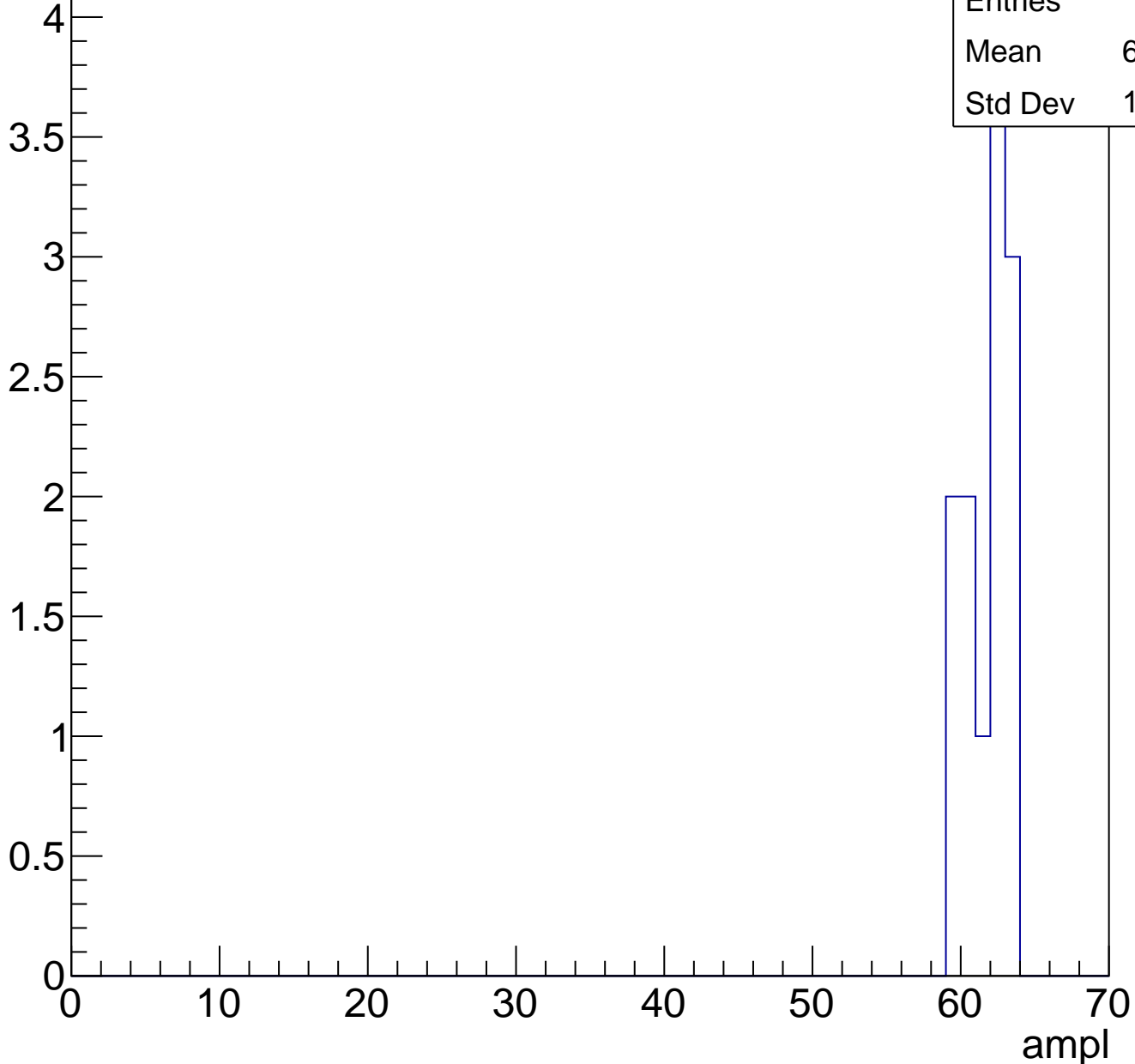
Entries	49
Mean	57.82
Std Dev	8.852



# B1L103S, U2-ch93, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U2-ch93, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch94, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	83
Mean	28.08
Std Dev	5.962

**Gaus mean : 28.9594**

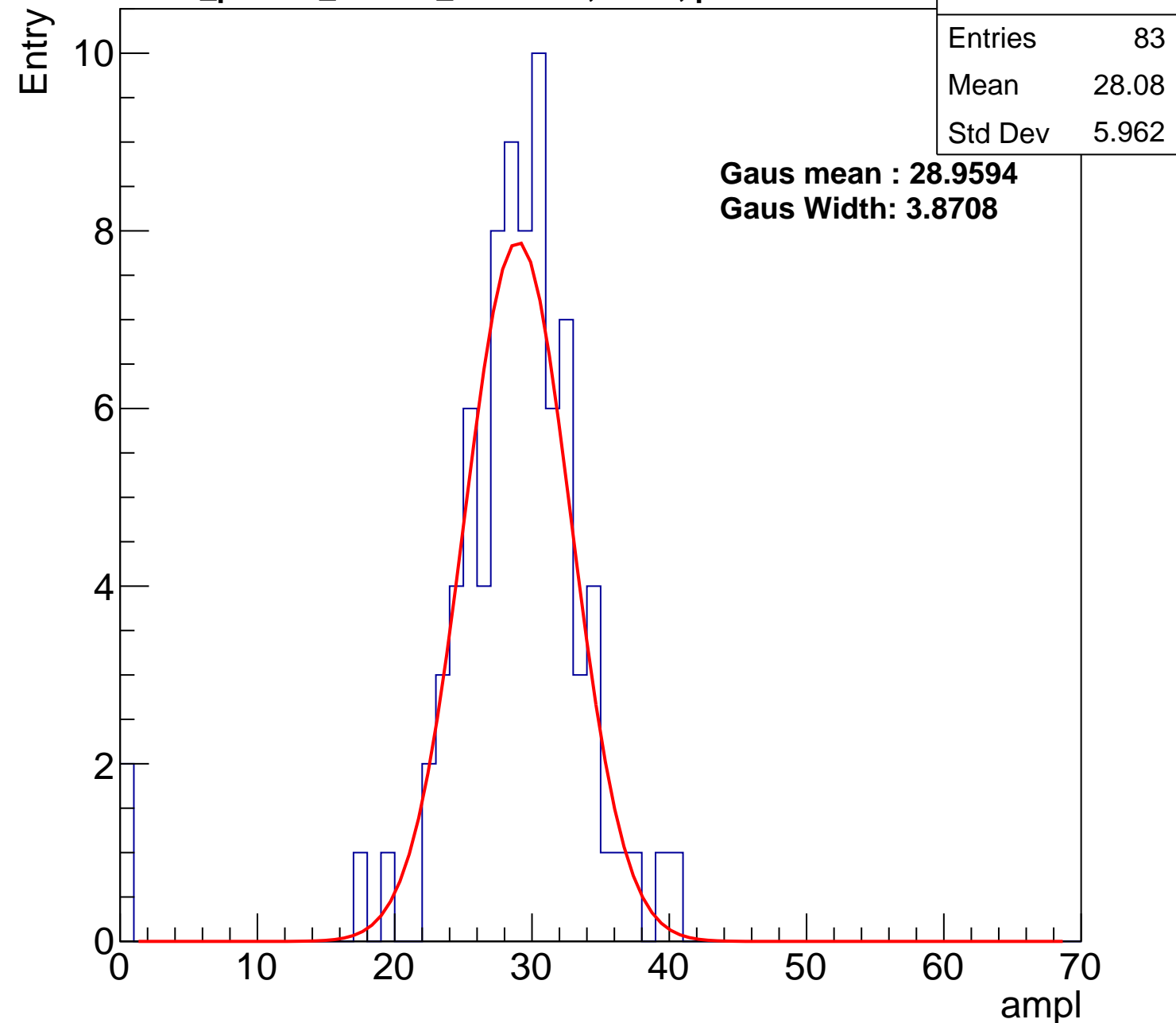
**Gaus Width: 3.8708**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U2-ch94, adc1

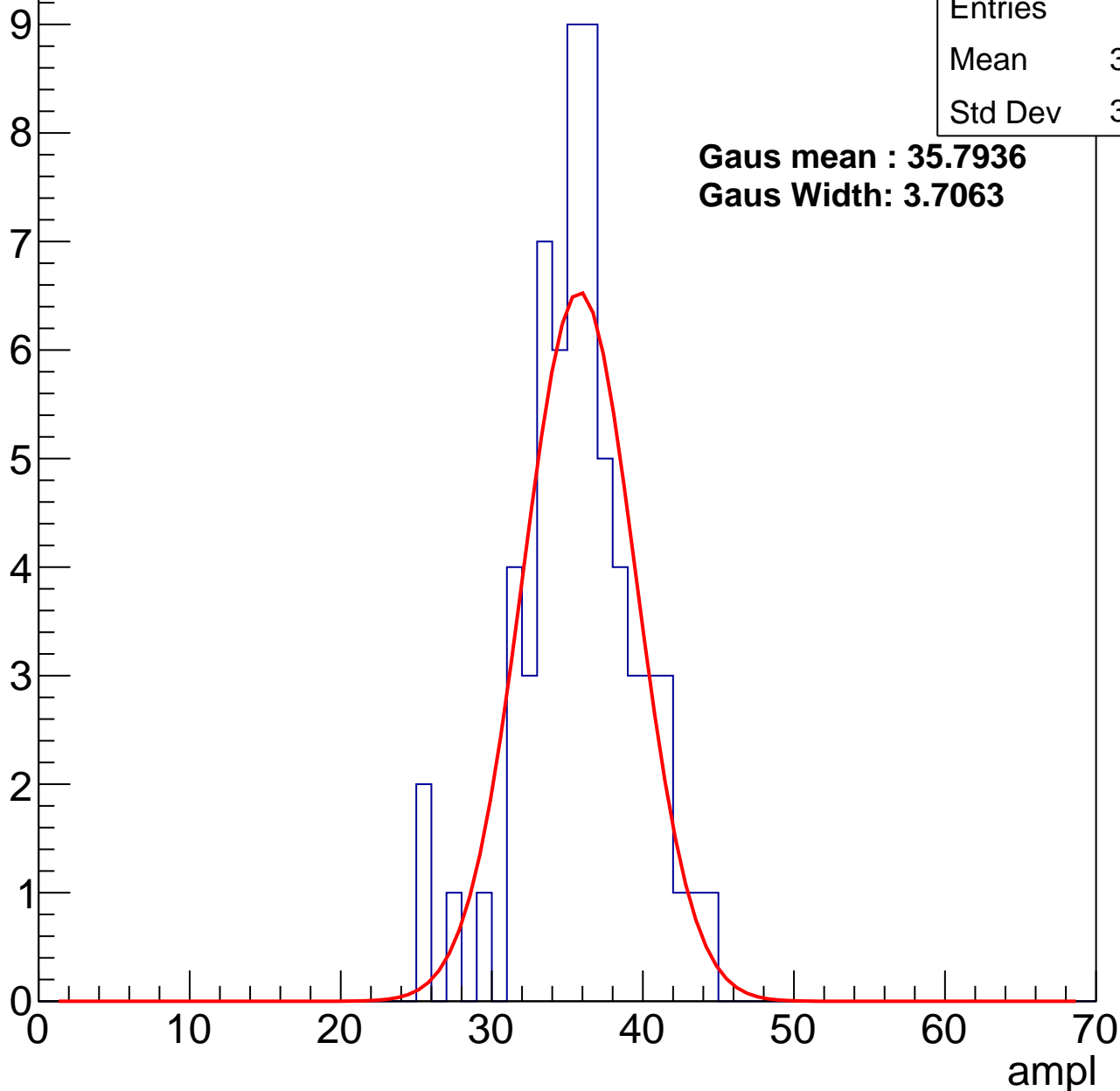
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	35.33
Std Dev	3.796

**Gaus mean : 35.7936**

**Gaus Width: 3.7063**



# B1L103S, U2-ch94, adc2

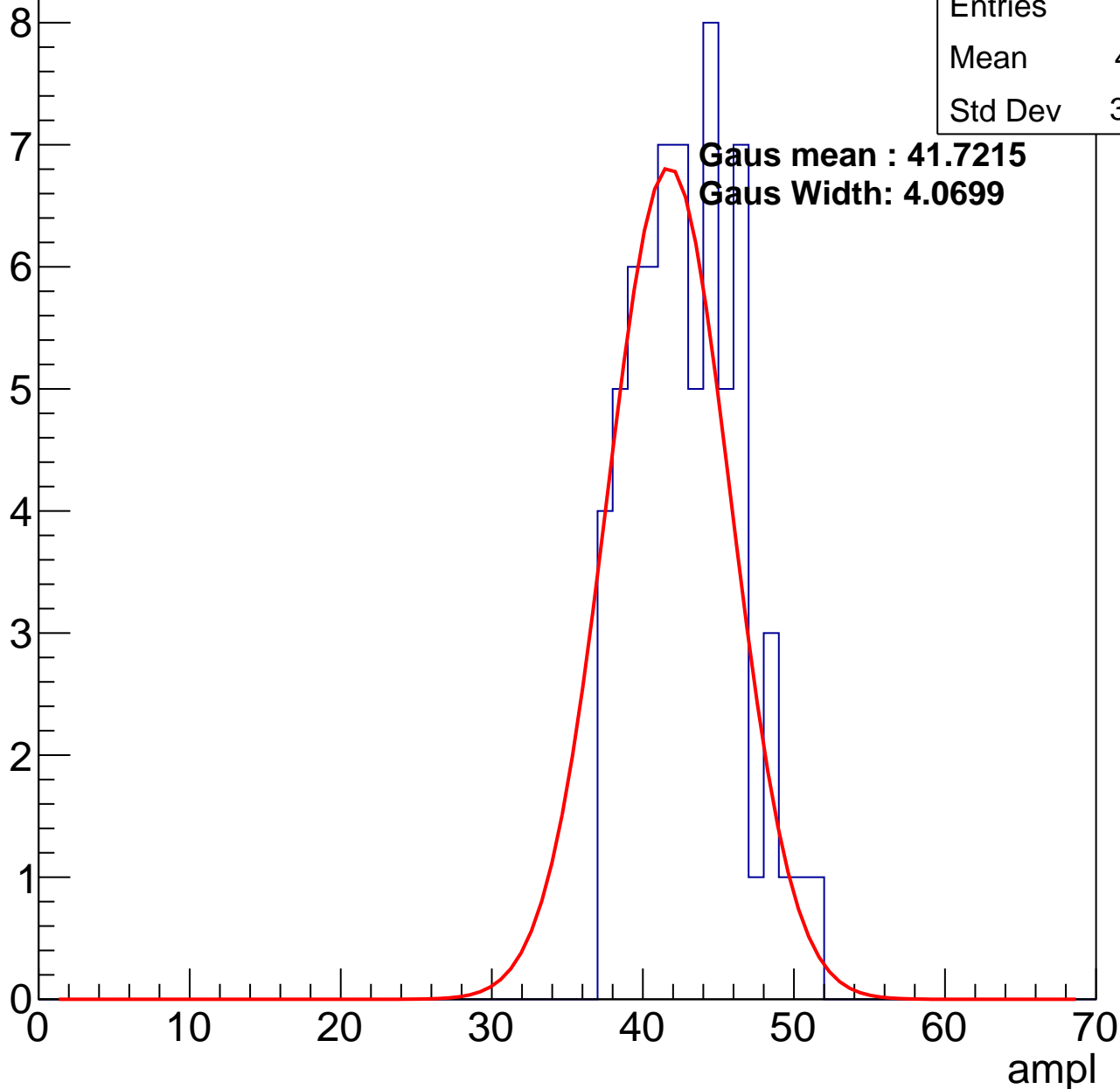
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	42.51
Std Dev	3.387

**Gaus mean : 41.7215**

**Gaus Width: 4.0699**

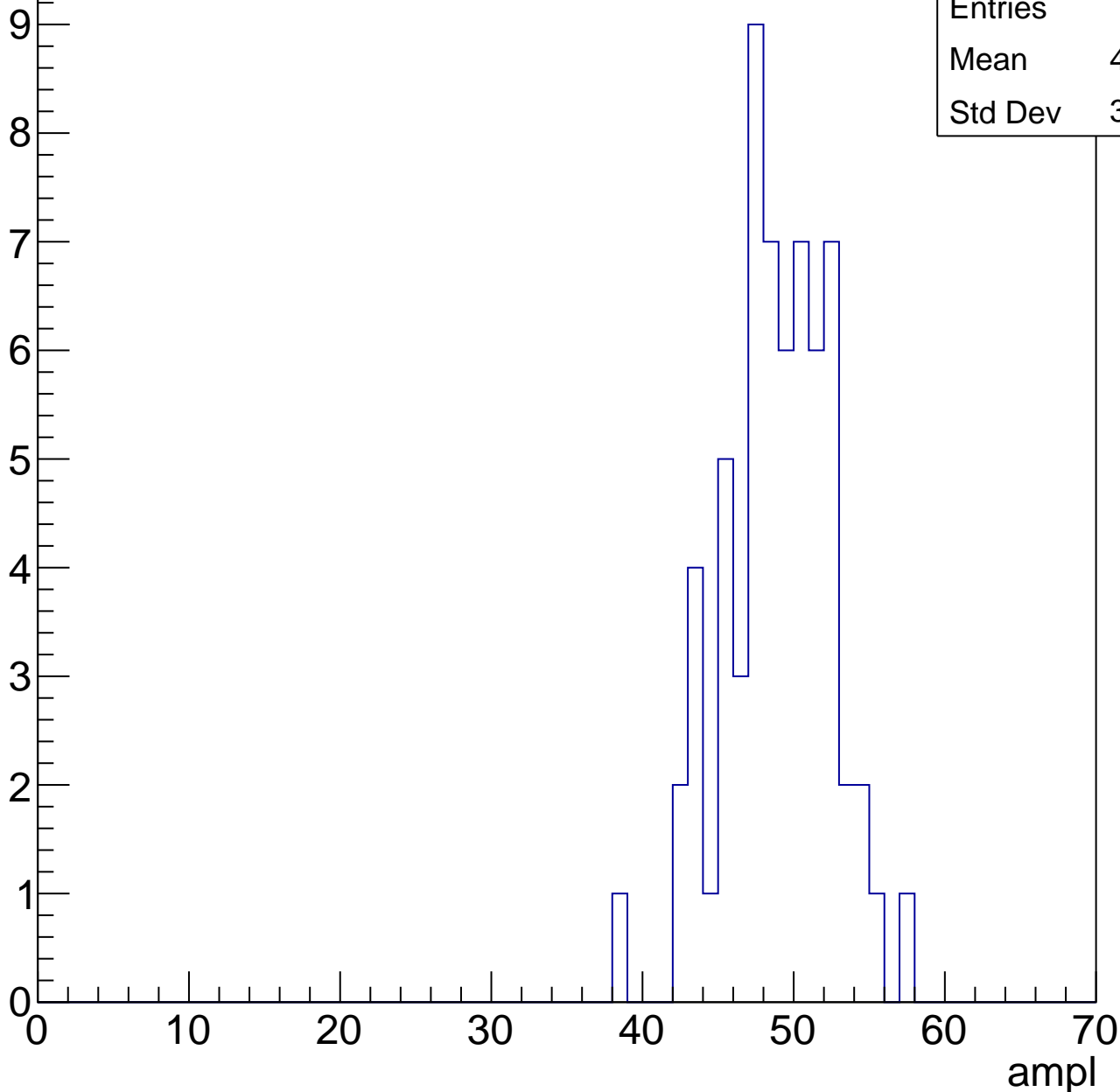


# B1L103S, U2-ch94, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

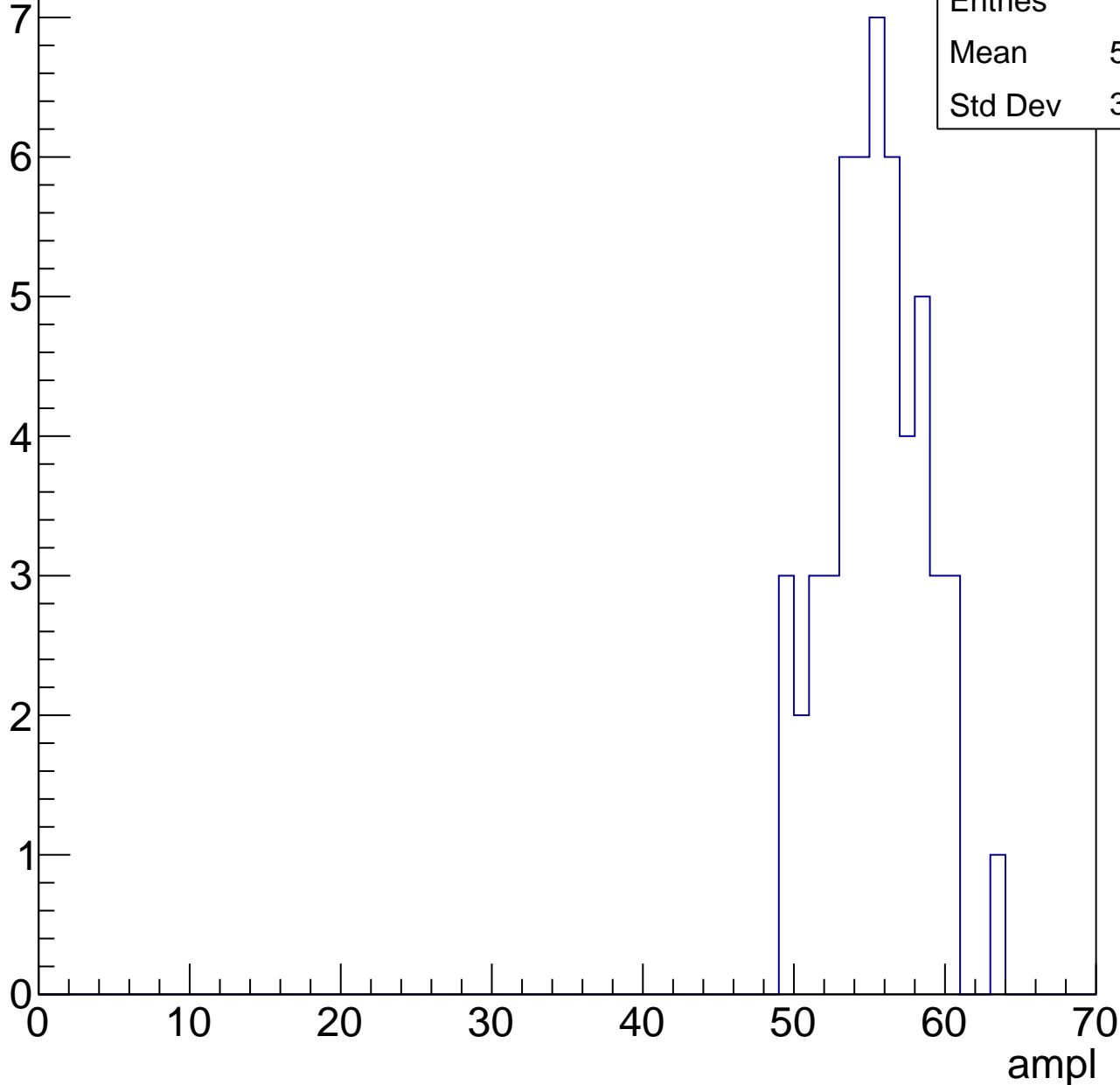
Entries	64
Mean	48.44
Std Dev	3.522



# B1L103S, U2-ch94, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

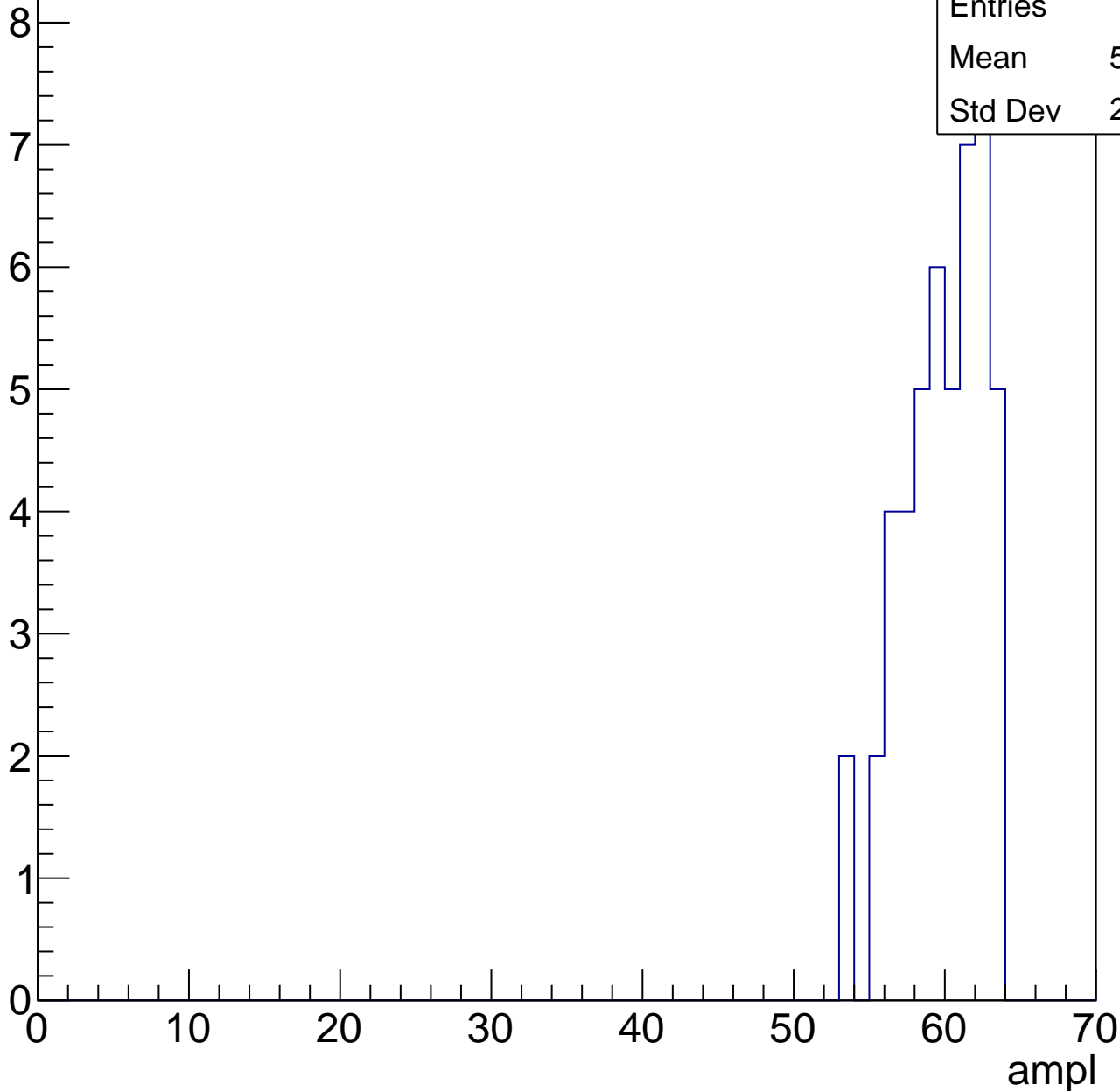


# B1L103S, U2-ch94, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

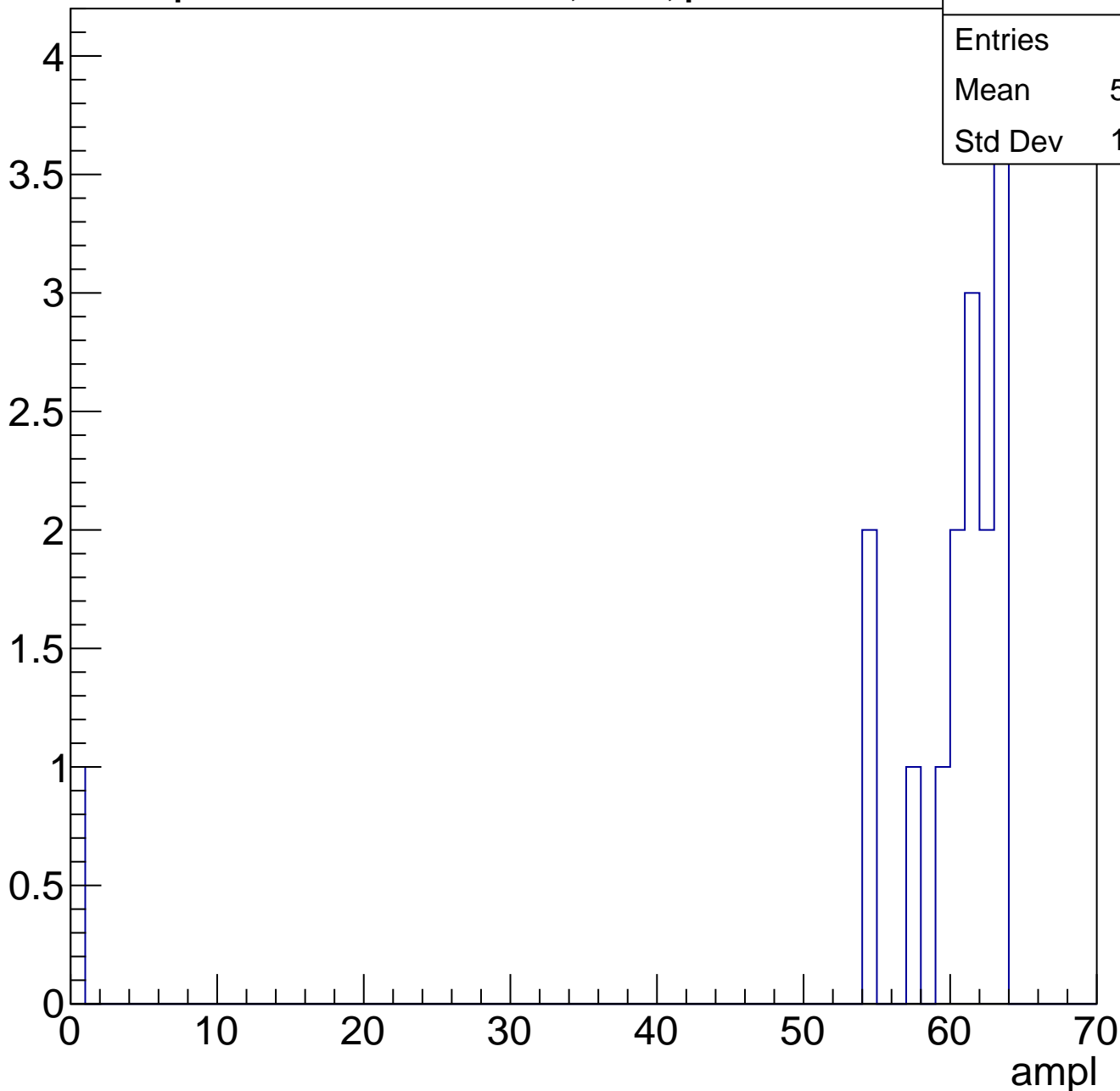
Entries	48
Mean	59.38
Std Dev	2.659



# B1L103S, U2-ch94, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U2-ch94, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U2-ch95, adc0

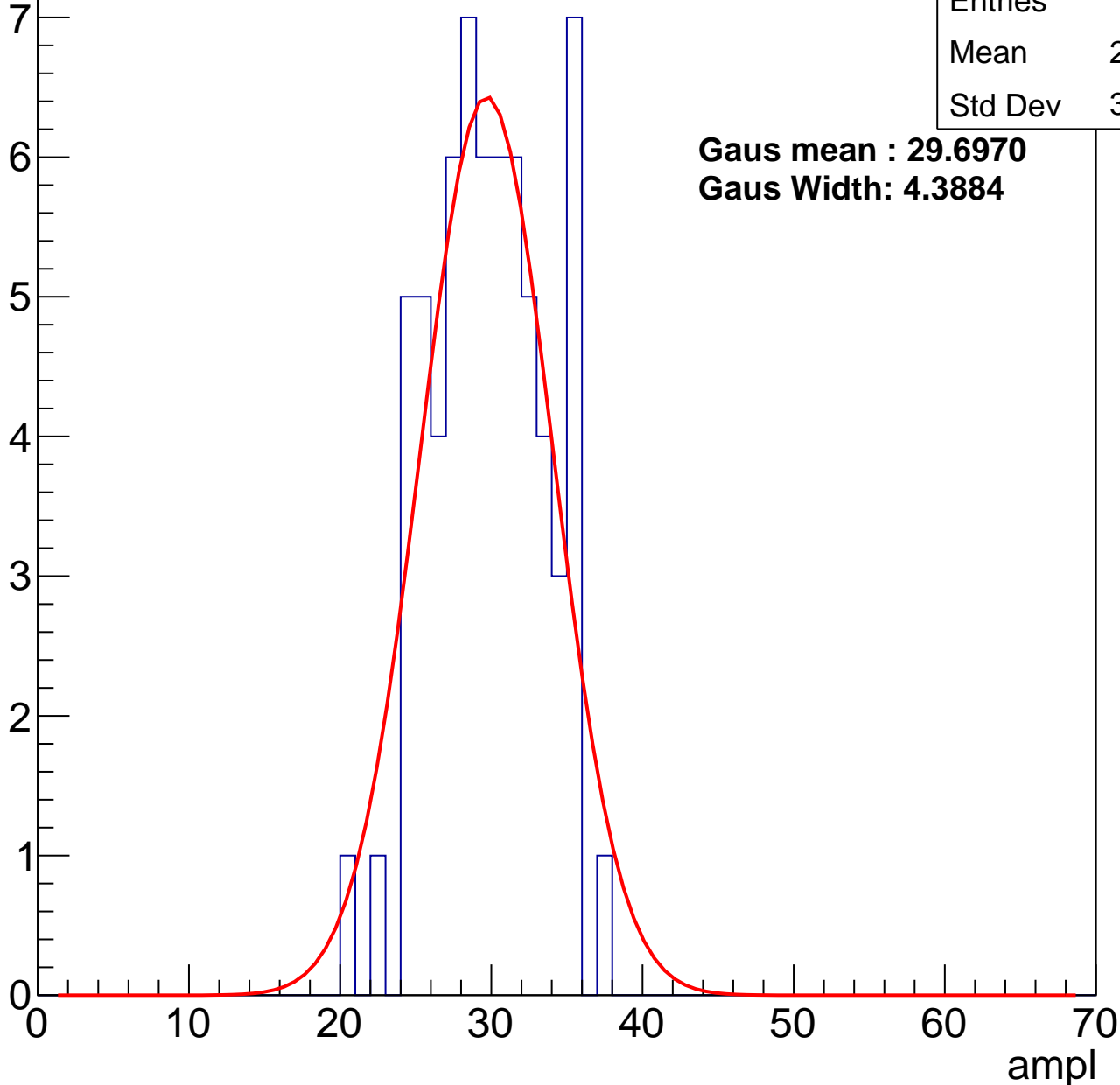
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	29.33
Std Dev	3.715

**Gaus mean : 29.6970**

**Gaus Width: 4.3884**



# B1L103S, U2-ch95, adc1

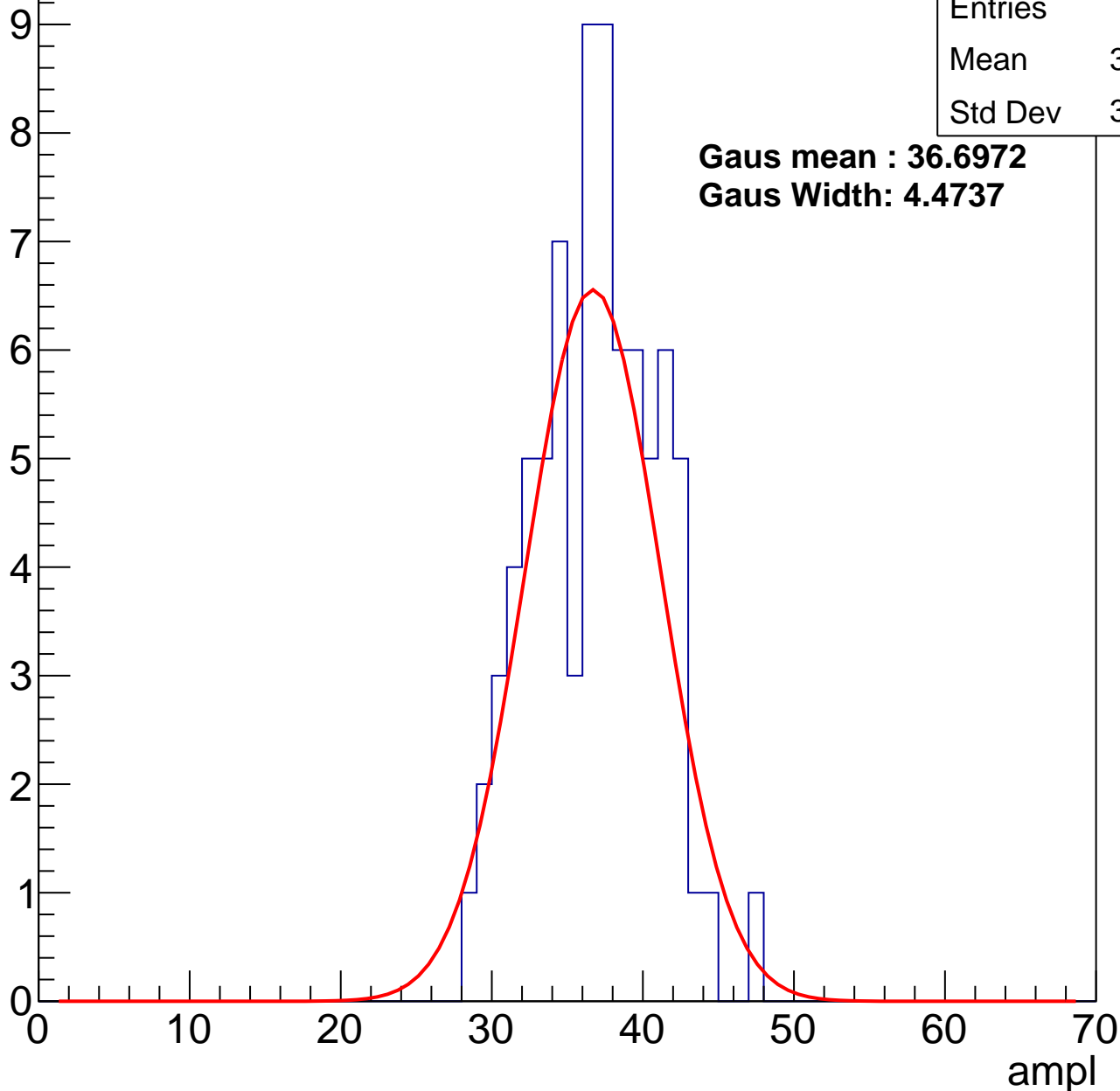
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	79
Mean	36.42
Std Dev	3.967

**Gaus mean : 36.6972**

**Gaus Width: 4.4737**



# B1L103S, U2-ch95, adc2

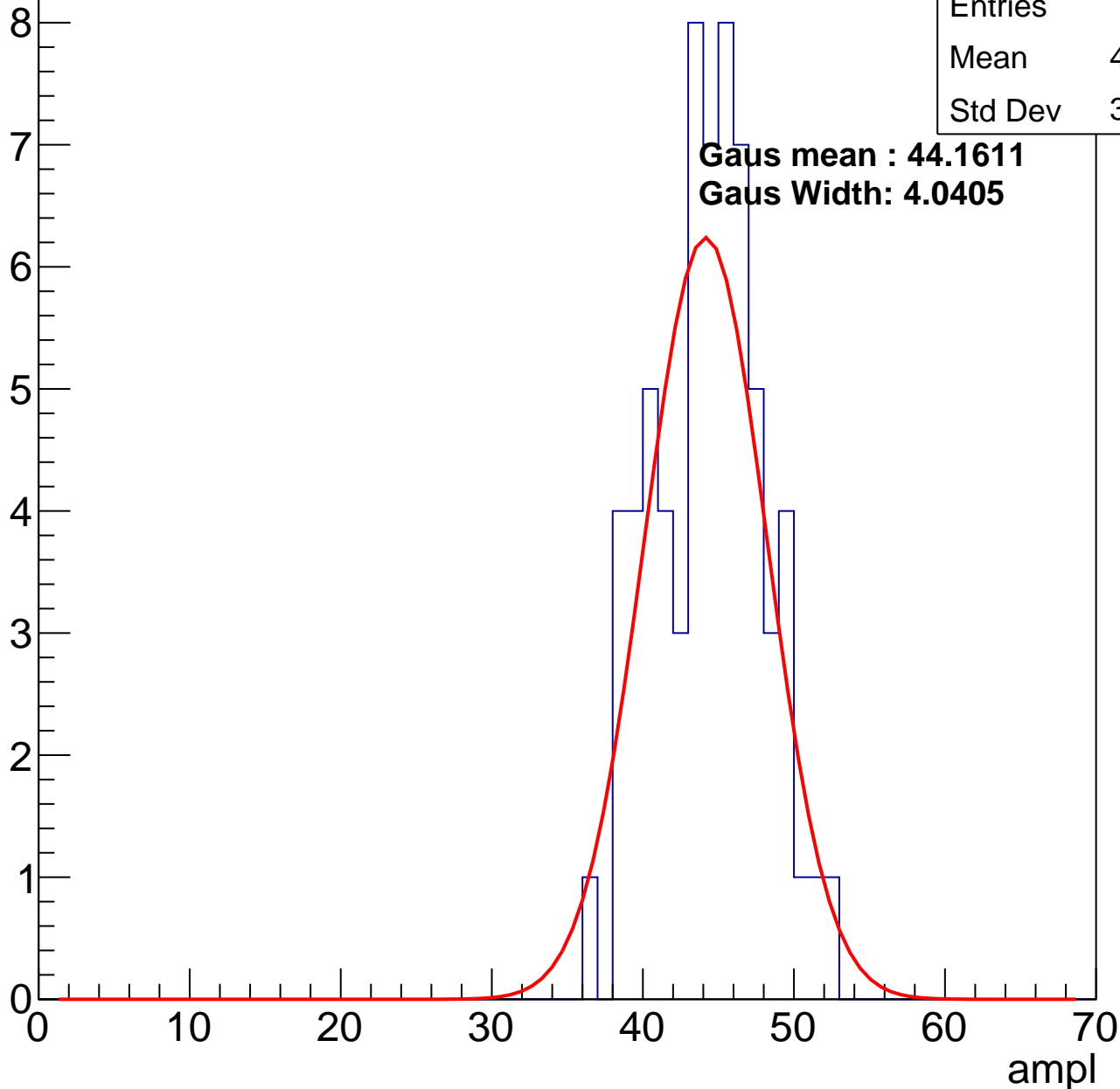
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	43.88
Std Dev	3.527

**Gaus mean : 44.1611**

**Gaus Width: 4.0405**

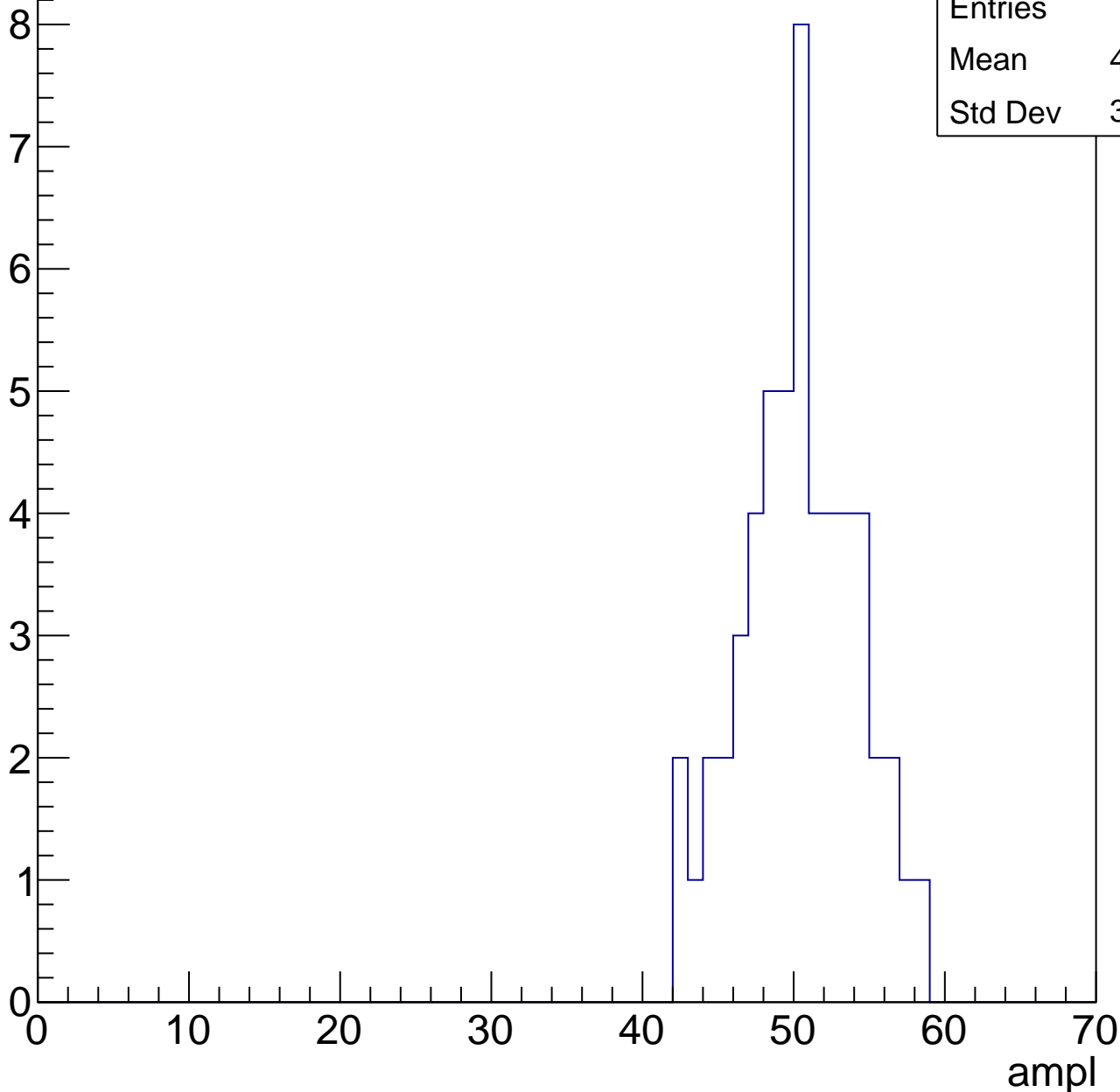


# B1L103S, U2-ch95, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

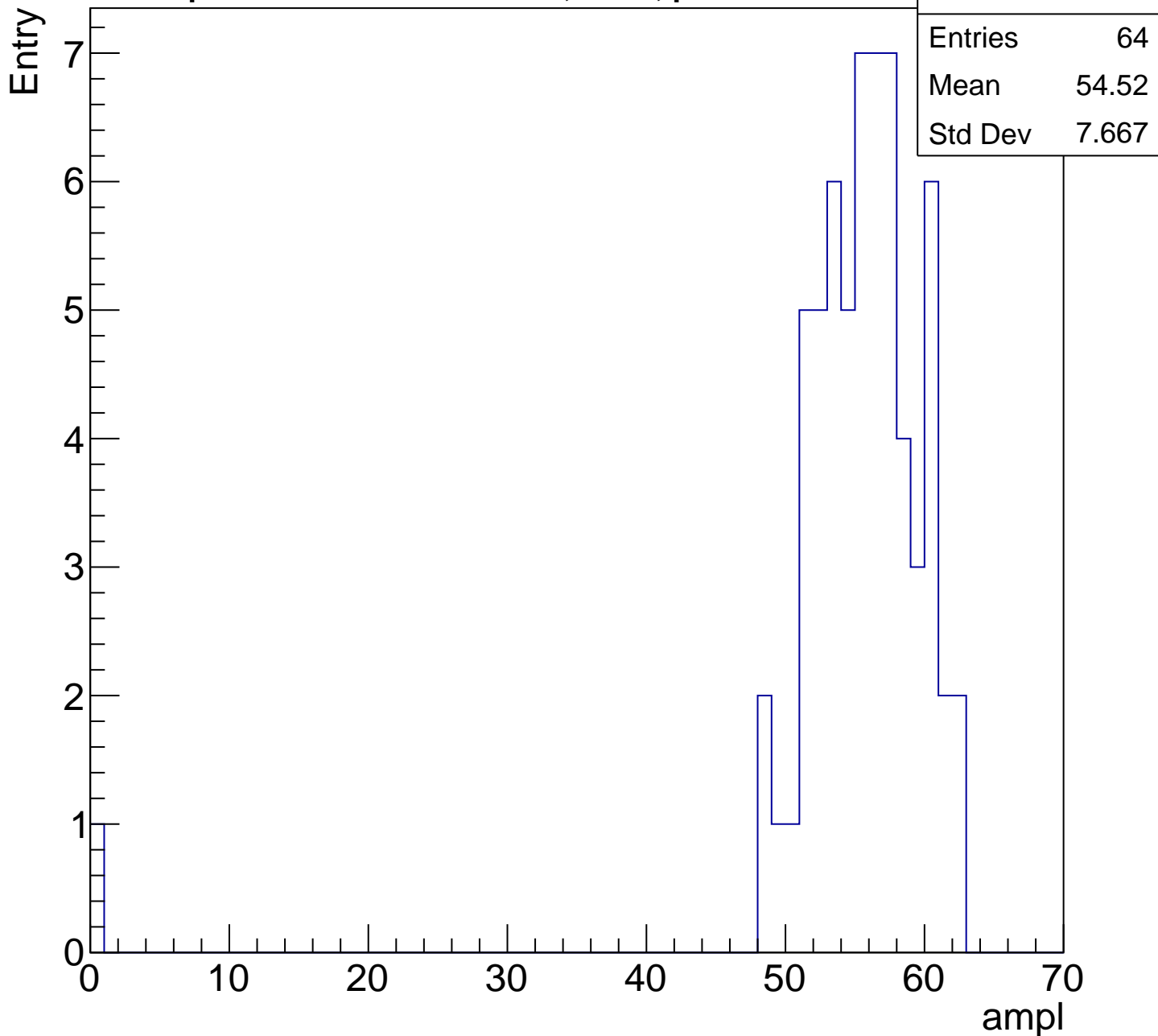
Entry

Entries	54
Mean	49.87
Std Dev	3.757



# B1L103S, U2-ch95, adc4

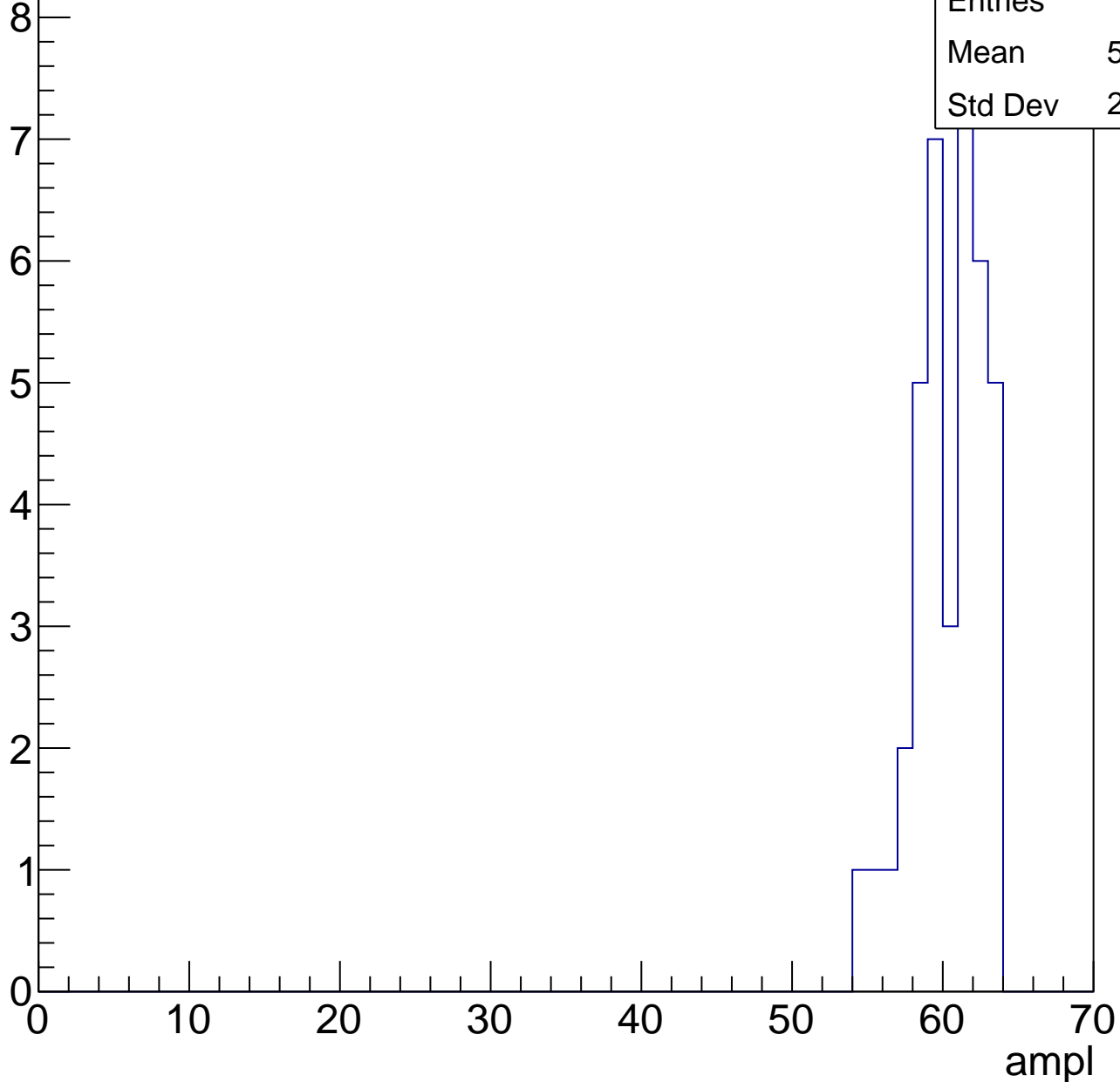
calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U2-ch95, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



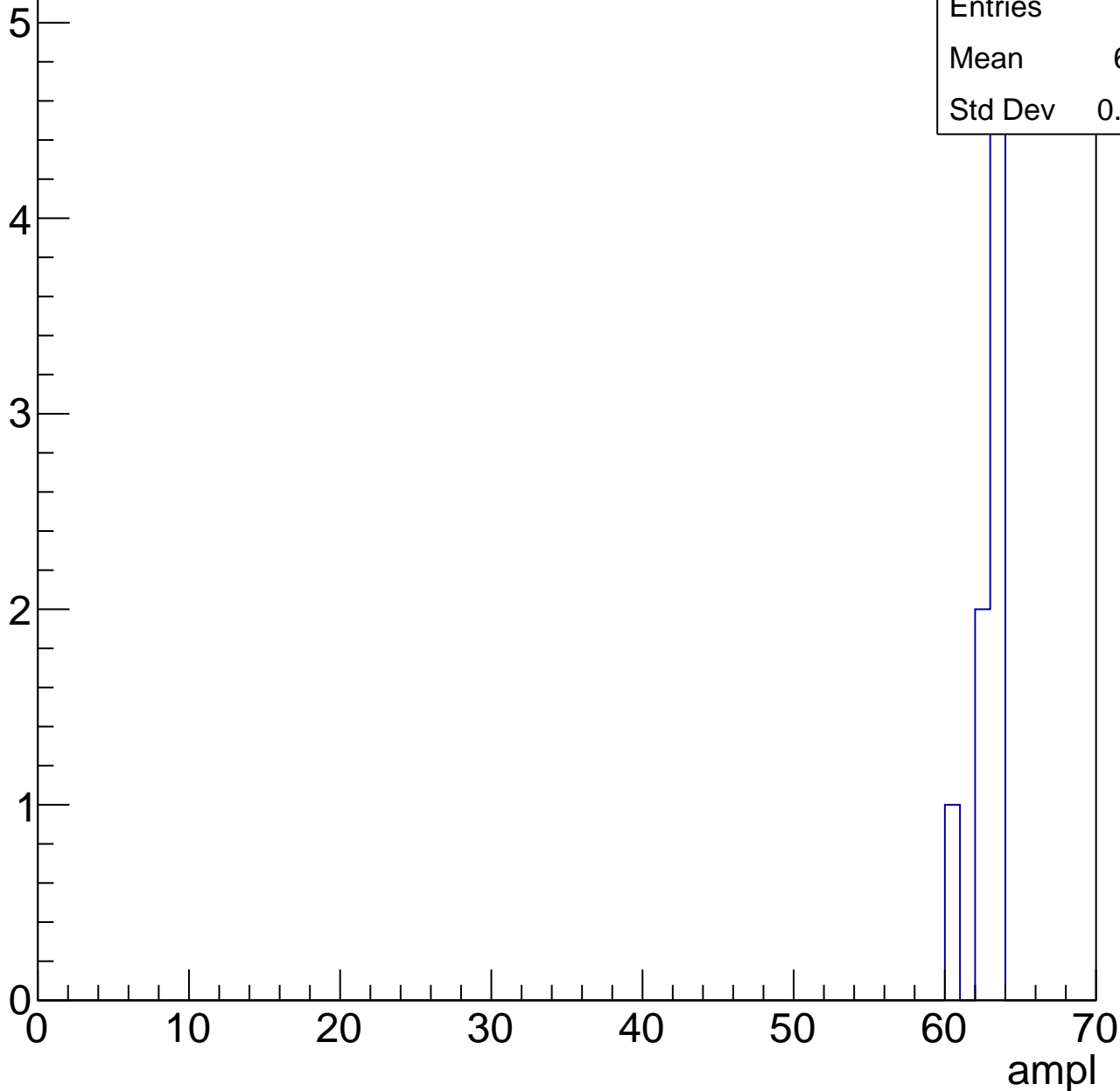
Entries	39
Mean	59.92
Std Dev	2.258

# B1L103S, U2-ch95, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	8
Mean	62.38
Std Dev	0.9922





# B1L103S, U2-ch95, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L103S, U2-ch96, adc0

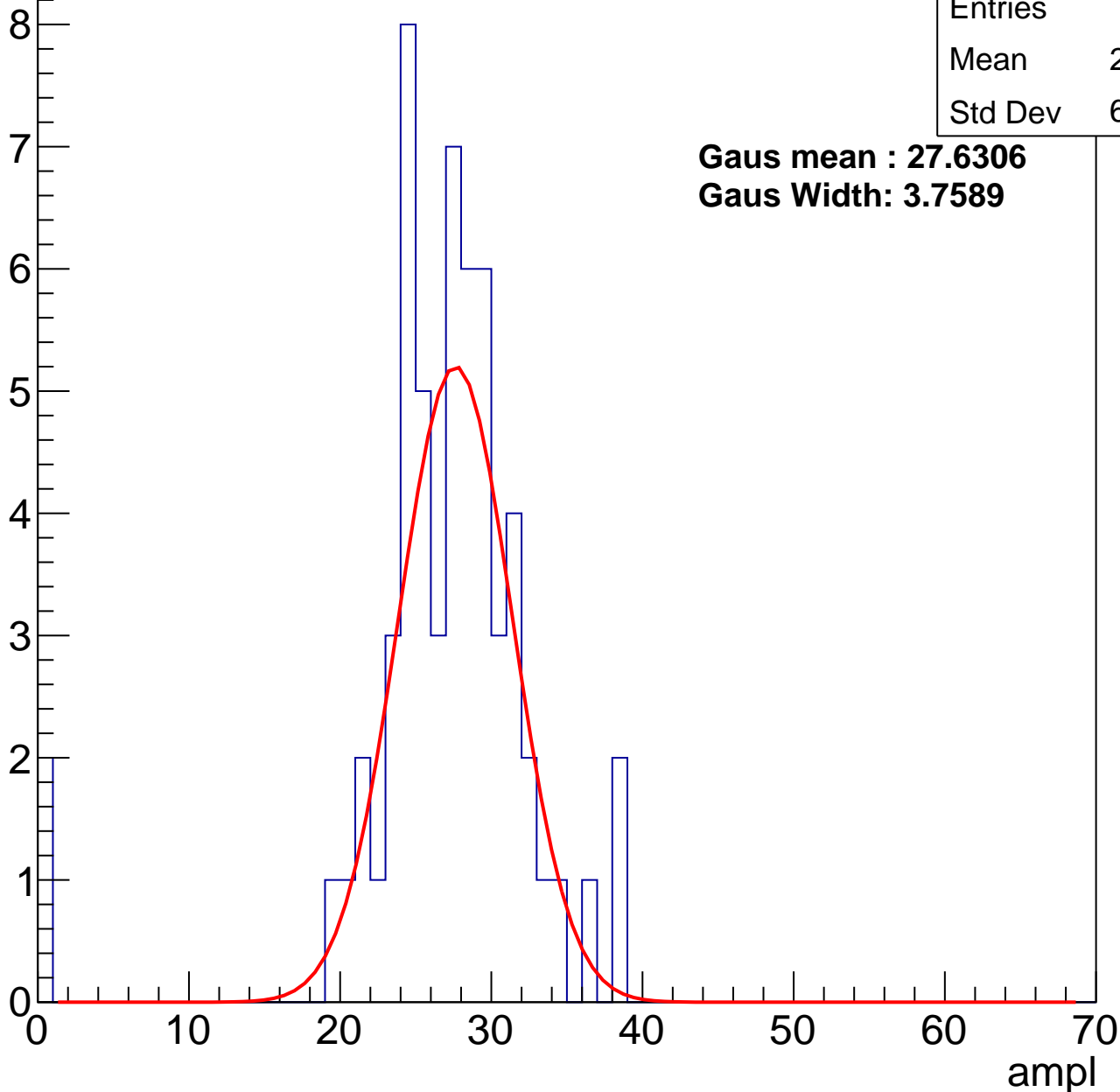
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	26.36
Std Dev	6.332

**Gaus mean : 27.6306**

**Gaus Width: 3.7589**



# B1L103S, U2-ch96, adc1

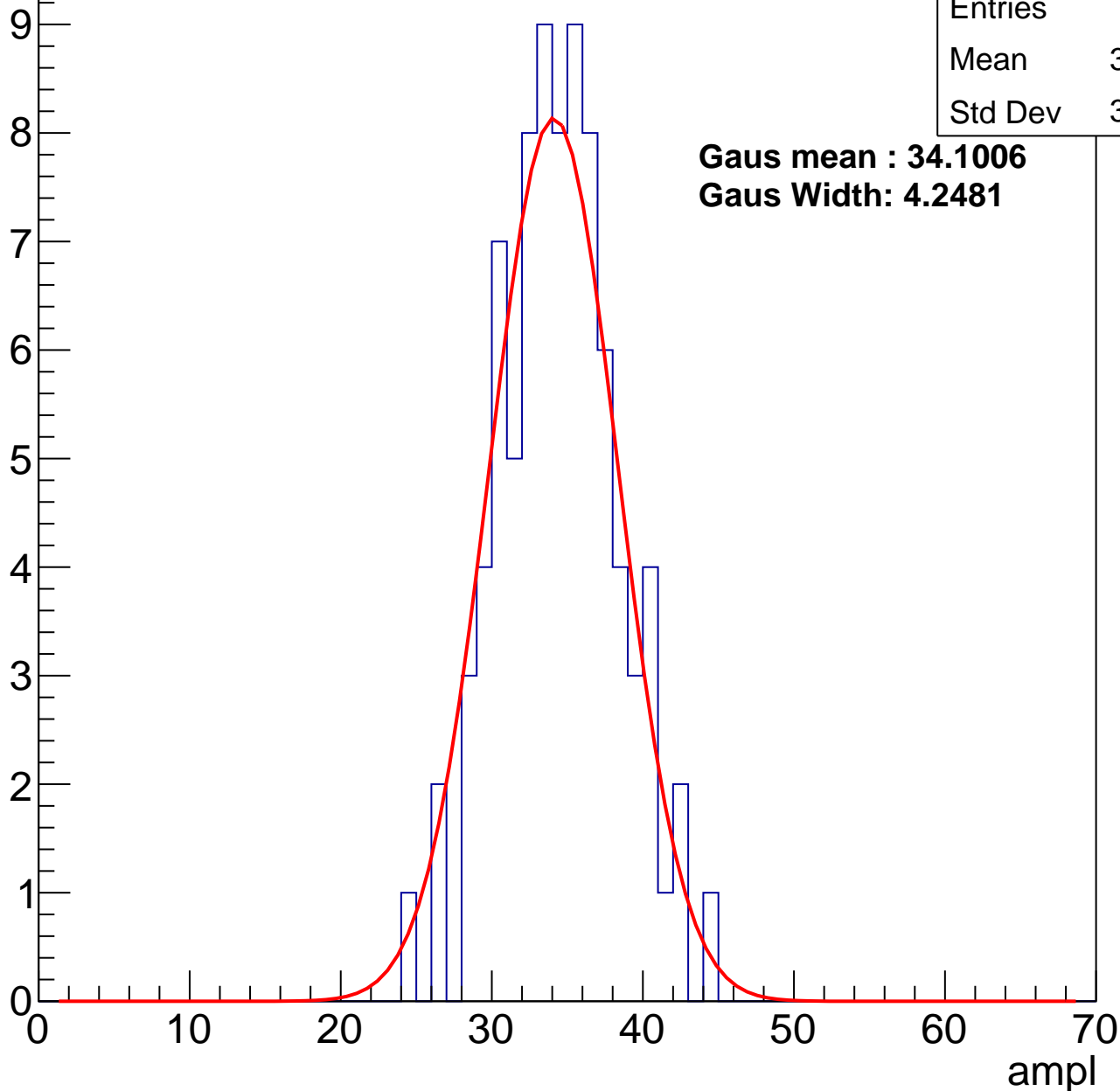
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	85
Mean	33.99
Std Dev	3.894

**Gaus mean : 34.1006**

**Gaus Width: 4.2481**



# B1L103S, U2-ch96, adc2

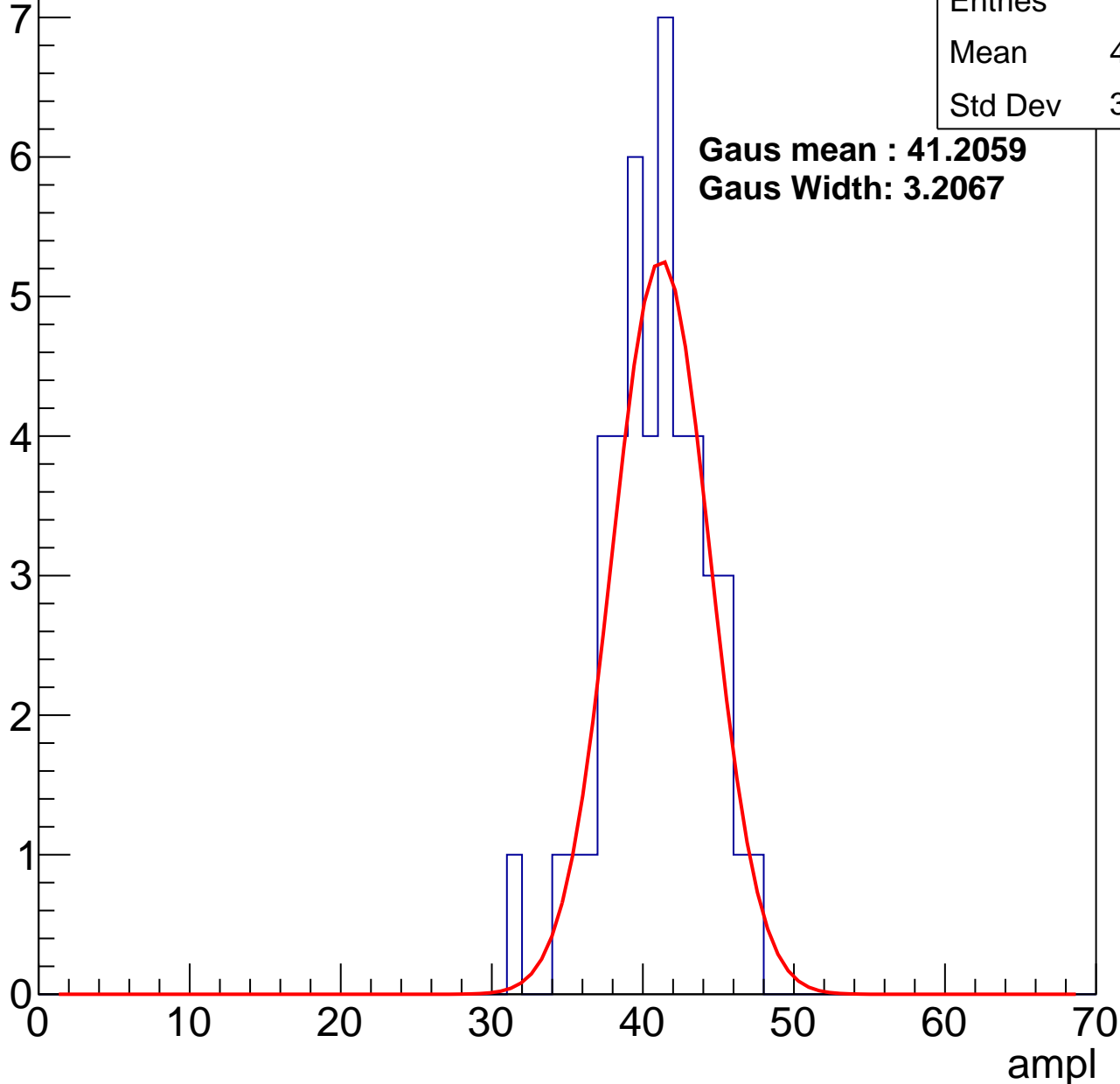
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	45
Mean	40.38
Std Dev	3.254

**Gaus mean : 41.2059**

**Gaus Width: 3.2067**

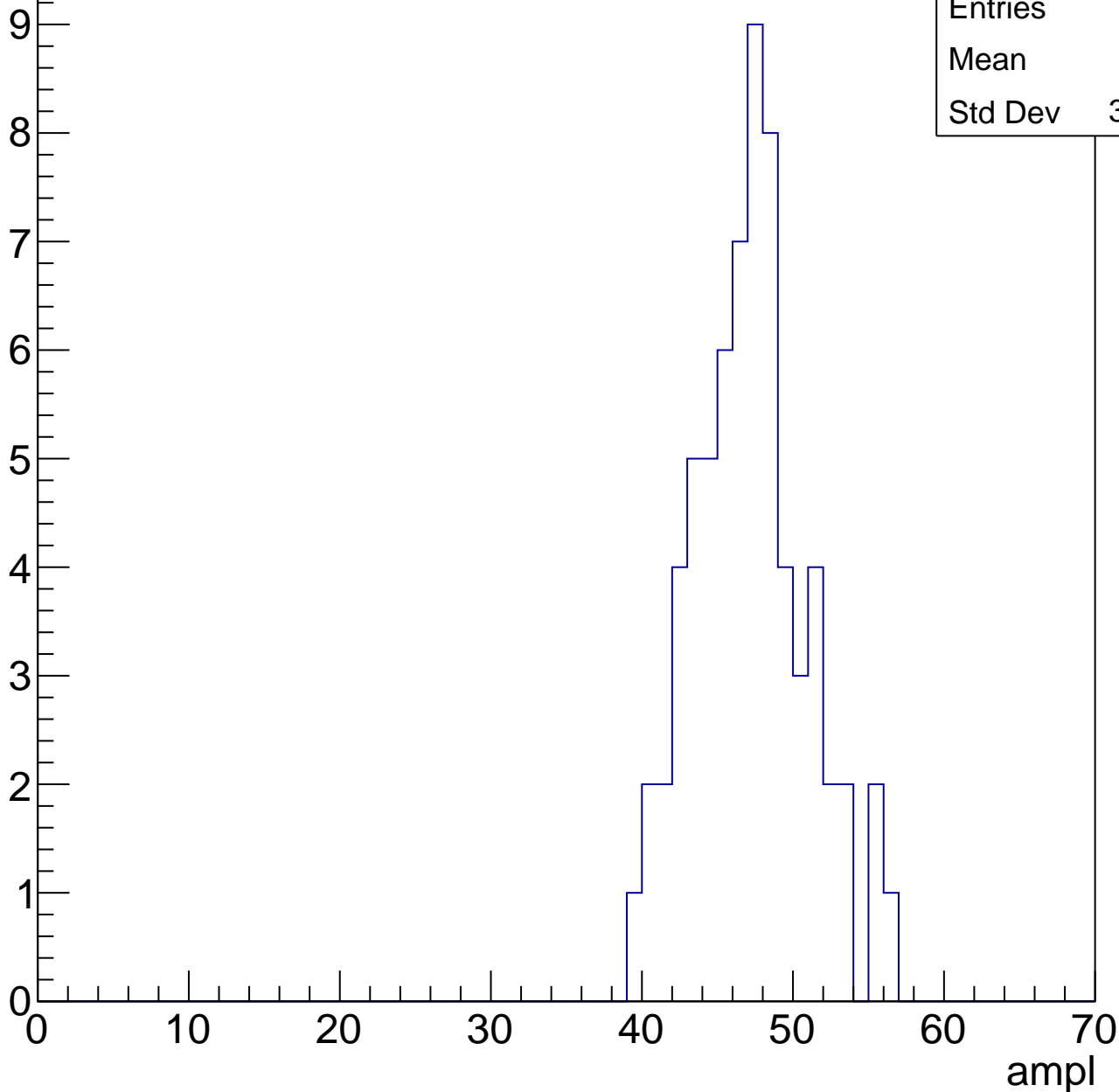


# B1L103S, U2-ch96, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

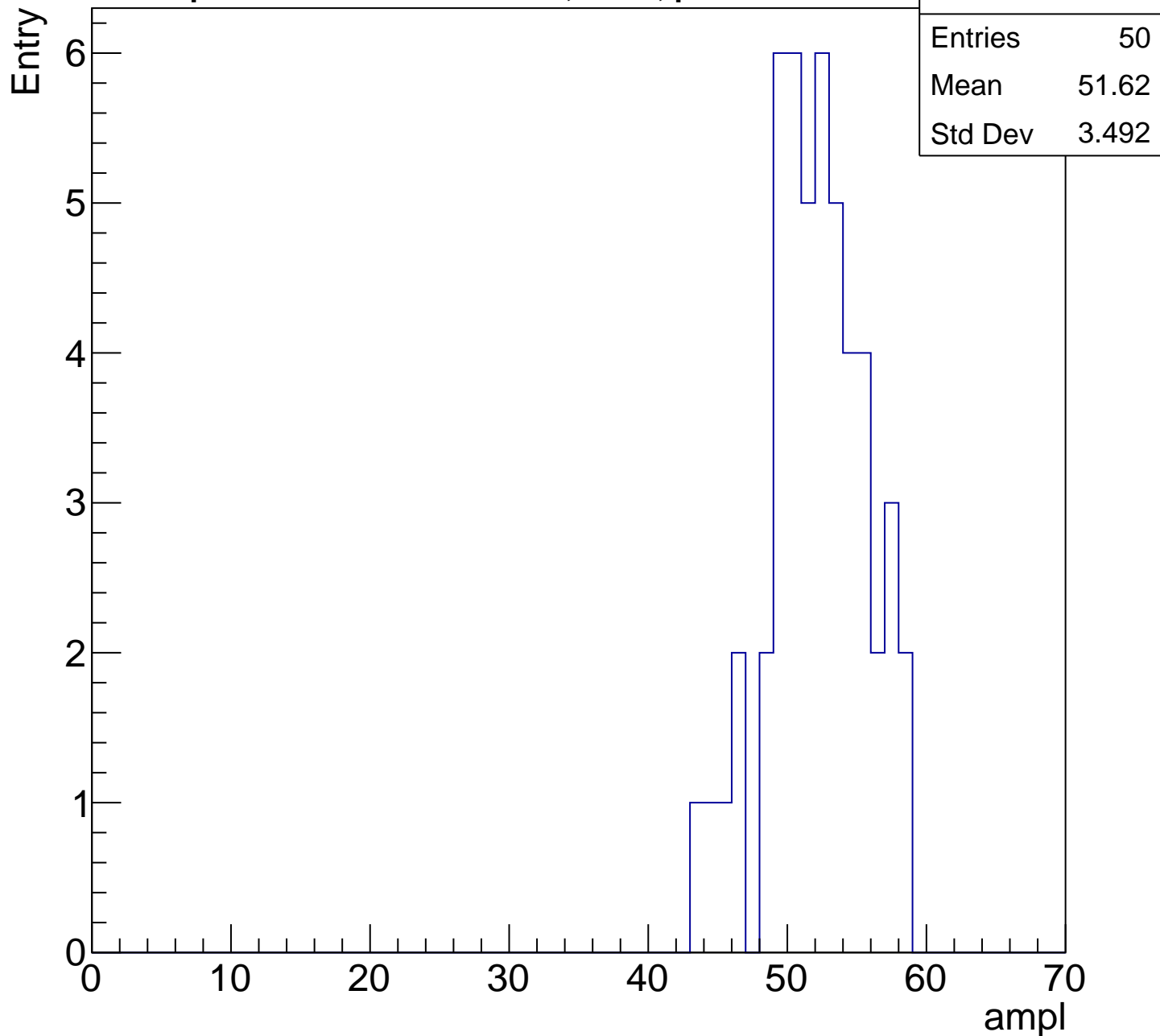
Entry

Entries	67
Mean	46.7
Std Dev	3.726



# B1L103S, U2-ch96, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

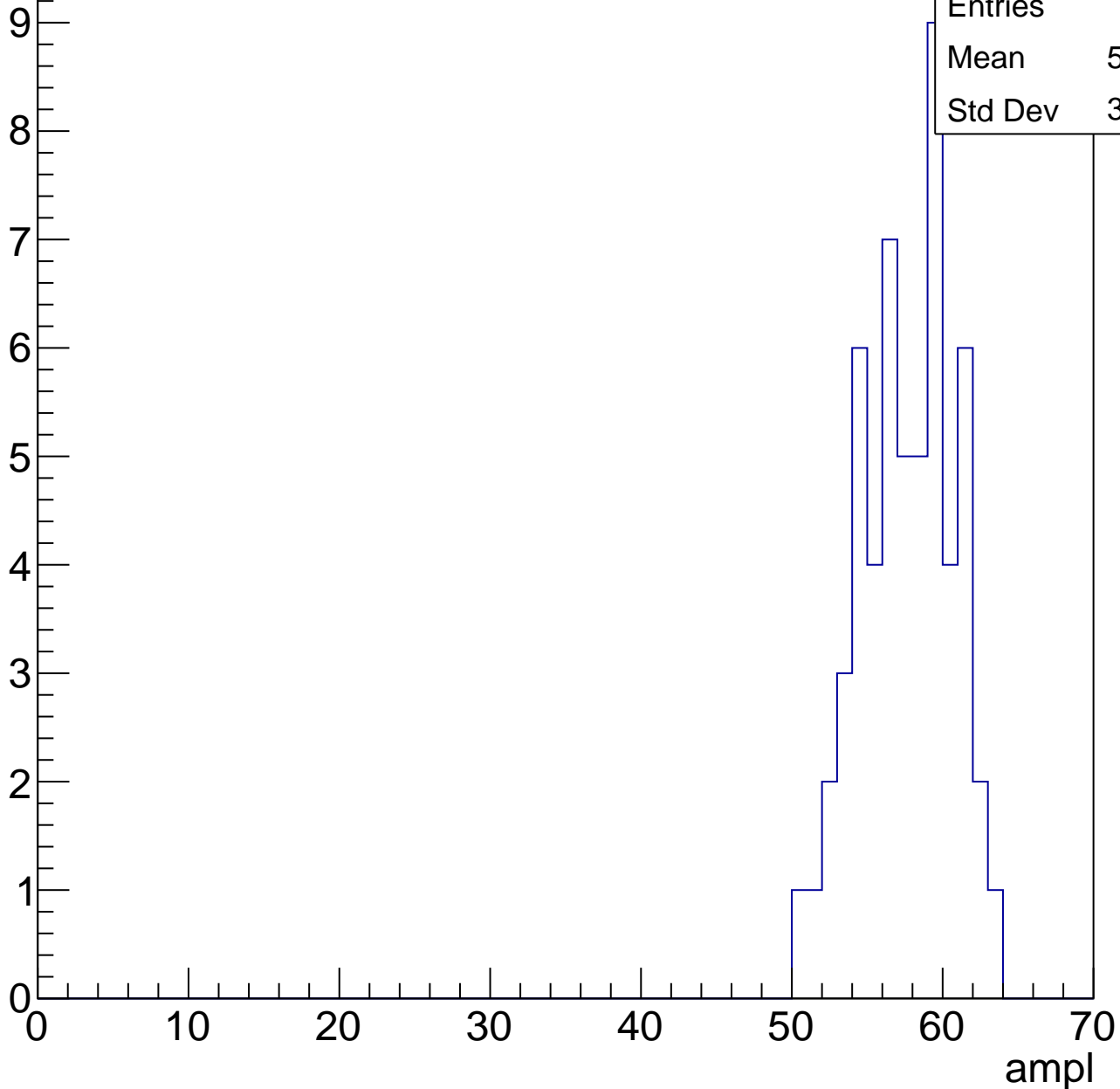


# B1L103S, U2-ch96, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	57.12
Std Dev	3.042

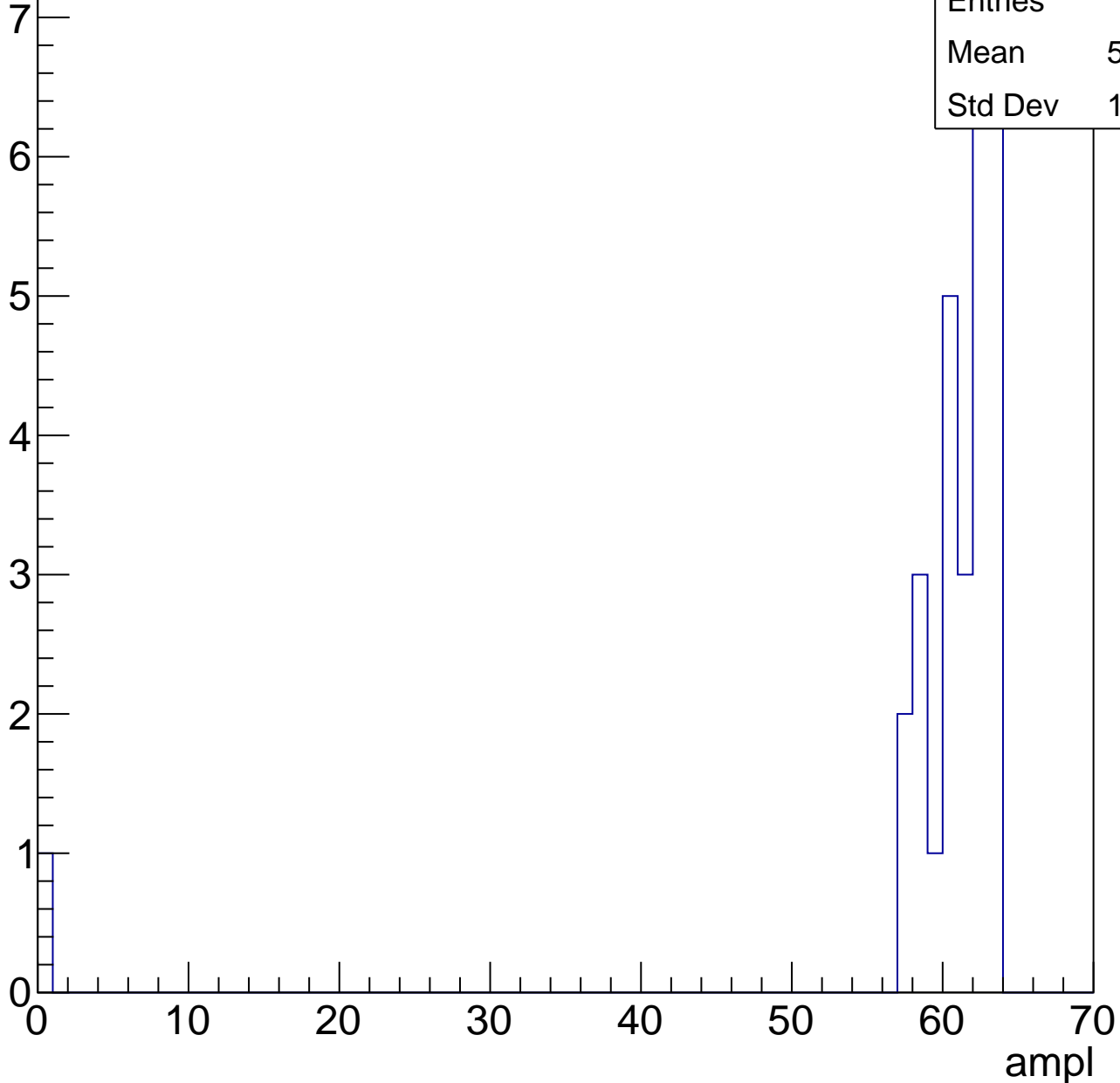


# B1L103S, U2-ch96, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	29
Mean	58.79
Std Dev	11.27

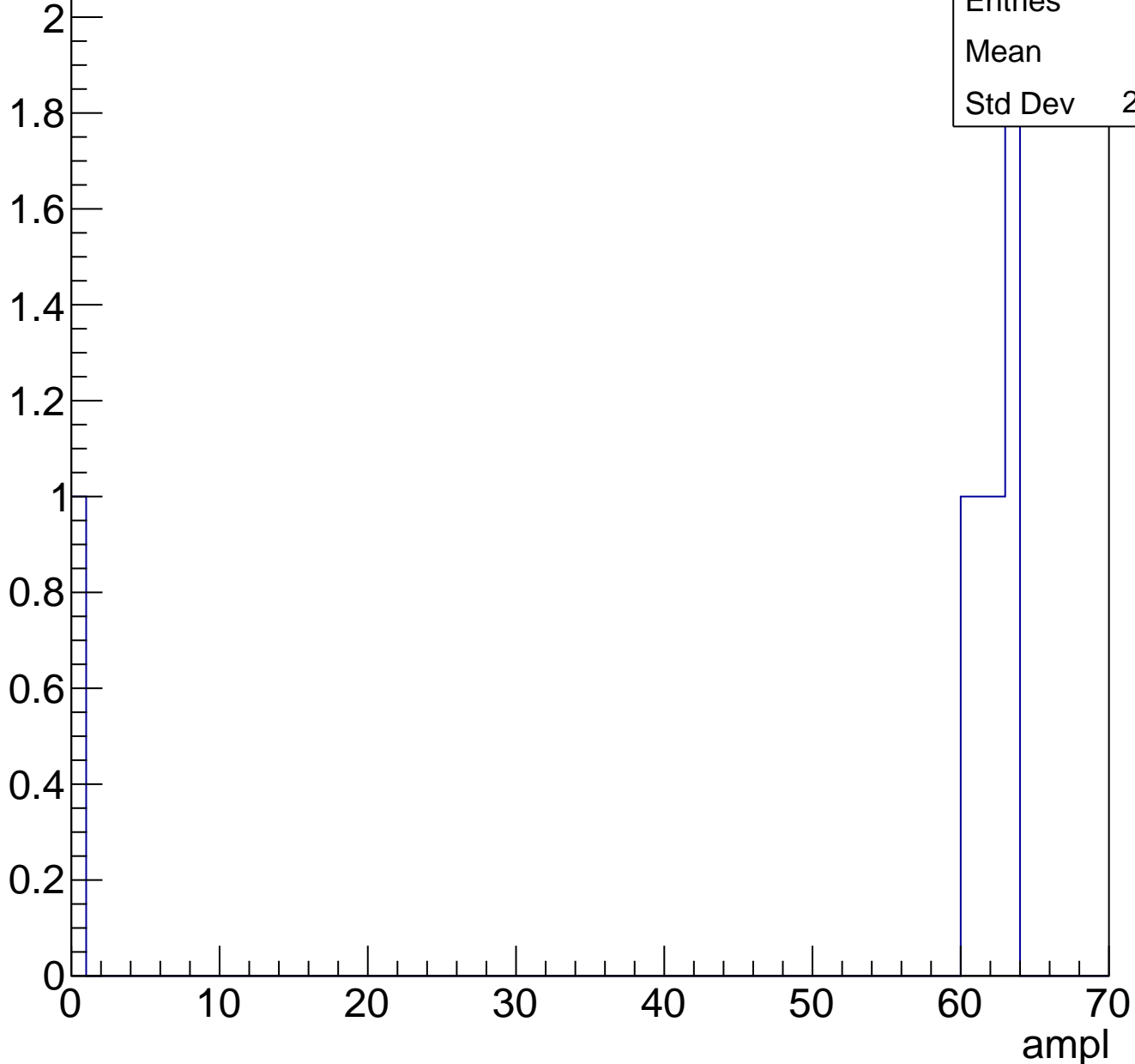




# B1L103S, U2-ch96, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch97, adc0

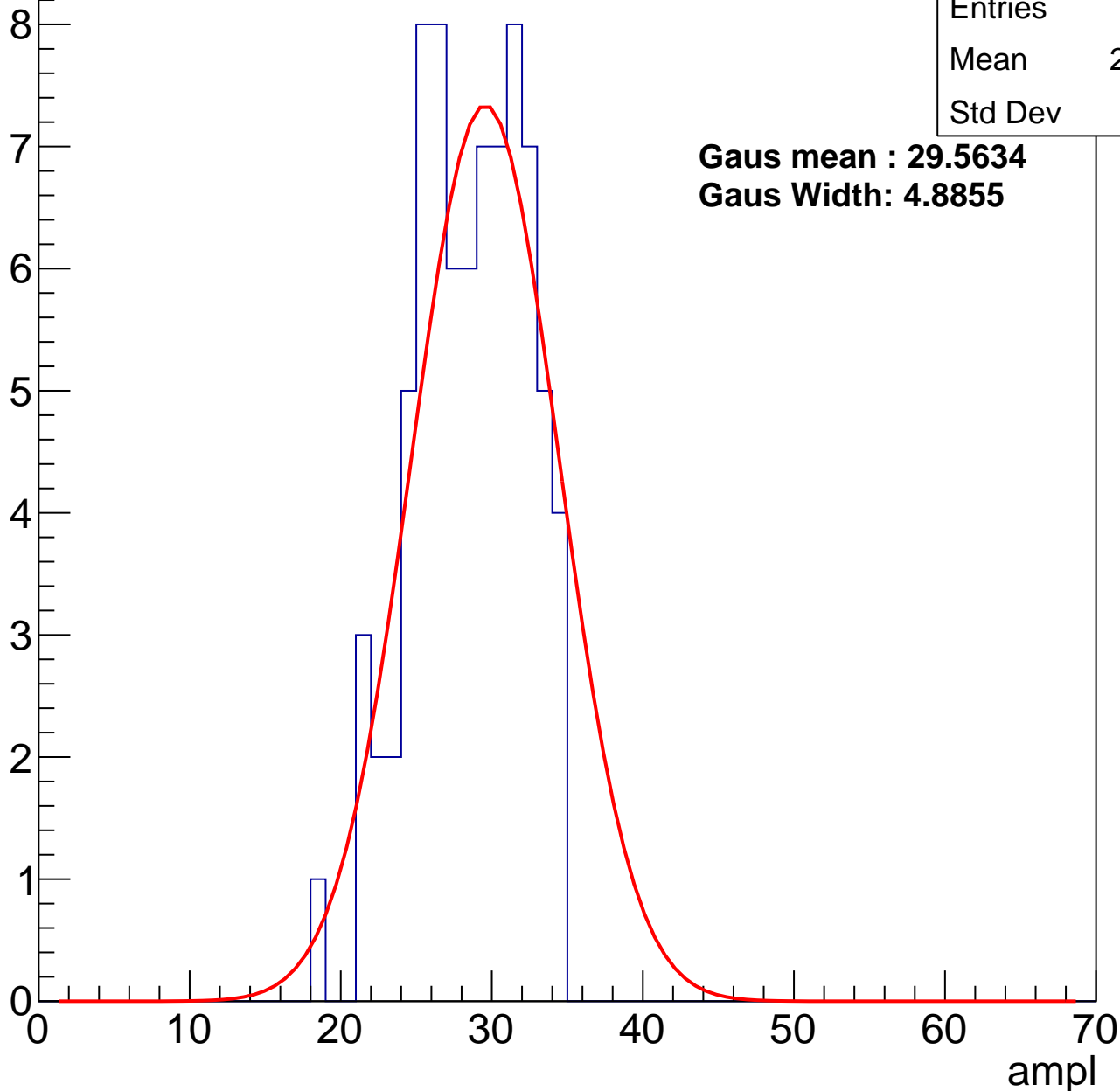
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	79
Mean	28.04
Std Dev	3.64

**Gaus mean : 29.5634**

**Gaus Width: 4.8855**



# B1L103S, U2-ch97, adc1

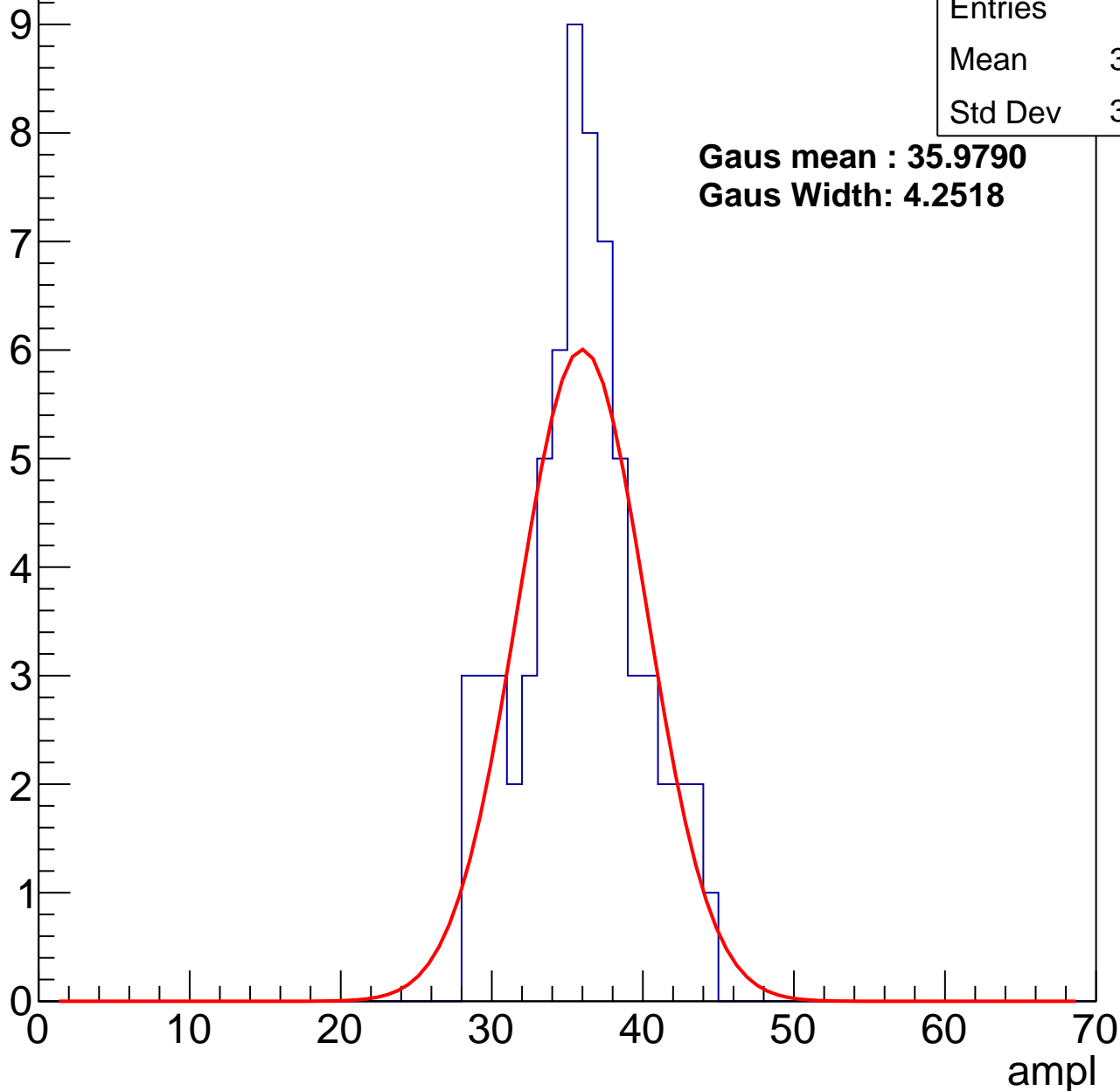
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	35.42
Std Dev	3.837

**Gaus mean : 35.9790**

**Gaus Width: 4.2518**



# B1L103S, U2-ch97, adc2

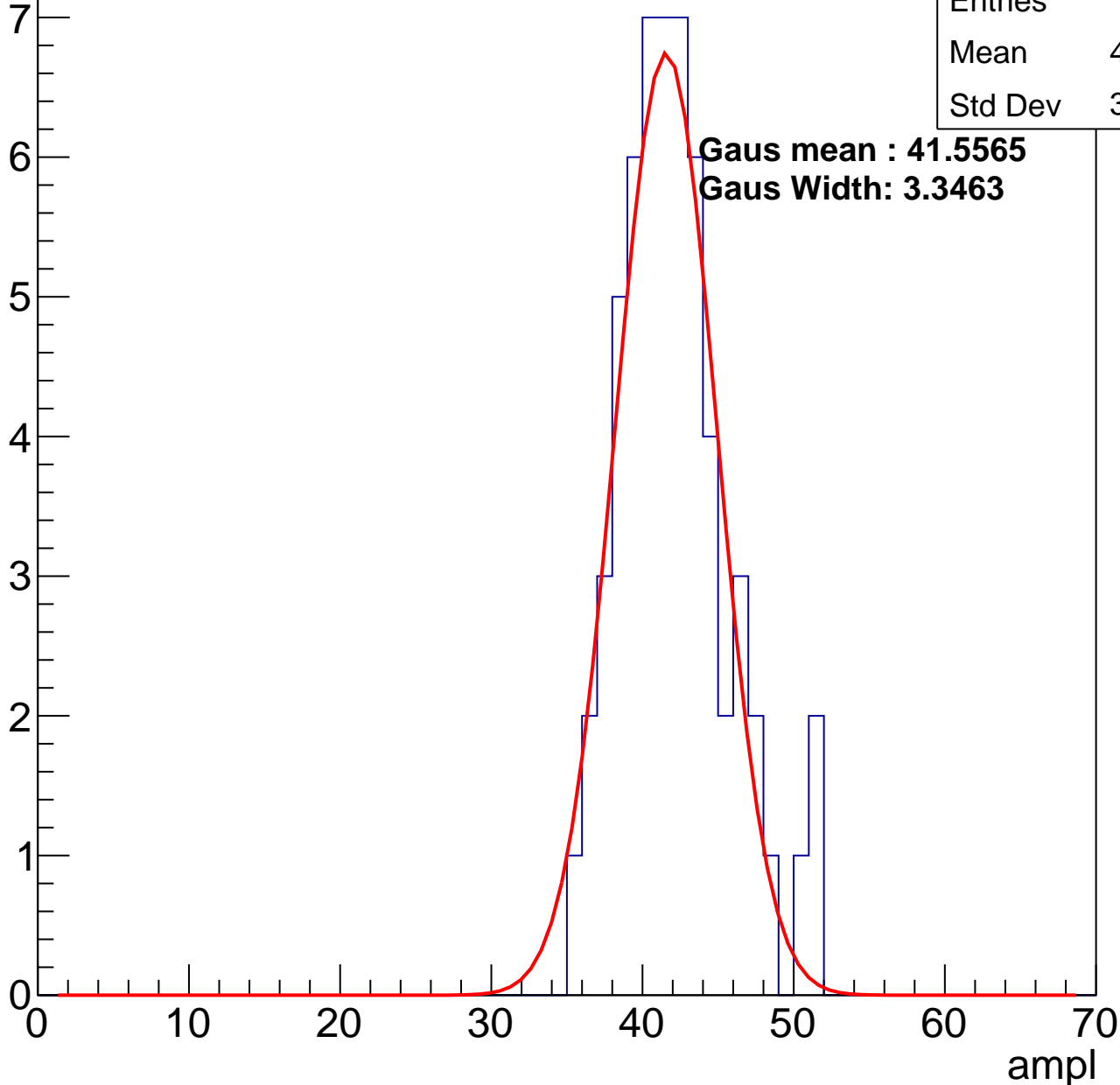
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	41.68
Std Dev	3.586

**Gaus mean : 41.5565**

**Gaus Width: 3.3463**

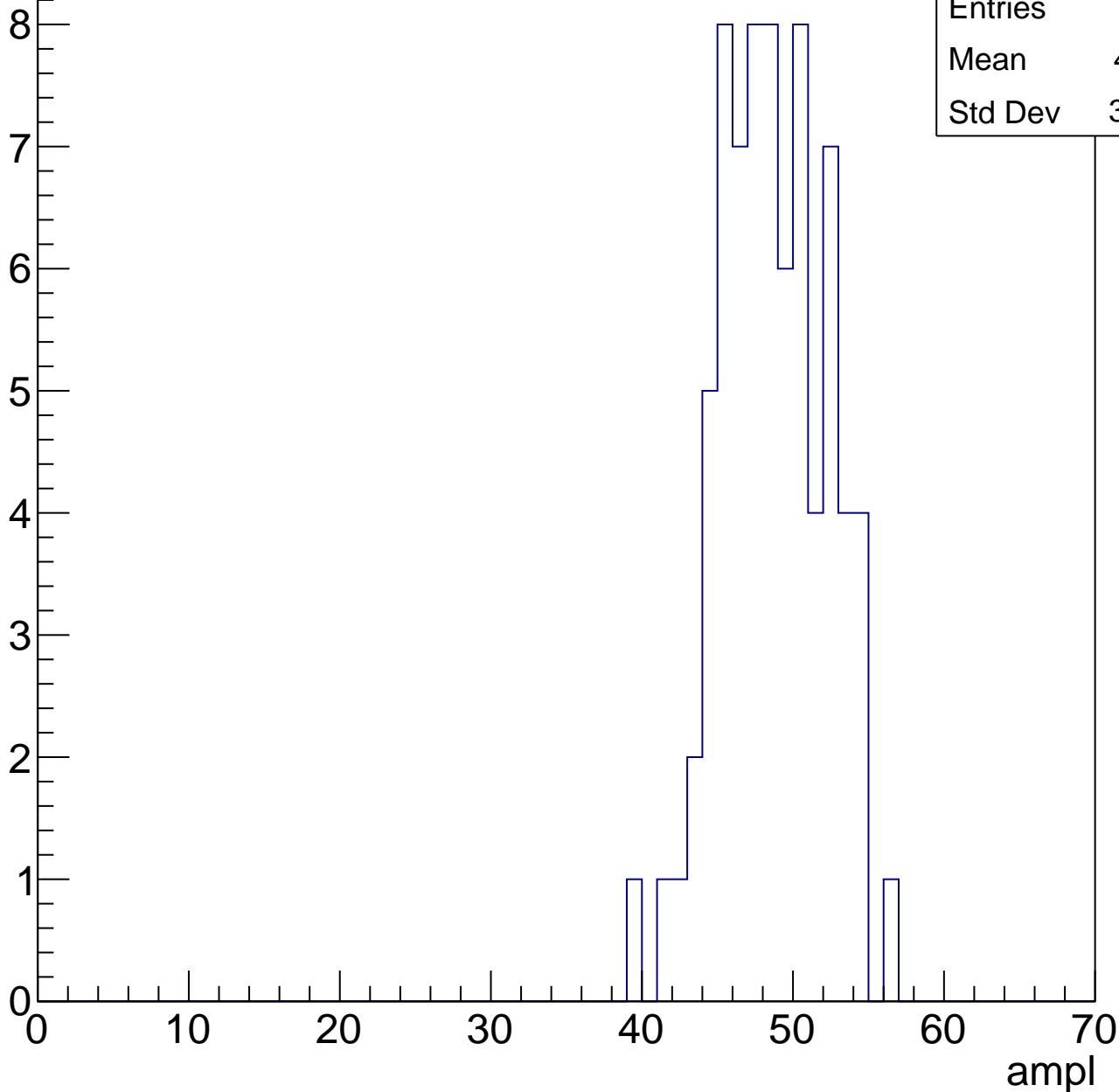


# B1L103S, U2-ch97, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	48.21
Std Dev	3.454

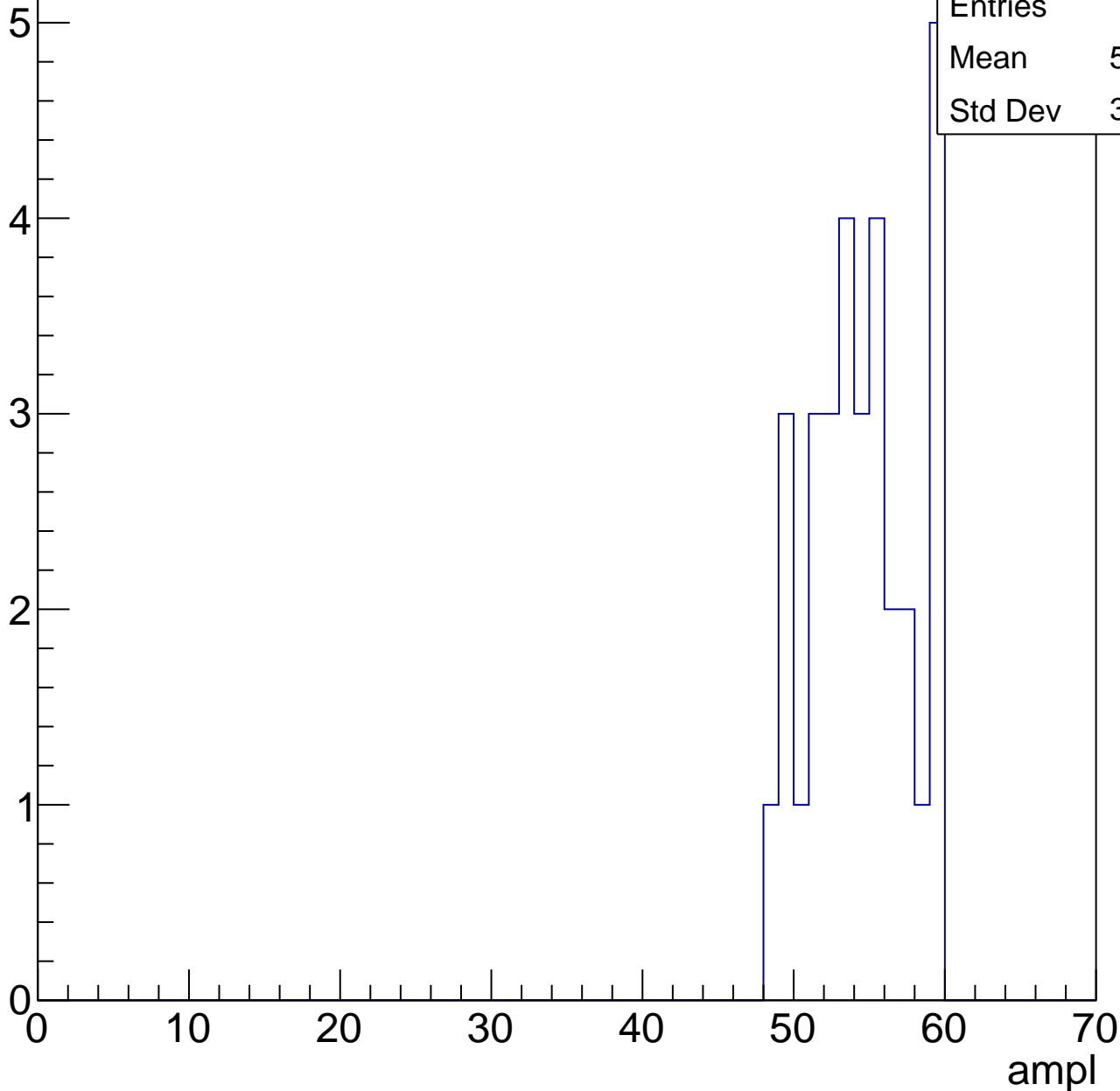


# B1L103S, U2-ch97, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	32
Mean	53.97
Std Dev	3.264



# B1L103S, U2-ch97, adc5

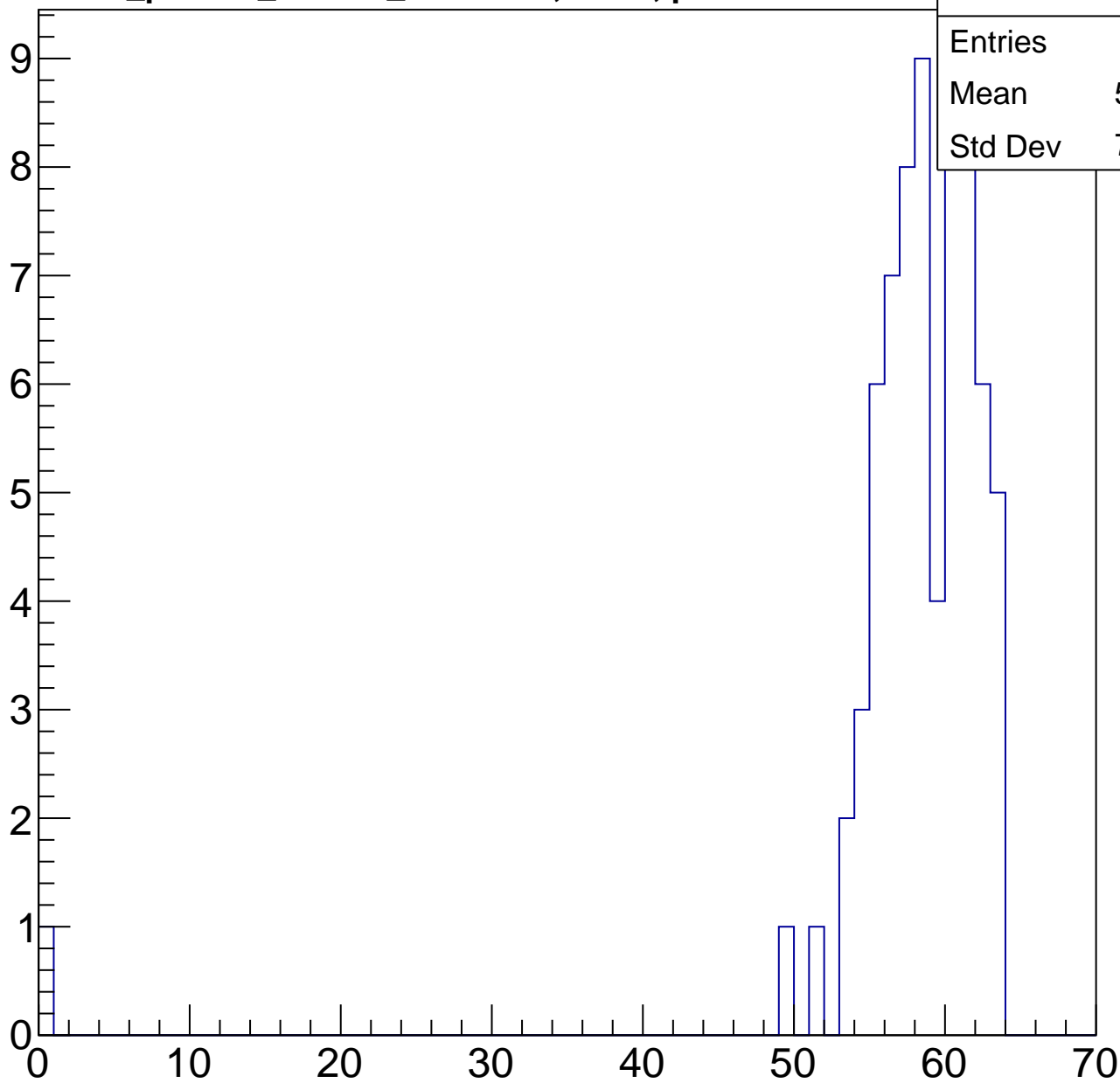
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	70
Mean	57.41
Std Dev	7.551

ampl

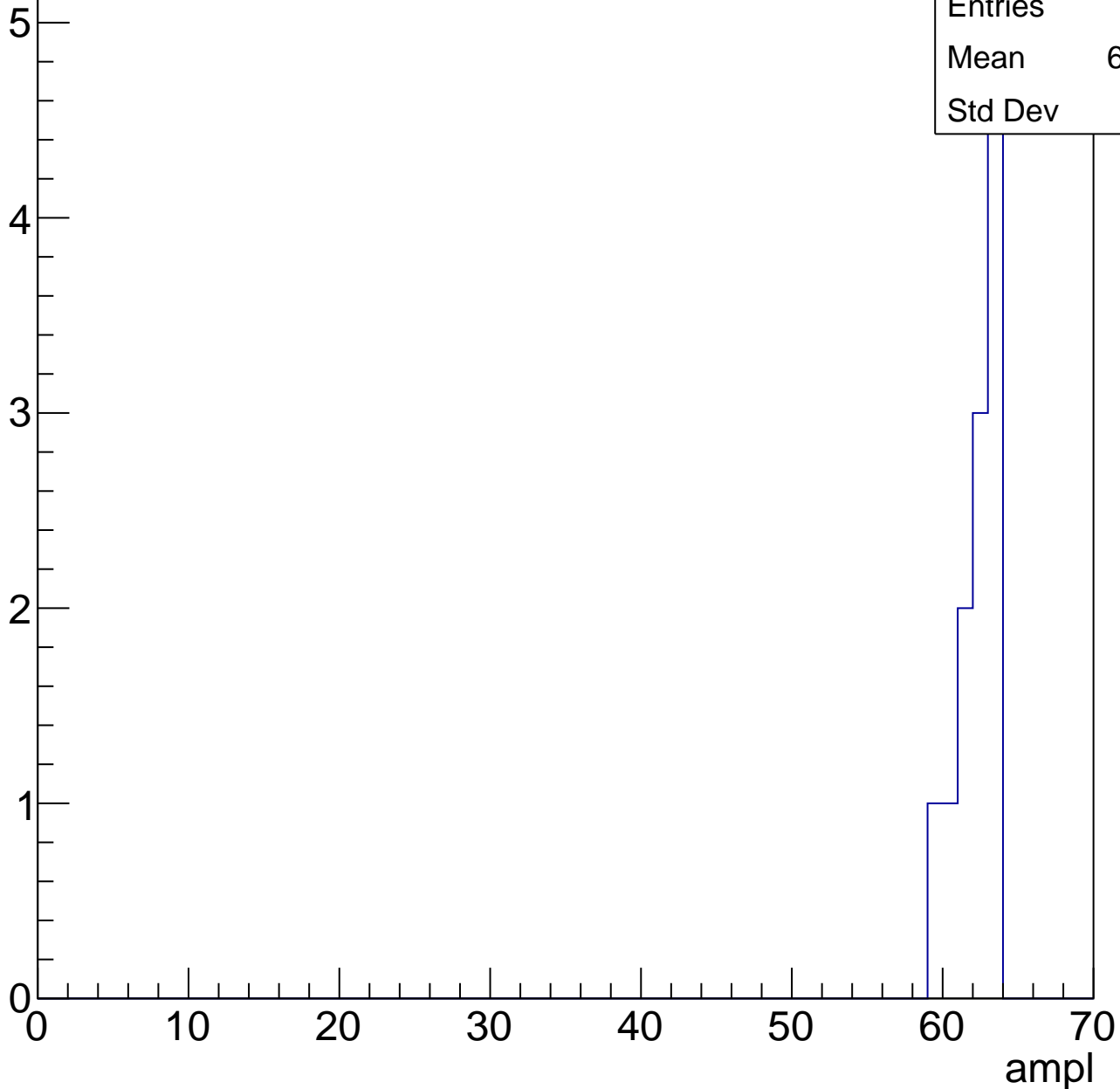


# B1L103S, U2-ch97, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	12
Mean	61.83
Std Dev	1.28

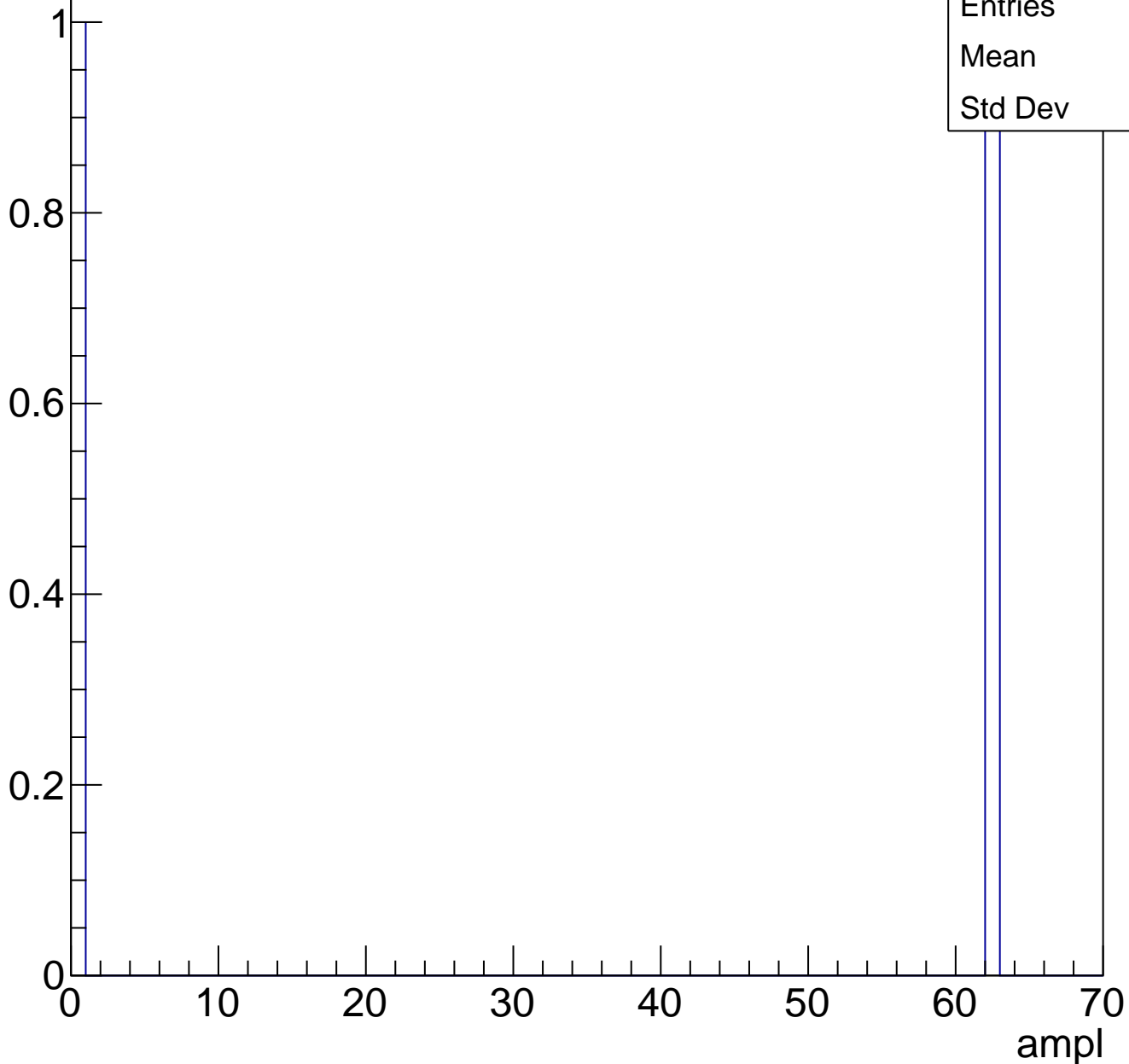




# B1L103S, U2-ch97, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch98, adc0

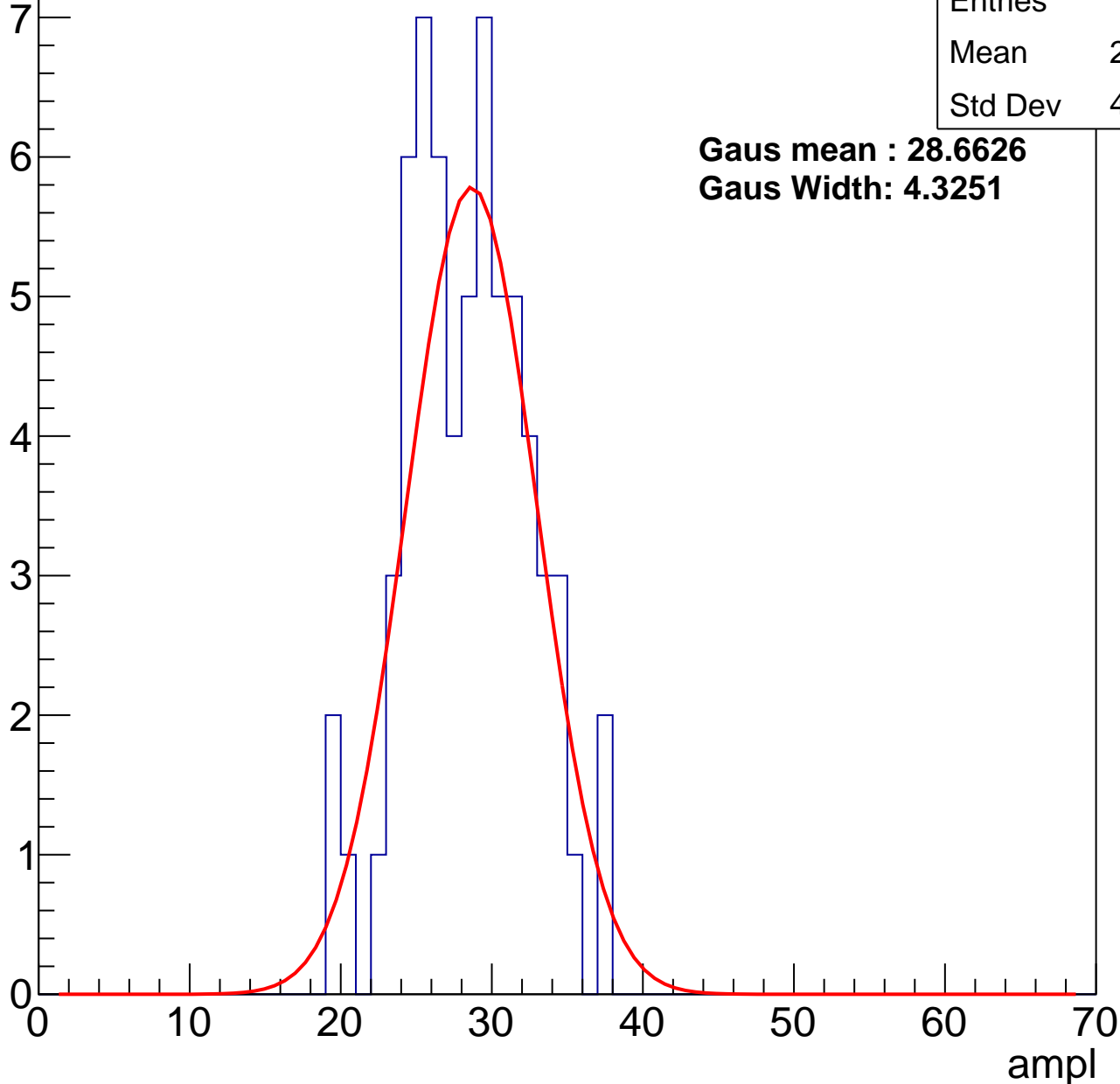
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	27.97
Std Dev	4.027

**Gaus mean : 28.6626**

**Gaus Width: 4.3251**



# B1L103S, U2-ch98, adc1

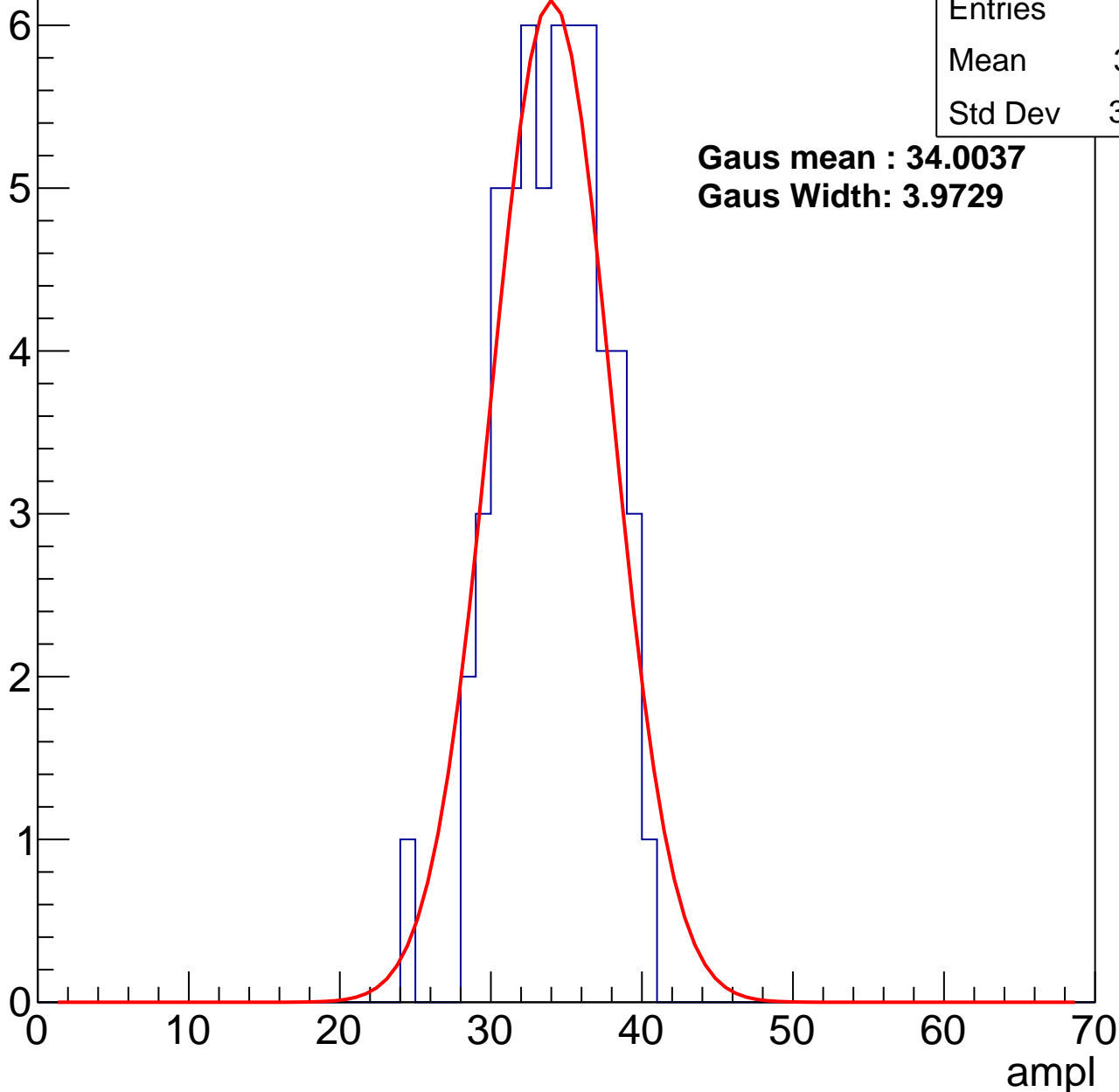
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	33.61
Std Dev	3.334

**Gaus mean : 34.0037**

**Gaus Width: 3.9729**



# B1L103S, U2-ch98, adc2

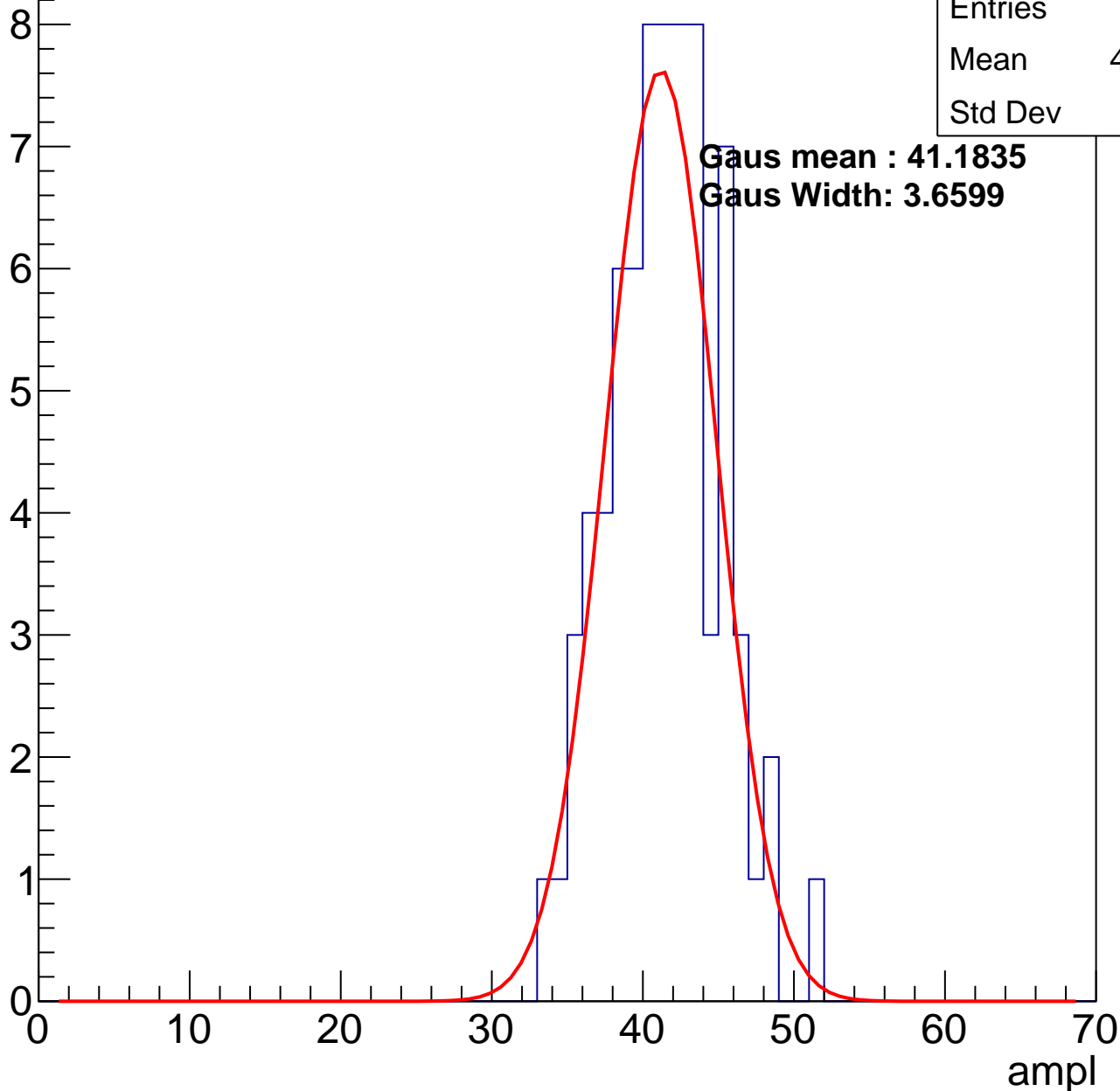
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	40.99
Std Dev	3.6

**Gaus mean : 41.1835**

**Gaus Width: 3.6599**

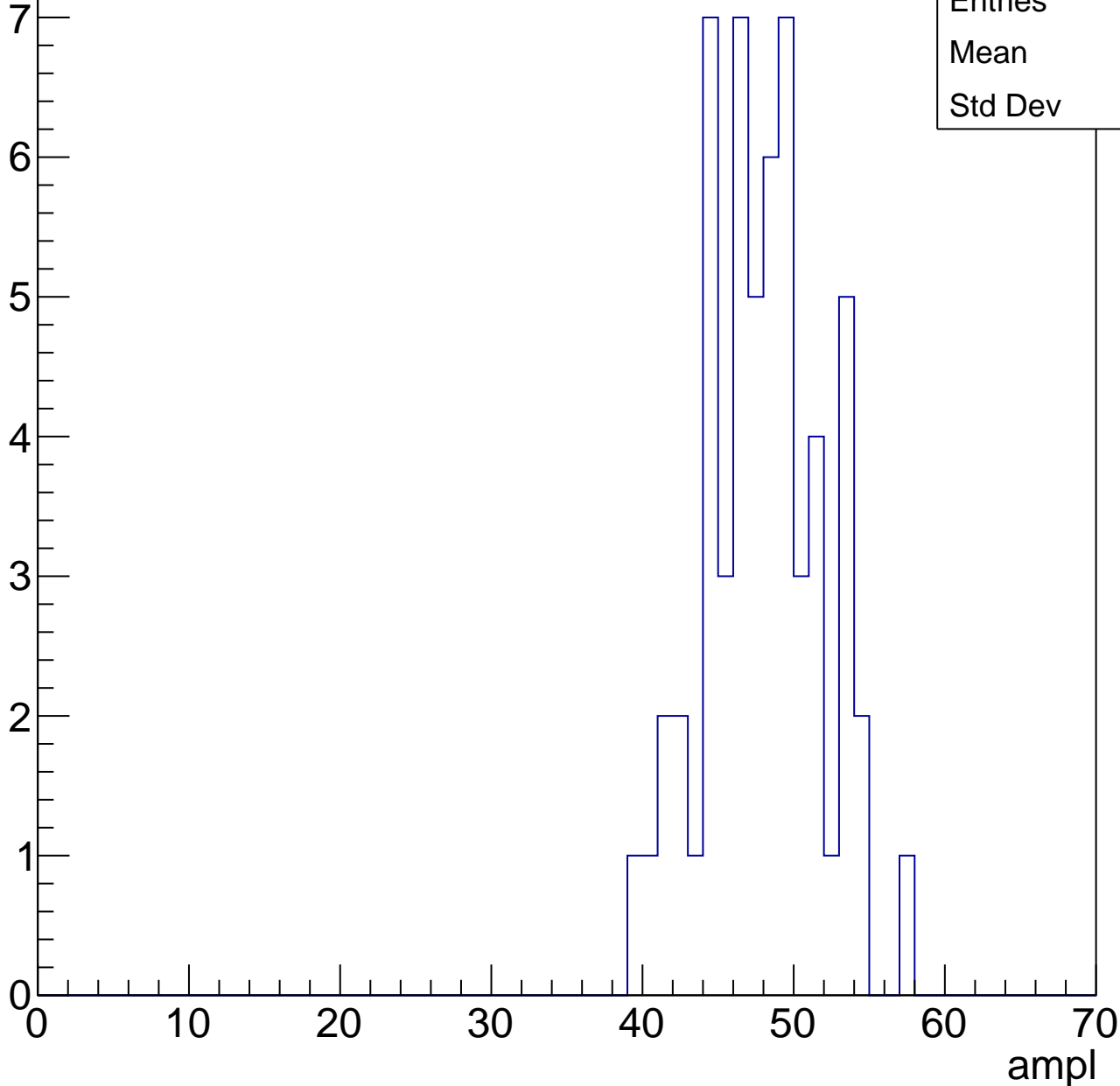


# B1L103S, U2-ch98, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	47.5
Std Dev	3.82

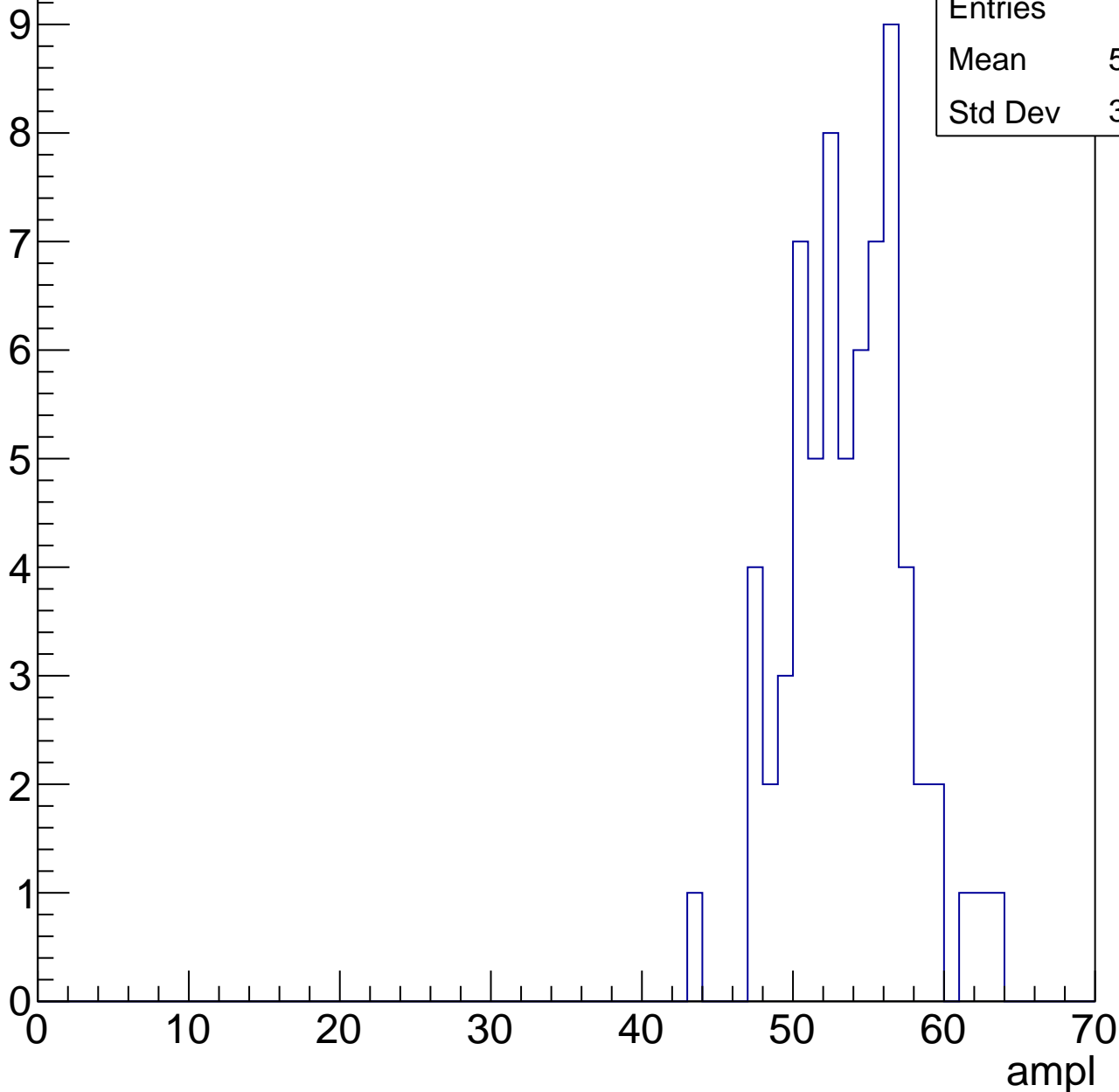


# B1L103S, U2-ch98, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	53.25
Std Dev	3.786



# B1L103S, U2-ch98, adc5

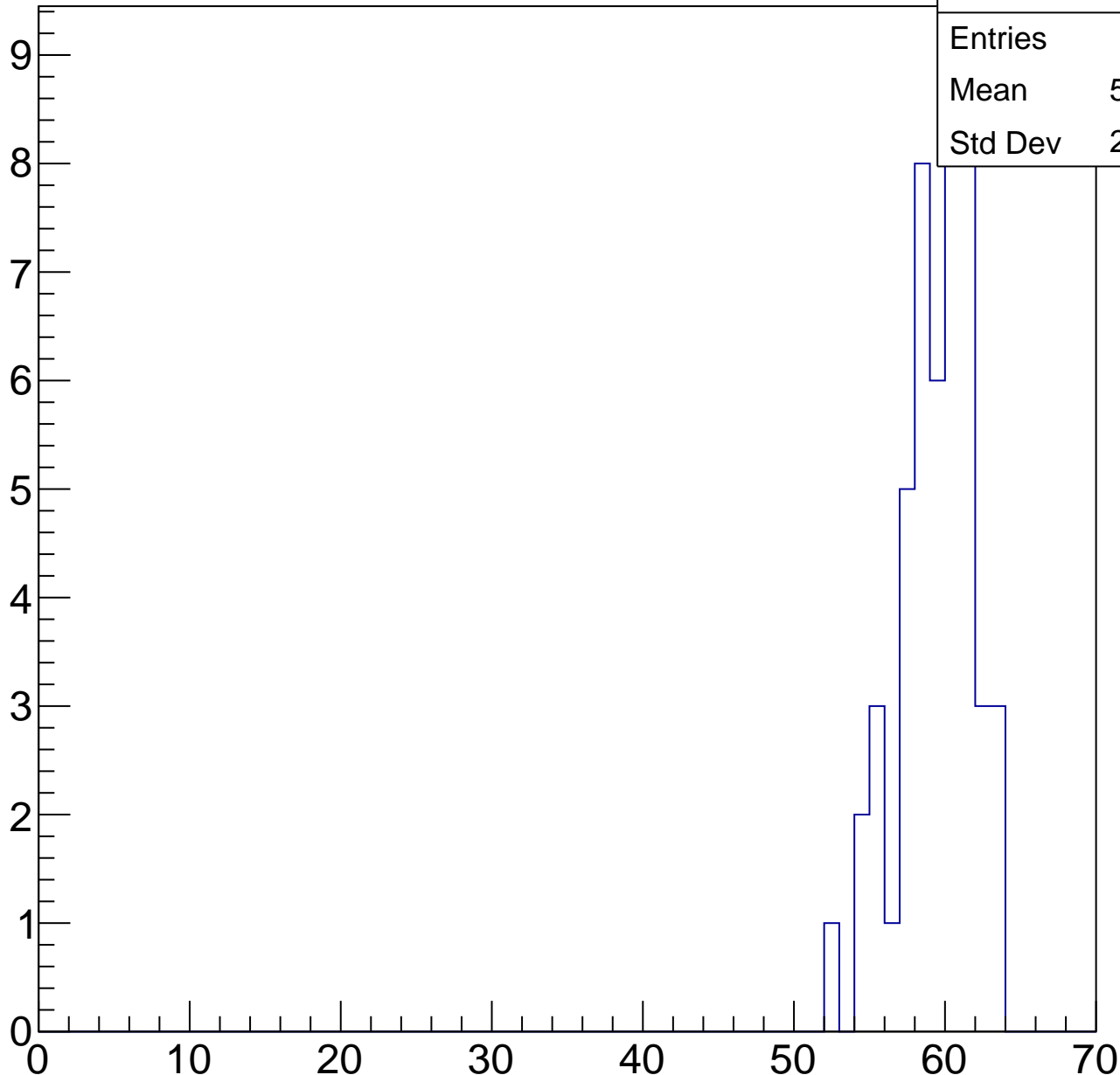
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	49
Mean	58.92
Std Dev	2.473

ampl

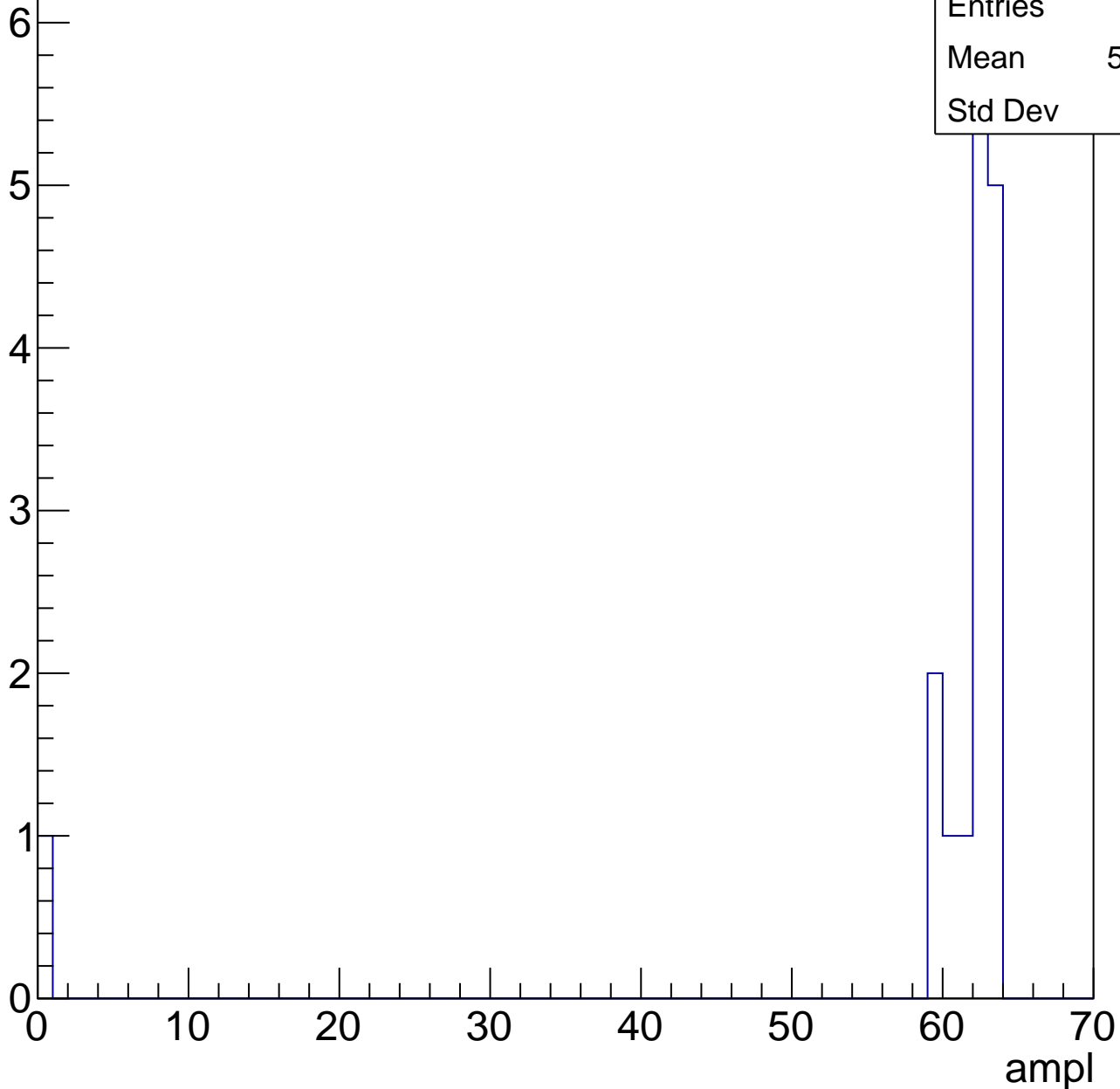


# B1L103S, U2-ch98, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	16
Mean	57.88
Std Dev	15

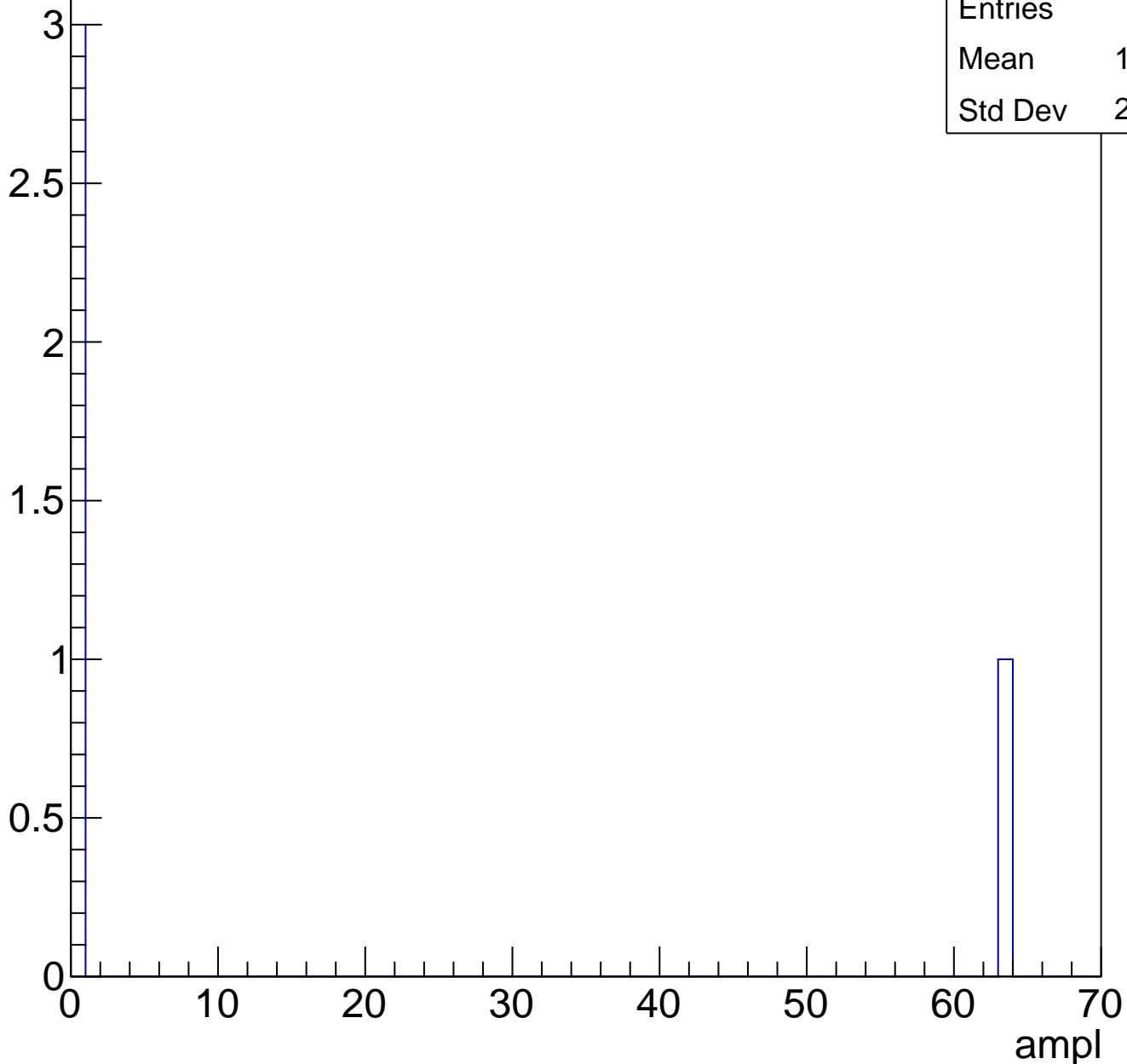




# B1L103S, U2-ch98, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	4
Mean	15.75
Std Dev	27.28

# B1L103S, U2-ch99, adc0

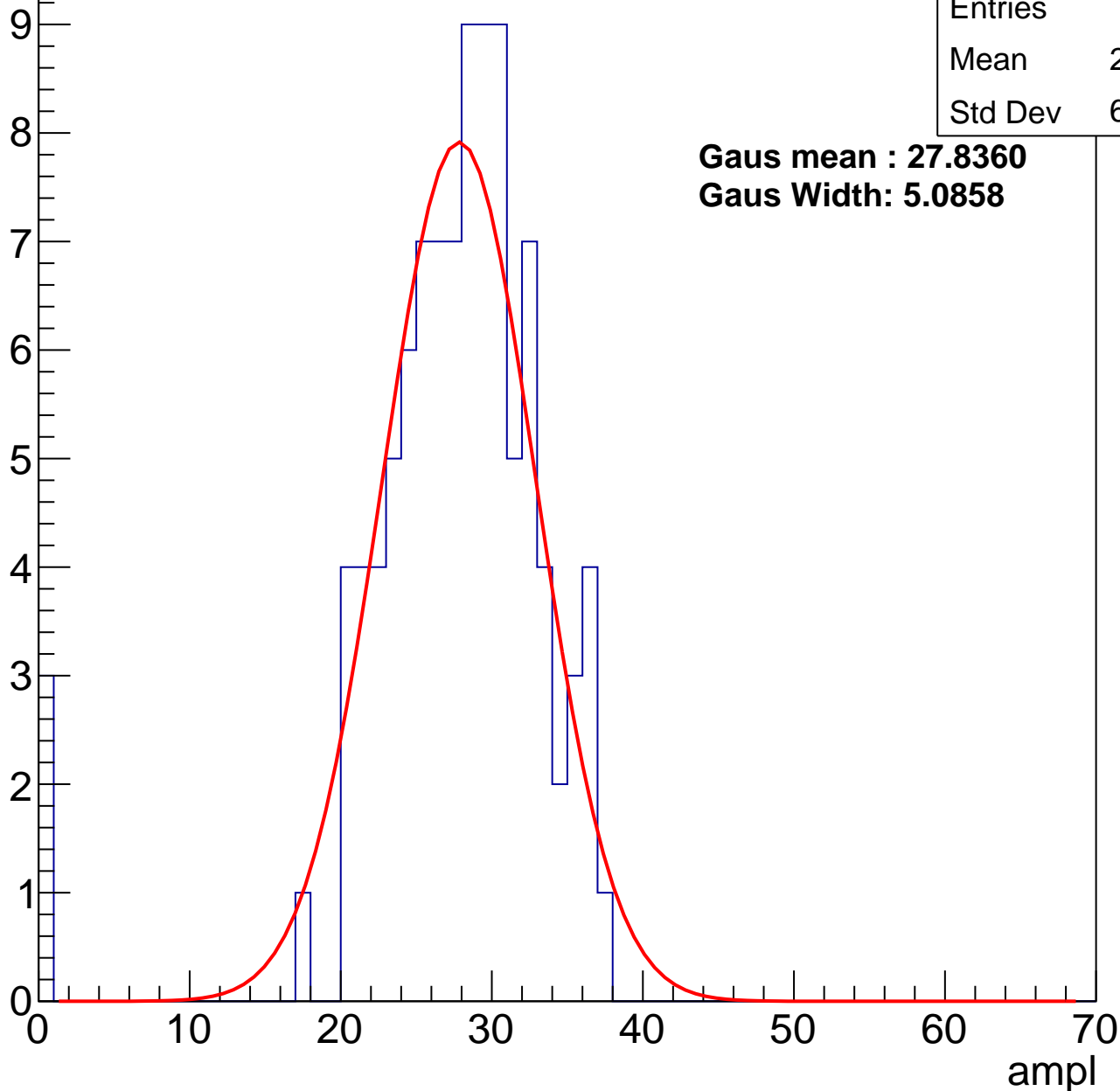
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	101
Mean	26.95
Std Dev	6.398

**Gaus mean : 27.8360**

**Gaus Width: 5.0858**



# B1L103S, U2-ch99, adc1

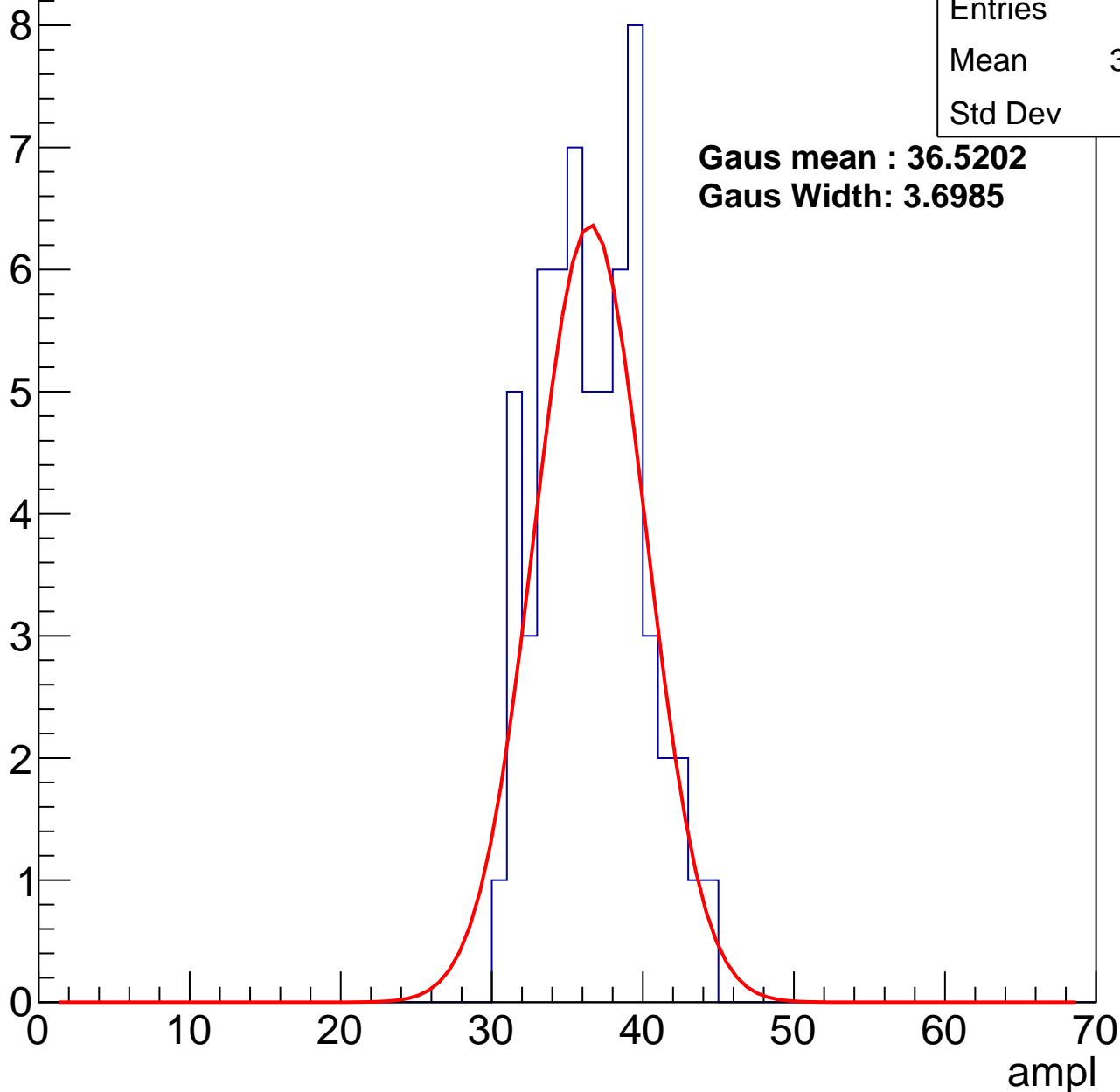
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	36.16
Std Dev	3.33

**Gaus mean : 36.5202**

**Gaus Width: 3.6985**



# B1L103S, U2-ch99, adc2

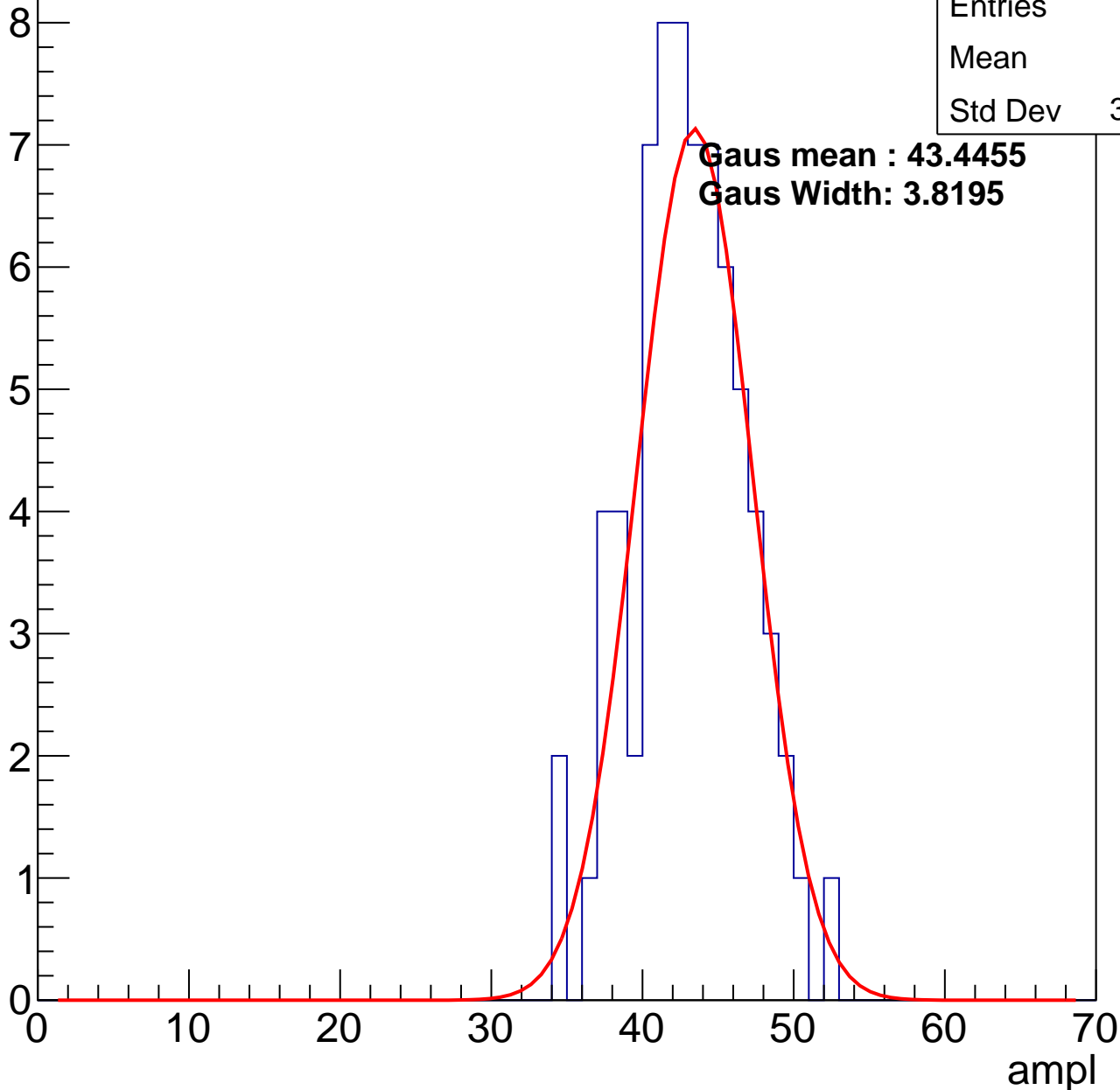
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	42.6
Std Dev	3.718

**Gaus mean : 43.4455**

**Gaus Width: 3.8195**

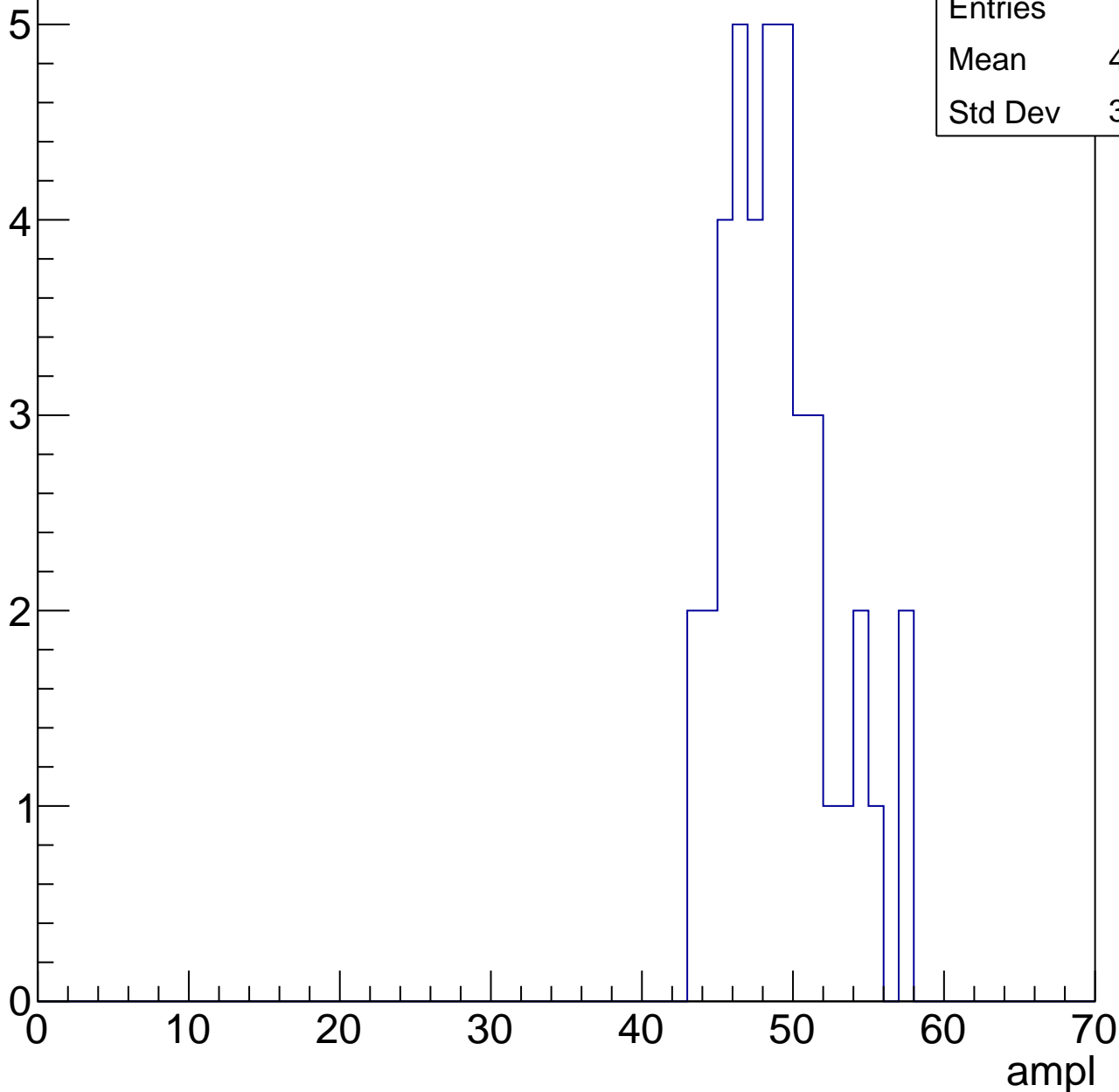


# B1L103S, U2-ch99, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	40
Mean	48.55
Std Dev	3.528

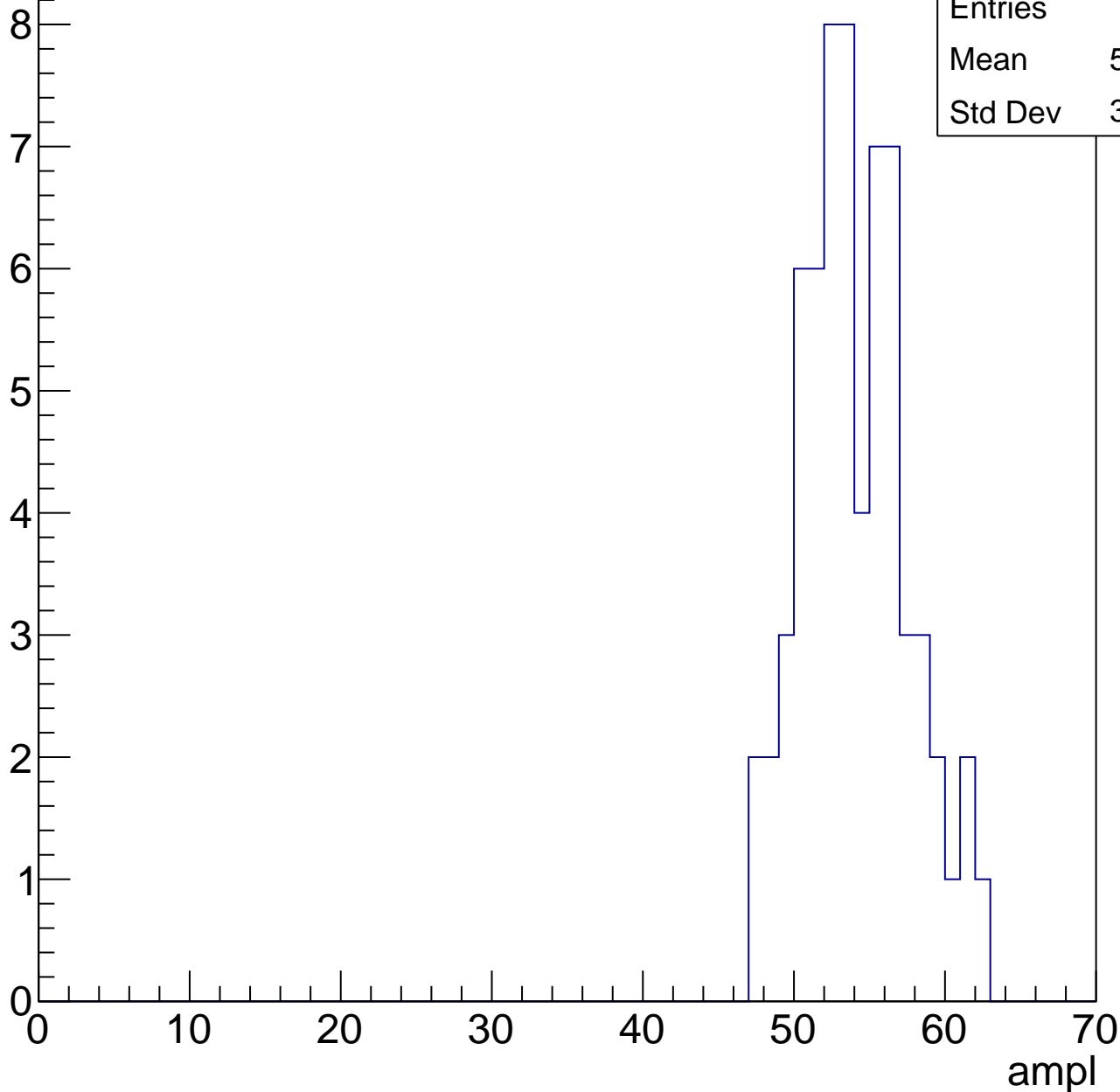


# B1L103S, U2-ch99, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	53.58
Std Dev	3.468

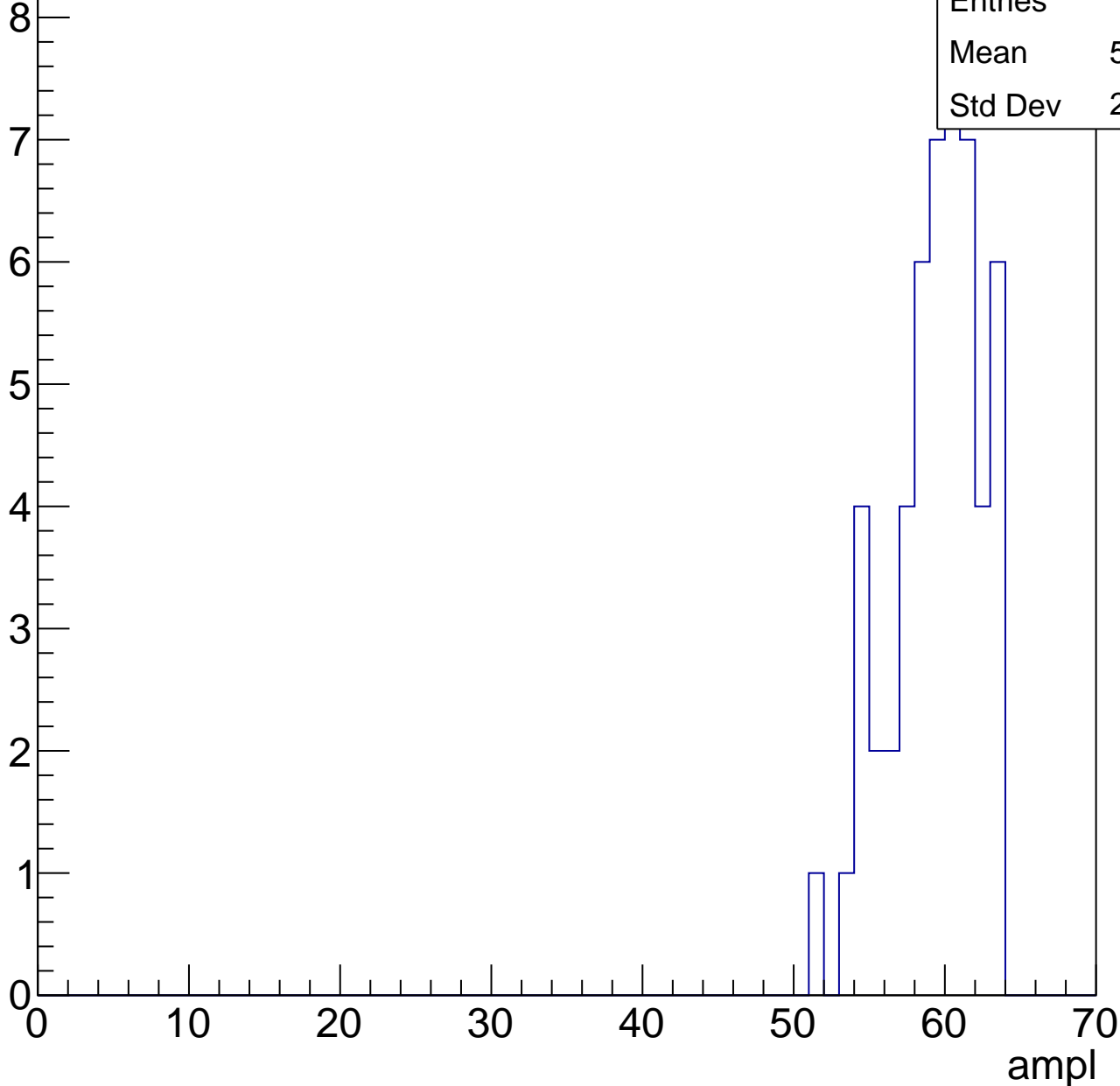


# B1L103S, U2-ch99, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	58.92
Std Dev	2.908







# B1L103S, U2-ch99, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U2-ch100, adc0

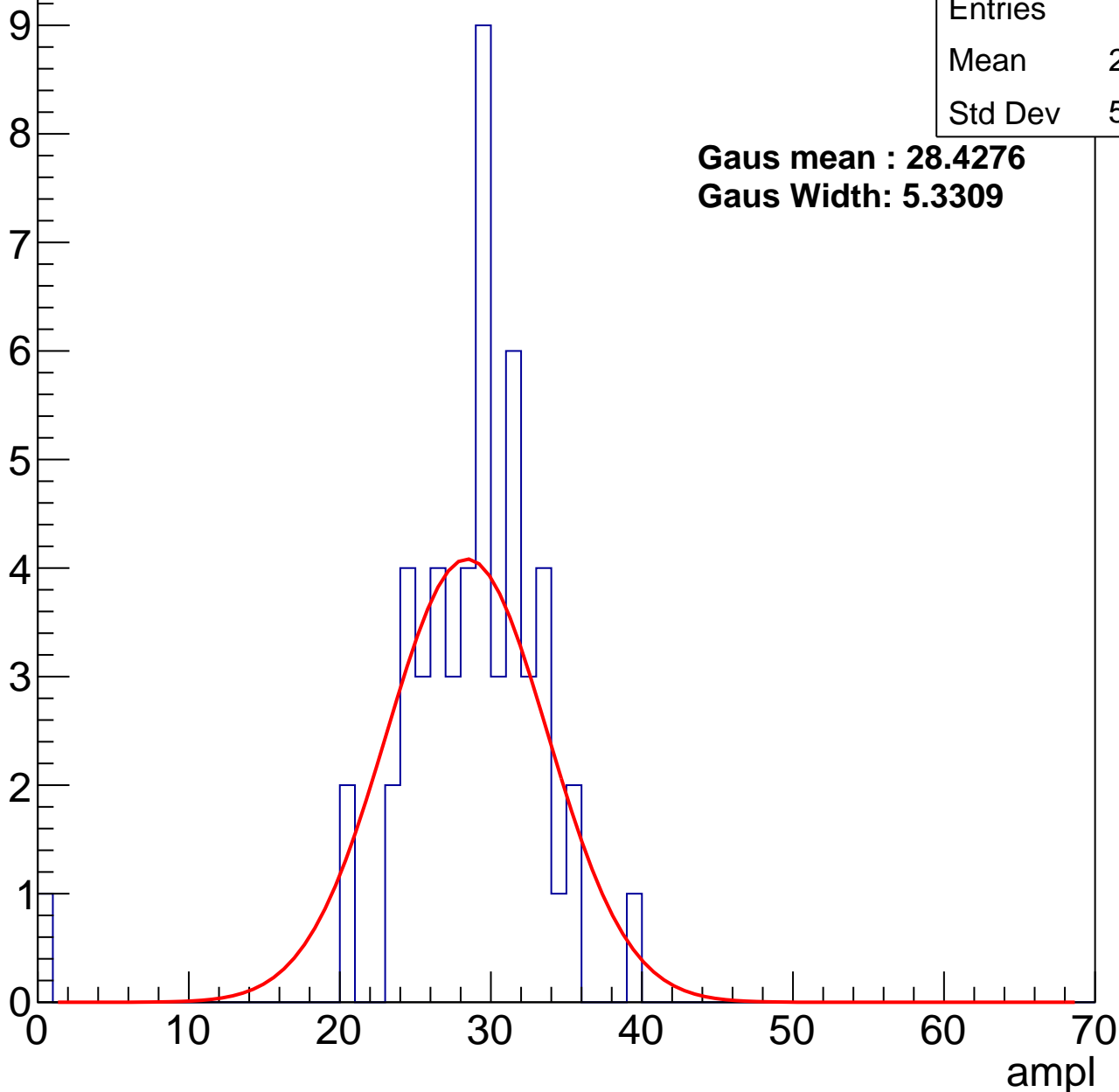
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	28.12
Std Dev	5.458

**Gaus mean : 28.4276**

**Gaus Width: 5.3309**



# B1L103S, U2-ch100, adc1

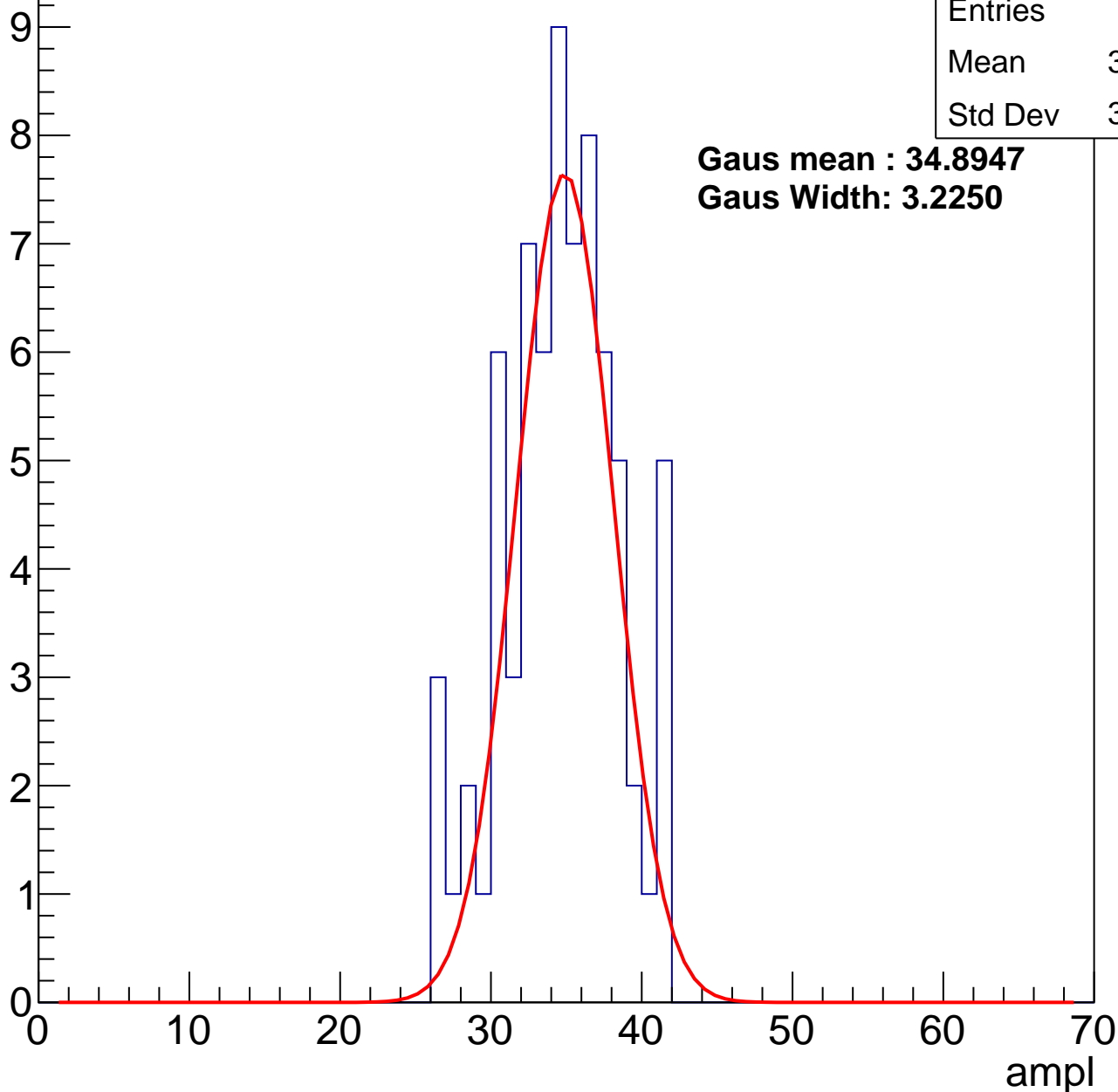
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	34.15
Std Dev	3.722

**Gaus mean : 34.8947**

**Gaus Width: 3.2250**



# B1L103S, U2-ch100, adc2

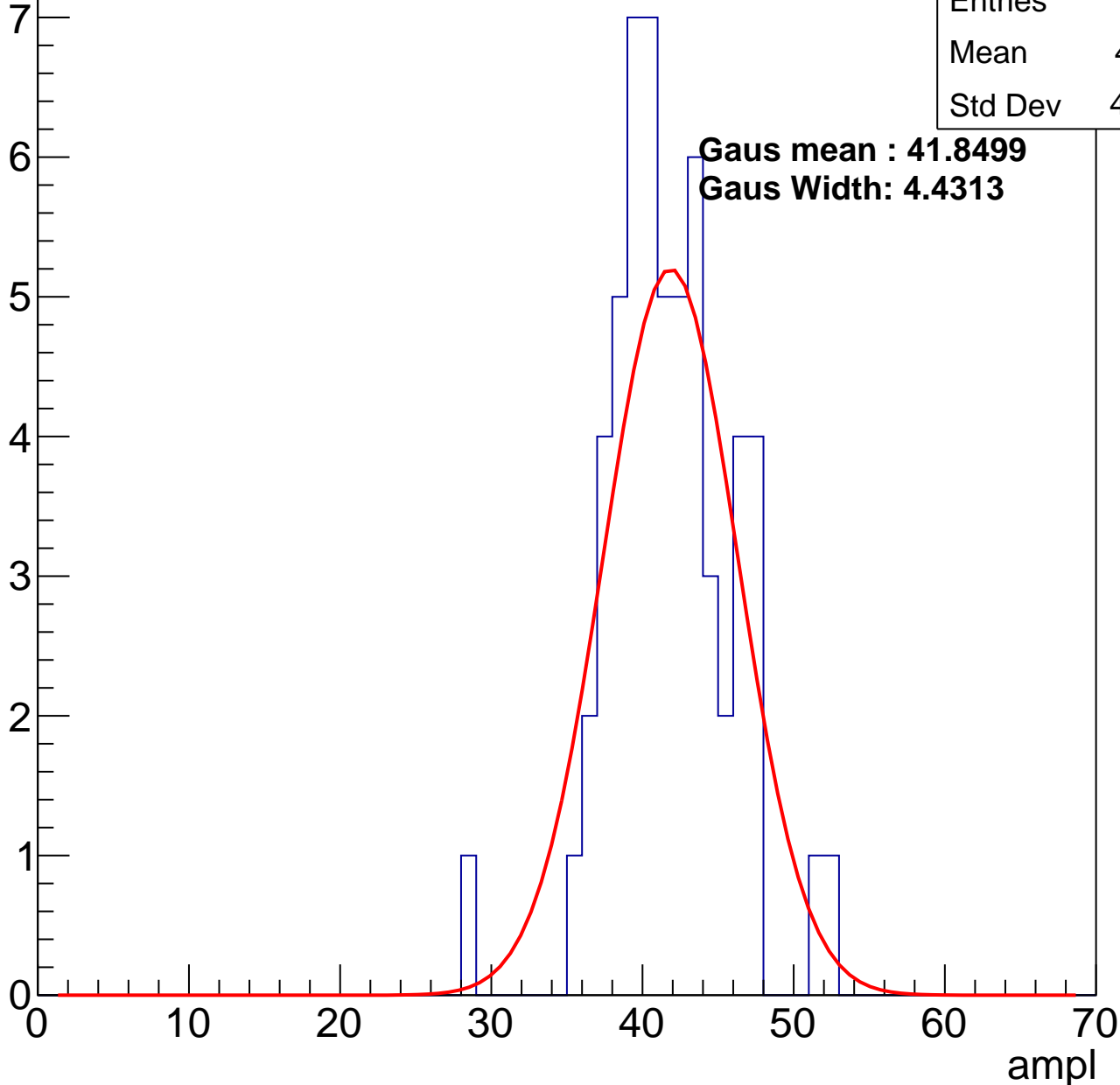
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	41.31
Std Dev	4.039

**Gaus mean : 41.8499**

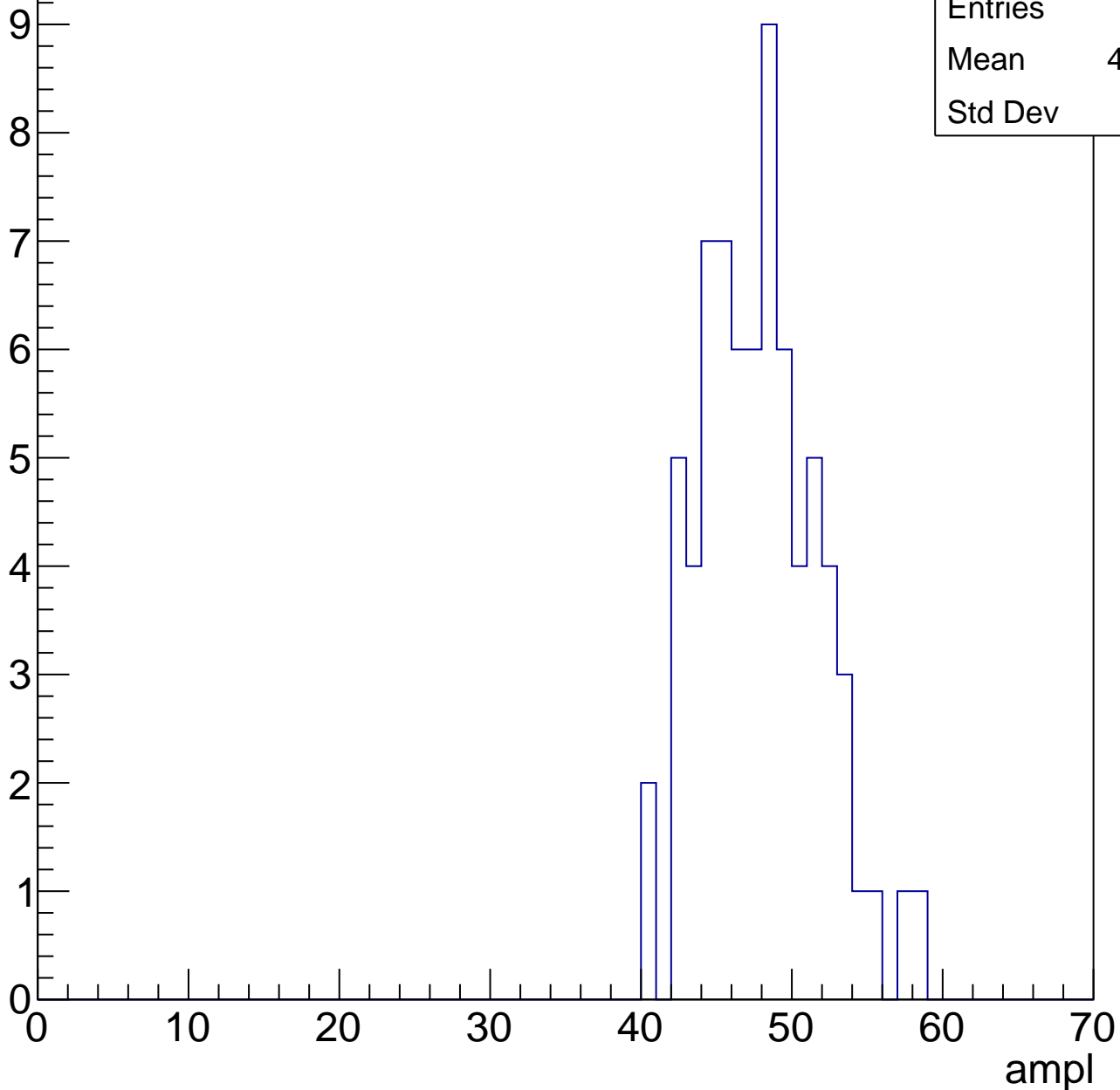
**Gaus Width: 4.4313**



# B1L103S, U2-ch100, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

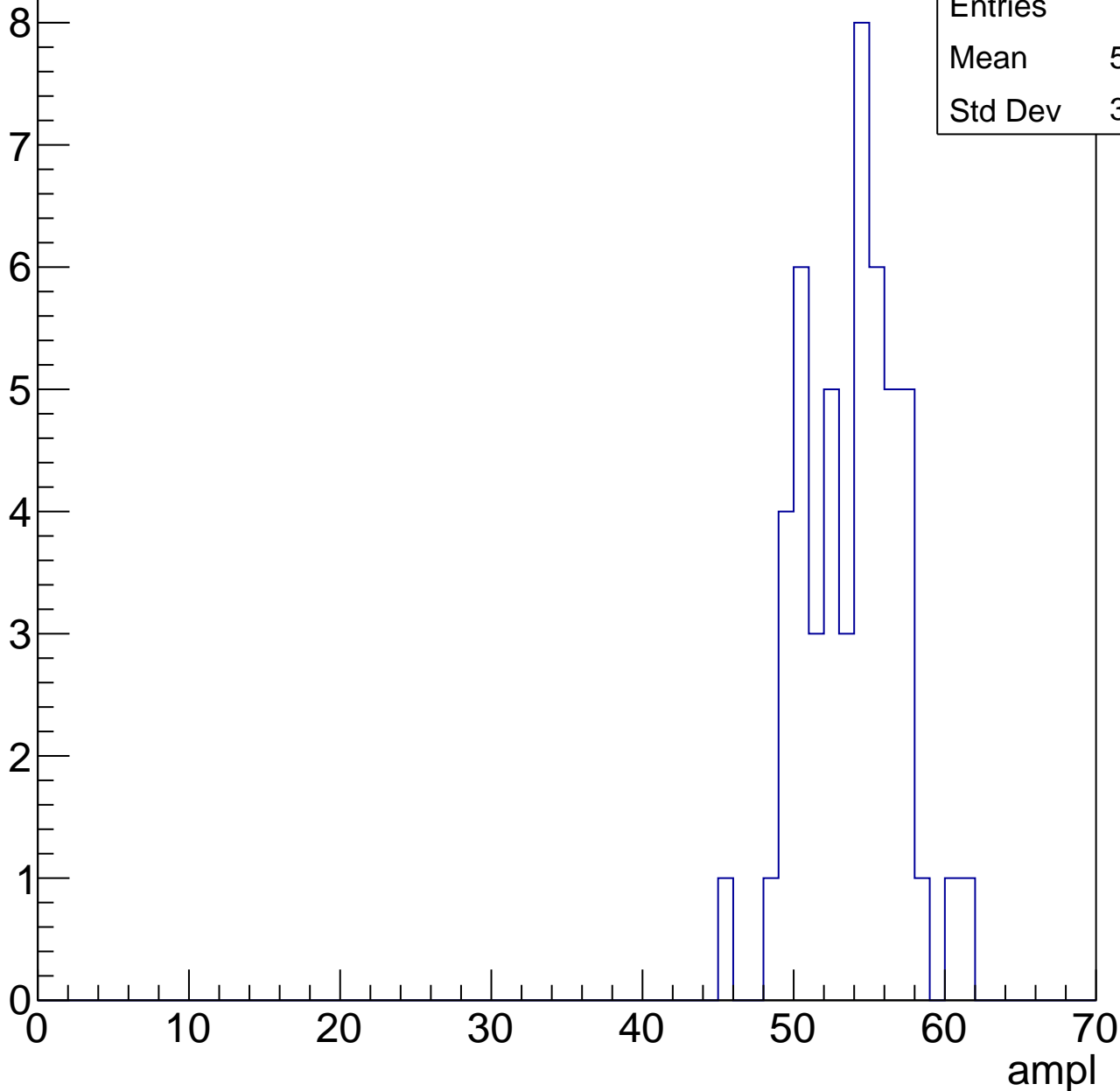


# B1L103S, U2-ch100, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

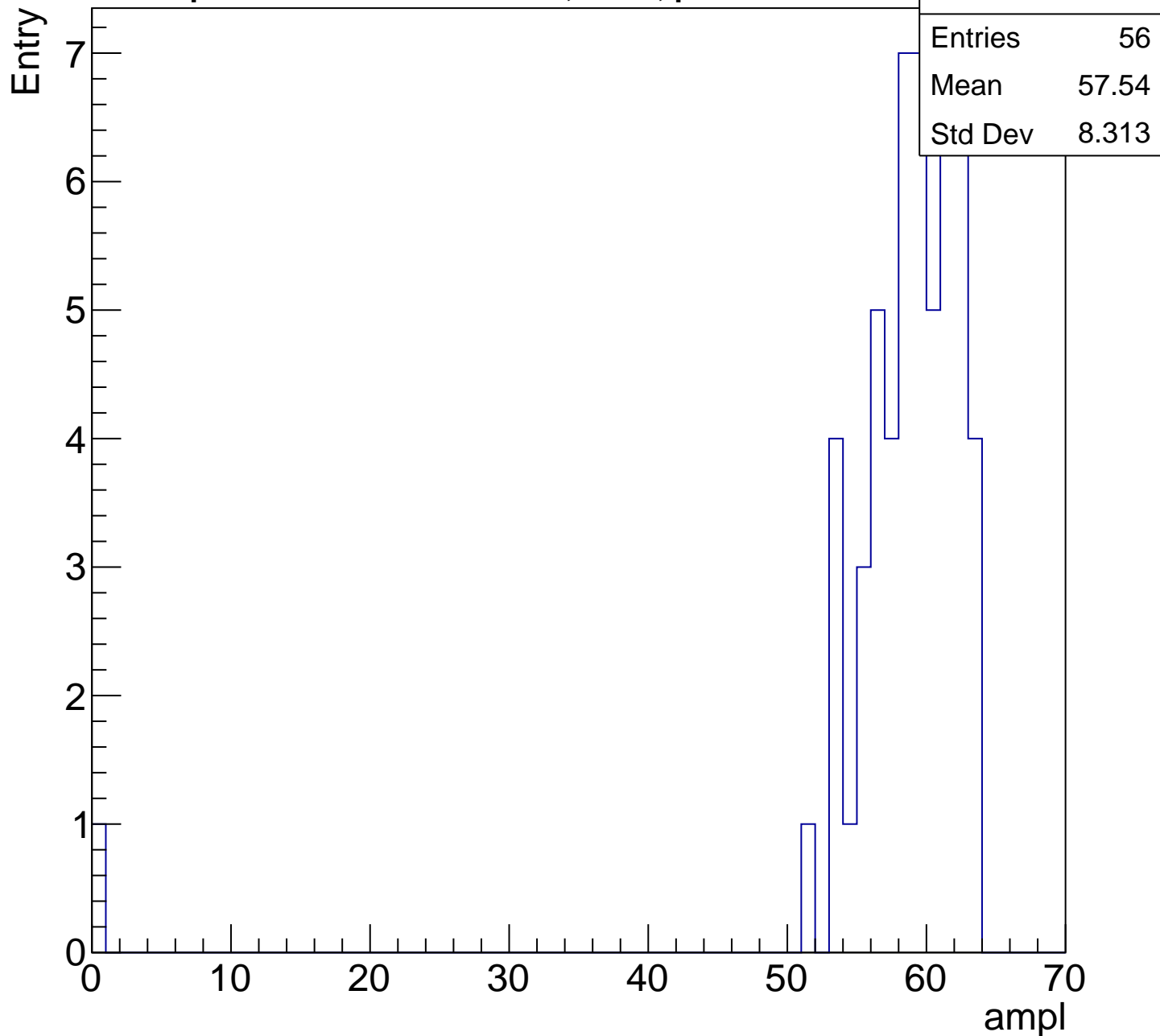
Entry

Entries	50
Mean	53.34
Std Dev	3.204



# B1L103S, U2-ch100, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

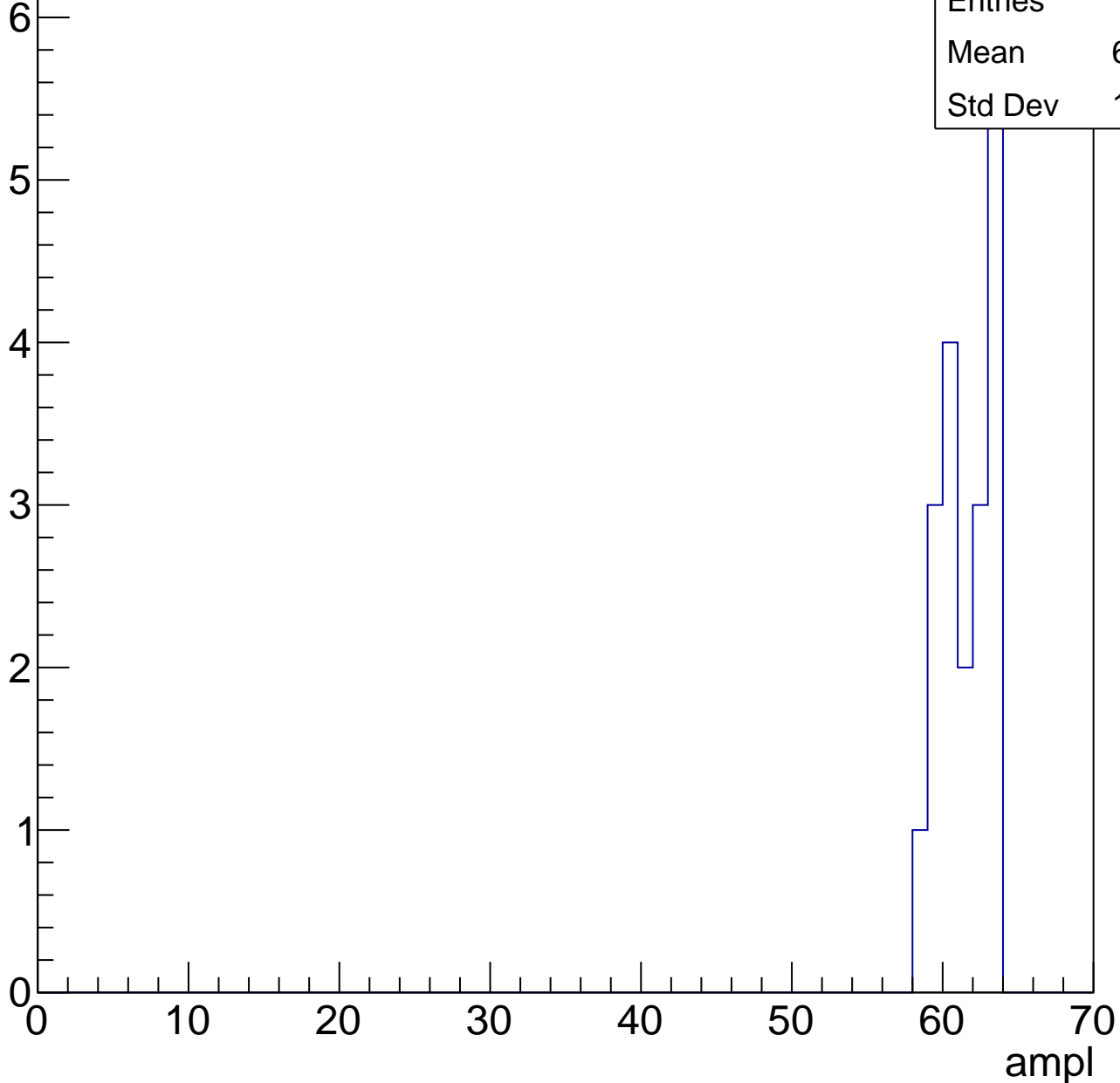


# B1L103S, U2-ch100, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	19
Mean	61.11
Std Dev	1.651





# B1L103S, U2-ch100, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U2-ch101, adc0

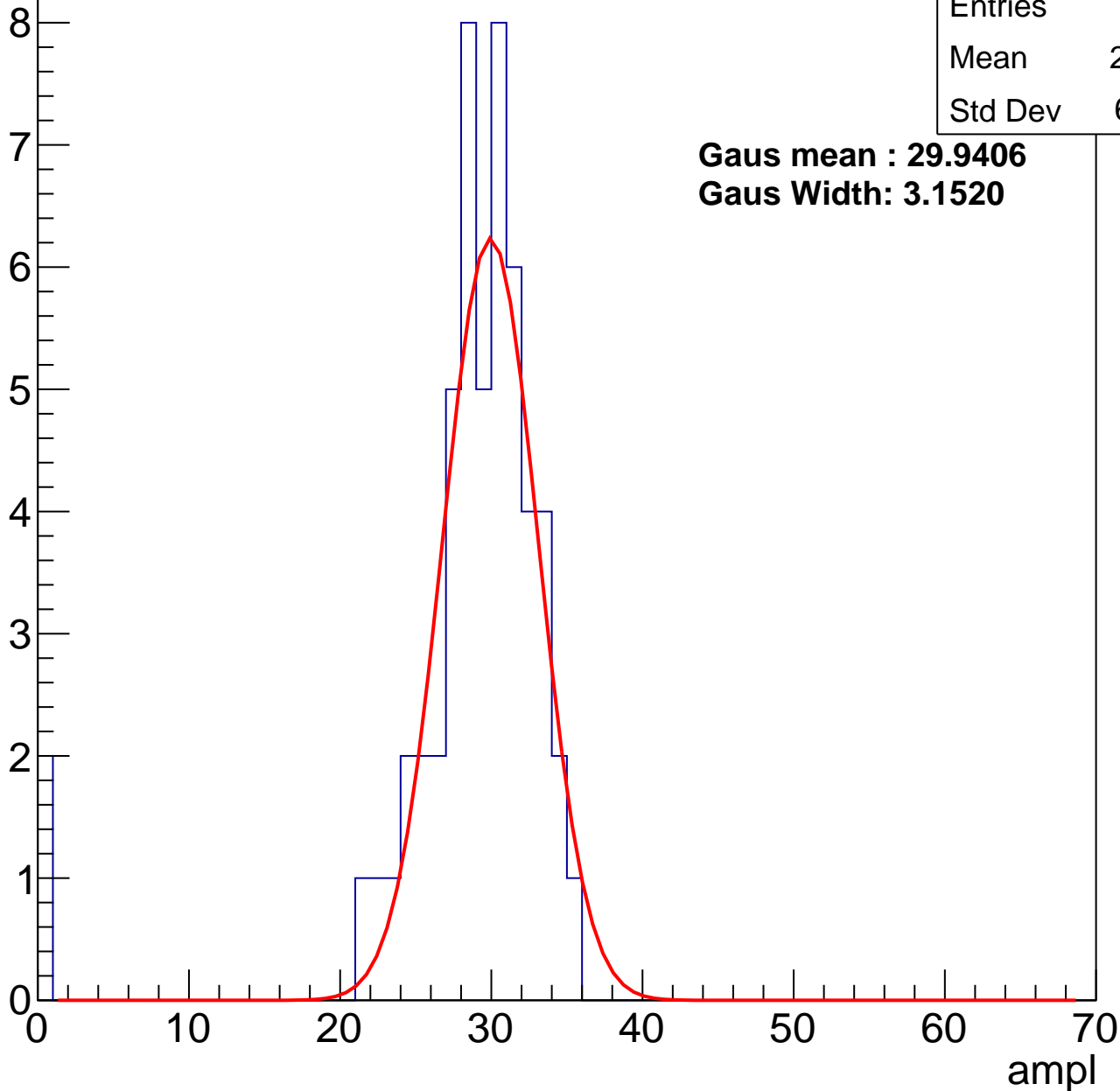
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	27.94
Std Dev	6.261

**Gaus mean : 29.9406**

**Gaus Width: 3.1520**



# B1L103S, U2-ch101, adc1

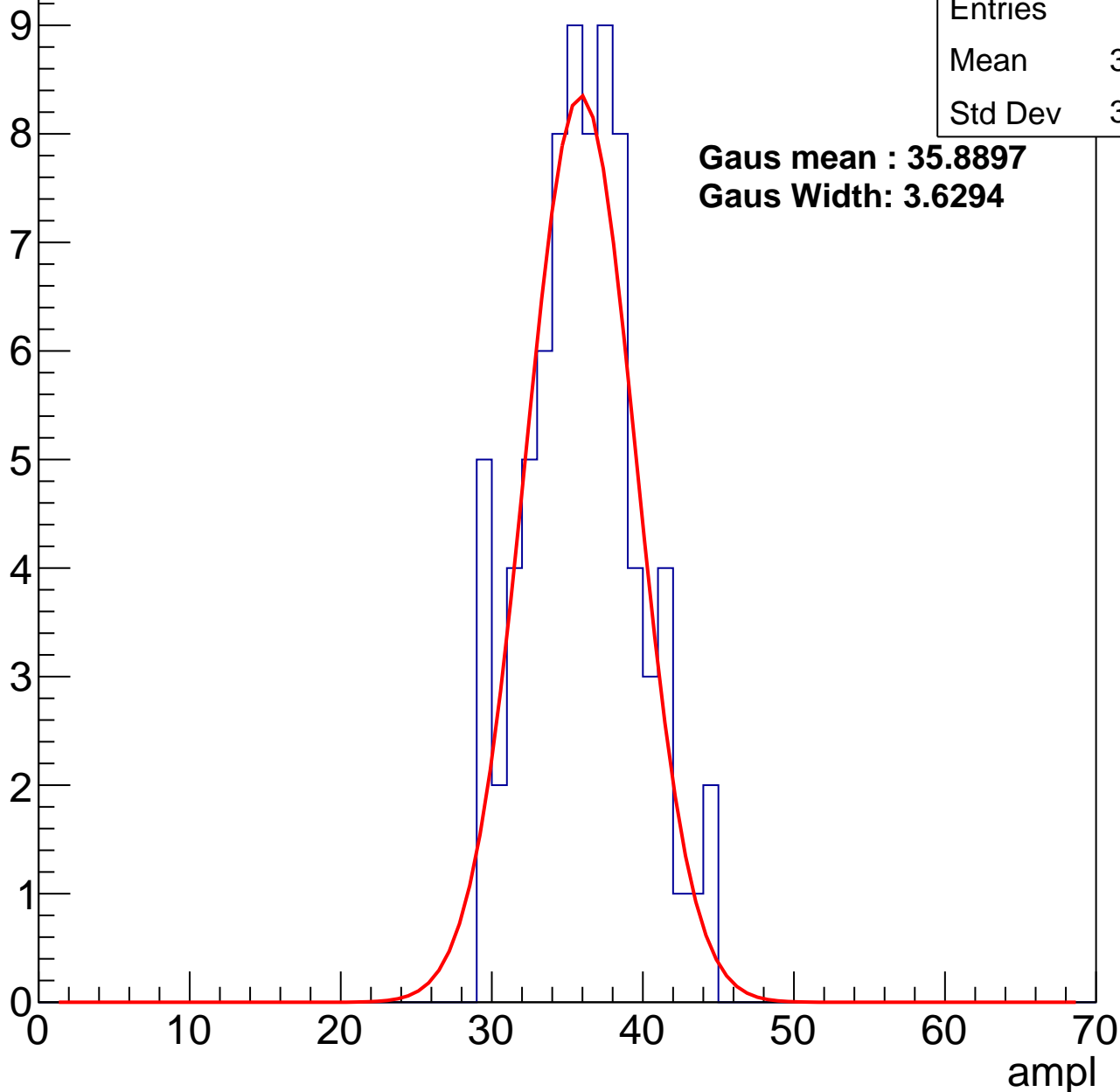
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	79
Mean	35.59
Std Dev	3.588

**Gaus mean : 35.8897**

**Gaus Width: 3.6294**



# B1L103S, U2-ch101, adc2

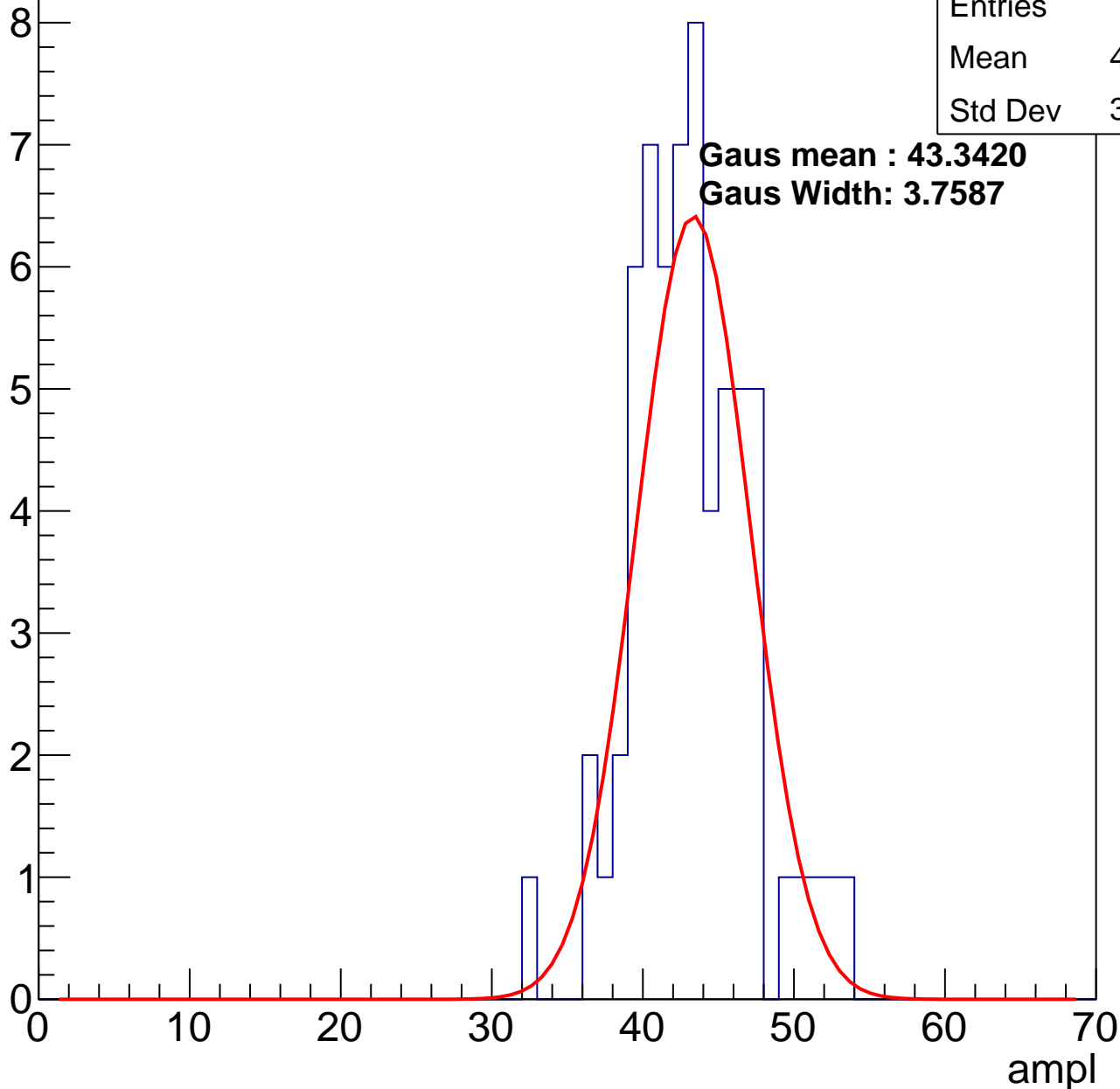
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	42.75
Std Dev	3.893

**Gaus mean : 43.3420**

**Gaus Width: 3.7587**

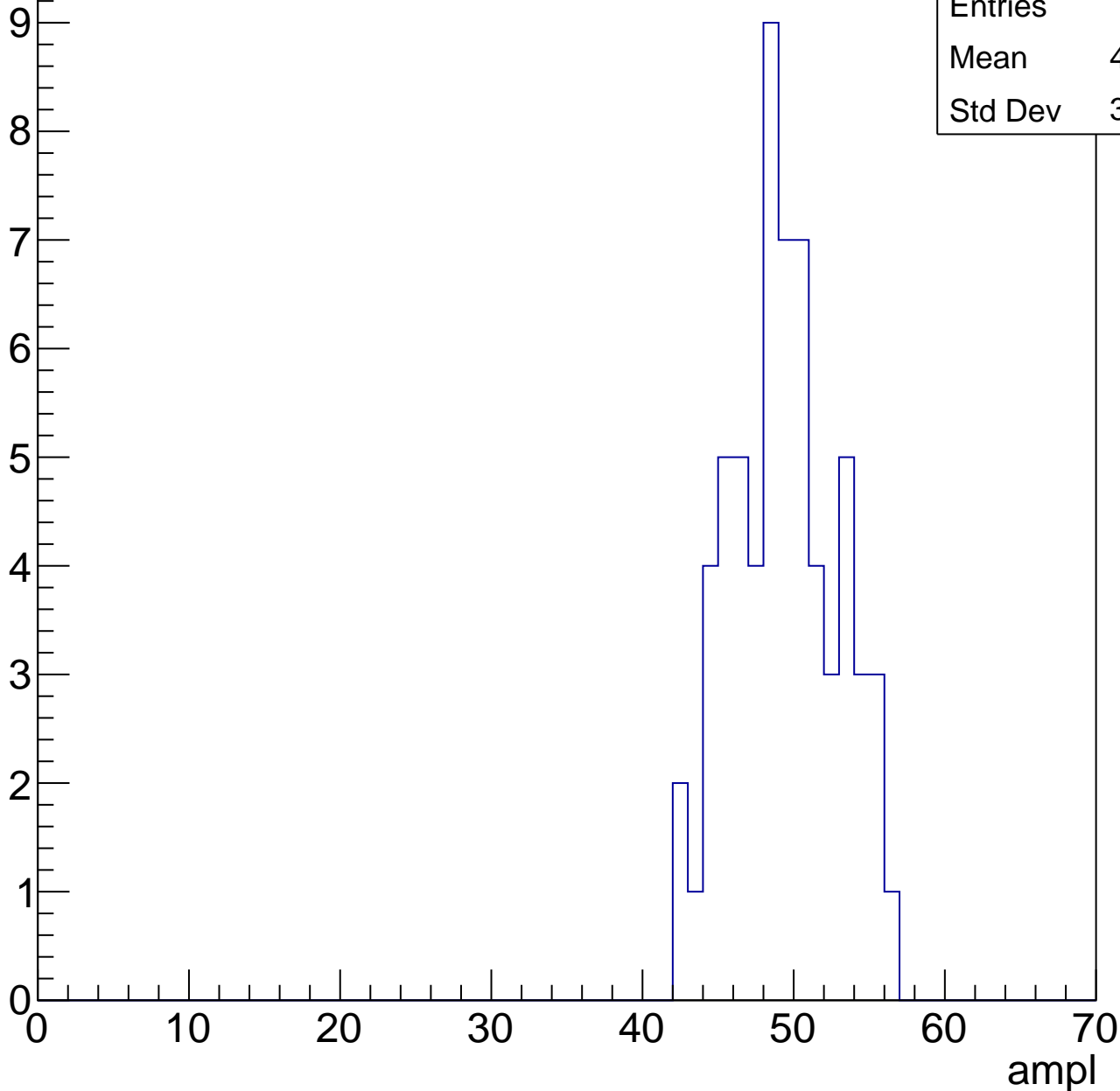


# B1L103S, U2-ch101, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	48.87
Std Dev	3.439

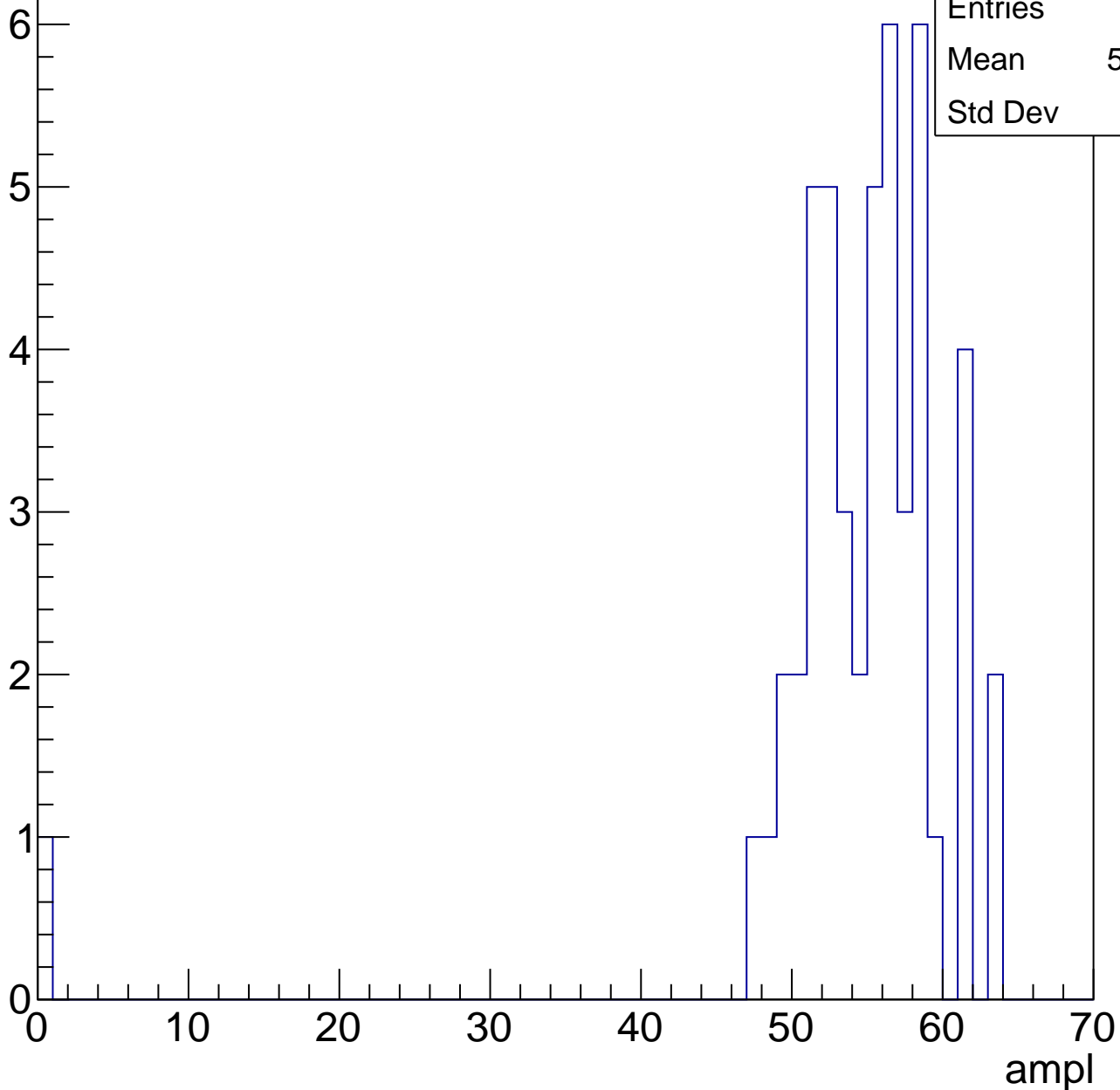


# B1L103S, U2-ch101, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	53.76
Std Dev	8.67

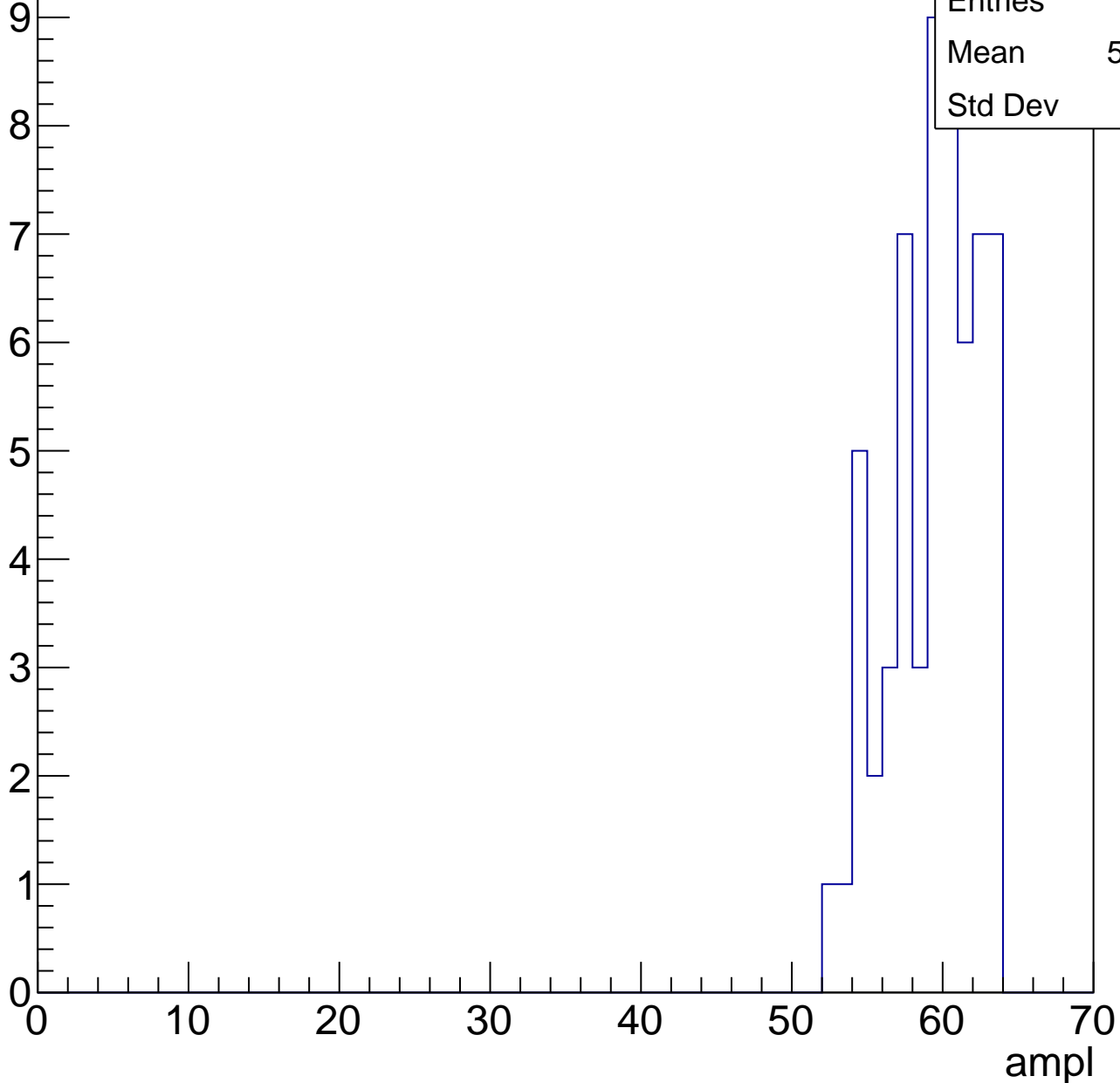


# B1L103S, U2-ch101, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

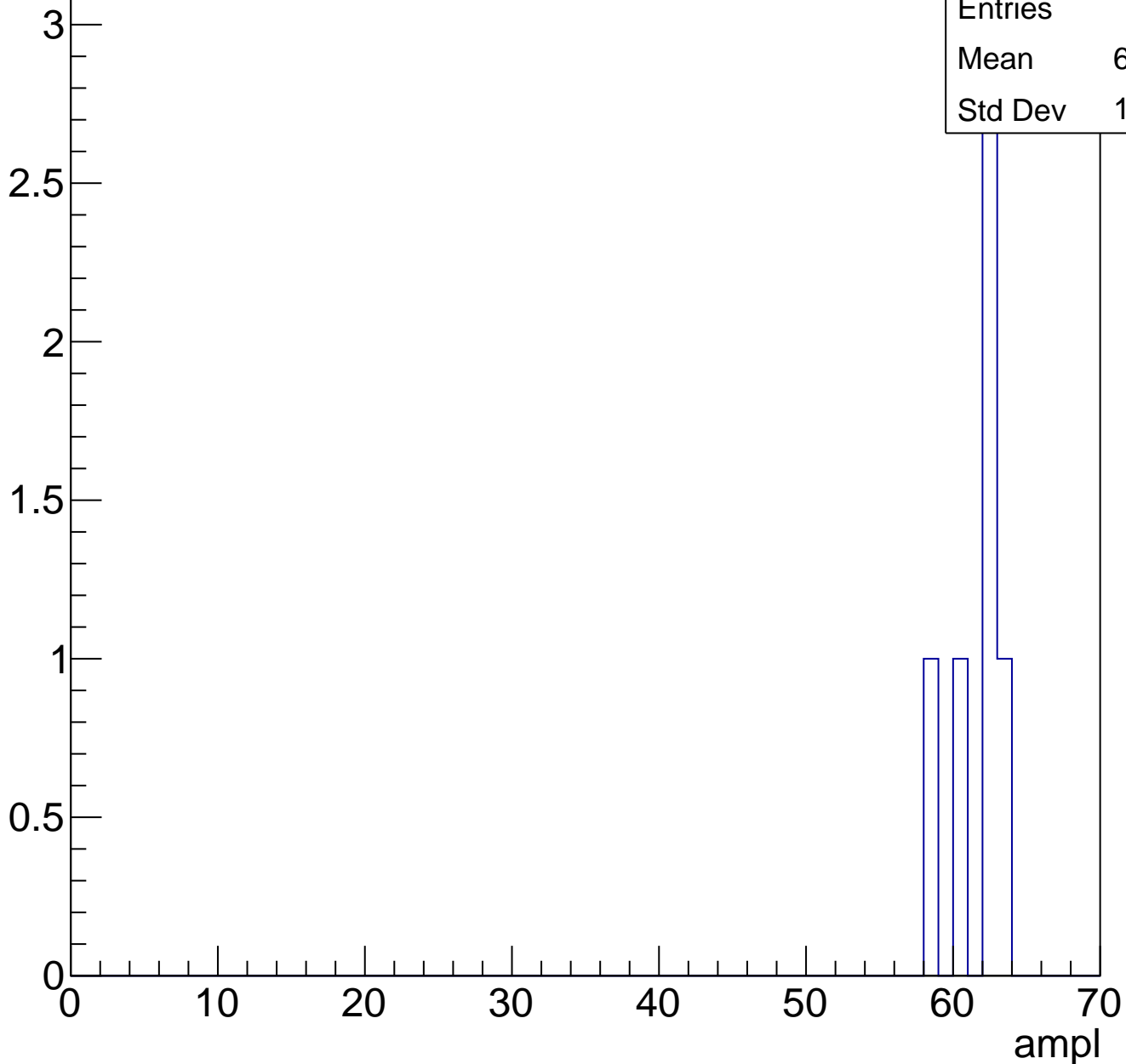
Entries	60
Mean	58.97
Std Dev	2.91



# B1L103S, U2-ch101, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U2-ch101, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U2-ch102, adc0

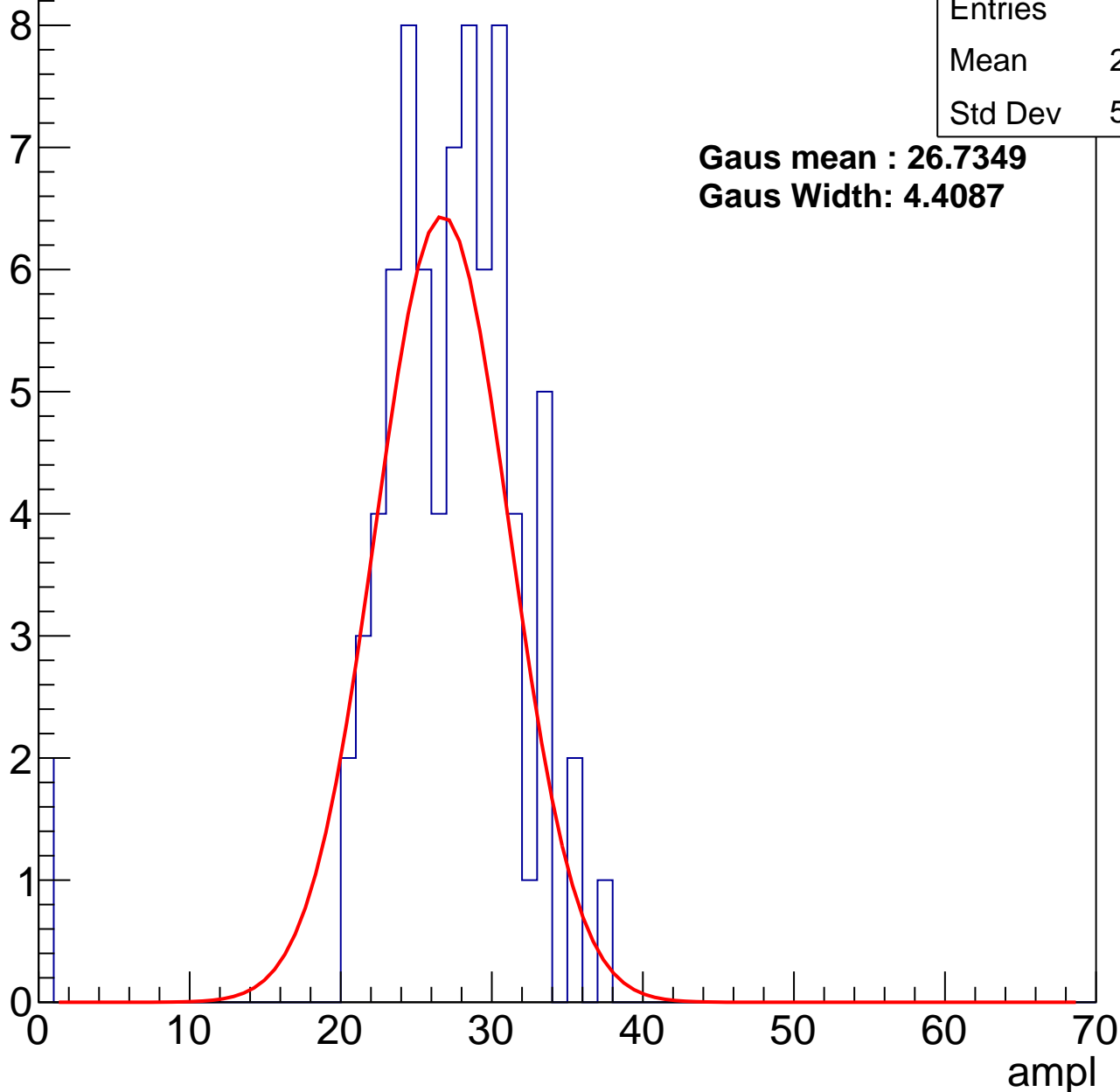
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	26.36
Std Dev	5.732

**Gaus mean : 26.7349**

**Gaus Width: 4.4087**



# B1L103S, U2-ch102, adc1

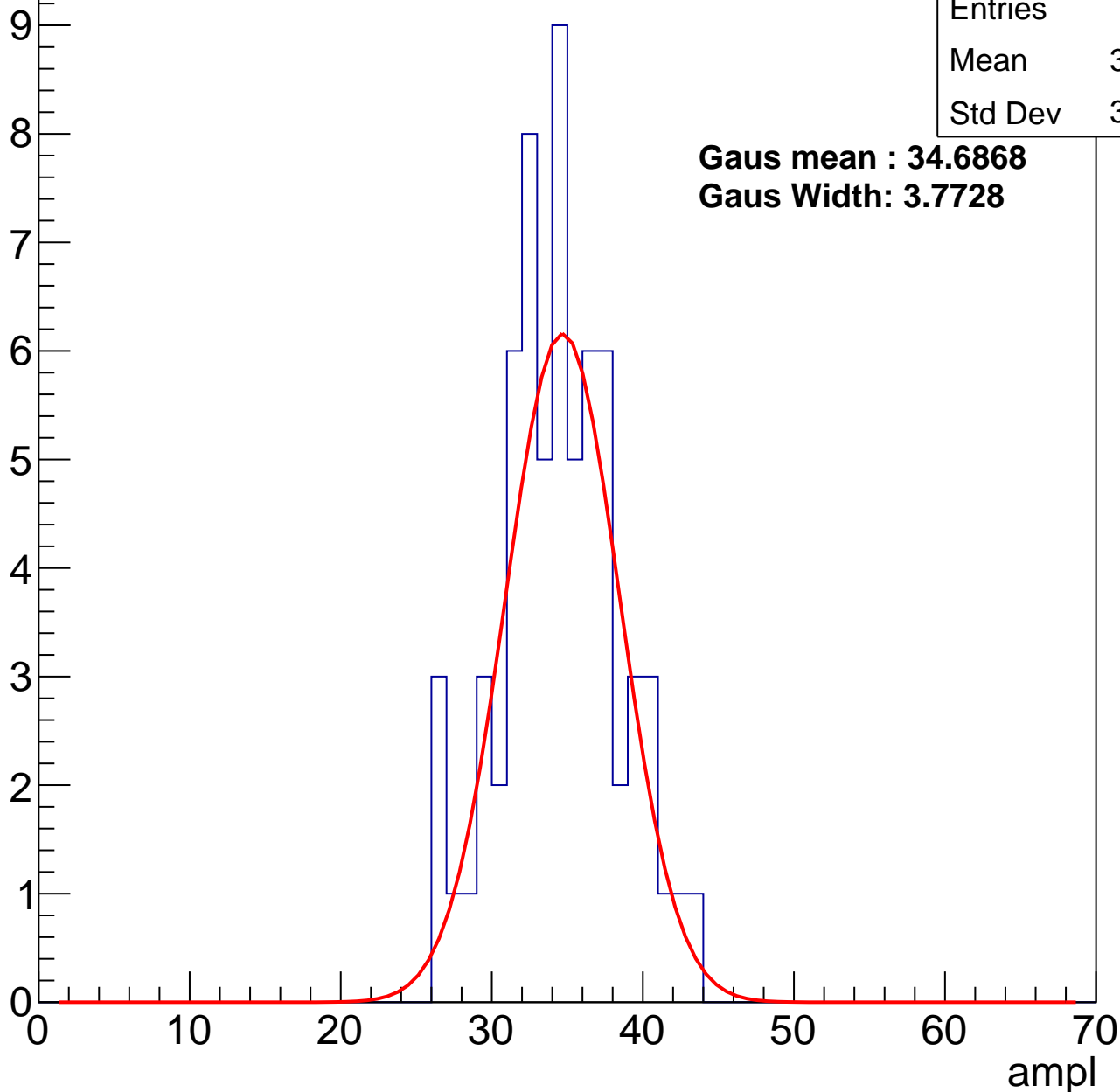
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	34.02
Std Dev	3.828

**Gaus mean : 34.6868**

**Gaus Width: 3.7728**



# B1L103S, U2-ch102, adc2

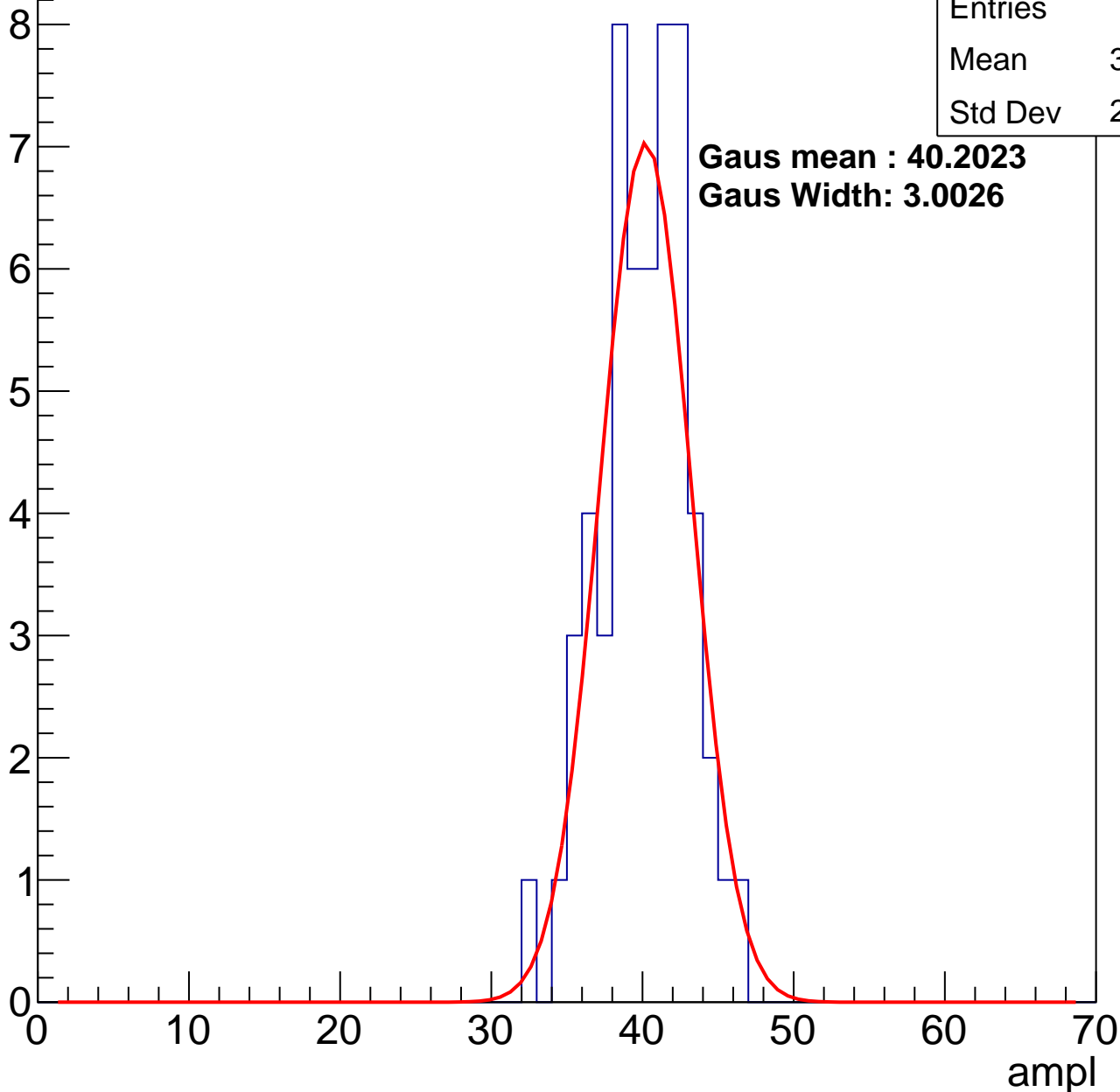
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	39.62
Std Dev	2.882

**Gaus mean : 40.2023**

**Gaus Width: 3.0026**

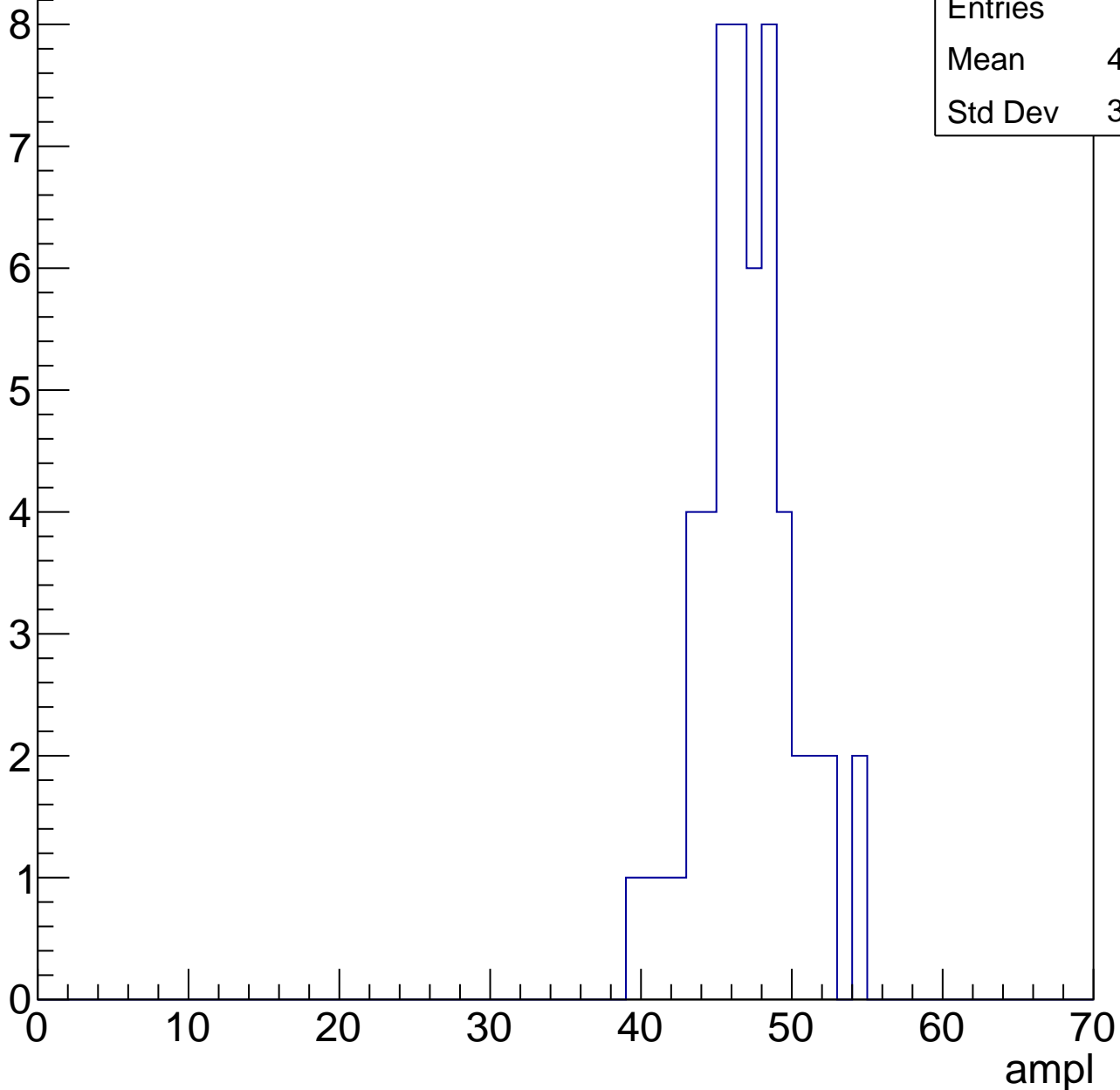


# B1L103S, U2-ch102, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	46.56
Std Dev	3.119

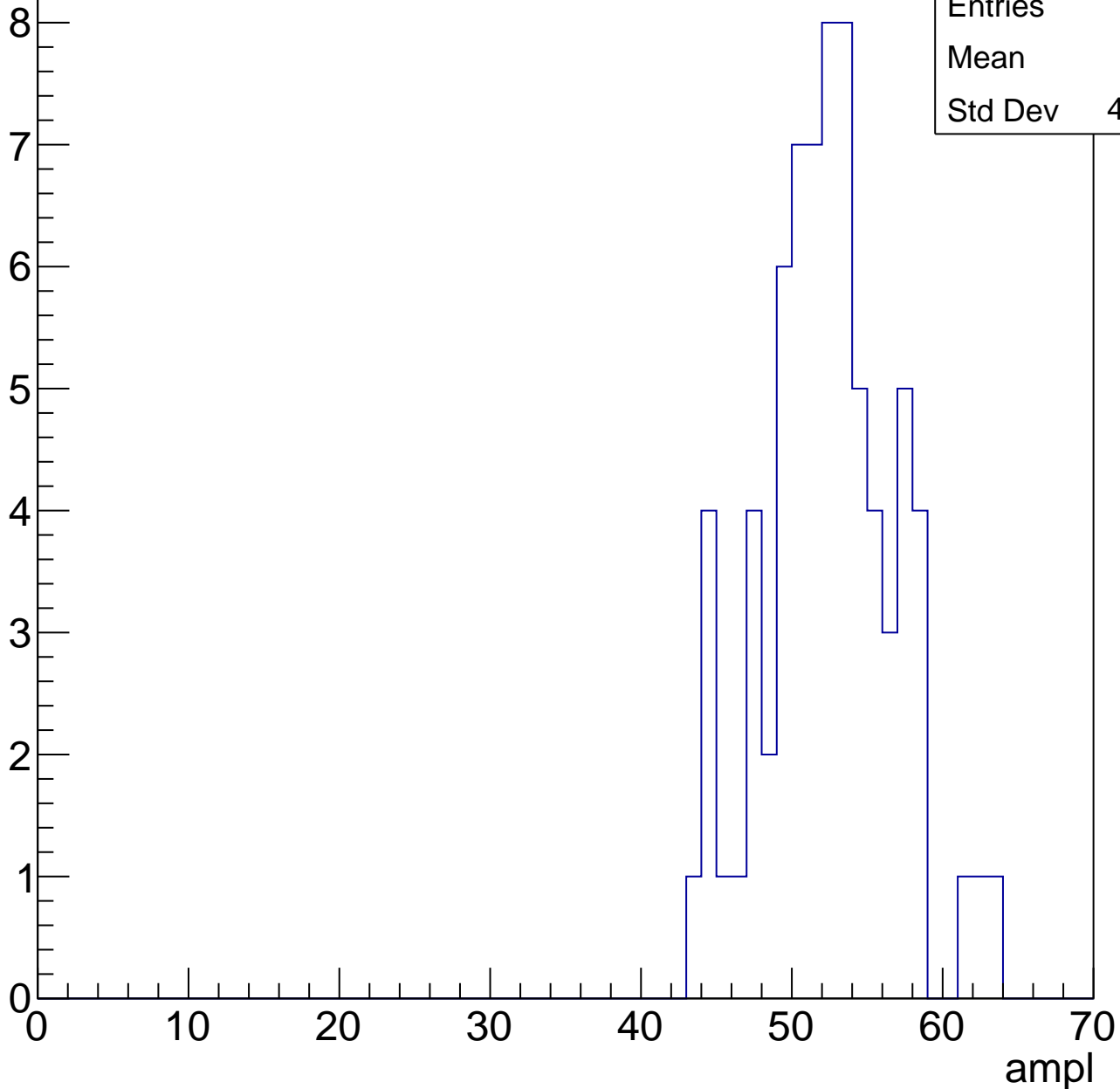


# B1L103S, U2-ch102, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	52
Std Dev	4.262

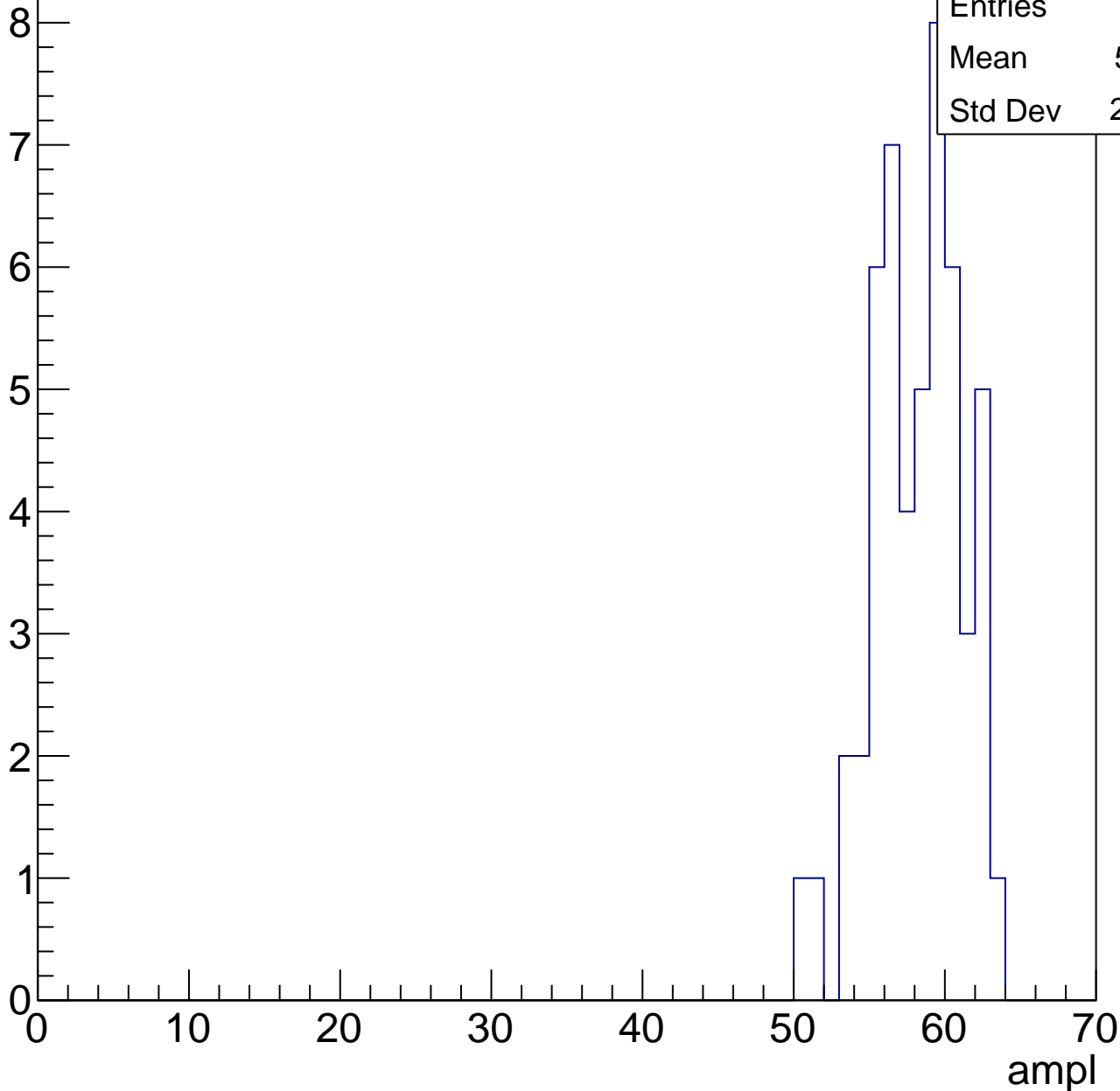


# B1L103S, U2-ch102, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	57.71
Std Dev	2.939

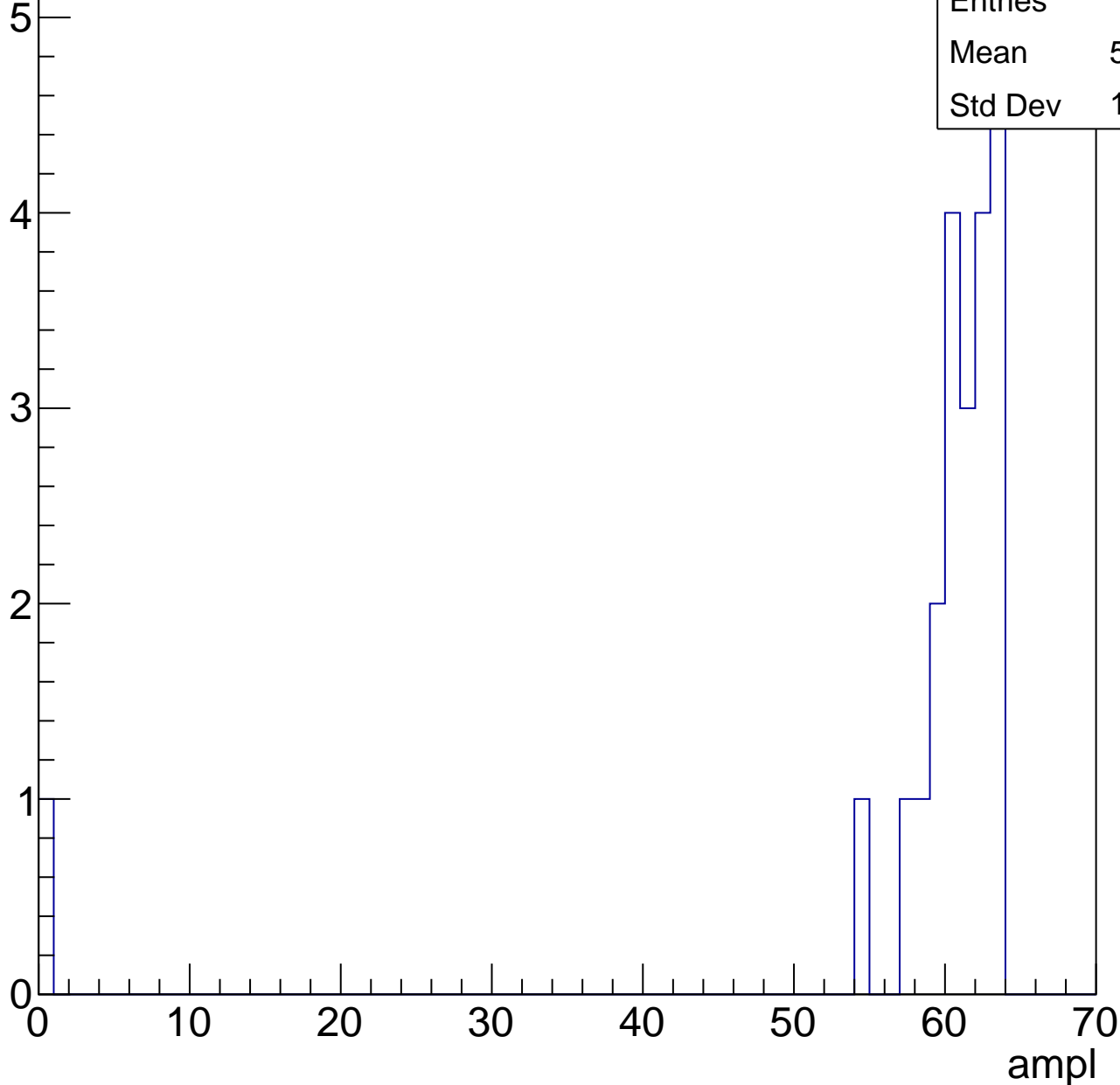


# B1L103S, U2-ch102, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	22
Mean	57.86
Std Dev	12.82

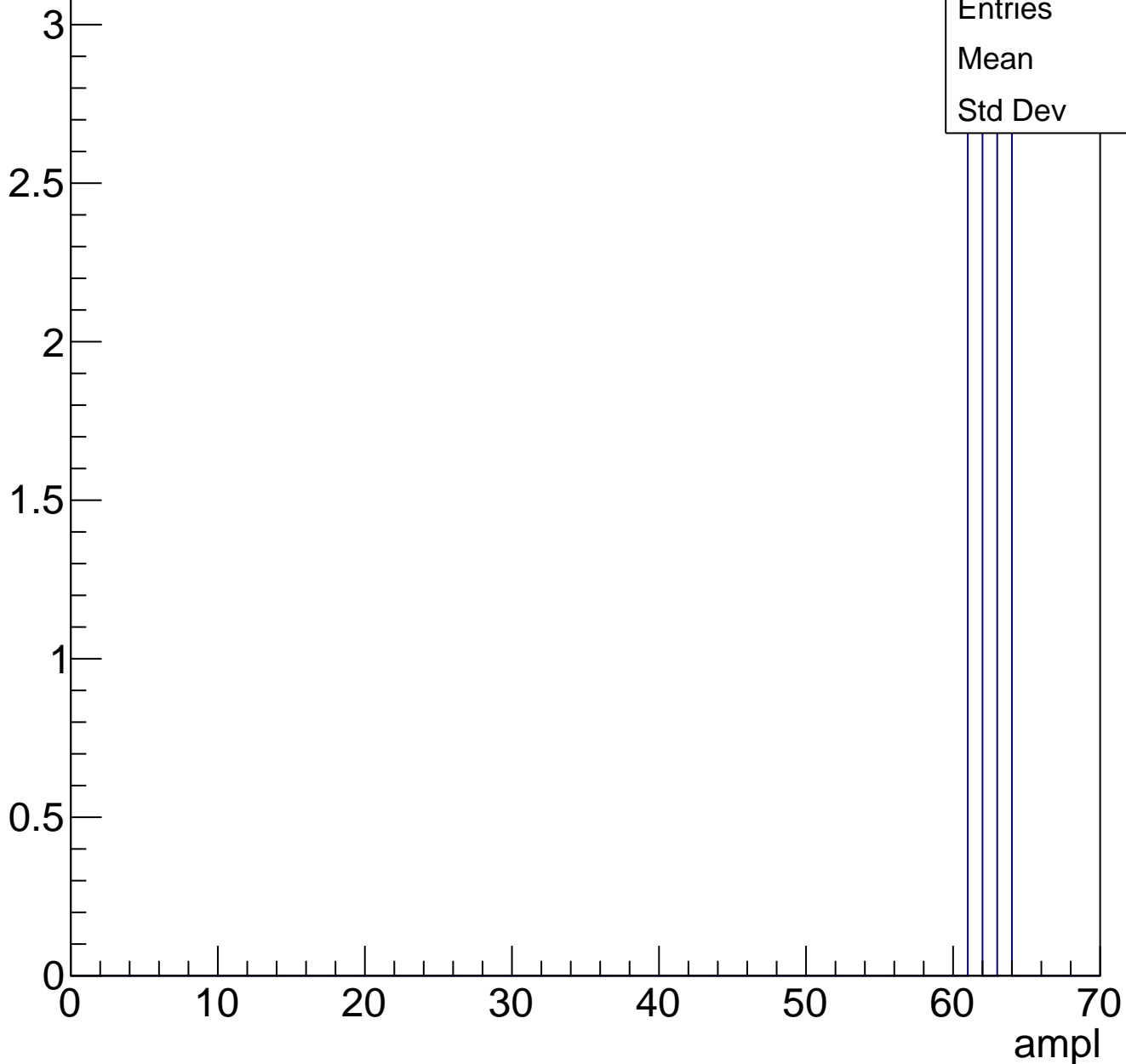




# B1L103S, U2-ch102, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch103, adc0

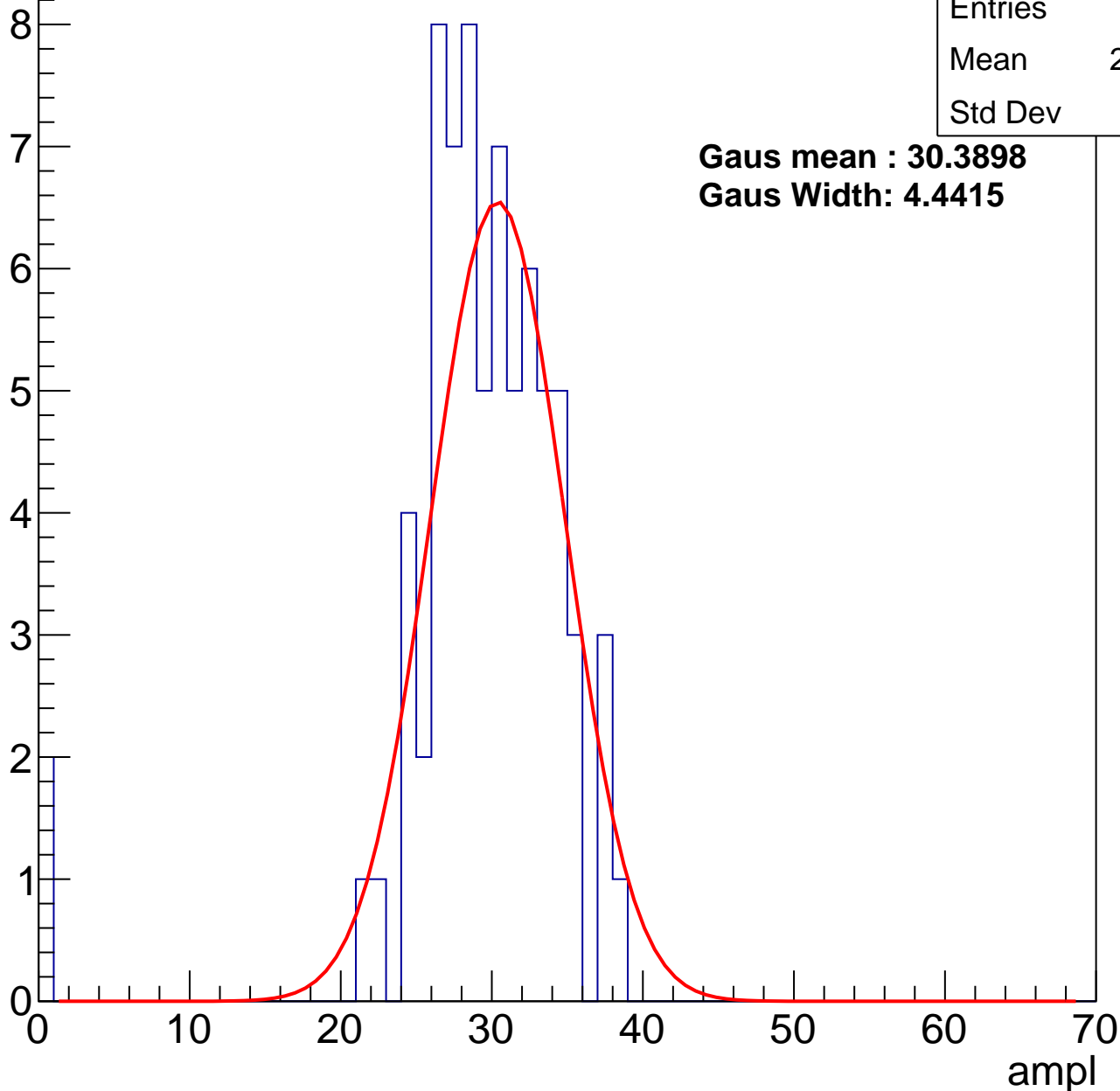
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	28.78
Std Dev	6.08

**Gaus mean : 30.3898**

**Gaus Width: 4.4415**



# B1L103S, U2-ch103, adc1

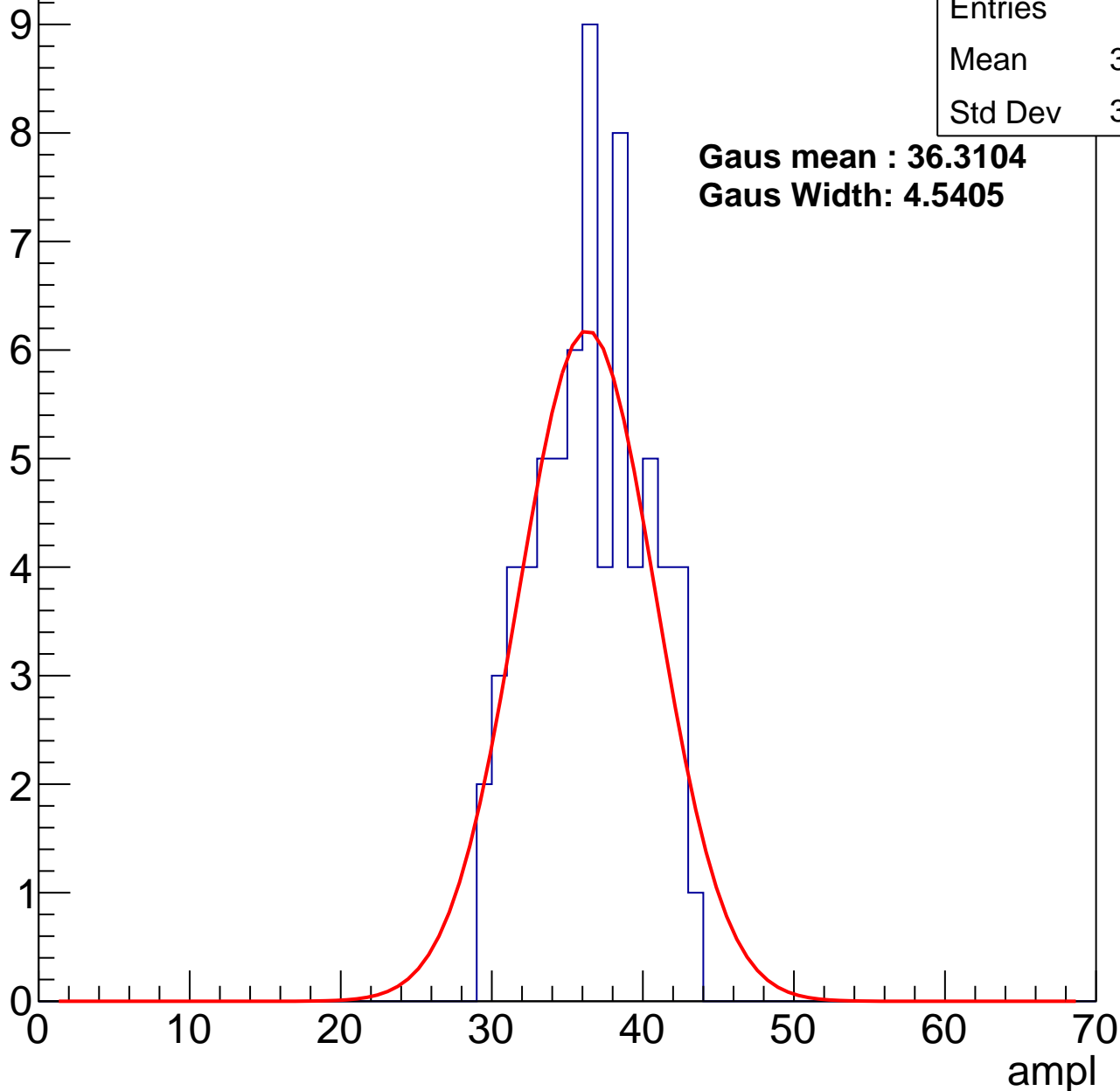
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	36.06
Std Dev	3.609

**Gaus mean : 36.3104**

**Gaus Width: 4.5405**



# B1L103S, U2-ch103, adc2

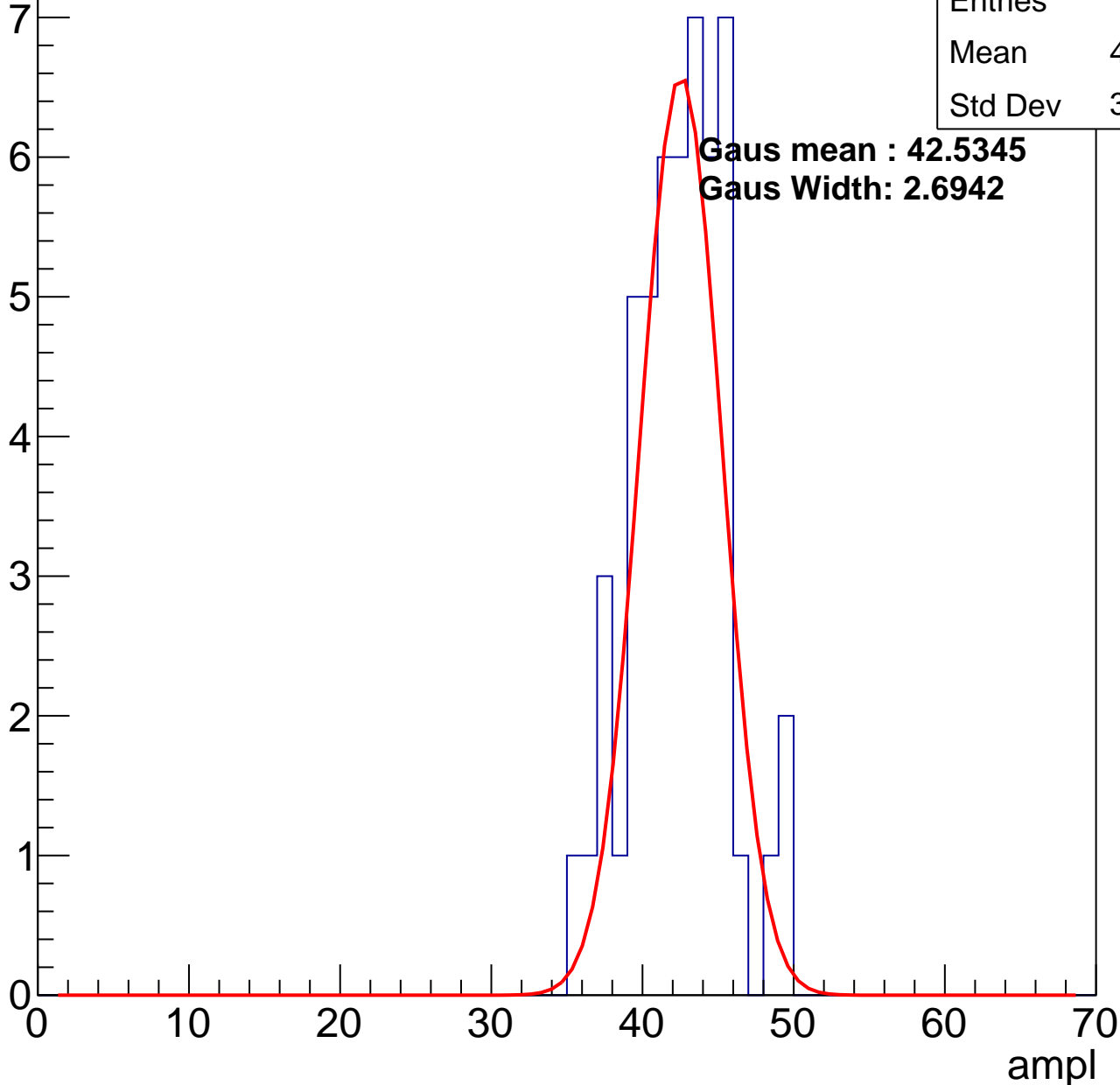
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	42.02
Std Dev	3.073

**Gaus mean : 42.5345**

**Gaus Width: 2.6942**

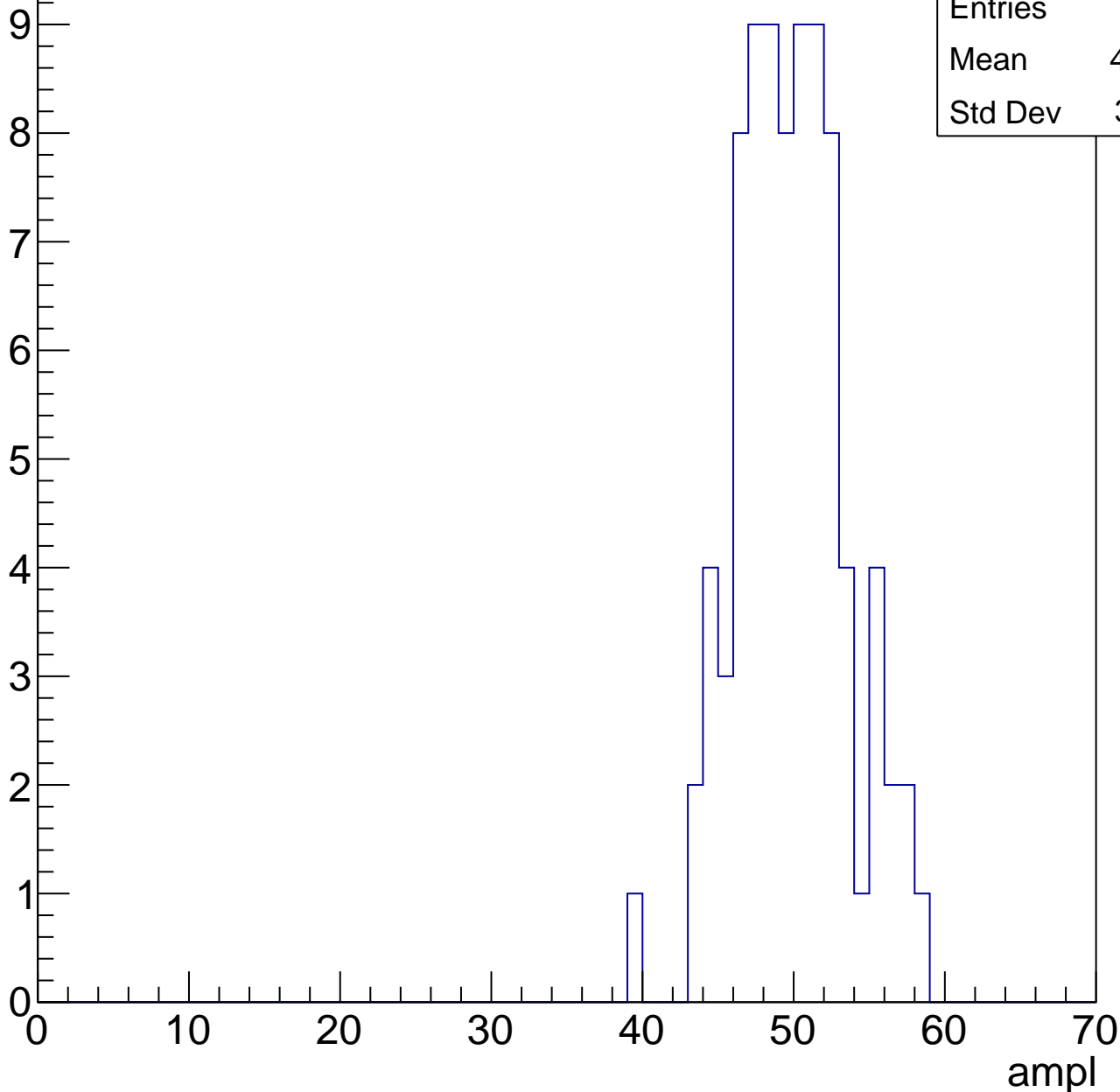


# B1L103S, U2-ch103, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	84
Mean	49.36
Std Dev	3.591

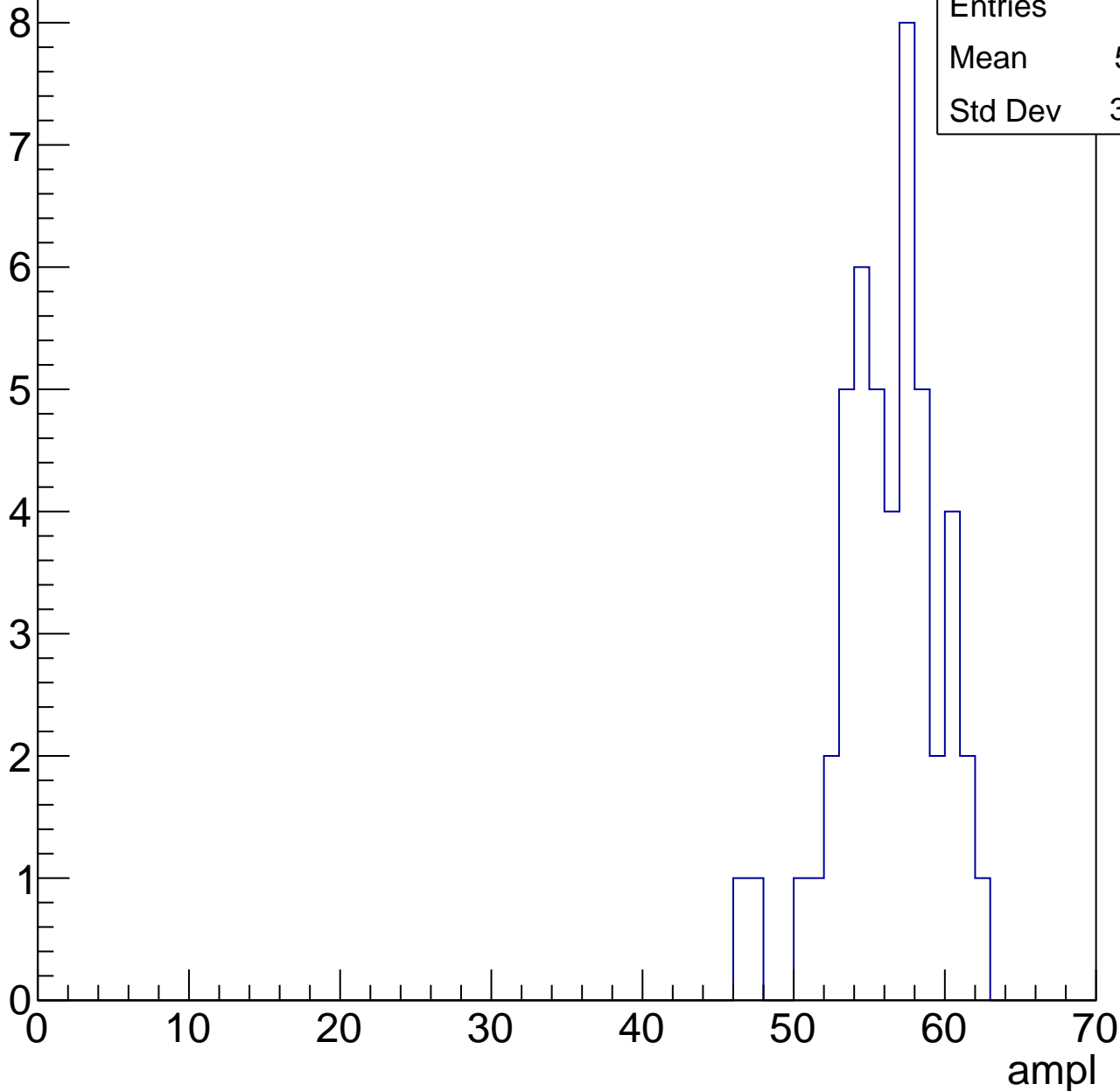


# B1L103S, U2-ch103, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

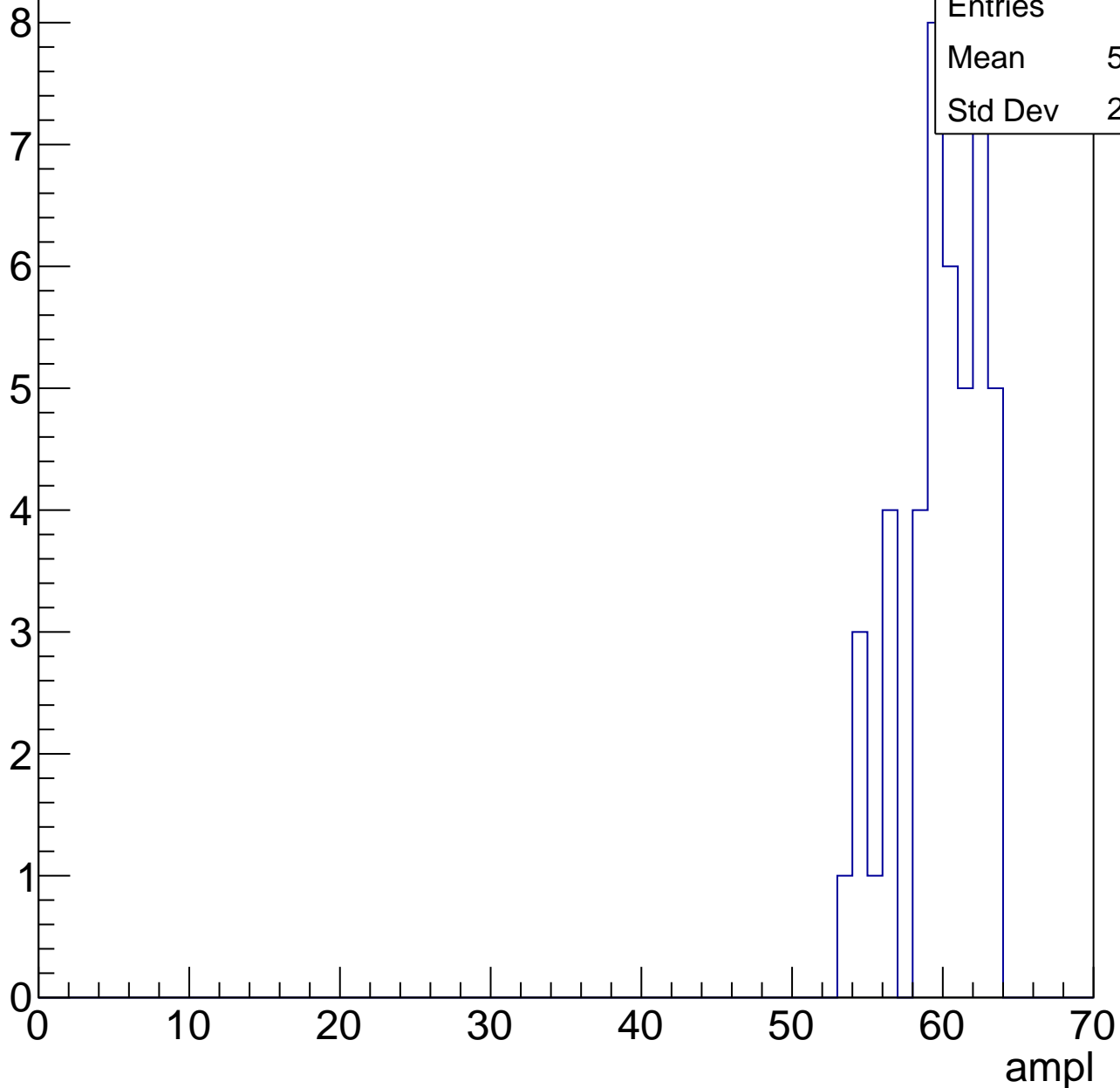
Entries	48
Mean	55.71
Std Dev	3.354



# B1L103S, U2-ch103, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

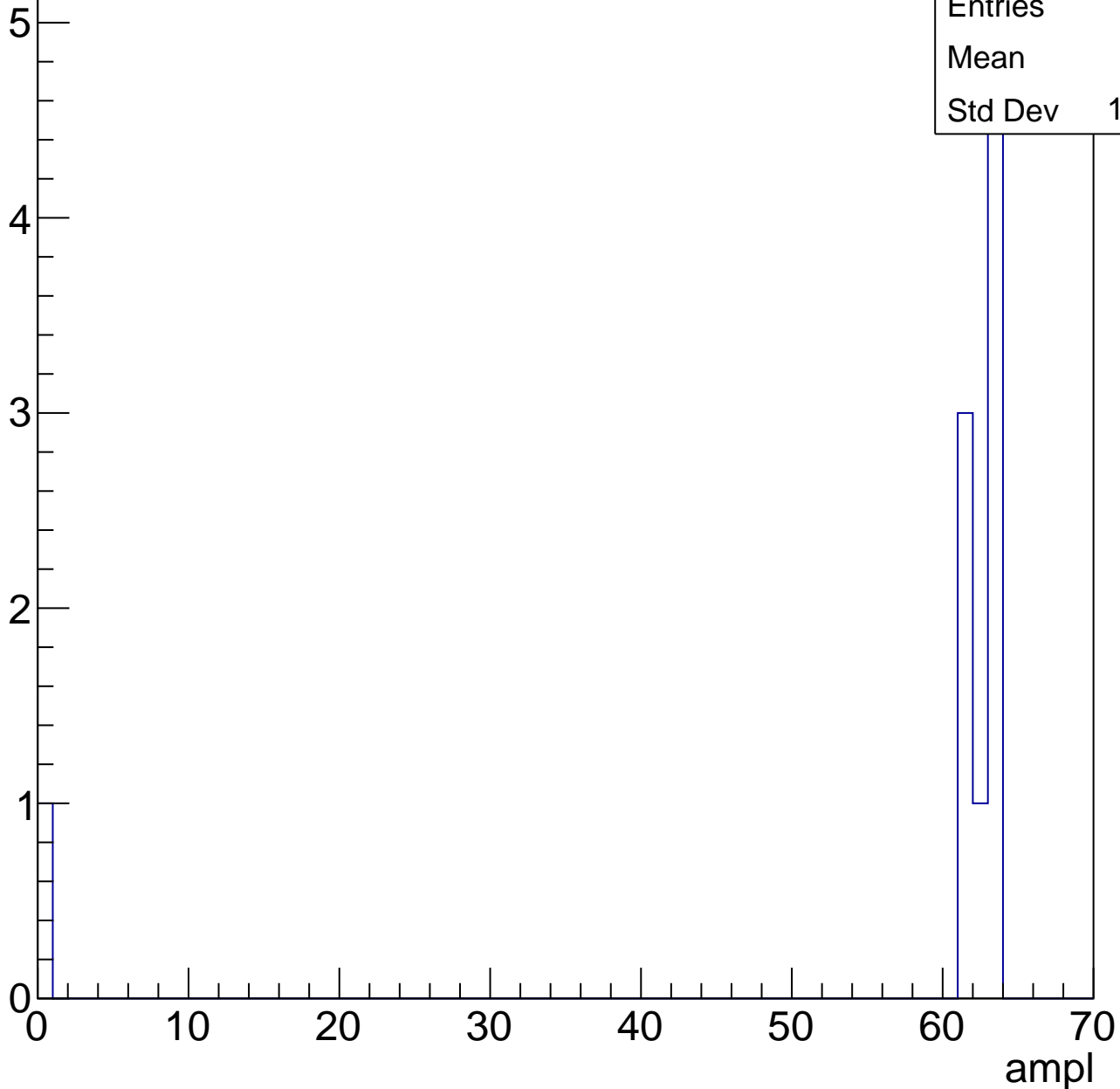


# B1L103S, U2-ch103, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	10
Mean	56
Std Dev	18.69





# B1L103S, U2-ch103, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U2-ch104, adc0

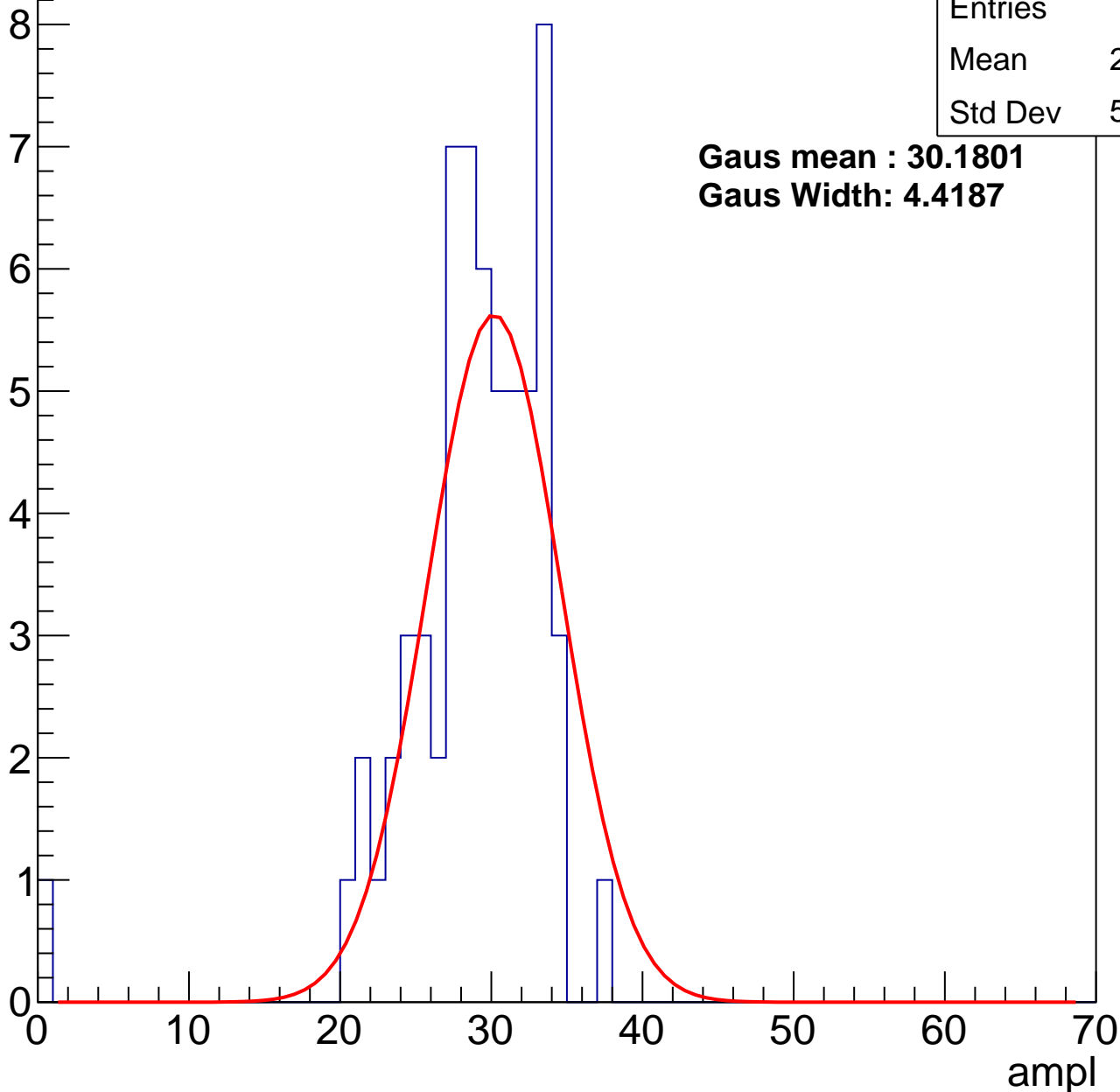
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	28.32
Std Dev	5.167

**Gaus mean : 30.1801**

**Gaus Width: 4.4187**



# B1L103S, U2-ch104, adc1

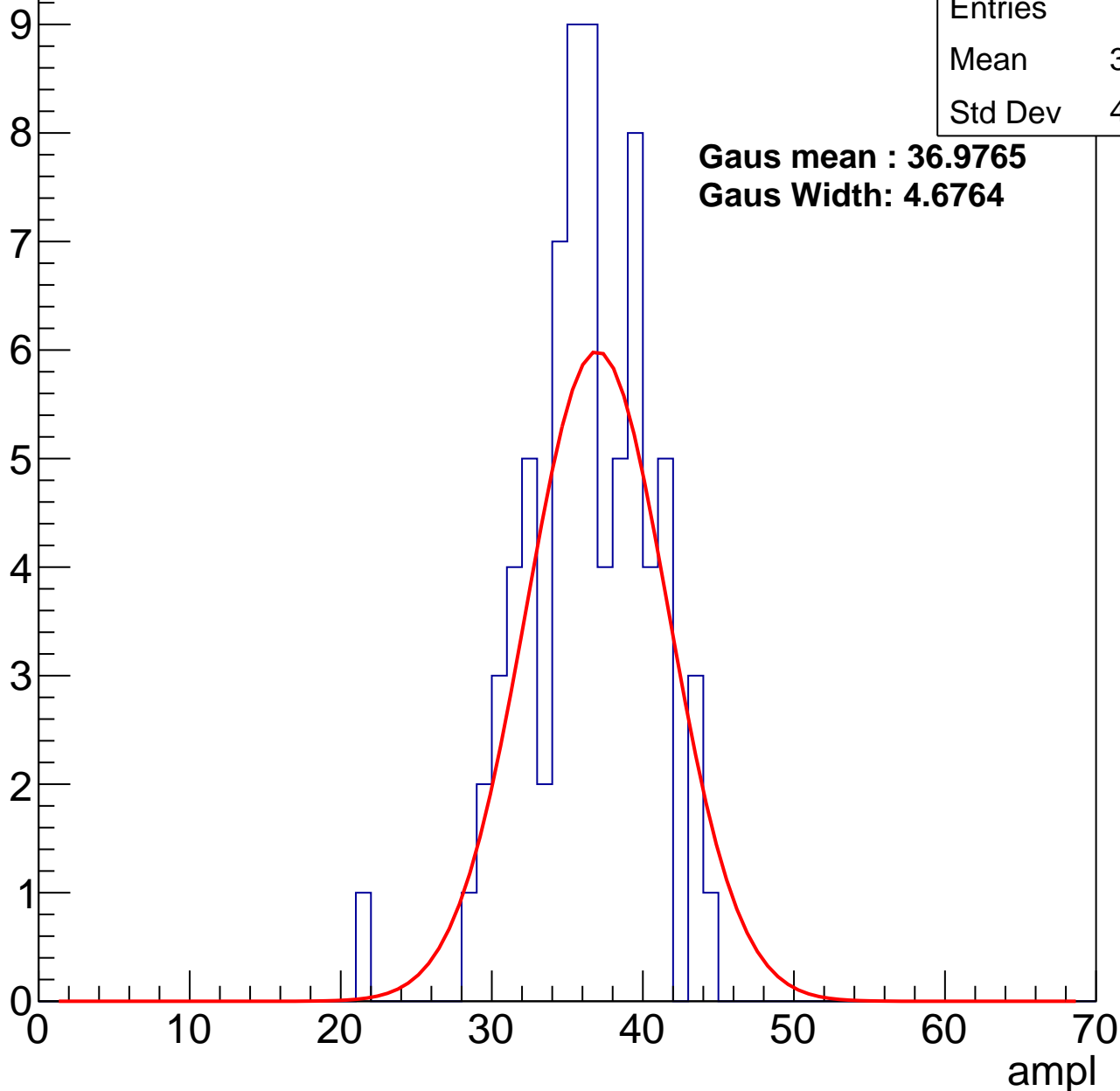
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	35.78
Std Dev	4.092

**Gaus mean : 36.9765**

**Gaus Width: 4.6764**



# B1L103S, U2-ch104, adc2

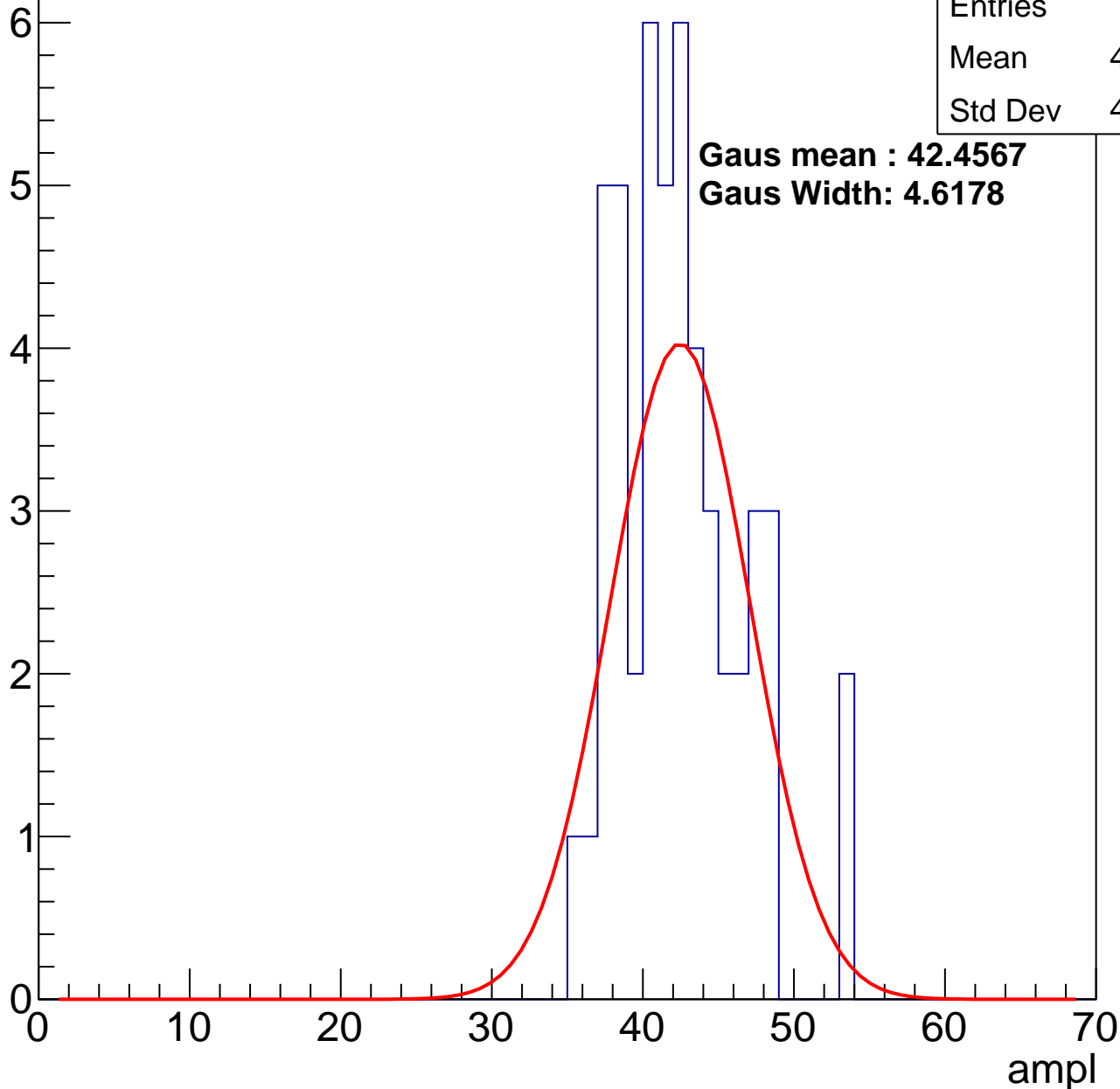
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	41.96
Std Dev	4.069

**Gaus mean : 42.4567**

**Gaus Width: 4.6178**

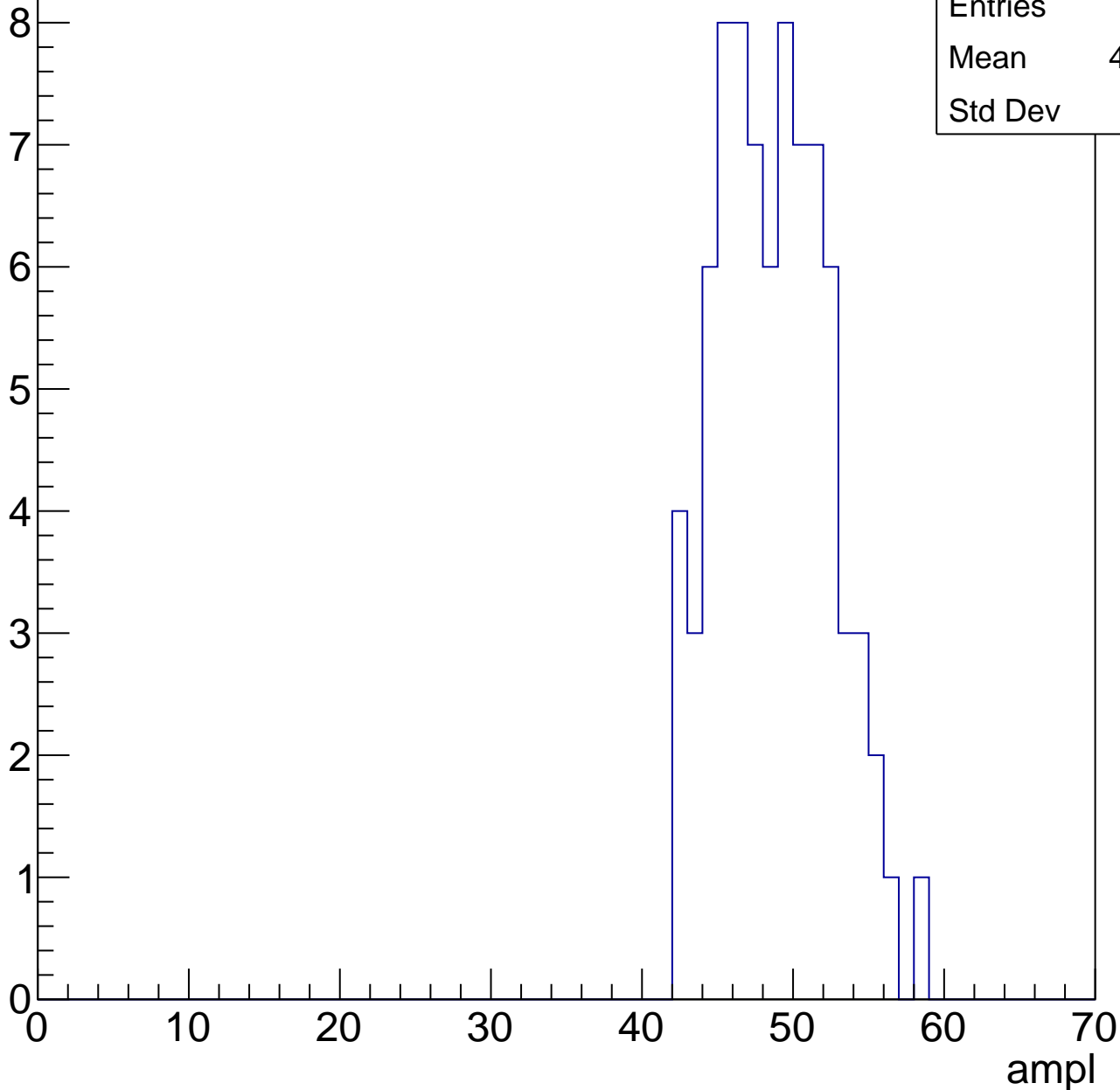


# B1L103S, U2-ch104, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

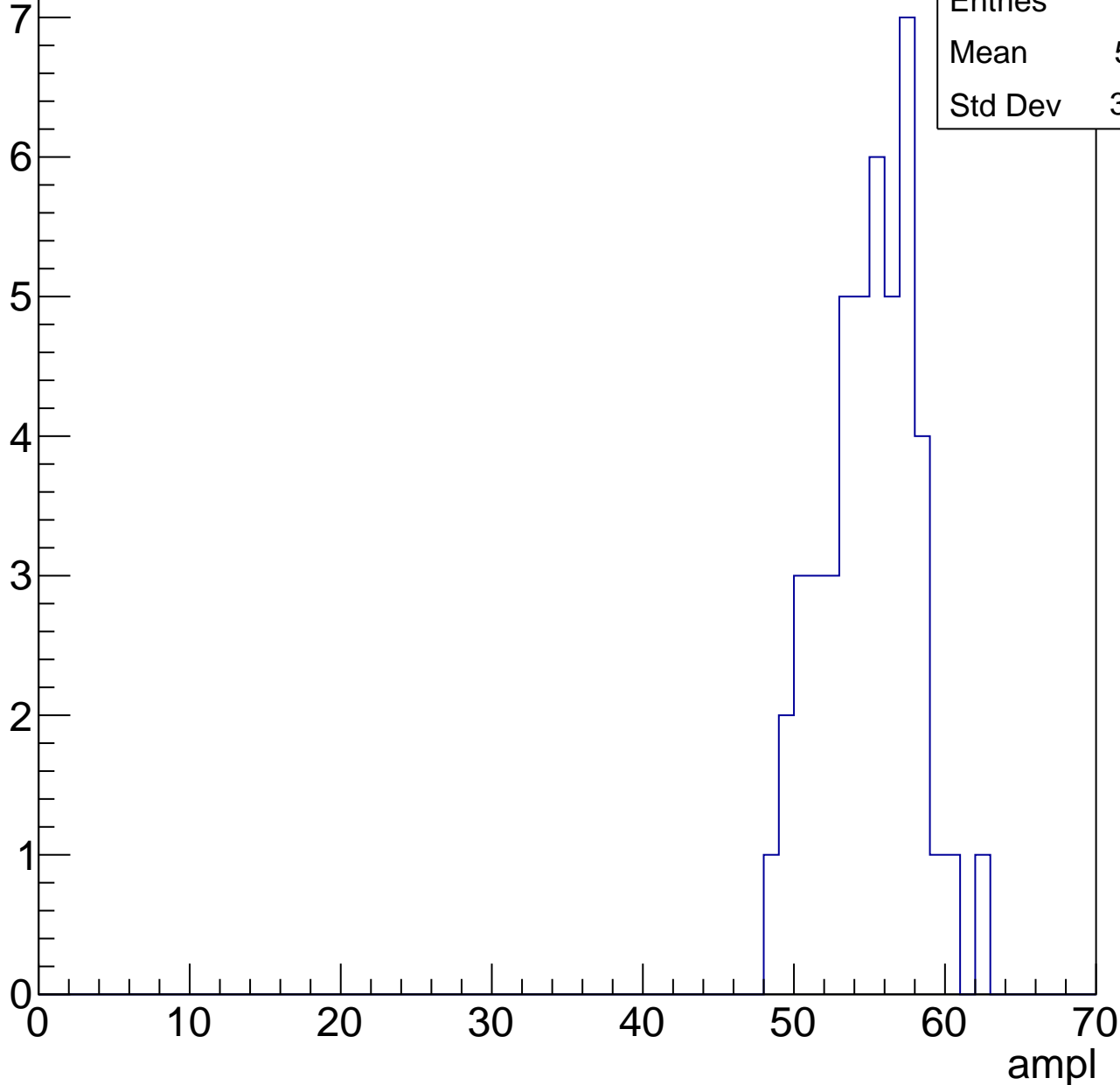
Entries	80
Mean	48.27
Std Dev	3.64



# B1L103S, U2-ch104, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



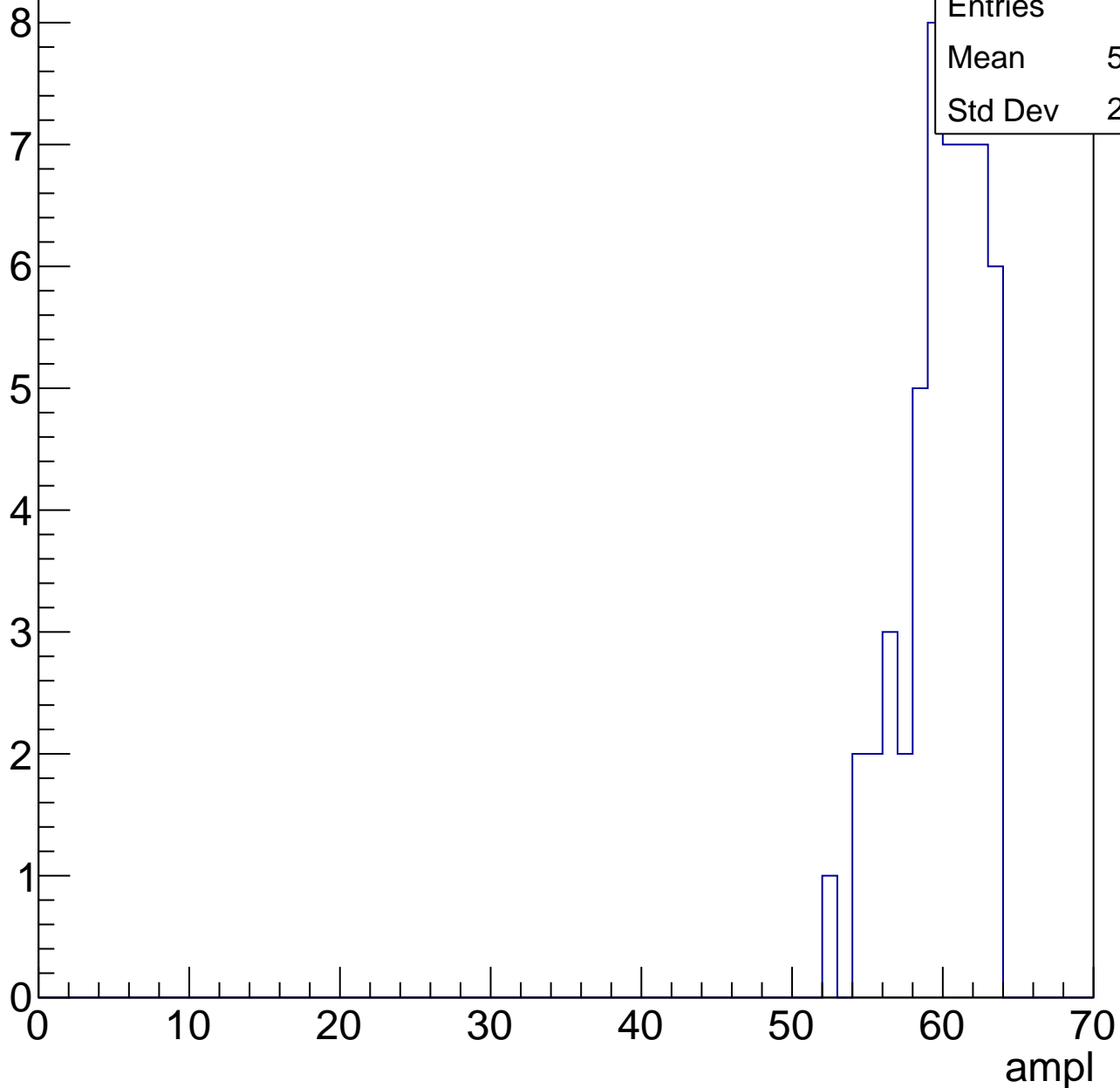
Entries	47
Mean	54.51
Std Dev	3.073

# B1L103S, U2-ch104, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

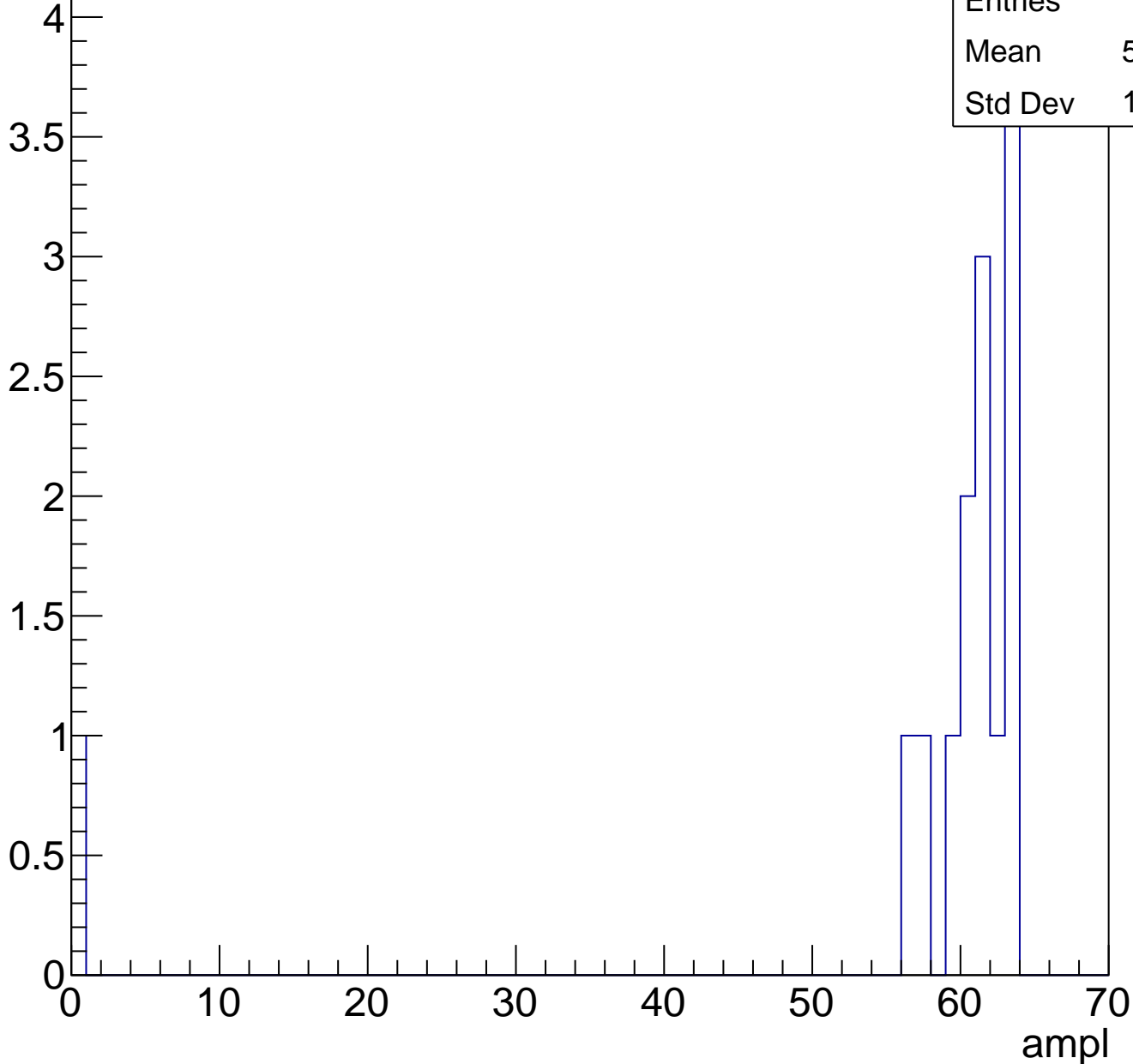
Entries	50
Mean	59.46
Std Dev	2.662



# B1L103S, U2-ch104, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

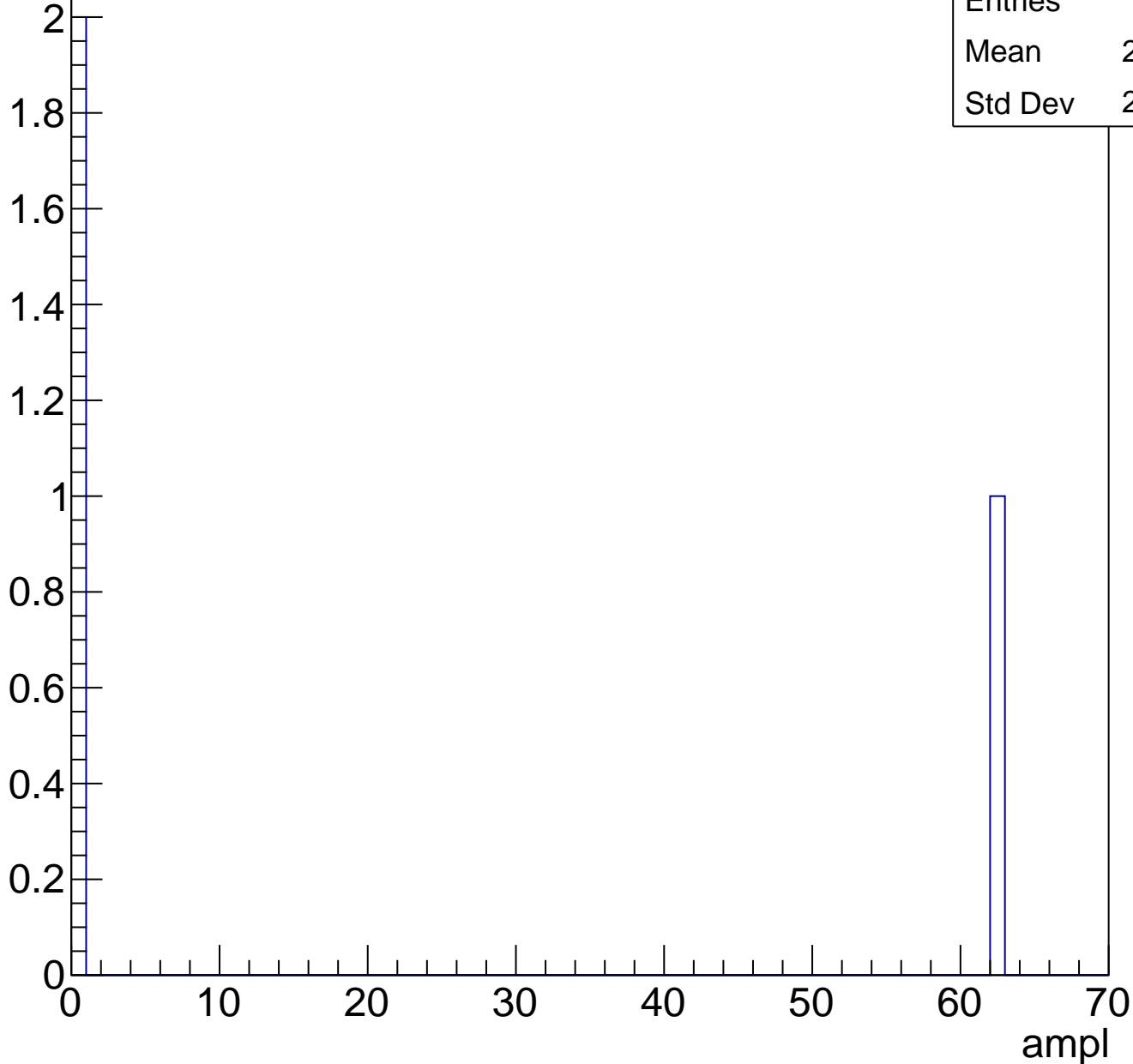




# B1L103S, U2-ch104, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch105, adc0

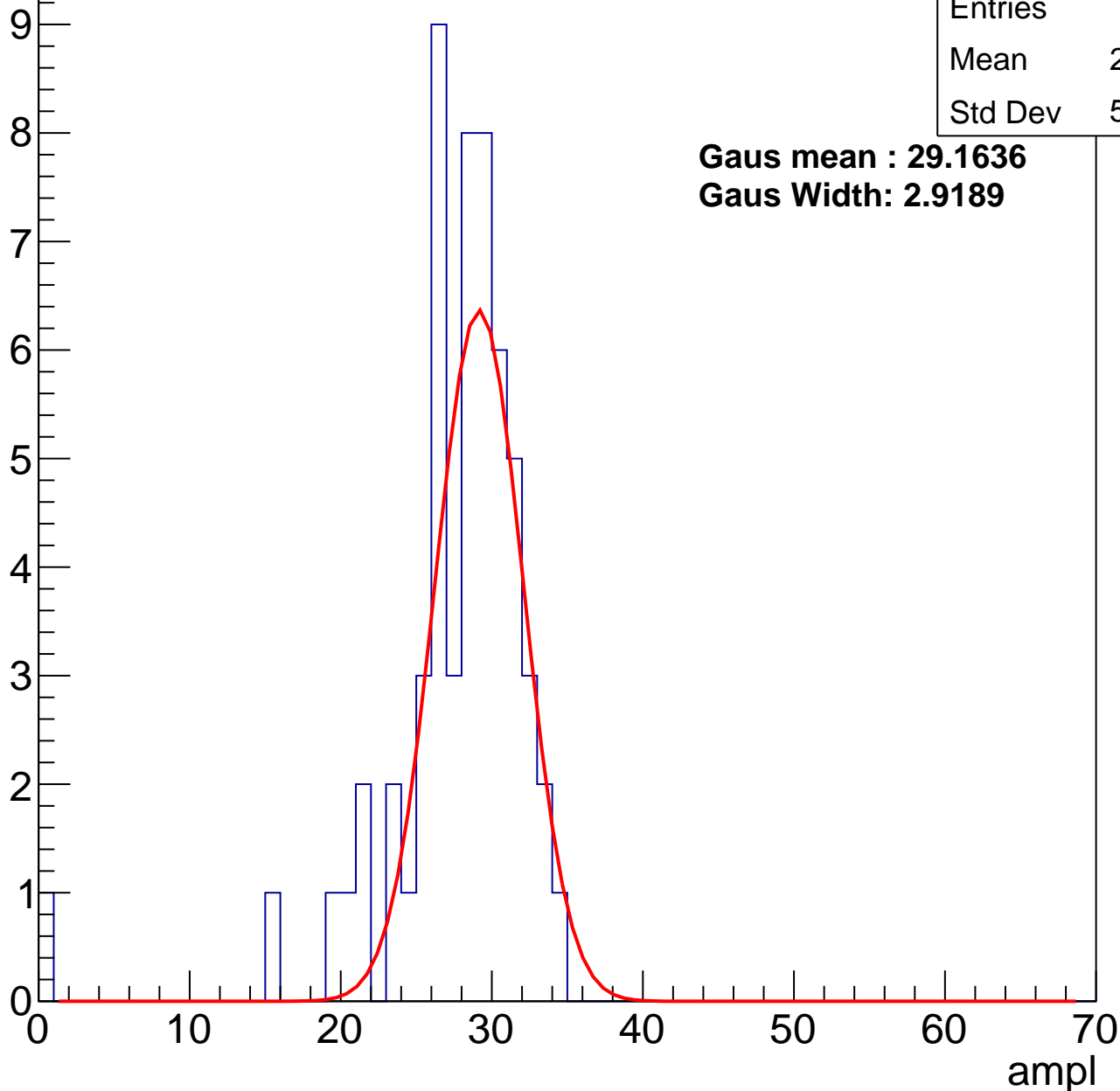
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	27.07
Std Dev	5.112

**Gaus mean : 29.1636**

**Gaus Width: 2.9189**



# B1L103S, U2-ch105, adc1

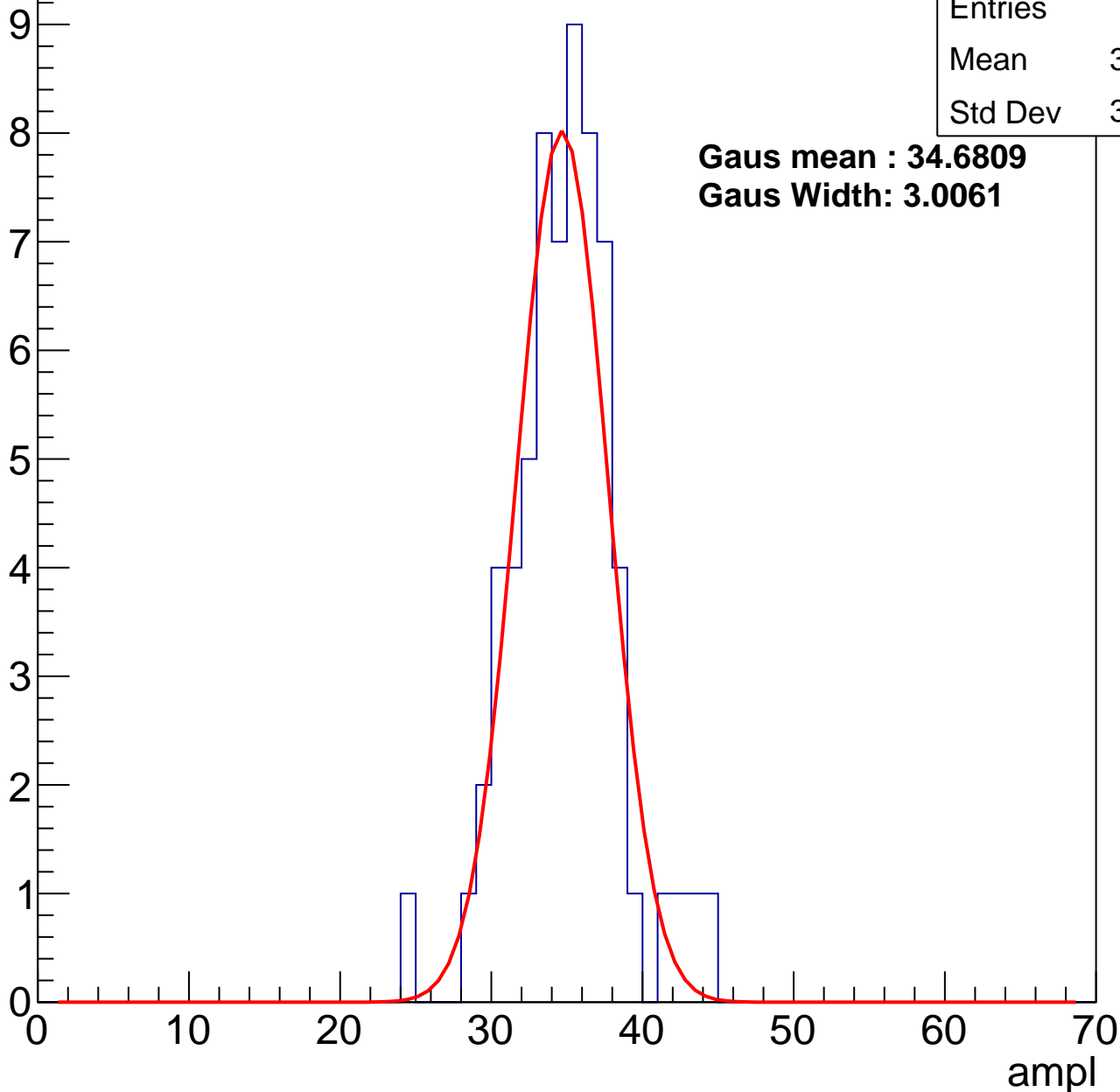
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	34.45
Std Dev	3.482

**Gaus mean : 34.6809**

**Gaus Width: 3.0061**



# B1L103S, U2-ch105, adc2

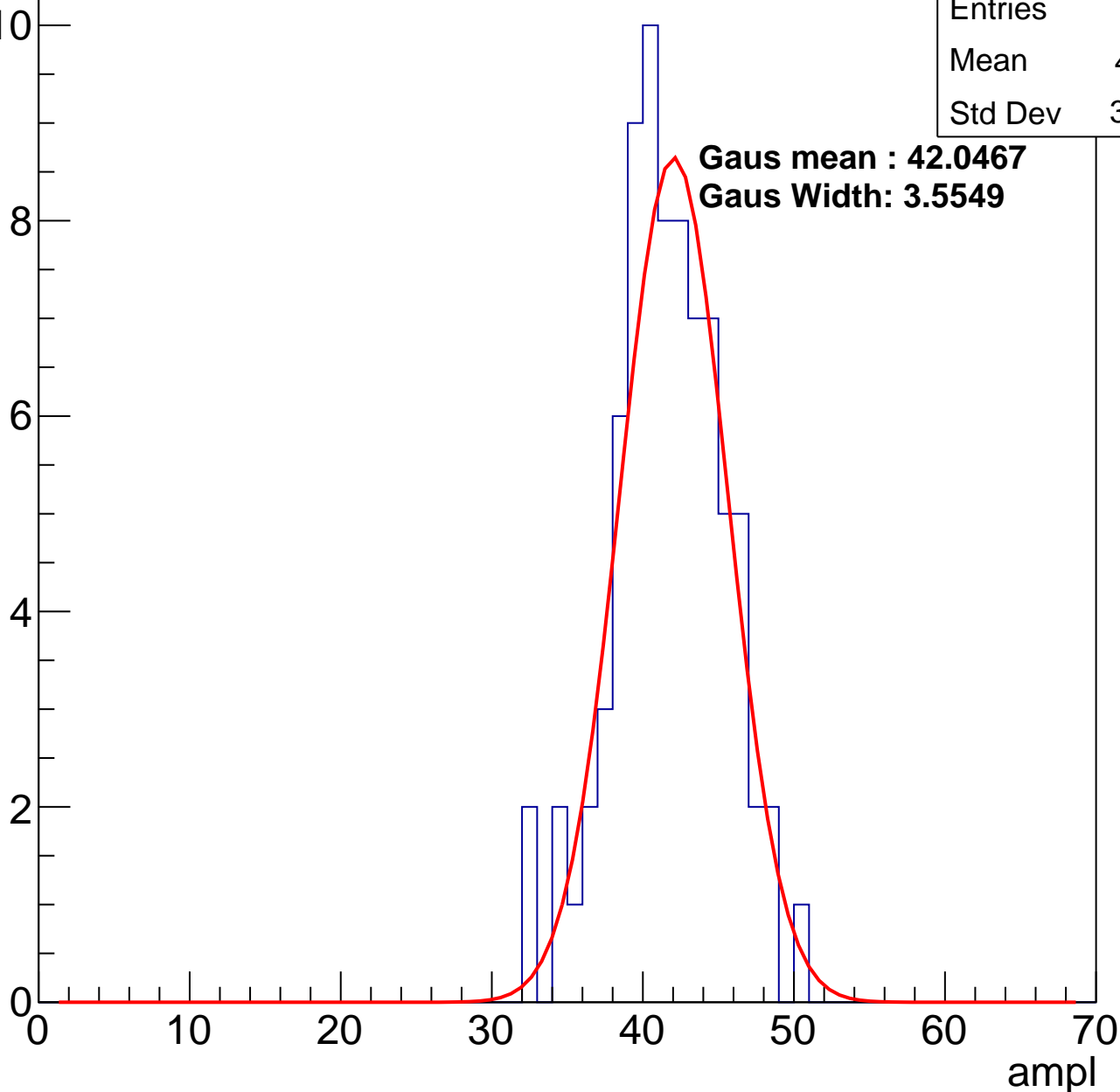
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	80
Mean	41.21
Std Dev	3.615

**Gaus mean : 42.0467**

**Gaus Width: 3.5549**

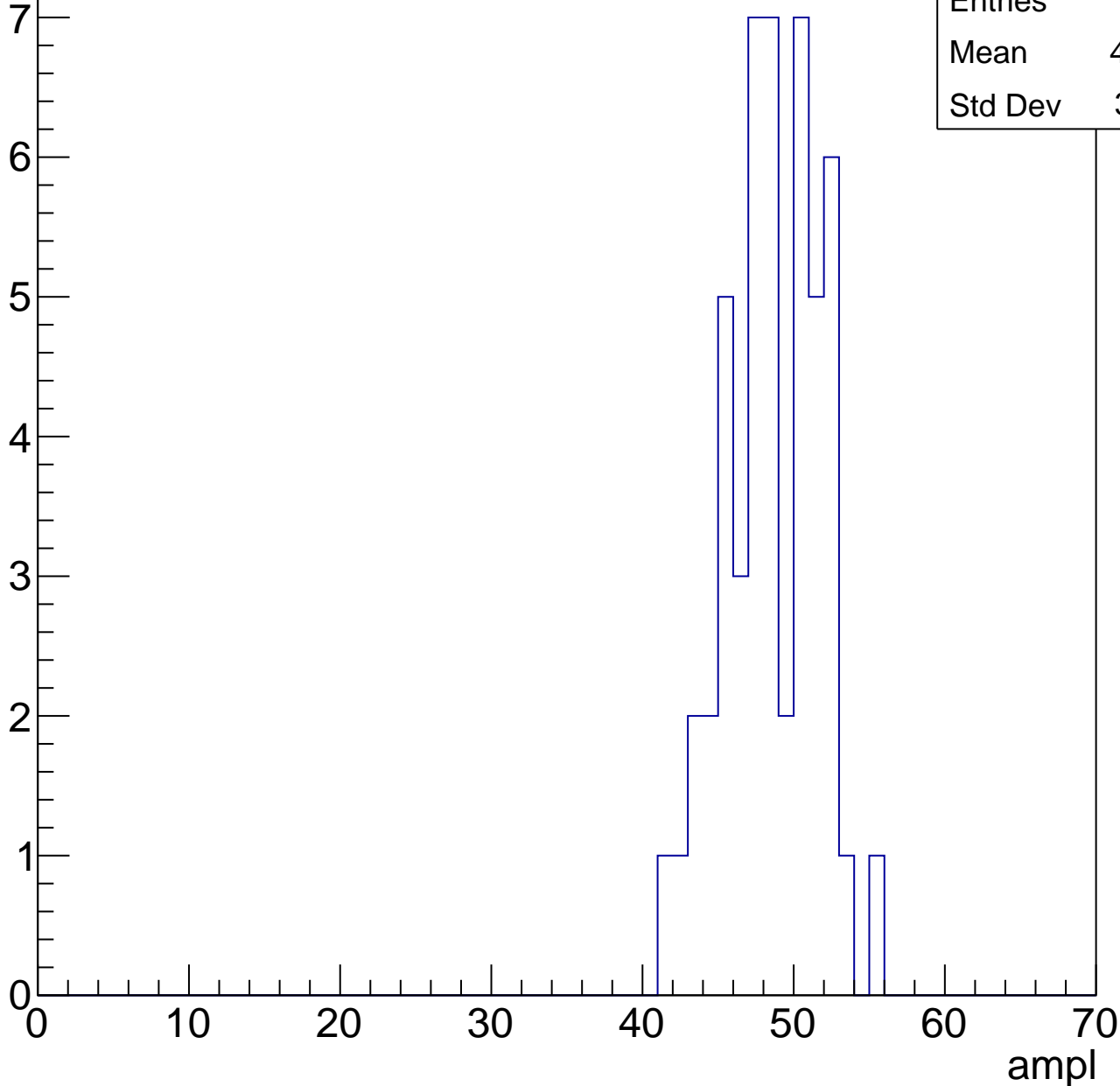


# B1L103S, U2-ch105, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	48.16
Std Dev	3.081

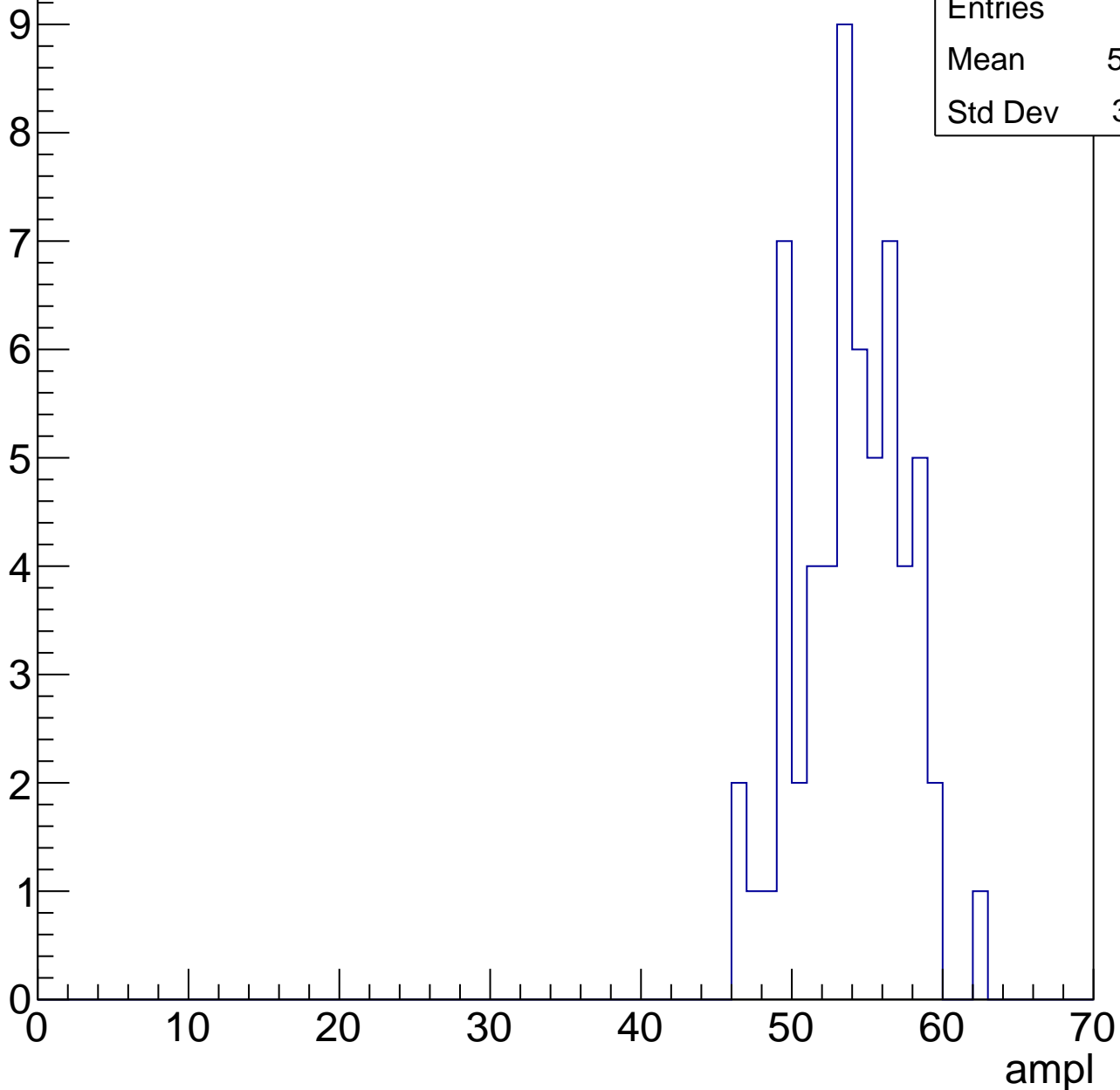


# B1L103S, U2-ch105, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	53.47
Std Dev	3.481



# B1L103S, U2-ch105, adc5

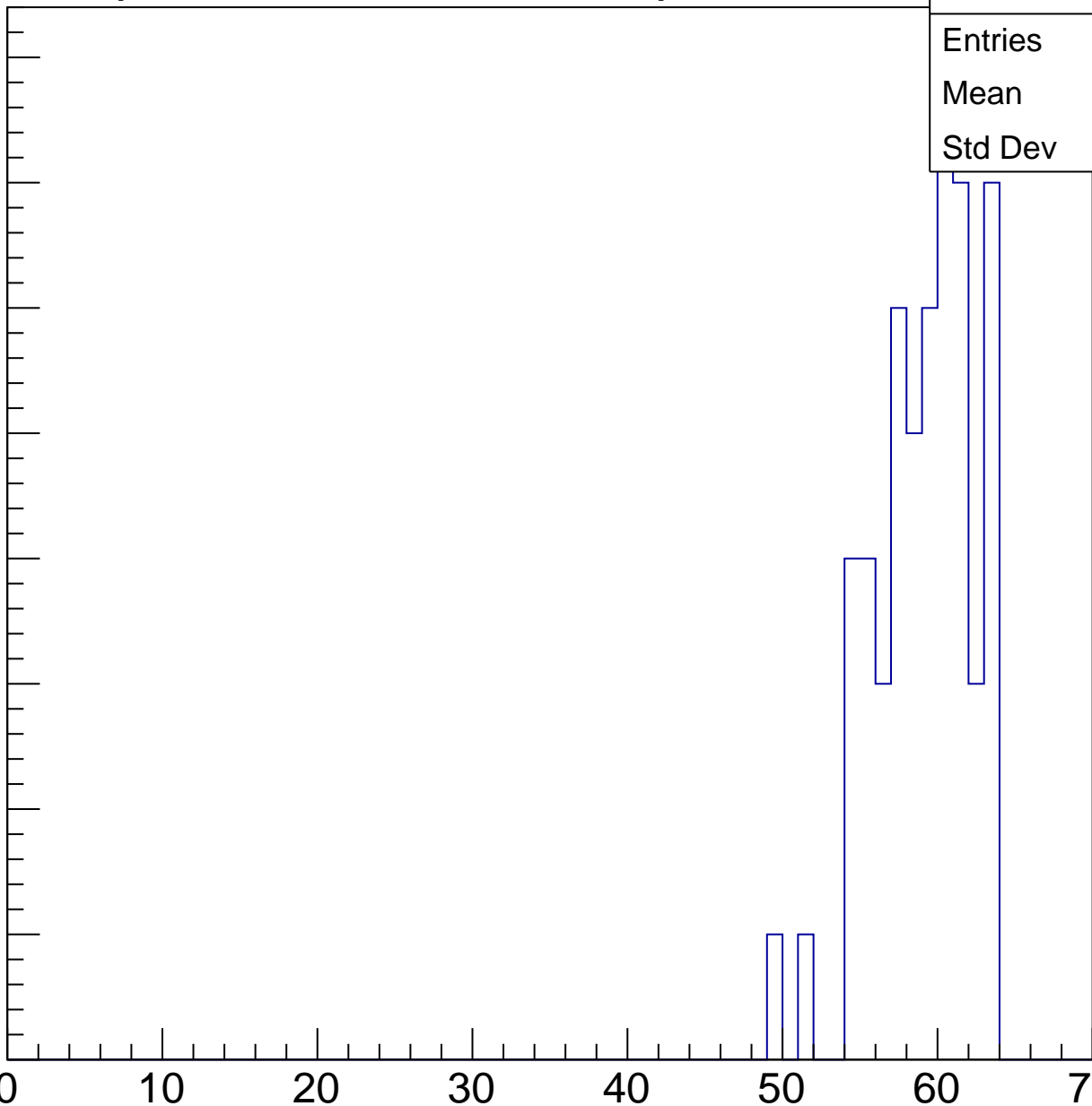
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	55
Mean	58.62
Std Dev	3.165

ampl

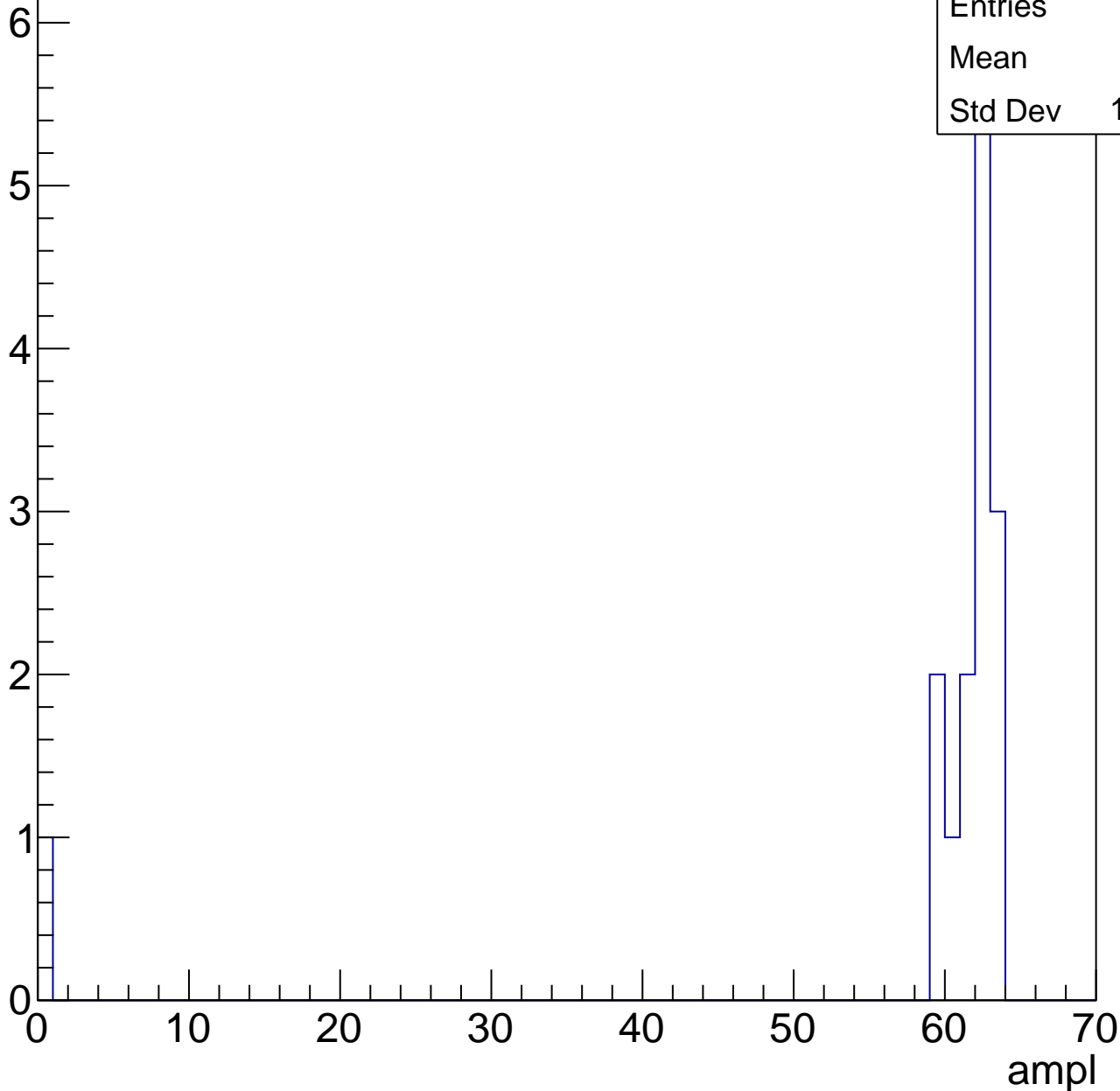


# B1L103S, U2-ch105, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	15
Mean	57.4
Std Dev	15.39

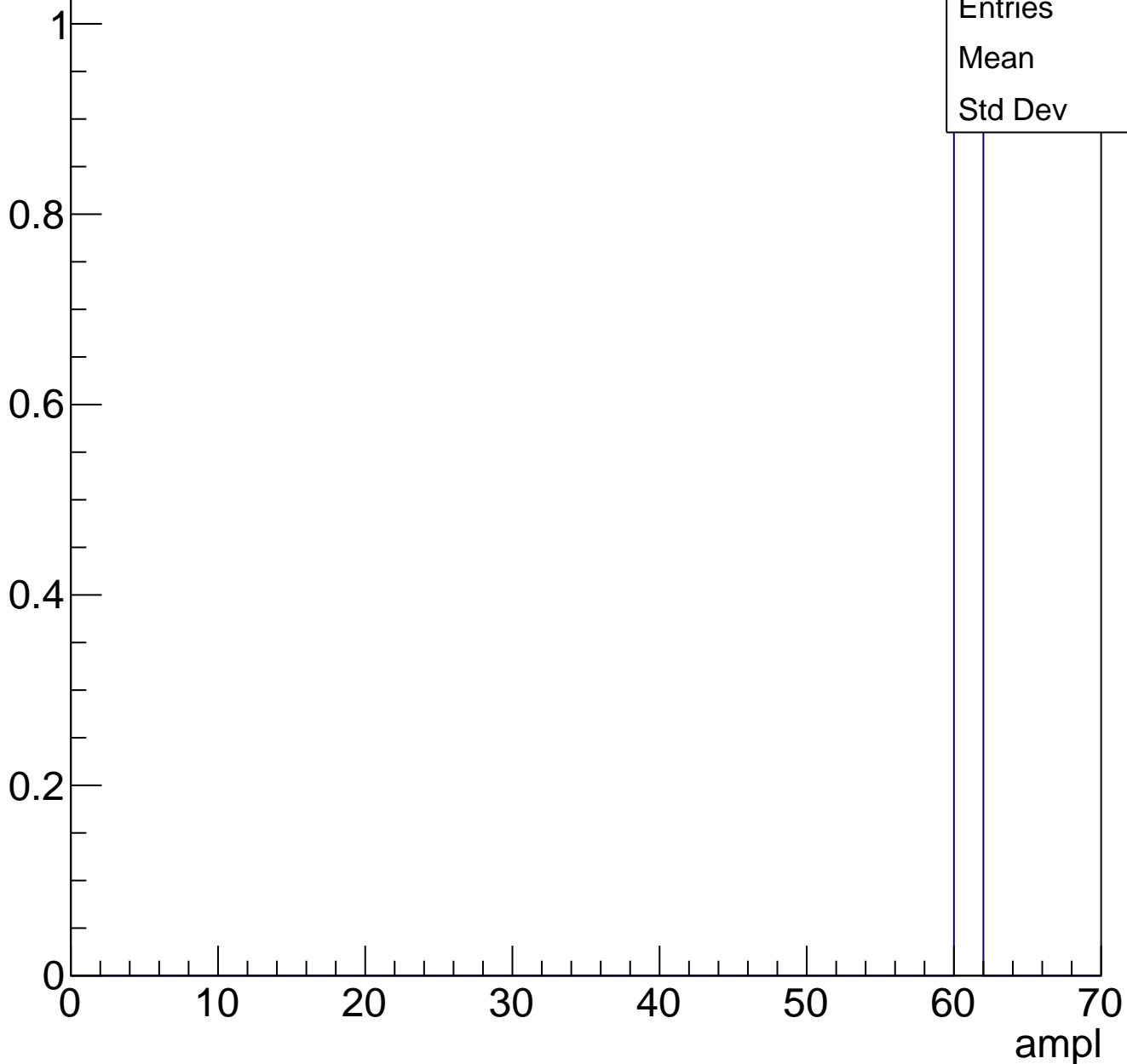




# B1L103S, U2-ch105, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch106, adc0

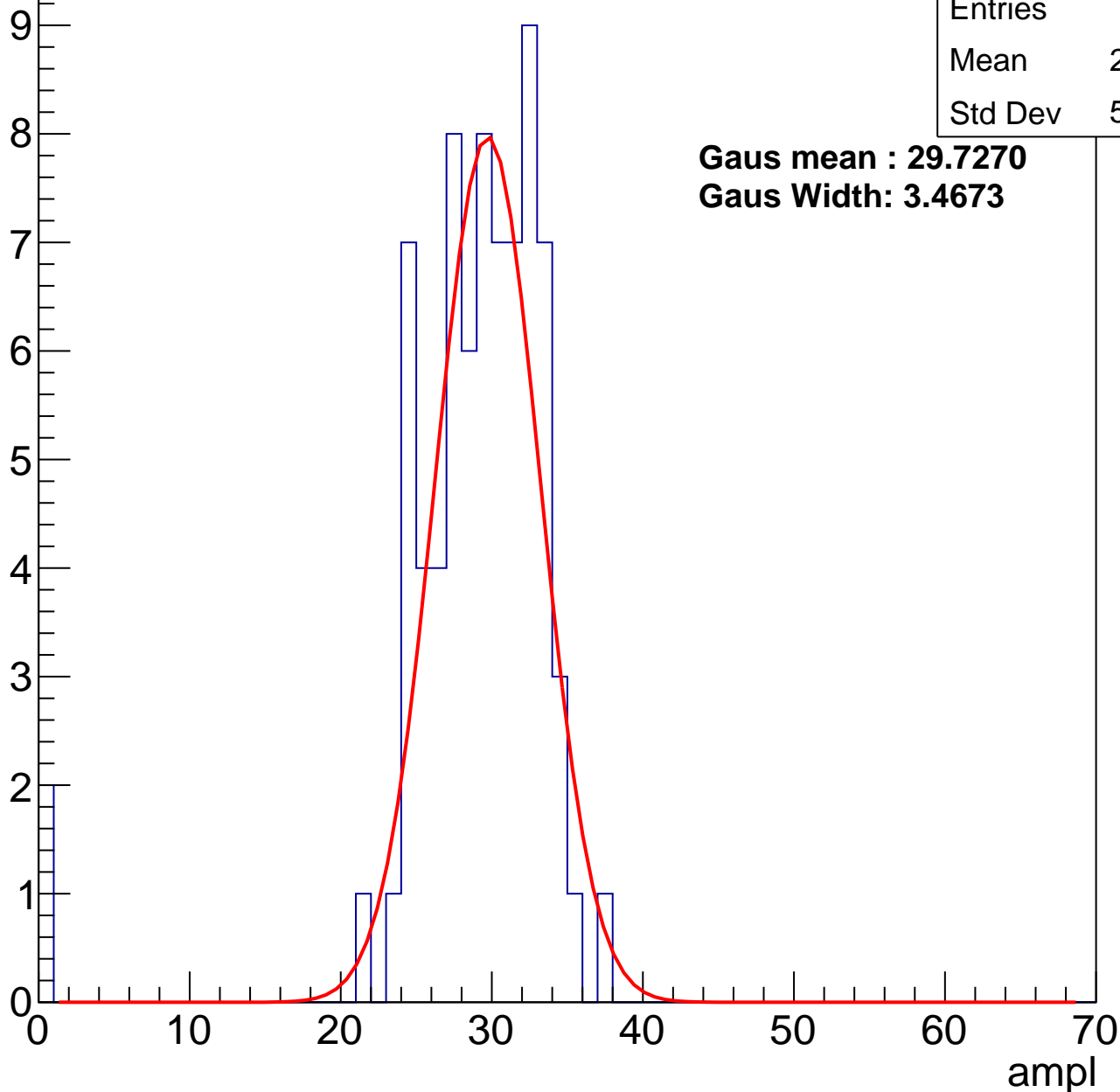
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	28.32
Std Dev	5.692

**Gaus mean : 29.7270**

**Gaus Width: 3.4673**



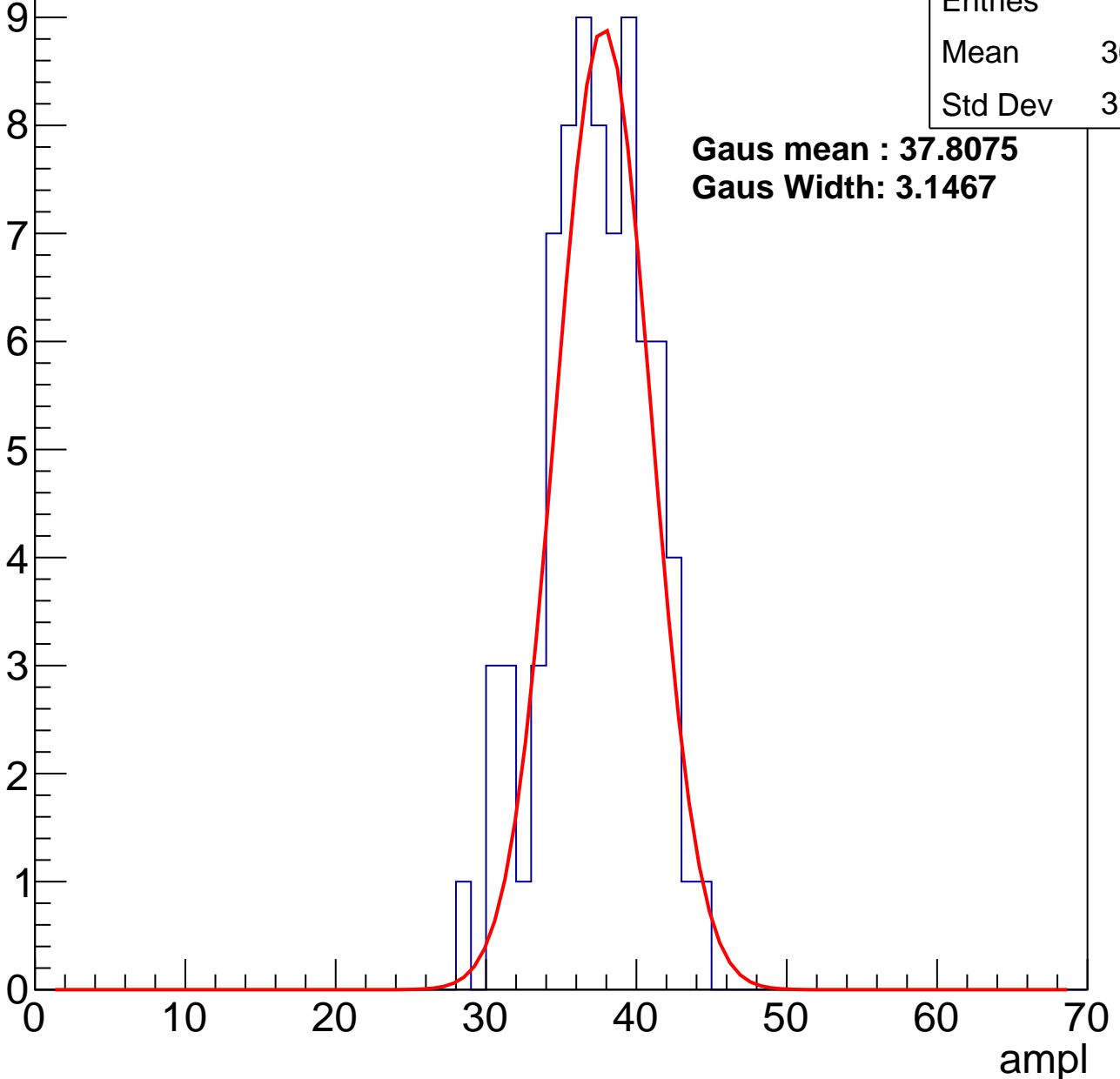
# B1L103S, U2-ch106, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	36.86
Std Dev	3.399

**Gaus mean : 37.8075**  
**Gaus Width: 3.1467**



# B1L103S, U2-ch106, adc2

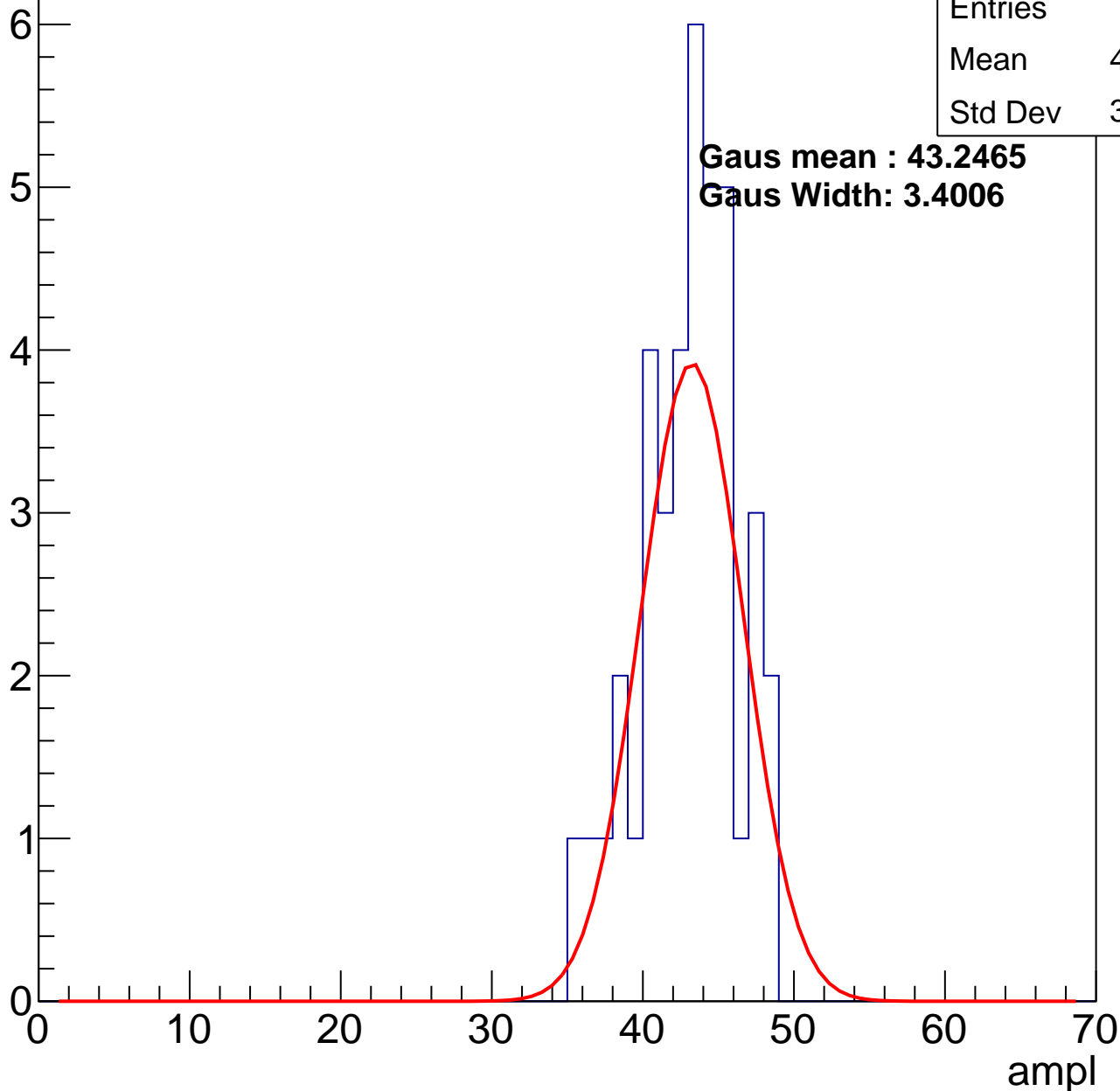
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	39
Mean	42.56
Std Dev	3.169

**Gaus mean : 43.2465**

**Gaus Width: 3.4006**

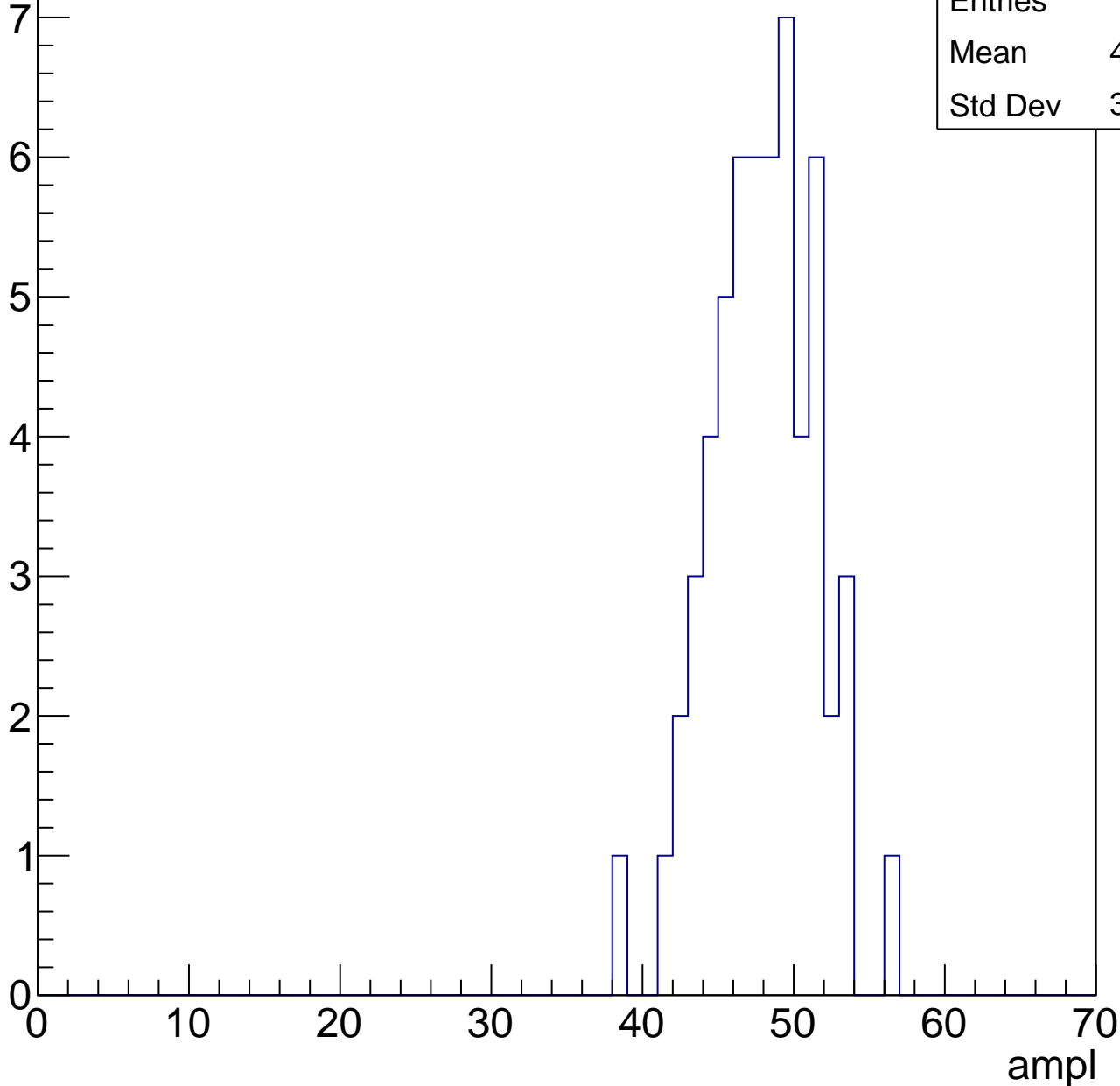


# B1L103S, U2-ch106, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	47.49
Std Dev	3.424

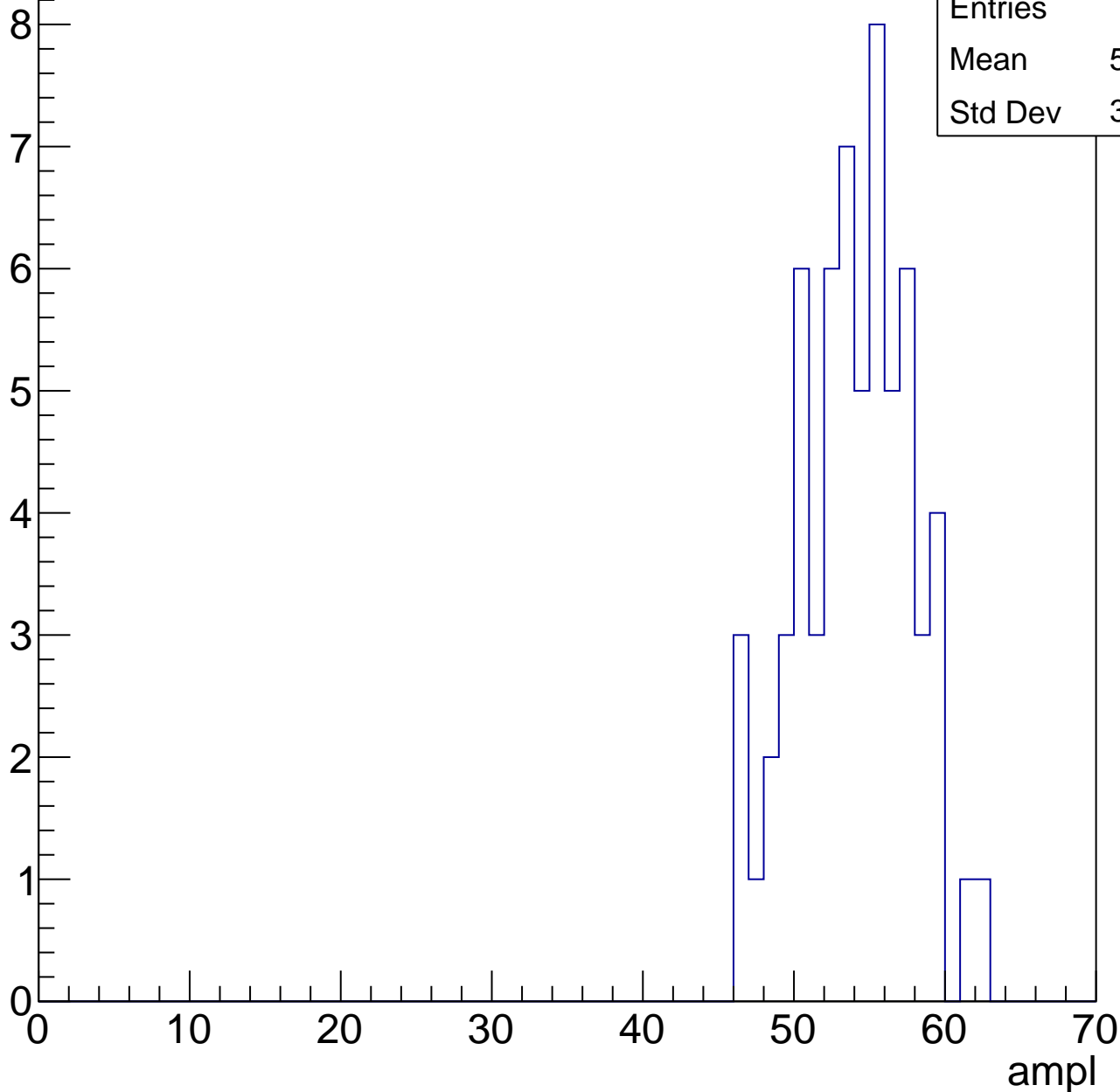


# B1L103S, U2-ch106, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	53.58
Std Dev	3.695

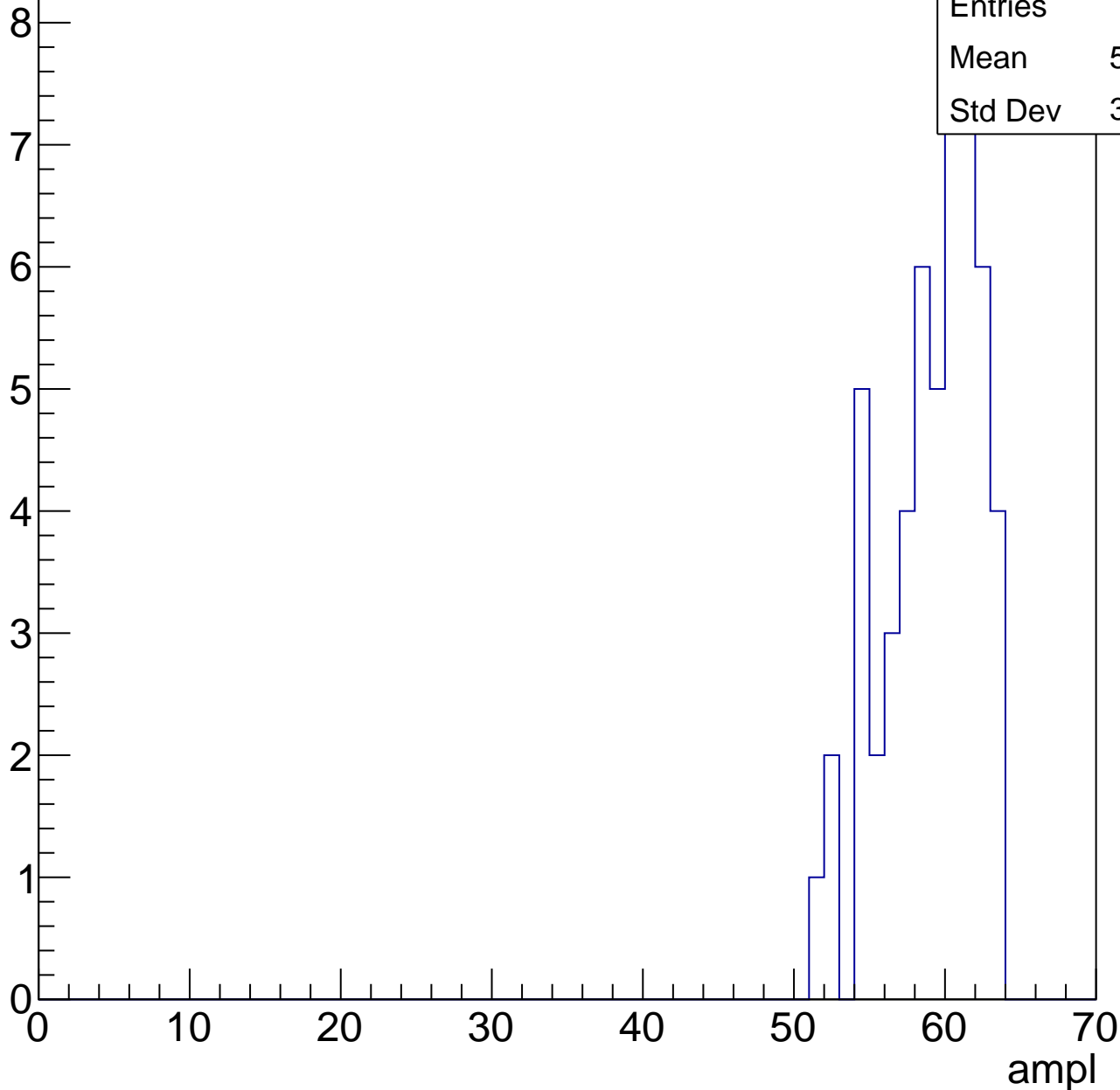


# B1L103S, U2-ch106, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	58.63
Std Dev	3.099

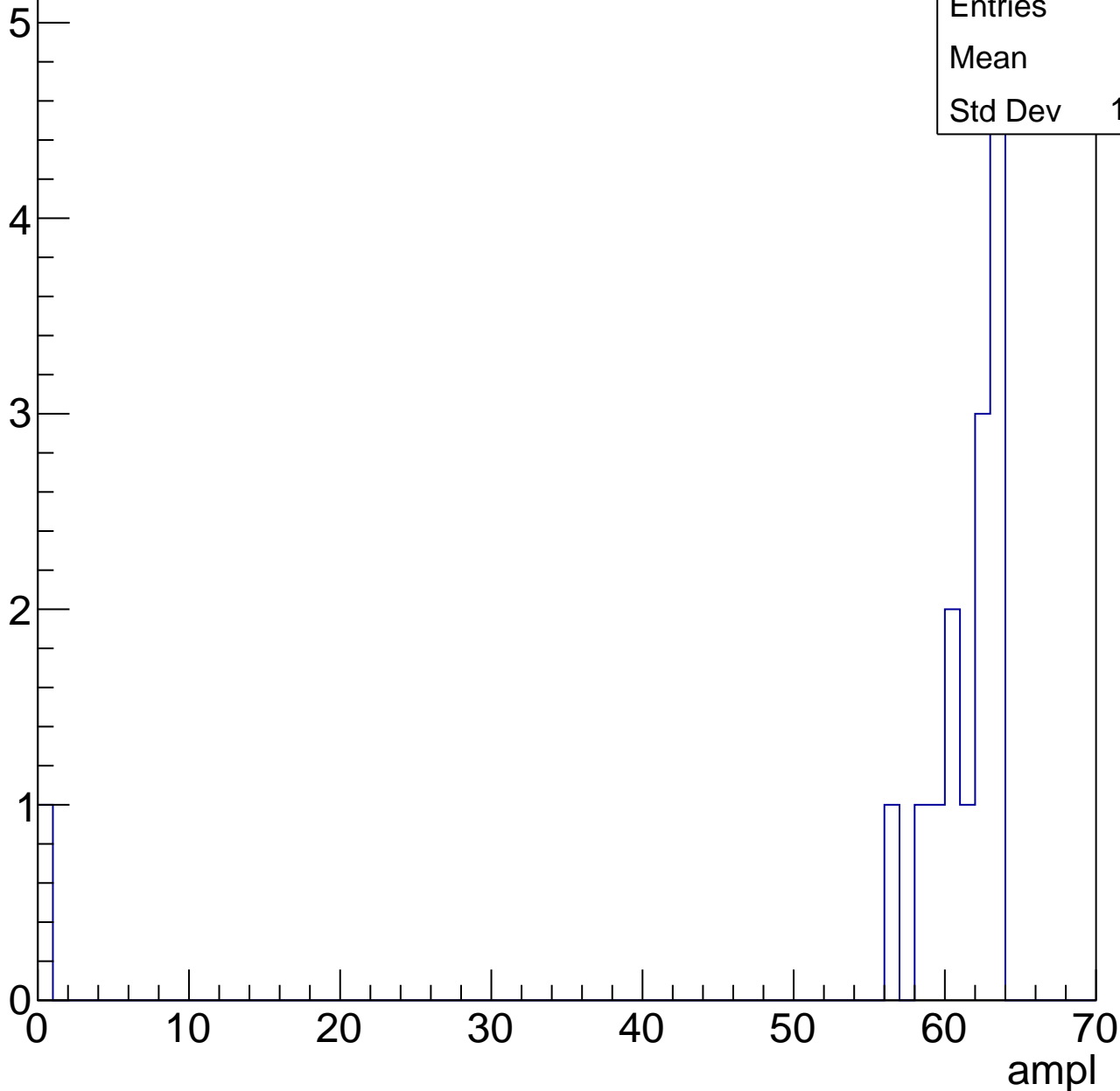


# B1L103S, U2-ch106, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	15
Mean	57
Std Dev	15.37





# B1L103S, U2-ch106, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch107, adc0

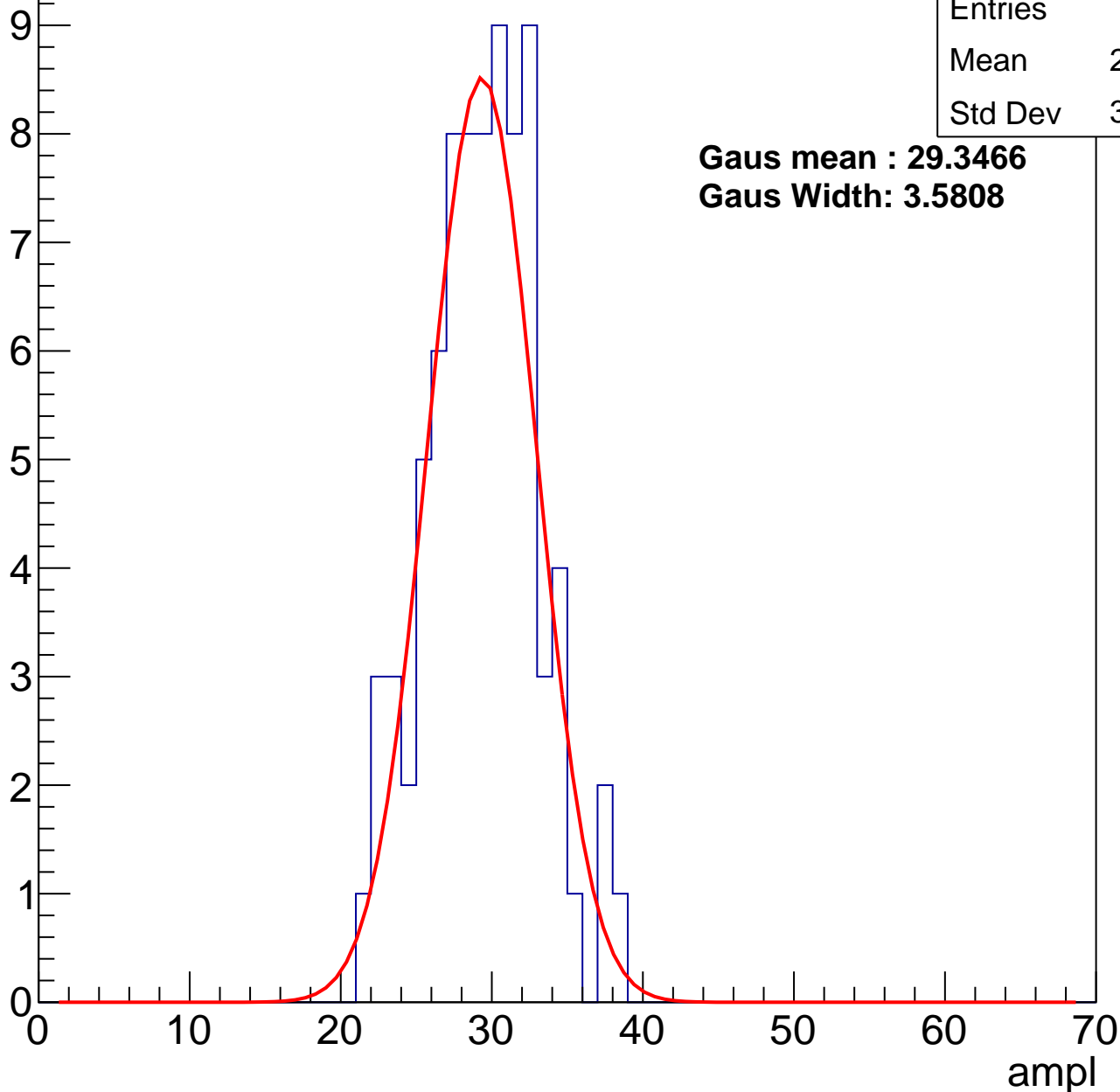
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	81
Mean	28.95
Std Dev	3.614

**Gaus mean : 29.3466**

**Gaus Width: 3.5808**



# B1L103S, U2-ch107, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	59
Mean	35.93
Std Dev	3.267

**Gaus mean : 36.4504**

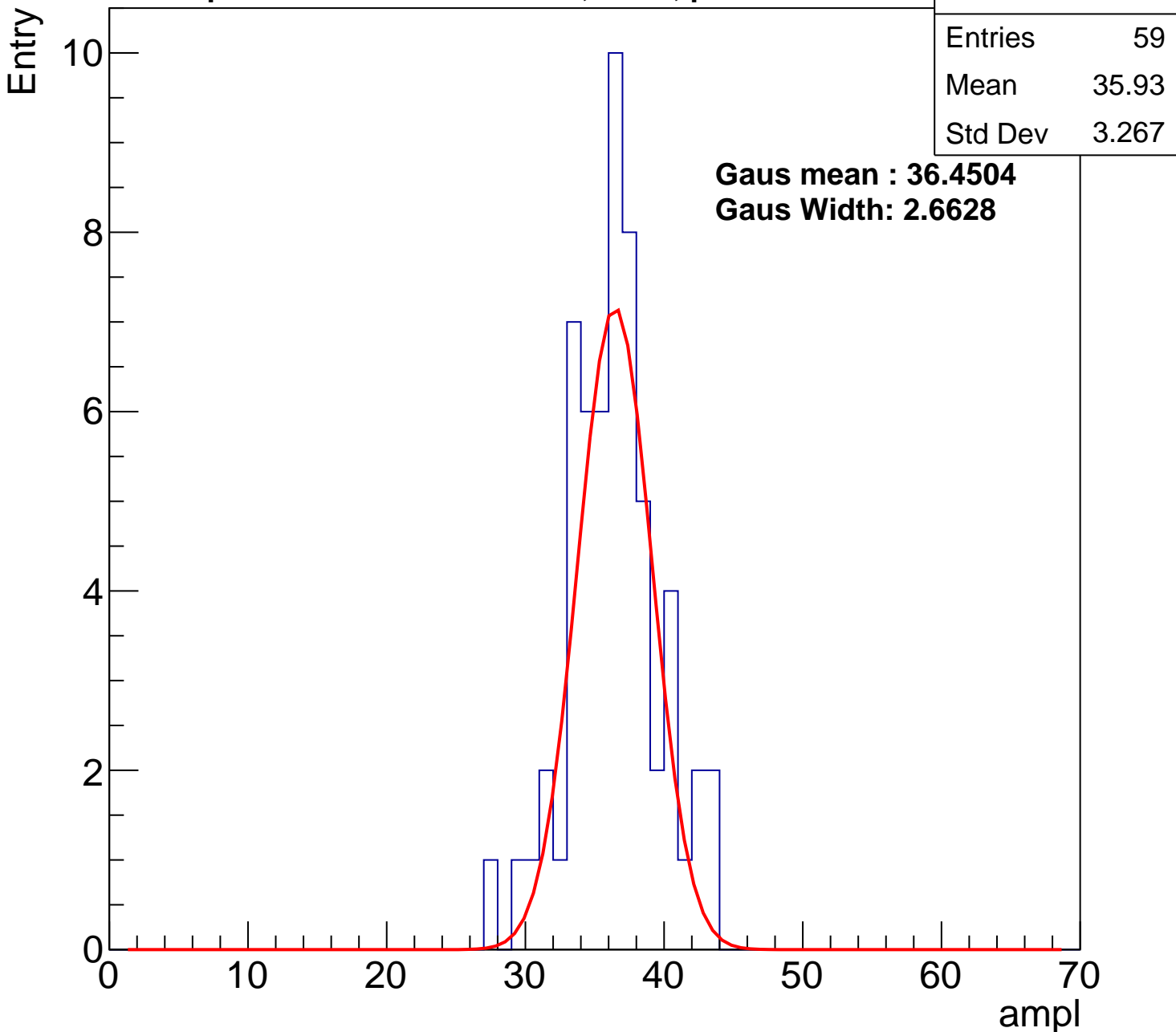
**Gaus Width: 2.6628**

Entry

10  
8  
6  
4  
2  
0

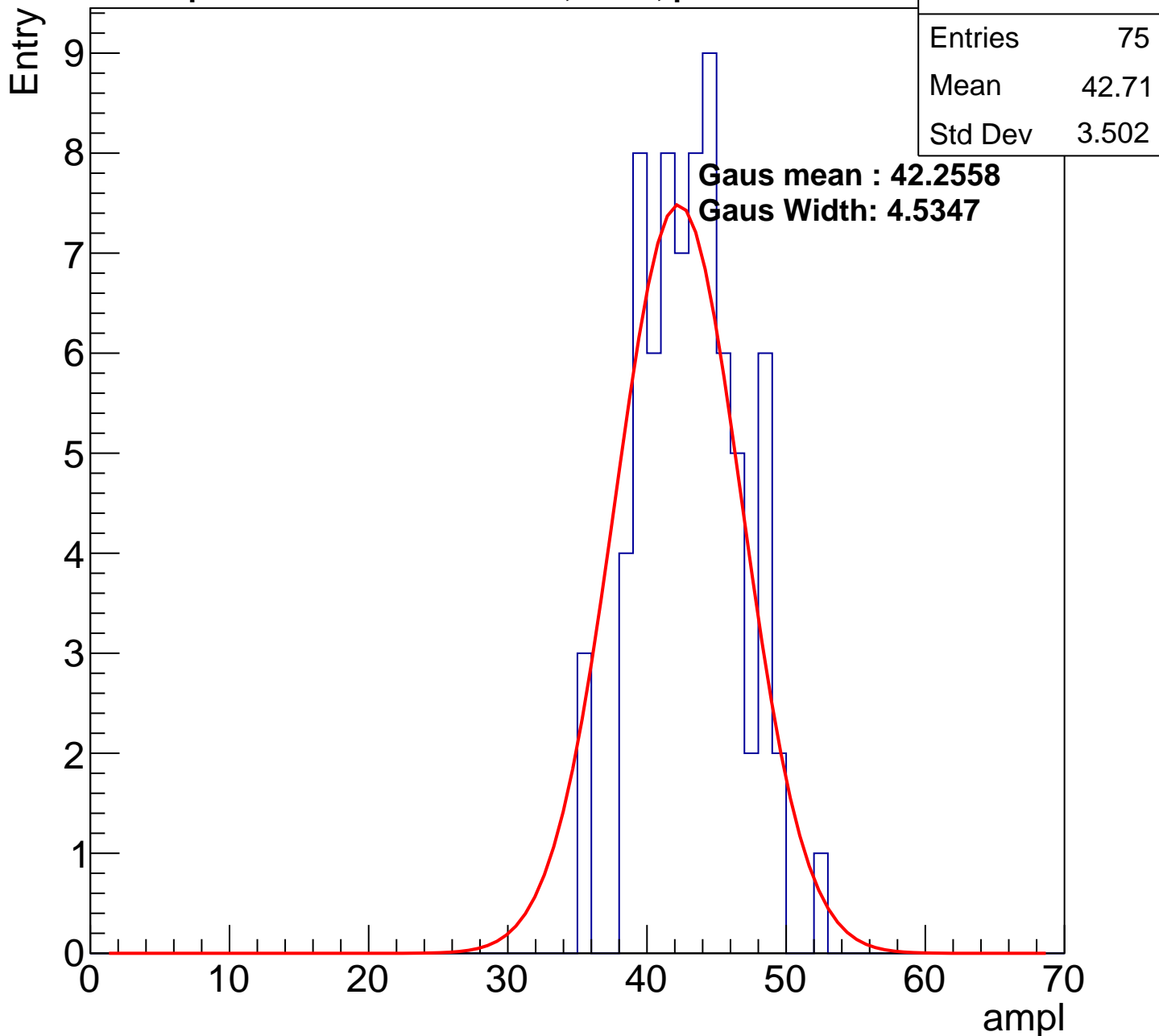
ampl

0 10 20 30 40 50 60 70



# B1L103S, U2-ch107, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

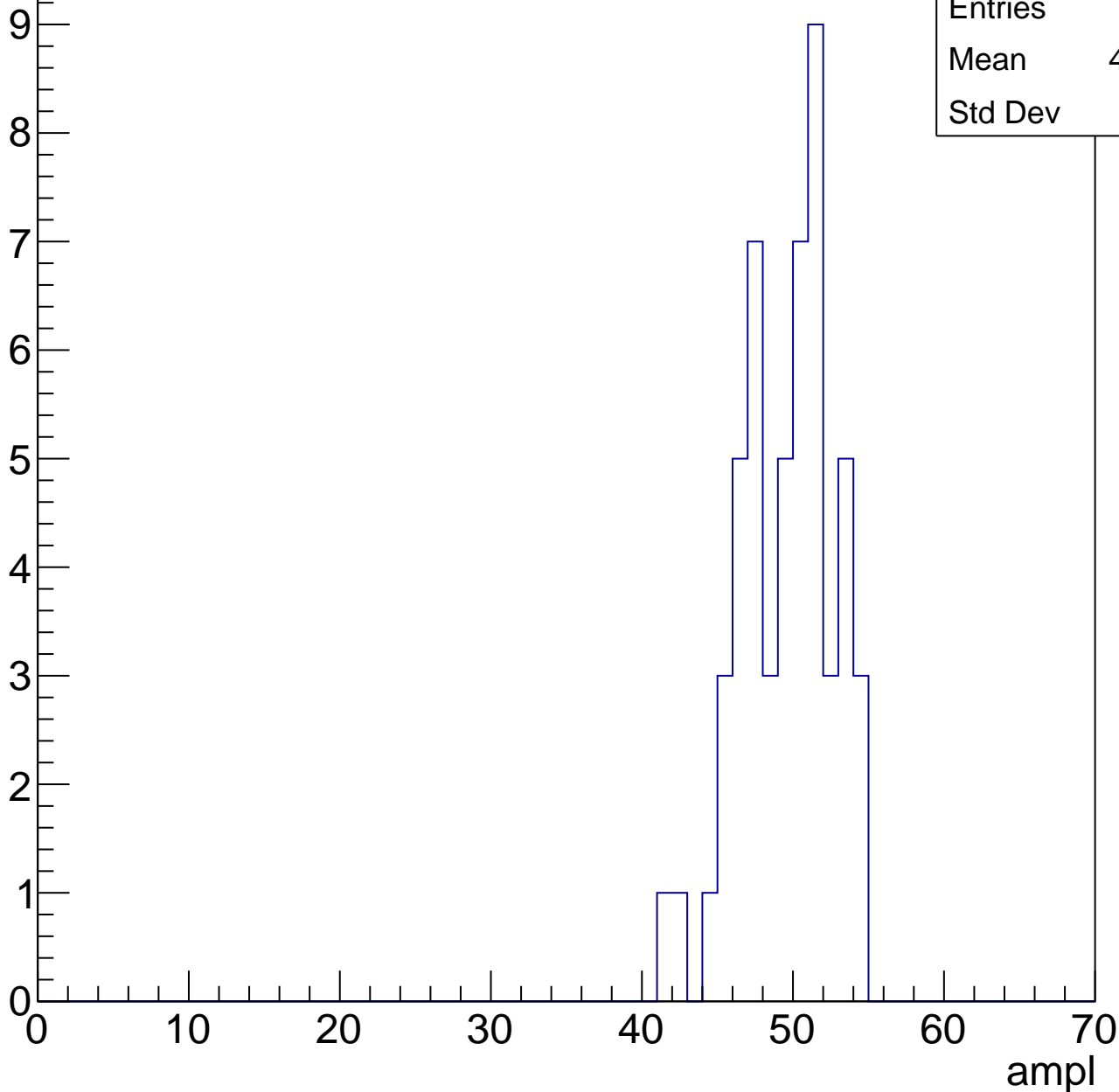


# B1L103S, U2-ch107, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	49.09
Std Dev	3.03

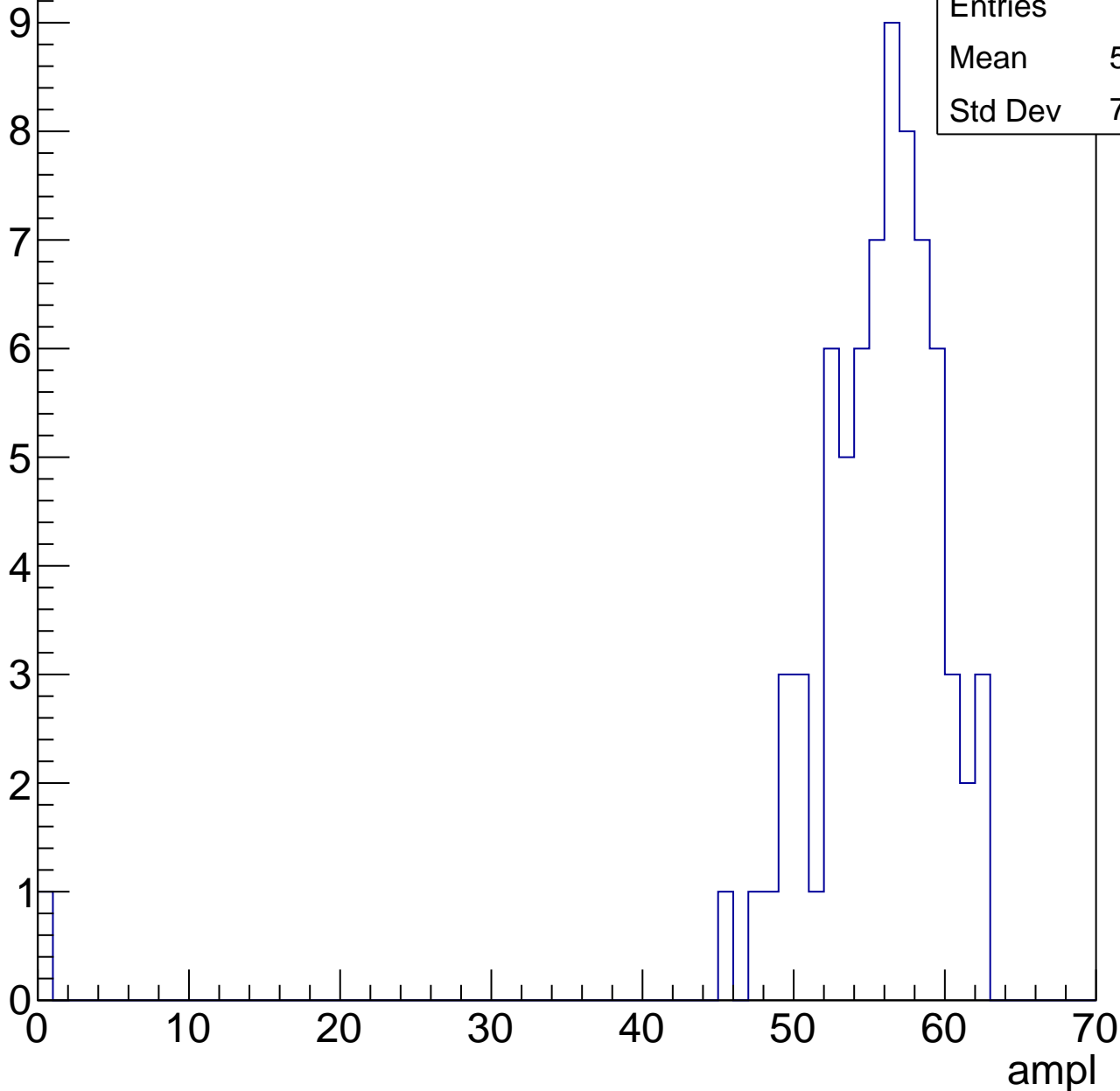


# B1L103S, U2-ch107, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	54.55
Std Dev	7.399

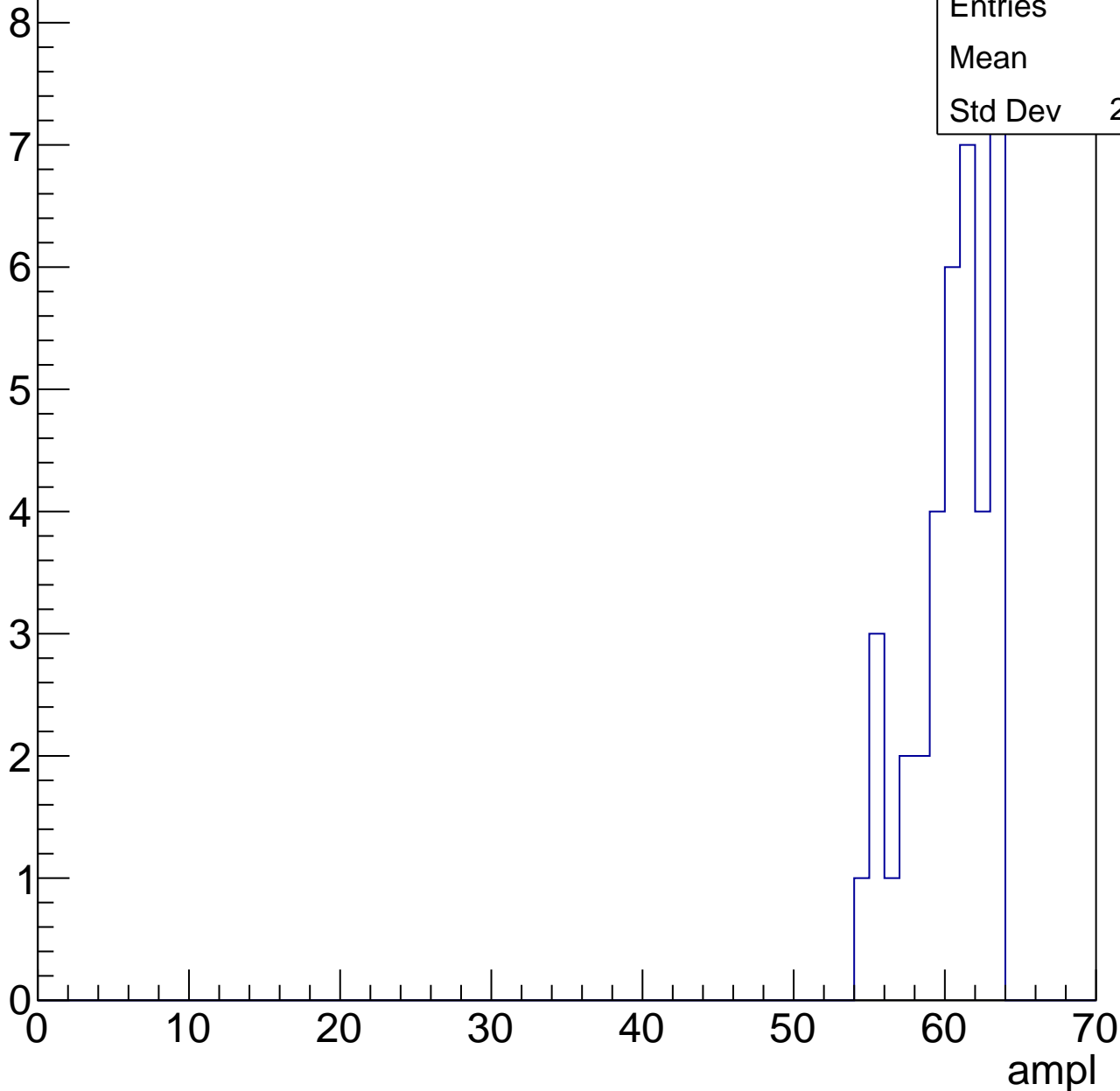


# B1L103S, U2-ch107, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

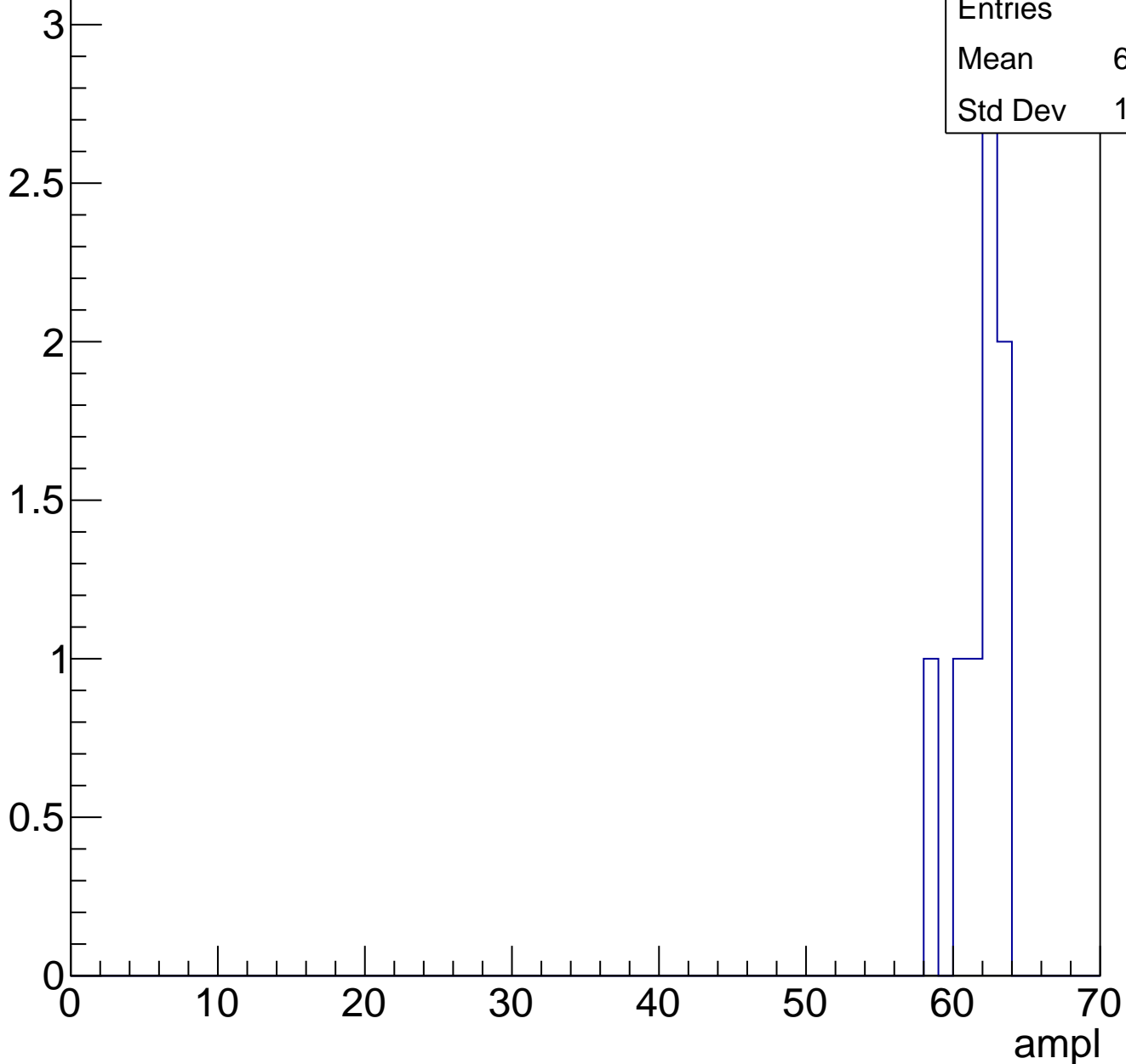
Entries	38
Mean	60
Std Dev	2.575



# B1L103S, U2-ch107, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U2-ch107, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch108, adc0

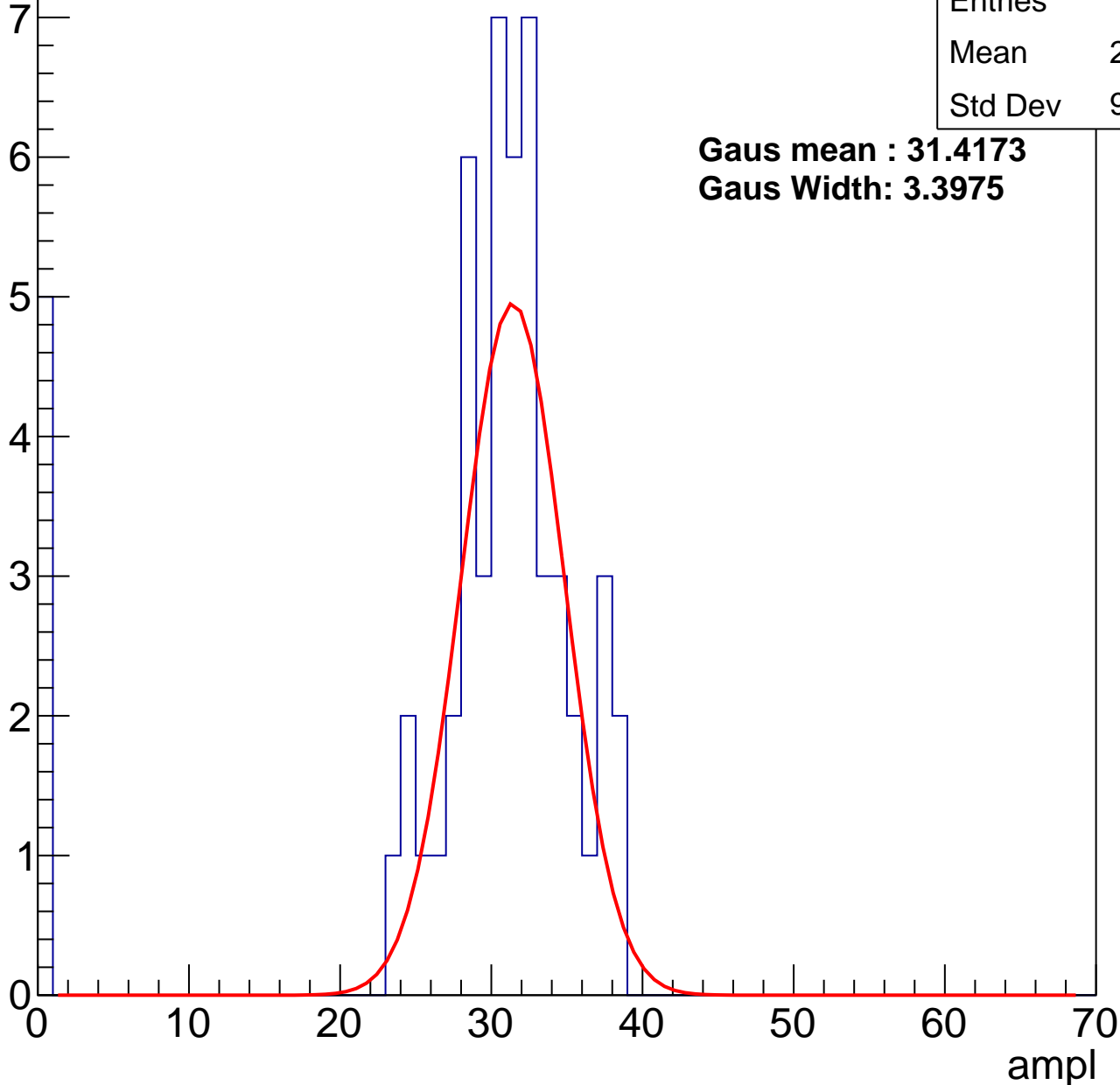
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	28.09
Std Dev	9.512

**Gaus mean : 31.4173**

**Gaus Width: 3.3975**



# B1L103S, U2-ch108, adc1

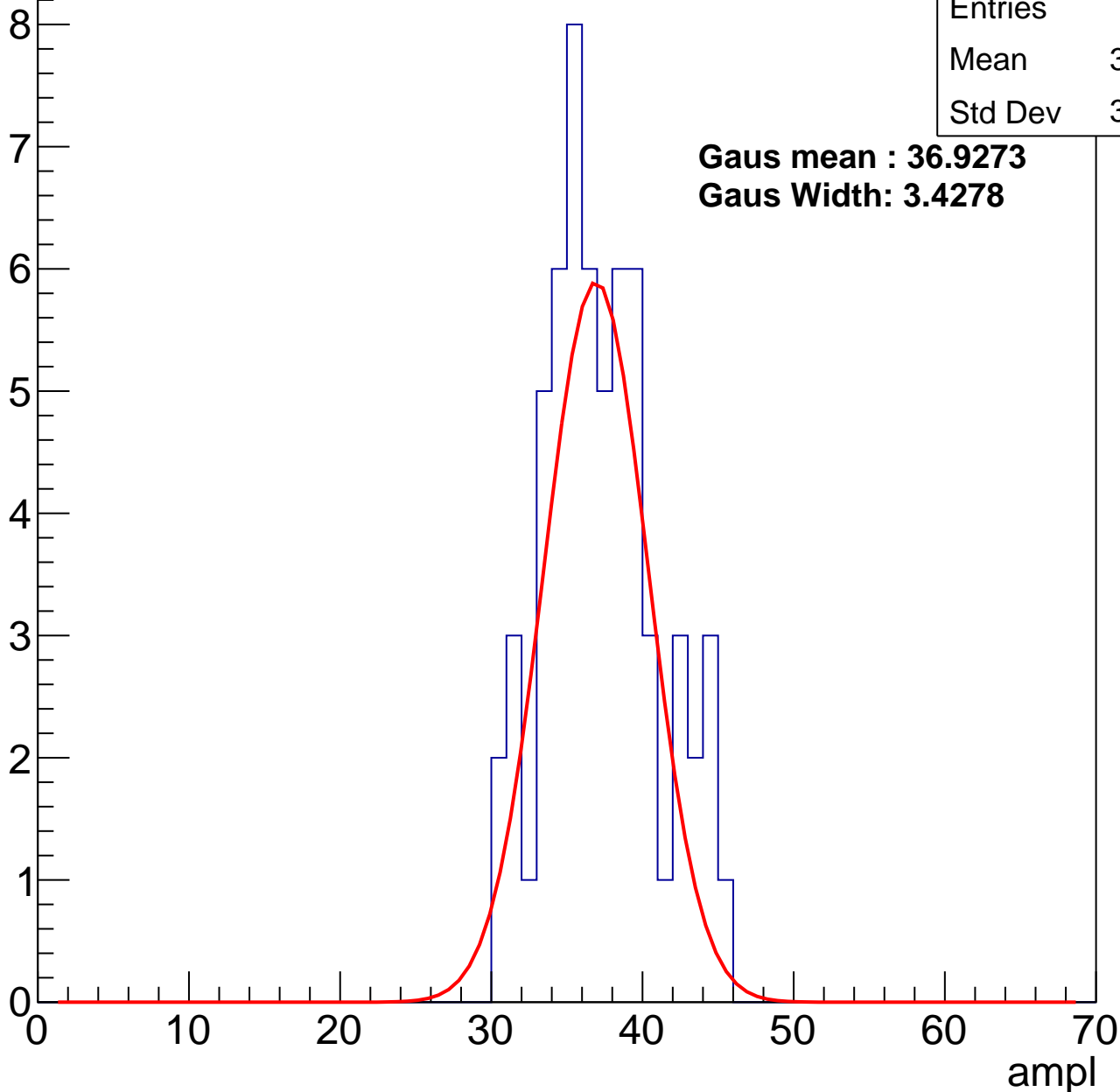
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	36.84
Std Dev	3.694

**Gaus mean : 36.9273**

**Gaus Width: 3.4278**



# B1L103S, U2-ch108, adc2

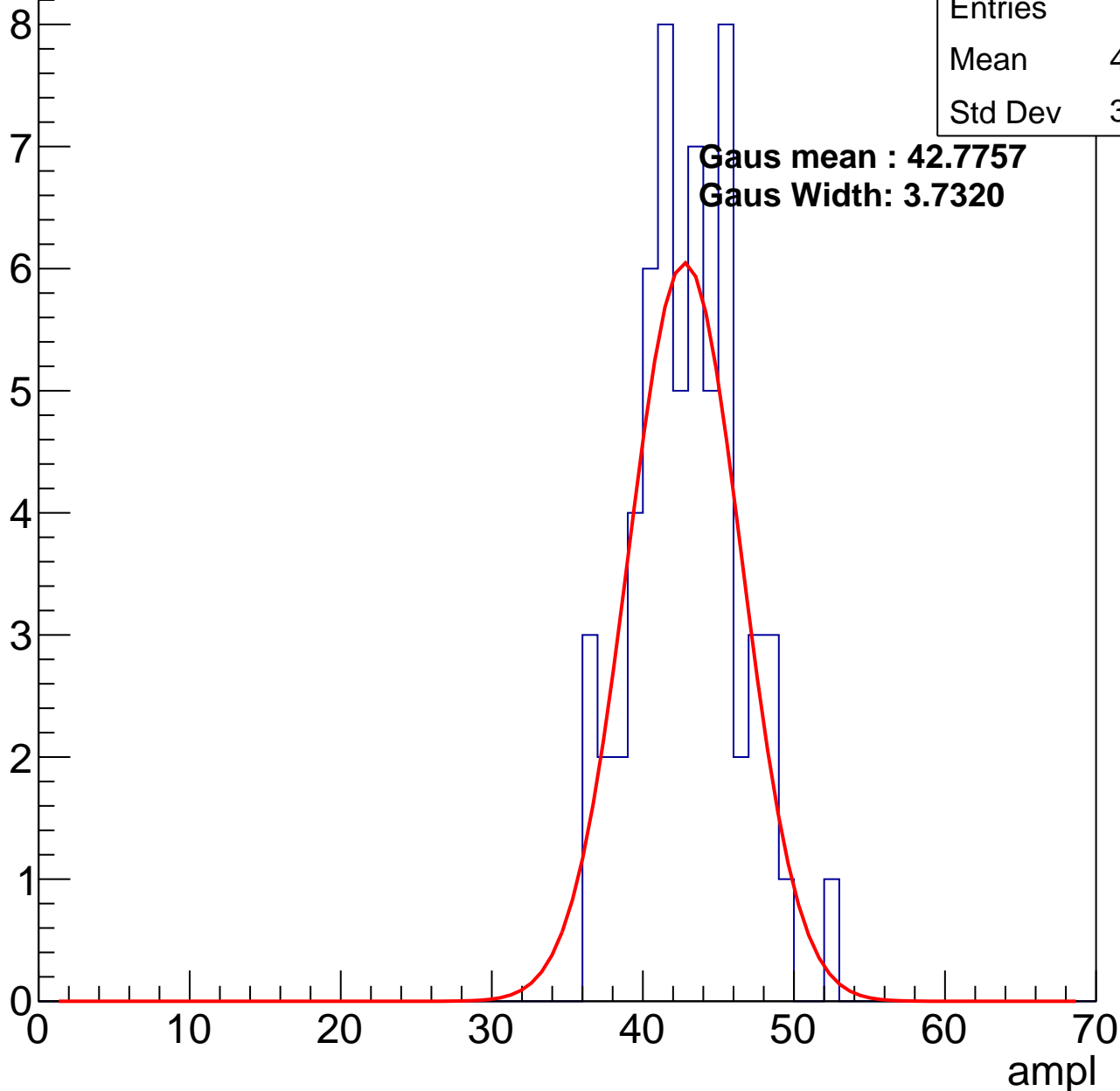
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	42.52
Std Dev	3.428

**Gaus mean : 42.7757**

**Gaus Width: 3.7320**

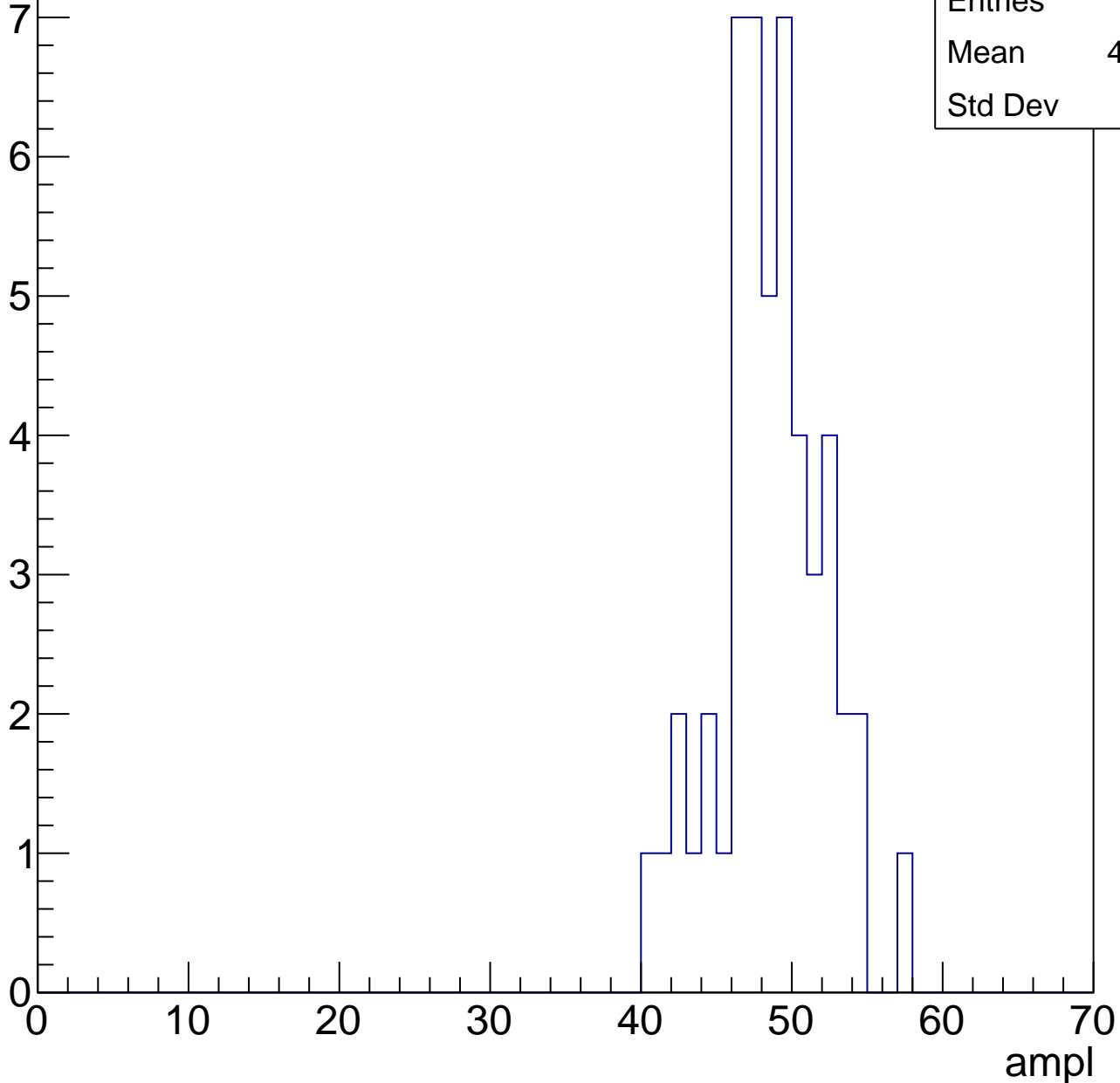


# B1L103S, U2-ch108, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	48.14
Std Dev	3.47

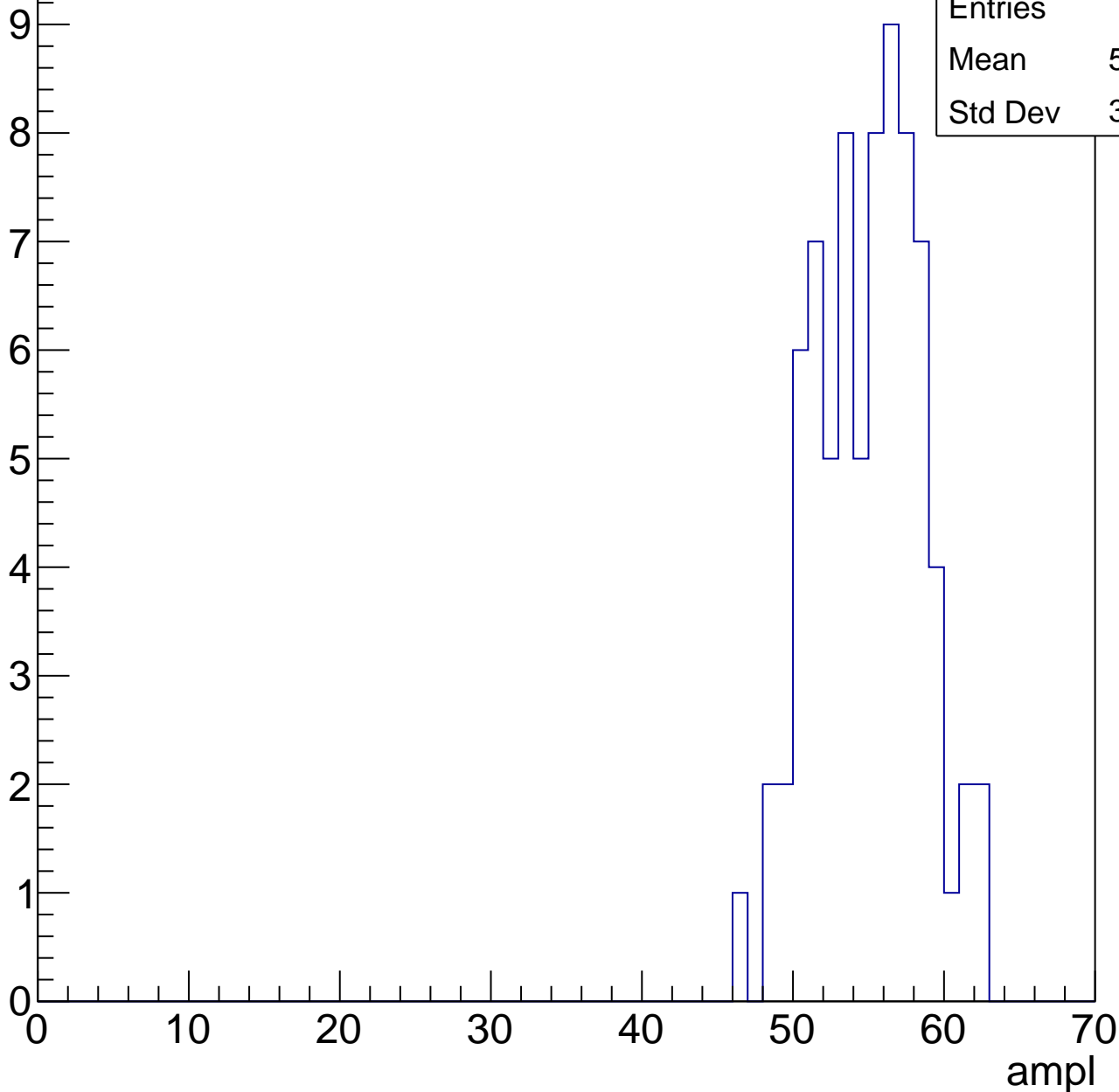


# B1L103S, U2-ch108, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

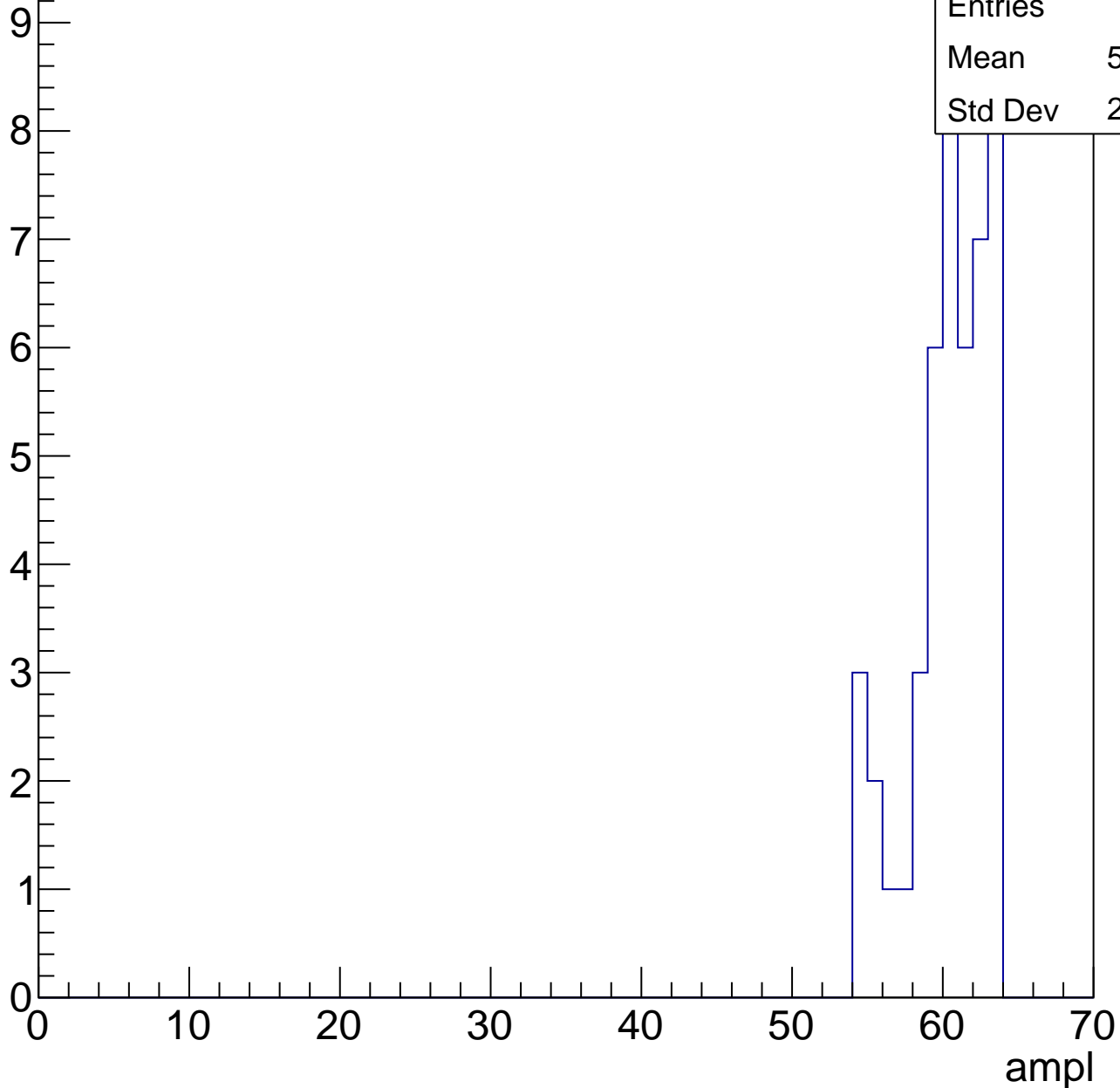
Entries	77
Mean	54.53
Std Dev	3.496



# B1L103S, U2-ch108, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch108, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

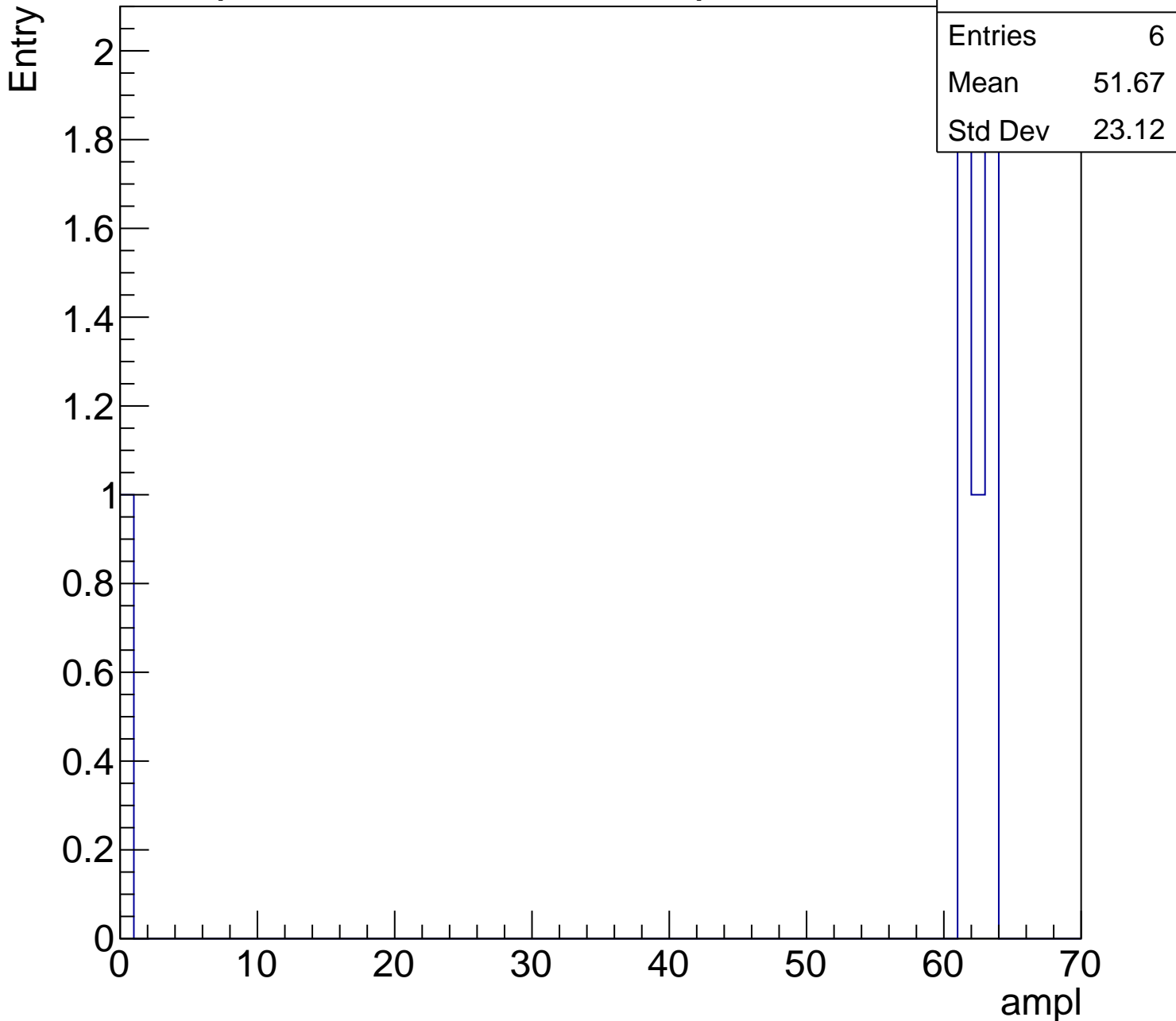
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	51.67
Std Dev	23.12

0 10 20 30 40 50 60 70

ampl





# B1L103S, U2-ch108, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U2-ch109, adc0

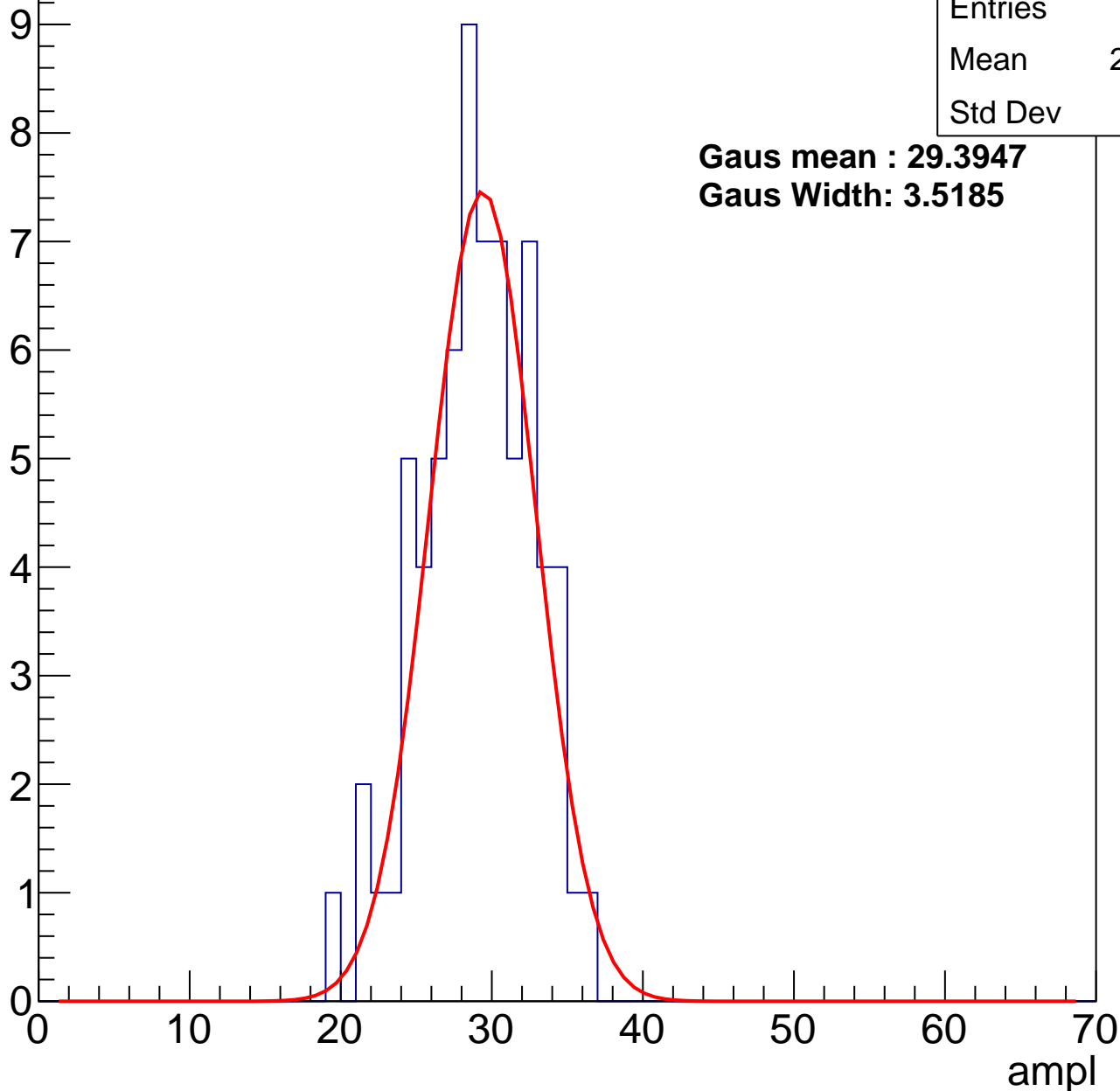
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	28.59
Std Dev	3.6

**Gaus mean : 29.3947**

**Gaus Width: 3.5185**



# B1L103S, U2-ch109, adc1

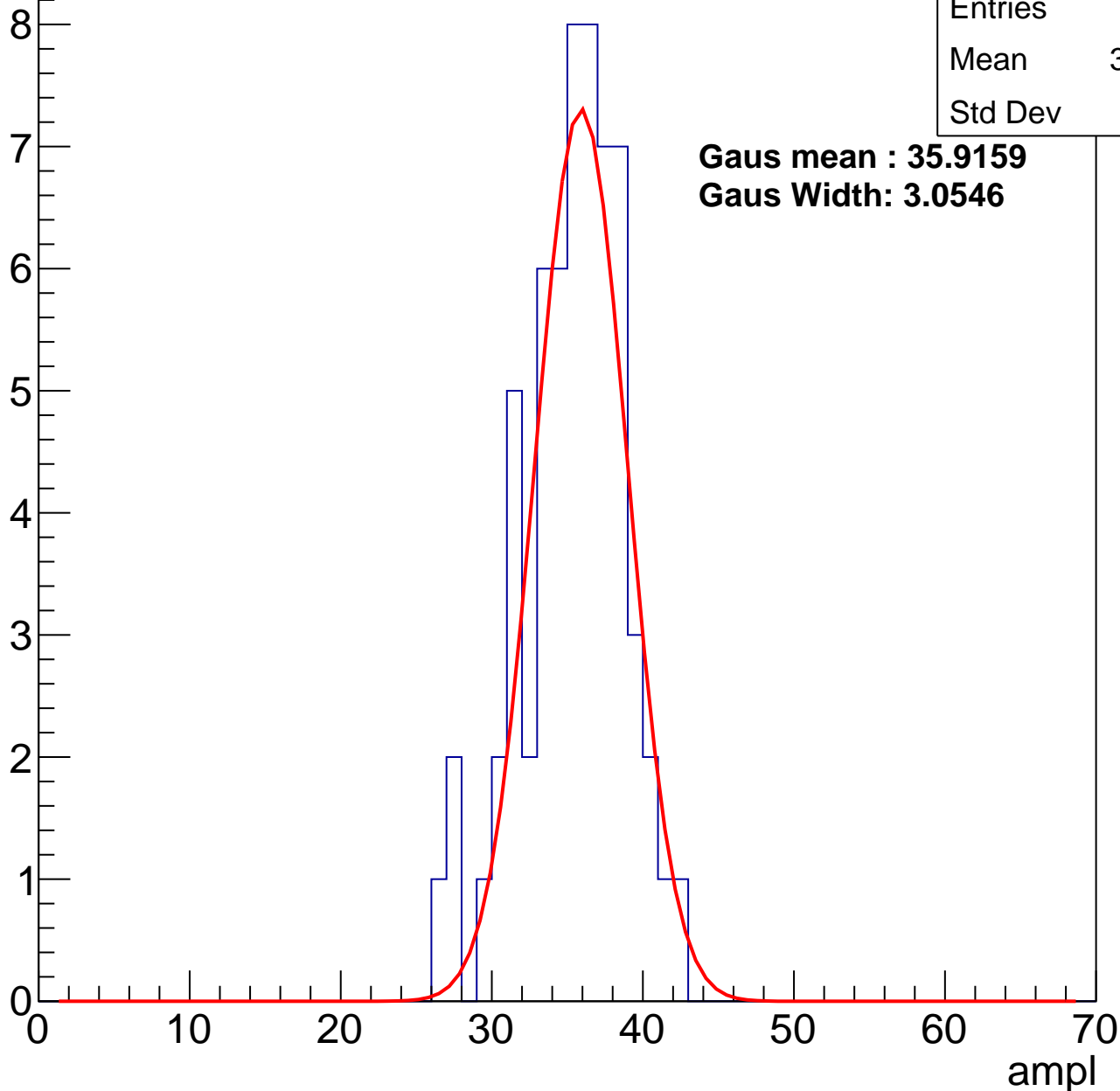
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	34.89
Std Dev	3.37

**Gaus mean : 35.9159**

**Gaus Width: 3.0546**



# B1L103S, U2-ch109, adc2

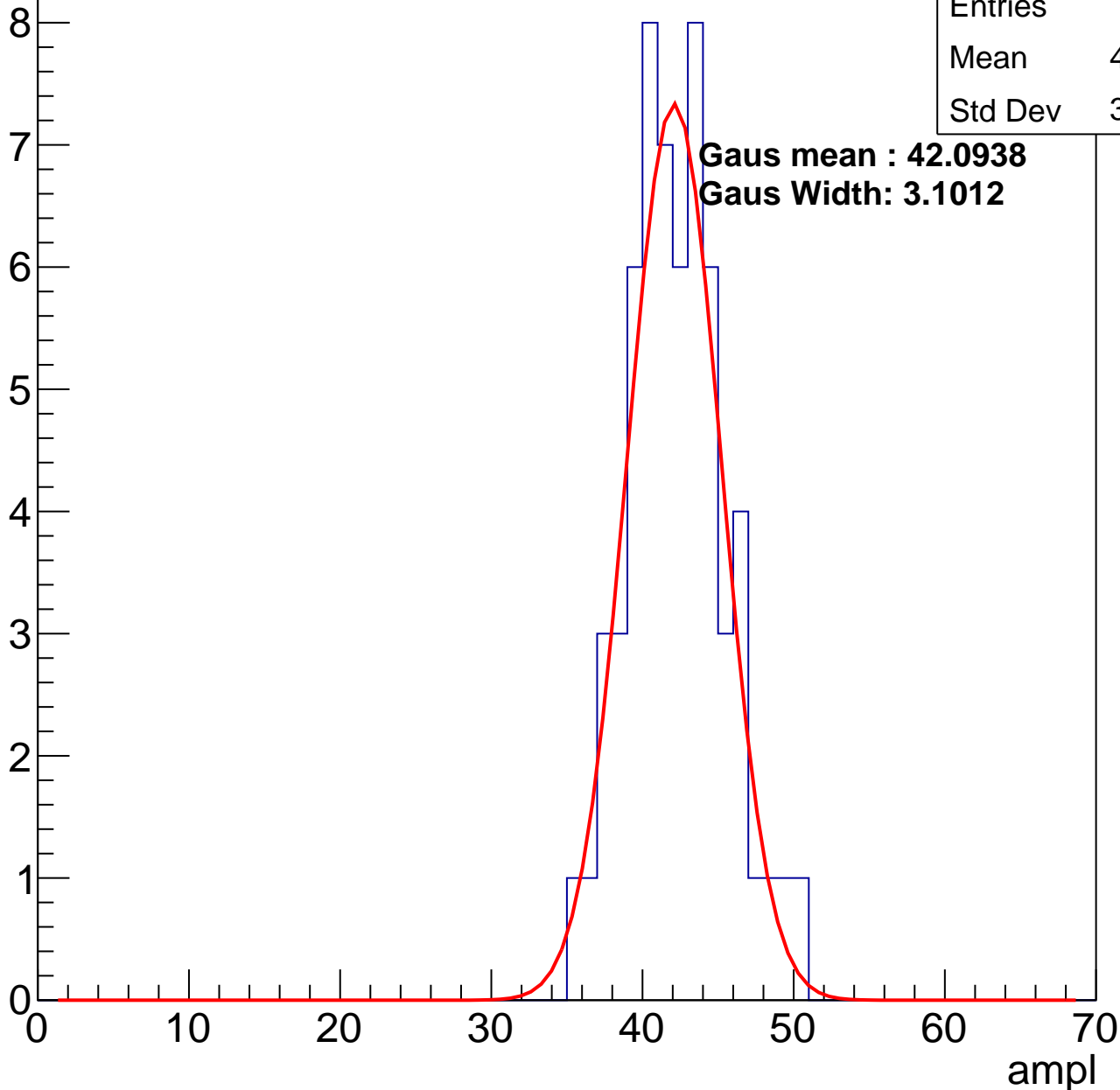
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	41.83
Std Dev	3.153

**Gaus mean : 42.0938**

**Gaus Width: 3.1012**

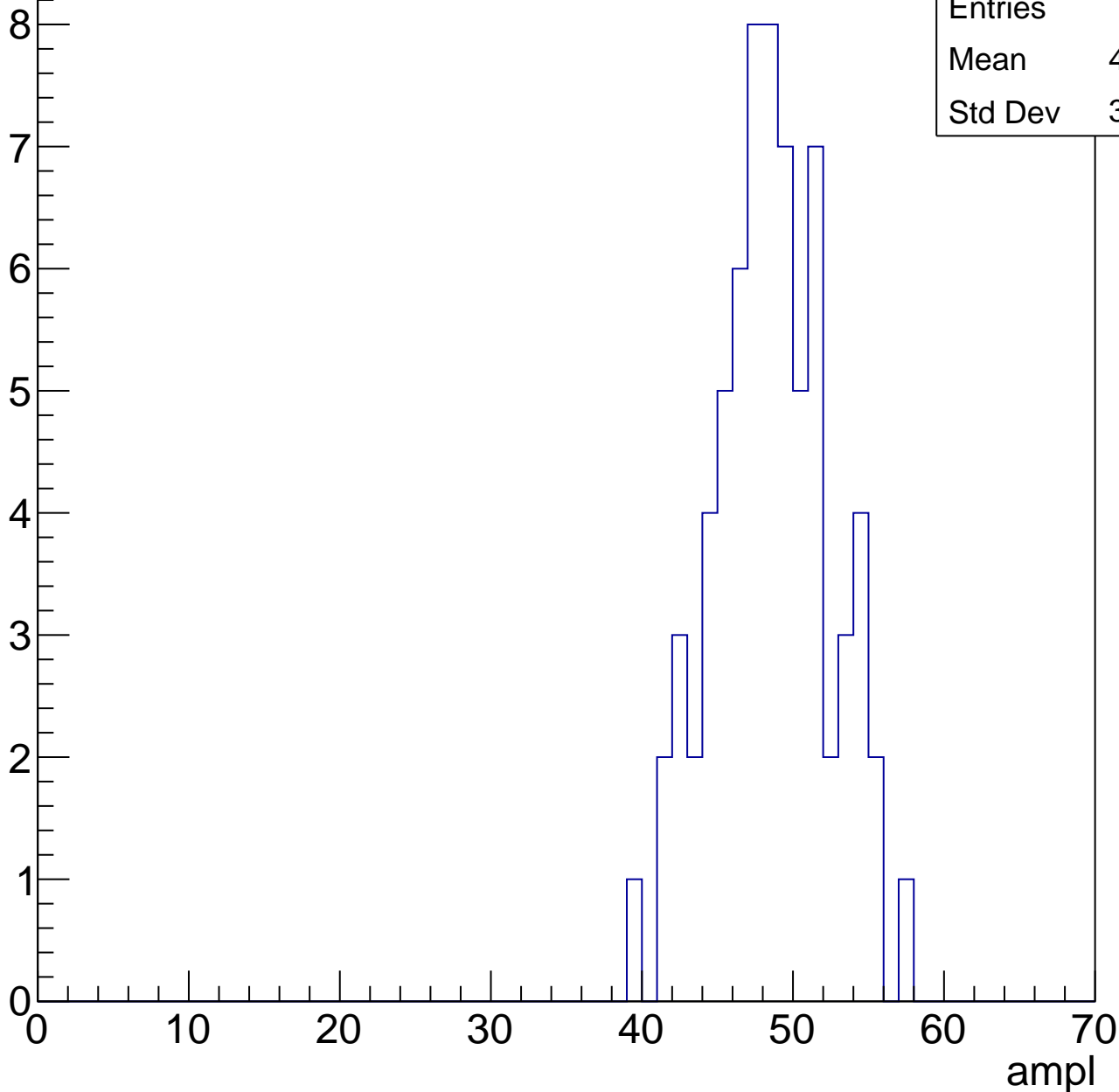


# B1L103S, U2-ch109, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	48.09
Std Dev	3.775

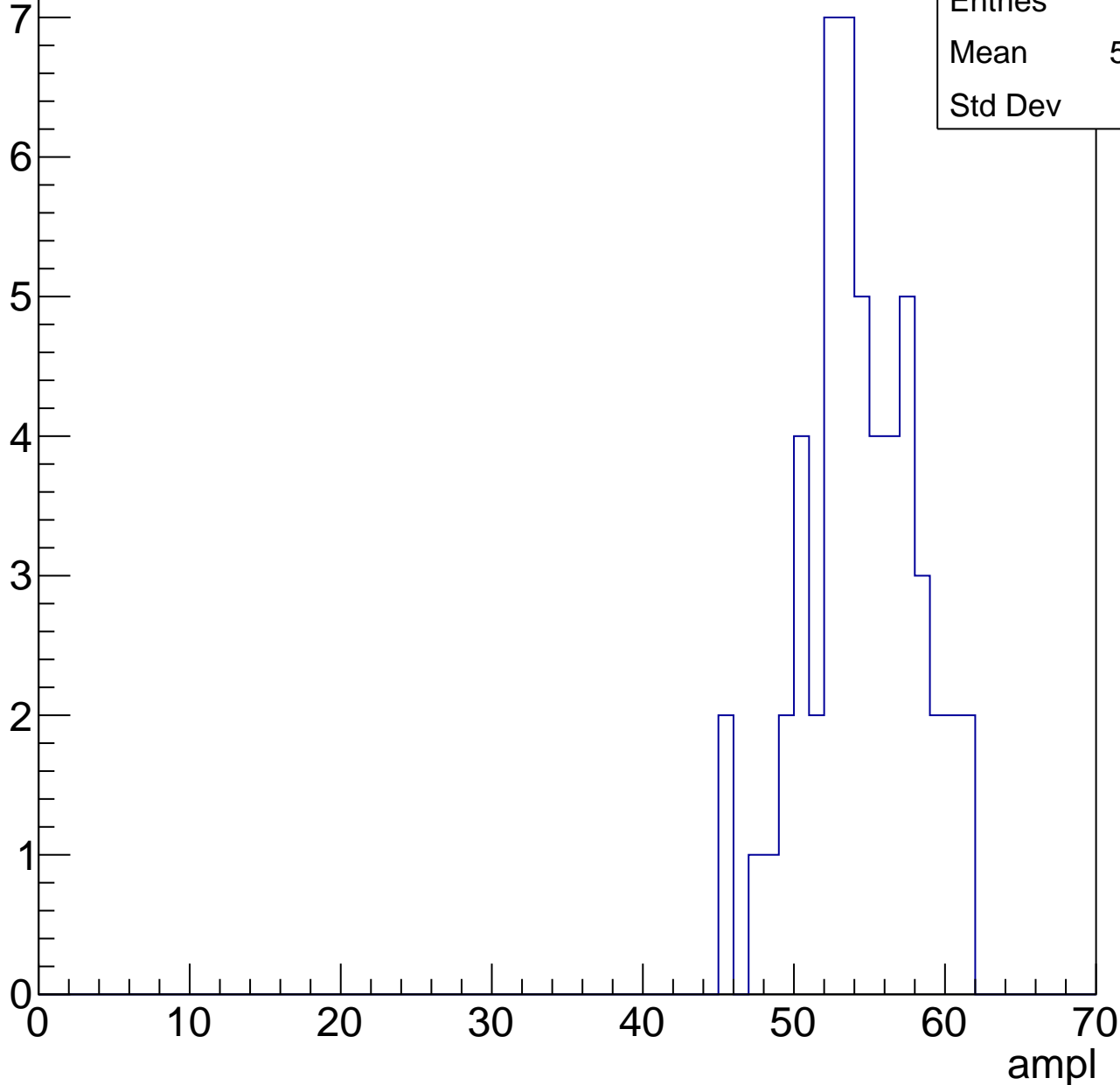


# B1L103S, U2-ch109, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	53.83
Std Dev	3.75

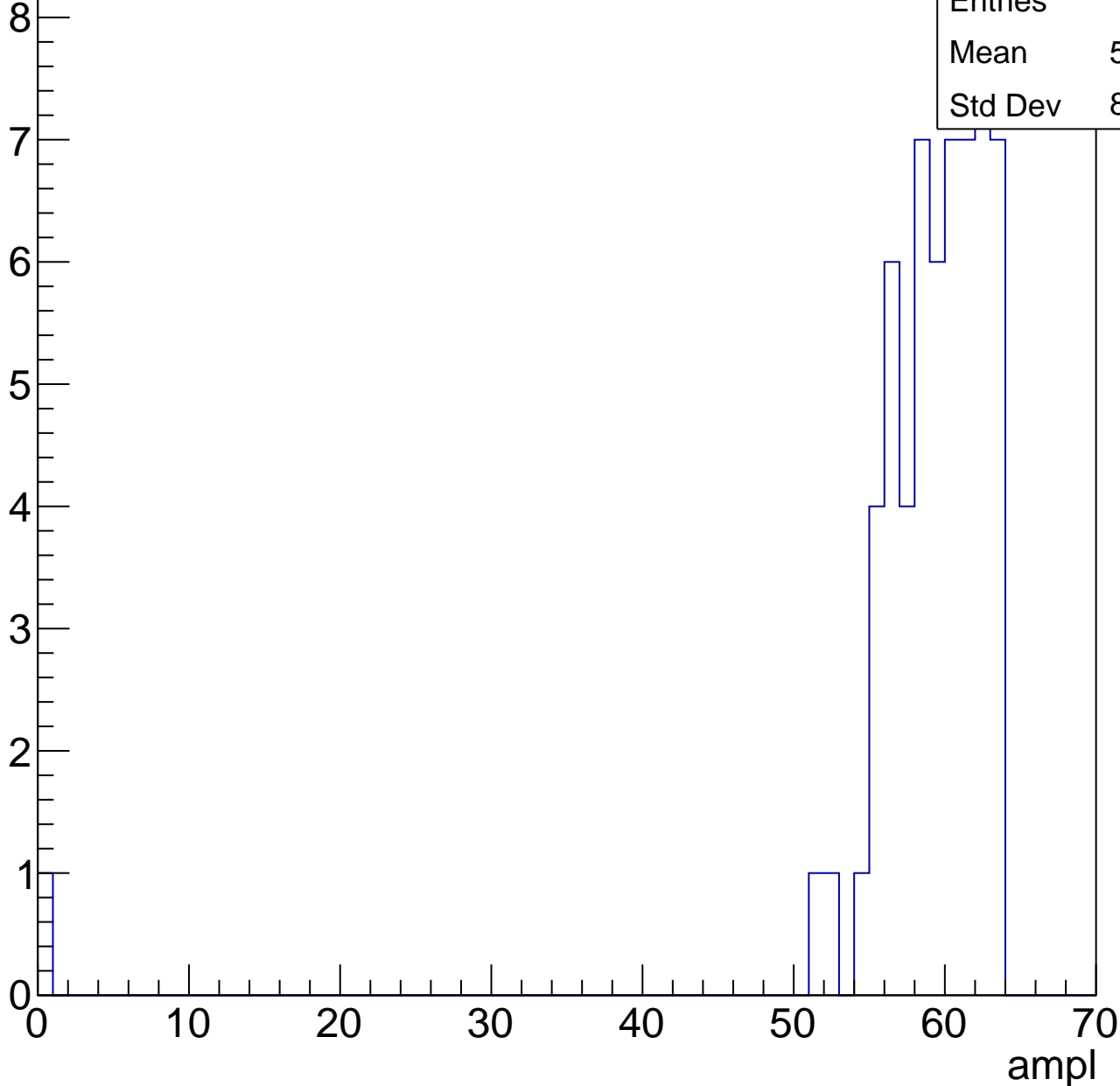


# B1L103S, U2-ch109, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

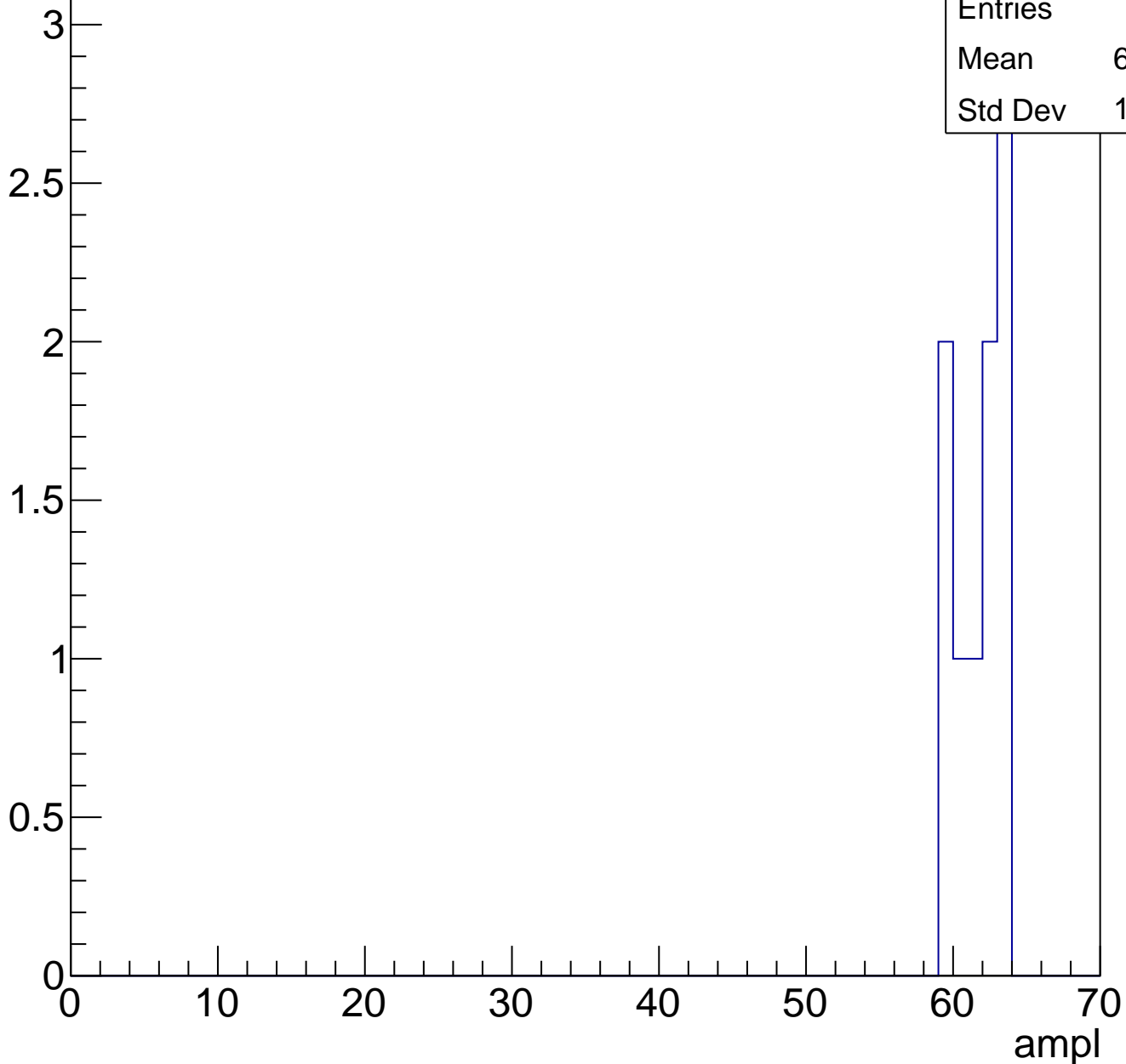
Entries	60
Mean	58.08
Std Dev	8.092



# B1L103S, U2-ch109, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U2-ch109, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U2-ch110, adc0

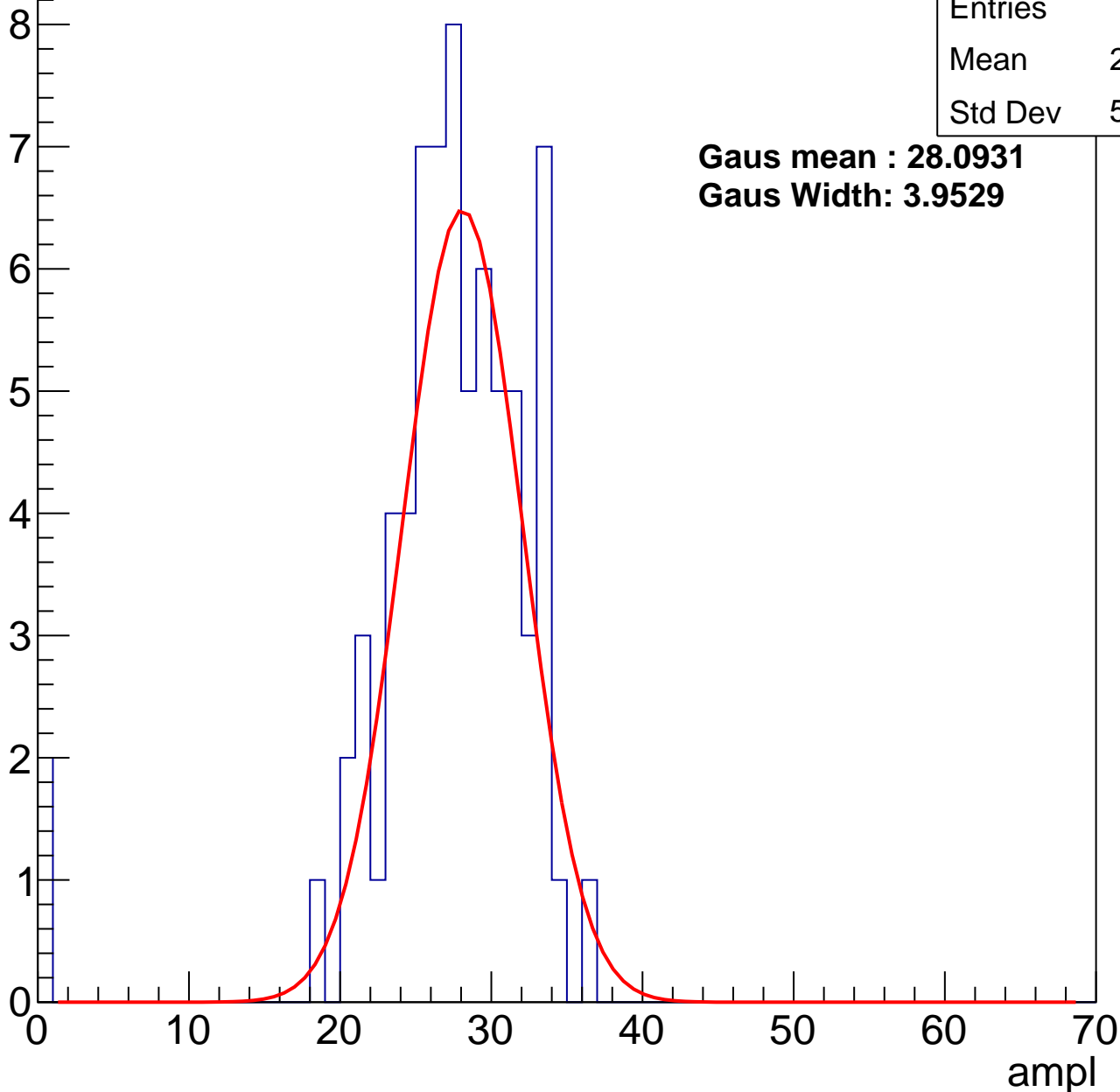
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	26.67
Std Dev	5.902

**Gaus mean : 28.0931**

**Gaus Width: 3.9529**



# B1L103S, U2-ch110, adc1

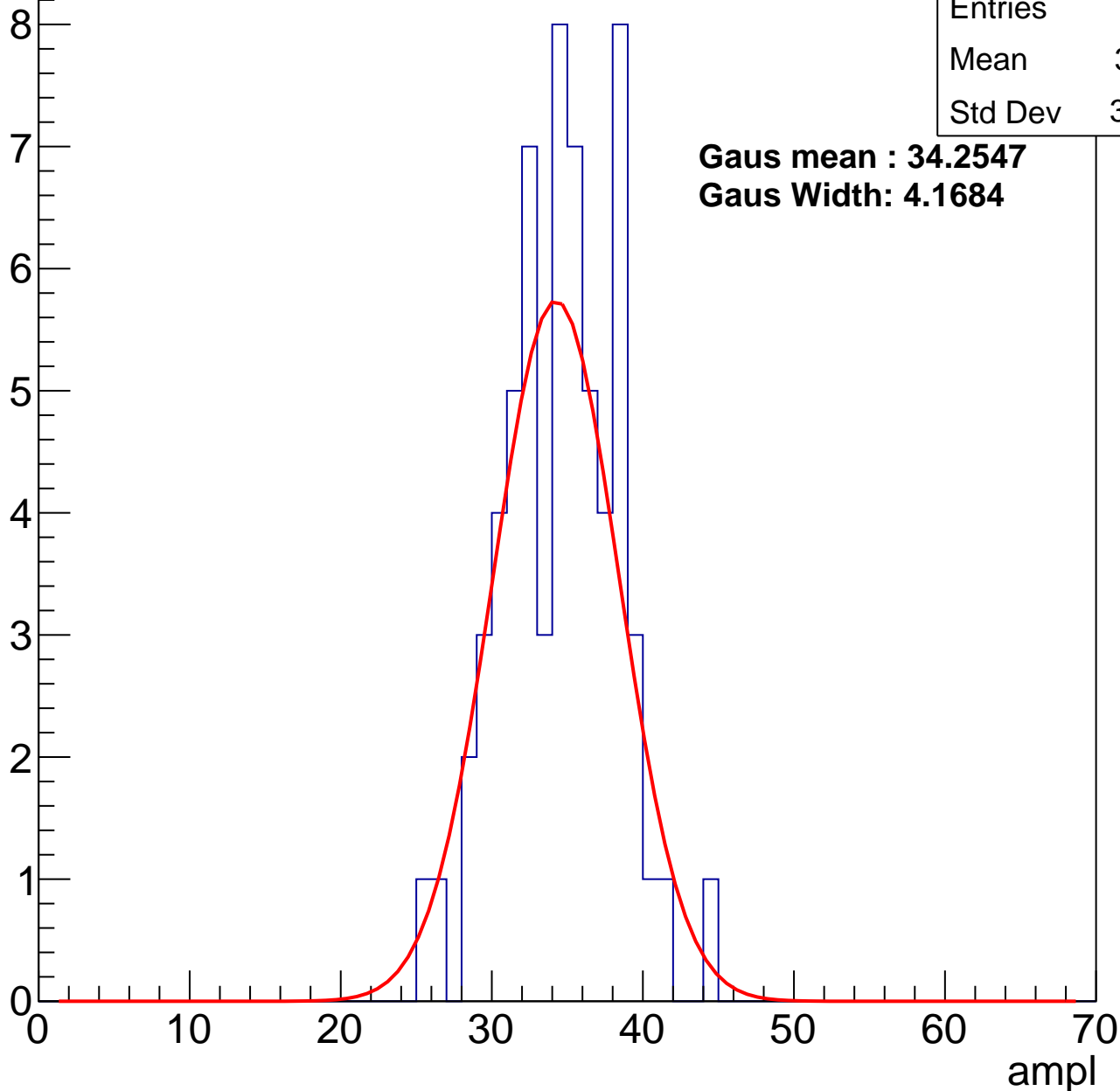
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	34.11
Std Dev	3.713

**Gaus mean : 34.2547**

**Gaus Width: 4.1684**



# B1L103S, U2-ch110, adc2

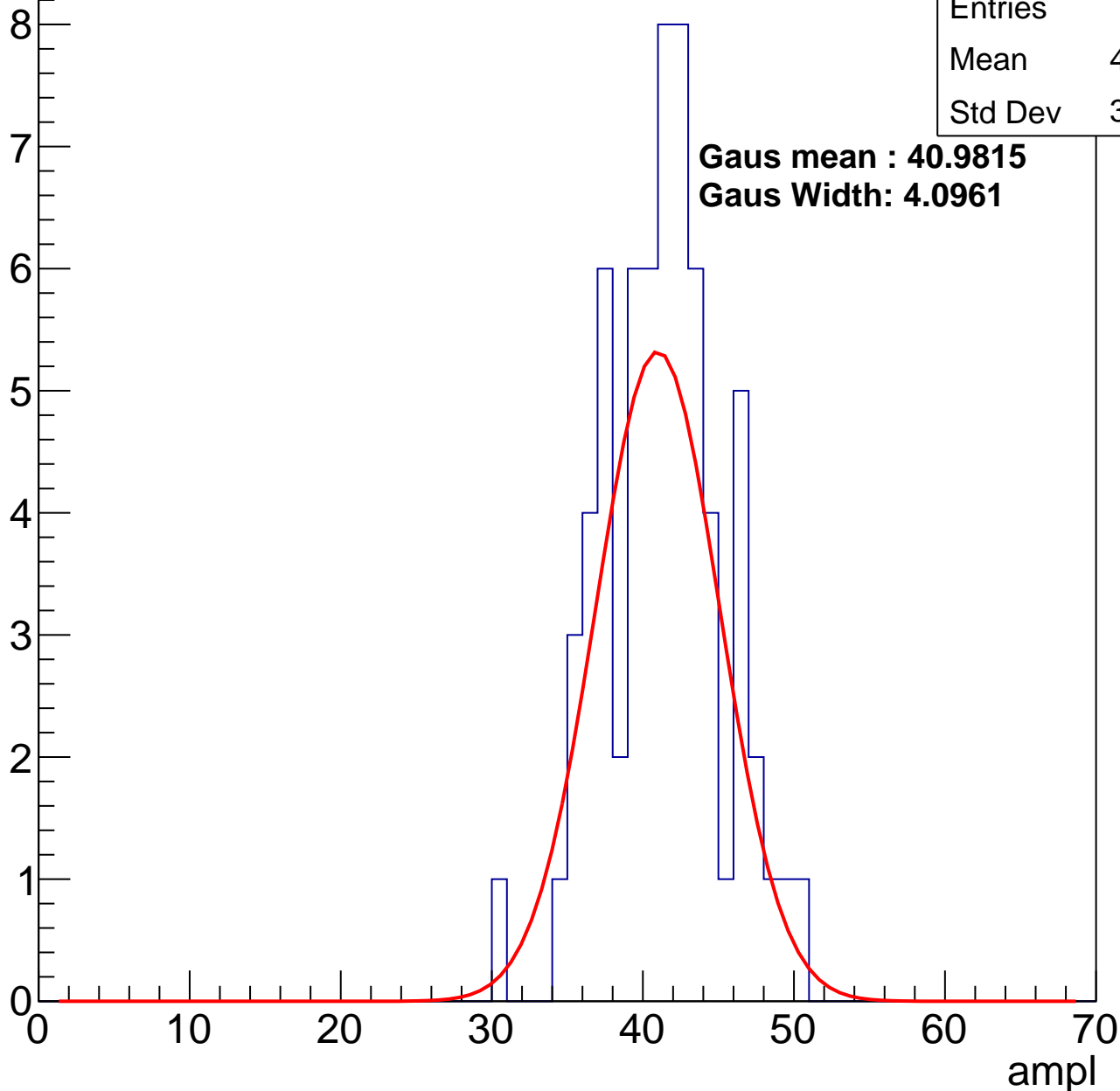
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	40.89
Std Dev	3.885

**Gaus mean : 40.9815**

**Gaus Width: 4.0961**

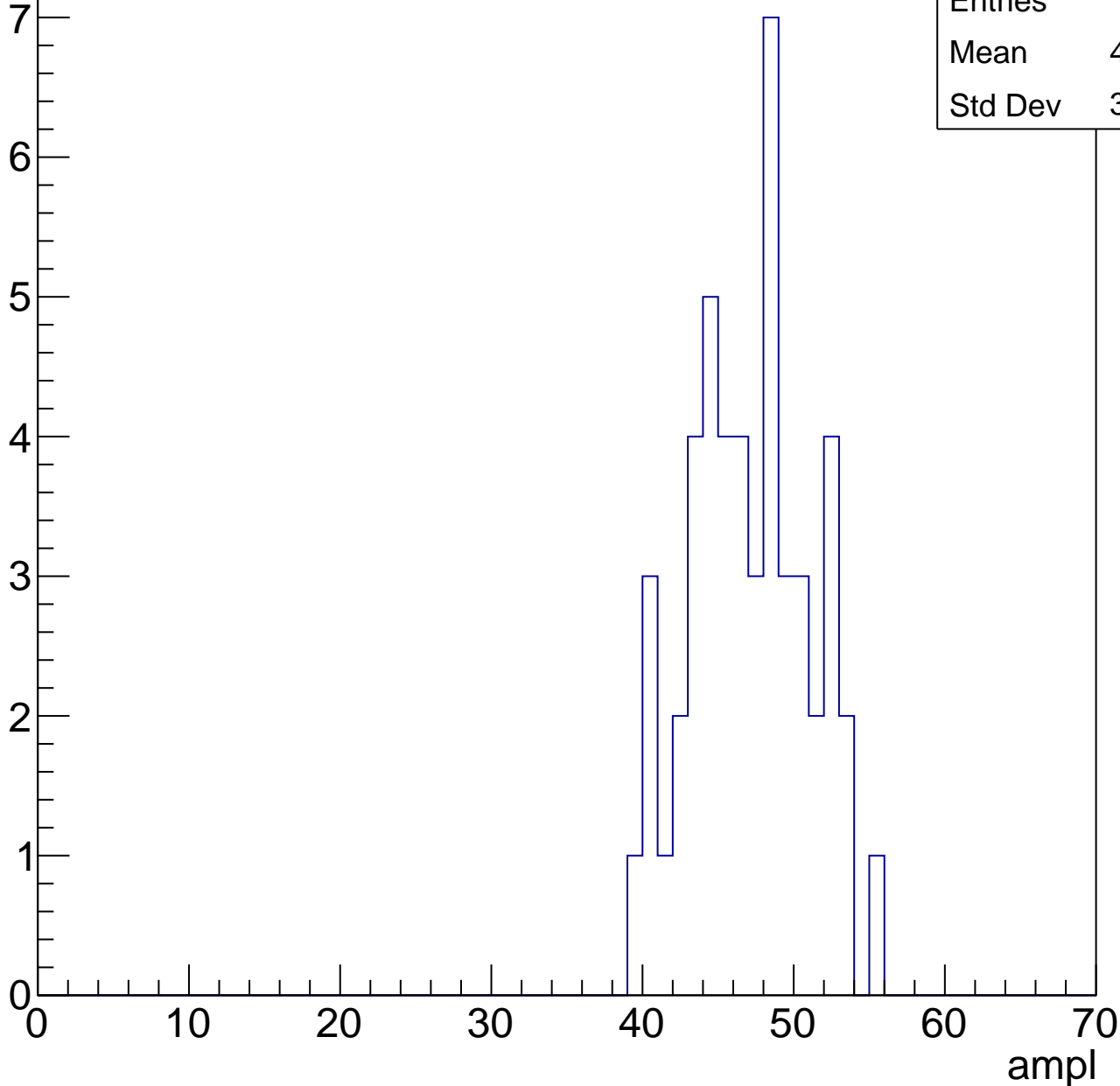


# B1L103S, U2-ch110, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	46.63
Std Dev	3.869

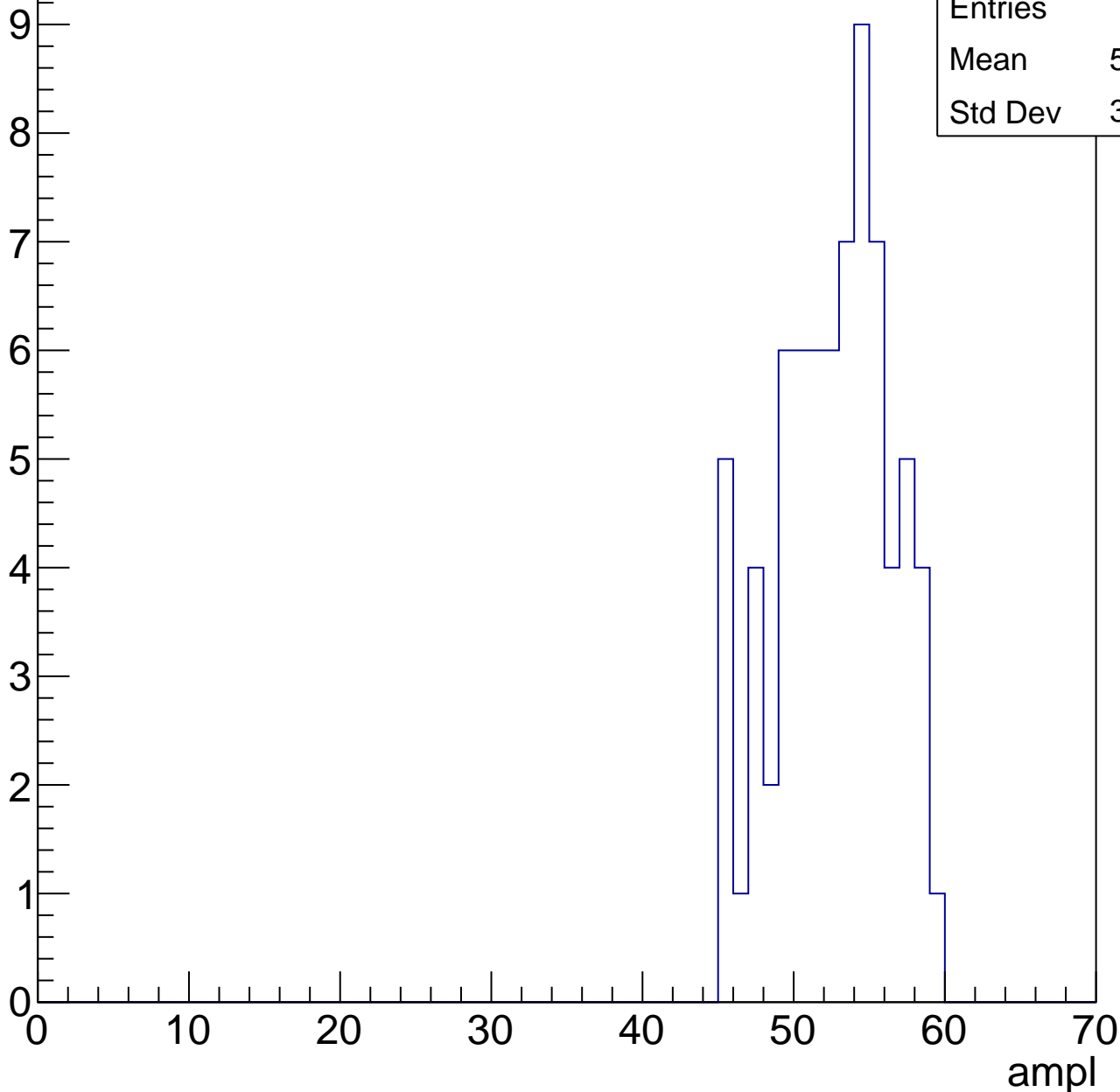


# B1L103S, U2-ch110, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	52.18
Std Dev	3.669

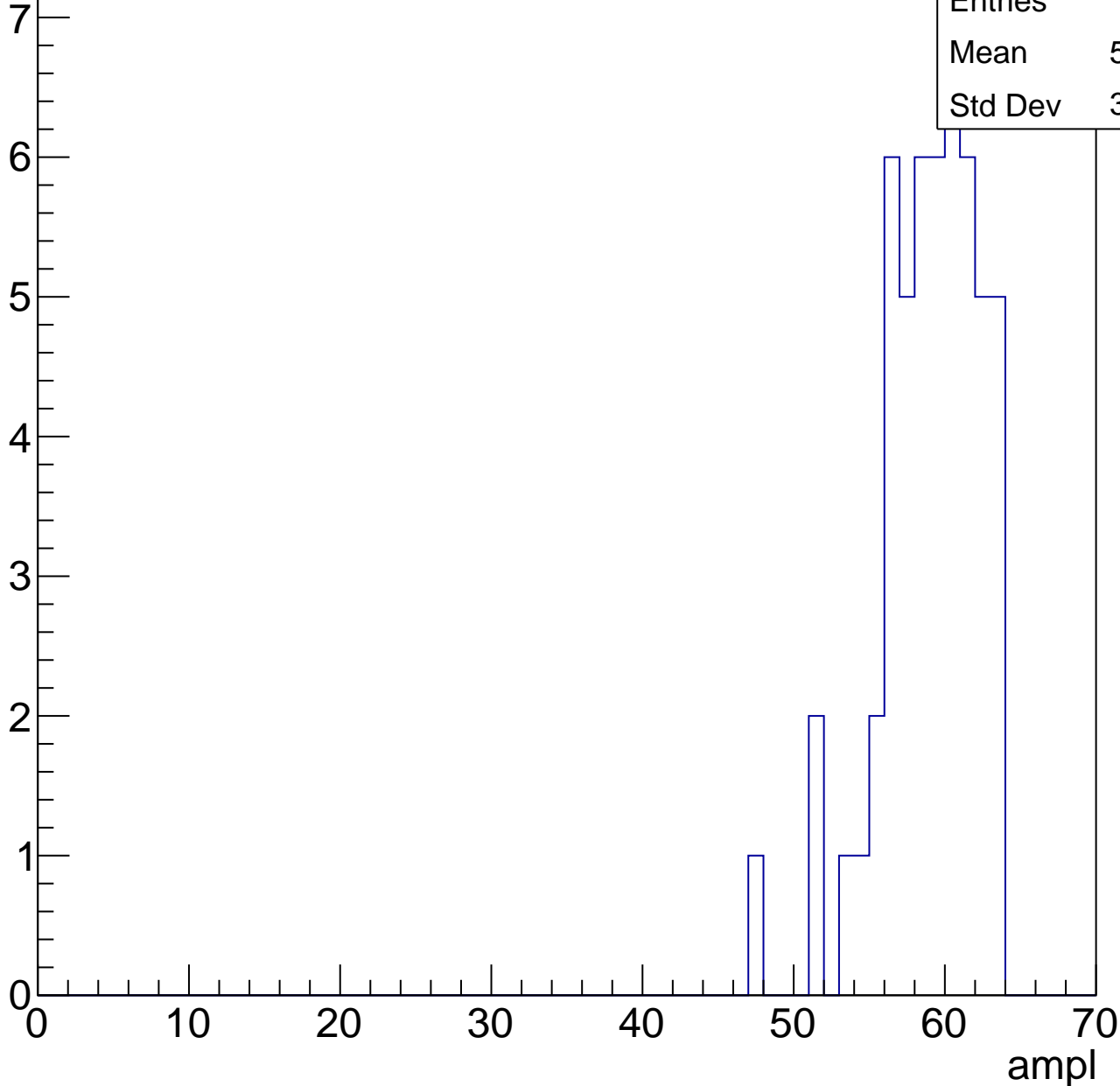


# B1L103S, U2-ch110, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

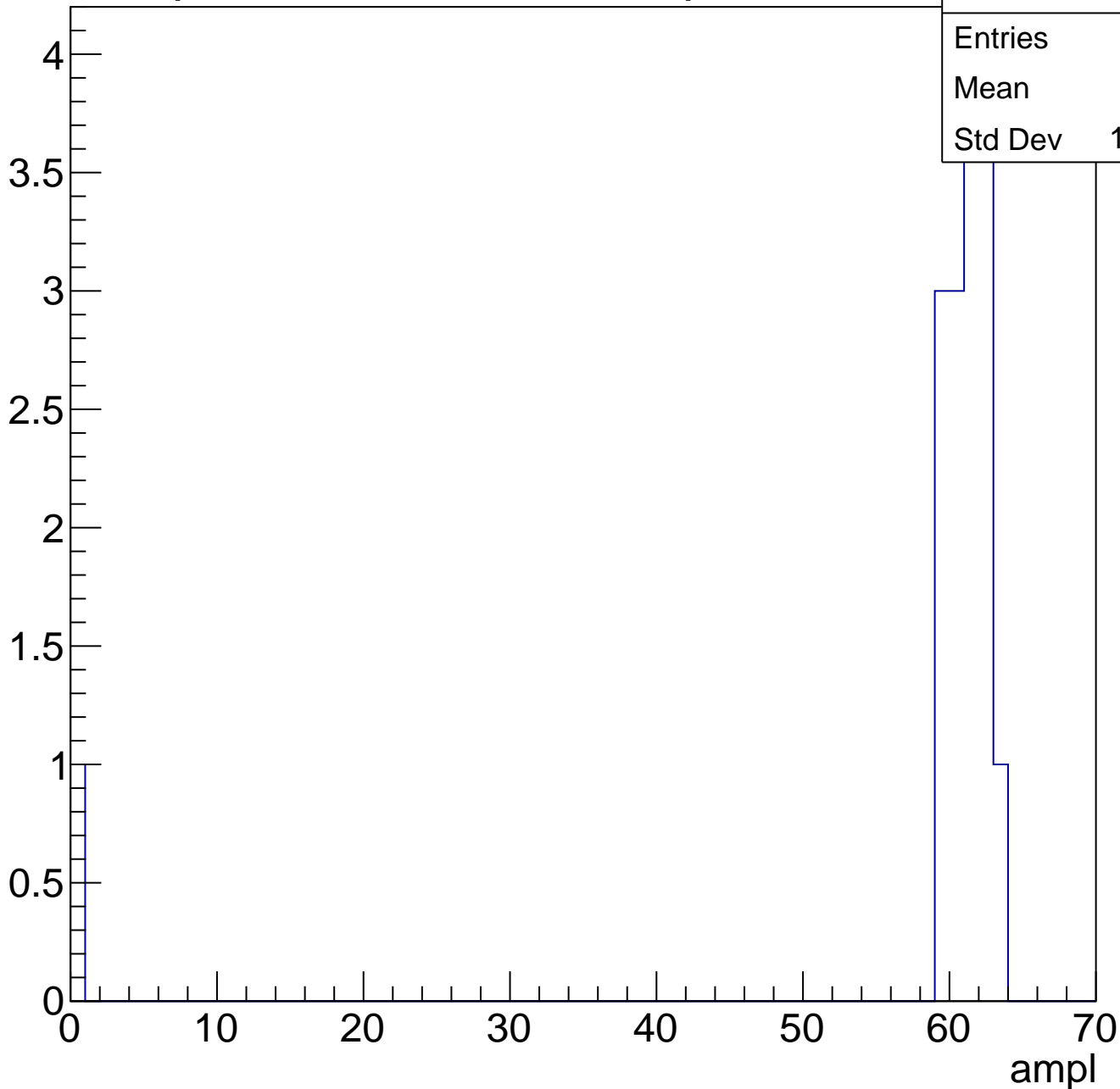
Entries	53
Mean	58.49
Std Dev	3.329



# B1L103S, U2-ch110, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

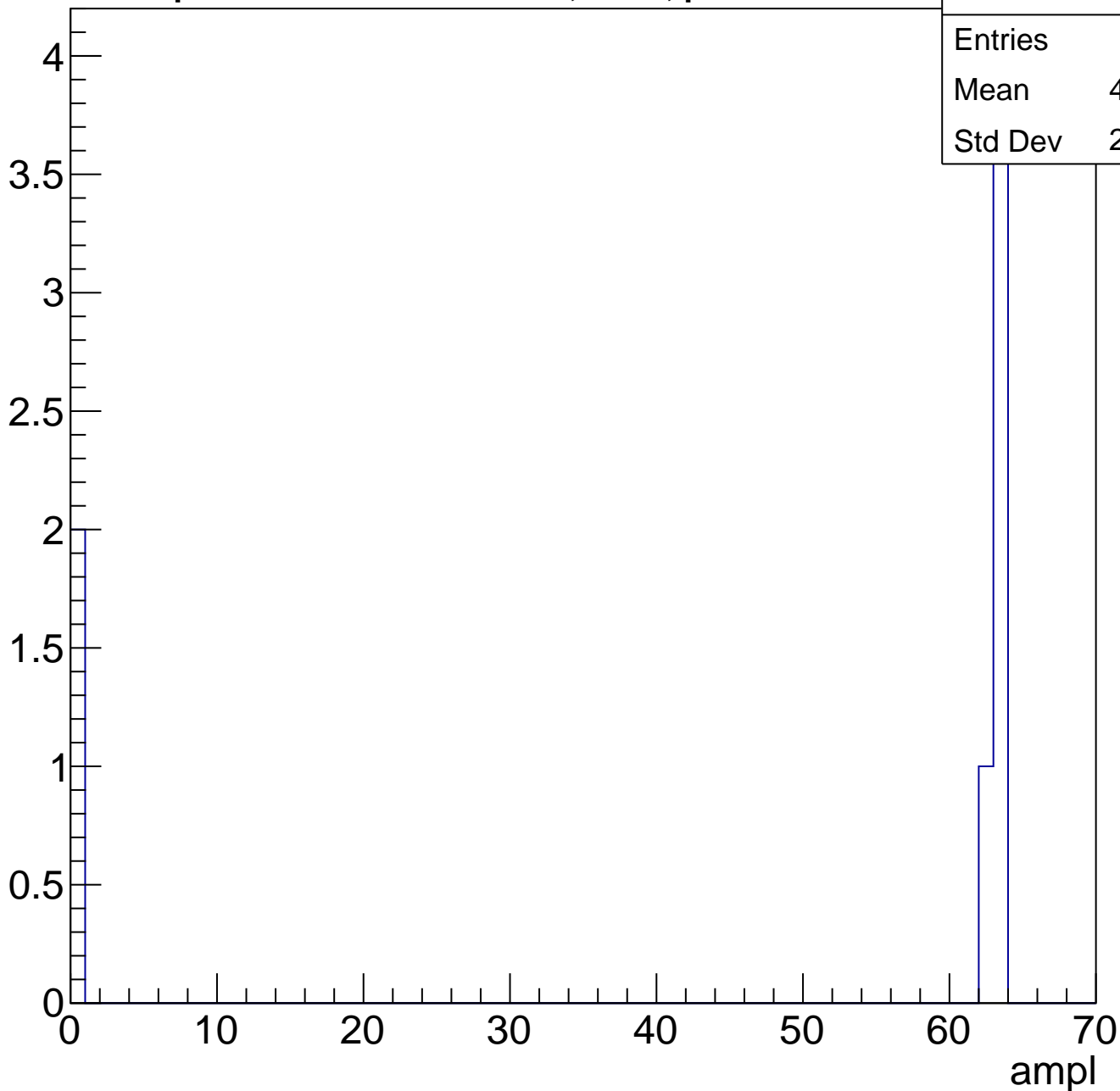




# B1L103S, U2-ch110, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch111, adc0

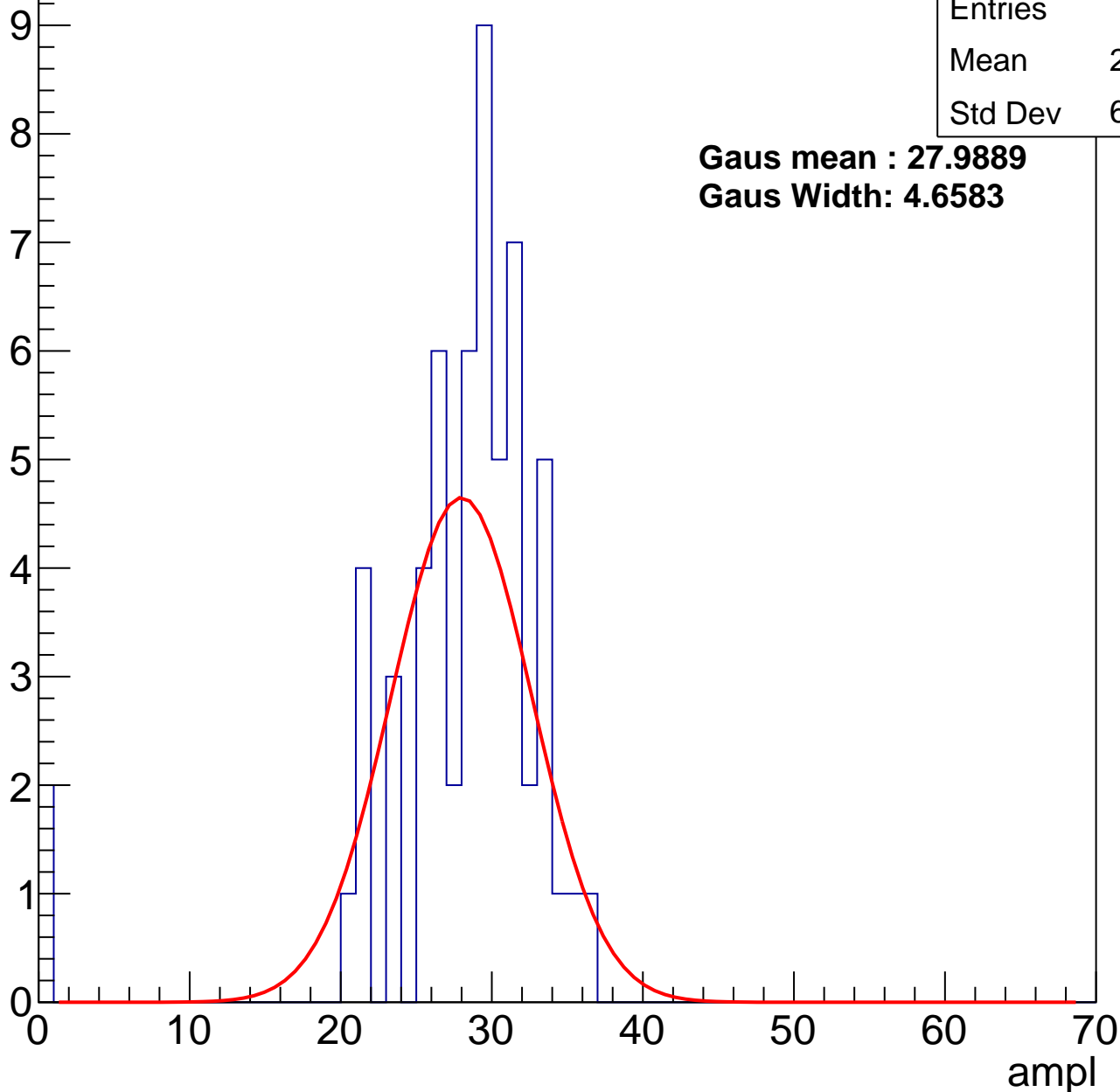
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	27.34
Std Dev	6.294

**Gaus mean : 27.9889**

**Gaus Width: 4.6583**



# B1L103S, U2-ch111, adc1

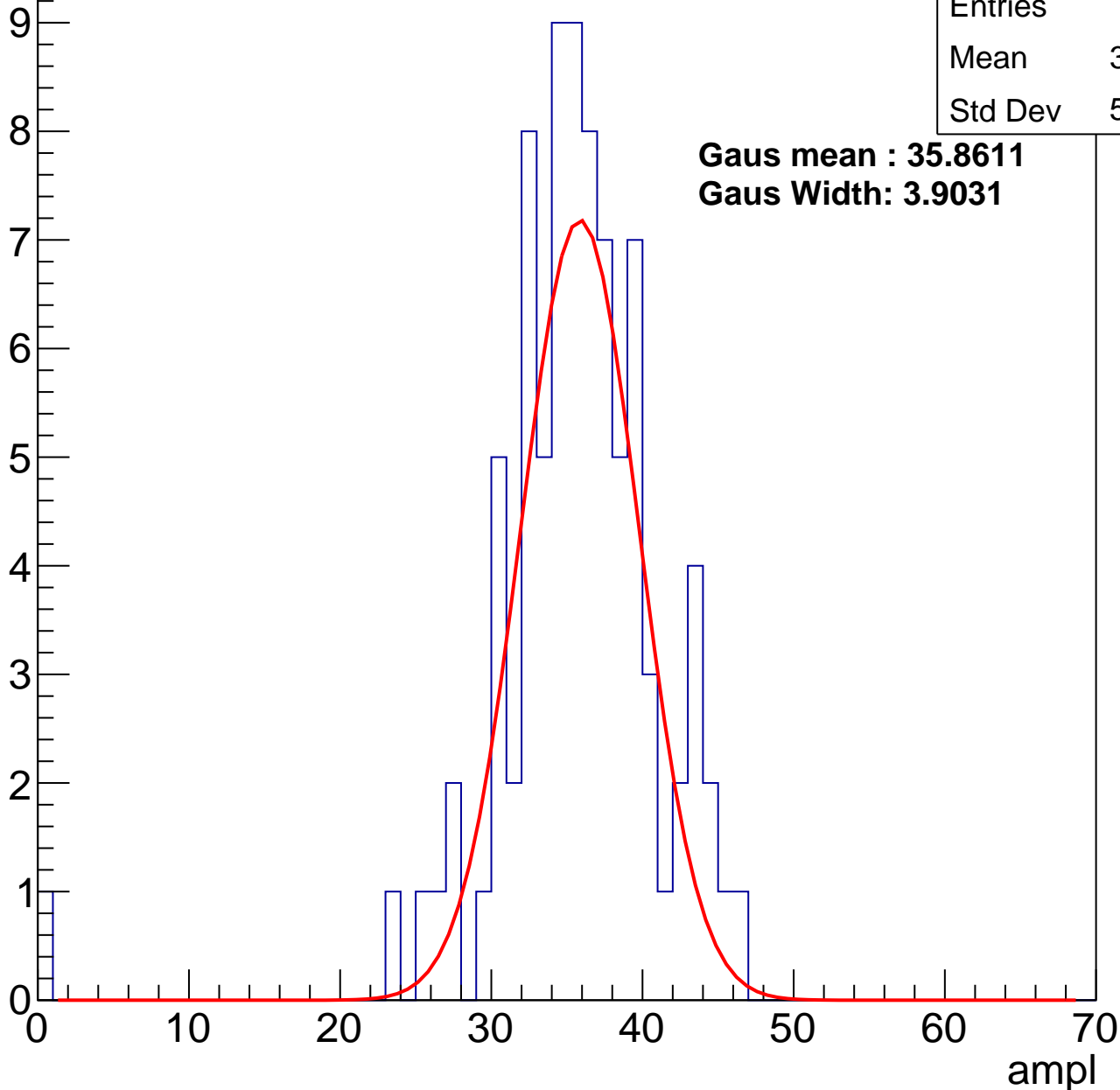
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	86
Mean	35.08
Std Dev	5.918

**Gaus mean : 35.8611**

**Gaus Width: 3.9031**



# B1L103S, U2-ch111, adc2

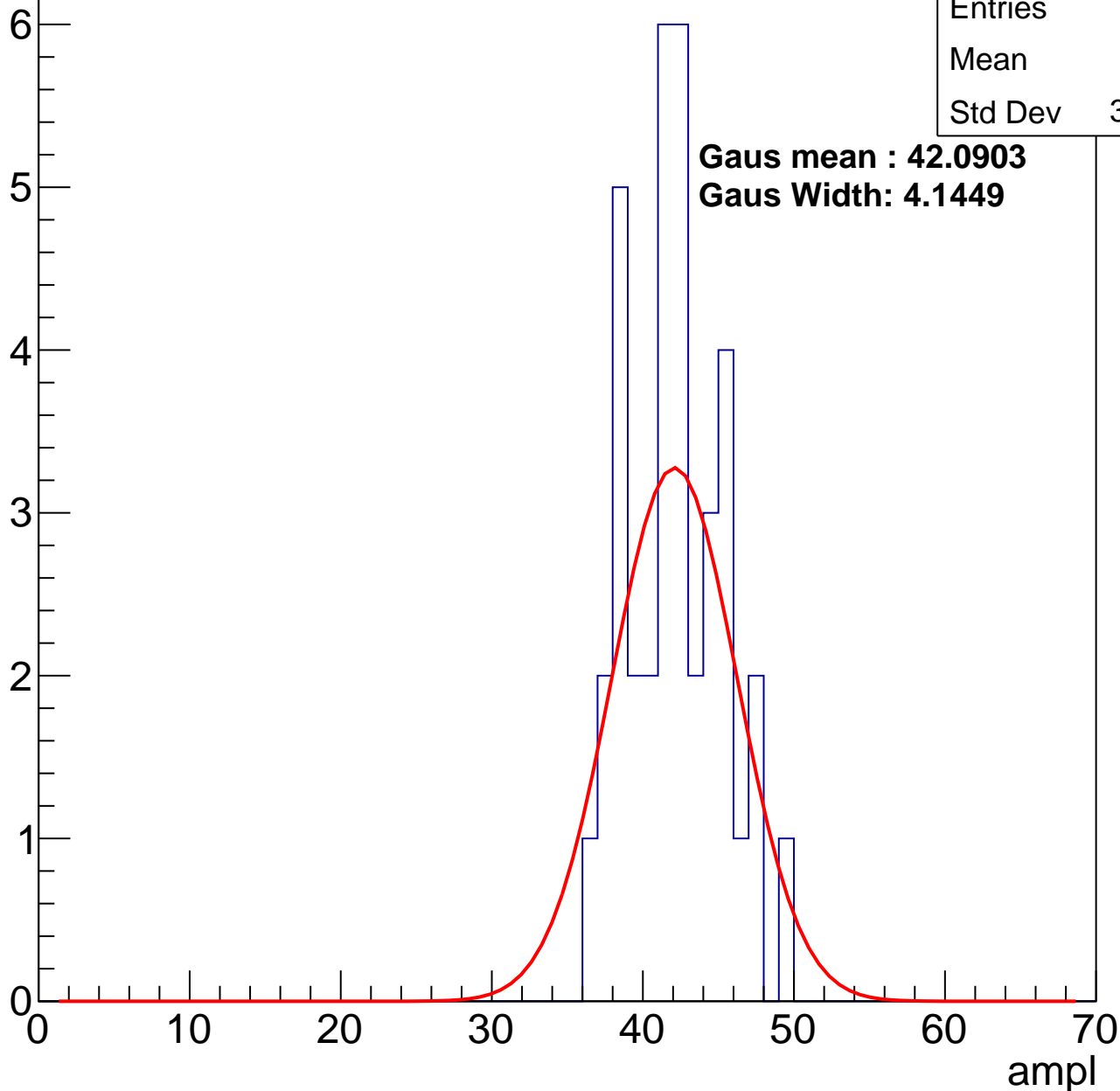
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	37
Mean	41.7
Std Dev	3.118

**Gaus mean : 42.0903**

**Gaus Width: 4.1449**

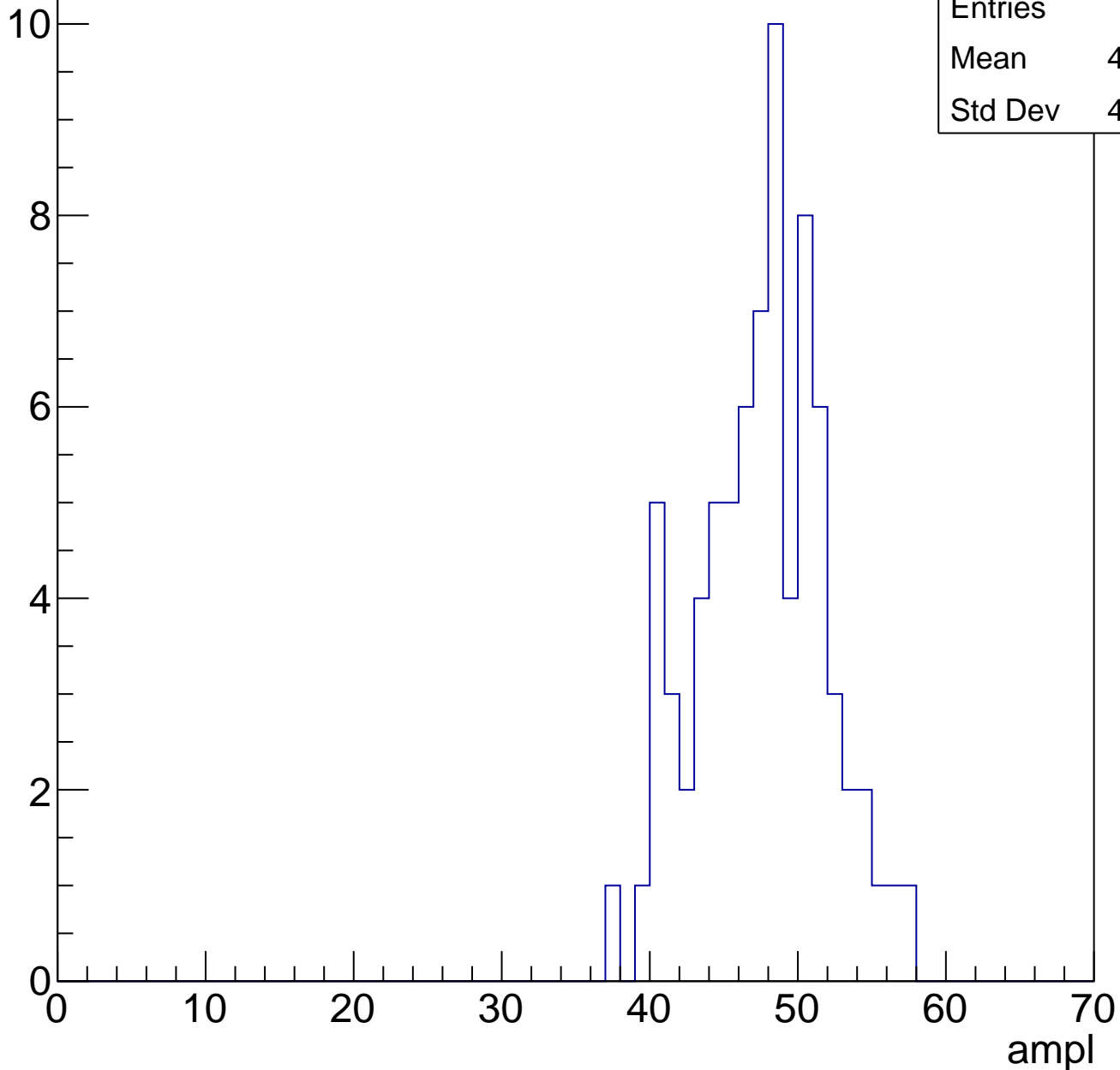


# B1L103S, U2-ch111, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	77
Mean	47.08
Std Dev	4.242

Entry

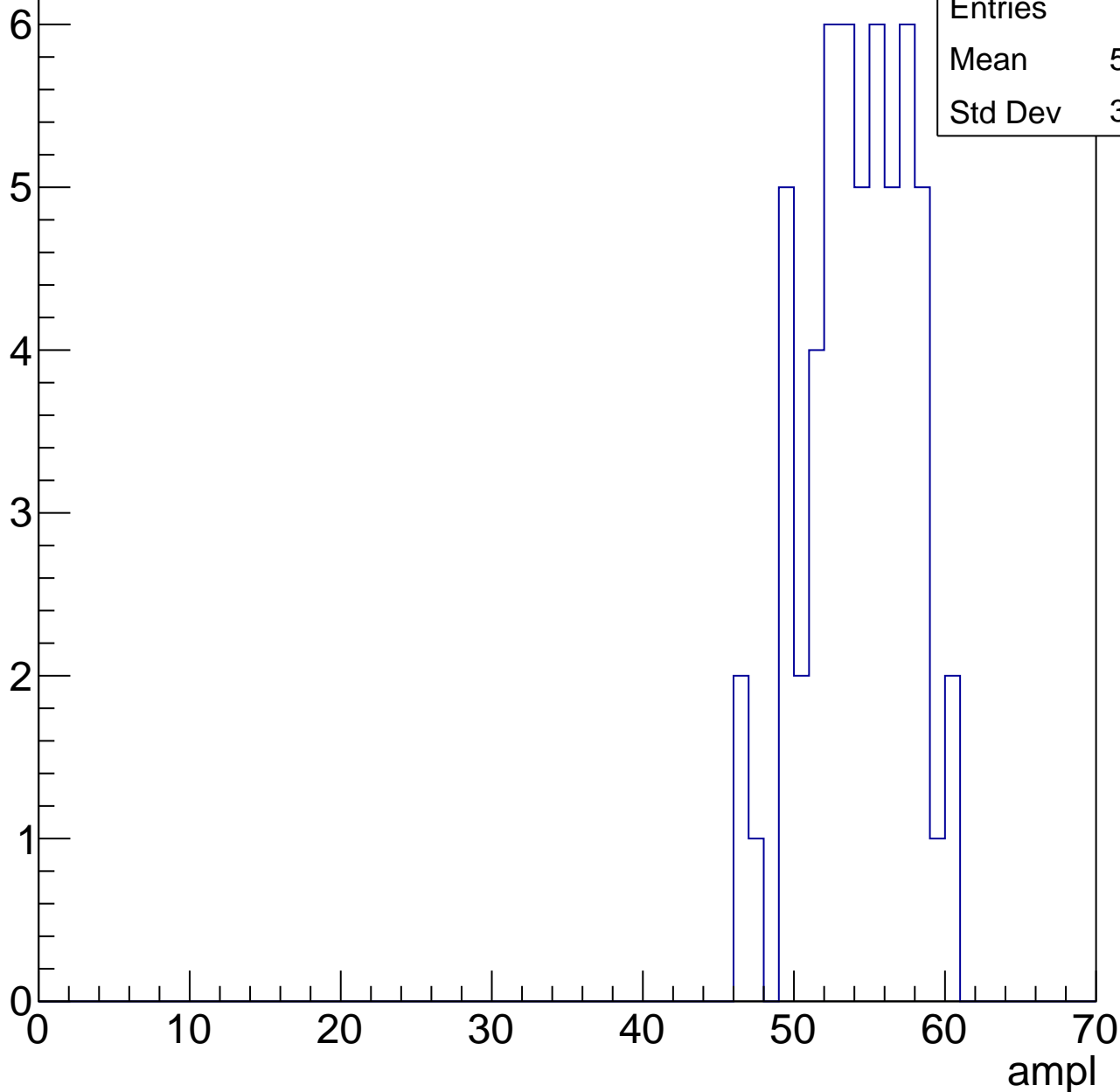


# B1L103S, U2-ch111, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	53.73
Std Dev	3.415

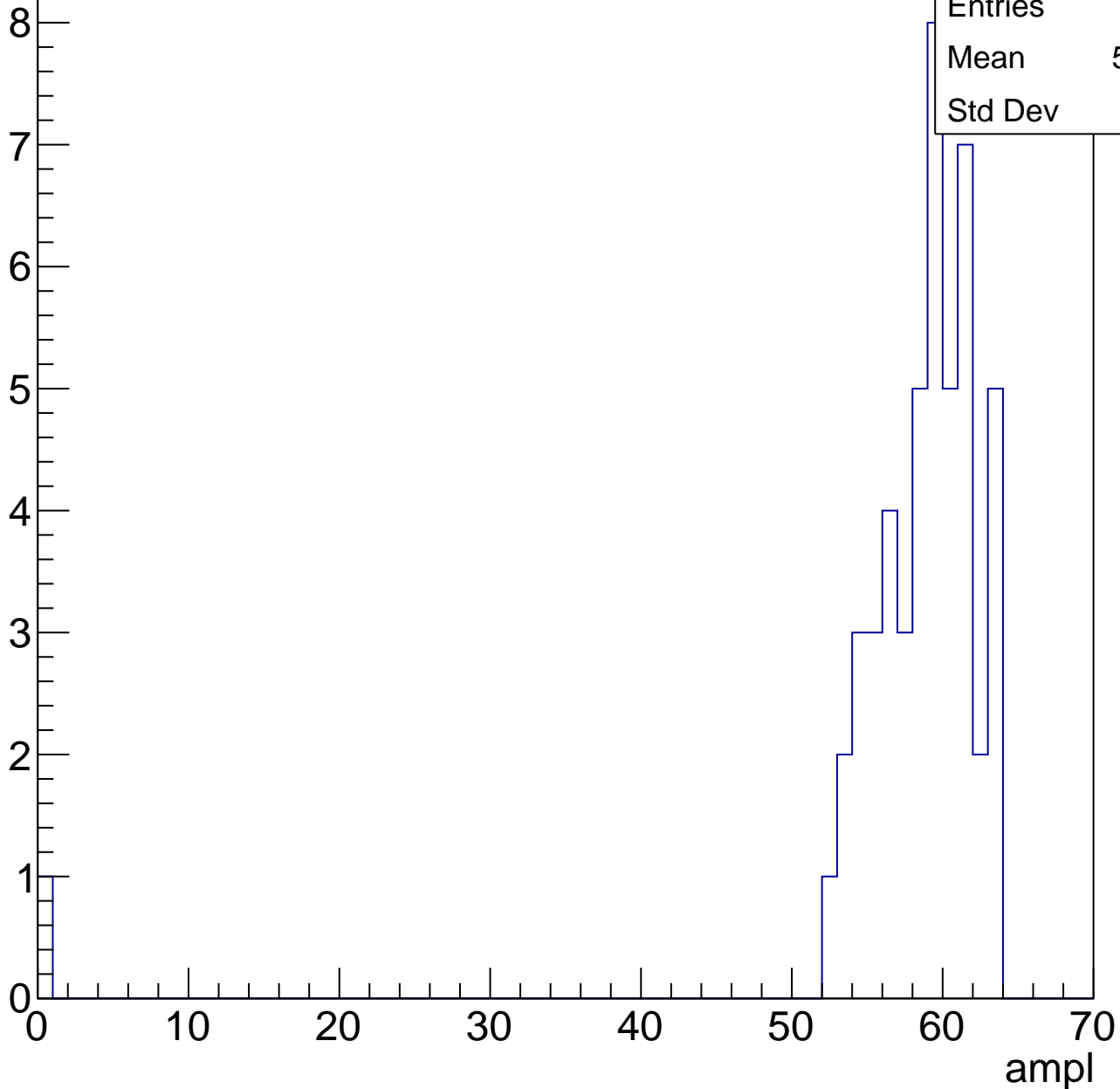


# B1L103S, U2-ch111, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	57.31
Std Dev	8.77

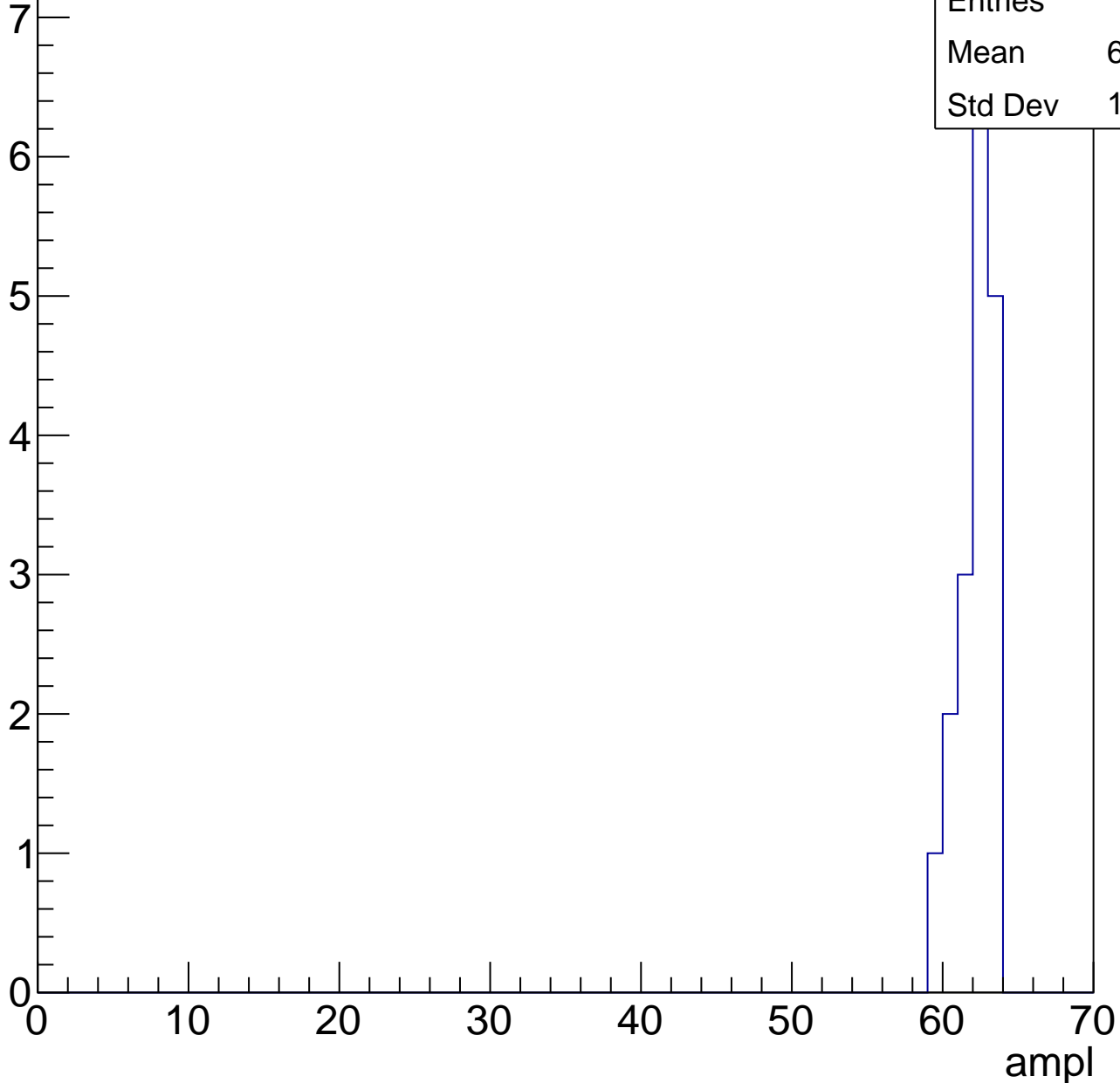


# B1L103S, U2-ch111, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	18
Mean	61.72
Std Dev	1.145

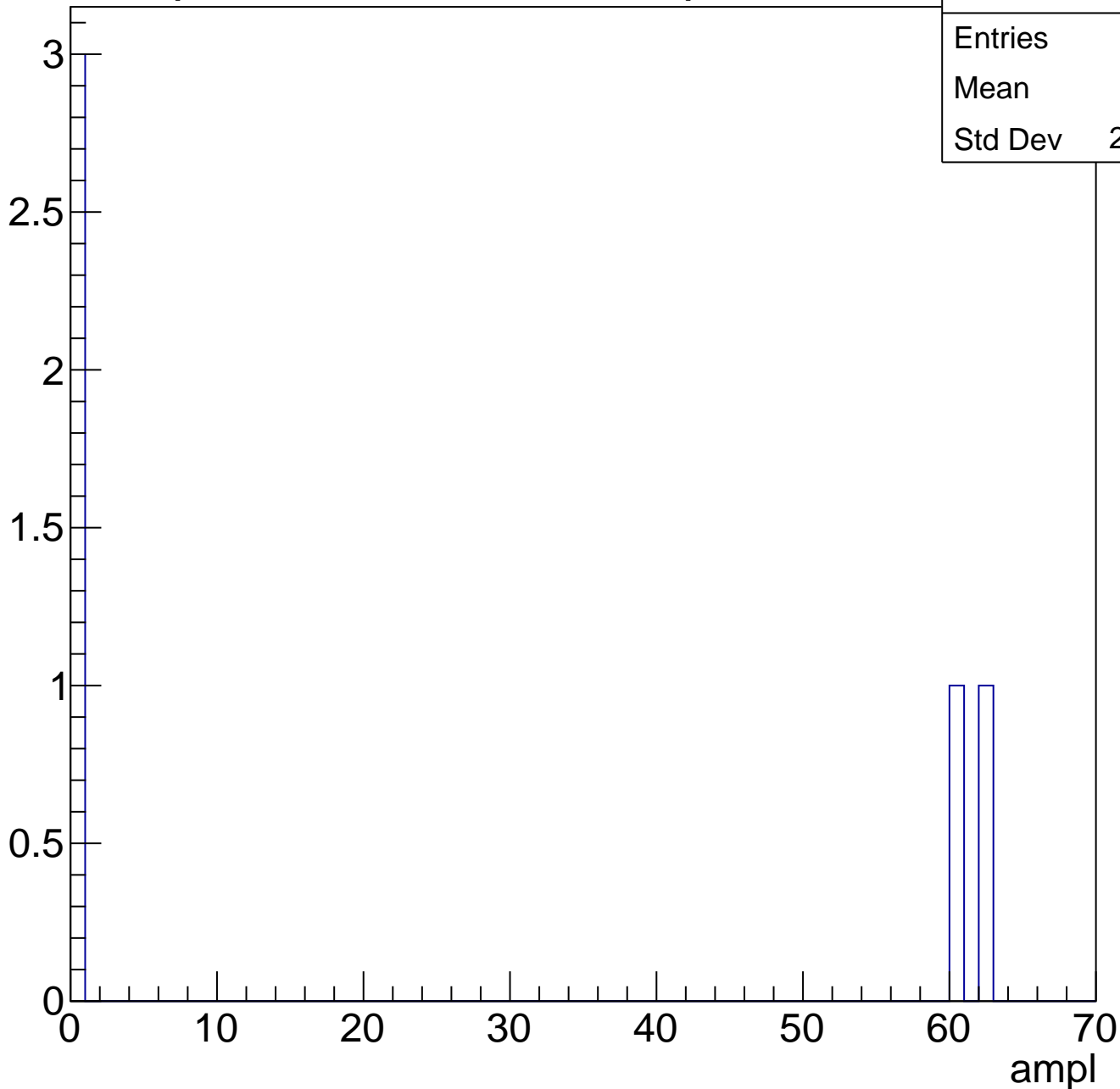




# B1L103S, U2-ch111, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch112, adc0

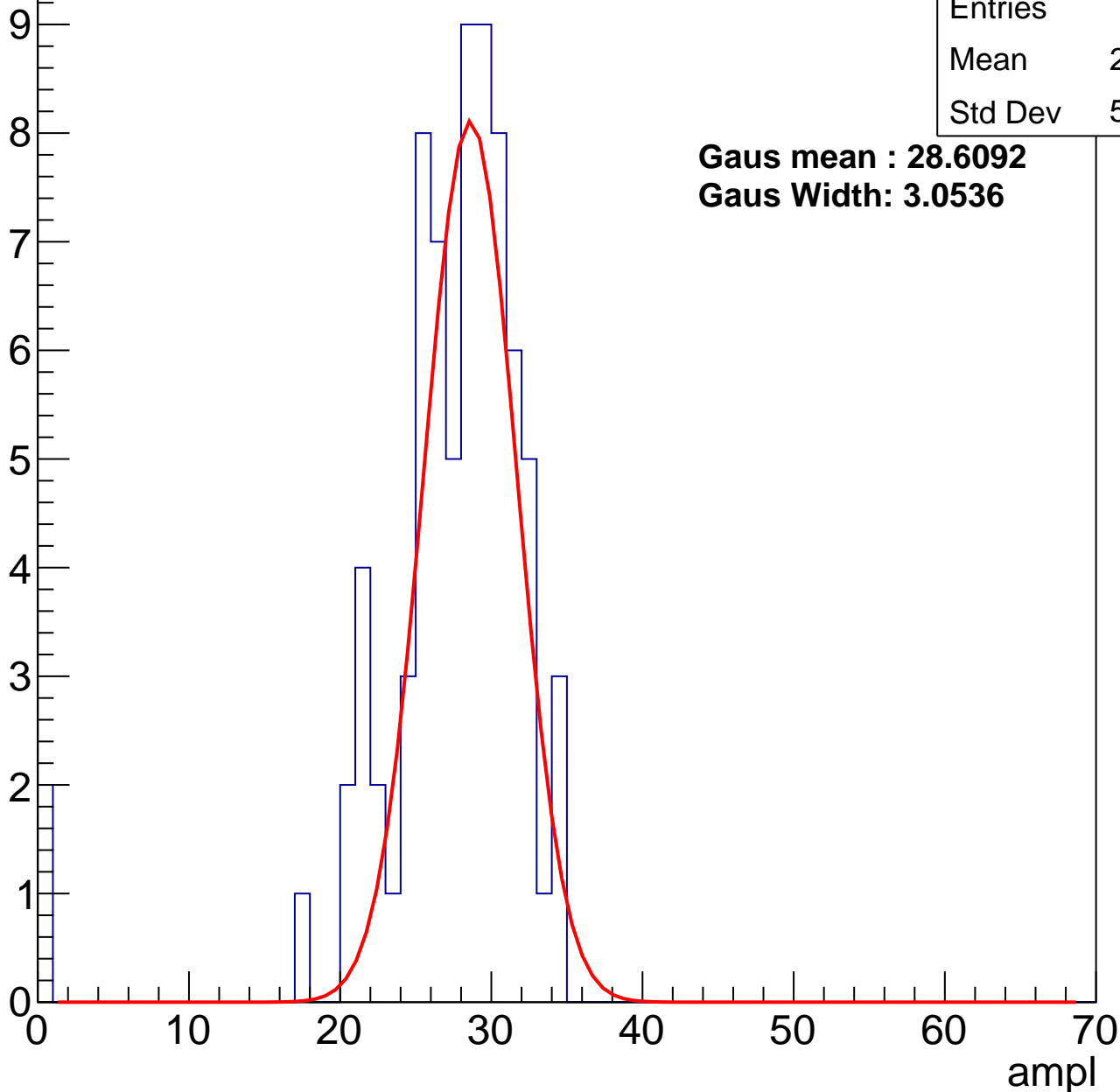
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	26.72
Std Dev	5.675

**Gaus mean : 28.6092**

**Gaus Width: 3.0536**



# B1L103S, U2-ch112, adc1

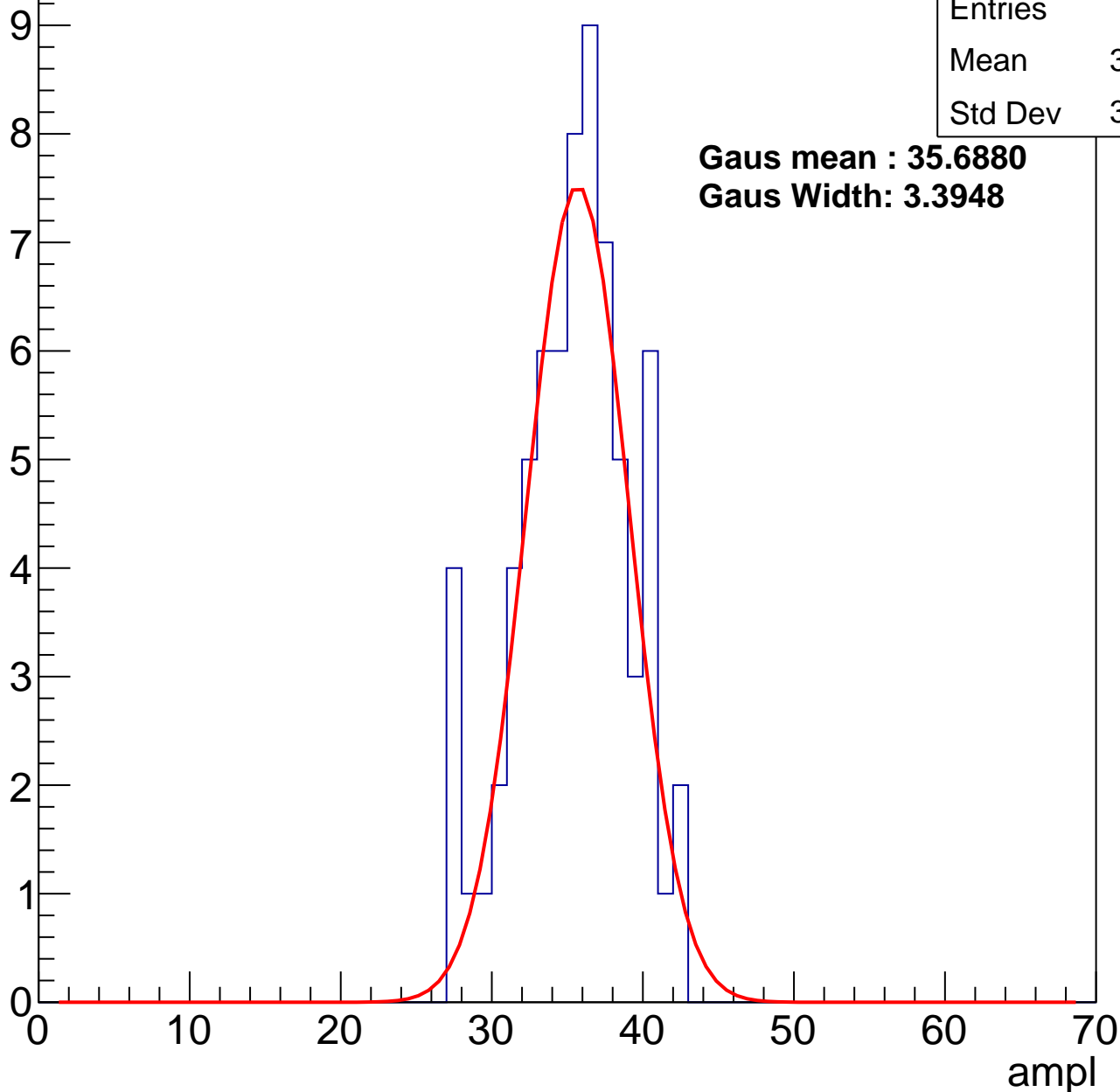
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	34.94
Std Dev	3.672

**Gaus mean : 35.6880**

**Gaus Width: 3.3948**



# B1L103S, U2-ch112, adc2

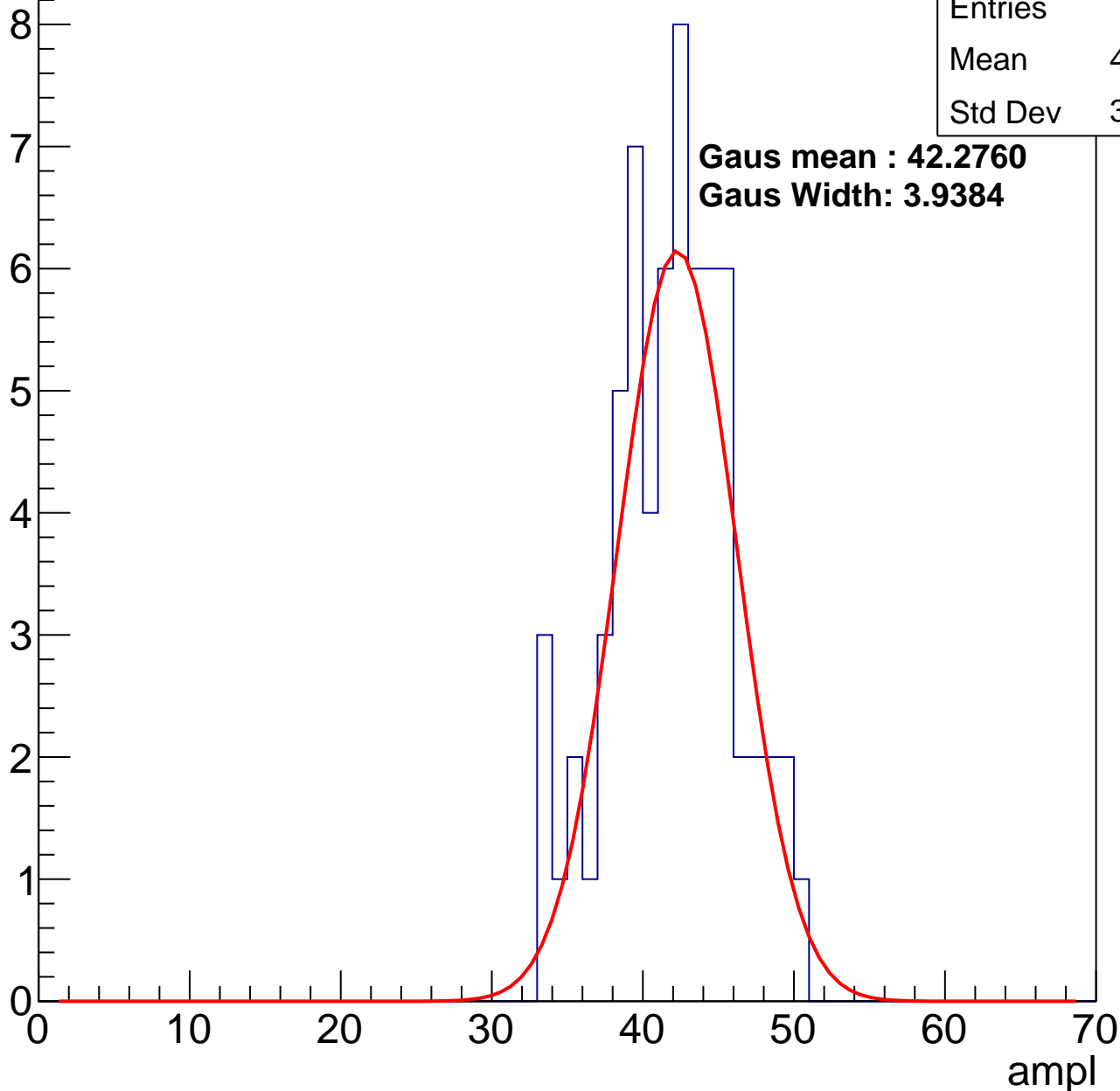
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	41.45
Std Dev	3.979

**Gaus mean : 42.2760**

**Gaus Width: 3.9384**

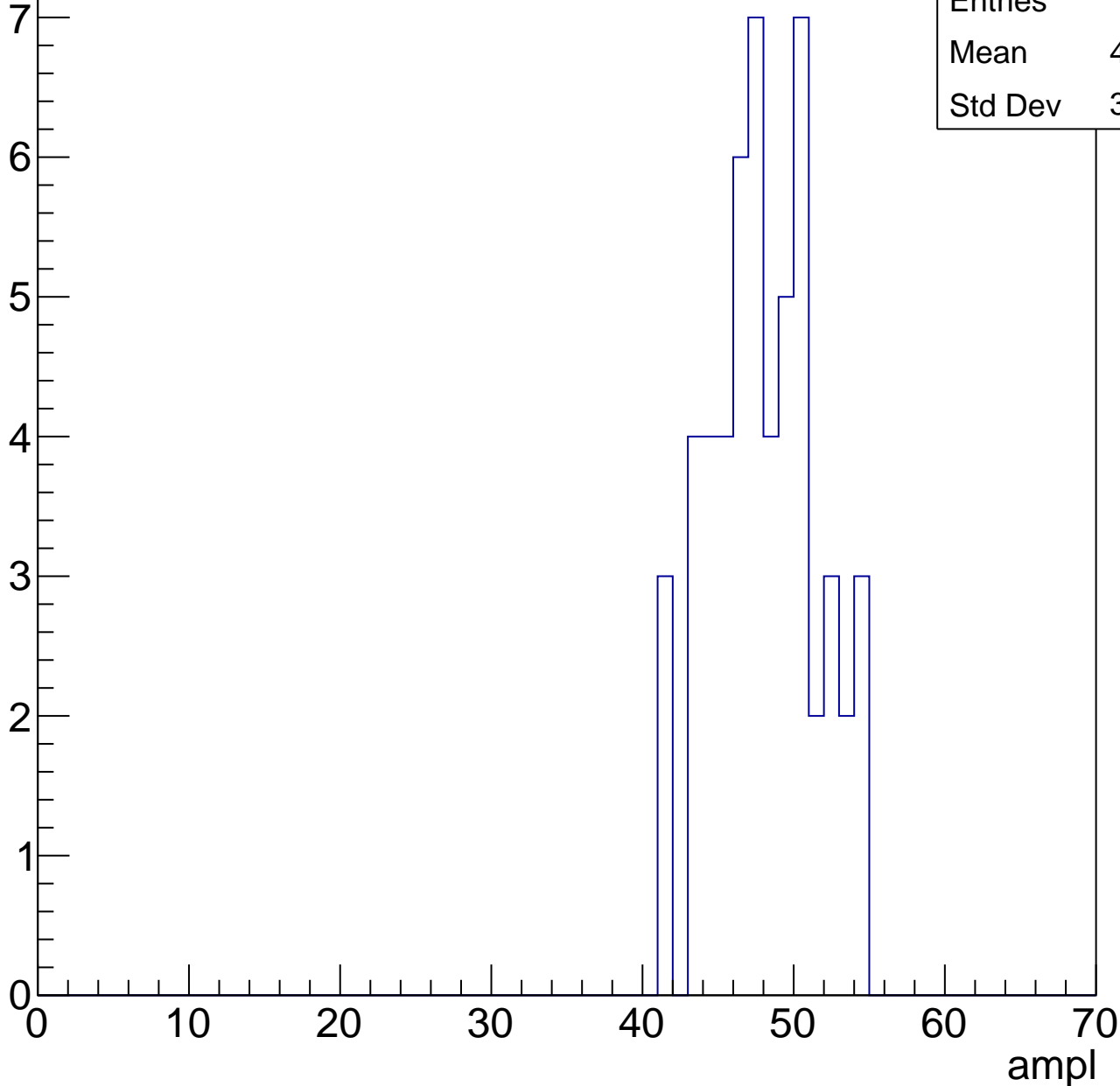


# B1L103S, U2-ch112, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	47.57
Std Dev	3.403

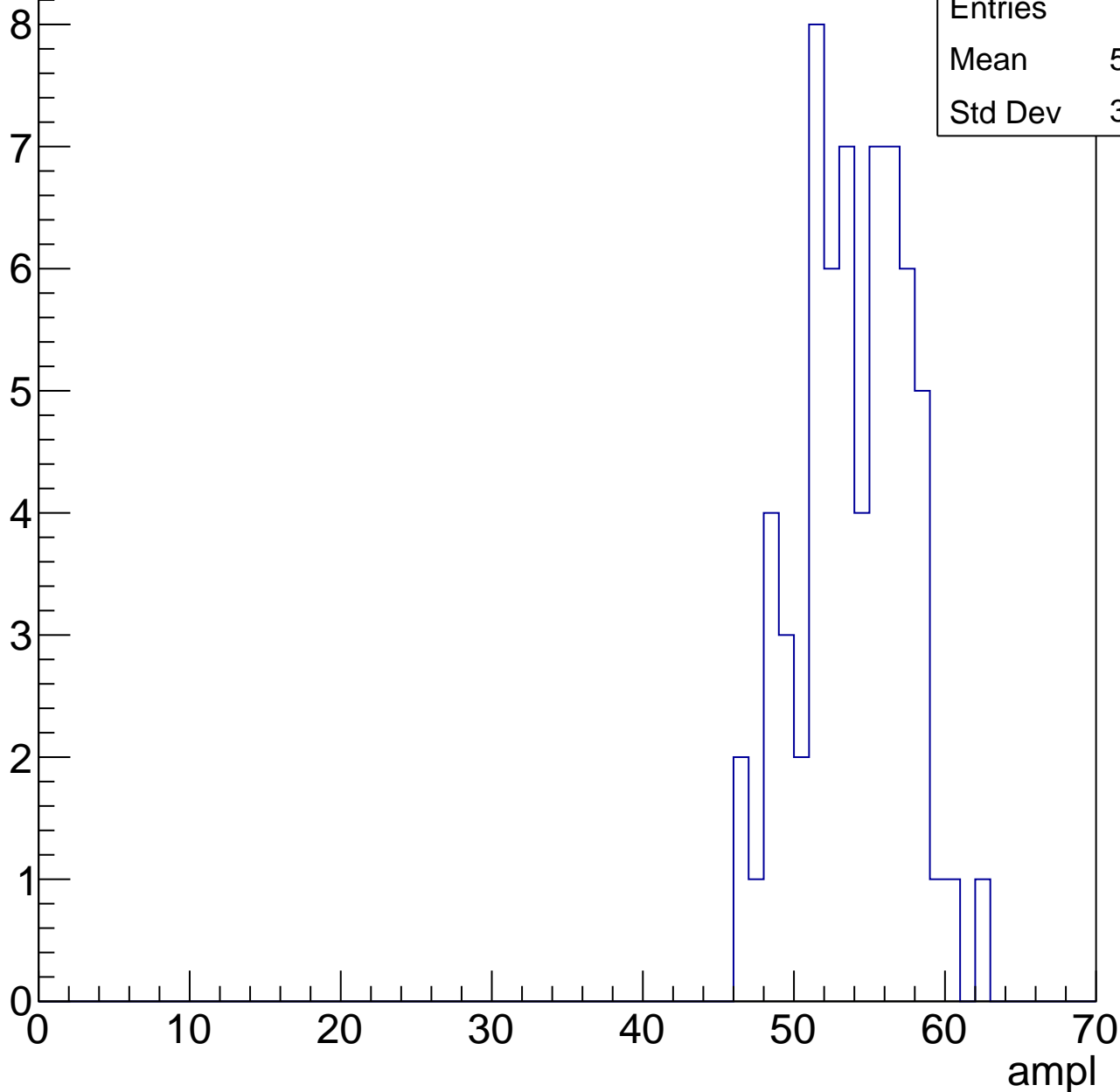


# B1L103S, U2-ch112, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	53.46
Std Dev	3.522

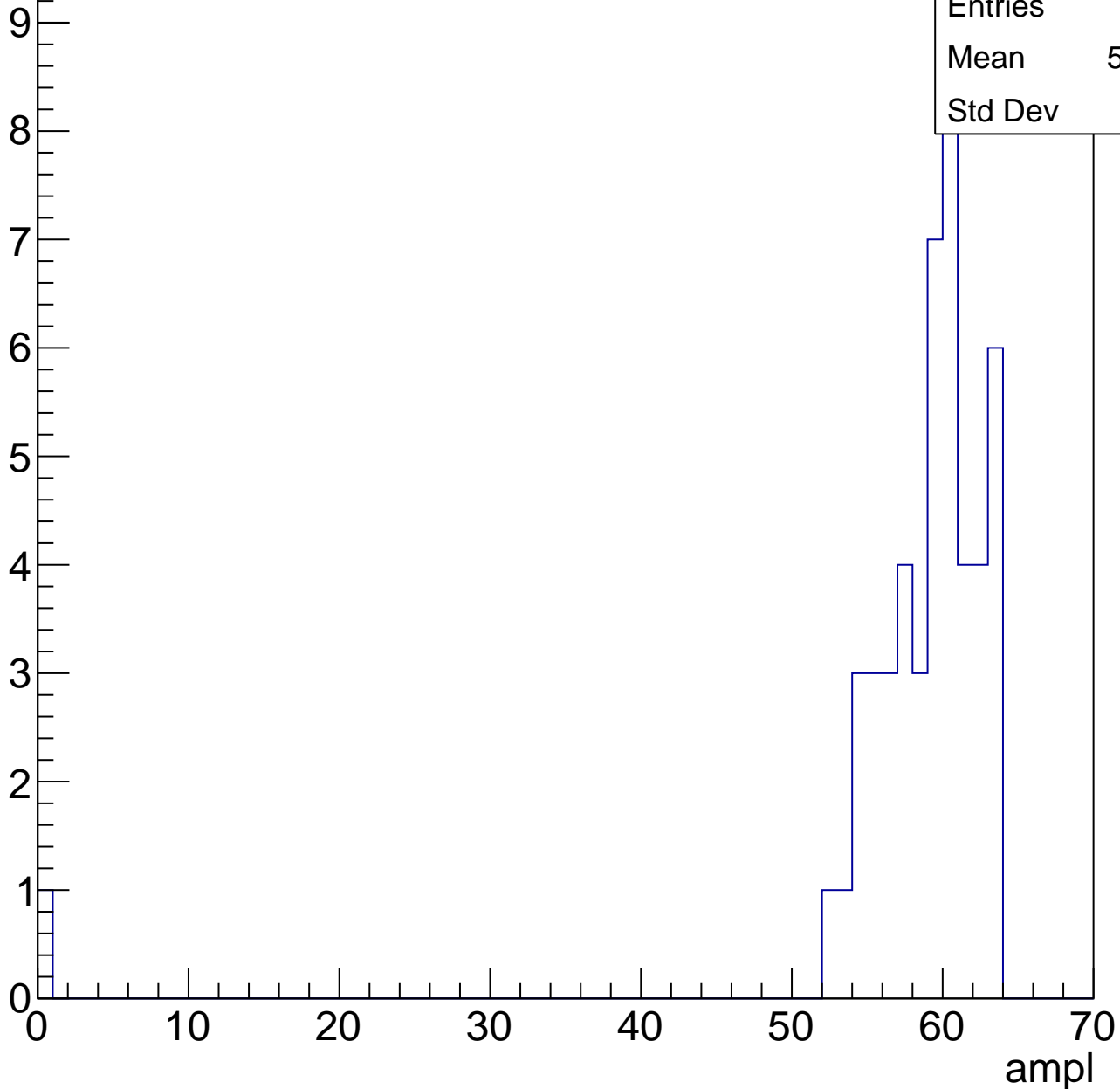


# B1L103S, U2-ch112, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	57.65
Std Dev	8.81

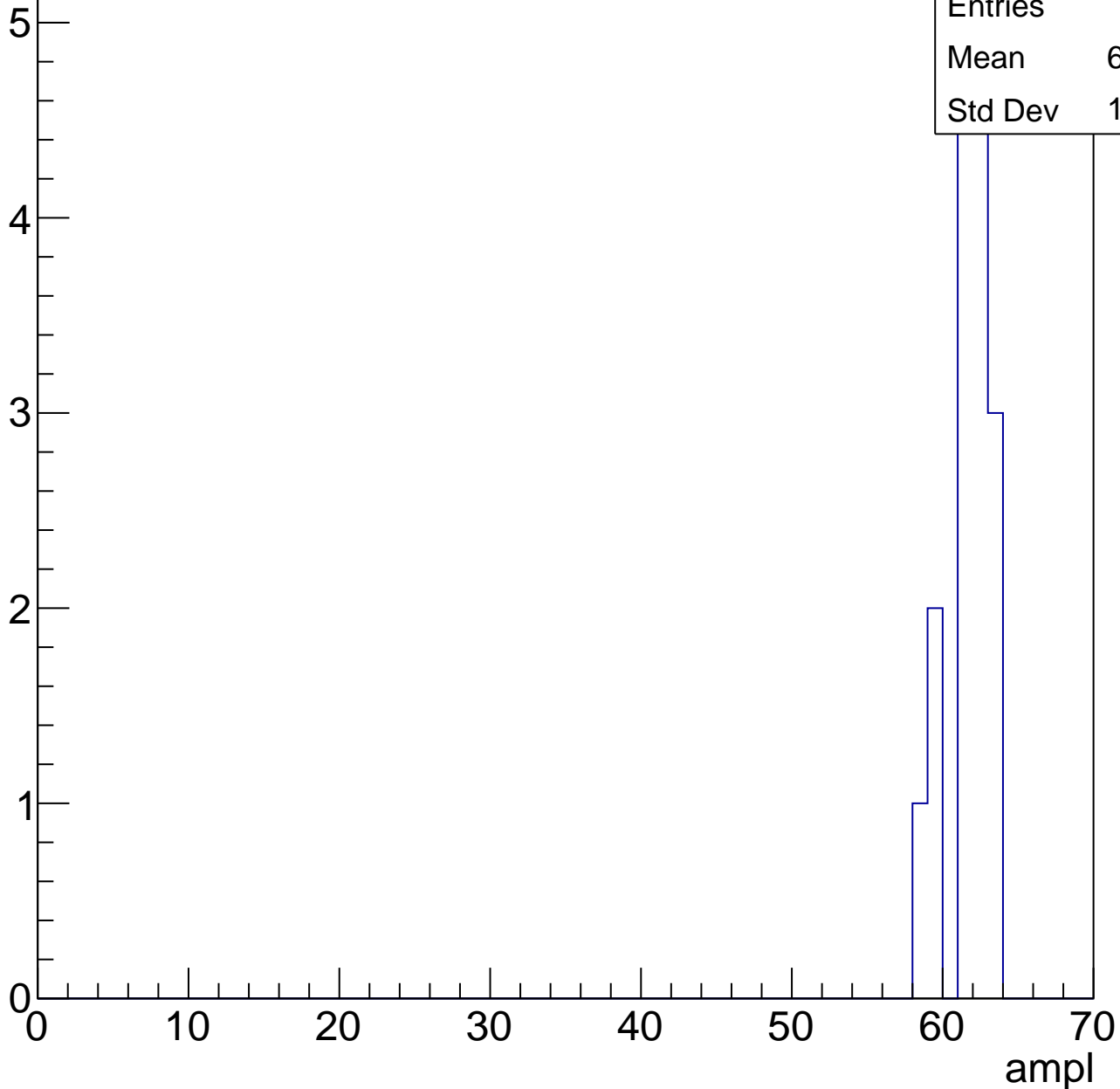


# B1L103S, U2-ch112, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	16
Mean	61.25
Std Dev	1.436

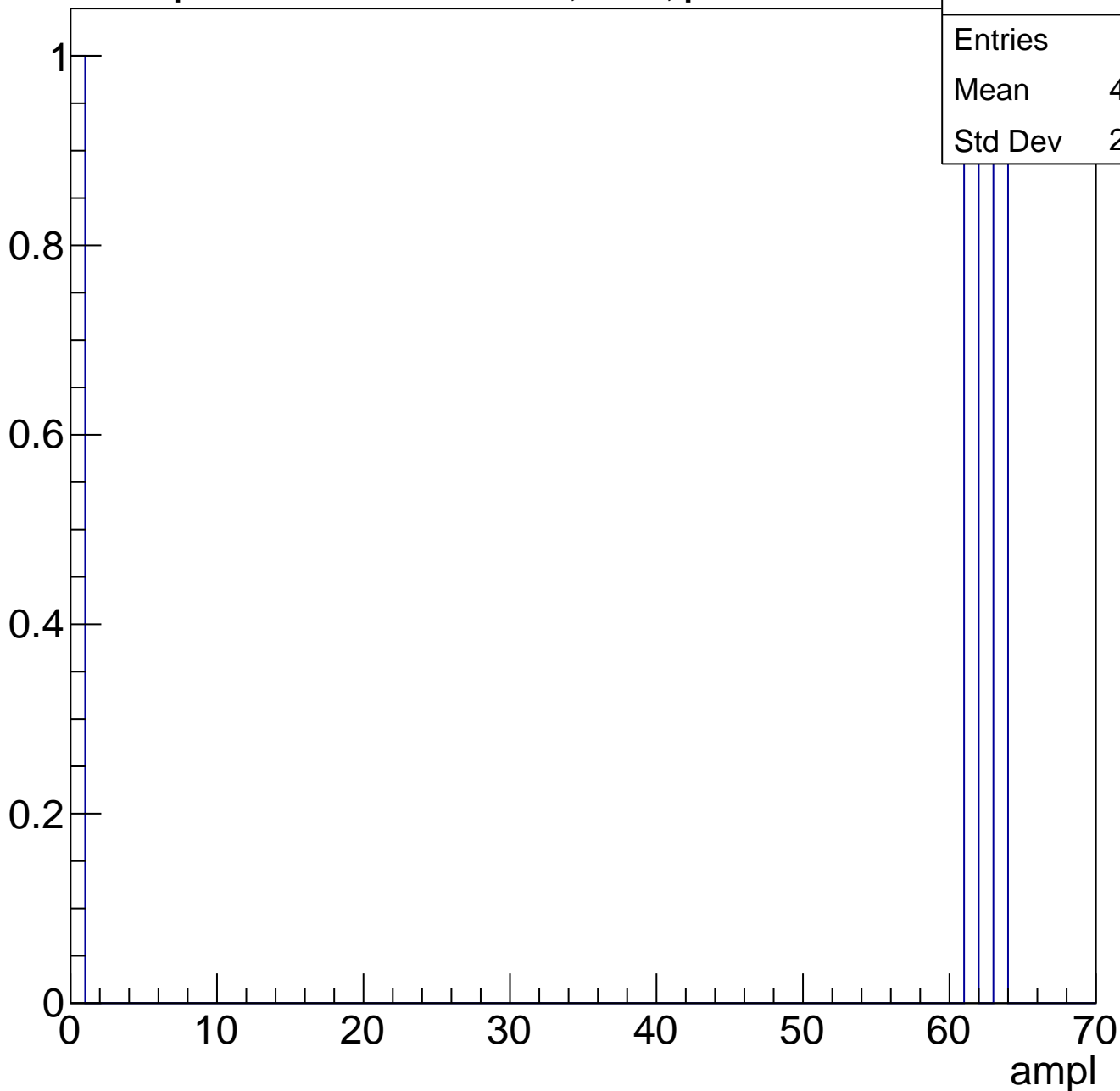




# B1L103S, U2-ch112, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch113, adc0

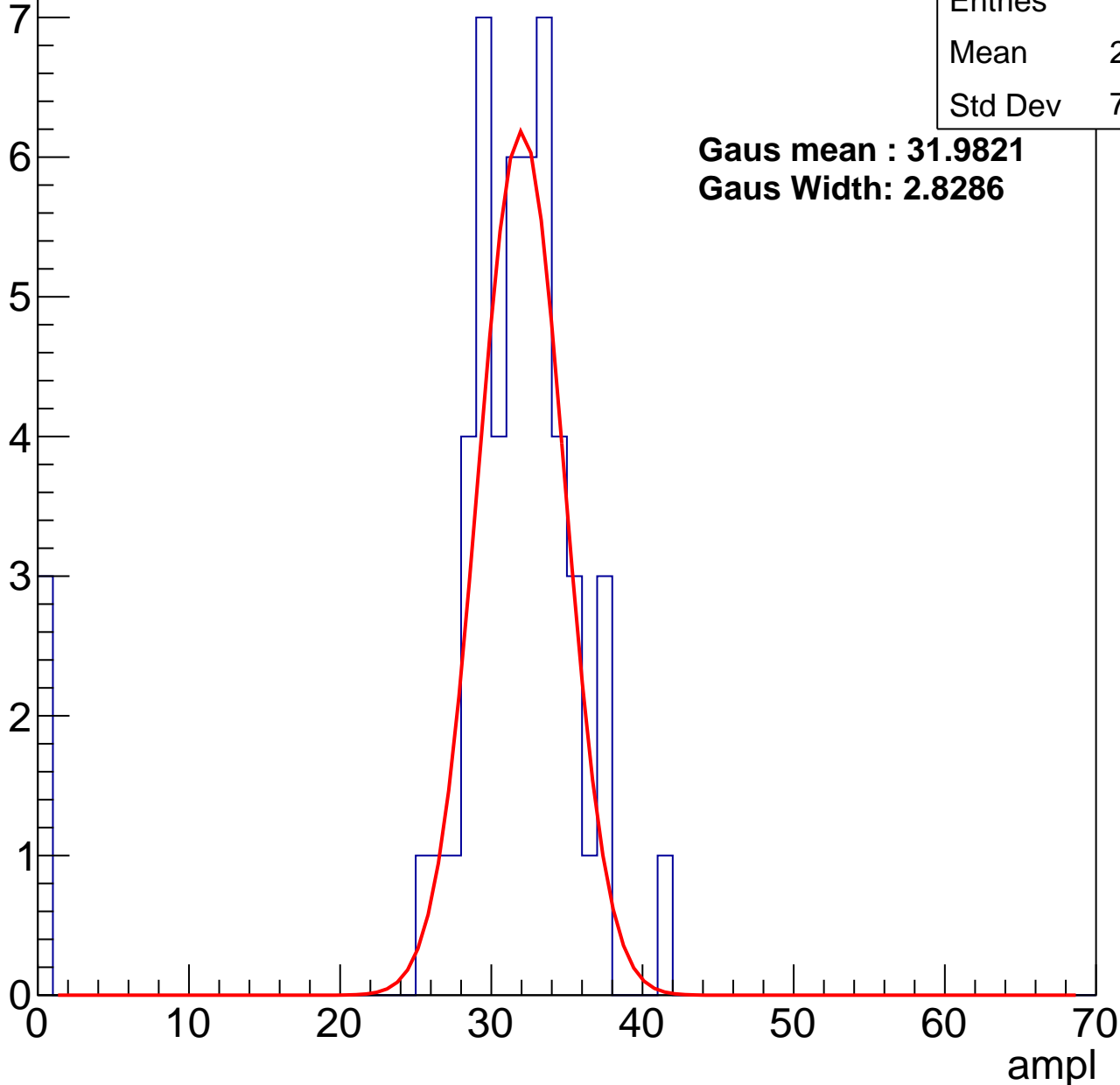
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	29.83
Std Dev	7.975

**Gaus mean : 31.9821**

**Gaus Width: 2.8286**



# B1L103S, U2-ch113, adc1

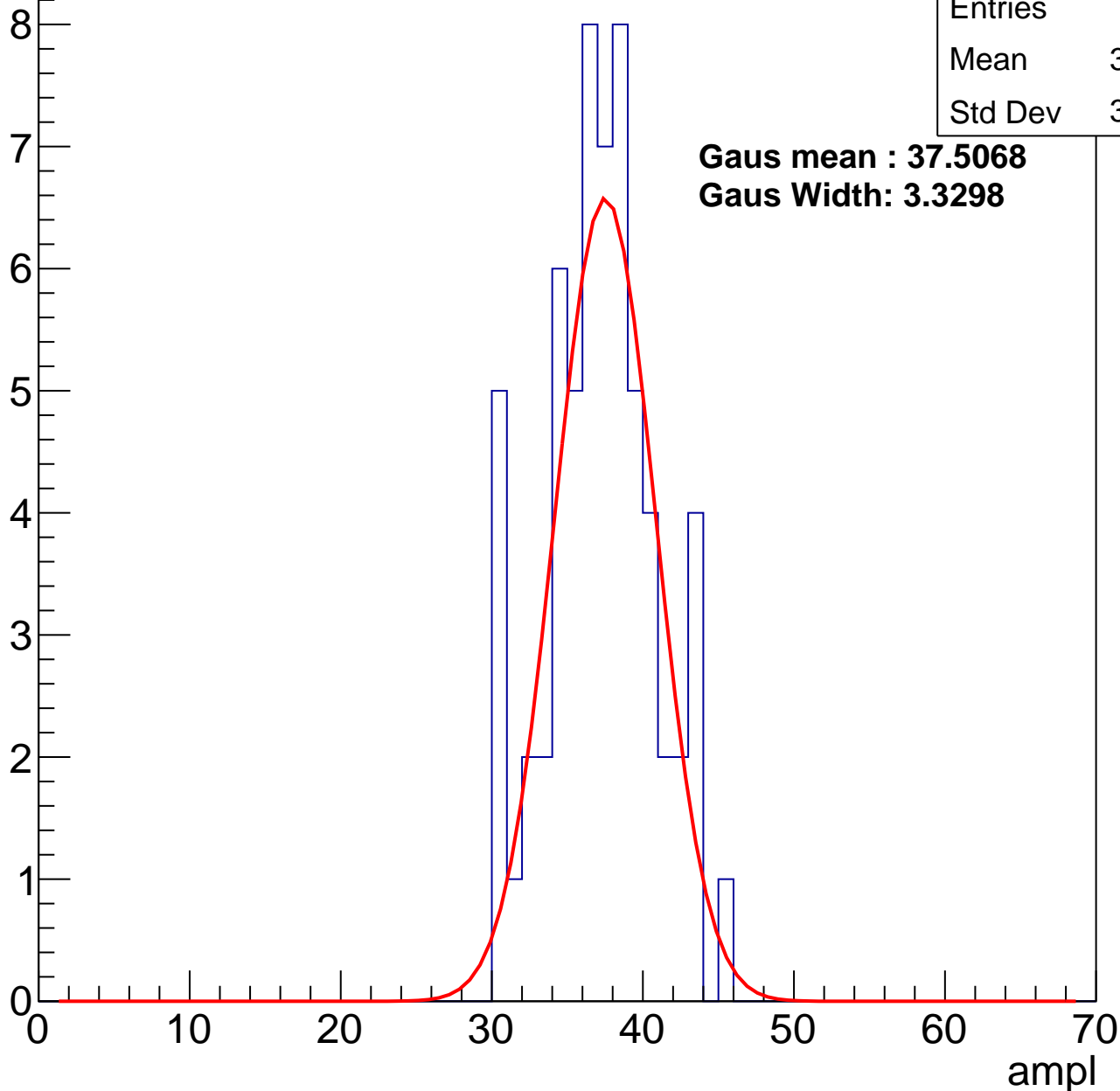
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	36.76
Std Dev	3.582

**Gaus mean : 37.5068**

**Gaus Width: 3.3298**



# B1L103S, U2-ch113, adc2

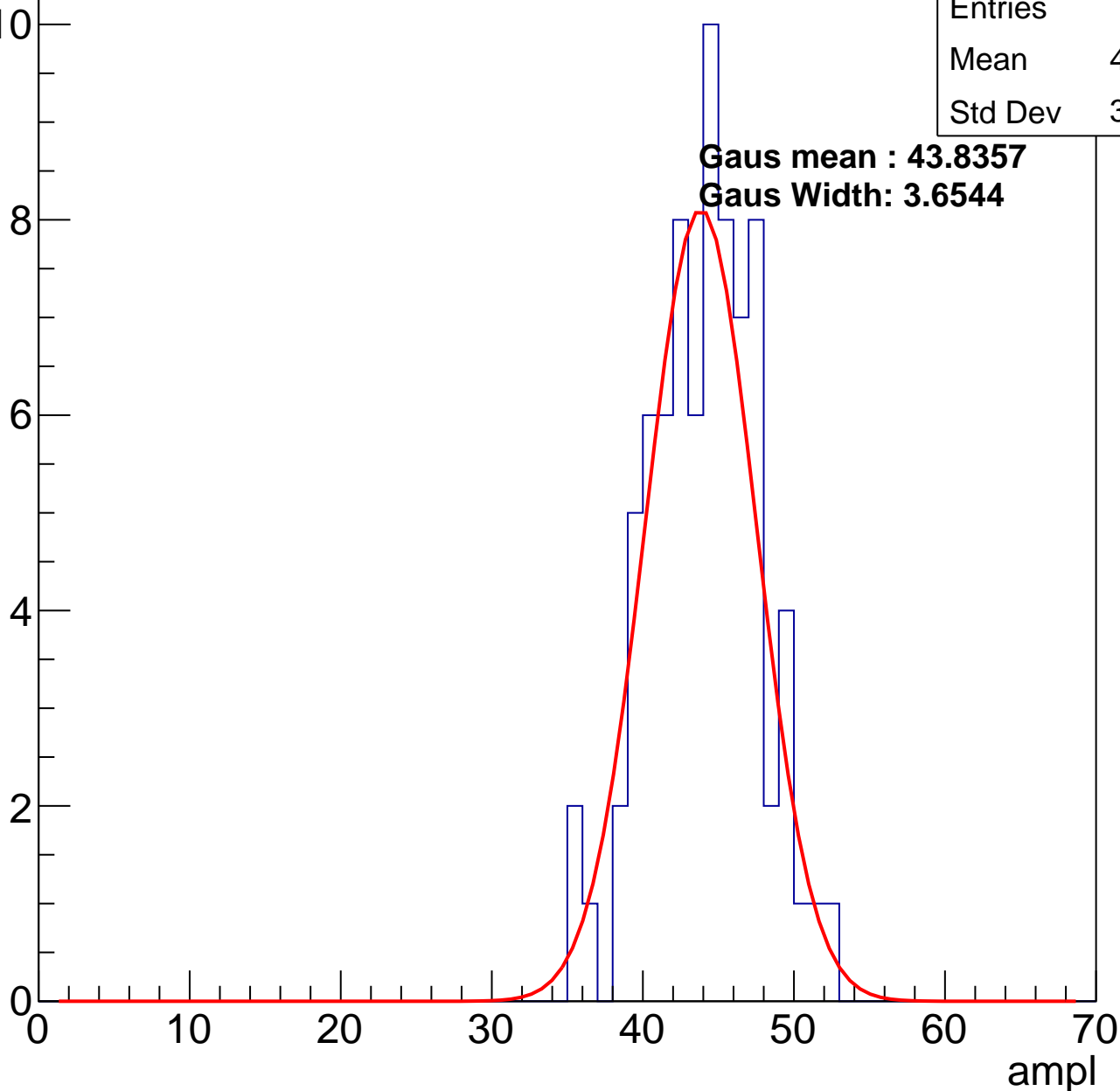
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	43.59
Std Dev	3.557

**Gaus mean : 43.8357**

**Gaus Width: 3.6544**

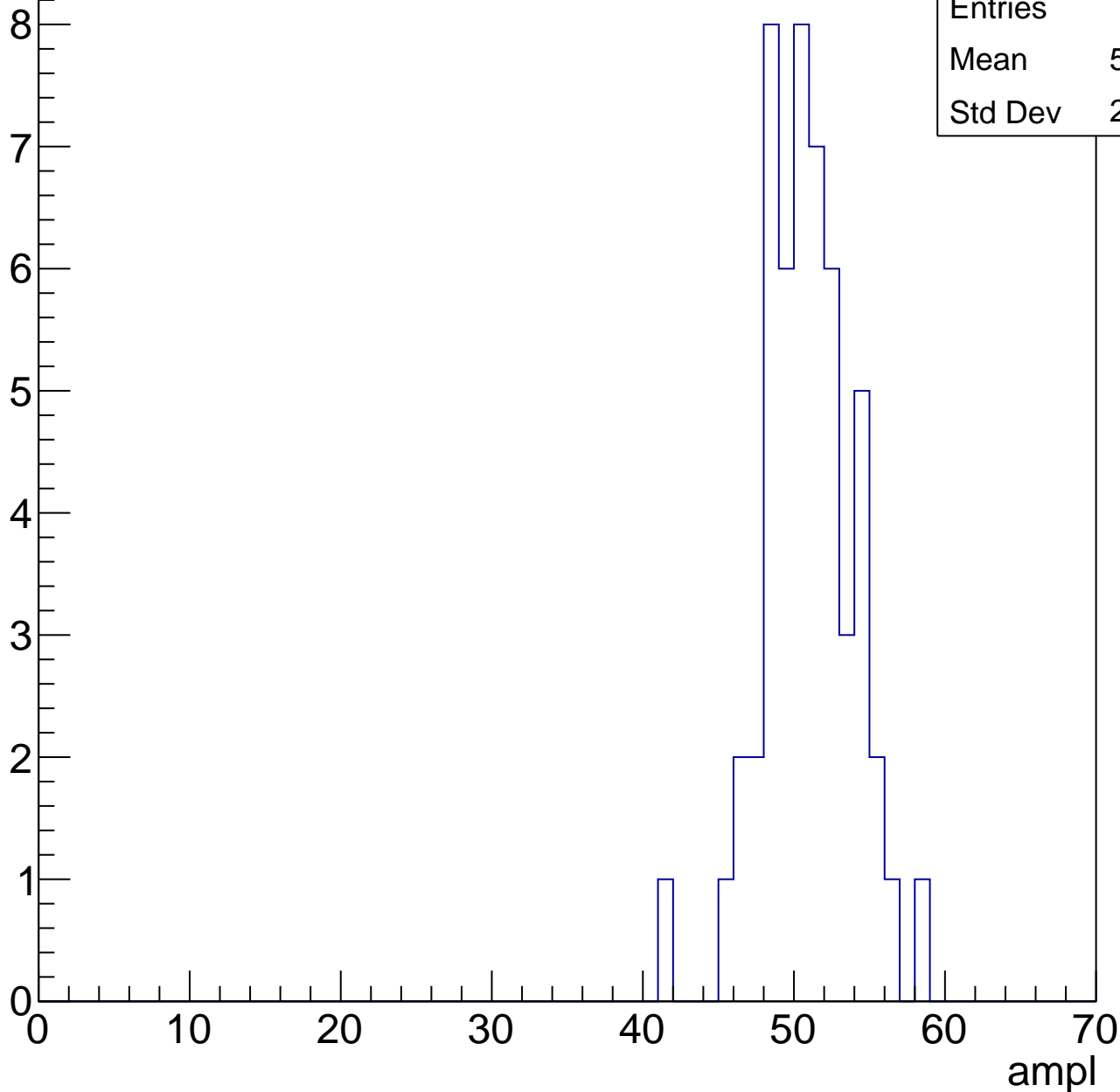


# B1L103S, U2-ch113, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	50.42
Std Dev	2.987

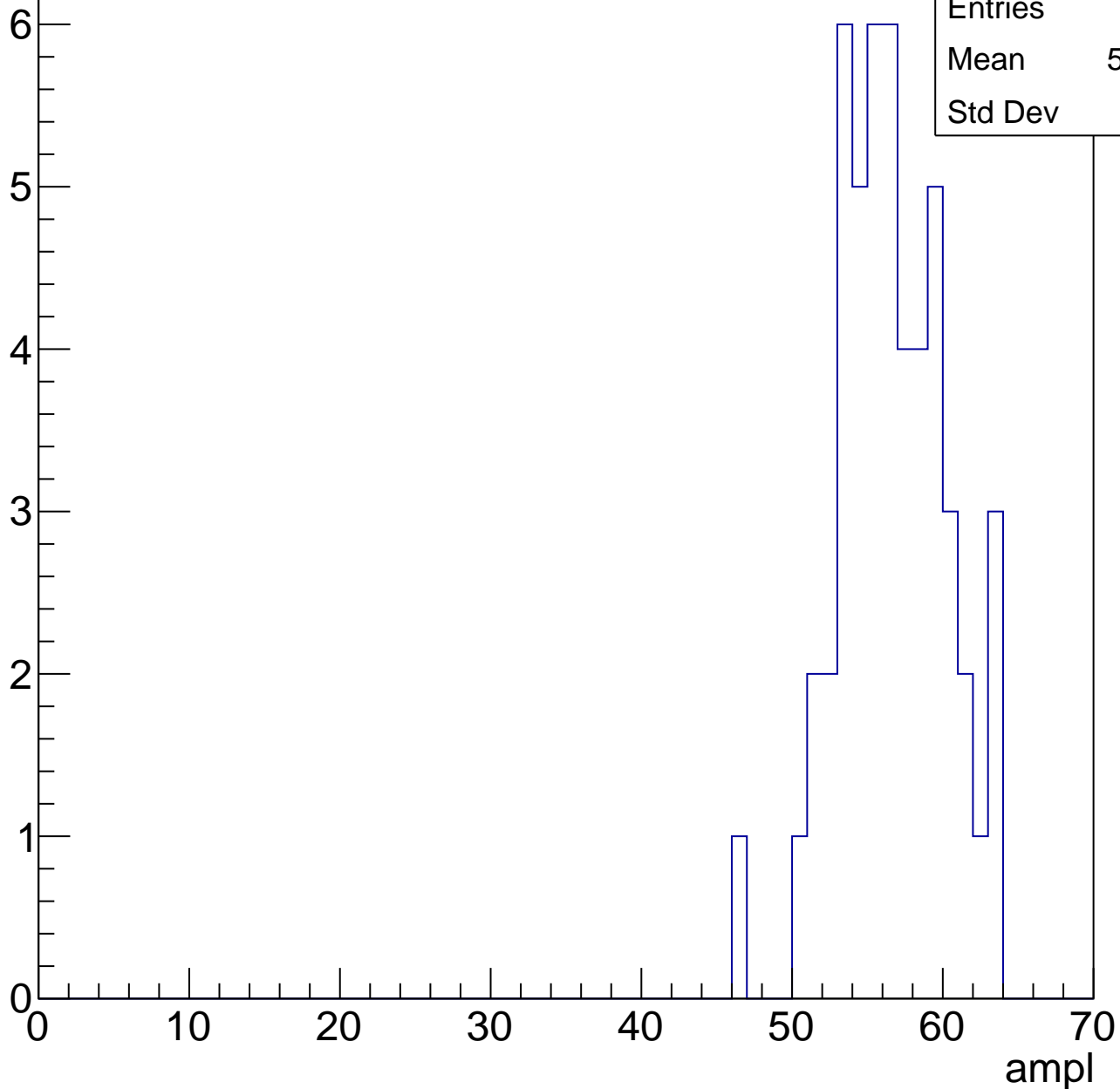


# B1L103S, U2-ch113, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	56.16
Std Dev	3.55

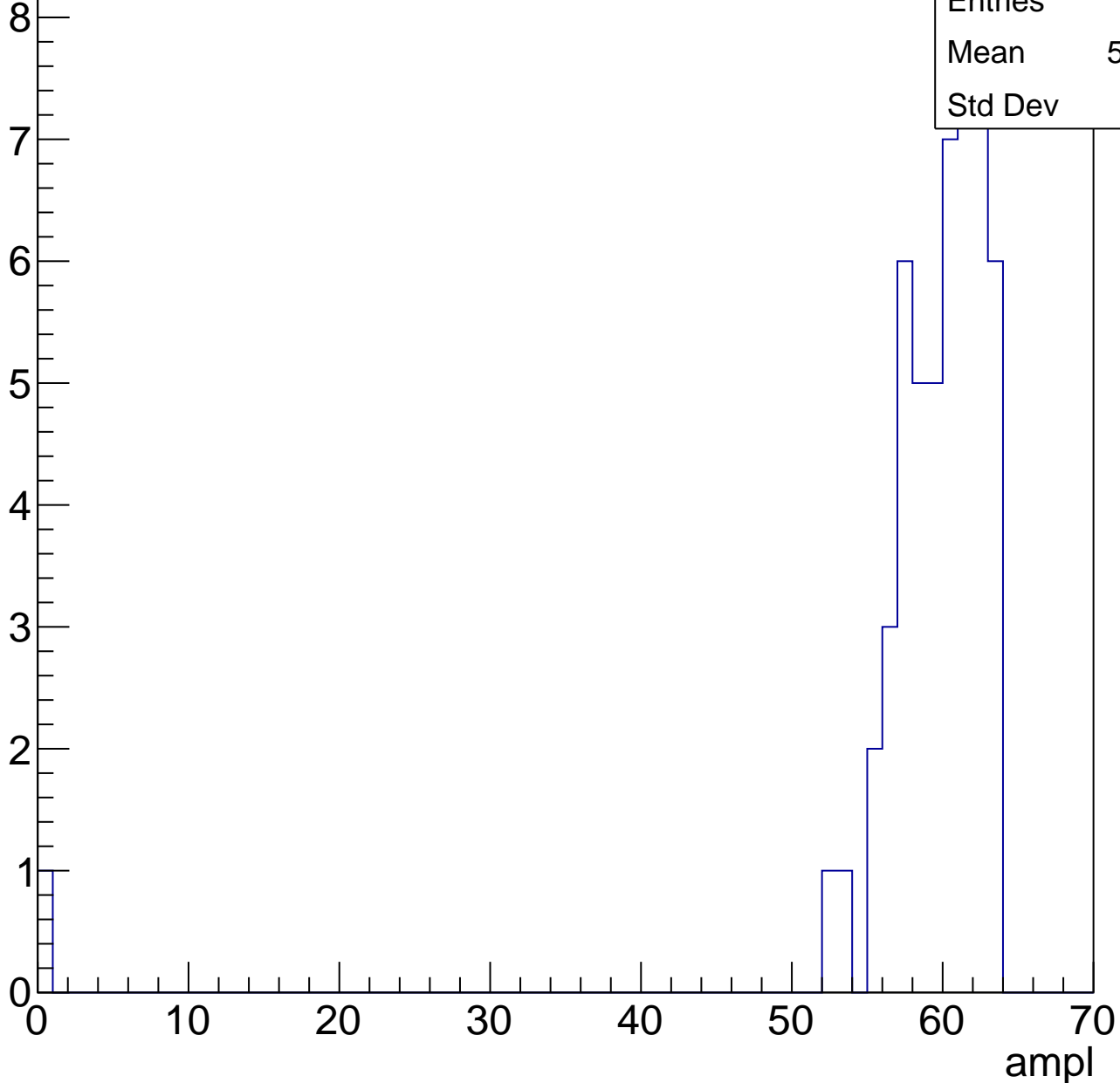


# B1L103S, U2-ch113, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	58.34
Std Dev	8.51



# B1L103S, U2-ch113, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U2-ch113, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U2-ch114, adc0

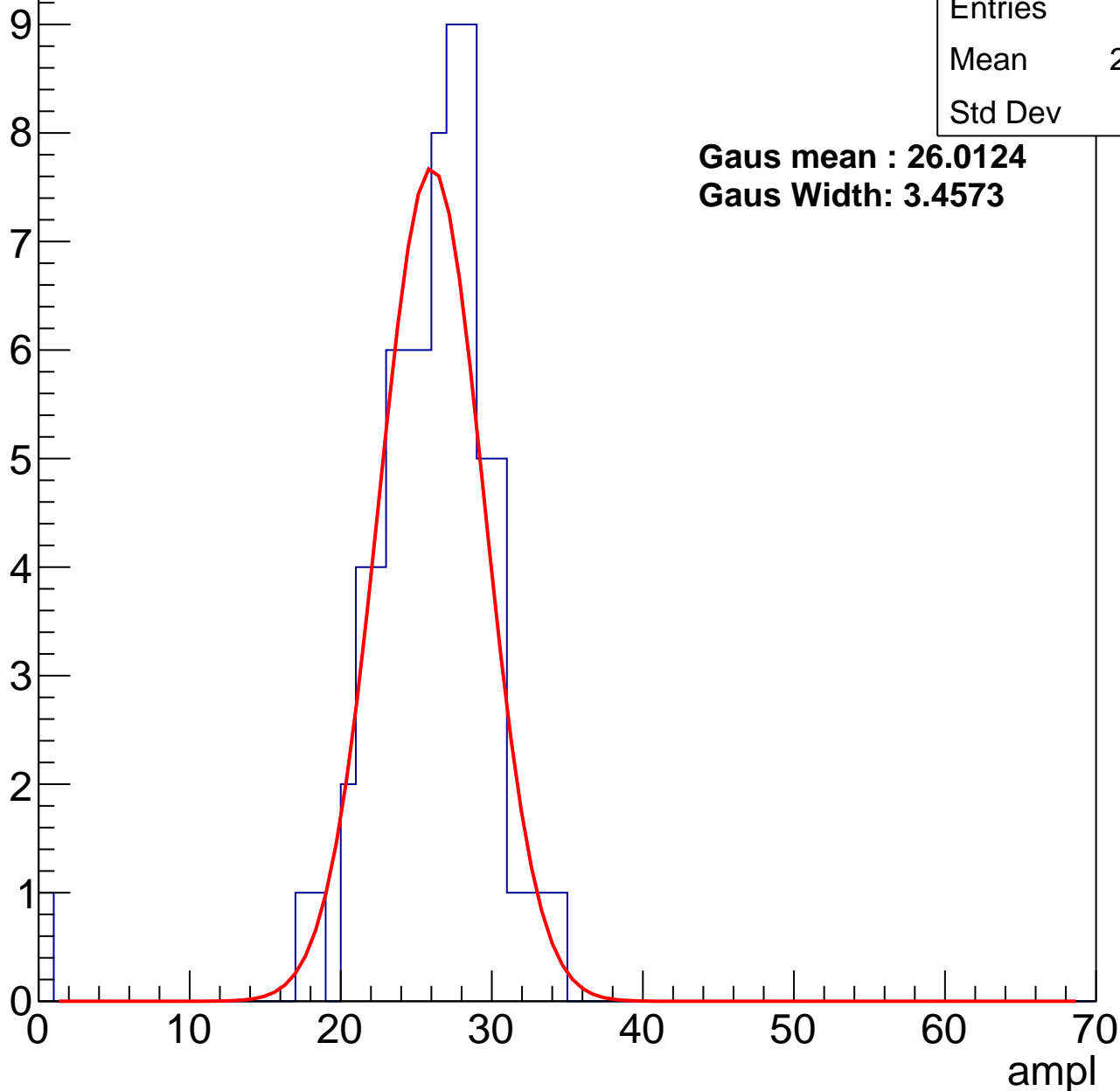
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	25.45
Std Dev	4.54

**Gaus mean : 26.0124**

**Gaus Width: 3.4573**



# B1L103S, U2-ch114, adc1

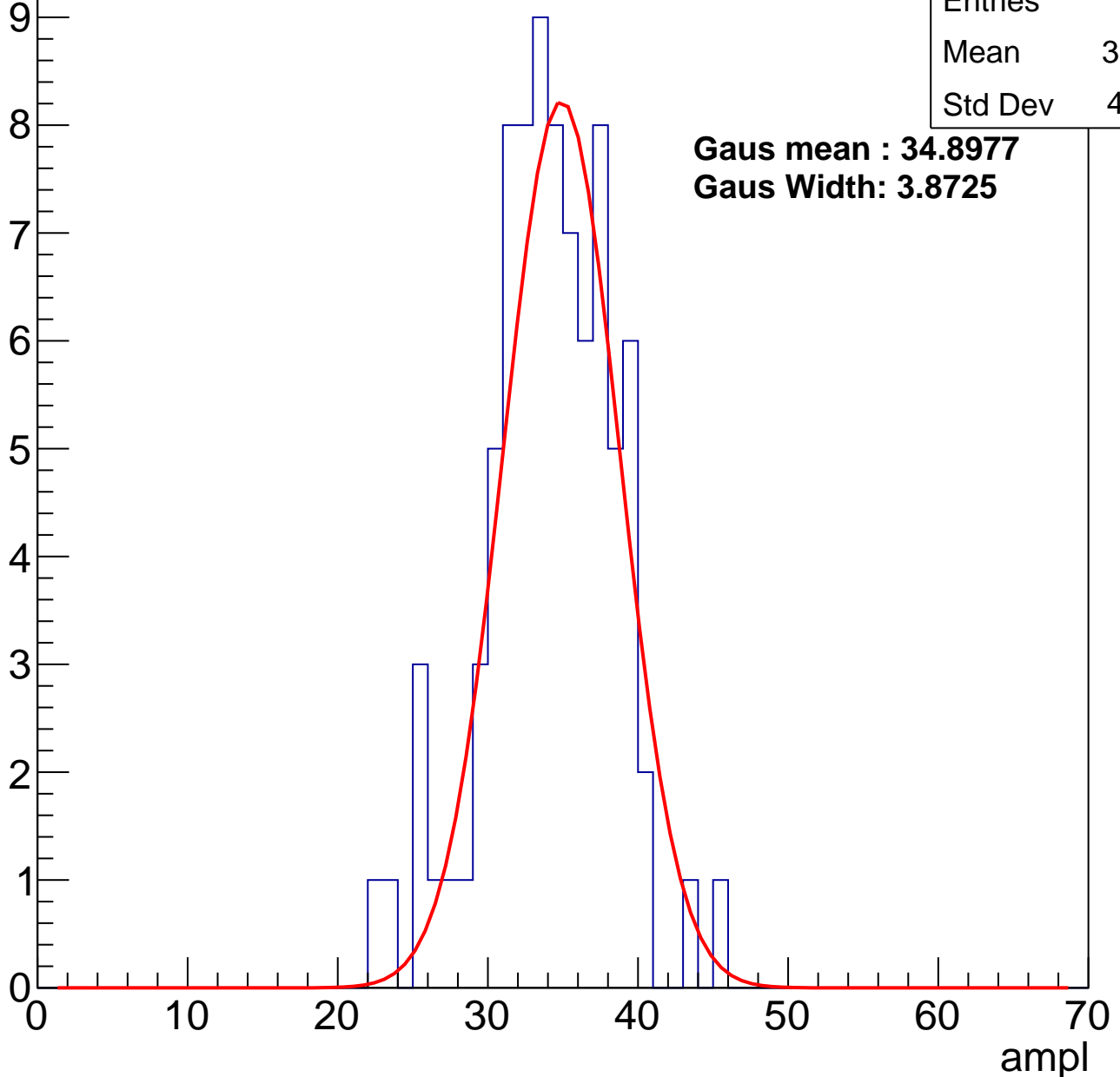
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	85
Mean	33.65
Std Dev	4.231

**Gaus mean : 34.8977**

**Gaus Width: 3.8725**



# B1L103S, U2-ch114, adc2

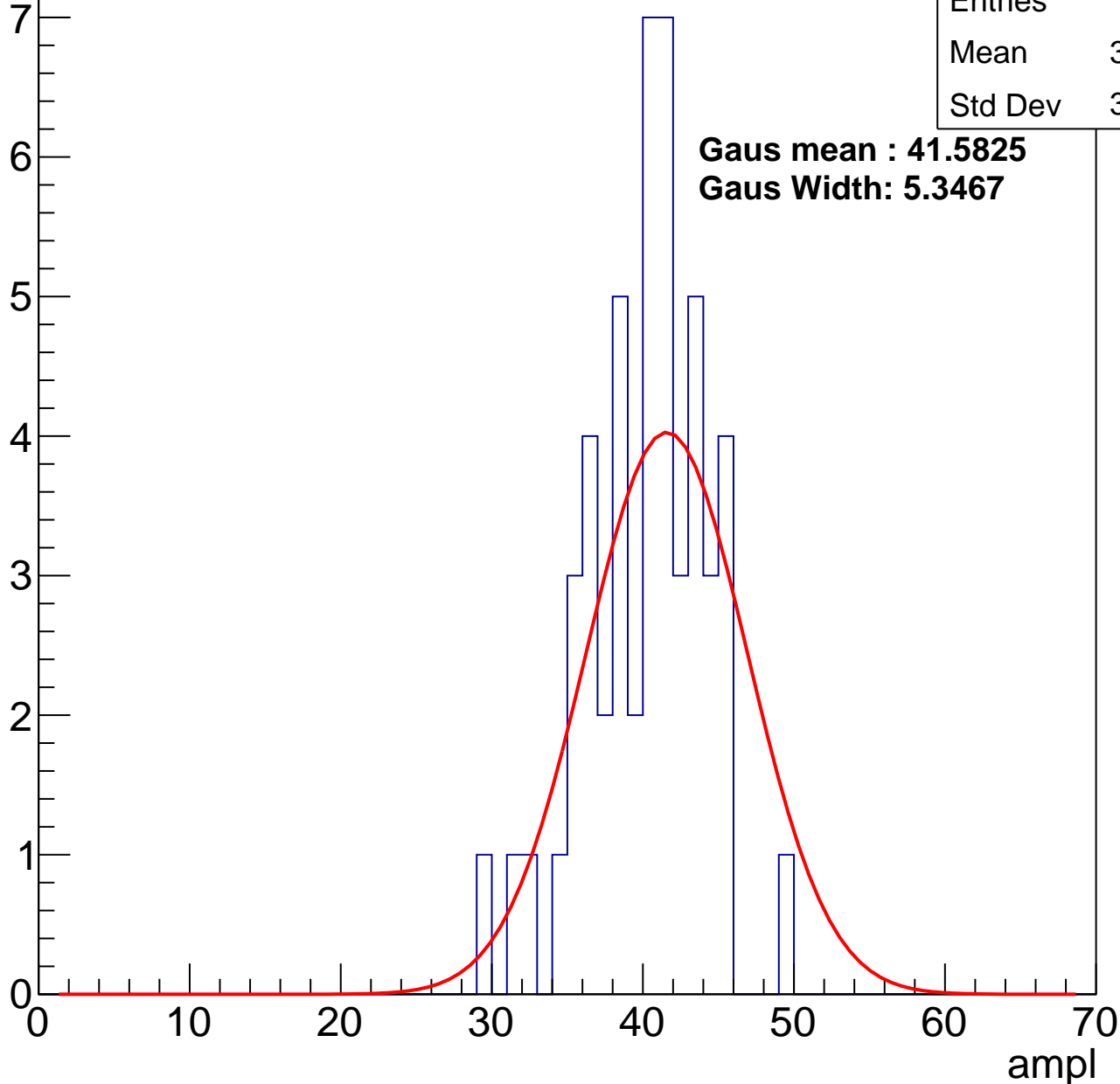
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	39.72
Std Dev	3.924

**Gaus mean : 41.5825**

**Gaus Width: 5.3467**

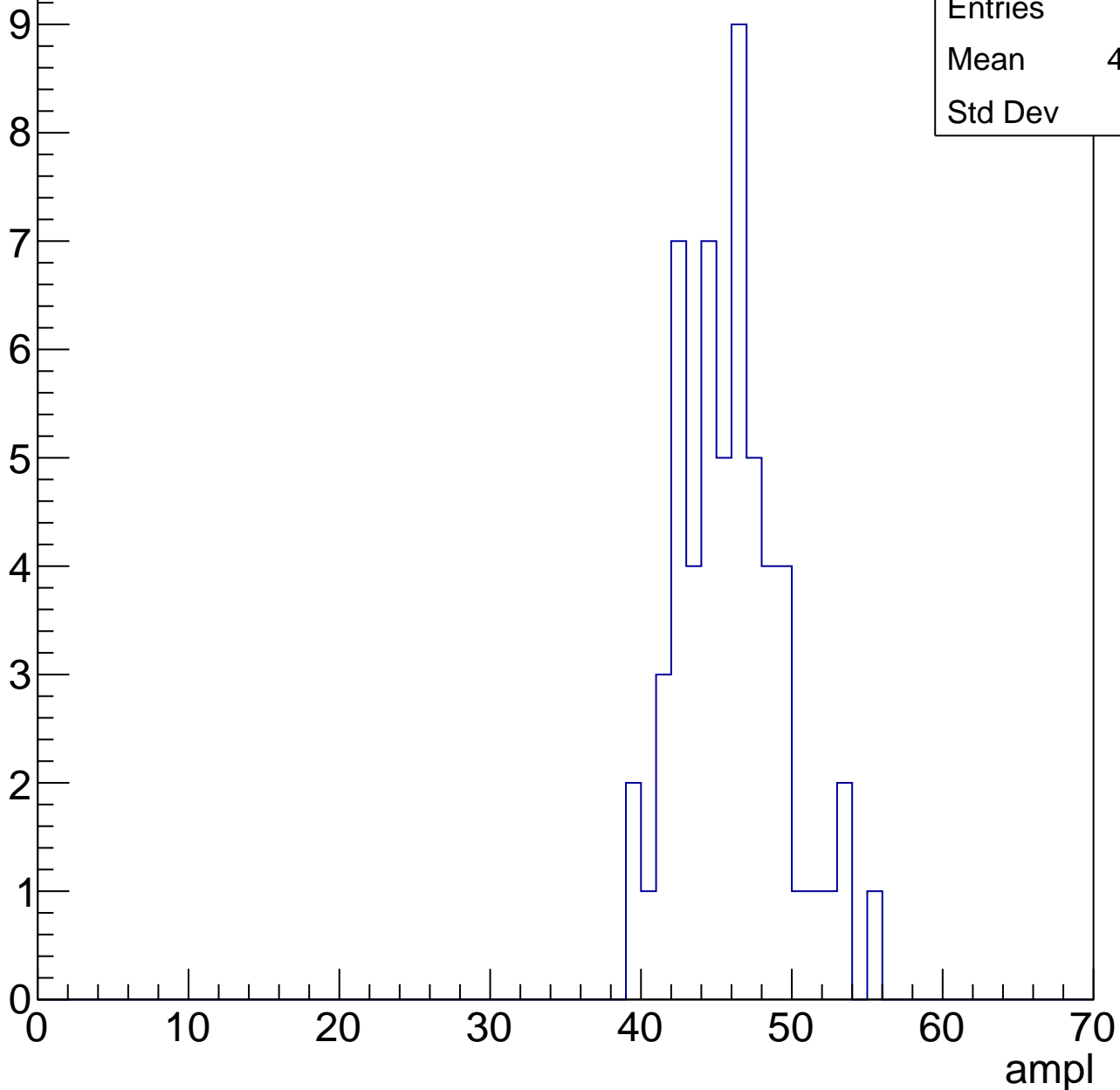


# B1L103S, U2-ch114, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	45.46
Std Dev	3.47

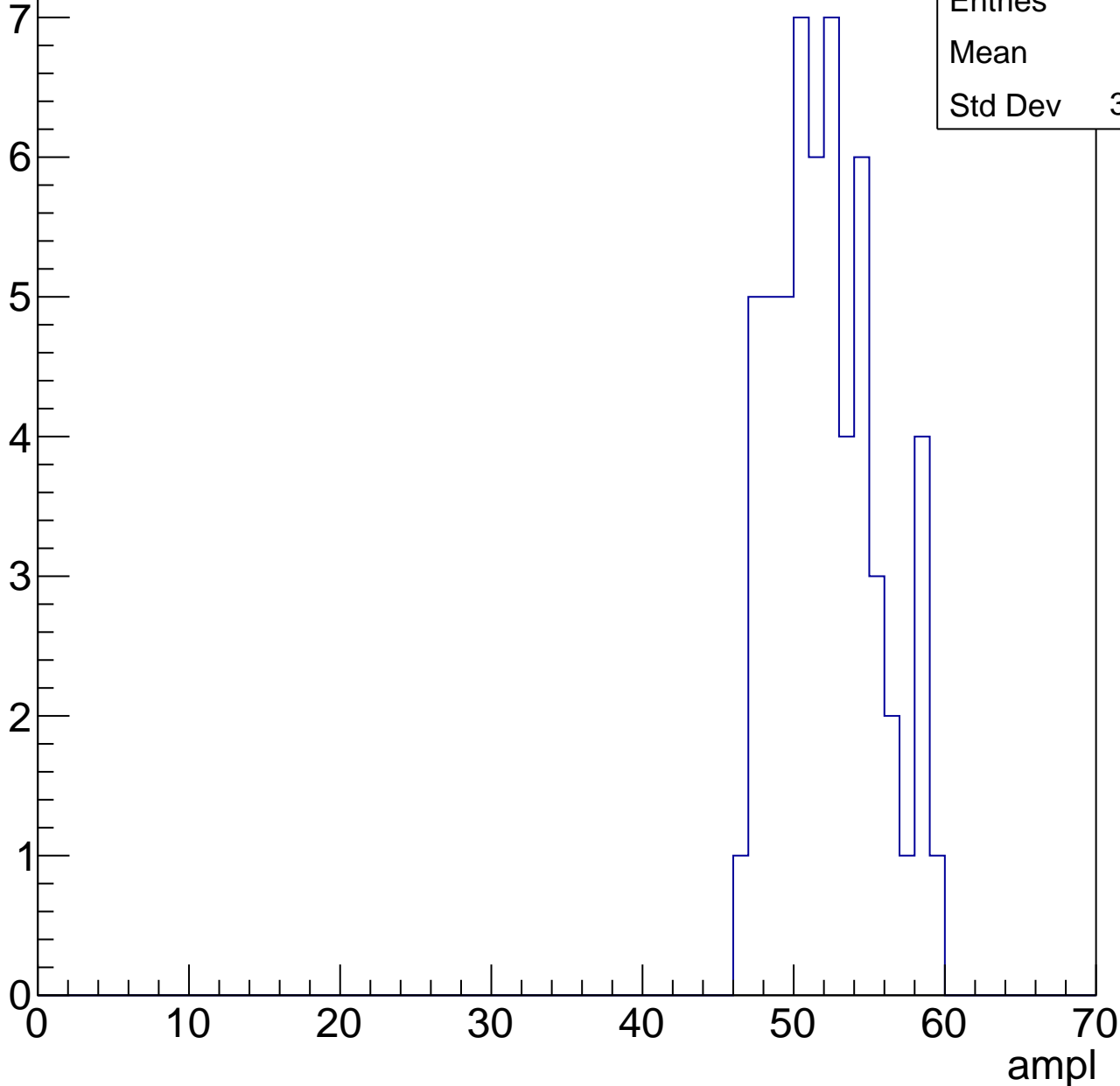


# B1L103S, U2-ch114, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	51.7
Std Dev	3.298

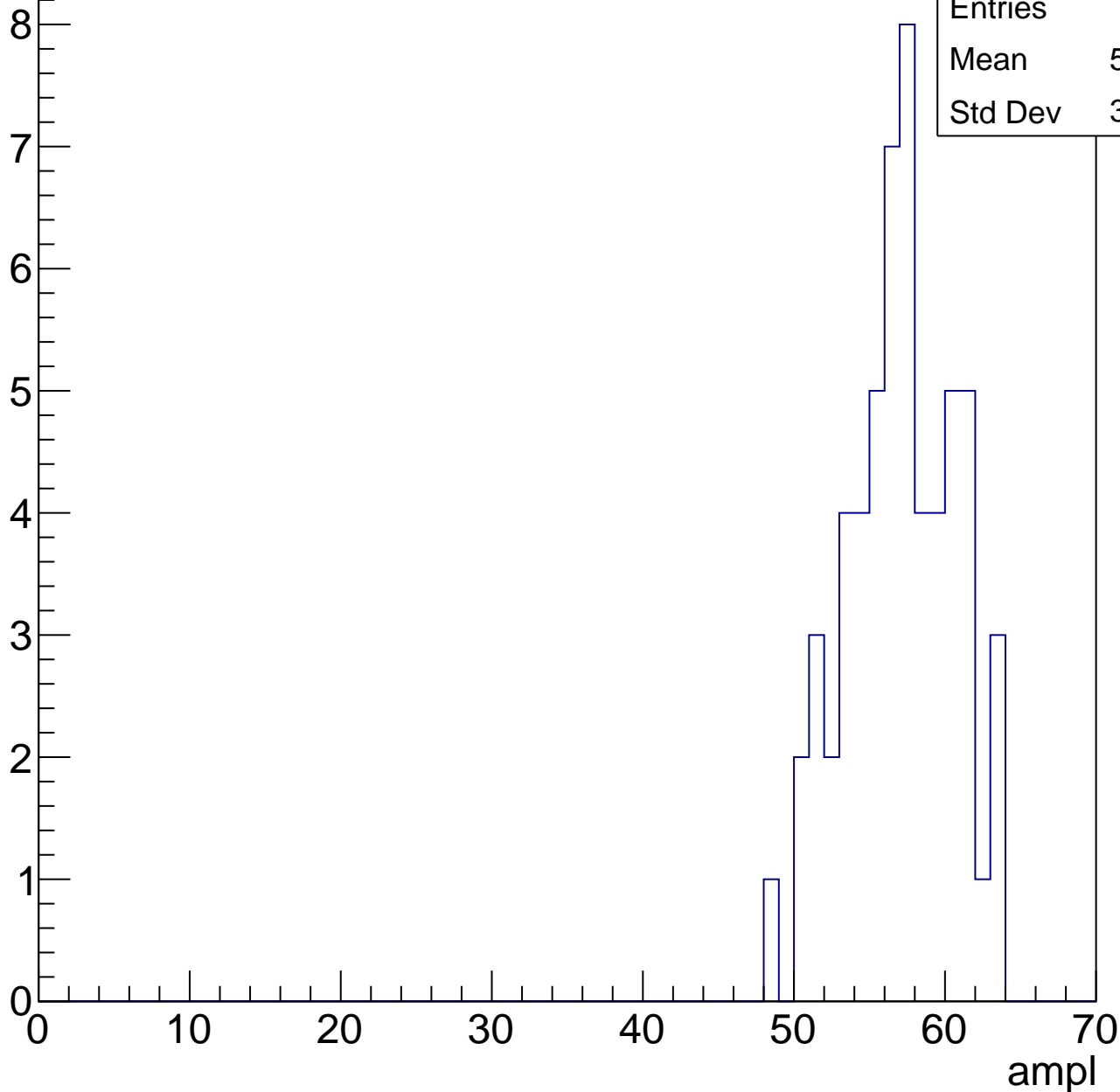


# B1L103S, U2-ch114, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	56.55
Std Dev	3.549

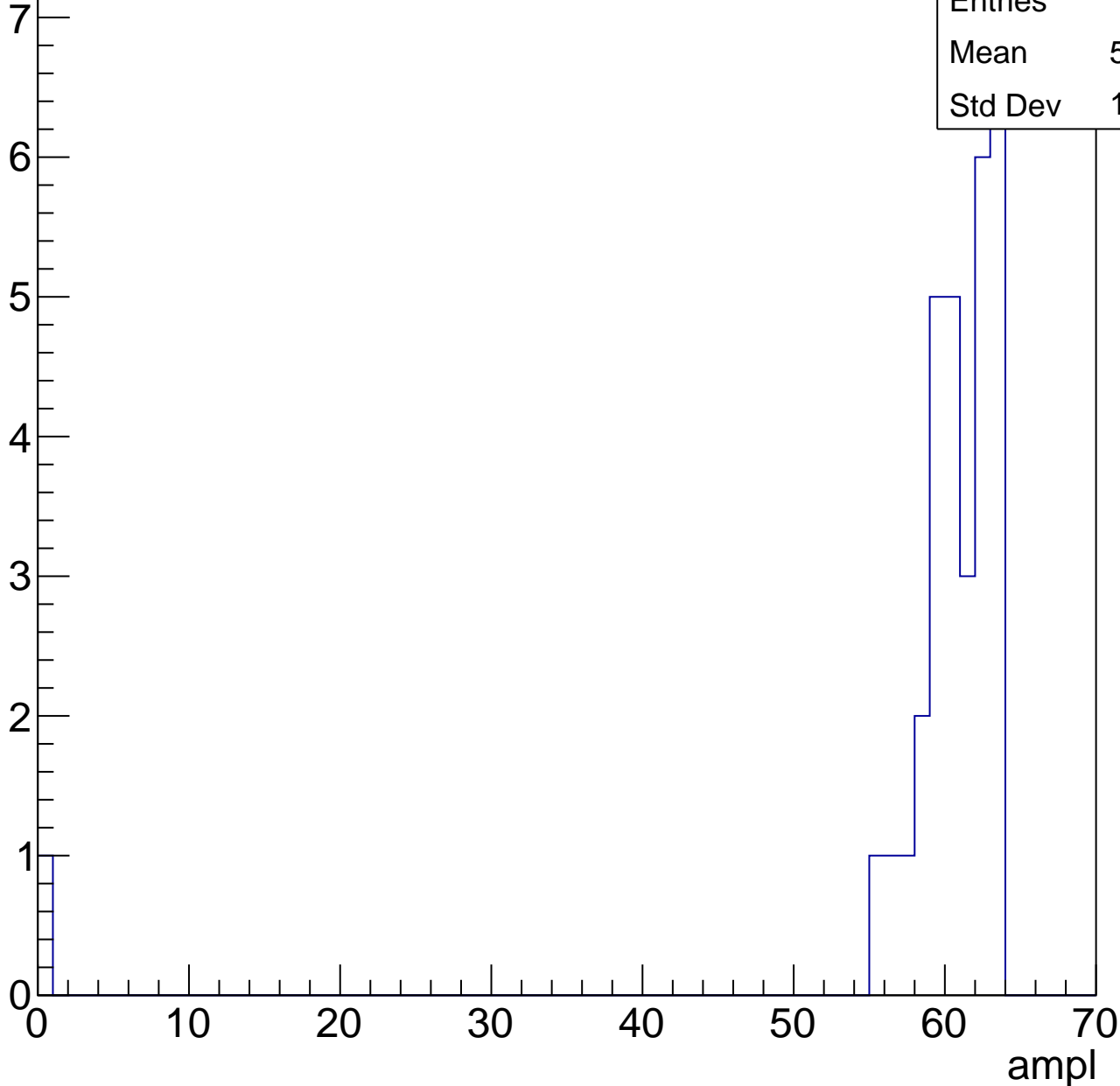


# B1L103S, U2-ch114, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	32
Mean	58.59
Std Dev	10.74

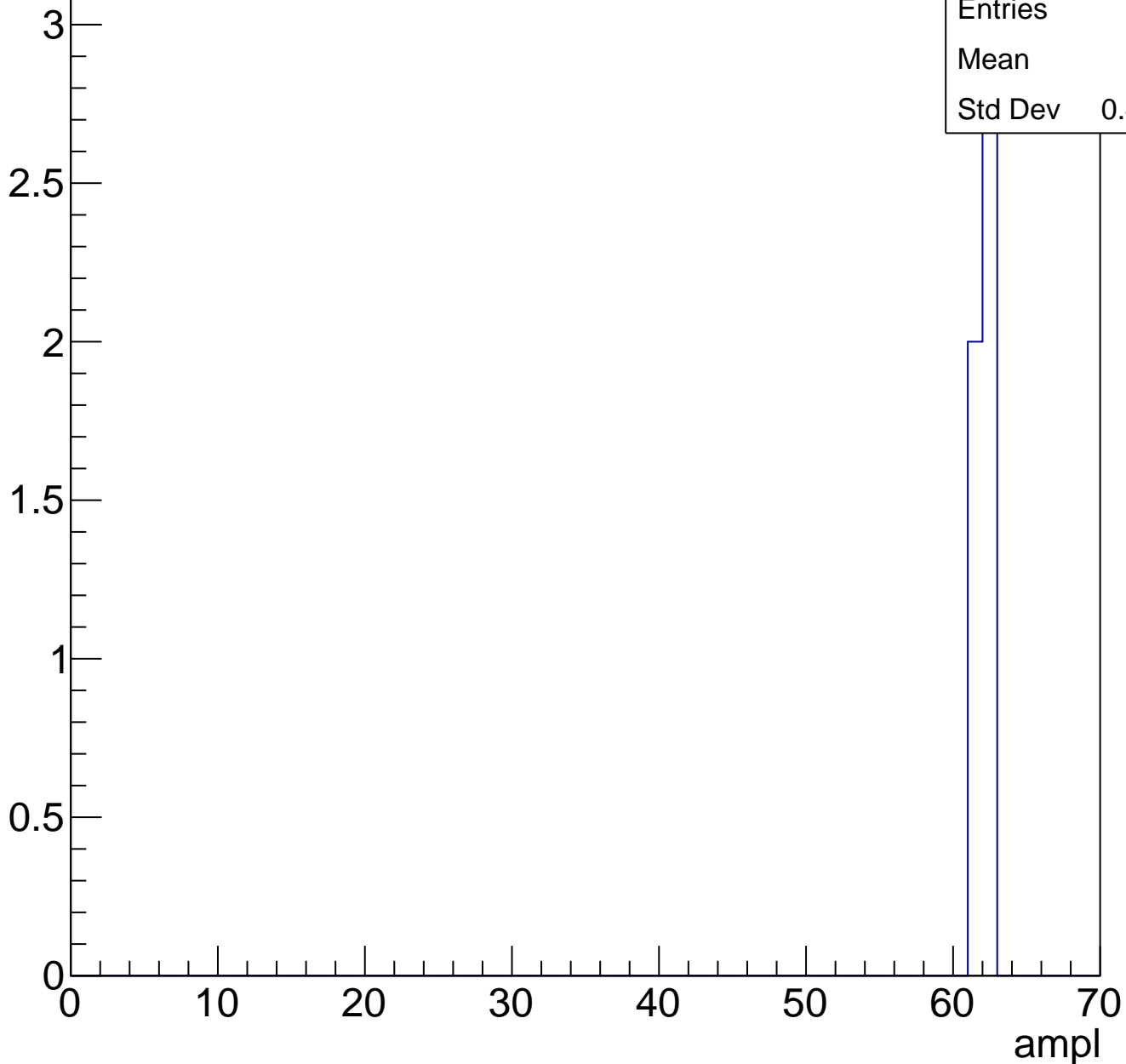




# B1L103S, U2-ch114, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch115, adc0

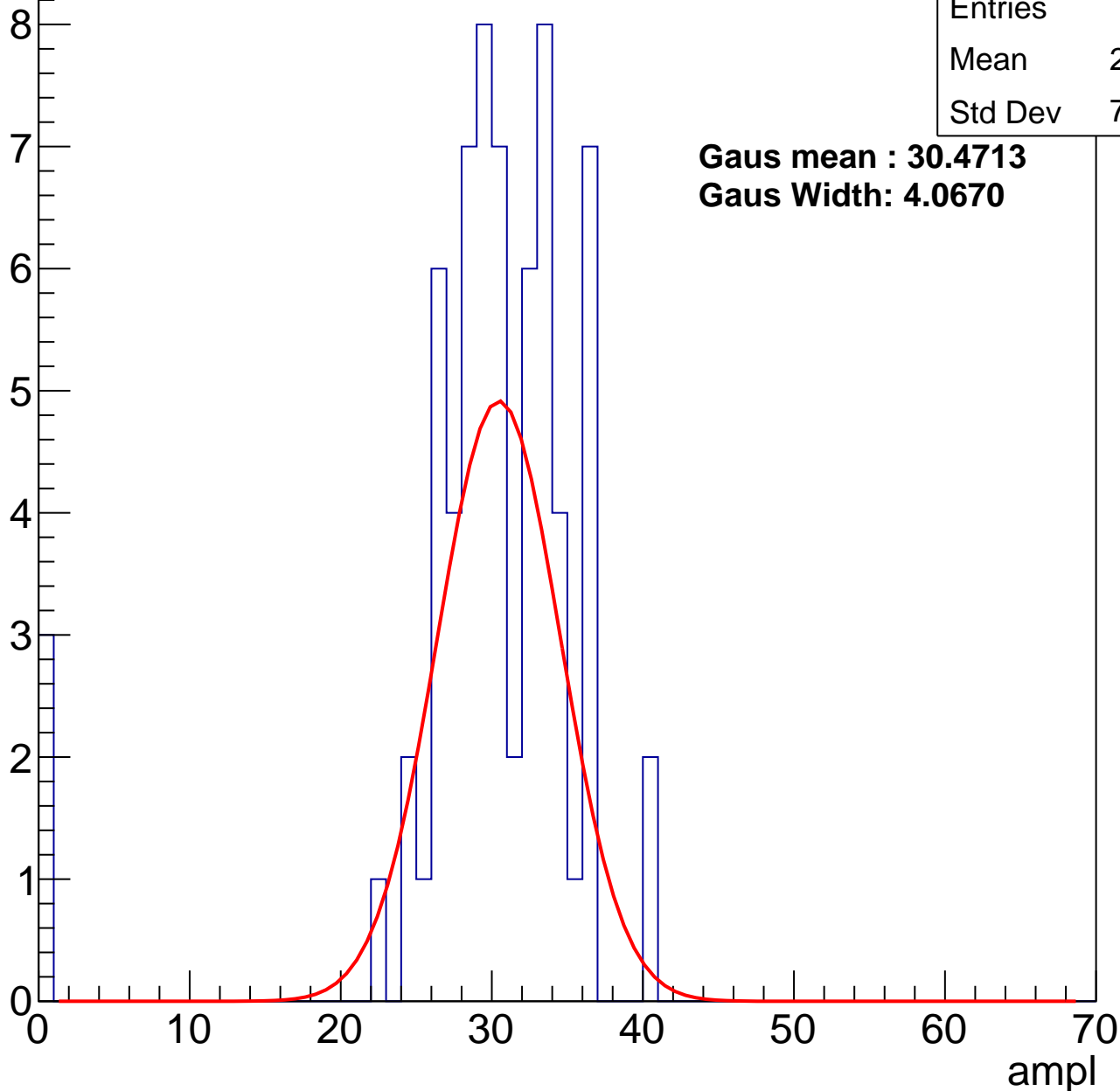
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	29.25
Std Dev	7.252

**Gaus mean : 30.4713**

**Gaus Width: 4.0670**

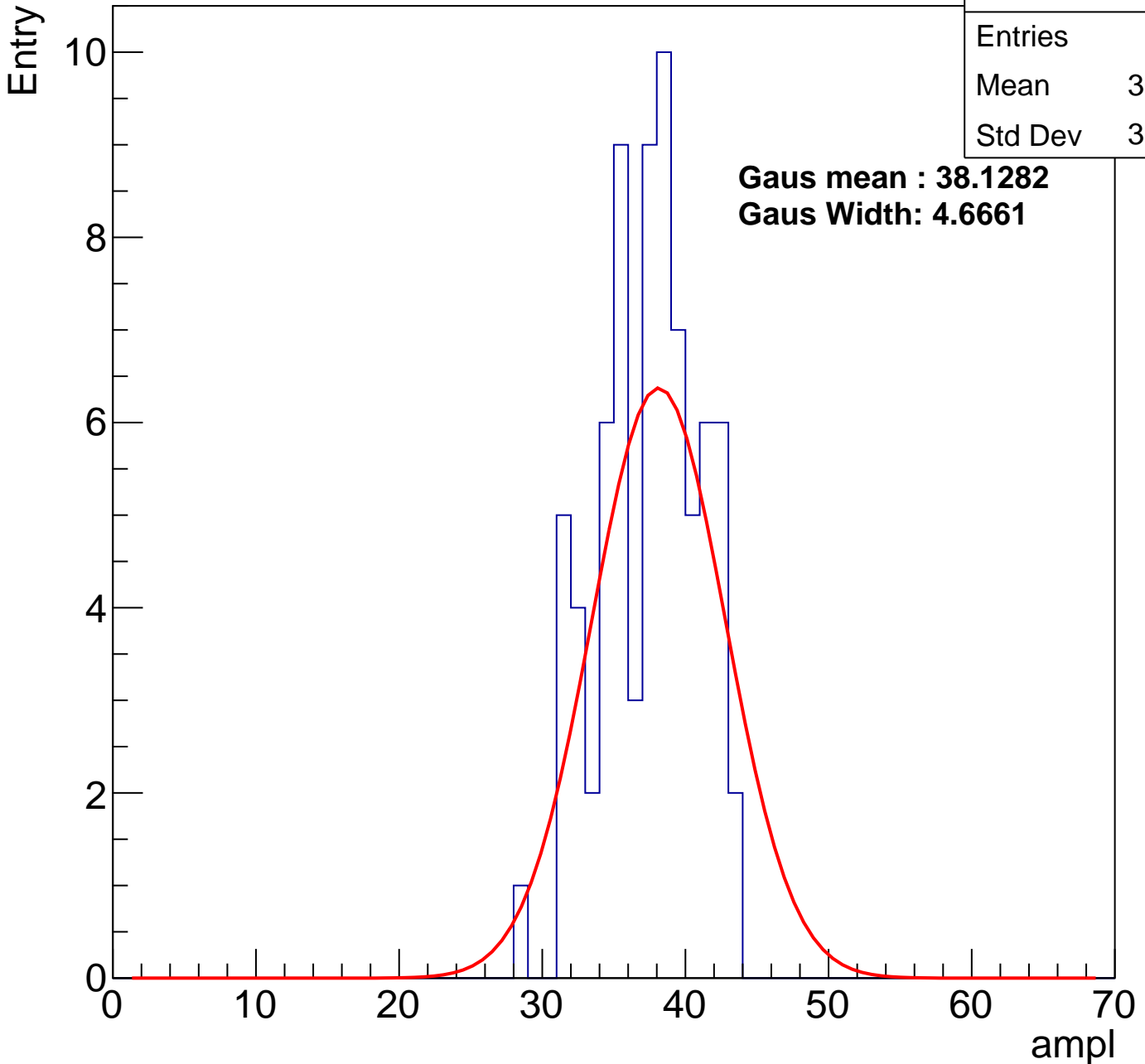


# B1L103S, U2-ch115, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	75
Mean	36.99
Std Dev	3.439

**Gaus mean : 38.1282**  
**Gaus Width: 4.6661**



# B1L103S, U2-ch115, adc2

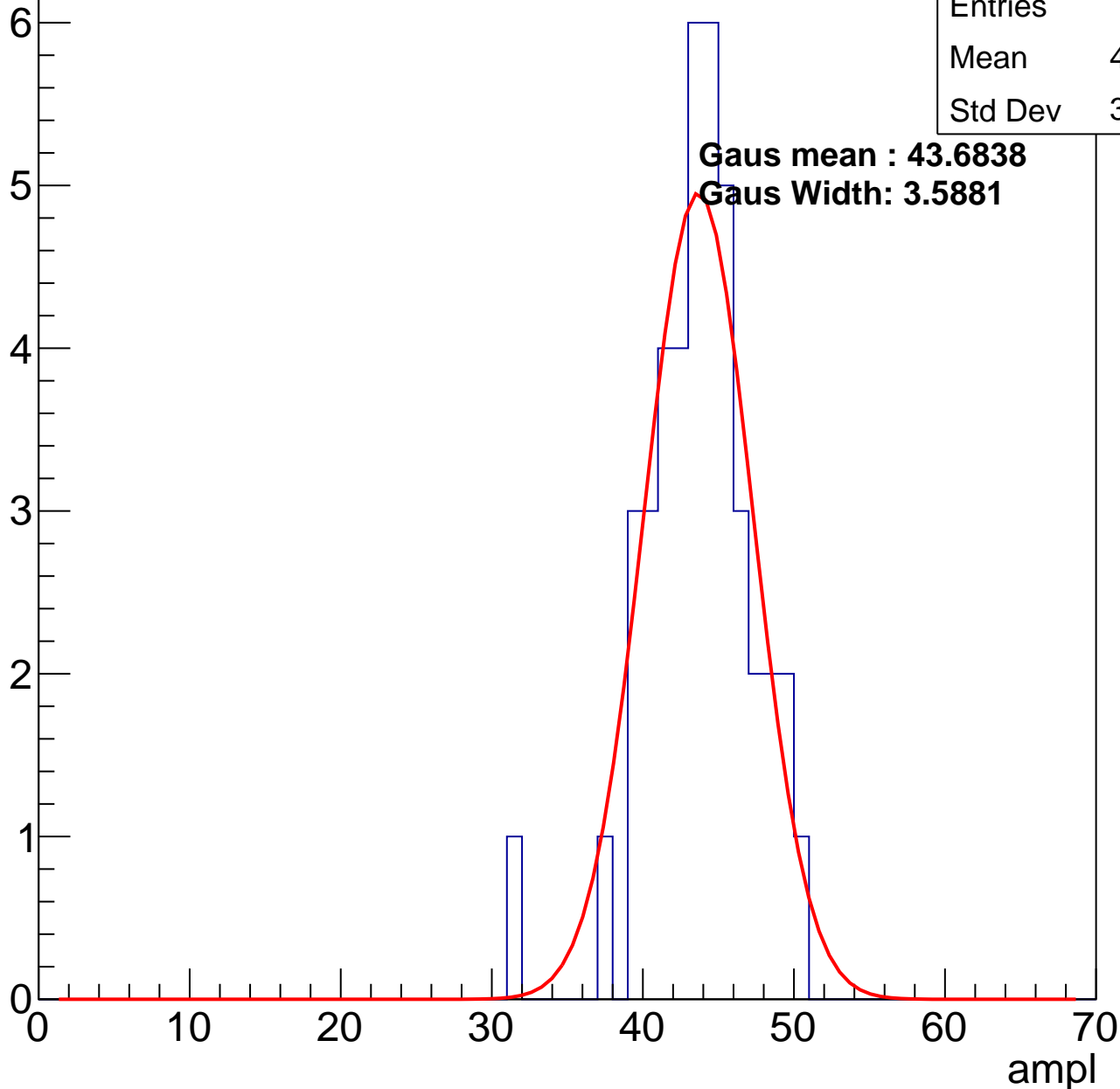
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	43
Mean	43.26
Std Dev	3.505

**Gaus mean : 43.6838**

**Gaus Width: 3.5881**

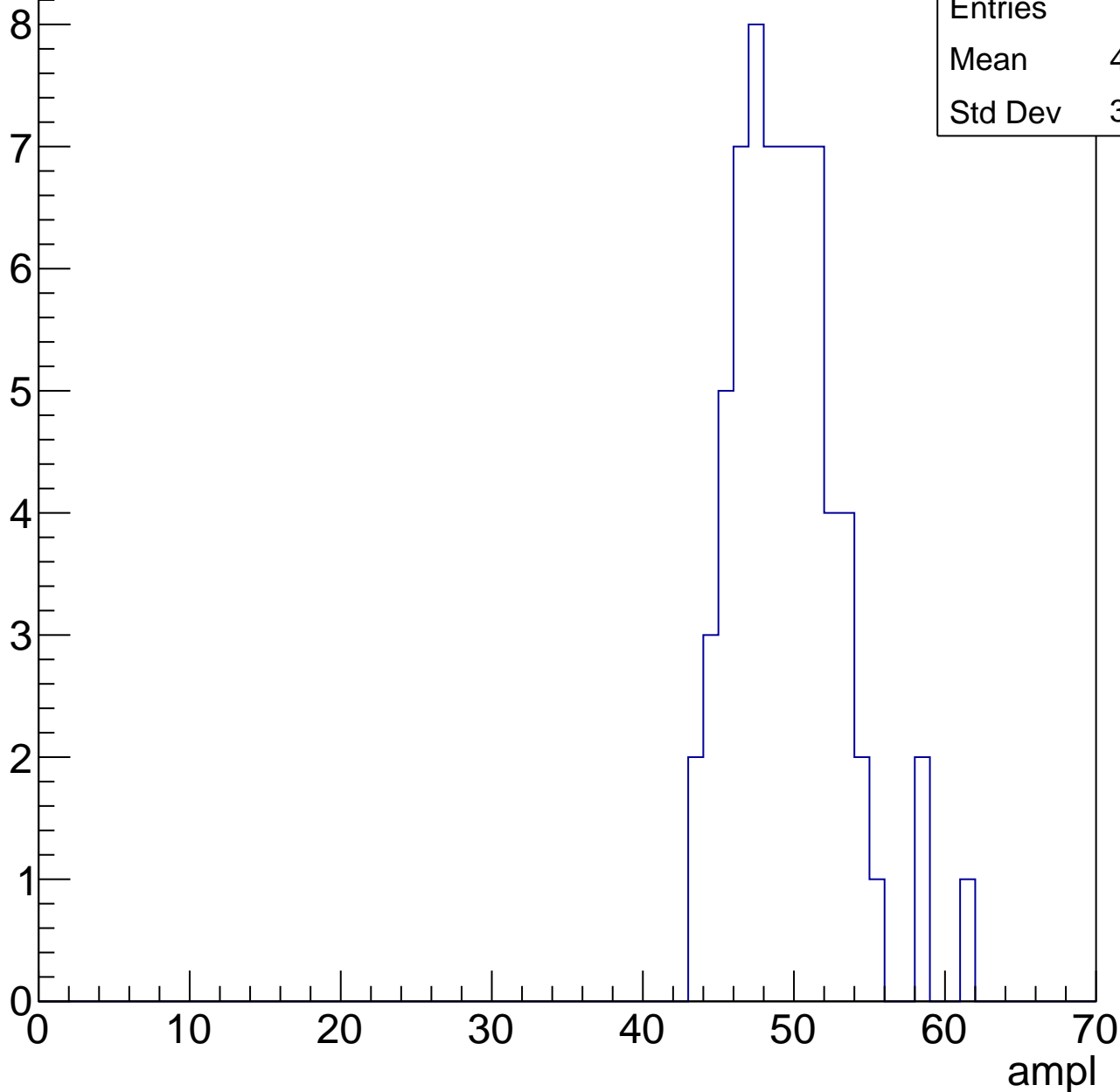


# B1L103S, U2-ch115, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

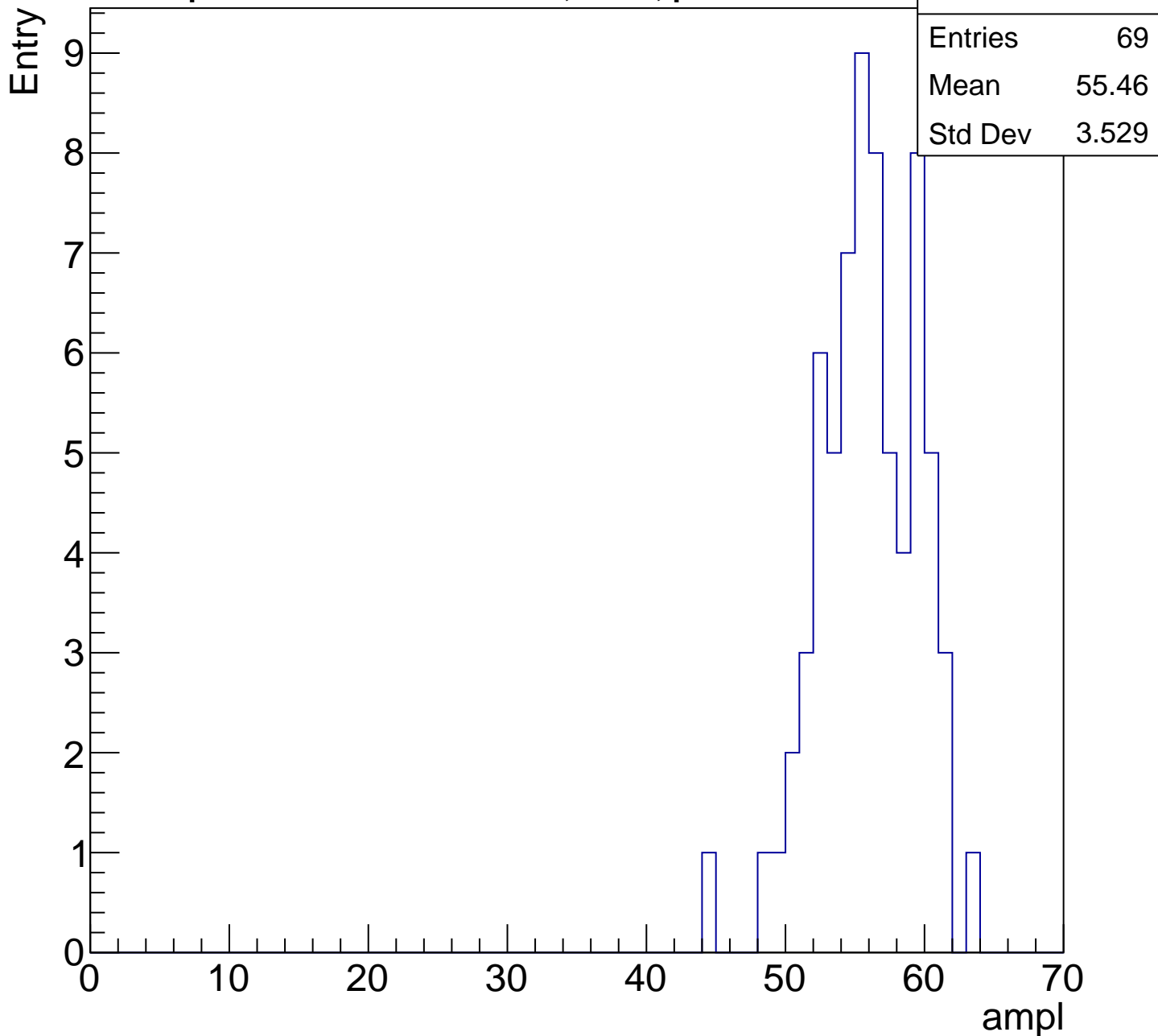
Entry

Entries	67
Mean	49.06
Std Dev	3.574



# B1L103S, U2-ch115, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

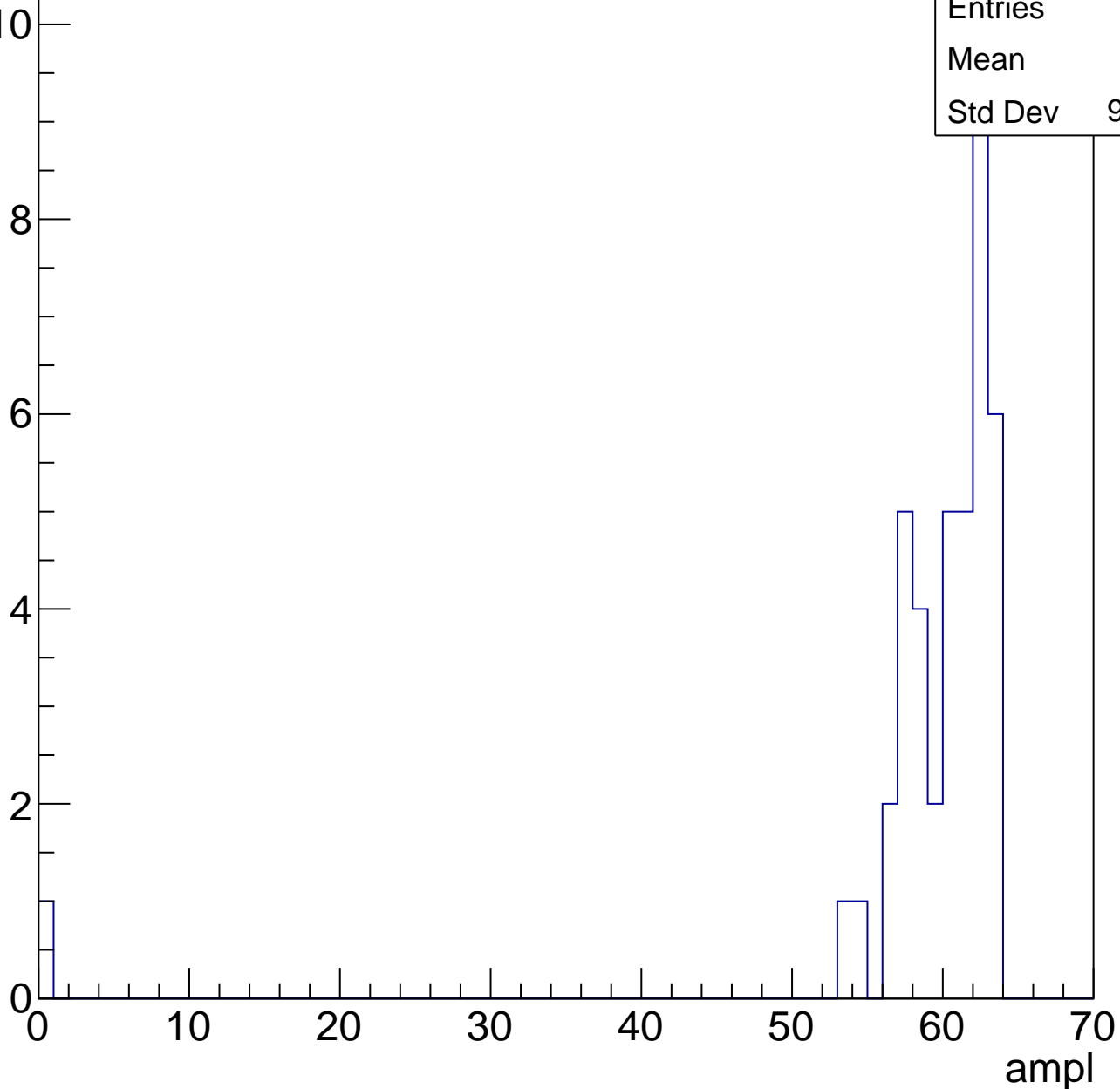


# B1L103S, U2-ch115, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	42
Mean	58.5
Std Dev	9.492



# B1L103S, U2-ch115, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U2-ch115, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch116, adc0

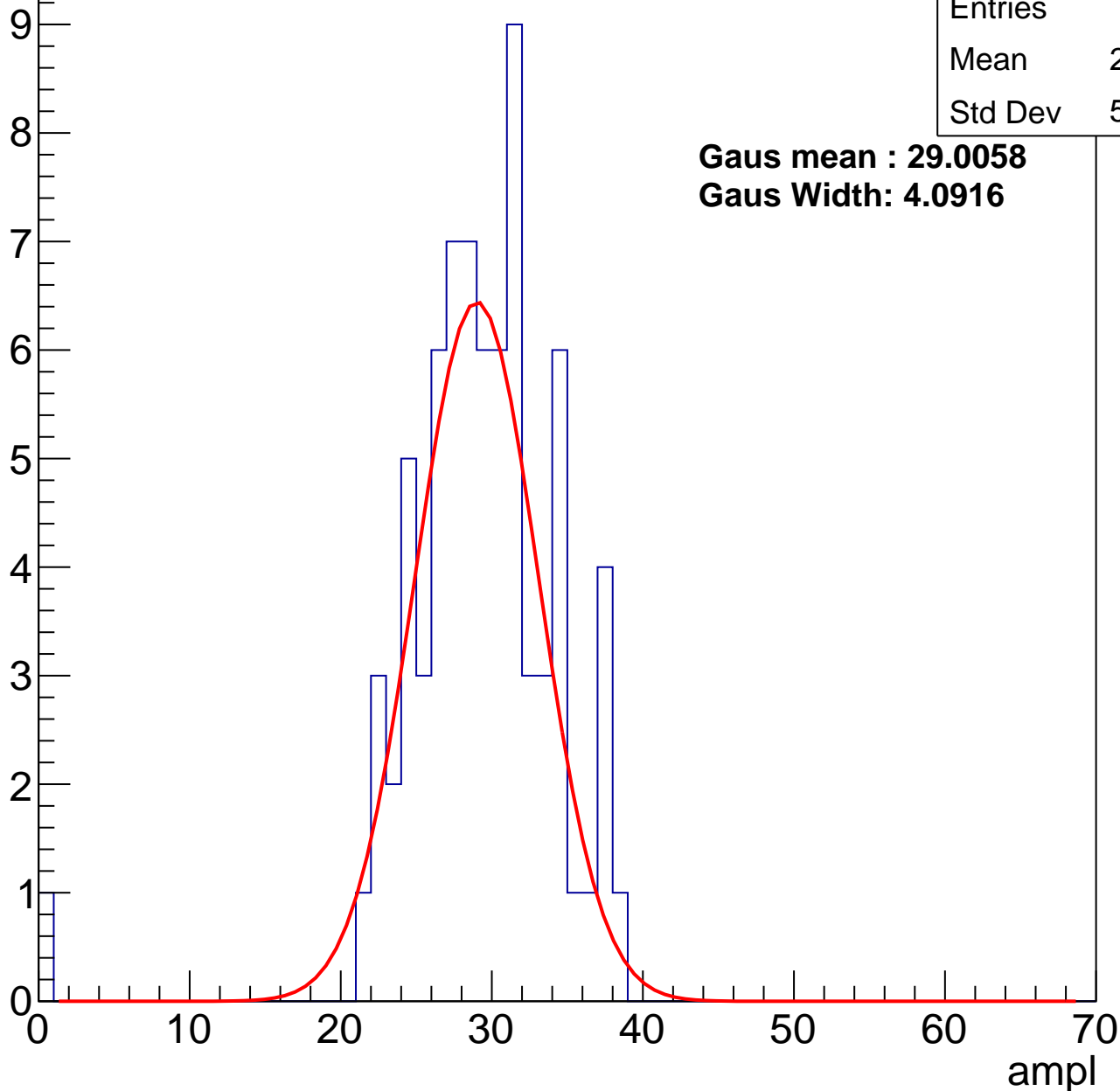
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	28.77
Std Dev	5.255

**Gaus mean : 29.0058**

**Gaus Width: 4.0916**



# B1L103S, U2-ch116, adc1

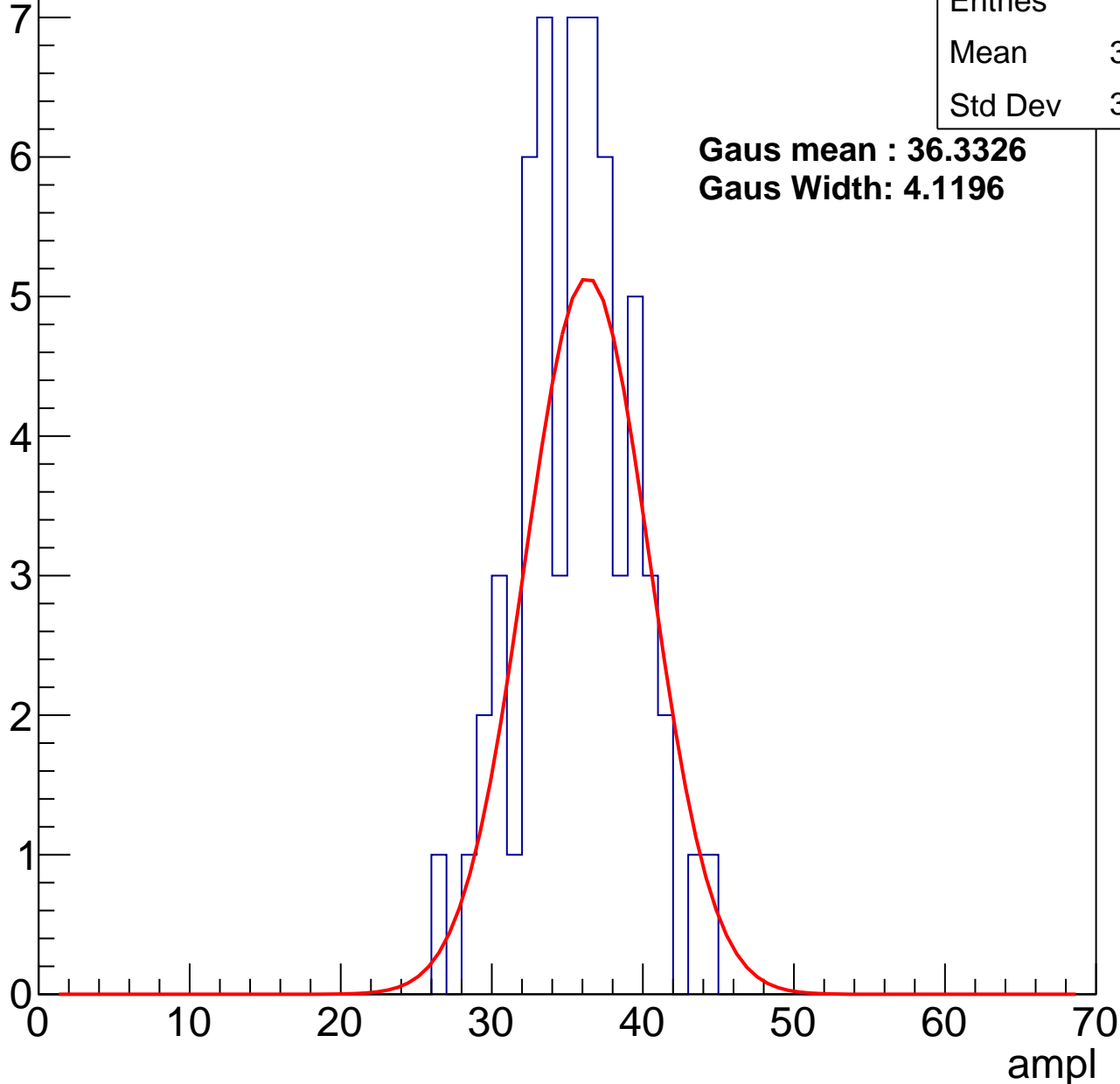
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	35.17
Std Dev	3.697

**Gaus mean : 36.3326**

**Gaus Width: 4.1196**

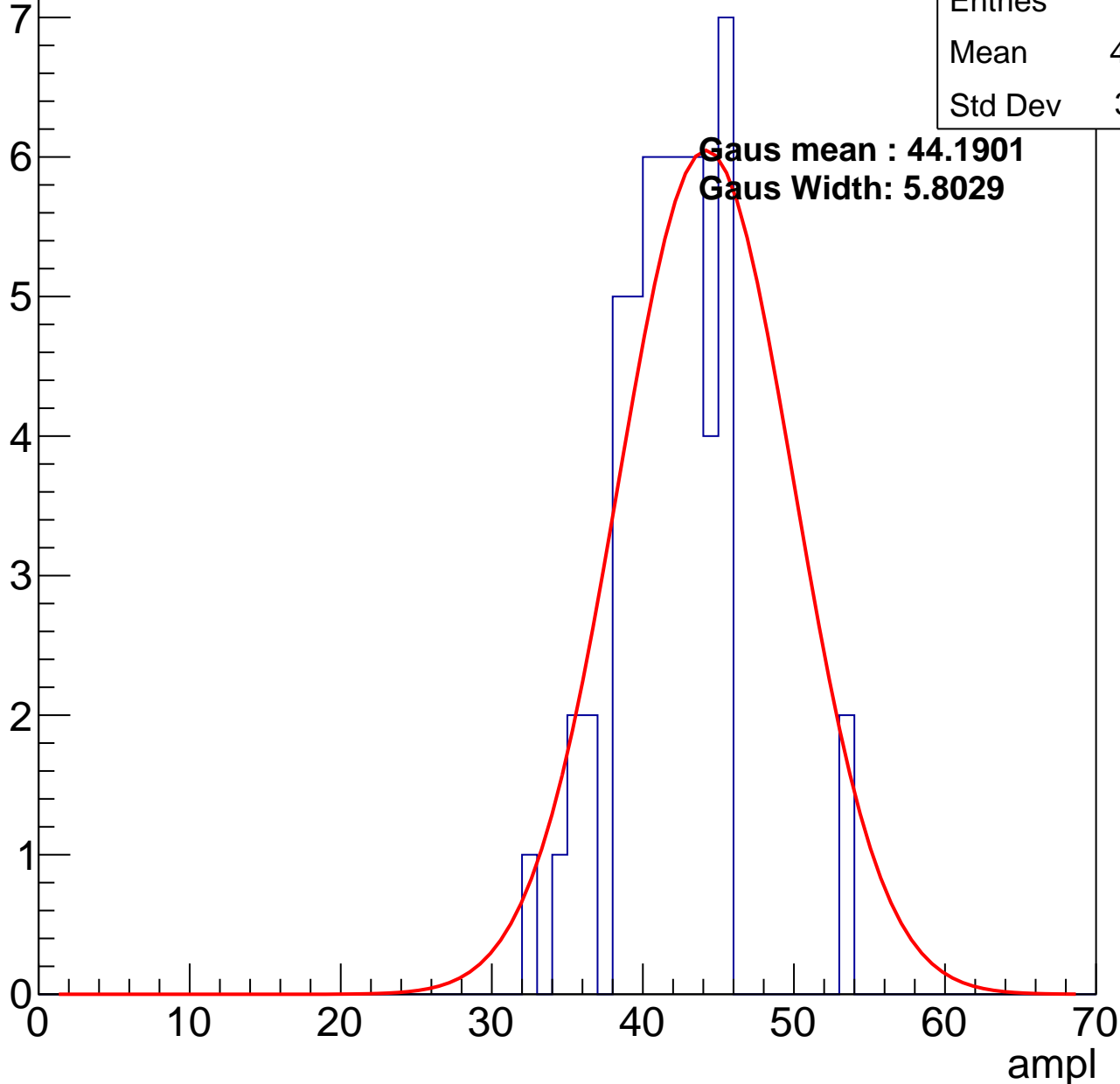


# B1L103S, U2-ch116, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	41.25
Std Dev	3.851

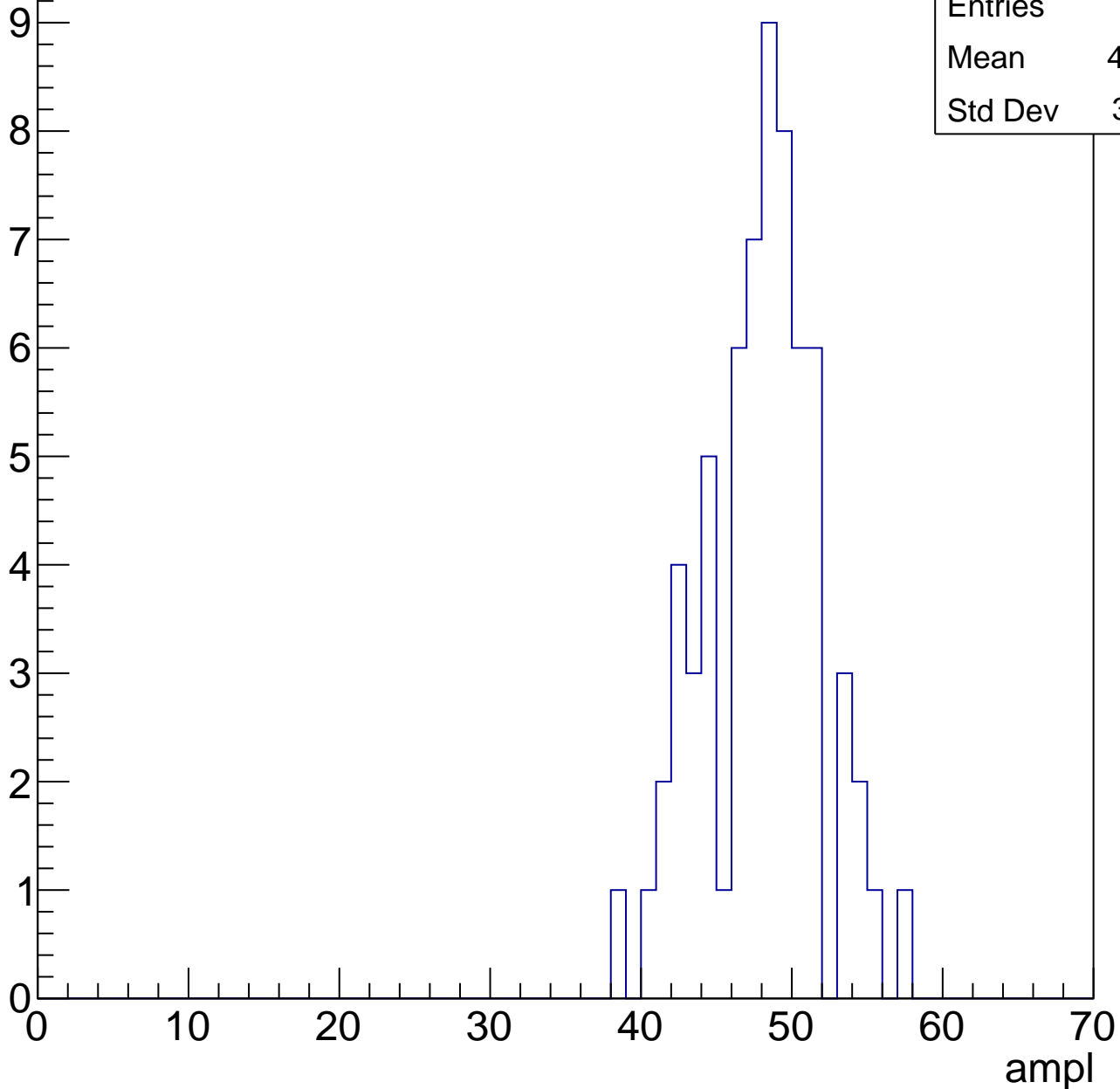


# B1L103S, U2-ch116, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	47.52
Std Dev	3.791

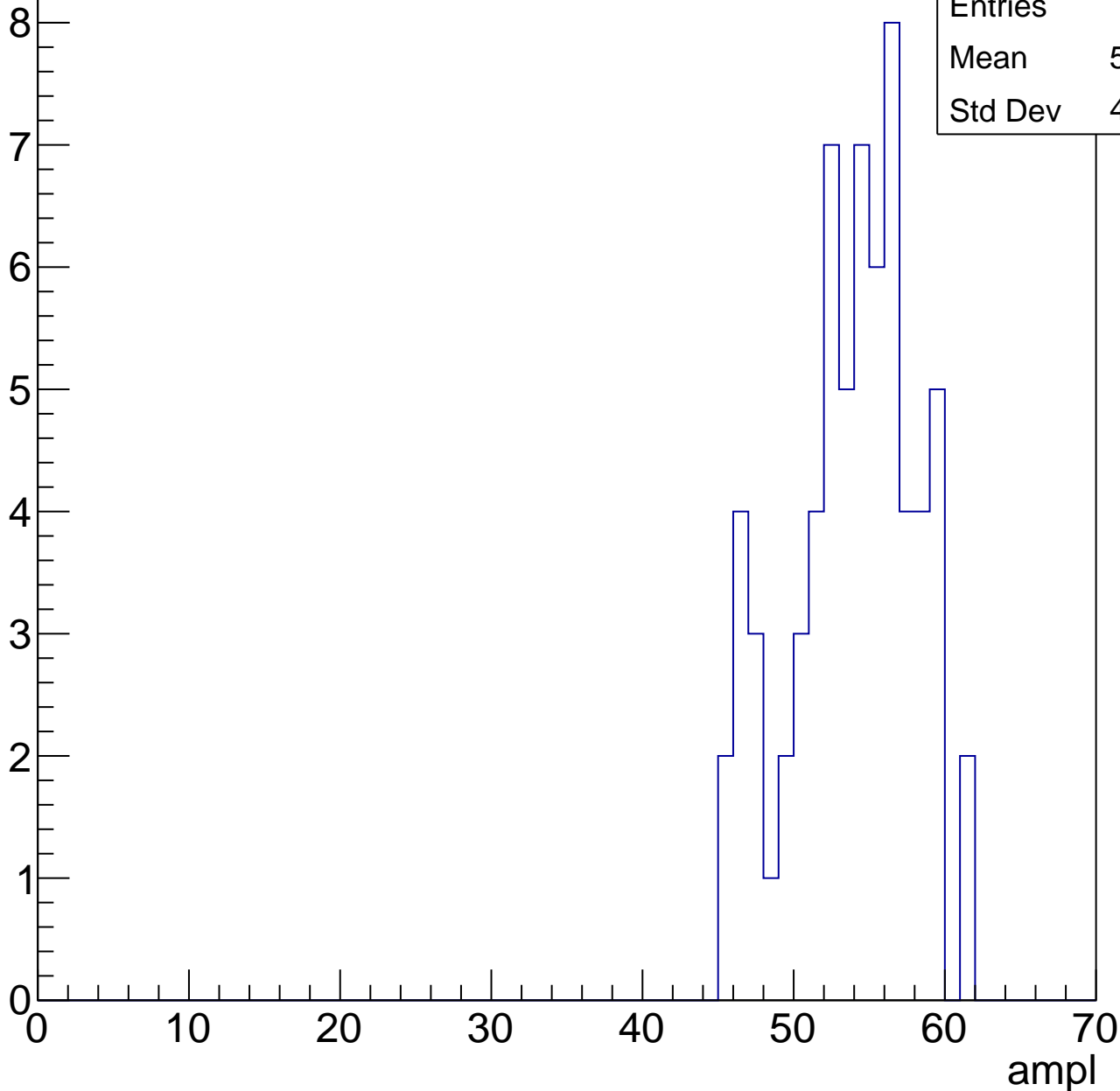


# B1L103S, U2-ch116, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	53.39
Std Dev	4.059

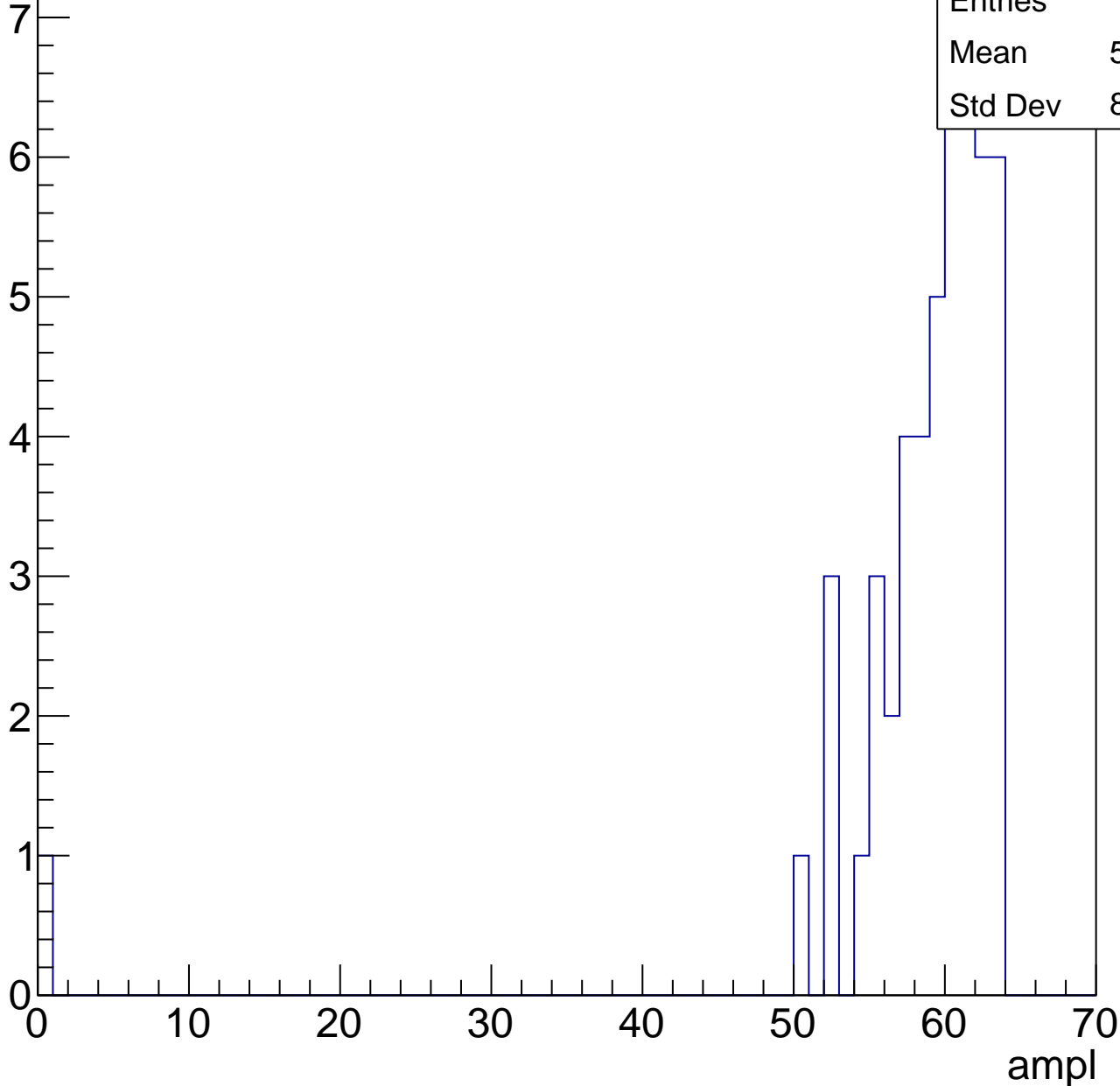


# B1L103S, U2-ch116, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

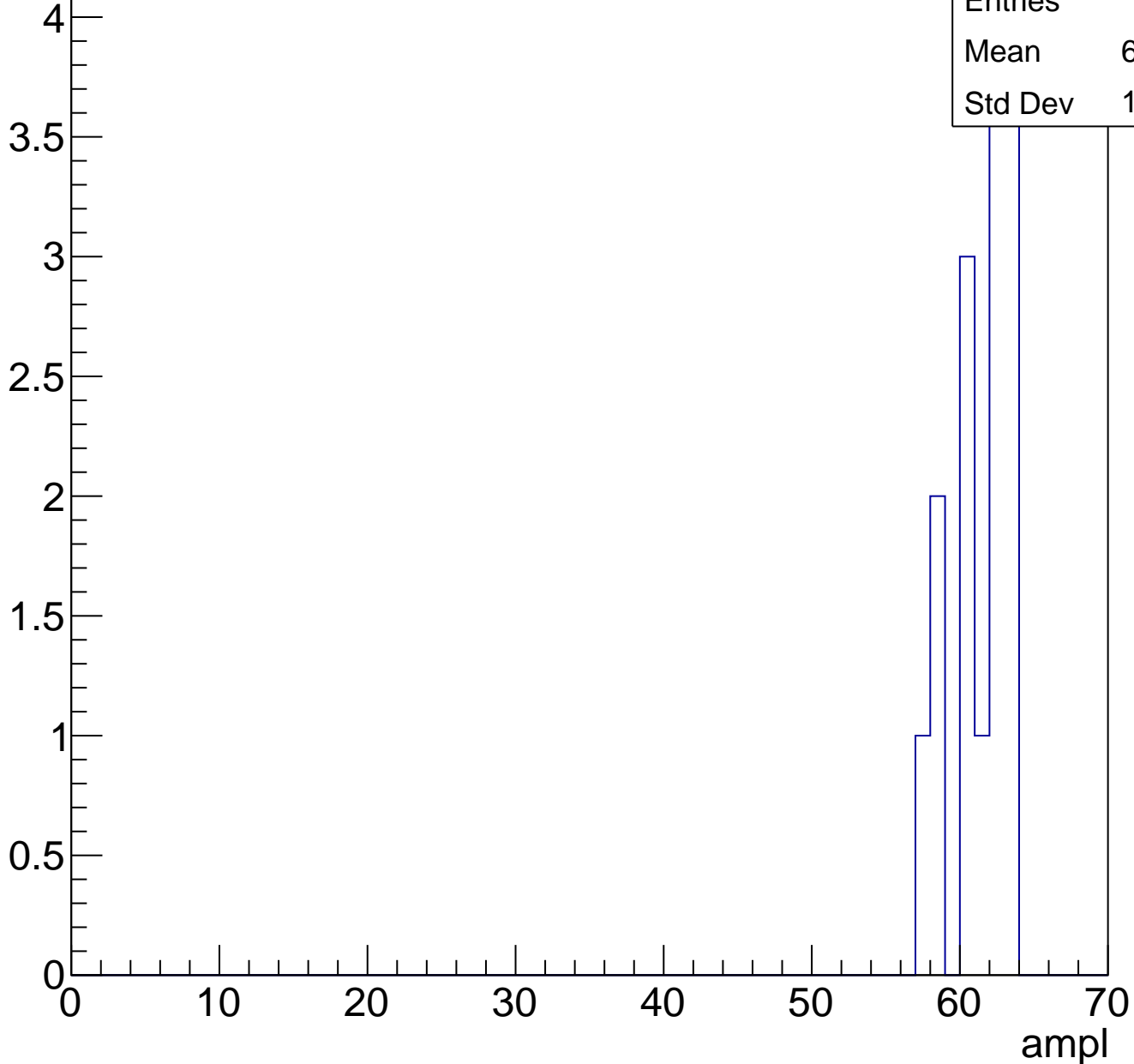
Entries	50
Mean	57.78
Std Dev	8.866



# B1L103S, U2-ch116, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U2-ch116, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U2-ch117, adc0

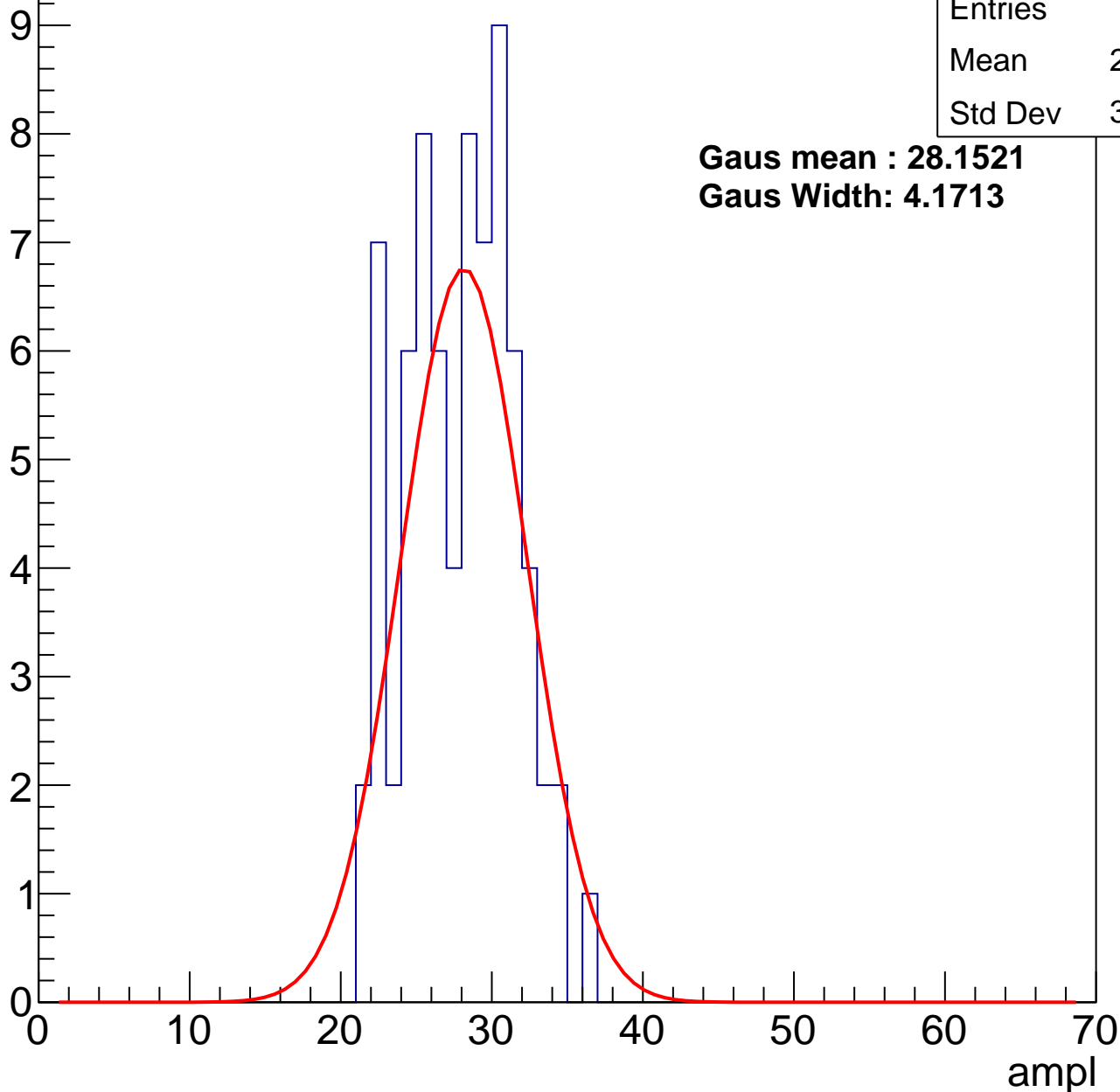
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	27.45
Std Dev	3.527

**Gaus mean : 28.1521**

**Gaus Width: 4.1713**



# B1L103S, U2-ch117, adc1

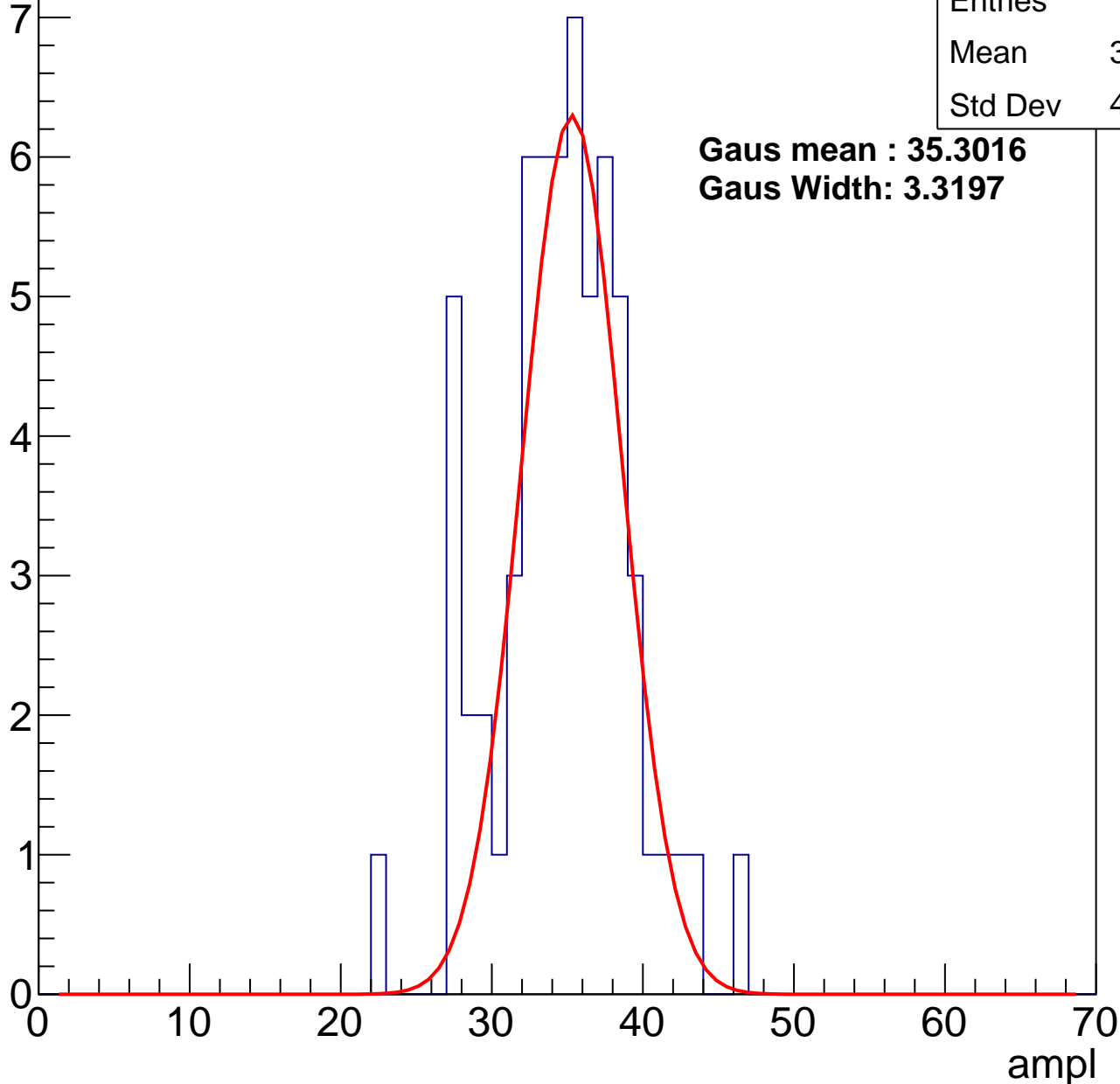
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	34.19
Std Dev	4.349

**Gaus mean : 35.3016**

**Gaus Width: 3.3197**



# B1L103S, U2-ch117, adc2

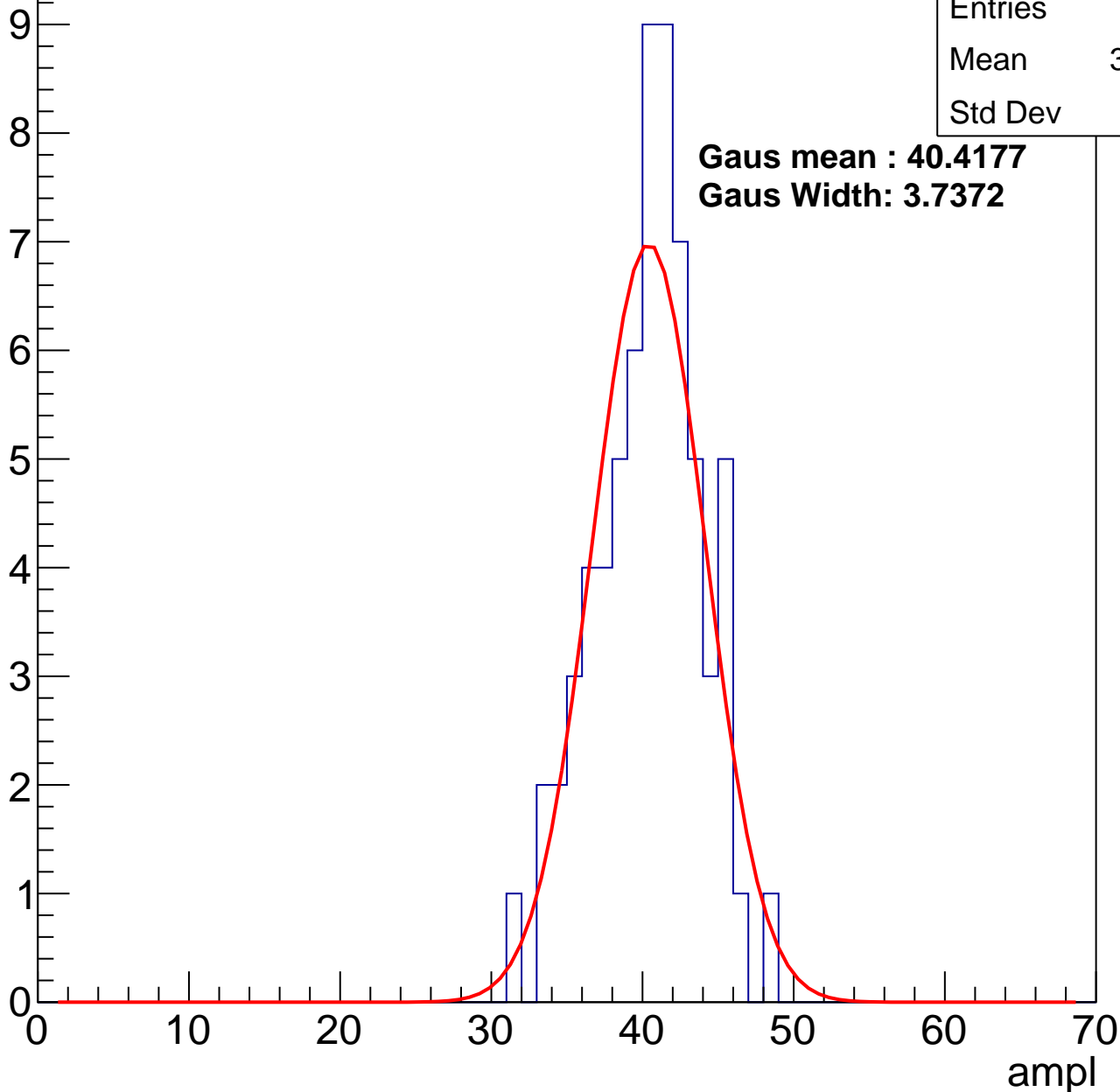
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	39.93
Std Dev	3.47

**Gaus mean : 40.4177**

**Gaus Width: 3.7372**

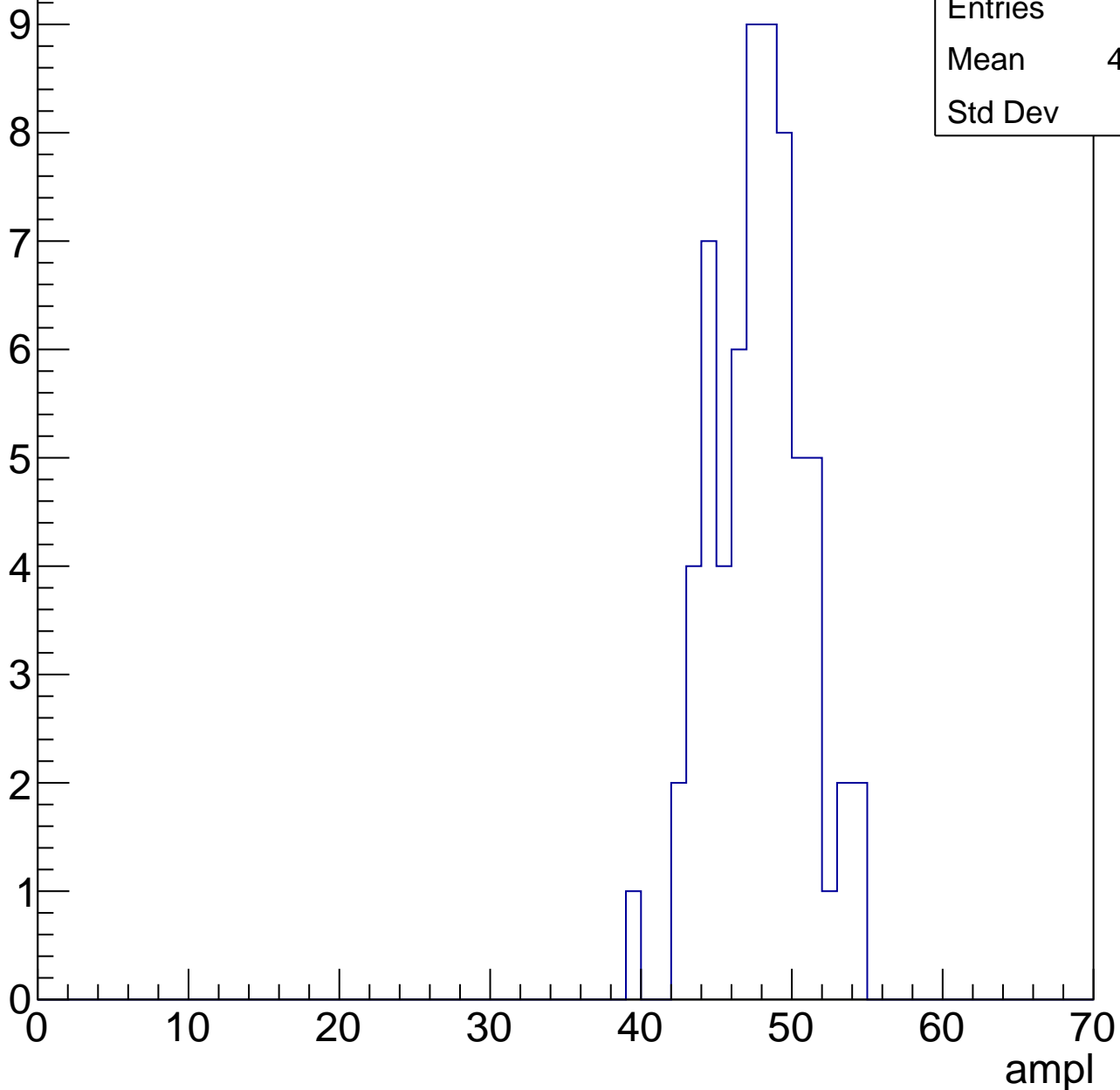


# B1L103S, U2-ch117, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	47.34
Std Dev	3.08

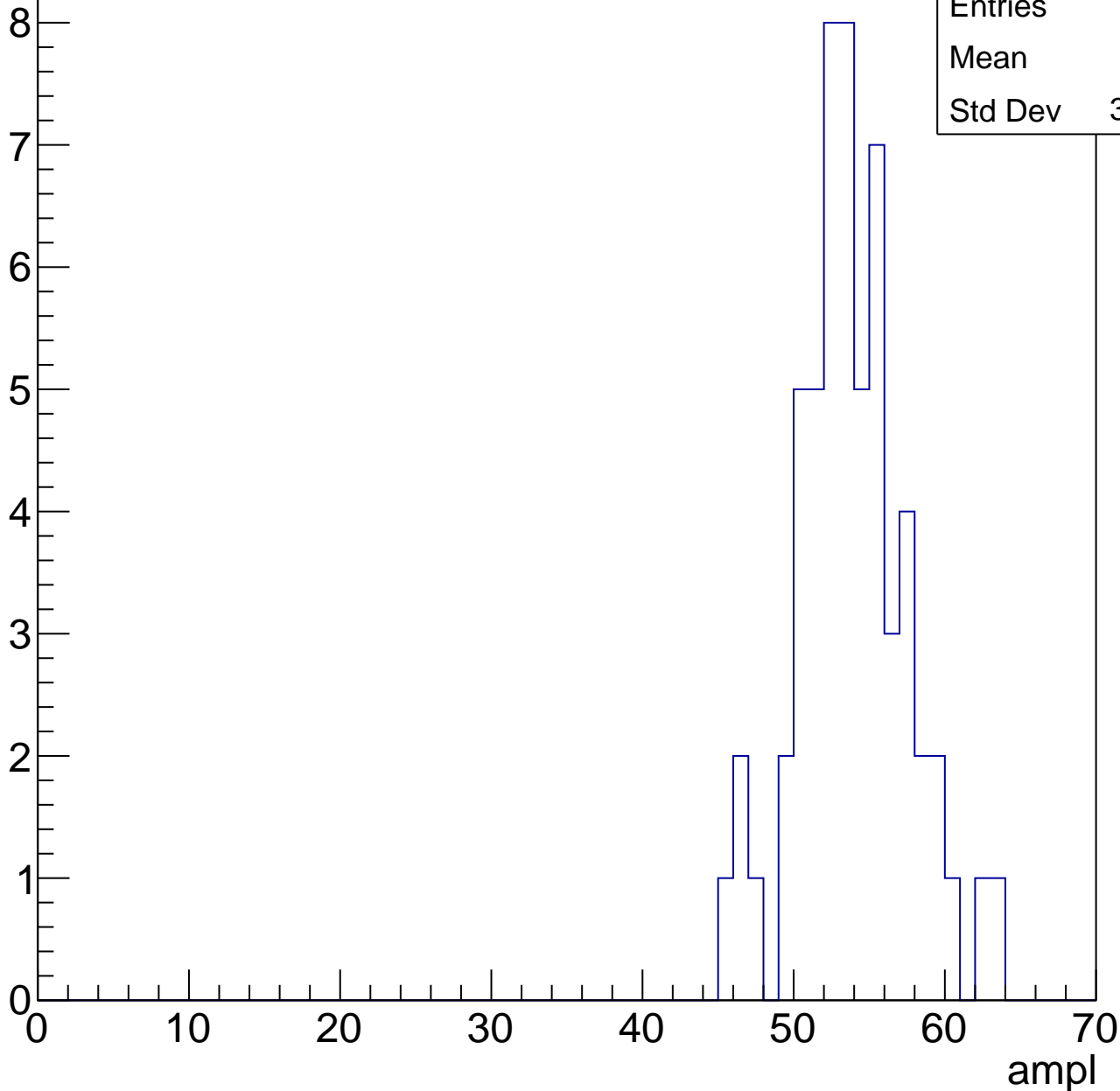


# B1L103S, U2-ch117, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	53.4
Std Dev	3.643

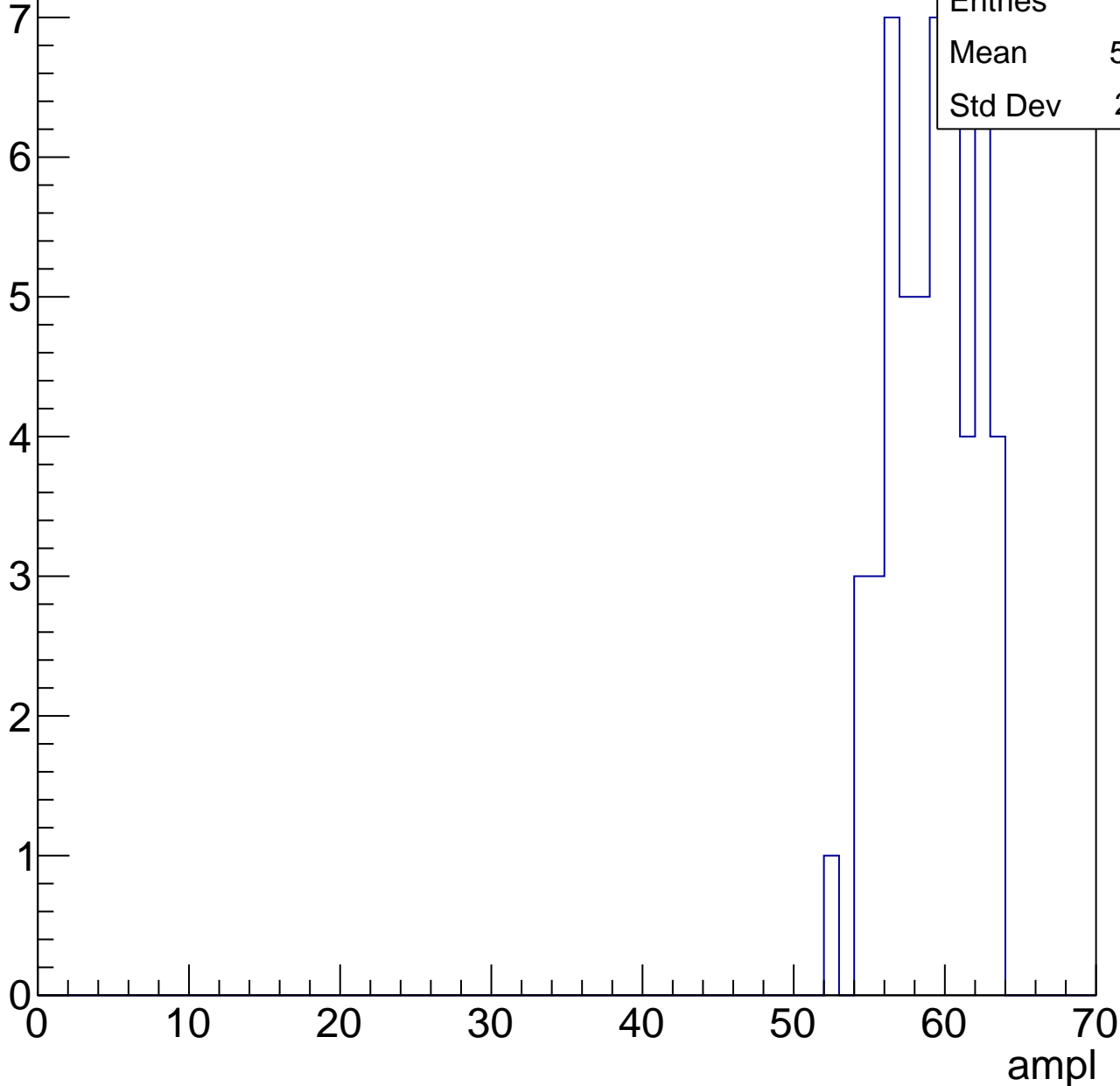


# B1L103S, U2-ch117, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	58.66
Std Dev	2.761

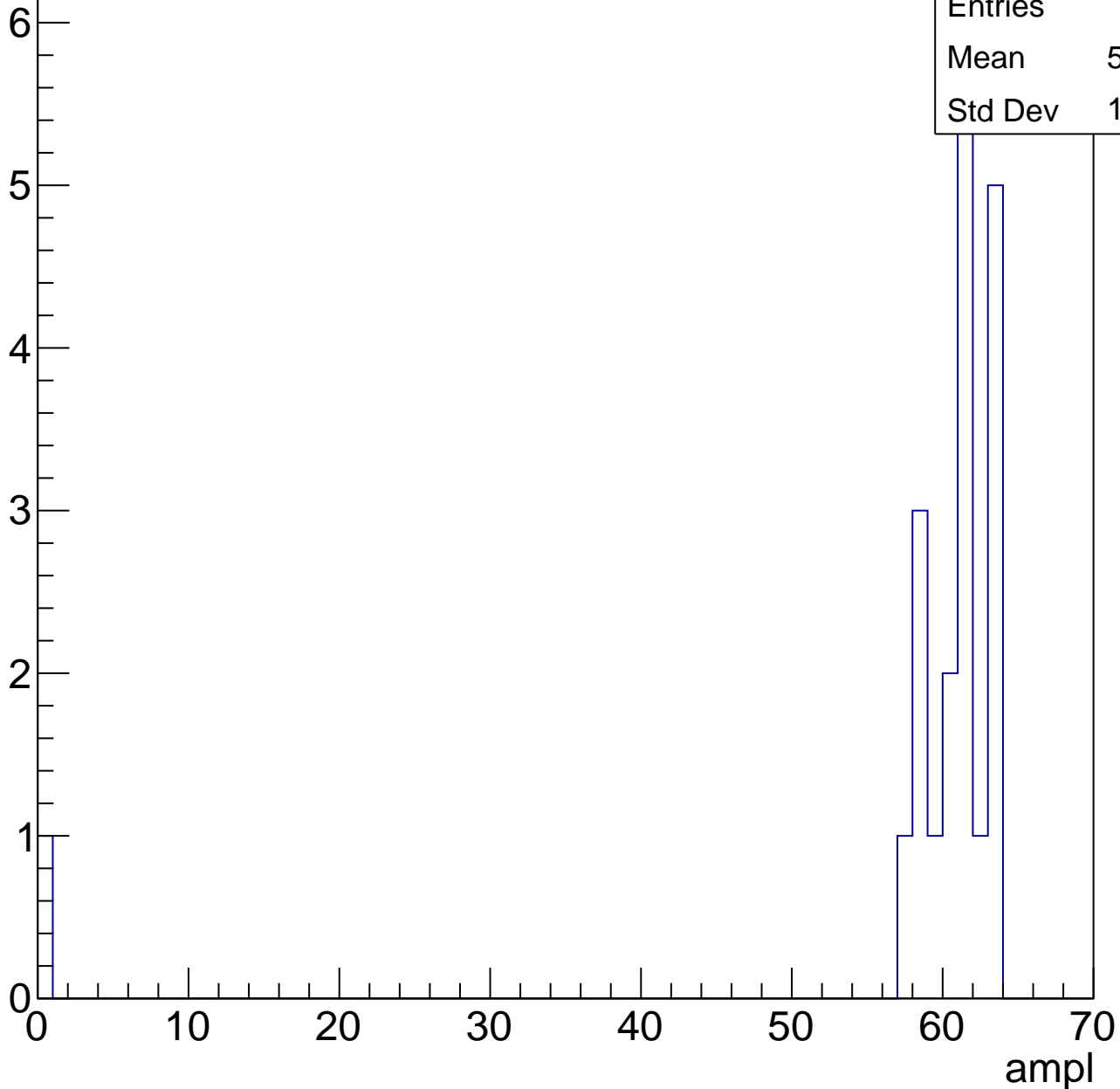


# B1L103S, U2-ch117, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	20
Mean	57.65
Std Dev	13.35





# B1L103S, U2-ch117, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	3
Mean	20.67
Std Dev	29.23

# B1L103S, U2-ch118, adc0

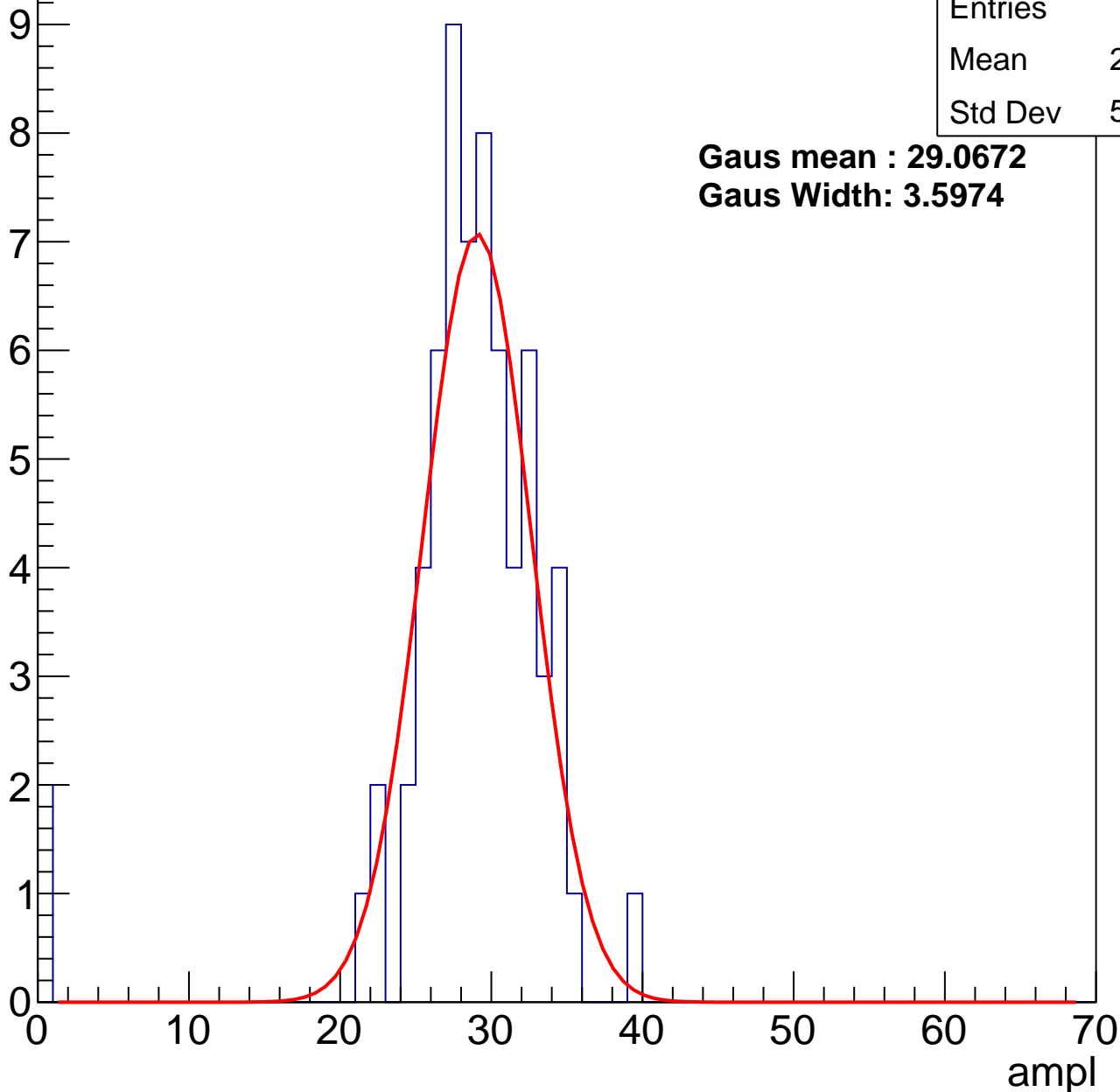
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	27.95
Std Dev	5.958

**Gaus mean : 29.0672**

**Gaus Width: 3.5974**



# B1L103S, U2-ch118, adc1

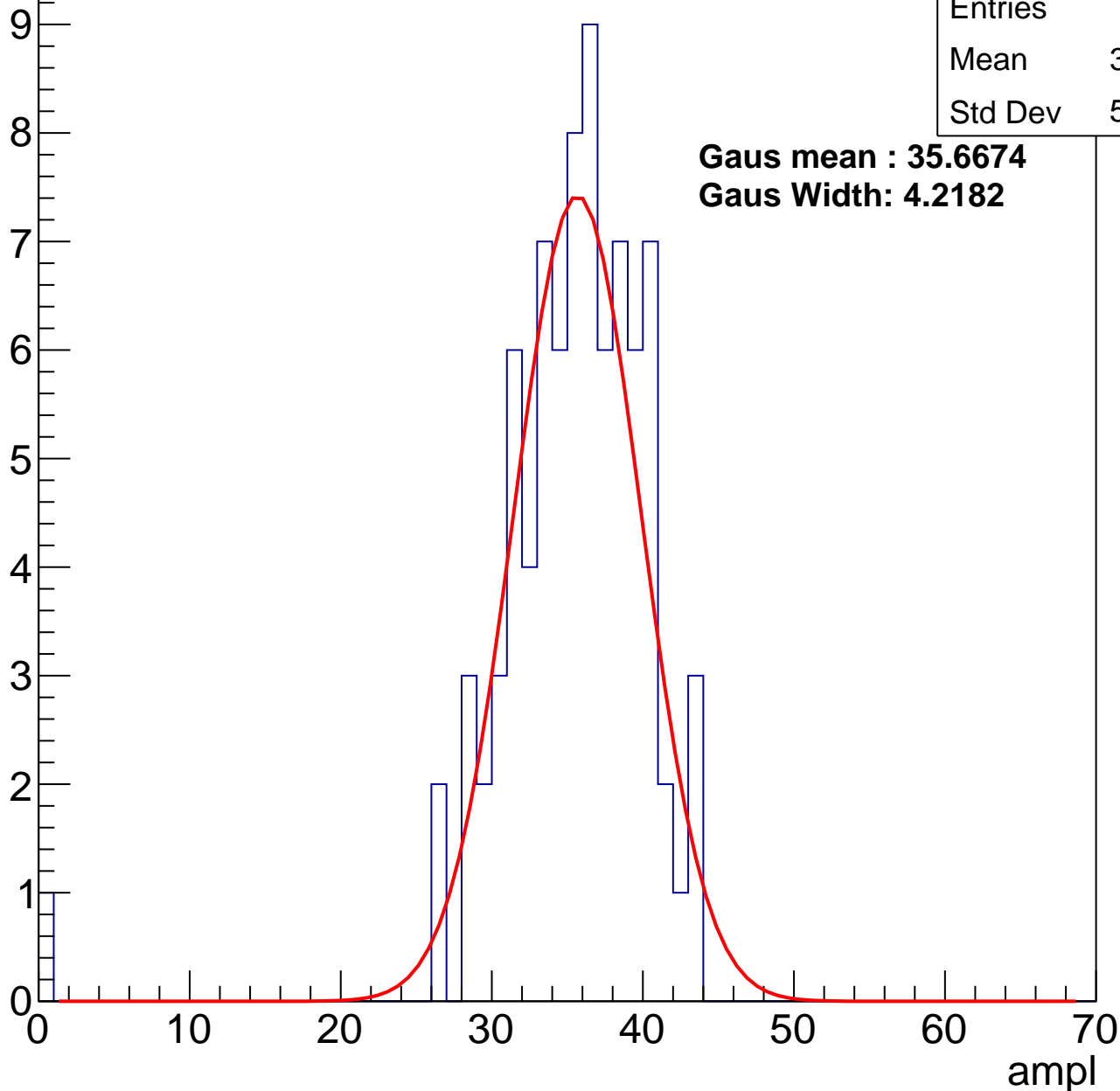
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	83
Mean	34.84
Std Dev	5.516

**Gaus mean : 35.6674**

**Gaus Width: 4.2182**



# B1L103S, U2-ch118, adc2

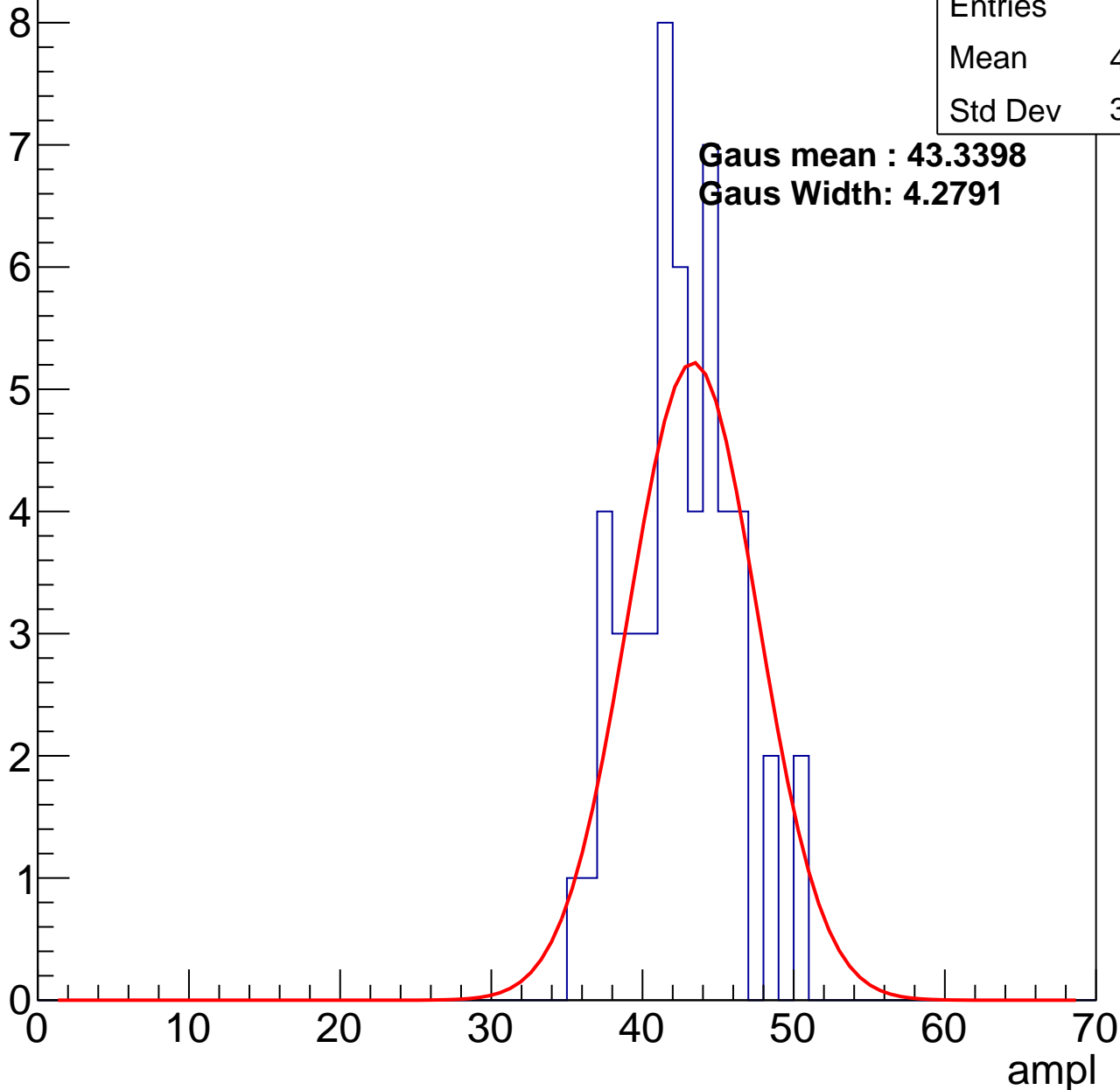
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	42.12
Std Dev	3.429

**Gaus mean : 43.3398**

**Gaus Width: 4.2791**

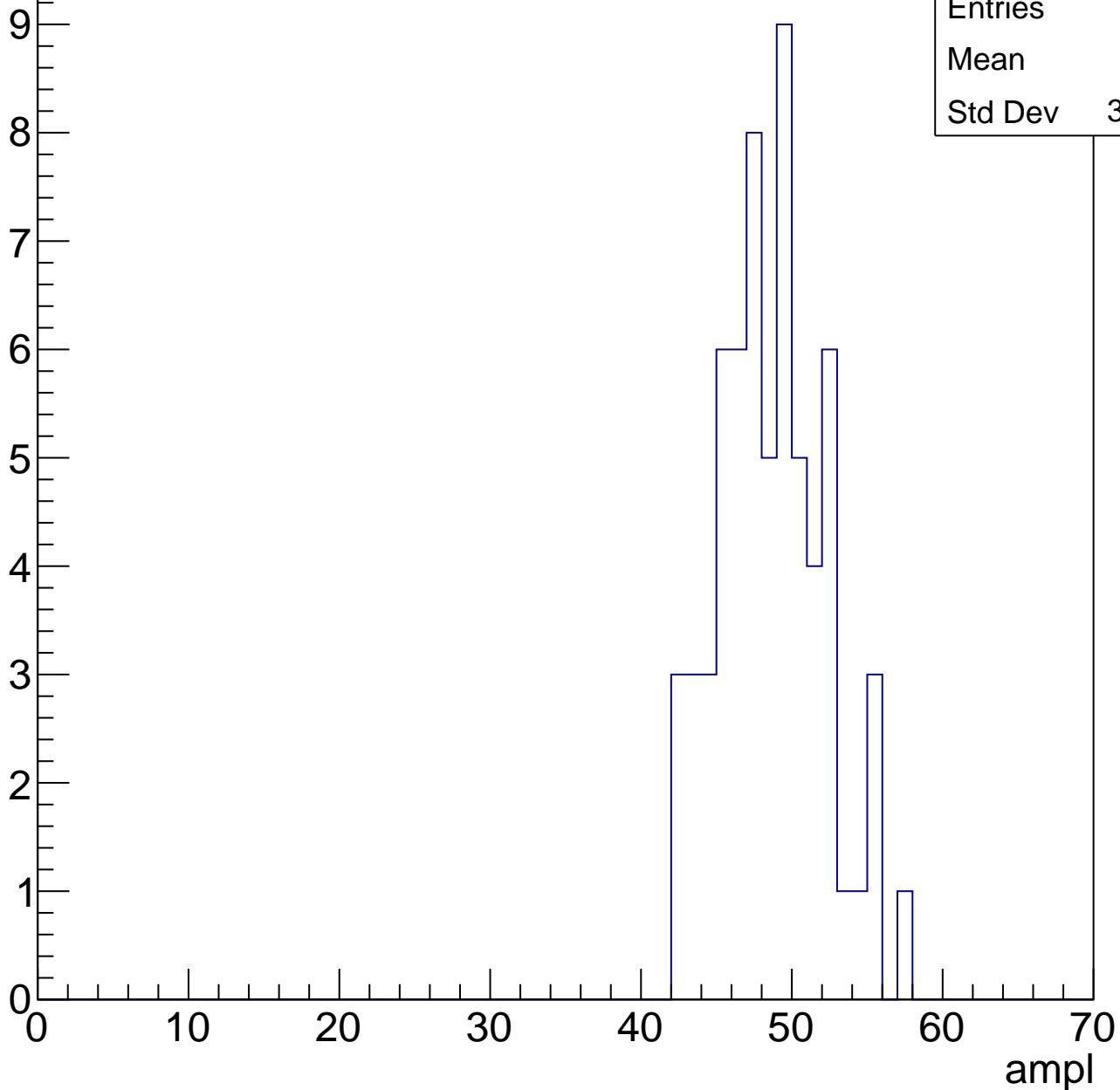


# B1L103S, U2-ch118, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	48.2
Std Dev	3.456

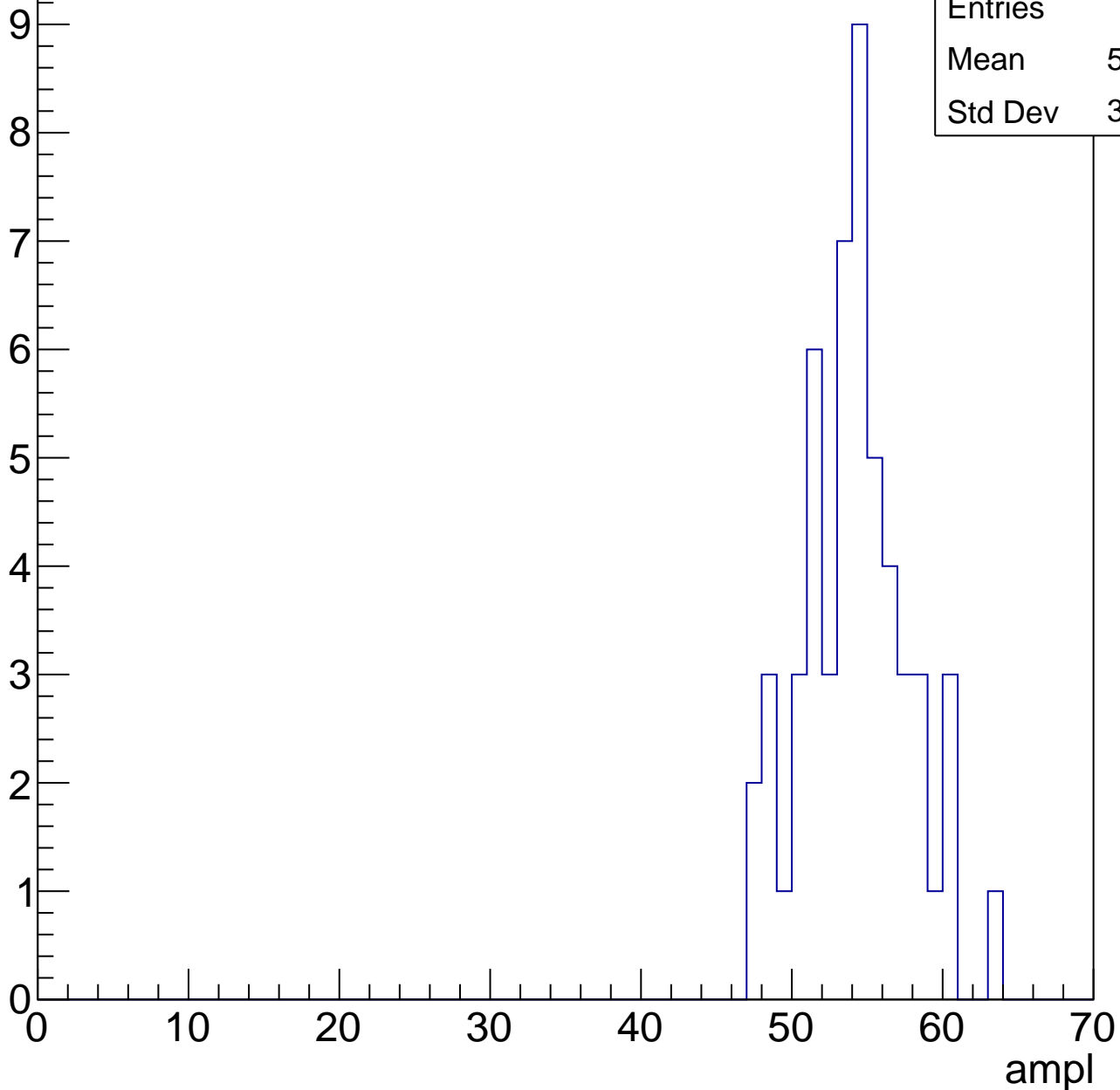


# B1L103S, U2-ch118, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

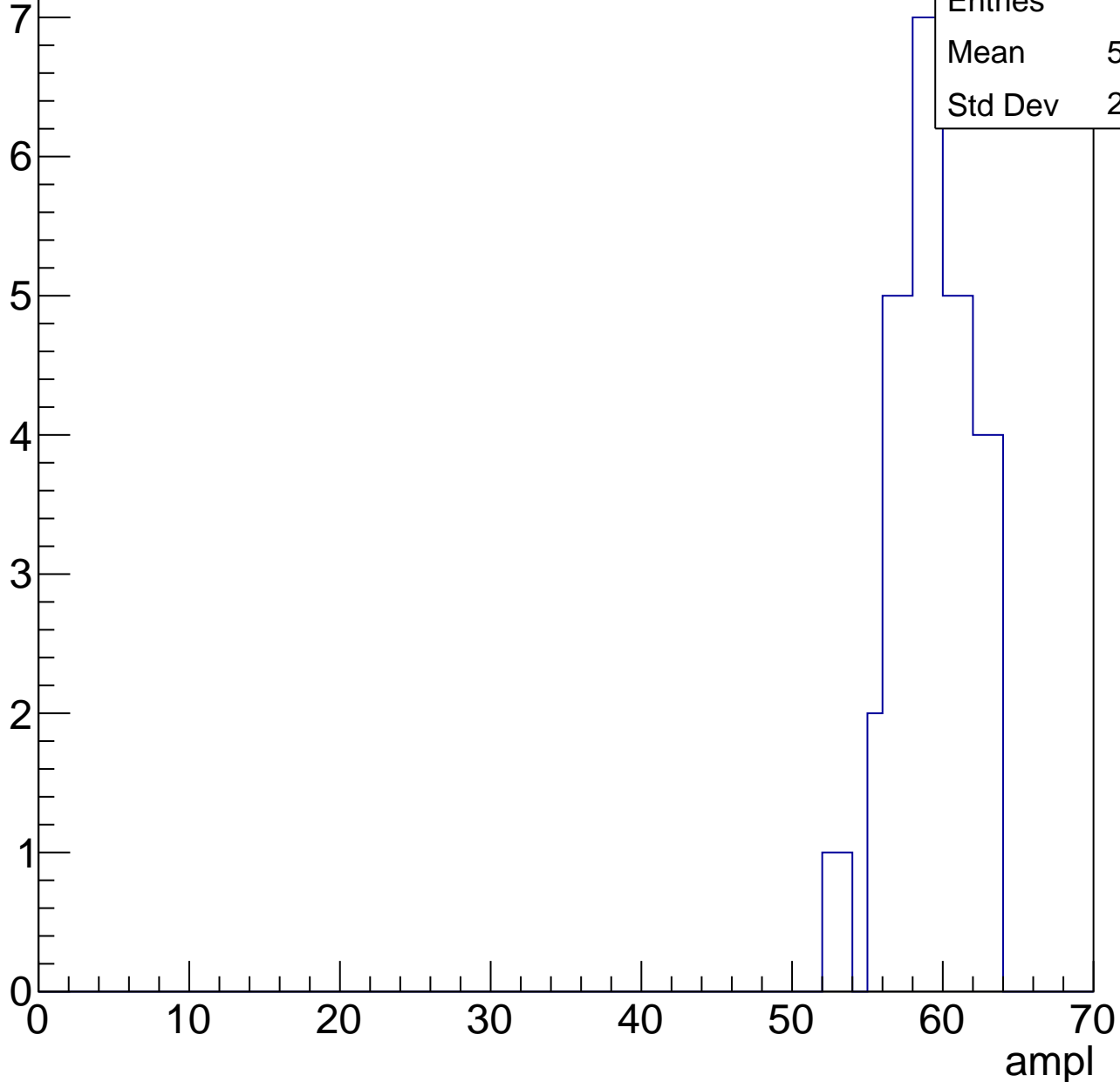
Entries	54
Mean	53.74
Std Dev	3.492



# B1L103S, U2-ch118, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

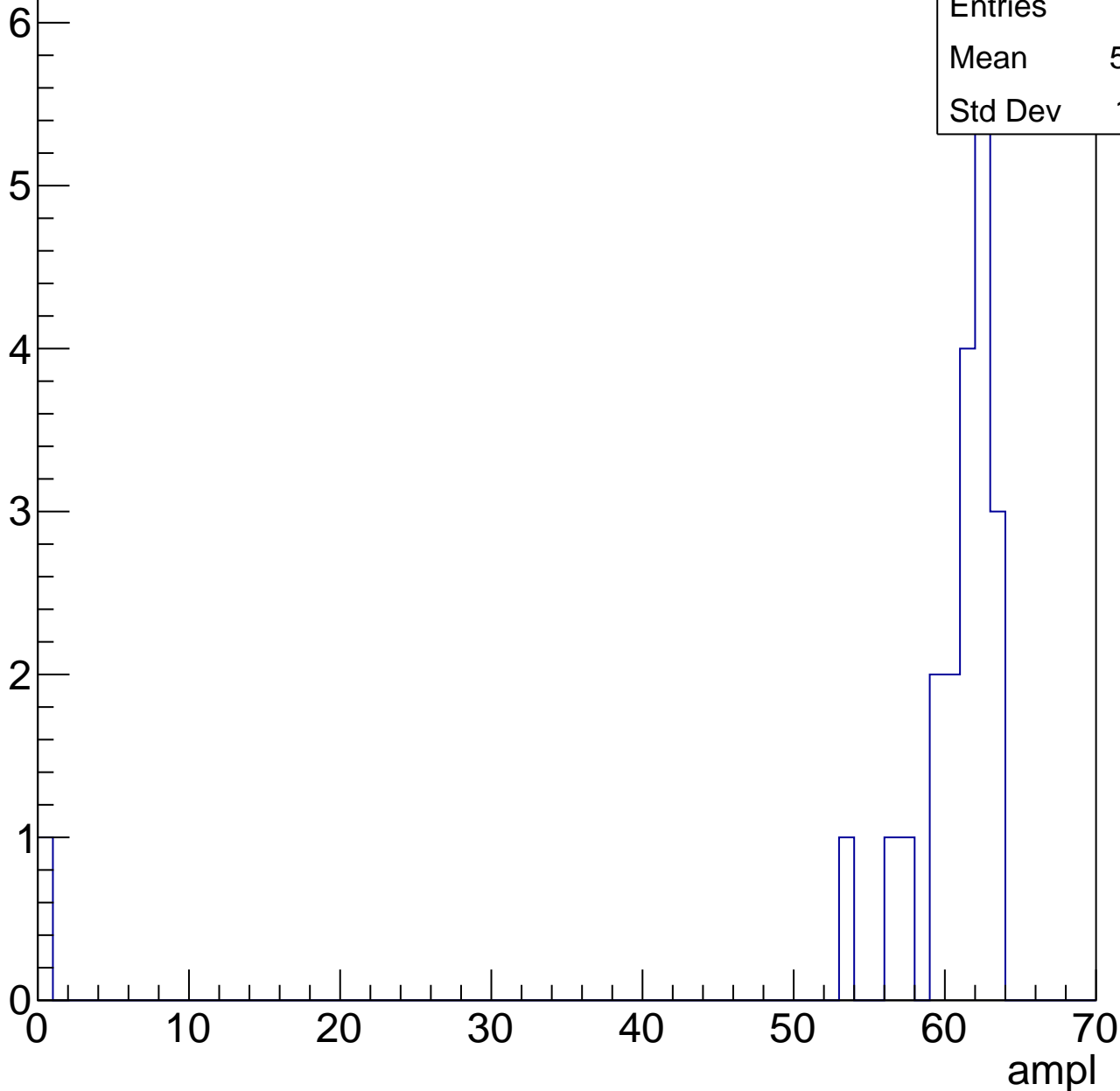


# B1L103S, U2-ch118, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	21
Mean	57.57
Std Dev	13.11

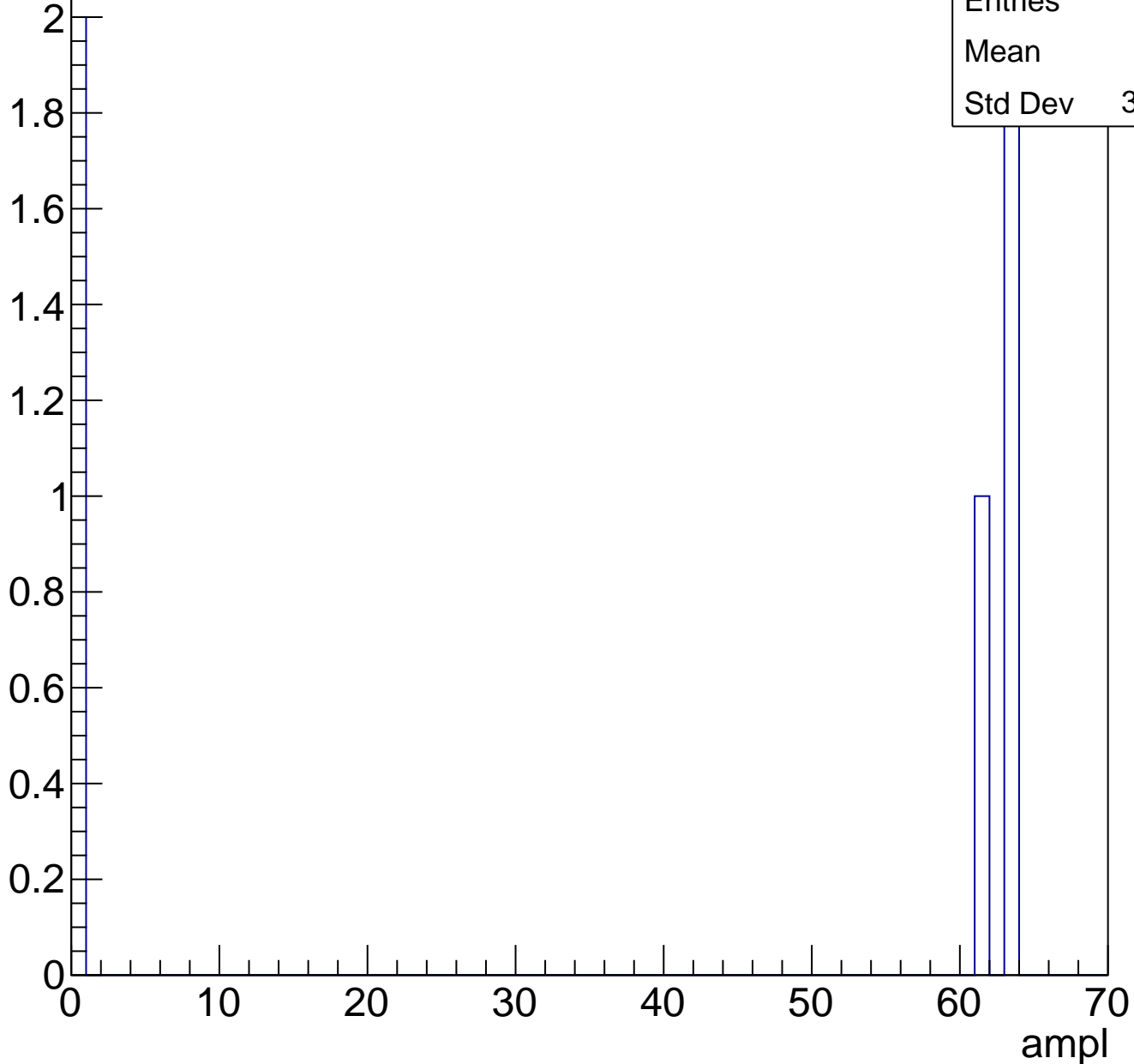




# B1L103S, U2-ch118, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch119, adc0

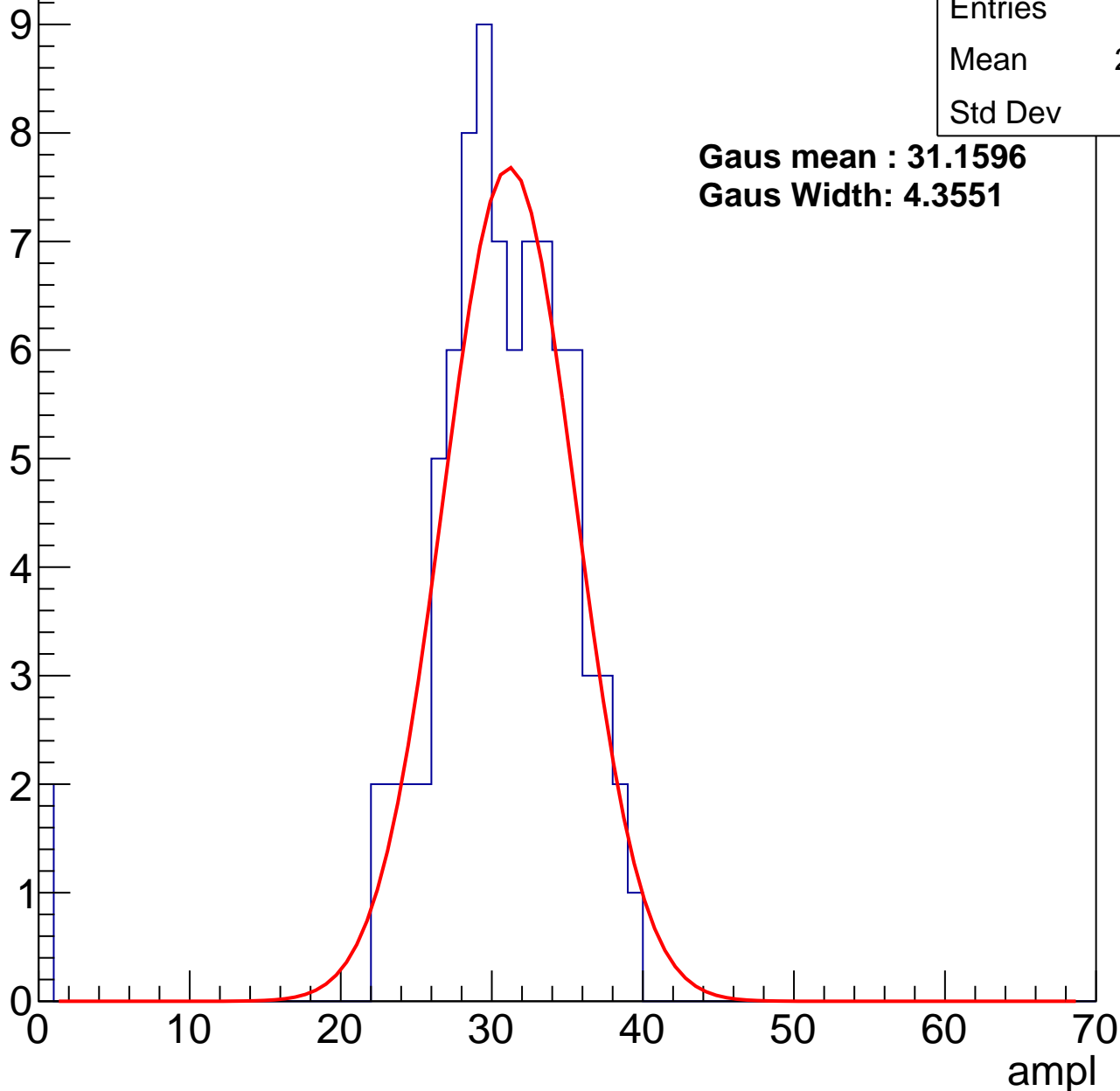
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	86
Mean	29.81
Std Dev	6.03

**Gaus mean : 31.1596**

**Gaus Width: 4.3551**



# B1L103S, U2-ch119, adc1

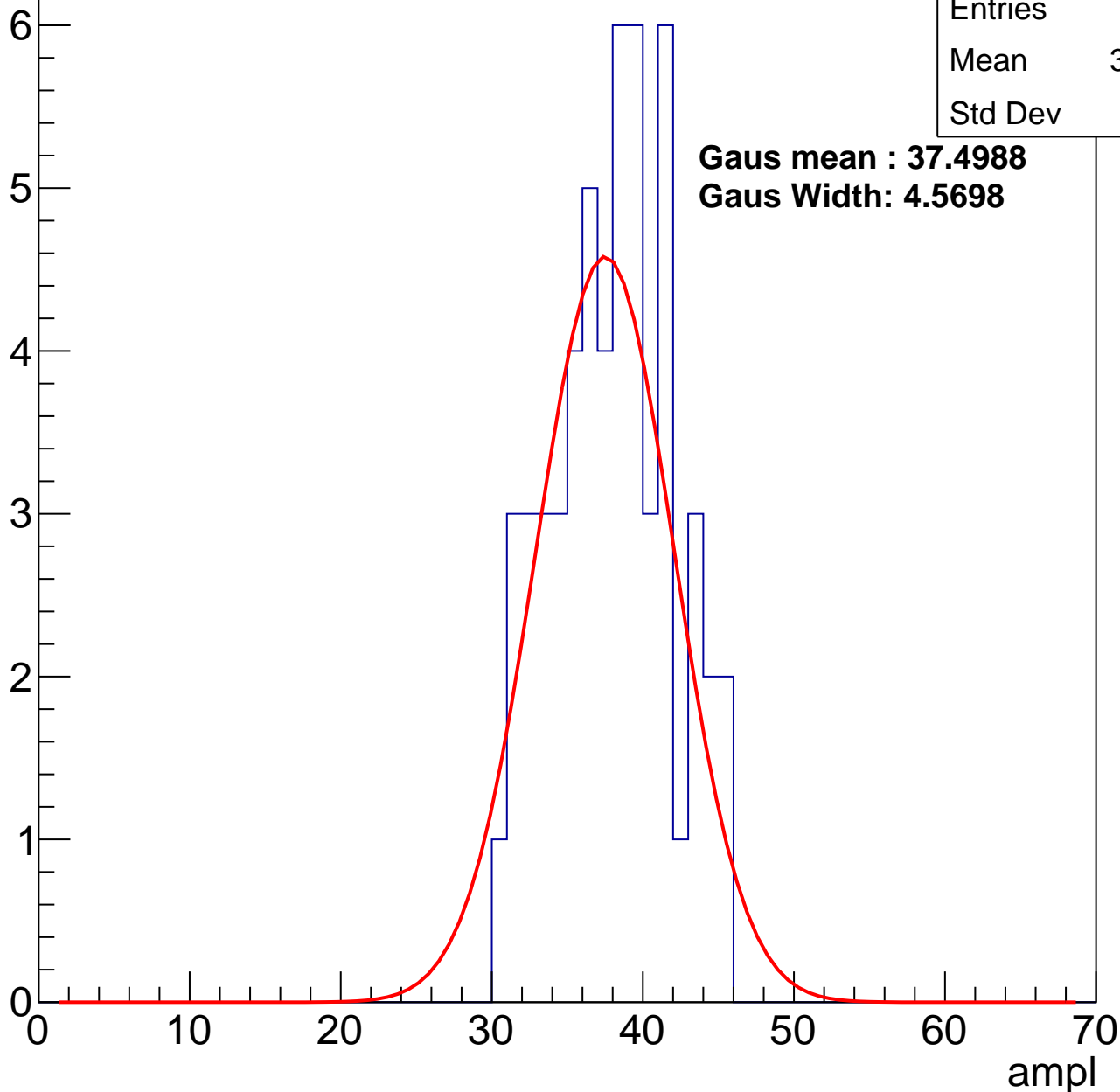
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	37.55
Std Dev	3.87

**Gaus mean : 37.4988**

**Gaus Width: 4.5698**



# B1L103S, U2-ch119, adc2

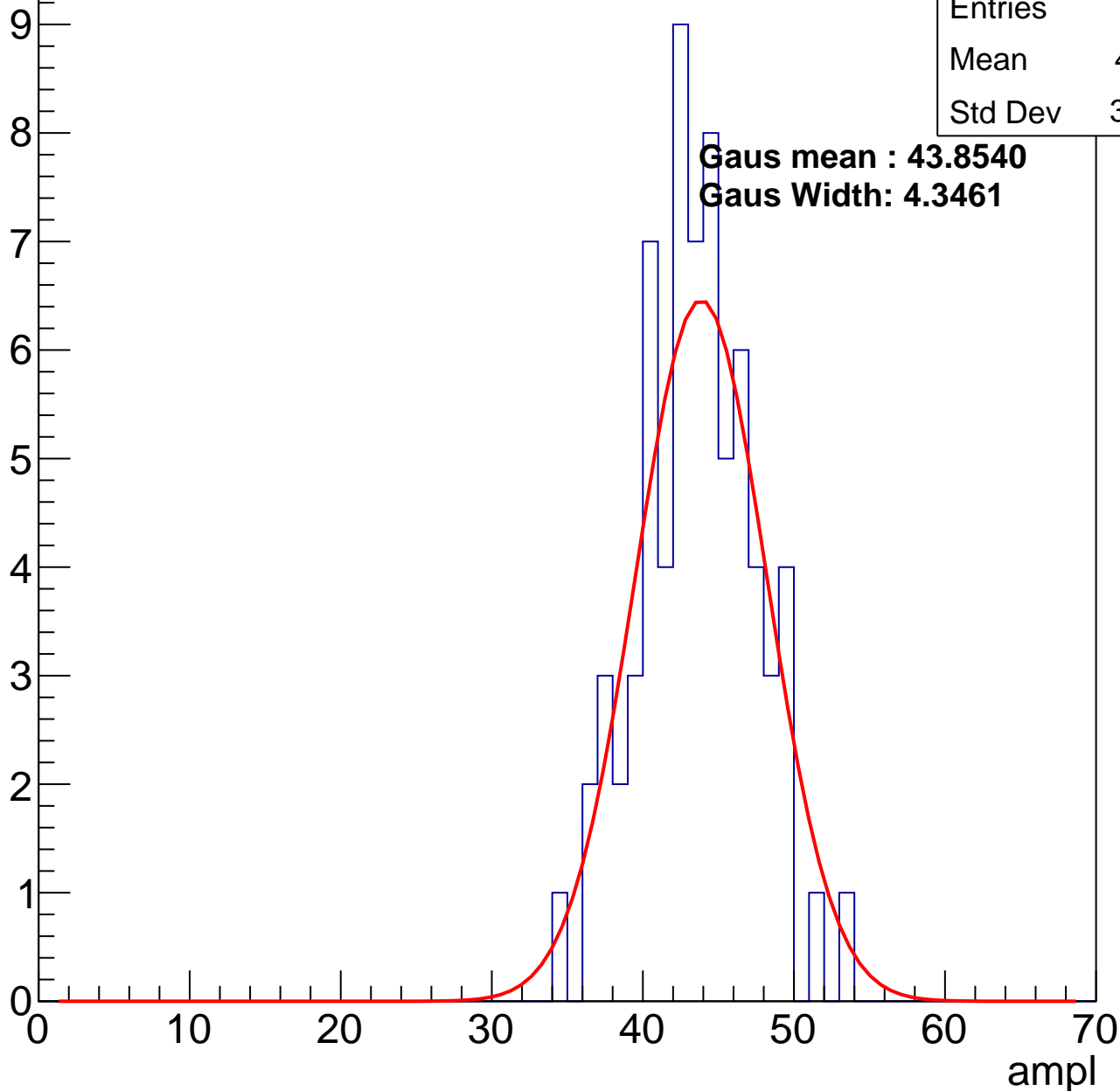
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	43.11
Std Dev	3.782

**Gaus mean : 43.8540**

**Gaus Width: 4.3461**

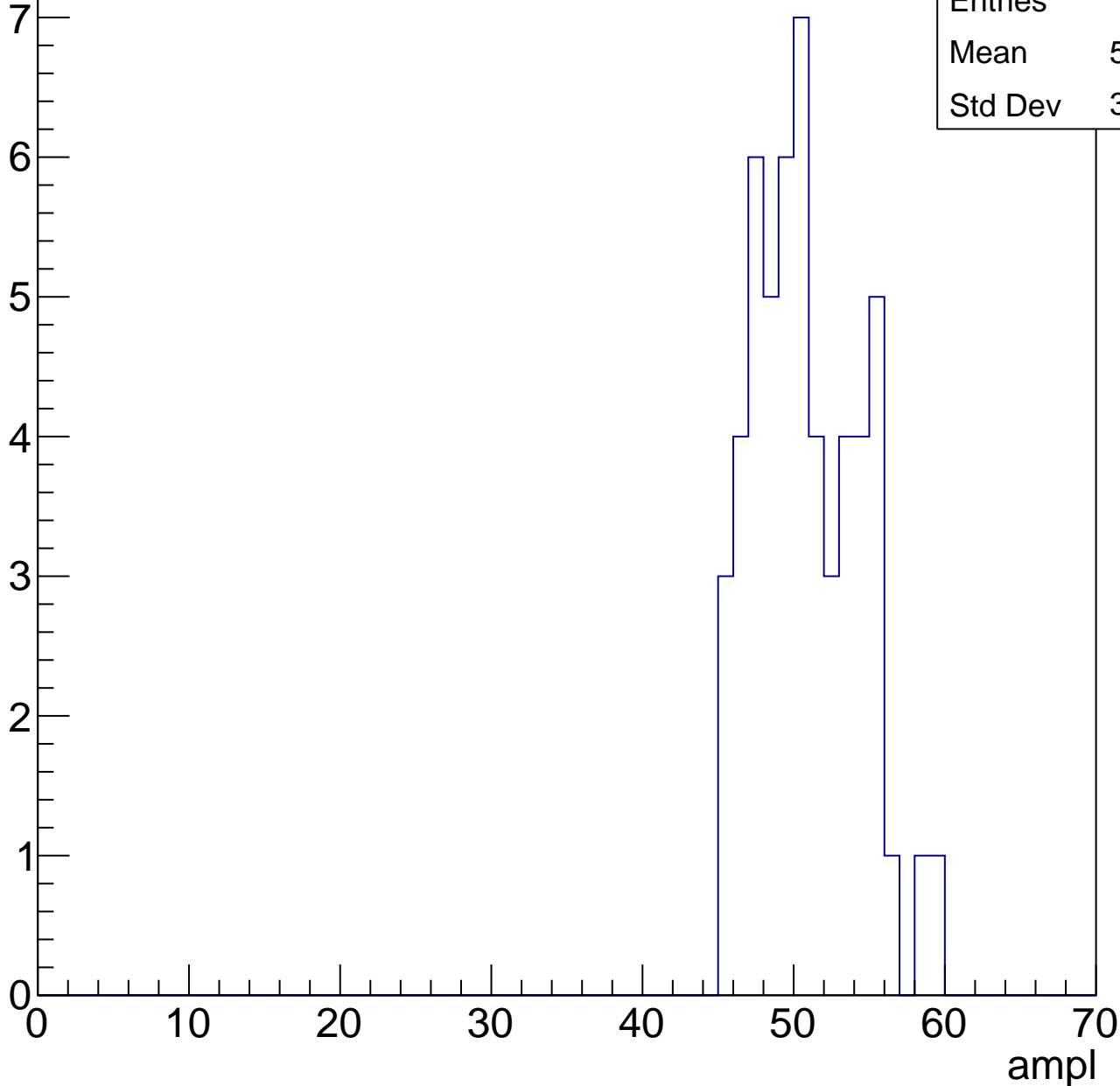


# B1L103S, U2-ch119, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	50.39
Std Dev	3.423

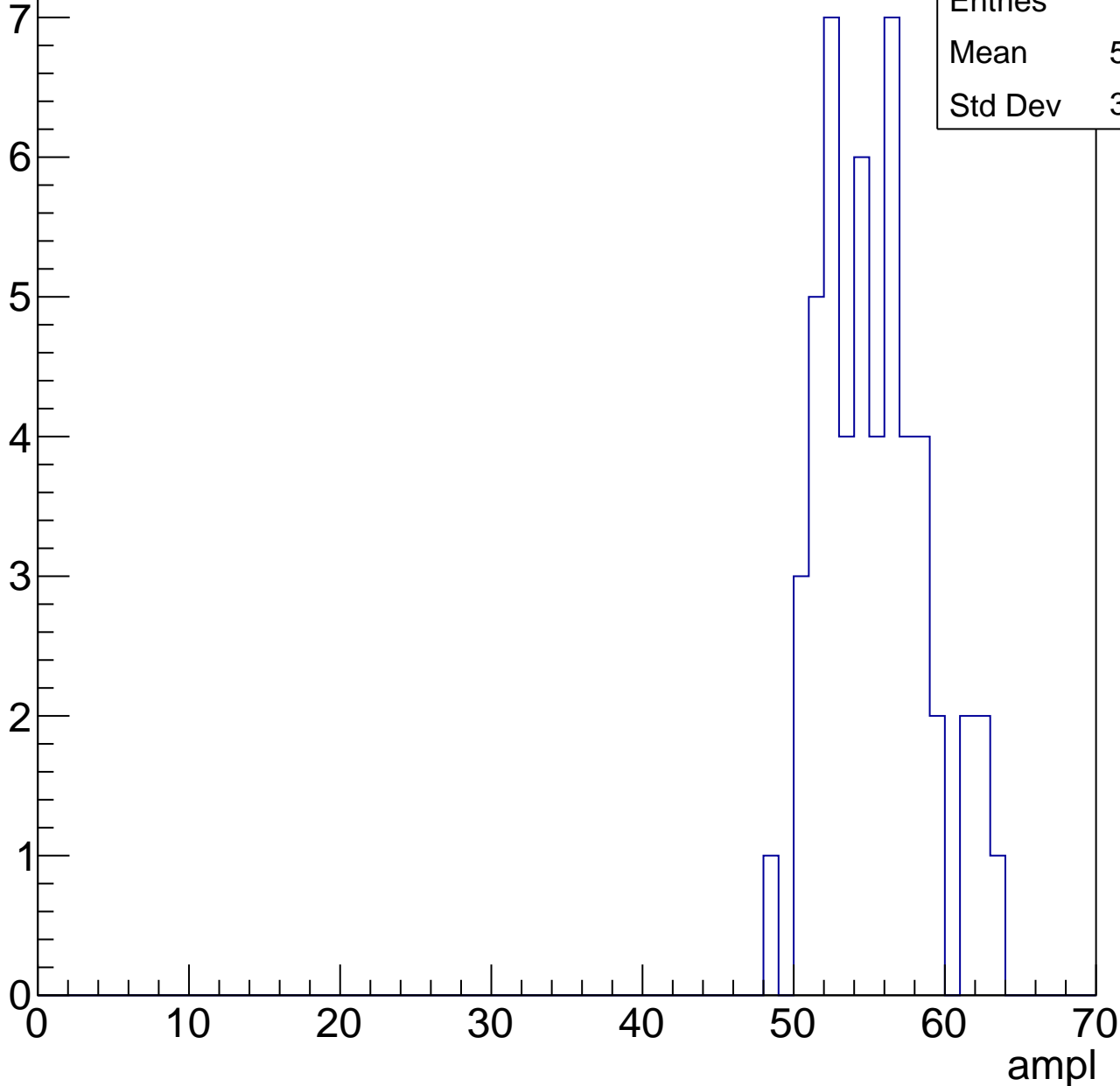


# B1L103S, U2-ch119, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	54.85
Std Dev	3.433

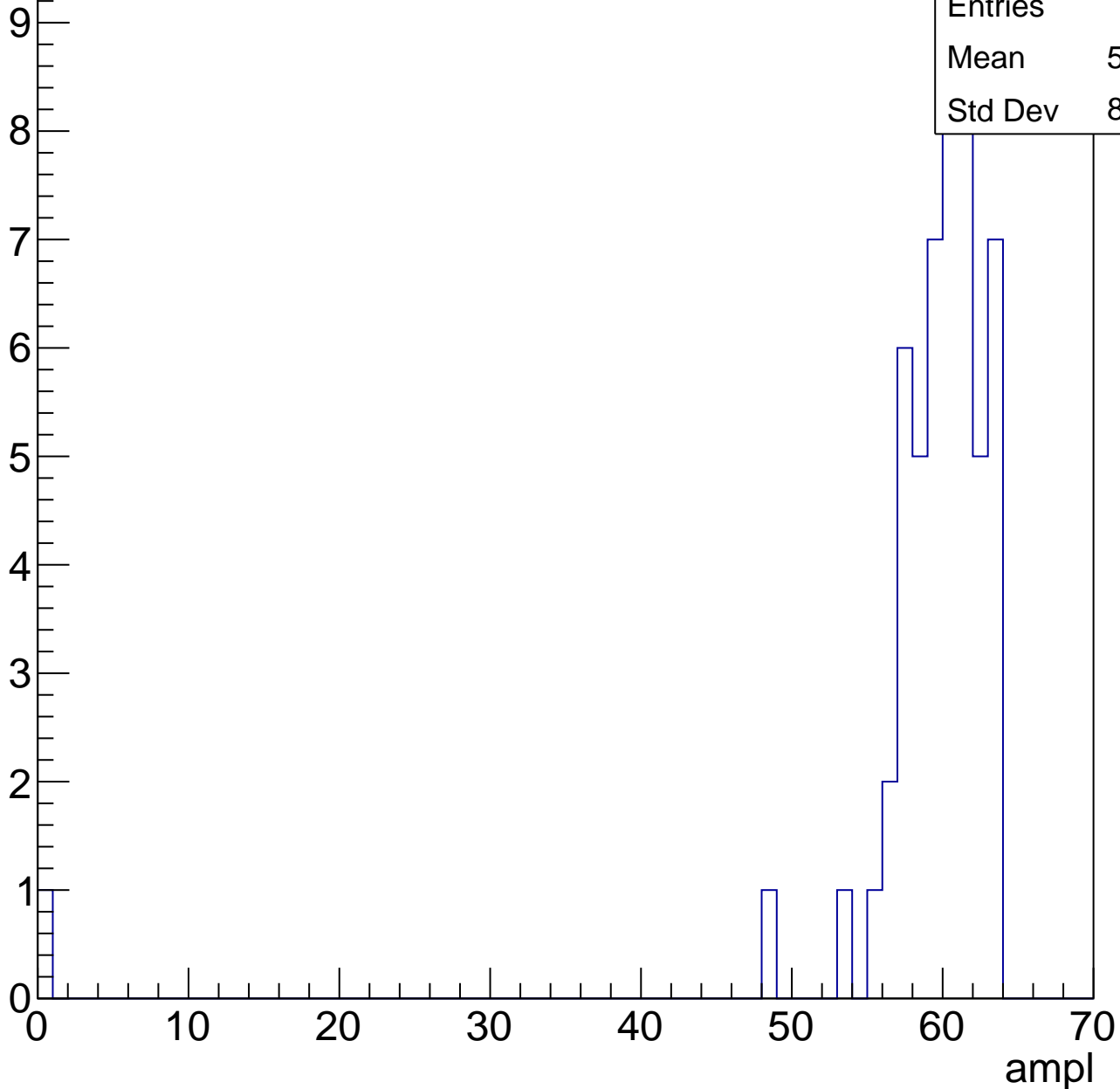


# B1L103S, U2-ch119, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

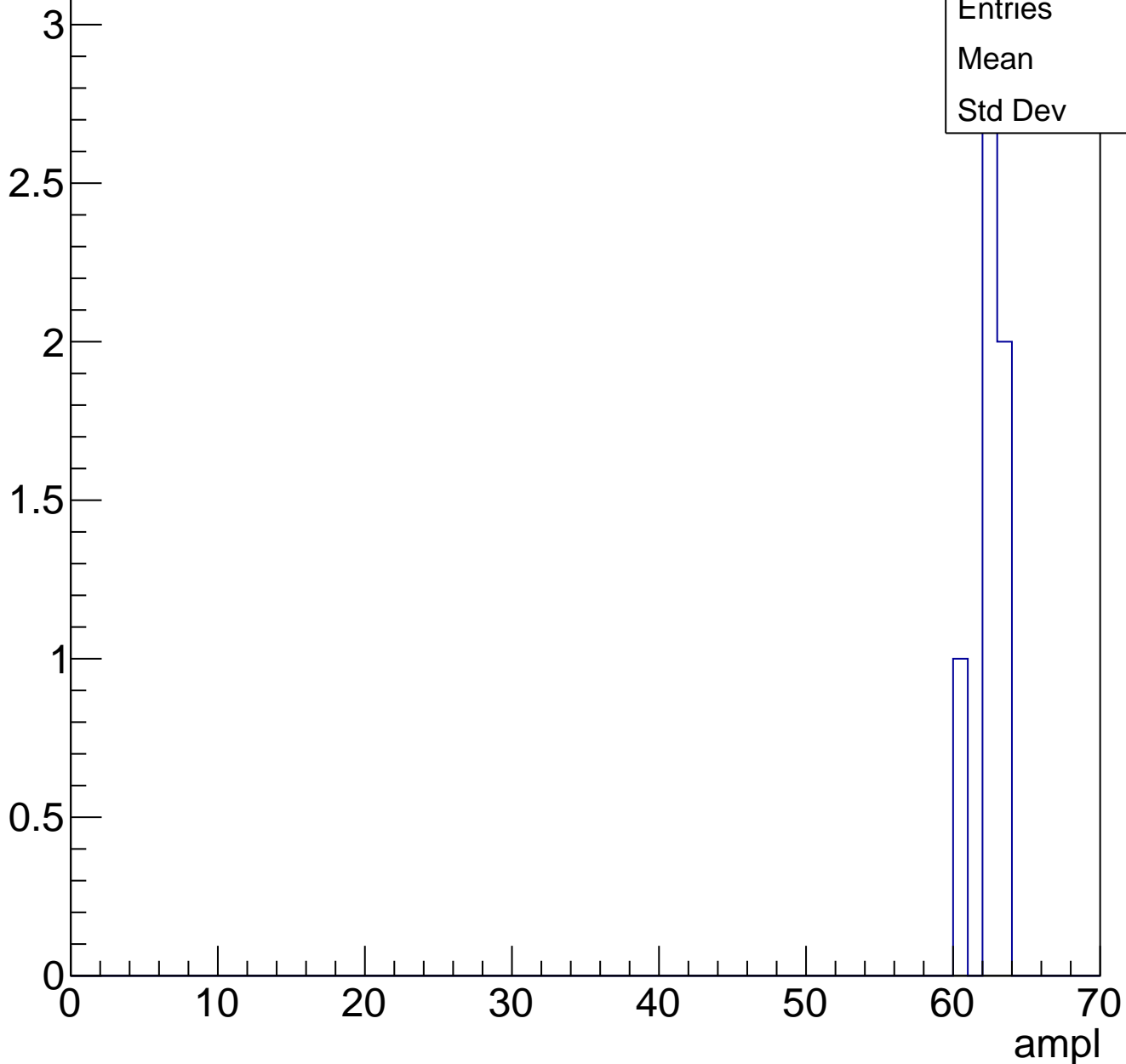
Entries	53
Mean	58.34
Std Dev	8.552



# B1L103S, U2-ch119, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U2-ch119, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch120, adc0

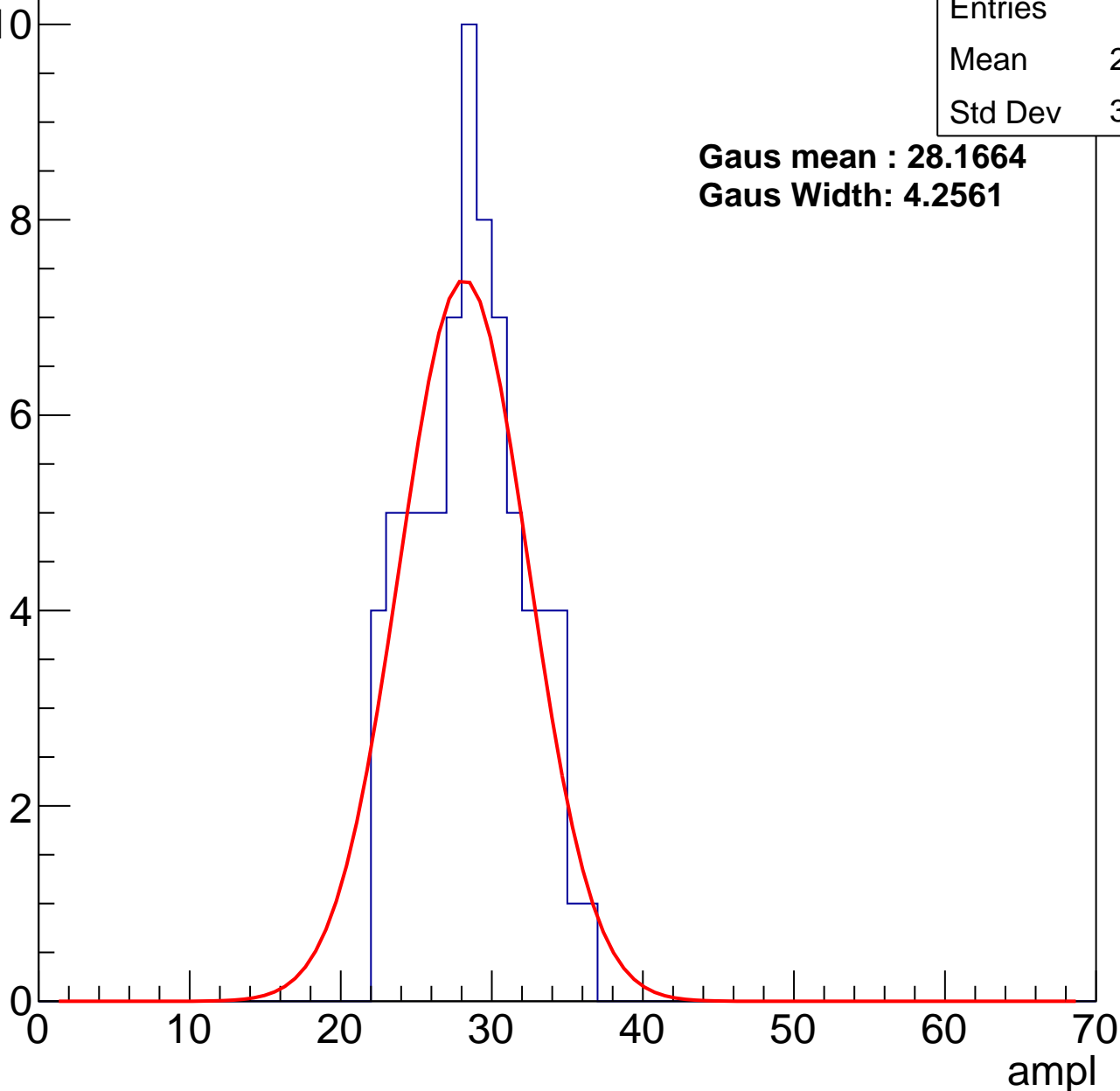
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	28.15
Std Dev	3.505

**Gaus mean : 28.1664**

**Gaus Width: 4.2561**



# B1L103S, U2-ch120, adc1

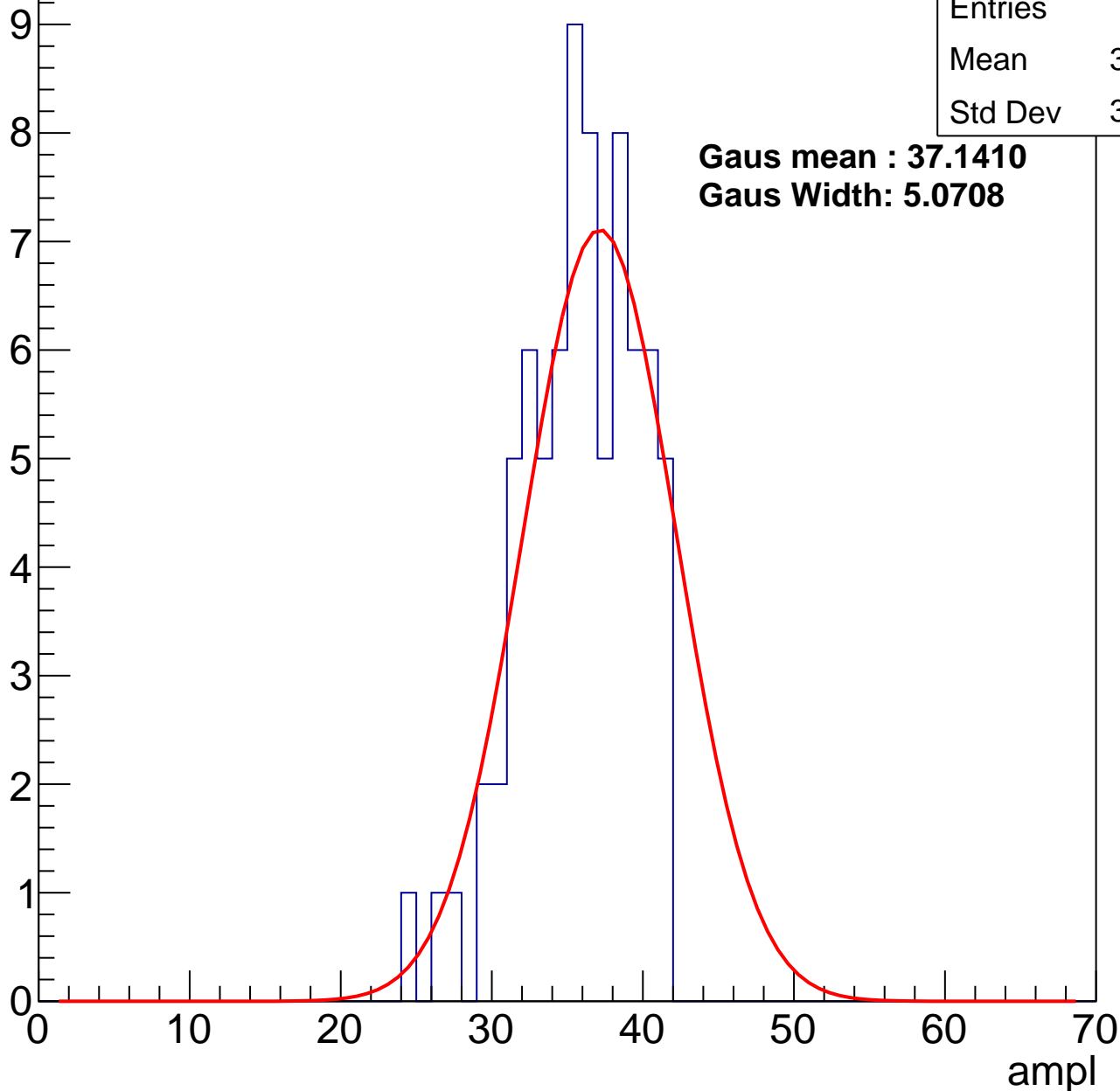
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	35.29
Std Dev	3.748

**Gaus mean : 37.1410**

**Gaus Width: 5.0708**



# B1L103S, U2-ch120, adc2

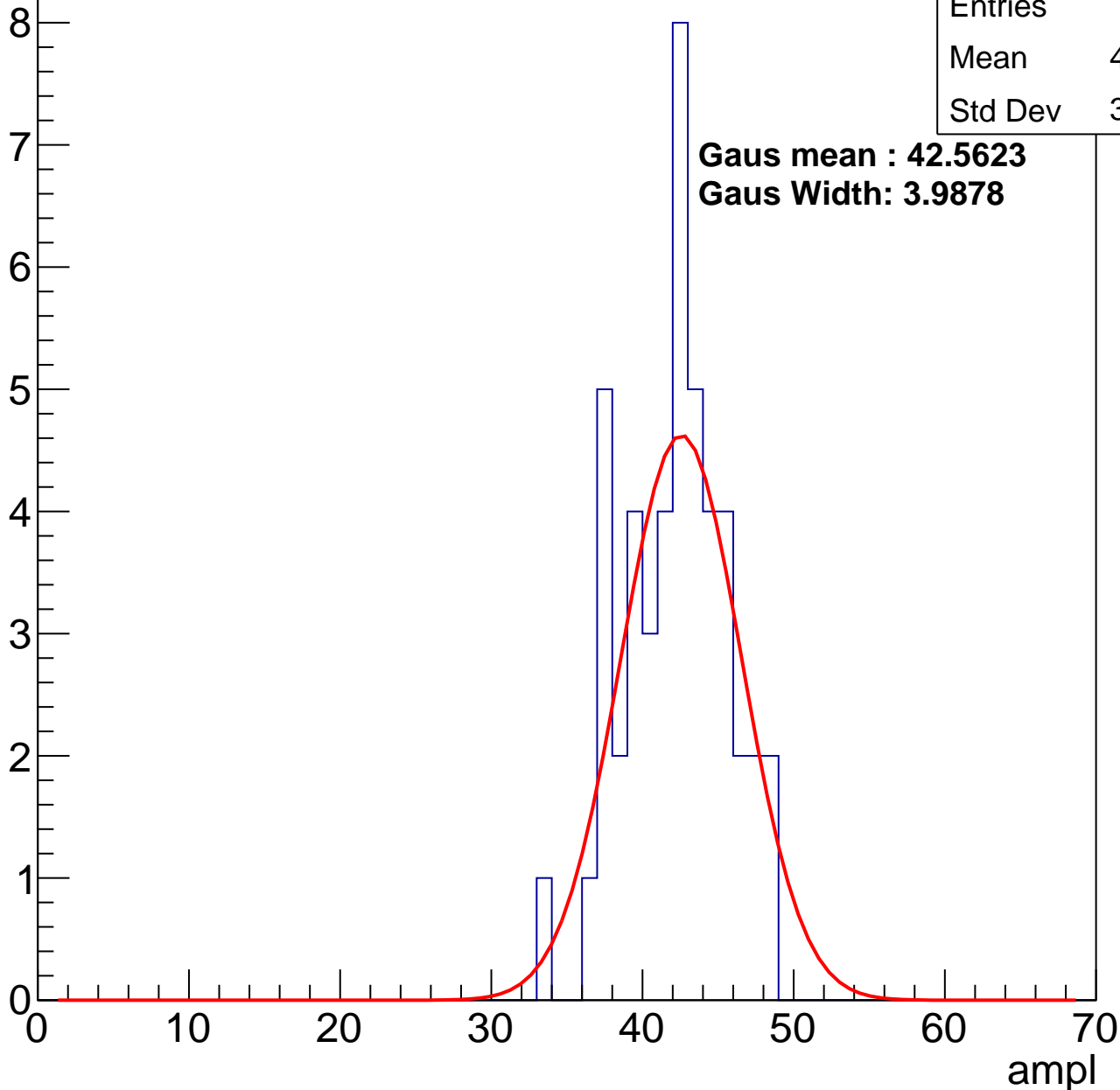
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	47
Mean	41.68
Std Dev	3.365

**Gaus mean : 42.5623**

**Gaus Width: 3.9878**

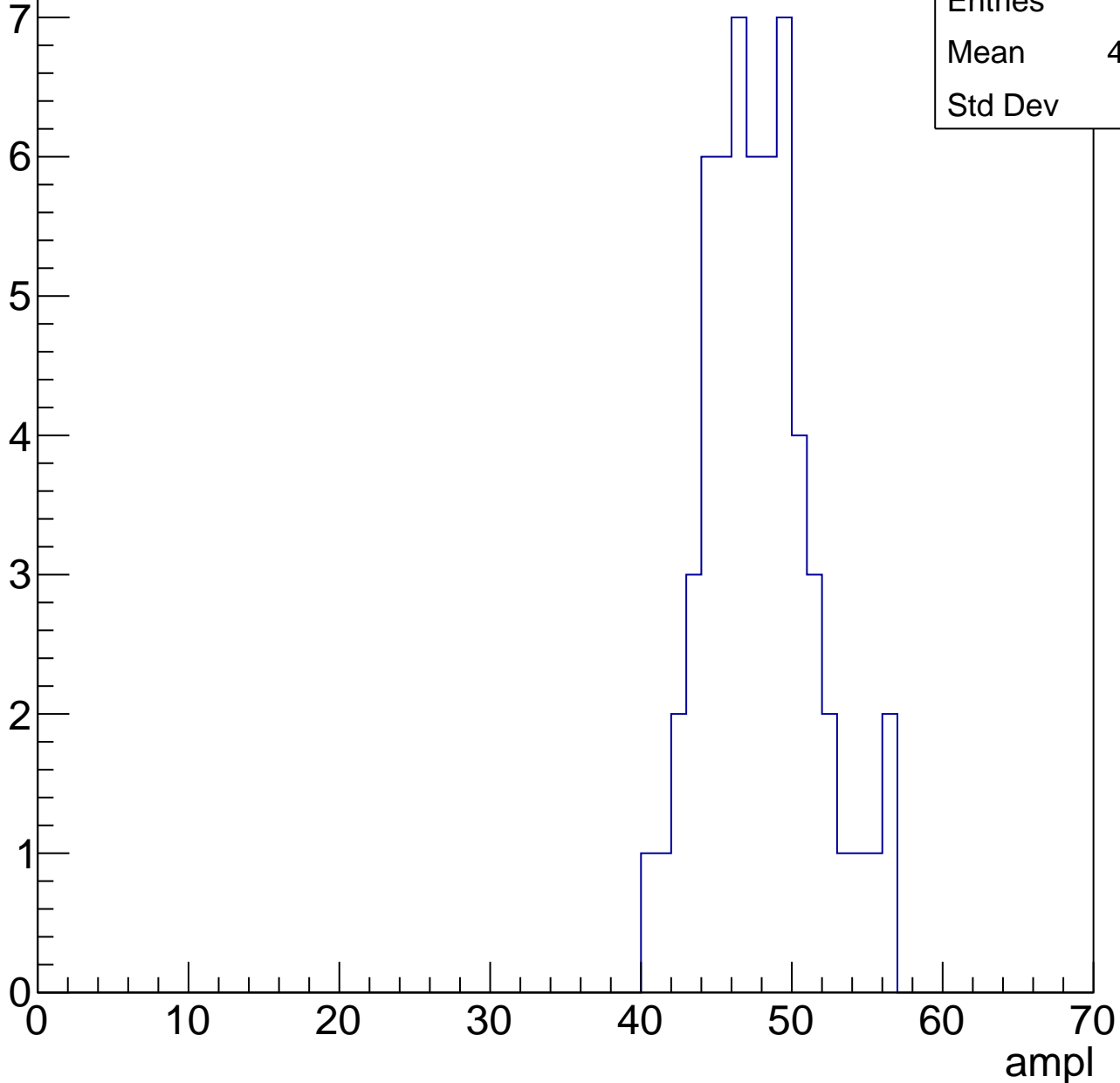


# B1L103S, U2-ch120, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

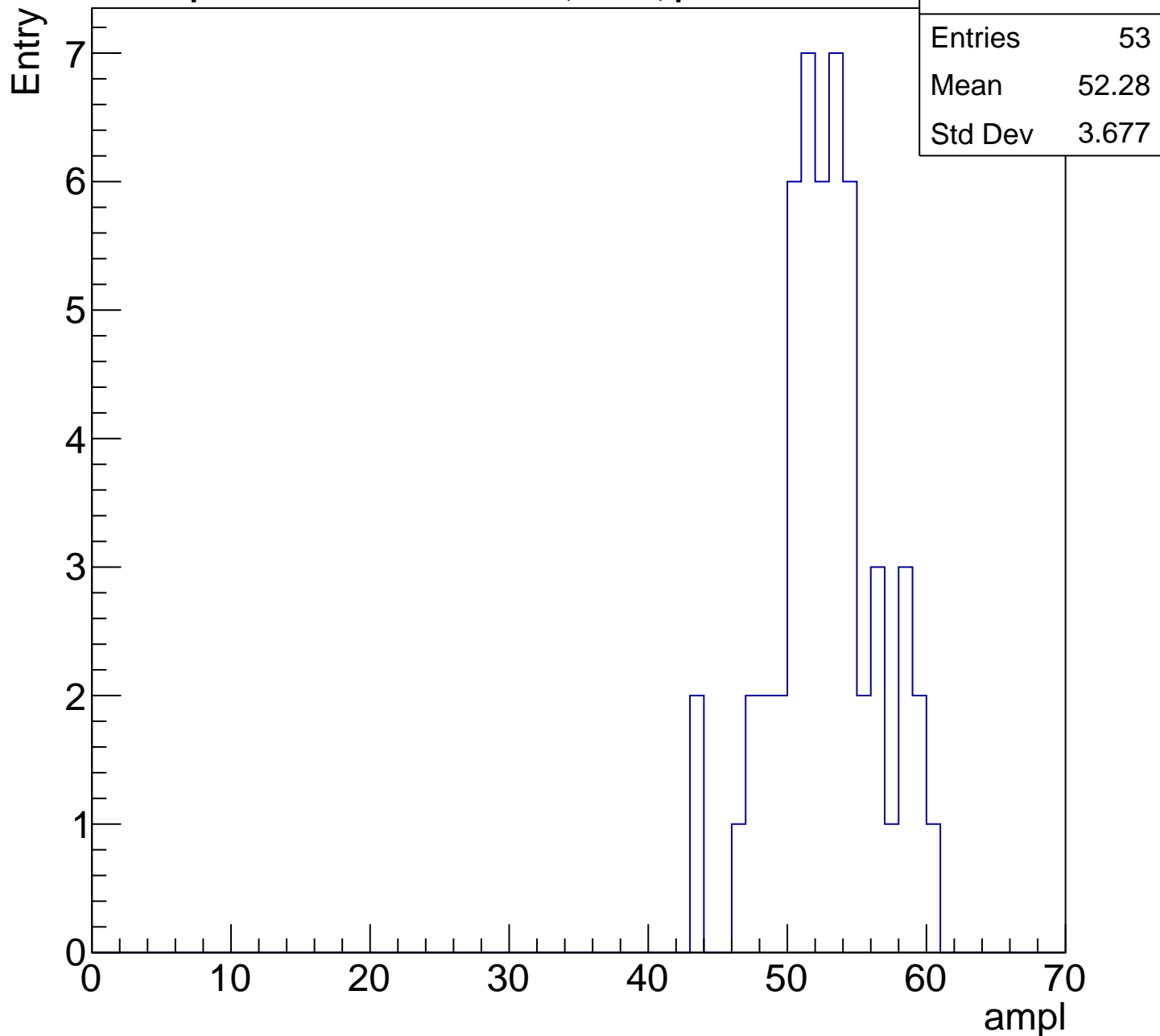
Entry

Entries	59
Mean	47.36
Std Dev	3.54



# B1L103S, U2-ch120, adc4

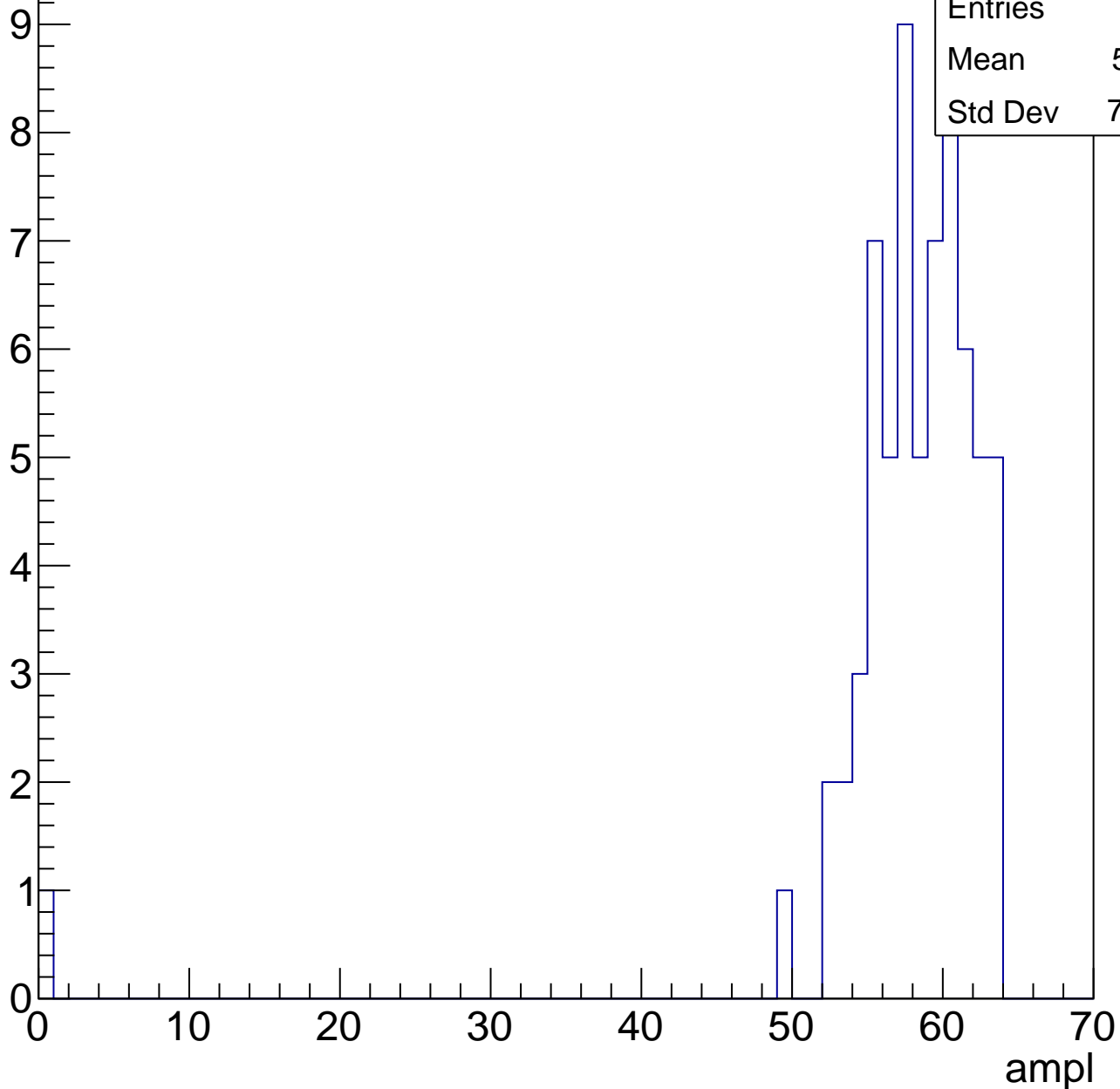
calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U2-ch120, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

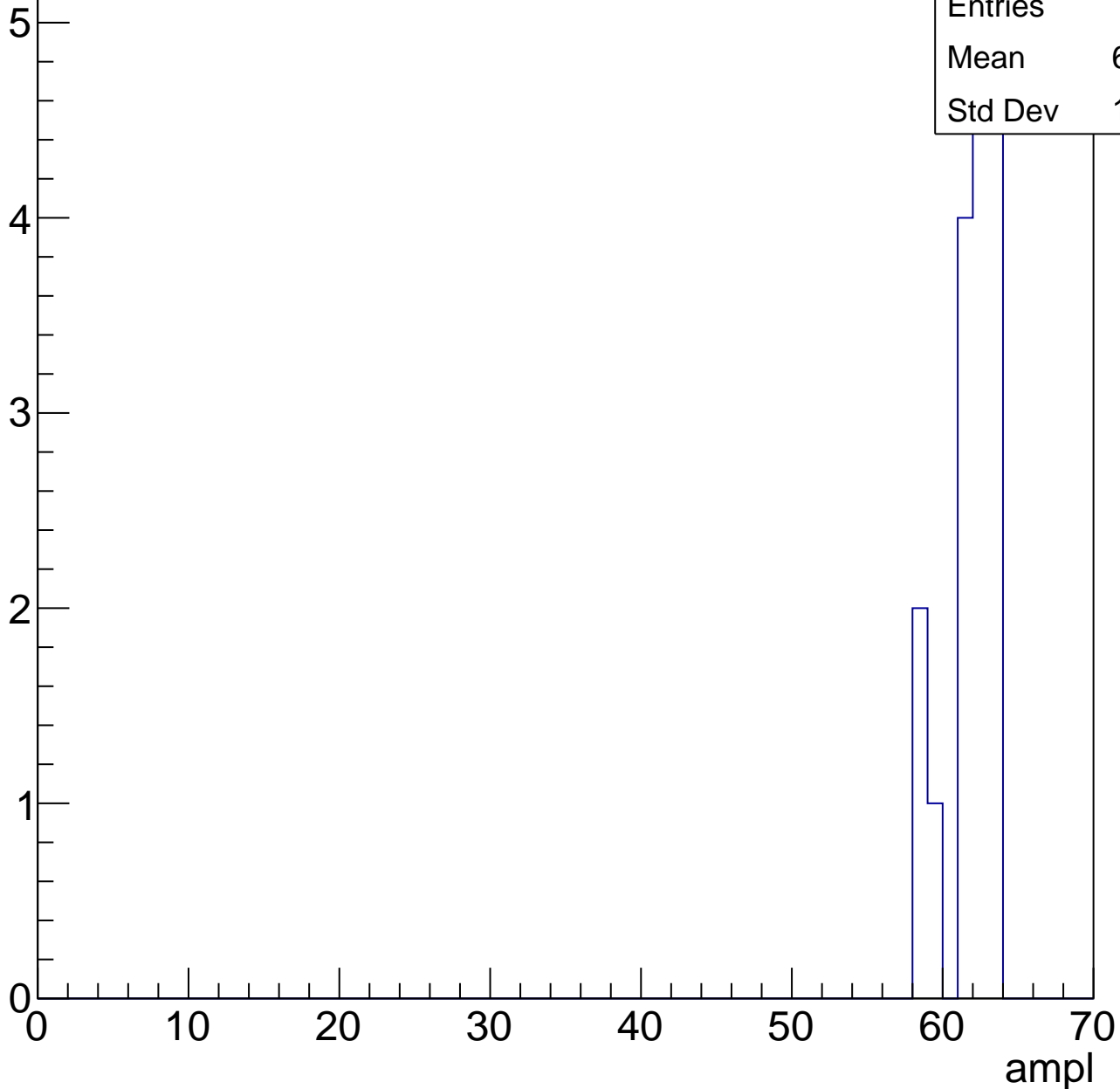


# B1L103S, U2-ch120, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	17
Mean	61.41
Std Dev	1.611





# B1L103S, U2-ch120, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch121, adc0

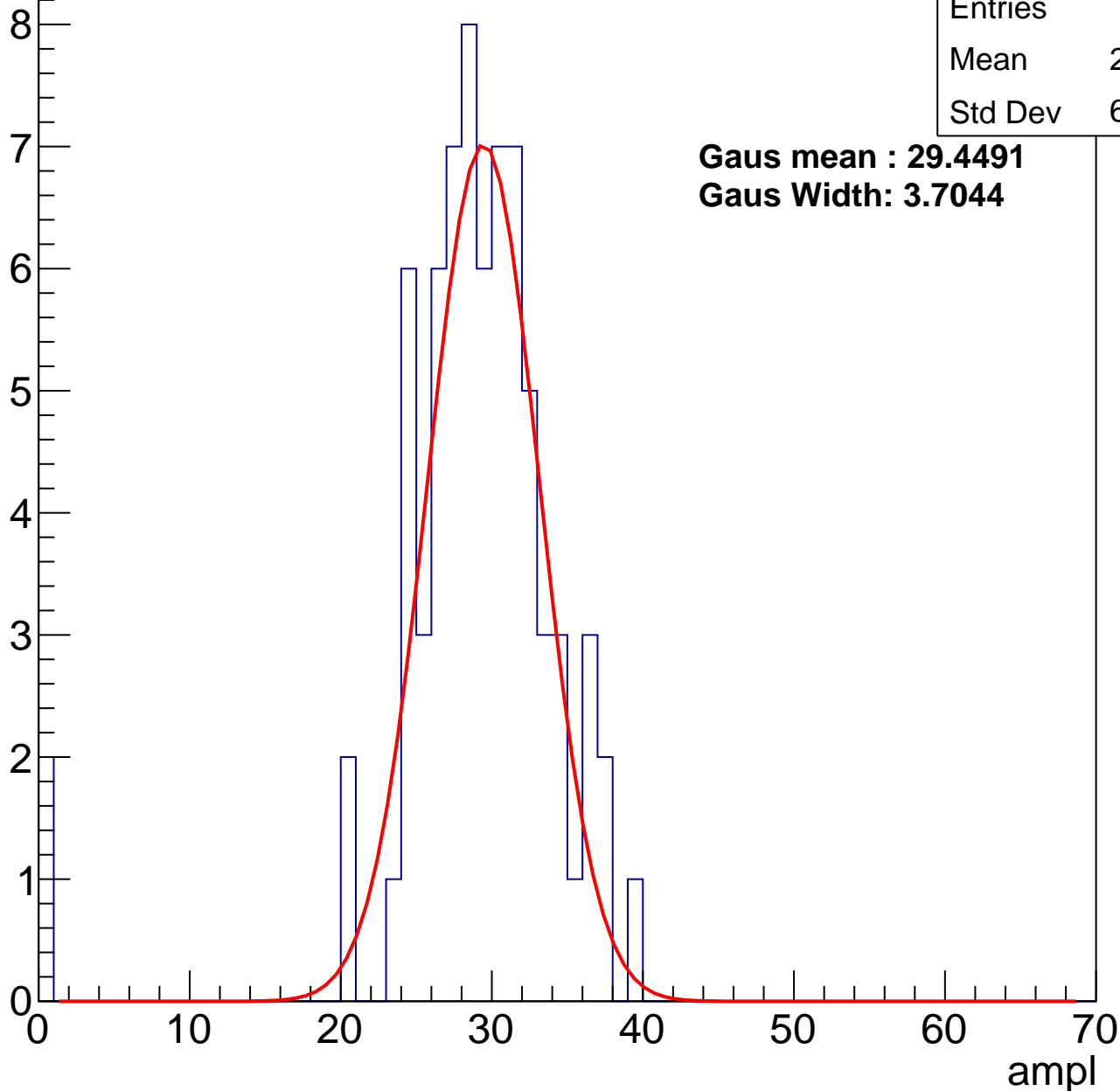
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	28.34
Std Dev	6.138

**Gaus mean : 29.4491**

**Gaus Width: 3.7044**



# B1L103S, U2-ch121, adc1

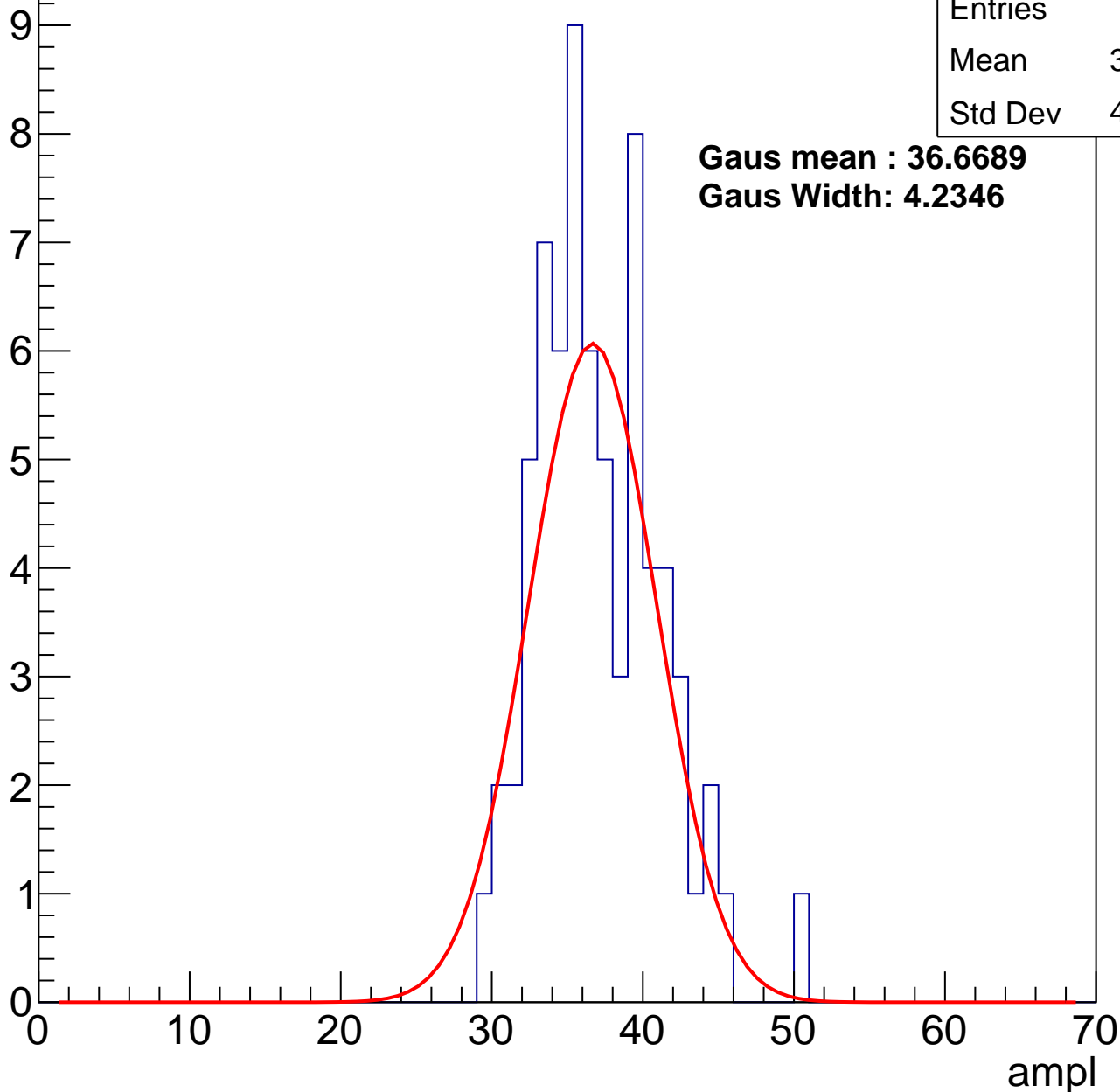
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	36.63
Std Dev	4.026

**Gaus mean : 36.6689**

**Gaus Width: 4.2346**



# B1L103S, U2-ch121, adc2

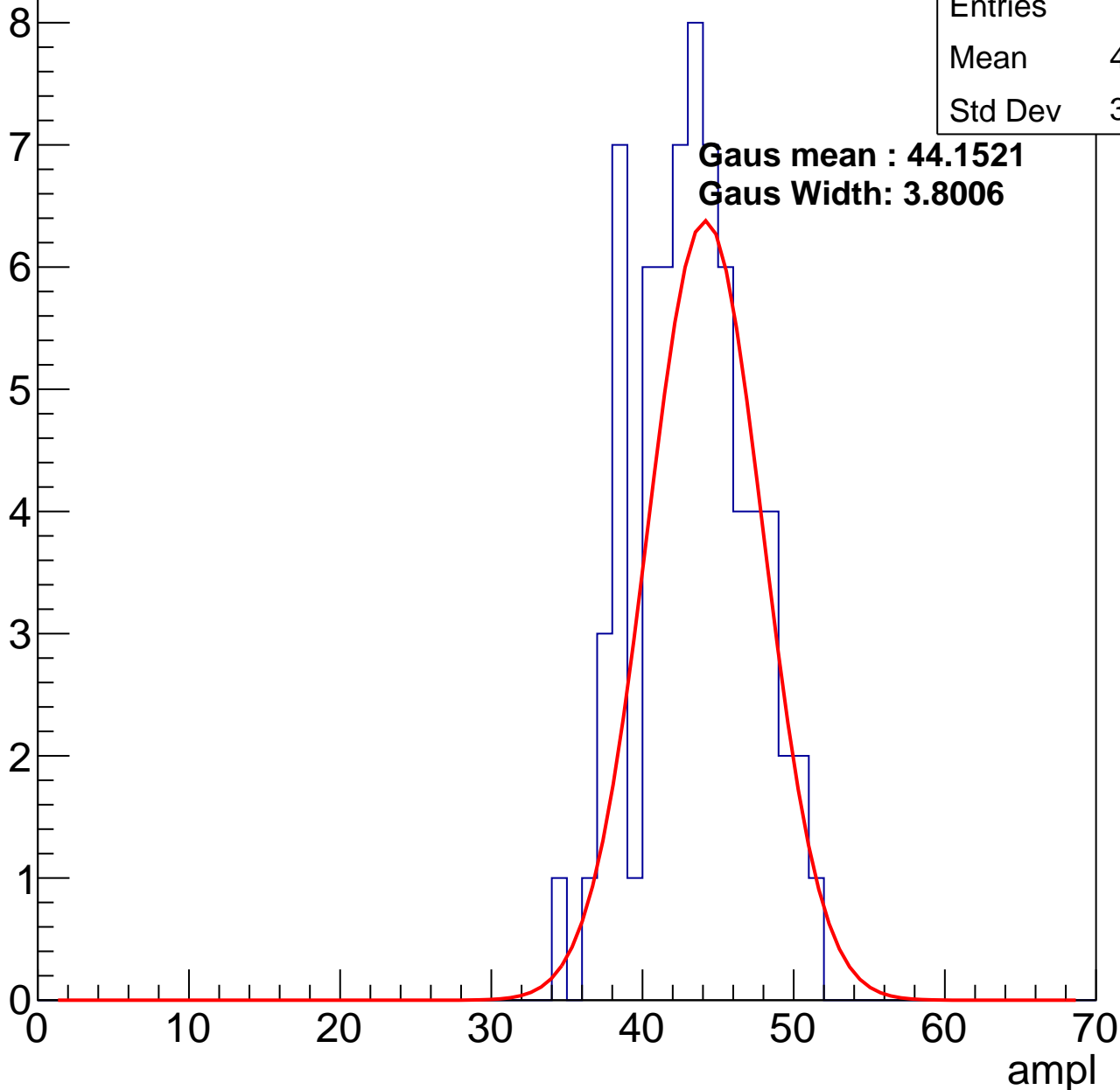
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	42.87
Std Dev	3.738

**Gaus mean : 44.1521**

**Gaus Width: 3.8006**

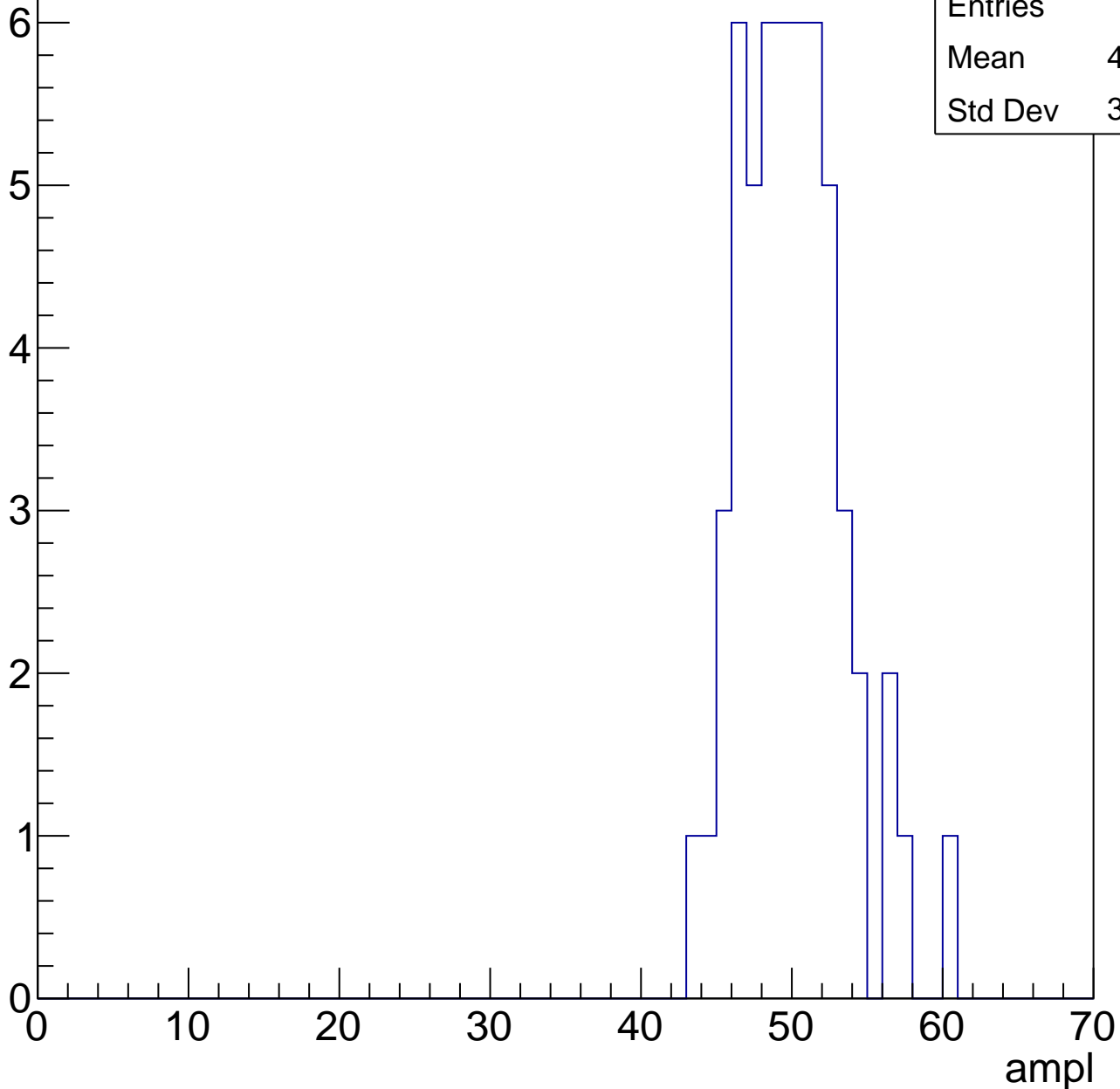


# B1L103S, U2-ch121, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

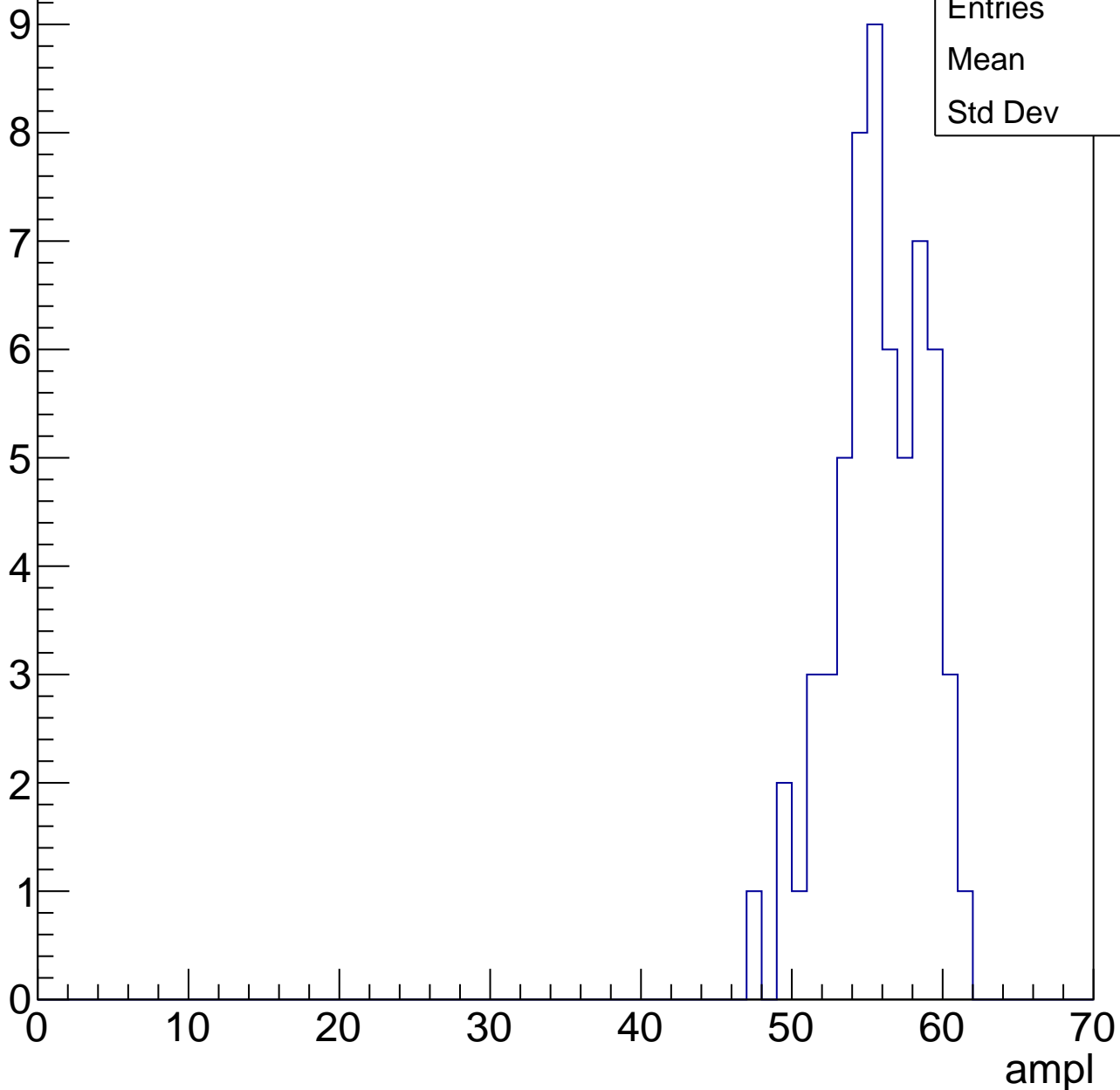
Entries	54
Mean	49.57
Std Dev	3.408



# B1L103S, U2-ch121, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



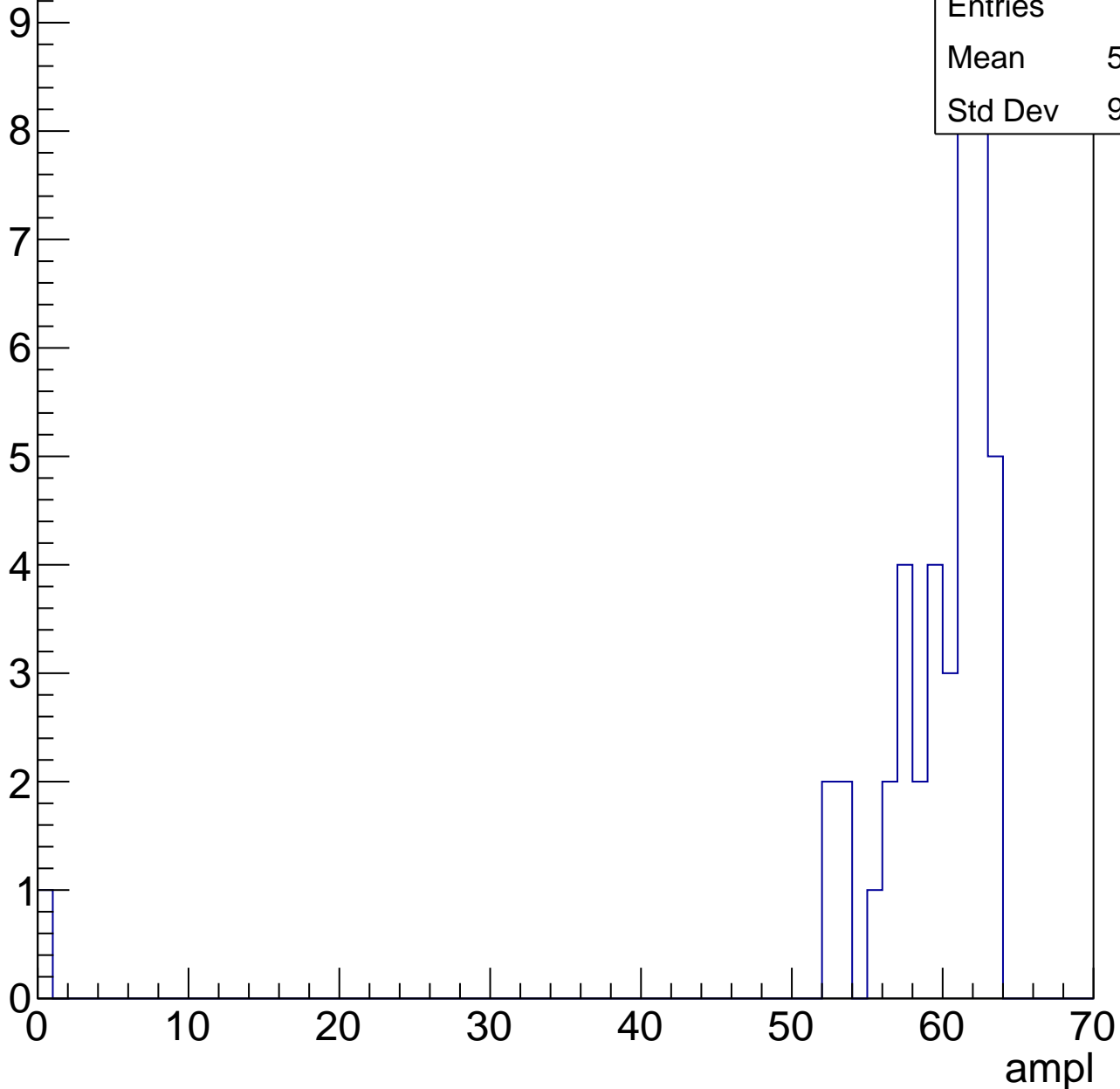
Entries	60
Mean	55.3
Std Dev	3.04

# B1L103S, U2-ch121, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

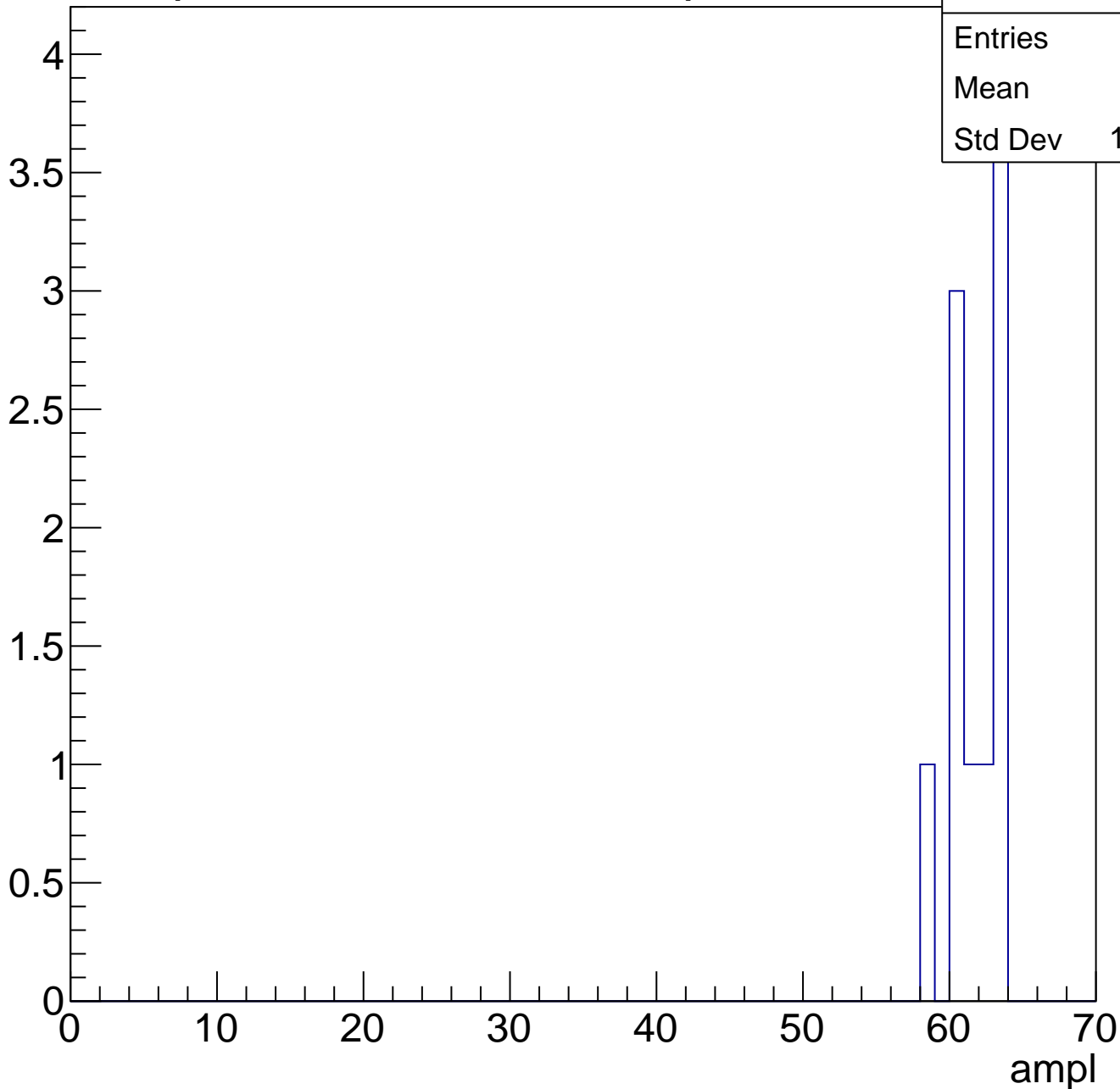
Entries	43
Mean	58.09
Std Dev	9.479



# B1L103S, U2-ch121, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U2-ch121, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch122, adc0

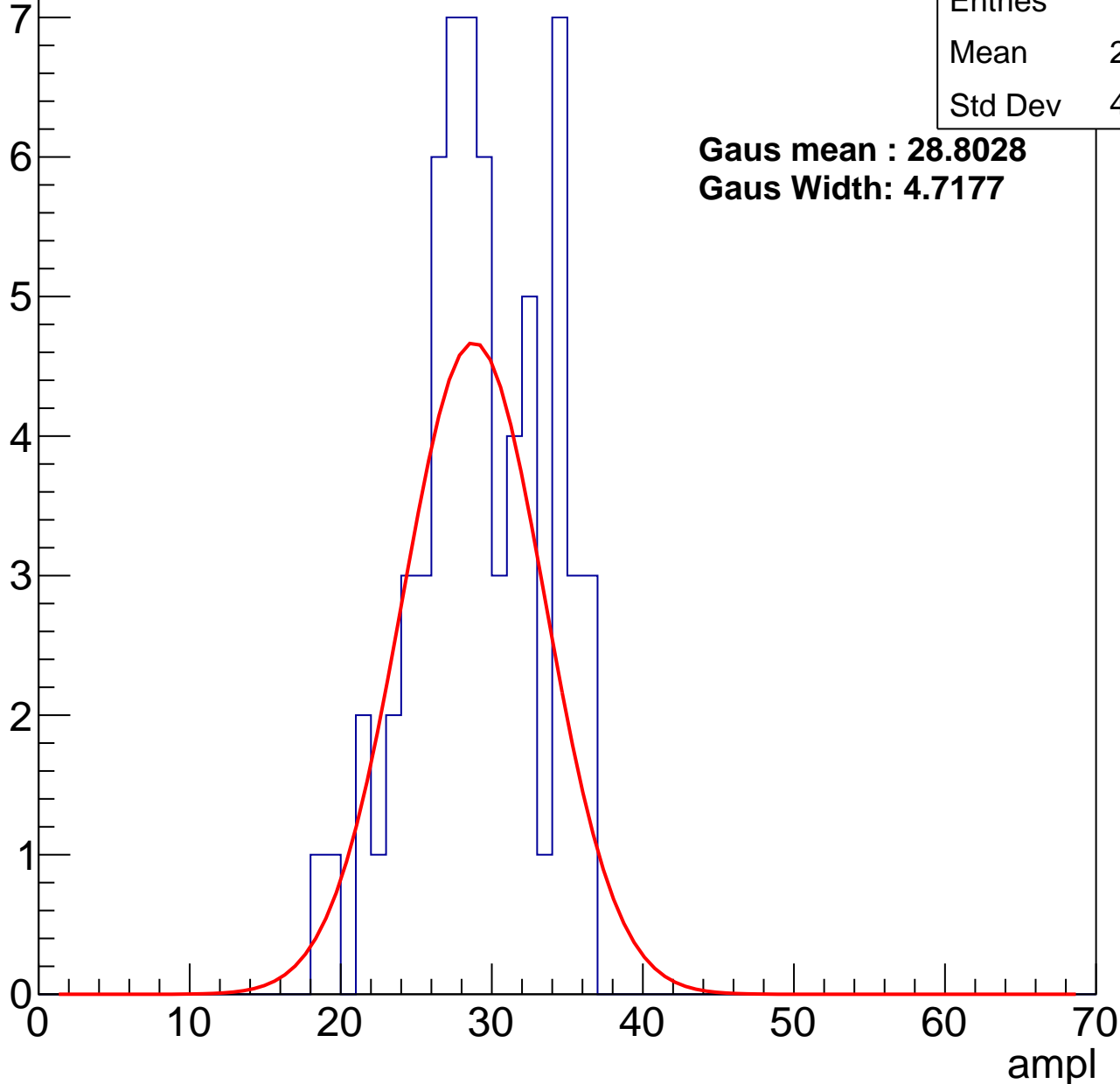
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	28.72
Std Dev	4.273

**Gaus mean : 28.8028**

**Gaus Width: 4.7177**



# B1L103S, U2-ch122, adc1

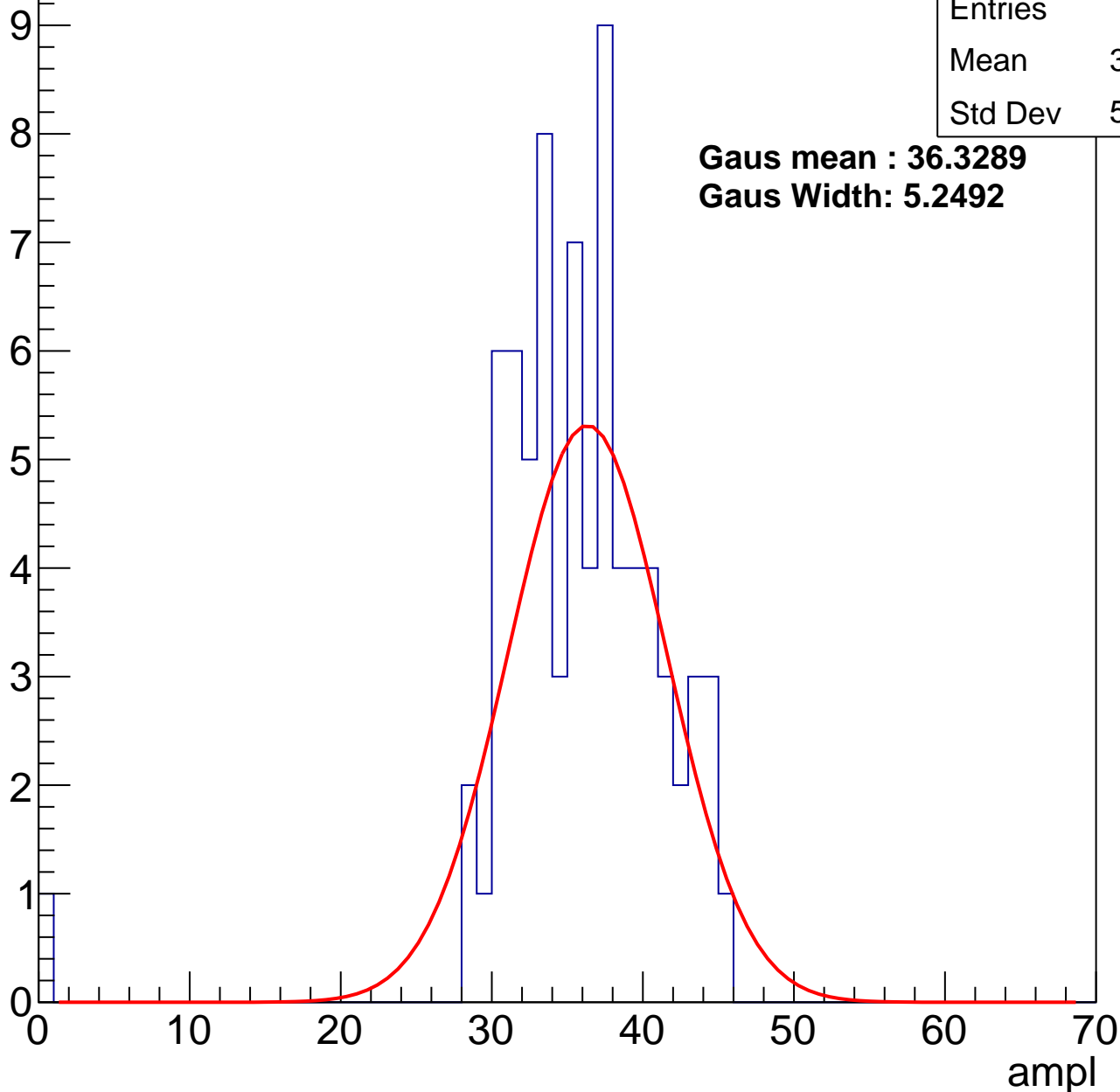
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	35.26
Std Dev	5.917

**Gaus mean : 36.3289**

**Gaus Width: 5.2492**



# B1L103S, U2-ch122, adc2

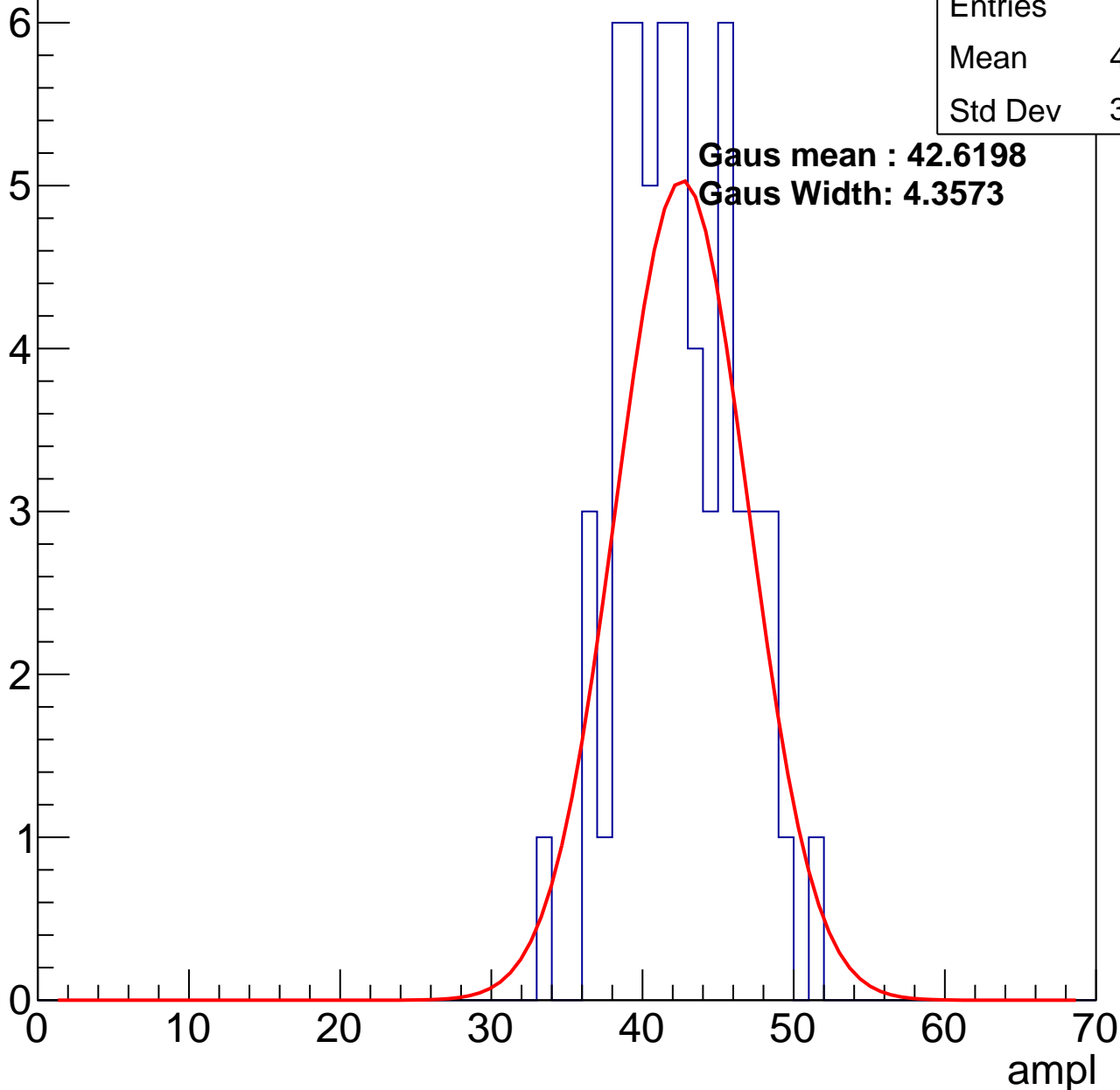
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	41.98
Std Dev	3.762

**Gaus mean : 42.6198**

**Gaus Width: 4.3573**

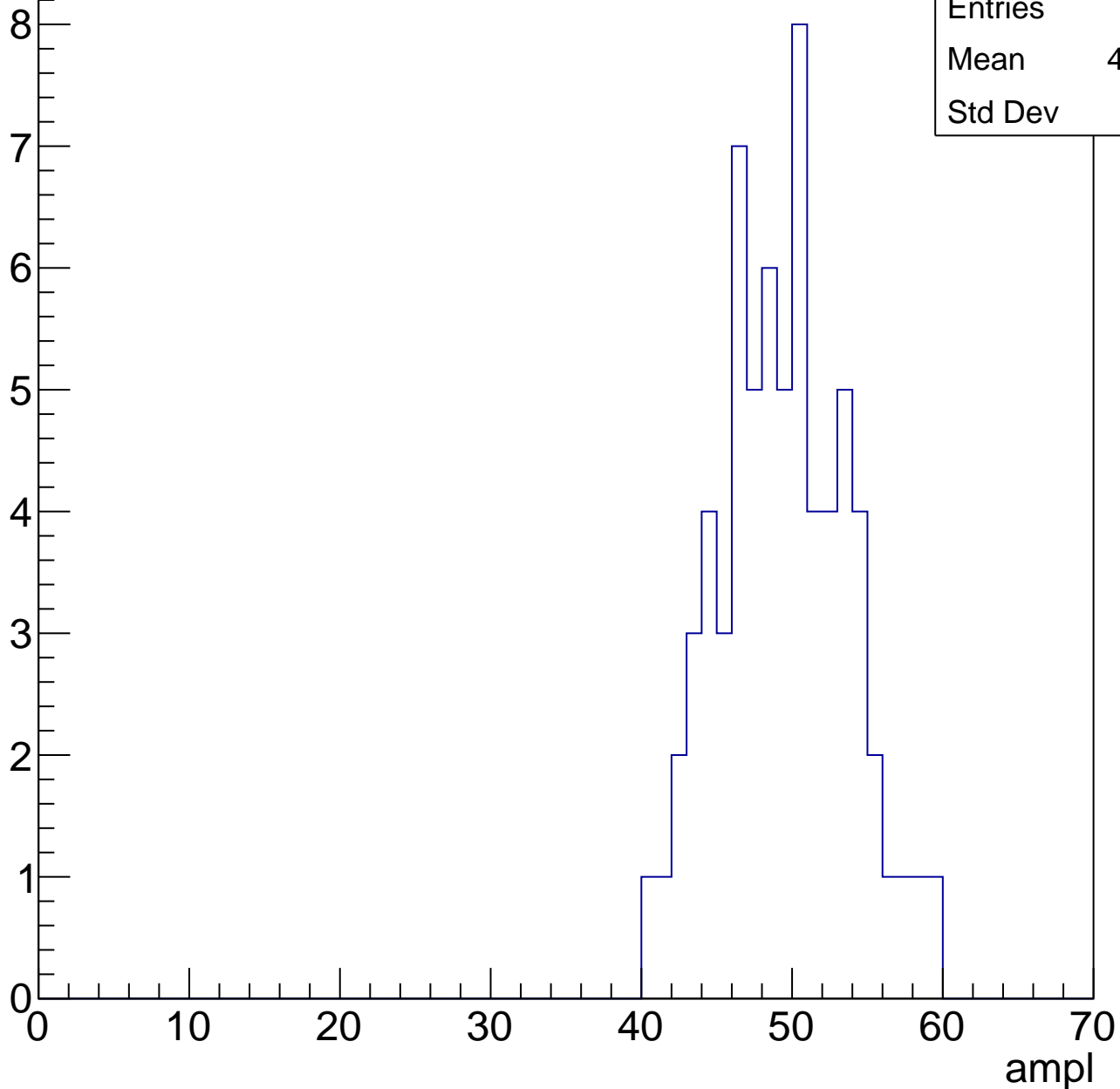


# B1L103S, U2-ch122, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	48.94
Std Dev	4.19

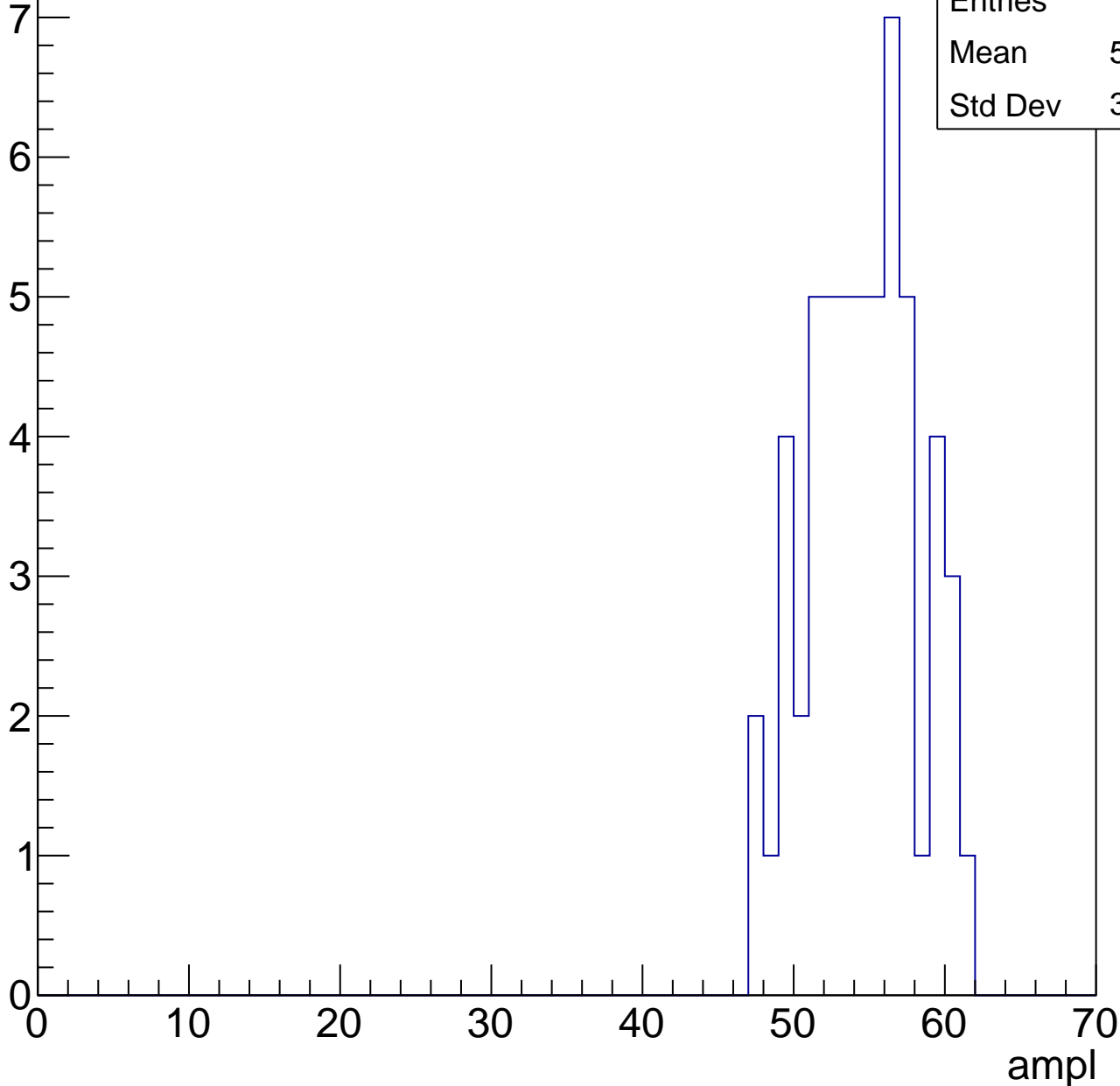


# B1L103S, U2-ch122, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	54.09
Std Dev	3.533

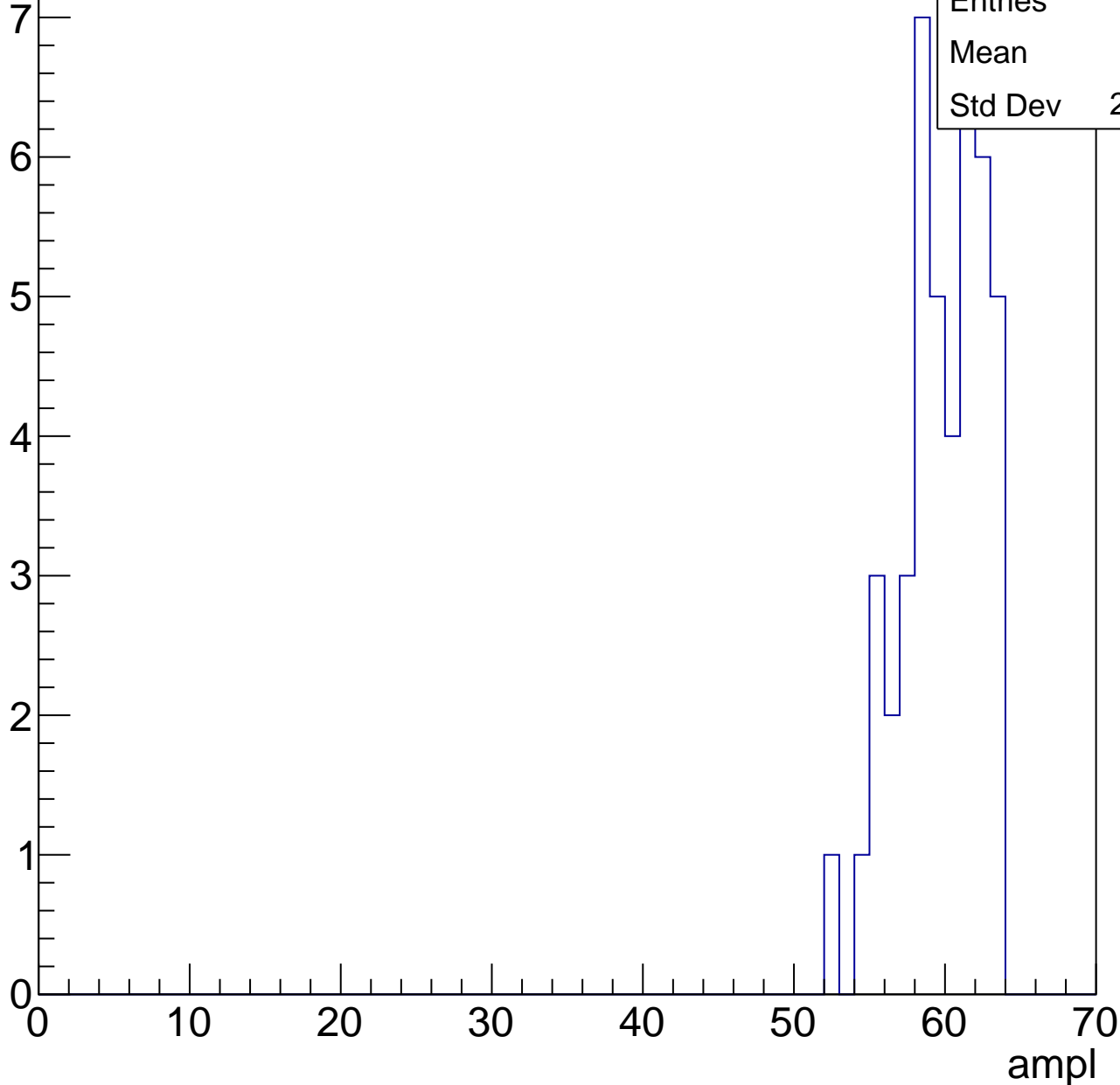


# B1L103S, U2-ch122, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	44
Mean	59.3
Std Dev	2.702

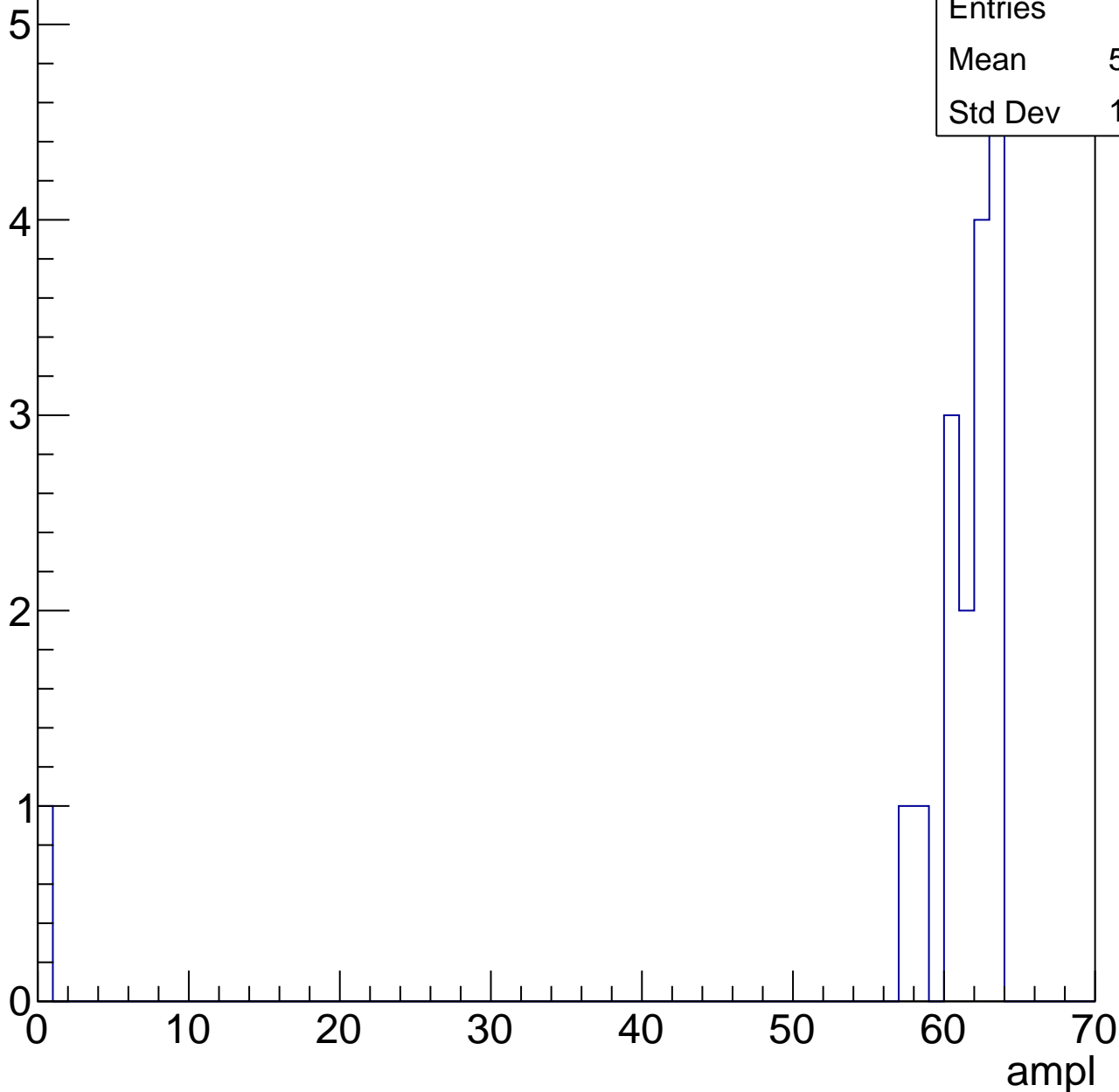


# B1L103S, U2-ch122, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	17
Mean	57.65
Std Dev	14.52





# B1L103S, U2-ch122, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U2-ch123, adc0

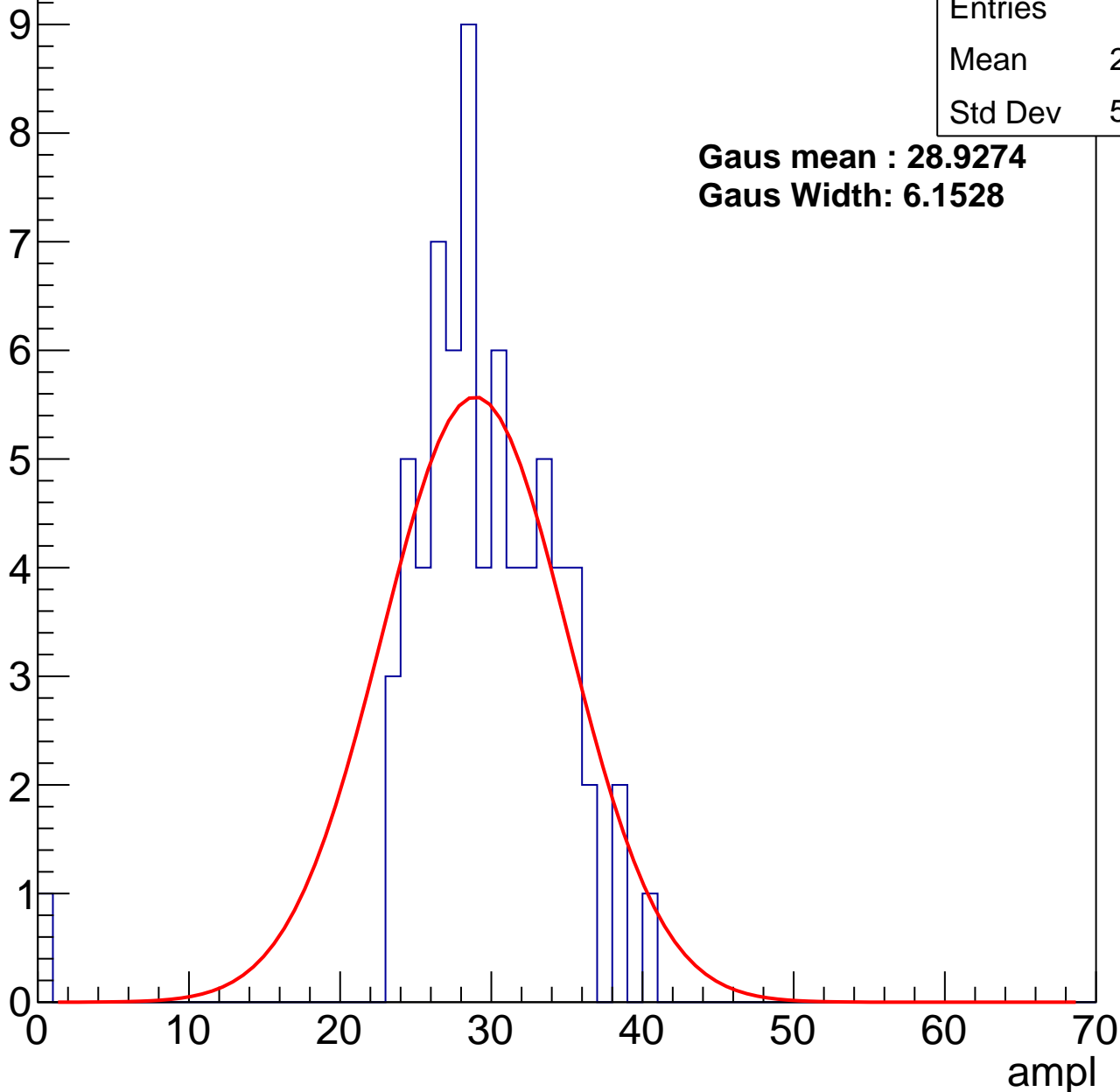
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	29.04
Std Dev	5.303

**Gaus mean : 28.9274**

**Gaus Width: 6.1528**



# B1L103S, U2-ch123, adc1

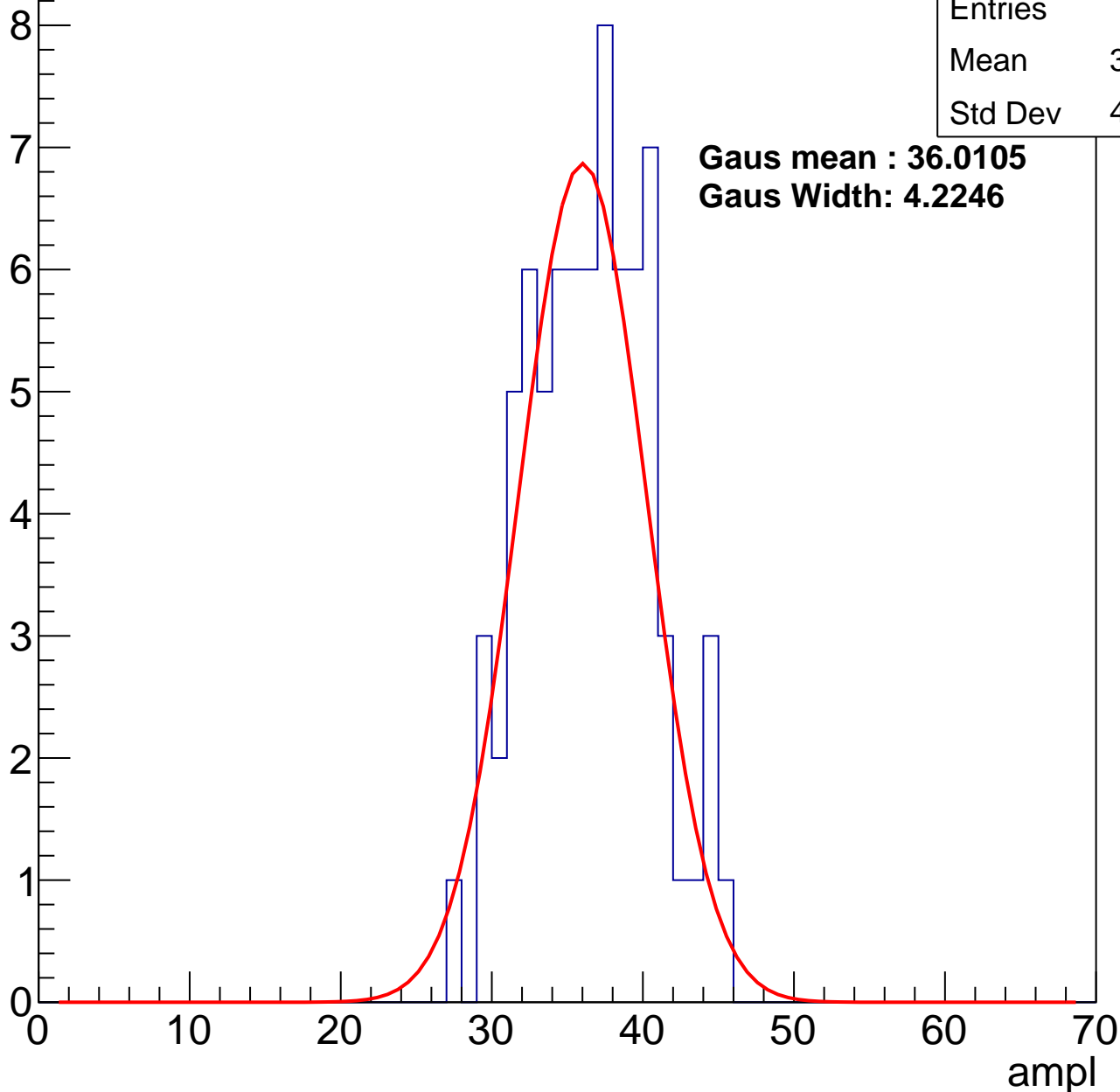
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	36.04
Std Dev	4.018

**Gaus mean : 36.0105**

**Gaus Width: 4.2246**



# B1L103S, U2-ch123, adc2

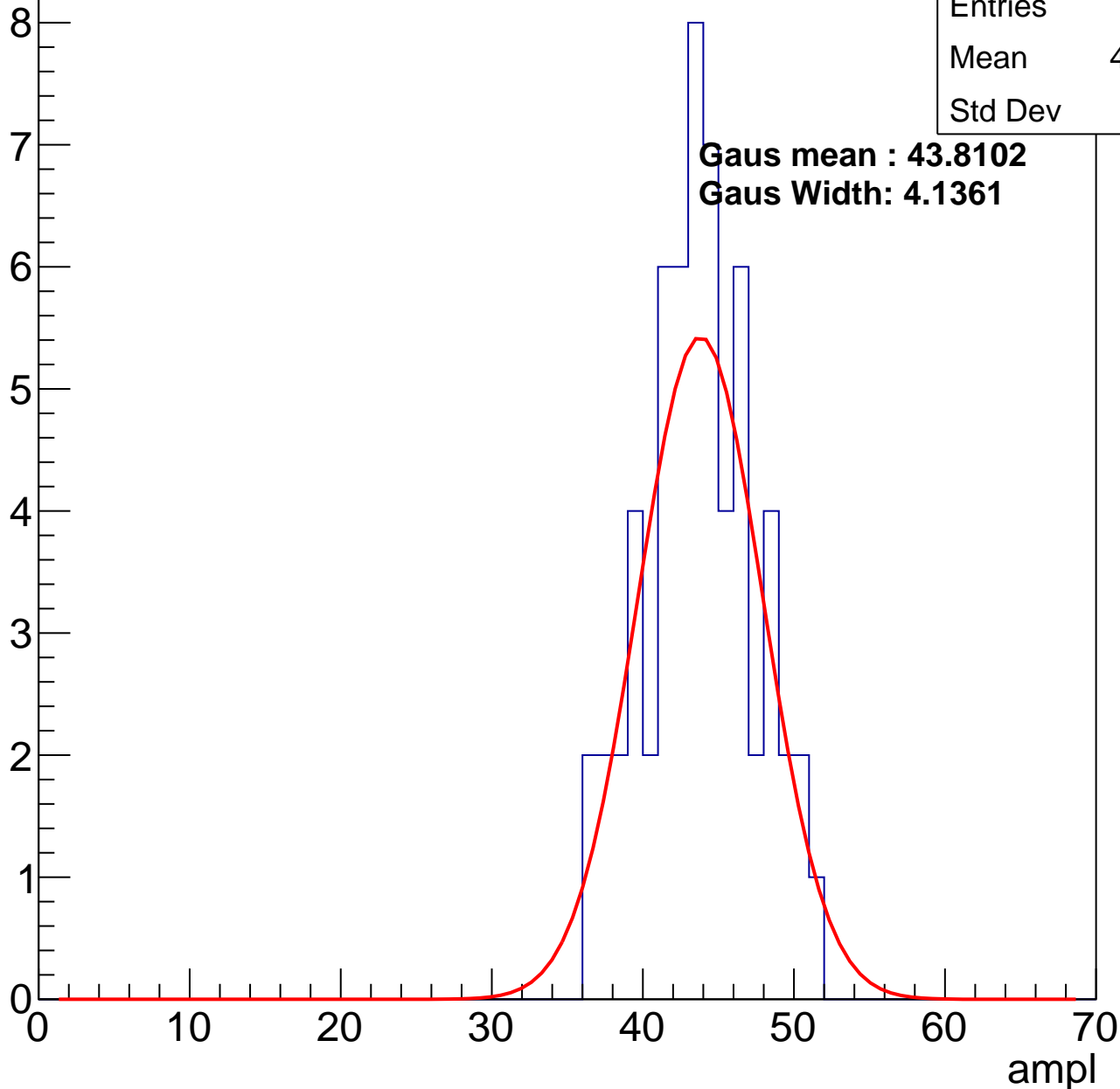
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	43.32
Std Dev	3.58

**Gaus mean : 43.8102**

**Gaus Width: 4.1361**

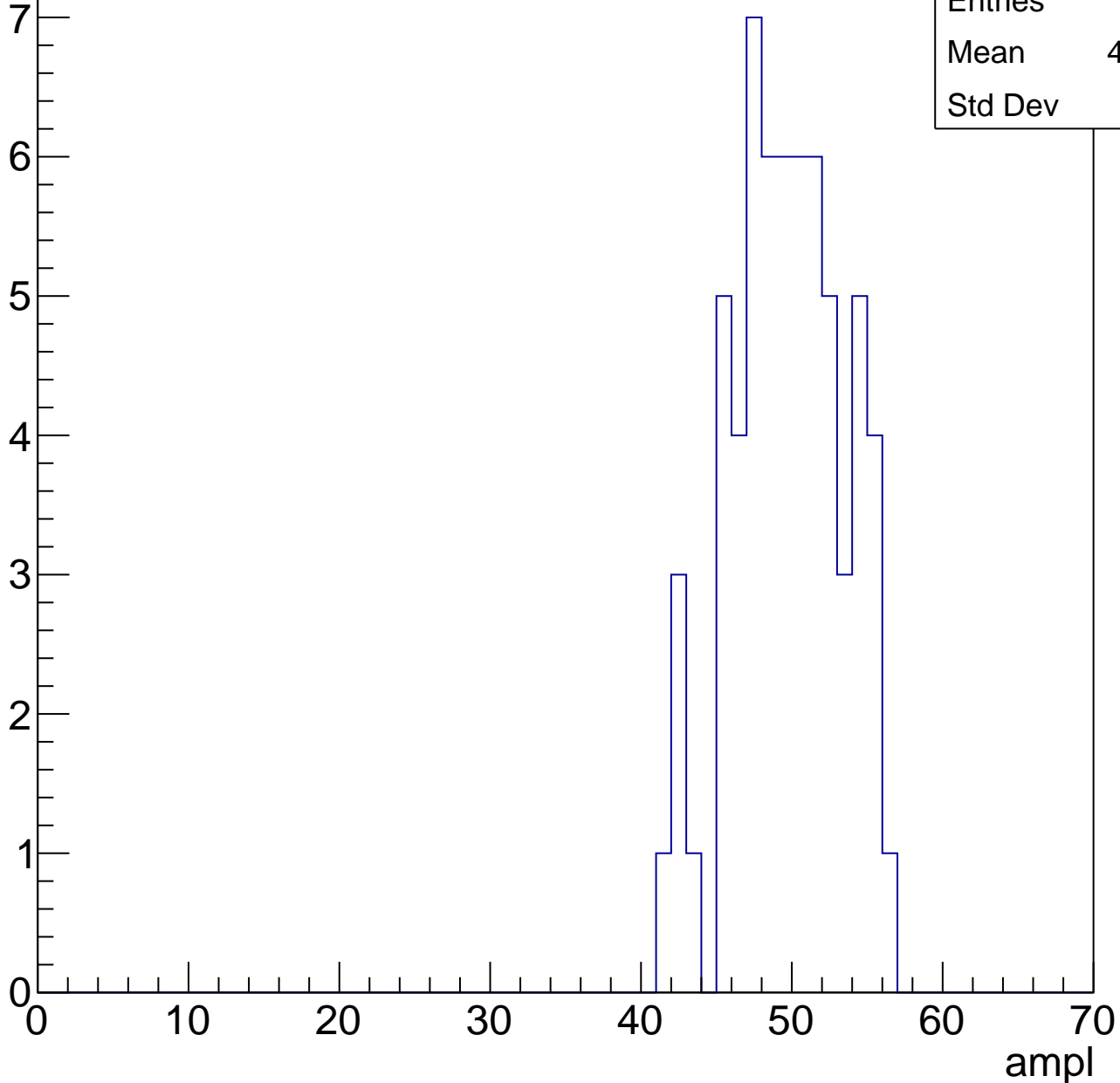


# B1L103S, U2-ch123, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	49.22
Std Dev	3.64

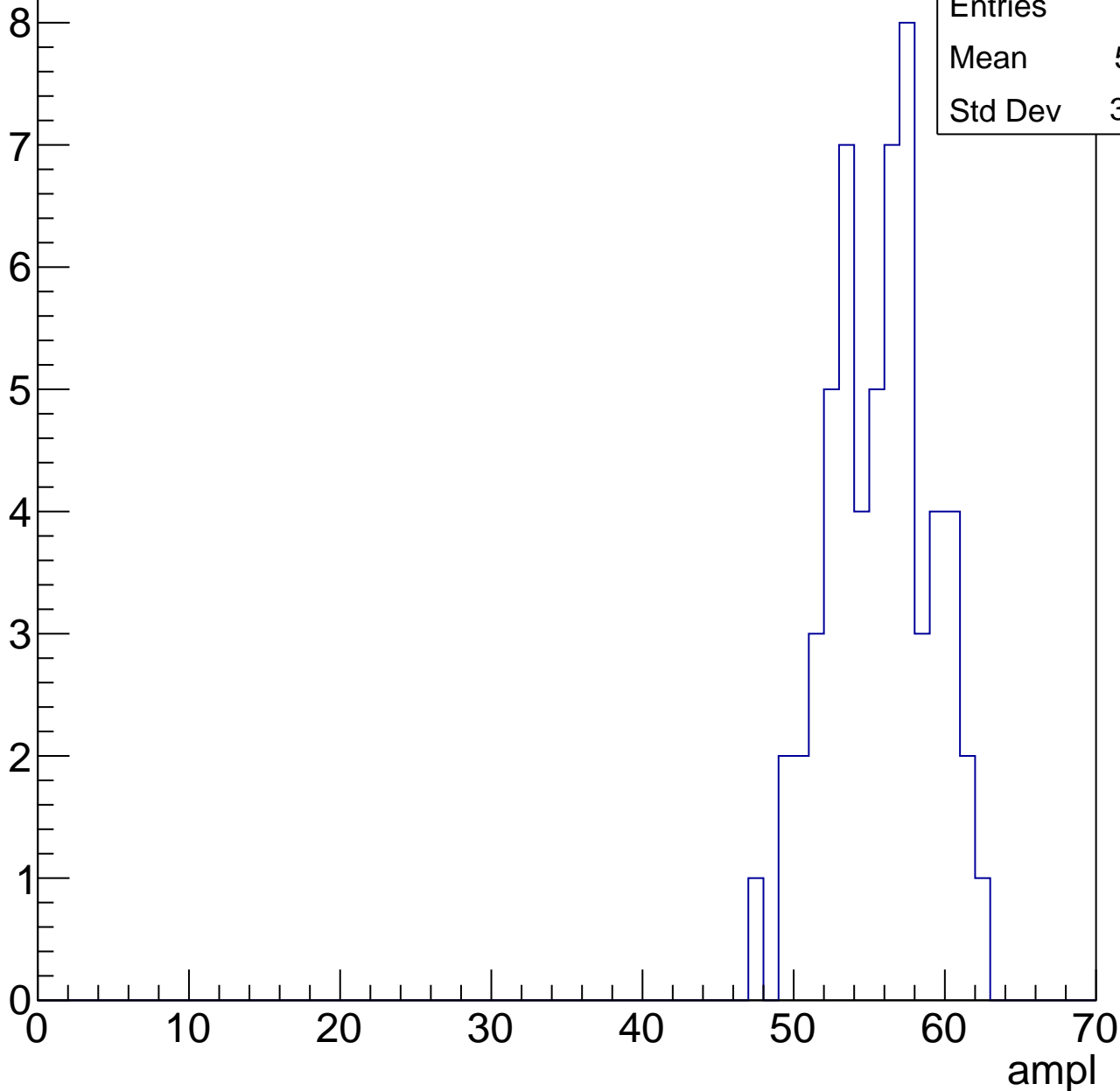


# B1L103S, U2-ch123, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	55.21
Std Dev	3.372



# B1L103S, U2-ch123, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

7

6

5

4

3

2

1

0

Entries	41
Mean	59.68
Std Dev	2.279

ampl

0

10

20

30

40

50

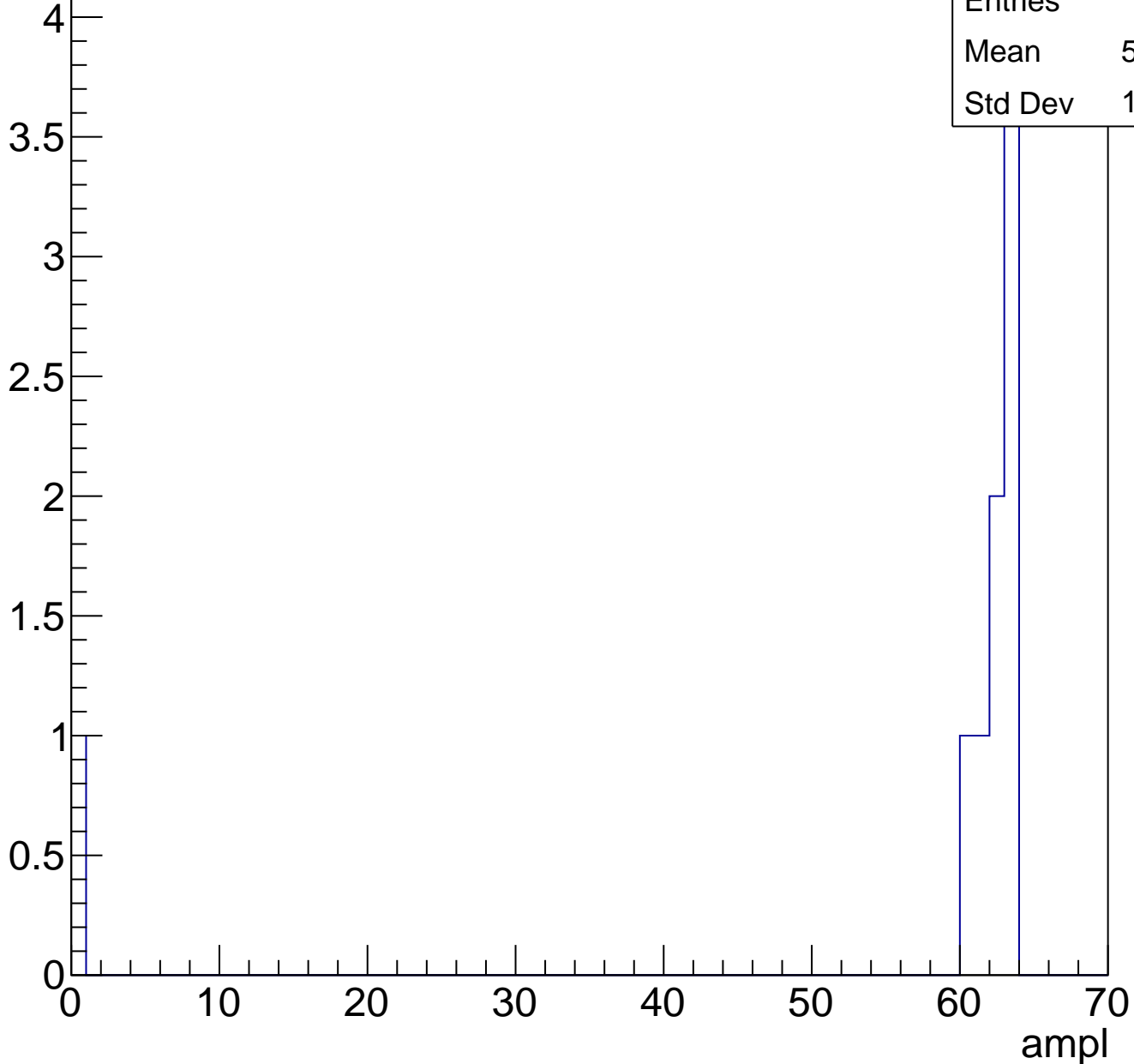
60

70

# B1L103S, U2-ch123, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

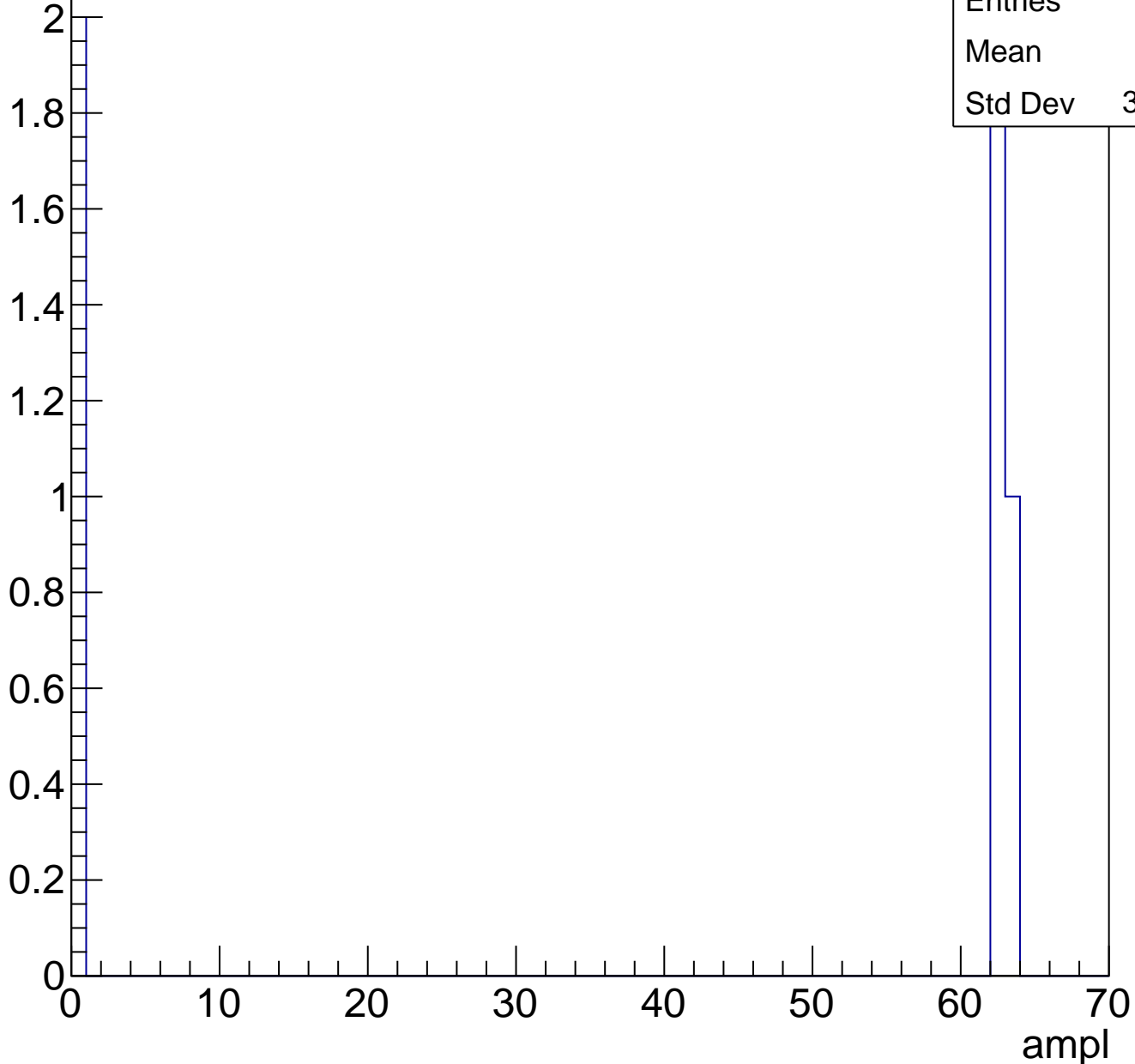




# B1L103S, U2-ch123, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	5
Mean	37.4
Std Dev	30.54

# B1L103S, U2-ch124, adc0

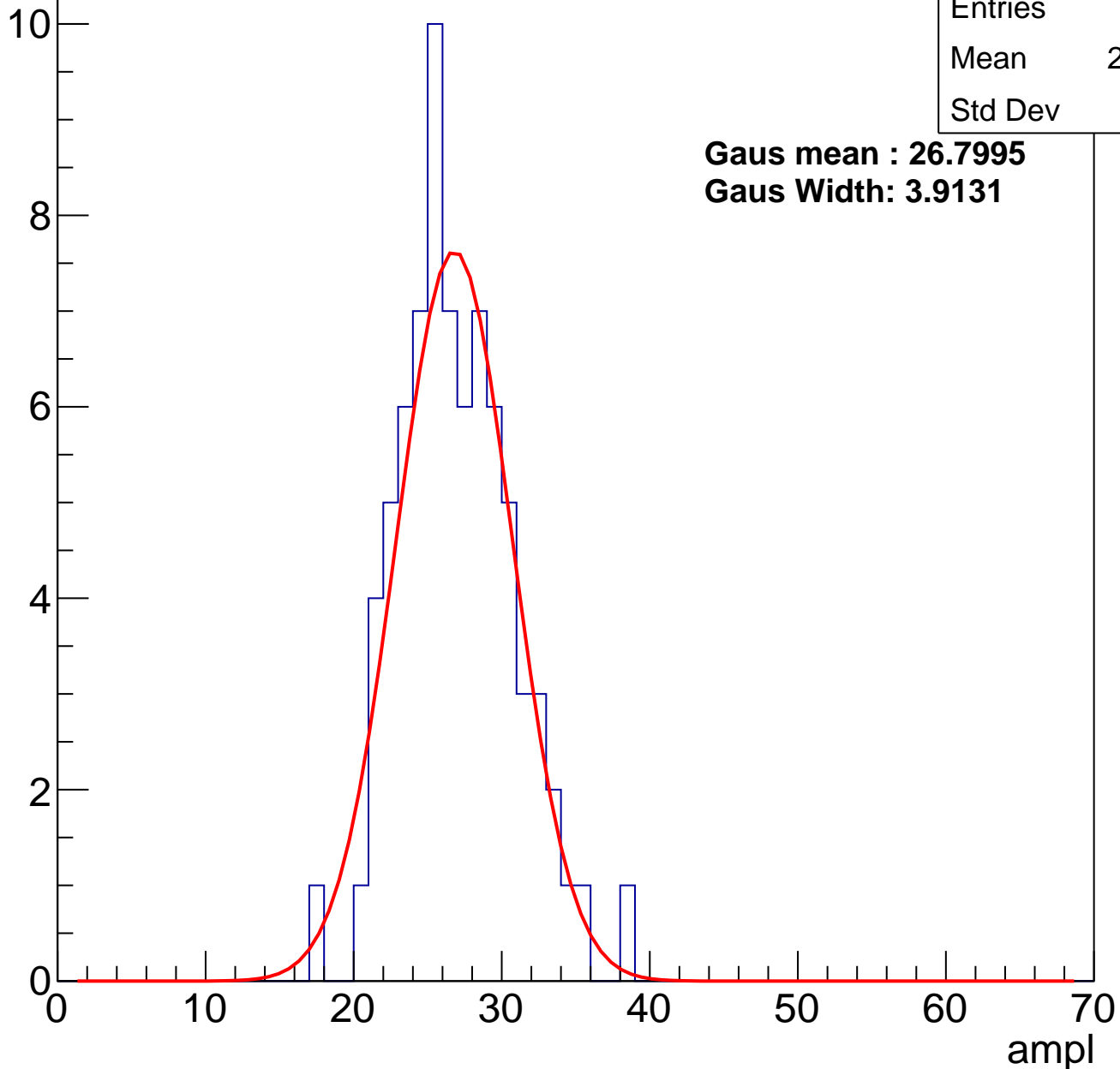
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	76
Mean	26.49
Std Dev	3.82

**Gaus mean : 26.7995**

**Gaus Width: 3.9131**

Entry



# B1L103S, U2-ch124, adc1

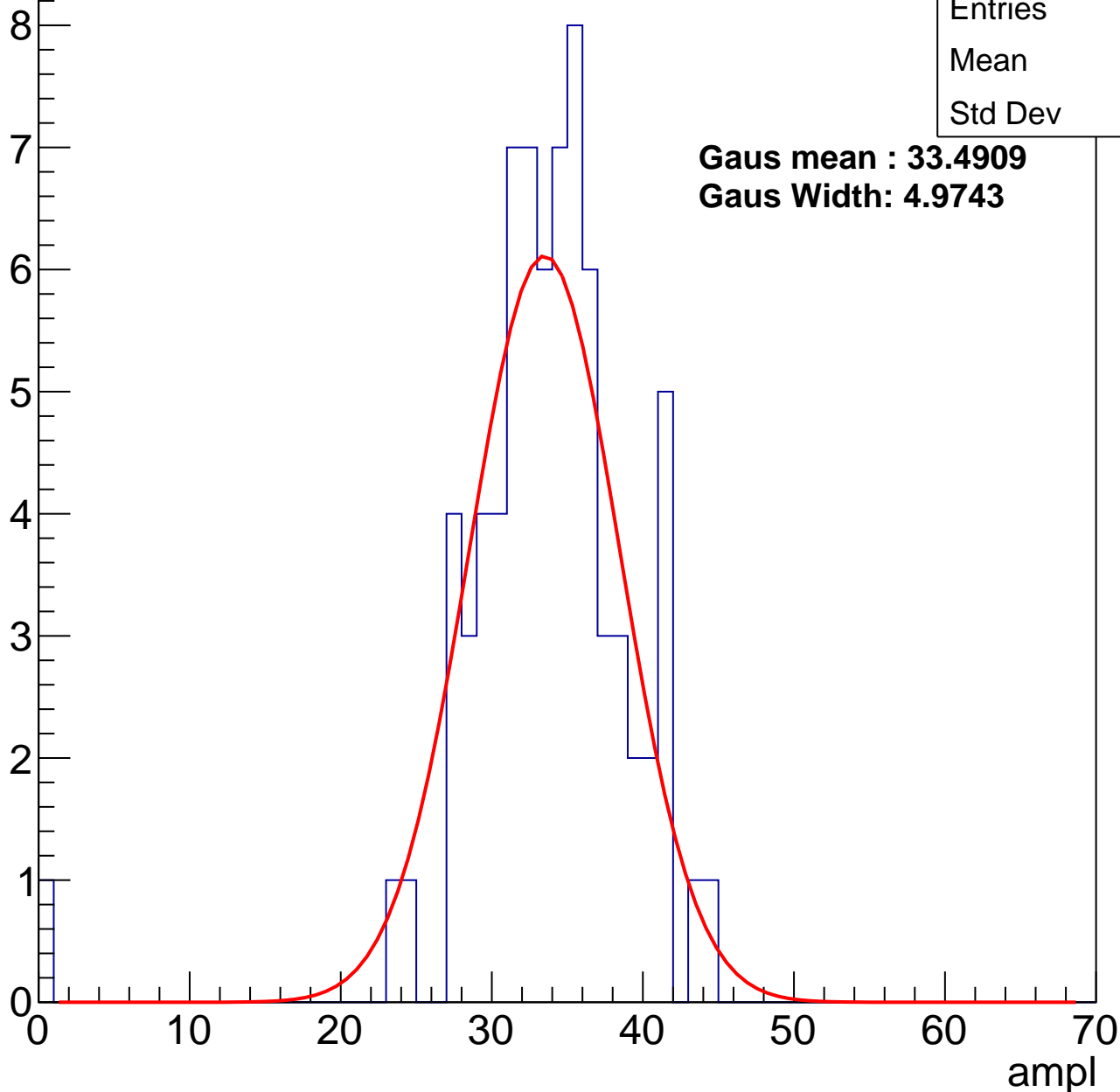
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	33.2
Std Dev	5.79

**Gaus mean : 33.4909**

**Gaus Width: 4.9743**



# B1L103S, U2-ch124, adc2

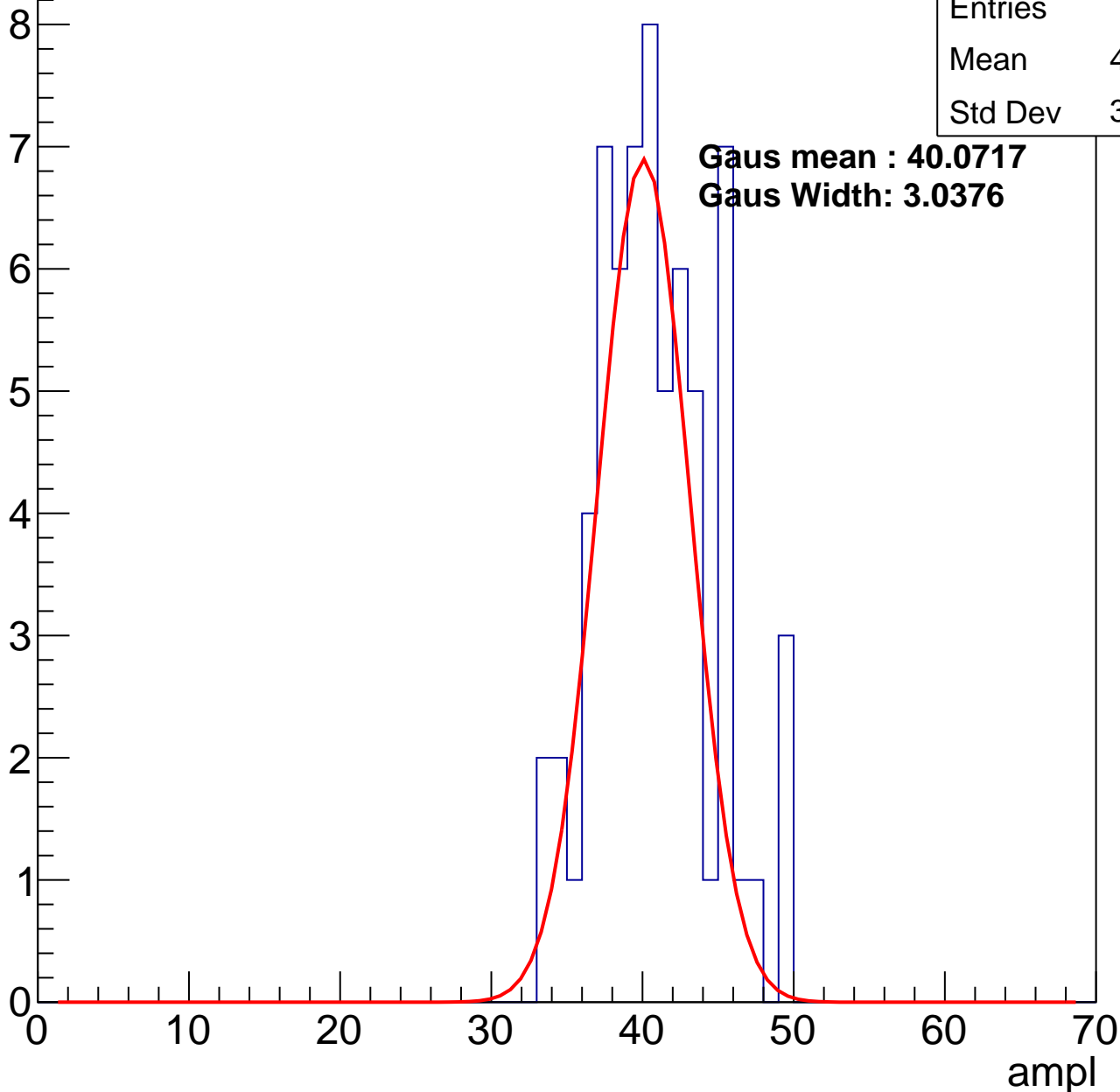
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	40.36
Std Dev	3.768

**Gaus mean : 40.0717**

**Gaus Width: 3.0376**

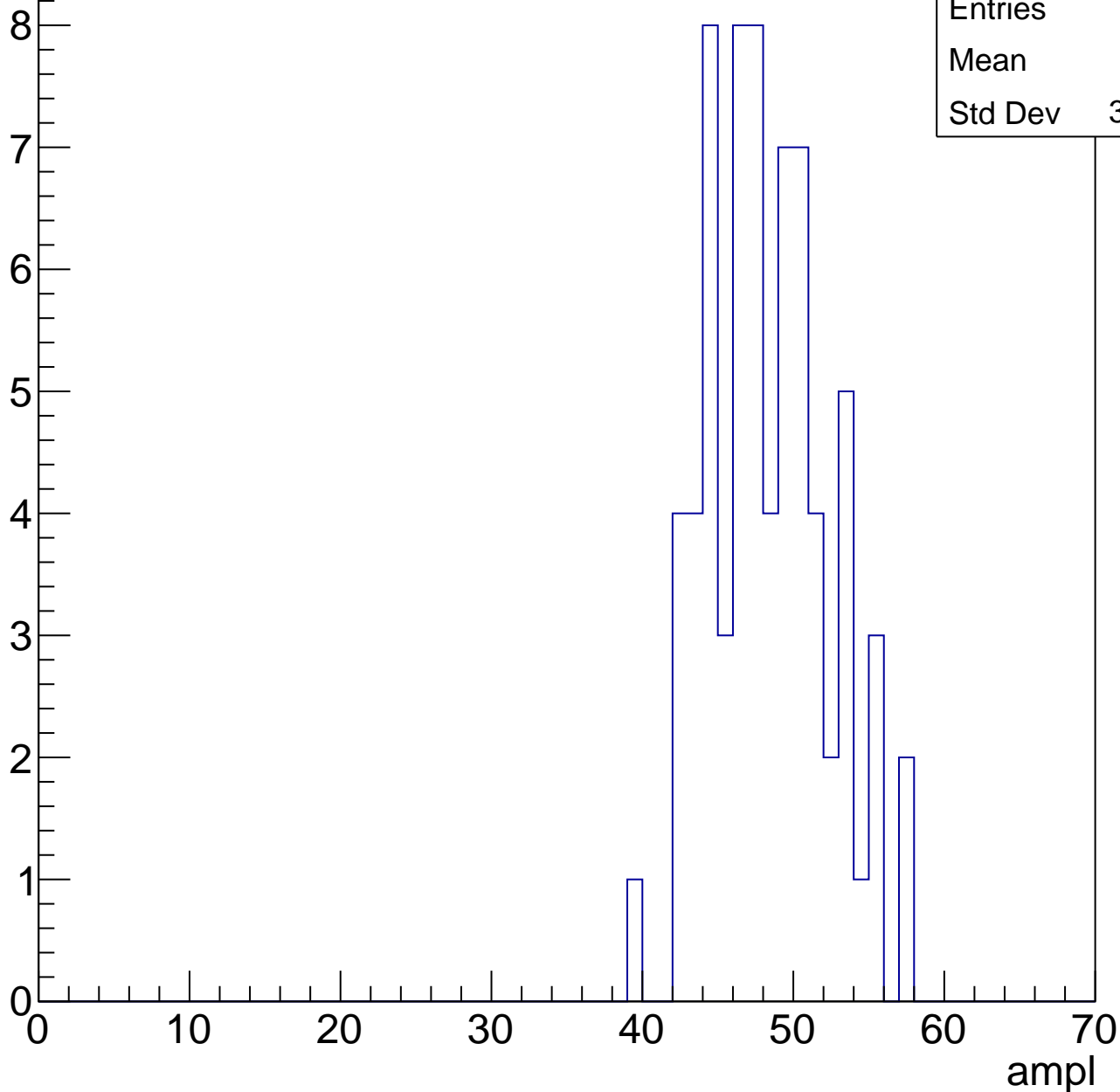


# B1L103S, U2-ch124, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	47.9
Std Dev	3.922

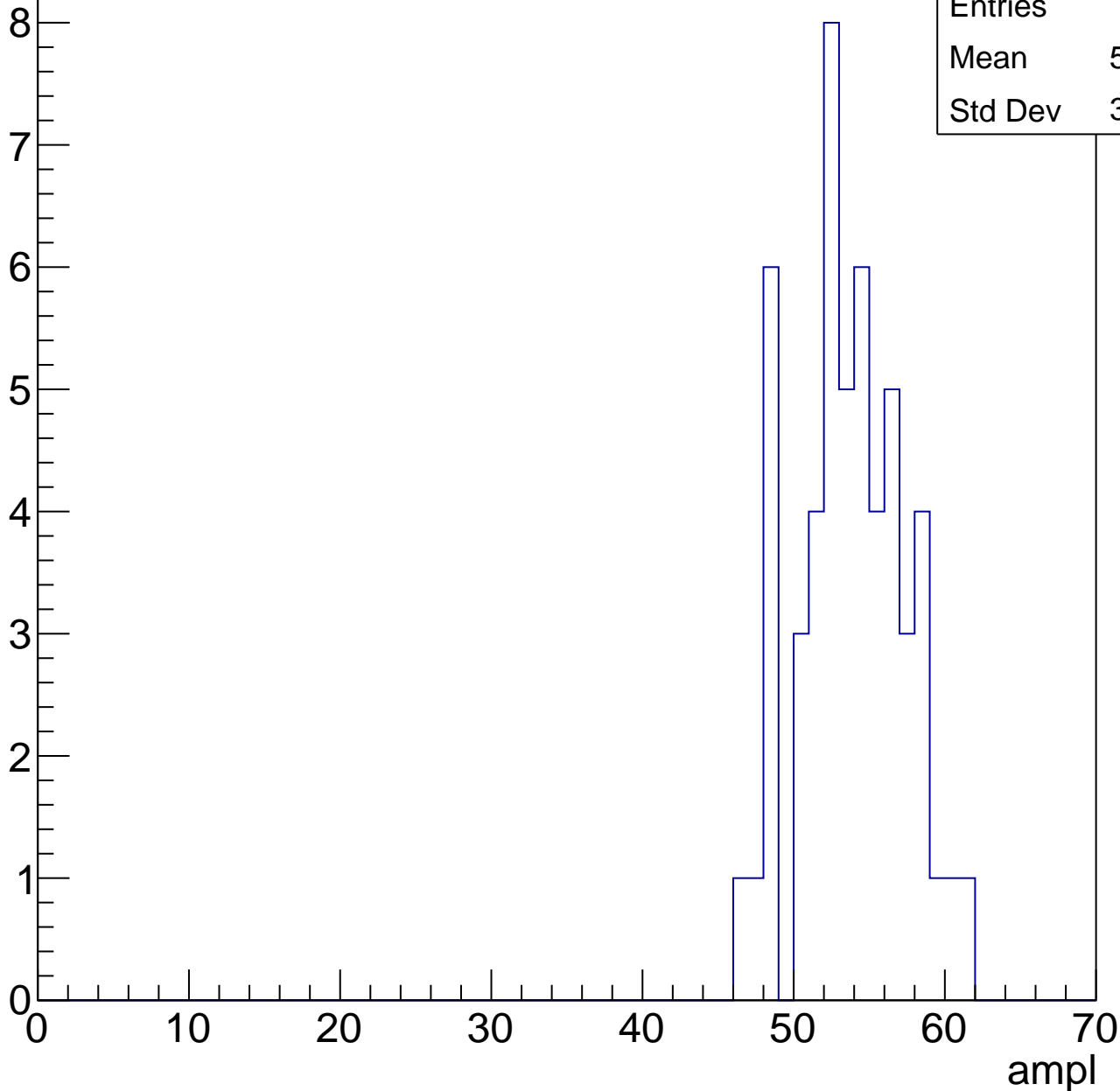


# B1L103S, U2-ch124, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

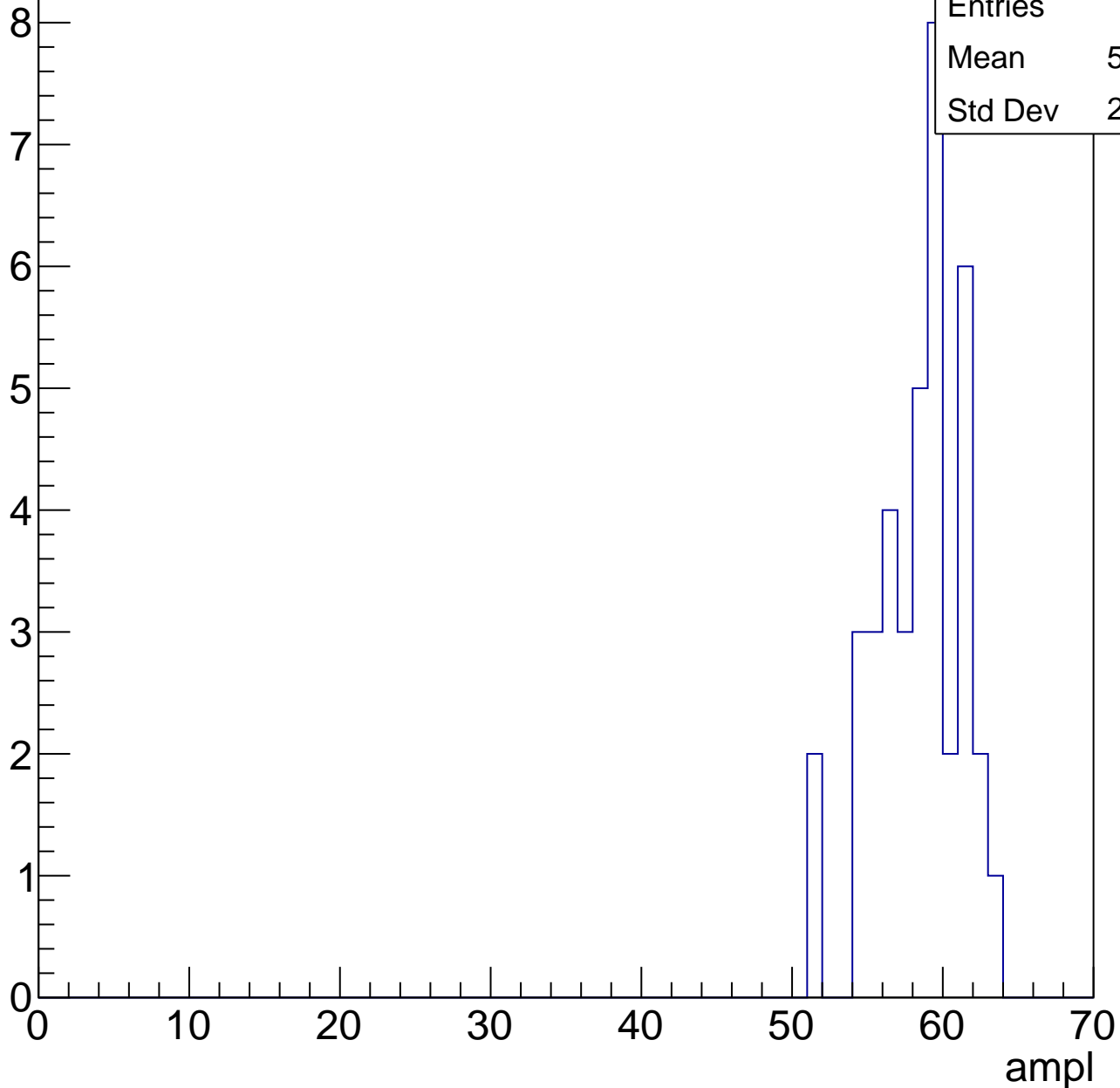
Entries	53
Mean	53.26
Std Dev	3.492



# B1L103S, U2-ch124, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

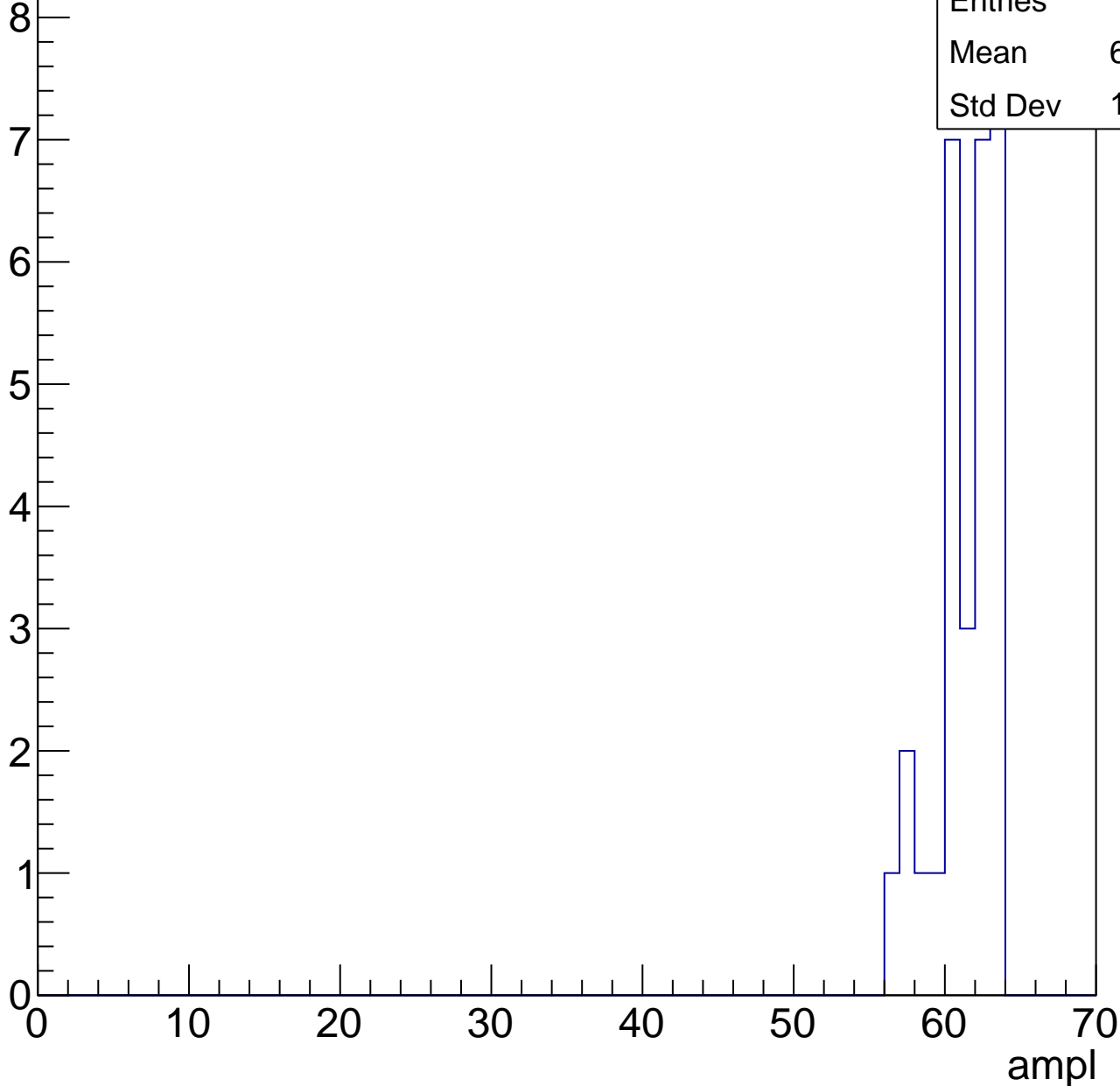


# B1L103S, U2-ch124, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	30
Mean	60.93
Std Dev	1.965





# B1L103S, U2-ch124, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	4
Mean	31.25
Std Dev	31.25

# B1L103S, U2-ch125, adc0

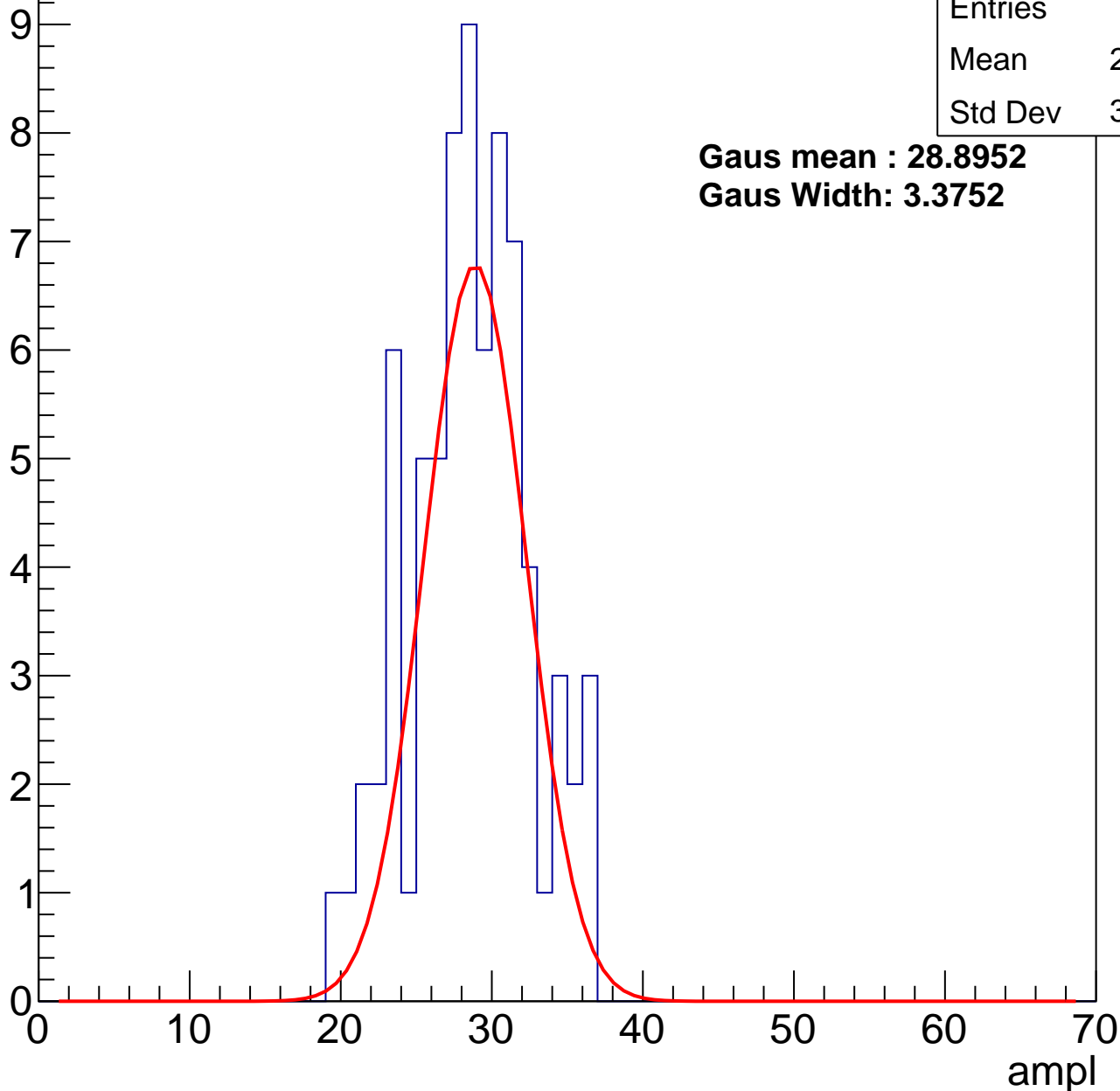
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	28.14
Std Dev	3.926

**Gaus mean : 28.8952**

**Gaus Width: 3.3752**



# B1L103S, U2-ch125, adc1

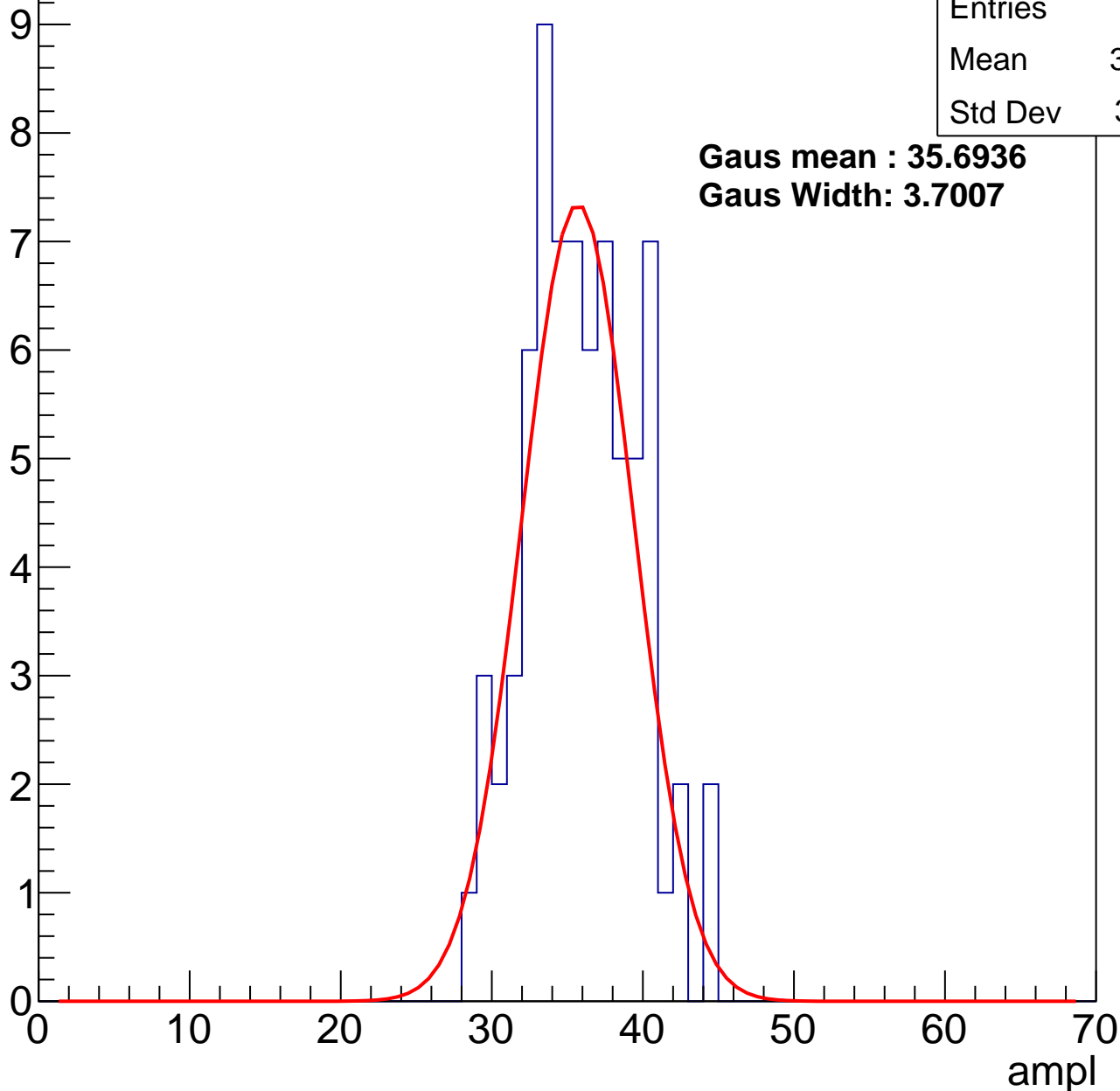
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	35.52
Std Dev	3.631

**Gaus mean : 35.6936**

**Gaus Width: 3.7007**



# B1L103S, U2-ch125, adc2

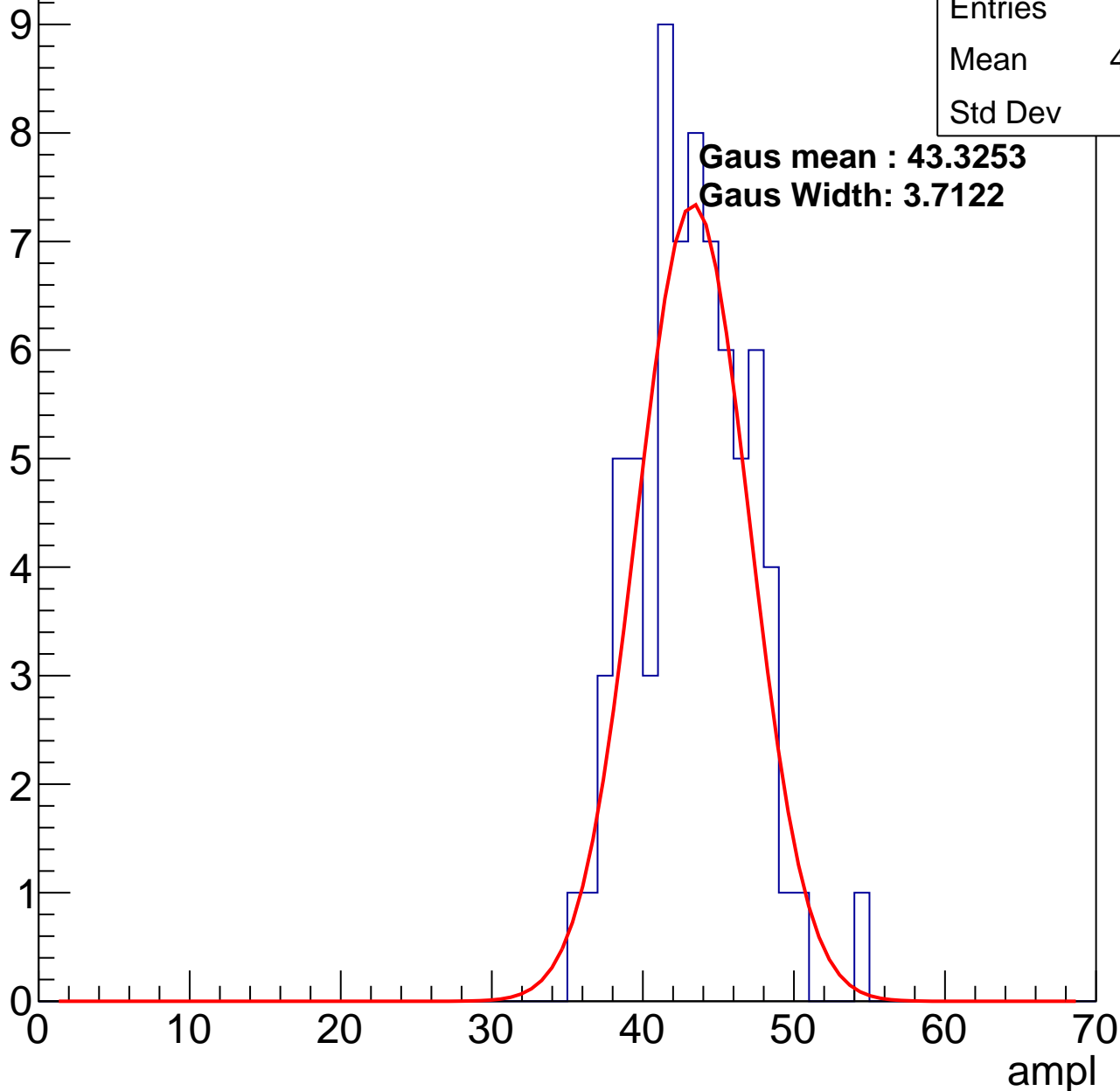
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	42.86
Std Dev	3.65

**Gaus mean : 43.3253**

**Gaus Width: 3.7122**

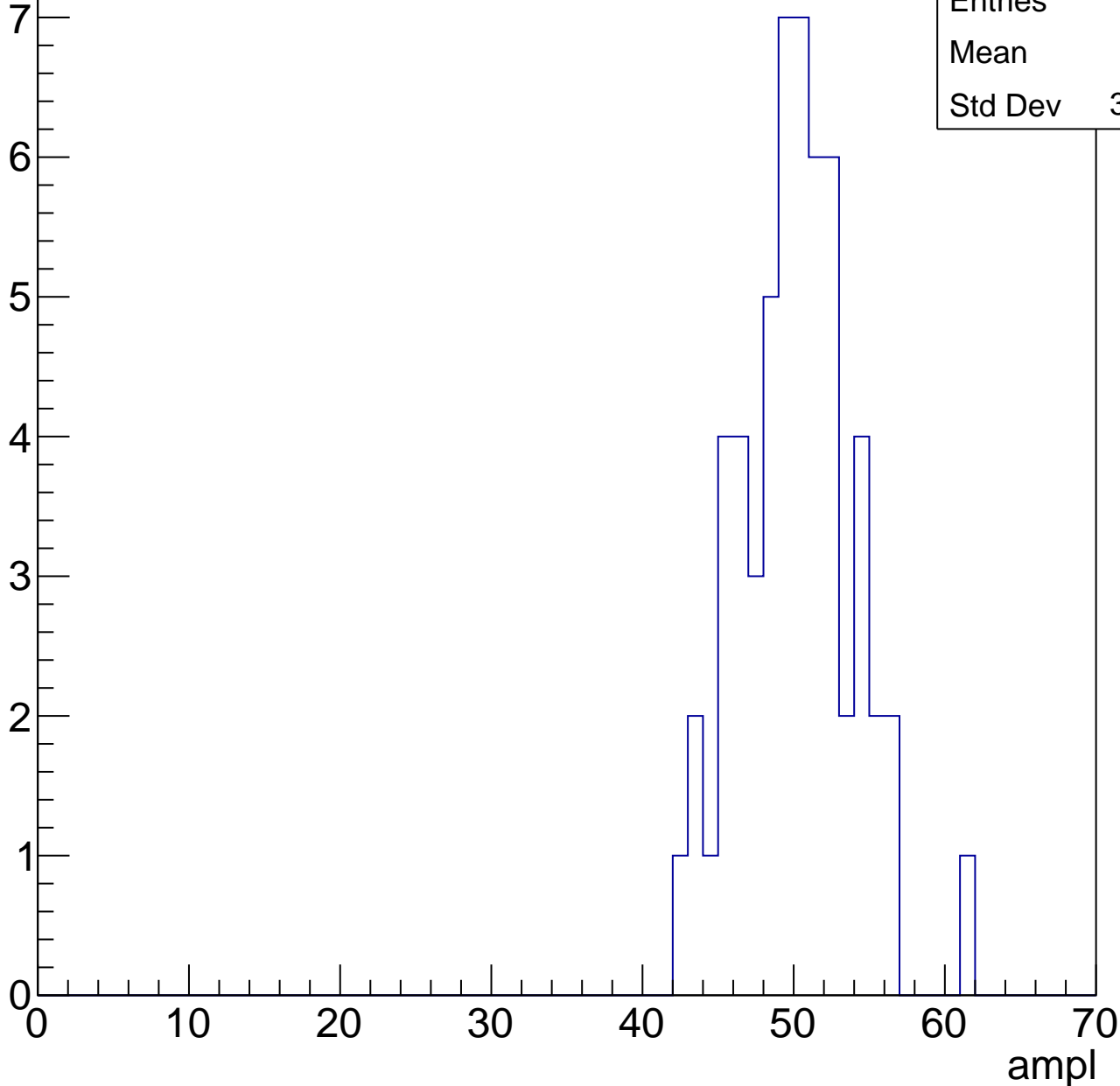


# B1L103S, U2-ch125, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	49.7
Std Dev	3.666

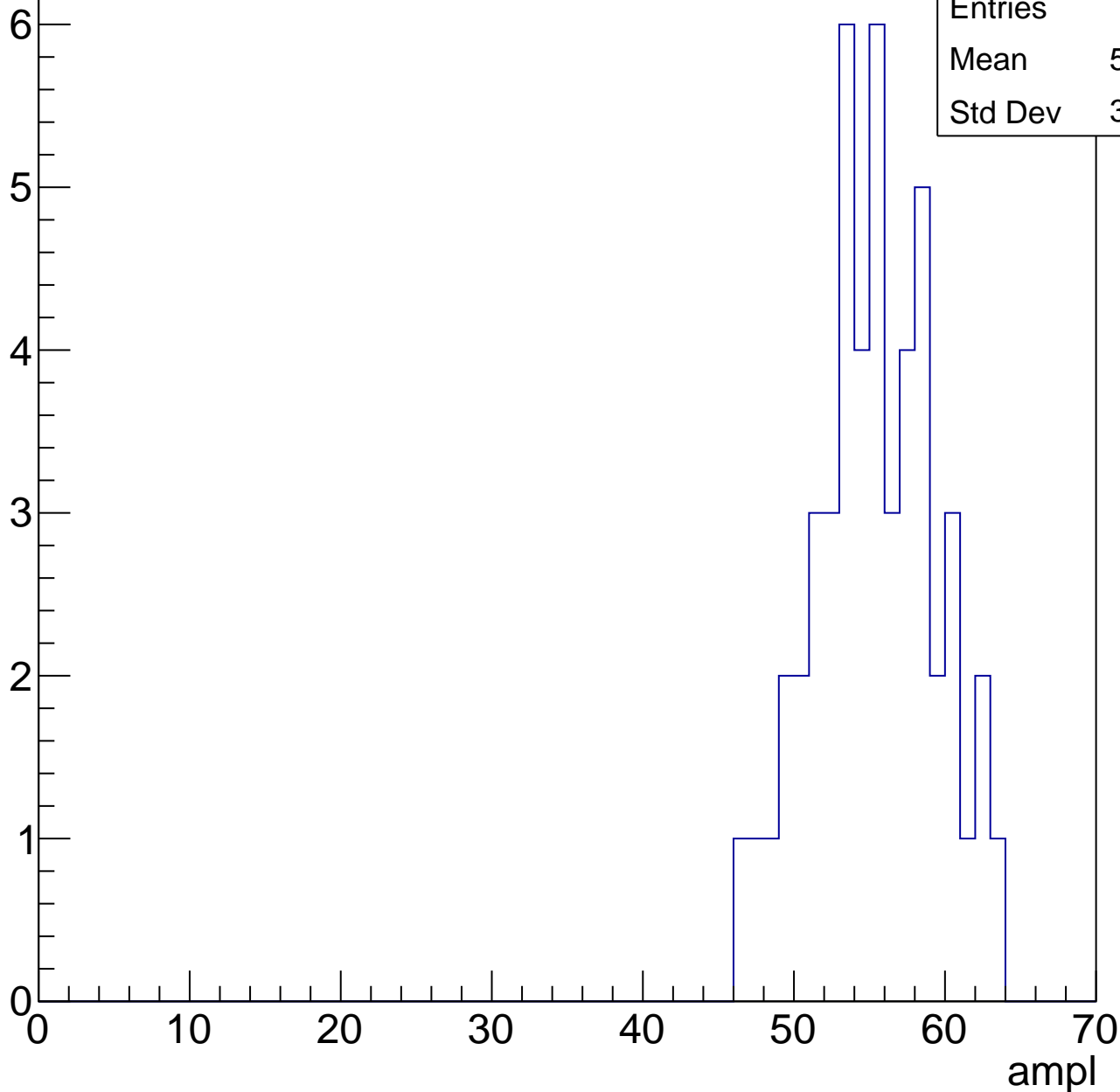


# B1L103S, U2-ch125, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

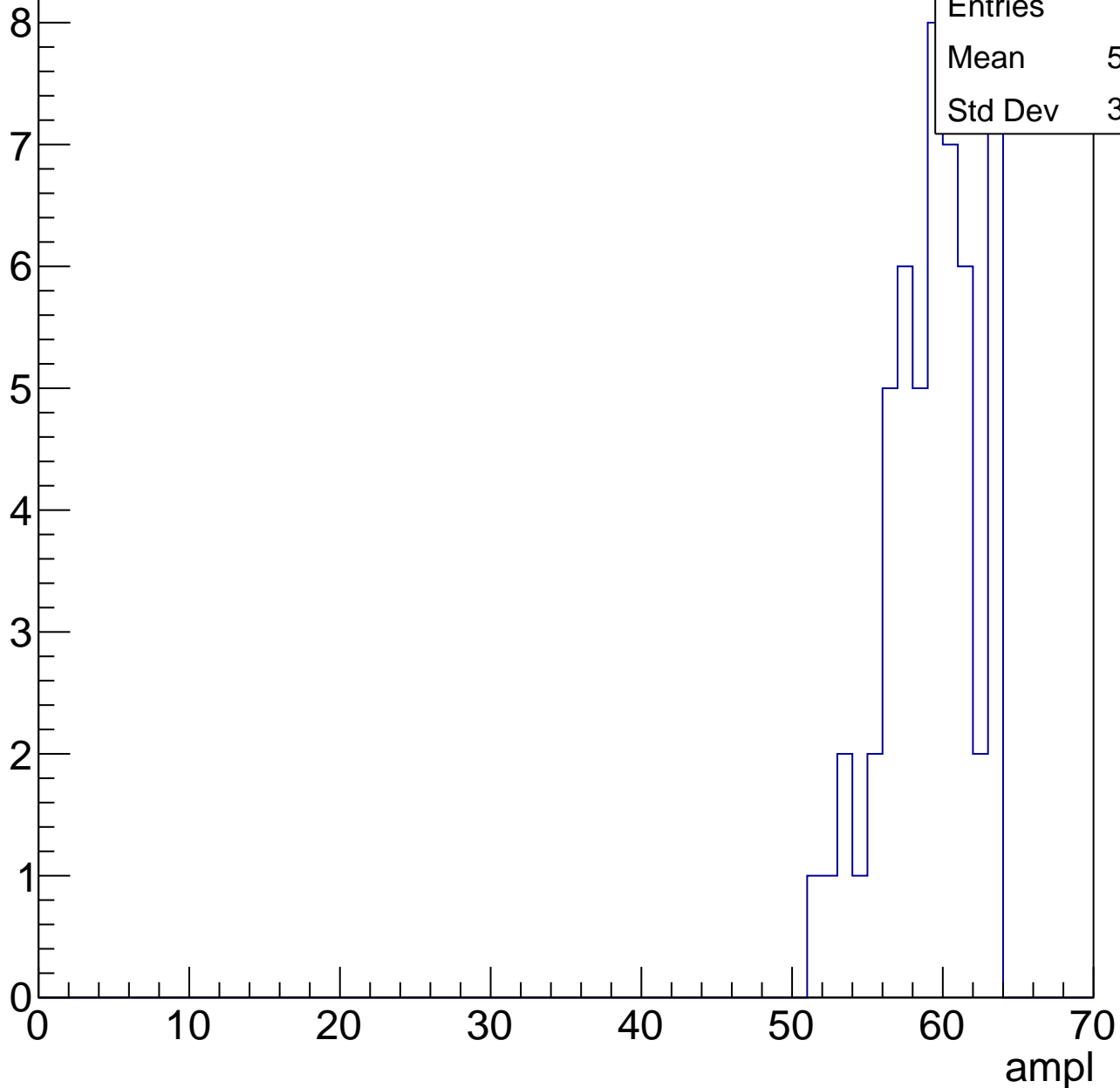
Entries	50
Mean	54.88
Std Dev	3.968



# B1L103S, U2-ch125, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



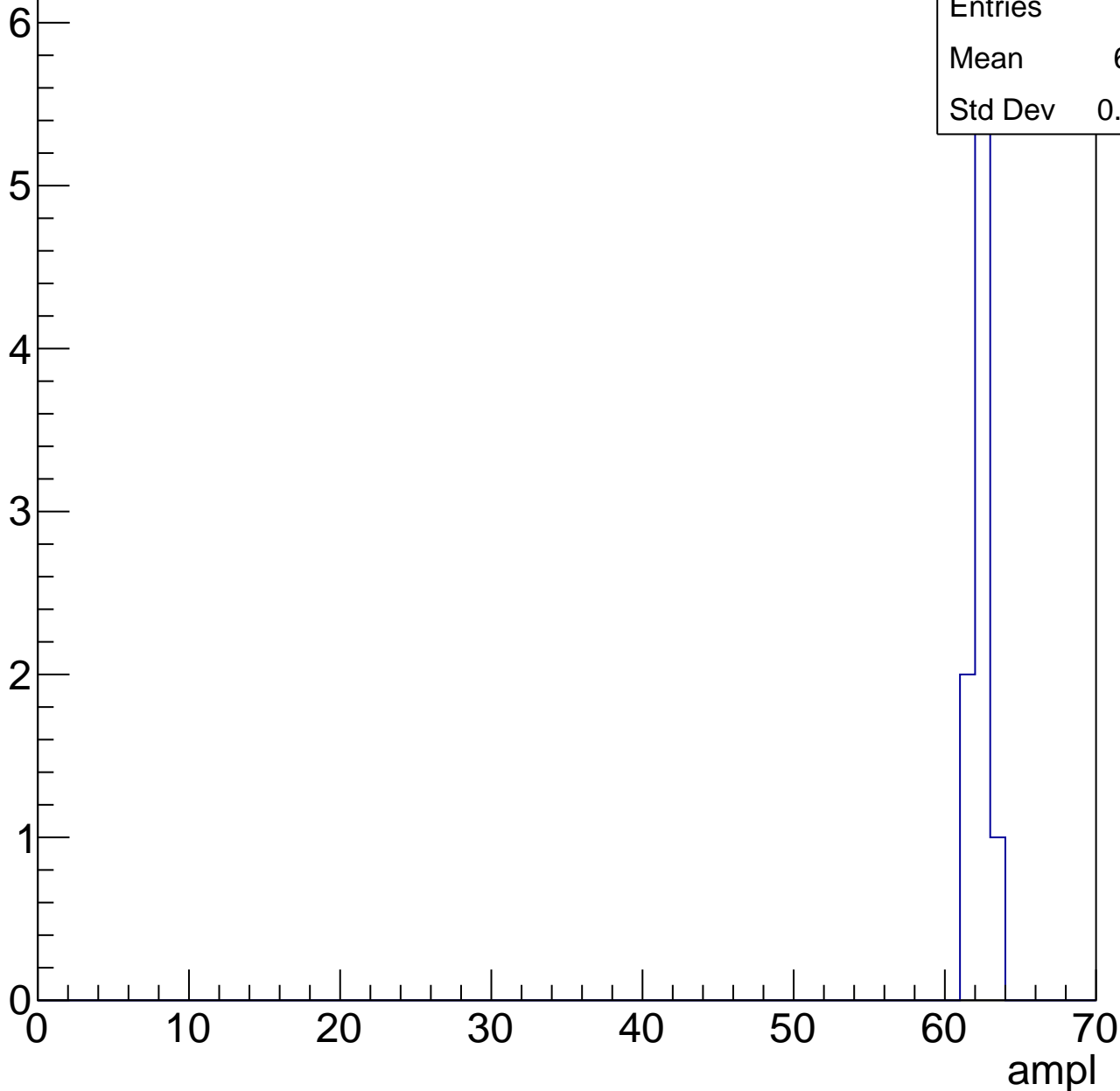
Entries	54
Mean	58.72
Std Dev	3.009

# B1L103S, U2-ch125, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	9
Mean	61.89
Std Dev	0.5666





# B1L103S, U2-ch125, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch126, adc0

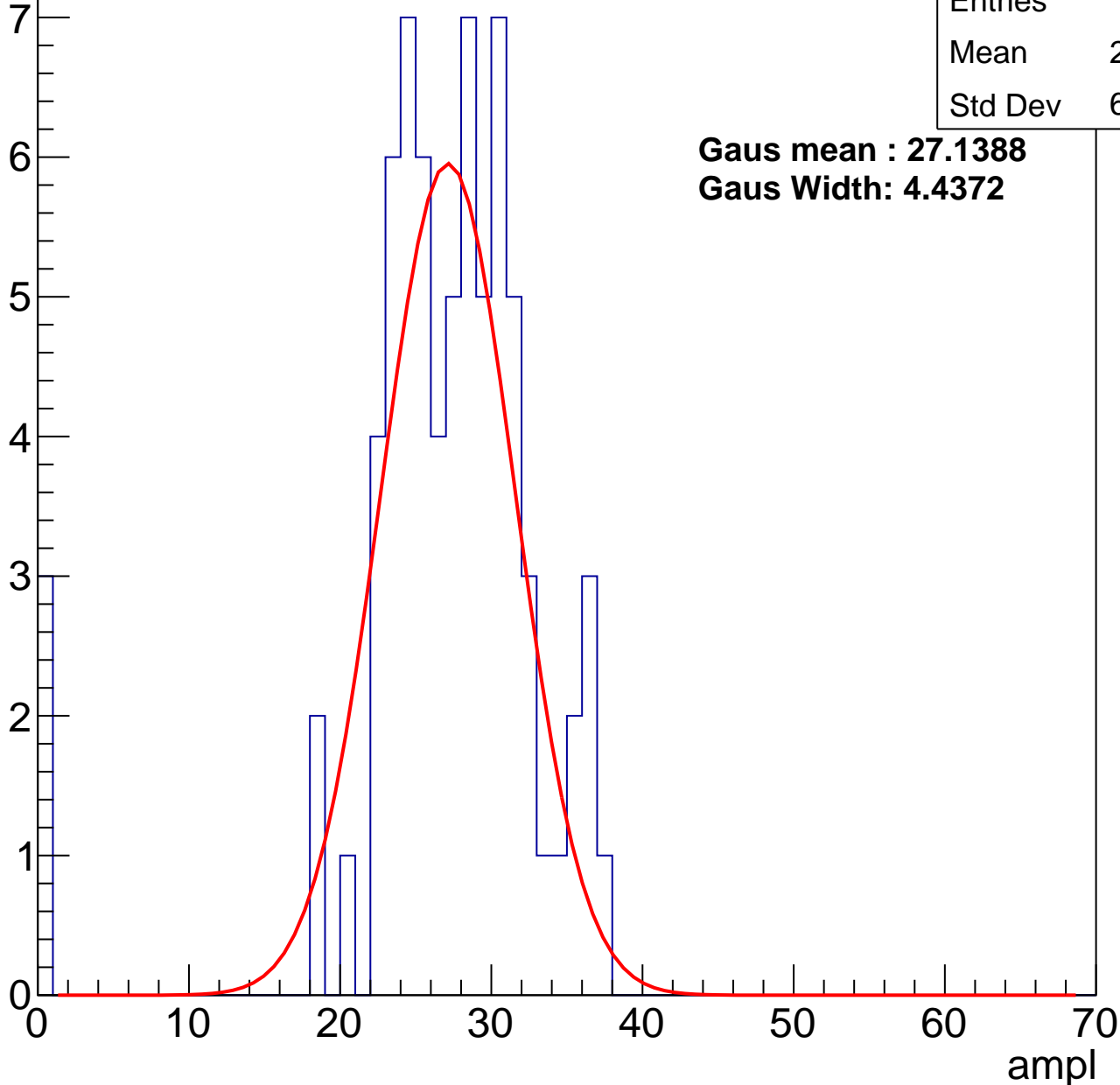
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	26.34
Std Dev	6.879

**Gaus mean : 27.1388**

**Gaus Width: 4.4372**



# B1L103S, U2-ch126, adc1

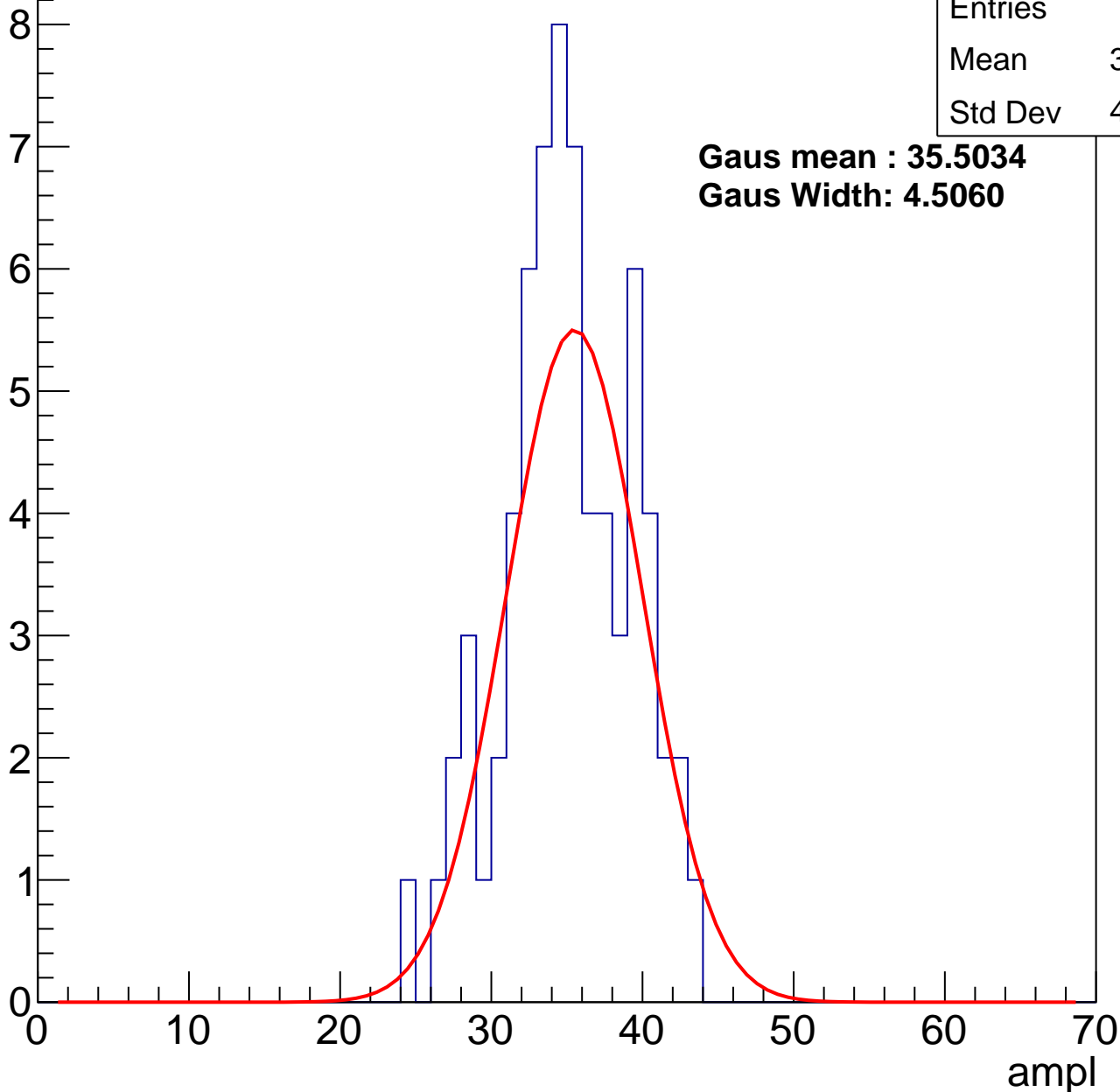
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	34.56
Std Dev	4.167

**Gaus mean : 35.5034**

**Gaus Width: 4.5060**



# B1L103S, U2-ch126, adc2

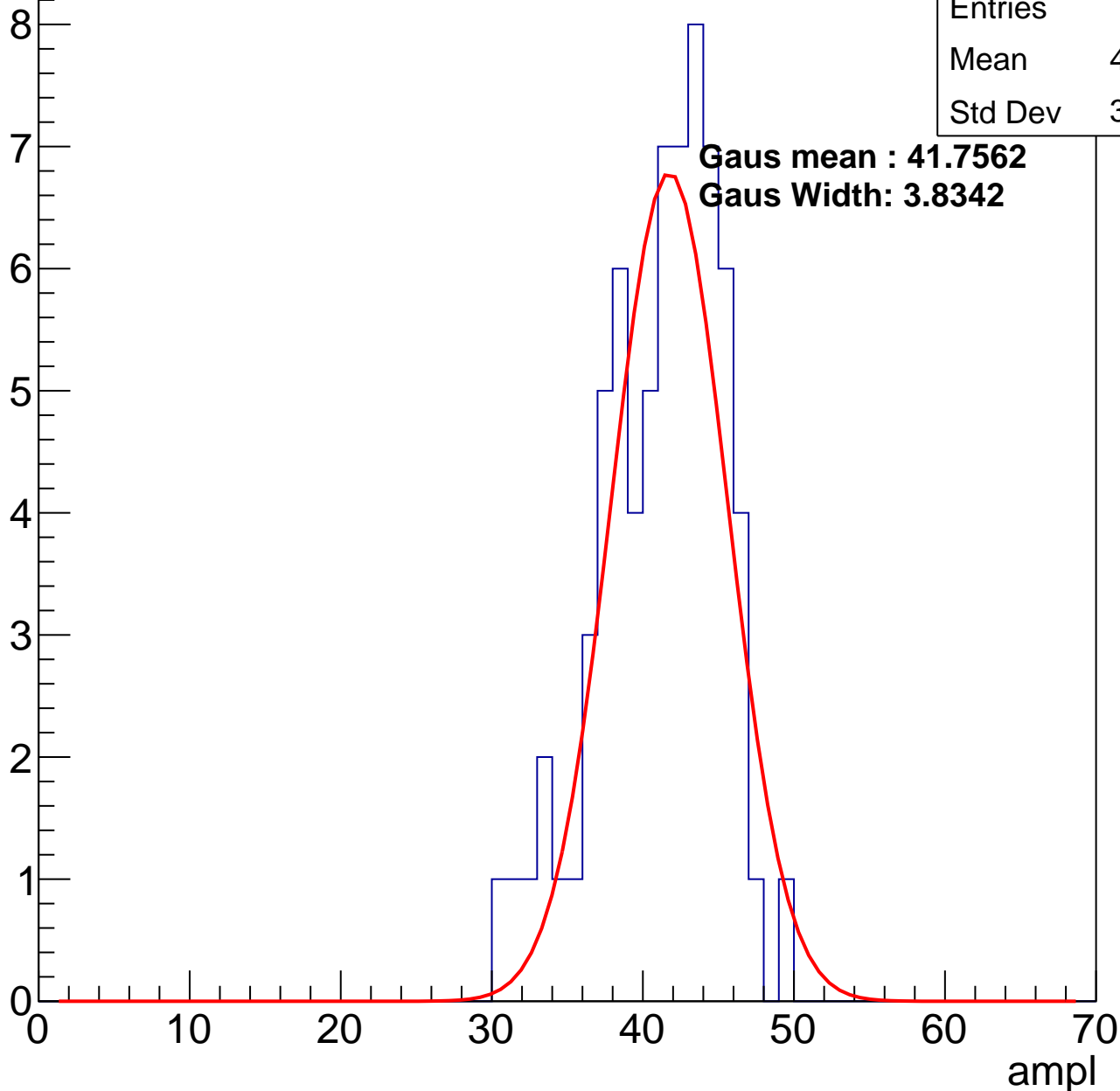
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	40.68
Std Dev	3.999

**Gaus mean : 41.7562**

**Gaus Width: 3.8342**

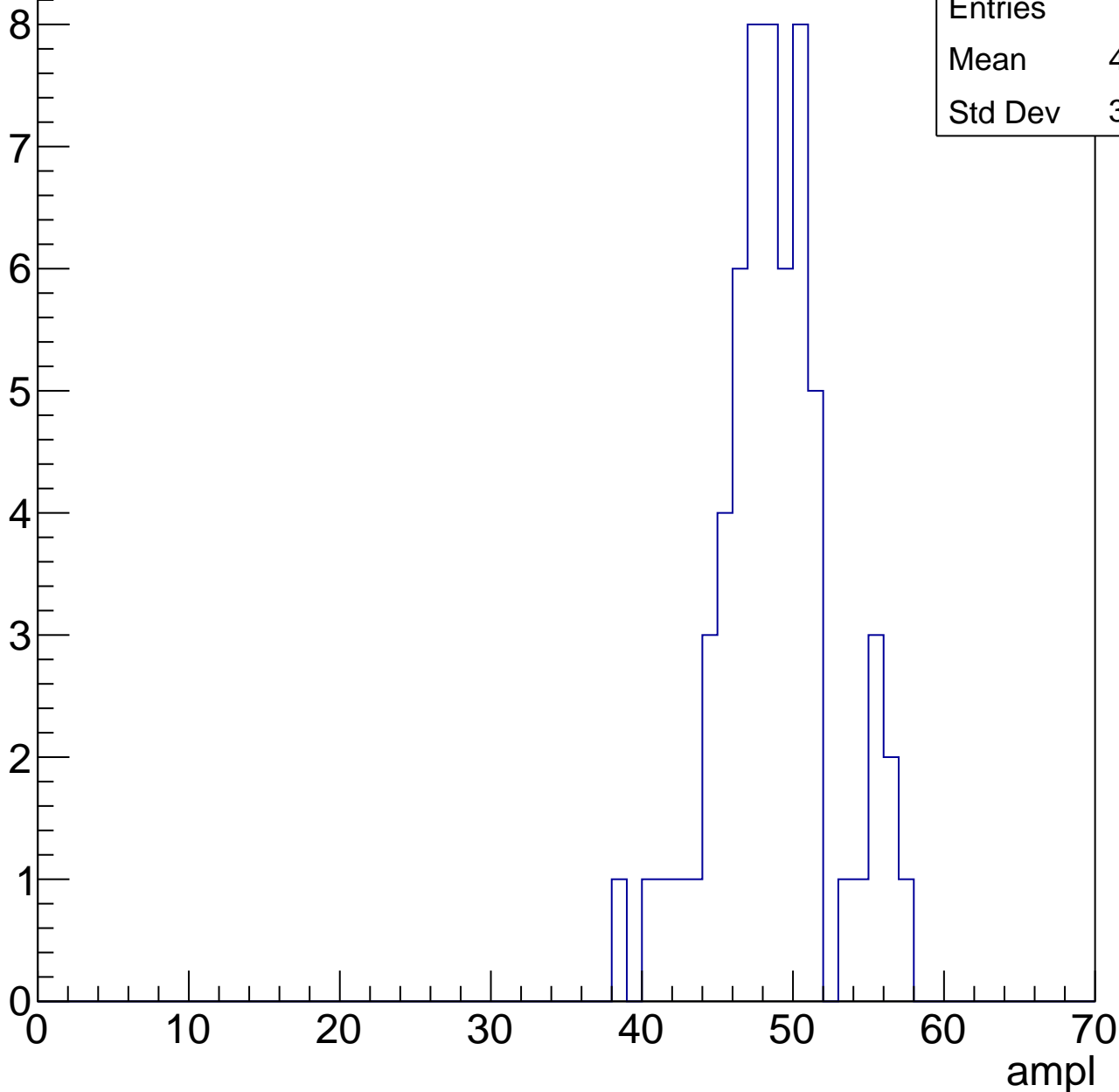


# B1L103S, U2-ch126, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	48.23
Std Dev	3.813

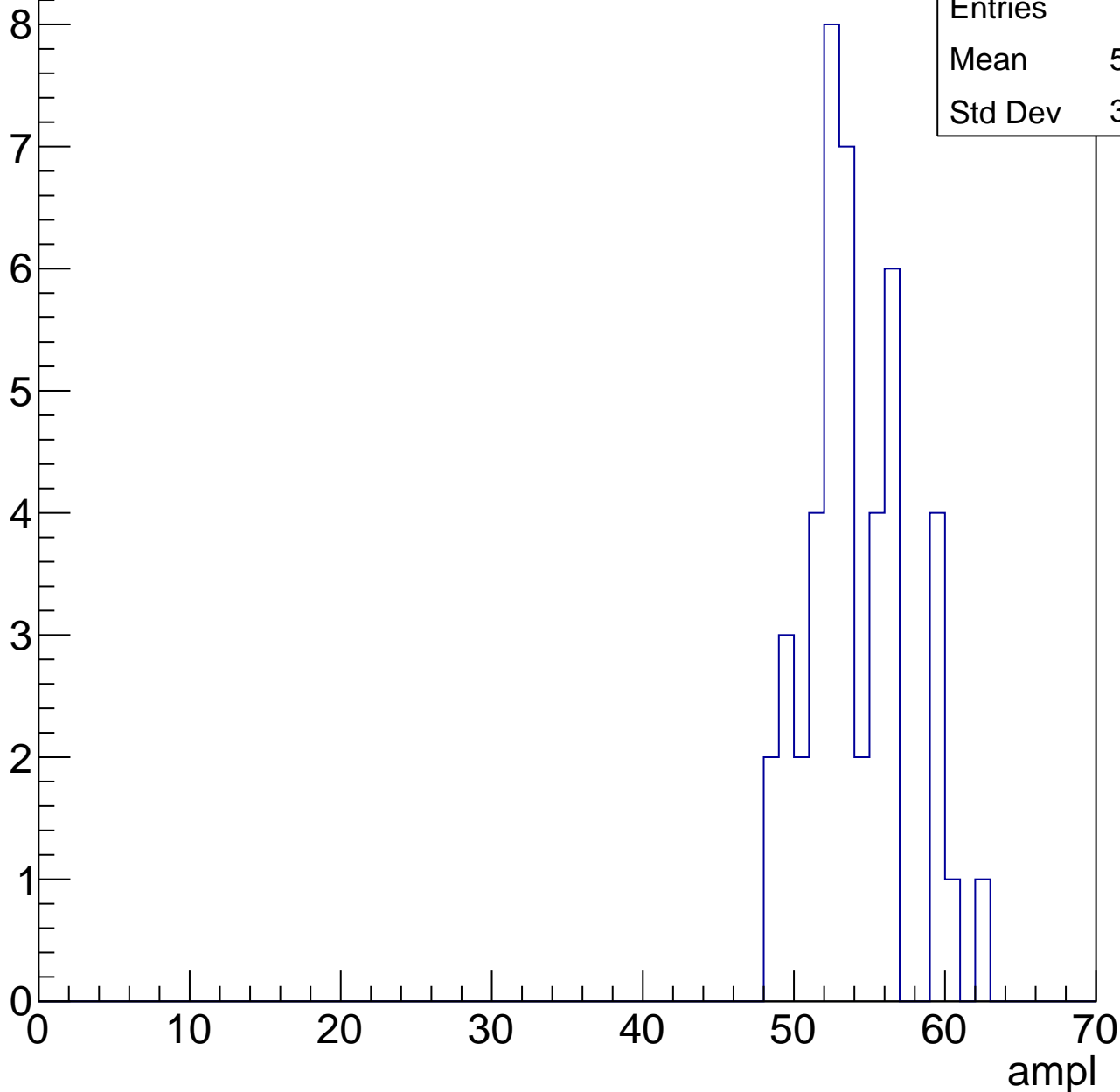


# B1L103S, U2-ch126, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	44
Mean	53.55
Std Dev	3.278

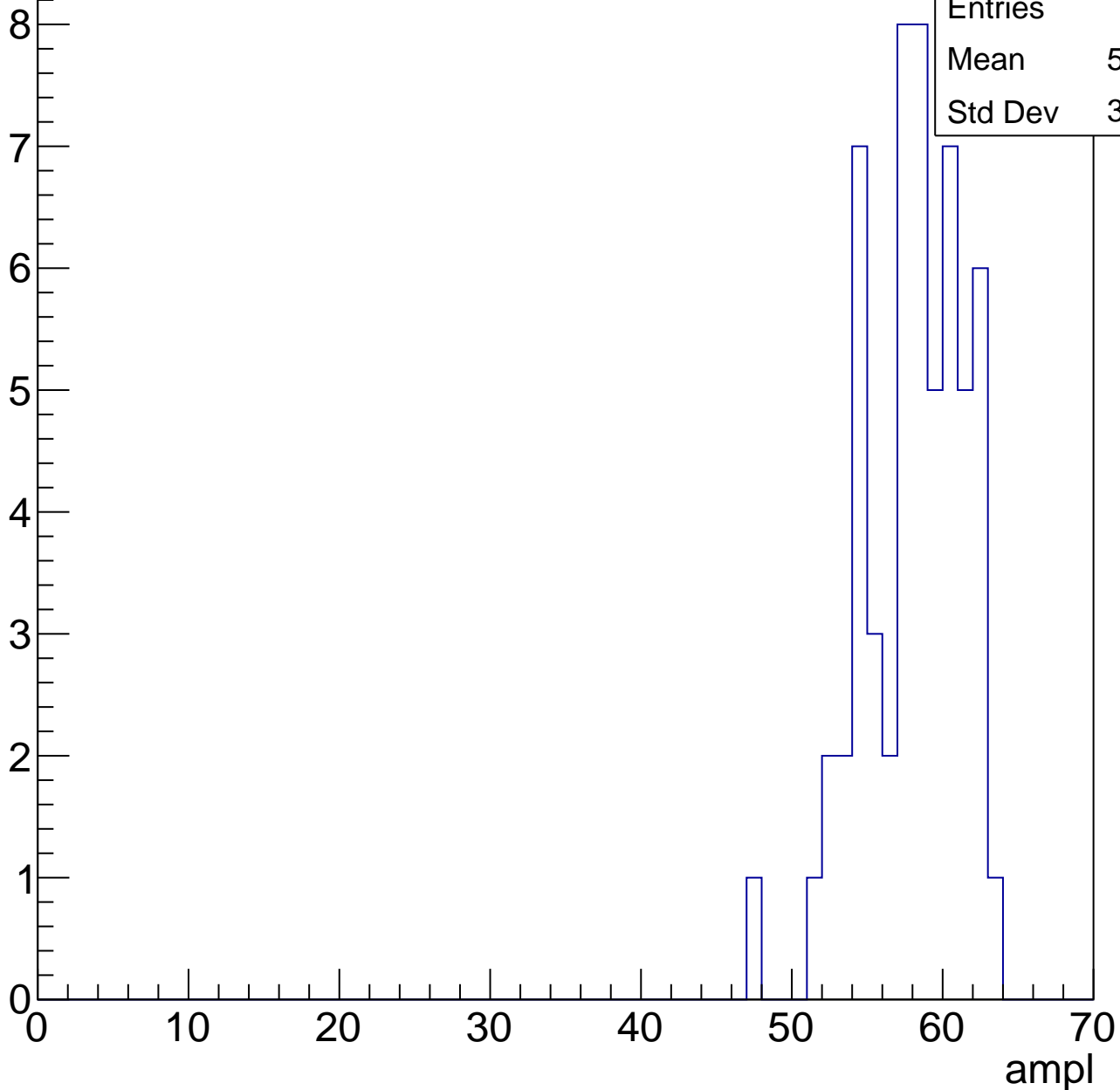


# B1L103S, U2-ch126, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	57.55
Std Dev	3.307

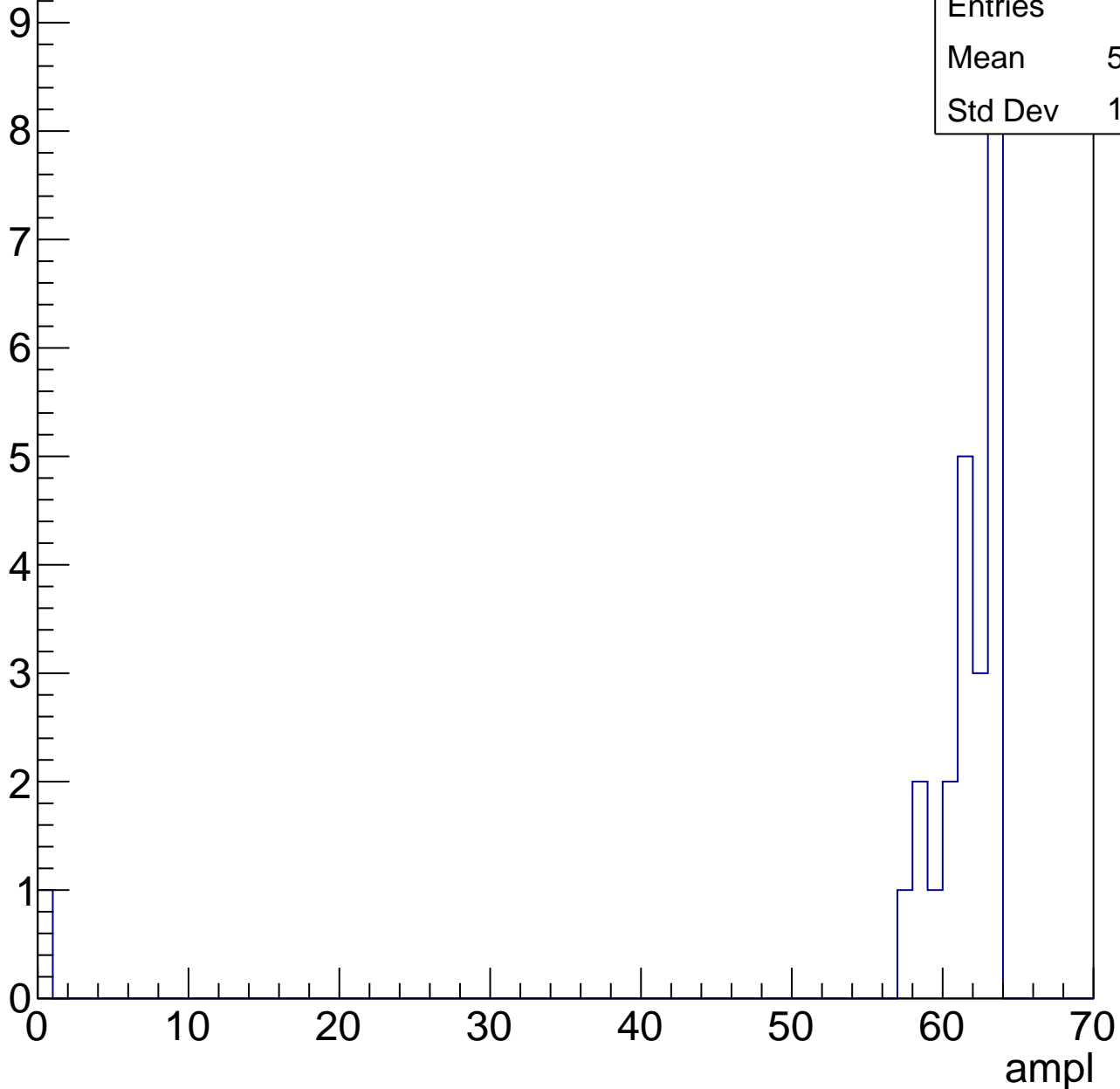


# B1L103S, U2-ch126, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	24
Mean	58.75
Std Dev	12.38





# B1L103S, U2-ch126, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U2-ch127, adc0

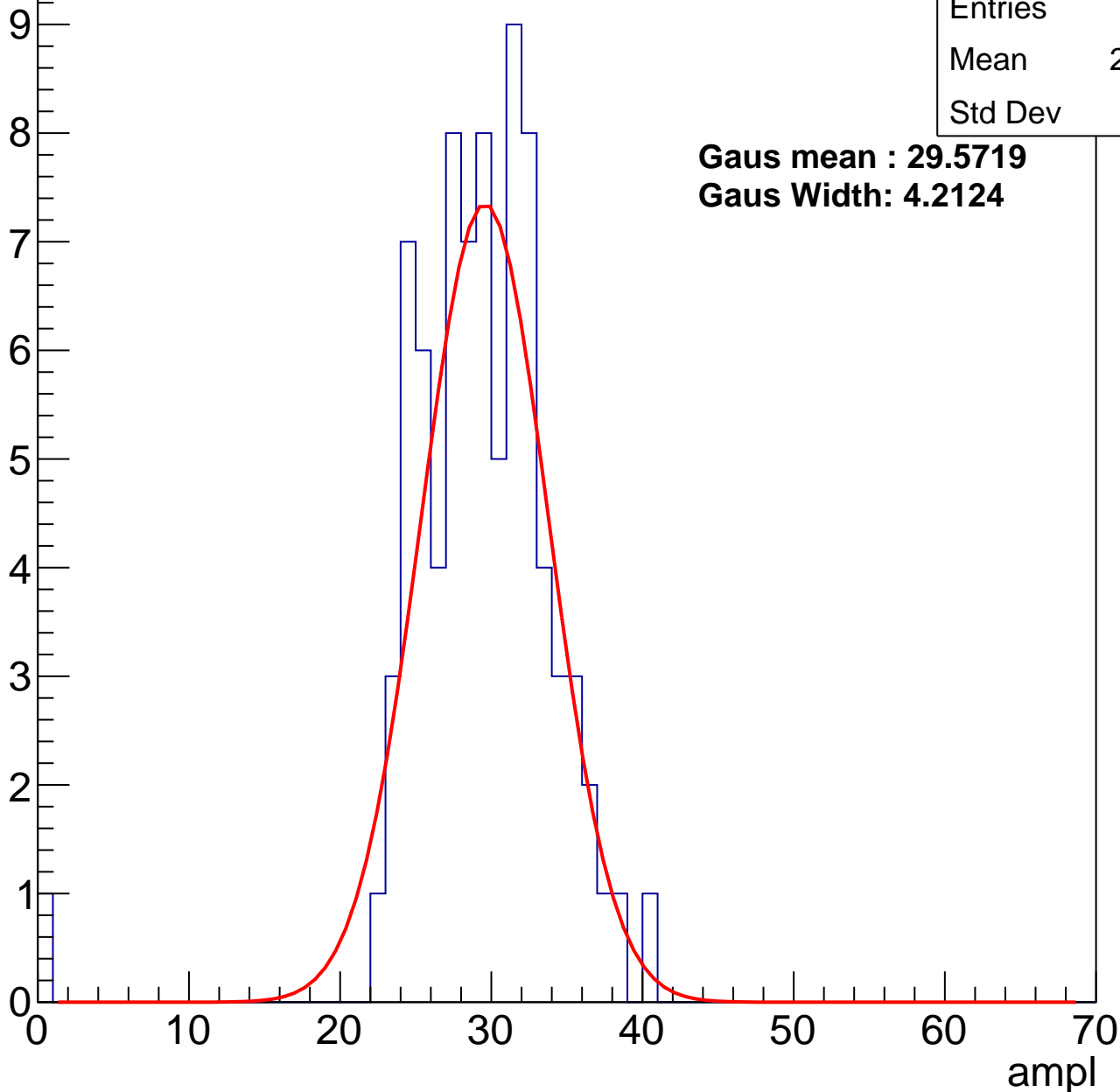
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	82
Mean	28.88
Std Dev	5.02

**Gaus mean : 29.5719**

**Gaus Width: 4.2124**



# B1L103S, U2-ch127, adc1

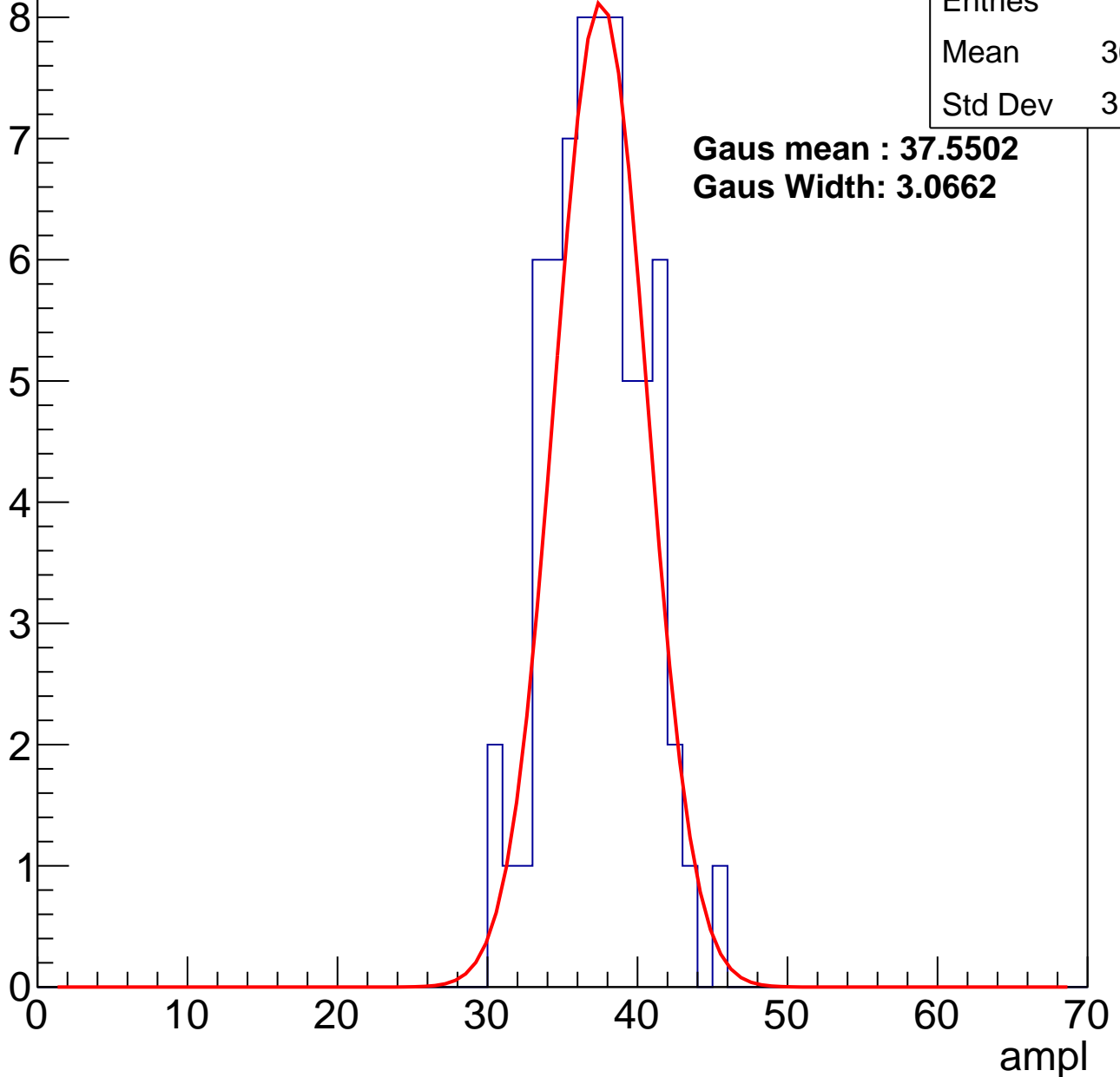
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	36.88
Std Dev	3.146

**Gaus mean : 37.5502**

**Gaus Width: 3.0662**



# B1L103S, U2-ch127, adc2

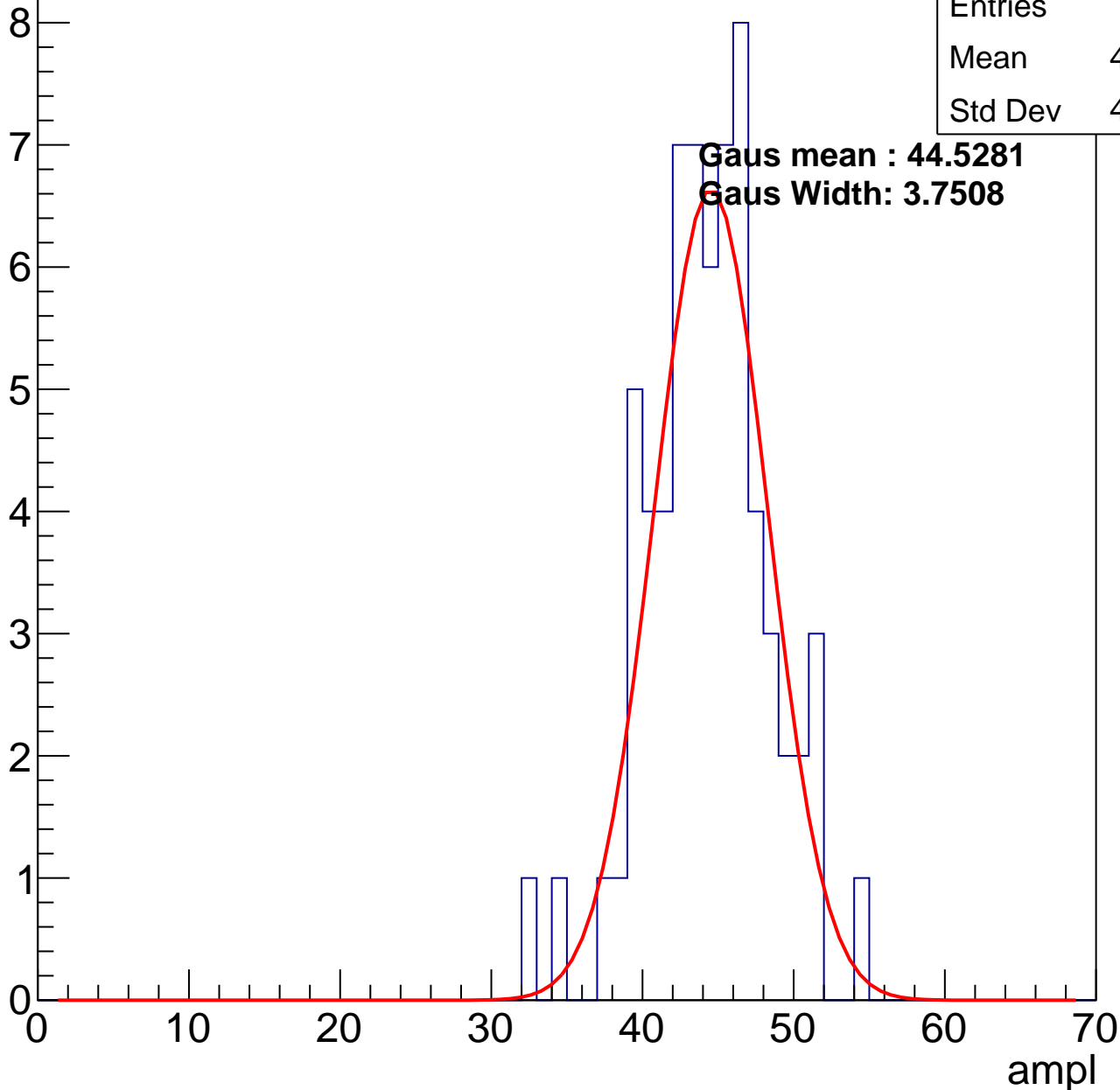
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	43.87
Std Dev	4.015

**Gaus mean : 44.5281**

**Gaus Width: 3.7508**

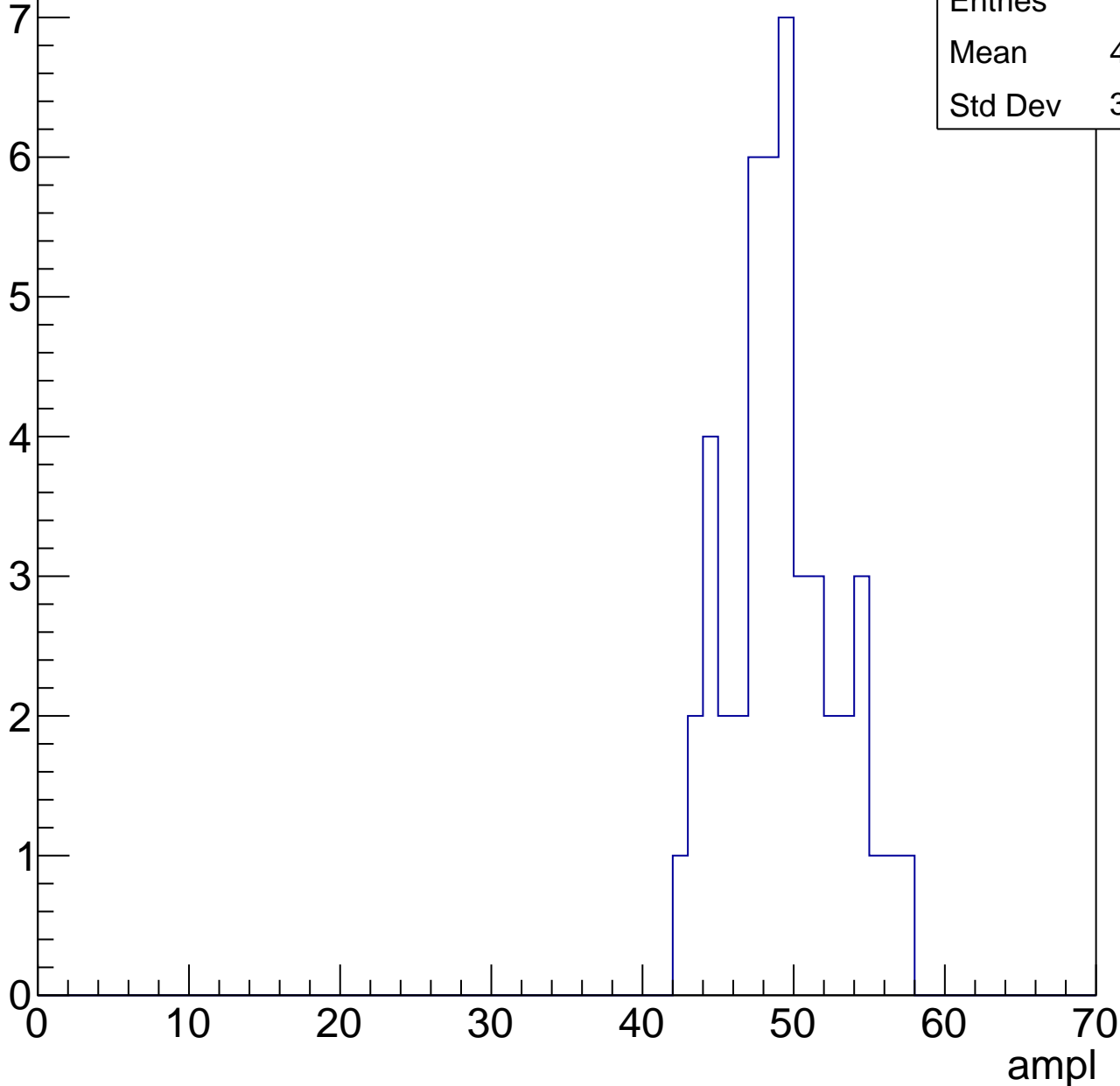


# B1L103S, U2-ch127, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	46
Mean	48.74
Std Dev	3.572

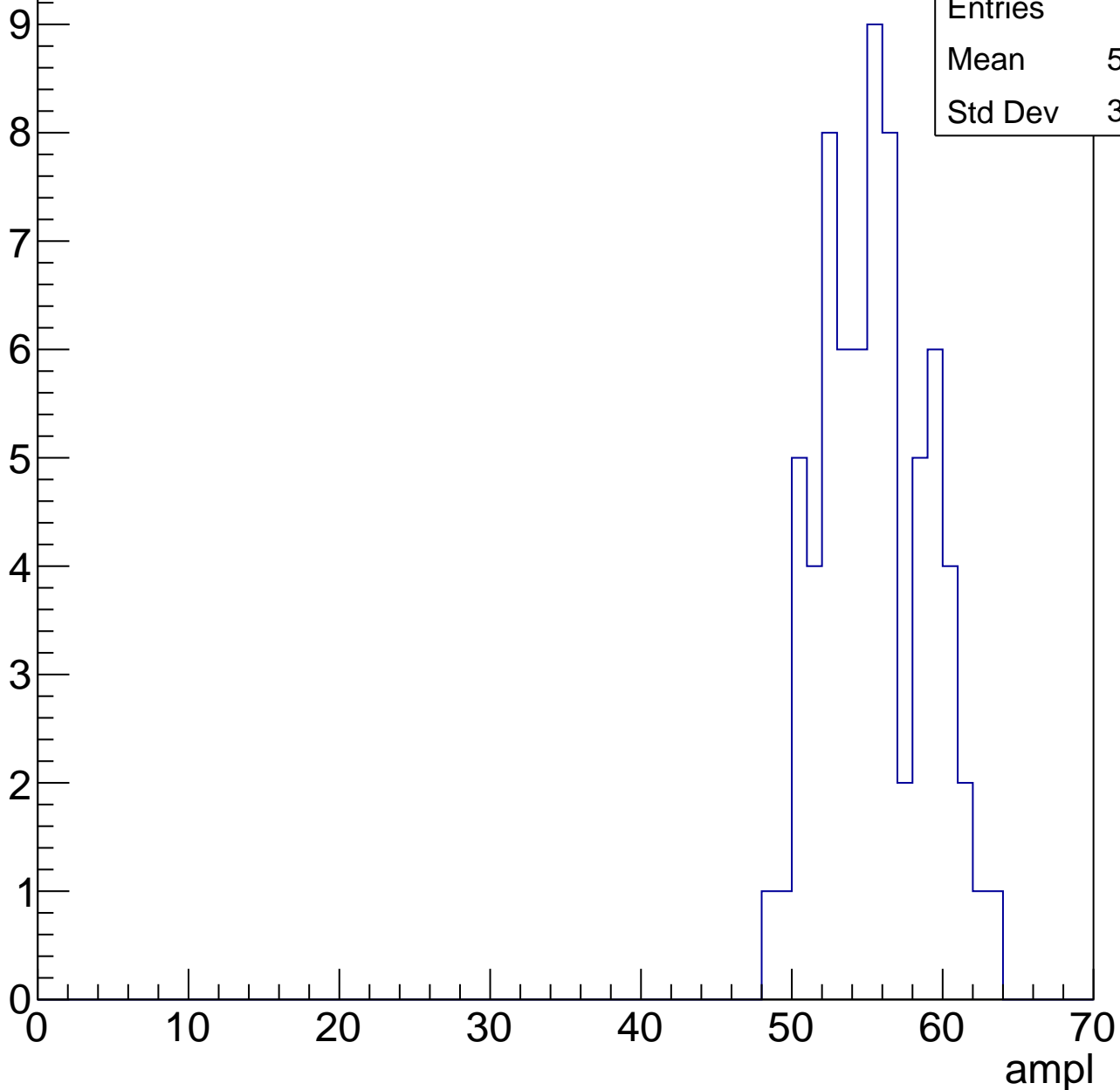


# B1L103S, U2-ch127, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	55.03
Std Dev	3.443

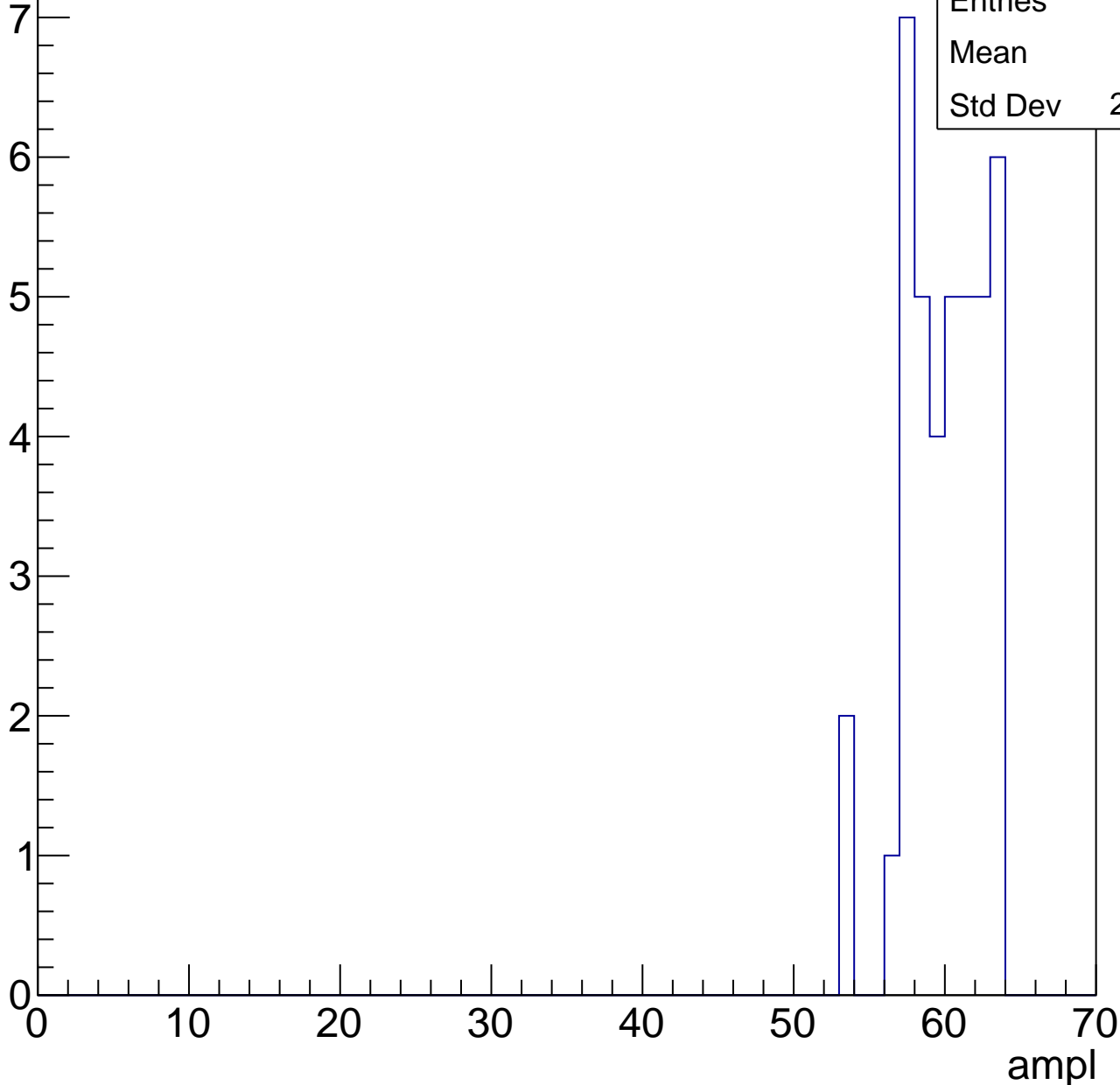


# B1L103S, U2-ch127, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

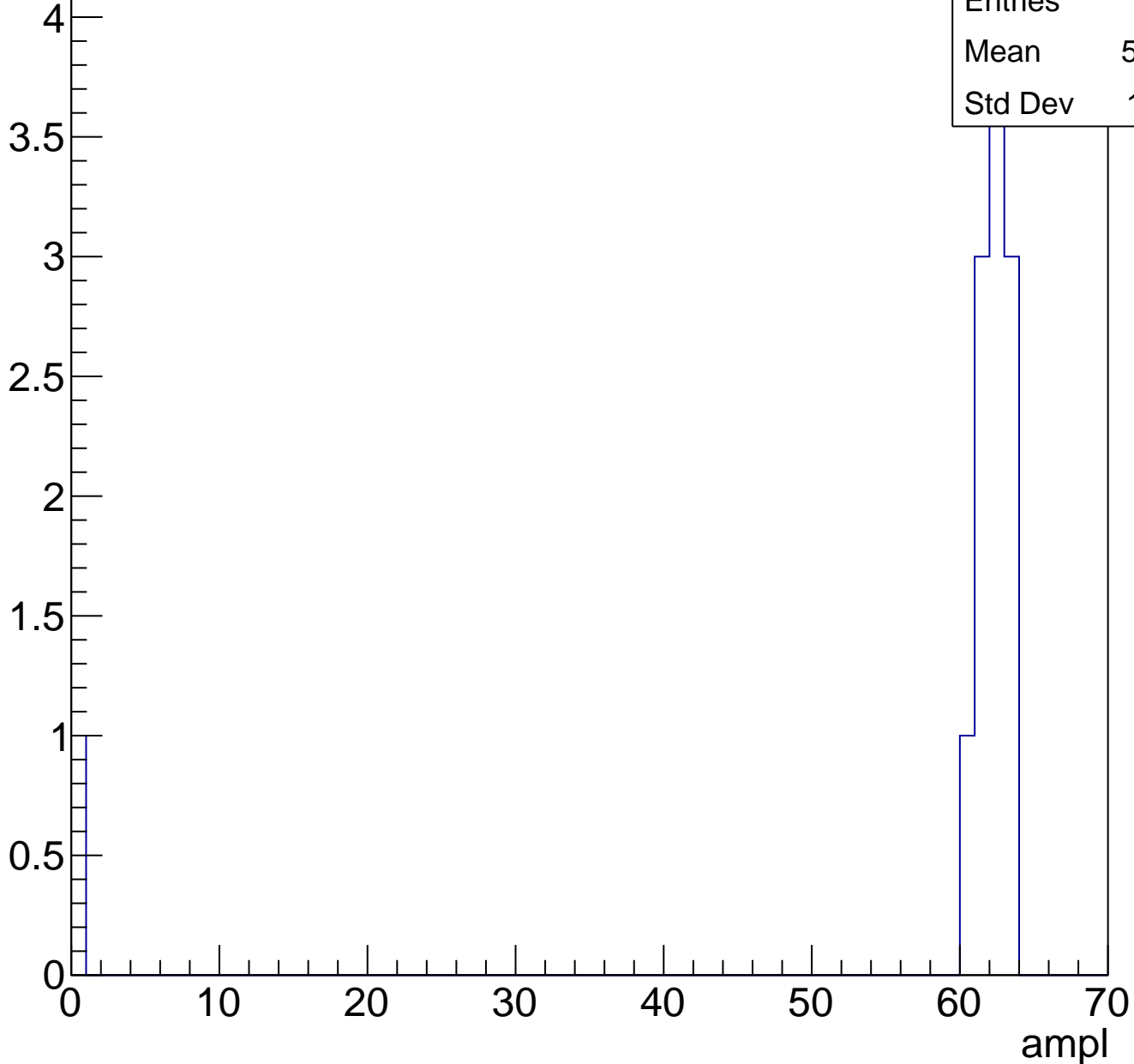
Entries	40
Mean	59.5
Std Dev	2.598



# B1L103S, U2-ch127, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U2-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U2-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

