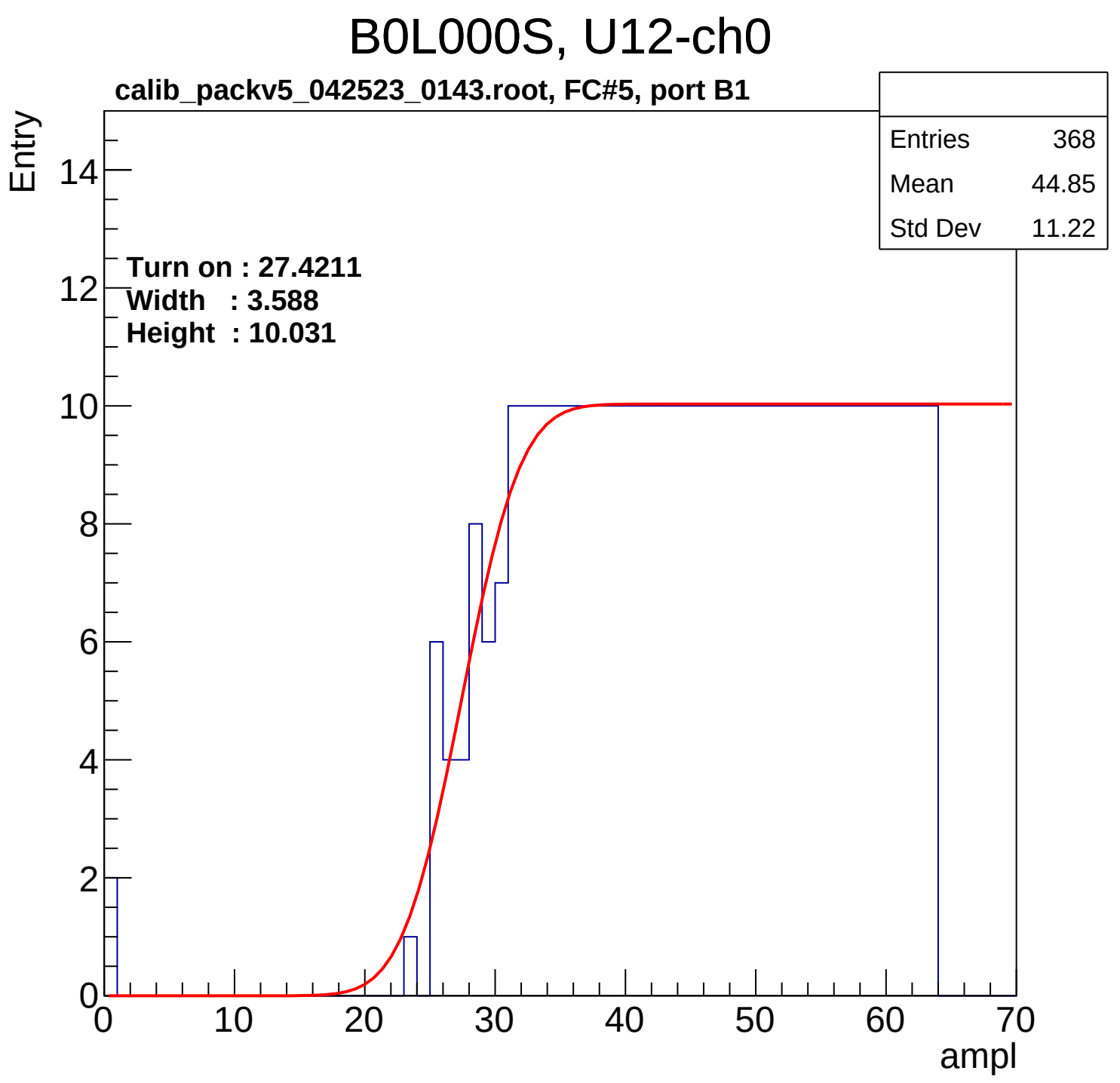
B0L000S, U12-ch0
calib_packv5_042523_0143.root, FC#5, port B1
Entries 368
Mean 44.85
Std Dev 11.22
Turn on : 27.4211
Width : 3.588
Height : 10.031
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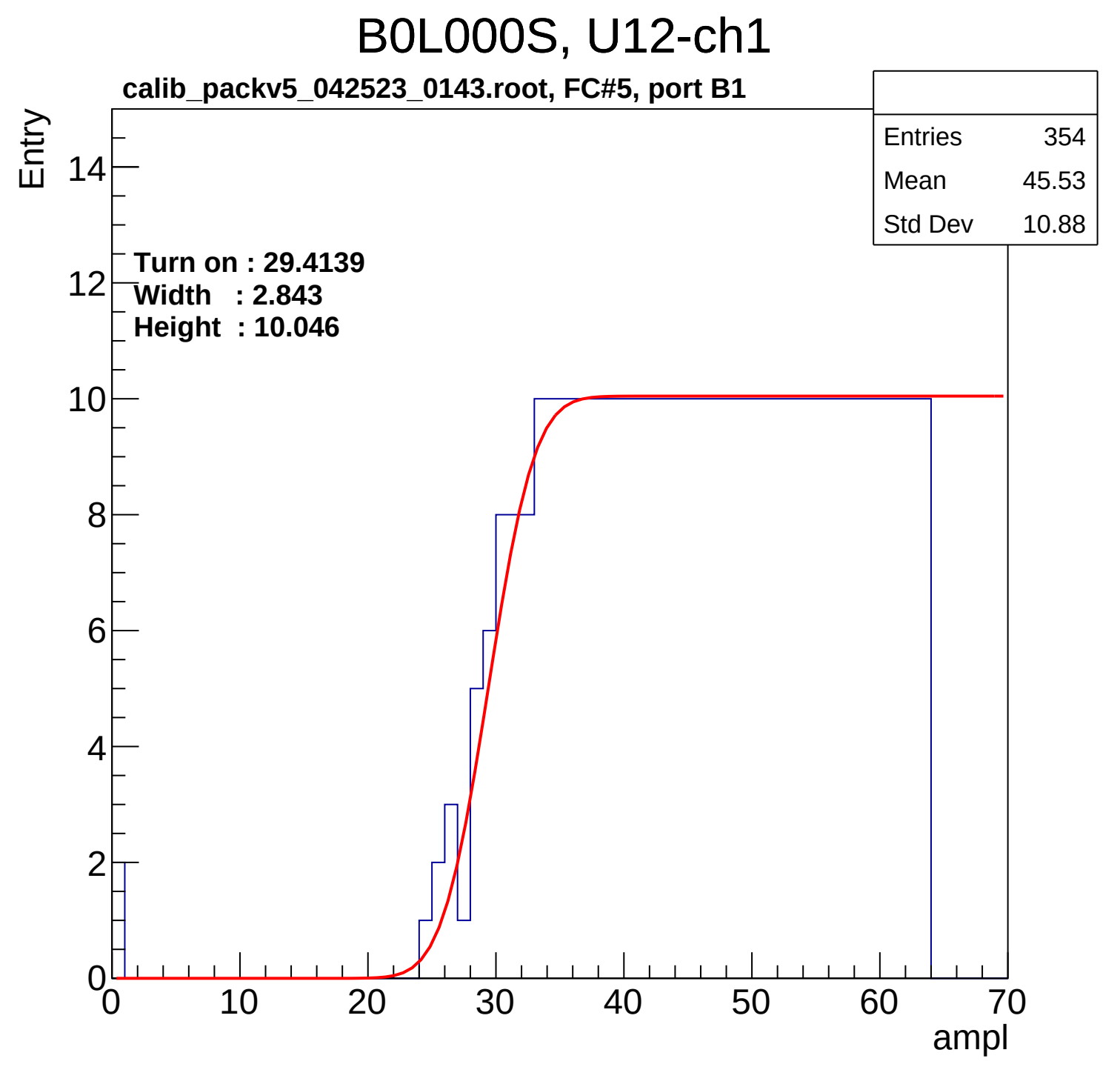
B0L000S, U12-ch1
calib_packv5_042523_0143.root, FC#5, port B1
Entries 354
Mean 45.53
Std Dev 10.88
Turn on : 29.4139
Width : 2.843
Height : 10.046
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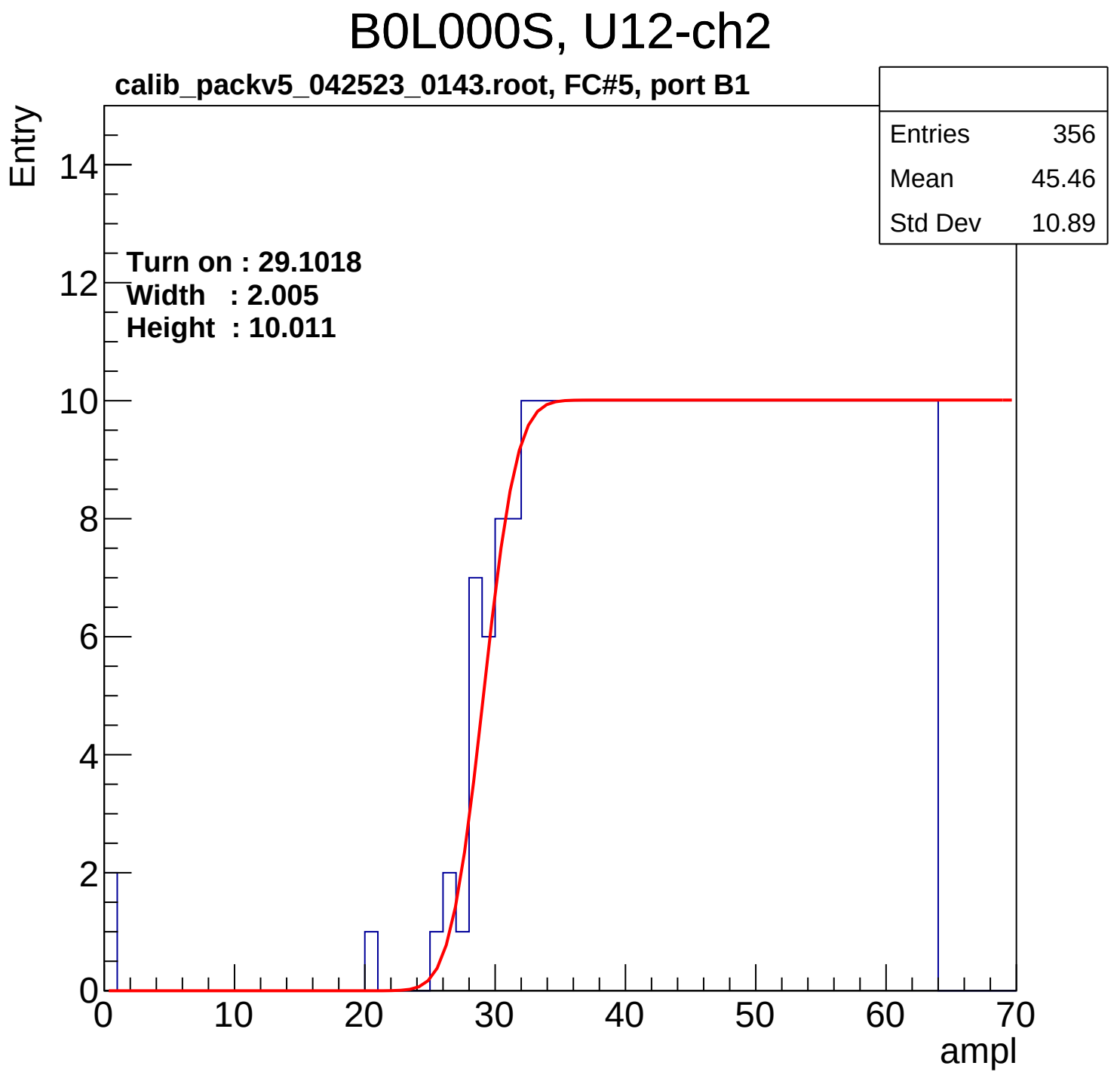
B0L000S, U12-ch2
calib_packv5_042523_0143.root, FC#5, port B1
Entries 356
Mean 45.46
Std Dev 10.89
Turn on : 29.1018
Width : 2.005
Height : 10.011
Entry
ampl
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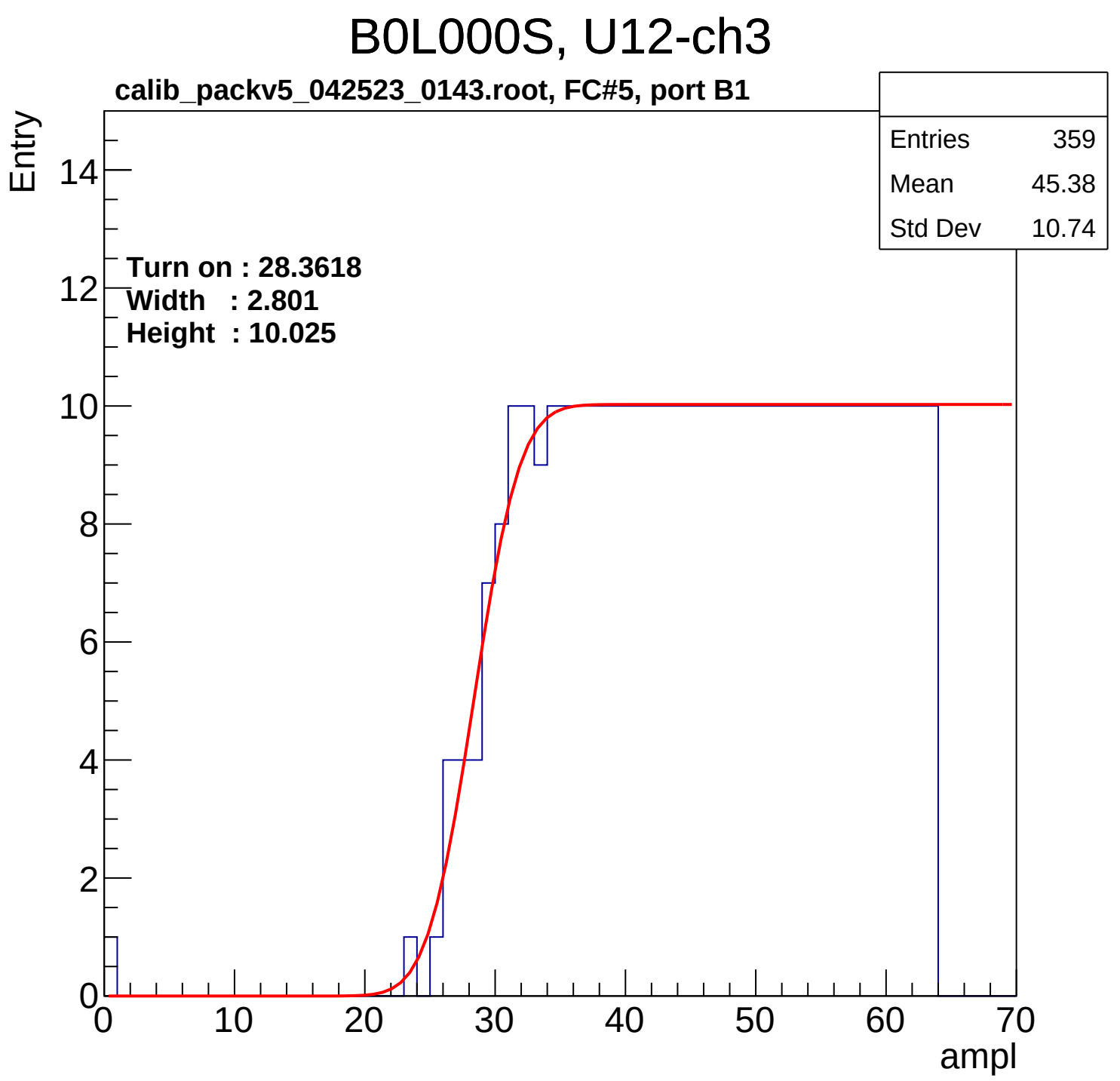
B0L000S, U12-ch3
calib_packv5_042523_0143.root, FC#5, port B1
Entries 359
Mean 45.38
Std Dev 10.74
Turn on : 28.3618
Width : 2.801
Height : 10.025
Entry
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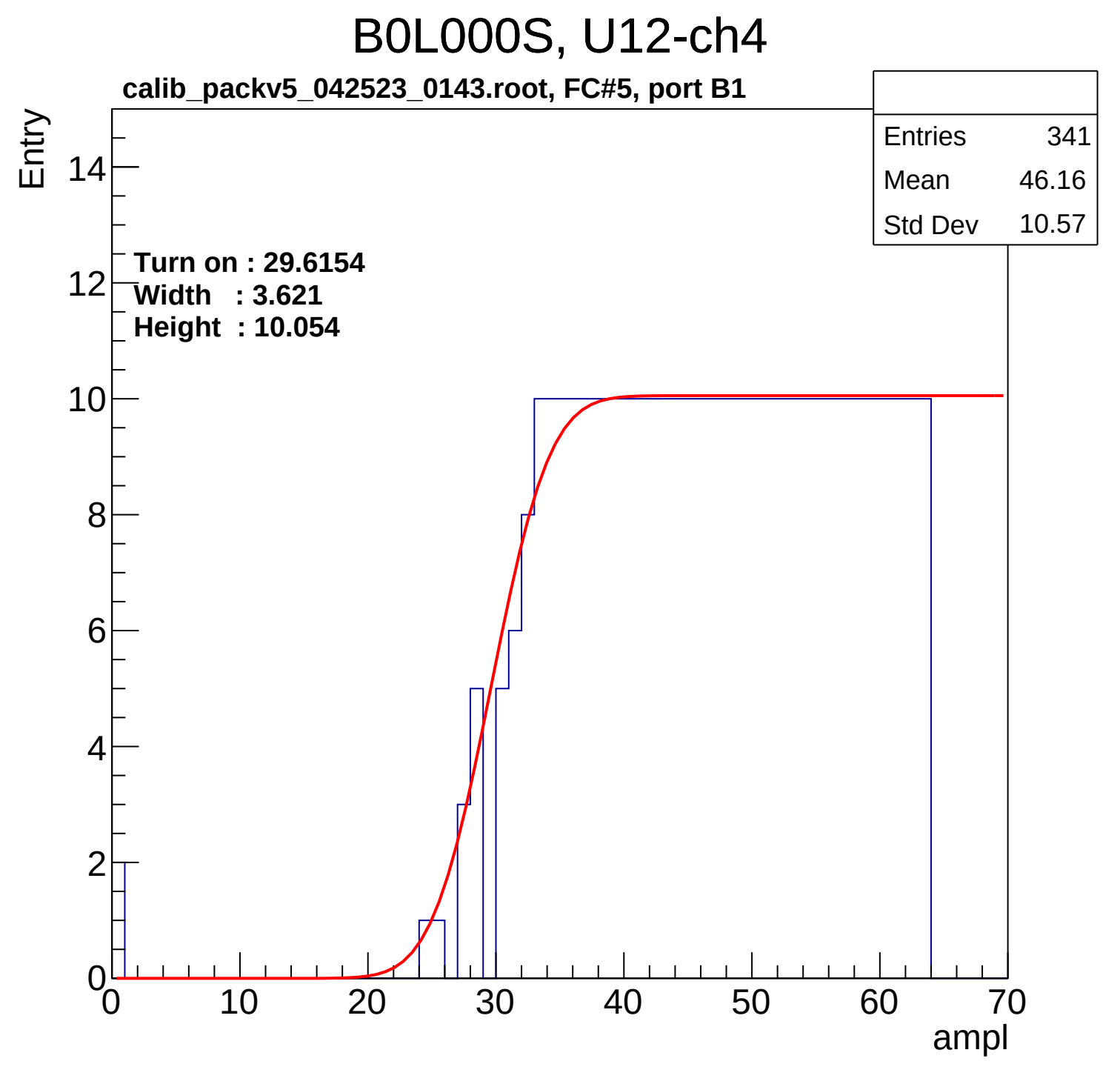
B0L000S, U12-ch4
calib_packv5_042523_0143.root, FC#5, port B1
Entries 341
Mean 46.16
Std Dev 10.57
Turn on : 29.6154
Width : 3.621
Height : 10.054
Entry
ampl
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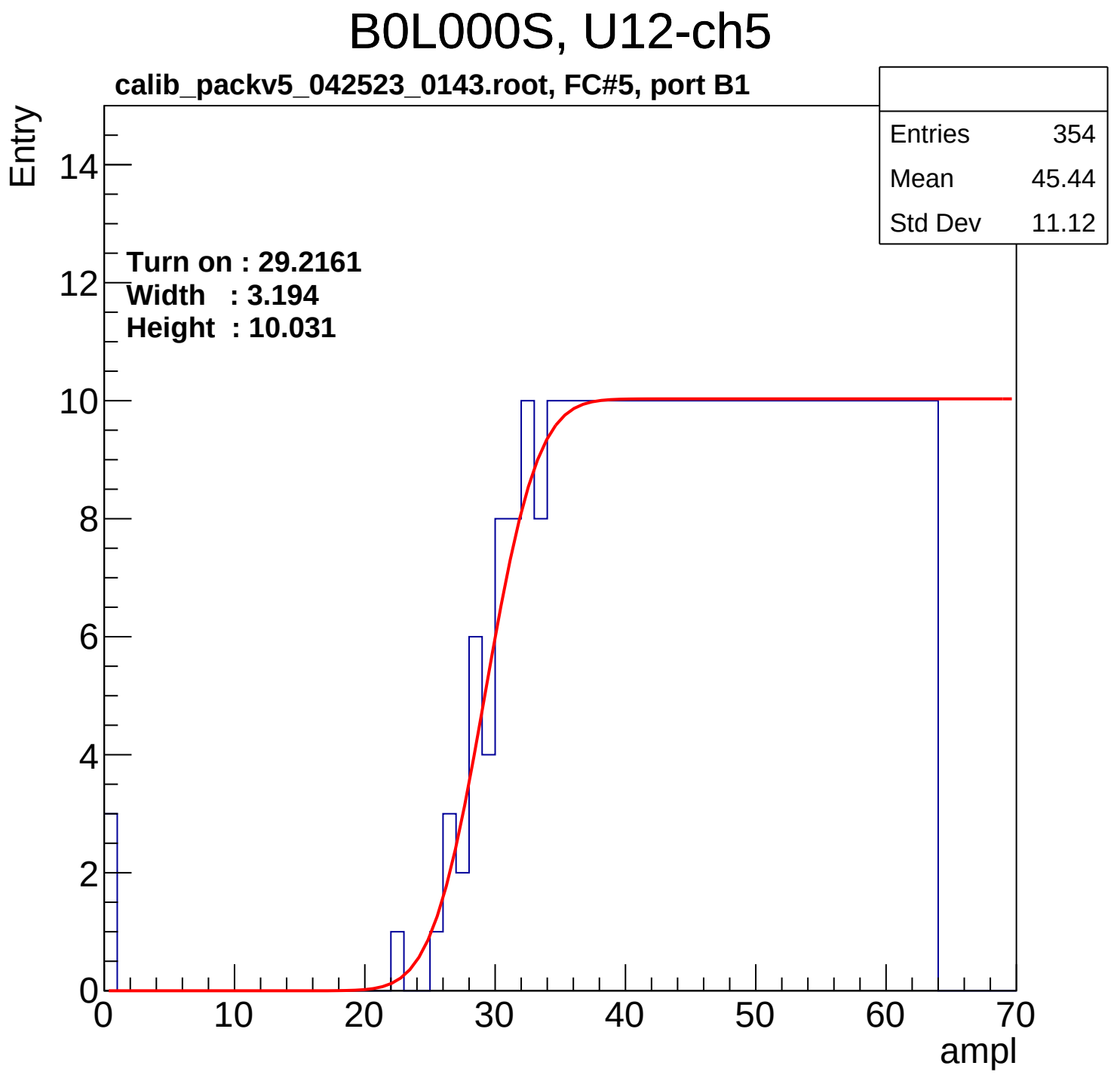
B0L000S, U12-ch5
calib_packv5_042523_0143.root, FC#5, port B1
Entries 354
Mean 45.44
Std Dev 11.12
Turn on : 29.2161
Width : 3.194
Height : 10.031
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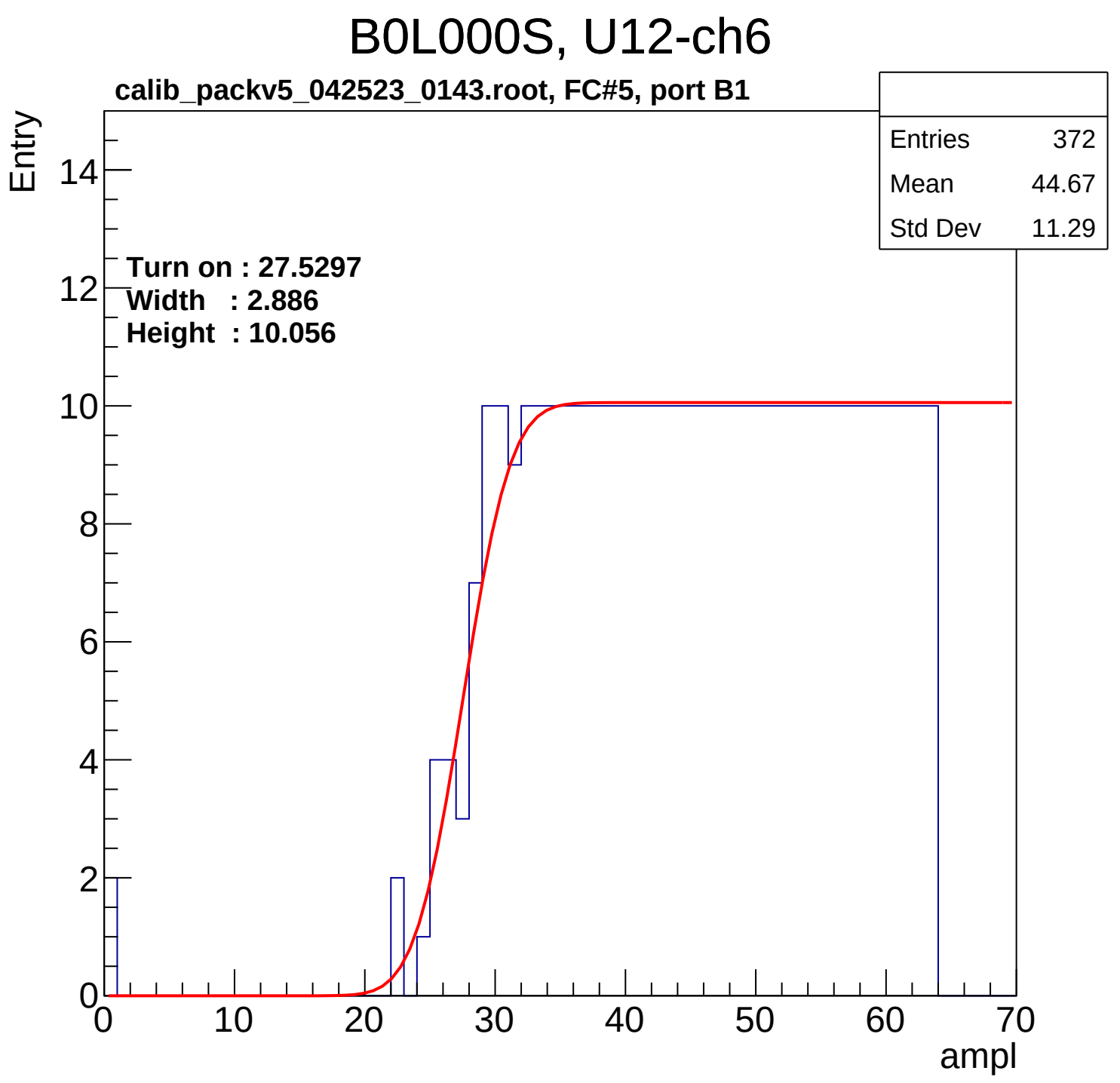
B0L000S, U12-ch6
calib_packv5_042523_0143.root, FC#5, port B1
Entries 372
Mean 44.67
Std Dev 11.29
Turn on : 27.5297
Width : 2.886
Height : 10.056
Entry
ampl
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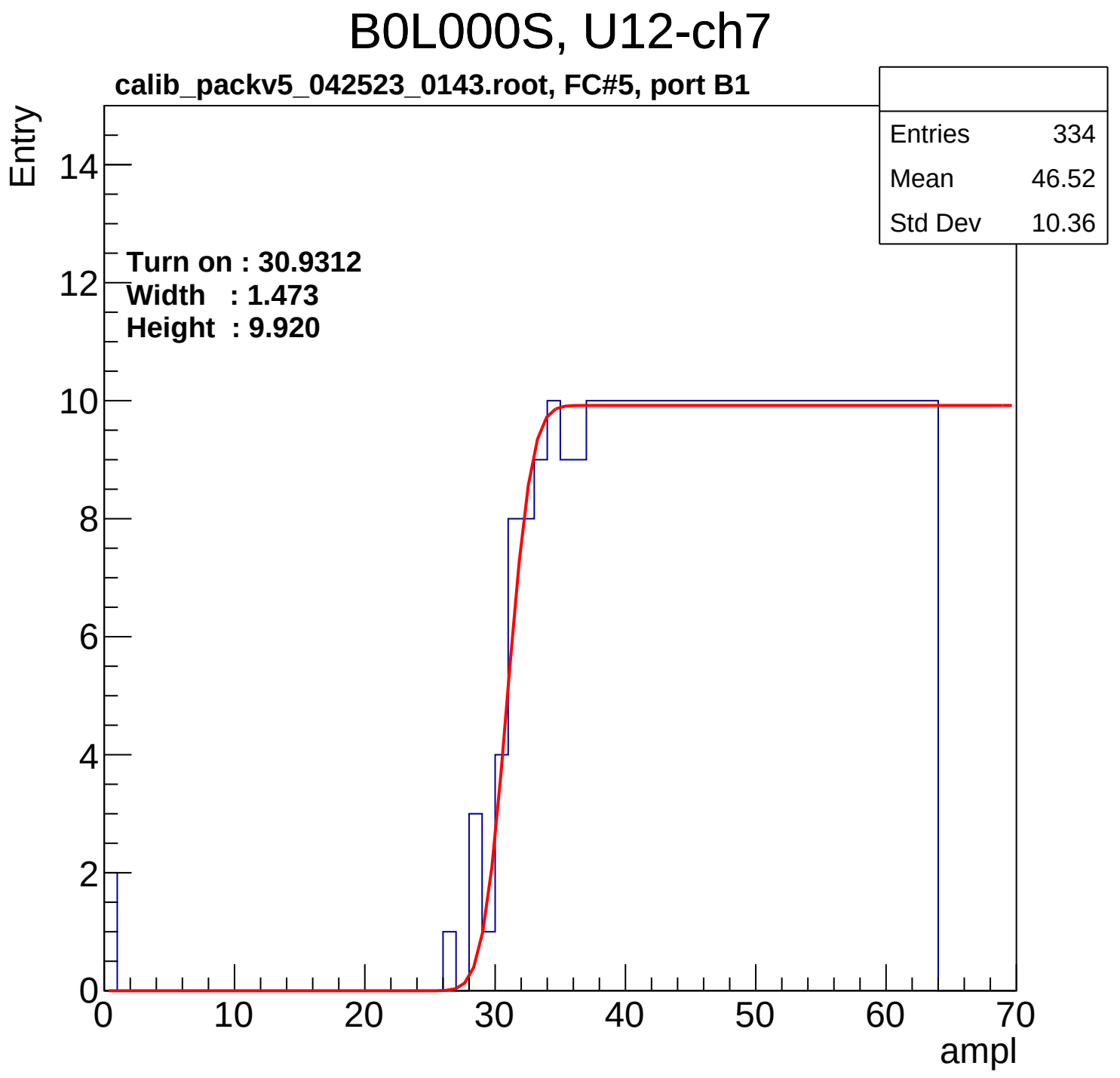
B0L000S, U12-ch7
calib_packv5_042523_0143.root, FC#5, port B1
Entries 334
Mean 46.52
Std Dev 10.36
Turn on : 30.9312
Width : 1.473
Height : 9.920
Entry
ampl
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2
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6
8
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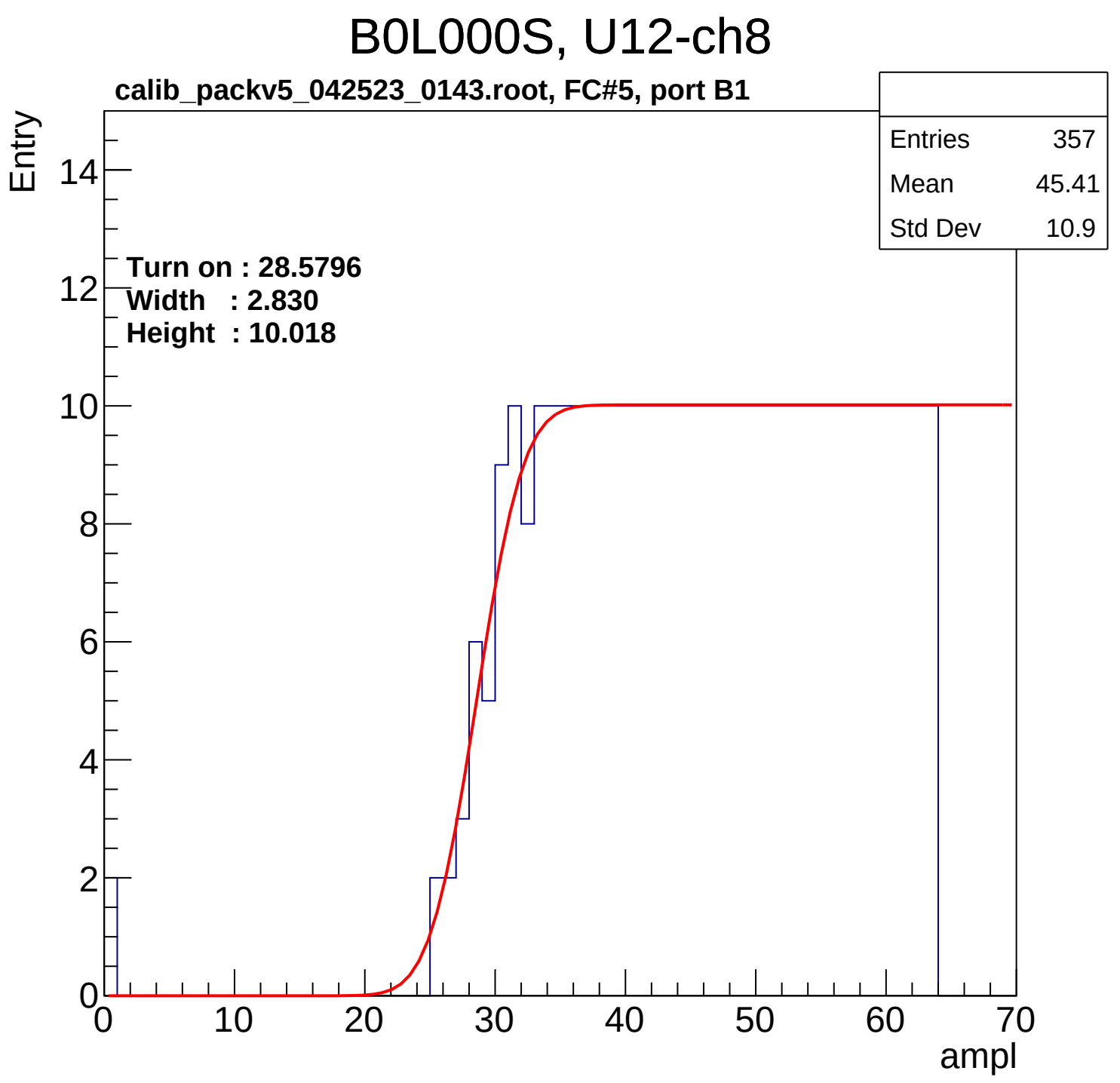
B0L000S, U12-ch8
calib_packv5_042523_0143.root, FC#5, port B1
Entries 357
Mean 45.41
Std Dev 10.9
Turn on : 28.5796
Width : 2.830
Height : 10.018
Entry
ampl
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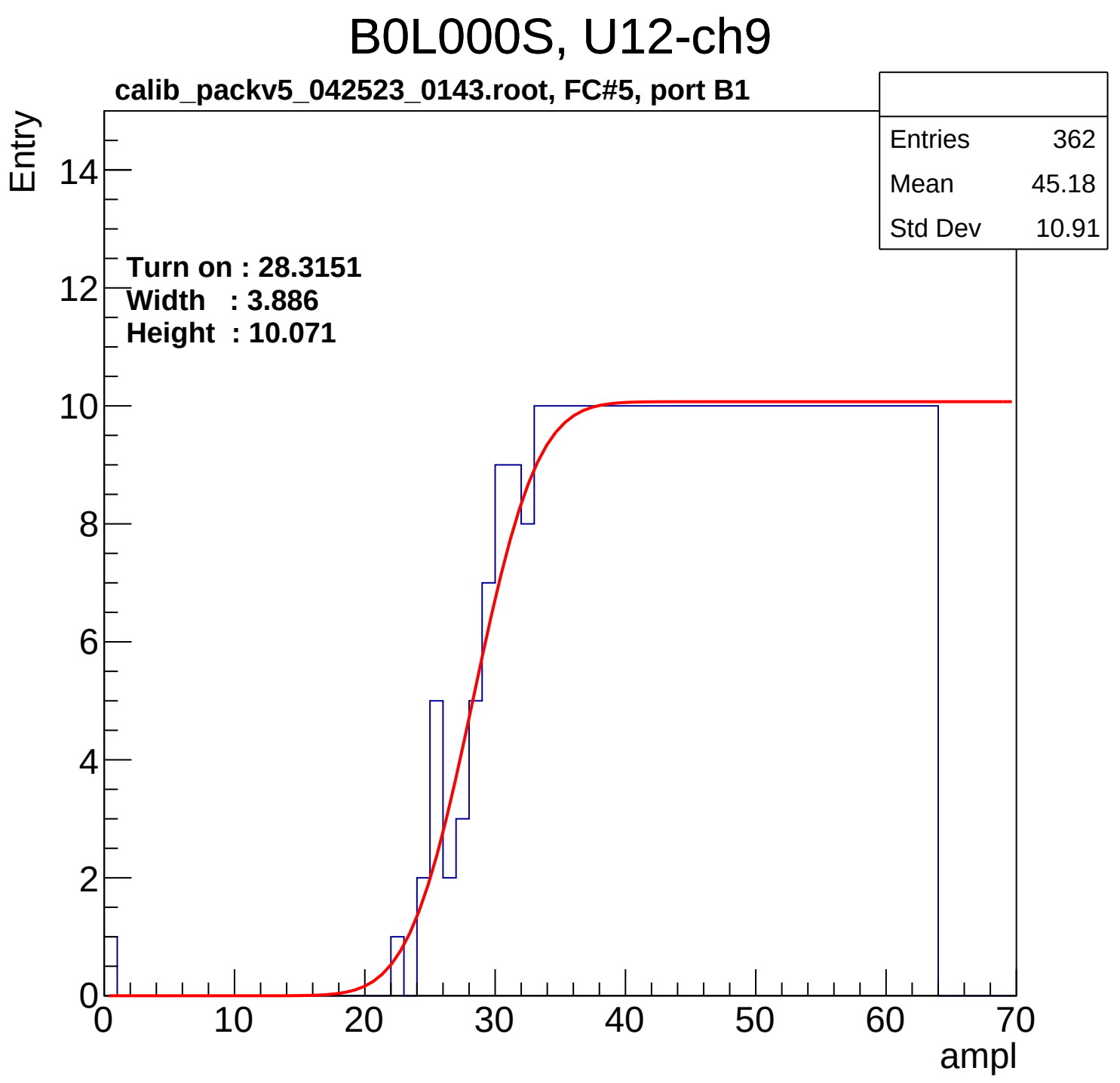
B0L000S, U12-ch9
calib_packv5_042523_0143.root, FC#5, port B1
Entries 362
Mean 45.18
Std Dev 10.91
Turn on : 28.3151
Width : 3.886
Height : 10.071
Entry
ampl
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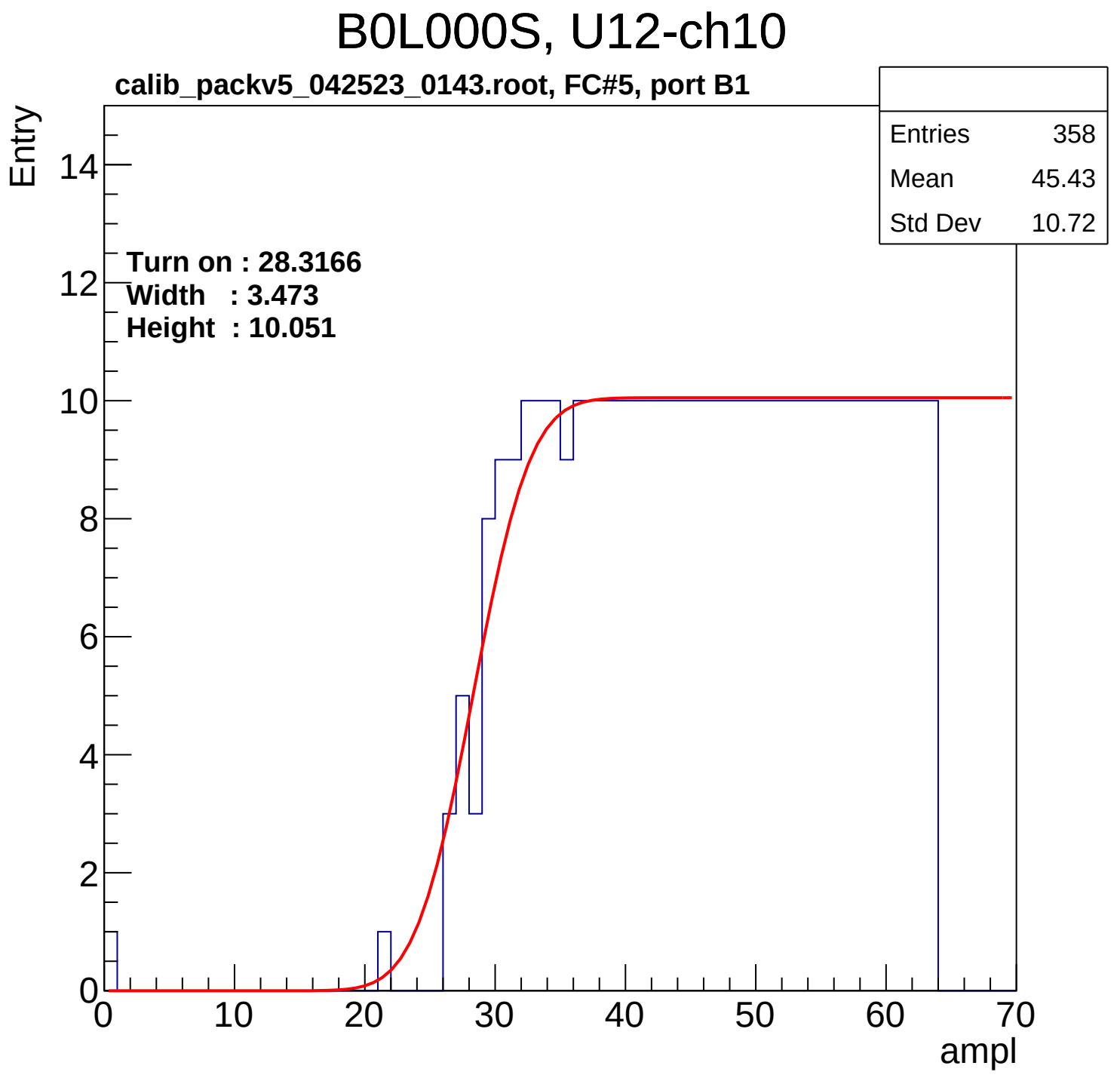
B0L000S, U12-ch10
calib_packv5_042523_0143.root, FC#5, port B1
Entries 358
Mean 45.43
Std Dev 10.72
Turn on : 28.3166
Width : 3.473
Height : 10.051
Entry
ampl
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6
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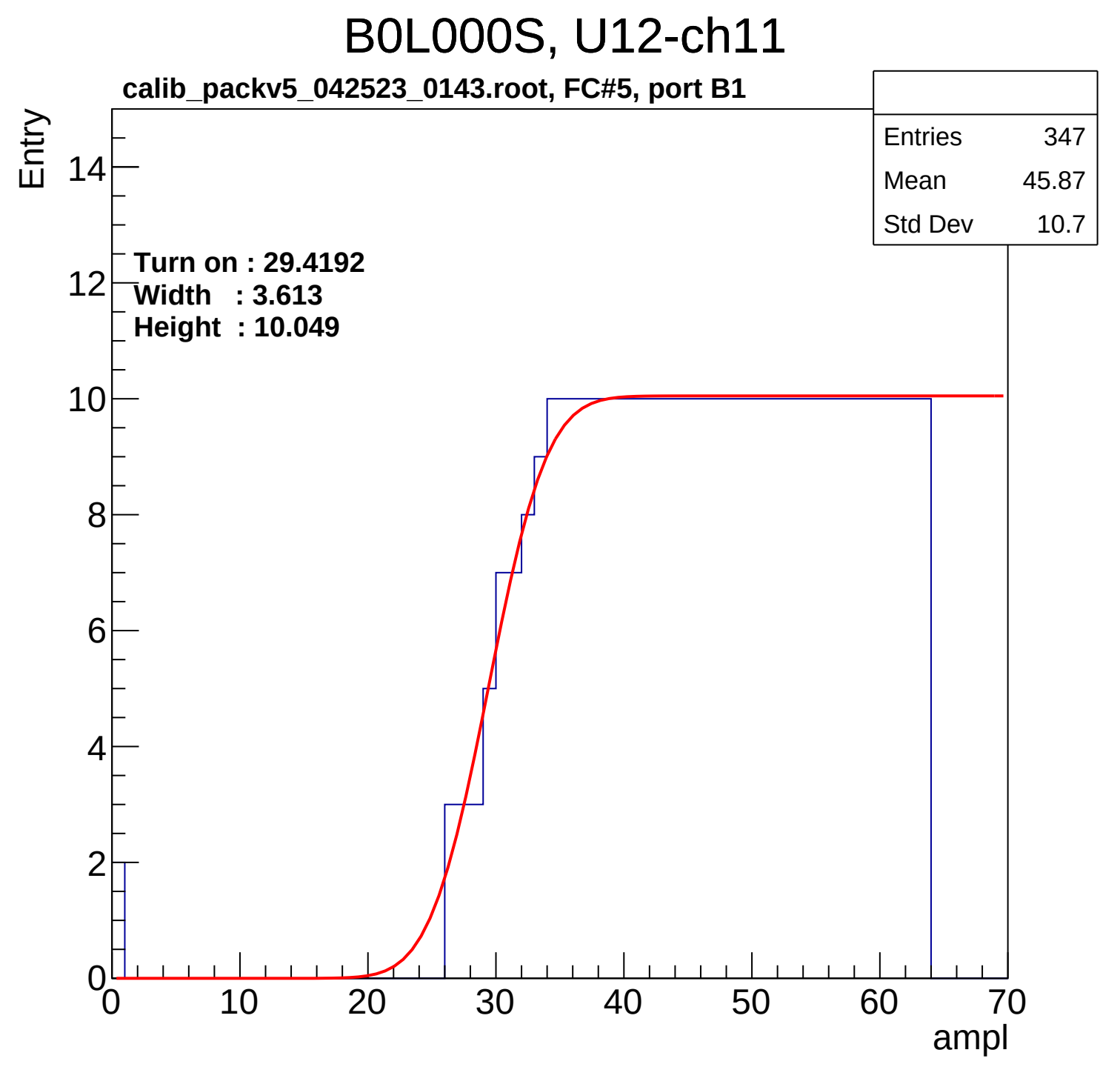
B0L000S, U12-ch11
calib_packv5_042523_0143.root, FC#5, port B1
Entries 347
Mean 45.87
Std Dev 10.7
Turn on : 29.4192
Width : 3.613
Height : 10.049
Entry
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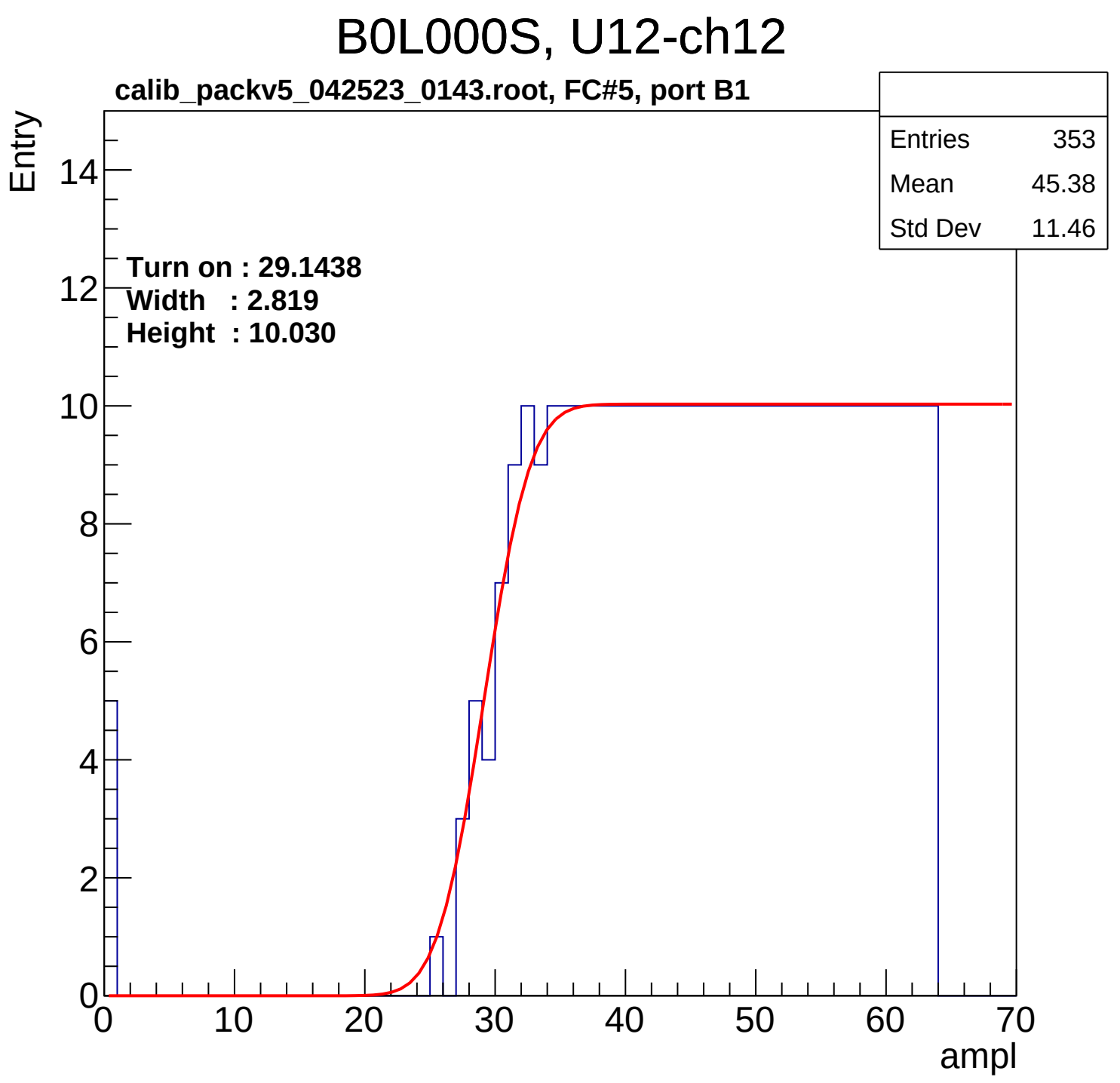
B0L000S, U12-ch12
calib_packv5_042523_0143.root, FC#5, port B1
Entries 353
Mean 45.38
Std Dev 11.46
Turn on : 29.1438
Width : 2.819
Height : 10.030
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ampl
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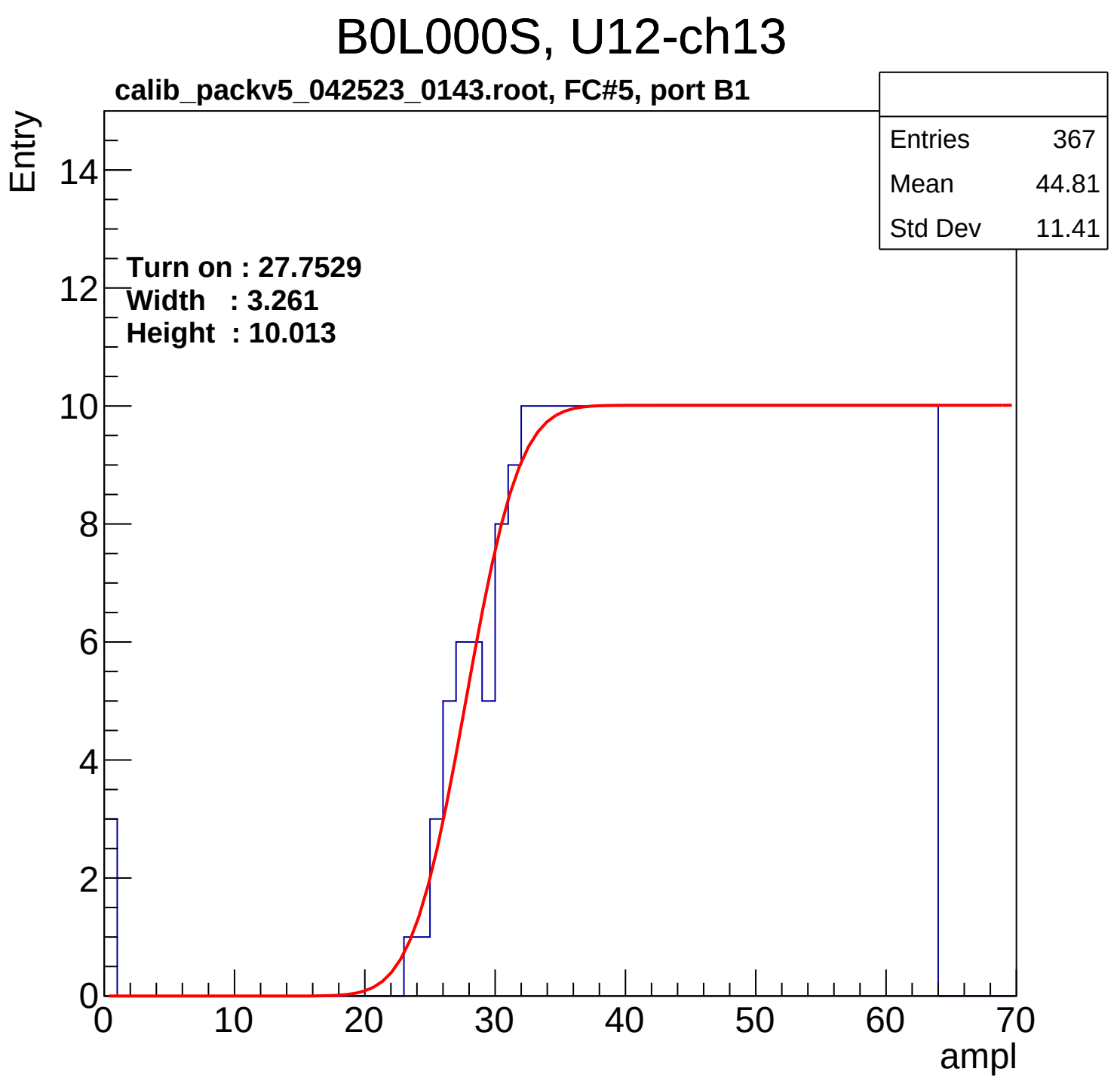
B0L000S, U12-ch13
calib_packv5_042523_0143.root, FC#5, port B1
Entries 367
Mean 44.81
Std Dev 11.41
Turn on : 27.7529
Width : 3.261
Height : 10.013
Entry
ampl
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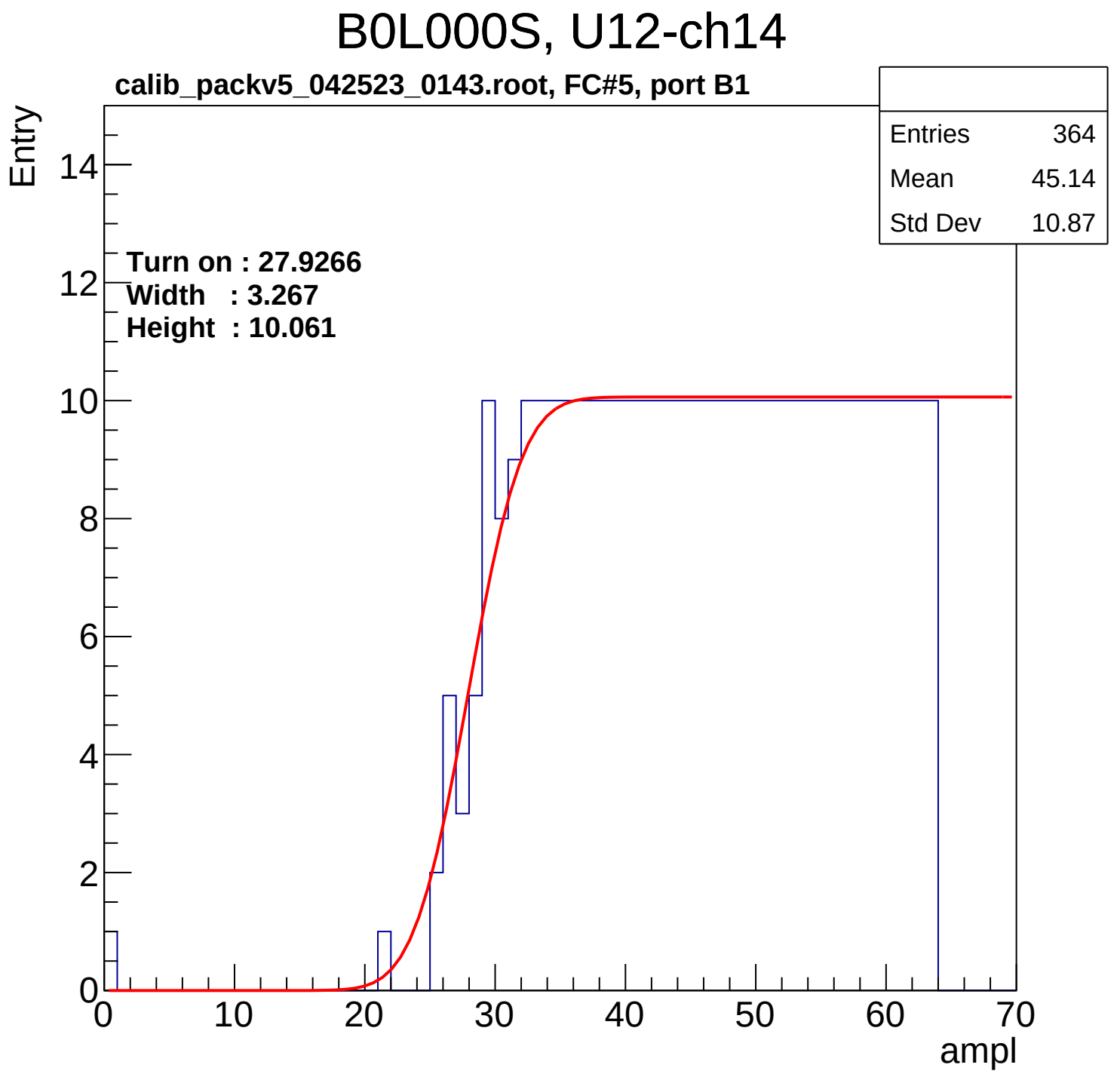
B0L000S, U12-ch14
calib_packv5_042523_0143.root, FC#5, port B1
Entries 364
Mean 45.14
Std Dev 10.87
Turn on : 27.9266
Width : 3.267
Height : 10.061
Entry
ampl
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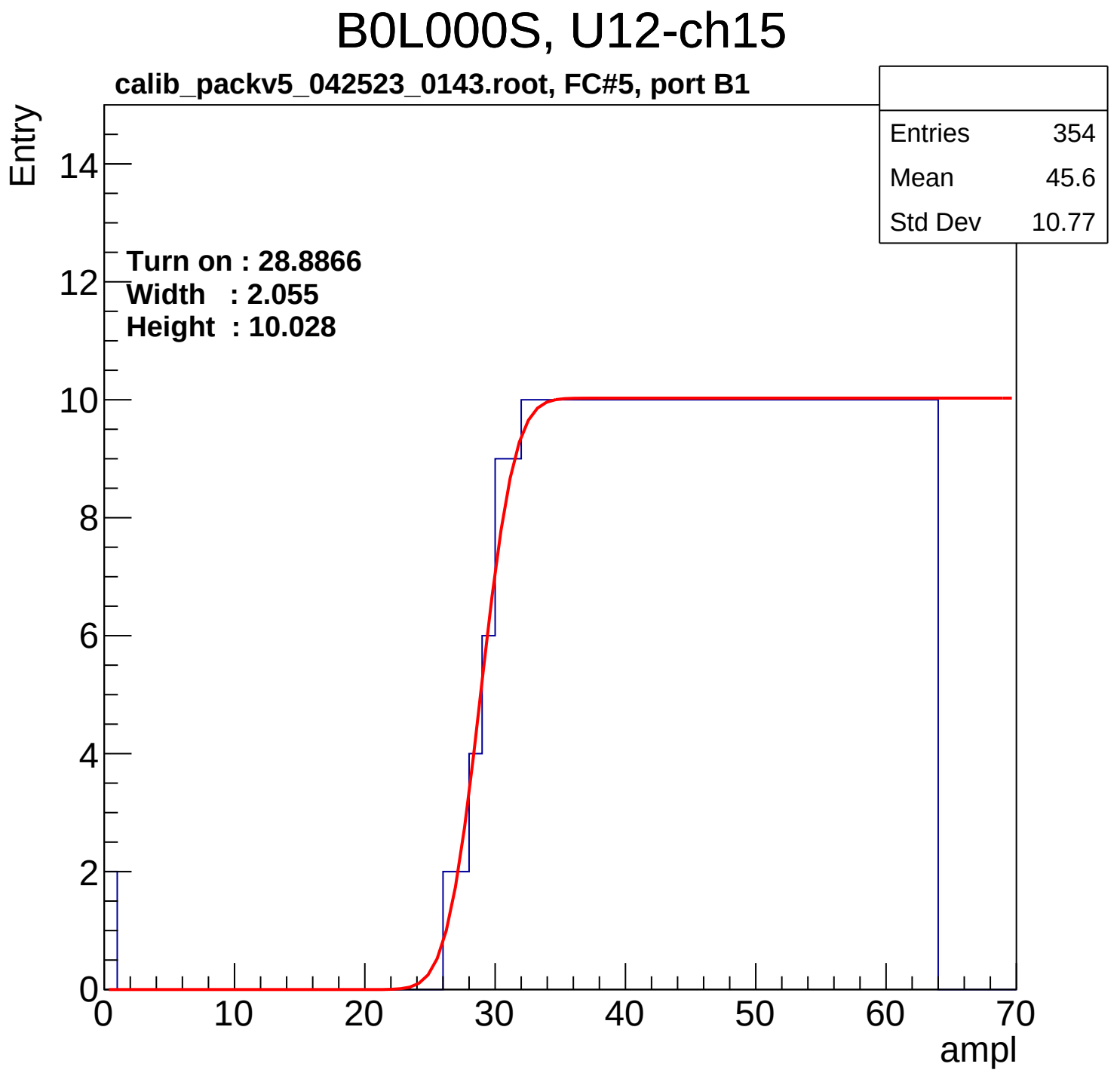
B0L000S, U12-ch15
calib_packv5_042523_0143.root, FC#5, port B1
Entries 354
Mean 45.6
Std Dev 10.77
Turn on : 28.8866
Width : 2.055
Height : 10.028
Entry
ampl
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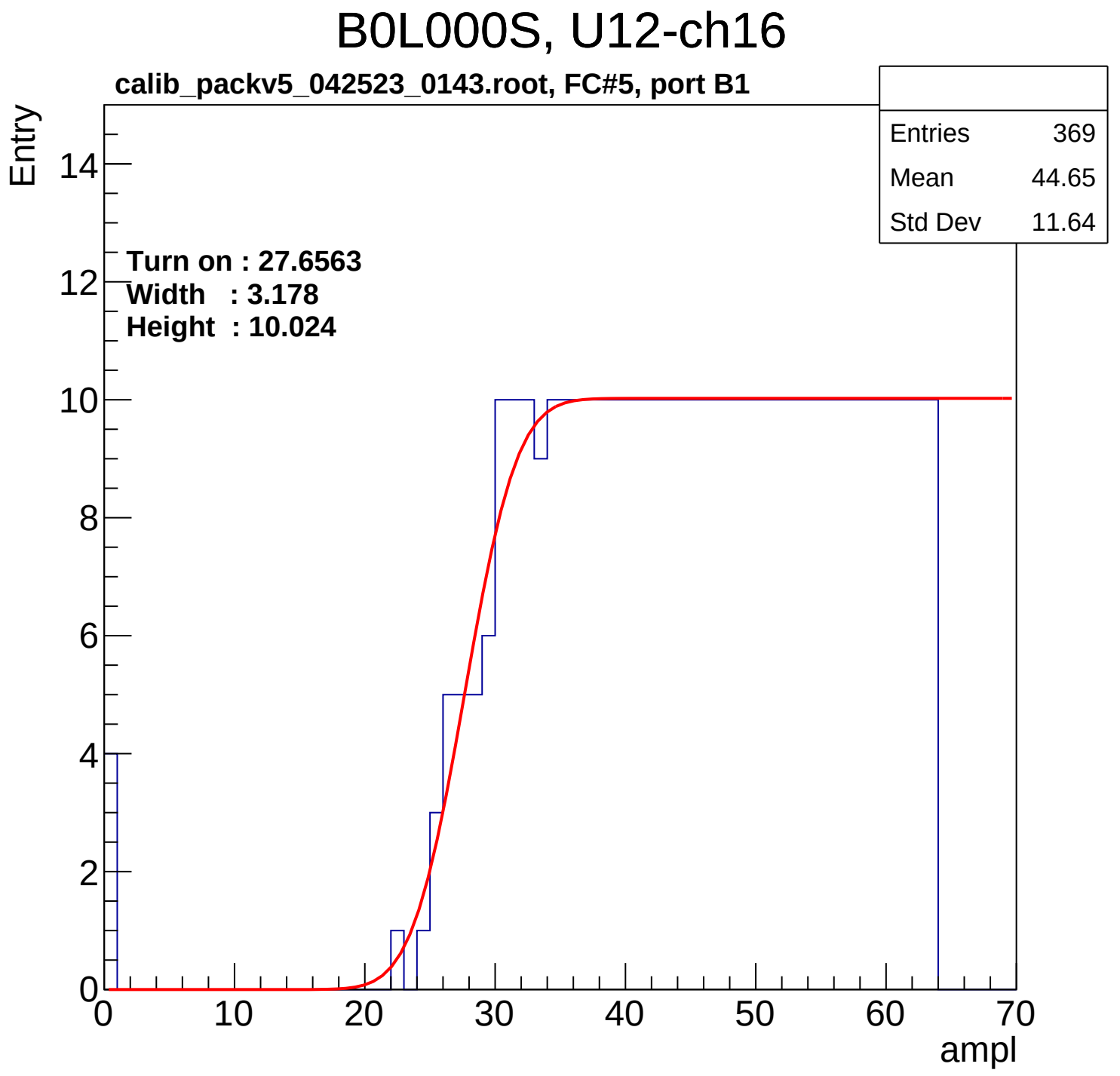
B0L000S, U12-ch16
calib_packv5_042523_0143.root, FC#5, port B1
Entries 369
Mean 44.65
Std Dev 11.64
Turn on : 27.6563
Width : 3.178
Height : 10.024
Entry
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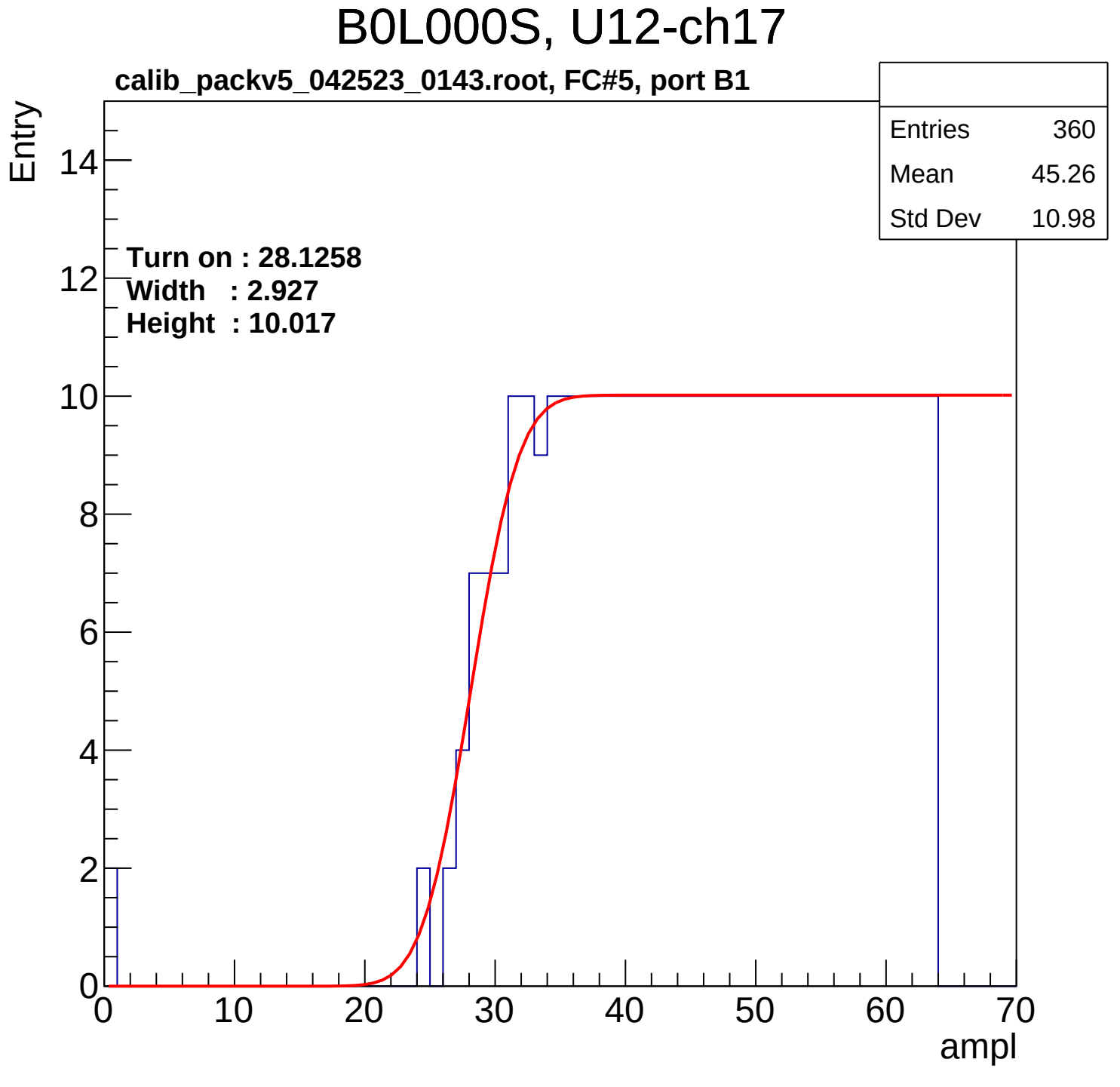
B0L000S, U12-ch17
calib_packv5_042523_0143.root, FC#5, port B1
Entries 360
Mean 45.26
Std Dev 10.98
Turn on : 28.1258
Width : 2.927
Height : 10.017
Entry
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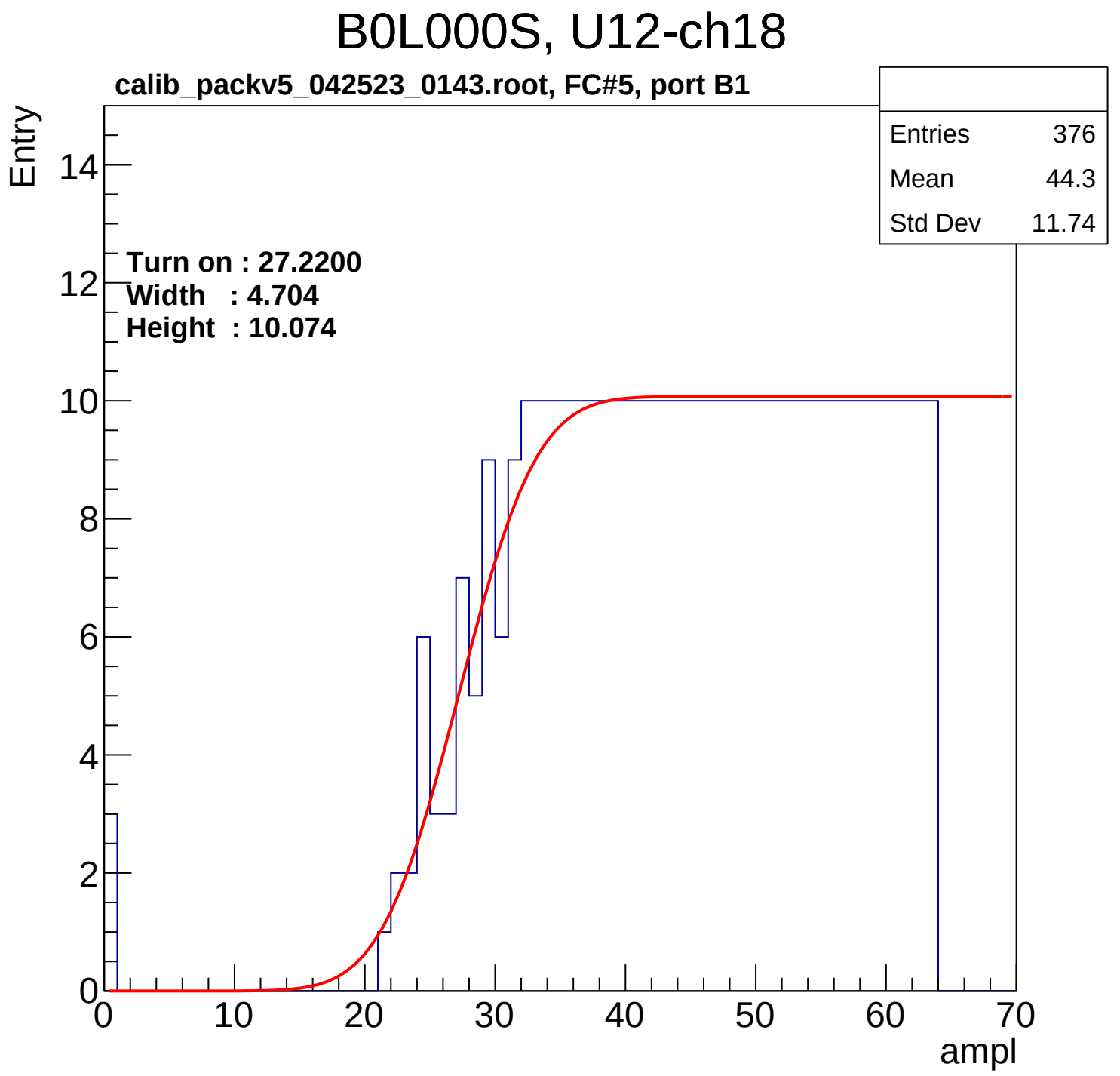
B0L000S, U12-ch18
calib_packv5_042523_0143.root, FC#5, port B1
Entries 376
Mean 44.3
Std Dev 11.74
Turn on : 27.2200
Width : 4.704
Height : 10.074
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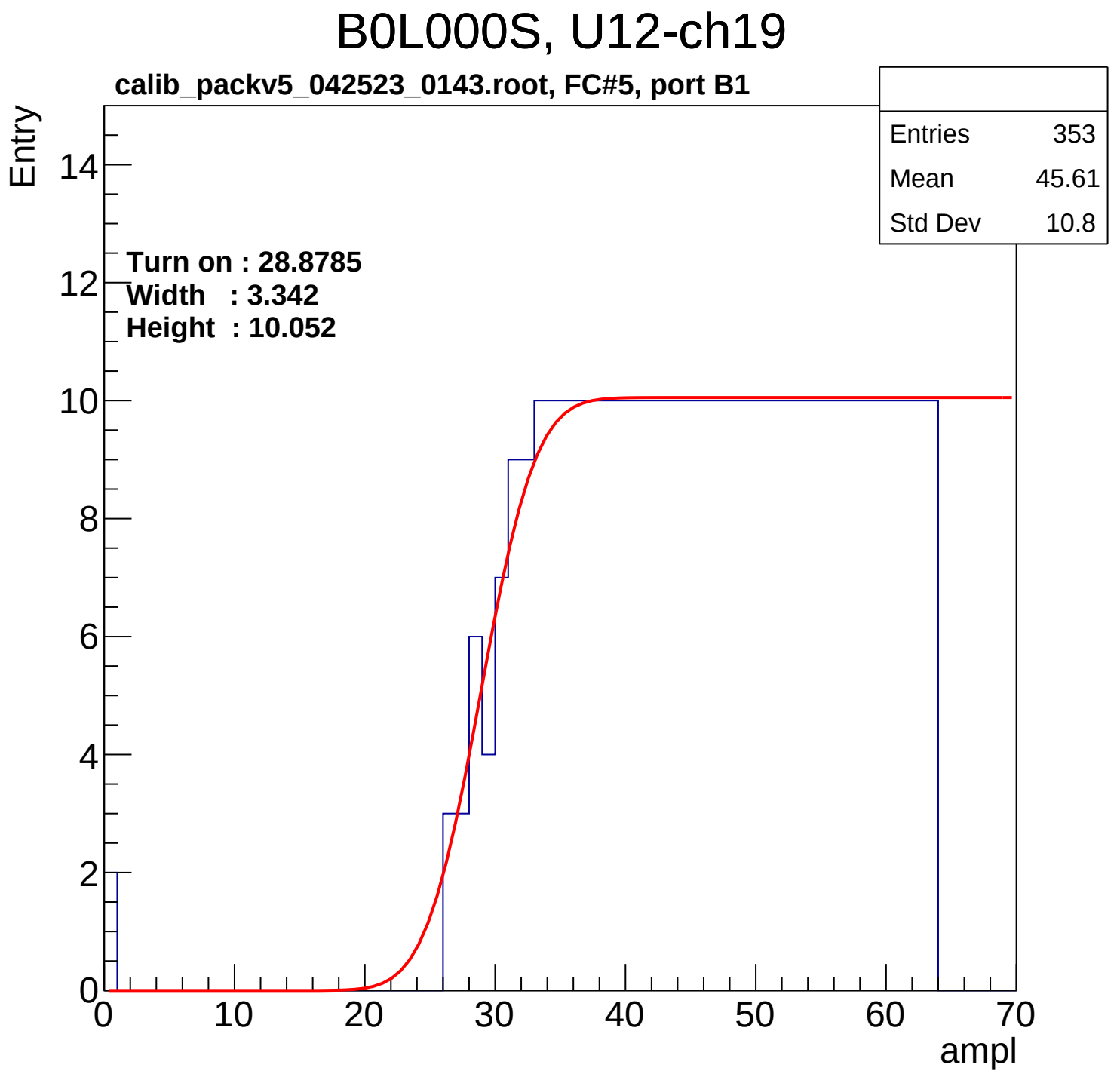
B0L000S, U12-ch19
calib_packv5_042523_0143.root, FC#5, port B1
Entries 353
Mean 45.61
Std Dev 10.8
Turn on : 28.8785
Width : 3.342
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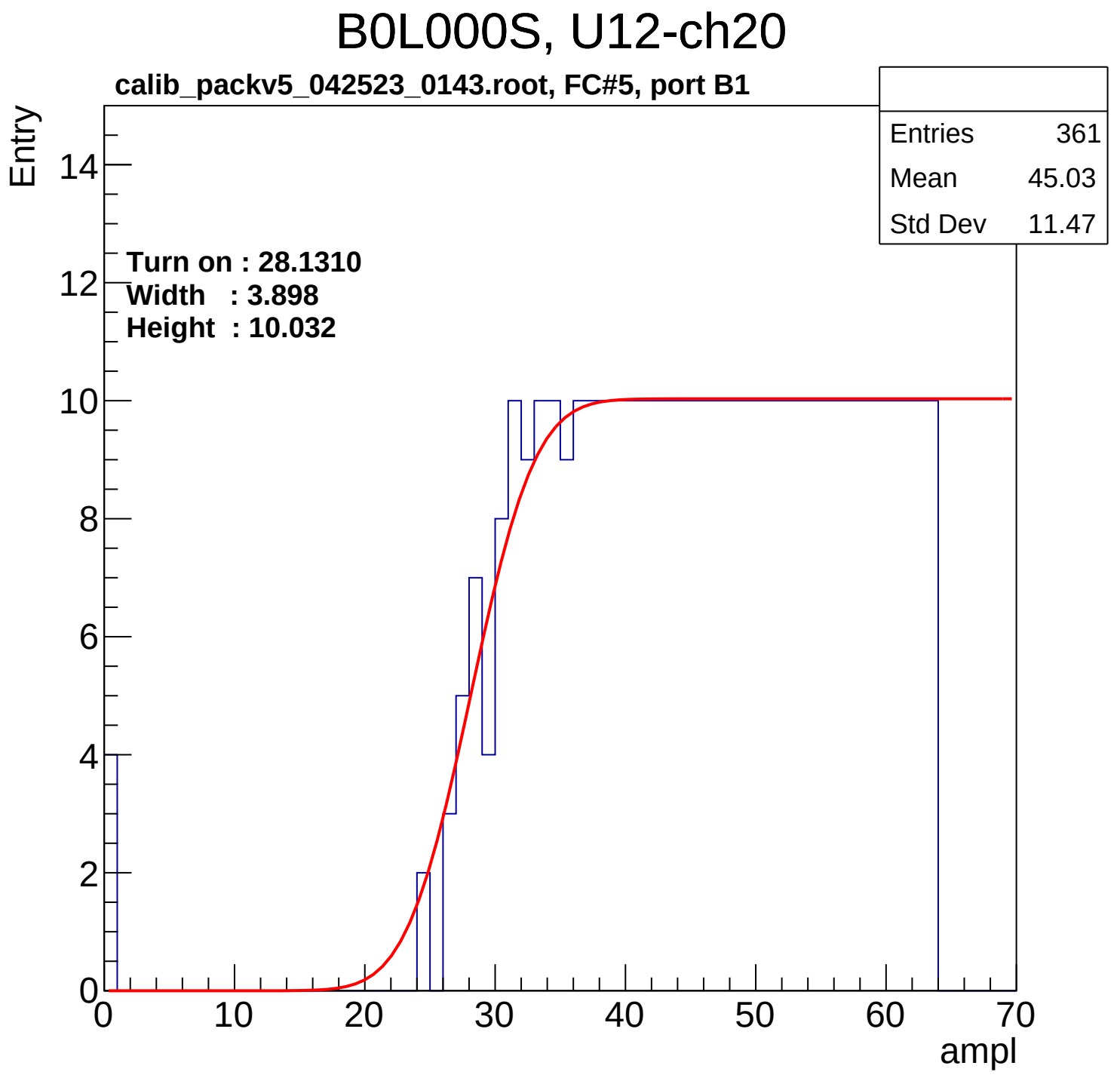
B0L000S, U12-ch20
calib_packv5_042523_0143.root, FC#5, port B1
Entries 361
Mean 45.03
Std Dev 11.47
Turn on : 28.1310
Width : 3.898
Height : 10.032
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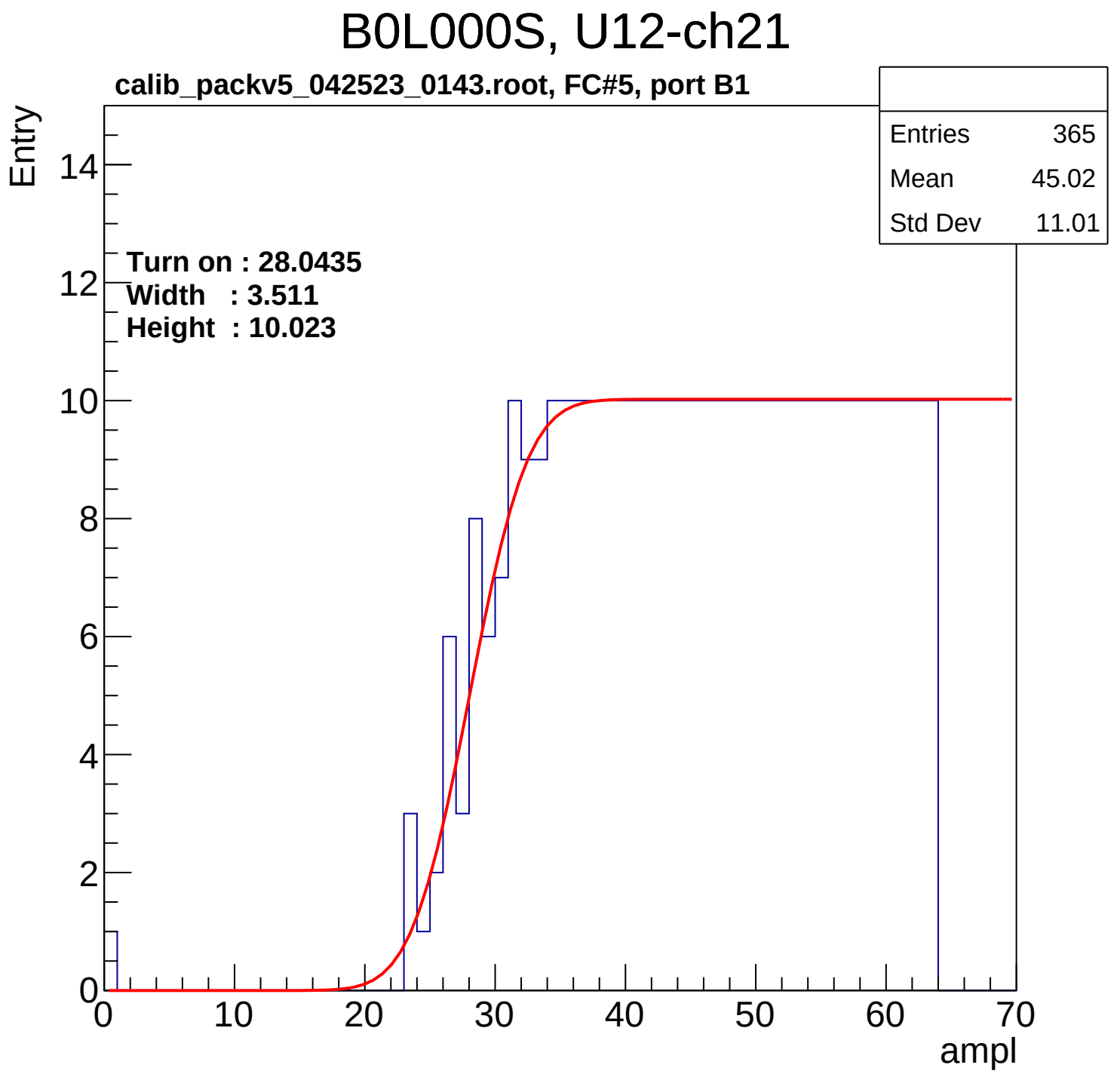
B0L000S, U12-ch21
calib_packv5_042523_0143.root, FC#5, port B1
Entries 365
Mean 45.02
Std Dev 11.01
Turn on : 28.0435
Width : 3.511
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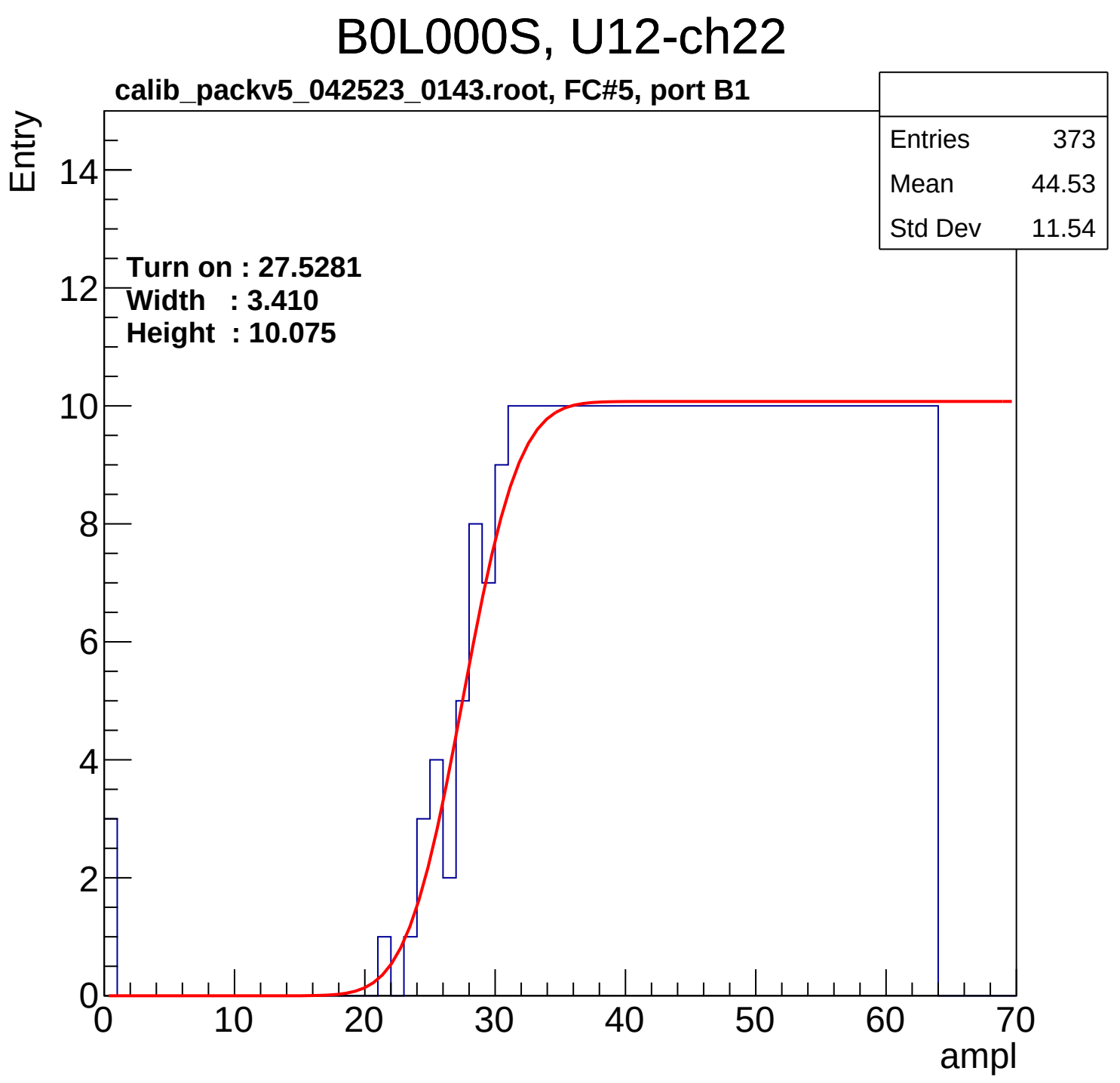
B0L000S, U12-ch22
calib_packv5_042523_0143.root, FC#5, port B1
Entries 373
Mean 44.53
Std Dev 11.54
Turn on : 27.5281
Width : 3.410
Height : 10.075
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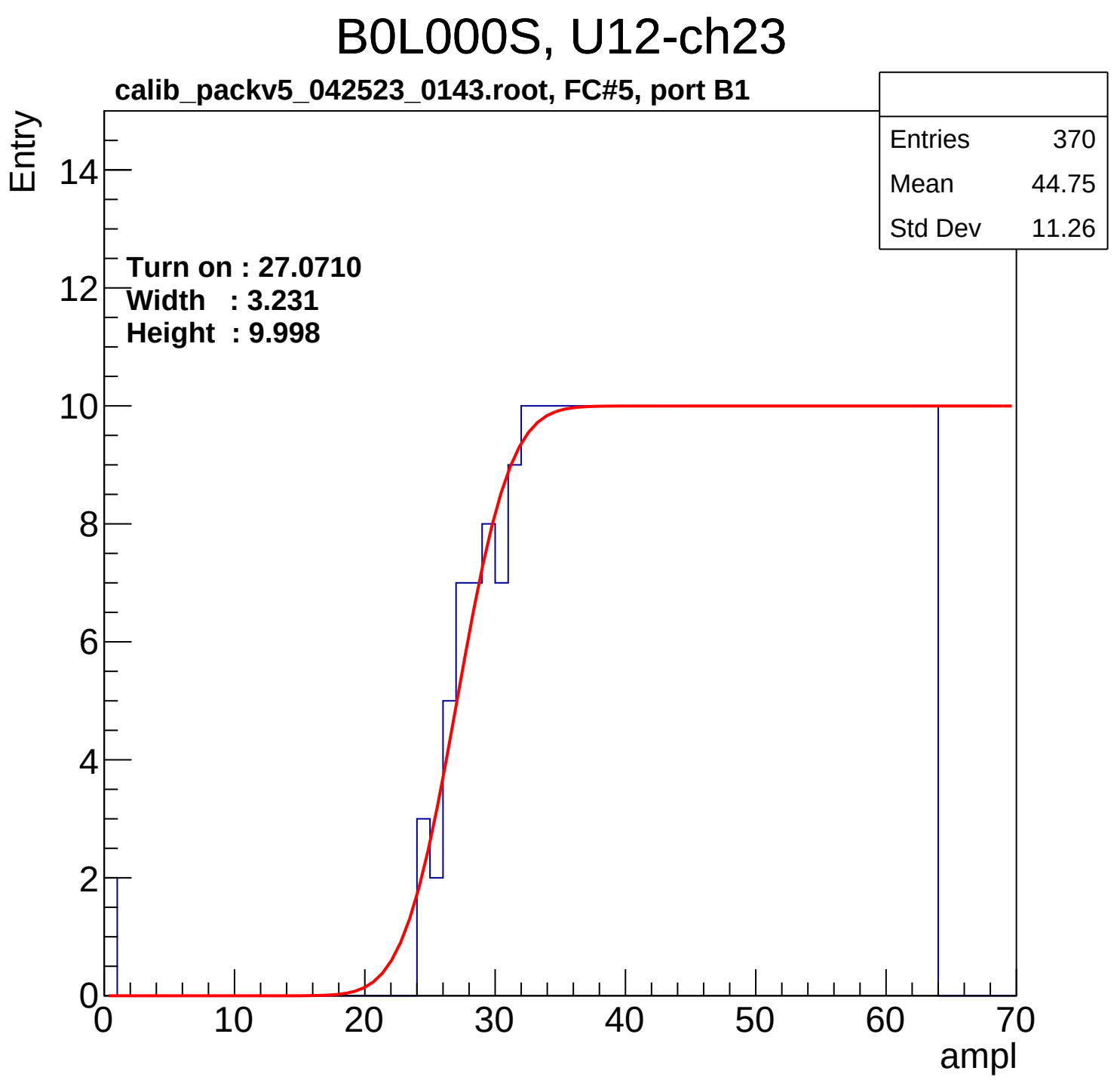
B0L000S, U12-ch23
calib_packv5_042523_0143.root, FC#5, port B1
Entries 370
Mean 44.75
Std Dev 11.26
Turn on : 27.0710
Width : 3.231
Height : 9.998
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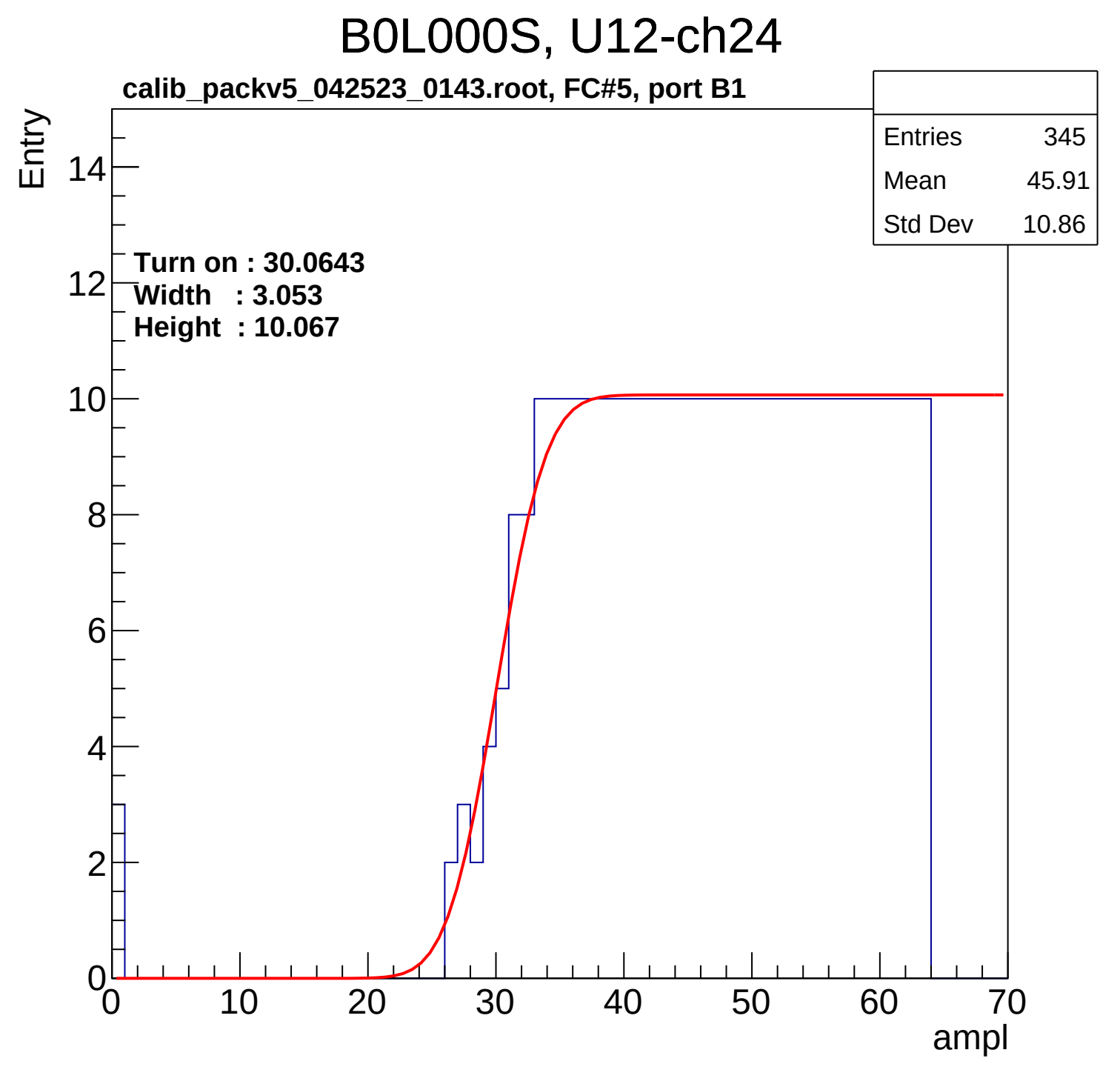
B0L000S, U12-ch24
calib_packv5_042523_0143.root, FC#5, port B1
Entries 345
Mean 45.91
Std Dev 10.86
Turn on : 30.0643
Width : 3.053
Height : 10.067
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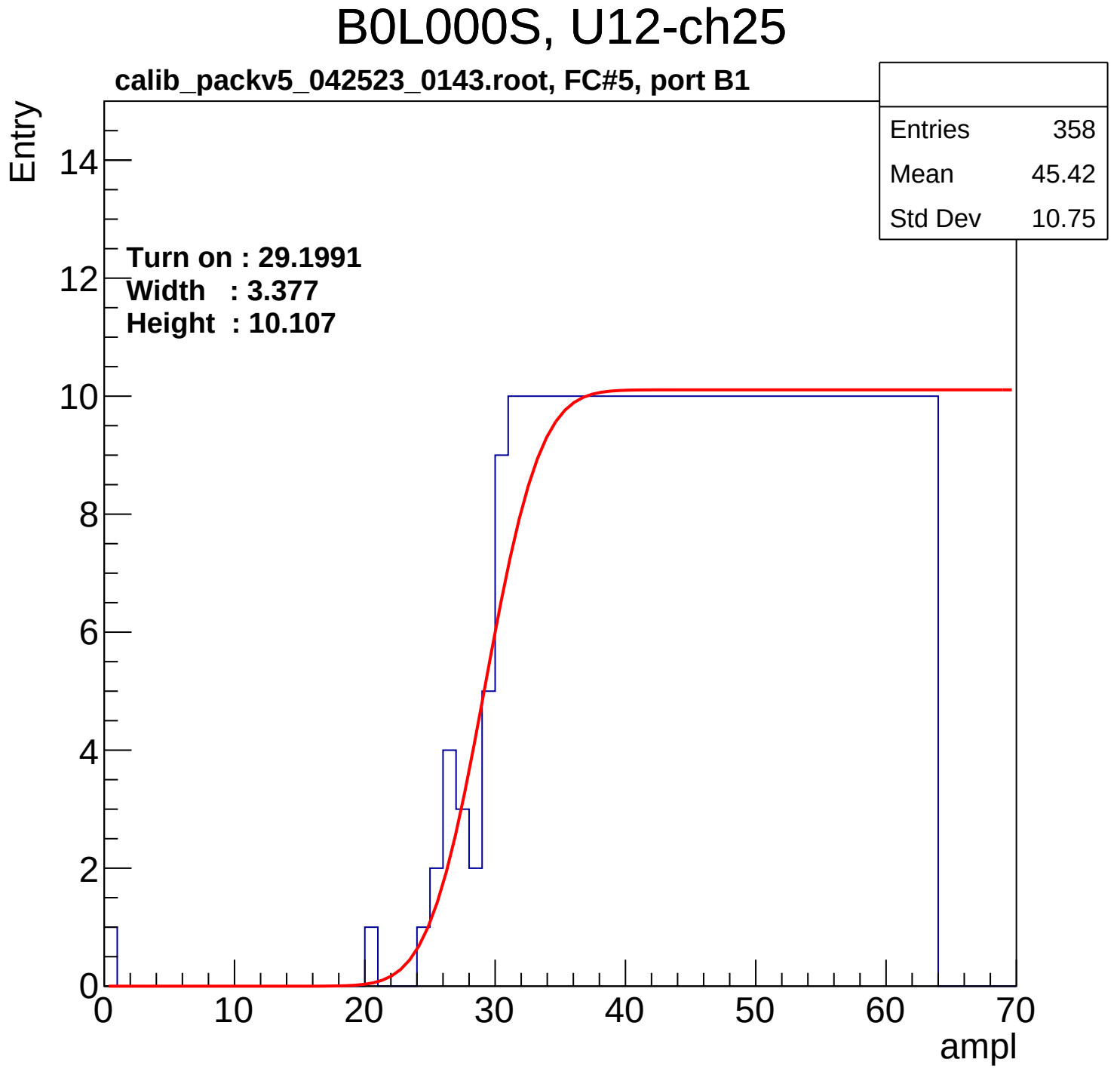
B0L000S, U12-ch25
calib_packv5_042523_0143.root, FC#5, port B1
Entries 358
Mean 45.42
Std Dev 10.75
Turn on : 29.1991
Width : 3.377
Height : 10.107
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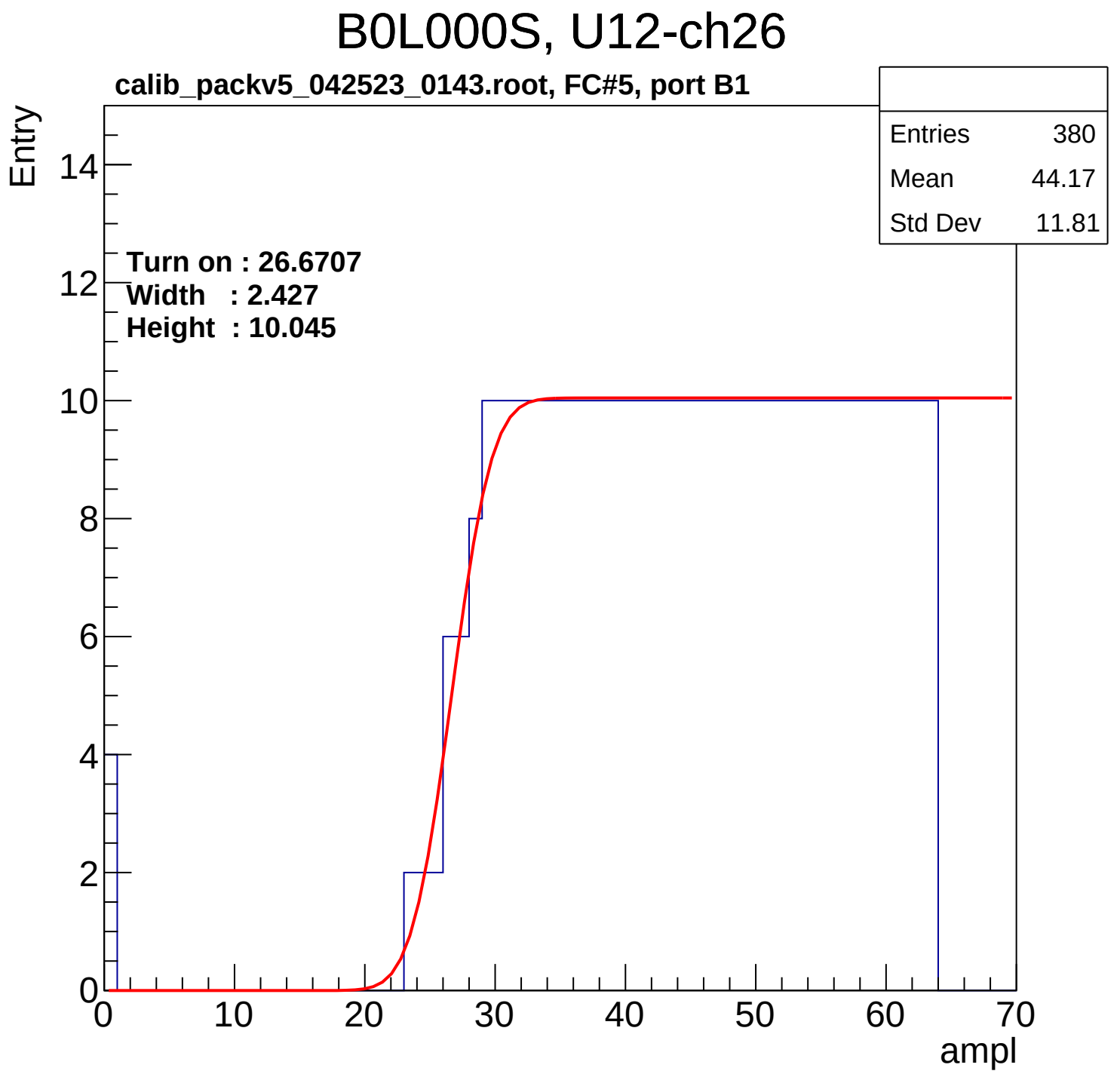
B0L000S, U12-ch26
calib_packv5_042523_0143.root, FC#5, port B1
Entries 380
Mean 44.17
Std Dev 11.81
Turn on : 26.6707
Width : 2.427
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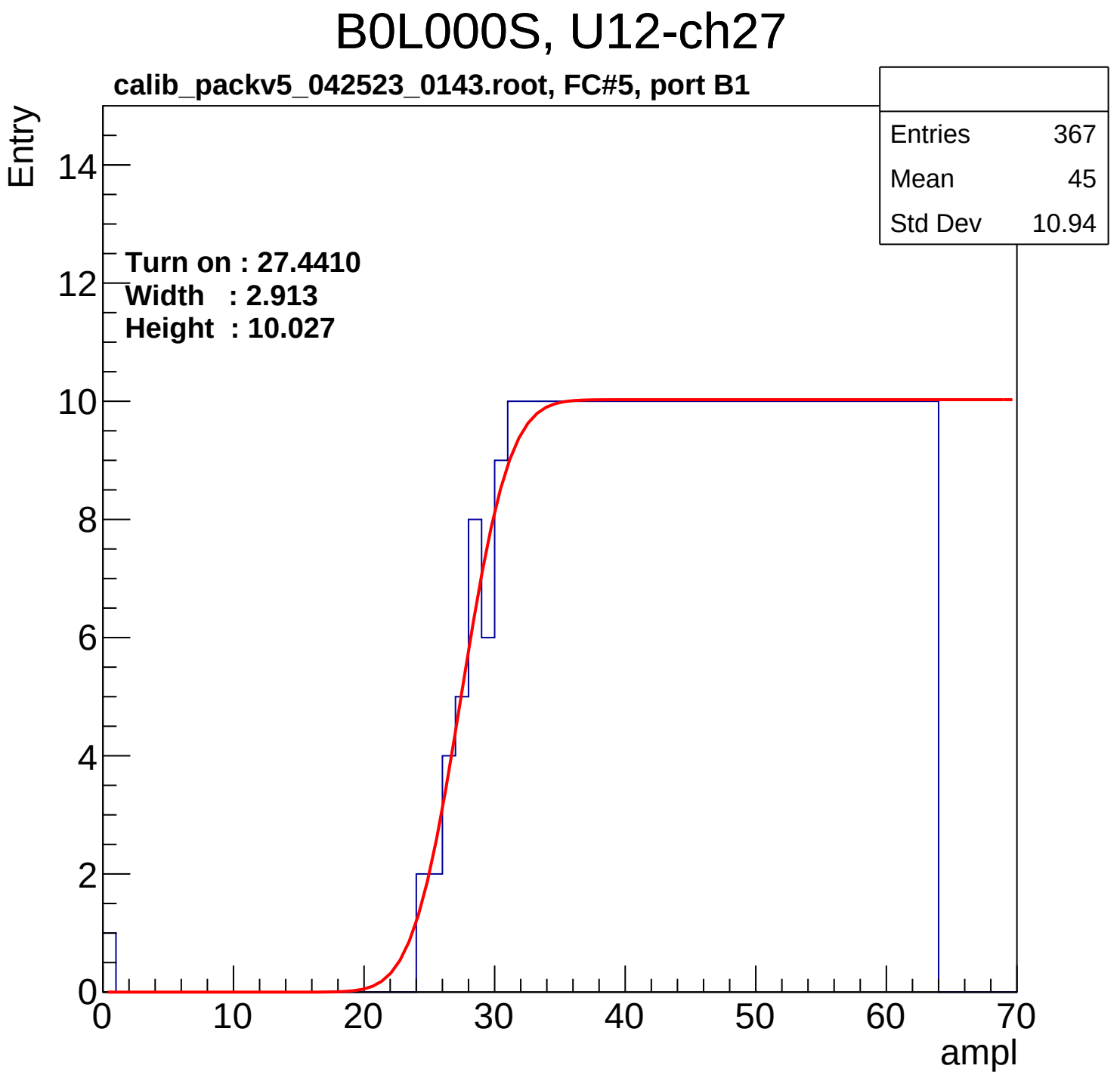
B0L000S, U12-ch27
calib_packv5_042523_0143.root, FC#5, port B1
Entries 367
Mean 45
Std Dev 10.94
Turn on : 27.4410
Width : 2.913
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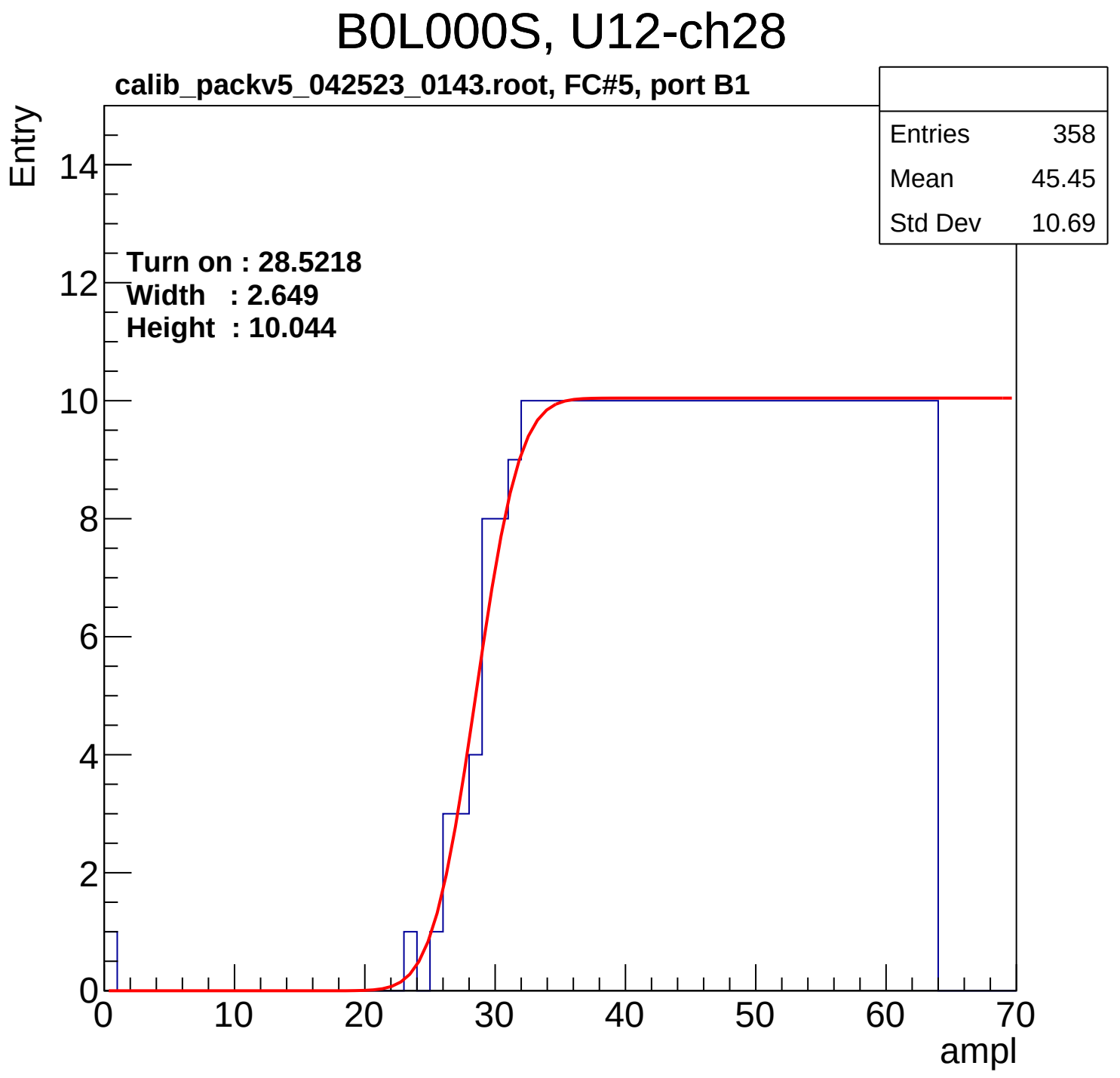
B0L000S, U12-ch28
calib_packv5_042523_0143.root, FC#5, port B1
Entries 358
Mean 45.45
Std Dev 10.69
Turn on : 28.5218
Width : 2.649
Height : 10.044
Entry
ampl
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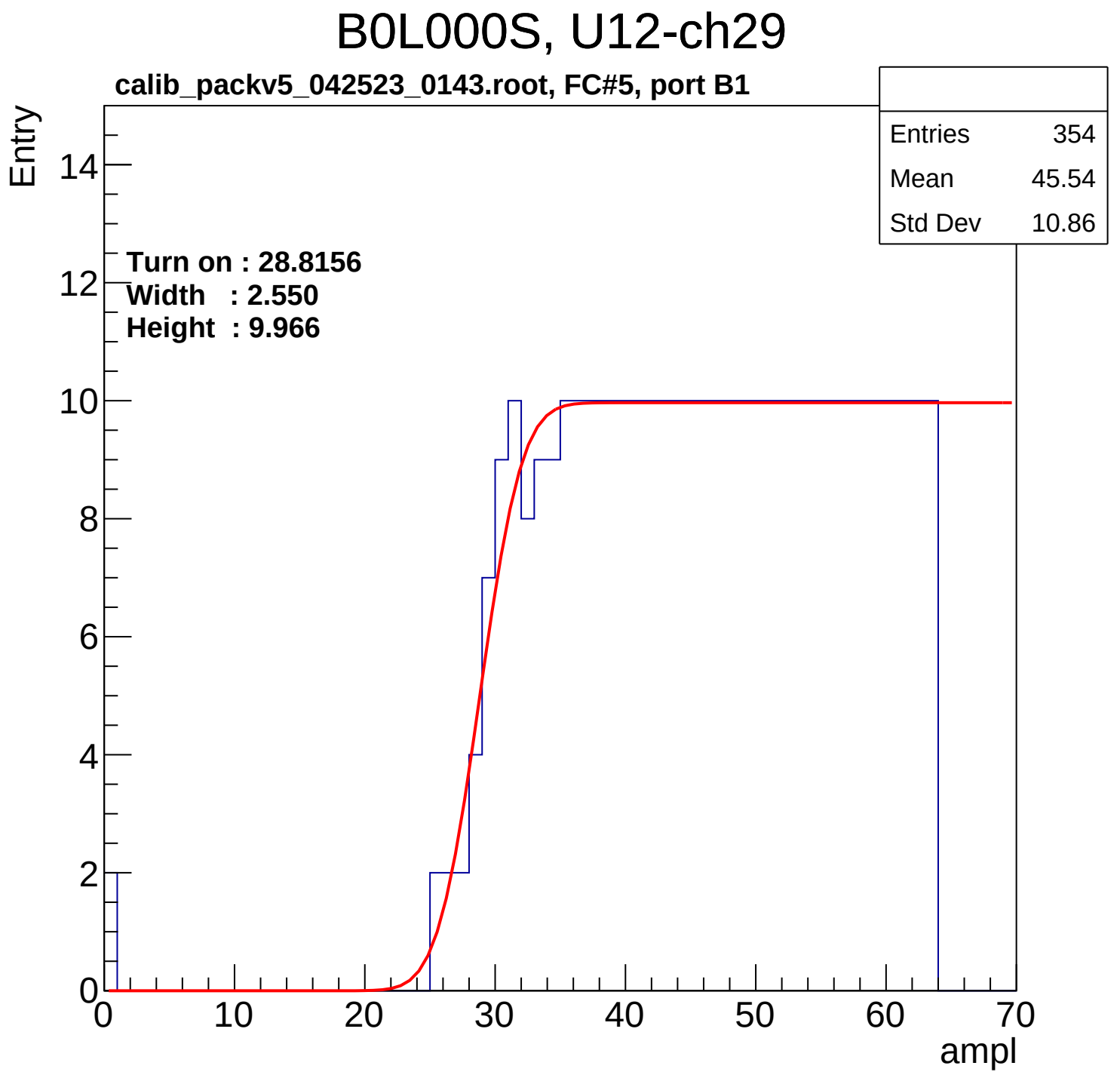
B0L000S, U12-ch29
calib_packv5_042523_0143.root, FC#5, port B1
Entries 354
Mean 45.54
Std Dev 10.86
Turn on : 28.8156
Width : 2.550
Height : 9.966
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ampl
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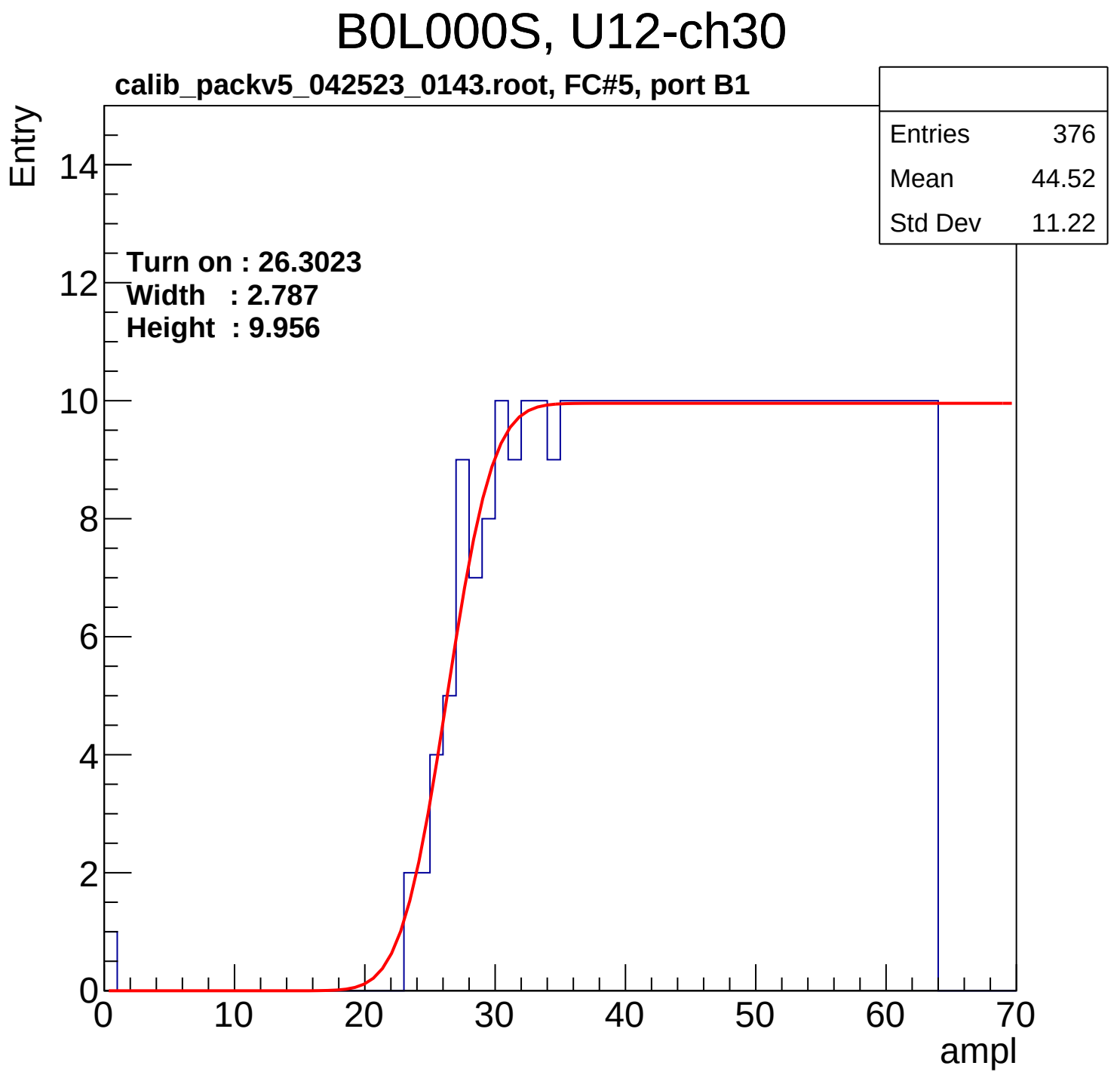
B0L000S, U12-ch30
calib_packv5_042523_0143.root, FC#5, port B1
Entries 376
Mean 44.52
Std Dev 11.22
Turn on : 26.3023
Width : 2.787
Height : 9.956
Entry
ampl
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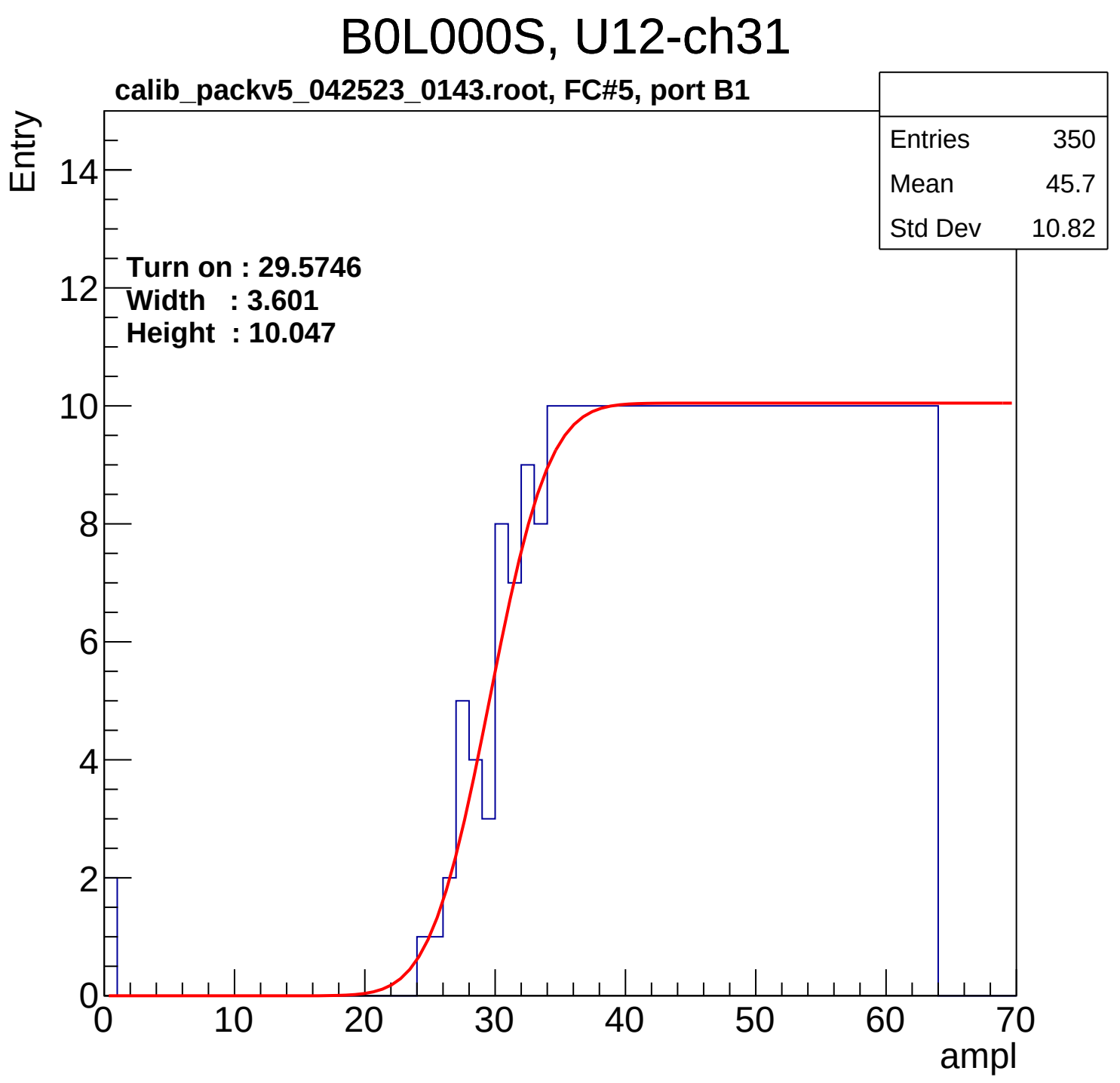
B0L000S, U12-ch31
calib_packv5_042523_0143.root, FC#5, port B1
Entries 350
Mean 45.7
Std Dev 10.82
Turn on : 29.5746
Width : 3.601
Height : 10.047
Entry
ampl
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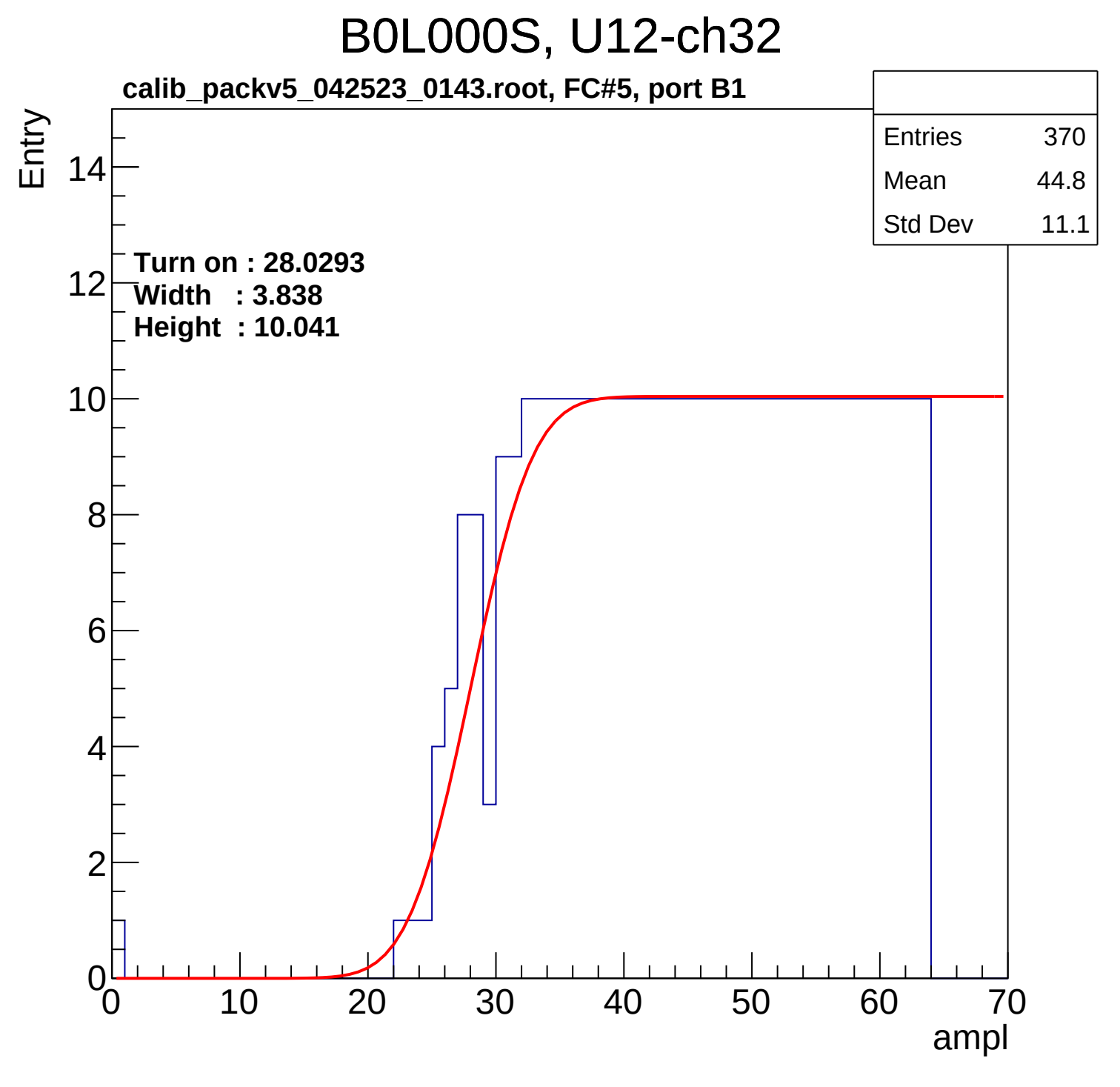
B0L000S, U12-ch32
calib_packv5_042523_0143.root, FC#5, port B1
Entries 370
Mean 44.8
Std Dev 11.1
Turn on : 28.0293
Width : 3.838
Height : 10.041
Entry
ampl
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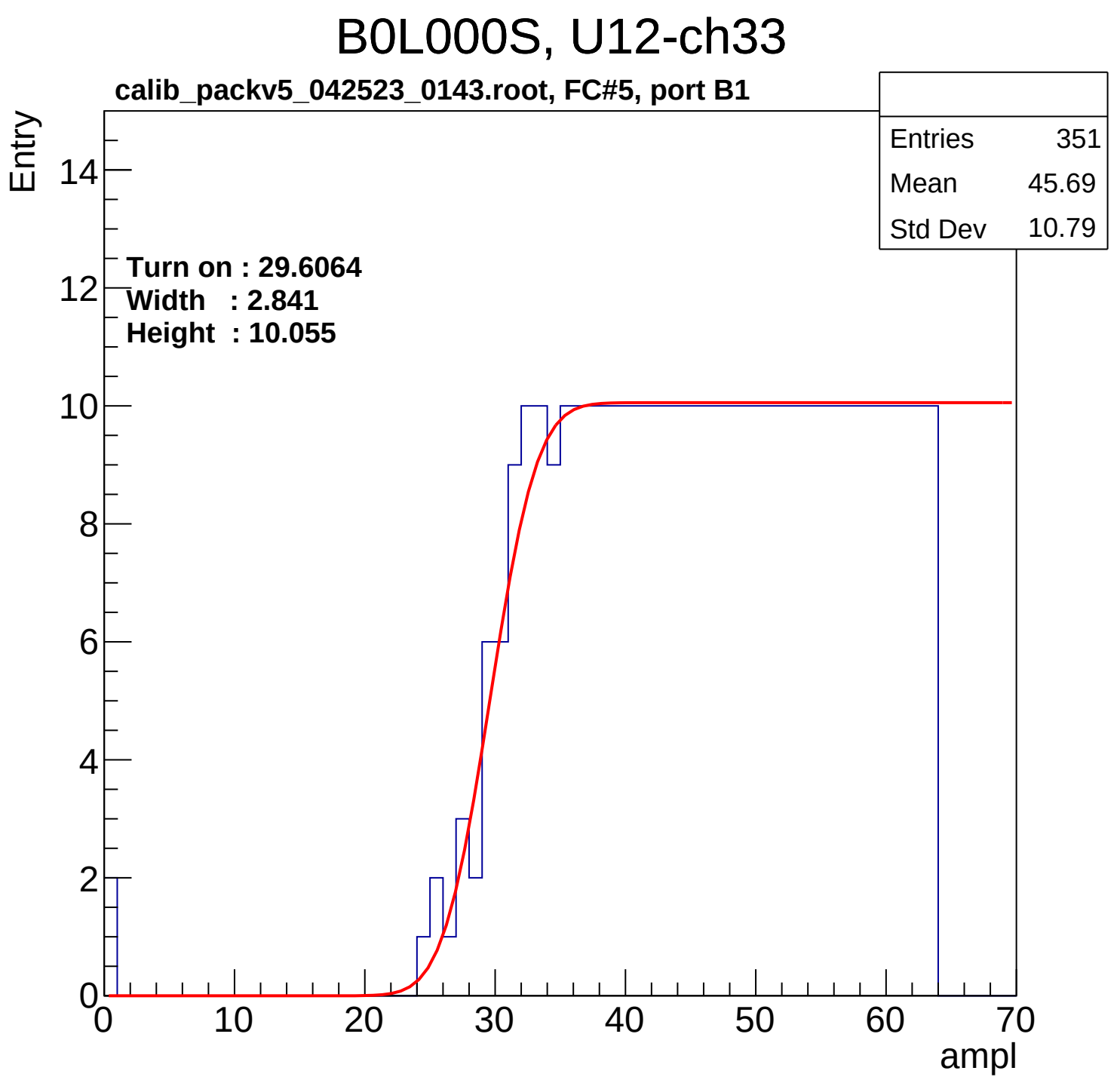
B0L000S, U12-ch33
calib_packv5_042523_0143.root, FC#5, port B1
Entries 351
Mean 45.69
Std Dev 10.79
Turn on : 29.6064
Width : 2.841
Height : 10.055
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ampl
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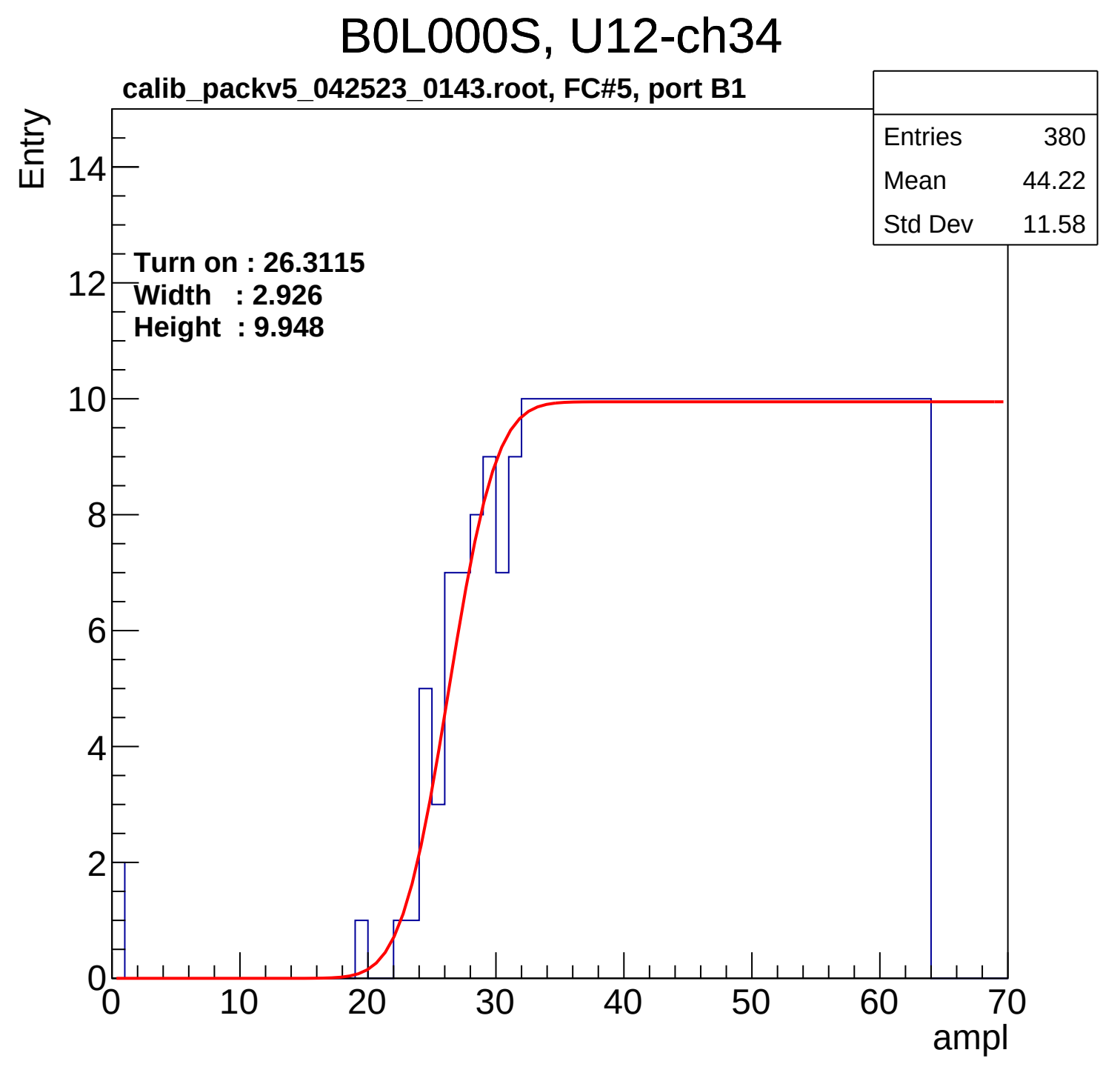
B0L000S, U12-ch34
calib_packv5_042523_0143.root, FC#5, port B1
Entries 380
Mean 44.22
Std Dev 11.58
Turn on : 26.3115
Width : 2.926
Height : 9.948
Entry
ampl
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2
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6
8
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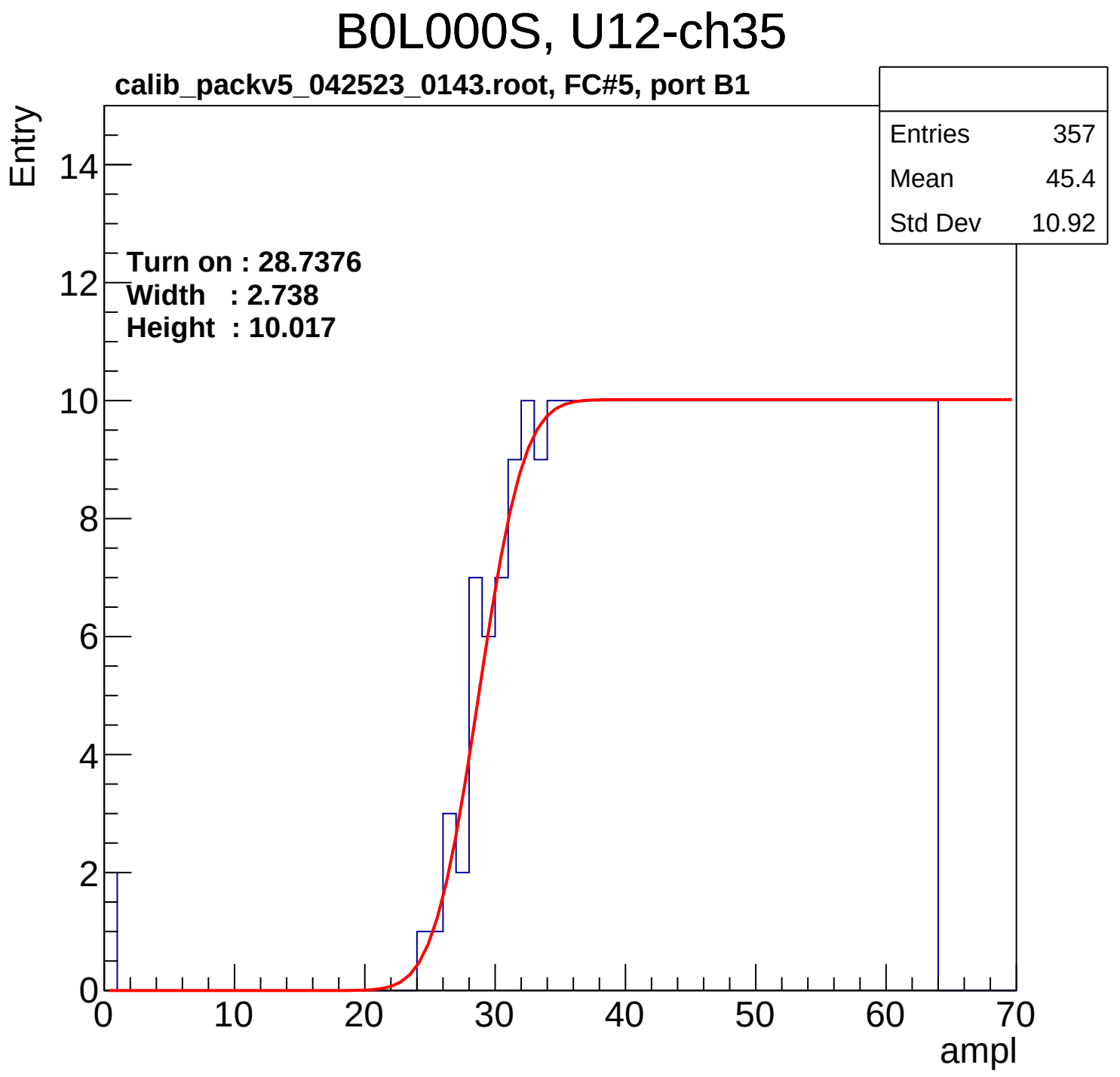
B0L000S, U12-ch35
calib_packv5_042523_0143.root, FC#5, port B1
Entries 357
Mean 45.4
Std Dev 10.92
Turn on : 28.7376
Width : 2.738
Height : 10.017
Entry
ampl
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2
4
6
8
10
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0
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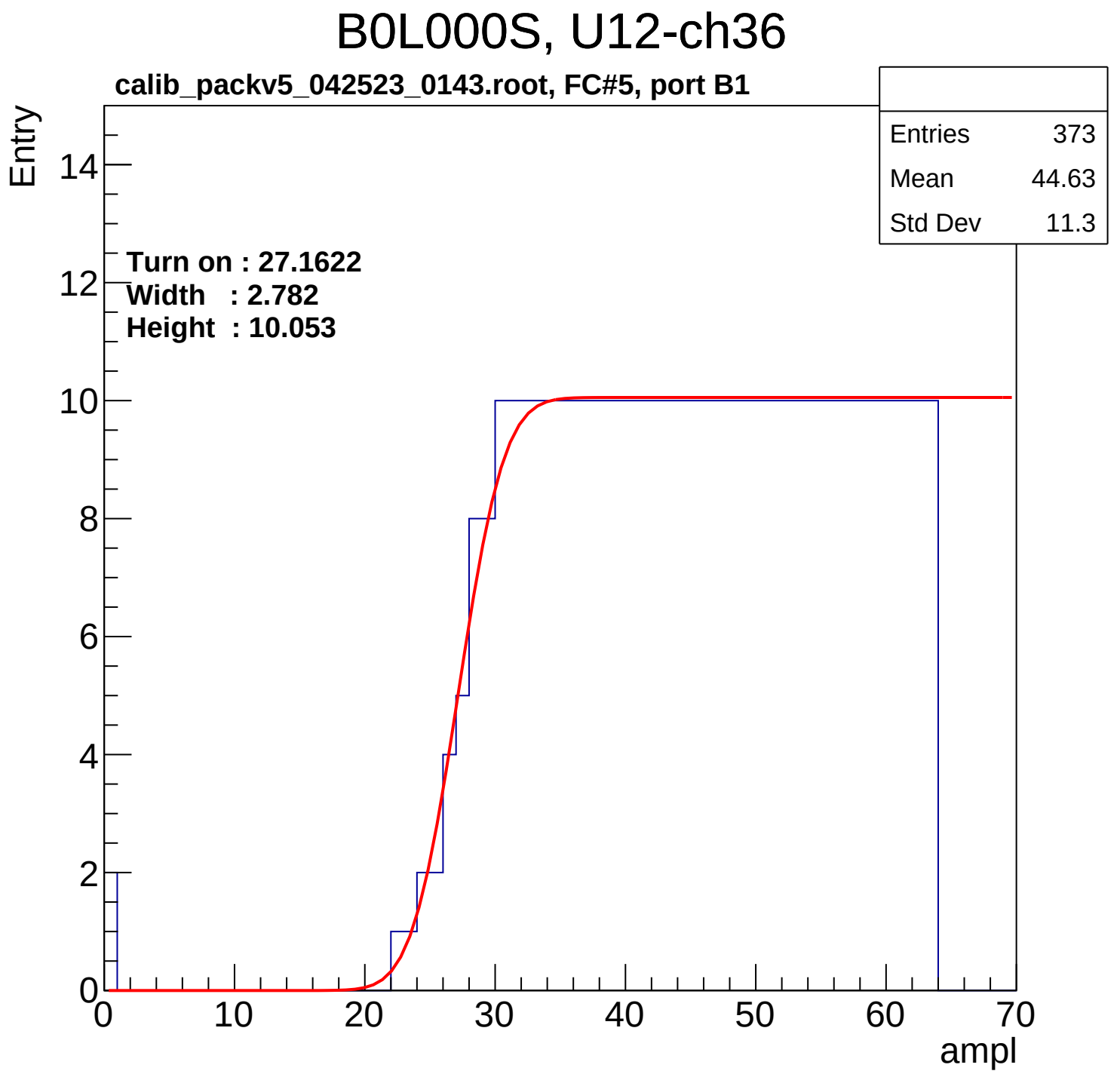
B0L000S, U12-ch36
calib_packv5_042523_0143.root, FC#5, port B1
Entries 373
Mean 44.63
Std Dev 11.3
Turn on : 27.1622
Width : 2.782
Height : 10.053
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
50
60
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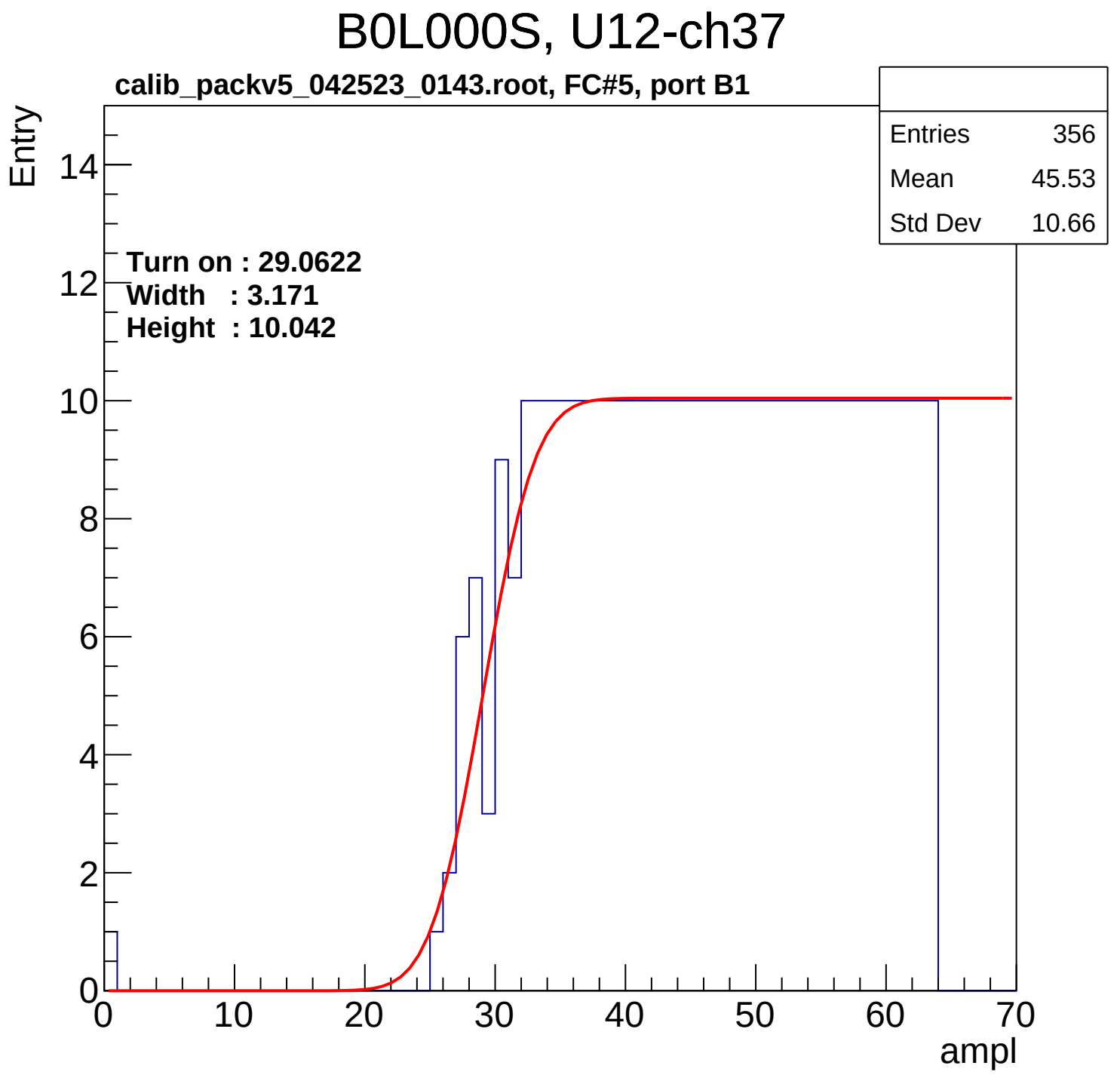
B0L000S, U12-ch37
calib_packv5_042523_0143.root, FC#5, port B1
Entries 356
Mean 45.53
Std Dev 10.66
Turn on : 29.0622
Width : 3.171
Height : 10.042
Entry
ampl
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4
6
8
10
12
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60
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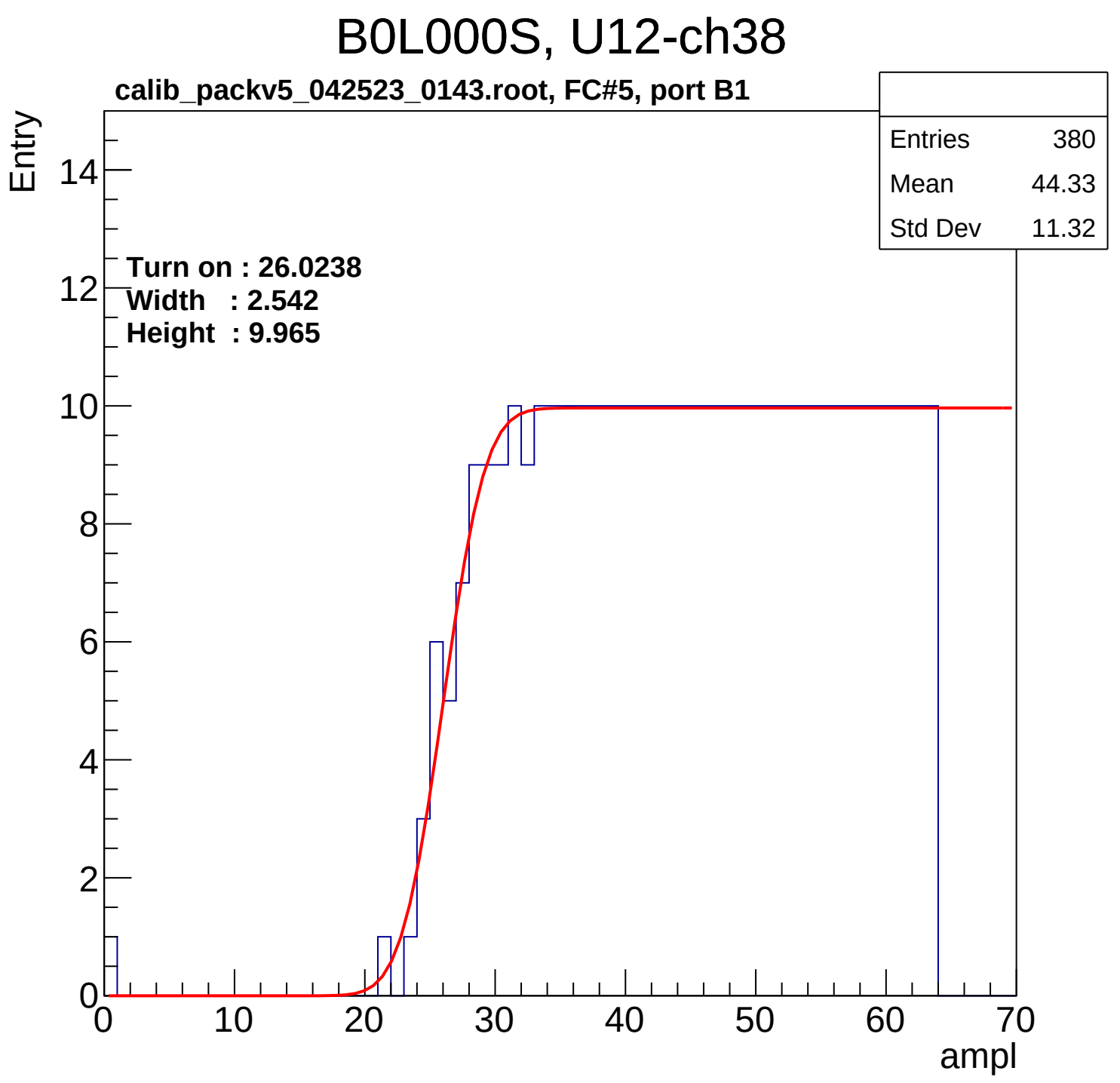
B0L000S, U12-ch38
calib_packv5_042523_0143.root, FC#5, port B1
Entries 380
Mean 44.33
Std Dev 11.32
Turn on : 26.0238
Width : 2.542
Height : 9.965
Entry
ampl
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6
8
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60
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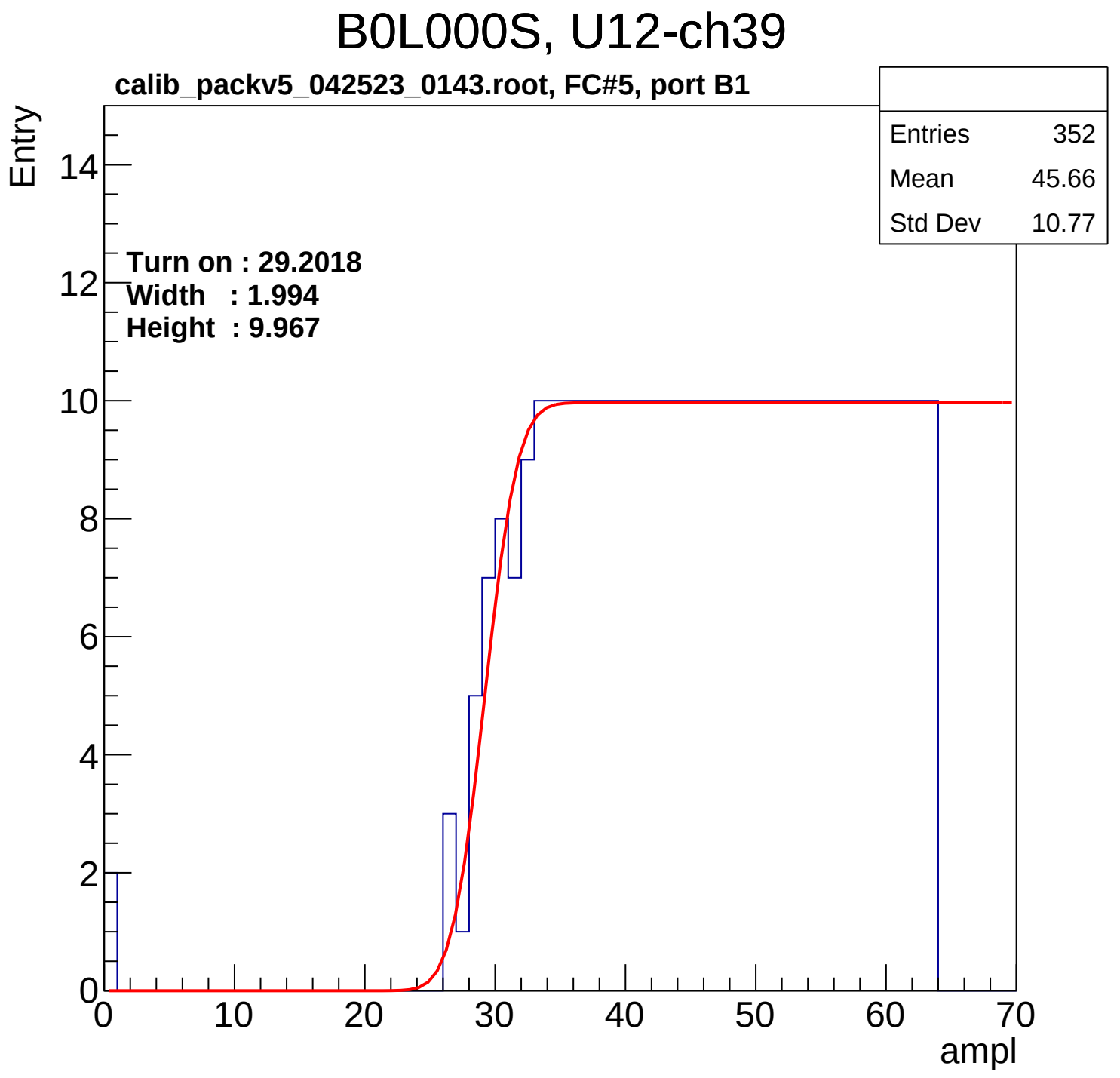
B0L000S, U12-ch39
calib_packv5_042523_0143.root, FC#5, port B1
Entries 352
Mean 45.66
Std Dev 10.77
Turn on : 29.2018
Width : 1.994
Height : 9.967
Entry
ampl
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6
8
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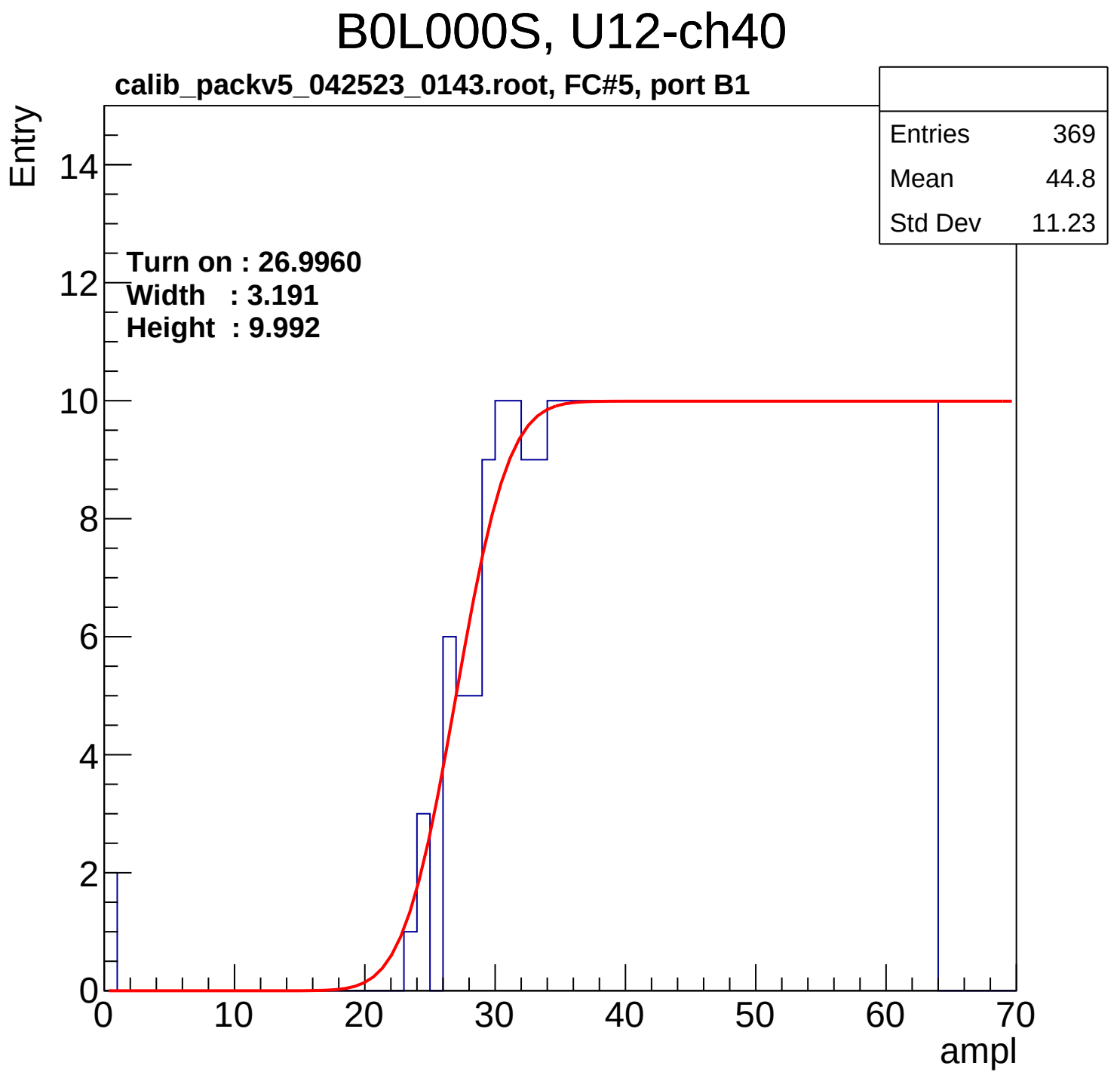
B0L000S, U12-ch40
calib_packv5_042523_0143.root, FC#5, port B1
Entries 369
Mean 44.8
Std Dev 11.23
Turn on : 26.9960
Width : 3.191
Height : 9.992
Entry
ampl
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8
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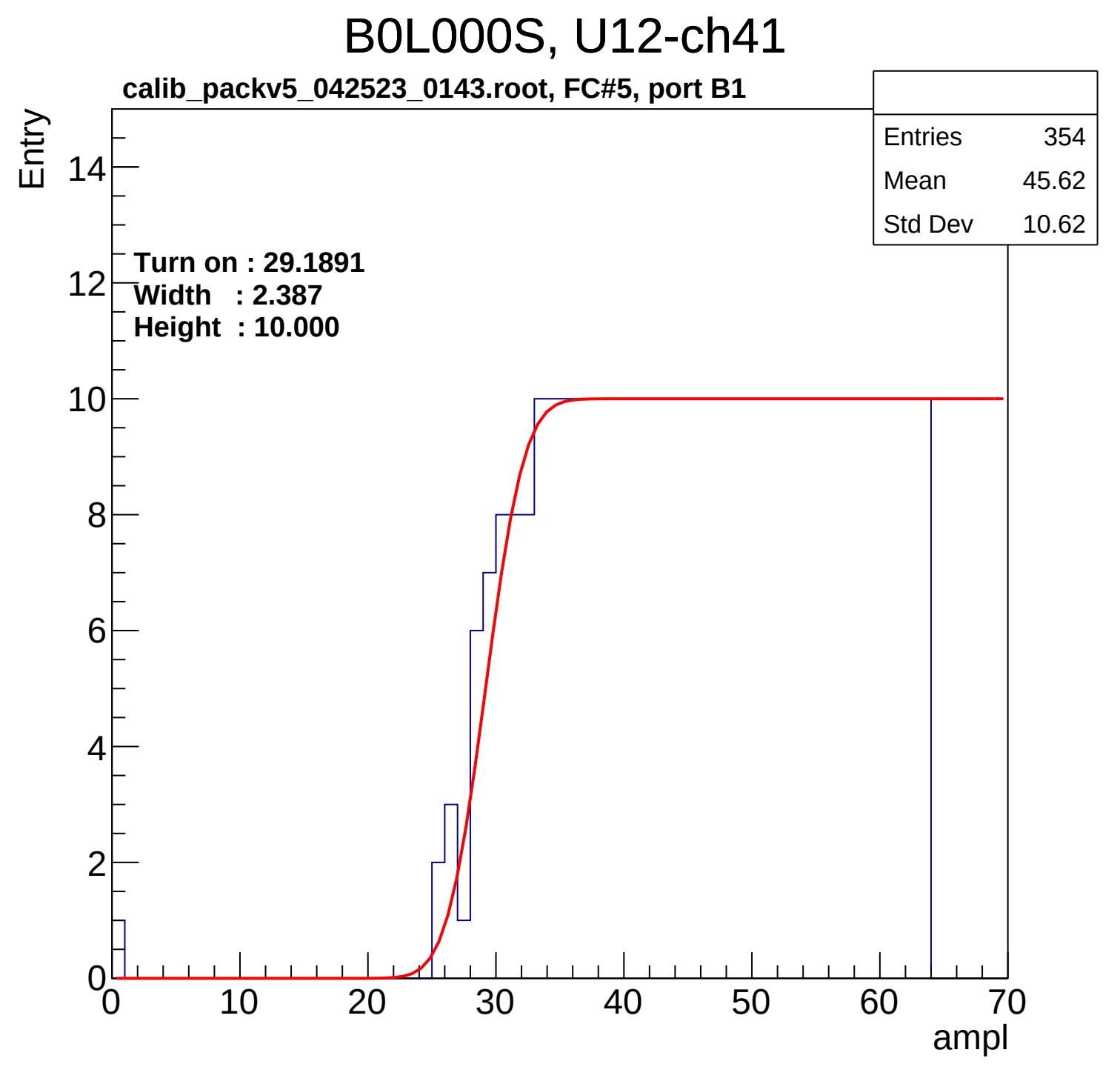
B0L000S, U12-ch41
calib_packv5_042523_0143.root, FC#5, port B1
Entries 354
Mean 45.62
Std Dev 10.62
Turn on : 29.1891
Width : 2.387
Height : 10.000
Entry
ampl
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6
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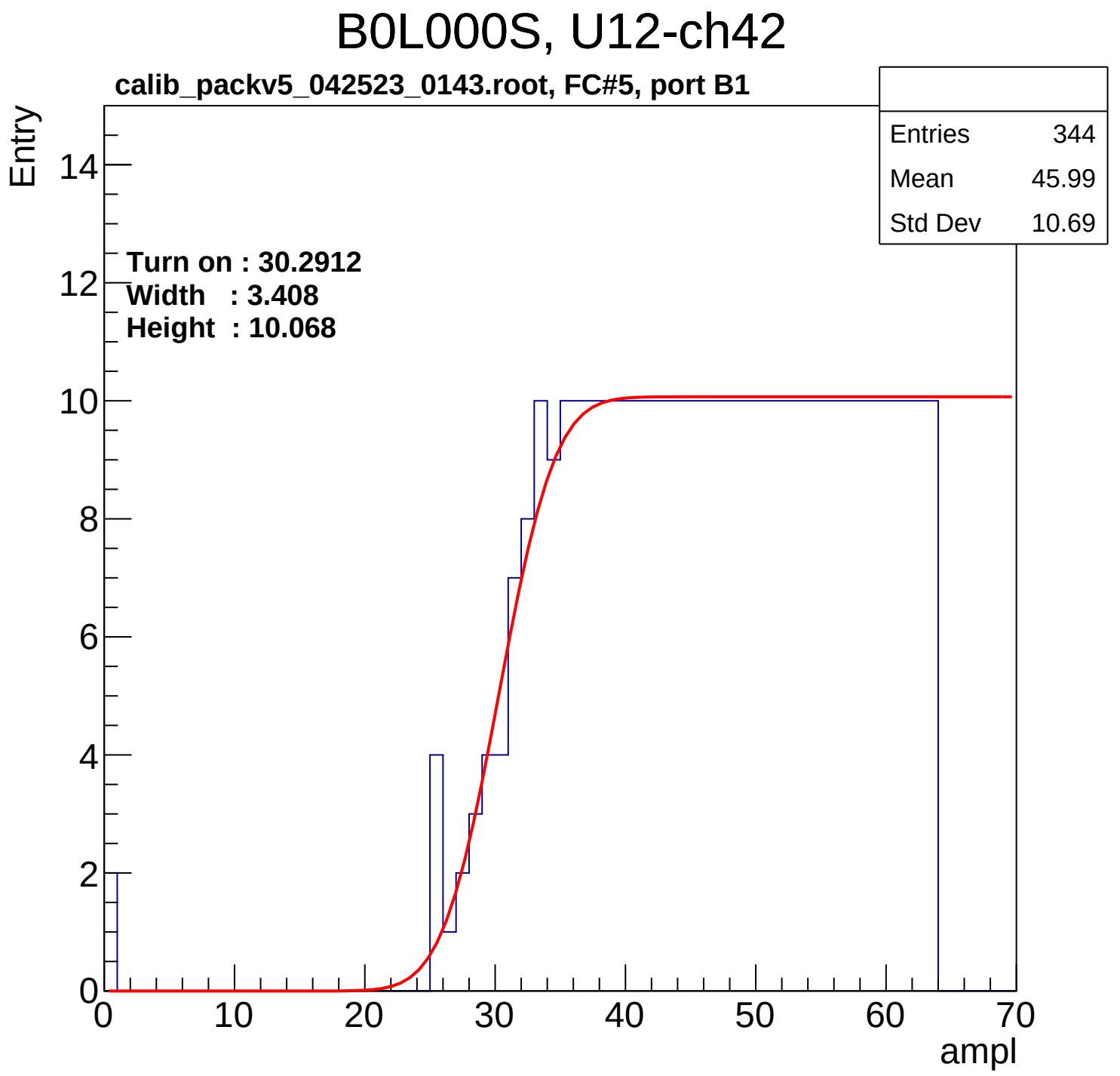
B0L000S, U12-ch42
calib_packv5_042523_0143.root, FC#5, port B1
Entries 344
Mean 45.99
Std Dev 10.69
Turn on : 30.2912
Width : 3.408
Height : 10.068
Entry
ampl
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4
6
8
10
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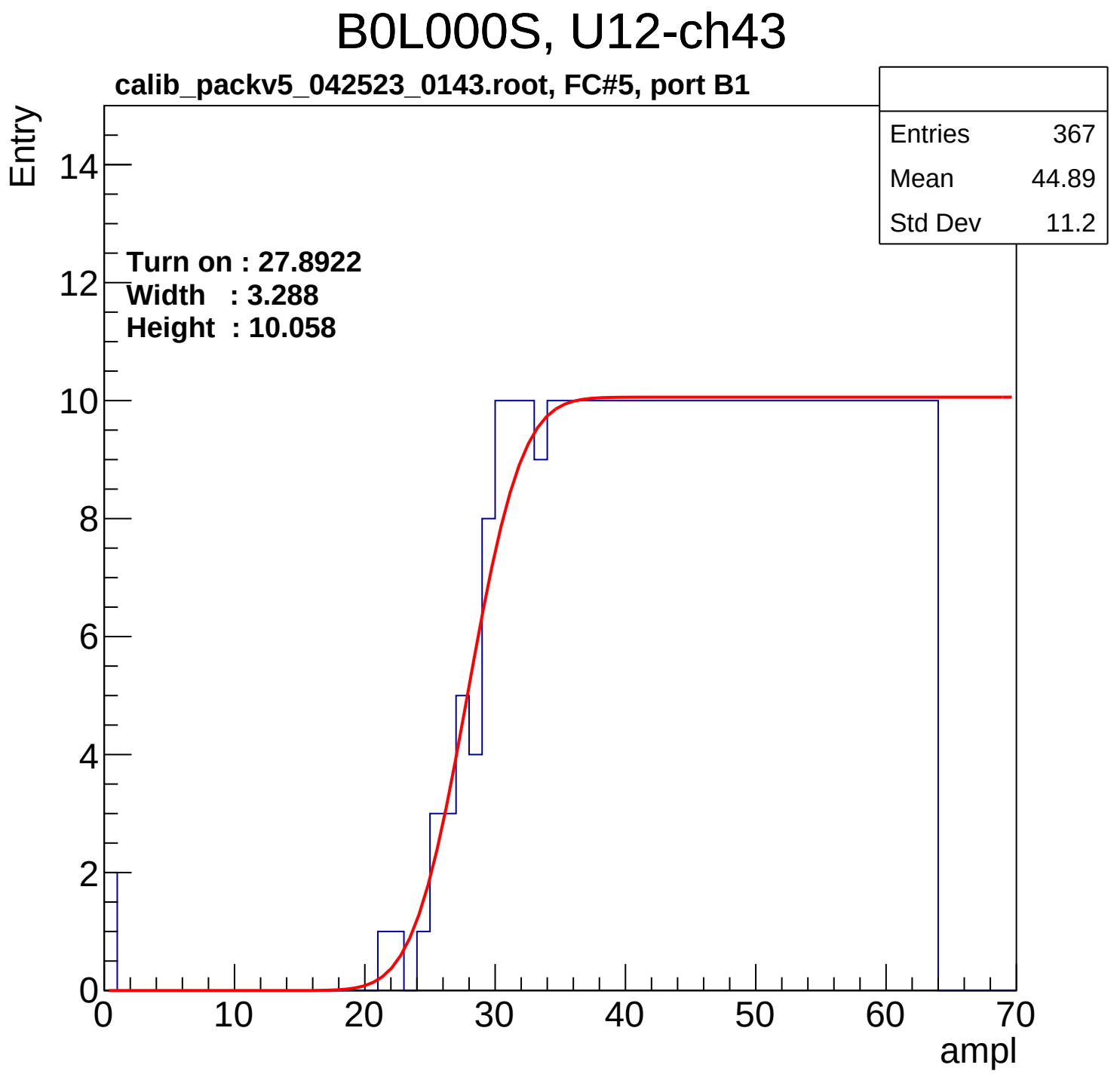
B0L000S, U12-ch43
calib_packv5_042523_0143.root, FC#5, port B1
Entries 367
Mean 44.89
Std Dev 11.2
Turn on : 27.8922
Width : 3.288
Height : 10.058
Entry
ampl
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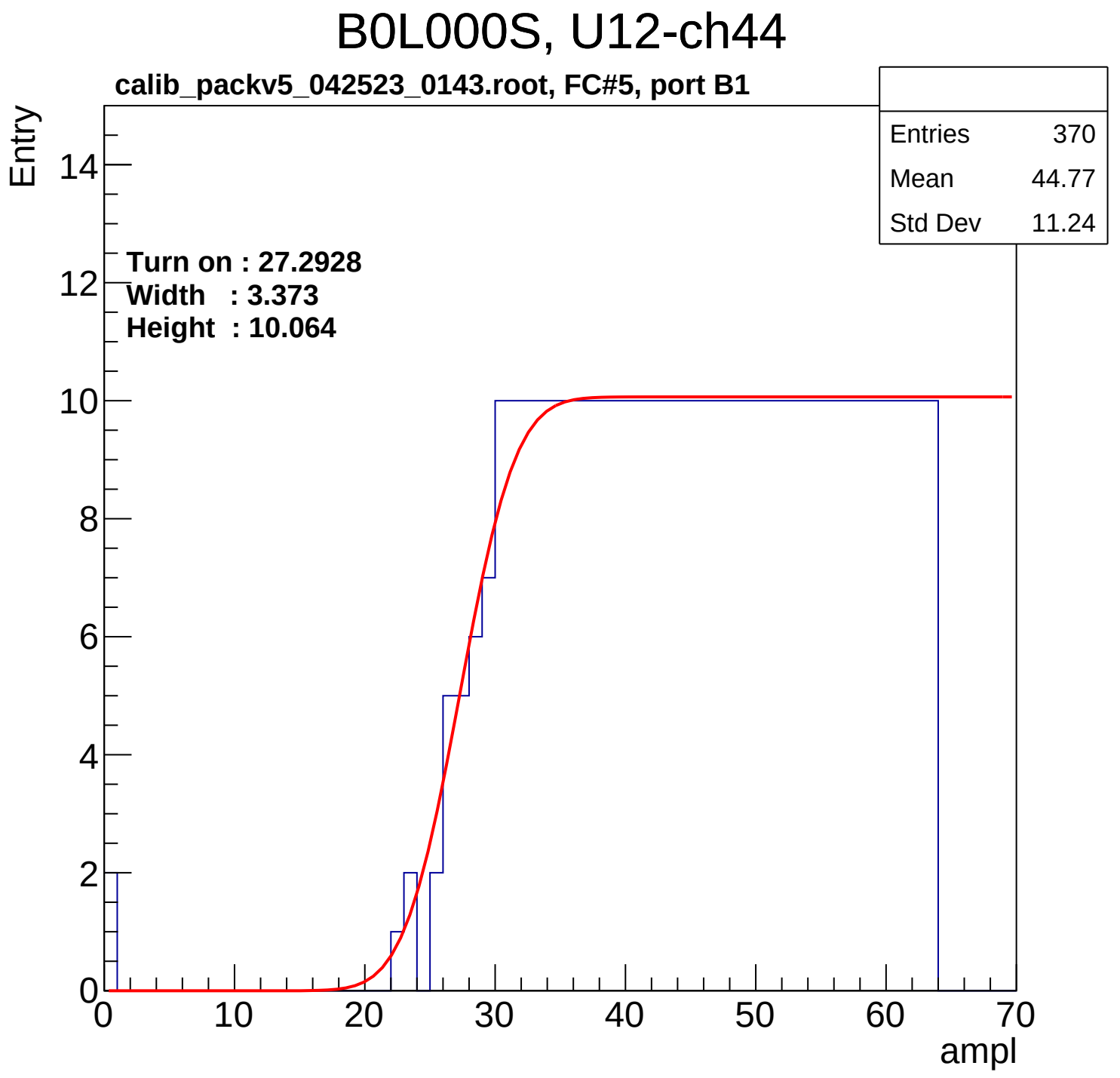
B0L000S, U12-ch44
calib_packv5_042523_0143.root, FC#5, port B1
Entries 370
Mean 44.77
Std Dev 11.24
Turn on : 27.2928
Width : 3.373
Height : 10.064
Entry
ampl
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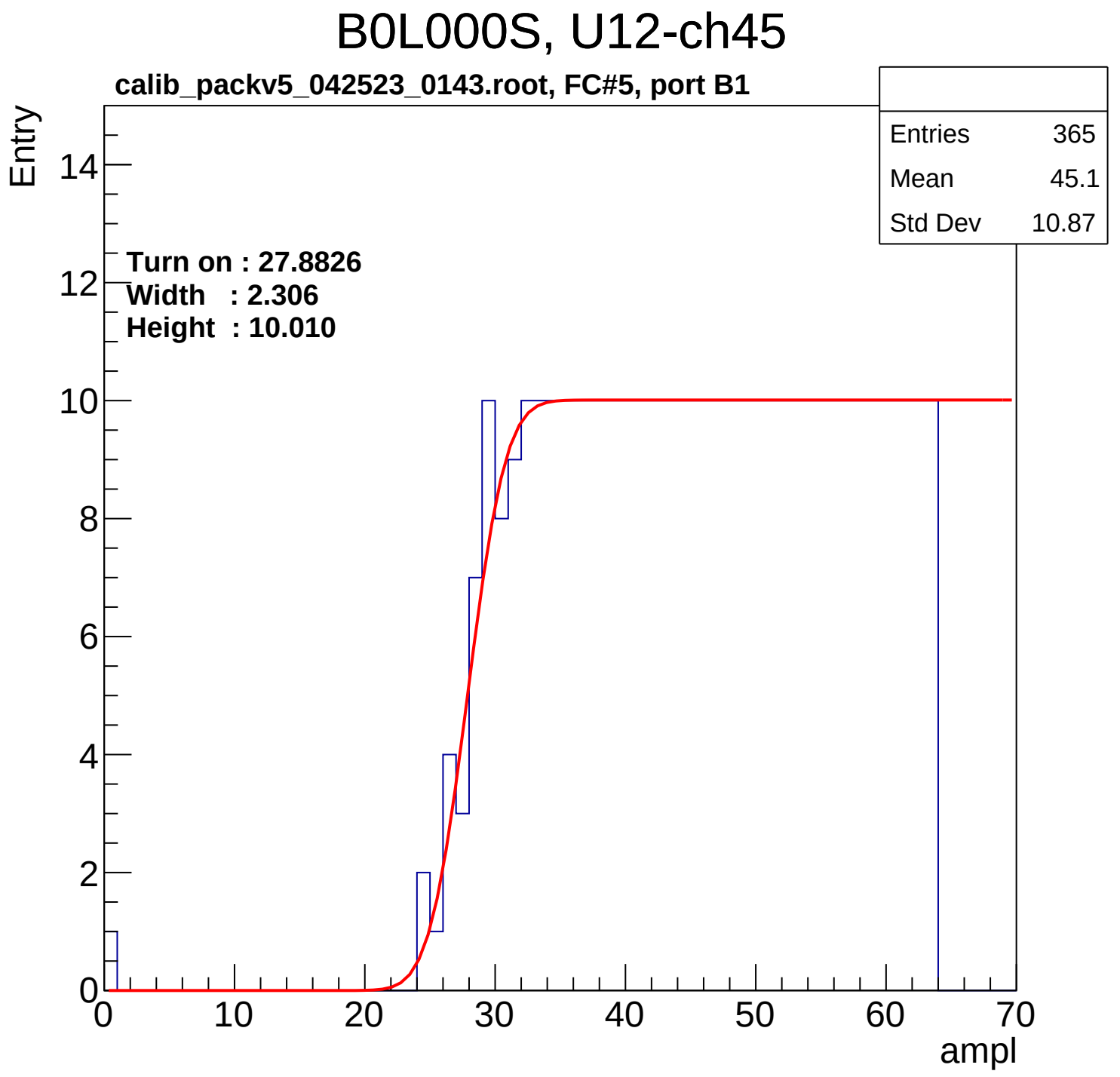
B0L000S, U12-ch45
calib_packv5_042523_0143.root, FC#5, port B1
Entries 365
Mean 45.1
Std Dev 10.87
Turn on : 27.8826
Width : 2.306
Height : 10.010
Entry
ampl
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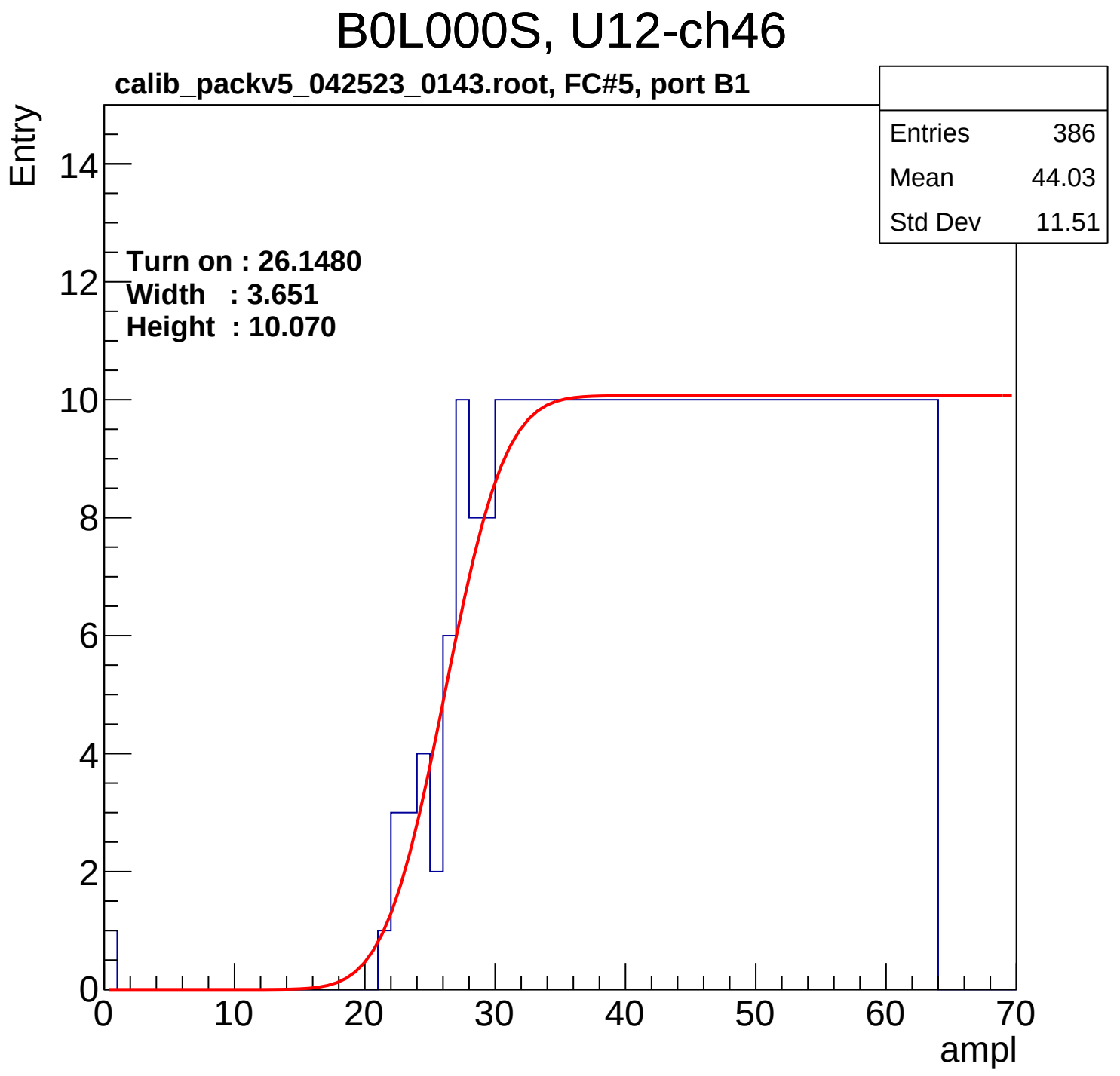
B0L000S, U12-ch46
calib_packv5_042523_0143.root, FC#5, port B1
Entries 386
Mean 44.03
Std Dev 11.51
Turn on : 26.1480
Width : 3.651
Height : 10.070
Entry
ampl
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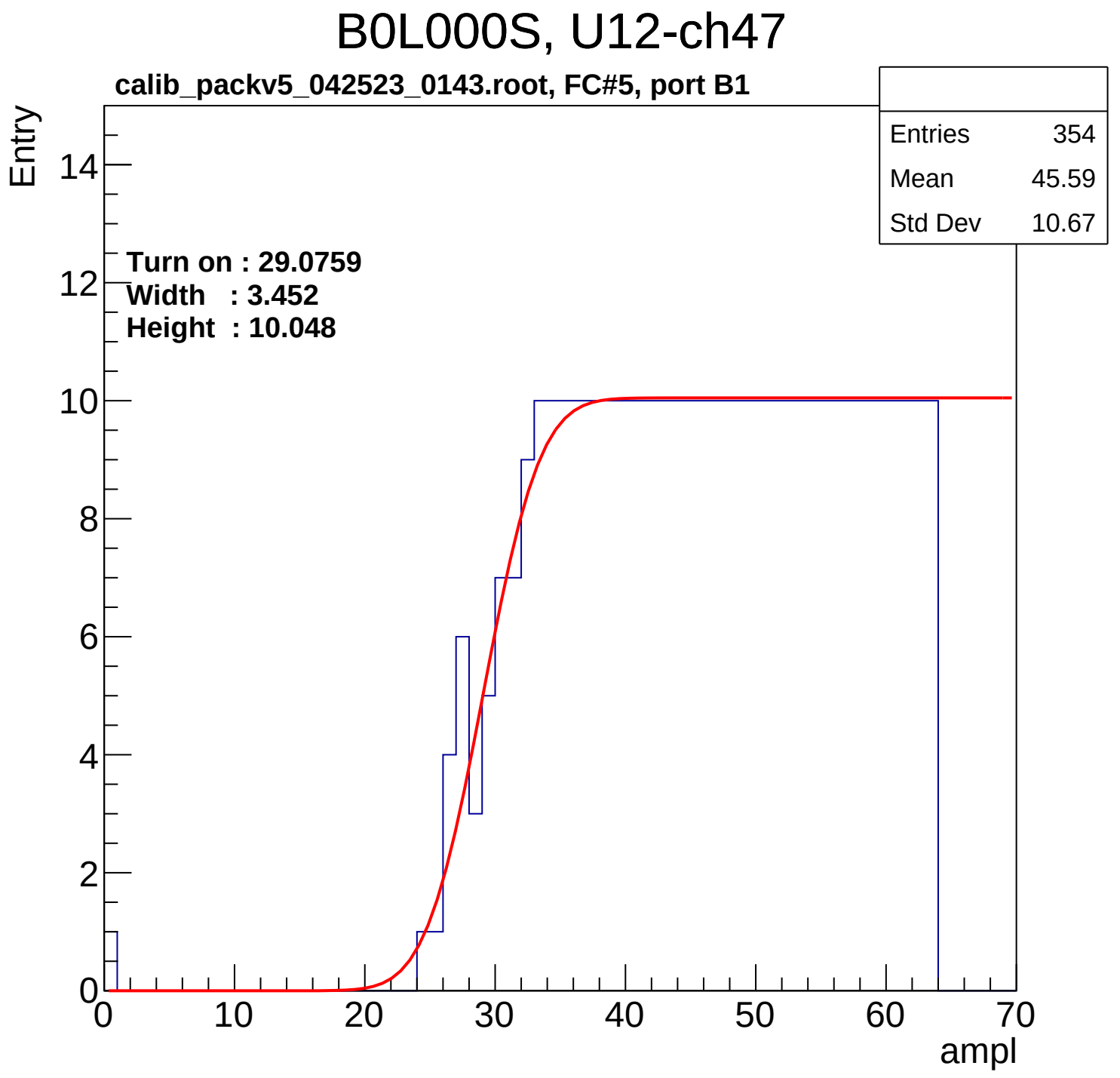
B0L000S, U12-ch47
calib_packv5_042523_0143.root, FC#5, port B1
Entries 354
Mean 45.59
Std Dev 10.67
Turn on : 29.0759
Width : 3.452
Height : 10.048
Entry
ampl
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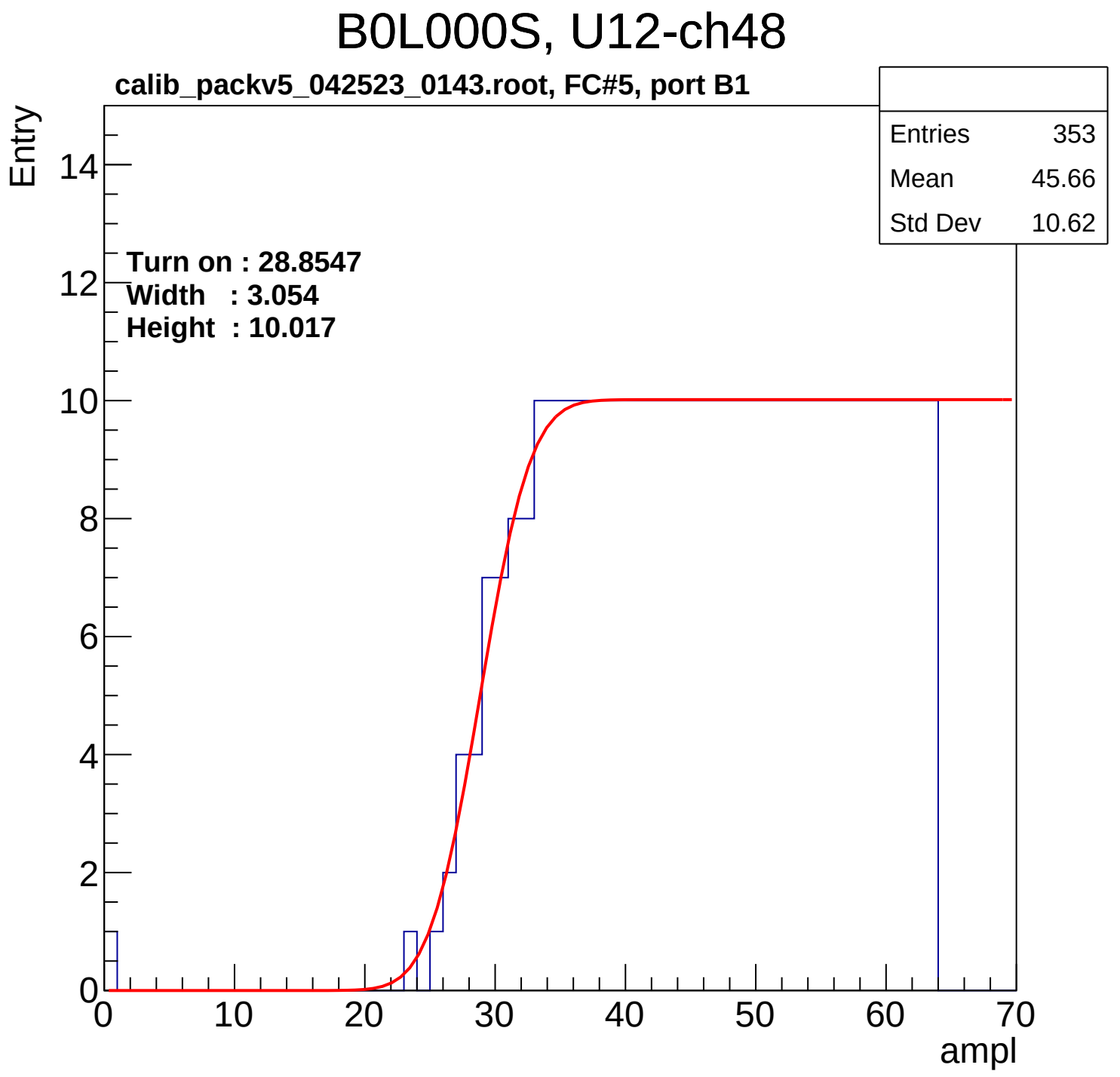
B0L000S, U12-ch48
calib_packv5_042523_0143.root, FC#5, port B1
Entries 353
Mean 45.66
Std Dev 10.62
Turn on : 28.8547
Width : 3.054
Height : 10.017
Entry
ampl
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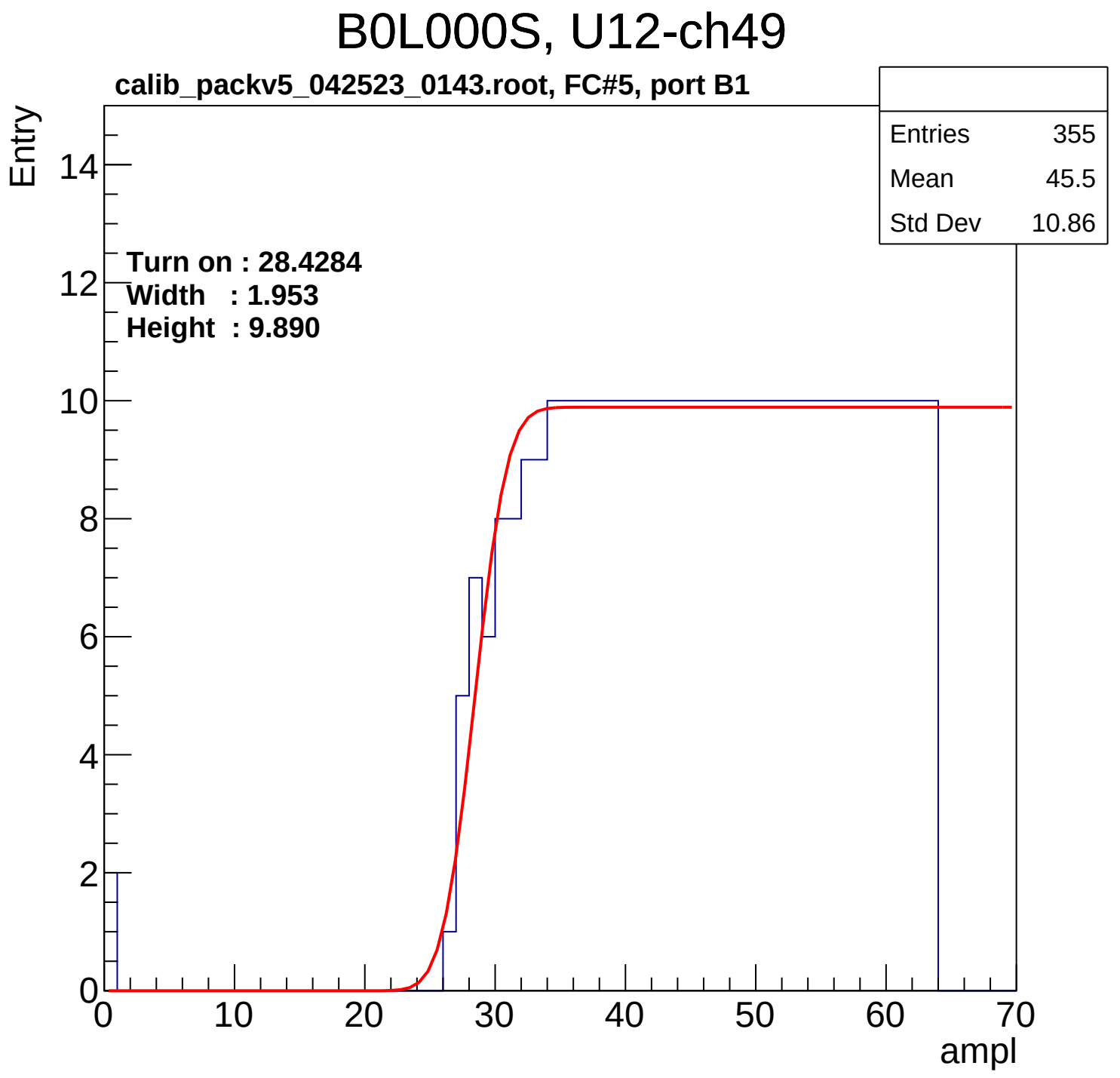
B0L000S, U12-ch49
calib_packv5_042523_0143.root, FC#5, port B1
Entries 355
Mean 45.5
Std Dev 10.86
Turn on : 28.4284
Width : 1.953
Height : 9.890
Entry
ampl
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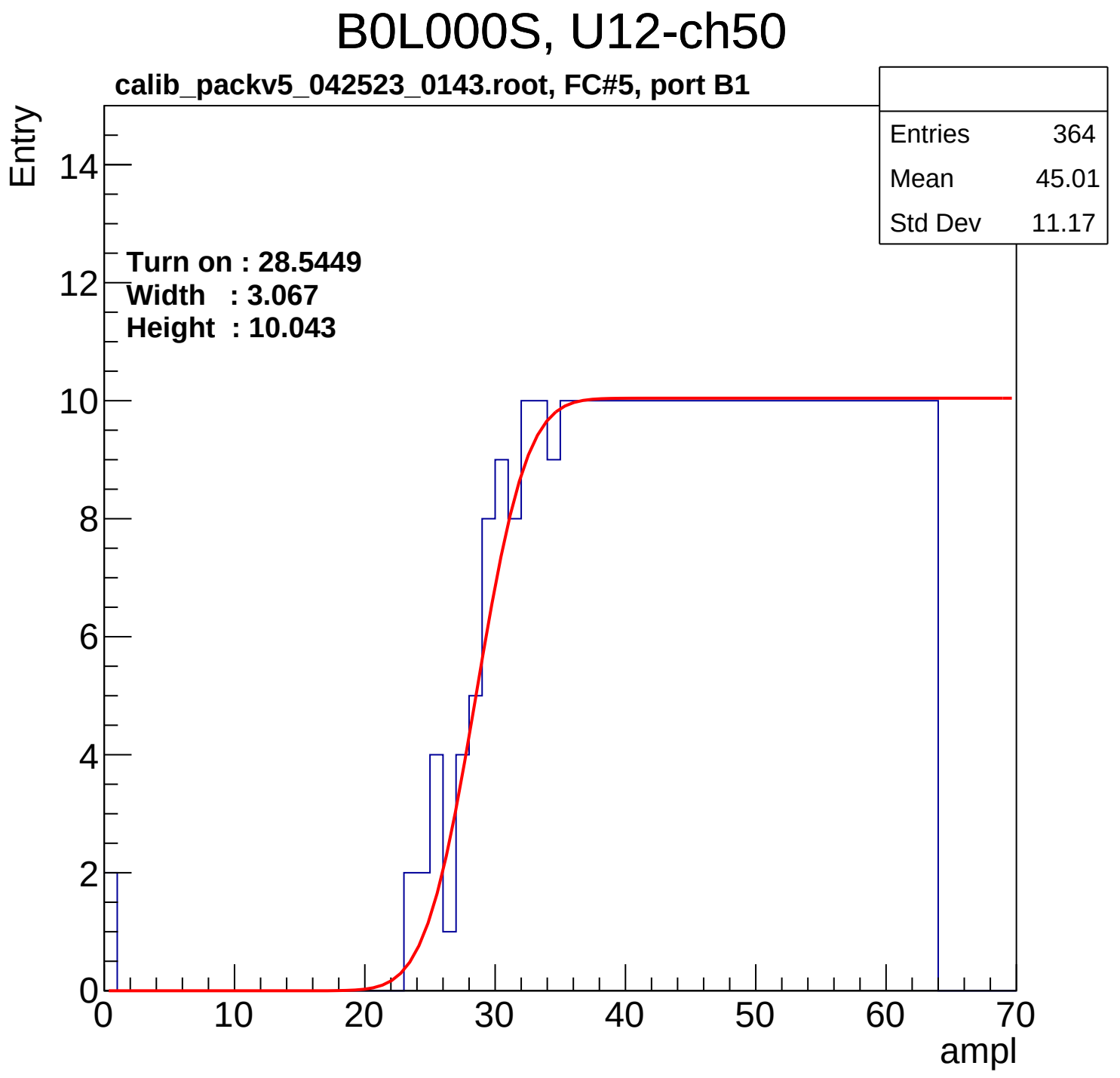
B0L000S, U12-ch50
calib_packv5_042523_0143.root, FC#5, port B1
Entries 364
Mean 45.01
Std Dev 11.17
Turn on : 28.5449
Width : 3.067
Height : 10.043
Entry
ampl
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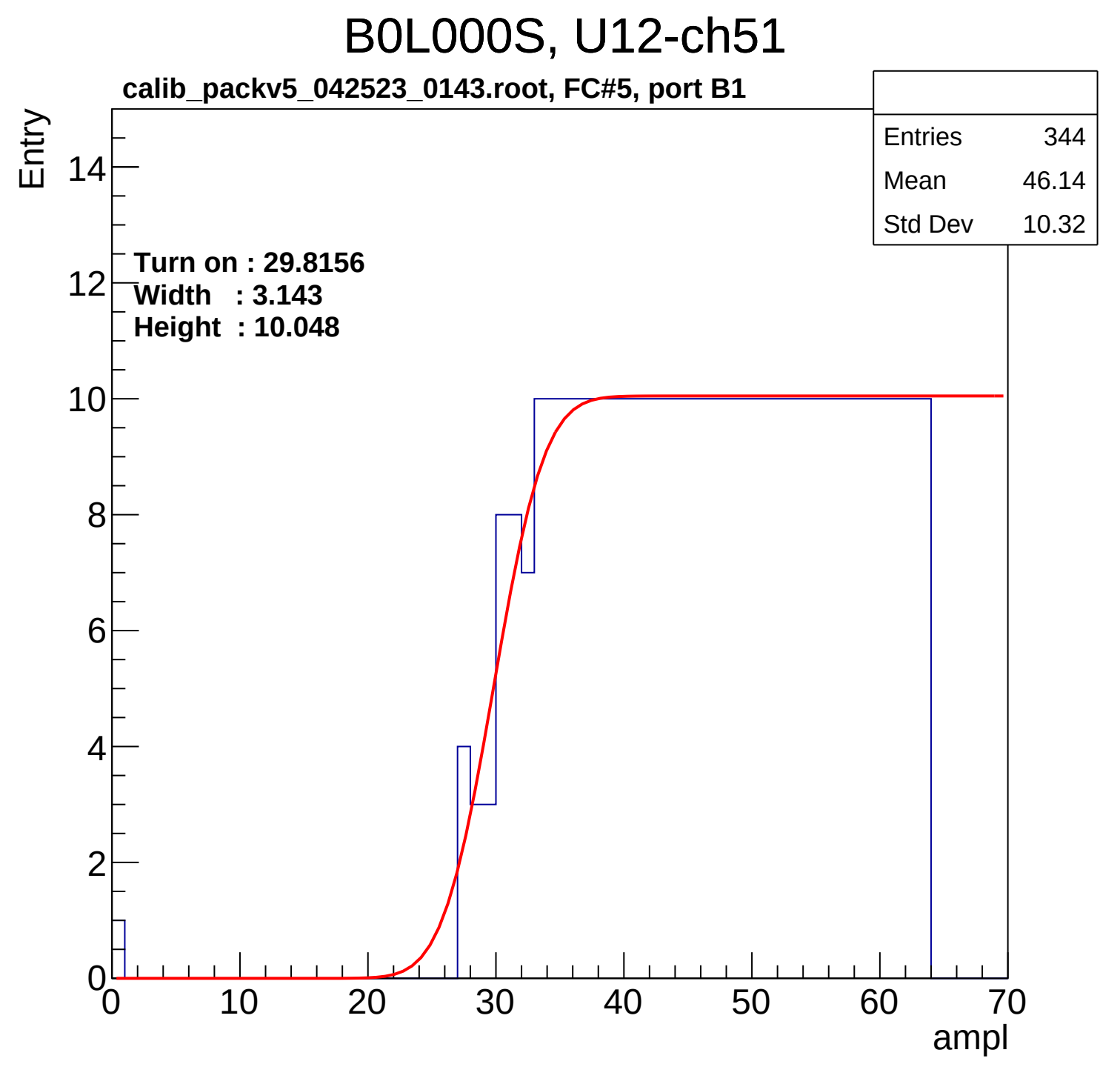
B0L000S, U12-ch51
calib_packv5_042523_0143.root, FC#5, port B1
Entries 344
Mean 46.14
Std Dev 10.32
Turn on : 29.8156
Width : 3.143
Height : 10.048
Entry
ampl
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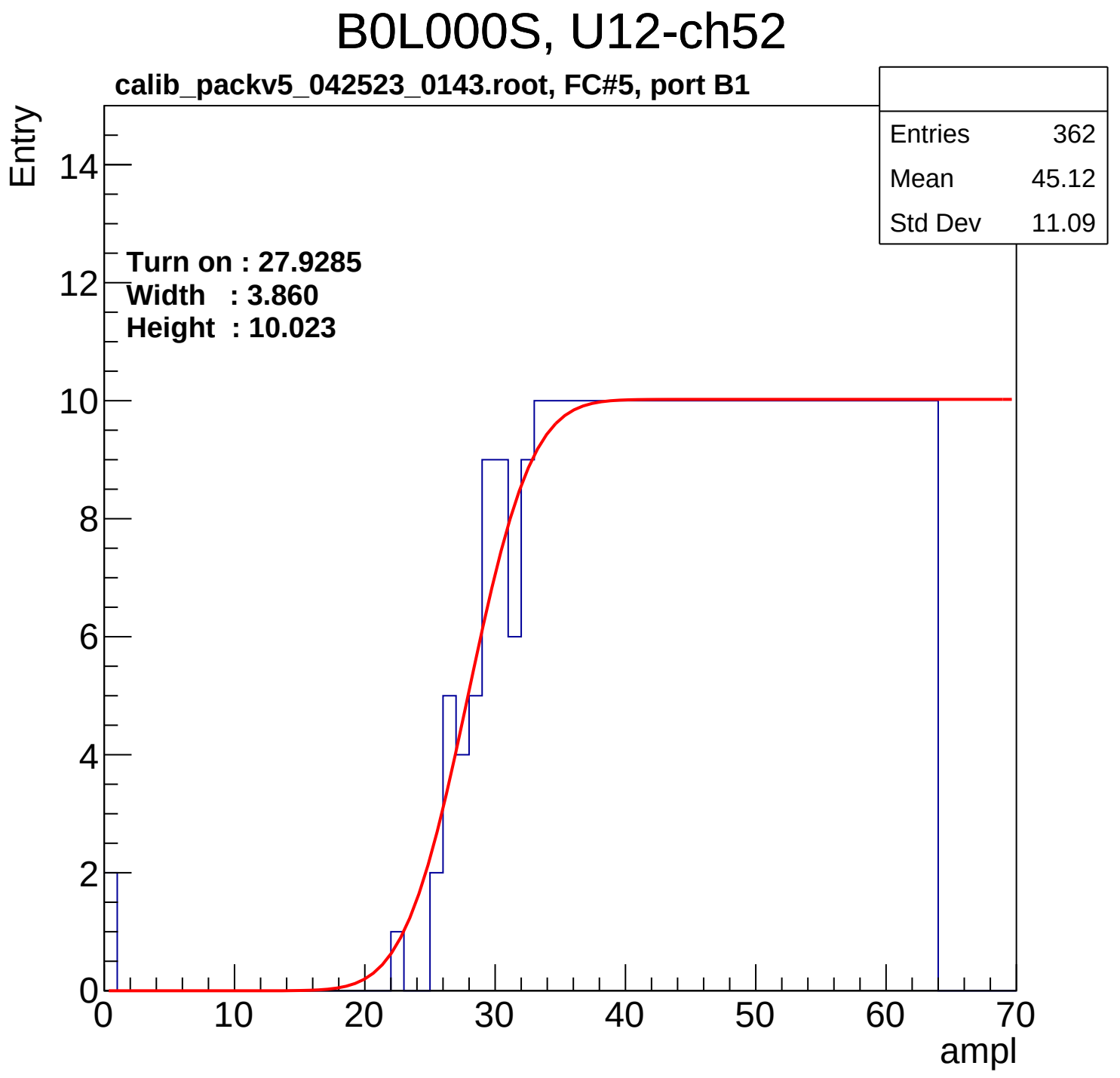
B0L000S, U12-ch52
calib_packv5_042523_0143.root, FC#5, port B1
Entries 362
Mean 45.12
Std Dev 11.09
Turn on : 27.9285
Width : 3.860
Height : 10.023
Entry
ampl
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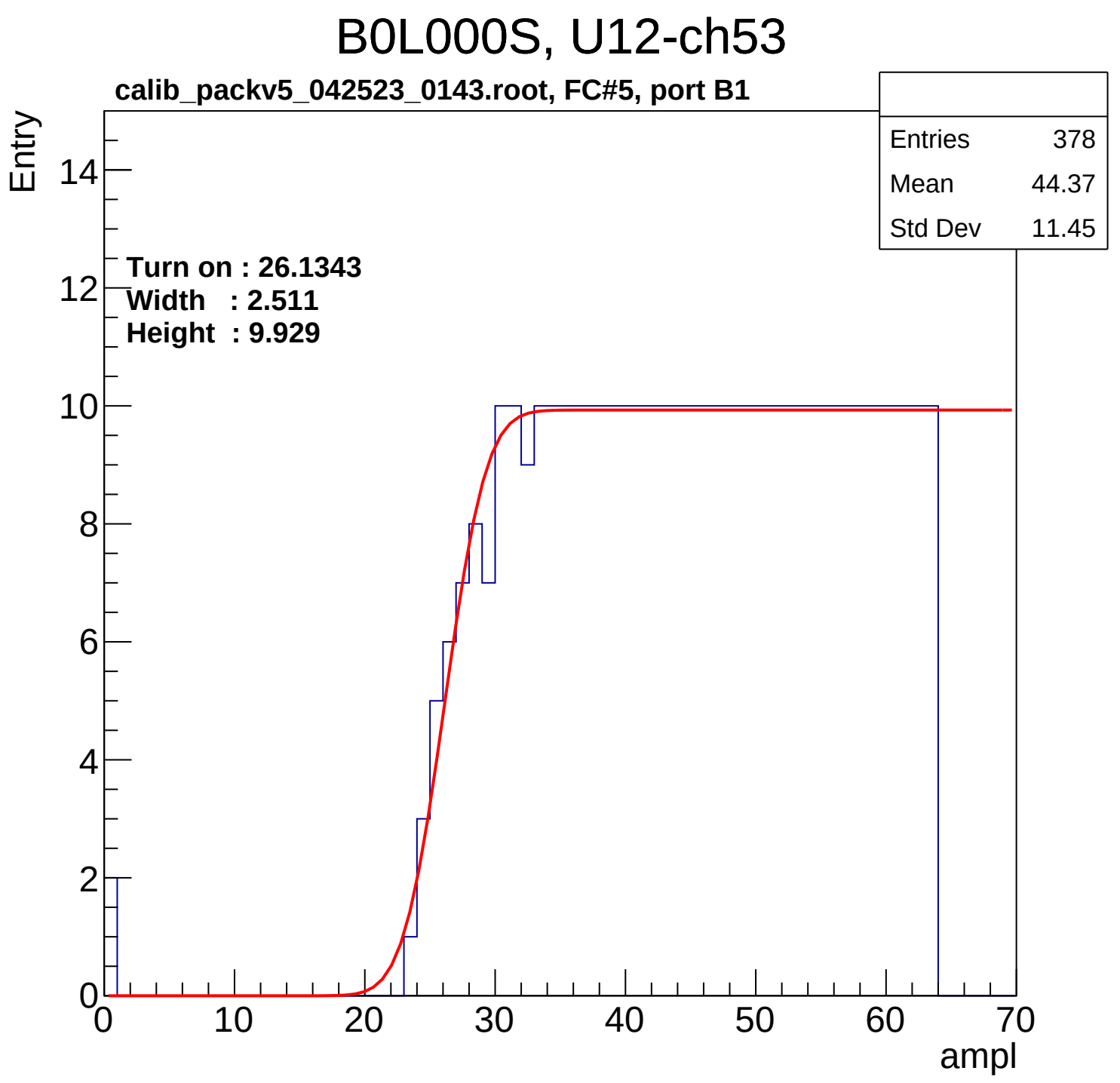
B0L000S, U12-ch53
calib_packv5_042523_0143.root, FC#5, port B1
Entries 378
Mean 44.37
Std Dev 11.45
Turn on : 26.1343
Width : 2.511
Height : 9.929
Entry
ampl
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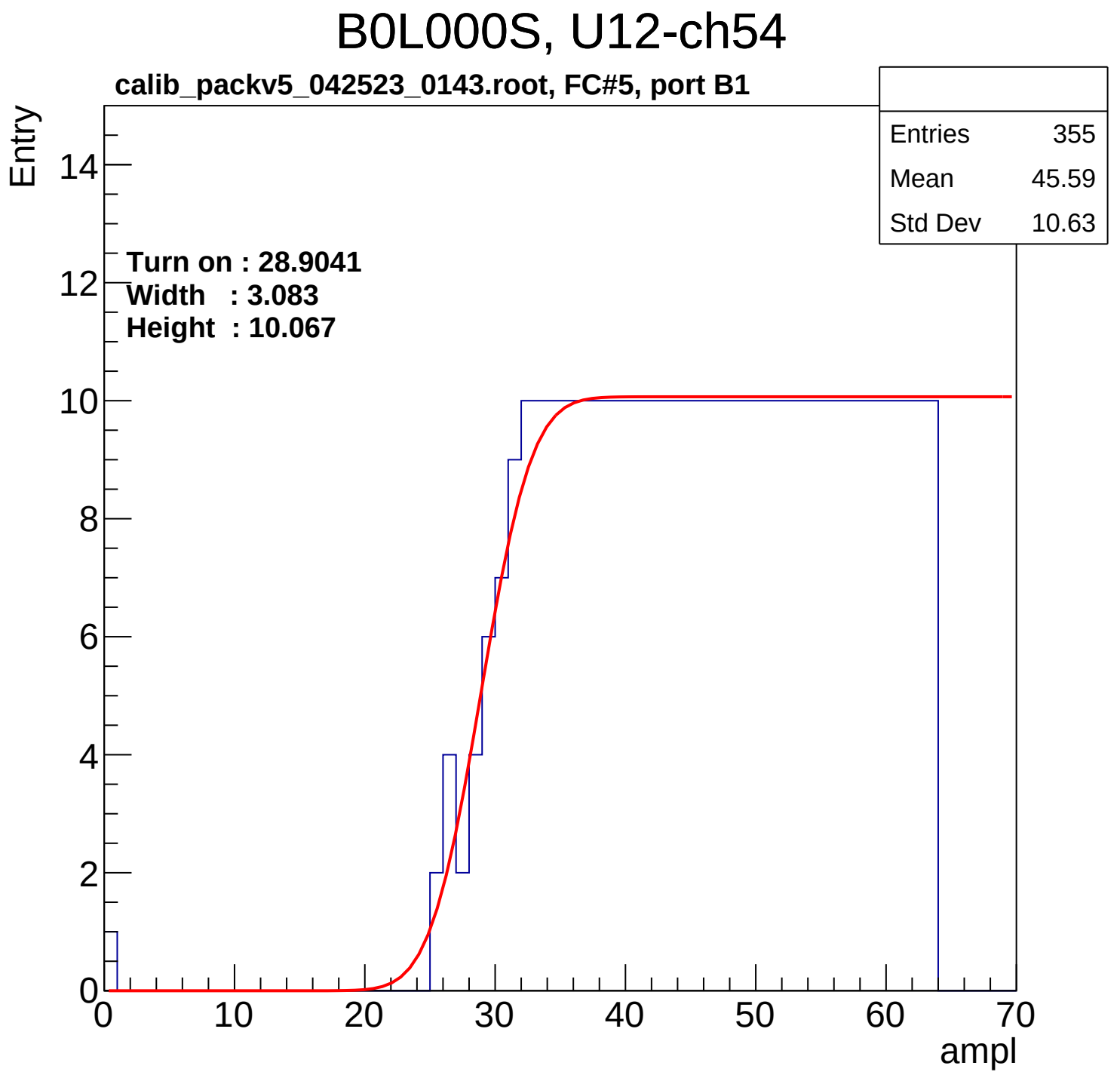
B0L000S, U12-ch54
calib_packv5_042523_0143.root, FC#5, port B1
Entries 355
Mean 45.59
Std Dev 10.63
Turn on : 28.9041
Width : 3.083
Height : 10.067
Entry
ampl
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6
8
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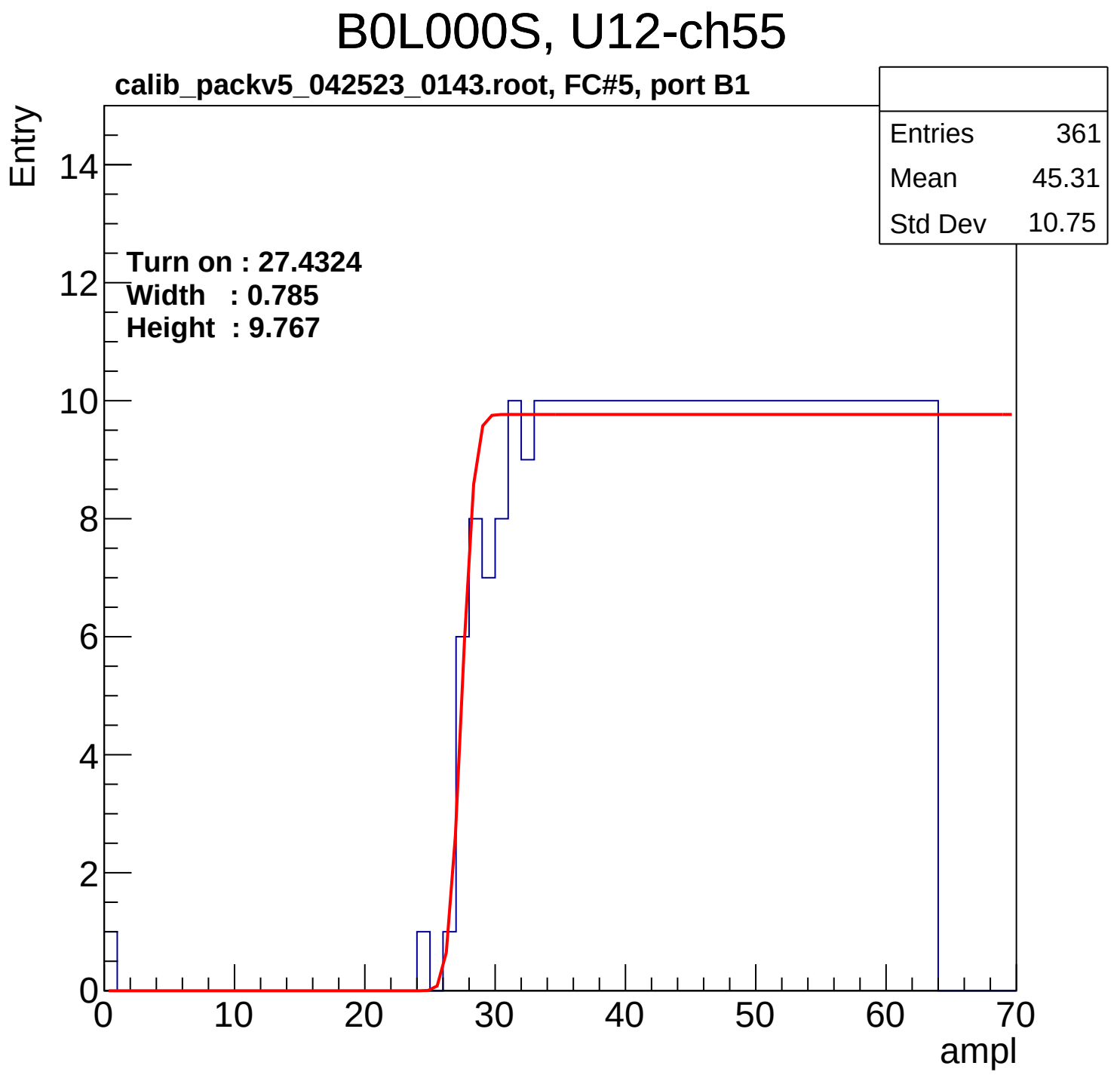
B0L000S, U12-ch55
calib_packv5_042523_0143.root, FC#5, port B1
Entries 361
Mean 45.31
Std Dev 10.75
Turn on : 27.4324
Width : 0.785
Height : 9.767
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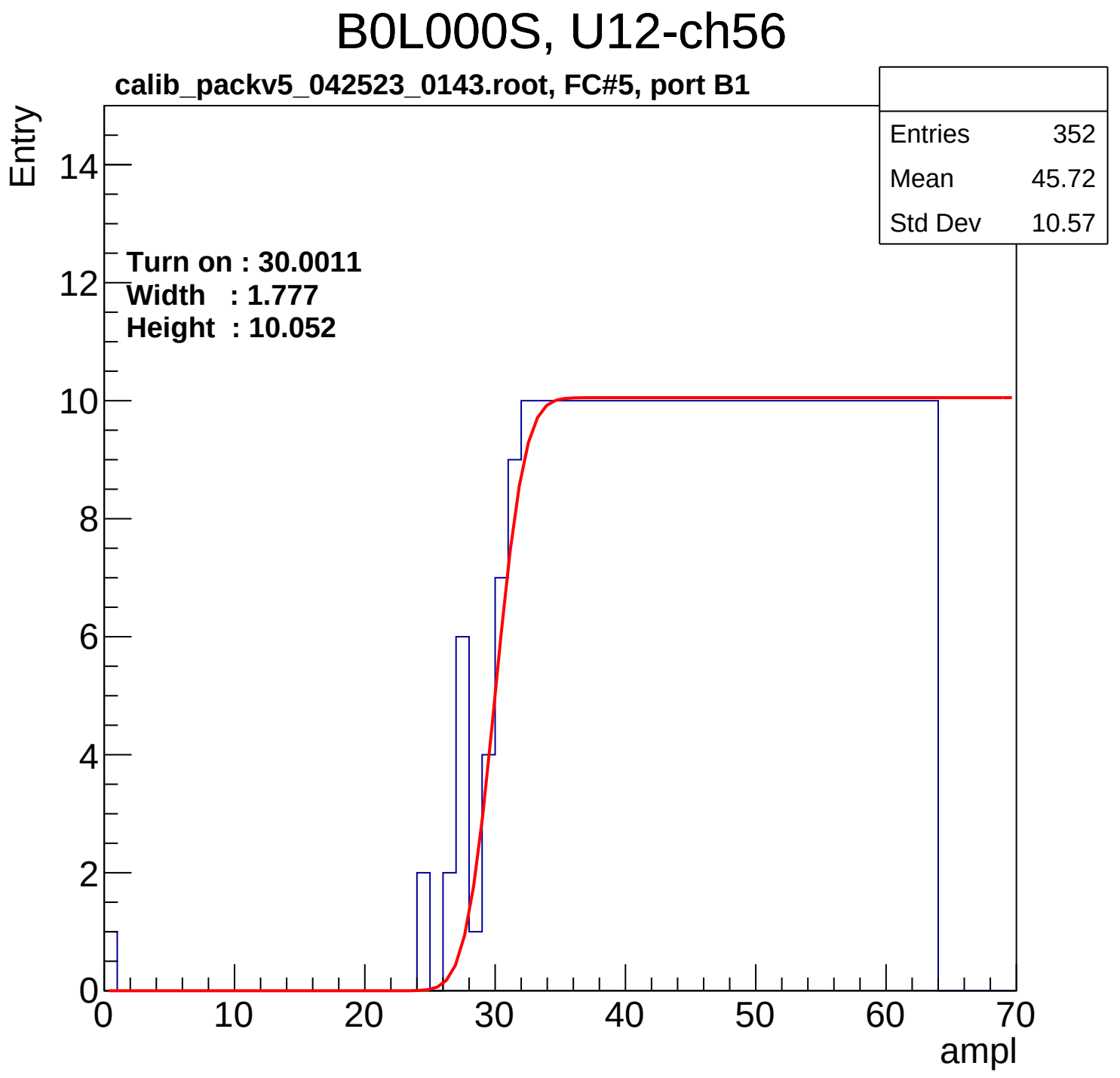
B0L000S, U12-ch56
calib_packv5_042523_0143.root, FC#5, port B1
Entries 352
Mean 45.72
Std Dev 10.57
Turn on : 30.0011
Width : 1.777
Height : 10.052
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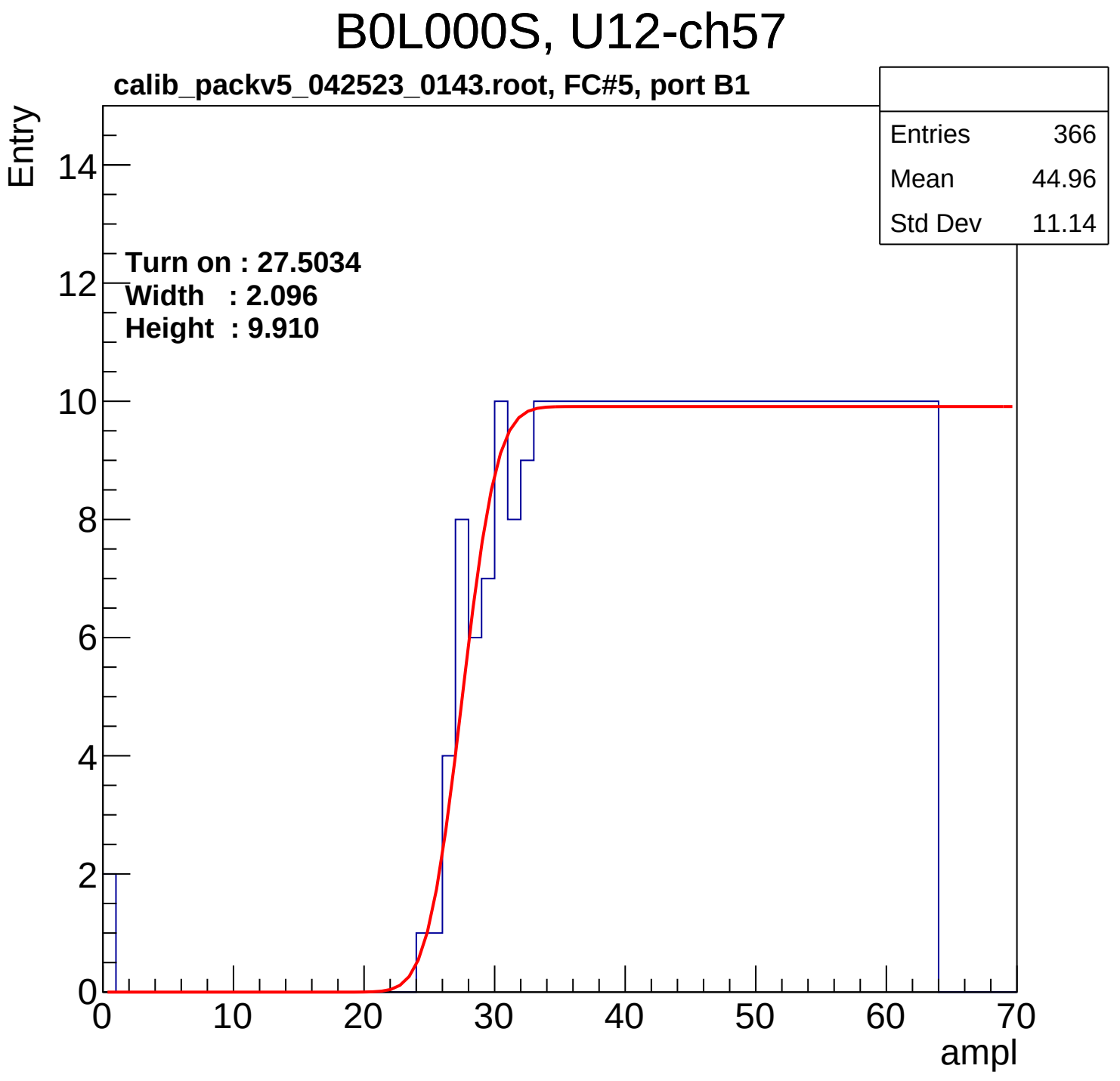
B0L000S, U12-ch57
calib_packv5_042523_0143.root, FC#5, port B1
Entries 366
Mean 44.96
Std Dev 11.14
Turn on : 27.5034
Width : 2.096
Height : 9.910
Entry
ampl
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4
6
8
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10
20
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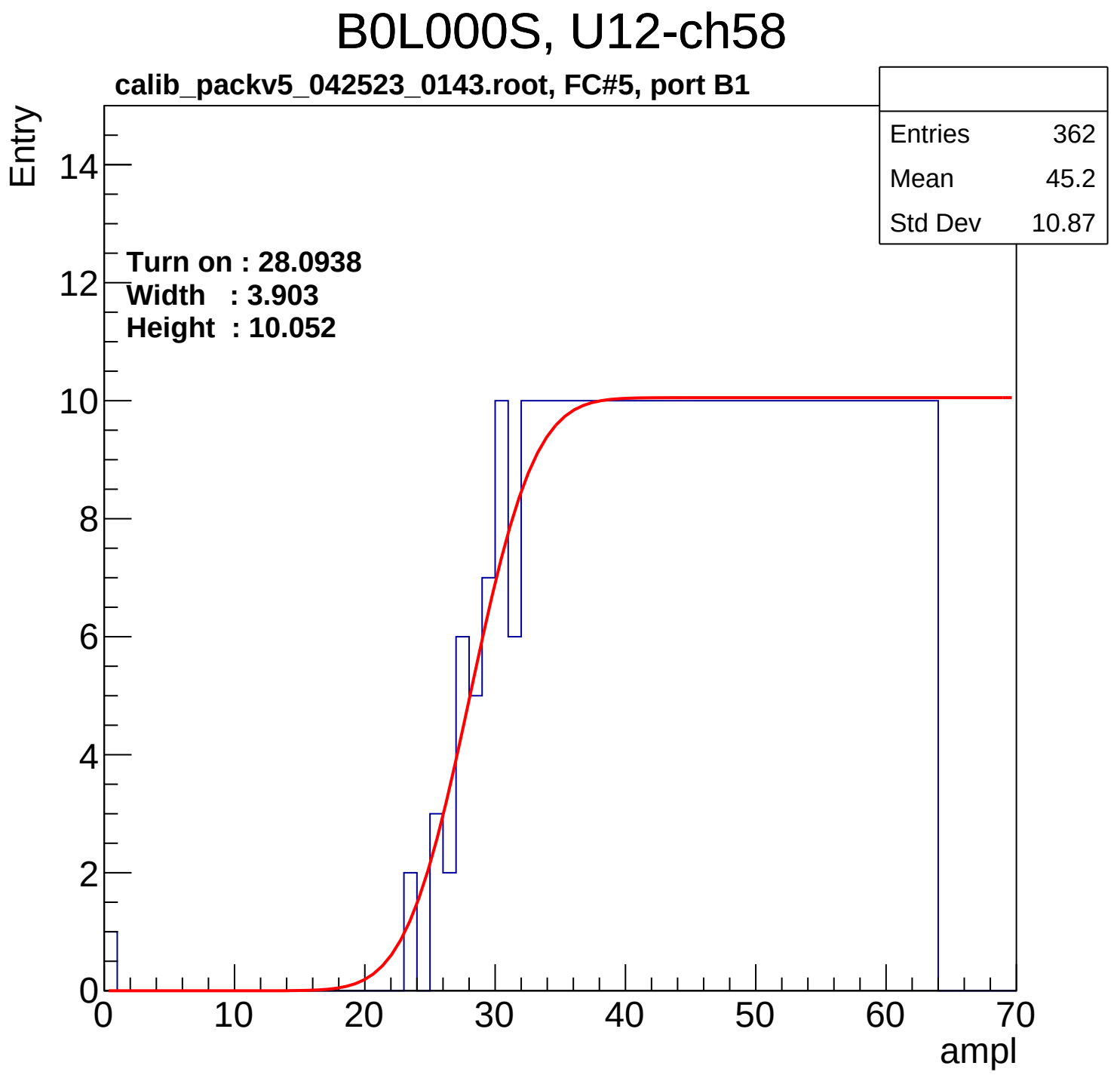
B0L000S, U12-ch58
calib_packv5_042523_0143.root, FC#5, port B1
Entries 362
Mean 45.2
Std Dev 10.87
Turn on : 28.0938
Width : 3.903
Height : 10.052
Entry
ampl
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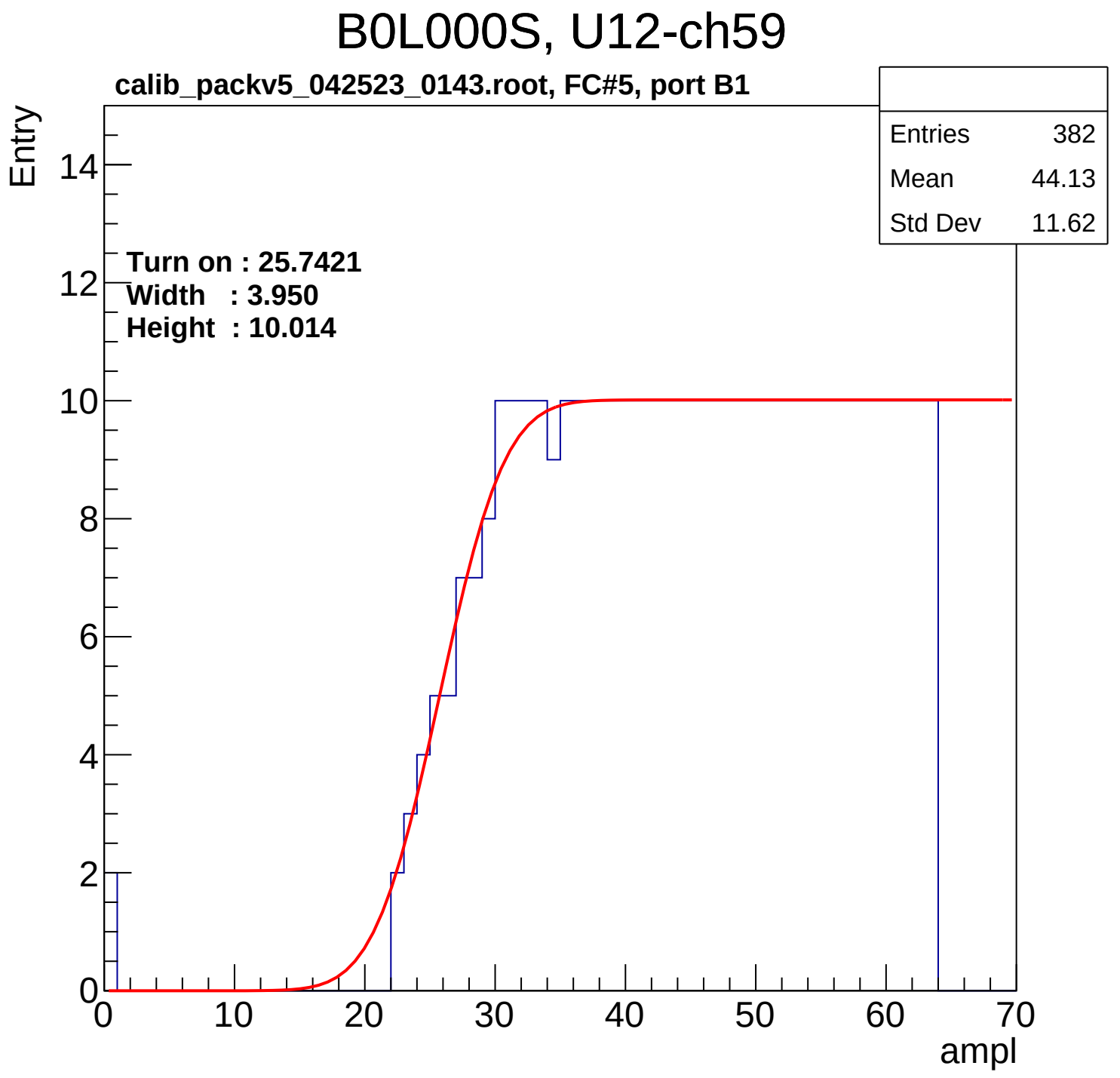
B0L000S, U12-ch59
calib_packv5_042523_0143.root, FC#5, port B1
Entries 382
Mean 44.13
Std Dev 11.62
Turn on : 25.7421
Width : 3.950
Height : 10.014
Entry
ampl
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2
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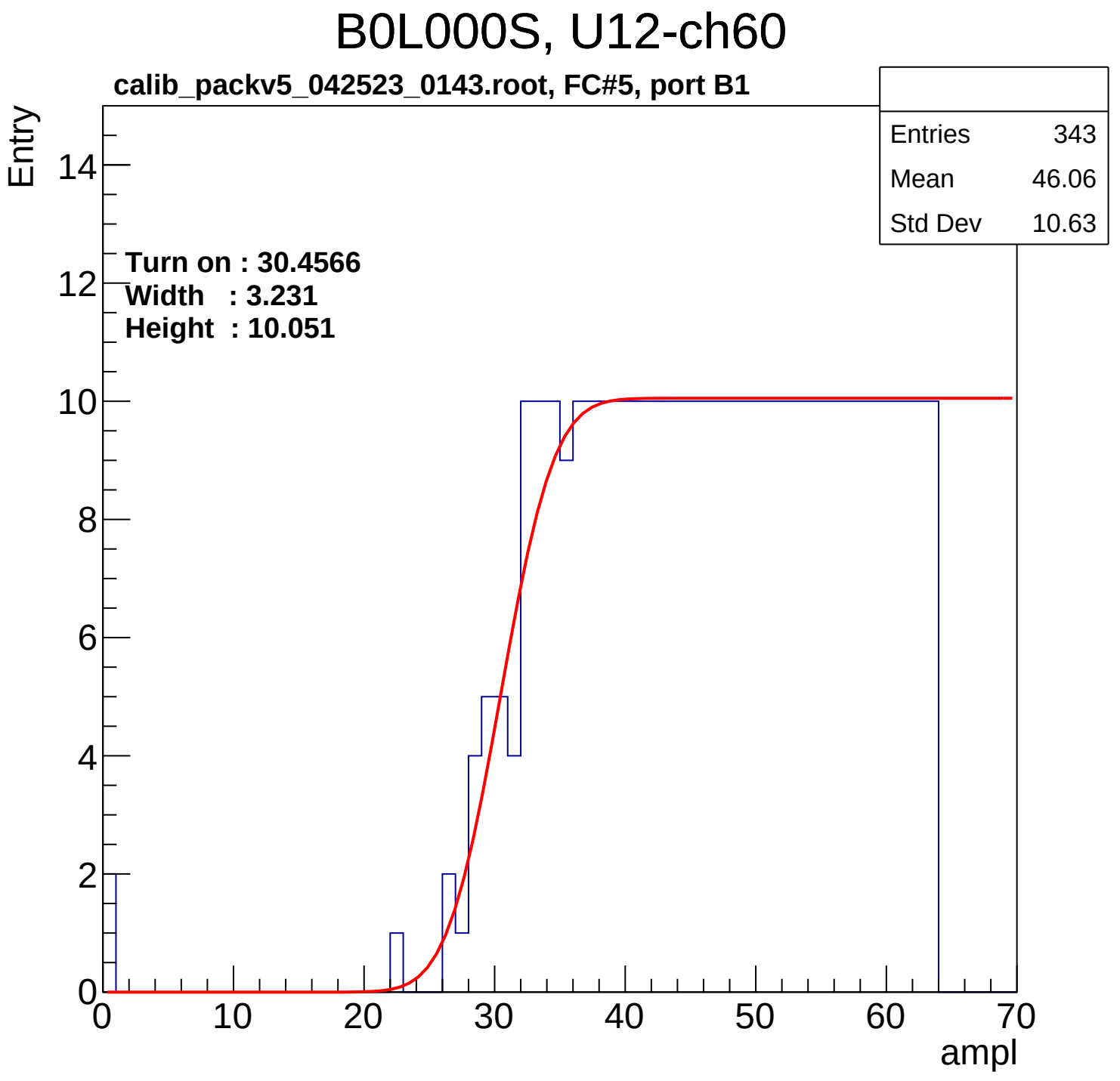
B0L000S, U12-ch60
calib_packv5_042523_0143.root, FC#5, port B1
Entries 343
Mean 46.06
Std Dev 10.63
Turn on : 30.4566
Width : 3.231
Height : 10.051
Entry
ampl
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2
4
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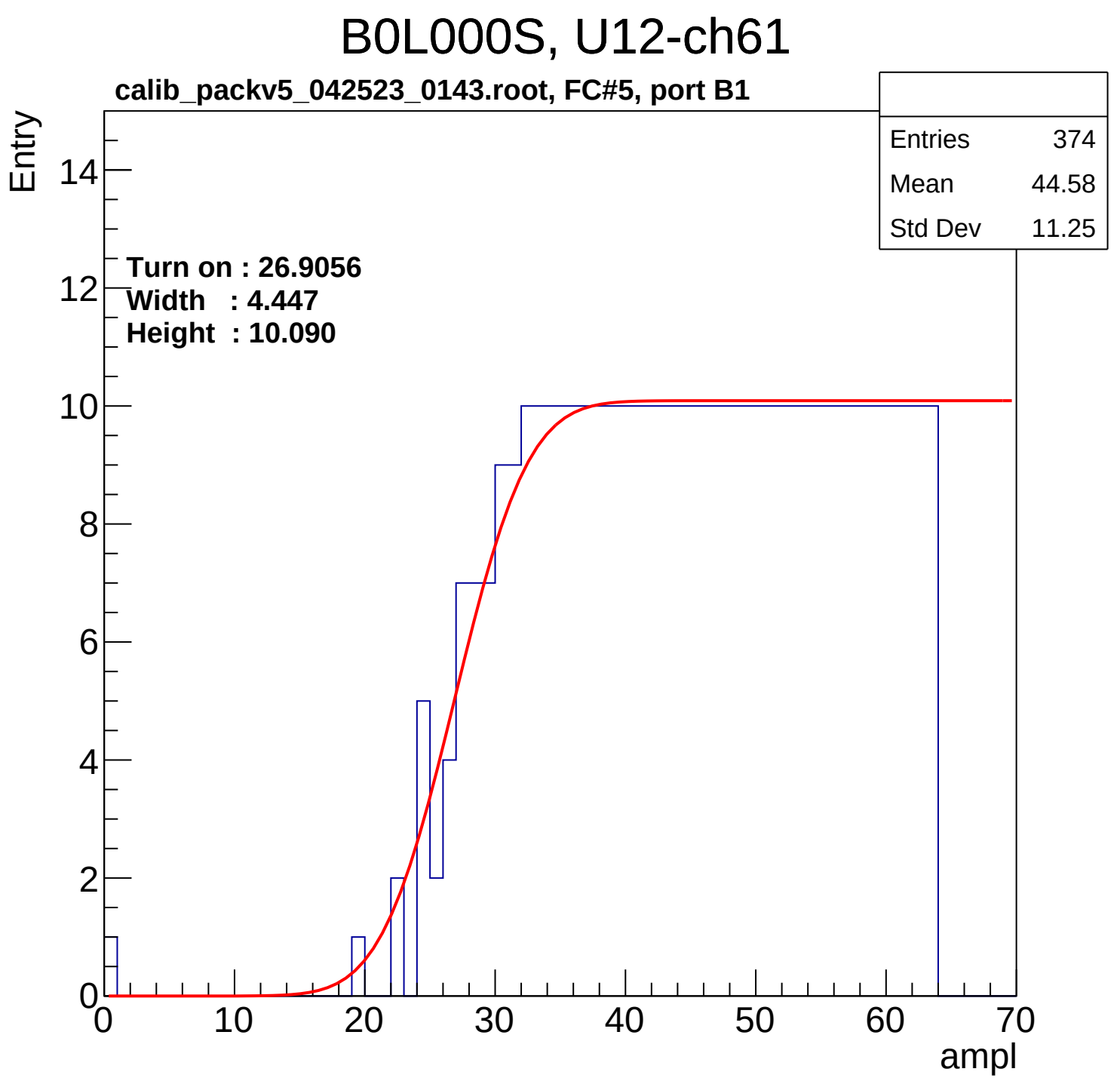
B0L000S, U12-ch61
calib_packv5_042523_0143.root, FC#5, port B1
Entries 374
Mean 44.58
Std Dev 11.25
Turn on : 26.9056
Width : 4.447
Height : 10.090
Entry
ampl
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2
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6
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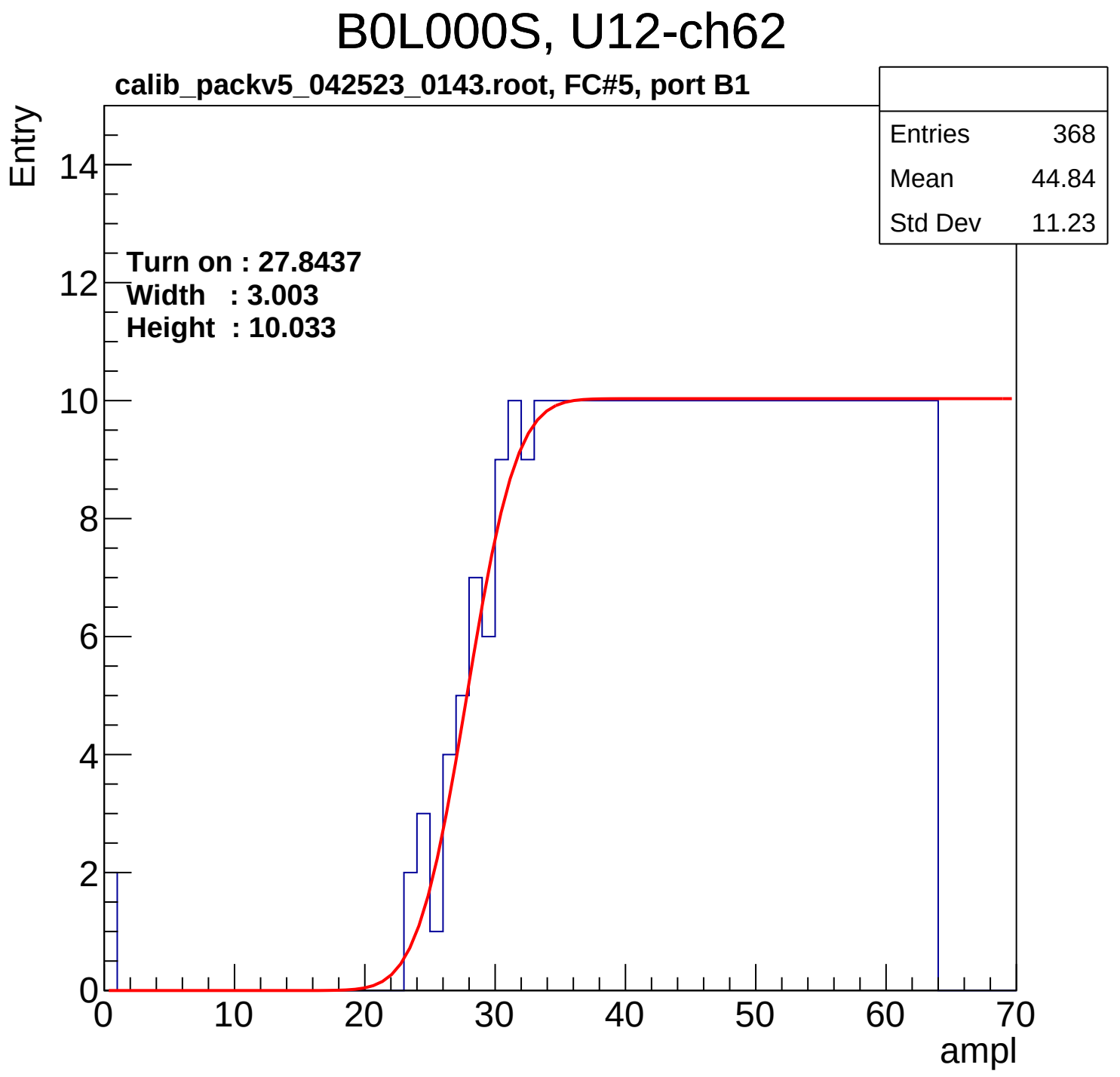
B0L000S, U12-ch62
calib_packv5_042523_0143.root, FC#5, port B1
Entries 368
Mean 44.84
Std Dev 11.23
Turn on : 27.8437
Width : 3.003
Height : 10.033
Entry
ampl
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2
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6
8
10
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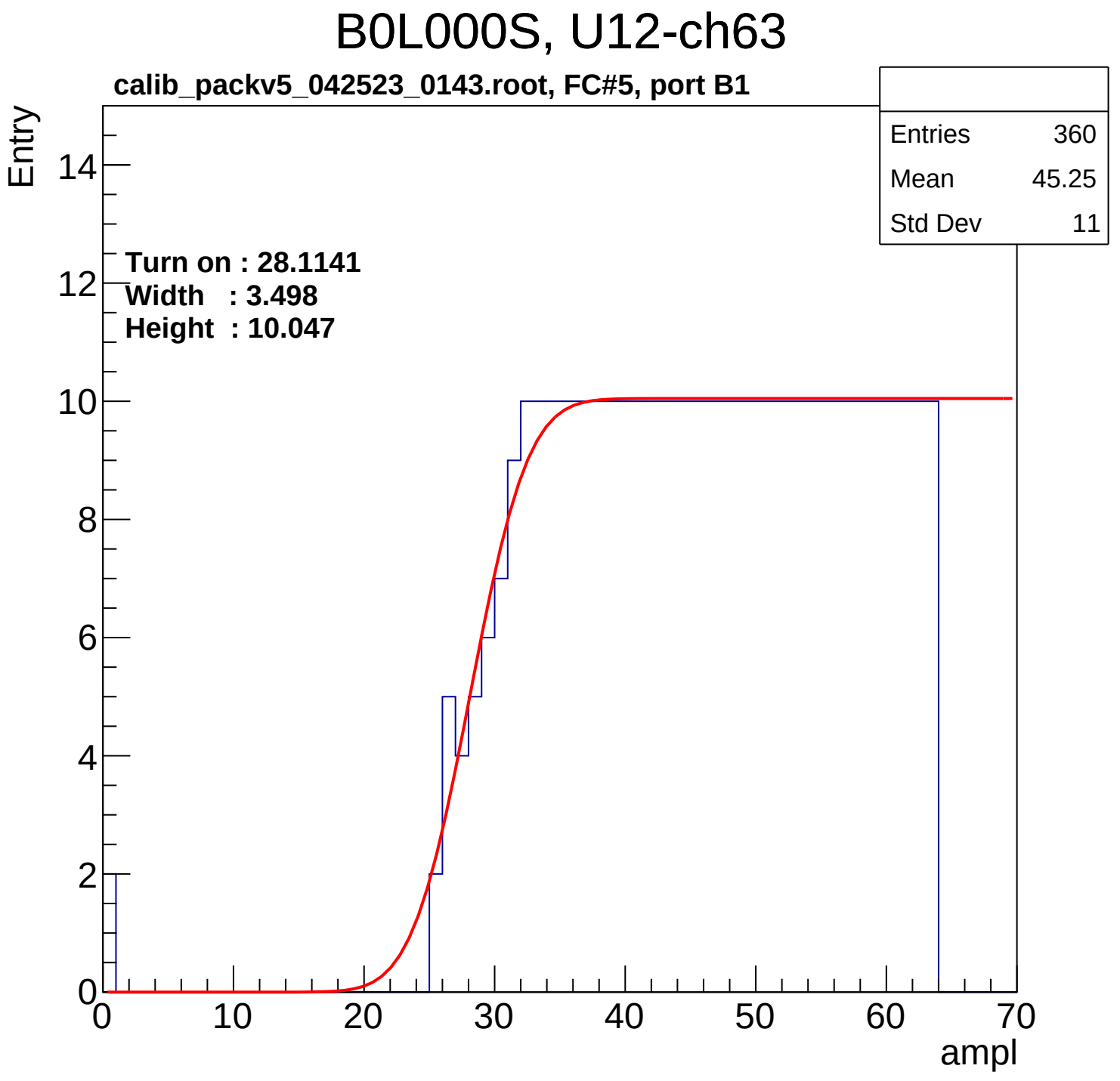
B0L000S, U12-ch63
calib_packv5_042523_0143.root, FC#5, port B1
Entries 360
Mean 45.25
Std Dev 11
Turn on : 28.1141
Width : 3.498
Height : 10.047
Entry
ampl
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2
4
6
8
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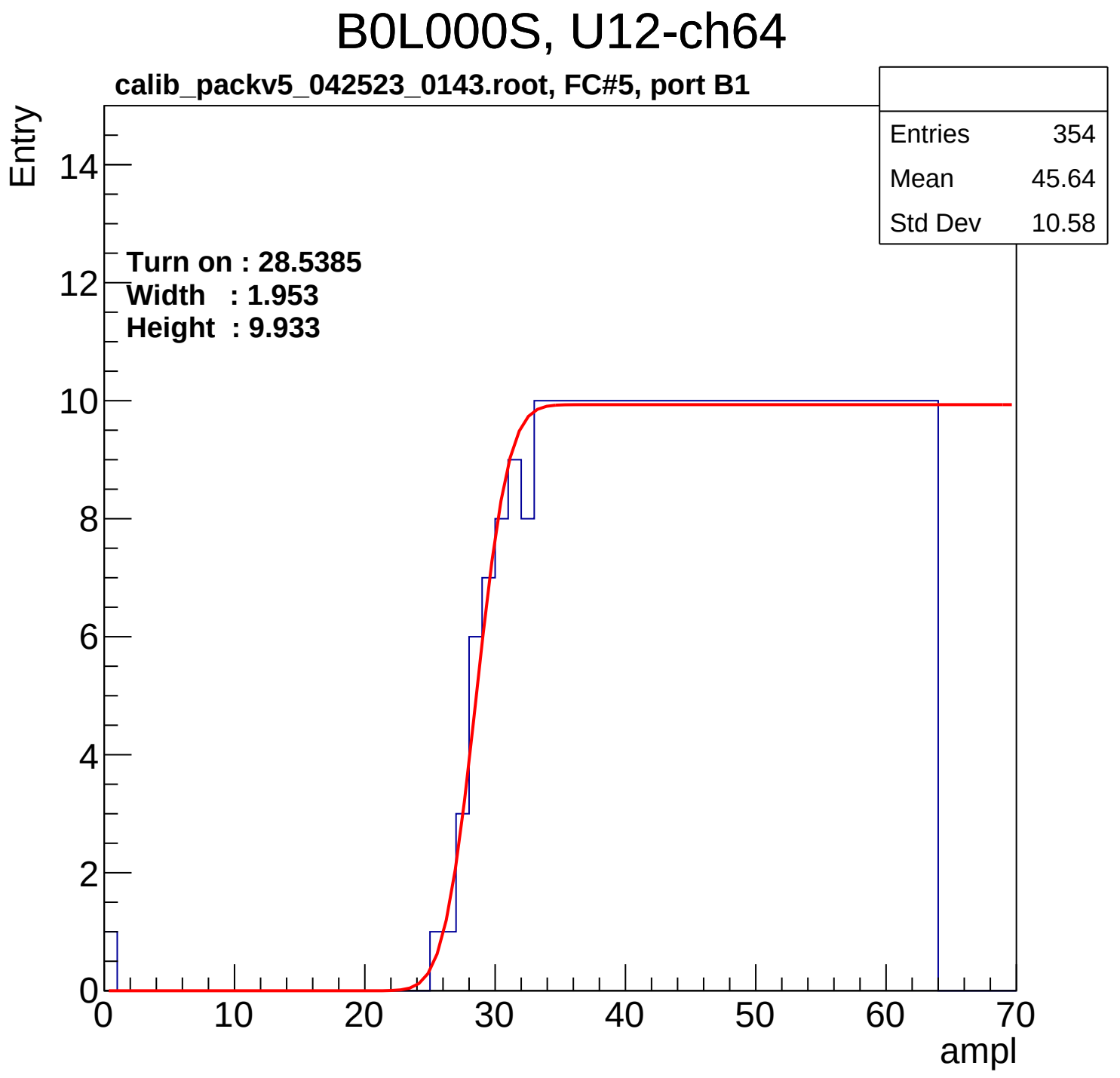
B0L000S, U12-ch64
calib_packv5_042523_0143.root, FC#5, port B1
Entries 354
Mean 45.64
Std Dev 10.58
Turn on : 28.5385
Width : 1.953
Height : 9.933
Entry
ampl
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4
6
8
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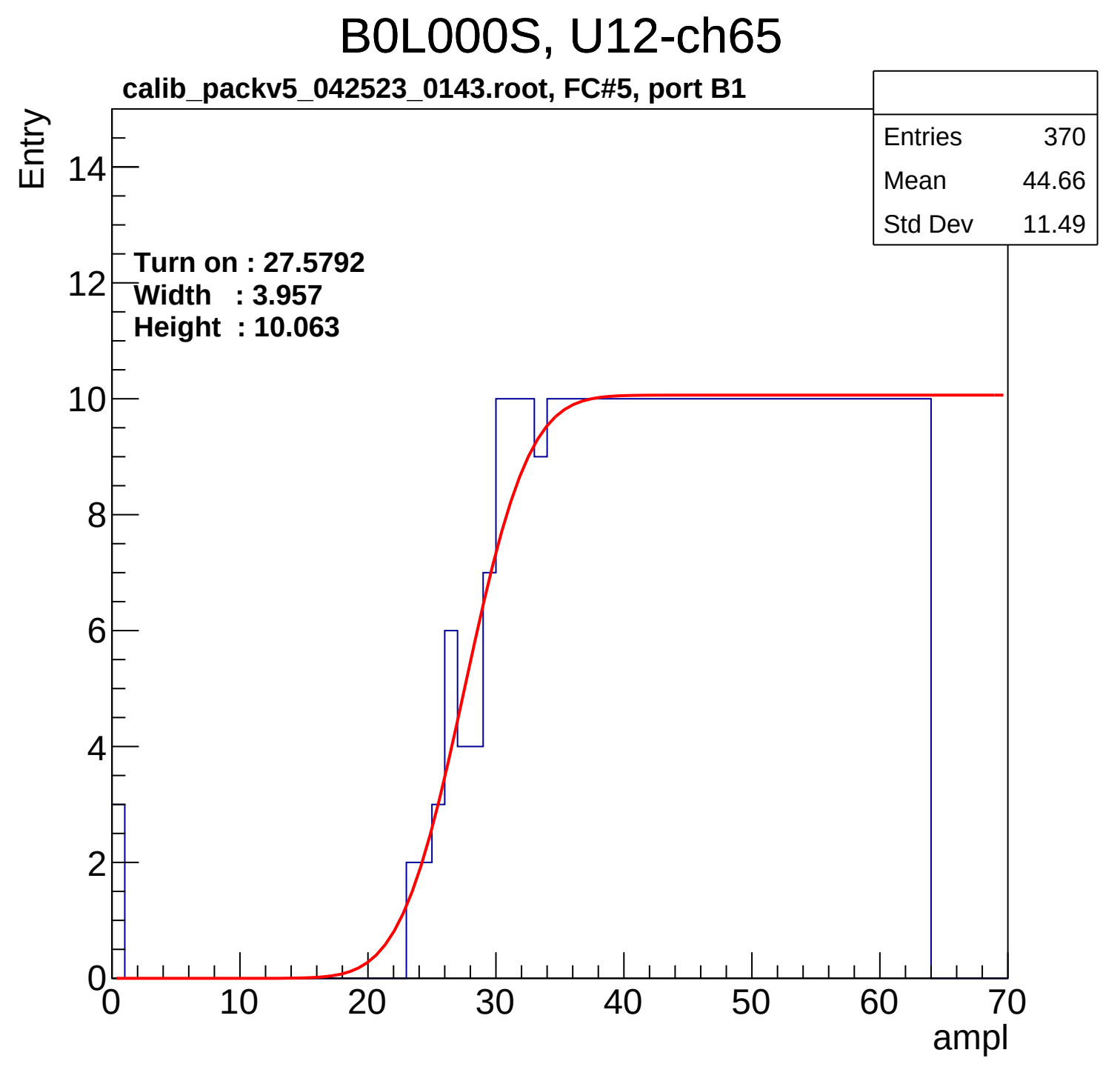
B0L000S, U12-ch65
calib_packv5_042523_0143.root, FC#5, port B1
Entries 370
Mean 44.66
Std Dev 11.49
Turn on : 27.5792
Width : 3.957
Height : 10.063
Entry
ampl
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4
6
8
10
12
14
0
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20
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60
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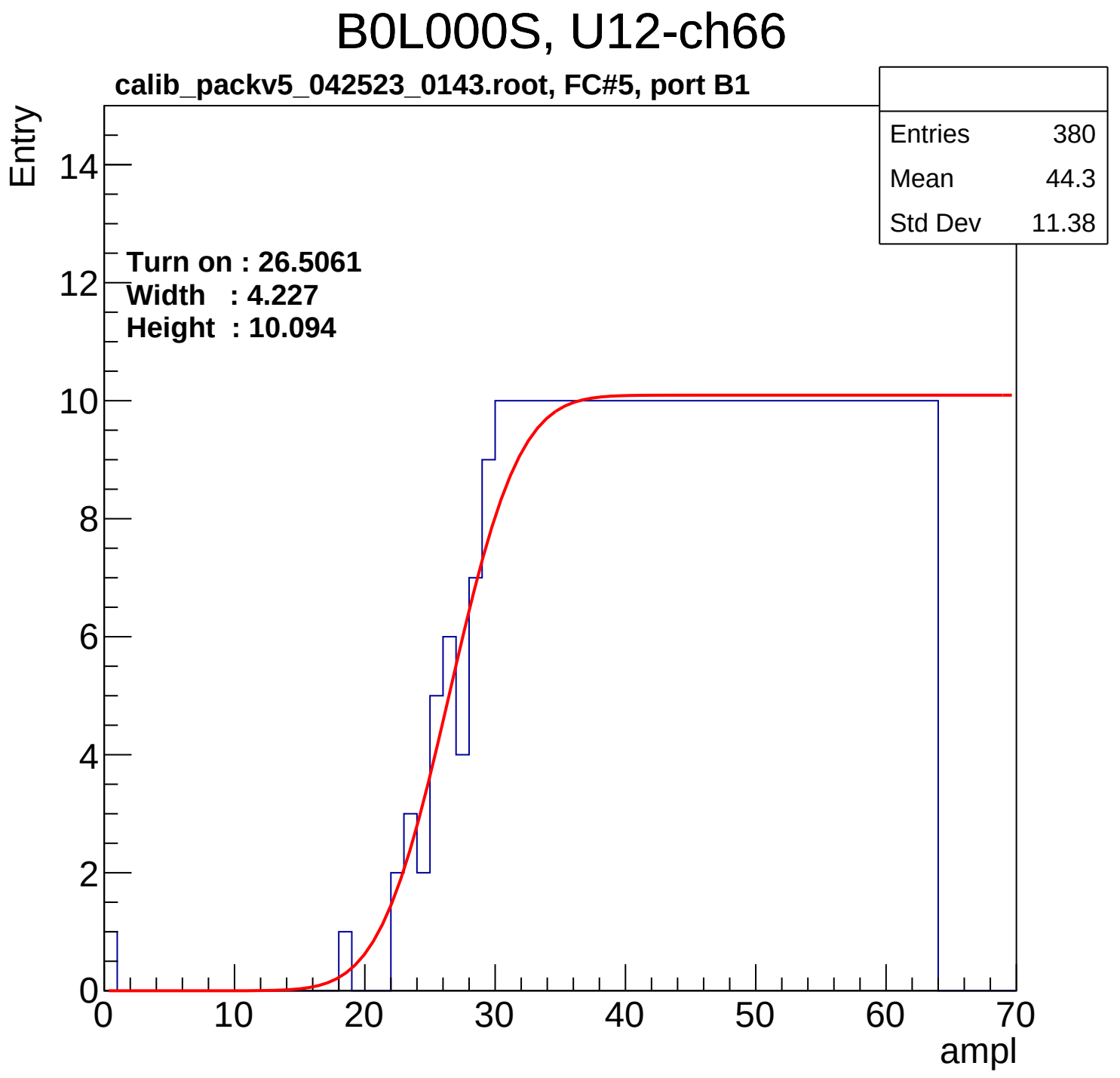
B0L000S, U12-ch66
calib_packv5_042523_0143.root, FC#5, port B1
Entries 380
Mean 44.3
Std Dev 11.38
Turn on : 26.5061
Width : 4.227
Height : 10.094
Entry
ampl
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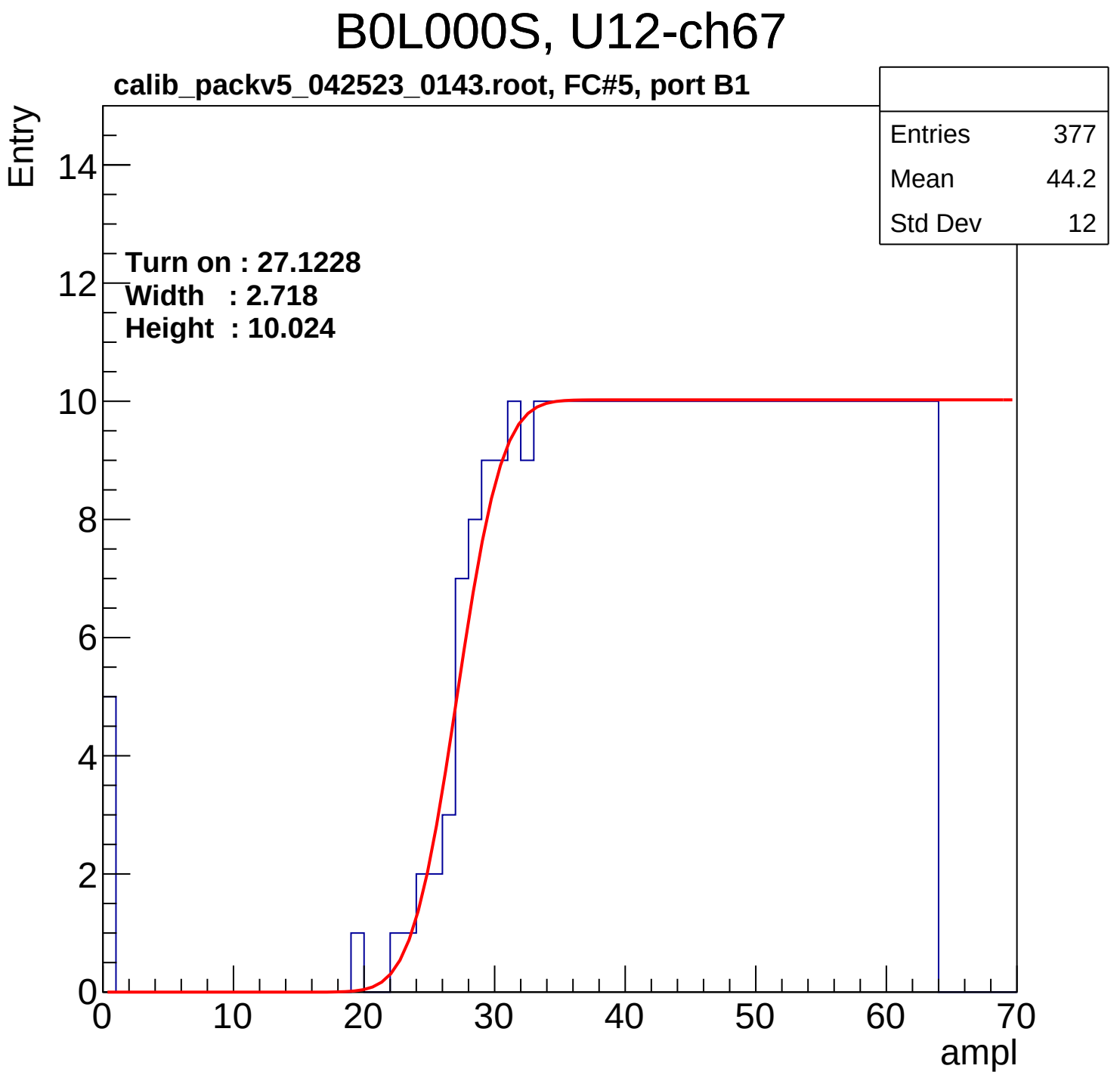
B0L000S, U12-ch67
calib_packv5_042523_0143.root, FC#5, port B1
Entries 377
Mean 44.2
Std Dev 12
Turn on : 27.1228
Width : 2.718
Height : 10.024
Entry
ampl
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2
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6
8
10
12
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0
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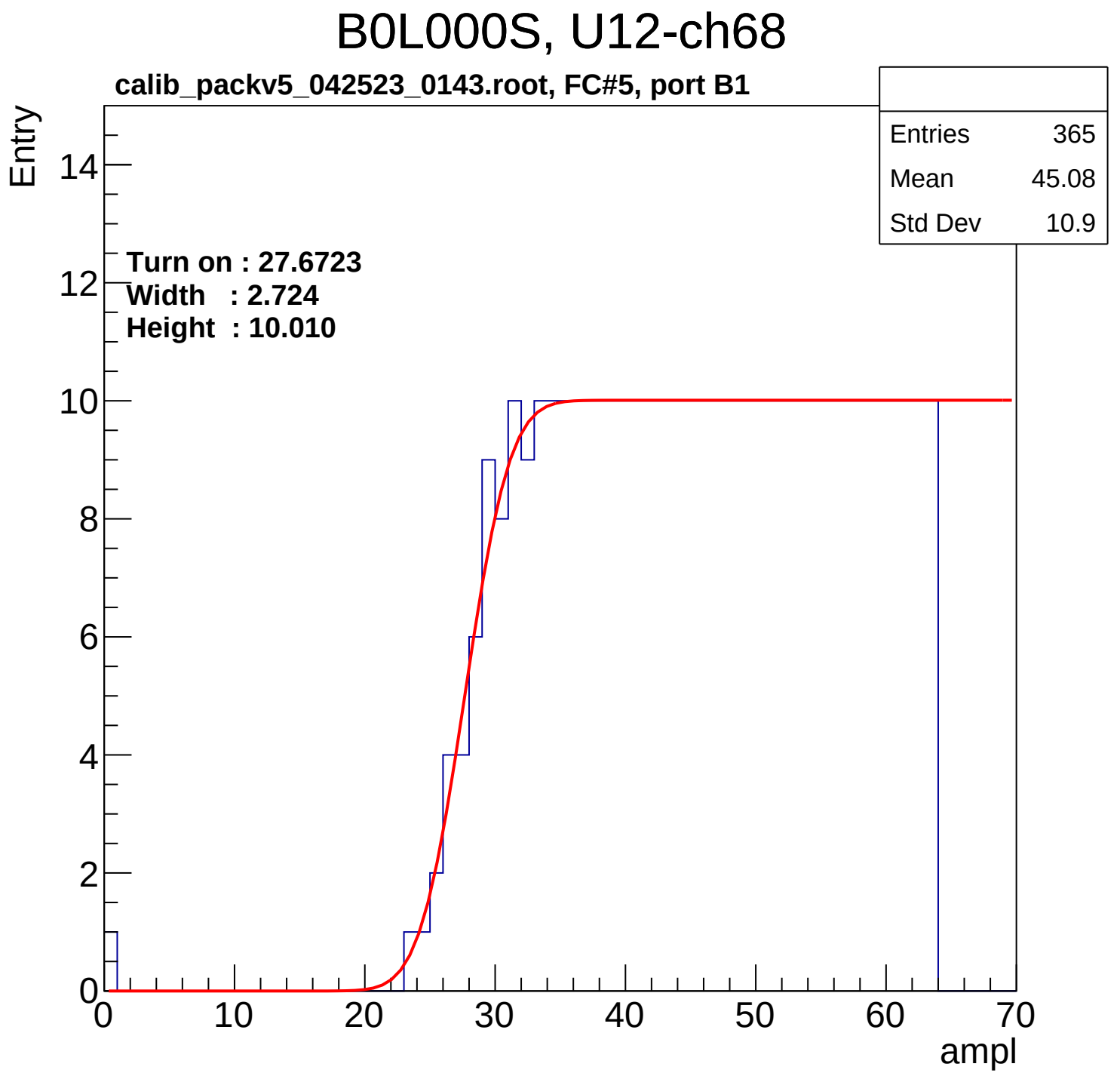
B0L000S, U12-ch68
calib_packv5_042523_0143.root, FC#5, port B1
Entries 365
Mean 45.08
Std Dev 10.9
Turn on : 27.6723
Width : 2.724
Height : 10.010
Entry
ampl
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2
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6
8
10
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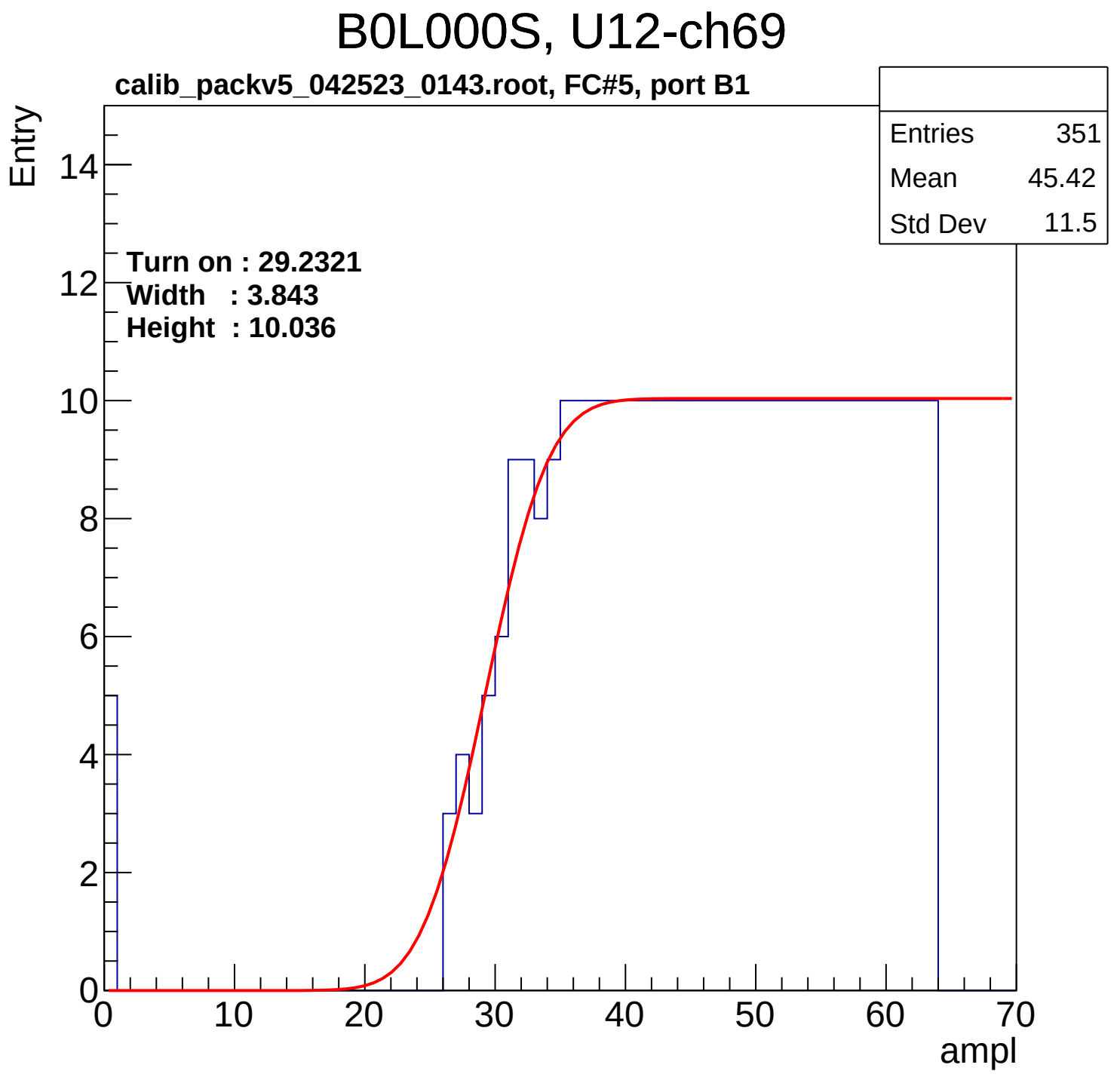
B0L000S, U12-ch69
calib_packv5_042523_0143.root, FC#5, port B1
Entries 351
Mean 45.42
Std Dev 11.5
Turn on : 29.2321
Width : 3.843
Height : 10.036
Entry
ampl
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8
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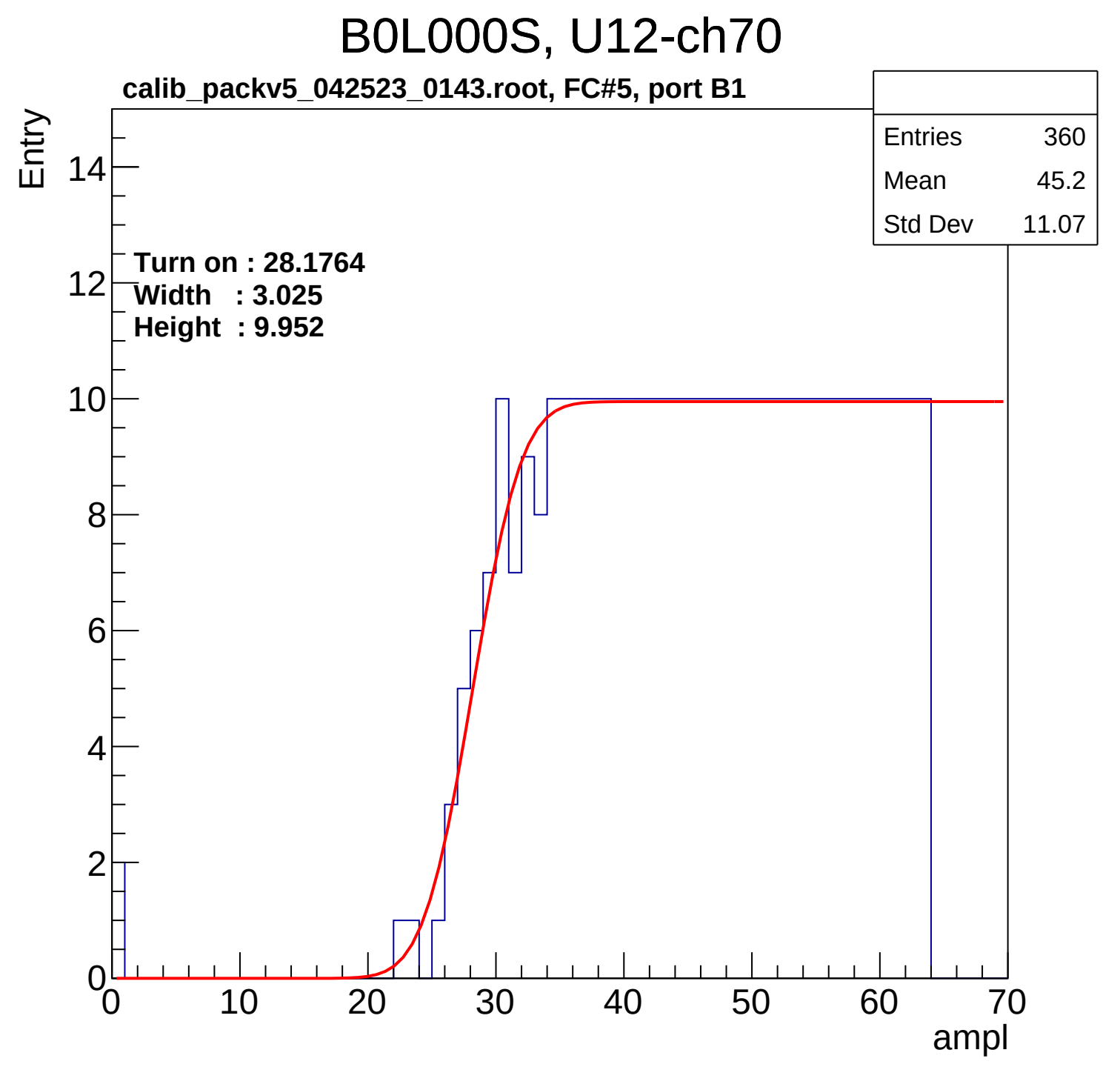
B0L000S, U12-ch70
calib_packv5_042523_0143.root, FC#5, port B1
Entries 360
Mean 45.2
Std Dev 11.07
Turn on : 28.1764
Width : 3.025
Height : 9.952
Entry
ampl
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8
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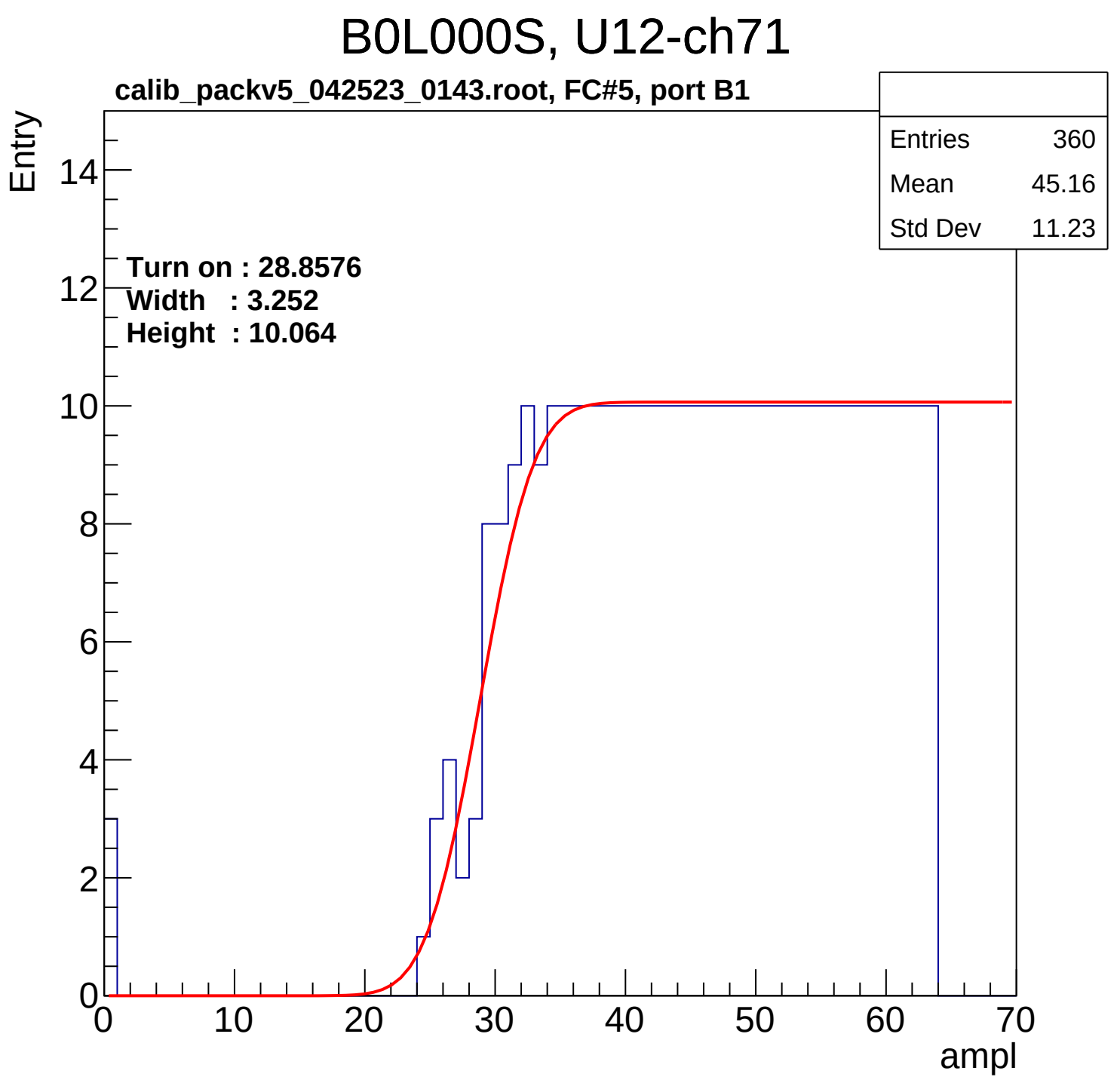
B0L000S, U12-ch71
calib_packv5_042523_0143.root, FC#5, port B1
Entries 360
Mean 45.16
Std Dev 11.23
Turn on : 28.8576
Width : 3.252
Height : 10.064
Entry
ampl
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6
8
10
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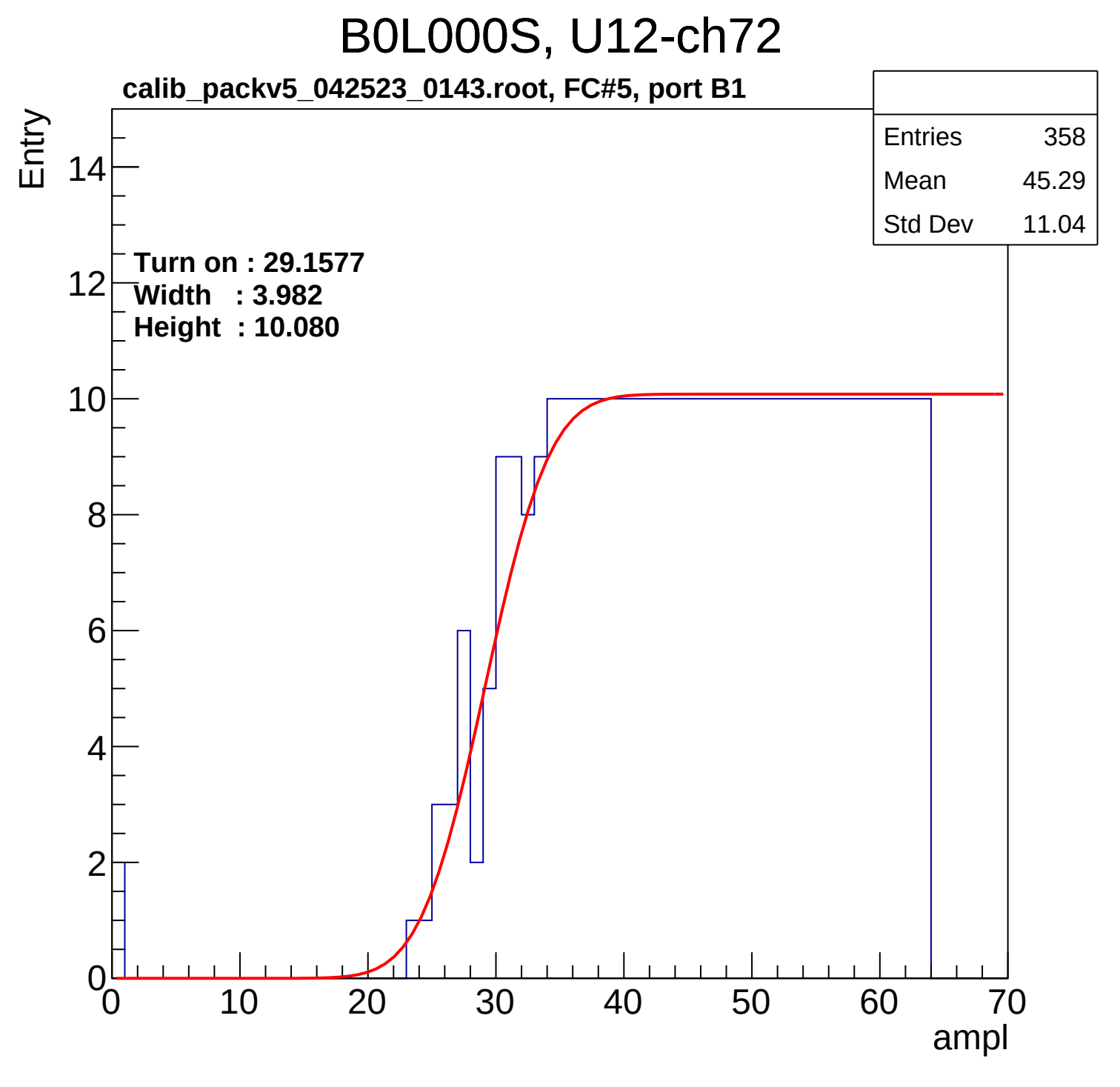
B0L000S, U12-ch72
calib_packv5_042523_0143.root, FC#5, port B1
Entries 358
Mean 45.29
Std Dev 11.04
Turn on : 29.1577
Width : 3.982
Height : 10.080
Entry
ampl
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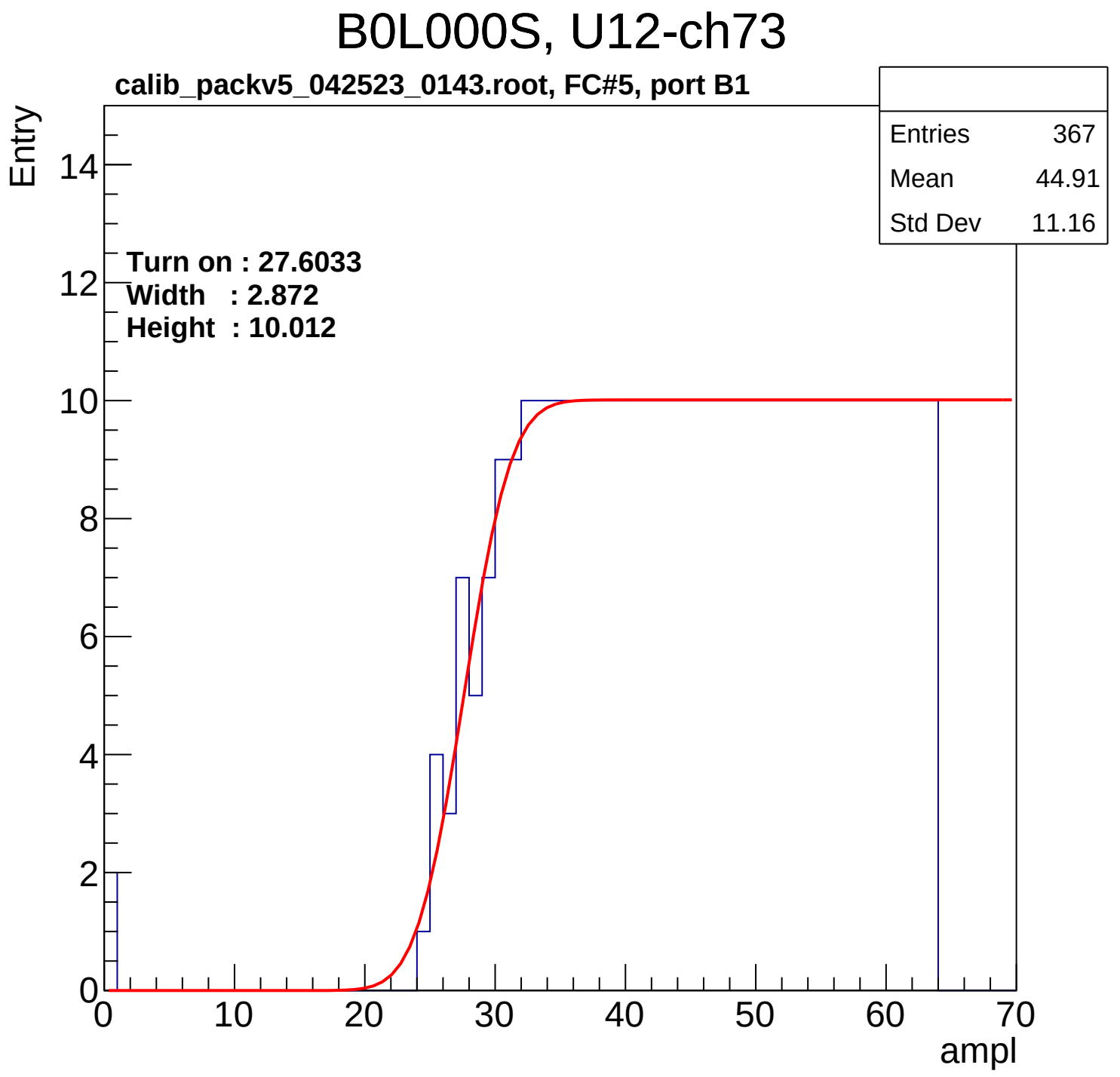
B0L000S, U12-ch73
calib_packv5_042523_0143.root, FC#5, port B1
Entries 367
Mean 44.91
Std Dev 11.16
Turn on : 27.6033
Width : 2.872
Height : 10.012
Entry
ampl
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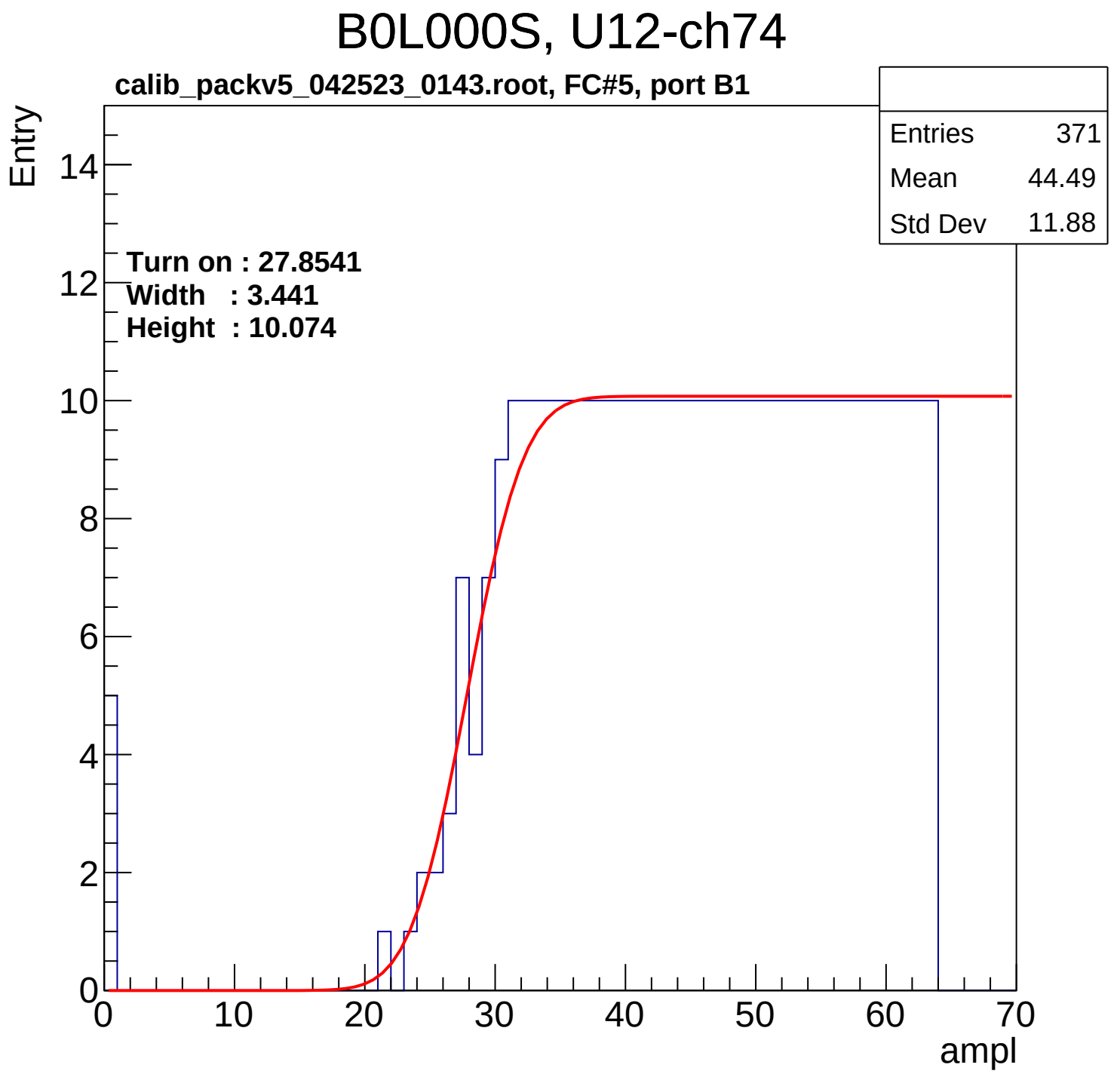
B0L000S, U12-ch74
calib_packv5_042523_0143.root, FC#5, port B1
Entries 371
Mean 44.49
Std Dev 11.88
Turn on : 27.8541
Width : 3.441
Height : 10.074
Entry
ampl
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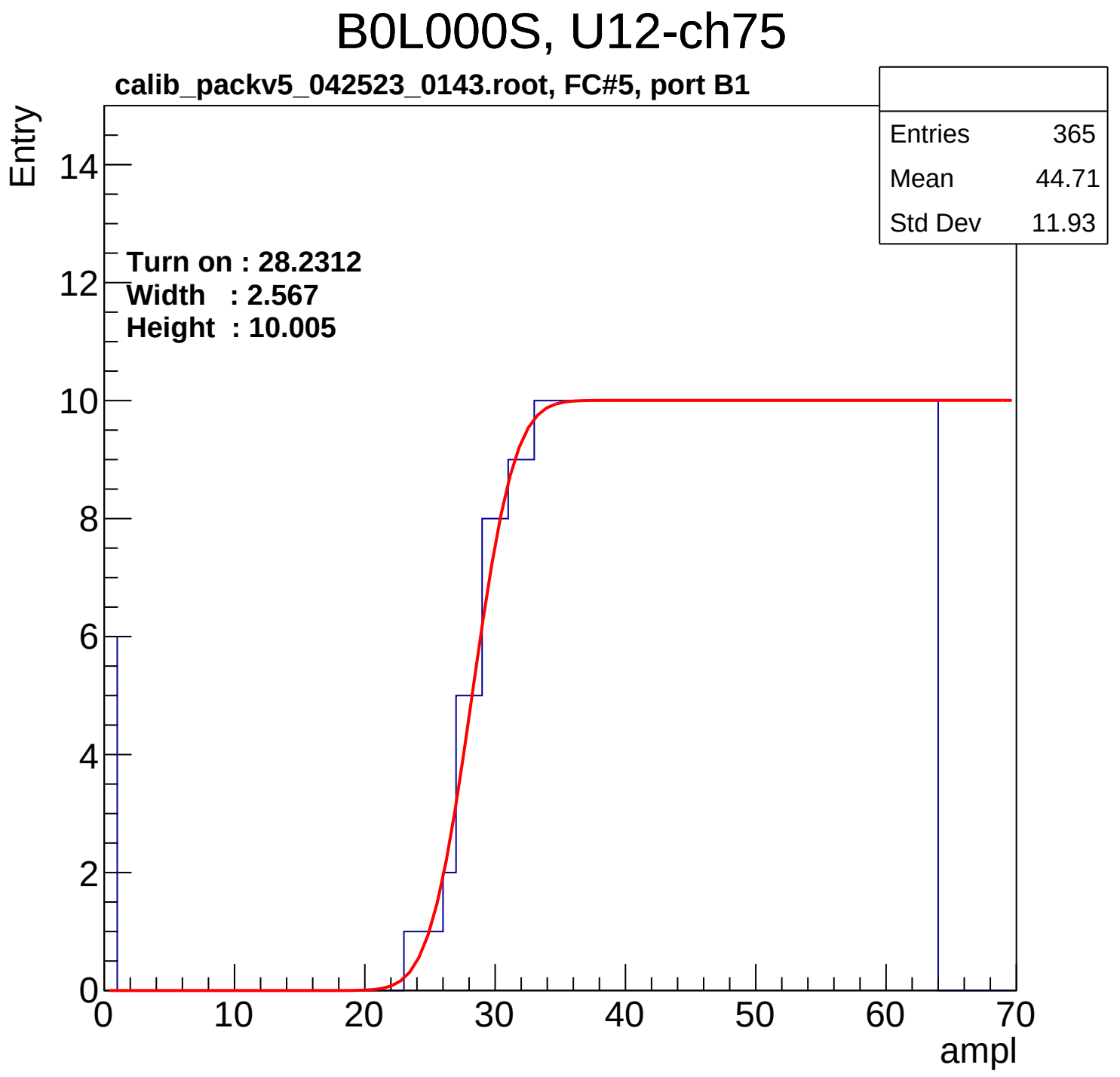
B0L000S, U12-ch75
calib_packv5_042523_0143.root, FC#5, port B1
Entries 365
Mean 44.71
Std Dev 11.93
Turn on : 28.2312
Width : 2.567
Height : 10.005
Entry
ampl
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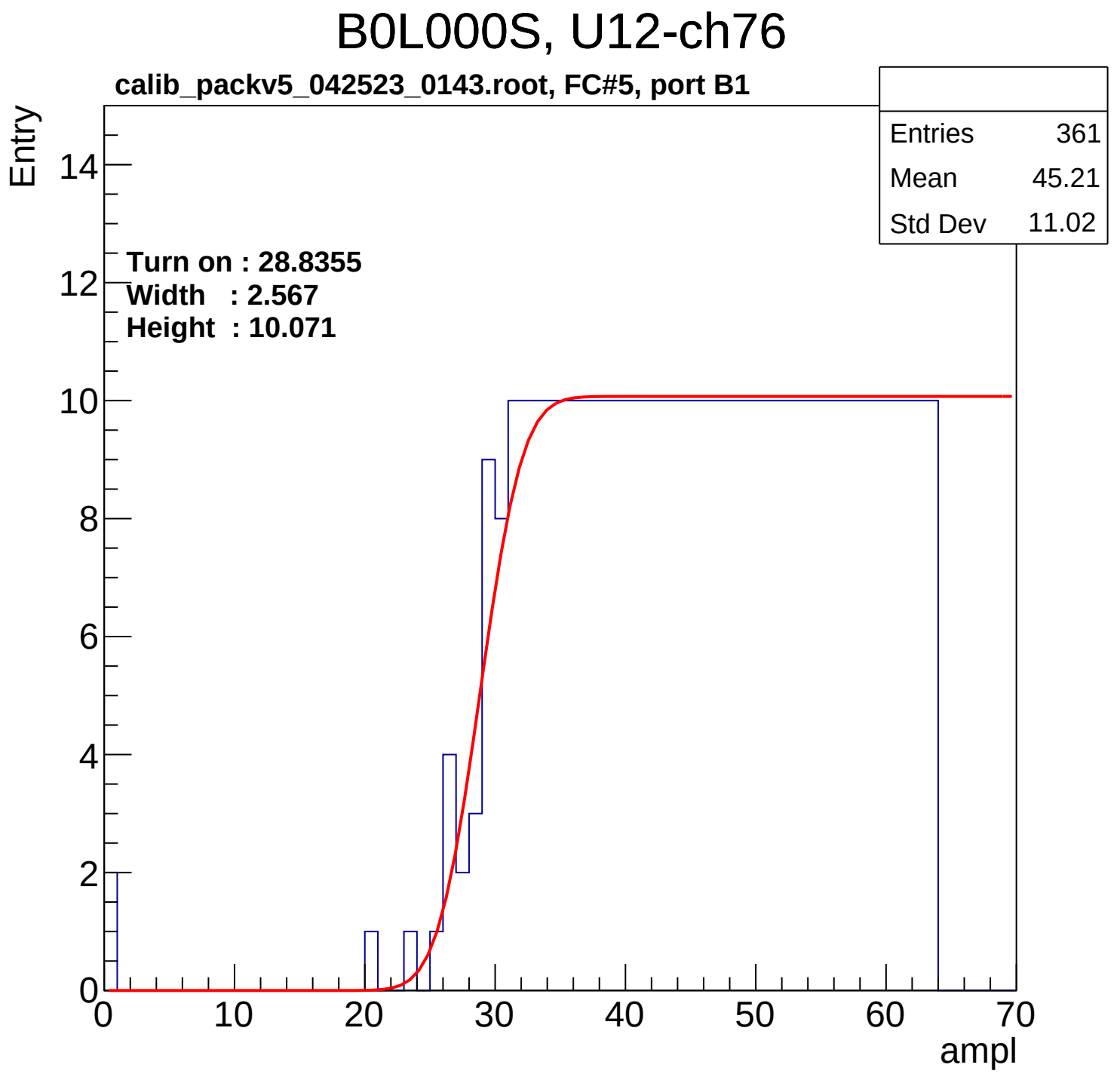
B0L000S, U12-ch76
calib_packv5_042523_0143.root, FC#5, port B1
Entries 361
Mean 45.21
Std Dev 11.02
Turn on : 28.8355
Width : 2.567
Height : 10.071
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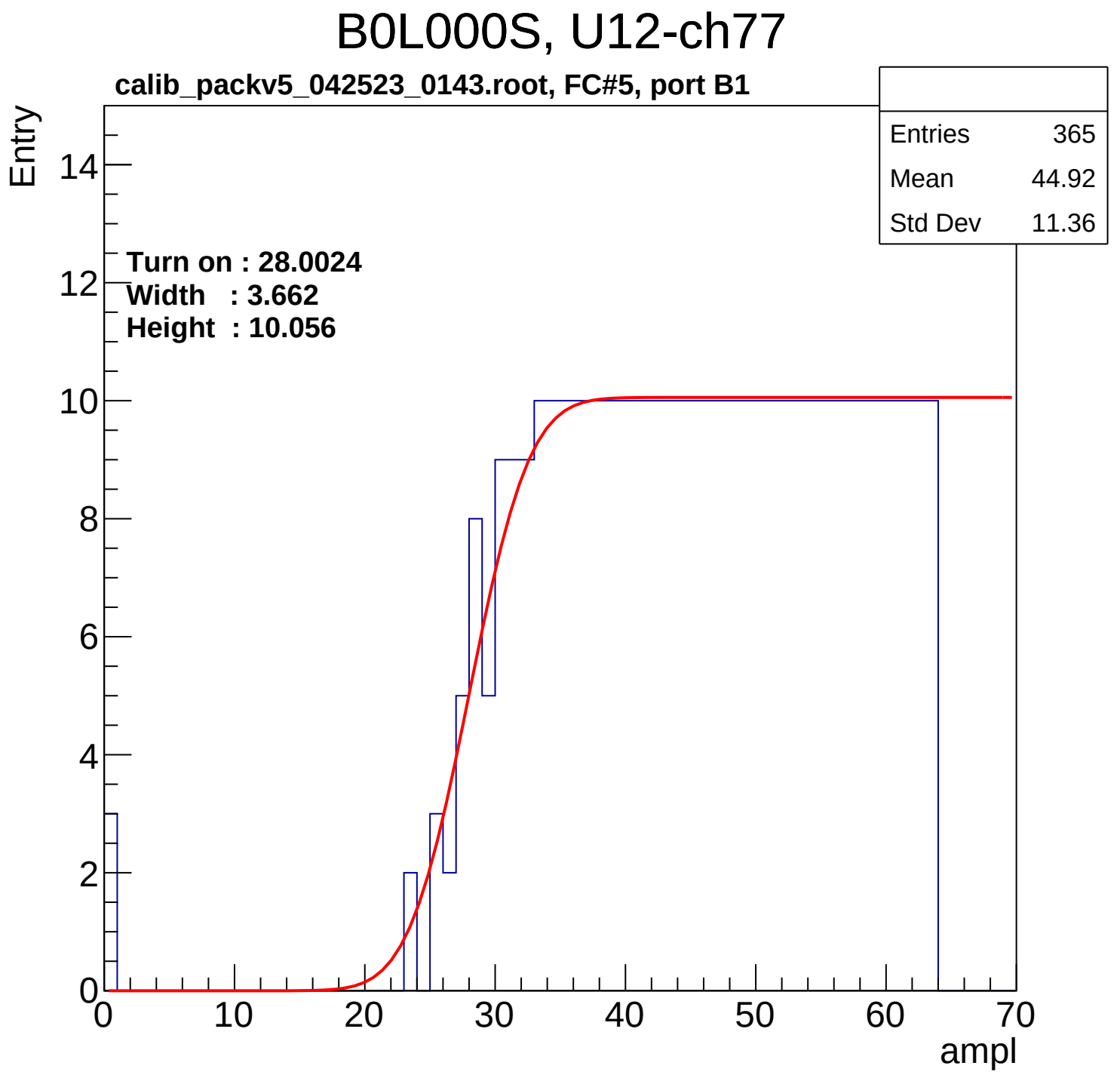
B0L000S, U12-ch77
calib_packv5_042523_0143.root, FC#5, port B1
Entries 365
Mean 44.92
Std Dev 11.36
Turn on : 28.0024
Width : 3.662
Height : 10.056
Entry
ampl
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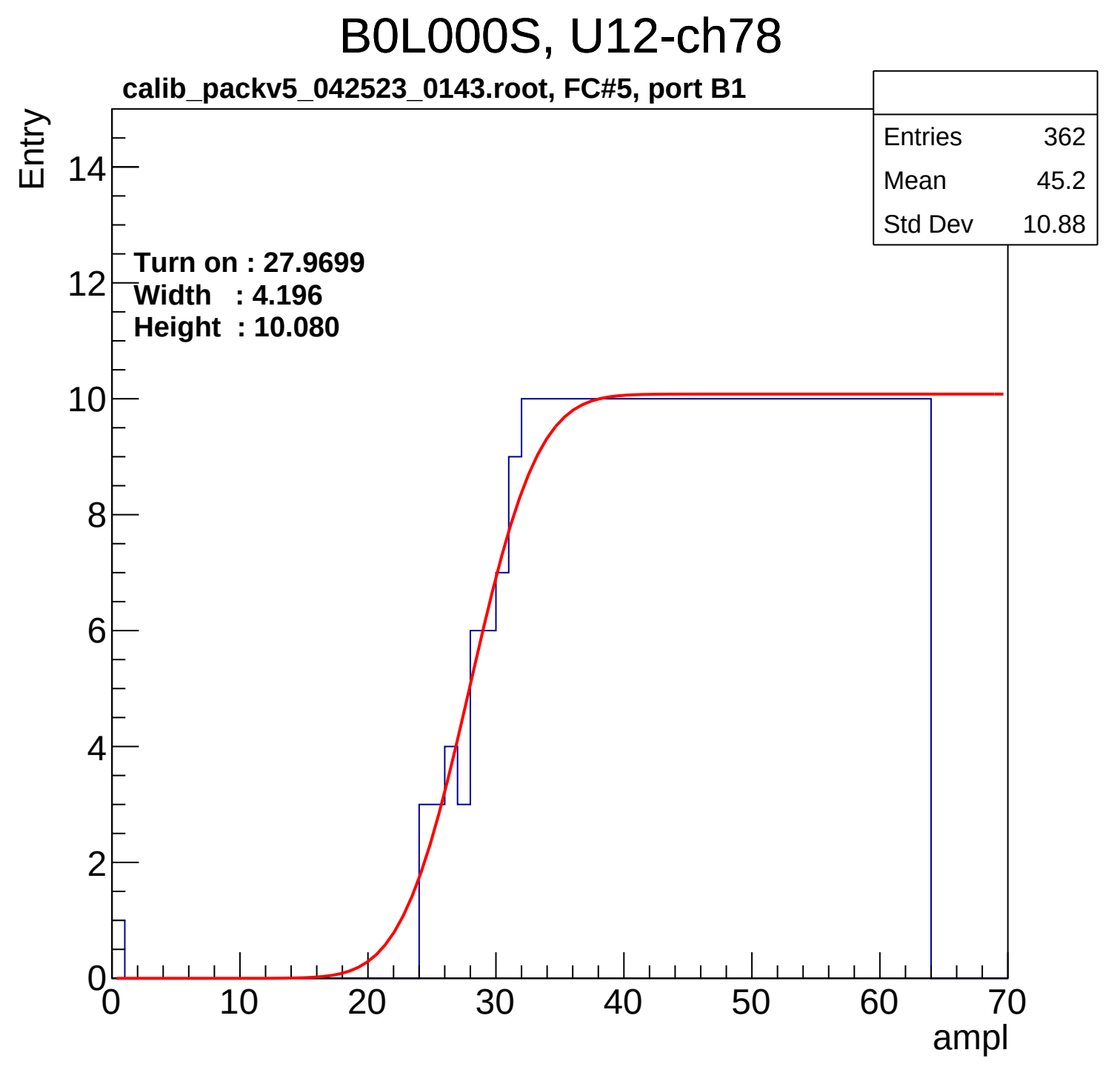
B0L000S, U12-ch78
calib_packv5_042523_0143.root, FC#5, port B1
Entries 362
Mean 45.2
Std Dev 10.88
Turn on : 27.9699
Width : 4.196
Height : 10.080
Entry
ampl
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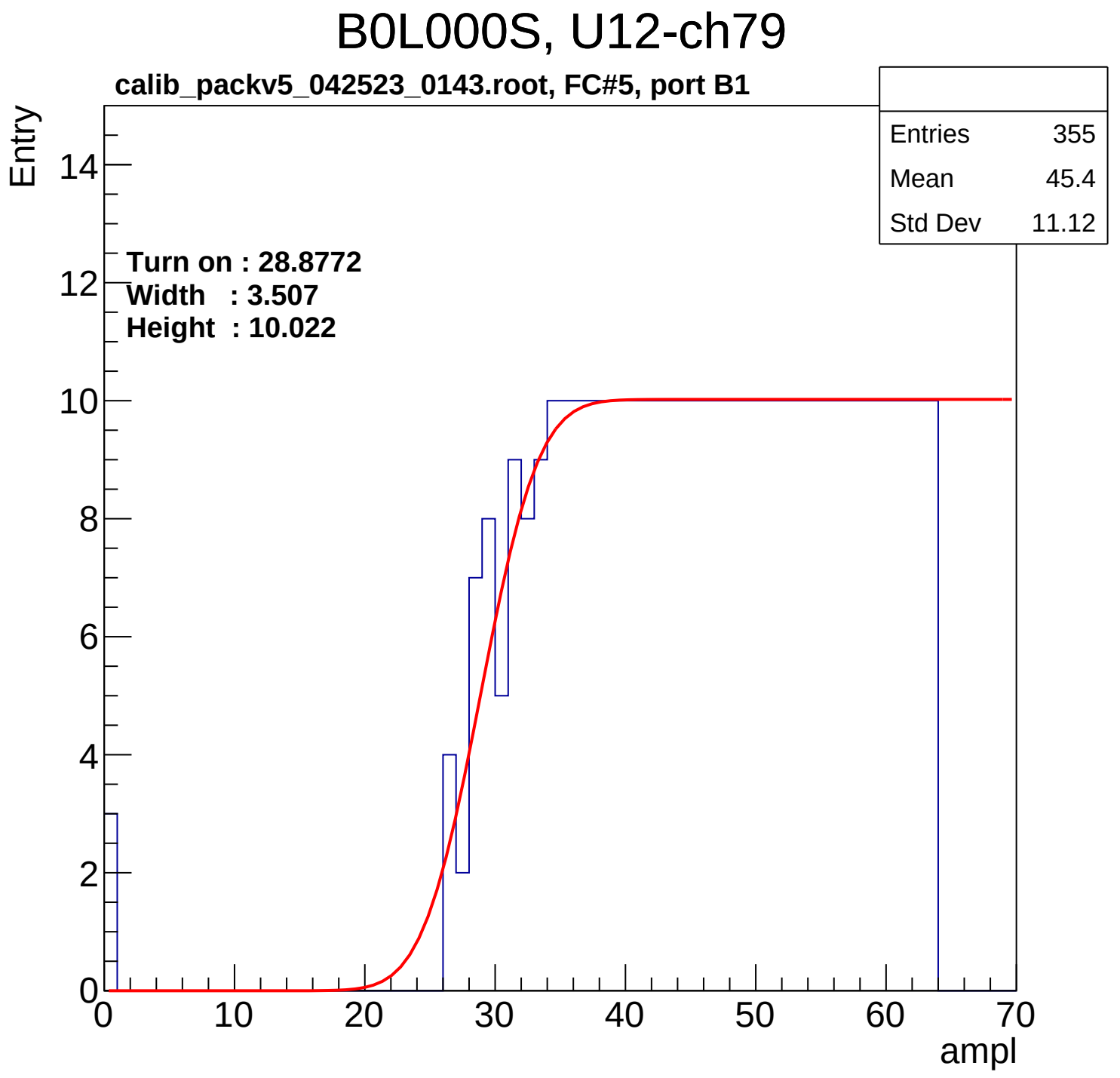
B0L000S, U12-ch79
calib_packv5_042523_0143.root, FC#5, port B1
Entries 355
Mean 45.4
Std Dev 11.12
Turn on : 28.8772
Width : 3.507
Height : 10.022
Entry
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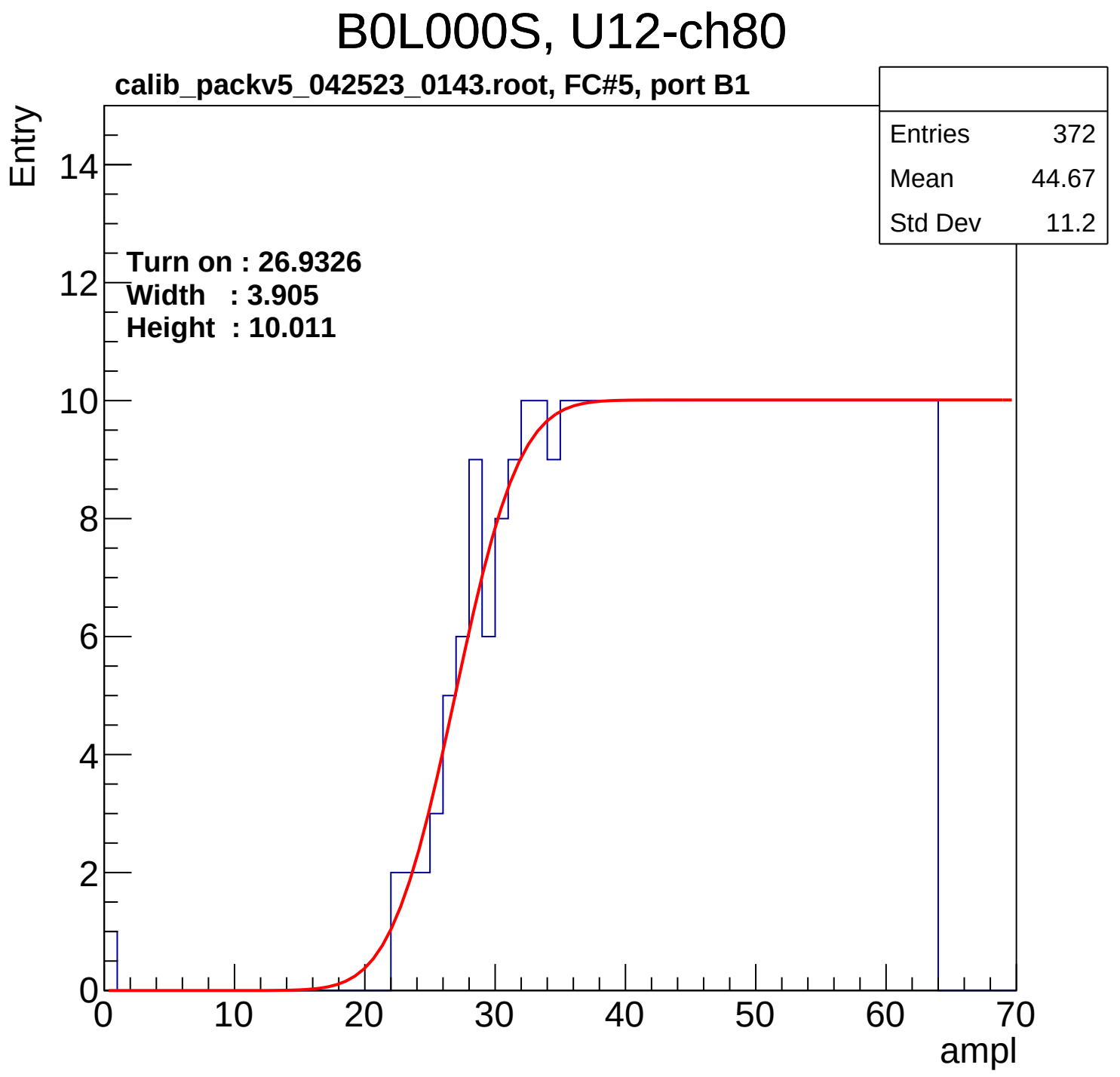
B0L000S, U12-ch80
calib_packv5_042523_0143.root, FC#5, port B1
Entries 372
Mean 44.67
Std Dev 11.2
Turn on : 26.9326
Width : 3.905
Height : 10.011
Entry
ampl
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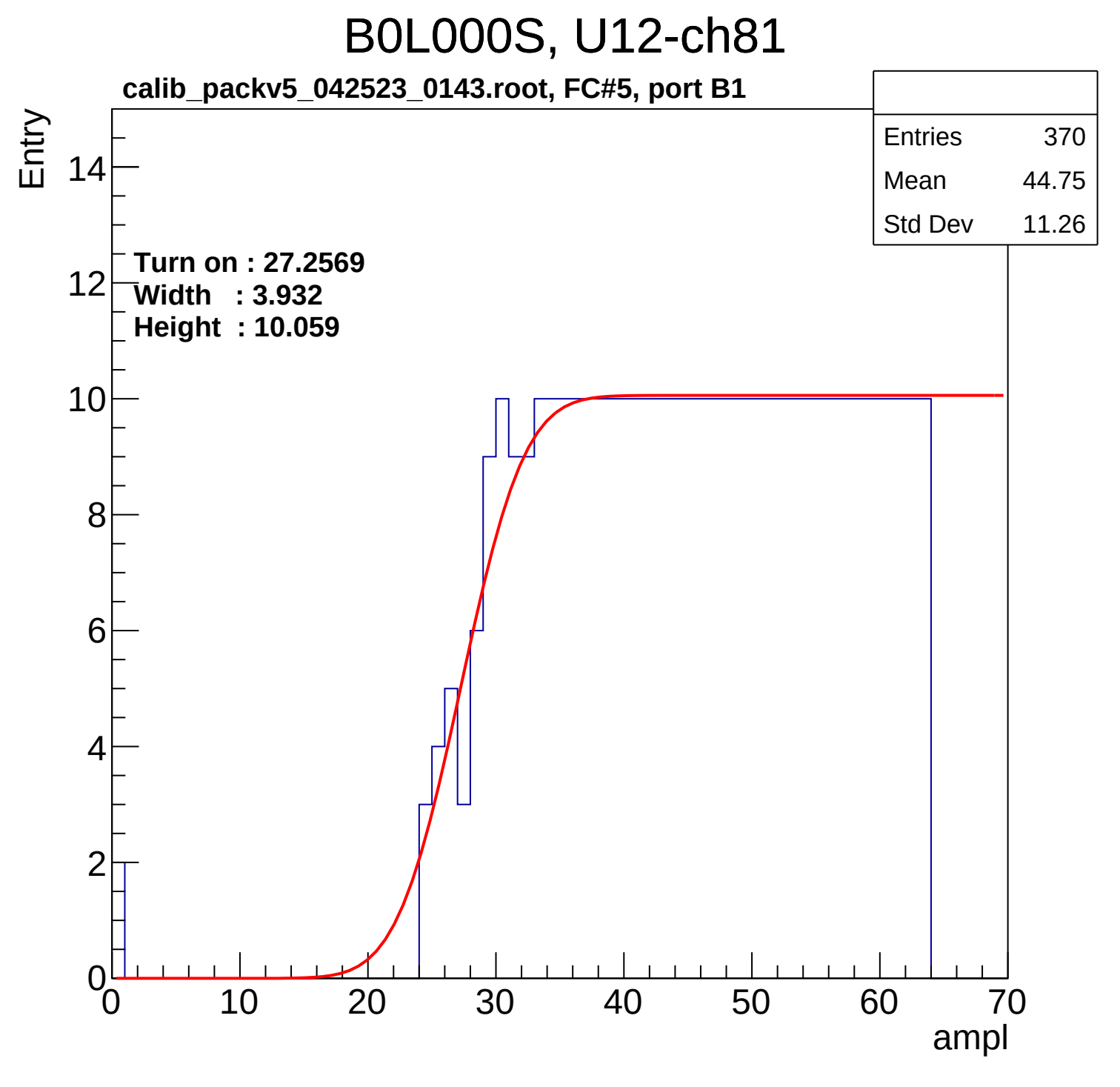
B0L000S, U12-ch81
calib_packv5_042523_0143.root, FC#5, port B1
Entries 370
Mean 44.75
Std Dev 11.26
Turn on : 27.2569
Width : 3.932
Height : 10.059
Entry
ampl
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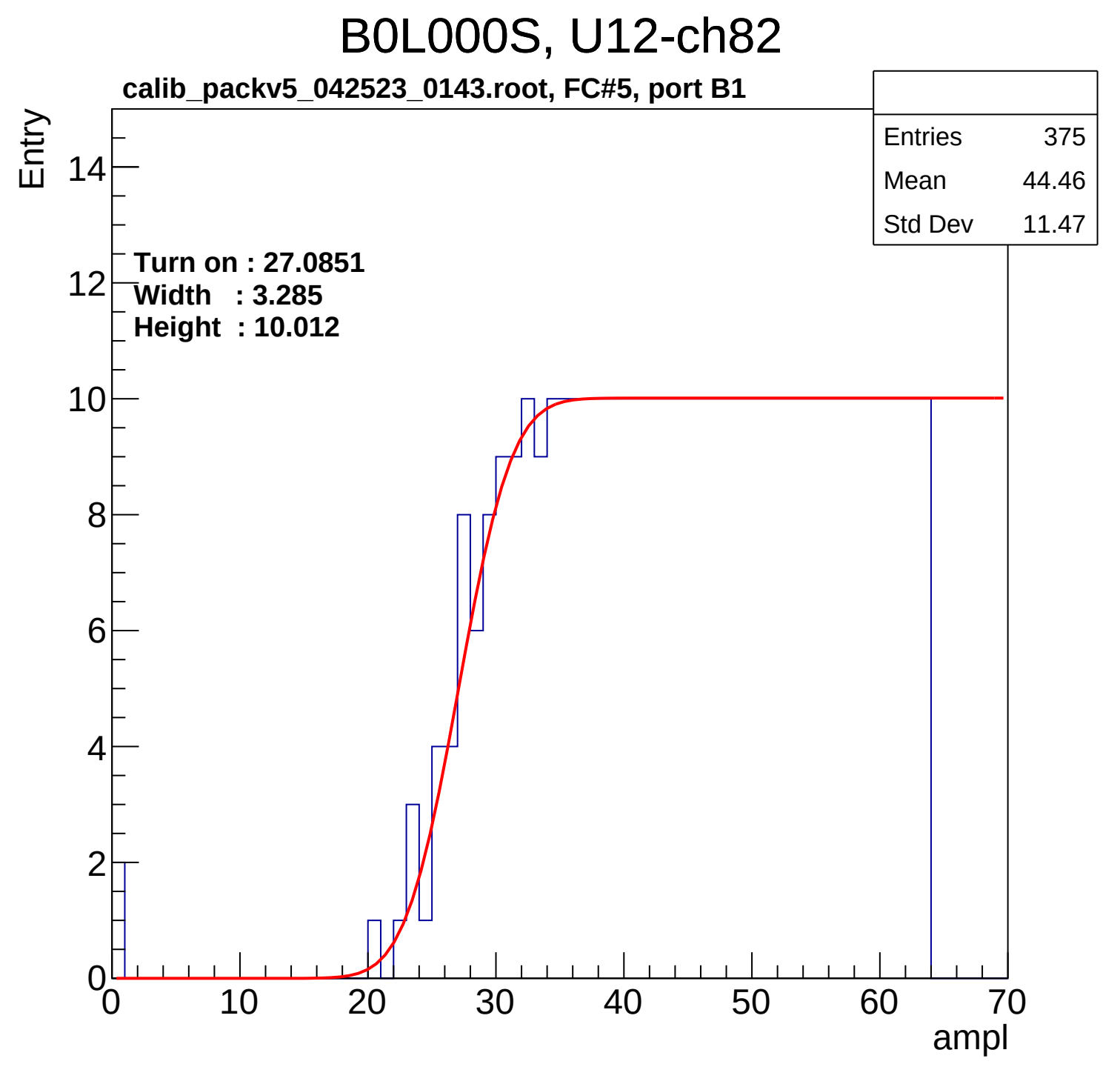
B0L000S, U12-ch82
calib_packv5_042523_0143.root, FC#5, port B1
Entries 375
Mean 44.46
Std Dev 11.47
Turn on : 27.0851
Width : 3.285
Height : 10.012
Entry
ampl
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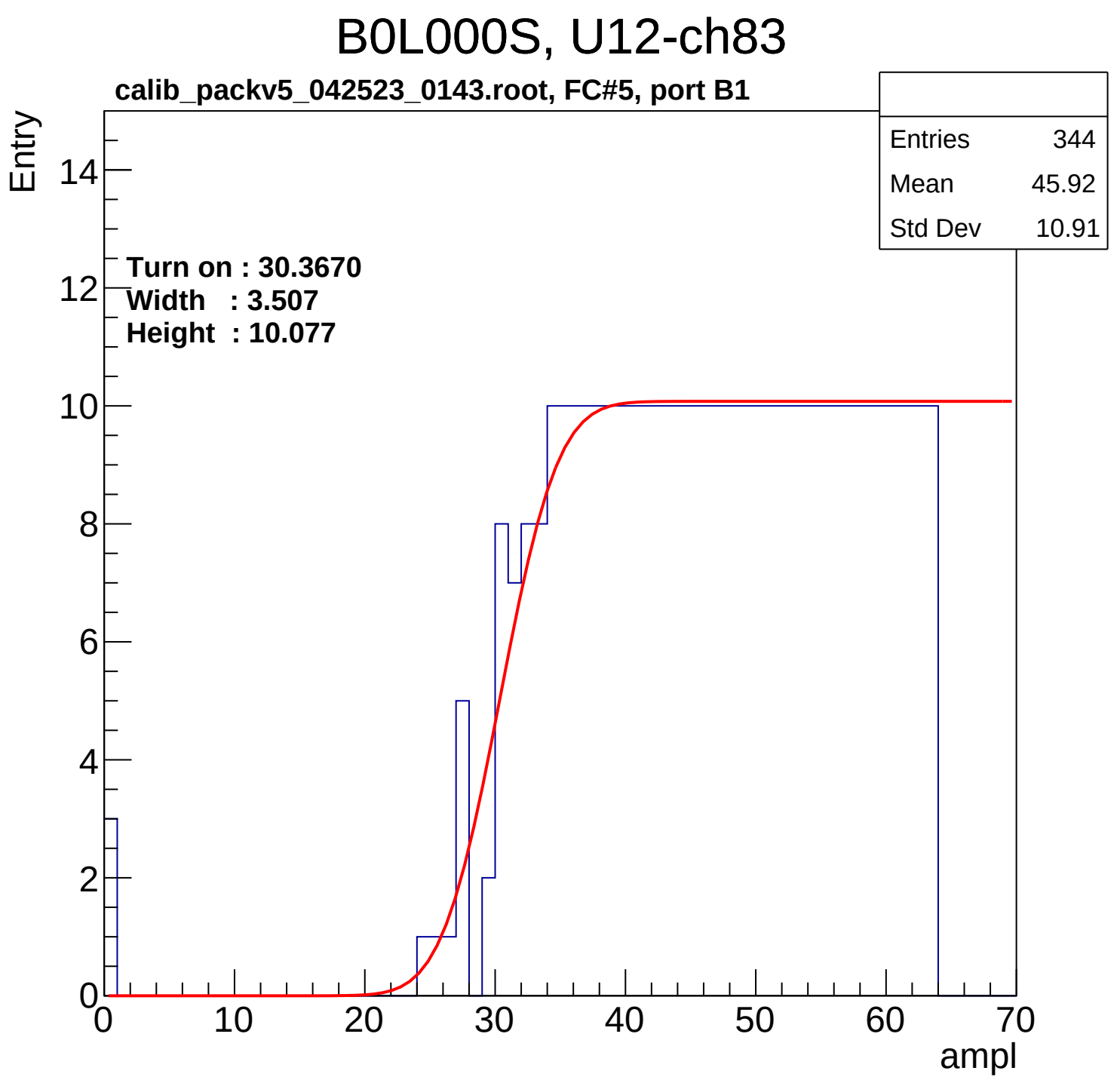
B0L000S, U12-ch83
calib_packv5_042523_0143.root, FC#5, port B1
Entries 344
Mean 45.92
Std Dev 10.91
Turn on : 30.3670
Width : 3.507
Height : 10.077
Entry
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6
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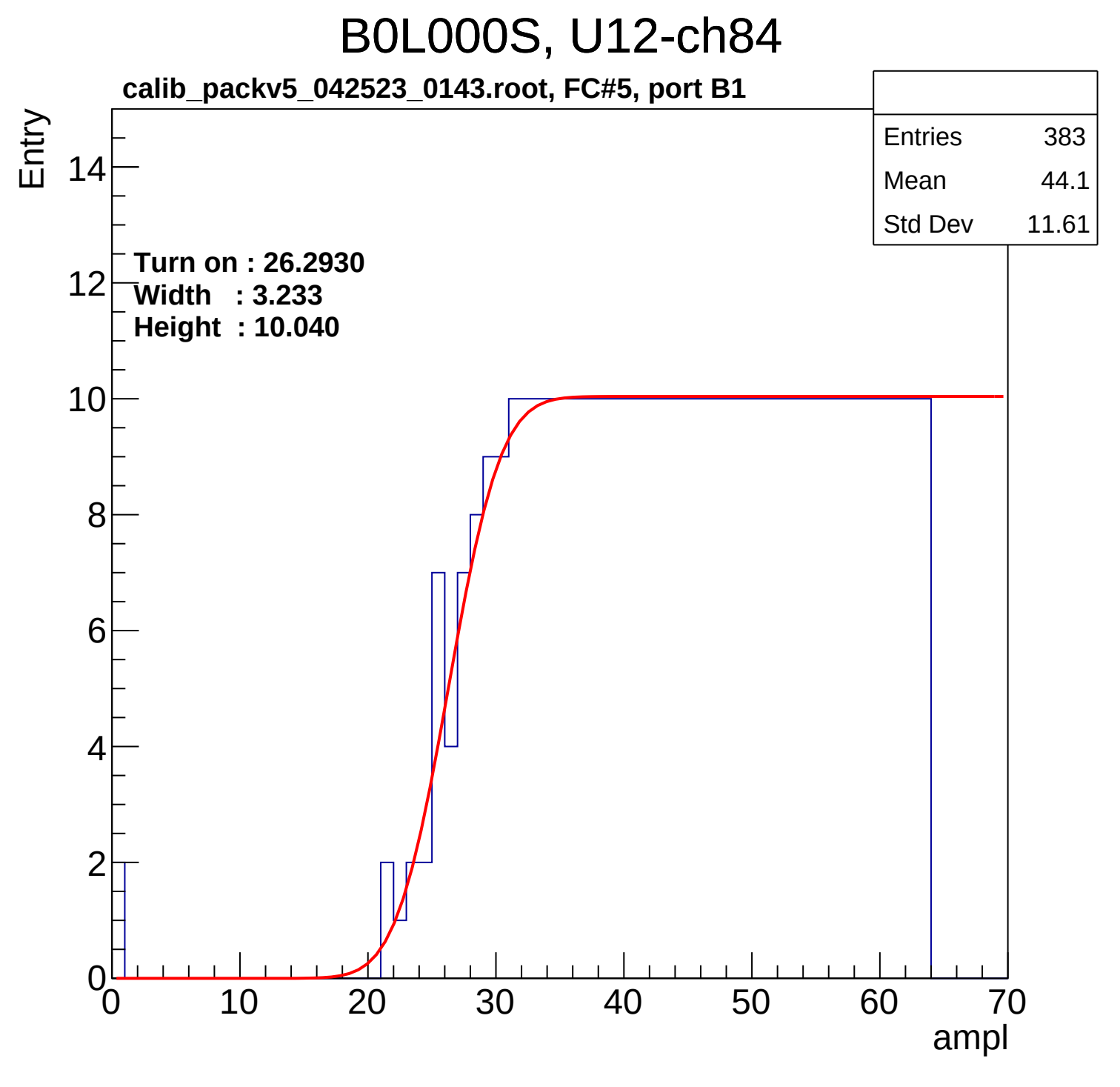
B0L000S, U12-ch84
calib_packv5_042523_0143.root, FC#5, port B1
Entries 383
Mean 44.1
Std Dev 11.61
Turn on : 26.2930
Width : 3.233
Height : 10.040
Entry
ampl
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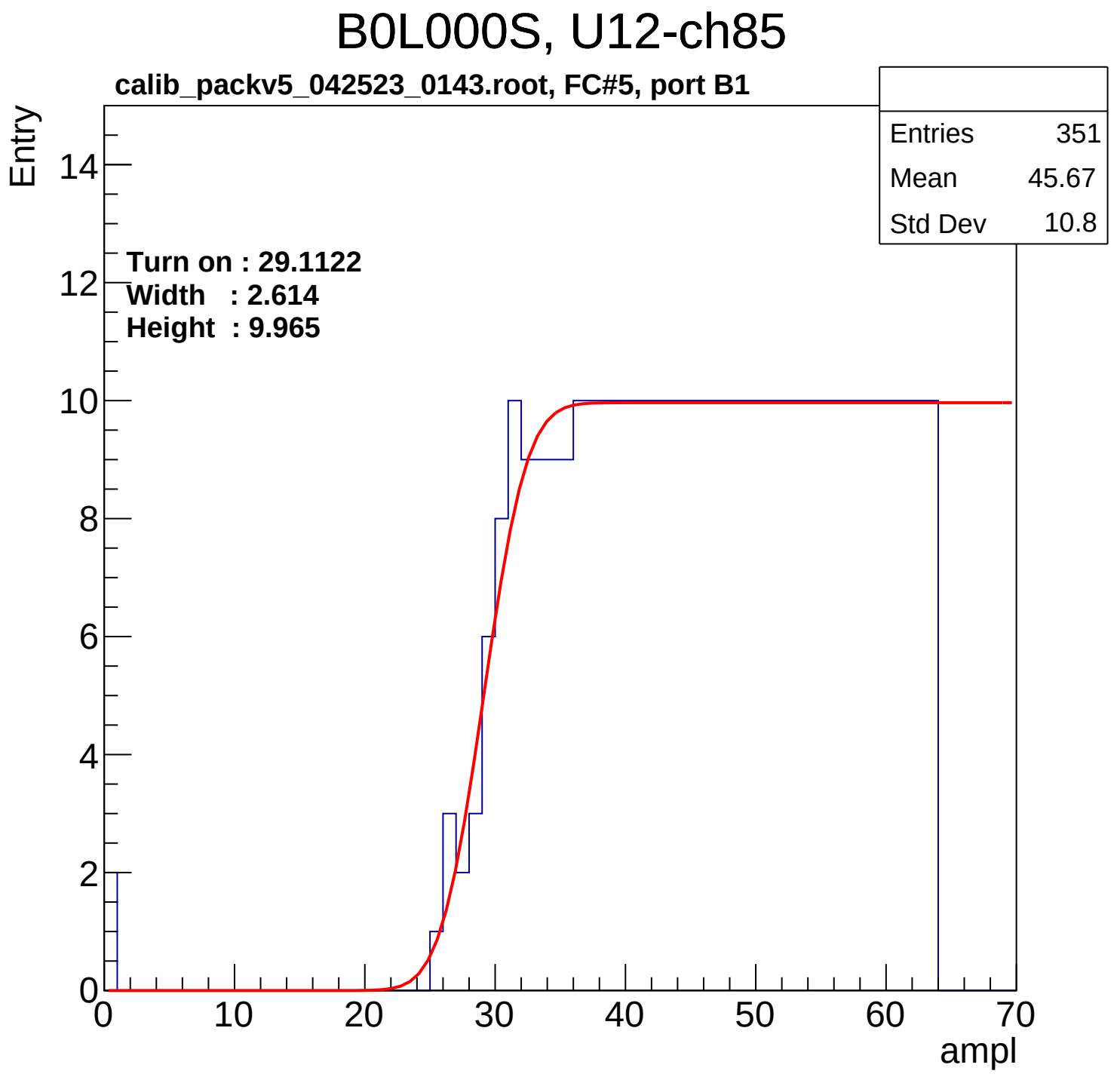
B0L000S, U12-ch85
calib_packv5_042523_0143.root, FC#5, port B1
Entries 351
Mean 45.67
Std Dev 10.8
Turn on : 29.1122
Width : 2.614
Height : 9.965
Entry
ampl
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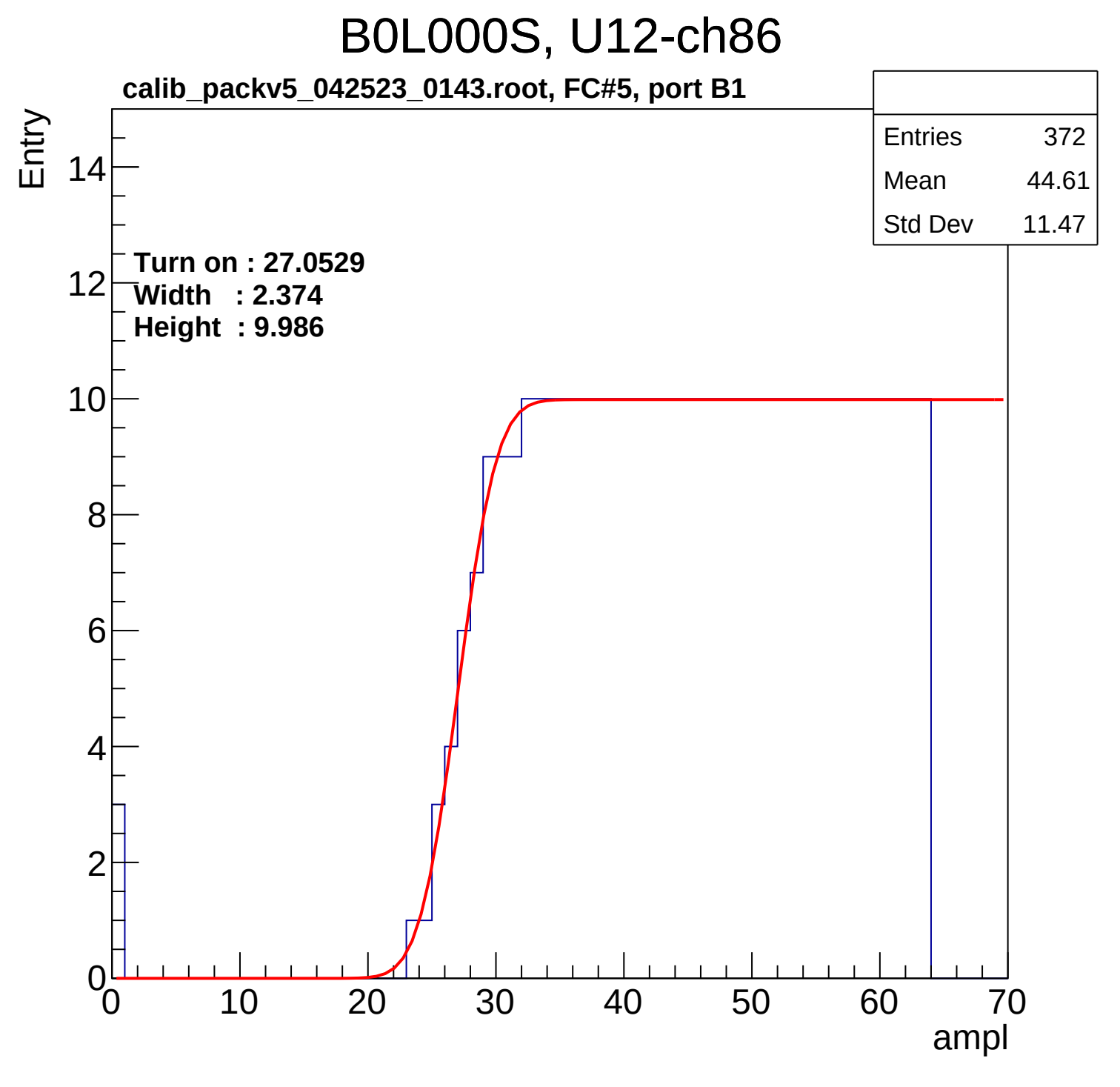
B0L000S, U12-ch86
calib_packv5_042523_0143.root, FC#5, port B1
Entries 372
Mean 44.61
Std Dev 11.47
Turn on : 27.0529
Width : 2.374
Height : 9.986
Entry
ampl
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6
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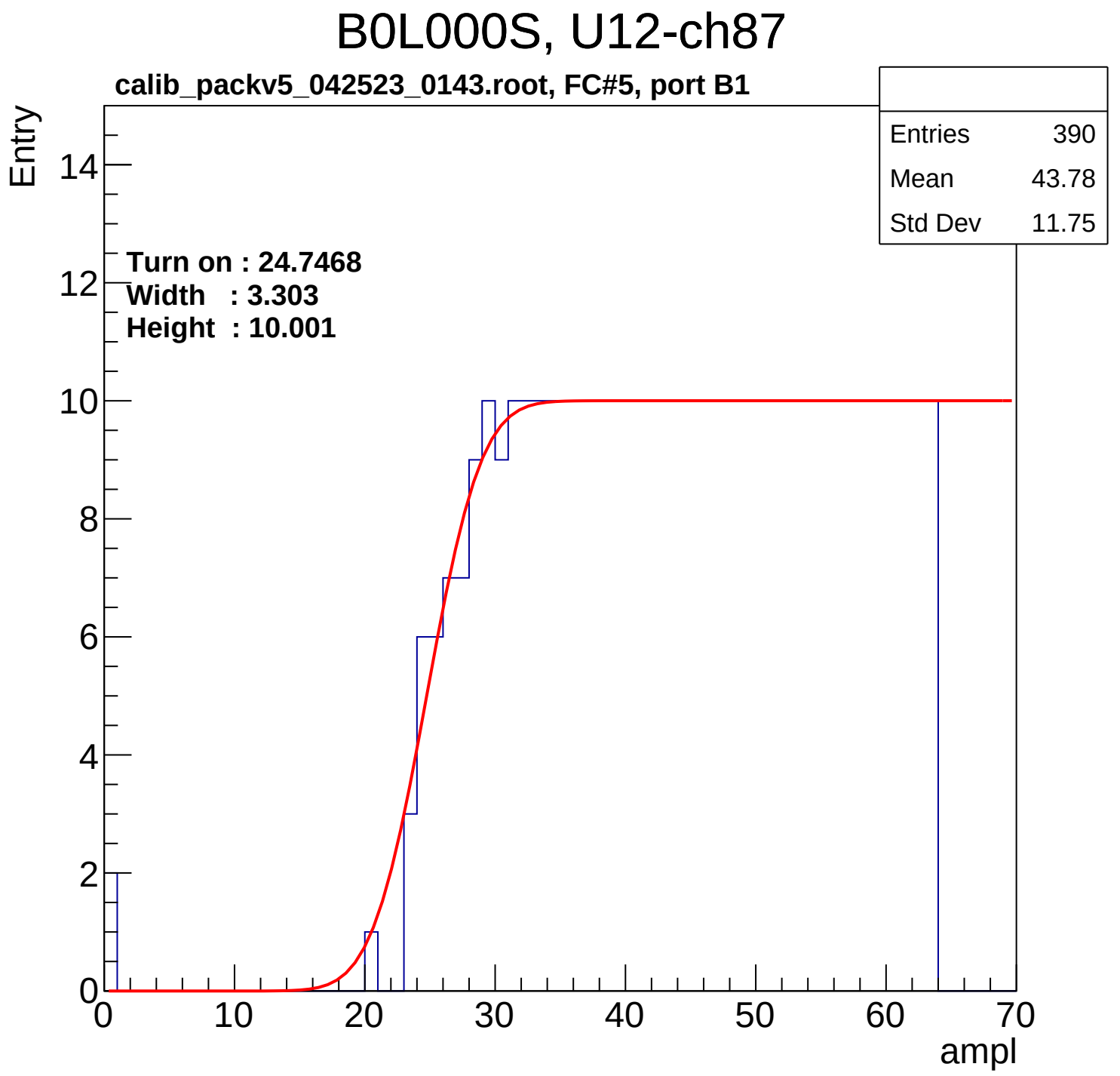
B0L000S, U12-ch87
calib_packv5_042523_0143.root, FC#5, port B1
Entries 390
Mean 43.78
Std Dev 11.75
Turn on : 24.7468
Width : 3.303
Height : 10.001
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ampl
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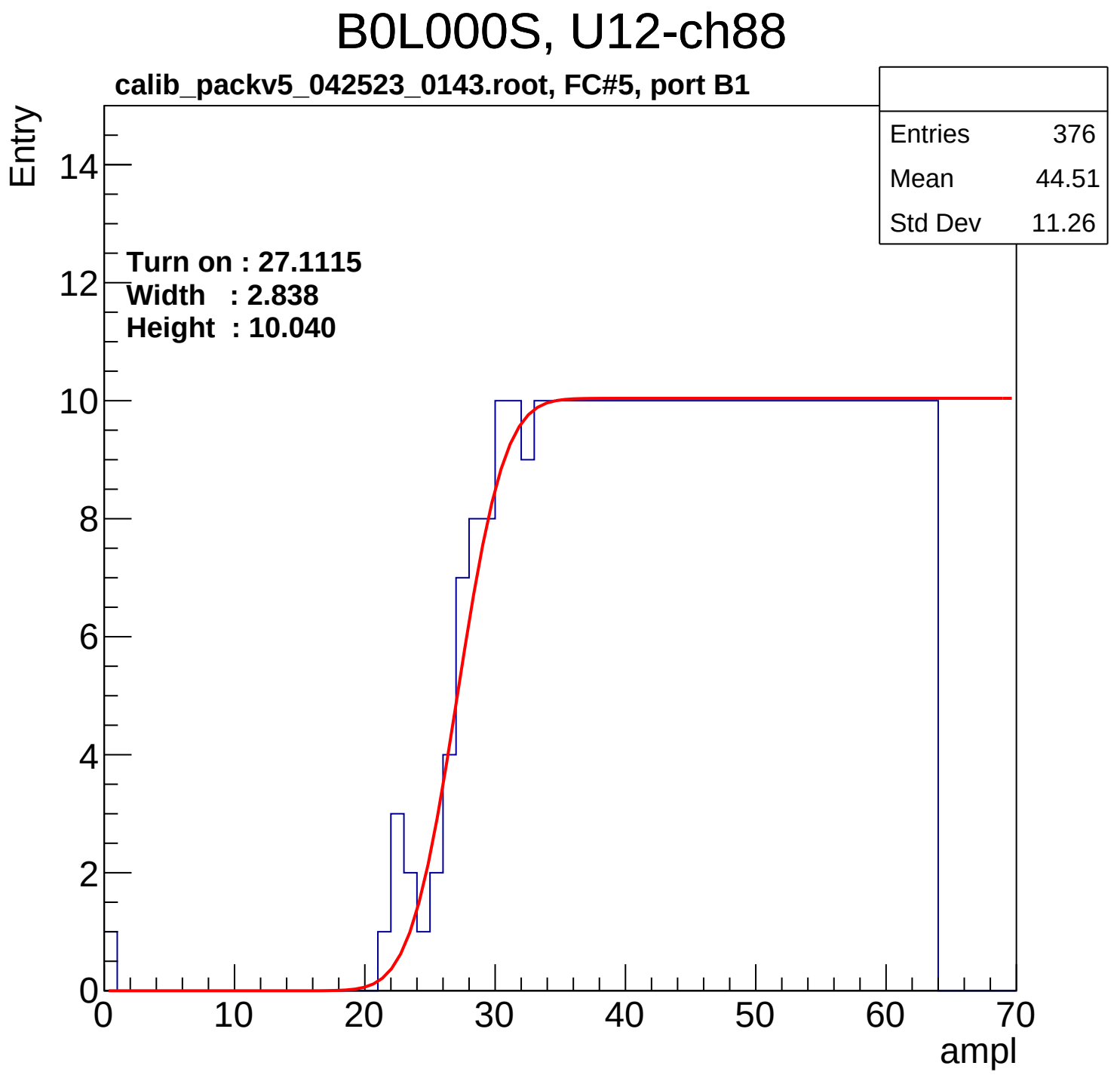
B0L000S, U12-ch88
calib_packv5_042523_0143.root, FC#5, port B1
Entries 376
Mean 44.51
Std Dev 11.26
Turn on : 27.1115
Width : 2.838
Height : 10.040
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ampl
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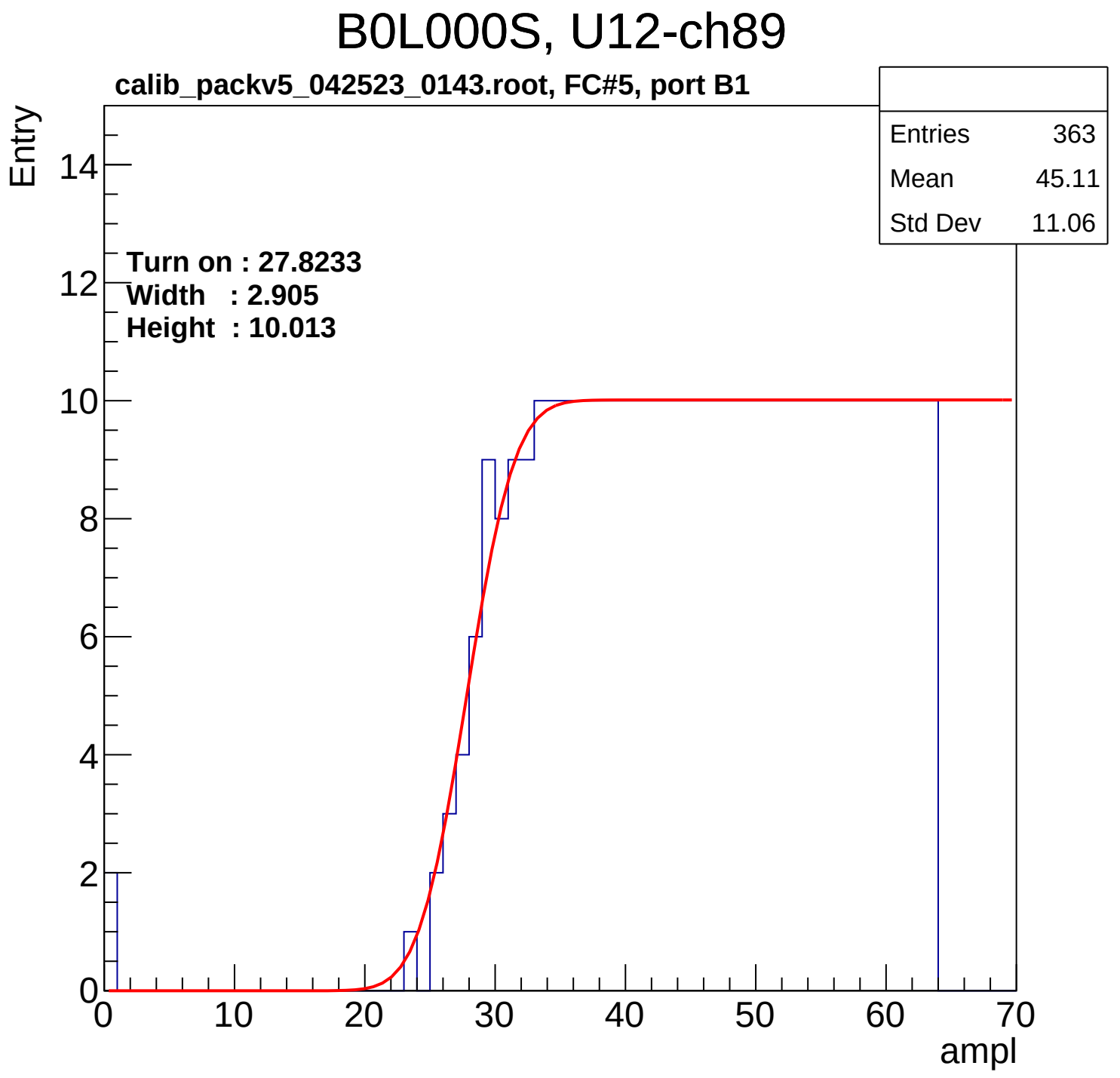
B0L000S, U12-ch89
calib_packv5_042523_0143.root, FC#5, port B1
Entries 363
Mean 45.11
Std Dev 11.06
Turn on : 27.8233
Width : 2.905
Height : 10.013
Entry
ampl
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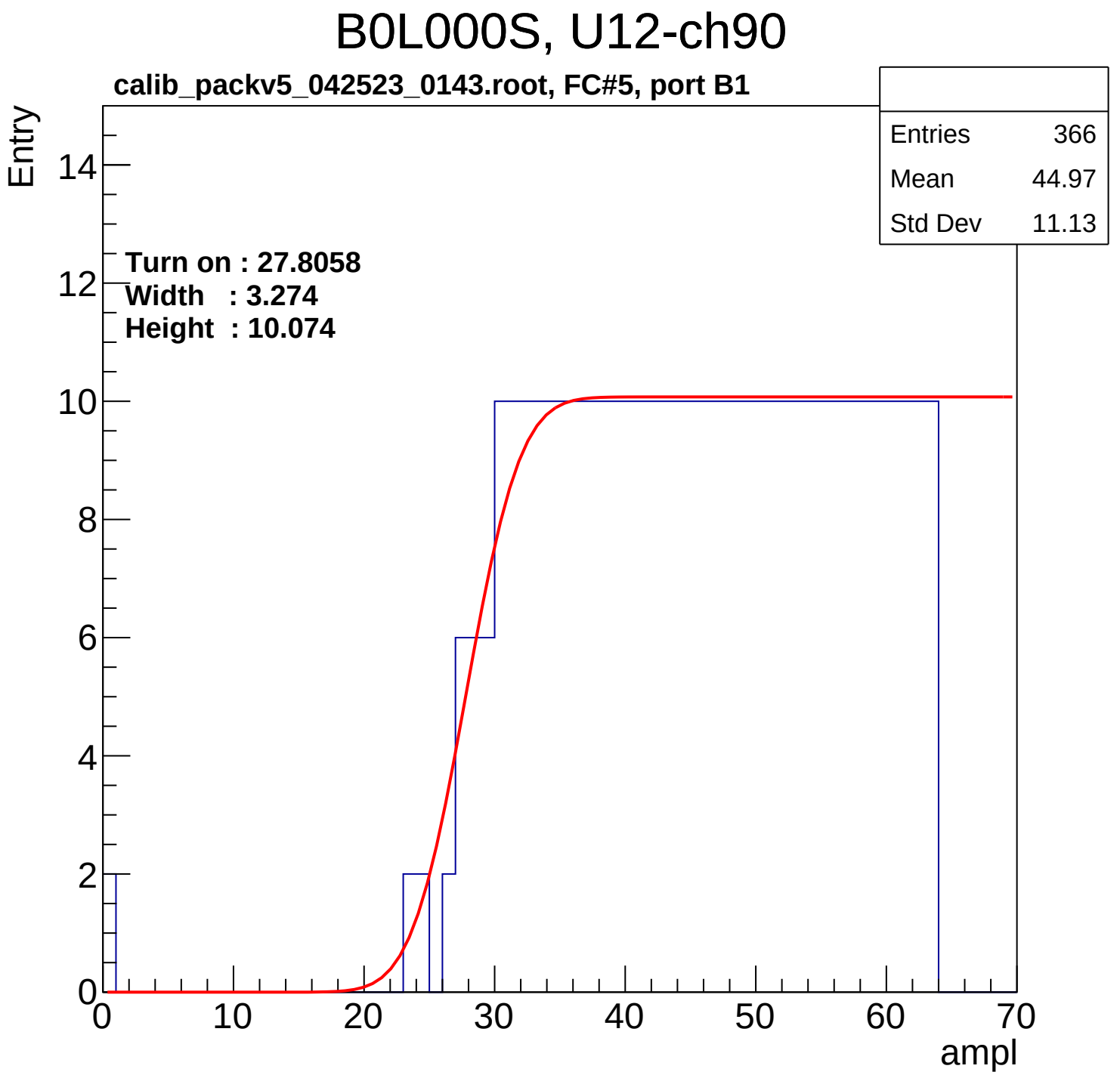
B0L000S, U12-ch90
calib_packv5_042523_0143.root, FC#5, port B1
Entries 366
Mean 44.97
Std Dev 11.13
Turn on : 27.8058
Width : 3.274
Height : 10.074
Entry
ampl
0
2
4
6
8
10
12
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0
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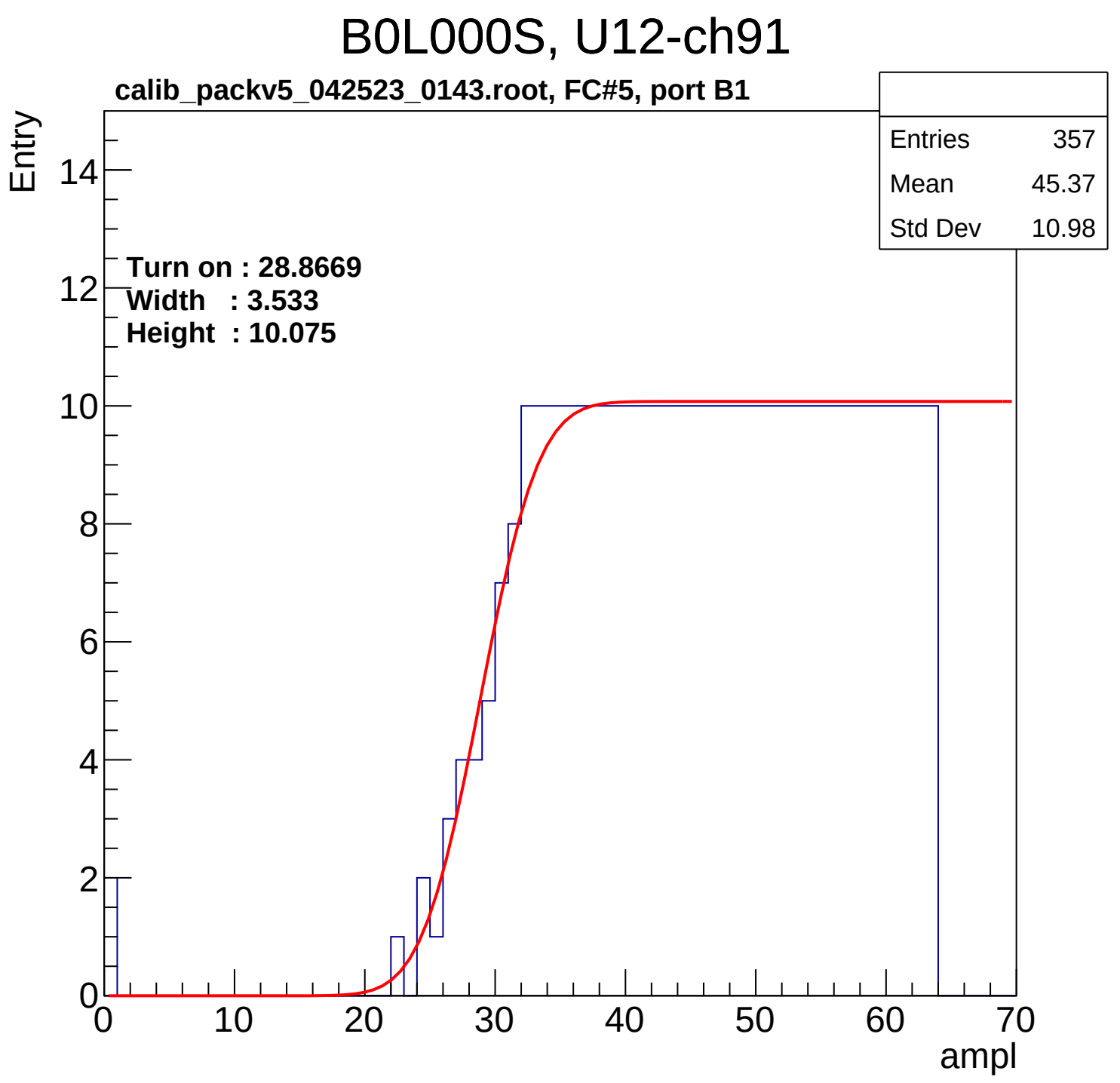
B0L000S, U12-ch91
calib_packv5_042523_0143.root, FC#5, port B1
Entries 357
Mean 45.37
Std Dev 10.98
Turn on : 28.8669
Width : 3.533
Height : 10.075
Entry
ampl
0
2
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6
8
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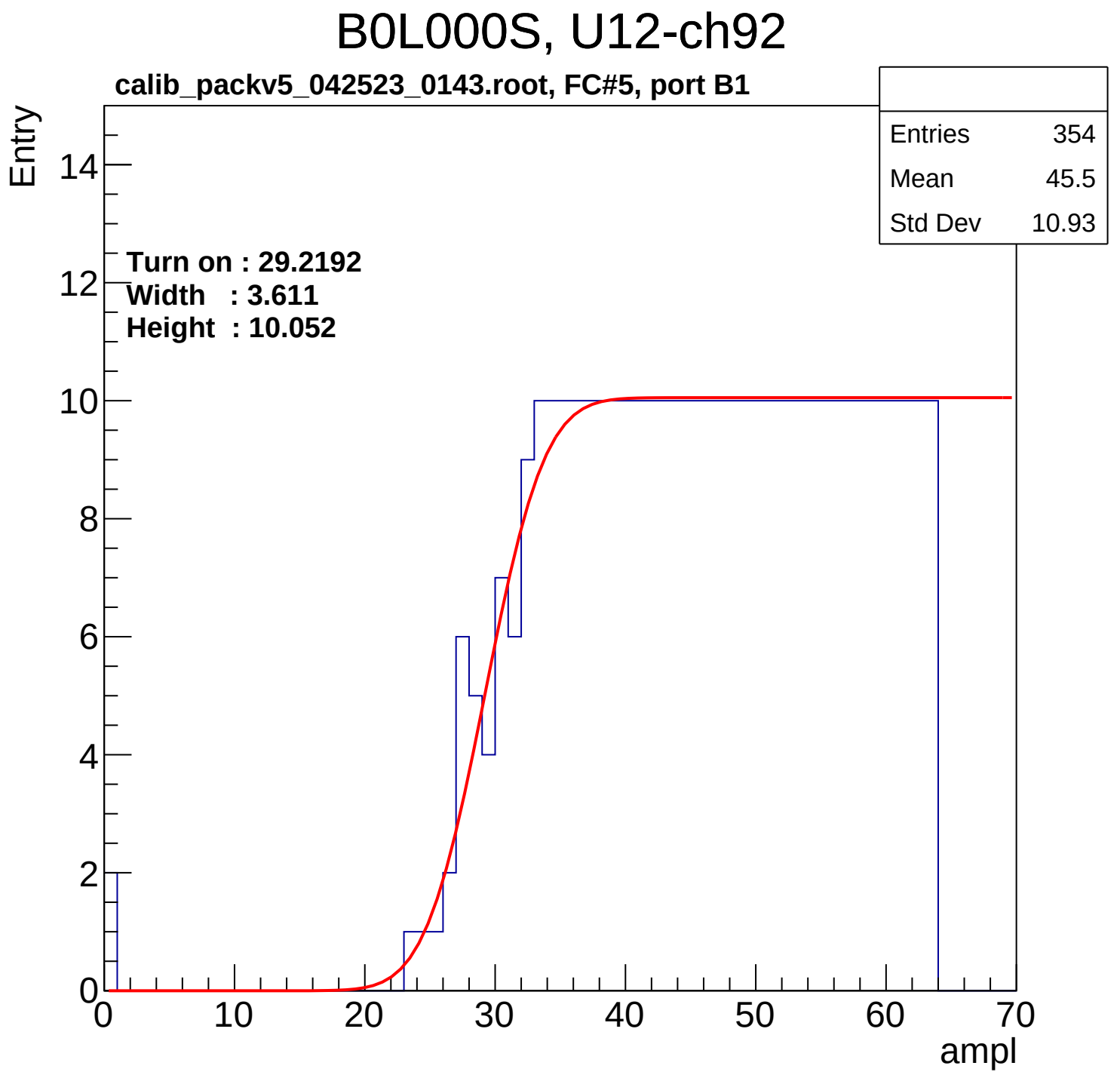
B0L000S, U12-ch92
calib_packv5_042523_0143.root, FC#5, port B1
Entries 354
Mean 45.5
Std Dev 10.93
Turn on : 29.2192
Width : 3.611
Height : 10.052
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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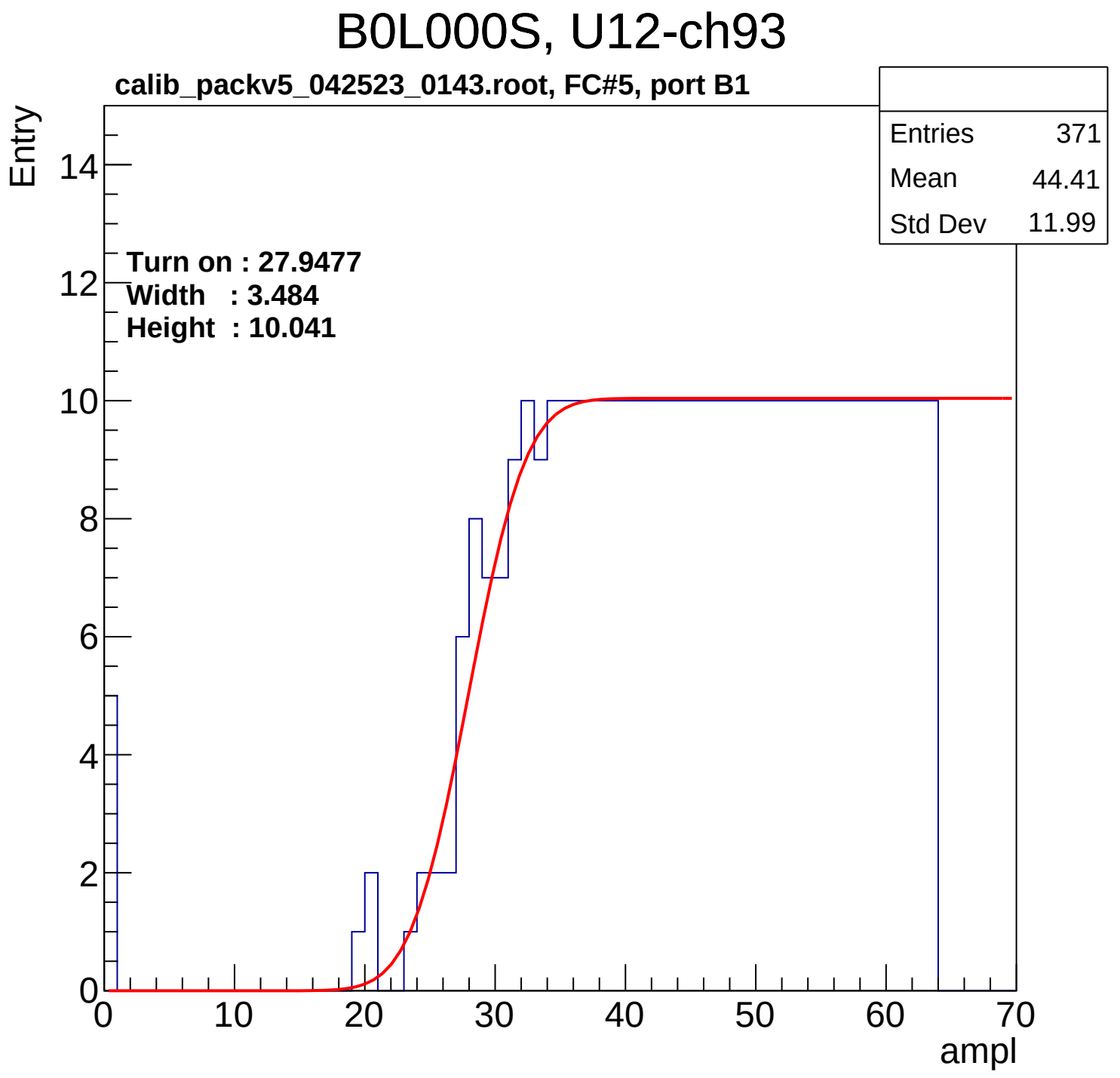
B0L000S, U12-ch93
calib_packv5_042523_0143.root, FC#5, port B1
Entries 371
Mean 44.41
Std Dev 11.99
Turn on : 27.9477
Width : 3.484
Height : 10.041
Entry
ampl
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4
6
8
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12
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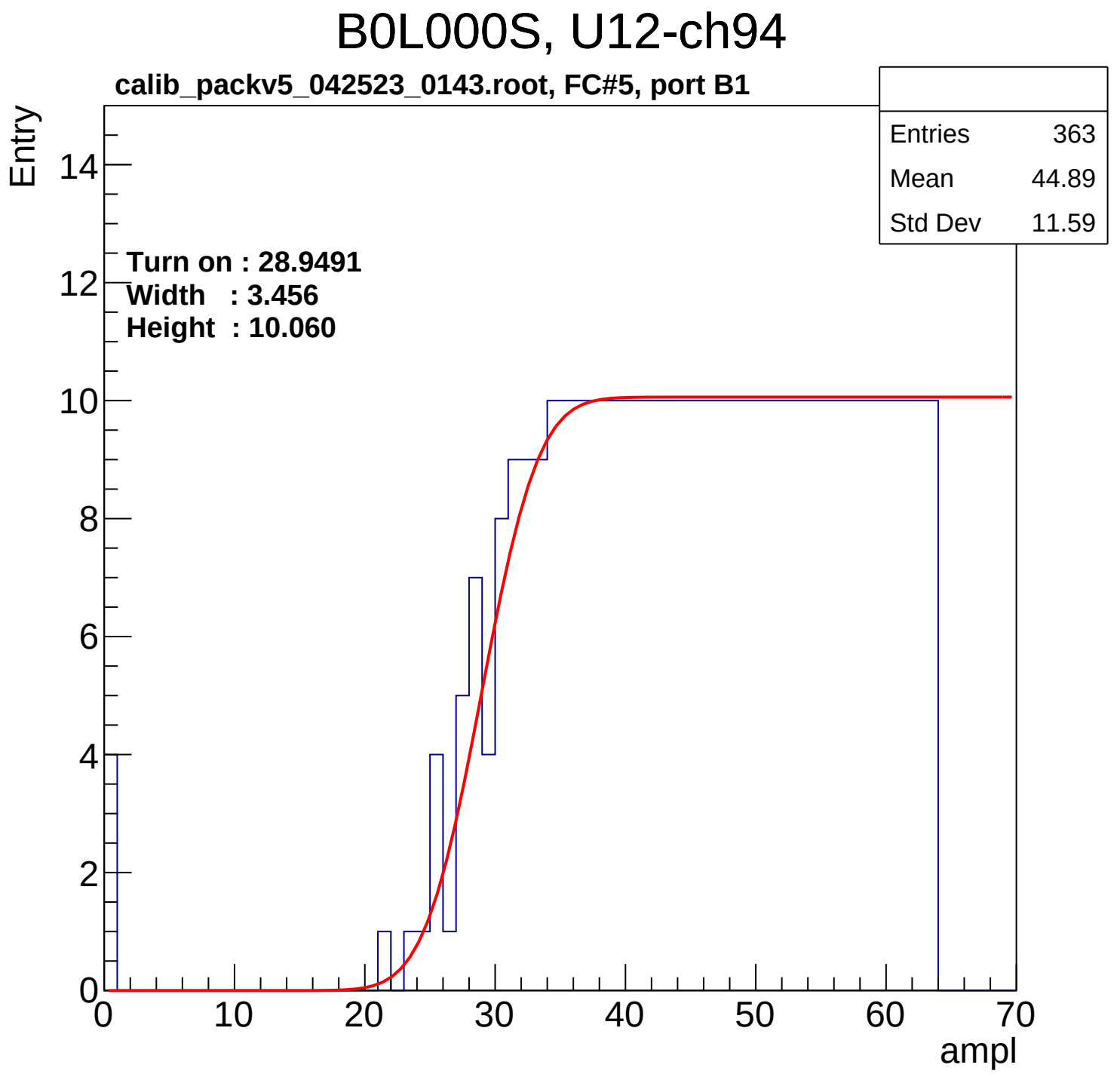
B0L000S, U12-ch94
calib_packv5_042523_0143.root, FC#5, port B1
Entries 363
Mean 44.89
Std Dev 11.59
Turn on : 28.9491
Width : 3.456
Height : 10.060
Entry
ampl
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2
4
6
8
10
12
14
0
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60
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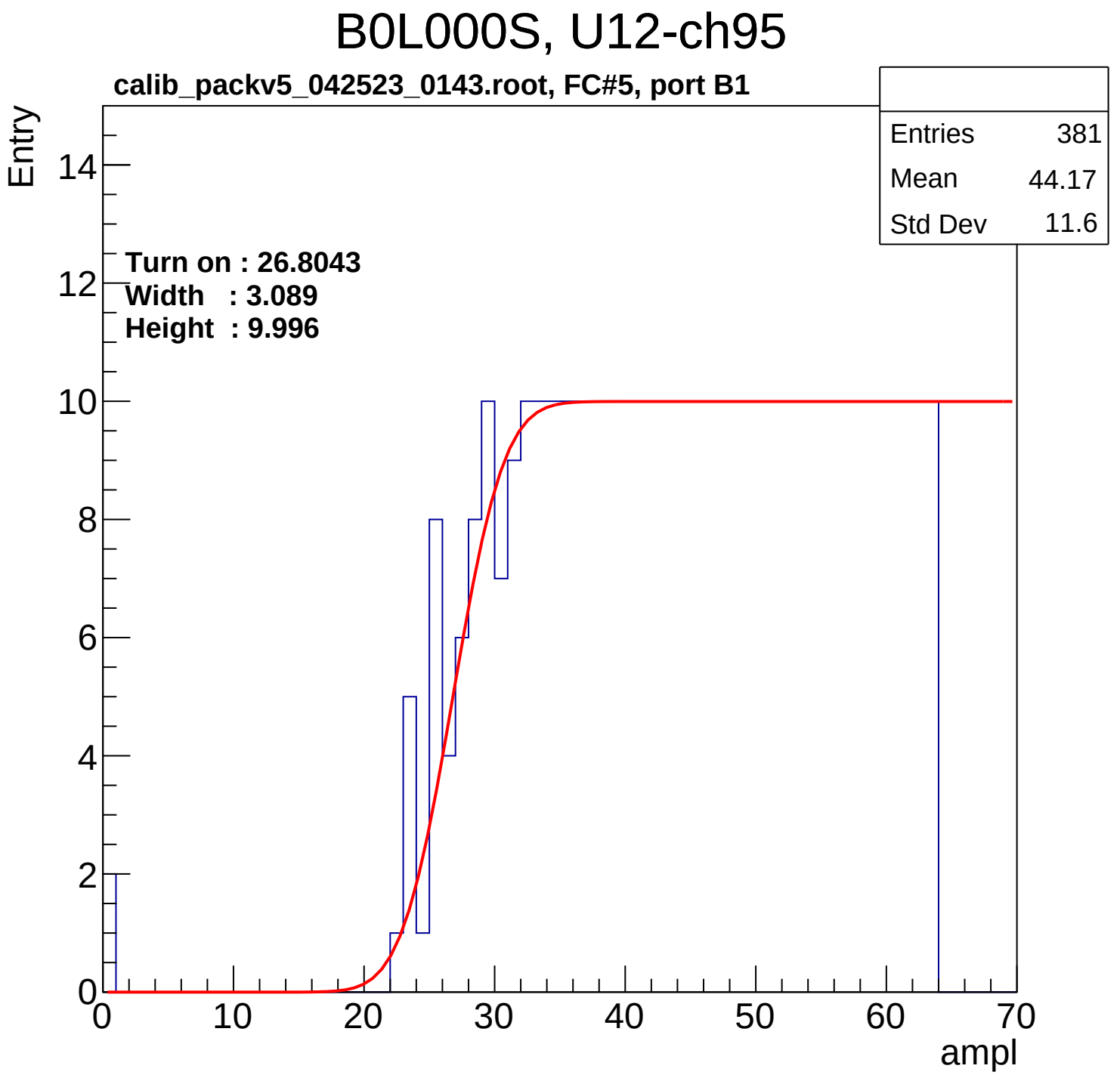
B0L000S, U12-ch95
calib_packv5_042523_0143.root, FC#5, port B1
Entries 381
Mean 44.17
Std Dev 11.6
Turn on : 26.8043
Width : 3.089
Height : 9.996
Entry
ampl
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2
4
6
8
10
12
14
0
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20
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40
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60
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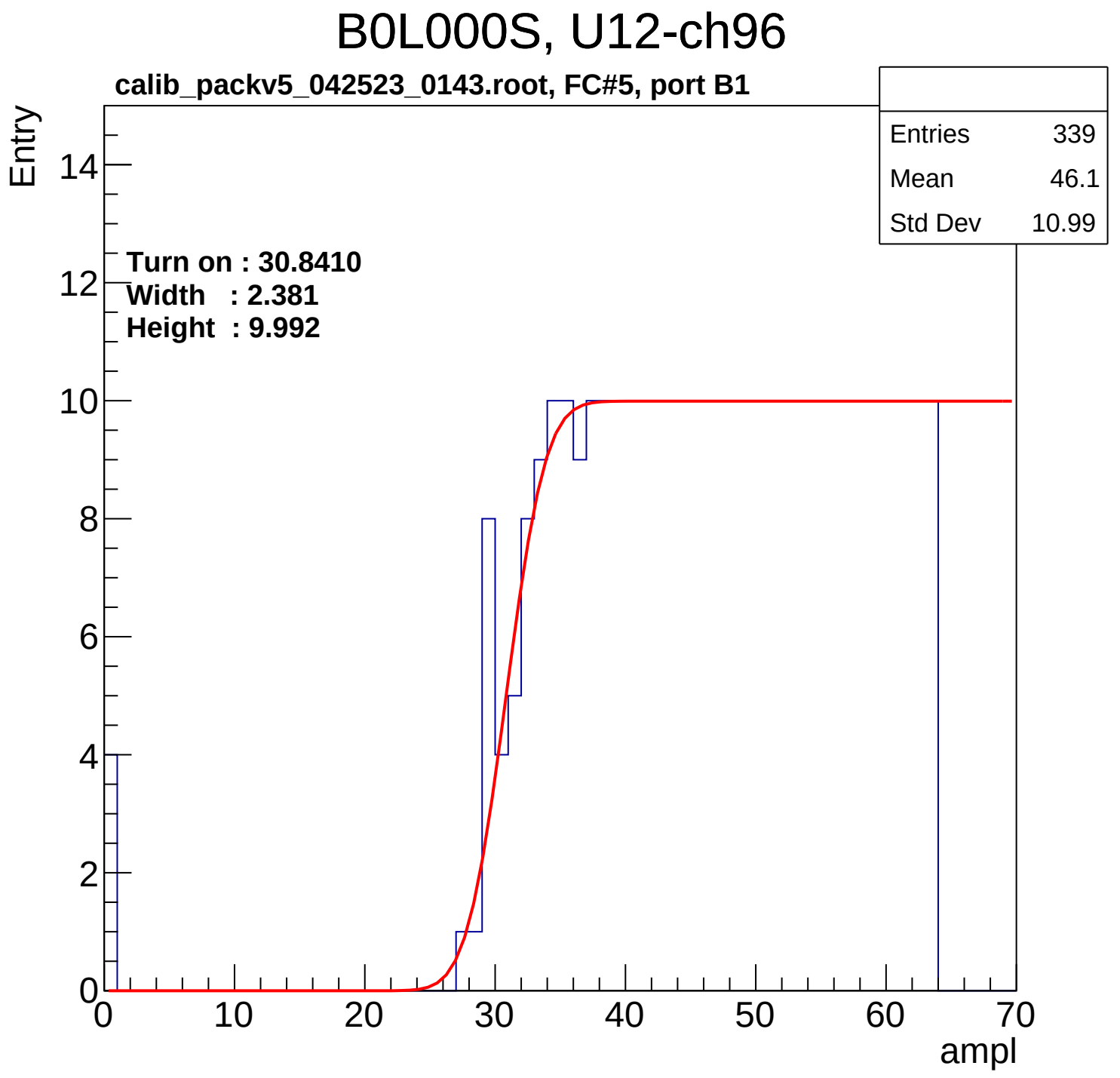
B0L000S, U12-ch96
calib_packv5_042523_0143.root, FC#5, port B1
Entries 339
Mean 46.1
Std Dev 10.99
Turn on : 30.8410
Width : 2.381
Height : 9.992
Entry
ampl
0
2
4
6
8
10
12
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0
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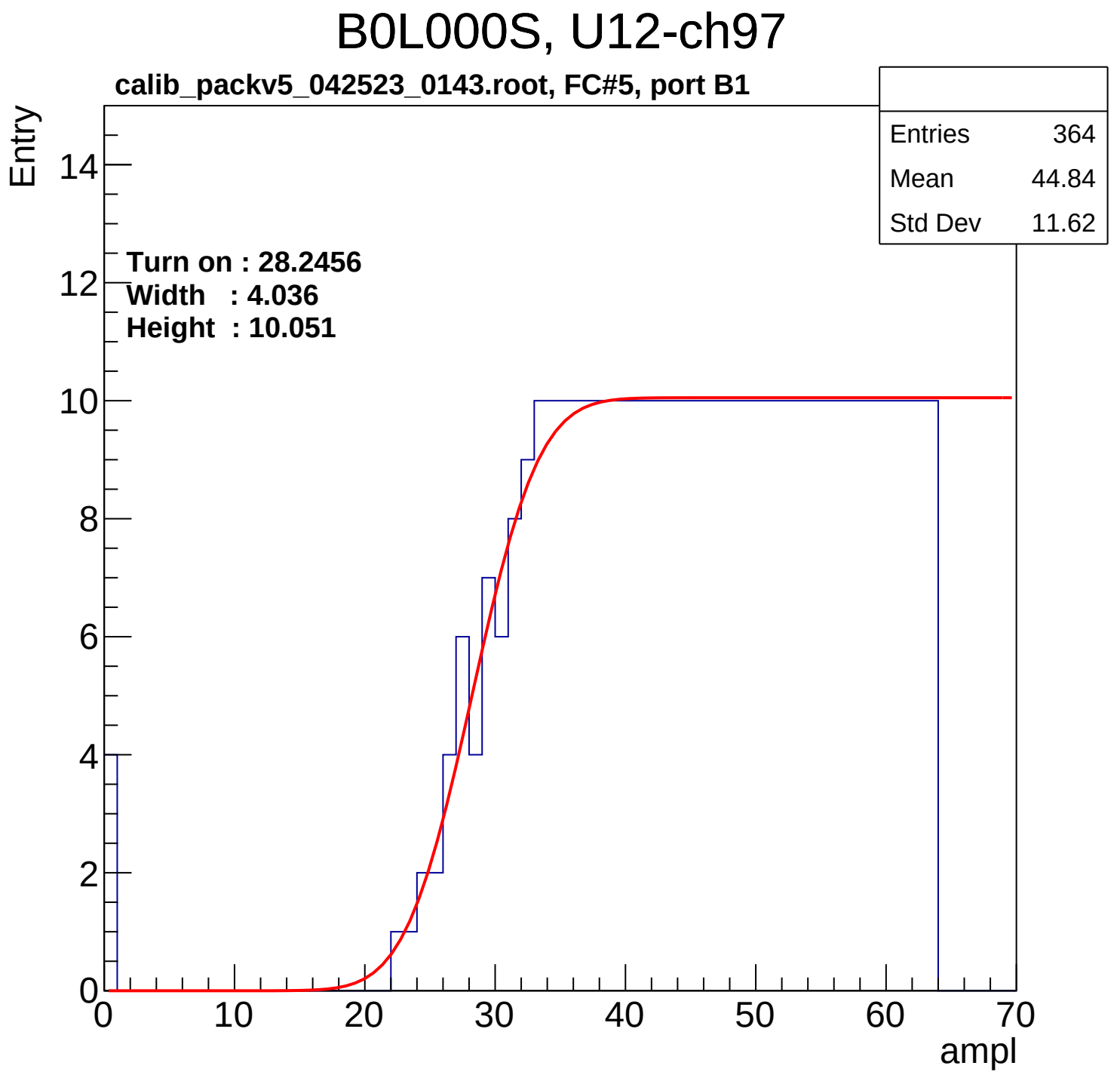
B0L000S, U12-ch97
calib_packv5_042523_0143.root, FC#5, port B1
Entries 364
Mean 44.84
Std Dev 11.62
Turn on : 28.2456
Width : 4.036
Height : 10.051
Entry
ampl
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6
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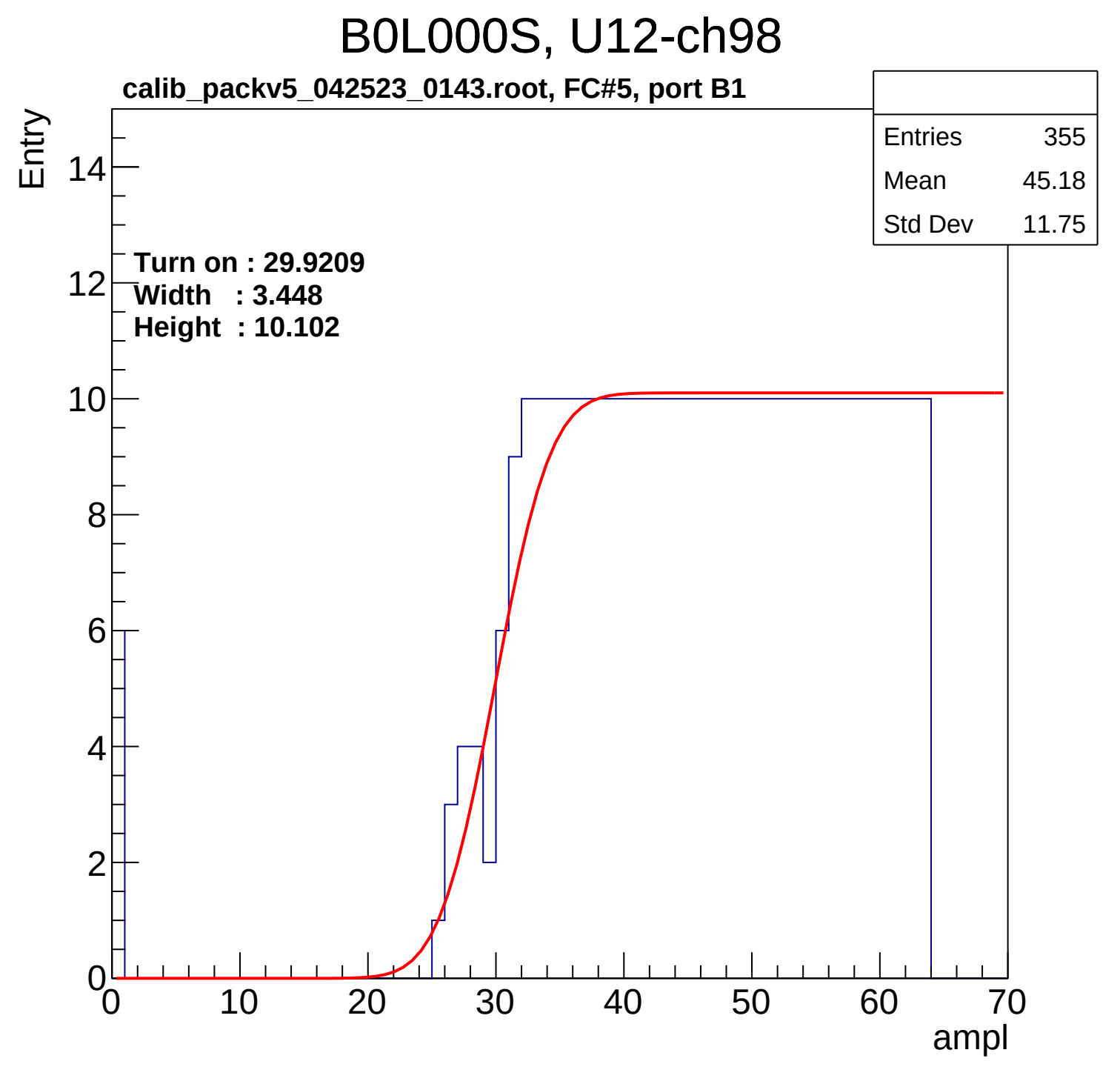
B0L000S, U12-ch98
calib_packv5_042523_0143.root, FC#5, port B1
Entries 355
Mean 45.18
Std Dev 11.75
Turn on : 29.9209
Width : 3.448
Height : 10.102
Entry
ampl
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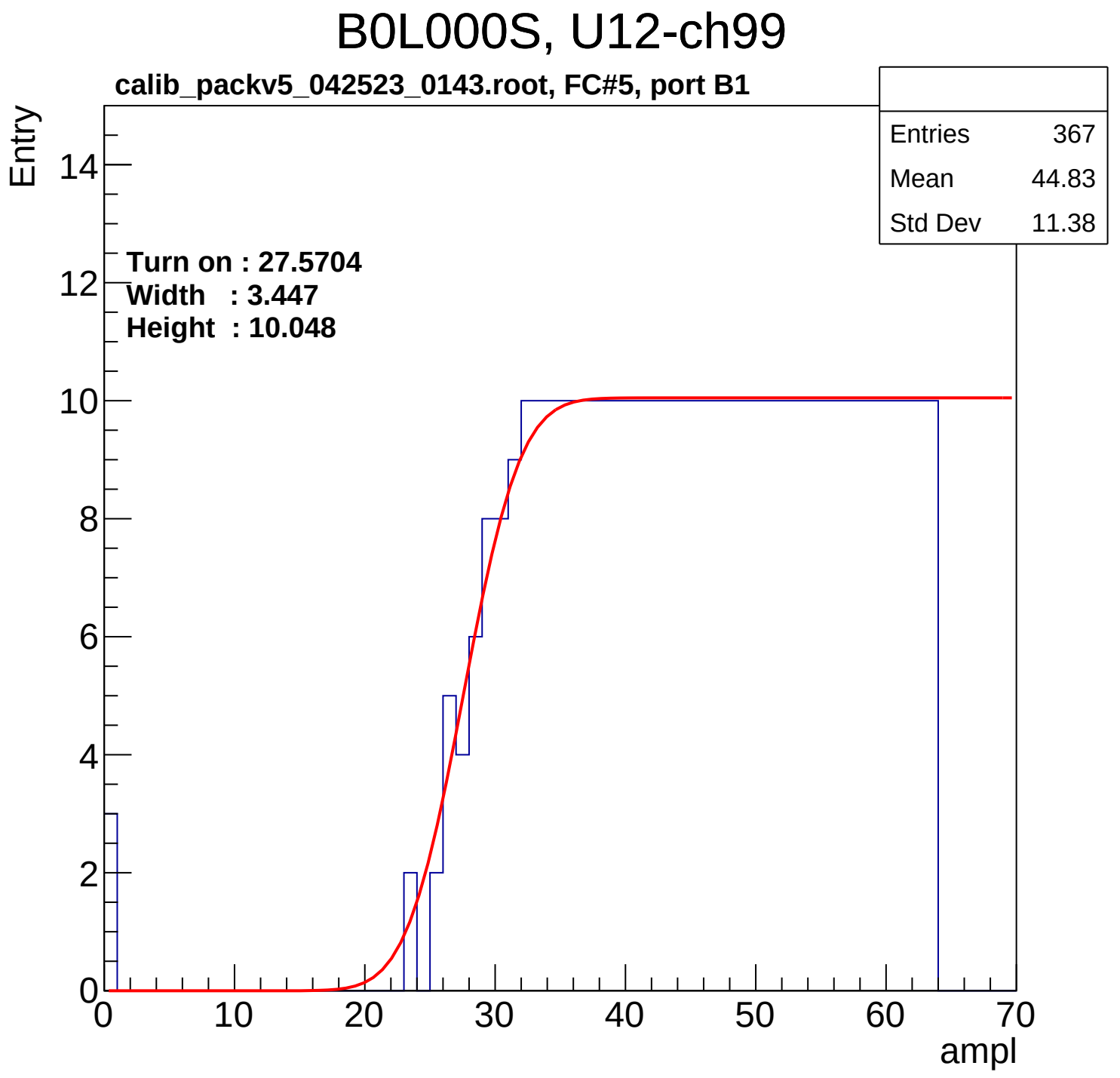
B0L000S, U12-ch99
calib_packv5_042523_0143.root, FC#5, port B1
Entries 367
Mean 44.83
Std Dev 11.38
Turn on : 27.5704
Width : 3.447
Height : 10.048
Entry
ampl
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6
8
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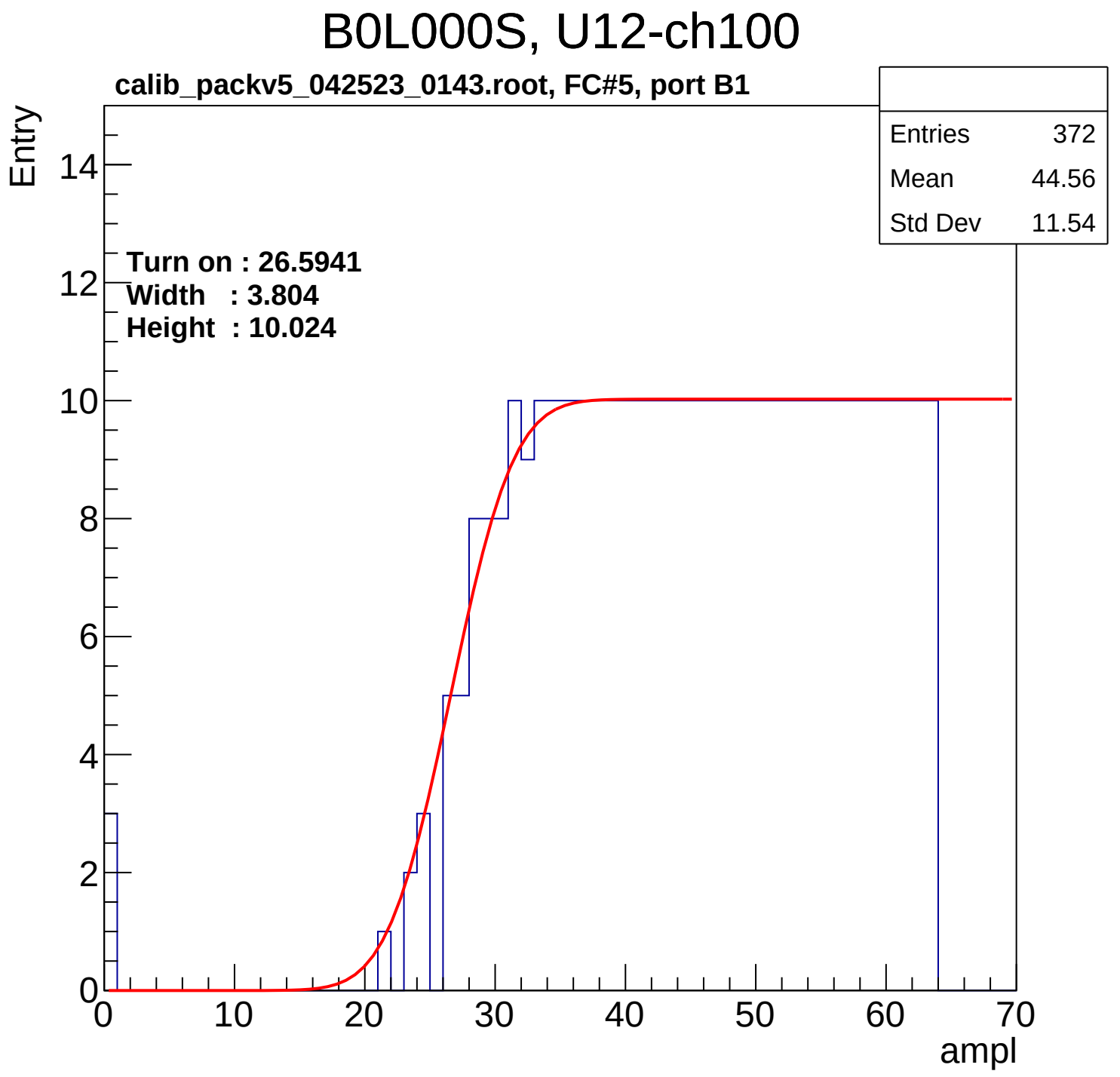
B0L000S, U12-ch100
calib_packv5_042523_0143.root, FC#5, port B1
Entries 372
Mean 44.56
Std Dev 11.54
Turn on : 26.5941
Width : 3.804
Height : 10.024
Entry
ampl
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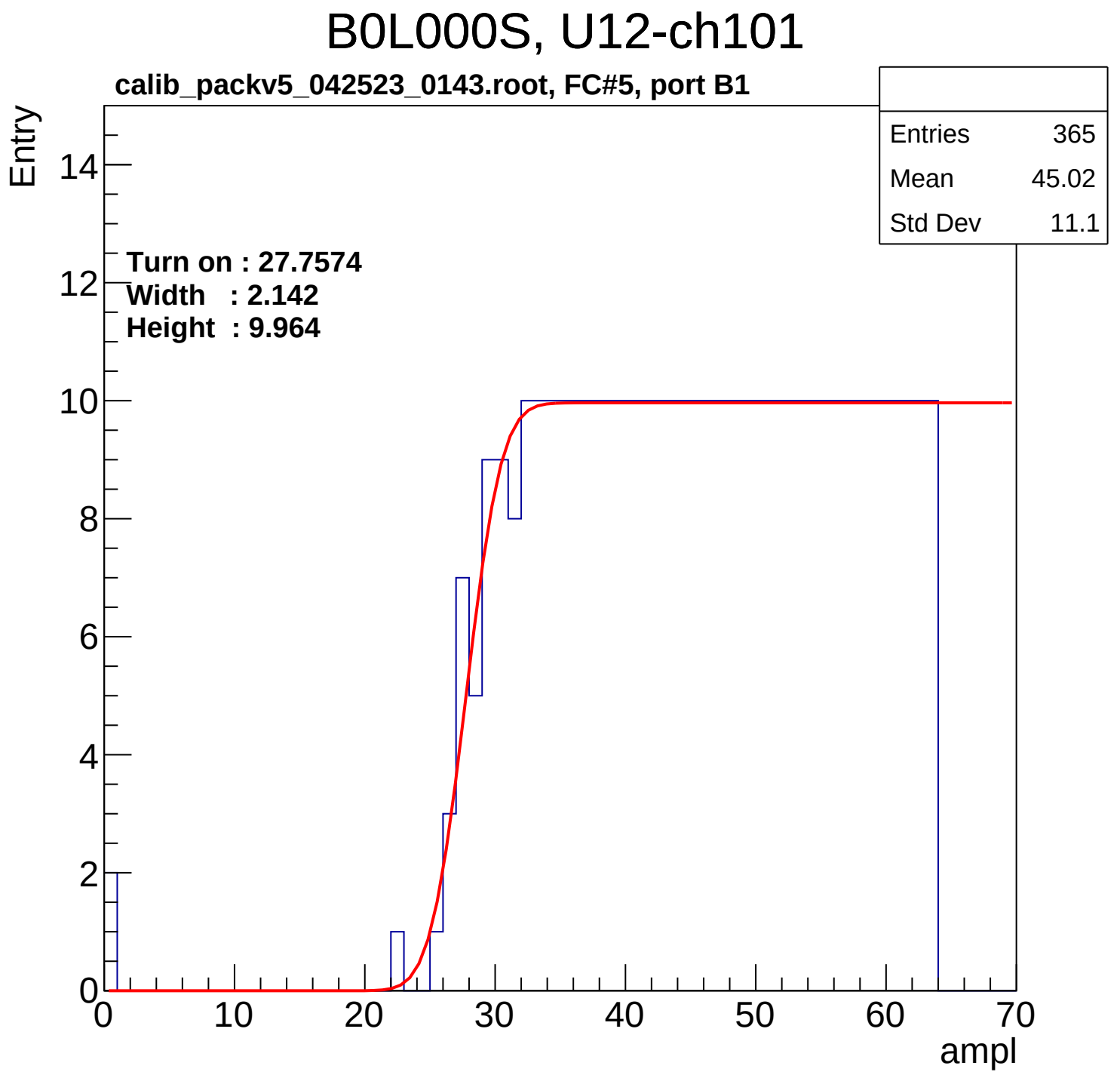
B0L000S, U12-ch101
calib_packv5_042523_0143.root, FC#5, port B1
Entries 365
Mean 45.02
Std Dev 11.1
Turn on : 27.7574
Width : 2.142
Height : 9.964
Entry
ampl
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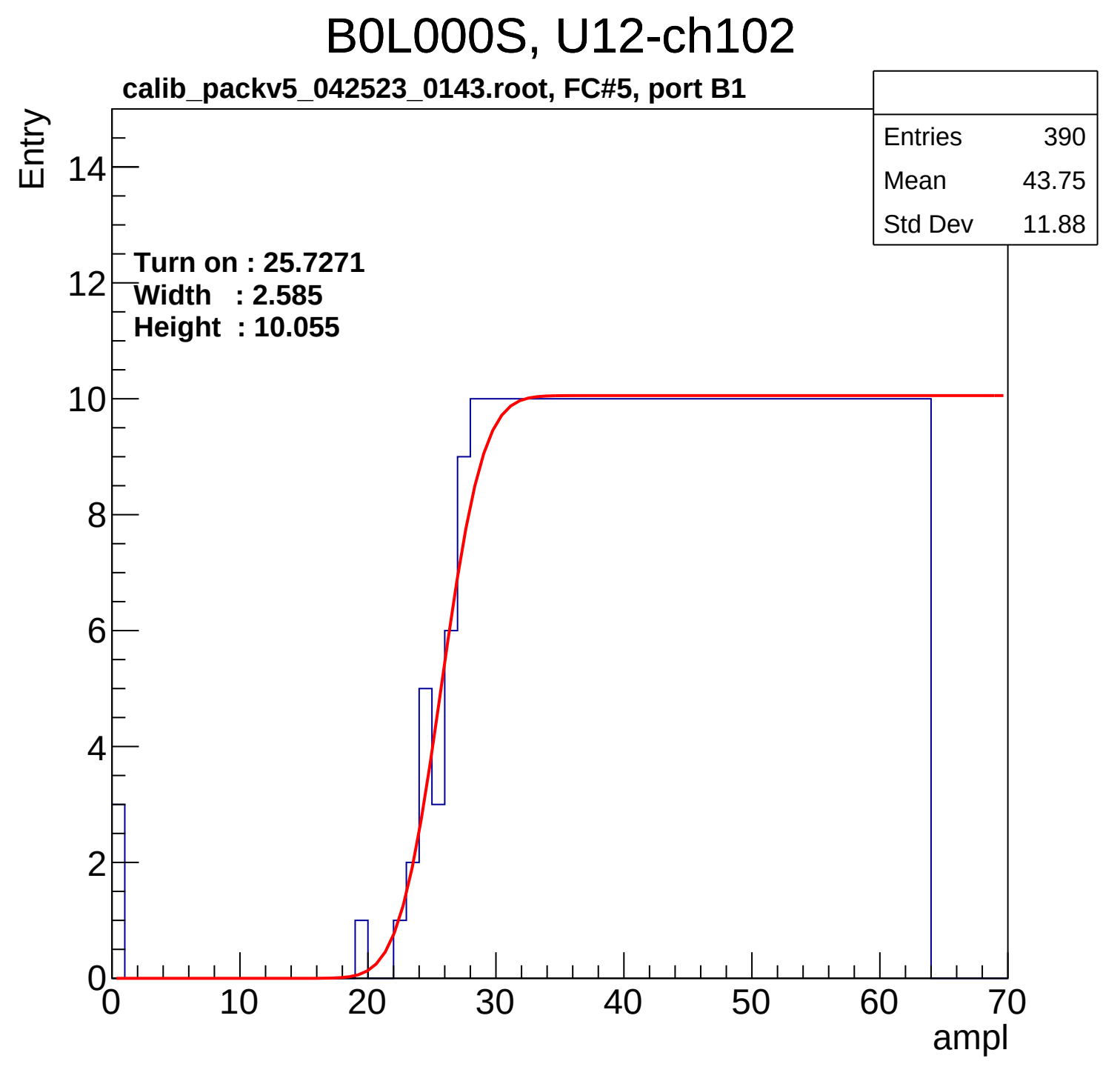
B0L000S, U12-ch102
calib_packv5_042523_0143.root, FC#5, port B1
Entries 390
Mean 43.75
Std Dev 11.88
Turn on : 25.7271
Width : 2.585
Height : 10.055
Entry
ampl
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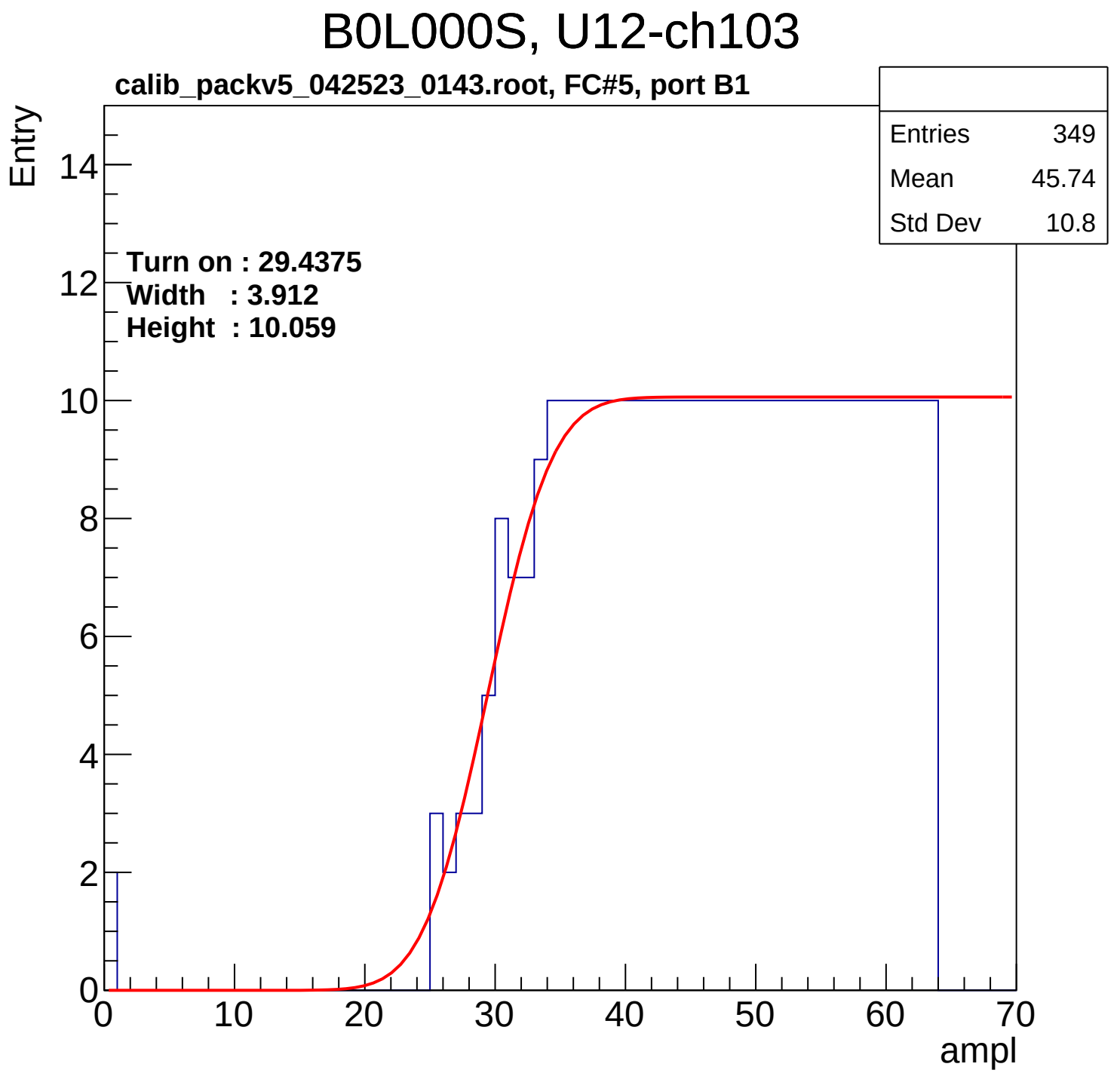
B0L000S, U12-ch103
calib_packv5_042523_0143.root, FC#5, port B1
Entries 349
Mean 45.74
Std Dev 10.8
Turn on : 29.4375
Width : 3.912
Height : 10.059
Entry
ampl
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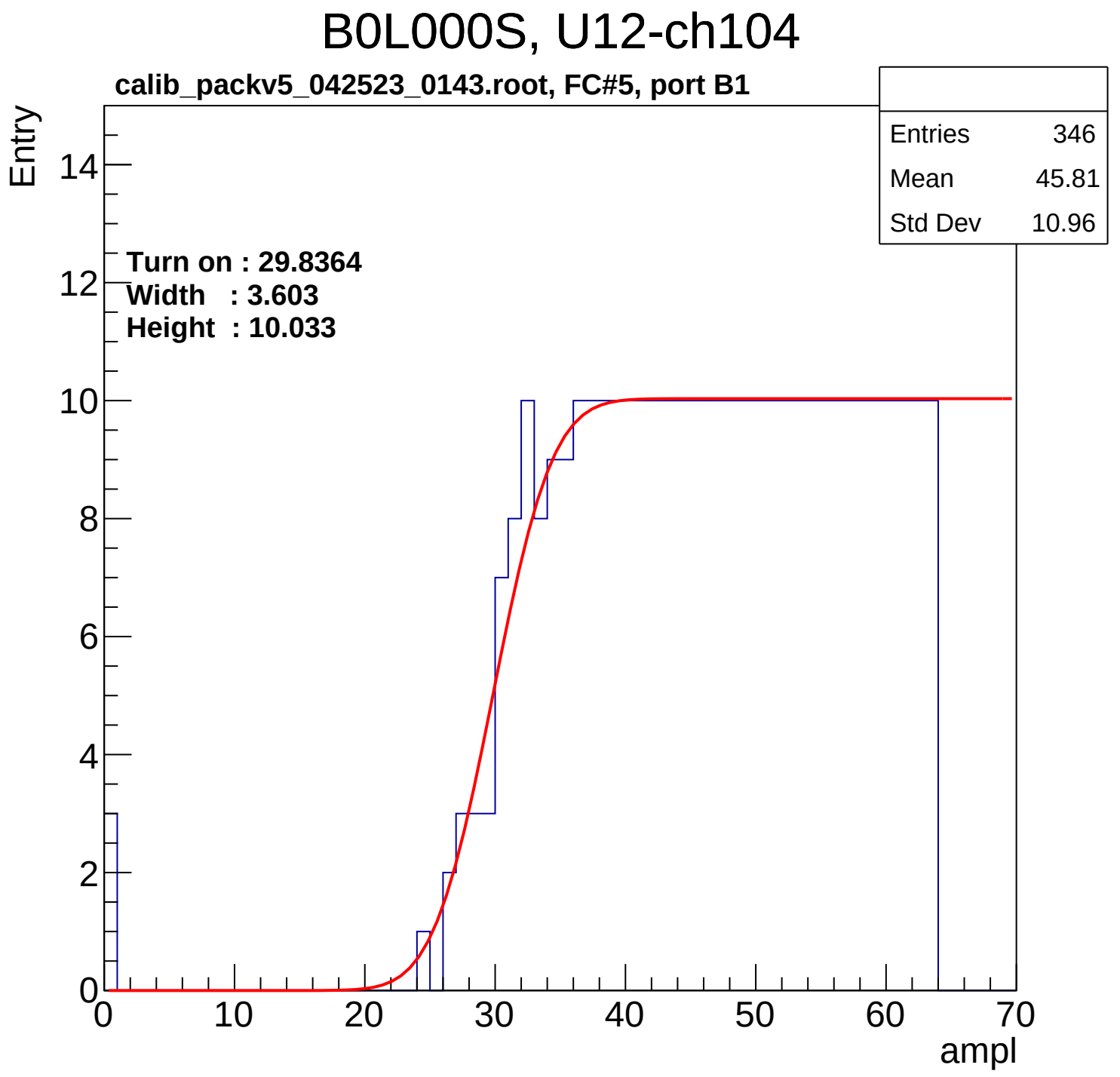
B0L000S, U12-ch104
calib_packv5_042523_0143.root, FC#5, port B1
Entries 346
Mean 45.81
Std Dev 10.96
Turn on : 29.8364
Width : 3.603
Height : 10.033
Entry
ampl
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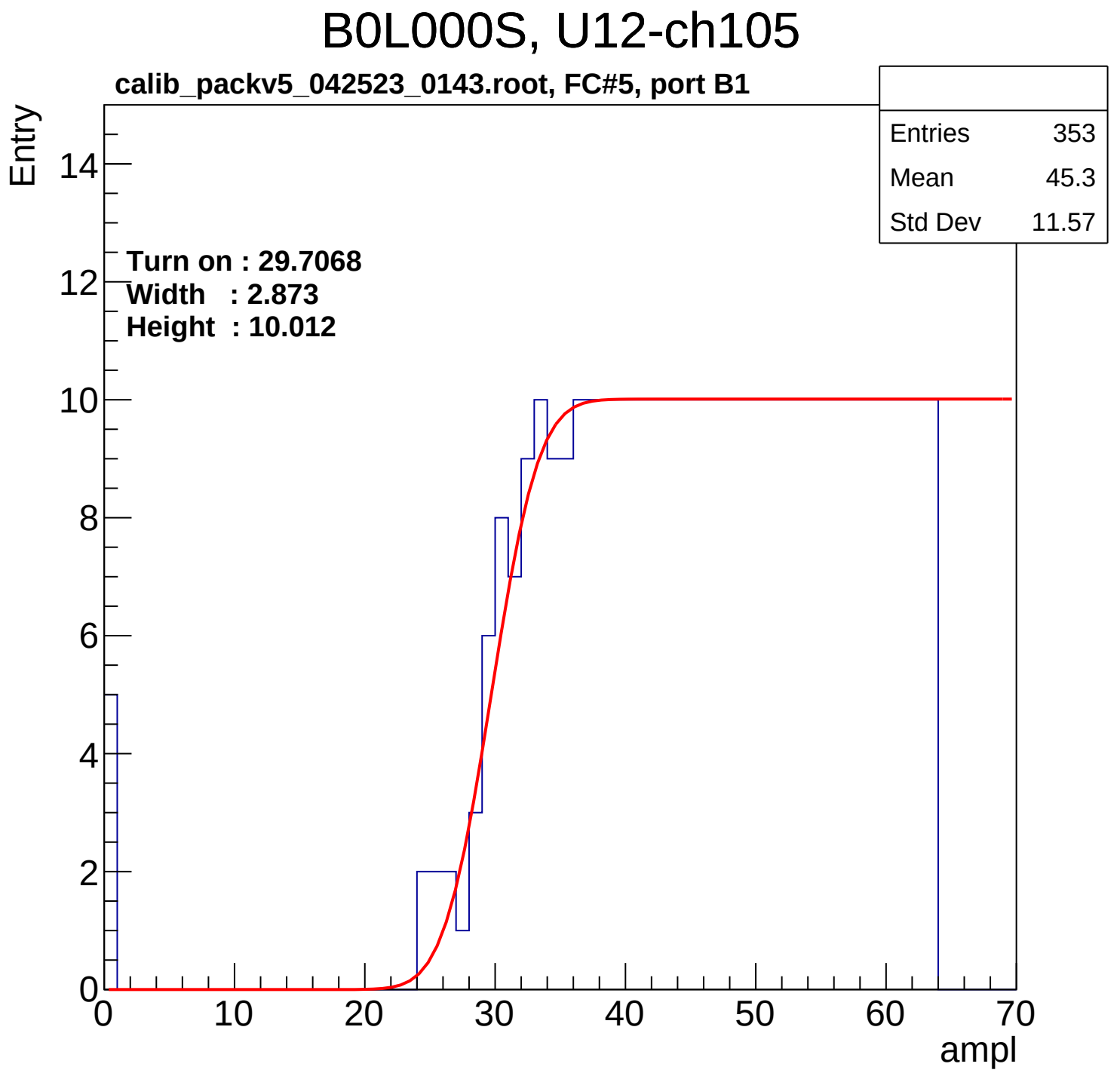
B0L000S, U12-ch105
calib_packv5_042523_0143.root, FC#5, port B1
Entries 353
Mean 45.3
Std Dev 11.57
Turn on : 29.7068
Width : 2.873
Height : 10.012
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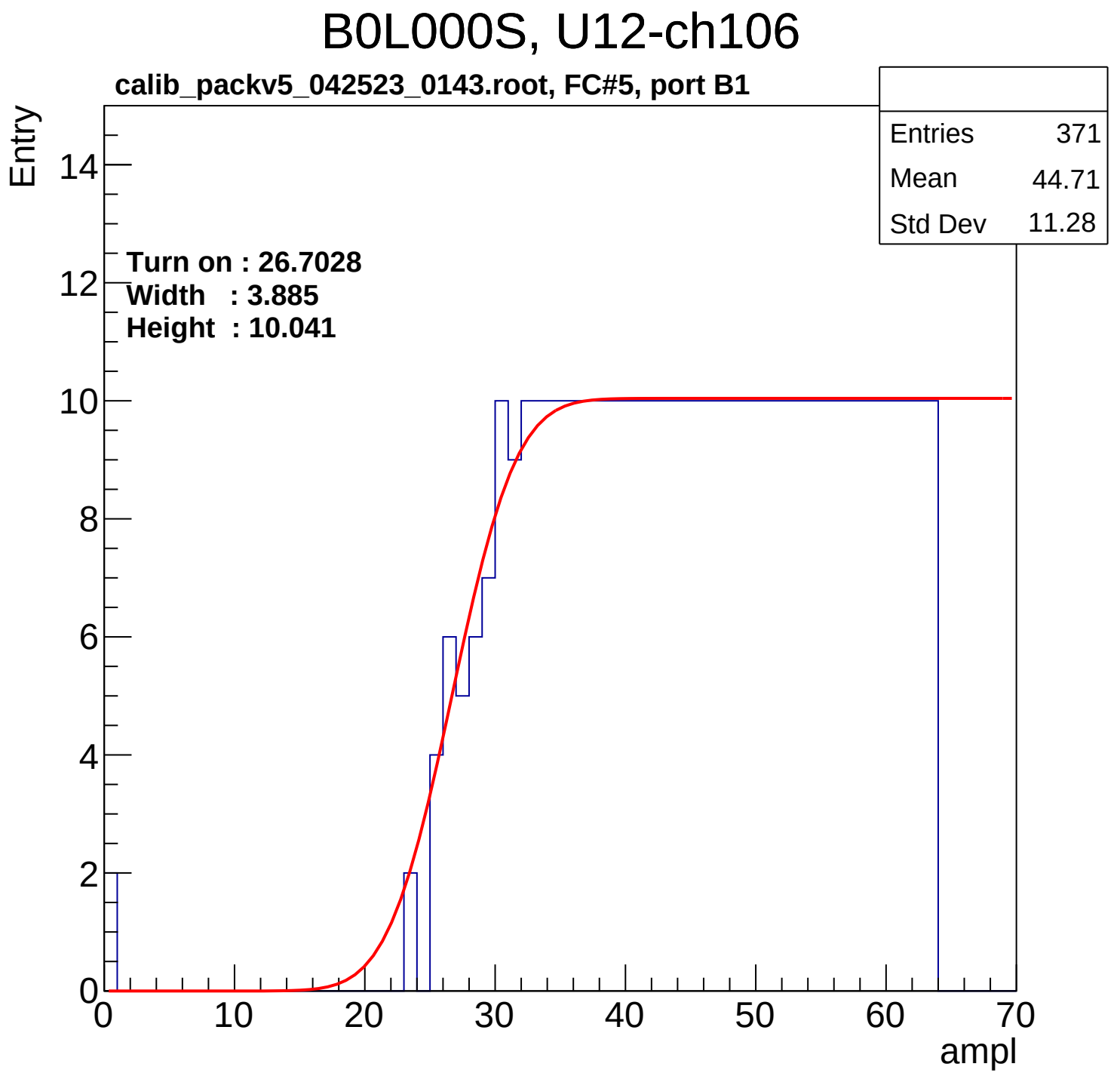
B0L000S, U12-ch106
calib_packv5_042523_0143.root, FC#5, port B1
Entries 371
Mean 44.71
Std Dev 11.28
Turn on : 26.7028
Width : 3.885
Height : 10.041
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ampl
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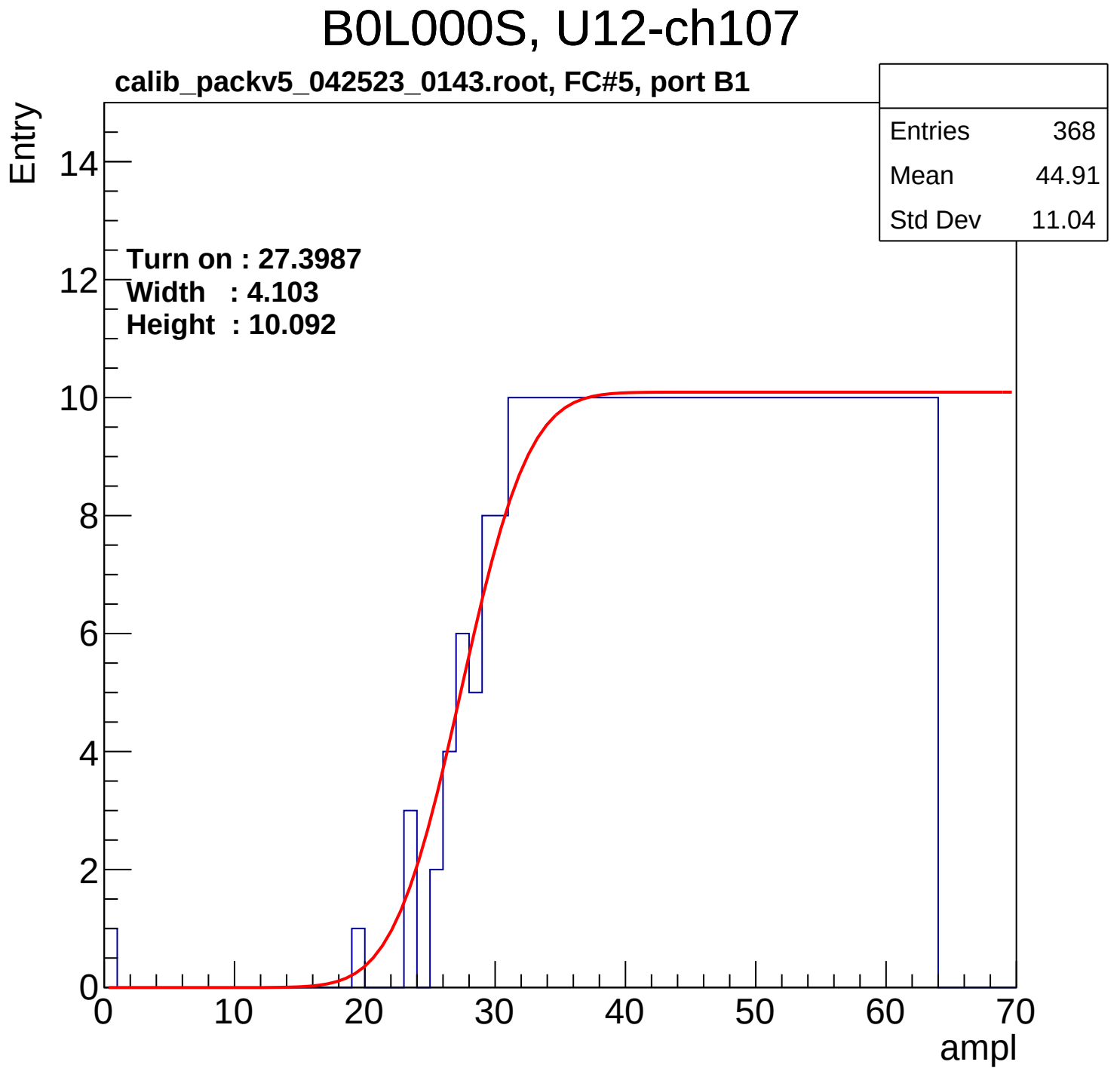
B0L000S, U12-ch107
calib_packv5_042523_0143.root, FC#5, port B1
Entries 368
Mean 44.91
Std Dev 11.04
Turn on : 27.3987
Width : 4.103
Height : 10.092
Entry
ampl
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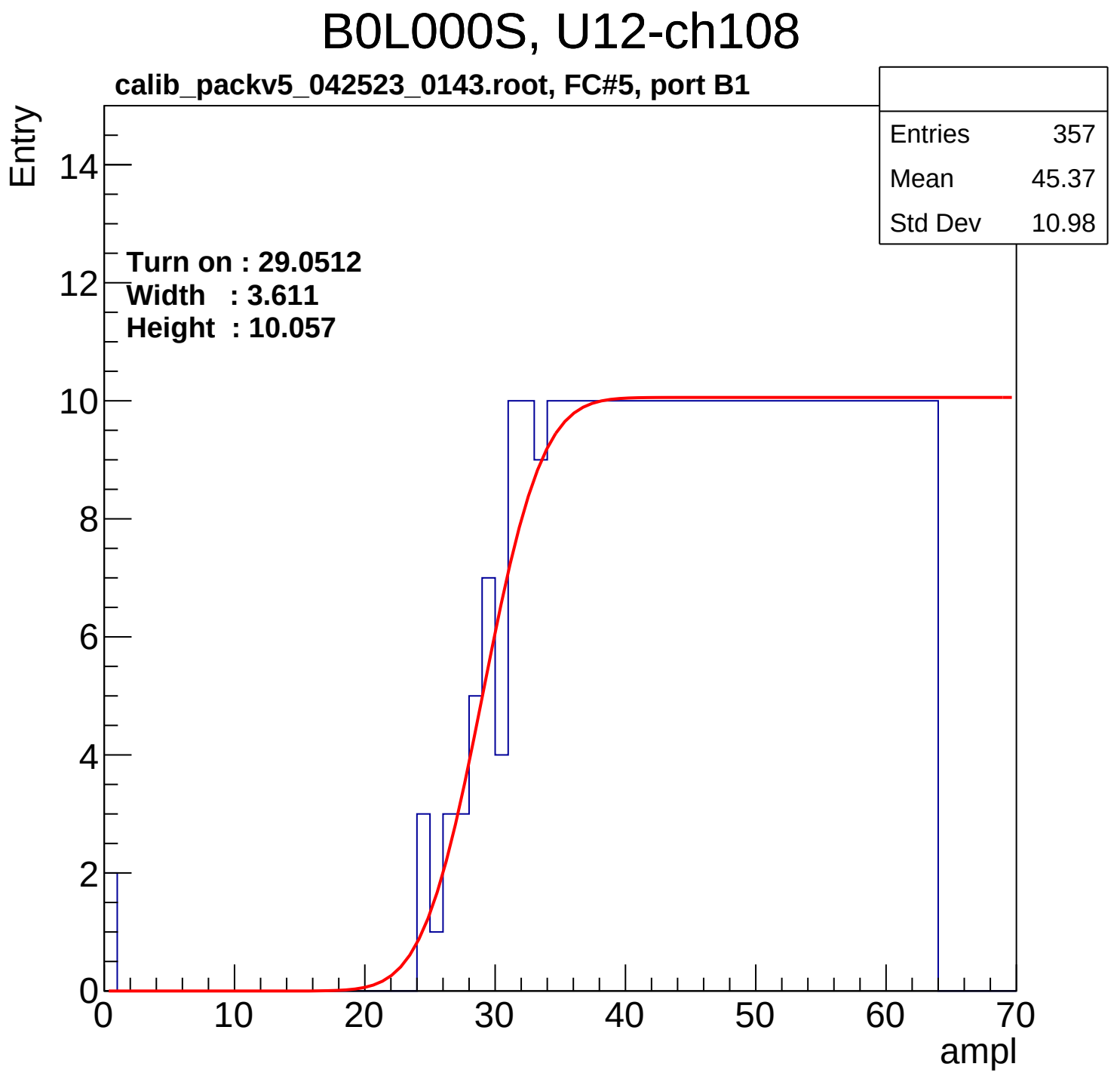
B0L000S, U12-ch108
calib_packv5_042523_0143.root, FC#5, port B1
Entries 357
Mean 45.37
Std Dev 10.98
Turn on : 29.0512
Width : 3.611
Height : 10.057
Entry
ampl
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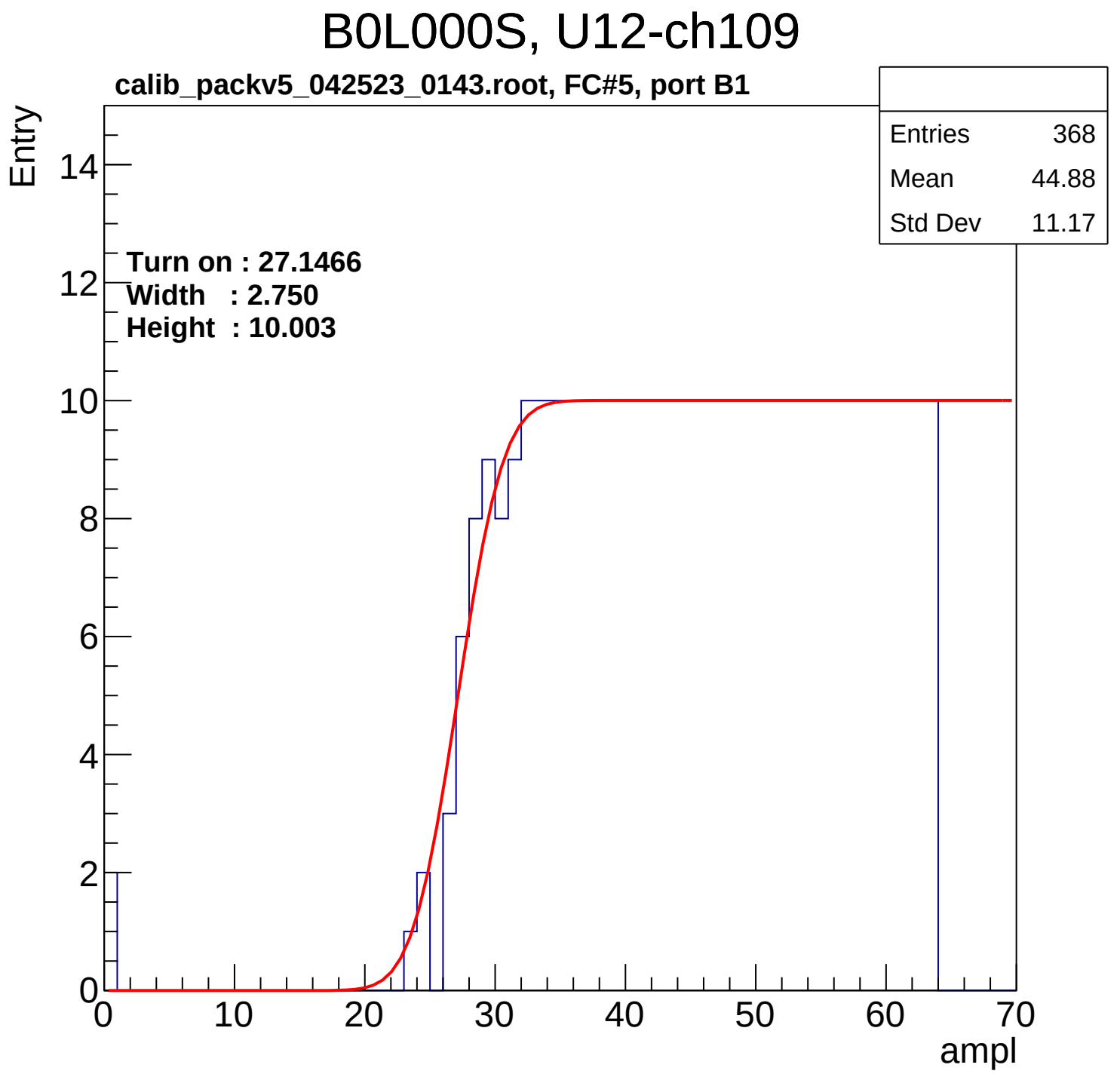
B0L000S, U12-ch109
calib_packv5_042523_0143.root, FC#5, port B1
Entries 368
Mean 44.88
Std Dev 11.17
Turn on : 27.1466
Width : 2.750
Height : 10.003
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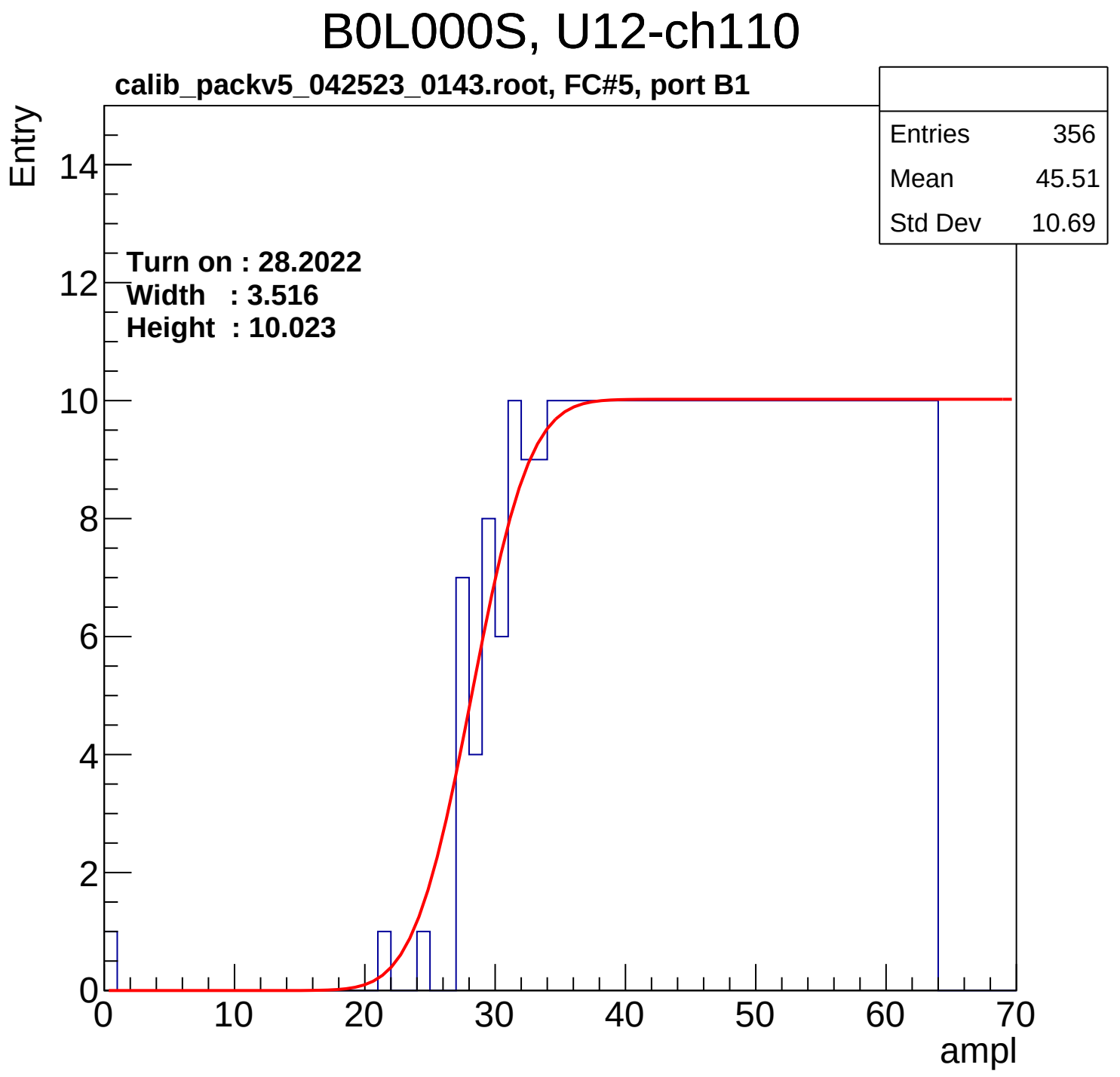
B0L000S, U12-ch110
calib_packv5_042523_0143.root, FC#5, port B1
Entries 356
Mean 45.51
Std Dev 10.69
Turn on : 28.2022
Width : 3.516
Height : 10.023
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ampl
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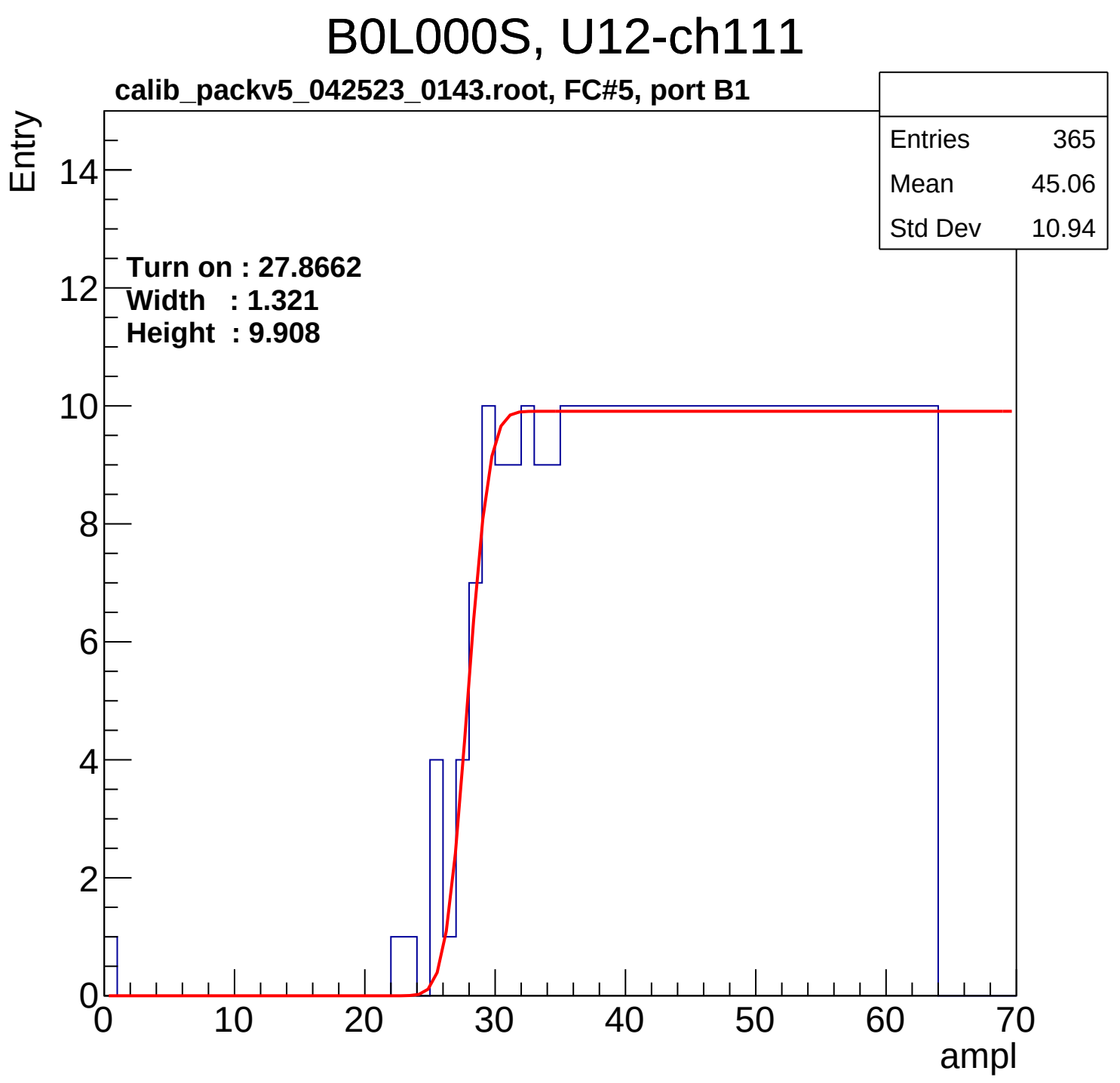
B0L000S, U12-ch111
calib_packv5_042523_0143.root, FC#5, port B1
Entries 365
Mean 45.06
Std Dev 10.94
Turn on : 27.8662
Width : 1.321
Height : 9.908
Entry
ampl
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6
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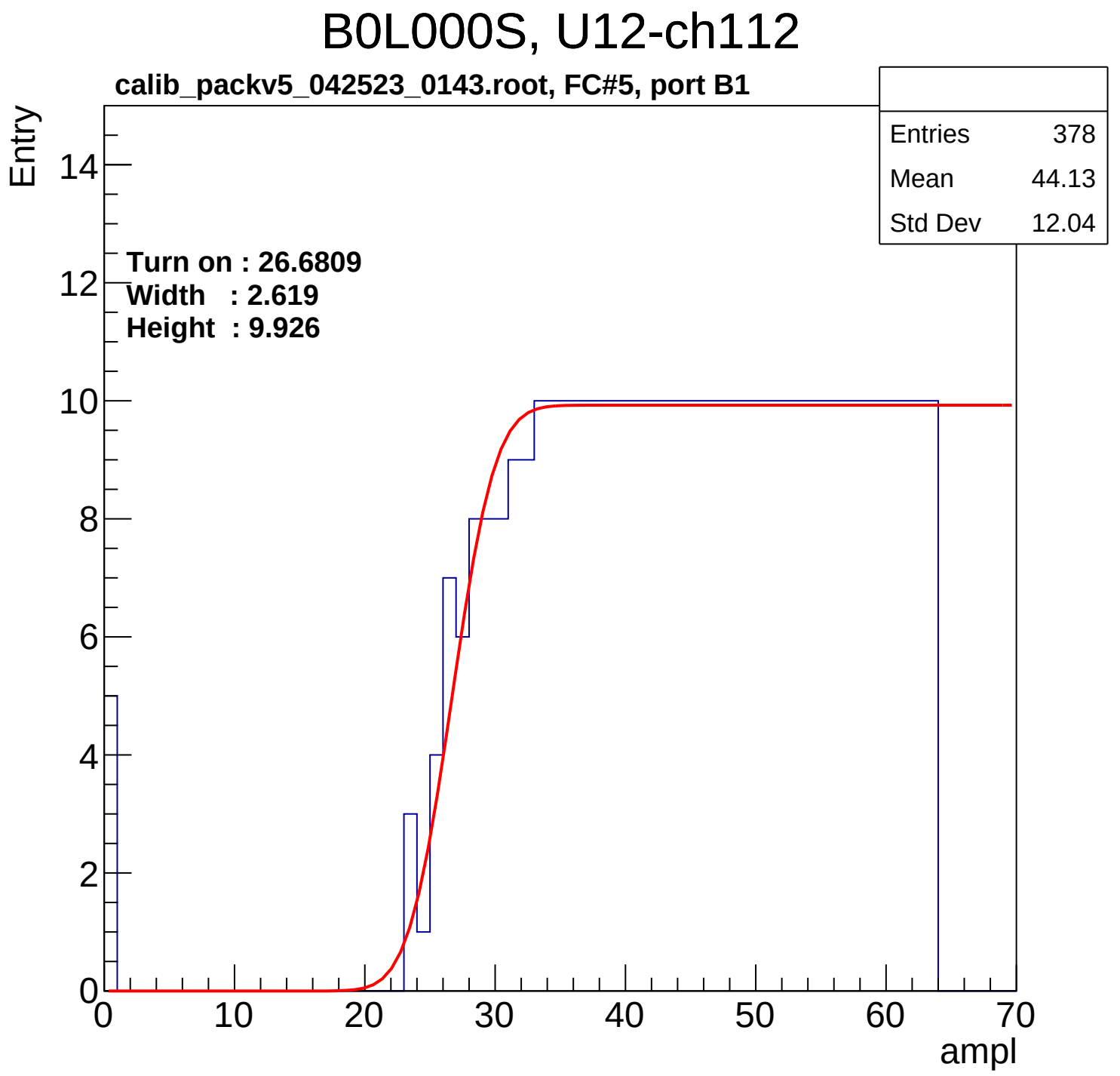
B0L000S, U12-ch112
calib_packv5_042523_0143.root, FC#5, port B1
Entries 378
Mean 44.13
Std Dev 12.04
Turn on : 26.6809
Width : 2.619
Height : 9.926
Entry
ampl
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2
4
6
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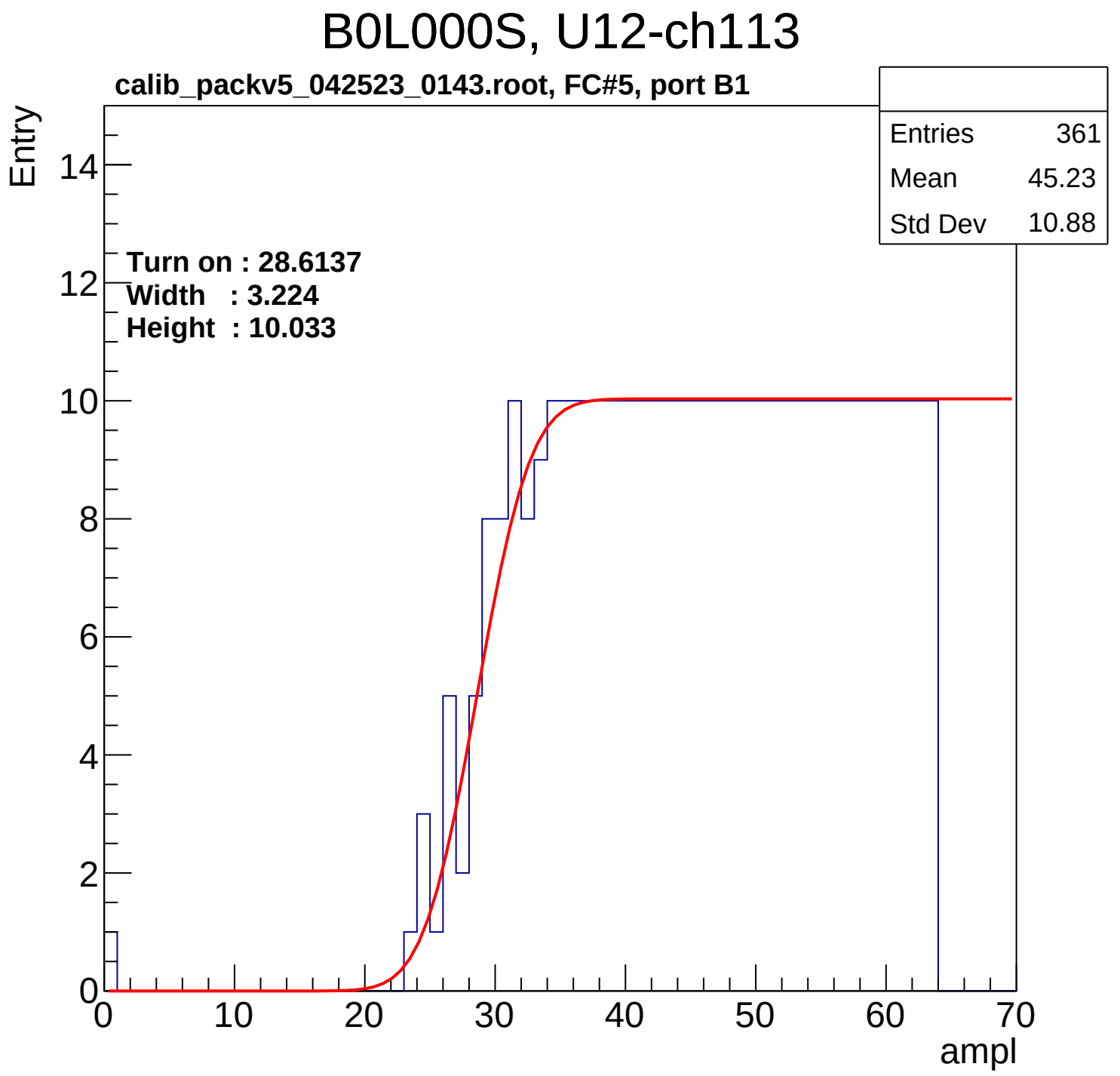
B0L000S, U12-ch113
calib_packv5_042523_0143.root, FC#5, port B1
Entries 361
Mean 45.23
Std Dev 10.88
Turn on : 28.6137
Width : 3.224
Height : 10.033
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ampl
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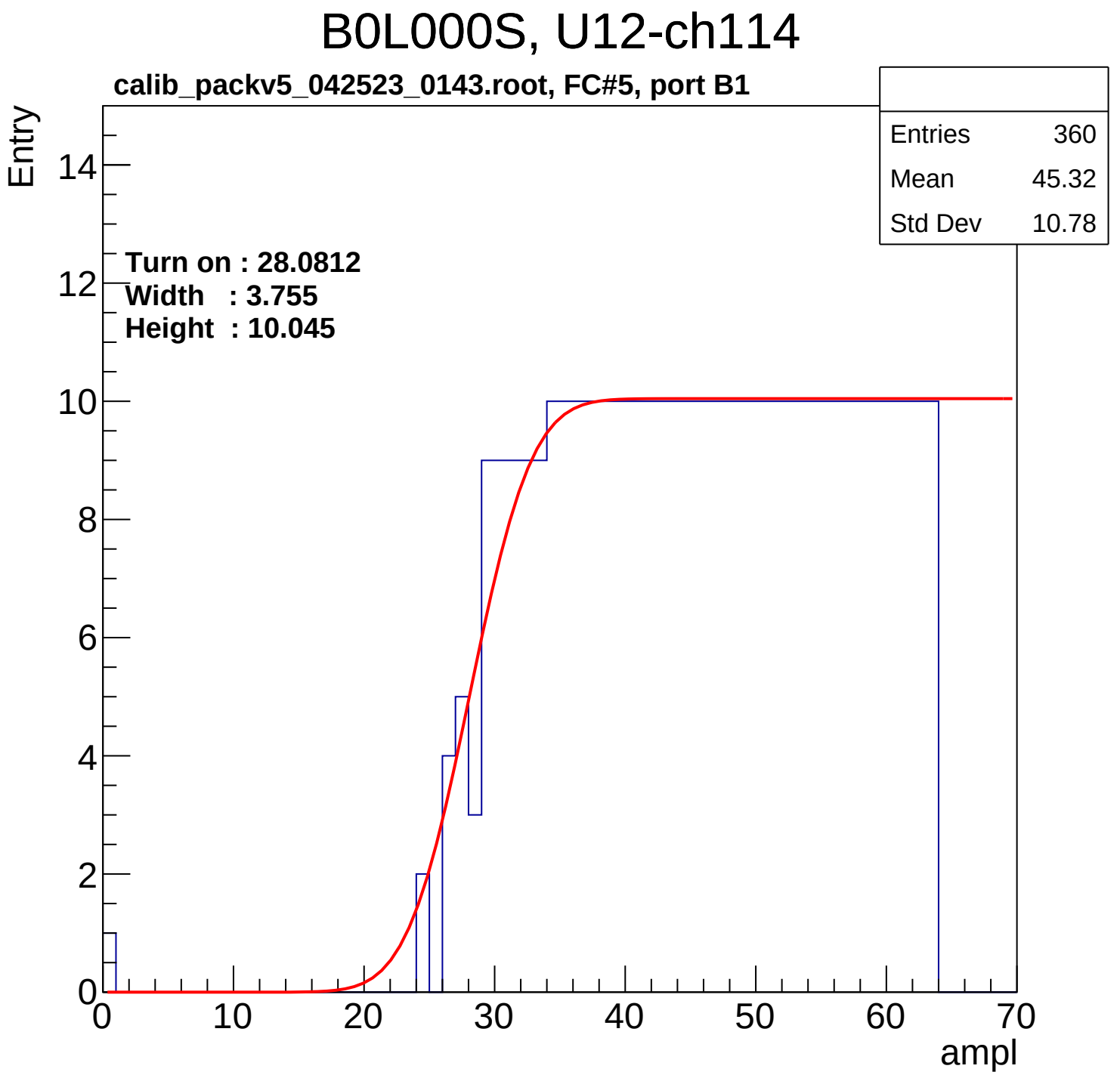
B0L000S, U12-ch114
calib_packv5_042523_0143.root, FC#5, port B1
Entries 360
Mean 45.32
Std Dev 10.78
Turn on : 28.0812
Width : 3.755
Height : 10.045
Entry
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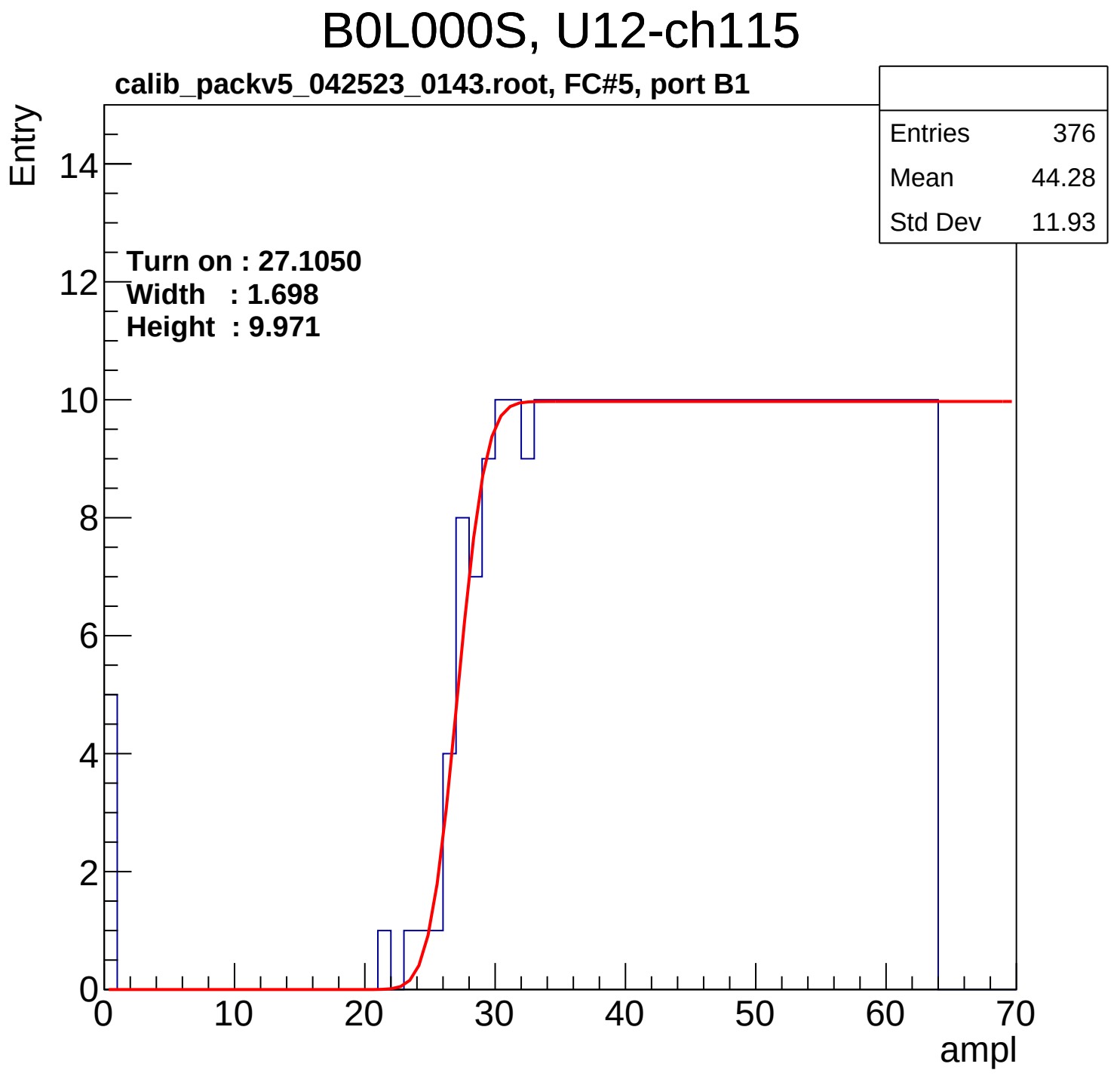
B0L000S, U12-ch115
calib_packv5_042523_0143.root, FC#5, port B1
Entries 376
Mean 44.28
Std Dev 11.93
Turn on : 27.1050
Width : 1.698
Height : 9.971
Entry
ampl
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4
6
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10
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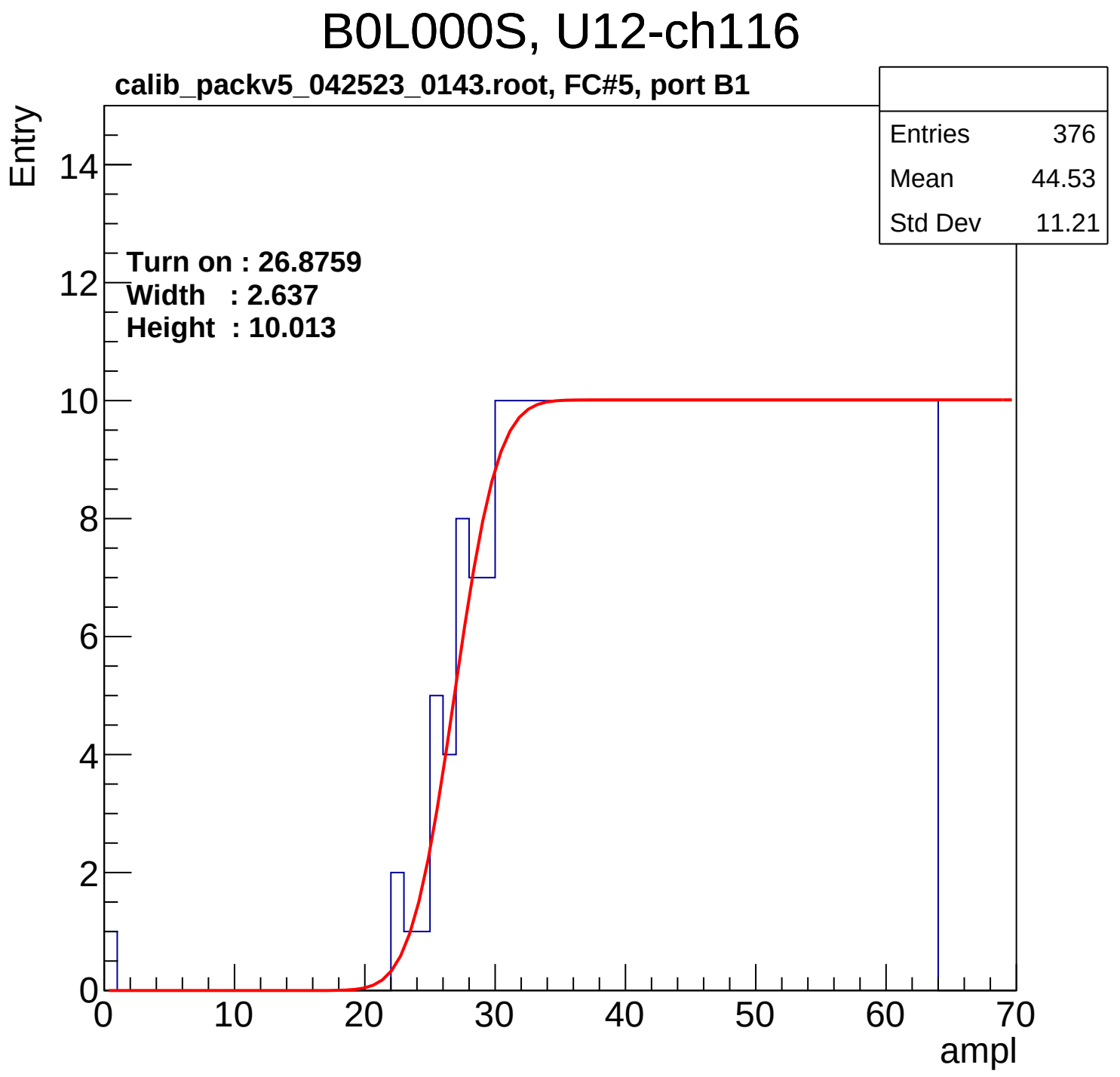
B0L000S, U12-ch116
calib_packv5_042523_0143.root, FC#5, port B1
Entries 376
Mean 44.53
Std Dev 11.21
Turn on : 26.8759
Width : 2.637
Height : 10.013
Entry
ampl
0
2
4
6
8
10
12
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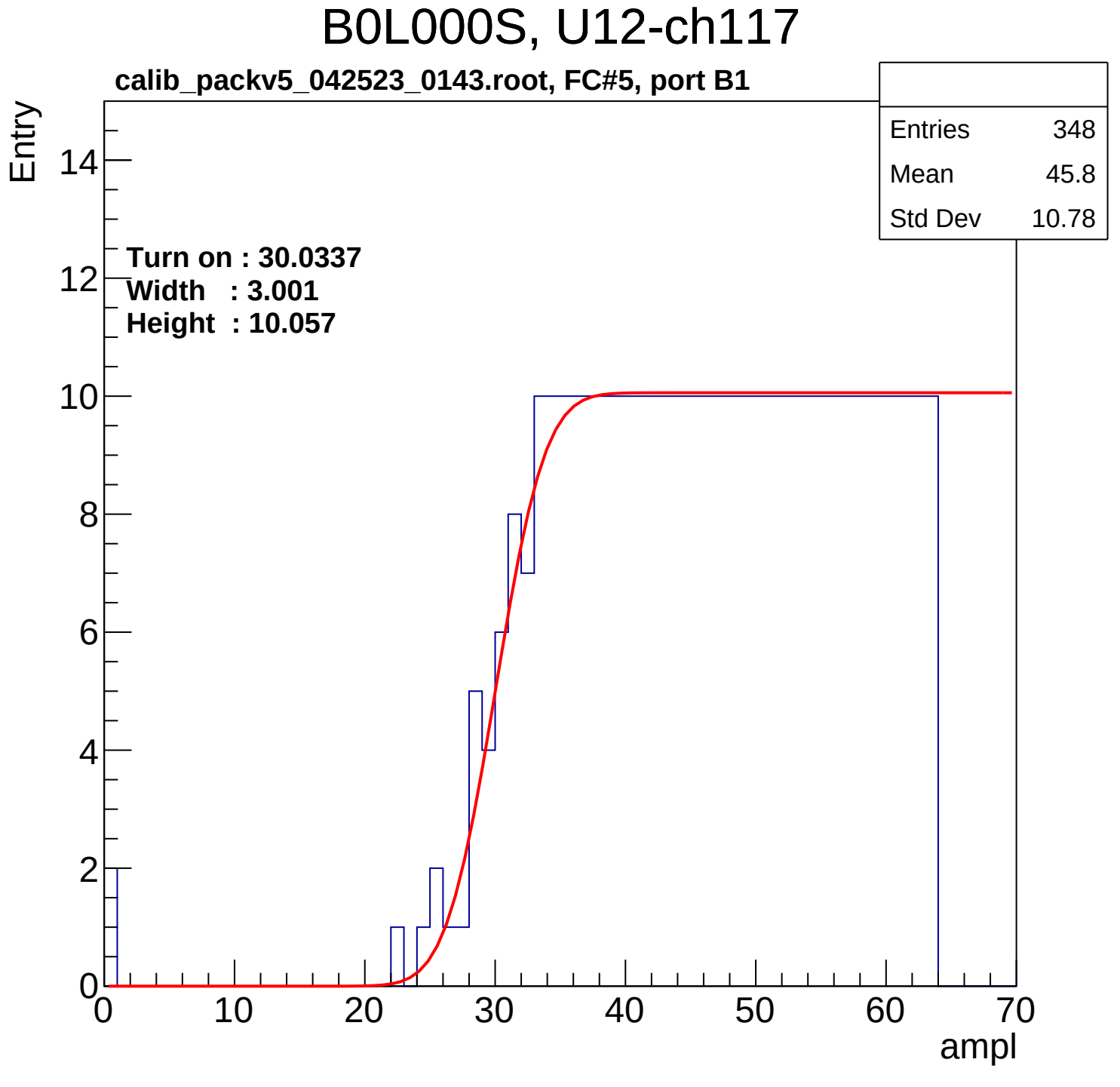
B0L000S, U12-ch117
calib_packv5_042523_0143.root, FC#5, port B1
Entries 348
Mean 45.8
Std Dev 10.78
Turn on : 30.0337
Width : 3.001
Height : 10.057
Entry
ampl
0
2
4
6
8
10
12
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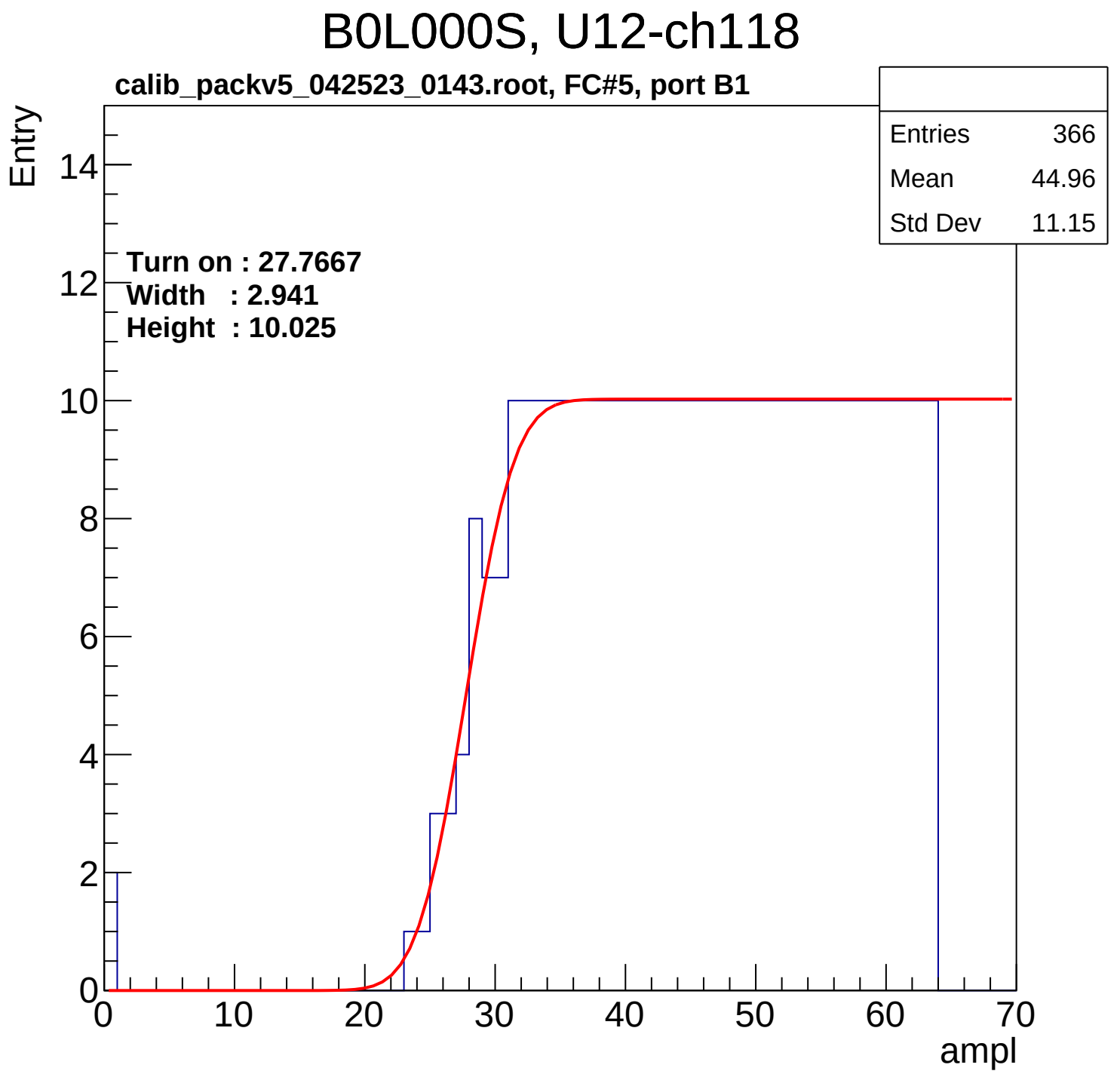
B0L000S, U12-ch118
calib_packv5_042523_0143.root, FC#5, port B1
Entries 366
Mean 44.96
Std Dev 11.15
Turn on : 27.7667
Width : 2.941
Height : 10.025
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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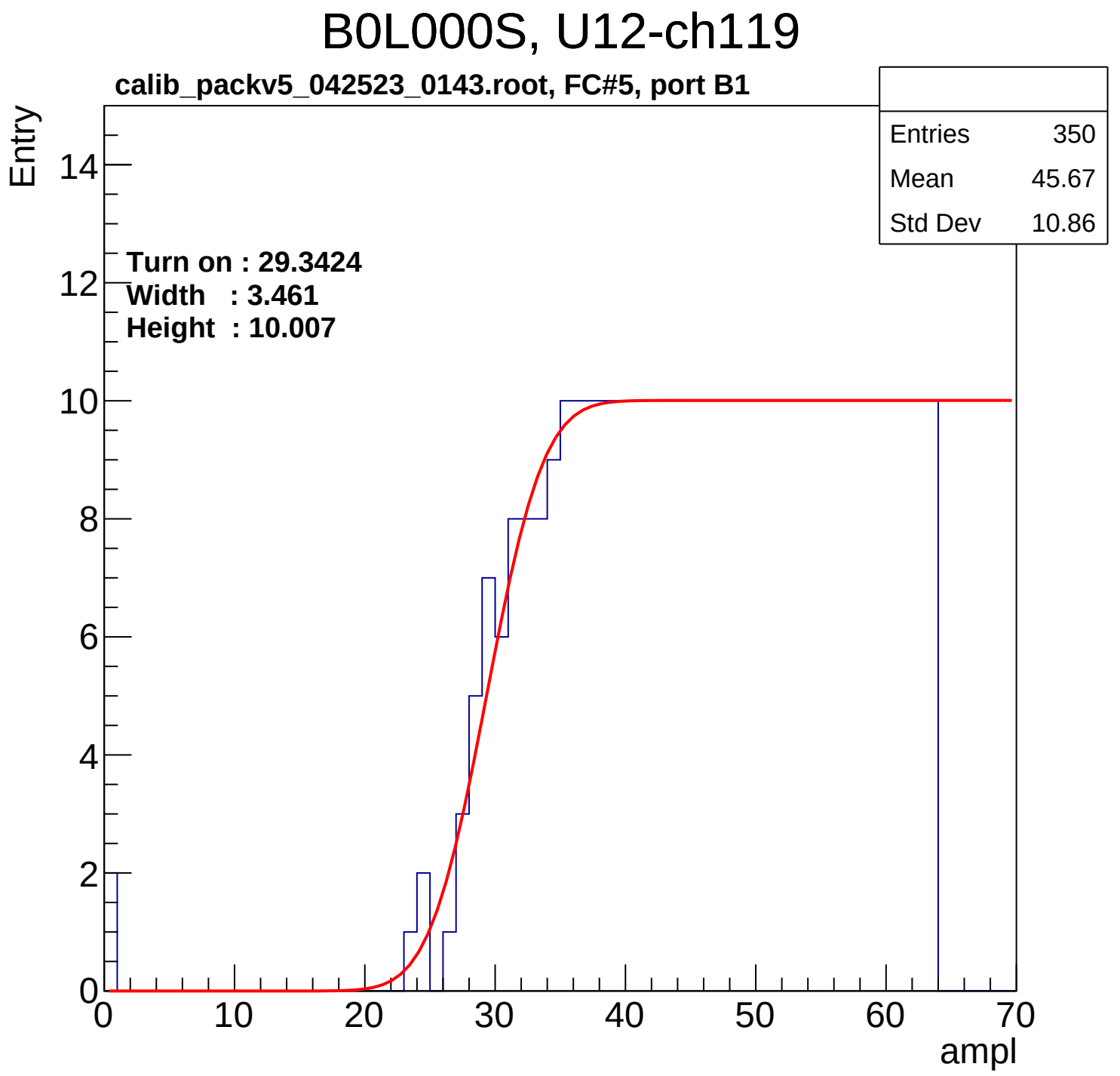
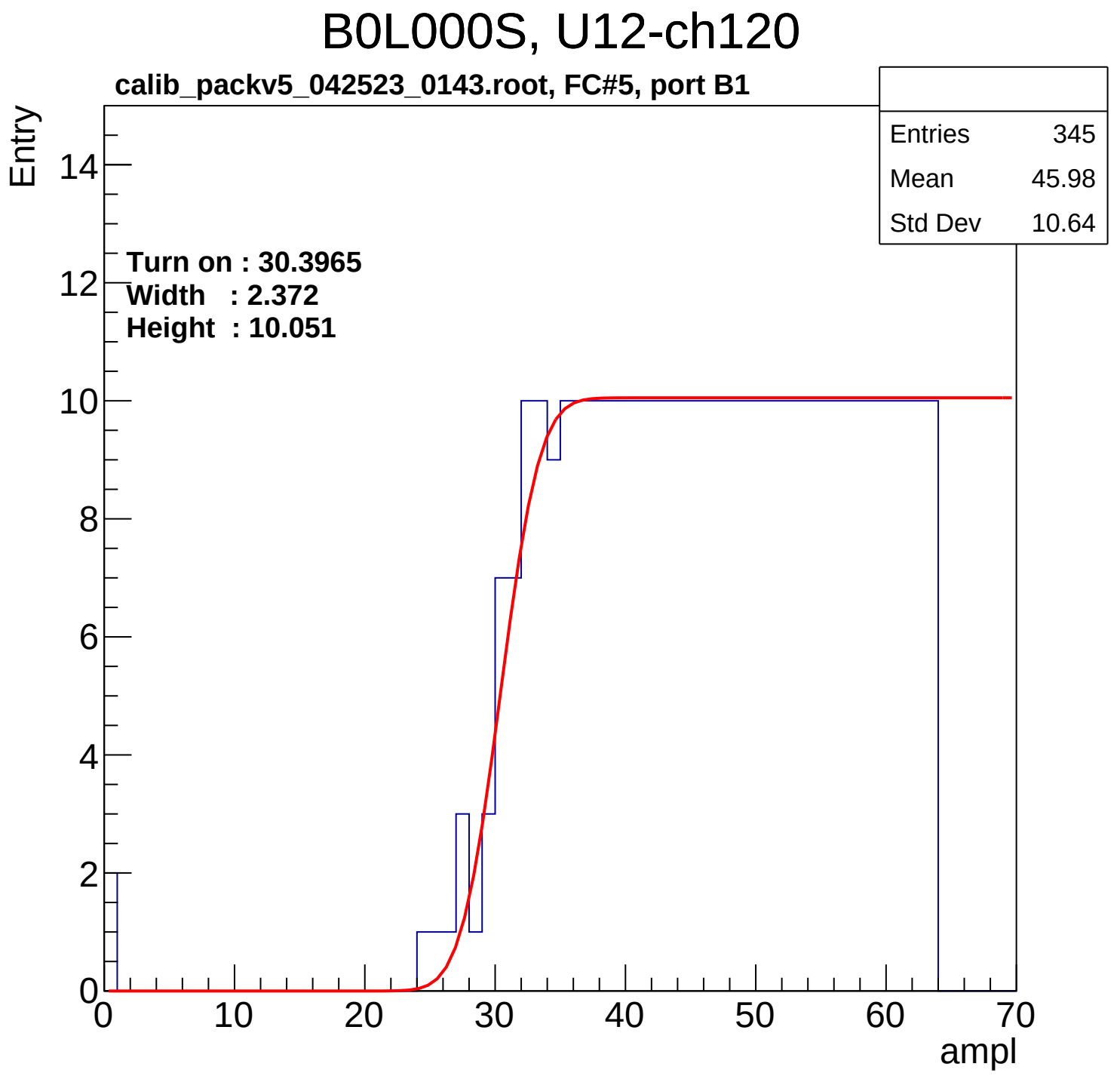

B0L000S, U12-ch119
calib_packv5_042523_0143.root, FC#5, port B1
Entries 350
Mean 45.67
Std Dev 10.86
Turn on : 29.3424
Width : 3.461
Height : 10.007
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L000S, U12-ch120
calib_packv5_042523_0143.root, FC#5, port B1
Entries 345
Mean 45.98
Std Dev 10.64
Turn on : 30.3965
Width : 2.372
Height : 10.051
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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40
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60
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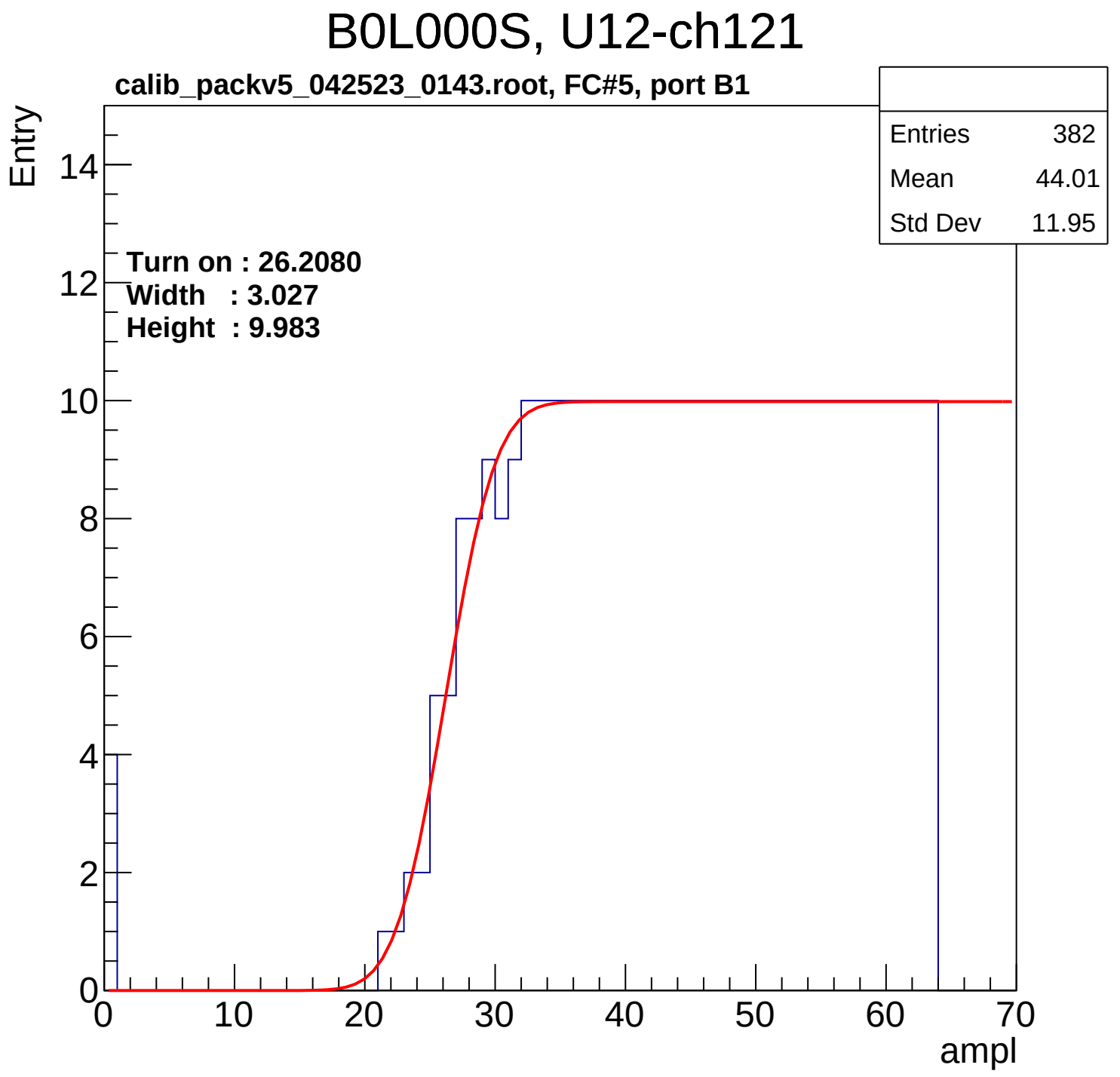
B0L000S, U12-ch121
calib_packv5_042523_0143.root, FC#5, port B1
Entries 382
Mean 44.01
Std Dev 11.95
Turn on : 26.2080
Width : 3.027
Height : 9.983
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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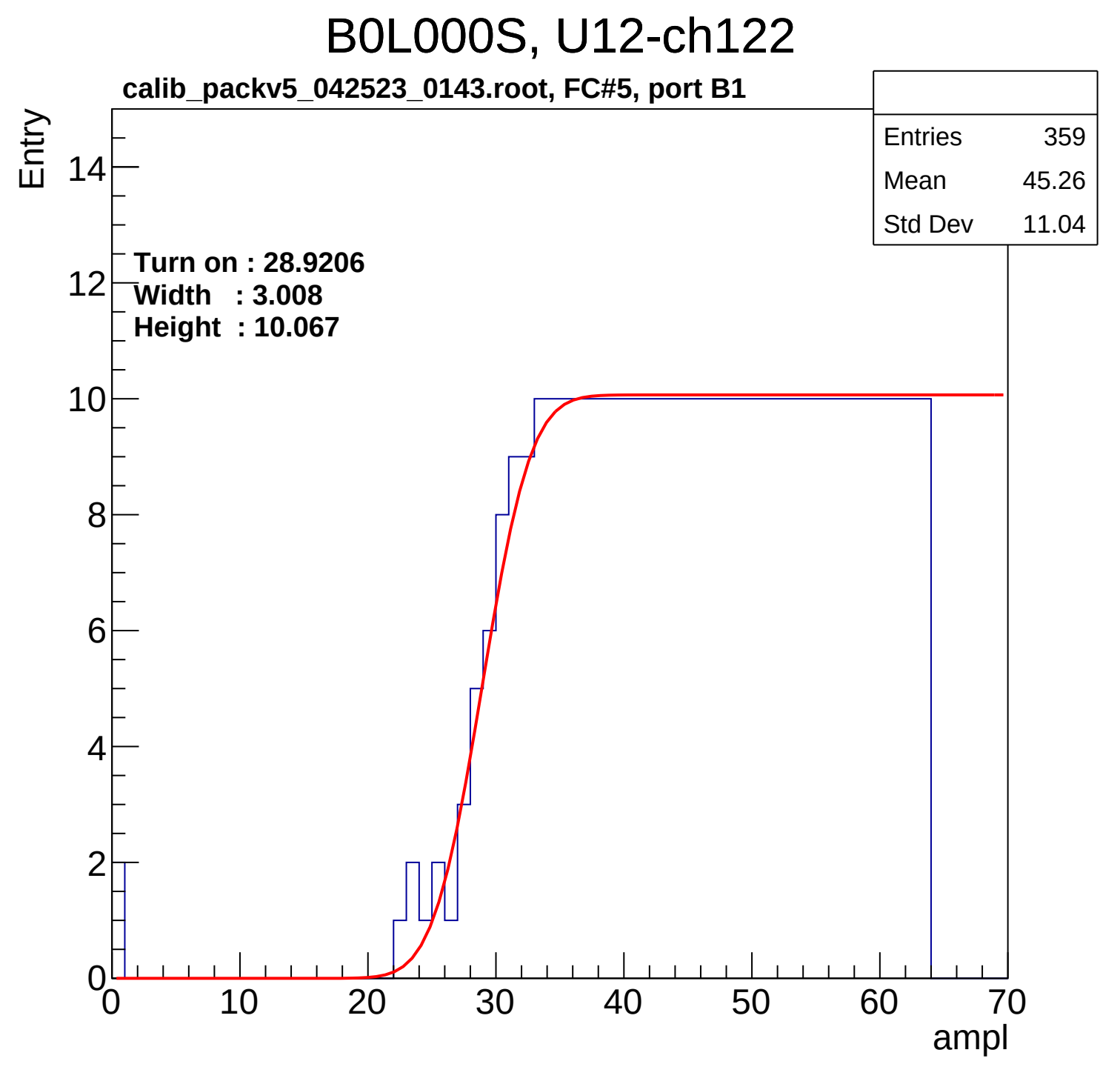
B0L000S, U12-ch122
calib_packv5_042523_0143.root, FC#5, port B1
Entries 359
Mean 45.26
Std Dev 11.04
Turn on : 28.9206
Width : 3.008
Height : 10.067
Entry
ampl
0
2
4
6
8
10
12
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20
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40
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60
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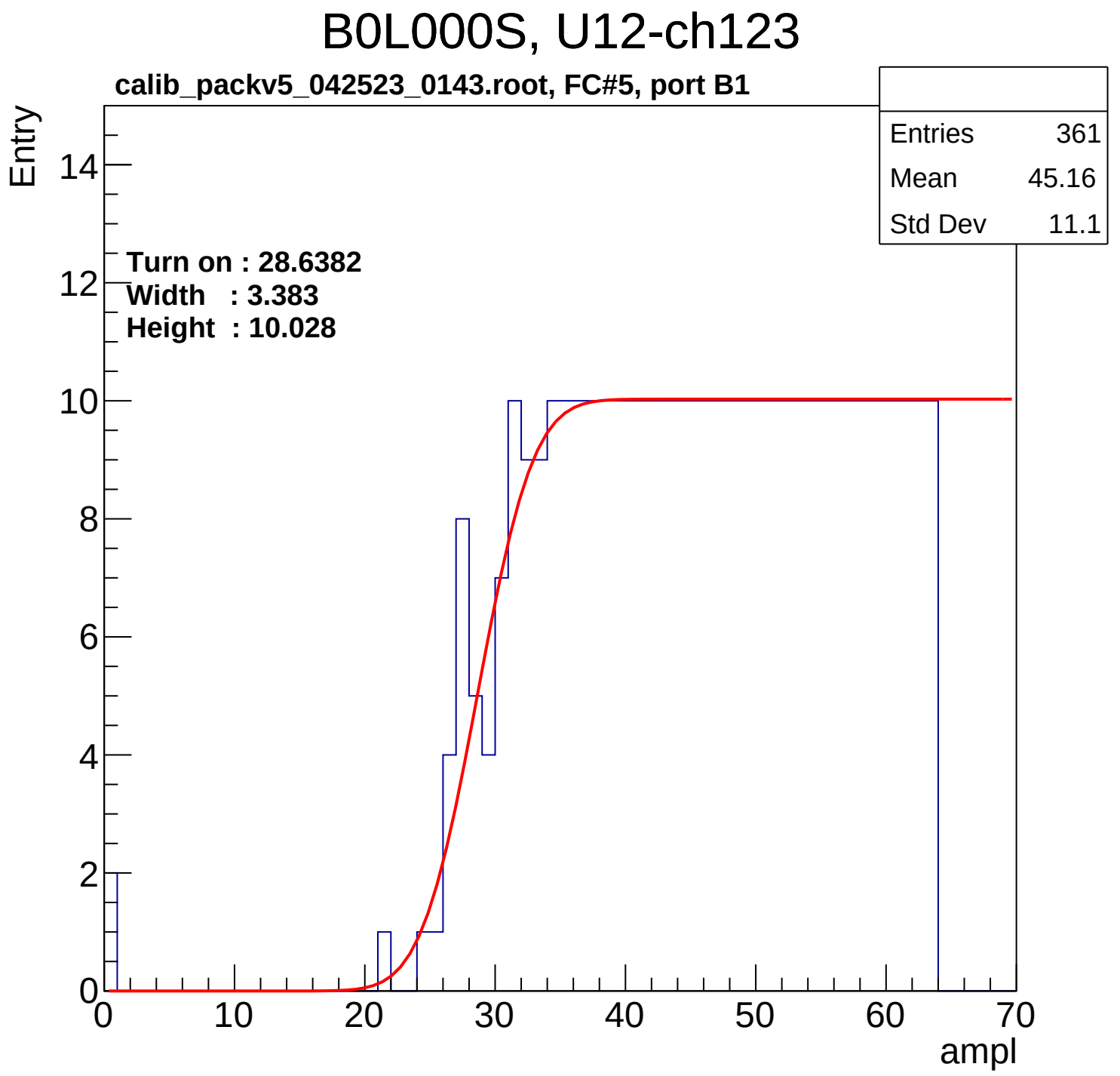
B0L000S, U12-ch123
calib_packv5_042523_0143.root, FC#5, port B1
Entries 361
Mean 45.16
Std Dev 11.1
Turn on : 28.6382
Width : 3.383
Height : 10.028
Entry
ampl
0
2
4
6
8
10
12
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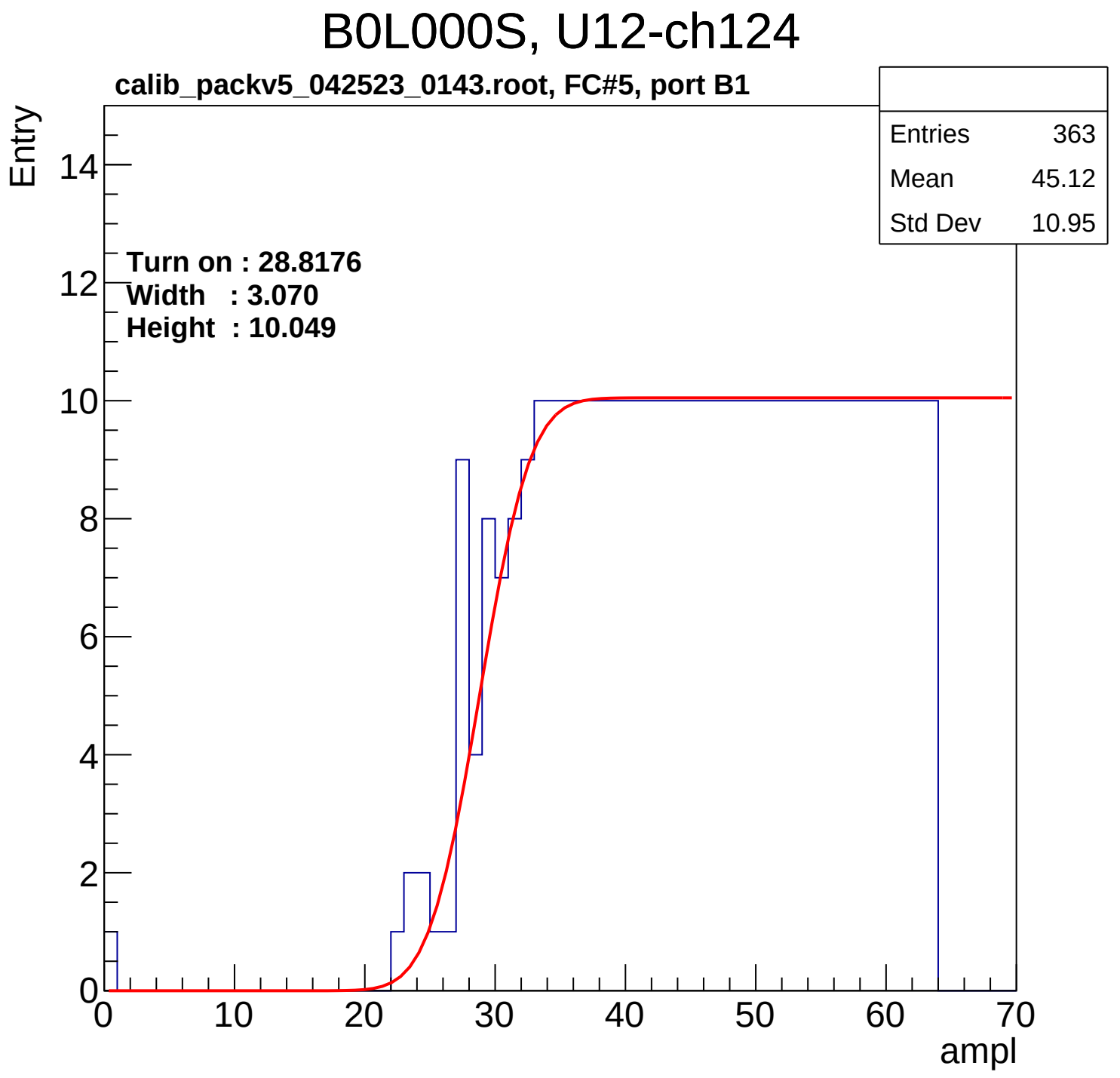
0
10
20
30
40
50
60
70


B0L000S, U12-ch124
calib_packv5_042523_0143.root, FC#5, port B1
Entries 363
Mean 45.12
Std Dev 10.95
Turn on : 28.8176
Width : 3.070
Height : 10.049
Entry
ampl
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4
6
8
10
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14
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20
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60
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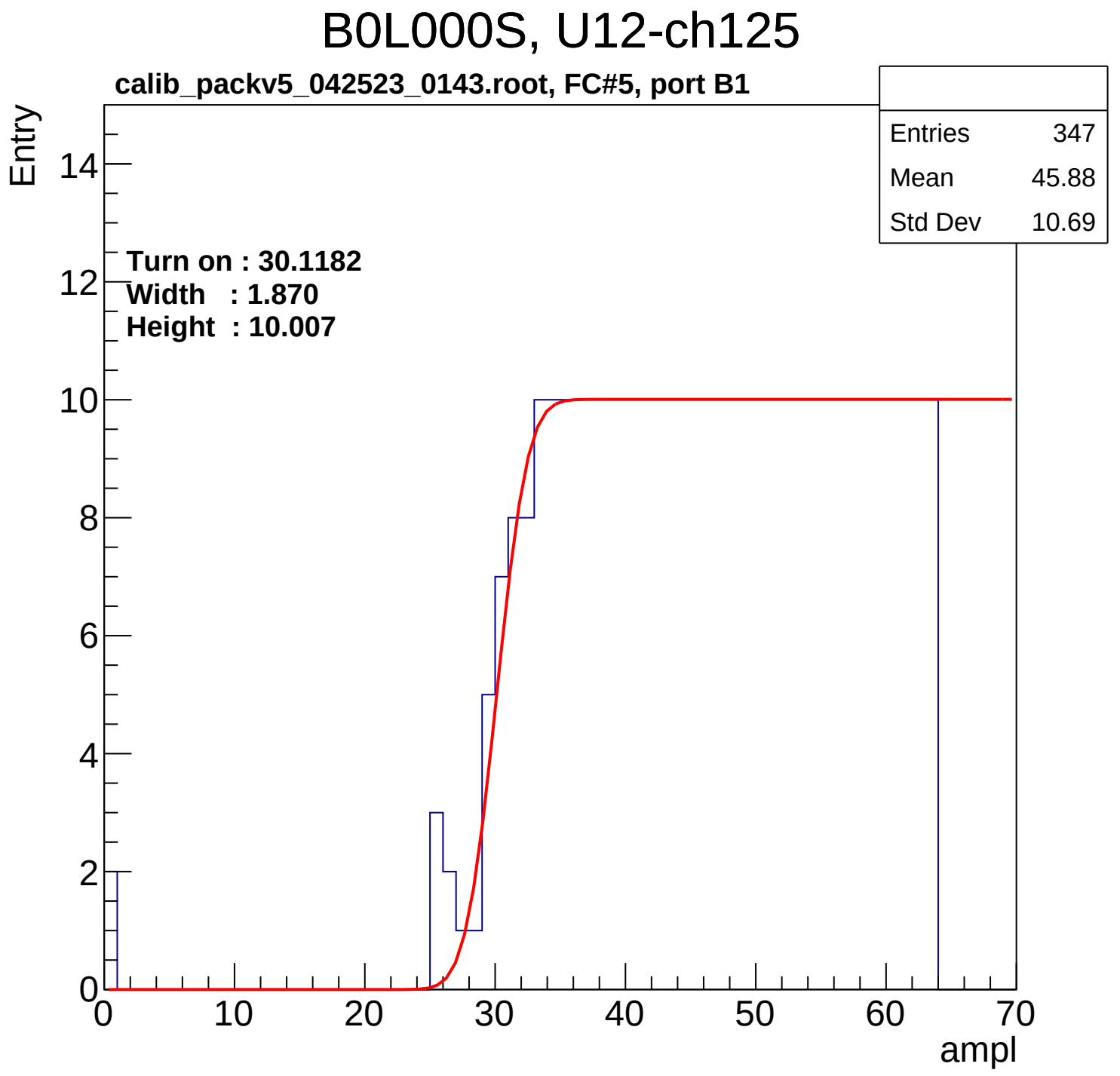
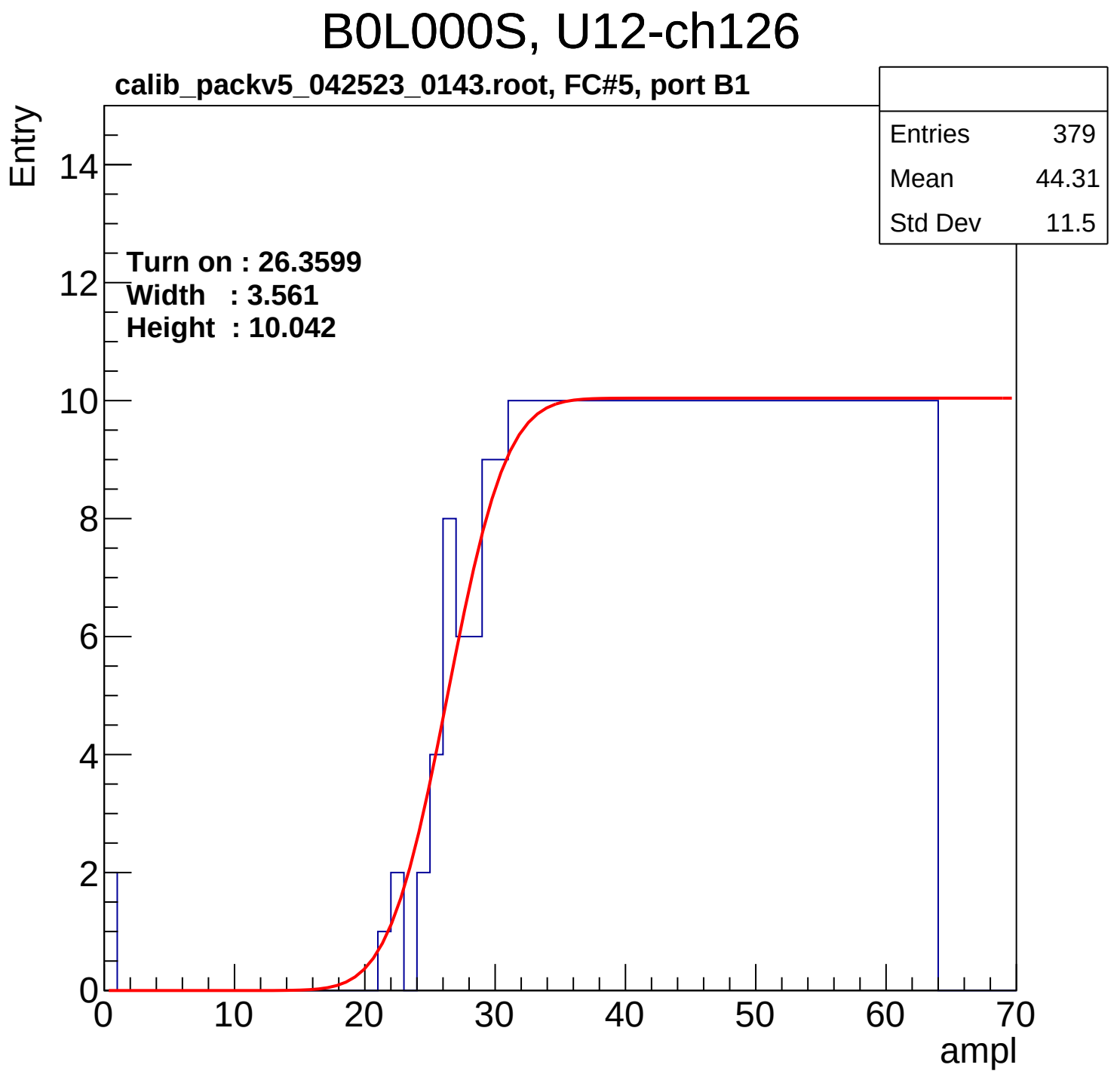

B0L000S, U12-ch125
calib_packv5_042523_0143.root, FC#5, port B1
Entries 347
Mean 45.88
Std Dev 10.69
Turn on : 30.1182
Width : 1.870
Height : 10.007
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L000S, U12-ch126
calib_packv5_042523_0143.root, FC#5, port B1
Entries 379
Mean 44.31
Std Dev 11.5
Turn on : 26.3599
Width : 3.561
Height : 10.042
Entry
ampl
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4
6
8
10
12
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0
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20
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60
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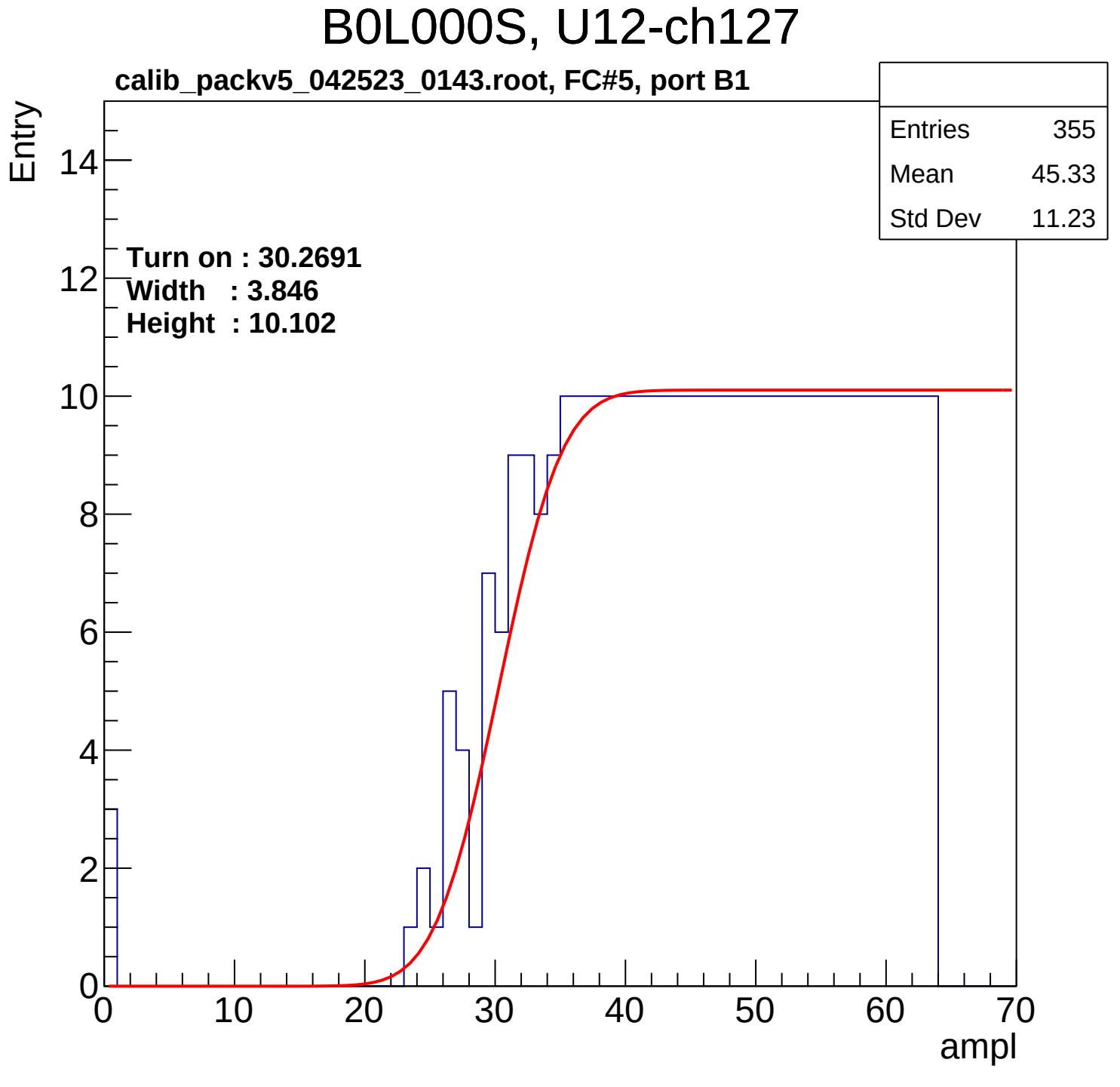
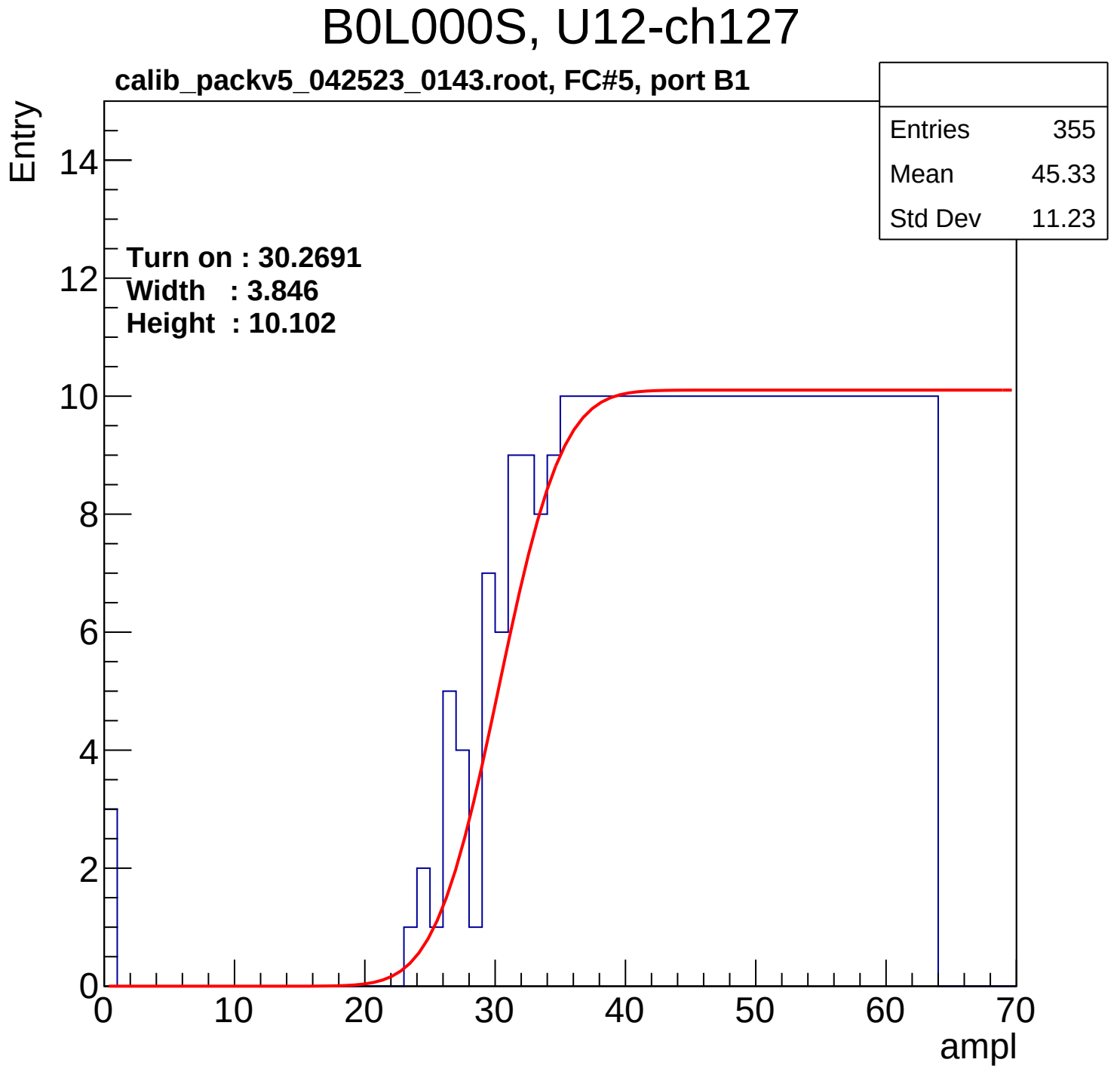

B0L000S, U12-ch127
calib_packv5_042523_0143.root, FC#5, port B1
Entries 355
Mean 45.33
Std Dev 11.23
Turn on : 30.2691
Width : 3.846
Height : 10.102
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L000S, U12-ch127
calib_packv5_042523_0143.root, FC#5, port B1
Entries 355
Mean 45.33
Std Dev 11.23
Turn on : 30.2691
Width : 3.846
Height : 10.102
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70