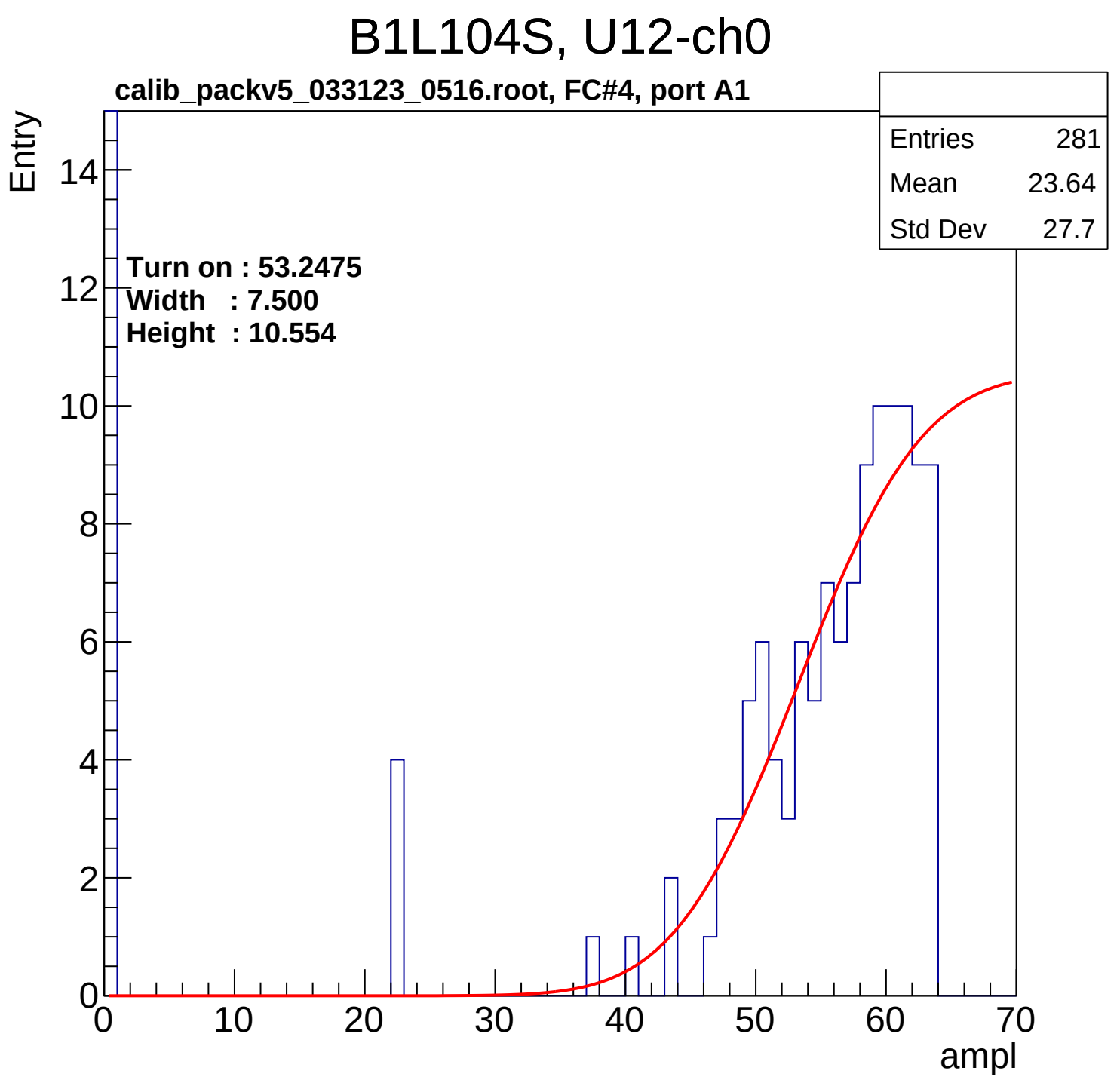
B1L104S, U12-ch0
calib_packv5_033123_0516.root, FC#4, port A1
Entries 281
Mean 23.64
Std Dev 27.7
Turn on : 53.2475
Width : 7.500
Height : 10.554
Entry
ampl
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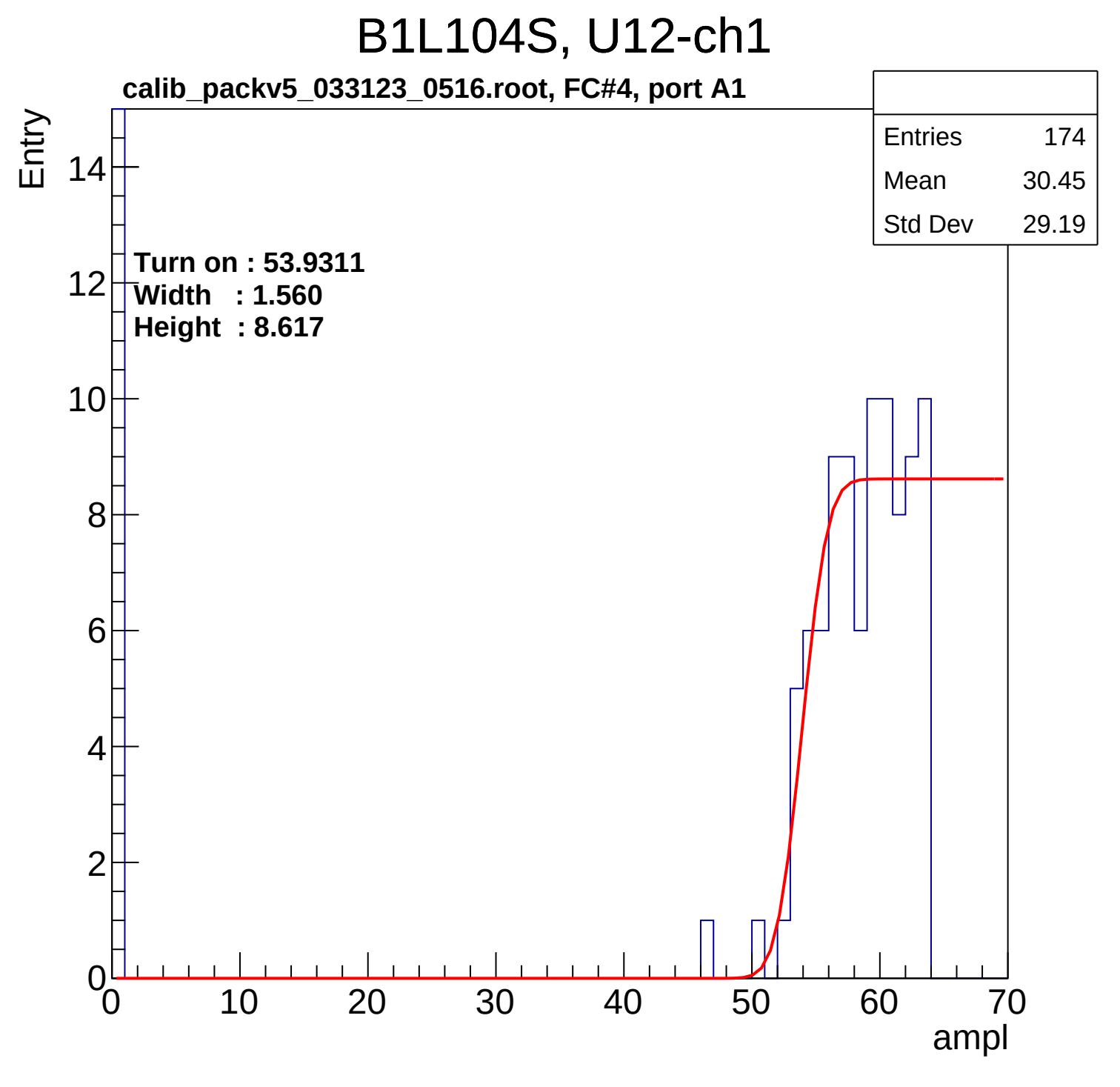
B1L104S, U12-ch1
calib_packv5_033123_0516.root, FC#4, port A1
Entries 174
Mean 30.45
Std Dev 29.19
Turn on : 53.9311
Width : 1.560
Height : 8.617
Entry
ampl
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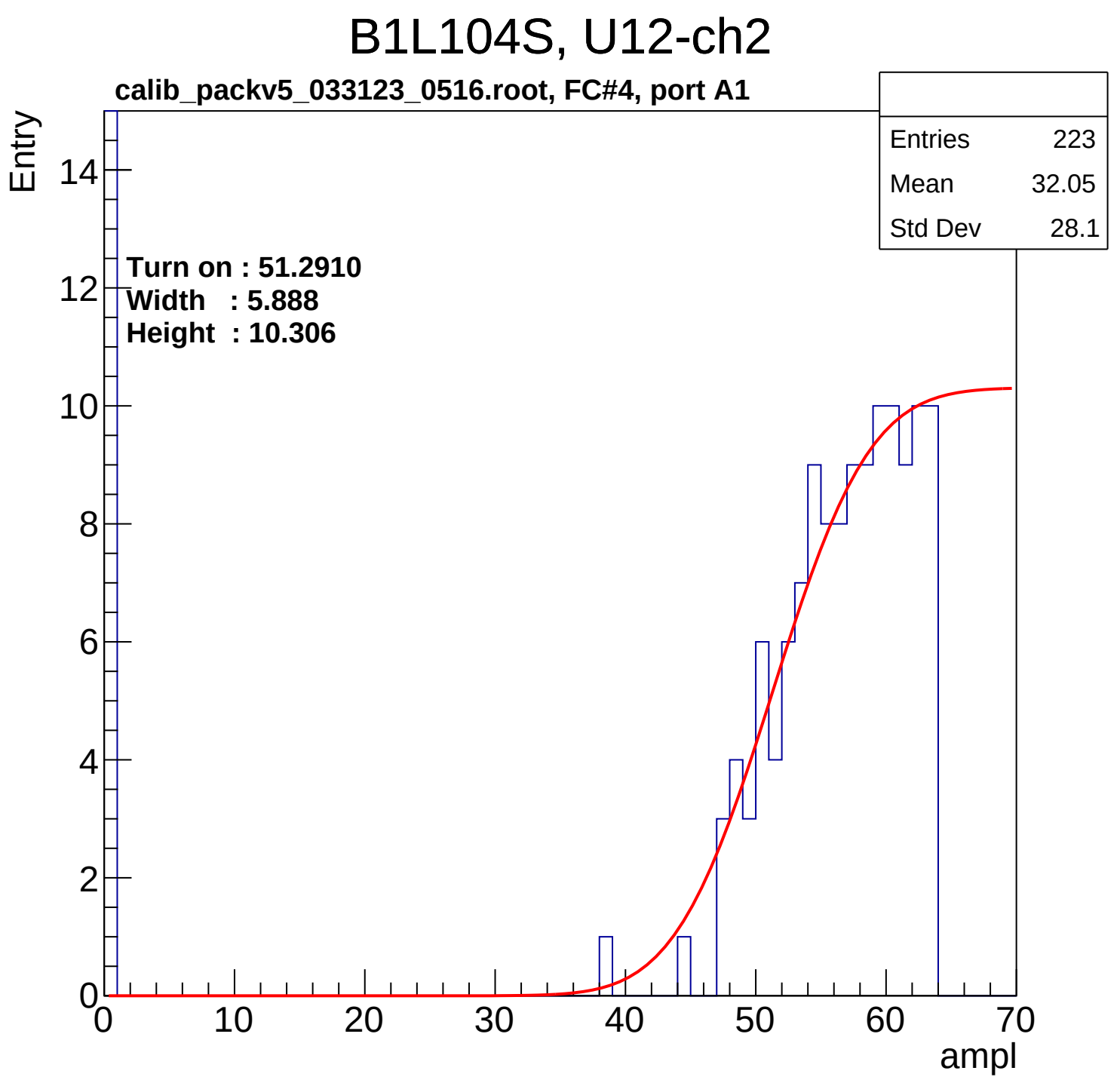
B1L104S, U12-ch2
calib_packv5_033123_0516.root, FC#4, port A1
Entries 223
Mean 32.05
Std Dev 28.1
Turn on : 51.2910
Width : 5.888
Height : 10.306
Entry
ampl
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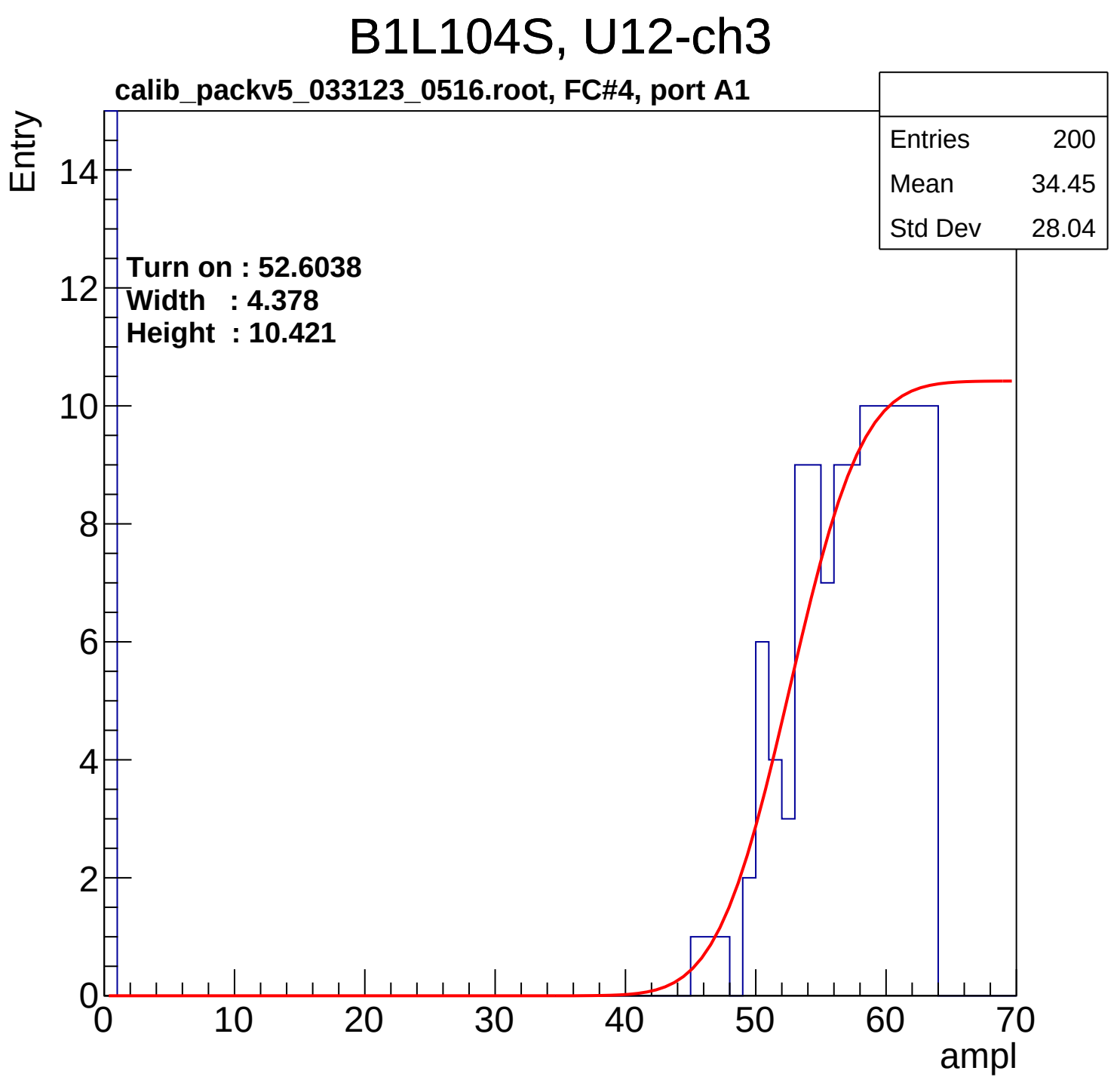
B1L104S, U12-ch3
calib_packv5_033123_0516.root, FC#4, port A1
Entries 200
Mean 34.45
Std Dev 28.04
Turn on : 52.6038
Width : 4.378
Height : 10.421
Entry
ampl
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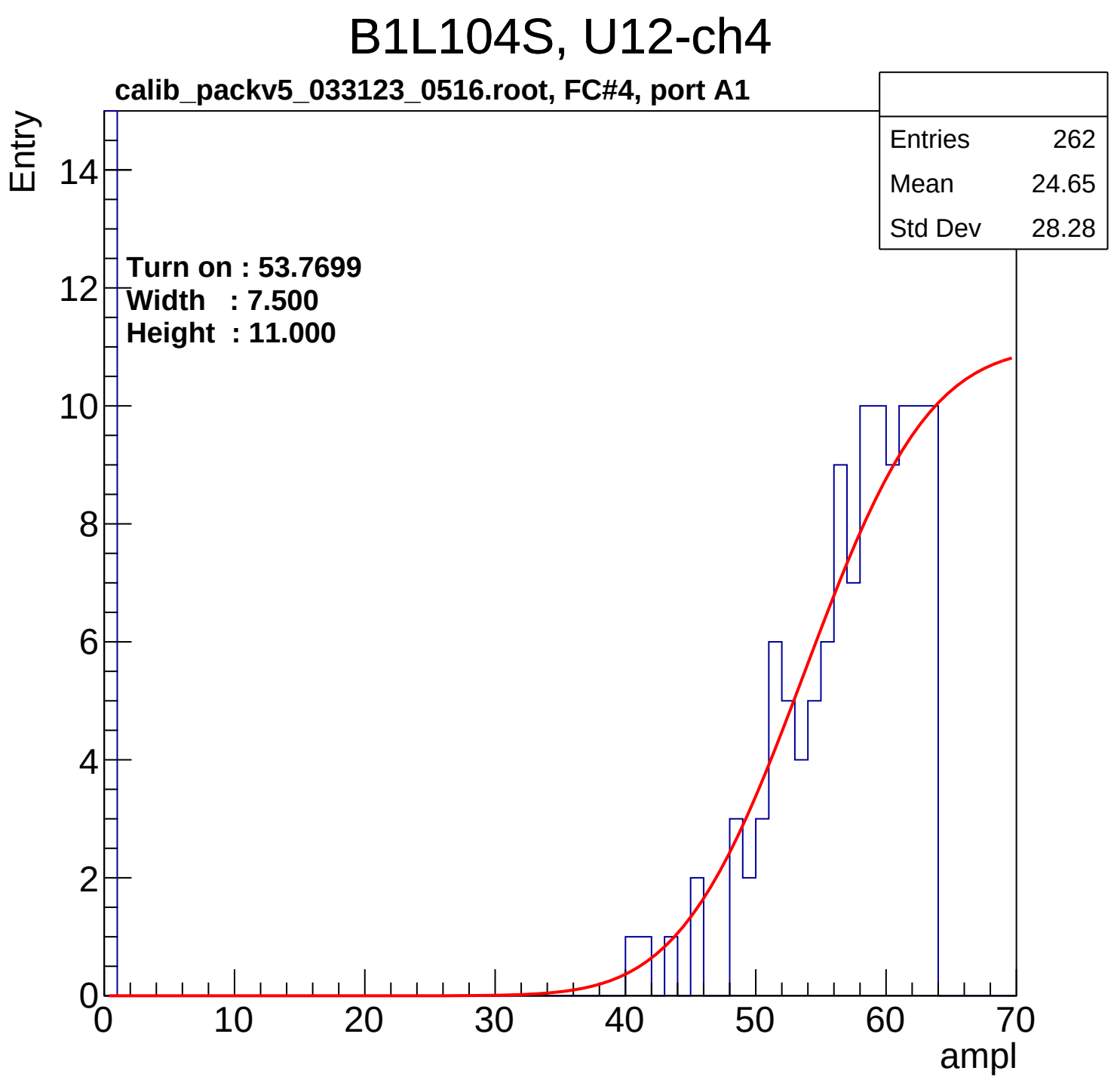
B1L104S, U12-ch4
calib_packv5_033123_0516.root, FC#4, port A1
Entries 262
Mean 24.65
Std Dev 28.28
Turn on : 53.7699
Width : 7.500
Height : 11.000
Entry
ampl
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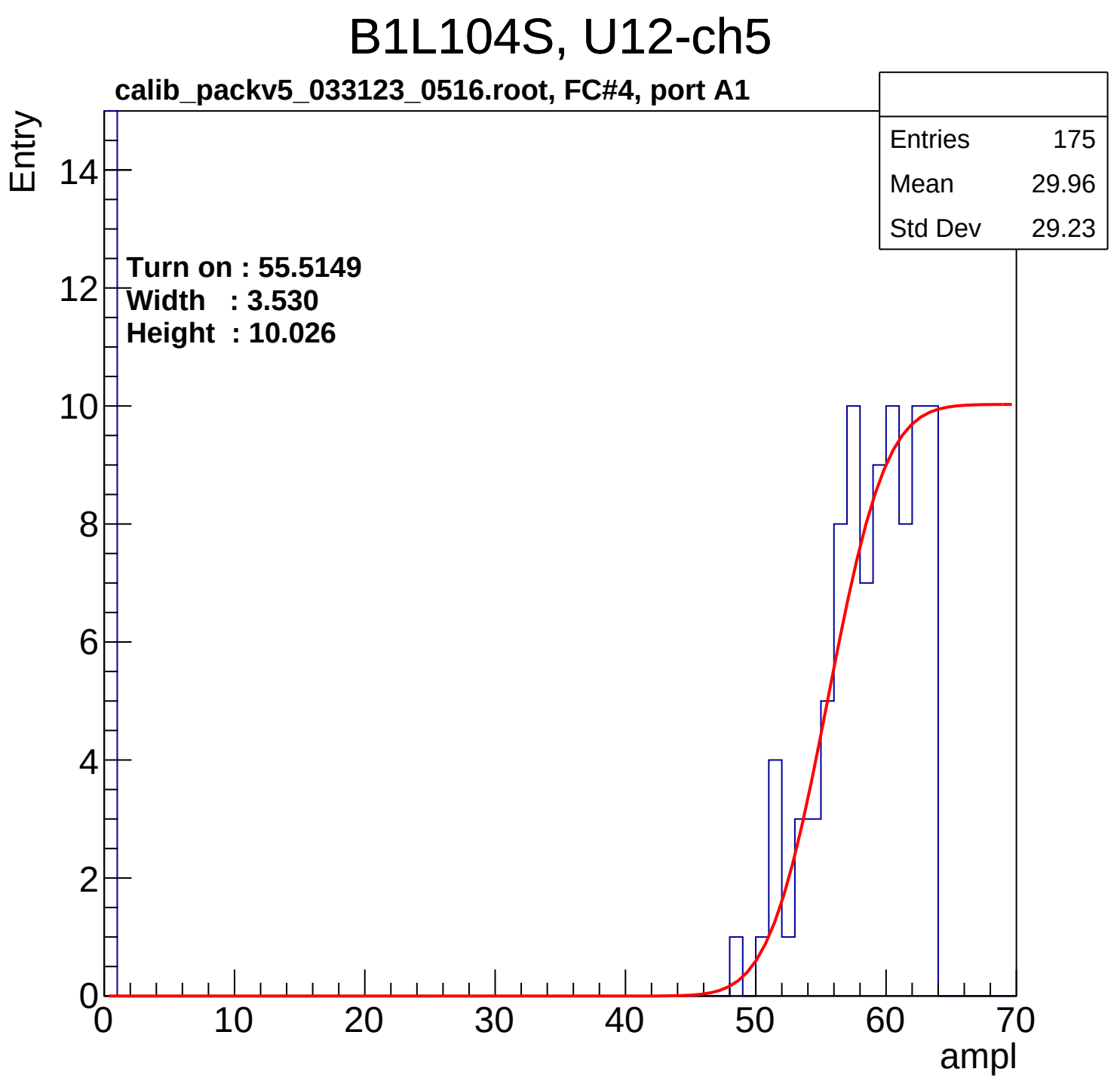
B1L104S, U12-ch5
calib_packv5_033123_0516.root, FC#4, port A1
Entries 175
Mean 29.96
Std Dev 29.23
Turn on : 55.5149
Width : 3.530
Height : 10.026
Entry
ampl
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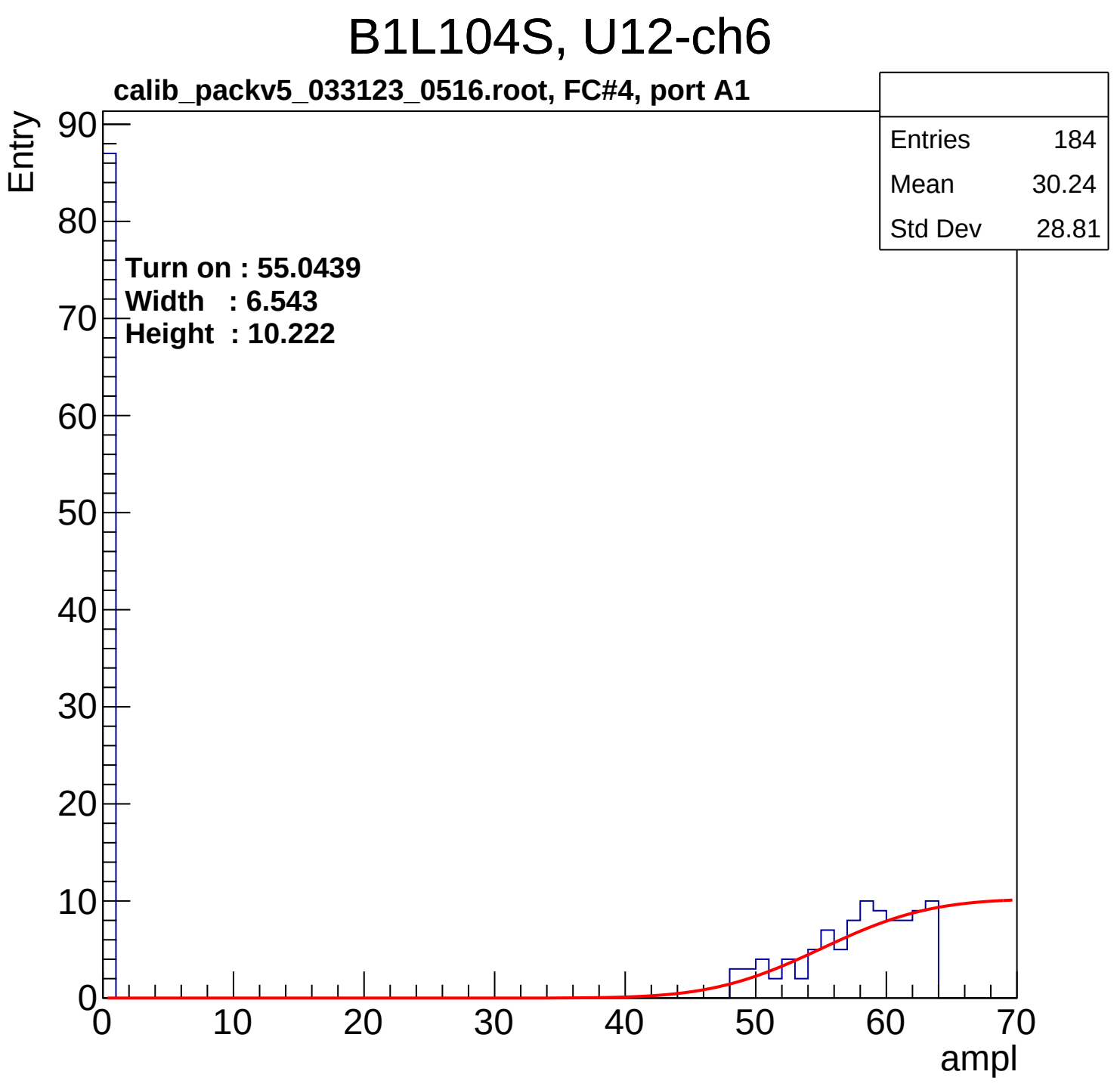
B1L104S, U12-ch6
calib_packv5_033123_0516.root, FC#4, port A1
Entries 184
Mean 30.24
Std Dev 28.81
Turn on : 55.0439
Width : 6.543
Height : 10.222
Entry
ampl
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20
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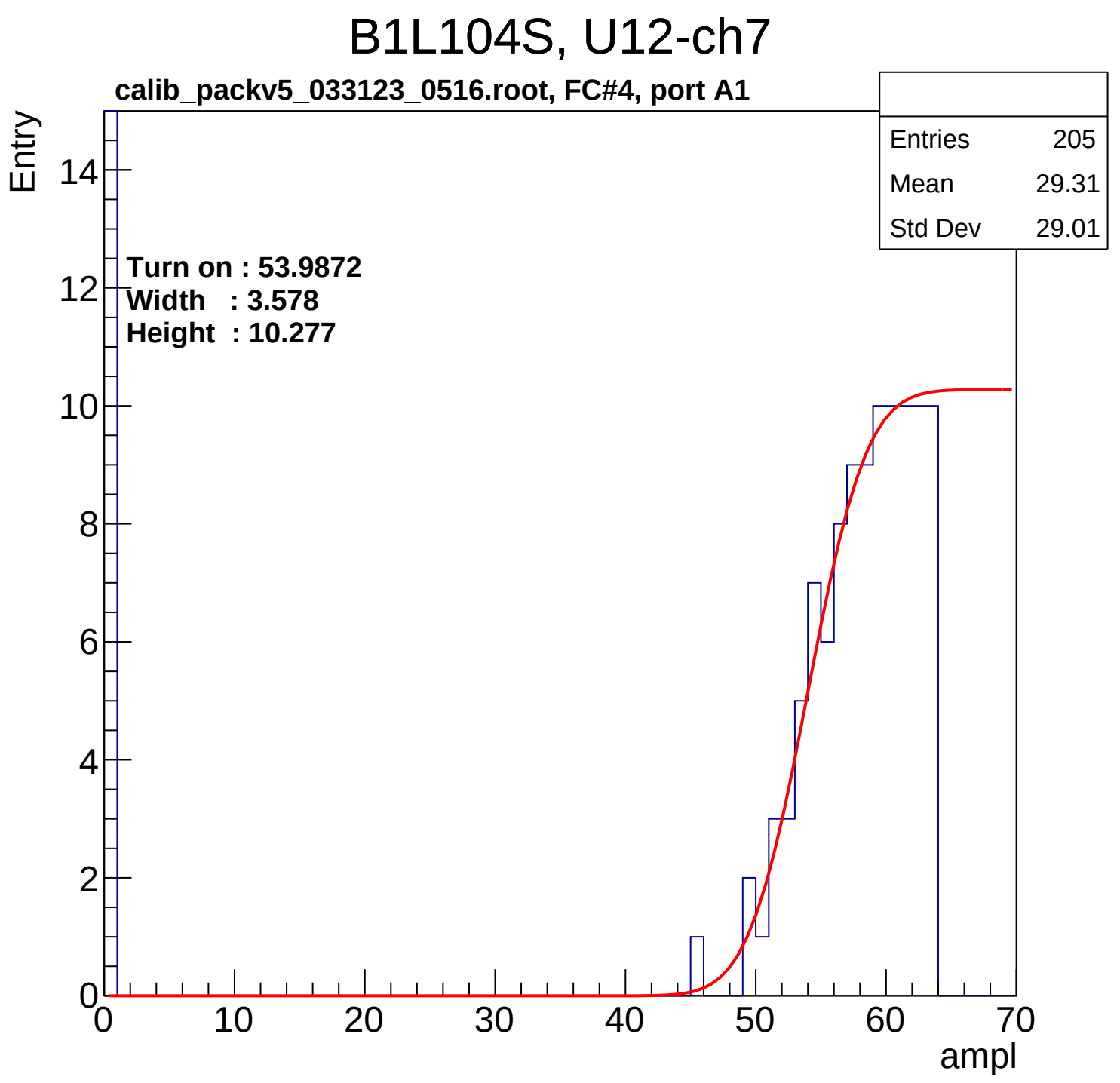
B1L104S, U12-ch7
calib_packv5_033123_0516.root, FC#4, port A1
Entries 205
Mean 29.31
Std Dev 29.01
Turn on : 53.9872
Width : 3.578
Height : 10.277
Entry
ampl
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6
8
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60
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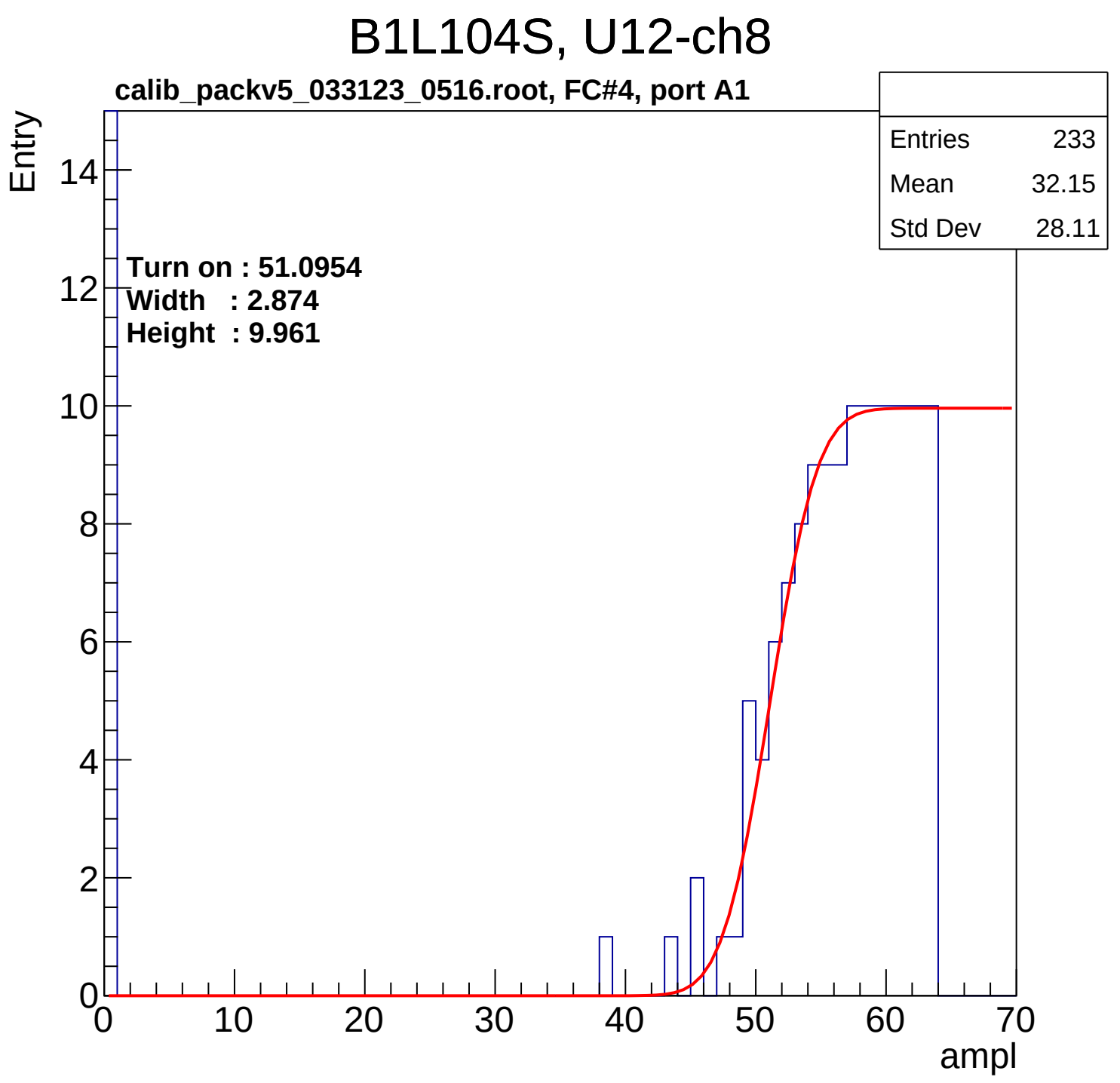
B1L104S, U12-ch8
calib_packv5_033123_0516.root, FC#4, port A1
Entries 233
Mean 32.15
Std Dev 28.11
Turn on : 51.0954
Width : 2.874
Height : 9.961
Entry
ampl
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6
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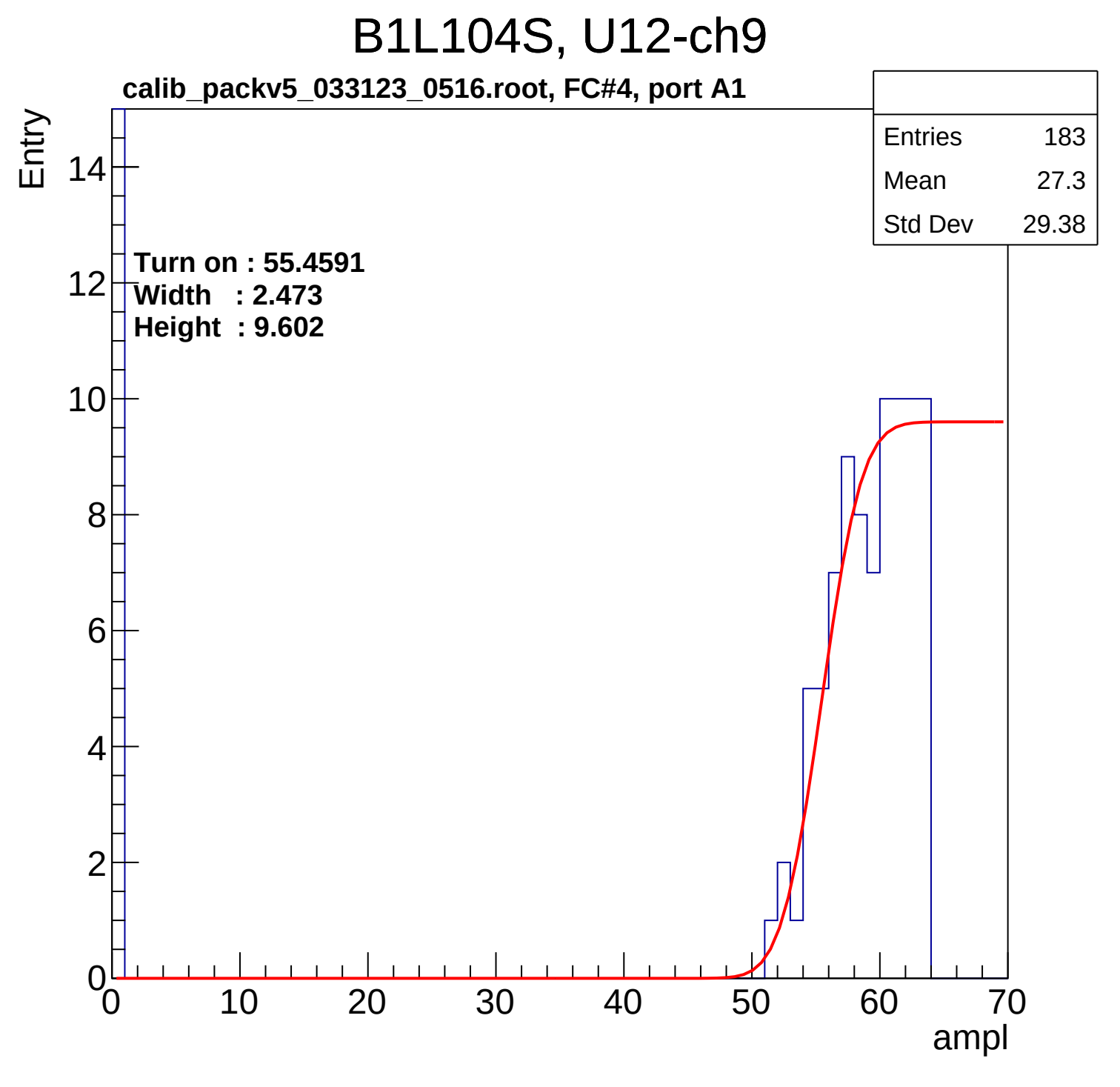
B1L104S, U12-ch9
calib_packv5_033123_0516.root, FC#4, port A1
Entries 183
Mean 27.3
Std Dev 29.38
Turn on : 55.4591
Width : 2.473
Height : 9.602
Entry
ampl
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4
6
8
10
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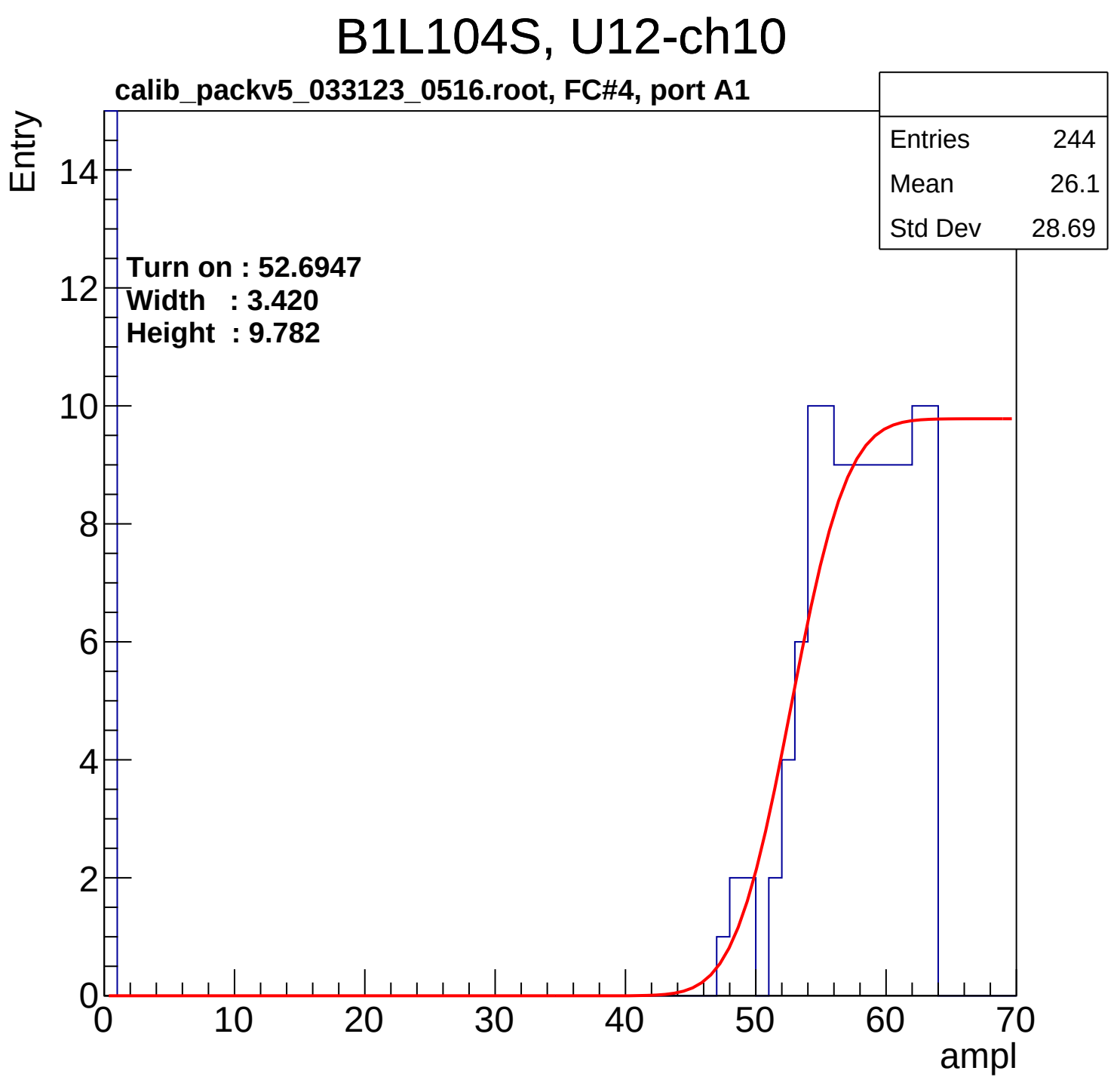
B1L104S, U12-ch10
calib_packv5_033123_0516.root, FC#4, port A1
Entries 244
Mean 26.1
Std Dev 28.69
Turn on : 52.6947
Width : 3.420
Height : 9.782
Entry
ampl
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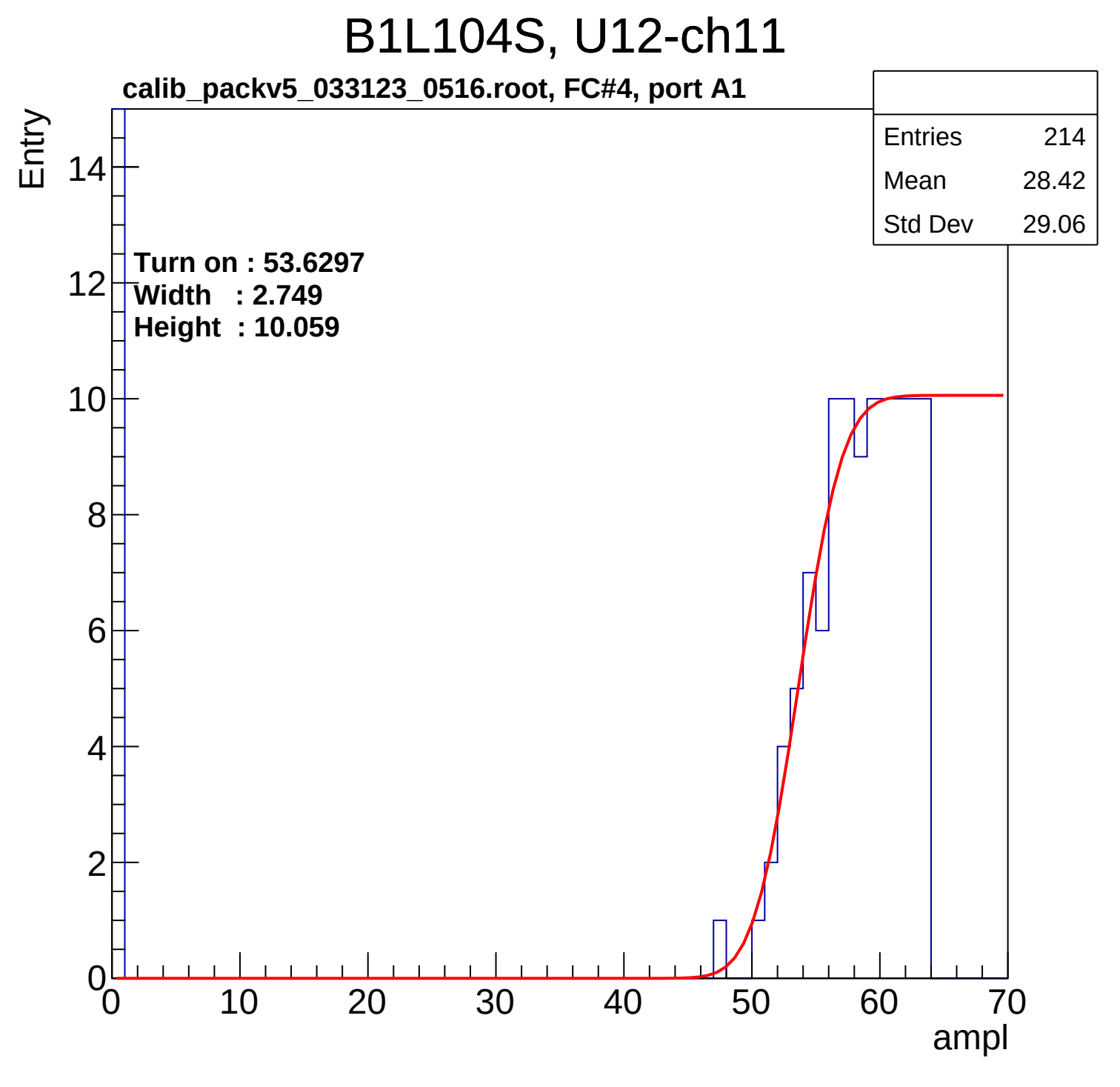
B1L104S, U12-ch11
calib_packv5_033123_0516.root, FC#4, port A1
Entries 214
Mean 28.42
Std Dev 29.06
Turn on : 53.6297
Width : 2.749
Height : 10.059
Entry
ampl
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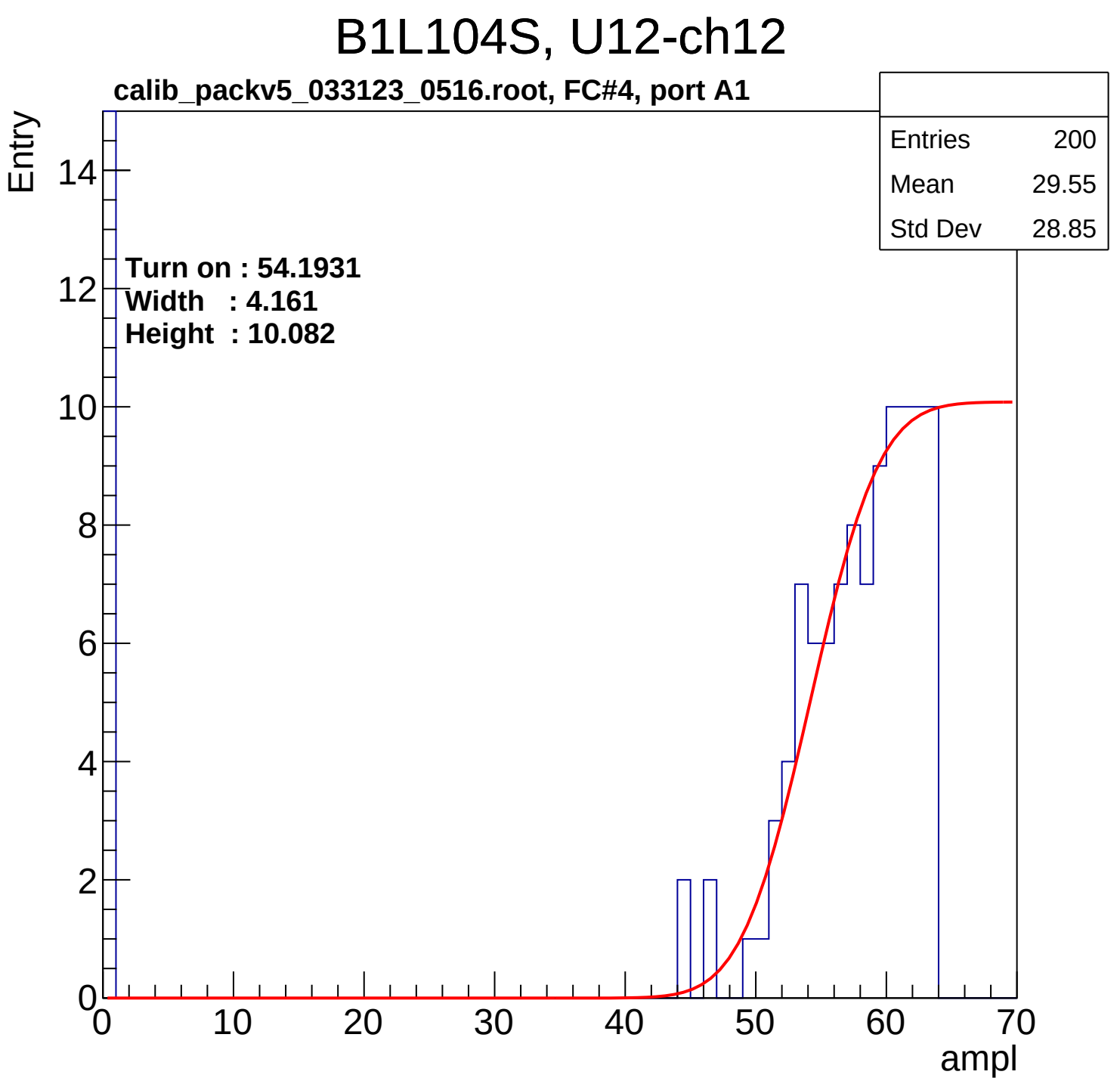
B1L104S, U12-ch12
calib_packv5_033123_0516.root, FC#4, port A1
Entries 200
Mean 29.55
Std Dev 28.85
Turn on : 54.1931
Width : 4.161
Height : 10.082
Entry
ampl
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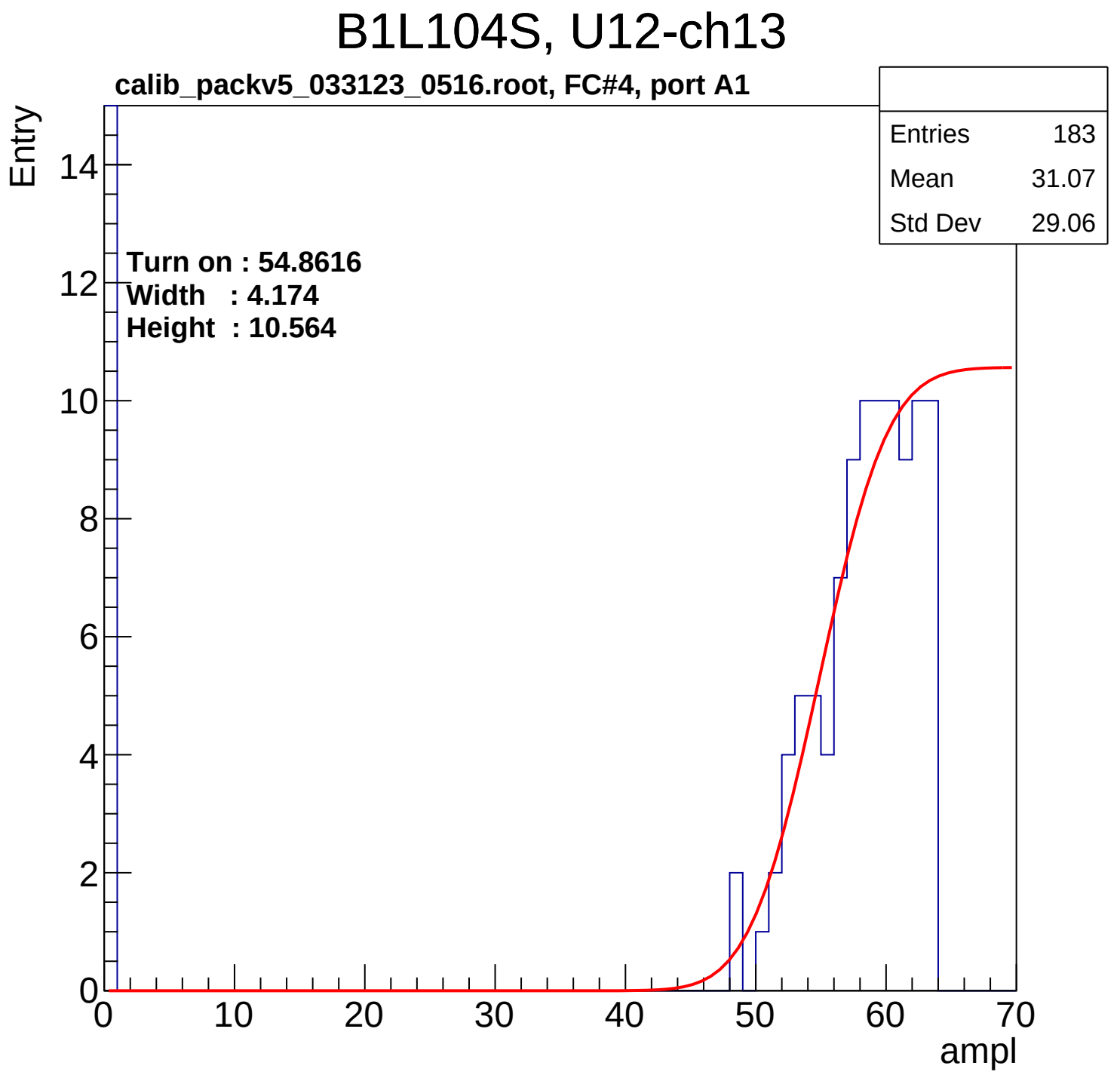
B1L104S, U12-ch13
calib_packv5_033123_0516.root, FC#4, port A1
Entries 183
Mean 31.07
Std Dev 29.06
Turn on : 54.8616
Width : 4.174
Height : 10.564
Entry
ampl
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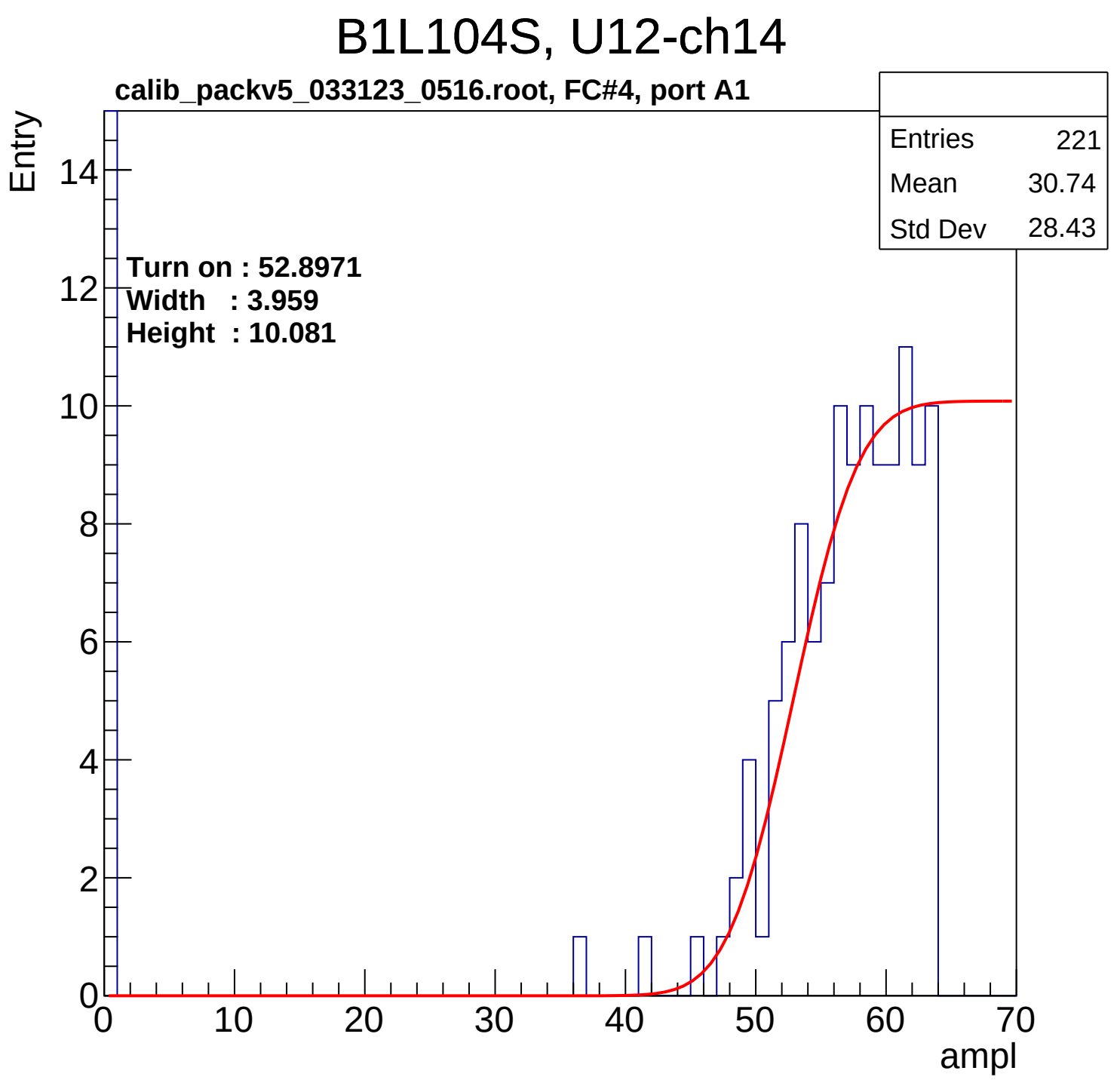
B1L104S, U12-ch14
calib_packv5_033123_0516.root, FC#4, port A1
Entries 221
Mean 30.74
Std Dev 28.43
Turn on : 52.8971
Width : 3.959
Height : 10.081
Entry
ampl
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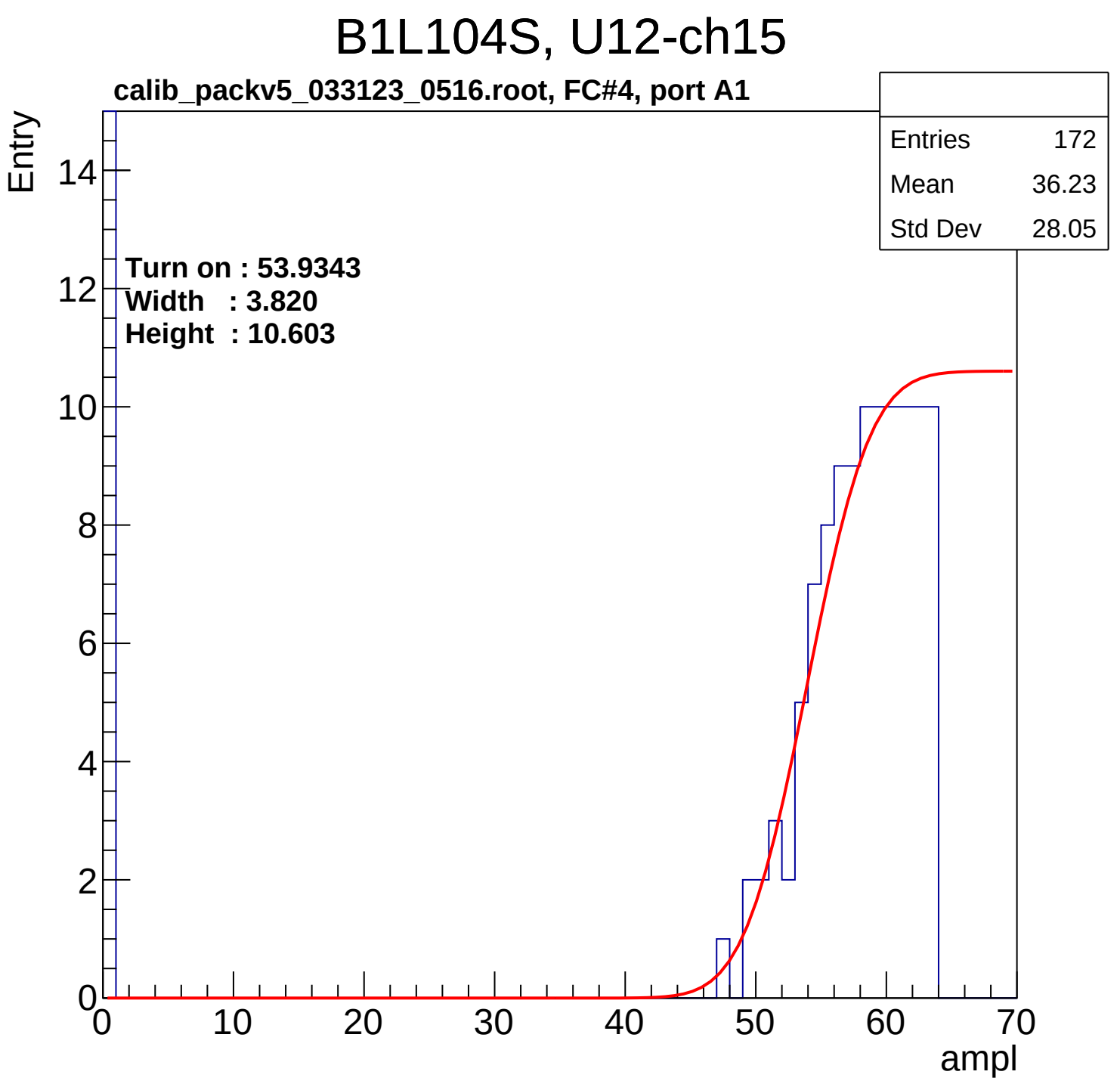
B1L104S, U12-ch15
calib_packv5_033123_0516.root, FC#4, port A1
Entries 172
Mean 36.23
Std Dev 28.05
Turn on : 53.9343
Width : 3.820
Height : 10.603
Entry
ampl
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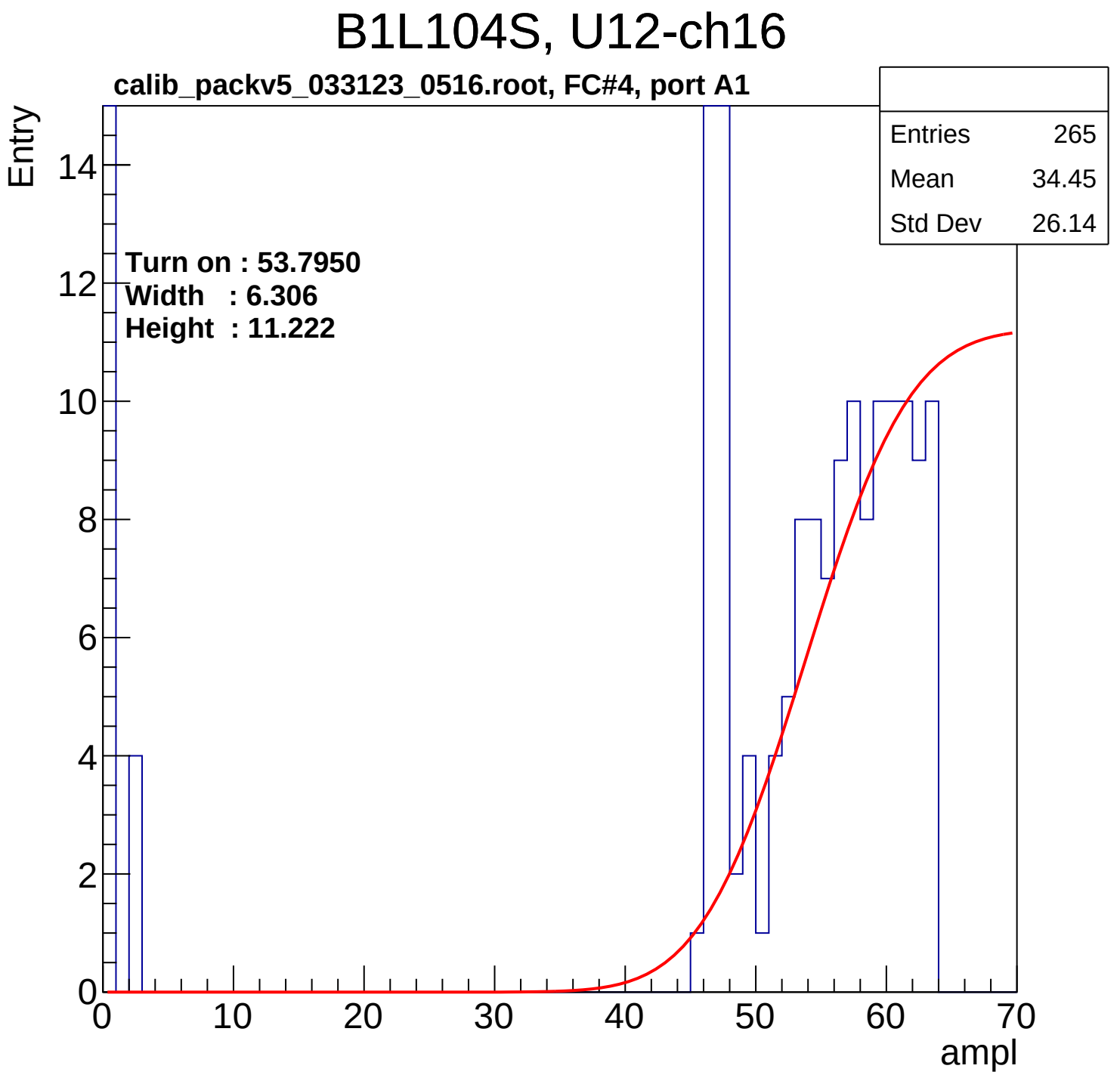
B1L104S, U12-ch16
calib_packv5_033123_0516.root, FC#4, port A1
Entries 265
Mean 34.45
Std Dev 26.14
Turn on : 53.7950
Width : 6.306
Height : 11.222
Entry
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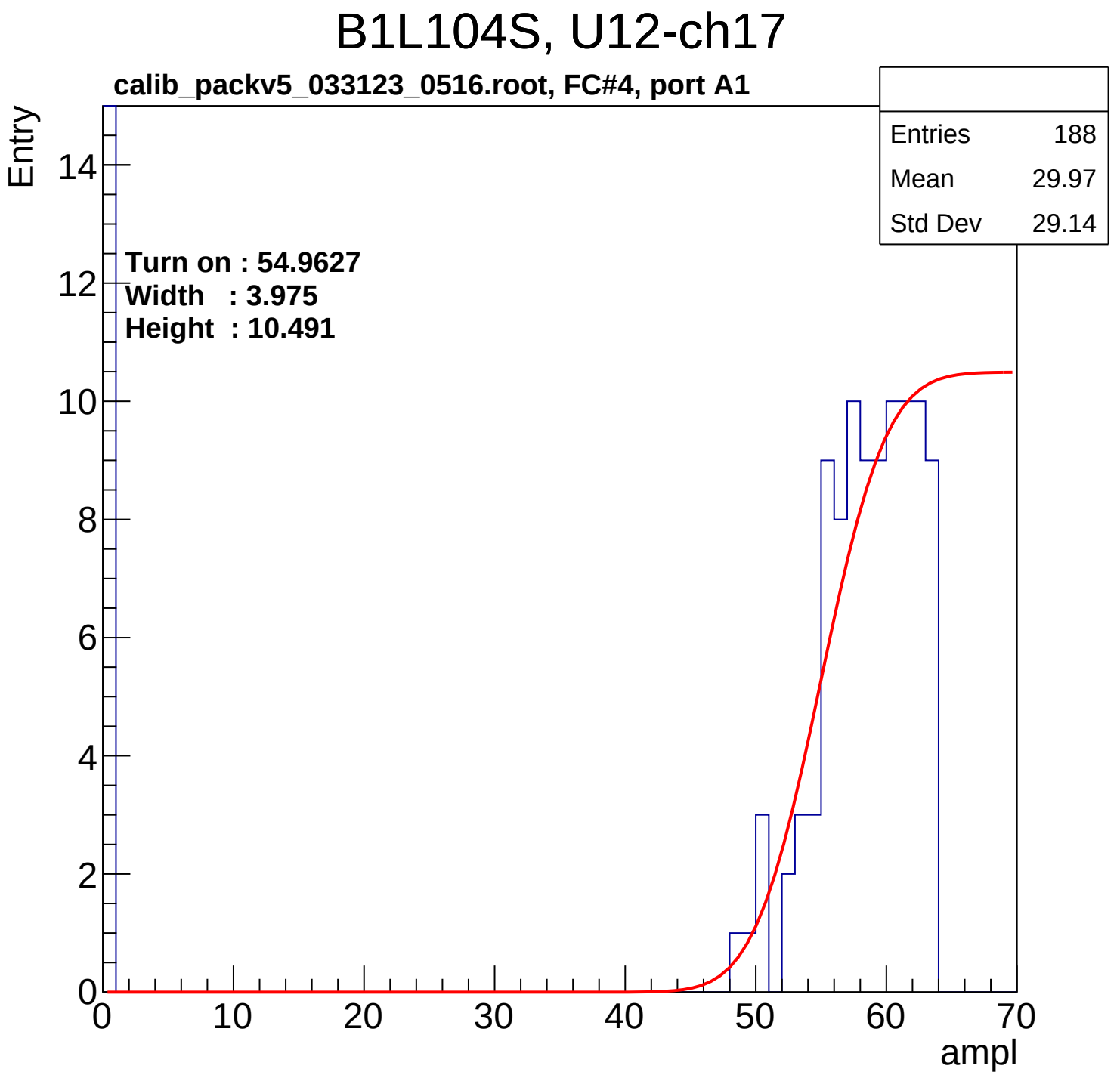
B1L104S, U12-ch17
calib_packv5_033123_0516.root, FC#4, port A1
Entries 188
Mean 29.97
Std Dev 29.14
Turn on : 54.9627
Width : 3.975
Height : 10.491
Entry
ampl
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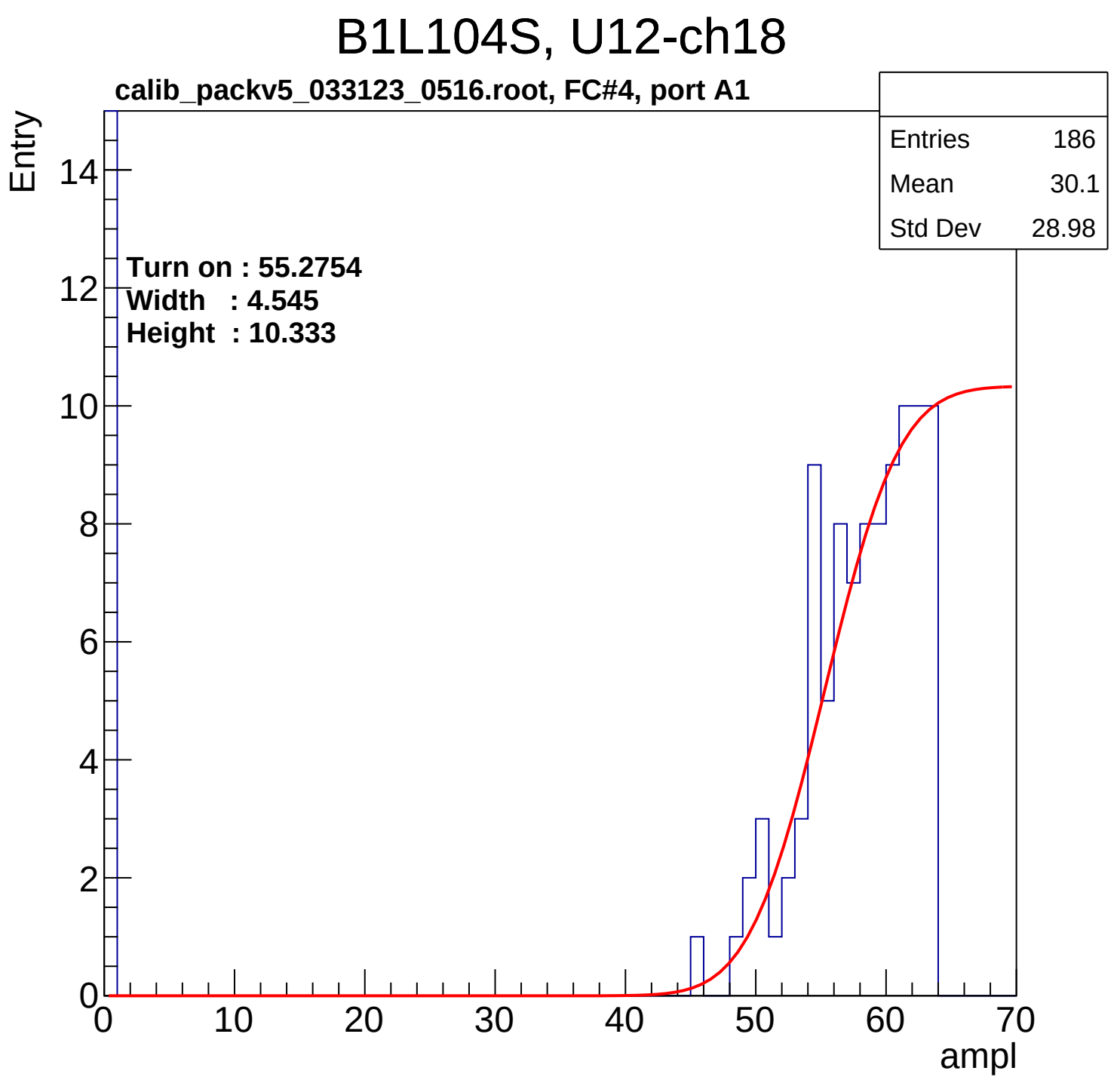
B1L104S, U12-ch18
calib_packv5_033123_0516.root, FC#4, port A1
Entries 186
Mean 30.1
Std Dev 28.98
Turn on : 55.2754
Width : 4.545
Height : 10.333
Entry
ampl
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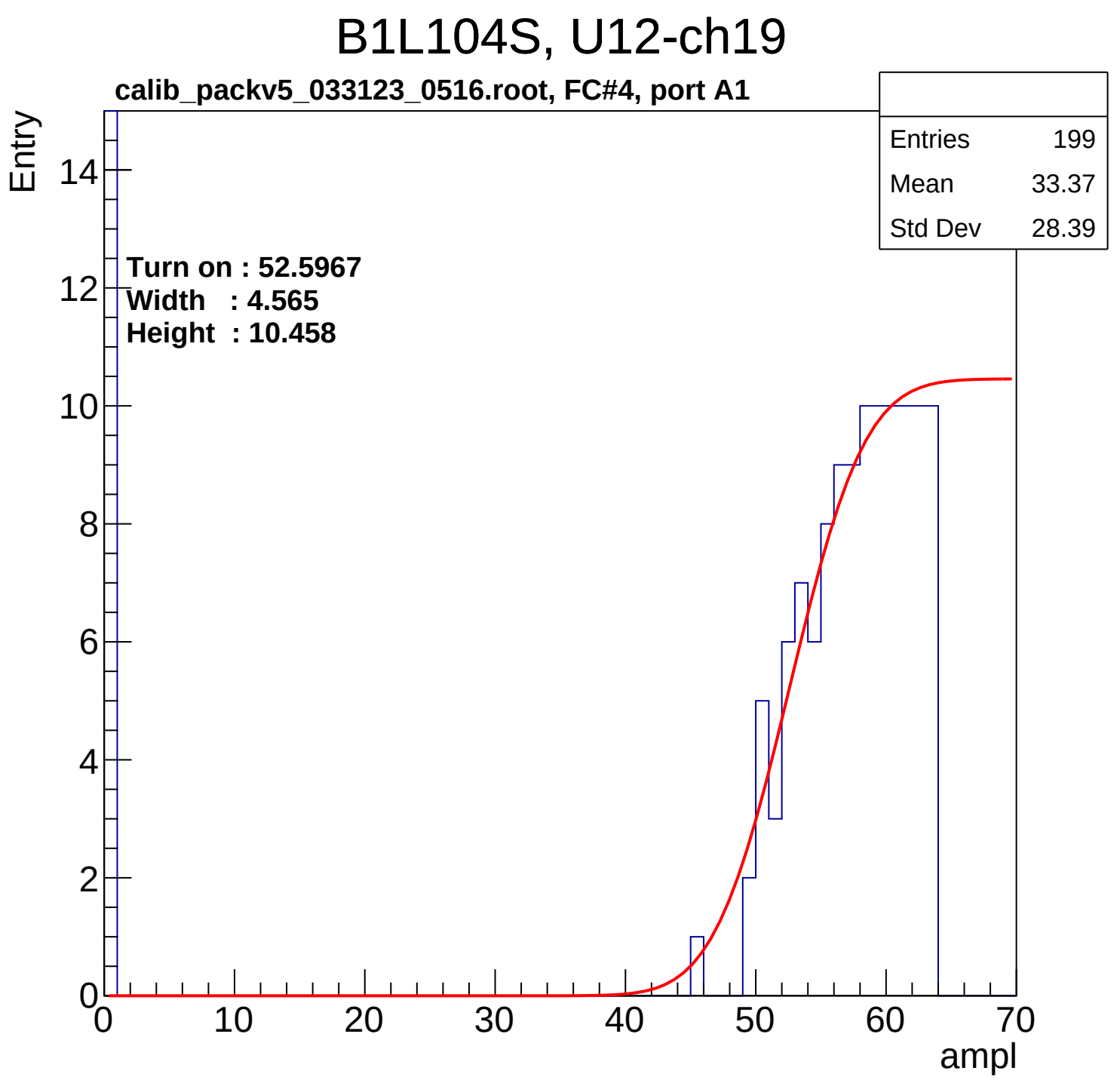
B1L104S, U12-ch19
calib_packv5_033123_0516.root, FC#4, port A1
Entries 199
Mean 33.37
Std Dev 28.39
Turn on : 52.5967
Width : 4.565
Height : 10.458
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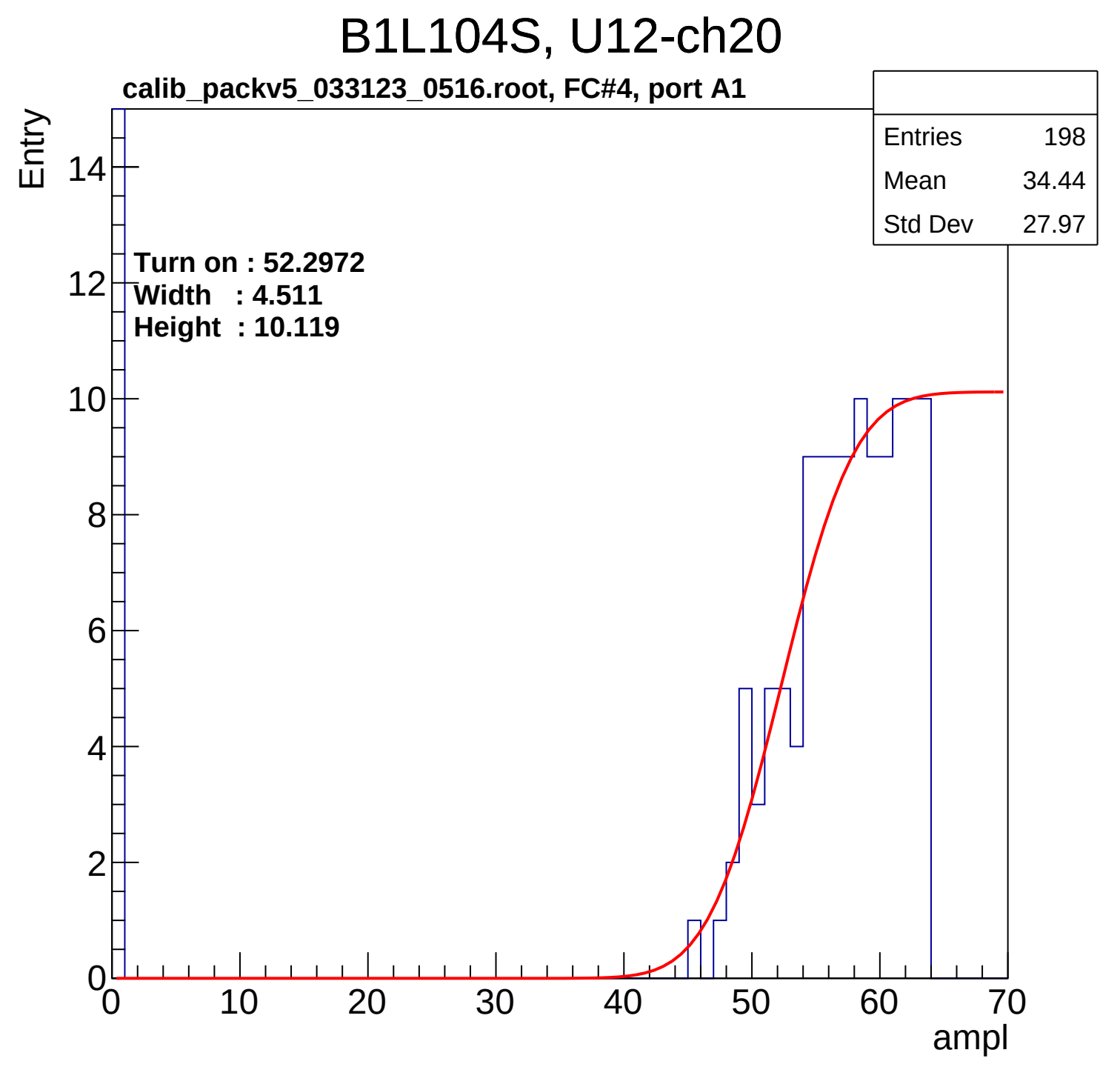
B1L104S, U12-ch20
calib_packv5_033123_0516.root, FC#4, port A1
Entries 198
Mean 34.44
Std Dev 27.97
Turn on : 52.2972
Width : 4.511
Height : 10.119
Entry
ampl
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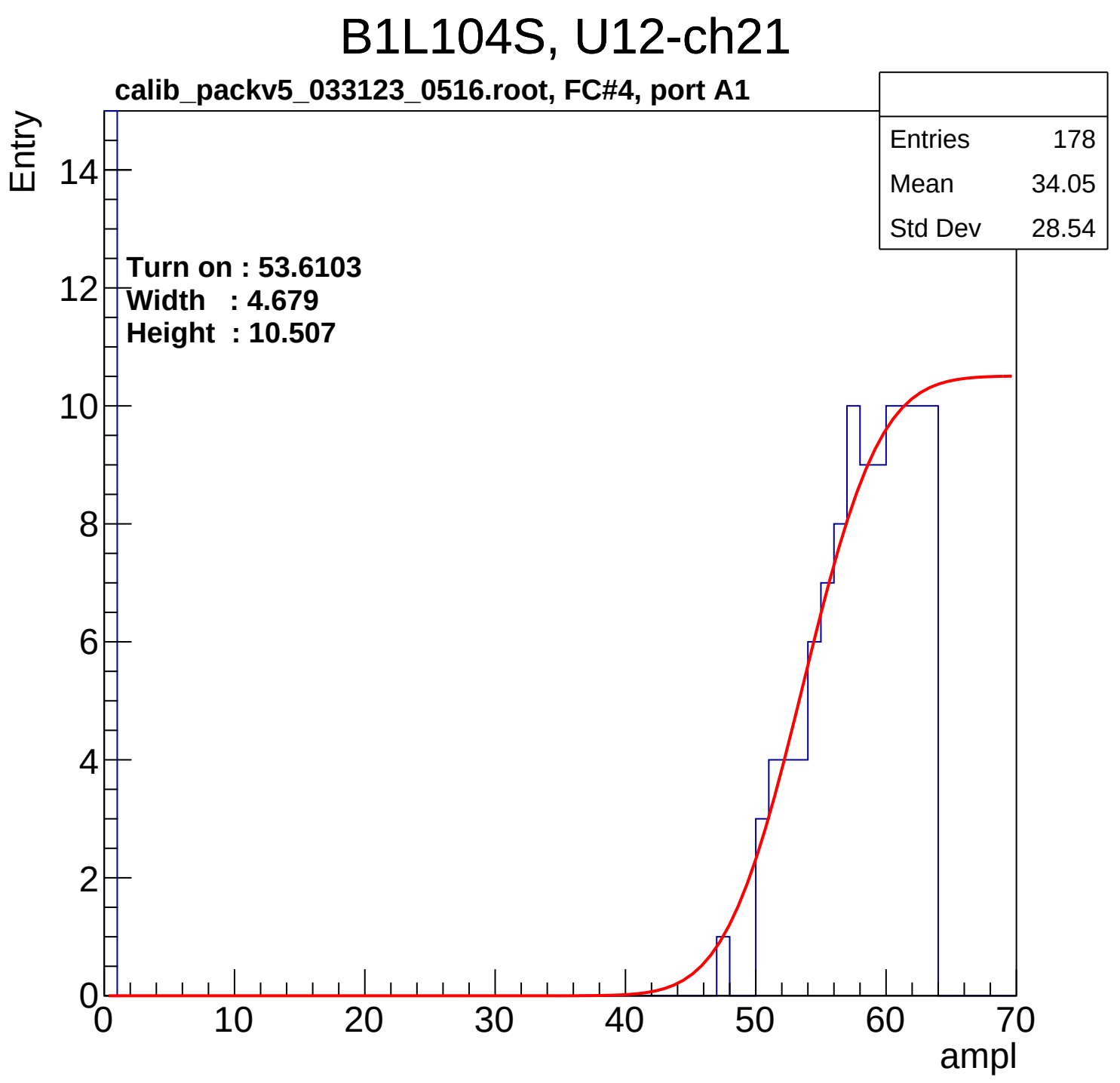
B1L104S, U12-ch21
calib_packv5_033123_0516.root, FC#4, port A1
Entries 178
Mean 34.05
Std Dev 28.54
Turn on : 53.6103
Width : 4.679
Height : 10.507
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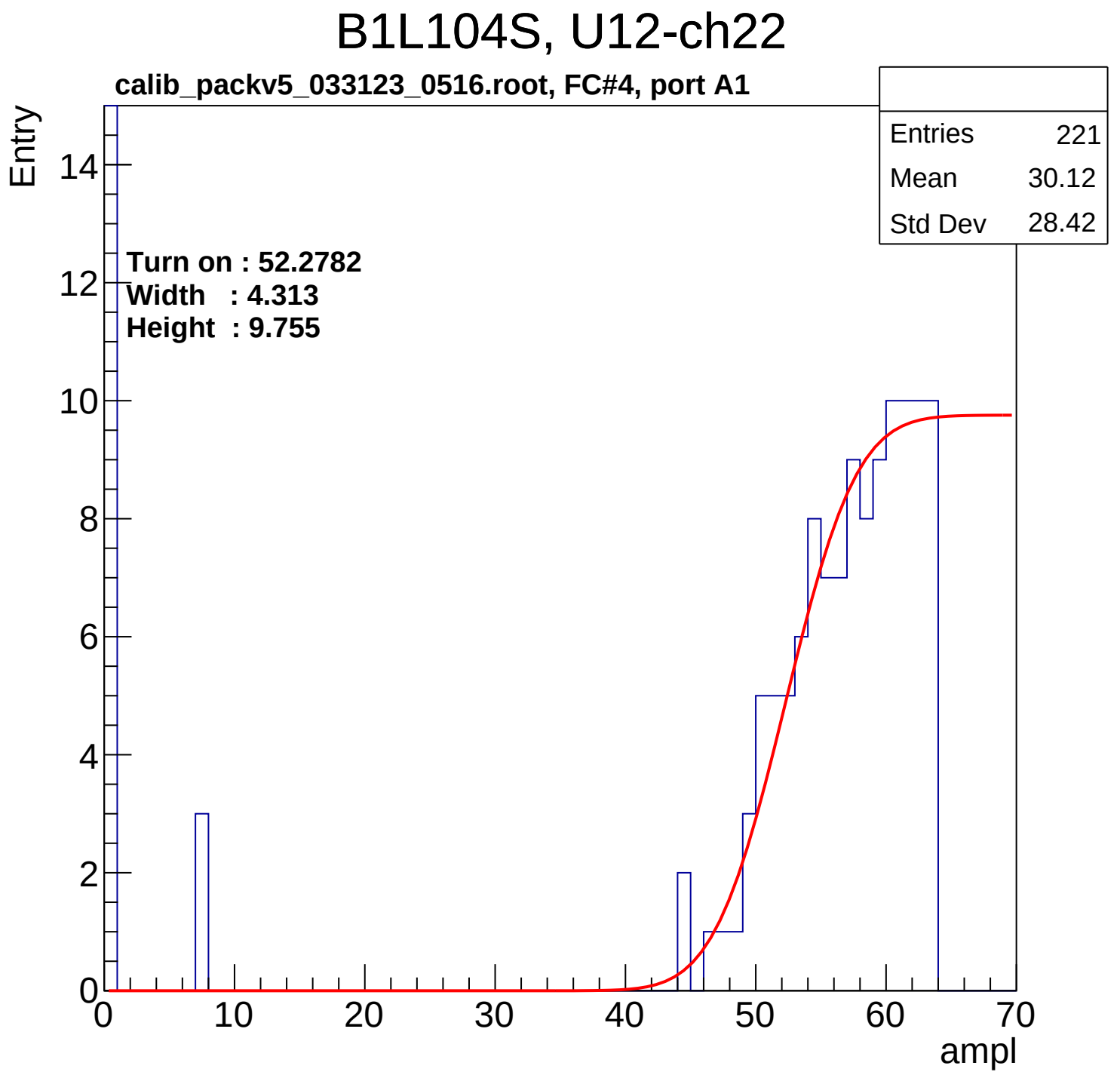
B1L104S, U12-ch22
calib_packv5_033123_0516.root, FC#4, port A1
Entries 221
Mean 30.12
Std Dev 28.42
Turn on : 52.2782
Width : 4.313
Height : 9.755
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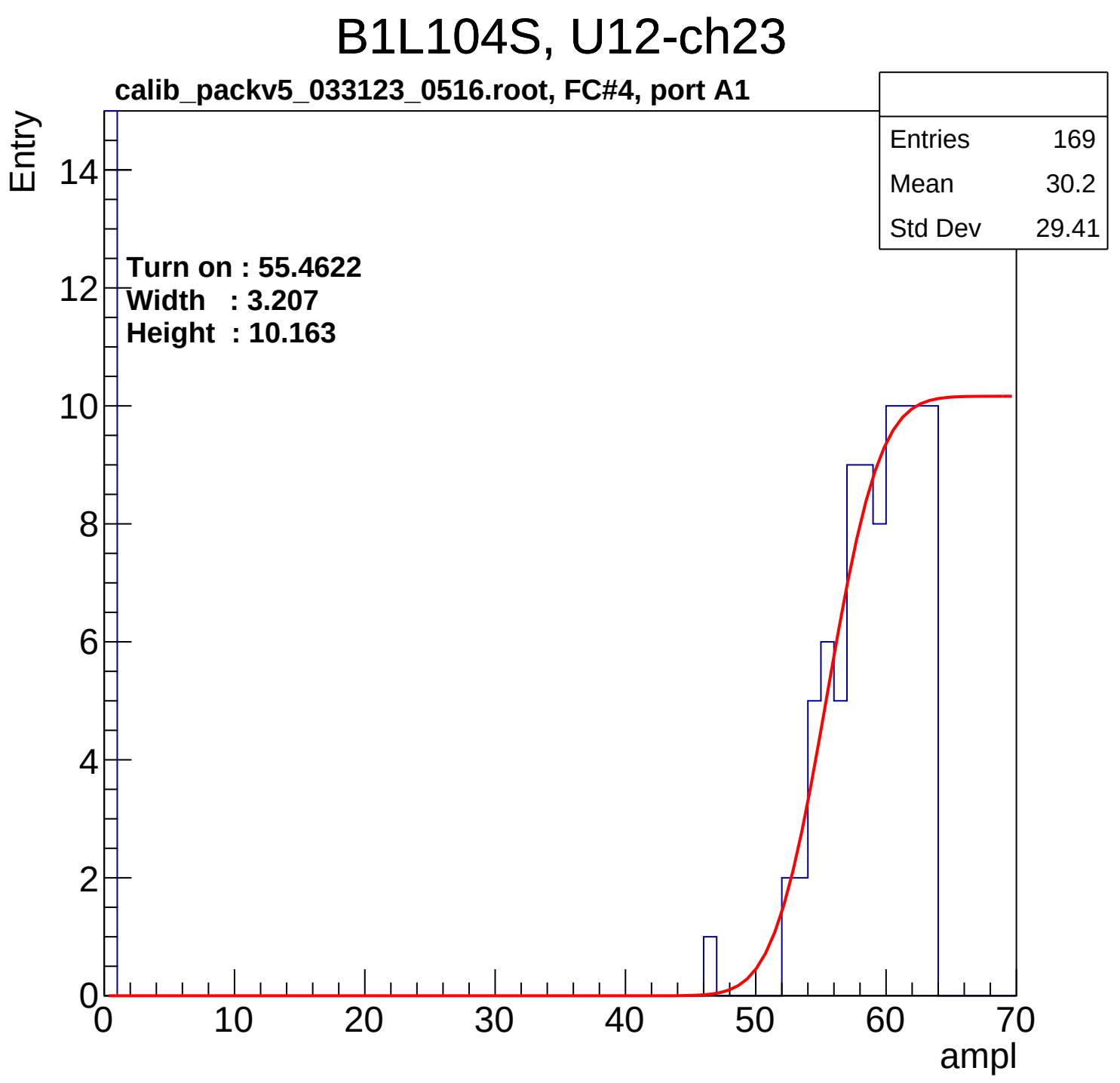
B1L104S, U12-ch23
calib_packv5_033123_0516.root, FC#4, port A1
Entries 169
Mean 30.2
Std Dev 29.41
Turn on : 55.4622
Width : 3.207
Height : 10.163
Entry
ampl
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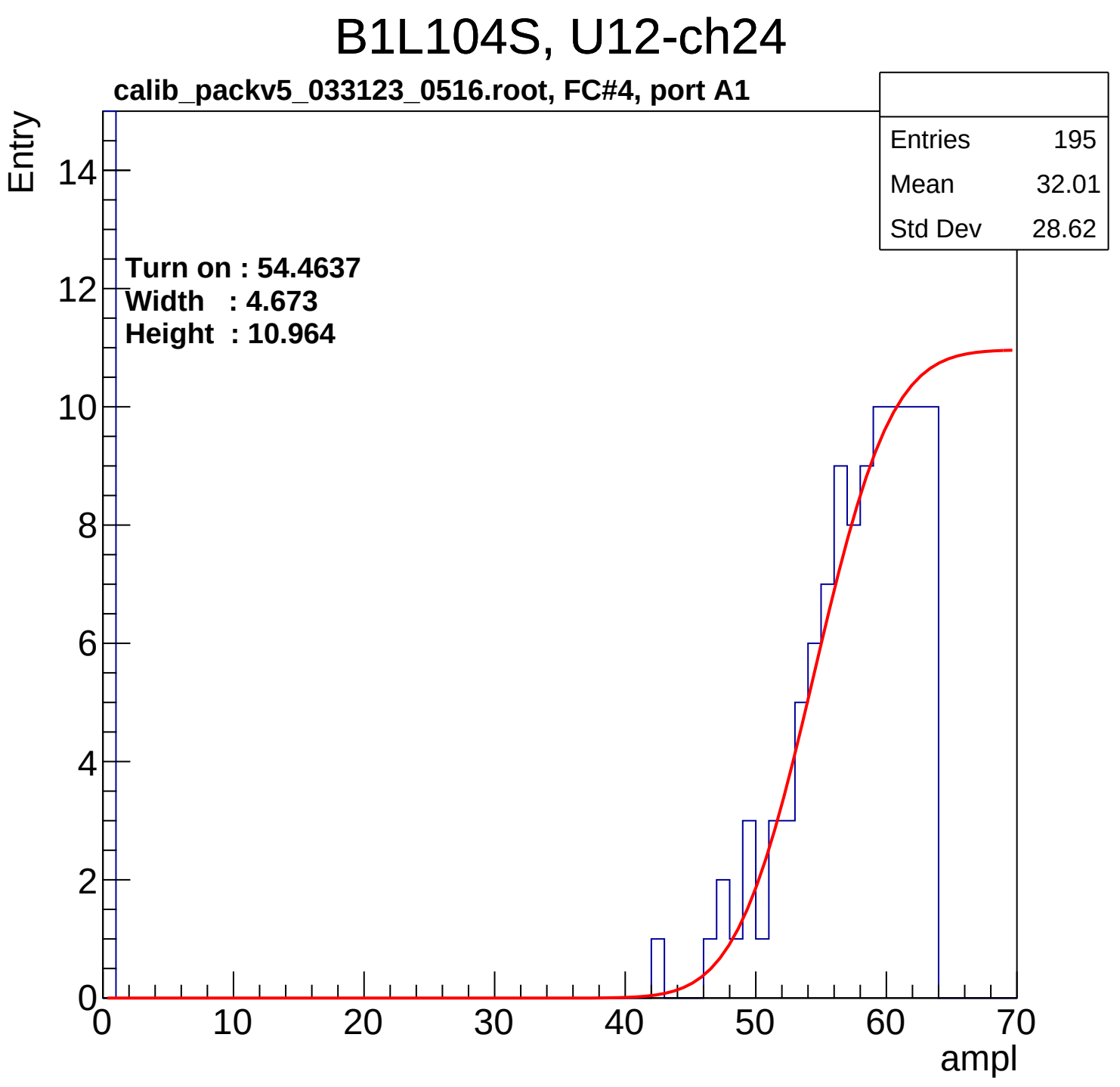
B1L104S, U12-ch24
calib_packv5_033123_0516.root, FC#4, port A1
Entries 195
Mean 32.01
Std Dev 28.62
Turn on : 54.4637
Width : 4.673
Height : 10.964
Entry
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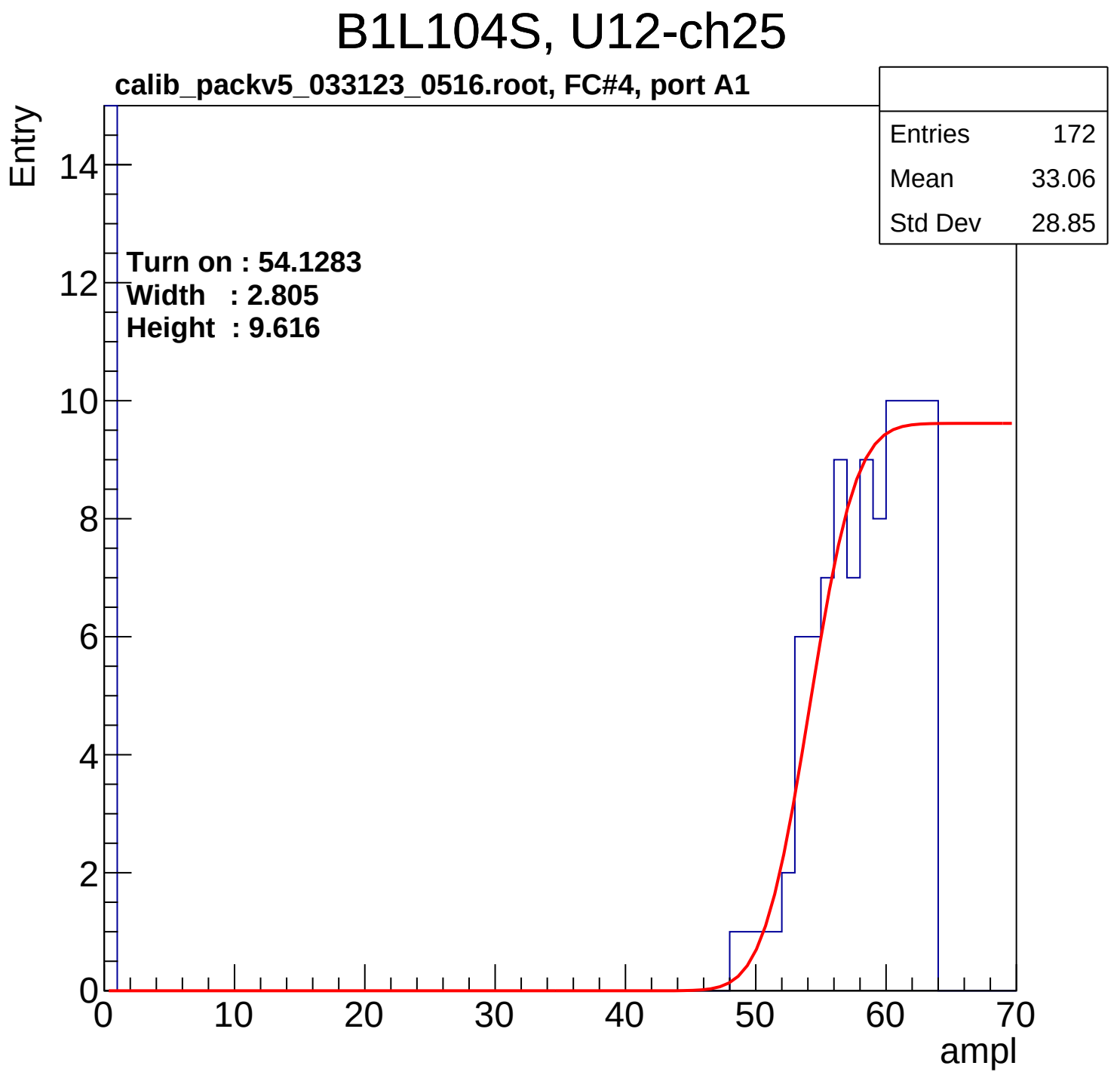
B1L104S, U12-ch25
calib_packv5_033123_0516.root, FC#4, port A1
Entries 172
Mean 33.06
Std Dev 28.85
Turn on : 54.1283
Width : 2.805
Height : 9.616
Entry
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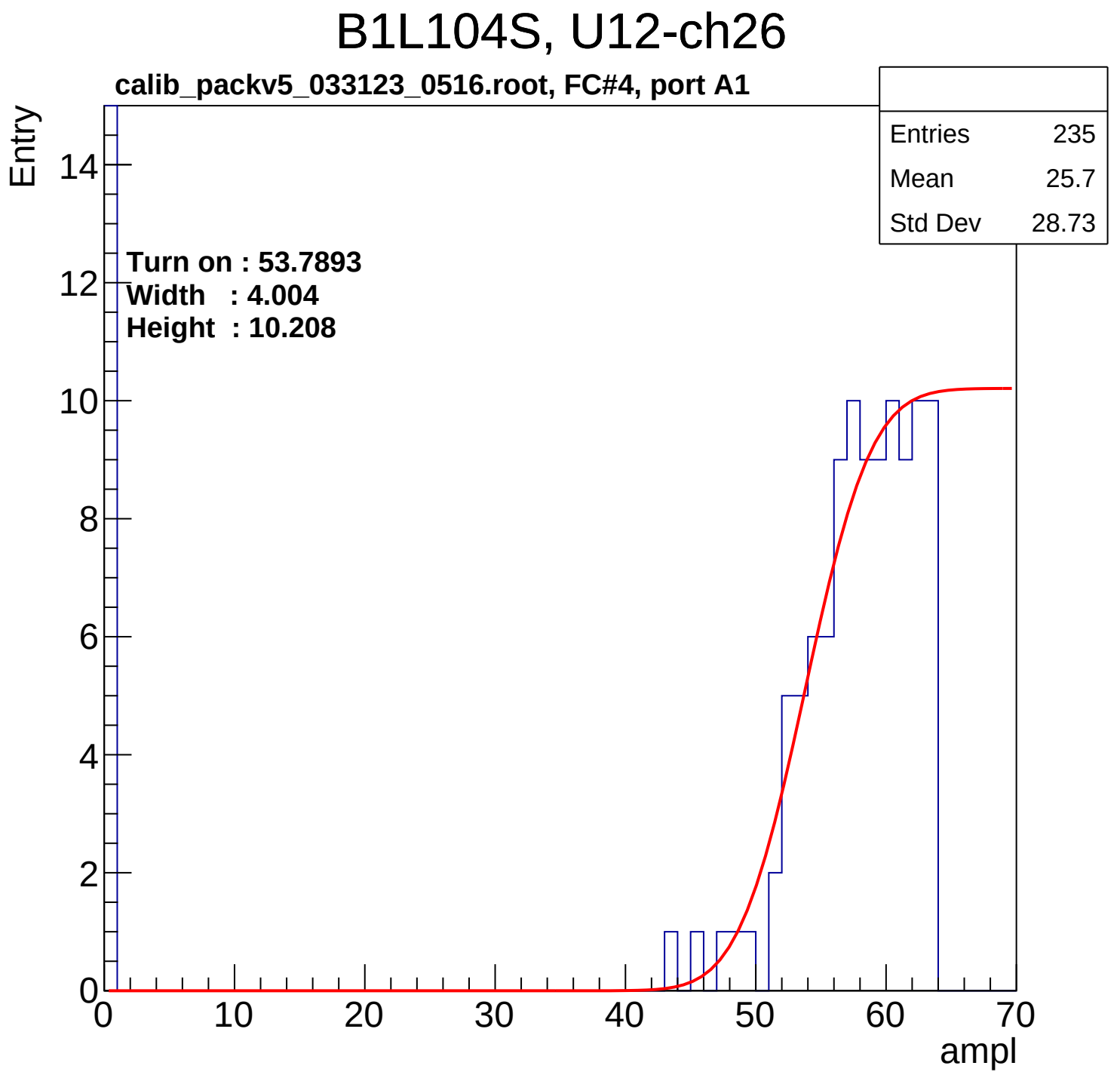
B1L104S, U12-ch26
calib_packv5_033123_0516.root, FC#4, port A1
Entries 235
Mean 25.7
Std Dev 28.73
Turn on : 53.7893
Width : 4.004
Height : 10.208
Entry
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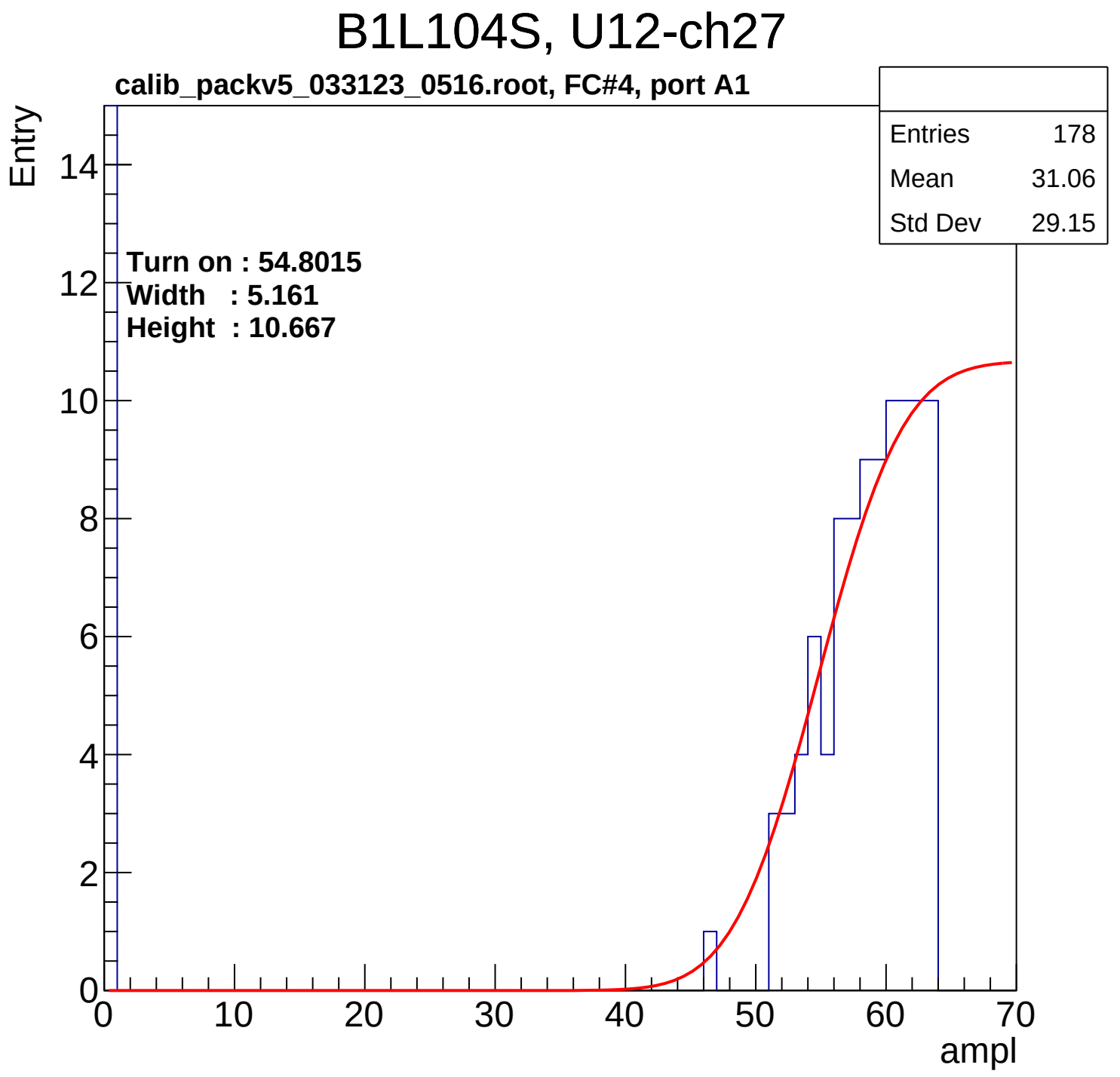
B1L104S, U12-ch27
calib_packv5_033123_0516.root, FC#4, port A1
Entries 178
Mean 31.06
Std Dev 29.15
Turn on : 54.8015
Width : 5.161
Height : 10.667
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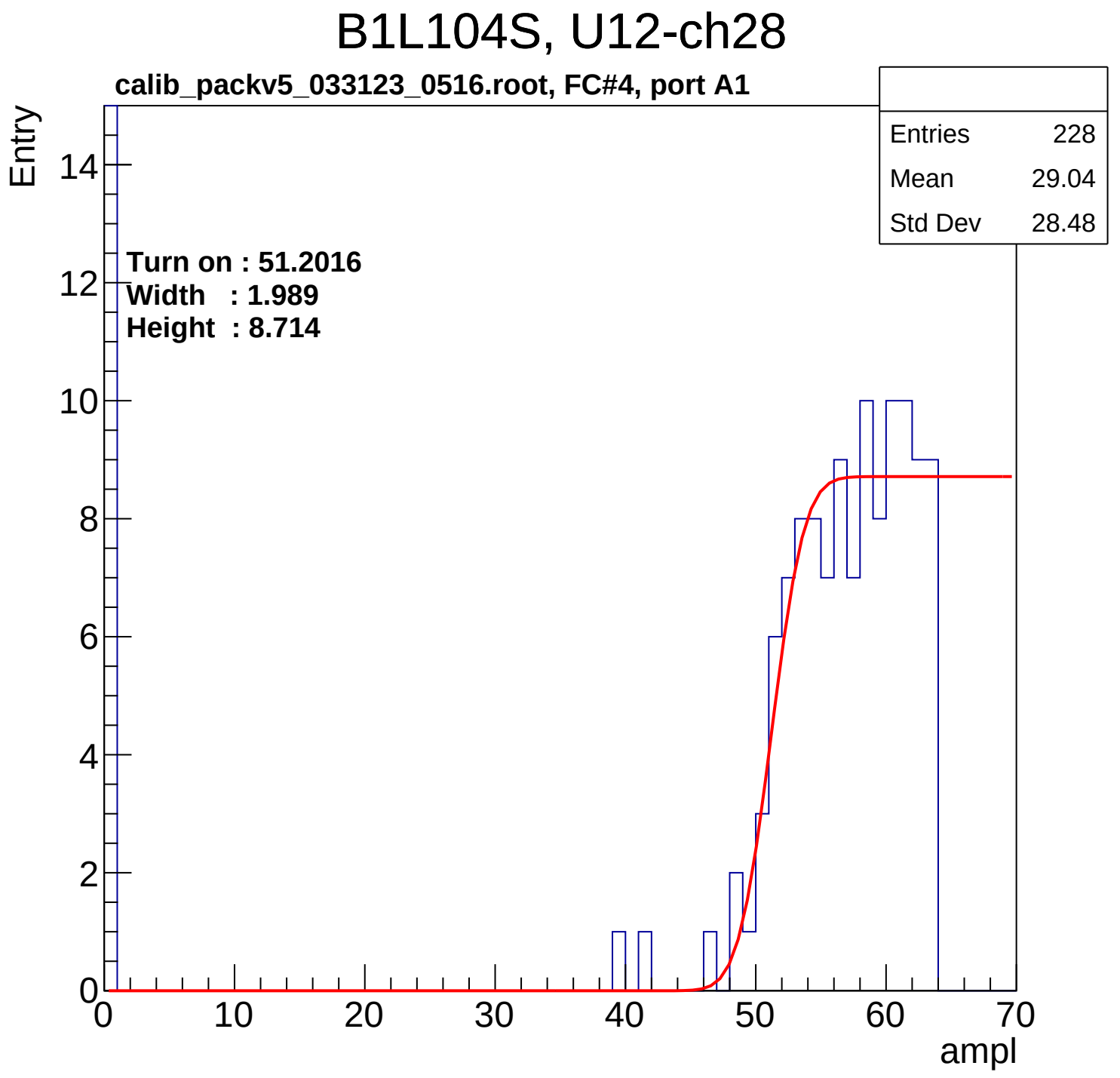
B1L104S, U12-ch28
calib_packv5_033123_0516.root, FC#4, port A1
Entries 228
Mean 29.04
Std Dev 28.48
Turn on : 51.2016
Width : 1.989
Height : 8.714
Entry
ampl
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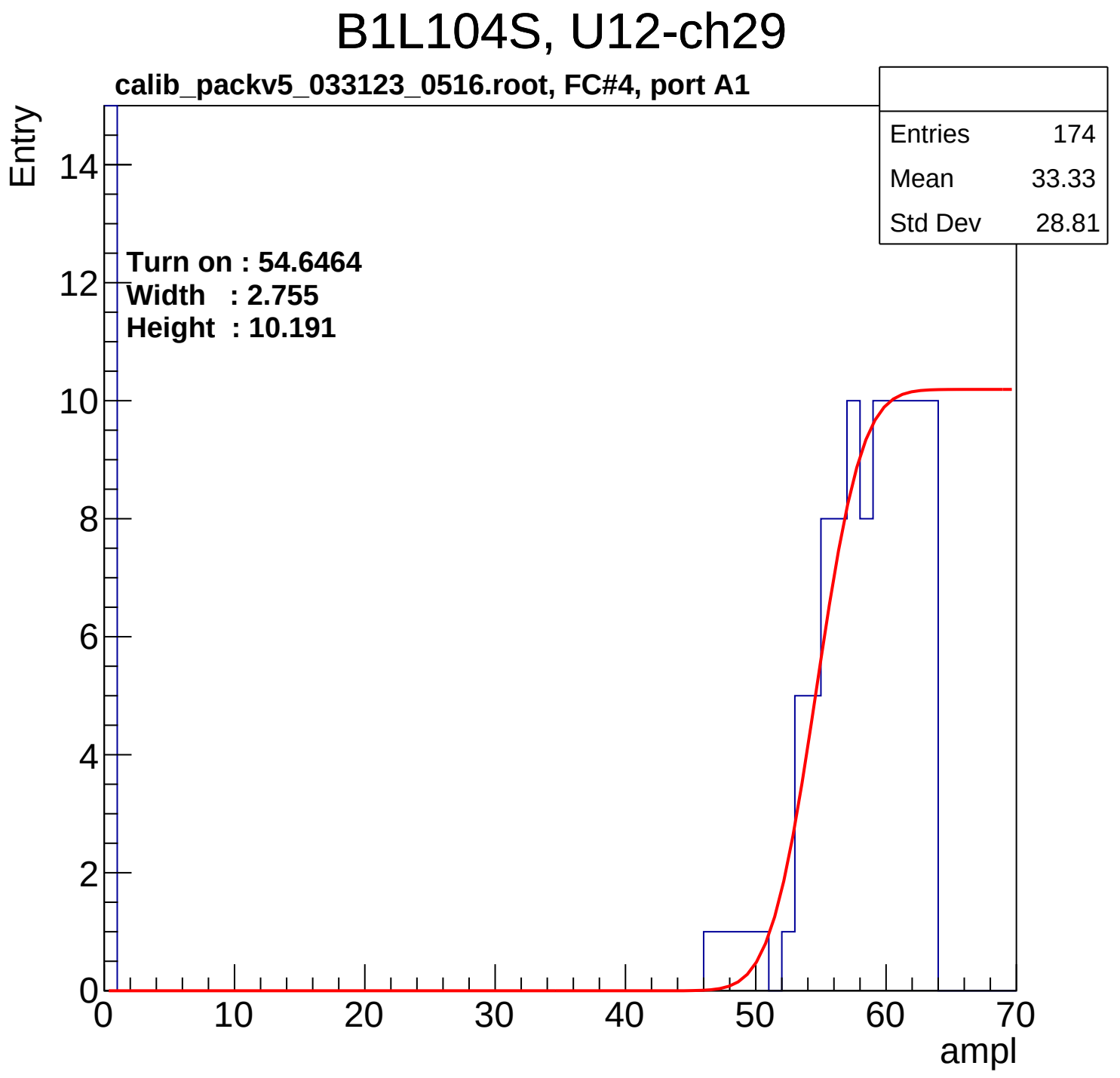
B1L104S, U12-ch29
calib_packv5_033123_0516.root, FC#4, port A1
Entries 174
Mean 33.33
Std Dev 28.81
Turn on : 54.6464
Width : 2.755
Height : 10.191
Entry
ampl
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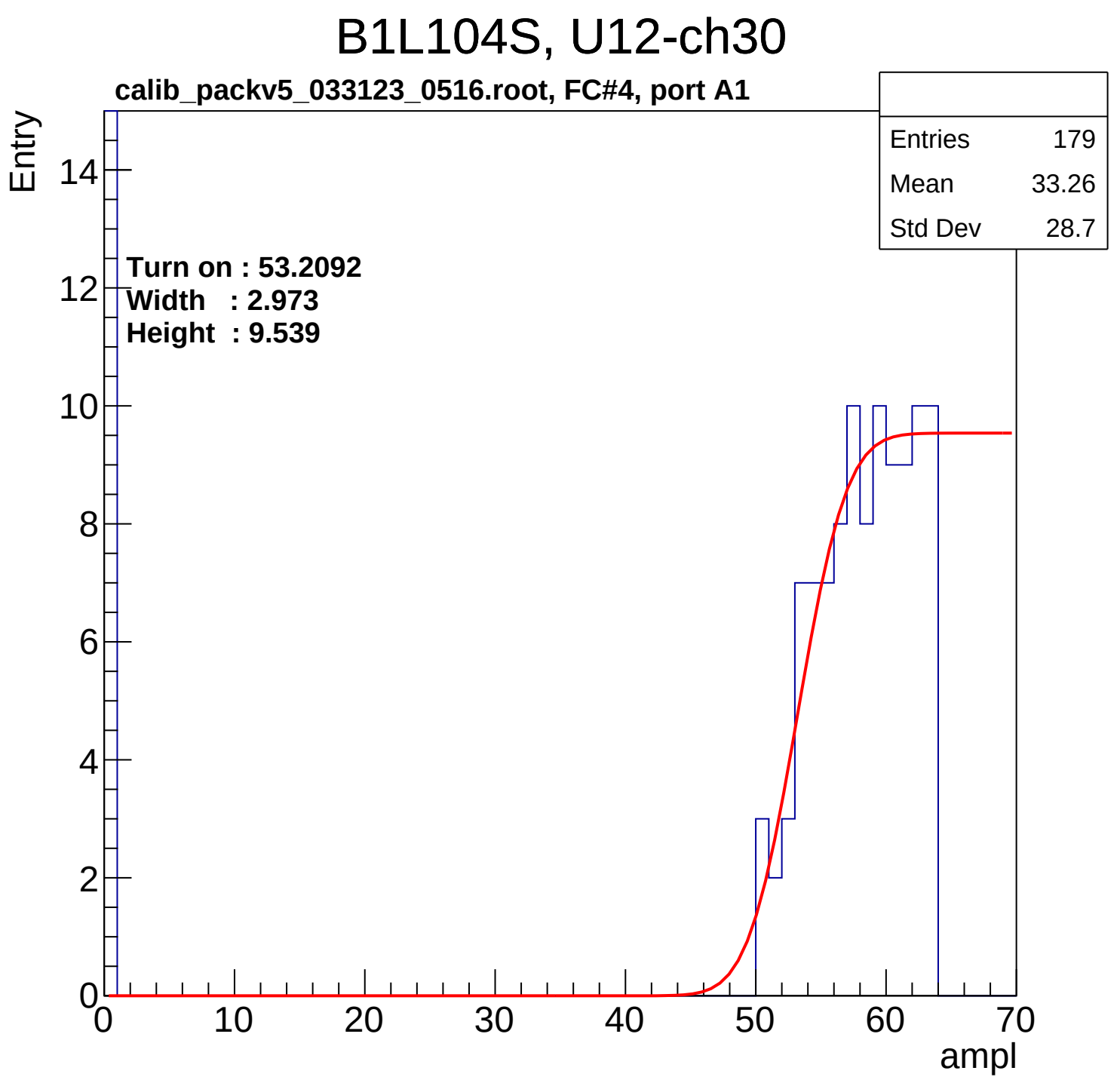
B1L104S, U12-ch30
calib_packv5_033123_0516.root, FC#4, port A1
Entries 179
Mean 33.26
Std Dev 28.7
Turn on : 53.2092
Width : 2.973
Height : 9.539
Entry
ampl
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2
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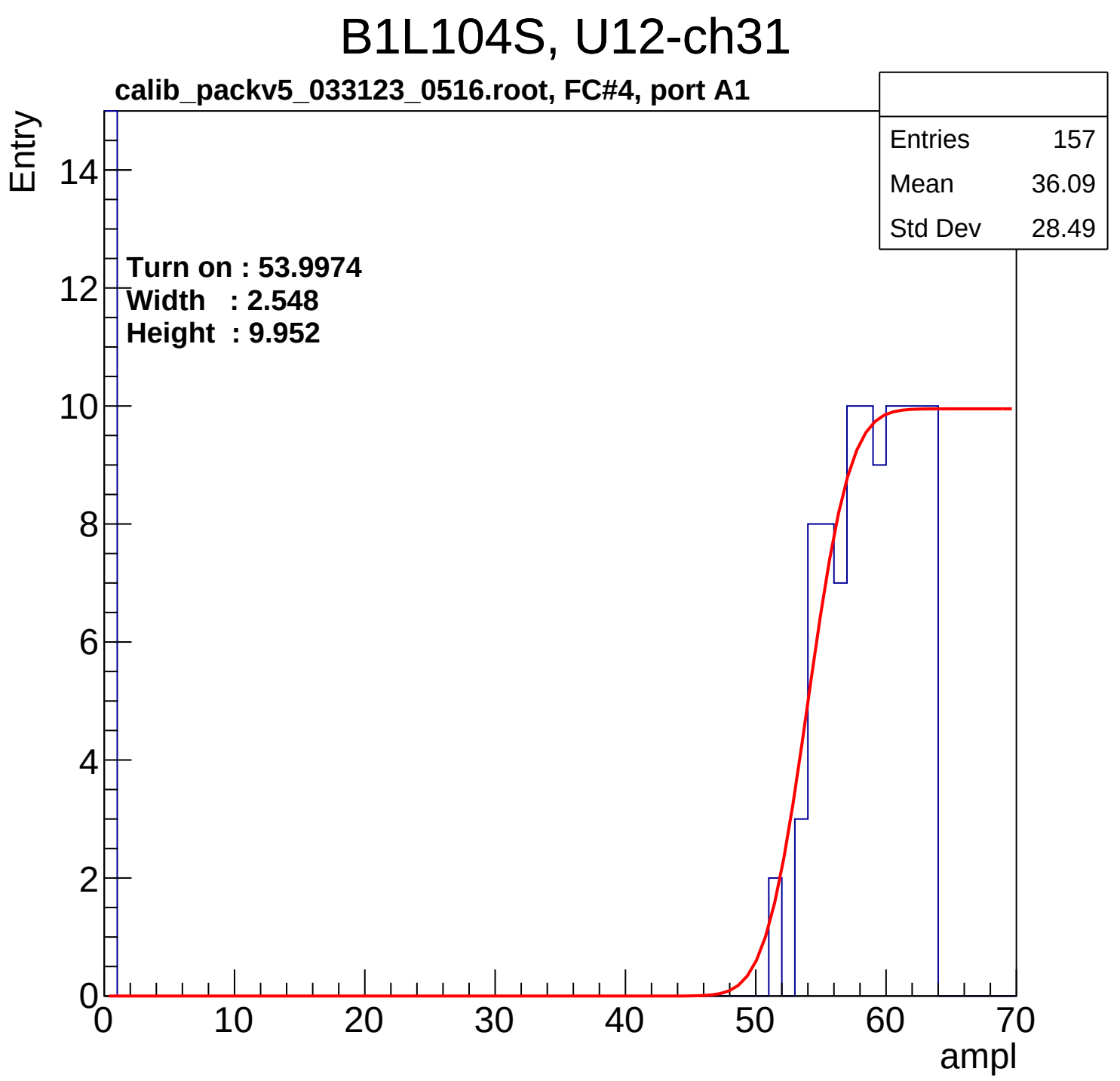
B1L104S, U12-ch31
calib_packv5_033123_0516.root, FC#4, port A1
Entries 157
Mean 36.09
Std Dev 28.49
Turn on : 53.9974
Width : 2.548
Height : 9.952
Entry
ampl
0
2
4
6
8
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12
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0
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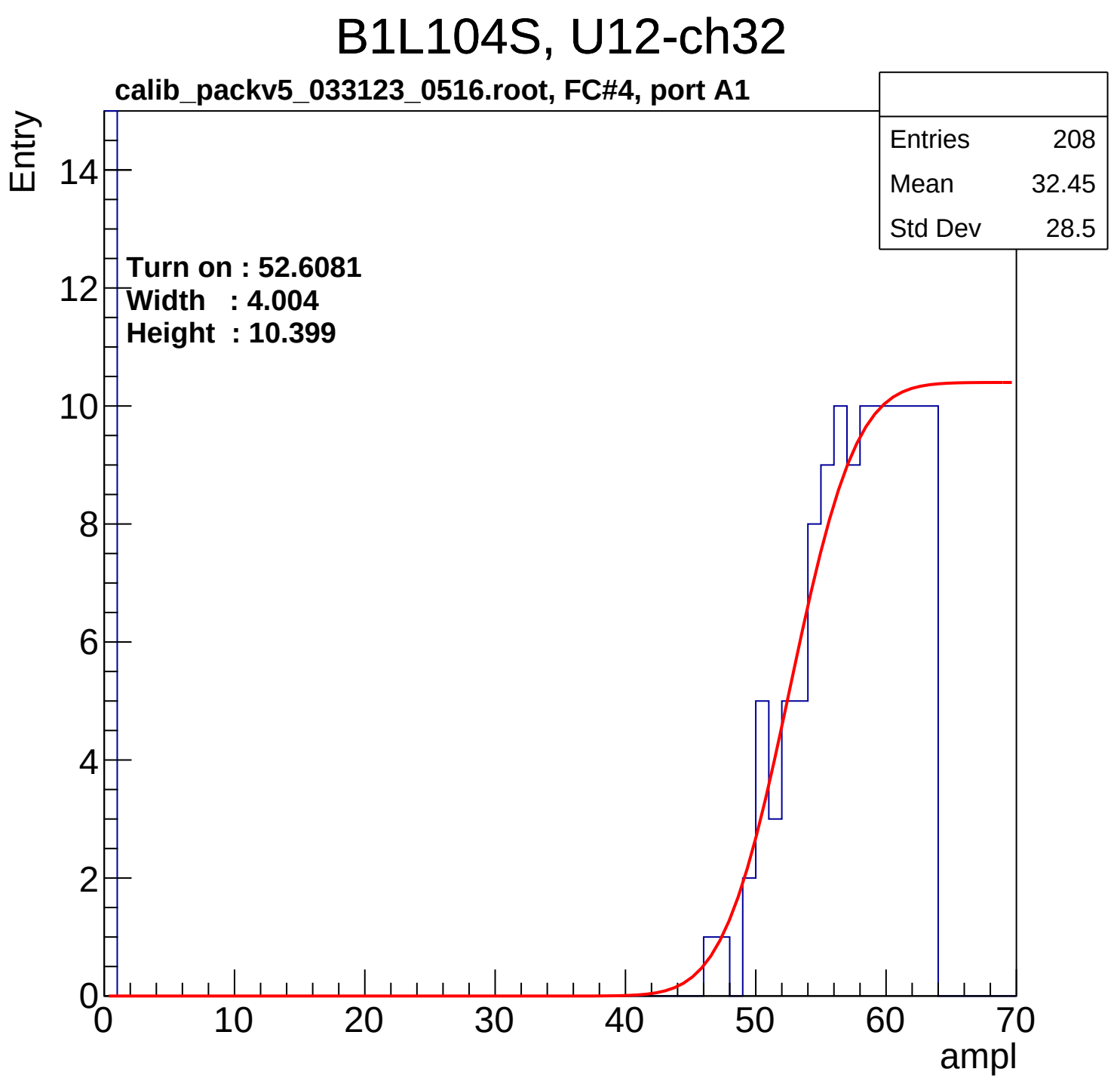
B1L104S, U12-ch32
calib_packv5_033123_0516.root, FC#4, port A1
Entries 208
Mean 32.45
Std Dev 28.5
Turn on : 52.6081
Width : 4.004
Height : 10.399
Entry
ampl
0
2
4
6
8
10
12
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0
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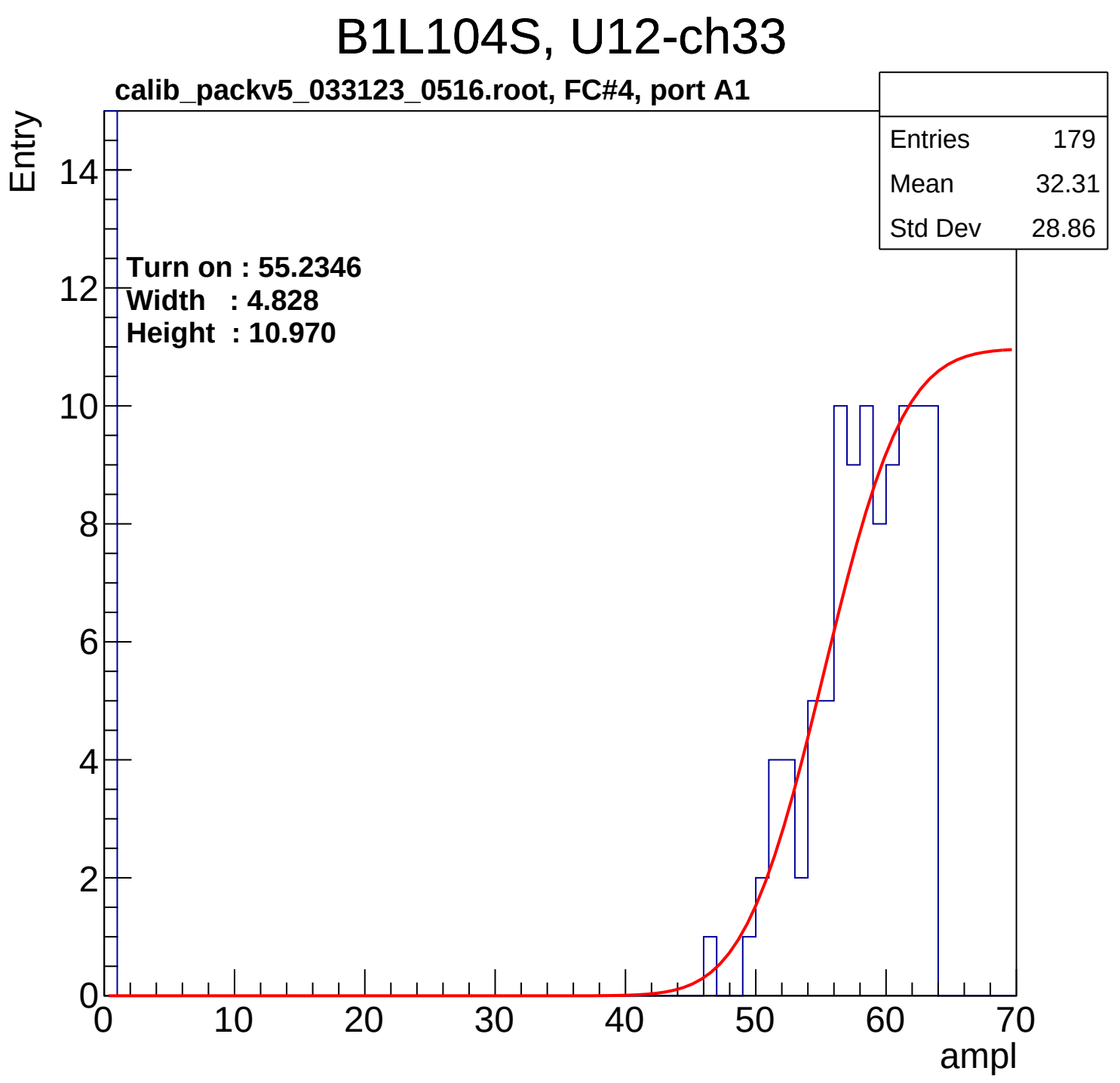
B1L104S, U12-ch33
calib_packv5_033123_0516.root, FC#4, port A1
Entries 179
Mean 32.31
Std Dev 28.86
Turn on : 55.2346
Width : 4.828
Height : 10.970
Entry
ampl
0
2
4
6
8
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0
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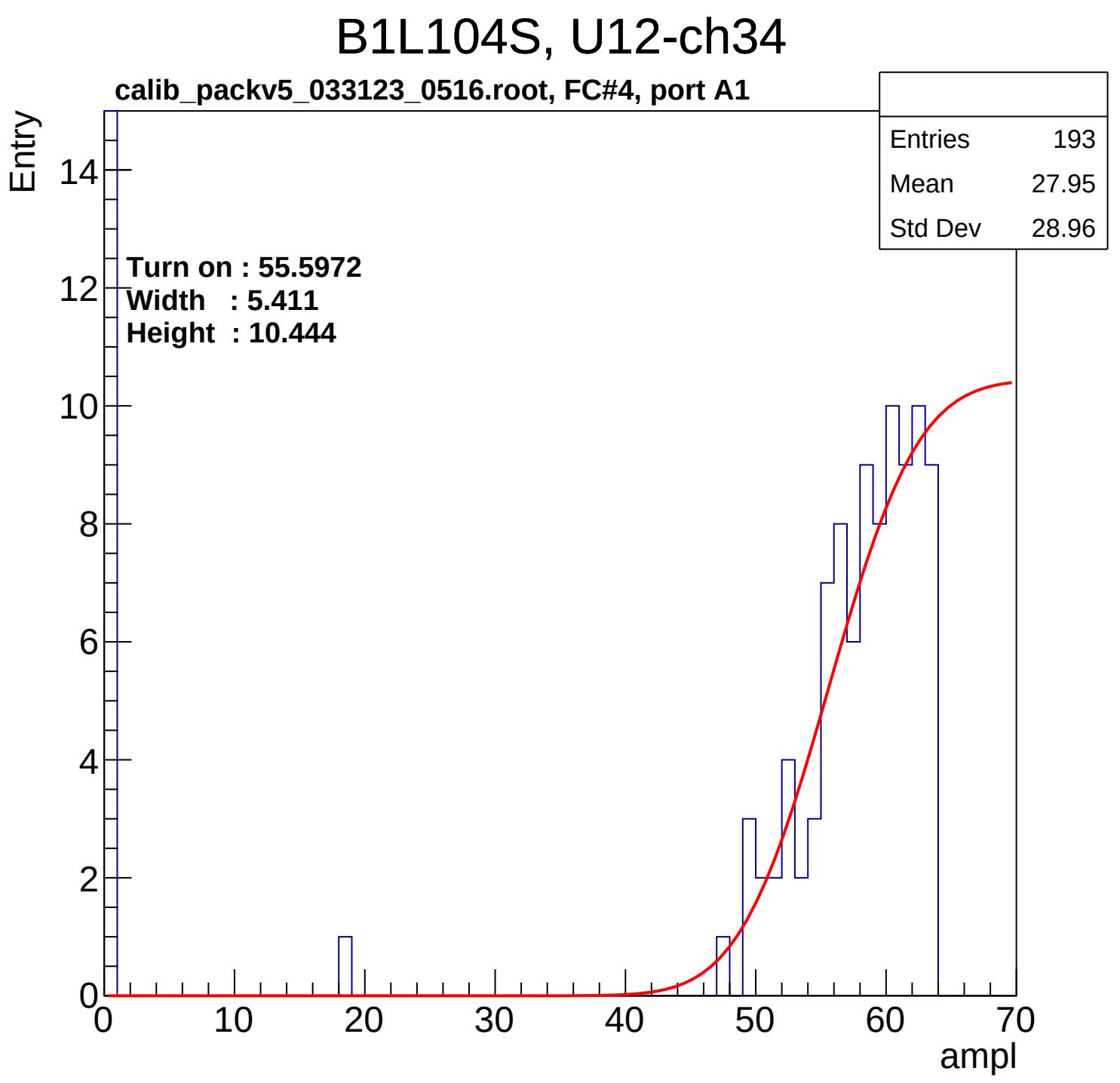
B1L104S, U12-ch34
calib_packv5_033123_0516.root, FC#4, port A1
Entries 193
Mean 27.95
Std Dev 28.96
Turn on : 55.5972
Width : 5.411
Height : 10.444
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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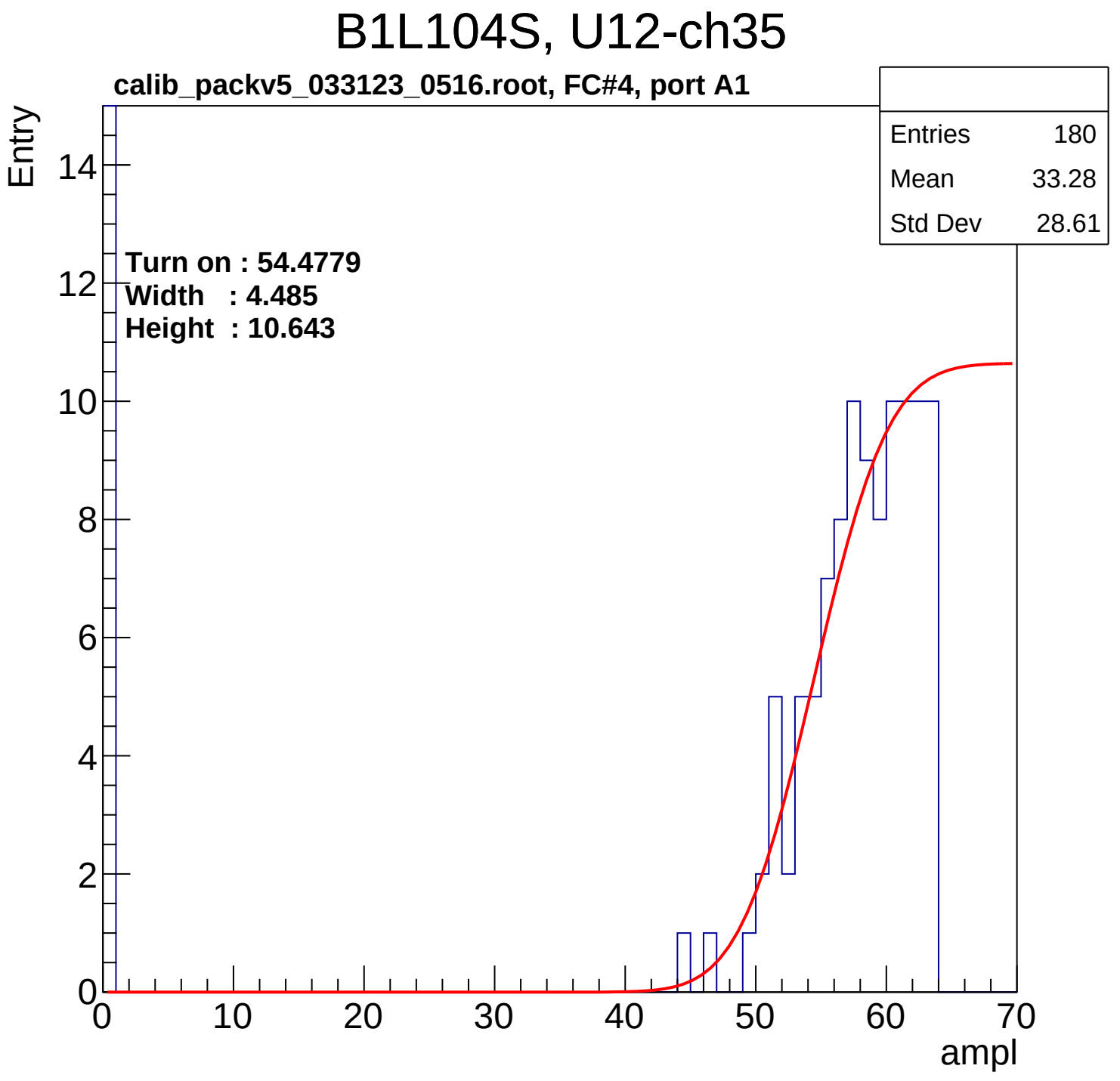
B1L104S, U12-ch35
calib_packv5_033123_0516.root, FC#4, port A1
Entries 180
Mean 33.28
Std Dev 28.61
Turn on : 54.4779
Width : 4.485
Height : 10.643
Entry
ampl
0
2
4
6
8
10
12
14
0
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60
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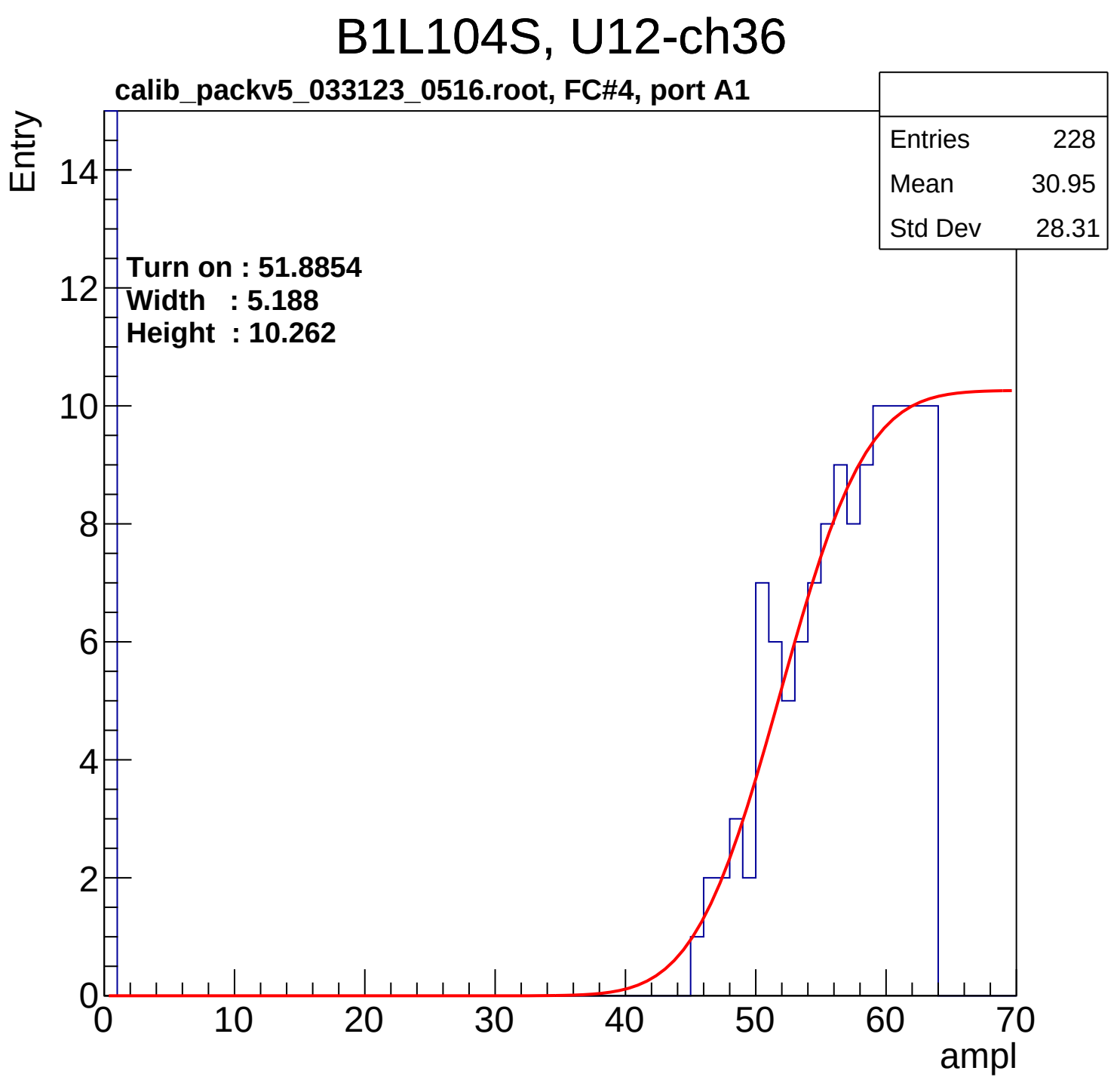
B1L104S, U12-ch36
calib_packv5_033123_0516.root, FC#4, port A1
Entries 228
Mean 30.95
Std Dev 28.31
Turn on : 51.8854
Width : 5.188
Height : 10.262
Entry
ampl
0
2
4
6
8
10
12
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0
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40
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60
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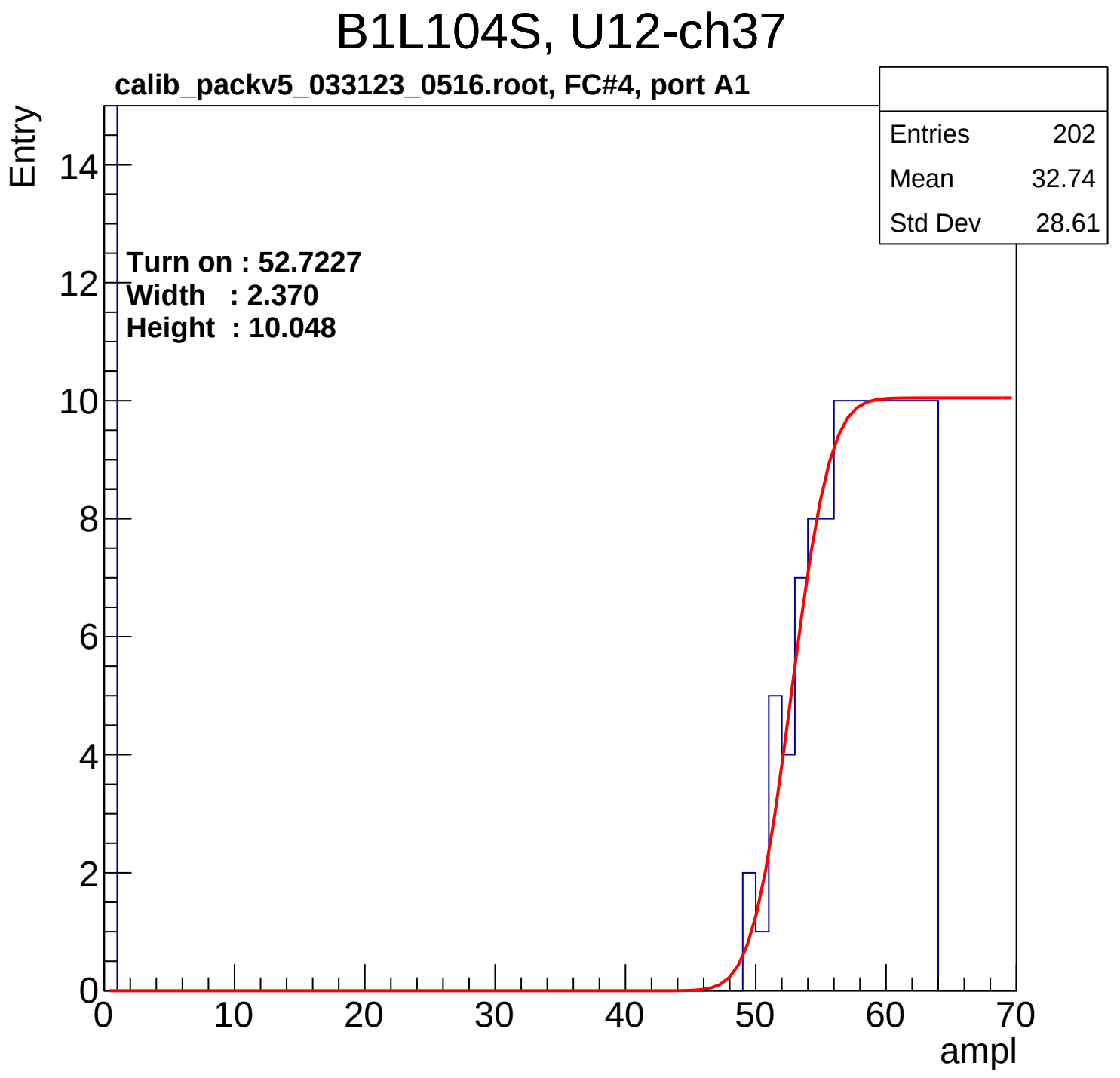
B1L104S, U12-ch37
calib_packv5_033123_0516.root, FC#4, port A1
Entries 202
Mean 32.74
Std Dev 28.61
Turn on : 52.7227
Width : 2.370
Height : 10.048
Entry
ampl
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6
8
10
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60
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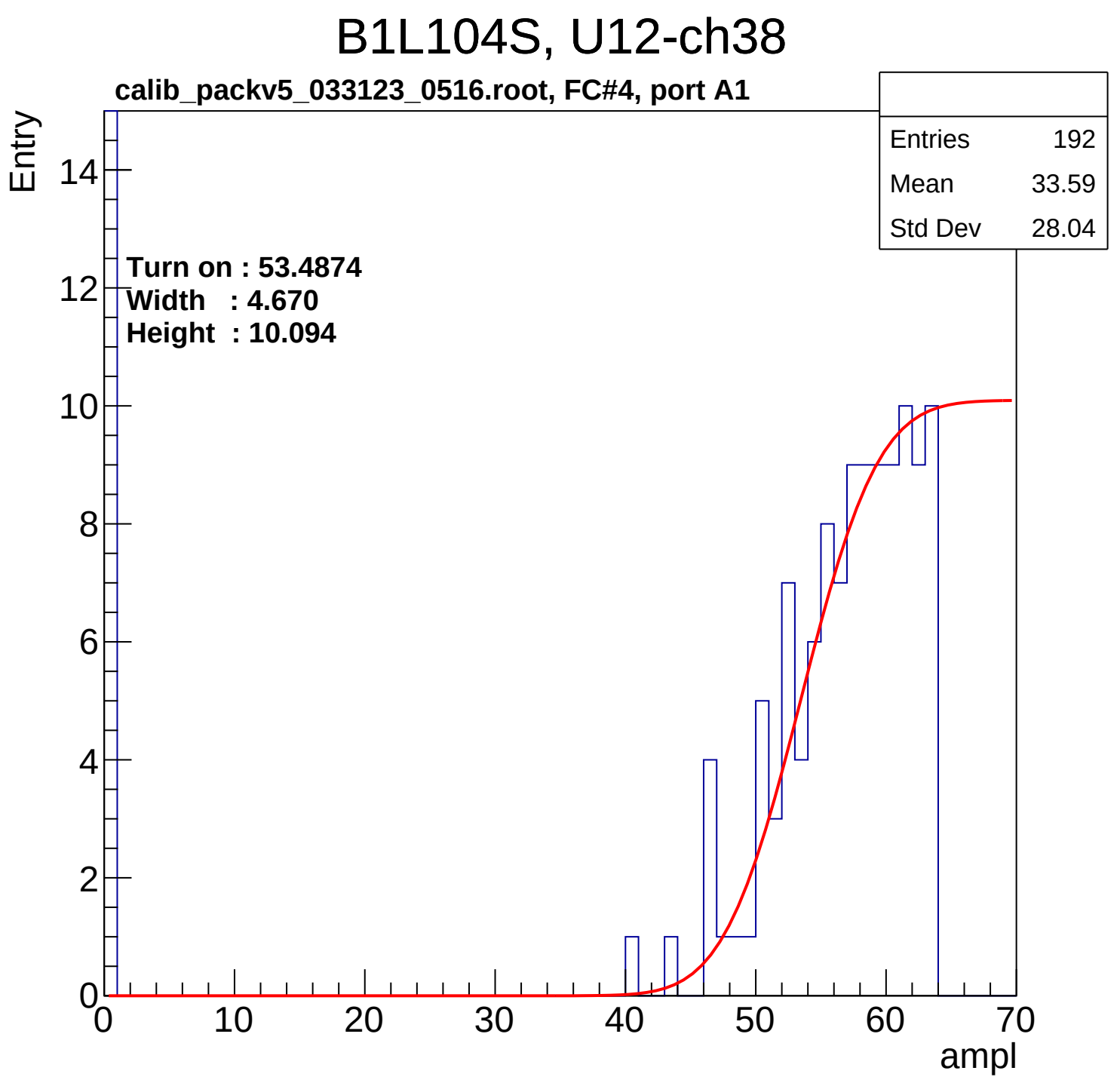
B1L104S, U12-ch38
calib_packv5_033123_0516.root, FC#4, port A1
Entries 192
Mean 33.59
Std Dev 28.04
Turn on : 53.4874
Width : 4.670
Height : 10.094
Entry
ampl
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2
4
6
8
10
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60
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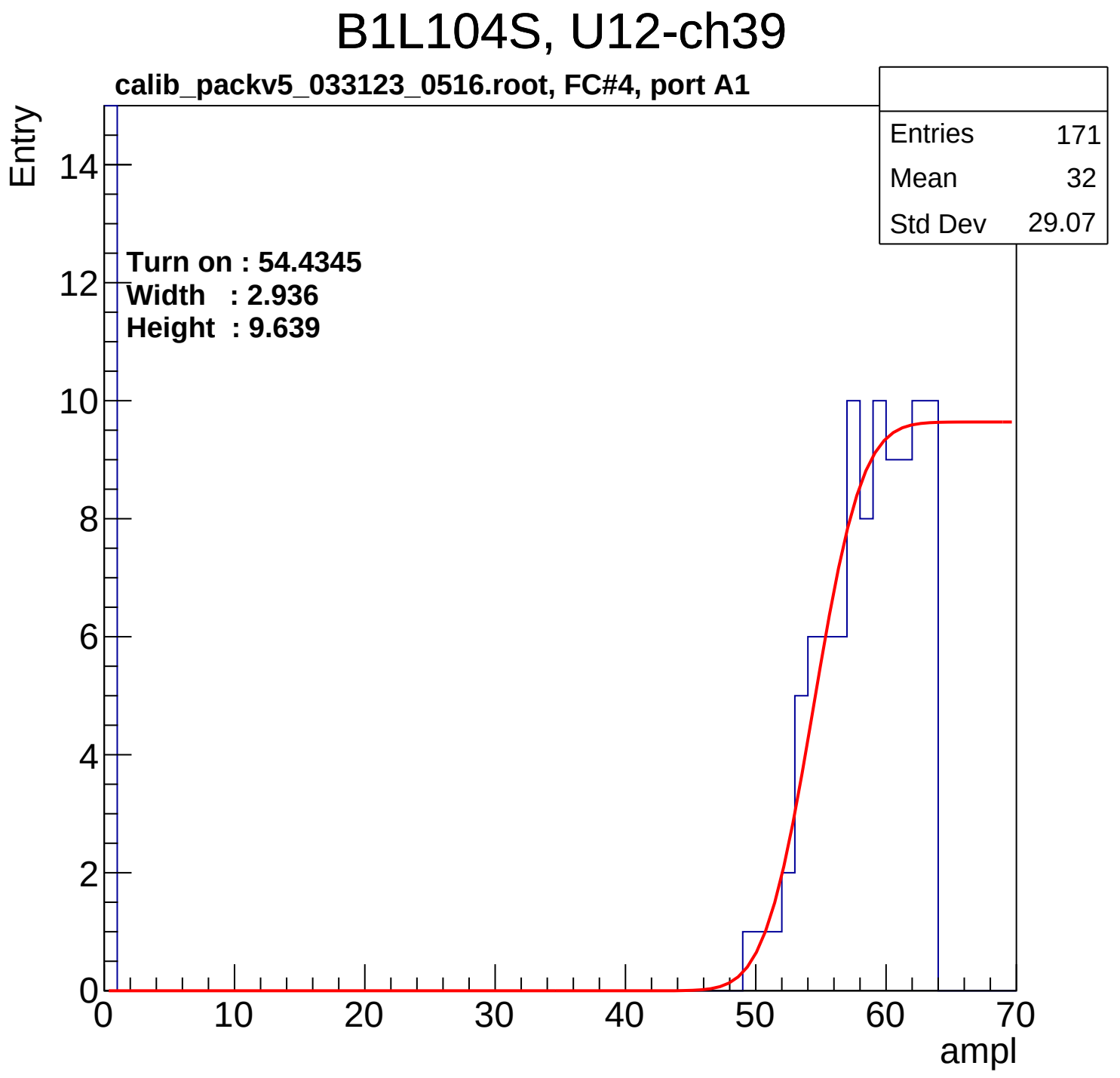
B1L104S, U12-ch39
calib_packv5_033123_0516.root, FC#4, port A1
Entries 171
Mean 32
Std Dev 29.07
Turn on : 54.4345
Width : 2.936
Height : 9.639
Entry
ampl
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6
8
10
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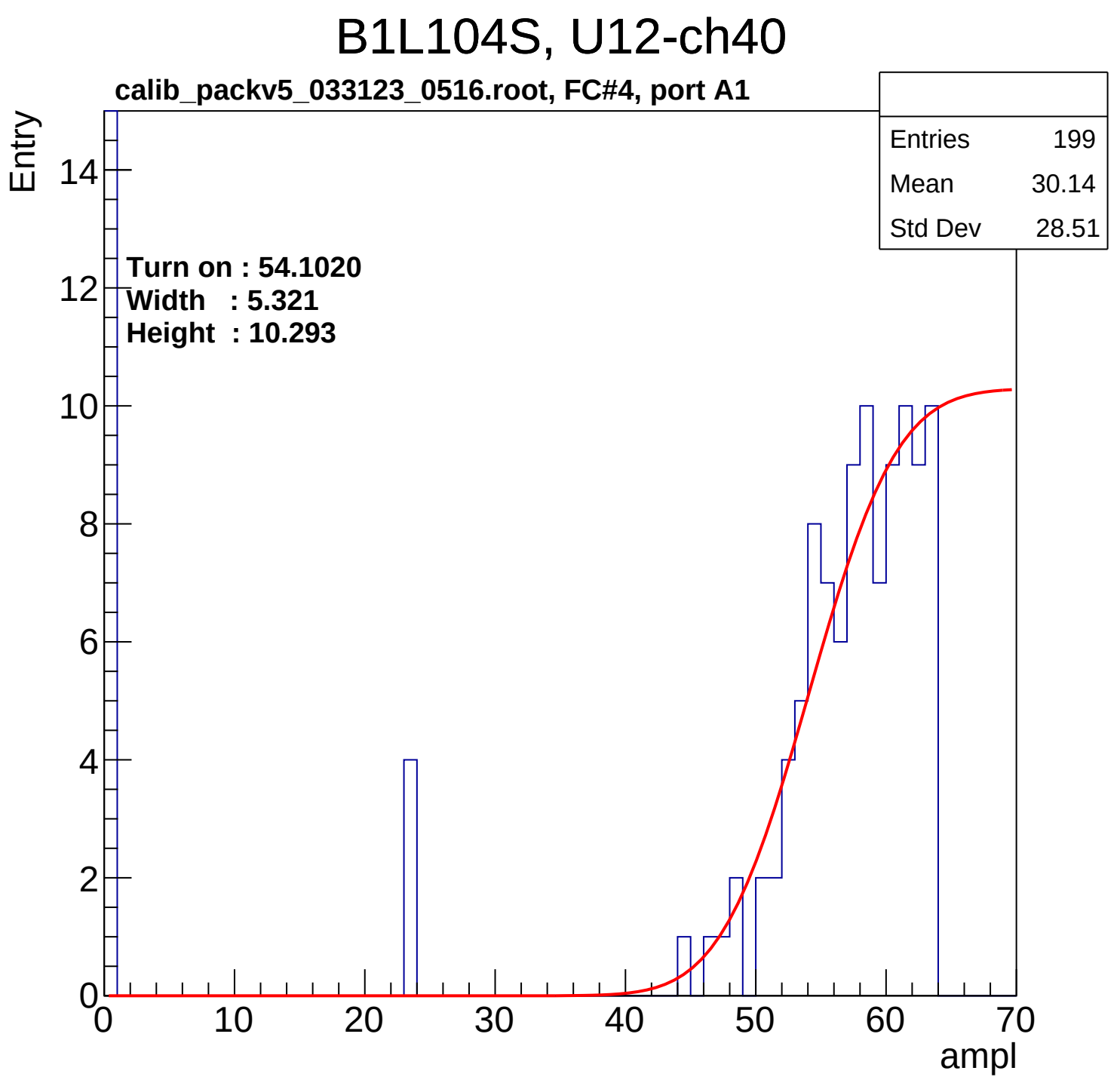
B1L104S, U12-ch40
calib_packv5_033123_0516.root, FC#4, port A1
Entries 199
Mean 30.14
Std Dev 28.51
Turn on : 54.1020
Width : 5.321
Height : 10.293
Entry
ampl
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4
6
8
10
12
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0
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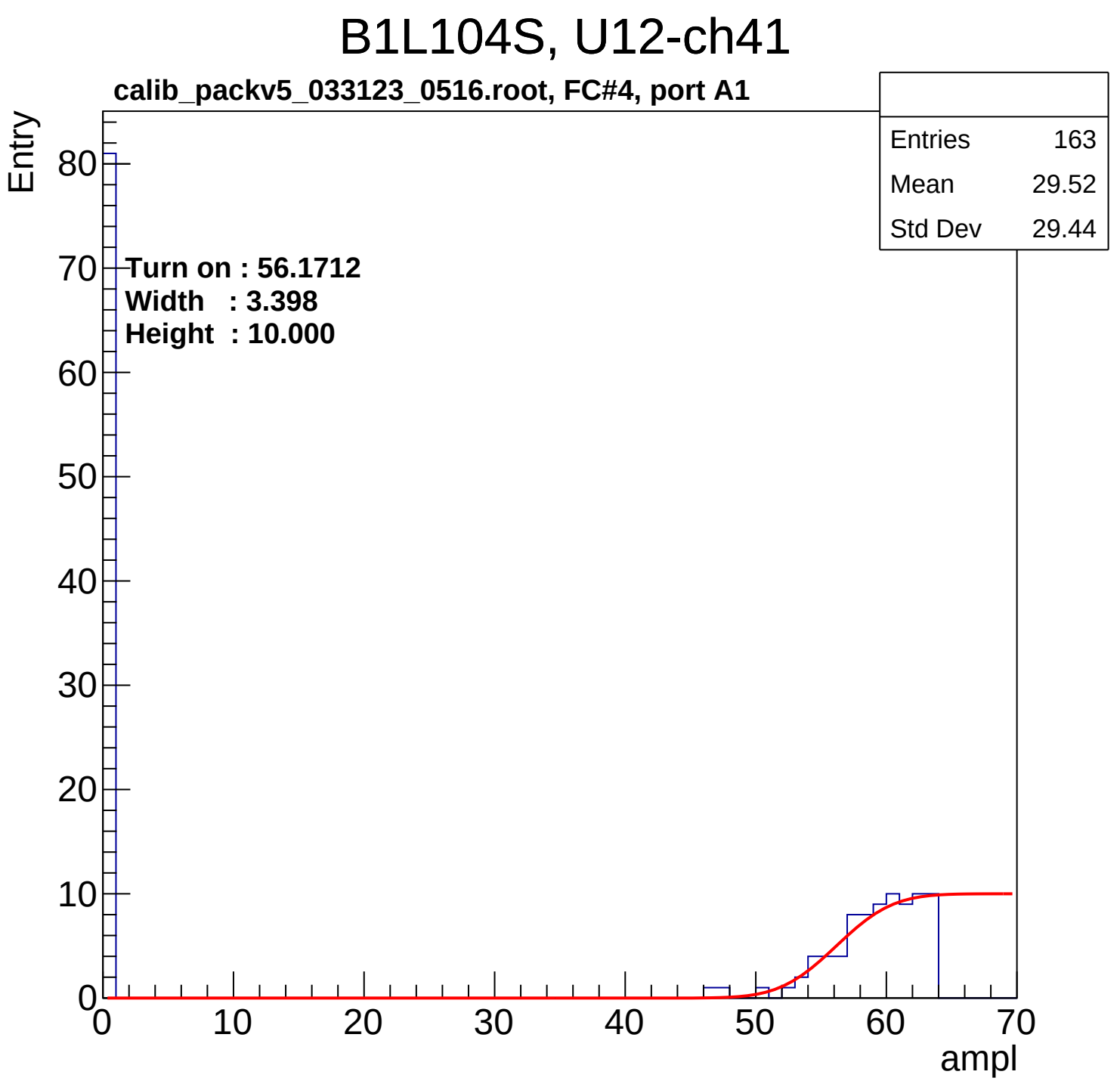
B1L104S, U12-ch41
calib_packv5_033123_0516.root, FC#4, port A1
Entries 163
Mean 29.52
Std Dev 29.44
Turn on : 56.1712
Width : 3.398
Height : 10.000
Entry
ampl
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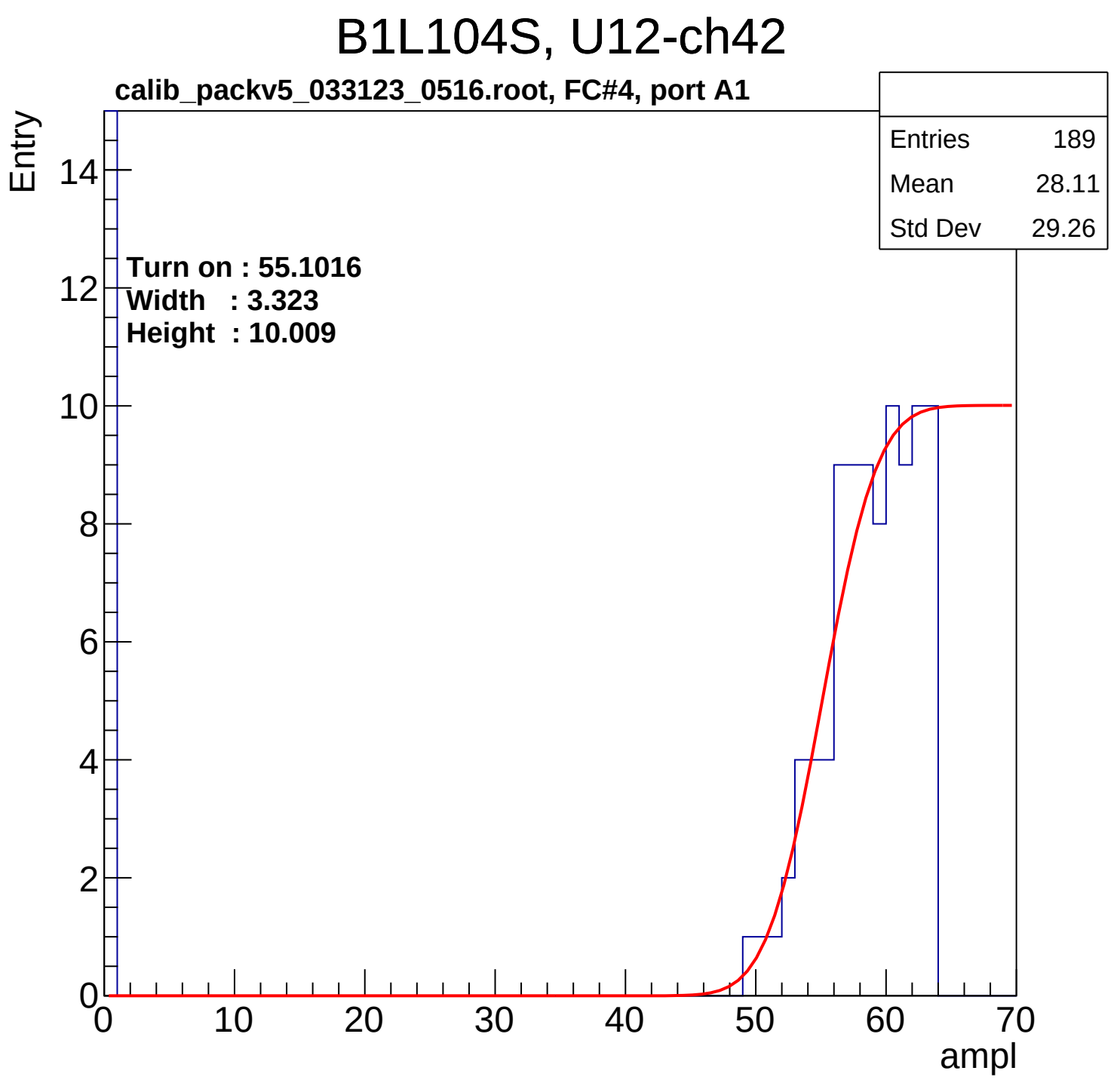
B1L104S, U12-ch42
calib_packv5_033123_0516.root, FC#4, port A1
Entries 189
Mean 28.11
Std Dev 29.26
Turn on : 55.1016
Width : 3.323
Height : 10.009
Entry
ampl
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6
8
10
12
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0
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60
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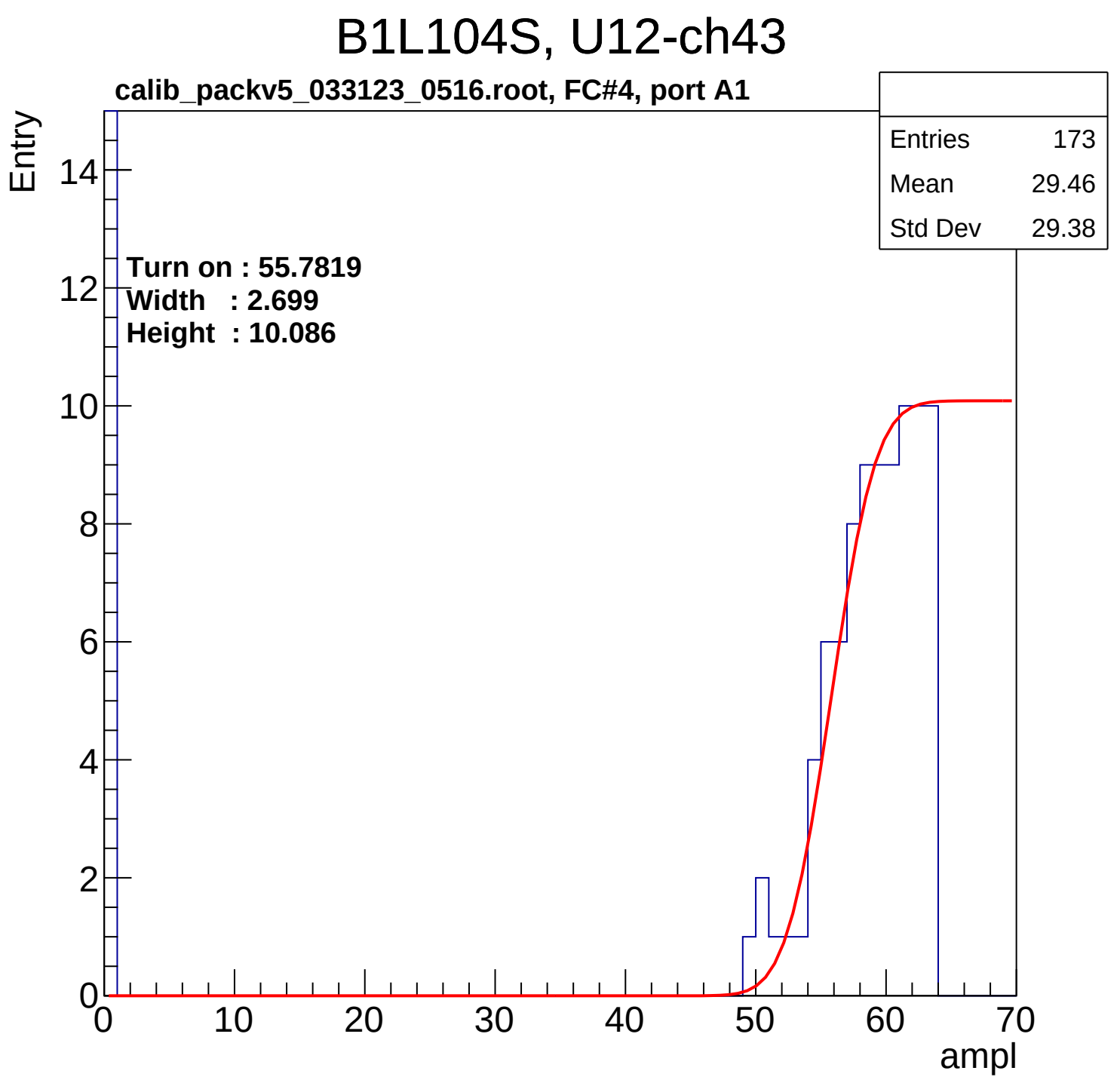
B1L104S, U12-ch43
calib_packv5_033123_0516.root, FC#4, port A1
Entries 173
Mean 29.46
Std Dev 29.38
Turn on : 55.7819
Width : 2.699
Height : 10.086
Entry
ampl
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6
8
10
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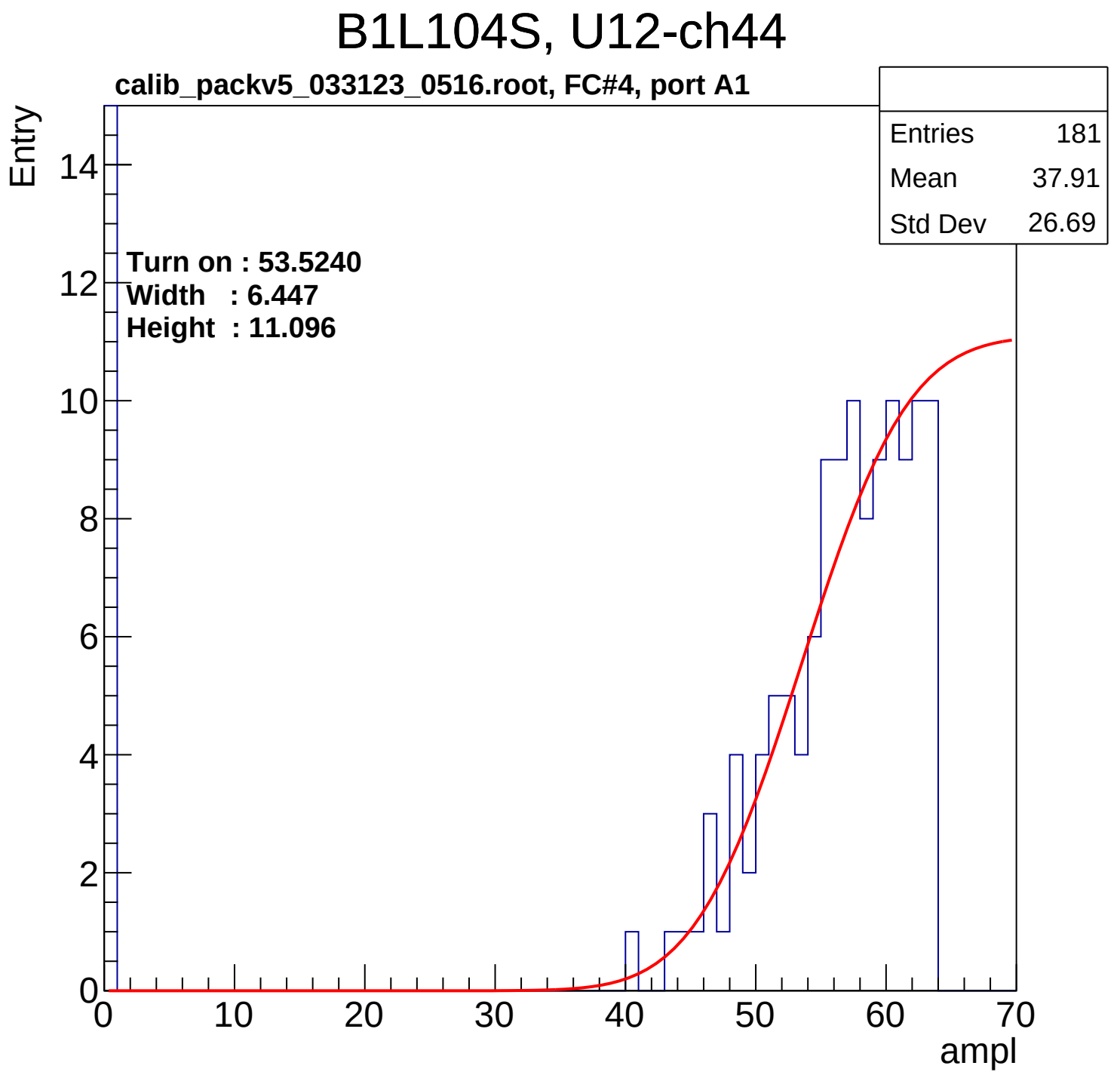
B1L104S, U12-ch44
calib_packv5_033123_0516.root, FC#4, port A1
Entries 181
Mean 37.91
Std Dev 26.69
Turn on : 53.5240
Width : 6.447
Height : 11.096
Entry
ampl
0
2
4
6
8
10
12
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0
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20
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60
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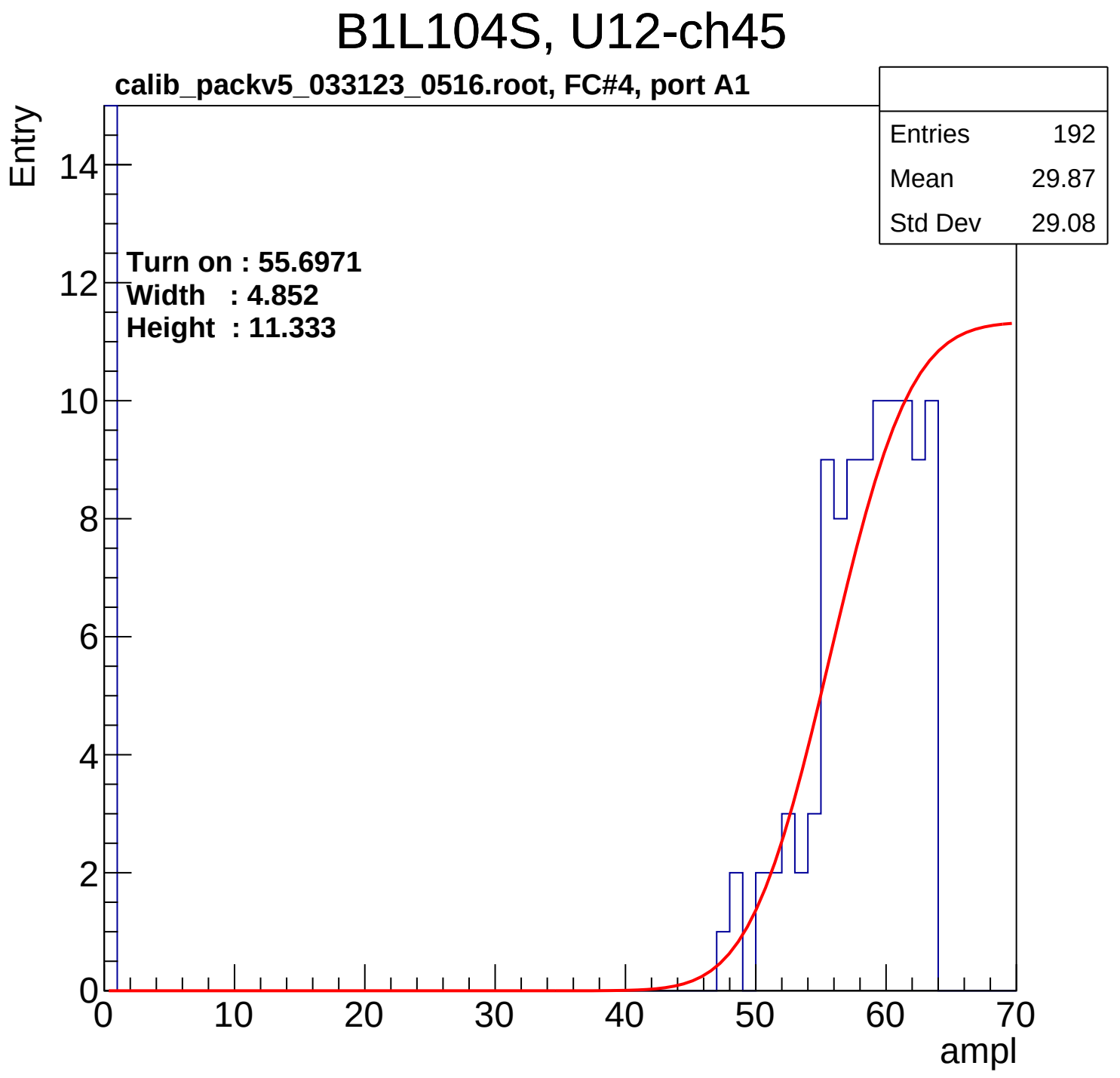
B1L104S, U12-ch45
calib_packv5_033123_0516.root, FC#4, port A1
Entries 192
Mean 29.87
Std Dev 29.08
Turn on : 55.6971
Width : 4.852
Height : 11.333
Entry
ampl
0
2
4
6
8
10
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0
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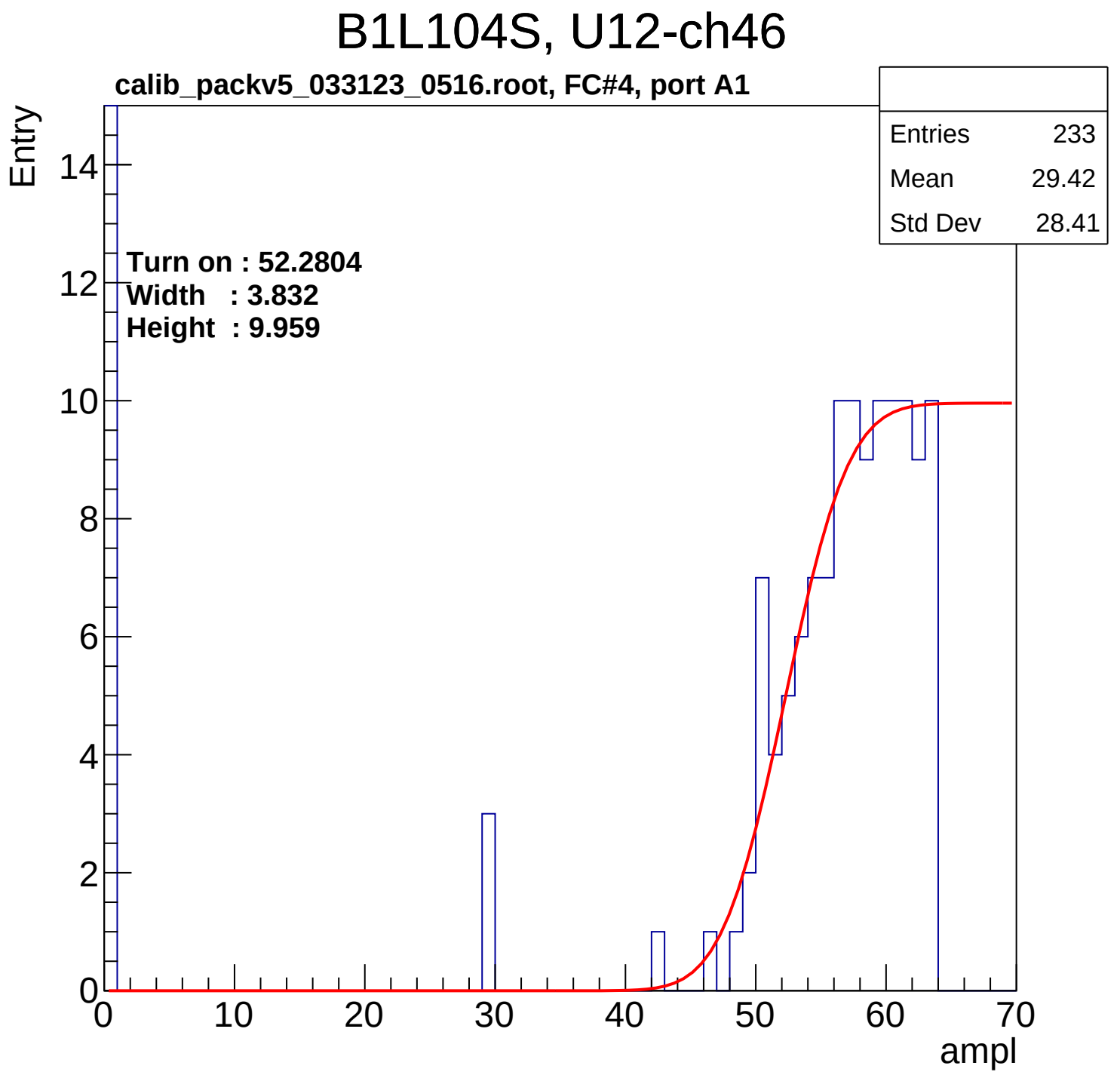
B1L104S, U12-ch46
calib_packv5_033123_0516.root, FC#4, port A1
Entries 233
Mean 29.42
Std Dev 28.41
Turn on : 52.2804
Width : 3.832
Height : 9.959
Entry
ampl
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0
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20
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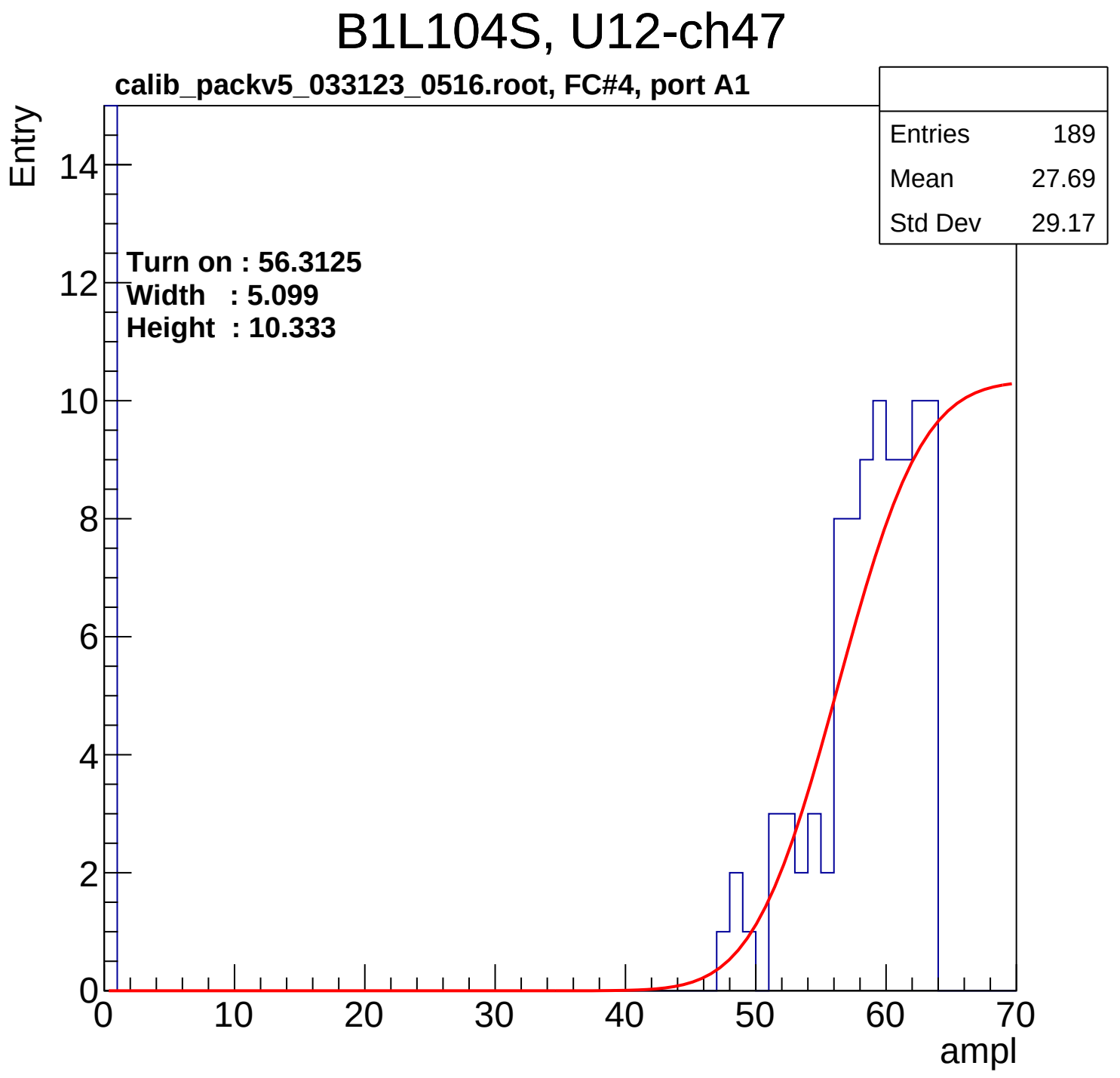
B1L104S, U12-ch47
calib_packv5_033123_0516.root, FC#4, port A1
Entries 189
Mean 27.69
Std Dev 29.17
Turn on : 56.3125
Width : 5.099
Height : 10.333
Entry
ampl
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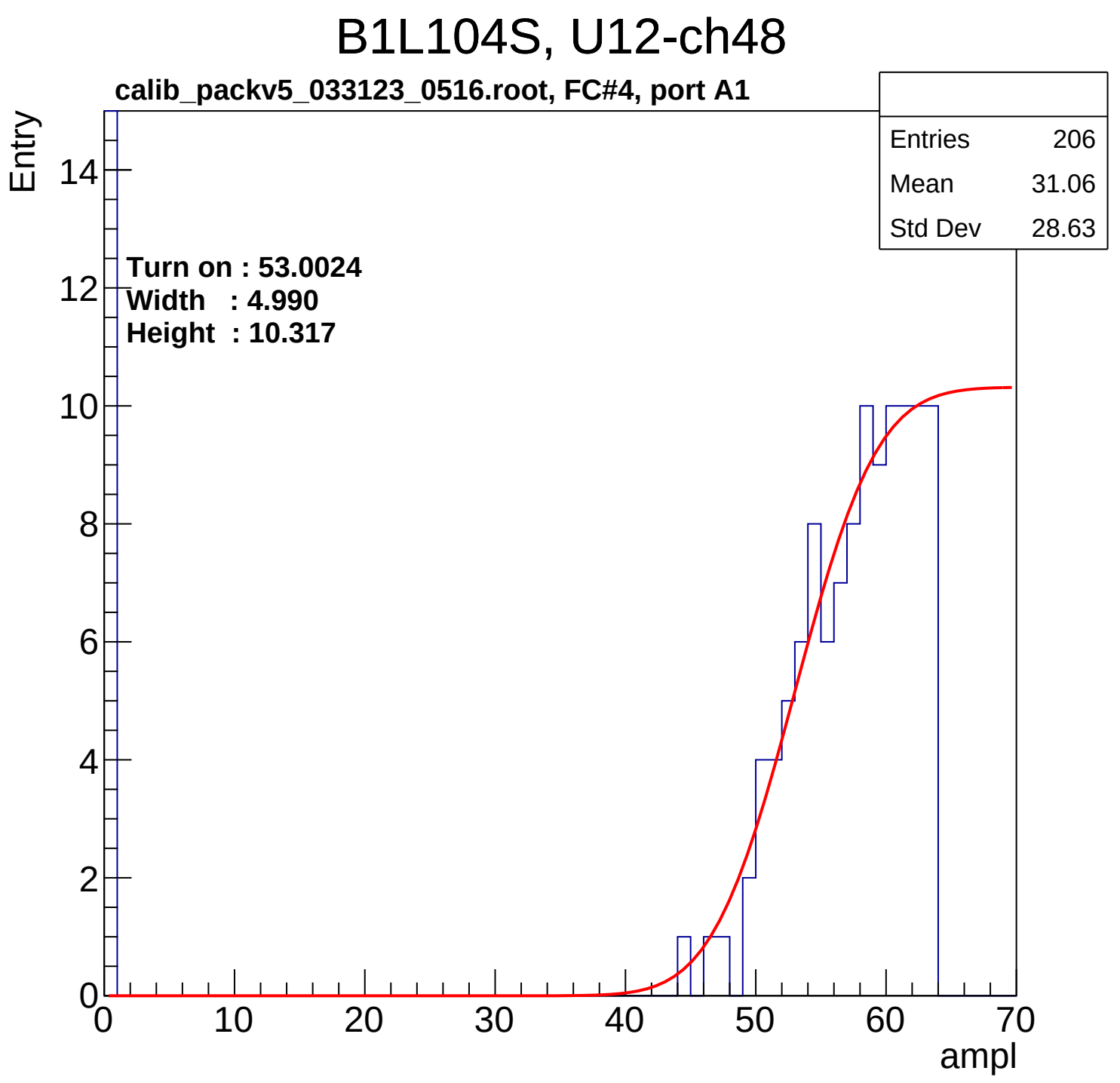
B1L104S, U12-ch48
calib_packv5_033123_0516.root, FC#4, port A1
Entries 206
Mean 31.06
Std Dev 28.63
Turn on : 53.0024
Width : 4.990
Height : 10.317
Entry
ampl
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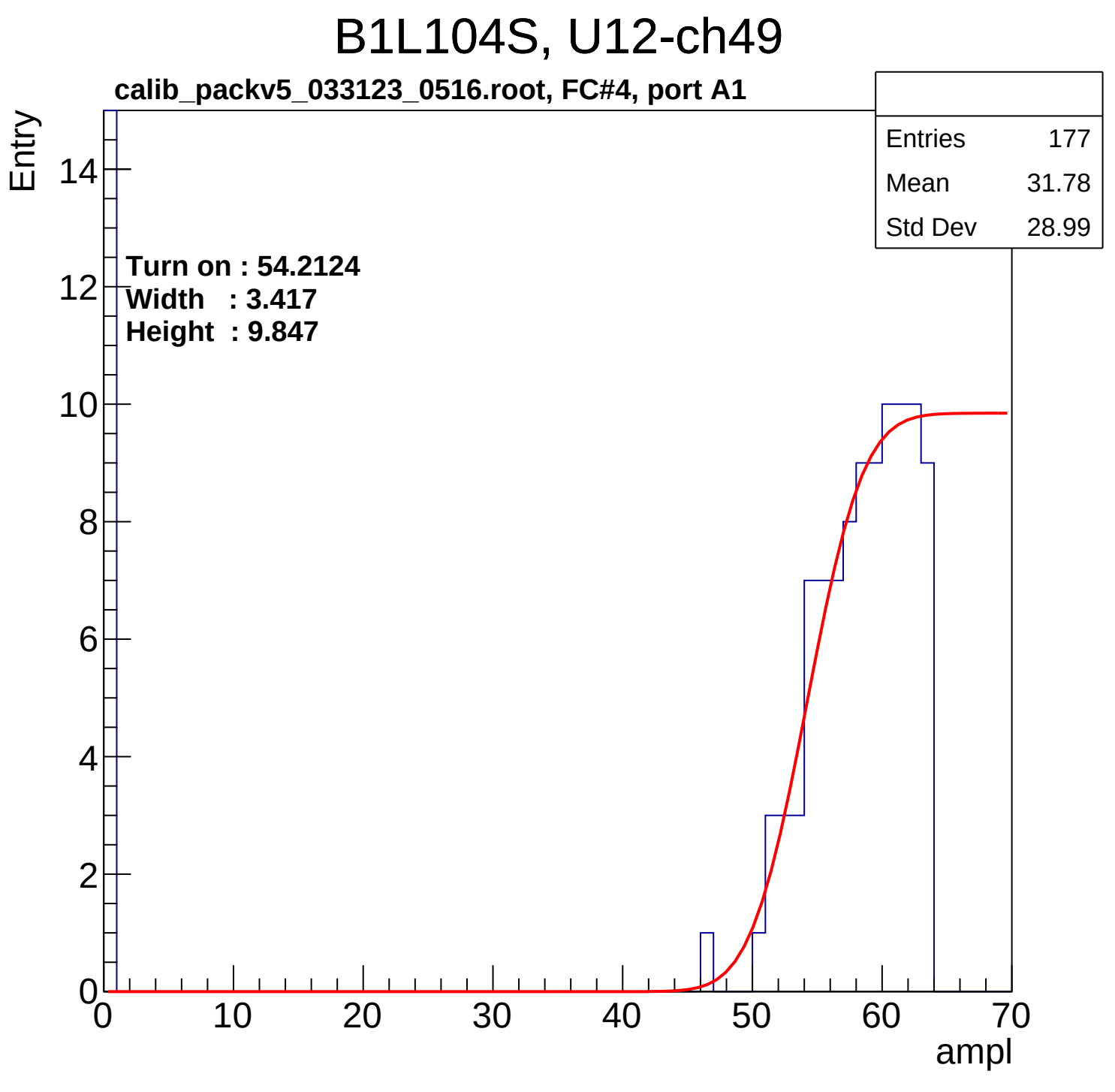
B1L104S, U12-ch49
calib_packv5_033123_0516.root, FC#4, port A1
Entries 177
Mean 31.78
Std Dev 28.99
Turn on : 54.2124
Width : 3.417
Height : 9.847
Entry
ampl
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6
8
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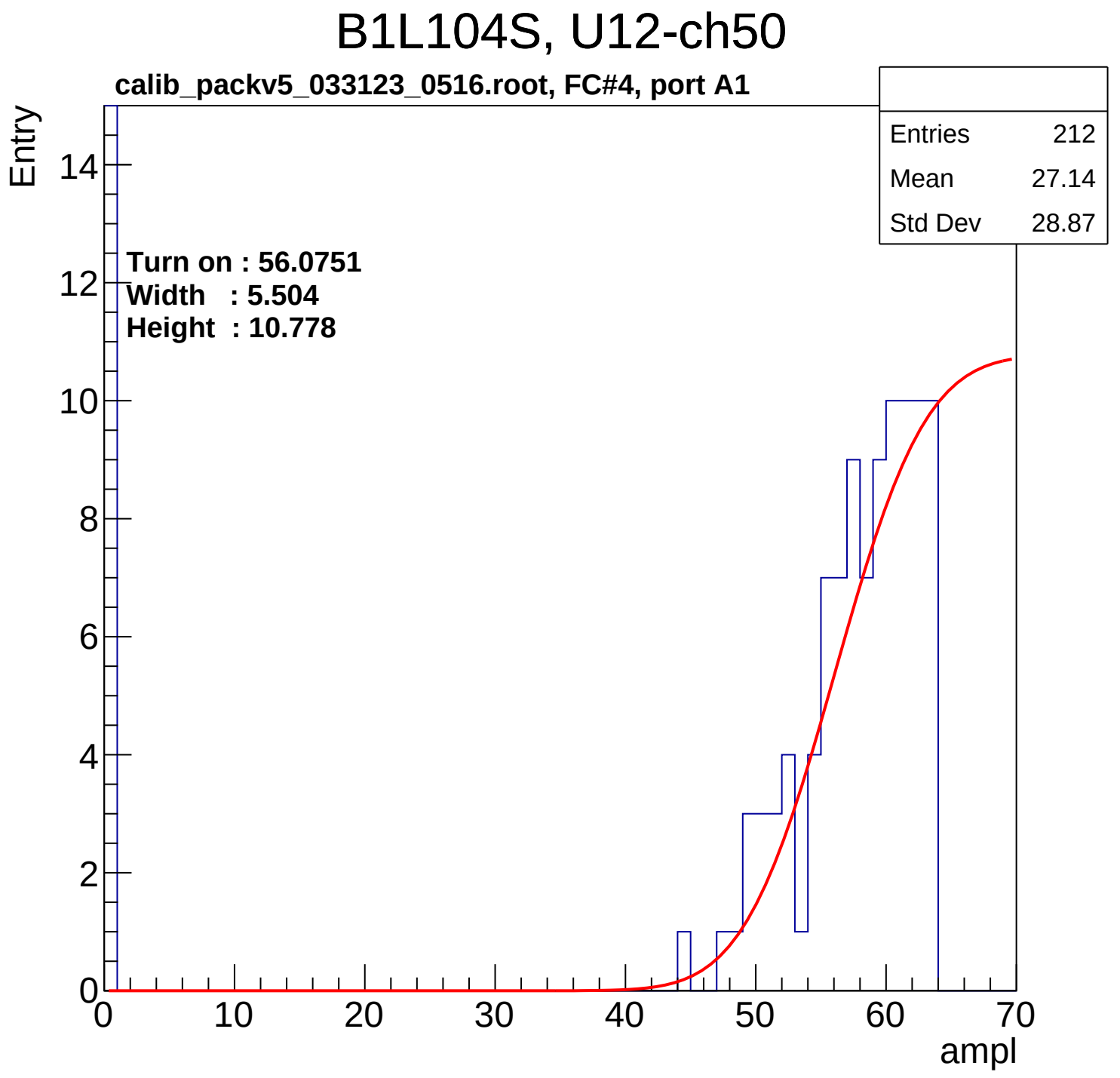
B1L104S, U12-ch50
calib_packv5_033123_0516.root, FC#4, port A1
Entries 212
Mean 27.14
Std Dev 28.87
Turn on : 56.0751
Width : 5.504
Height : 10.778
Entry
ampl
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6
8
10
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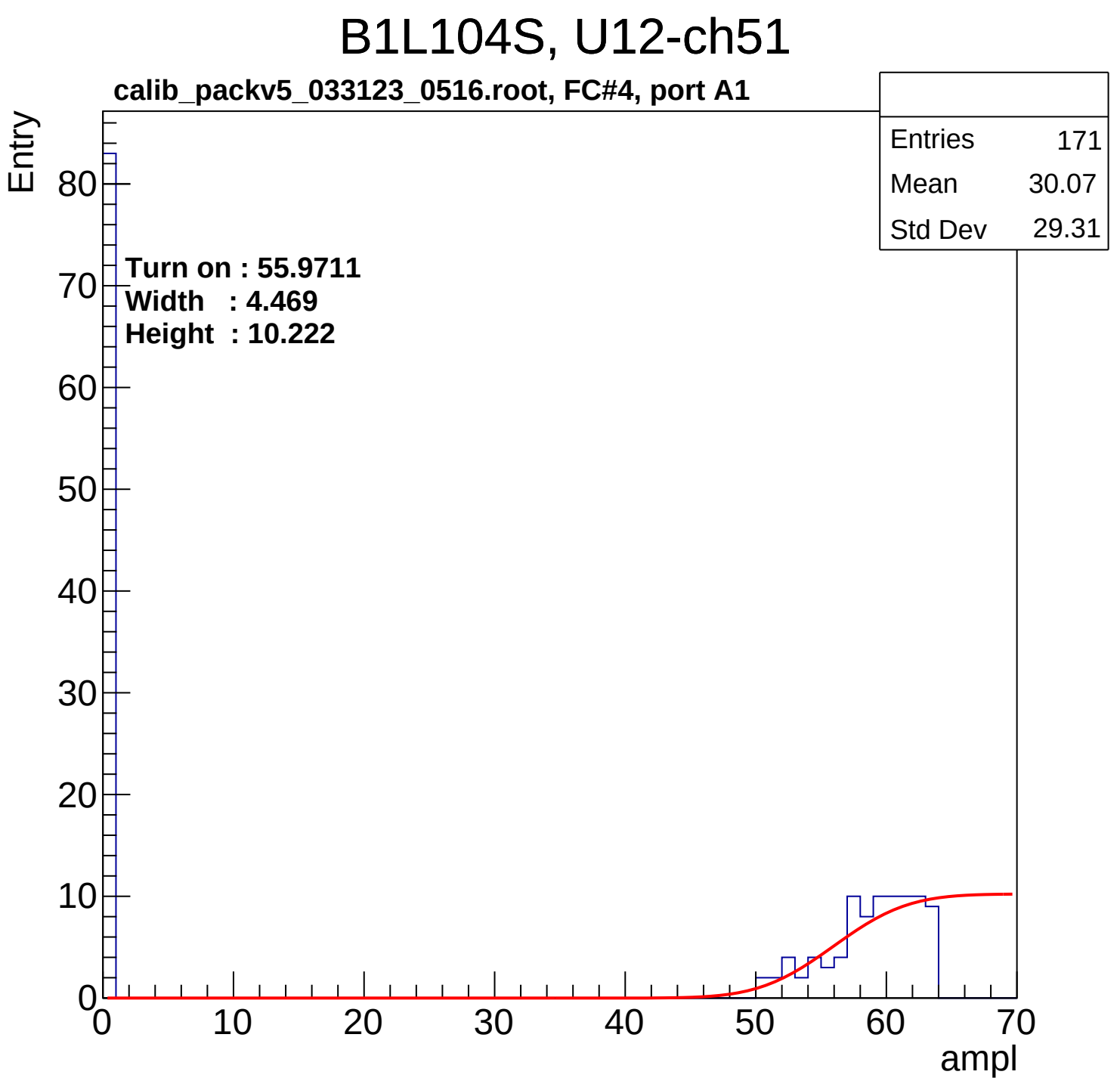
B1L104S, U12-ch51
calib_packv5_033123_0516.root, FC#4, port A1
Entries 171
Mean 30.07
Std Dev 29.31
Turn on : 55.9711
Width : 4.469
Height : 10.222
Entry
ampl
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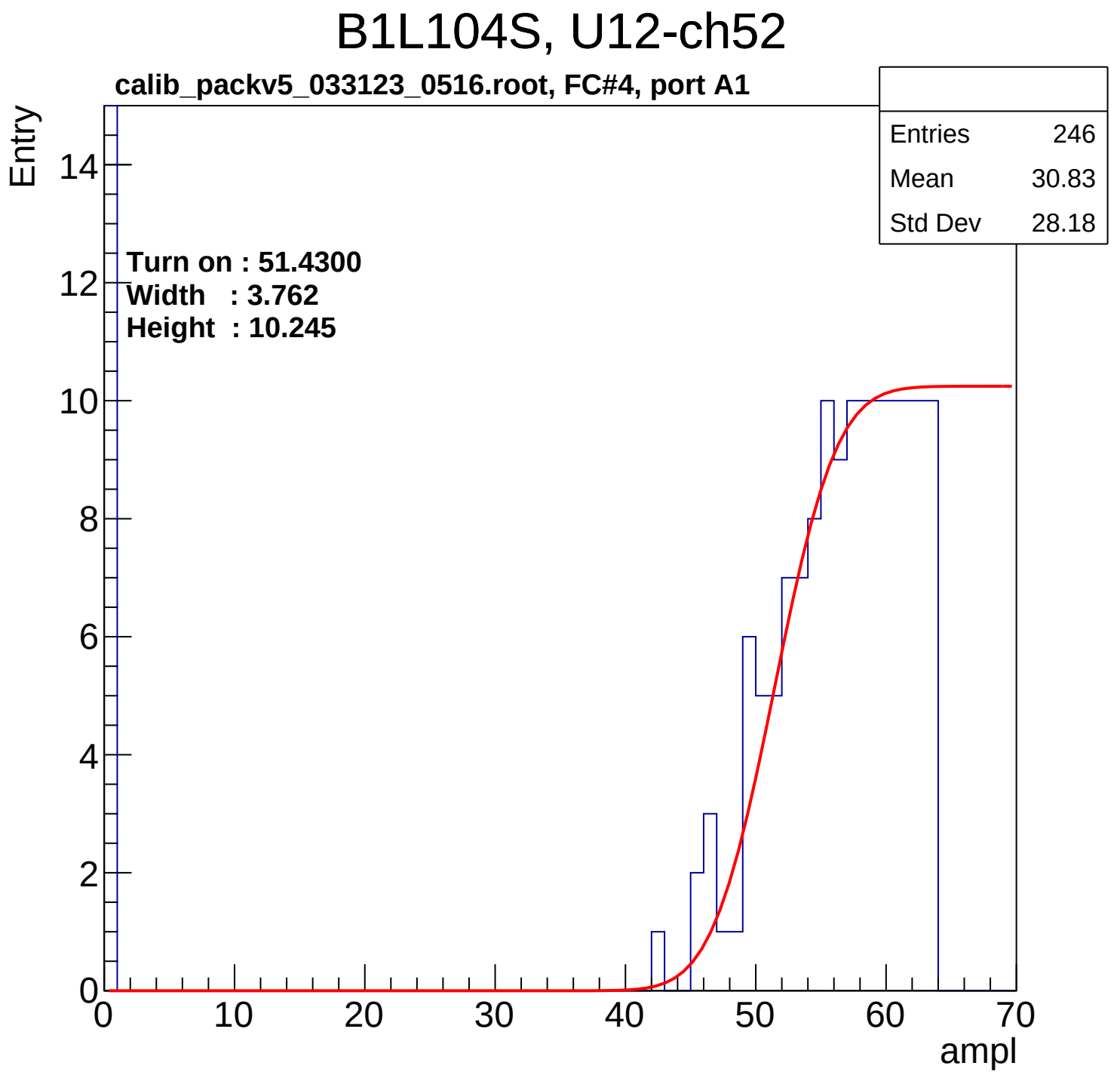
B1L104S, U12-ch52
calib_packv5_033123_0516.root, FC#4, port A1
Entries 246
Mean 30.83
Std Dev 28.18
Turn on : 51.4300
Width : 3.762
Height : 10.245
Entry
ampl
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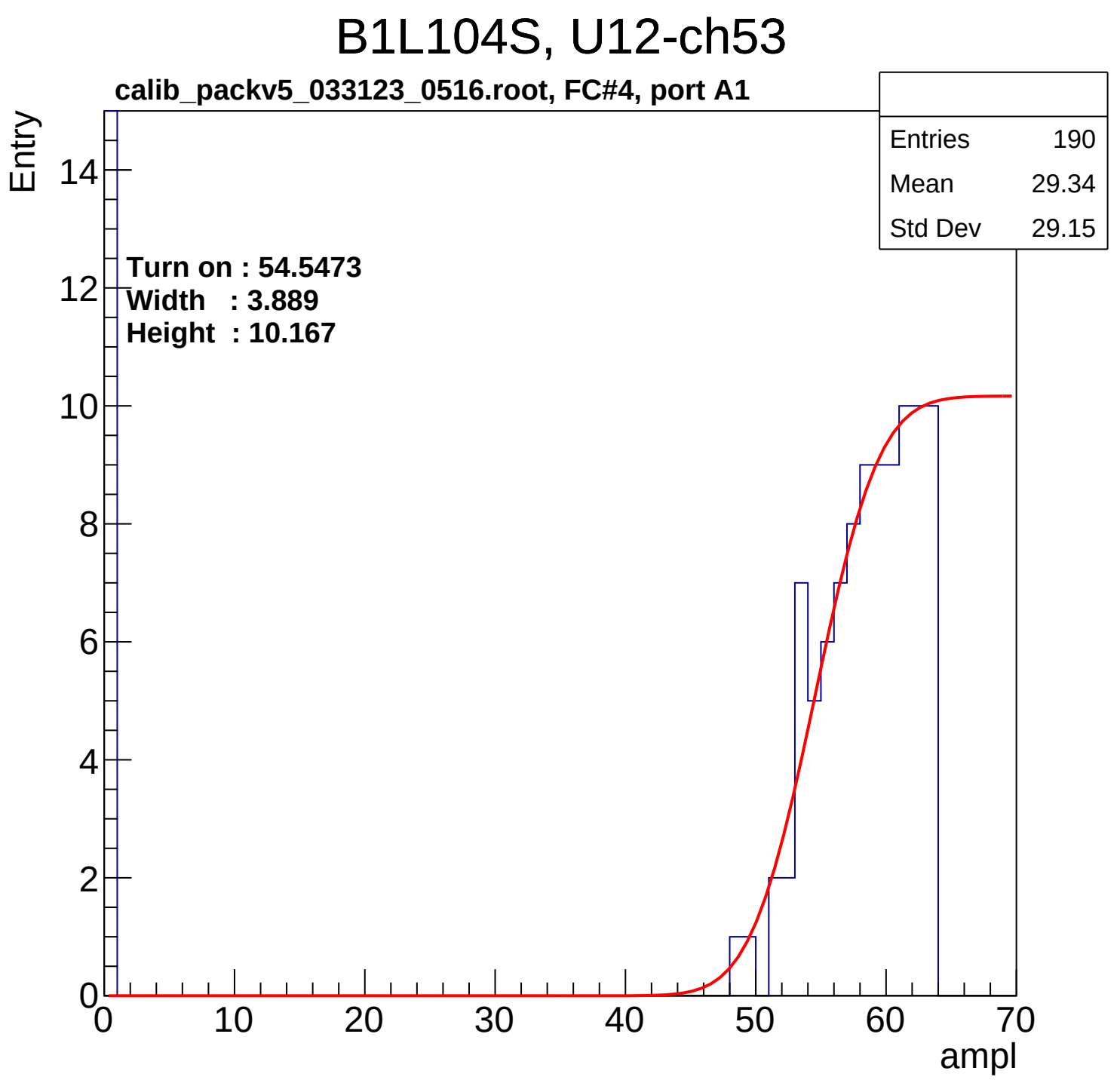
B1L104S, U12-ch53
calib_packv5_033123_0516.root, FC#4, port A1
Entries 190
Mean 29.34
Std Dev 29.15
Turn on : 54.5473
Width : 3.889
Height : 10.167
Entry
ampl
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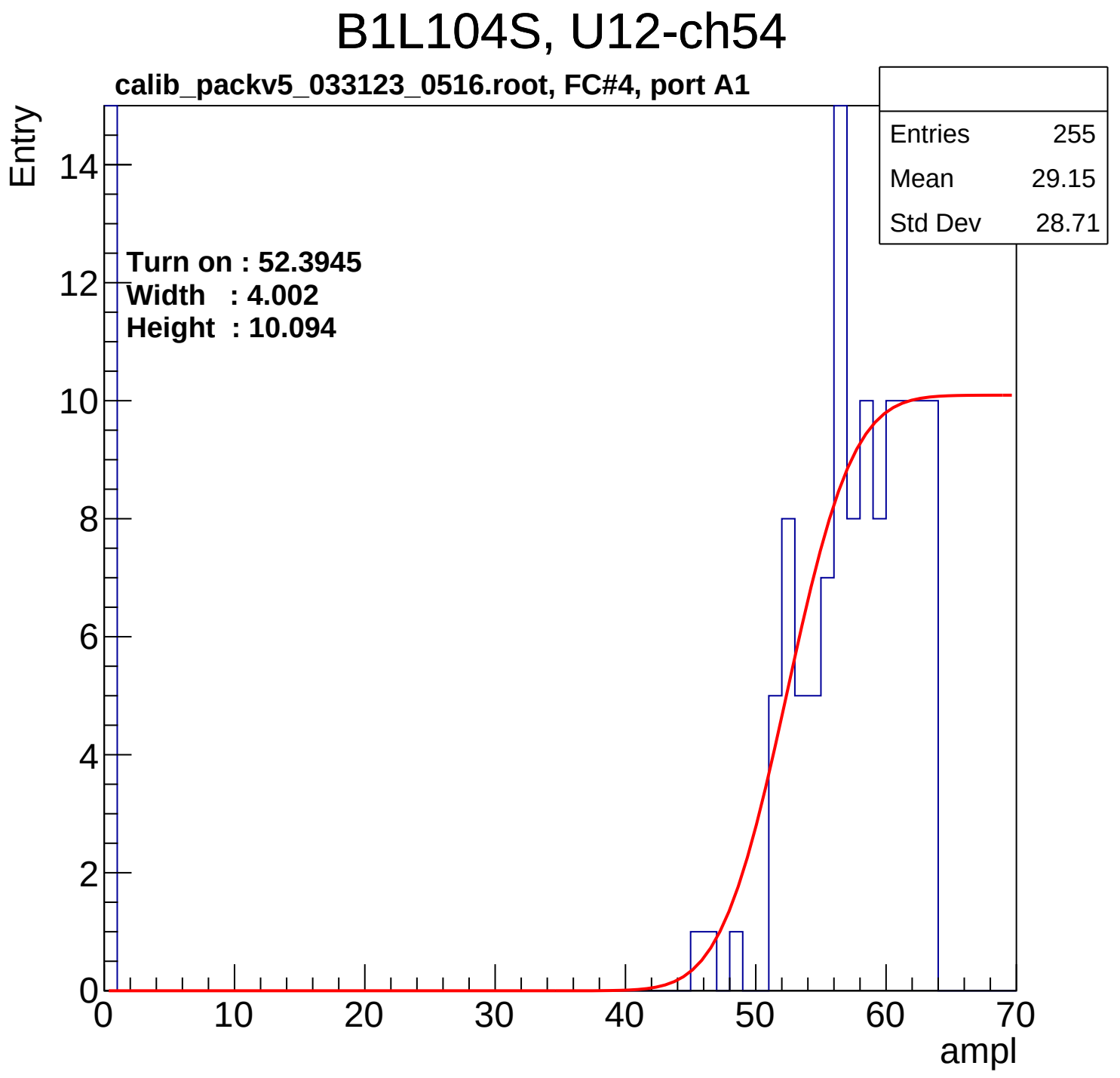
B1L104S, U12-ch54
calib_packv5_033123_0516.root, FC#4, port A1
Entries 255
Mean 29.15
Std Dev 28.71
Turn on : 52.3945
Width : 4.002
Height : 10.094
Entry
ampl
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6
8
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60
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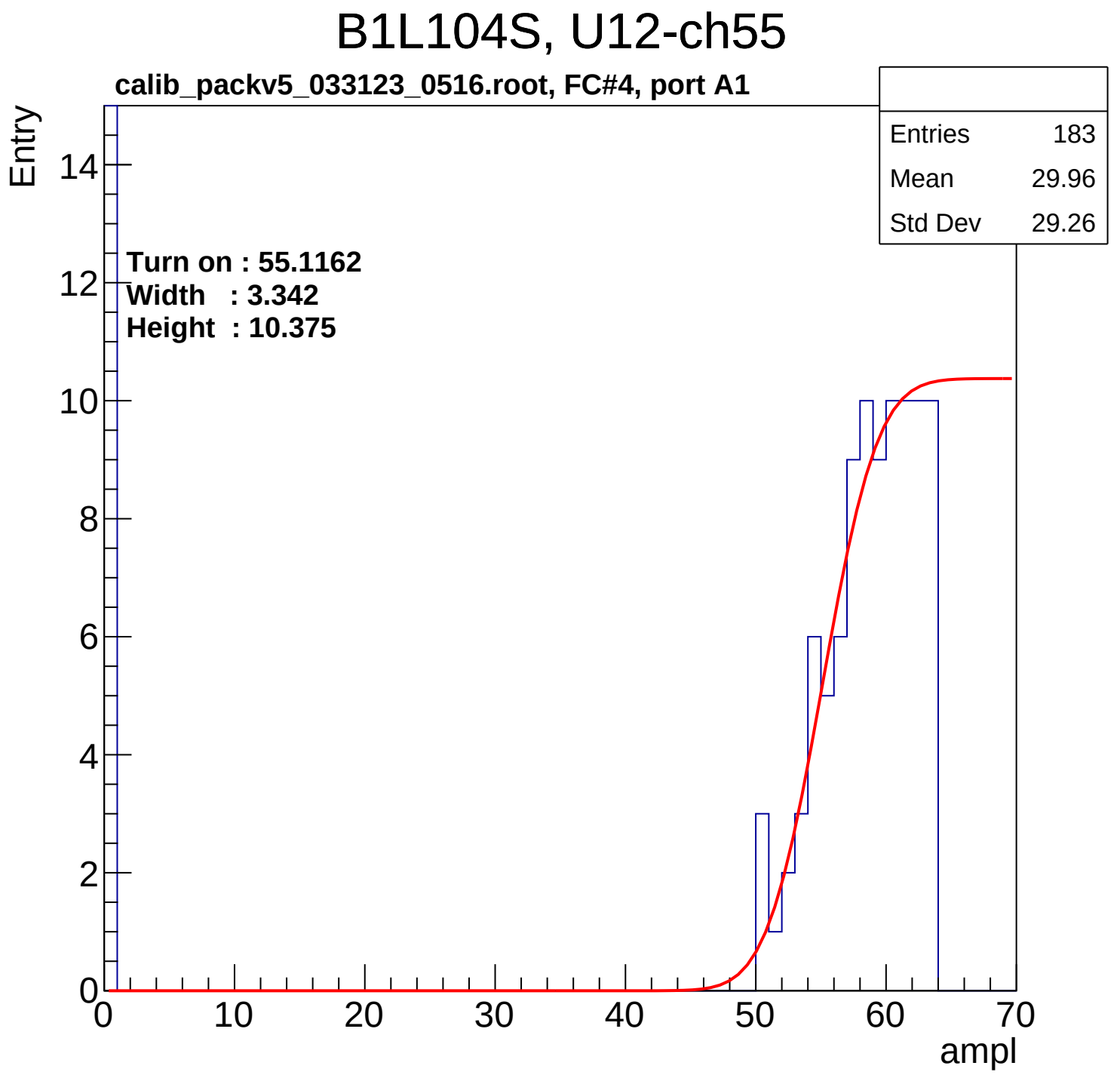
B1L104S, U12-ch55
calib_packv5_033123_0516.root, FC#4, port A1
Entries 183
Mean 29.96
Std Dev 29.26
Turn on : 55.1162
Width : 3.342
Height : 10.375
Entry
ampl
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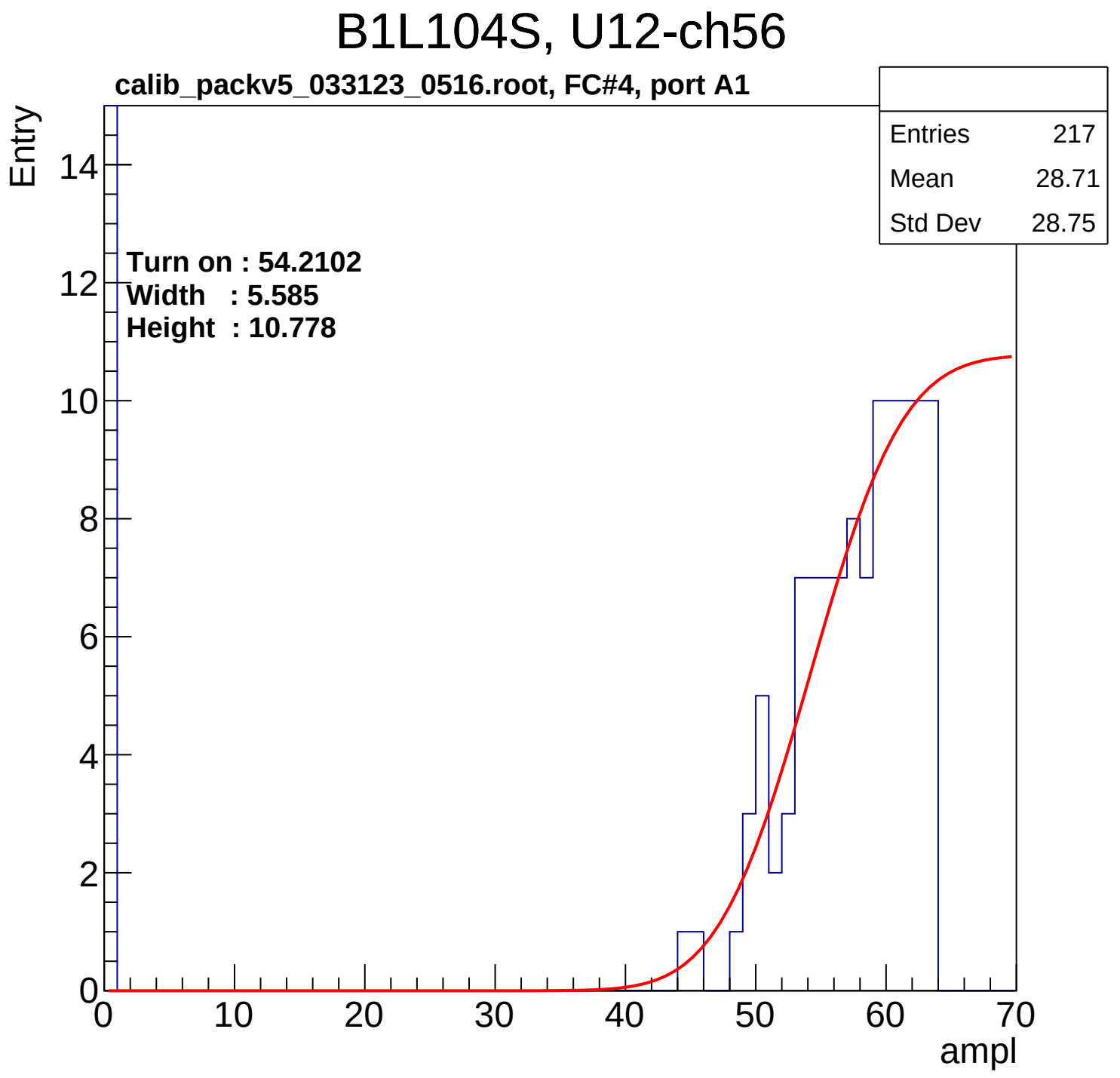
B1L104S, U12-ch56
calib_packv5_033123_0516.root, FC#4, port A1
Entries 217
Mean 28.71
Std Dev 28.75
Turn on : 54.2102
Width : 5.585
Height : 10.778
Entry
ampl
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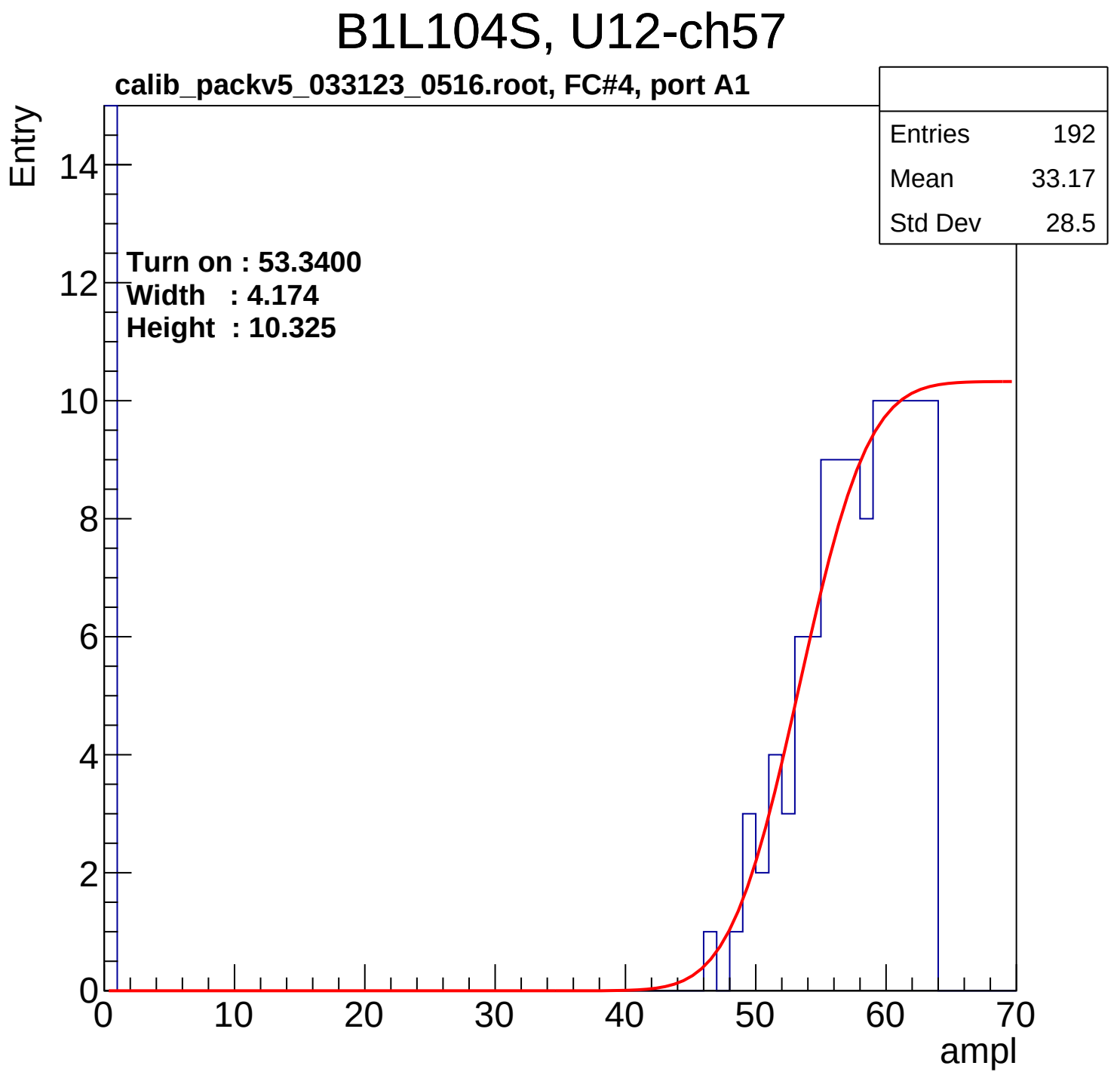
B1L104S, U12-ch57
calib_packv5_033123_0516.root, FC#4, port A1
Entries 192
Mean 33.17
Std Dev 28.5
Turn on : 53.3400
Width : 4.174
Height : 10.325
Entry
ampl
0
2
4
6
8
10
12
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20
30
40
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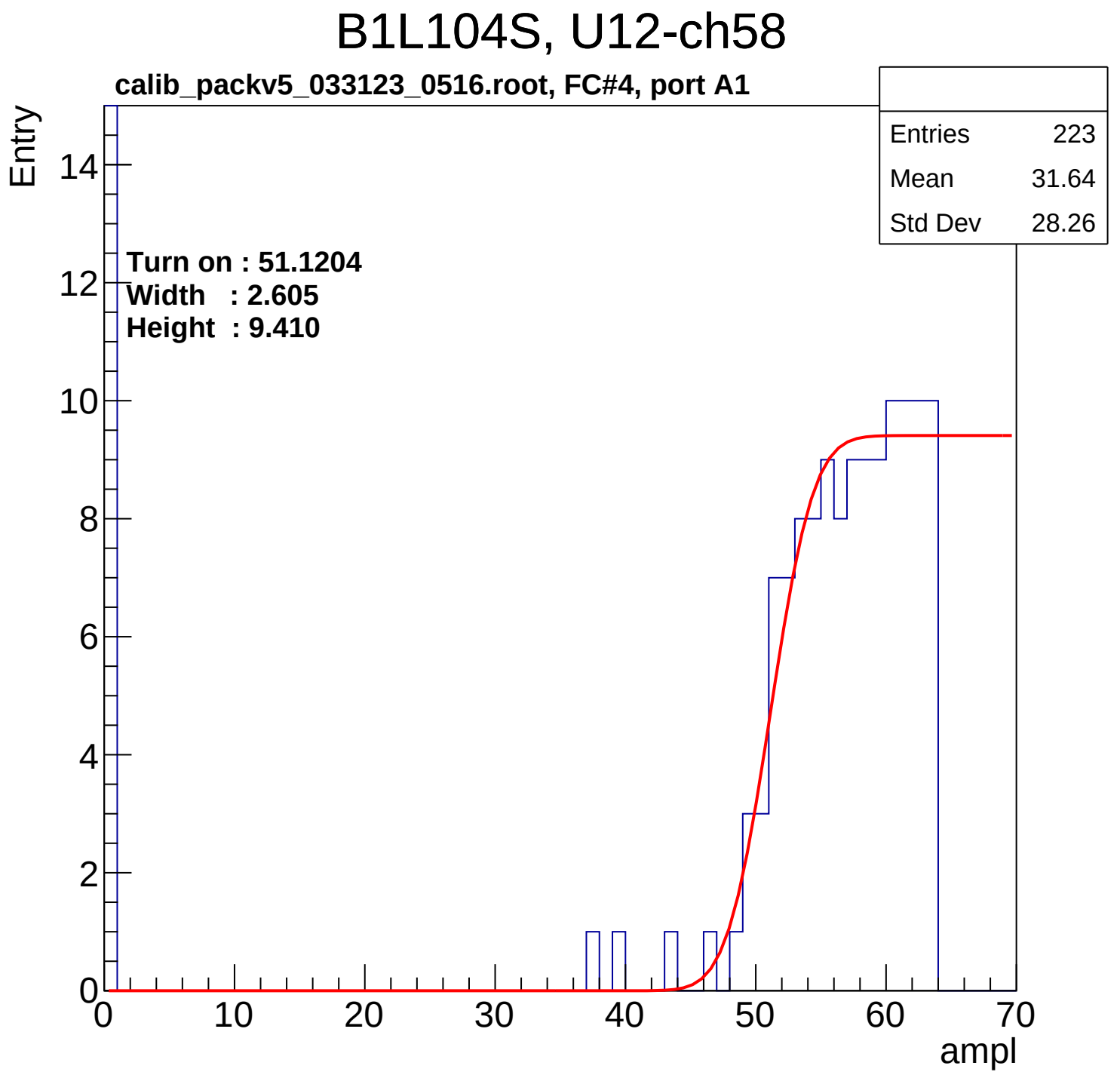
B1L104S, U12-ch58
calib_packv5_033123_0516.root, FC#4, port A1
Entries 223
Mean 31.64
Std Dev 28.26
Turn on : 51.1204
Width : 2.605
Height : 9.410
Entry
ampl
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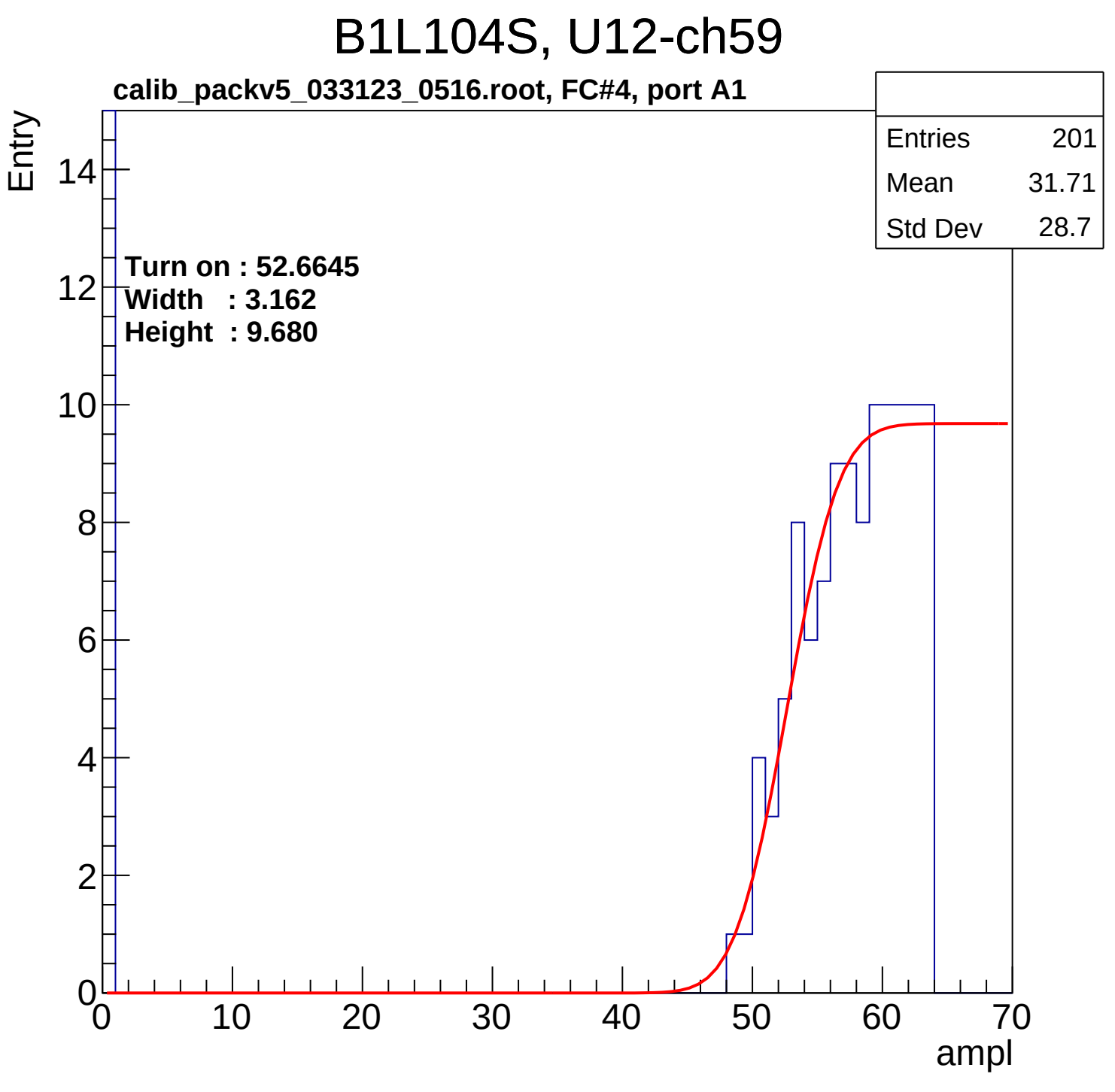
B1L104S, U12-ch59
calib_packv5_033123_0516.root, FC#4, port A1
Entries 201
Mean 31.71
Std Dev 28.7
Turn on : 52.6645
Width : 3.162
Height : 9.680
Entry
ampl
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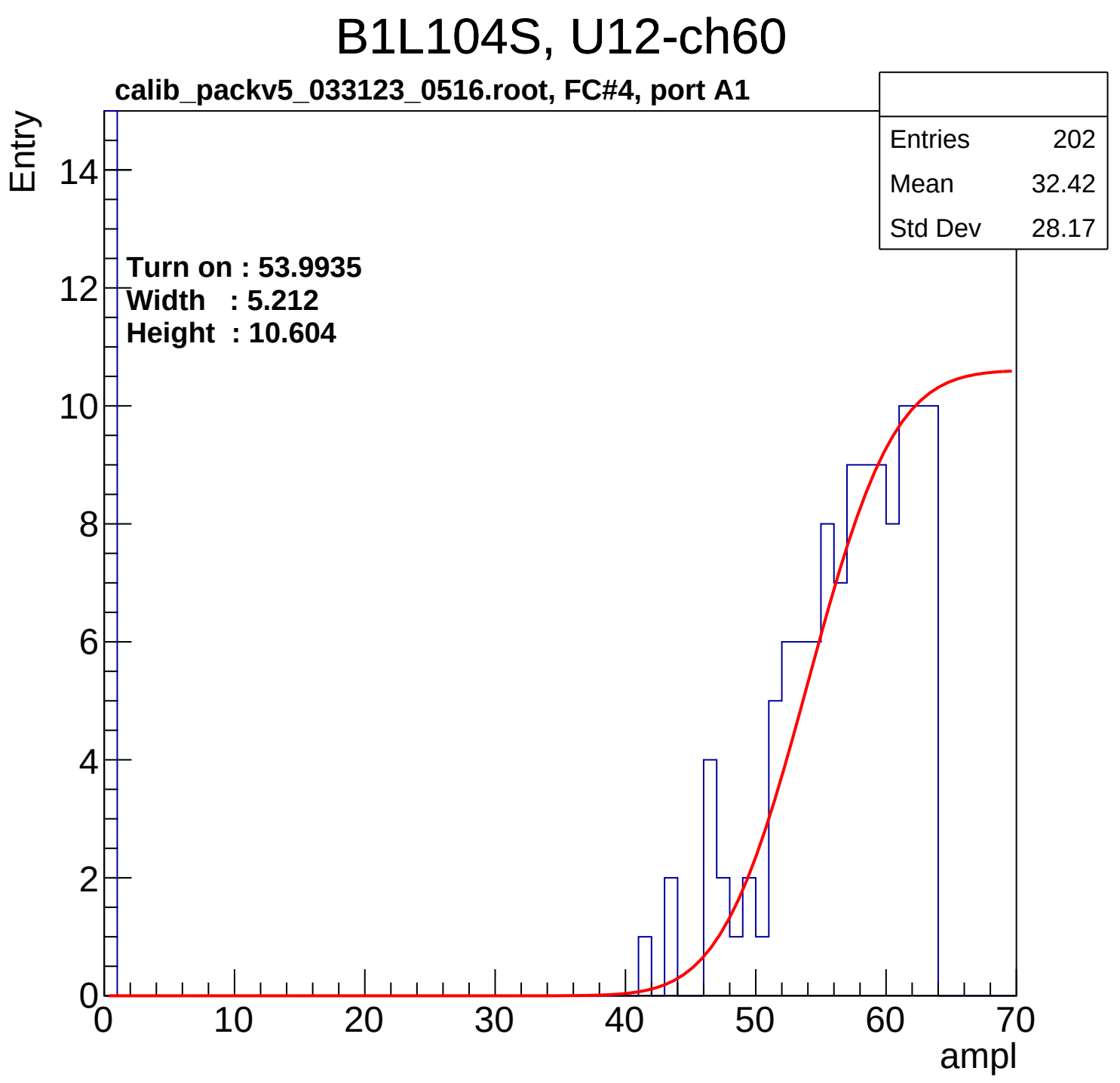
B1L104S, U12-ch60
calib_packv5_033123_0516.root, FC#4, port A1
Entries 202
Mean 32.42
Std Dev 28.17
Turn on : 53.9935
Width : 5.212
Height : 10.604
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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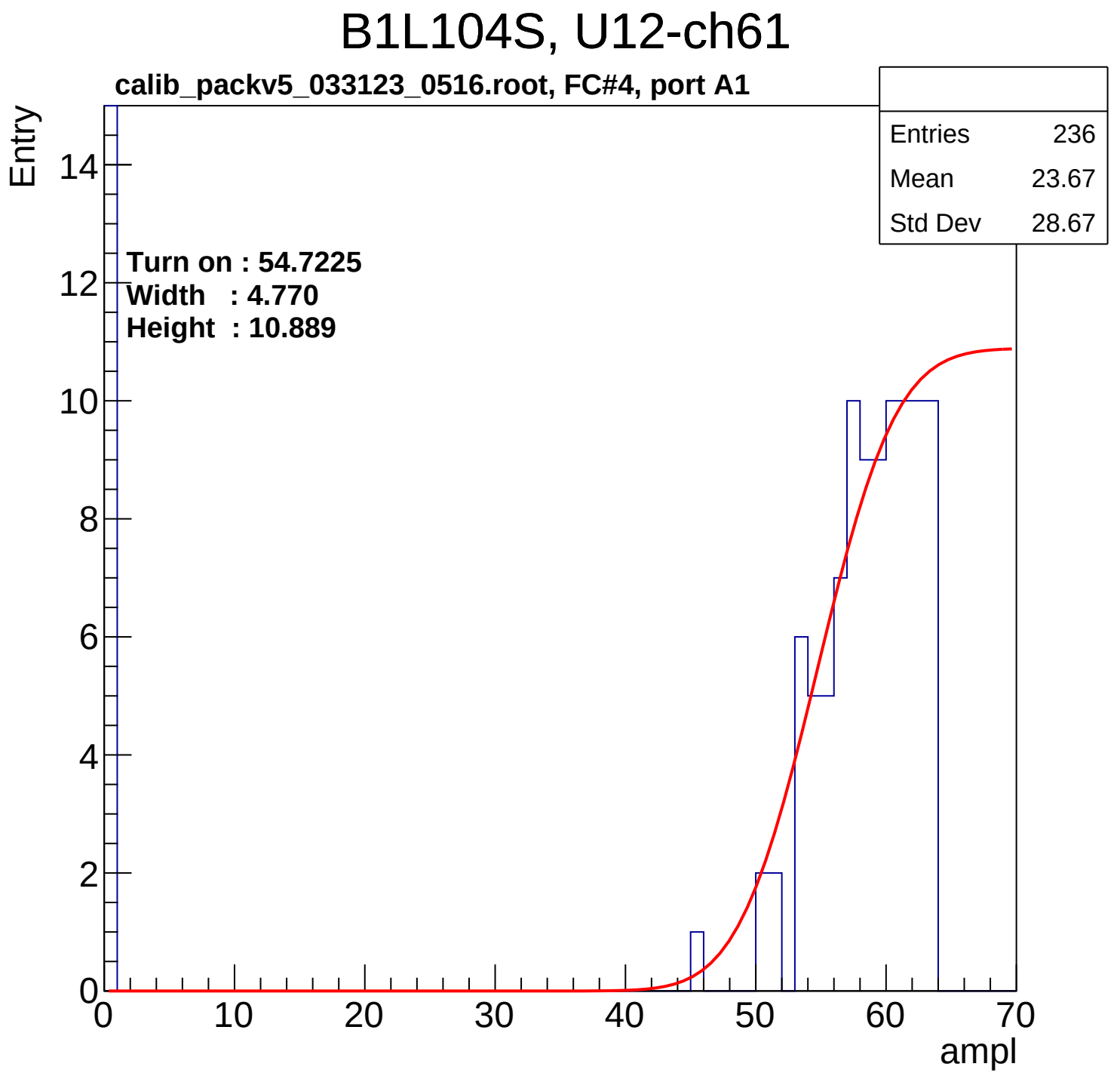
B1L104S, U12-ch61
calib_packv5_033123_0516.root, FC#4, port A1
Entries 236
Mean 23.67
Std Dev 28.67
Turn on : 54.7225
Width : 4.770
Height : 10.889
Entry
ampl
0
2
4
6
8
10
12
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0
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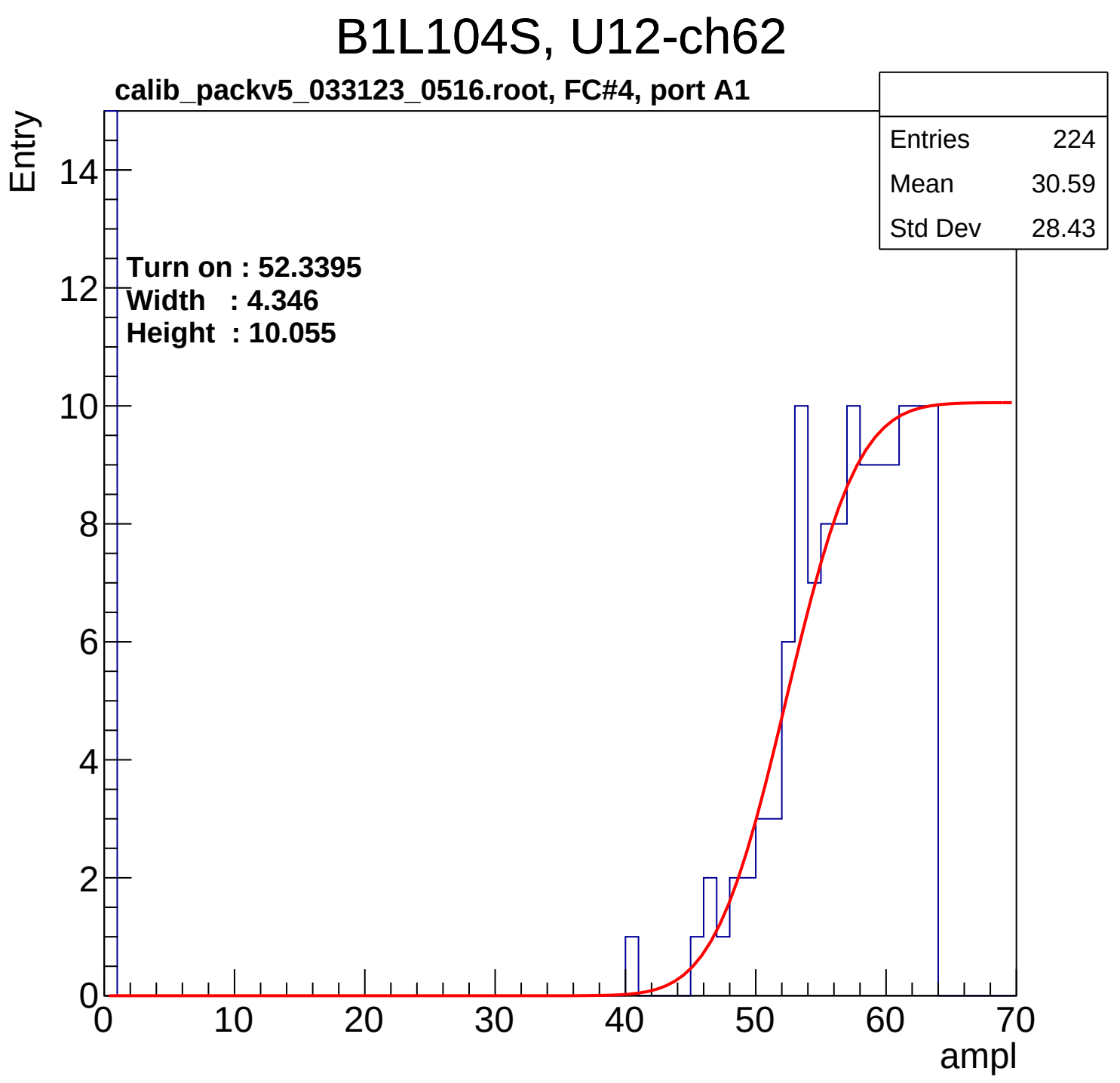
B1L104S, U12-ch62
calib_packv5_033123_0516.root, FC#4, port A1
Entries 224
Mean 30.59
Std Dev 28.43
Turn on : 52.3395
Width : 4.346
Height : 10.055
Entry
ampl
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2
4
6
8
10
12
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0
10
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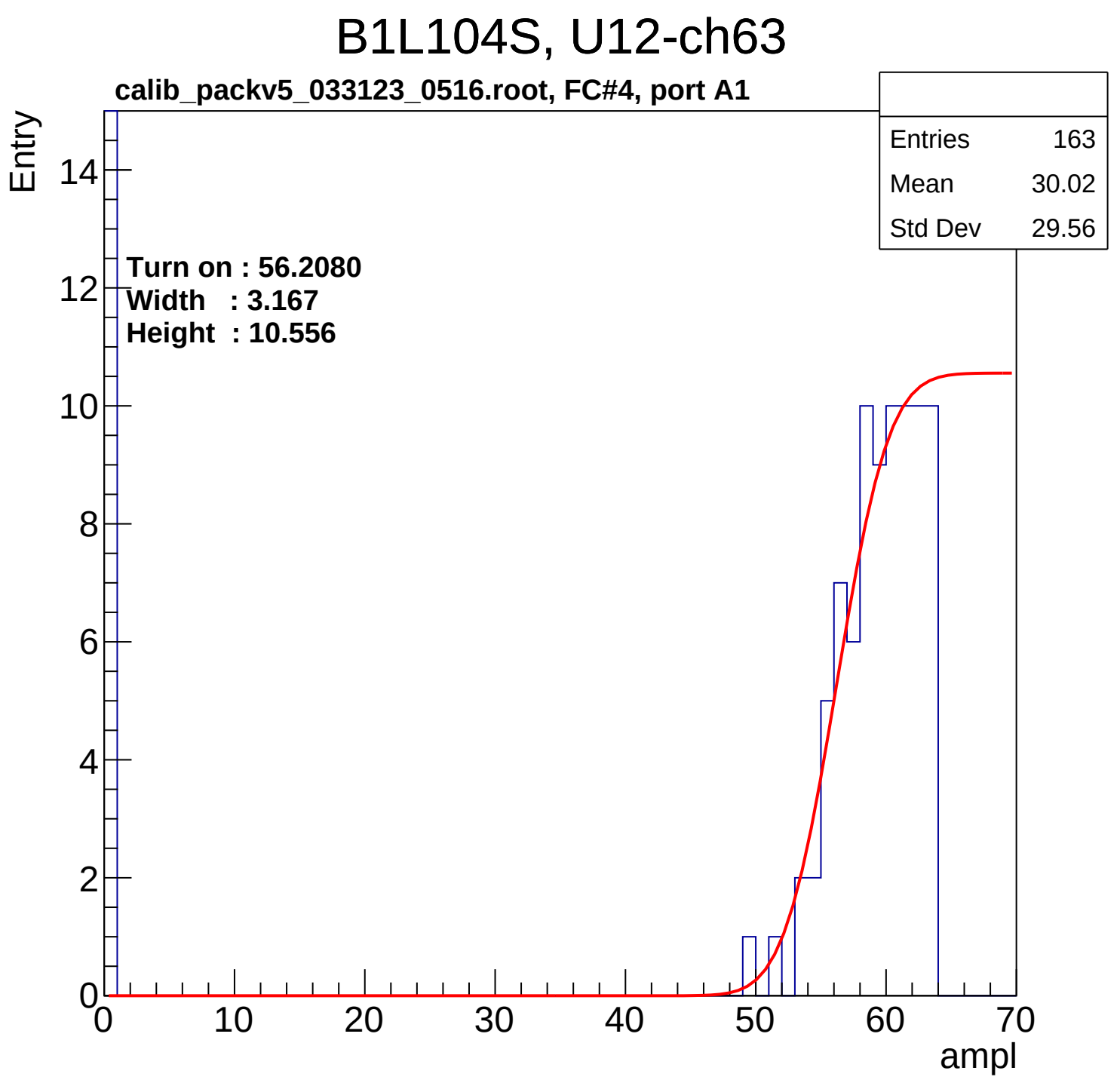
B1L104S, U12-ch63
calib_packv5_033123_0516.root, FC#4, port A1
Entries 163
Mean 30.02
Std Dev 29.56
Turn on : 56.2080
Width : 3.167
Height : 10.556
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
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60
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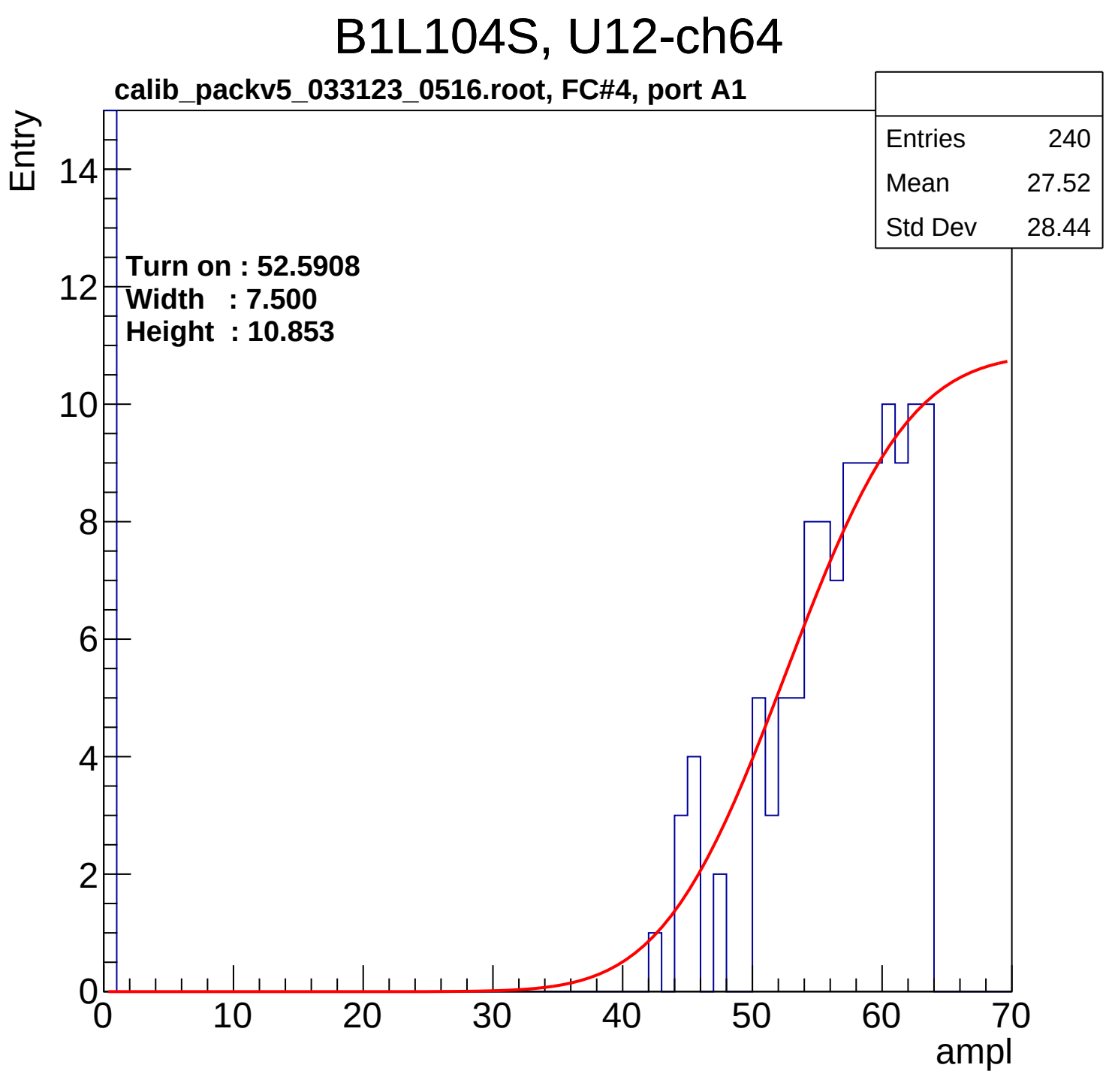
B1L104S, U12-ch64
calib_packv5_033123_0516.root, FC#4, port A1
Entries 240
Mean 27.52
Std Dev 28.44
Turn on : 52.5908
Width : 7.500
Height : 10.853
Entry
ampl
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4
6
8
10
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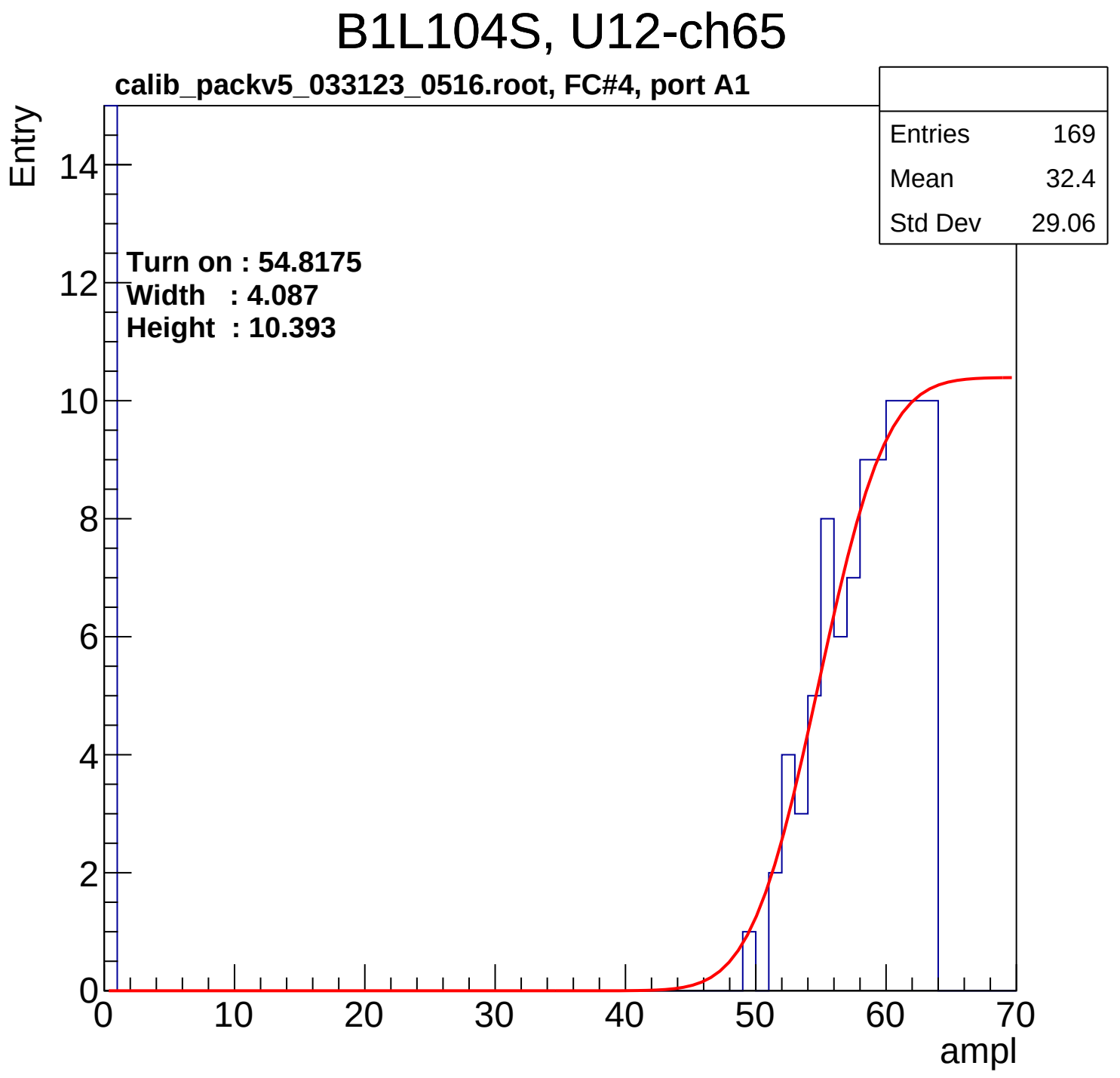
B1L104S, U12-ch65
calib_packv5_033123_0516.root, FC#4, port A1
Entries 169
Mean 32.4
Std Dev 29.06
Turn on : 54.8175
Width : 4.087
Height : 10.393
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
30
40
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60
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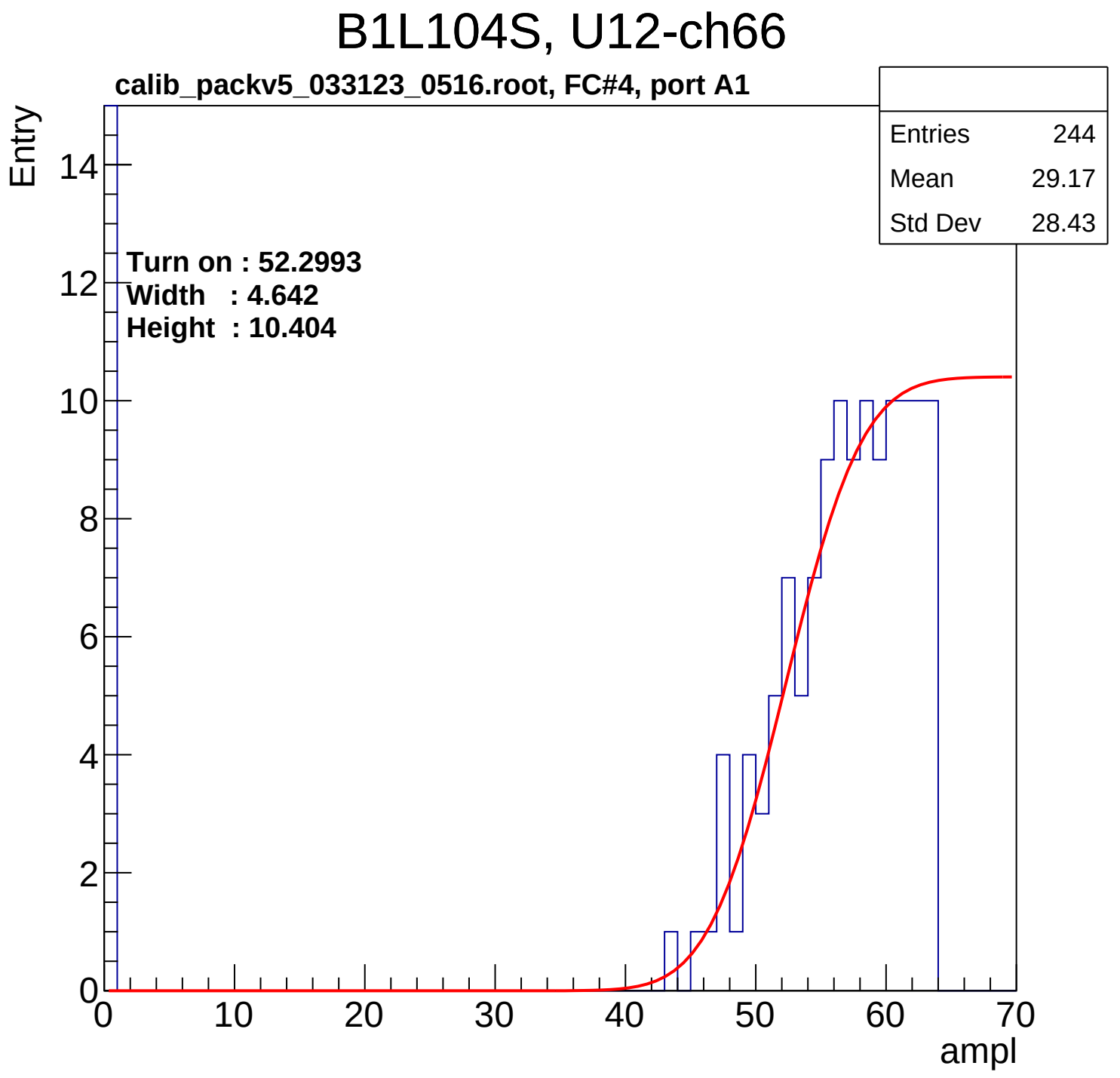
B1L104S, U12-ch66
calib_packv5_033123_0516.root, FC#4, port A1
Entries 244
Mean 29.17
Std Dev 28.43
Turn on : 52.2993
Width : 4.642
Height : 10.404
Entry
ampl
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6
8
10
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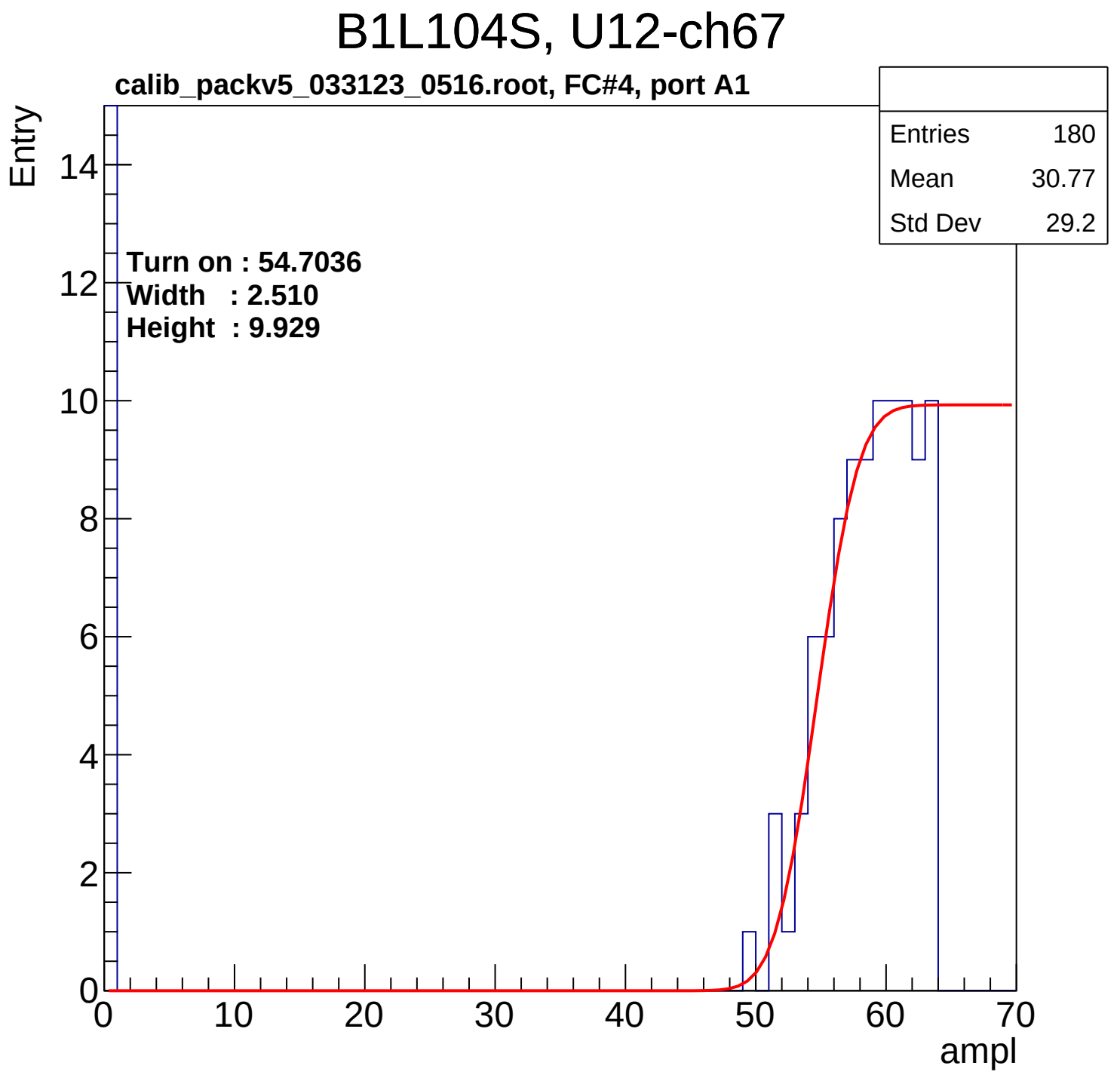
B1L104S, U12-ch67
calib_packv5_033123_0516.root, FC#4, port A1
Entries 180
Mean 30.77
Std Dev 29.2
Turn on : 54.7036
Width : 2.510
Height : 9.929
Entry
ampl
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6
8
10
12
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0
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60
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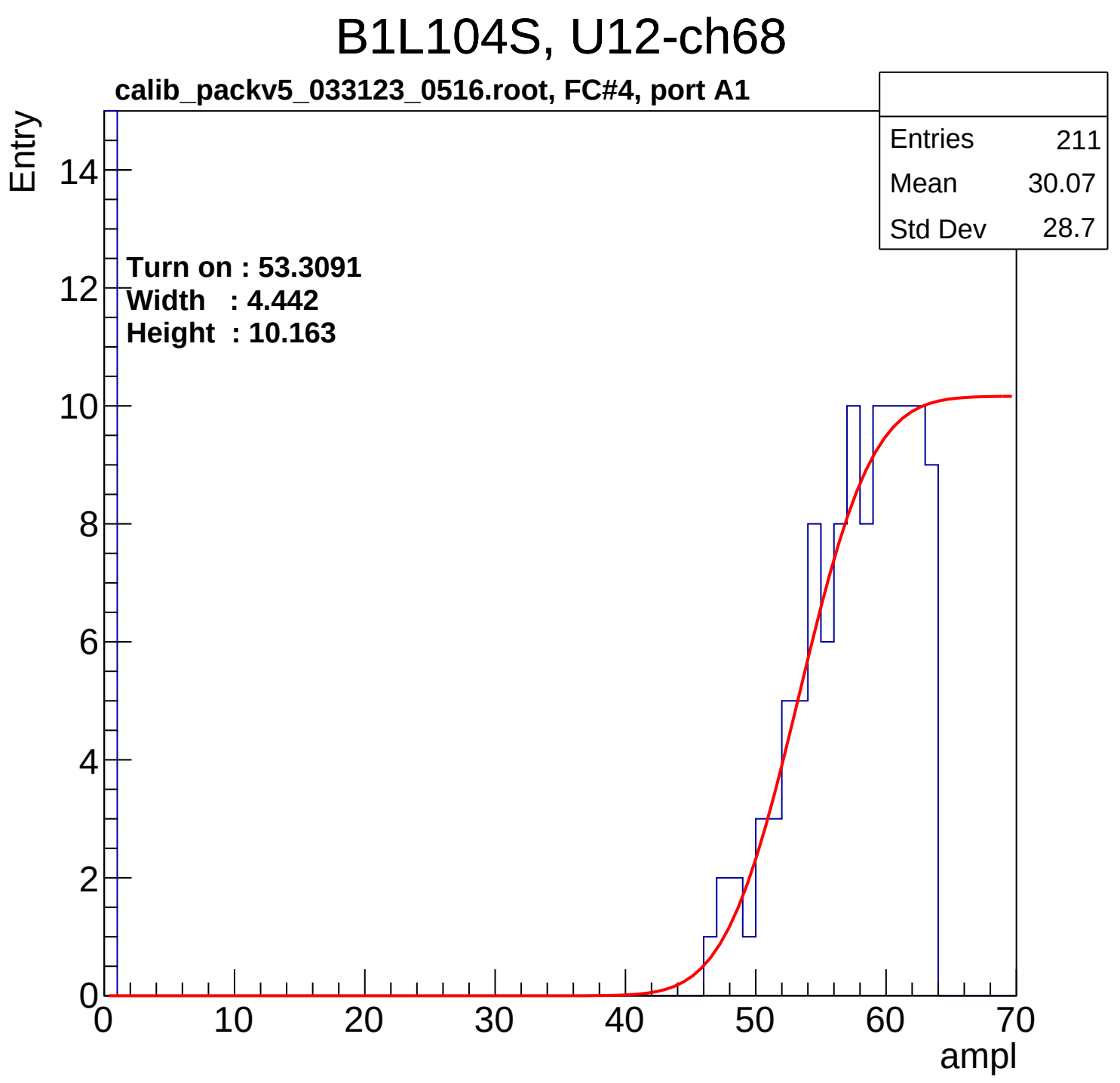
B1L104S, U12-ch68
calib_packv5_033123_0516.root, FC#4, port A1
Entries 211
Mean 30.07
Std Dev 28.7
Turn on : 53.3091
Width : 4.442
Height : 10.163
Entry
ampl
0
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6
8
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12
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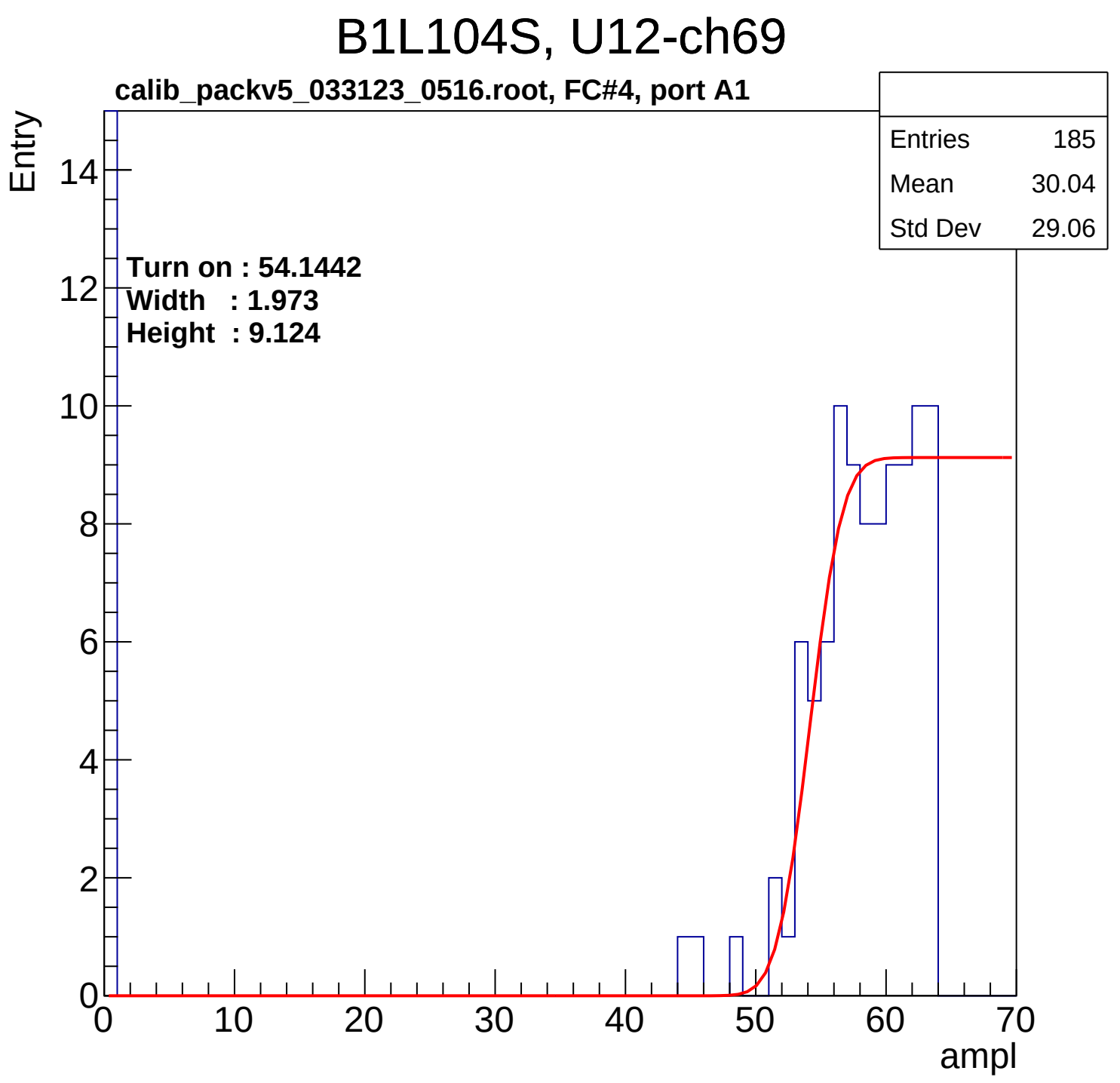
B1L104S, U12-ch69
calib_packv5_033123_0516.root, FC#4, port A1
Entries 185
Mean 30.04
Std Dev 29.06
Turn on : 54.1442
Width : 1.973
Height : 9.124
Entry
ampl
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4
6
8
10
12
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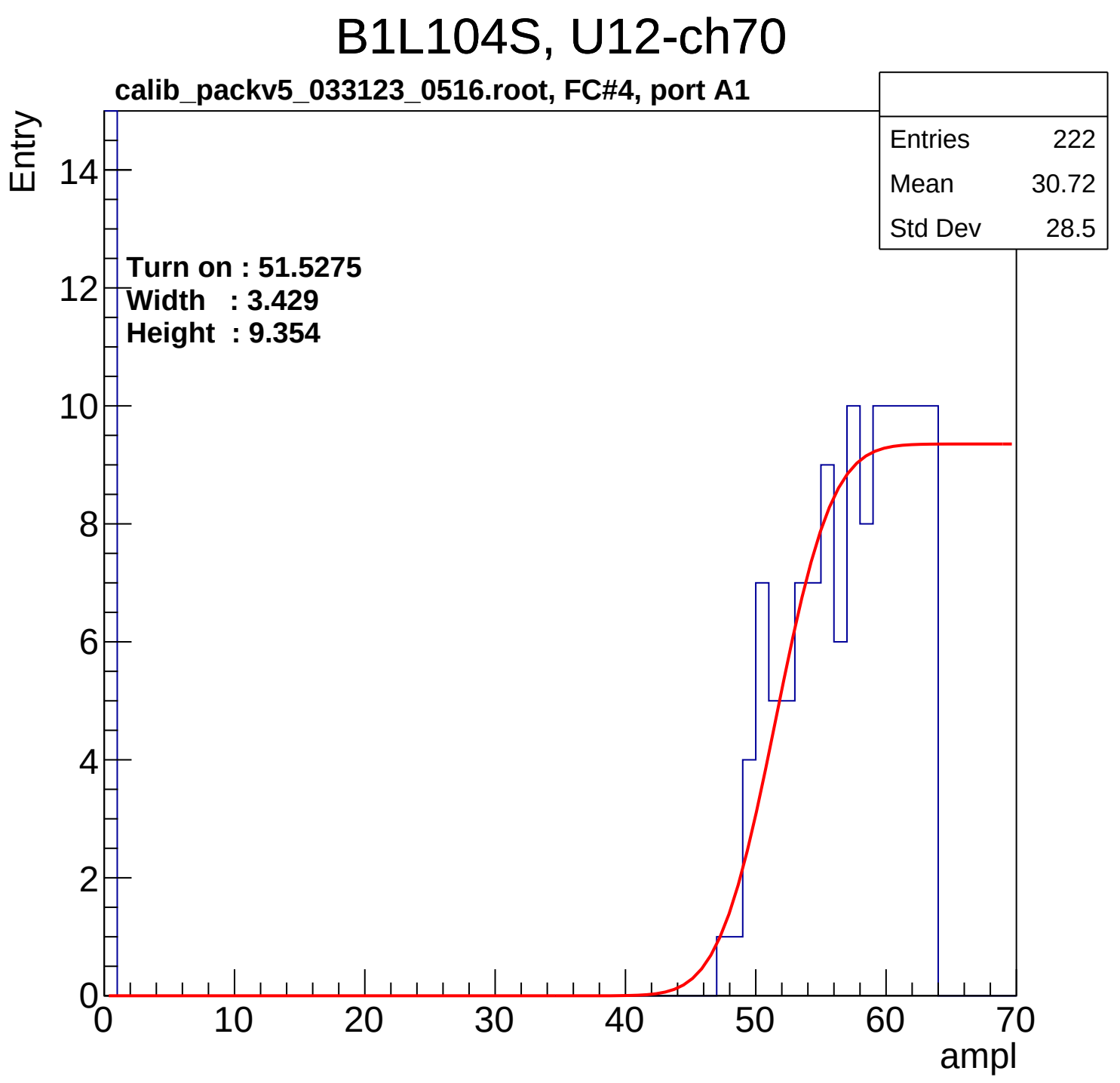
B1L104S, U12-ch70
calib_packv5_033123_0516.root, FC#4, port A1
Entries 222
Mean 30.72
Std Dev 28.5
Turn on : 51.5275
Width : 3.429
Height : 9.354
Entry
ampl
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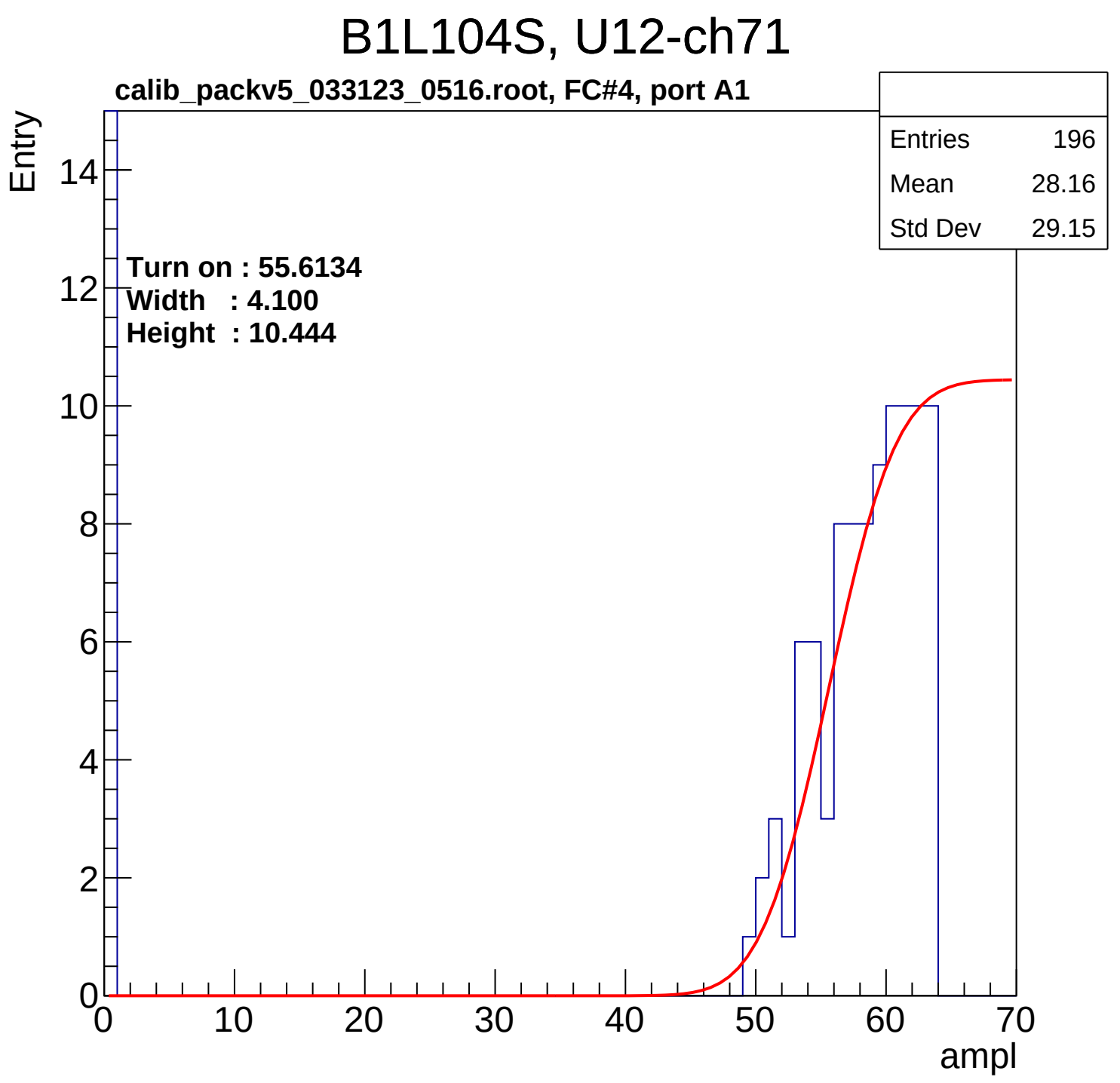
B1L104S, U12-ch71
calib_packv5_033123_0516.root, FC#4, port A1
Entries 196
Mean 28.16
Std Dev 29.15
Turn on : 55.6134
Width : 4.100
Height : 10.444
Entry
ampl
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6
8
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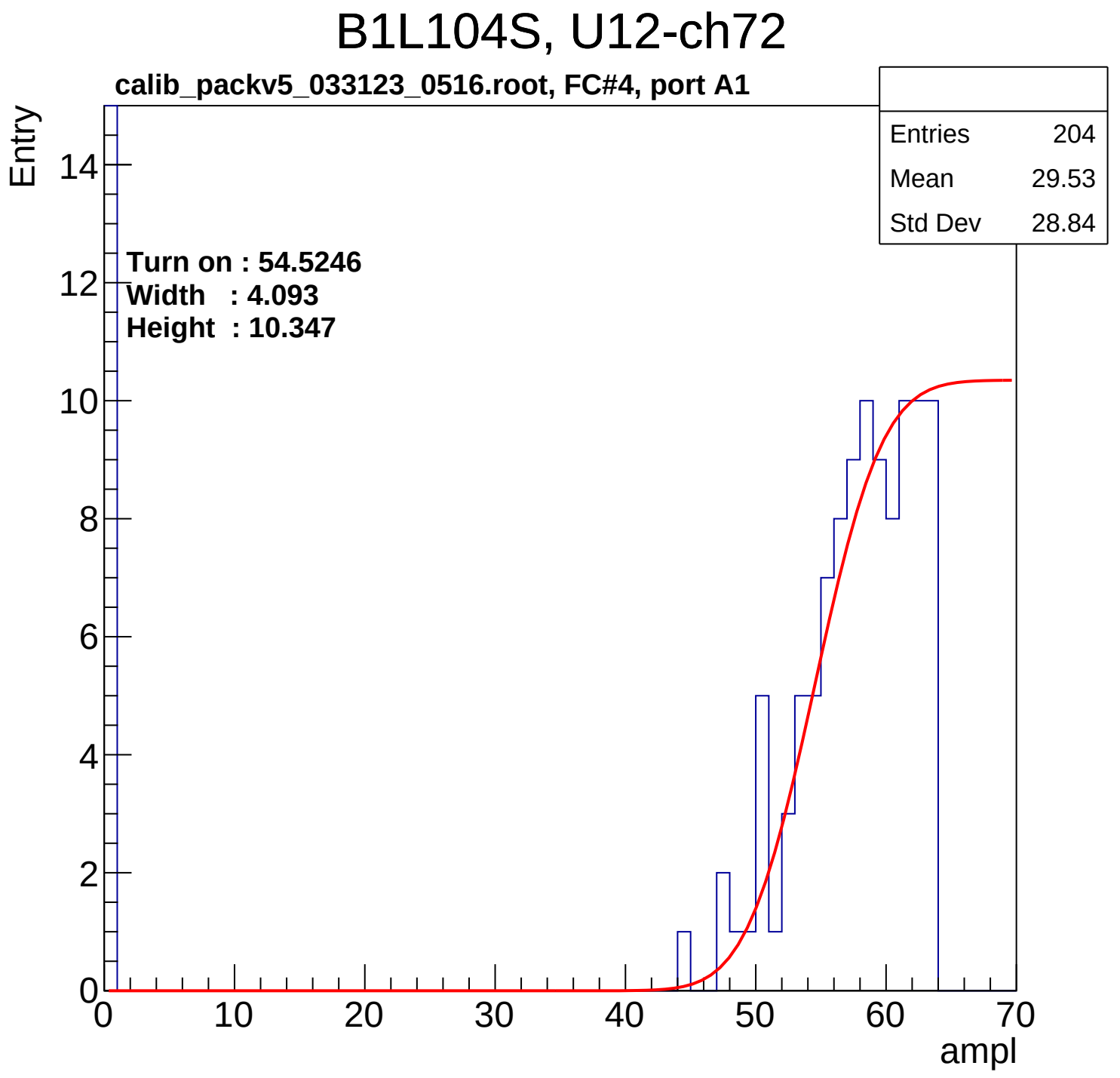
B1L104S, U12-ch72
calib_packv5_033123_0516.root, FC#4, port A1
Entries 204
Mean 29.53
Std Dev 28.84
Turn on : 54.5246
Width : 4.093
Height : 10.347
Entry
ampl
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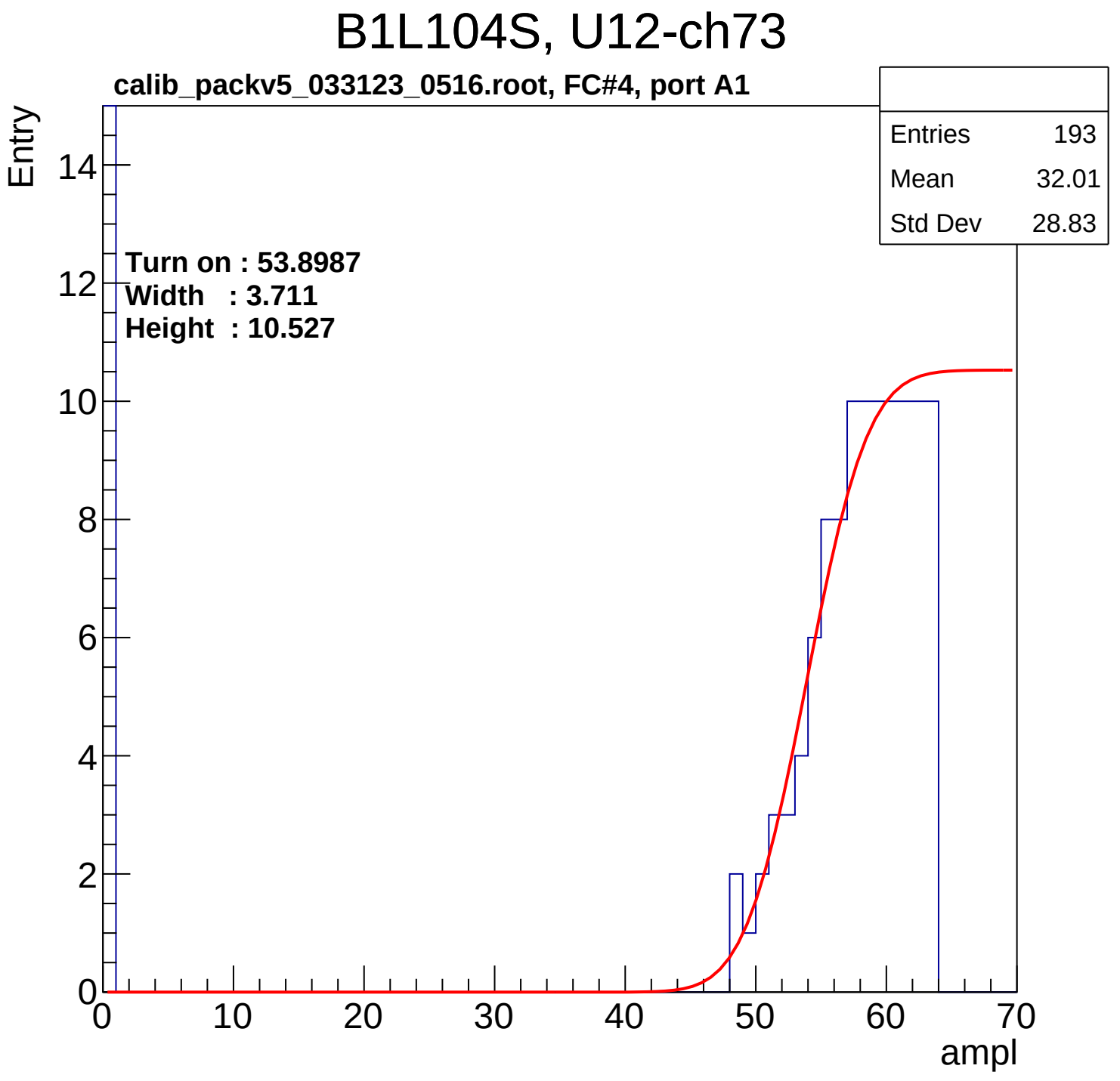
B1L104S, U12-ch73
calib_packv5_033123_0516.root, FC#4, port A1
Entries 193
Mean 32.01
Std Dev 28.83
Turn on : 53.8987
Width : 3.711
Height : 10.527
Entry
ampl
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8
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12
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0
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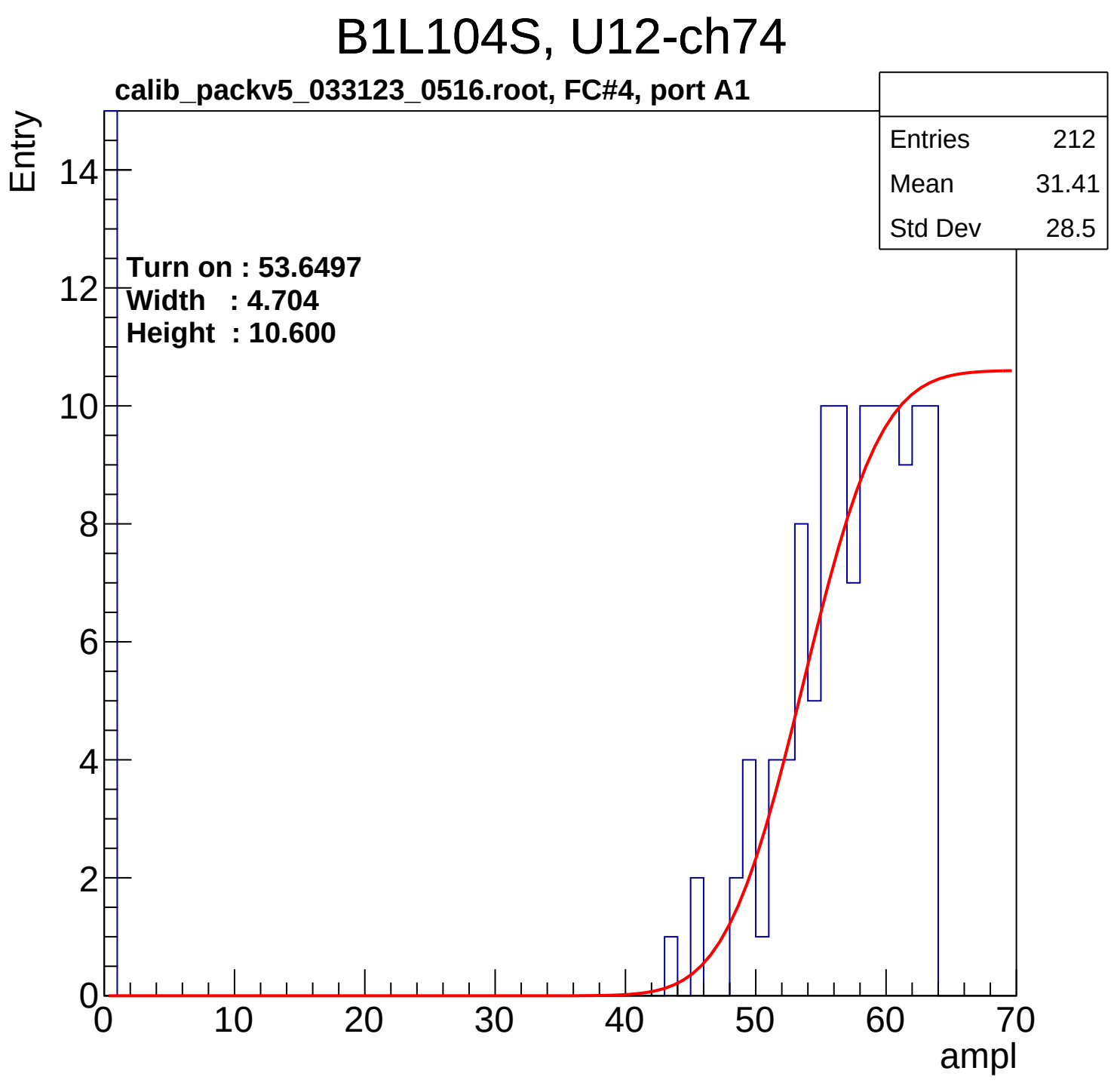
B1L104S, U12-ch74
calib_packv5_033123_0516.root, FC#4, port A1
Entries 212
Mean 31.41
Std Dev 28.5
Turn on : 53.6497
Width : 4.704
Height : 10.600
Entry
ampl
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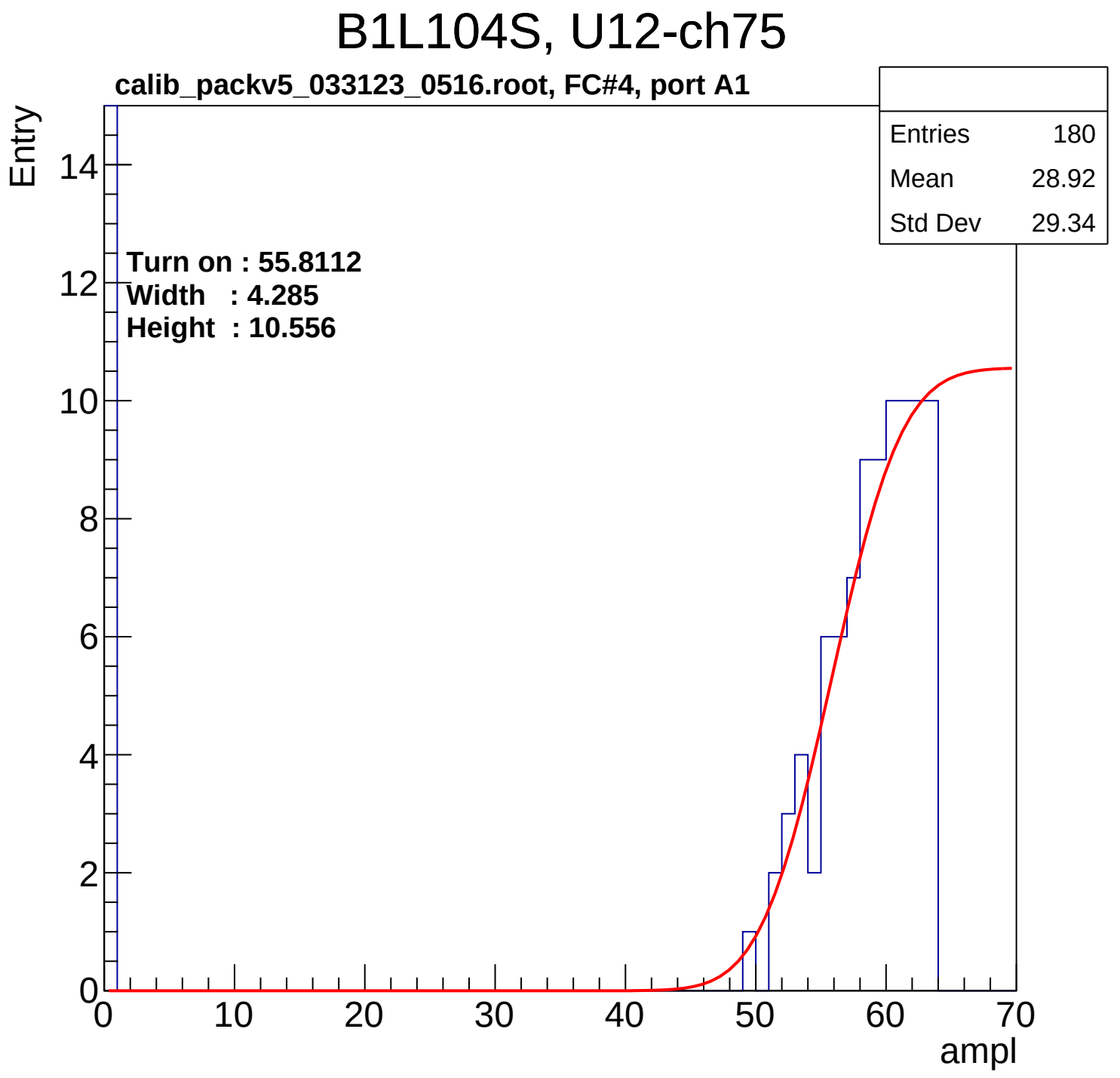
B1L104S, U12-ch75
calib_packv5_033123_0516.root, FC#4, port A1
Entries 180
Mean 28.92
Std Dev 29.34
Turn on : 55.8112
Width : 4.285
Height : 10.556
Entry
ampl
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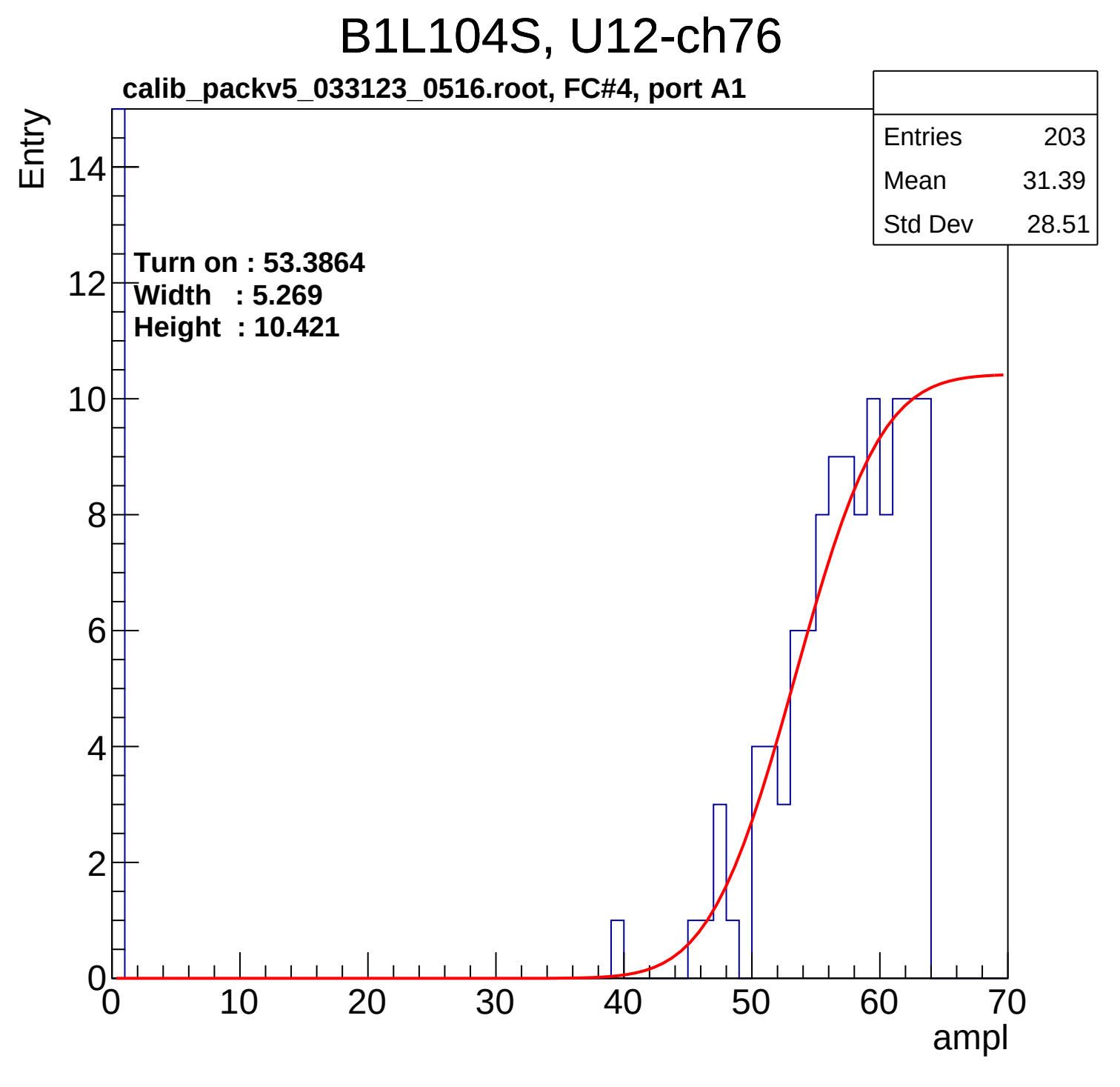
B1L104S, U12-ch76
calib_packv5_033123_0516.root, FC#4, port A1
Entries 203
Mean 31.39
Std Dev 28.51
Turn on : 53.3864
Width : 5.269
Height : 10.421
Entry
ampl
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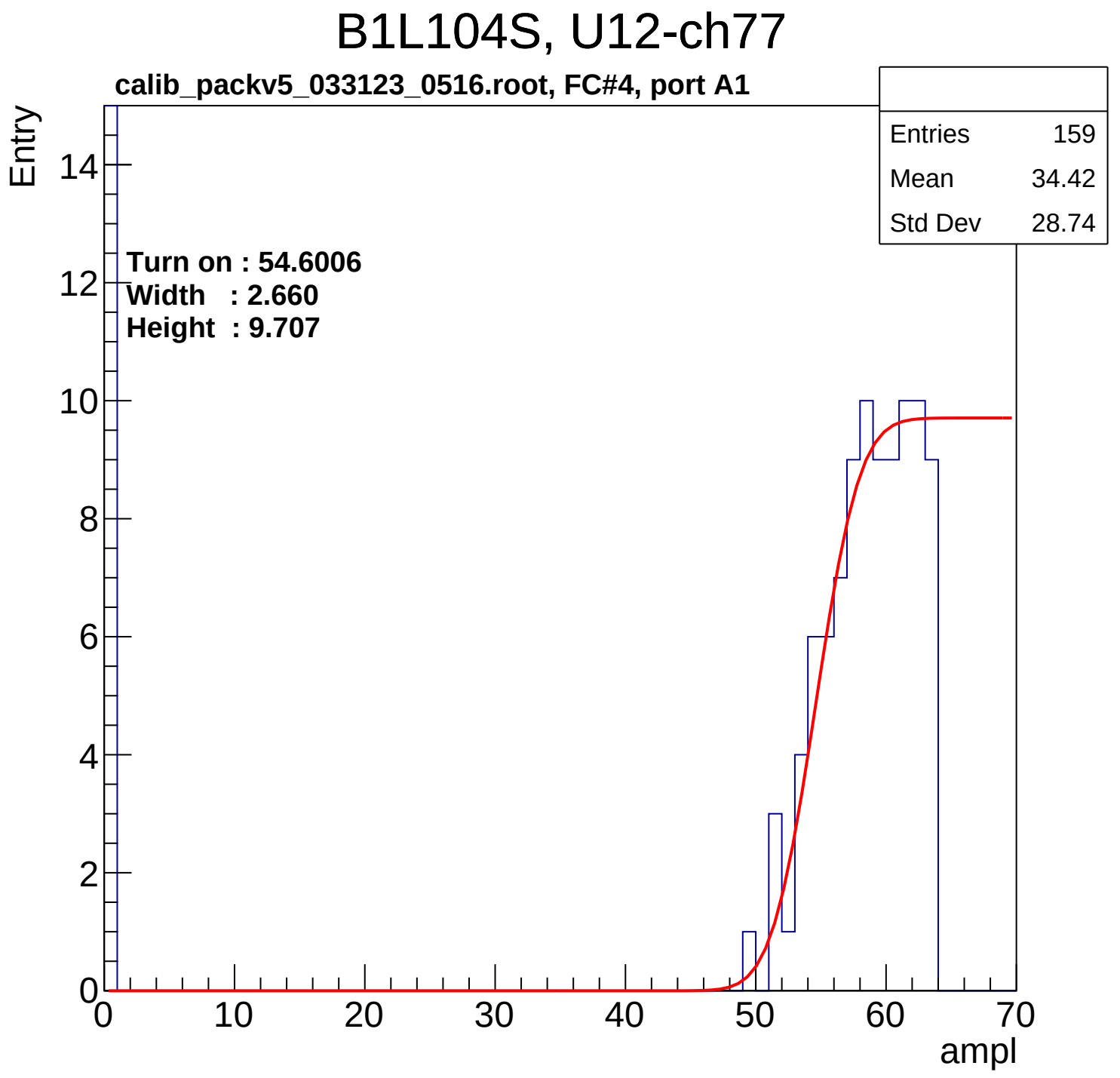
B1L104S, U12-ch77
calib_packv5_033123_0516.root, FC#4, port A1
Entries 159
Mean 34.42
Std Dev 28.74
Turn on : 54.6006
Width : 2.660
Height : 9.707
Entry
ampl
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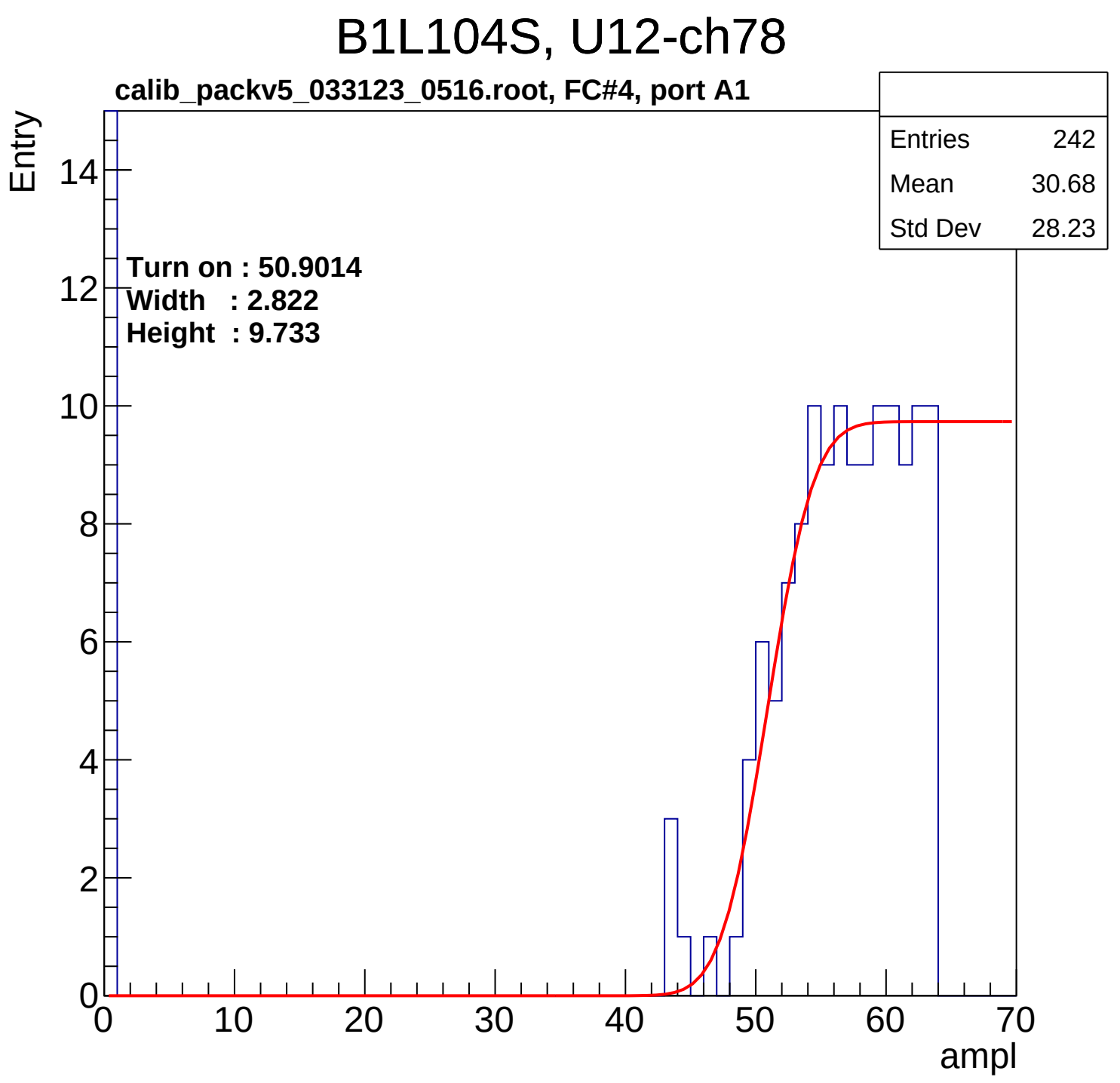
B1L104S, U12-ch78
calib_packv5_033123_0516.root, FC#4, port A1
Entries 242
Mean 30.68
Std Dev 28.23
Turn on : 50.9014
Width : 2.822
Height : 9.733
Entry
ampl
0
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4
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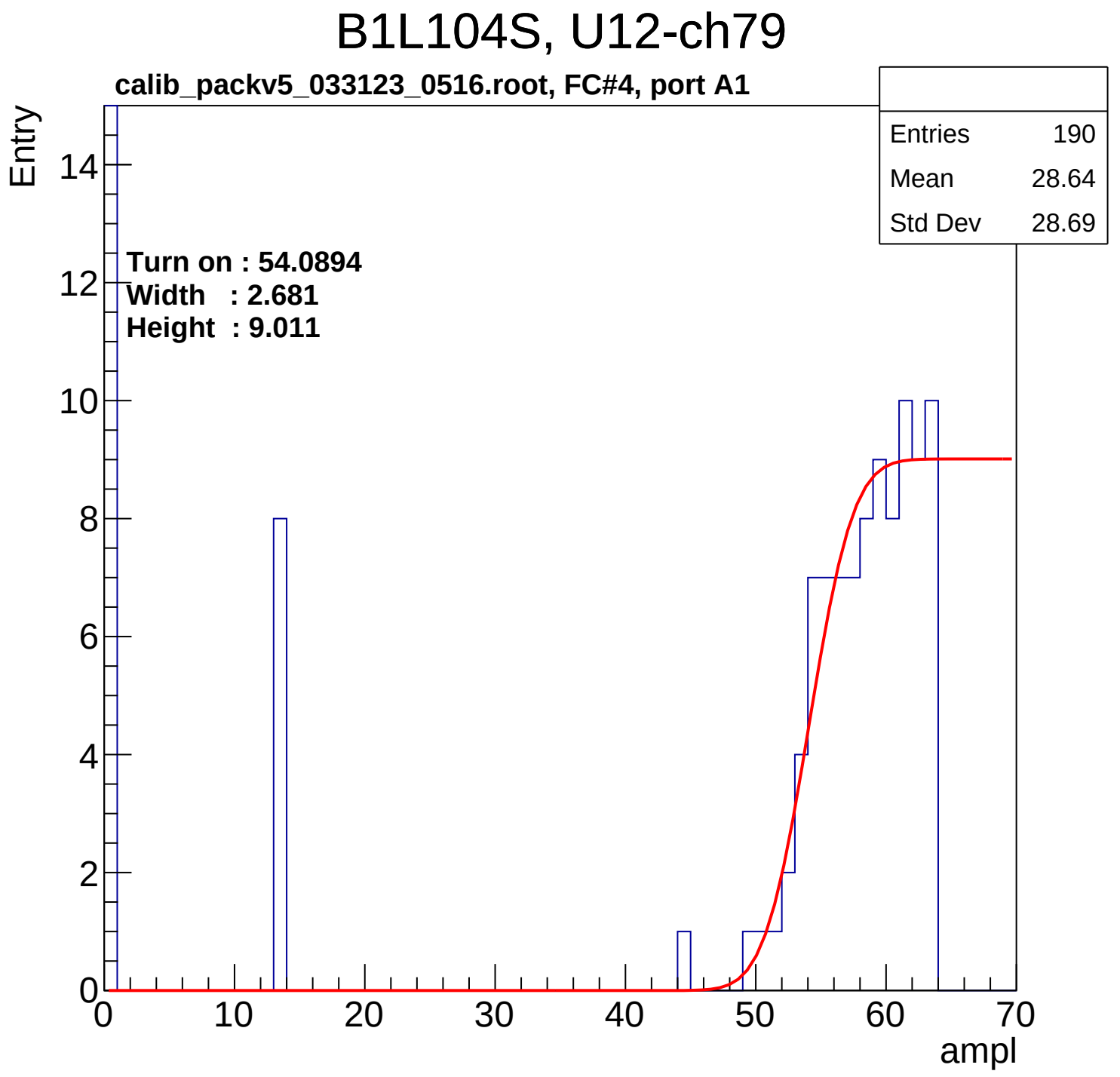
B1L104S, U12-ch79
calib_packv5_033123_0516.root, FC#4, port A1
Entries 190
Mean 28.64
Std Dev 28.69
Turn on : 54.0894
Width : 2.681
Height : 9.011
Entry
ampl
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8
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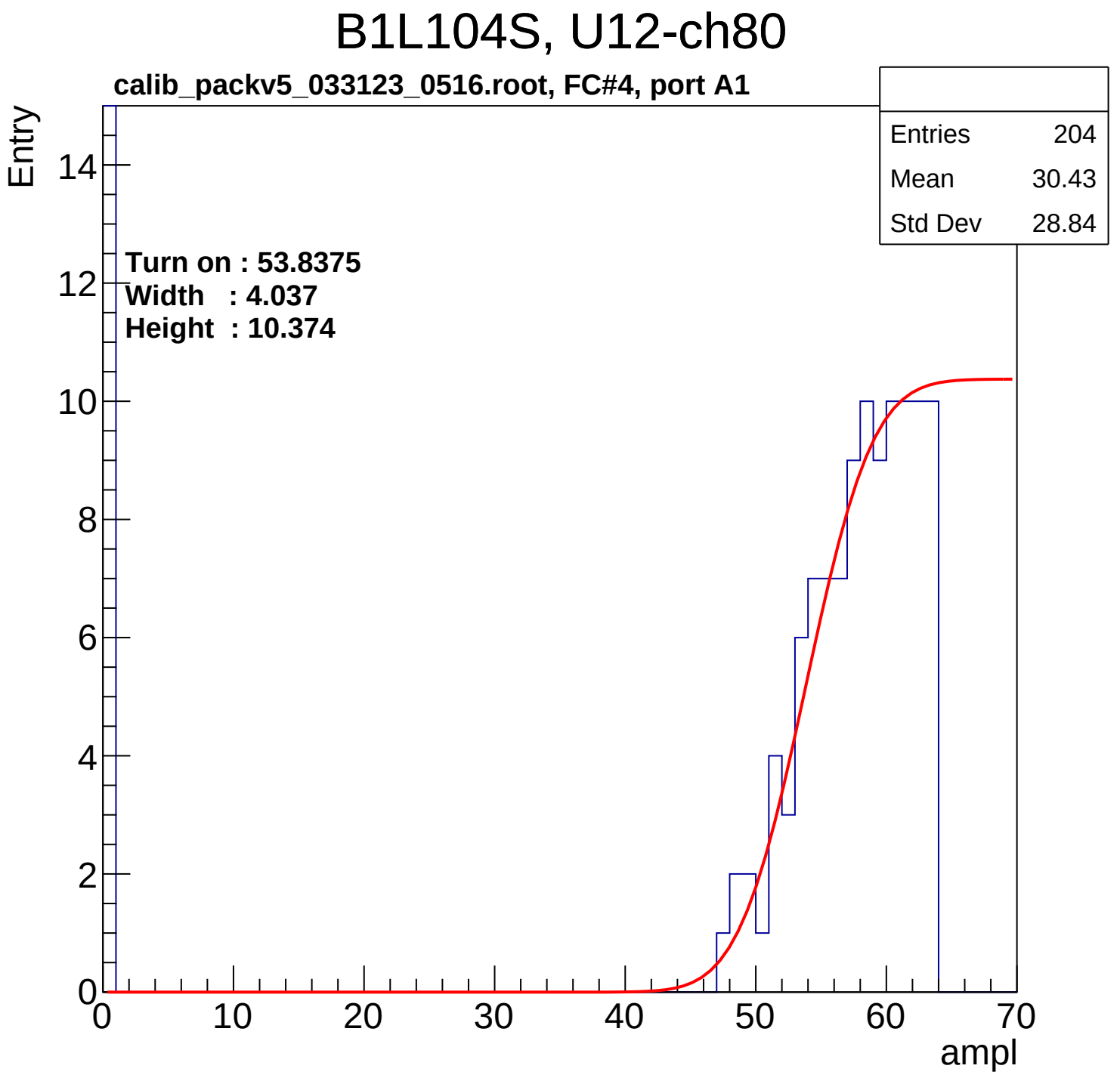
B1L104S, U12-ch80
calib_packv5_033123_0516.root, FC#4, port A1
Entries 204
Mean 30.43
Std Dev 28.84
Turn on : 53.8375
Width : 4.037
Height : 10.374
Entry
ampl
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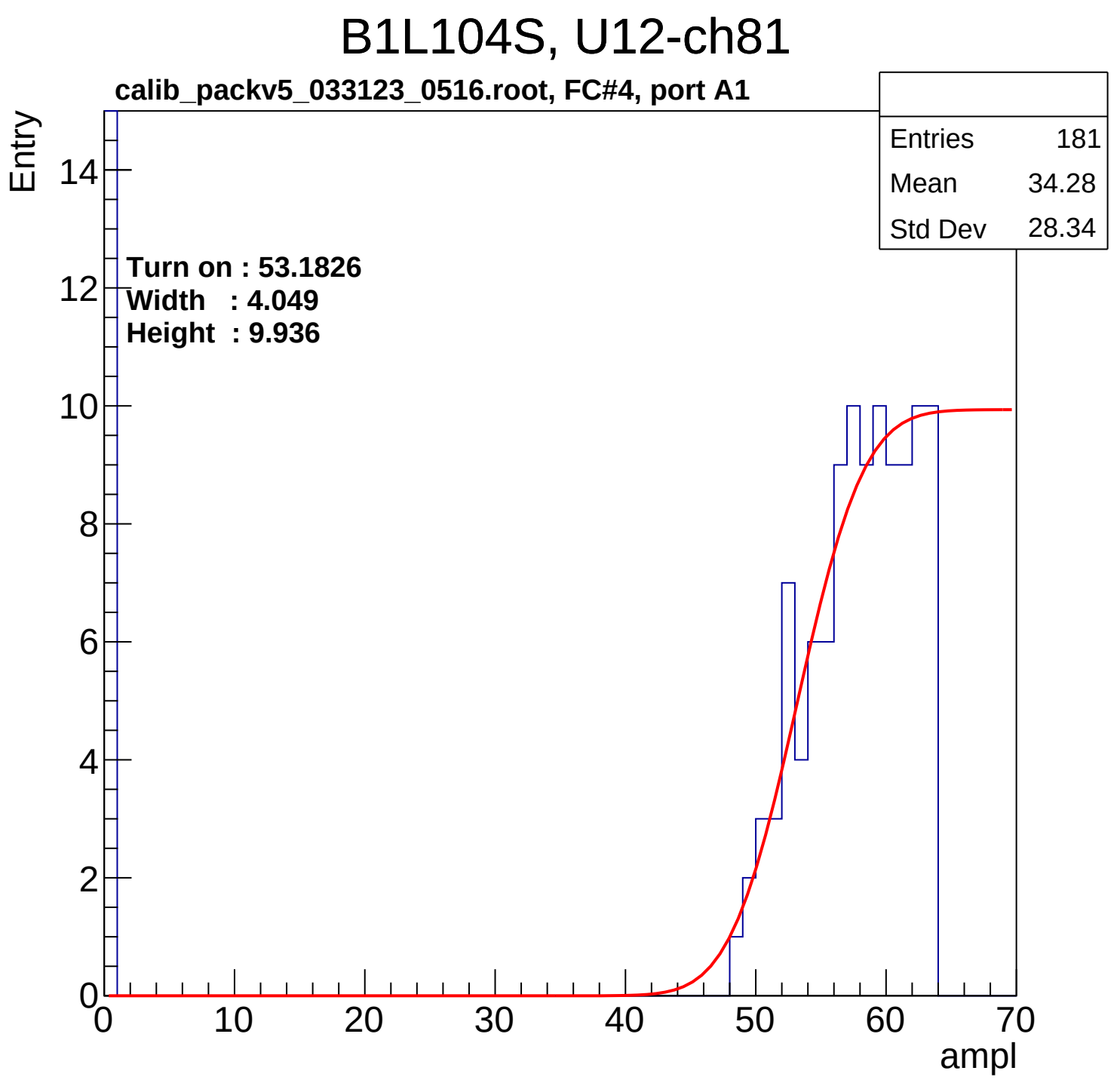
B1L104S, U12-ch81
calib_packv5_033123_0516.root, FC#4, port A1
Entries 181
Mean 34.28
Std Dev 28.34
Turn on : 53.1826
Width : 4.049
Height : 9.936
Entry
ampl
0
2
4
6
8
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0
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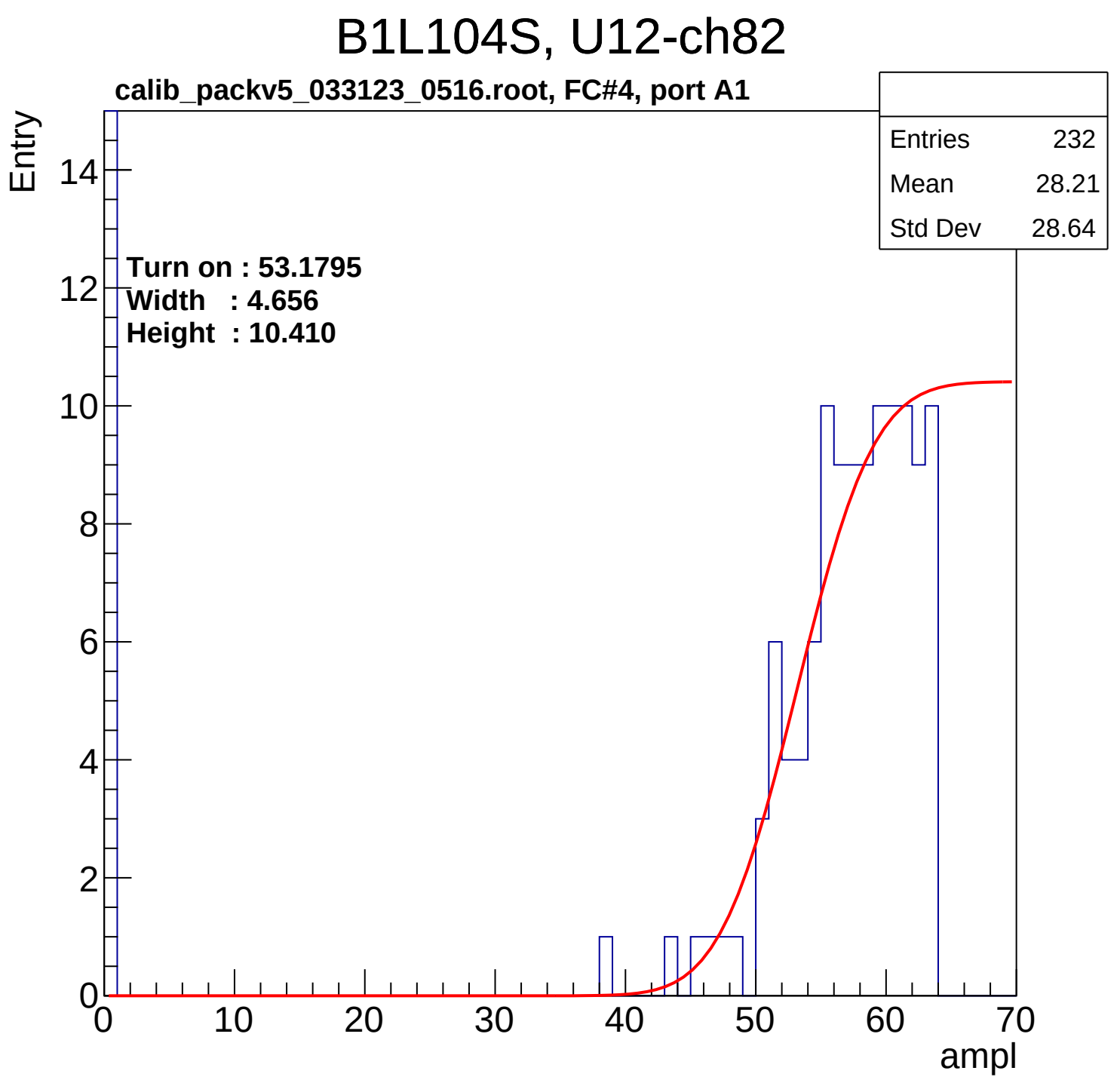
B1L104S, U12-ch82
calib_packv5_033123_0516.root, FC#4, port A1
Entries 232
Mean 28.21
Std Dev 28.64
Turn on : 53.1795
Width : 4.656
Height : 10.410
Entry
ampl
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4
6
8
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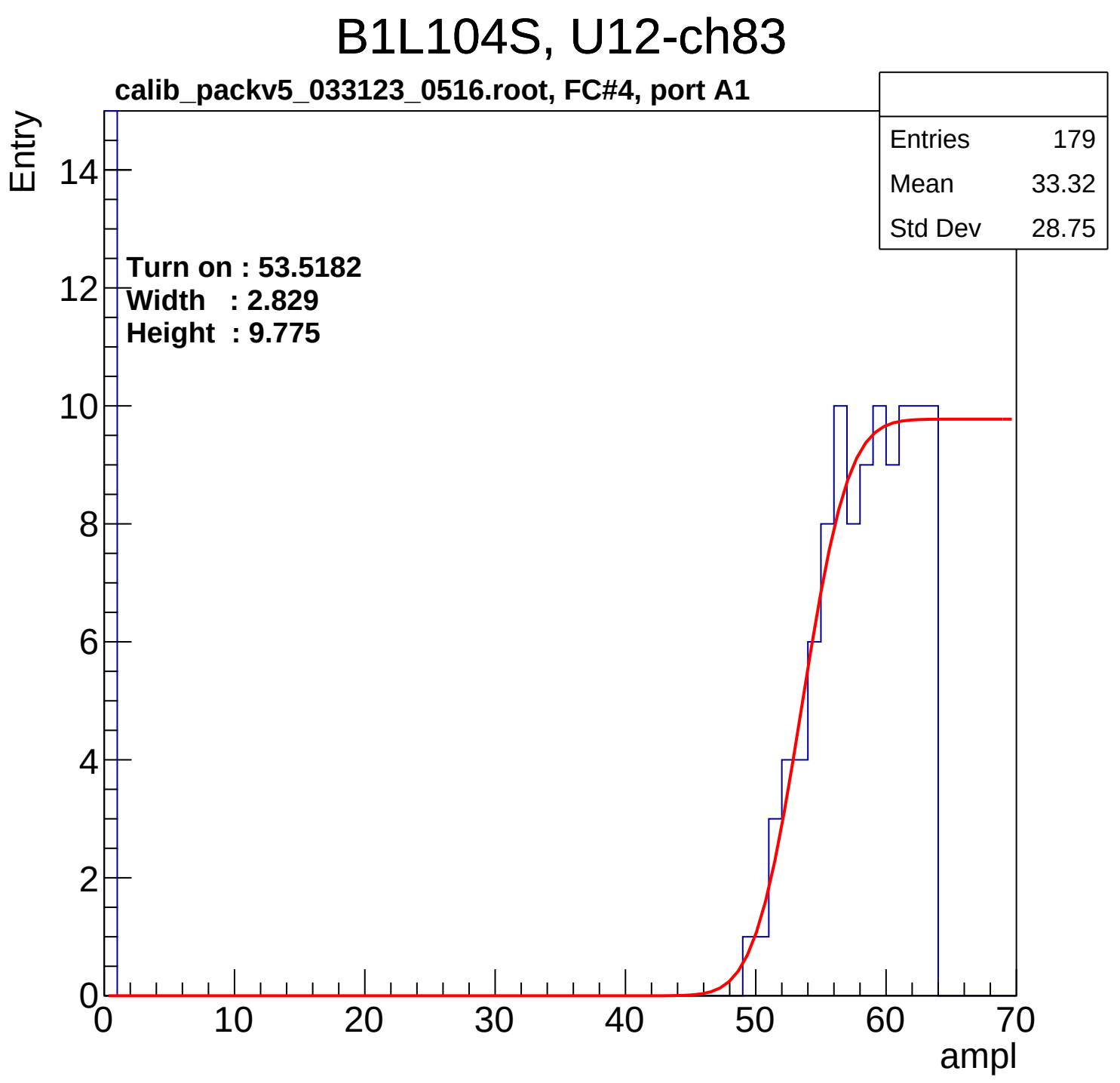
B1L104S, U12-ch83
calib_packv5_033123_0516.root, FC#4, port A1
Entries 179
Mean 33.32
Std Dev 28.75
Turn on : 53.5182
Width : 2.829
Height : 9.775
Entry
ampl
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6
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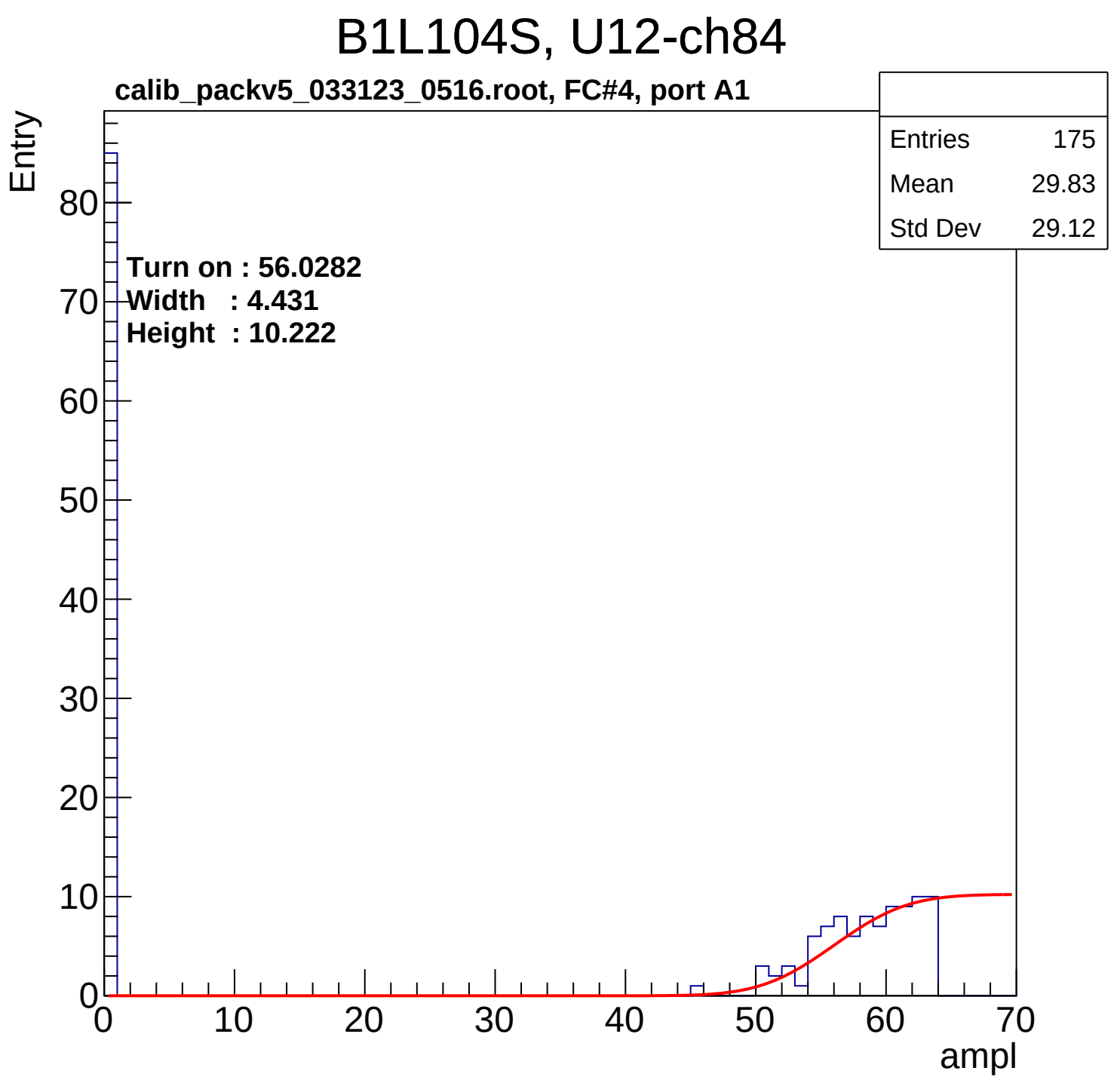
B1L104S, U12-ch84
calib_packv5_033123_0516.root, FC#4, port A1
Entries 175
Mean 29.83
Std Dev 29.12
Turn on : 56.0282
Width : 4.431
Height : 10.222
Entry
ampl
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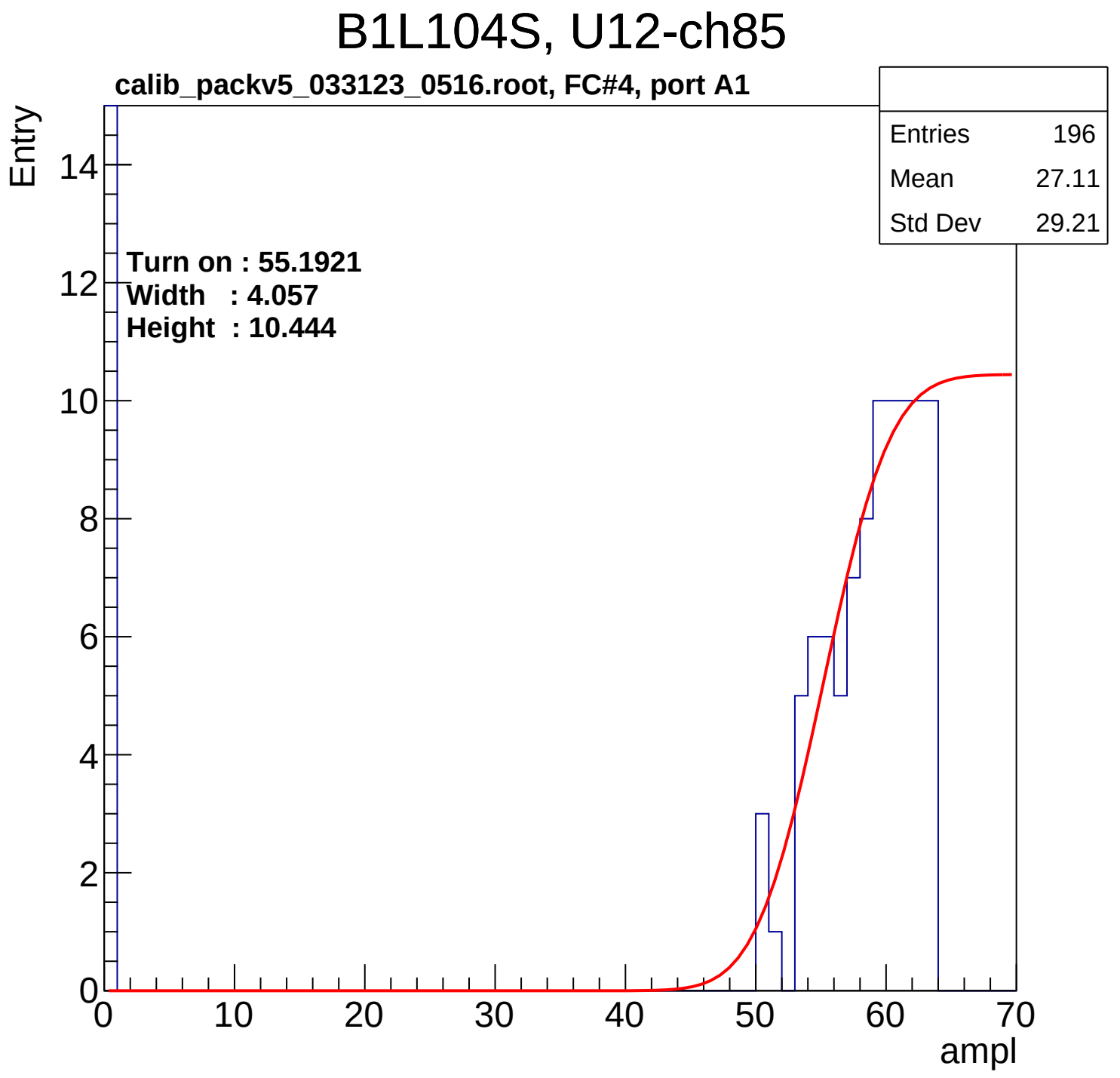
B1L104S, U12-ch85
calib_packv5_033123_0516.root, FC#4, port A1
Entries 196
Mean 27.11
Std Dev 29.21
Turn on : 55.1921
Width : 4.057
Height : 10.444
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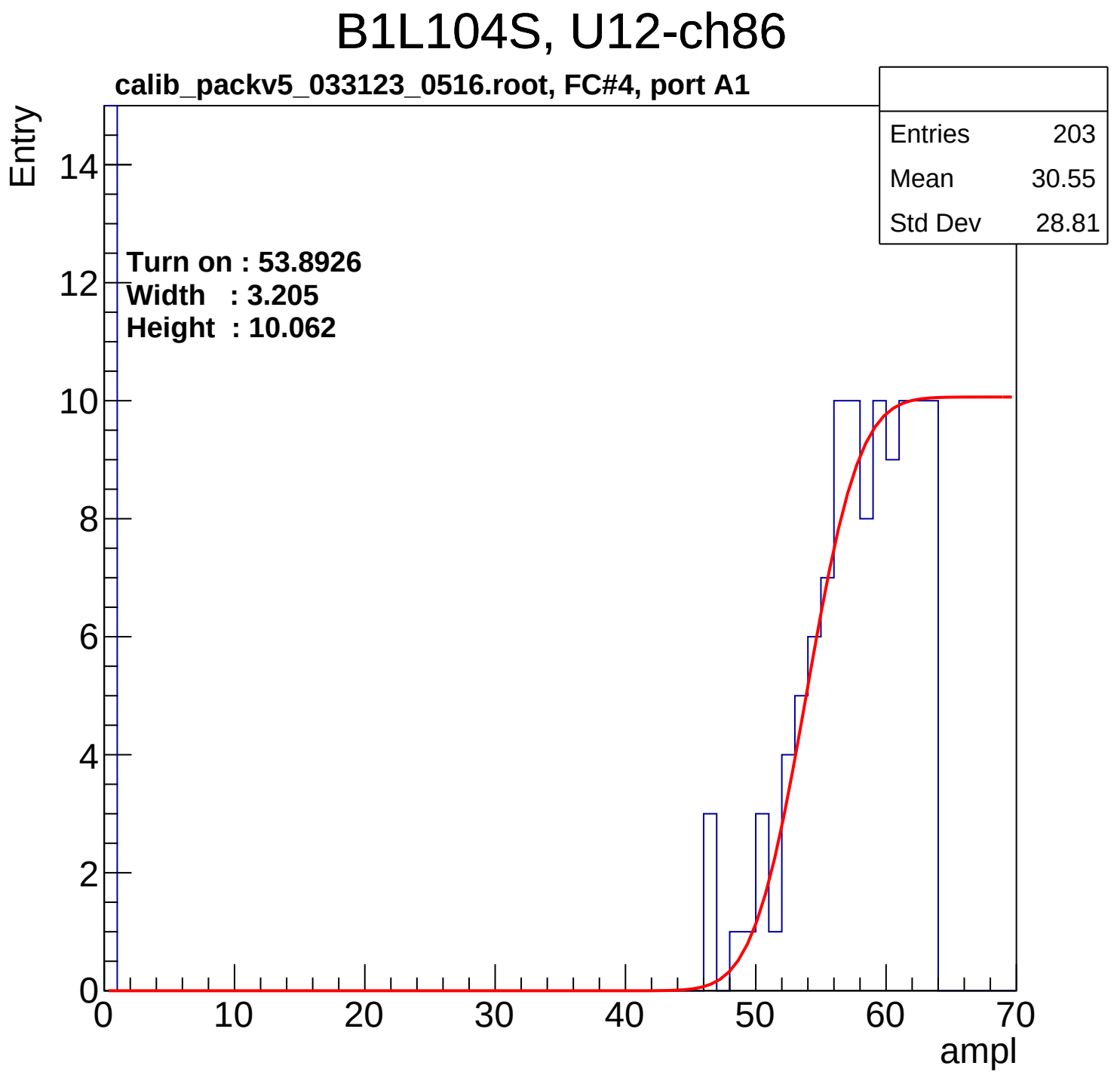
B1L104S, U12-ch86
calib_packv5_033123_0516.root, FC#4, port A1
Entries 203
Mean 30.55
Std Dev 28.81
Turn on : 53.8926
Width : 3.205
Height : 10.062
Entry
ampl
0
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4
6
8
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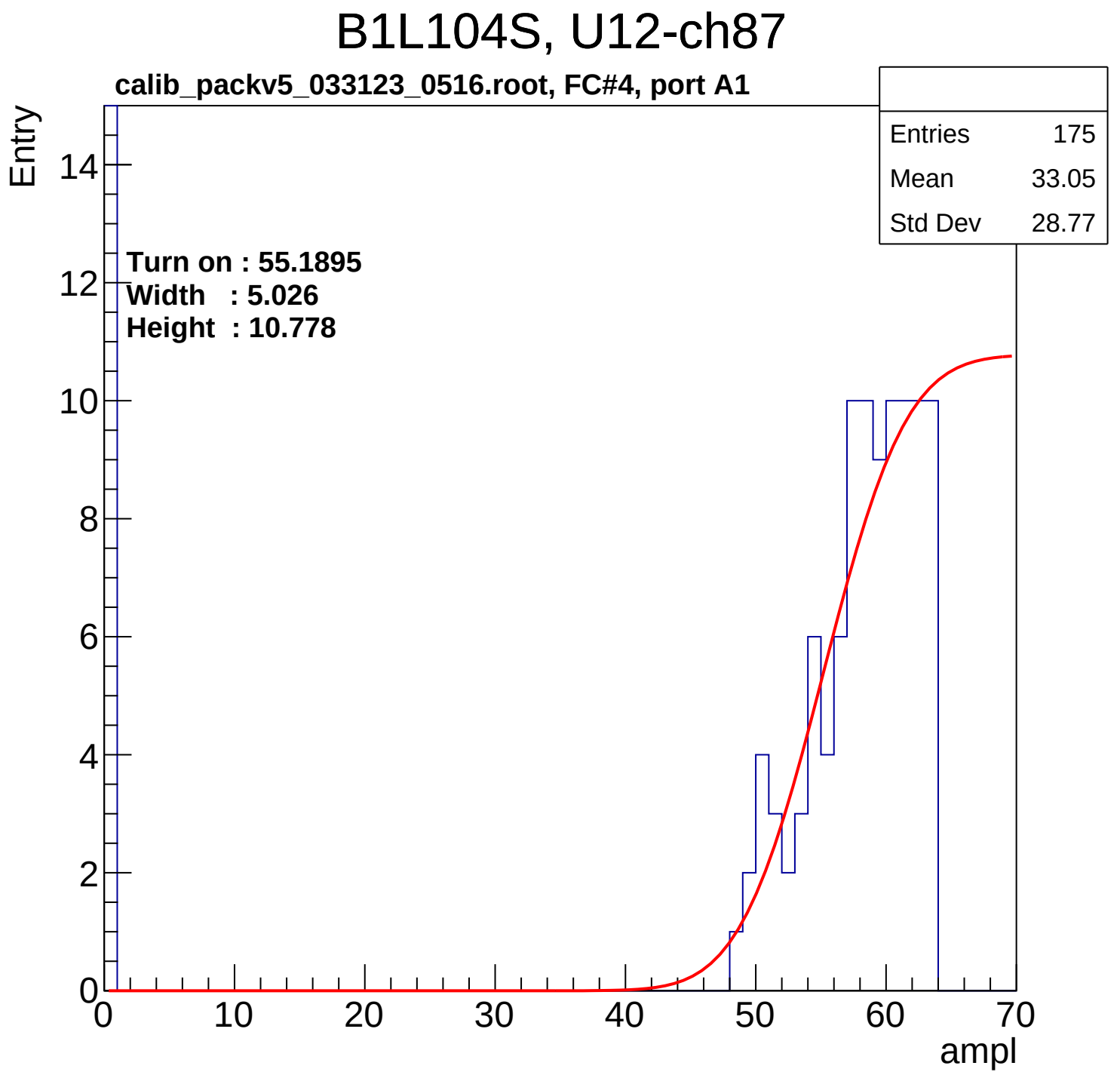
B1L104S, U12-ch87
calib_packv5_033123_0516.root, FC#4, port A1
Entries 175
Mean 33.05
Std Dev 28.77
Turn on : 55.1895
Width : 5.026
Height : 10.778
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ampl
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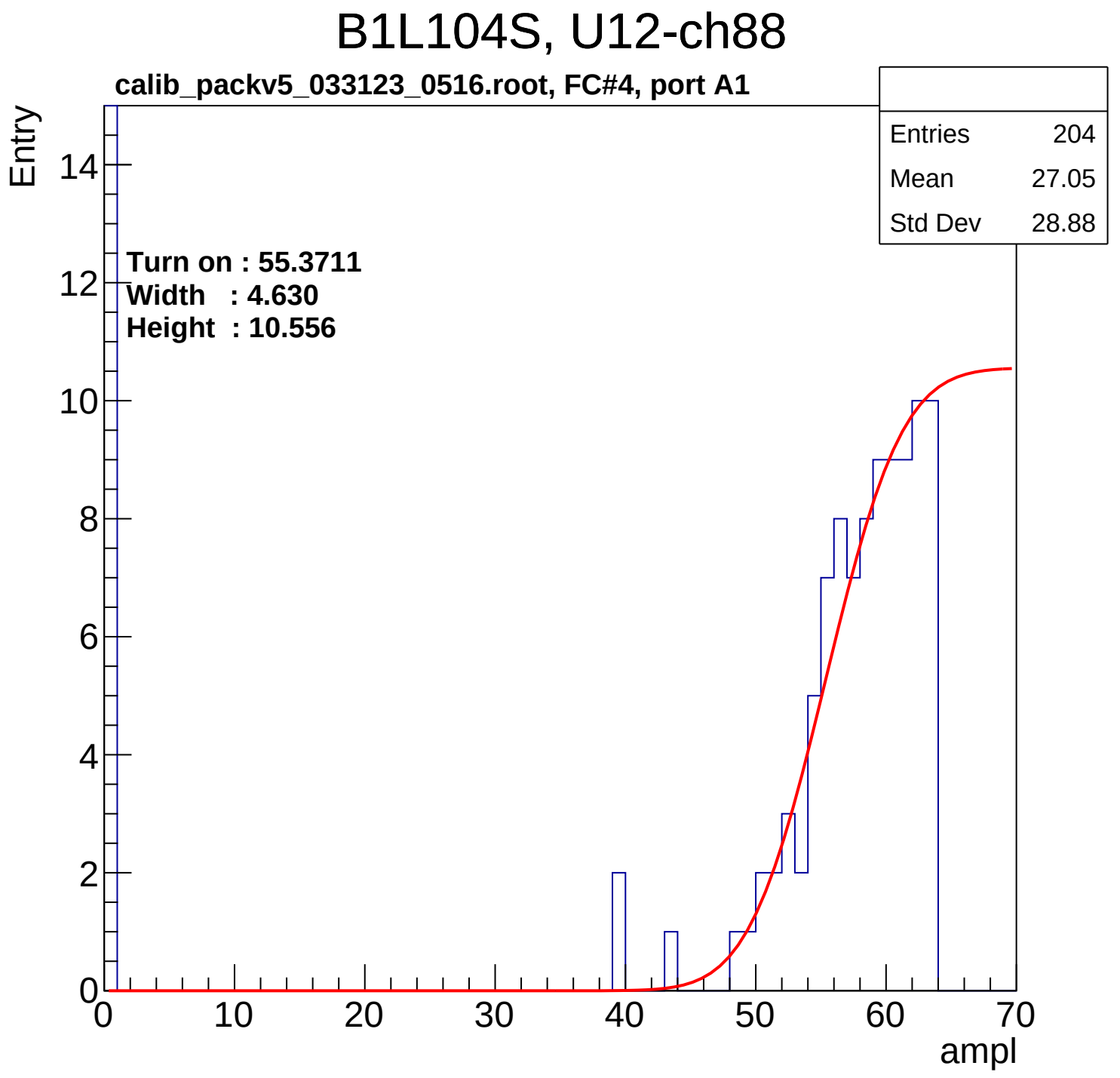
B1L104S, U12-ch88
calib_packv5_033123_0516.root, FC#4, port A1
Entries 204
Mean 27.05
Std Dev 28.88
Turn on : 55.3711
Width : 4.630
Height : 10.556
Entry
ampl
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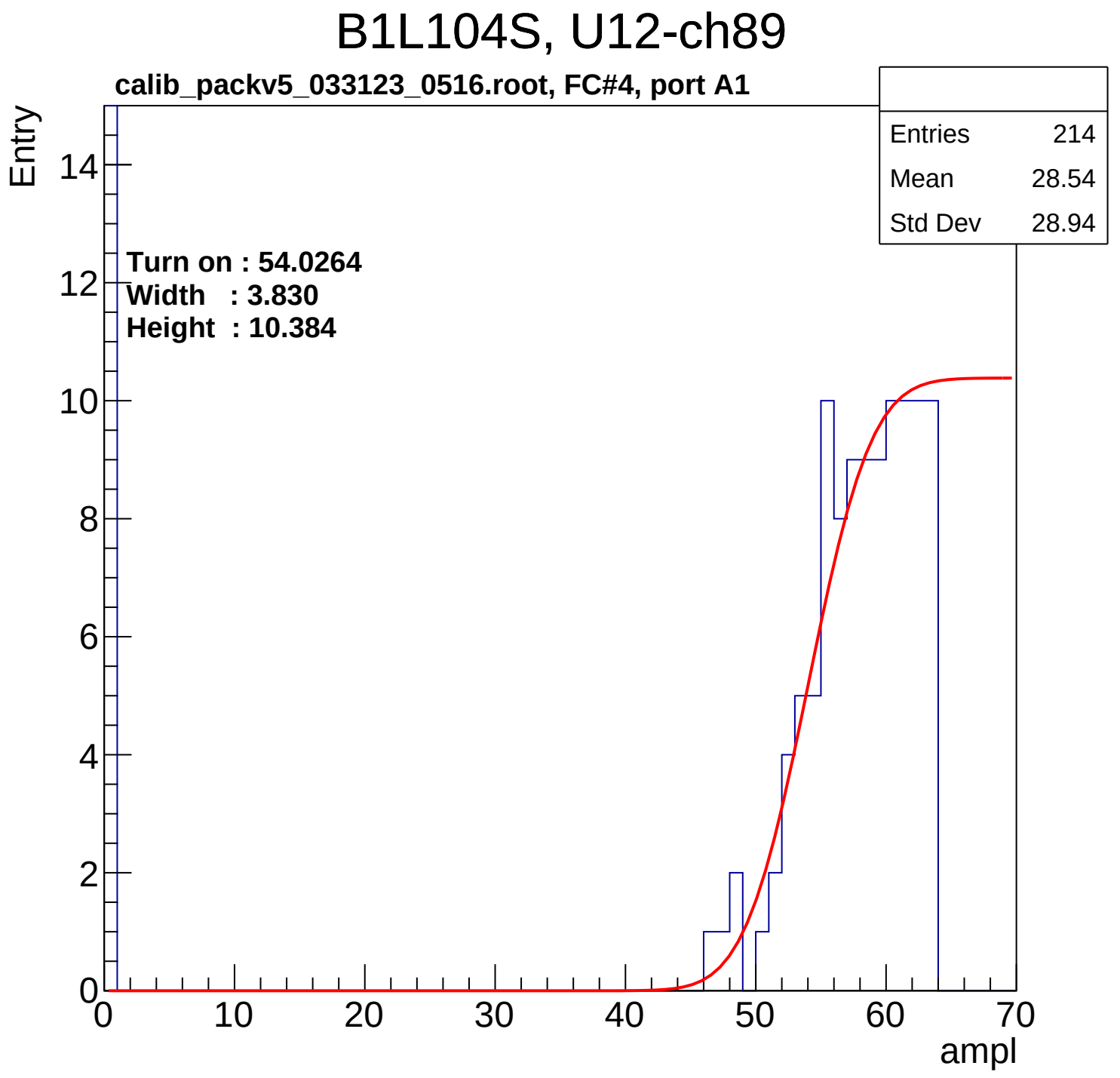
B1L104S, U12-ch89
calib_packv5_033123_0516.root, FC#4, port A1
Entries 214
Mean 28.54
Std Dev 28.94
Turn on : 54.0264
Width : 3.830
Height : 10.384
Entry
ampl
0
2
4
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8
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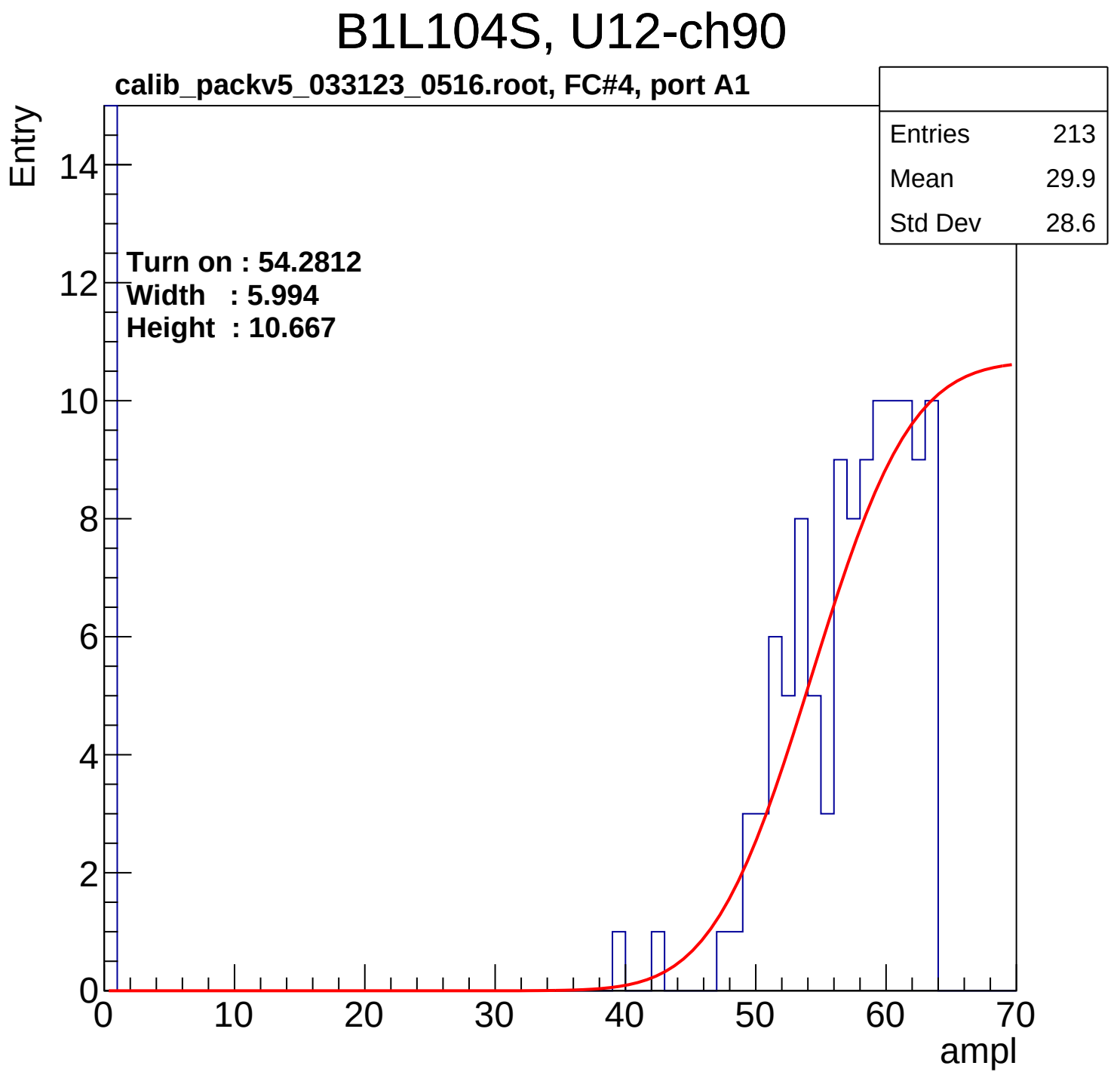
B1L104S, U12-ch90
calib_packv5_033123_0516.root, FC#4, port A1
Entries 213
Mean 29.9
Std Dev 28.6
Turn on : 54.2812
Width : 5.994
Height : 10.667
Entry
ampl
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2
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8
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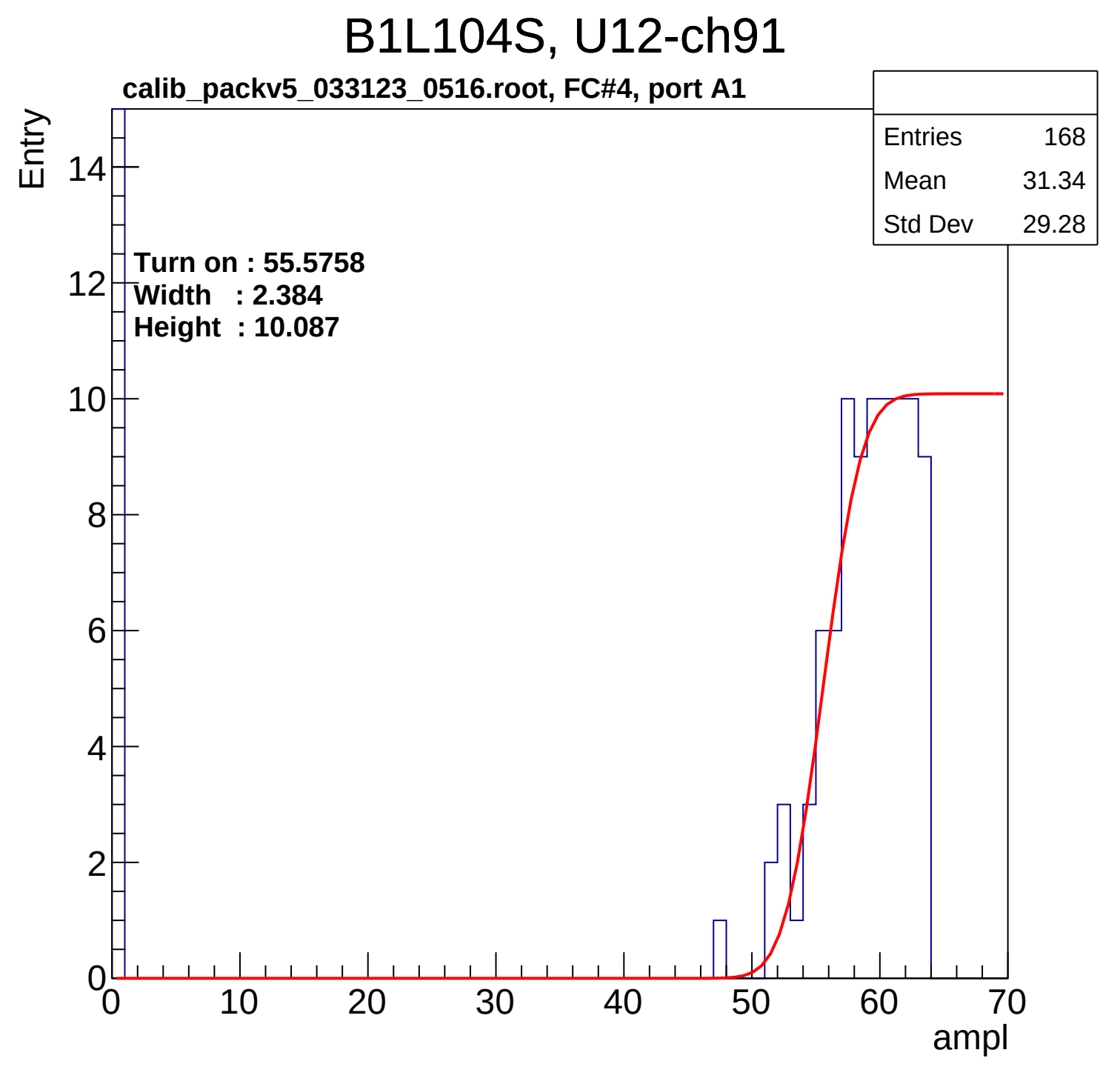
B1L104S, U12-ch91
calib_packv5_033123_0516.root, FC#4, port A1
Entries 168
Mean 31.34
Std Dev 29.28
Turn on : 55.5758
Width : 2.384
Height : 10.087
Entry
ampl
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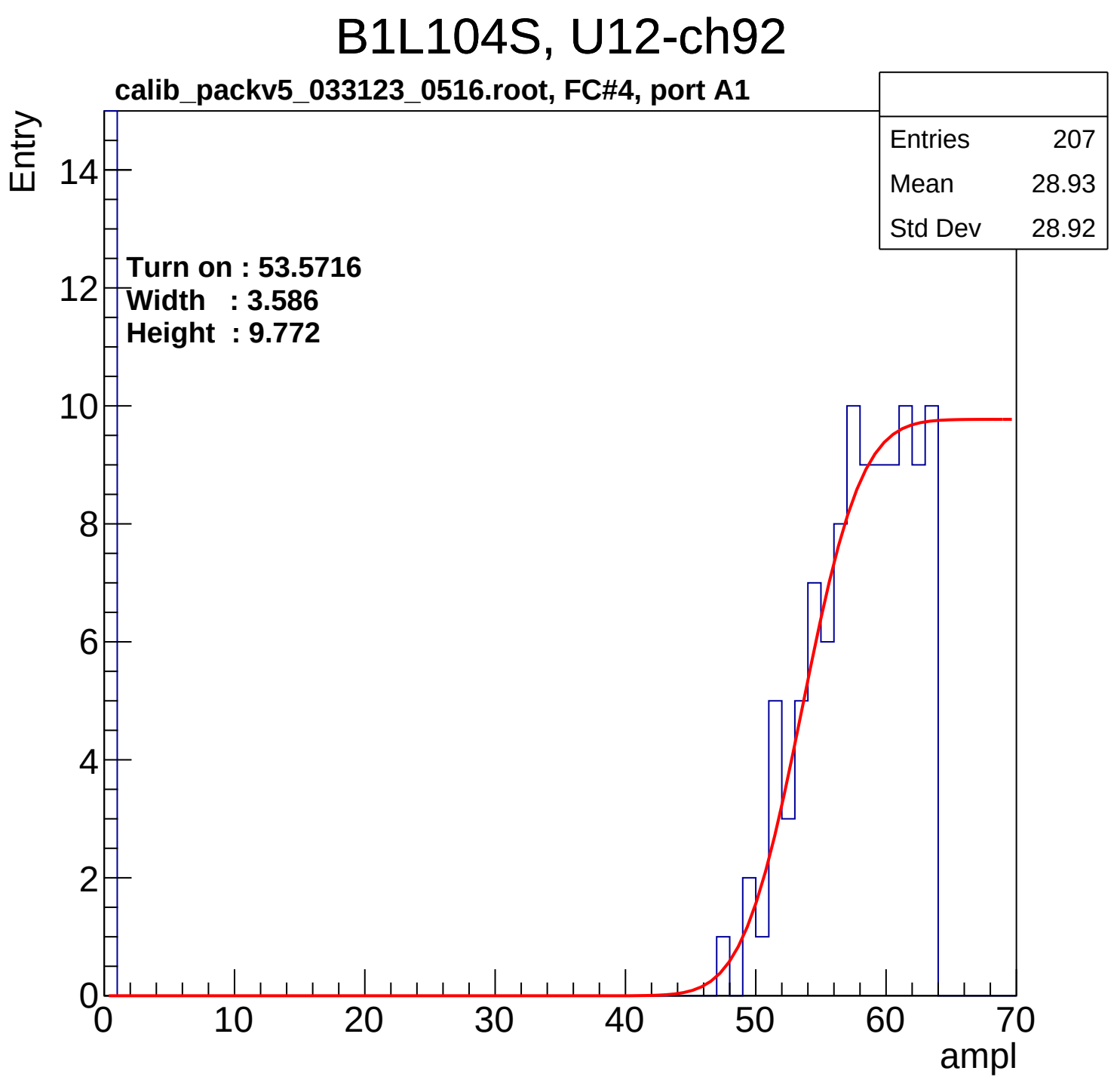
B1L104S, U12-ch92
calib_packv5_033123_0516.root, FC#4, port A1
Entries 207
Mean 28.93
Std Dev 28.92
Turn on : 53.5716
Width : 3.586
Height : 9.772
Entry
ampl
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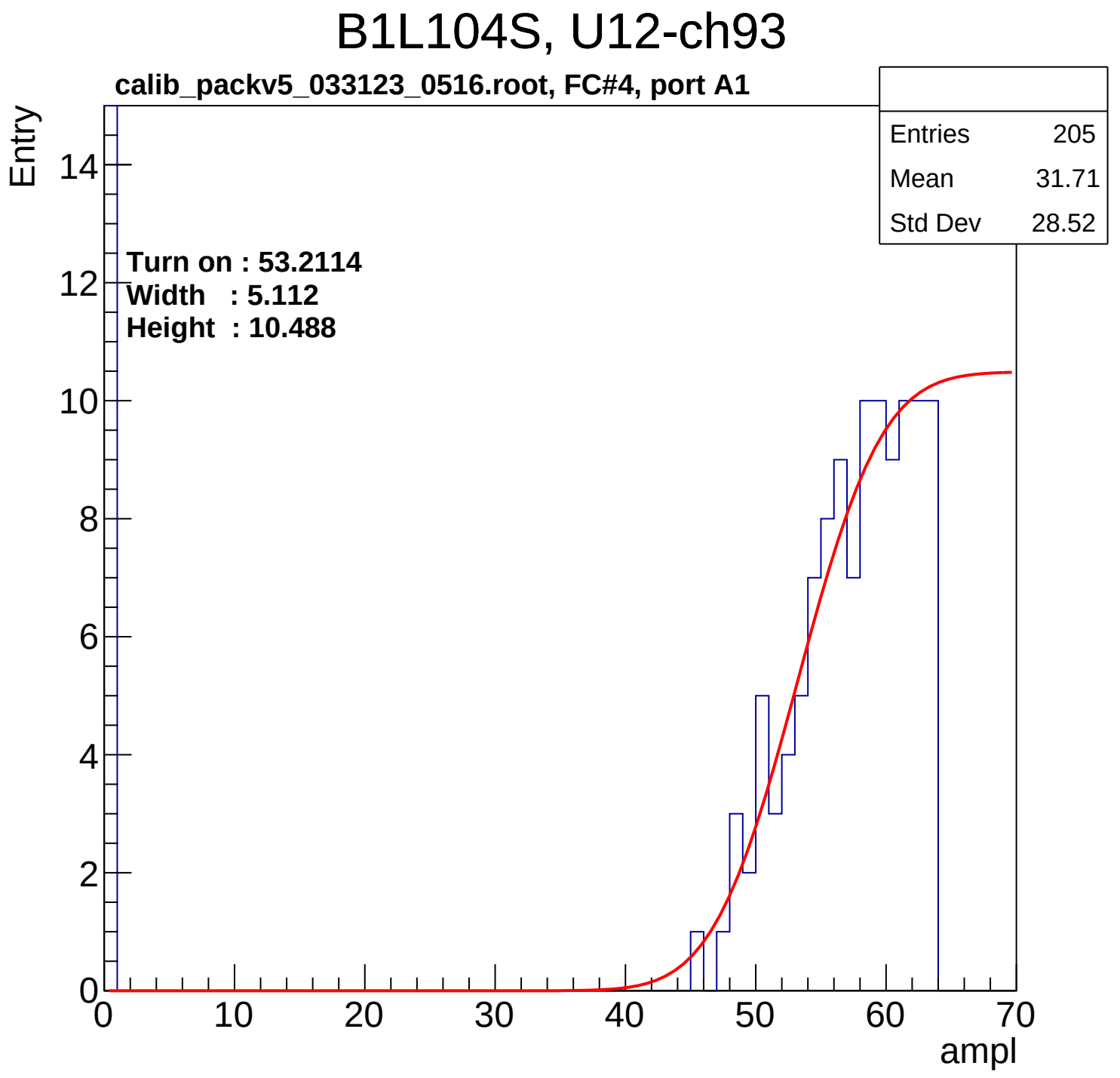
B1L104S, U12-ch93
calib_packv5_033123_0516.root, FC#4, port A1
Entries 205
Mean 31.71
Std Dev 28.52
Turn on : 53.2114
Width : 5.112
Height : 10.488
Entry
ampl
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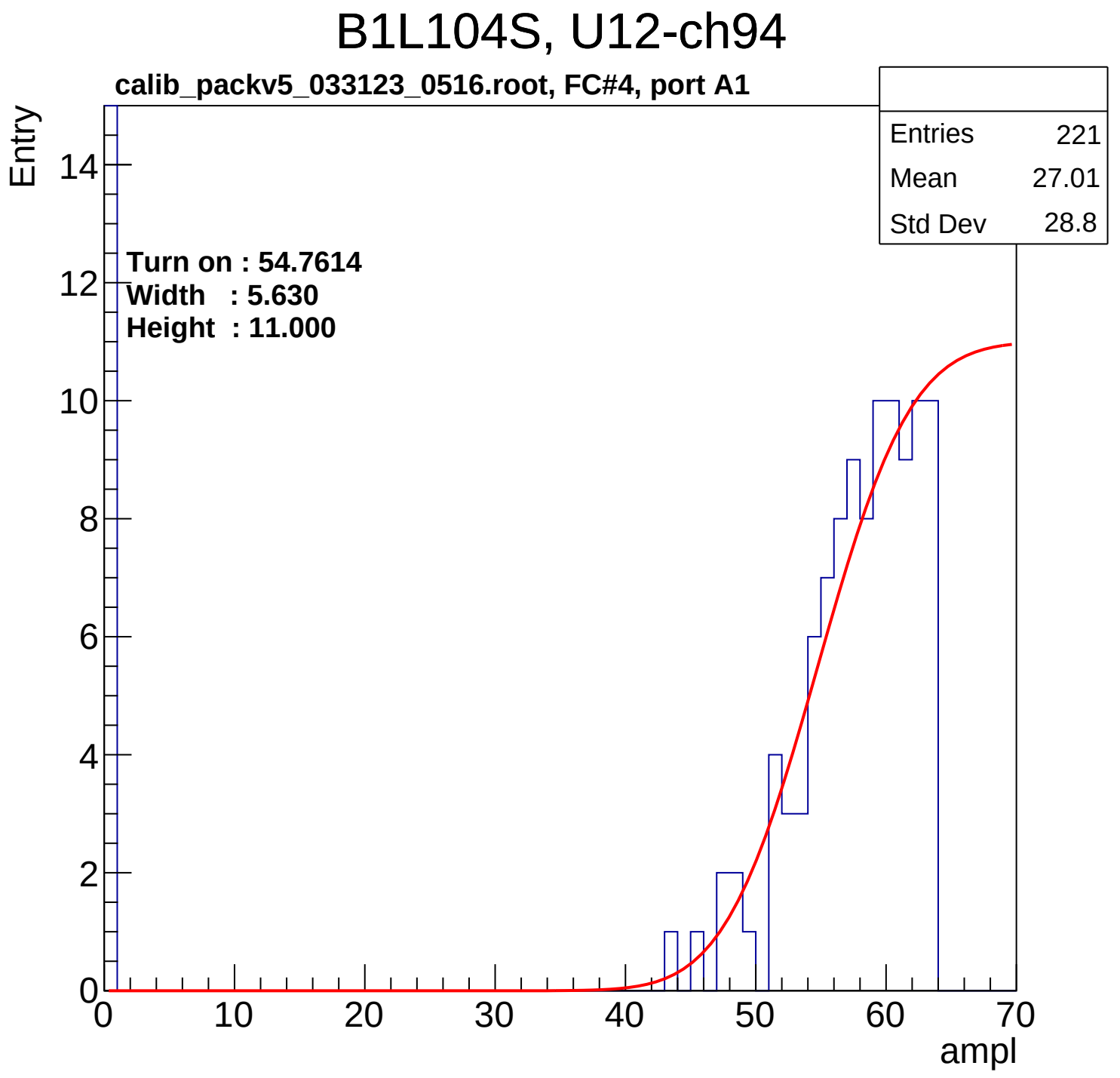
B1L104S, U12-ch94
calib_packv5_033123_0516.root, FC#4, port A1
Entries 221
Mean 27.01
Std Dev 28.8
Turn on : 54.7614
Width : 5.630
Height : 11.000
Entry
ampl
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6
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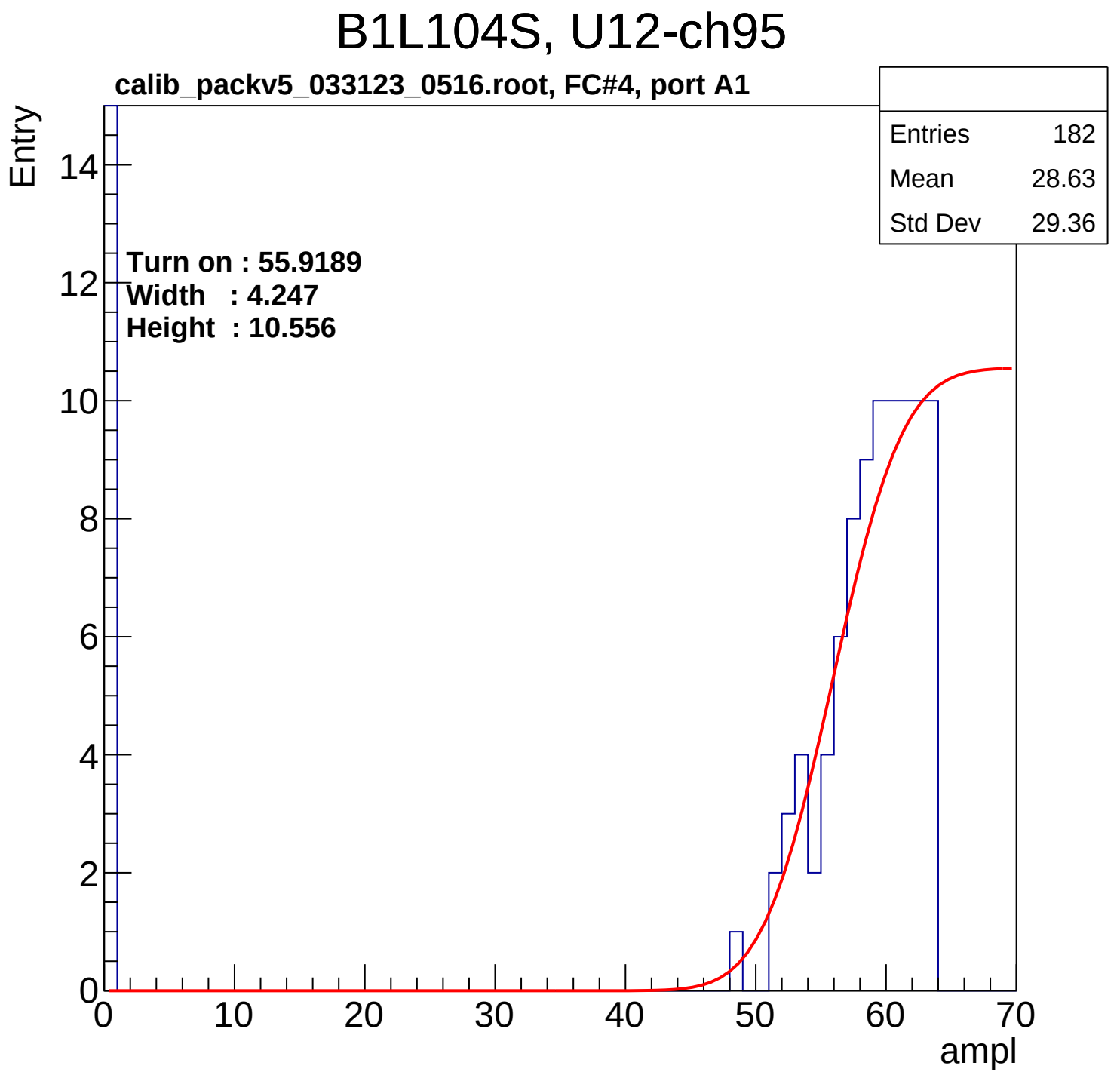
B1L104S, U12-ch95
calib_packv5_033123_0516.root, FC#4, port A1
Entries 182
Mean 28.63
Std Dev 29.36
Turn on : 55.9189
Width : 4.247
Height : 10.556
Entry
ampl
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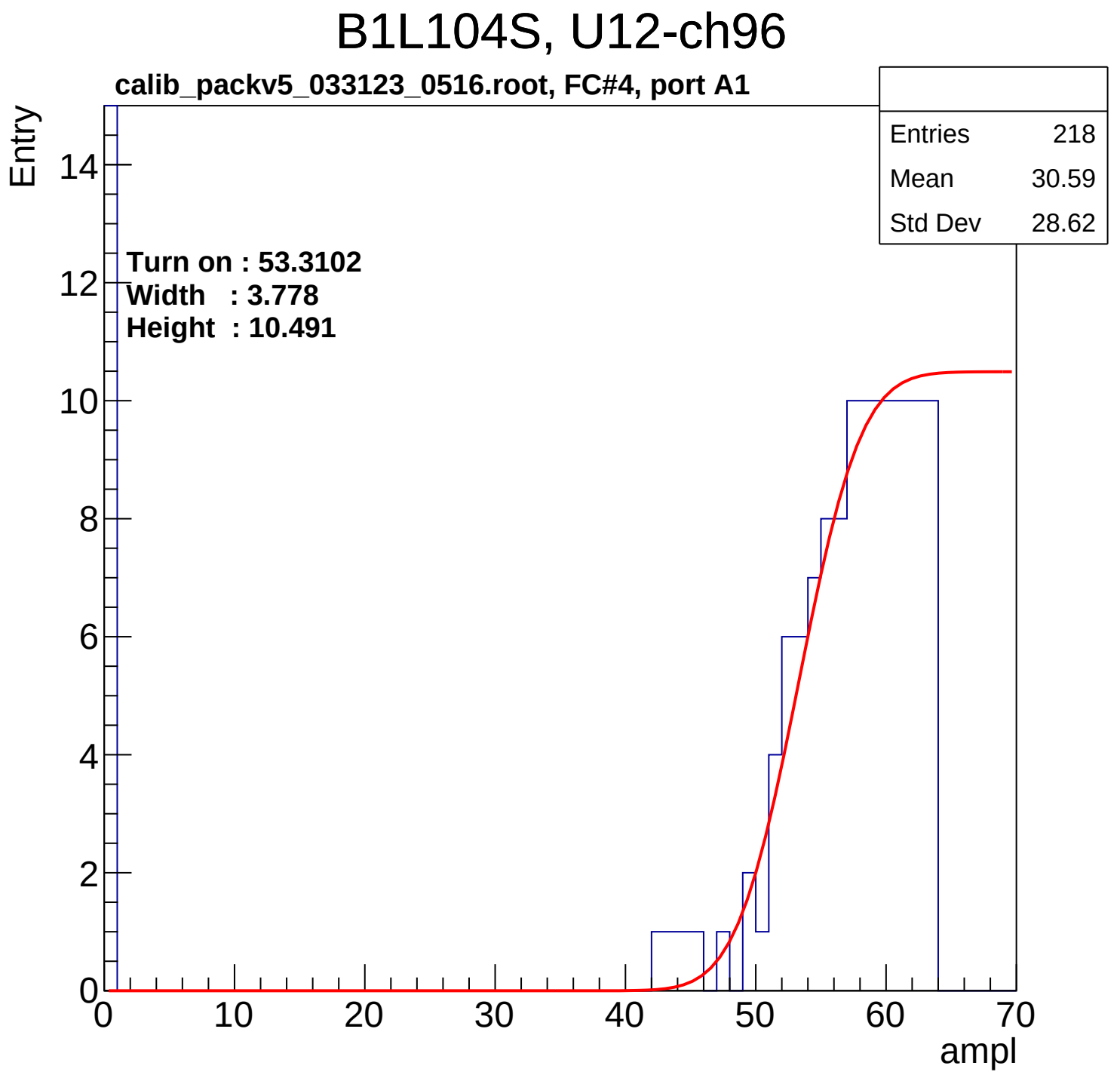
B1L104S, U12-ch96
calib_packv5_033123_0516.root, FC#4, port A1
Entries 218
Mean 30.59
Std Dev 28.62
Turn on : 53.3102
Width : 3.778
Height : 10.491
Entry
ampl
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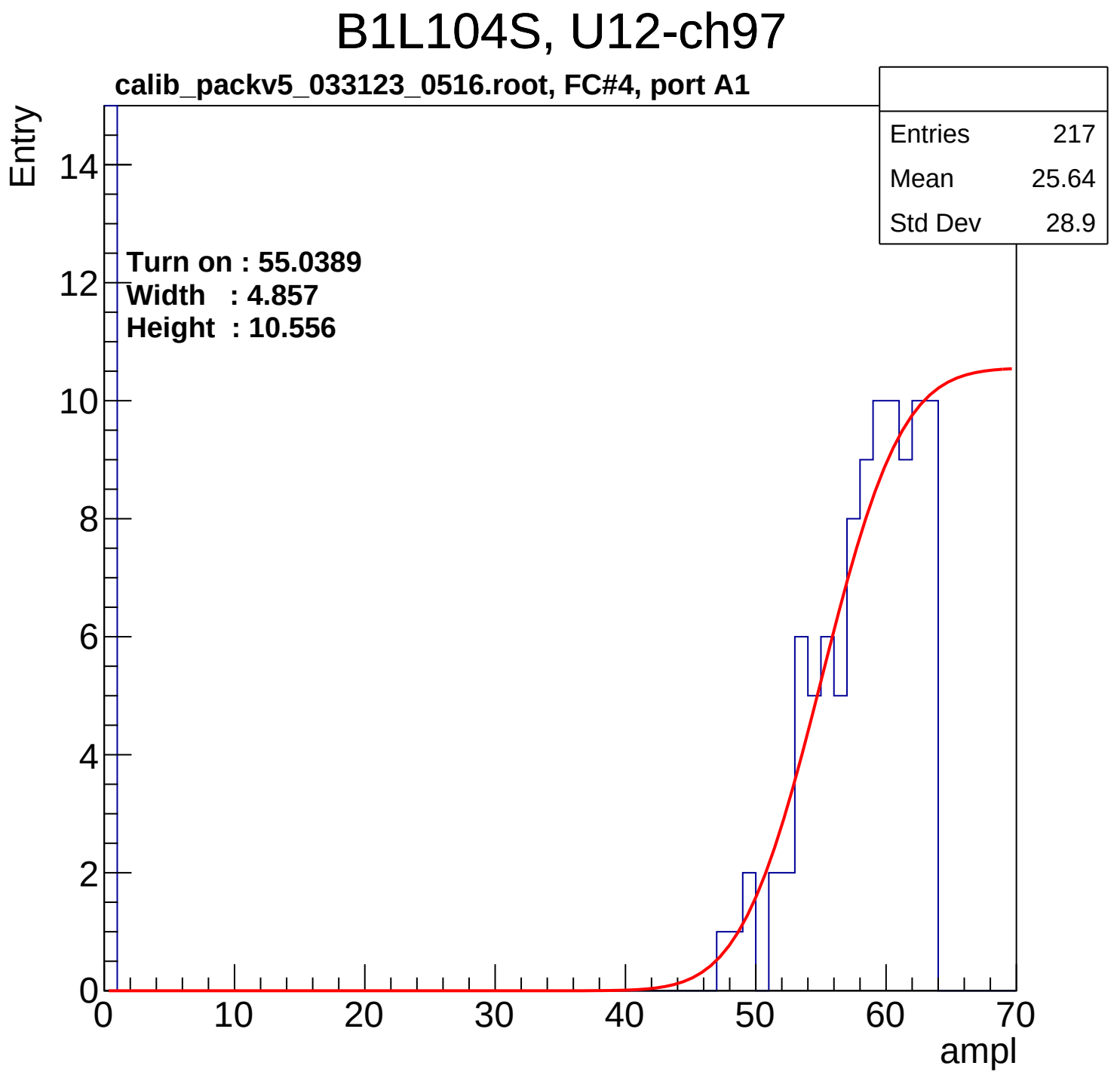
B1L104S, U12-ch97
calib_packv5_033123_0516.root, FC#4, port A1
Entries 217
Mean 25.64
Std Dev 28.9
Turn on : 55.0389
Width : 4.857
Height : 10.556
Entry
ampl
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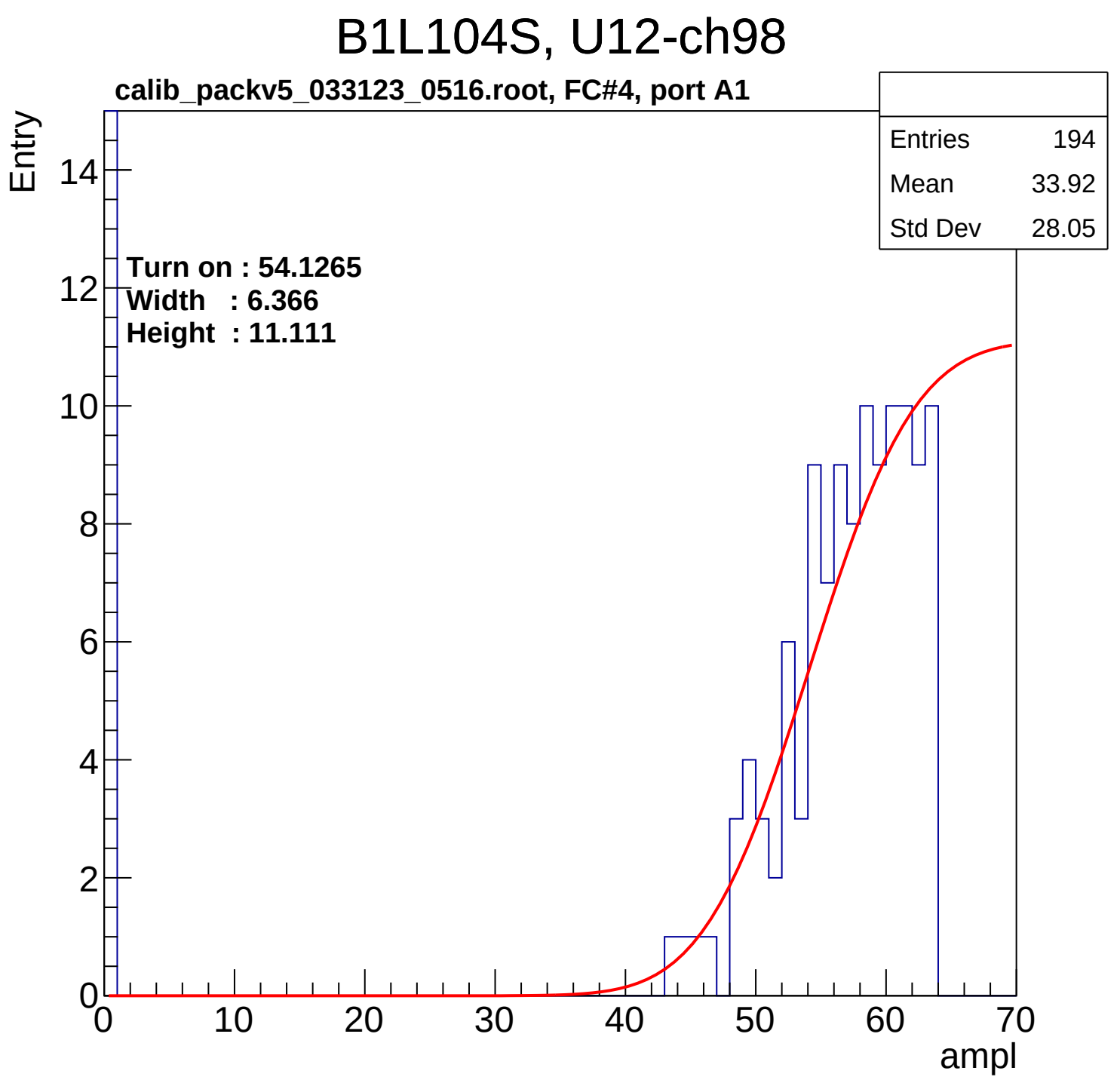
B1L104S, U12-ch98
calib_packv5_033123_0516.root, FC#4, port A1
Entries 194
Mean 33.92
Std Dev 28.05
Turn on : 54.1265
Width : 6.366
Height : 11.111
Entry
ampl
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2
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8
10
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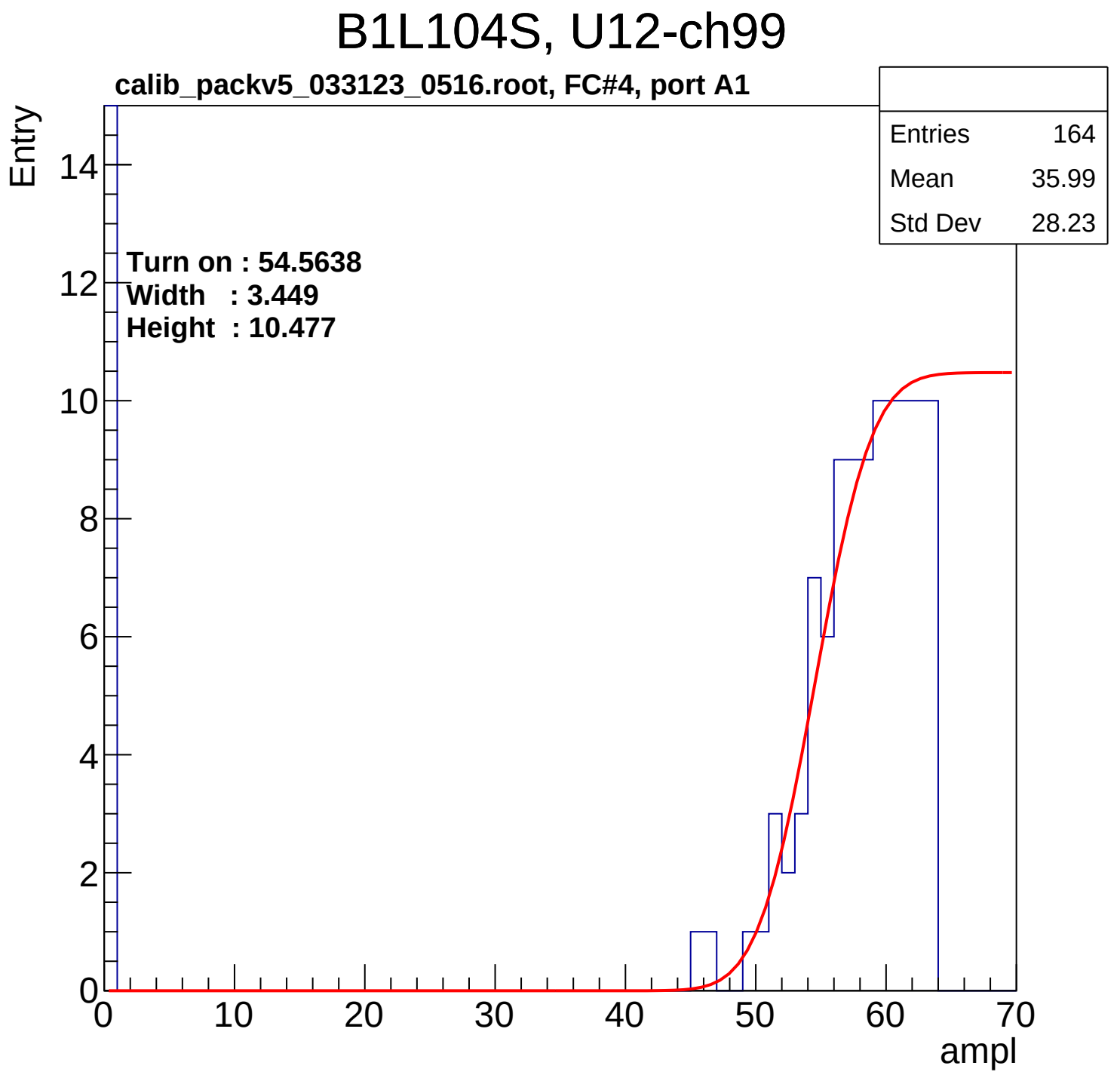
B1L104S, U12-ch99
calib_packv5_033123_0516.root, FC#4, port A1
Entries 164
Mean 35.99
Std Dev 28.23
Turn on : 54.5638
Width : 3.449
Height : 10.477
Entry
ampl
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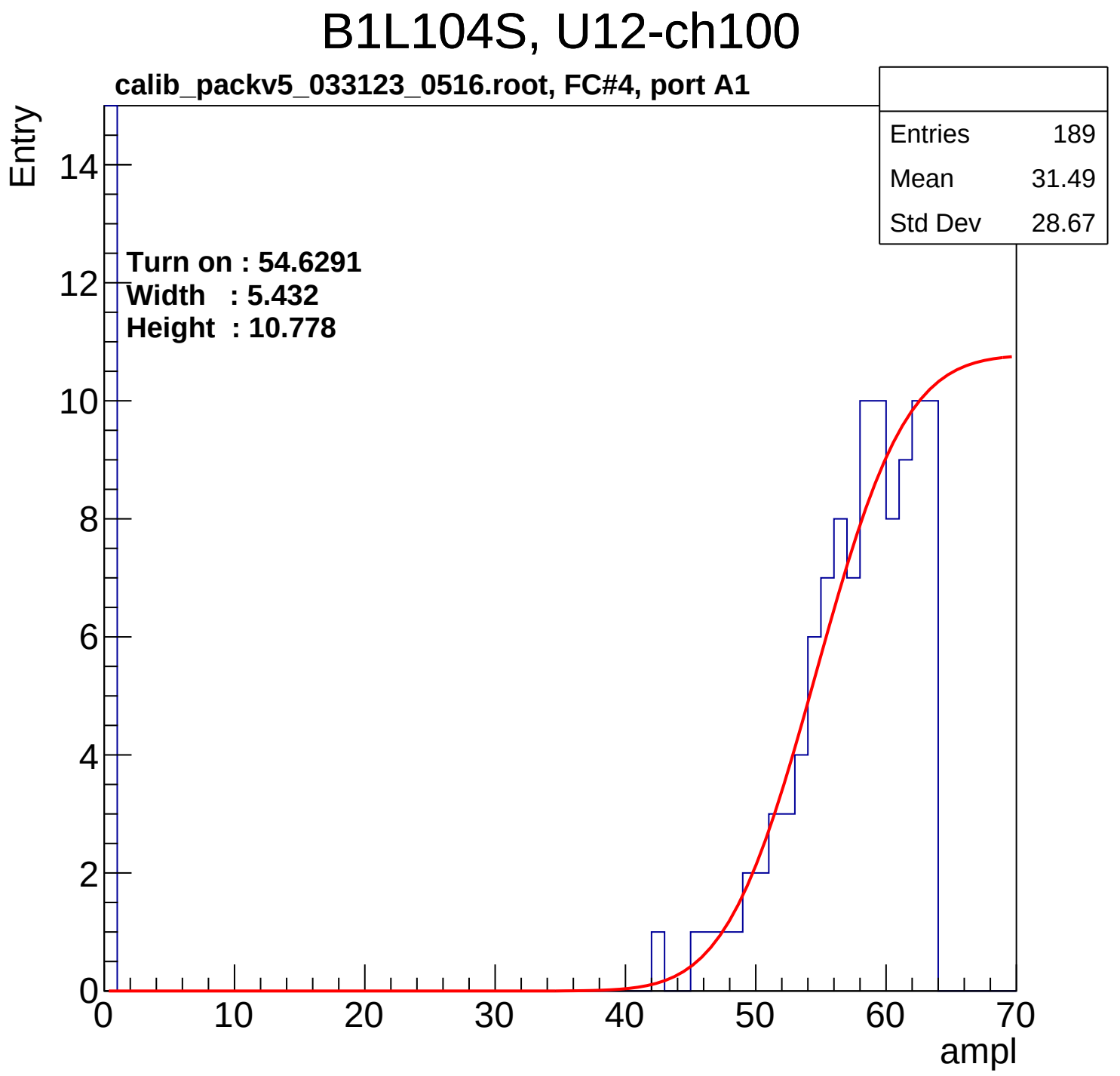
B1L104S, U12-ch100
calib_packv5_033123_0516.root, FC#4, port A1
Entries 189
Mean 31.49
Std Dev 28.67
Turn on : 54.6291
Width : 5.432
Height : 10.778
Entry
ampl
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6
8
10
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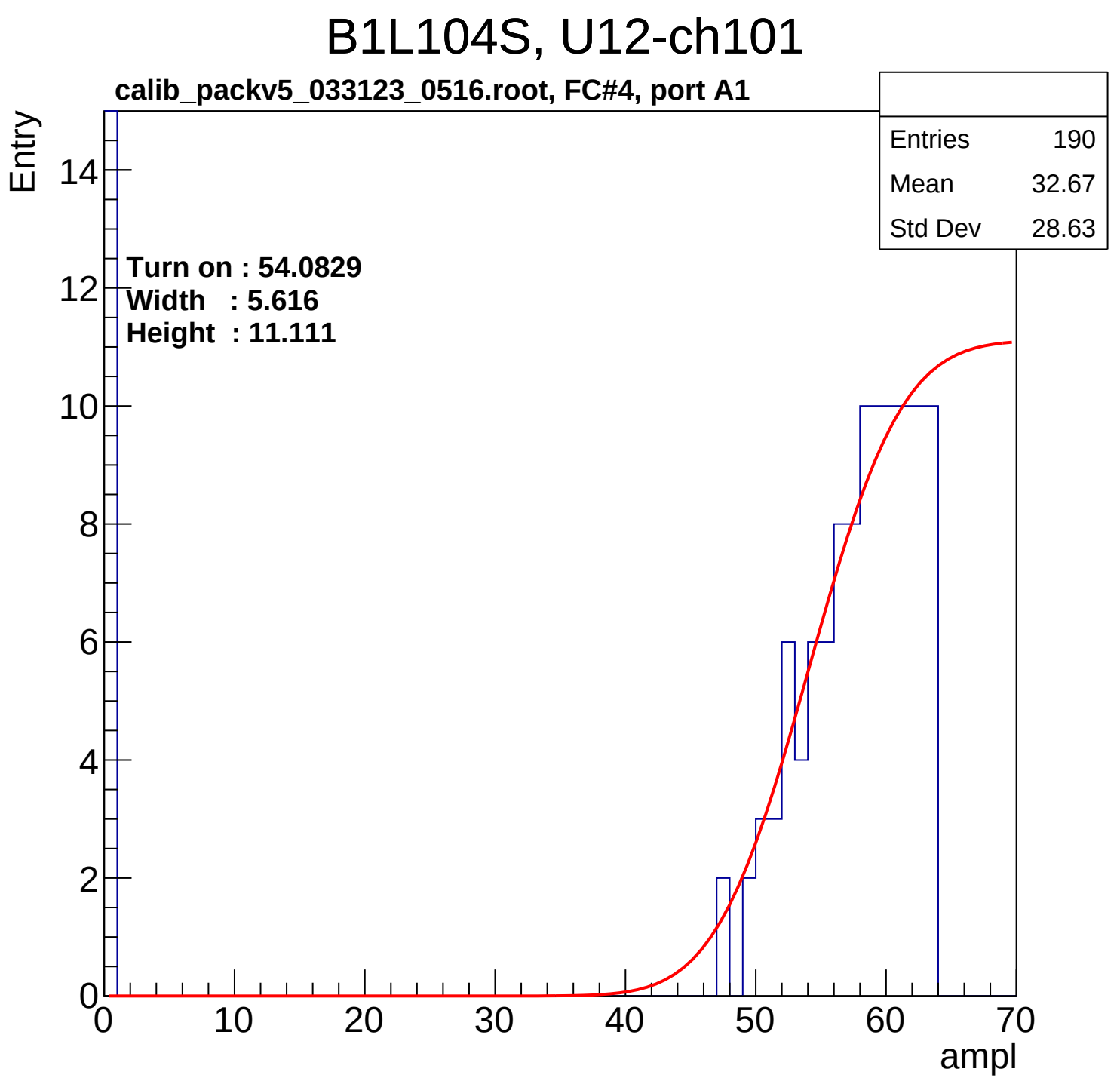
B1L104S, U12-ch101
calib_packv5_033123_0516.root, FC#4, port A1
Entries 190
Mean 32.67
Std Dev 28.63
Turn on : 54.0829
Width : 5.616
Height : 11.111
Entry
ampl
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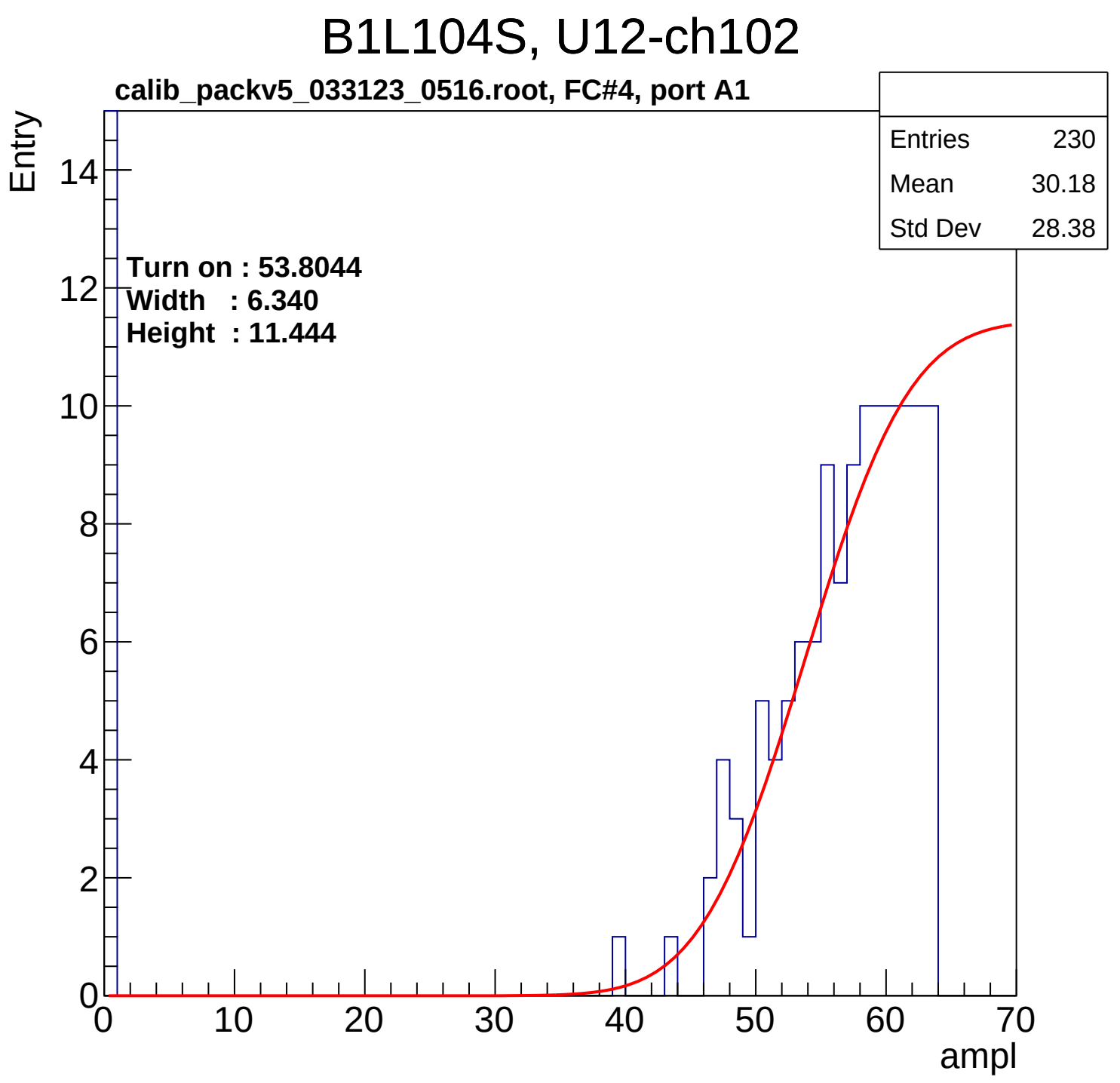
B1L104S, U12-ch102
calib_packv5_033123_0516.root, FC#4, port A1
Entries 230
Mean 30.18
Std Dev 28.38
Turn on : 53.8044
Width : 6.340
Height : 11.444
Entry
ampl
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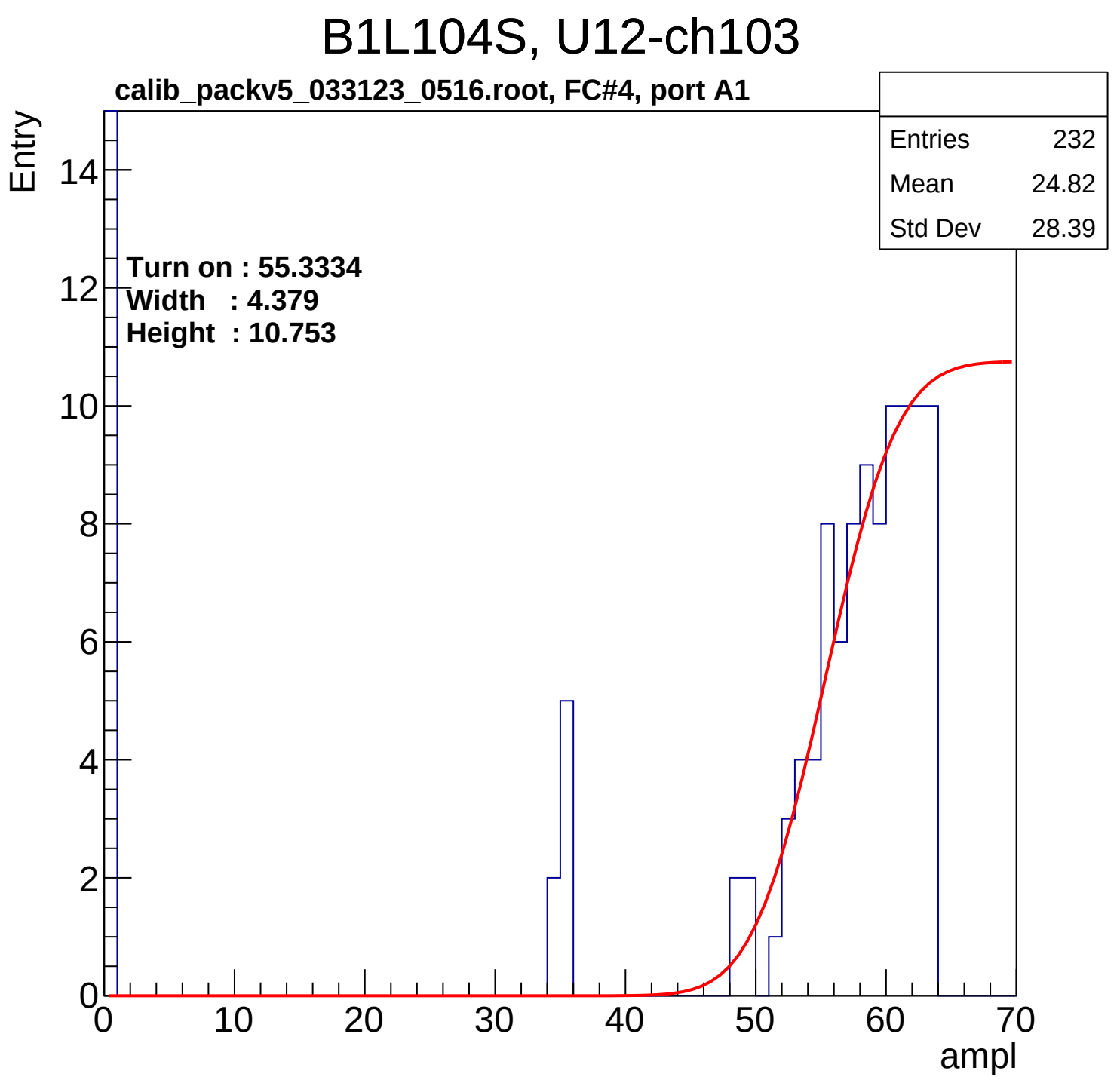
B1L104S, U12-ch103
calib_packv5_033123_0516.root, FC#4, port A1
Entries 232
Mean 24.82
Std Dev 28.39
Turn on : 55.3334
Width : 4.379
Height : 10.753
Entry
ampl
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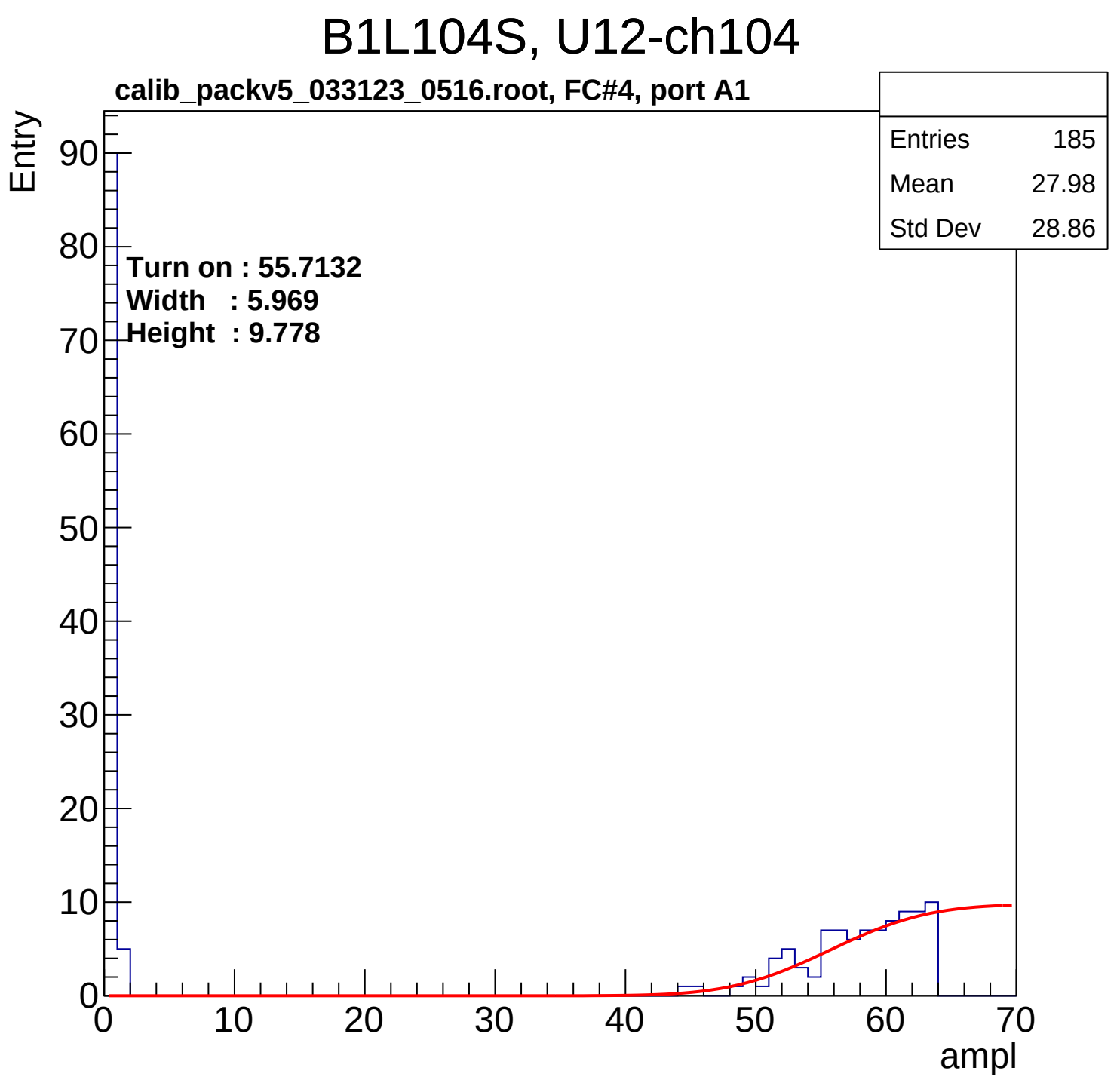
B1L104S, U12-ch104
calib_packv5_033123_0516.root, FC#4, port A1
Entries 185
Mean 27.98
Std Dev 28.86
Turn on : 55.7132
Width : 5.969
Height : 9.778
Entry
ampl
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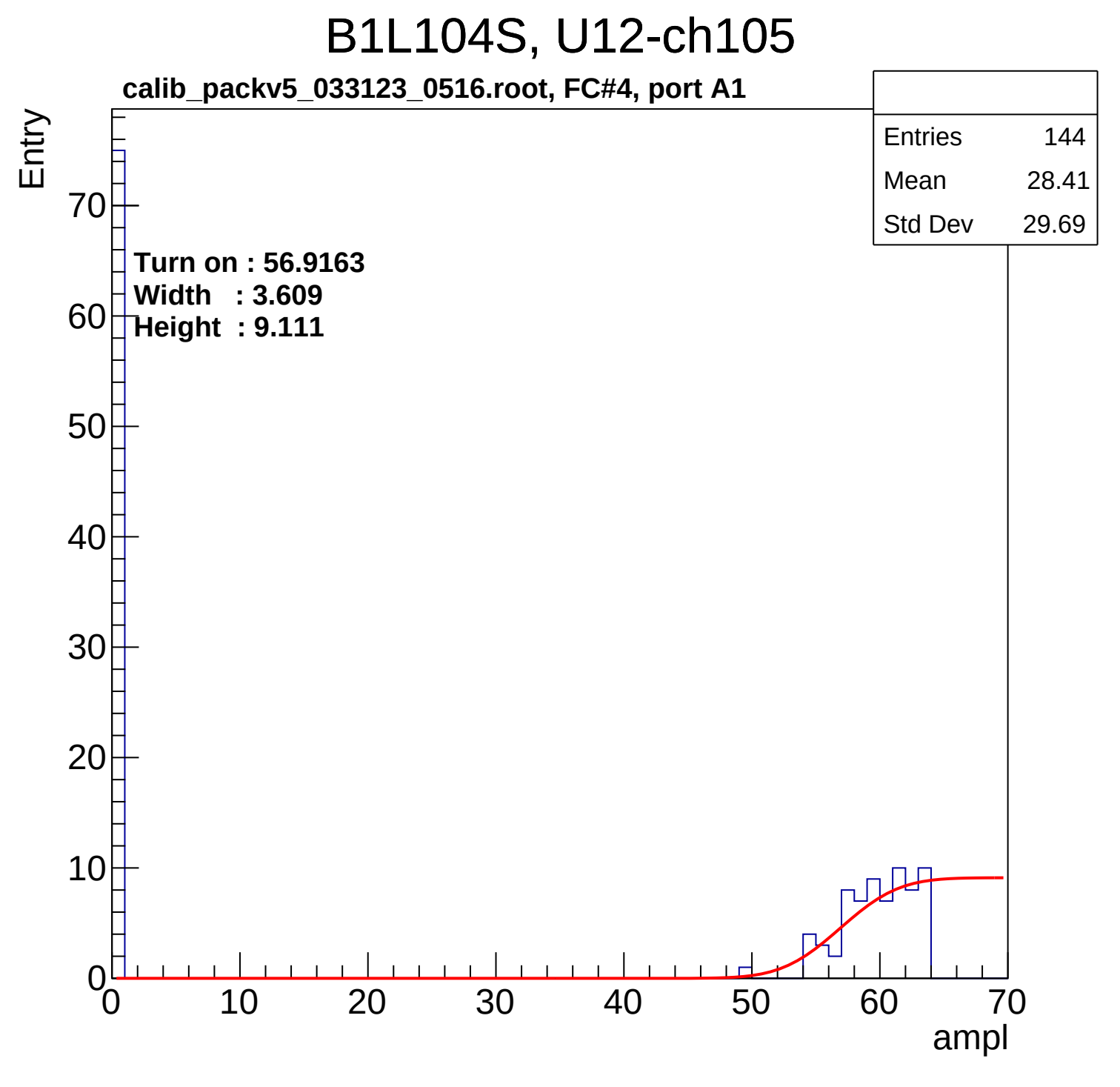
B1L104S, U12-ch105
calib_packv5_033123_0516.root, FC#4, port A1
Entries 144
Mean 28.41
Std Dev 29.69
Turn on : 56.9163
Width : 3.609
Height : 9.111
Entry
ampl
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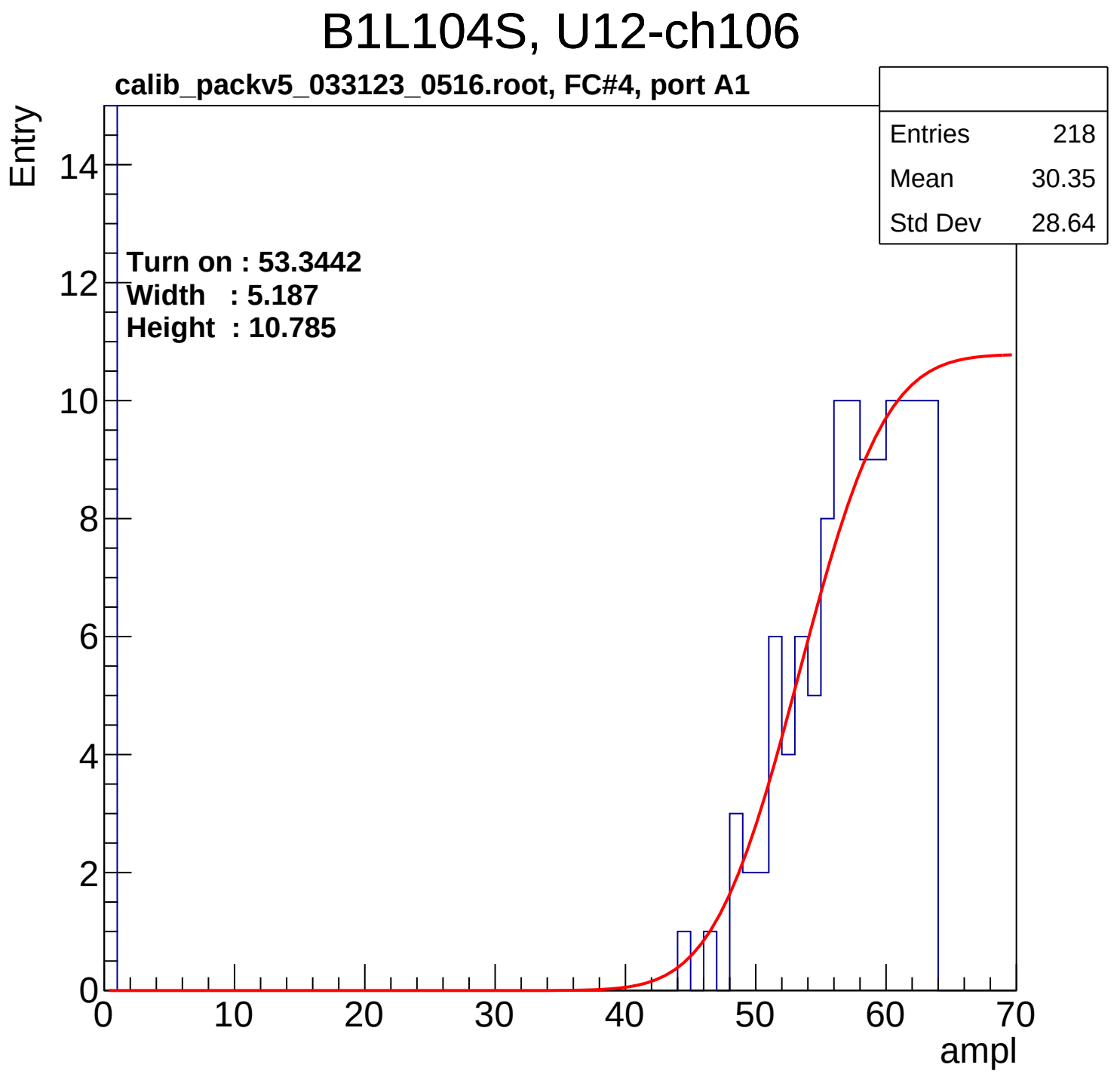
B1L104S, U12-ch106
calib_packv5_033123_0516.root, FC#4, port A1
Entries 218
Mean 30.35
Std Dev 28.64
Turn on : 53.3442
Width : 5.187
Height : 10.785
Entry
ampl
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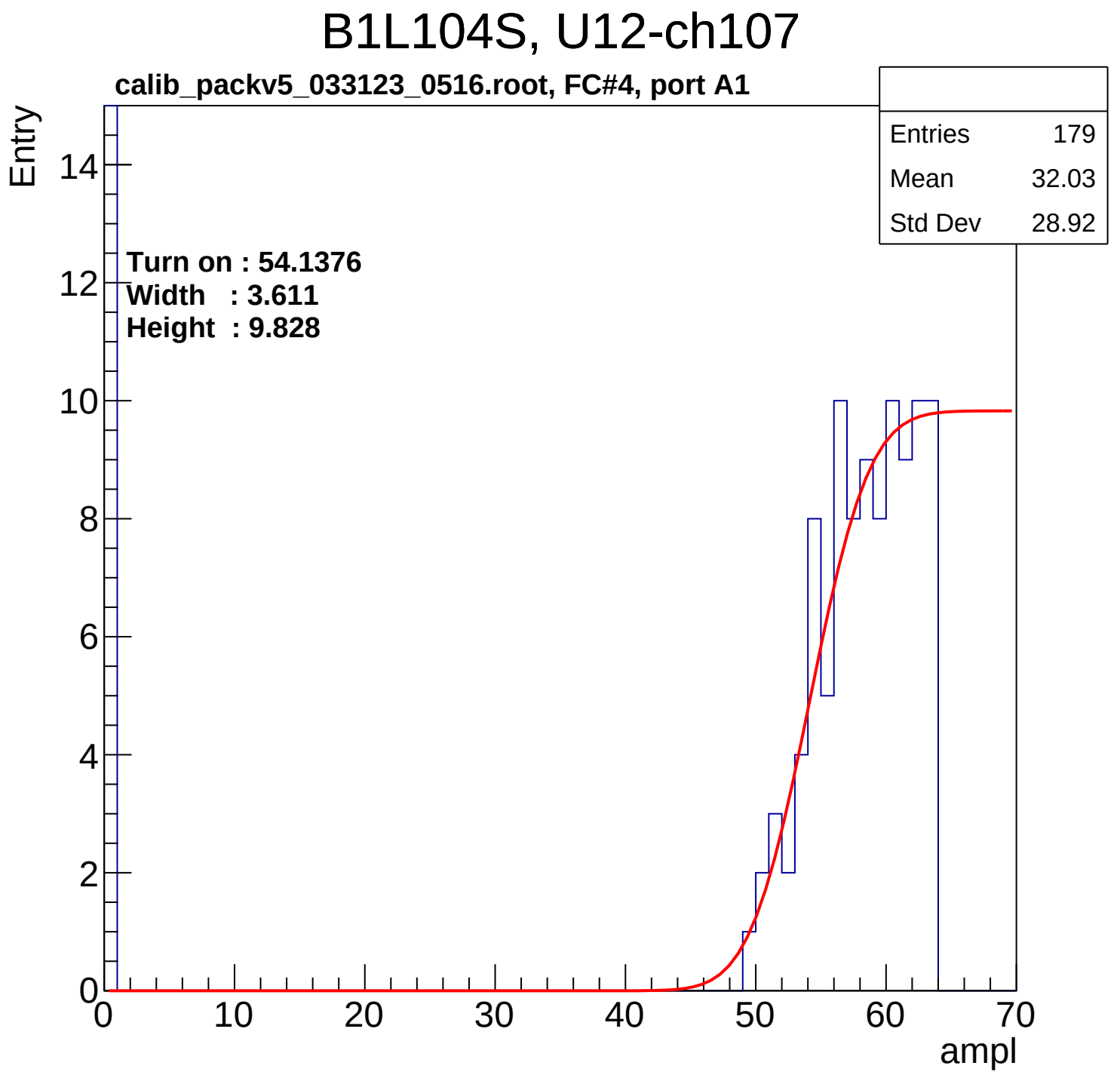
B1L104S, U12-ch107
calib_packv5_033123_0516.root, FC#4, port A1
Entries 179
Mean 32.03
Std Dev 28.92
Turn on : 54.1376
Width : 3.611
Height : 9.828
Entry
ampl
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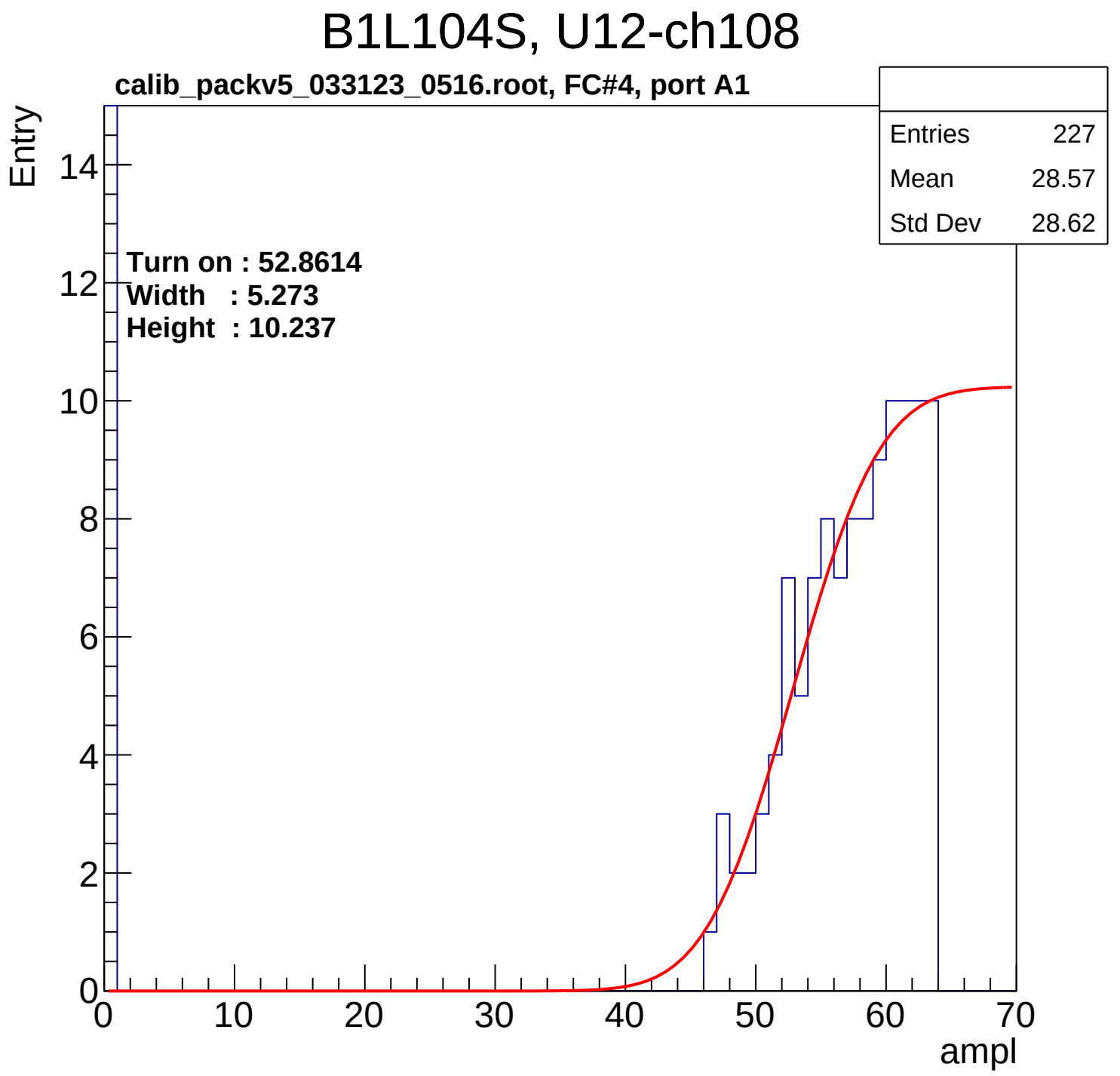
B1L104S, U12-ch108
calib_packv5_033123_0516.root, FC#4, port A1
Entries 227
Mean 28.57
Std Dev 28.62
Turn on : 52.8614
Width : 5.273
Height : 10.237
Entry
ampl
0
2
4
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8
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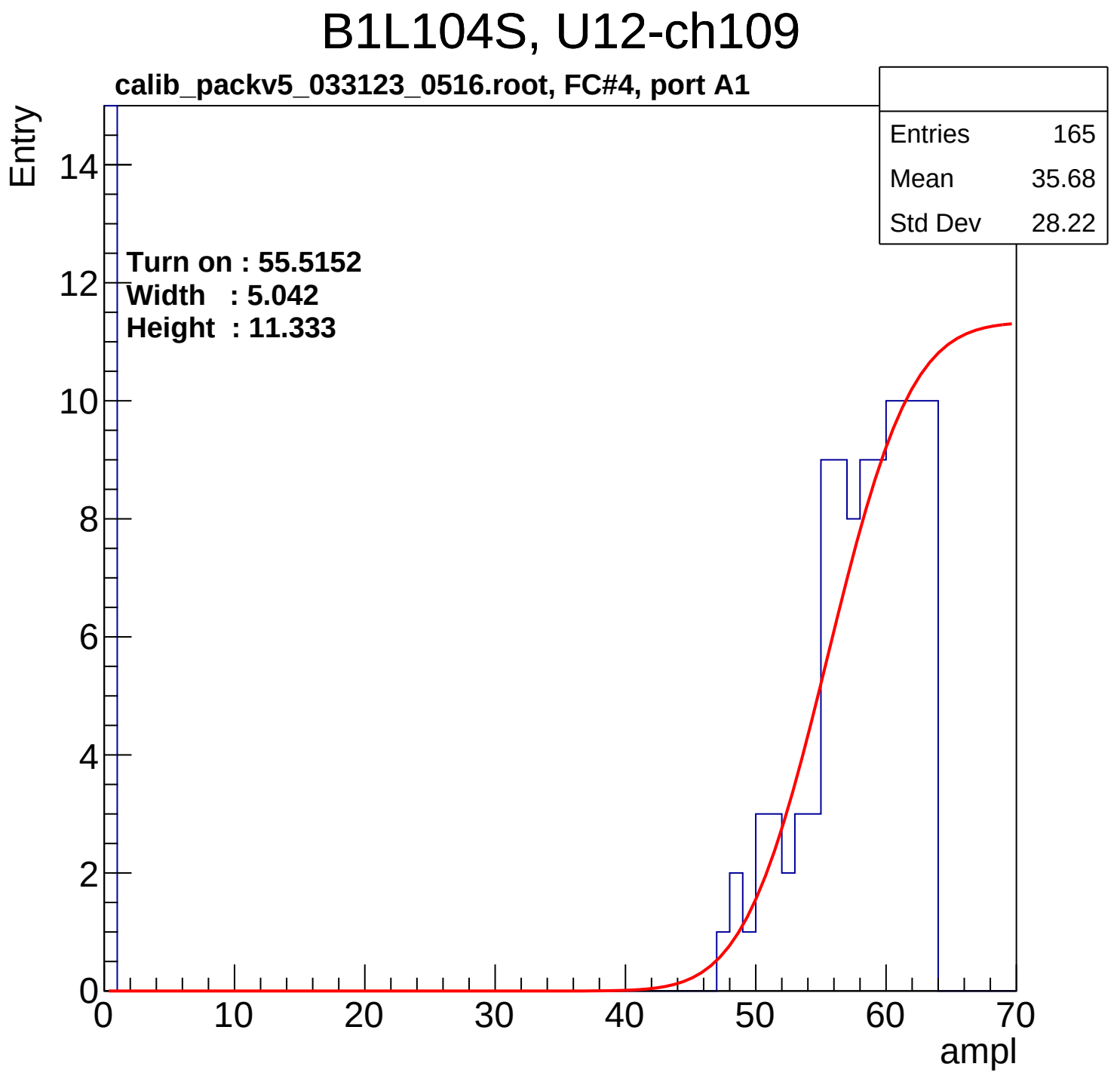
B1L104S, U12-ch109
calib_packv5_033123_0516.root, FC#4, port A1
Entries 165
Mean 35.68
Std Dev 28.22
Turn on : 55.5152
Width : 5.042
Height : 11.333
Entry
ampl
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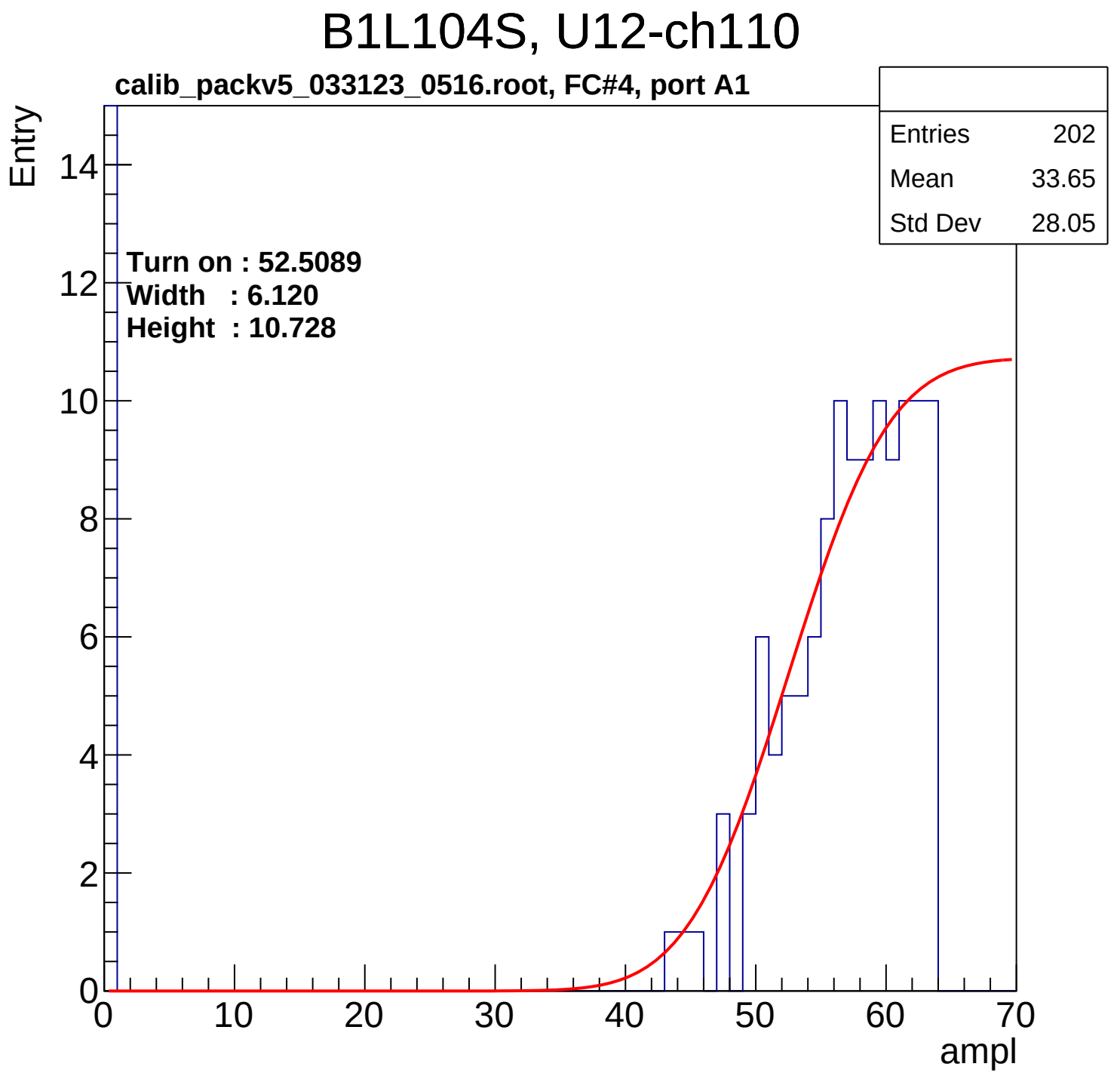
B1L104S, U12-ch110
calib_packv5_033123_0516.root, FC#4, port A1
Entries 202
Mean 33.65
Std Dev 28.05
Turn on : 52.5089
Width : 6.120
Height : 10.728
Entry
ampl
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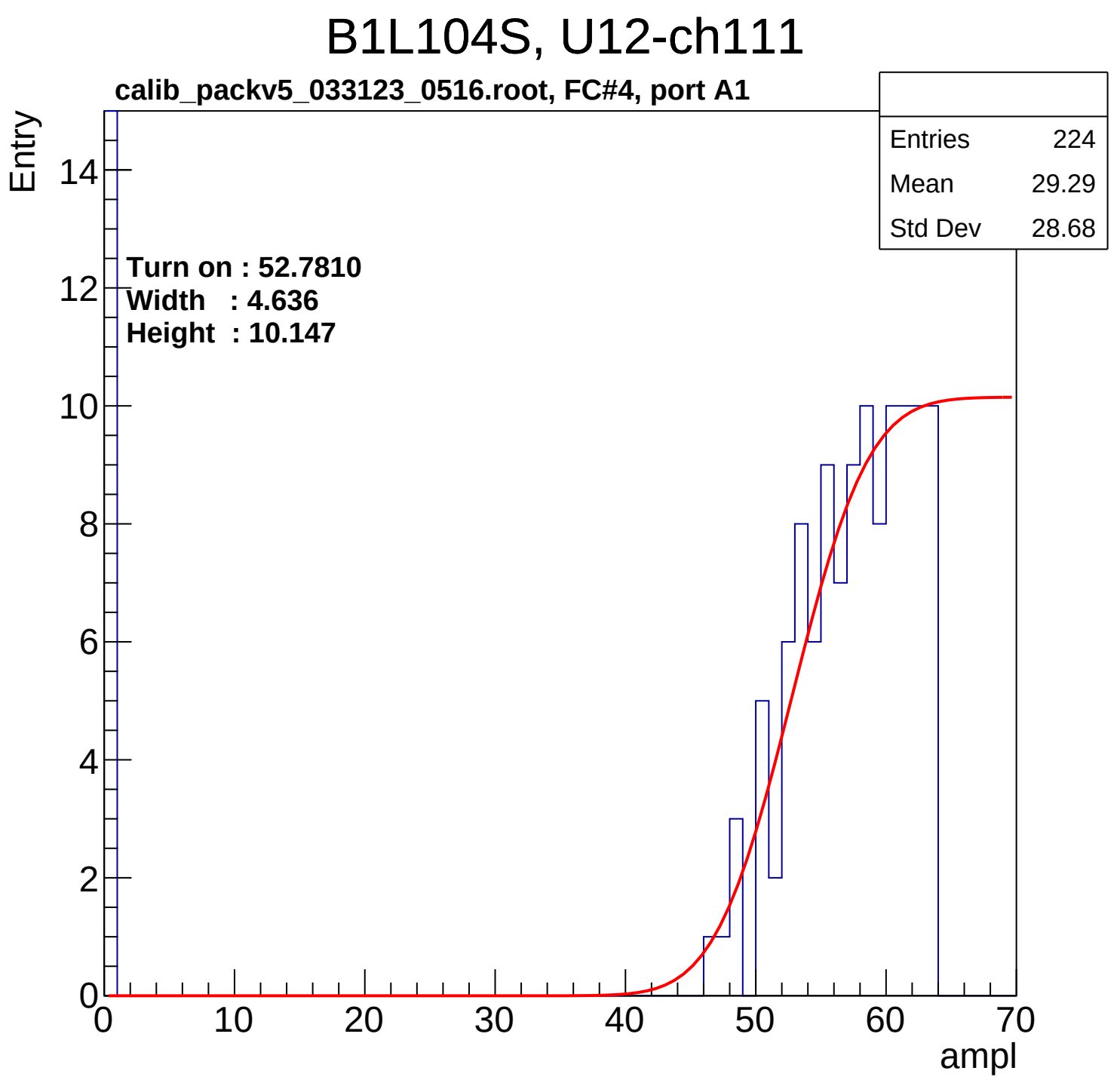
B1L104S, U12-ch111
calib_packv5_033123_0516.root, FC#4, port A1
Entries 224
Mean 29.29
Std Dev 28.68
Turn on : 52.7810
Width : 4.636
Height : 10.147
Entry
ampl
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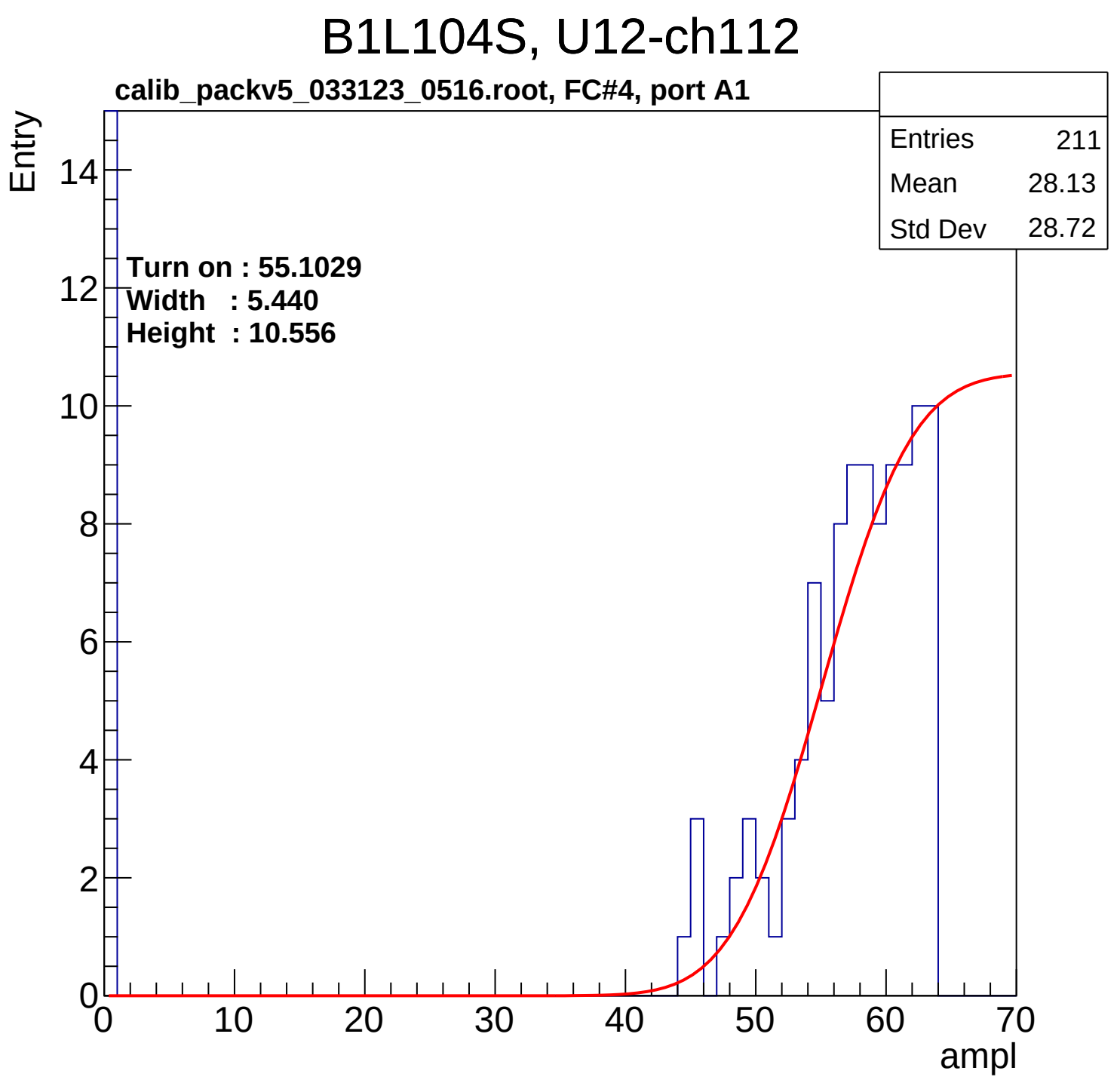
B1L104S, U12-ch112
calib_packv5_033123_0516.root, FC#4, port A1
Entries 211
Mean 28.13
Std Dev 28.72
Turn on : 55.1029
Width : 5.440
Height : 10.556
Entry
ampl
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8
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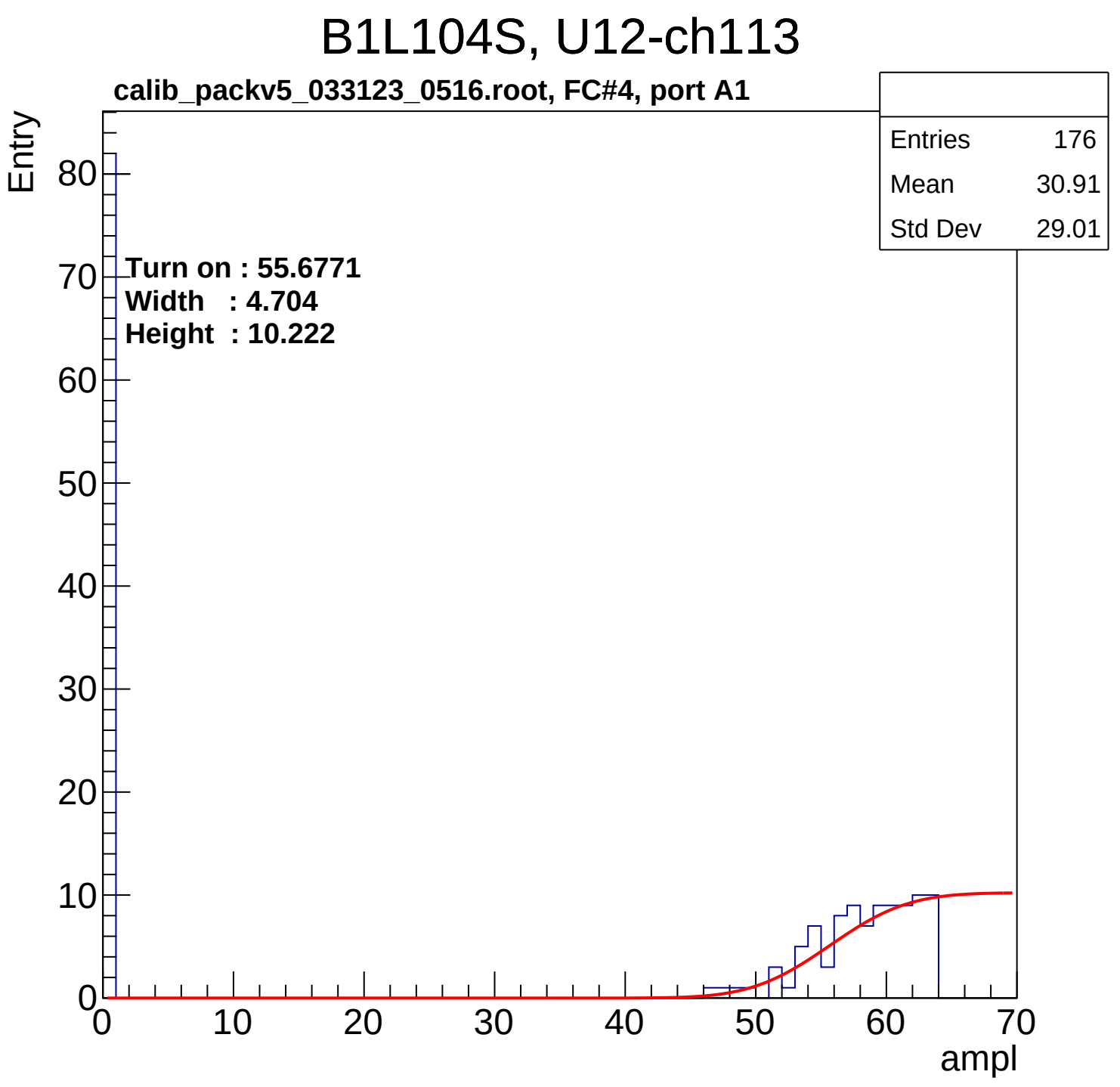
B1L104S, U12-ch113
calib_packv5_033123_0516.root, FC#4, port A1
Entries 176
Mean 30.91
Std Dev 29.01
Turn on : 55.6771
Width : 4.704
Height : 10.222
Entry
ampl
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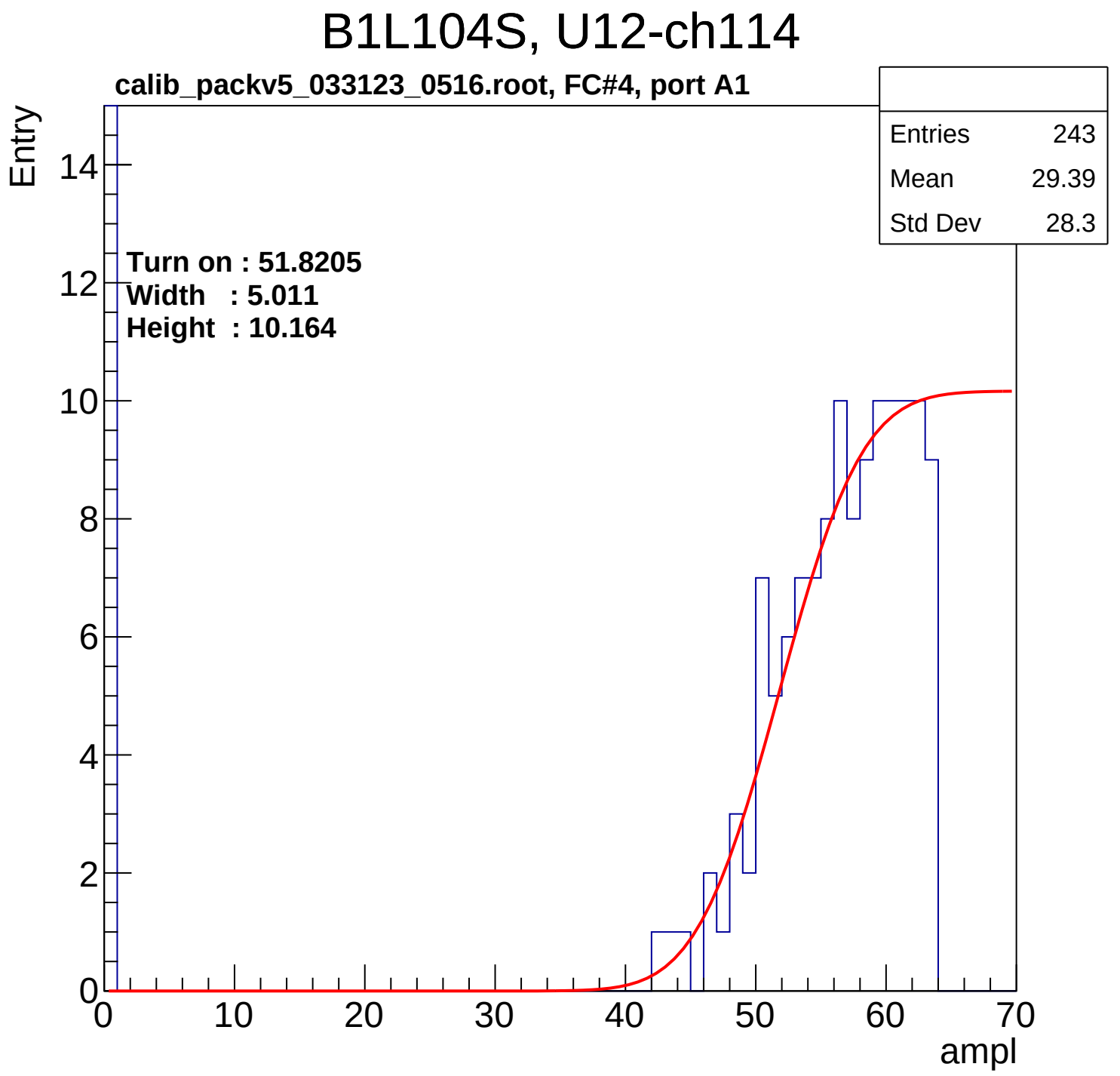
B1L104S, U12-ch114
calib_packv5_033123_0516.root, FC#4, port A1
Entries 243
Mean 29.39
Std Dev 28.3
Turn on : 51.8205
Width : 5.011
Height : 10.164
Entry
ampl
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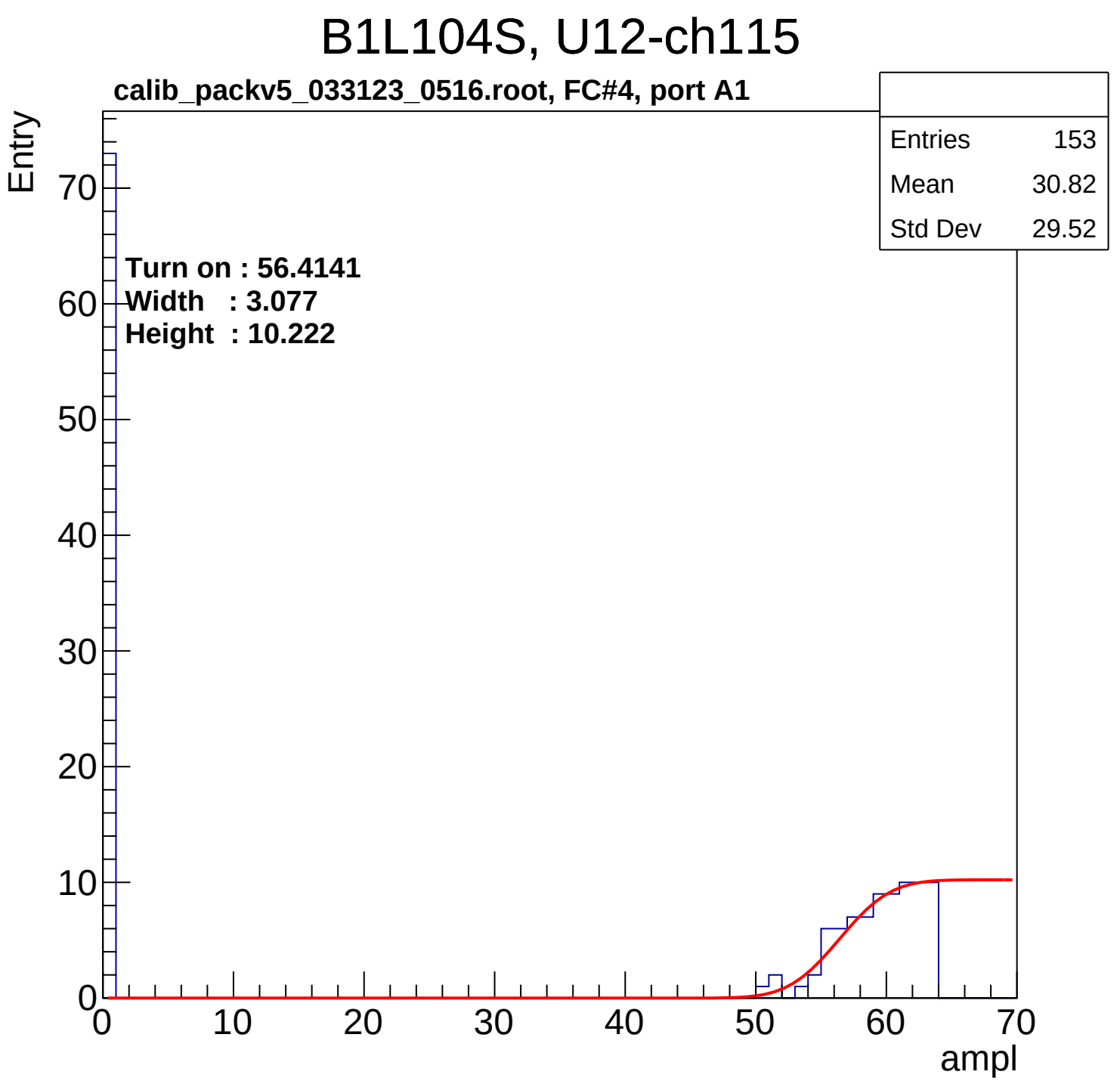
B1L104S, U12-ch115
calib_packv5_033123_0516.root, FC#4, port A1
Entries 153
Mean 30.82
Std Dev 29.52
Turn on : 56.4141
Width : 3.077
Height : 10.222
Entry
ampl
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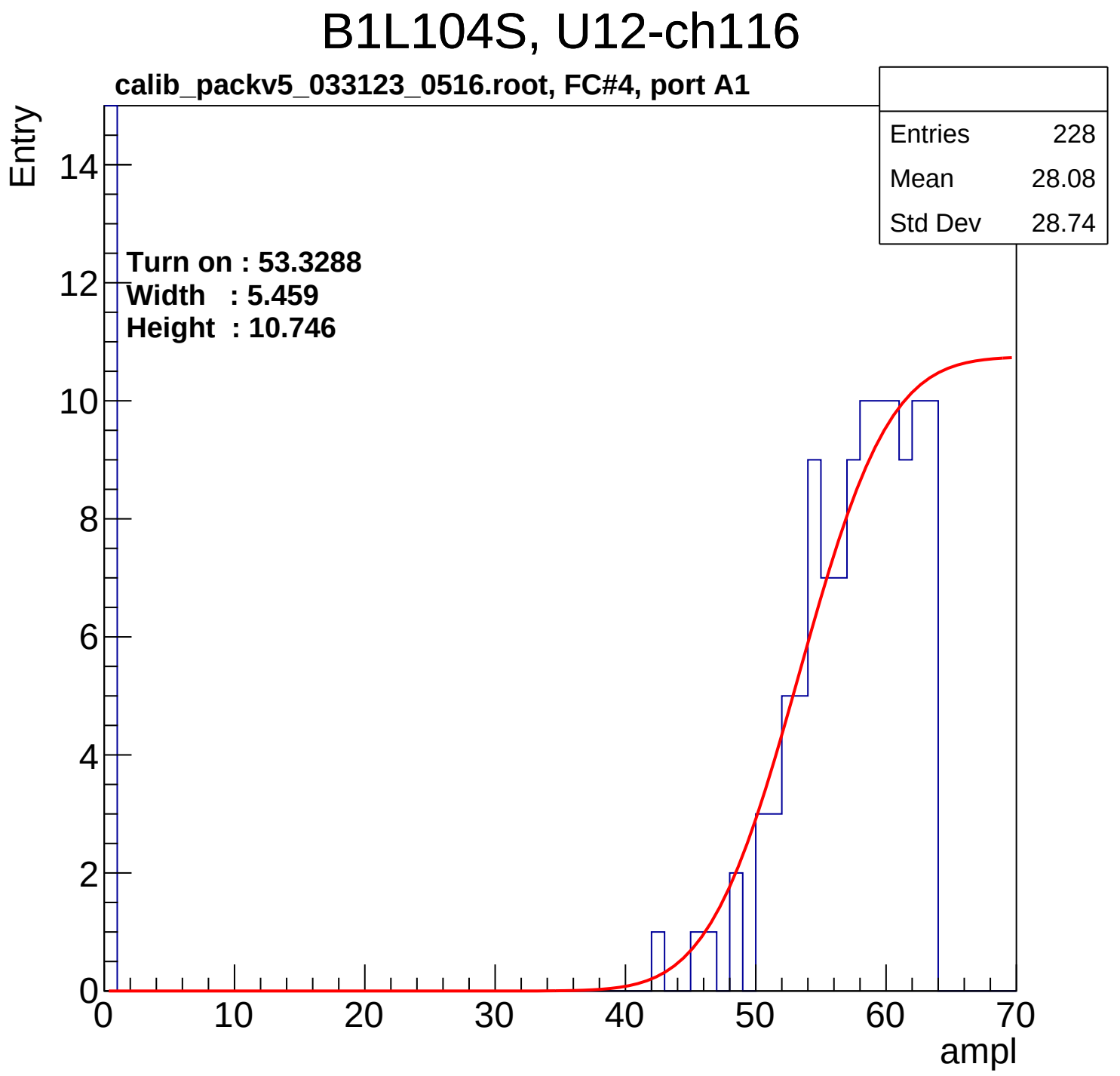
B1L104S, U12-ch116
calib_packv5_033123_0516.root, FC#4, port A1
Entries 228
Mean 28.08
Std Dev 28.74
Turn on : 53.3288
Width : 5.459
Height : 10.746
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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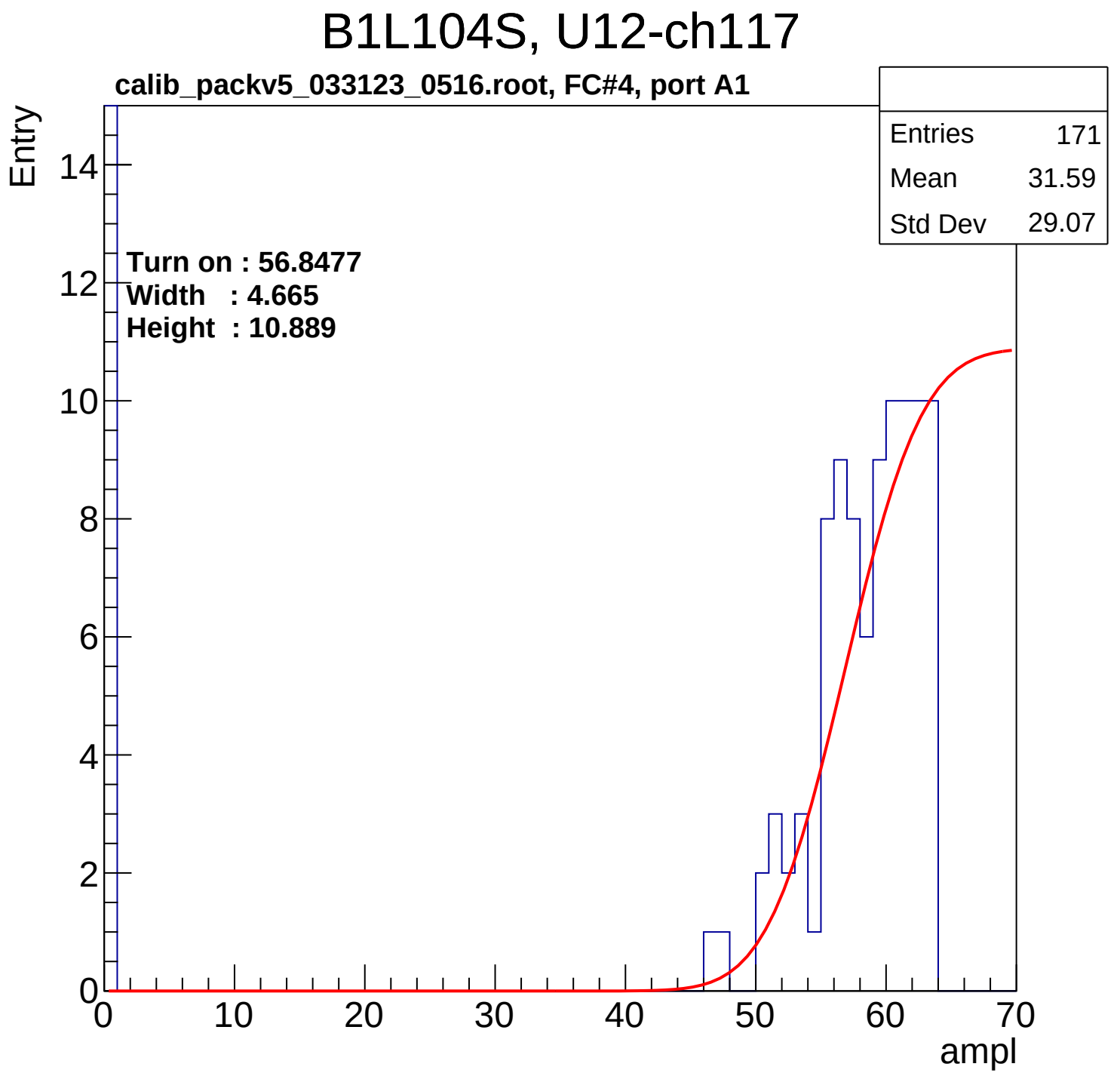
B1L104S, U12-ch117
calib_packv5_033123_0516.root, FC#4, port A1
Entries 171
Mean 31.59
Std Dev 29.07
Turn on : 56.8477
Width : 4.665
Height : 10.889
Entry
ampl
0
2
4
6
8
10
12
14
0
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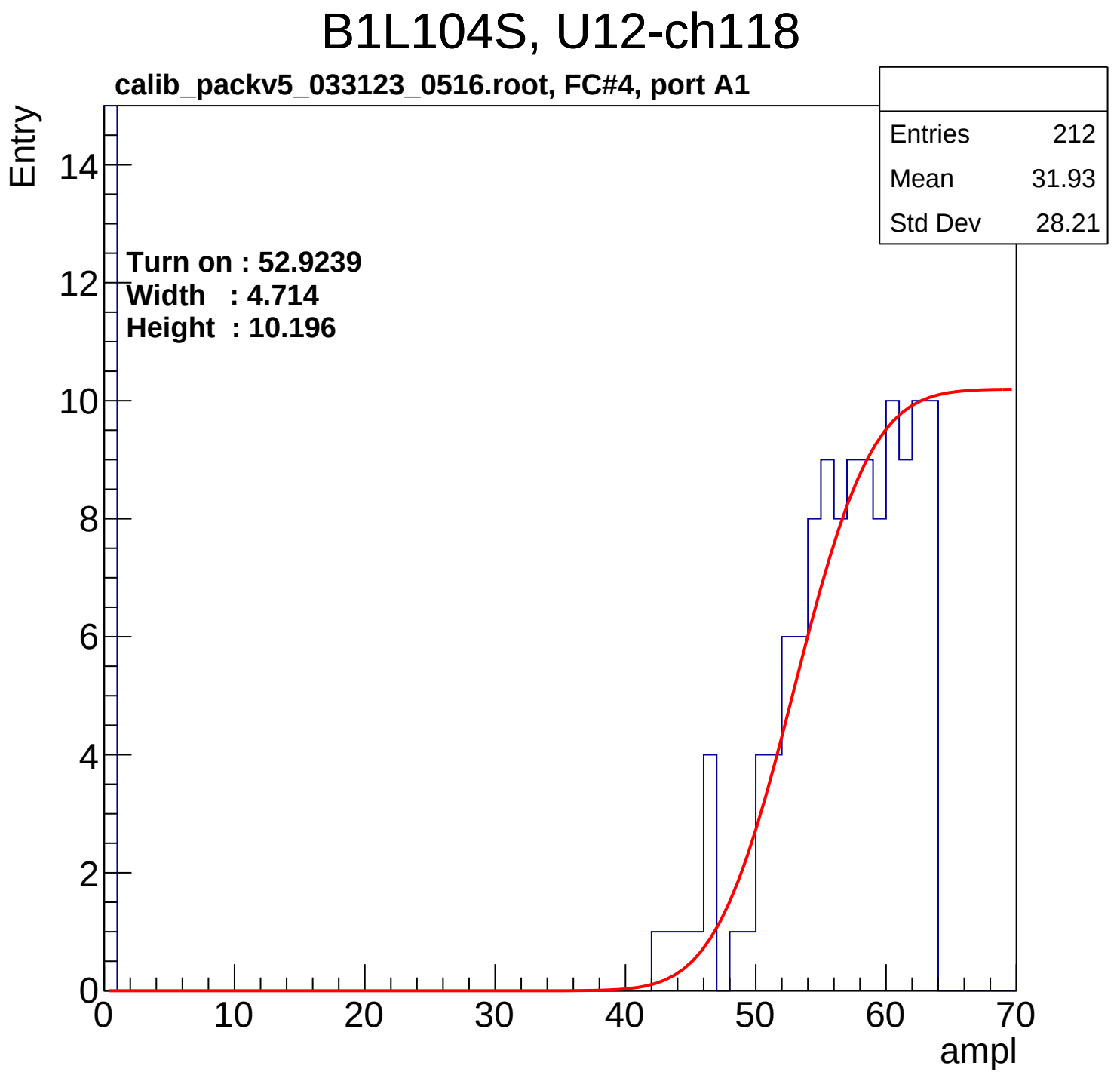
B1L104S, U12-ch118
calib_packv5_033123_0516.root, FC#4, port A1
Entries 212
Mean 31.93
Std Dev 28.21
Turn on : 52.9239
Width : 4.714
Height : 10.196
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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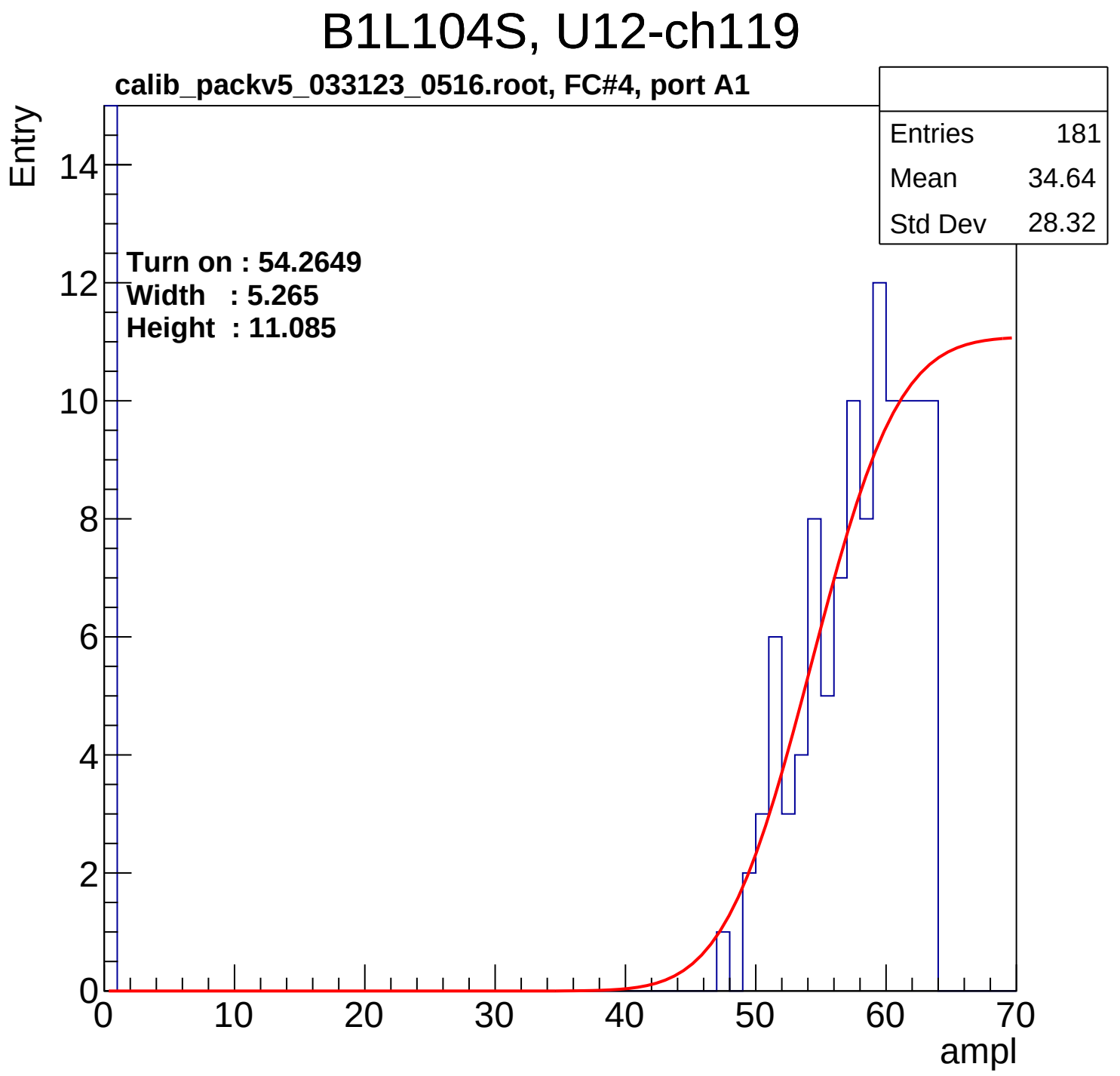
B1L104S, U12-ch119
calib_packv5_033123_0516.root, FC#4, port A1
Entries 181
Mean 34.64
Std Dev 28.32
Turn on : 54.2649
Width : 5.265
Height : 11.085
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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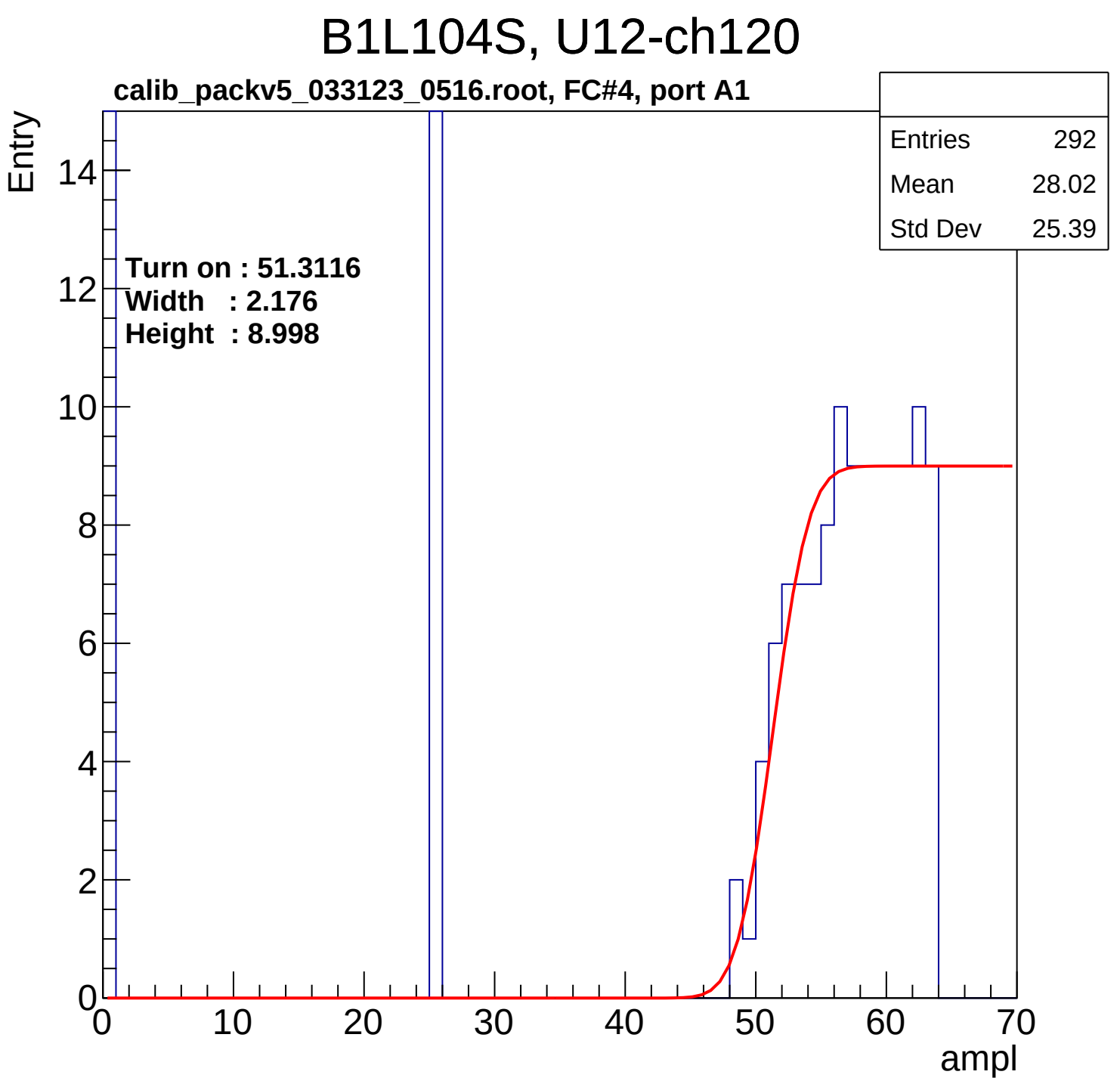
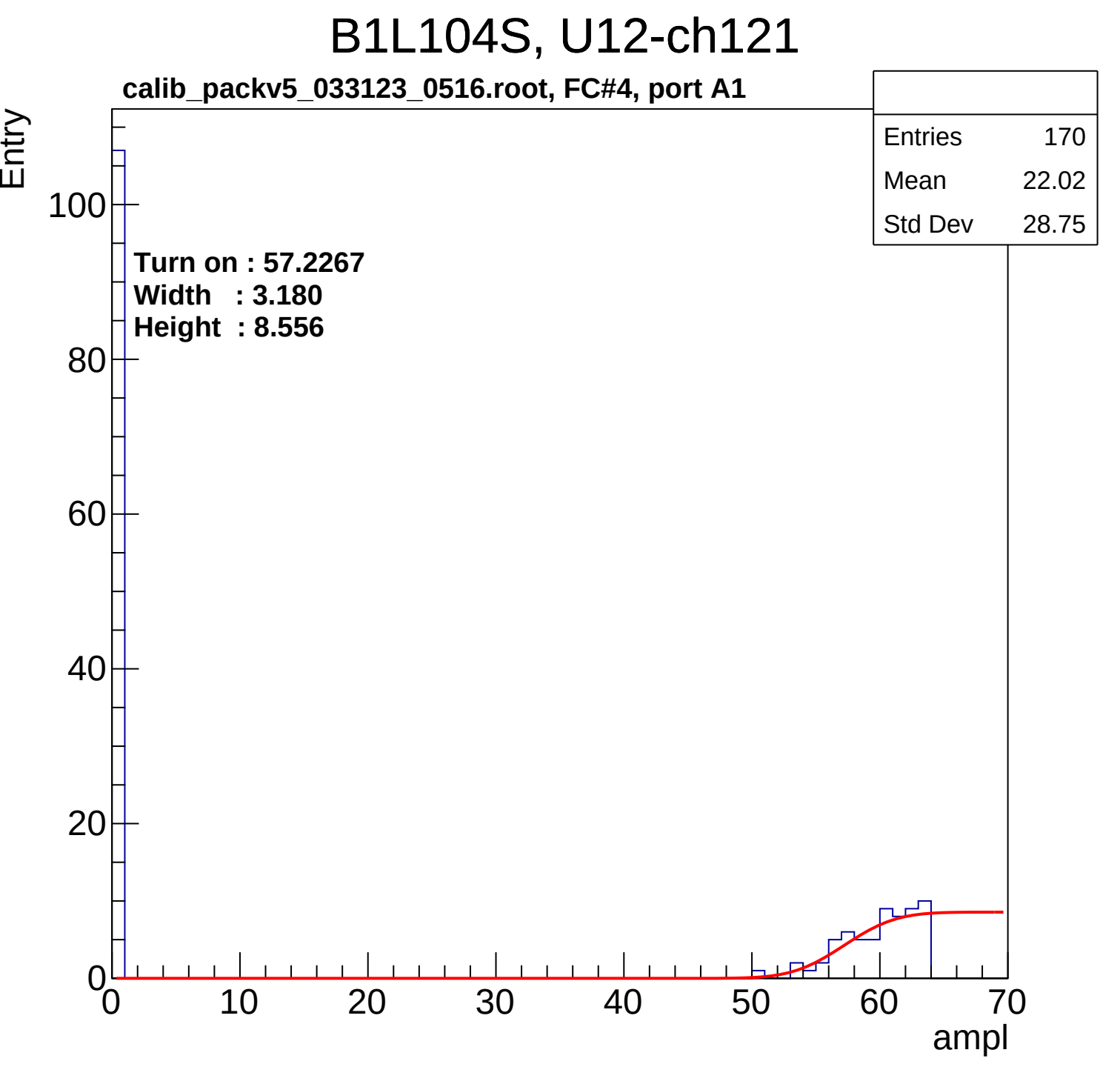
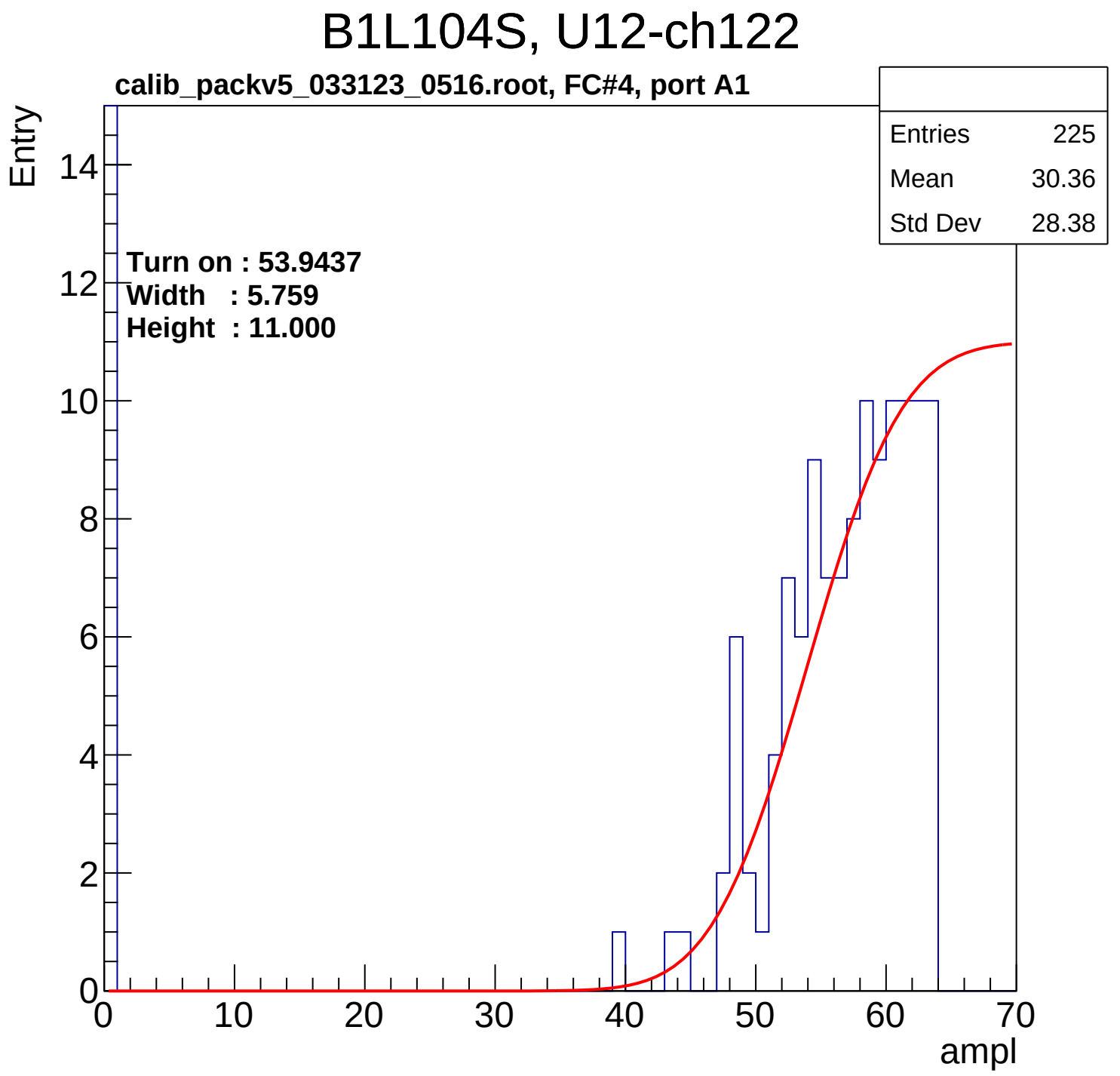
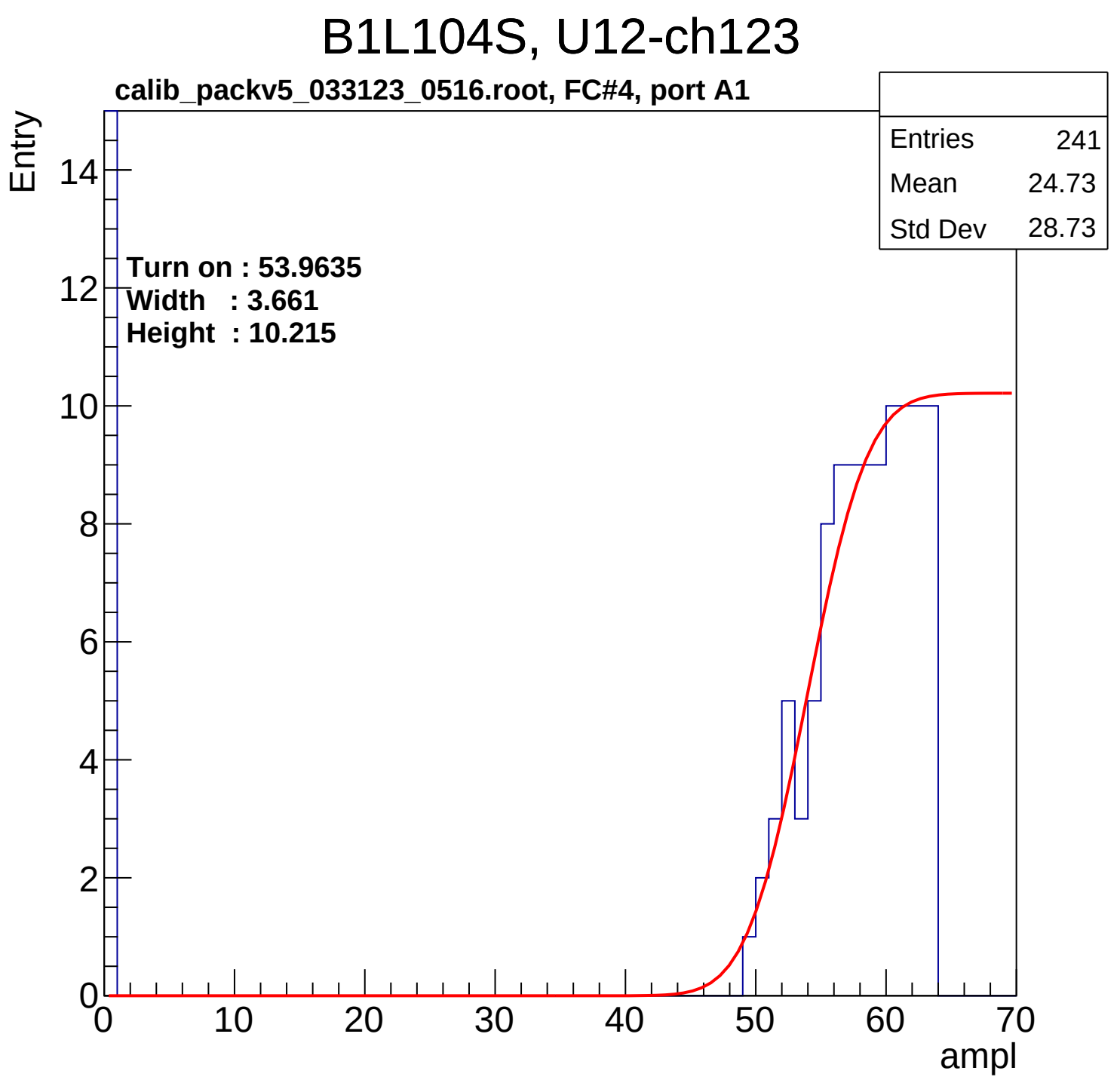

B1L104S, U12-ch120
calib_packv5_033123_0516.root, FC#4, port A1
Entries 292
Mean 28.02
Std Dev 25.39
Turn on : 51.3116
Width : 2.176
Height : 8.998
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L104S, U12-ch121
calib_packv5_033123_0516.root, FC#4, port A1
Entries 170
Mean 22.02
Std Dev 28.75
Turn on : 57.2267
Width : 3.180
Height : 8.556
Entry
ampl
0
20
40
60
80
100
0
10
20
30
40
50
60
70


B1L104S, U12-ch122
calib_packv5_033123_0516.root, FC#4, port A1
Entries 225
Mean 30.36
Std Dev 28.38
Turn on : 53.9437
Width : 5.759
Height : 11.000
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L104S, U12-ch123
calib_packv5_033123_0516.root, FC#4, port A1
Entries 241
Mean 24.73
Std Dev 28.73
Turn on : 53.9635
Width : 3.661
Height : 10.215
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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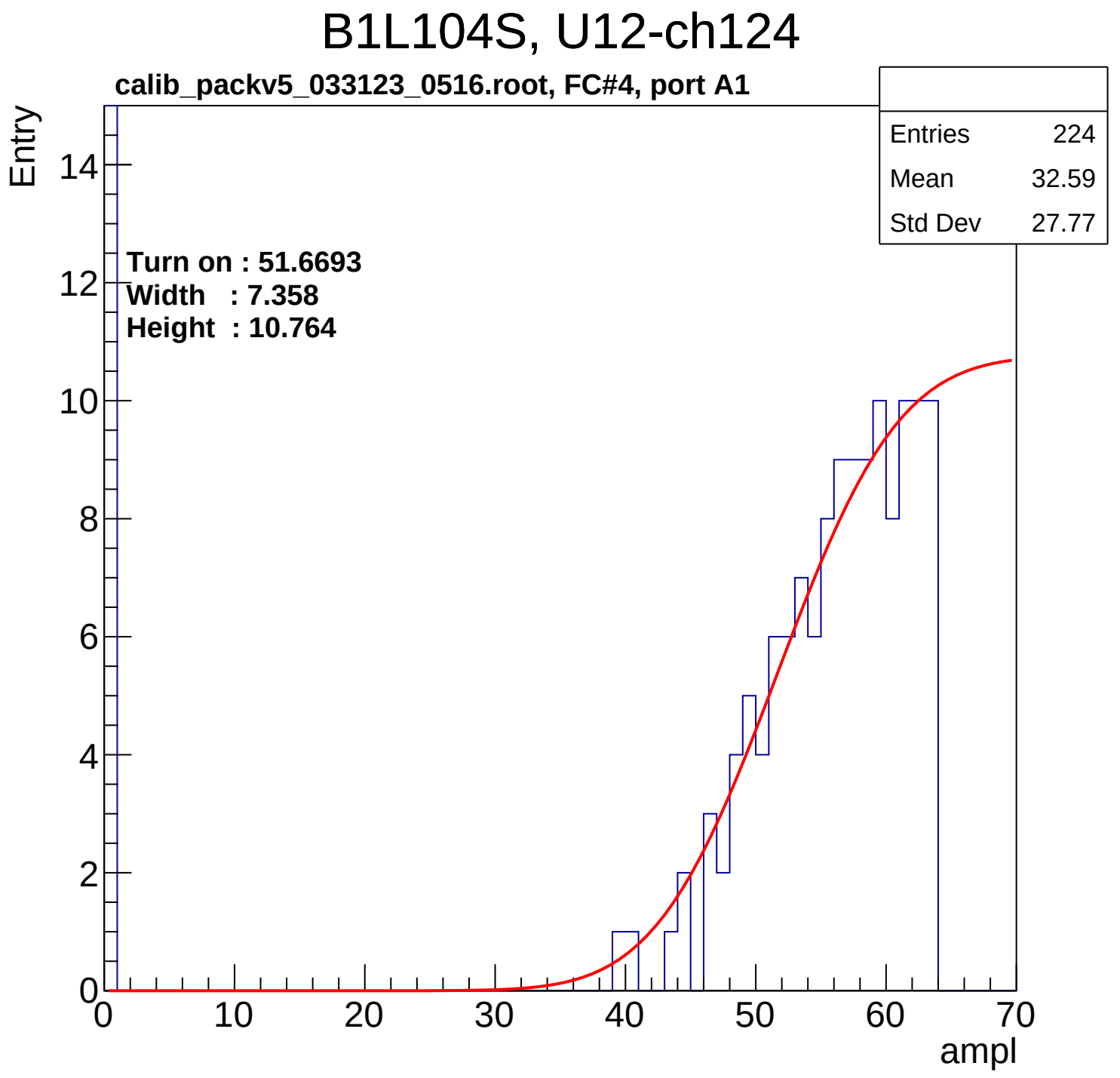
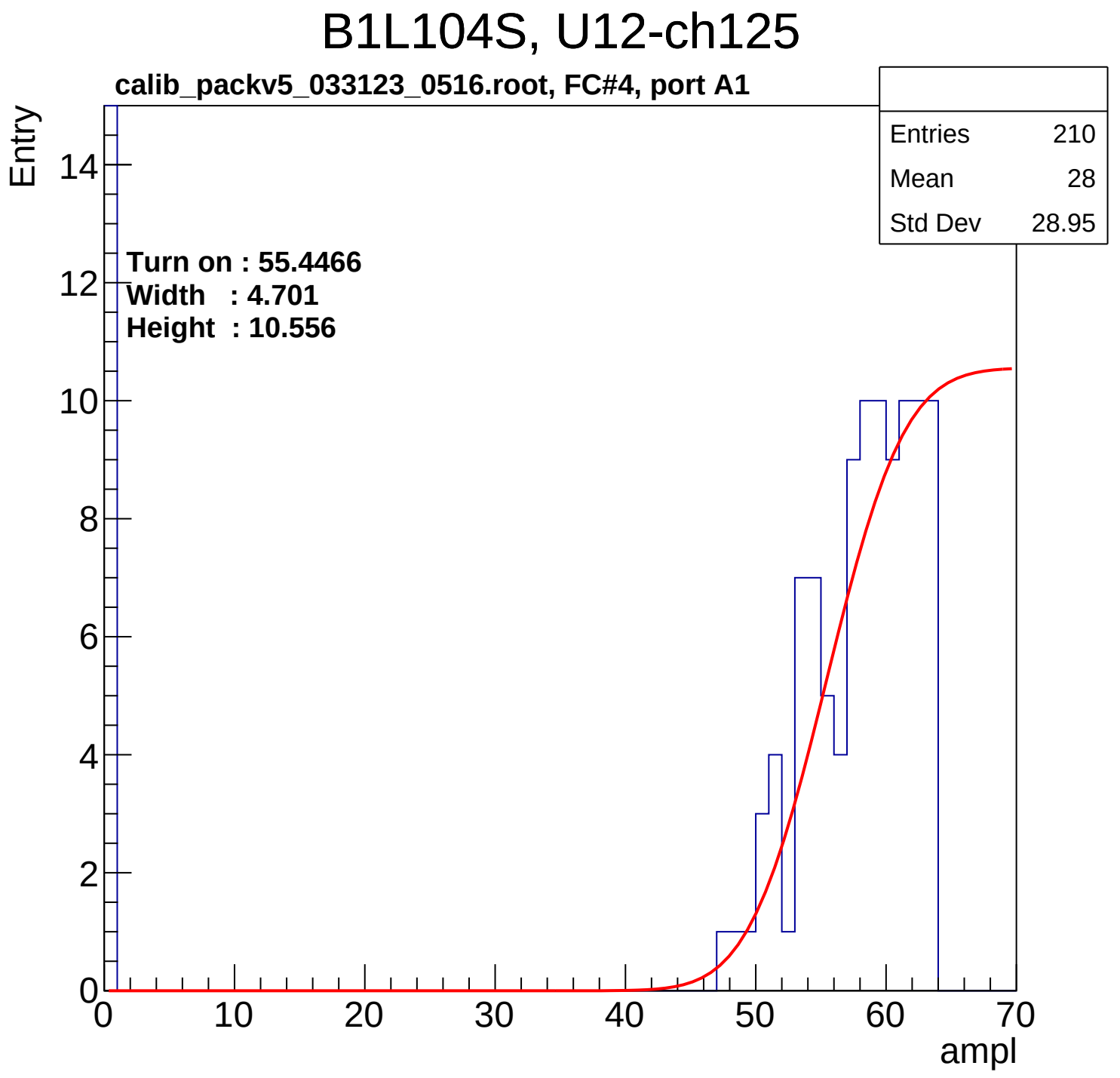
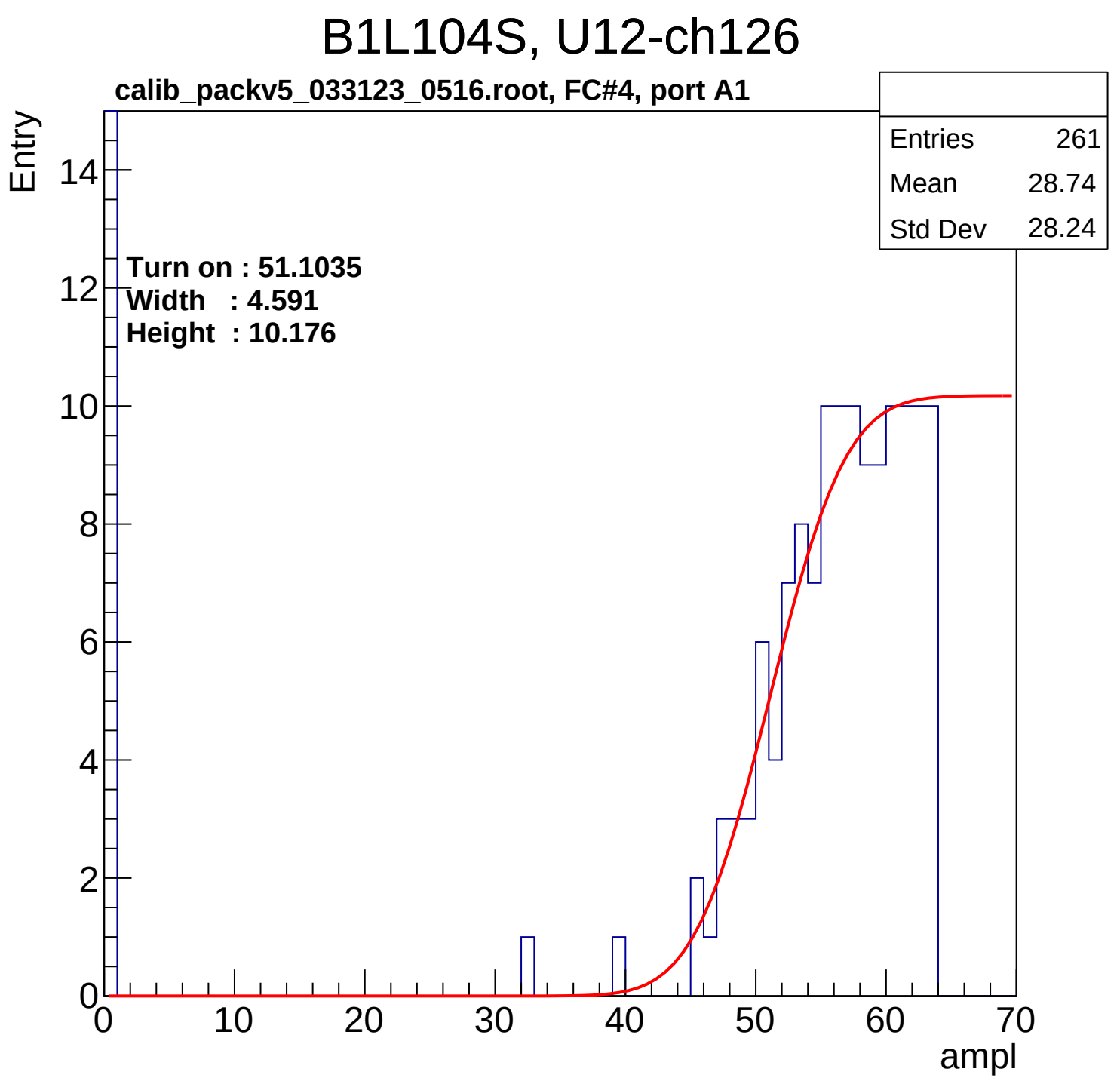
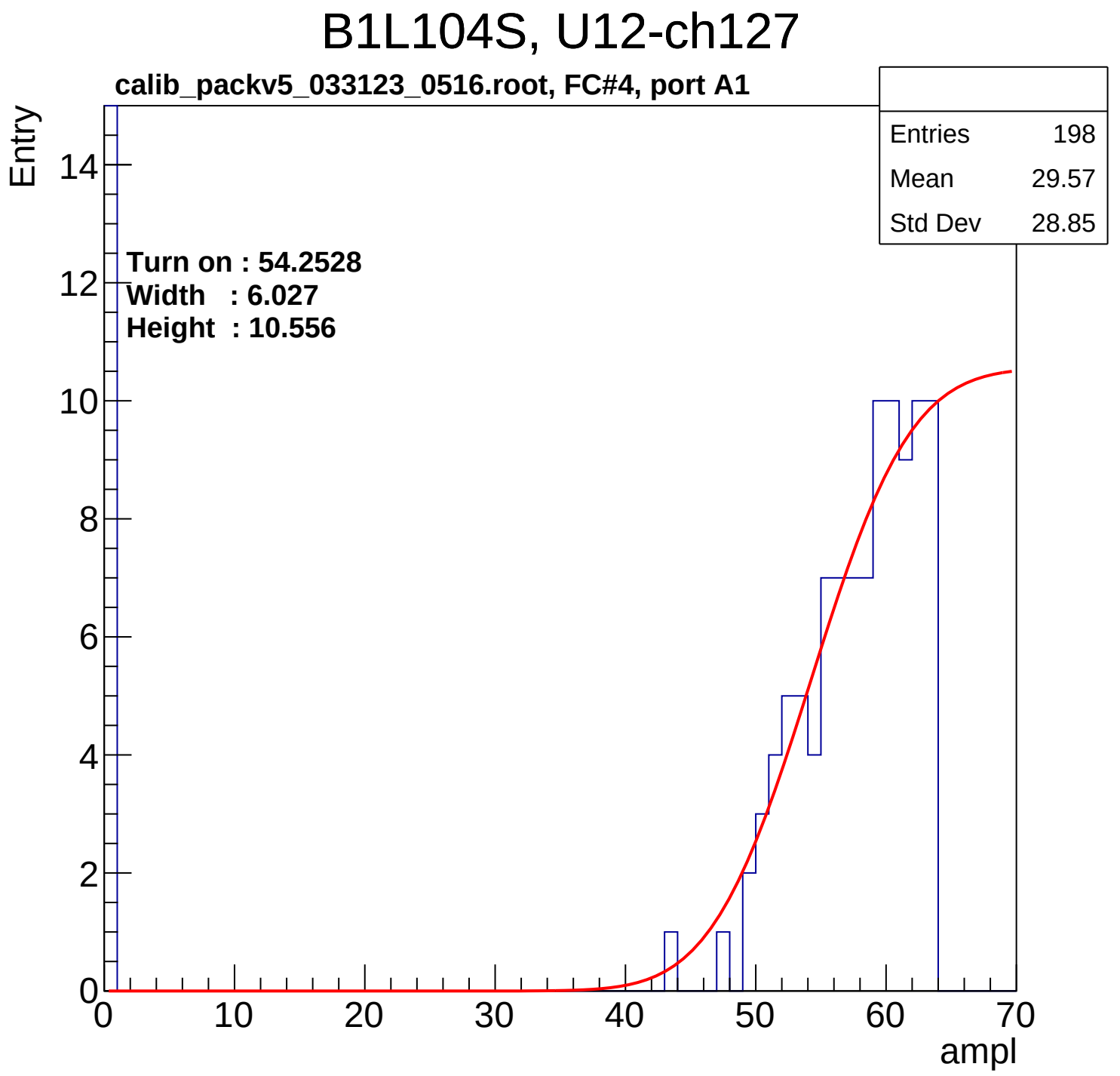
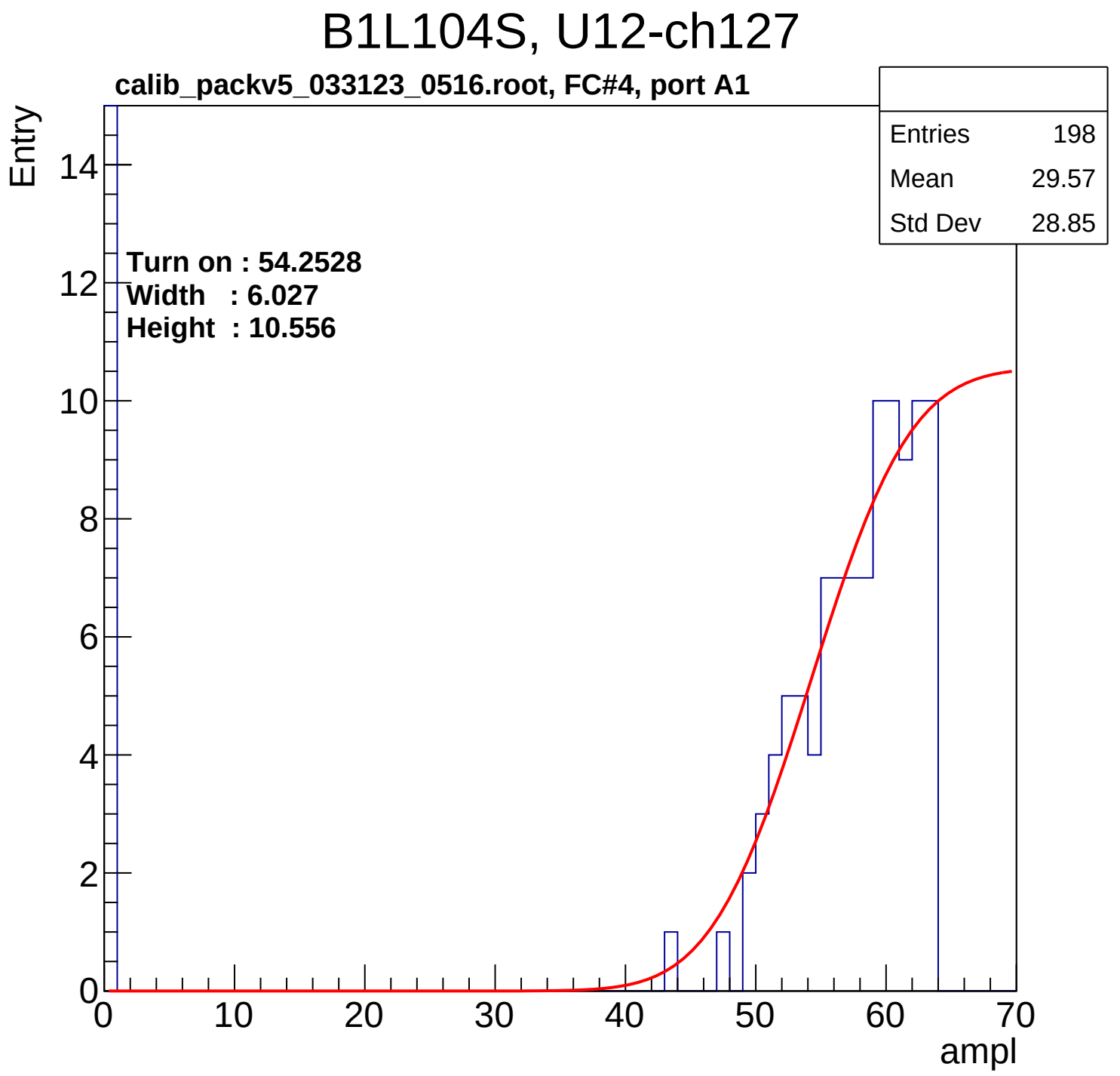

B1L104S, U12-ch124
calib_packv5_033123_0516.root, FC#4, port A1
Entries 224
Mean 32.59
Std Dev 27.77
Turn on : 51.6693
Width : 7.358
Height : 10.764
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L104S, U12-ch125
calib_packv5_033123_0516.root, FC#4, port A1
Entries 210
Mean 28
Std Dev 28.95
Turn on : 55.4466
Width : 4.701
Height : 10.556
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L104S, U12-ch126
calib_packv5_033123_0516.root, FC#4, port A1
Entries 261
Mean 28.74
Std Dev 28.24
Turn on : 51.1035
Width : 4.591
Height : 10.176
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L104S, U12-ch127
calib_packv5_033123_0516.root, FC#4, port A1
Entries 198
Mean 29.57
Std Dev 28.85
Turn on : 54.2528
Width : 6.027
Height : 10.556
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L104S, U12-ch127
calib_packv5_033123_0516.root, FC#4, port A1
Entries 198
Mean 29.57
Std Dev 28.85
Turn on : 54.2528
Width : 6.027
Height : 10.556
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70