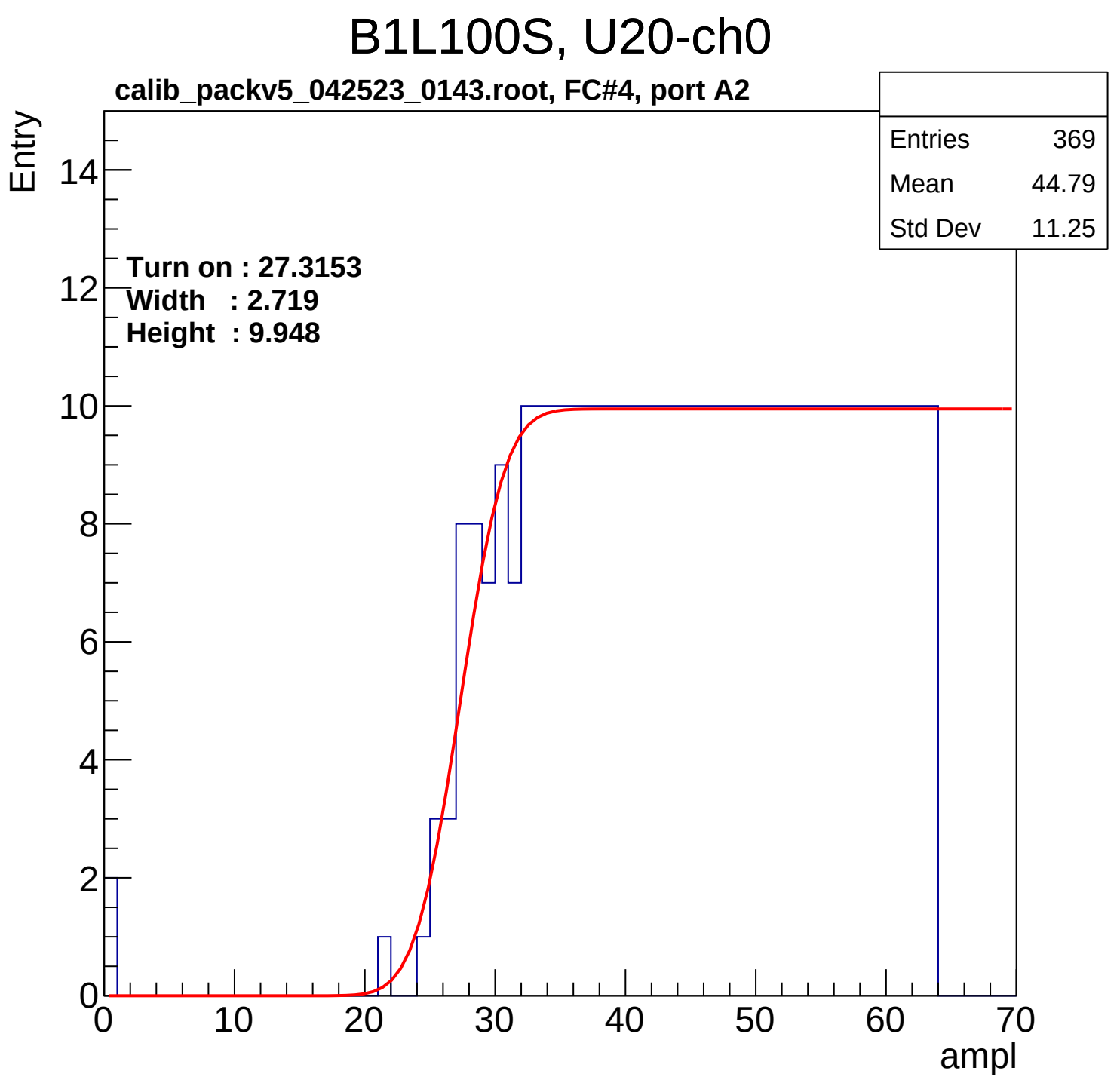
B1L100S, U20-ch0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 369
Mean 44.79
Std Dev 11.25
Turn on : 27.3153
Width : 2.719
Height : 9.948
Entry
ampl
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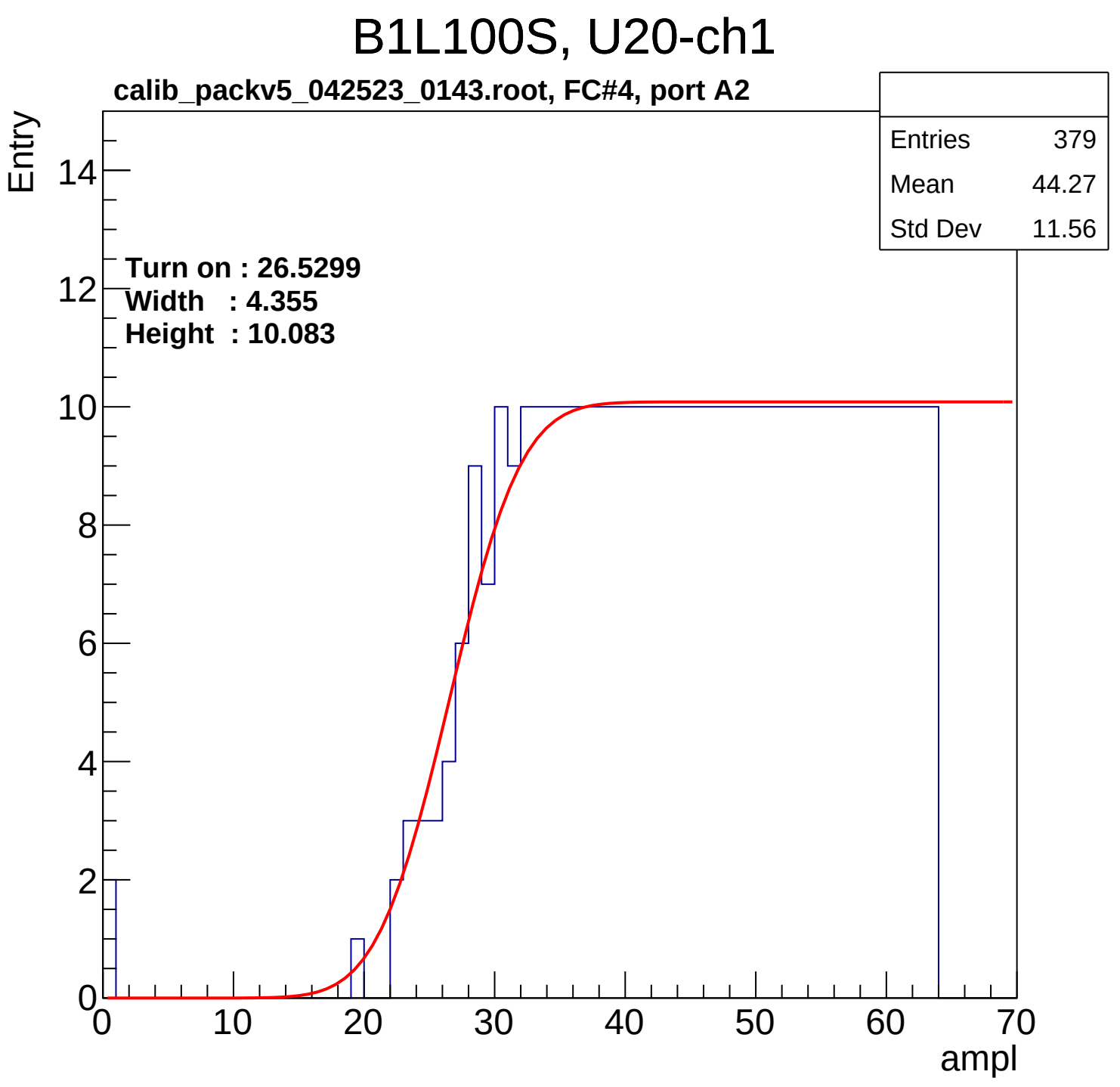
B1L100S, U20-ch1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 379
Mean 44.27
Std Dev 11.56
Turn on : 26.5299
Width : 4.355
Height : 10.083
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ampl
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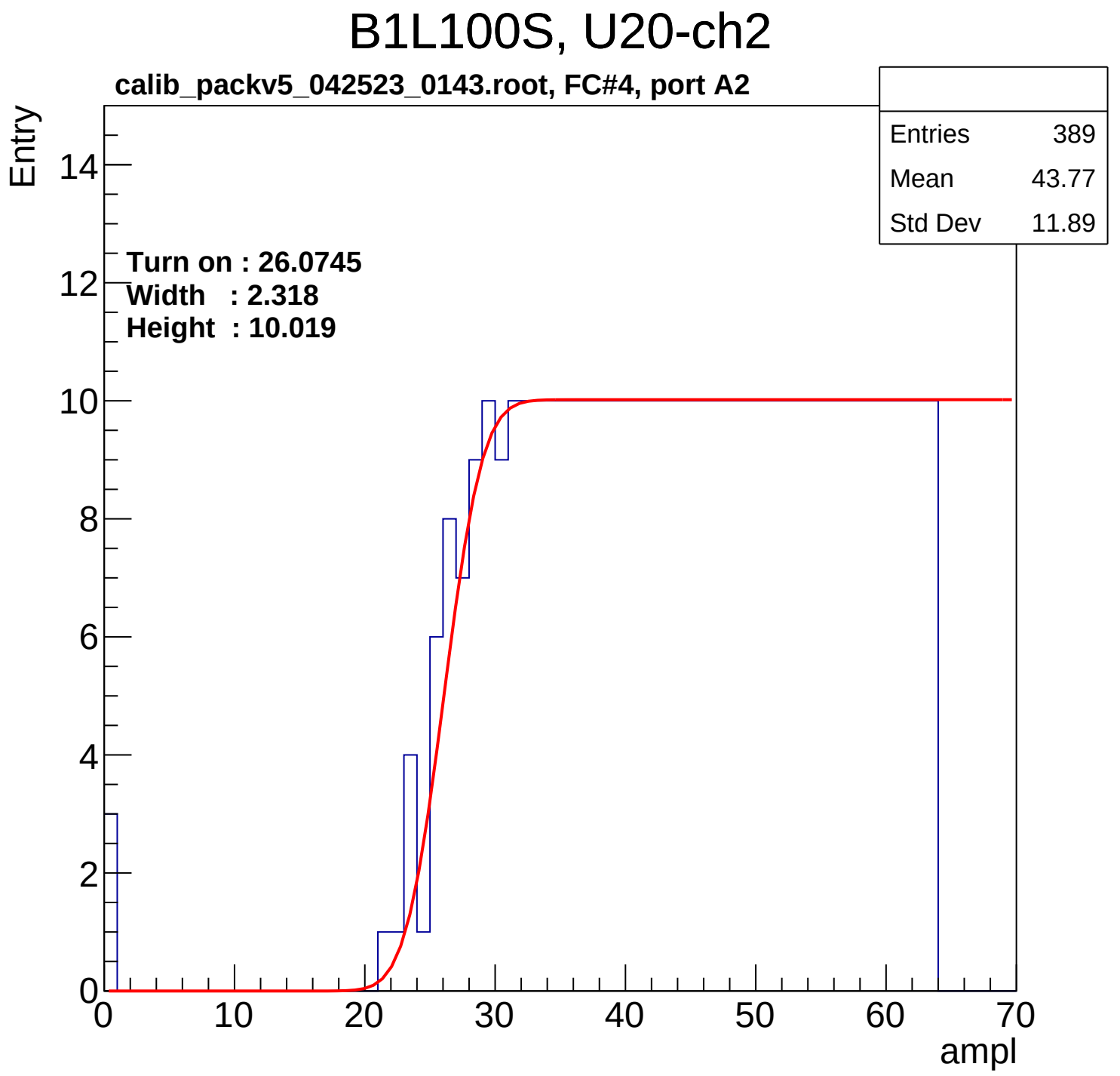
B1L100S, U20-ch2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 389
Mean 43.77
Std Dev 11.89
Turn on : 26.0745
Width : 2.318
Height : 10.019
Entry
ampl
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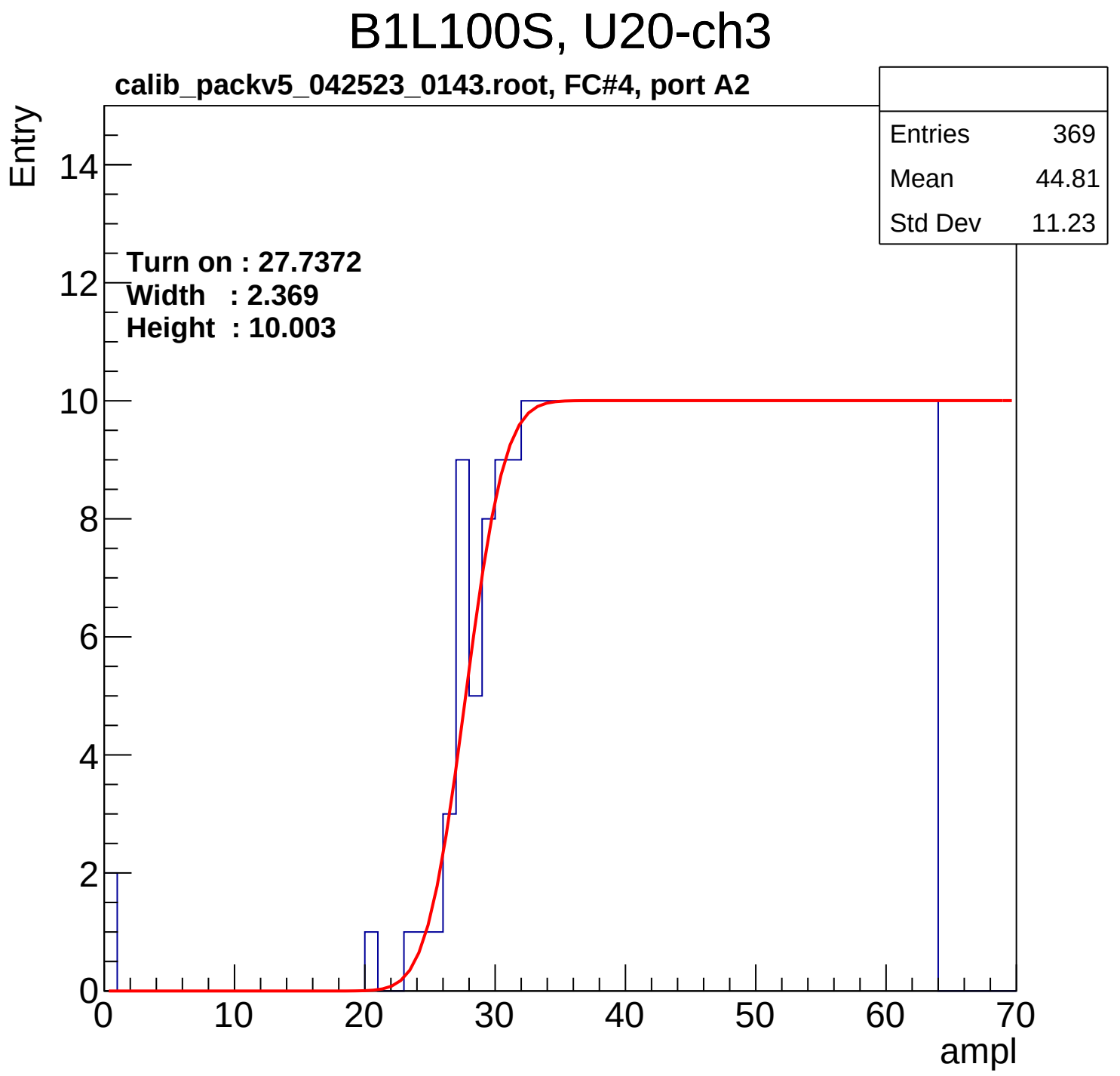
B1L100S, U20-ch3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 369
Mean 44.81
Std Dev 11.23
Turn on : 27.7372
Width : 2.369
Height : 10.003
Entry
ampl
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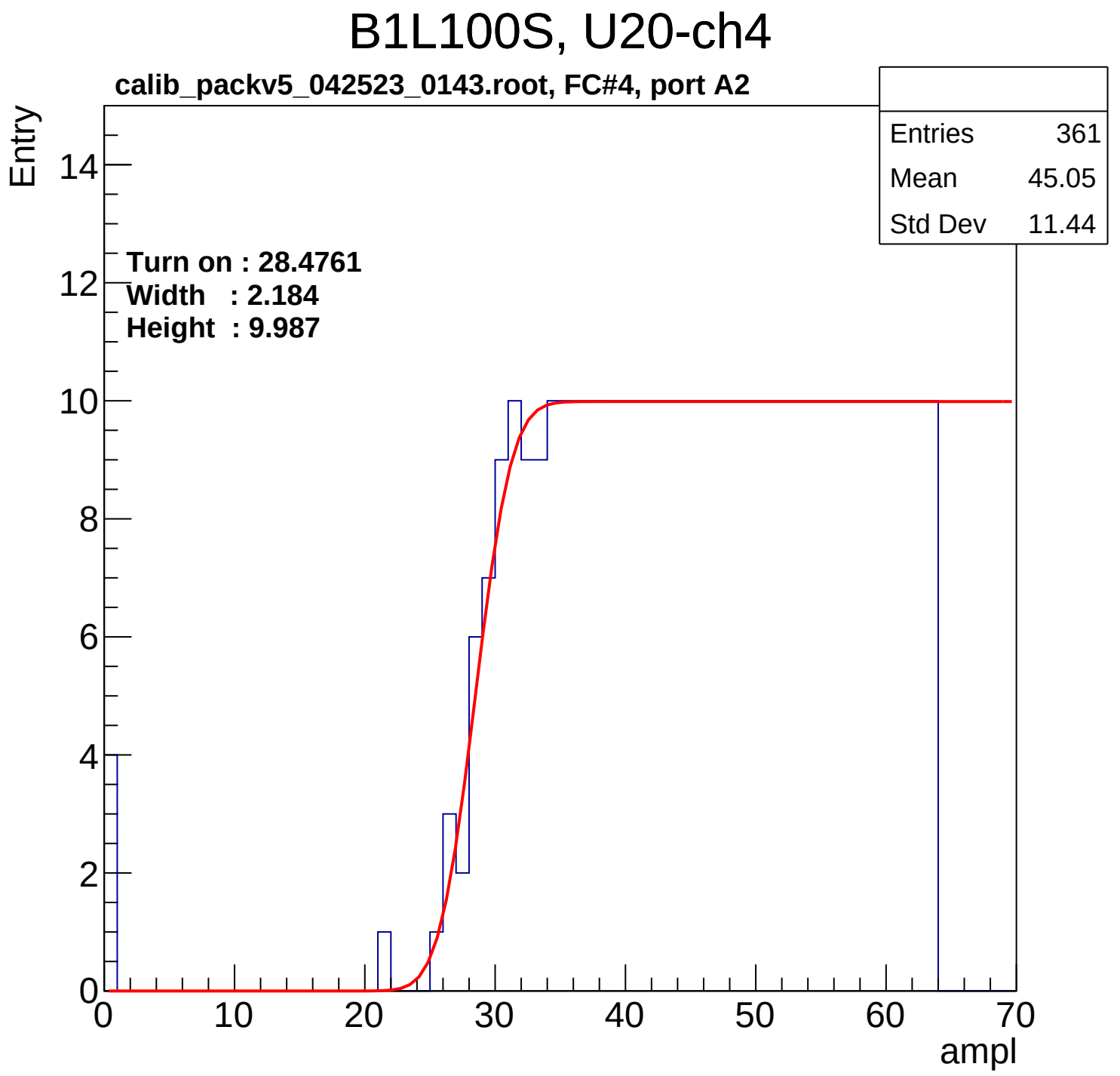
B1L100S, U20-ch4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 361
Mean 45.05
Std Dev 11.44
Turn on : 28.4761
Width : 2.184
Height : 9.987
Entry
ampl
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6
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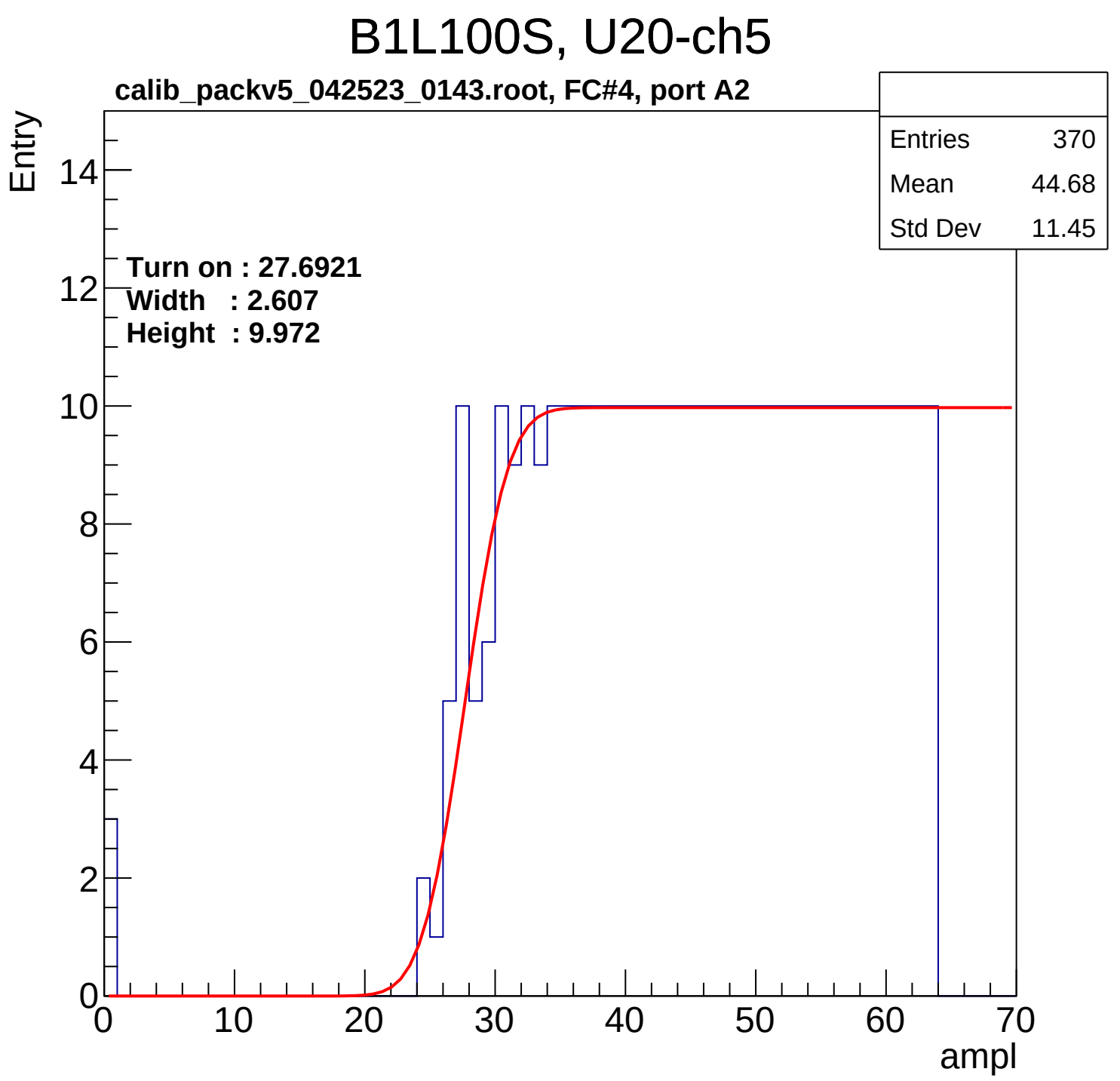
B1L100S, U20-ch5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 370
Mean 44.68
Std Dev 11.45
Turn on : 27.6921
Width : 2.607
Height : 9.972
Entry
ampl
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2
4
6
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0
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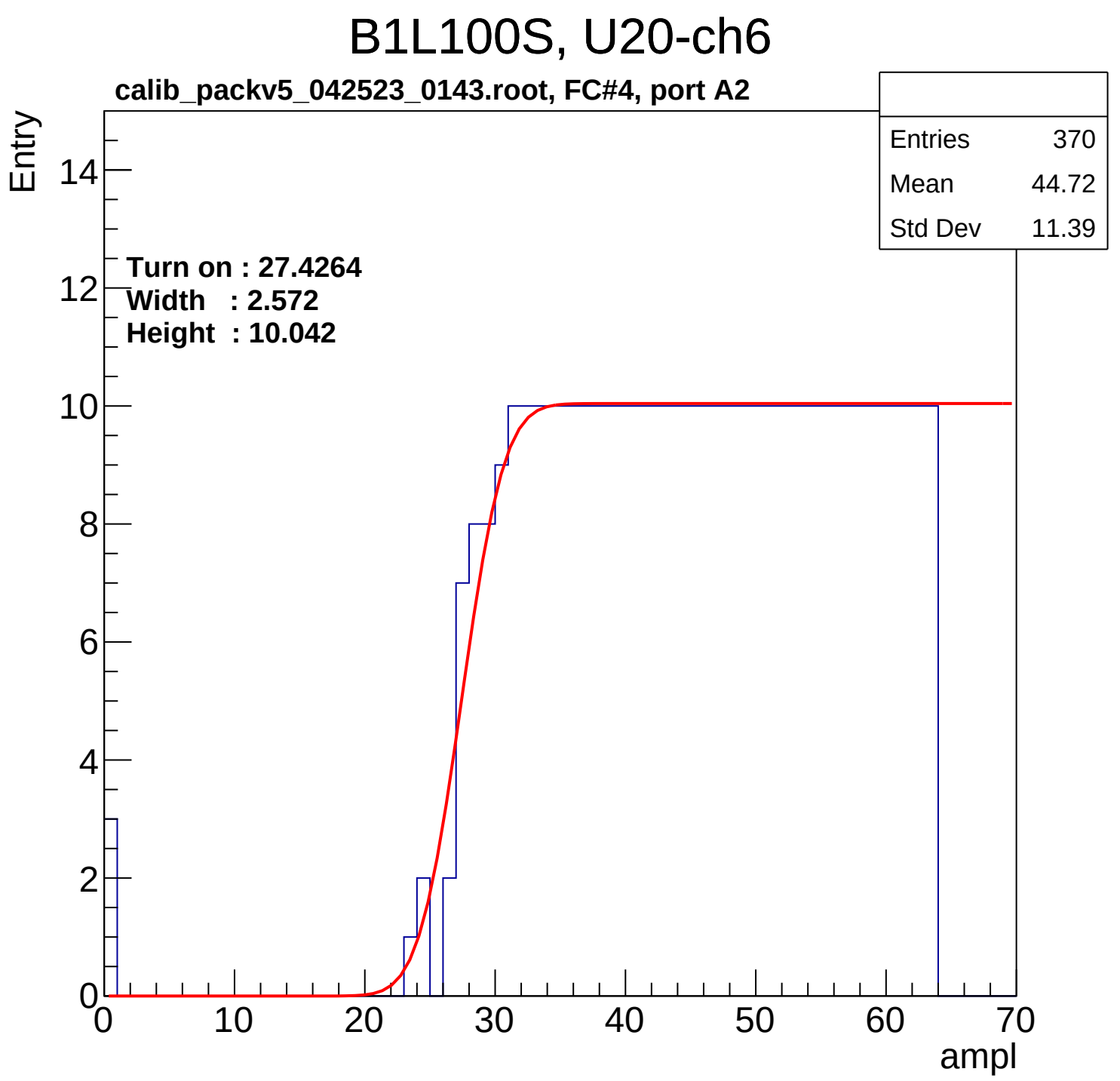
B1L100S, U20-ch6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 370
Mean 44.72
Std Dev 11.39
Turn on : 27.4264
Width : 2.572
Height : 10.042
Entry
ampl
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2
4
6
8
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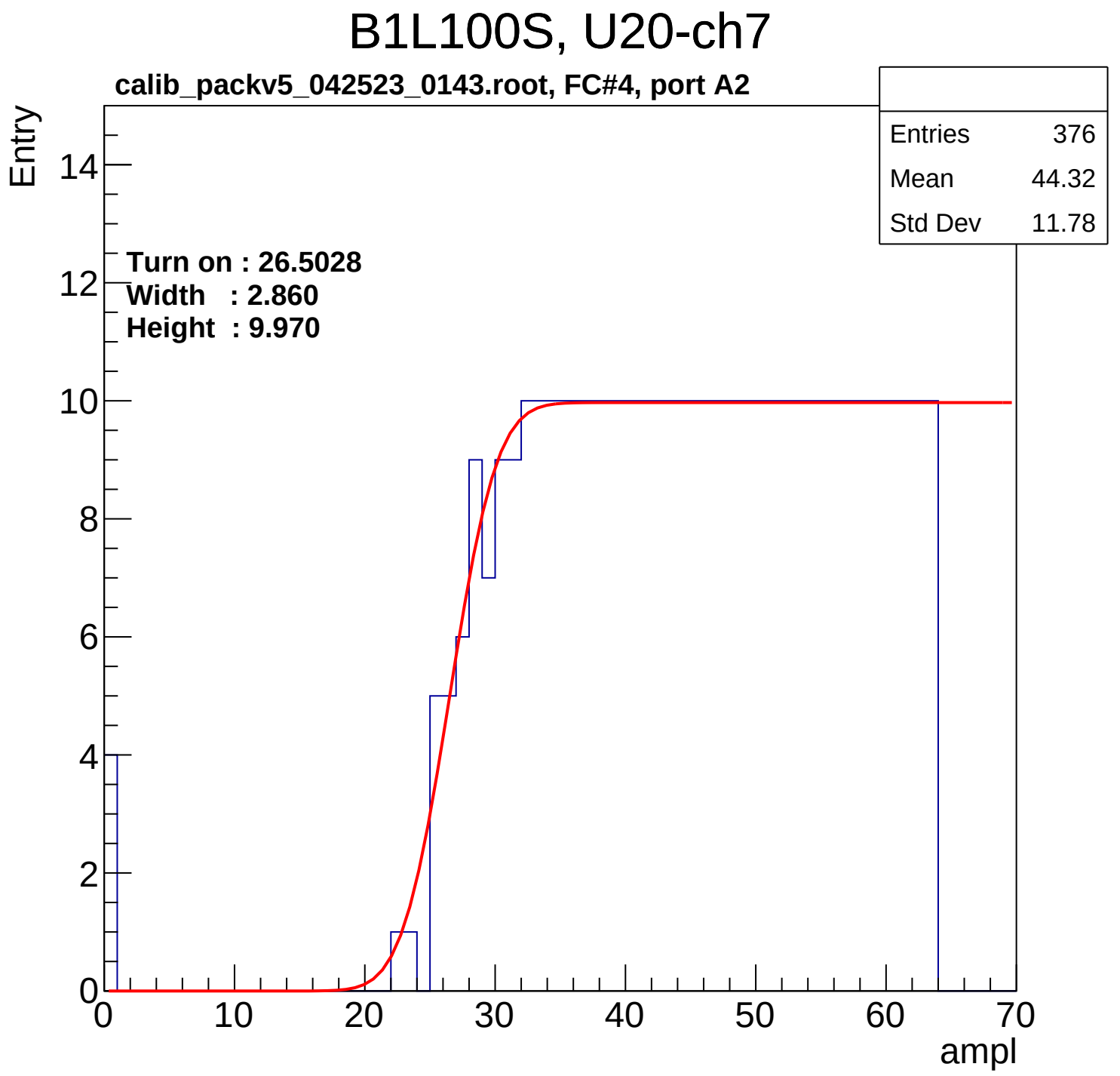
B1L100S, U20-ch7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 376
Mean 44.32
Std Dev 11.78
Turn on : 26.5028
Width : 2.860
Height : 9.970
Entry
ampl
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2
4
6
8
10
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0
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60
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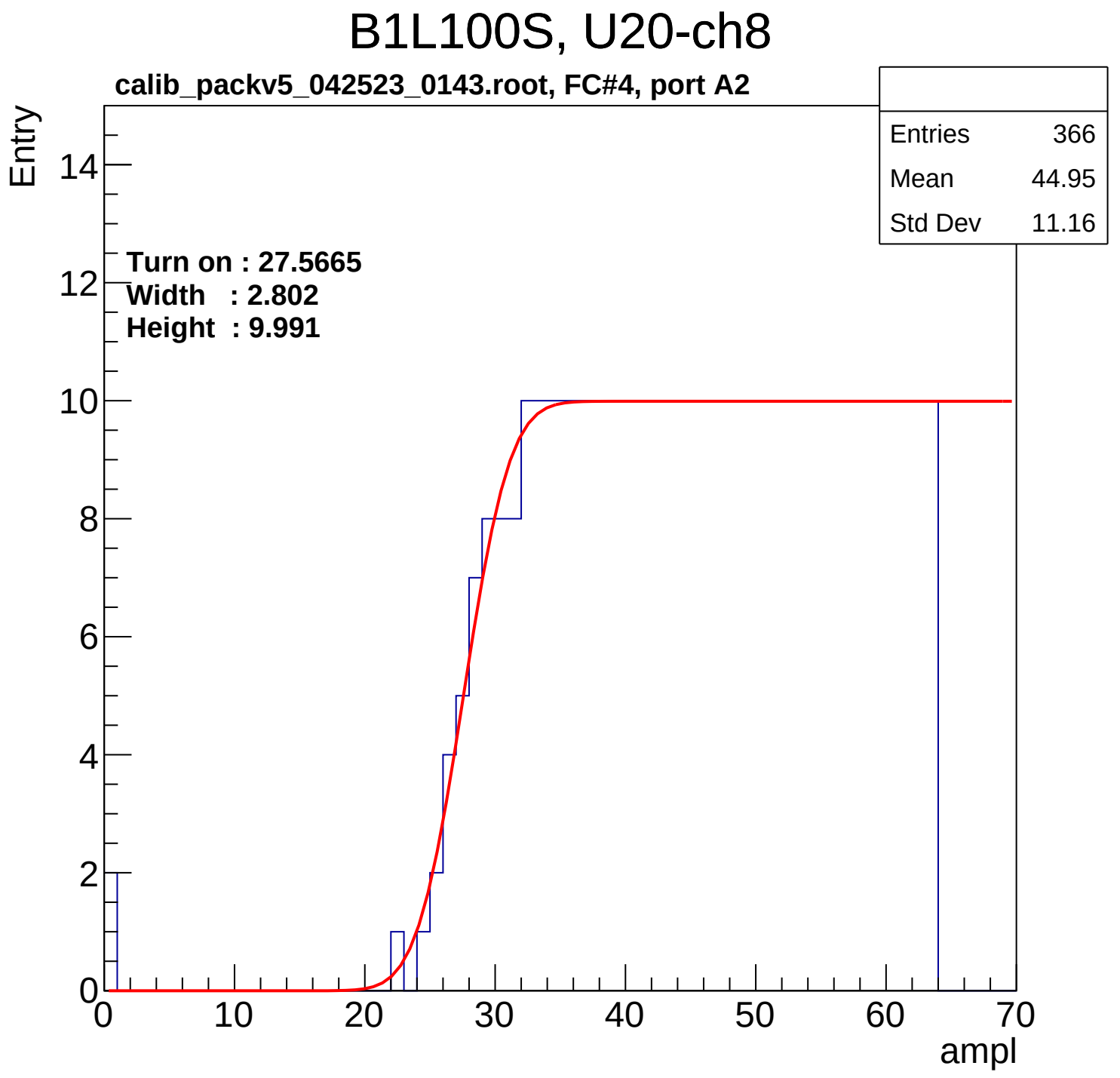
B1L100S, U20-ch8
calib_packv5_042523_0143.root, FC#4, port A2
Entries 366
Mean 44.95
Std Dev 11.16
Turn on : 27.5665
Width : 2.802
Height : 9.991
Entry
ampl
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4
6
8
10
12
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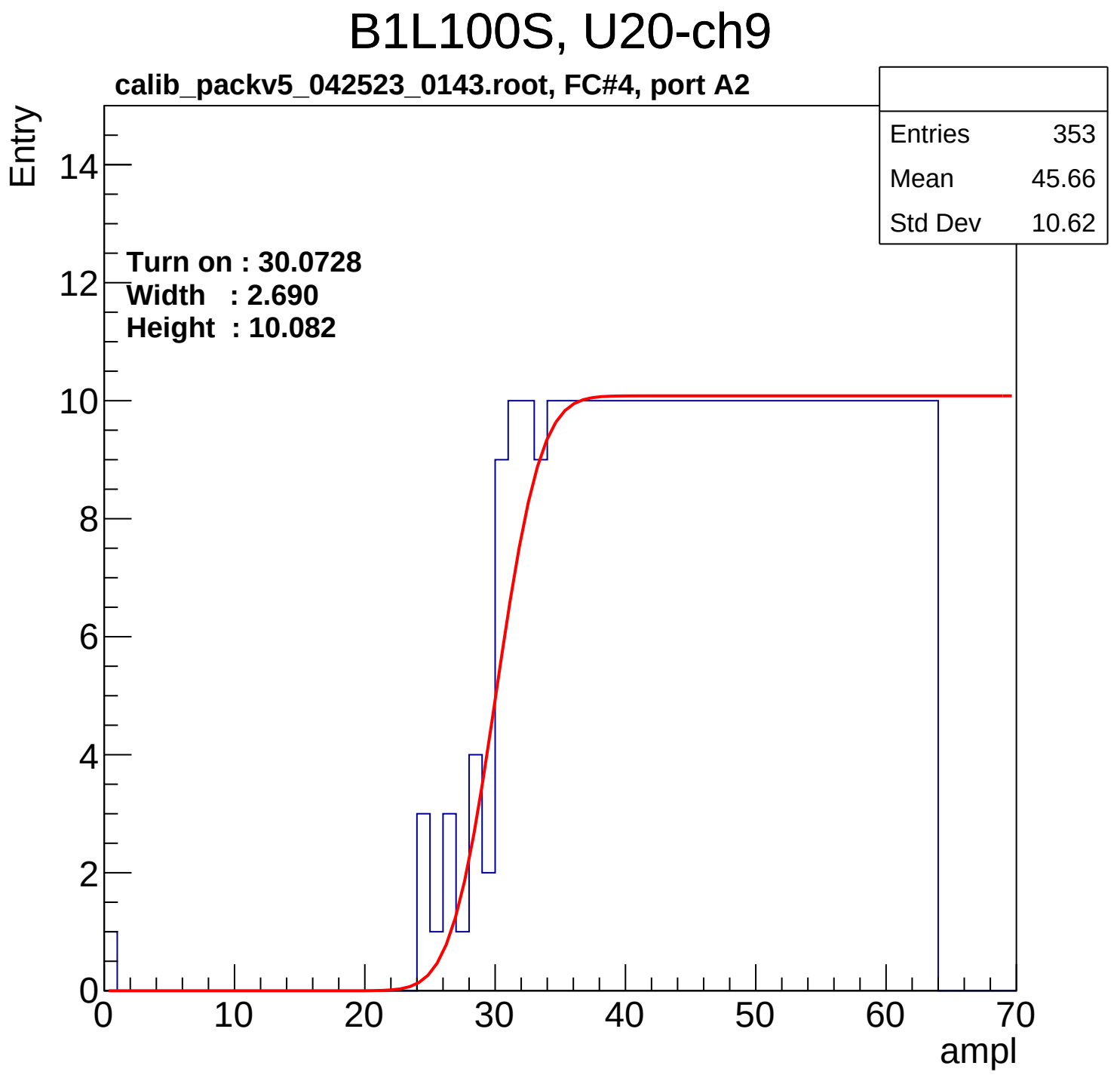
B1L100S, U20-ch9
calib_packv5_042523_0143.root, FC#4, port A2
Entries 353
Mean 45.66
Std Dev 10.62
Turn on : 30.0728
Width : 2.690
Height : 10.082
Entry
ampl
0
2
4
6
8
10
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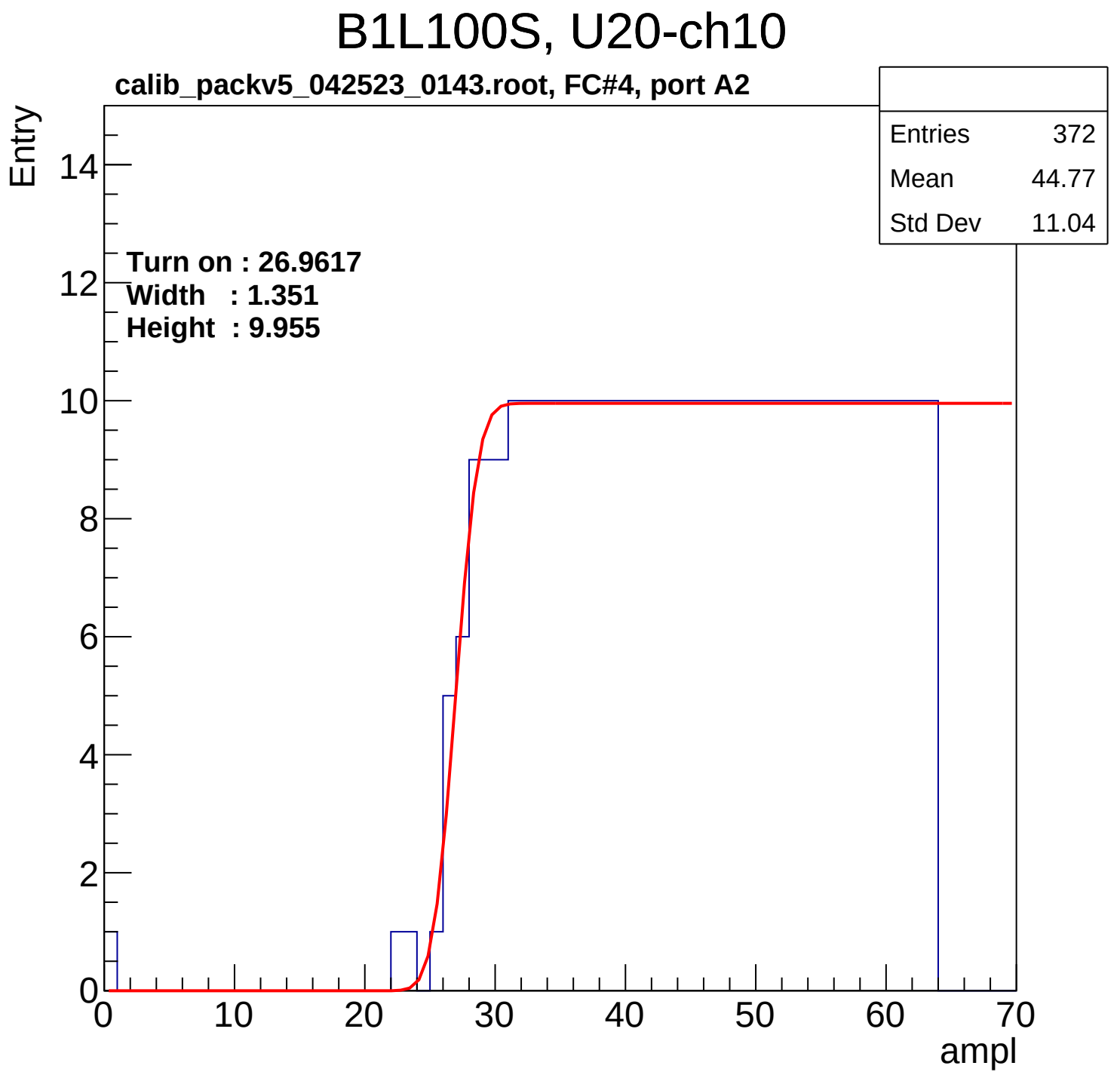
B1L100S, U20-ch10
calib_packv5_042523_0143.root, FC#4, port A2
Entries 372
Mean 44.77
Std Dev 11.04
Turn on : 26.9617
Width : 1.351
Height : 9.955
Entry
ampl
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6
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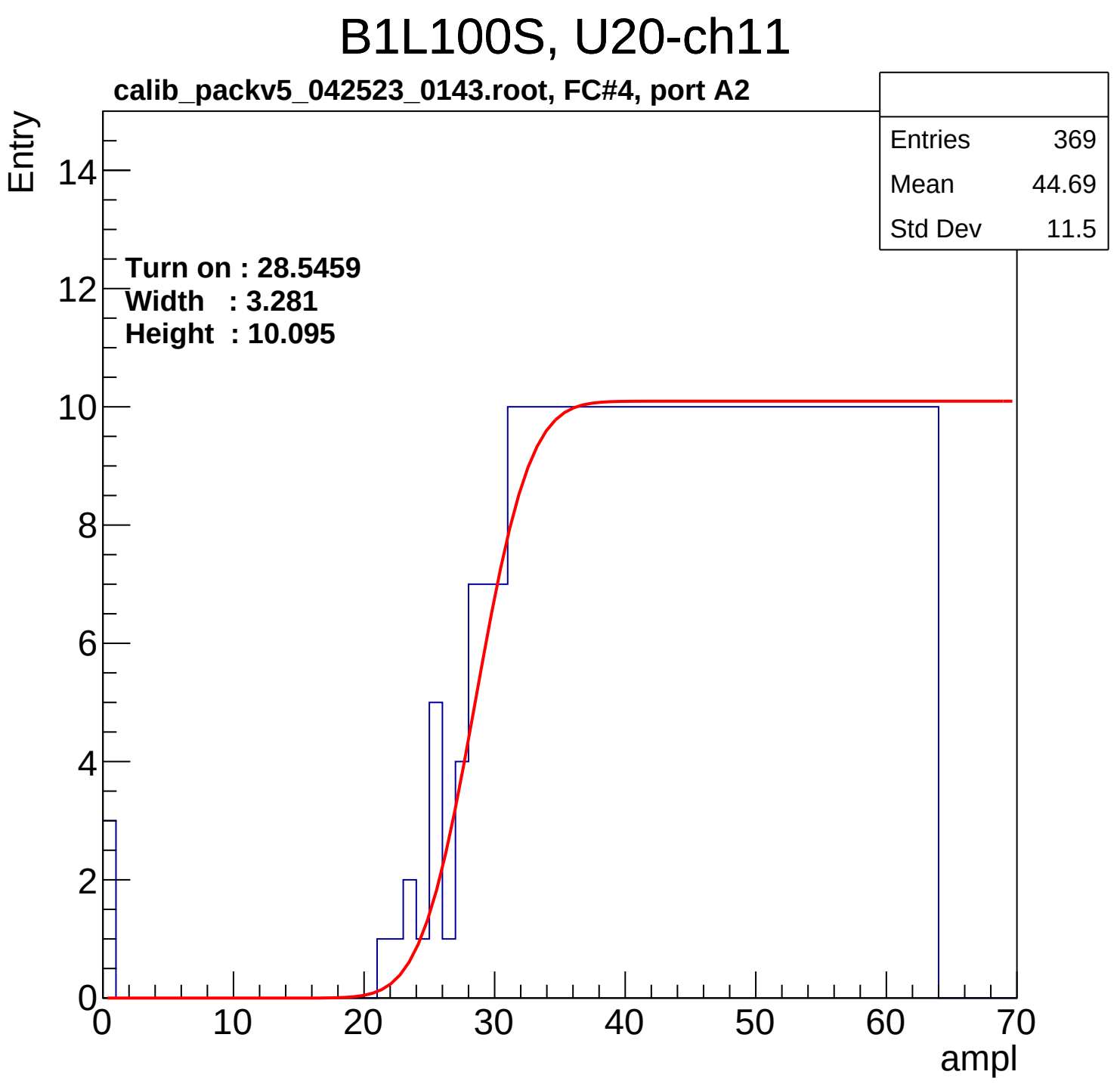
B1L100S, U20-ch11
calib_packv5_042523_0143.root, FC#4, port A2
Entries 369
Mean 44.69
Std Dev 11.5
Turn on : 28.5459
Width : 3.281
Height : 10.095
Entry
ampl
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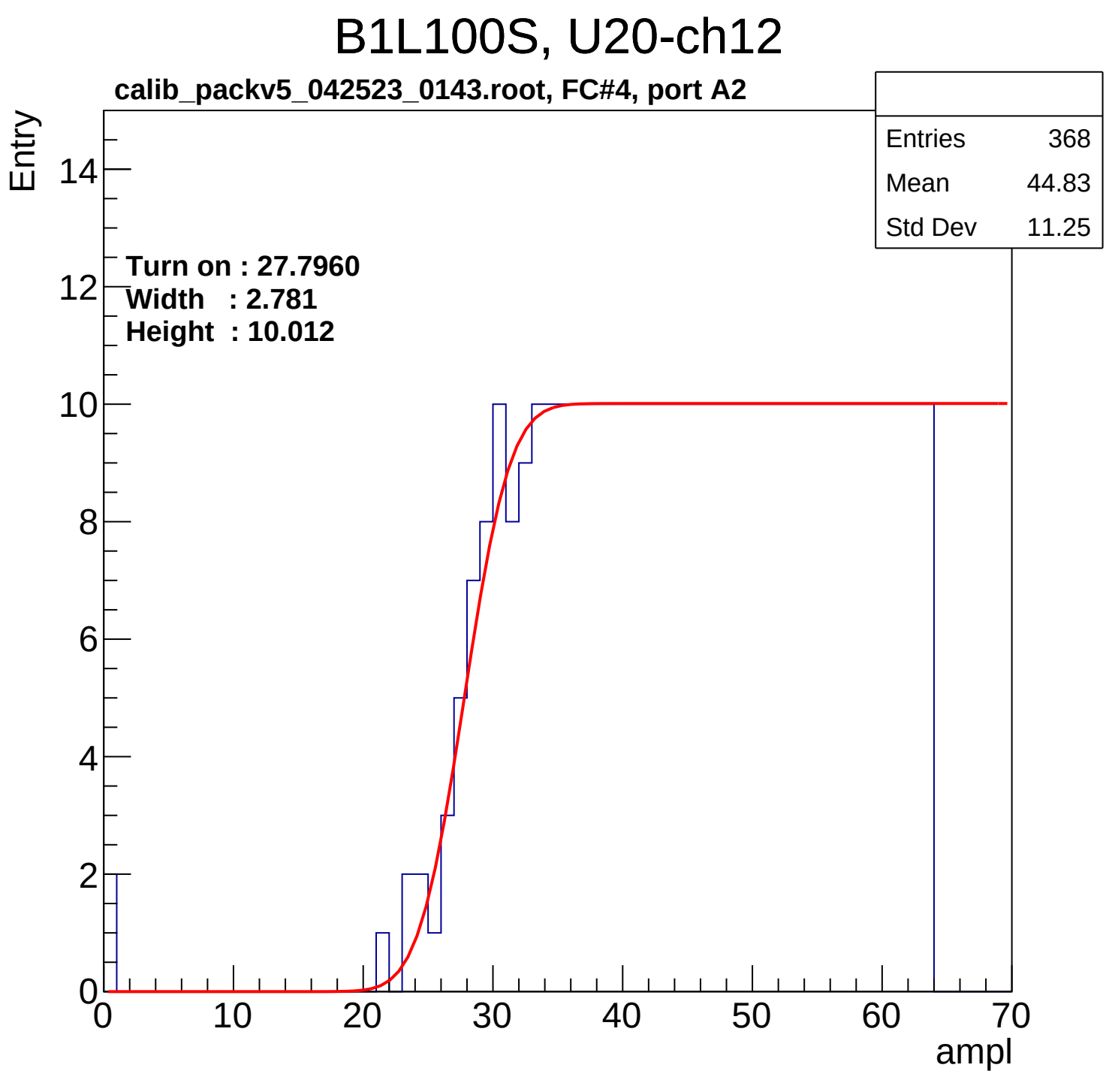
B1L100S, U20-ch12
calib_packv5_042523_0143.root, FC#4, port A2
Entries 368
Mean 44.83
Std Dev 11.25
Turn on : 27.7960
Width : 2.781
Height : 10.012
Entry
ampl
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2
4
6
8
10
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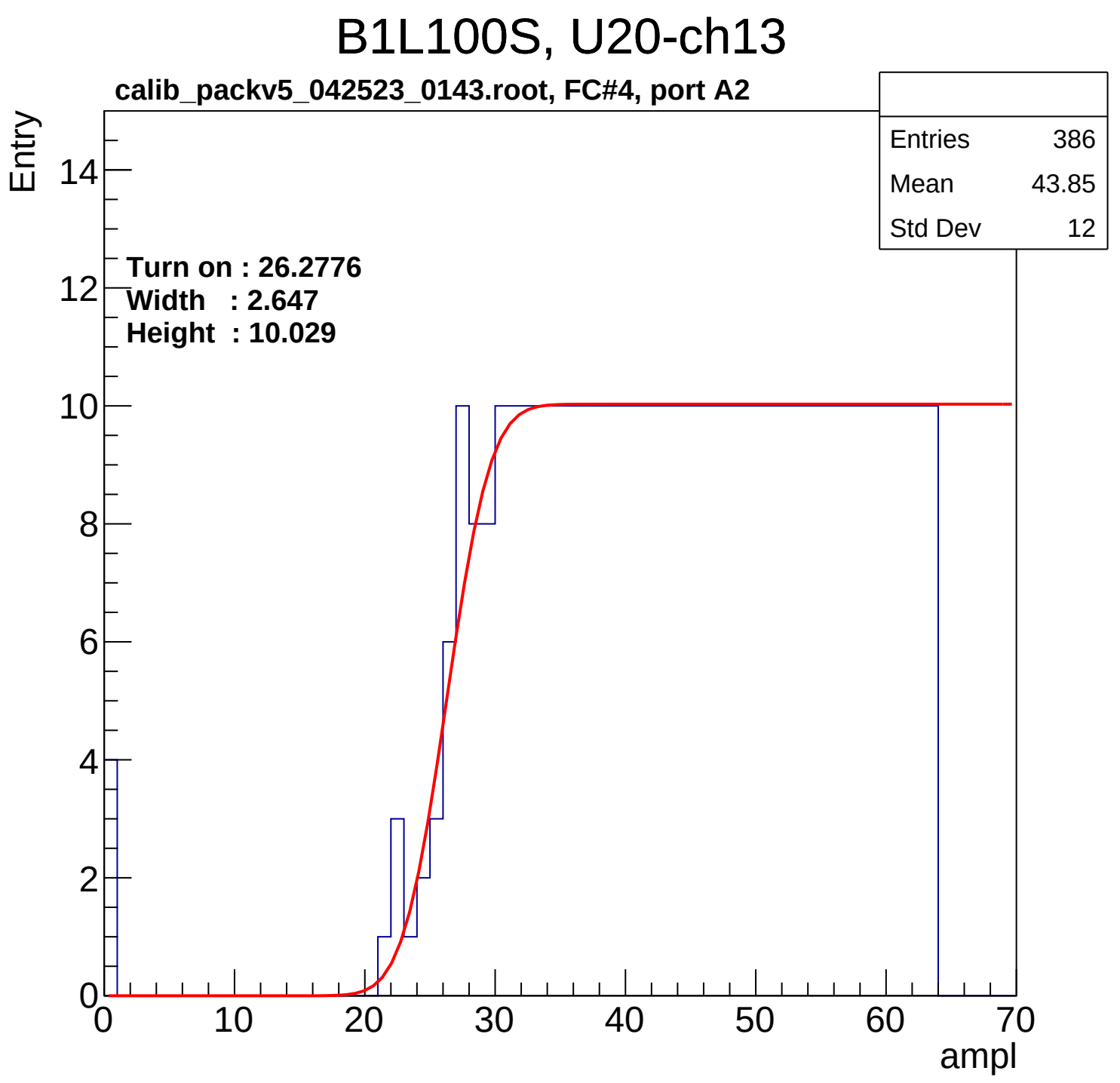
B1L100S, U20-ch13
calib_packv5_042523_0143.root, FC#4, port A2
Entries 386
Mean 43.85
Std Dev 12
Turn on : 26.2776
Width : 2.647
Height : 10.029
Entry
ampl
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6
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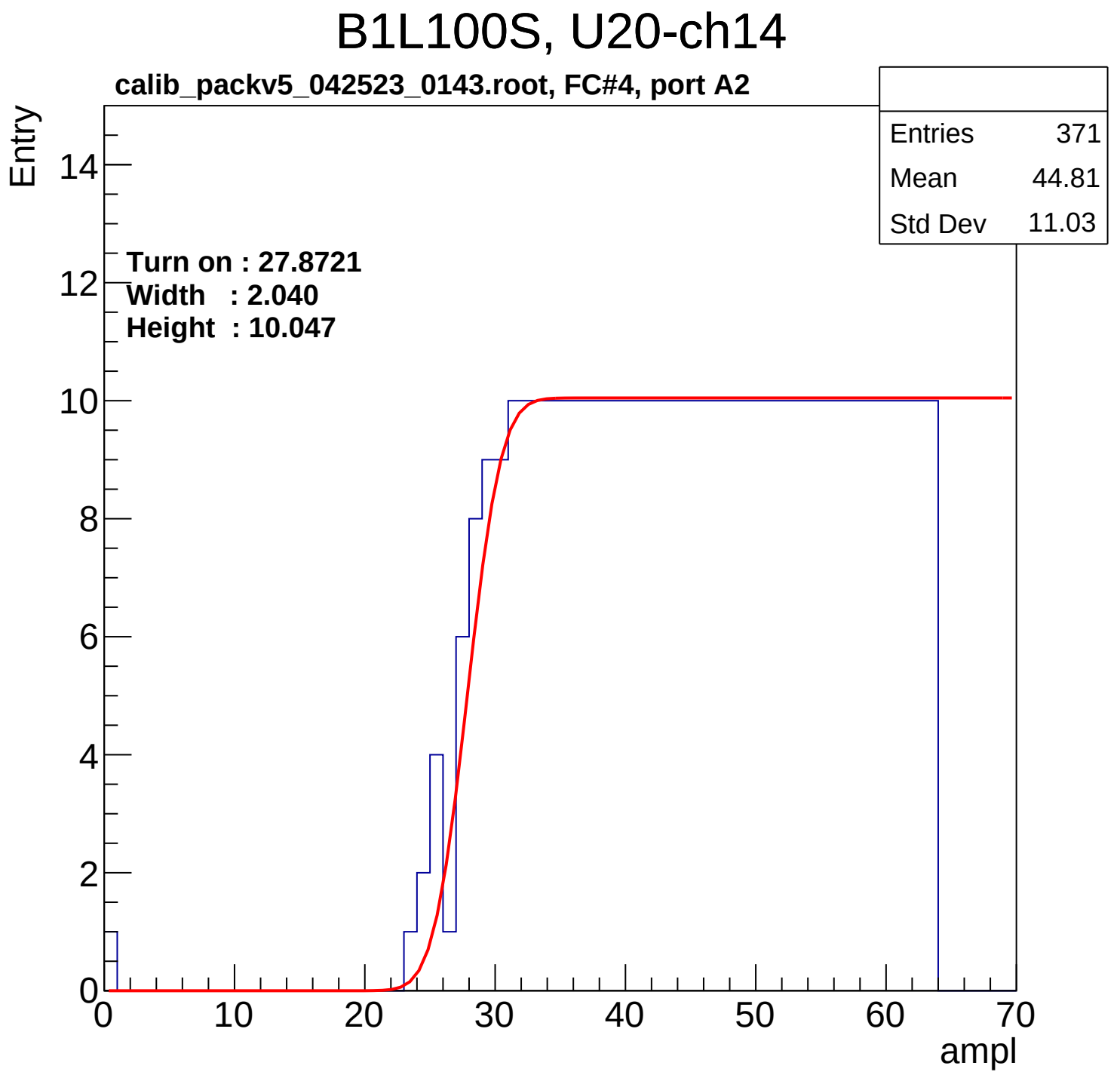
B1L100S, U20-ch14
calib_packv5_042523_0143.root, FC#4, port A2
Entries 371
Mean 44.81
Std Dev 11.03
Turn on : 27.8721
Width : 2.040
Height : 10.047
Entry
ampl
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6
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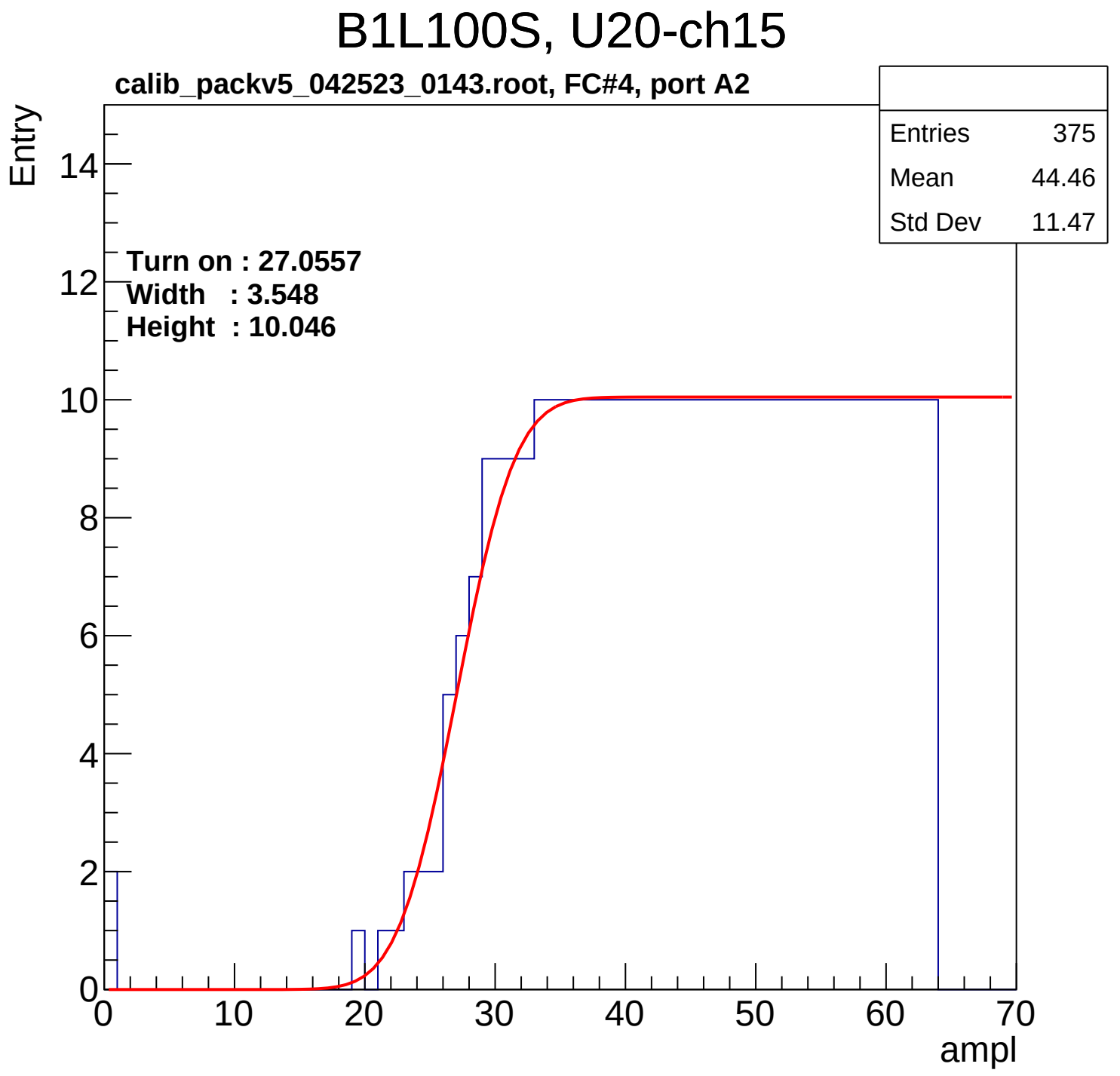
B1L100S, U20-ch15
calib_packv5_042523_0143.root, FC#4, port A2
Entries 375
Mean 44.46
Std Dev 11.47
Turn on : 27.0557
Width : 3.548
Height : 10.046
Entry
ampl
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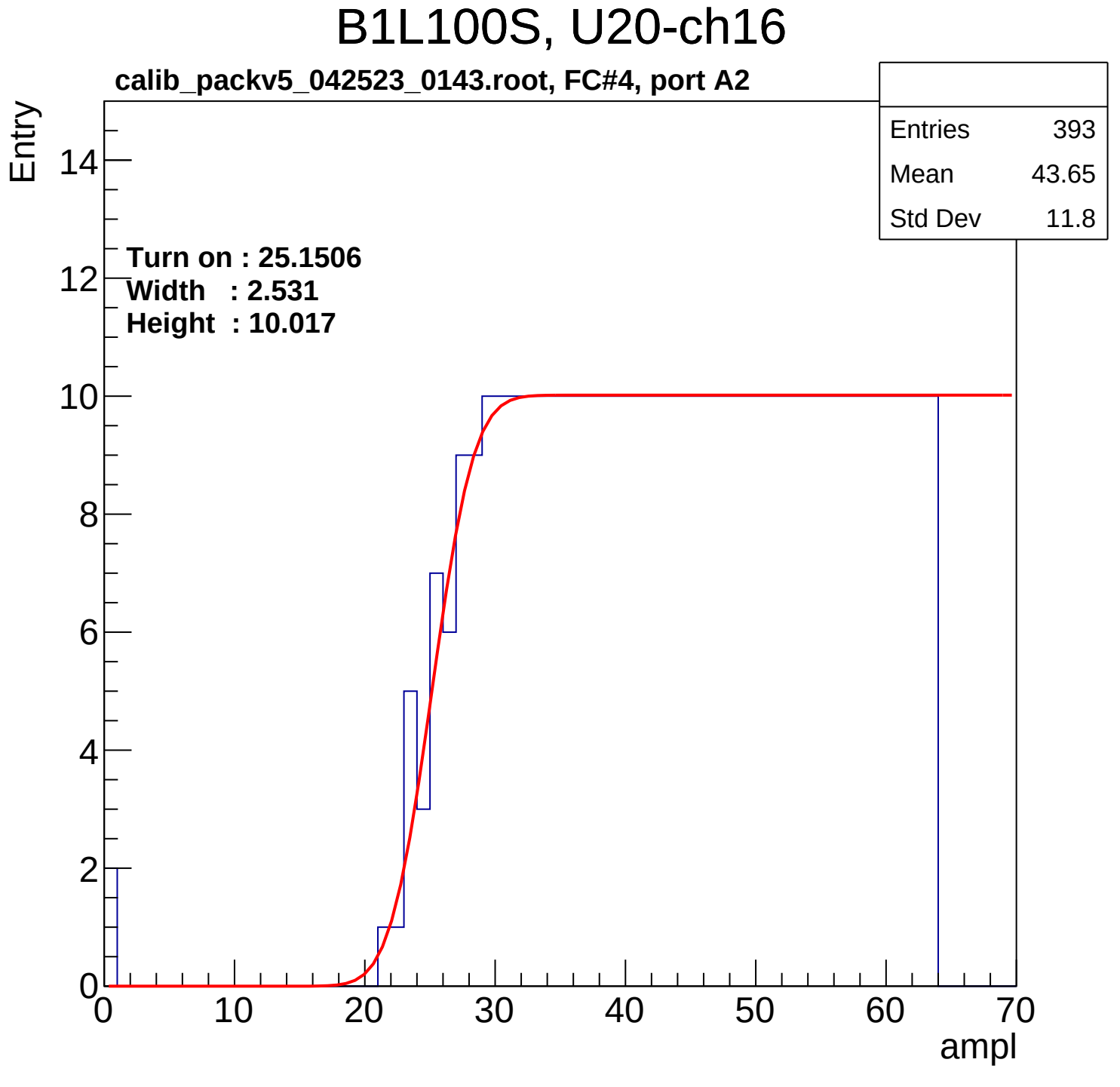
B1L100S, U20-ch16
calib_packv5_042523_0143.root, FC#4, port A2
Entries 393
Mean 43.65
Std Dev 11.8
Turn on : 25.1506
Width : 2.531
Height : 10.017
Entry
ampl
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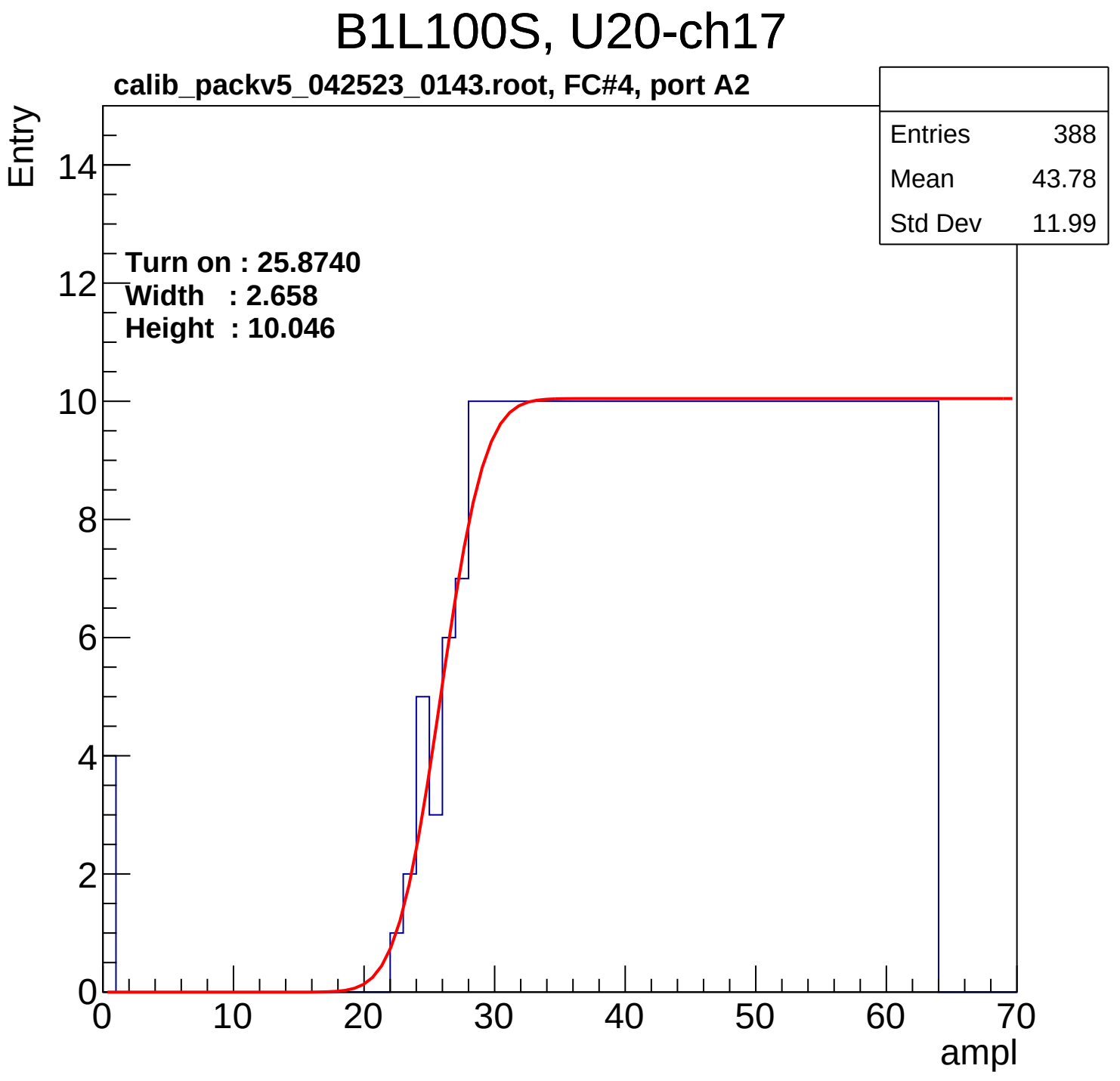
B1L100S, U20-ch17
calib_packv5_042523_0143.root, FC#4, port A2
Entries 388
Mean 43.78
Std Dev 11.99
Turn on : 25.8740
Width : 2.658
Height : 10.046
Entry
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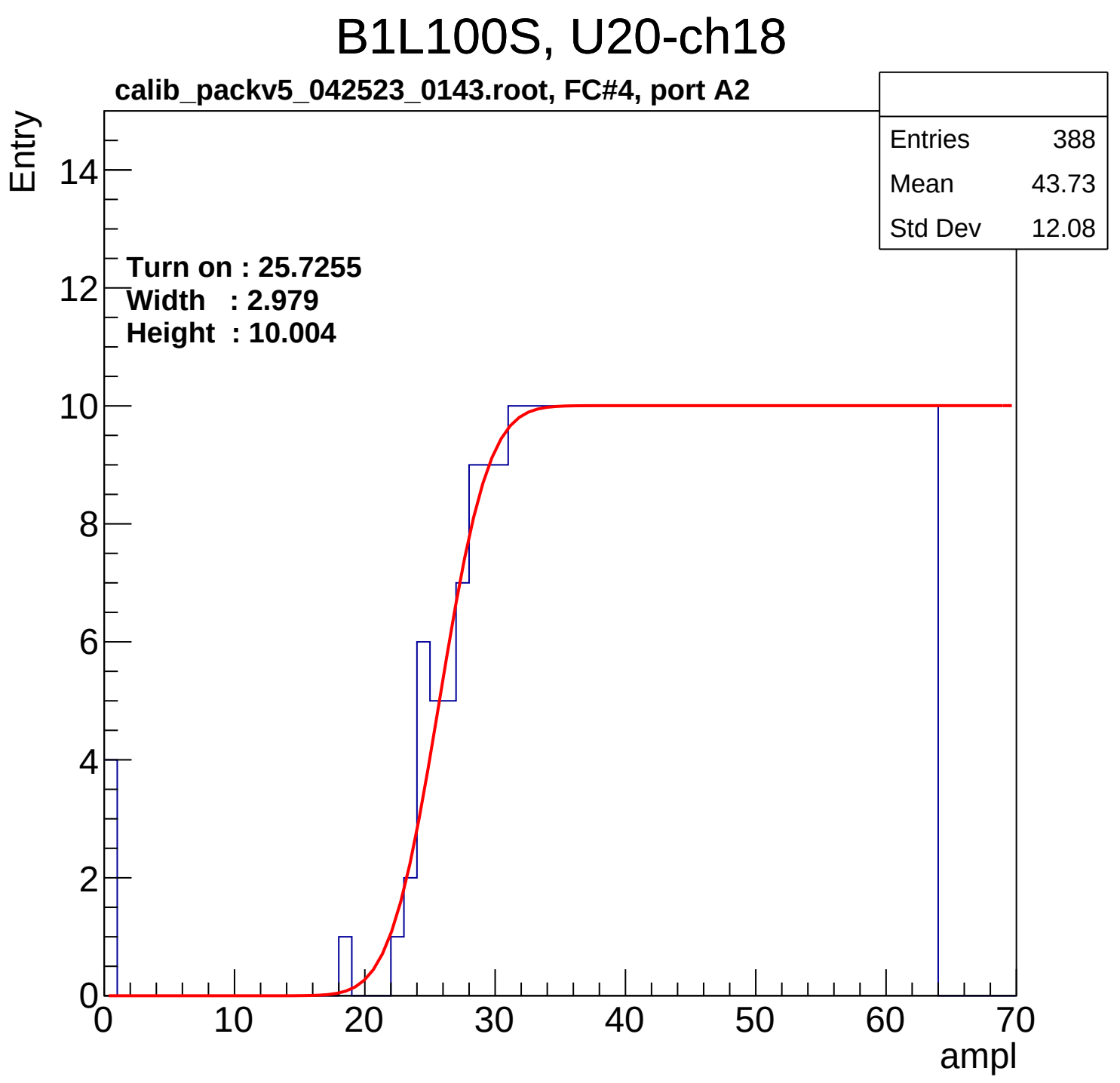
B1L100S, U20-ch18
calib_packv5_042523_0143.root, FC#4, port A2
Entries 388
Mean 43.73
Std Dev 12.08
Turn on : 25.7255
Width : 2.979
Height : 10.004
Entry
ampl
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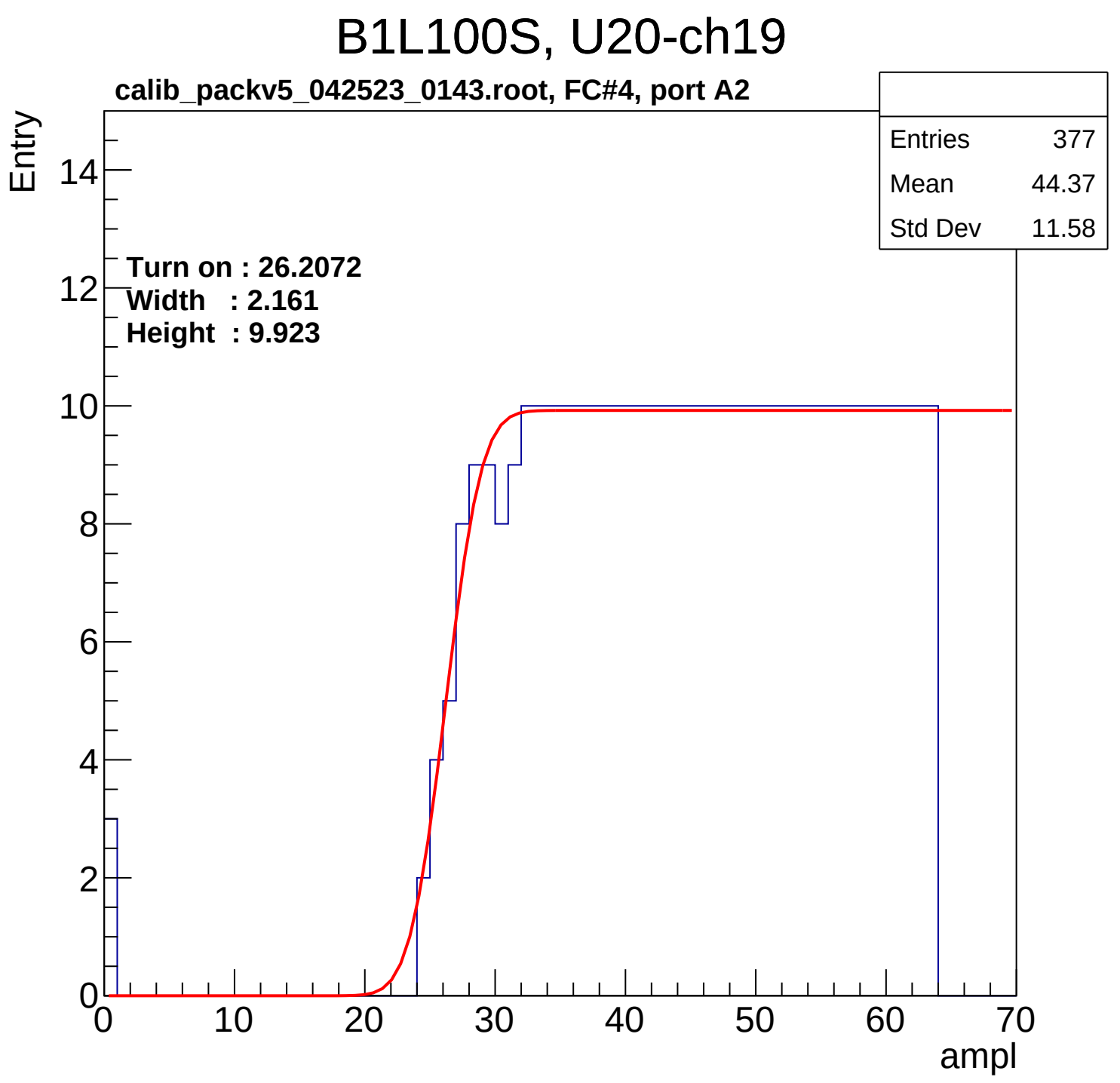
B1L100S, U20-ch19
calib_packv5_042523_0143.root, FC#4, port A2
Entries 377
Mean 44.37
Std Dev 11.58
Turn on : 26.2072
Width : 2.161
Height : 9.923
Entry
ampl
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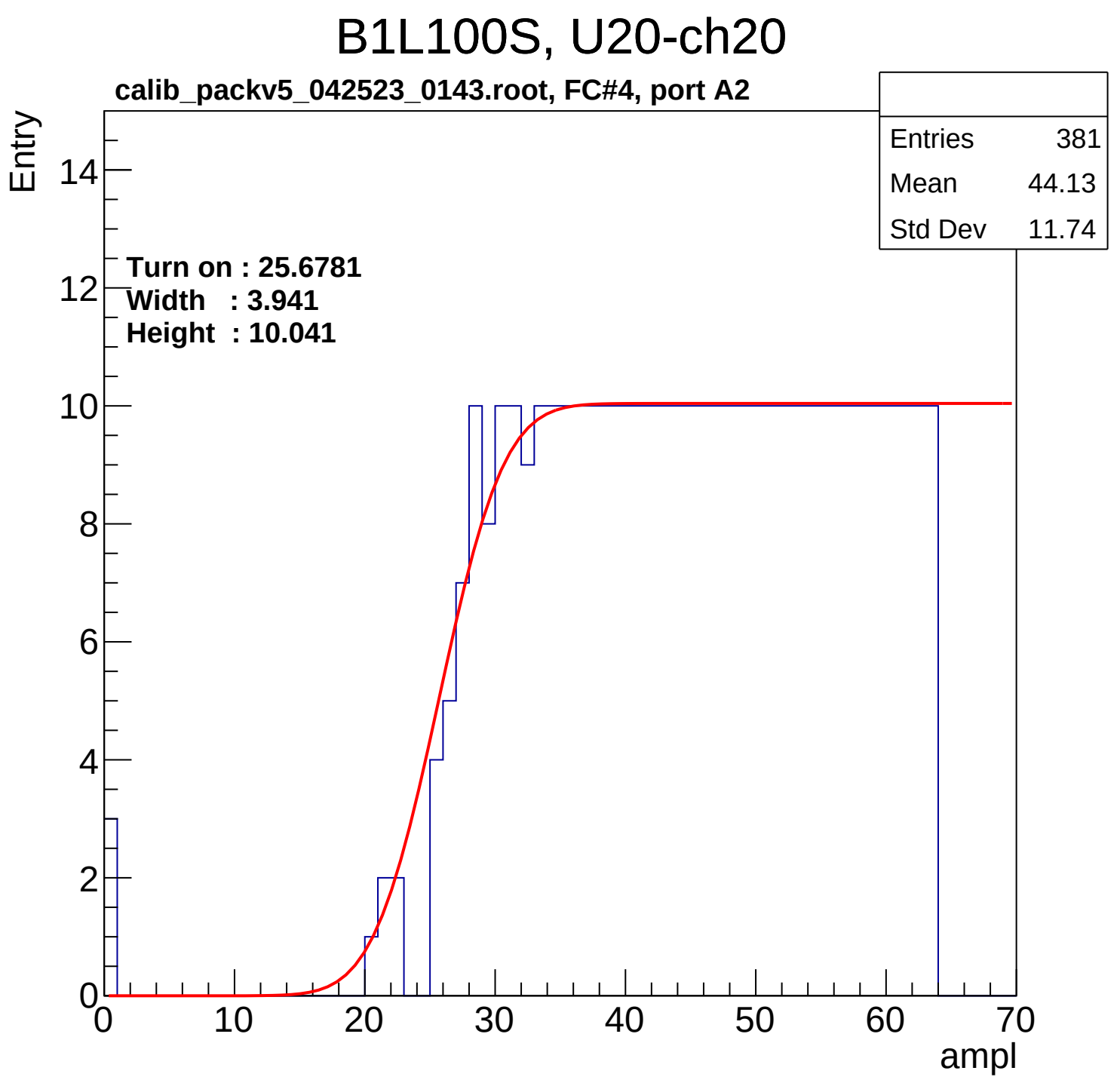
B1L100S, U20-ch20
calib_packv5_042523_0143.root, FC#4, port A2
Entries 381
Mean 44.13
Std Dev 11.74
Turn on : 25.6781
Width : 3.941
Height : 10.041
Entry
ampl
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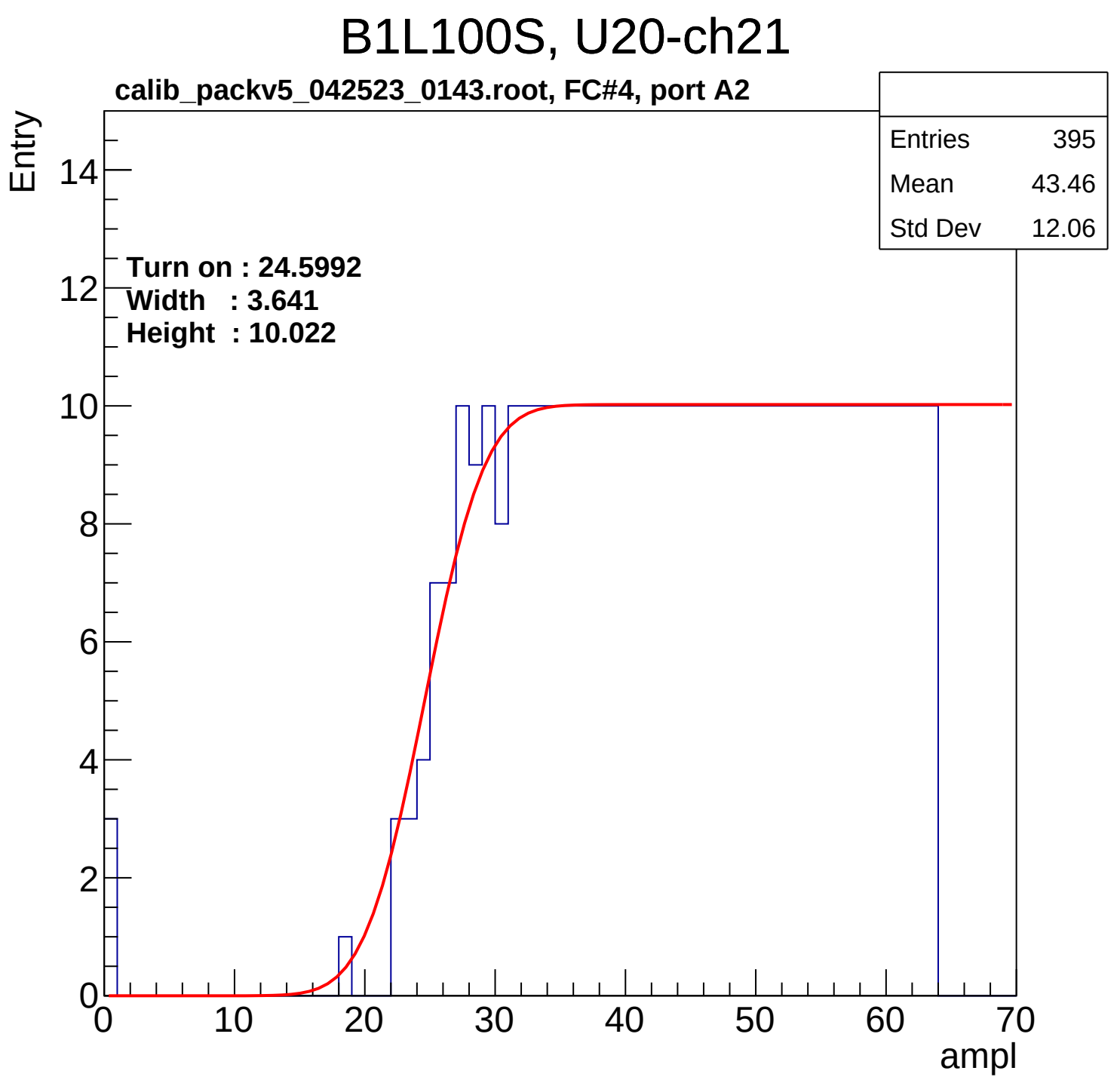
B1L100S, U20-ch21
calib_packv5_042523_0143.root, FC#4, port A2
Entries 395
Mean 43.46
Std Dev 12.06
Turn on : 24.5992
Width : 3.641
Height : 10.022
Entry
ampl
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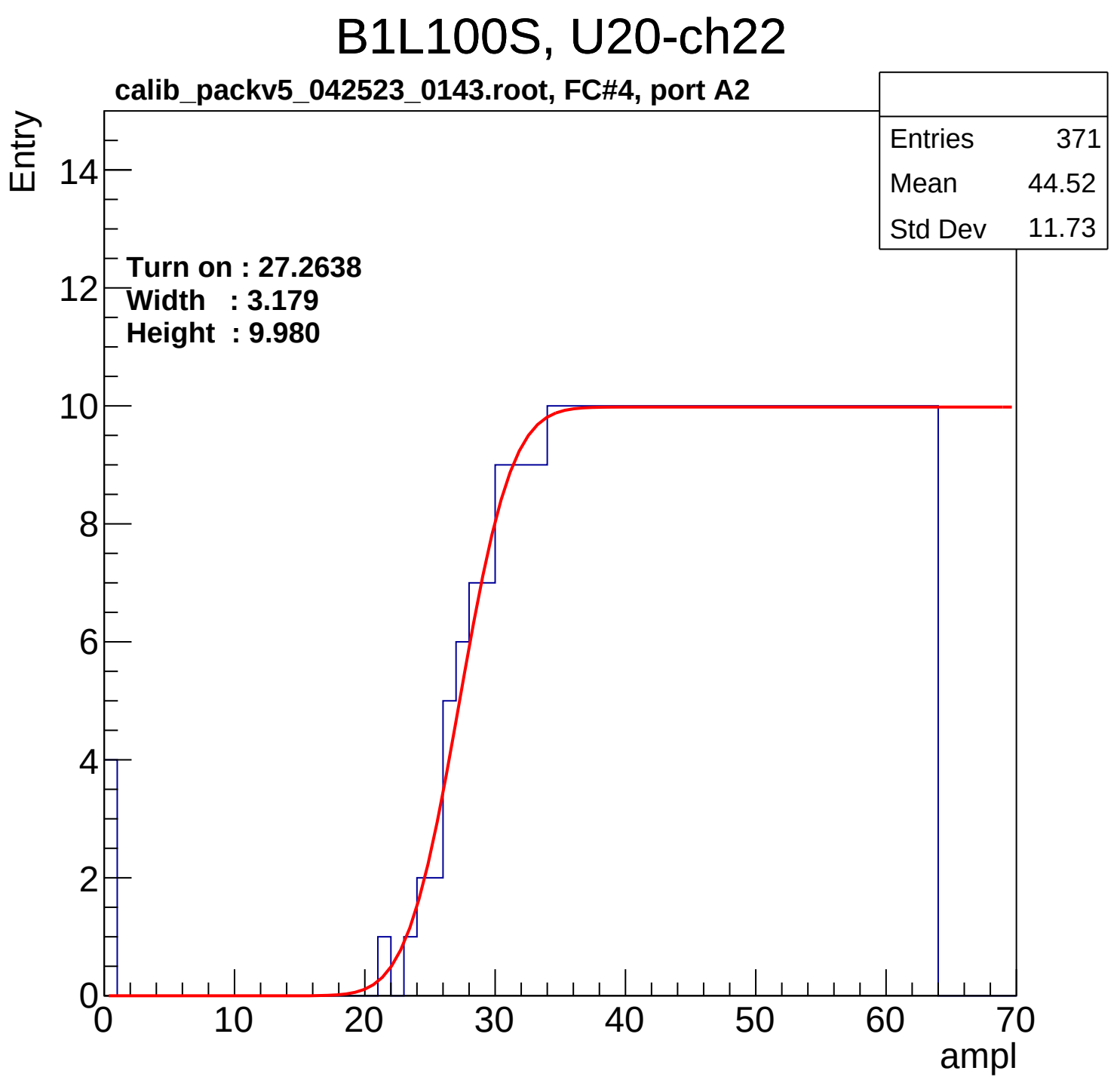
B1L100S, U20-ch22
calib_packv5_042523_0143.root, FC#4, port A2
Entries 371
Mean 44.52
Std Dev 11.73
Turn on : 27.2638
Width : 3.179
Height : 9.980
Entry
ampl
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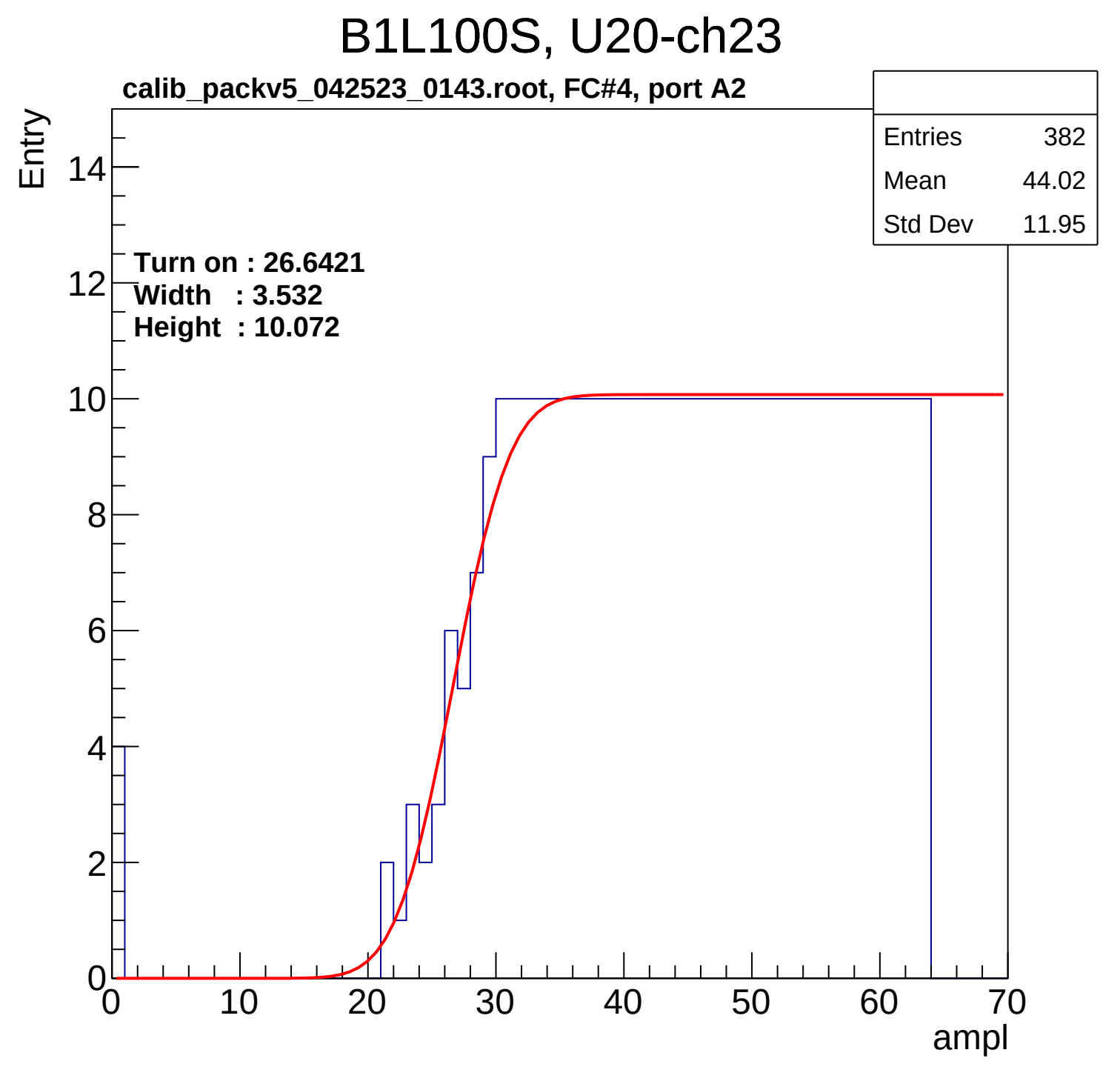
B1L100S, U20-ch23
calib_packv5_042523_0143.root, FC#4, port A2
Entries 382
Mean 44.02
Std Dev 11.95
Turn on : 26.6421
Width : 3.532
Height : 10.072
Entry
ampl
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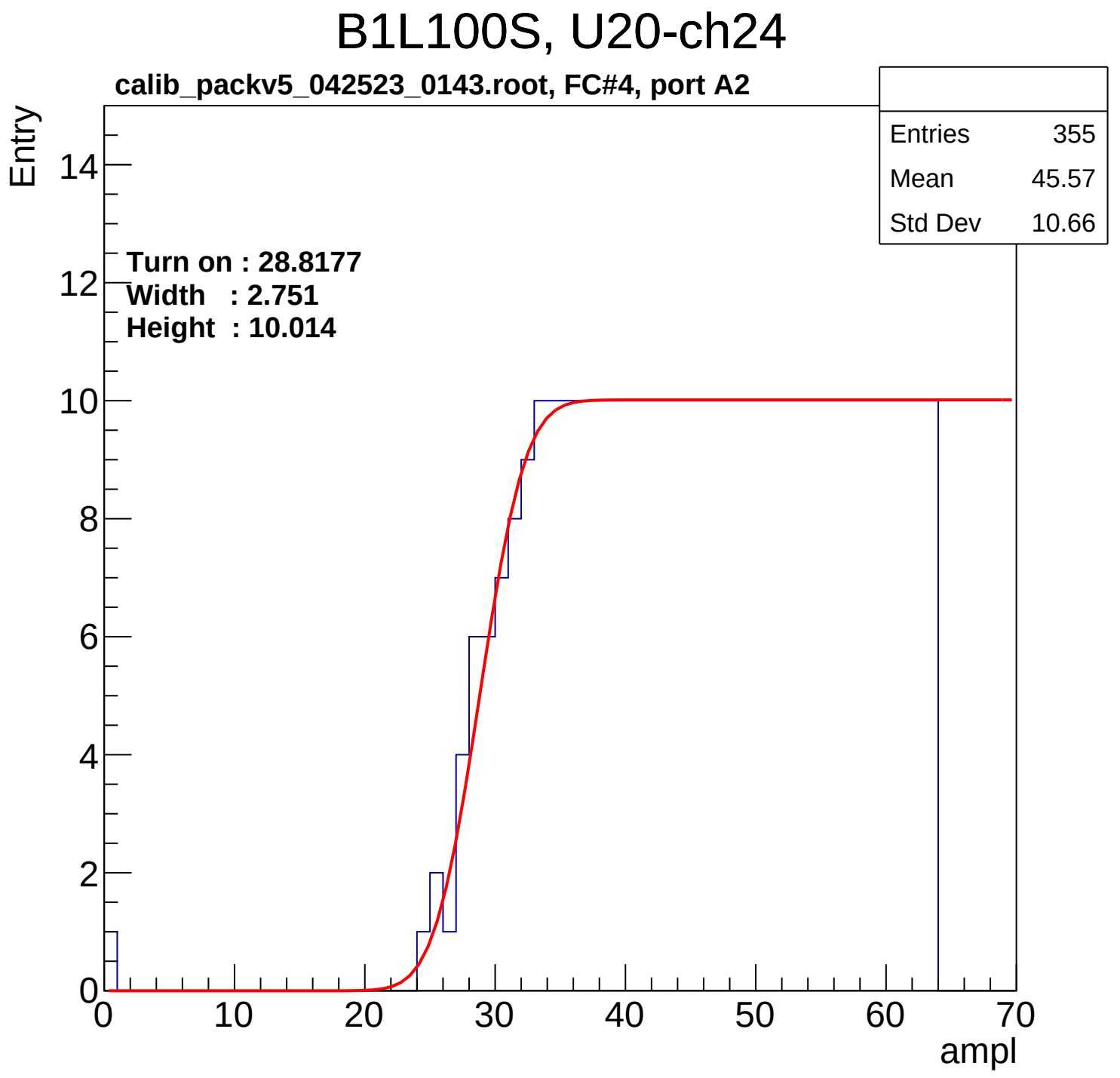
B1L100S, U20-ch24
calib_packv5_042523_0143.root, FC#4, port A2
Entries 355
Mean 45.57
Std Dev 10.66
Turn on : 28.8177
Width : 2.751
Height : 10.014
Entry
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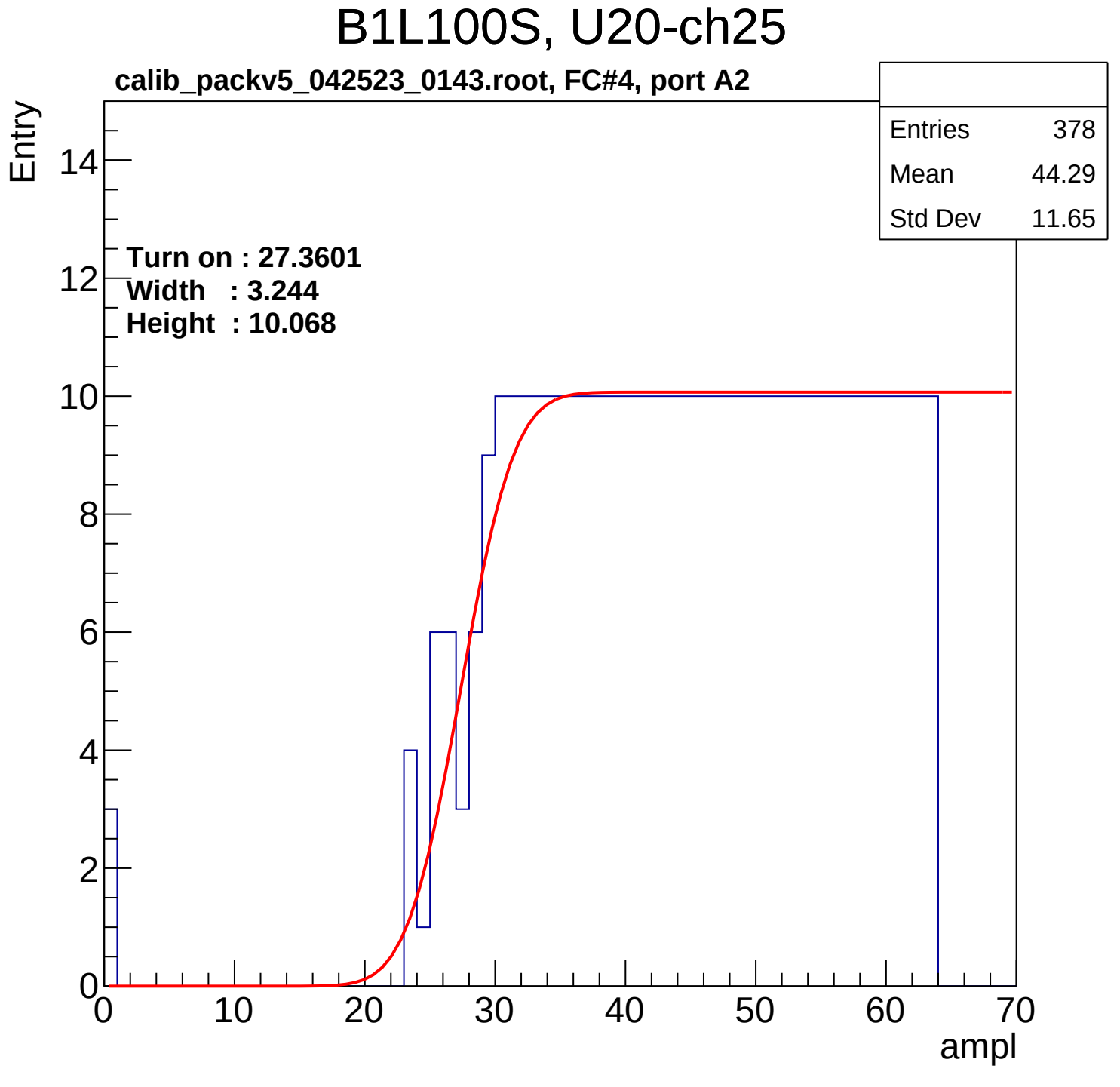
B1L100S, U20-ch25
calib_packv5_042523_0143.root, FC#4, port A2
Entries 378
Mean 44.29
Std Dev 11.65
Turn on : 27.3601
Width : 3.244
Height : 10.068
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ampl
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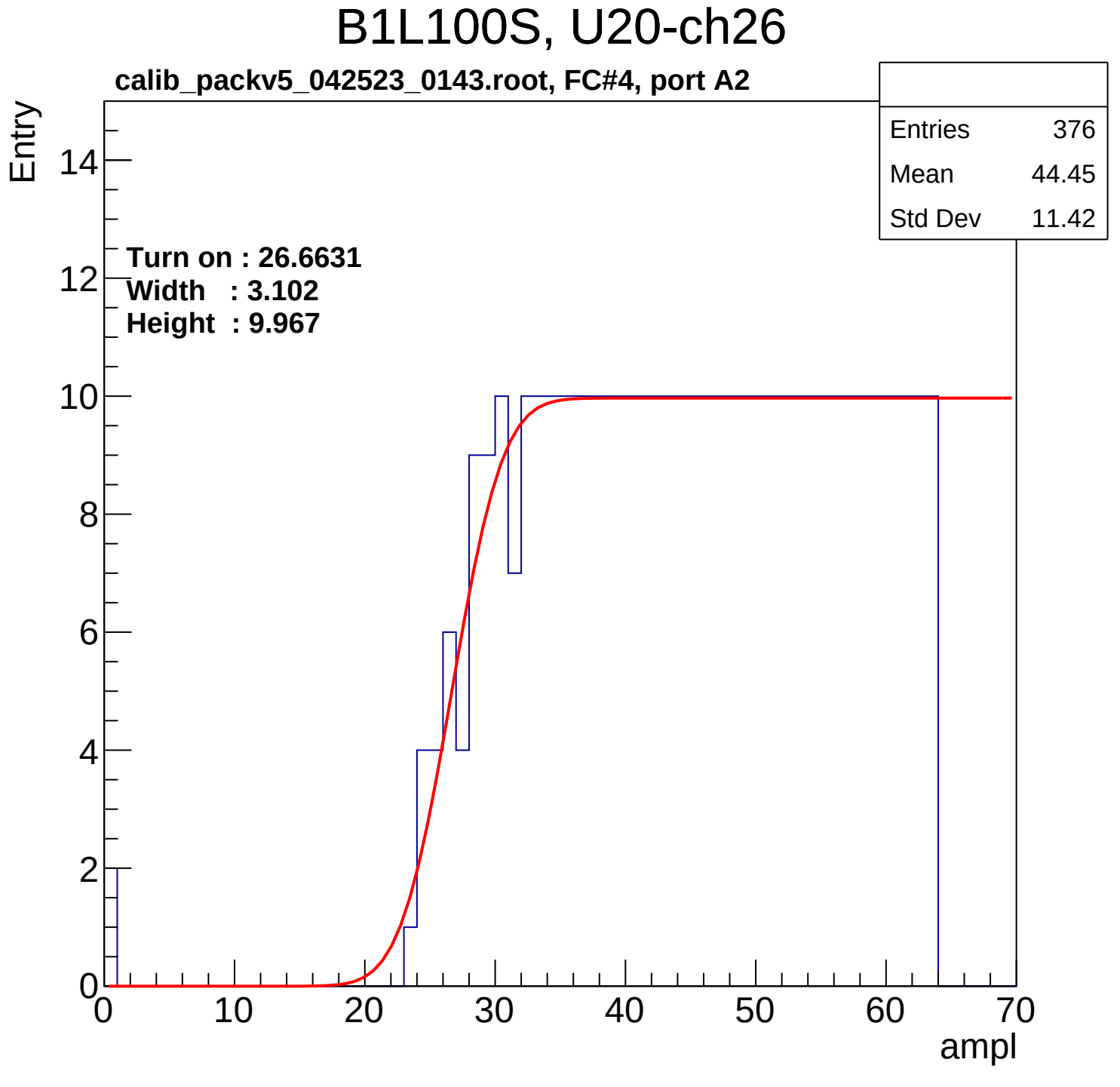
B1L100S, U20-ch26
calib_packv5_042523_0143.root, FC#4, port A2
Entries 376
Mean 44.45
Std Dev 11.42
Turn on : 26.6631
Width : 3.102
Height : 9.967
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ampl
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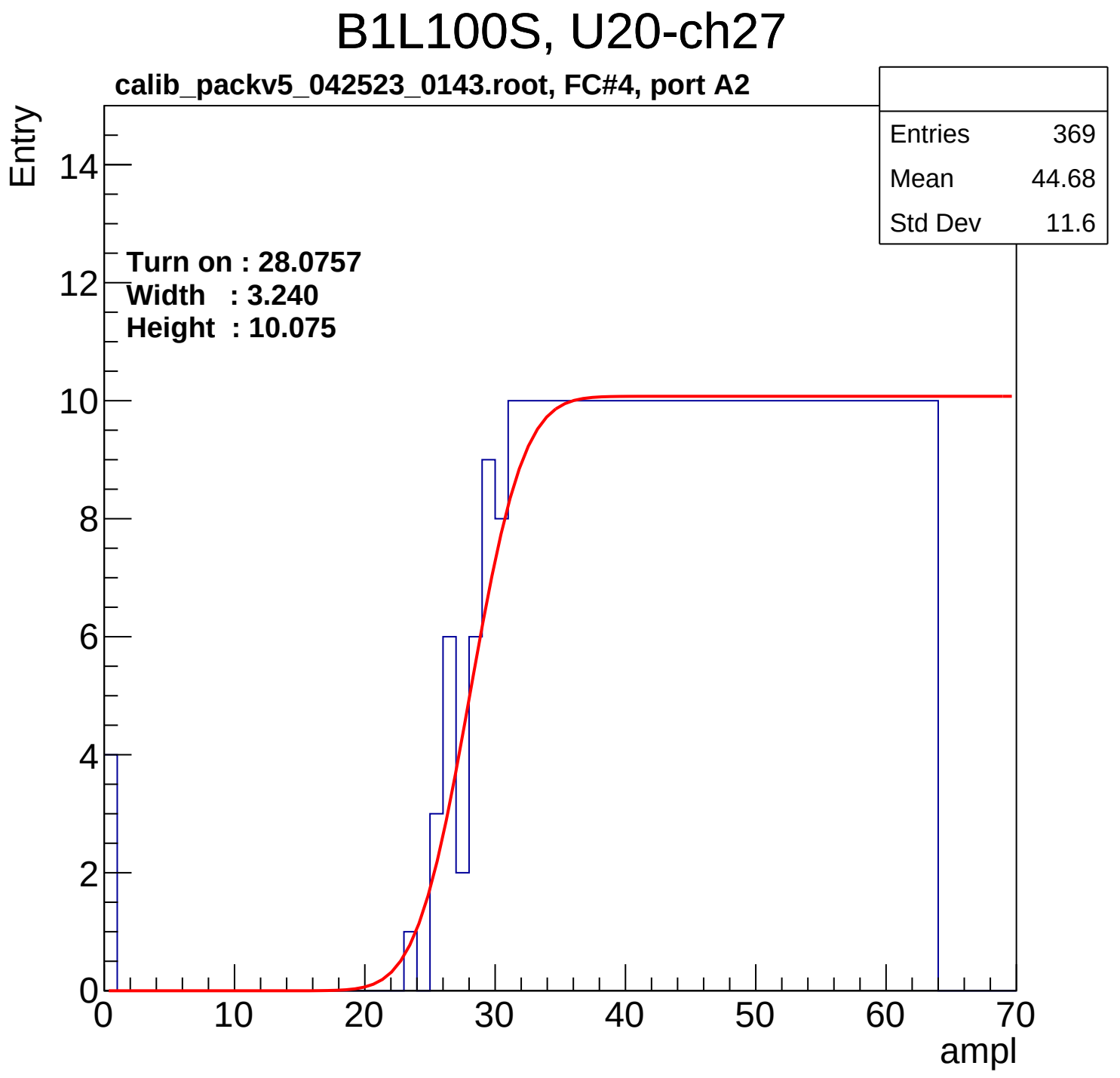
B1L100S, U20-ch27
calib_packv5_042523_0143.root, FC#4, port A2
Entries 369
Mean 44.68
Std Dev 11.6
Turn on : 28.0757
Width : 3.240
Height : 10.075
Entry
ampl
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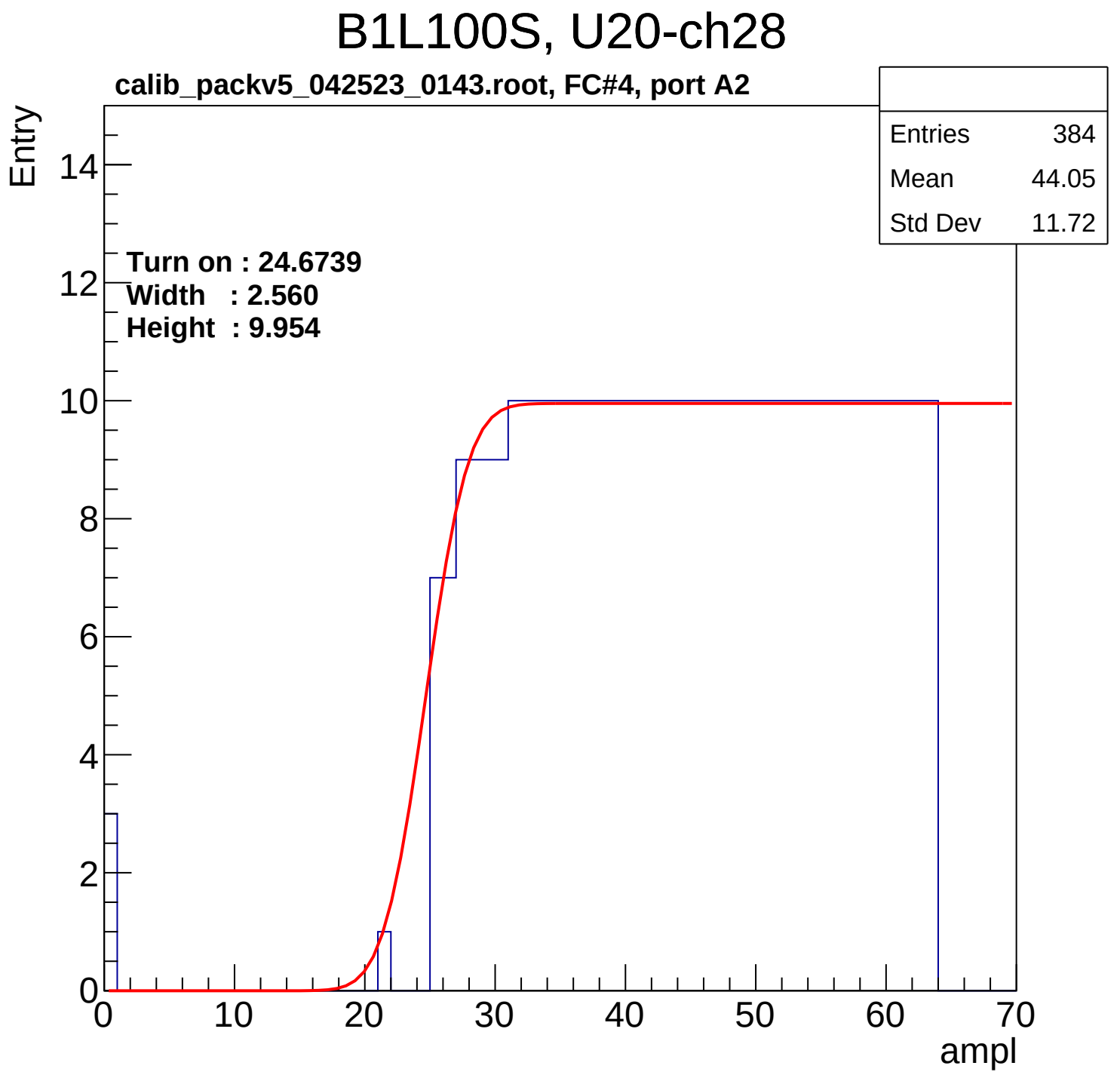
B1L100S, U20-ch28
calib_packv5_042523_0143.root, FC#4, port A2
Entries 384
Mean 44.05
Std Dev 11.72
Turn on : 24.6739
Width : 2.560
Height : 9.954
Entry
ampl
0
2
4
6
8
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12
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20
30
40
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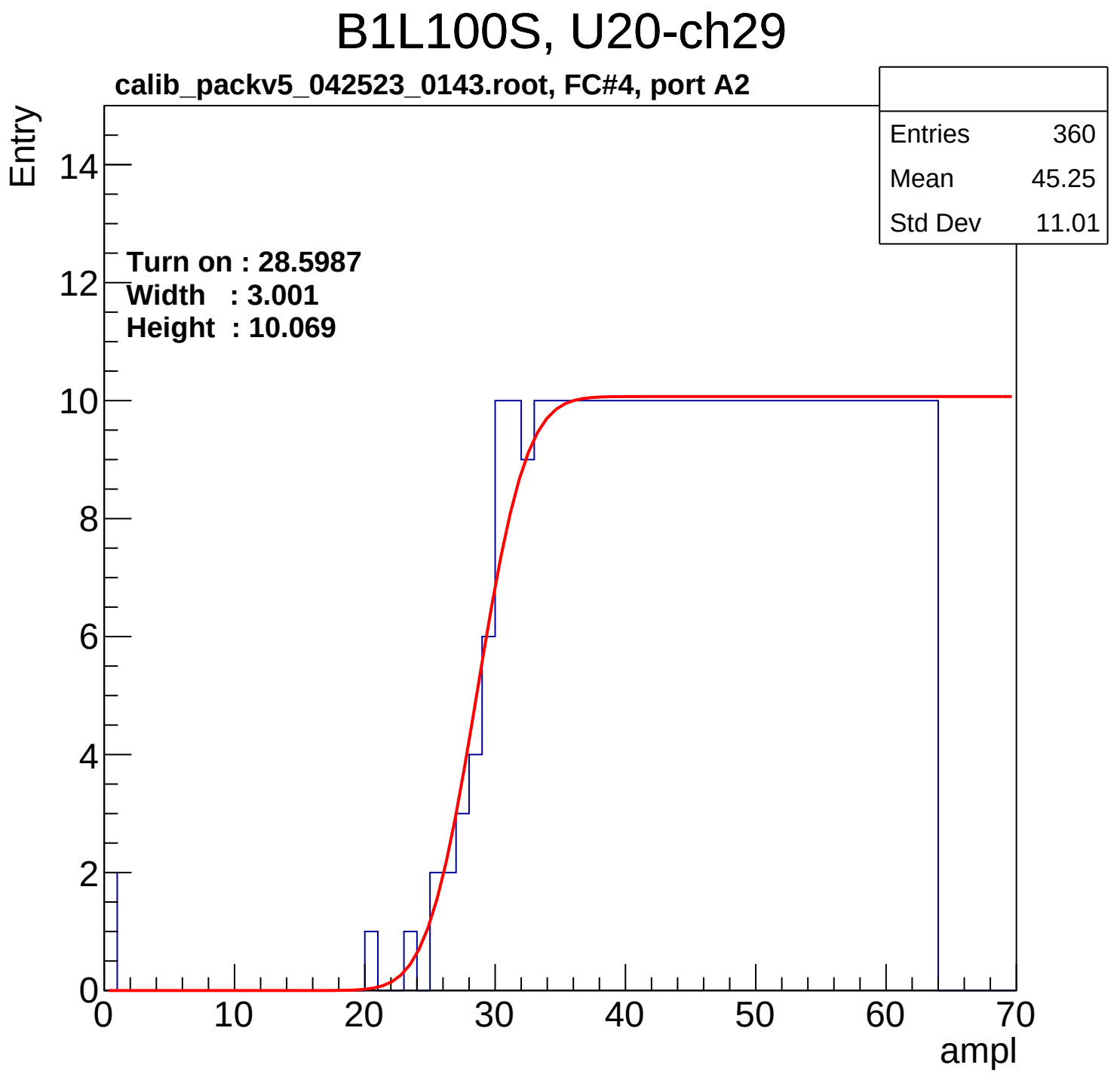
B1L100S, U20-ch29
calib_packv5_042523_0143.root, FC#4, port A2
Entries 360
Mean 45.25
Std Dev 11.01
Turn on : 28.5987
Width : 3.001
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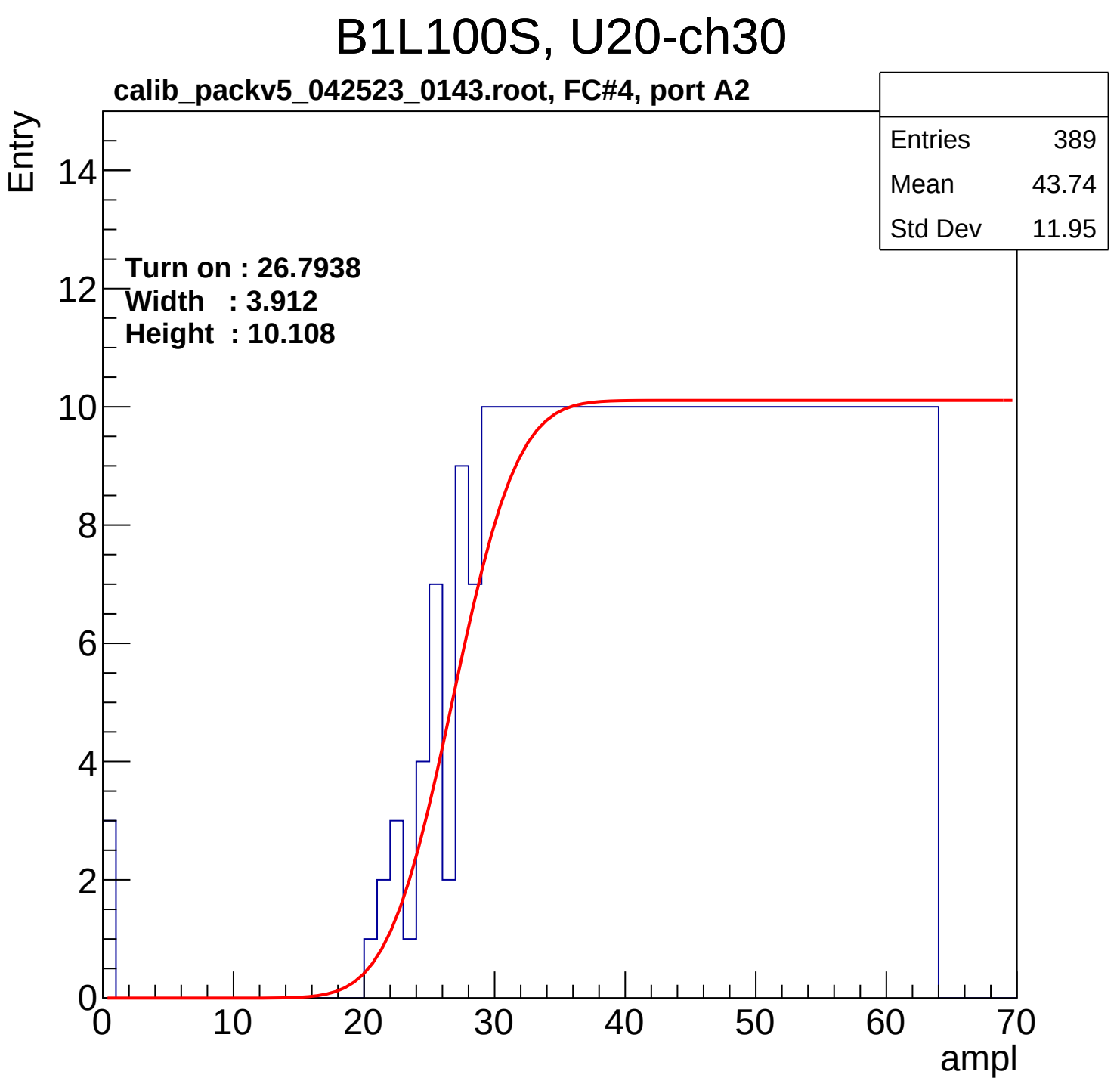
B1L100S, U20-ch30
calib_packv5_042523_0143.root, FC#4, port A2
Entries 389
Mean 43.74
Std Dev 11.95
Turn on : 26.7938
Width : 3.912
Height : 10.108
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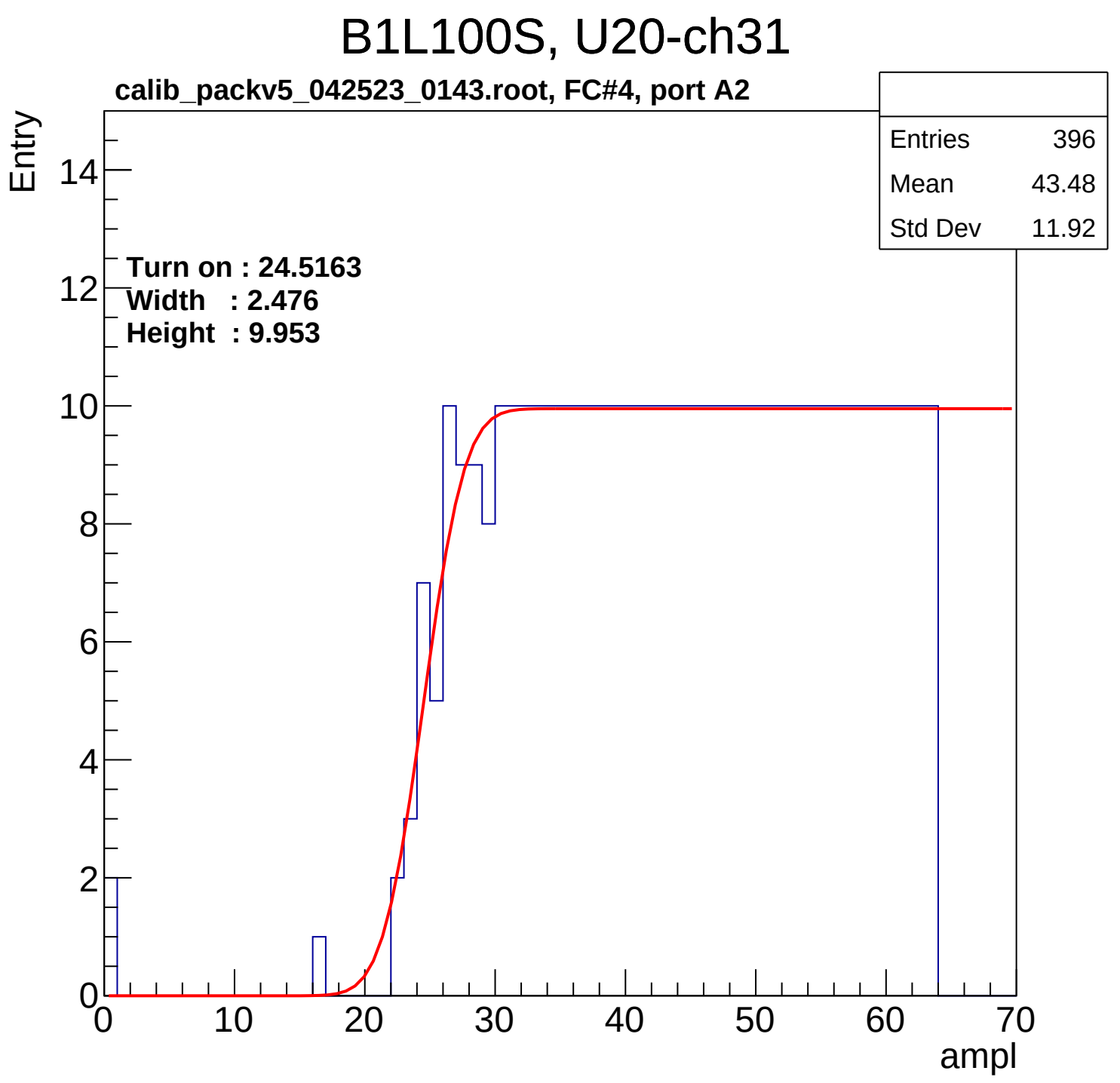
B1L100S, U20-ch31
calib_packv5_042523_0143.root, FC#4, port A2
Entries 396
Mean 43.48
Std Dev 11.92
Turn on : 24.5163
Width : 2.476
Height : 9.953
Entry
ampl
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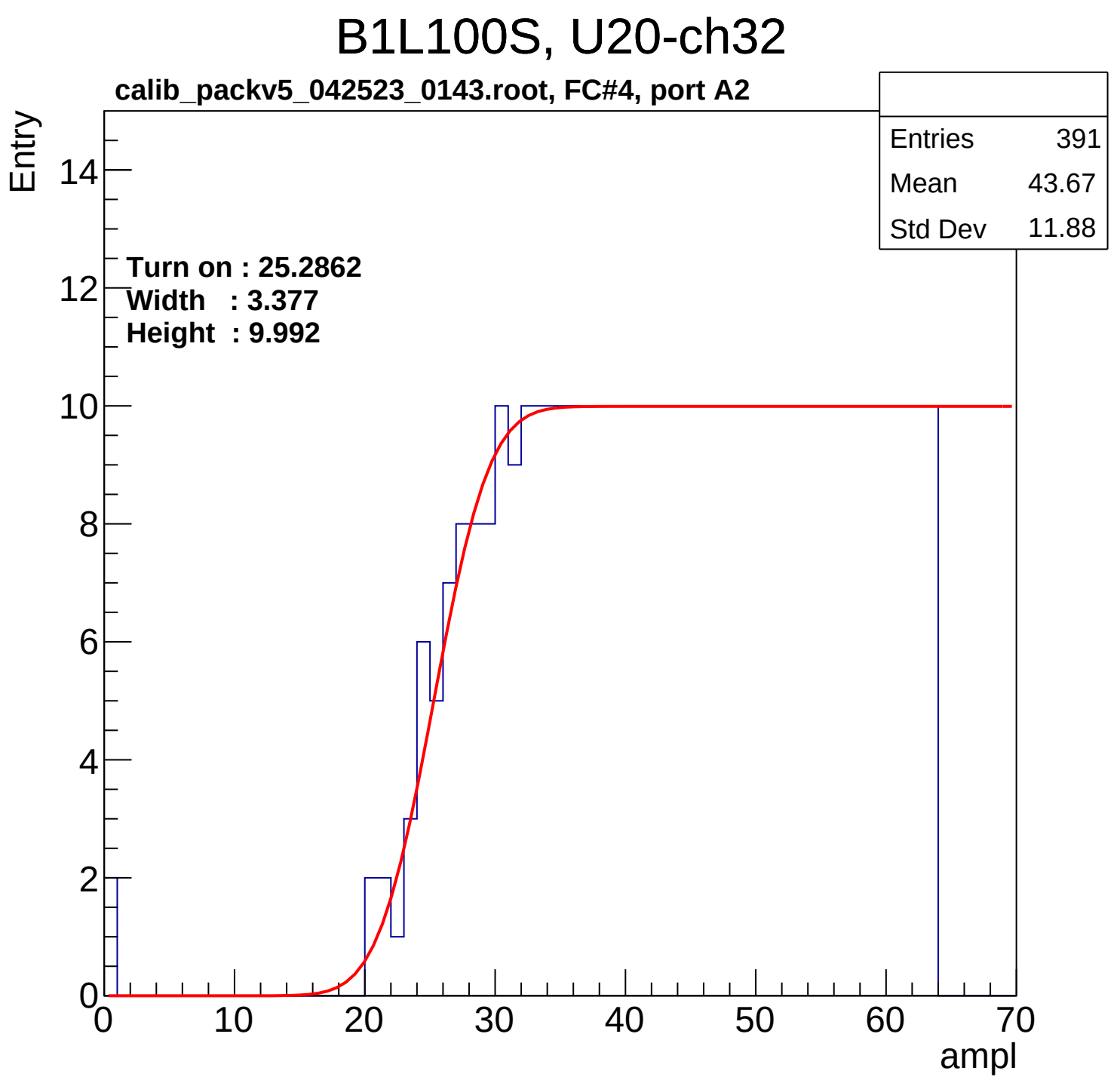
B1L100S, U20-ch32
calib_packv5_042523_0143.root, FC#4, port A2
Entries 391
Mean 43.67
Std Dev 11.88
Turn on : 25.2862
Width : 3.377
Height : 9.992
Entry
ampl
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6
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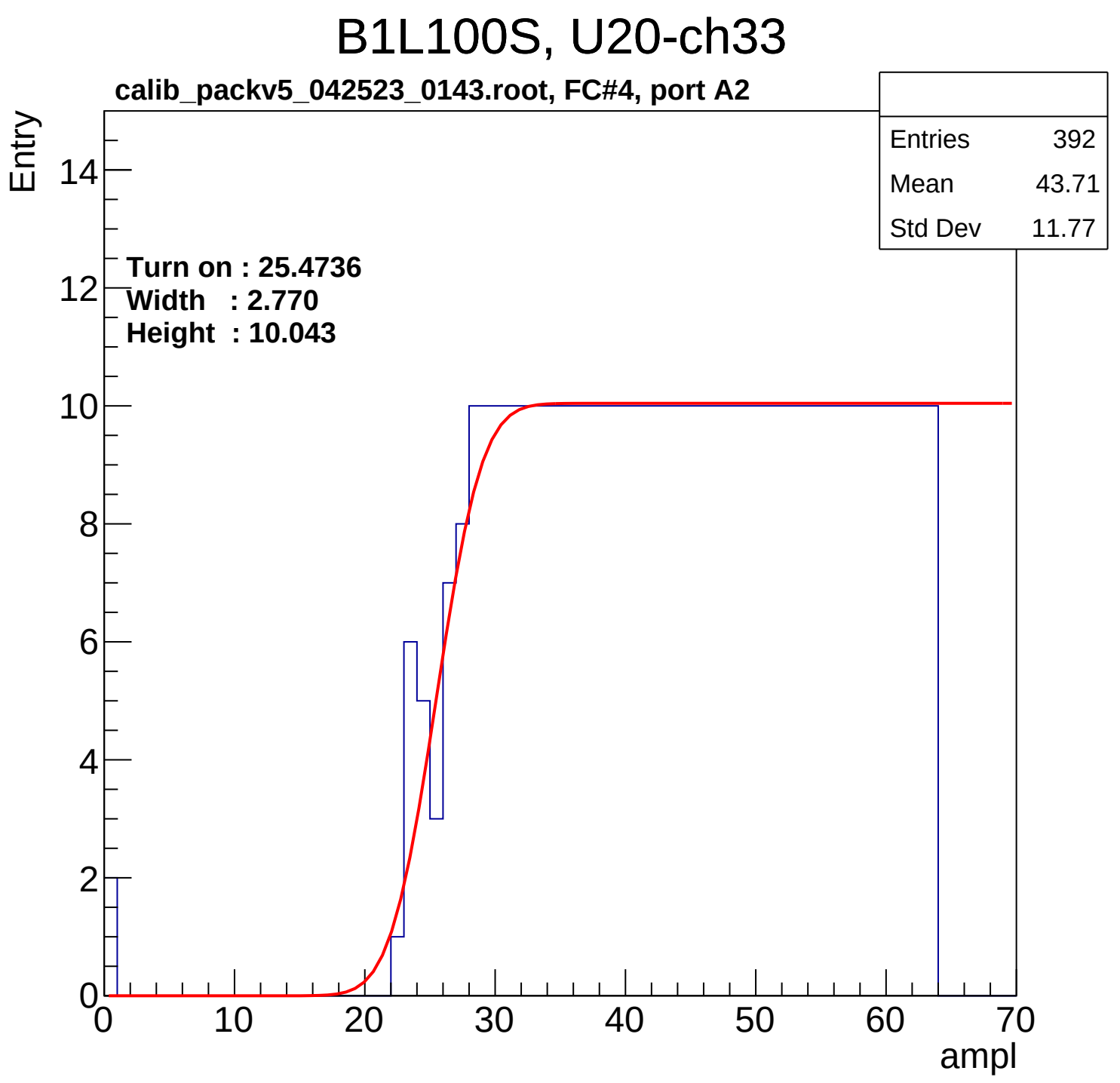
B1L100S, U20-ch33
calib_packv5_042523_0143.root, FC#4, port A2
Entries 392
Mean 43.71
Std Dev 11.77
Turn on : 25.4736
Width : 2.770
Height : 10.043
Entry
ampl
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8
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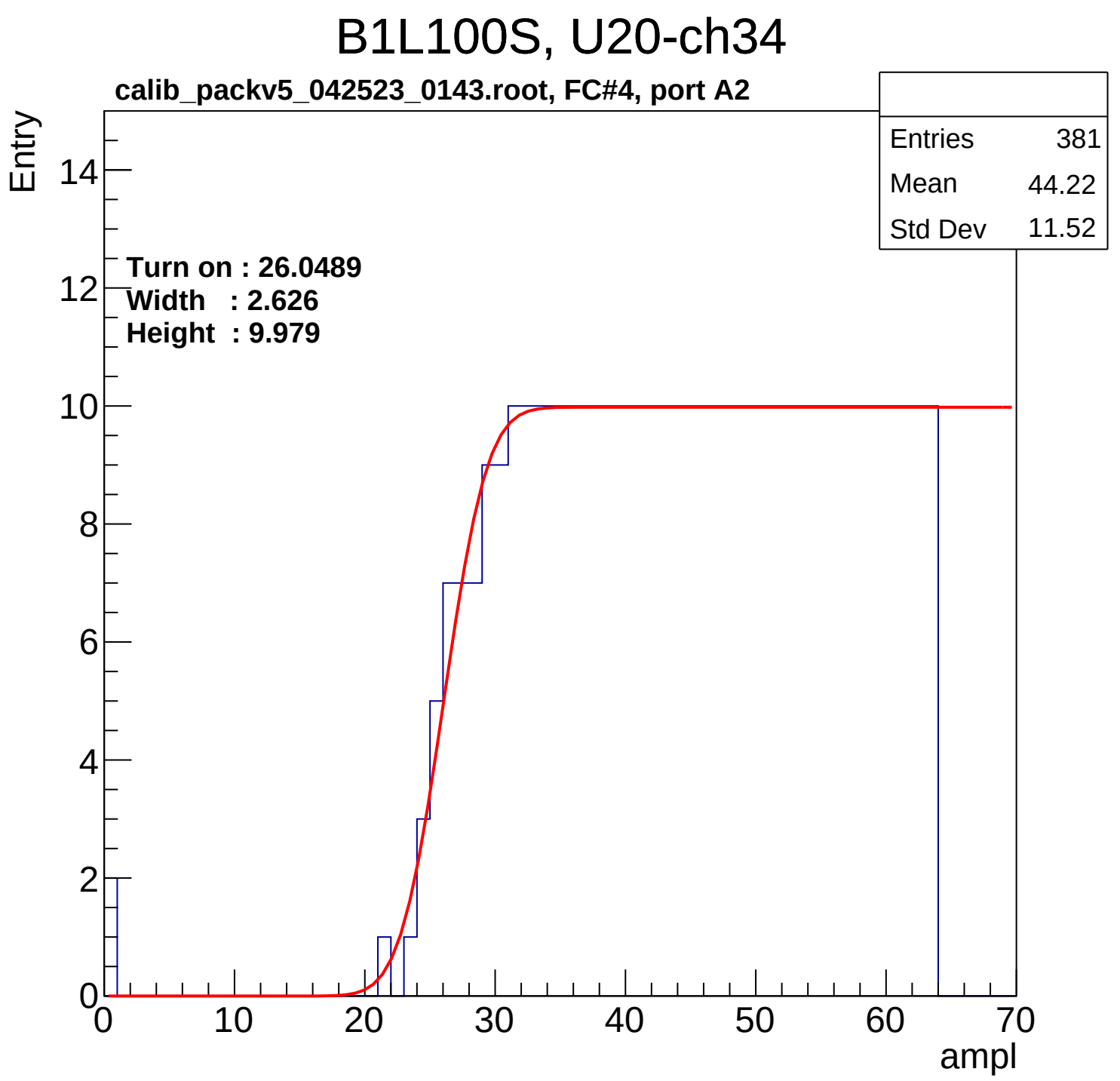
B1L100S, U20-ch34
calib_packv5_042523_0143.root, FC#4, port A2
Entries 381
Mean 44.22
Std Dev 11.52
Turn on : 26.0489
Width : 2.626
Height : 9.979
Entry
ampl
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6
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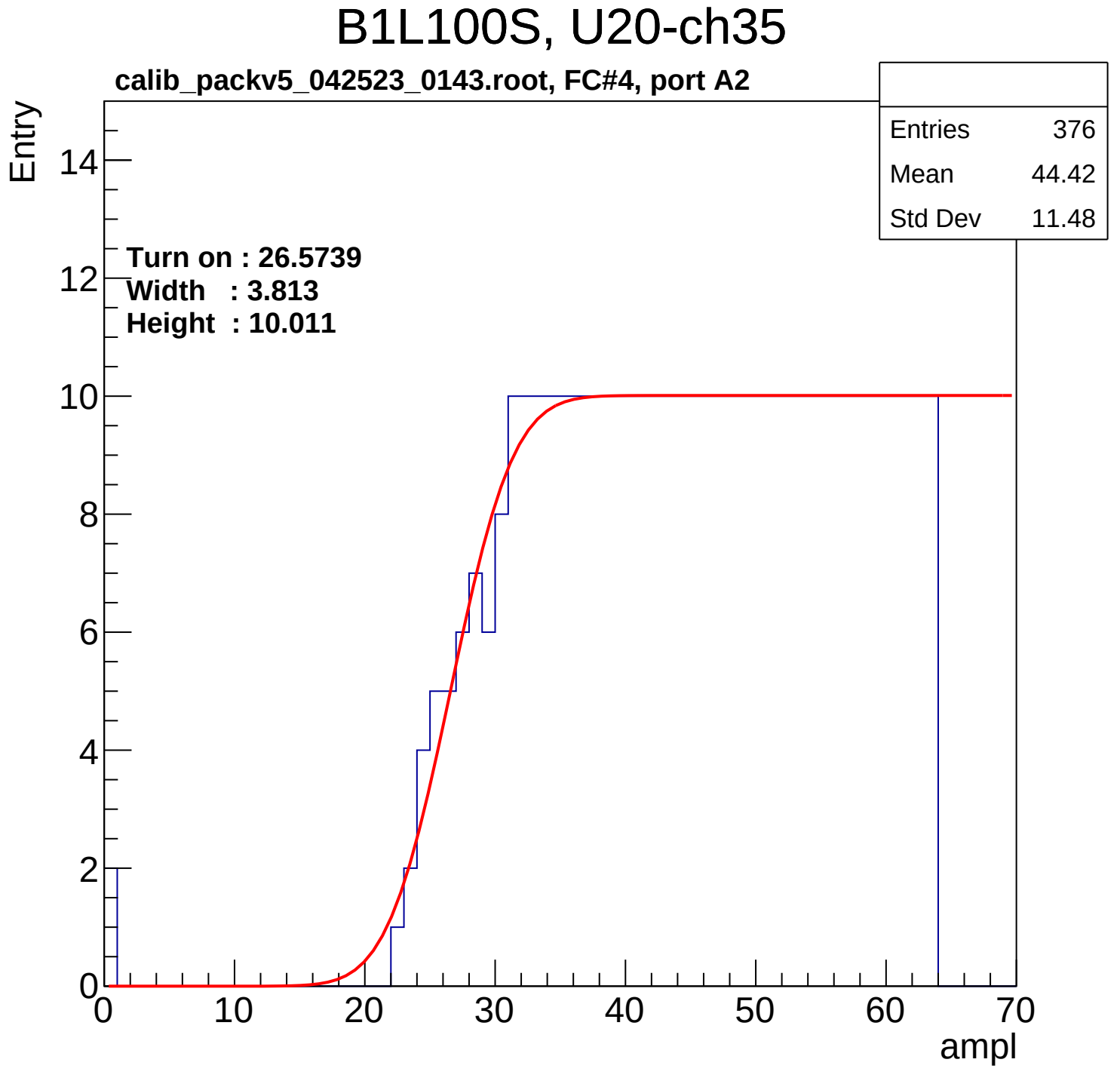
B1L100S, U20-ch35
calib_packv5_042523_0143.root, FC#4, port A2
Entries 376
Mean 44.42
Std Dev 11.48
Turn on : 26.5739
Width : 3.813
Height : 10.011
Entry
ampl
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2
4
6
8
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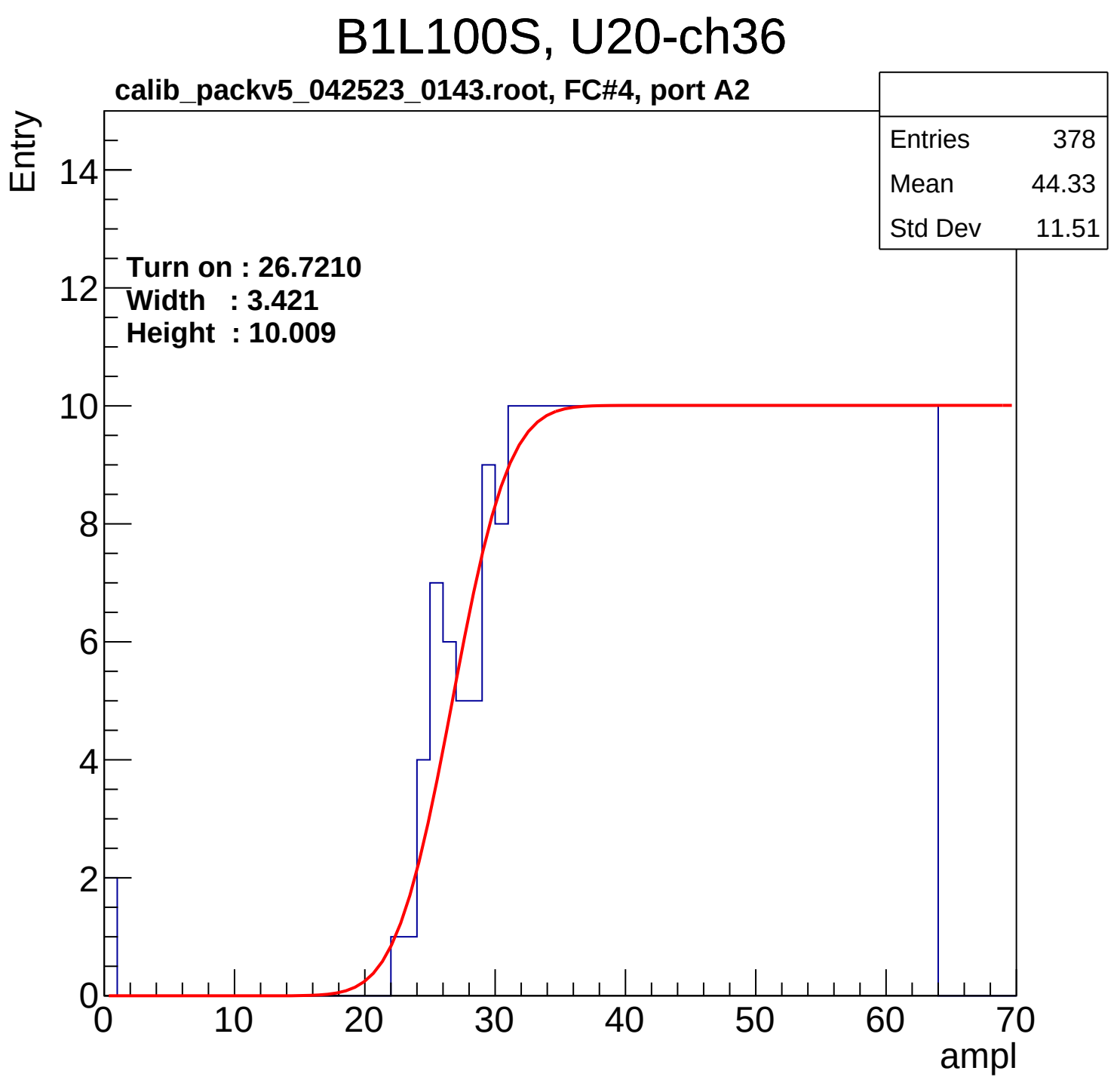
B1L100S, U20-ch36
calib_packv5_042523_0143.root, FC#4, port A2
Entries 378
Mean 44.33
Std Dev 11.51
Turn on : 26.7210
Width : 3.421
Height : 10.009
Entry
ampl
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2
4
6
8
10
12
14
0
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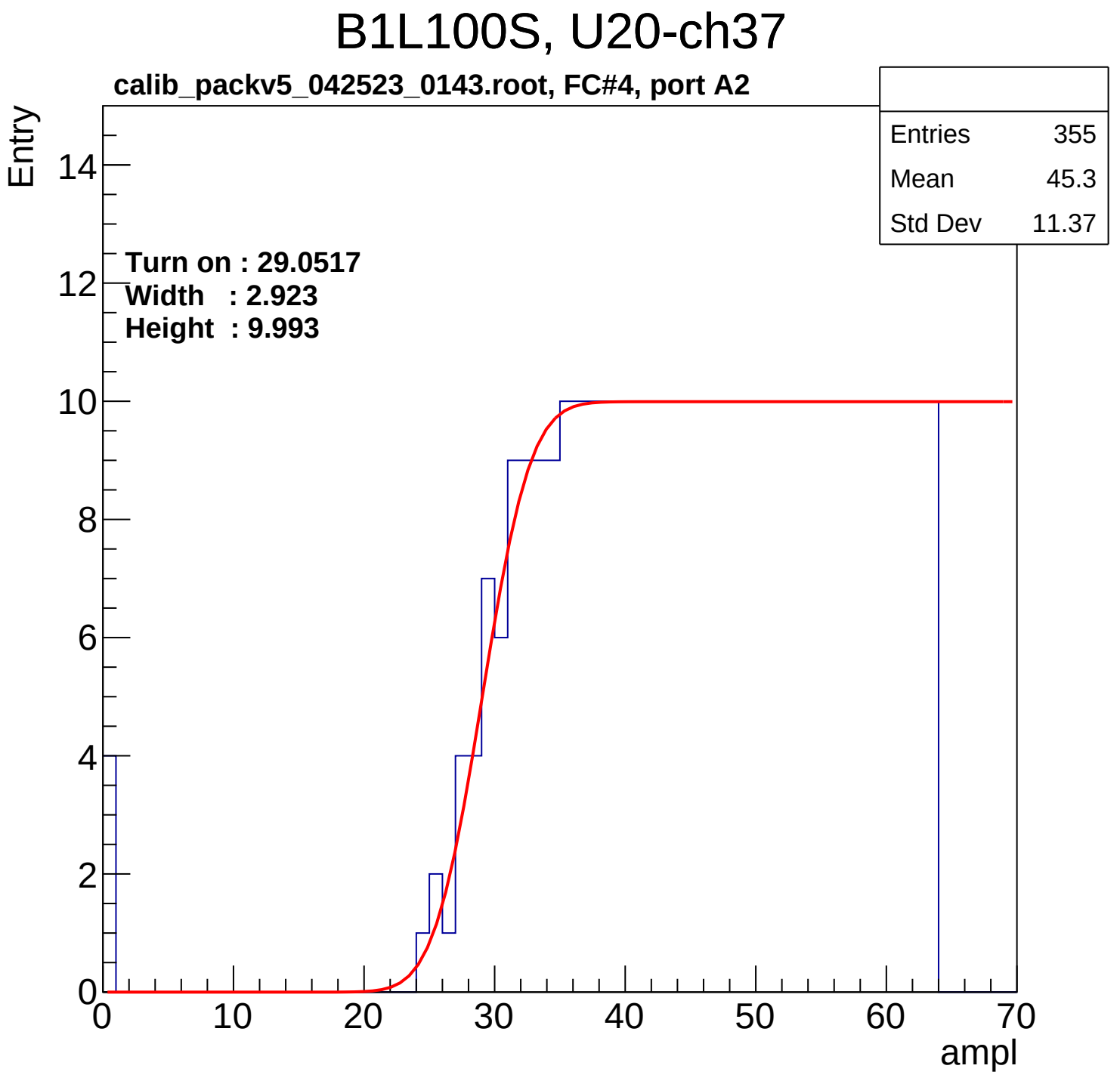
B1L100S, U20-ch37
calib_packv5_042523_0143.root, FC#4, port A2
Entries 355
Mean 45.3
Std Dev 11.37
Turn on : 29.0517
Width : 2.923
Height : 9.993
Entry
ampl
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2
4
6
8
10
12
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0
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60
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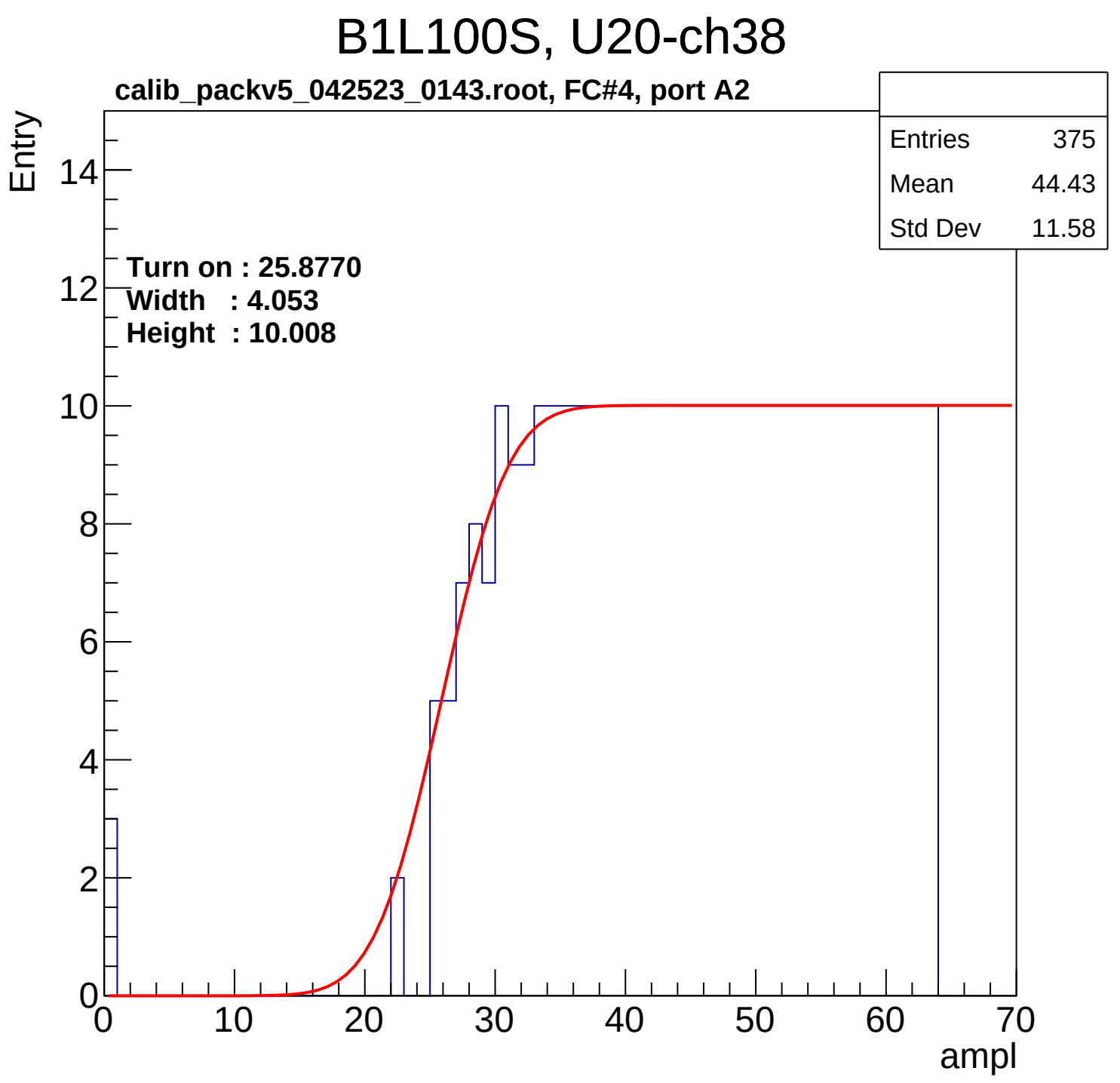
B1L100S, U20-ch38
calib_packv5_042523_0143.root, FC#4, port A2
Entries 375
Mean 44.43
Std Dev 11.58
Turn on : 25.8770
Width : 4.053
Height : 10.008
Entry
ampl
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2
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6
8
10
12
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0
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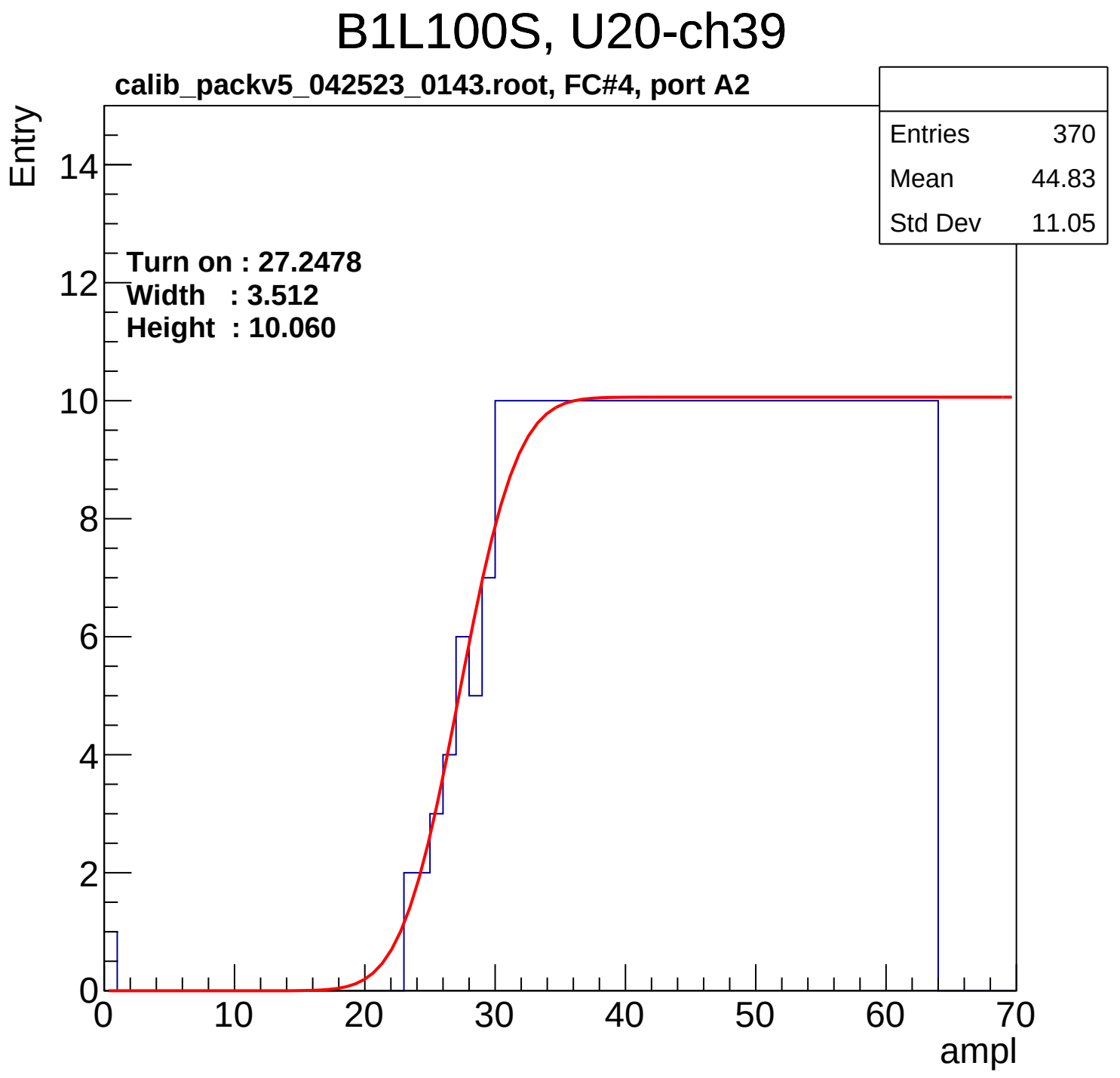
B1L100S, U20-ch39
calib_packv5_042523_0143.root, FC#4, port A2
Entries 370
Mean 44.83
Std Dev 11.05
Turn on : 27.2478
Width : 3.512
Height : 10.060
Entry
ampl
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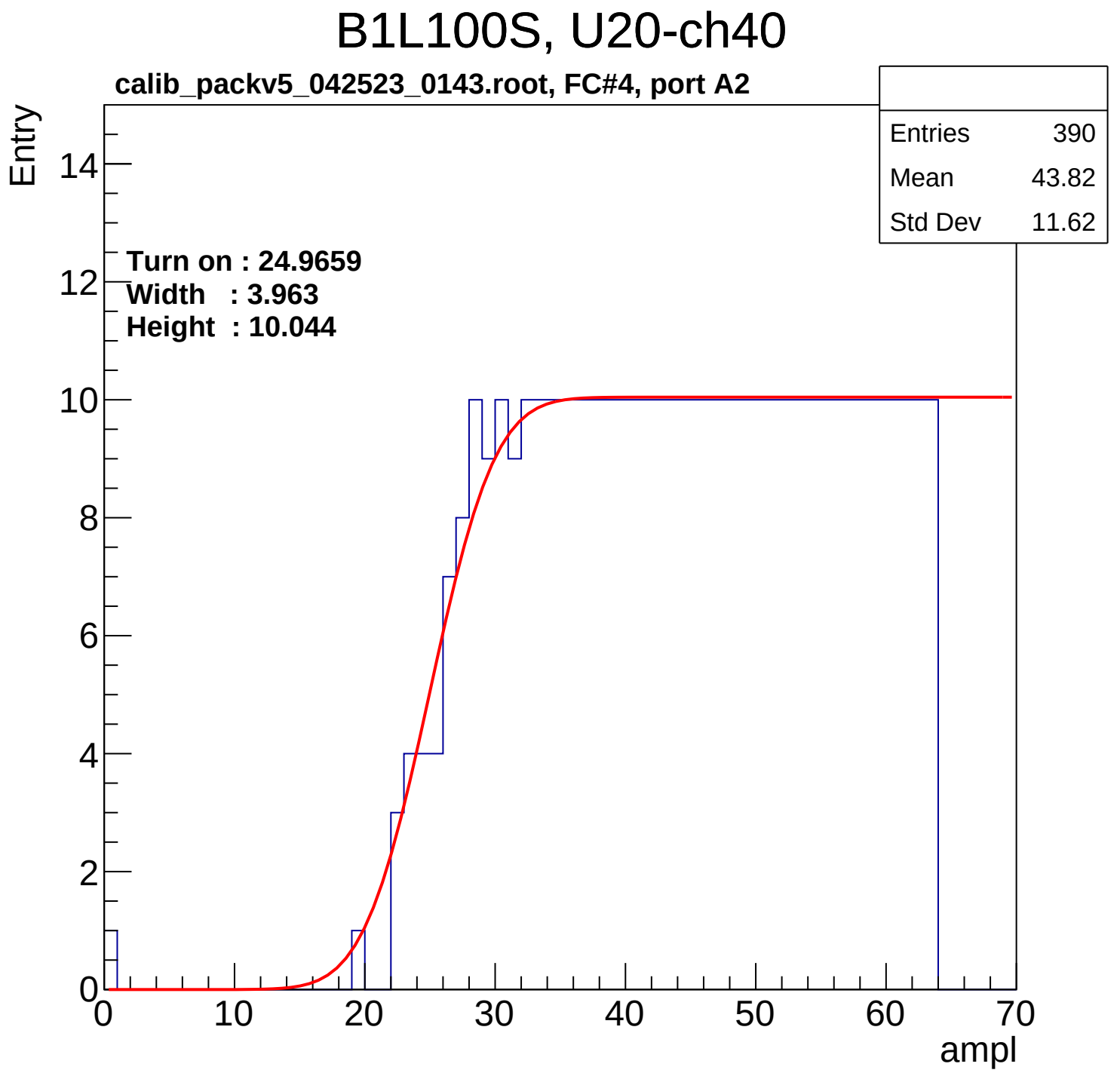
B1L100S, U20-ch40
calib_packv5_042523_0143.root, FC#4, port A2
Entries 390
Mean 43.82
Std Dev 11.62
Turn on : 24.9659
Width : 3.963
Height : 10.044
Entry
ampl
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8
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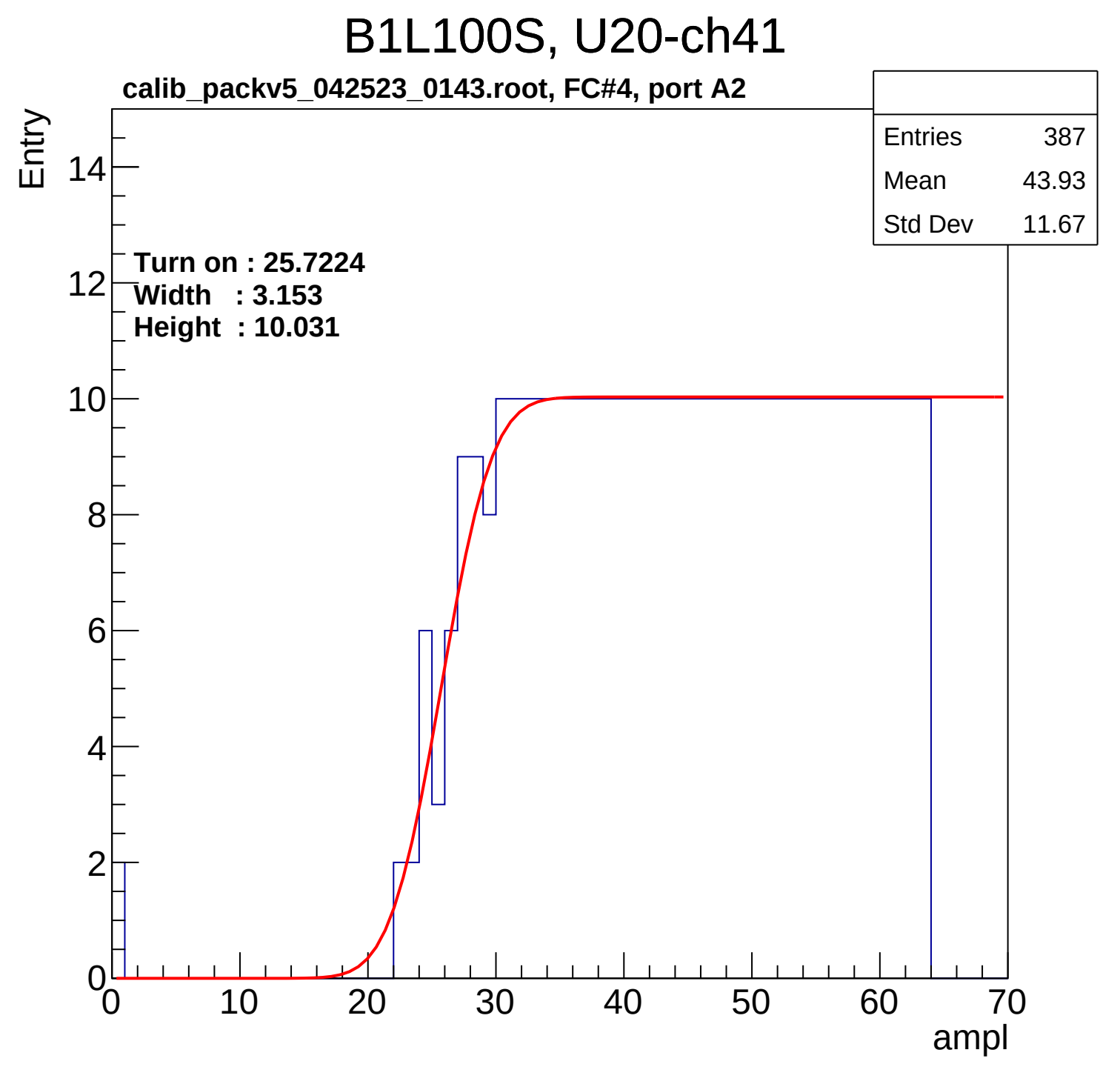
B1L100S, U20-ch41
calib_packv5_042523_0143.root, FC#4, port A2
Entries 387
Mean 43.93
Std Dev 11.67
Turn on : 25.7224
Width : 3.153
Height : 10.031
Entry
ampl
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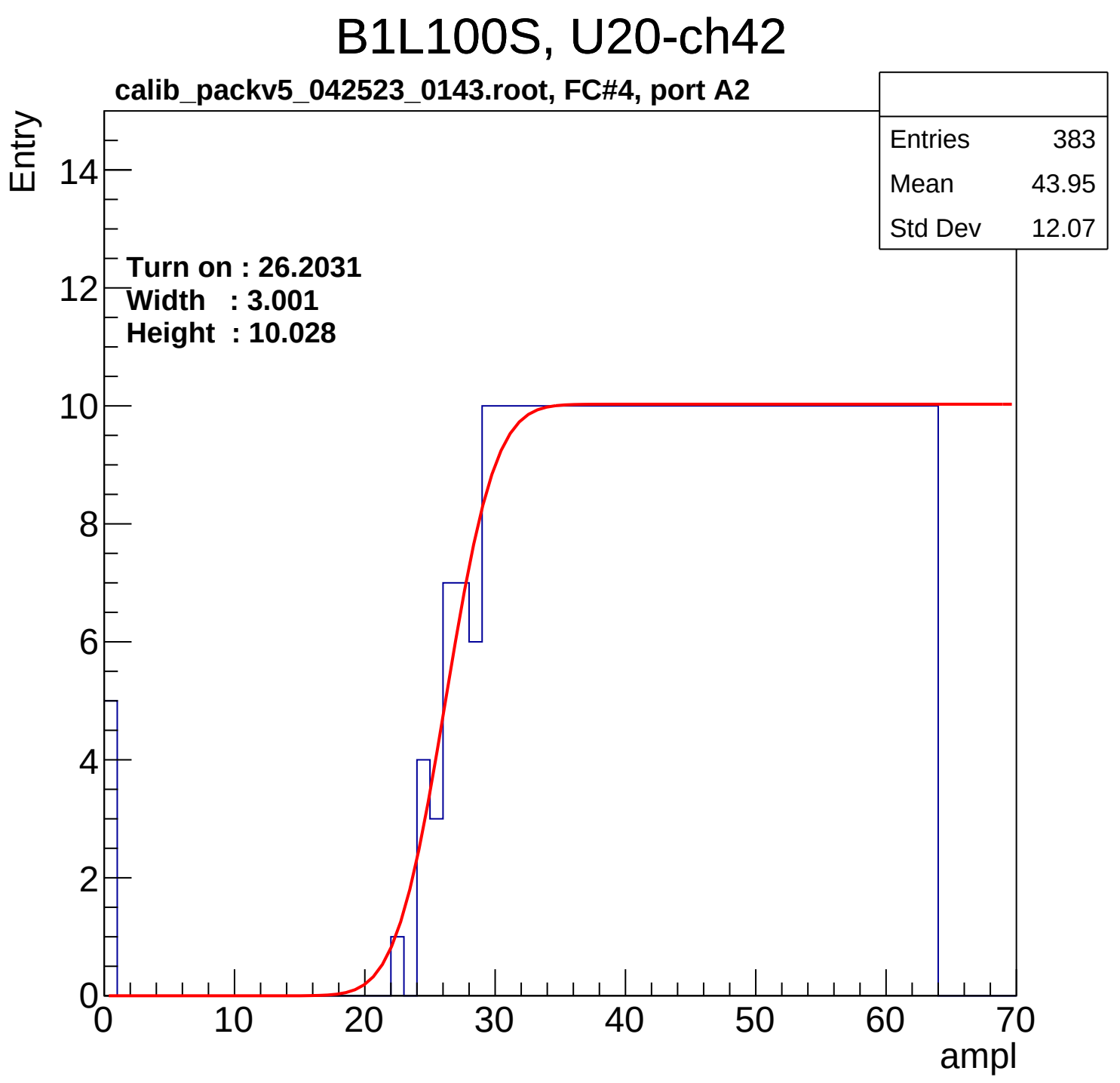
B1L100S, U20-ch42
calib_packv5_042523_0143.root, FC#4, port A2
Entries 383
Mean 43.95
Std Dev 12.07
Turn on : 26.2031
Width : 3.001
Height : 10.028
Entry
ampl
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2
4
6
8
10
12
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0
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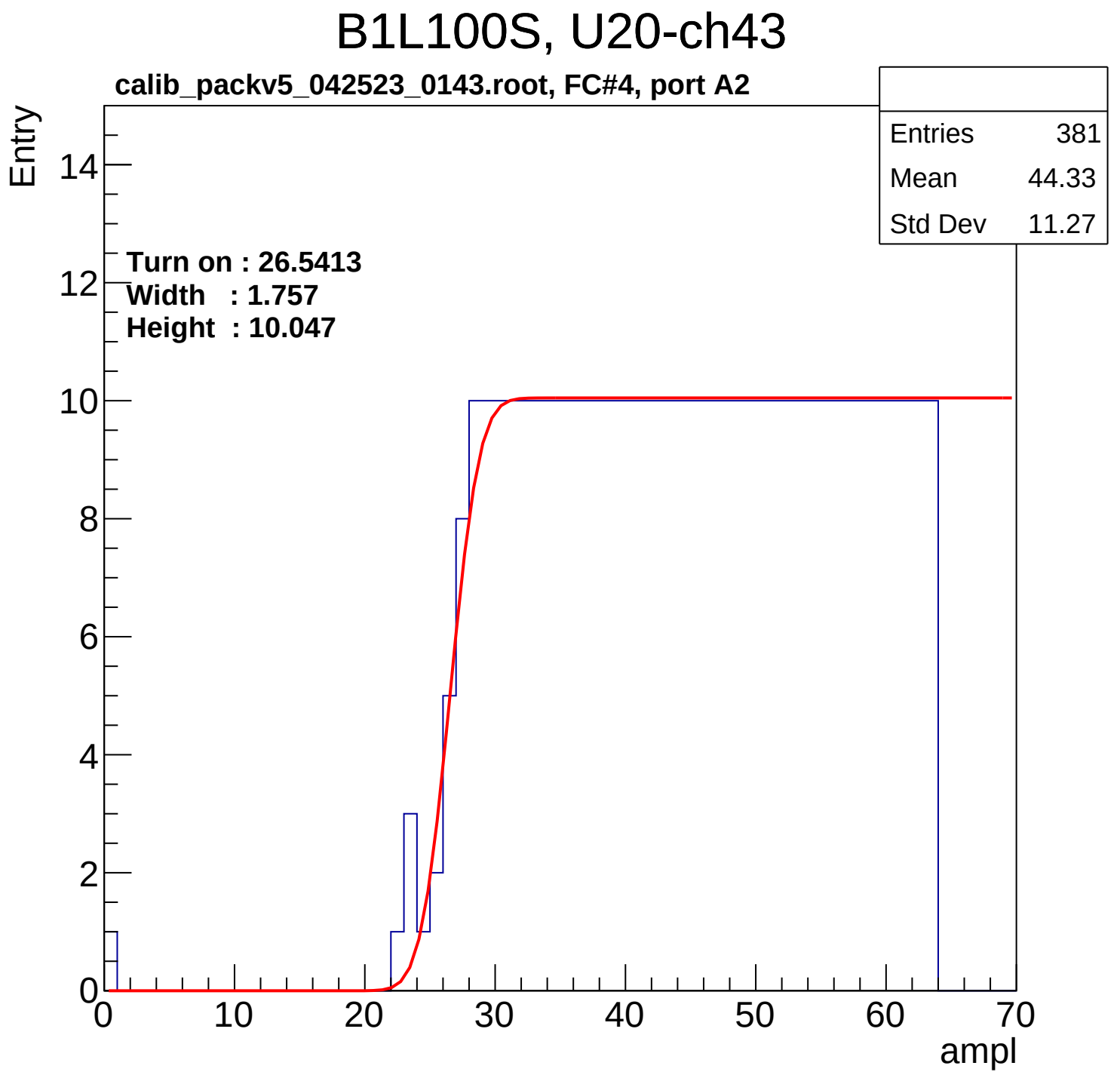
B1L100S, U20-ch43
calib_packv5_042523_0143.root, FC#4, port A2
Entries 381
Mean 44.33
Std Dev 11.27
Turn on : 26.5413
Width : 1.757
Height : 10.047
Entry
ampl
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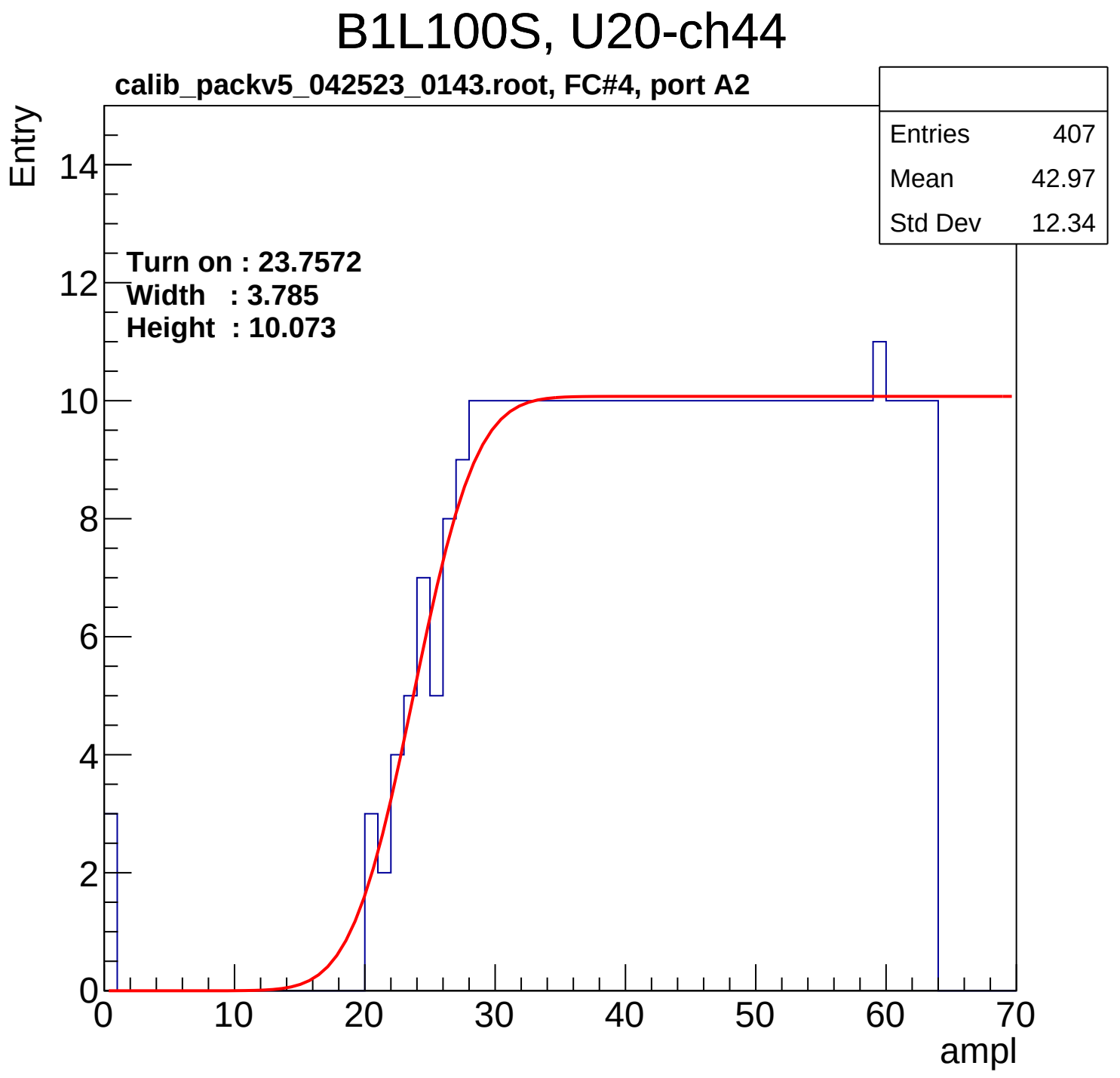
B1L100S, U20-ch44
calib_packv5_042523_0143.root, FC#4, port A2
Entries 407
Mean 42.97
Std Dev 12.34
Turn on : 23.7572
Width : 3.785
Height : 10.073
Entry
ampl
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8
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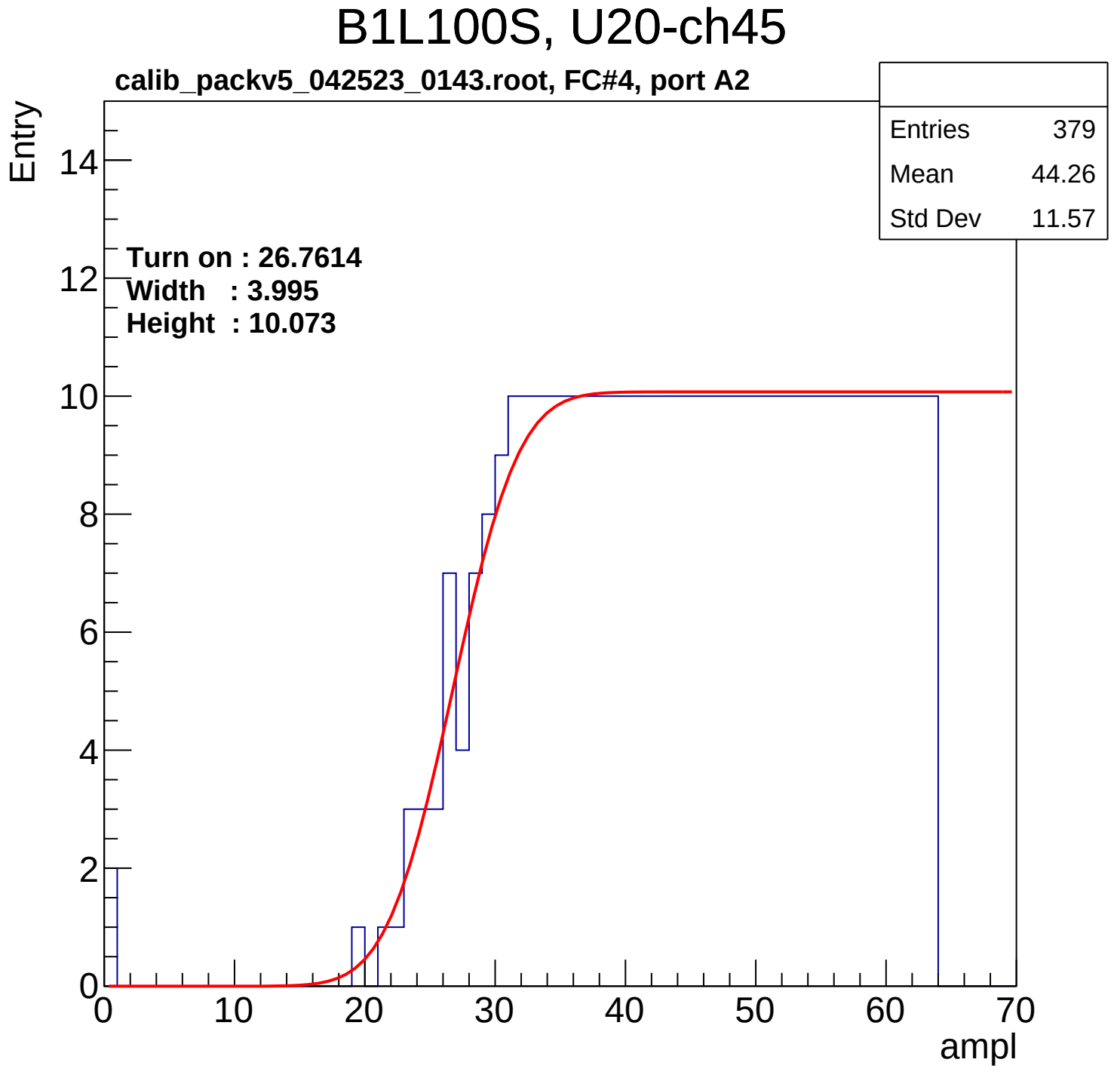
B1L100S, U20-ch45
calib_packv5_042523_0143.root, FC#4, port A2
Entries 379
Mean 44.26
Std Dev 11.57
Turn on : 26.7614
Width : 3.995
Height : 10.073
Entry
ampl
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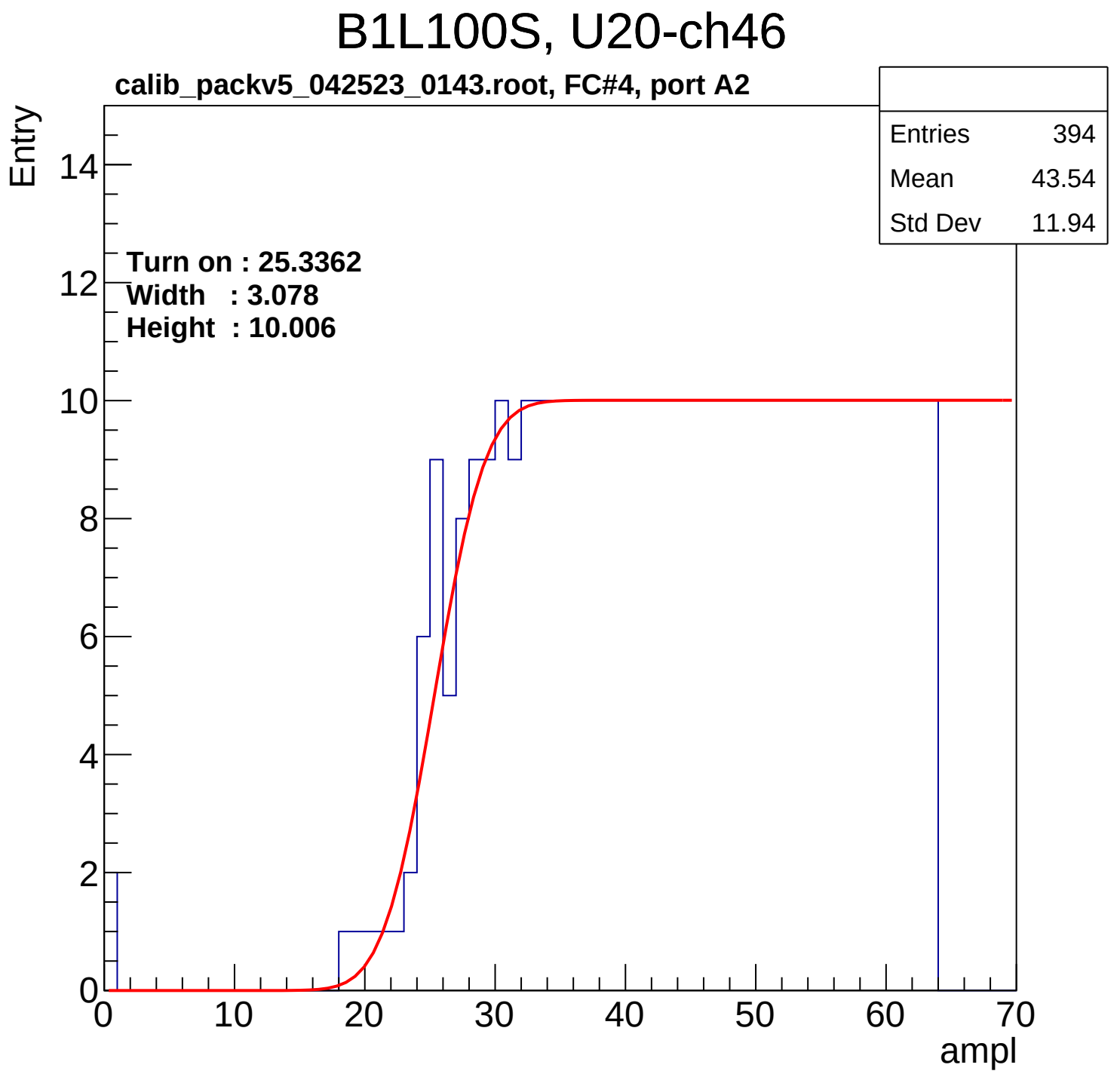
B1L100S, U20-ch46
calib_packv5_042523_0143.root, FC#4, port A2
Entries 394
Mean 43.54
Std Dev 11.94
Turn on : 25.3362
Width : 3.078
Height : 10.006
Entry
ampl
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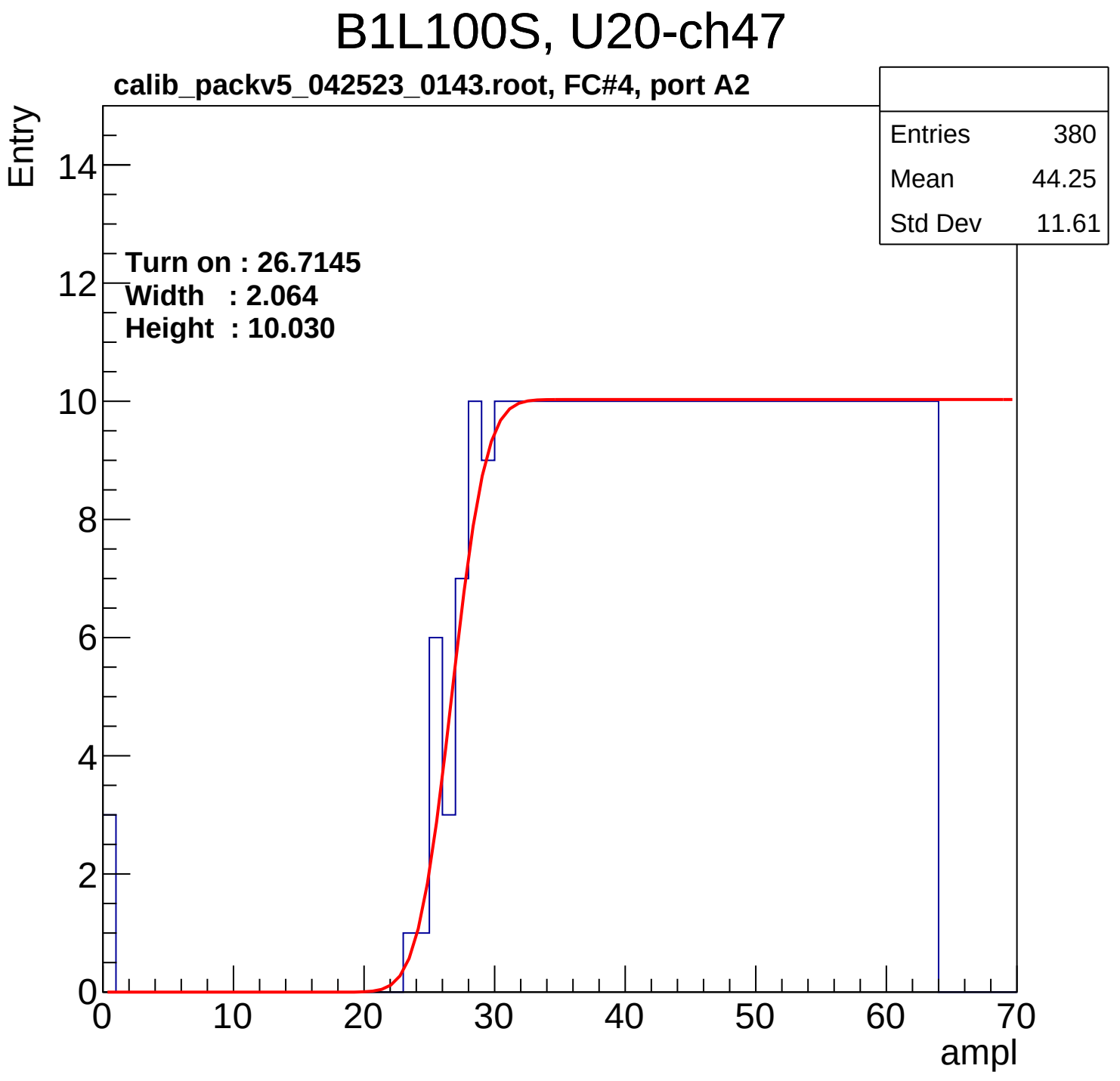
B1L100S, U20-ch47
calib_packv5_042523_0143.root, FC#4, port A2
Entries 380
Mean 44.25
Std Dev 11.61
Turn on : 26.7145
Width : 2.064
Height : 10.030
Entry
ampl
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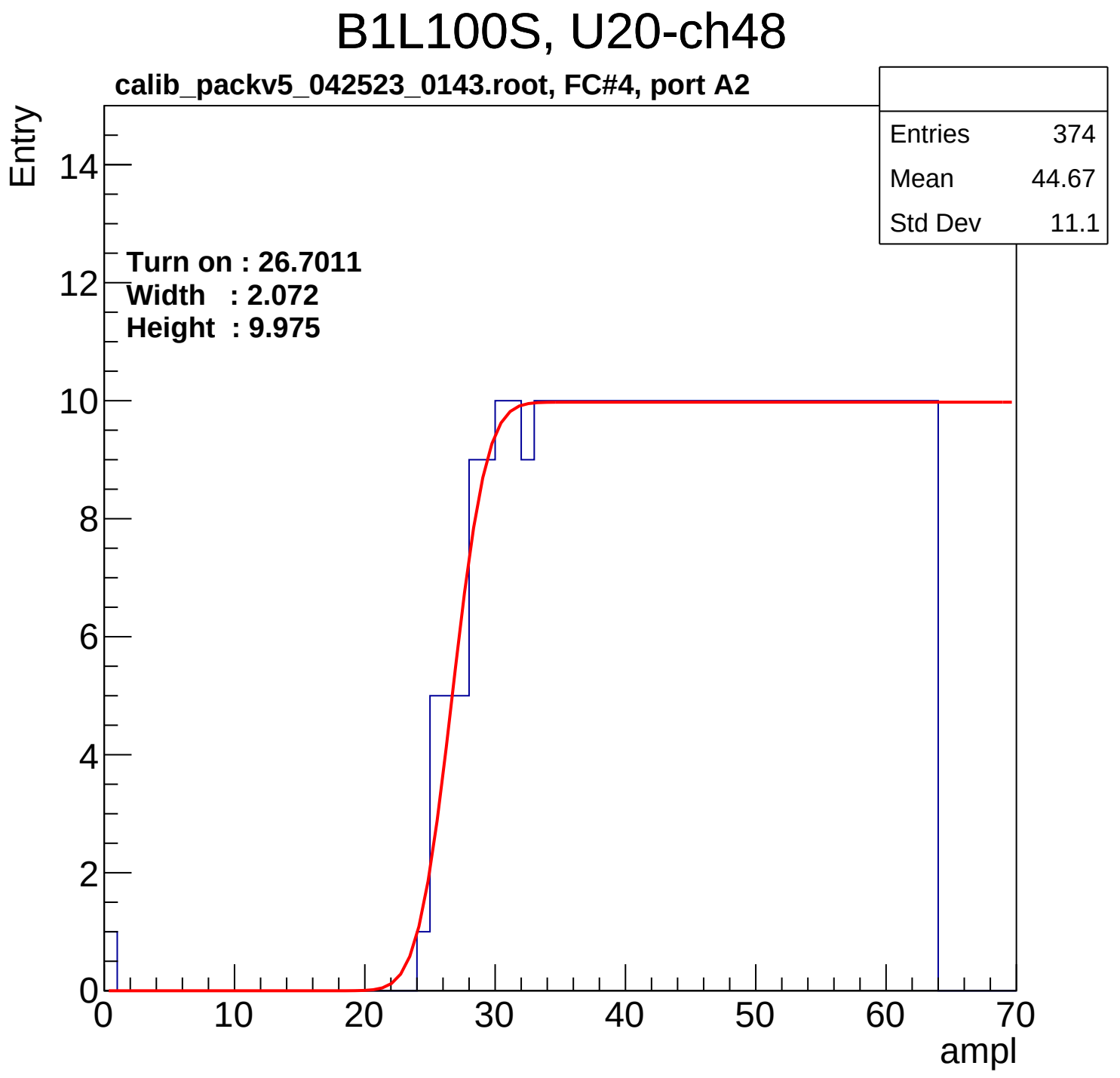
B1L100S, U20-ch48
calib_packv5_042523_0143.root, FC#4, port A2
Entries 374
Mean 44.67
Std Dev 11.1
Turn on : 26.7011
Width : 2.072
Height : 9.975
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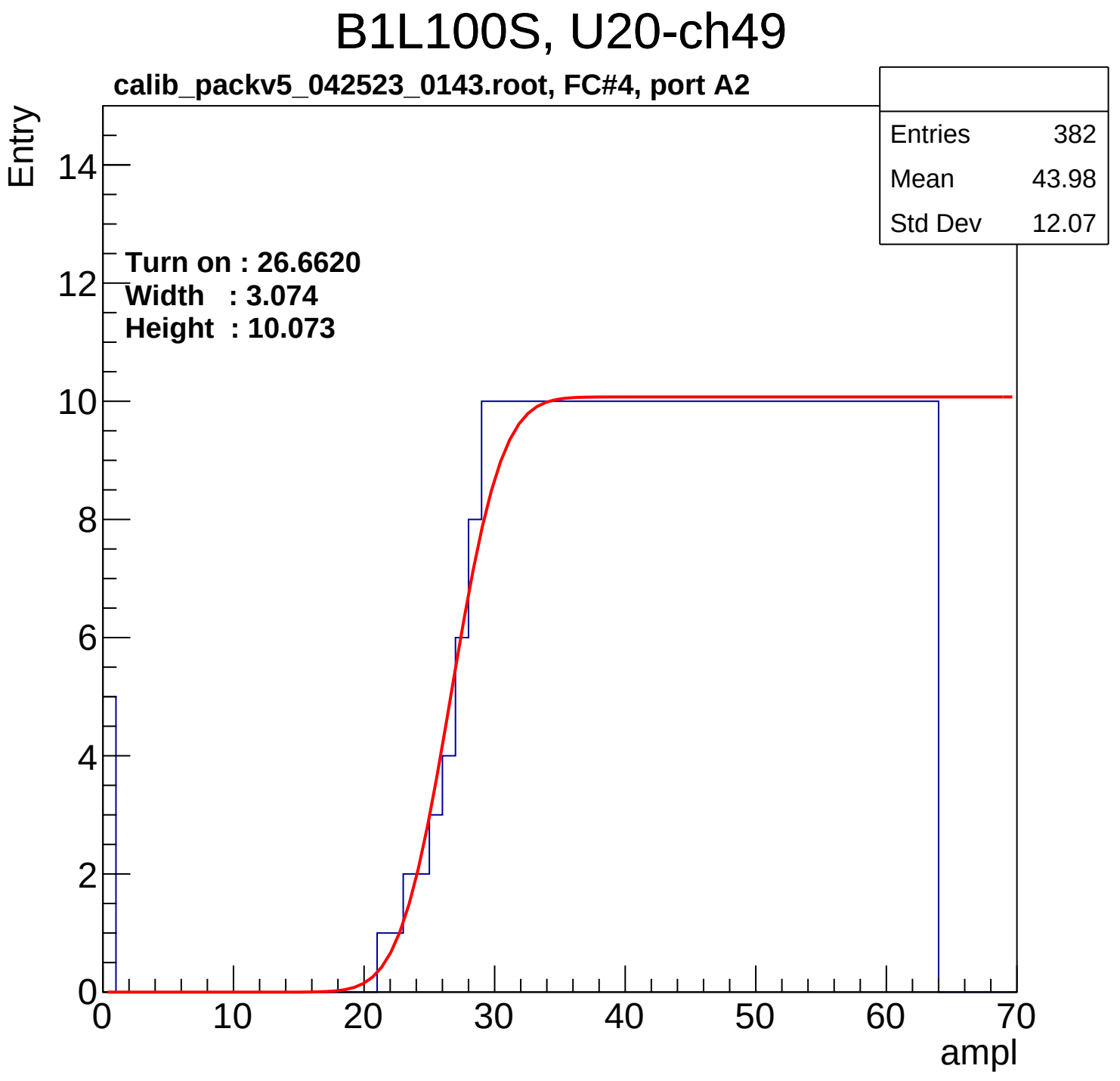
B1L100S, U20-ch49
calib_packv5_042523_0143.root, FC#4, port A2
Entries 382
Mean 43.98
Std Dev 12.07
Turn on : 26.6620
Width : 3.074
Height : 10.073
Entry
ampl
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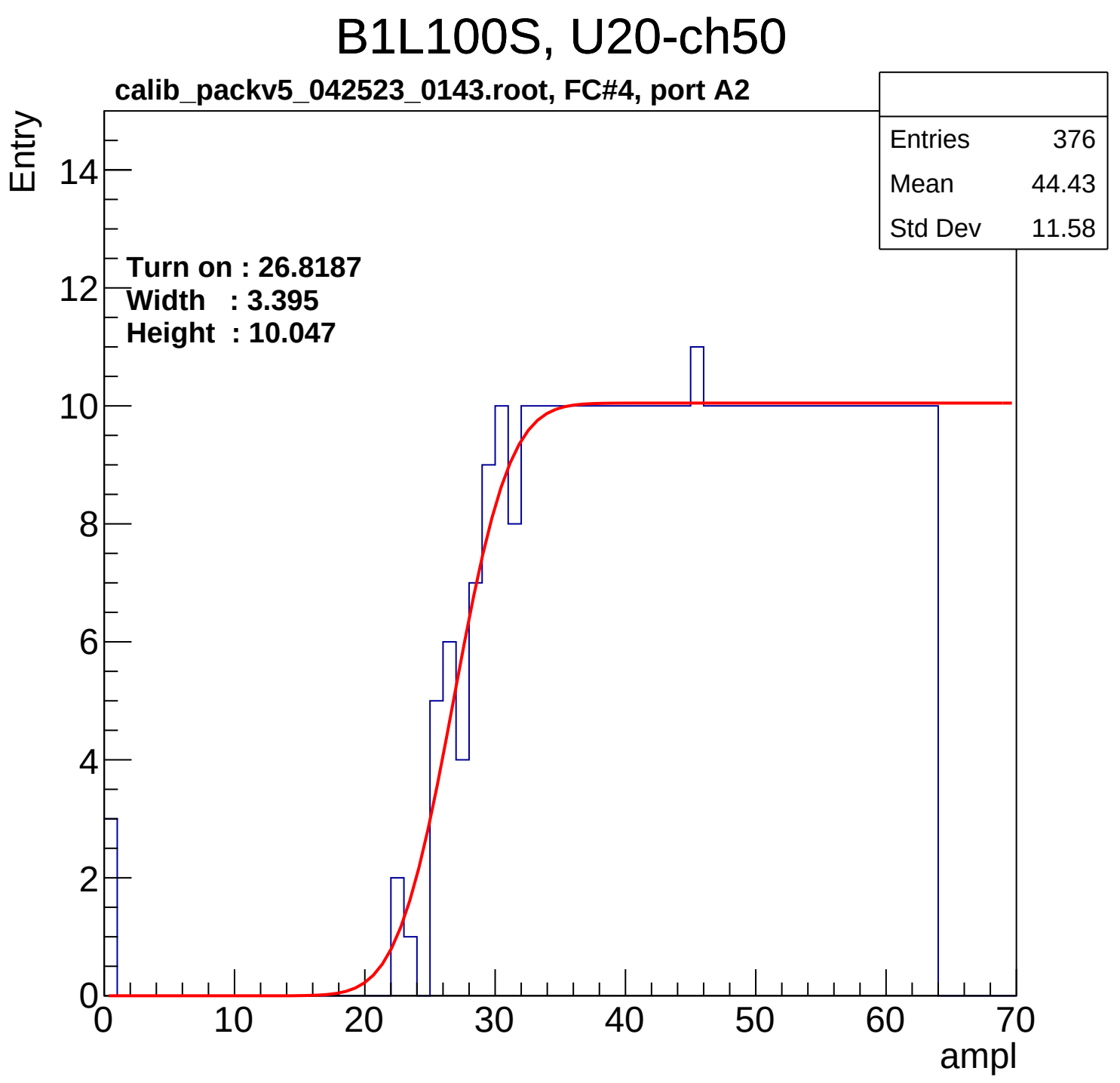
B1L100S, U20-ch50
calib_packv5_042523_0143.root, FC#4, port A2
Entries 376
Mean 44.43
Std Dev 11.58
Turn on : 26.8187
Width : 3.395
Height : 10.047
Entry
ampl
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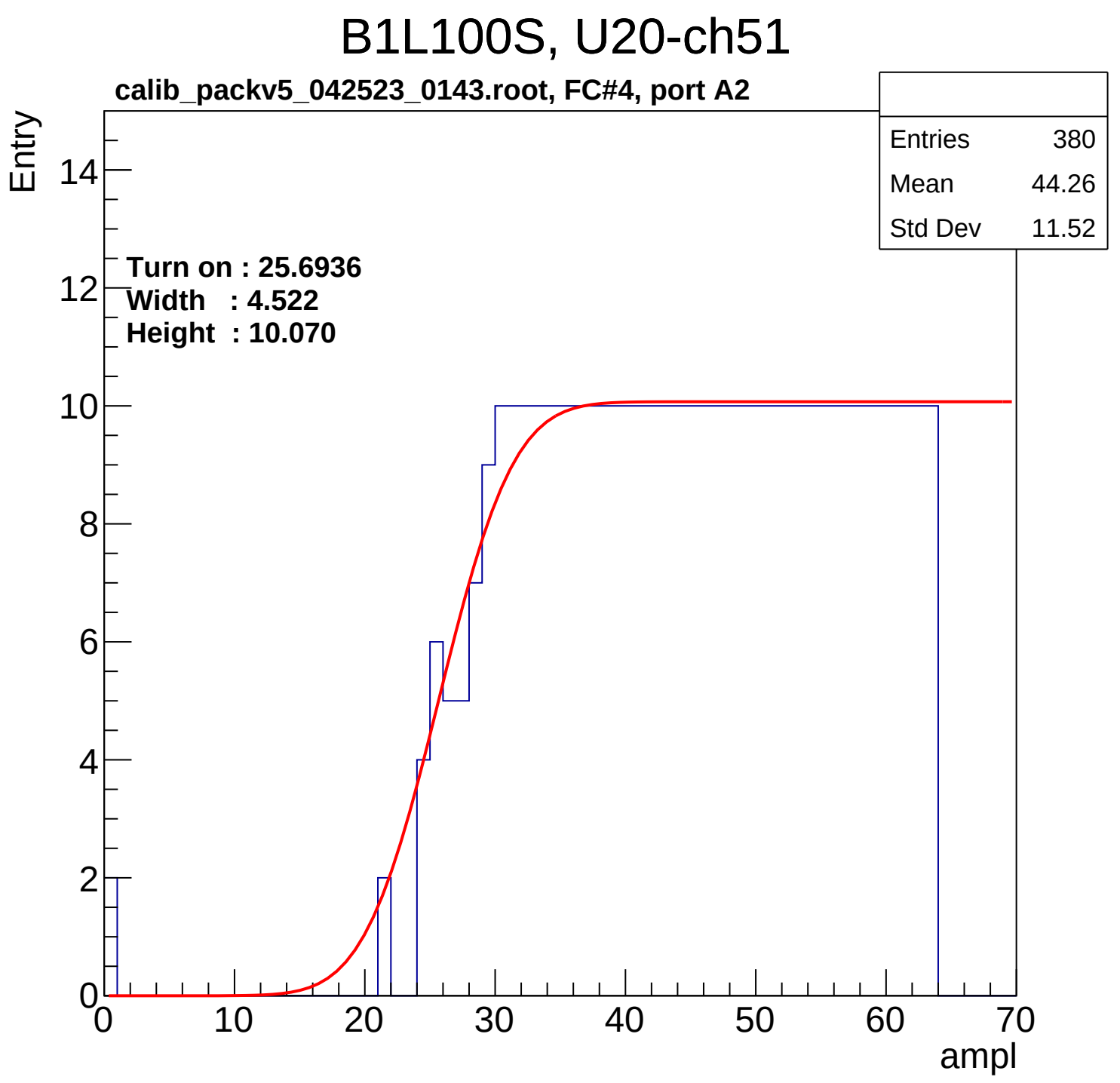
B1L100S, U20-ch51
calib_packv5_042523_0143.root, FC#4, port A2
Entries 380
Mean 44.26
Std Dev 11.52
Turn on : 25.6936
Width : 4.522
Height : 10.070
Entry
ampl
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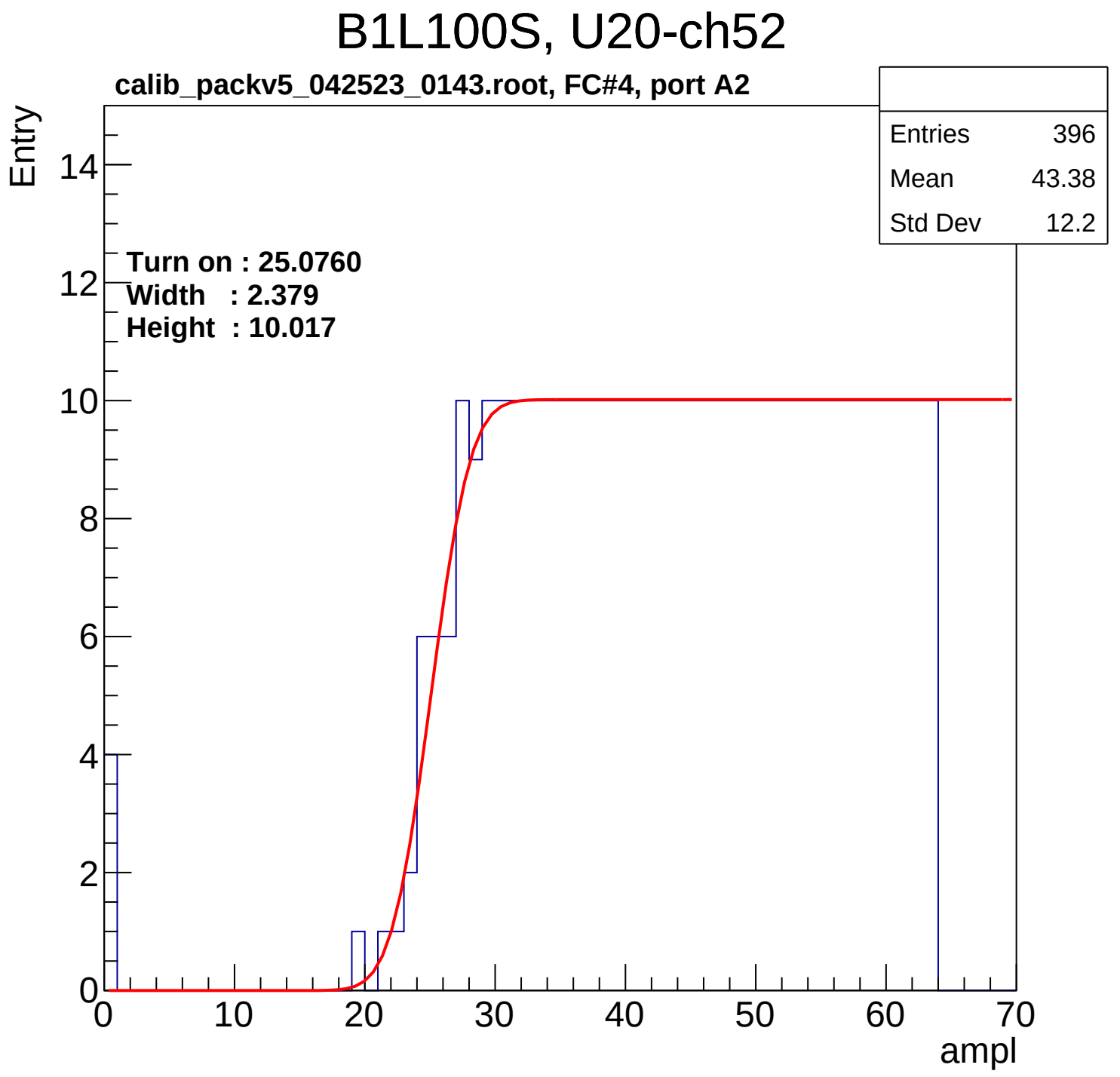
B1L100S, U20-ch52
calib_packv5_042523_0143.root, FC#4, port A2
Entries 396
Mean 43.38
Std Dev 12.2
Turn on : 25.0760
Width : 2.379
Height : 10.017
Entry
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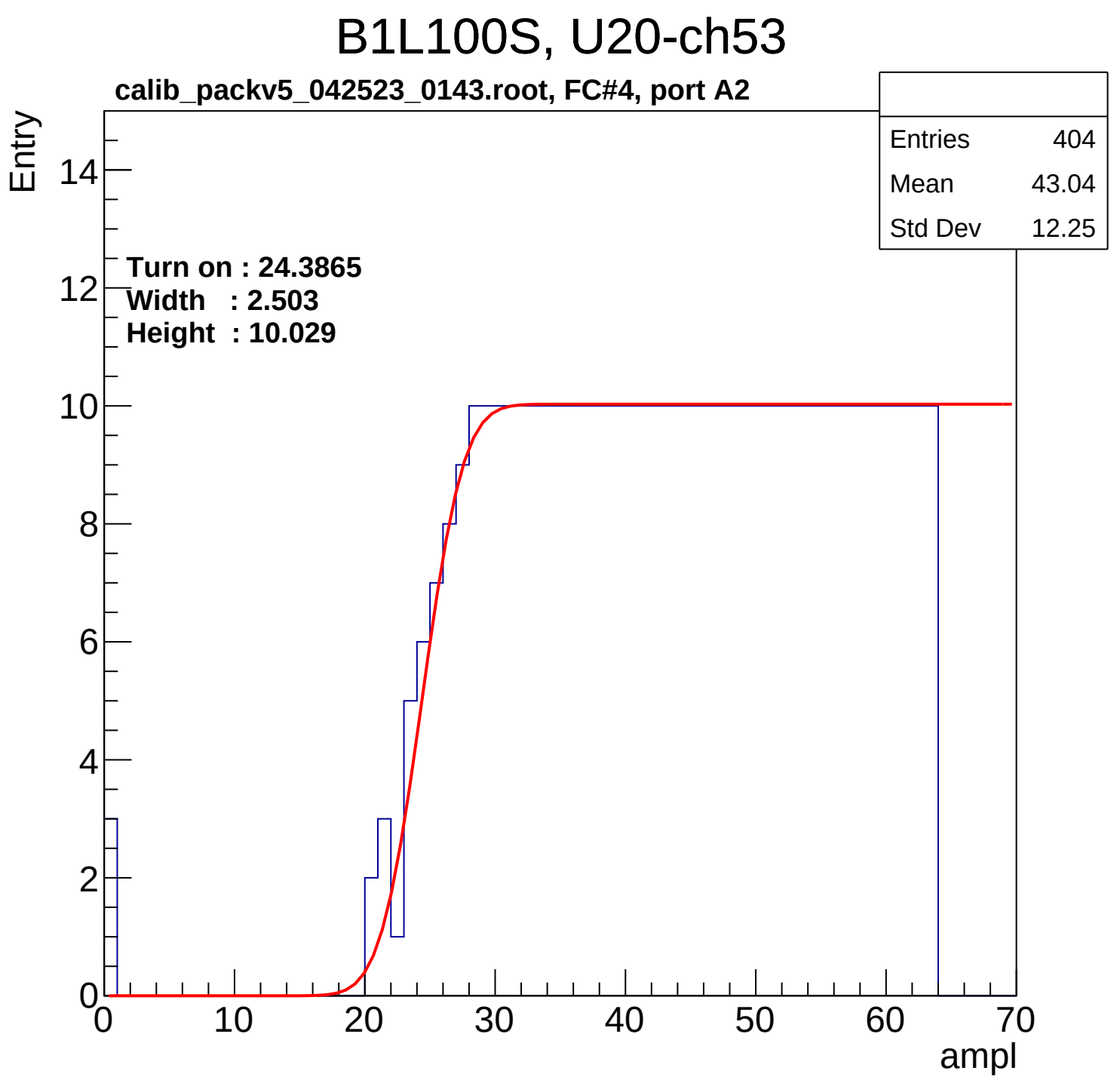
B1L100S, U20-ch53
calib_packv5_042523_0143.root, FC#4, port A2
Entries 404
Mean 43.04
Std Dev 12.25
Turn on : 24.3865
Width : 2.503
Height : 10.029
Entry
ampl
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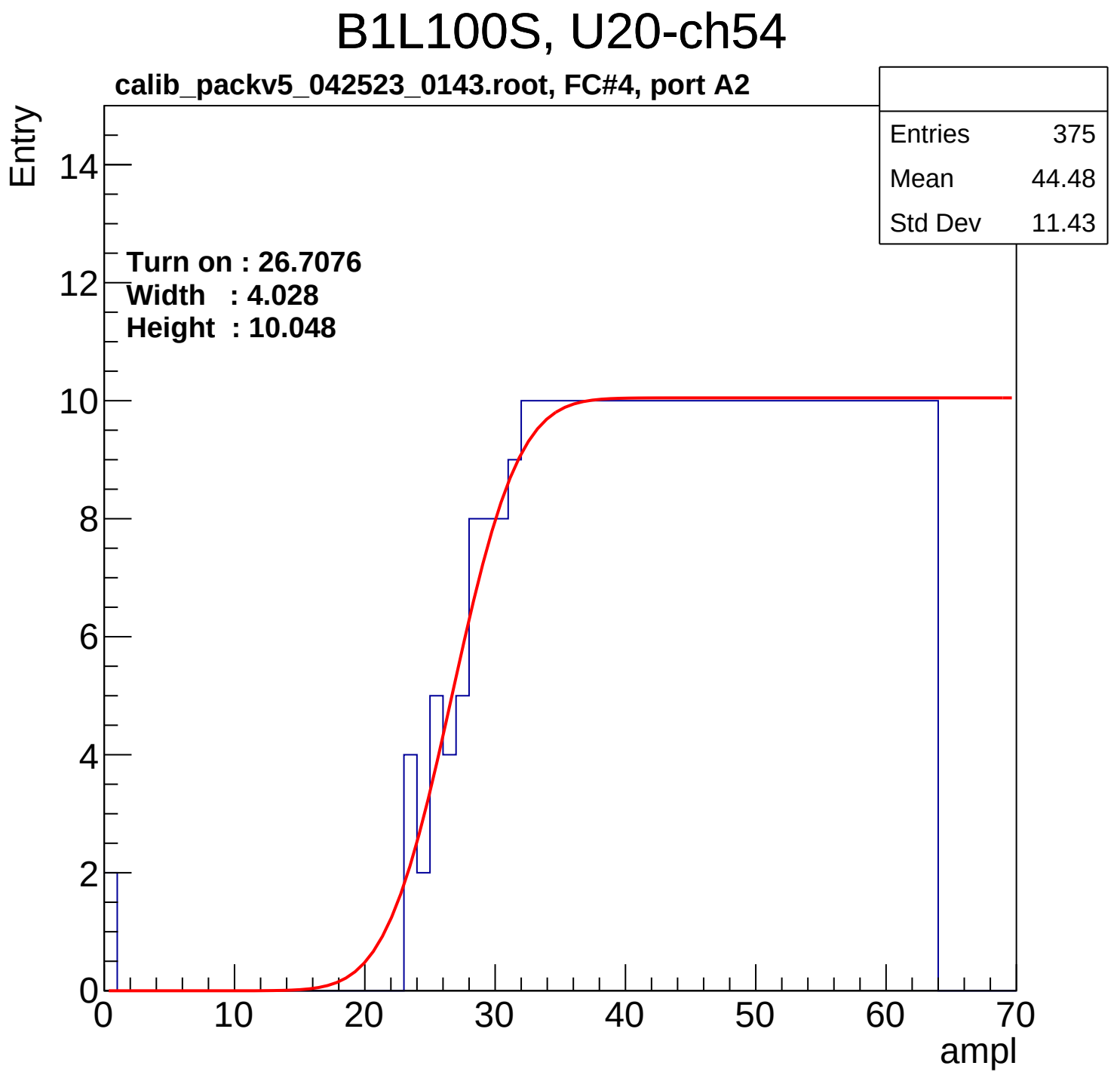
B1L100S, U20-ch54
calib_packv5_042523_0143.root, FC#4, port A2
Entries 375
Mean 44.48
Std Dev 11.43
Turn on : 26.7076
Width : 4.028
Height : 10.048
Entry
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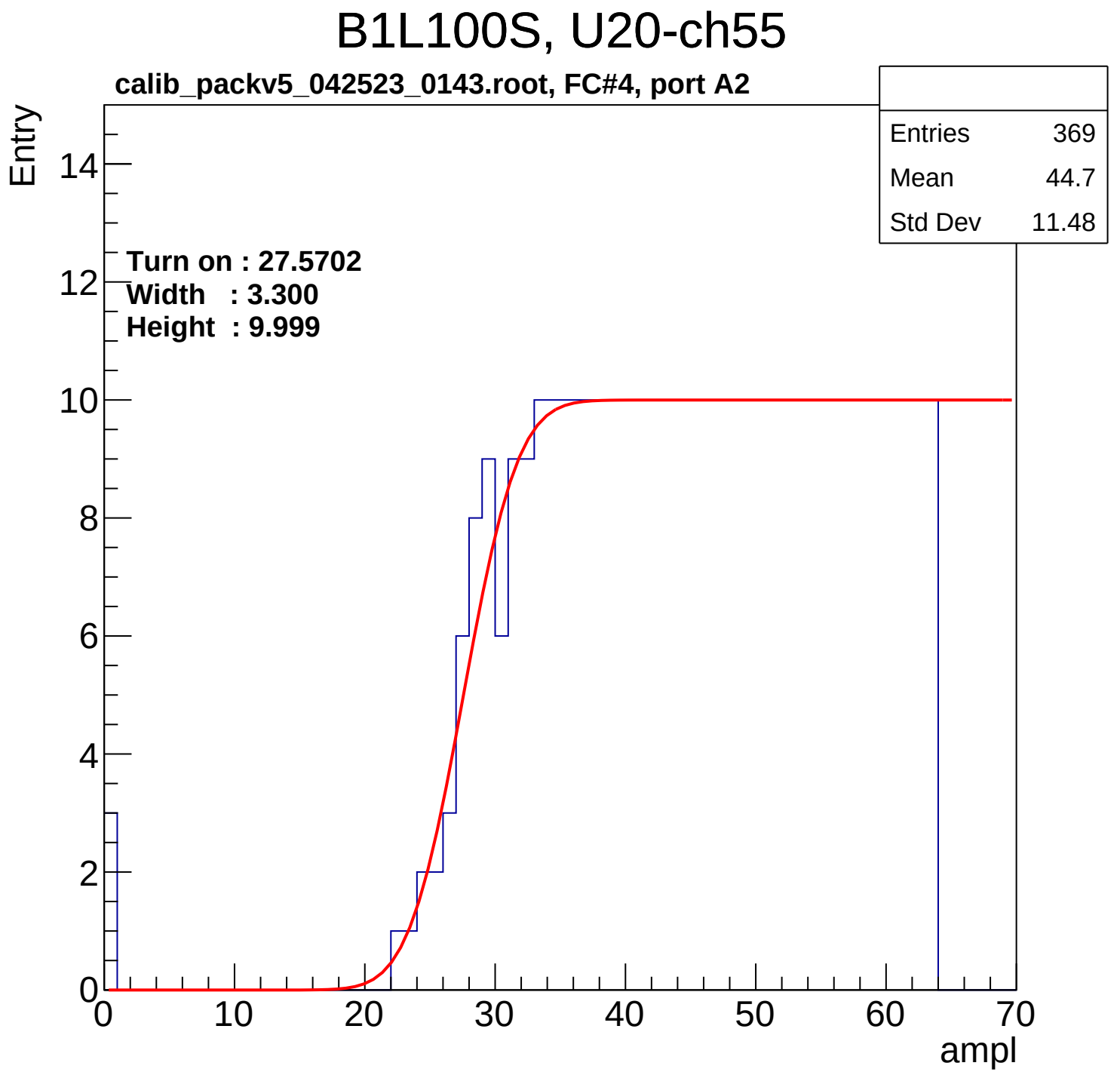
B1L100S, U20-ch55
calib_packv5_042523_0143.root, FC#4, port A2
Entries 369
Mean 44.7
Std Dev 11.48
Turn on : 27.5702
Width : 3.300
Height : 9.999
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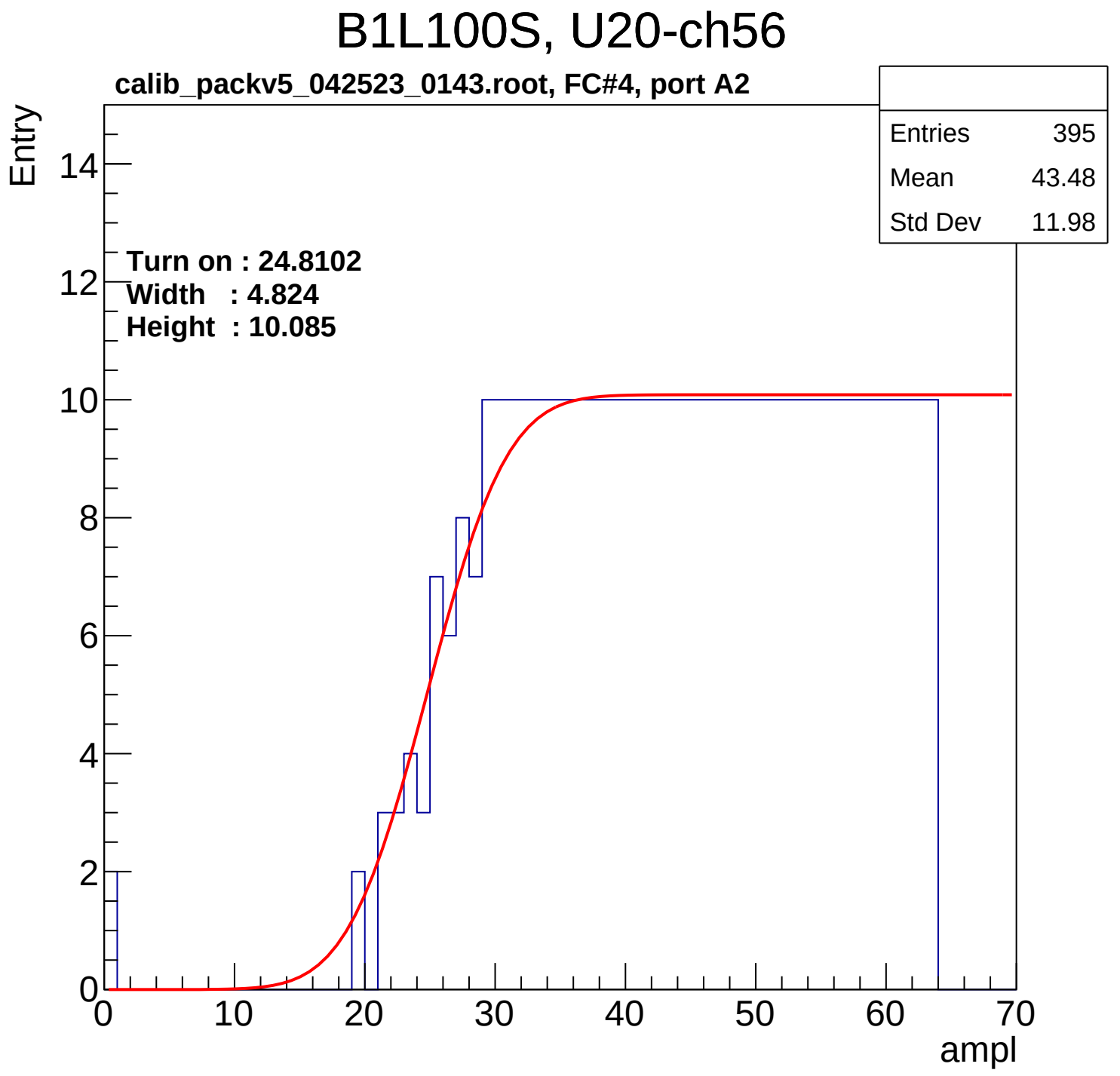
B1L100S, U20-ch56
calib_packv5_042523_0143.root, FC#4, port A2
Entries 395
Mean 43.48
Std Dev 11.98
Turn on : 24.8102
Width : 4.824
Height : 10.085
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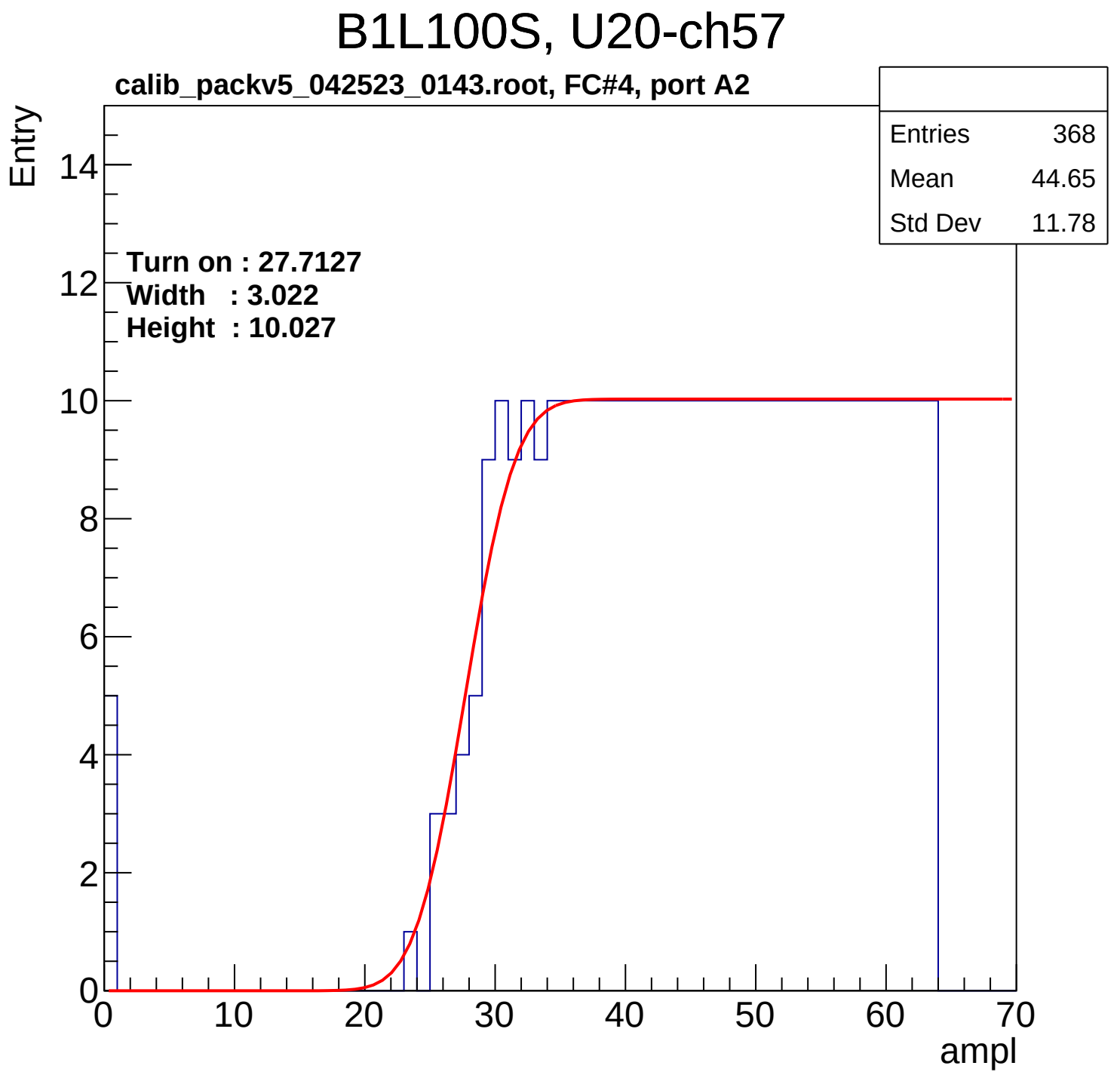
B1L100S, U20-ch57
calib_packv5_042523_0143.root, FC#4, port A2
Entries 368
Mean 44.65
Std Dev 11.78
Turn on : 27.7127
Width : 3.022
Height : 10.027
Entry
ampl
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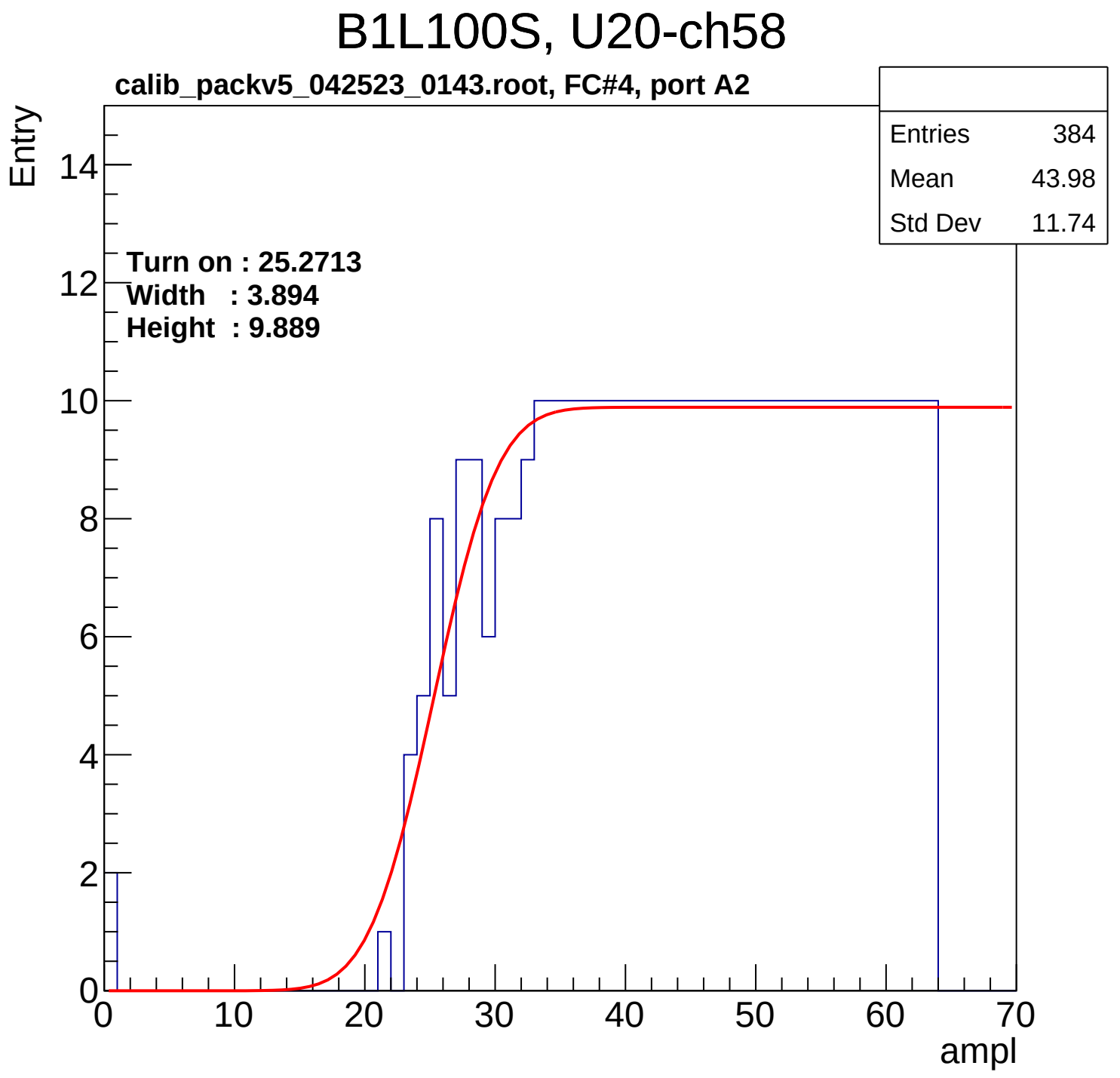
B1L100S, U20-ch58
calib_packv5_042523_0143.root, FC#4, port A2
Entries 384
Mean 43.98
Std Dev 11.74
Turn on : 25.2713
Width : 3.894
Height : 9.889
Entry
ampl
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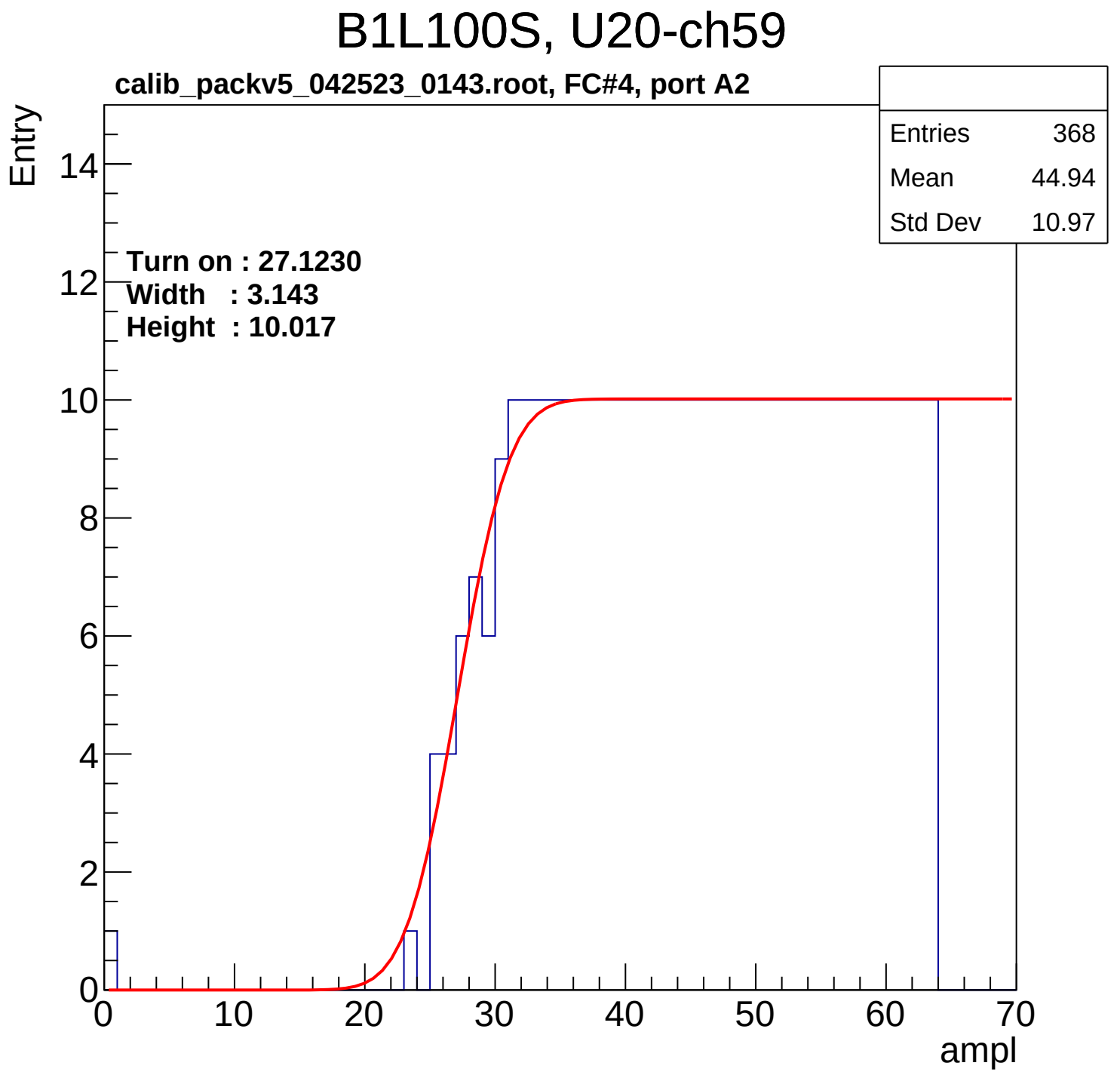
B1L100S, U20-ch59
calib_packv5_042523_0143.root, FC#4, port A2
Entries 368
Mean 44.94
Std Dev 10.97
Turn on : 27.1230
Width : 3.143
Height : 10.017
Entry
ampl
0
2
4
6
8
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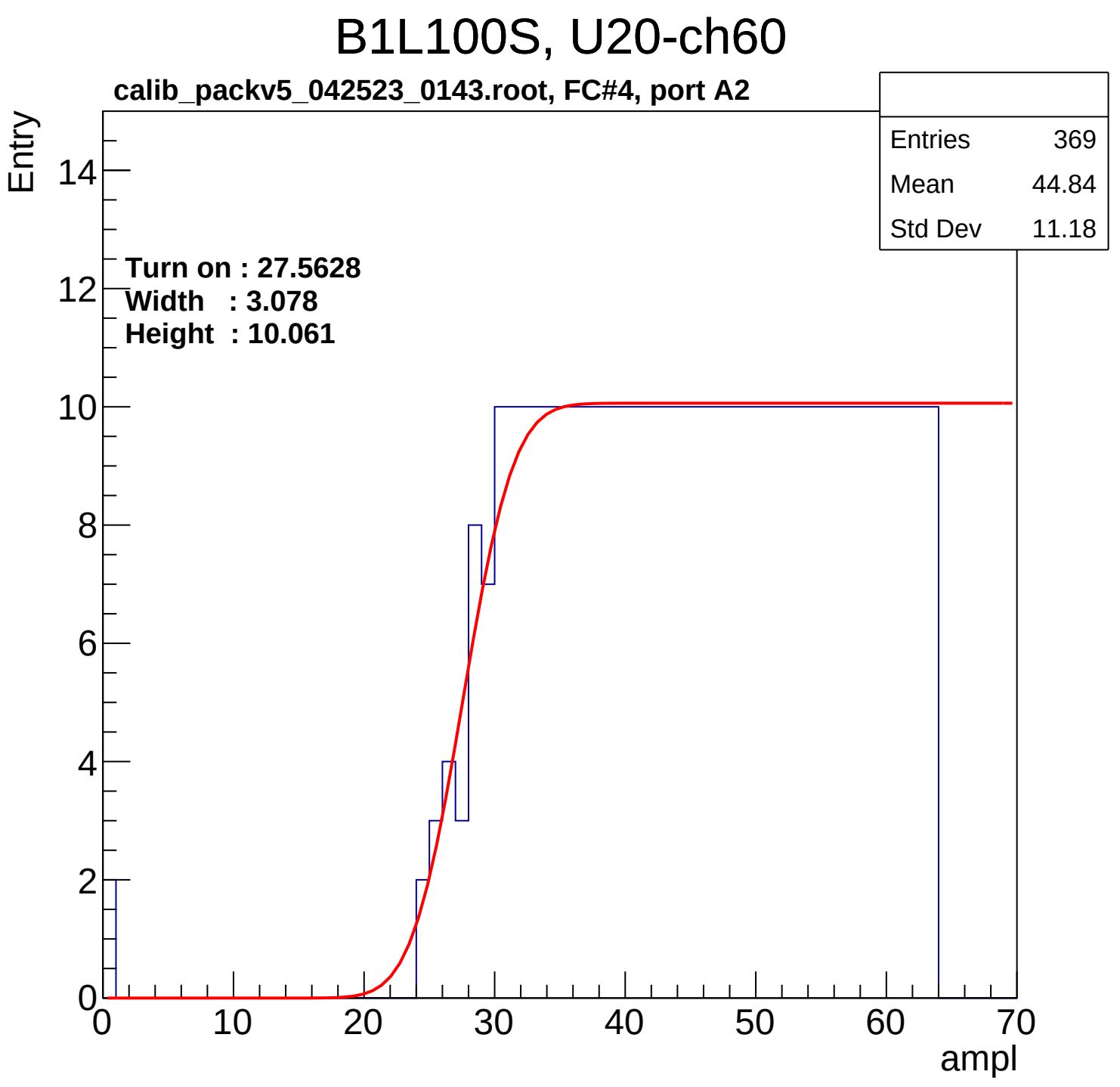
B1L100S, U20-ch60
calib_packv5_042523_0143.root, FC#4, port A2
Entries 369
Mean 44.84
Std Dev 11.18
Turn on : 27.5628
Width : 3.078
Height : 10.061
Entry
ampl
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2
4
6
8
10
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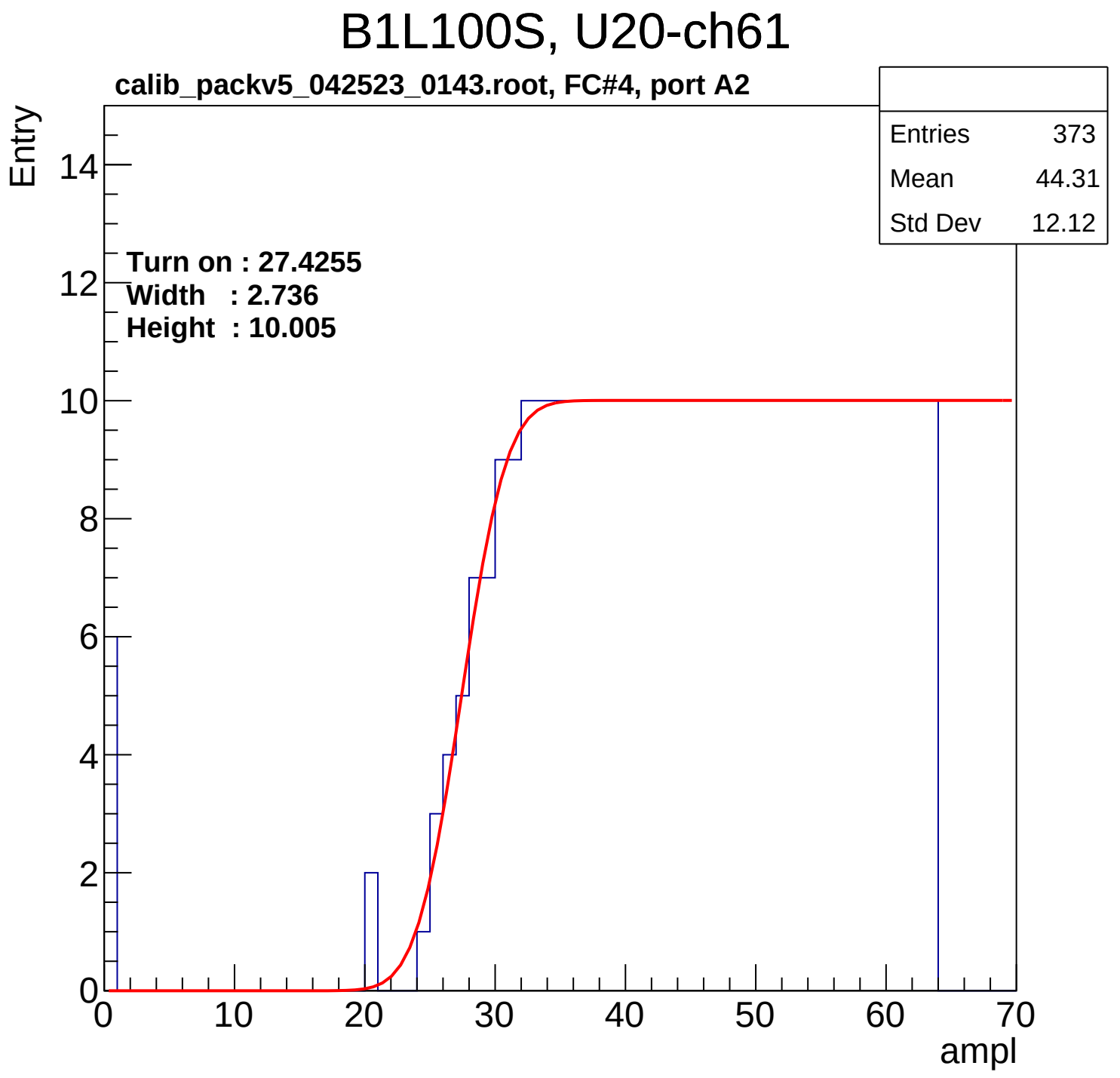
B1L100S, U20-ch61
calib_packv5_042523_0143.root, FC#4, port A2
Entries 373
Mean 44.31
Std Dev 12.12
Turn on : 27.4255
Width : 2.736
Height : 10.005
Entry
ampl
0
2
4
6
8
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0
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60
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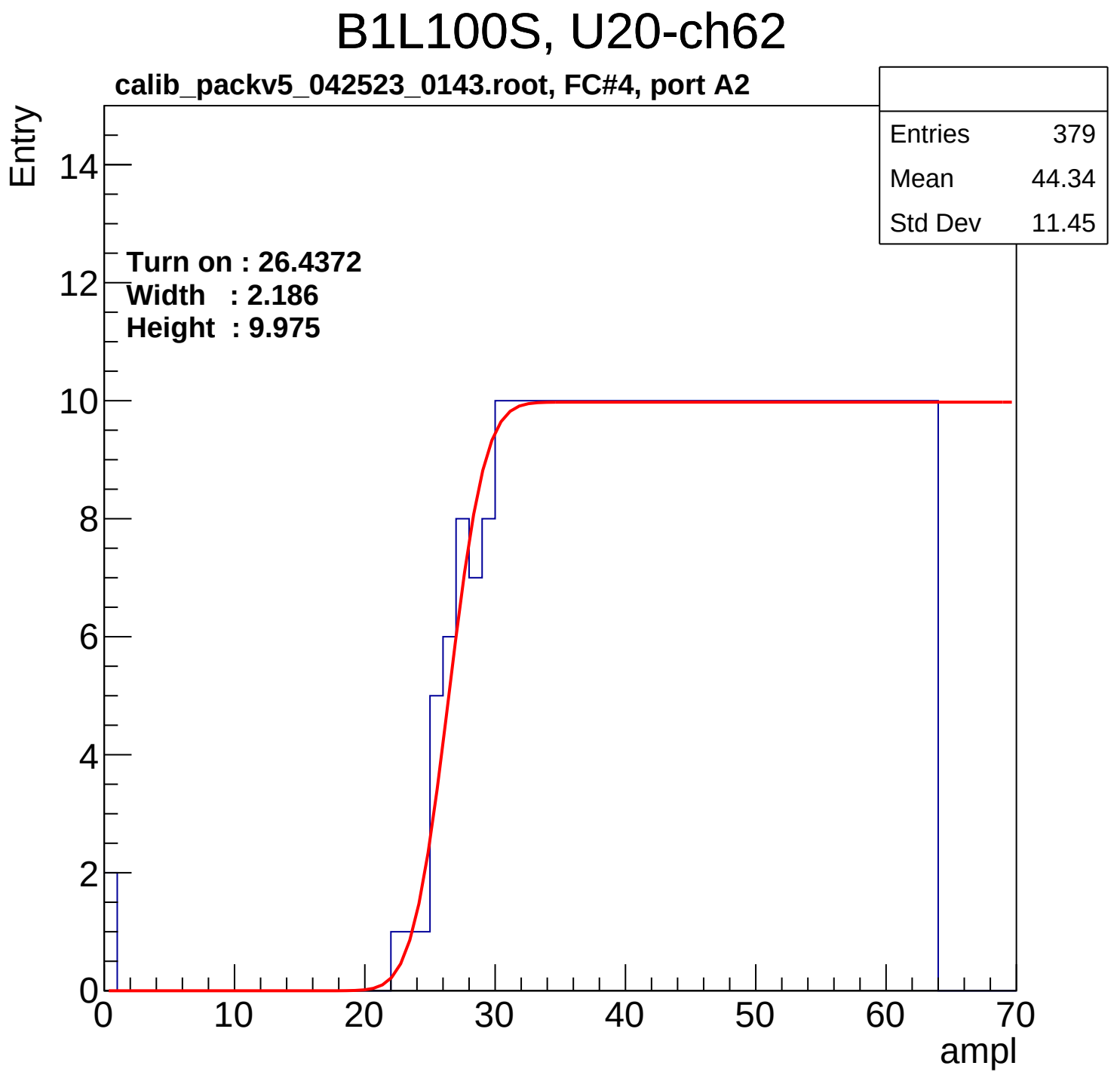
B1L100S, U20-ch62
calib_packv5_042523_0143.root, FC#4, port A2
Entries 379
Mean 44.34
Std Dev 11.45
Turn on : 26.4372
Width : 2.186
Height : 9.975
Entry
ampl
0
2
4
6
8
10
12
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0
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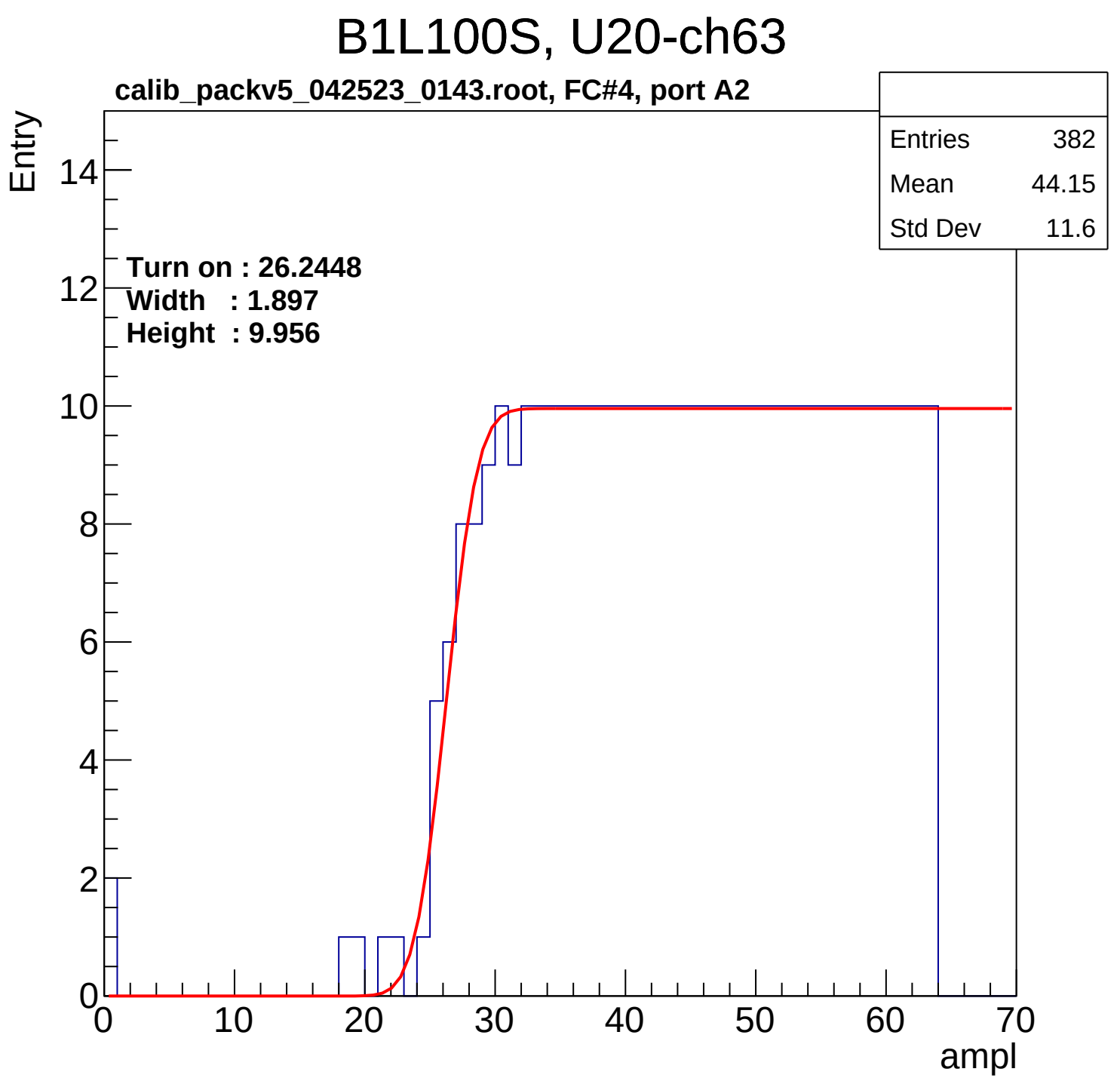
B1L100S, U20-ch63
calib_packv5_042523_0143.root, FC#4, port A2
Entries 382
Mean 44.15
Std Dev 11.6
Turn on : 26.2448
Width : 1.897
Height : 9.956
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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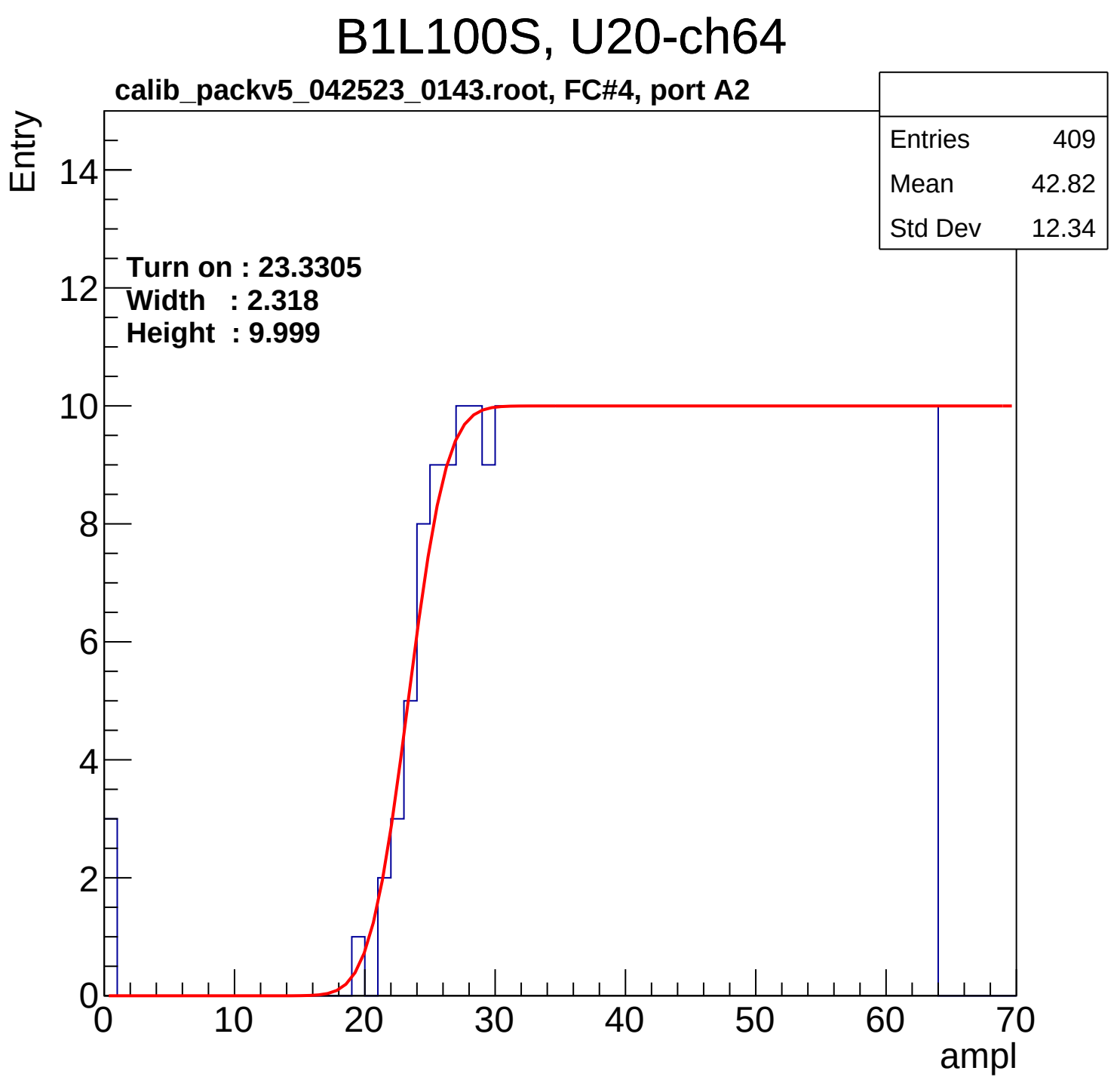
B1L100S, U20-ch64
calib_packv5_042523_0143.root, FC#4, port A2
Entries 409
Mean 42.82
Std Dev 12.34
Turn on : 23.3305
Width : 2.318
Height : 9.999
Entry
ampl
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2
4
6
8
10
12
14
0
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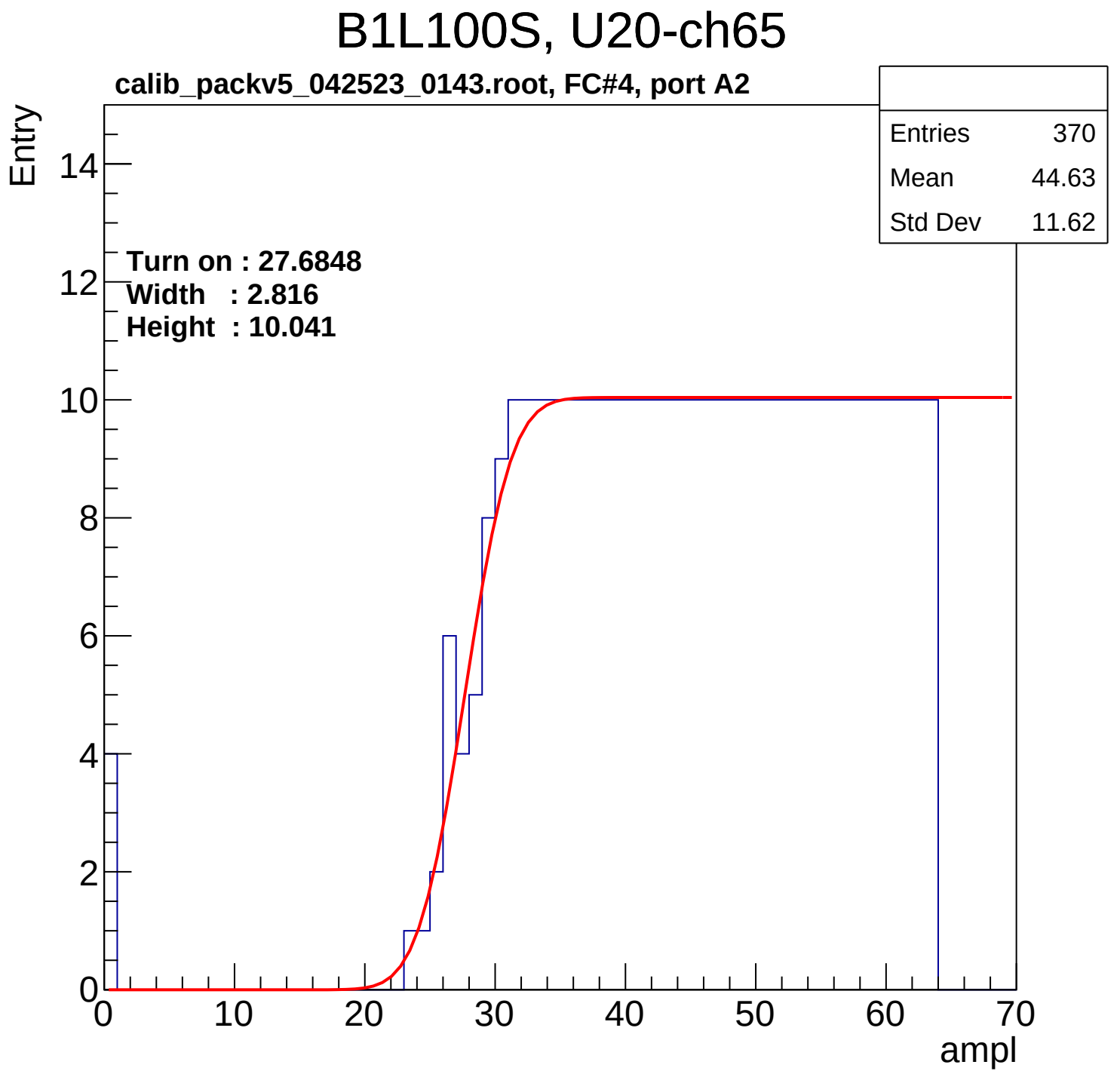
B1L100S, U20-ch65
calib_packv5_042523_0143.root, FC#4, port A2
Entries 370
Mean 44.63
Std Dev 11.62
Turn on : 27.6848
Width : 2.816
Height : 10.041
Entry
ampl
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2
4
6
8
10
12
14
0
10
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40
50
60
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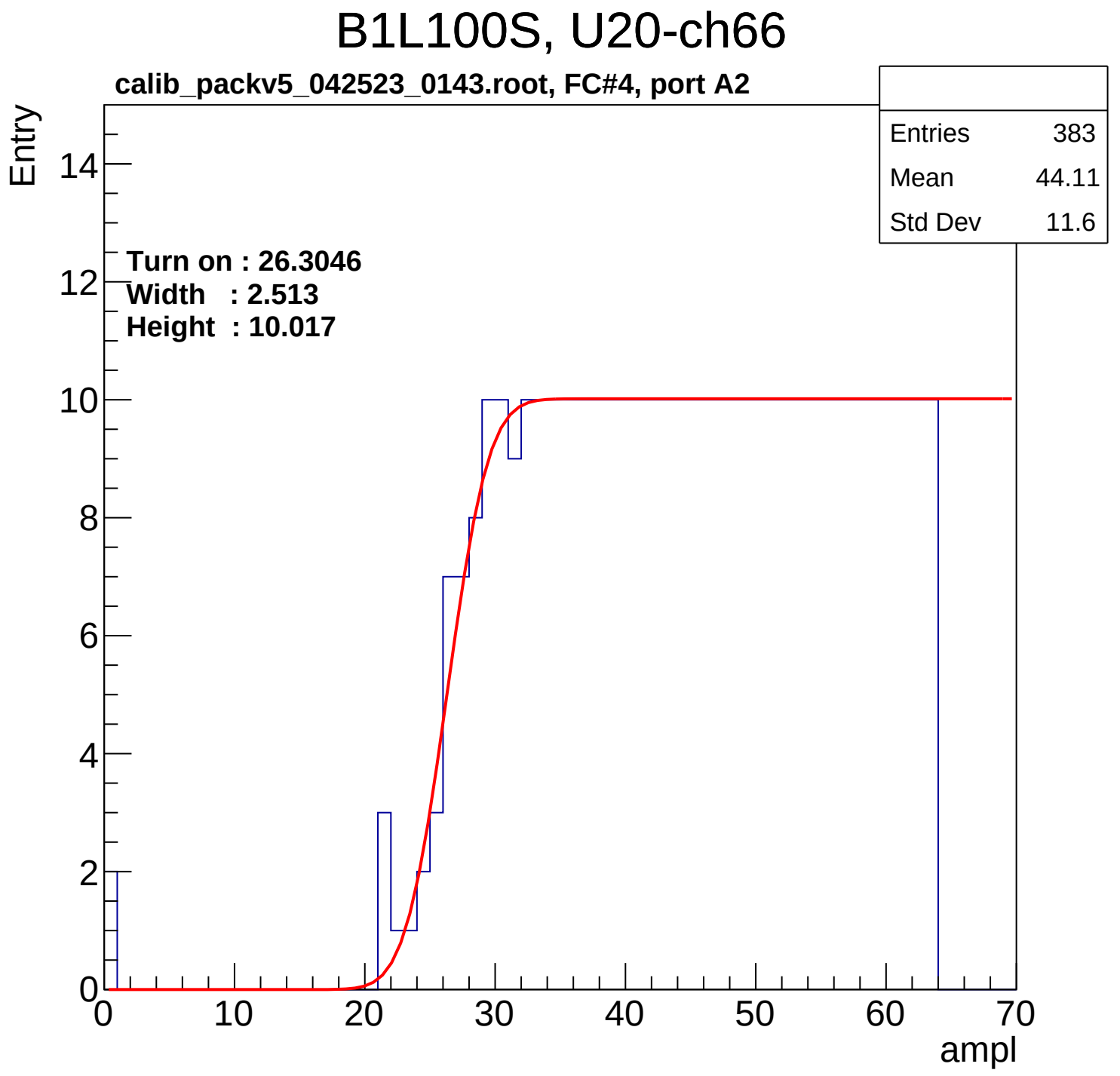
B1L100S, U20-ch66
calib_packv5_042523_0143.root, FC#4, port A2
Entries 383
Mean 44.11
Std Dev 11.6
Turn on : 26.3046
Width : 2.513
Height : 10.017
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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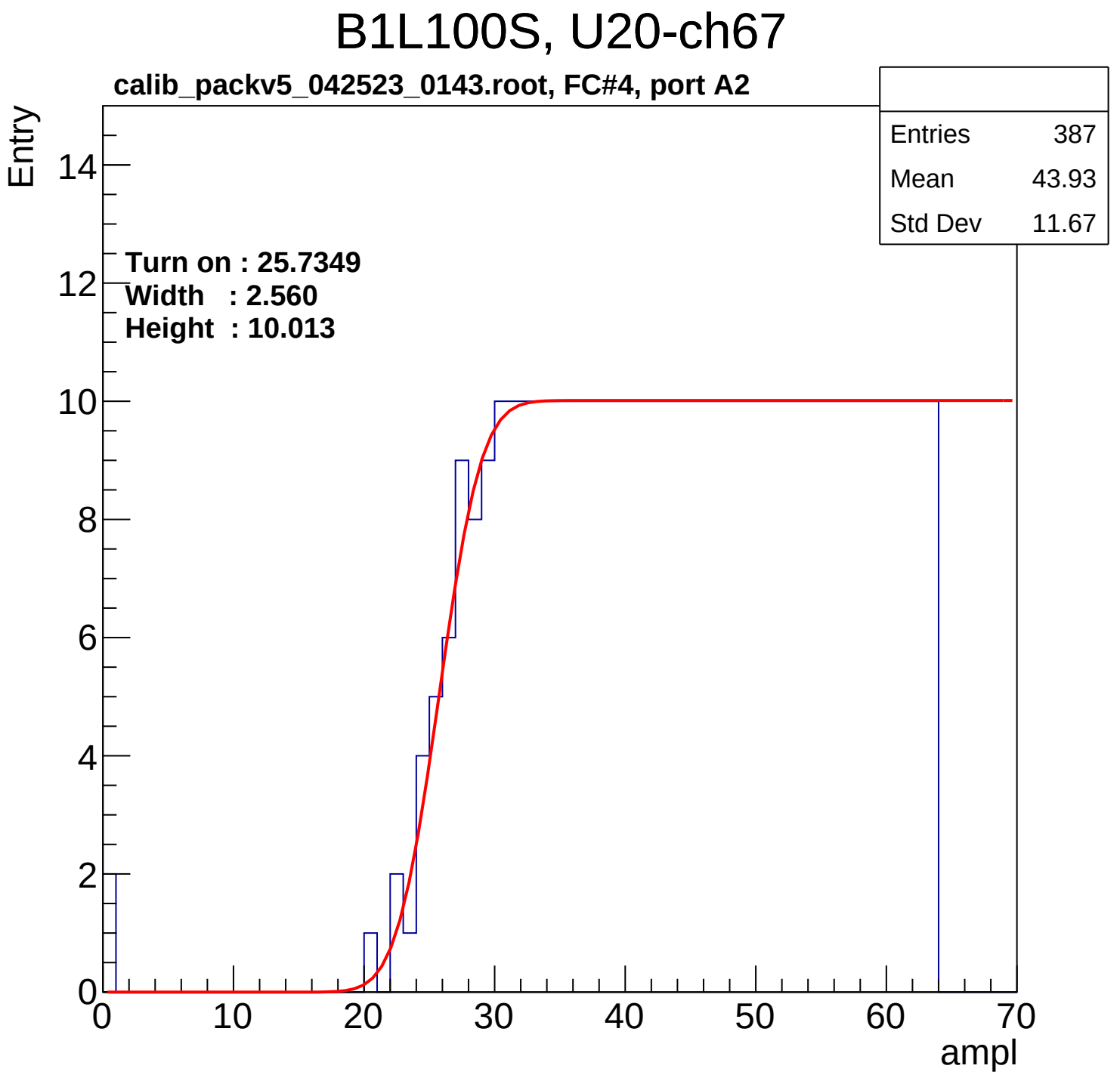
B1L100S, U20-ch67
calib_packv5_042523_0143.root, FC#4, port A2
Entries 387
Mean 43.93
Std Dev 11.67
Turn on : 25.7349
Width : 2.560
Height : 10.013
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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60
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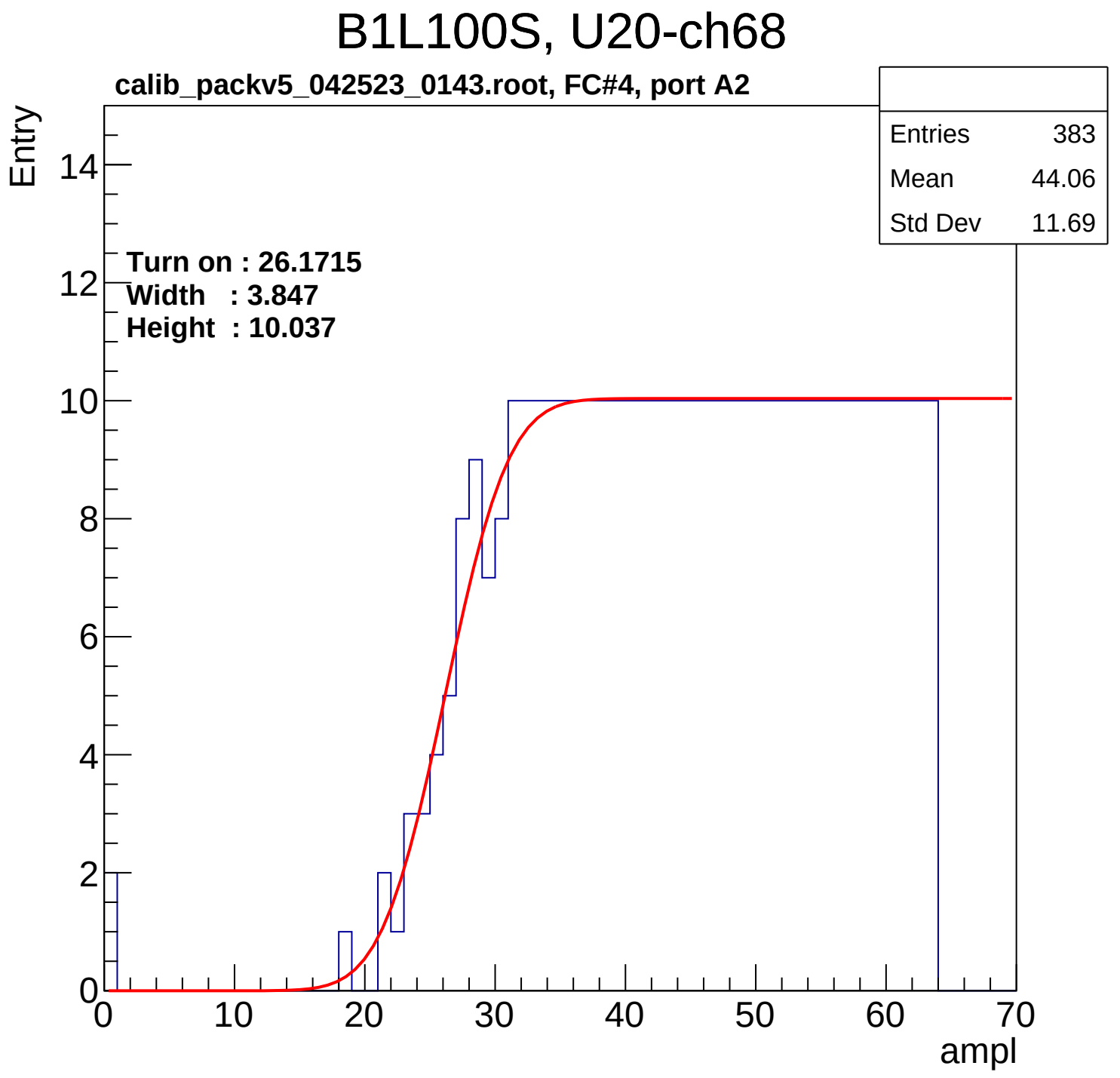
B1L100S, U20-ch68
calib_packv5_042523_0143.root, FC#4, port A2
Entries 383
Mean 44.06
Std Dev 11.69
Turn on : 26.1715
Width : 3.847
Height : 10.037
Entry
ampl
0
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6
8
10
12
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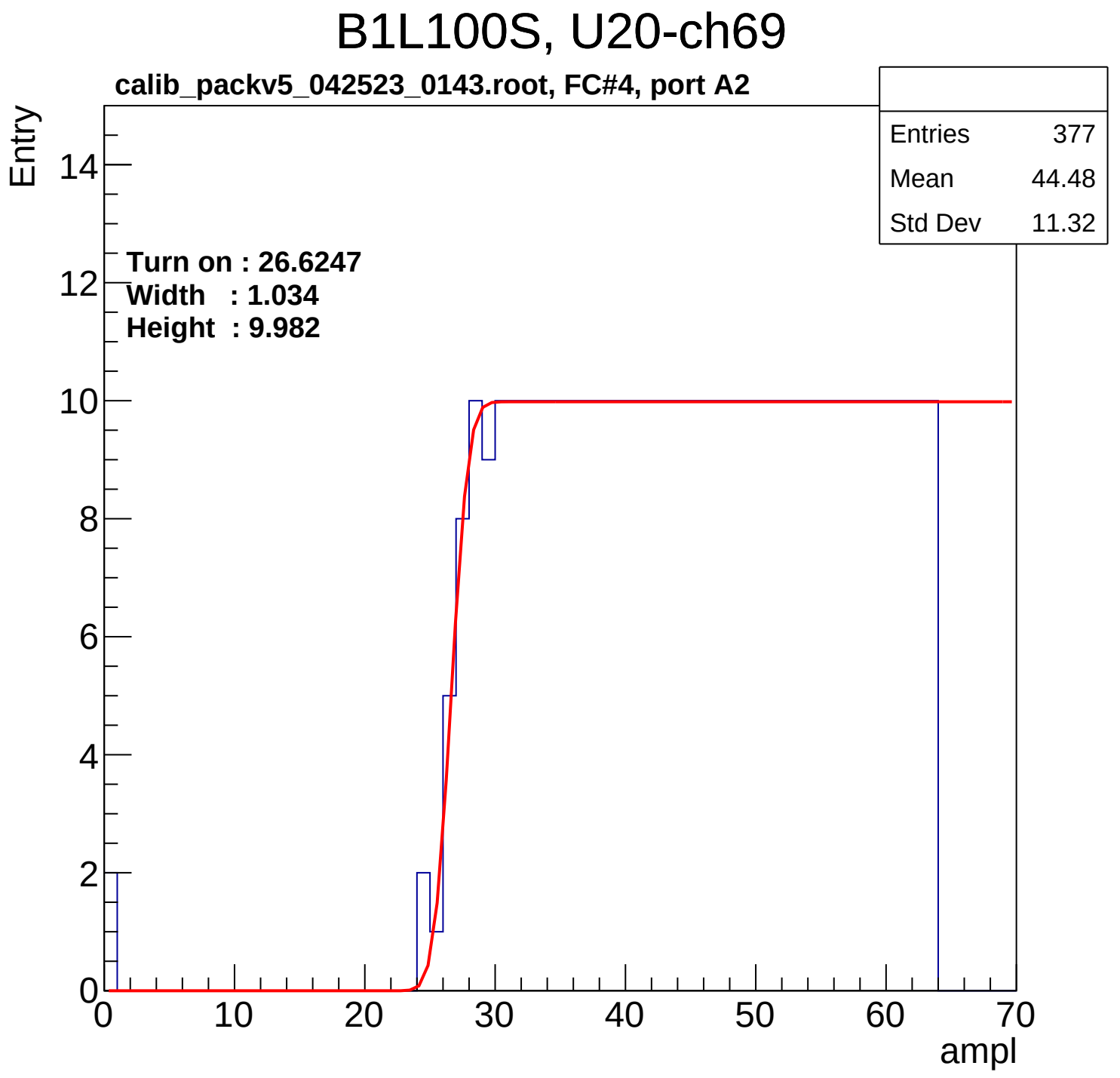
B1L100S, U20-ch69
calib_packv5_042523_0143.root, FC#4, port A2
Entries 377
Mean 44.48
Std Dev 11.32
Turn on : 26.6247
Width : 1.034
Height : 9.982
Entry
ampl
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6
8
10
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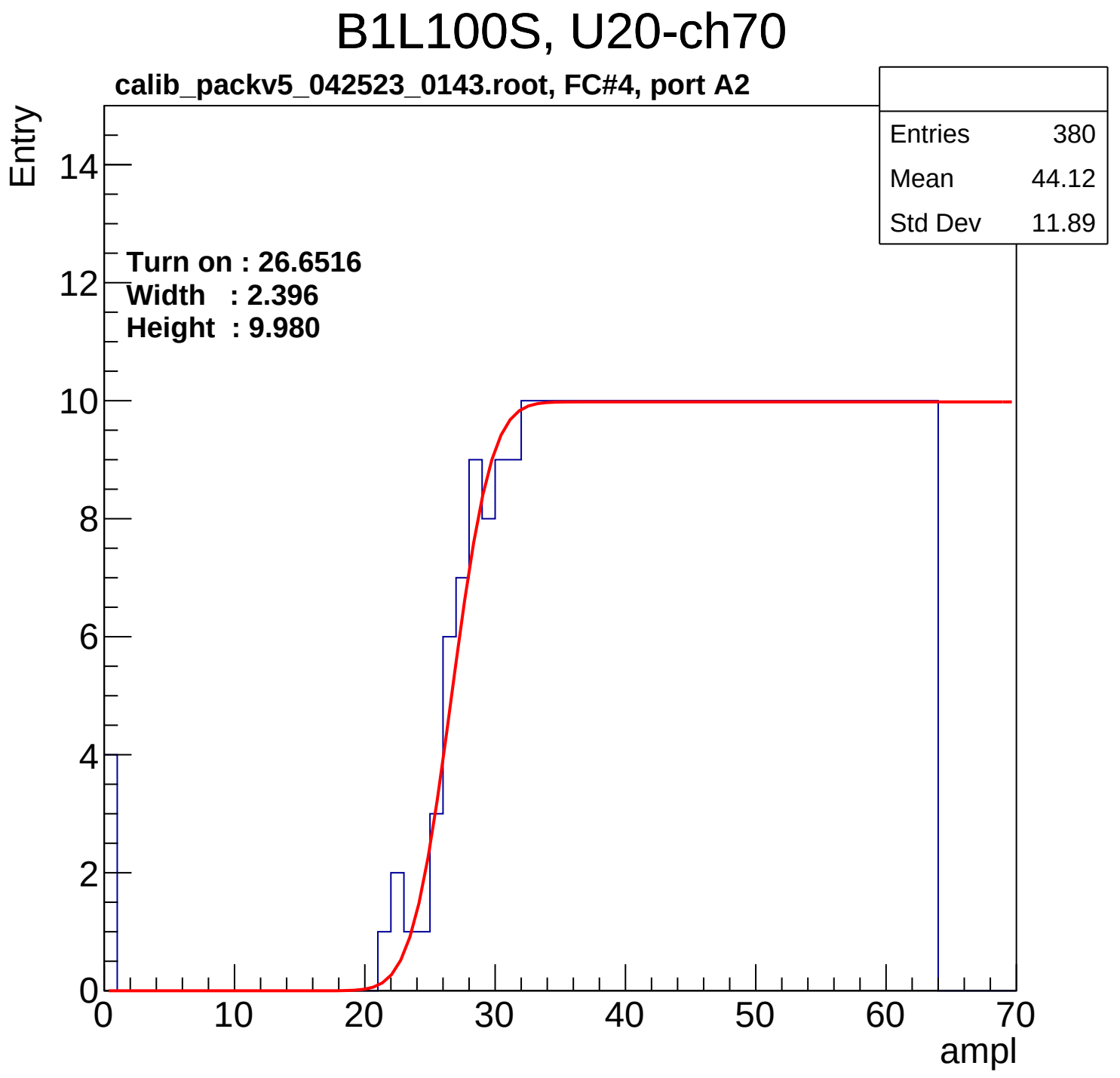
B1L100S, U20-ch70
calib_packv5_042523_0143.root, FC#4, port A2
Entries 380
Mean 44.12
Std Dev 11.89
Turn on : 26.6516
Width : 2.396
Height : 9.980
Entry
ampl
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6
8
10
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0
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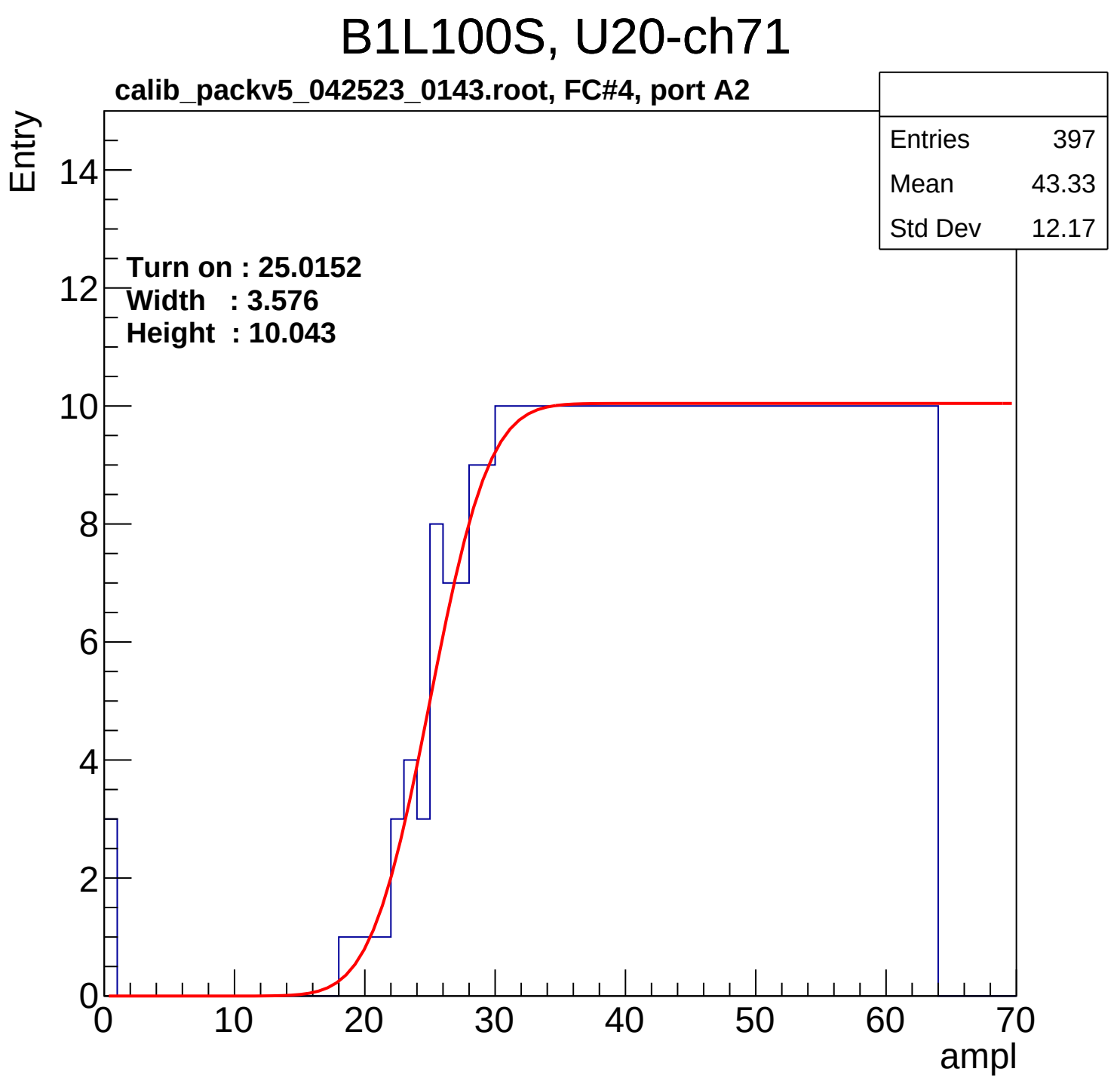
B1L100S, U20-ch71
calib_packv5_042523_0143.root, FC#4, port A2
Entries 397
Mean 43.33
Std Dev 12.17
Turn on : 25.0152
Width : 3.576
Height : 10.043
Entry
ampl
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4
6
8
10
12
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0
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60
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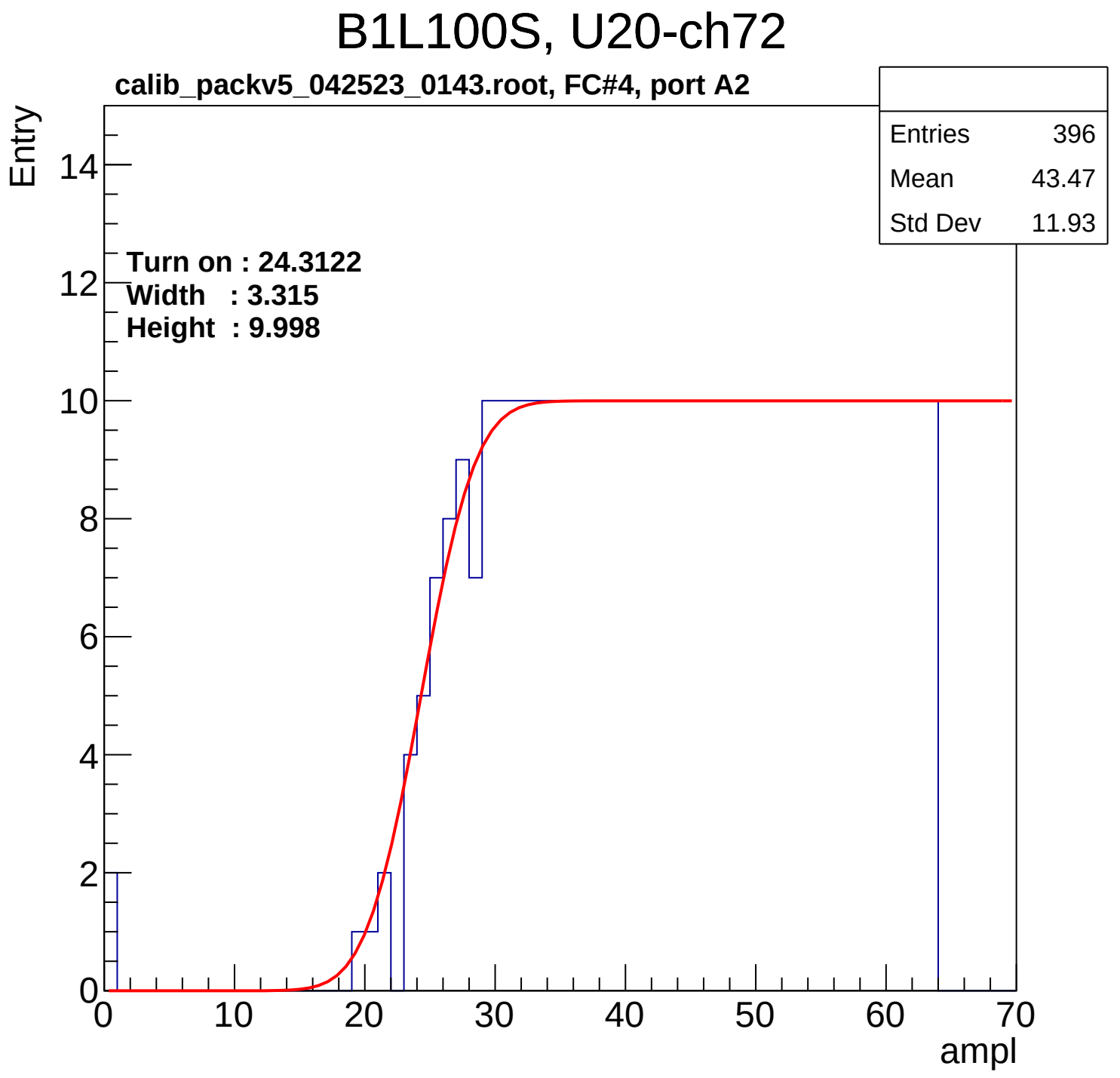
B1L100S, U20-ch72
calib_packv5_042523_0143.root, FC#4, port A2
Entries 396
Mean 43.47
Std Dev 11.93
Turn on : 24.3122
Width : 3.315
Height : 9.998
Entry
ampl
0
2
4
6
8
10
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0
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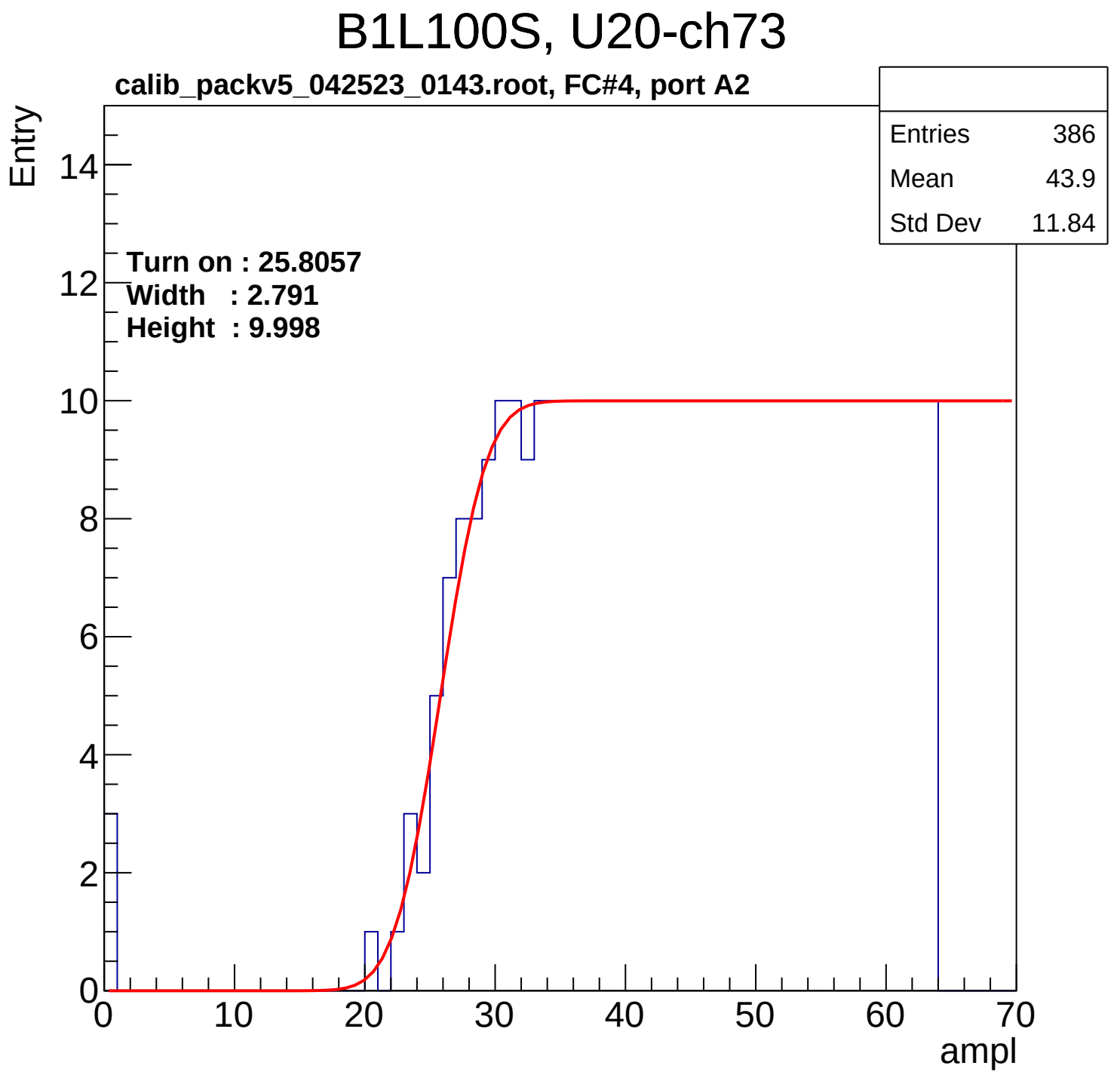
B1L100S, U20-ch73
calib_packv5_042523_0143.root, FC#4, port A2
Entries 386
Mean 43.9
Std Dev 11.84
Turn on : 25.8057
Width : 2.791
Height : 9.998
Entry
ampl
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6
8
10
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0
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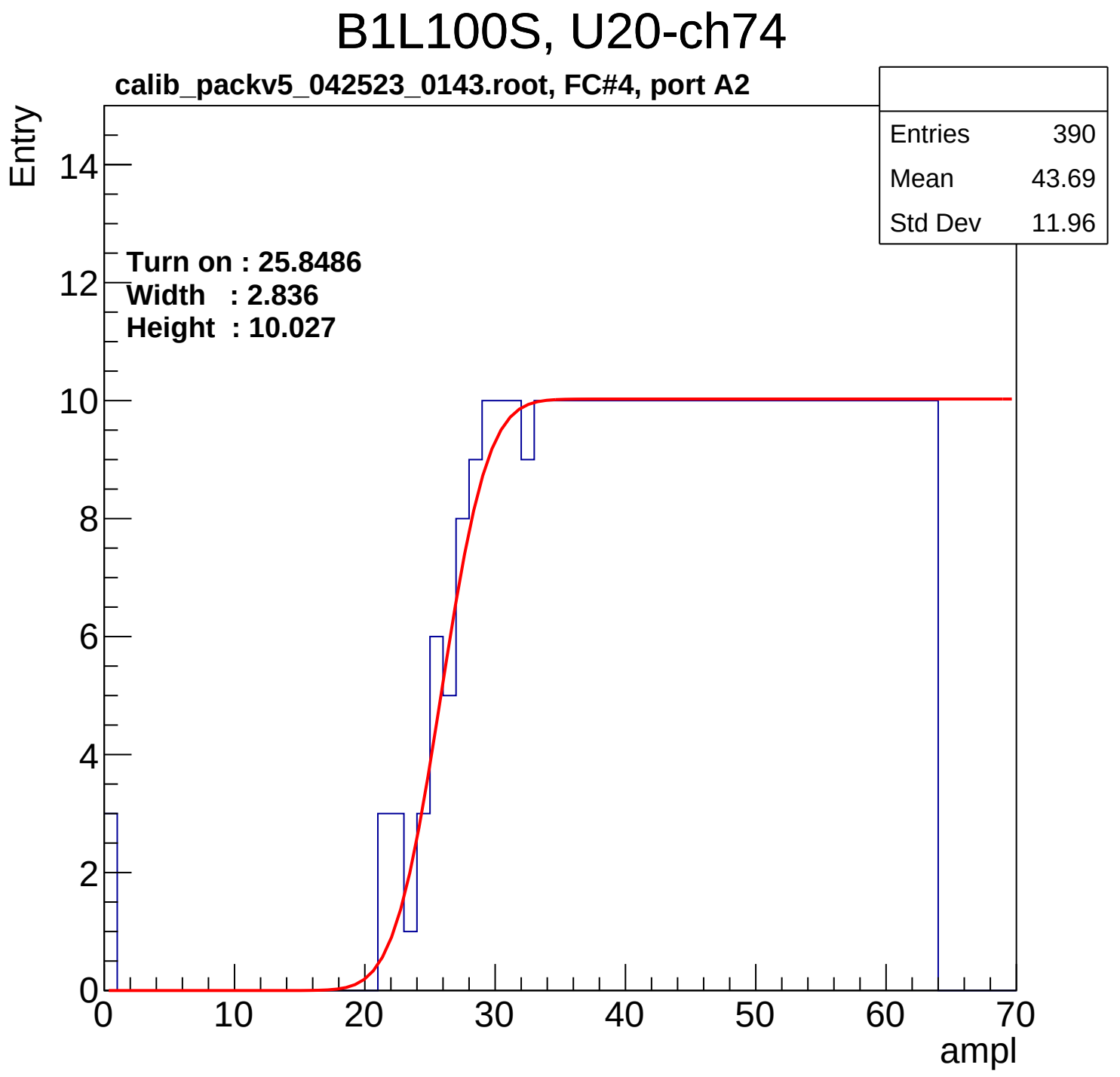
B1L100S, U20-ch74
calib_packv5_042523_0143.root, FC#4, port A2
Entries 390
Mean 43.69
Std Dev 11.96
Turn on : 25.8486
Width : 2.836
Height : 10.027
Entry
ampl
0
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6
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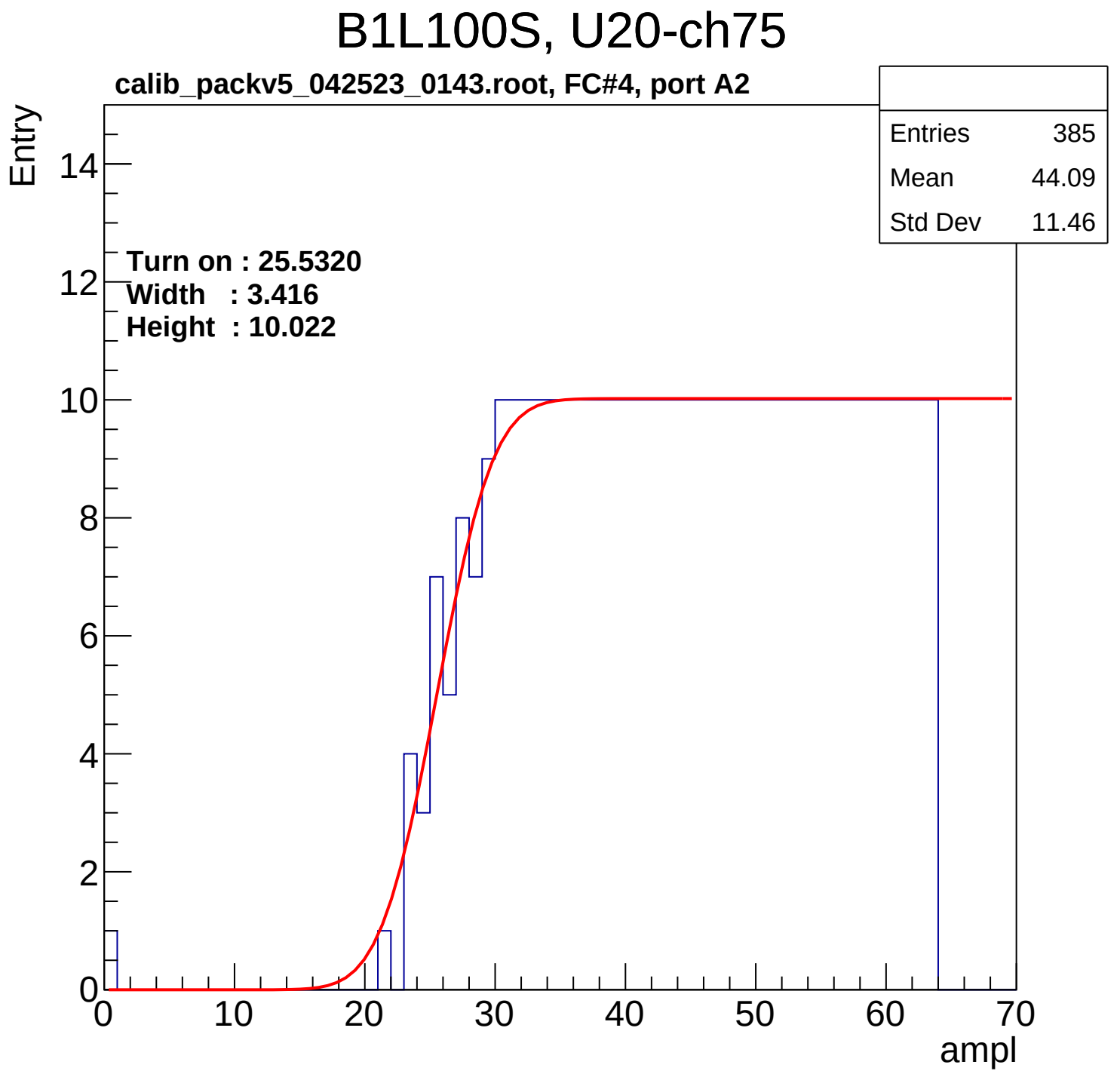
B1L100S, U20-ch75
calib_packv5_042523_0143.root, FC#4, port A2
Entries 385
Mean 44.09
Std Dev 11.46
Turn on : 25.5320
Width : 3.416
Height : 10.022
Entry
ampl
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8
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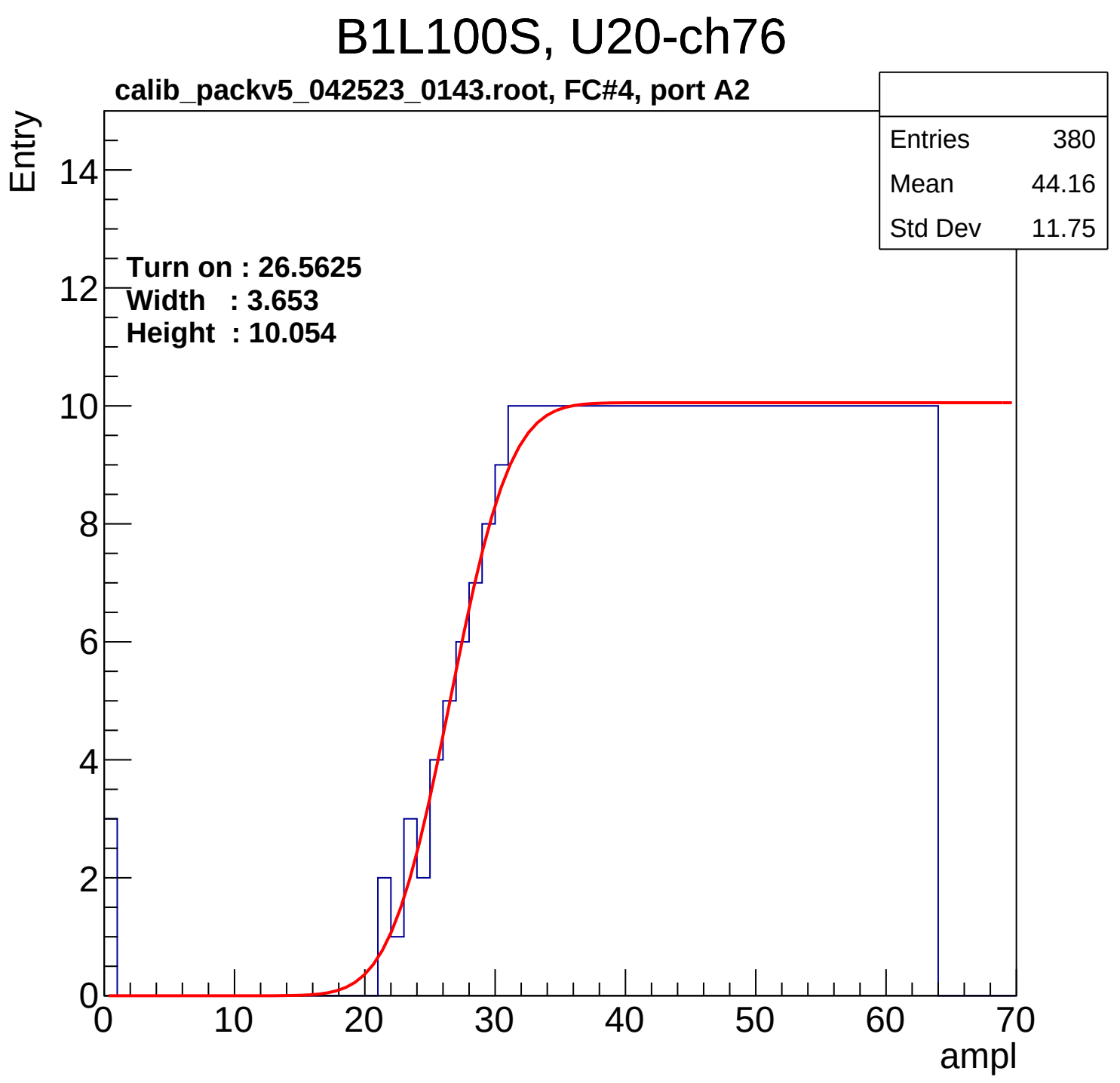
B1L100S, U20-ch76
calib_packv5_042523_0143.root, FC#4, port A2
Entries 380
Mean 44.16
Std Dev 11.75
Turn on : 26.5625
Width : 3.653
Height : 10.054
Entry
ampl
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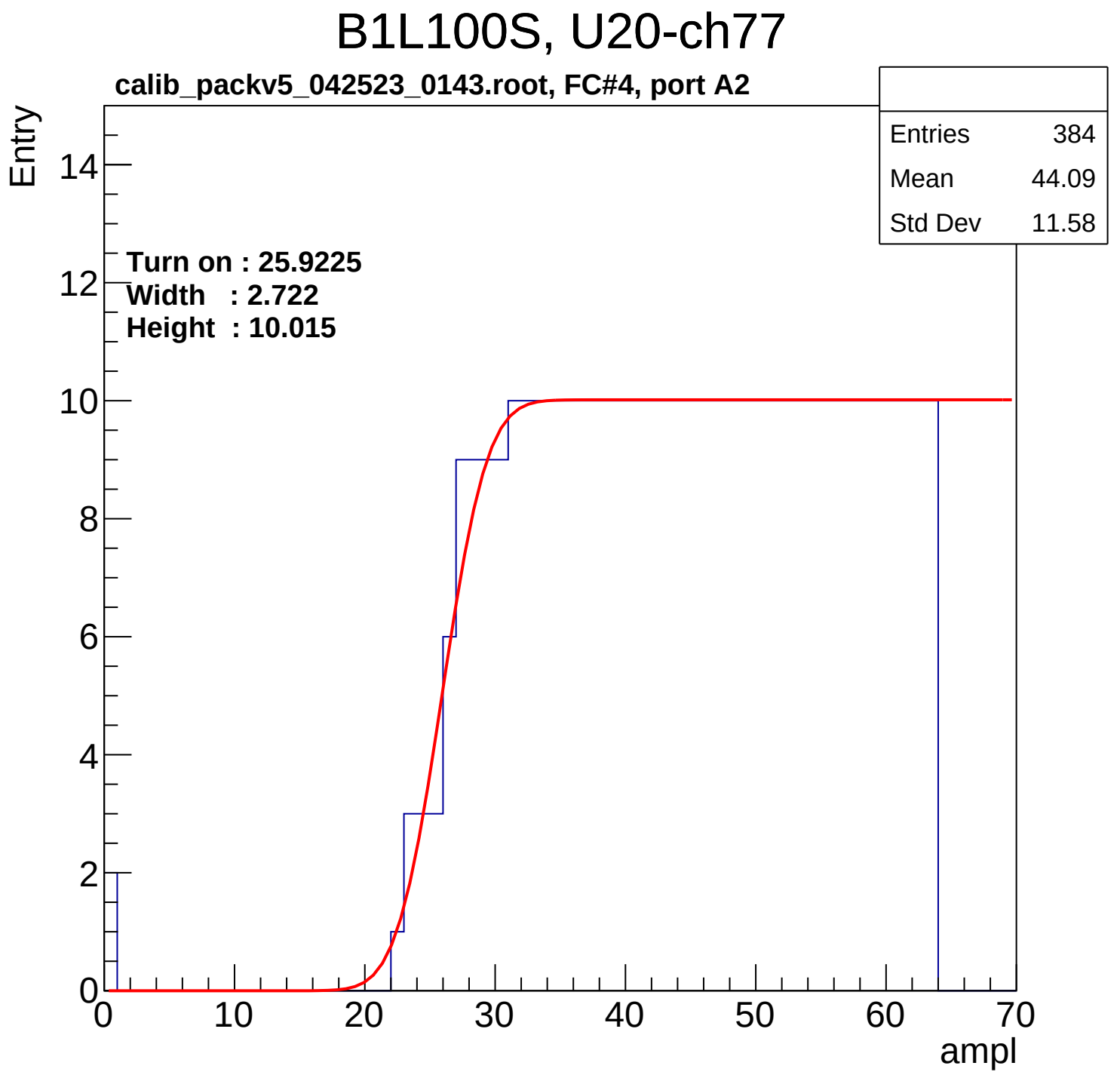
B1L100S, U20-ch77
calib_packv5_042523_0143.root, FC#4, port A2
Entries 384
Mean 44.09
Std Dev 11.58
Turn on : 25.9225
Width : 2.722
Height : 10.015
Entry
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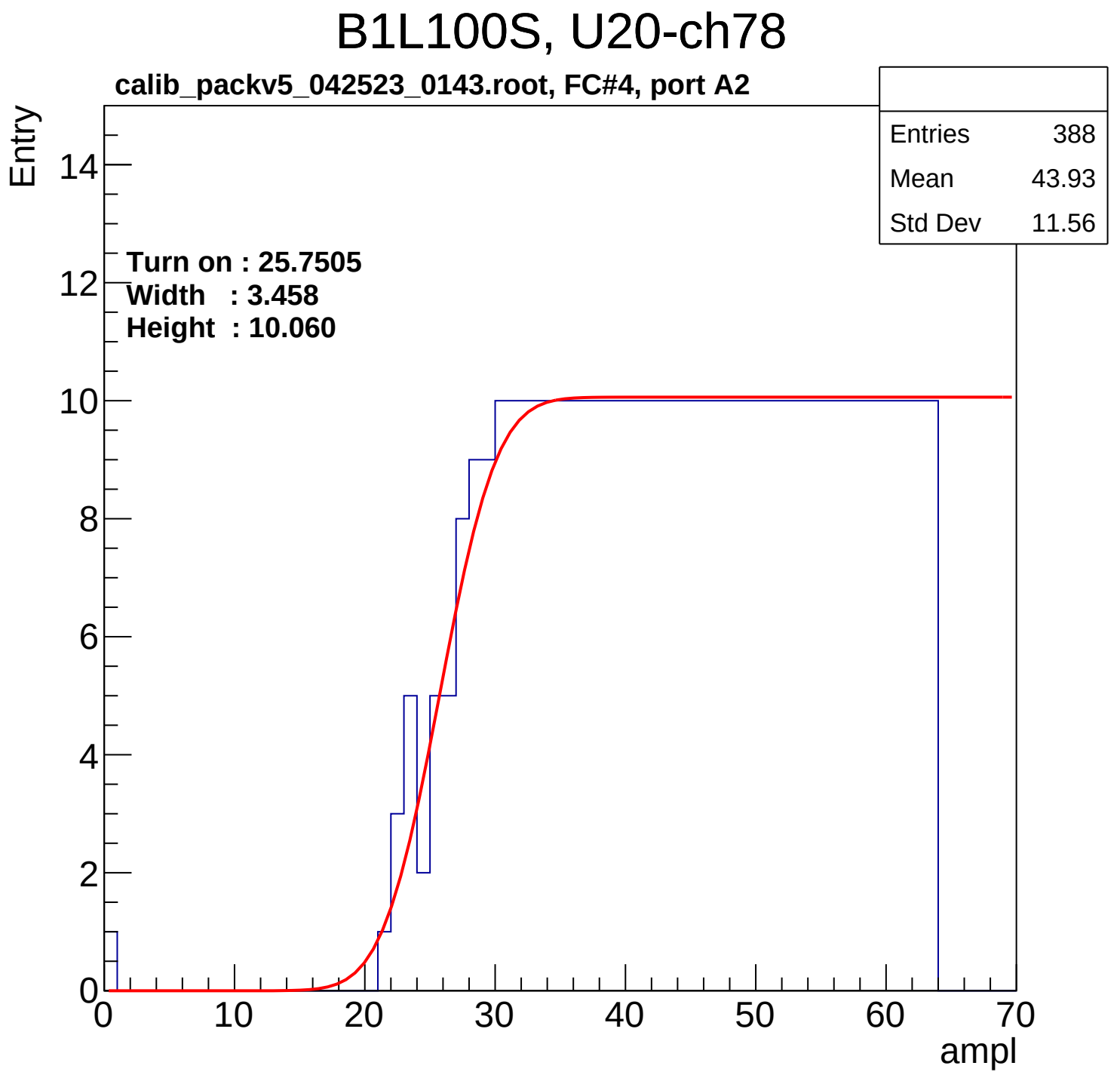
B1L100S, U20-ch78
calib_packv5_042523_0143.root, FC#4, port A2
Entries 388
Mean 43.93
Std Dev 11.56
Turn on : 25.7505
Width : 3.458
Height : 10.060
Entry
ampl
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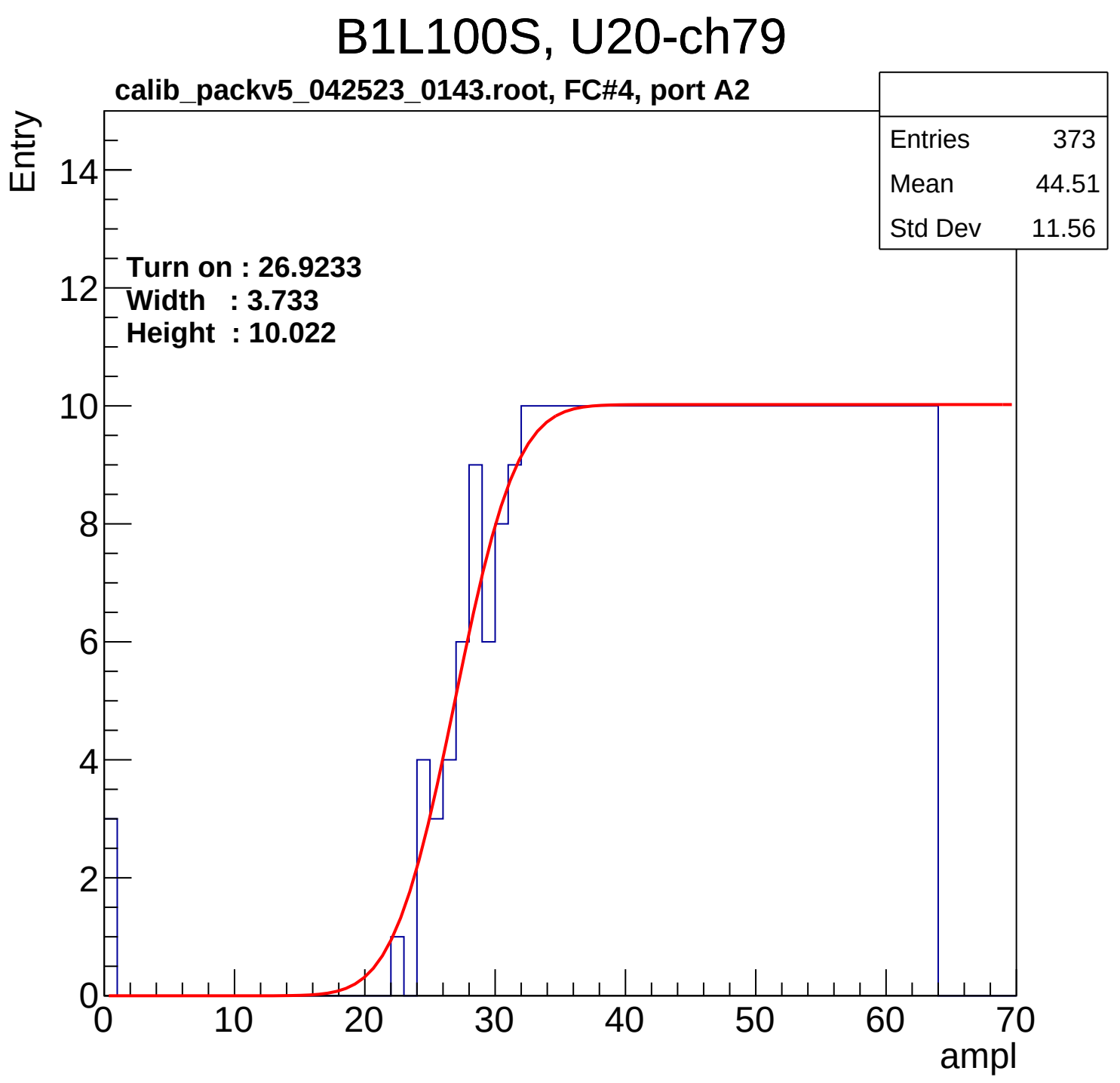
B1L100S, U20-ch79
calib_packv5_042523_0143.root, FC#4, port A2
Entries 373
Mean 44.51
Std Dev 11.56
Turn on : 26.9233
Width : 3.733
Height : 10.022
Entry
ampl
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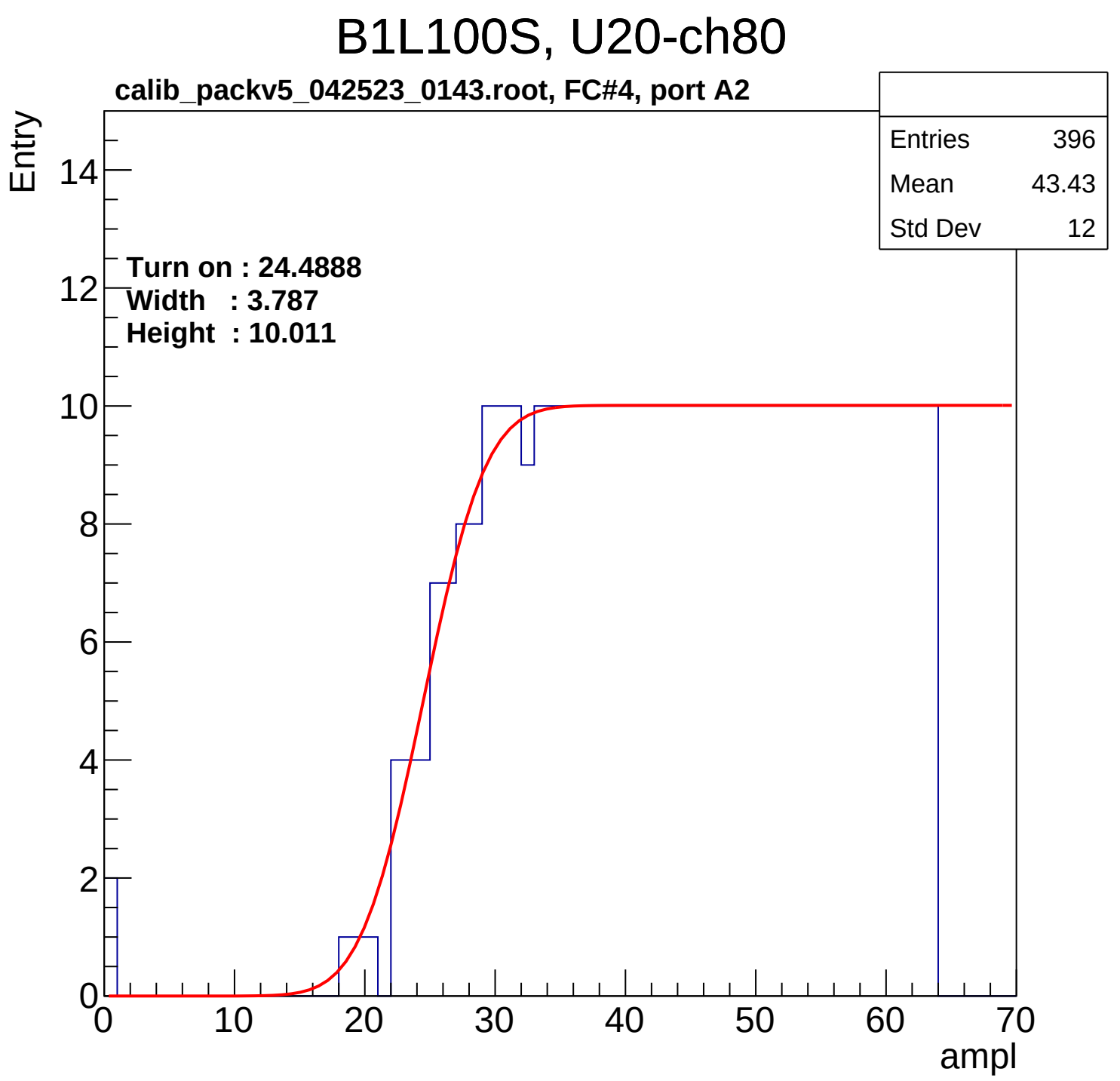
B1L100S, U20-ch80
calib_packv5_042523_0143.root, FC#4, port A2
Entries 396
Mean 43.43
Std Dev 12
Turn on : 24.4888
Width : 3.787
Height : 10.011
Entry
ampl
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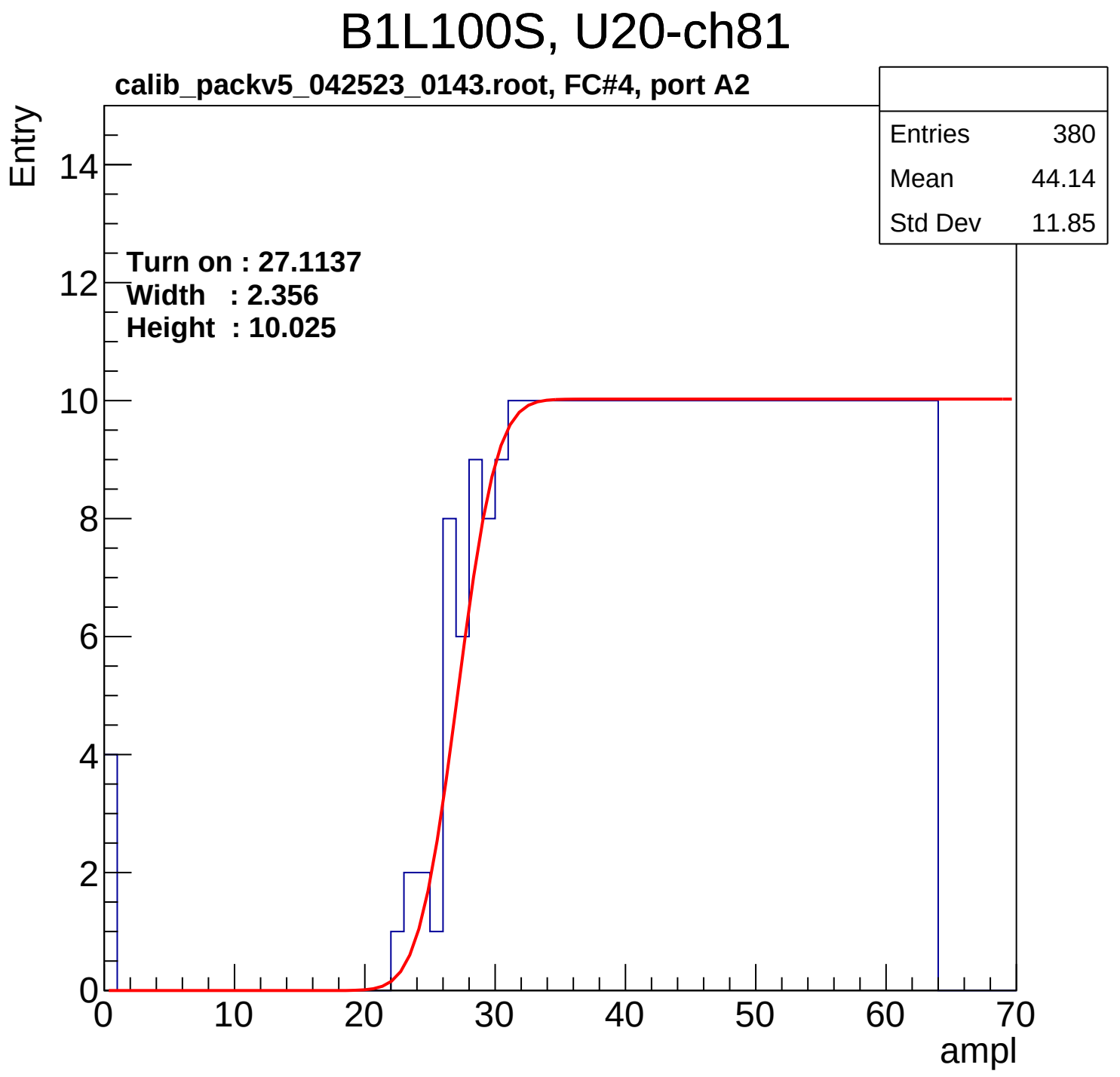
B1L100S, U20-ch81
calib_packv5_042523_0143.root, FC#4, port A2
Entries 380
Mean 44.14
Std Dev 11.85
Turn on : 27.1137
Width : 2.356
Height : 10.025
Entry
ampl
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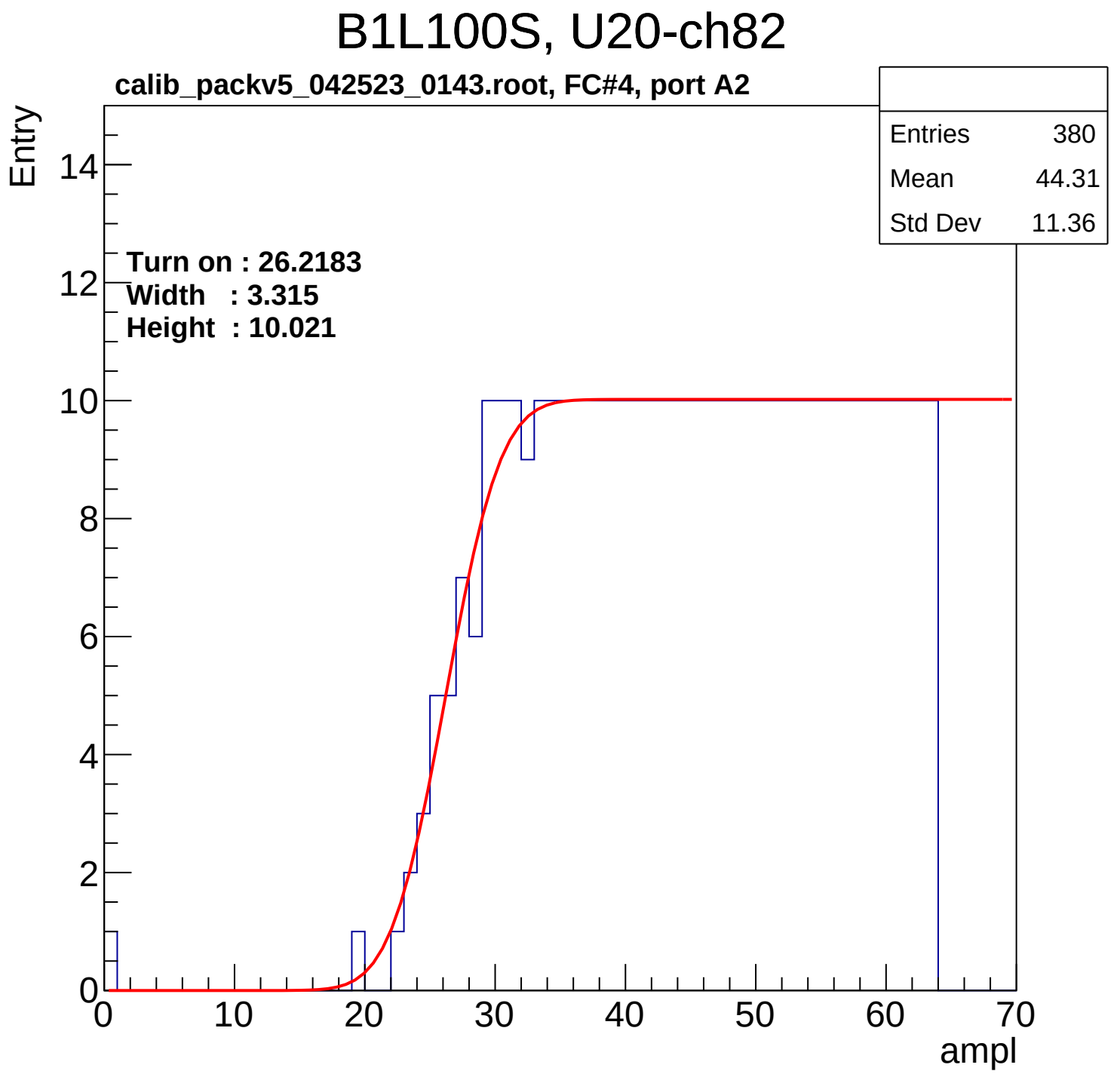
B1L100S, U20-ch82
calib_packv5_042523_0143.root, FC#4, port A2
Entries 380
Mean 44.31
Std Dev 11.36
Turn on : 26.2183
Width : 3.315
Height : 10.021
Entry
ampl
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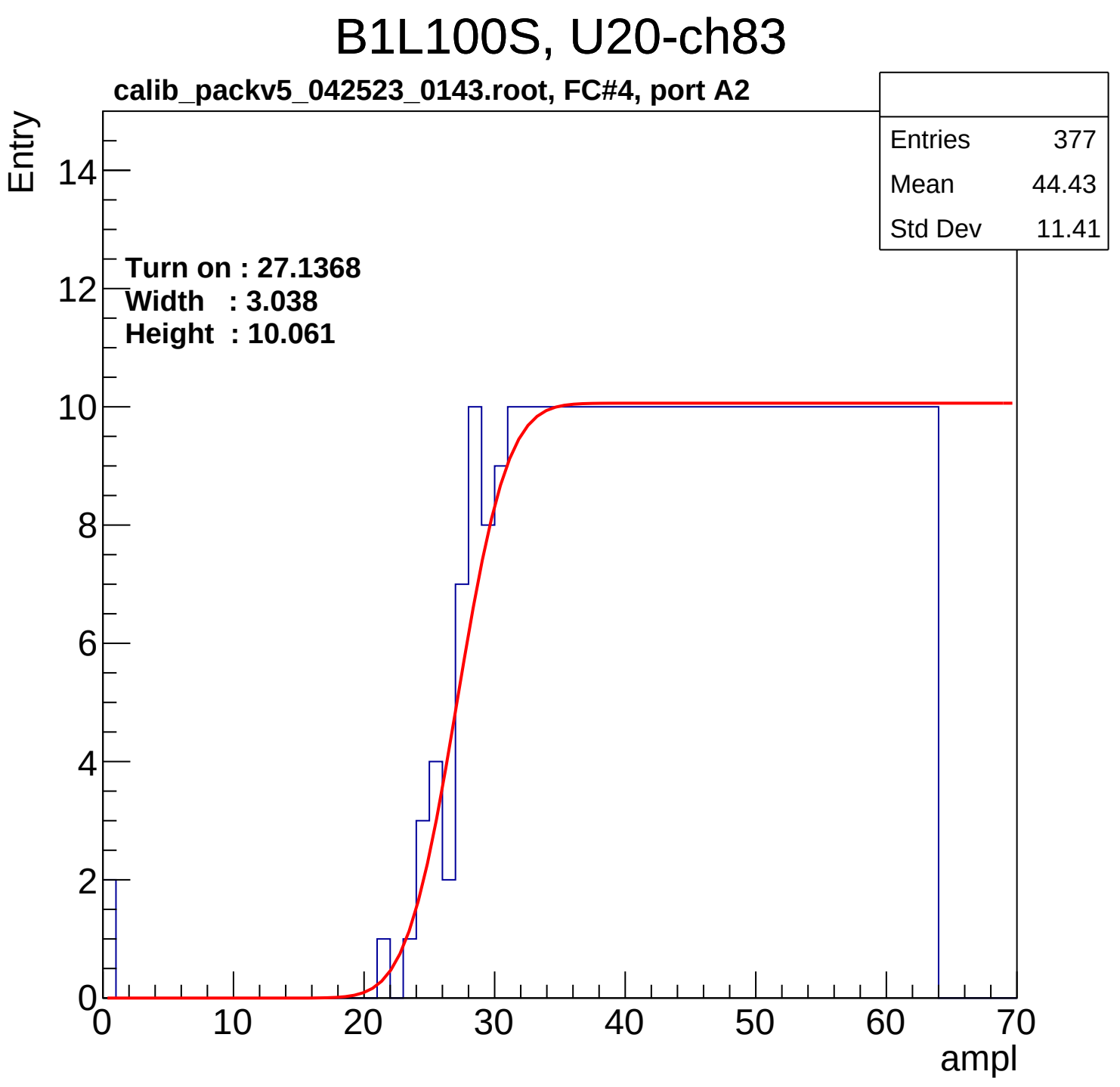
B1L100S, U20-ch83
calib_packv5_042523_0143.root, FC#4, port A2
Entries 377
Mean 44.43
Std Dev 11.41
Turn on : 27.1368
Width : 3.038
Height : 10.061
Entry
ampl
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6
8
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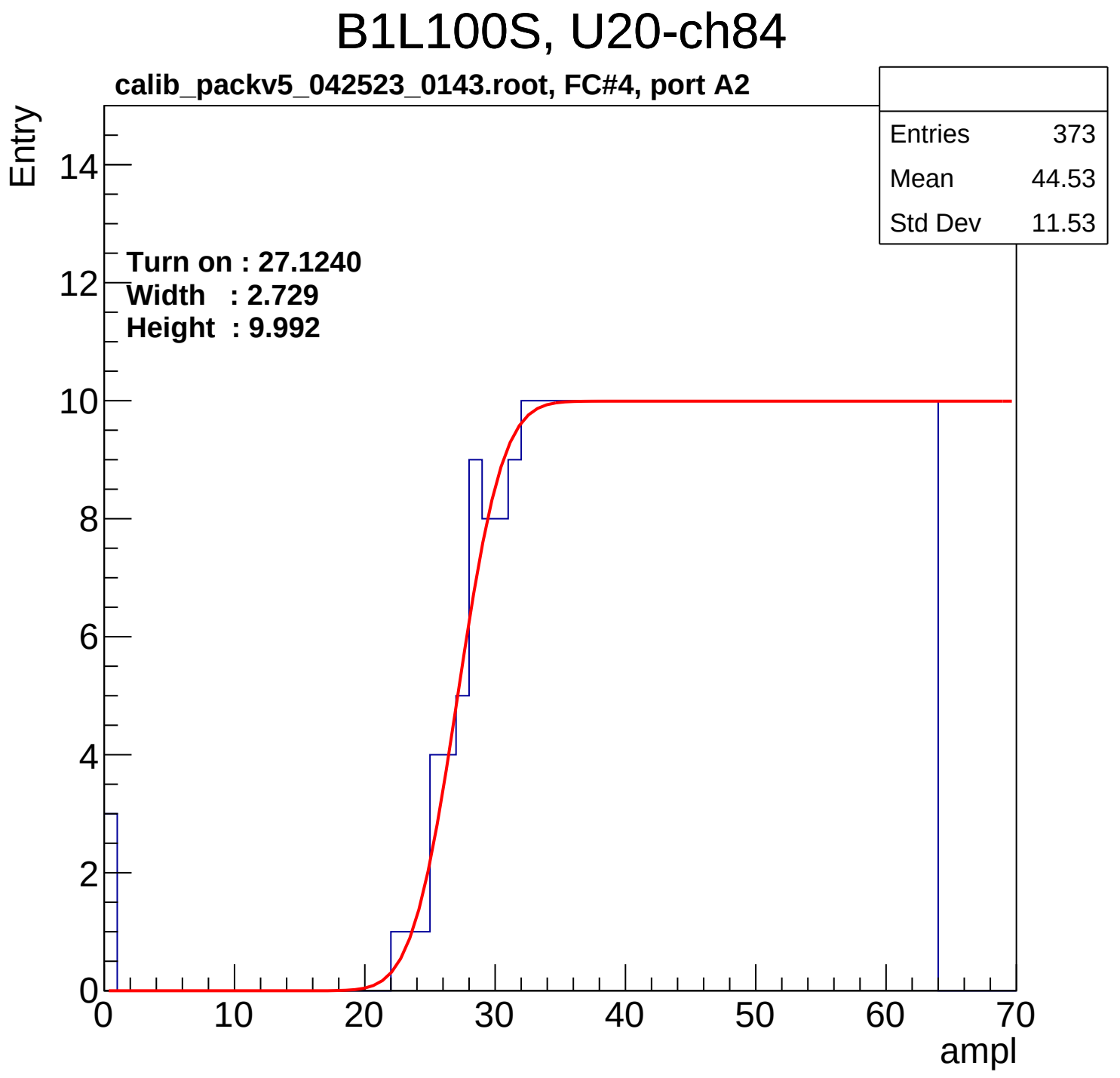
B1L100S, U20-ch84
calib_packv5_042523_0143.root, FC#4, port A2
Entries 373
Mean 44.53
Std Dev 11.53
Turn on : 27.1240
Width : 2.729
Height : 9.992
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ampl
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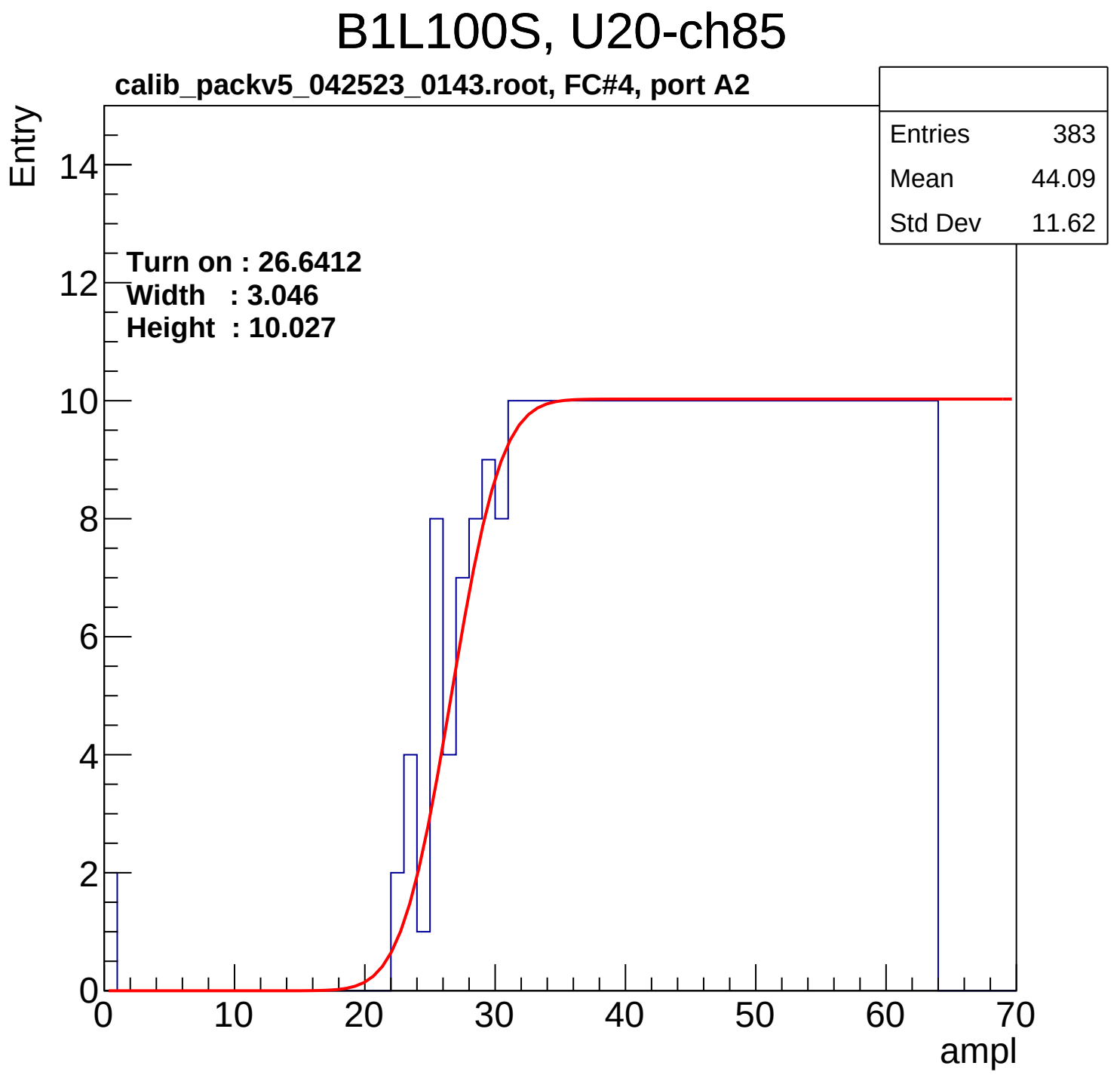
B1L100S, U20-ch85
calib_packv5_042523_0143.root, FC#4, port A2
Entries 383
Mean 44.09
Std Dev 11.62
Turn on : 26.6412
Width : 3.046
Height : 10.027
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ampl
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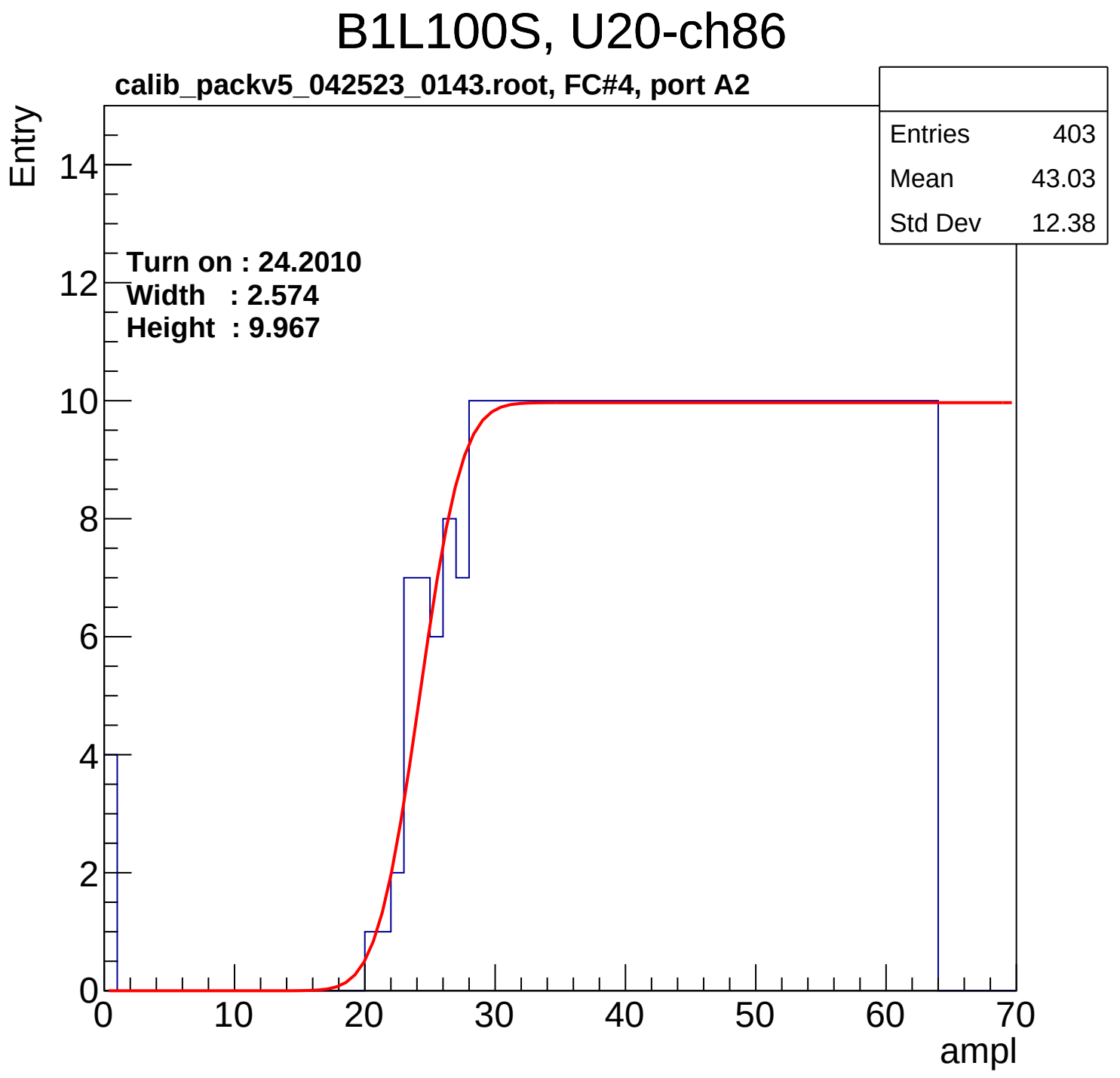
B1L100S, U20-ch86
calib_packv5_042523_0143.root, FC#4, port A2
Entries 403
Mean 43.03
Std Dev 12.38
Turn on : 24.2010
Width : 2.574
Height : 9.967
Entry
ampl
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4
6
8
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10
20
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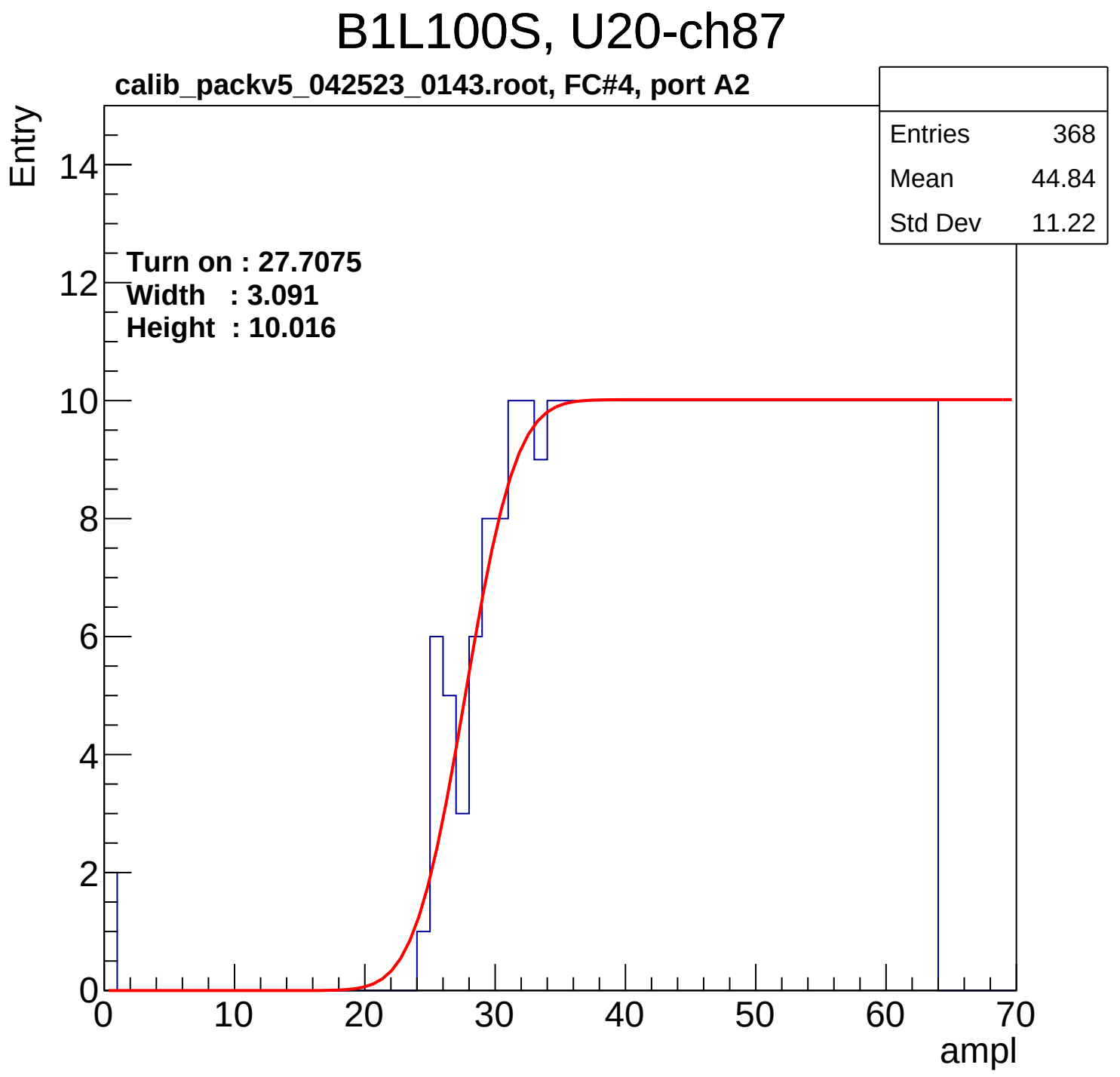
B1L100S, U20-ch87
calib_packv5_042523_0143.root, FC#4, port A2
Entries 368
Mean 44.84
Std Dev 11.22
Turn on : 27.7075
Width : 3.091
Height : 10.016
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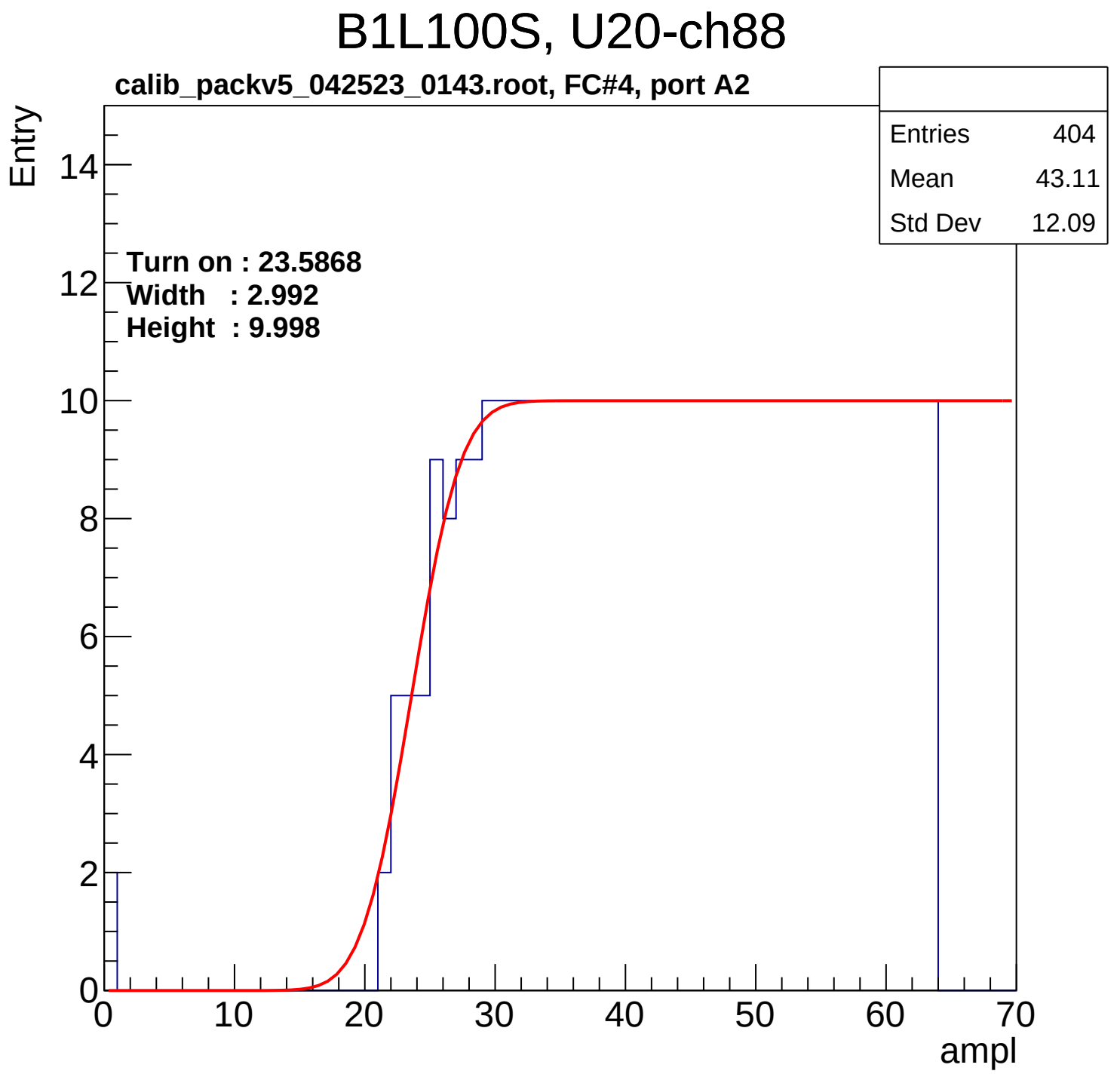
B1L100S, U20-ch88
calib_packv5_042523_0143.root, FC#4, port A2
Entries 404
Mean 43.11
Std Dev 12.09
Turn on : 23.5868
Width : 2.992
Height : 9.998
Entry
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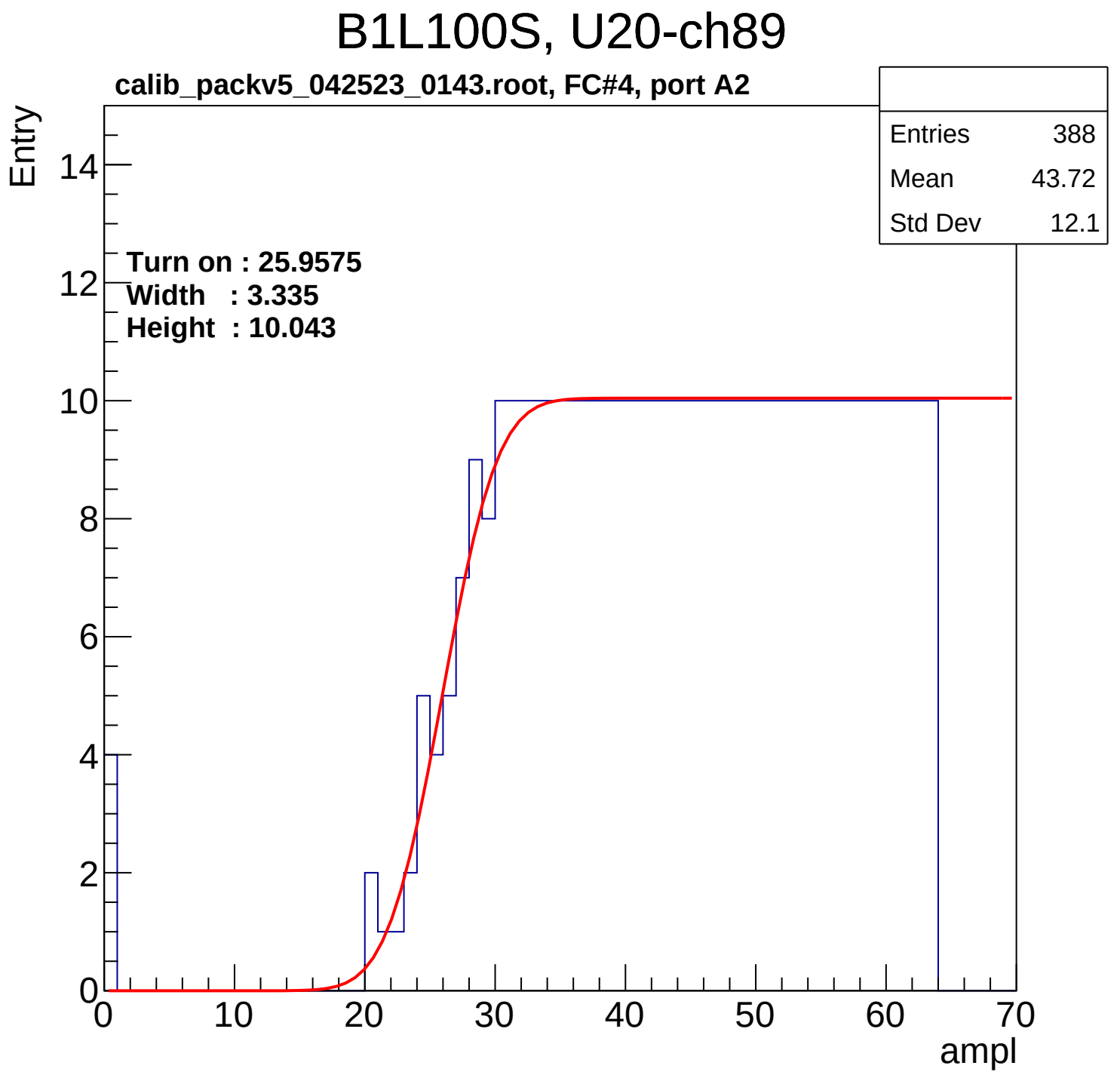
B1L100S, U20-ch89
calib_packv5_042523_0143.root, FC#4, port A2
Entries 388
Mean 43.72
Std Dev 12.1
Turn on : 25.9575
Width : 3.335
Height : 10.043
Entry
ampl
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8
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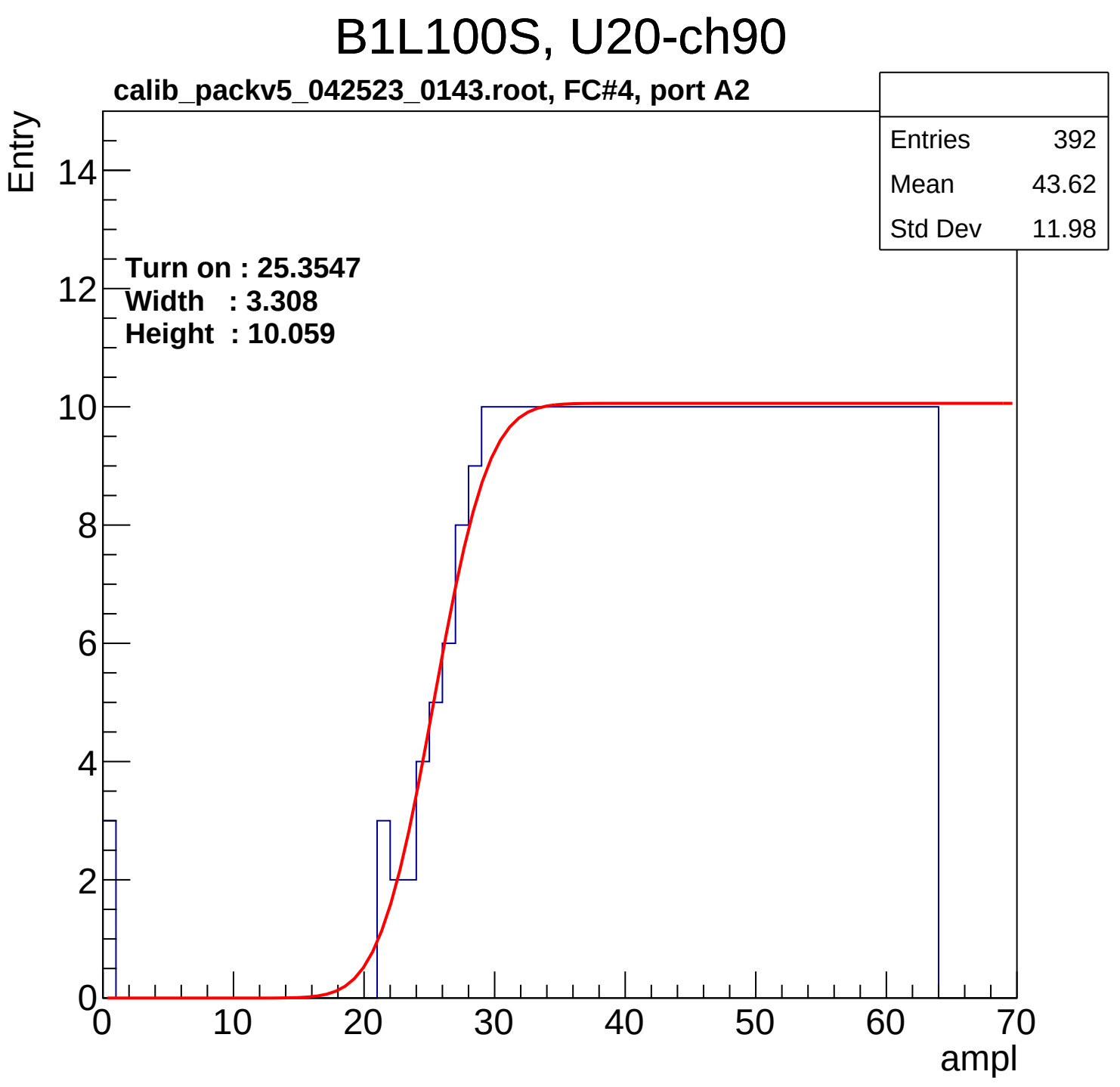
B1L100S, U20-ch90
calib_packv5_042523_0143.root, FC#4, port A2
Entries 392
Mean 43.62
Std Dev 11.98
Turn on : 25.3547
Width : 3.308
Height : 10.059
Entry
ampl
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4
6
8
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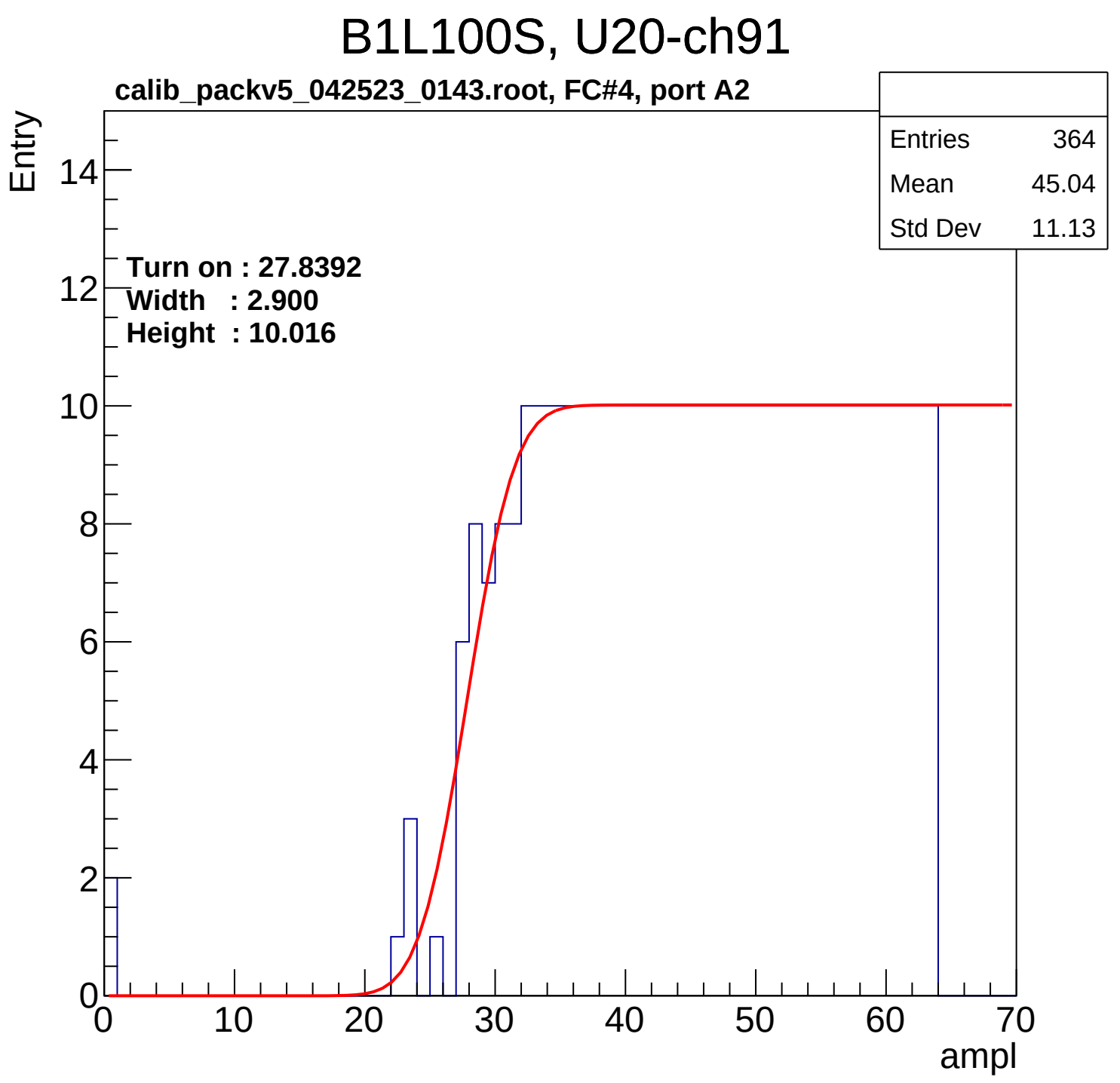
B1L100S, U20-ch91
calib_packv5_042523_0143.root, FC#4, port A2
Entries 364
Mean 45.04
Std Dev 11.13
Turn on : 27.8392
Width : 2.900
Height : 10.016
Entry
ampl
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2
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6
8
10
12
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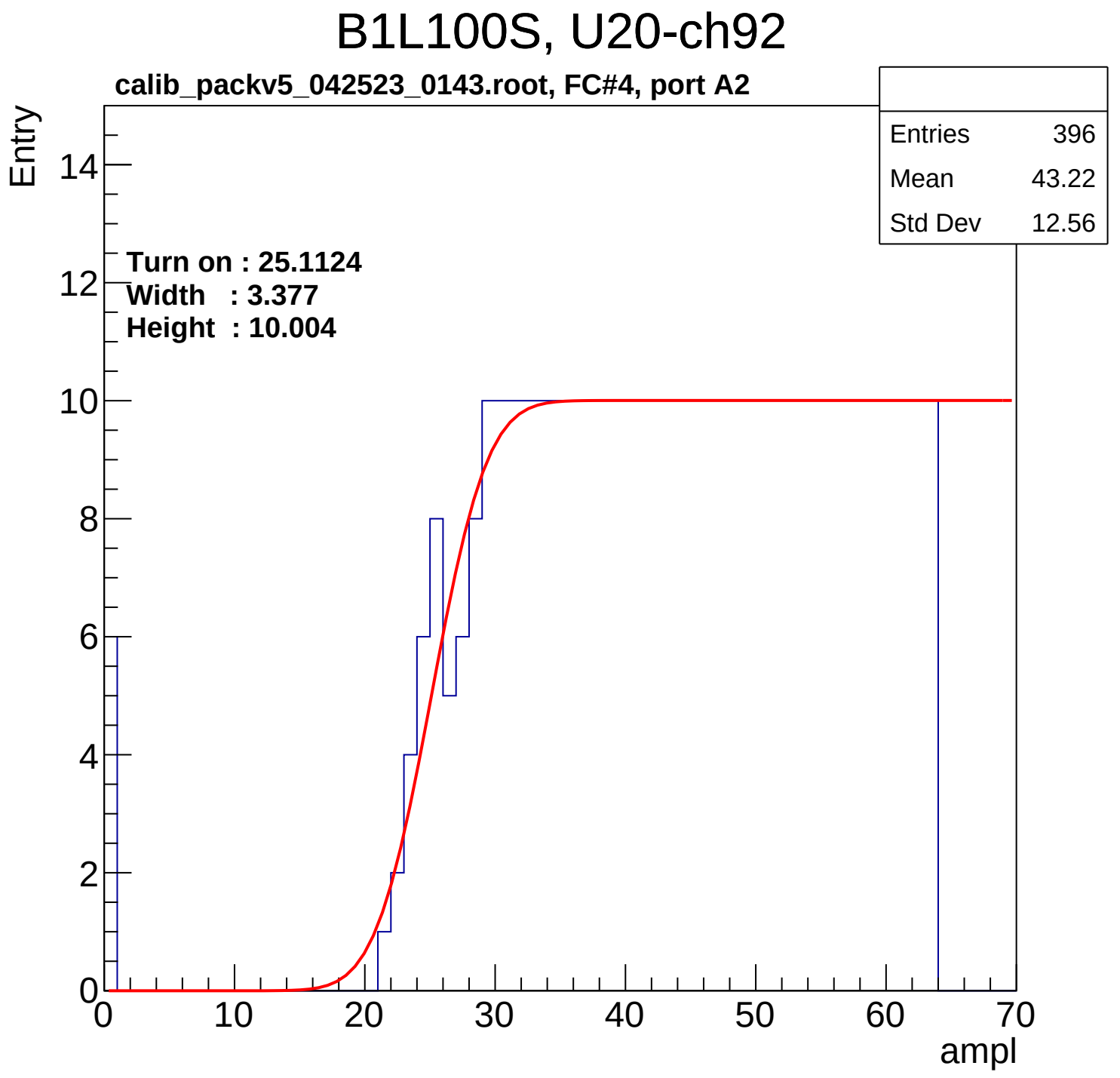
B1L100S, U20-ch92
calib_packv5_042523_0143.root, FC#4, port A2
Entries 396
Mean 43.22
Std Dev 12.56
Turn on : 25.1124
Width : 3.377
Height : 10.004
Entry
ampl
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4
6
8
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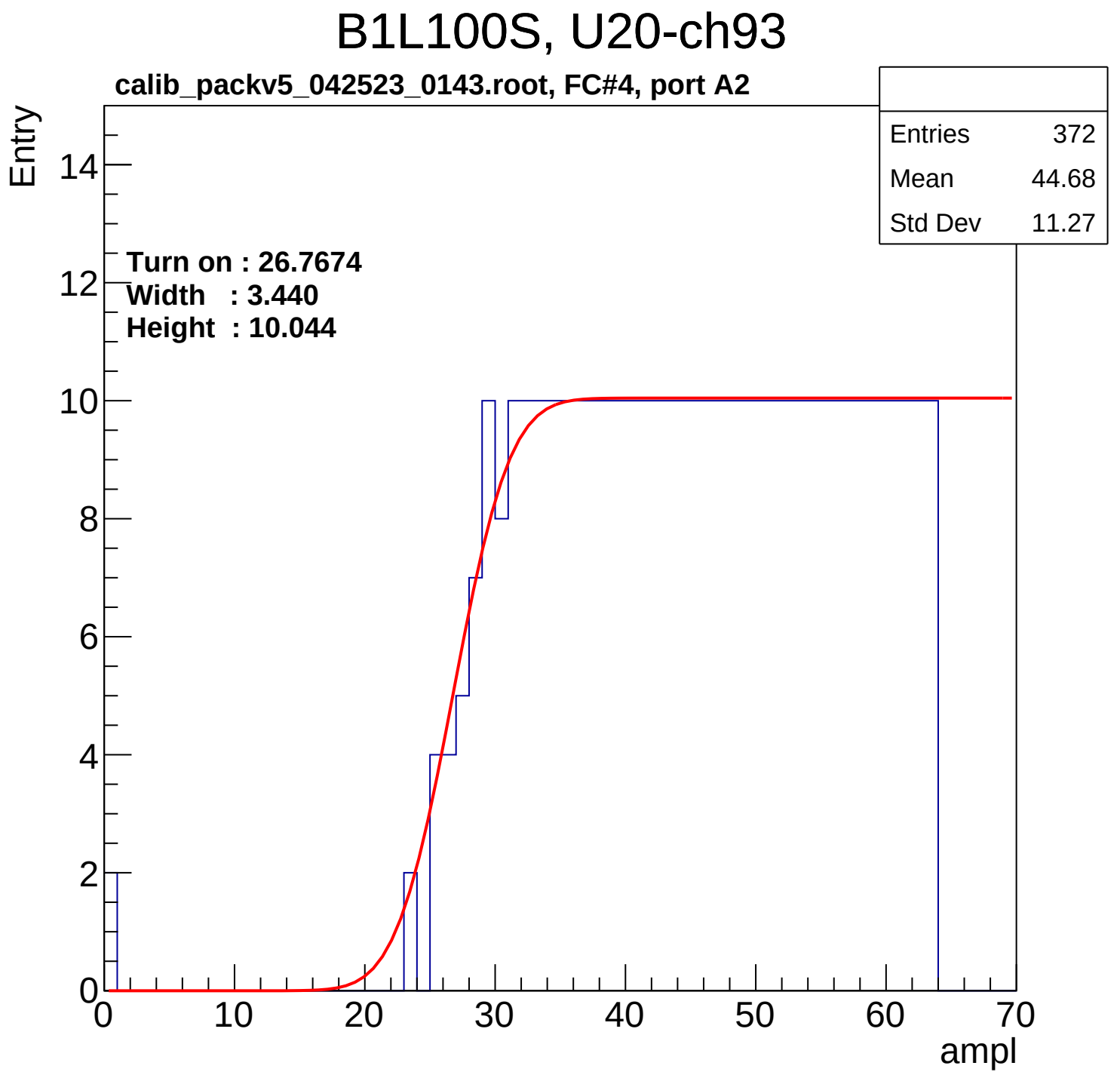
B1L100S, U20-ch93
calib_packv5_042523_0143.root, FC#4, port A2
Entries 372
Mean 44.68
Std Dev 11.27
Turn on : 26.7674
Width : 3.440
Height : 10.044
Entry
ampl
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6
8
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12
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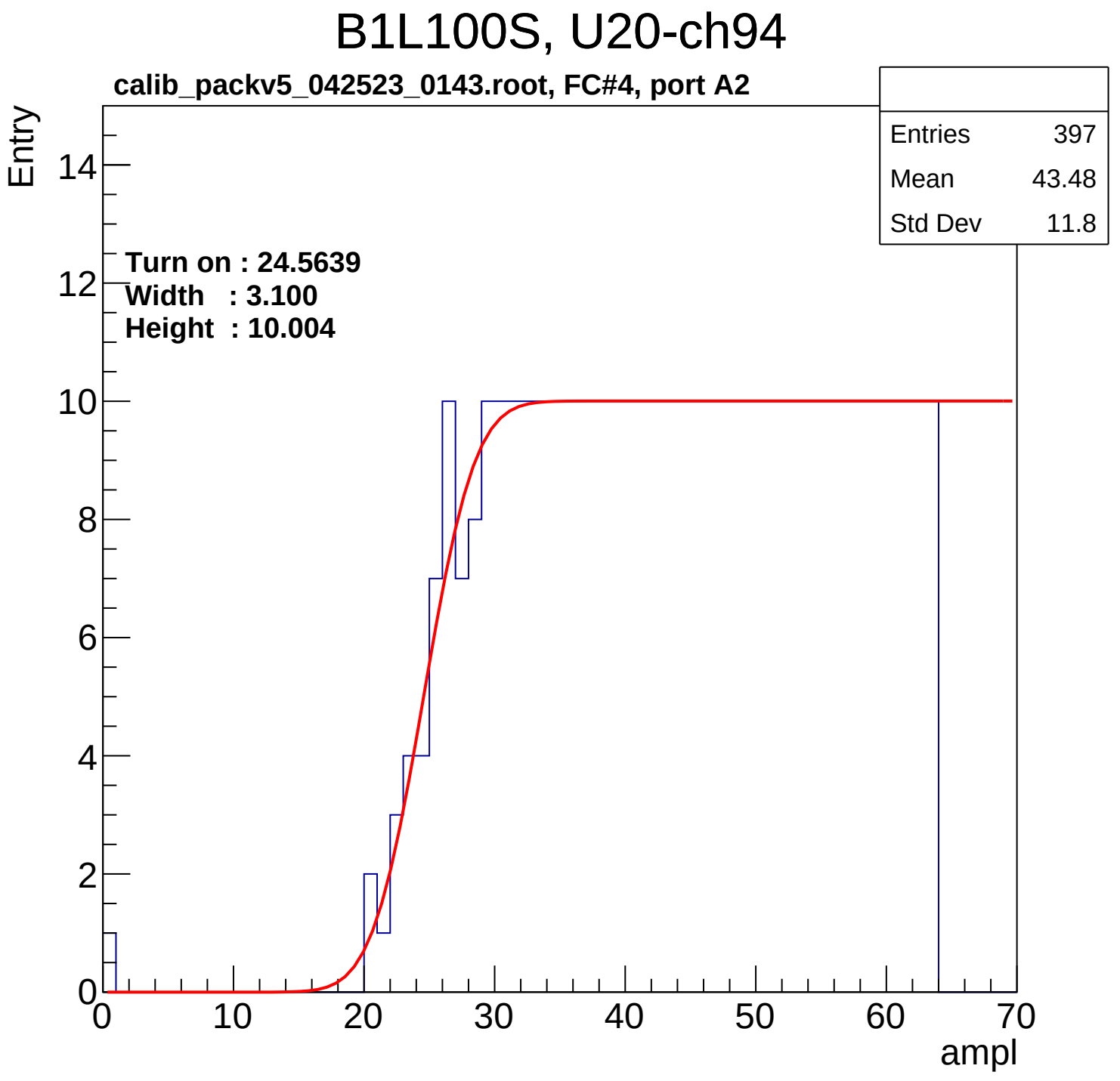
B1L100S, U20-ch94
calib_packv5_042523_0143.root, FC#4, port A2
Entries 397
Mean 43.48
Std Dev 11.8
Turn on : 24.5639
Width : 3.100
Height : 10.004
Entry
ampl
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2
4
6
8
10
12
14
0
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60
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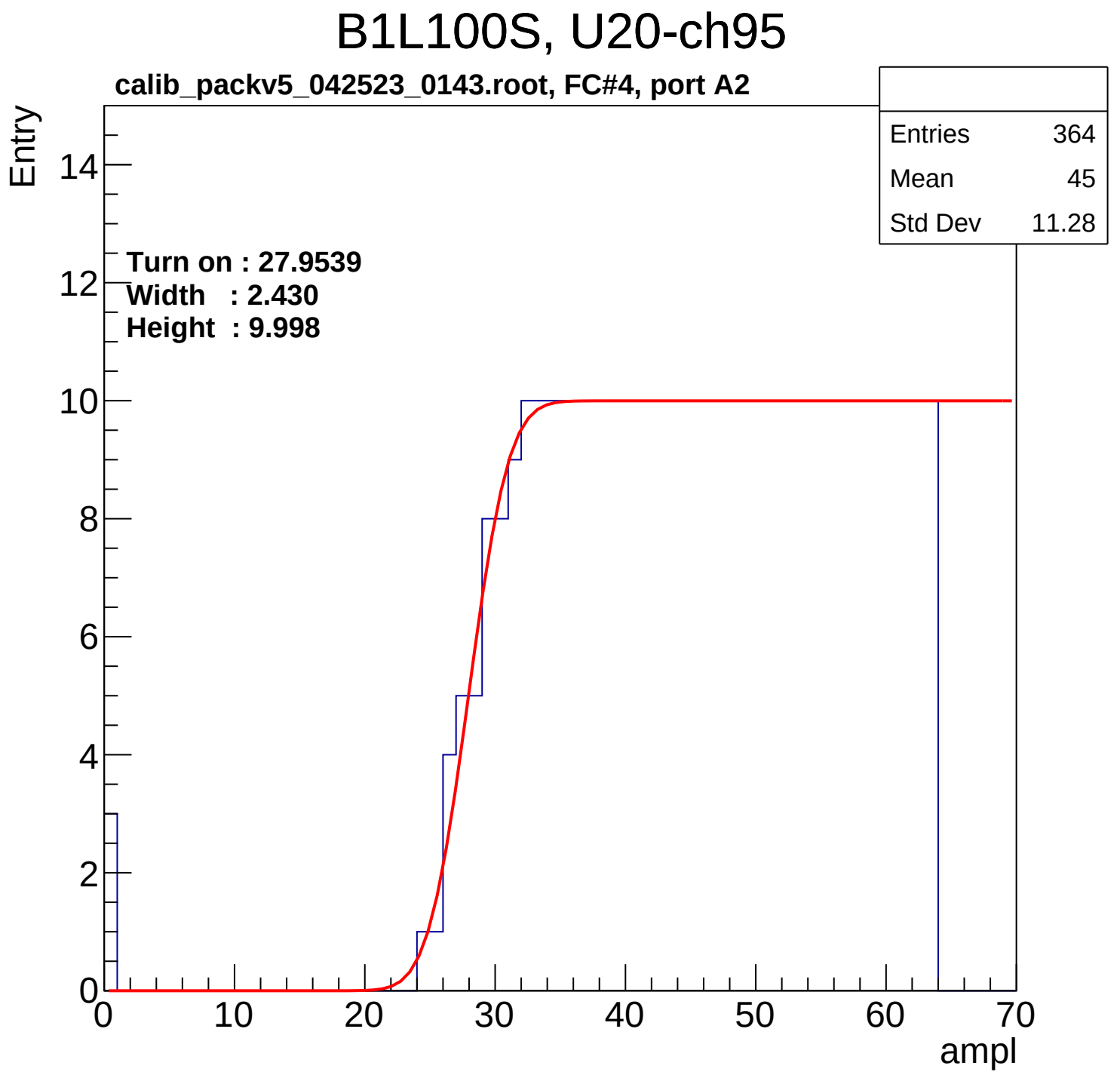
B1L100S, U20-ch95
calib_packv5_042523_0143.root, FC#4, port A2
Entries 364
Mean 45
Std Dev 11.28
Turn on : 27.9539
Width : 2.430
Height : 9.998
Entry
ampl
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2
4
6
8
10
12
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0
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60
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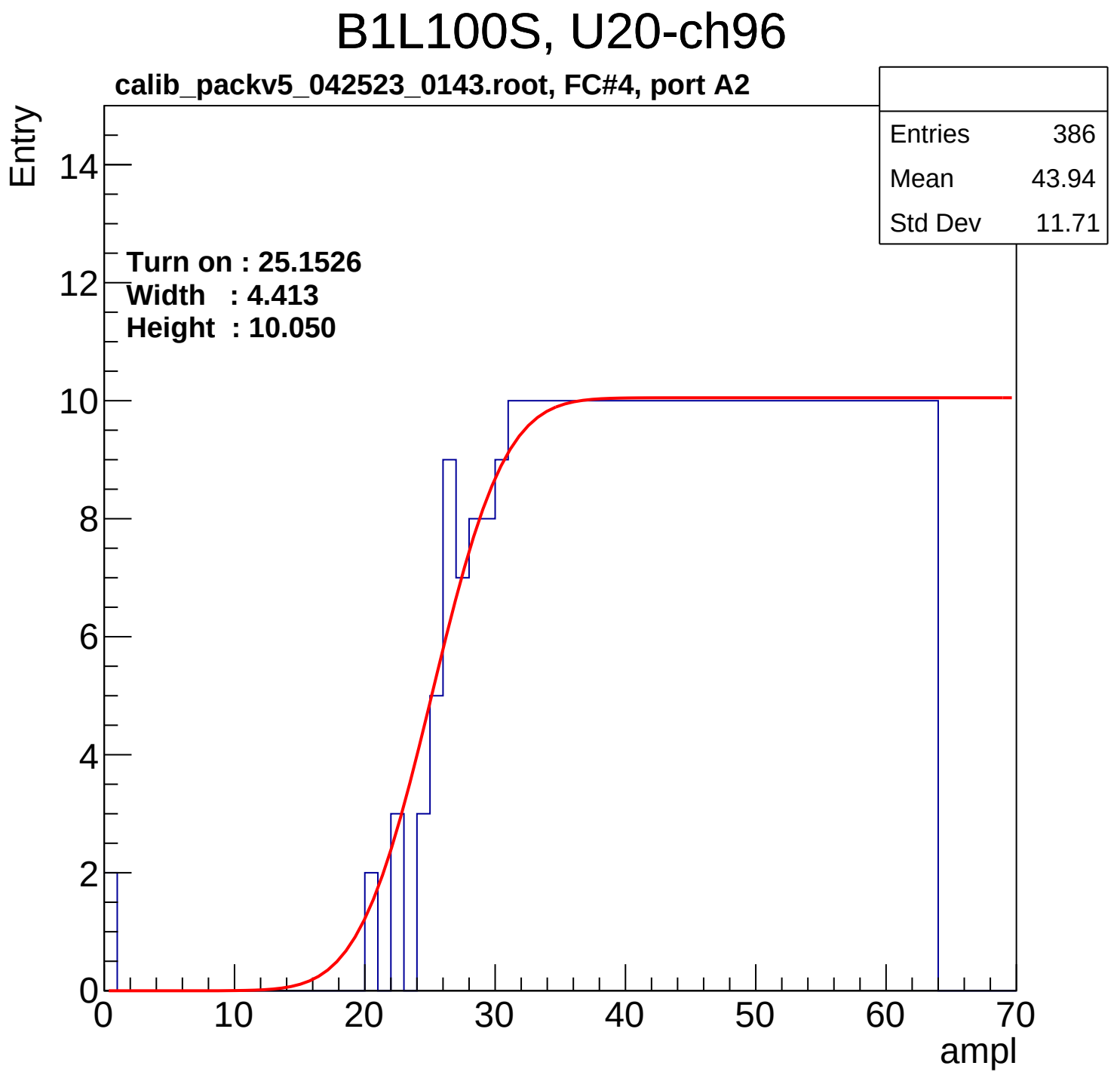
B1L100S, U20-ch96
calib_packv5_042523_0143.root, FC#4, port A2
Entries 386
Mean 43.94
Std Dev 11.71
Turn on : 25.1526
Width : 4.413
Height : 10.050
Entry
ampl
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2
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6
8
10
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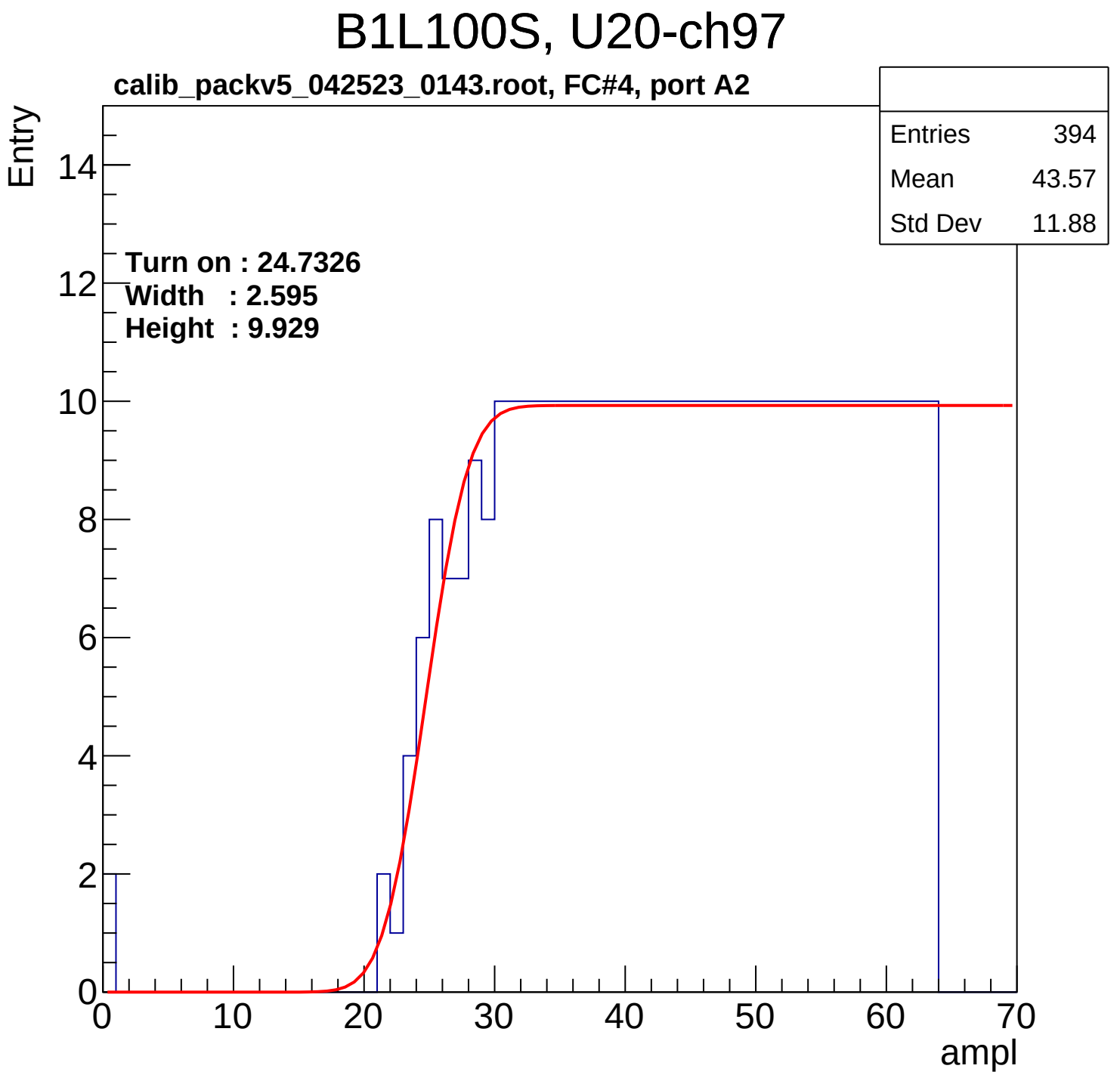
B1L100S, U20-ch97
calib_packv5_042523_0143.root, FC#4, port A2
Entries 394
Mean 43.57
Std Dev 11.88
Turn on : 24.7326
Width : 2.595
Height : 9.929
Entry
ampl
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6
8
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0
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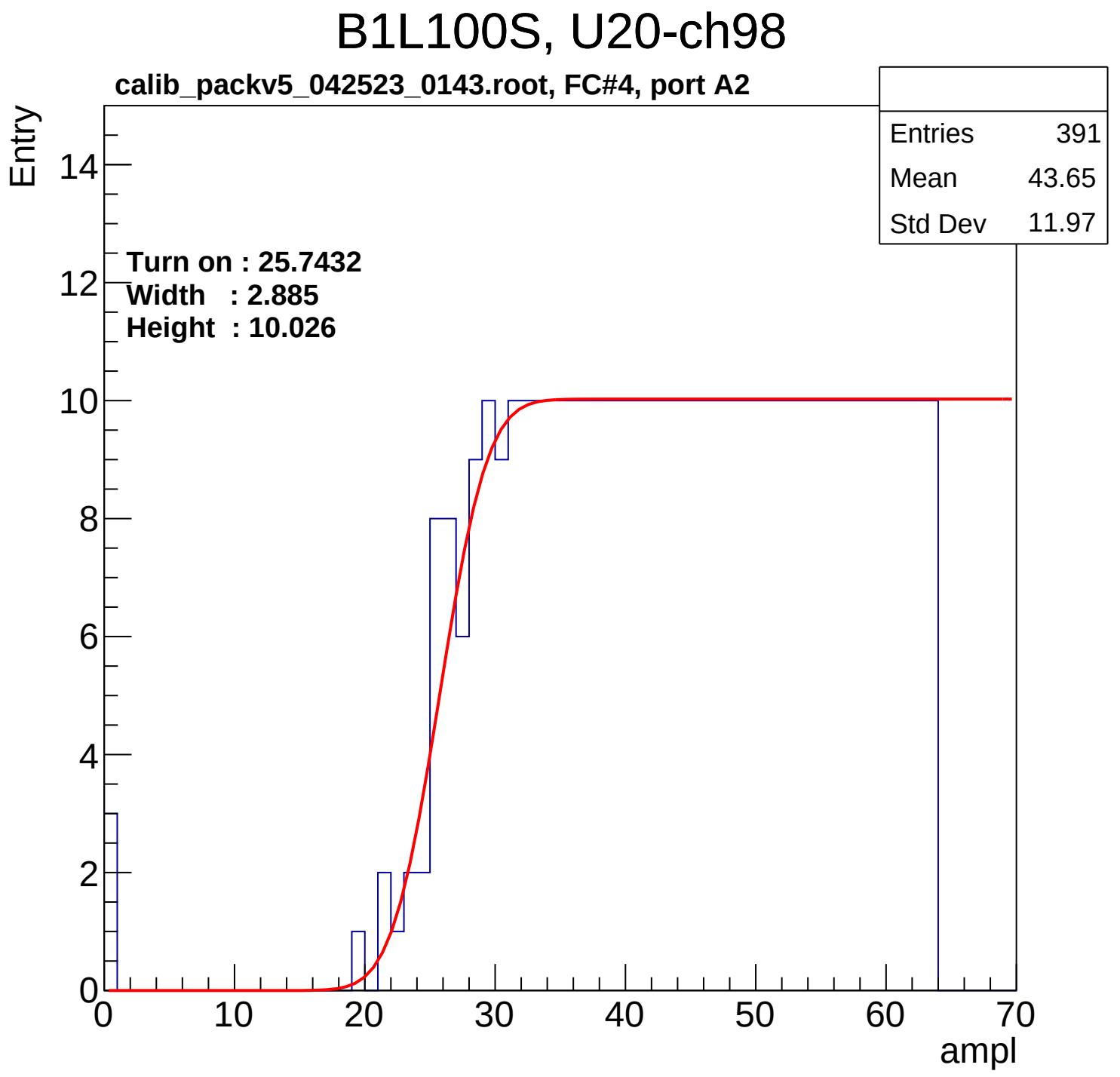
B1L100S, U20-ch98
calib_packv5_042523_0143.root, FC#4, port A2
Entries 391
Mean 43.65
Std Dev 11.97
Turn on : 25.7432
Width : 2.885
Height : 10.026
Entry
ampl
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2
4
6
8
10
12
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0
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20
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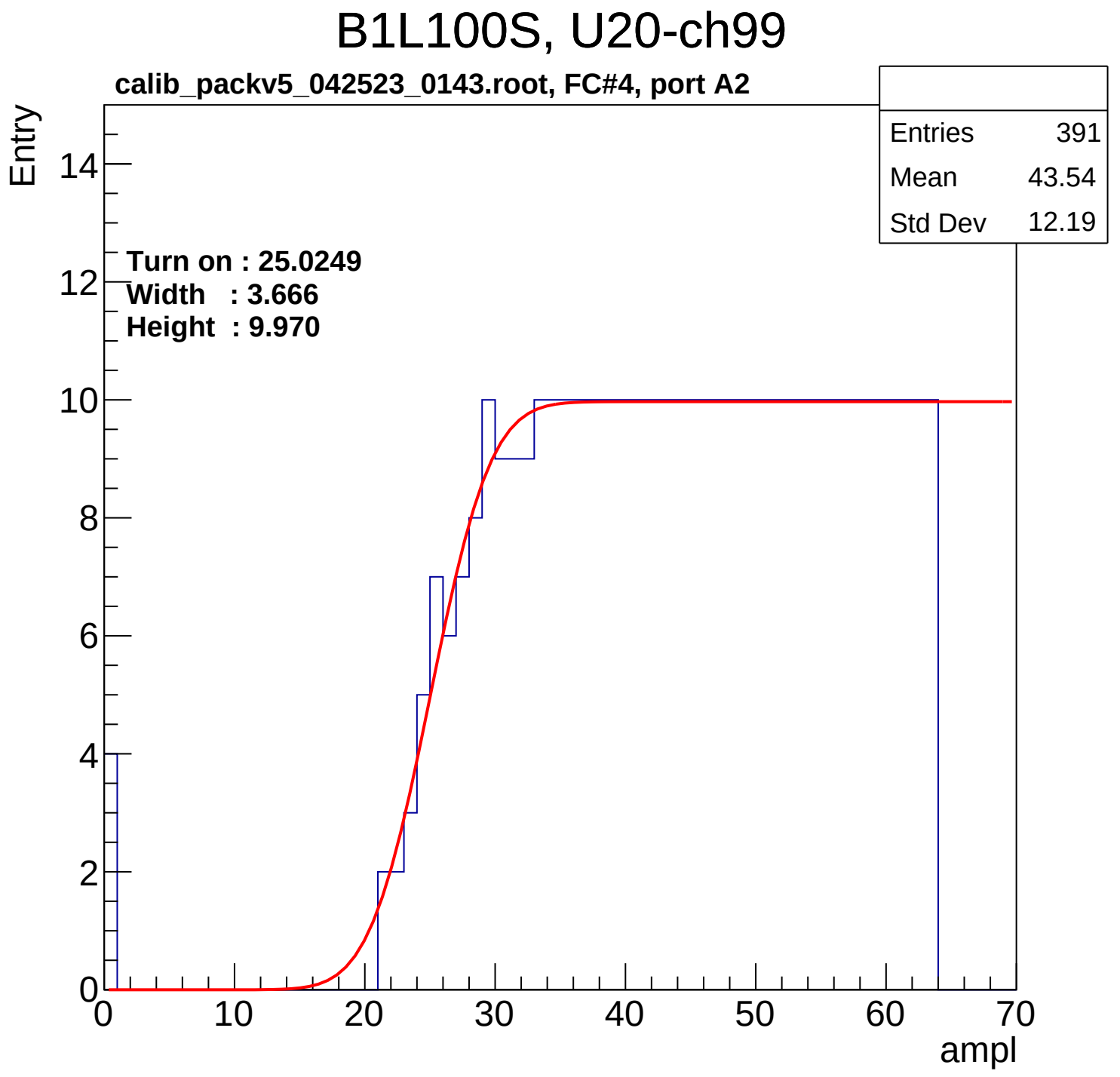
B1L100S, U20-ch99
calib_packv5_042523_0143.root, FC#4, port A2
Entries 391
Mean 43.54
Std Dev 12.19
Turn on : 25.0249
Width : 3.666
Height : 9.970
Entry
ampl
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2
4
6
8
10
12
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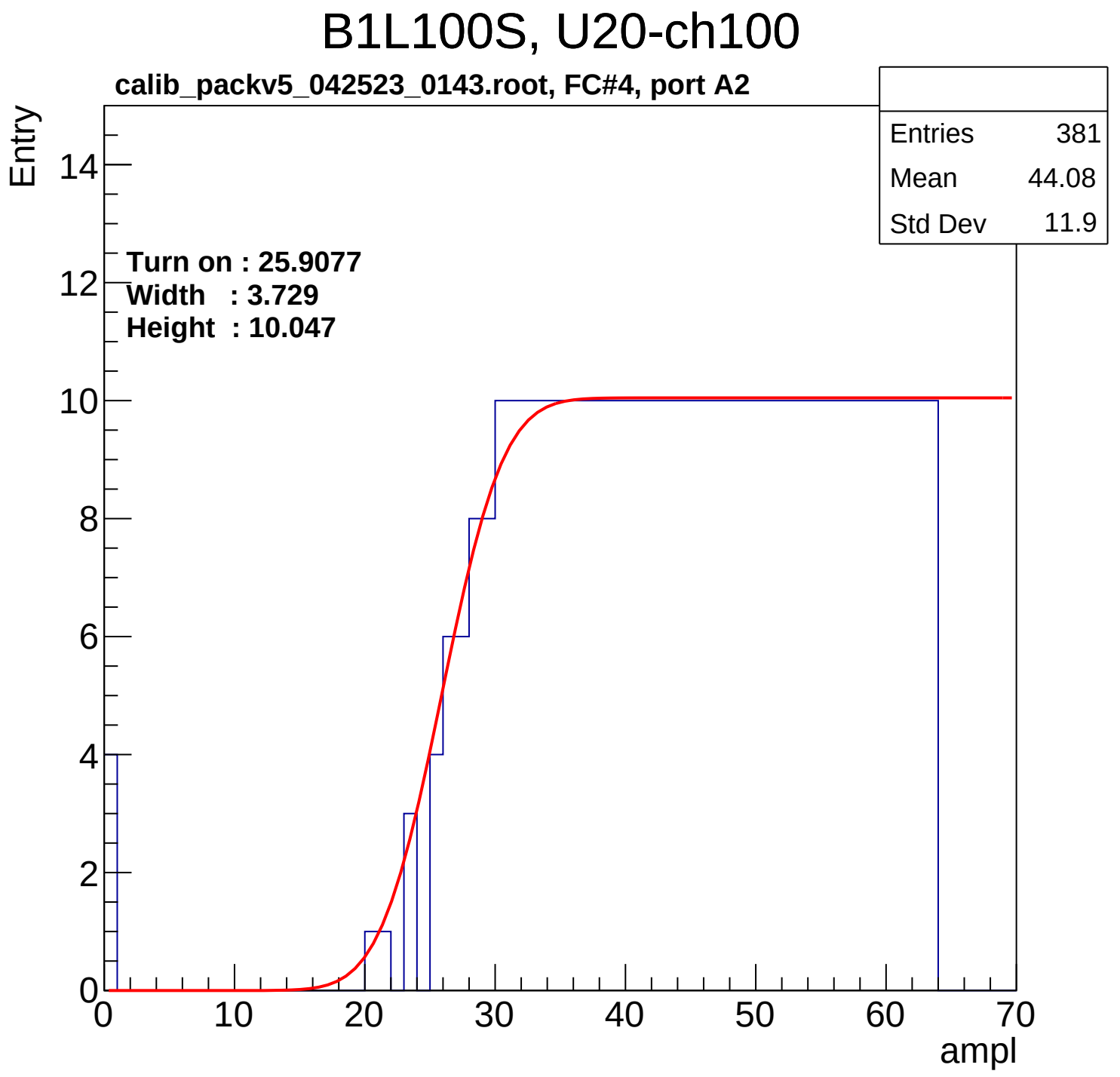
B1L100S, U20-ch100
calib_packv5_042523_0143.root, FC#4, port A2
Entries 381
Mean 44.08
Std Dev 11.9
Turn on : 25.9077
Width : 3.729
Height : 10.047
Entry
ampl
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8
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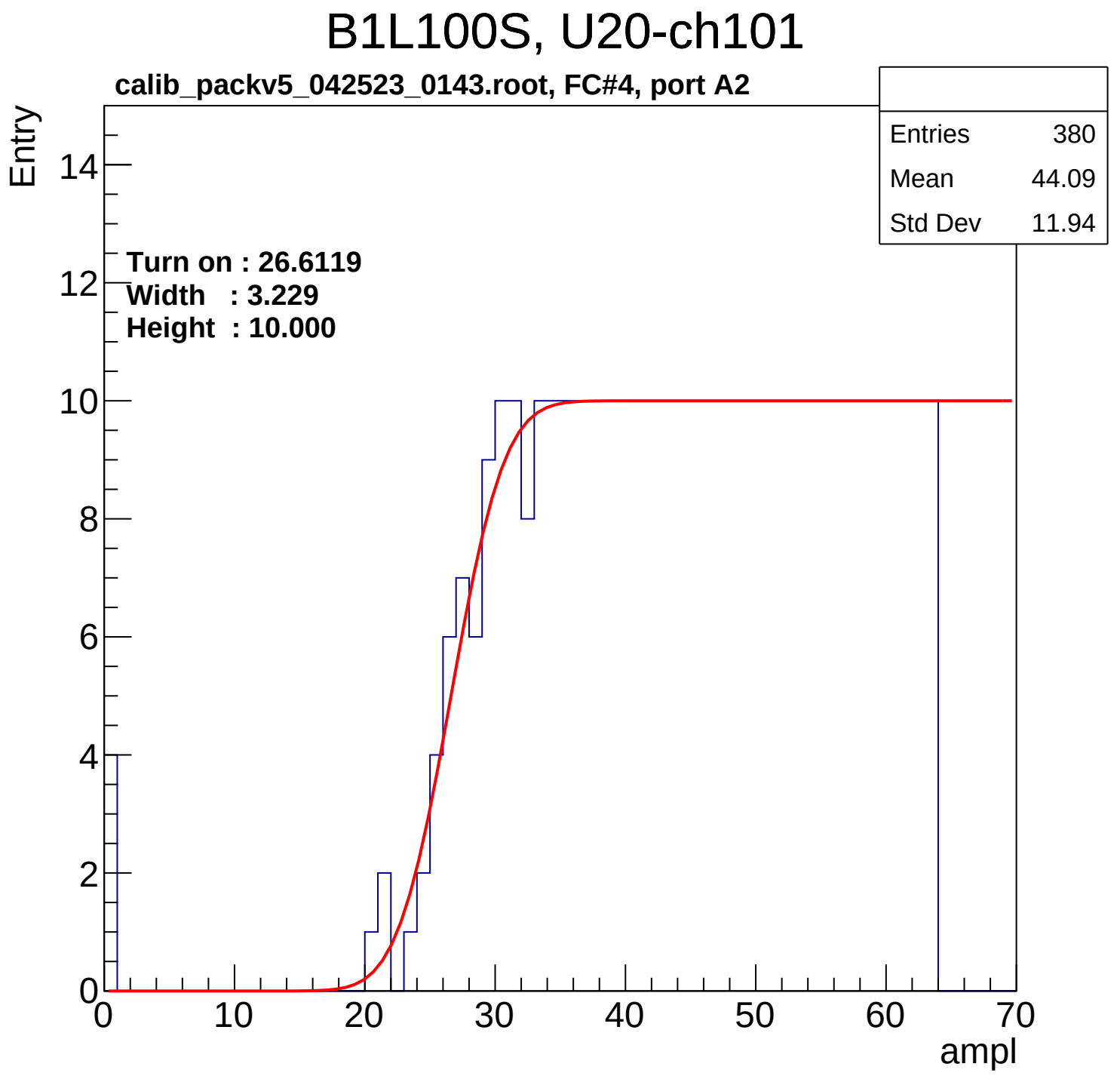
B1L100S, U20-ch101
calib_packv5_042523_0143.root, FC#4, port A2
Entries 380
Mean 44.09
Std Dev 11.94
Turn on : 26.6119
Width : 3.229
Height : 10.000
Entry
ampl
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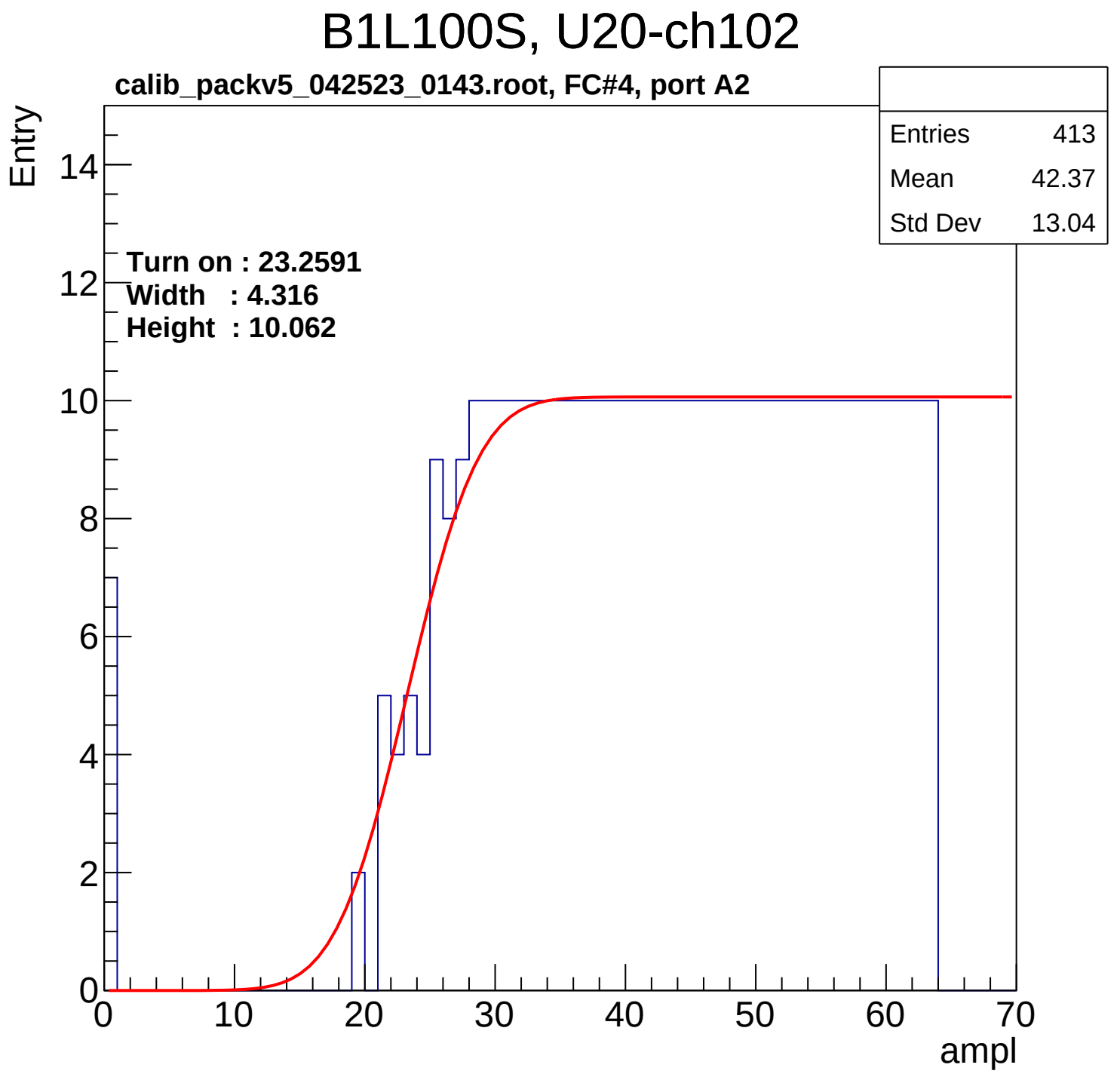
B1L100S, U20-ch102
calib_packv5_042523_0143.root, FC#4, port A2
Entries 413
Mean 42.37
Std Dev 13.04
Turn on : 23.2591
Width : 4.316
Height : 10.062
Entry
ampl
0
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6
8
10
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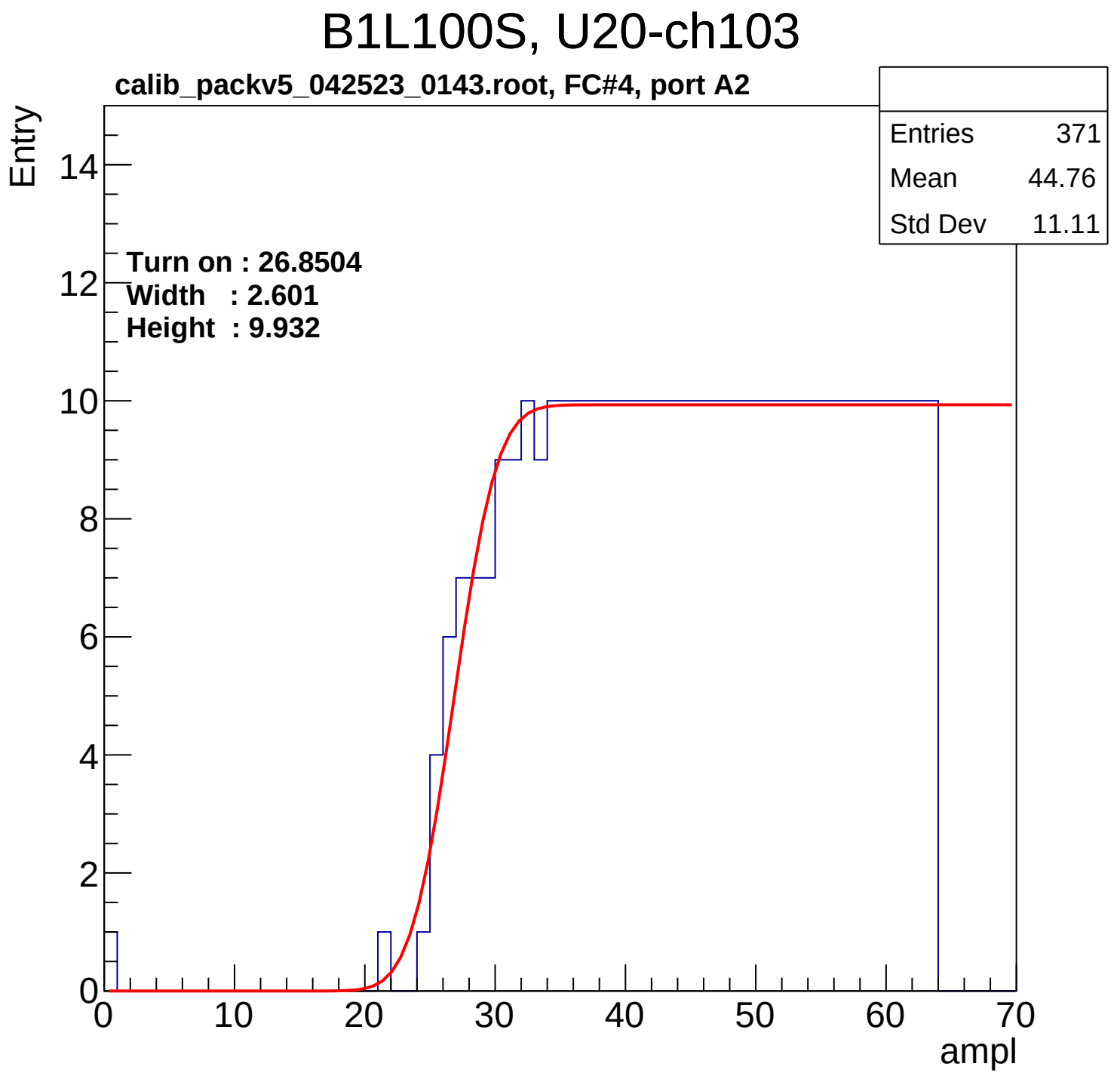
B1L100S, U20-ch103
calib_packv5_042523_0143.root, FC#4, port A2
Entries 371
Mean 44.76
Std Dev 11.11
Turn on : 26.8504
Width : 2.601
Height : 9.932
Entry
ampl
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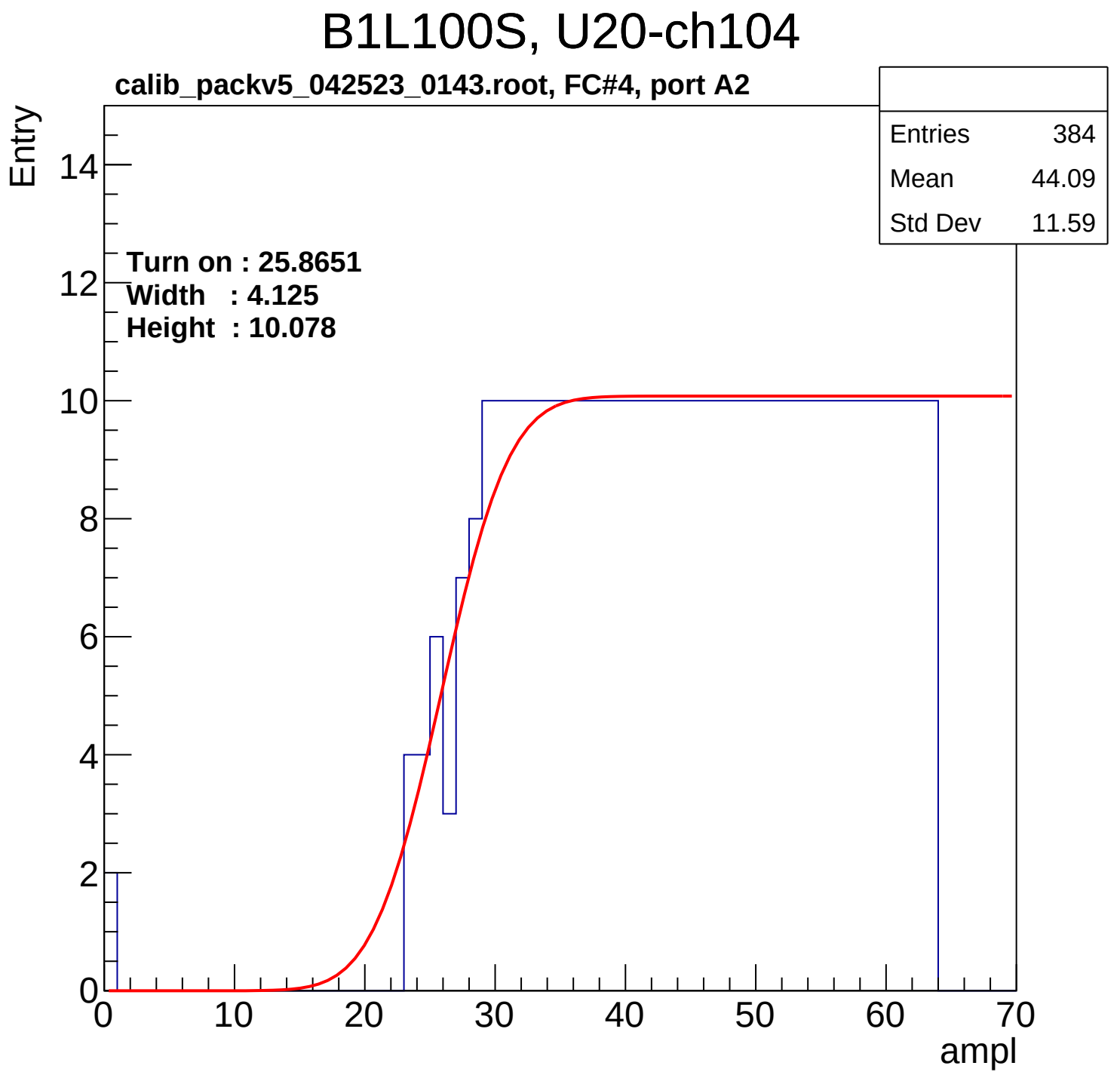
B1L100S, U20-ch104
calib_packv5_042523_0143.root, FC#4, port A2
Entries 384
Mean 44.09
Std Dev 11.59
Turn on : 25.8651
Width : 4.125
Height : 10.078
Entry
ampl
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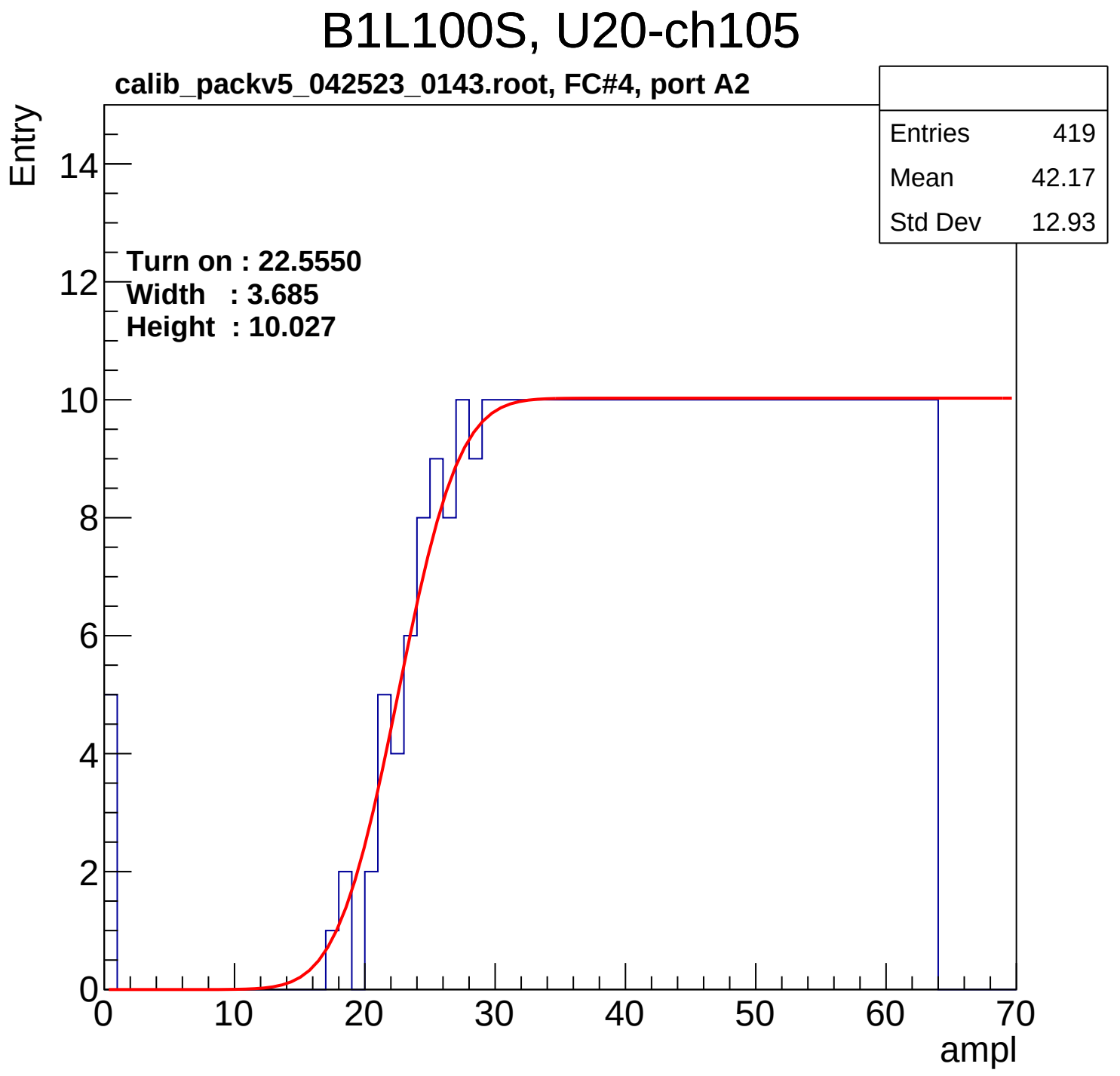
B1L100S, U20-ch105
calib_packv5_042523_0143.root, FC#4, port A2
Entries 419
Mean 42.17
Std Dev 12.93
Turn on : 22.5550
Width : 3.685
Height : 10.027
Entry
ampl
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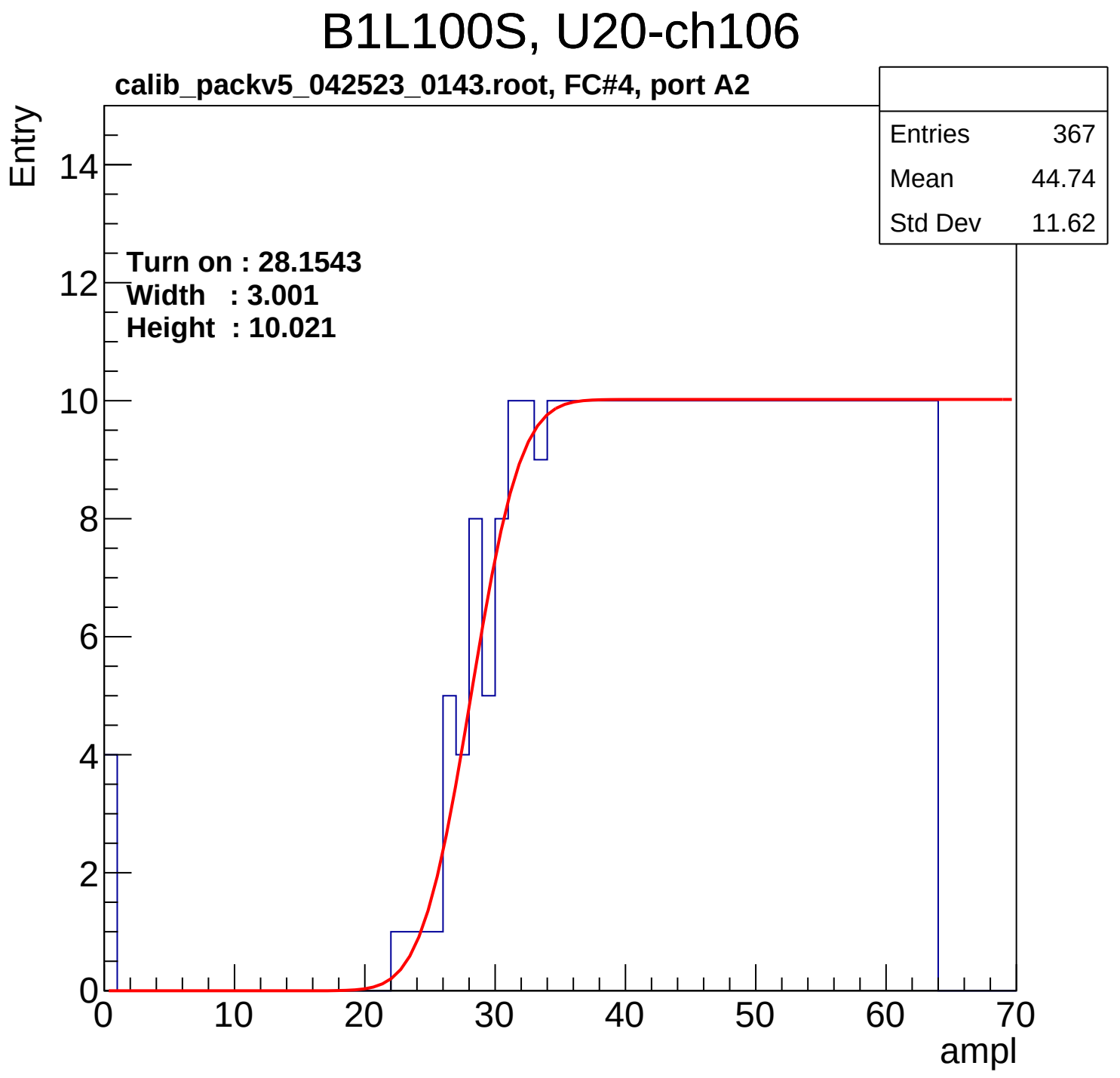
B1L100S, U20-ch106
calib_packv5_042523_0143.root, FC#4, port A2
Entries 367
Mean 44.74
Std Dev 11.62
Turn on : 28.1543
Width : 3.001
Height : 10.021
Entry
ampl
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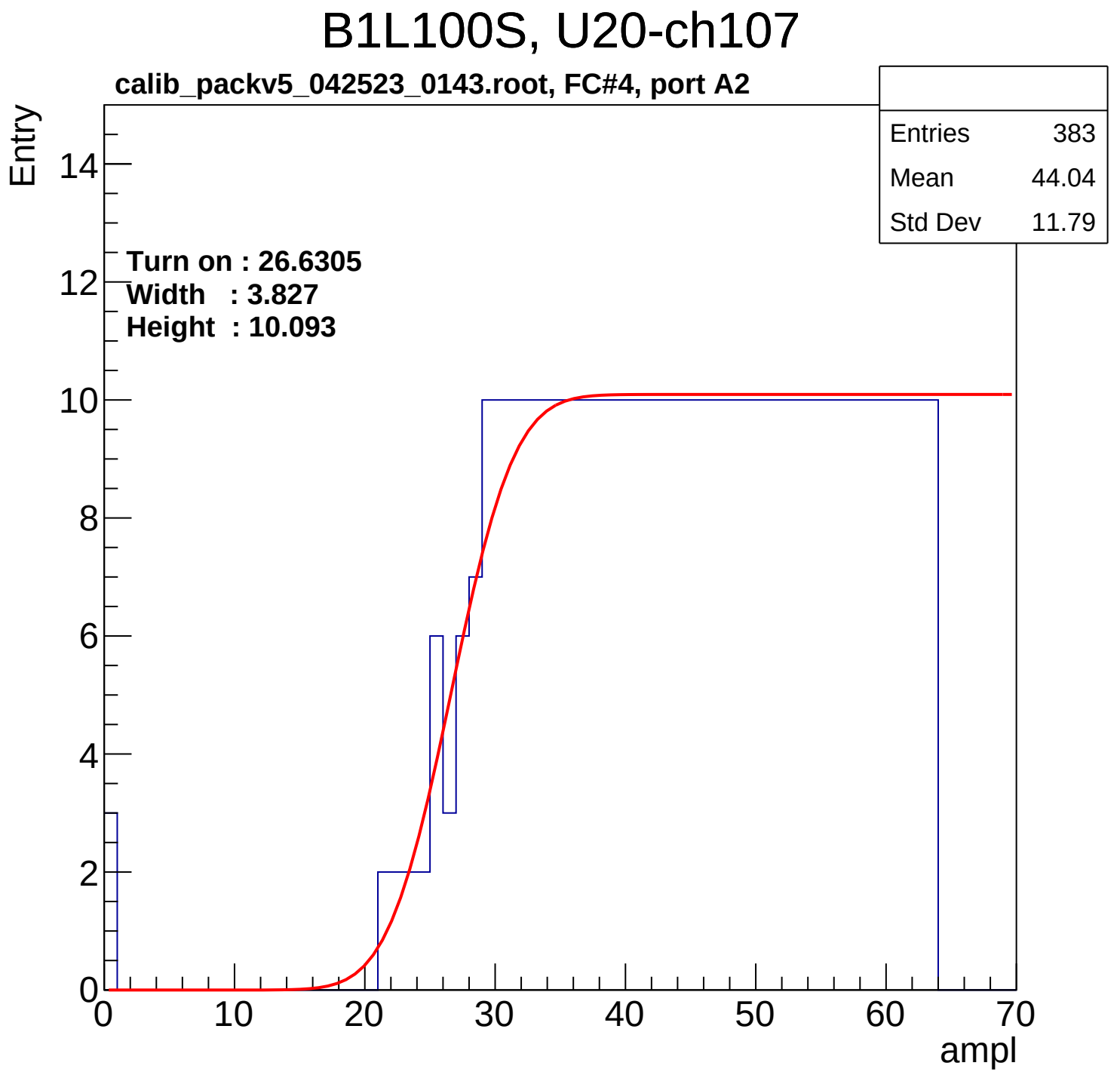
B1L100S, U20-ch107
calib_packv5_042523_0143.root, FC#4, port A2
Entries 383
Mean 44.04
Std Dev 11.79
Turn on : 26.6305
Width : 3.827
Height : 10.093
Entry
ampl
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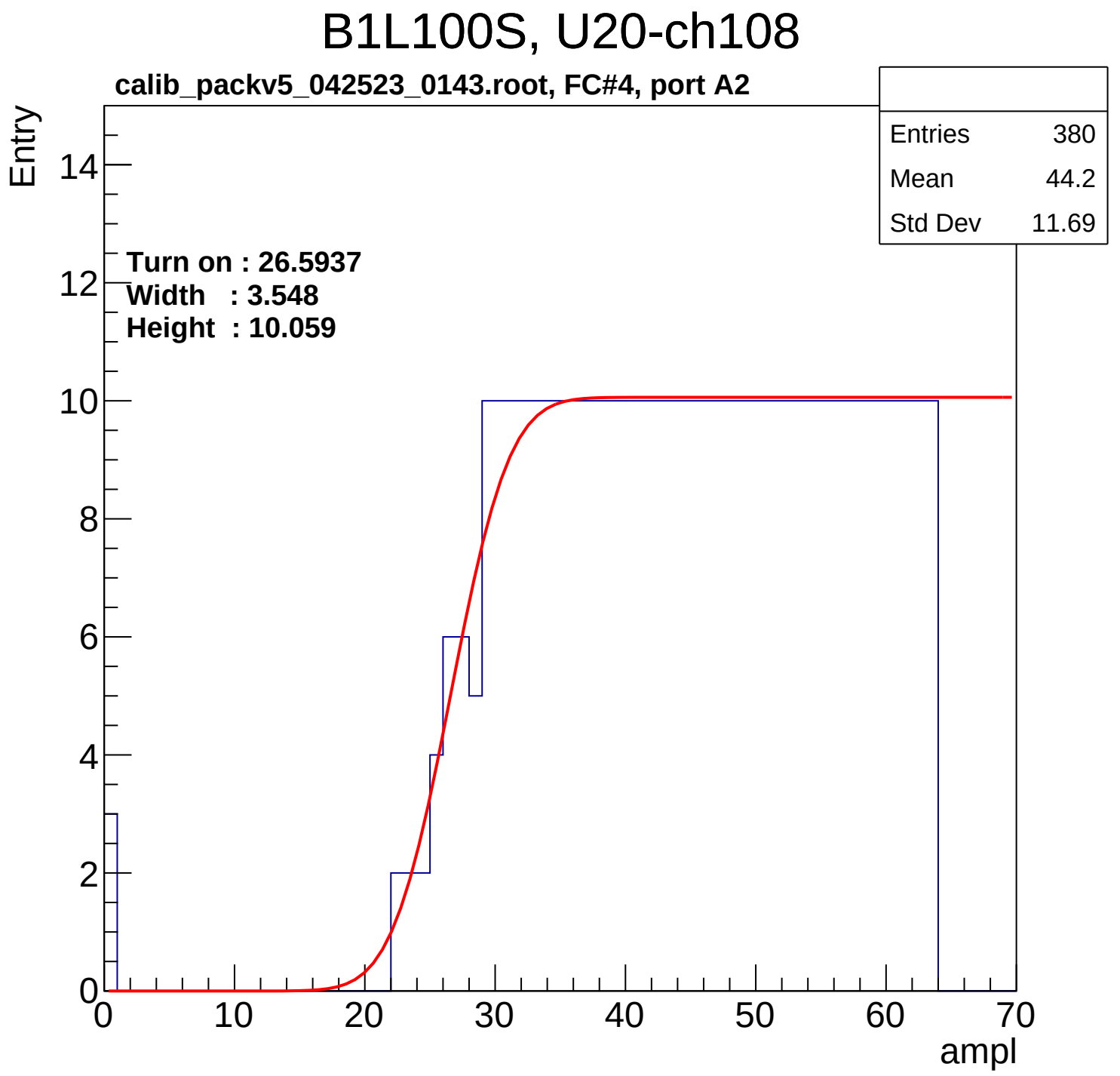
B1L100S, U20-ch108
calib_packv5_042523_0143.root, FC#4, port A2
Entries 380
Mean 44.2
Std Dev 11.69
Turn on : 26.5937
Width : 3.548
Height : 10.059
Entry
ampl
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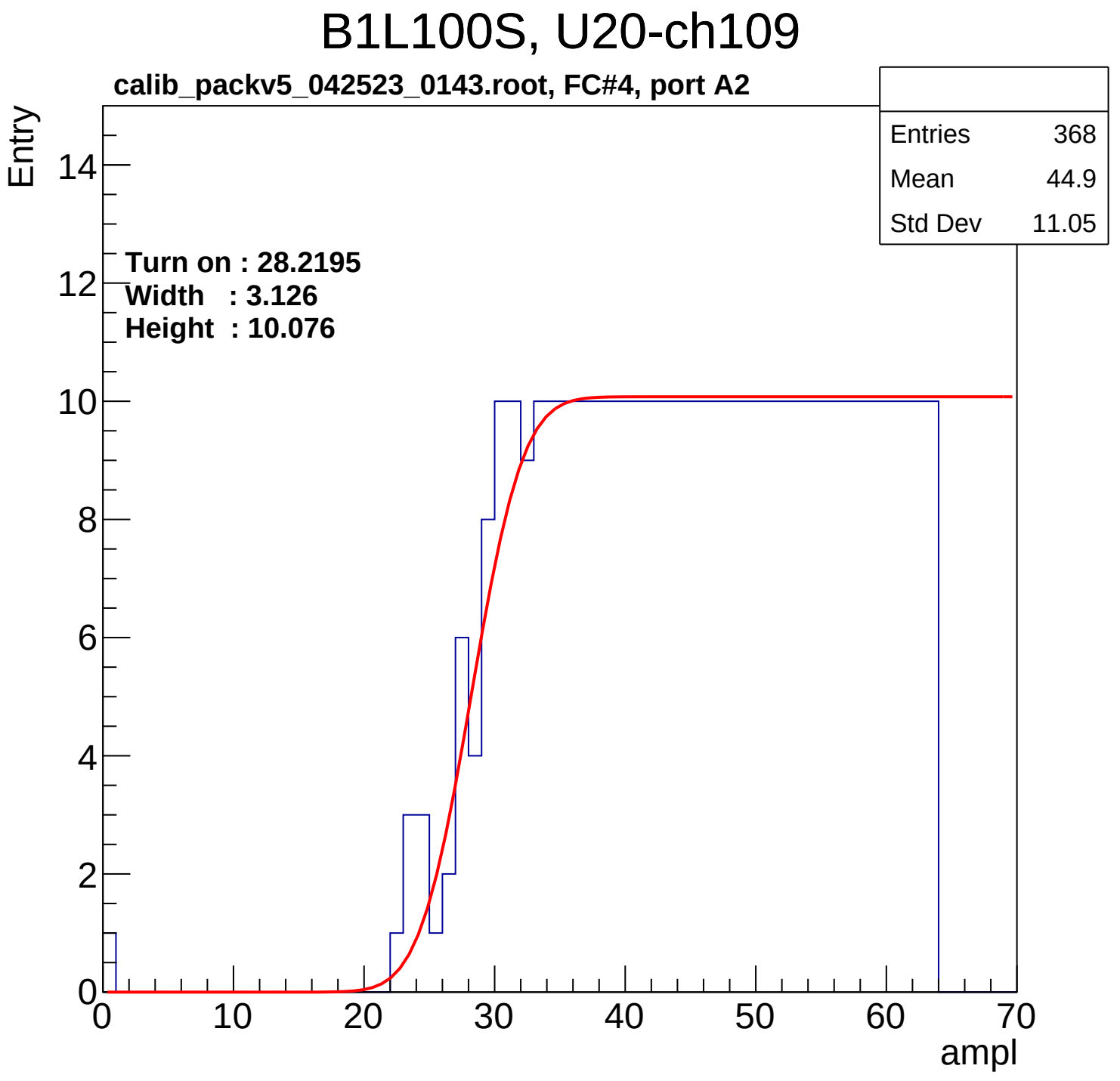
B1L100S, U20-ch109
calib_packv5_042523_0143.root, FC#4, port A2
Entries 368
Mean 44.9
Std Dev 11.05
Turn on : 28.2195
Width : 3.126
Height : 10.076
Entry
ampl
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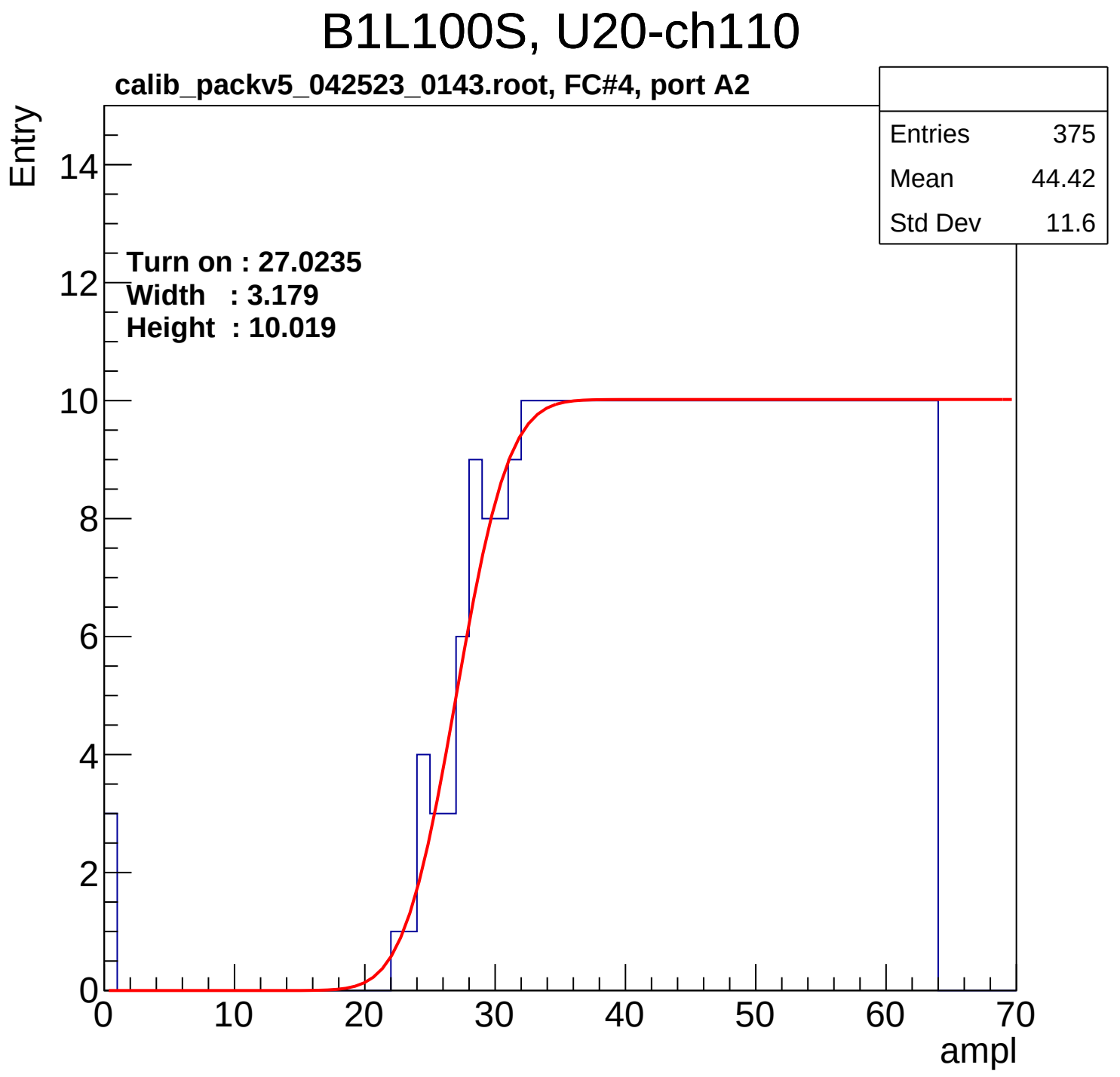
B1L100S, U20-ch110
calib_packv5_042523_0143.root, FC#4, port A2
Entries 375
Mean 44.42
Std Dev 11.6
Turn on : 27.0235
Width : 3.179
Height : 10.019
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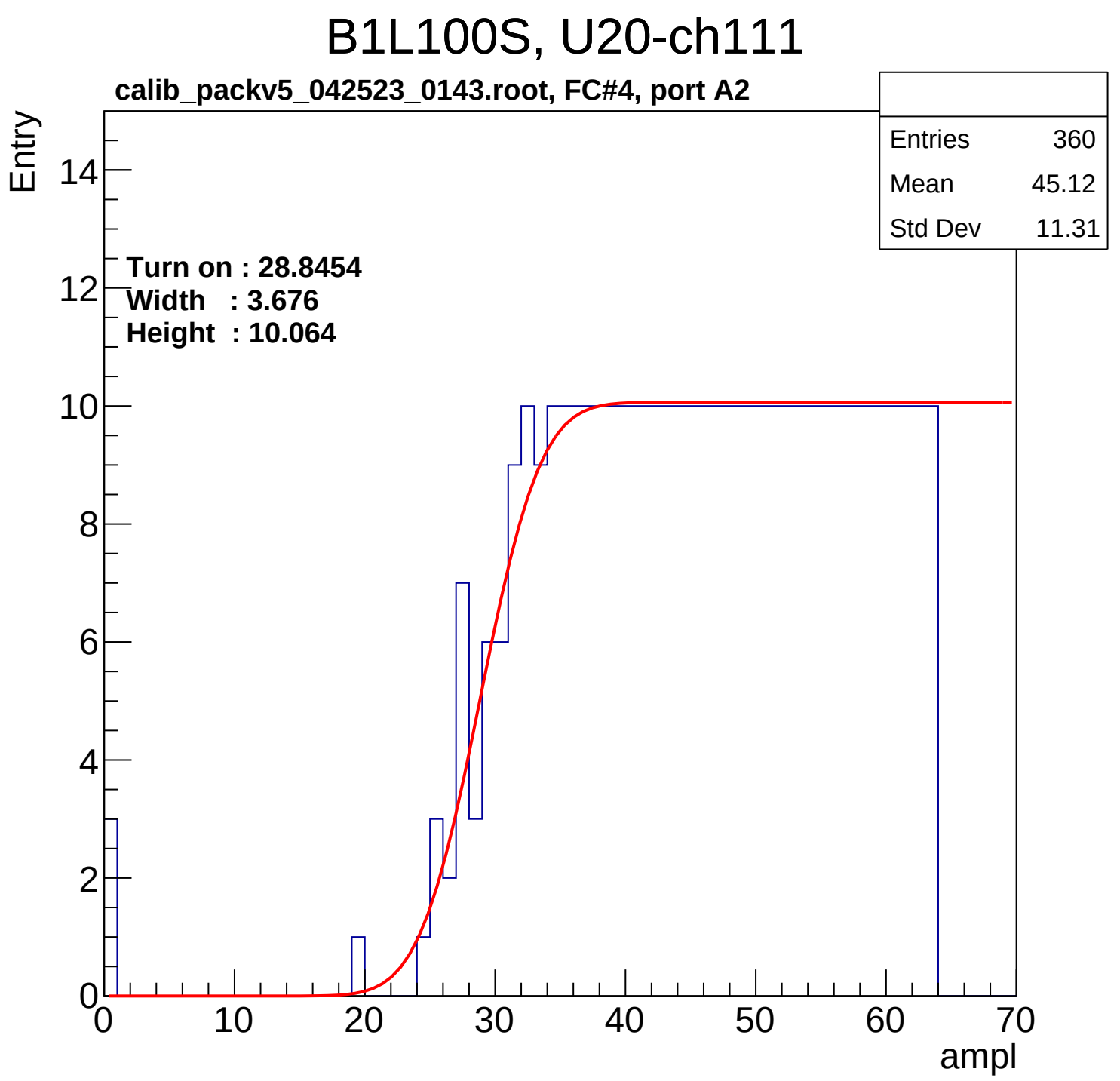
B1L100S, U20-ch111
calib_packv5_042523_0143.root, FC#4, port A2
Entries 360
Mean 45.12
Std Dev 11.31
Turn on : 28.8454
Width : 3.676
Height : 10.064
Entry
ampl
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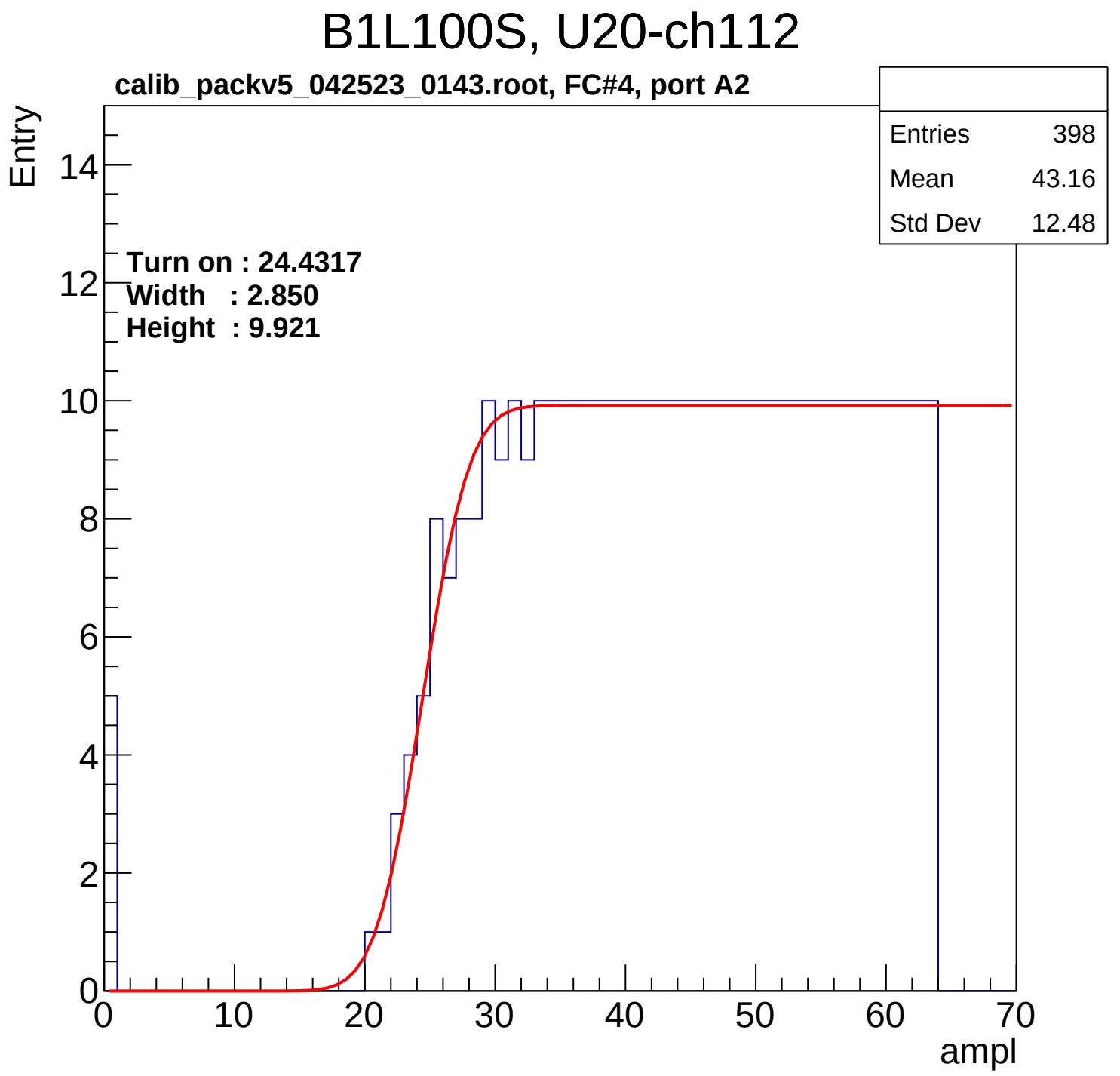
B1L100S, U20-ch112
calib_packv5_042523_0143.root, FC#4, port A2
Entries 398
Mean 43.16
Std Dev 12.48
Turn on : 24.4317
Width : 2.850
Height : 9.921
Entry
ampl
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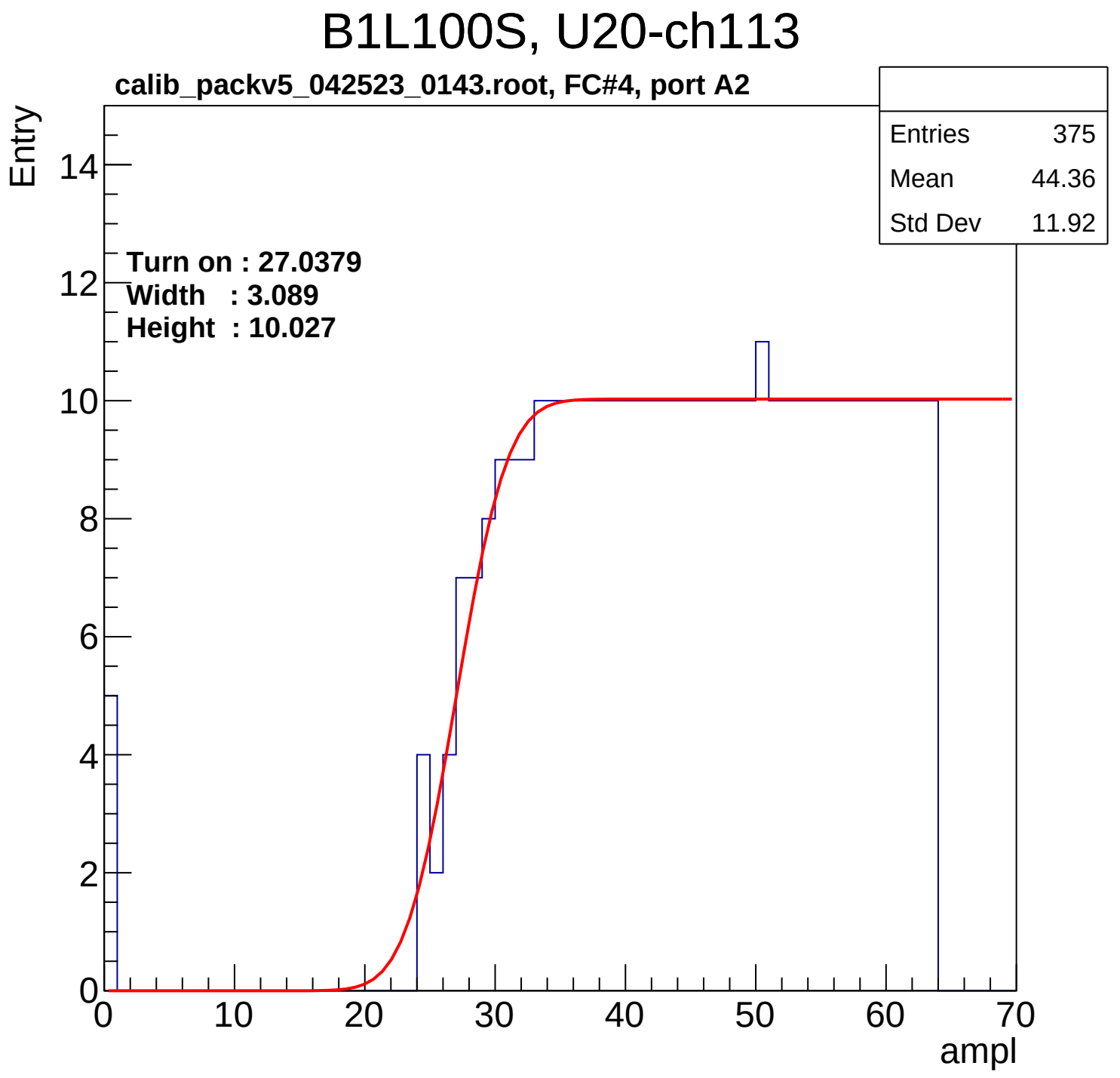
B1L100S, U20-ch113
calib_packv5_042523_0143.root, FC#4, port A2
Entries 375
Mean 44.36
Std Dev 11.92
Turn on : 27.0379
Width : 3.089
Height : 10.027
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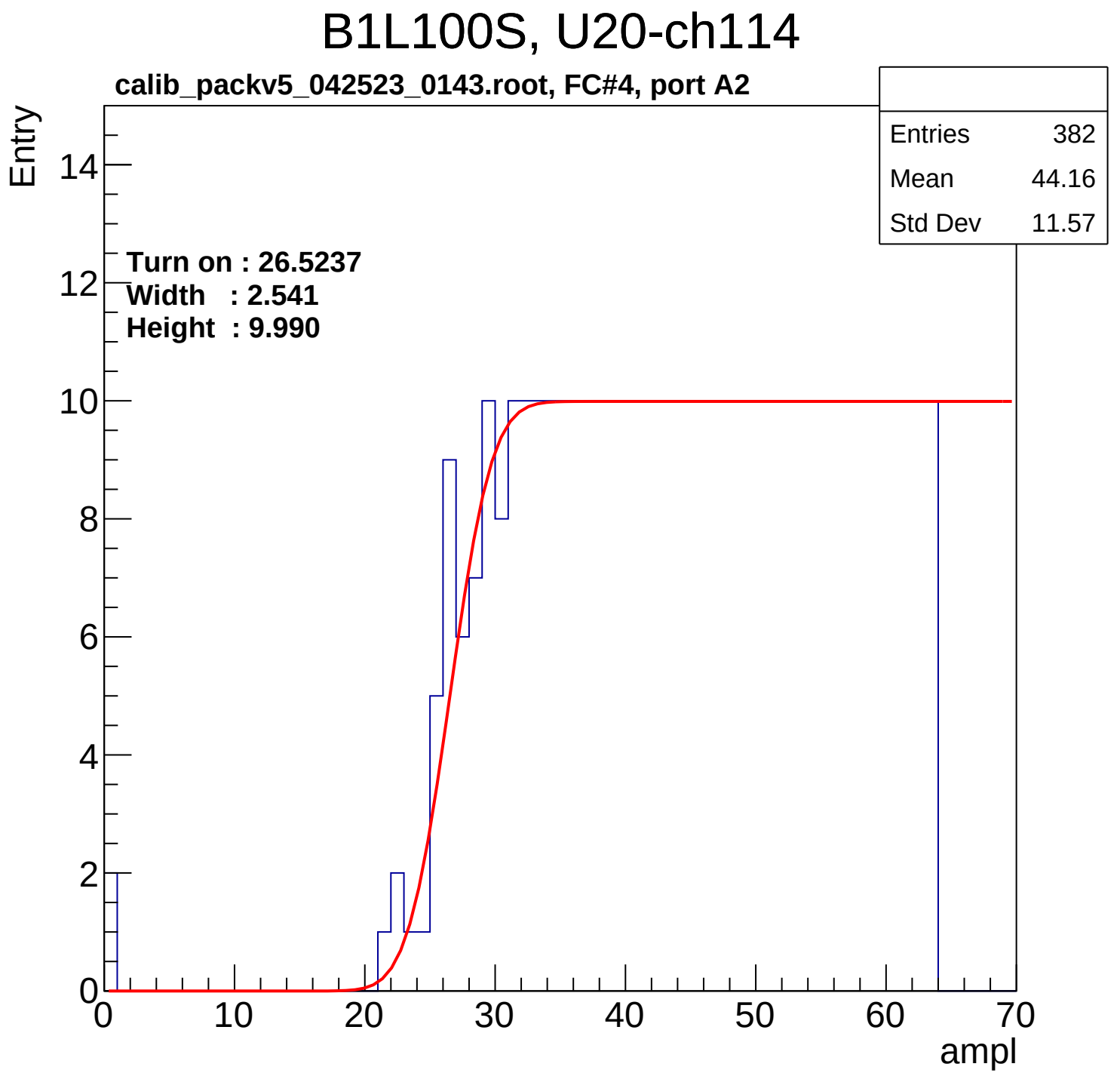
B1L100S, U20-ch114
calib_packv5_042523_0143.root, FC#4, port A2
Entries 382
Mean 44.16
Std Dev 11.57
Turn on : 26.5237
Width : 2.541
Height : 9.990
Entry
ampl
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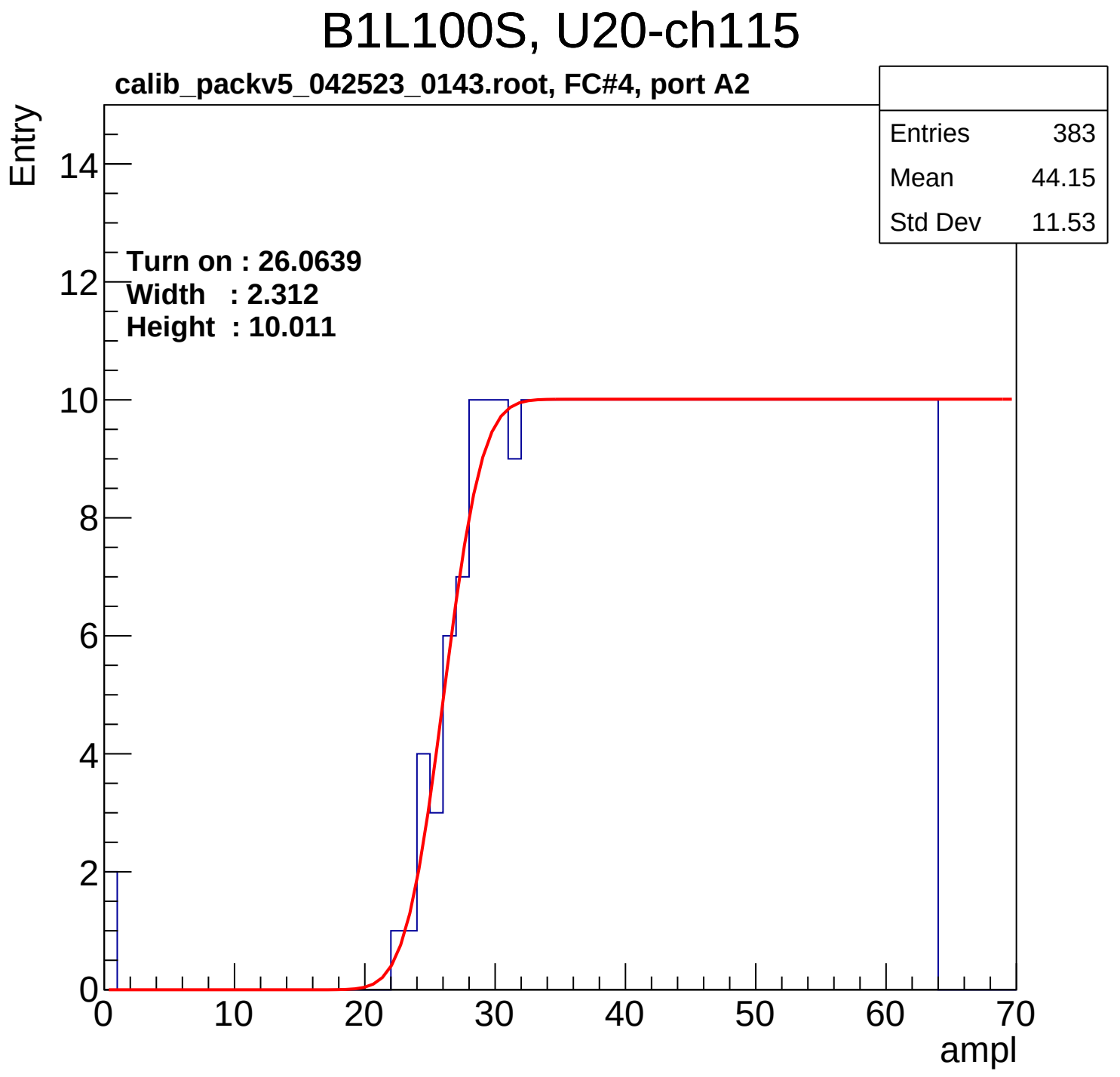
B1L100S, U20-ch115
calib_packv5_042523_0143.root, FC#4, port A2
Entries 383
Mean 44.15
Std Dev 11.53
Turn on : 26.0639
Width : 2.312
Height : 10.011
Entry
ampl
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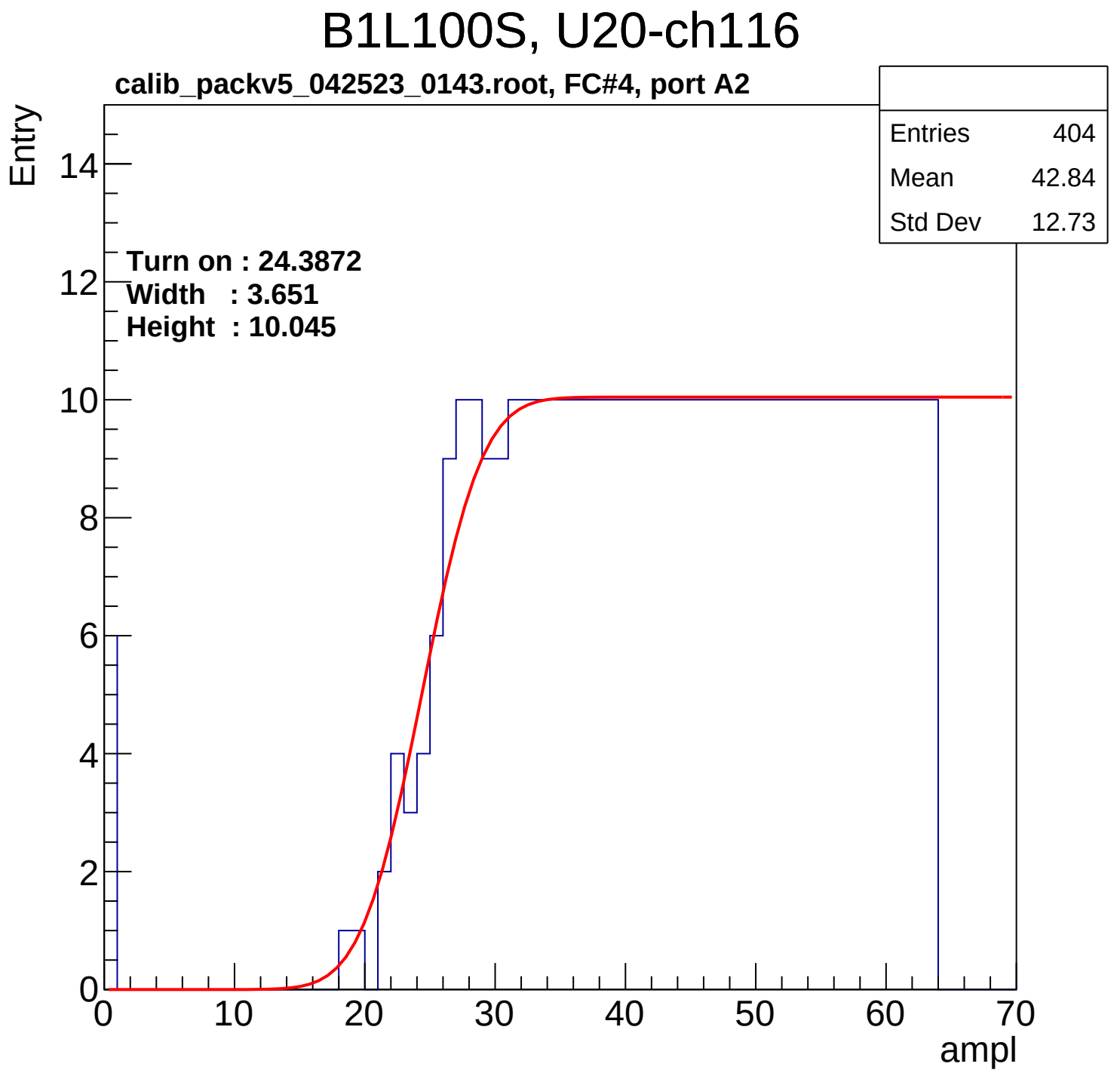
B1L100S, U20-ch116
calib_packv5_042523_0143.root, FC#4, port A2
Entries 404
Mean 42.84
Std Dev 12.73
Turn on : 24.3872
Width : 3.651
Height : 10.045
Entry
ampl
0
2
4
6
8
10
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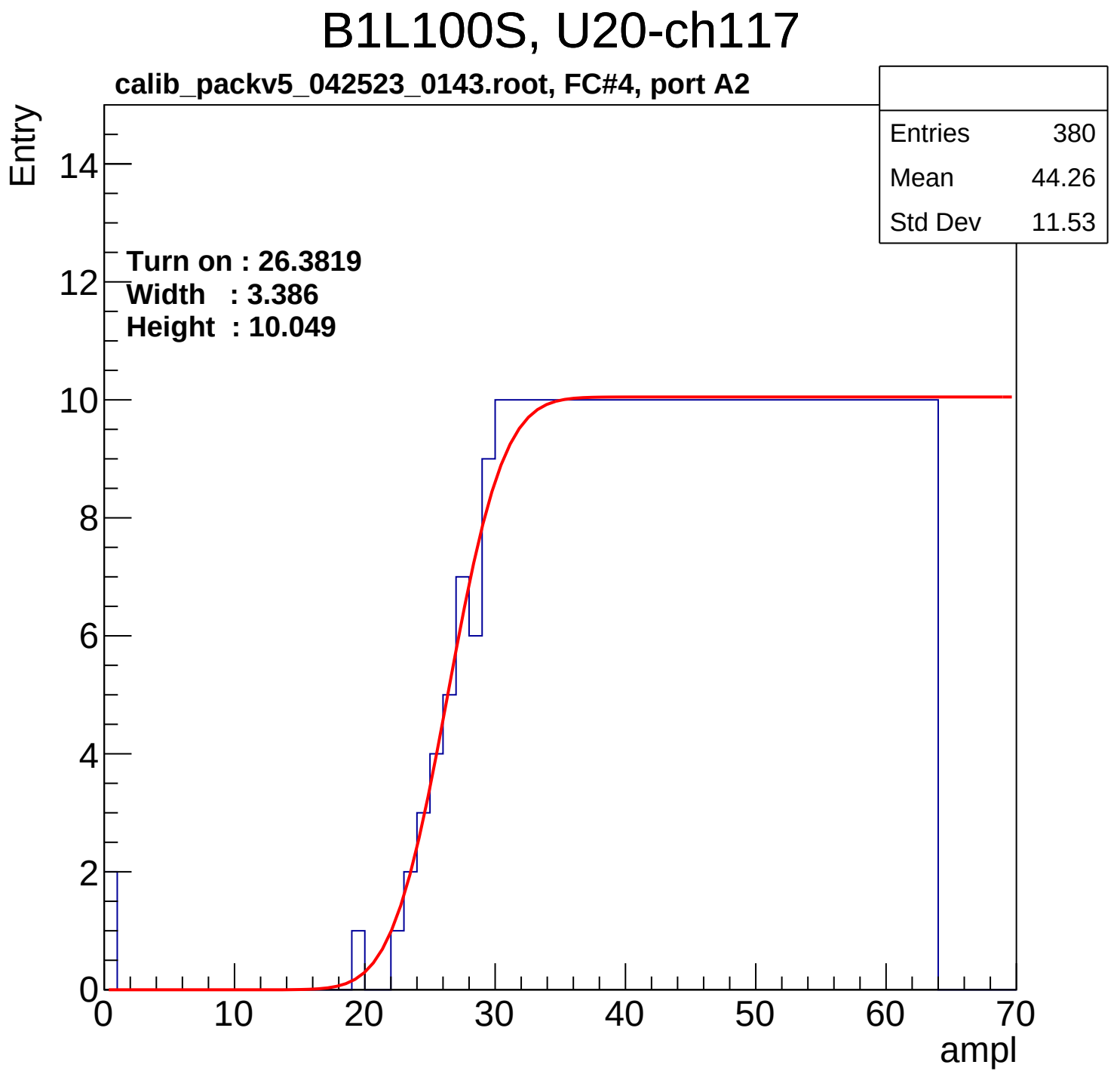
B1L100S, U20-ch117
calib_packv5_042523_0143.root, FC#4, port A2
Entries 380
Mean 44.26
Std Dev 11.53
Turn on : 26.3819
Width : 3.386
Height : 10.049
Entry
ampl
0
2
4
6
8
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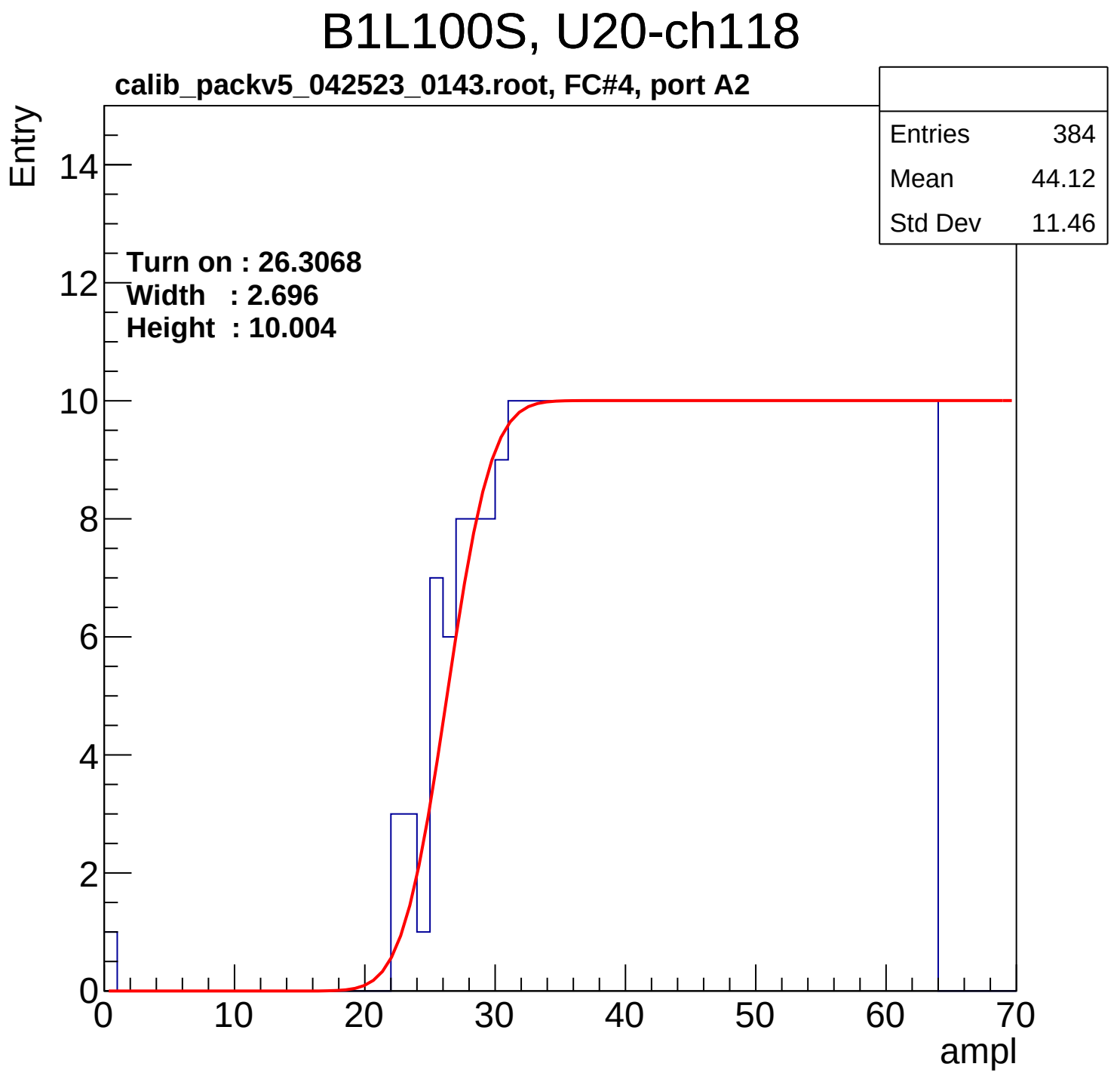
B1L100S, U20-ch118
calib_packv5_042523_0143.root, FC#4, port A2
Entries 384
Mean 44.12
Std Dev 11.46
Turn on : 26.3068
Width : 2.696
Height : 10.004
Entry
ampl
0
2
4
6
8
10
12
14
0
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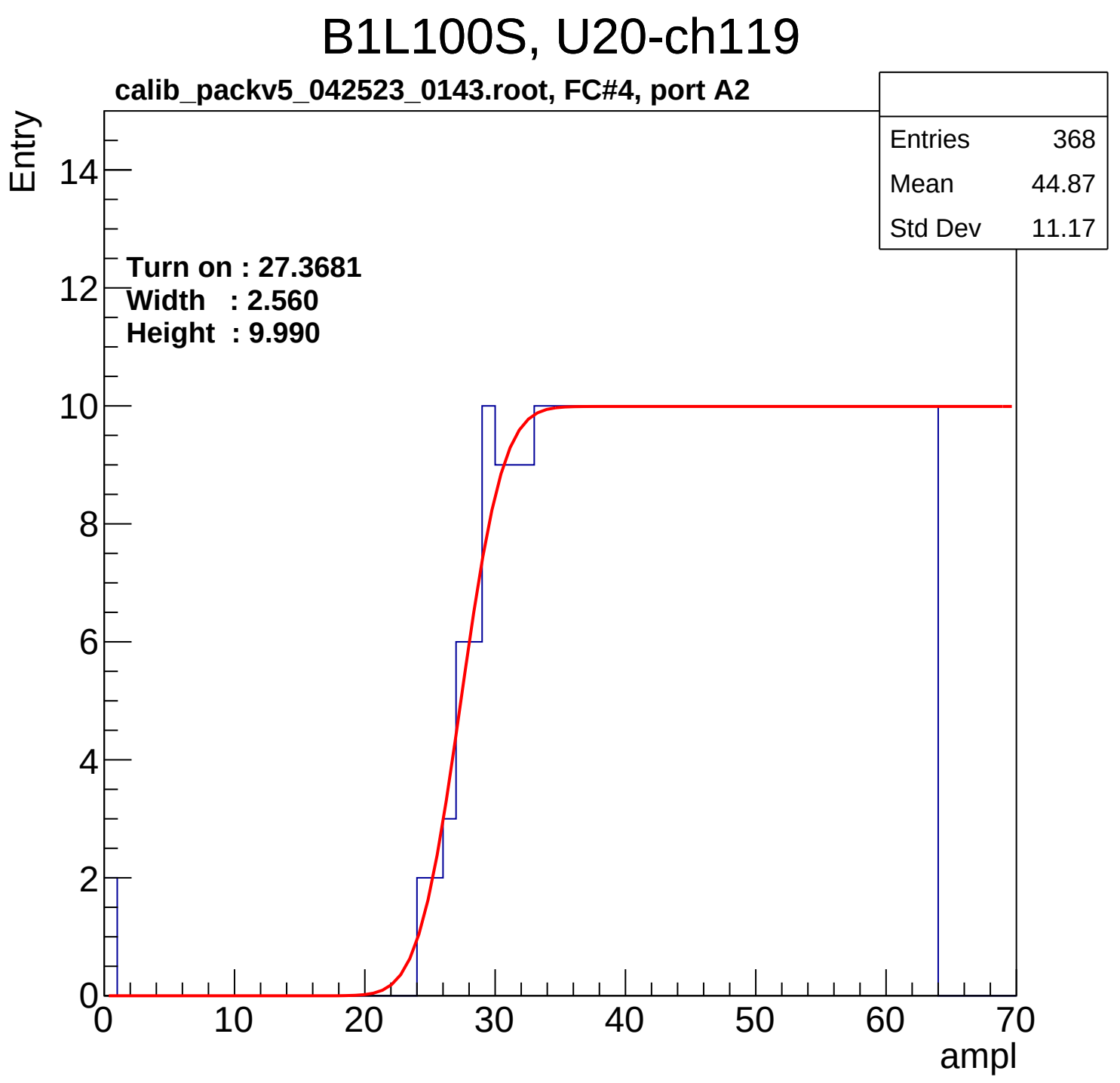
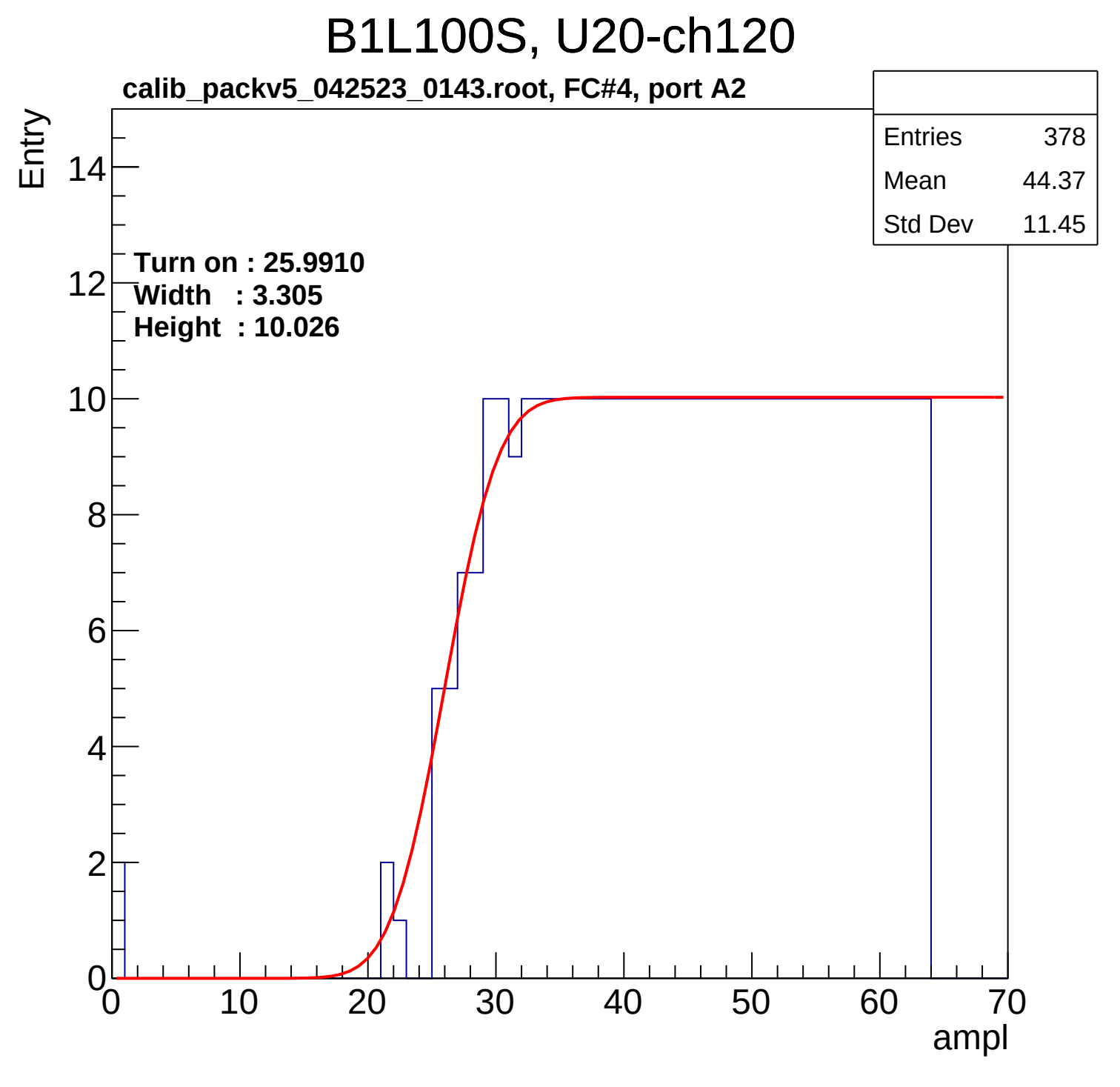

B1L100S, U20-ch119
calib_packv5_042523_0143.root, FC#4, port A2
Entries 368
Mean 44.87
Std Dev 11.17
Turn on : 27.3681
Width : 2.560
Height : 9.990
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L100S, U20-ch120
calib_packv5_042523_0143.root, FC#4, port A2
Entries 378
Mean 44.37
Std Dev 11.45
Turn on : 25.9910
Width : 3.305
Height : 10.026
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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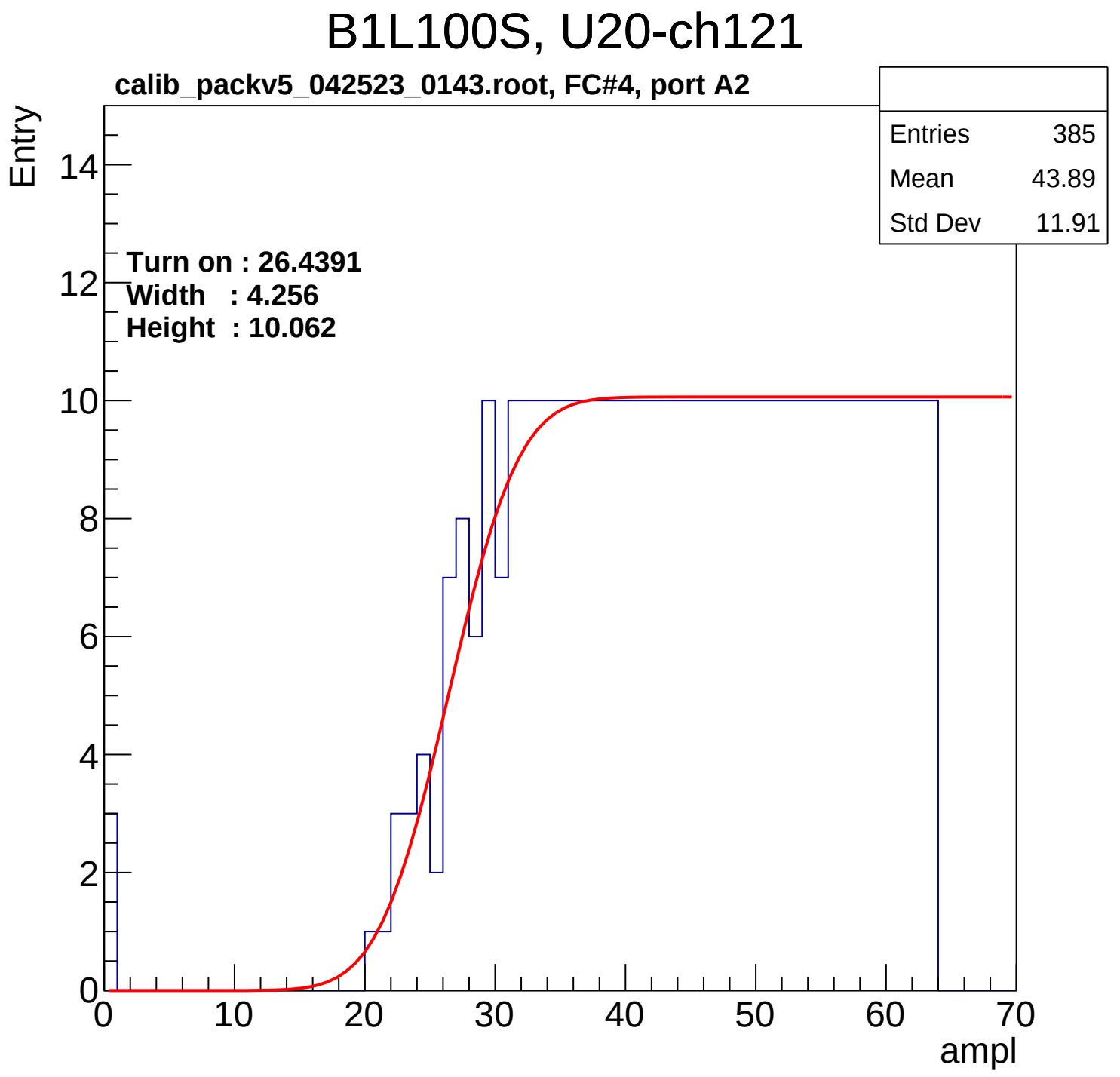
B1L100S, U20-ch121
calib_packv5_042523_0143.root, FC#4, port A2
Entries 385
Mean 43.89
Std Dev 11.91
Turn on : 26.4391
Width : 4.256
Height : 10.062
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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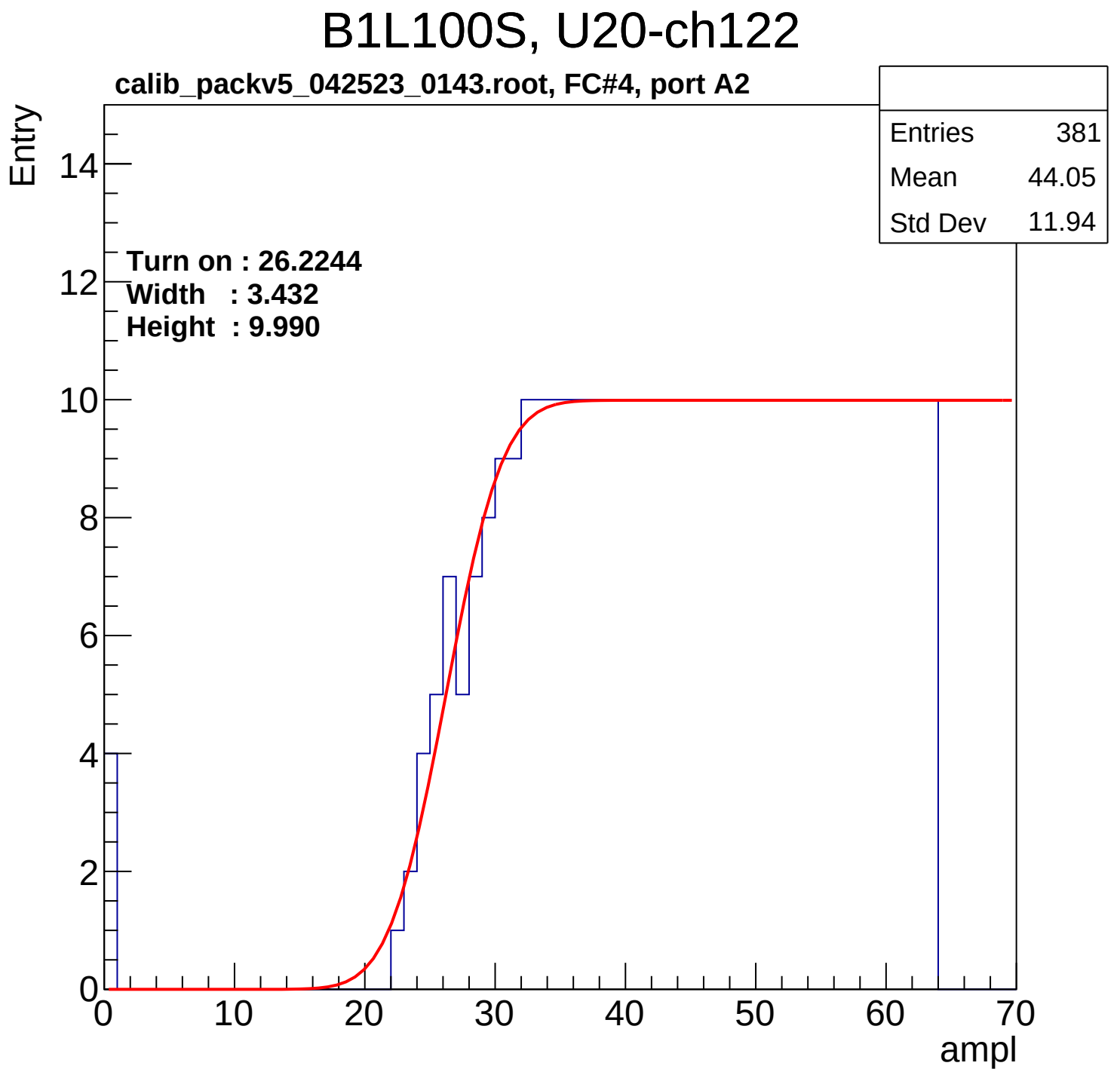
B1L100S, U20-ch122
calib_packv5_042523_0143.root, FC#4, port A2
Entries 381
Mean 44.05
Std Dev 11.94
Turn on : 26.2244
Width : 3.432
Height : 9.990
Entry
ampl
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6
8
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10
20
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40
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60
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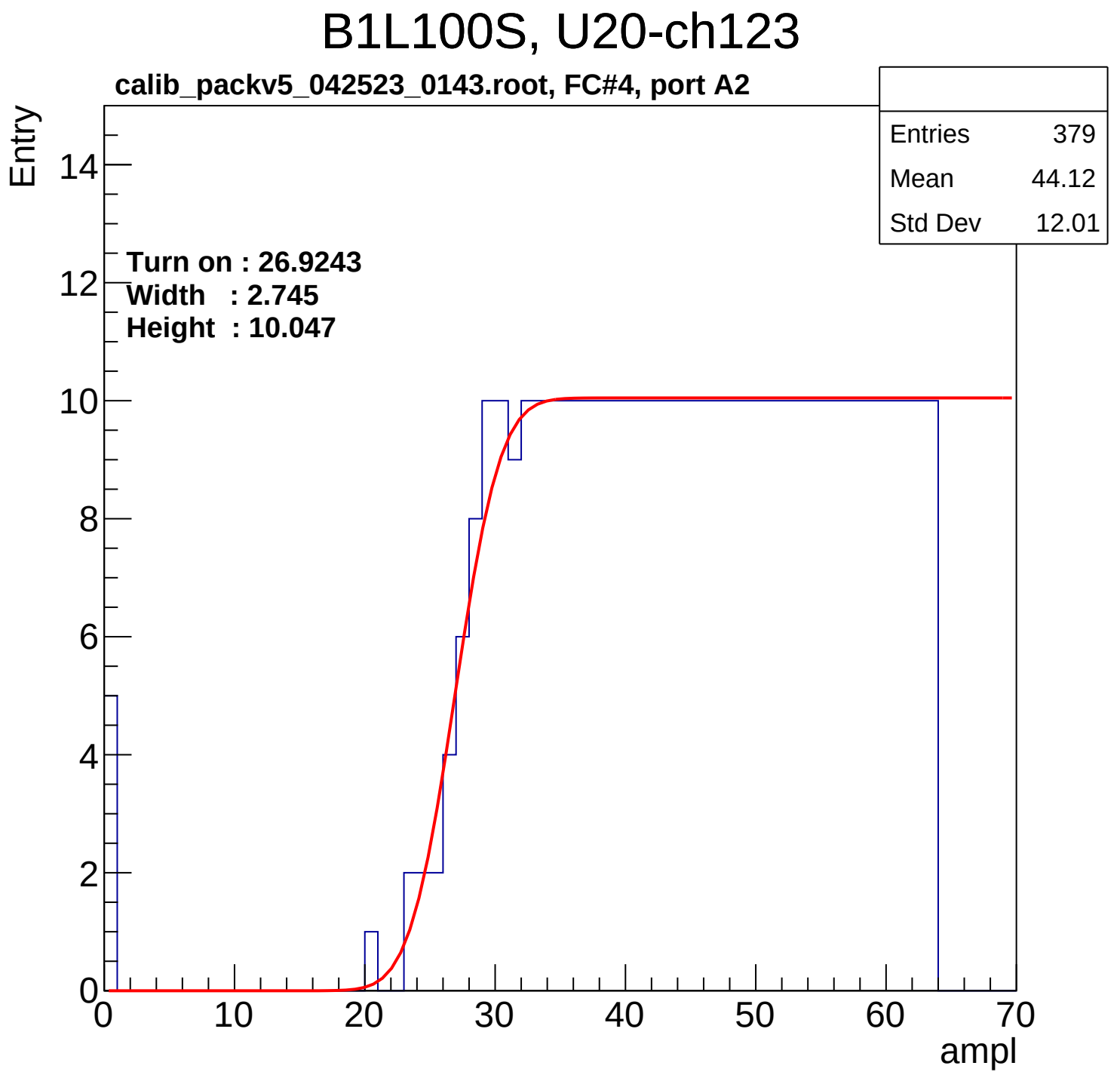
B1L100S, U20-ch123
calib_packv5_042523_0143.root, FC#4, port A2
Entries 379
Mean 44.12
Std Dev 12.01
Turn on : 26.9243
Width : 2.745
Height : 10.047
Entry
ampl
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4
6
8
10
12
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0
10
20
30
40
50
60
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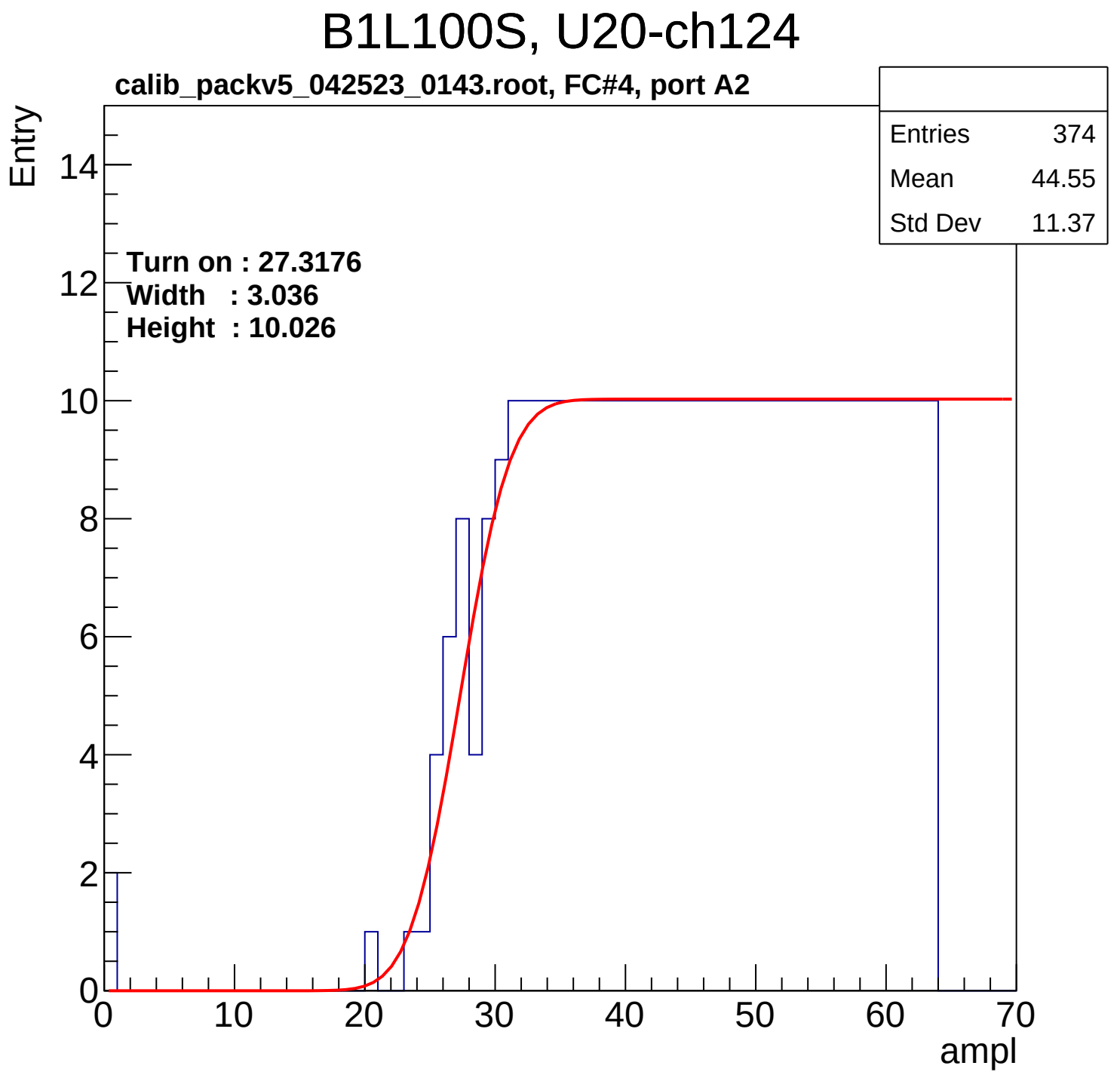
B1L100S, U20-ch124
calib_packv5_042523_0143.root, FC#4, port A2
Entries 374
Mean 44.55
Std Dev 11.37
Turn on : 27.3176
Width : 3.036
Height : 10.026
Entry
ampl
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4
6
8
10
12
14
0
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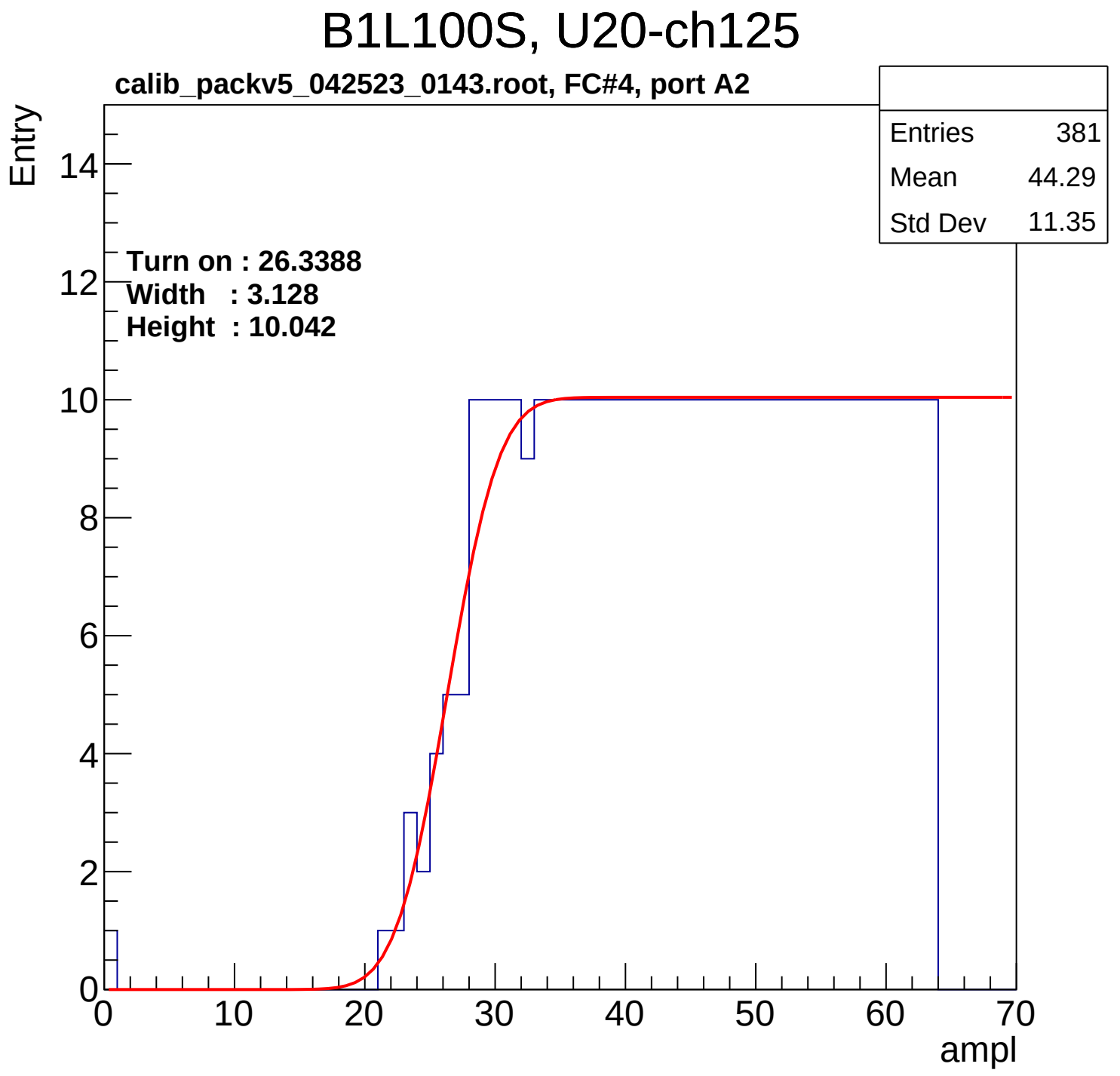
20
30
40
50
60
70


B1L100S, U20-ch125
calib_packv5_042523_0143.root, FC#4, port A2
Entries 381
Mean 44.29
Std Dev 11.35
Turn on : 26.3388
Width : 3.128
Height : 10.042
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
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60
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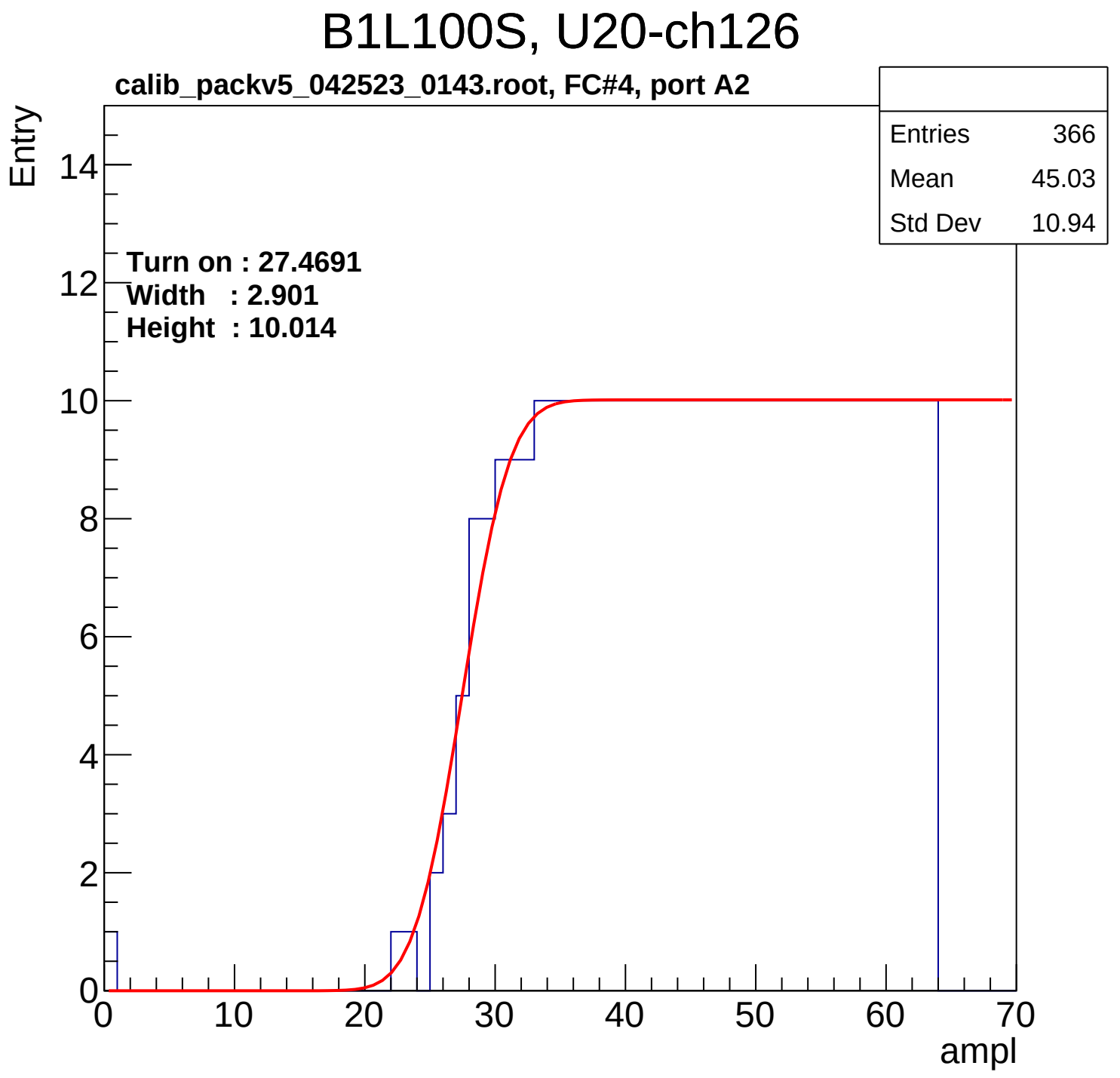
B1L100S, U20-ch126
calib_packv5_042523_0143.root, FC#4, port A2
Entries 366
Mean 45.03
Std Dev 10.94
Turn on : 27.4691
Width : 2.901
Height : 10.014
Entry
ampl
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6
8
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0
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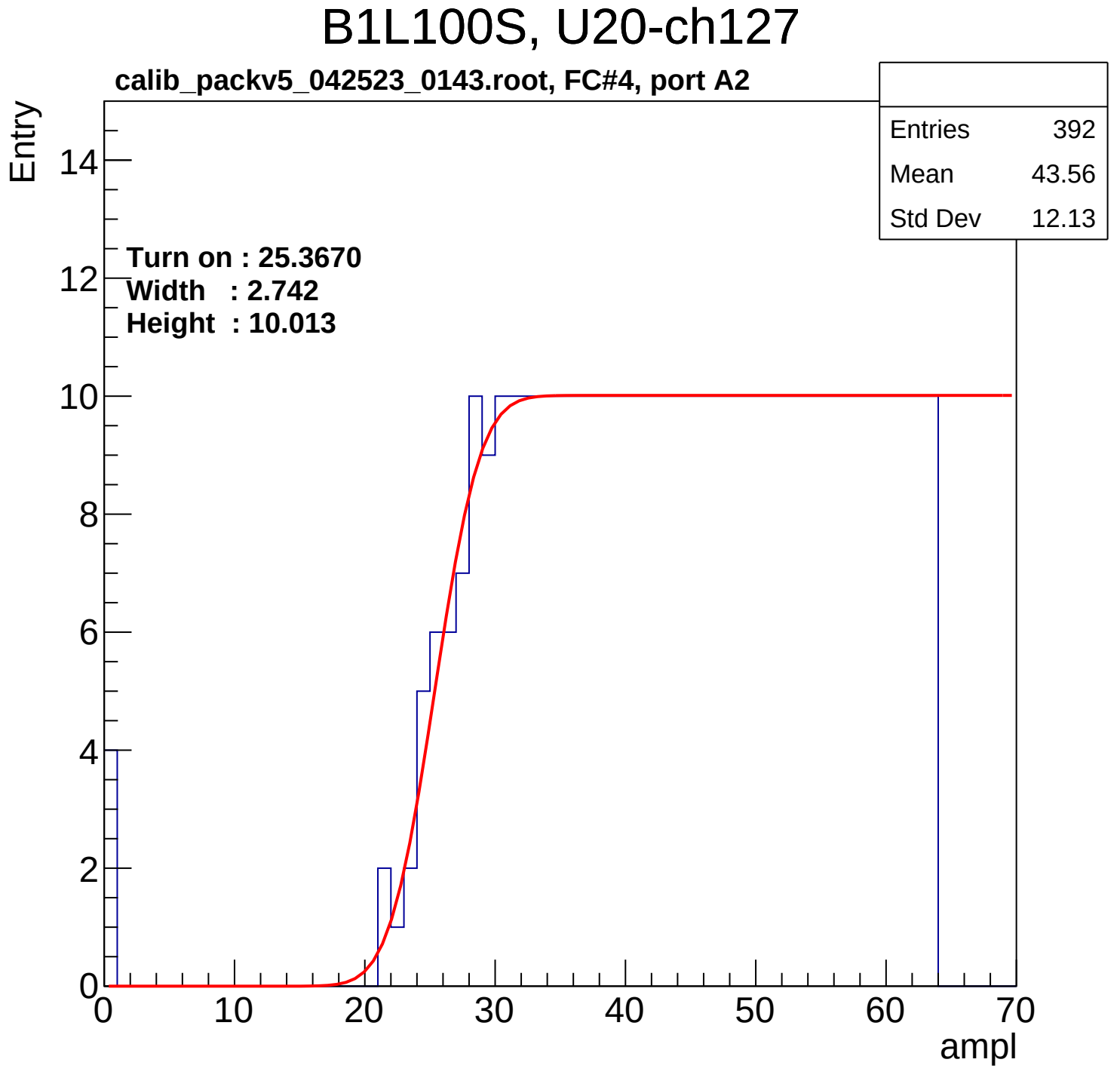
B1L100S, U20-ch127
calib_packv5_042523_0143.root, FC#4, port A2
Entries 392
Mean 43.56
Std Dev 12.13
Turn on : 25.3670
Width : 2.742
Height : 10.013
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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60
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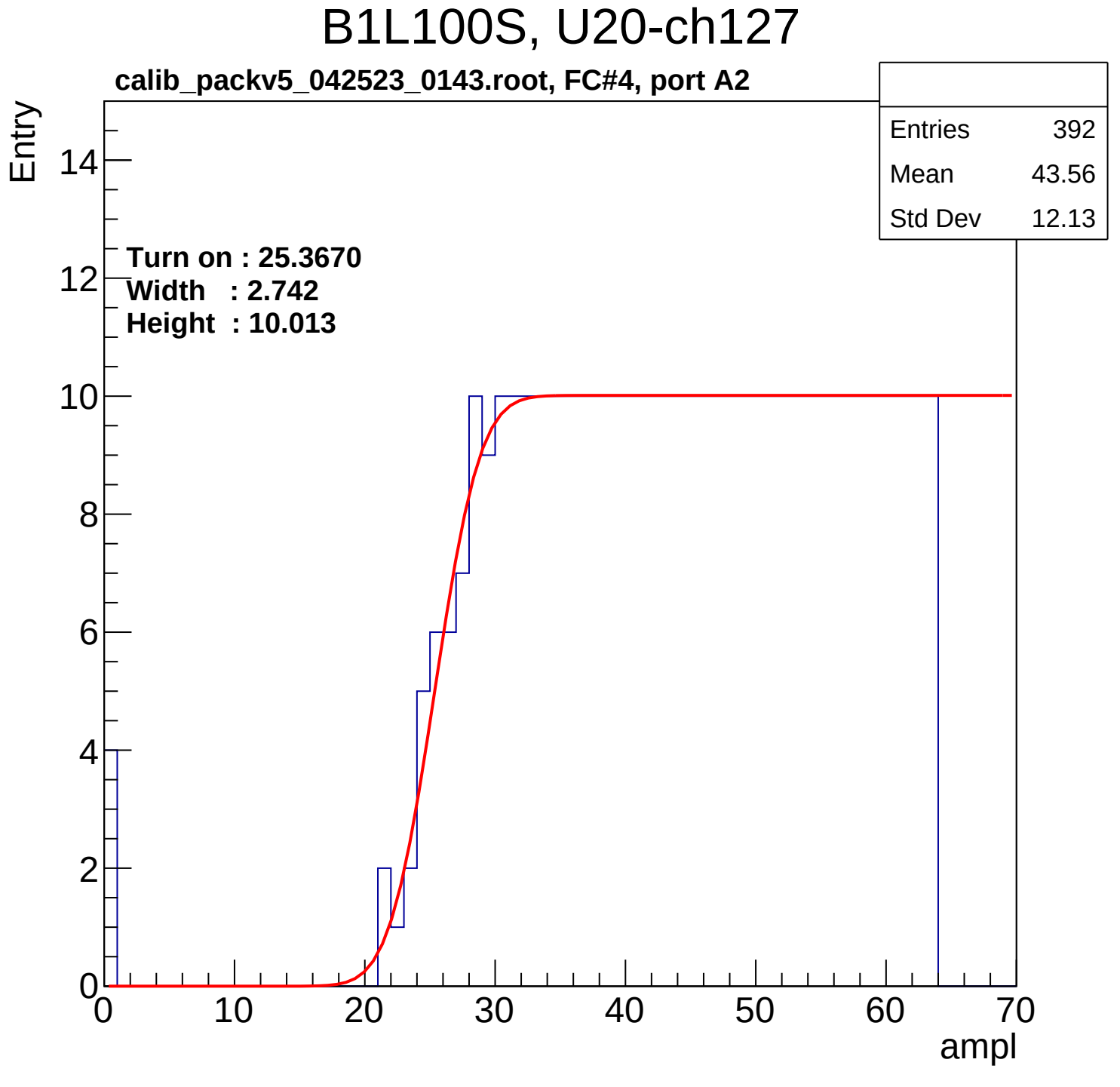
B1L100S, U20-ch127
calib_packv5_042523_0143.root, FC#4, port A2
Entries 392
Mean 43.56
Std Dev 12.13
Turn on : 25.3670
Width : 2.742
Height : 10.013
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70