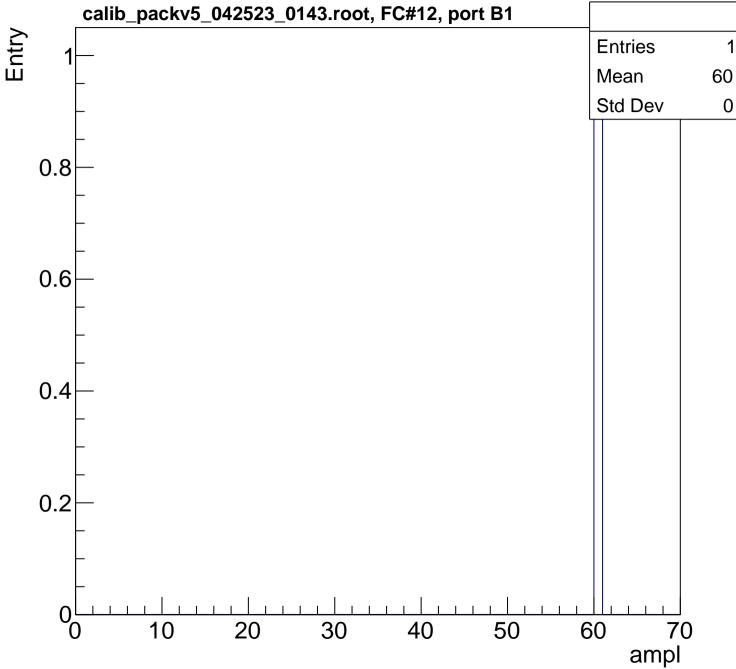
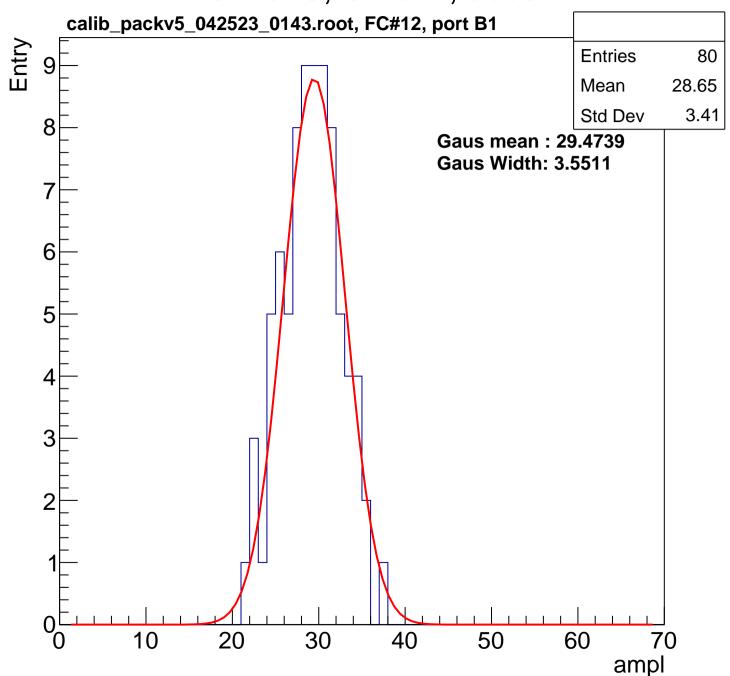
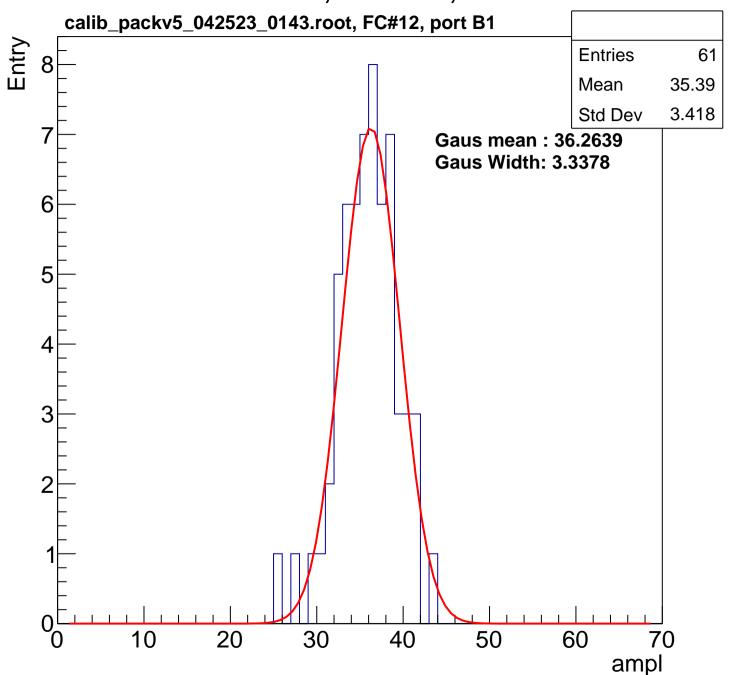
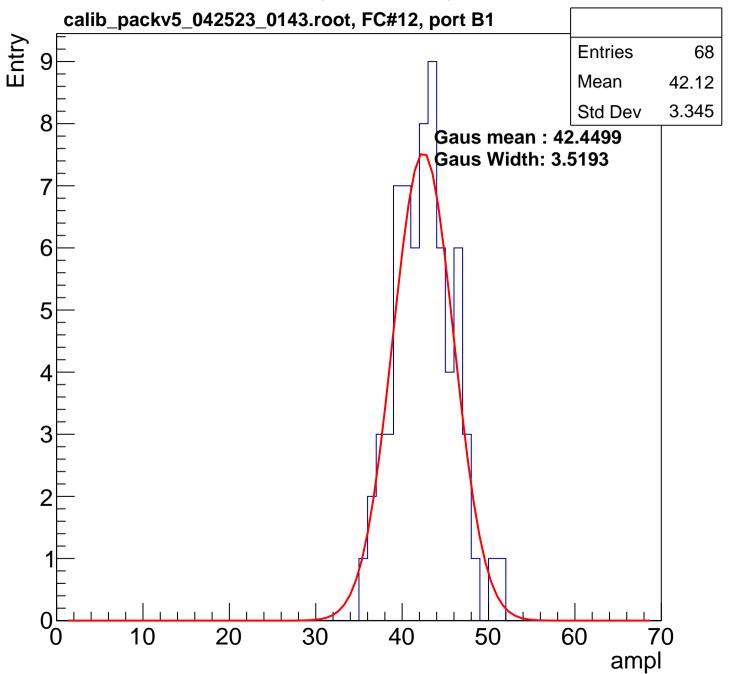


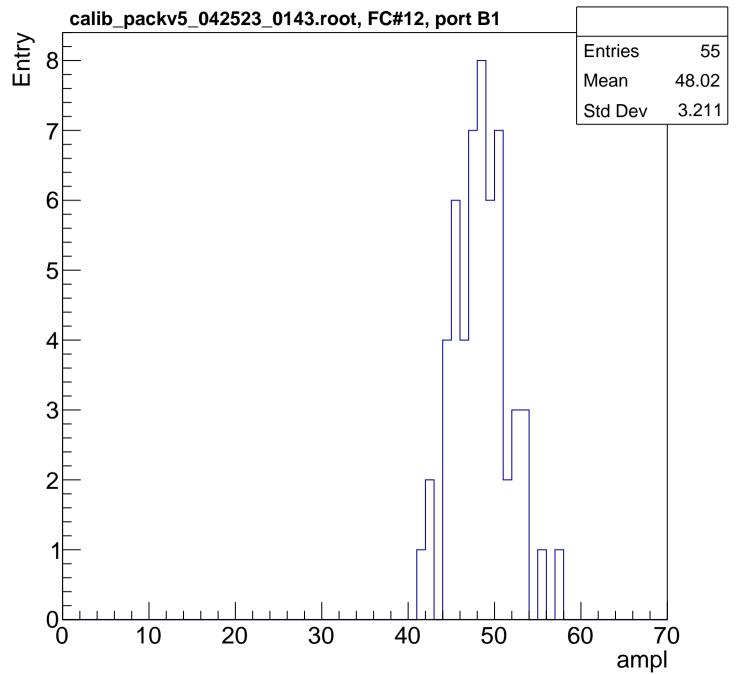
0

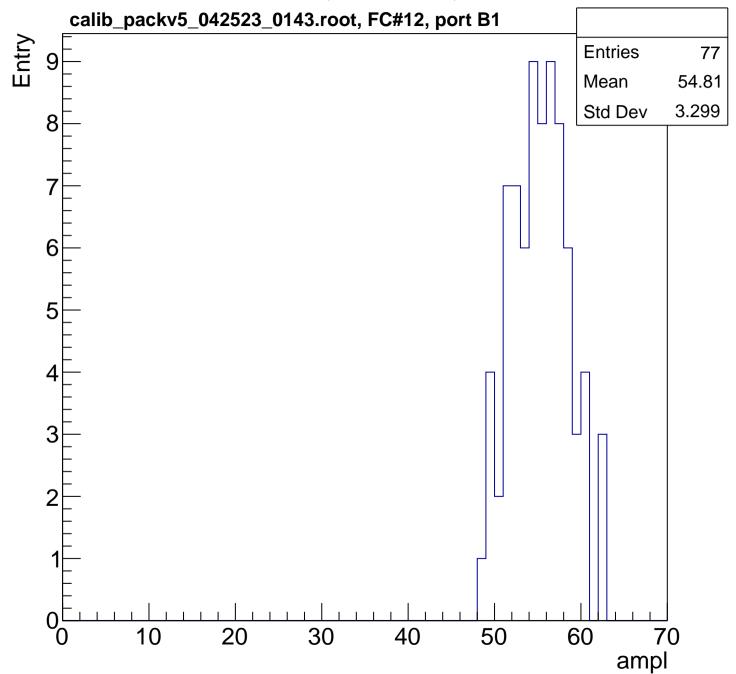


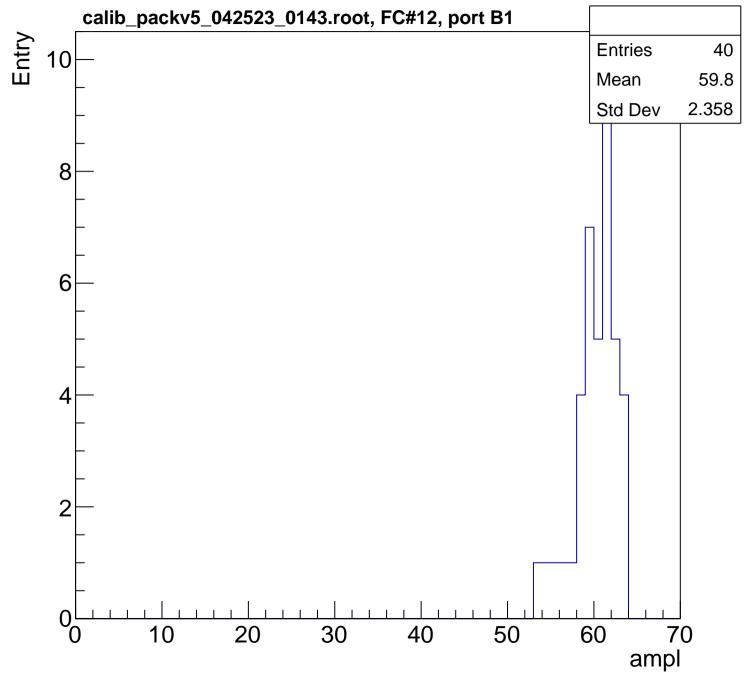


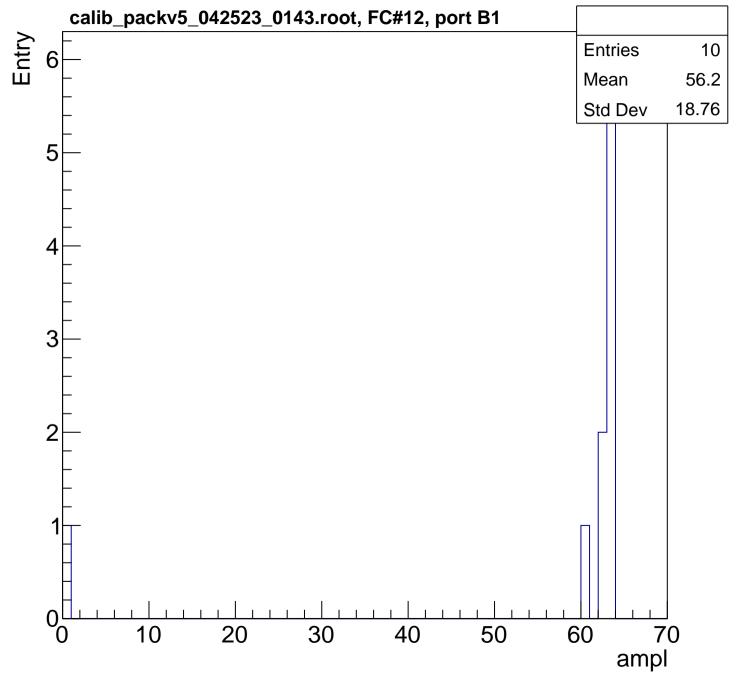




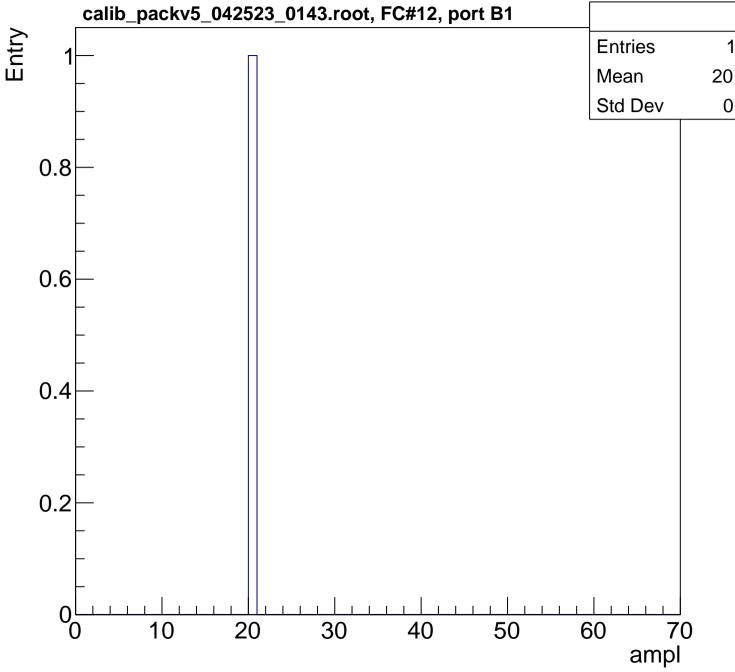


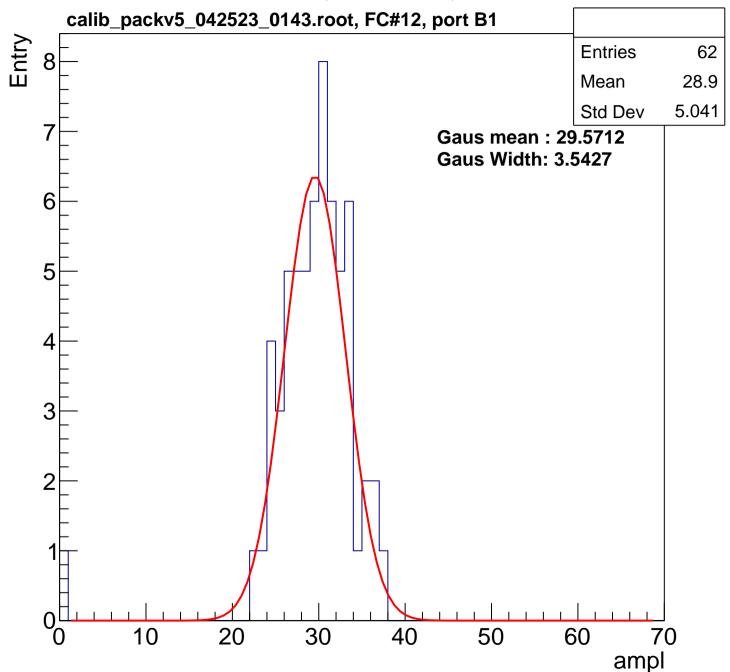


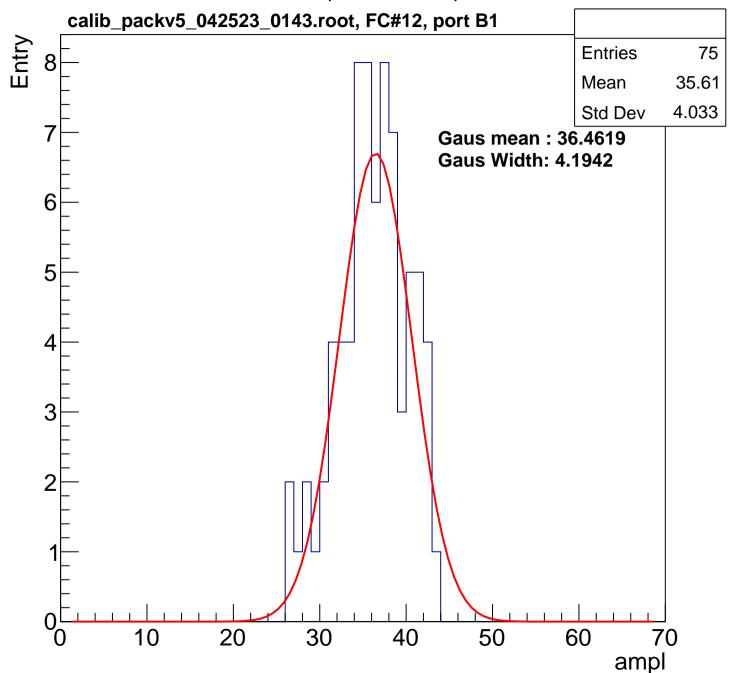


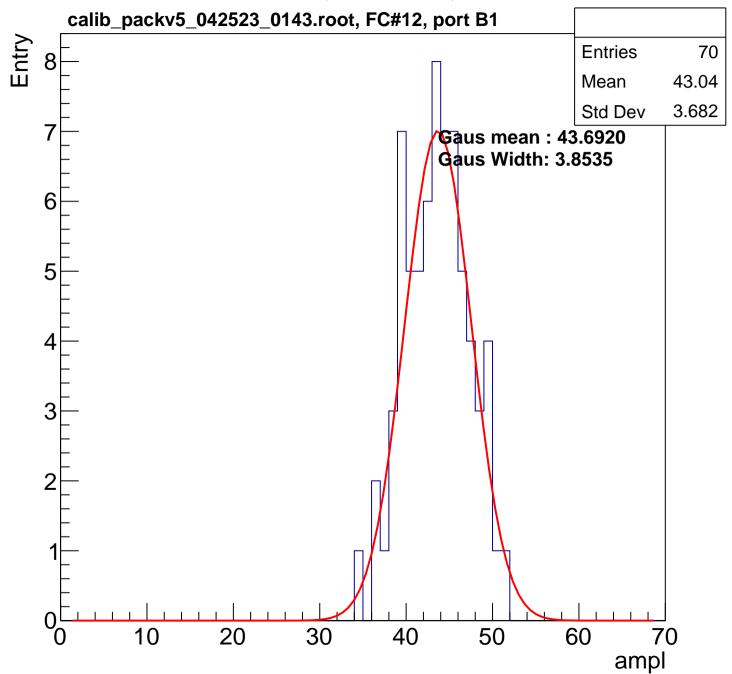


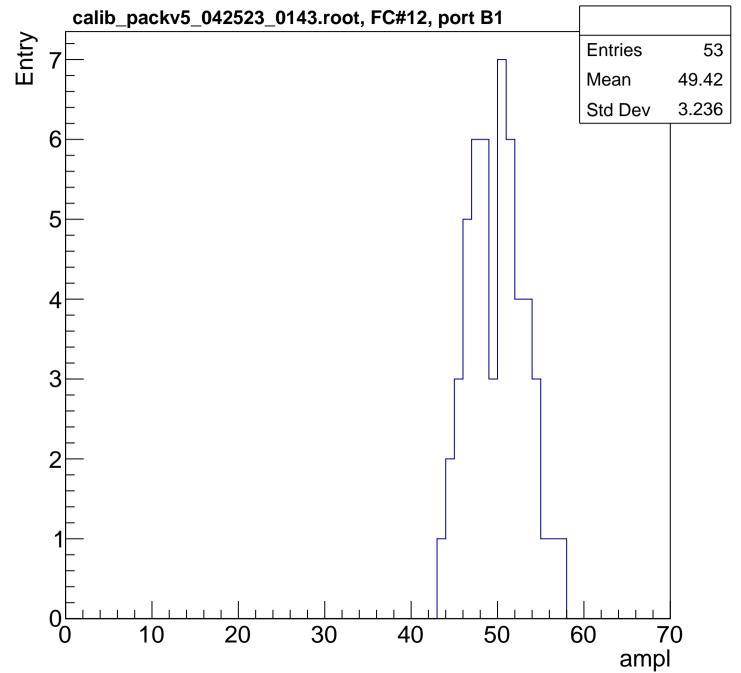
0

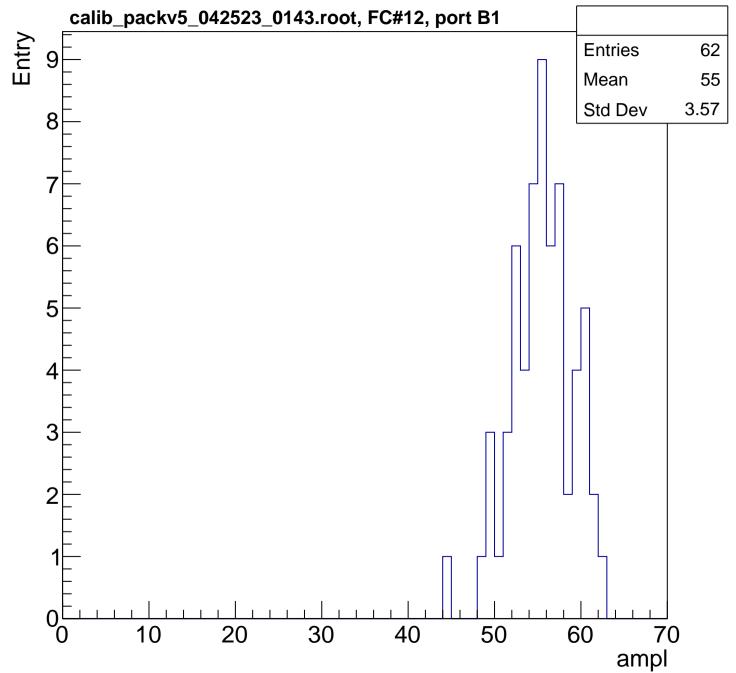


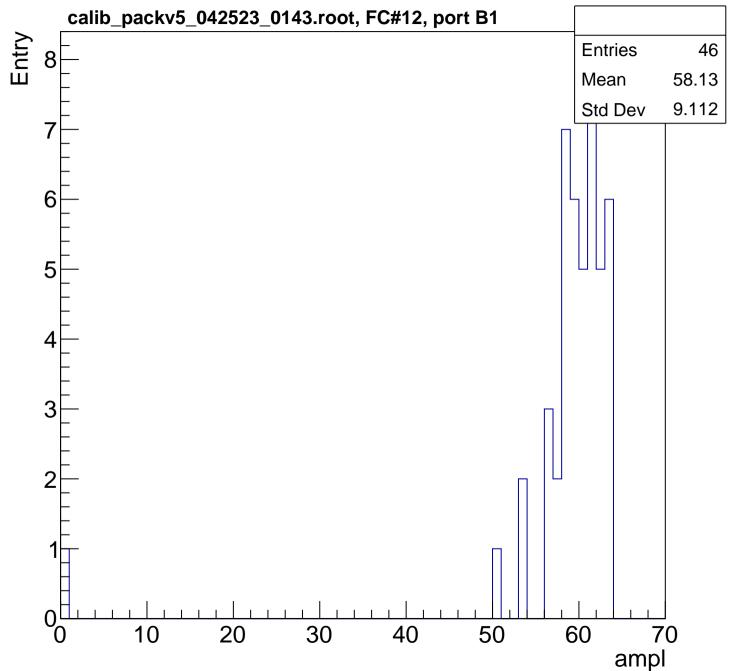


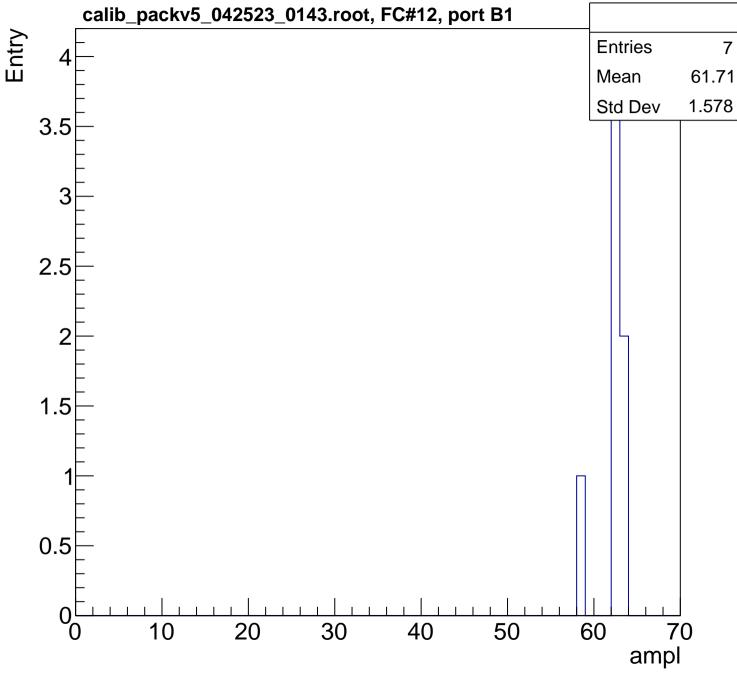


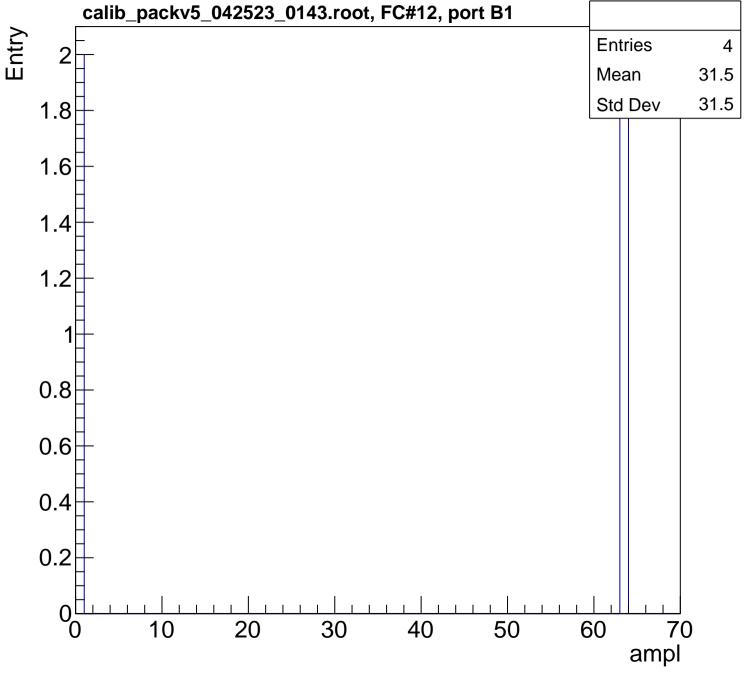


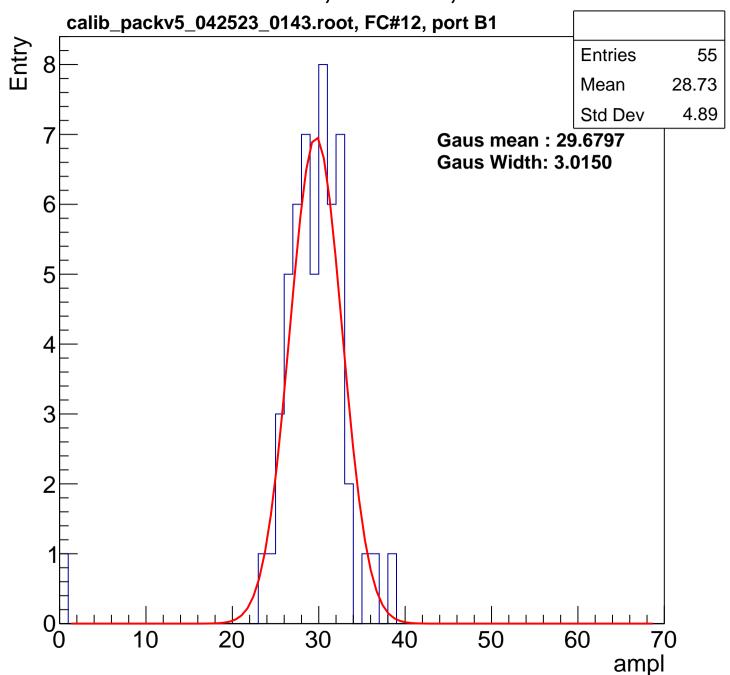


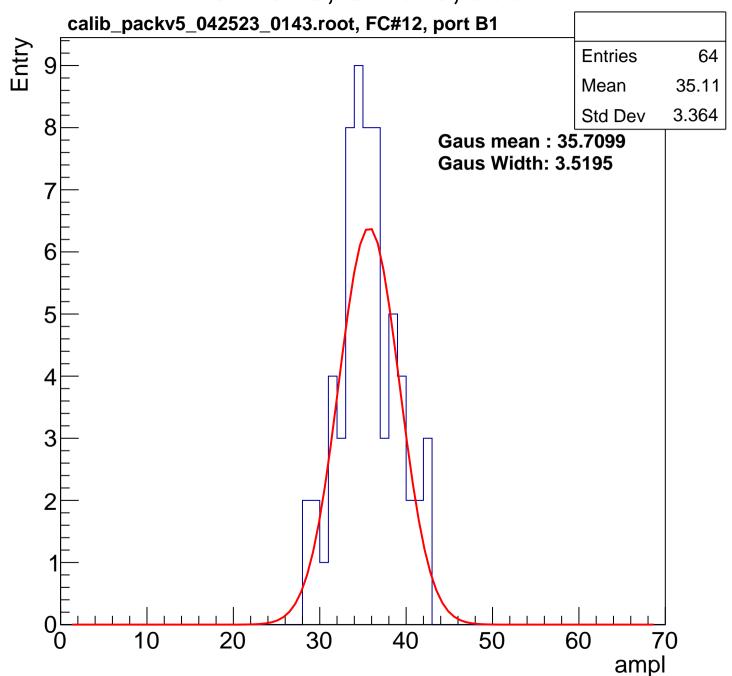


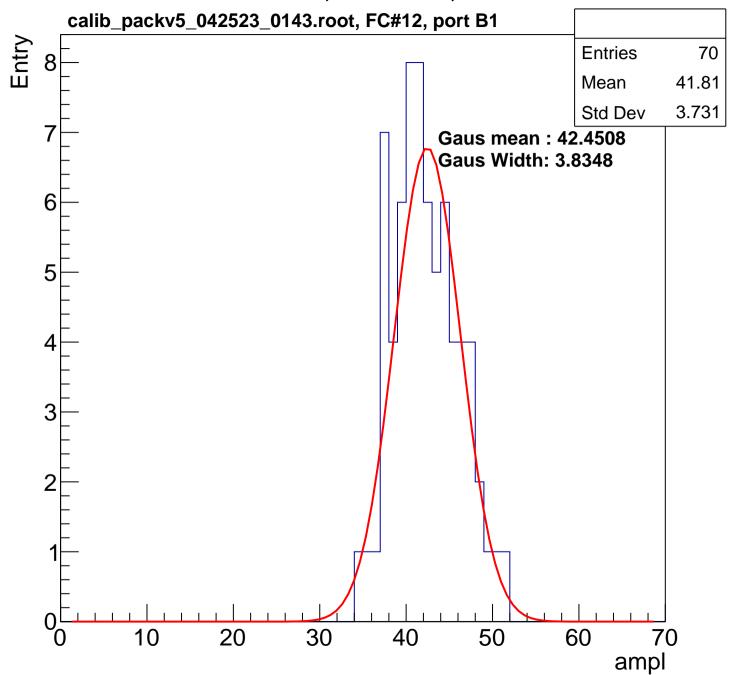


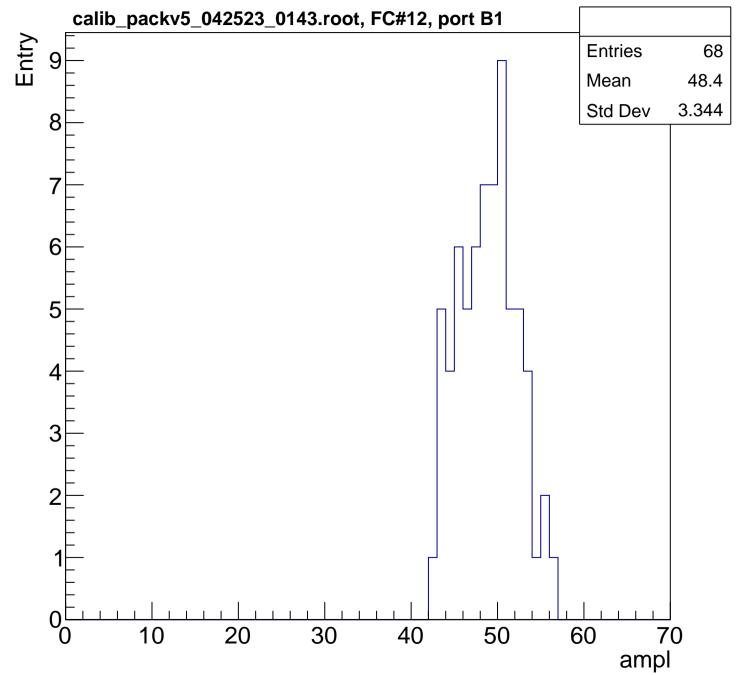


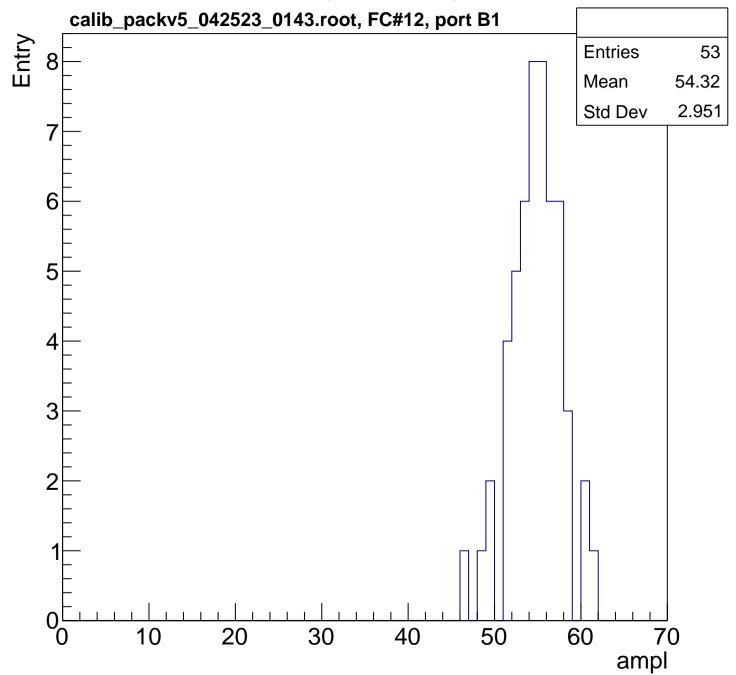


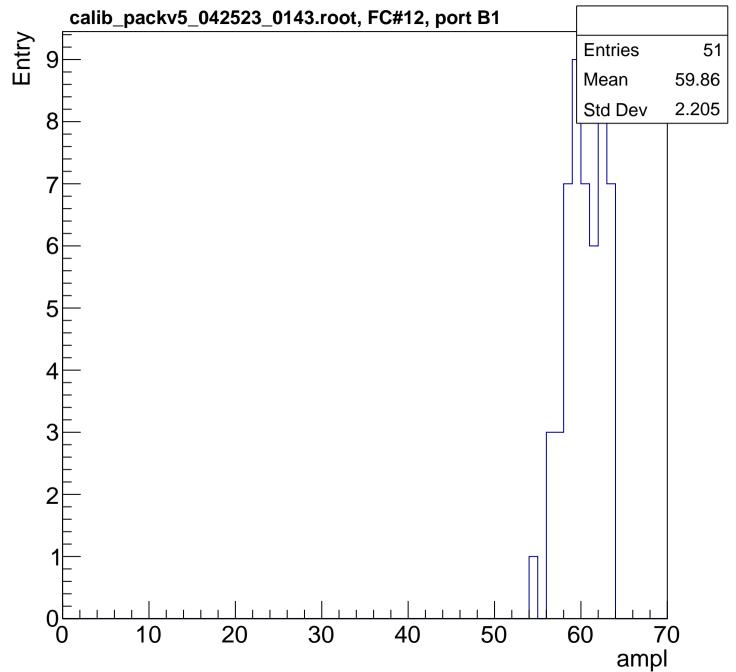


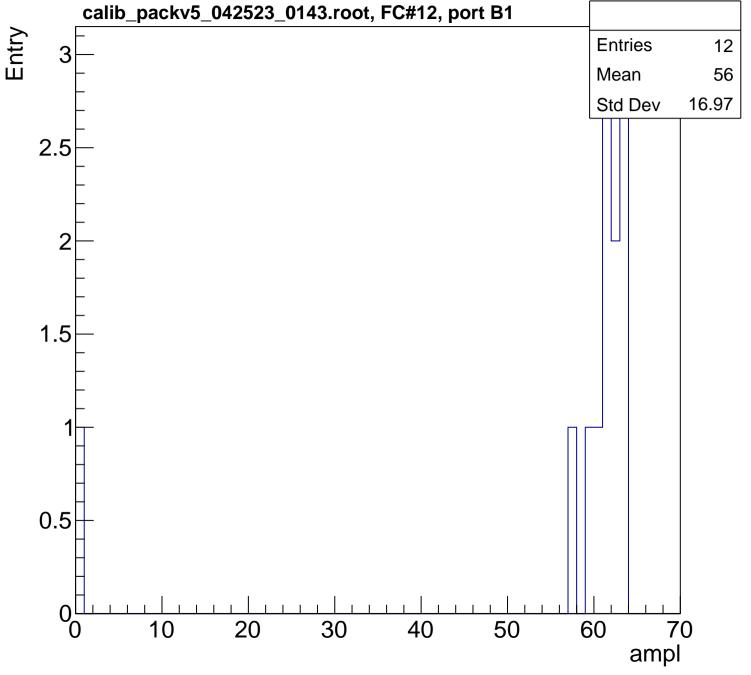




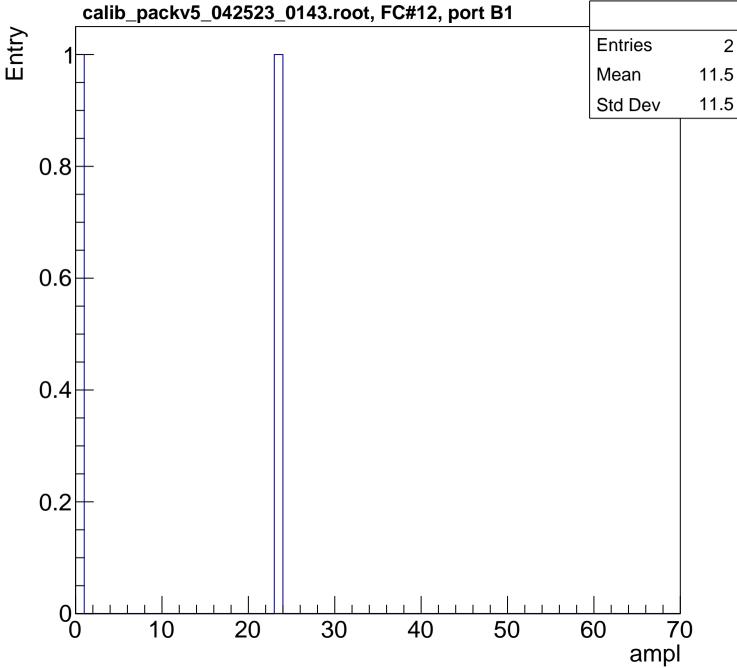


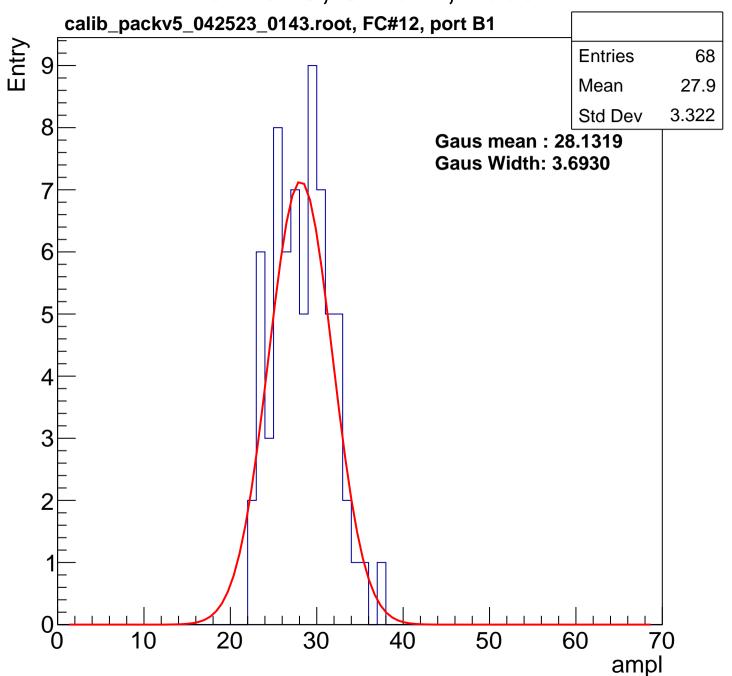


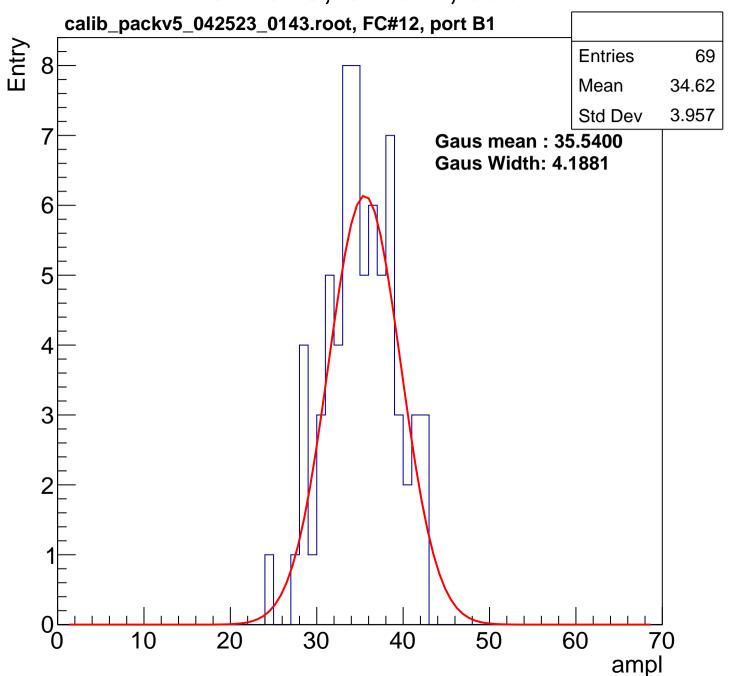


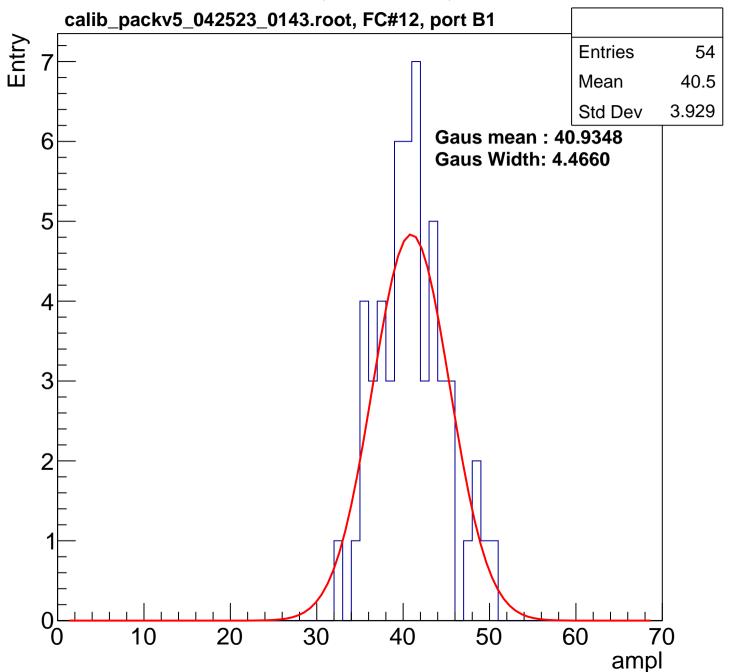


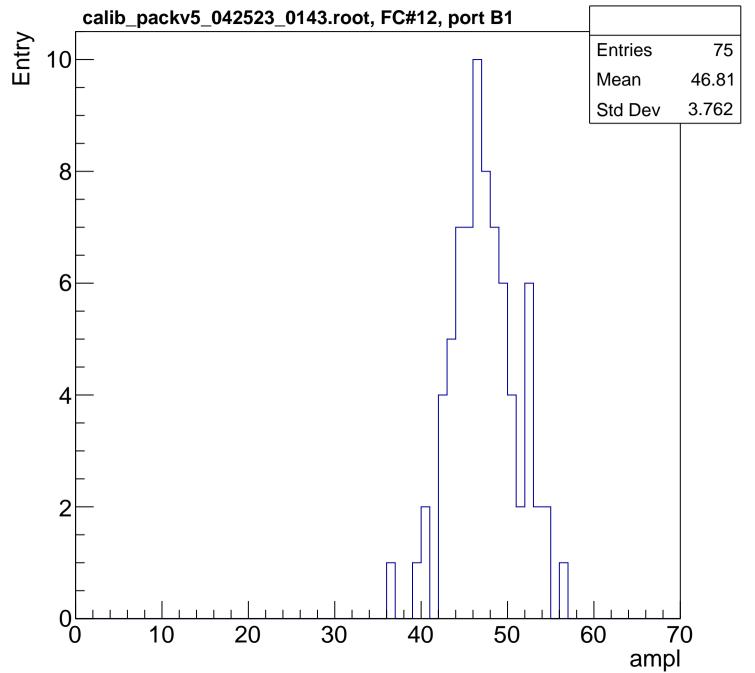
2

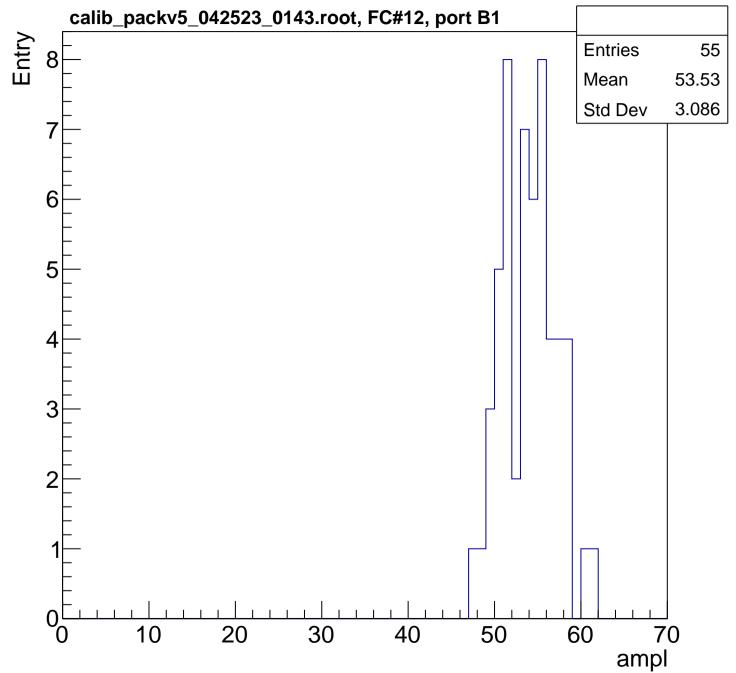


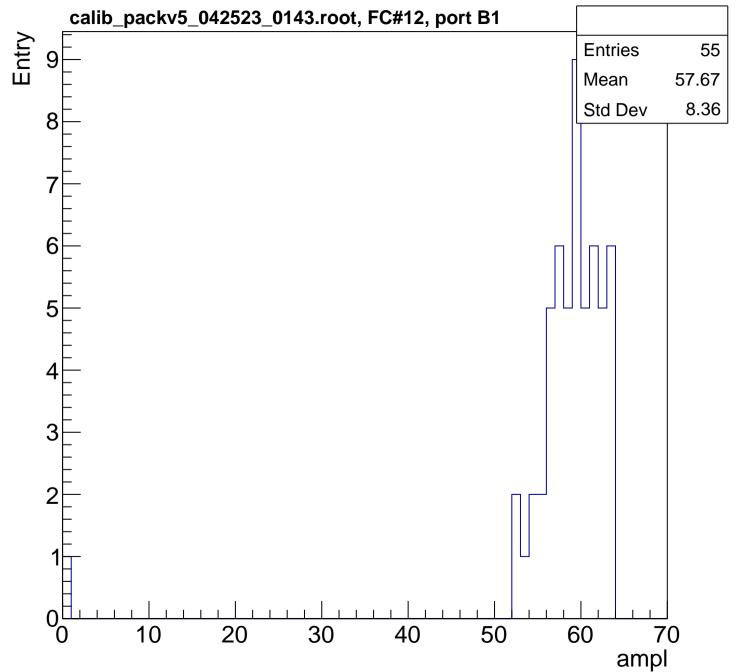


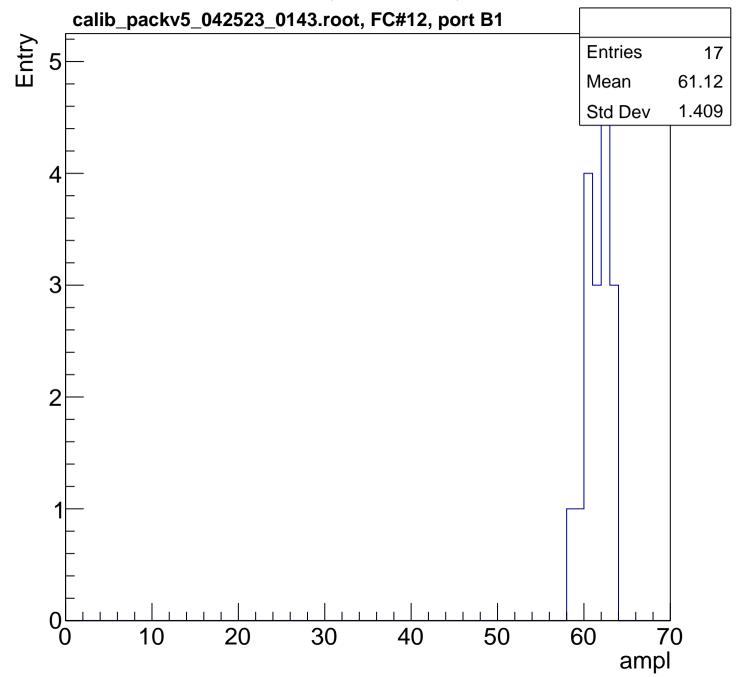


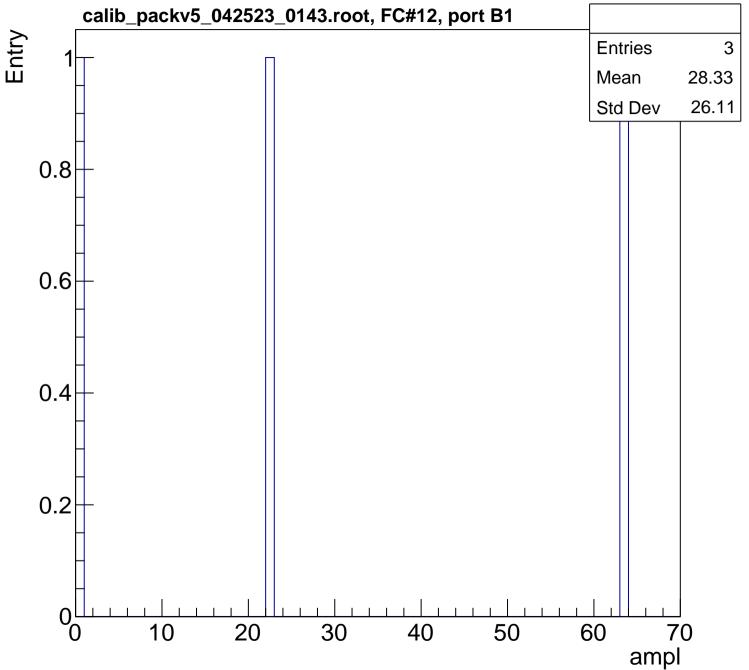


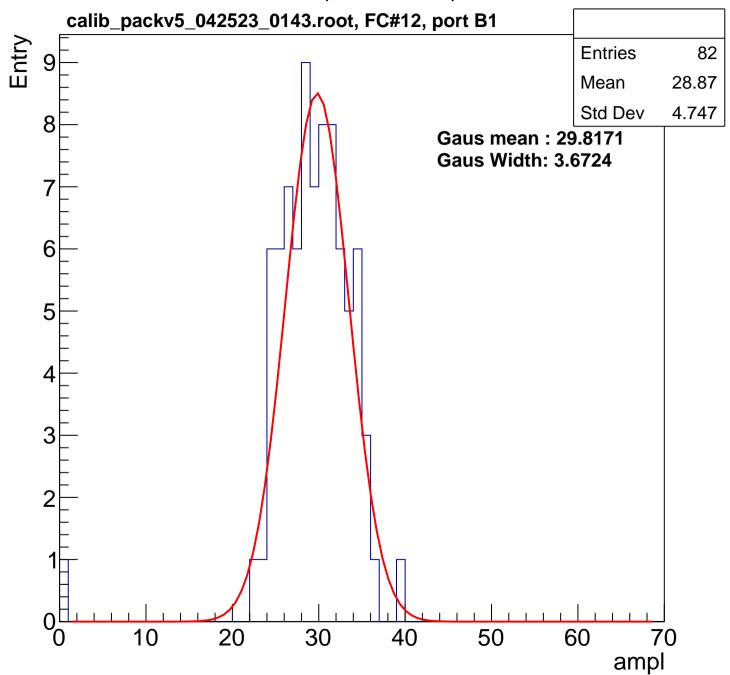


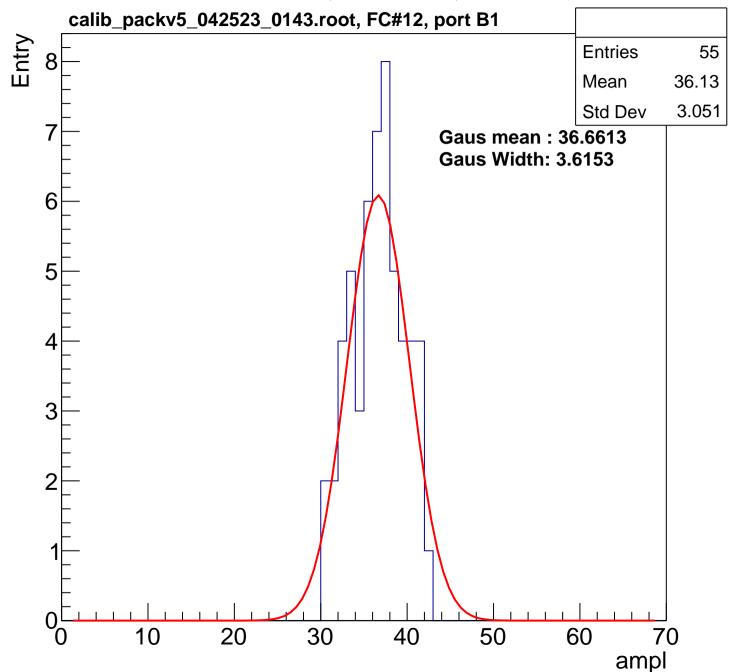


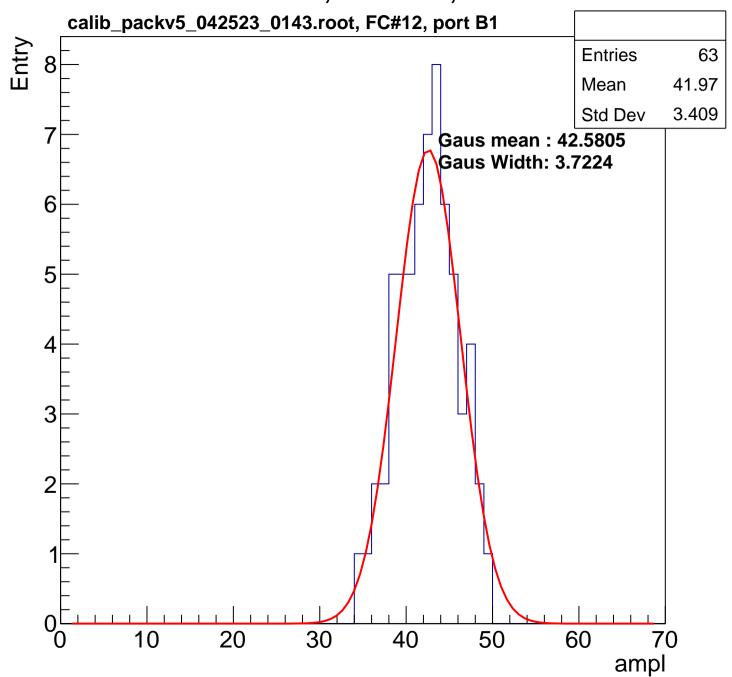


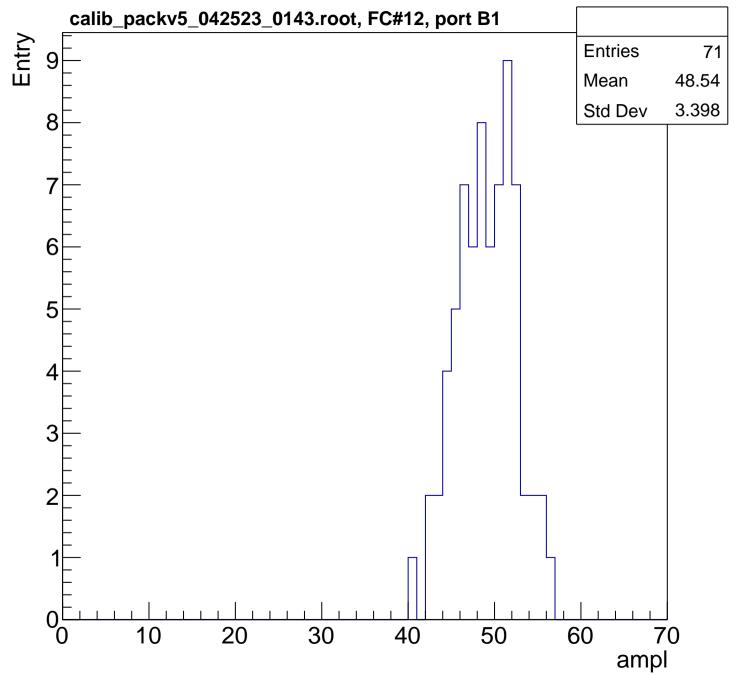


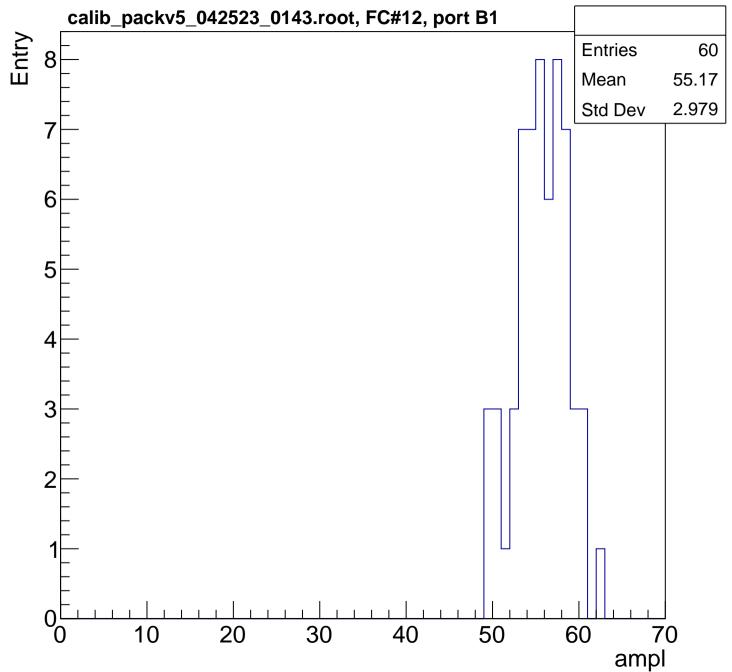


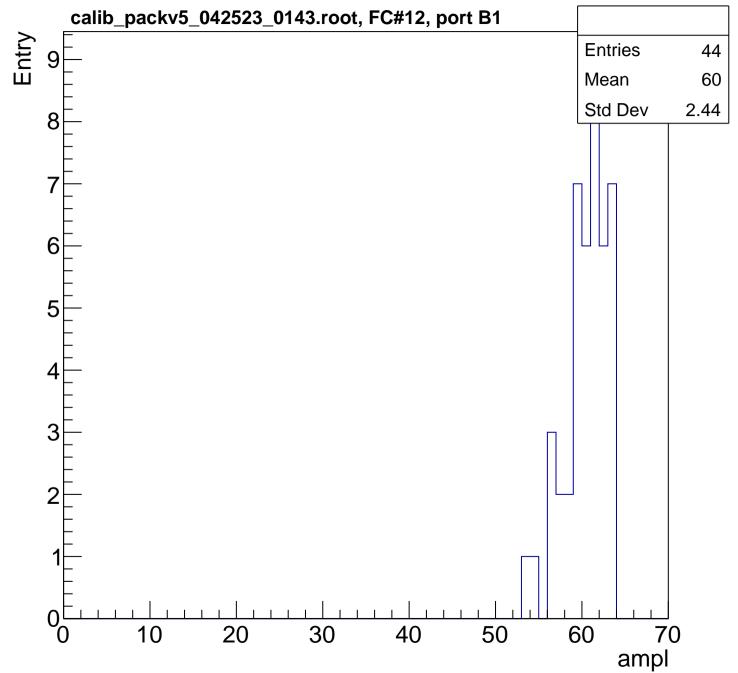


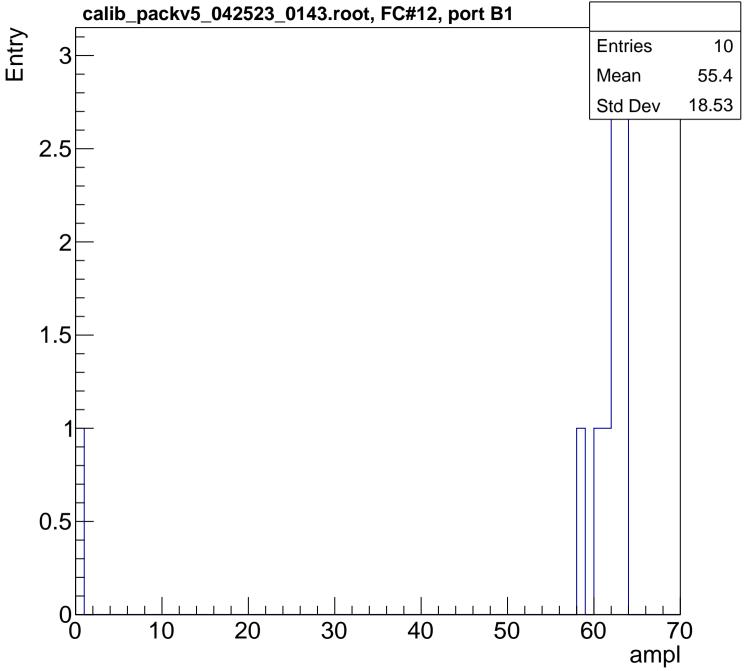


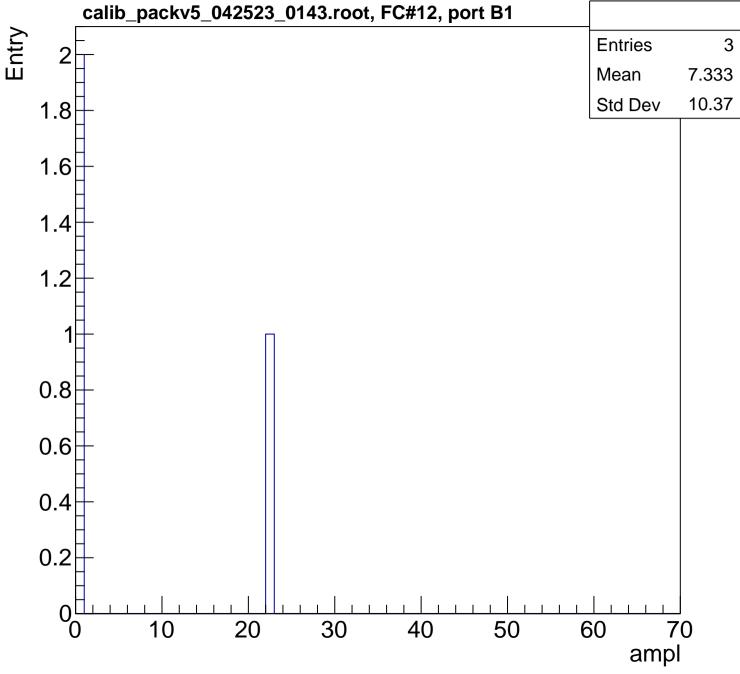


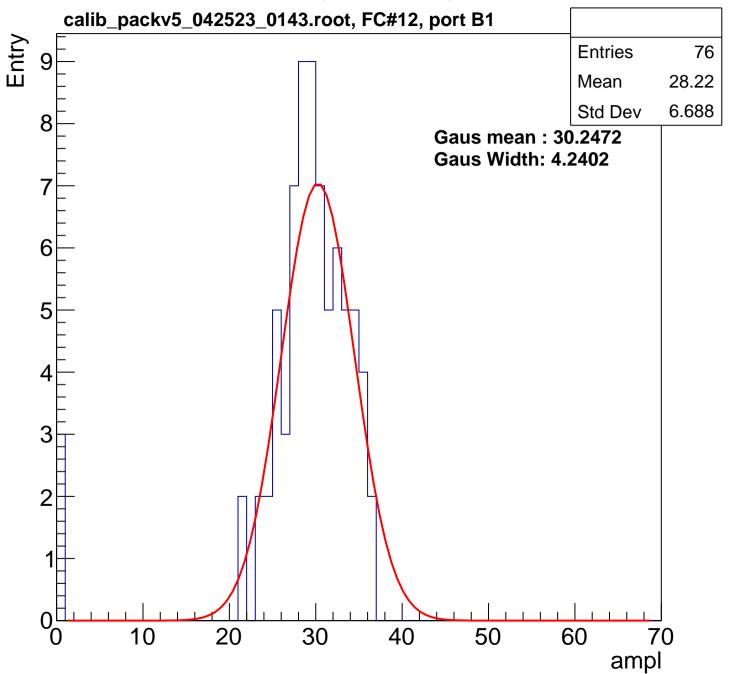


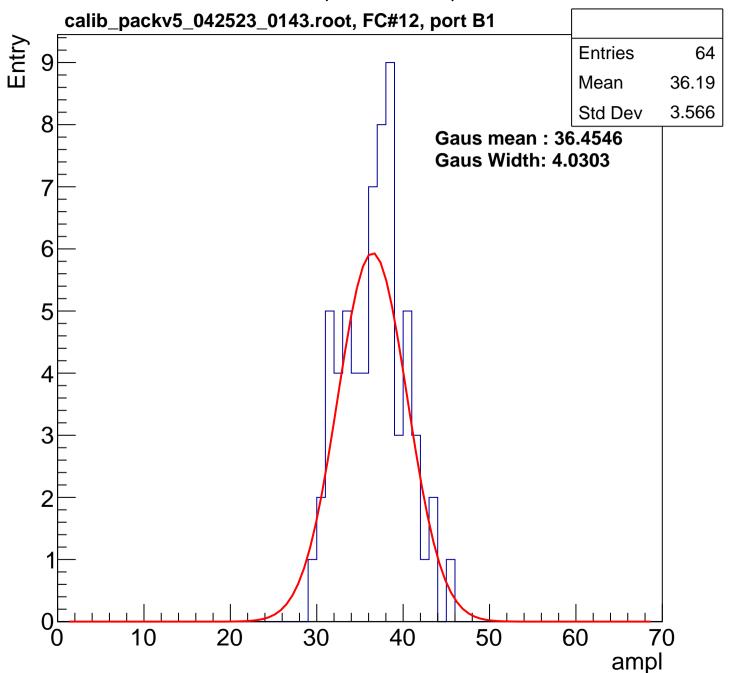


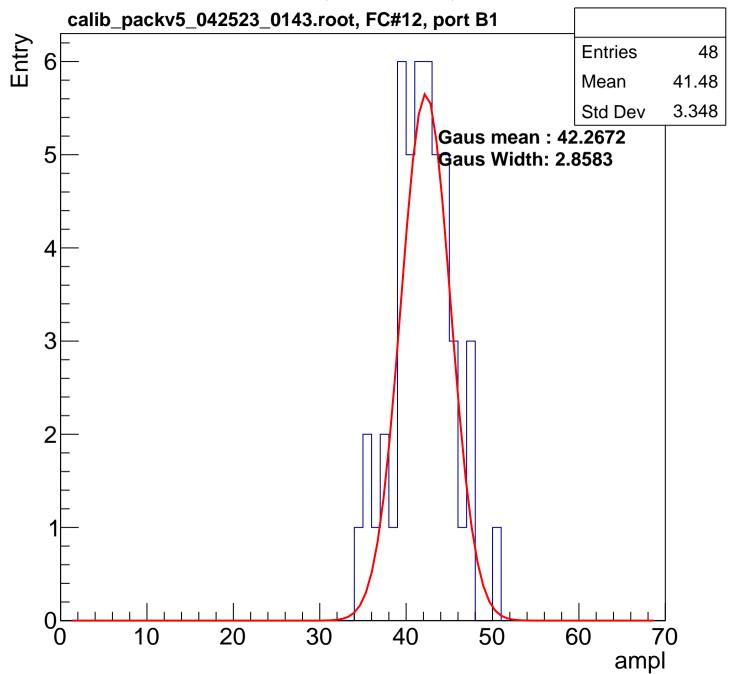


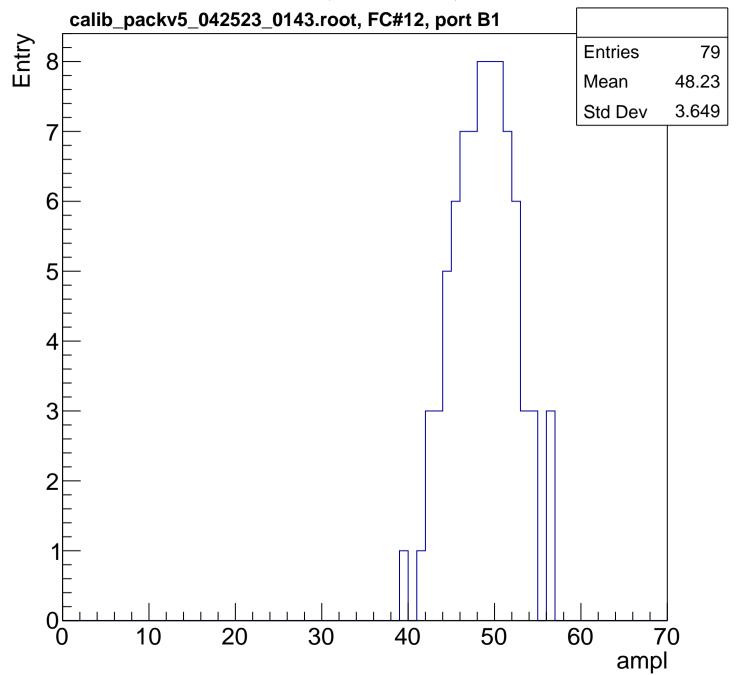


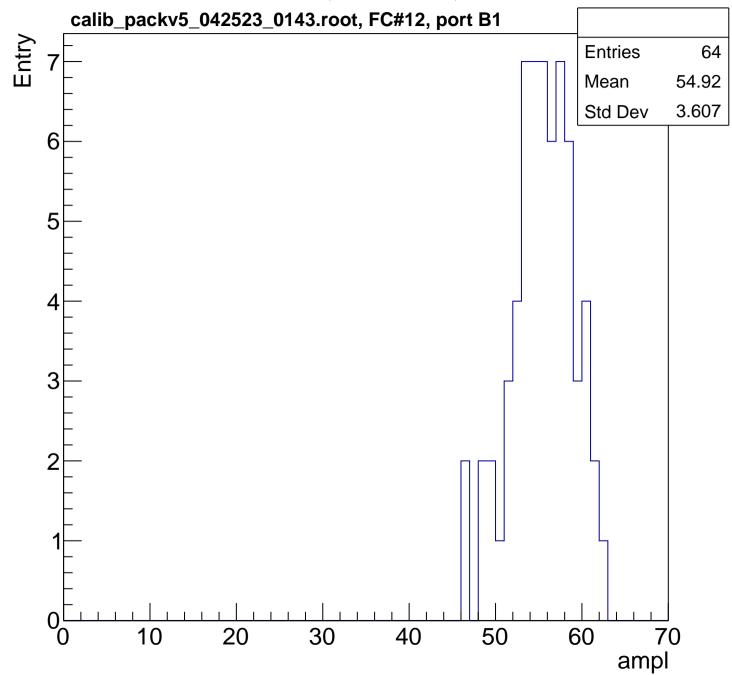


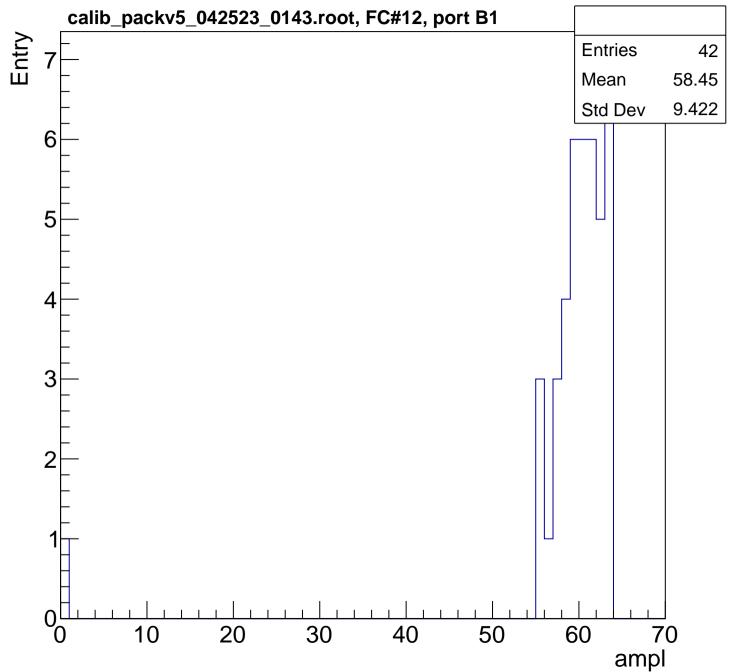


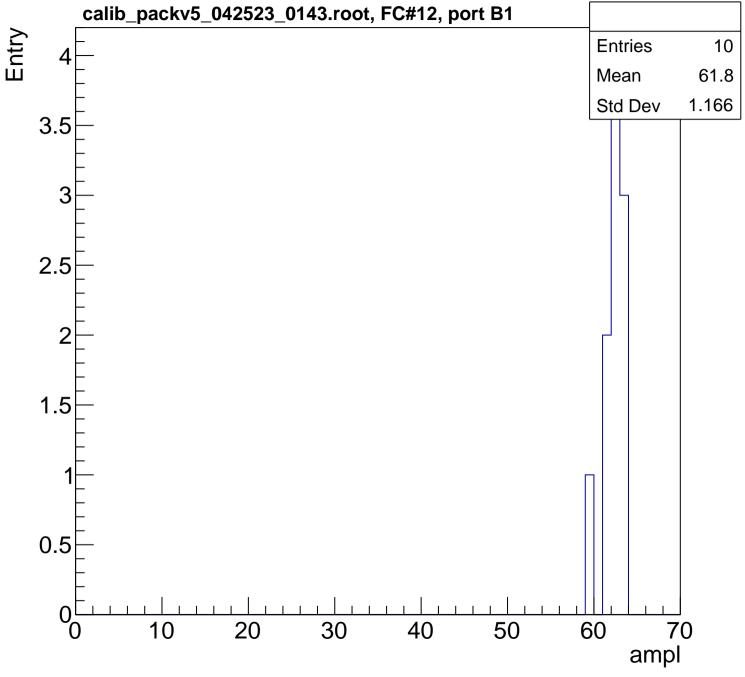




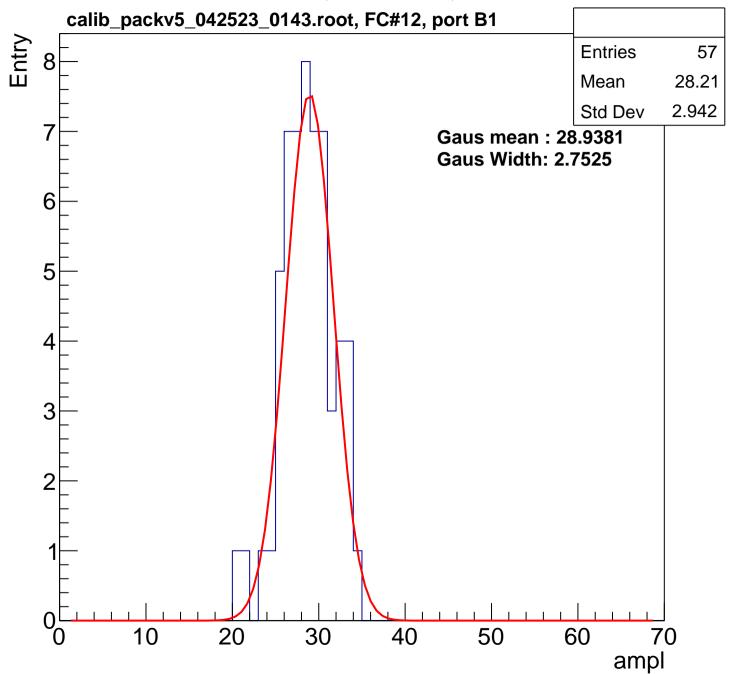


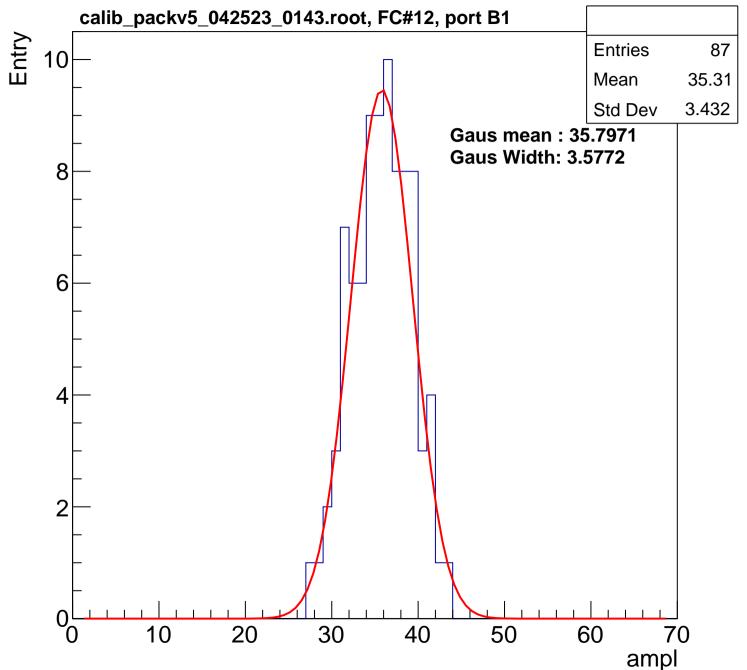


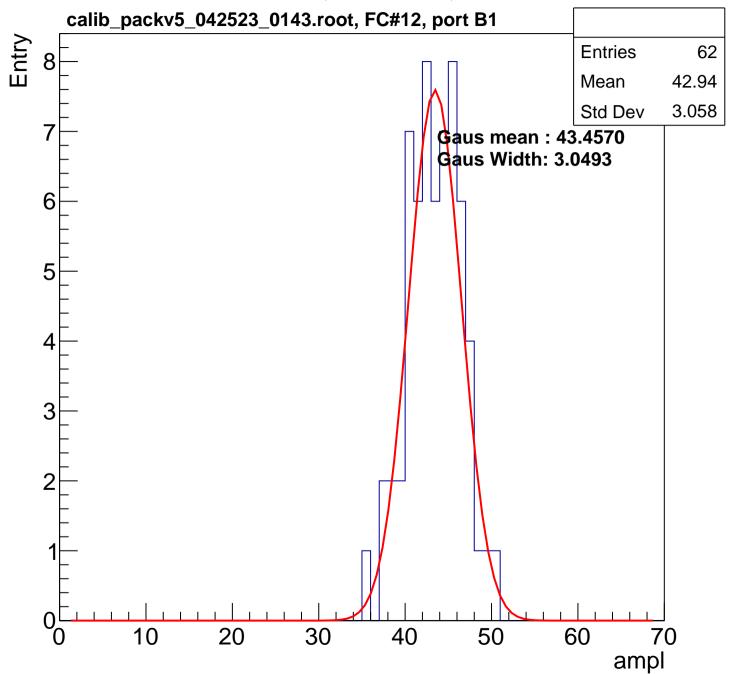


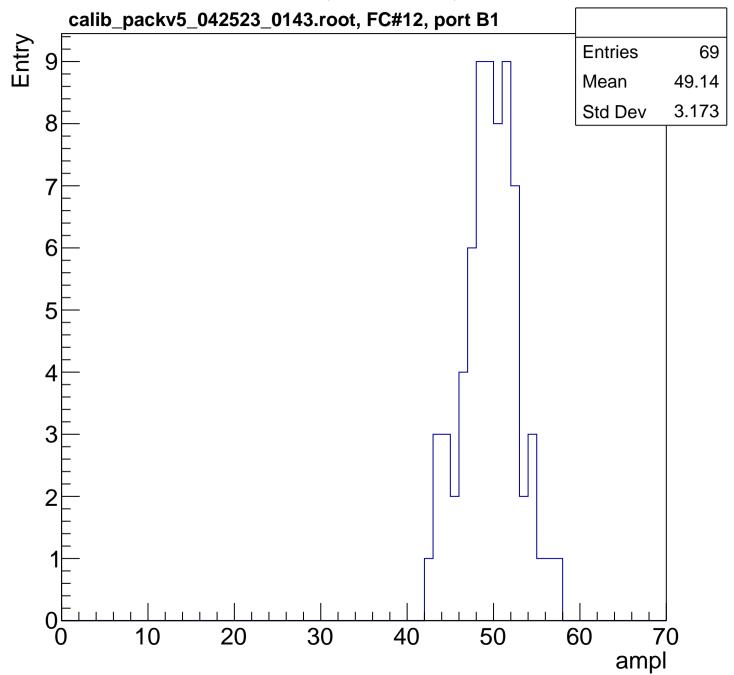


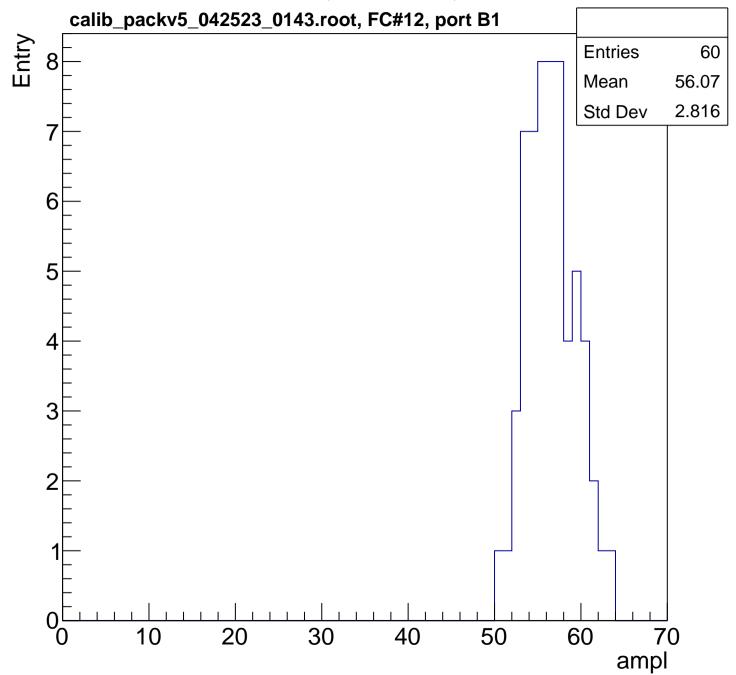
B0L102S, U7-ch6, adc7 calib_packv5_042523_0143.root, FC#12, port B1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

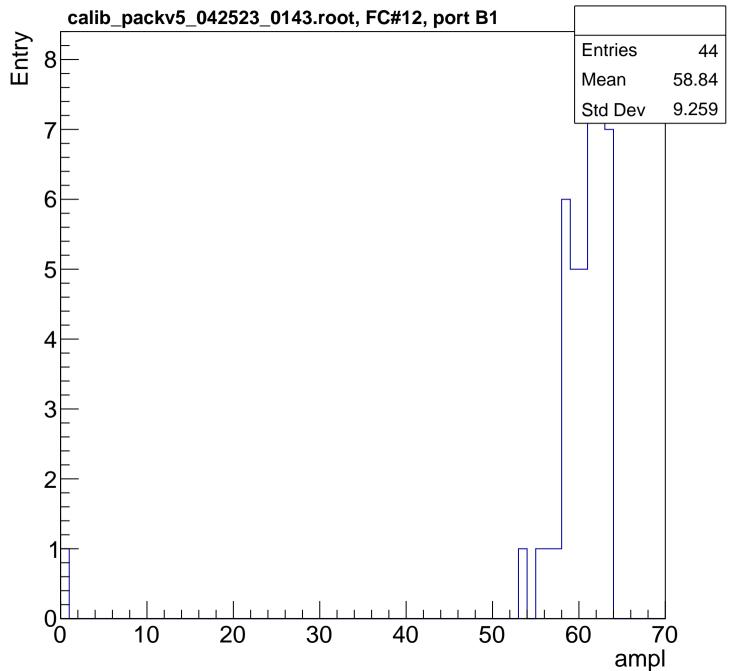


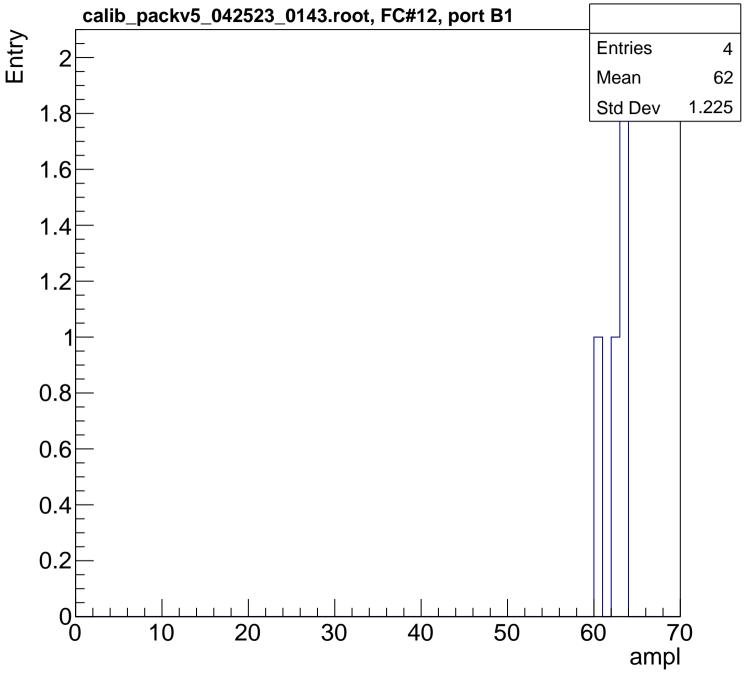


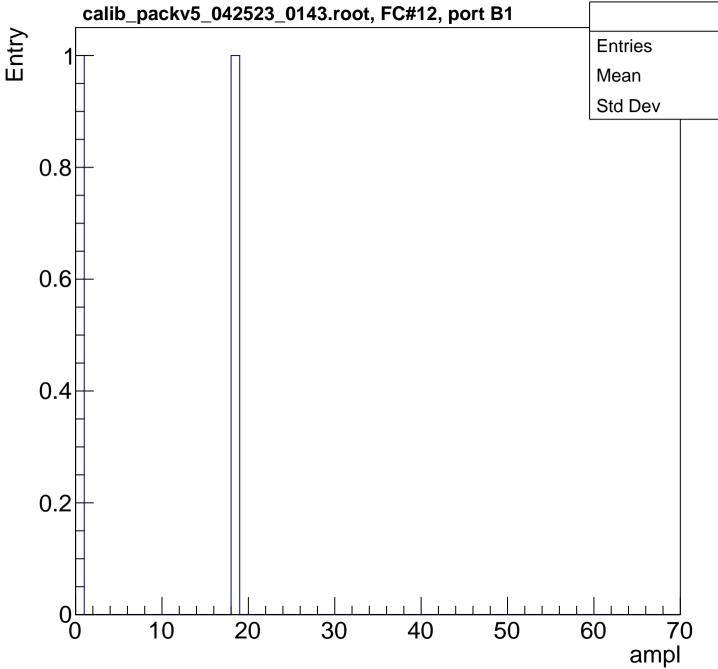


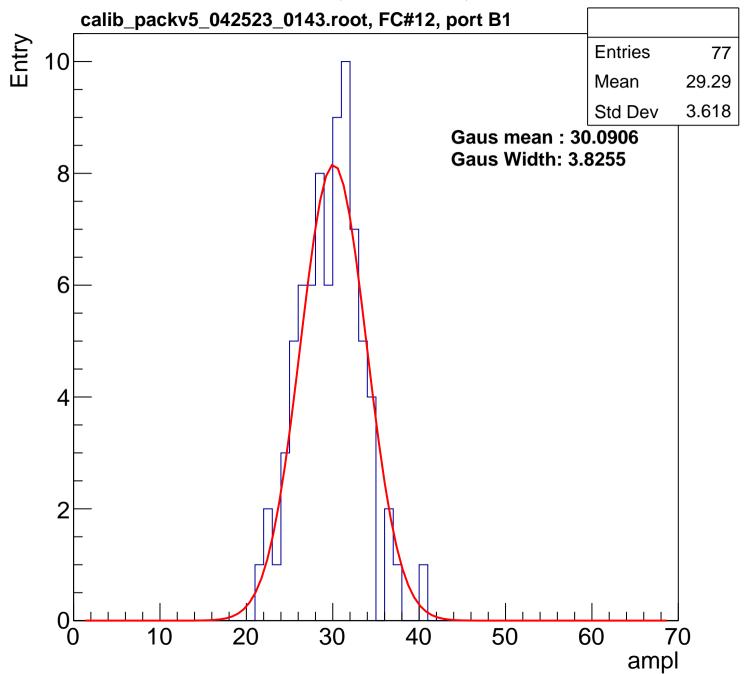


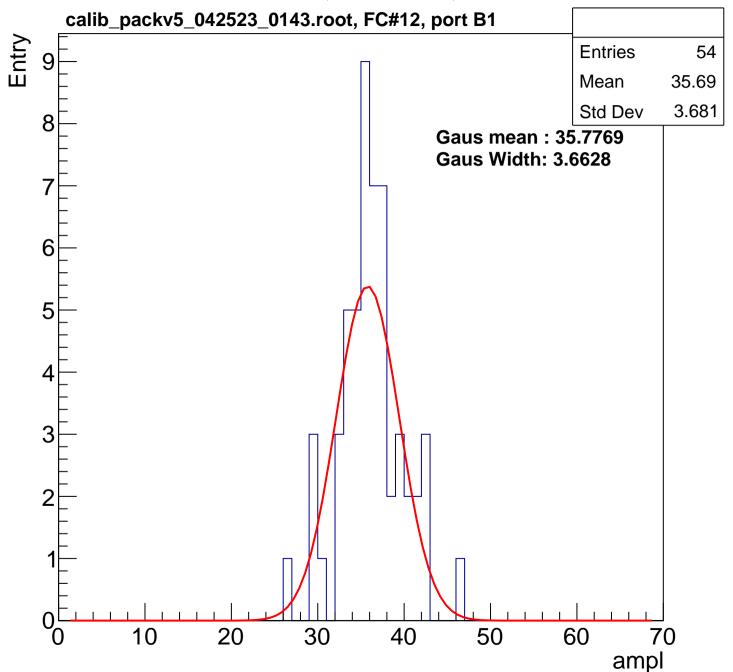


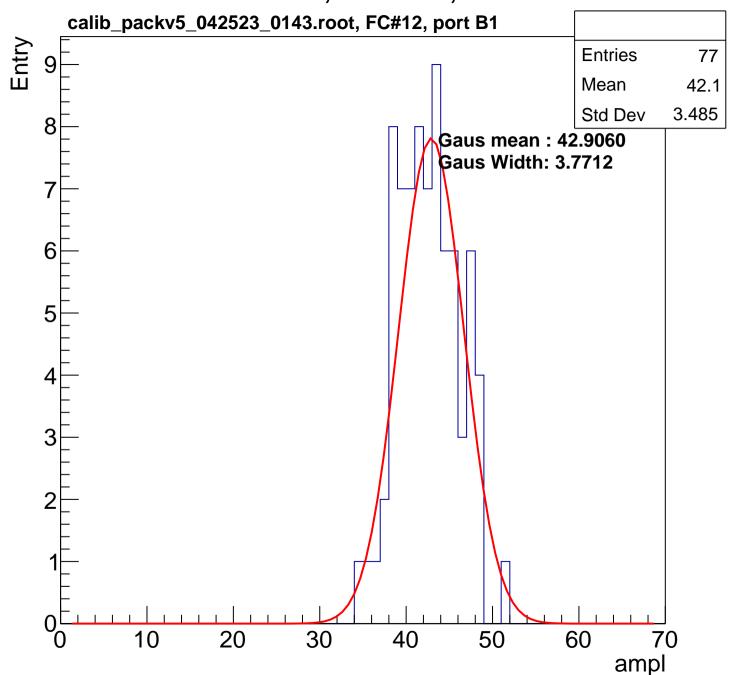


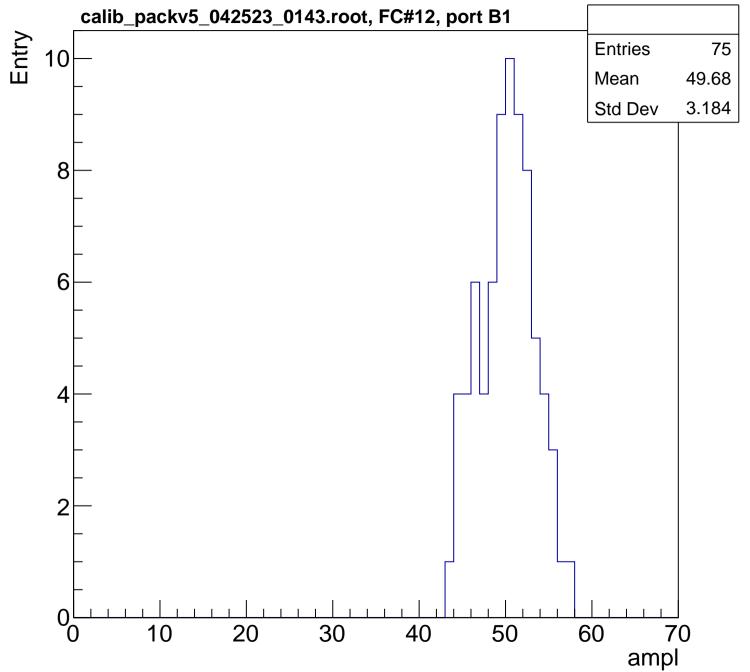


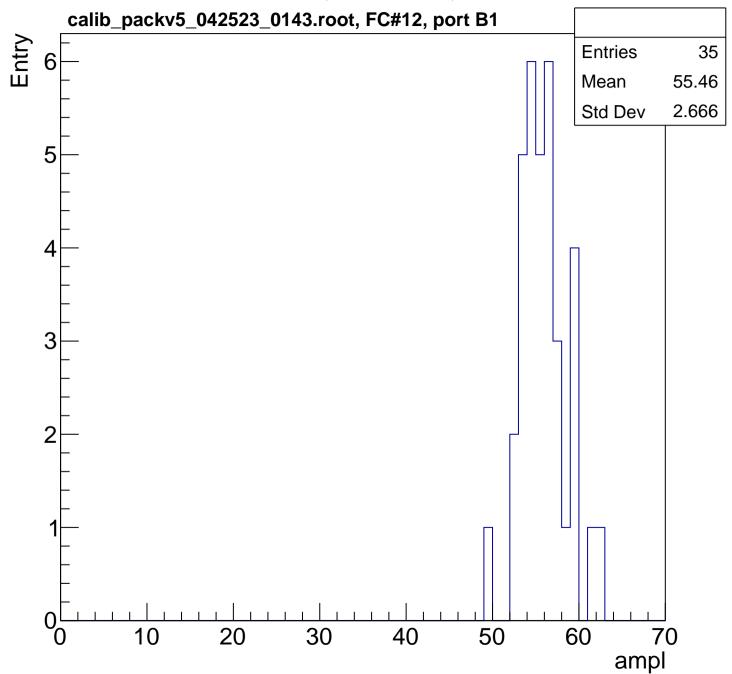


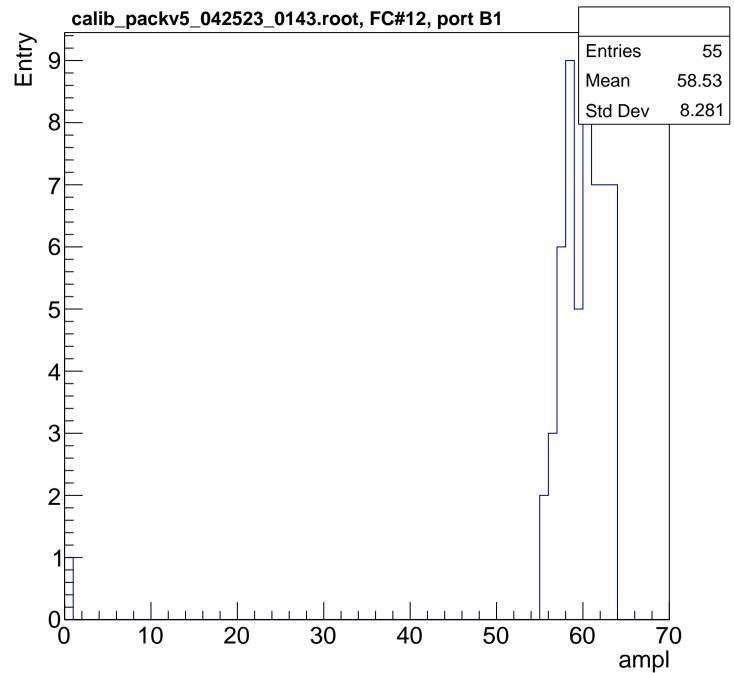


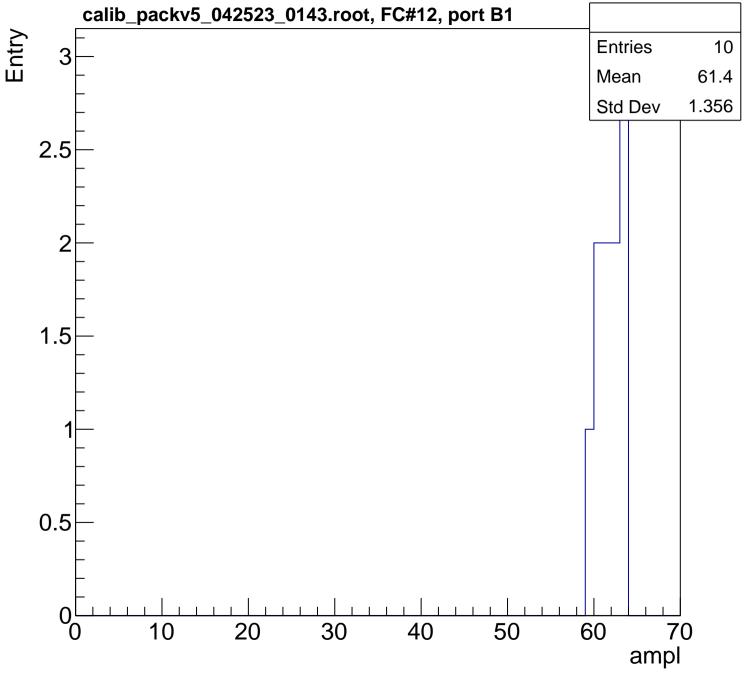


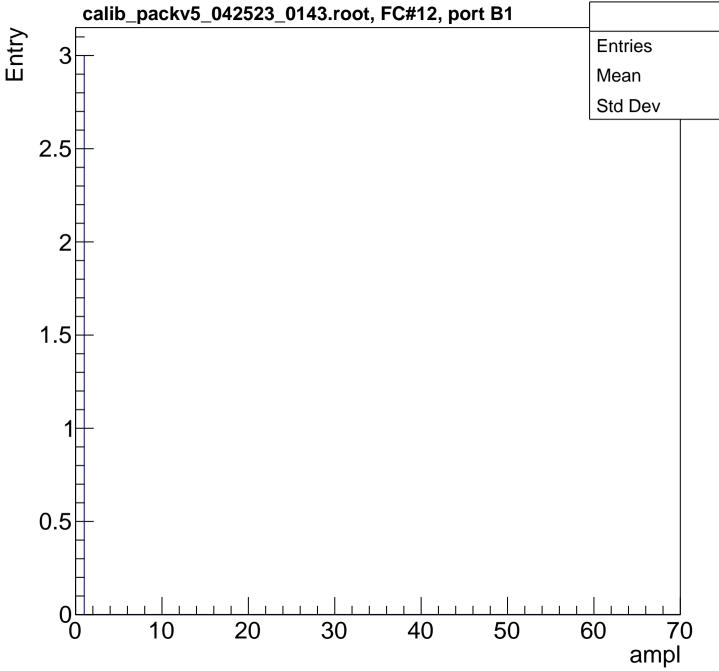


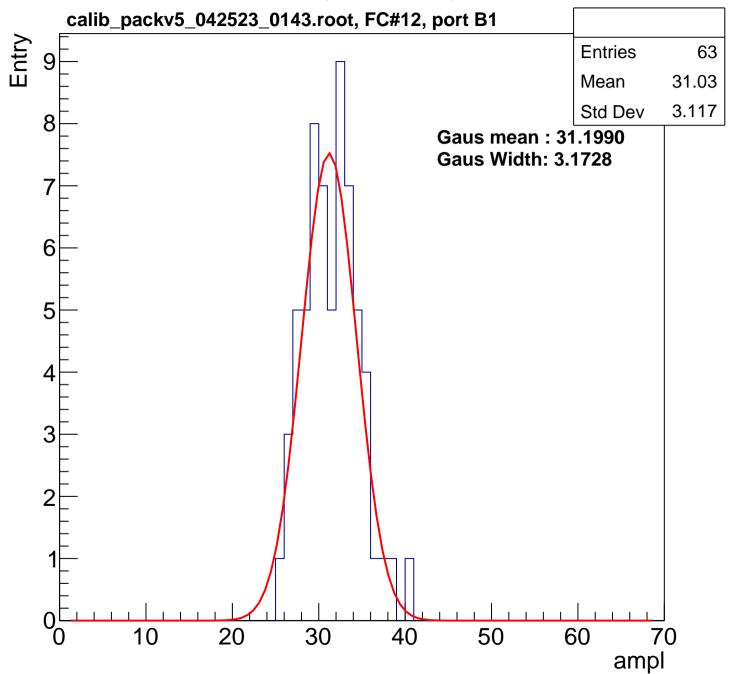


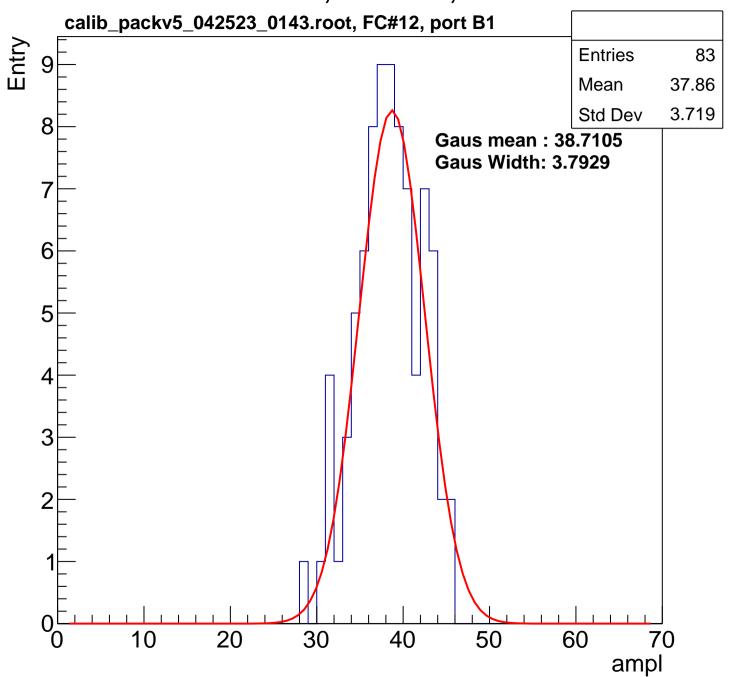


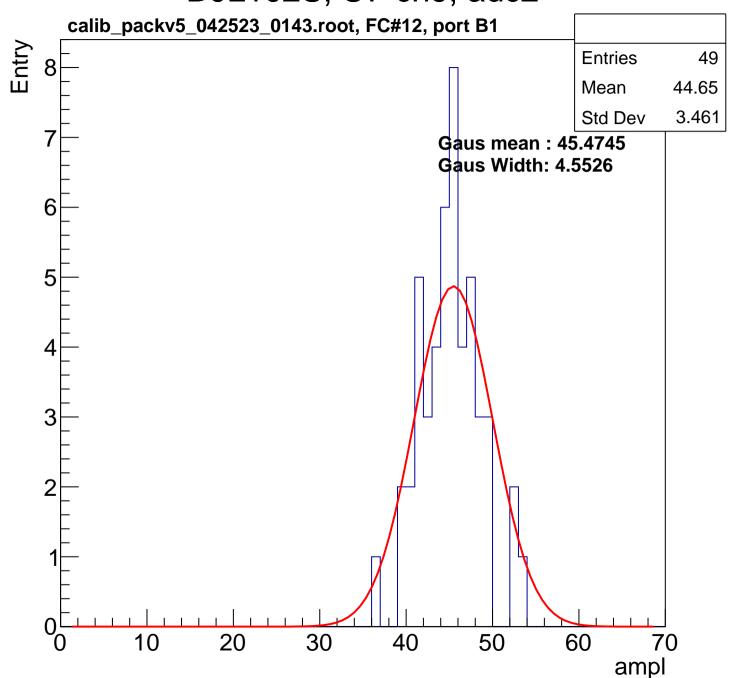


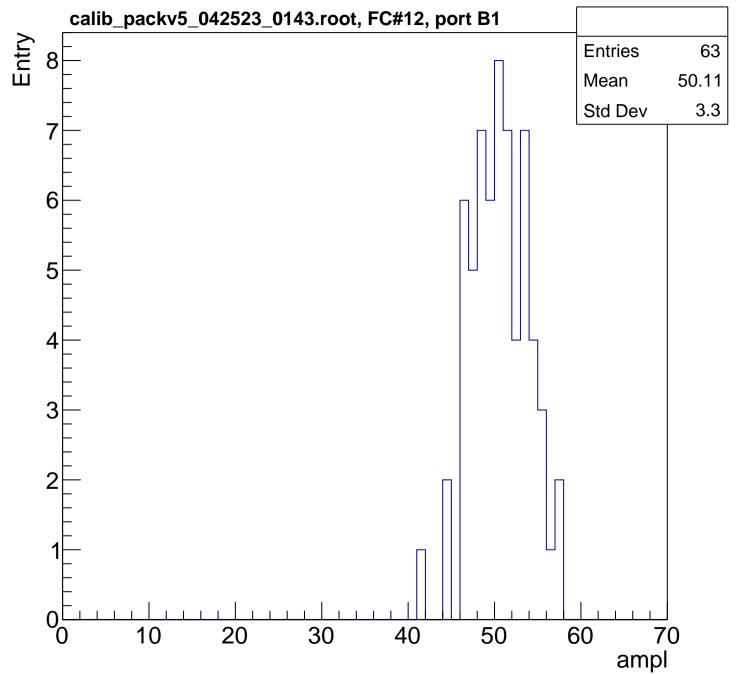


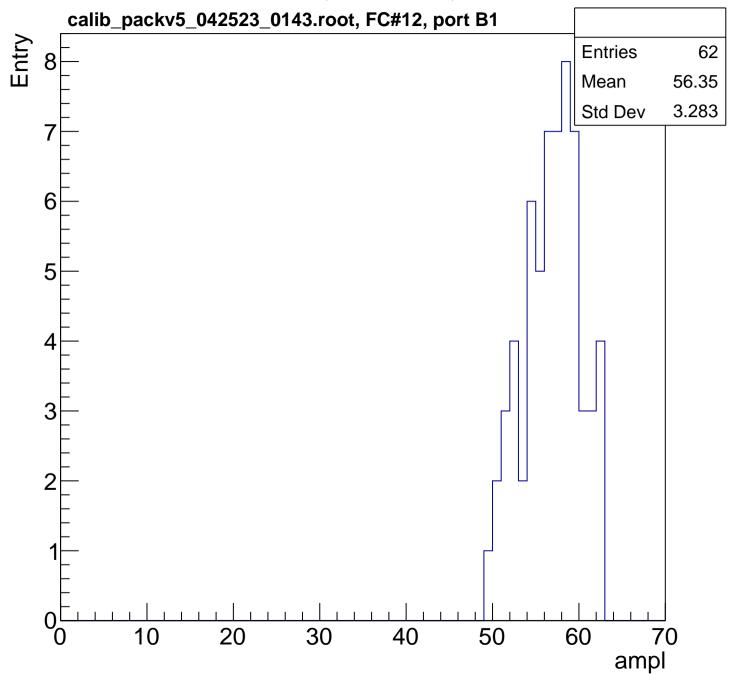


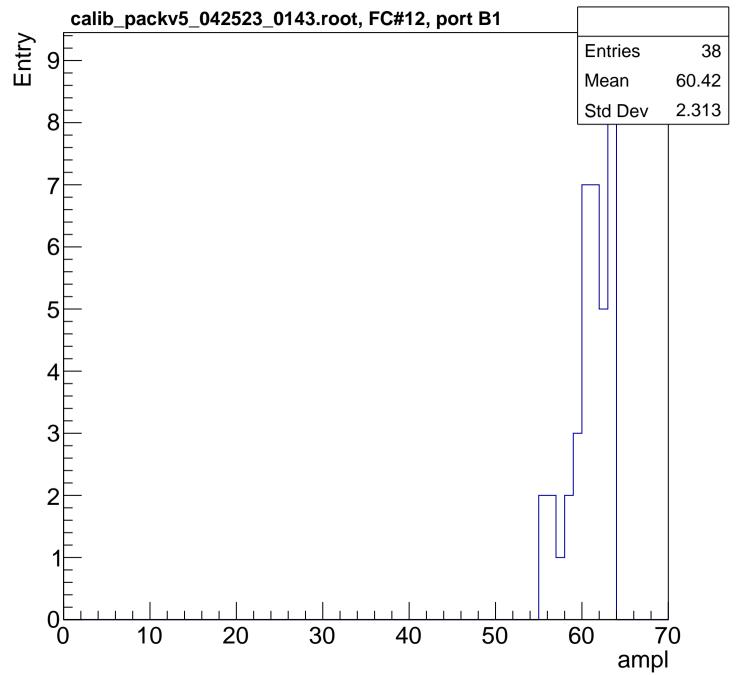


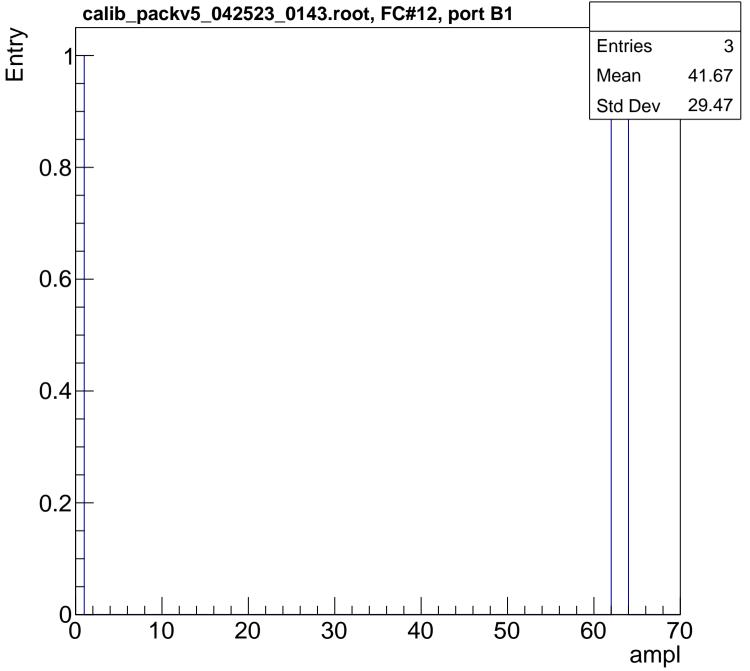




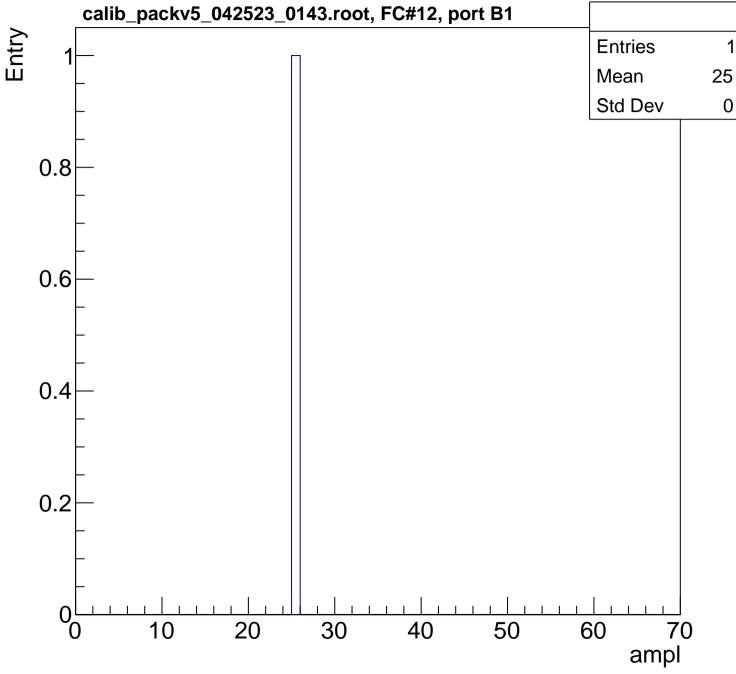


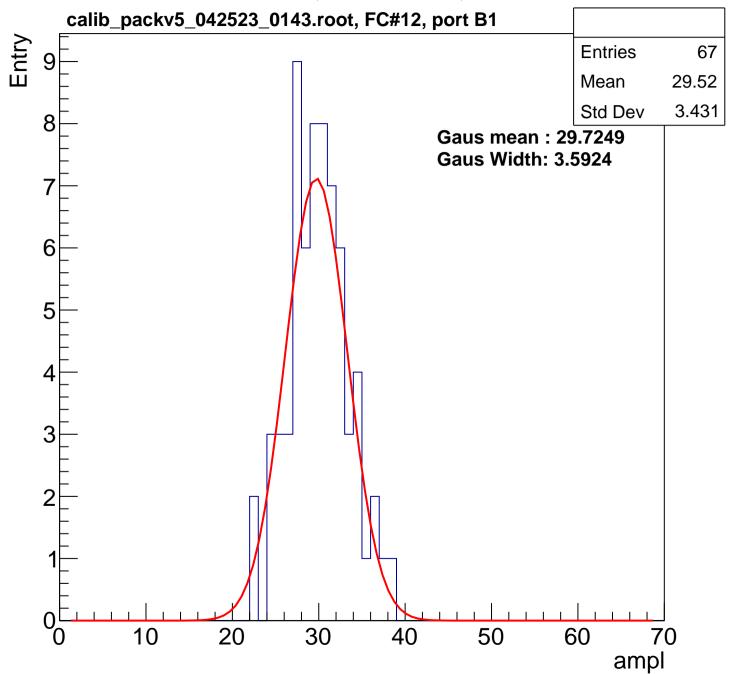


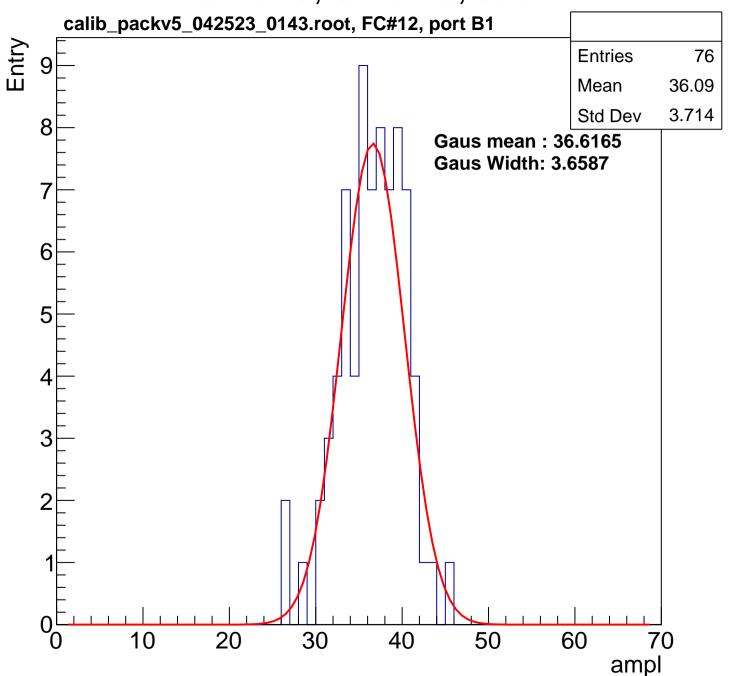


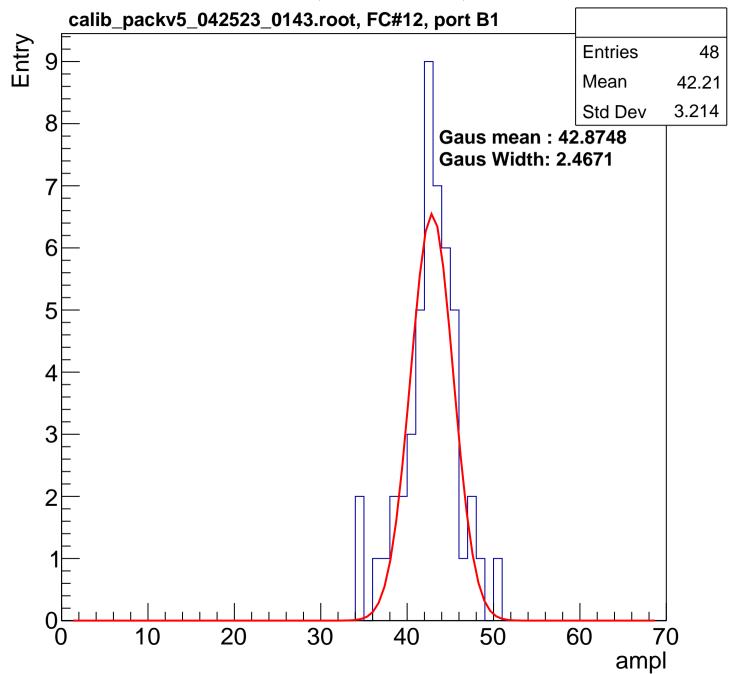


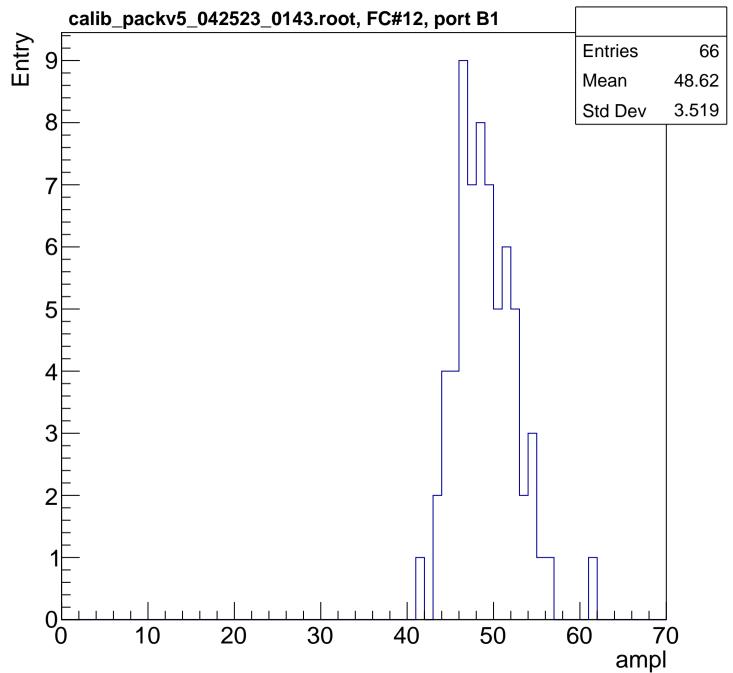
0

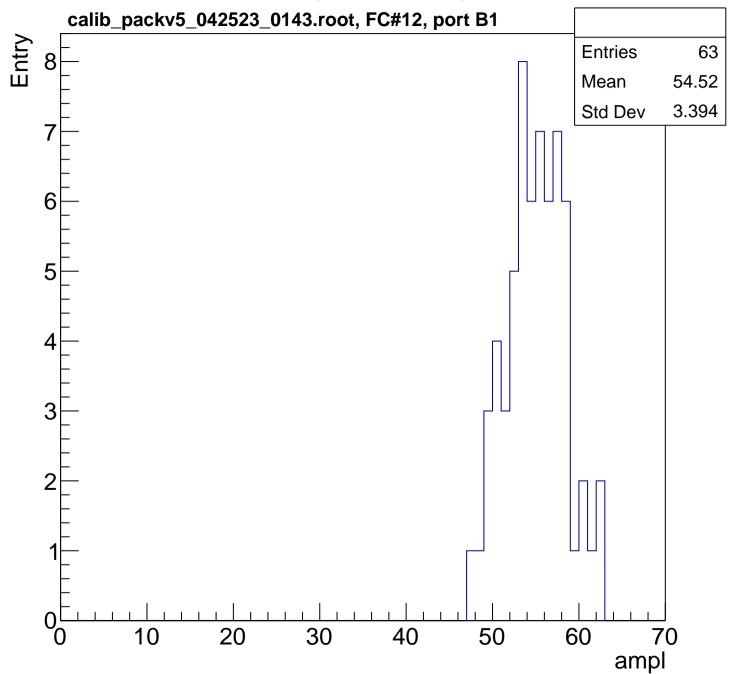


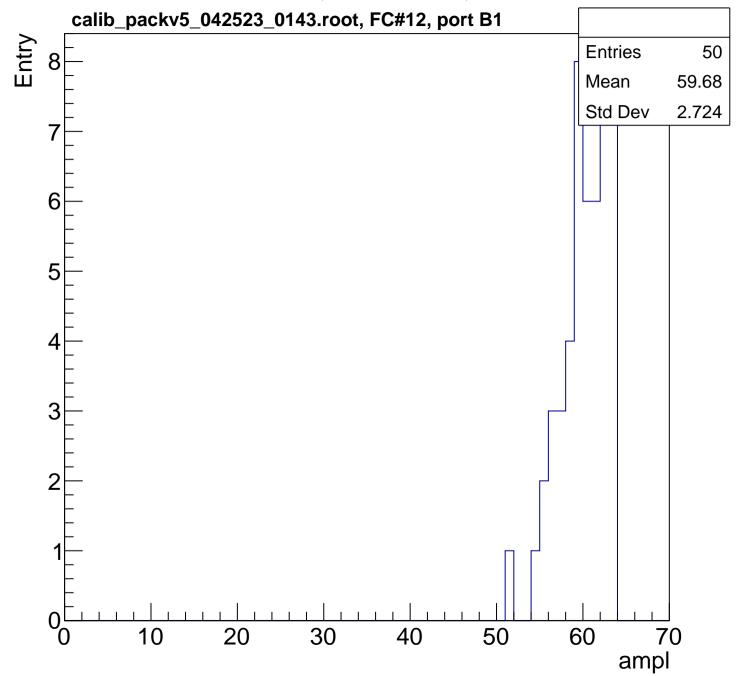


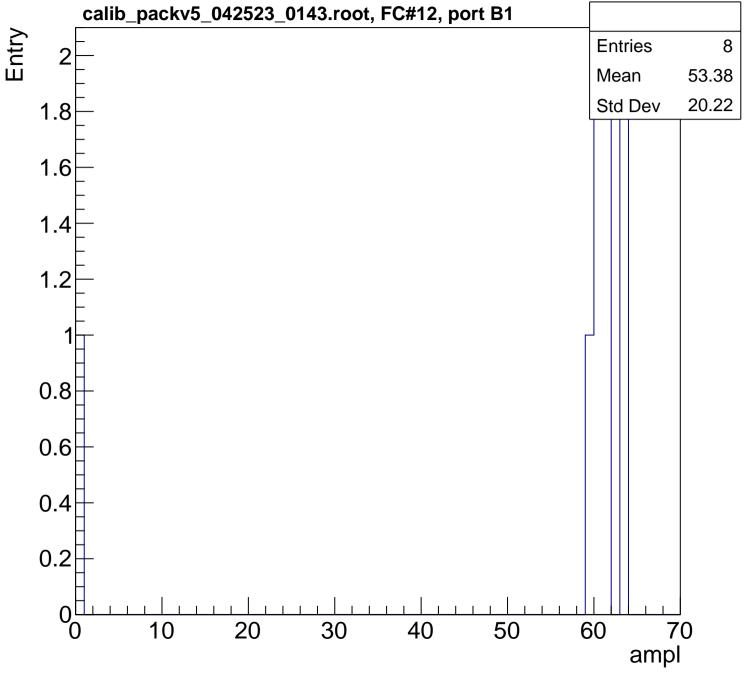


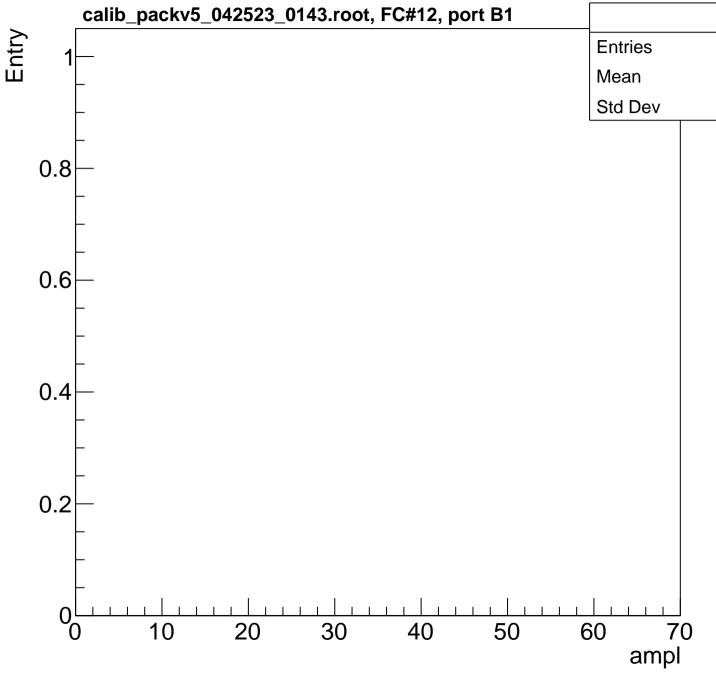


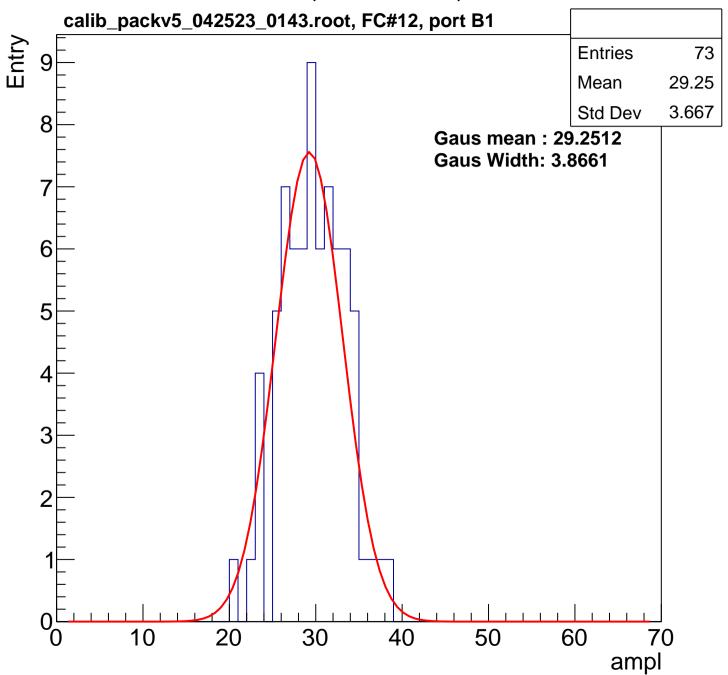


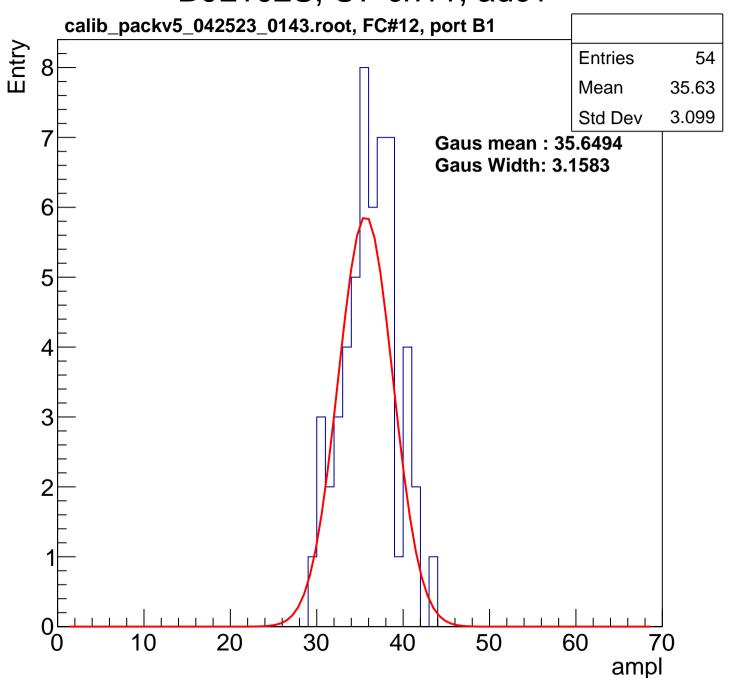


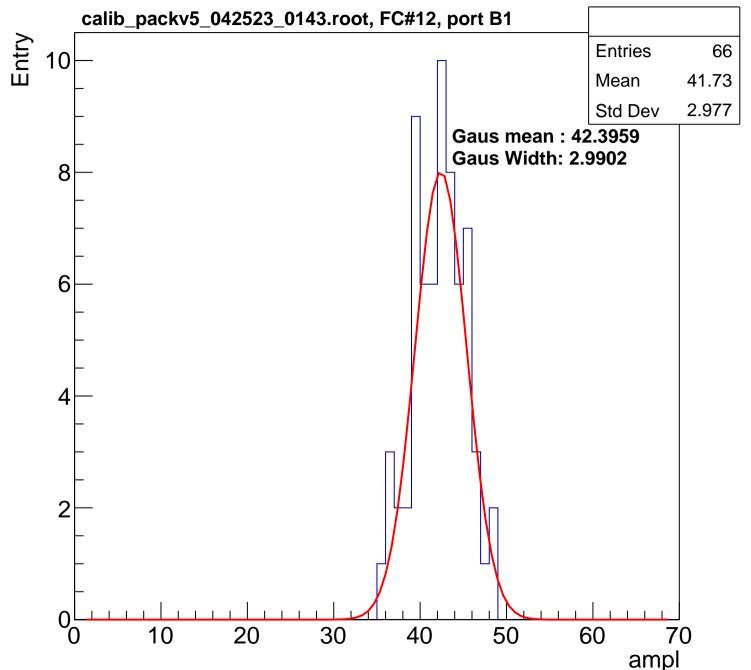


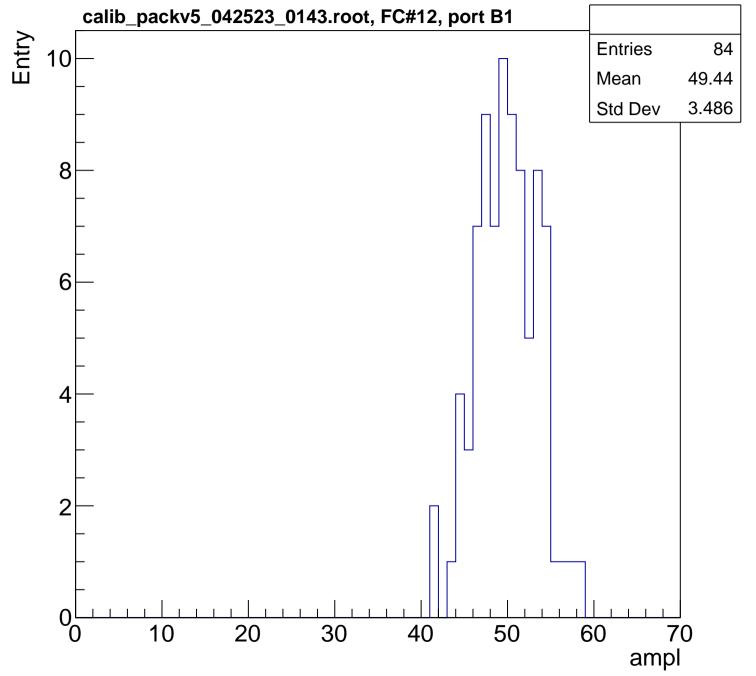


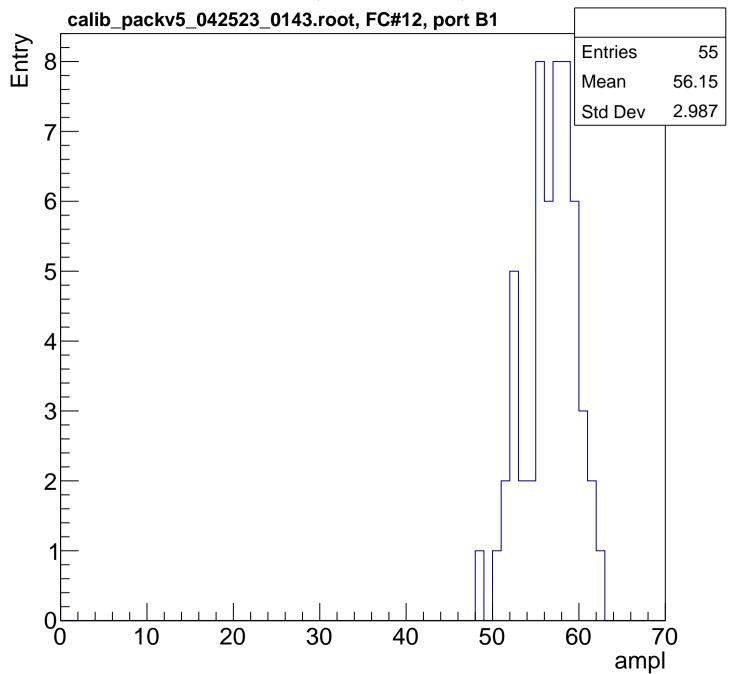


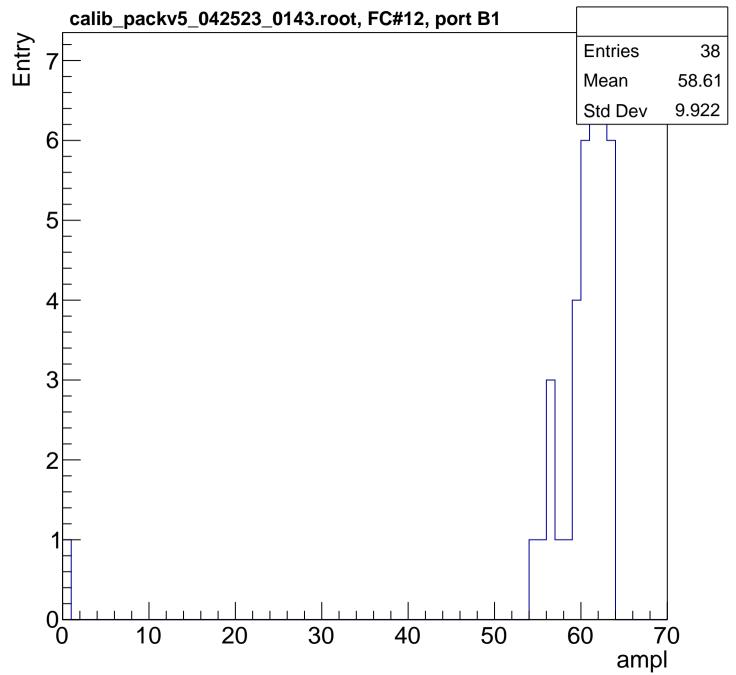


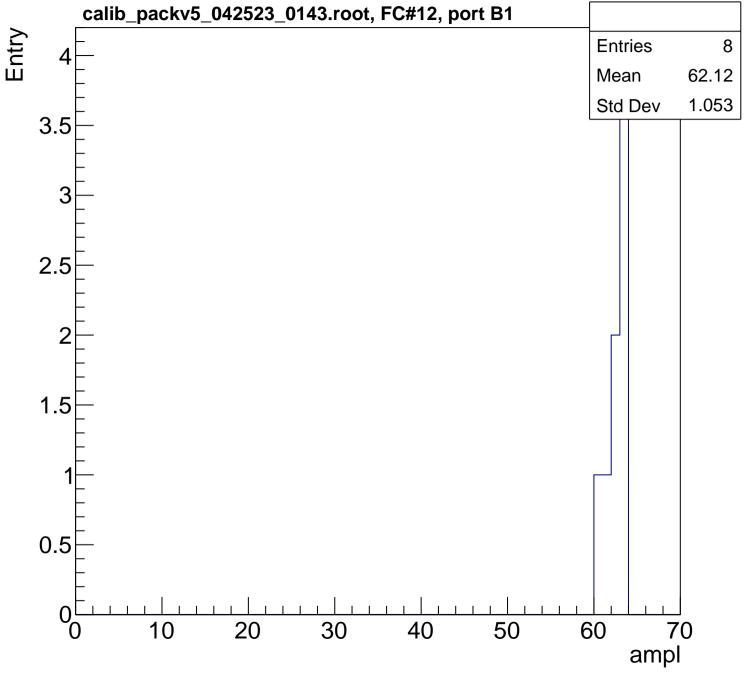




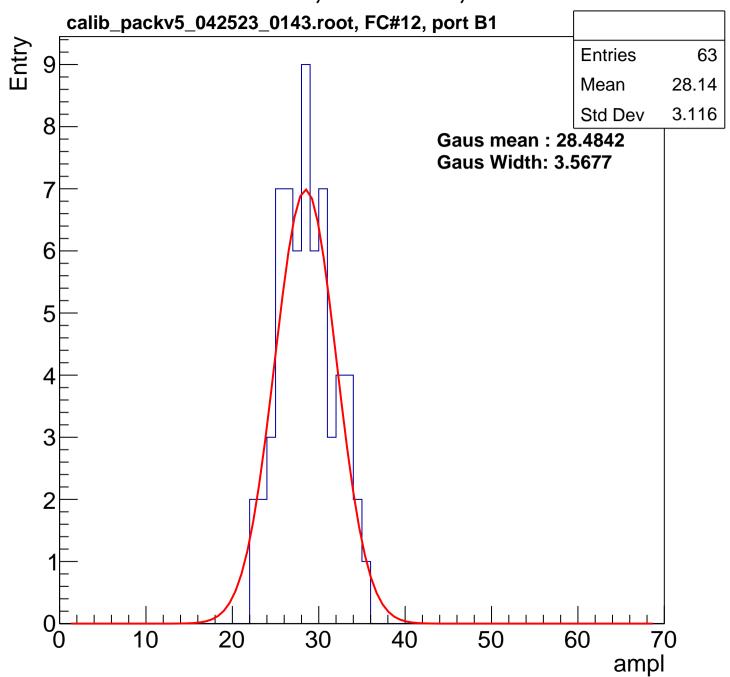


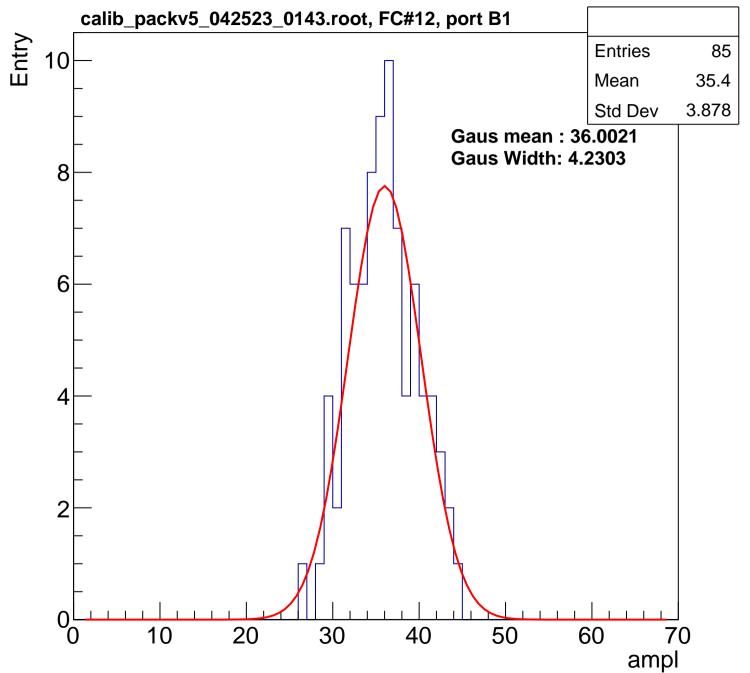


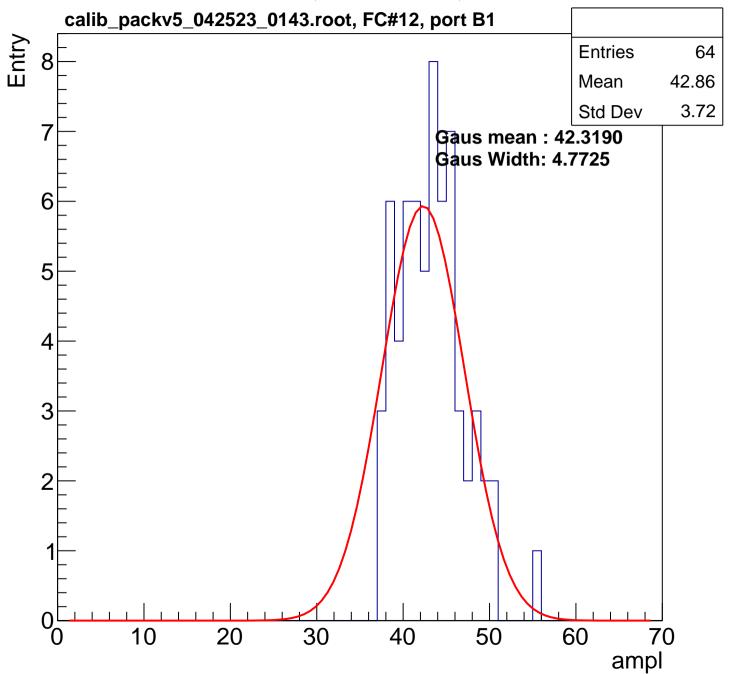


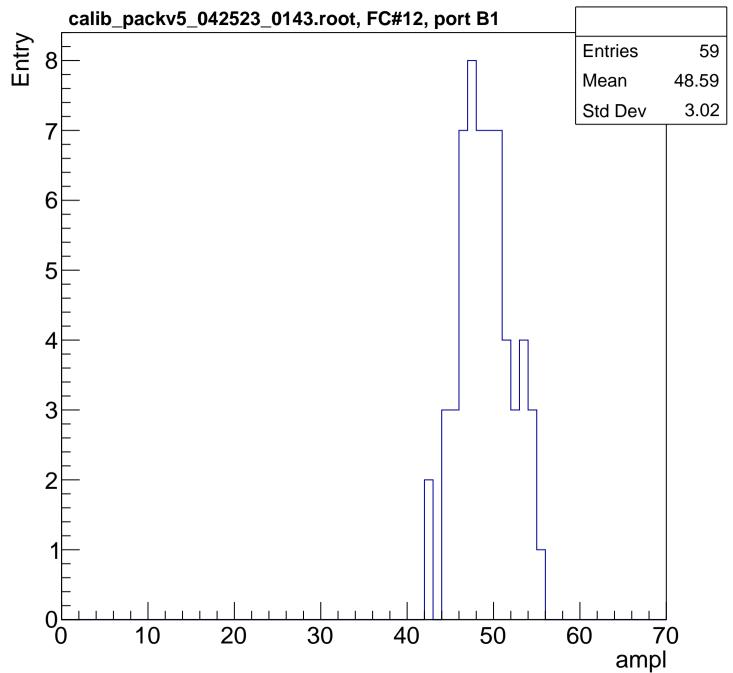


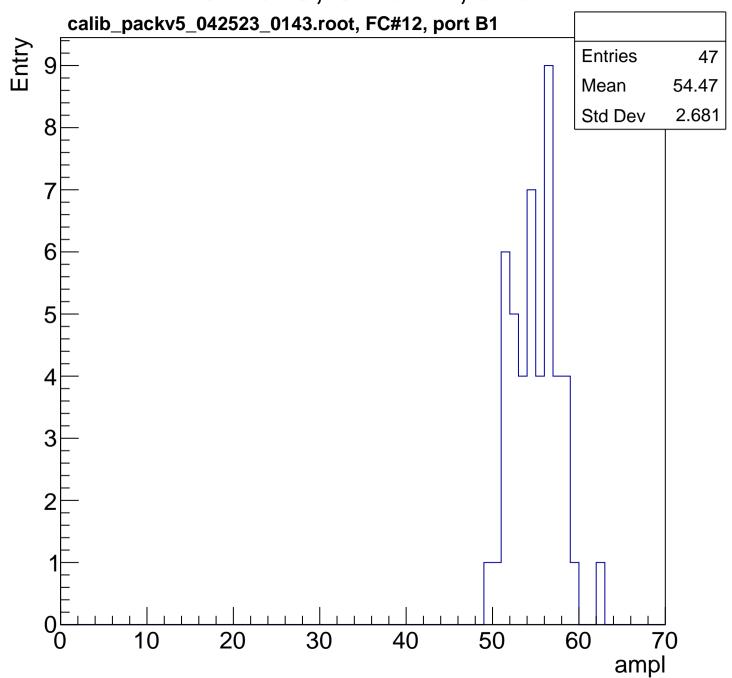


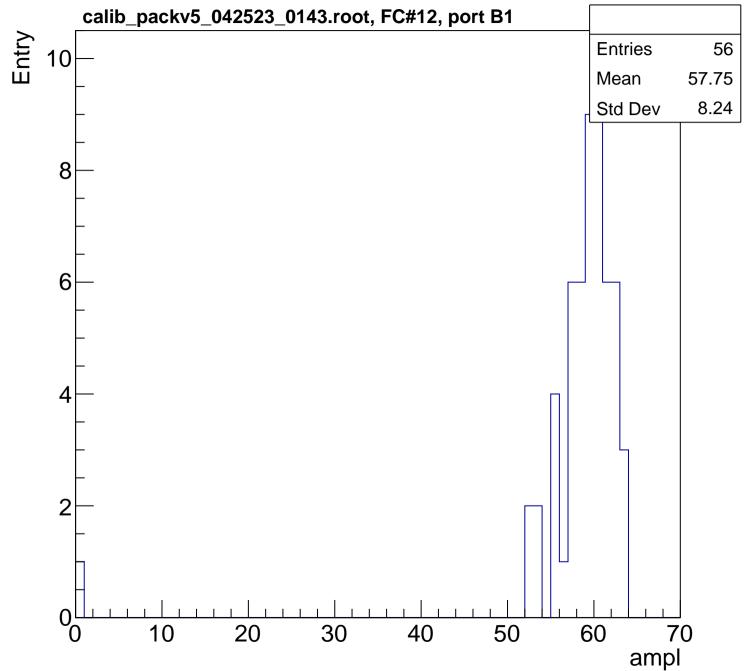


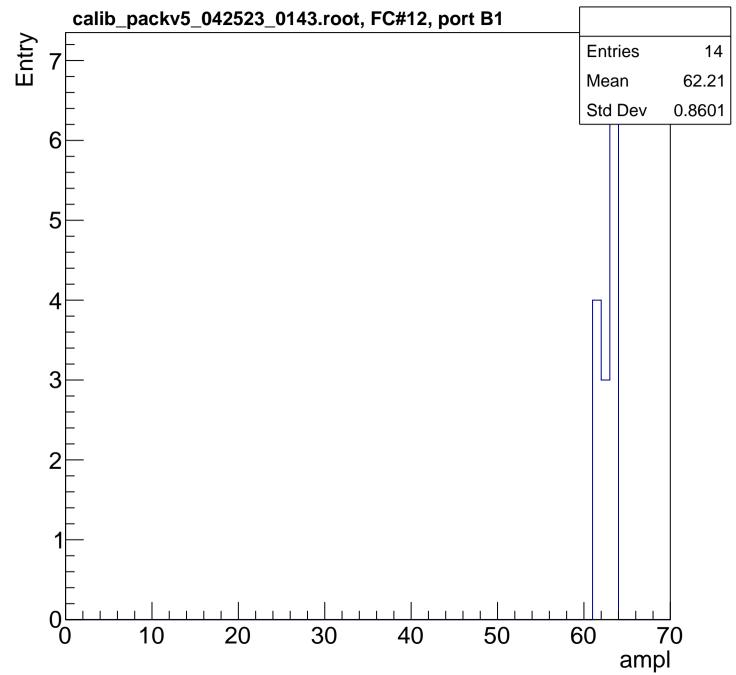




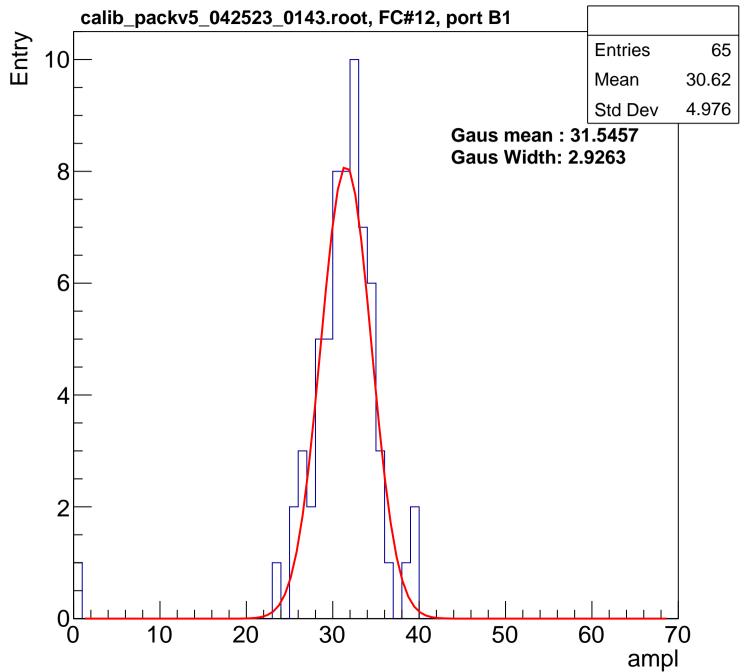


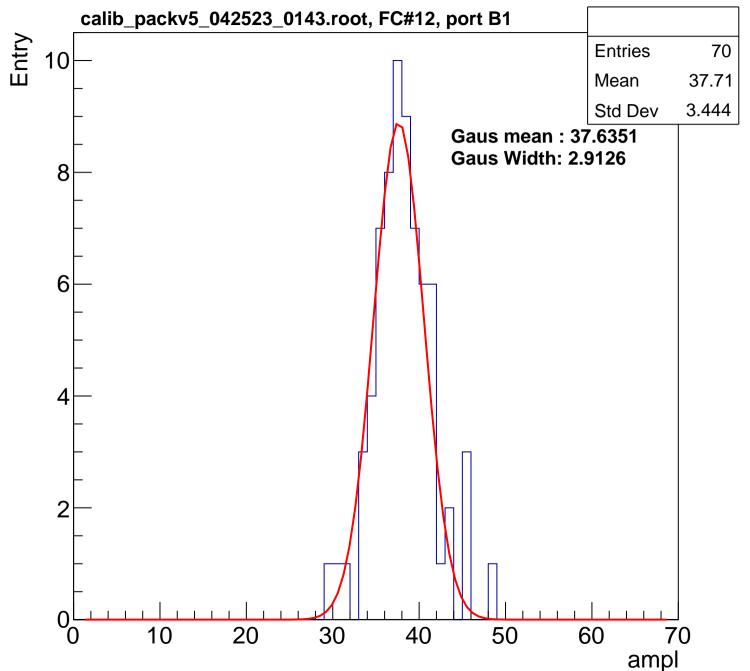


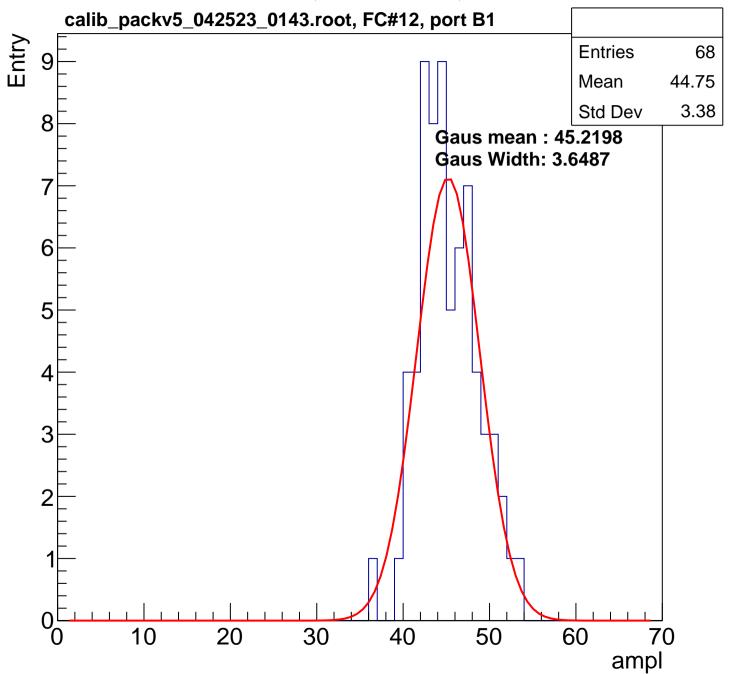


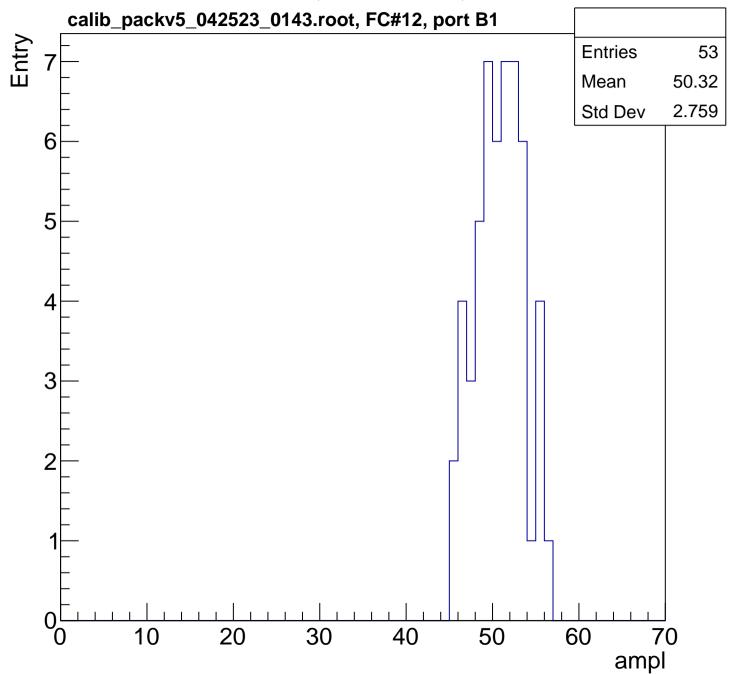


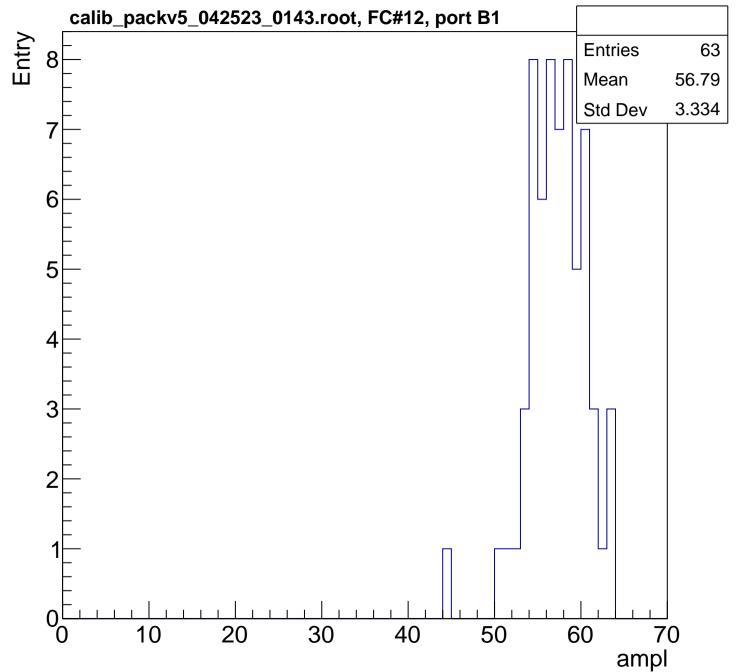
B0L102S, U7-ch12, adc7 calib_packv5_042523_0143.root, FC#12, port B1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

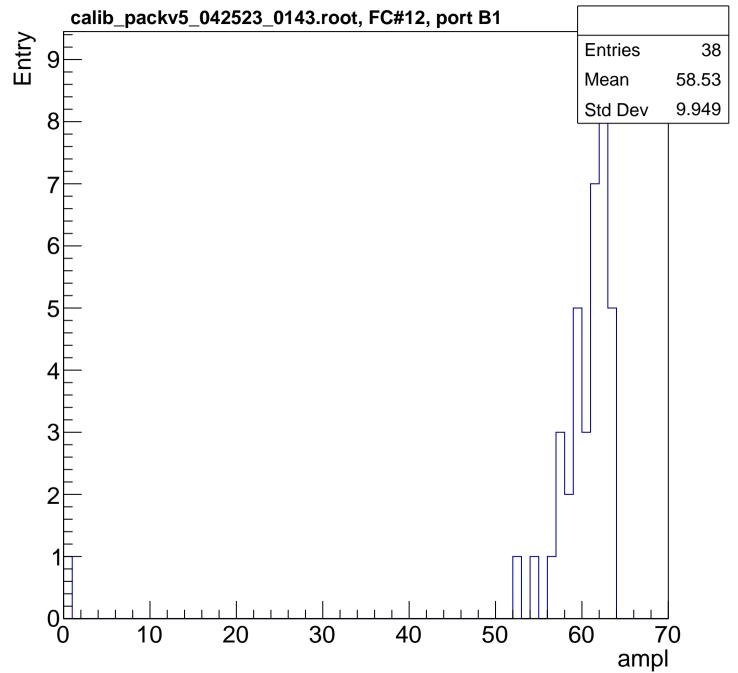


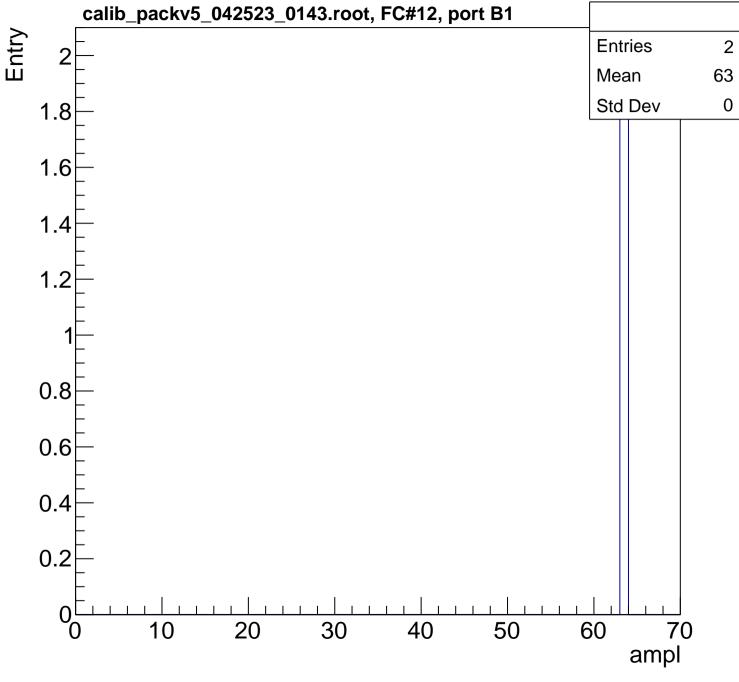


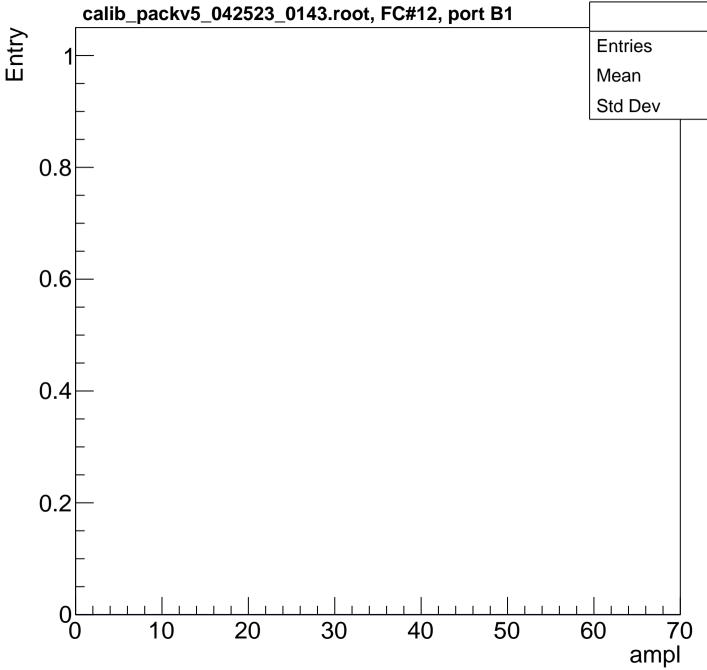


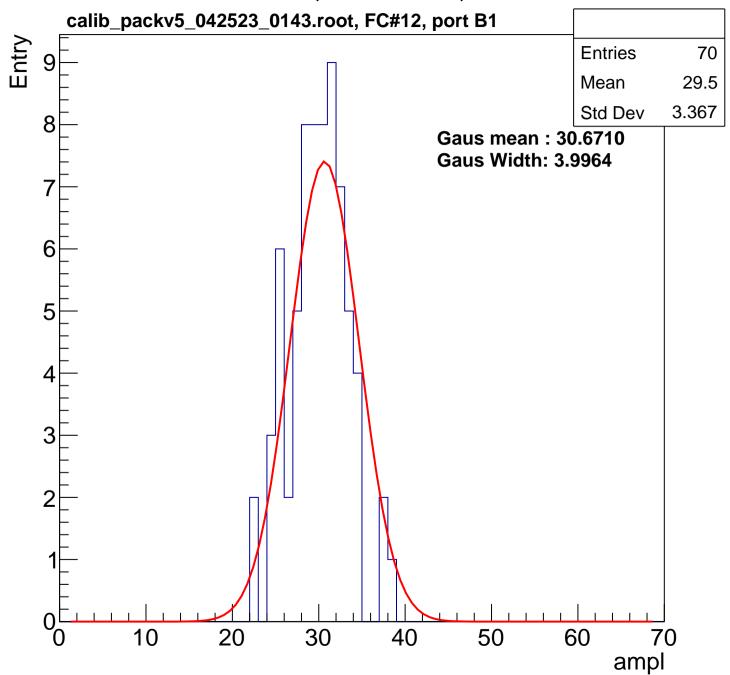


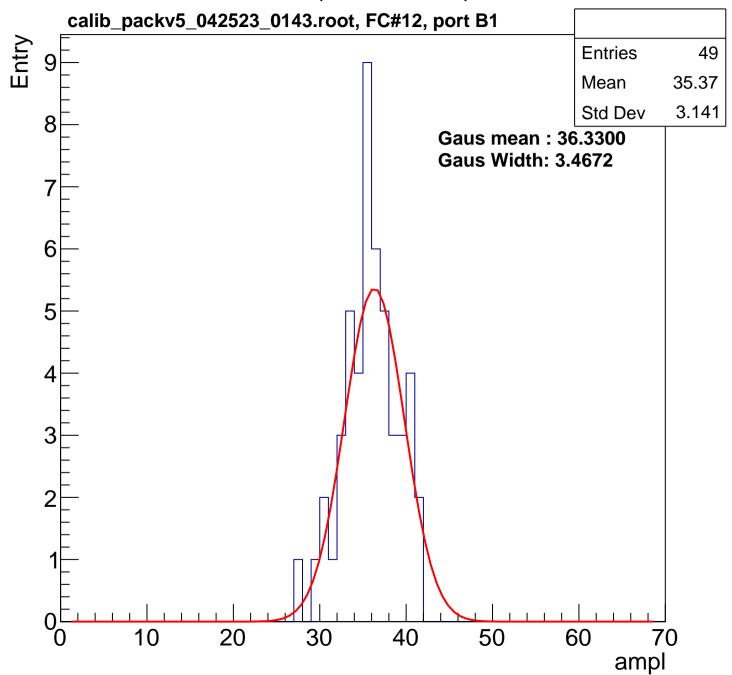


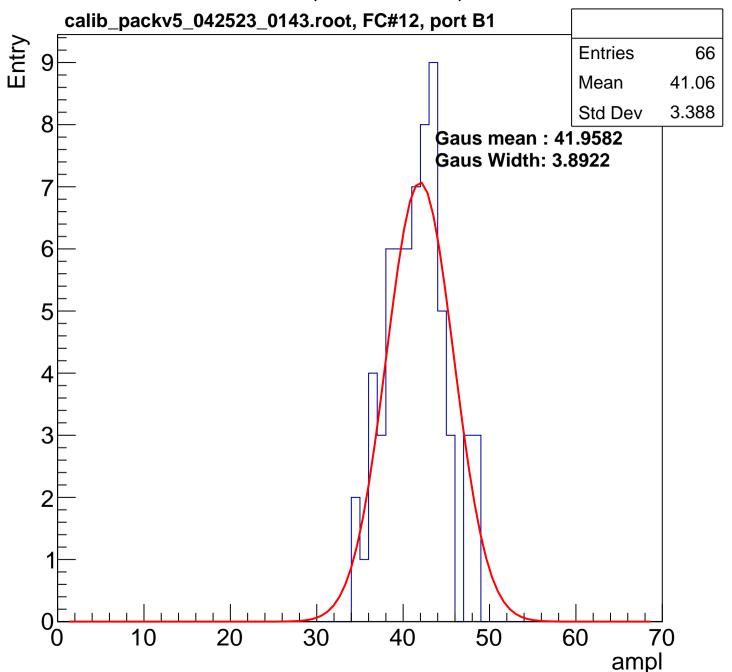


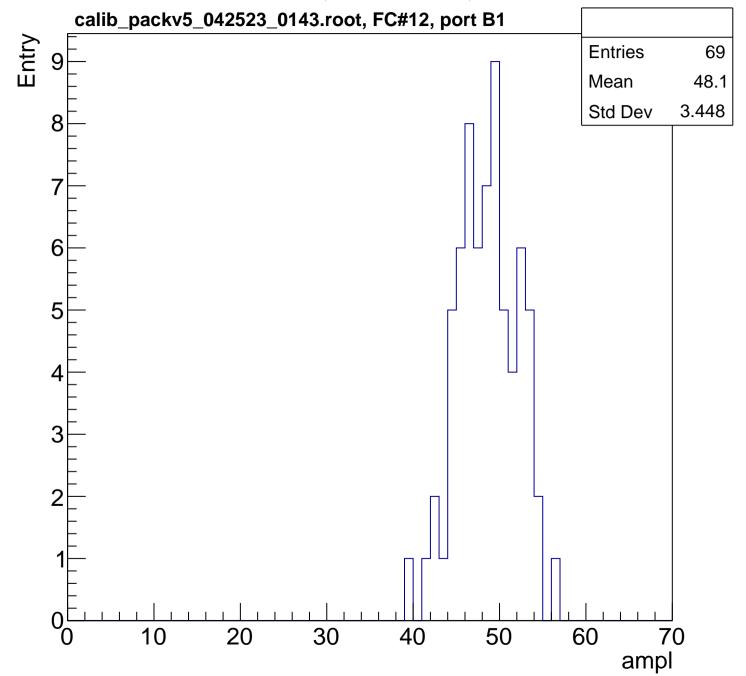


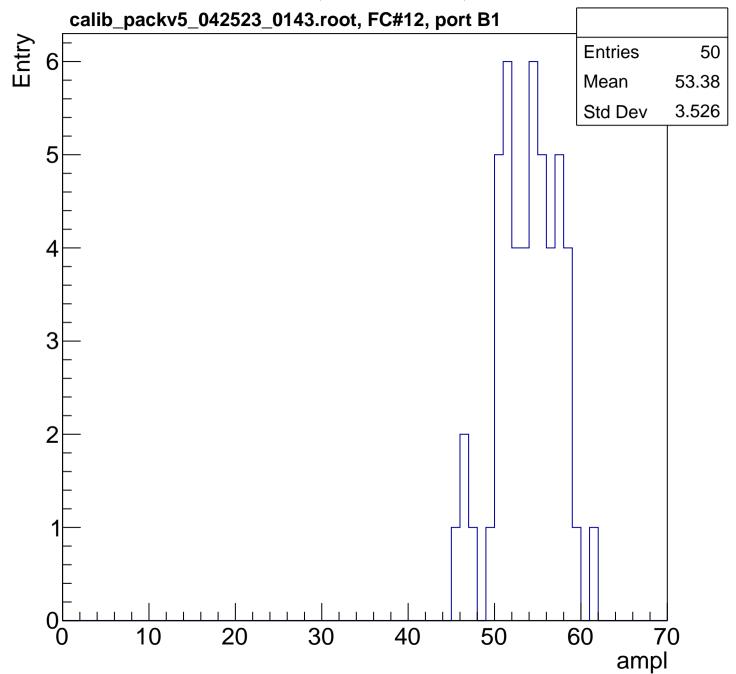


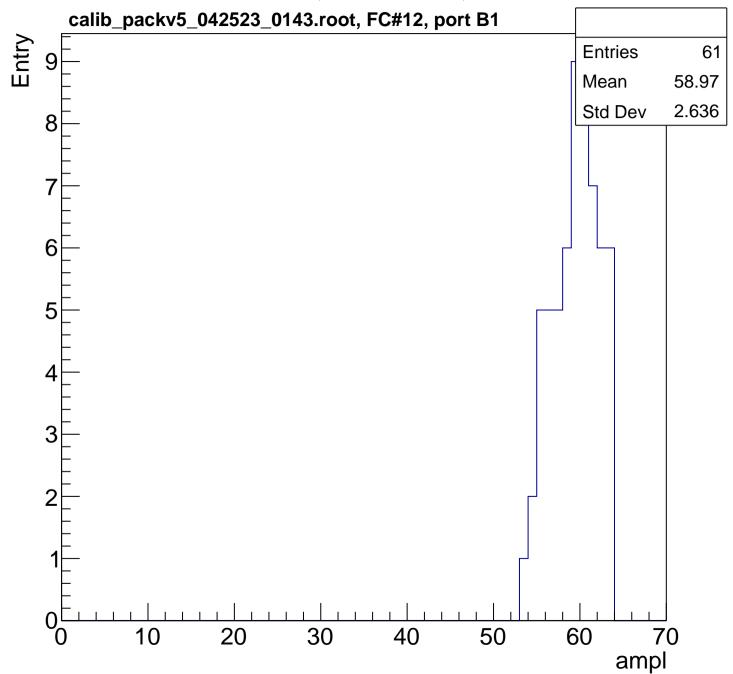


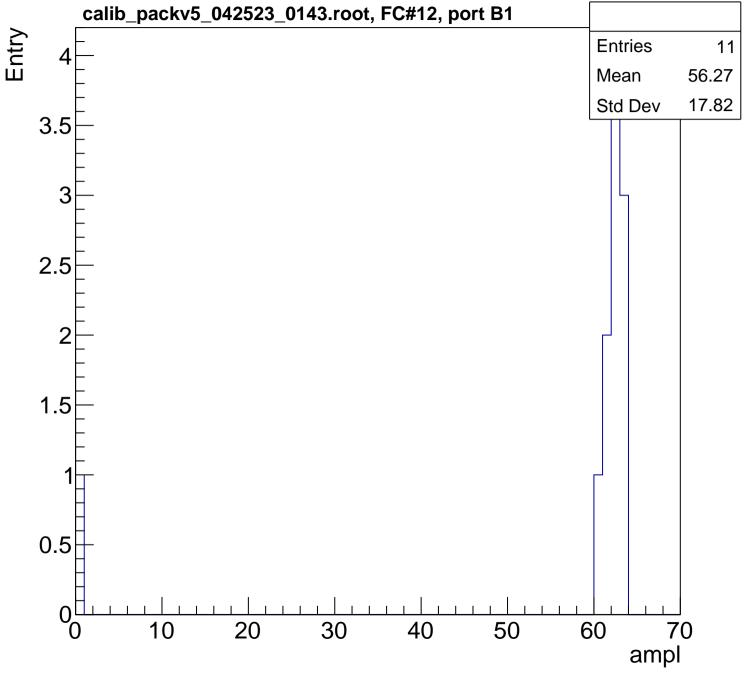


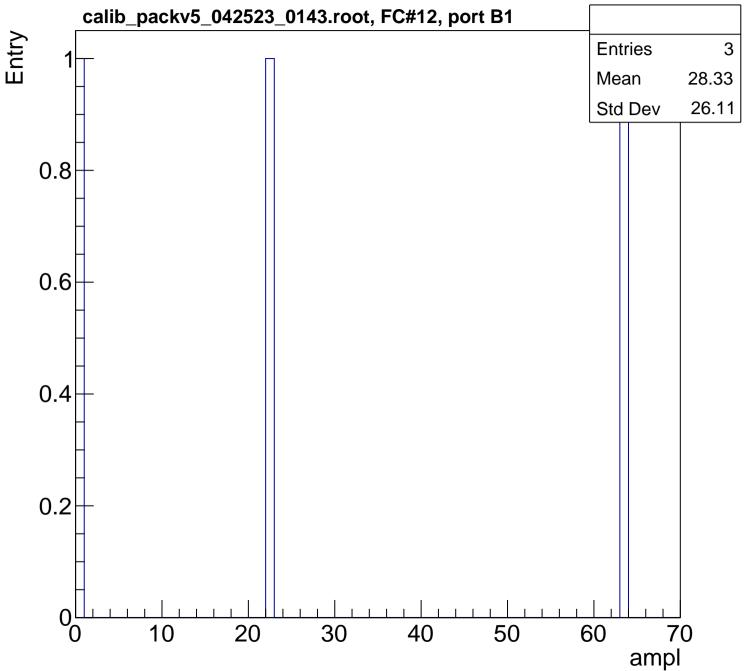


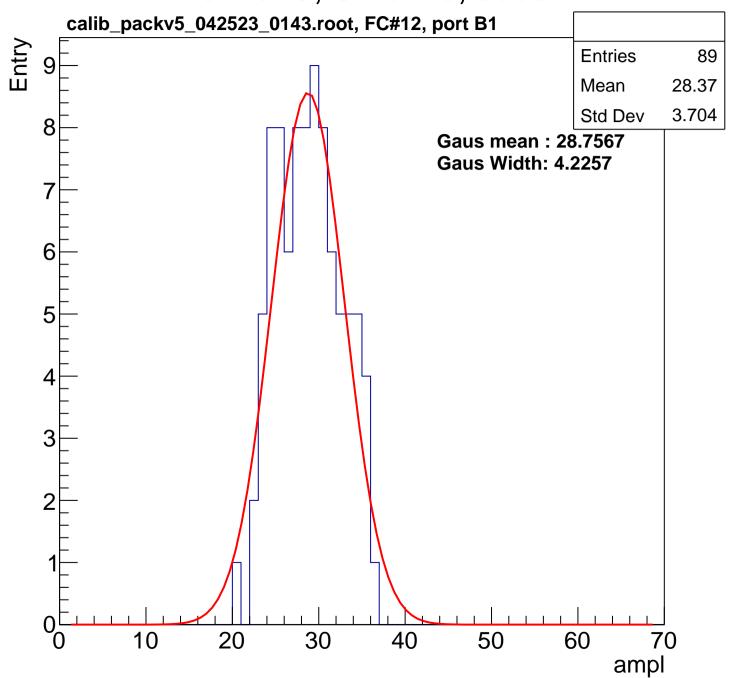


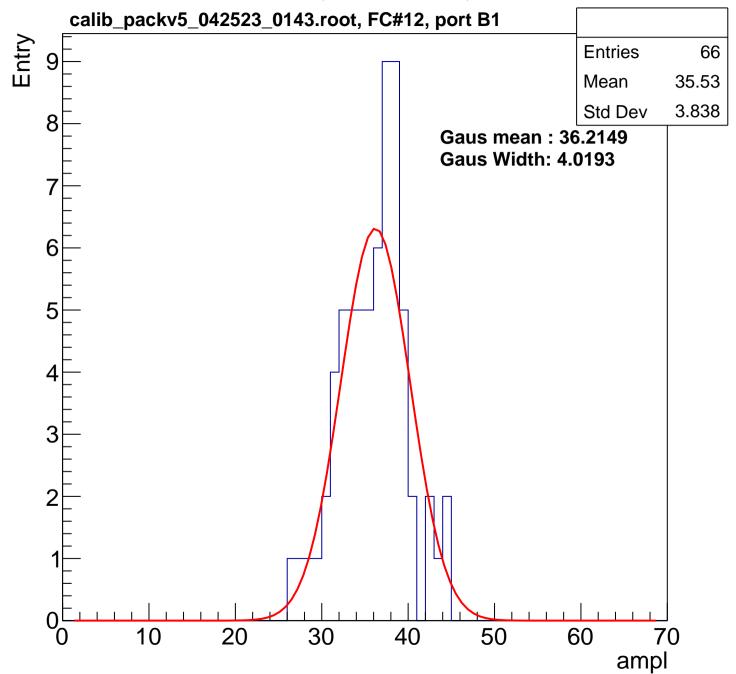


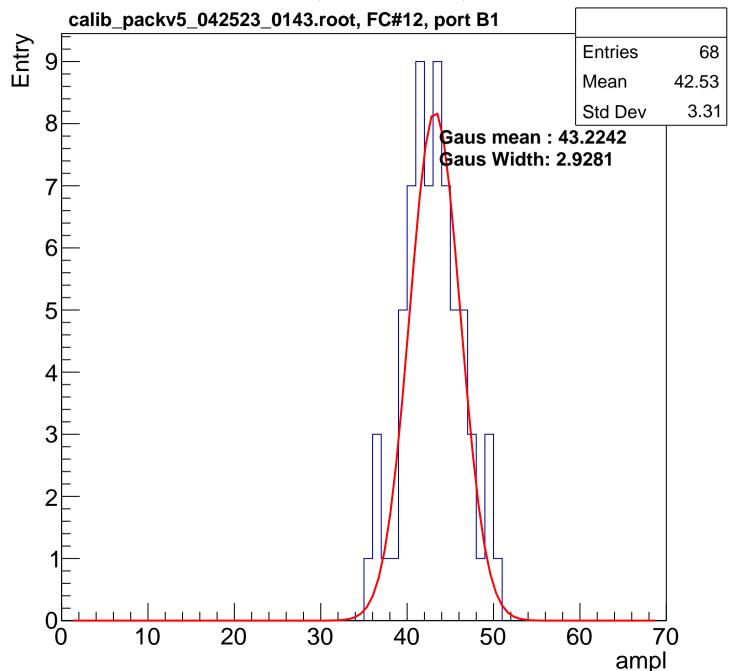


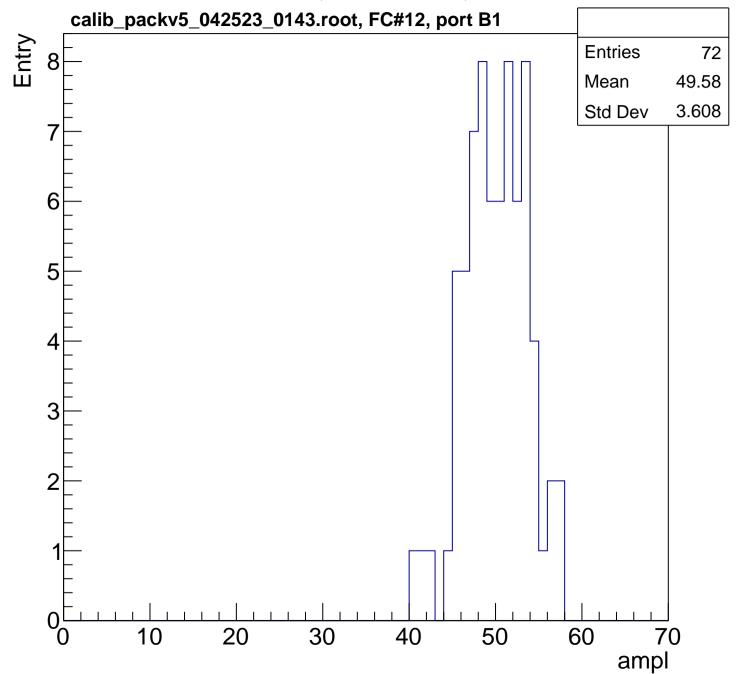


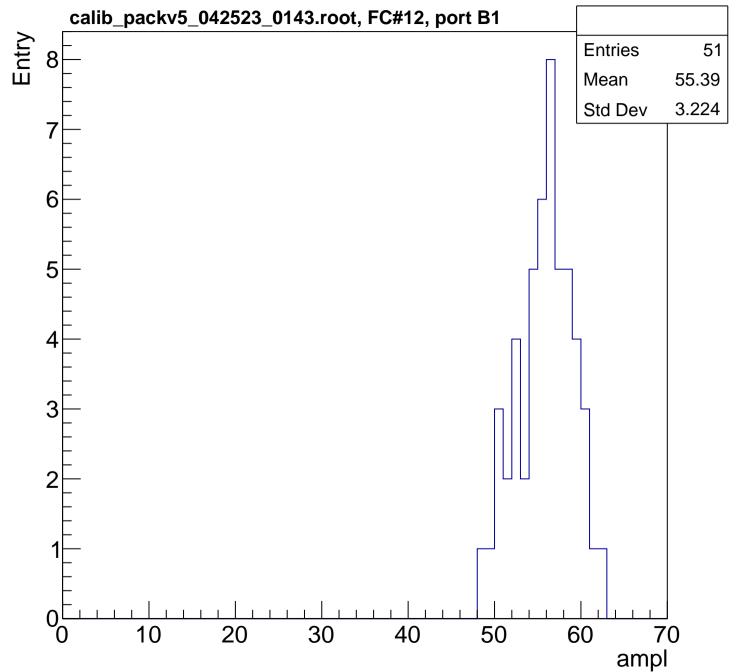


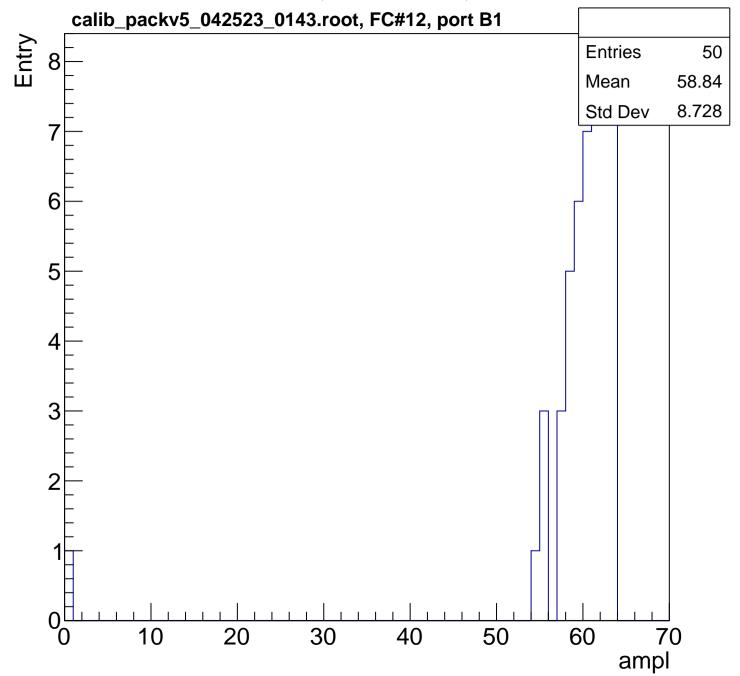


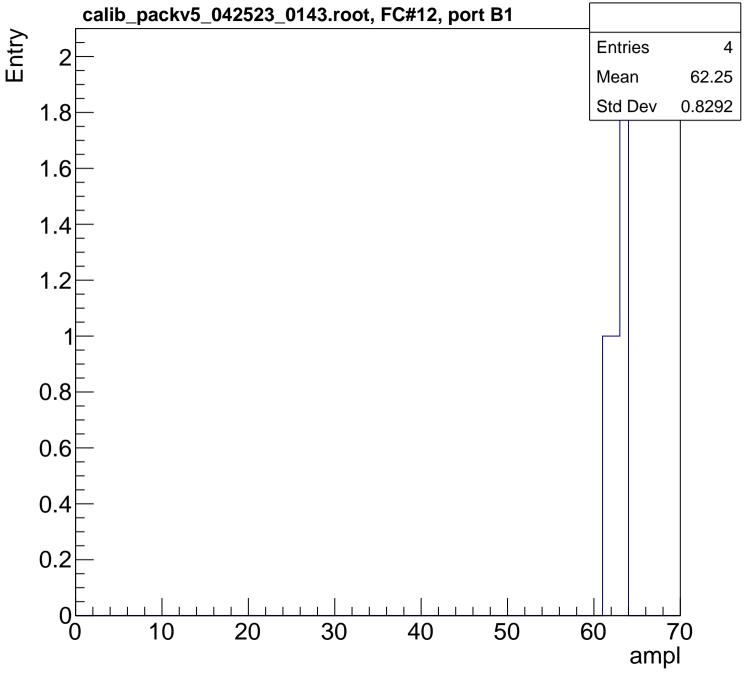




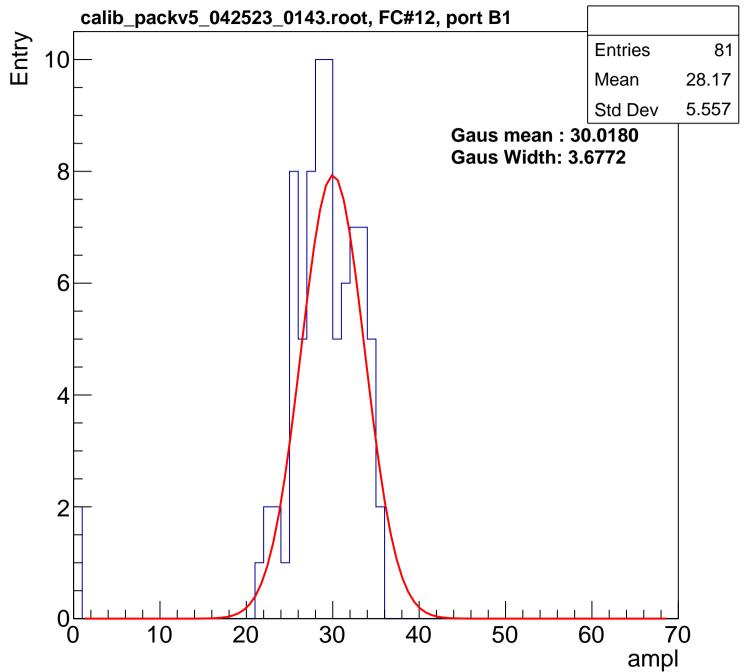


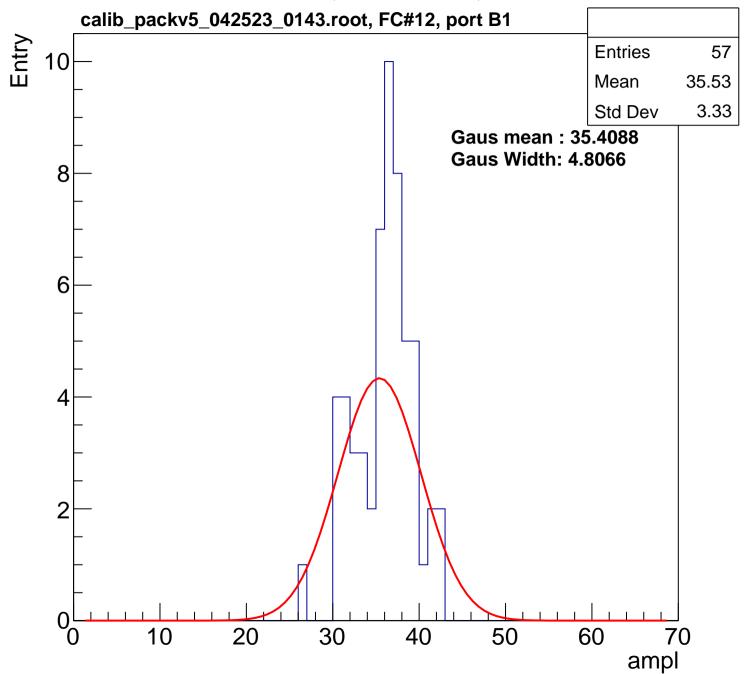


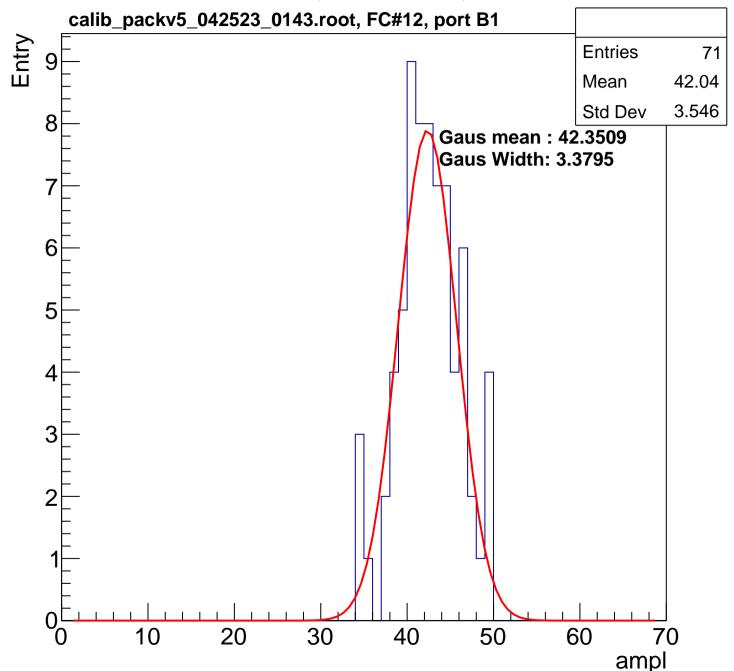


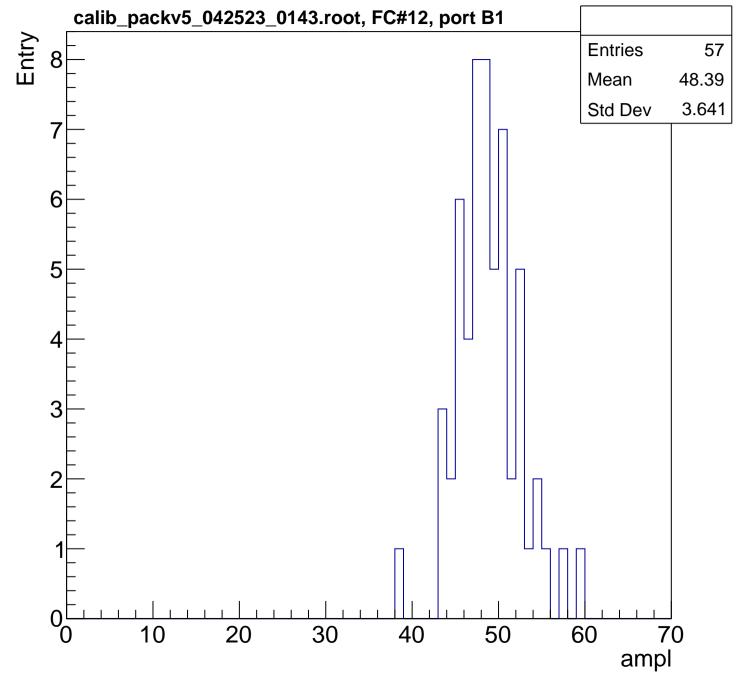


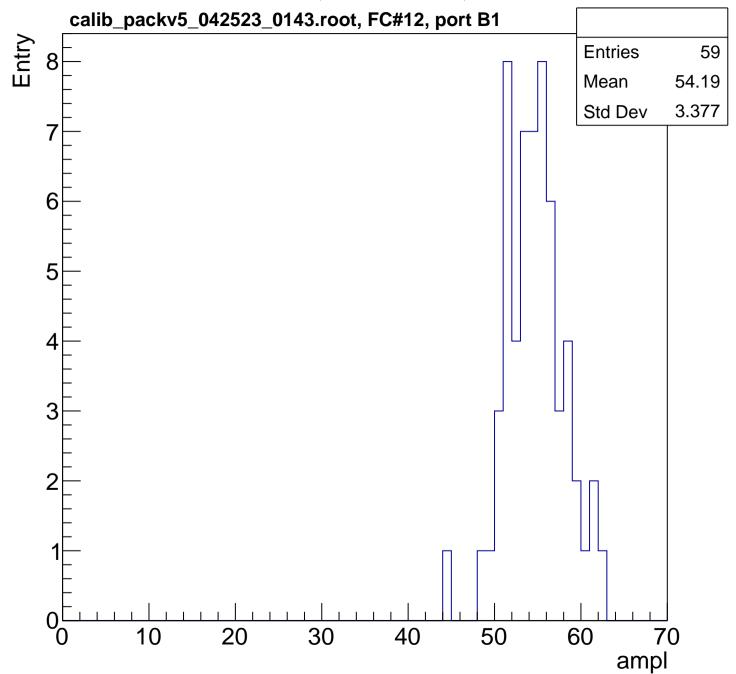


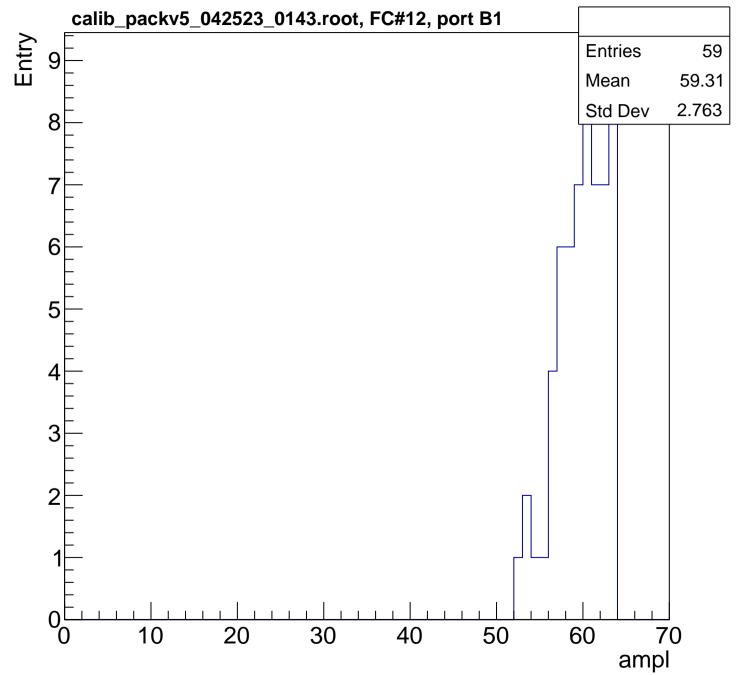


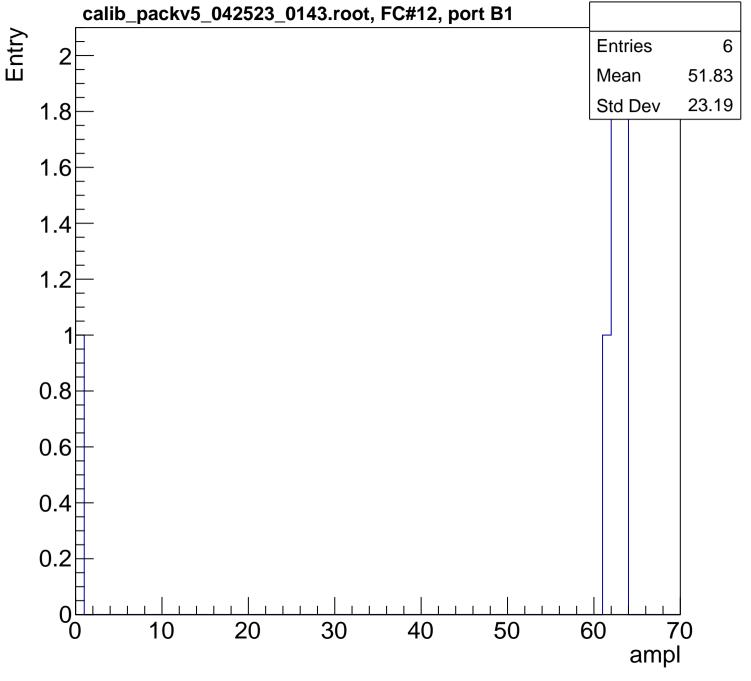






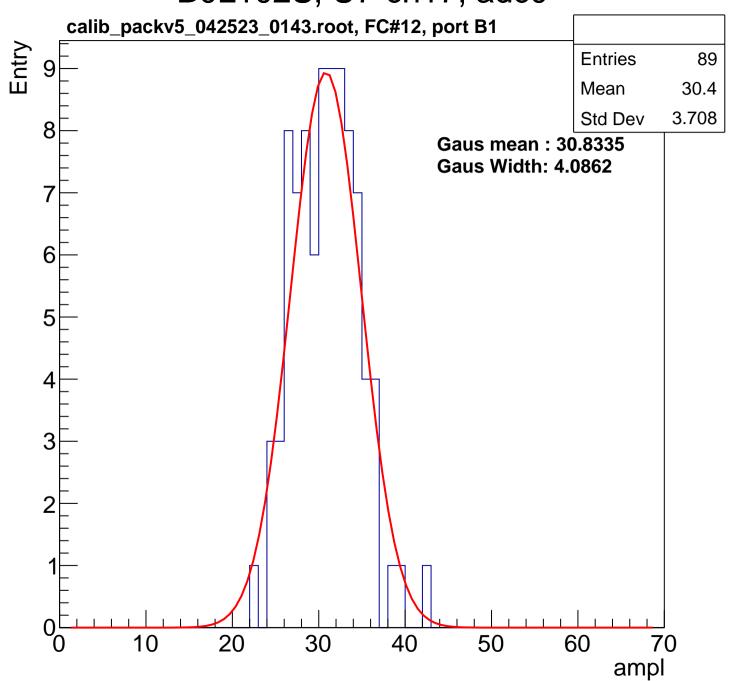


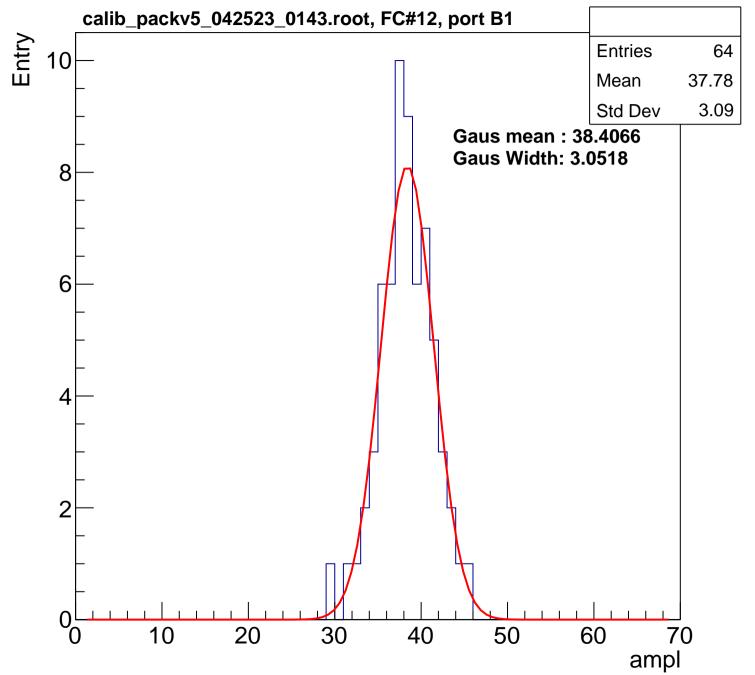


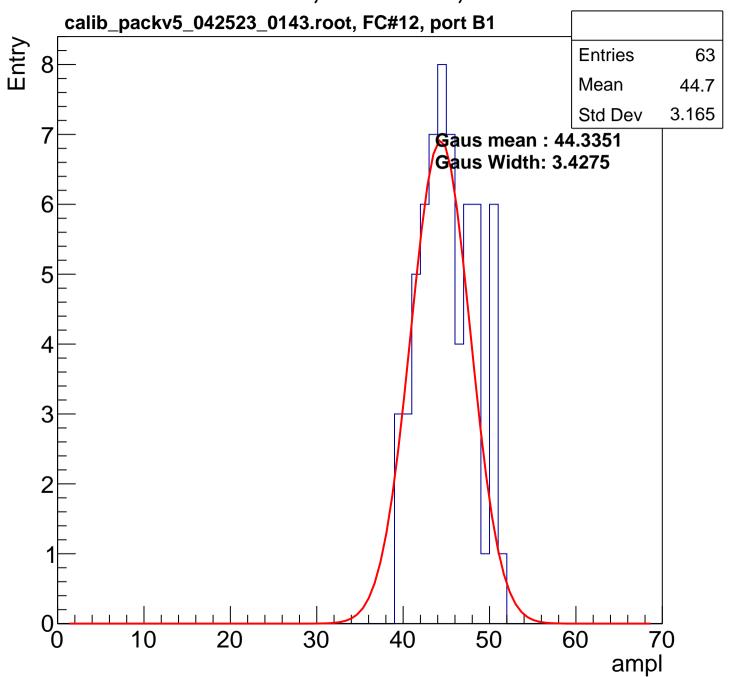


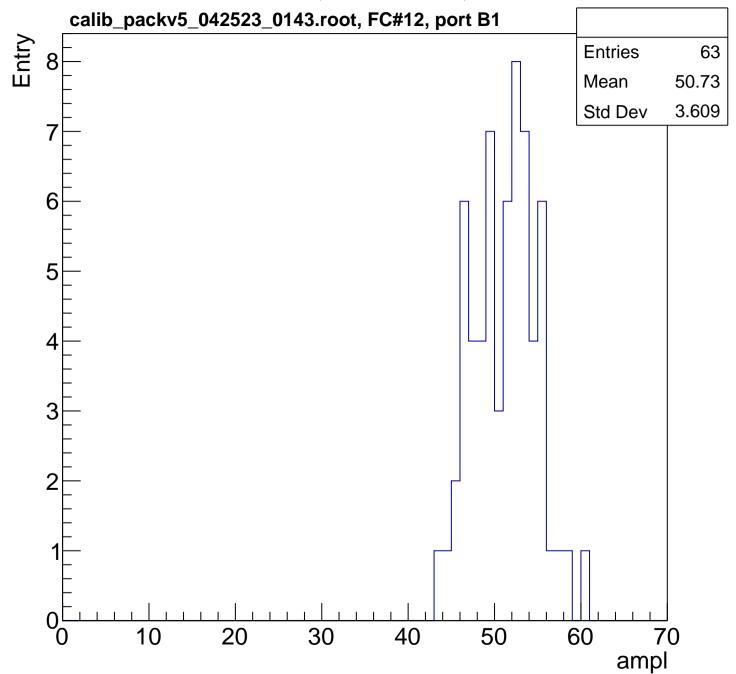
B0L102S, U7-ch16, adc7 calib_packv5_042523_0143.root, FC#12, port B1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70

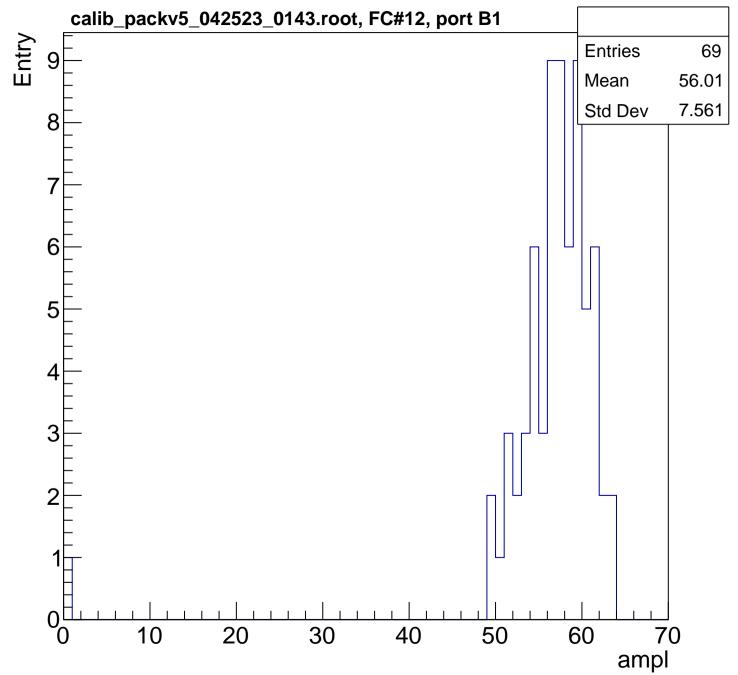
ampl

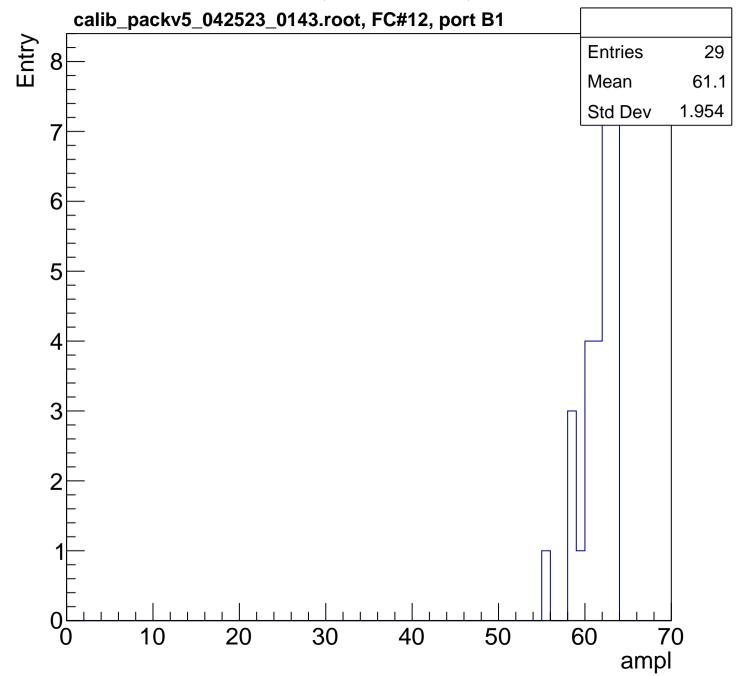






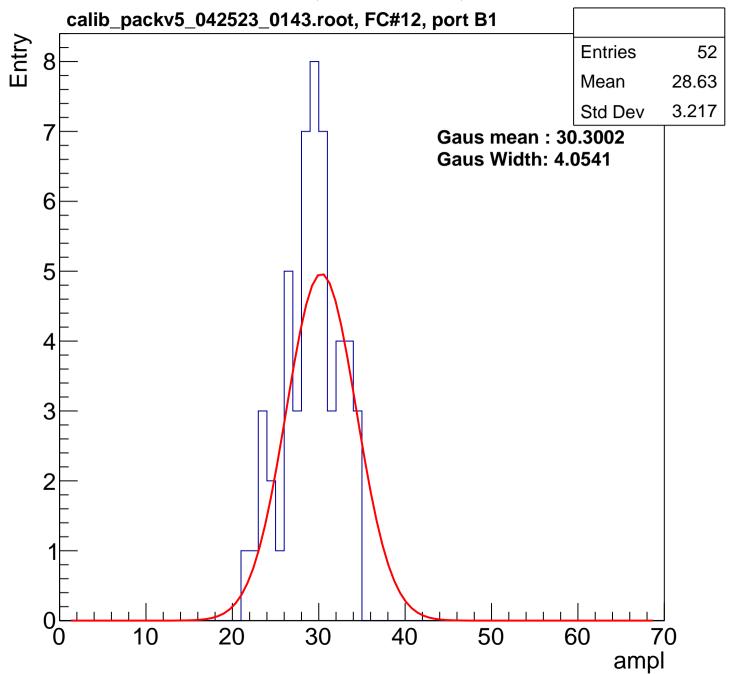


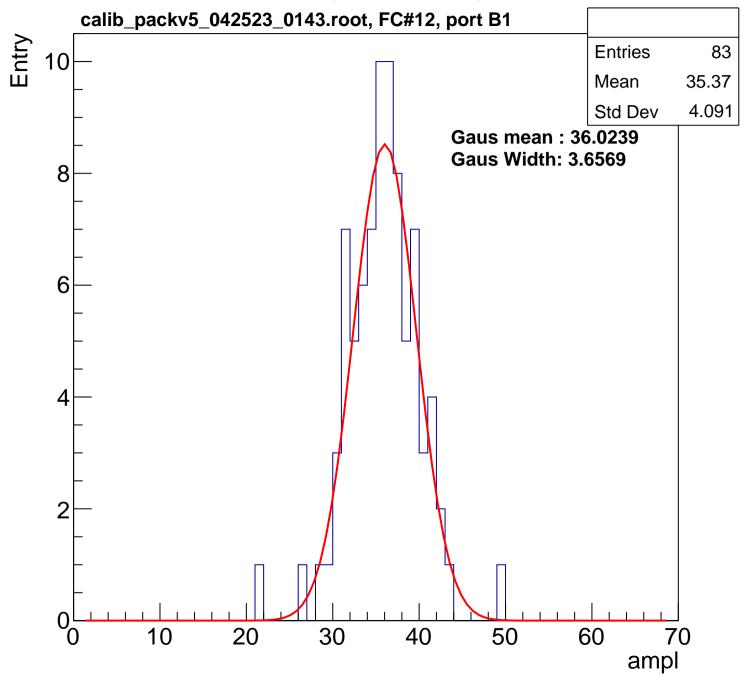


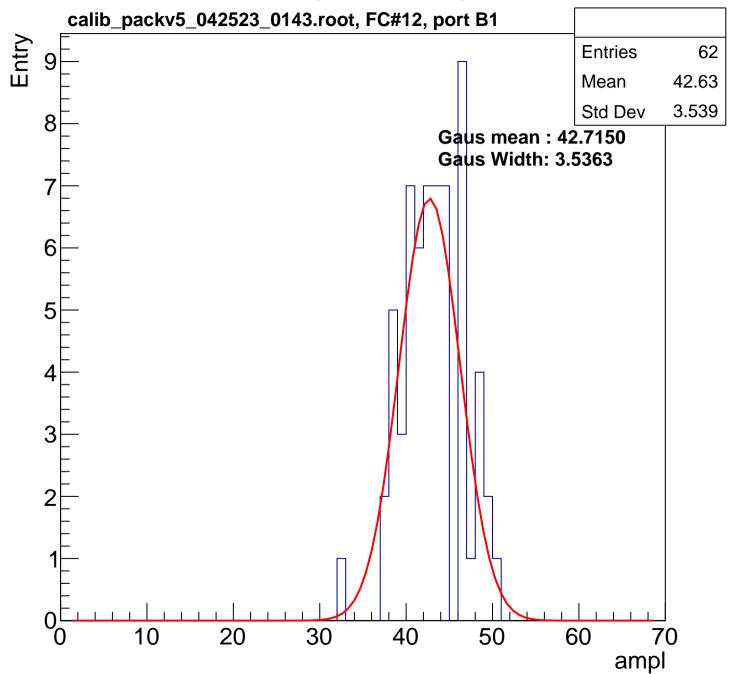


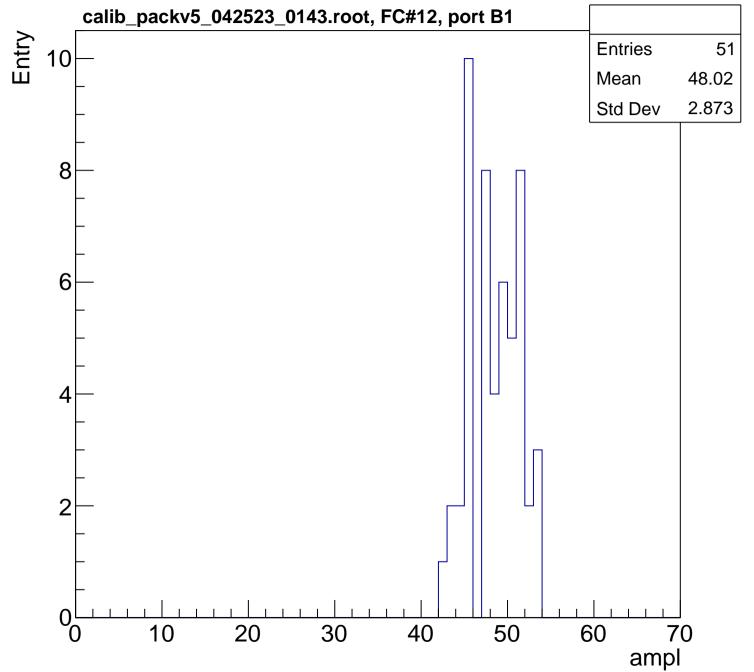


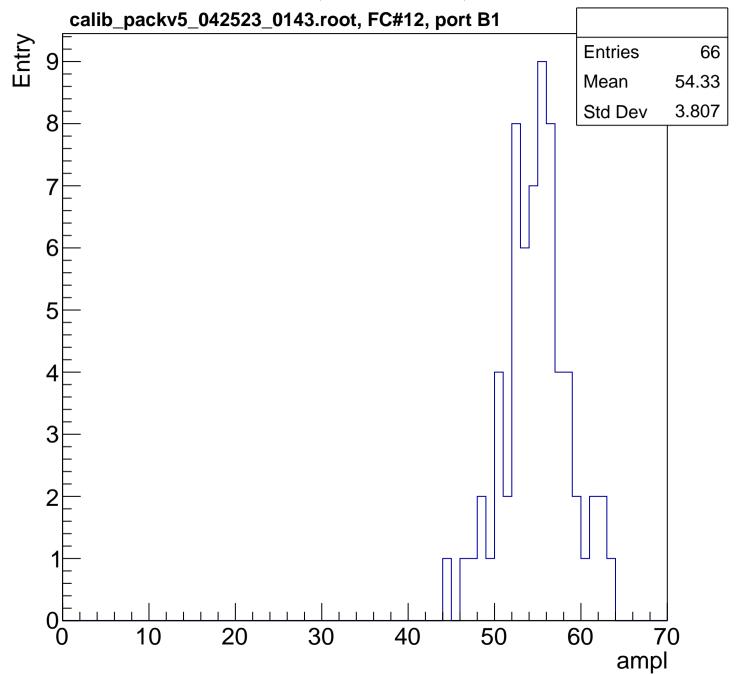
B0L102S, U7-ch17, adc7 calib_packv5_042523_0143.root, FC#12, port B1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

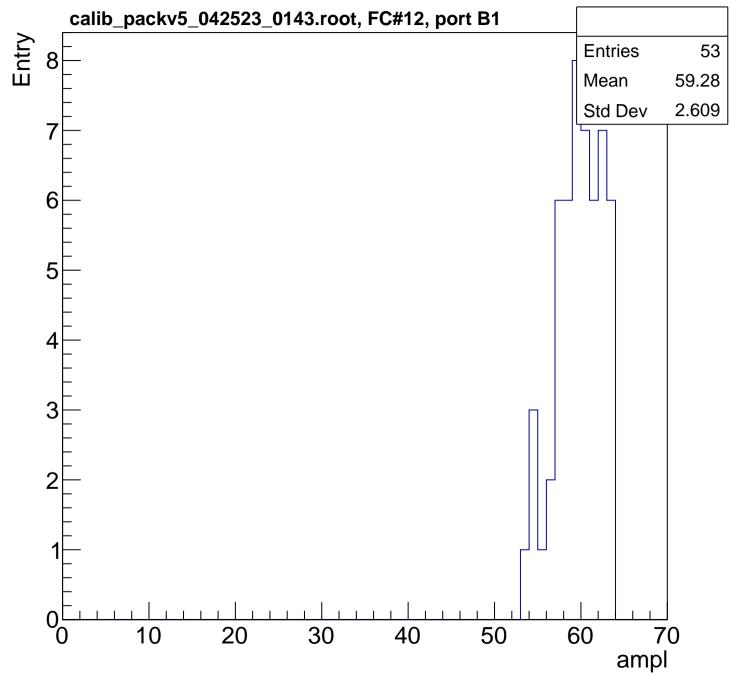


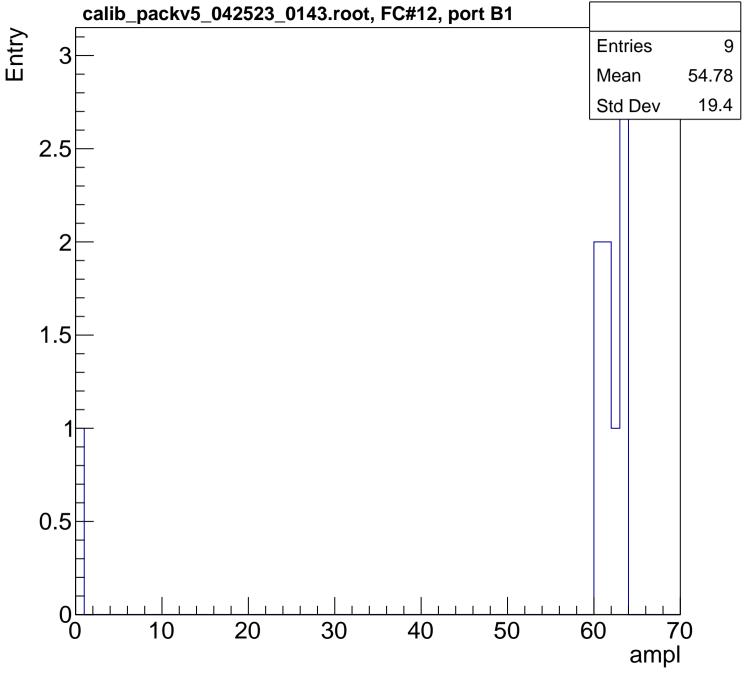


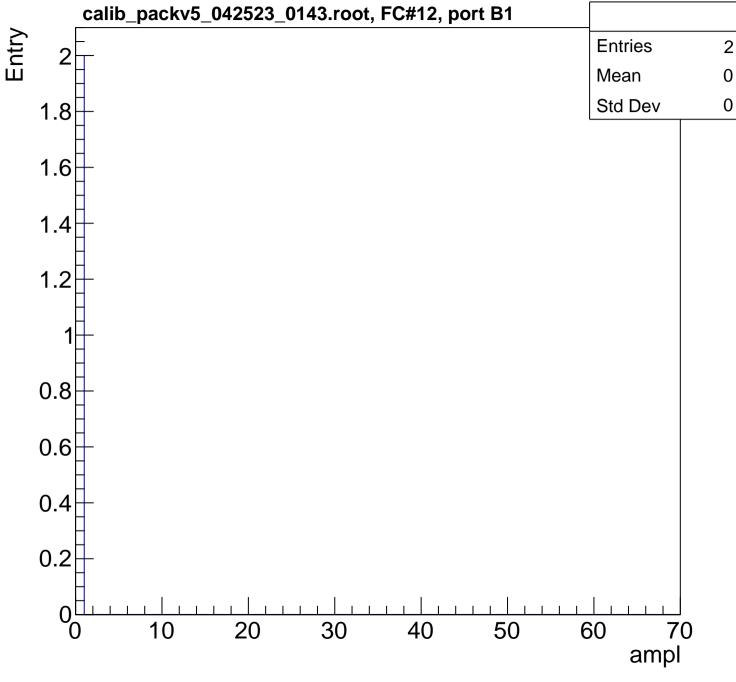


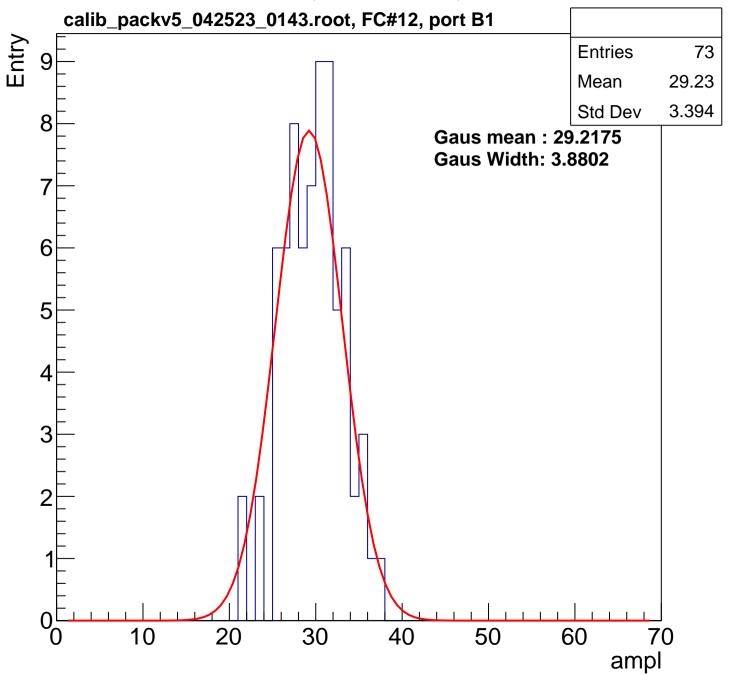


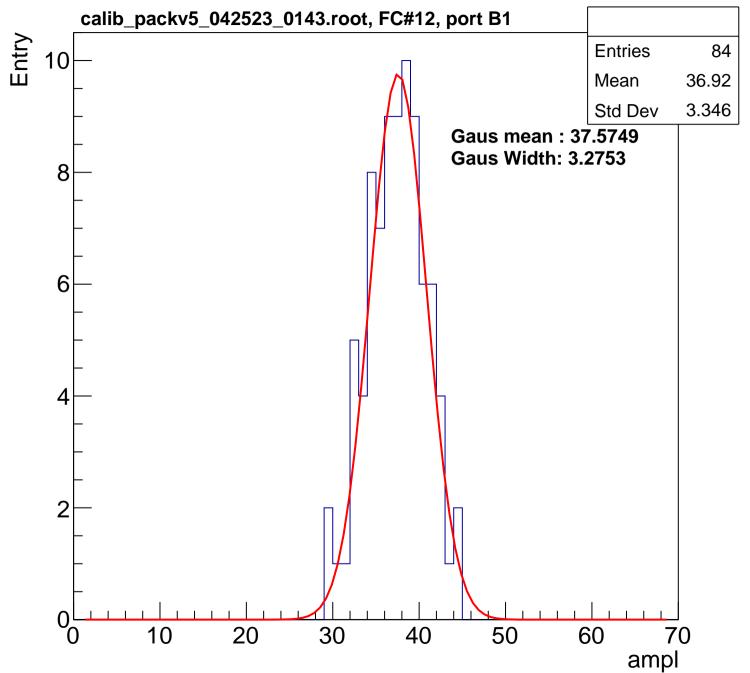


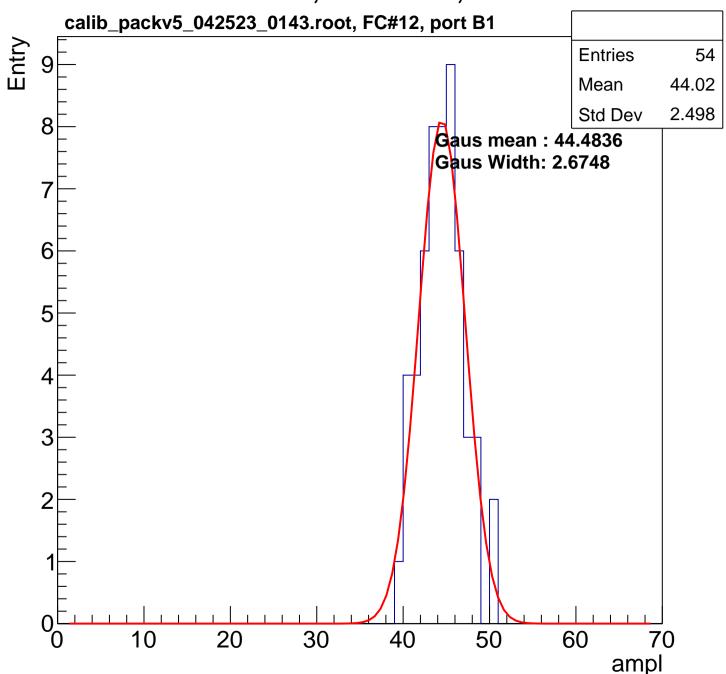


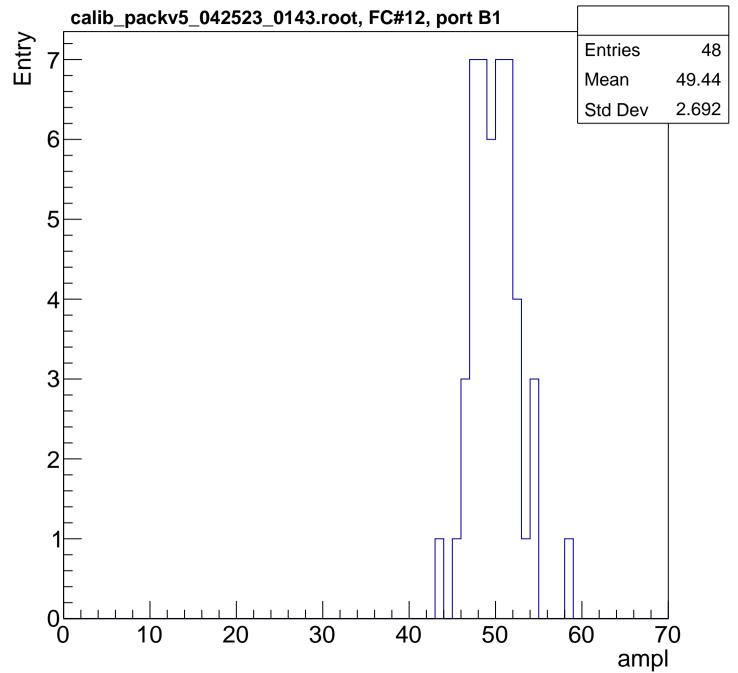


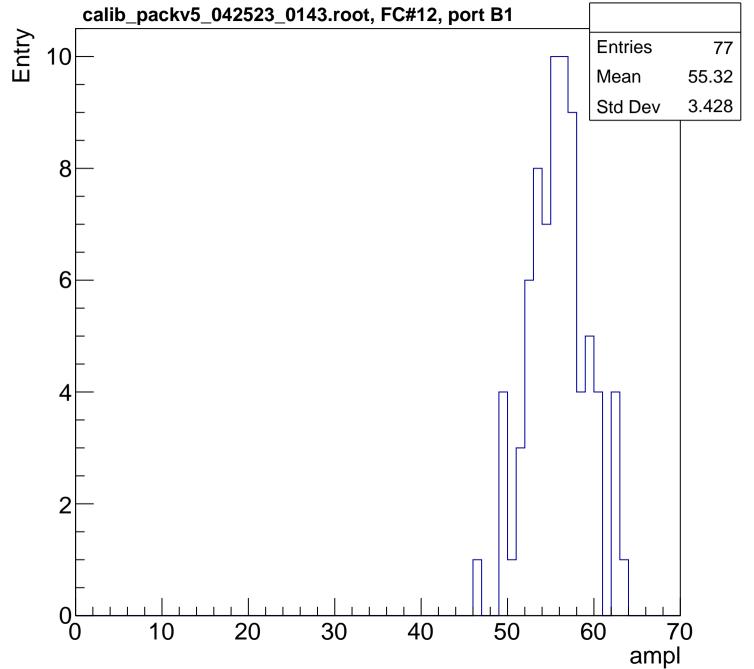


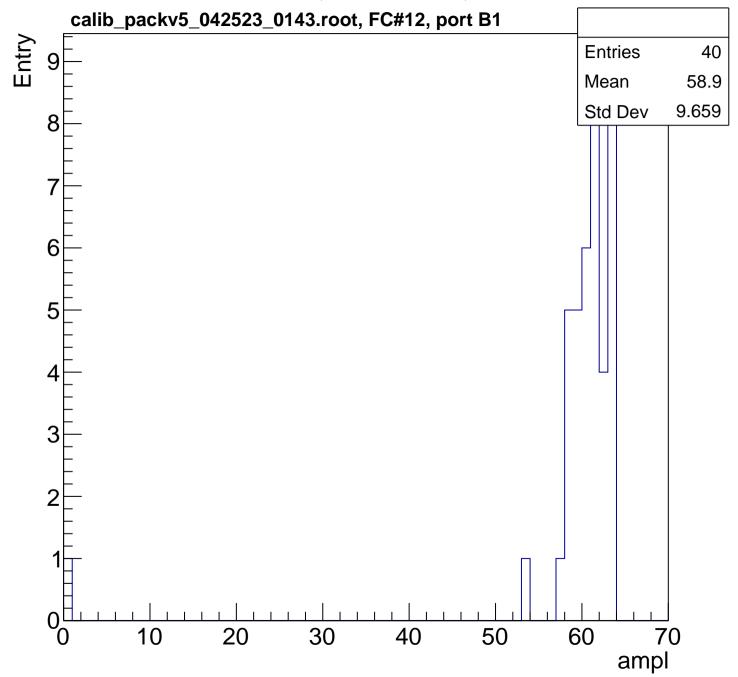


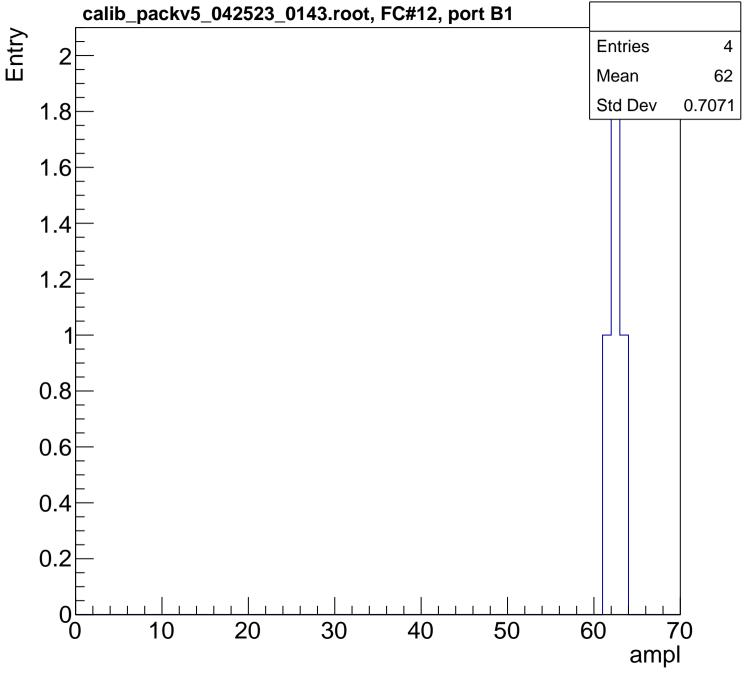


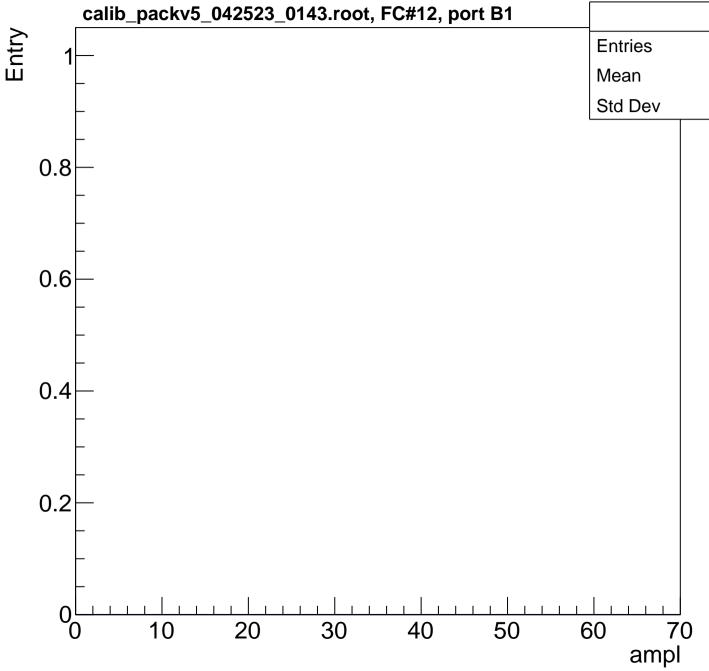


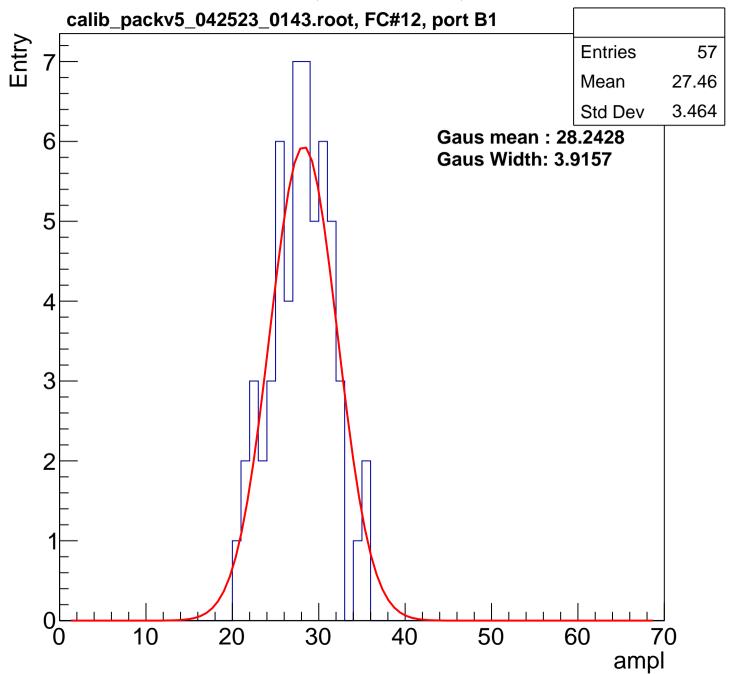


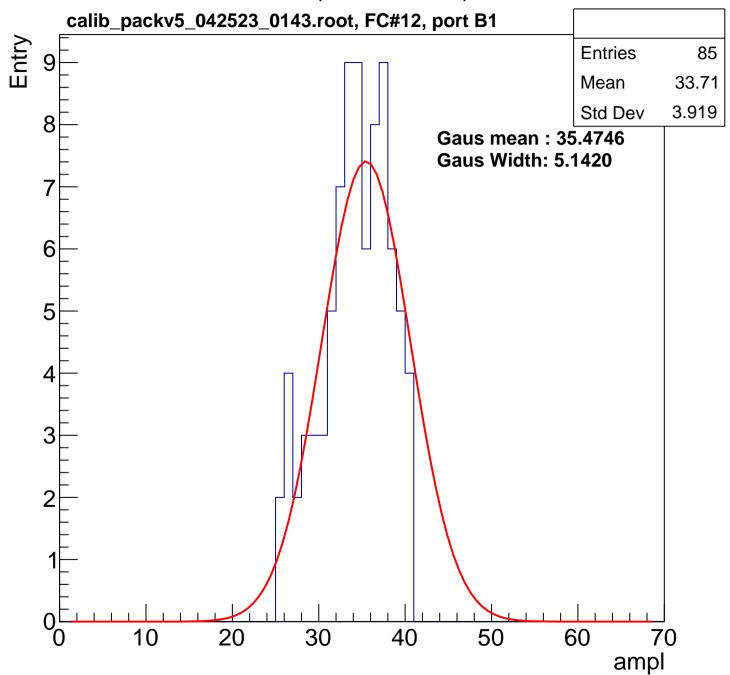


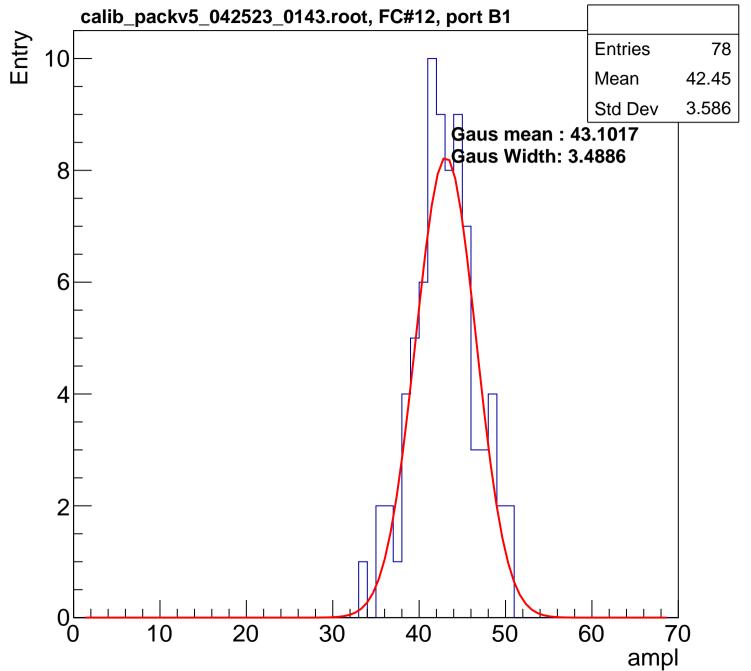


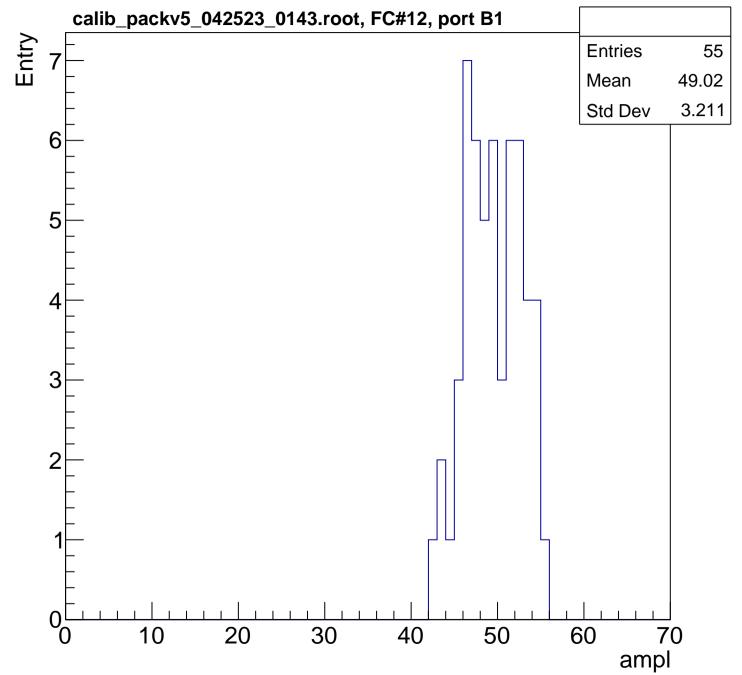


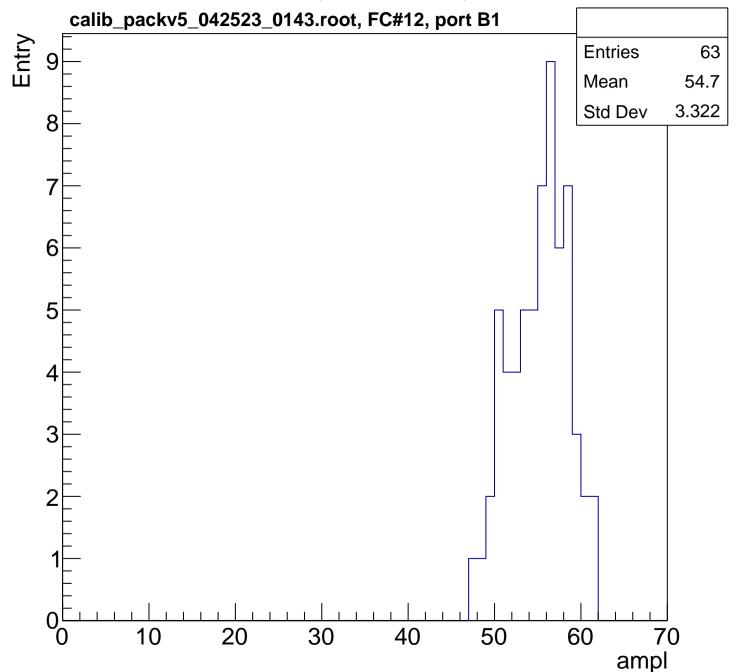


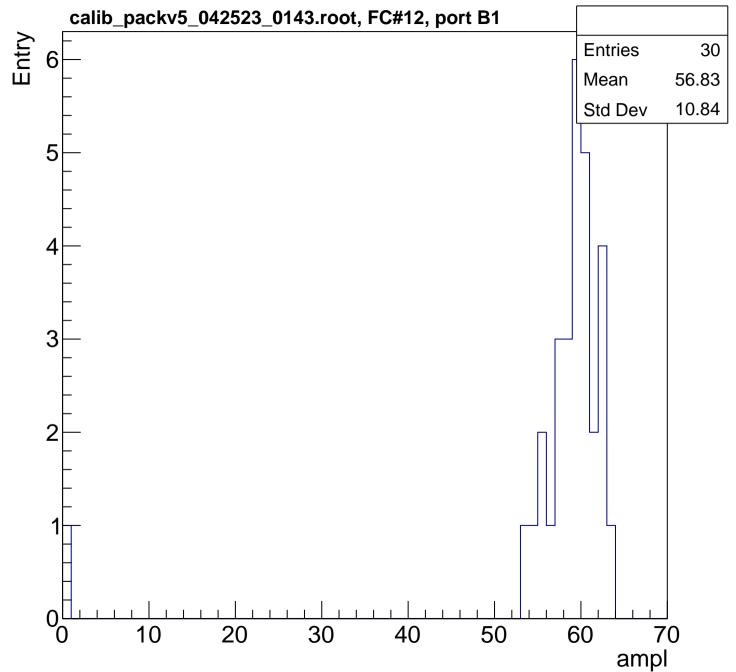


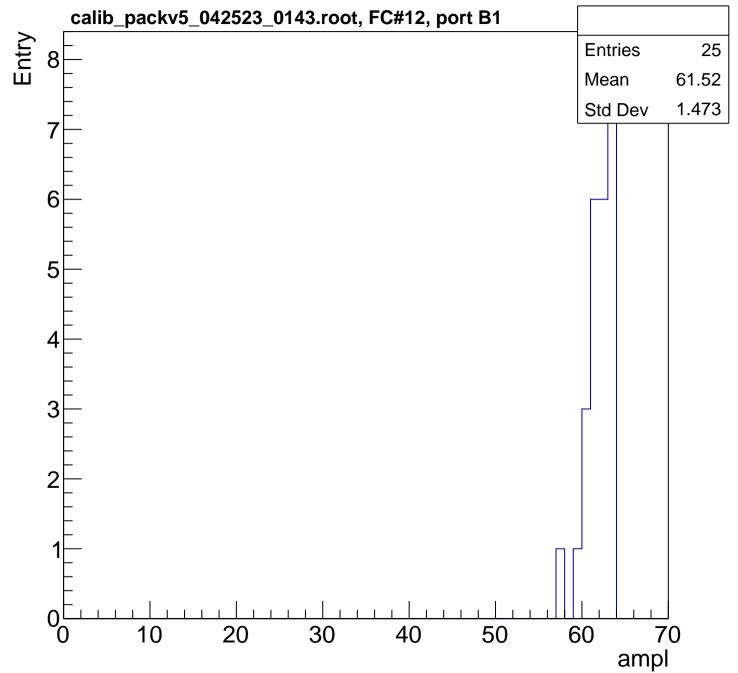


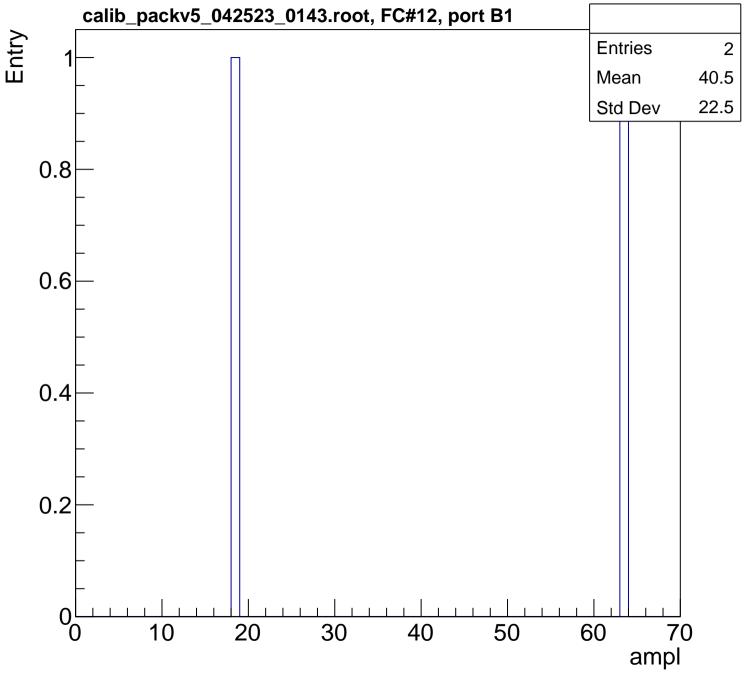


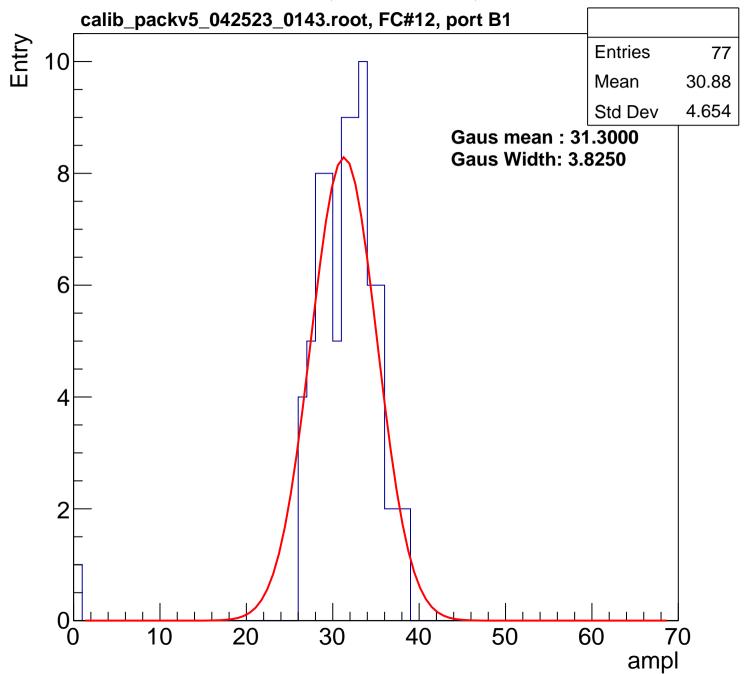


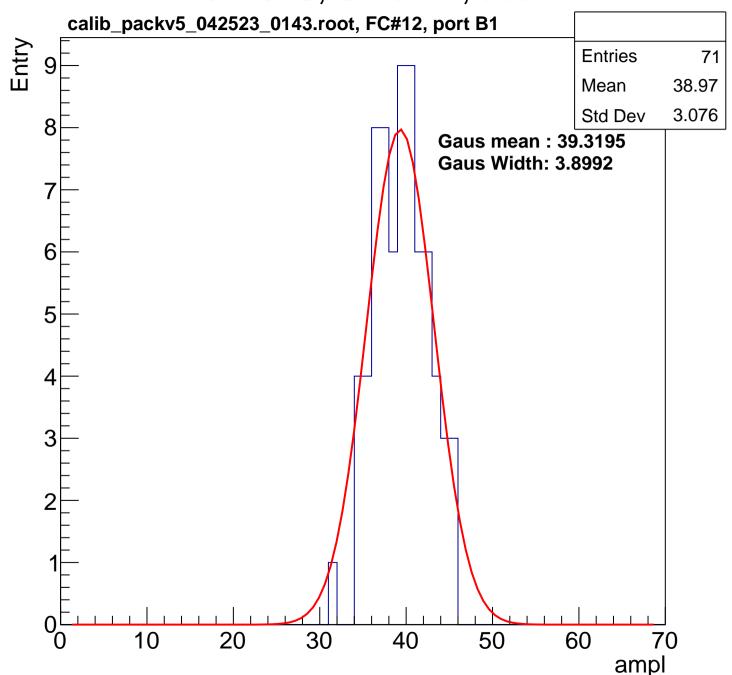


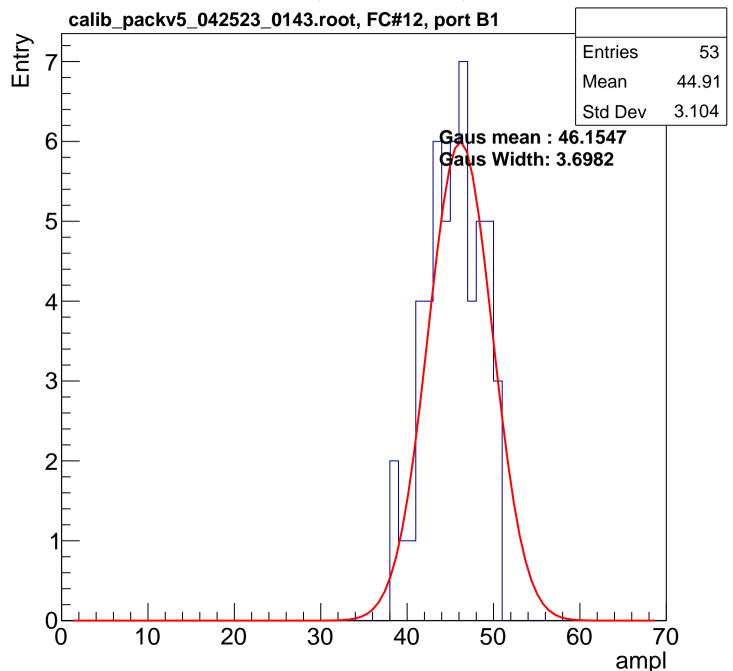


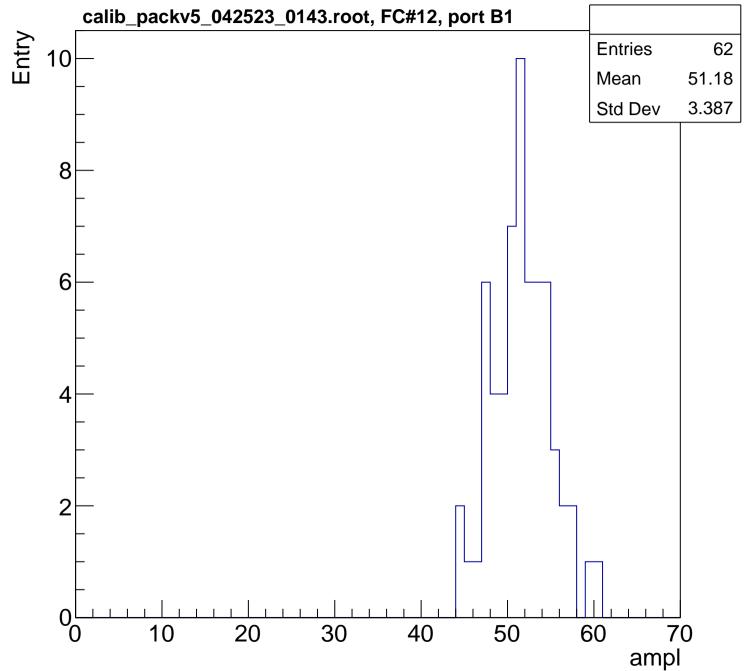


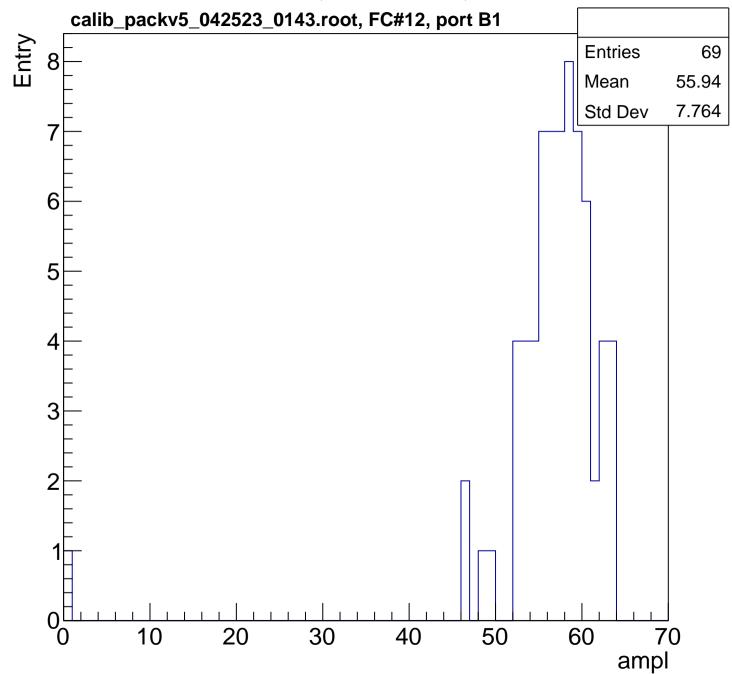


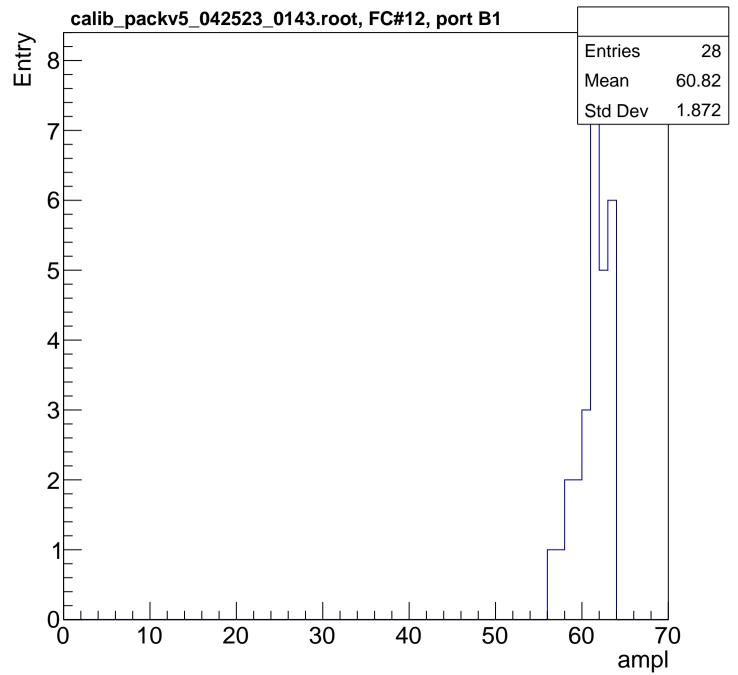




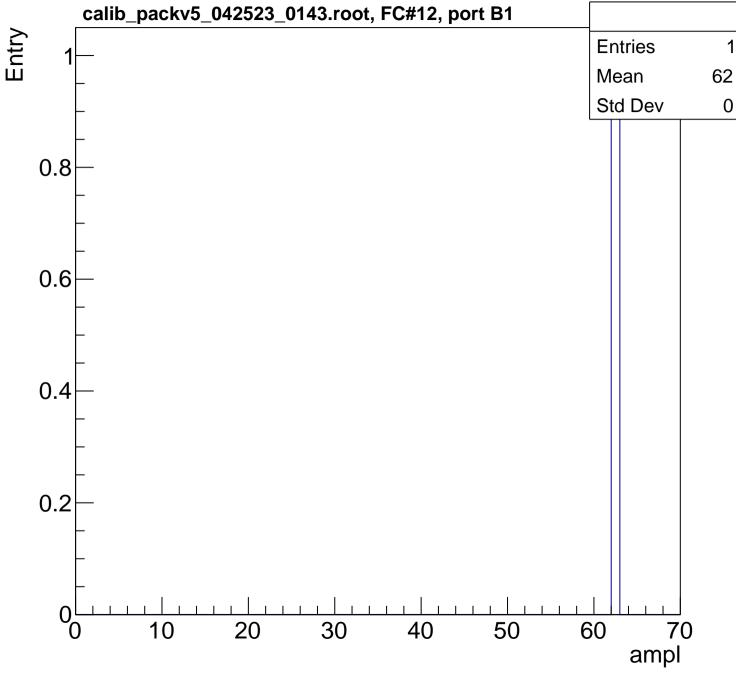


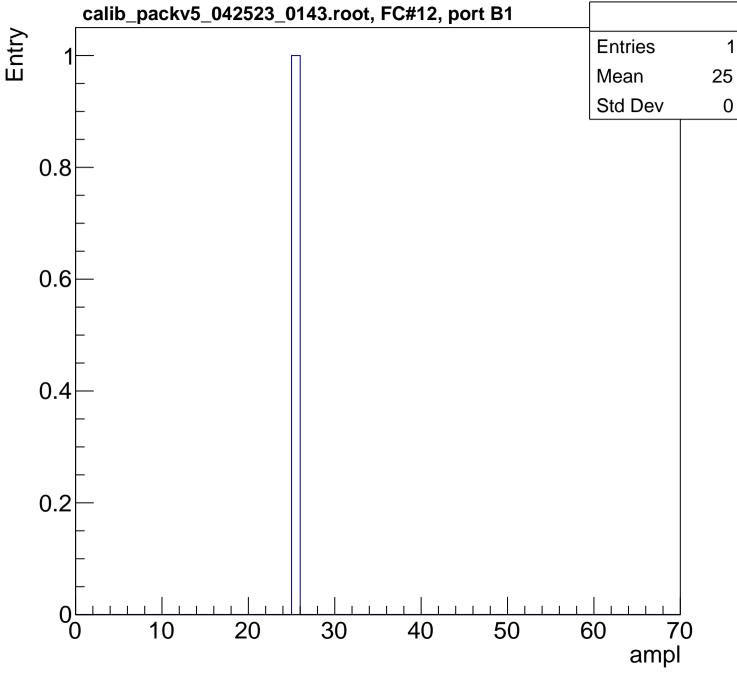


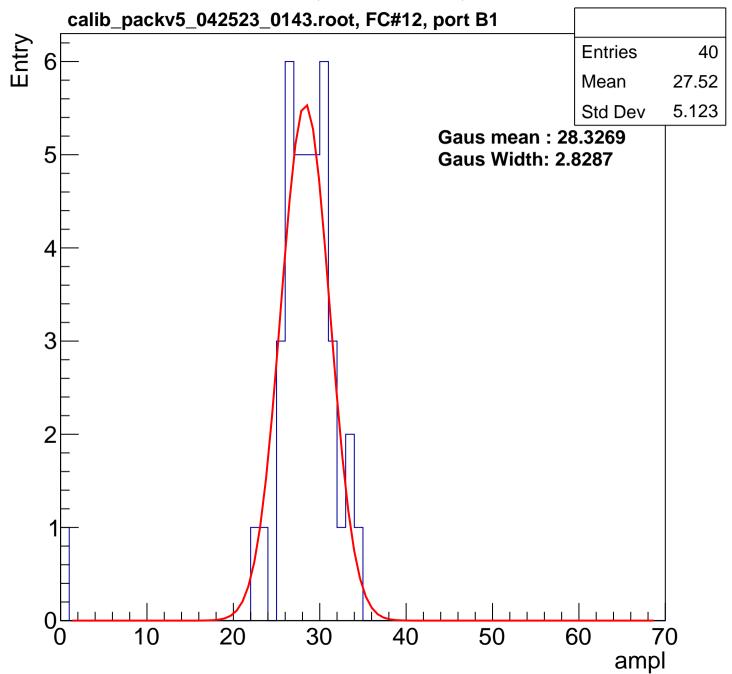


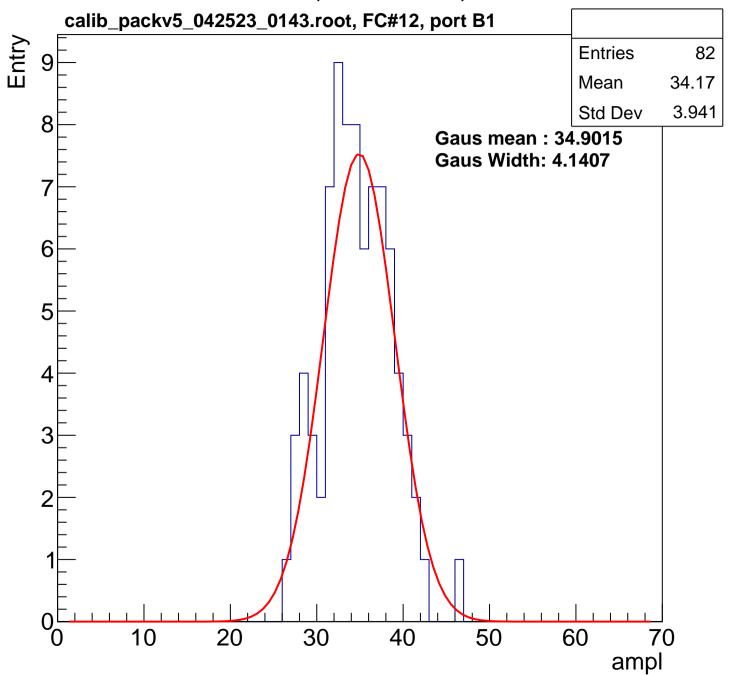


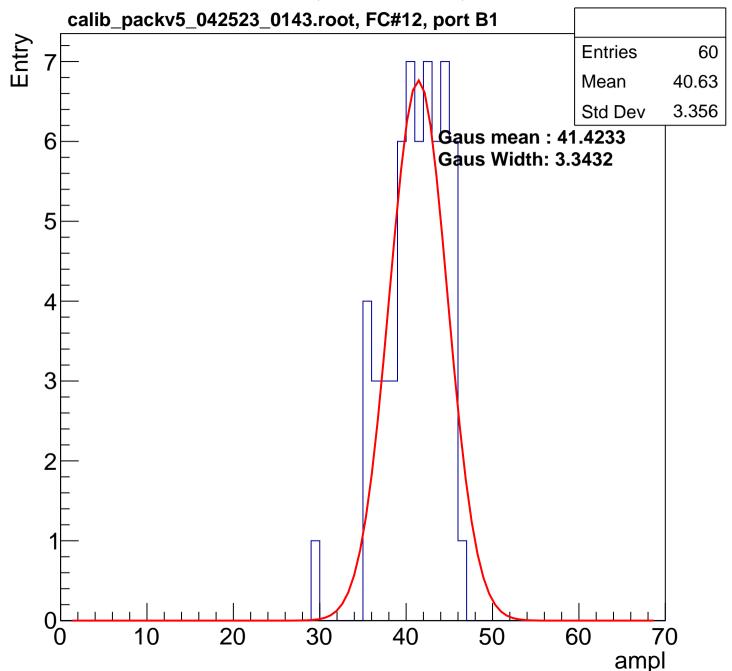
0

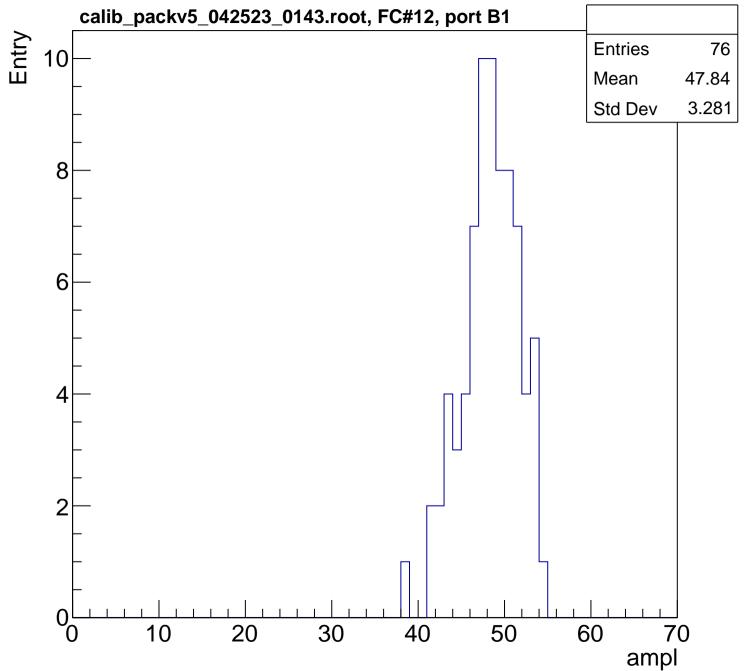


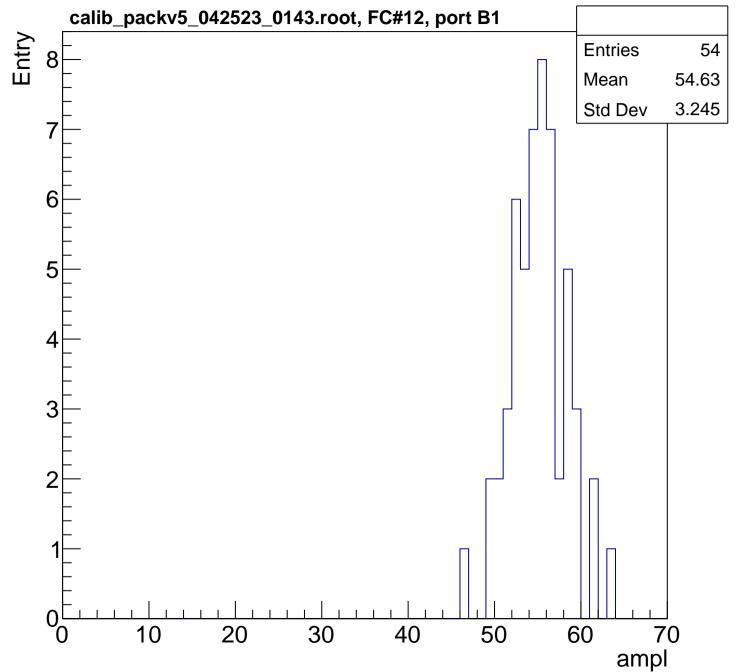


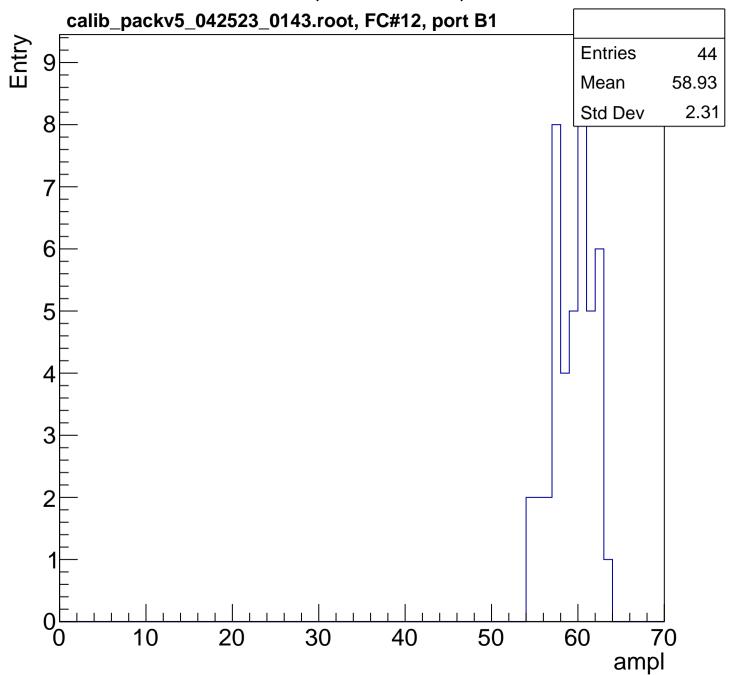


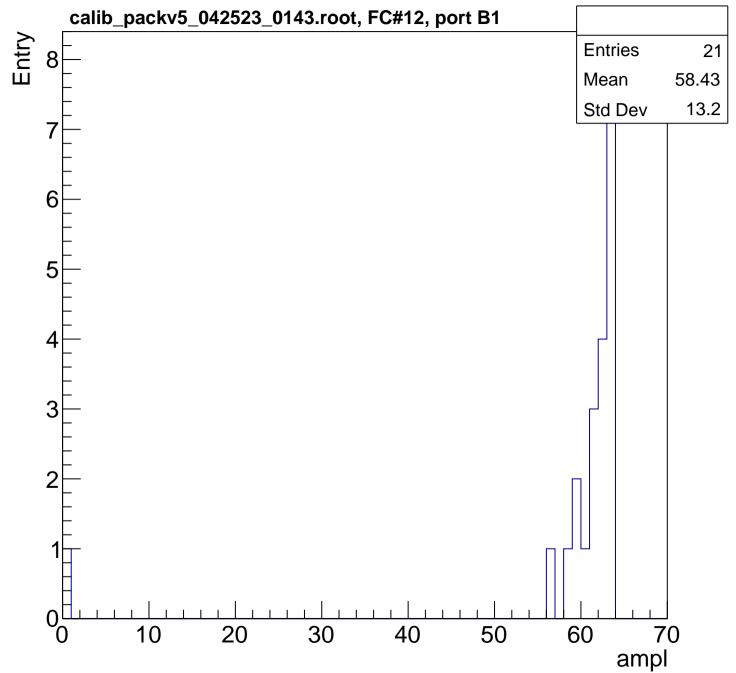




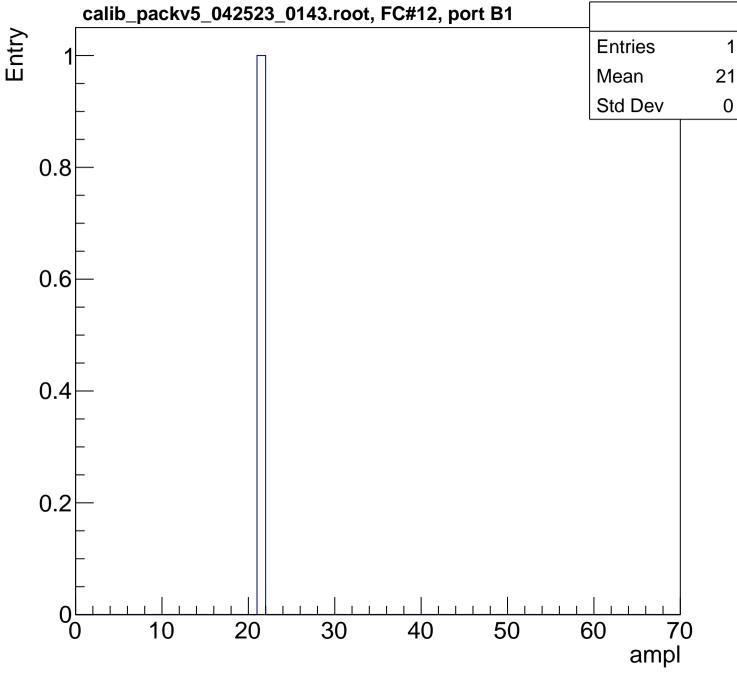


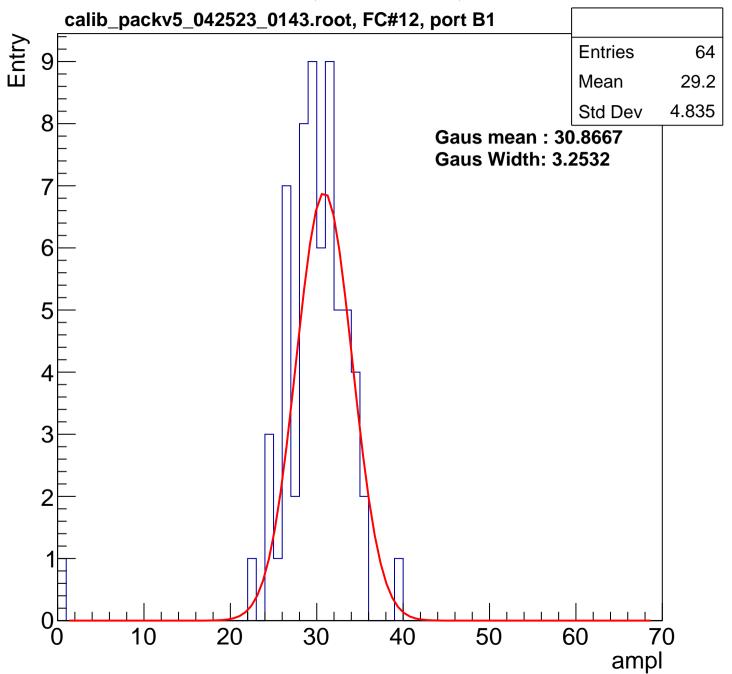


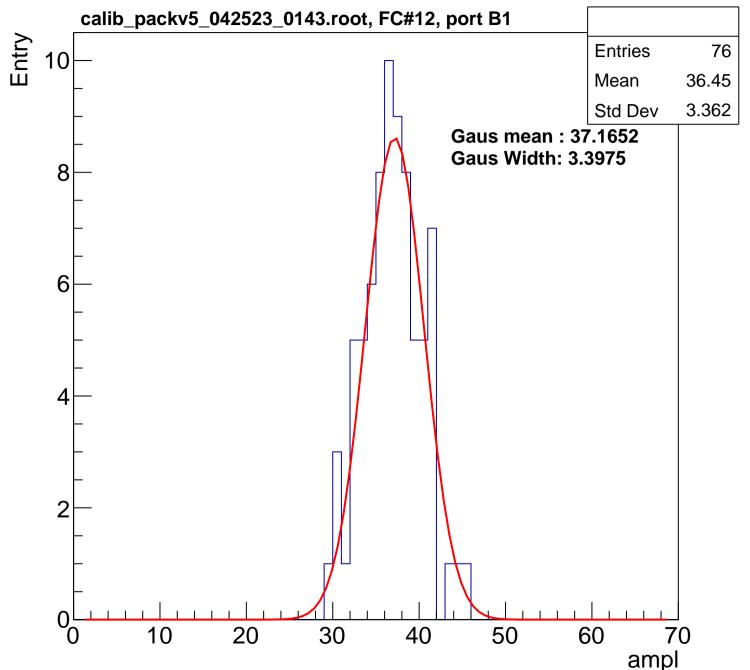


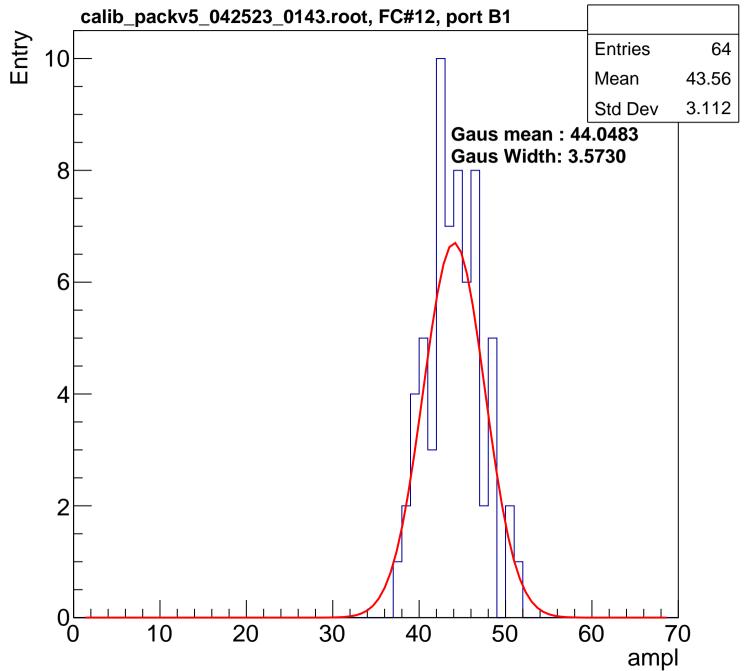


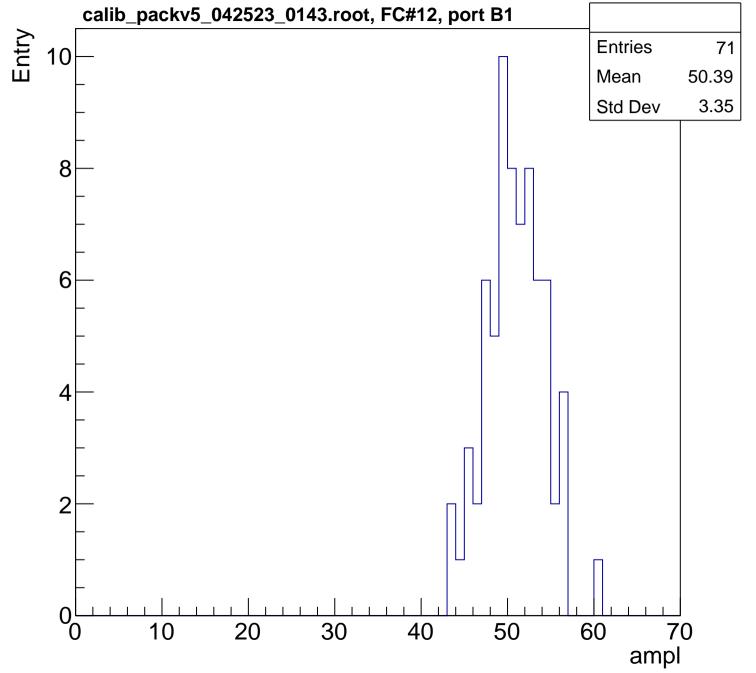
0

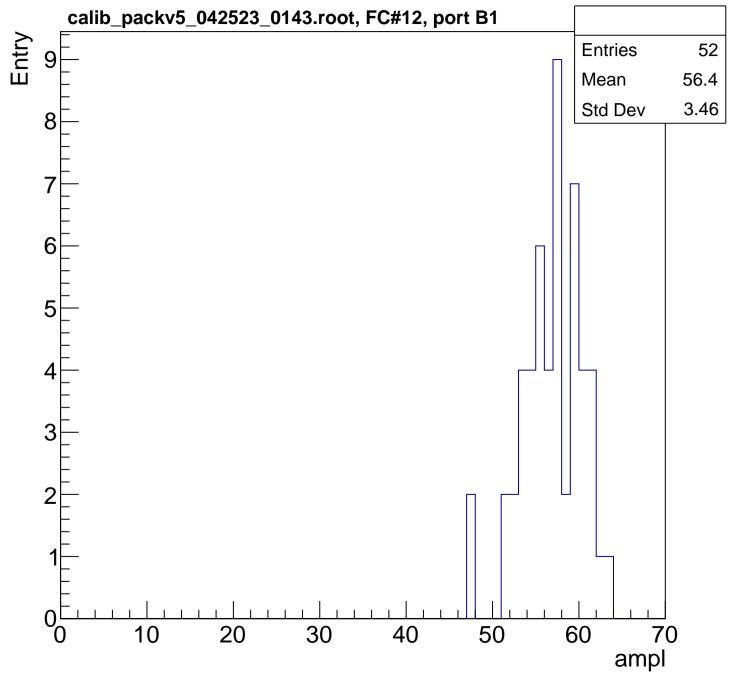


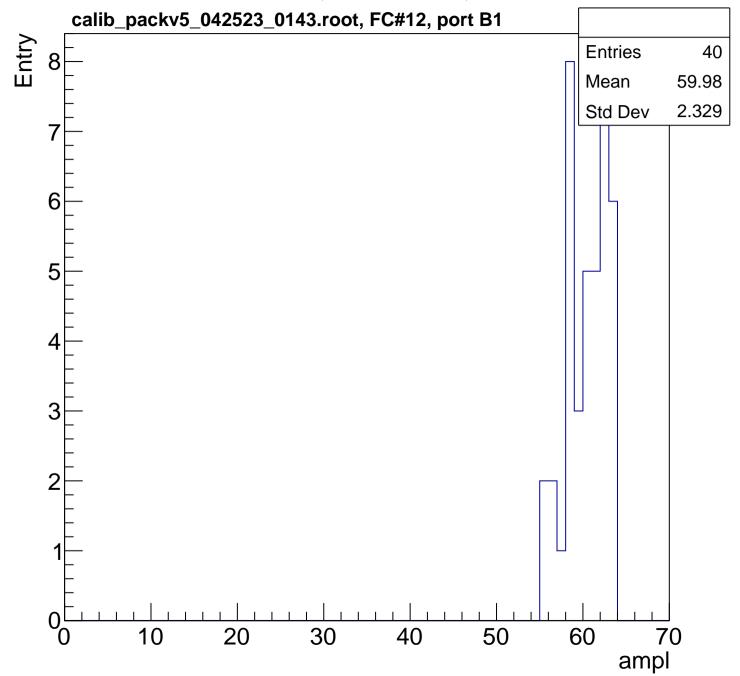


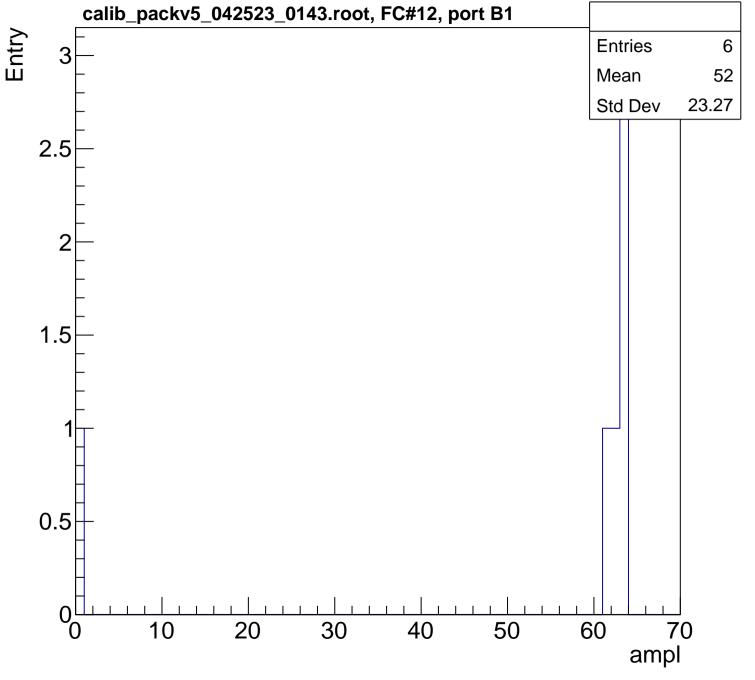


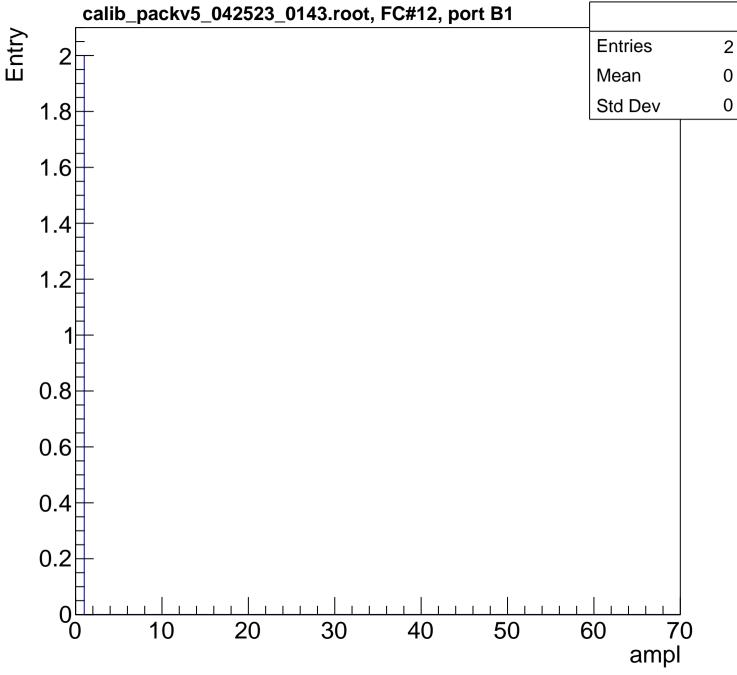


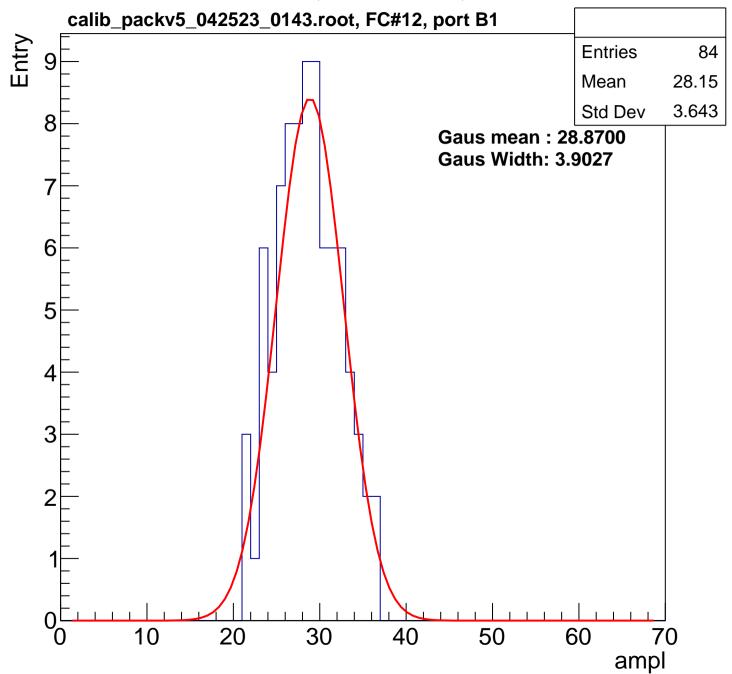


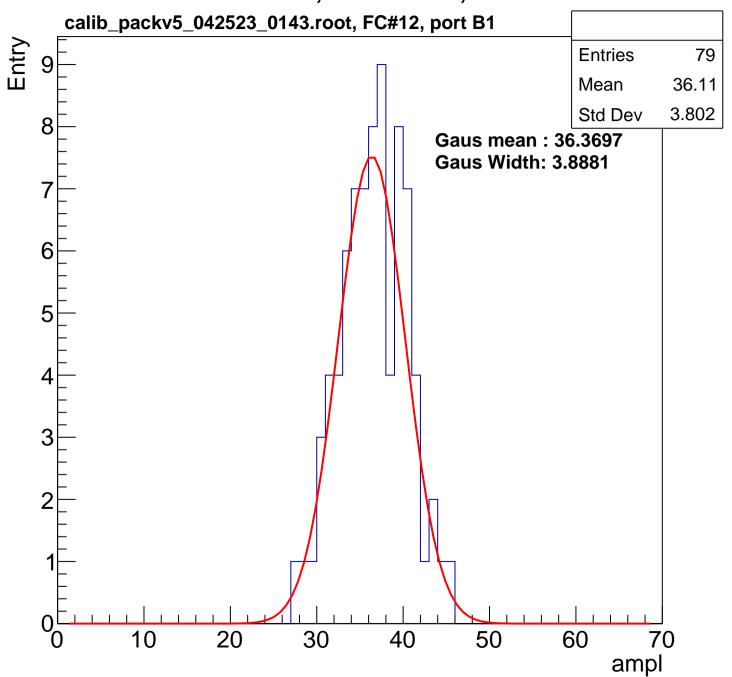


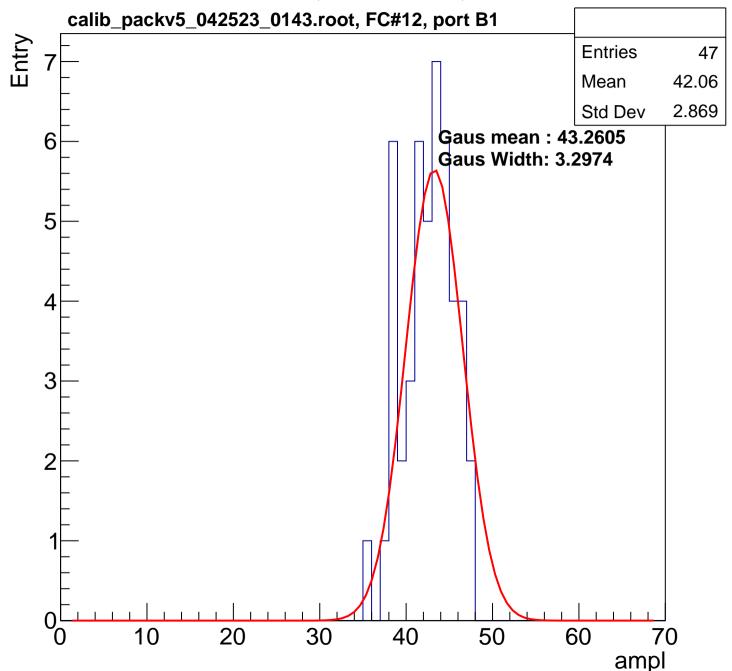


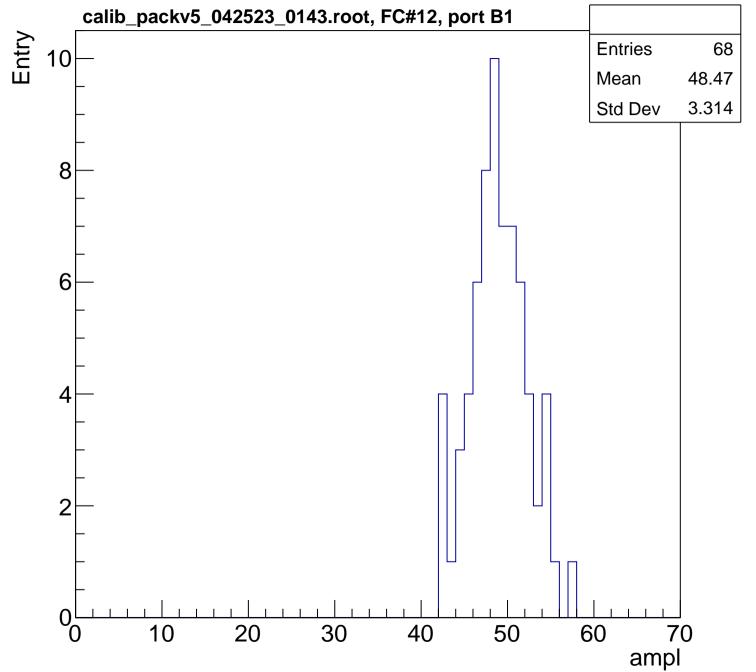


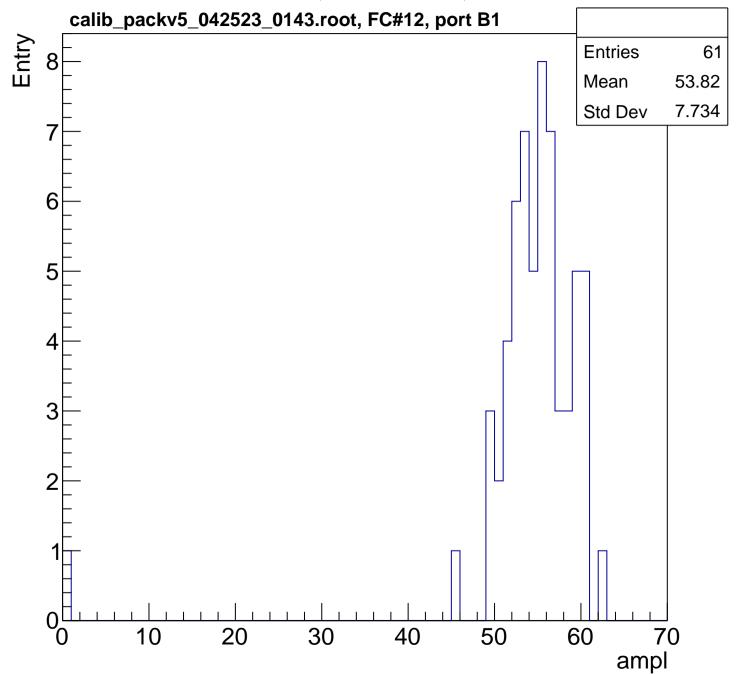


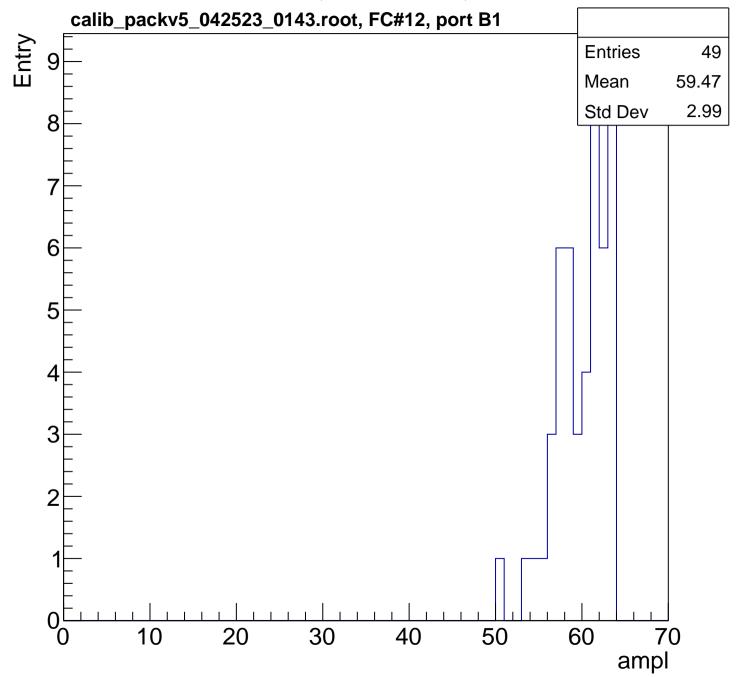


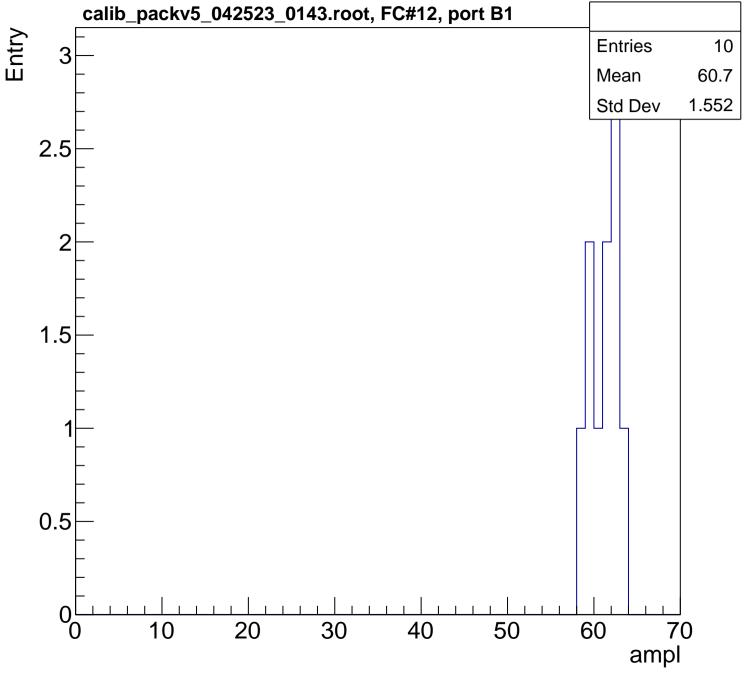






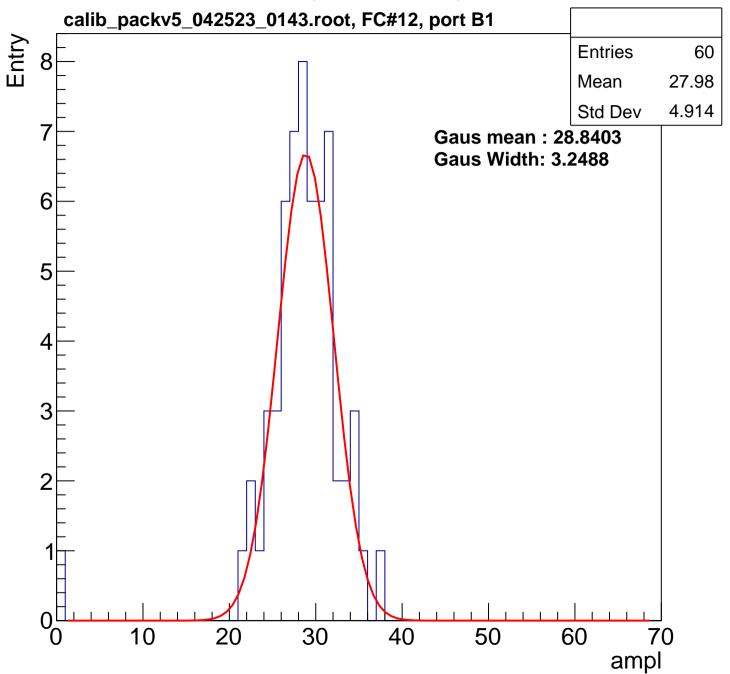


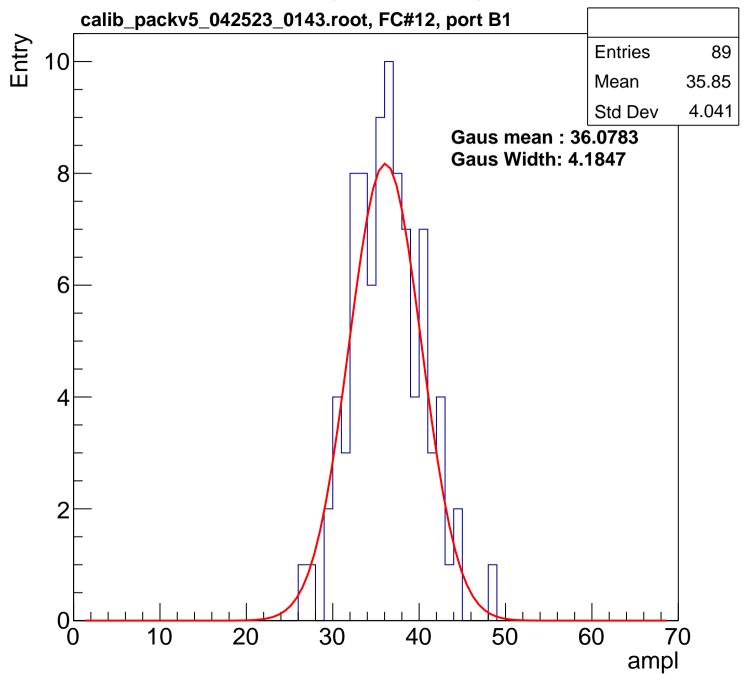


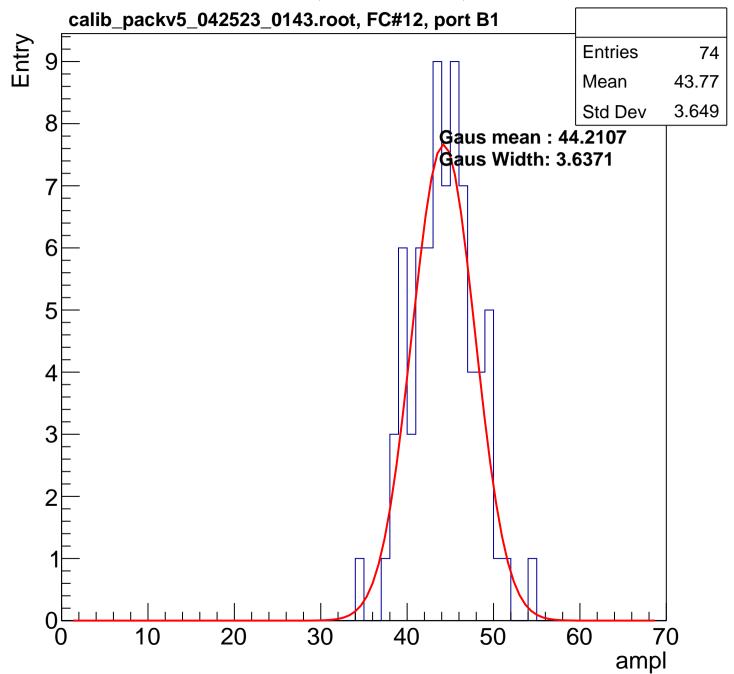


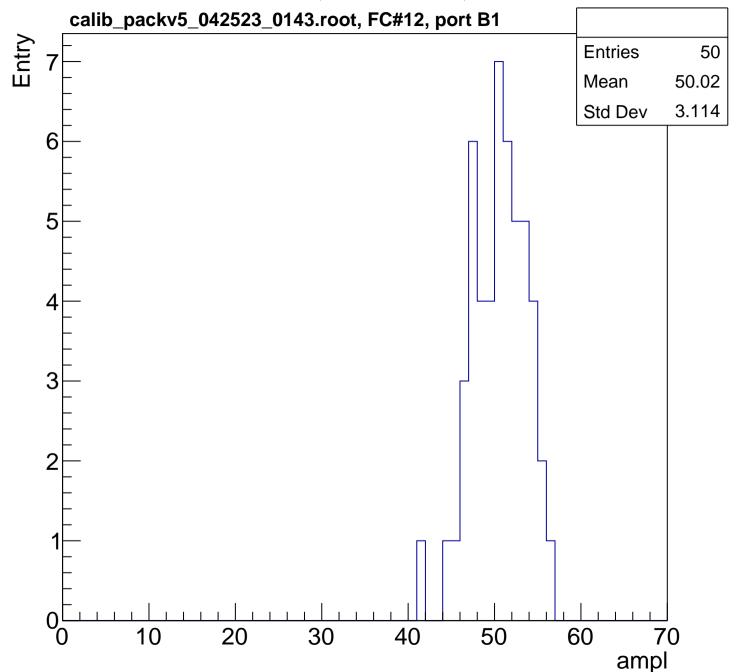
B0L102S, U7-ch24, adc7 calib_packv5_042523_0143.root, FC#12, port B1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70

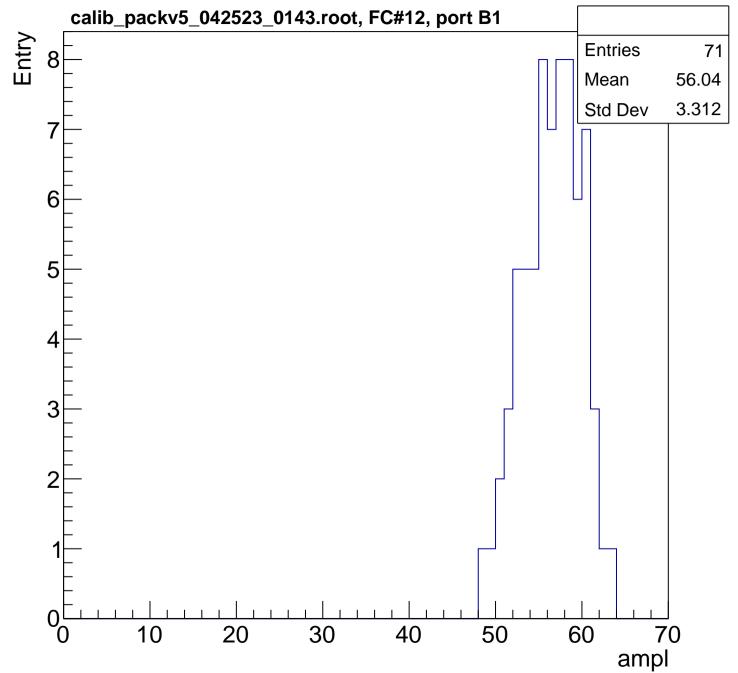
ampl

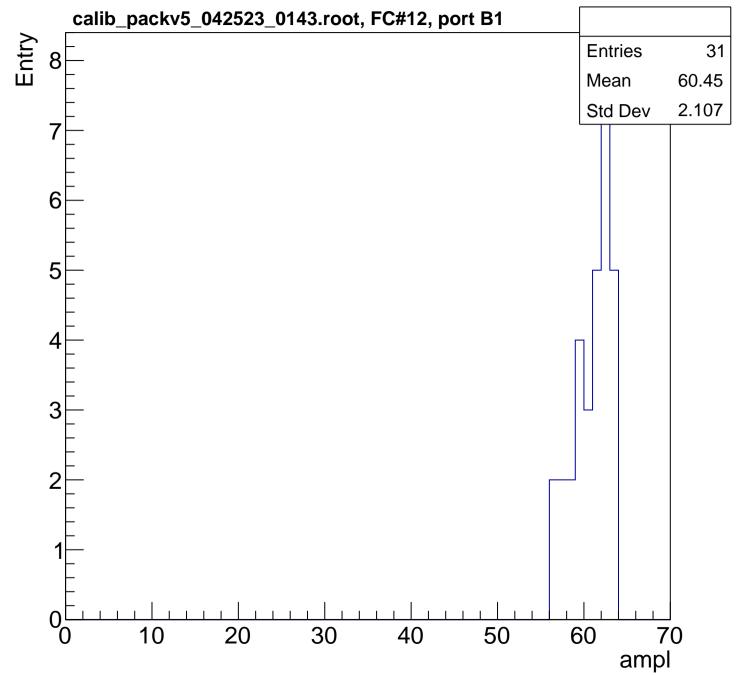


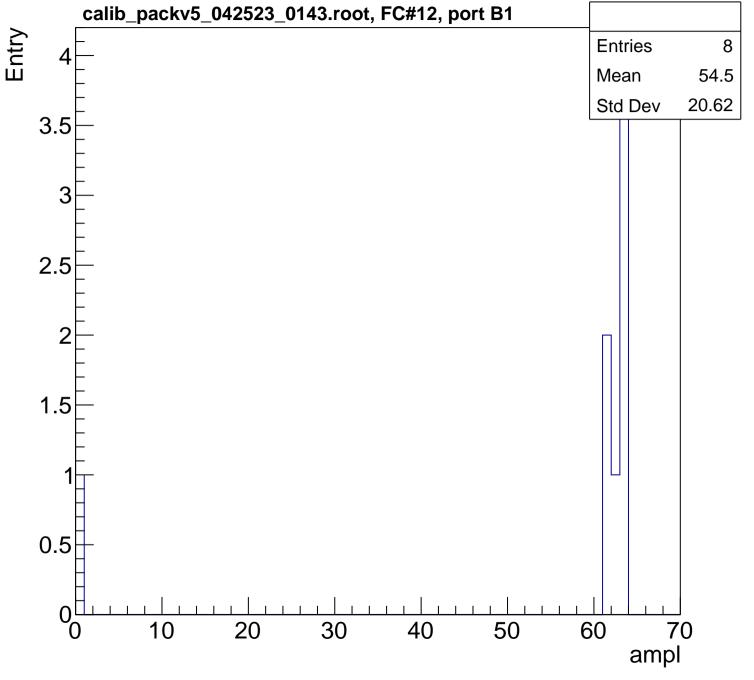


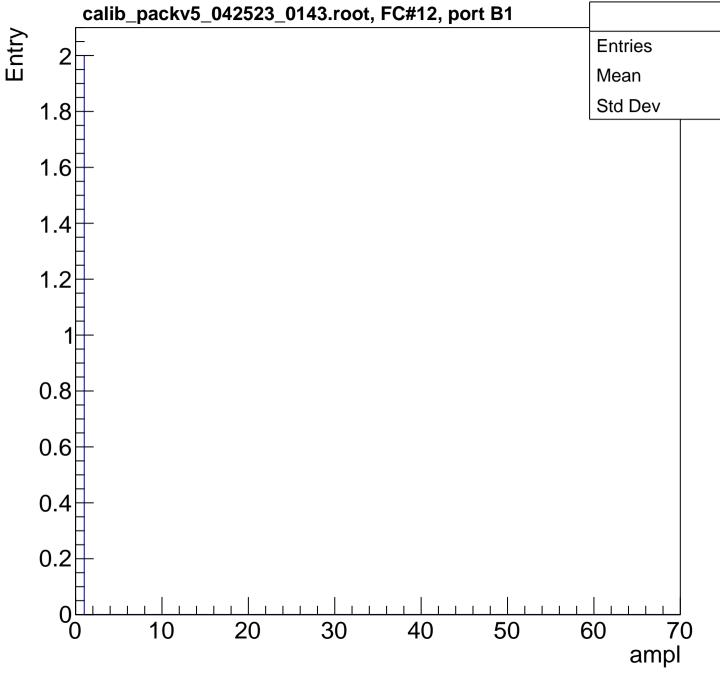


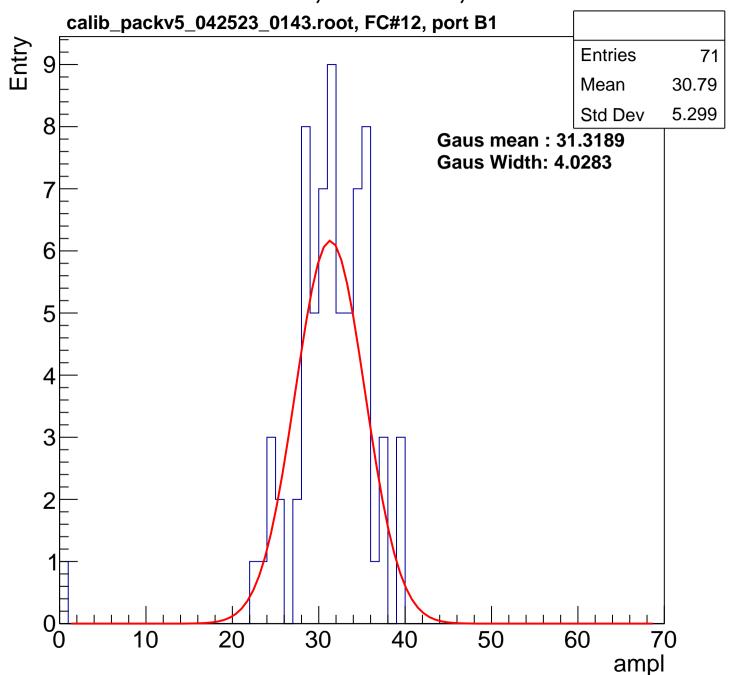


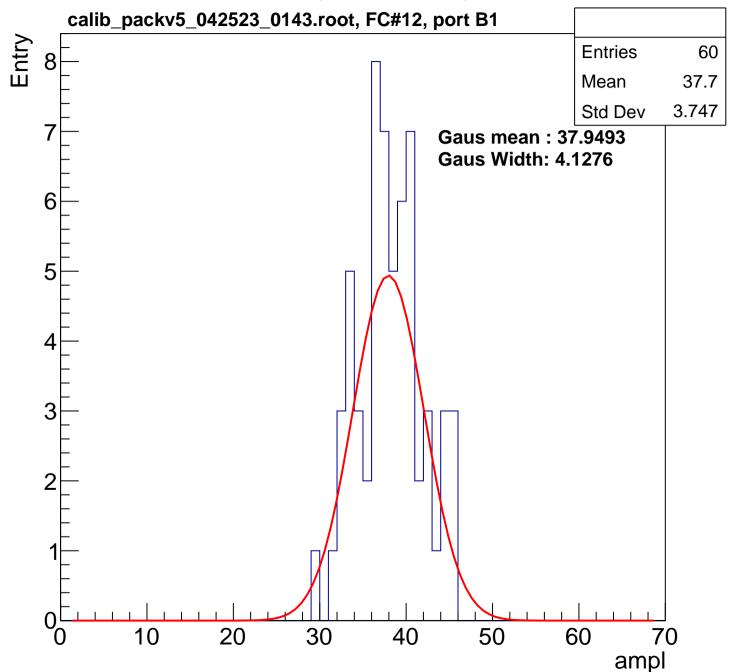


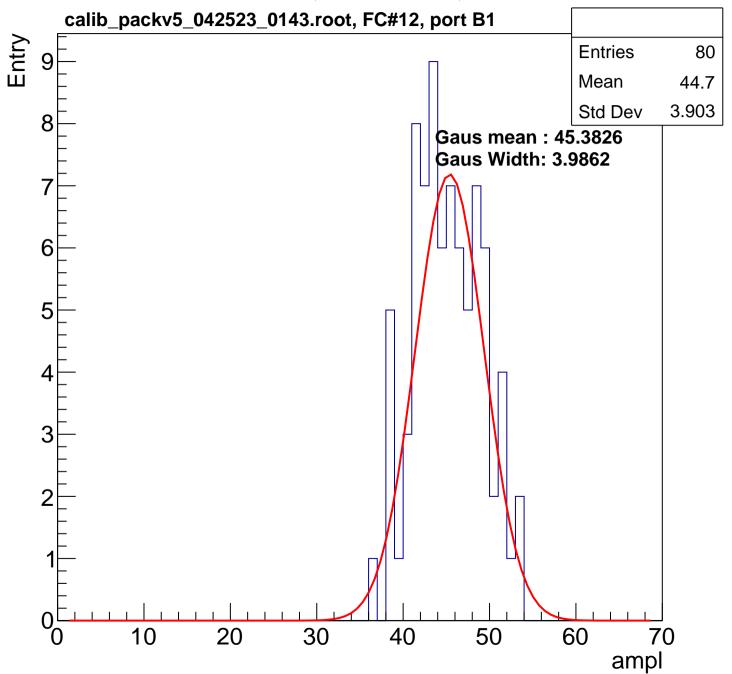


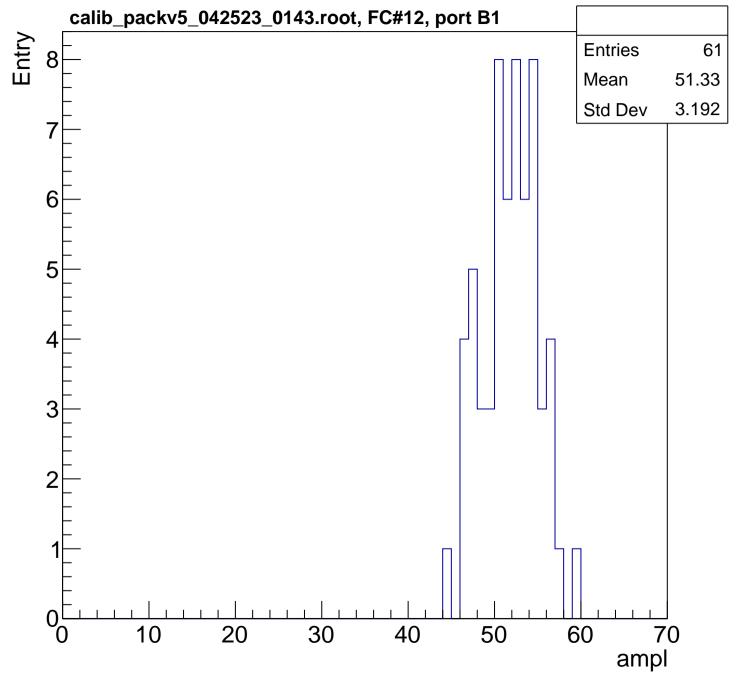


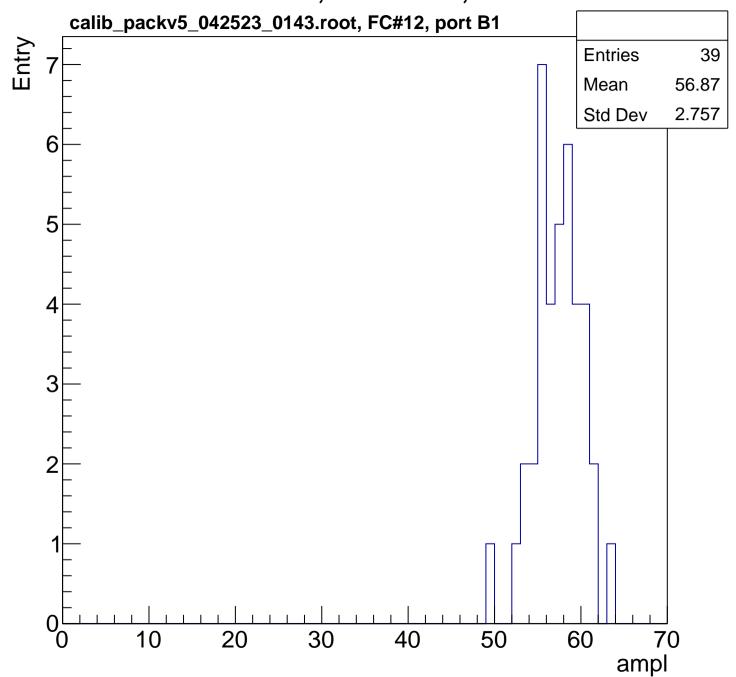


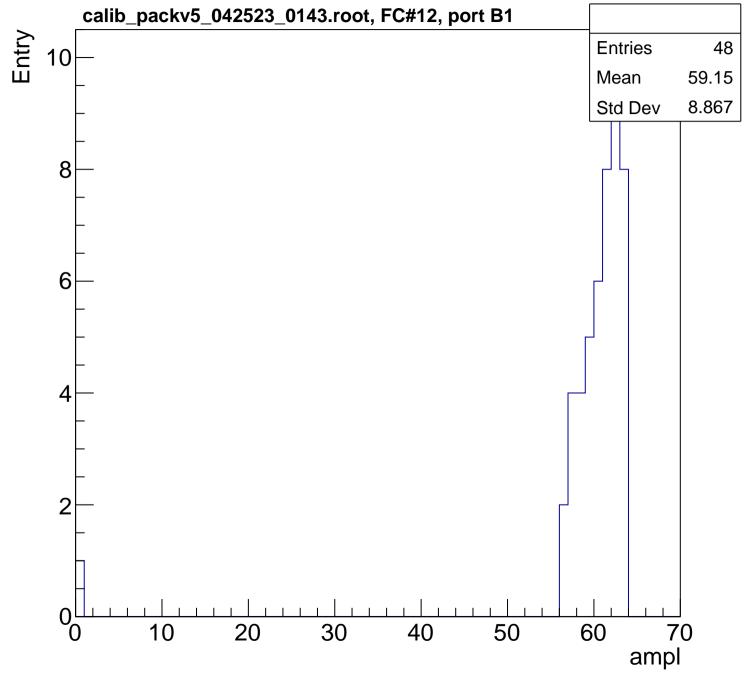


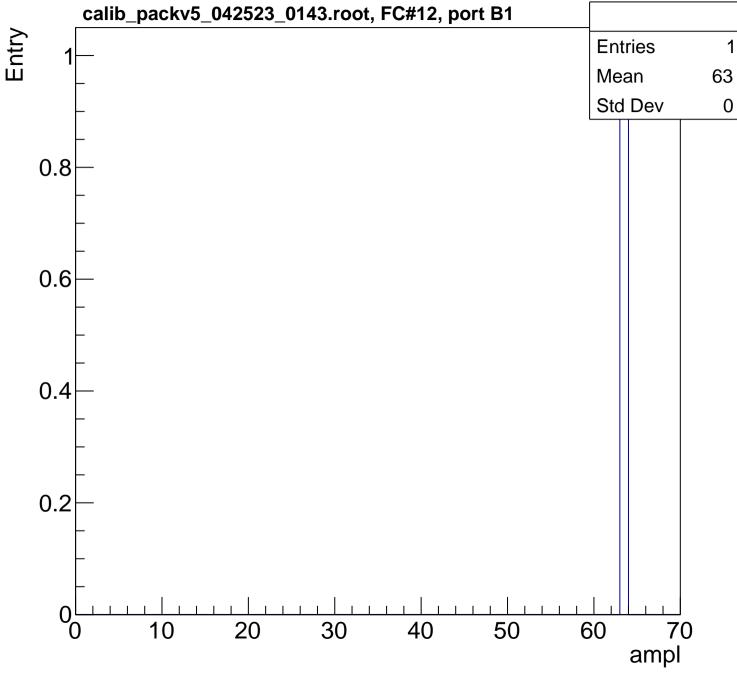




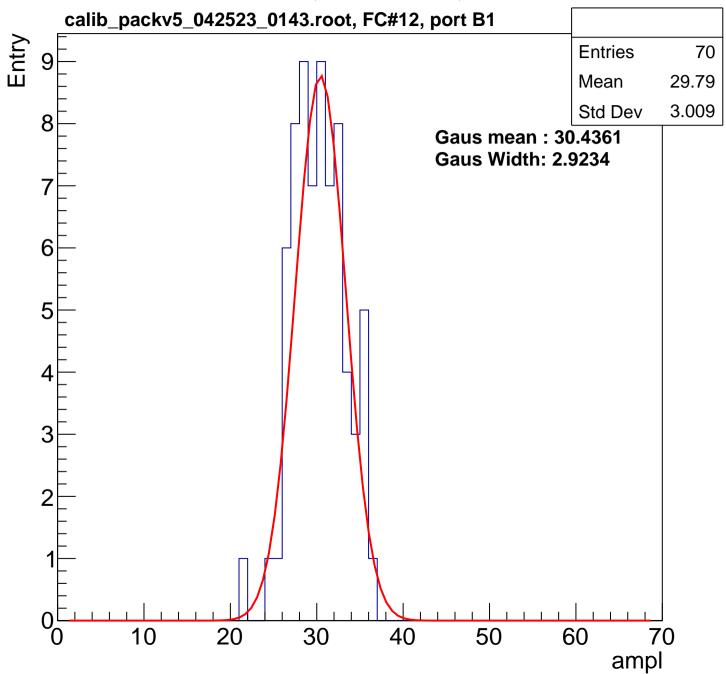


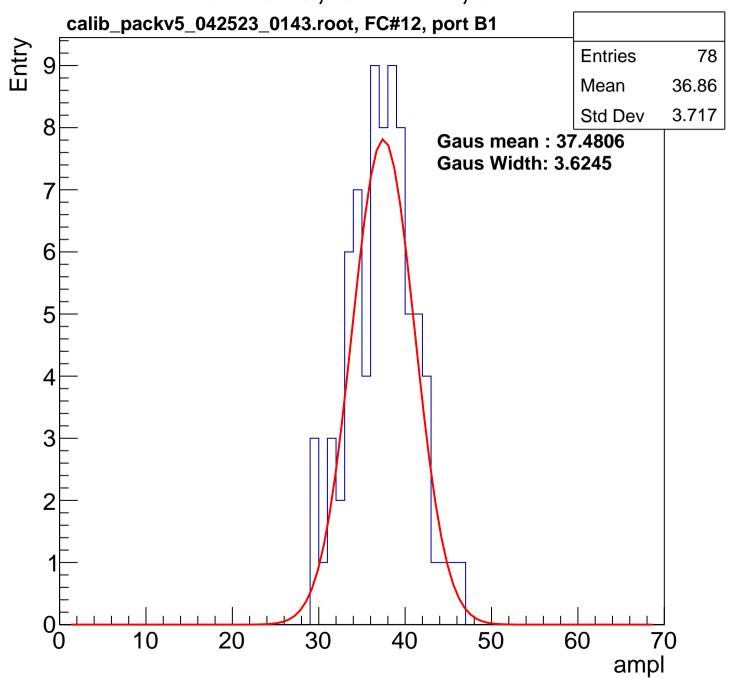


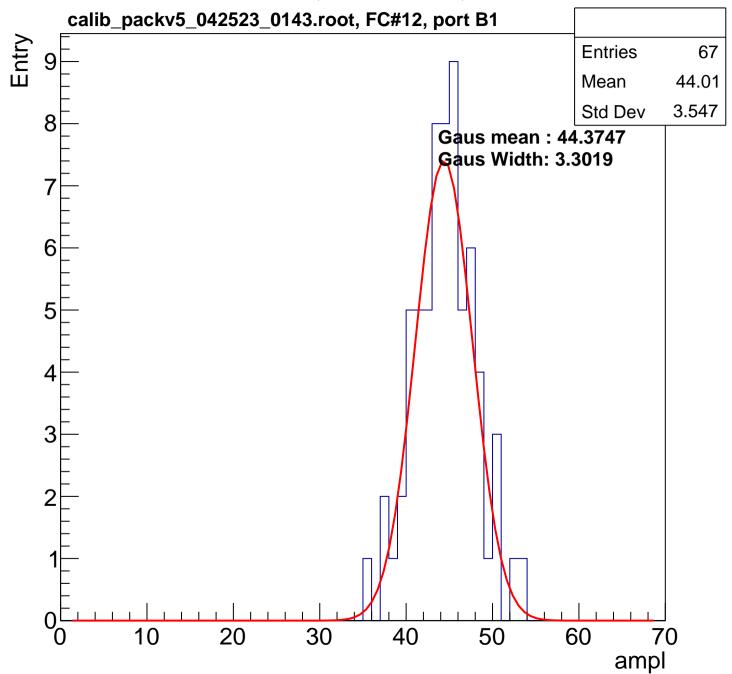


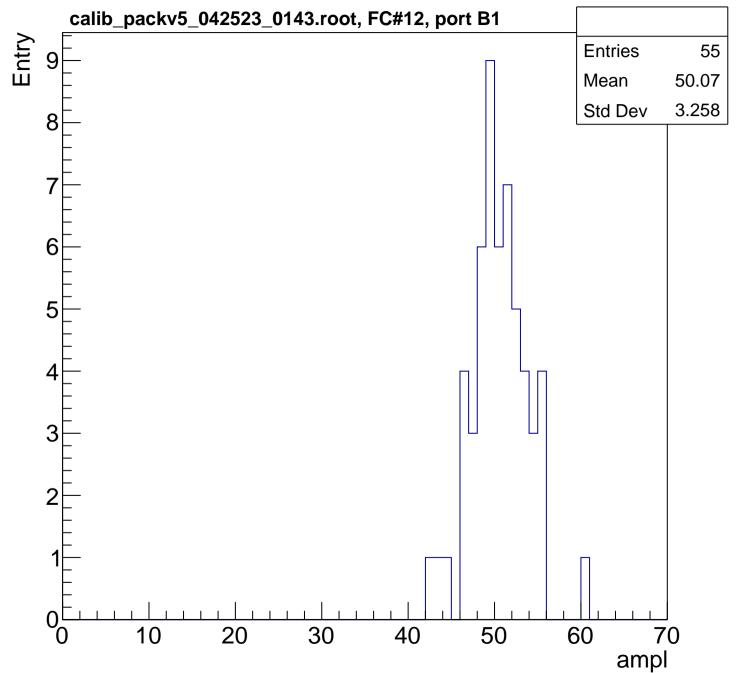


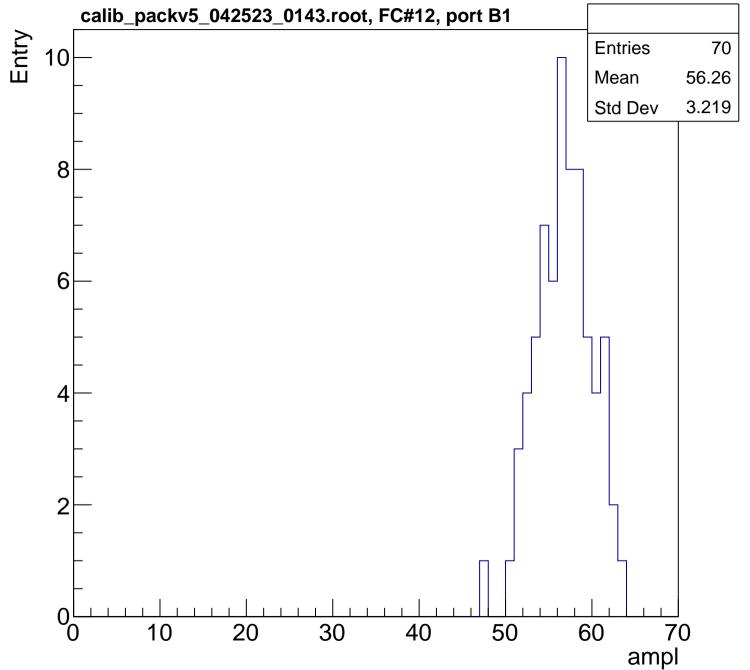


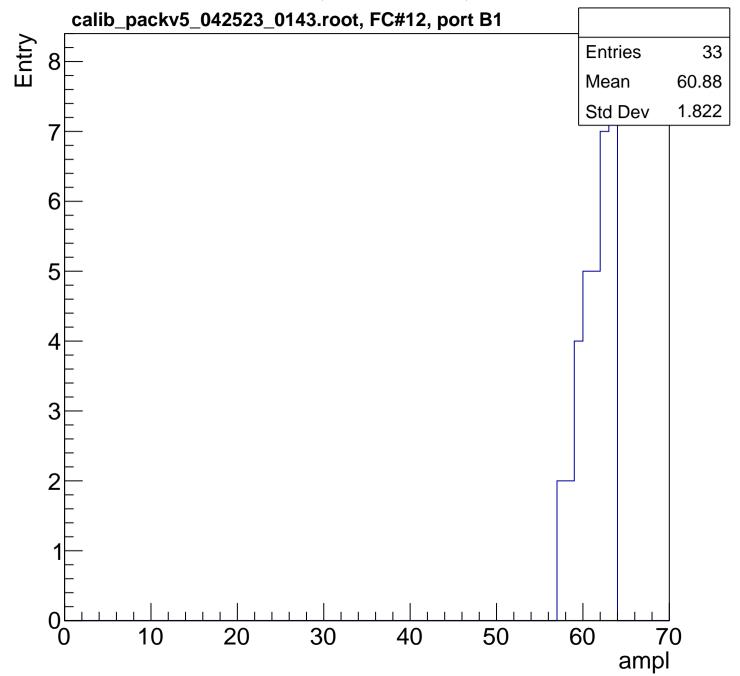


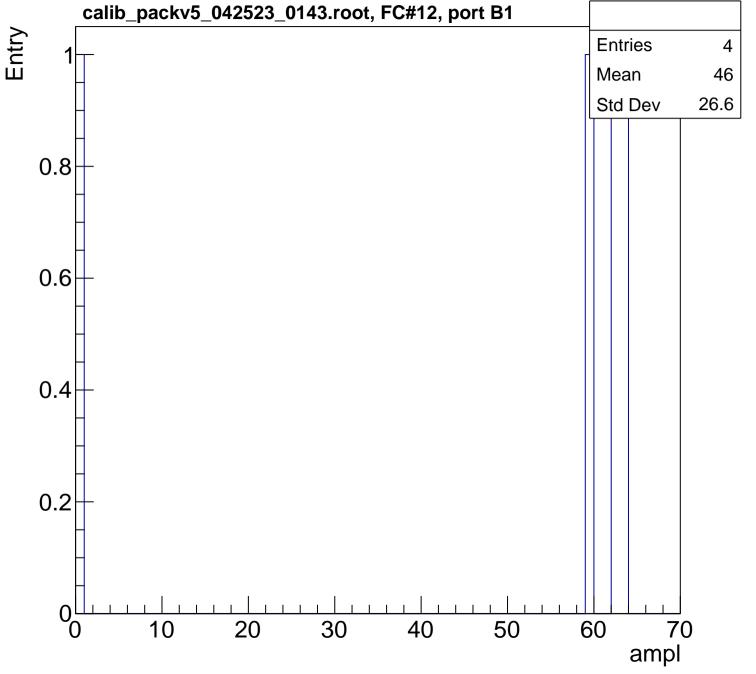


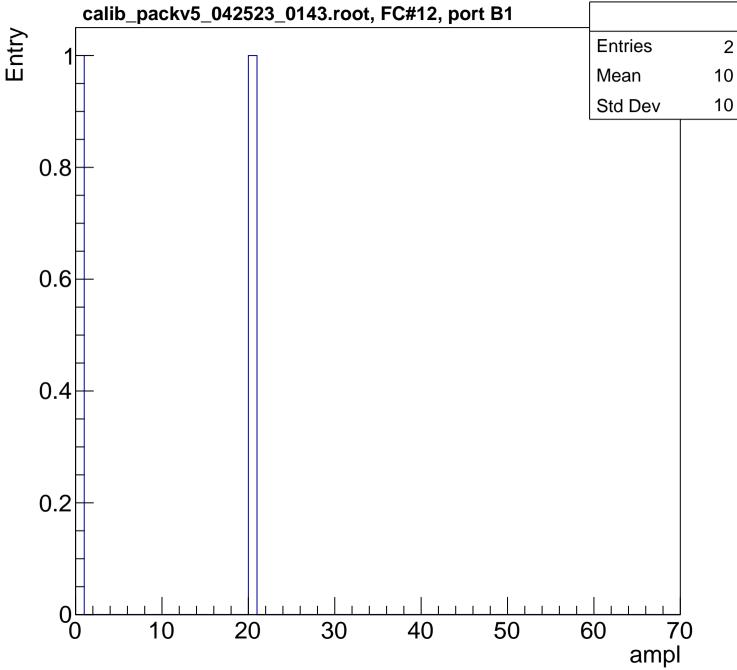


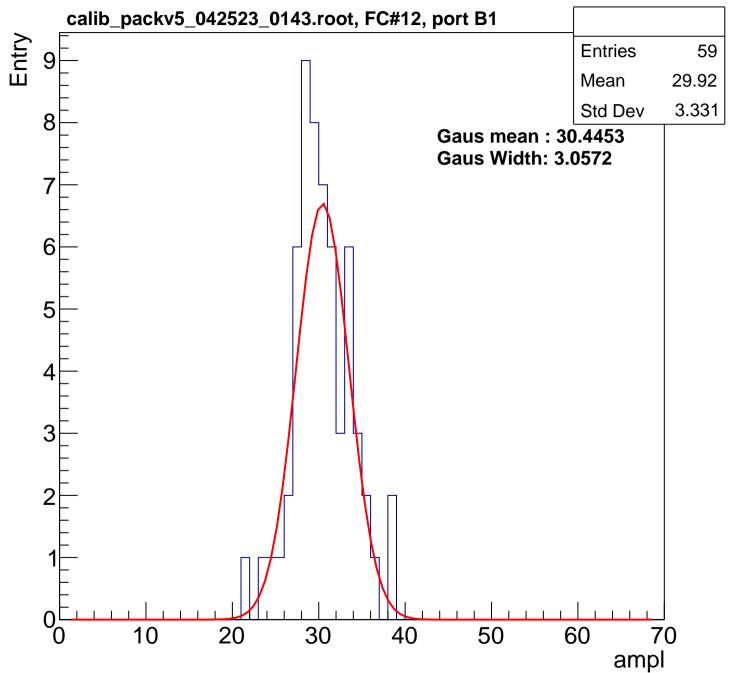


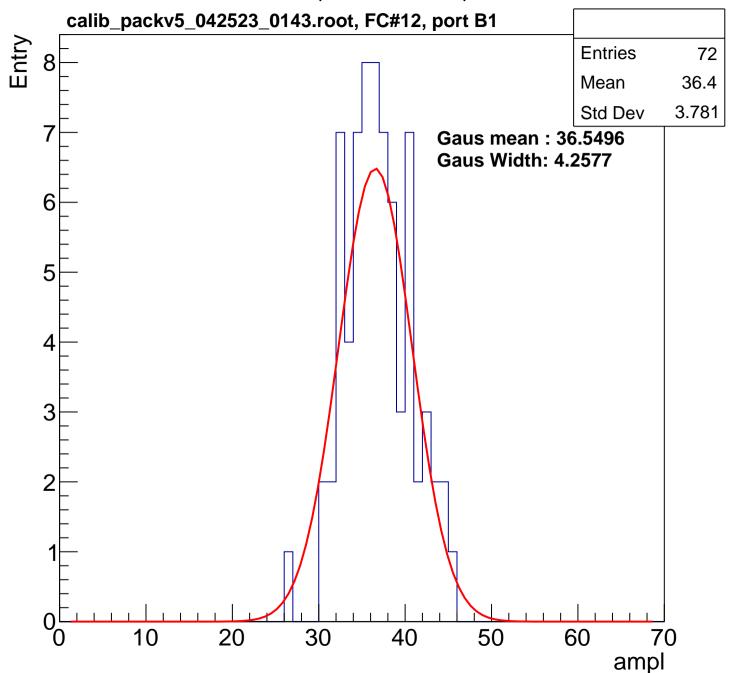


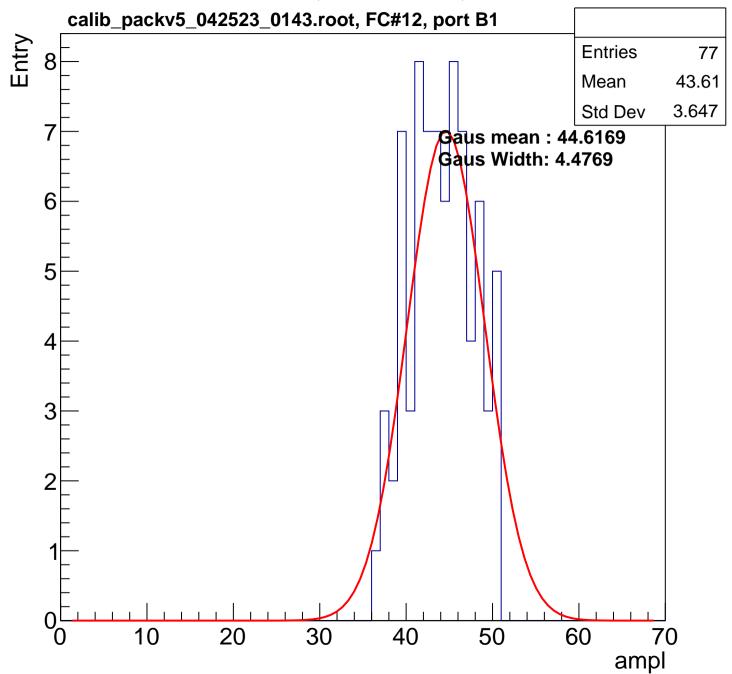


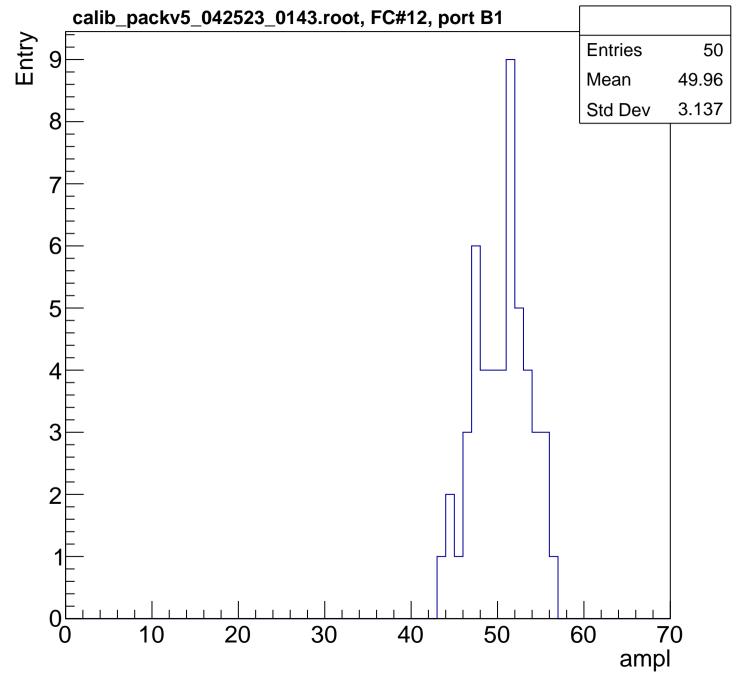


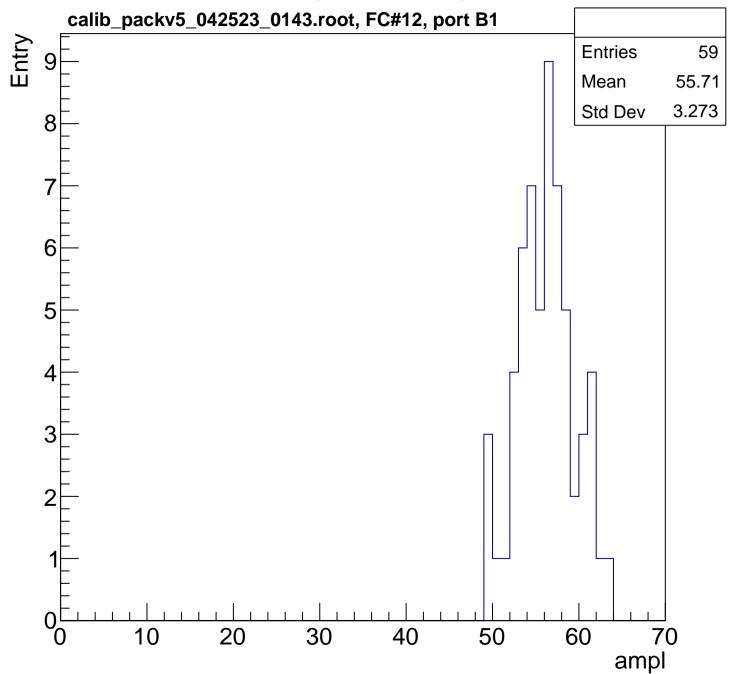


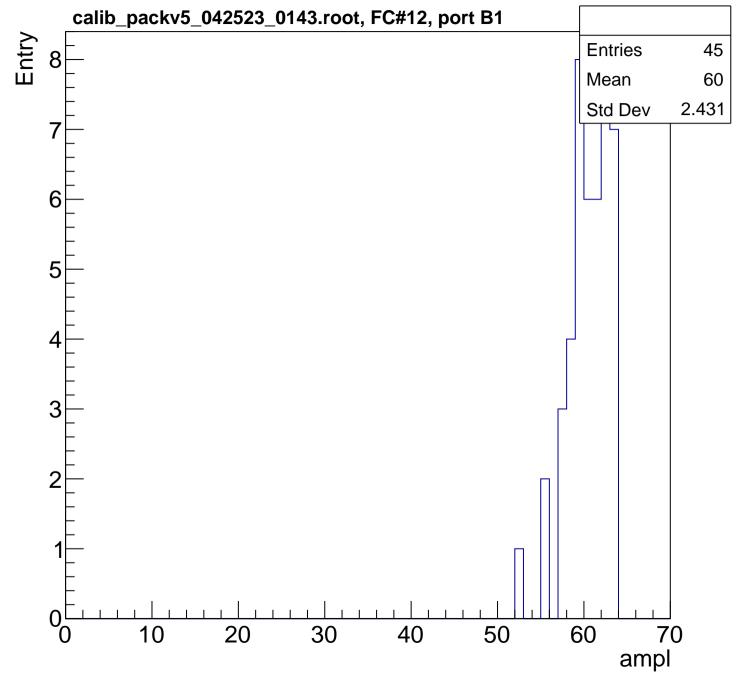


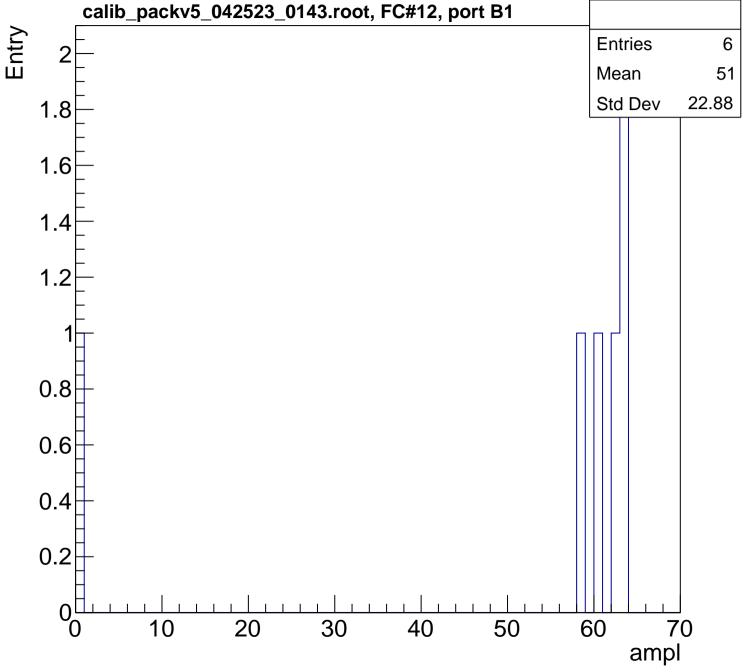




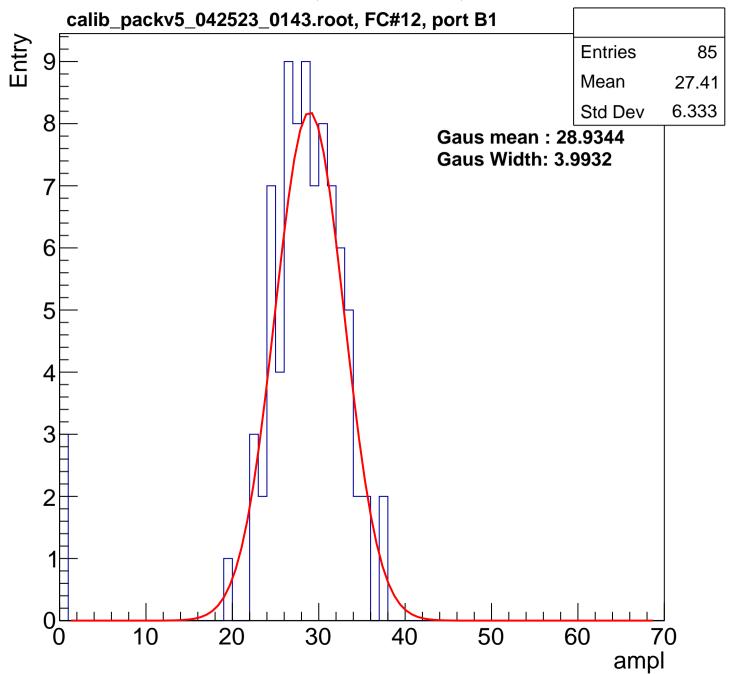


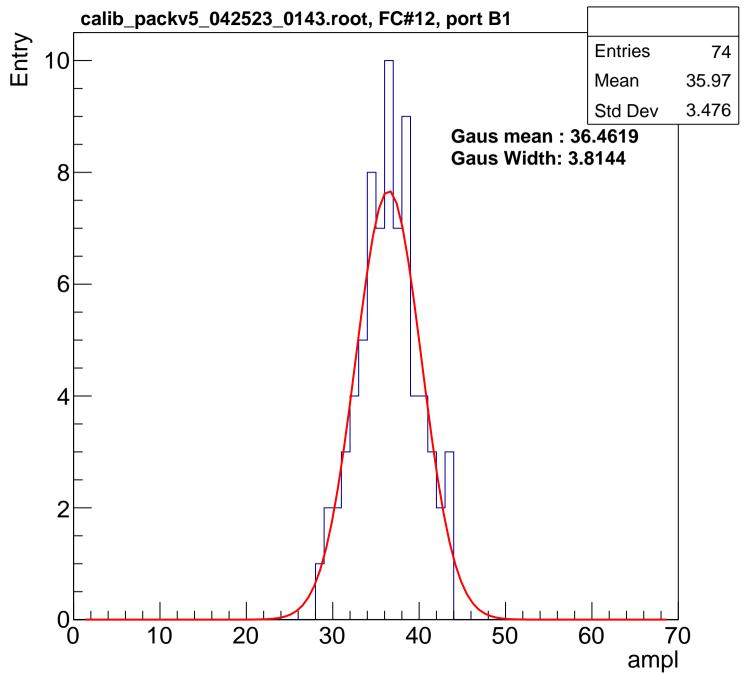


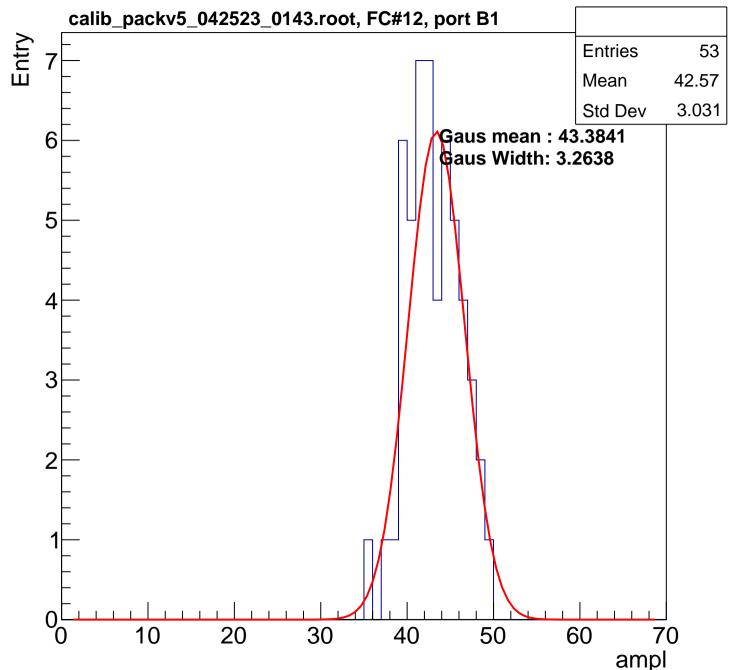


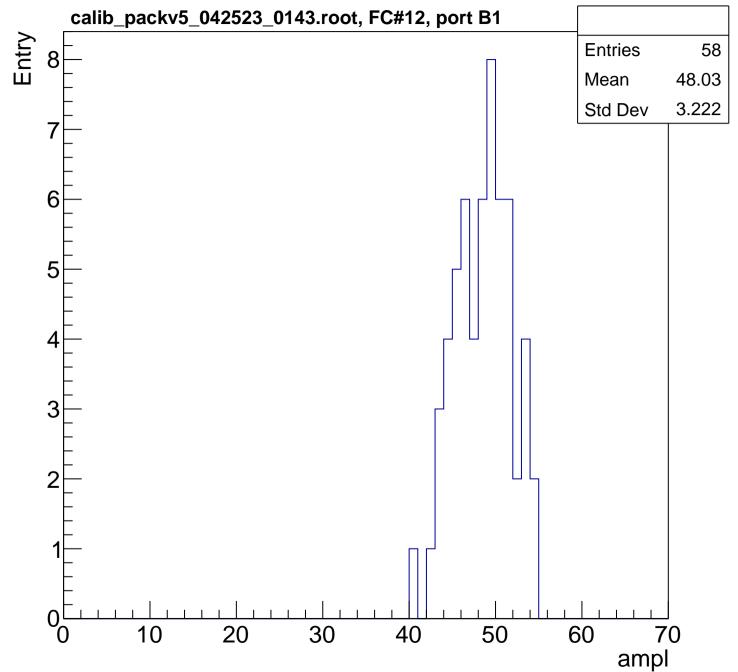


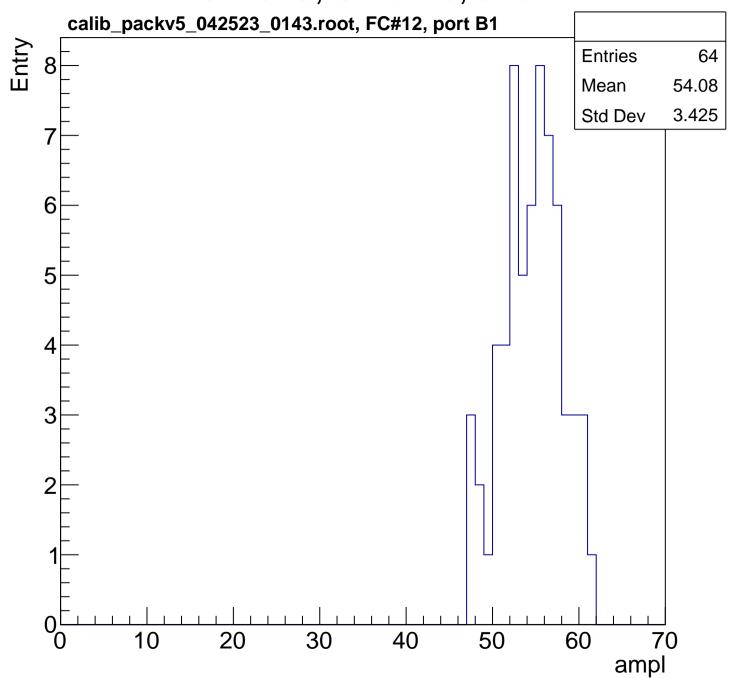


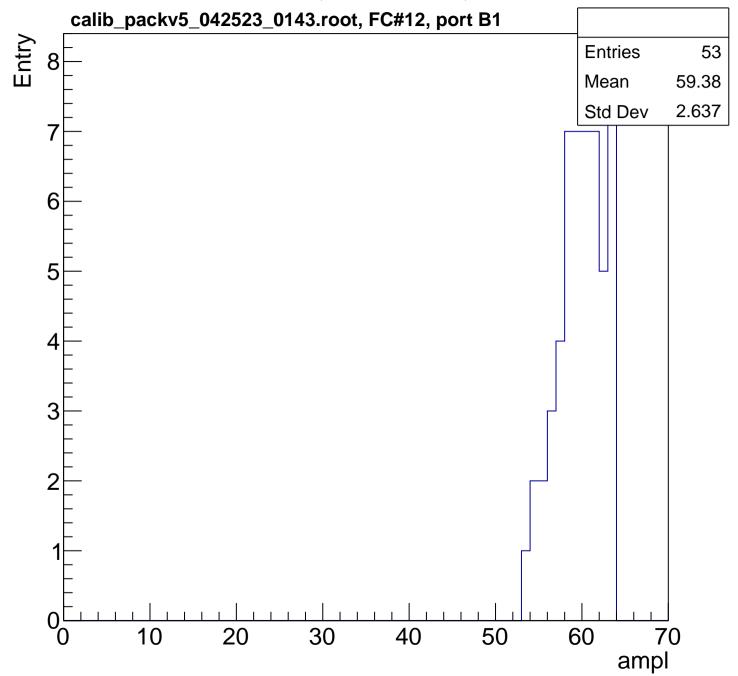


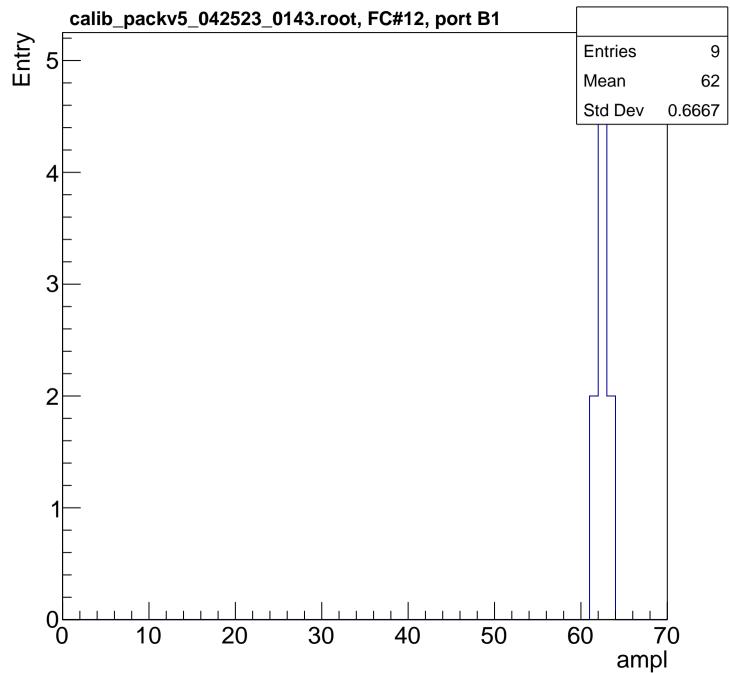


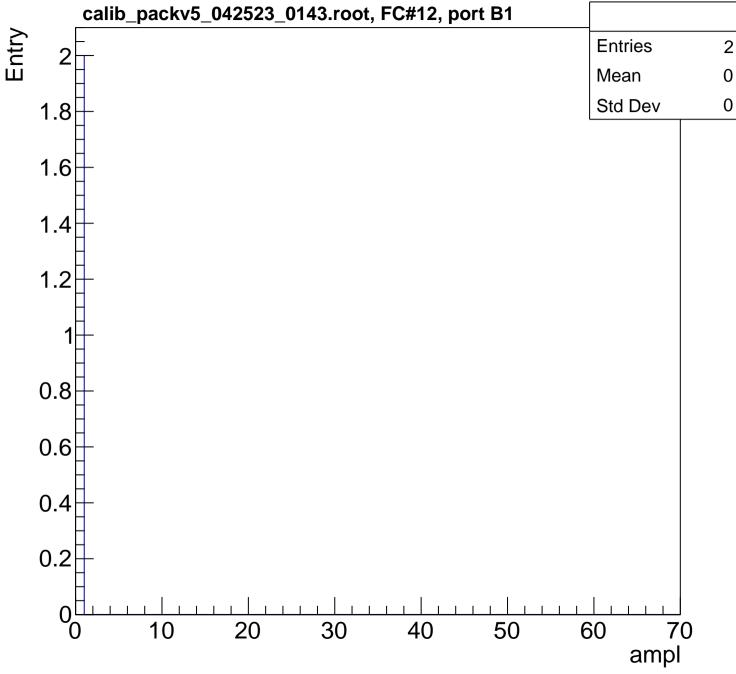


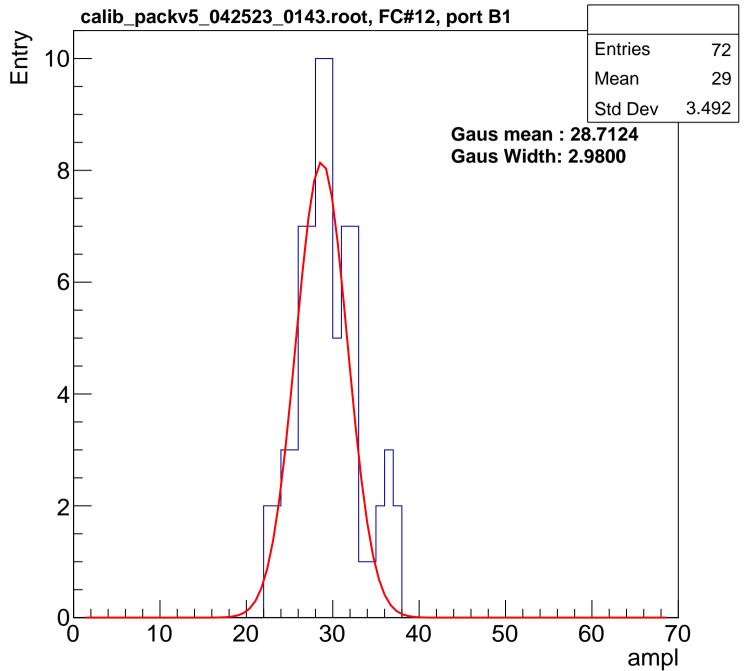


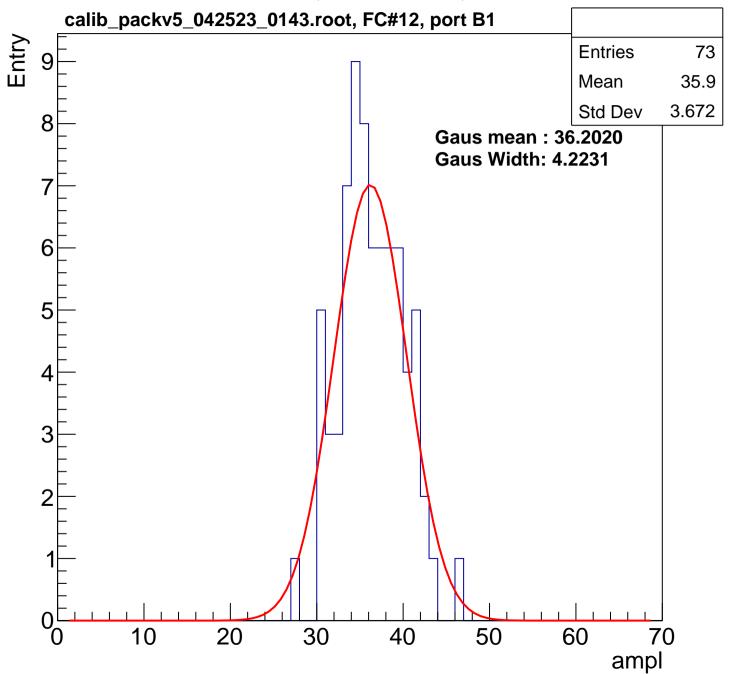


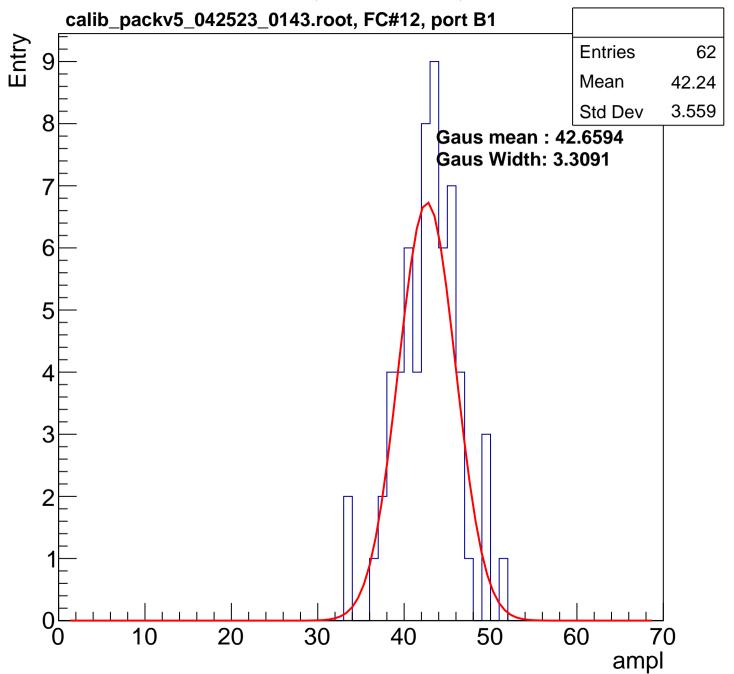


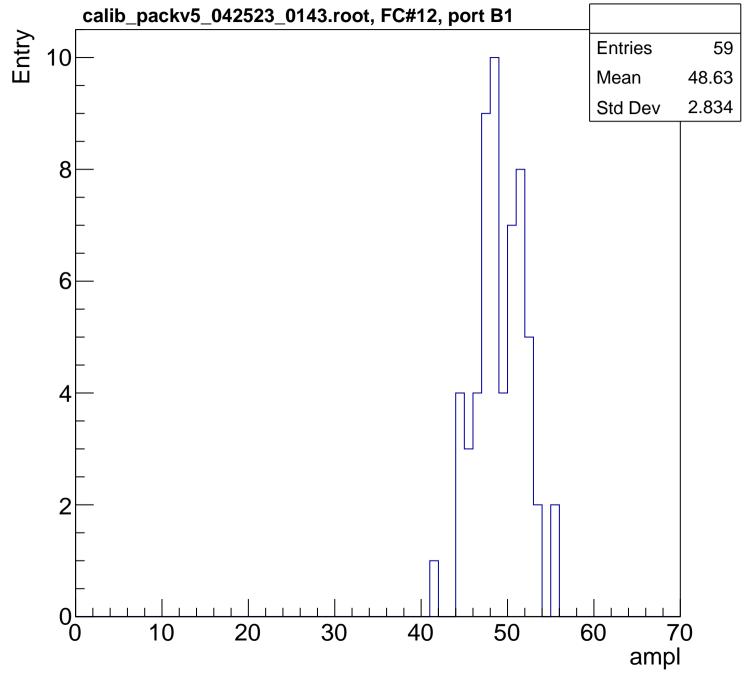


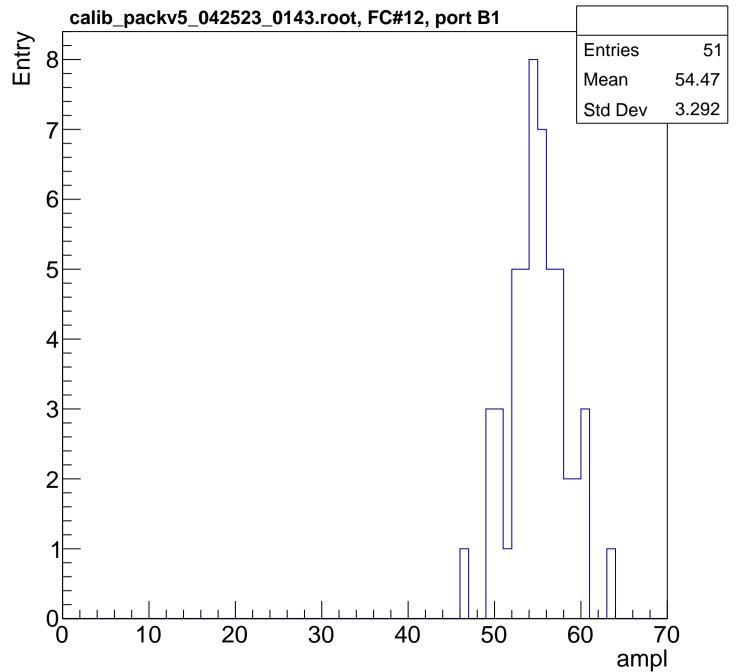


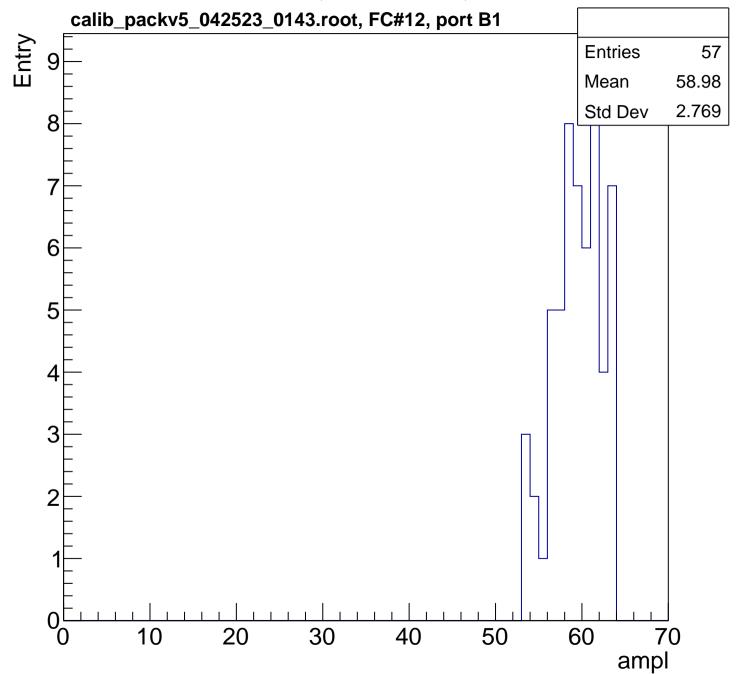


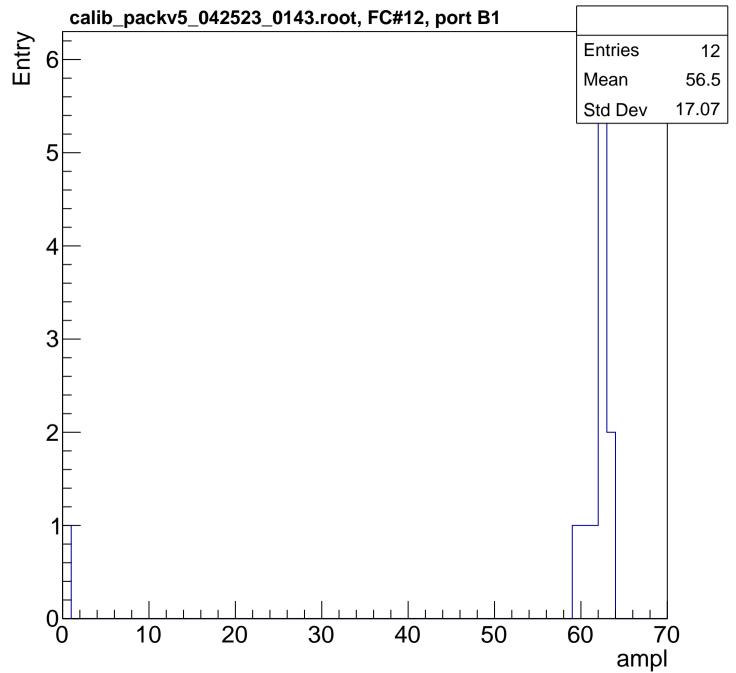




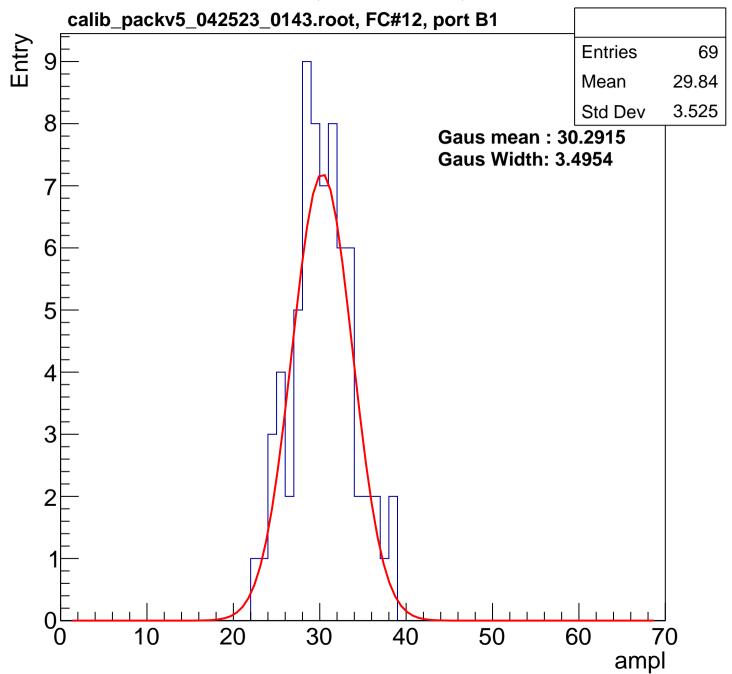


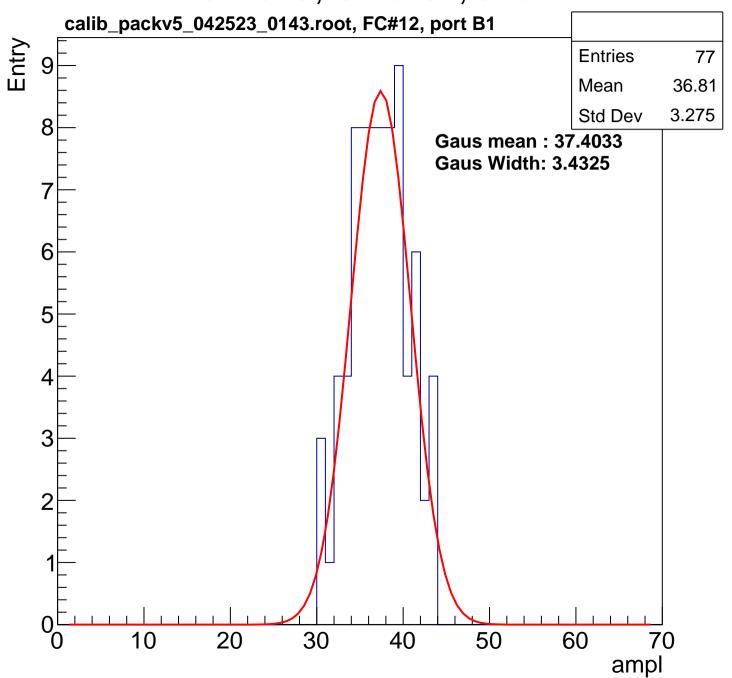


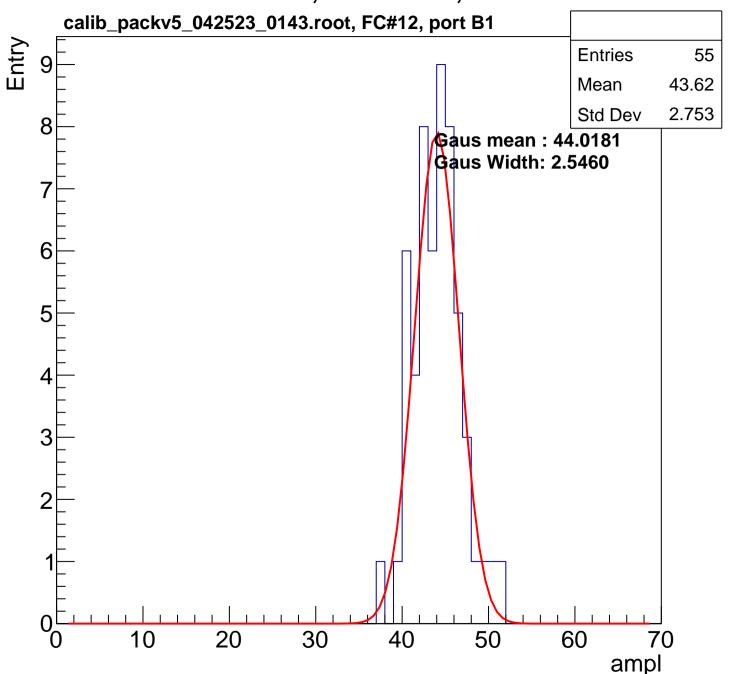


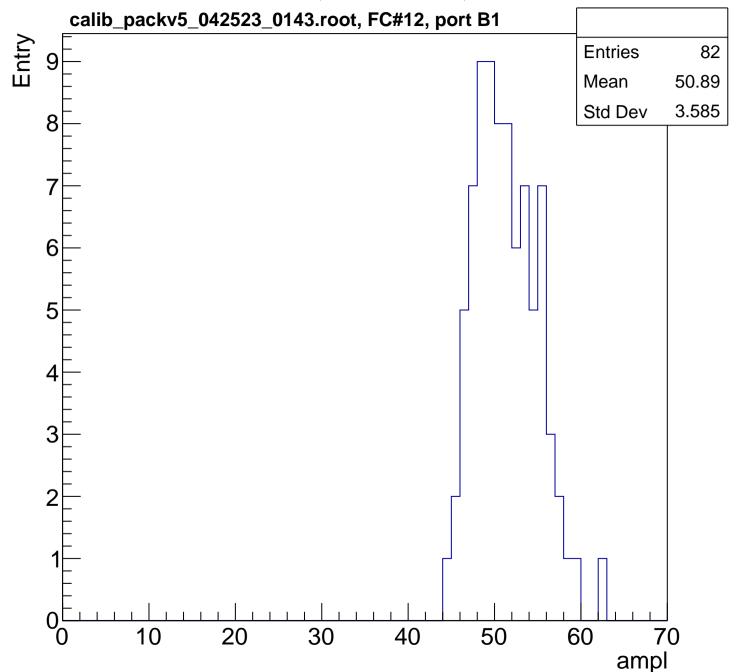


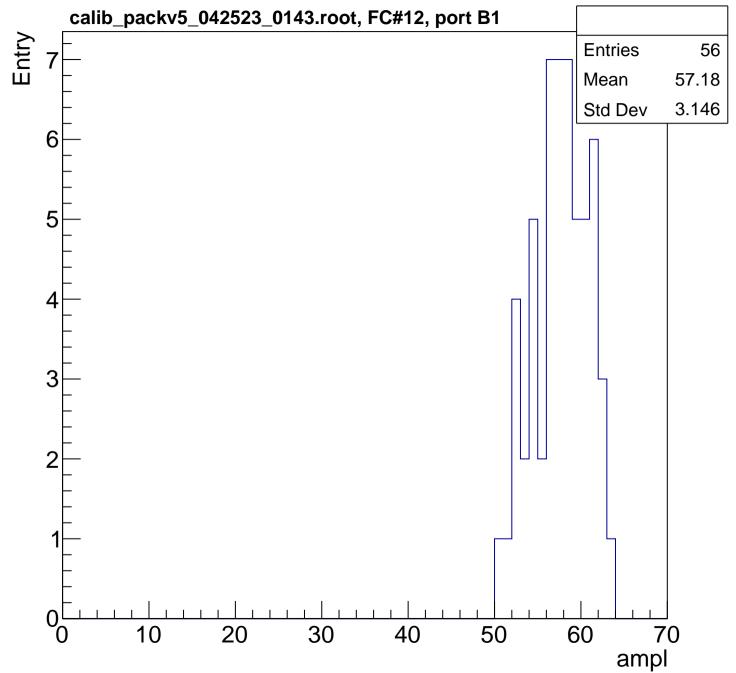
B0L102S, U7-ch30, adc7 calib_packv5_042523_0143.root, FC#12, port B1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

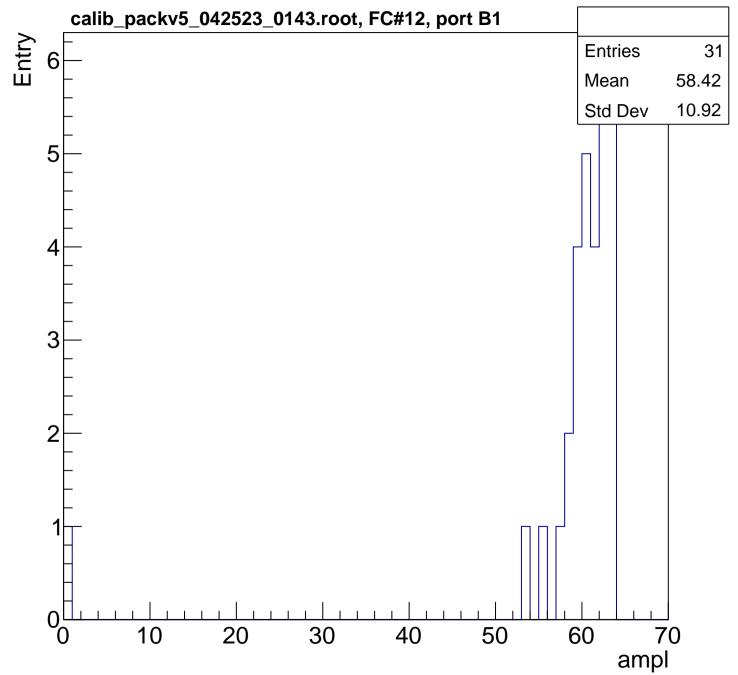


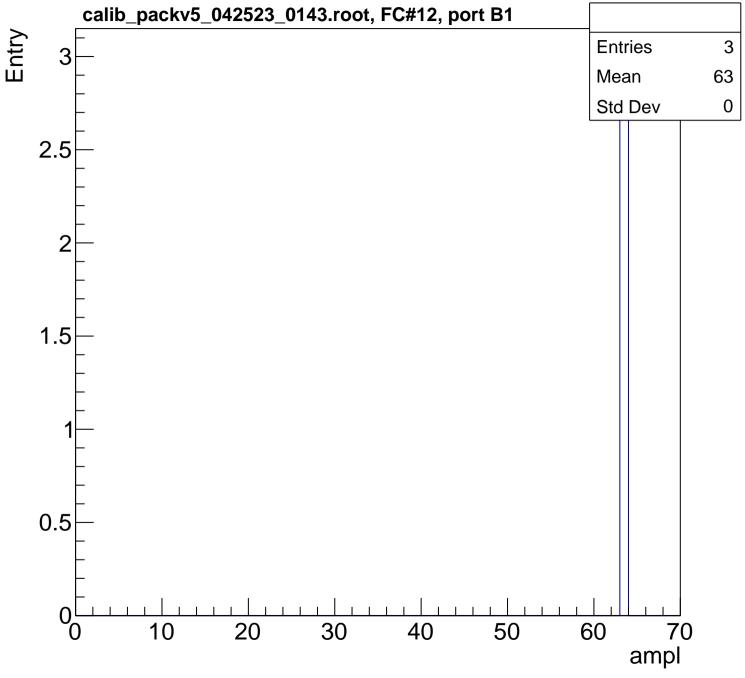


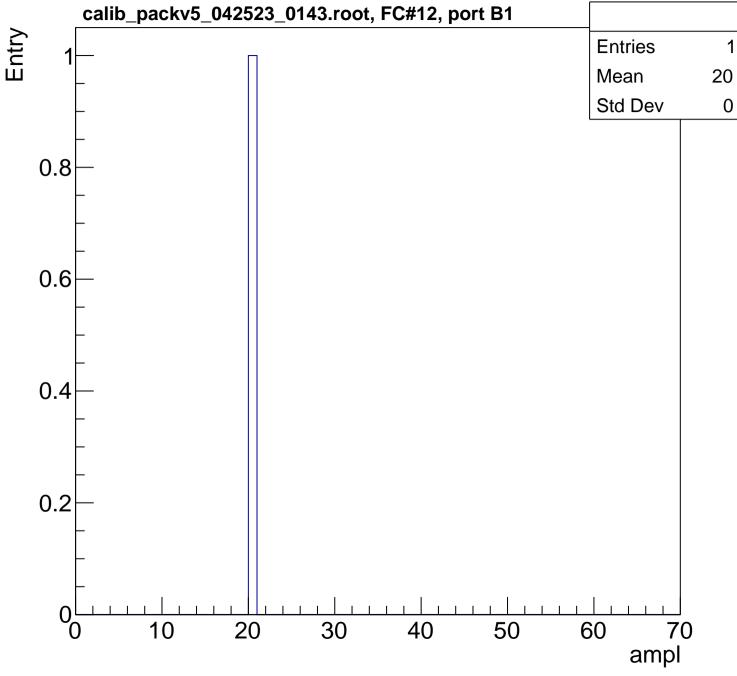


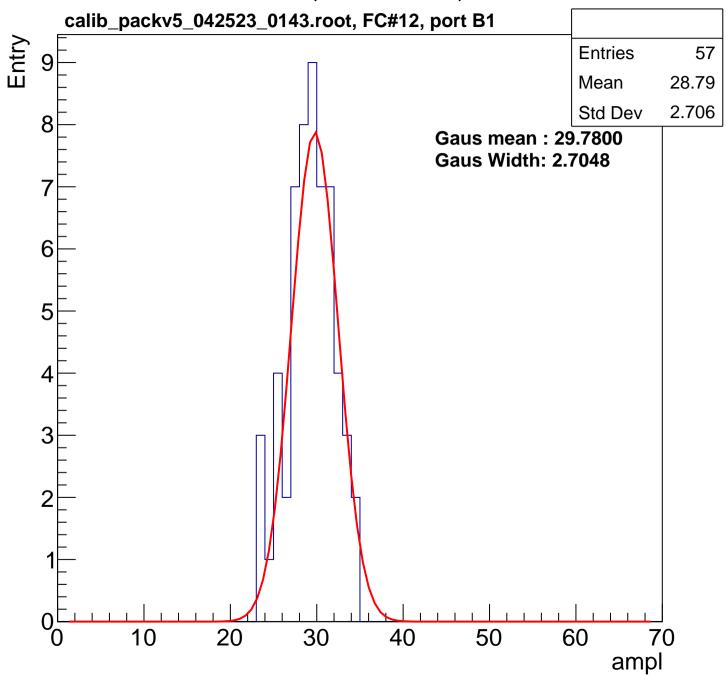


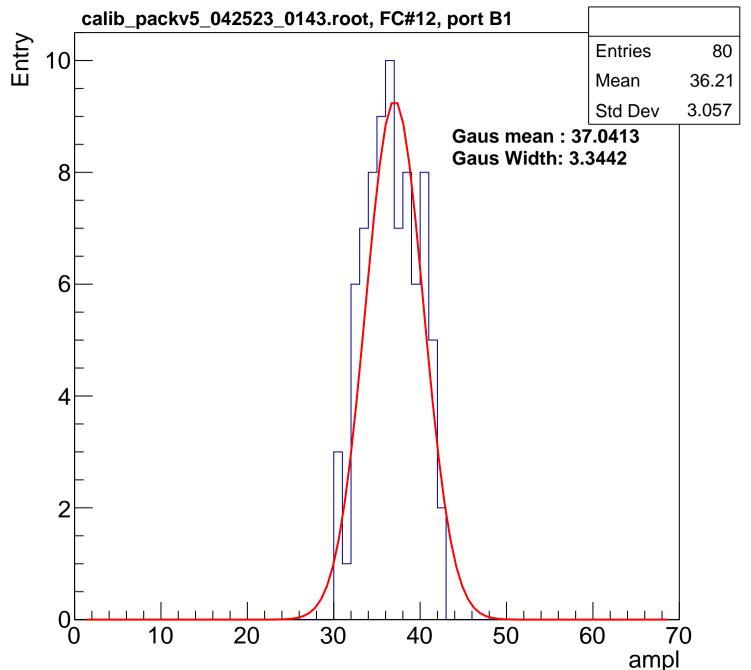


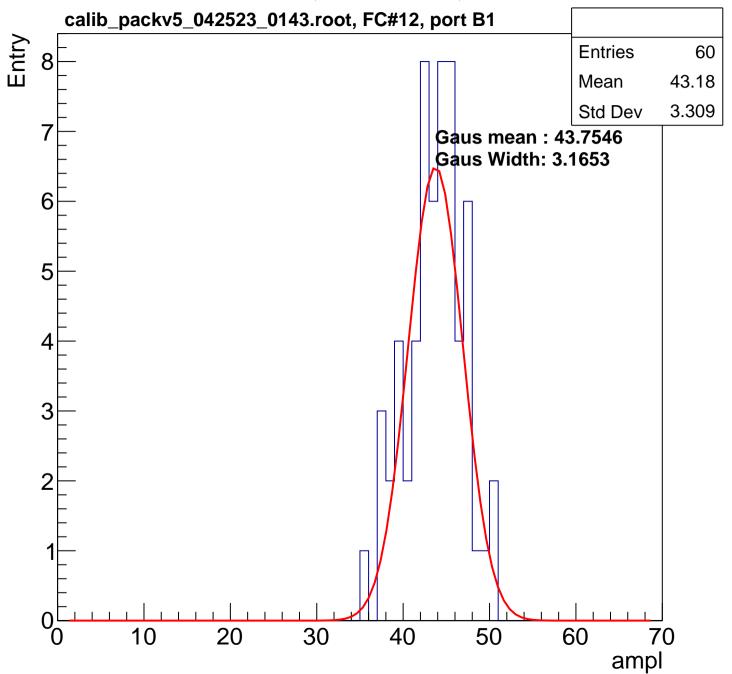


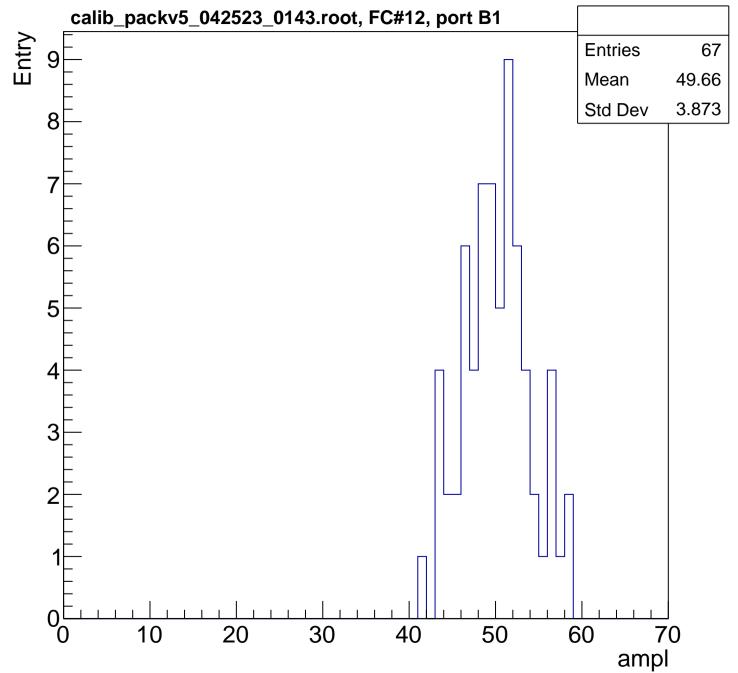


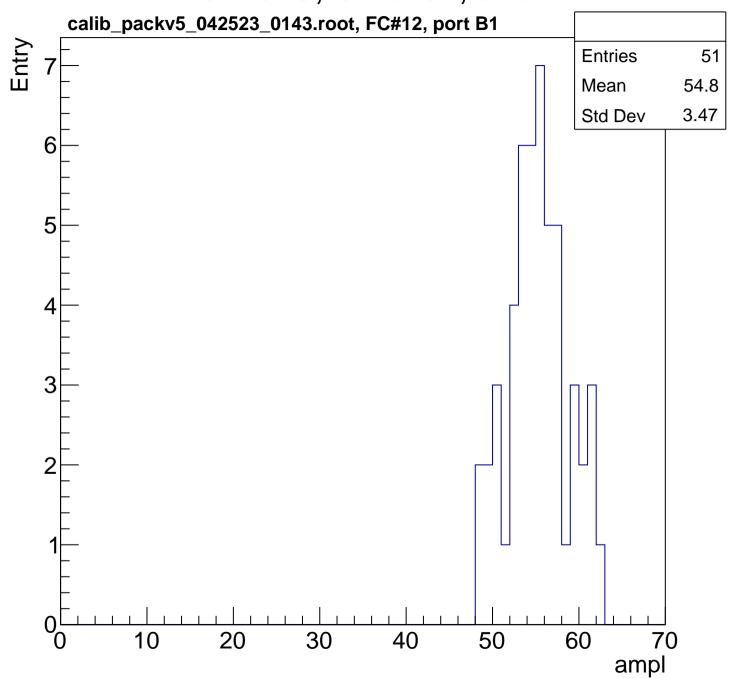


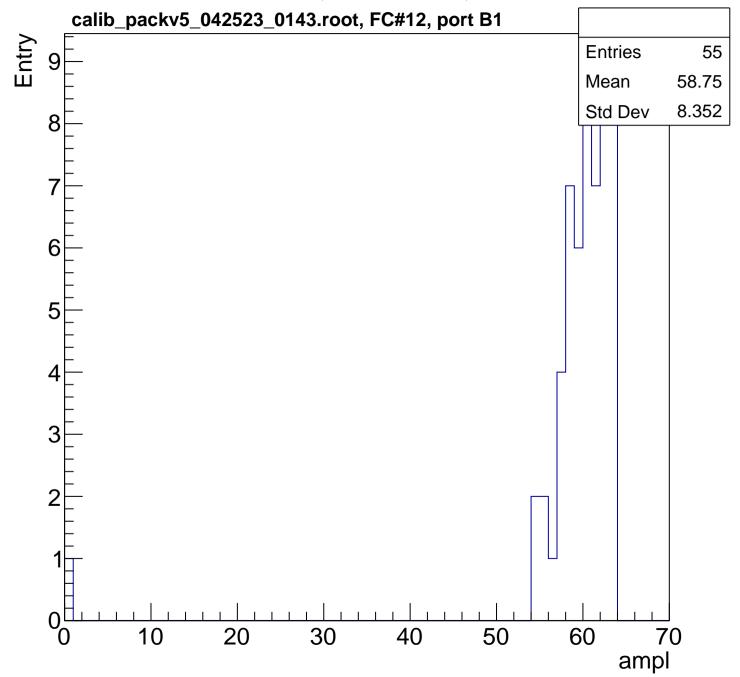


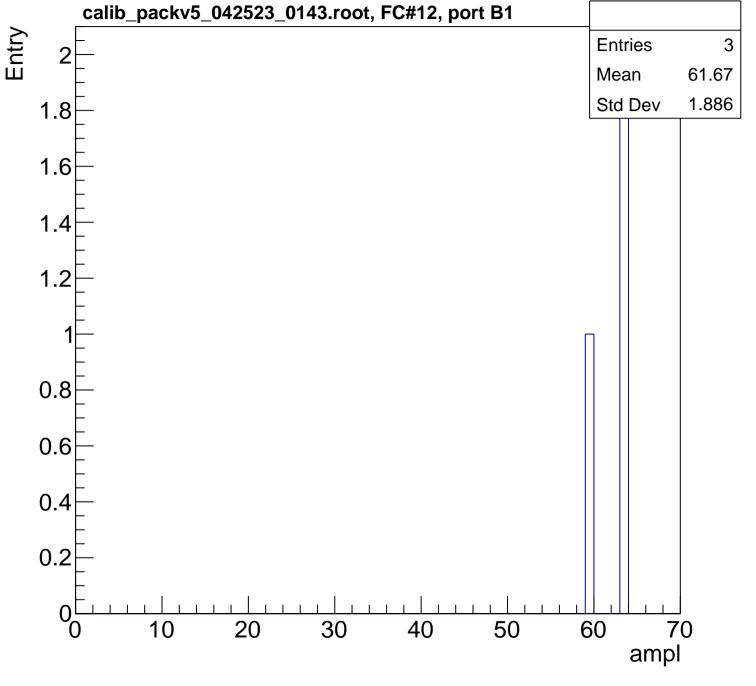




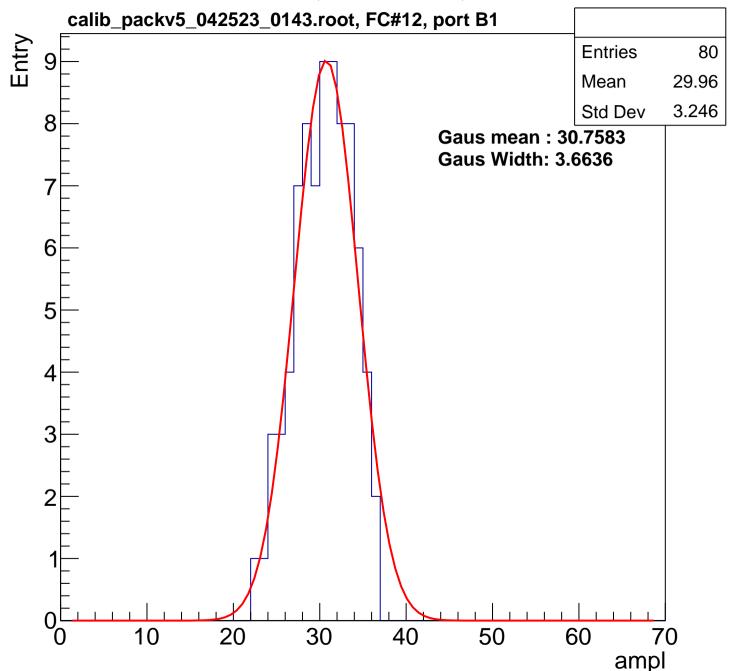


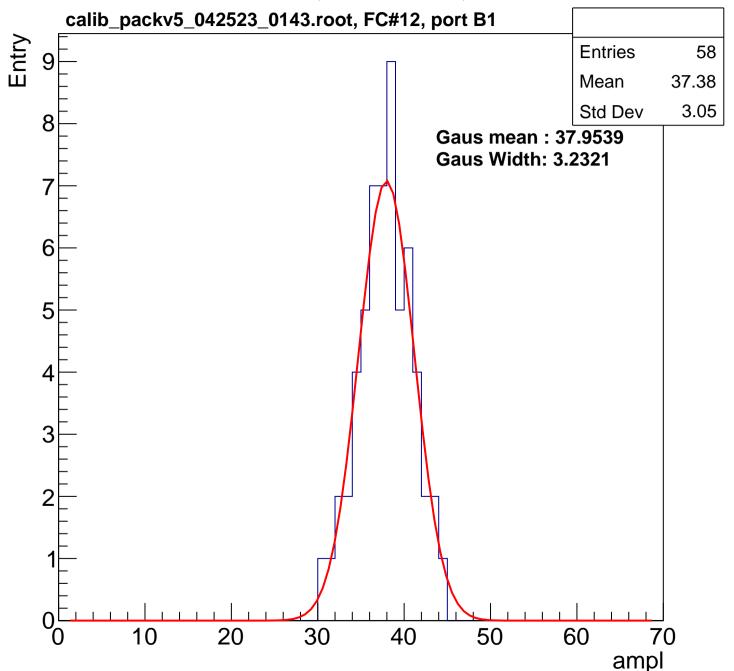


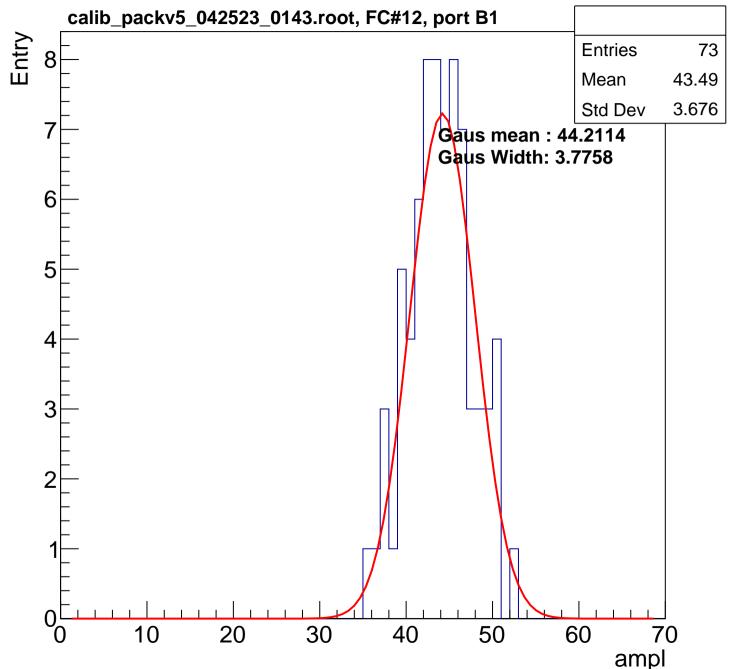


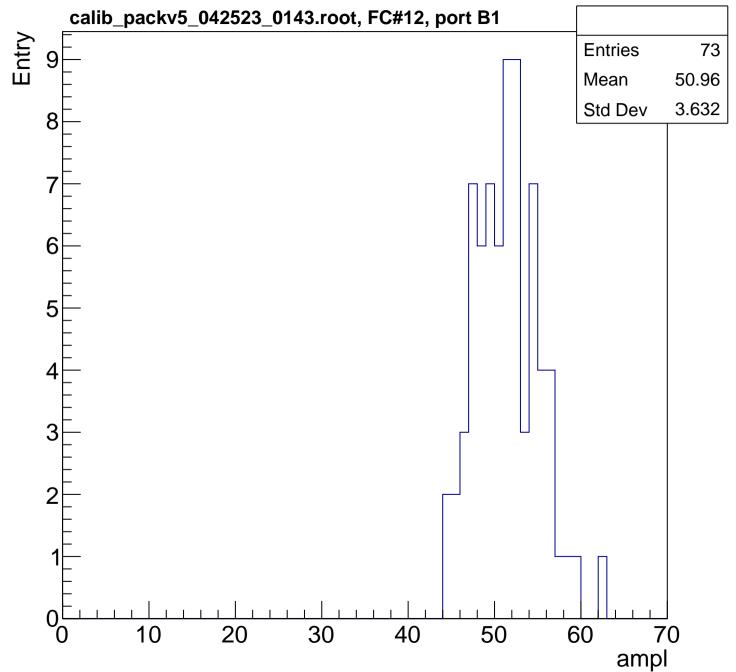


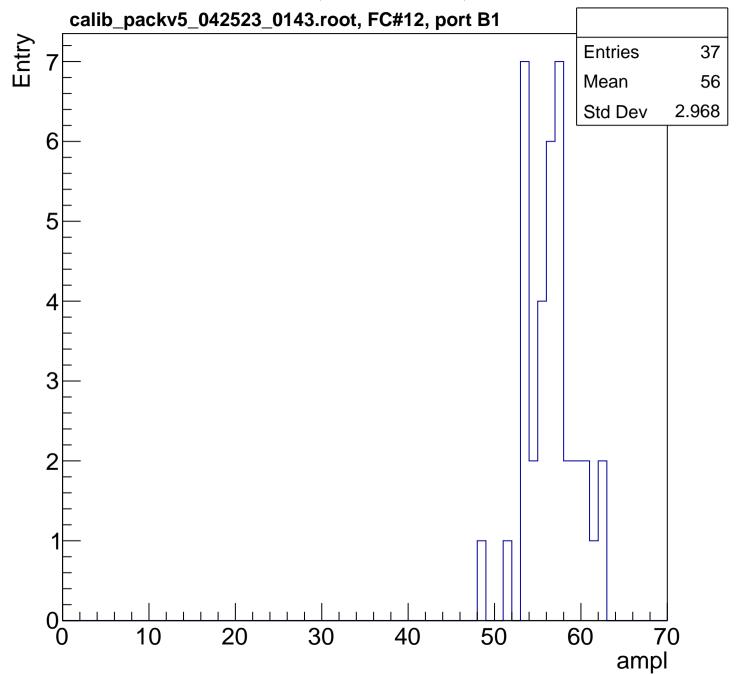


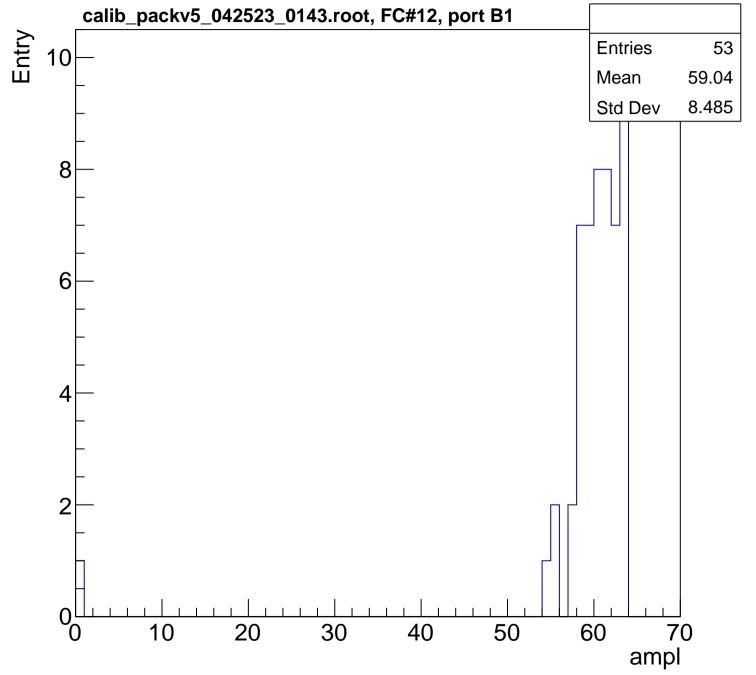


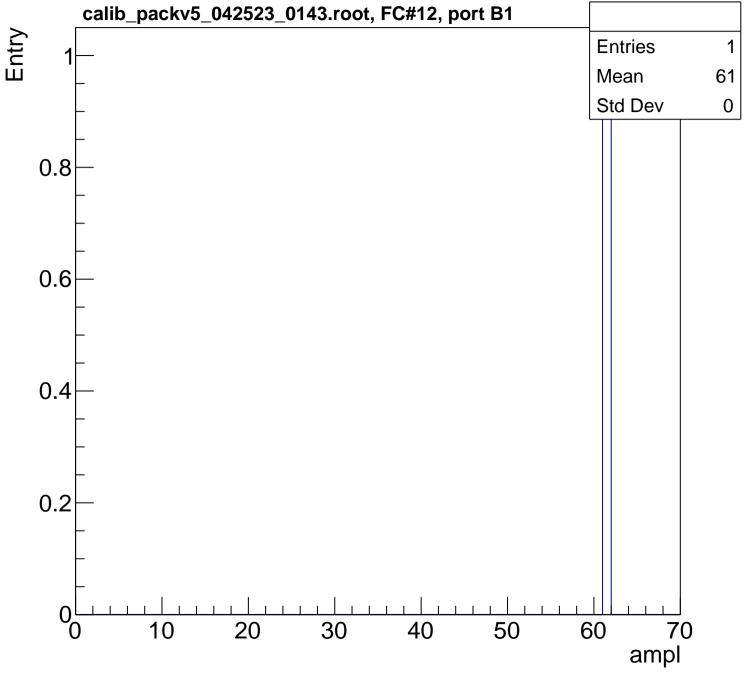


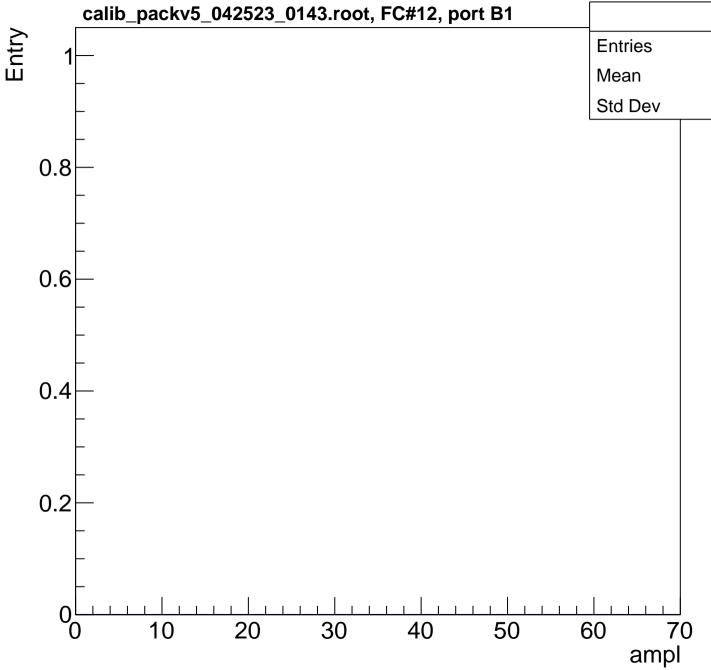


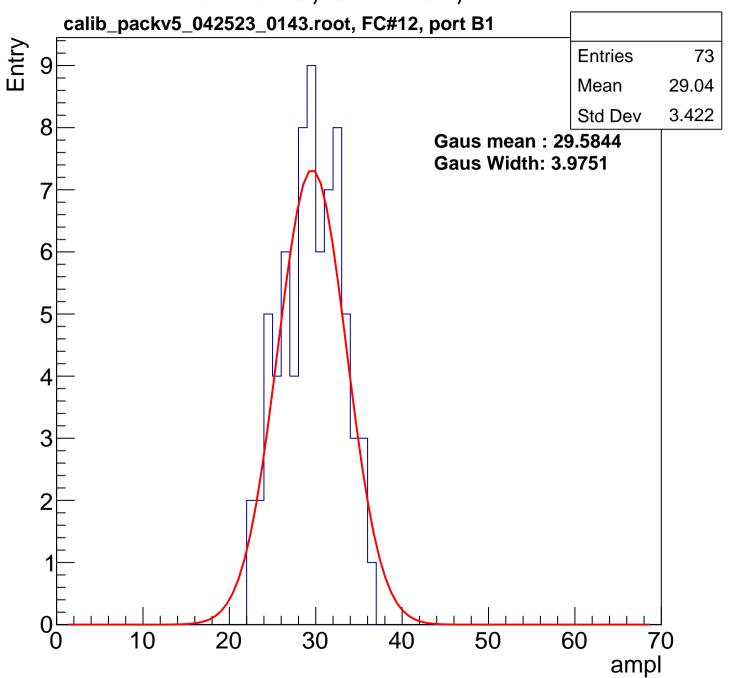


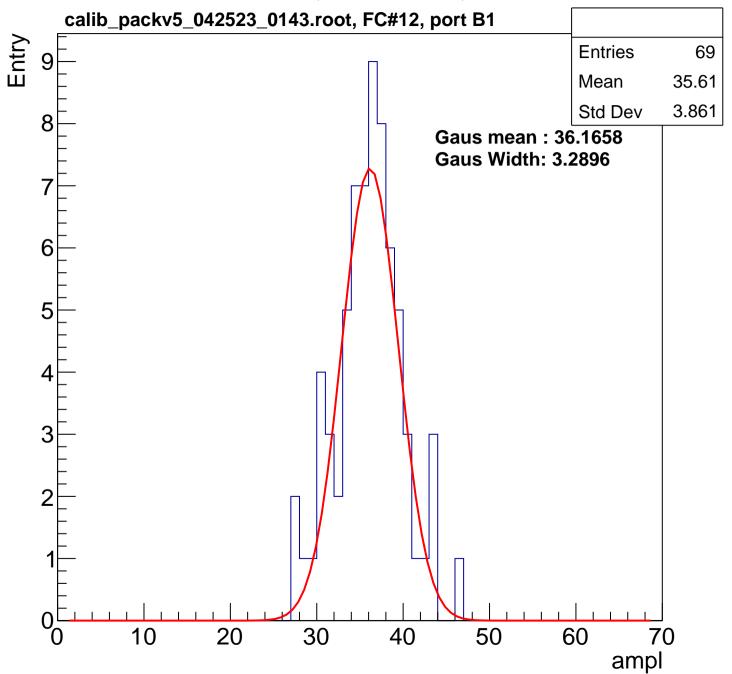


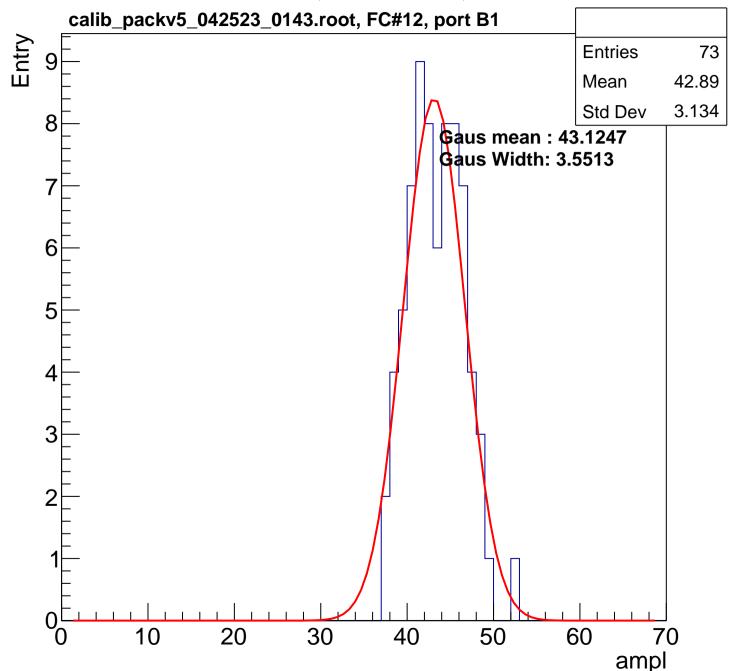


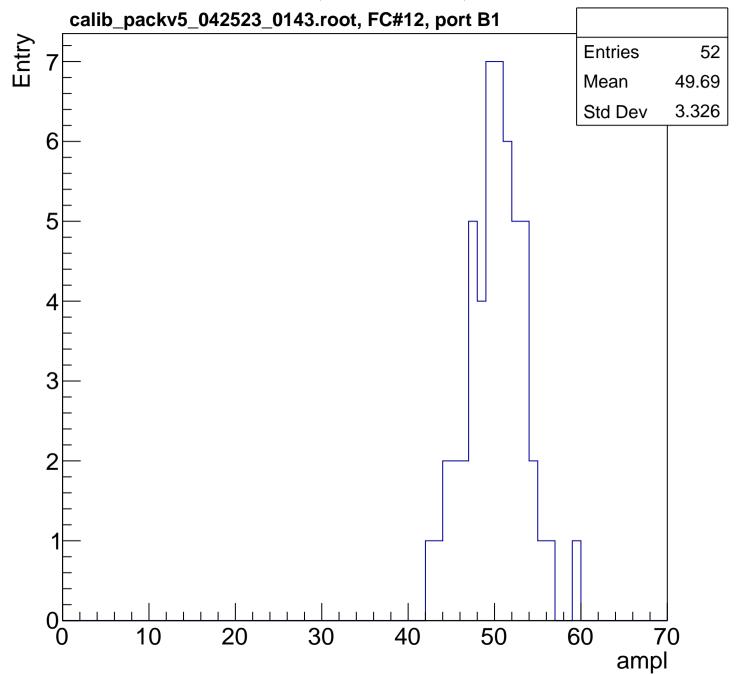


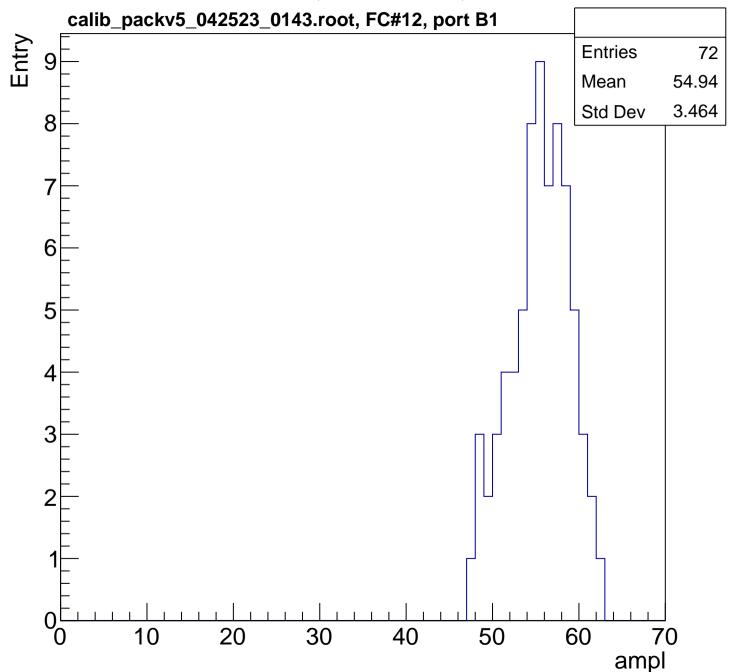


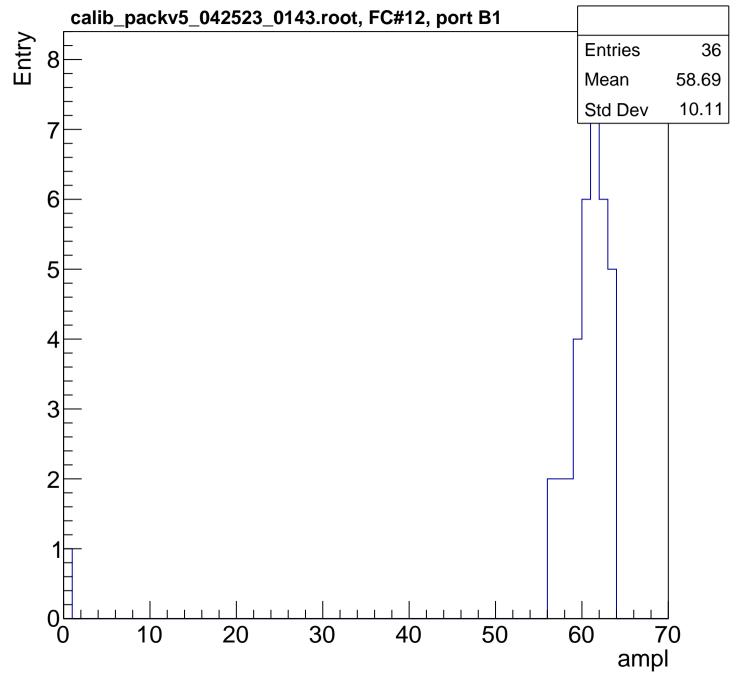


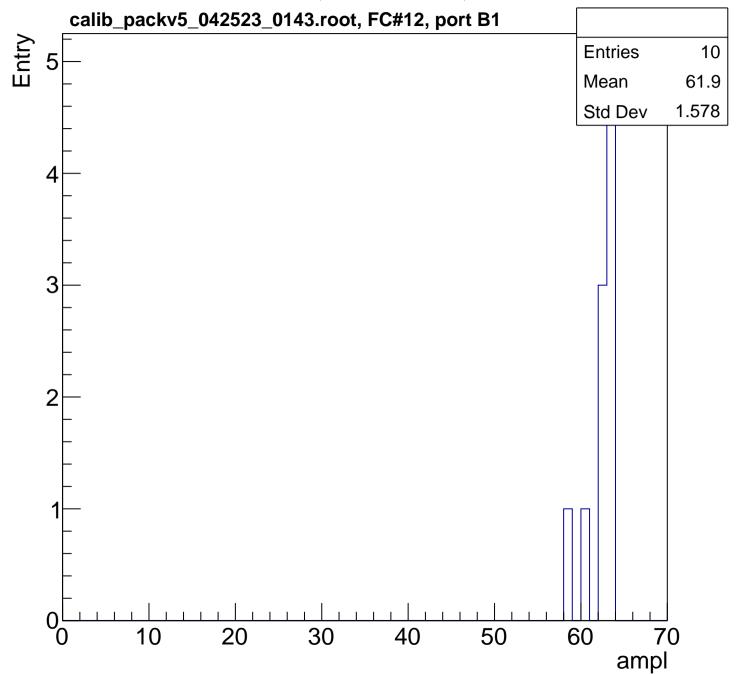


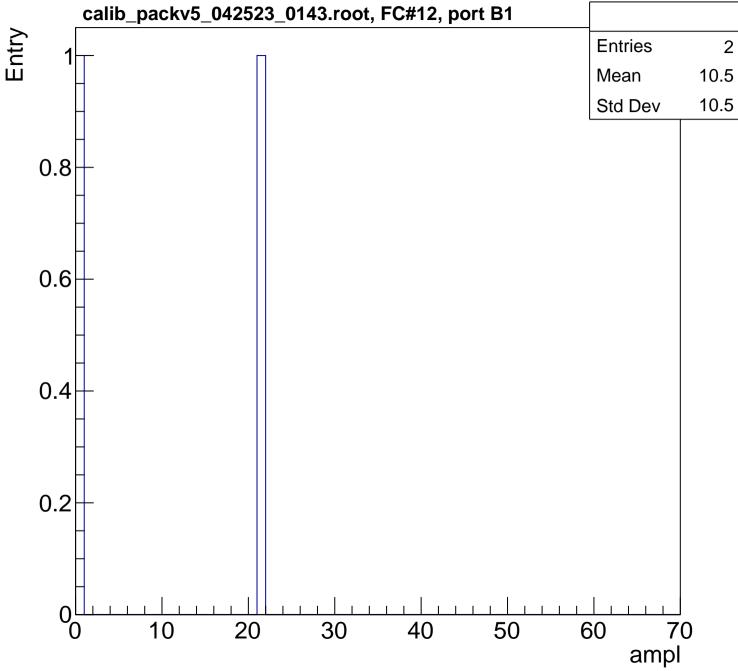


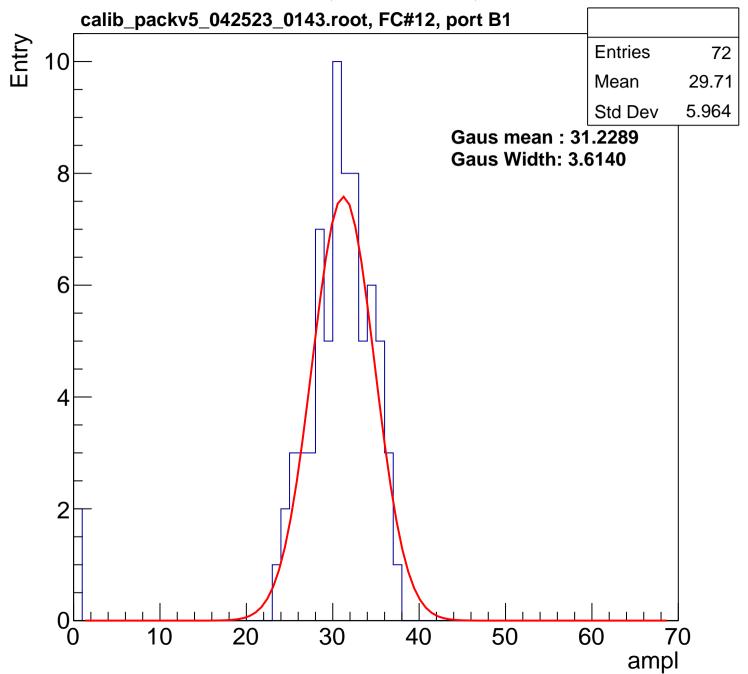


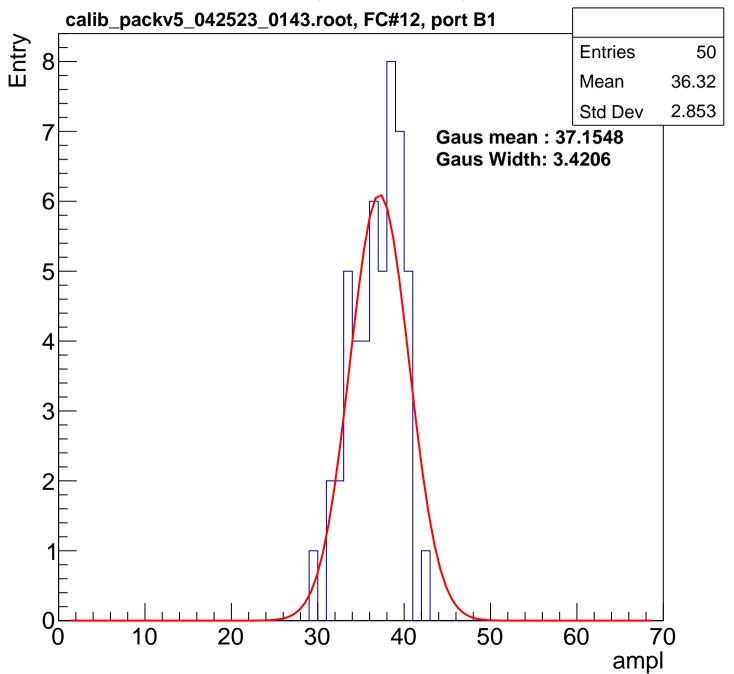


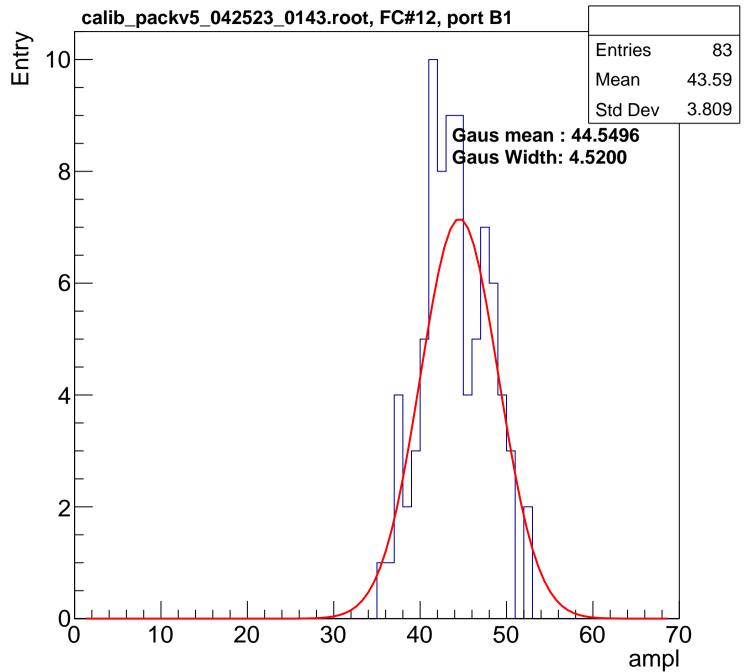


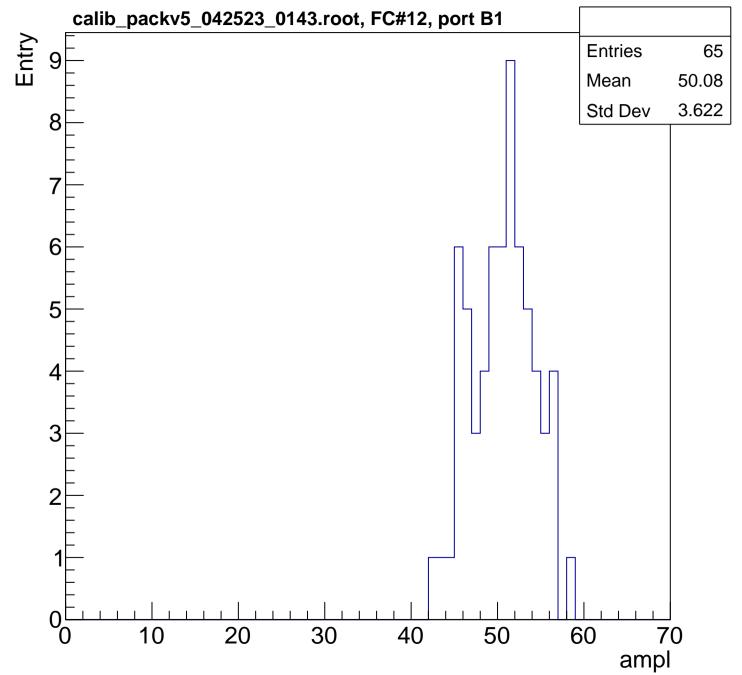


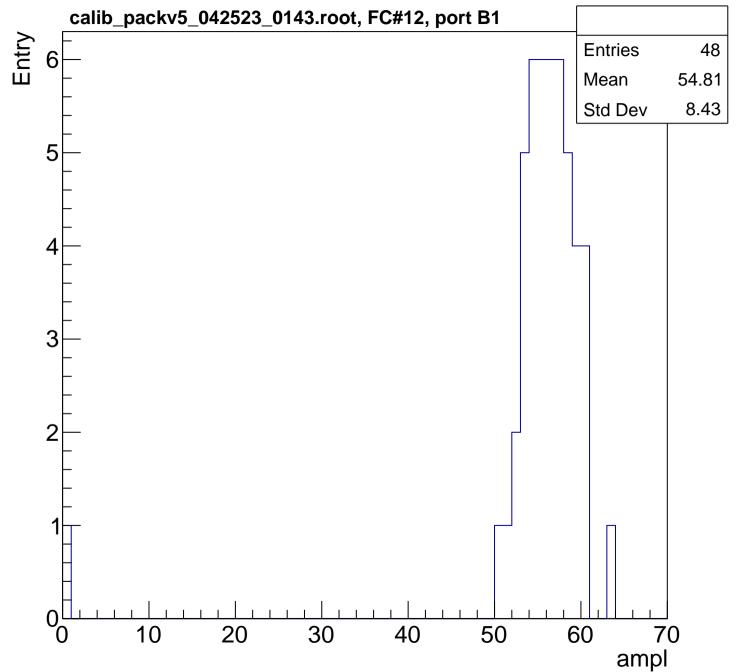


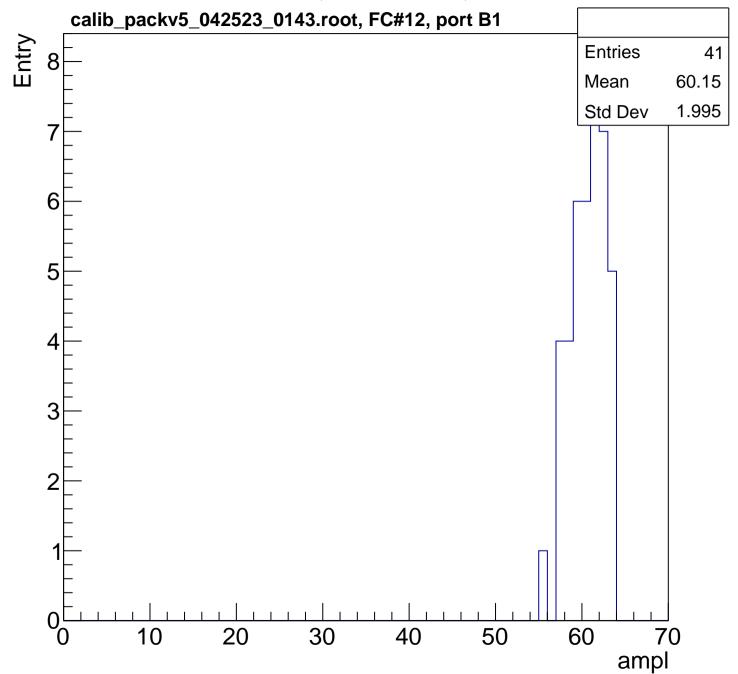


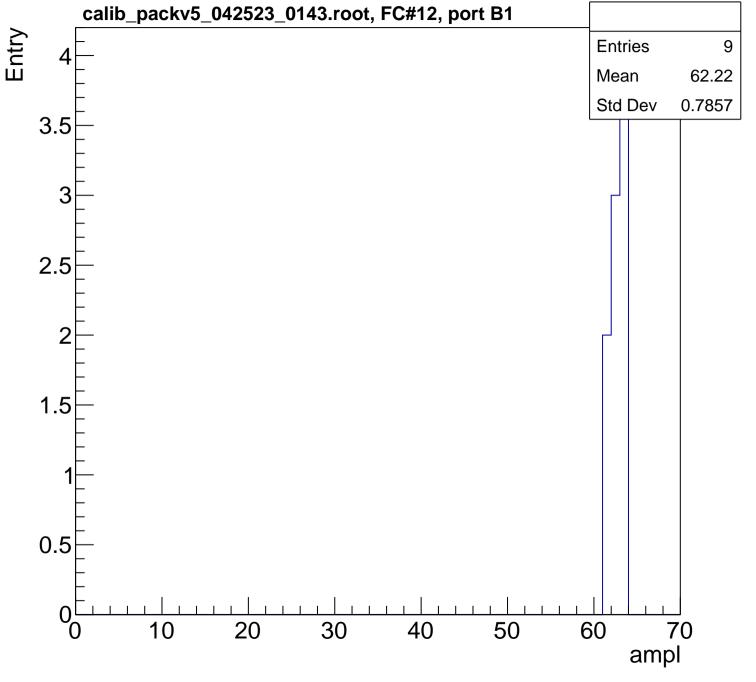






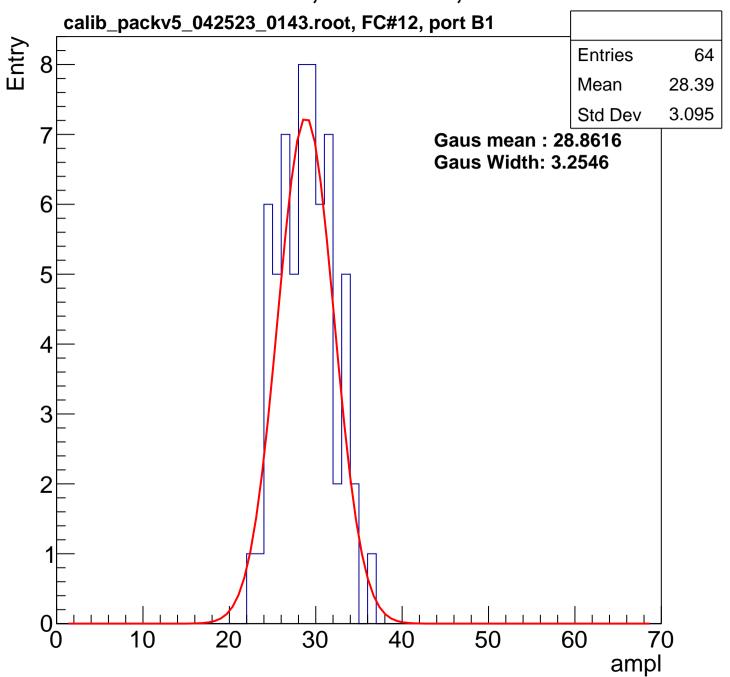


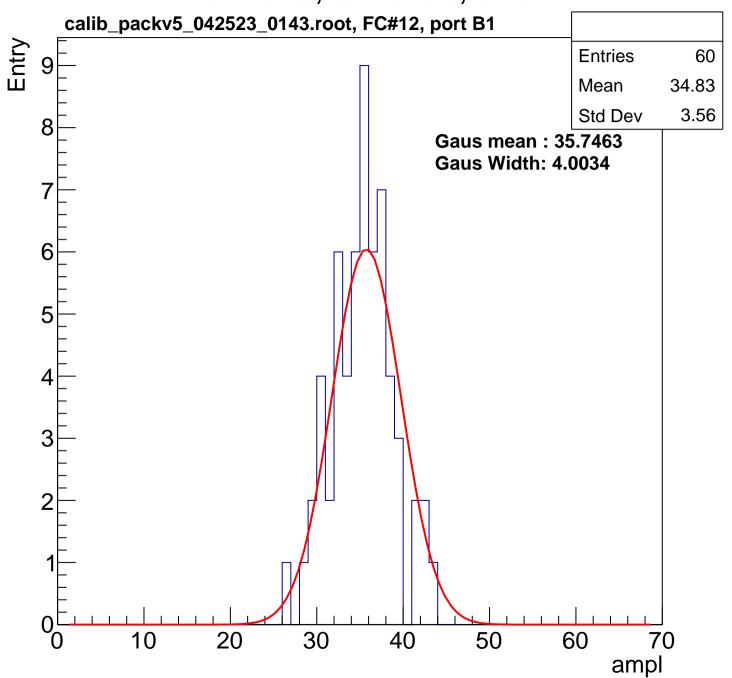


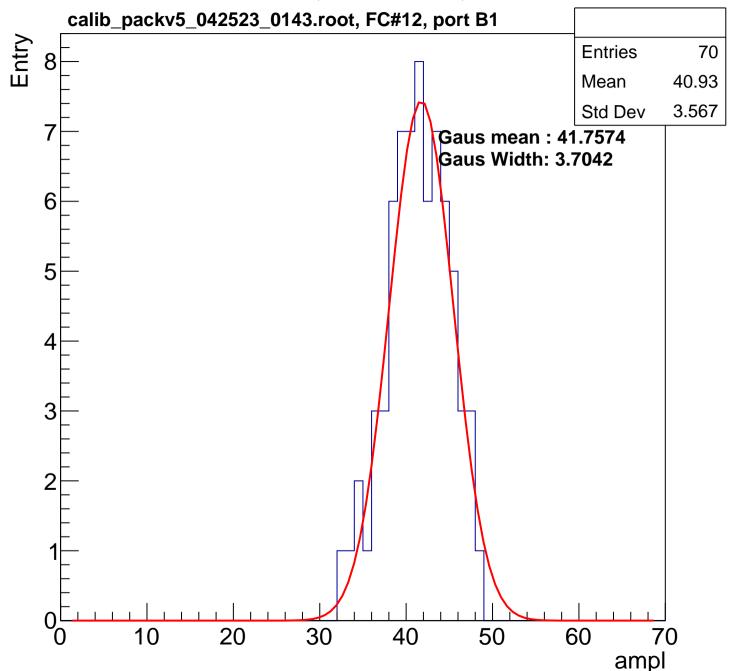


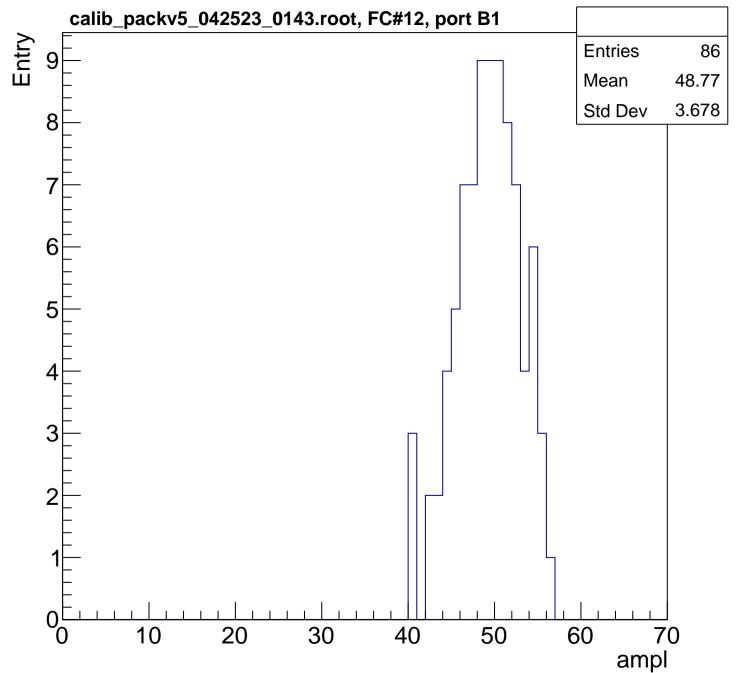
B0L102S, U7-ch35, adc7 calib_packv5_042523_0143.root, FC#12, port B1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70

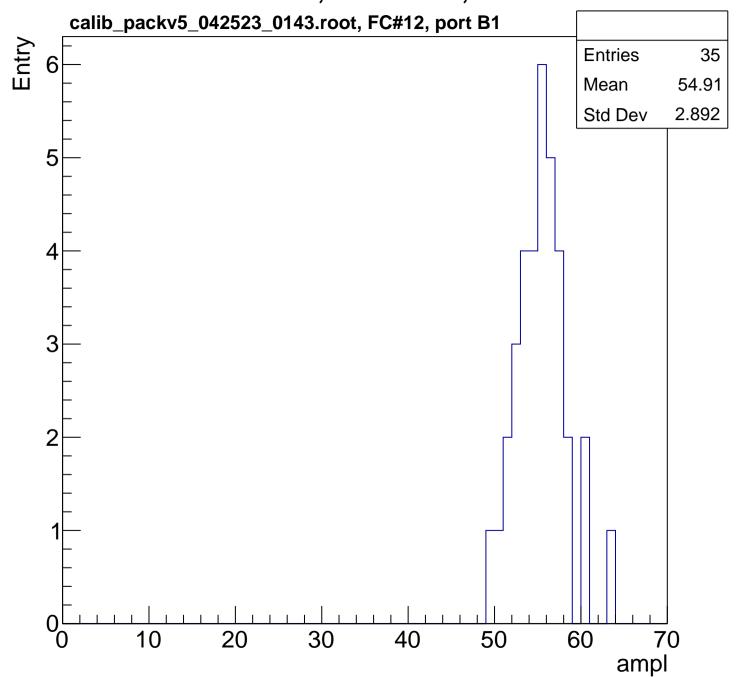
ampl

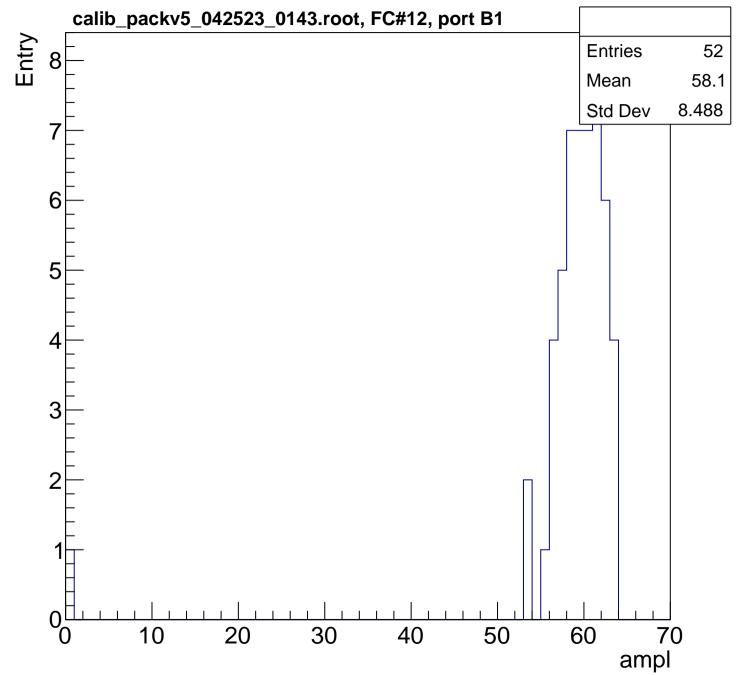


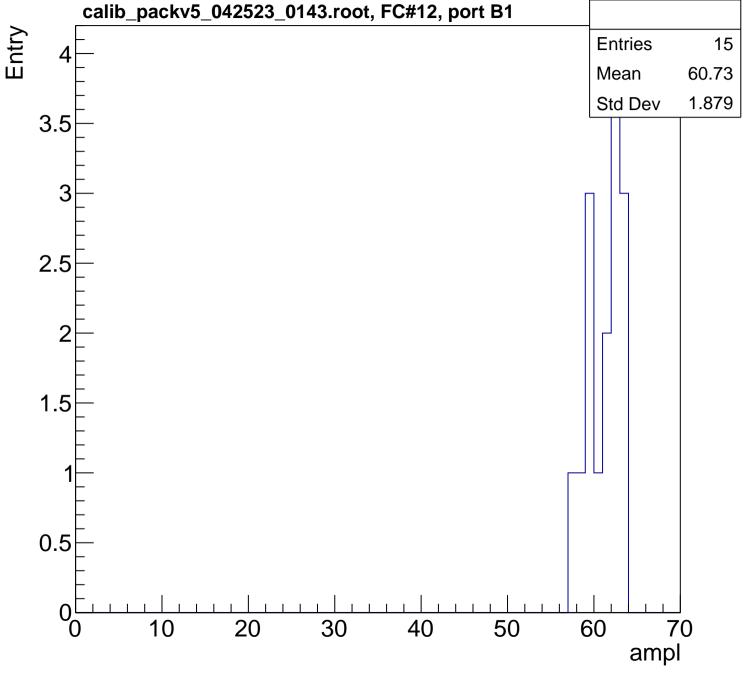


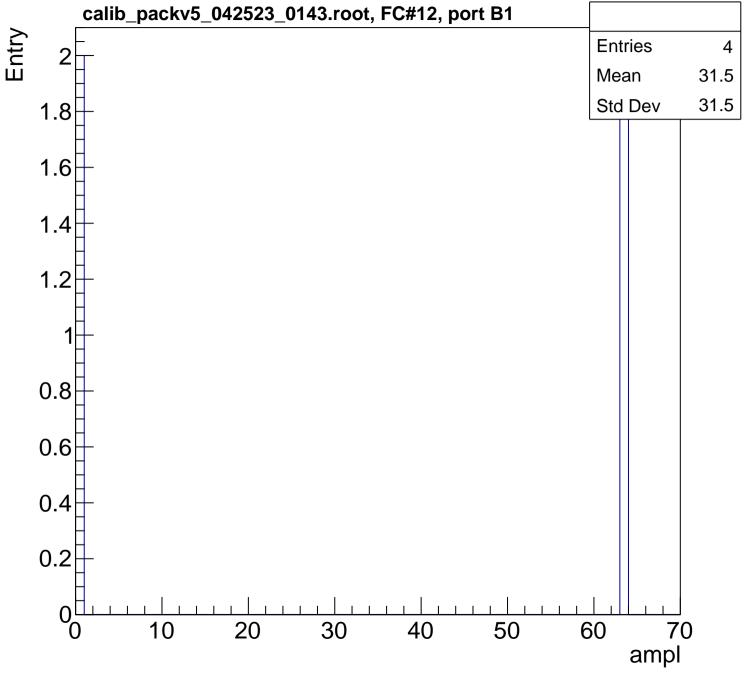


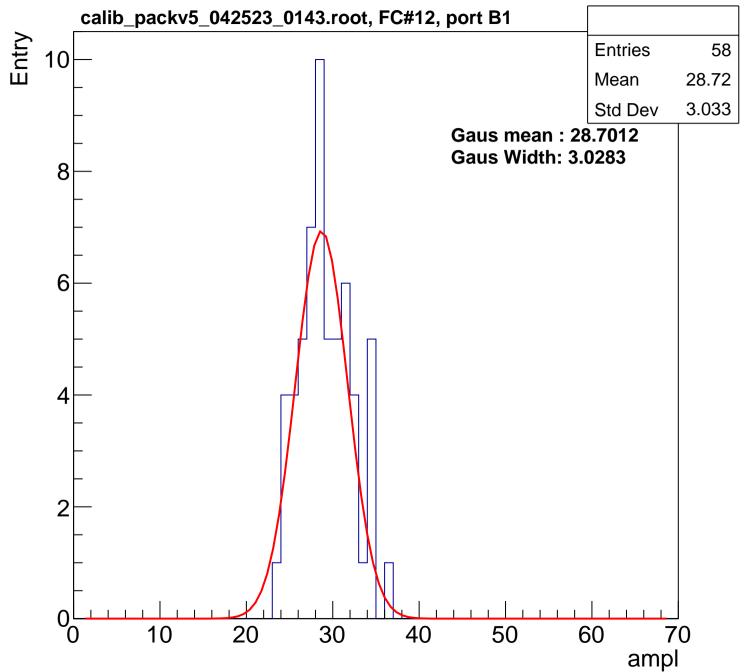


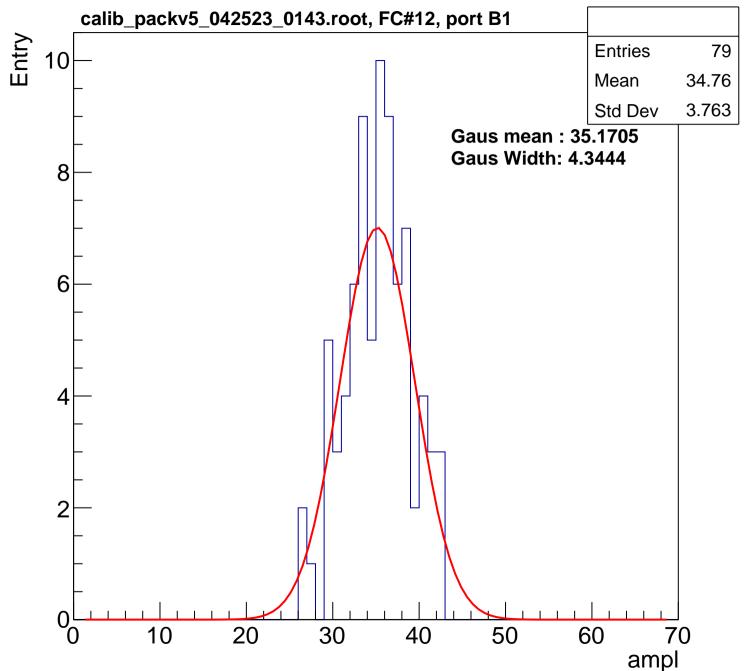


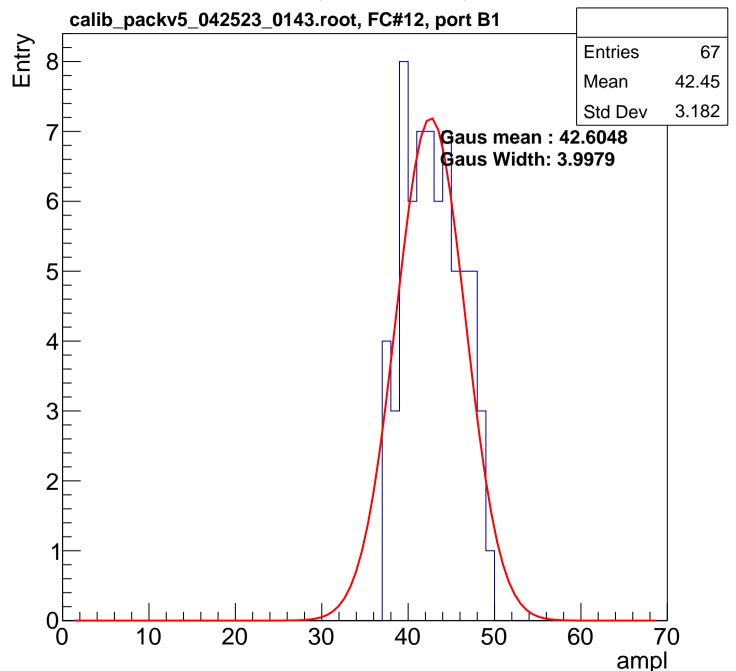


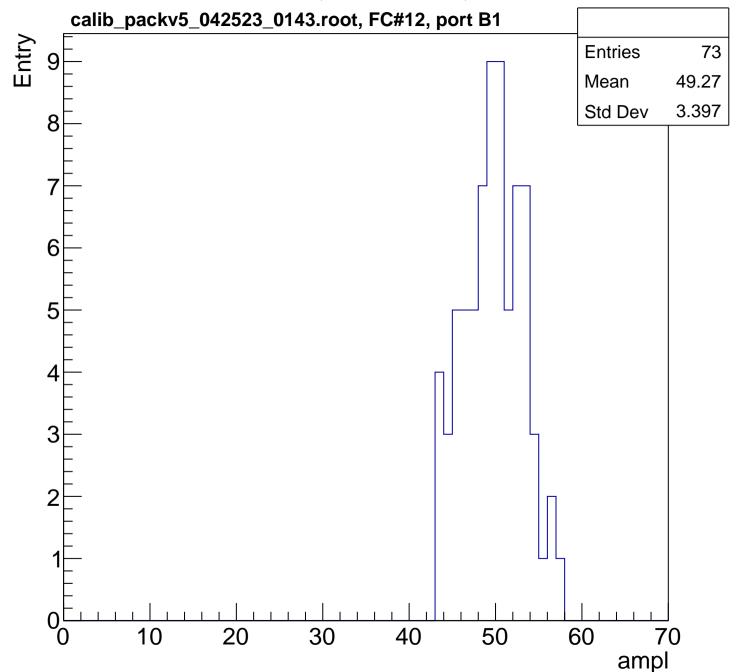


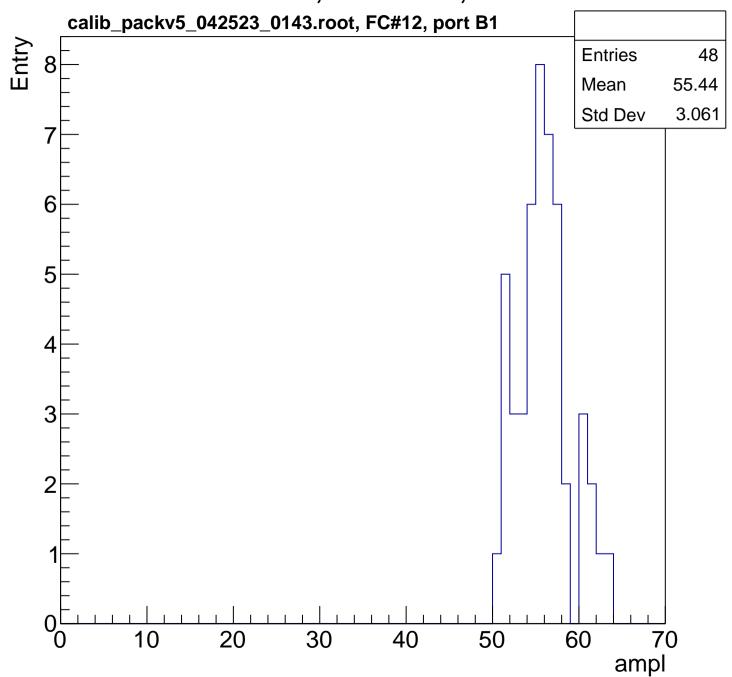


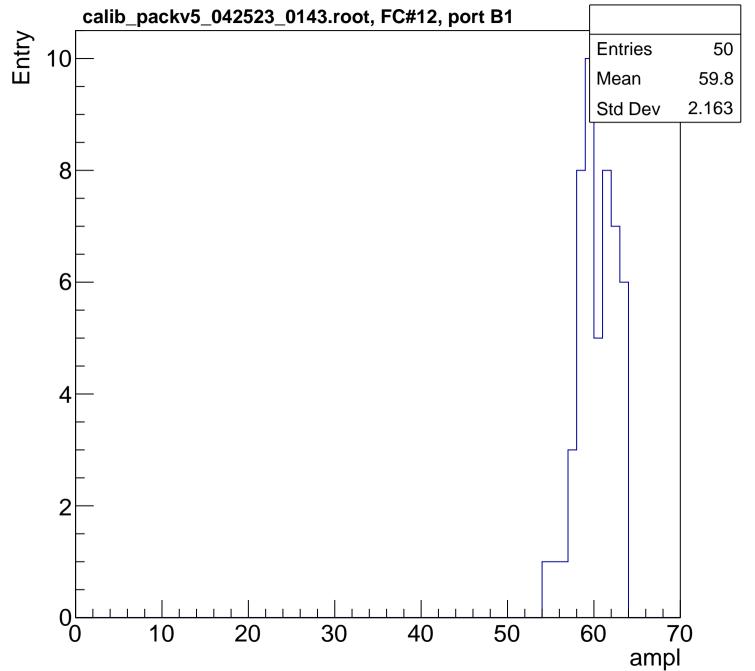


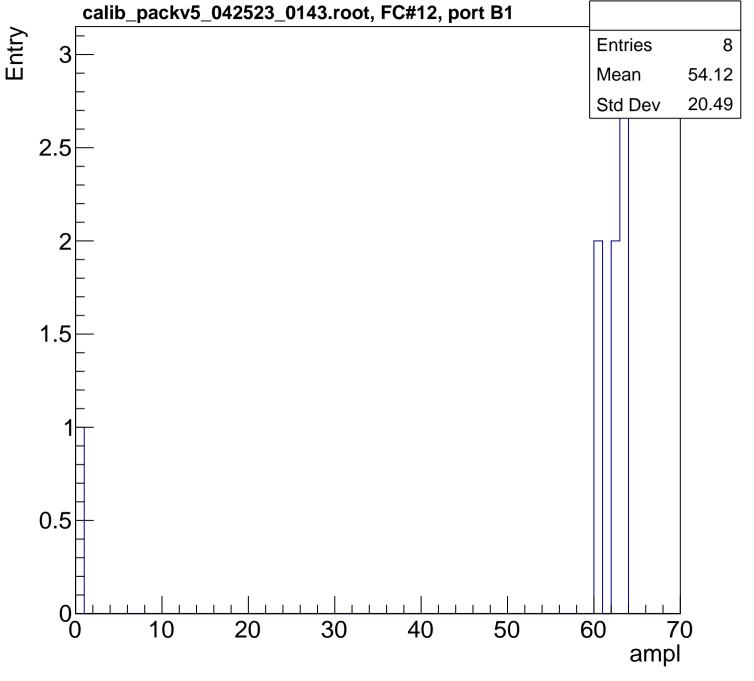


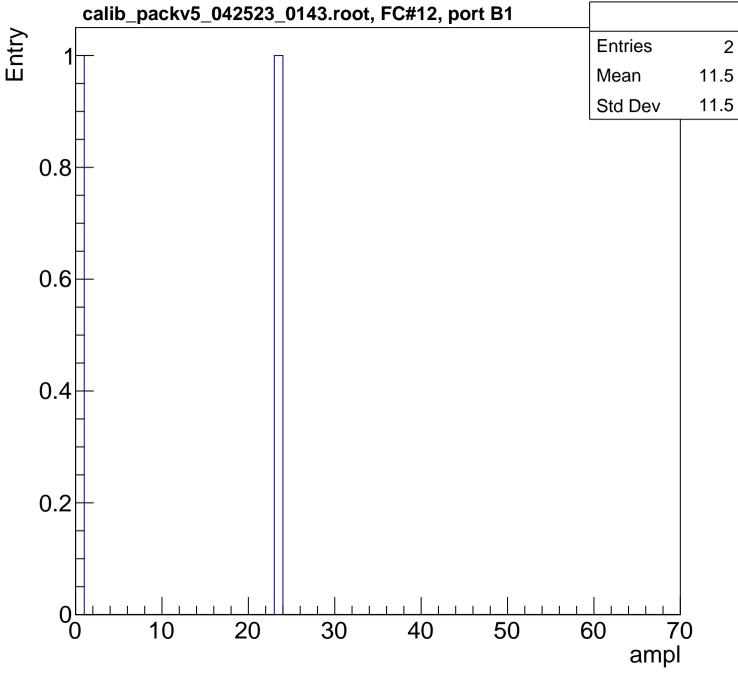


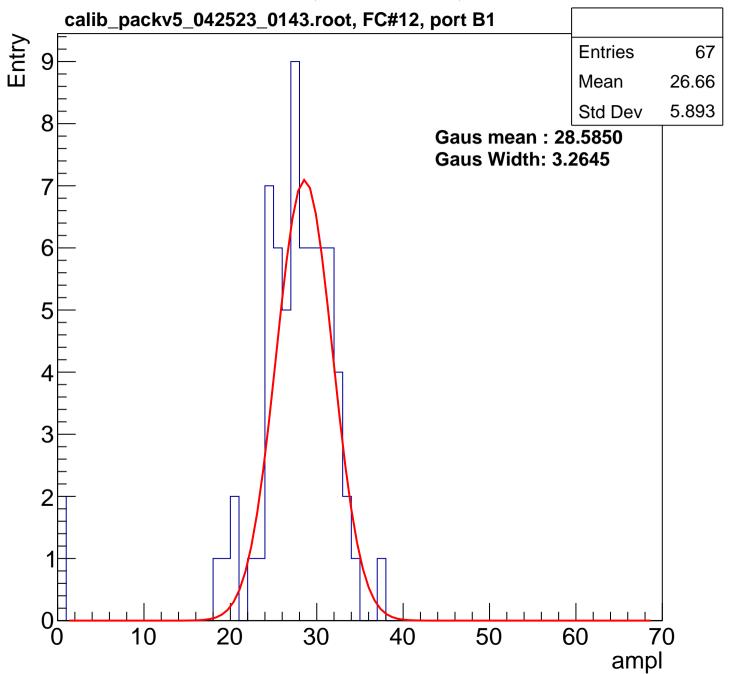


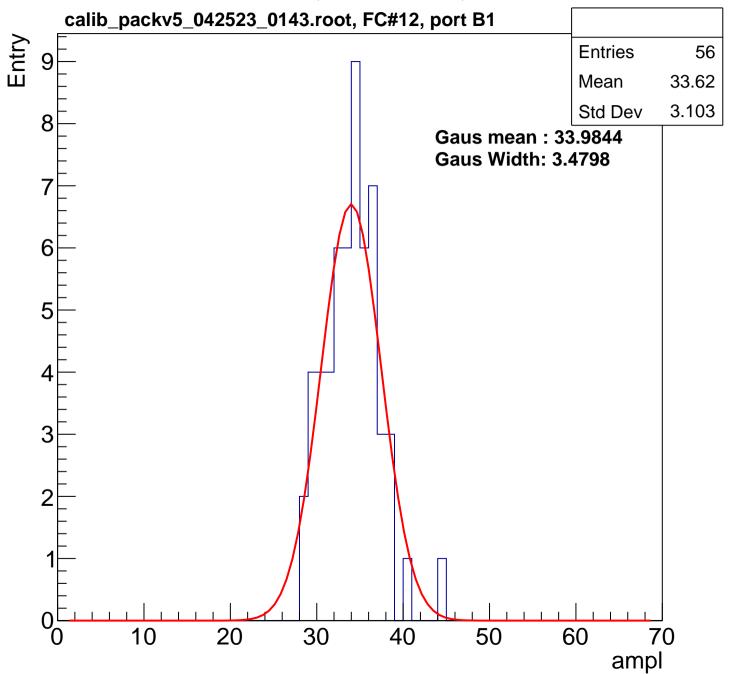


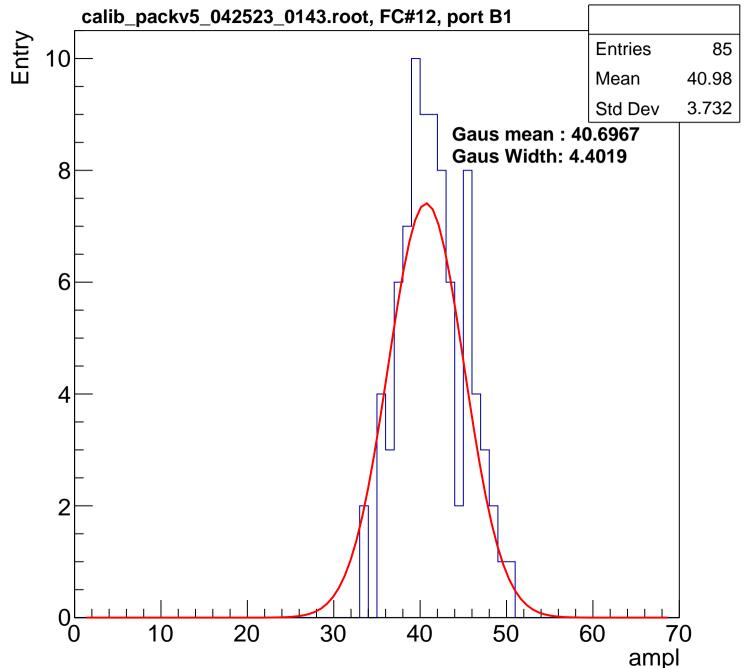


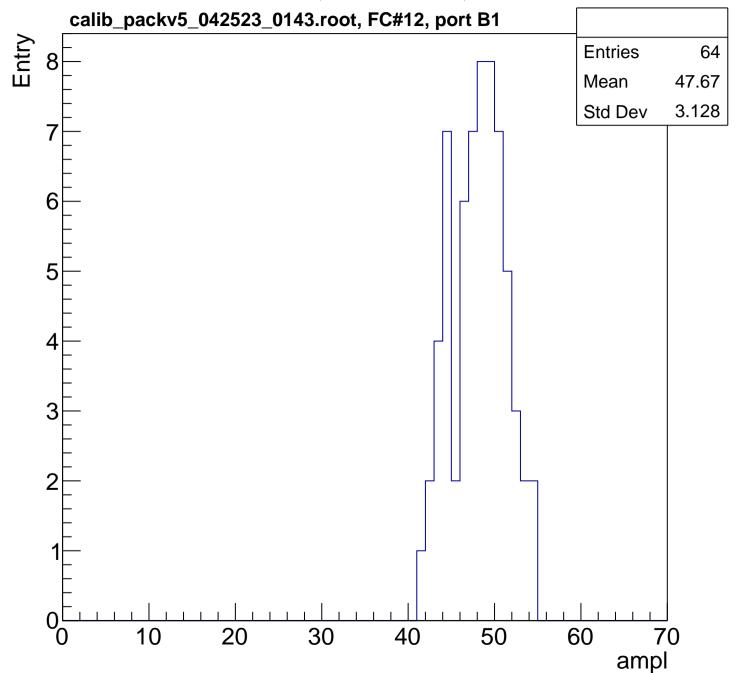


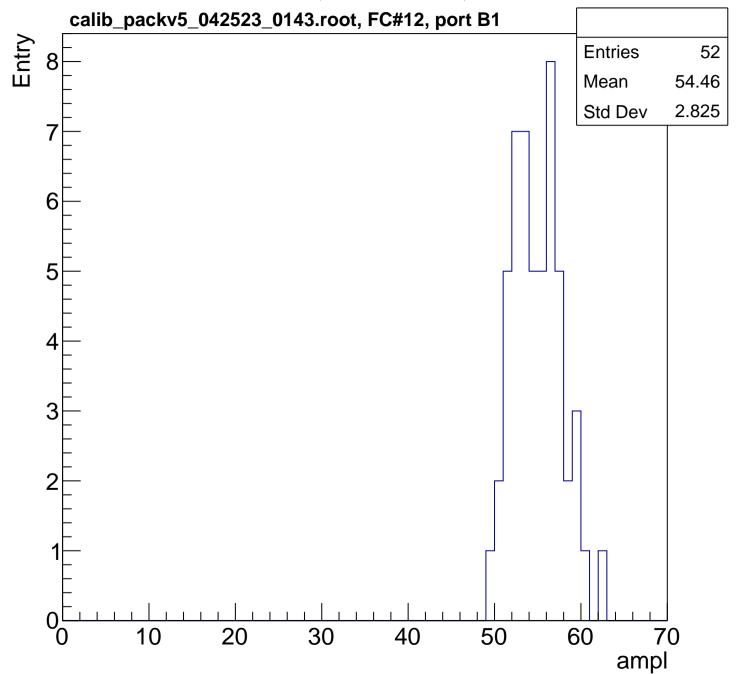


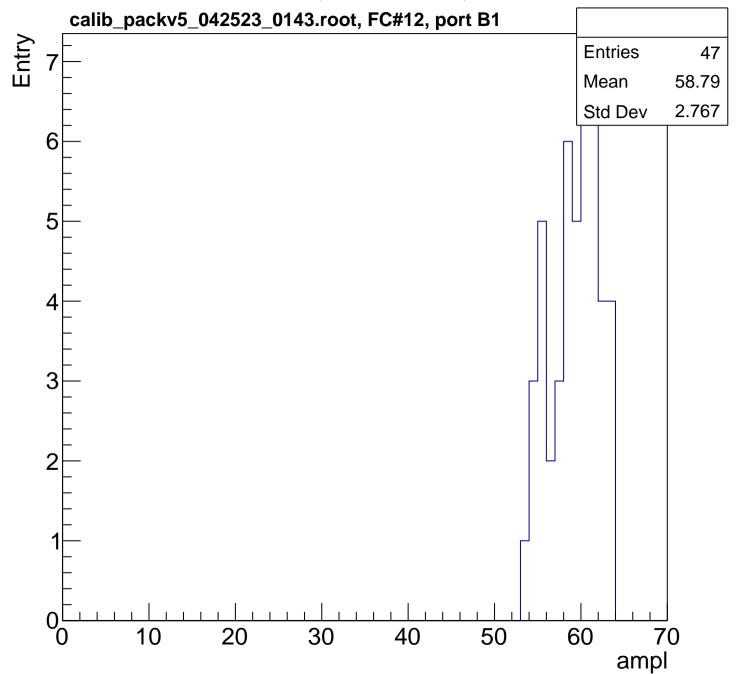


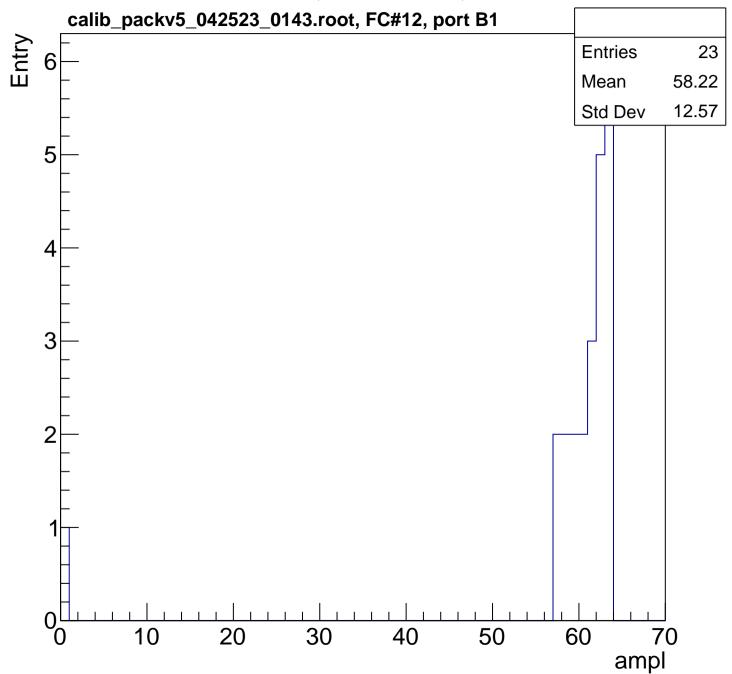




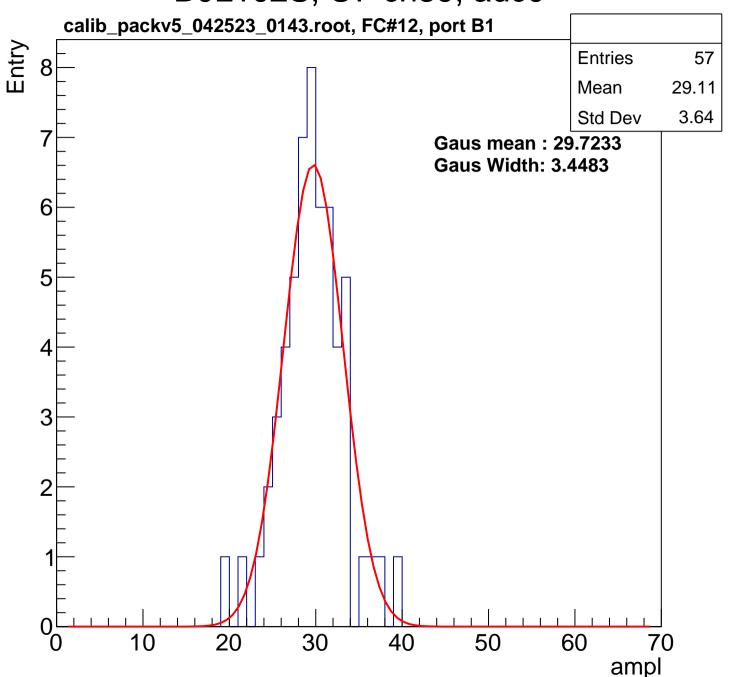


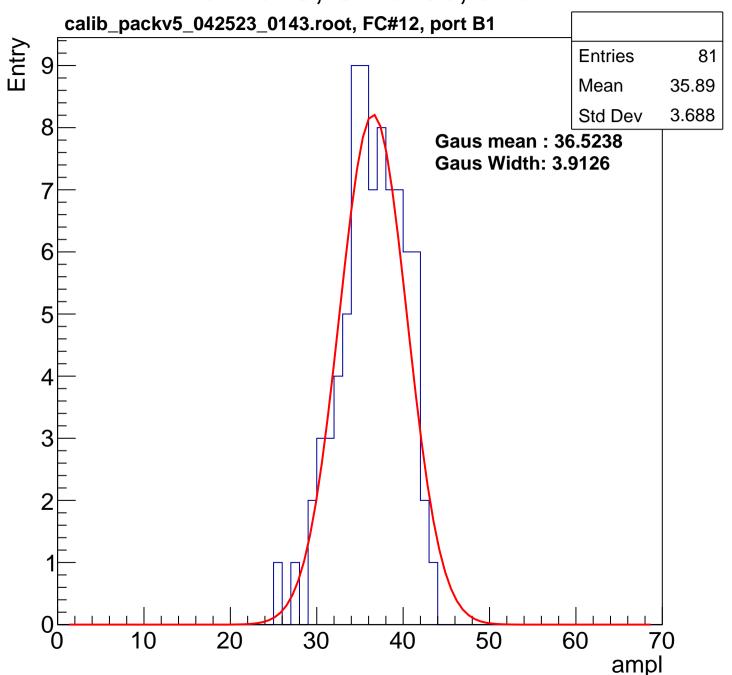


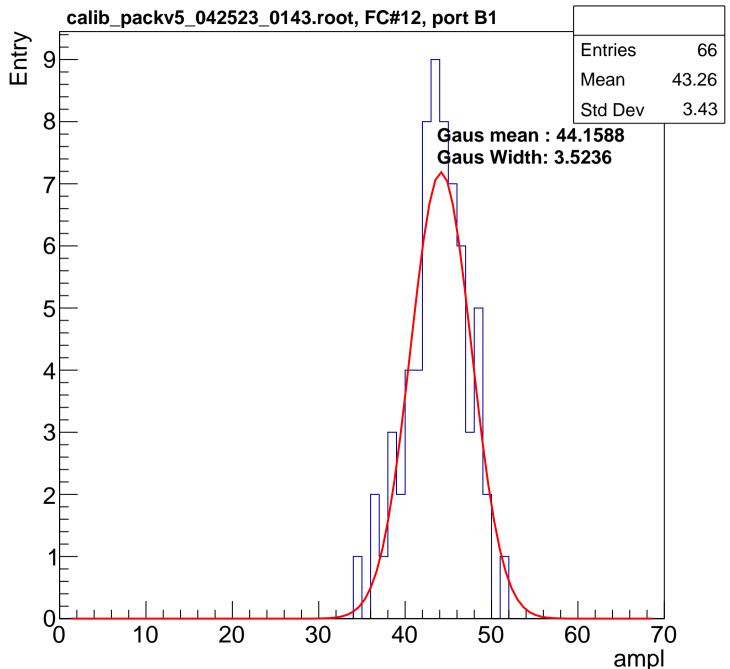


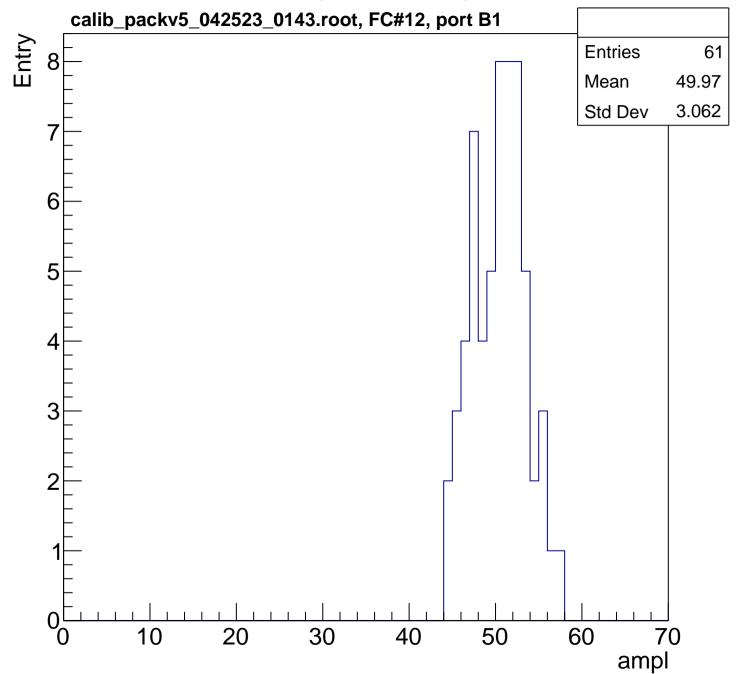


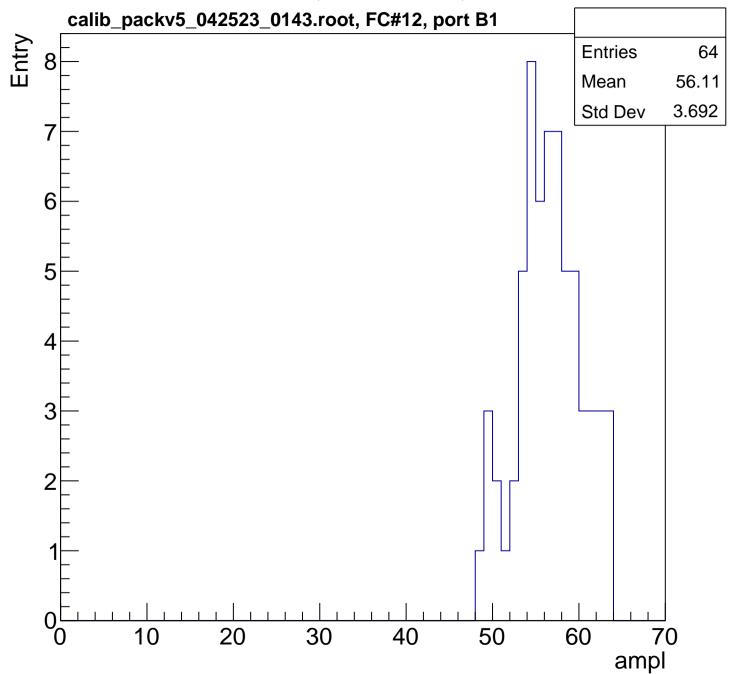
B0L102S, U7-ch38, adc7 calib_packv5_042523_0143.root, FC#12, port B1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

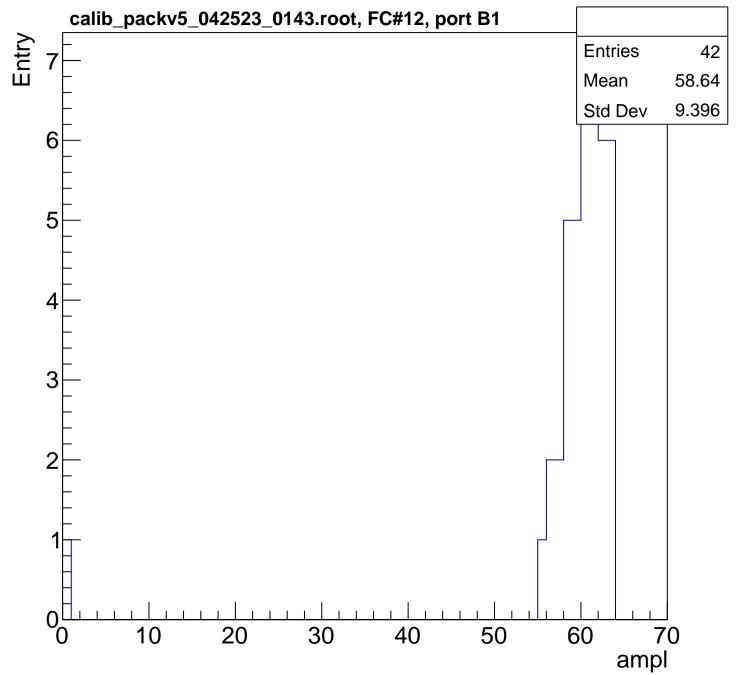


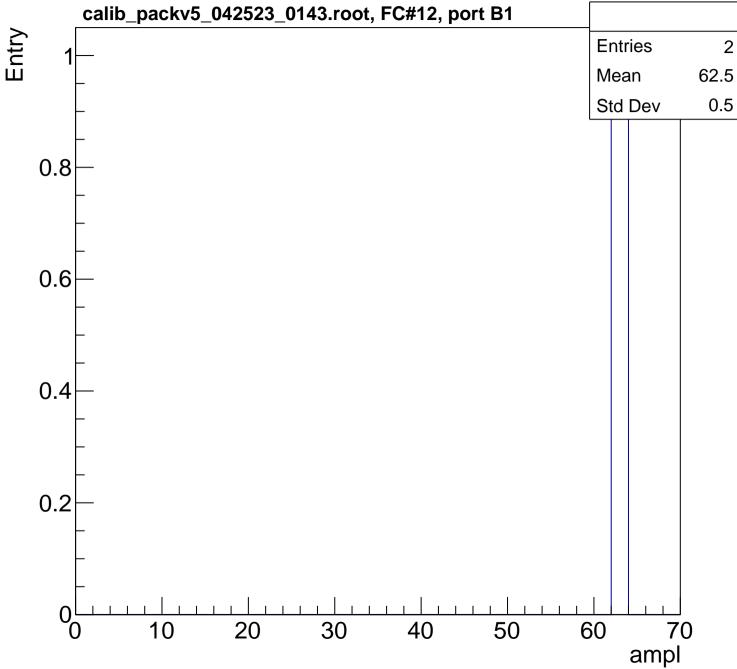




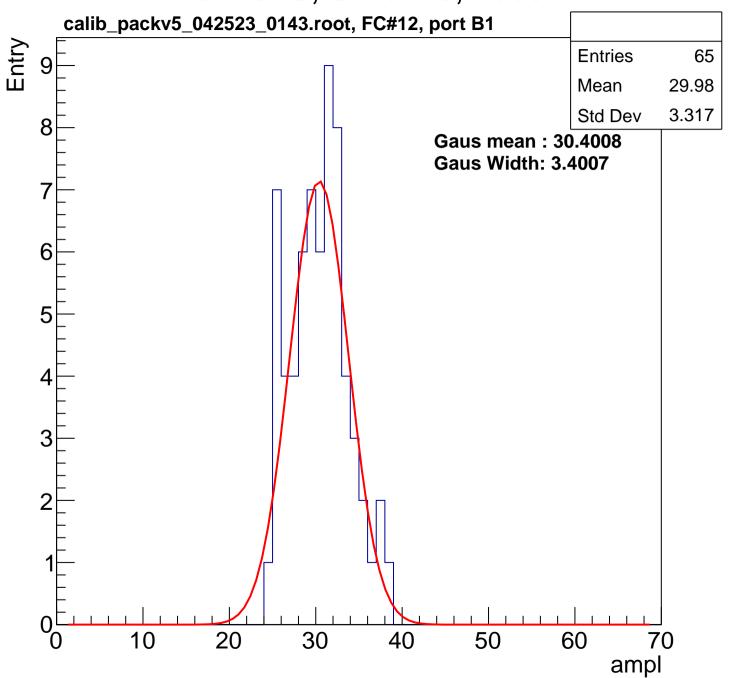


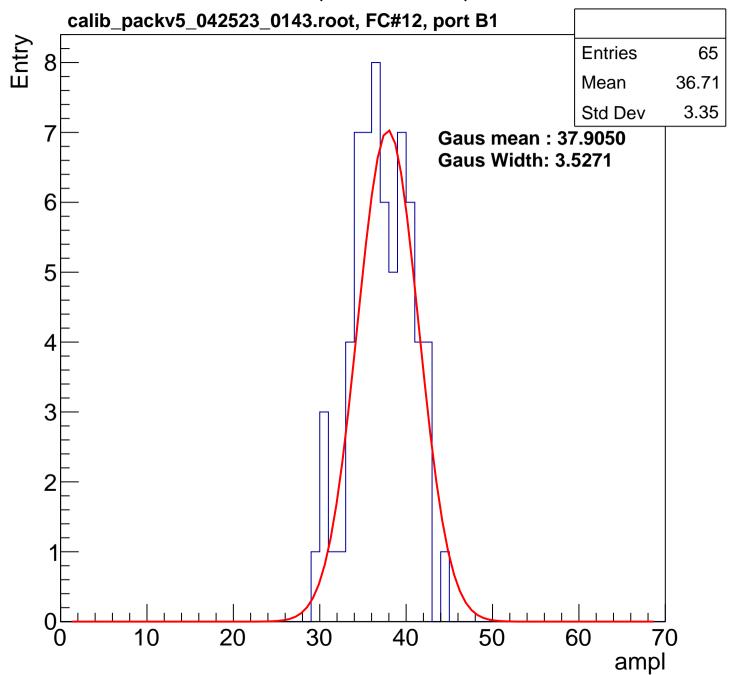


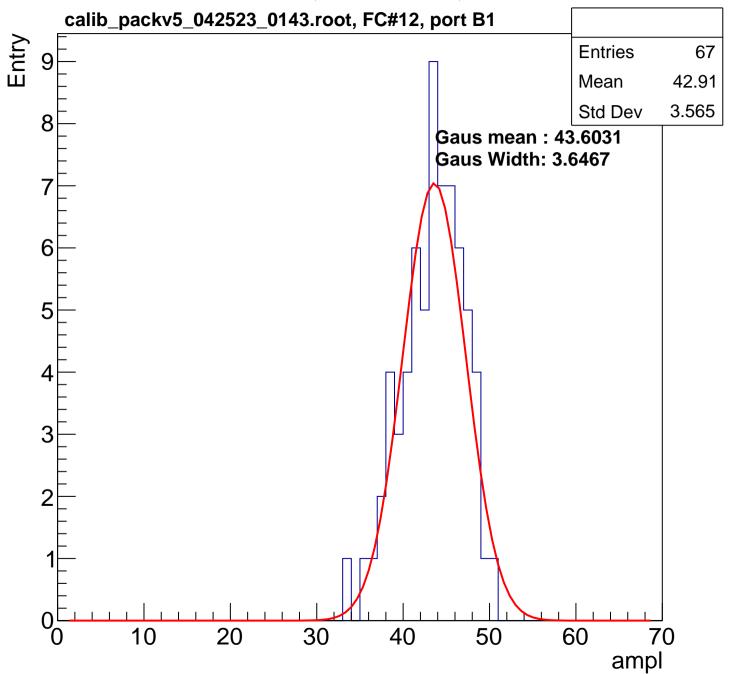


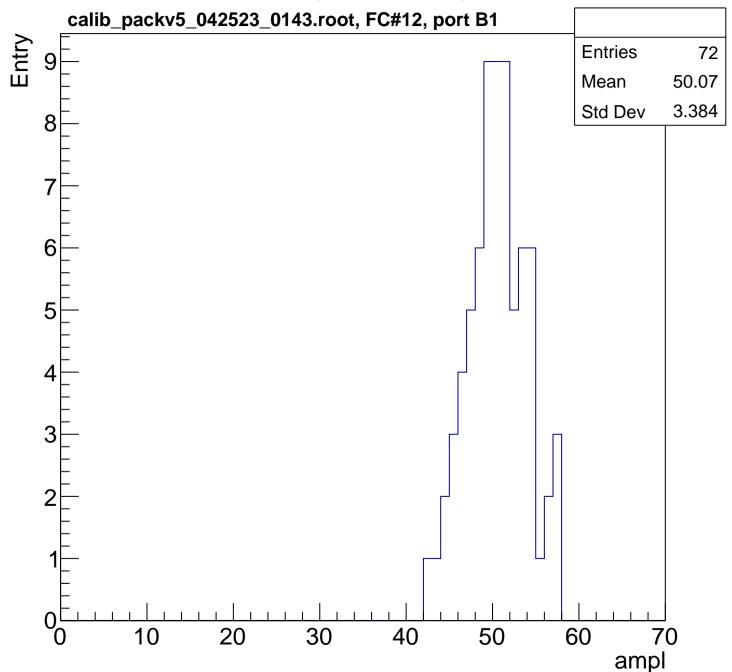


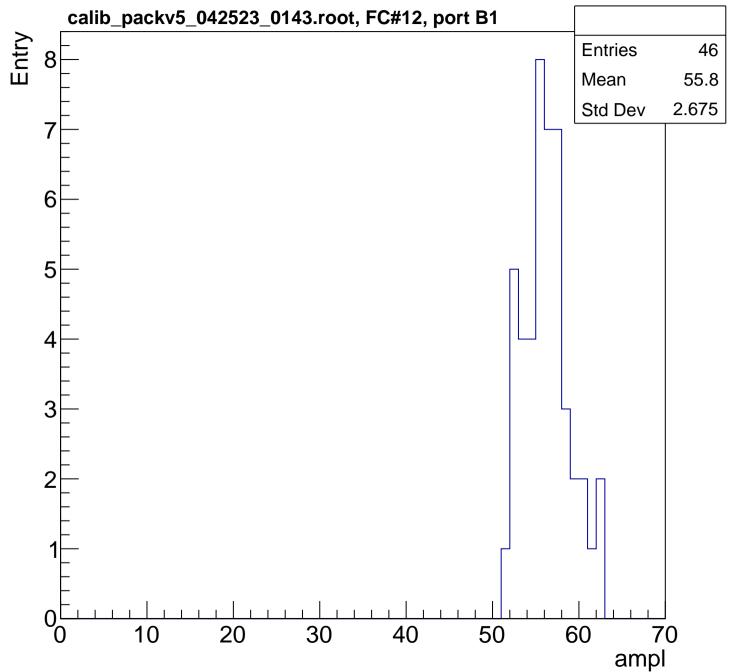


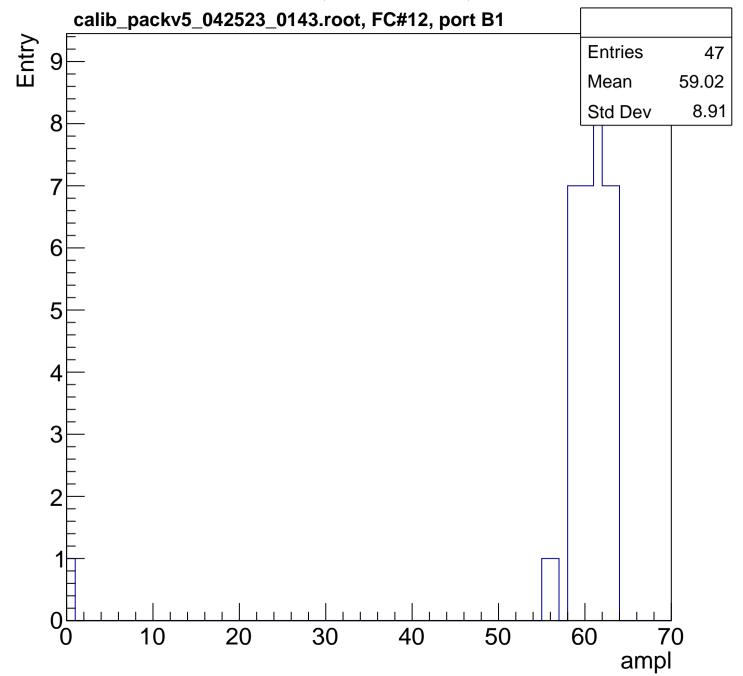


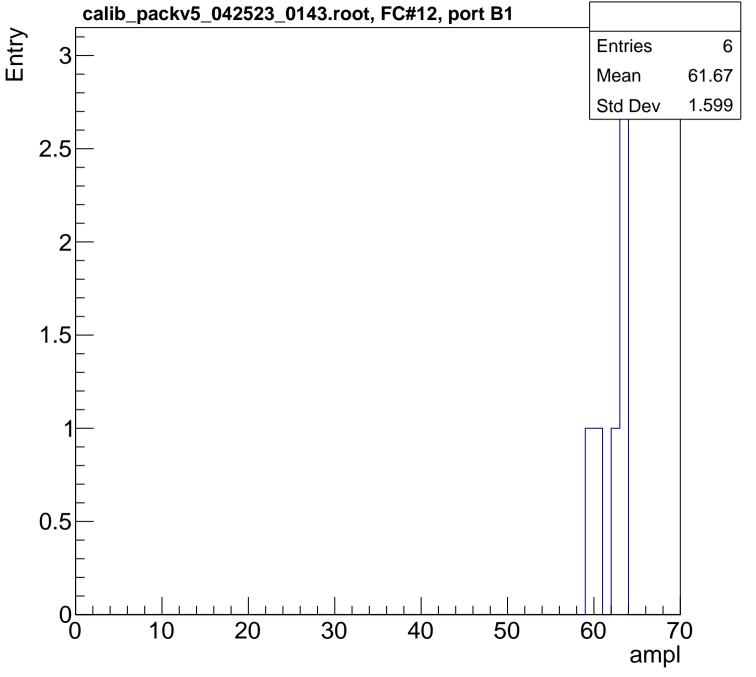


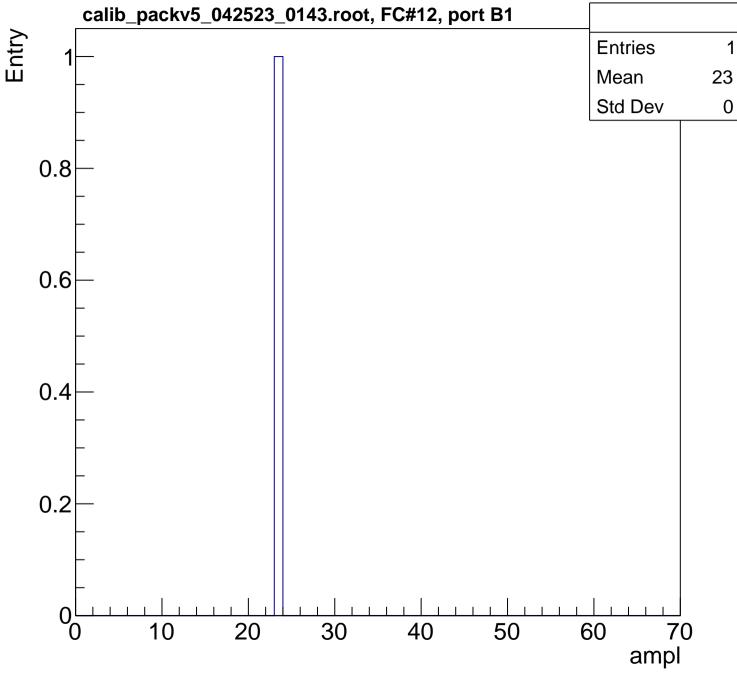


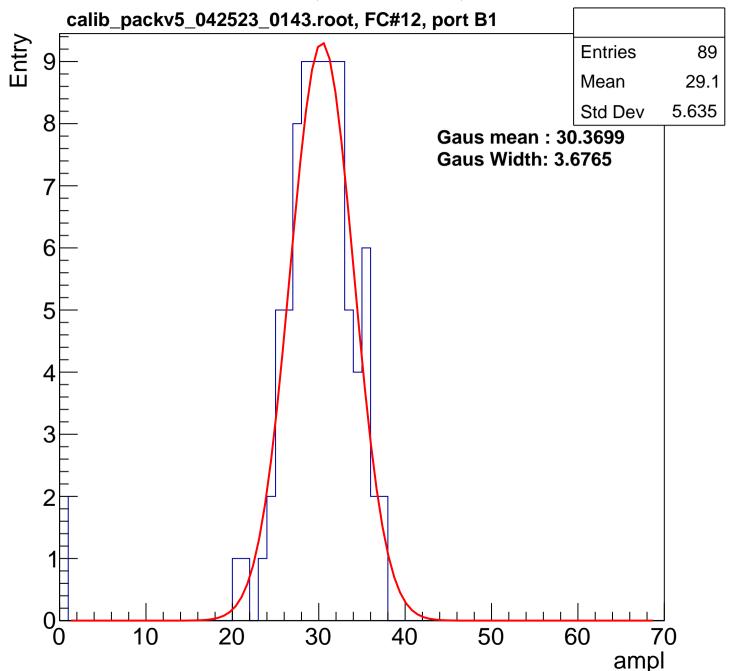


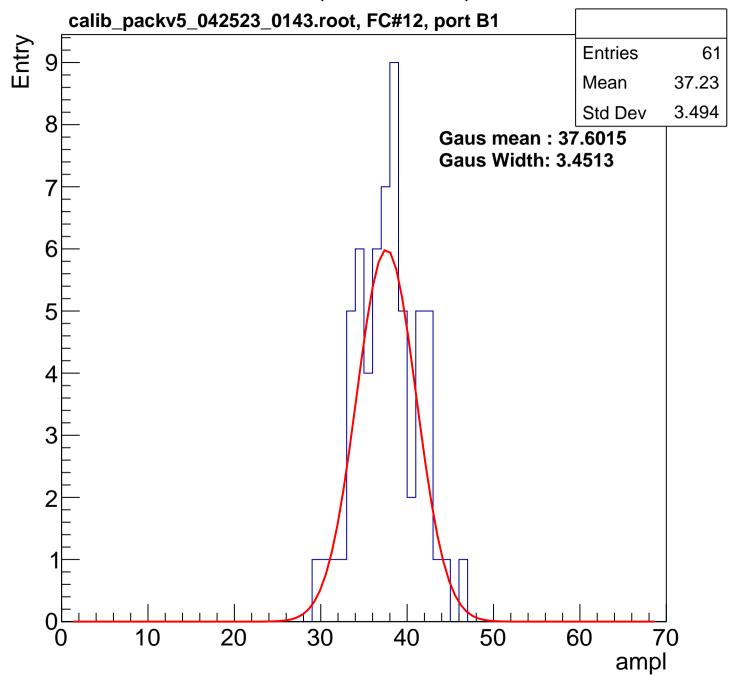


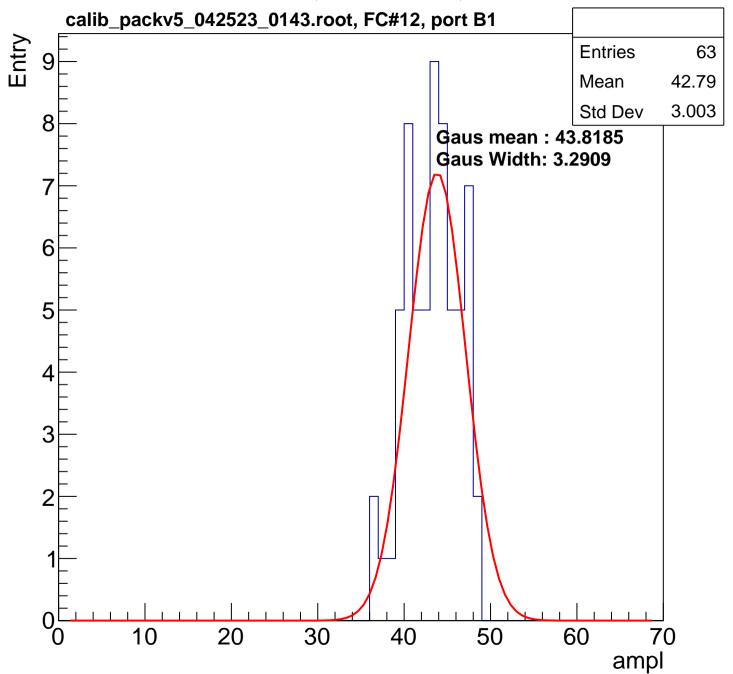


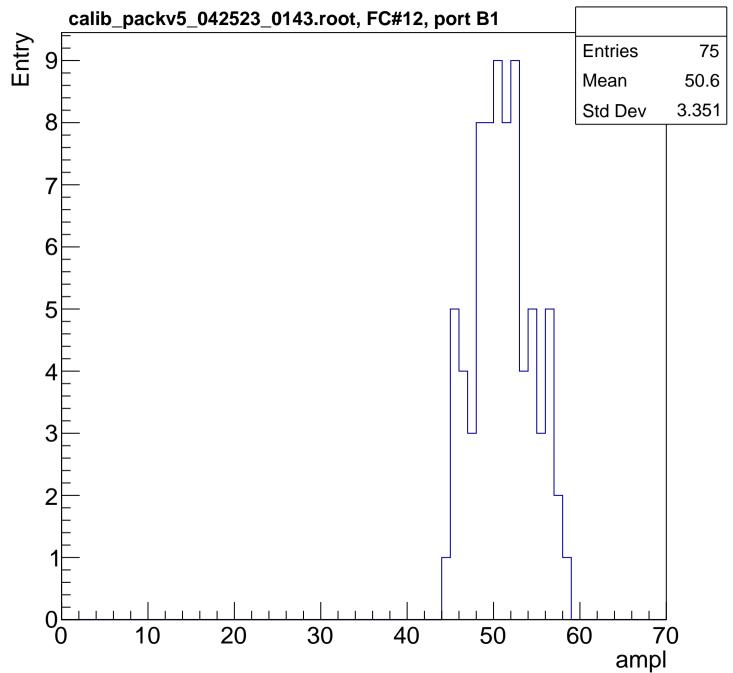


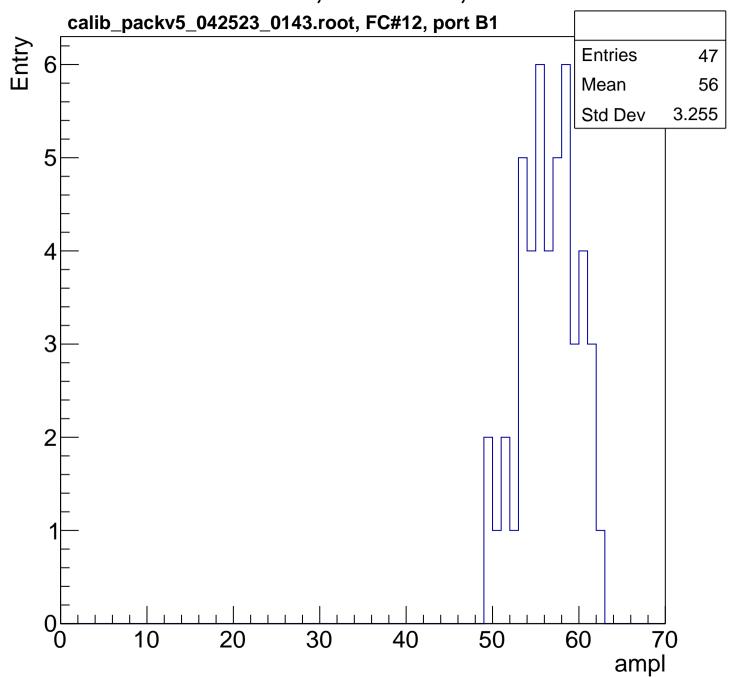


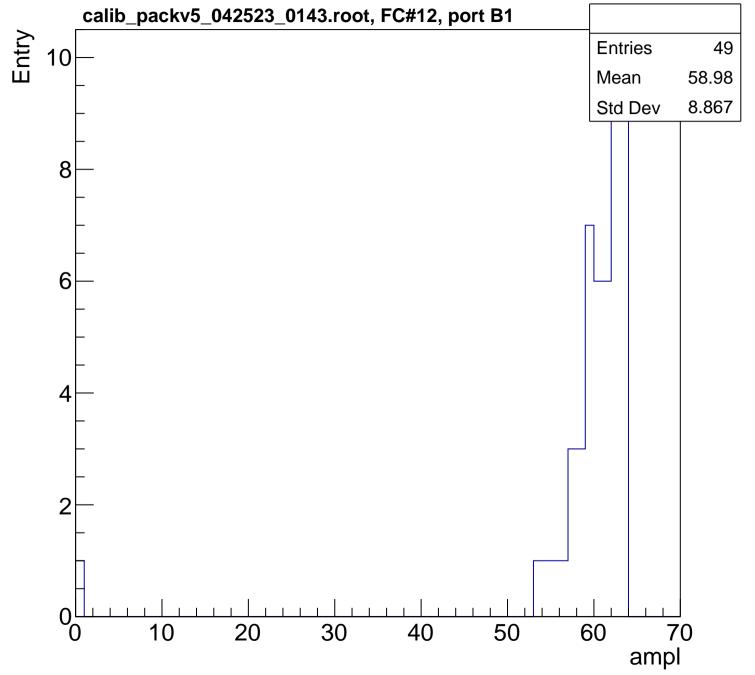


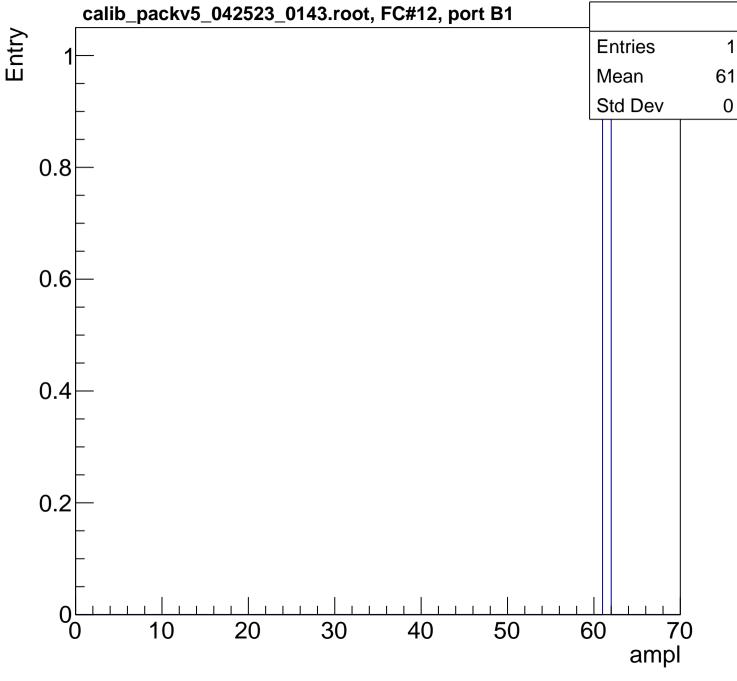


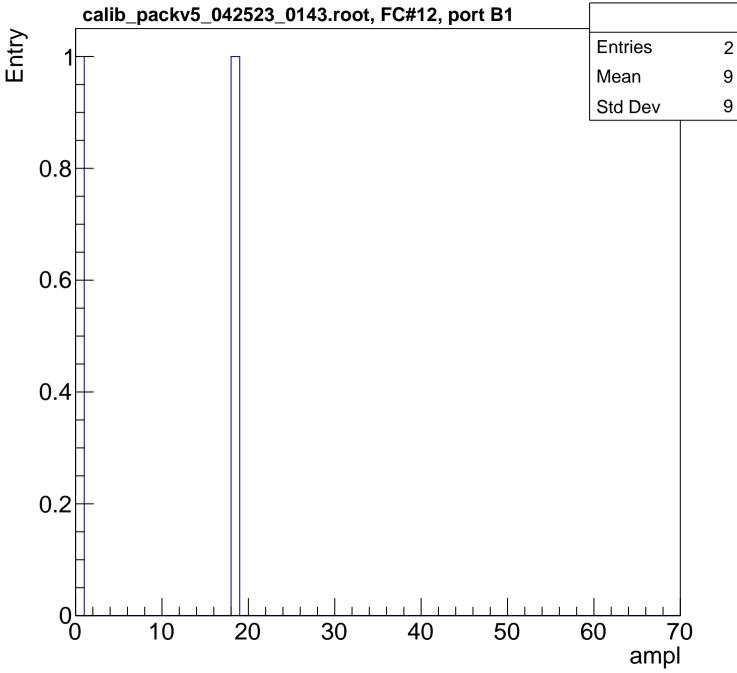


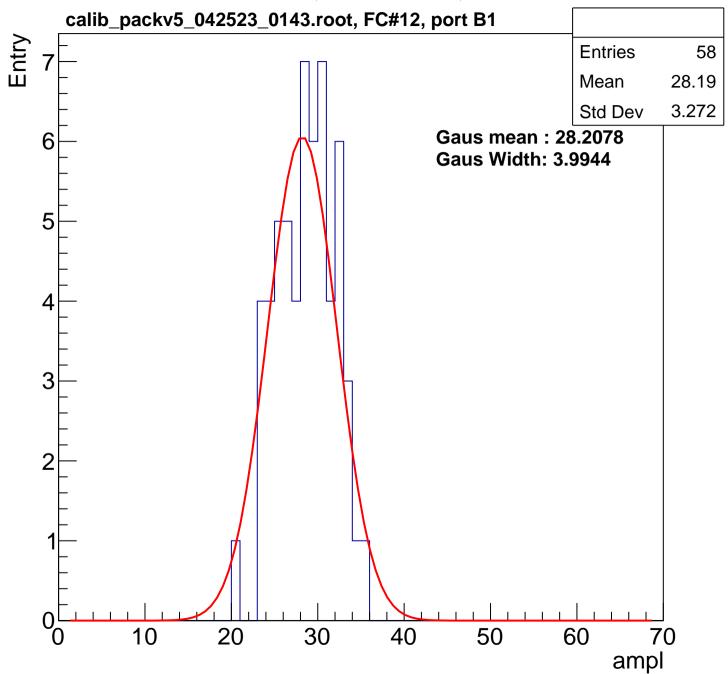


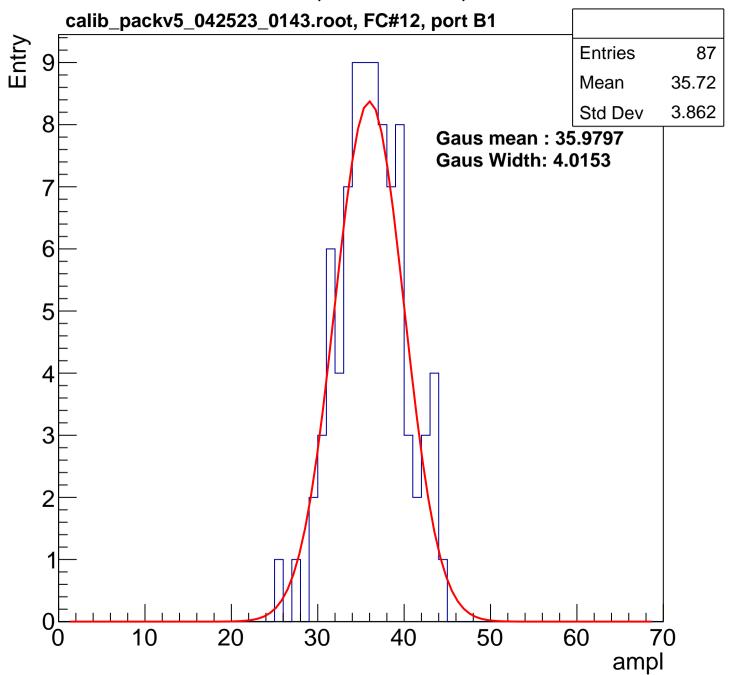


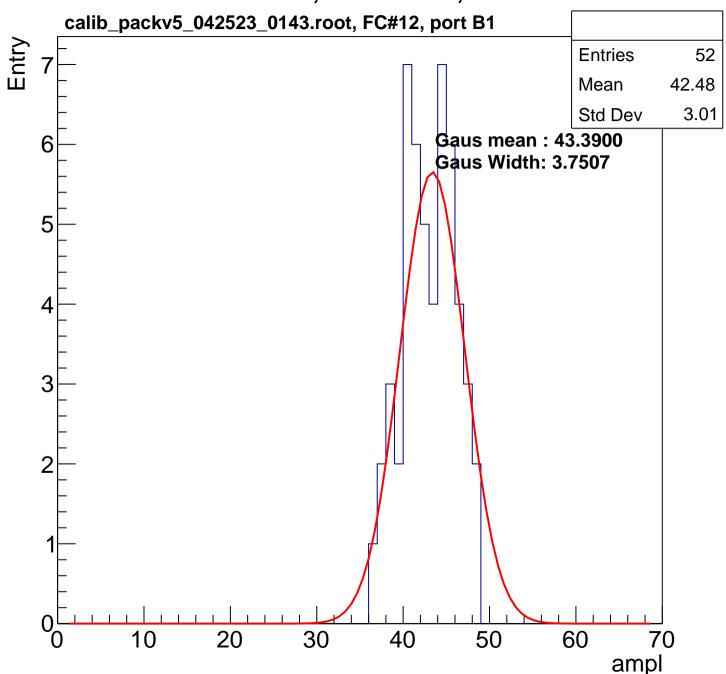


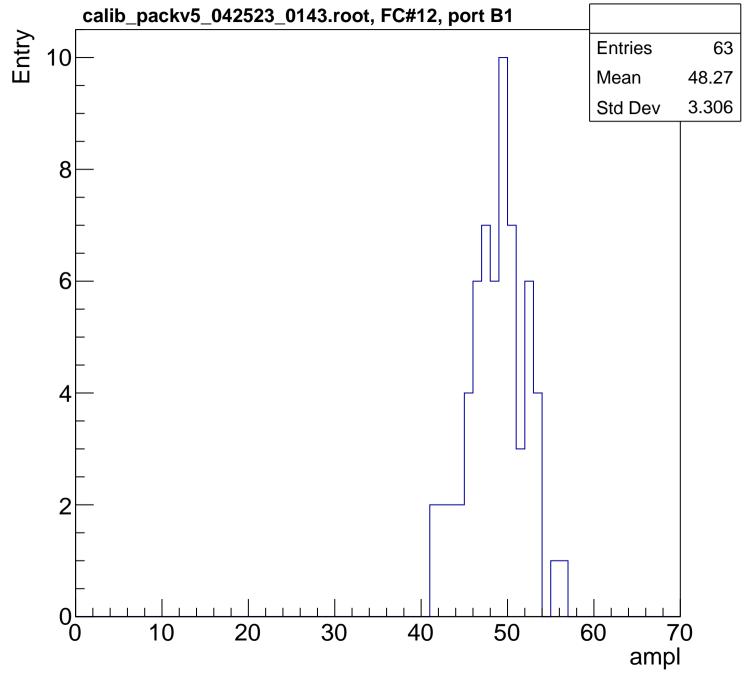


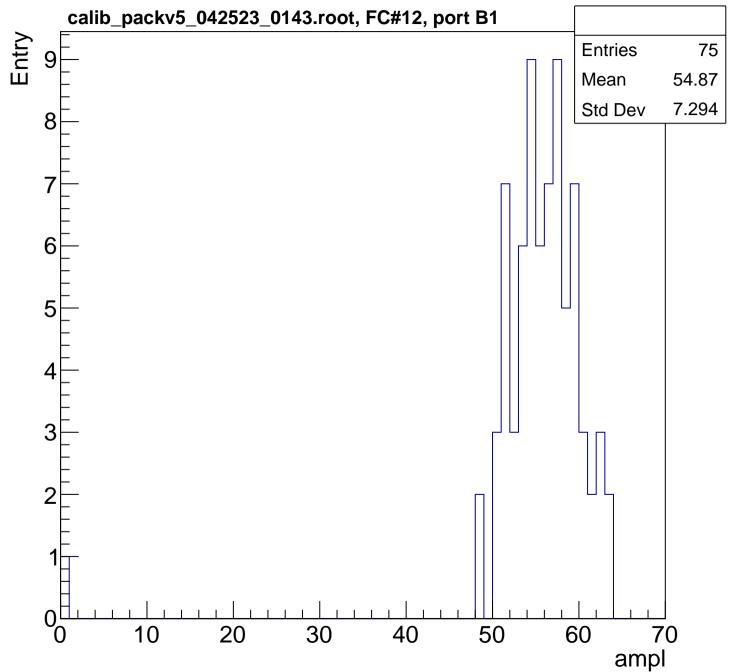


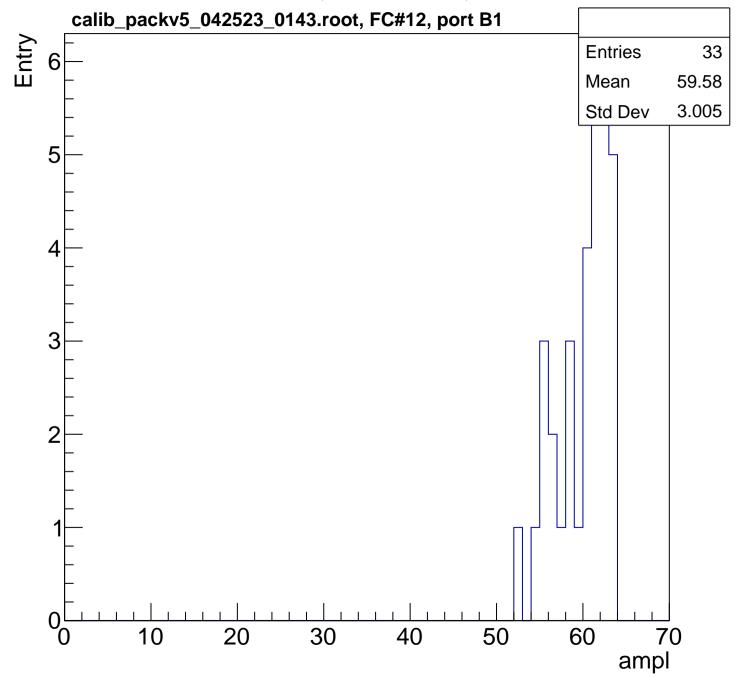


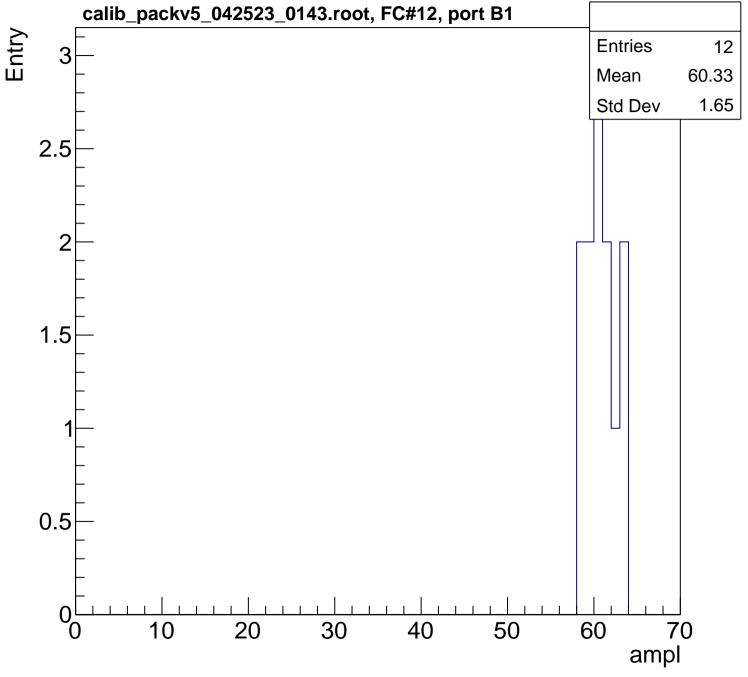




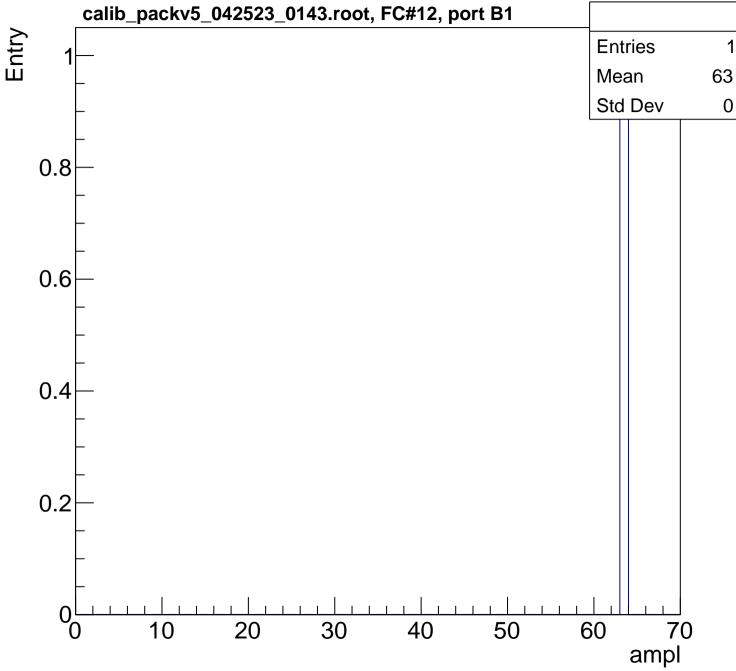


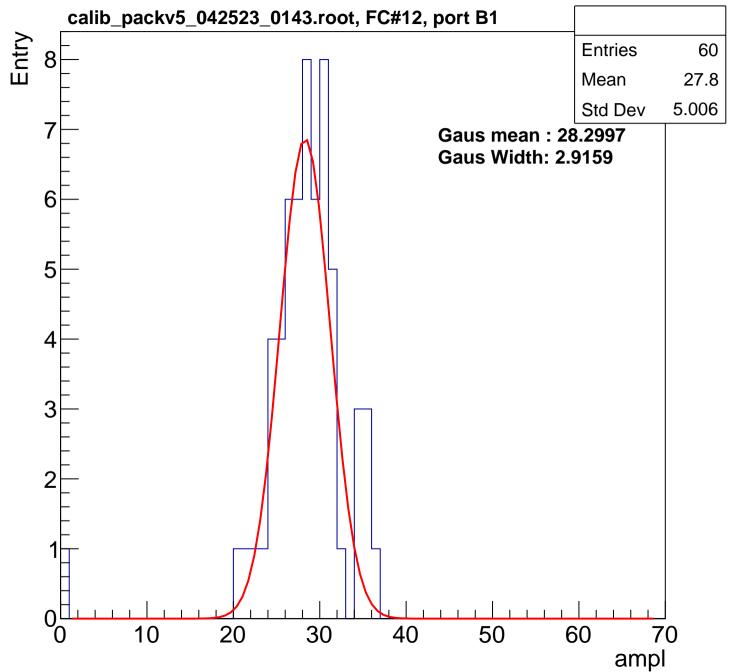


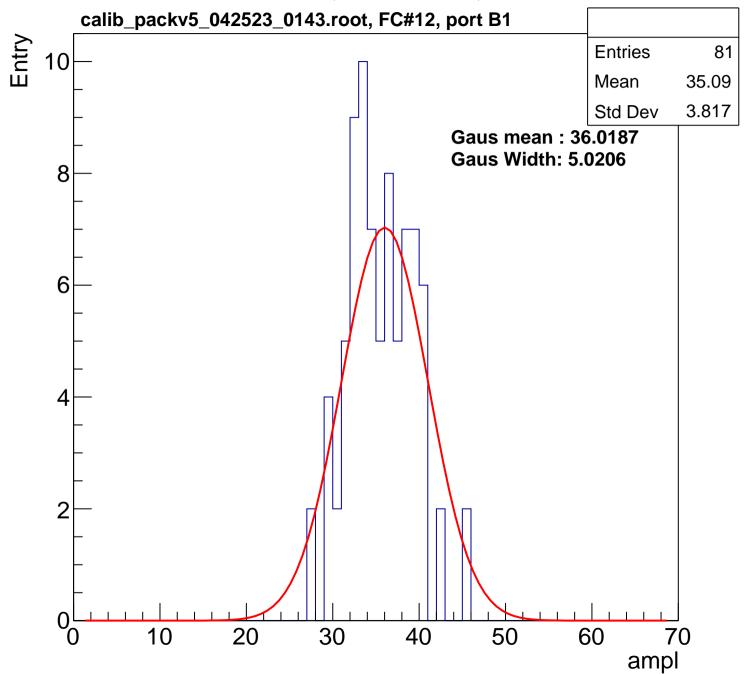


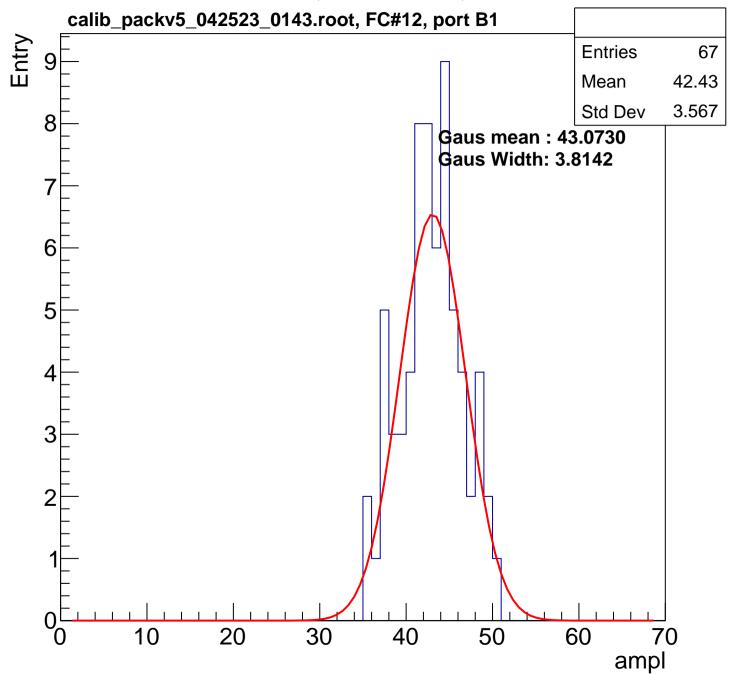


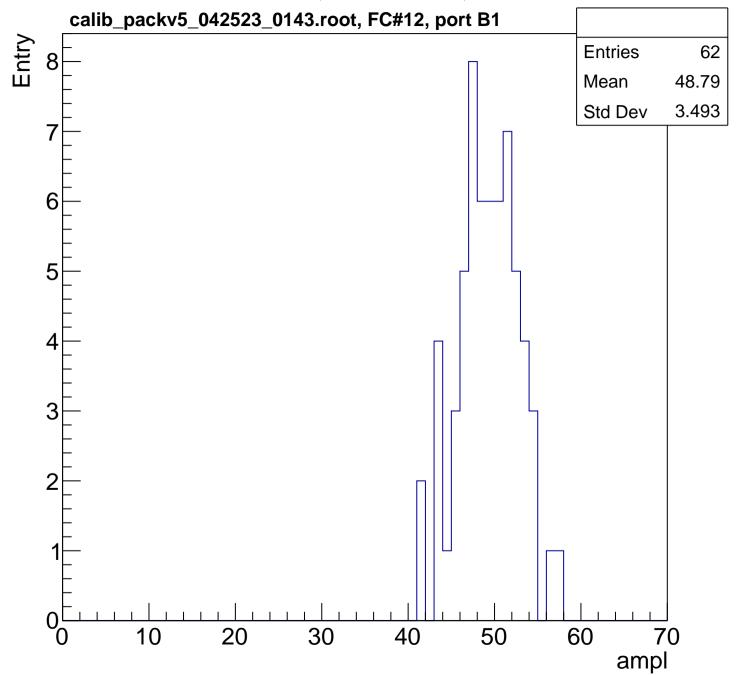
0

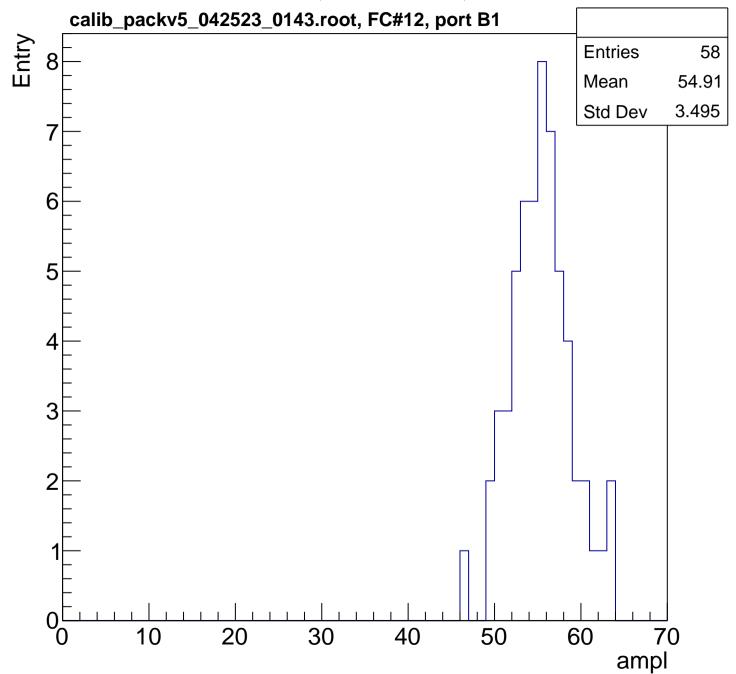


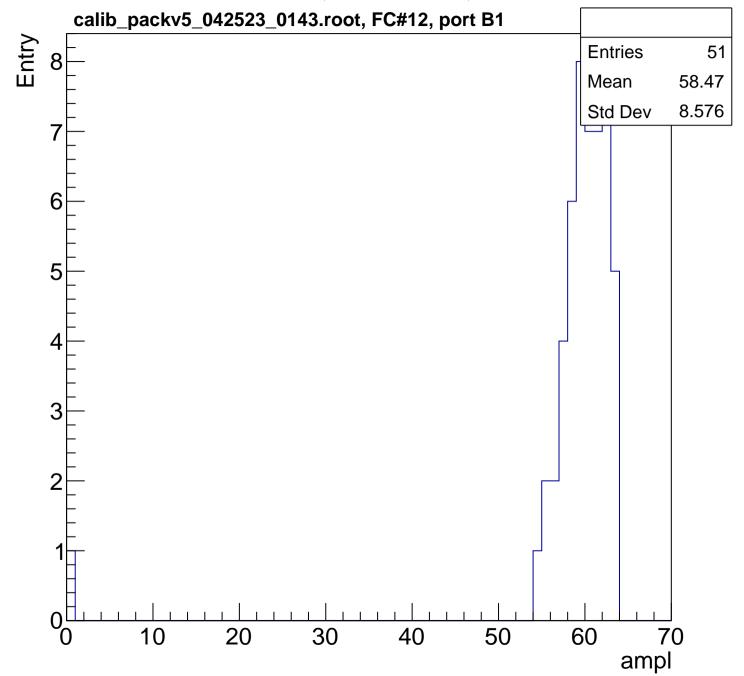


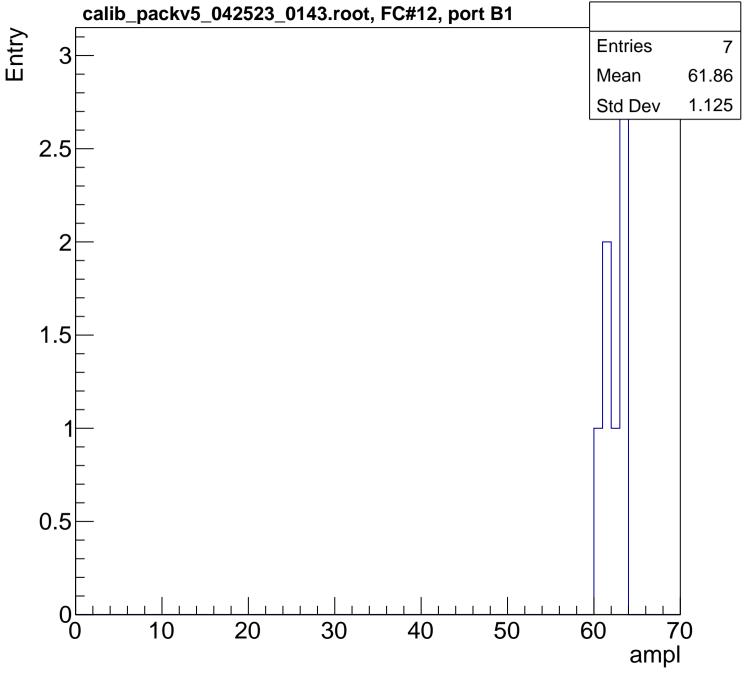




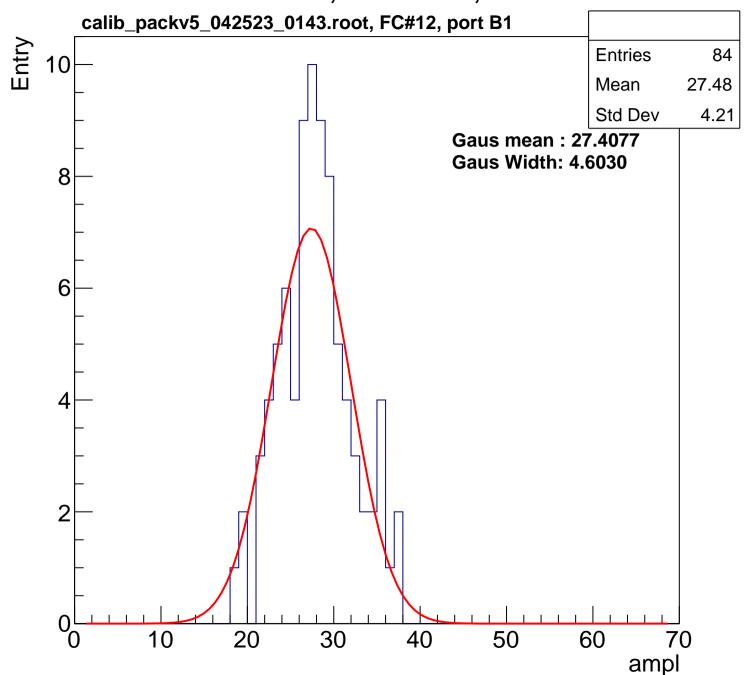


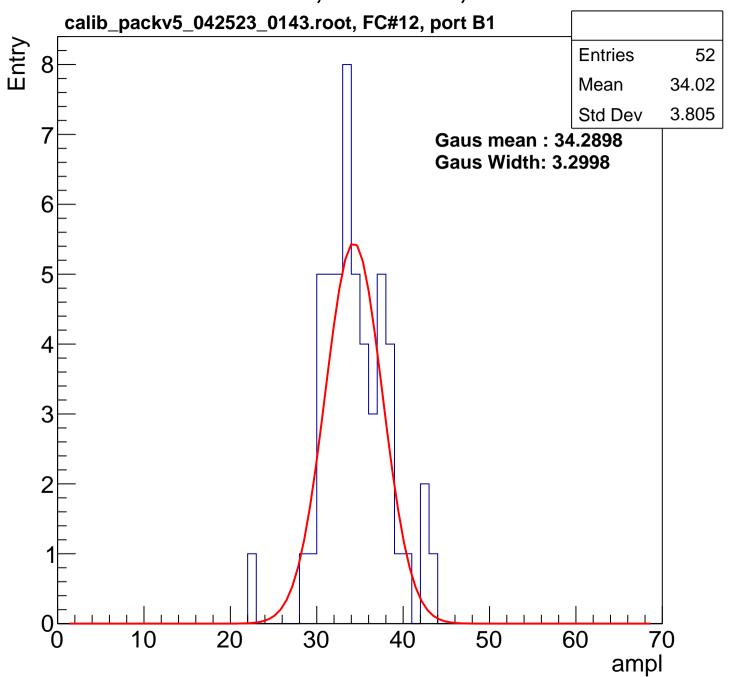


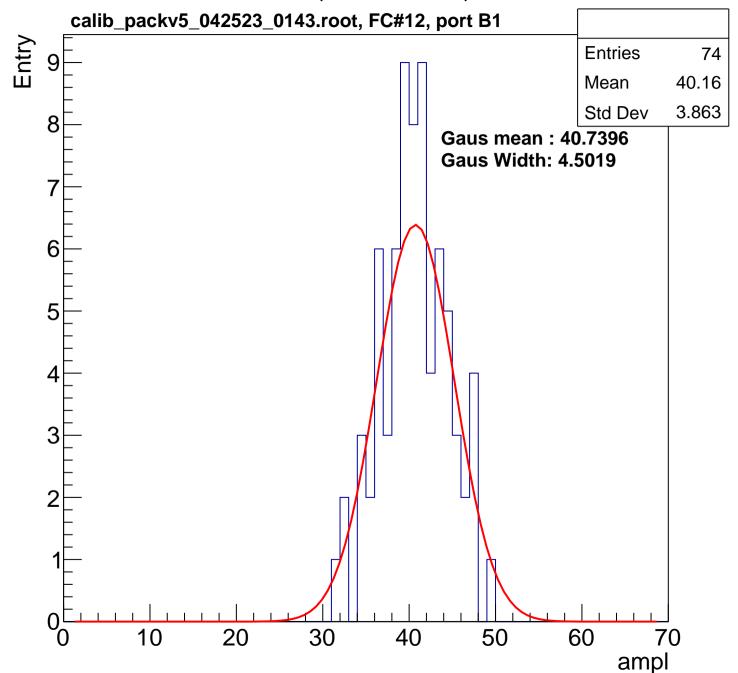


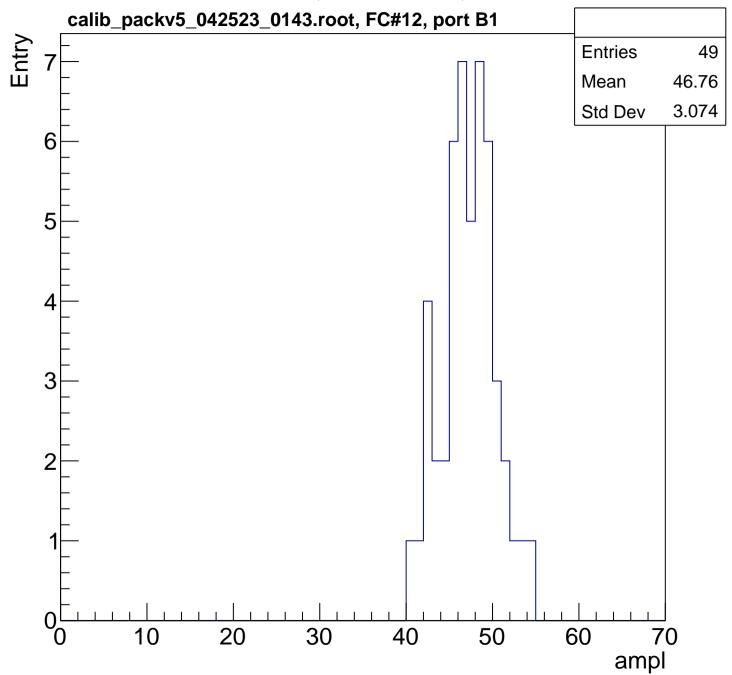


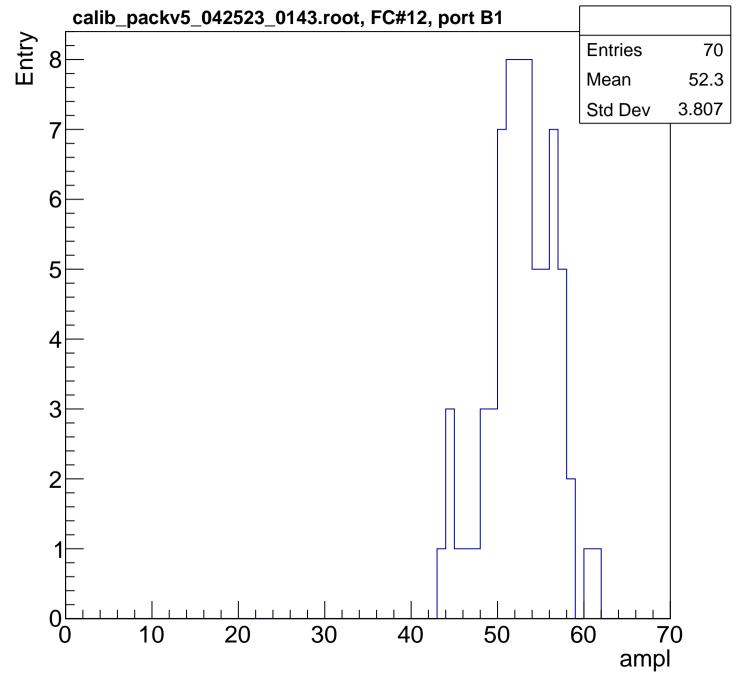
B0L102S, U7-ch43, adc7 calib_packv5_042523_0143.root, FC#12, port B1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

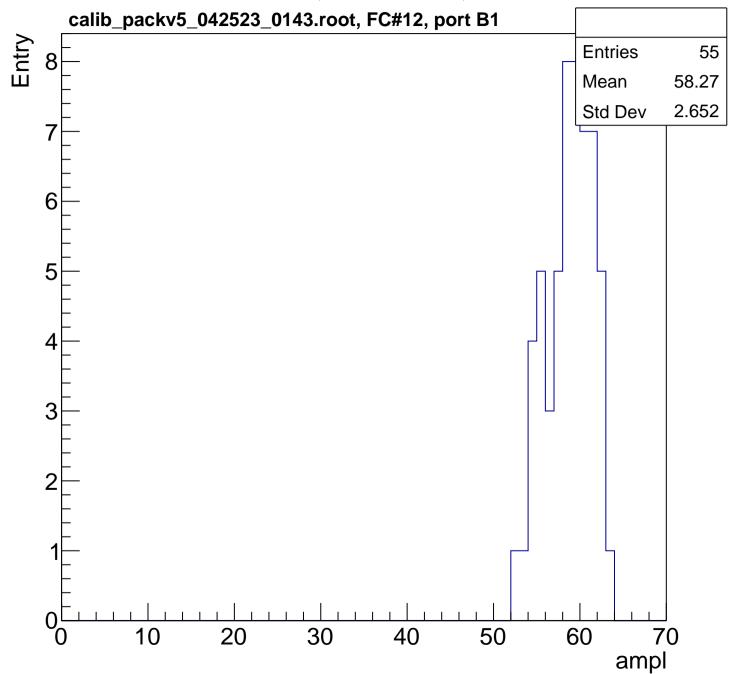


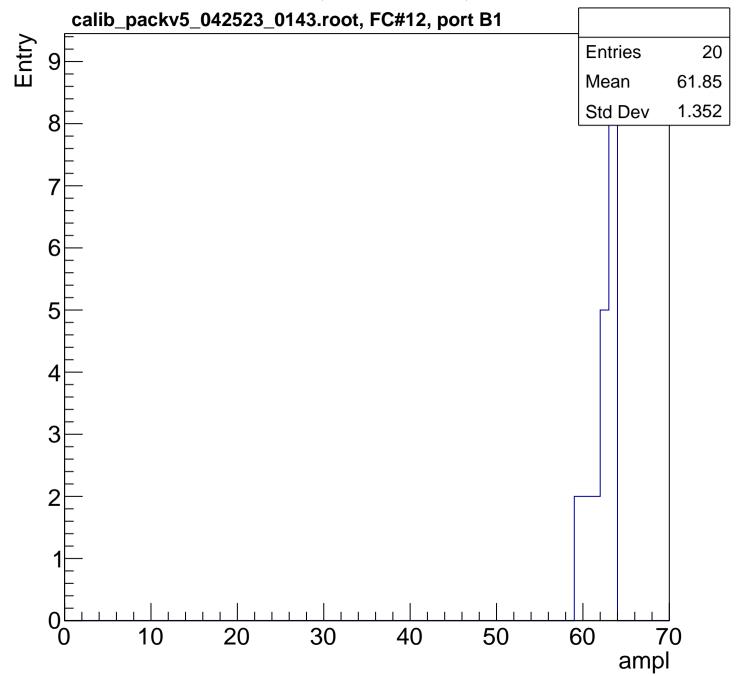


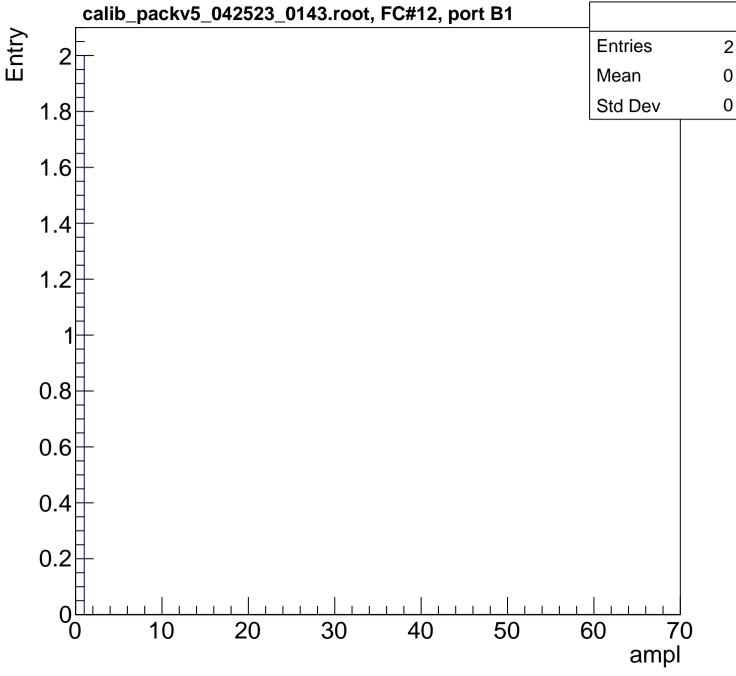


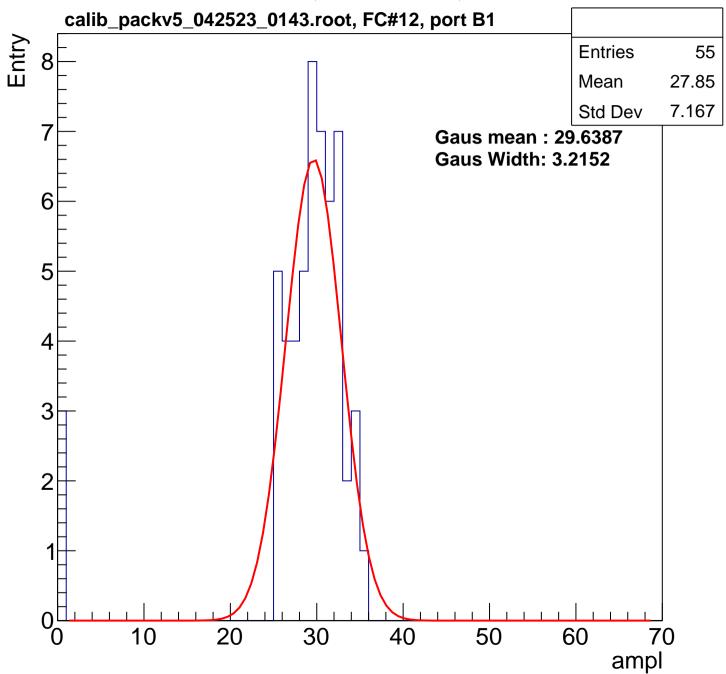


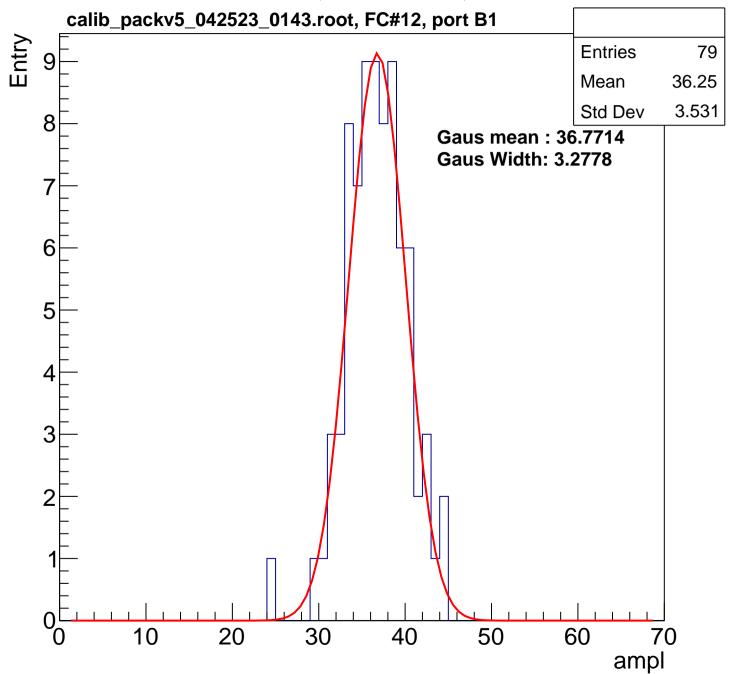


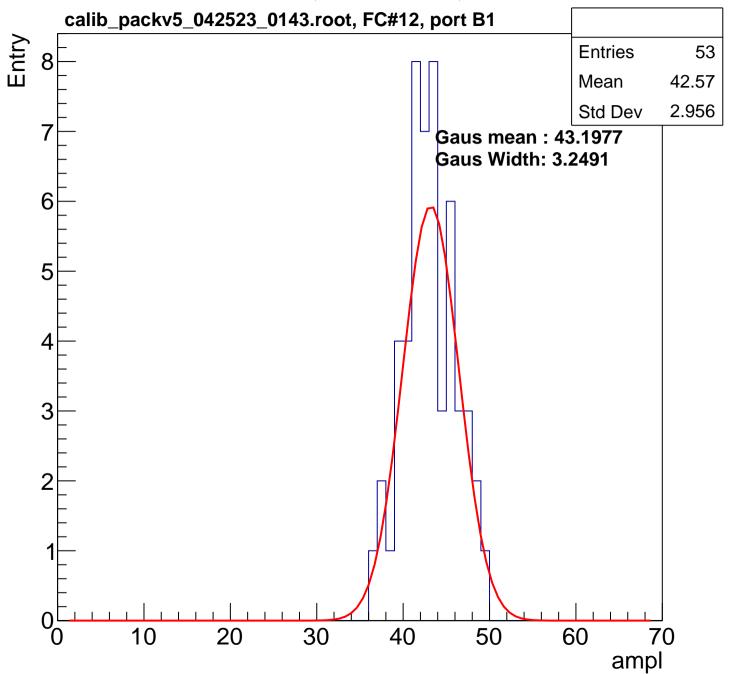


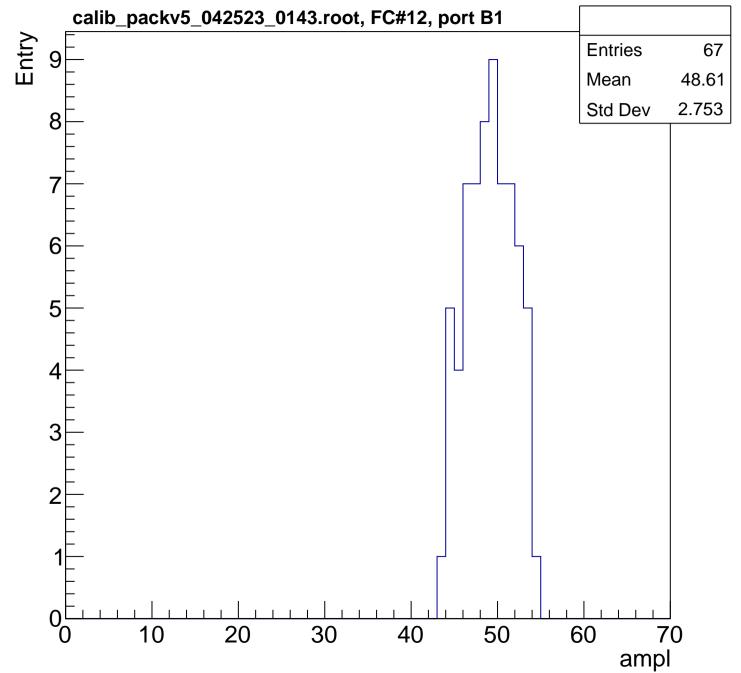


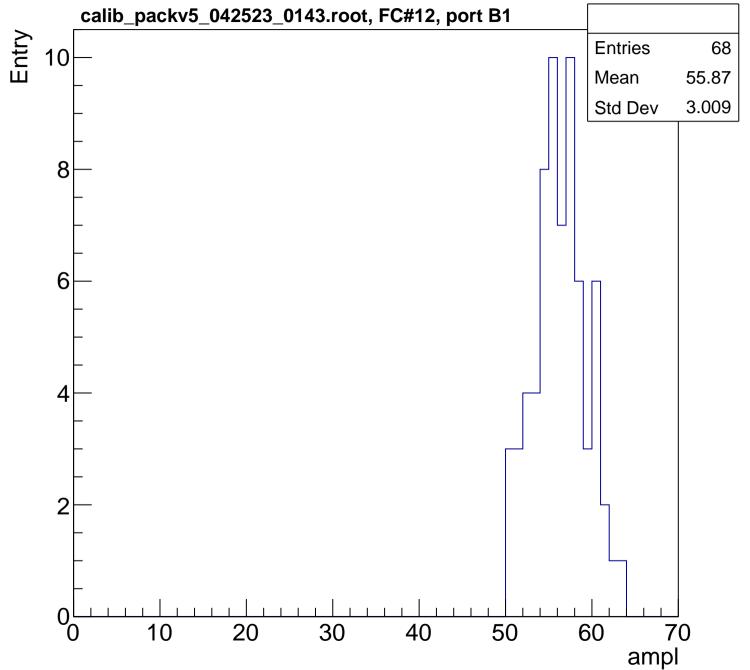


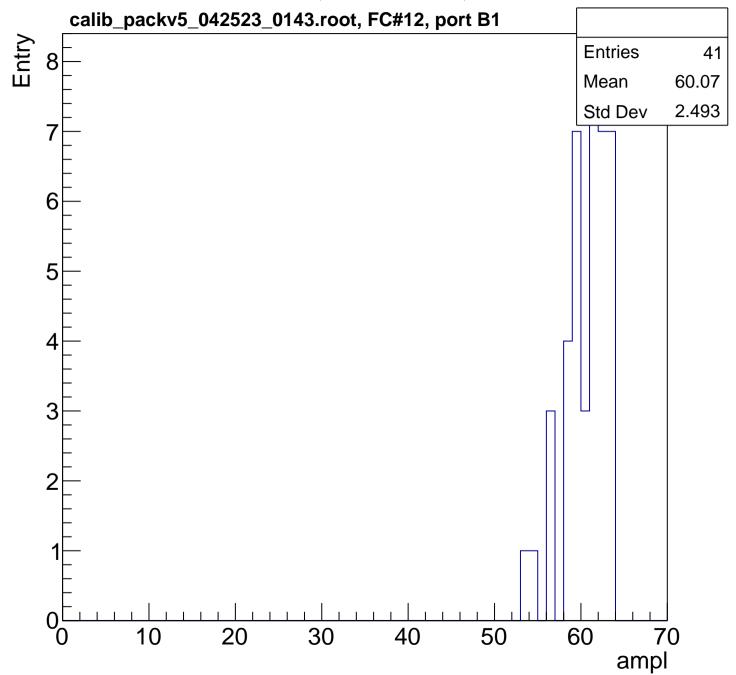


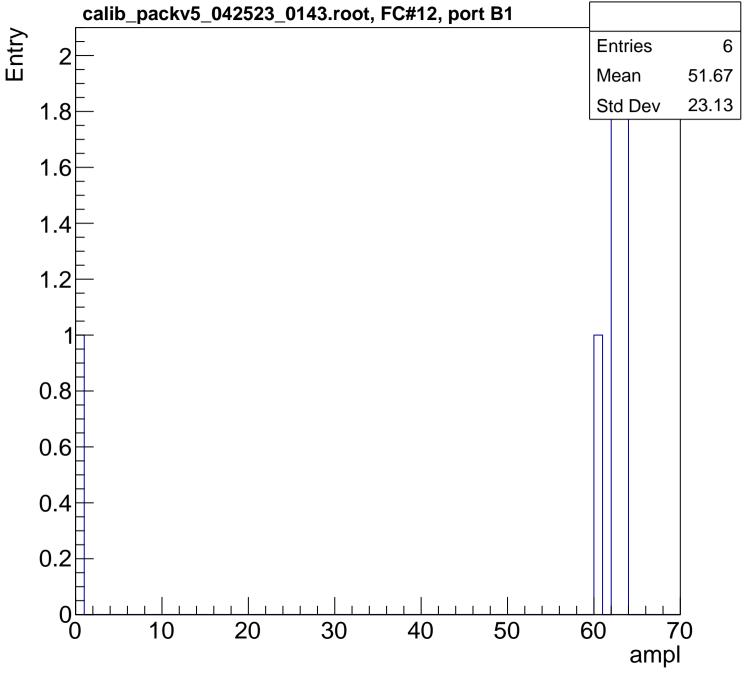




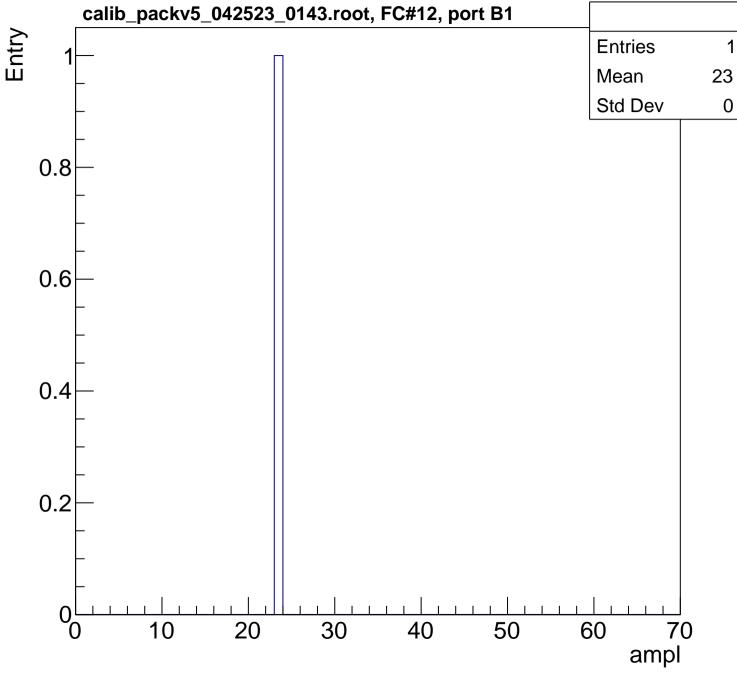


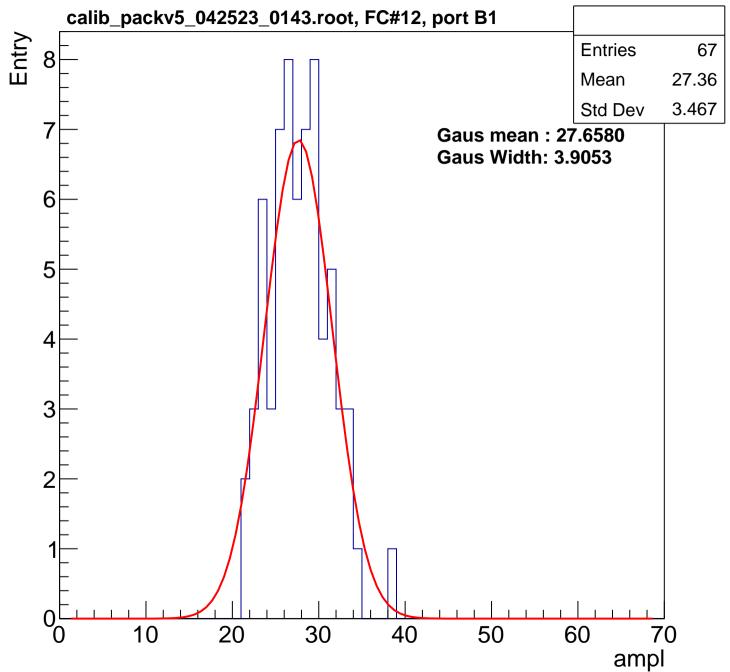


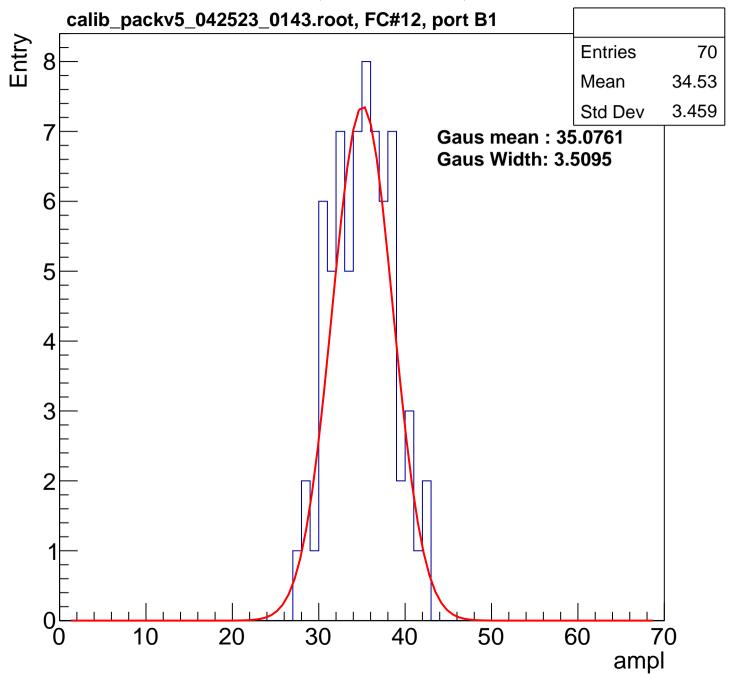


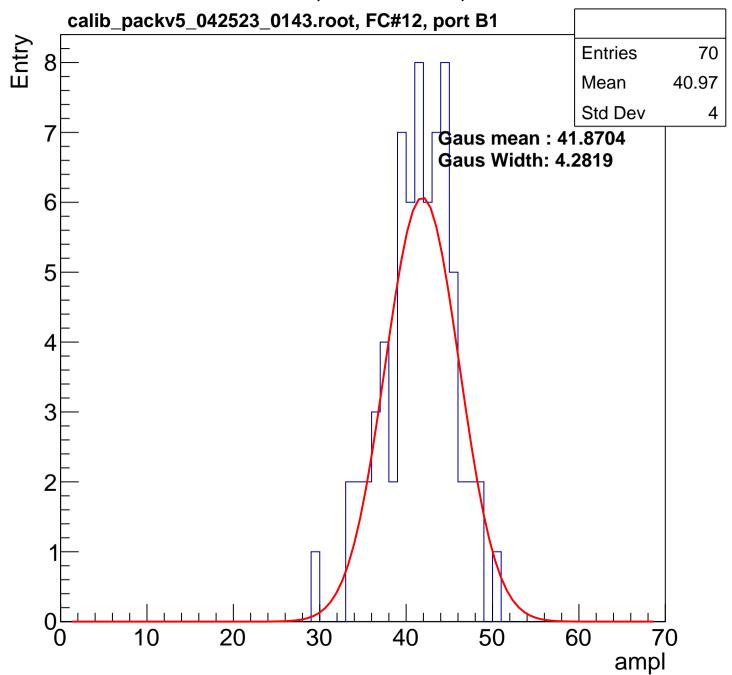


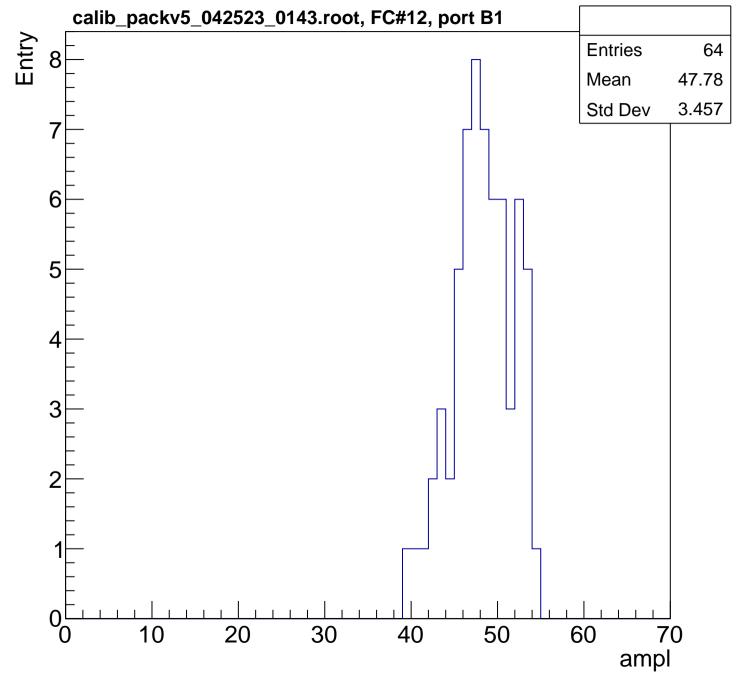
0

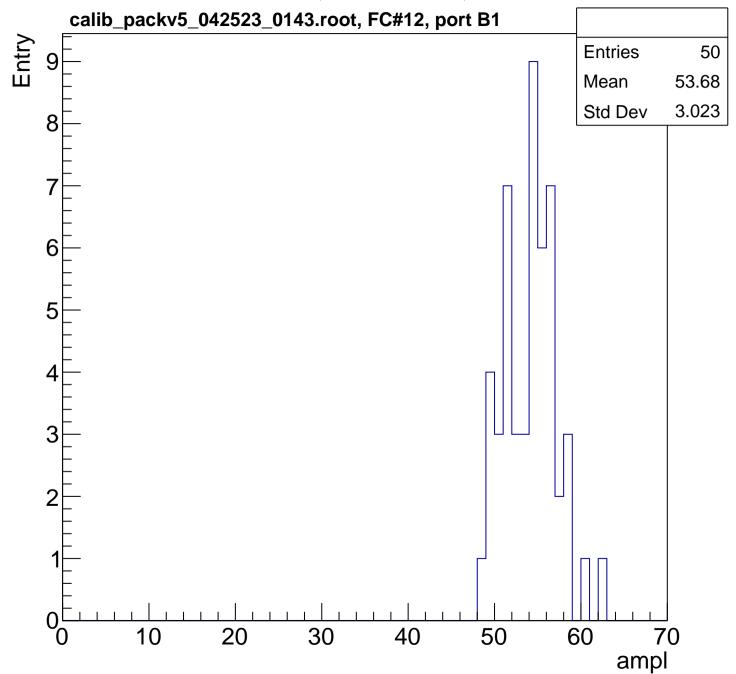


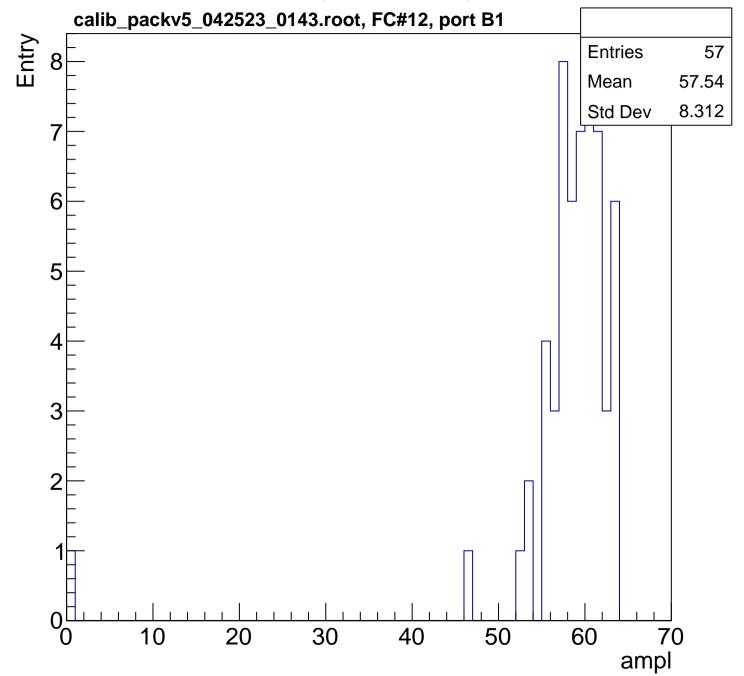


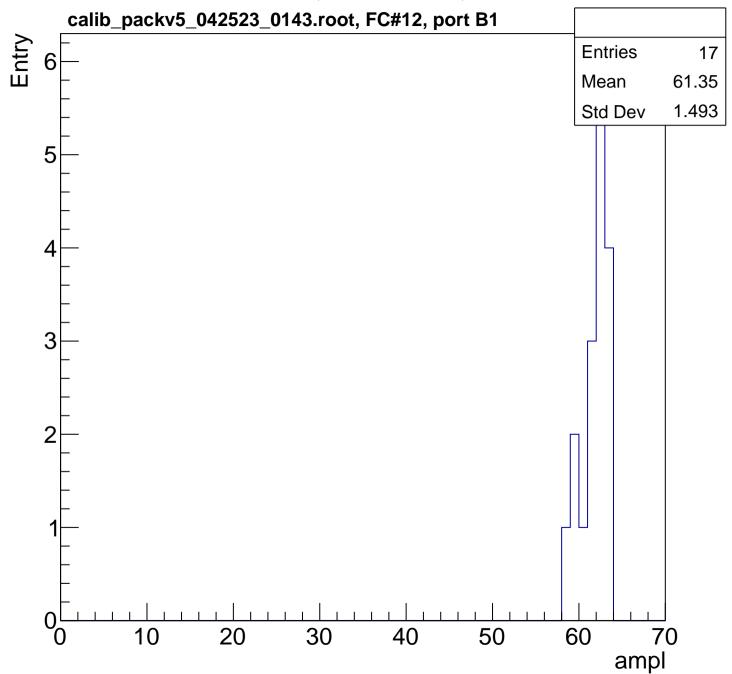


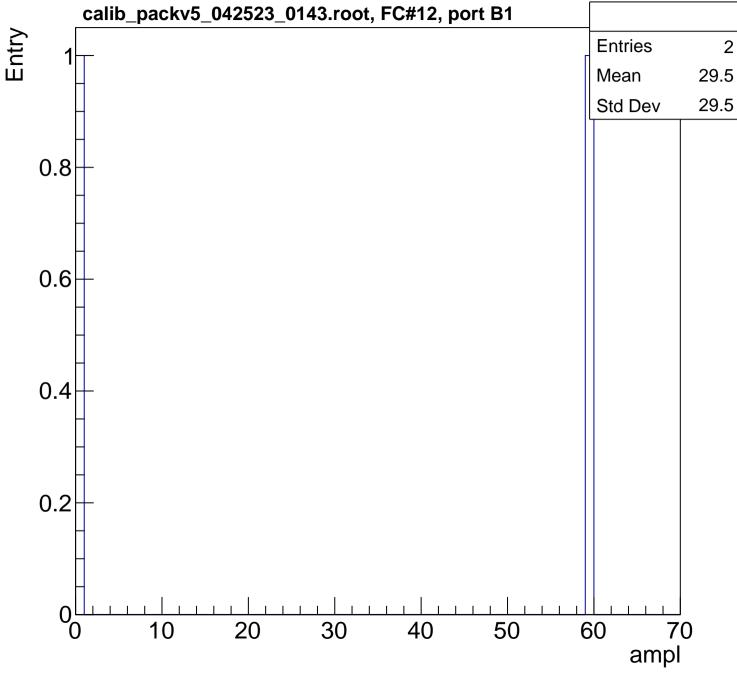


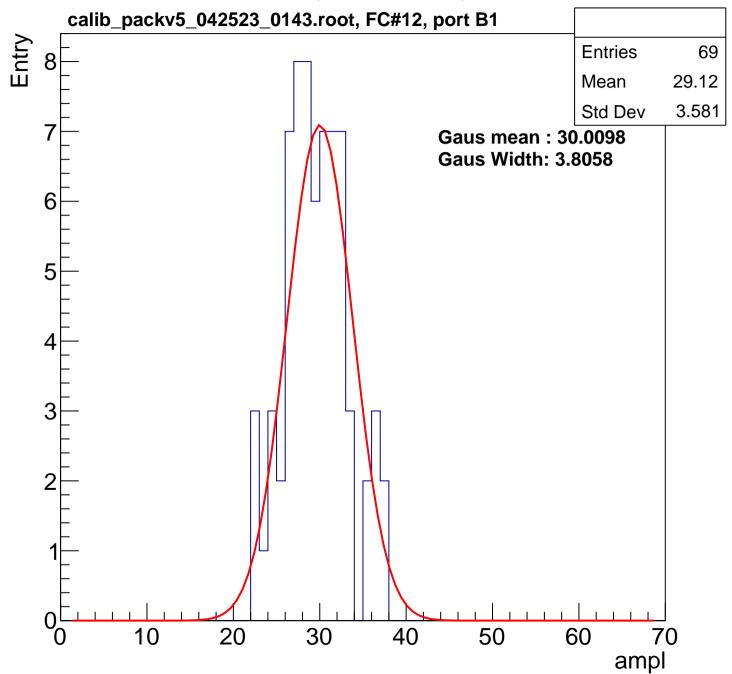


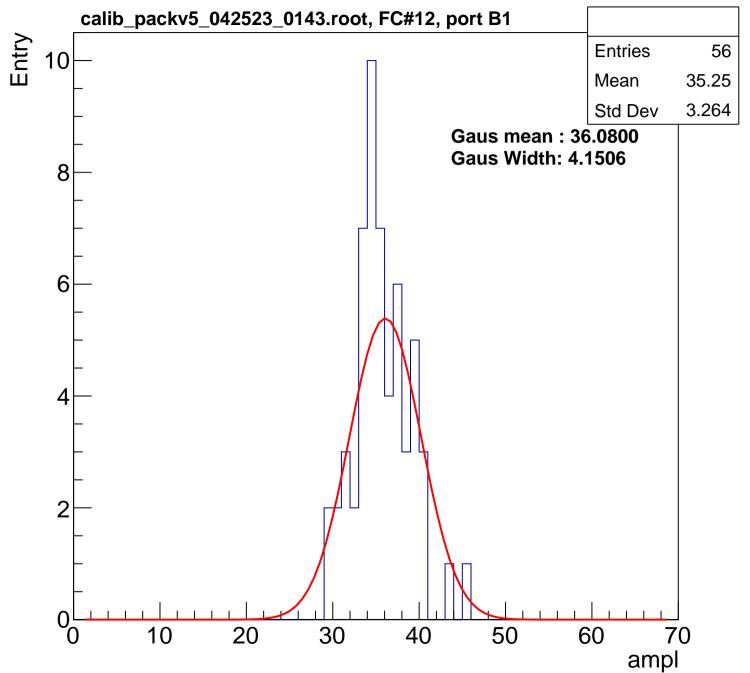


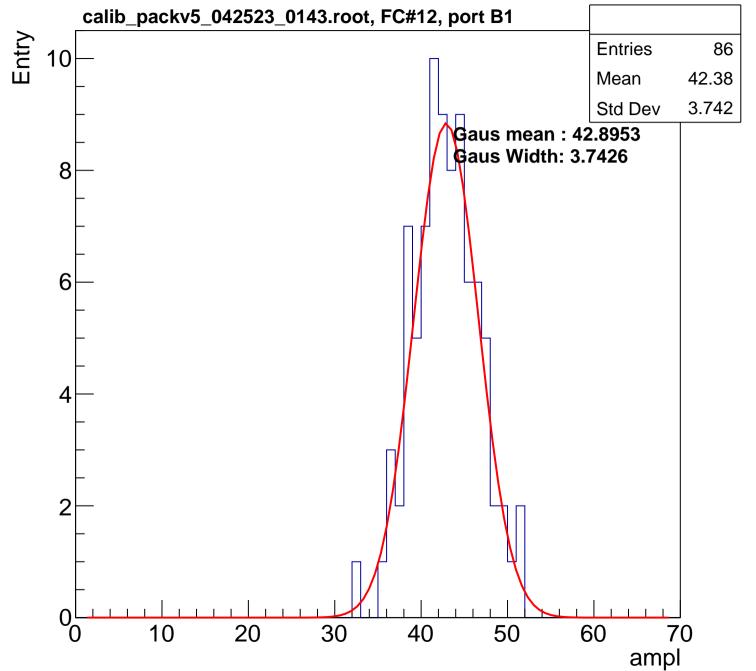


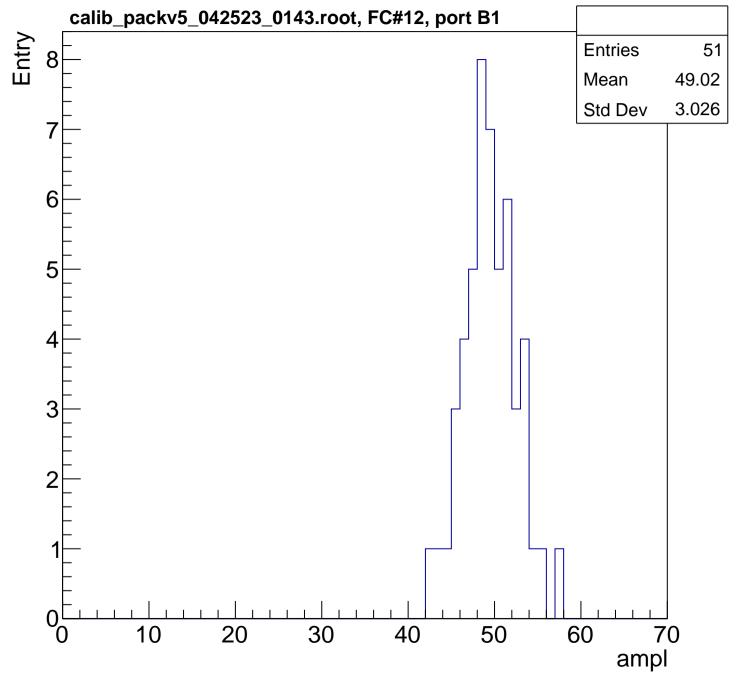


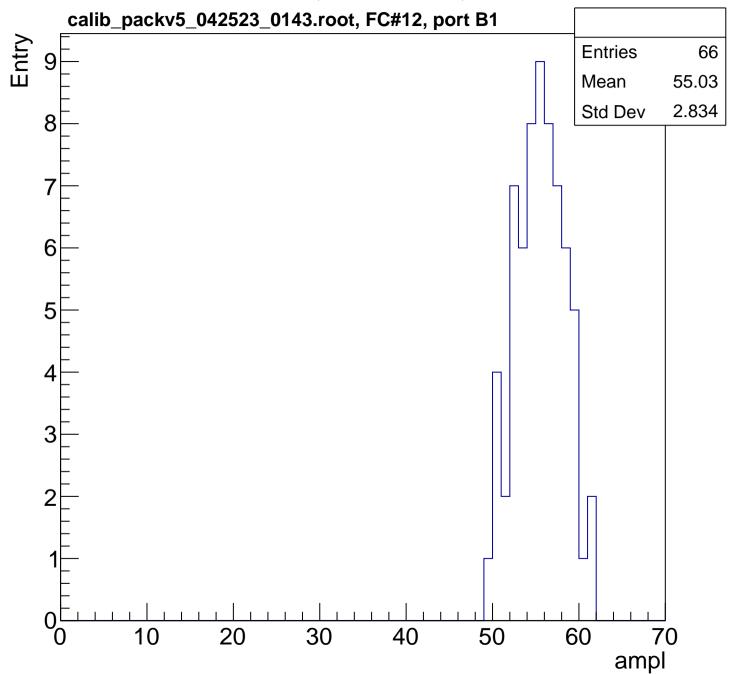


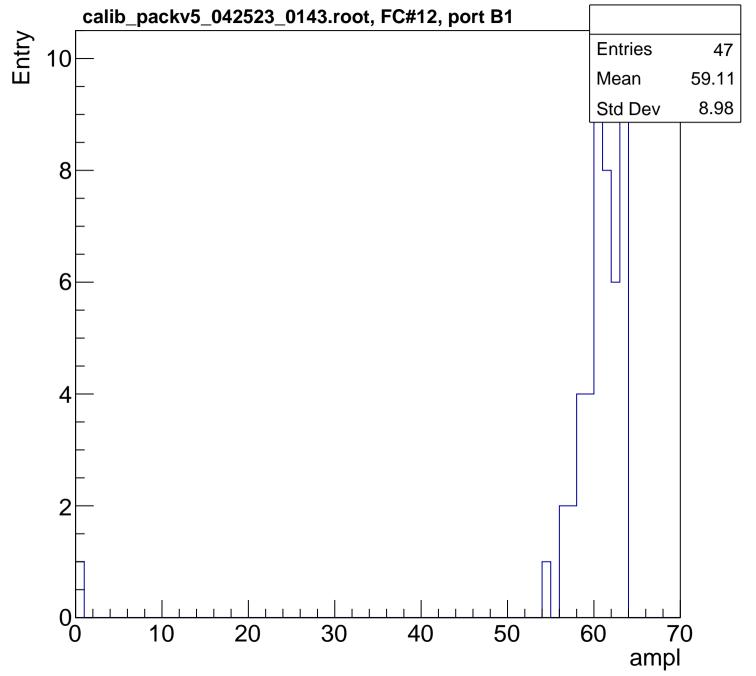


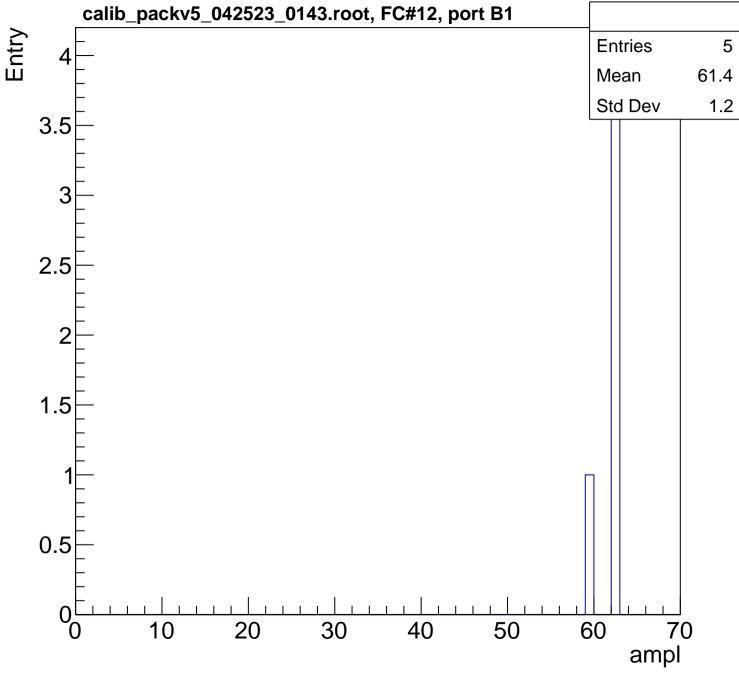


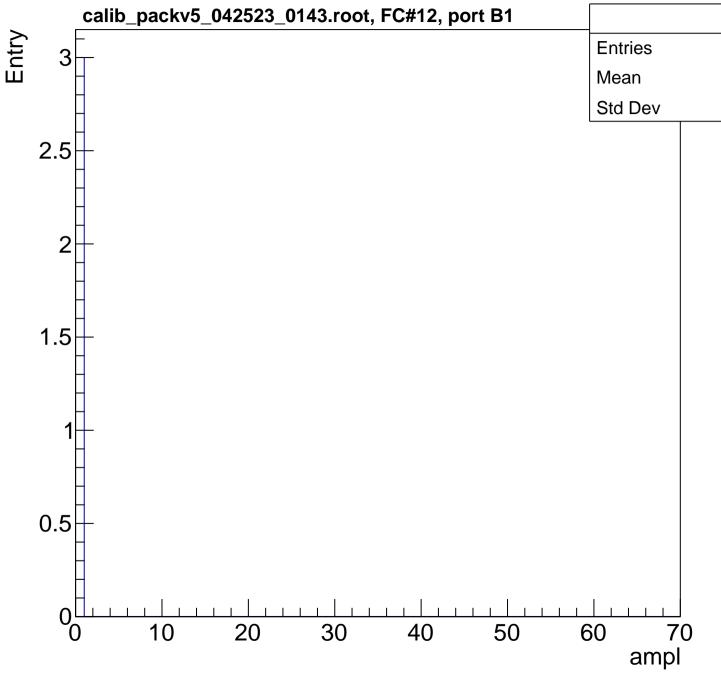


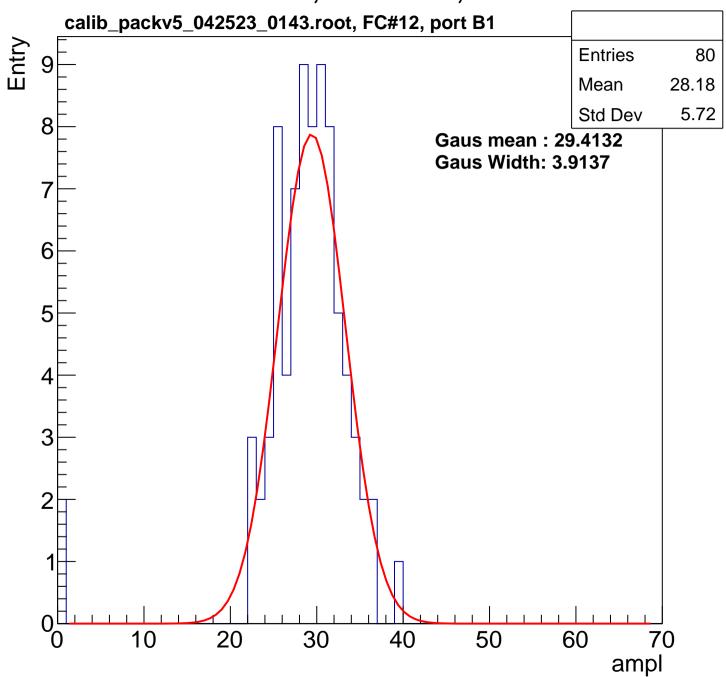


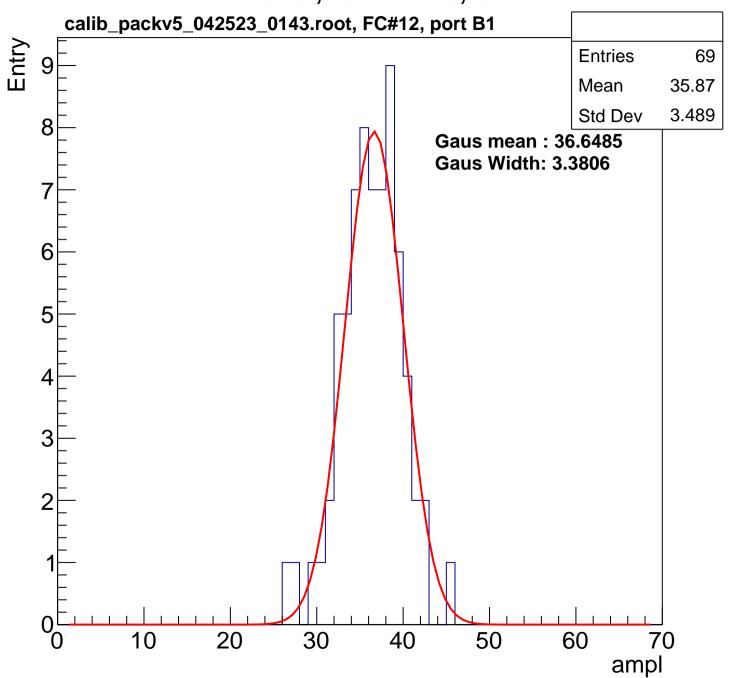


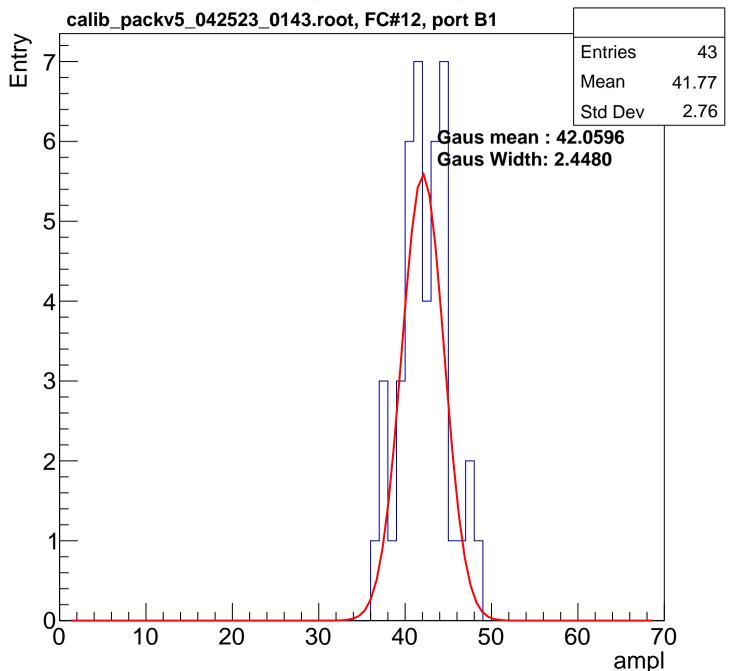


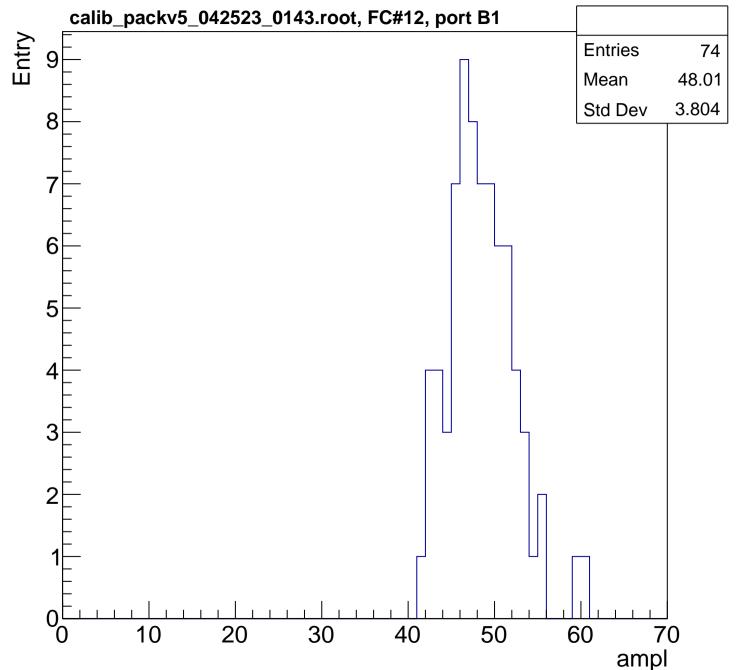


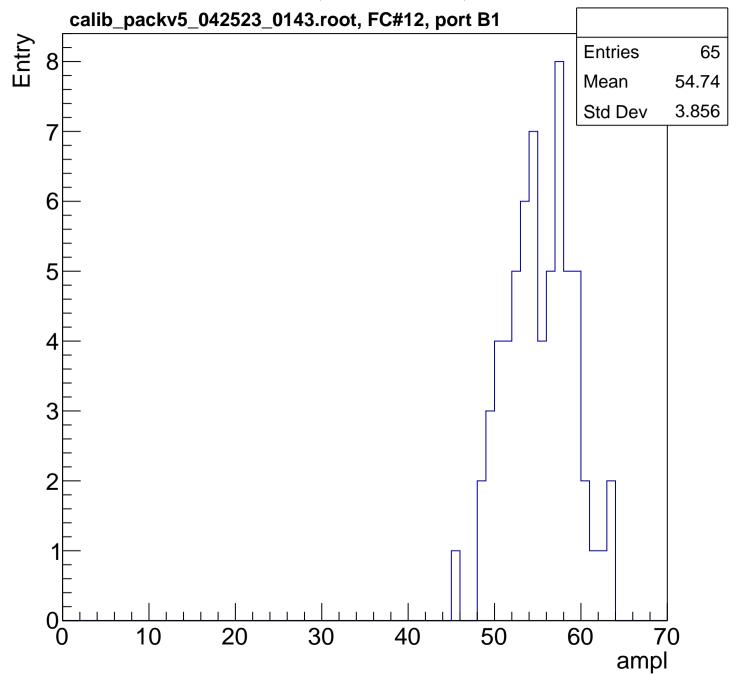


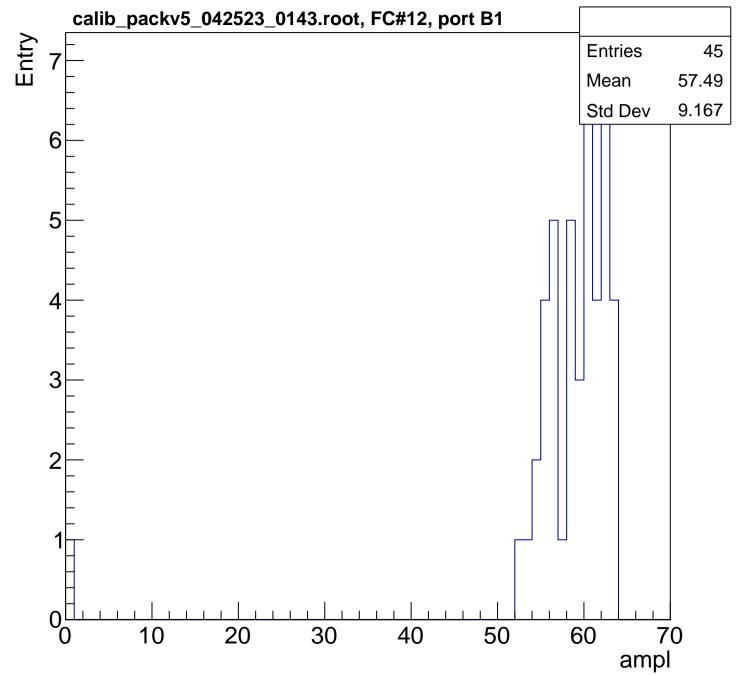


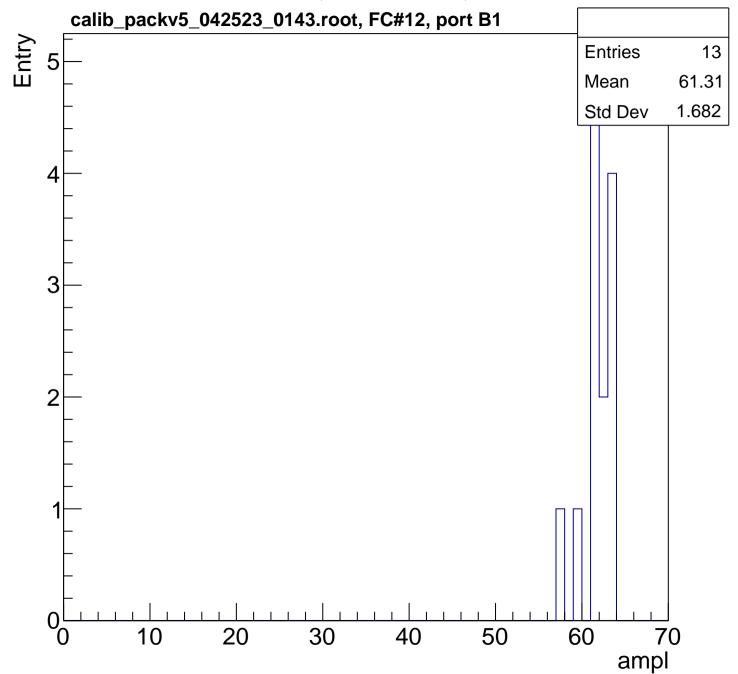




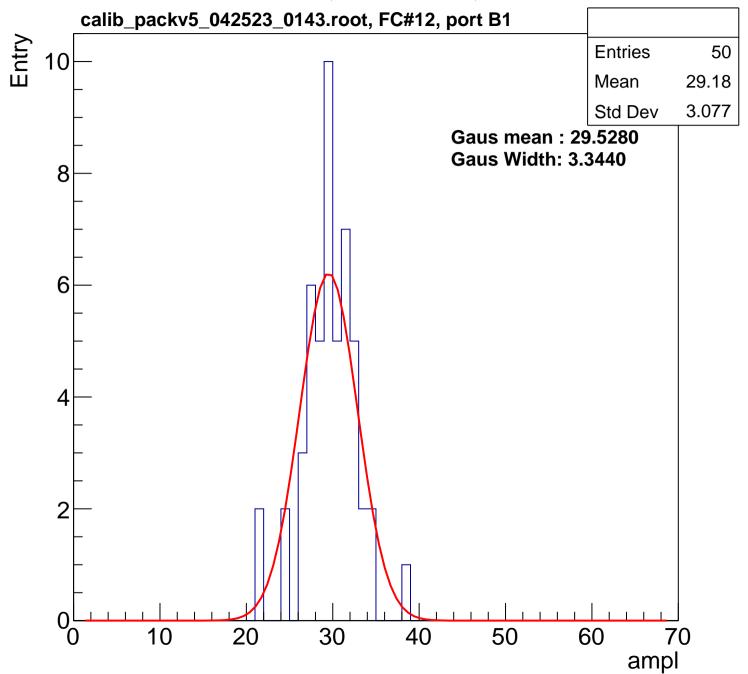


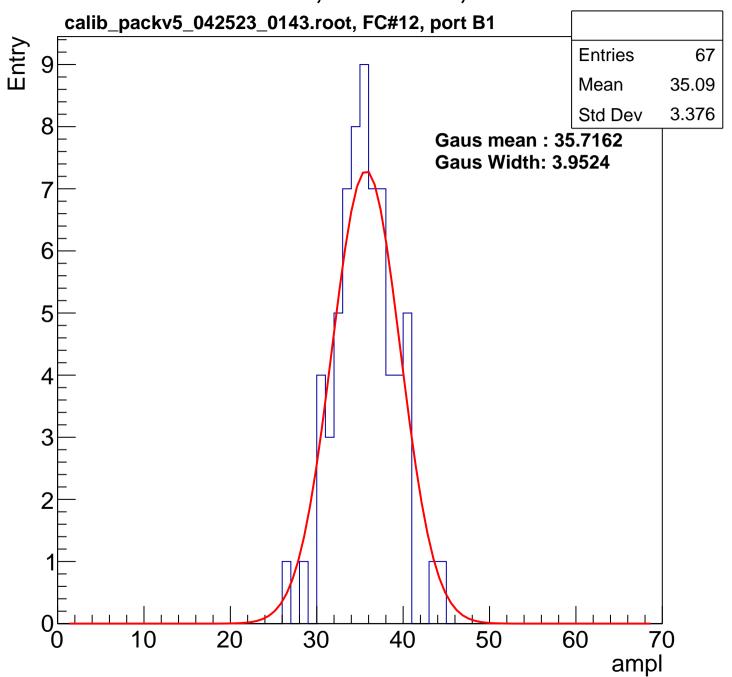


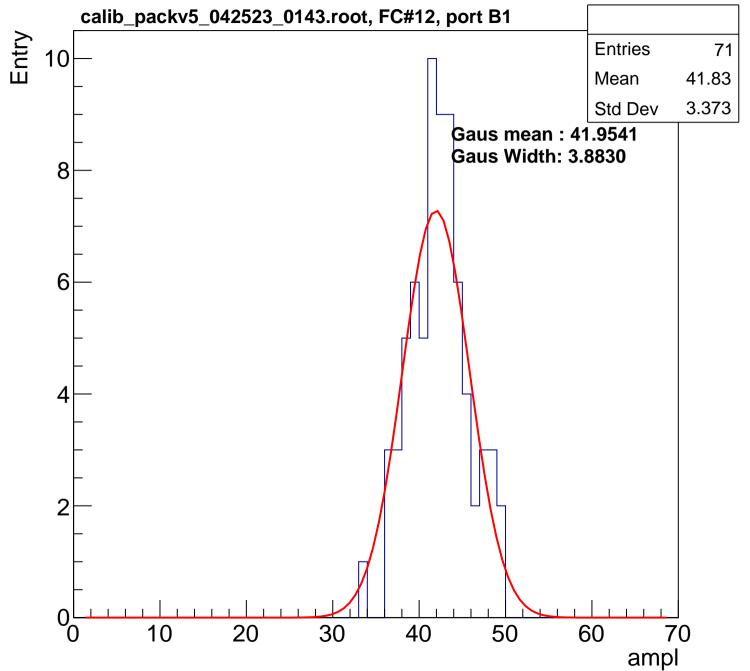


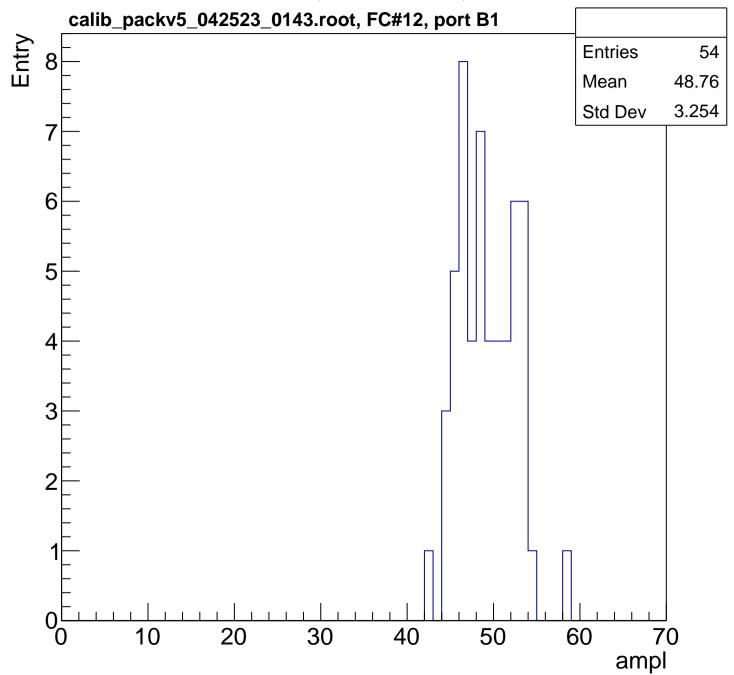


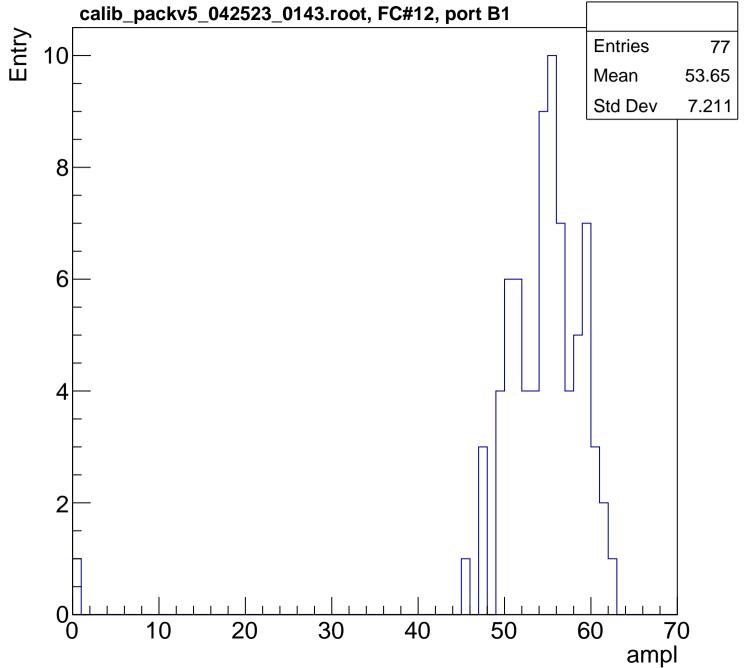
B0L102S, U7-ch48, adc7 calib_packv5_042523_0143.root, FC#12, port B1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

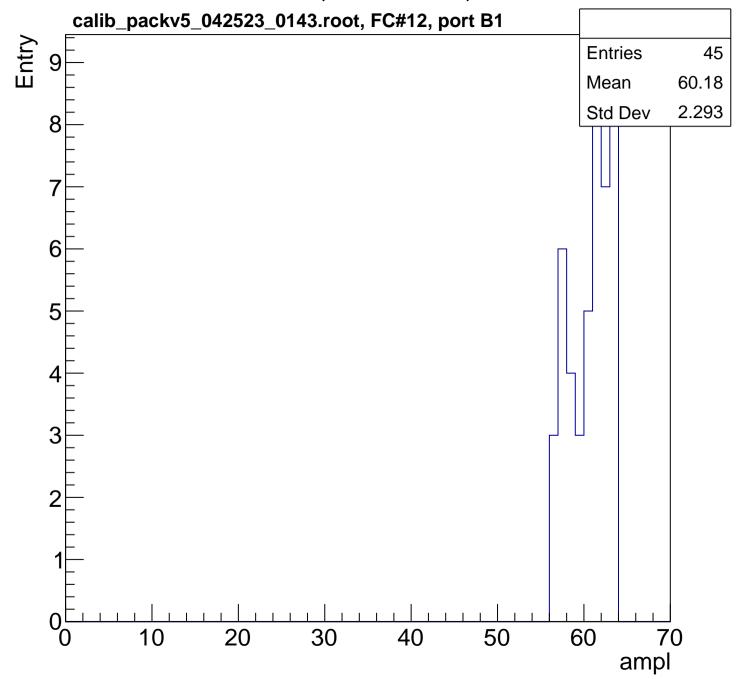


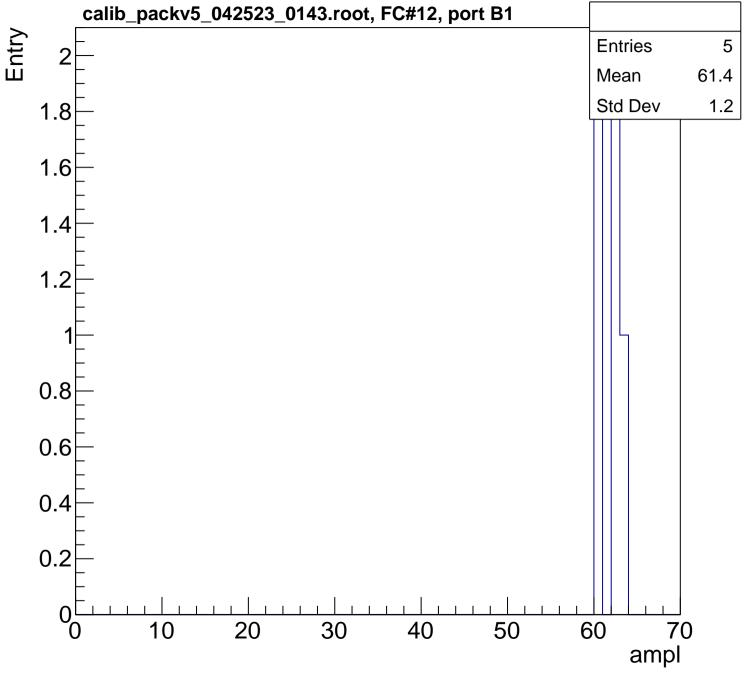


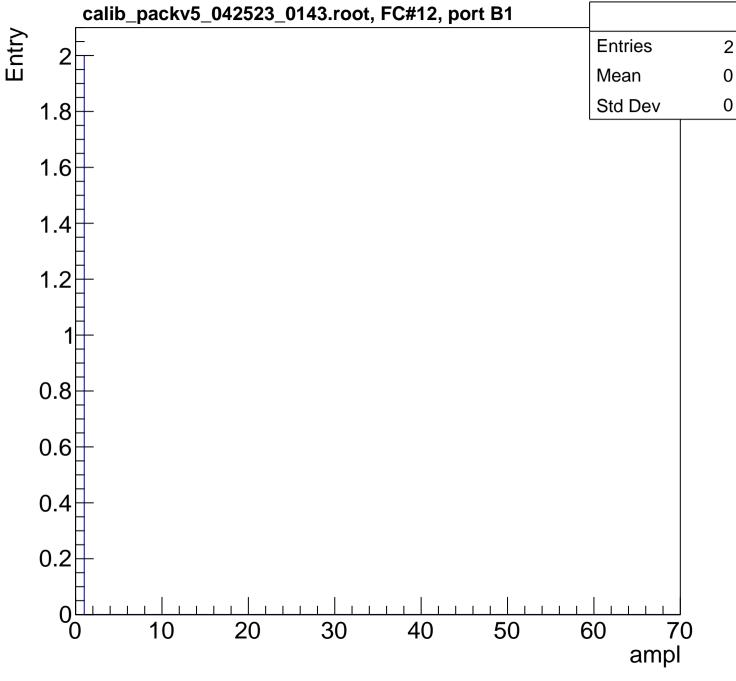


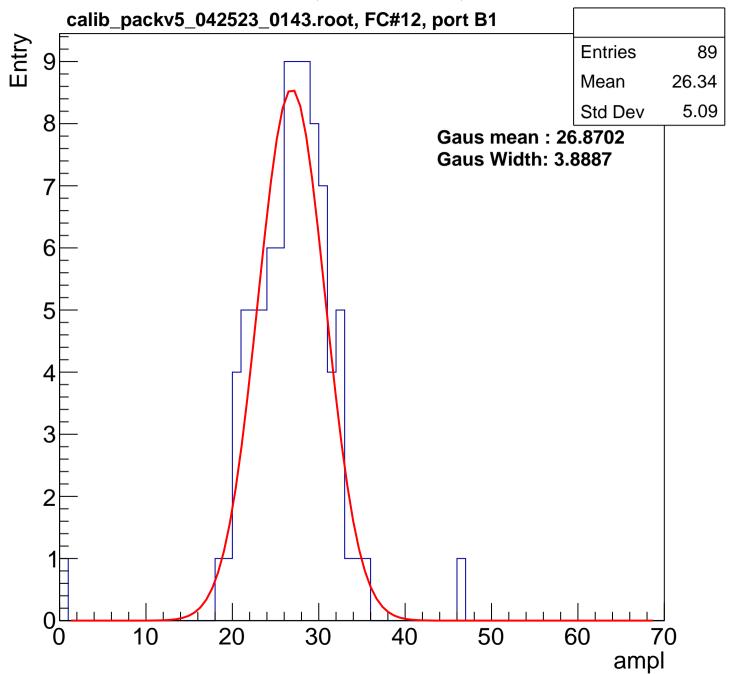


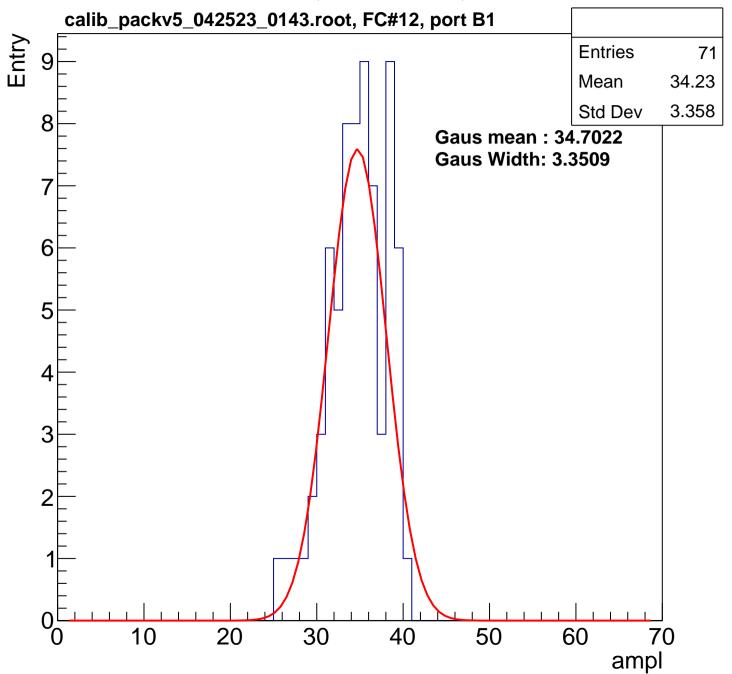


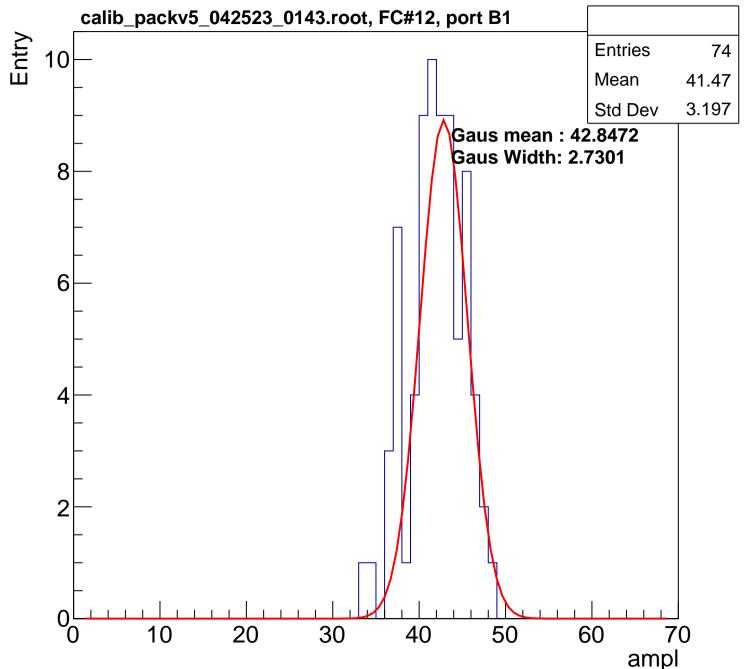


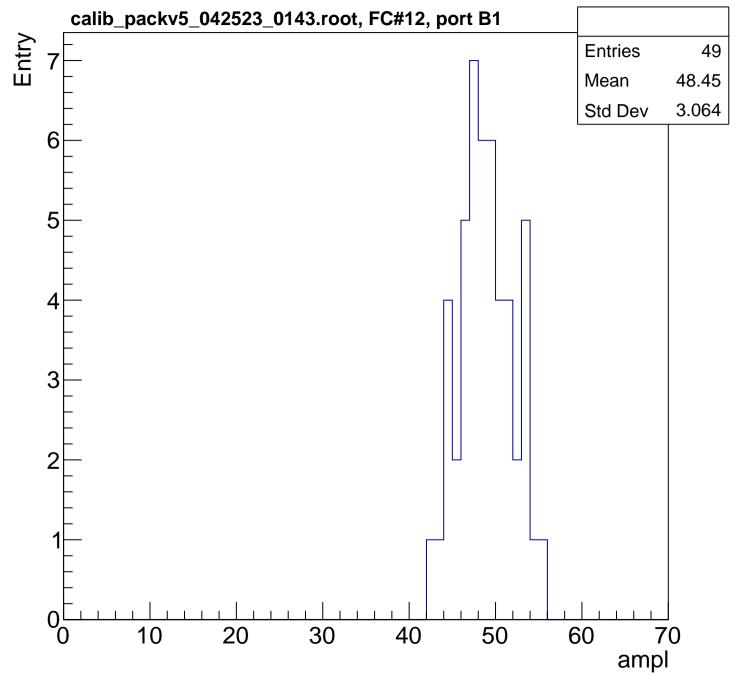


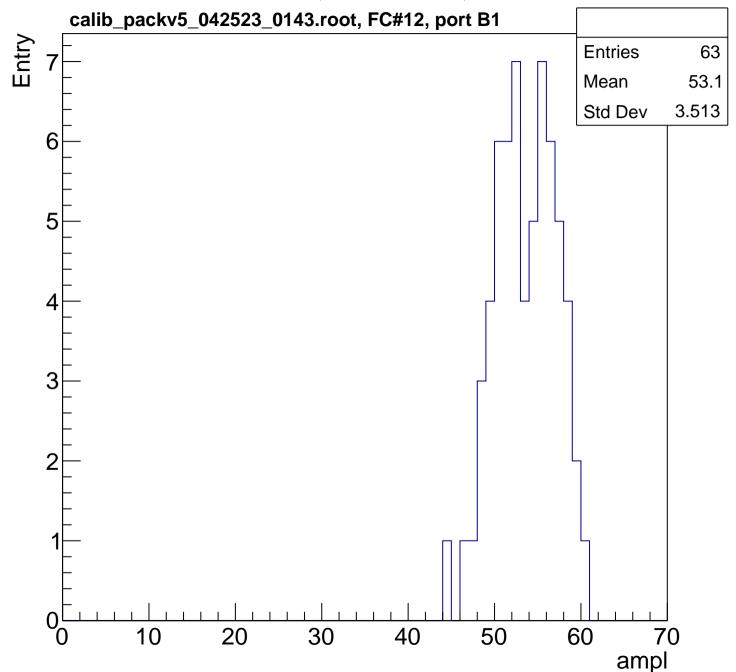


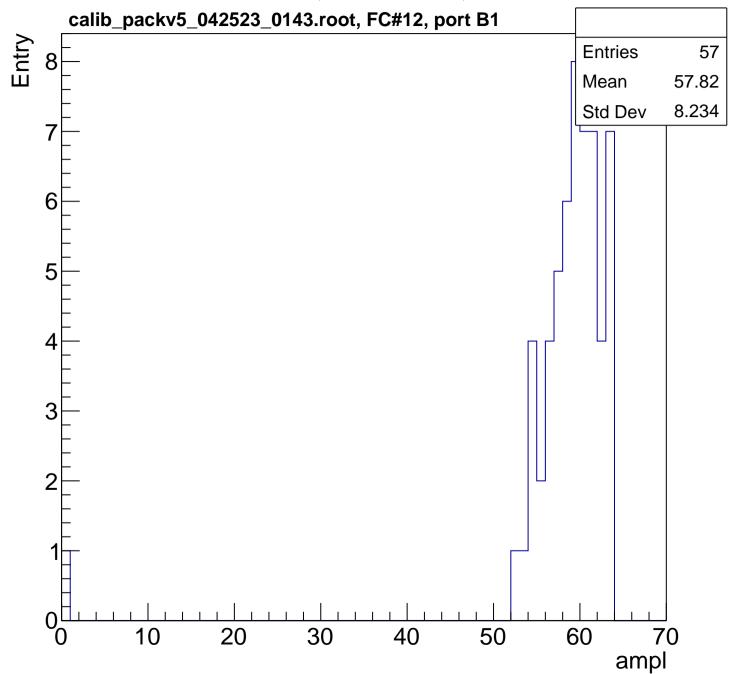


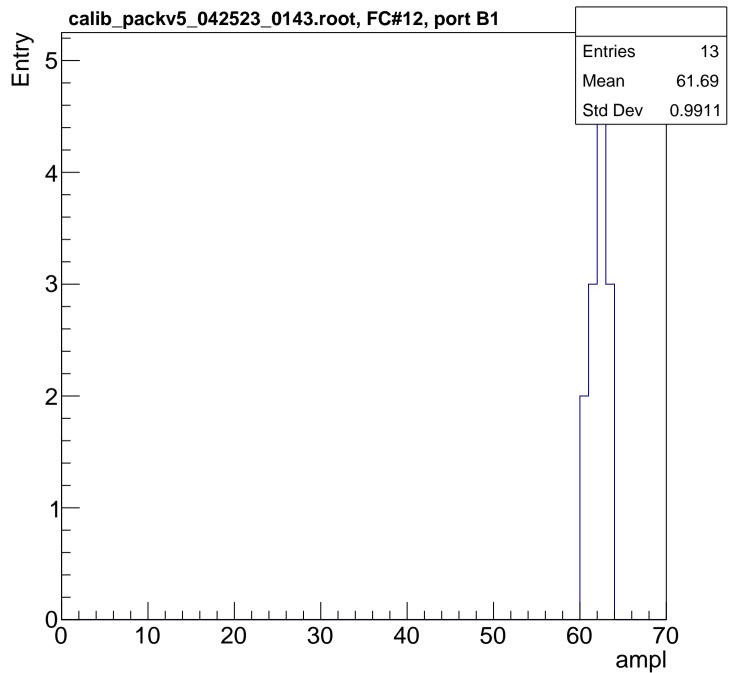


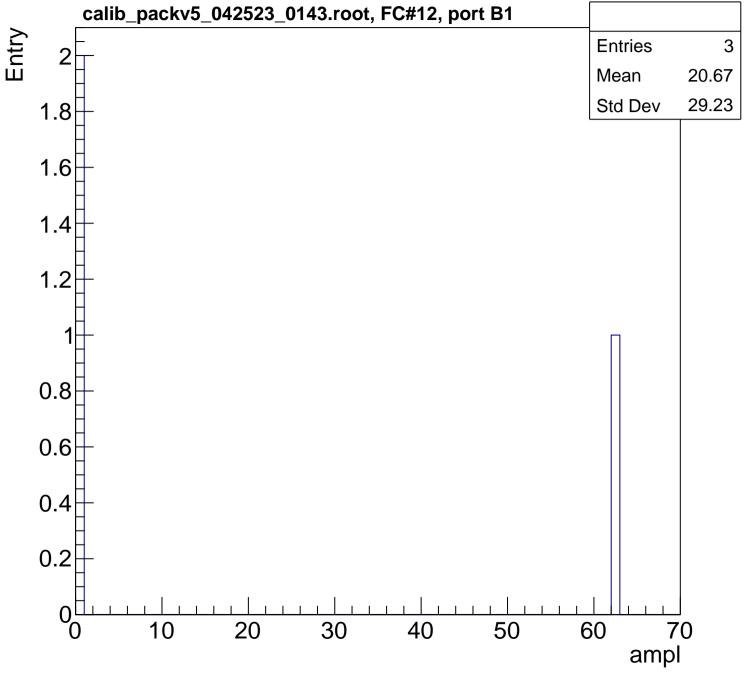


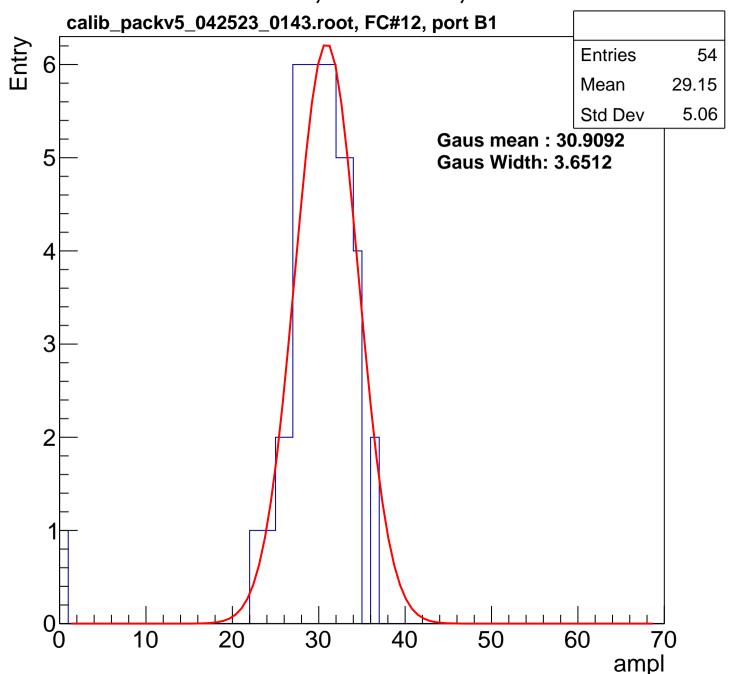


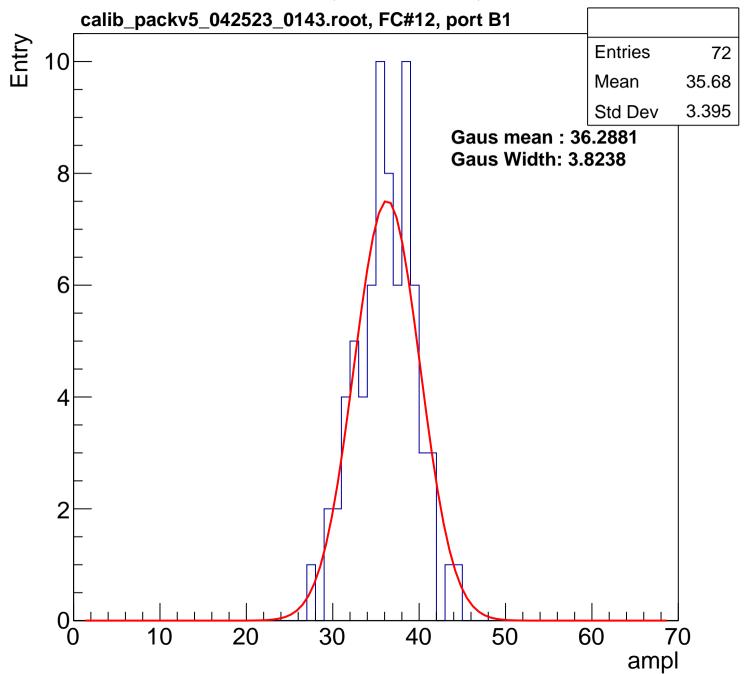


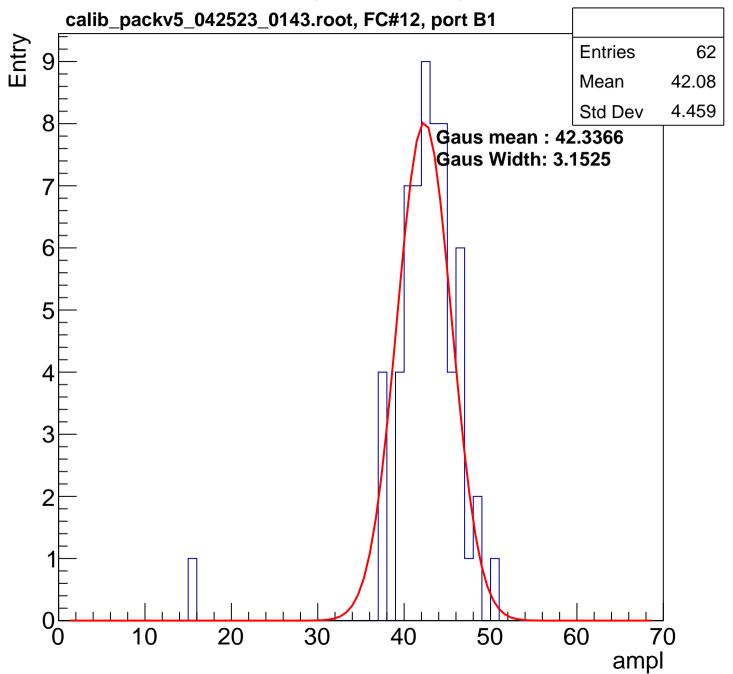


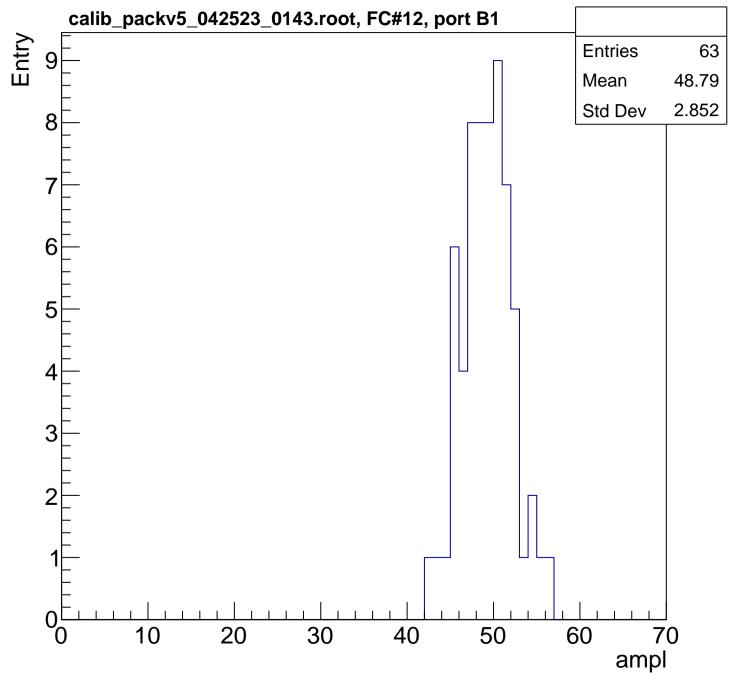


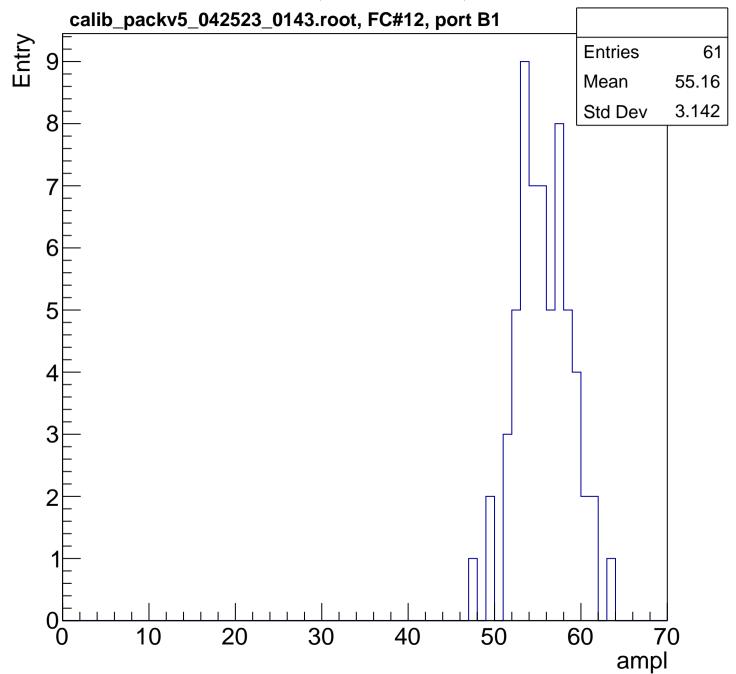


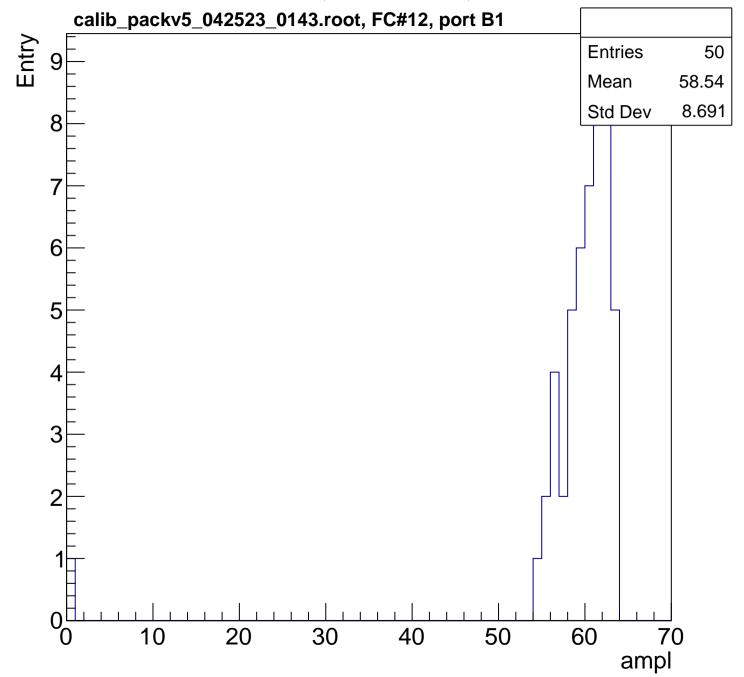


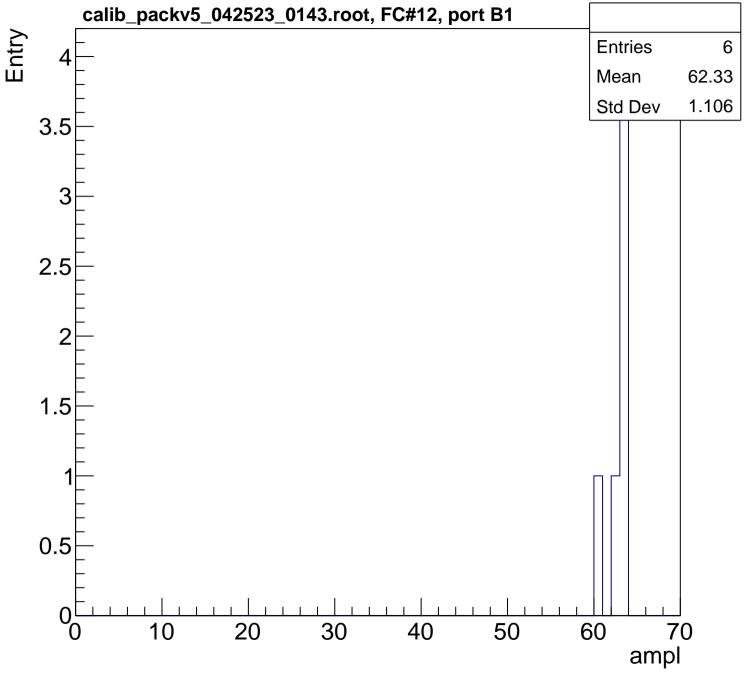


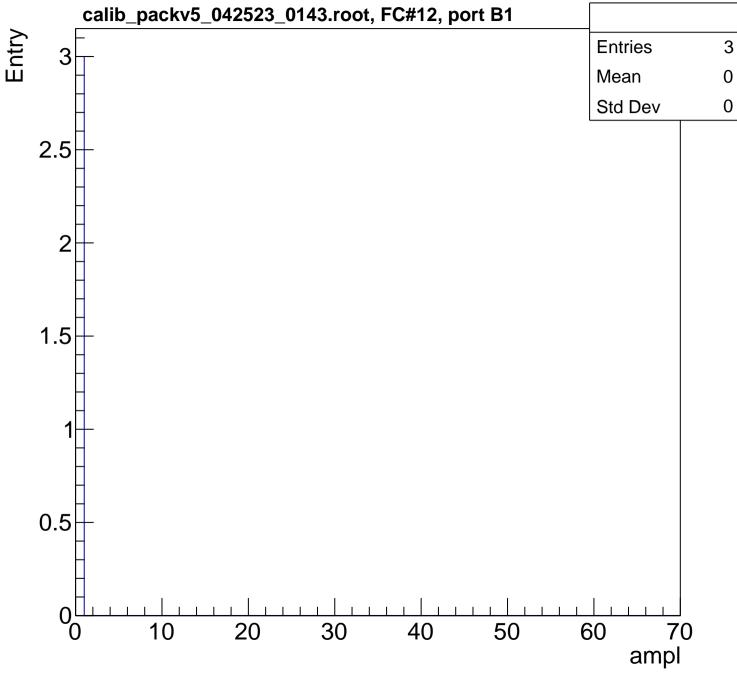


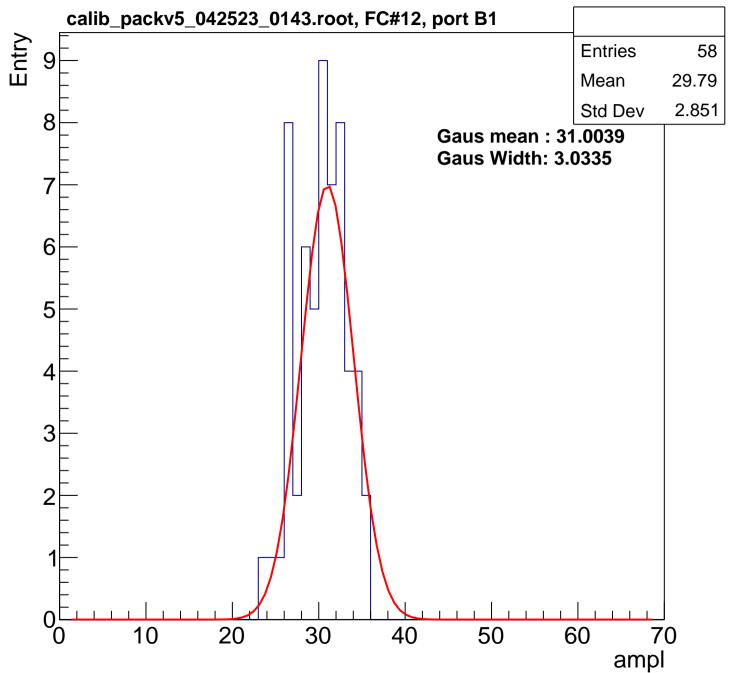


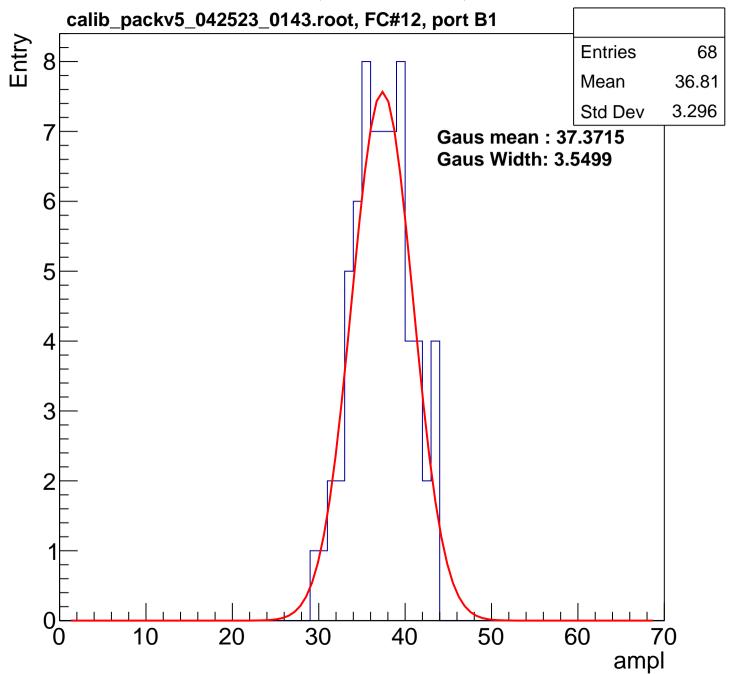


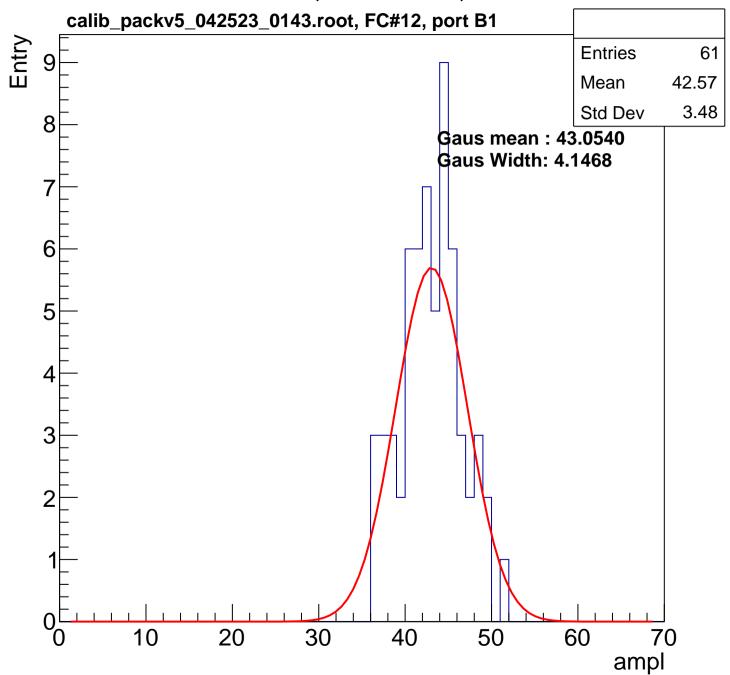


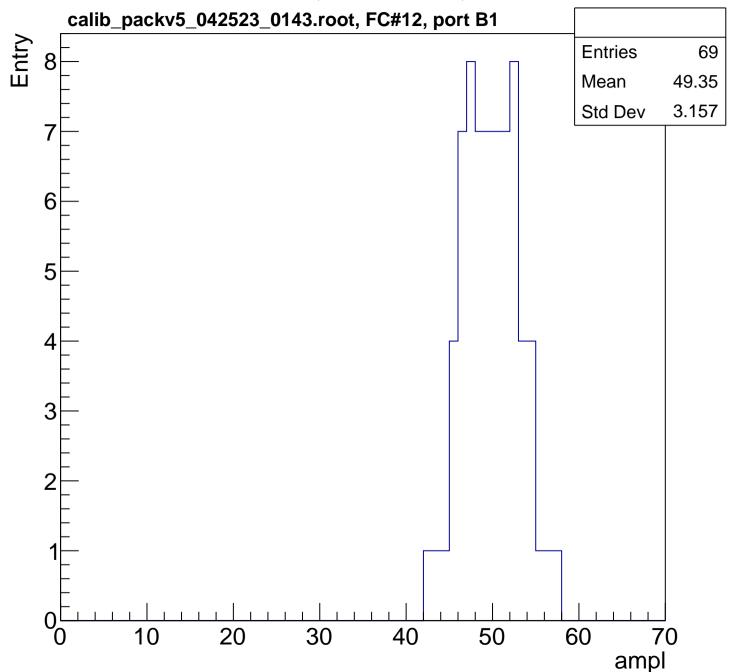


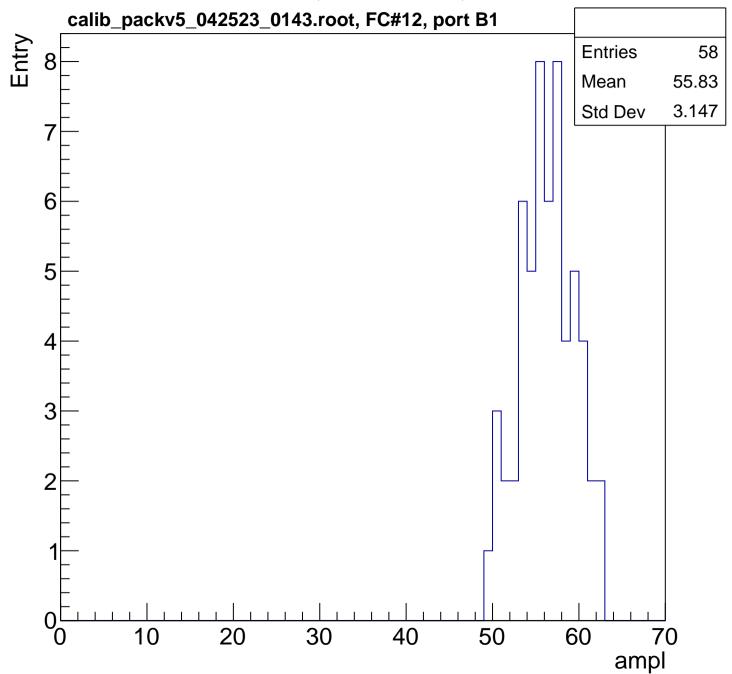


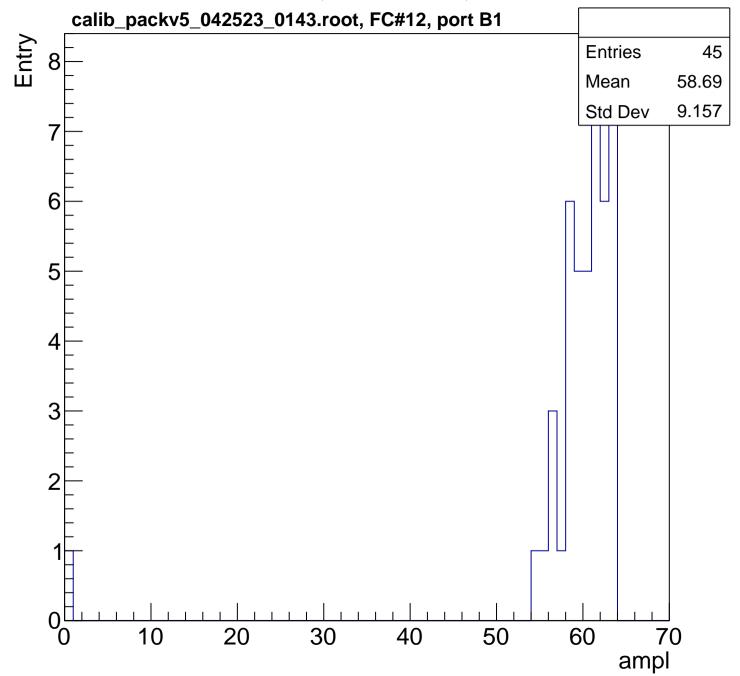


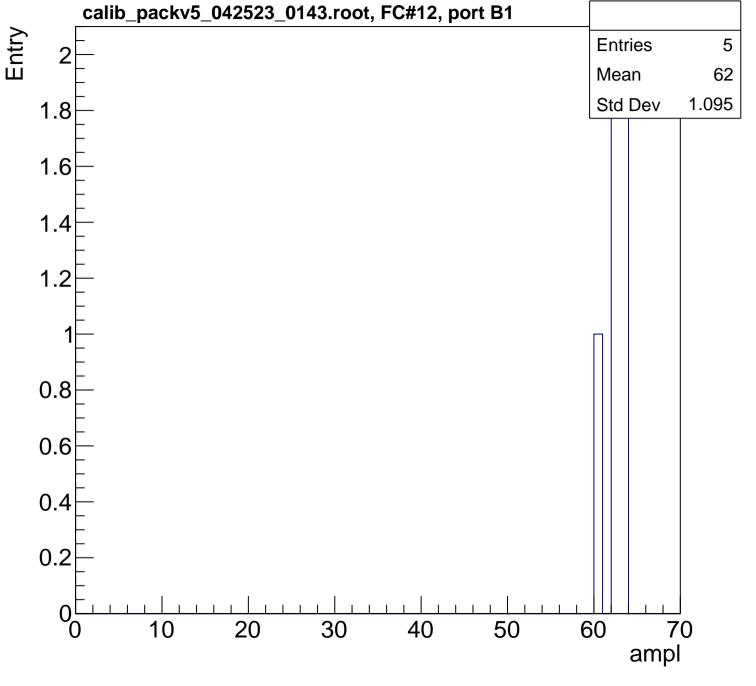






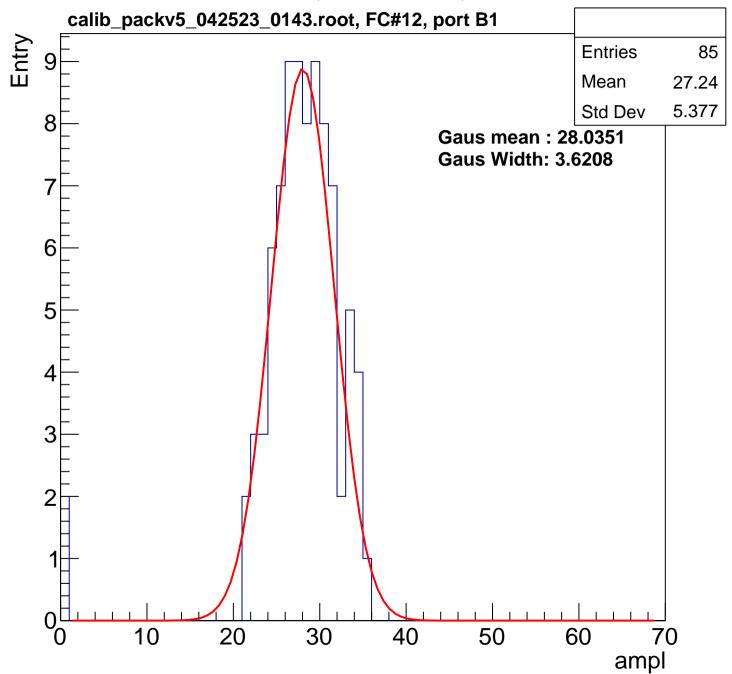


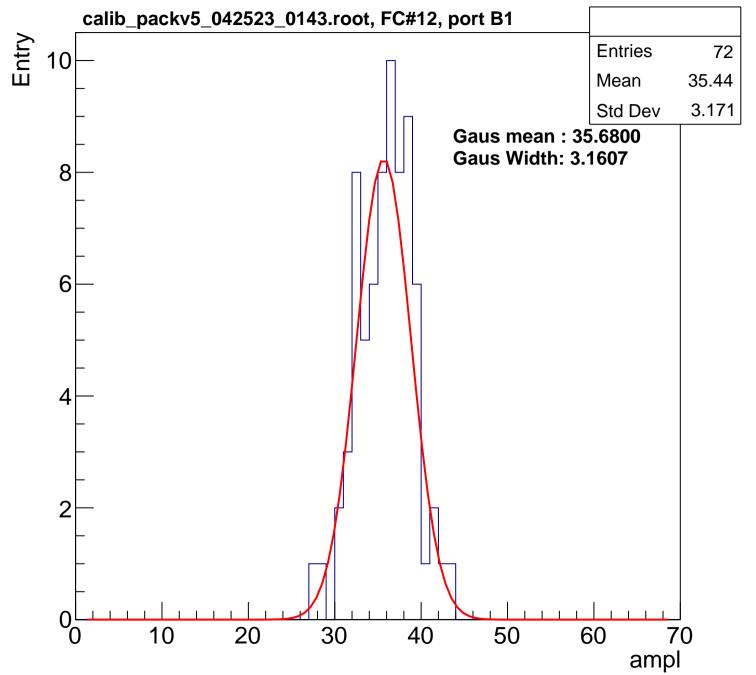


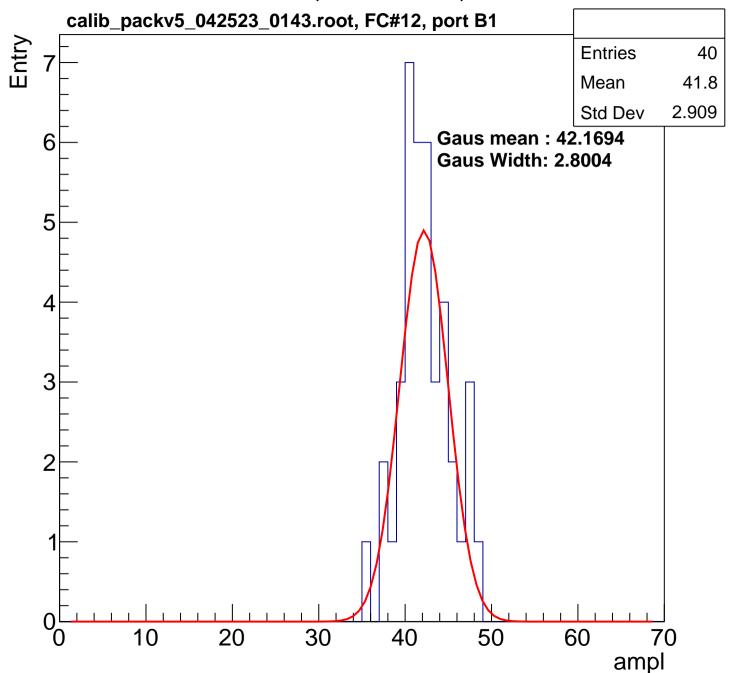


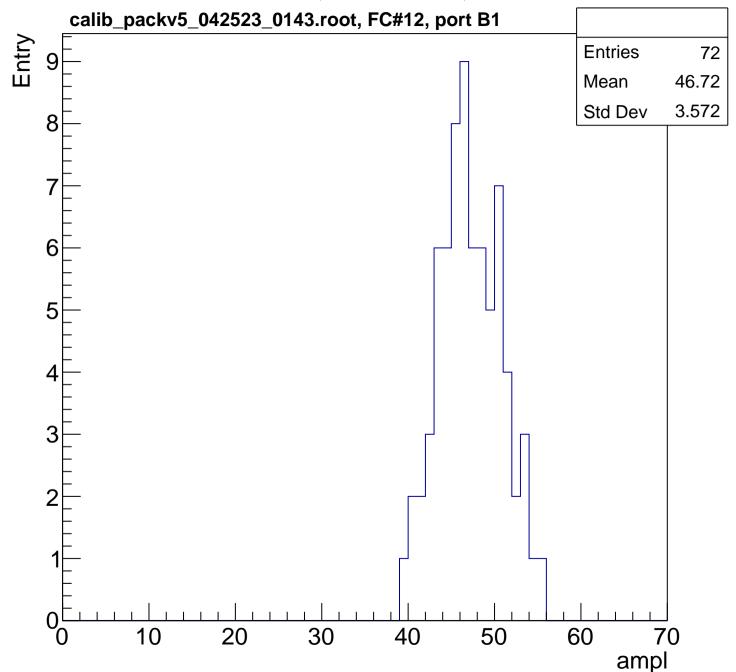
B0L102S, U7-ch52, adc7 calib_packv5_042523_0143.root, FC#12, port B1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70

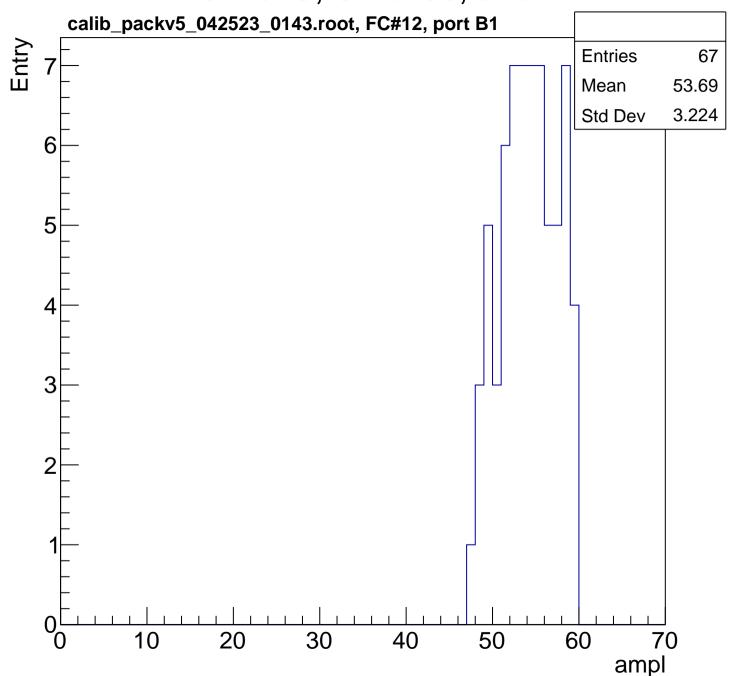
ampl

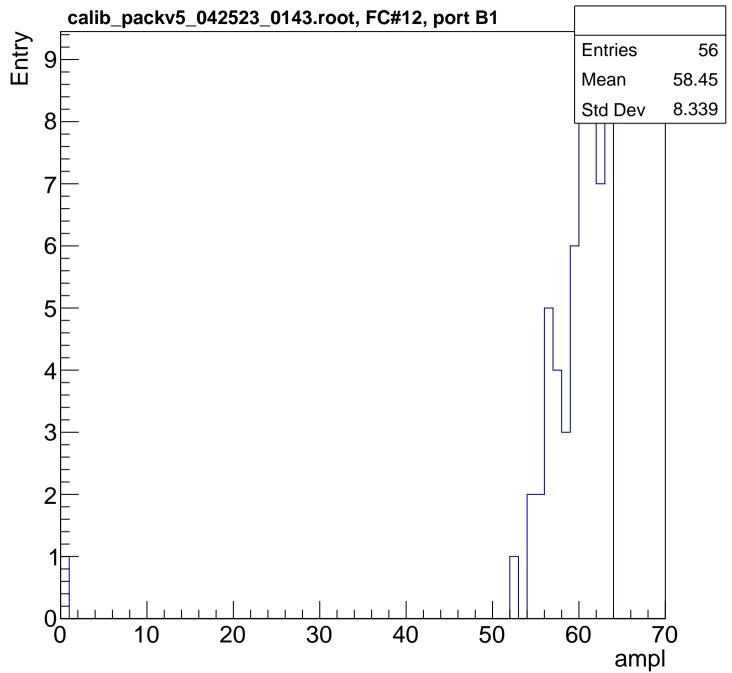


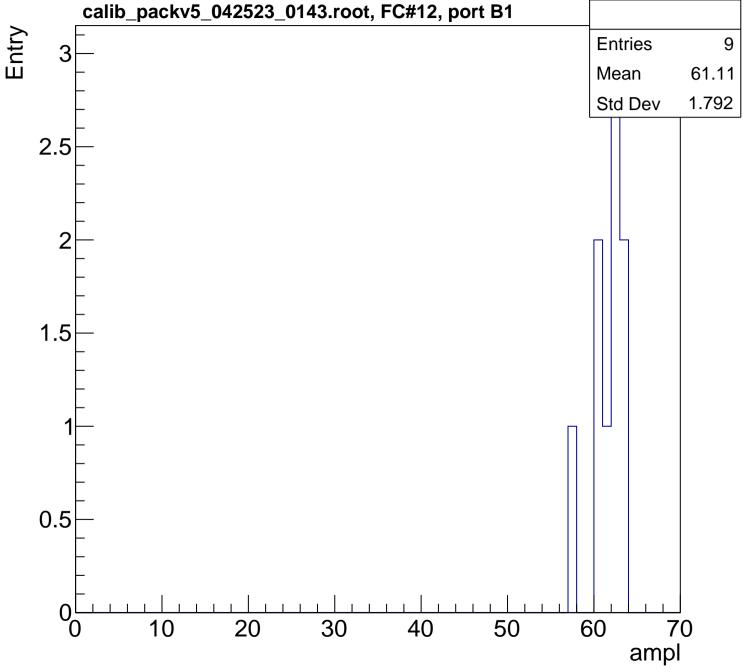


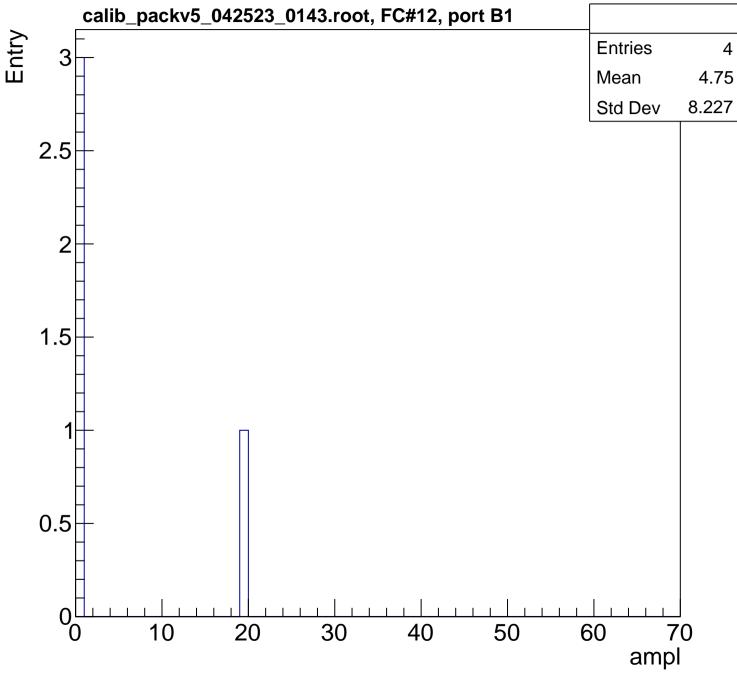


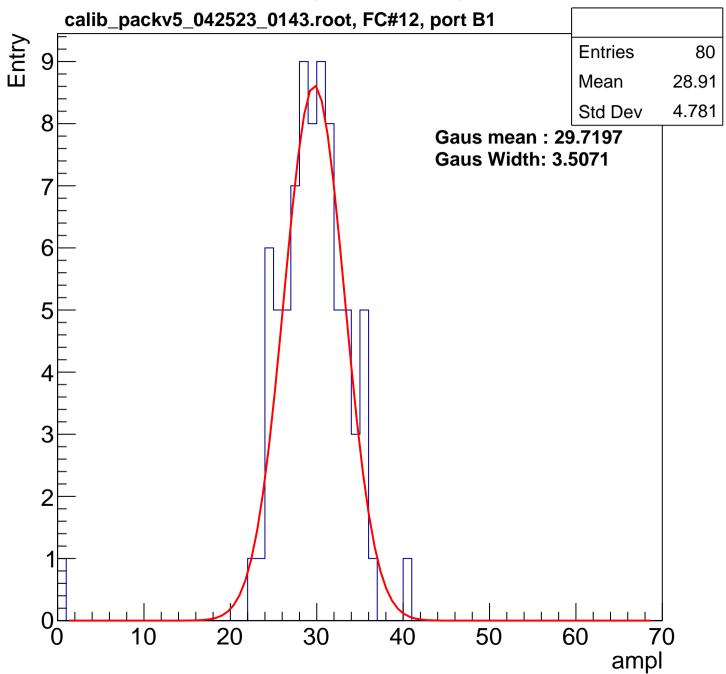


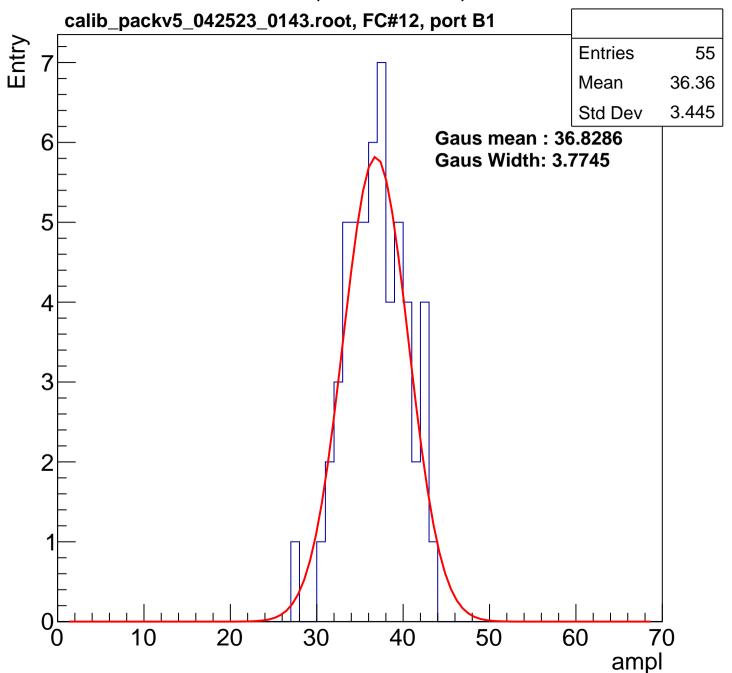


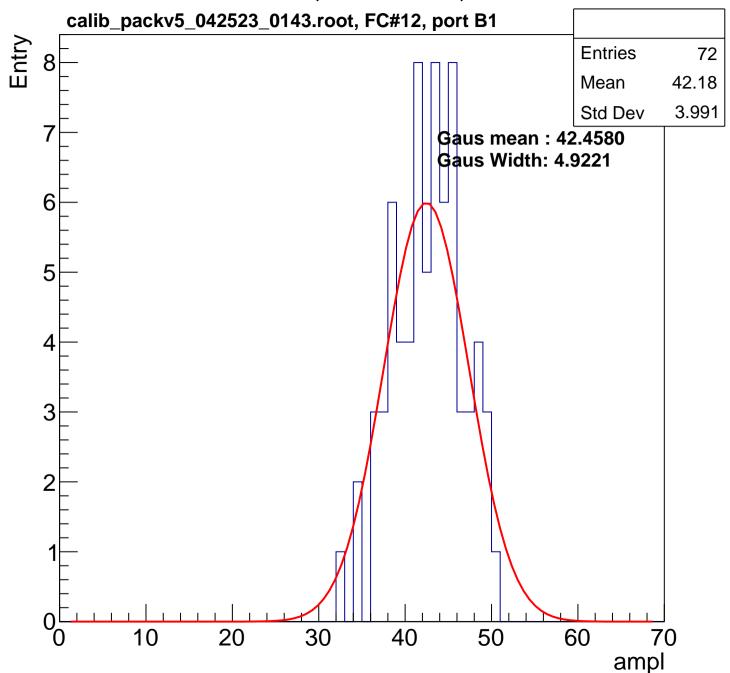


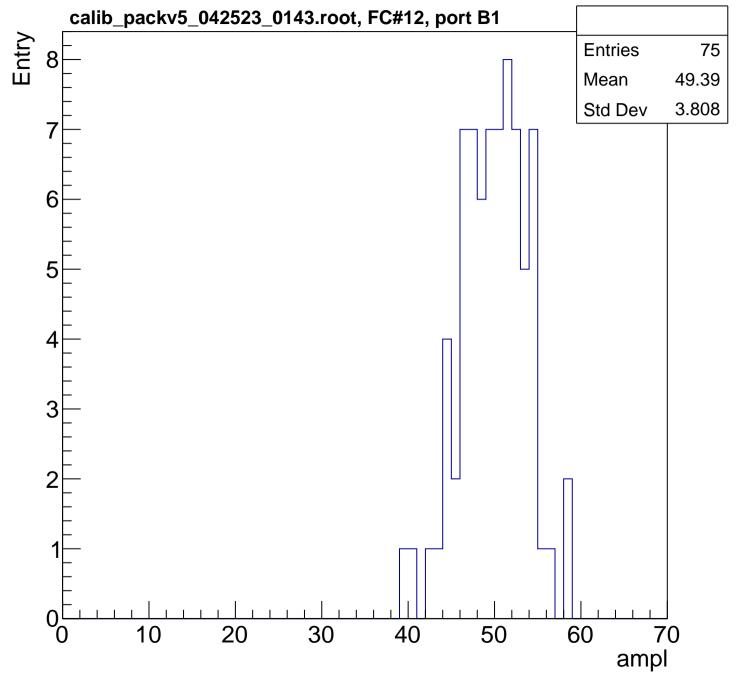


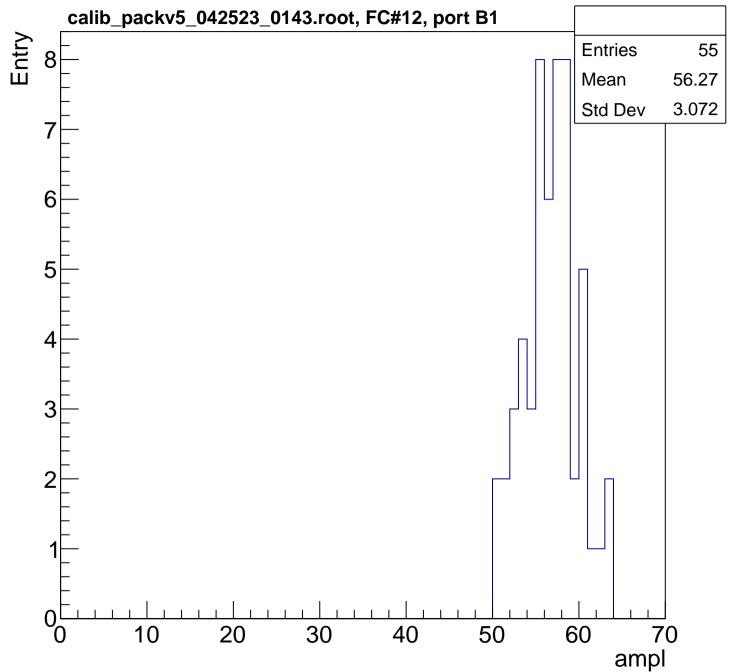


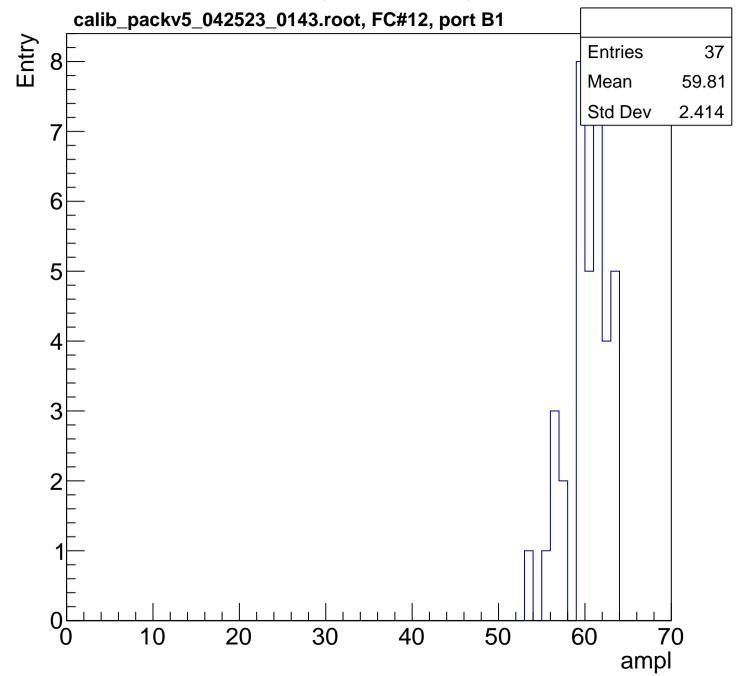


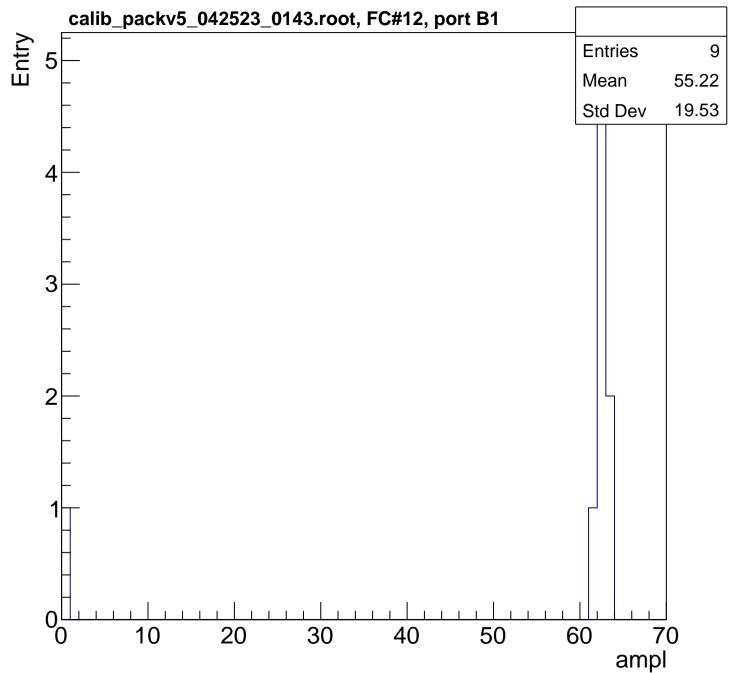




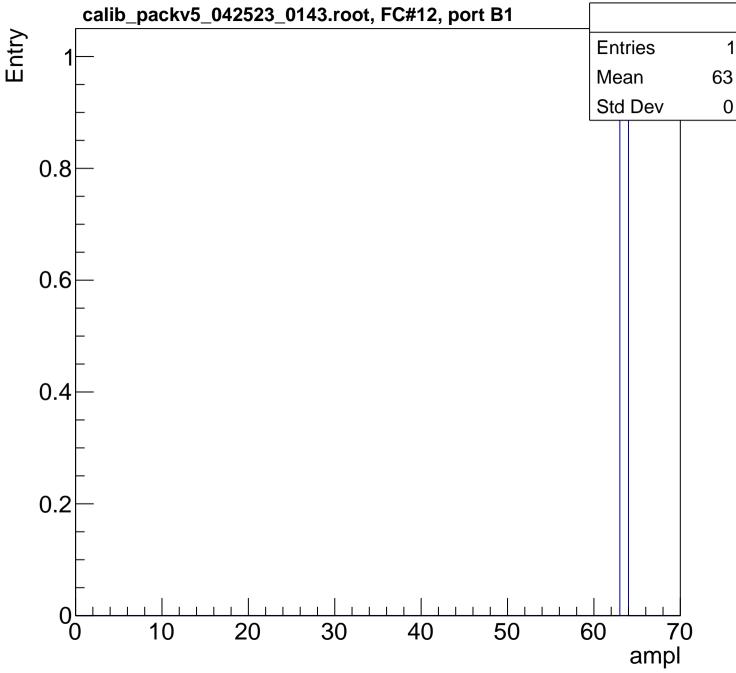


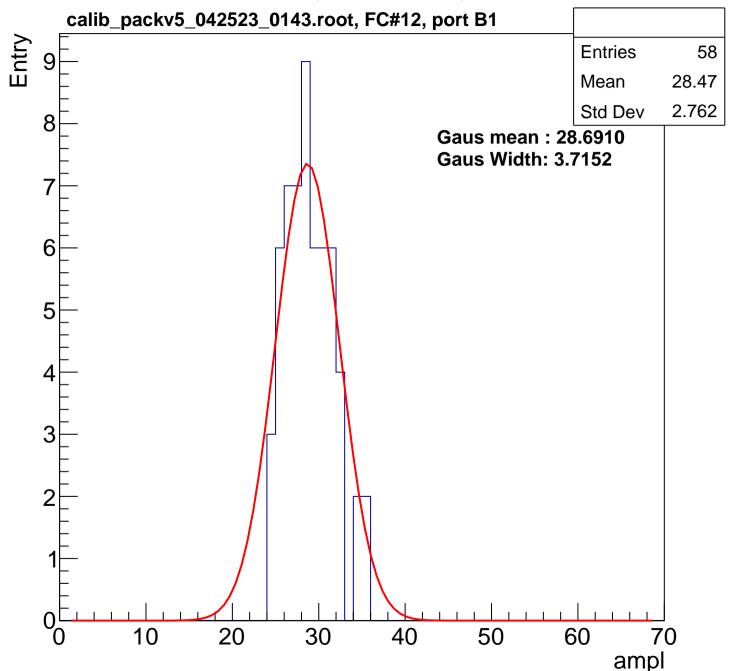


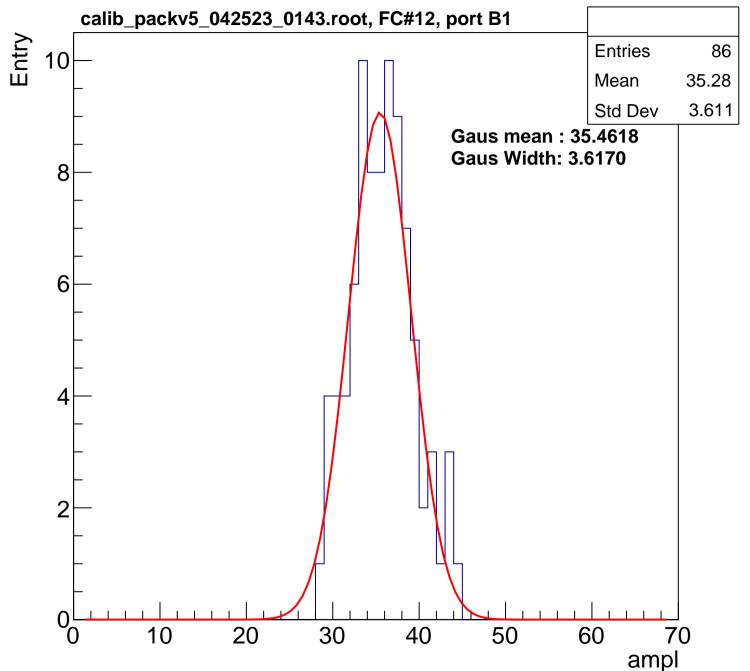


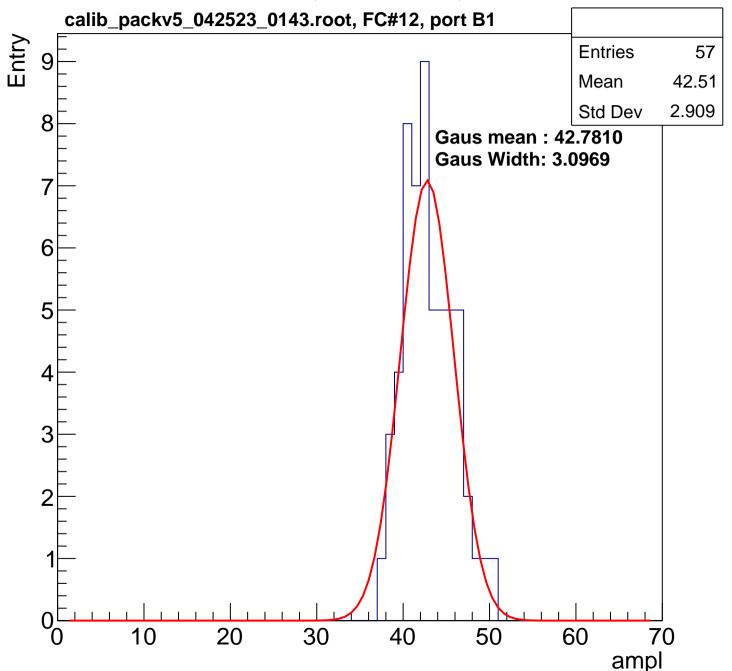


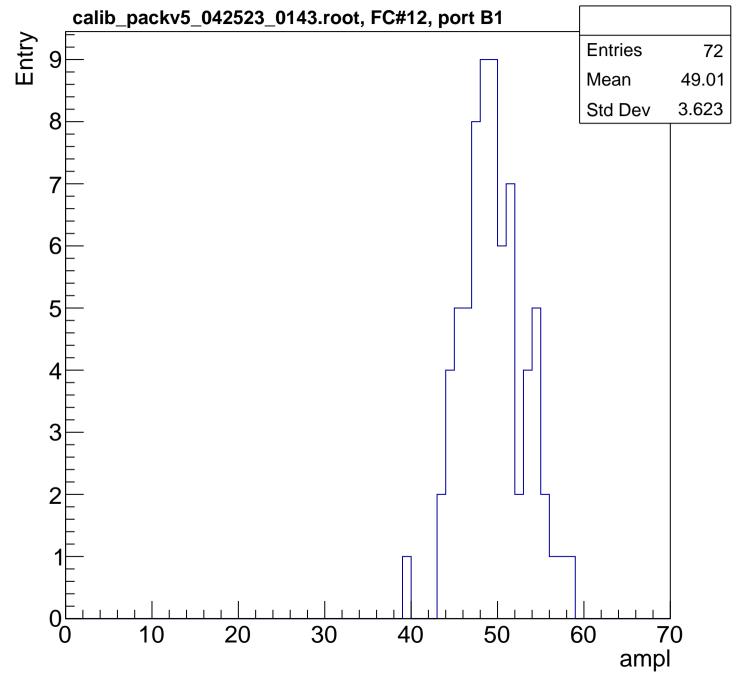
0

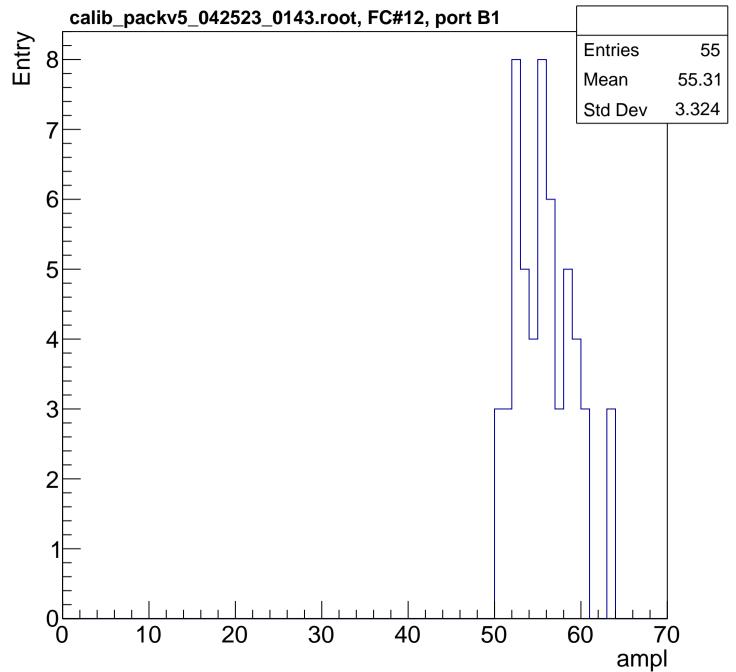


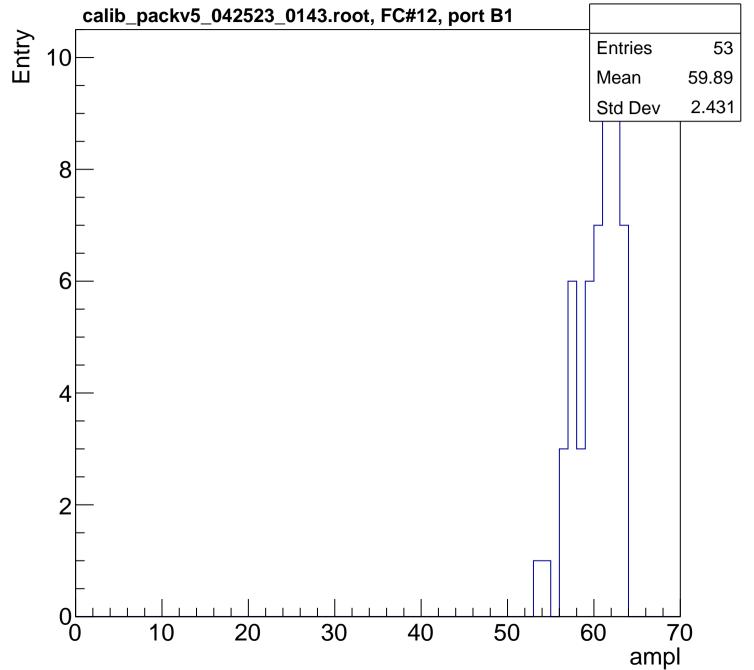


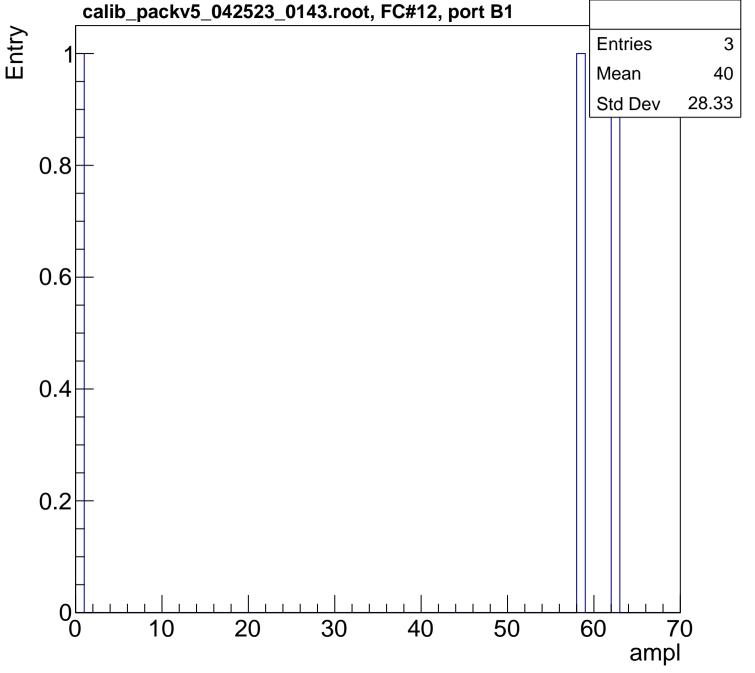






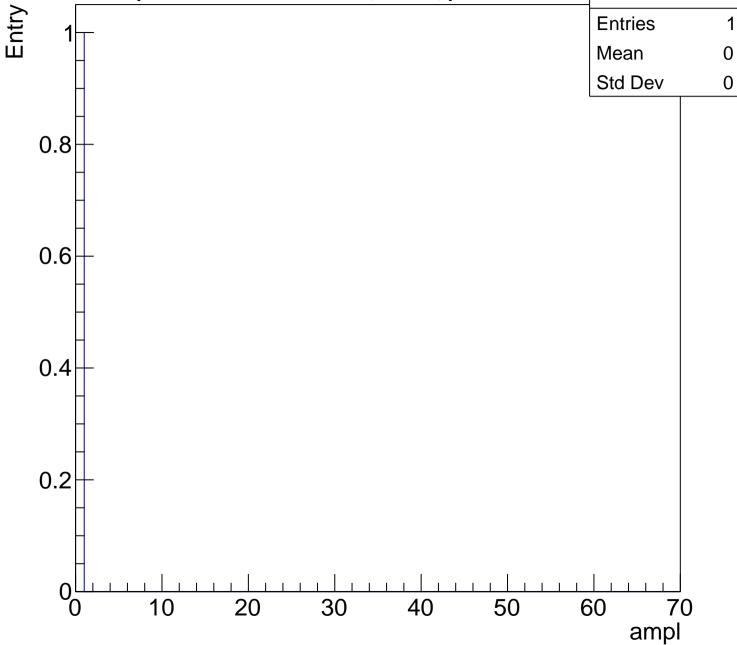


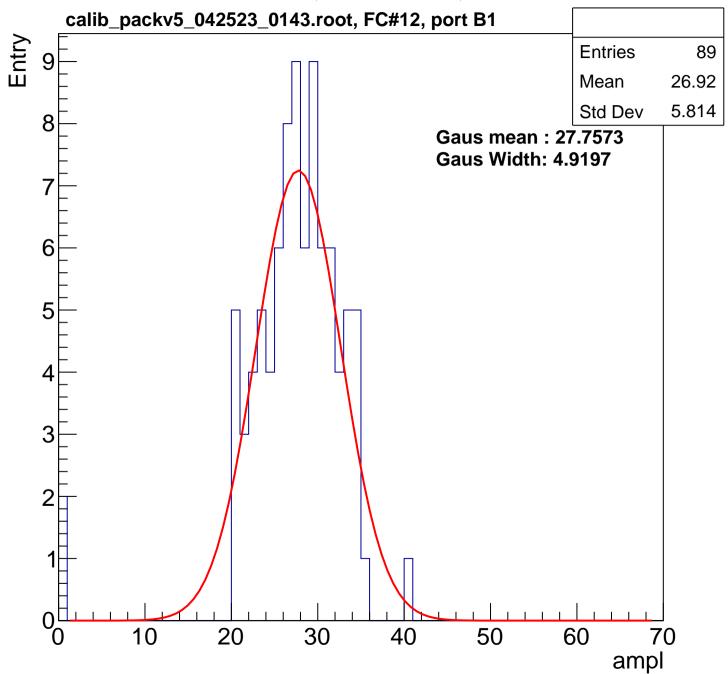


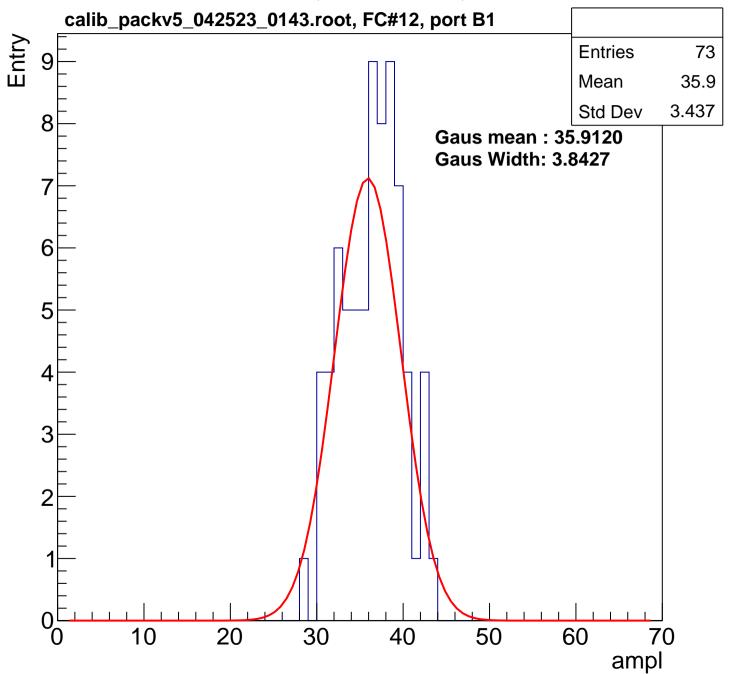


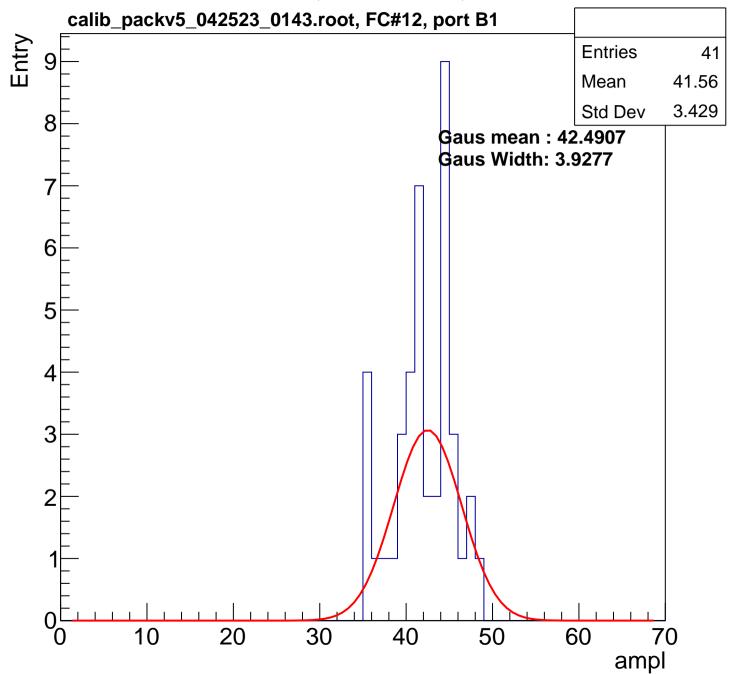
B0L102S, U7-ch55, adc7 calib_packv5_042523_0143.root, FC#12, port B1 **Entries** Mean Std Dev 8.0 0.6

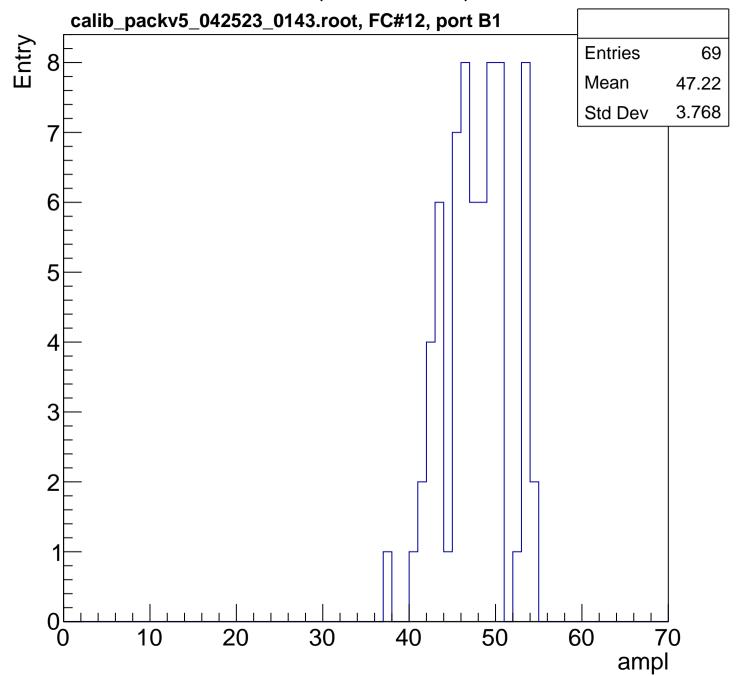
1

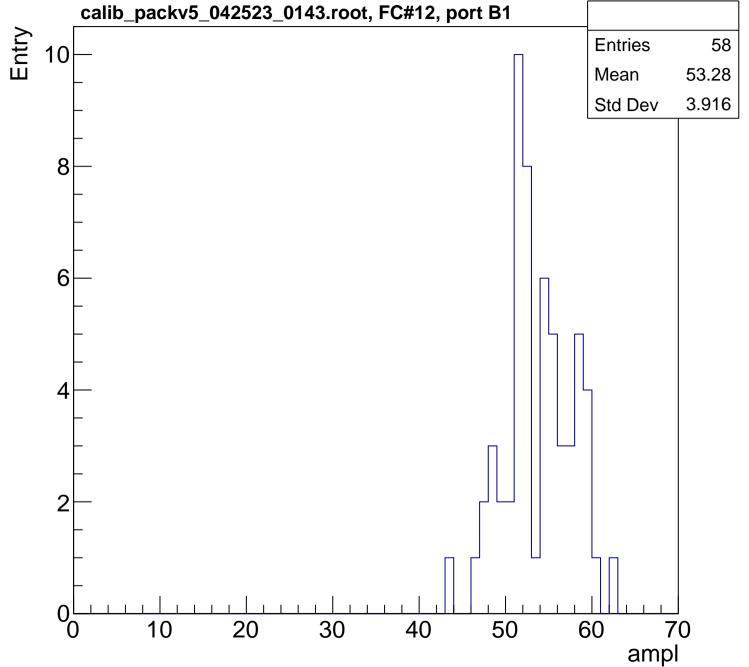


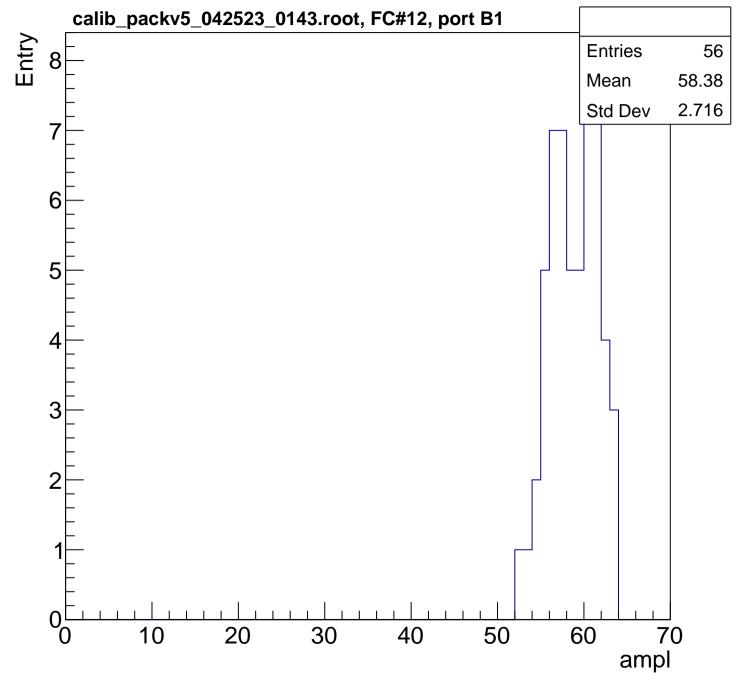


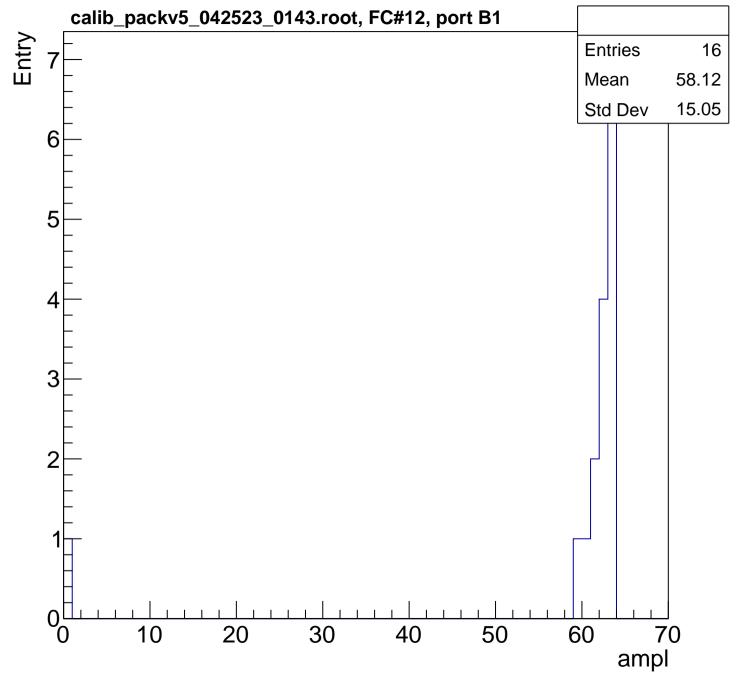


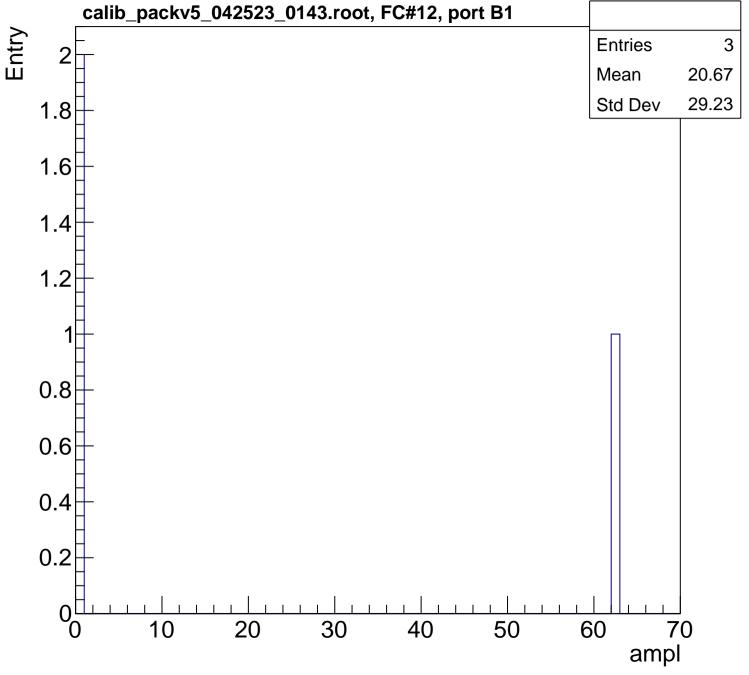


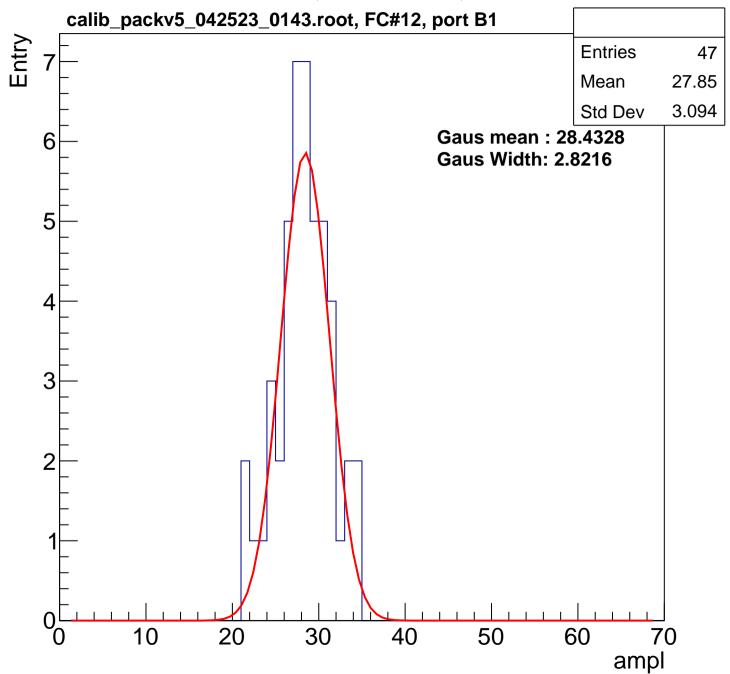


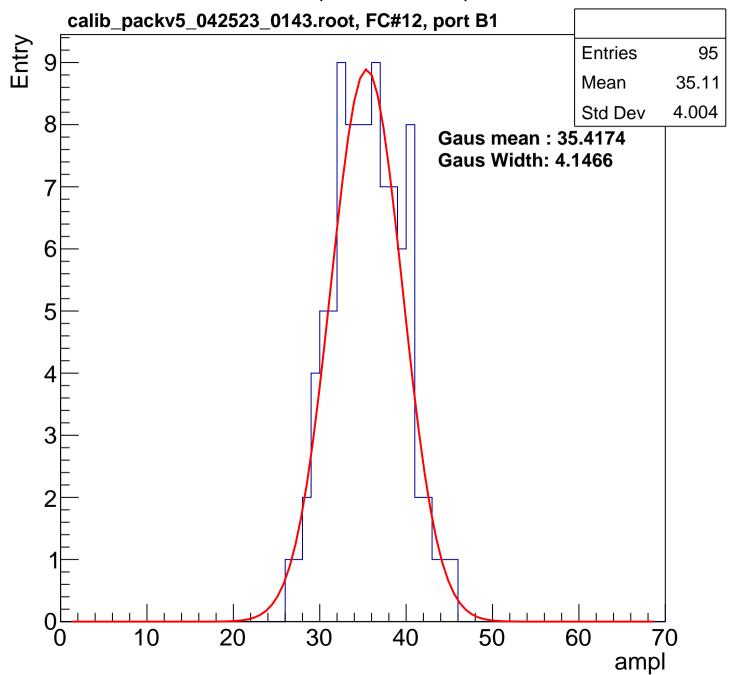


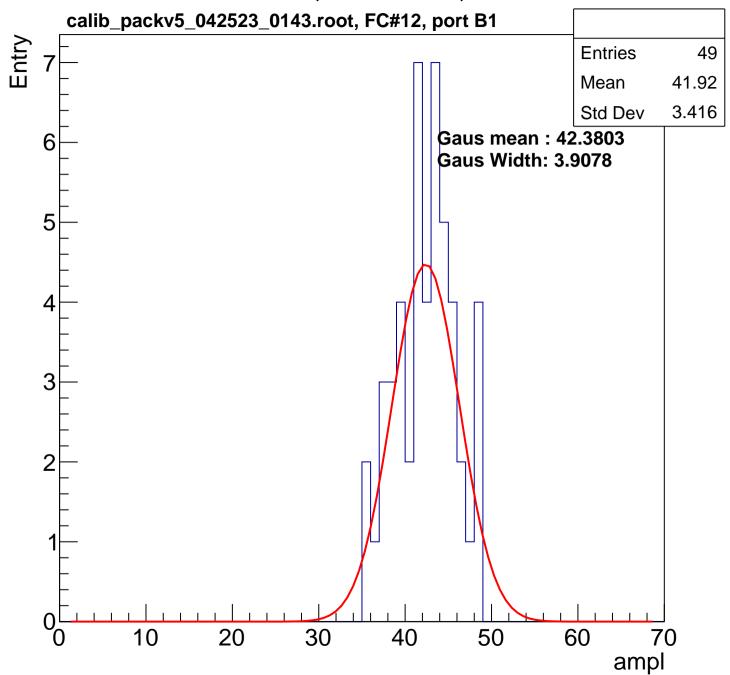


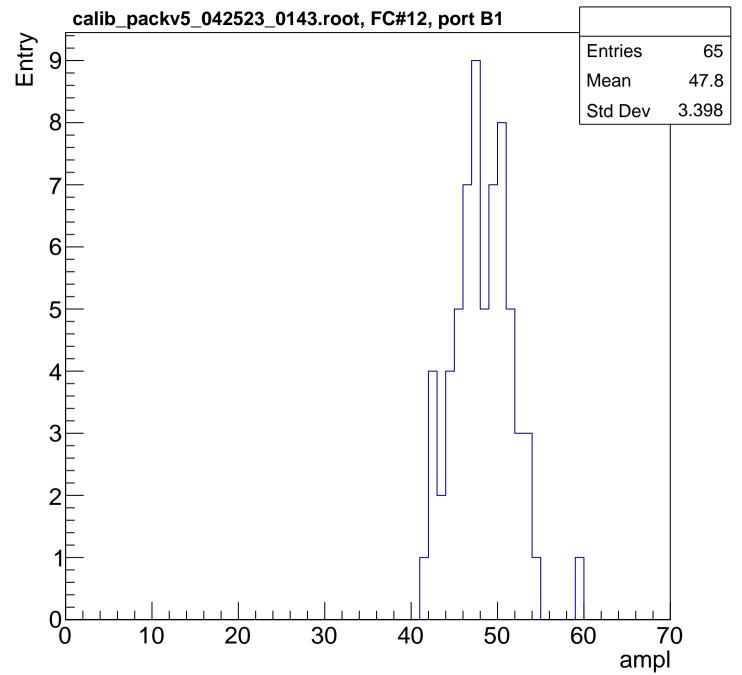


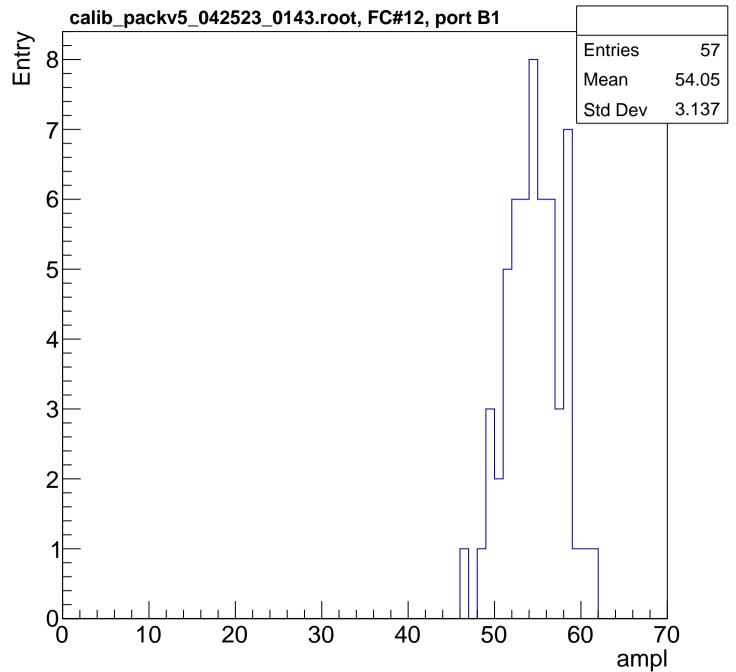


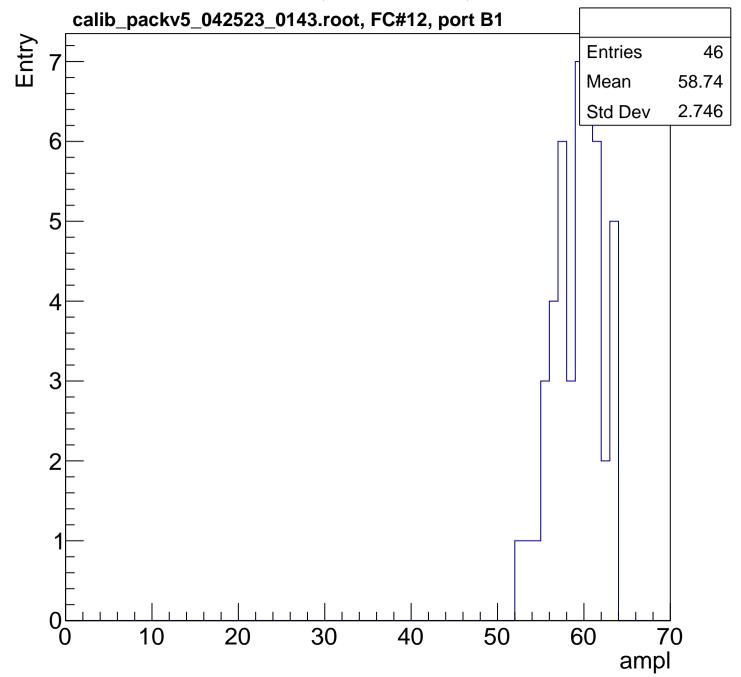


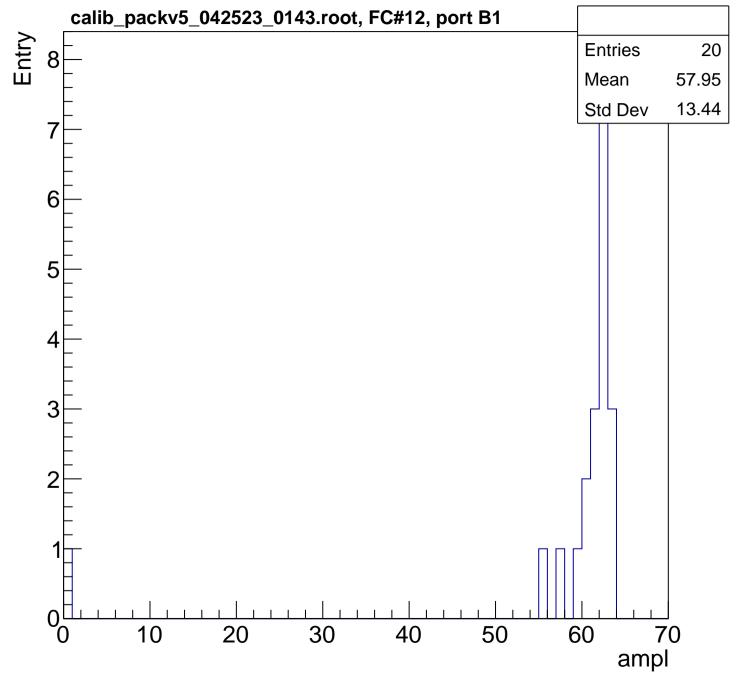


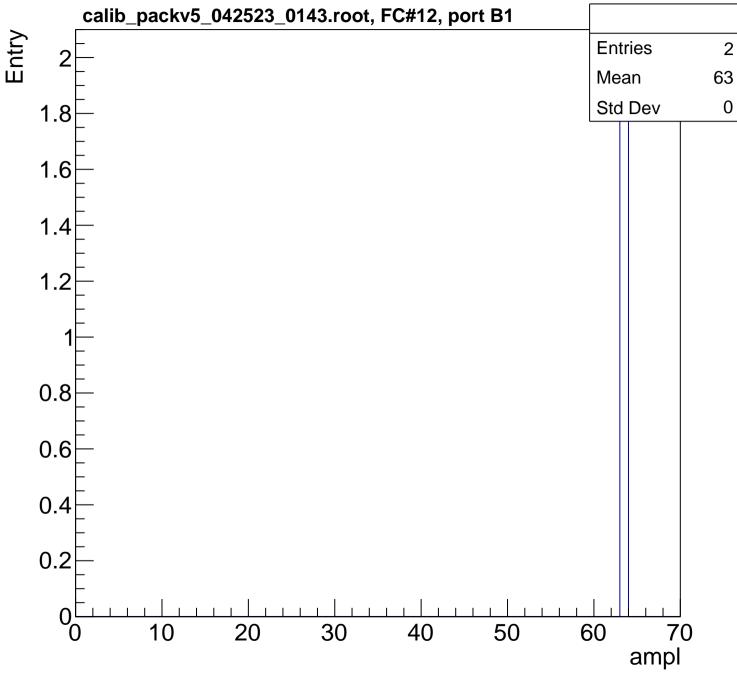


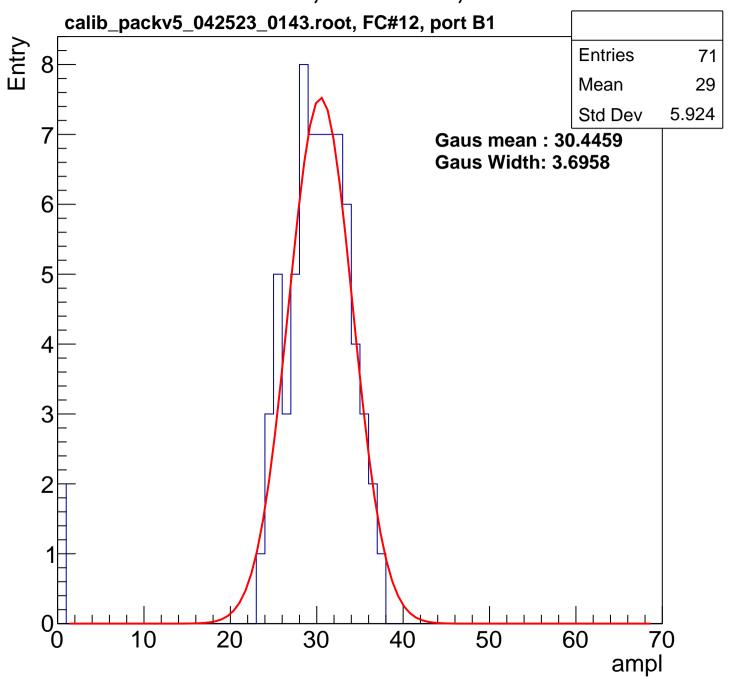


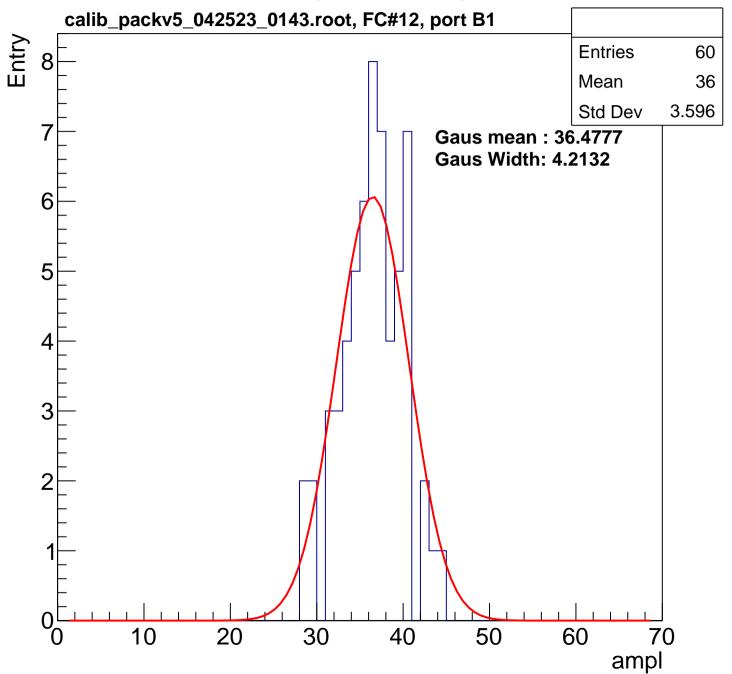


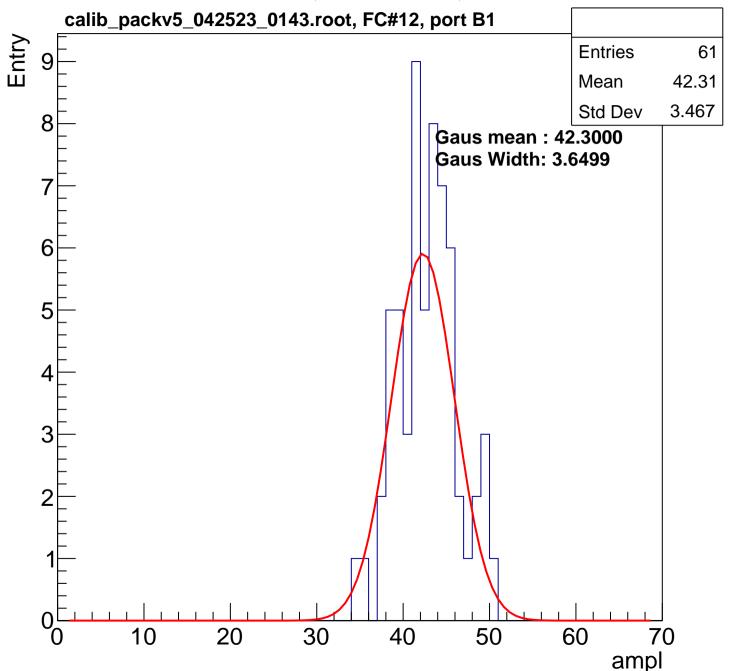


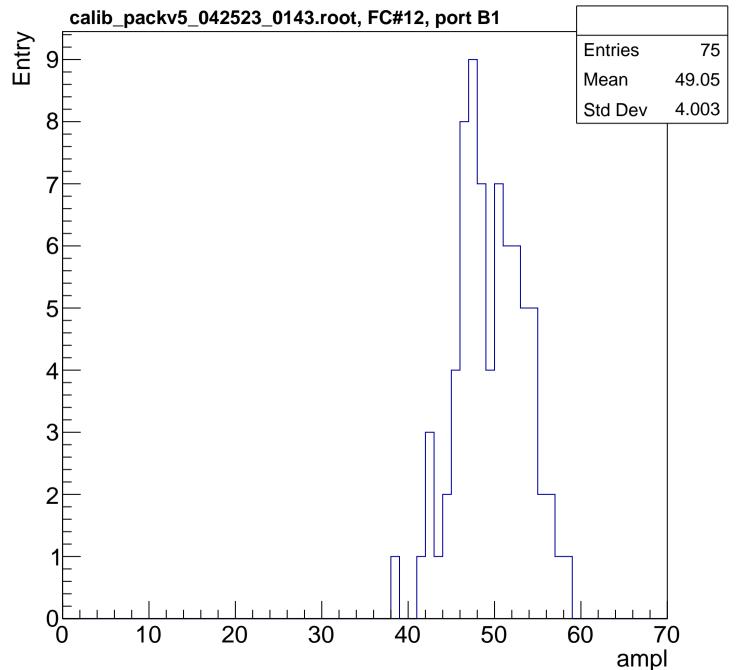


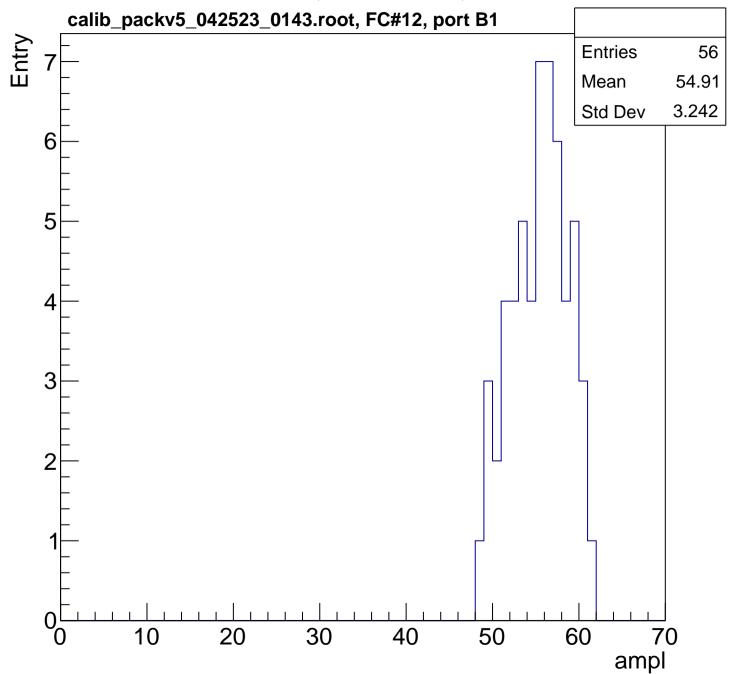


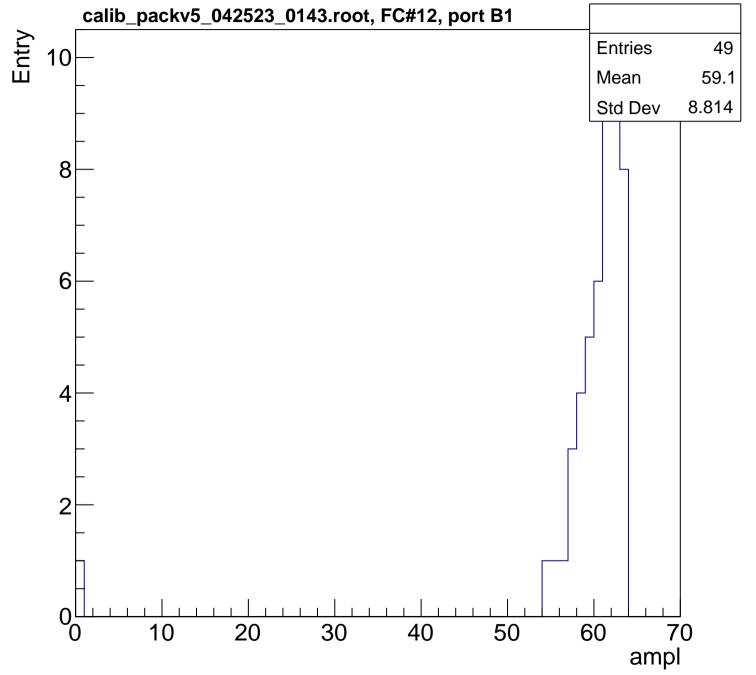


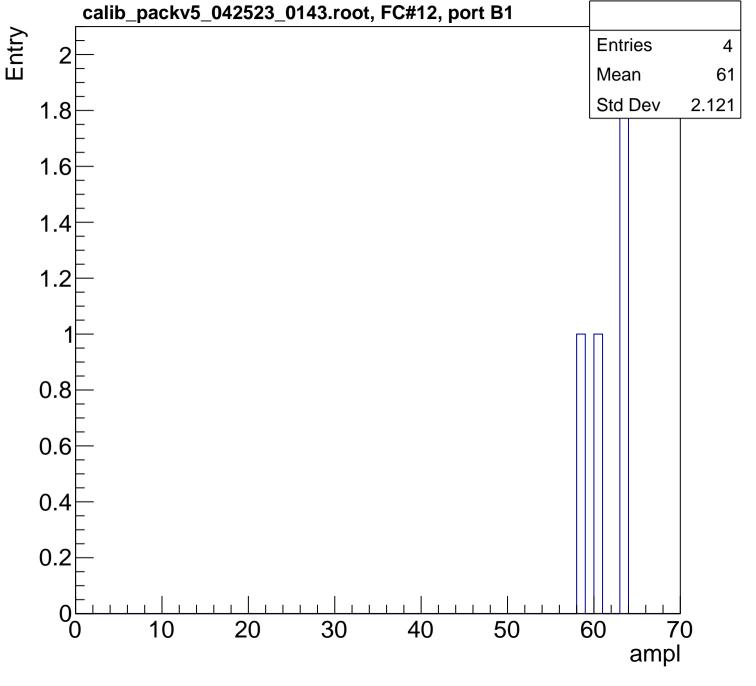




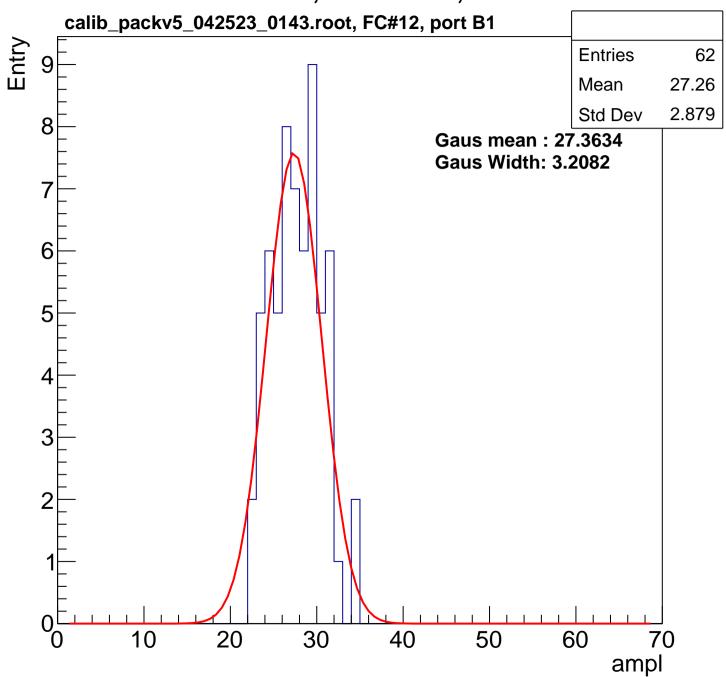


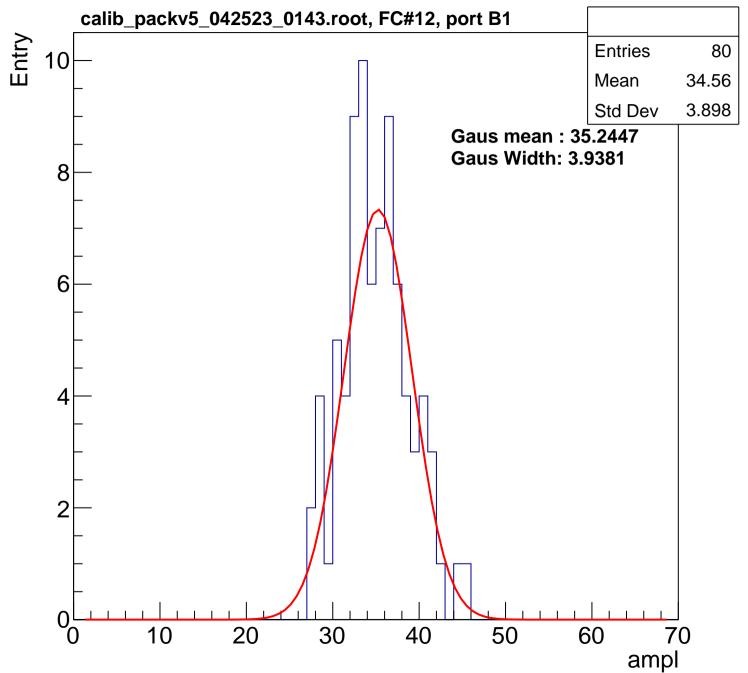


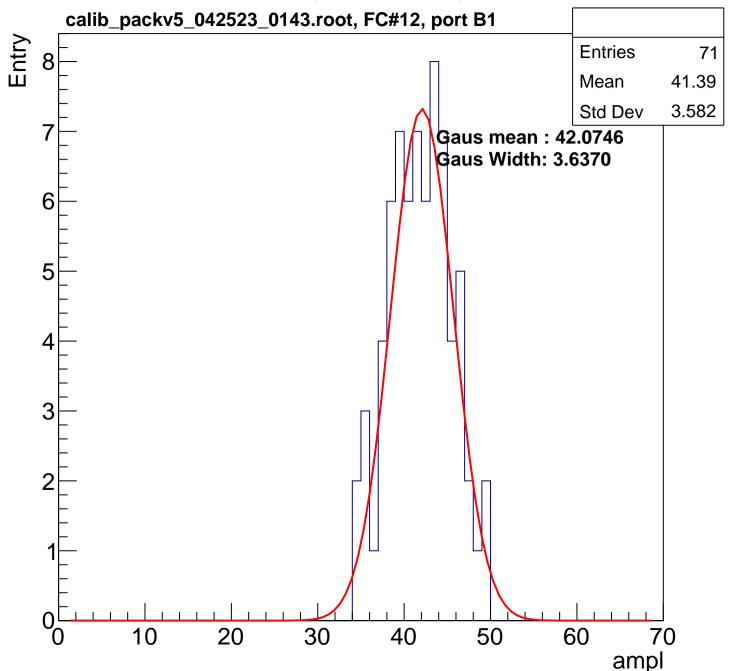


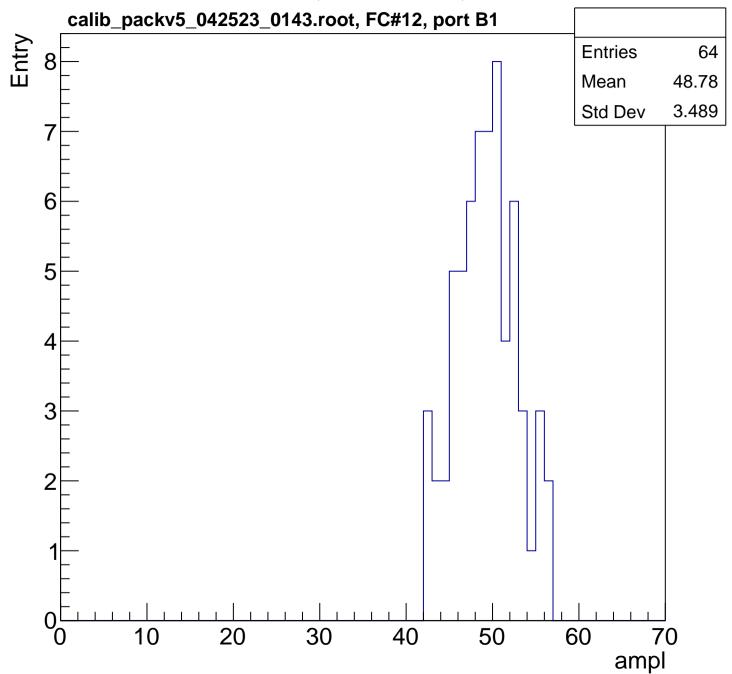


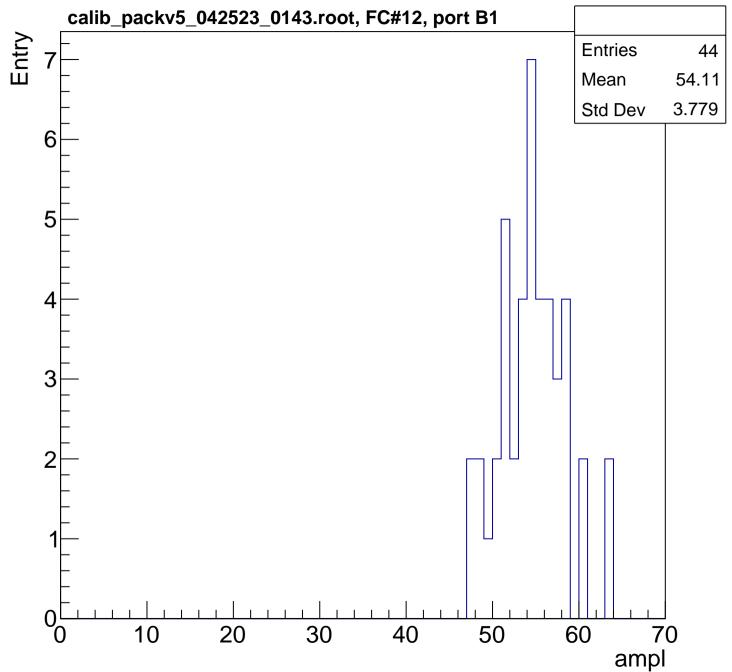


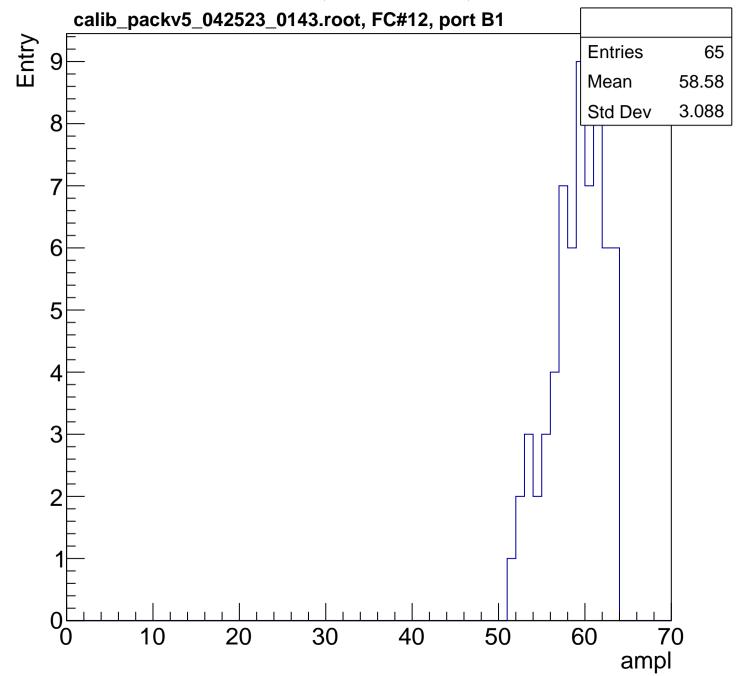


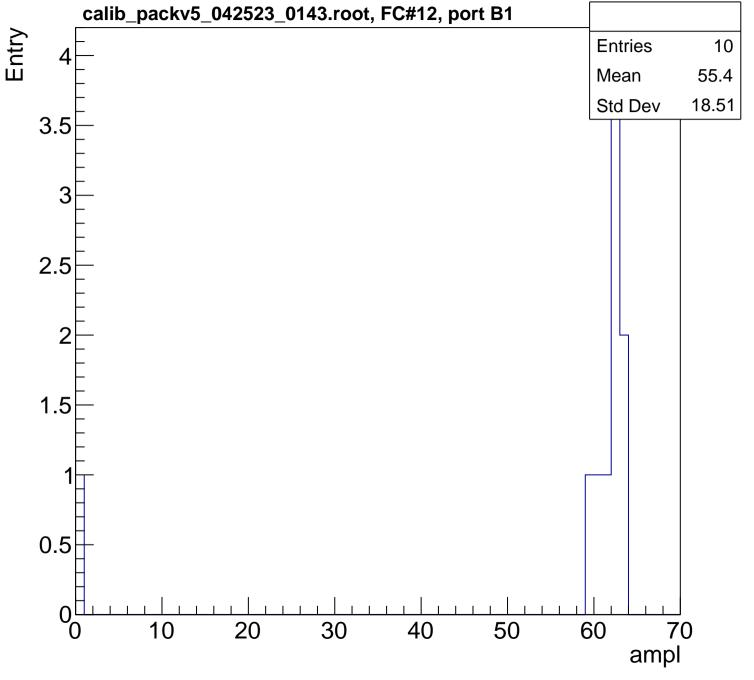




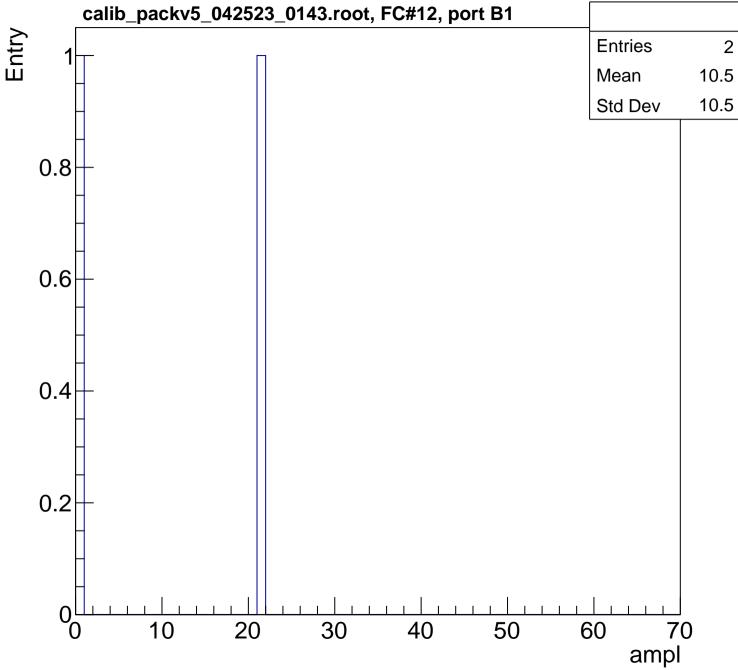


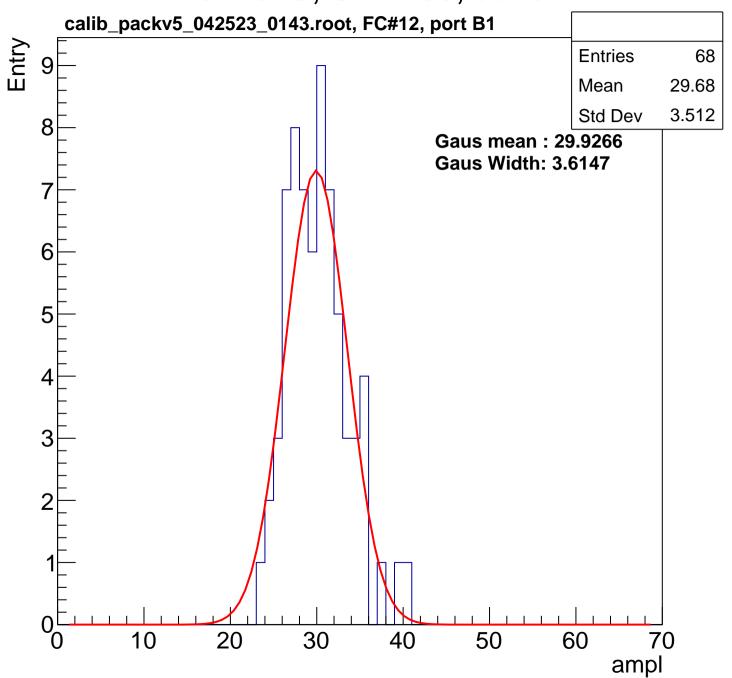


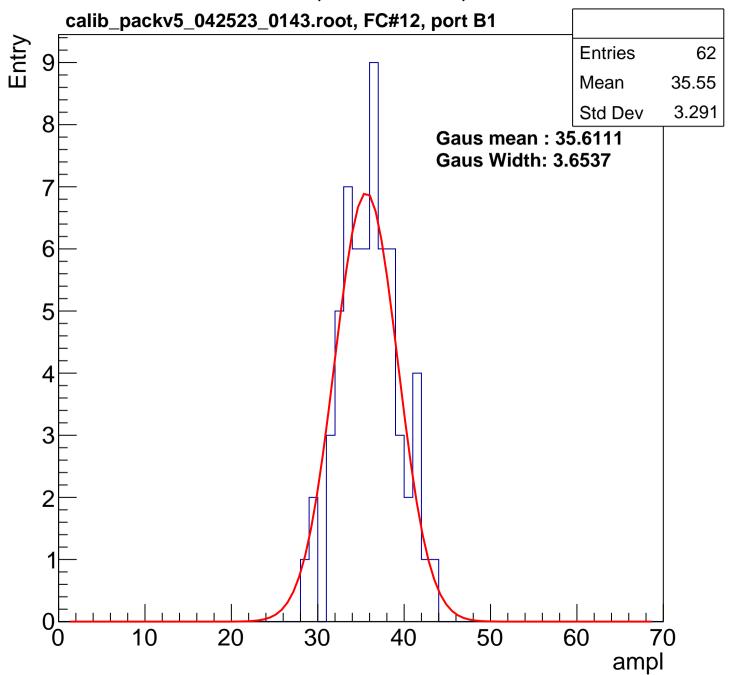


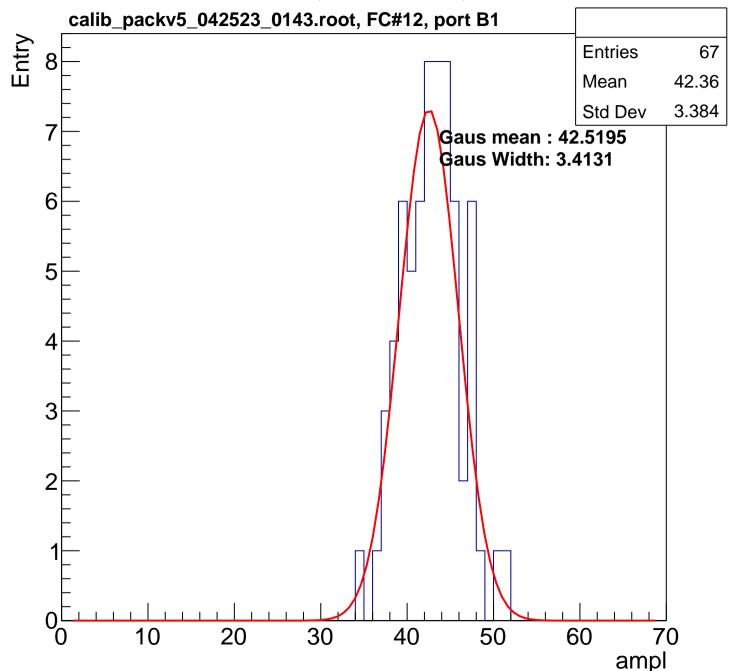


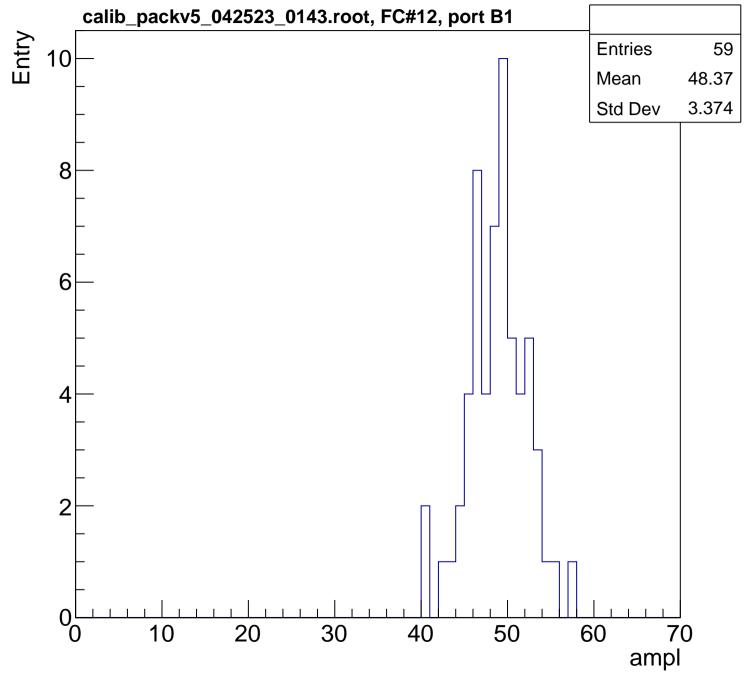
2

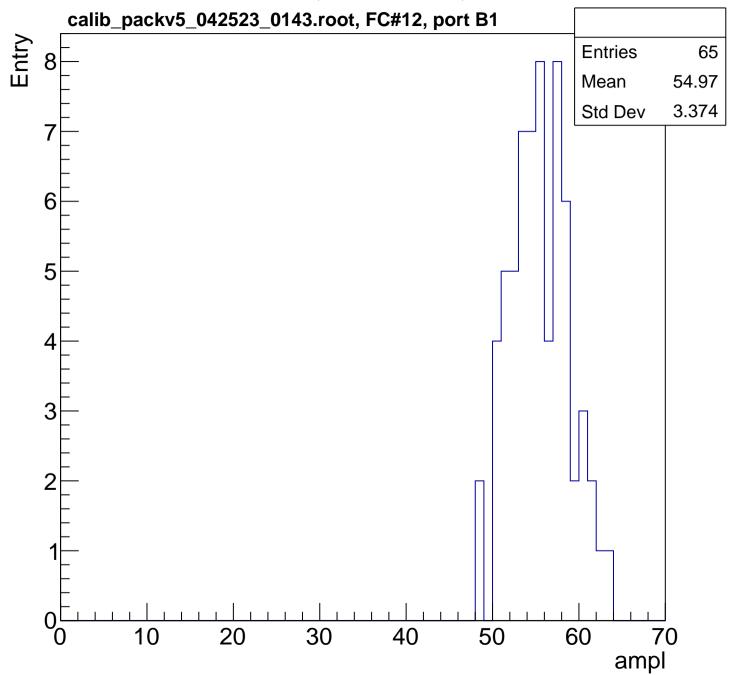


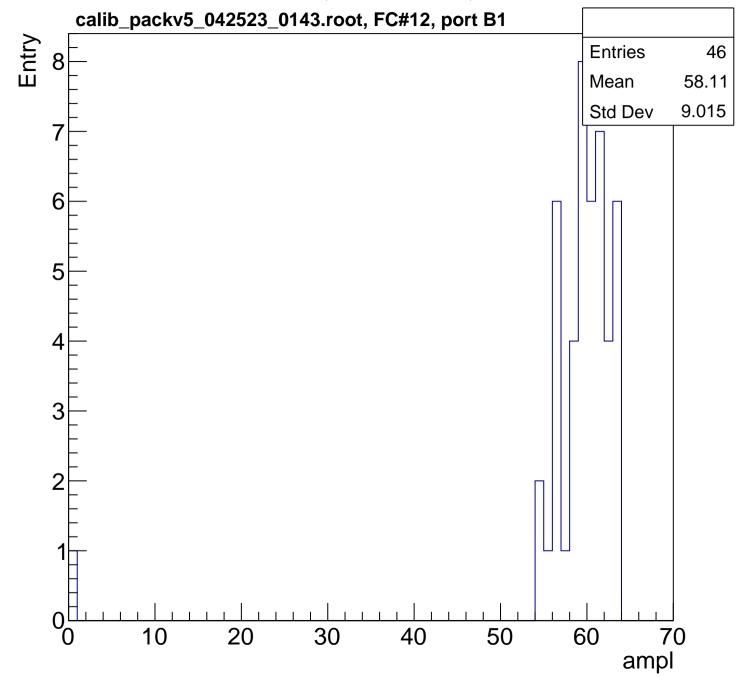


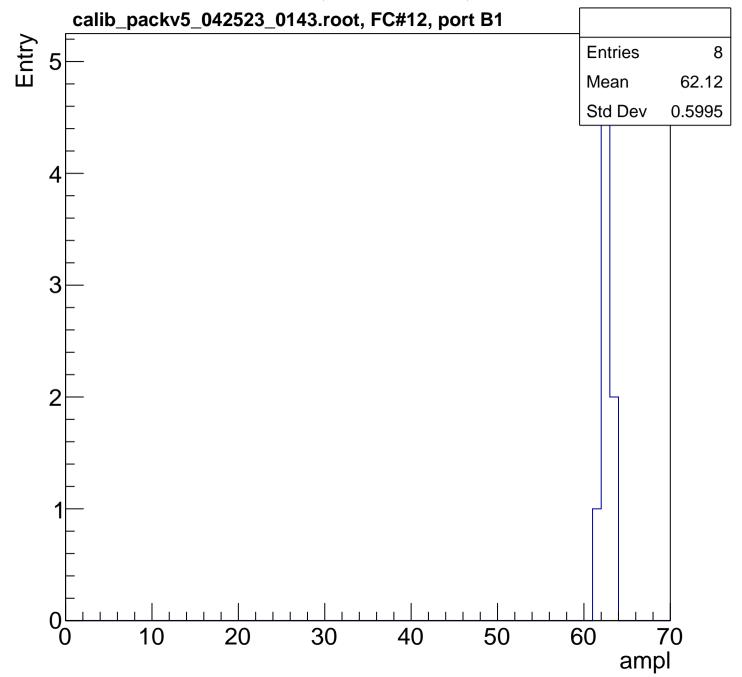


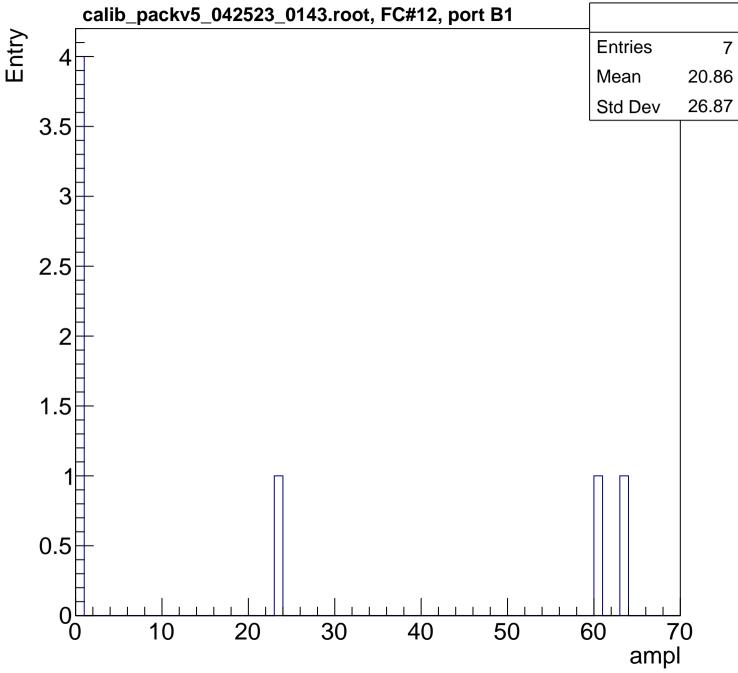


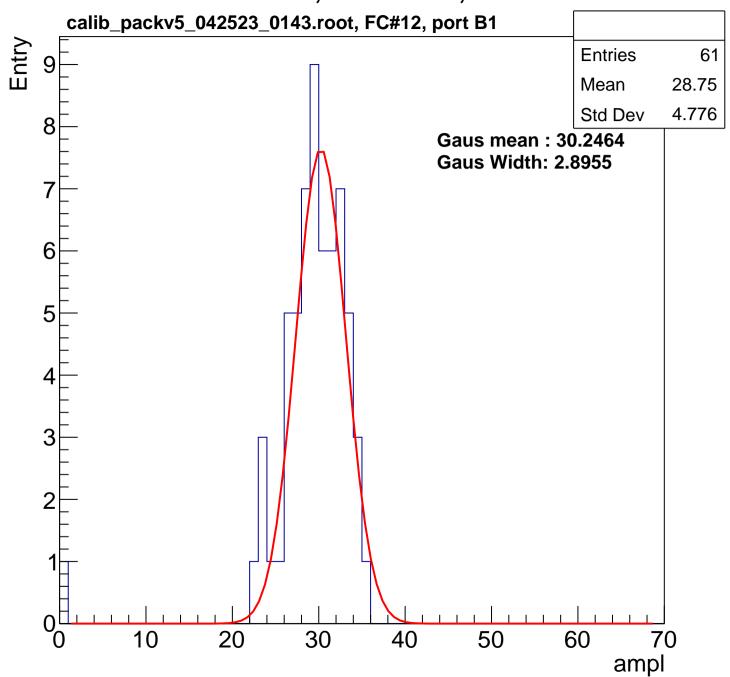


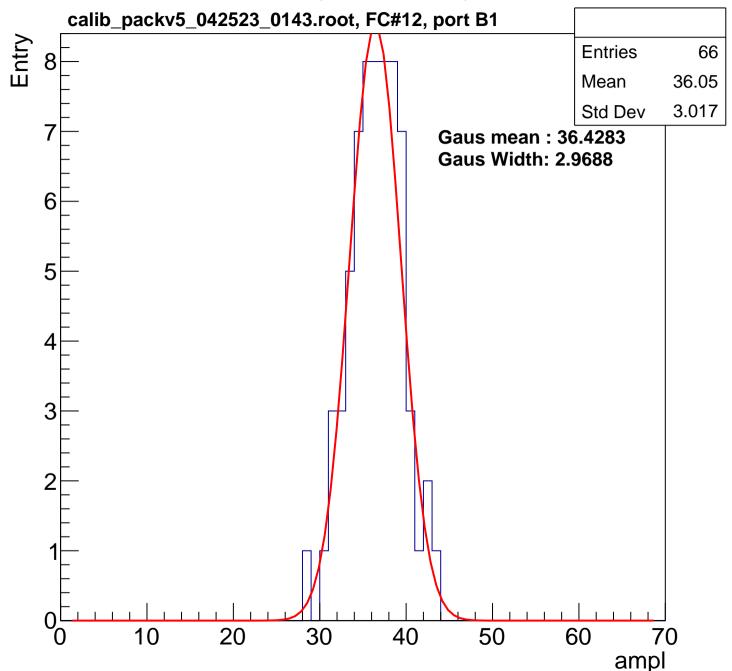


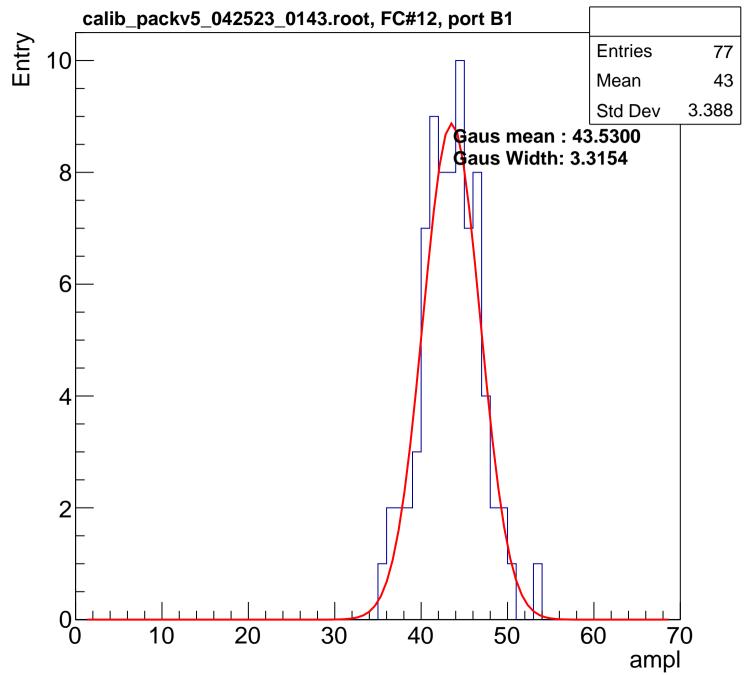


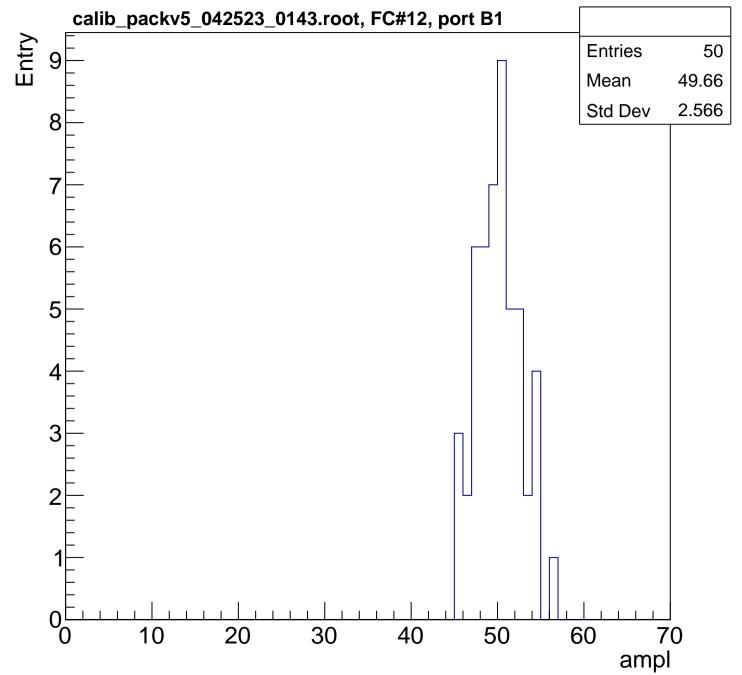


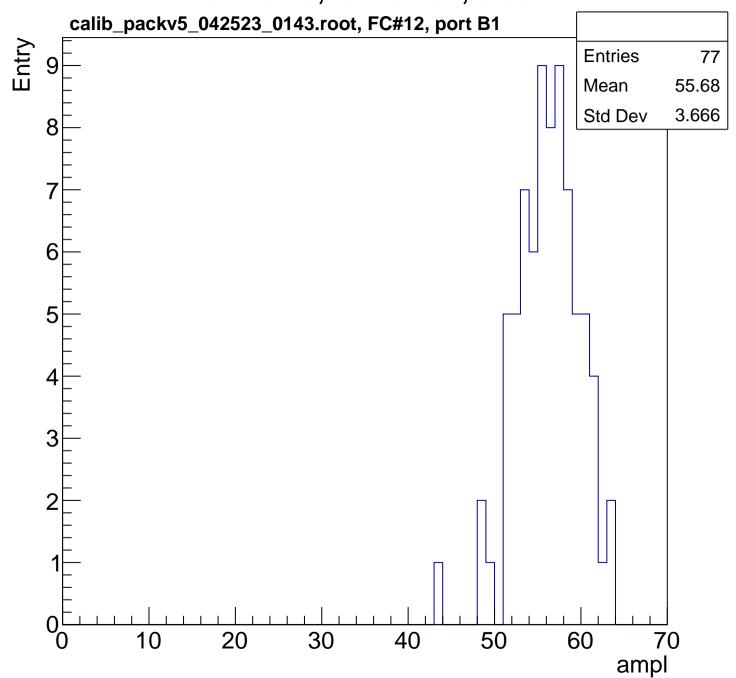


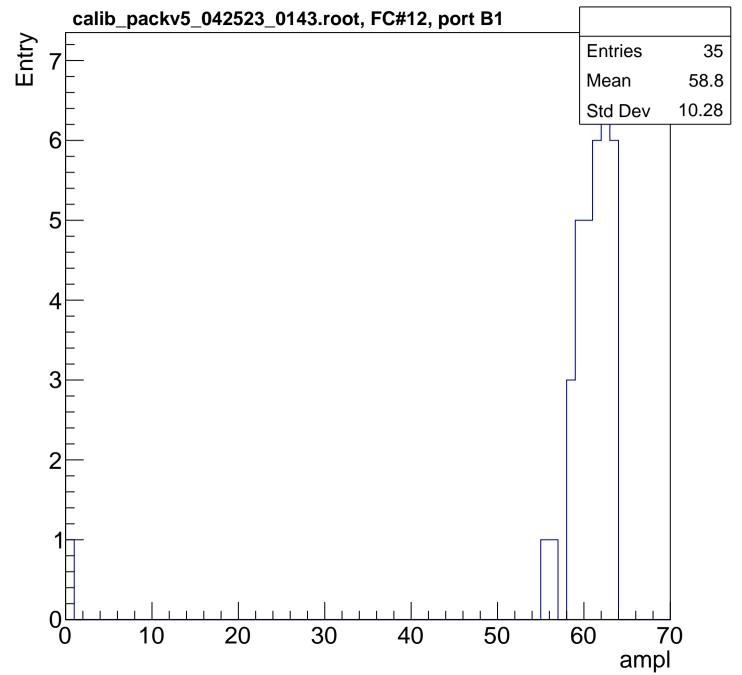


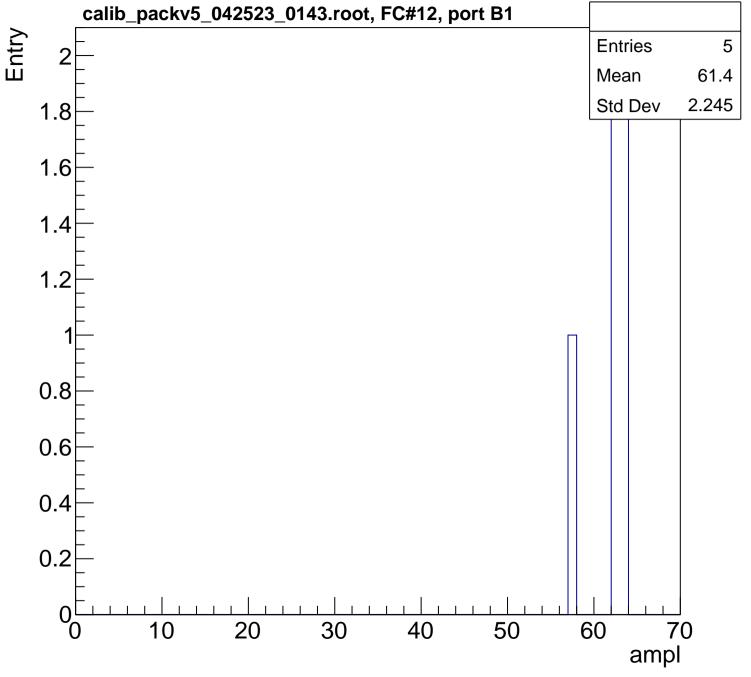








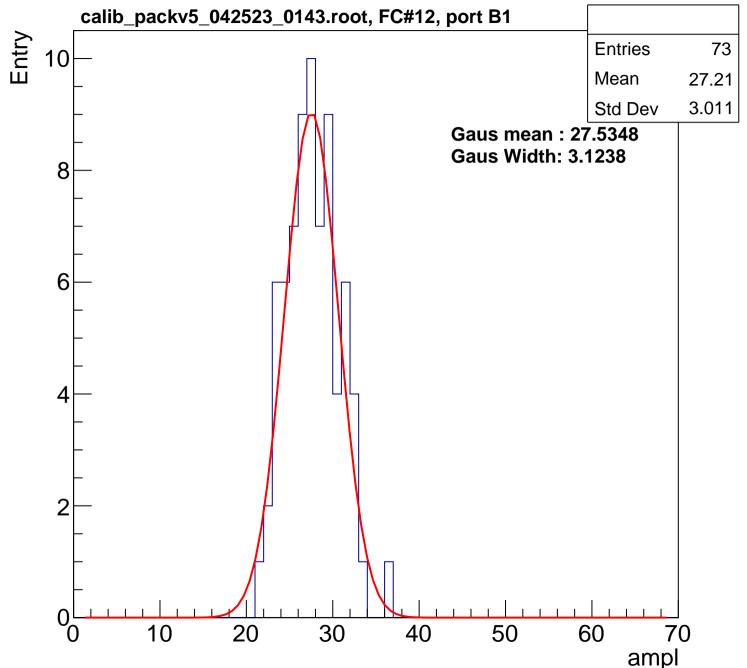


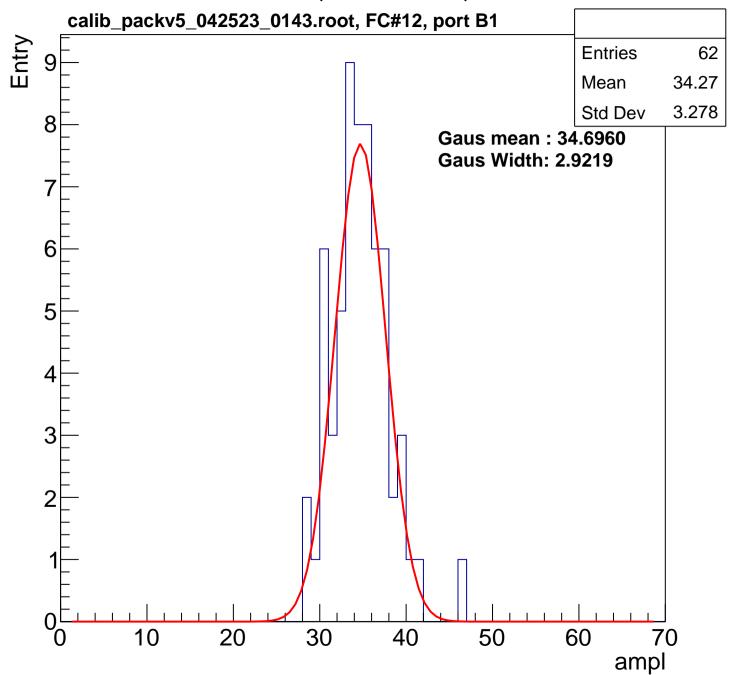


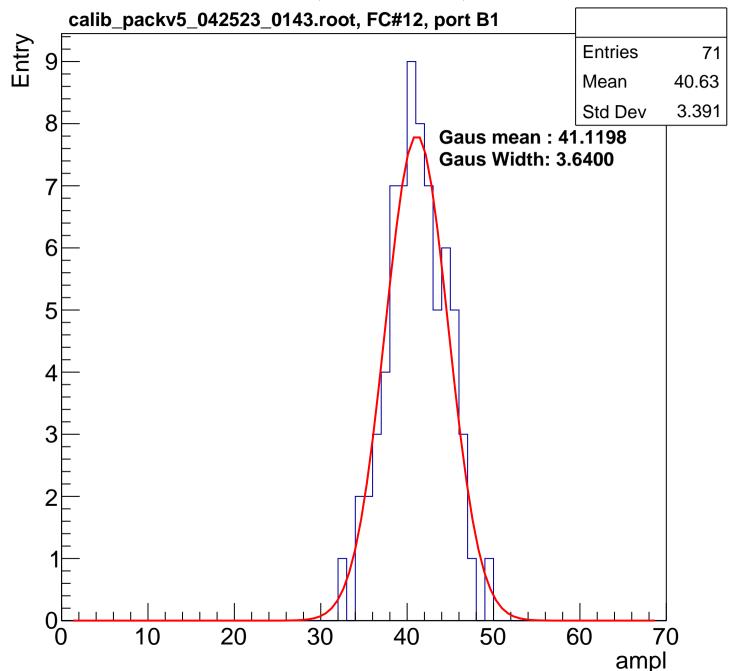
B0L102S, U7-ch61, adc7 calib_packv5_042523_0143.root, FC#12, port B1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60

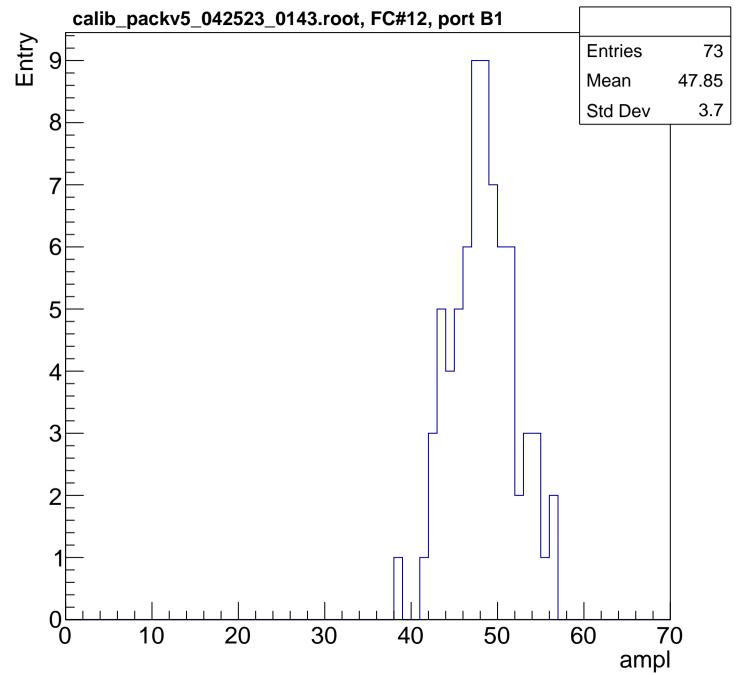
70

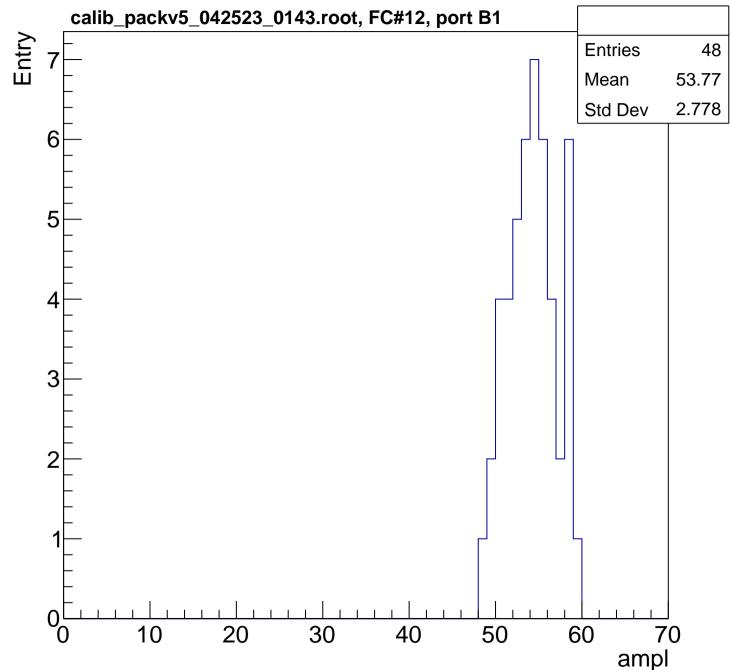
ampl

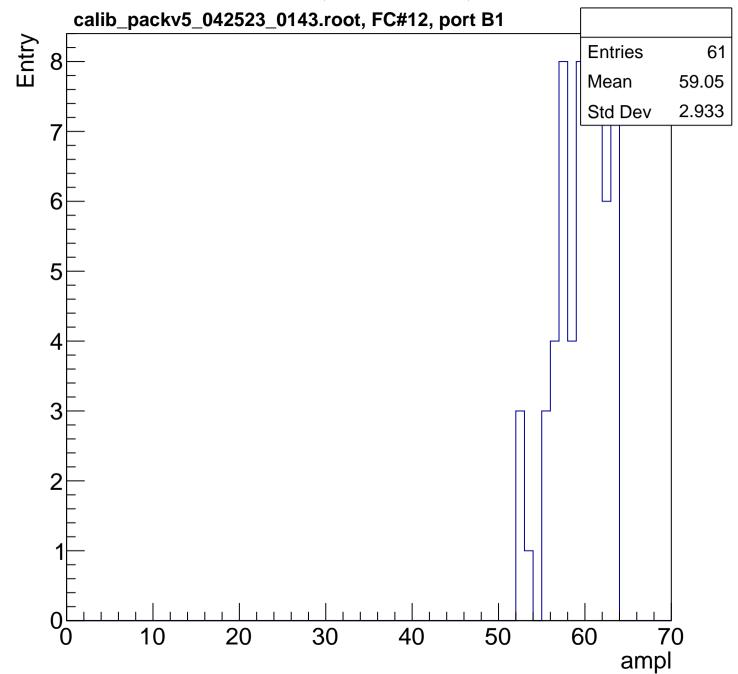


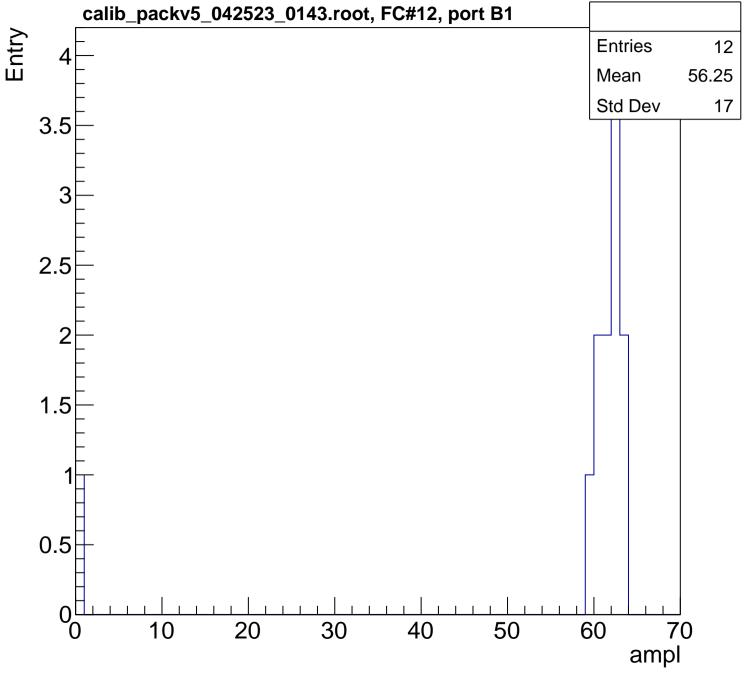




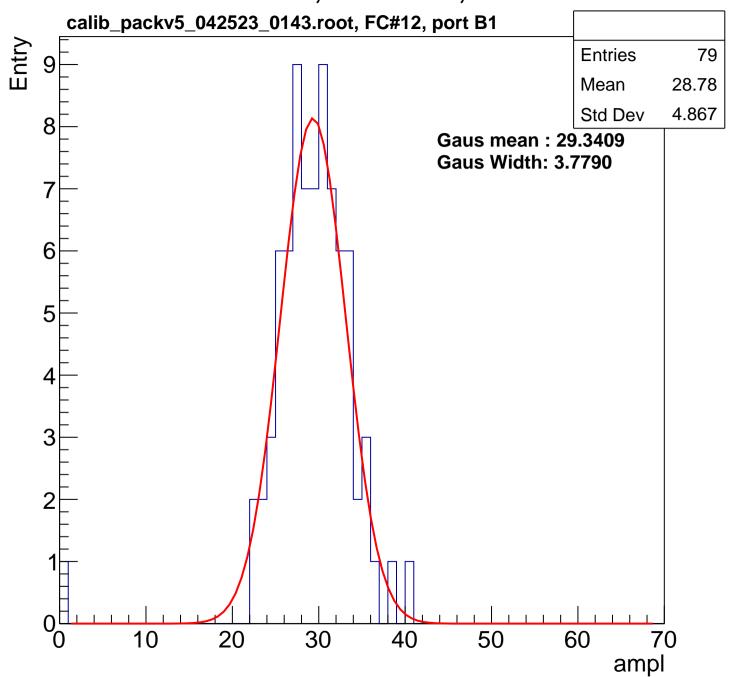


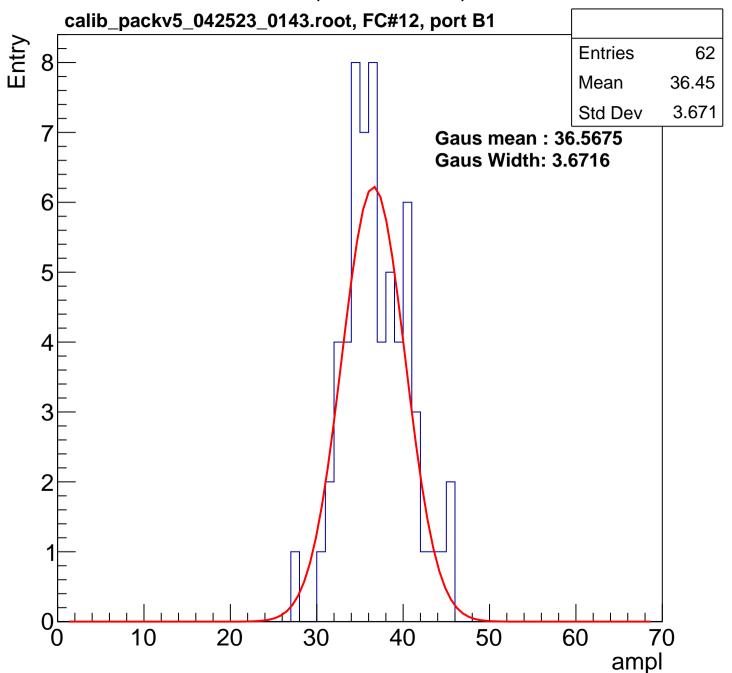


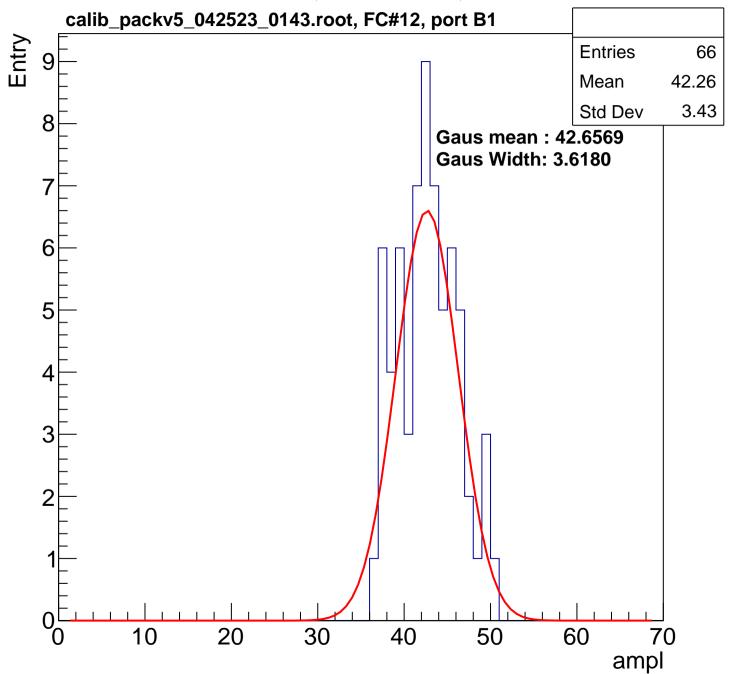


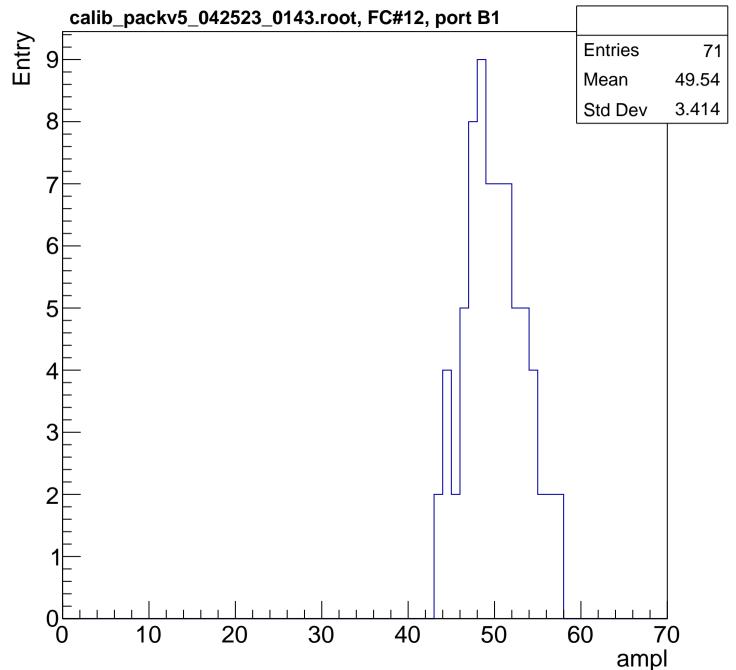


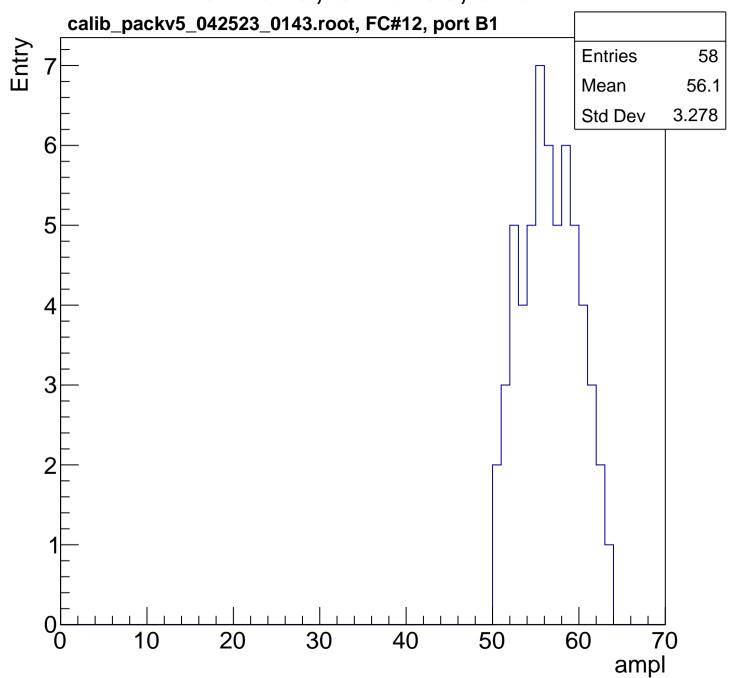
B0L102S, U7-ch62, adc7 calib_packv5_042523_0143.root, FC#12, port B1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

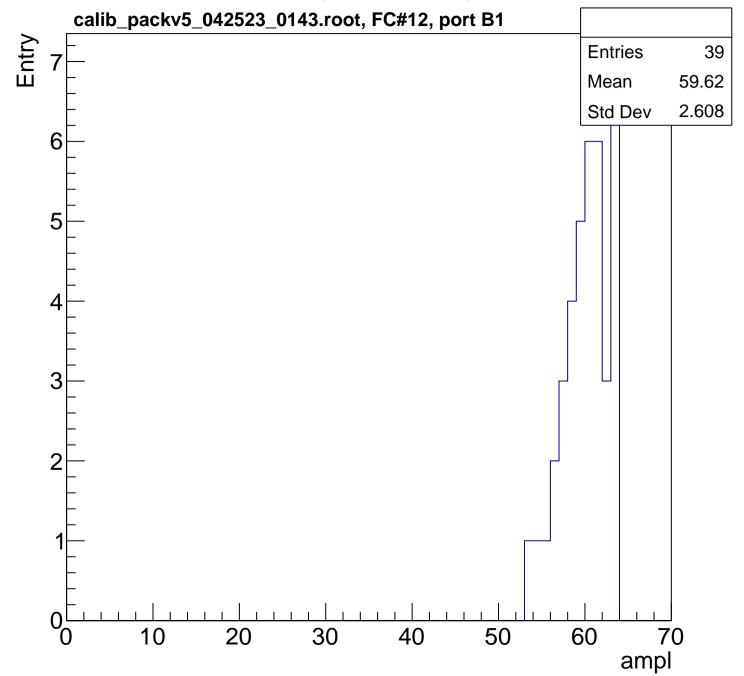


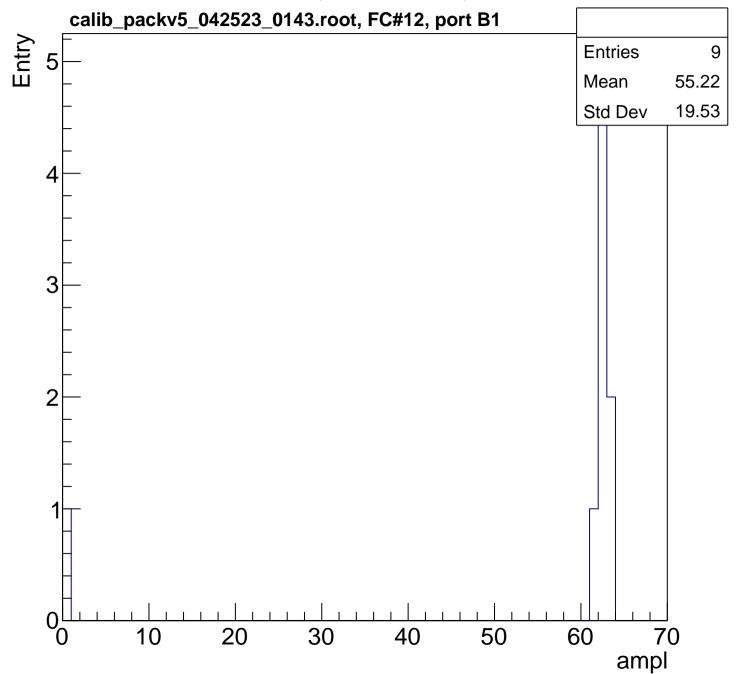




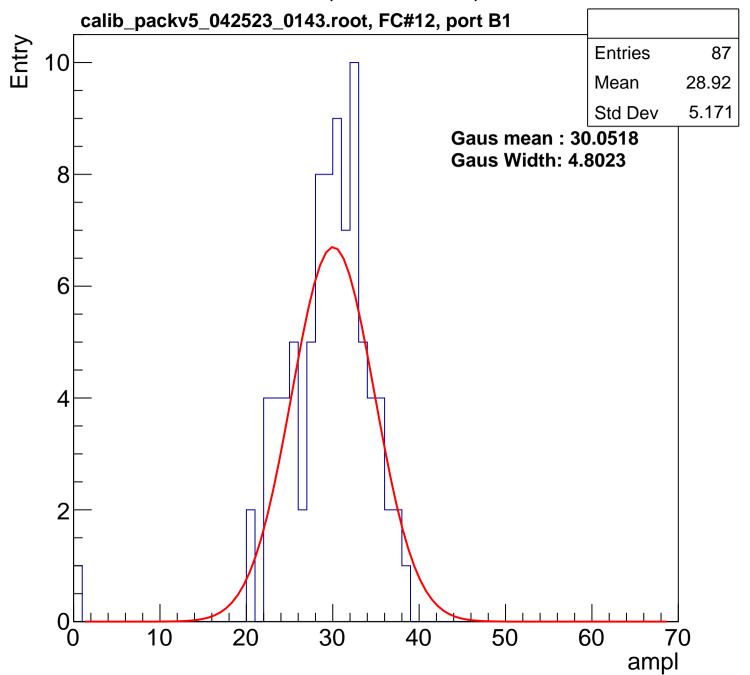


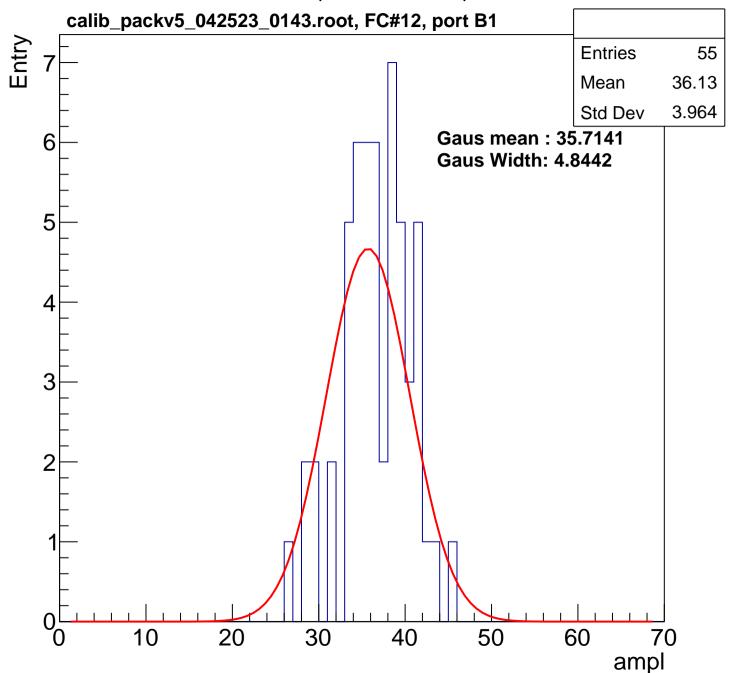


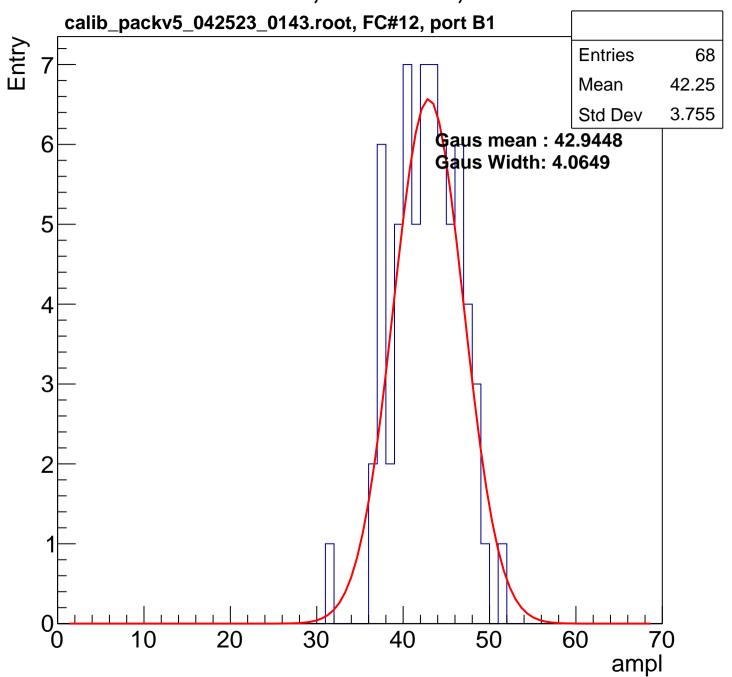


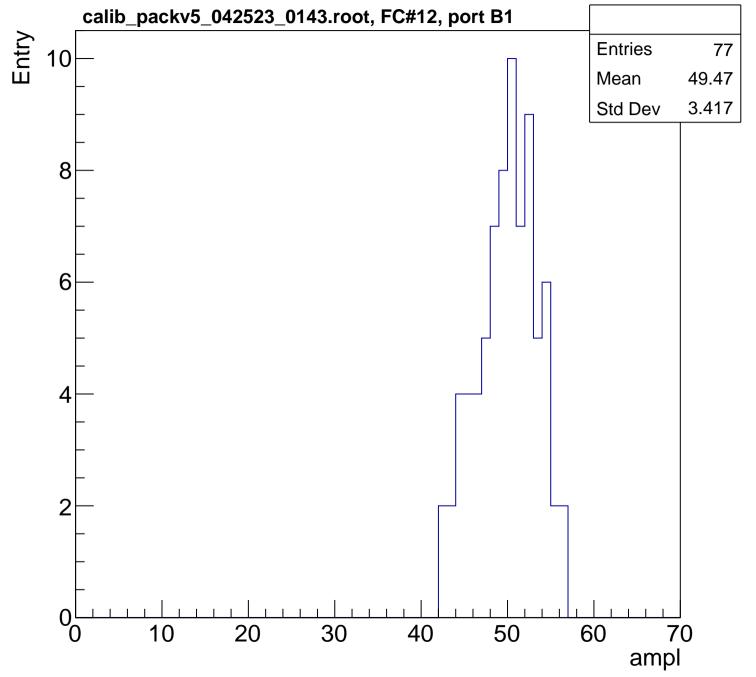


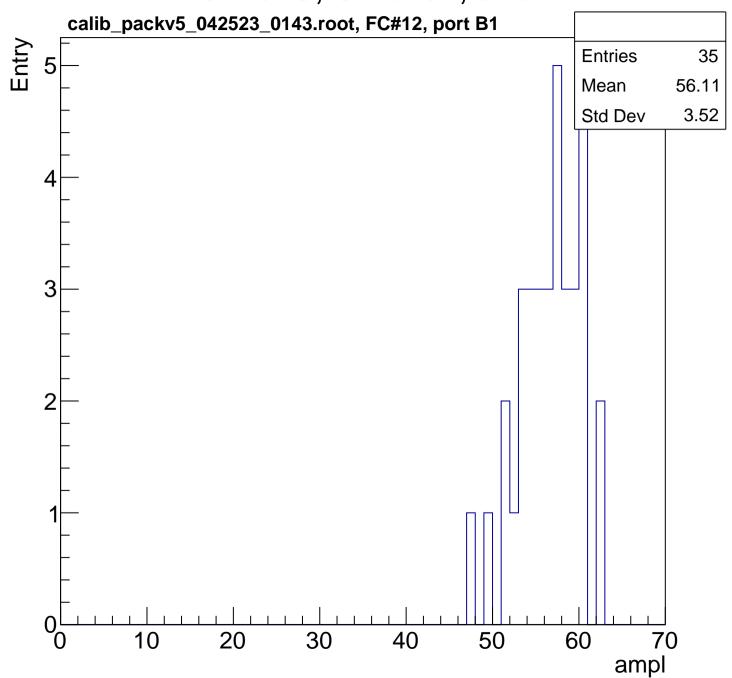
B0L102S, U7-ch63, adc7 calib_packv5_042523_0143.root, FC#12, port B1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

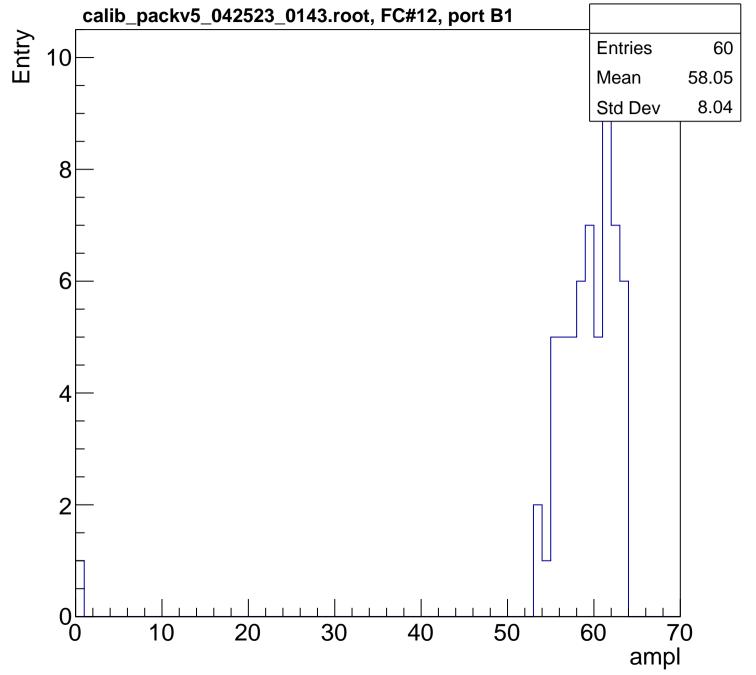


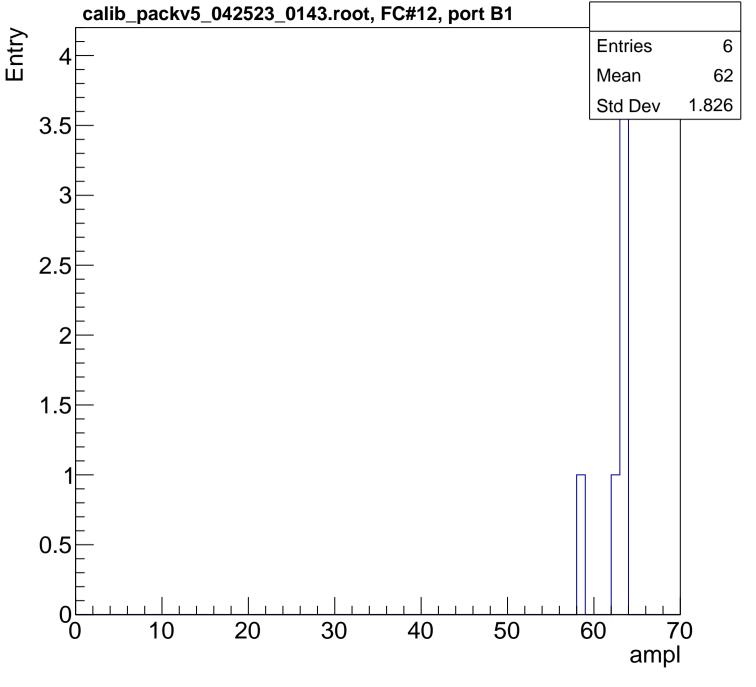




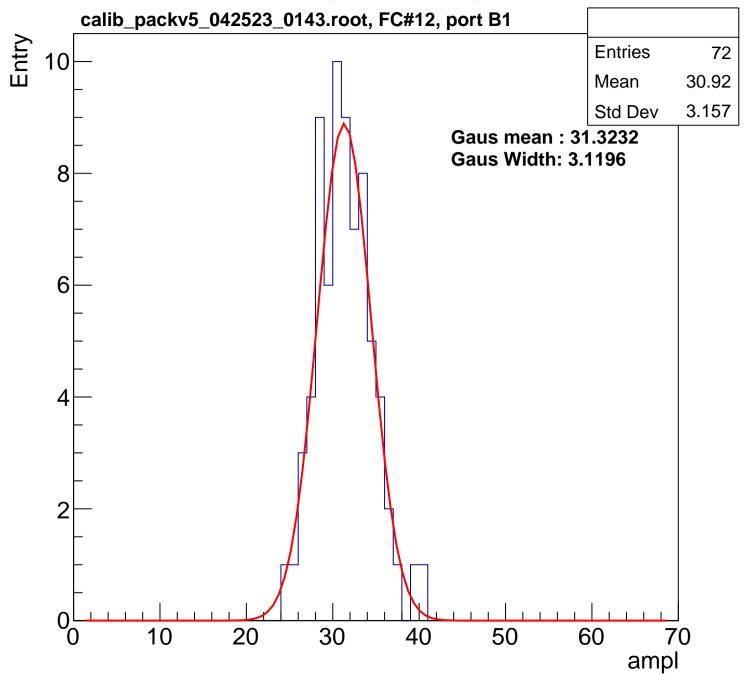


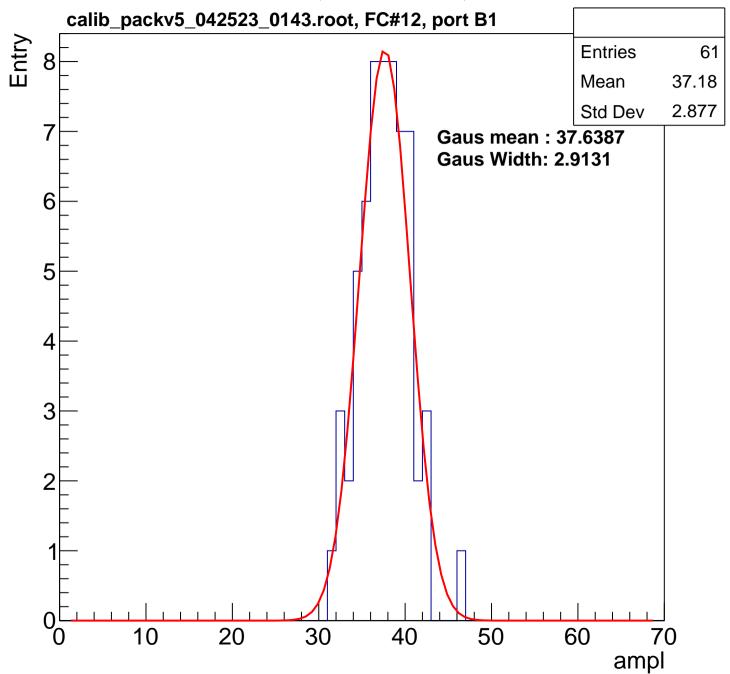


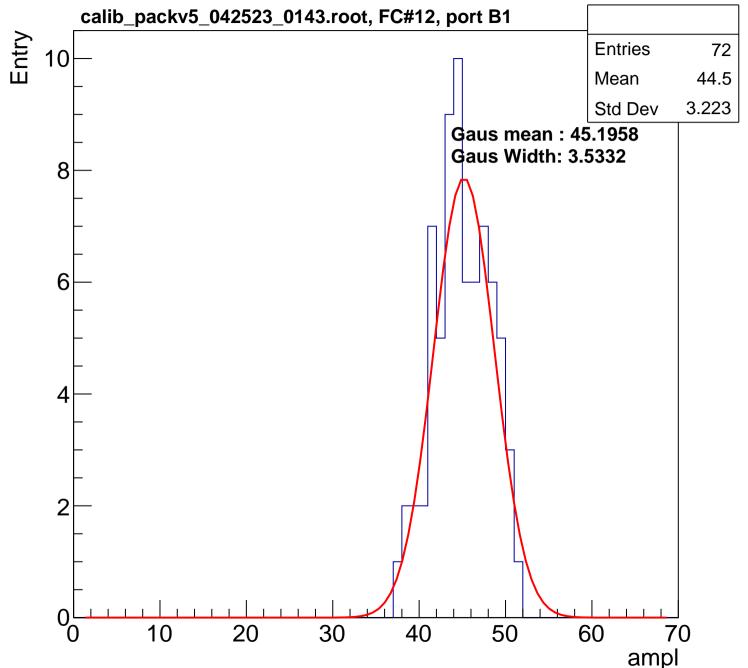


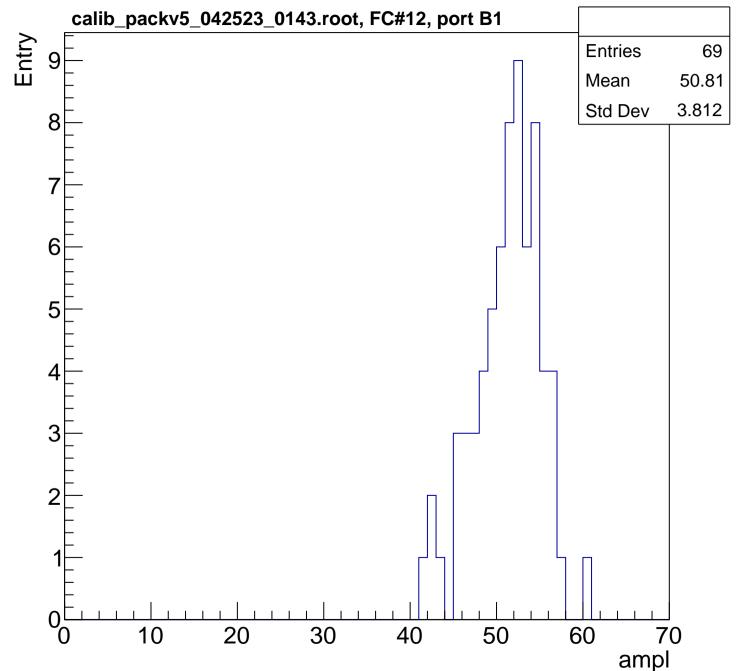


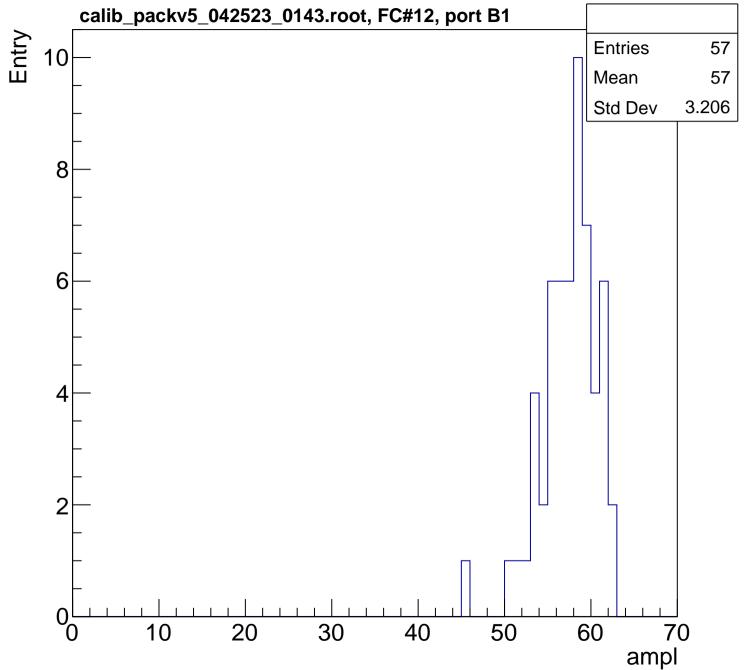


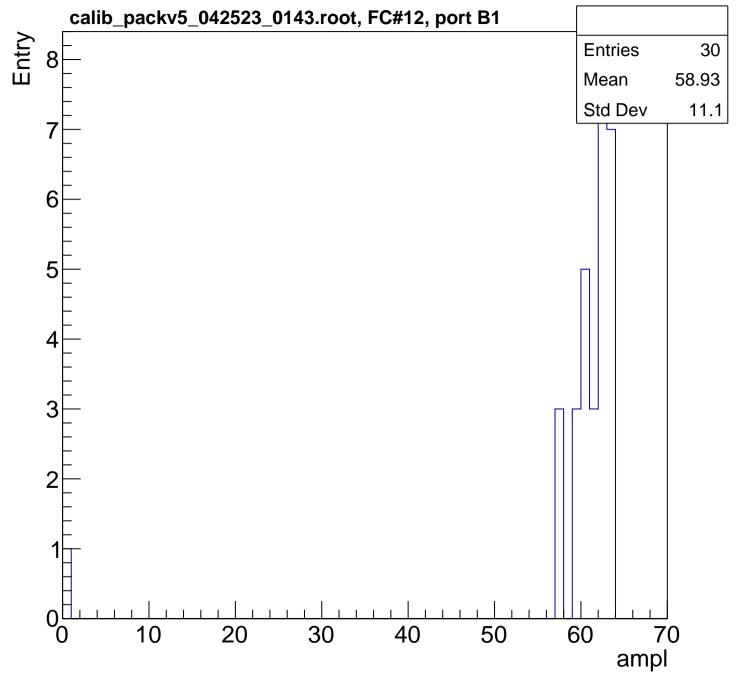


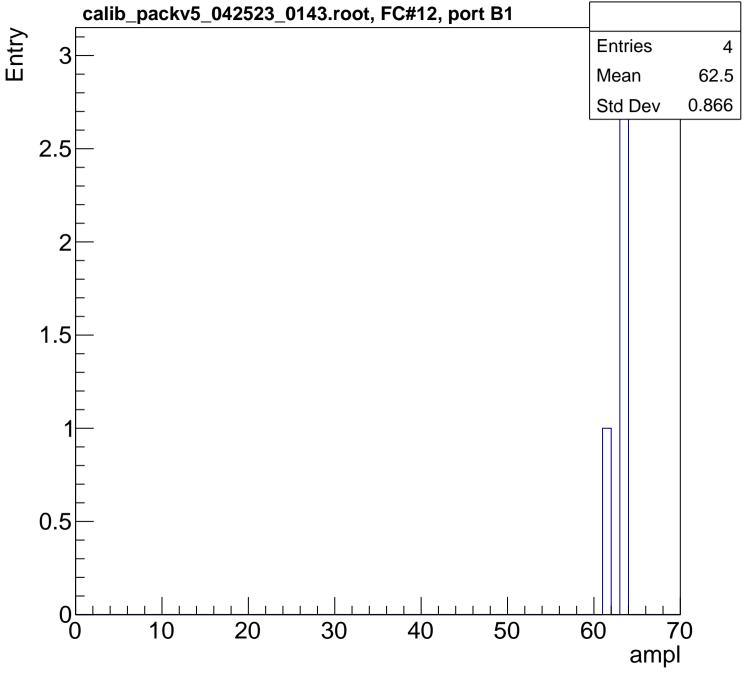




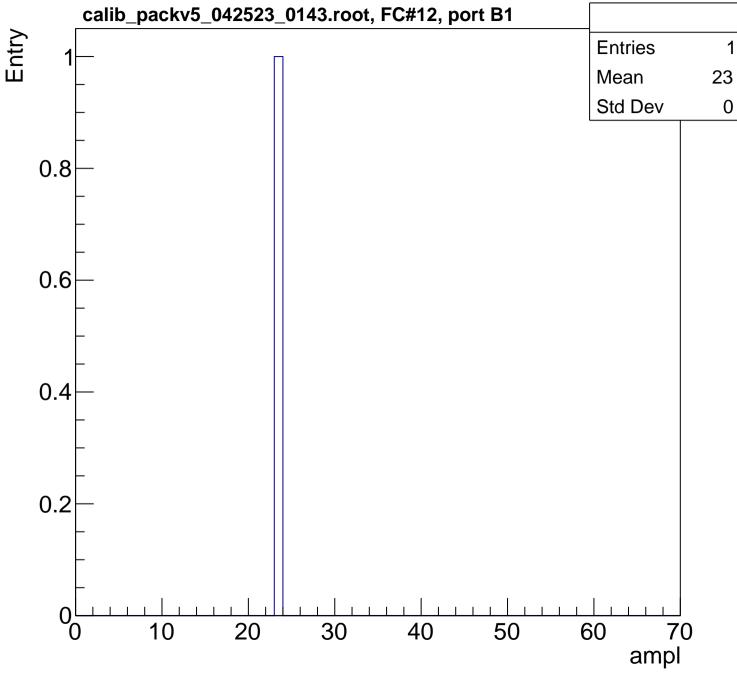


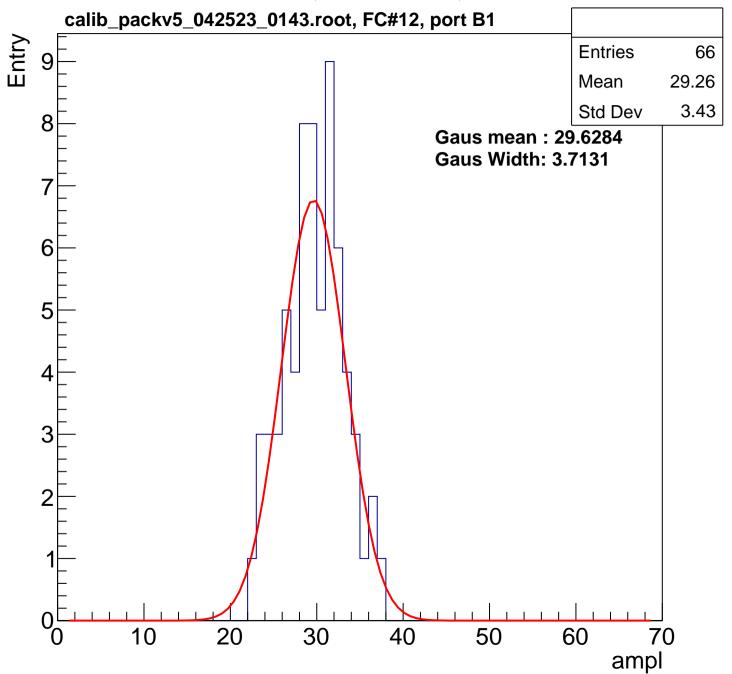


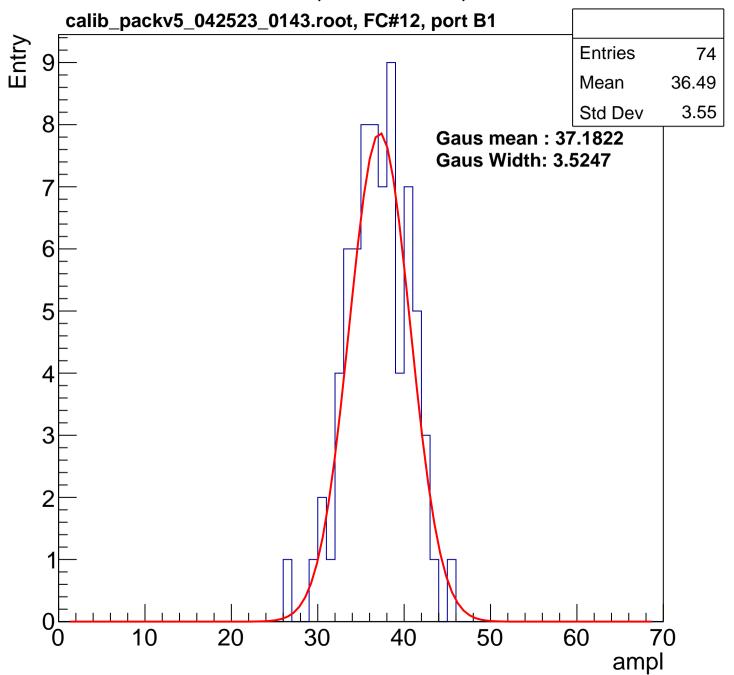


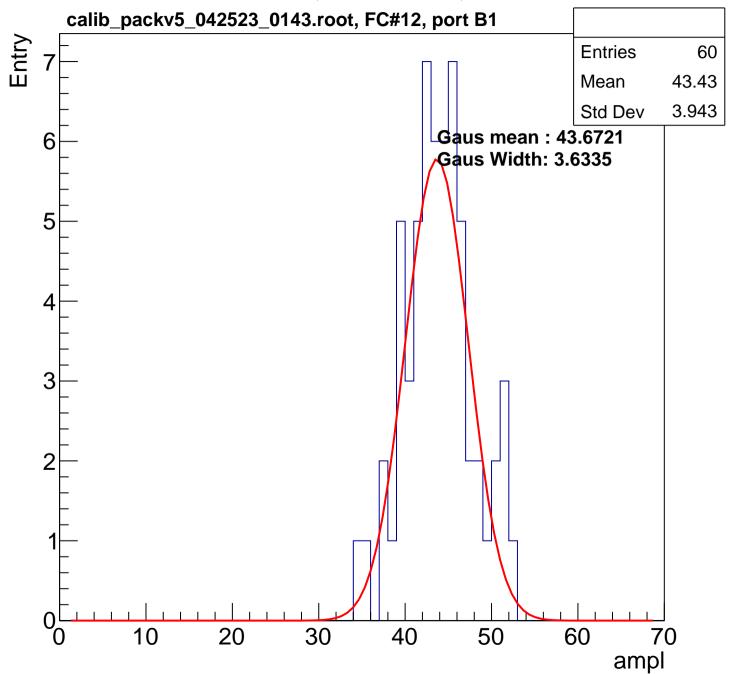


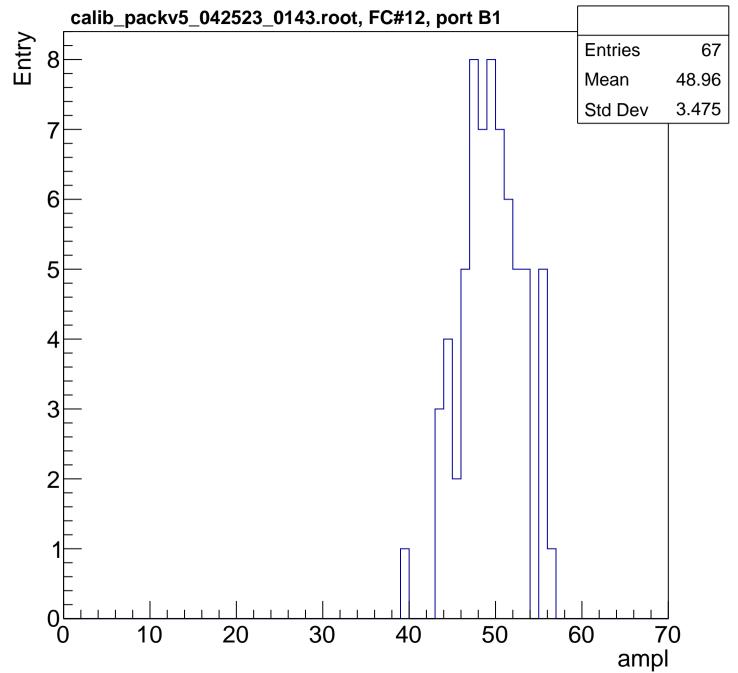
0

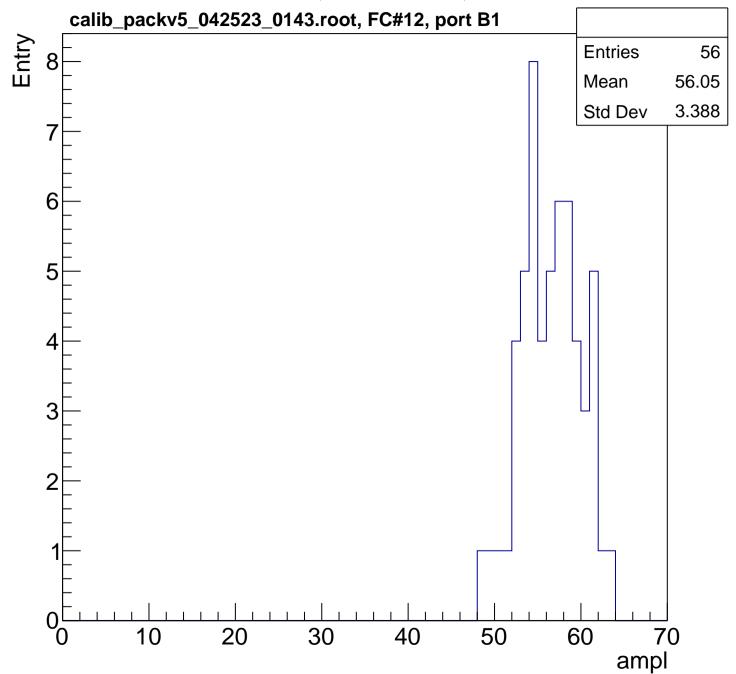


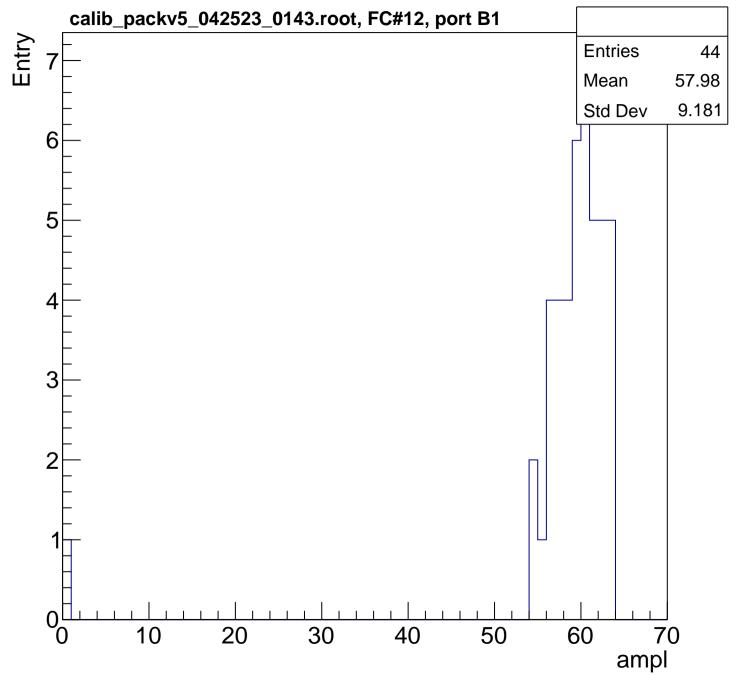


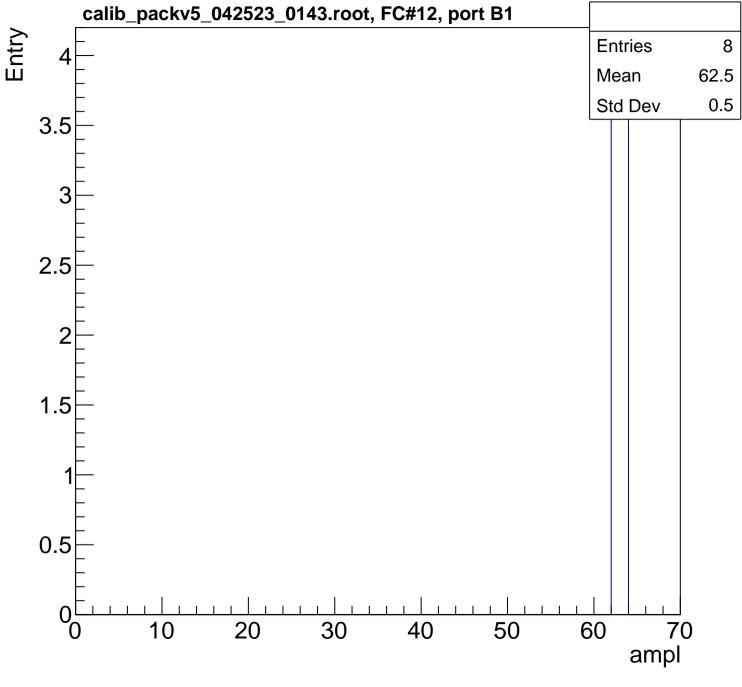




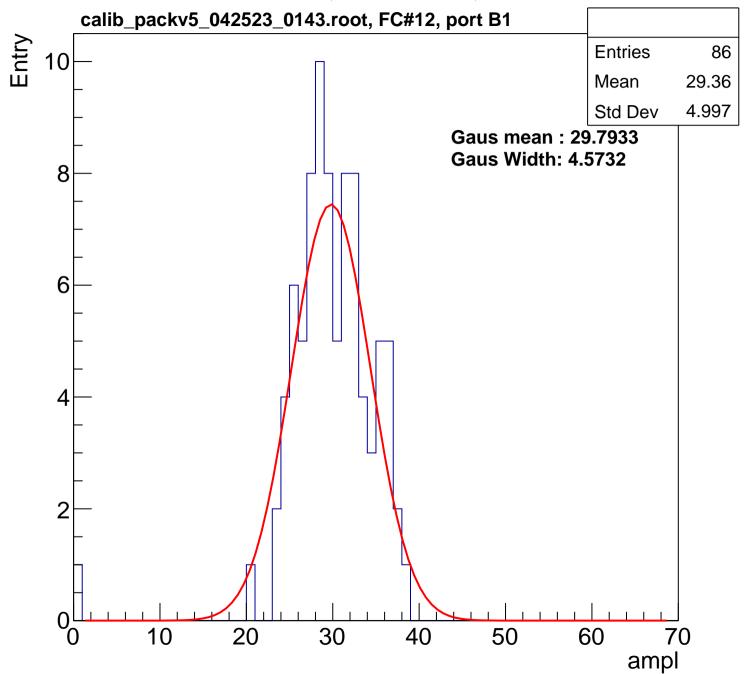


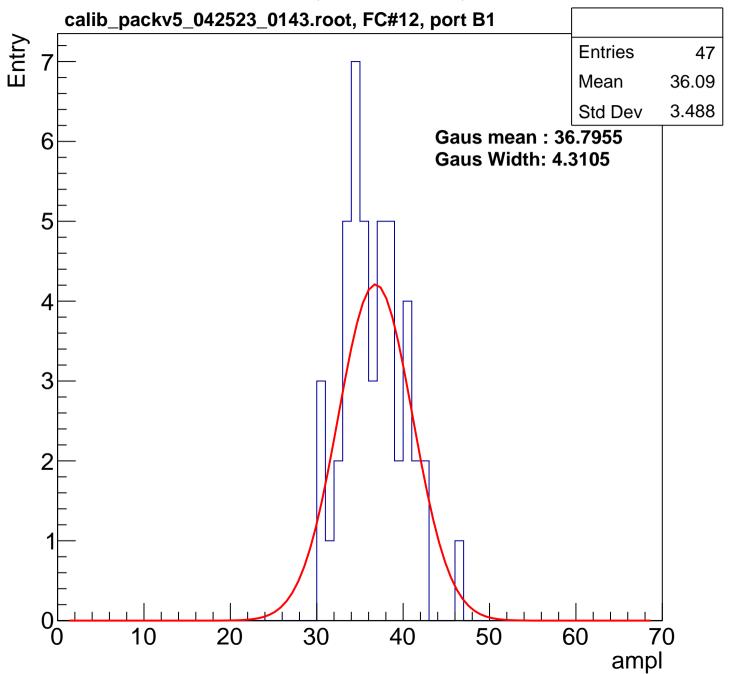


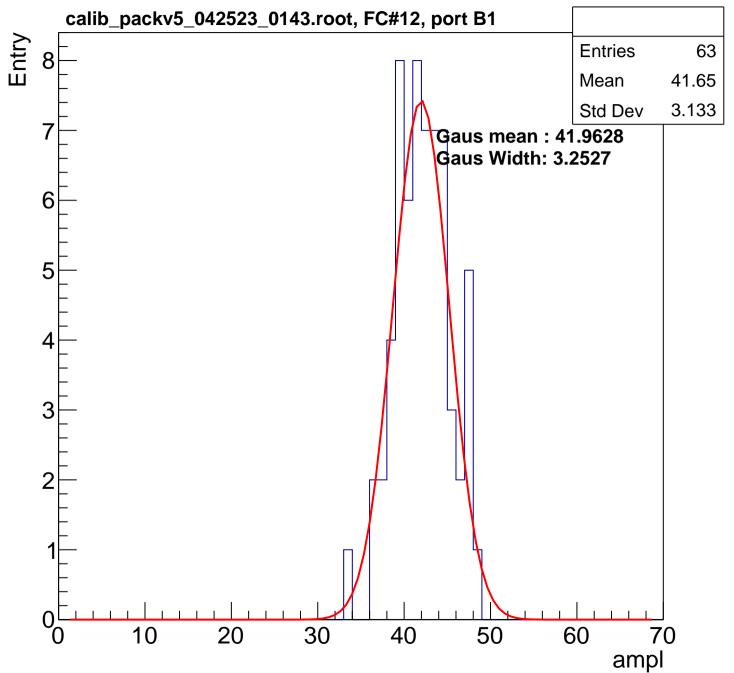


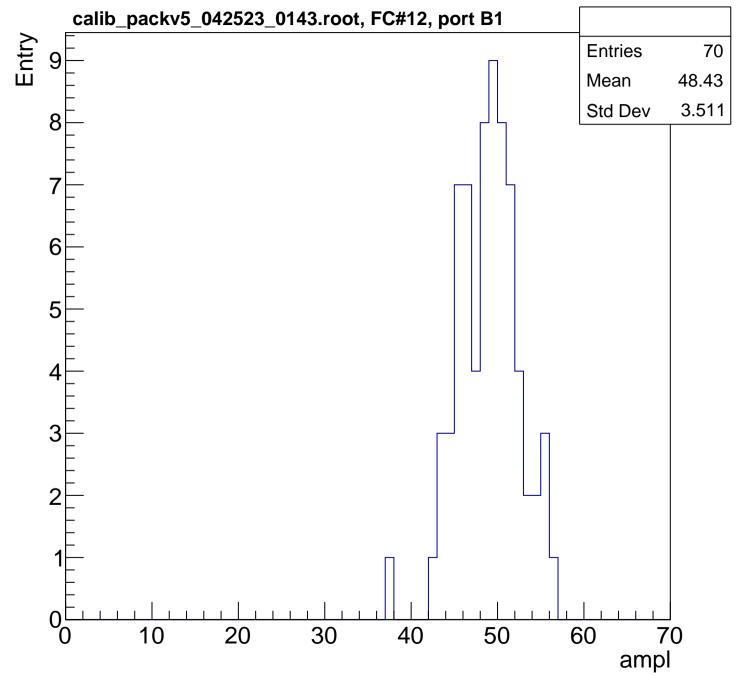


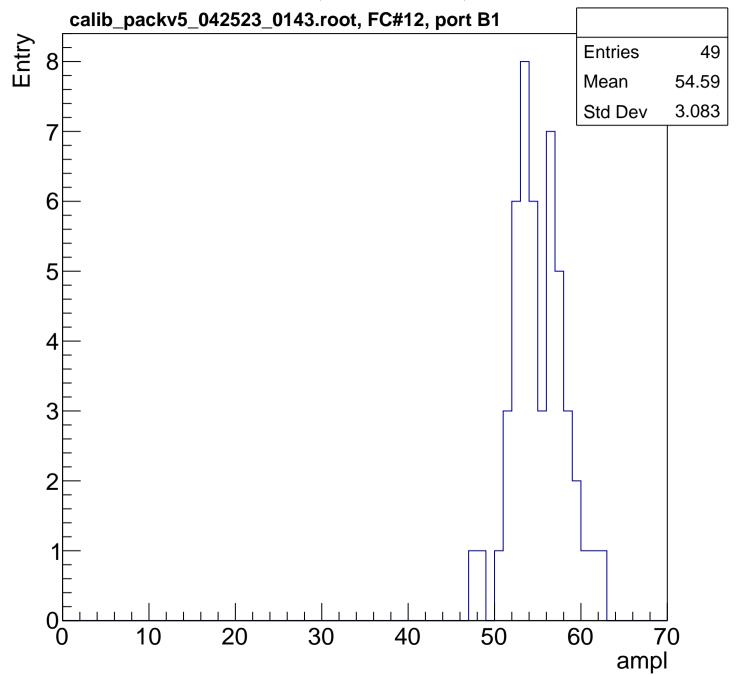


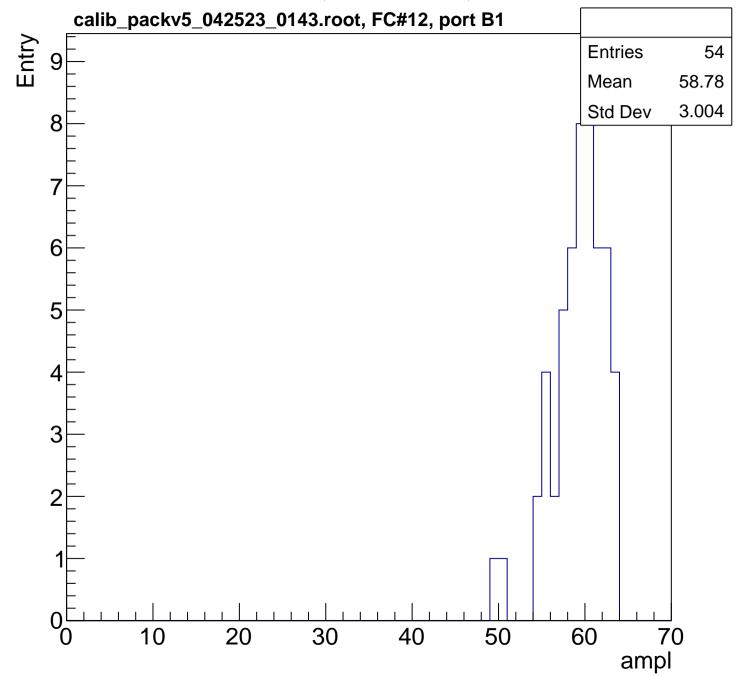


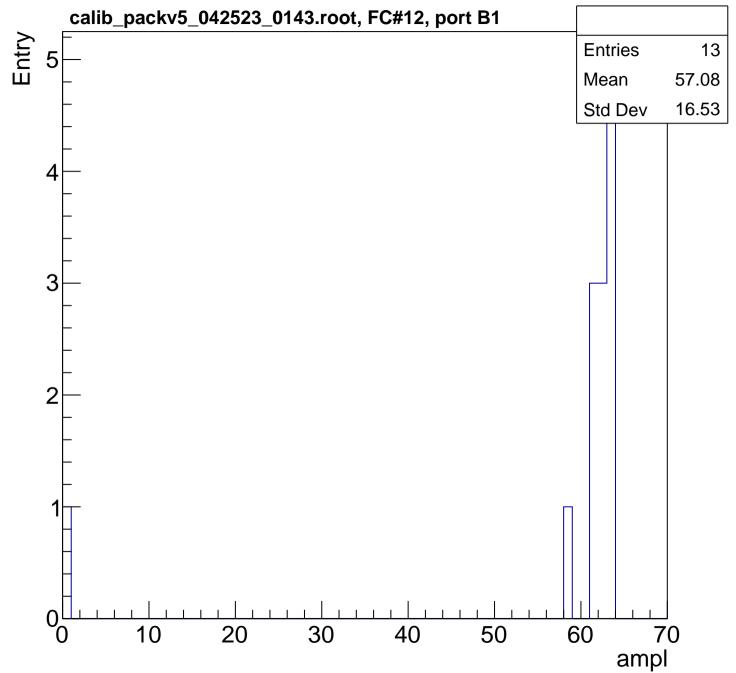


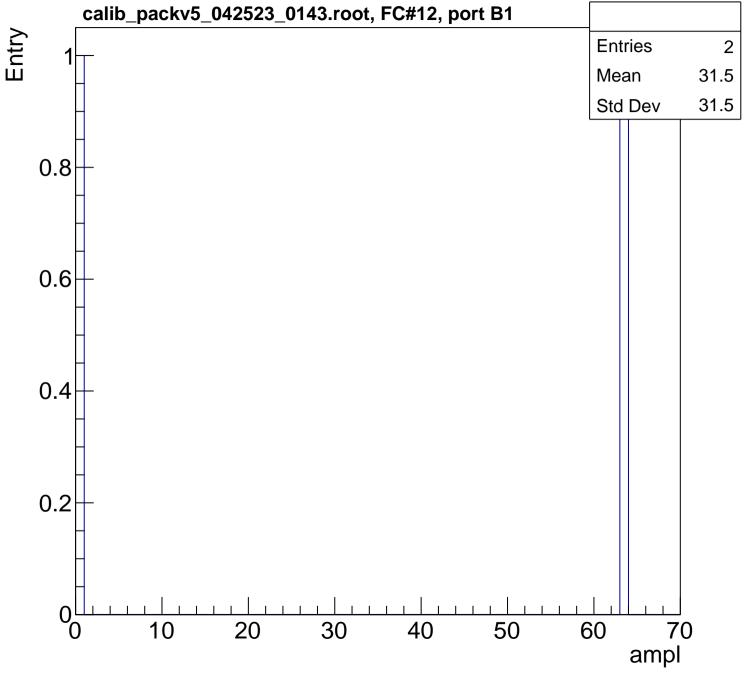


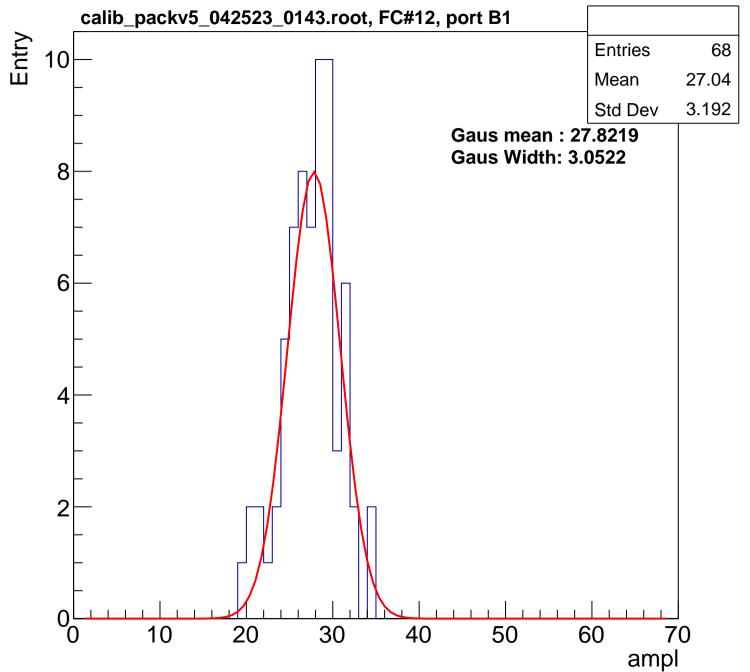


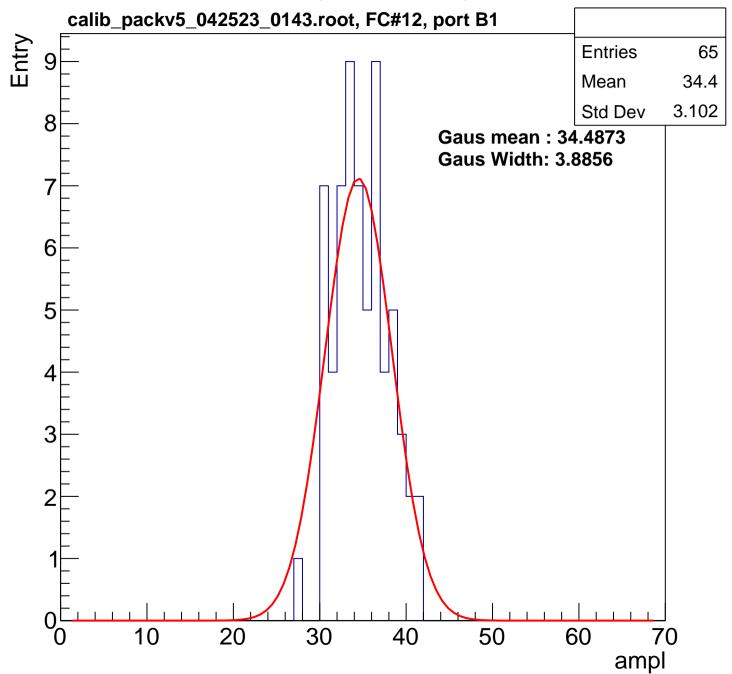


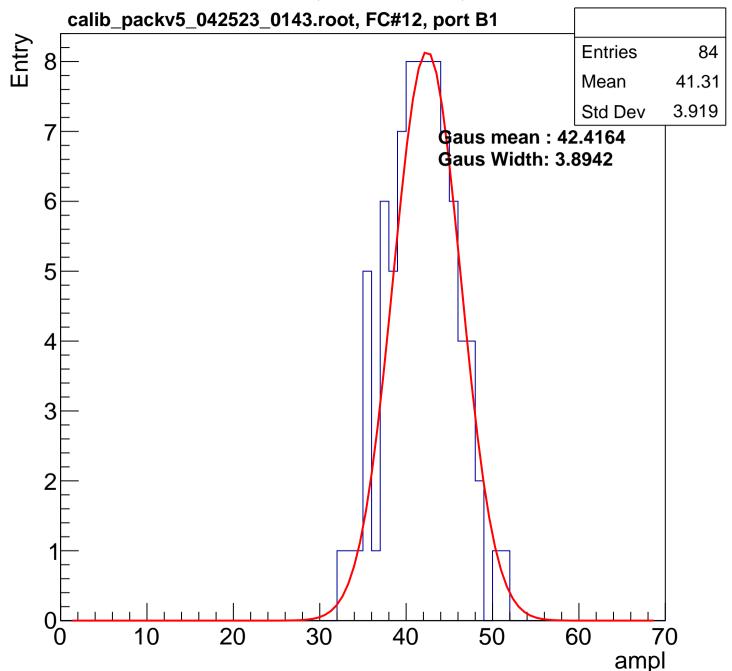


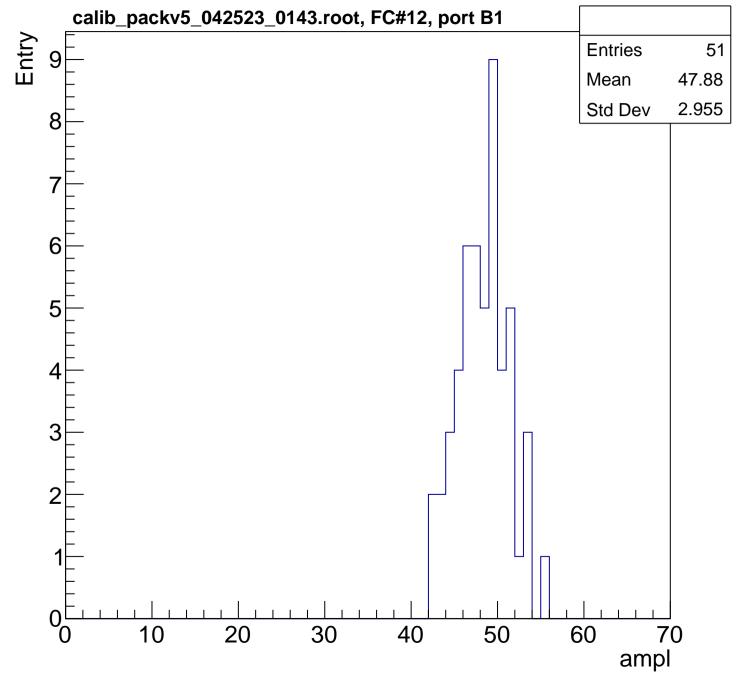


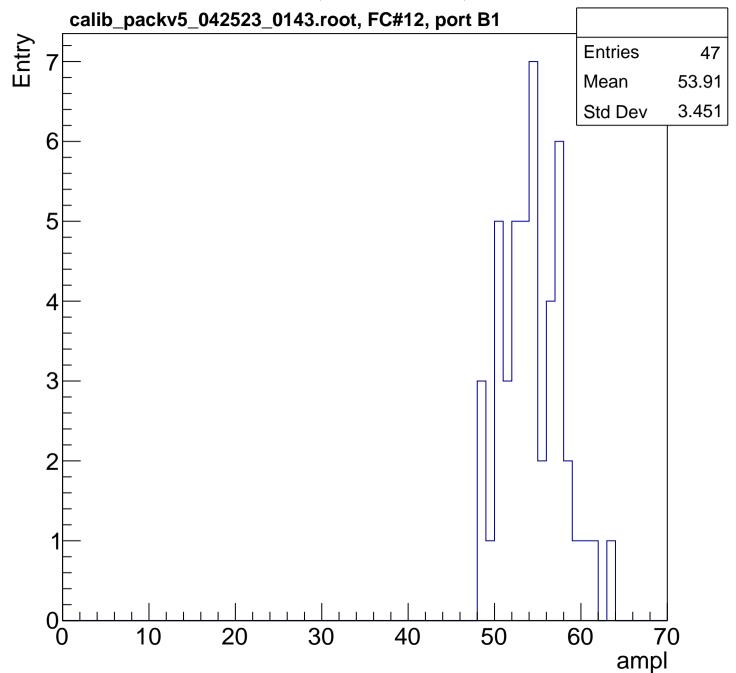


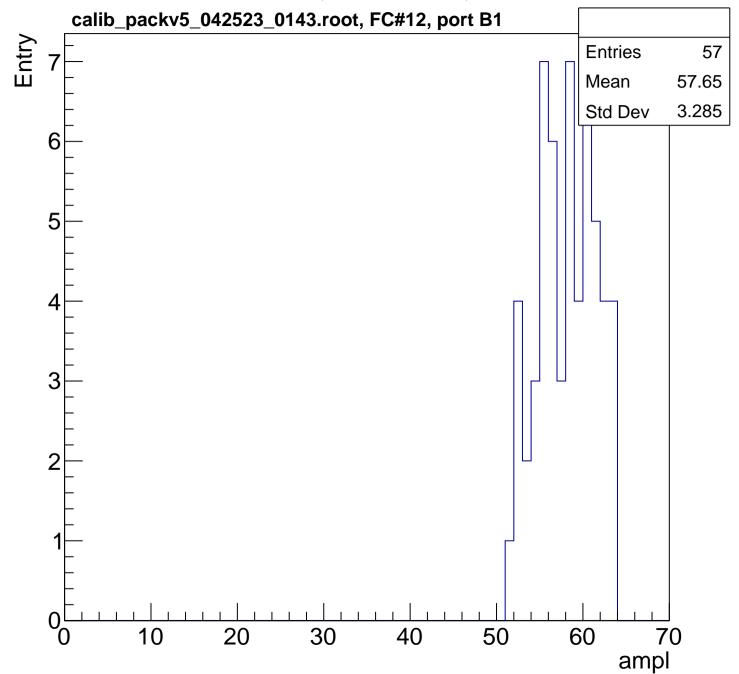


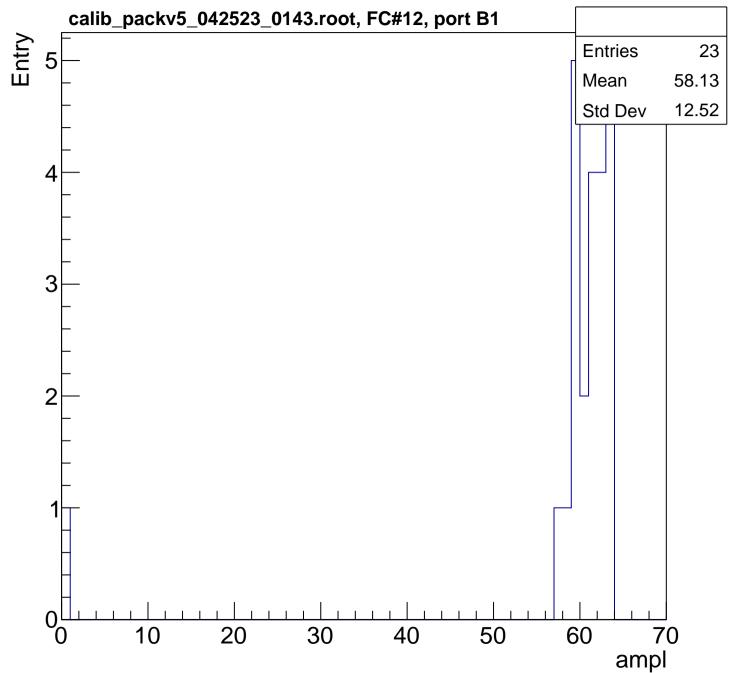


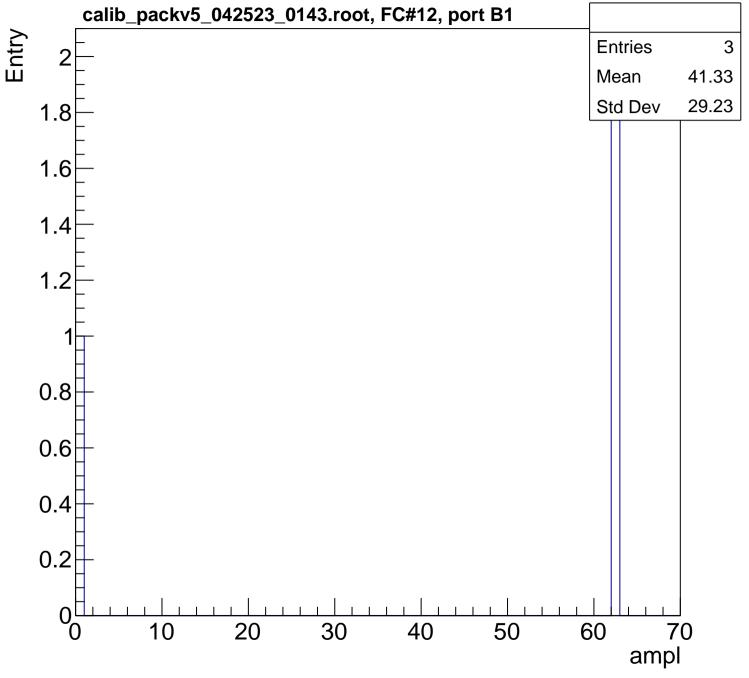


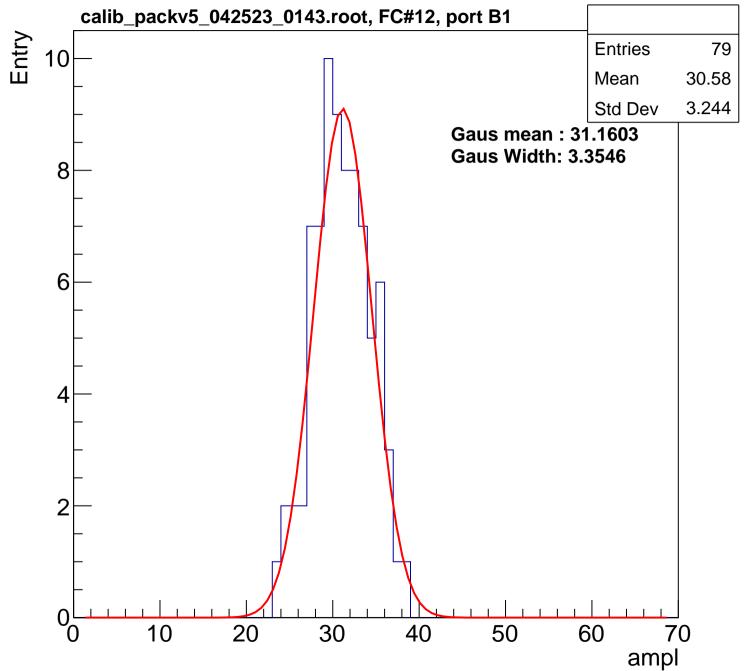


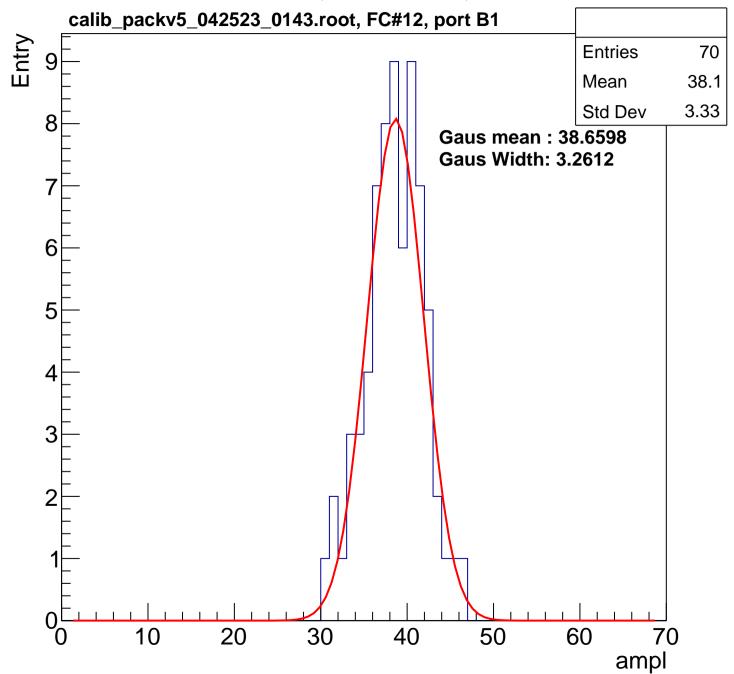


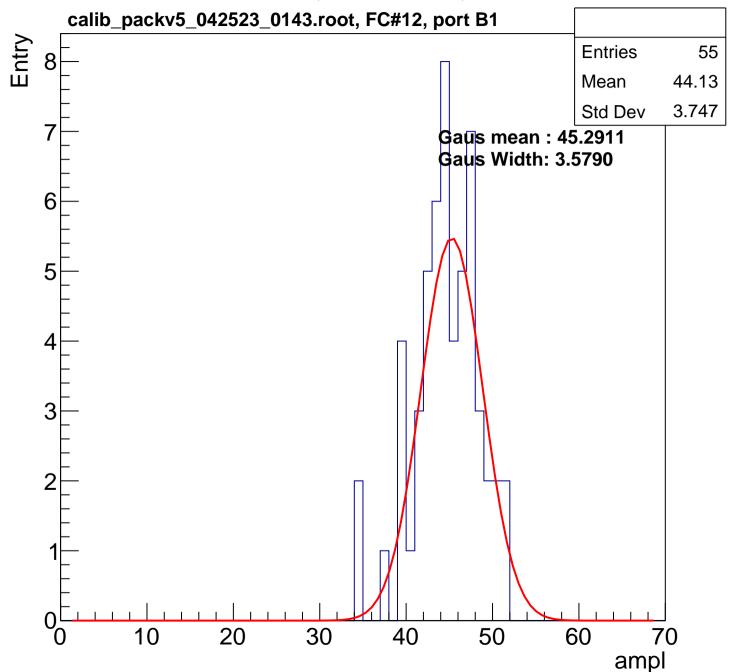


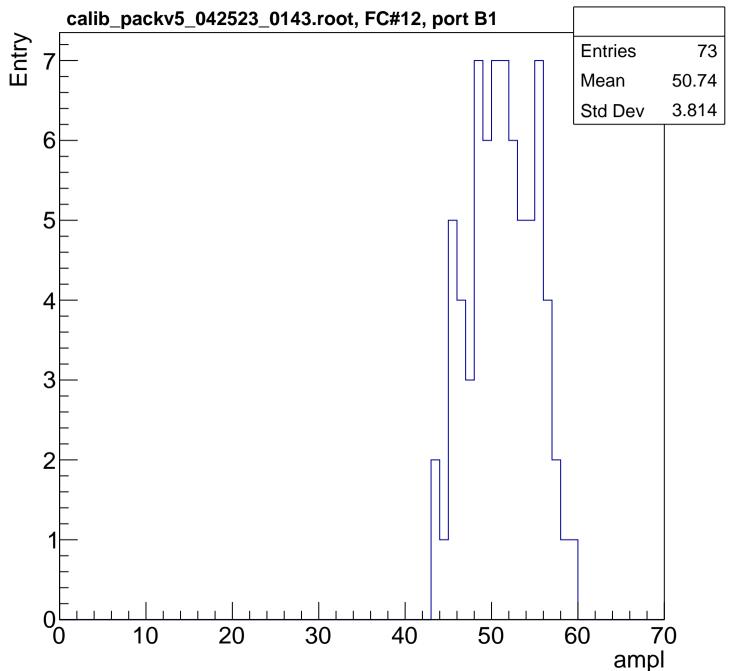


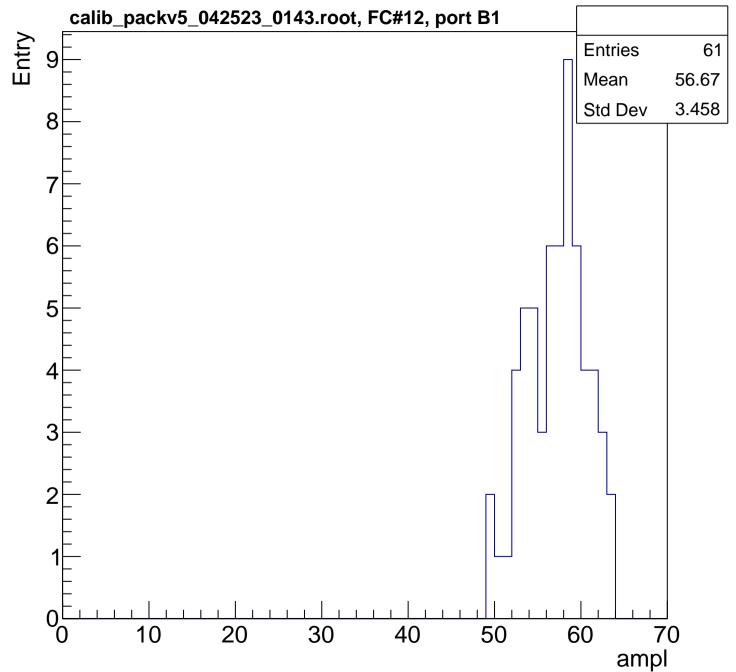


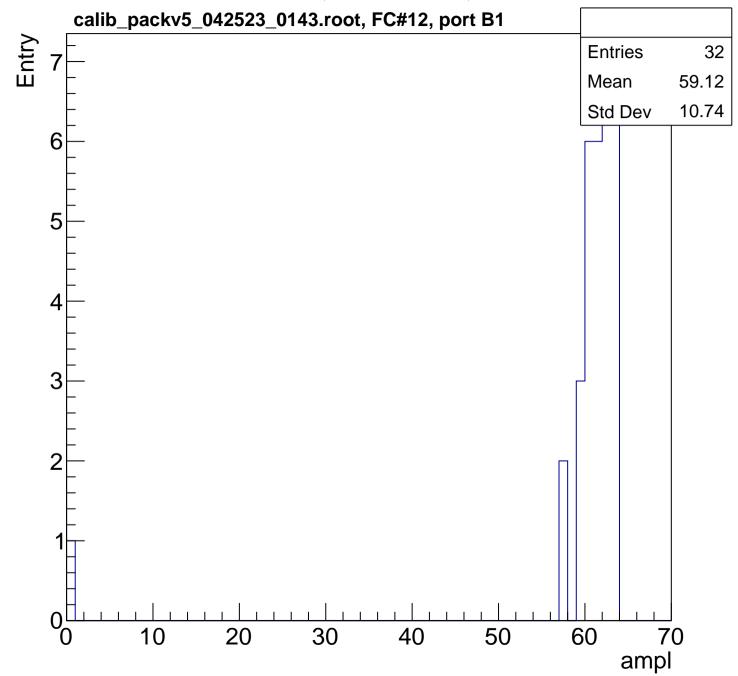


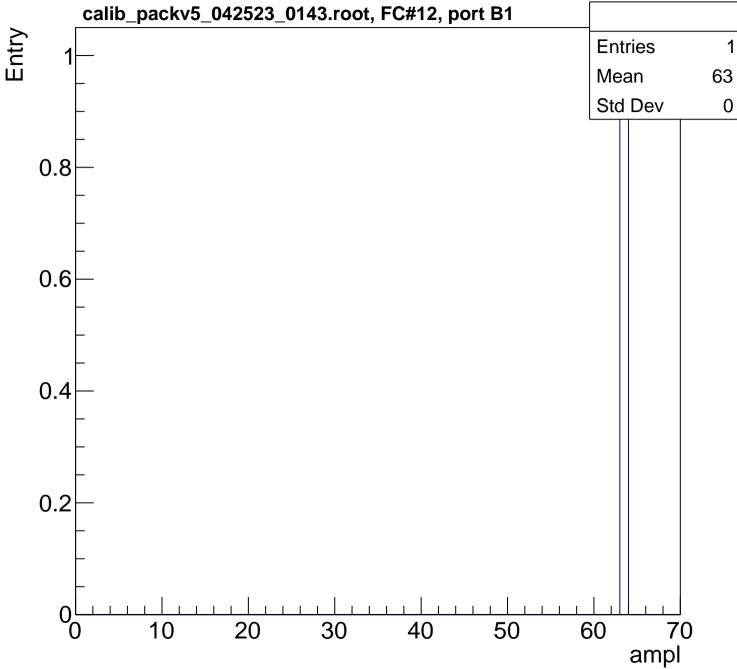




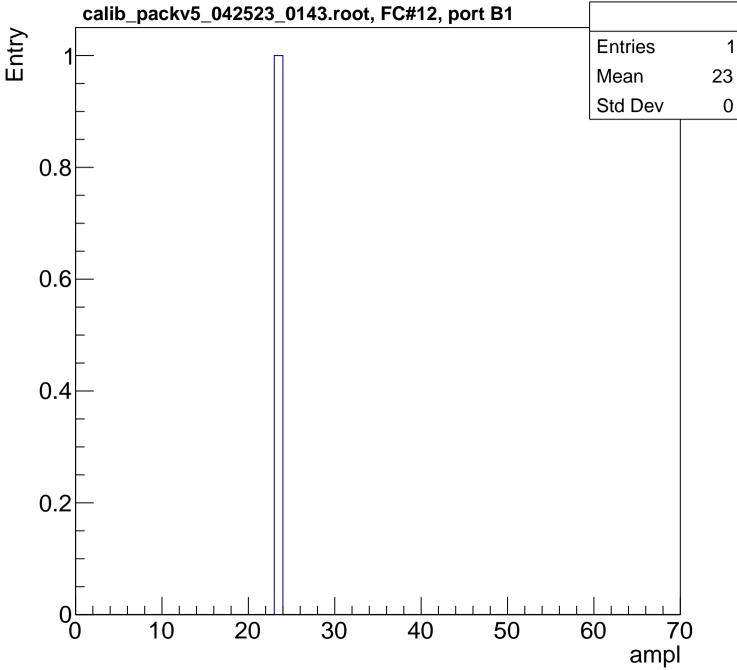


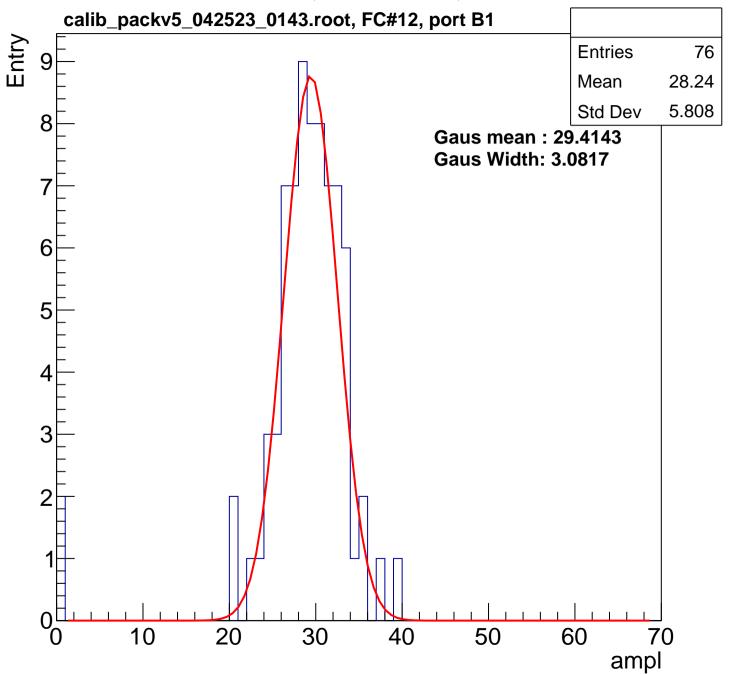


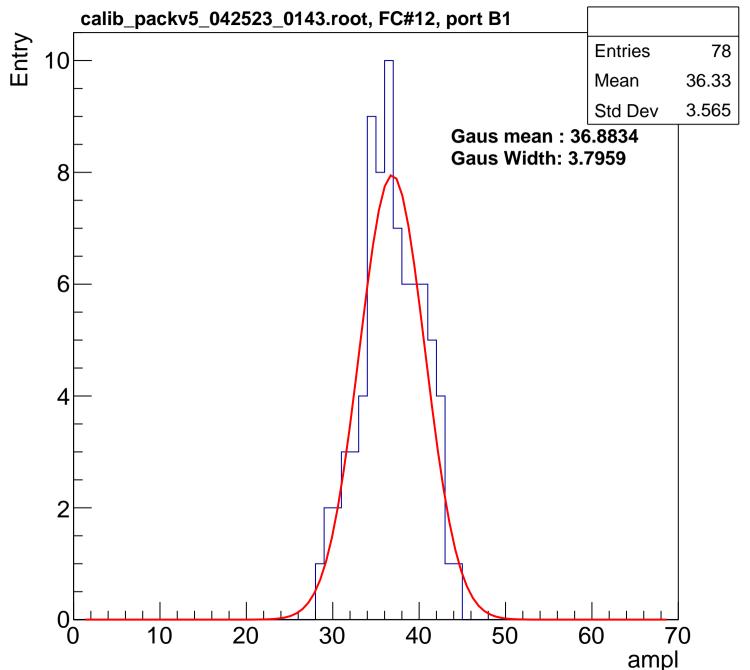


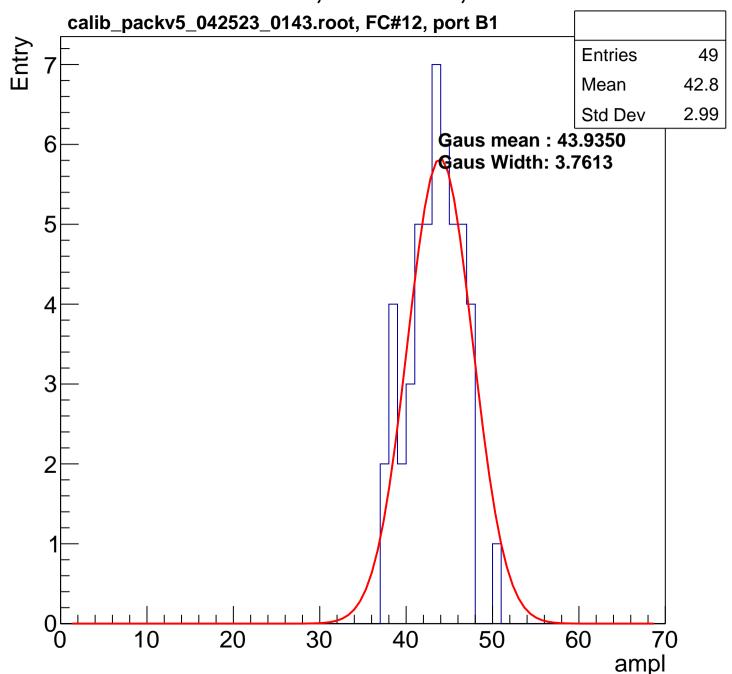


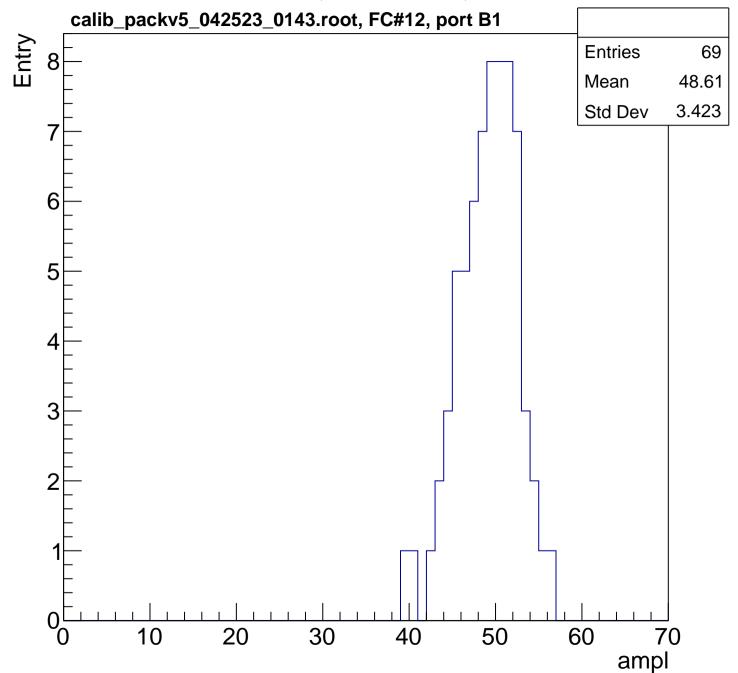
0

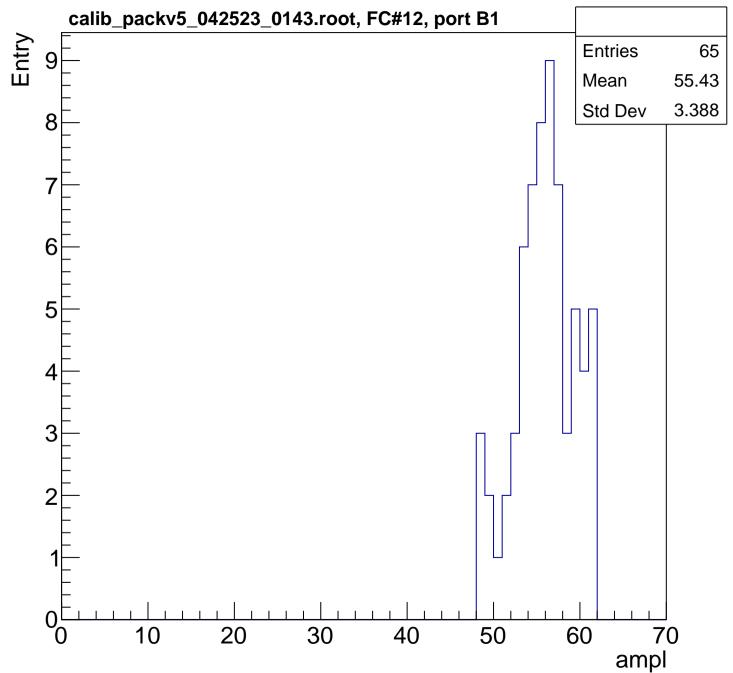


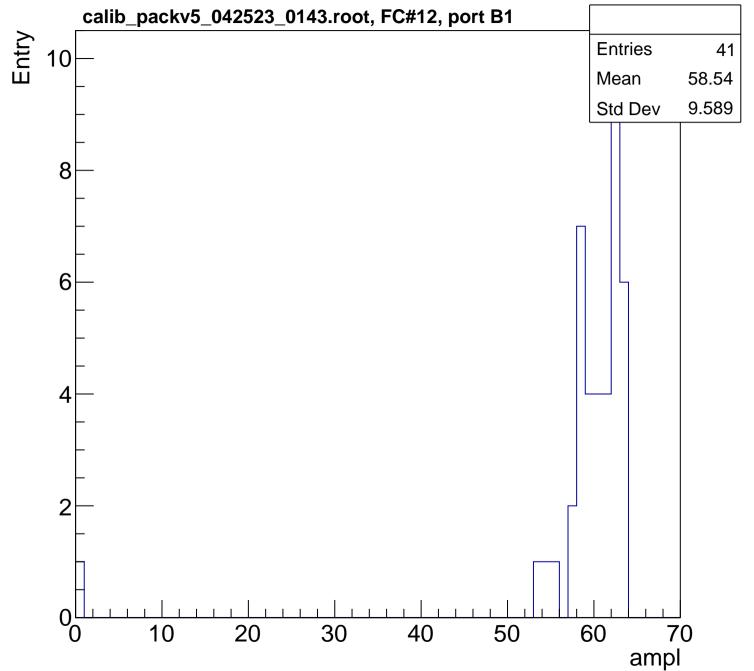


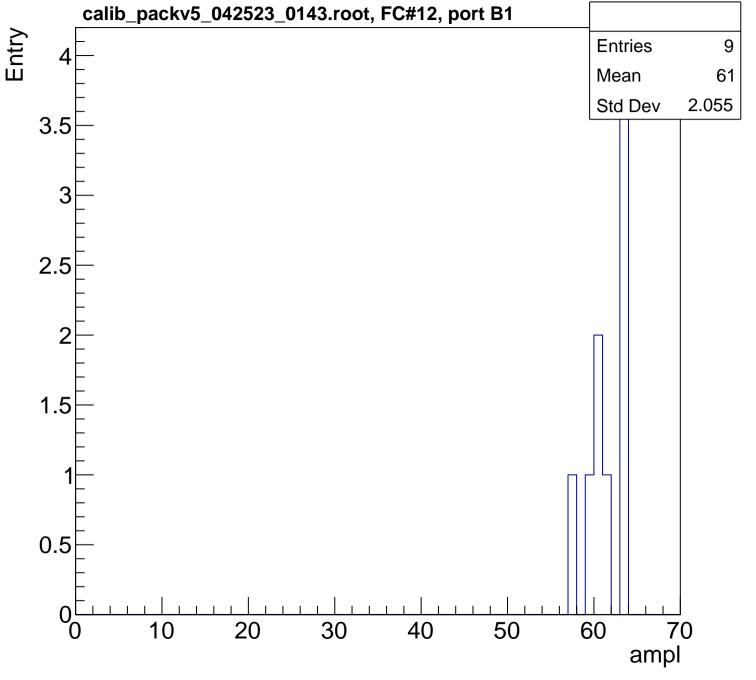




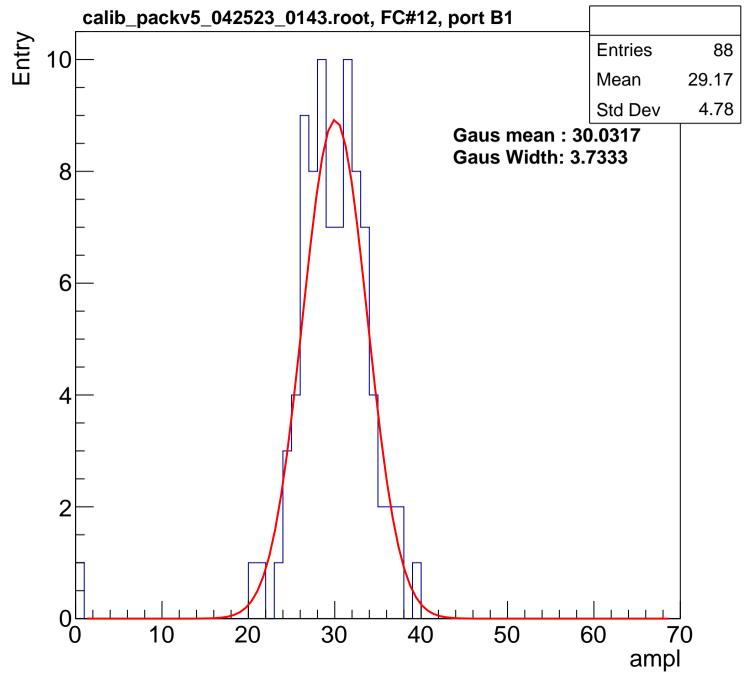


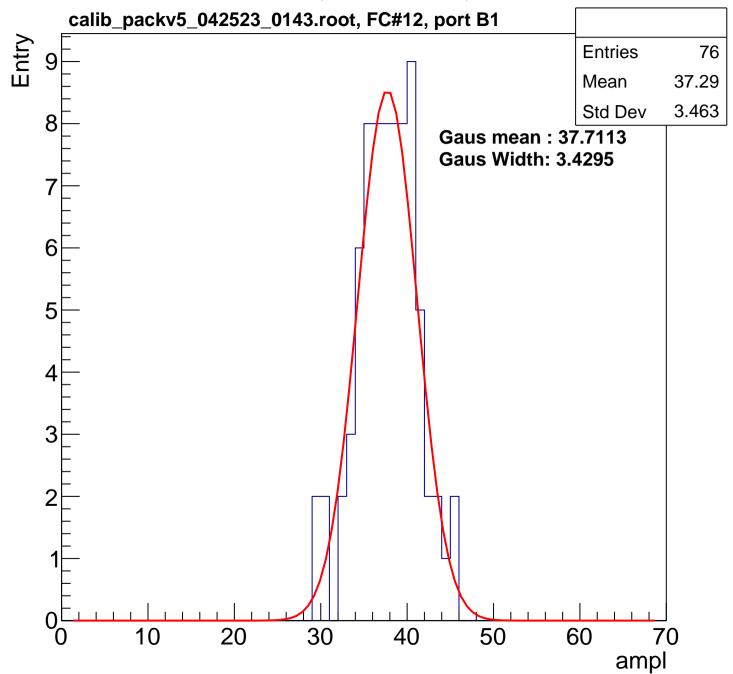


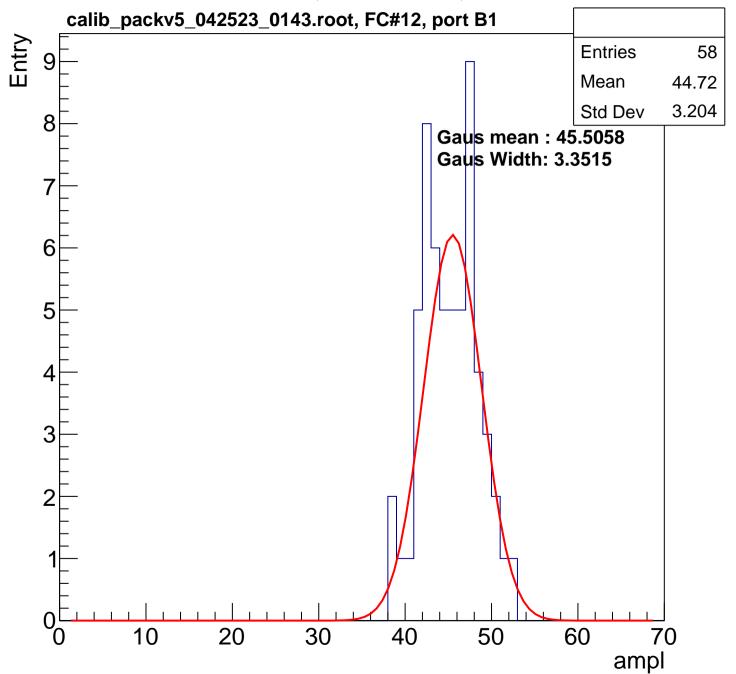


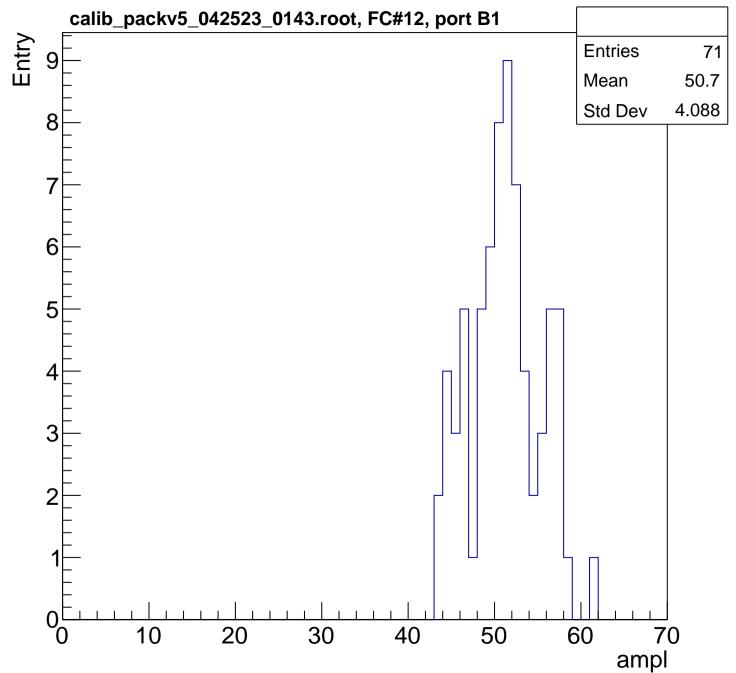


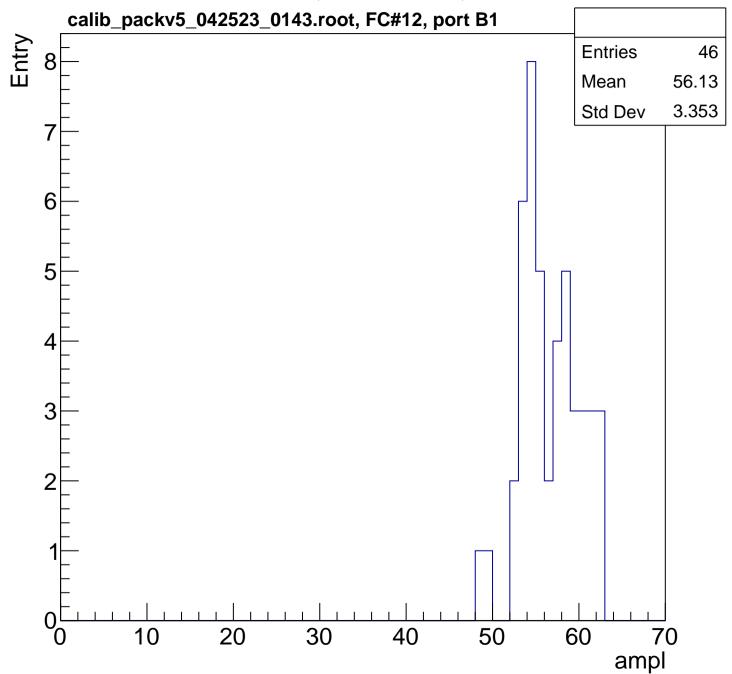


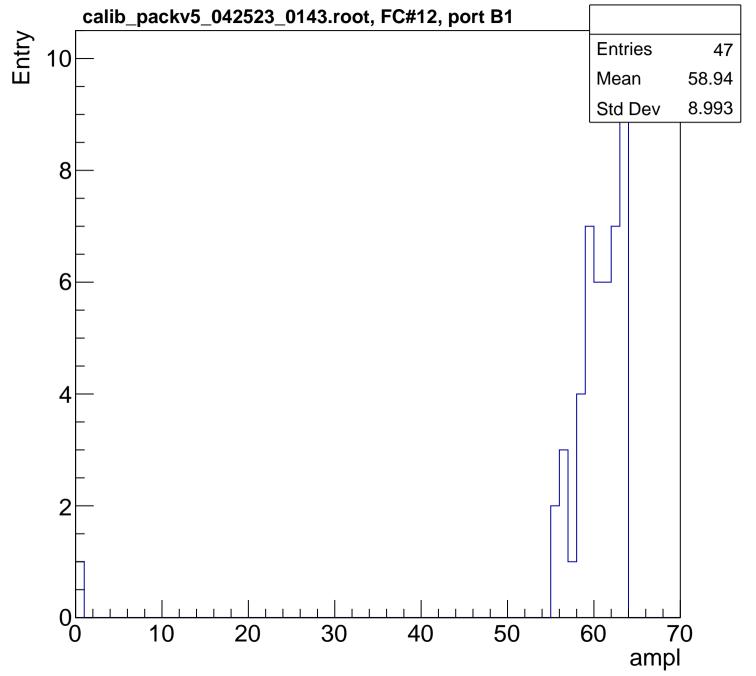




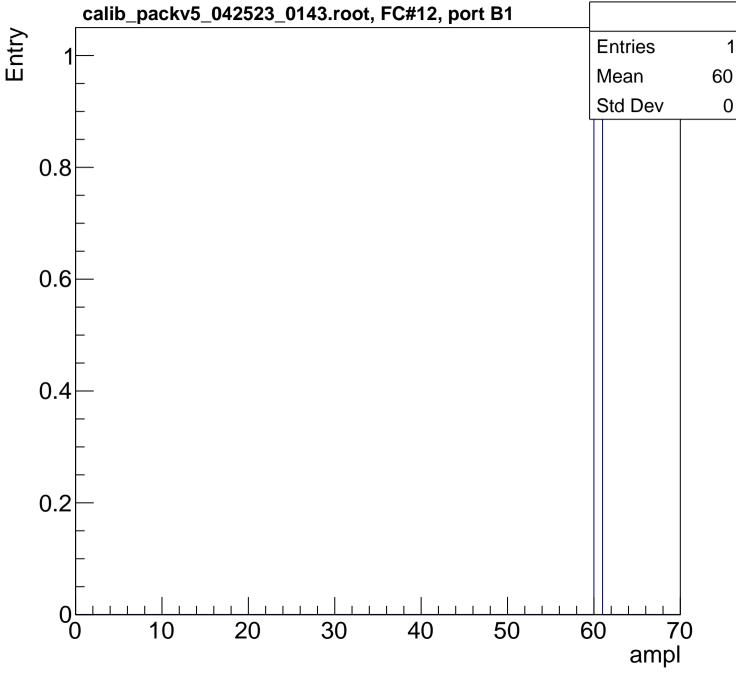


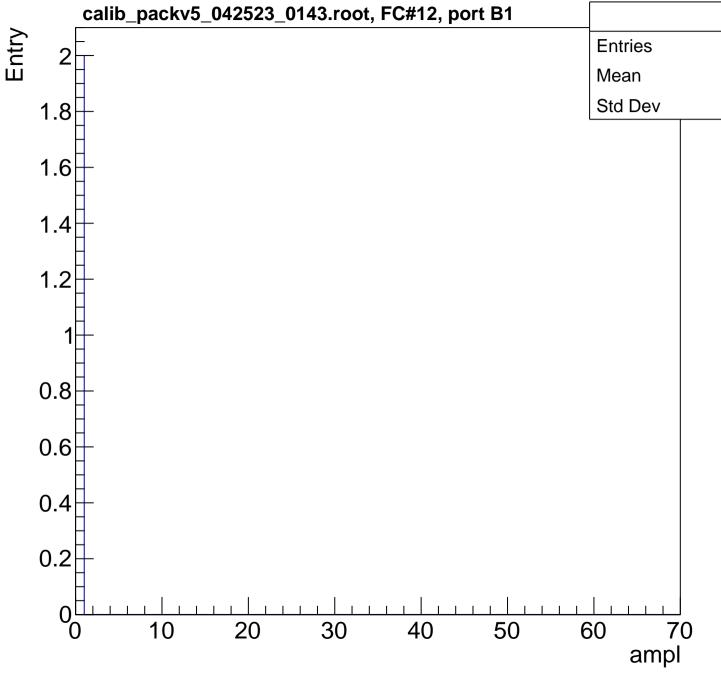


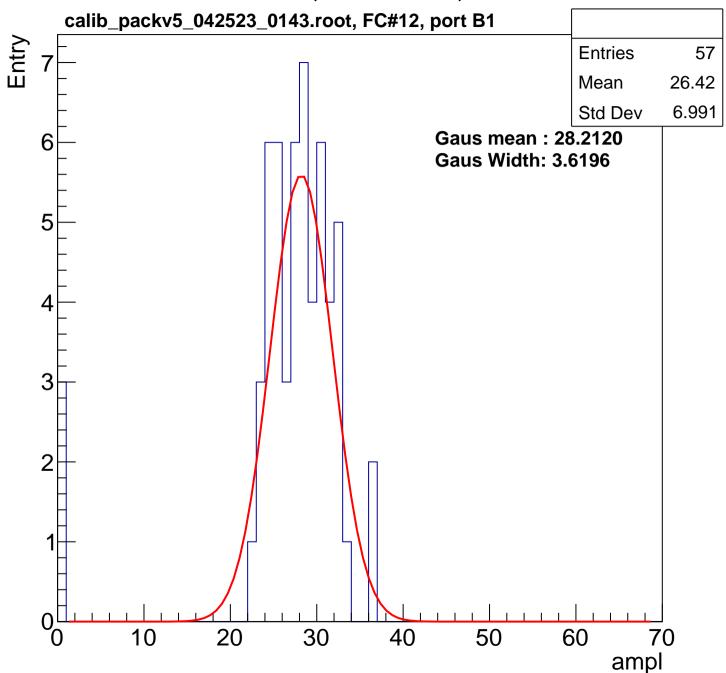


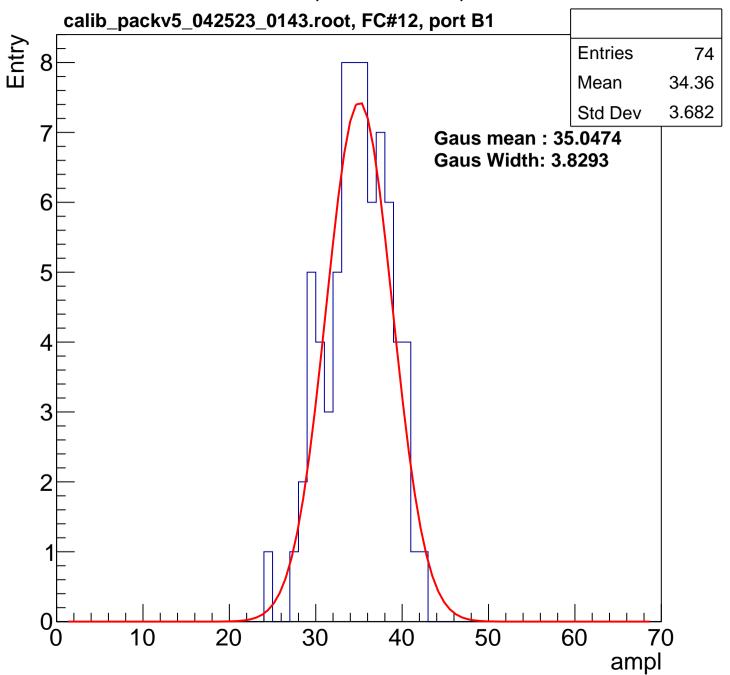


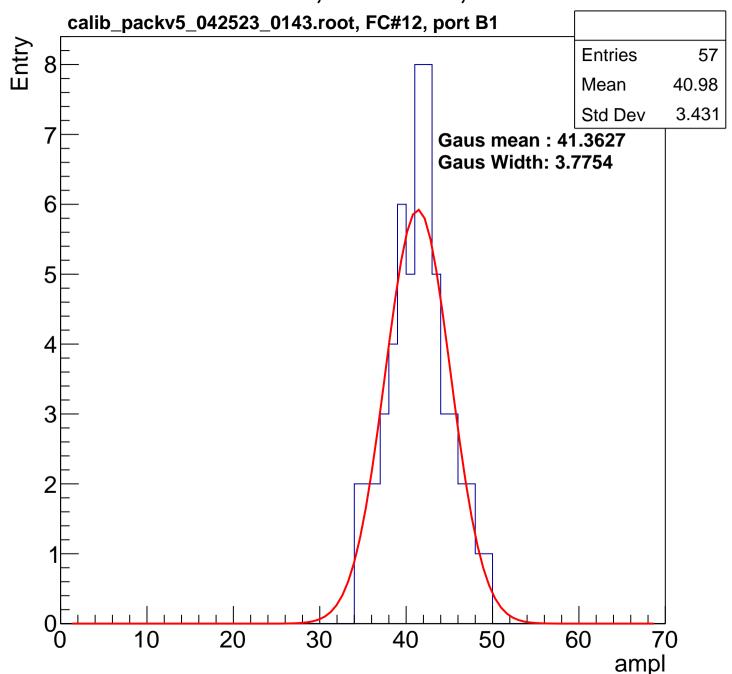
0

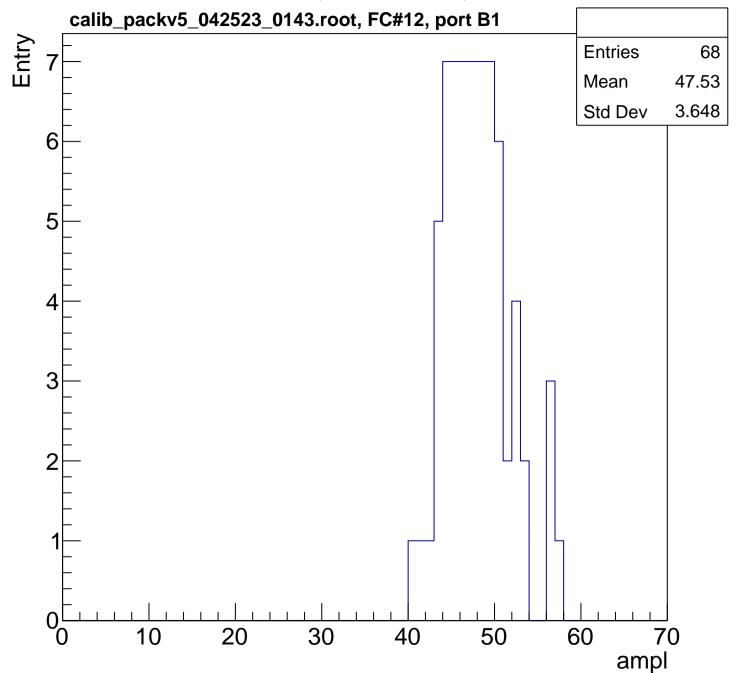


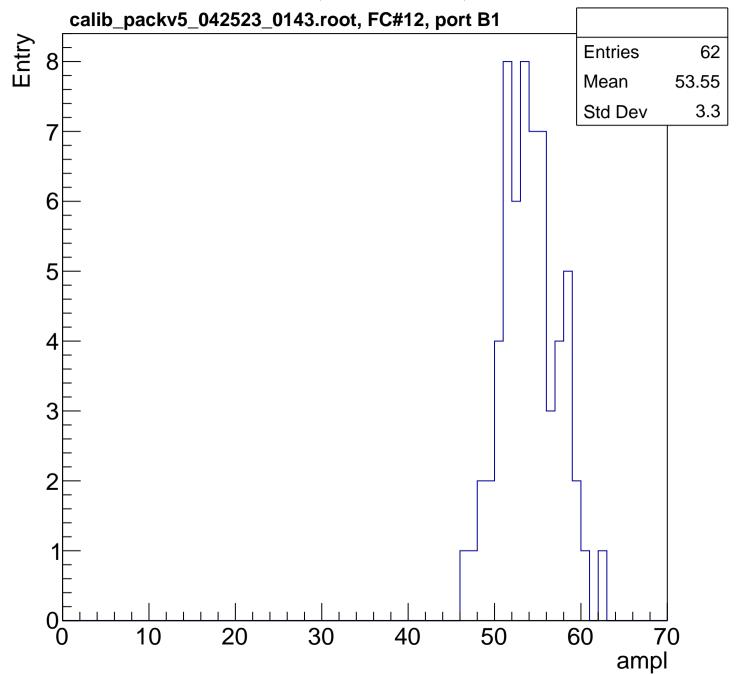


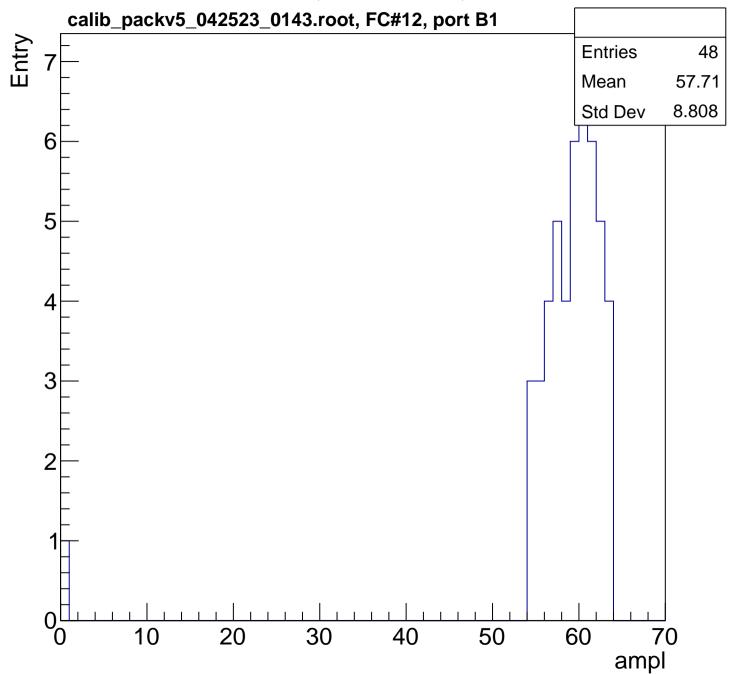


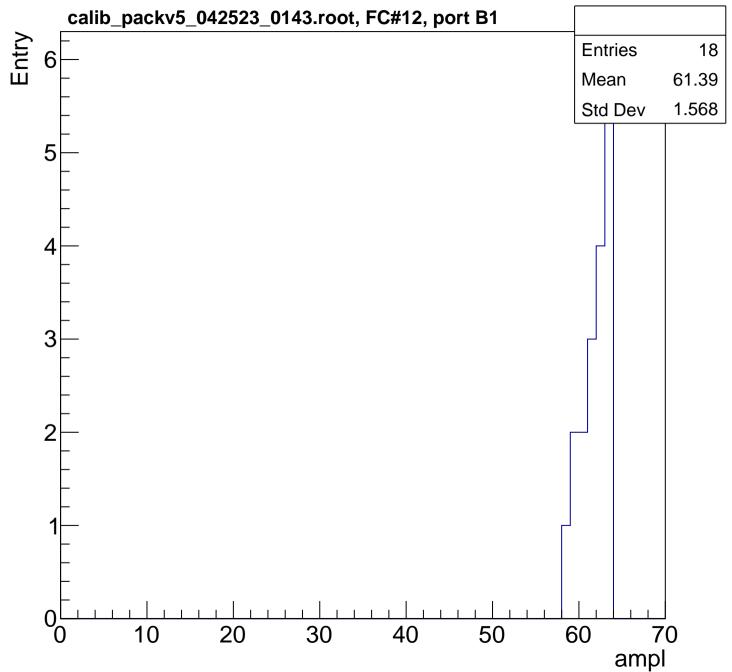


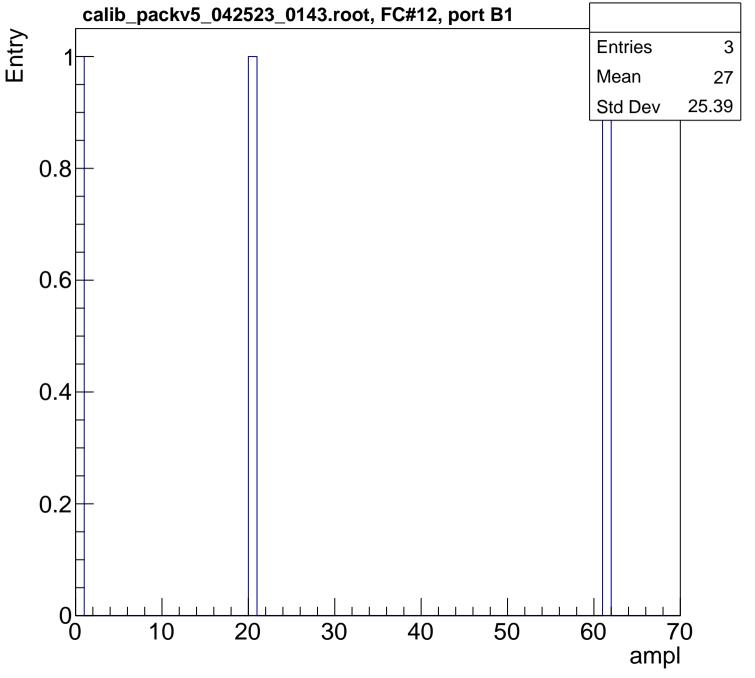


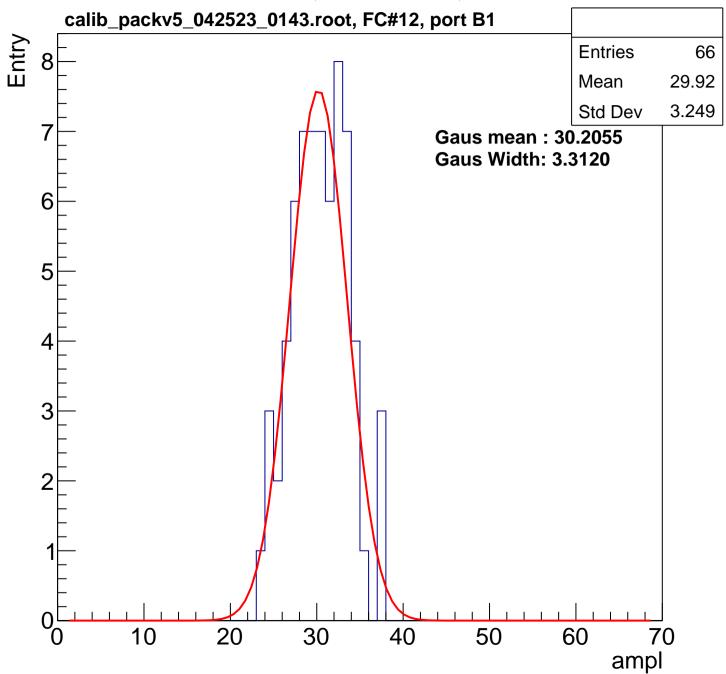


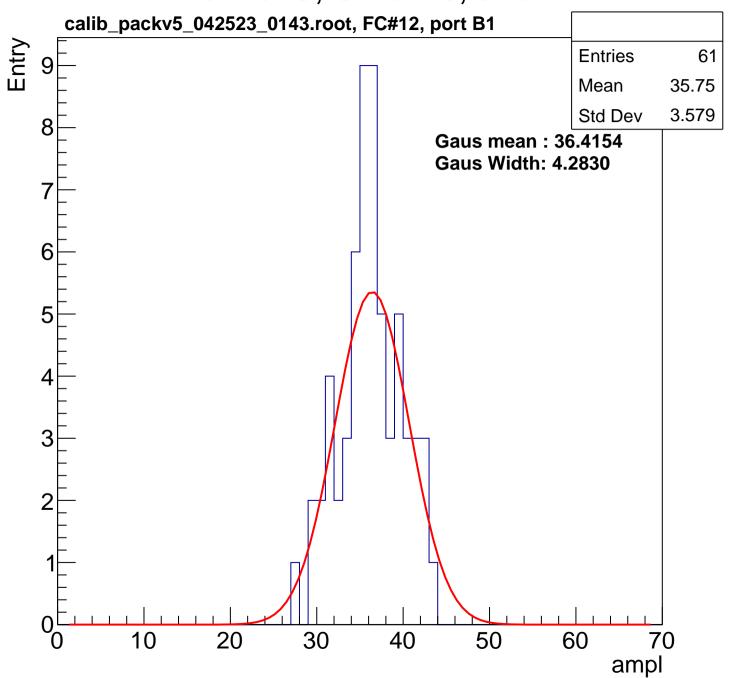


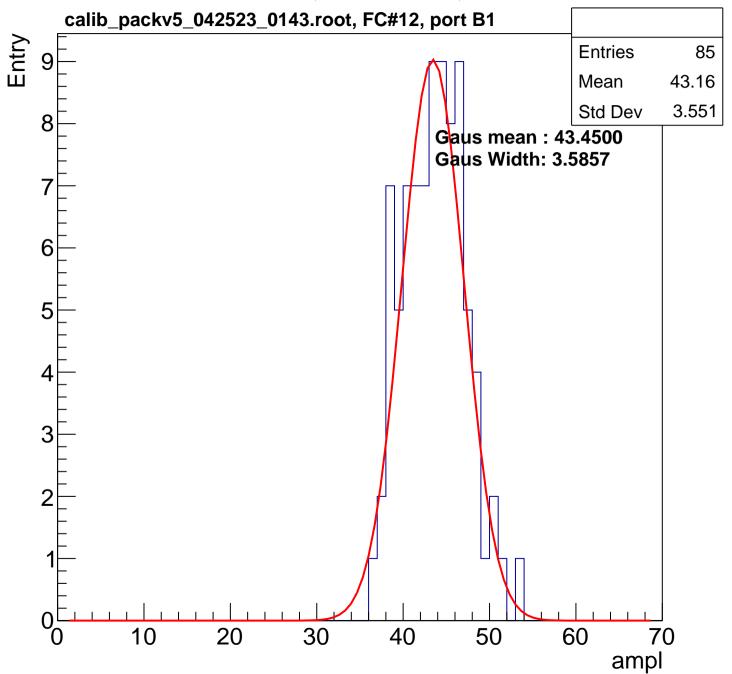


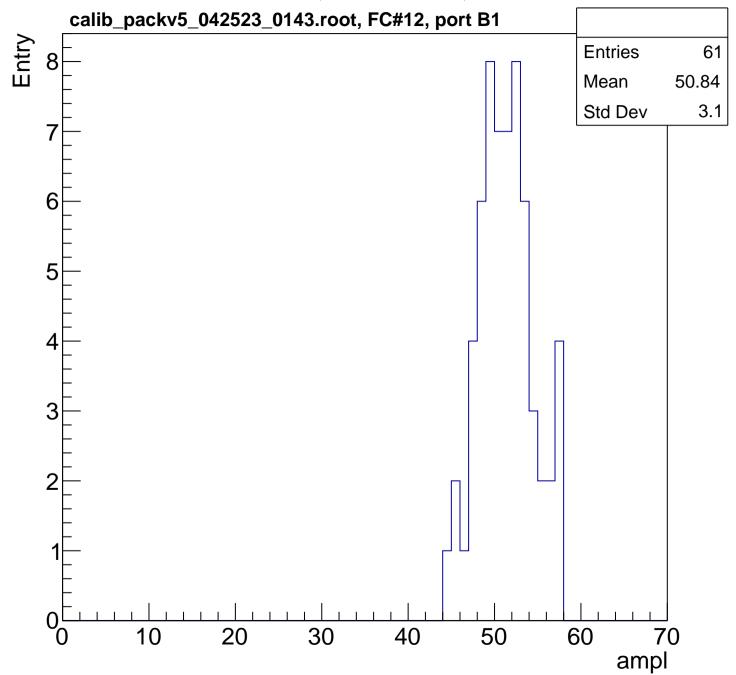


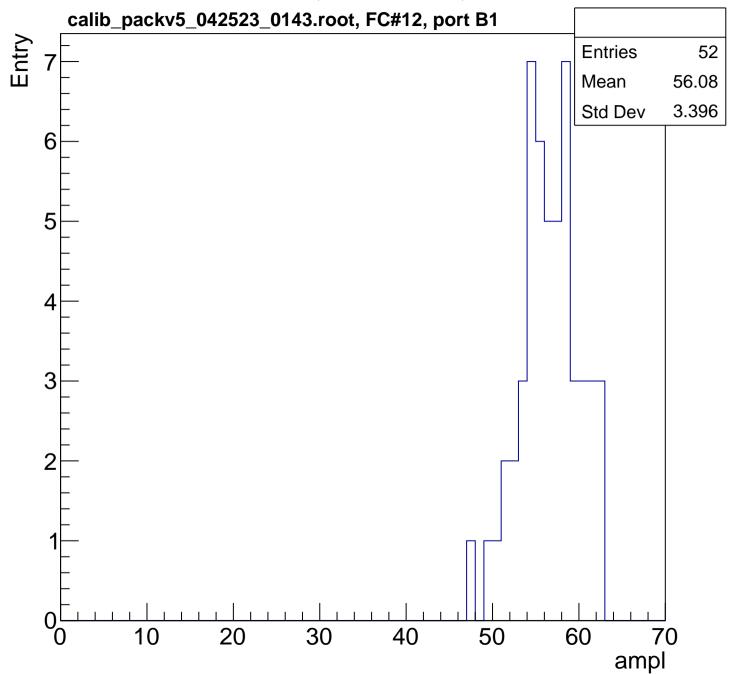


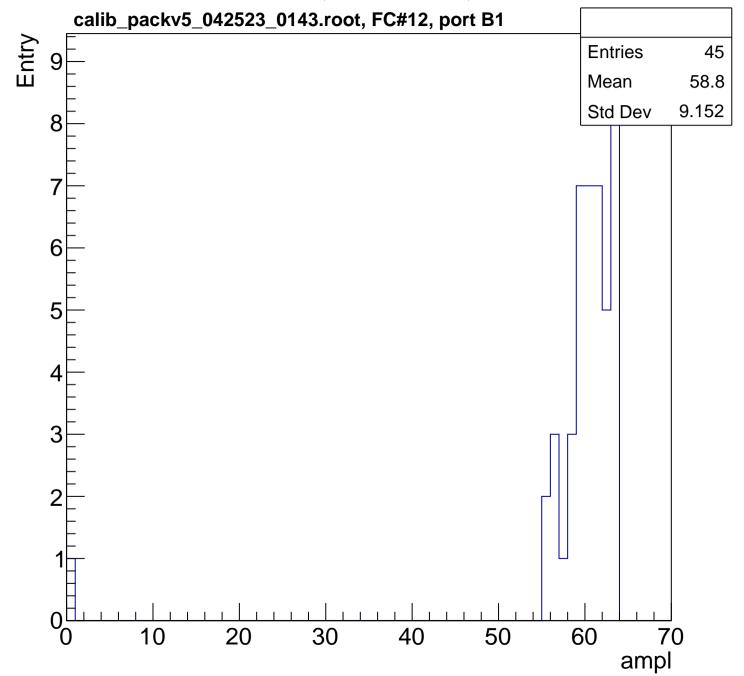


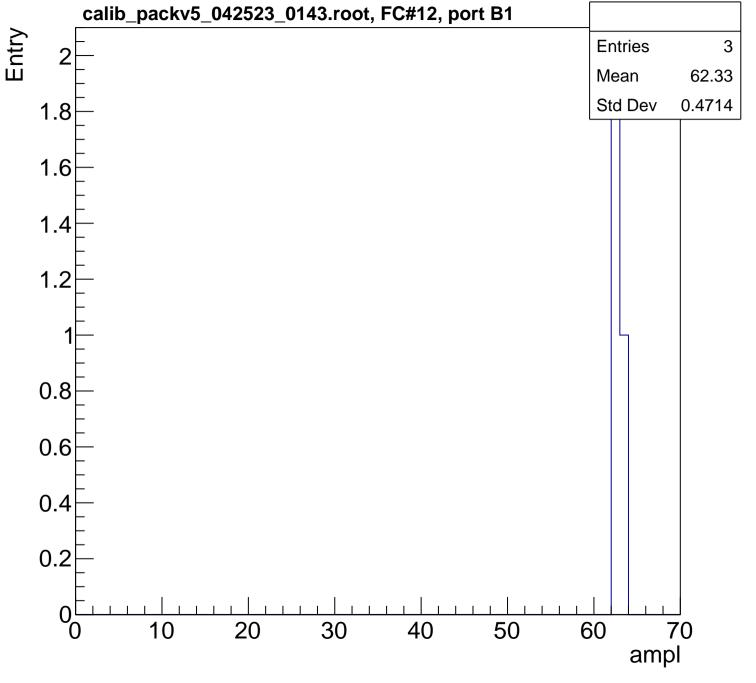


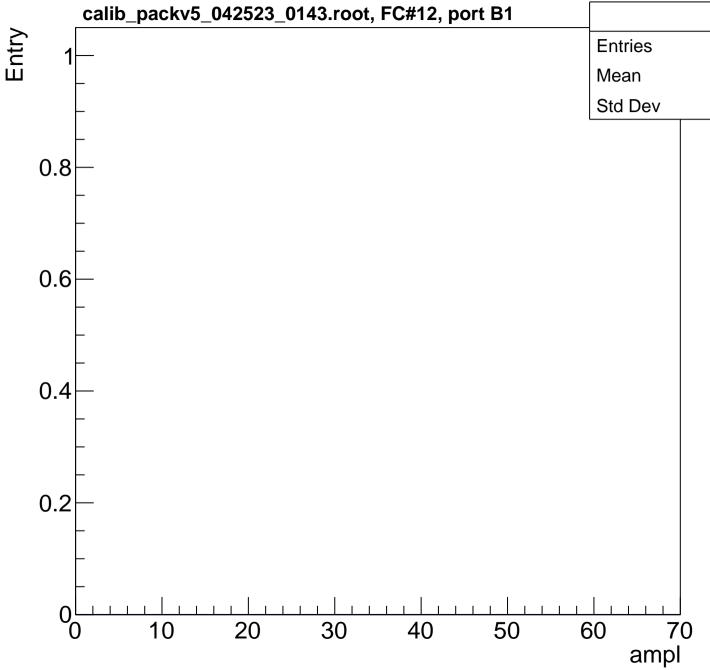


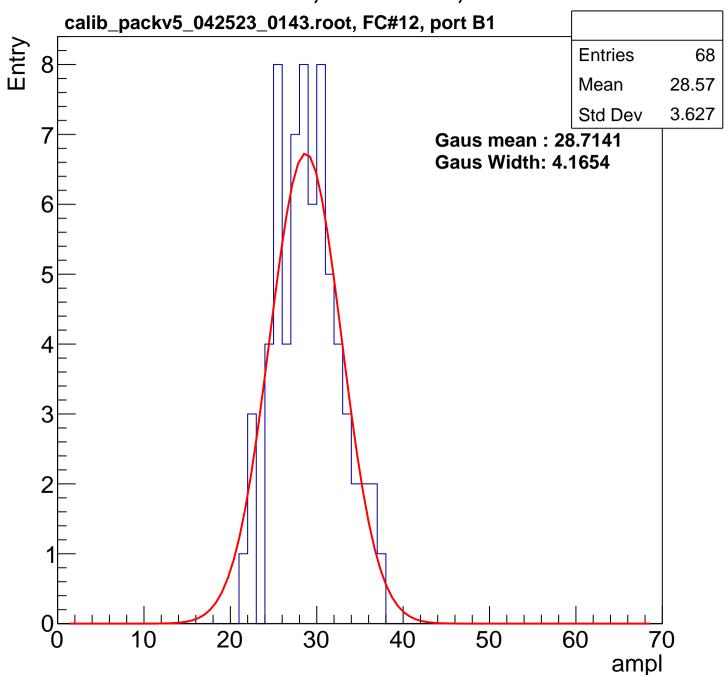


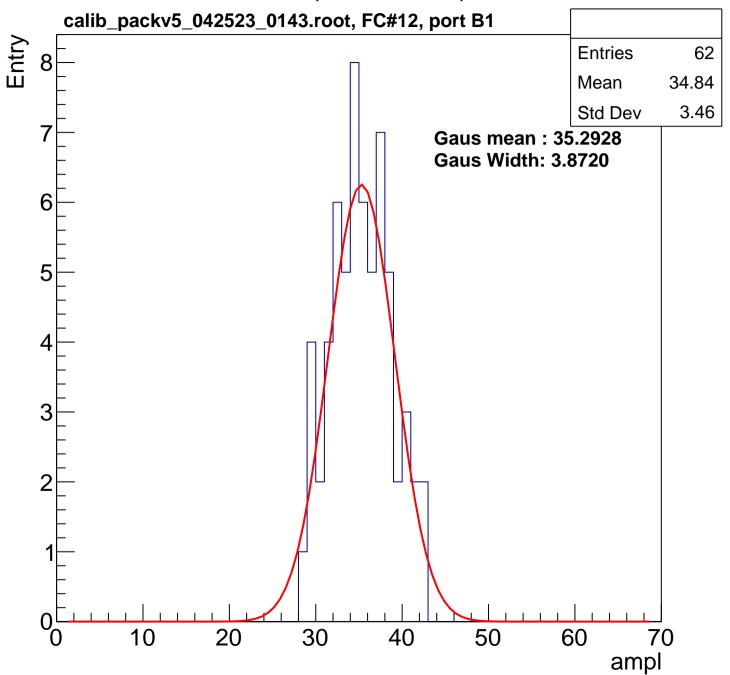


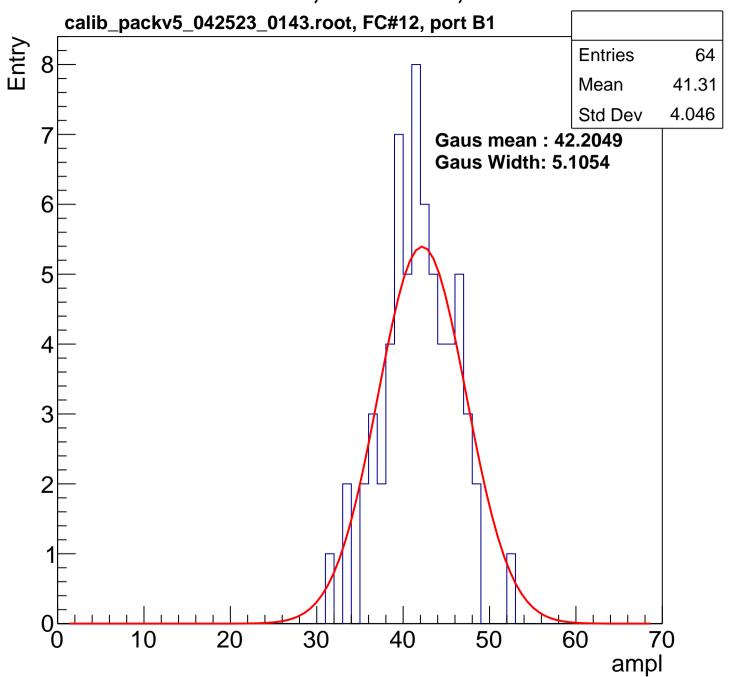


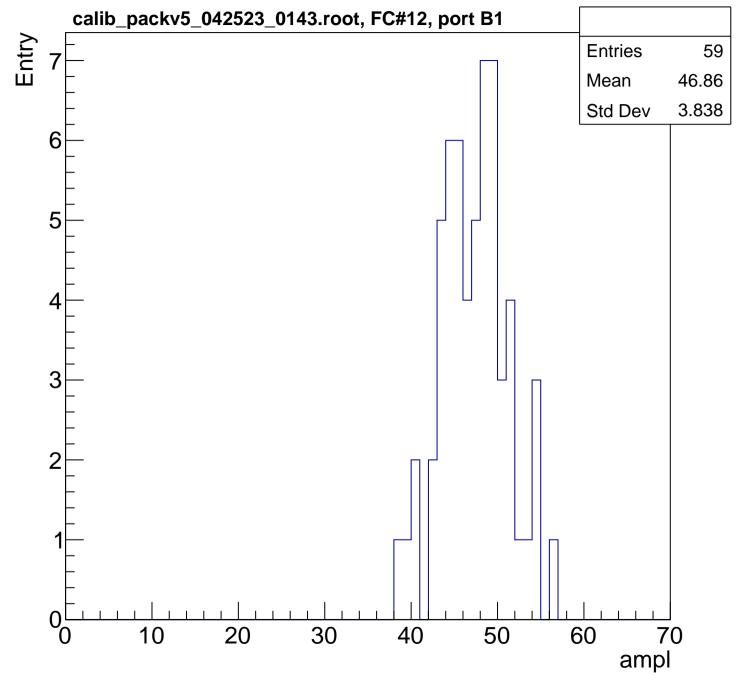


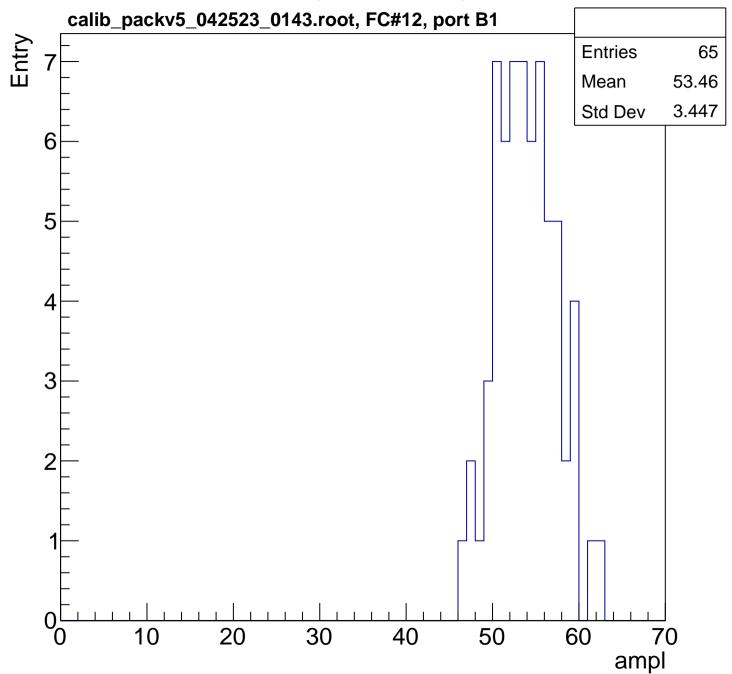


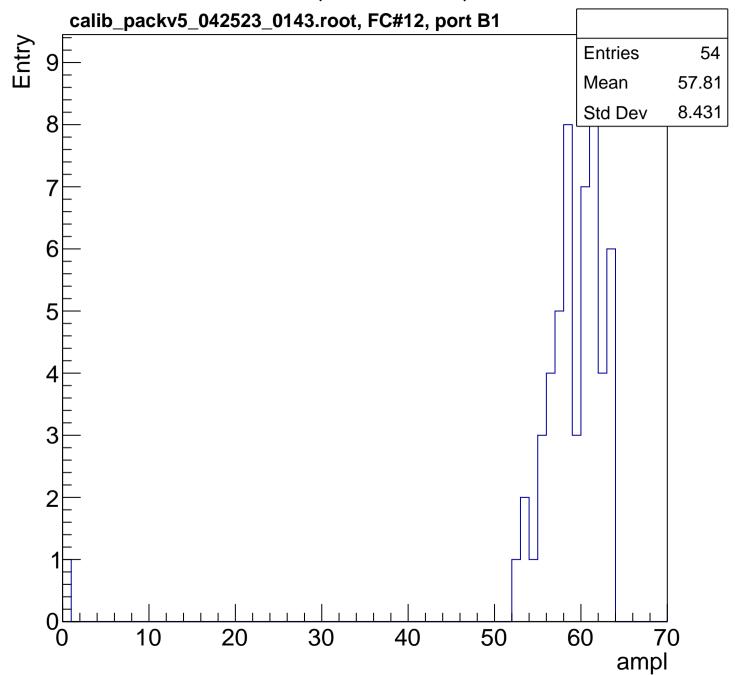


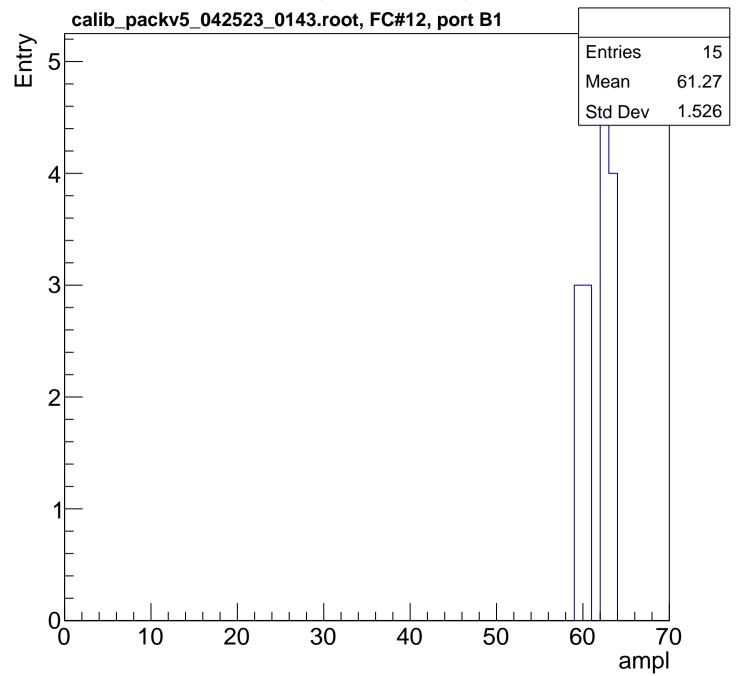


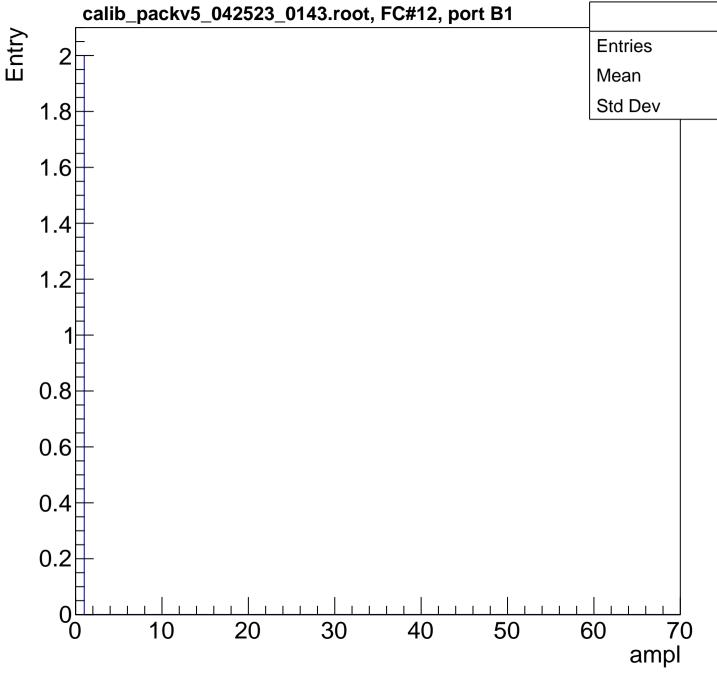


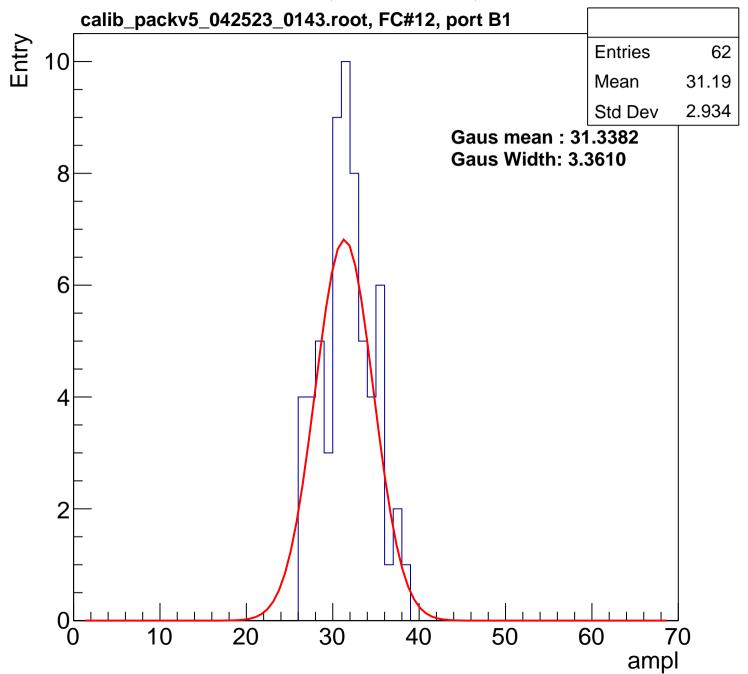


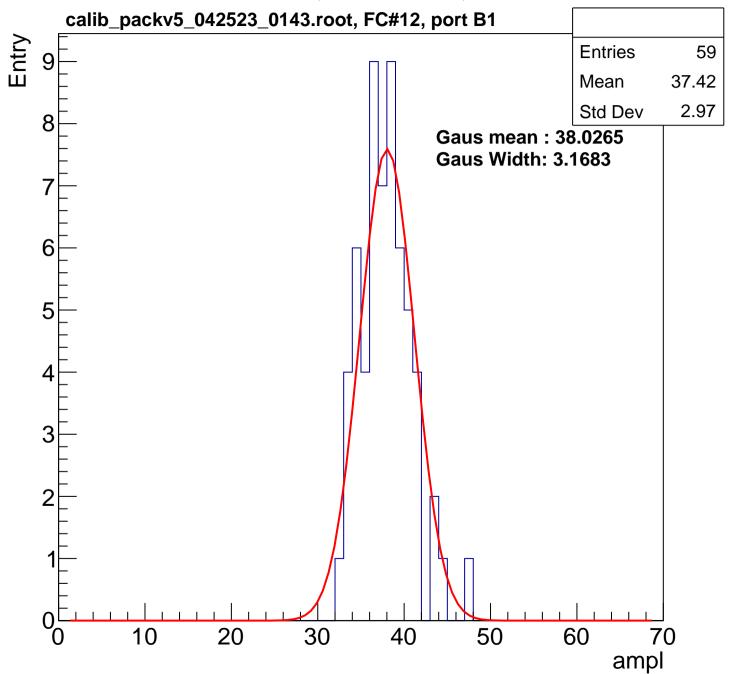


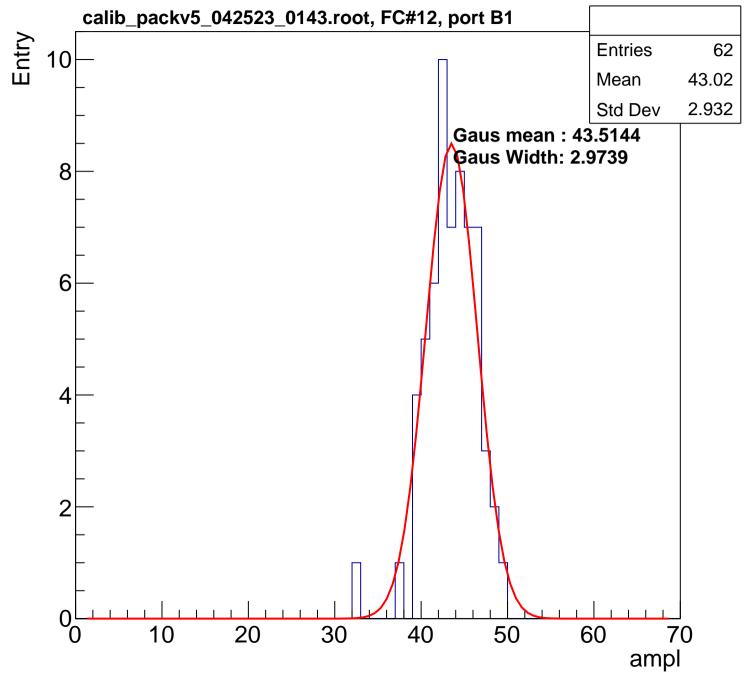


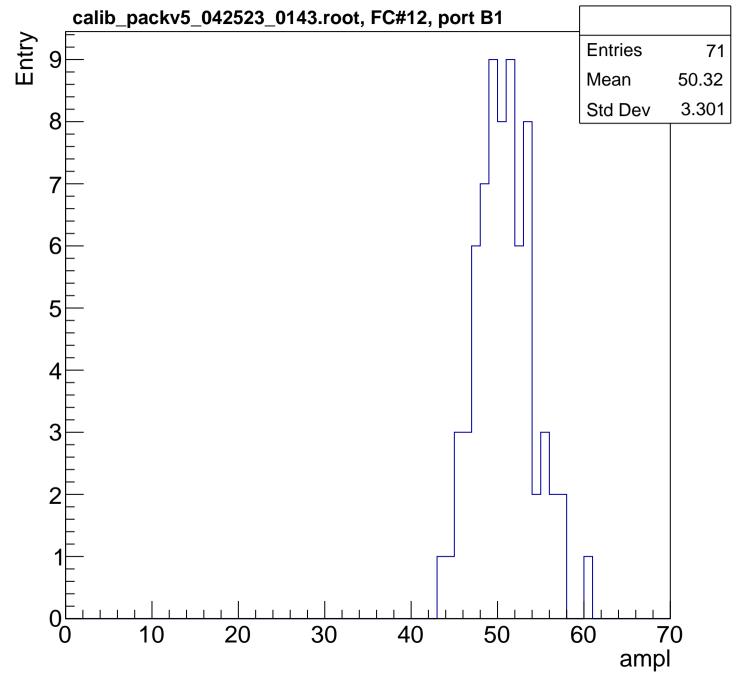


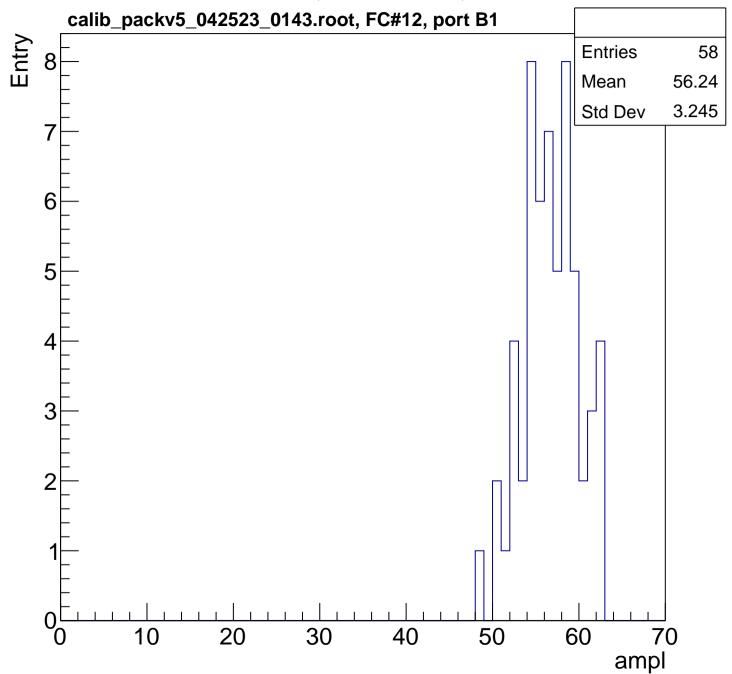


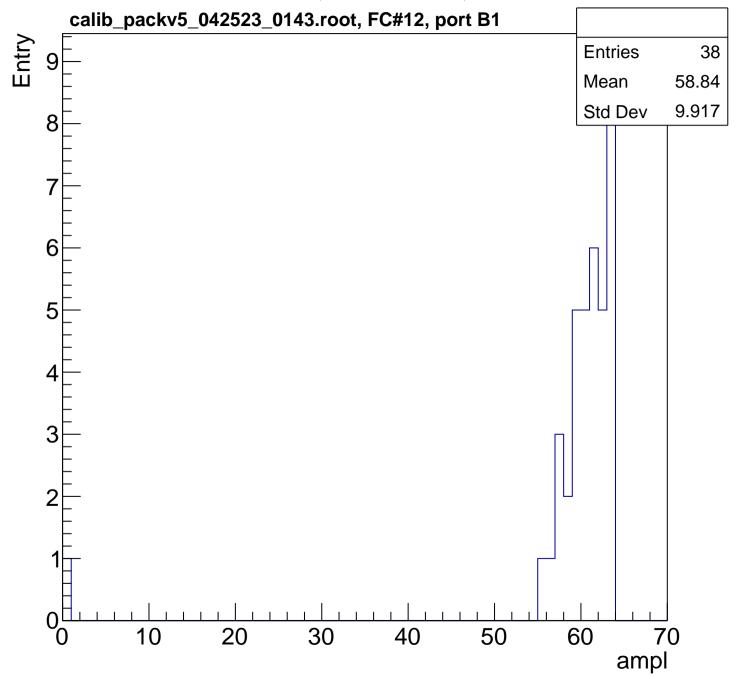


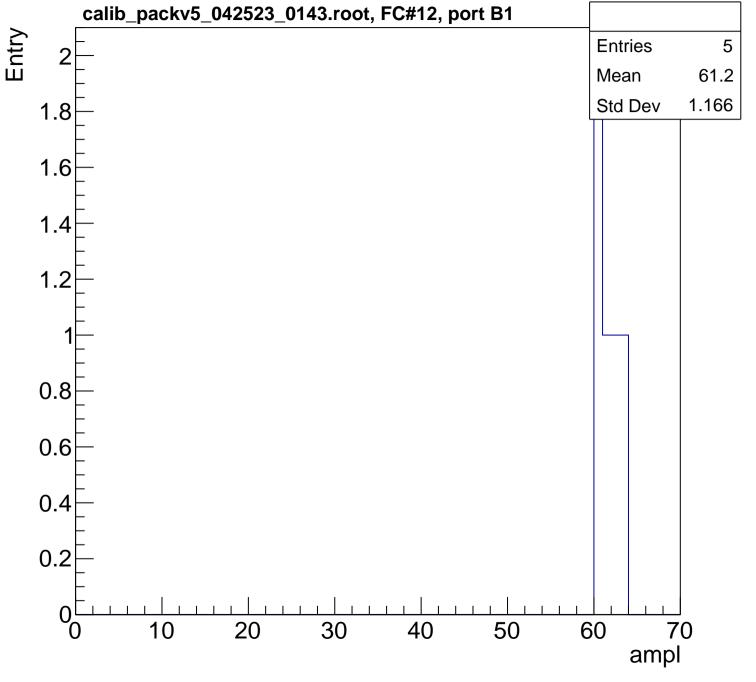


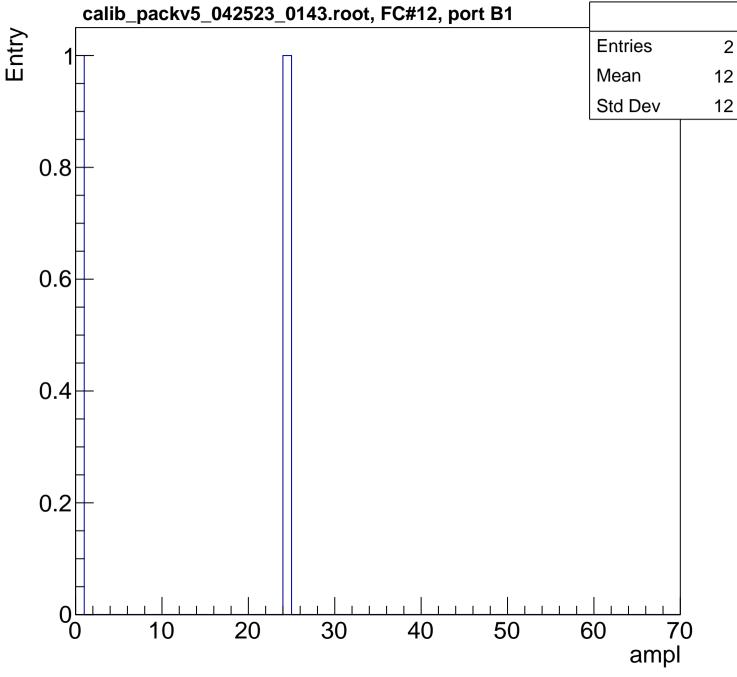


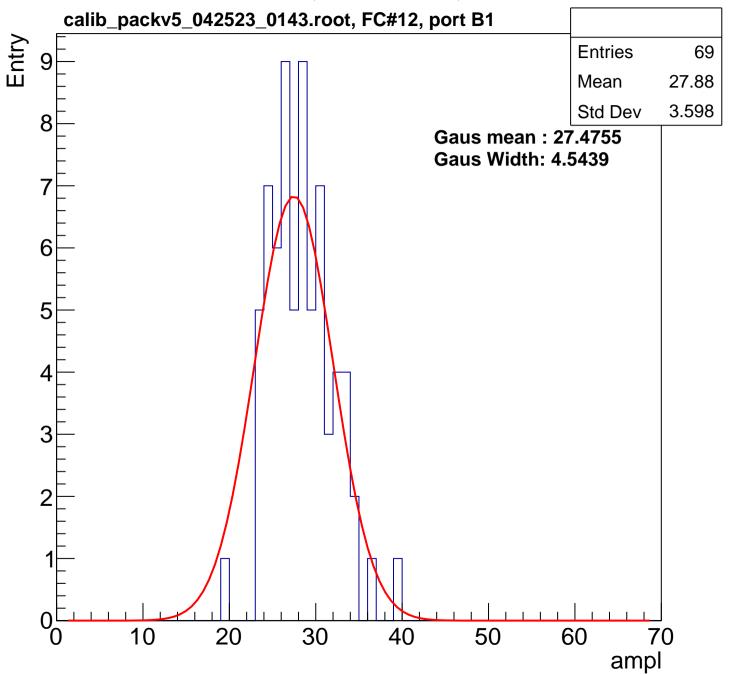


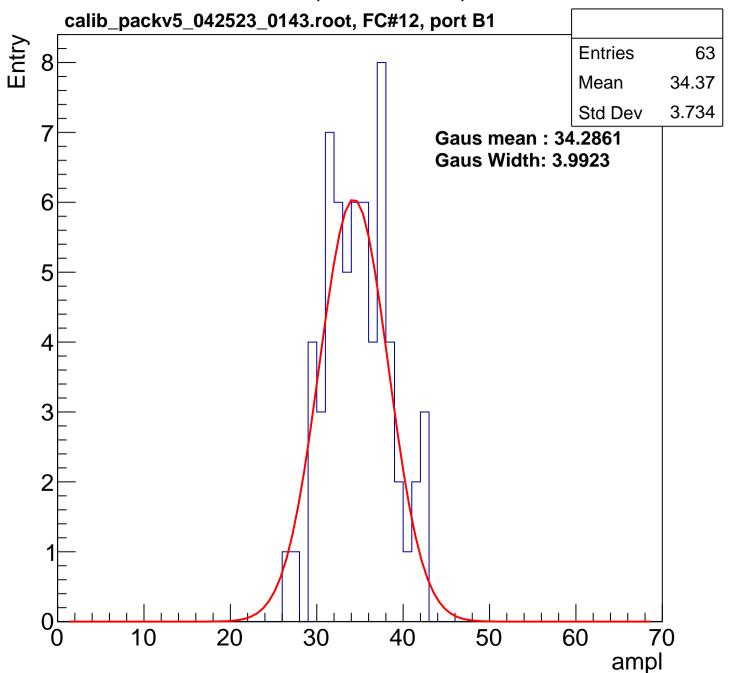


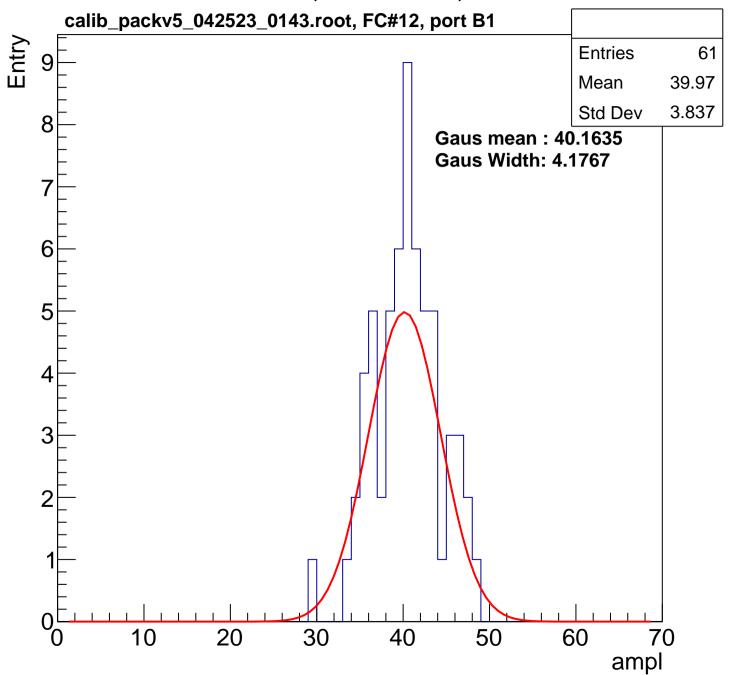


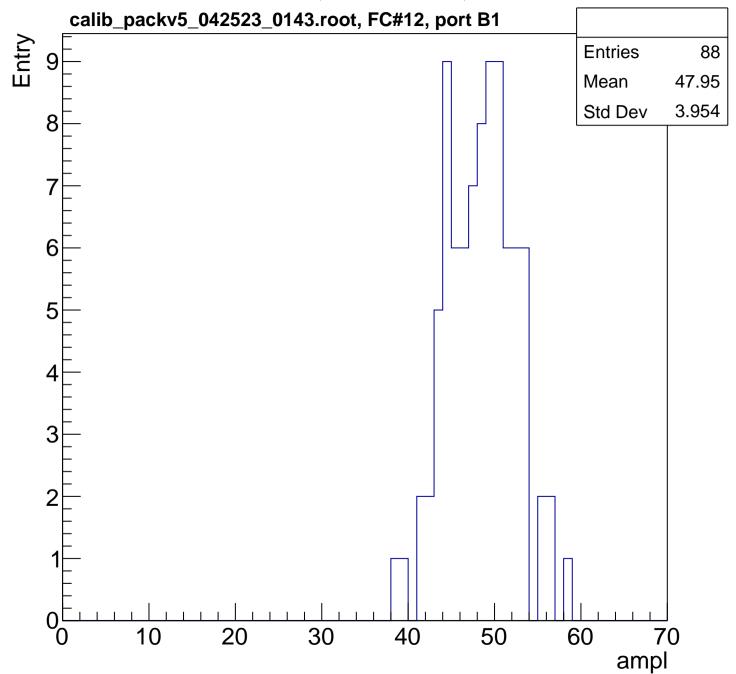


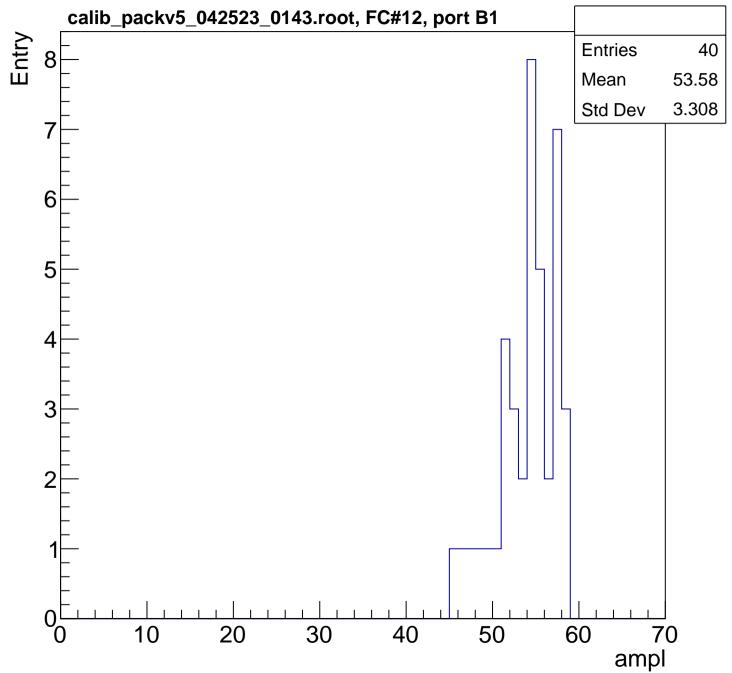


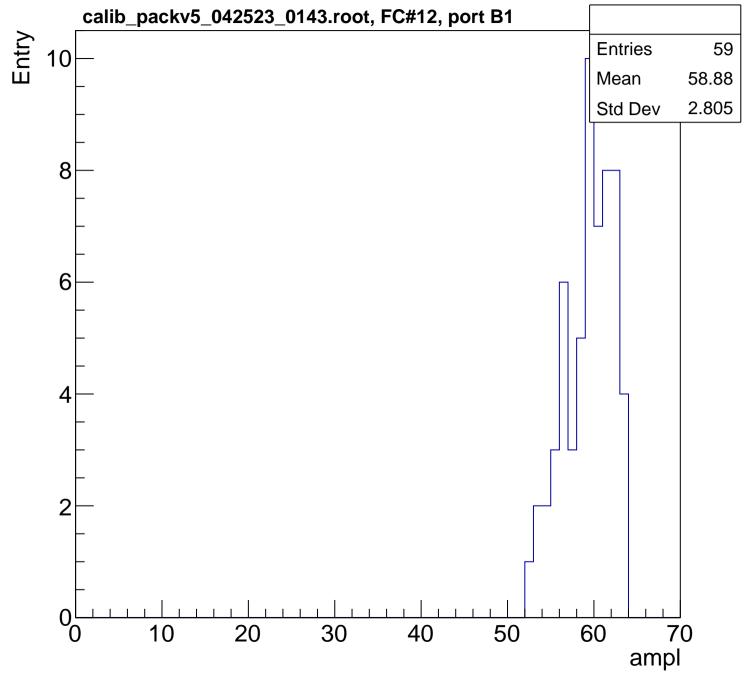


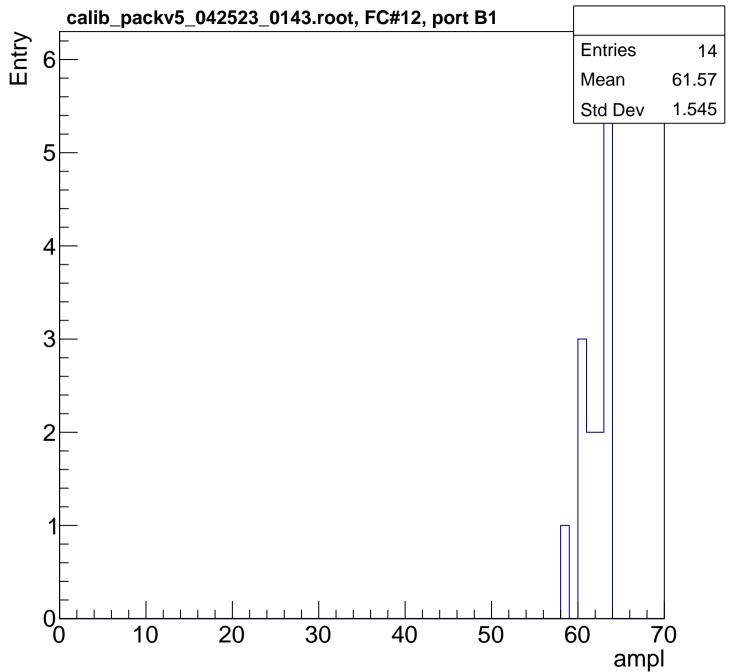


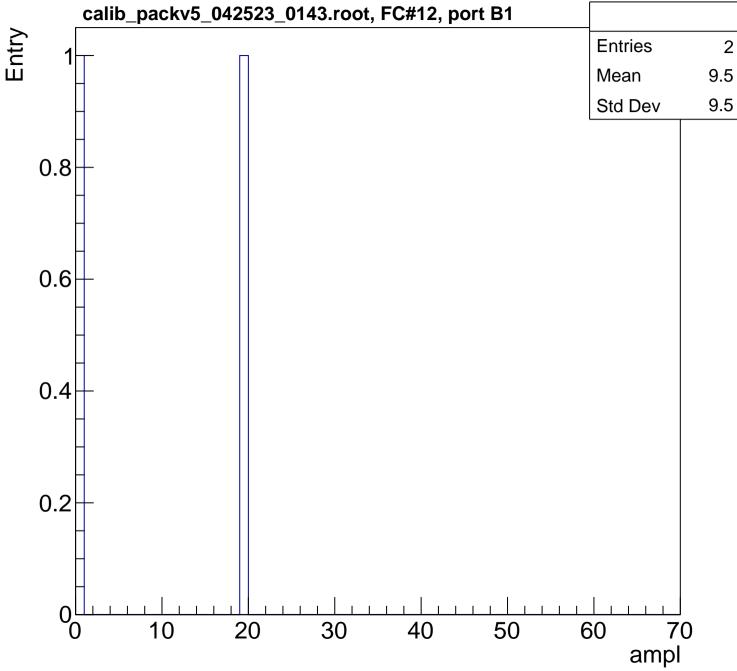


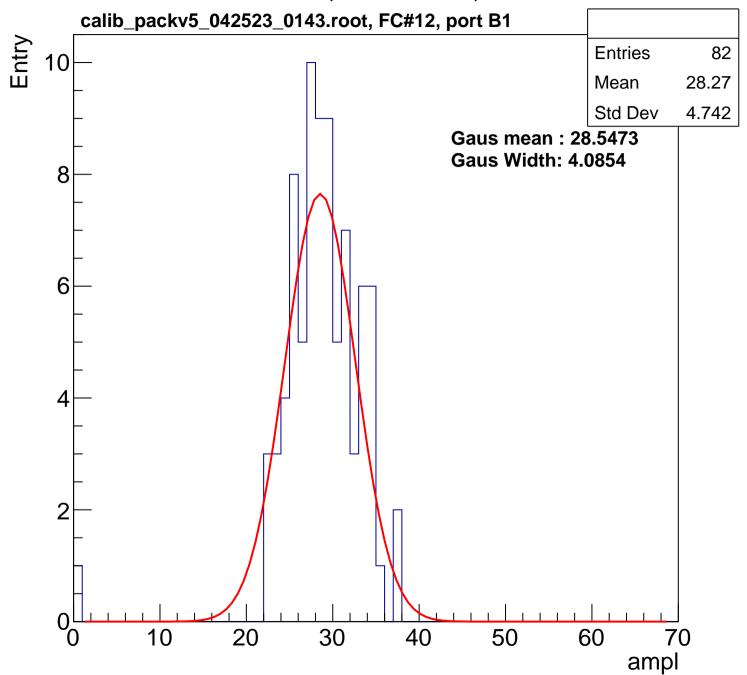


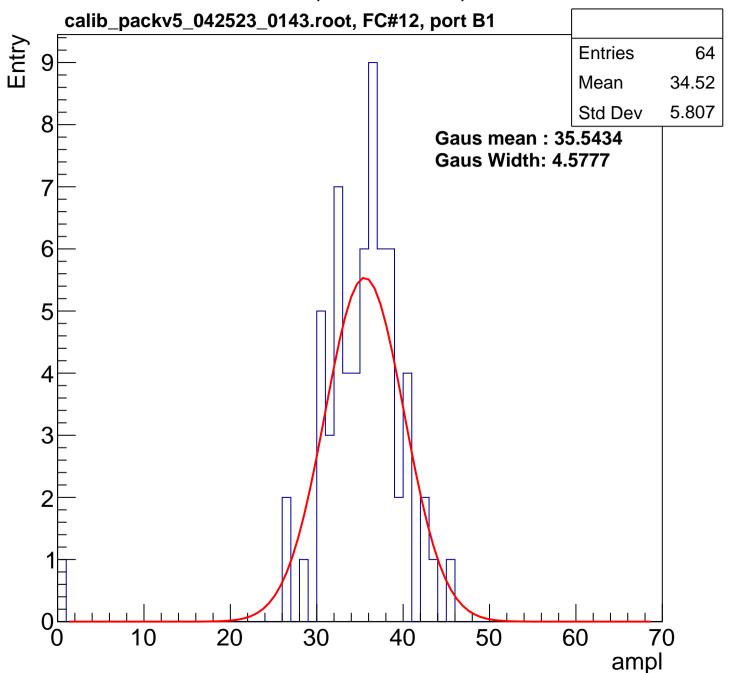


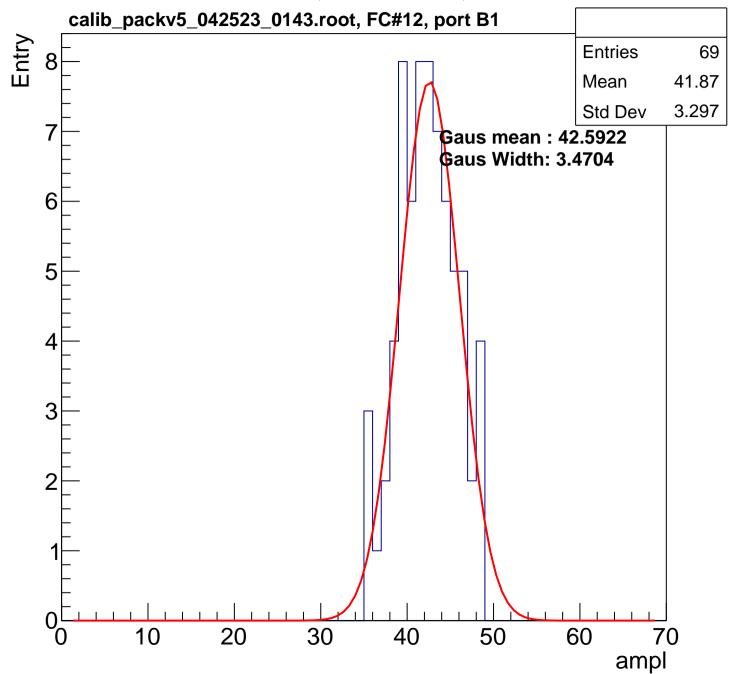


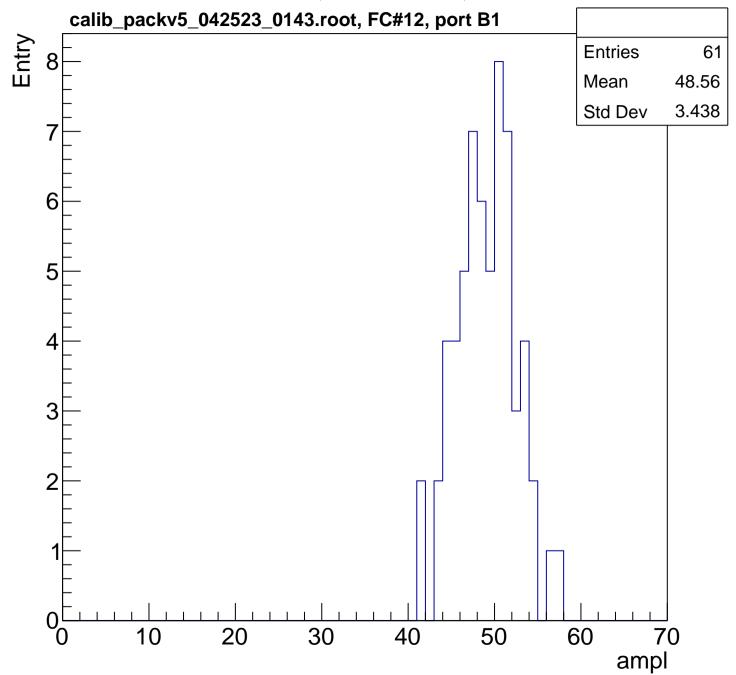


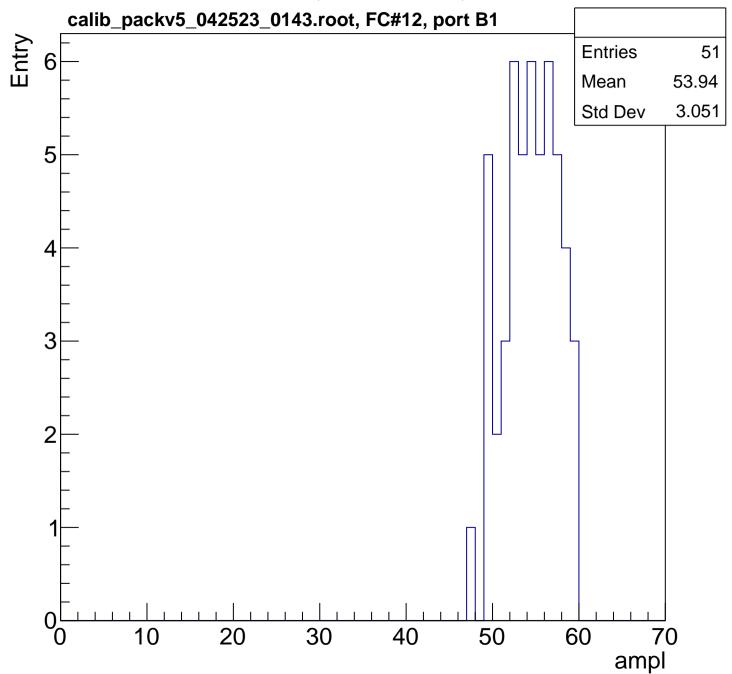


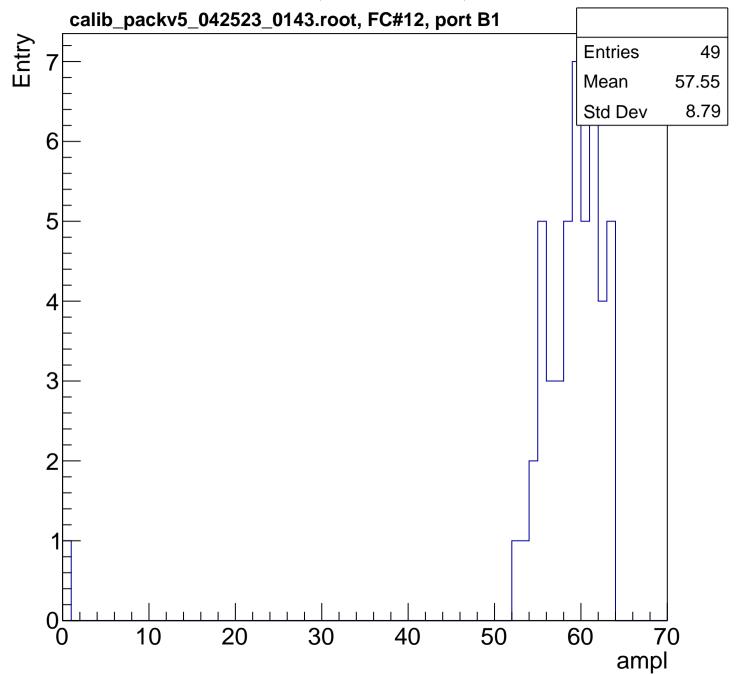


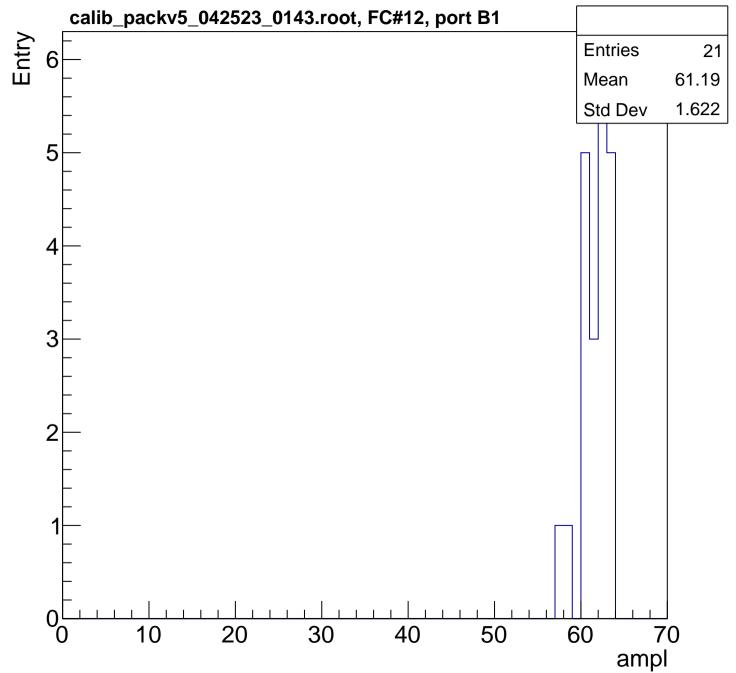




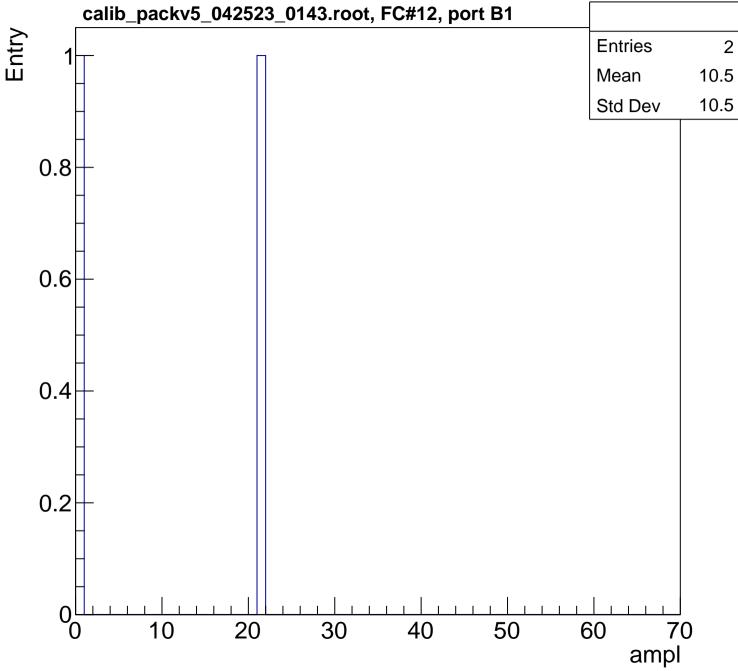


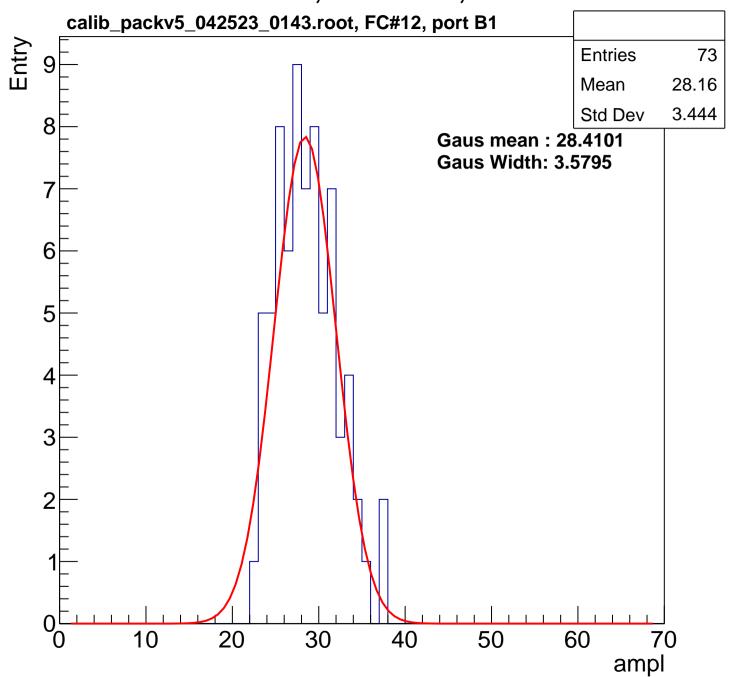


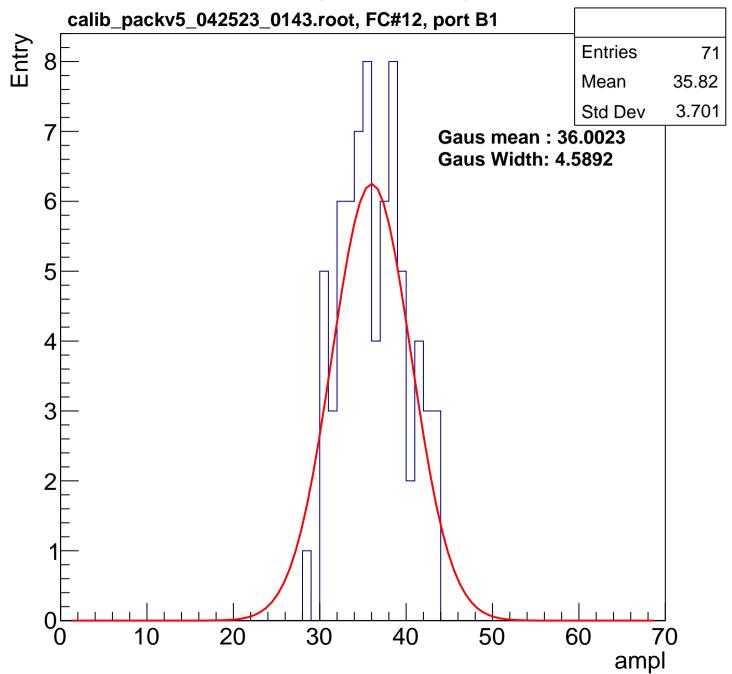


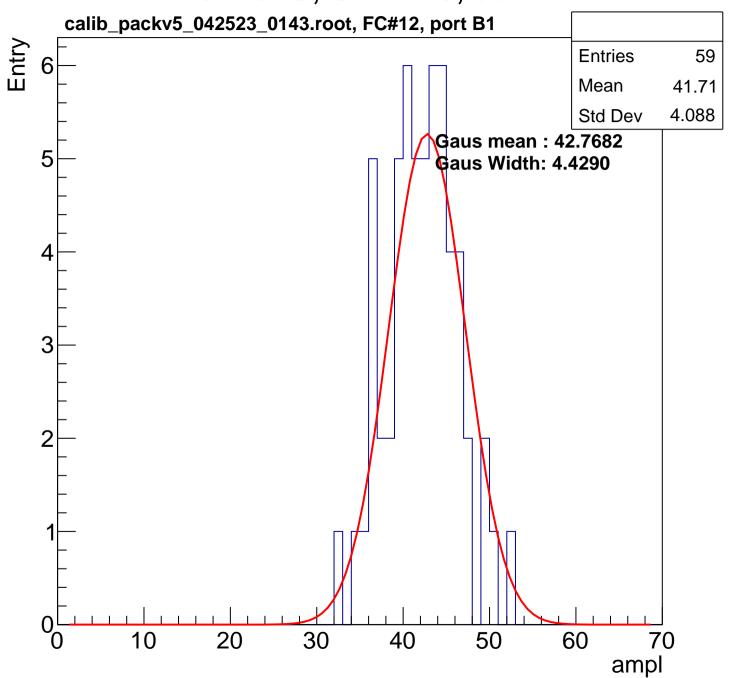


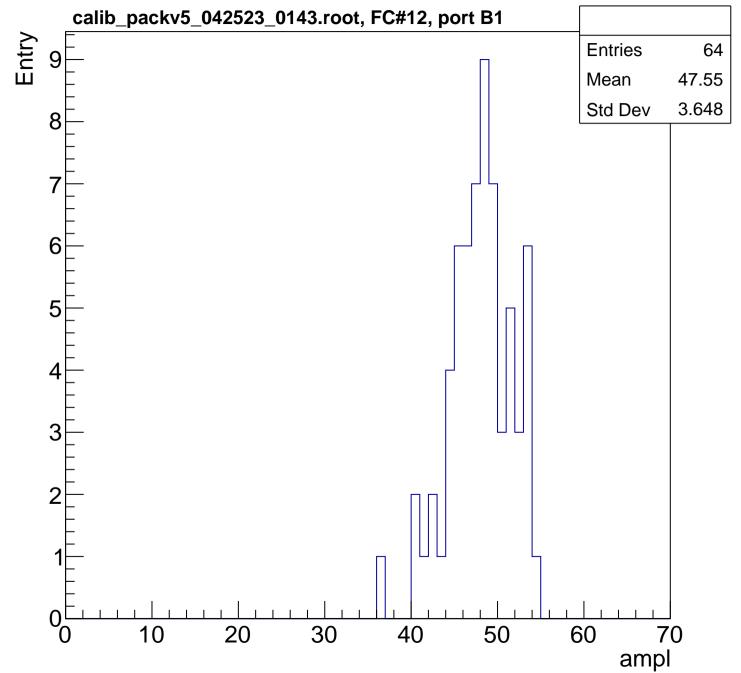
2

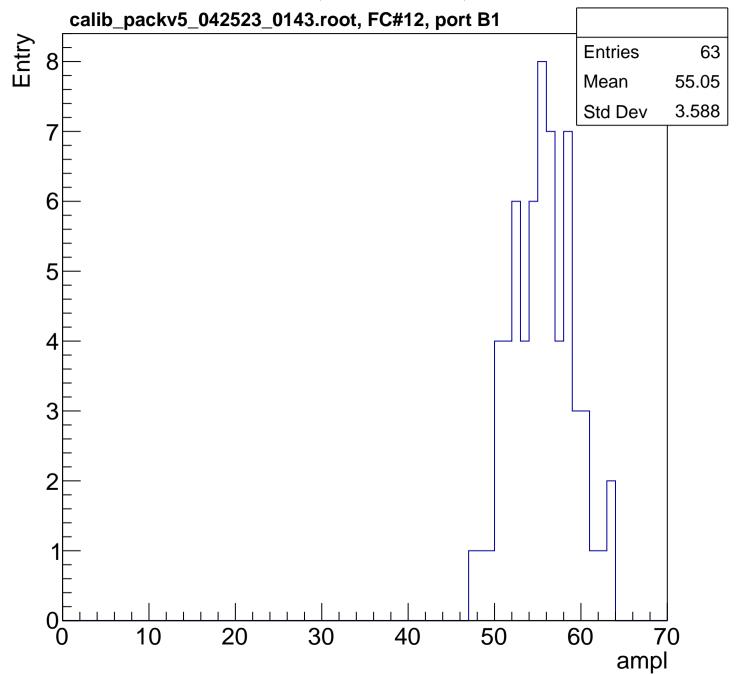


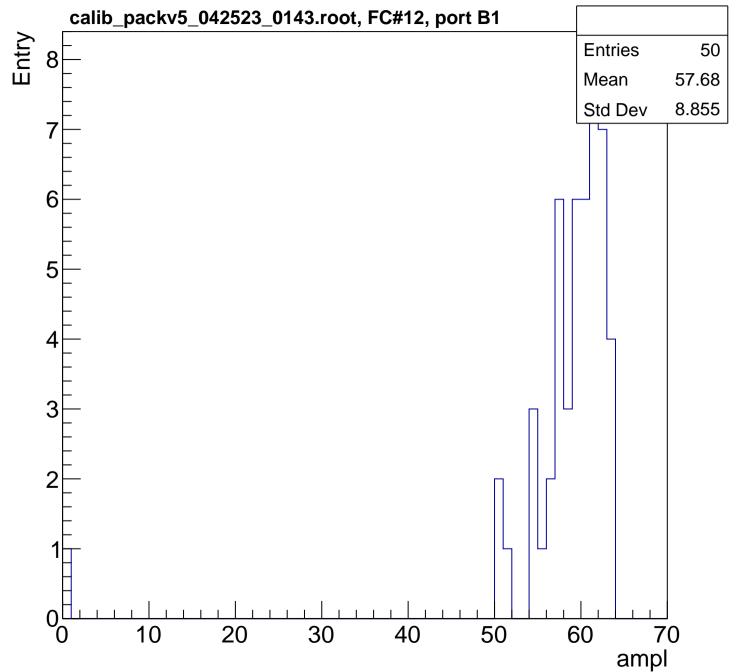


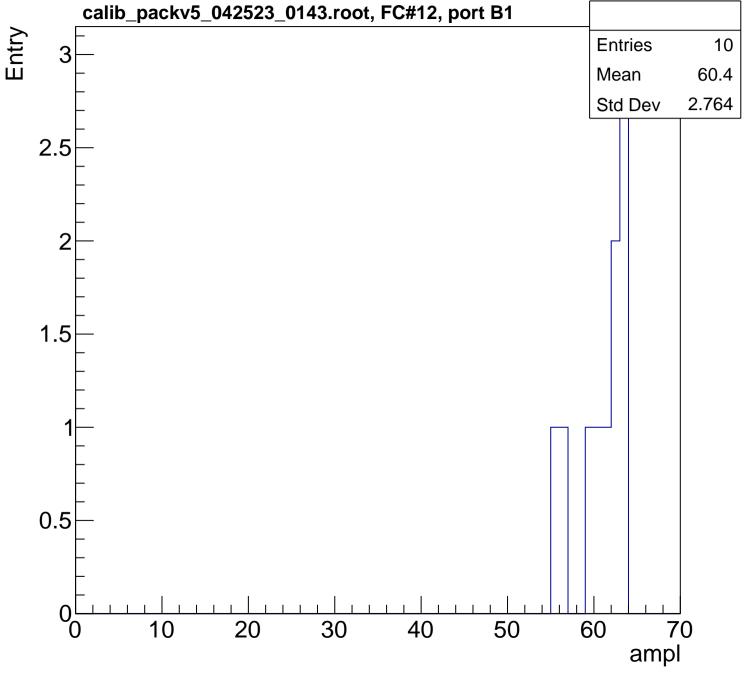


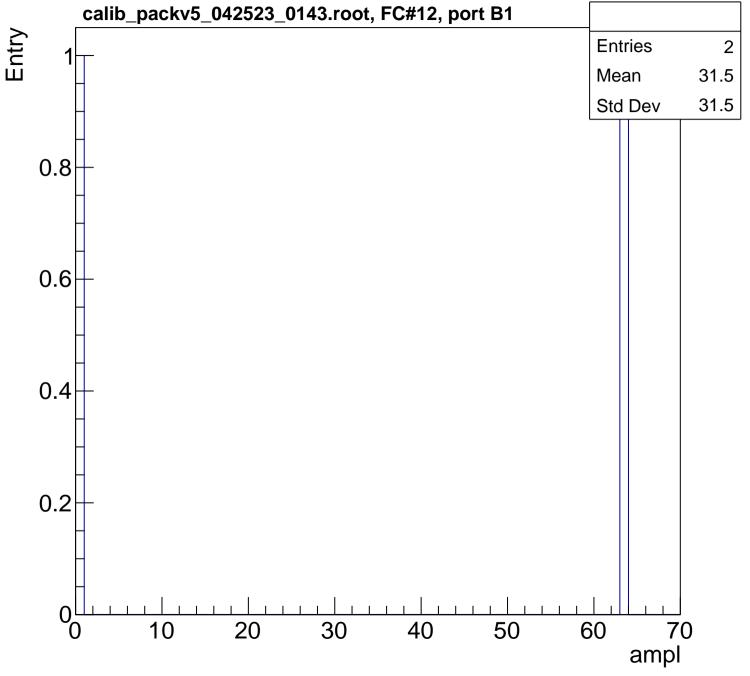


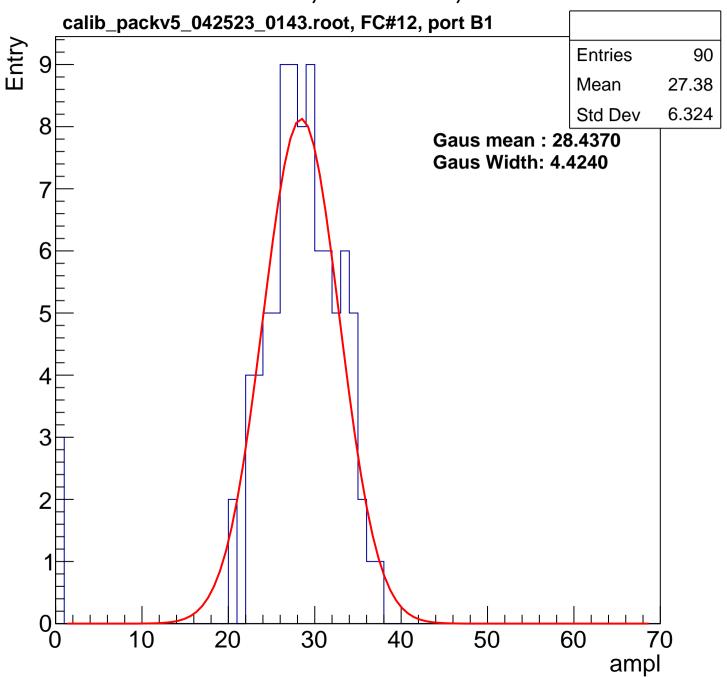


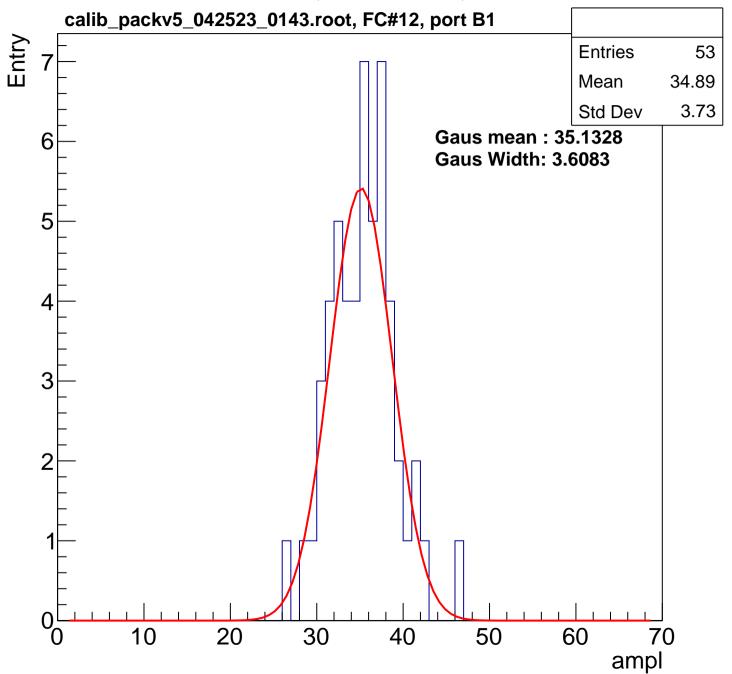


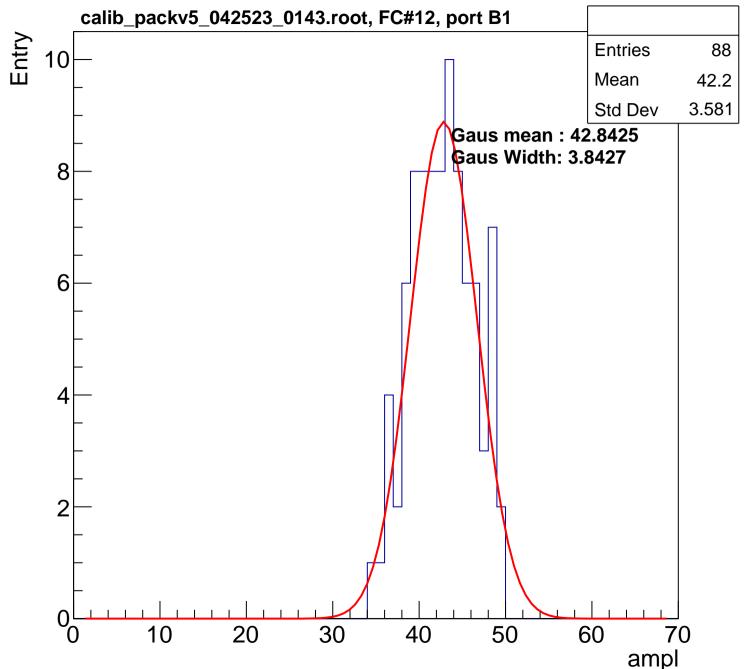


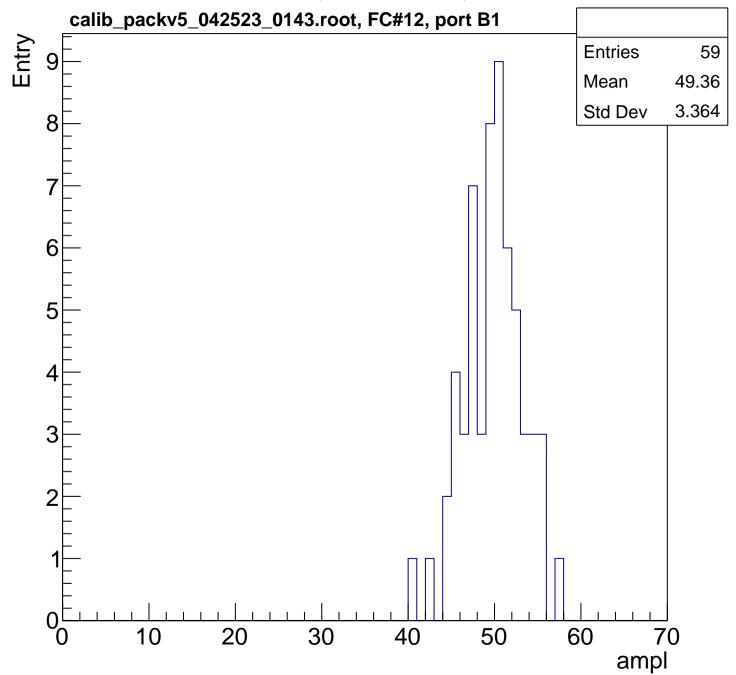


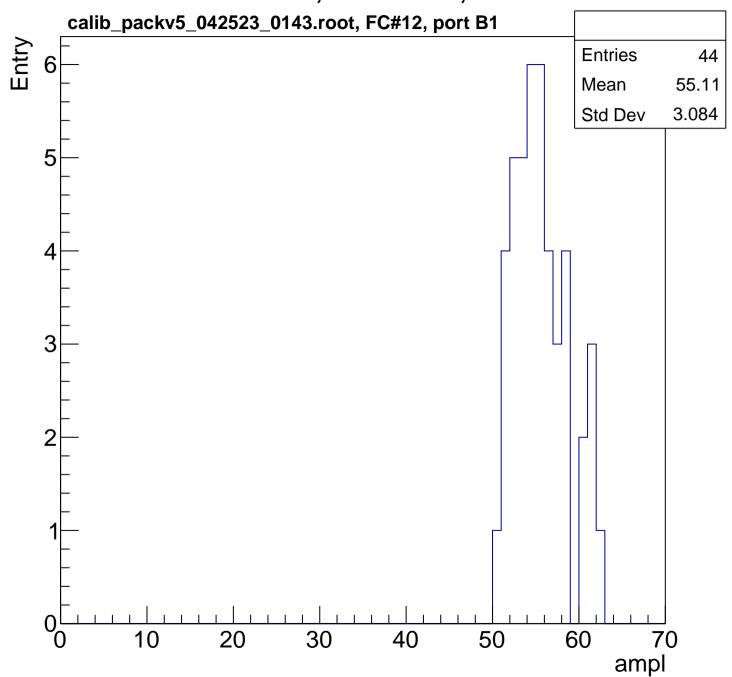


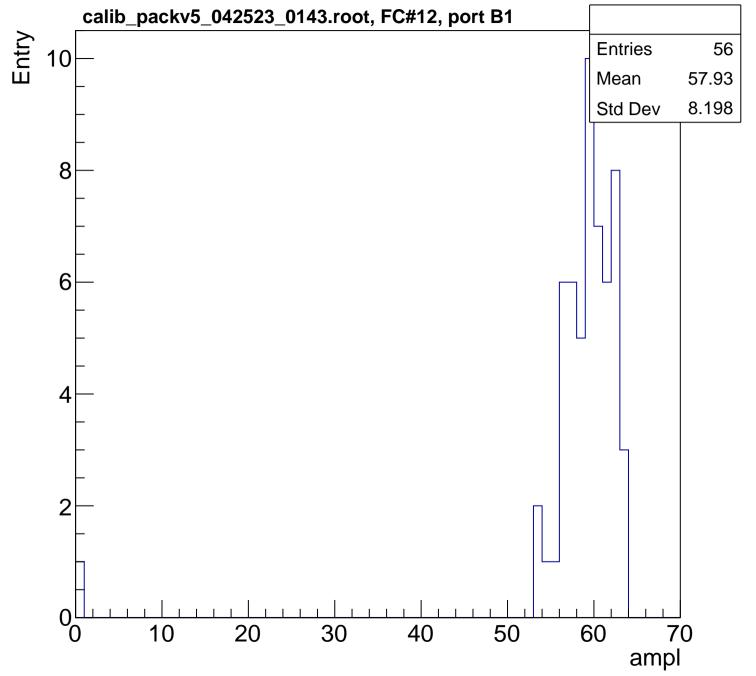


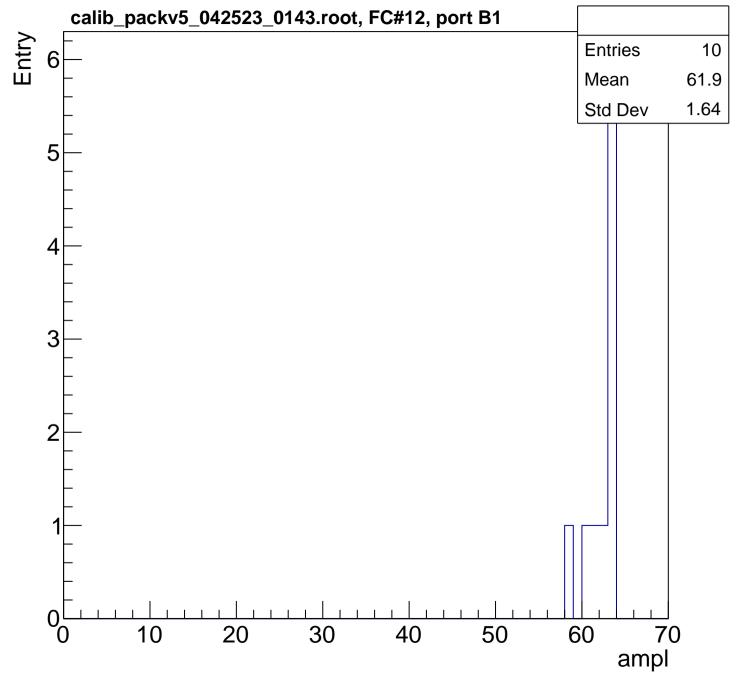


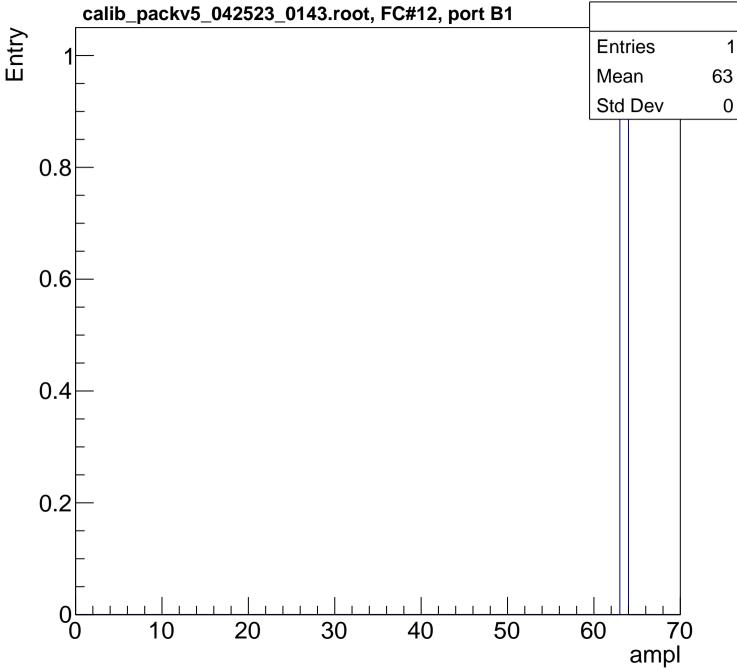


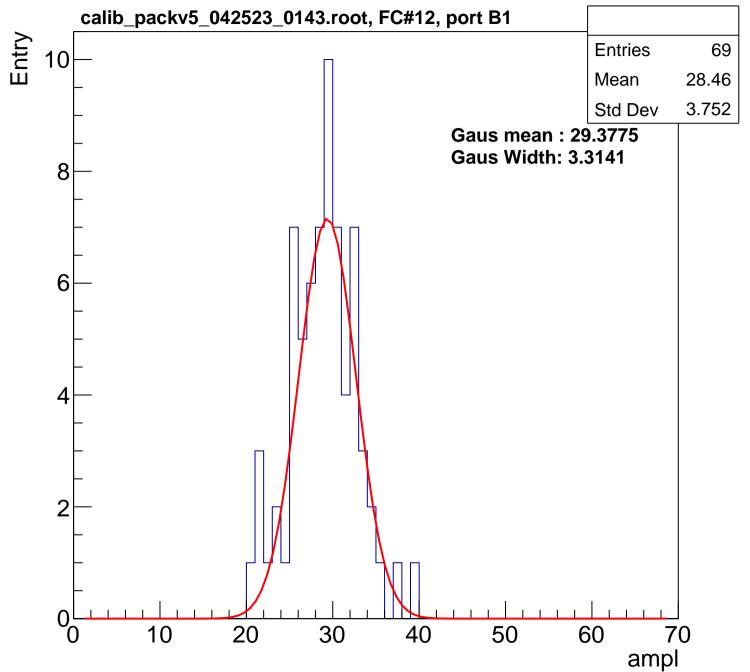


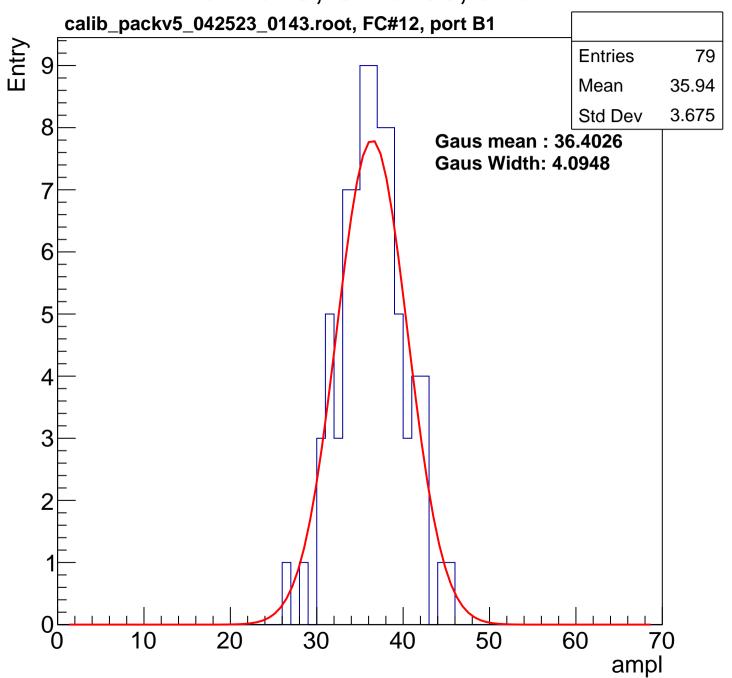


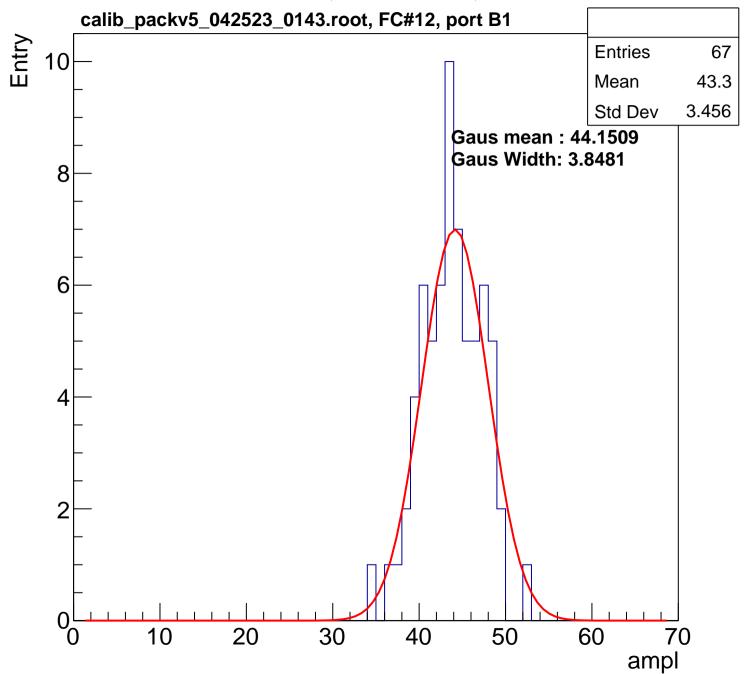


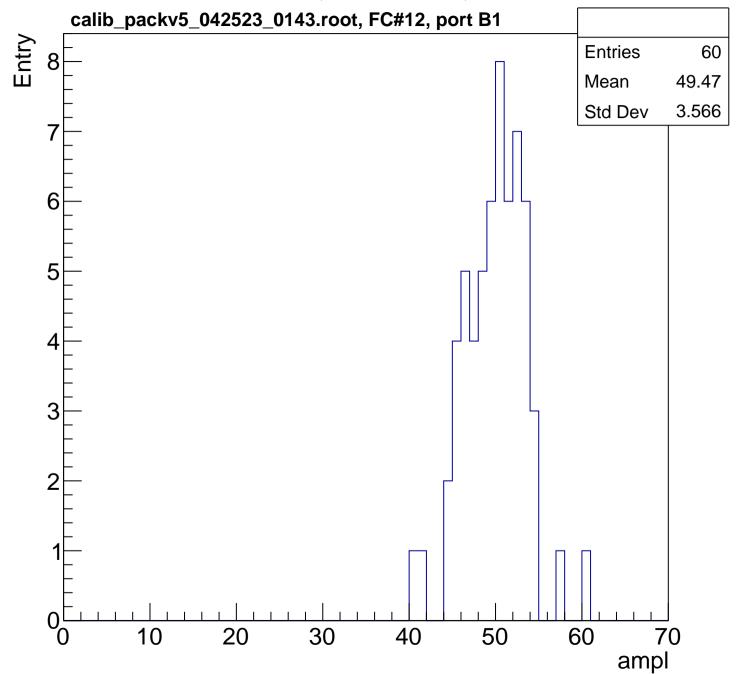


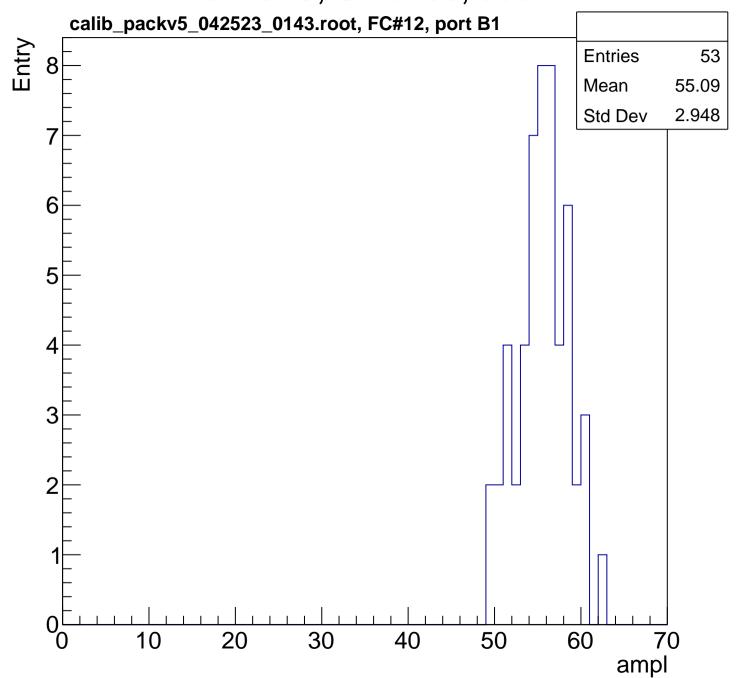


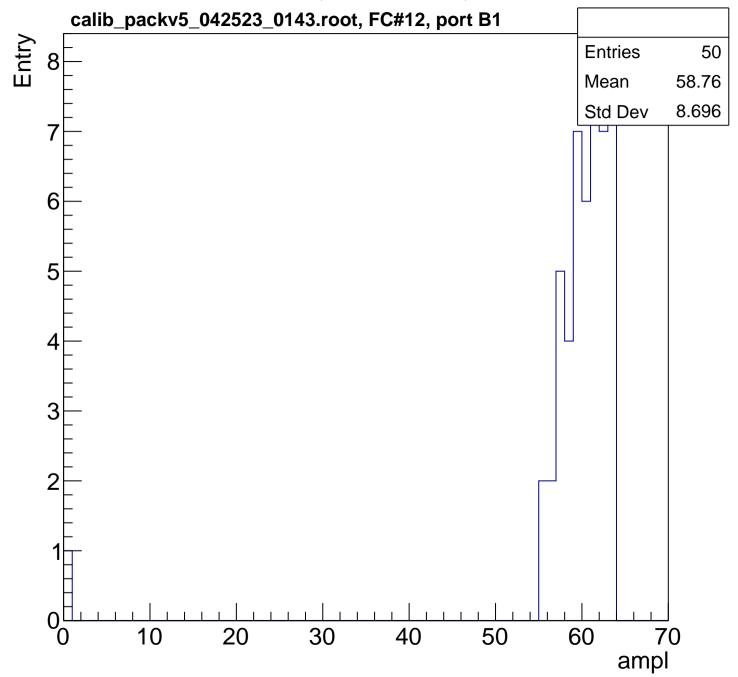


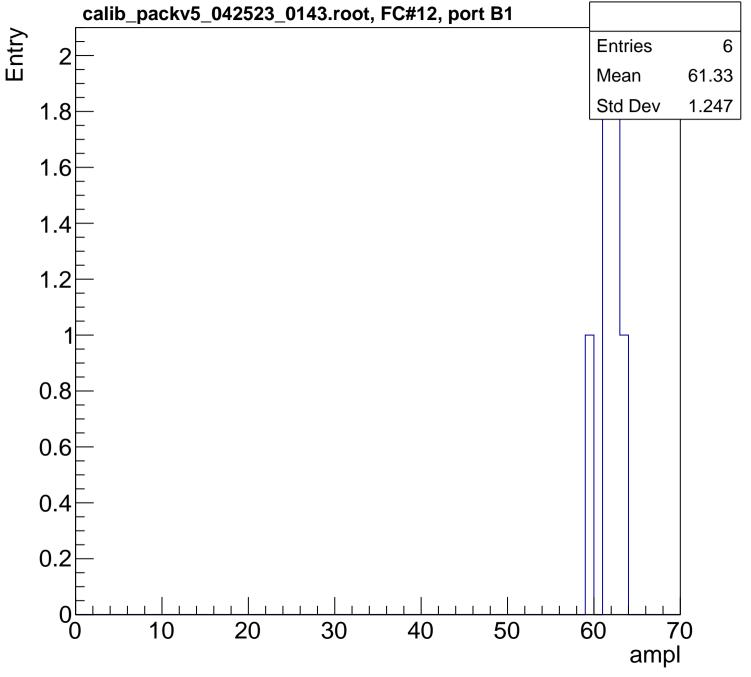




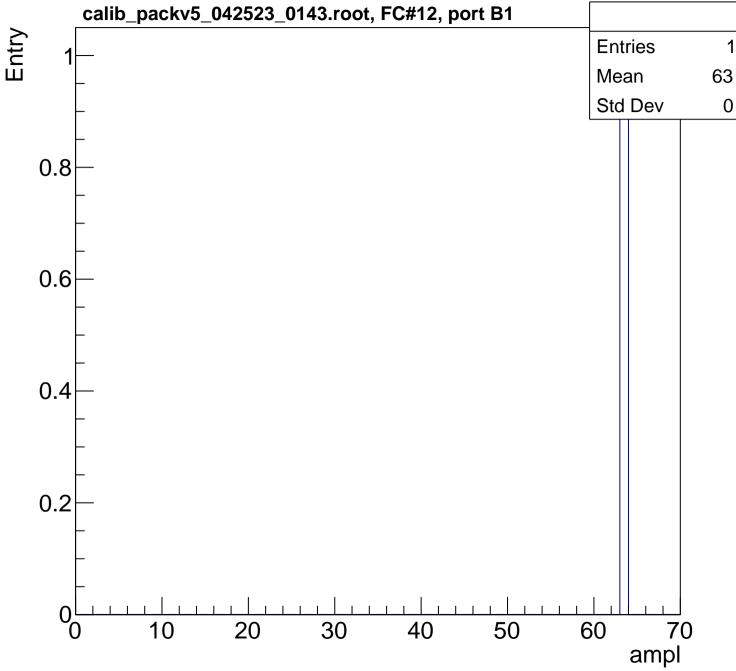


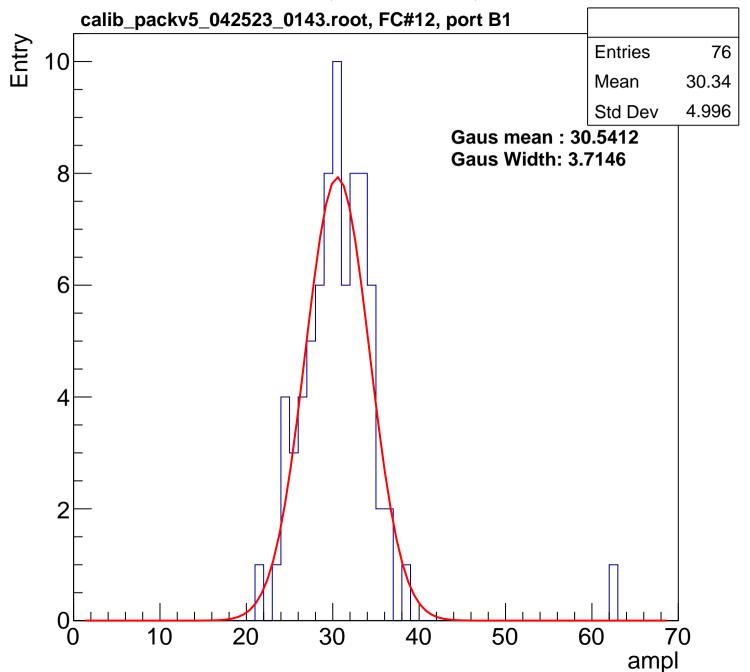


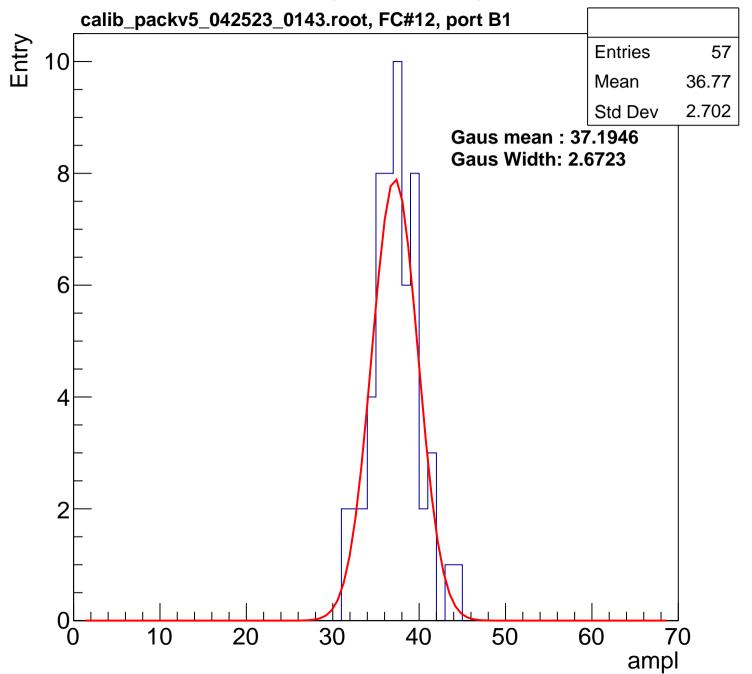


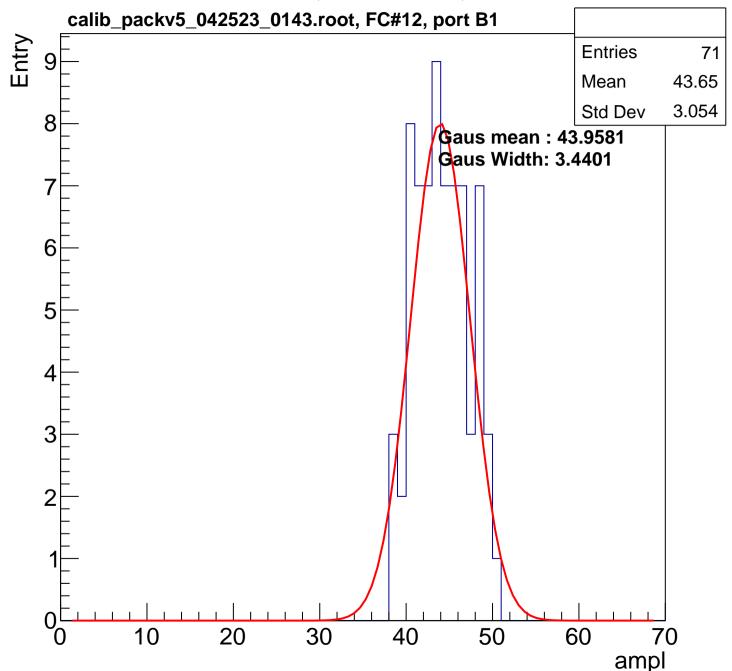


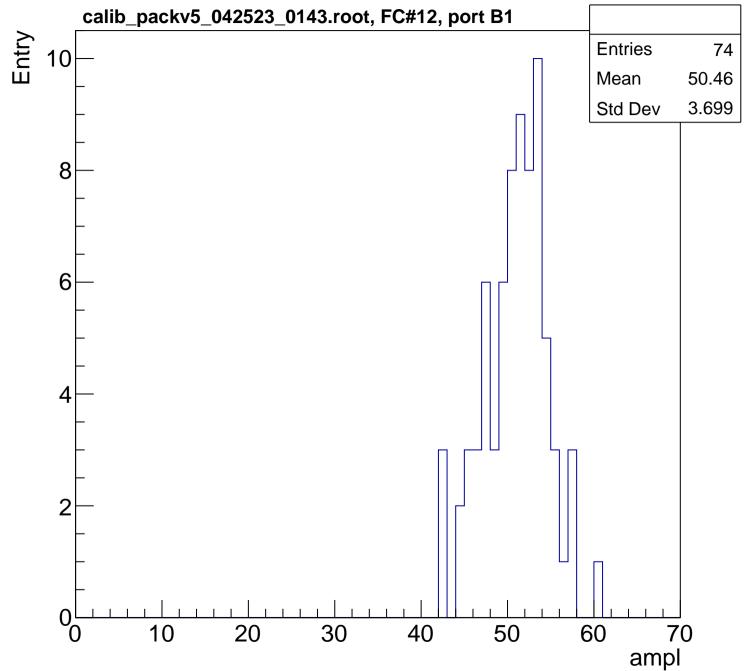
0

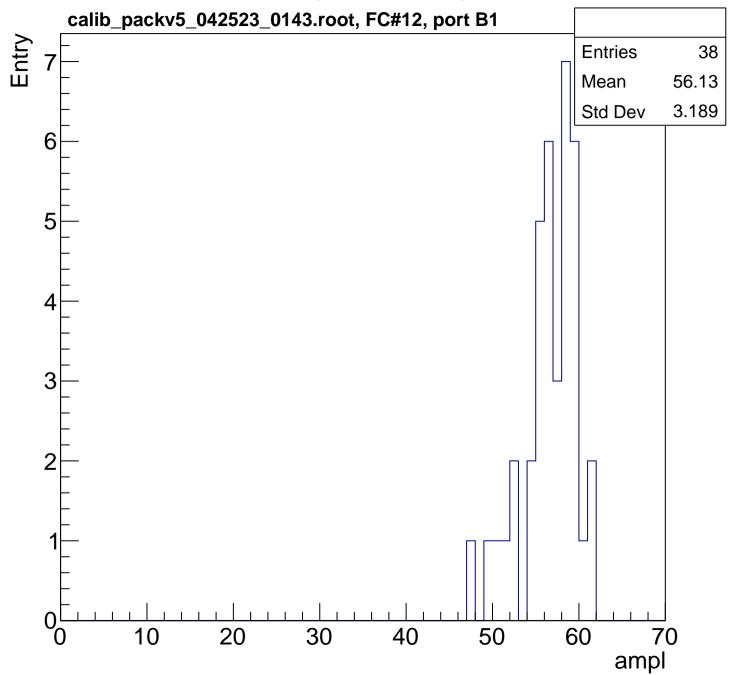


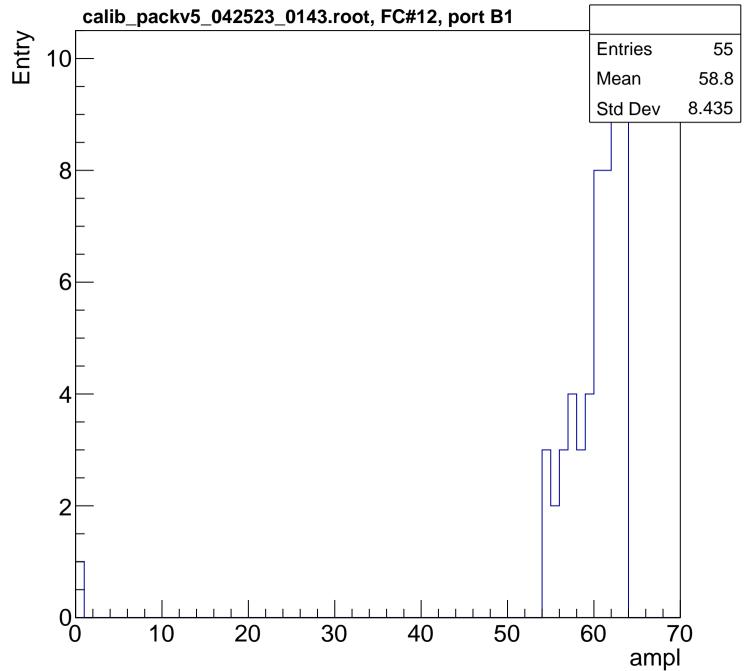




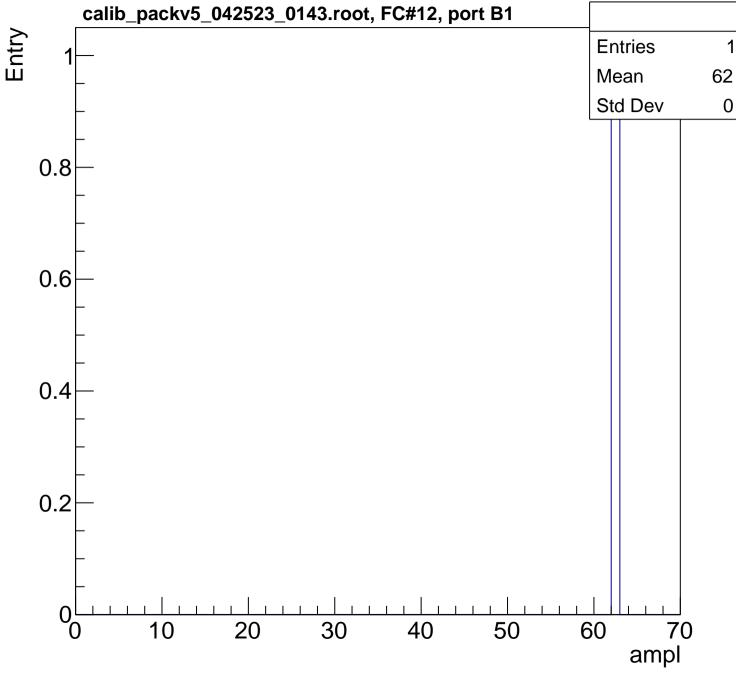


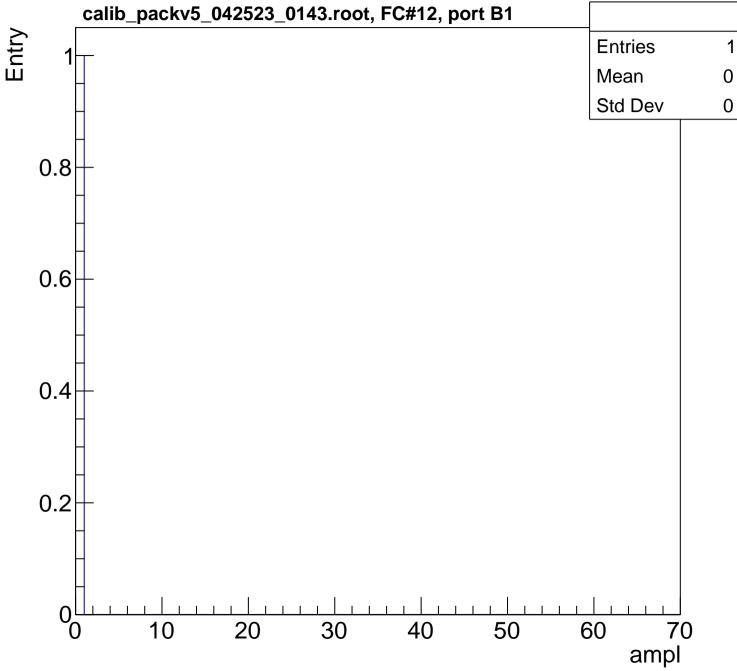


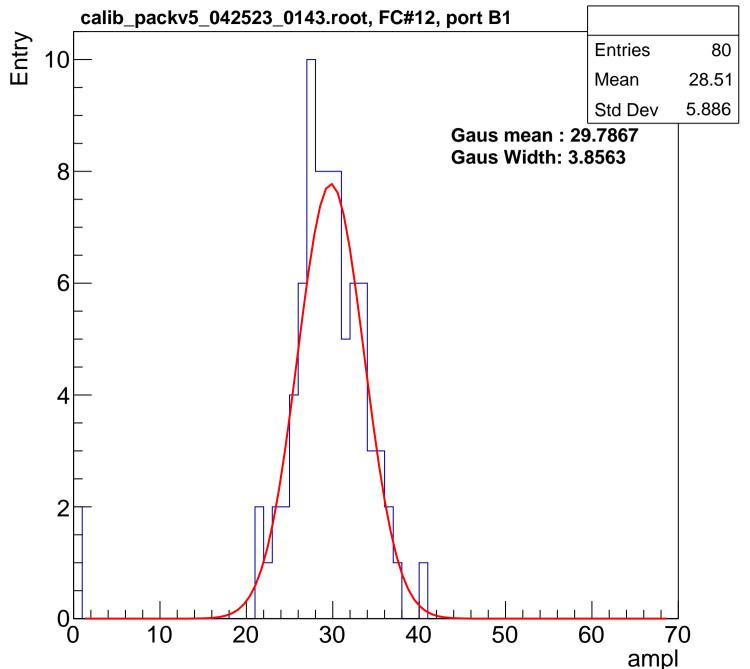


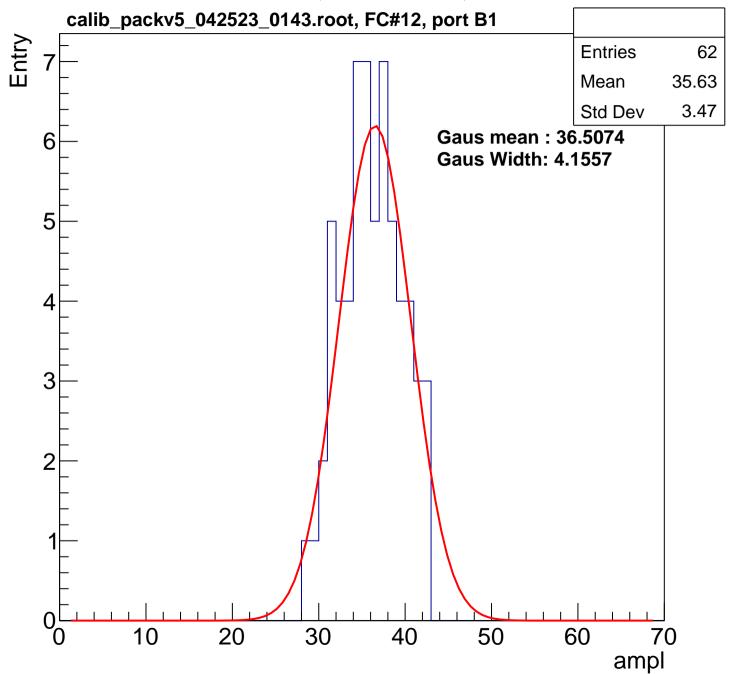


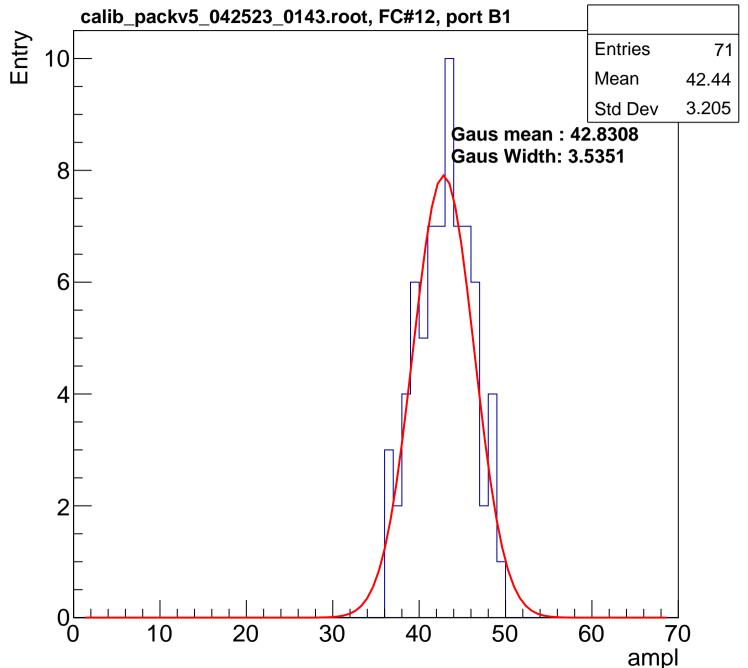
0

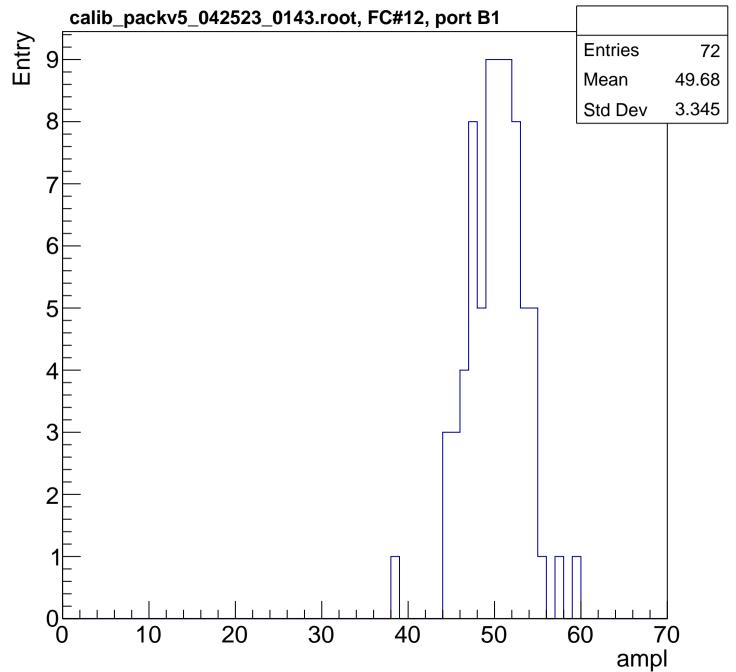


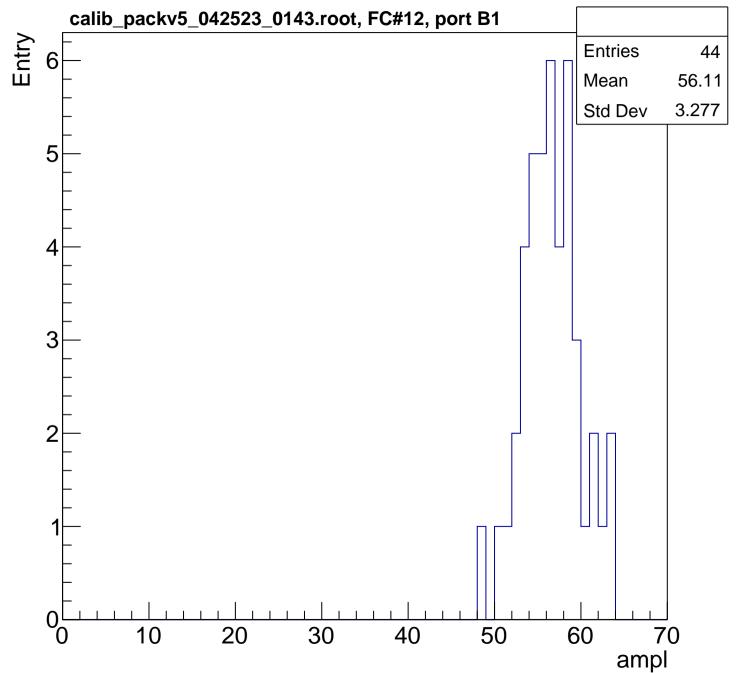


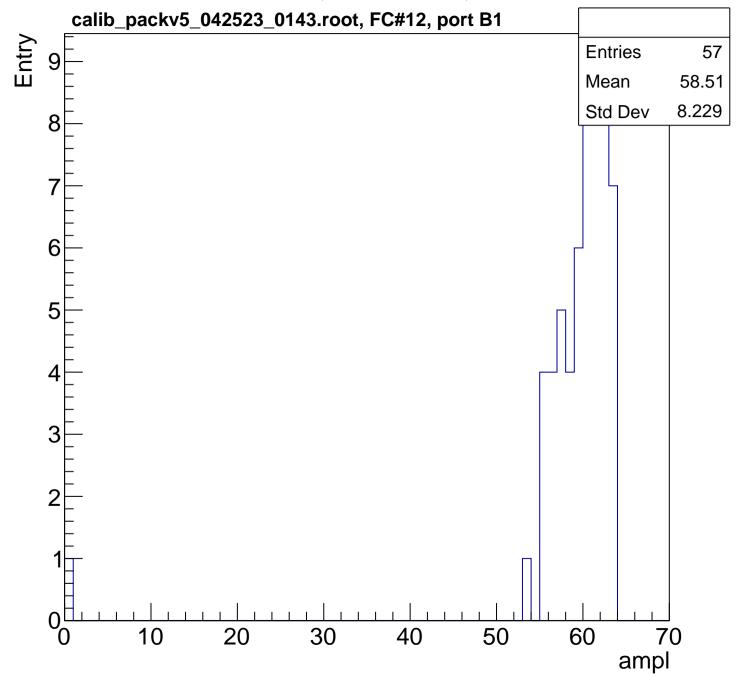


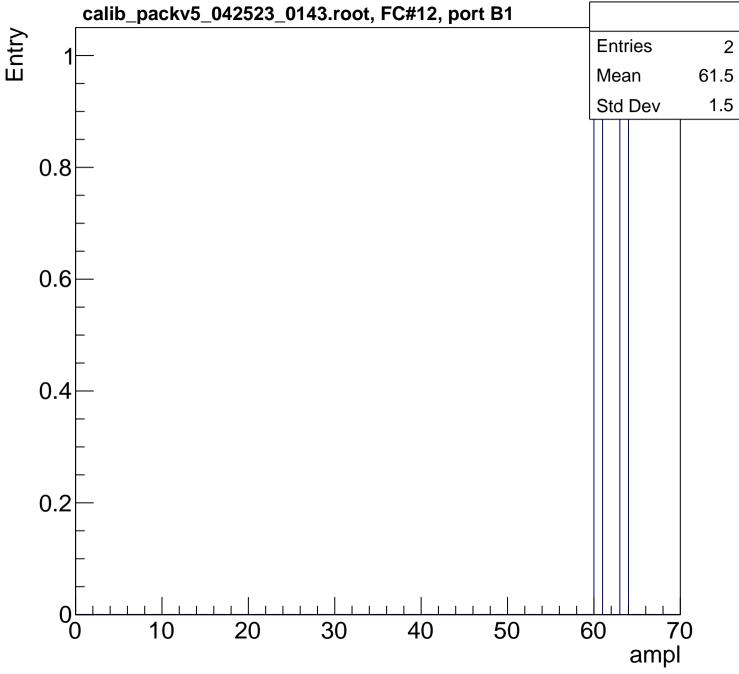


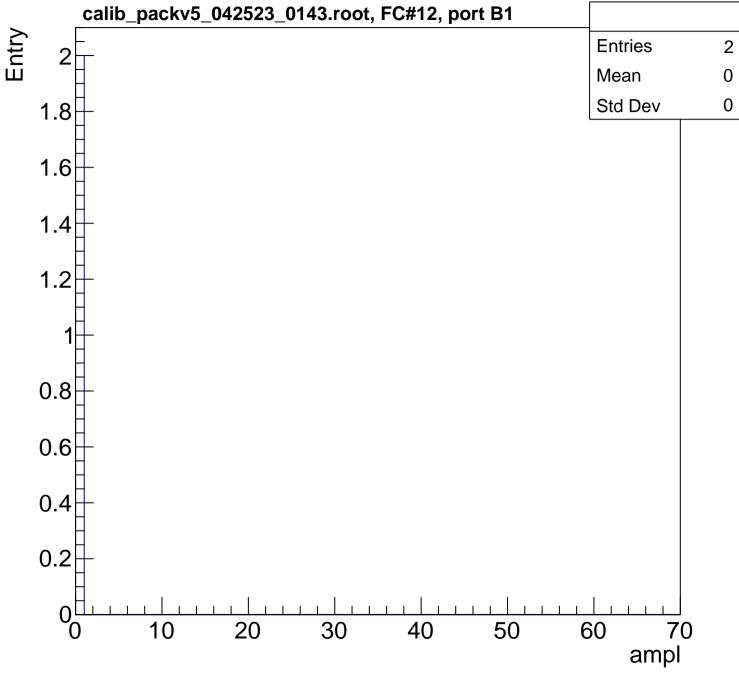


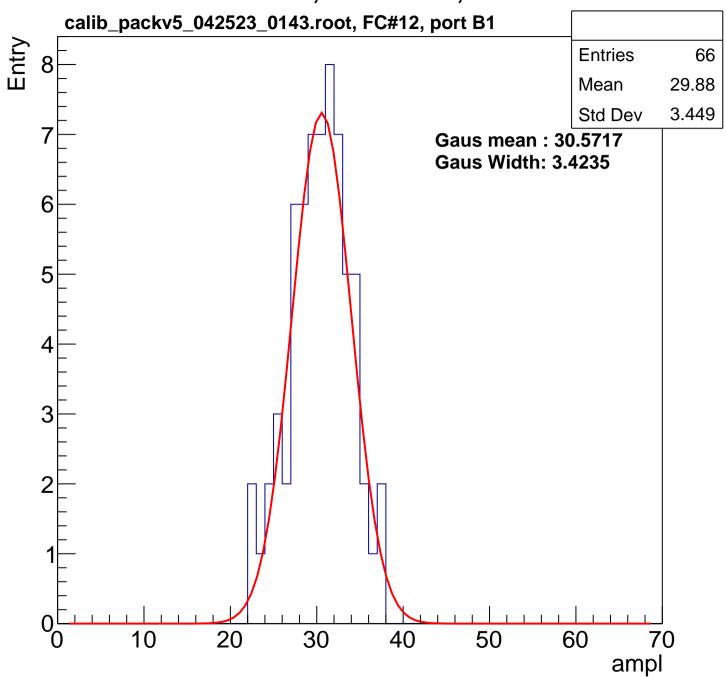


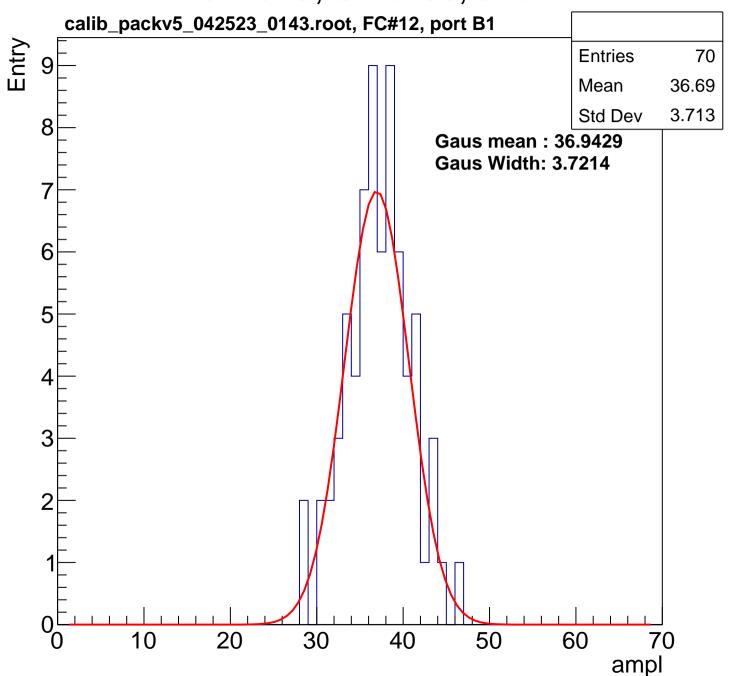


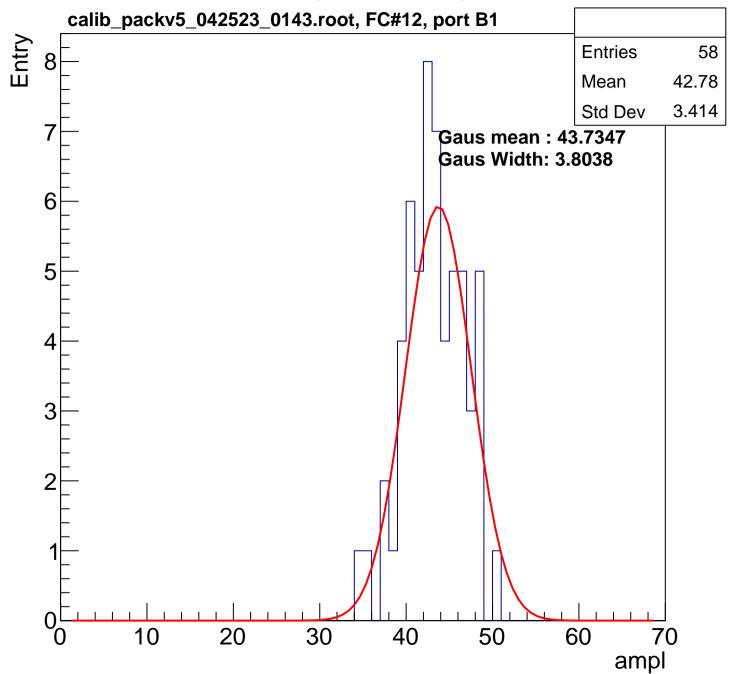


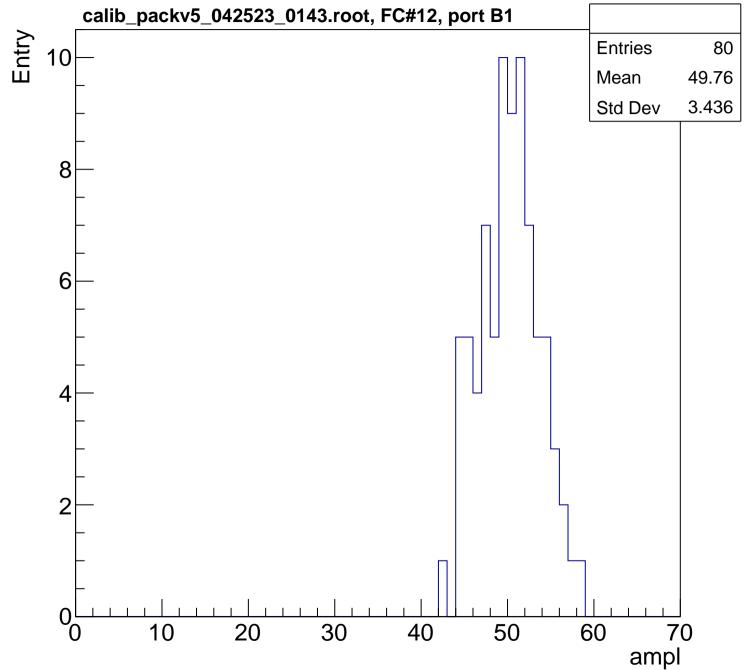


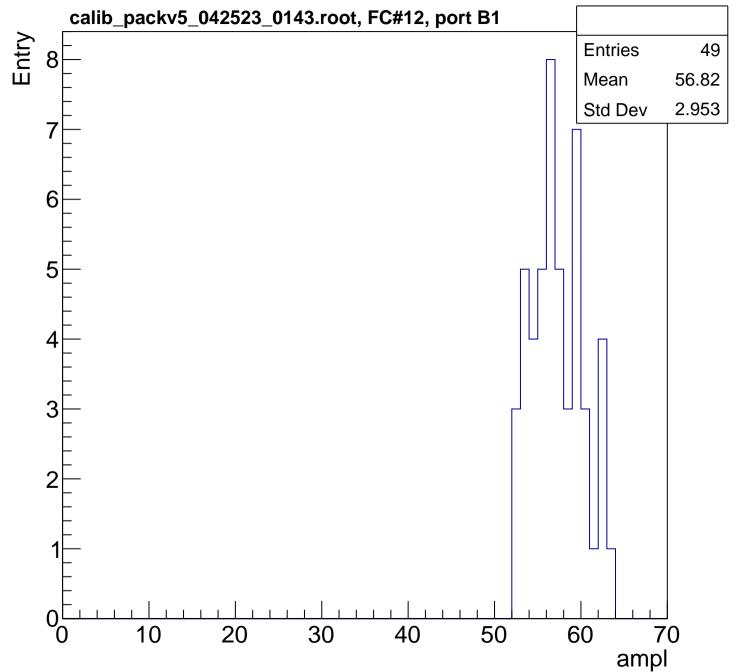


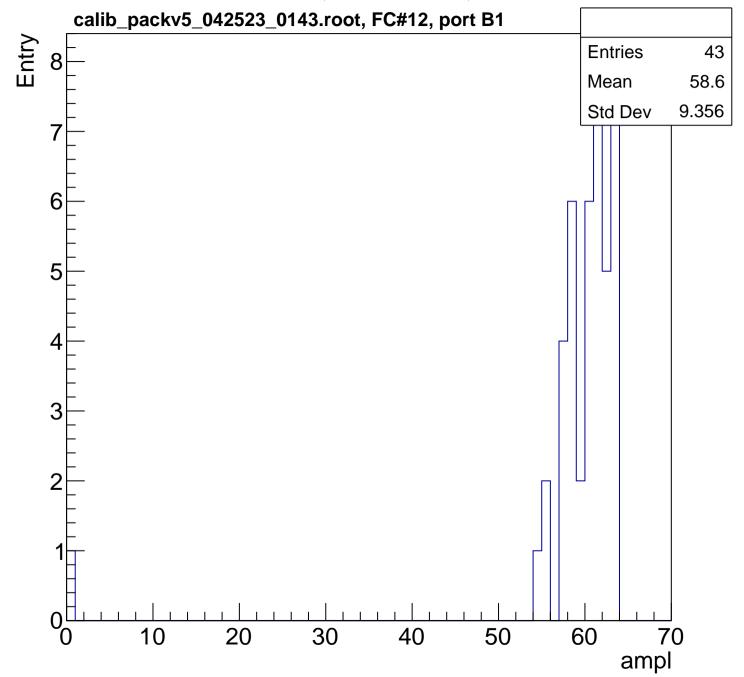


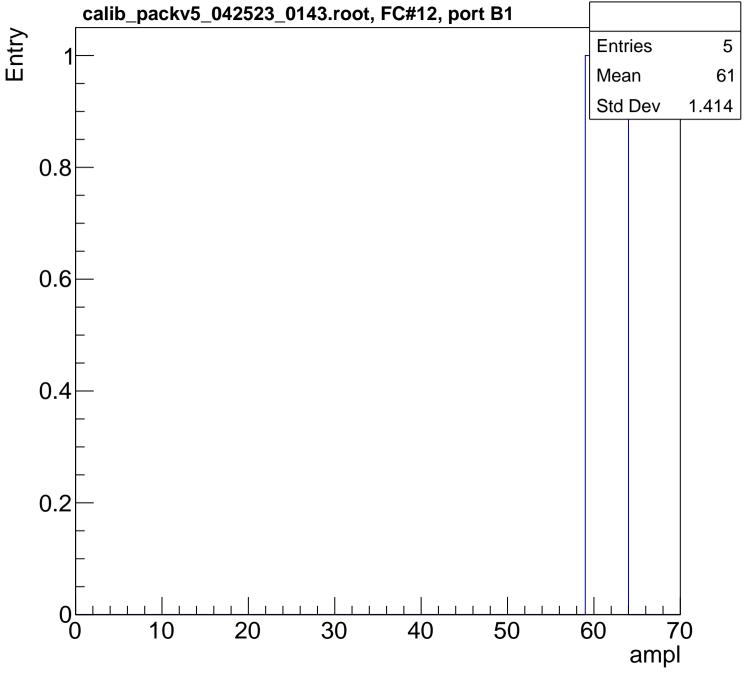


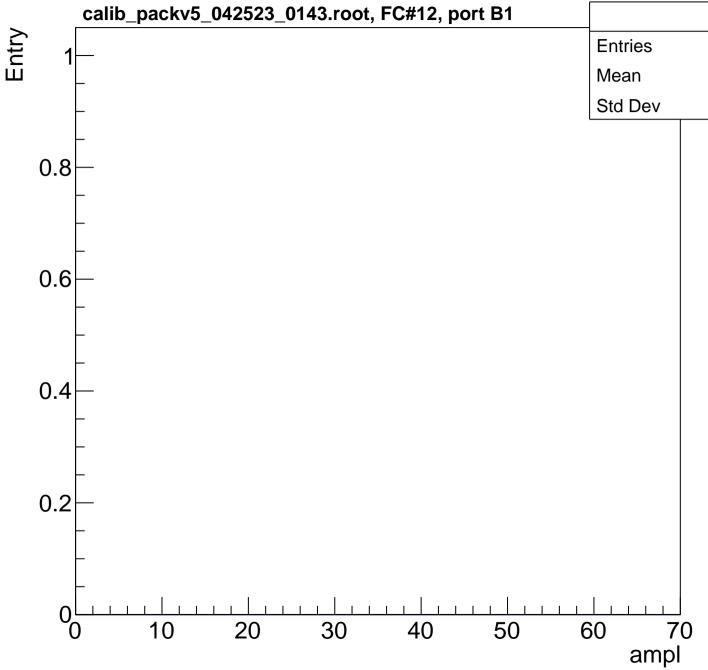


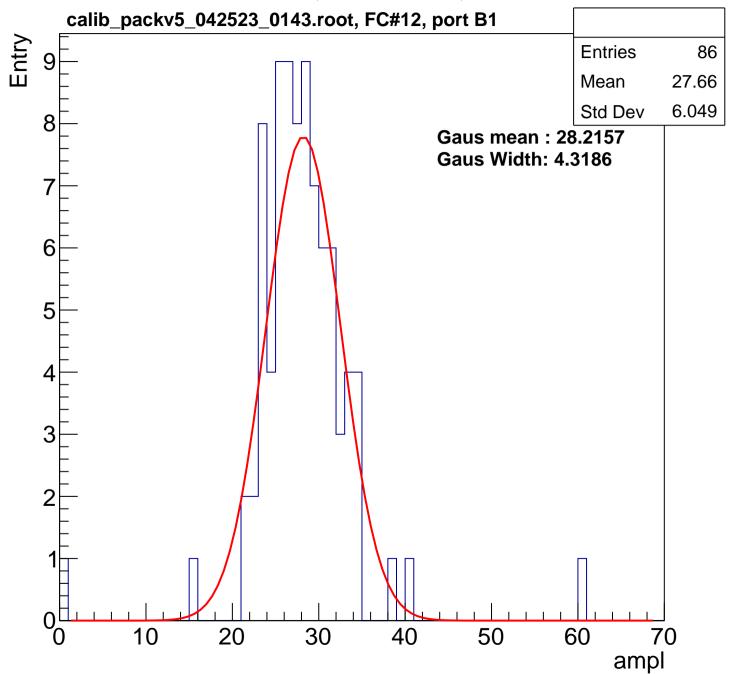


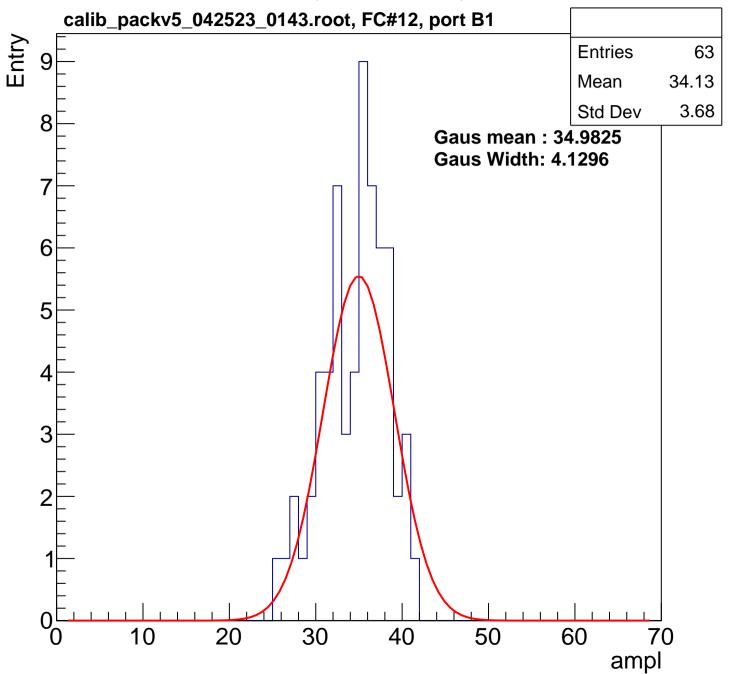


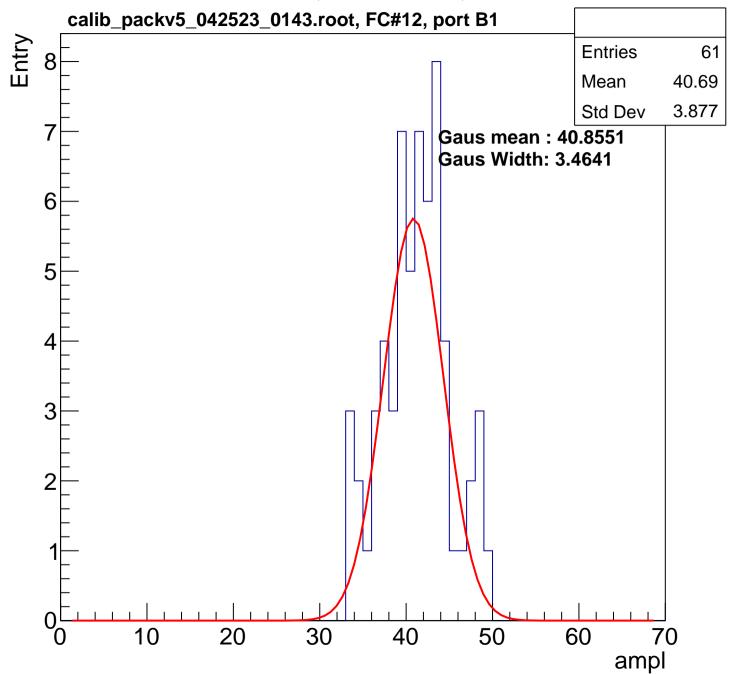


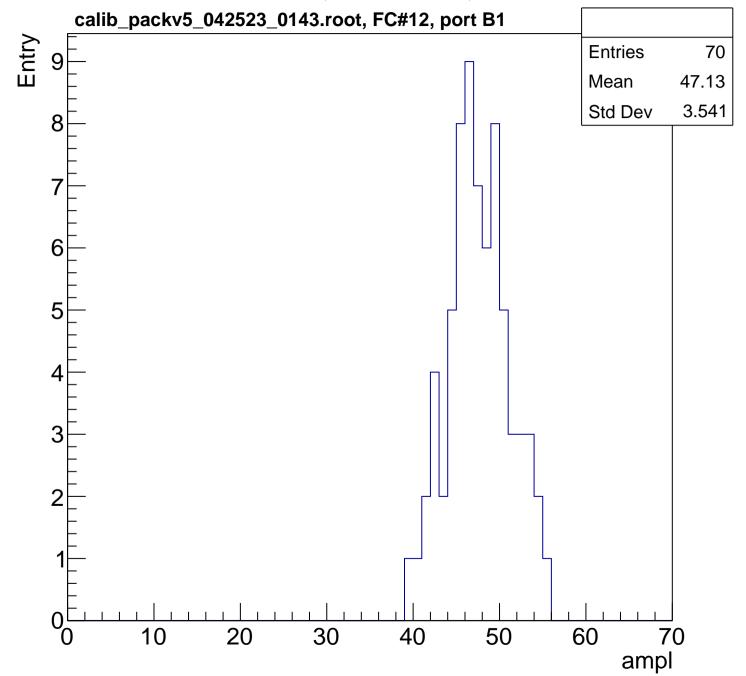


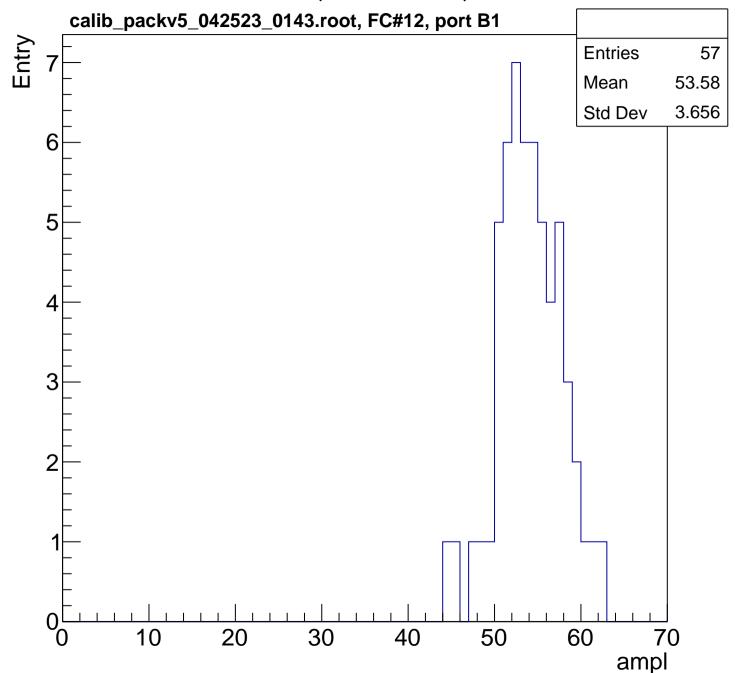


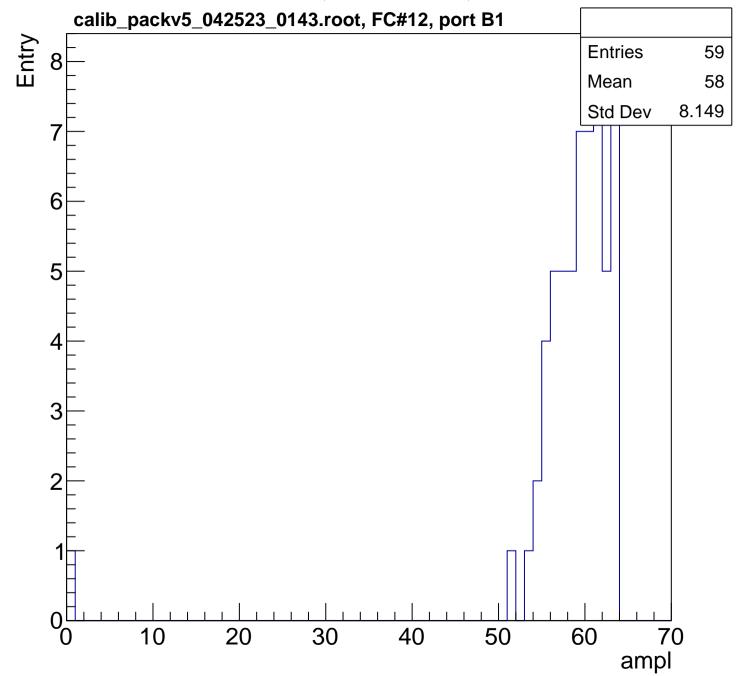


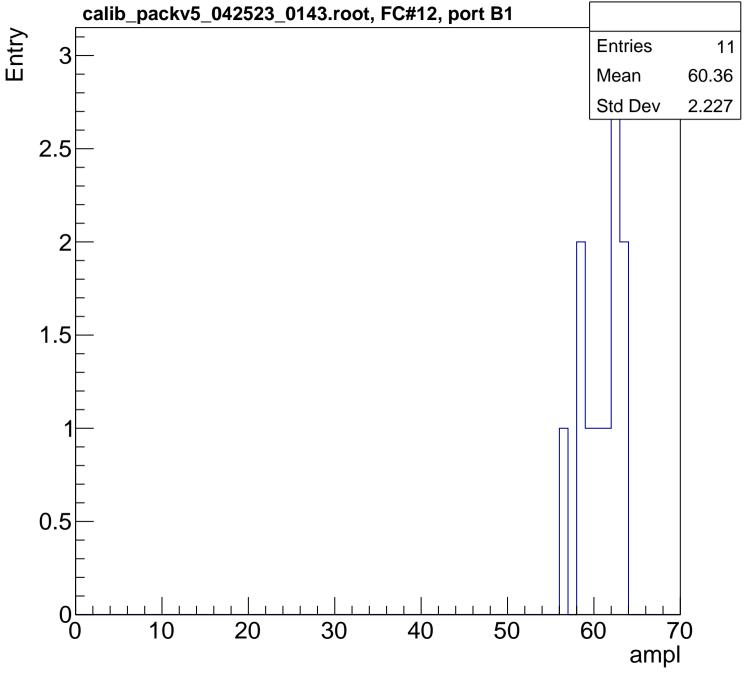


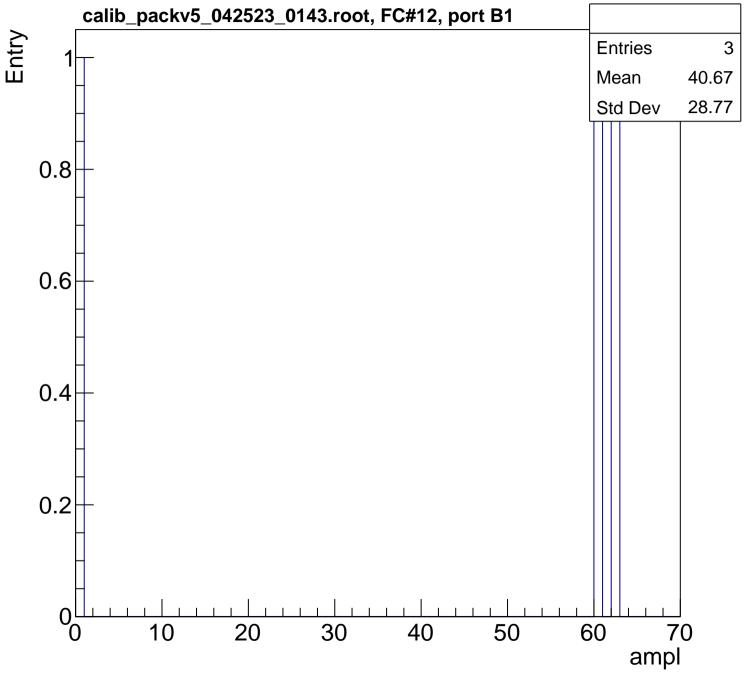


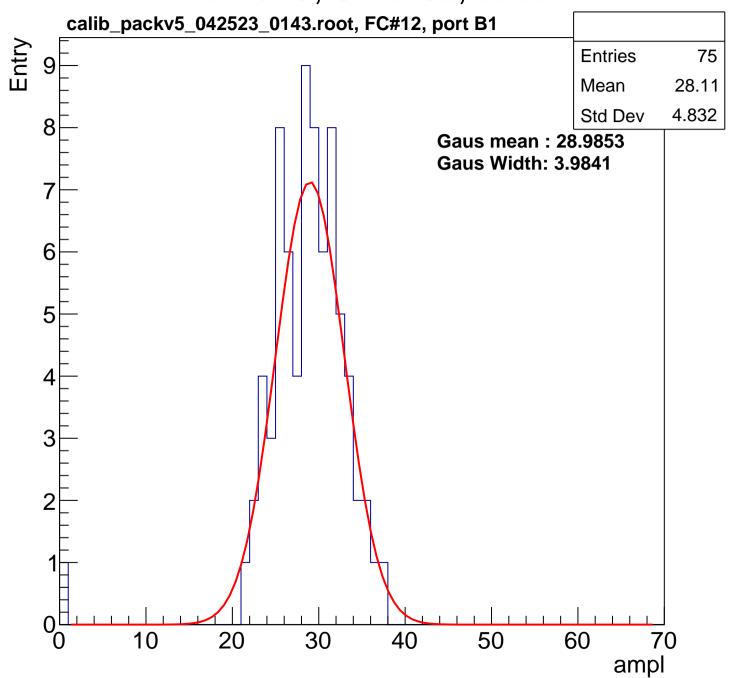


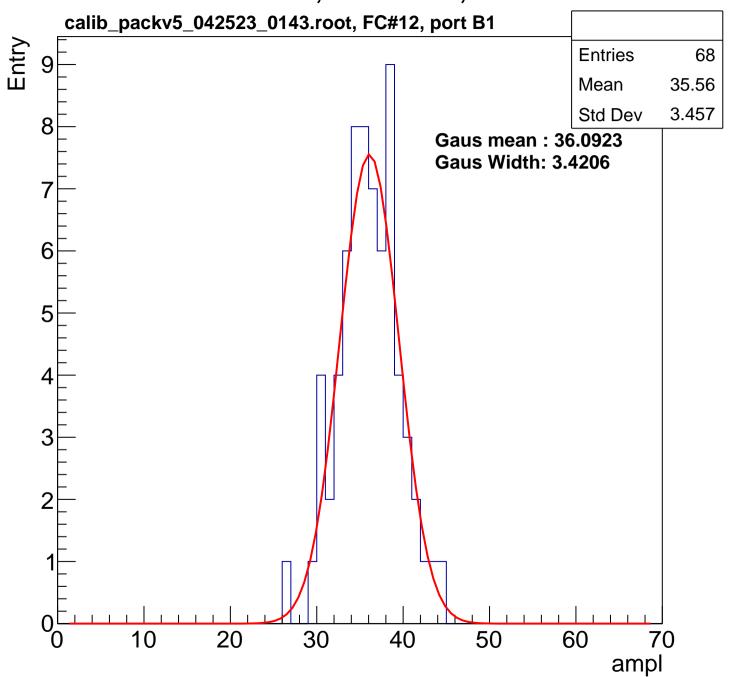


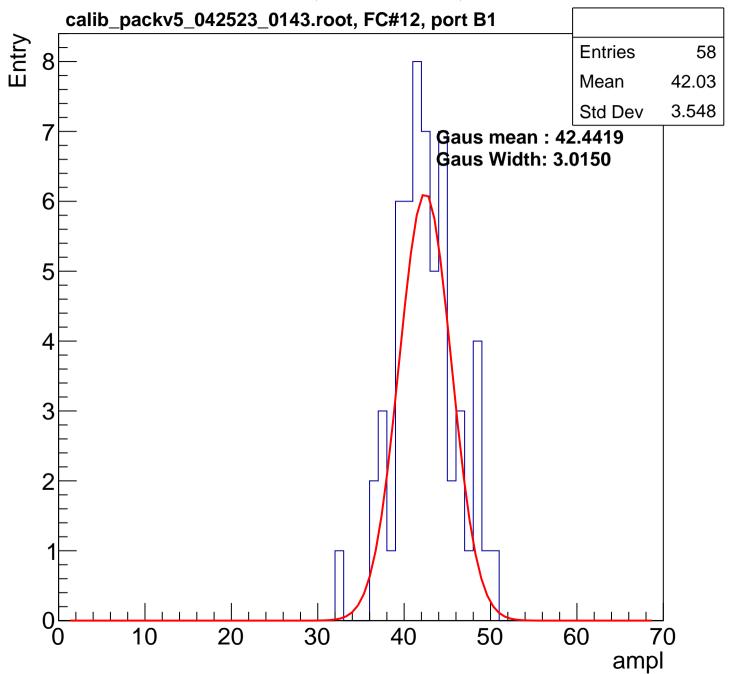


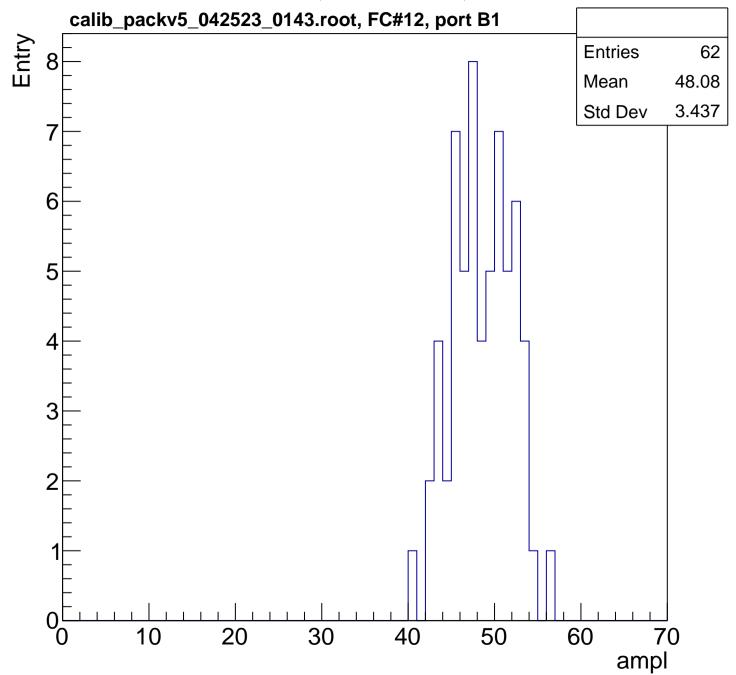


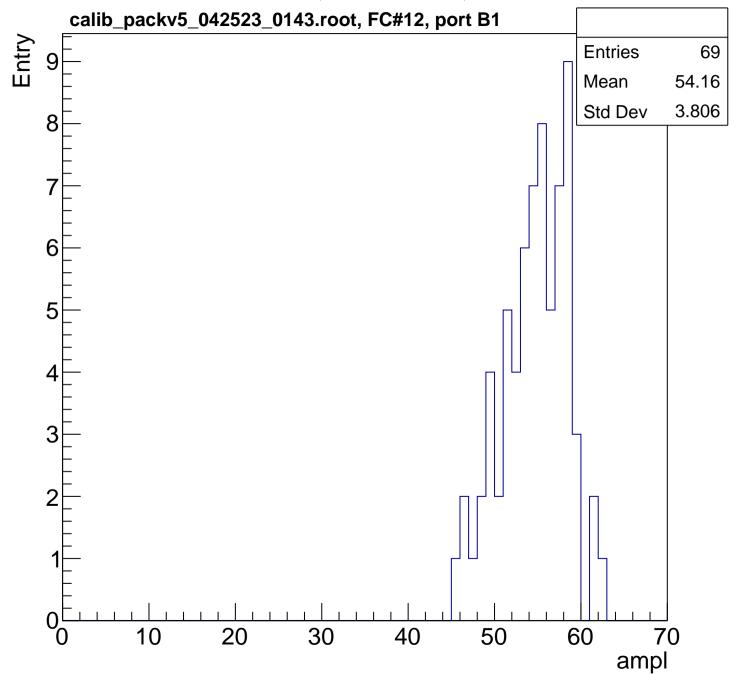


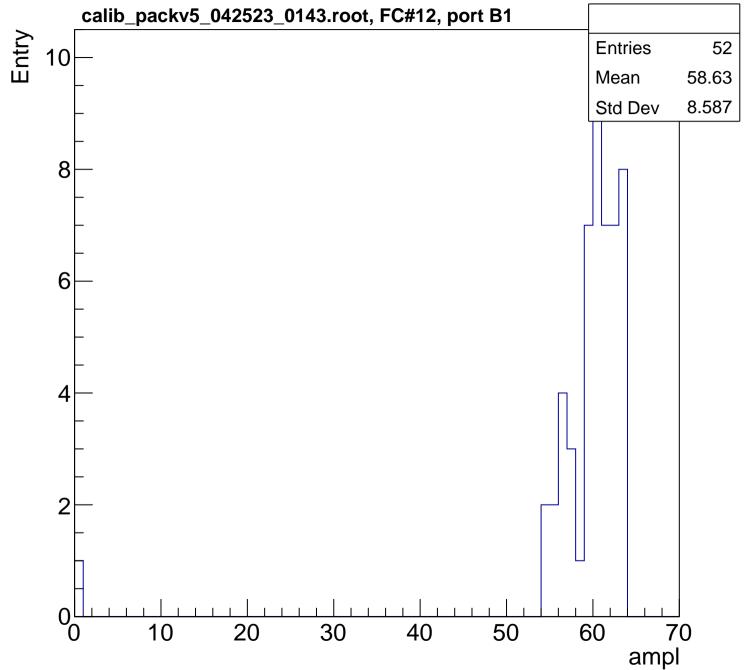


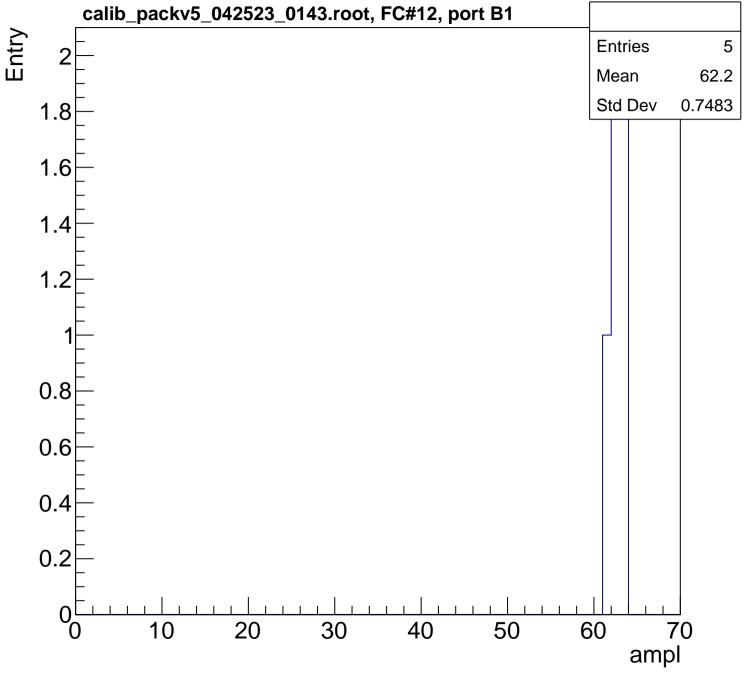




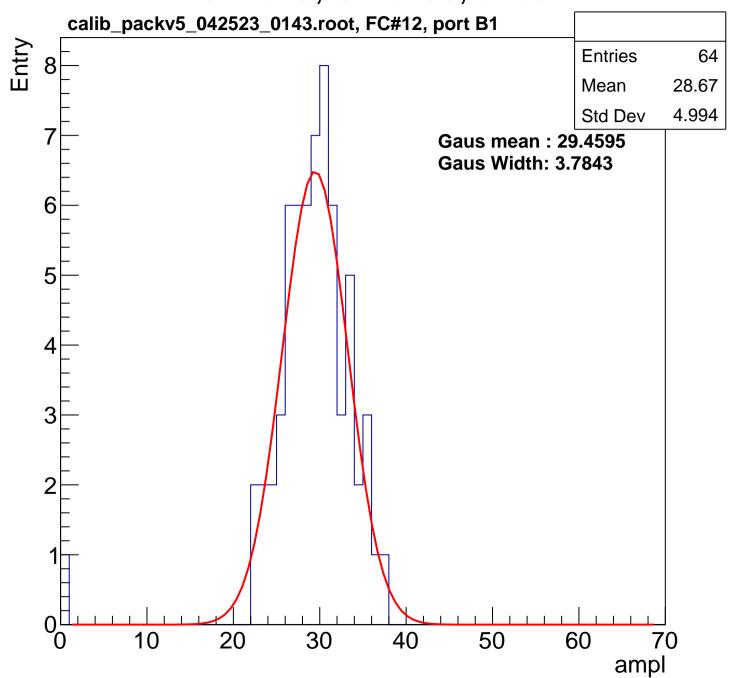


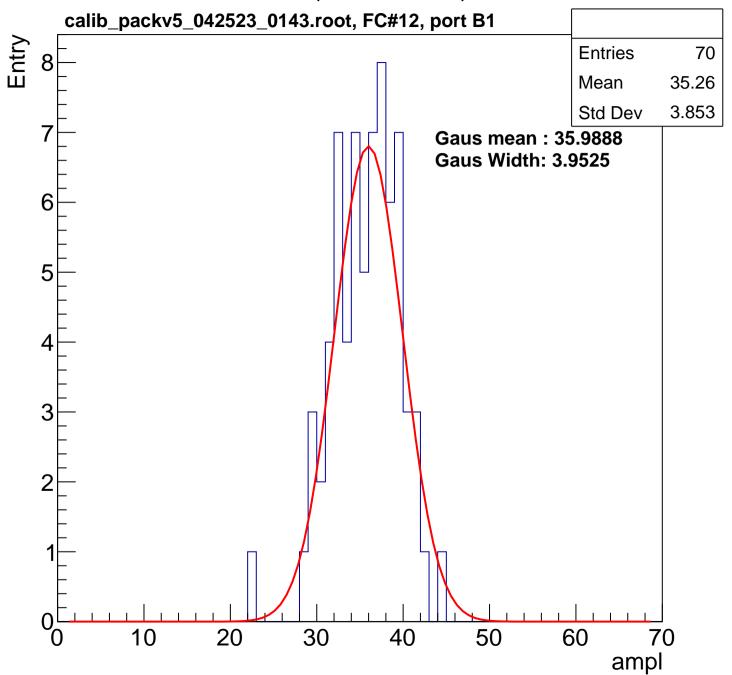


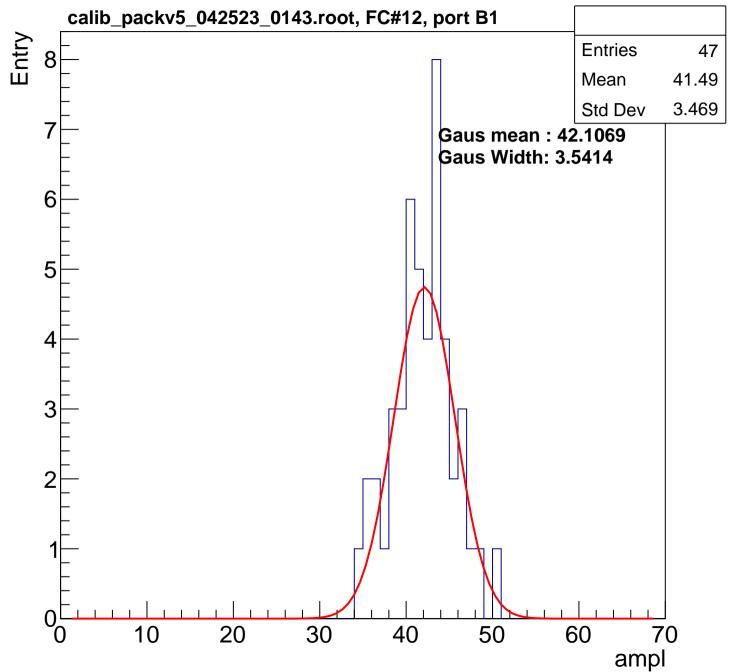


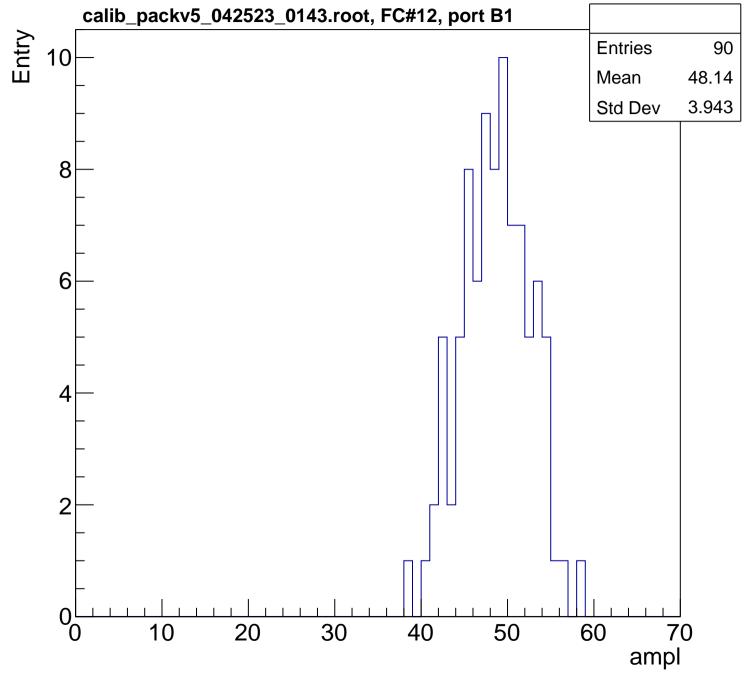


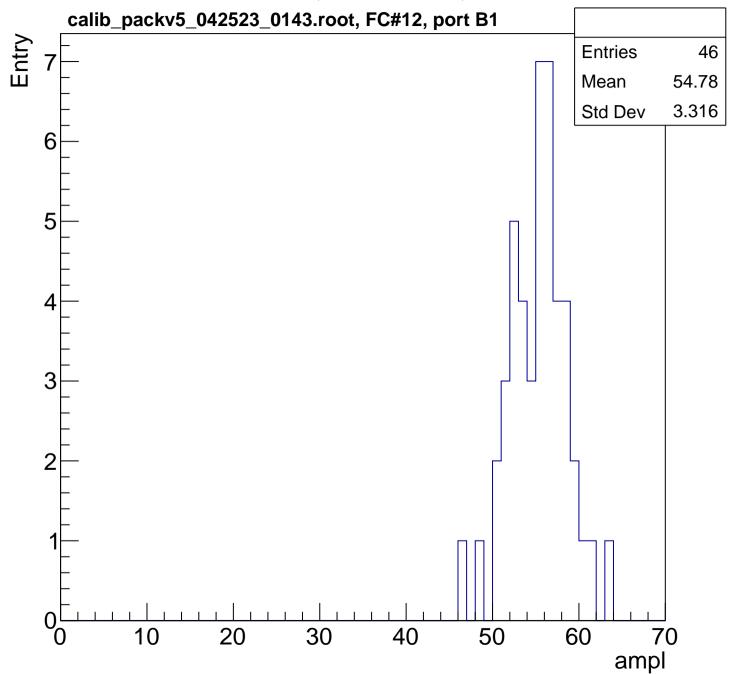


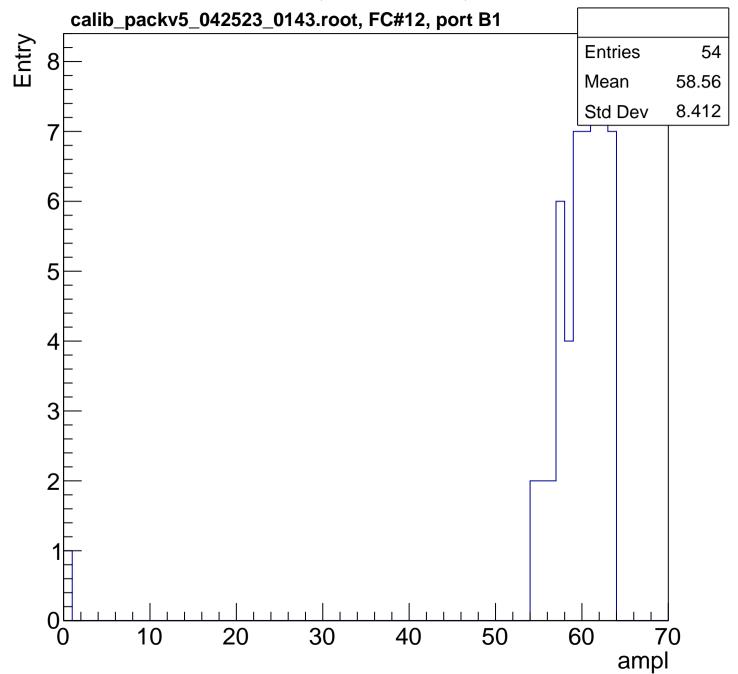


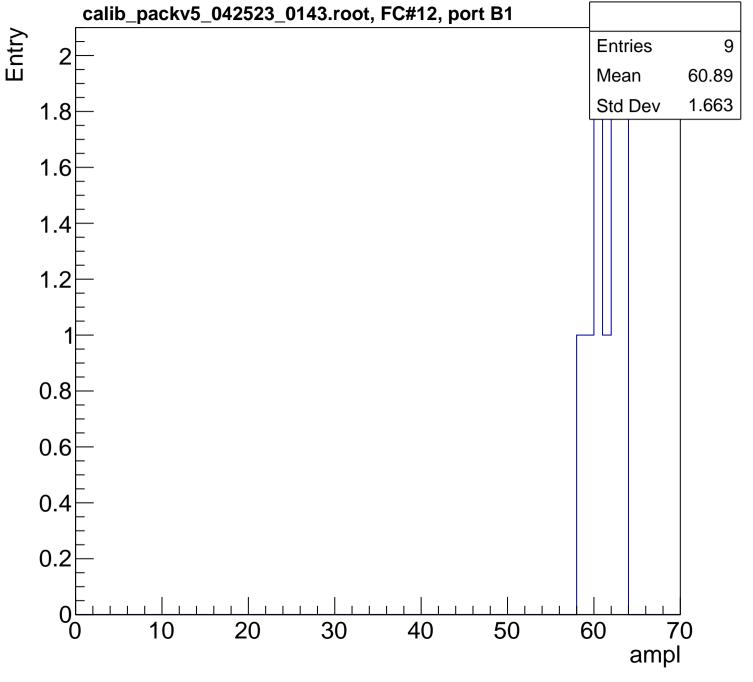


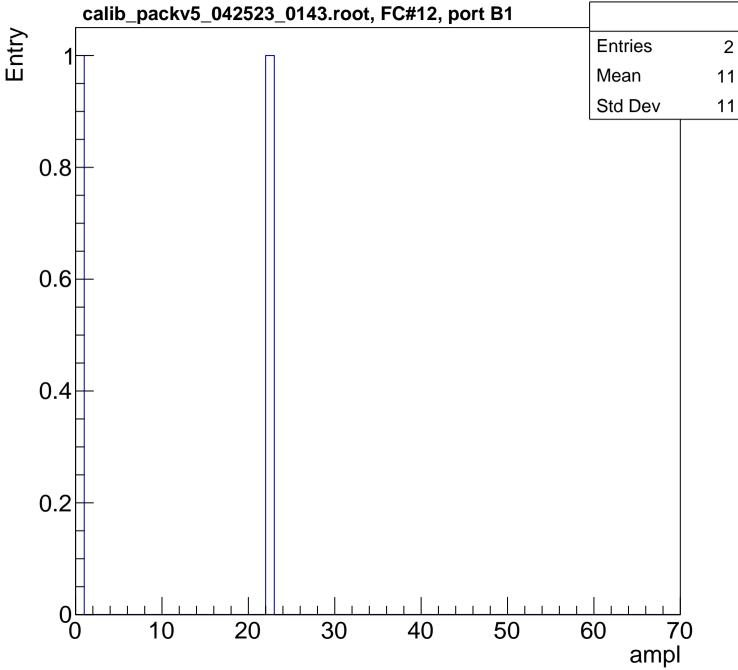


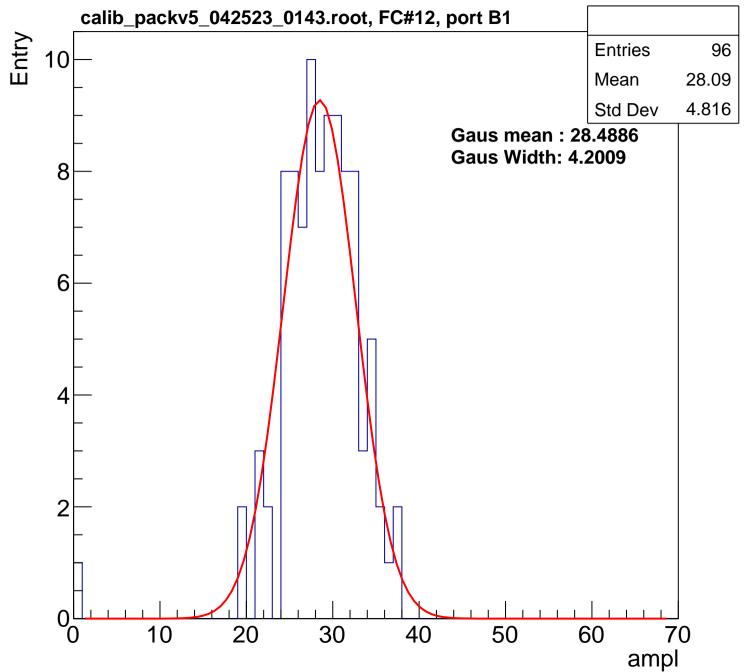


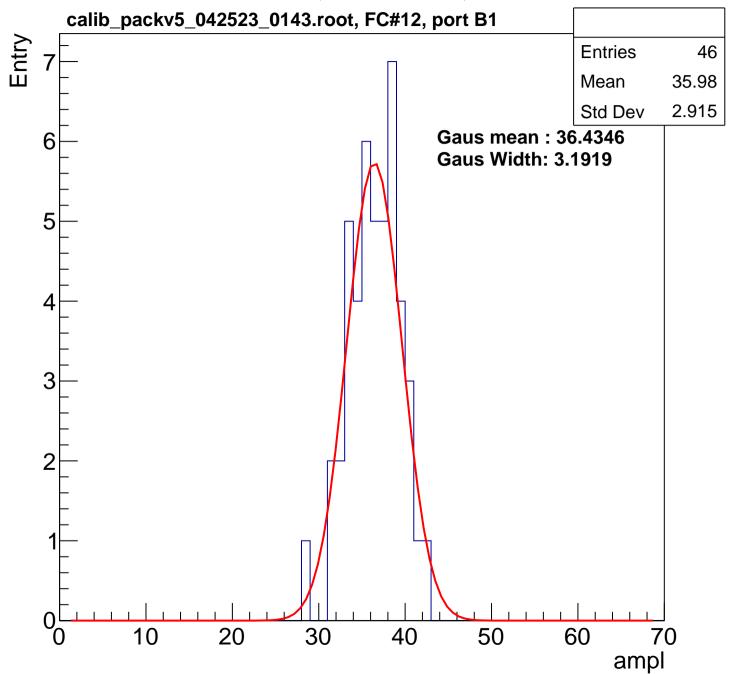


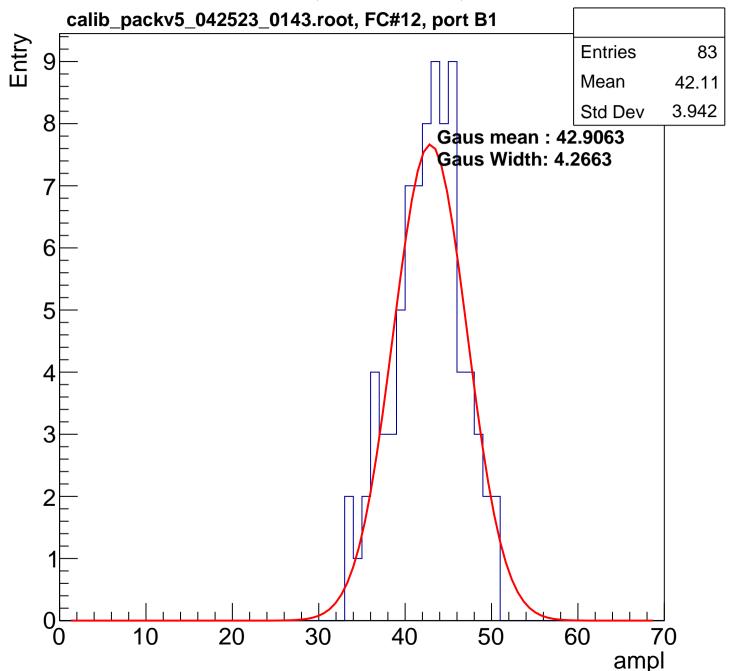


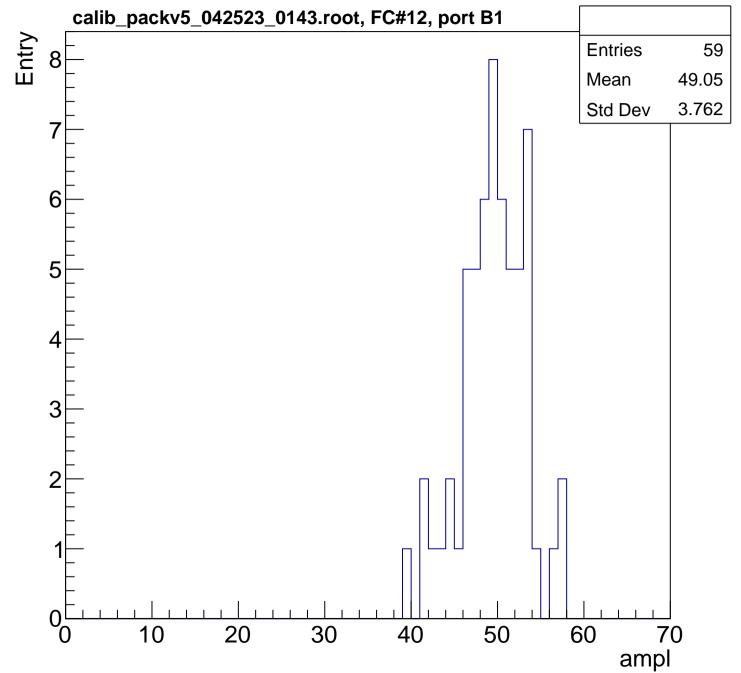


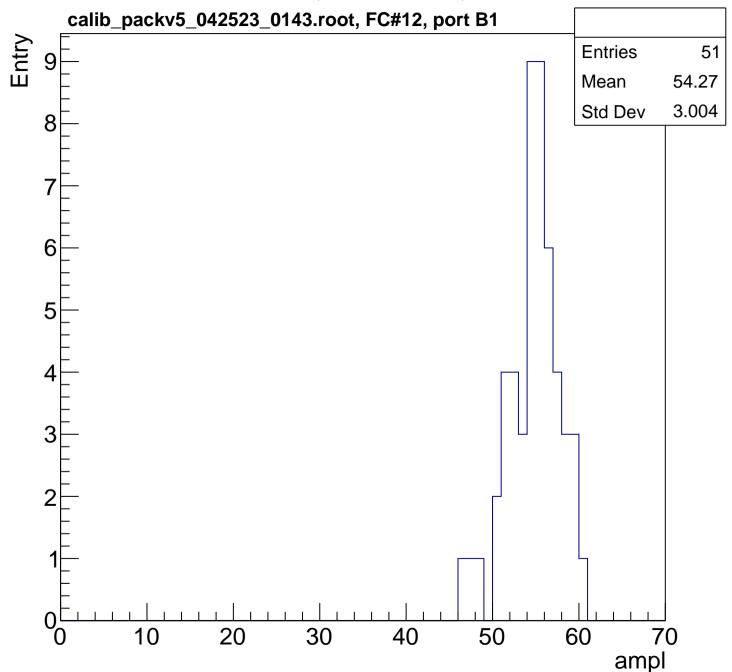


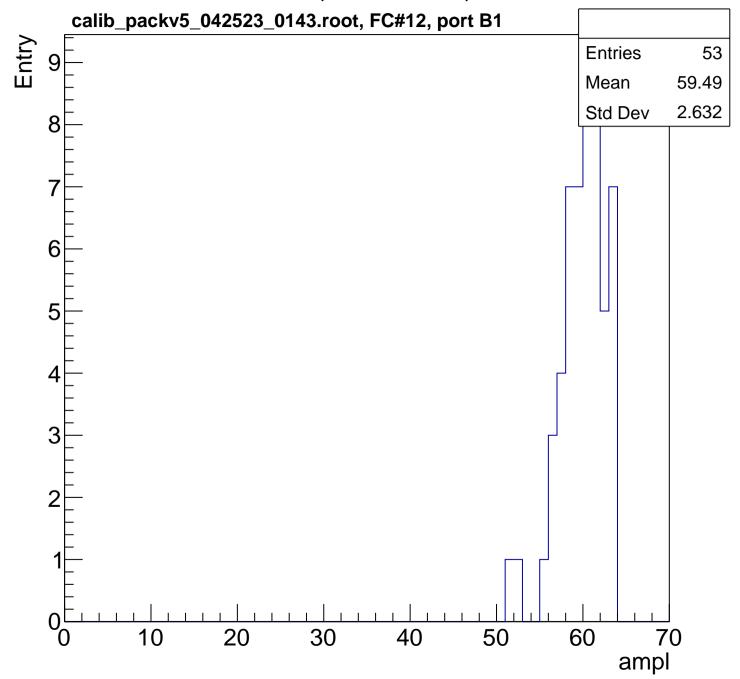


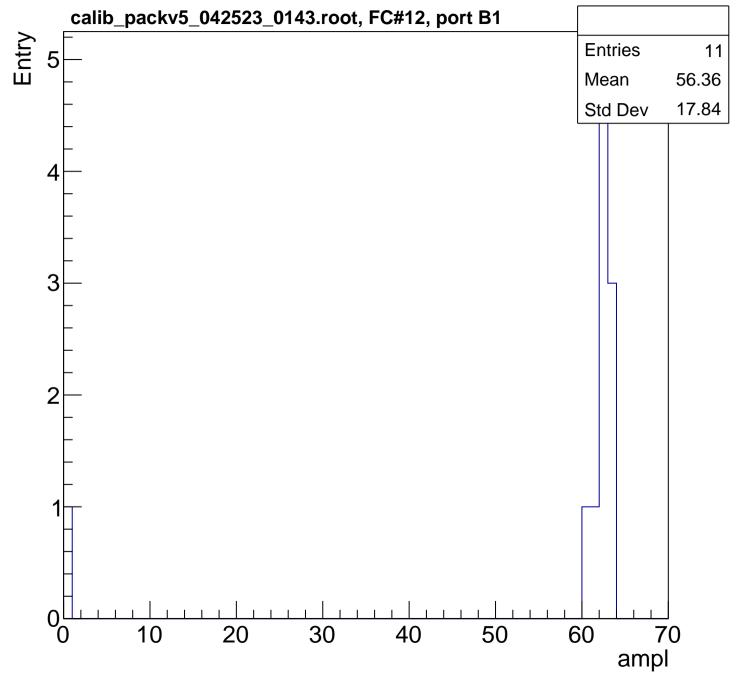




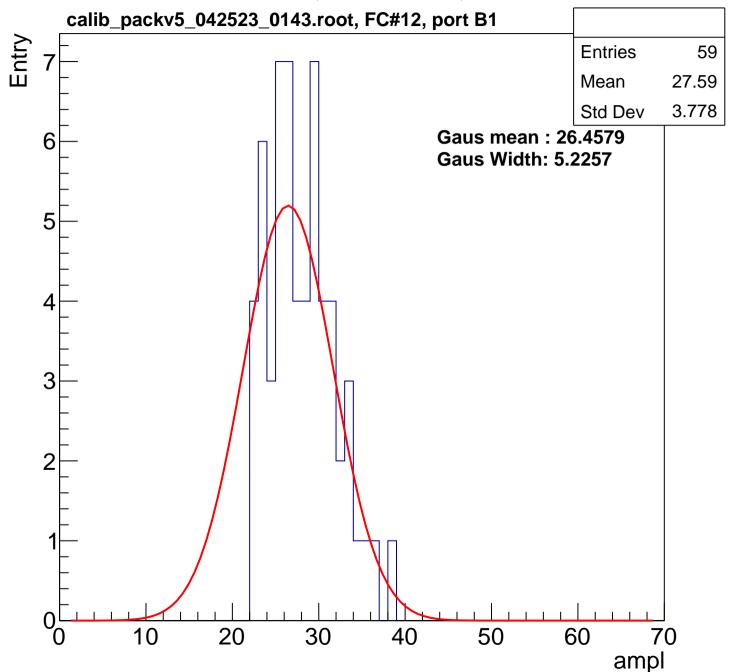


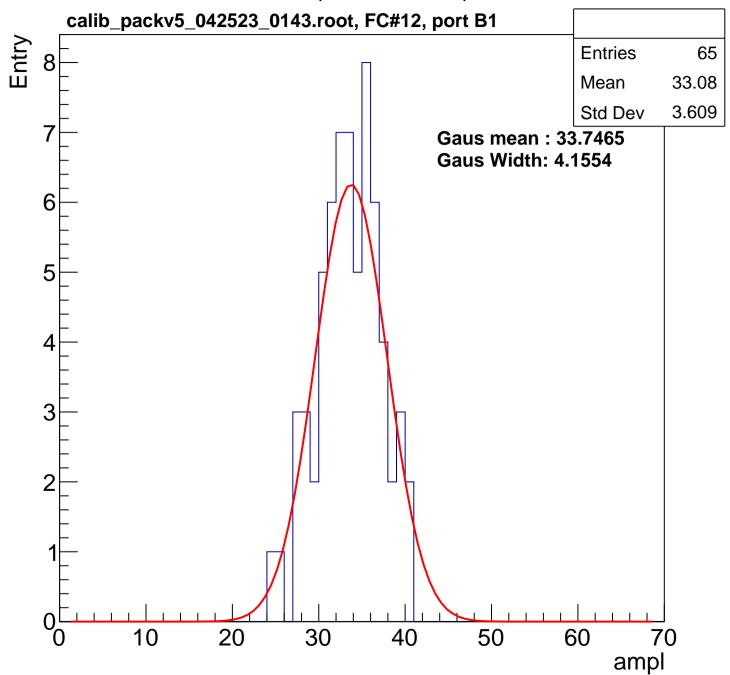


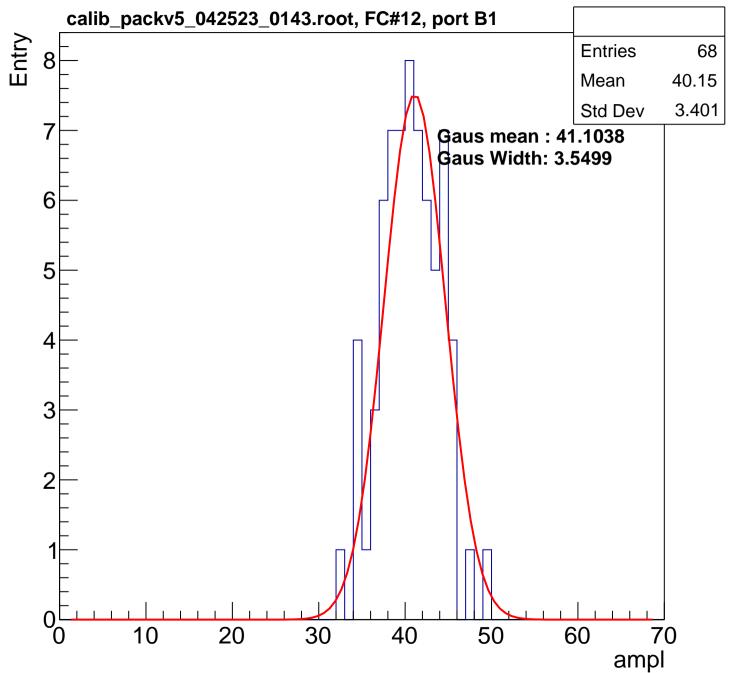


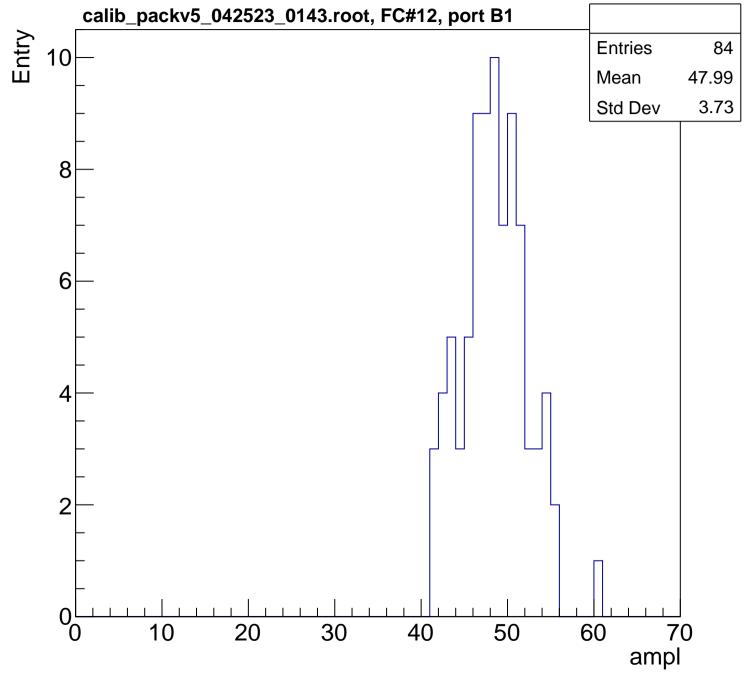


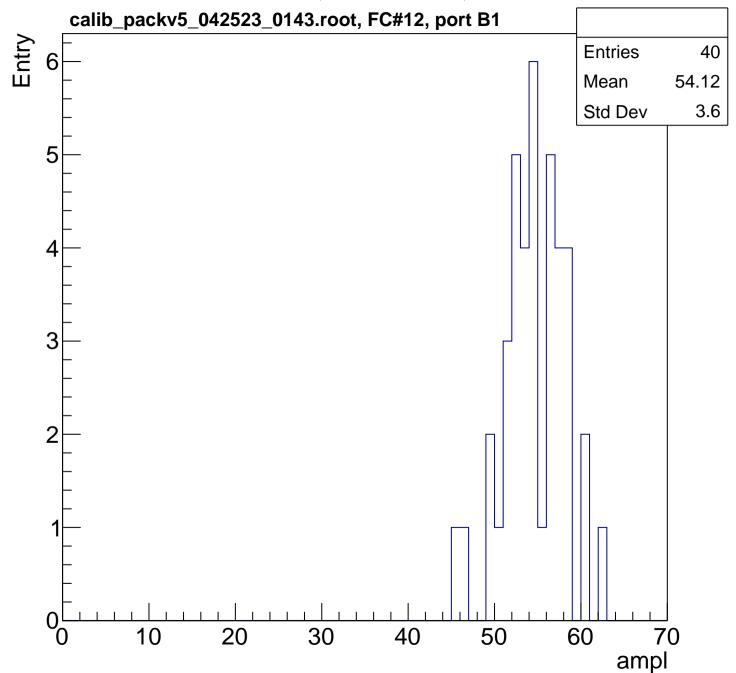


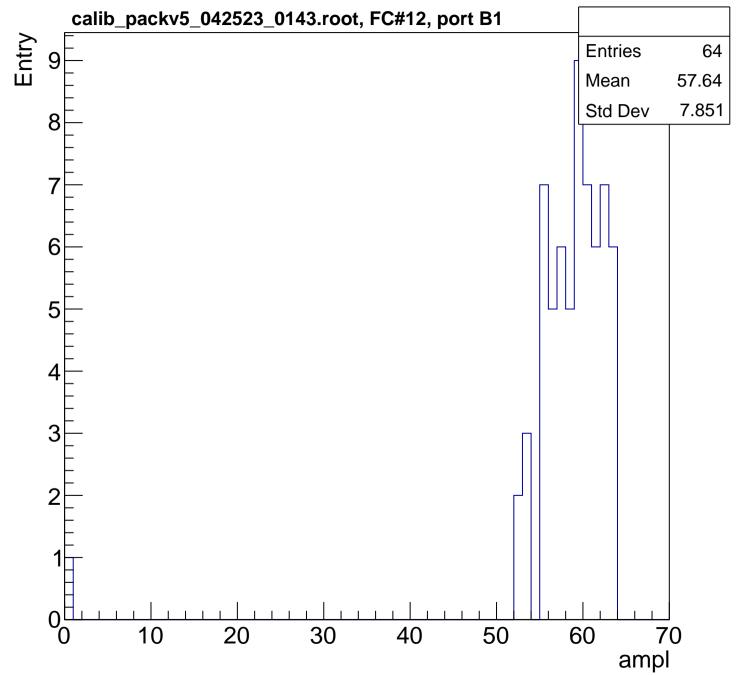


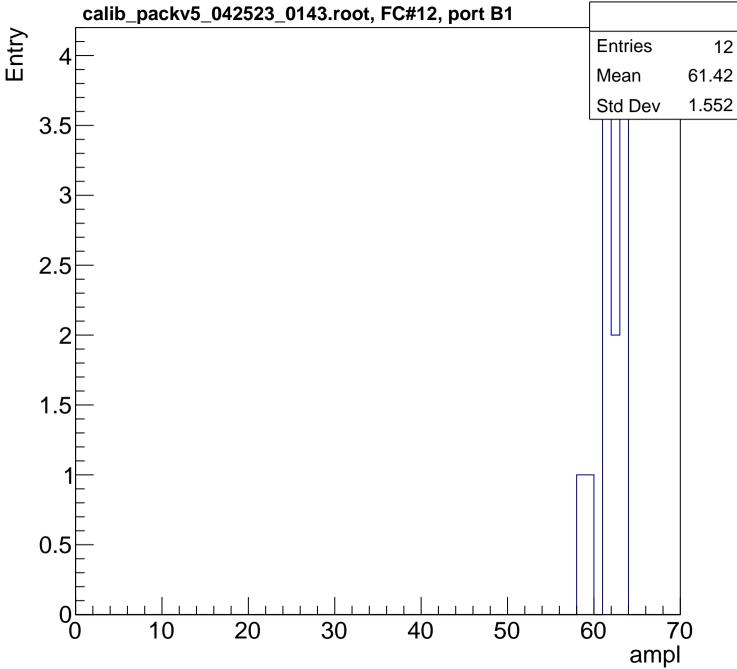


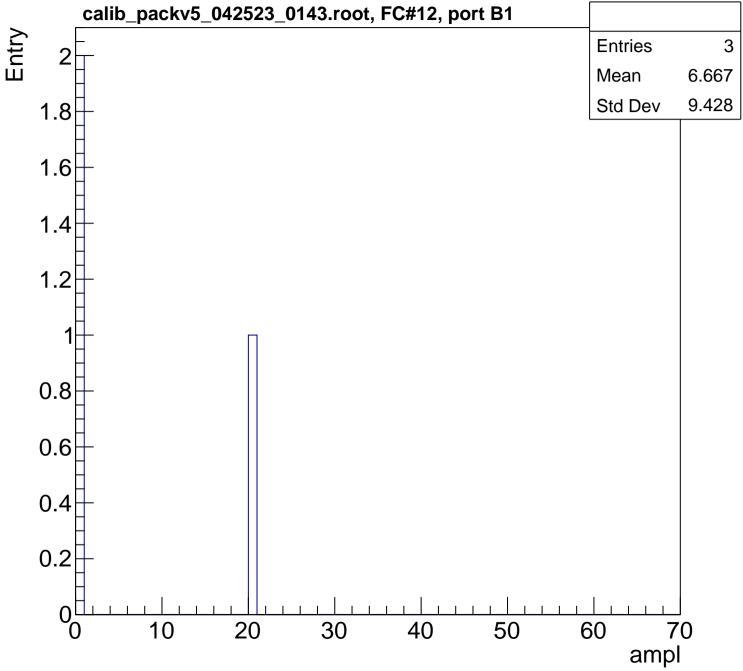


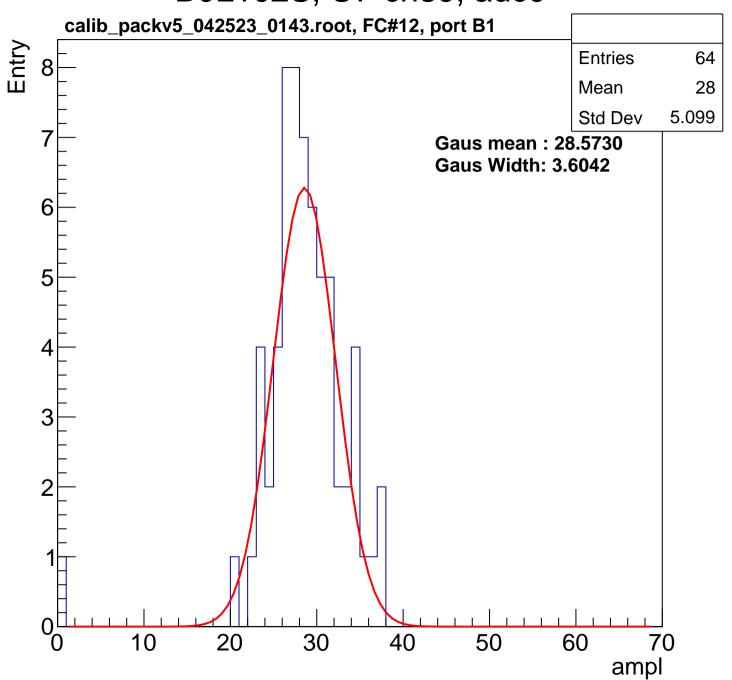


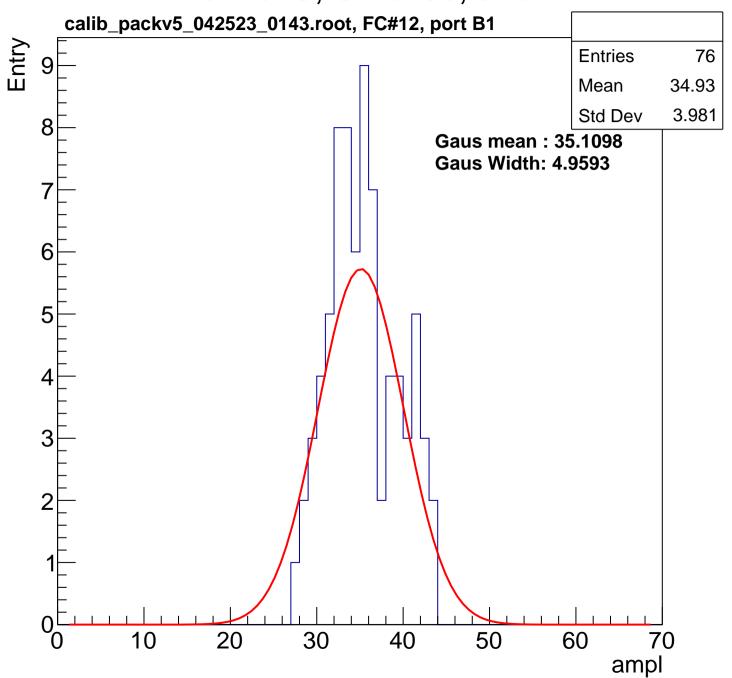


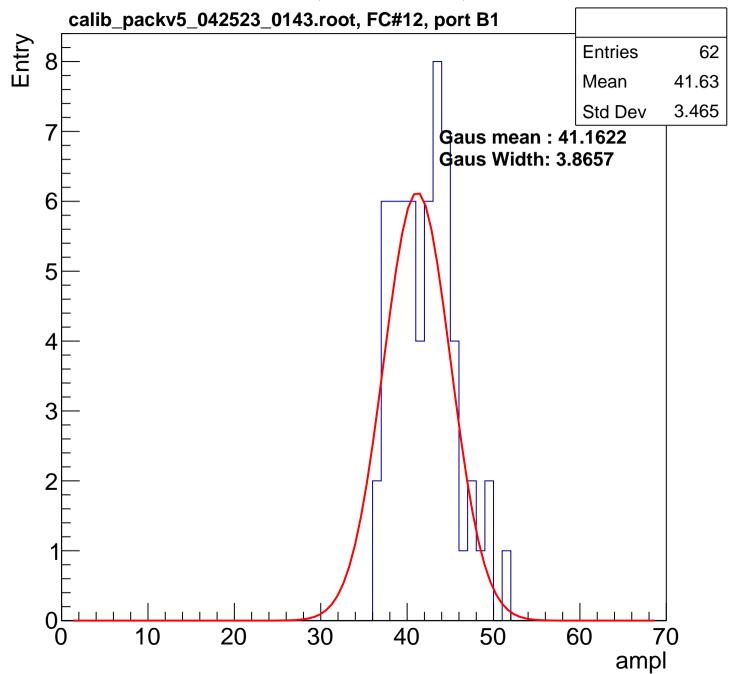


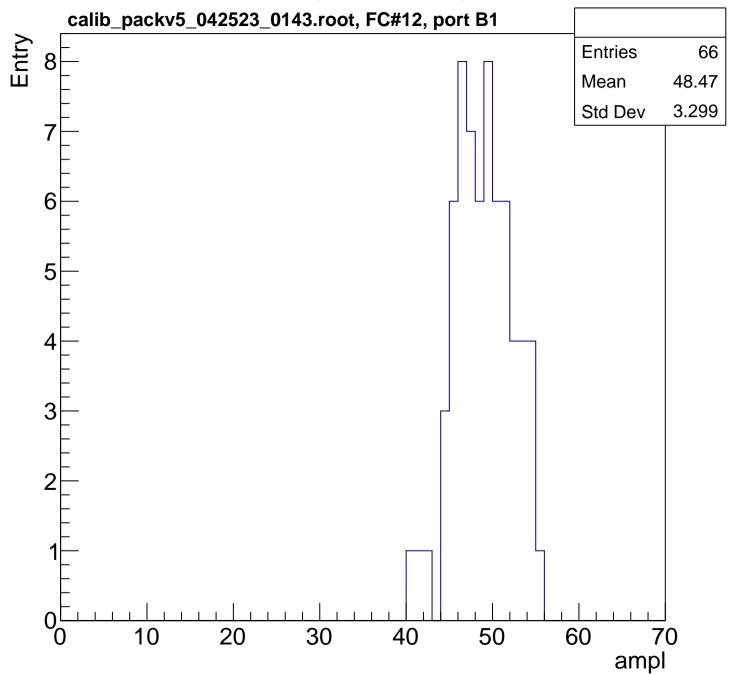


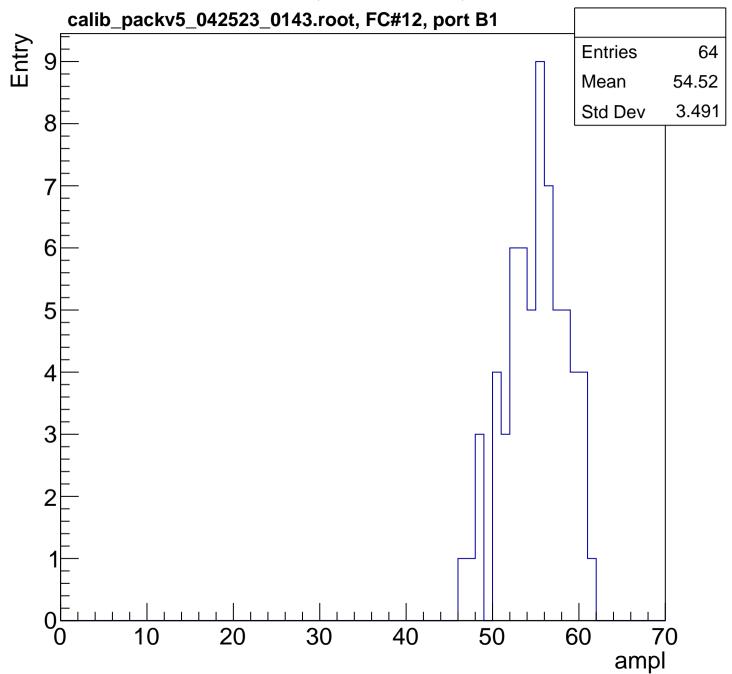


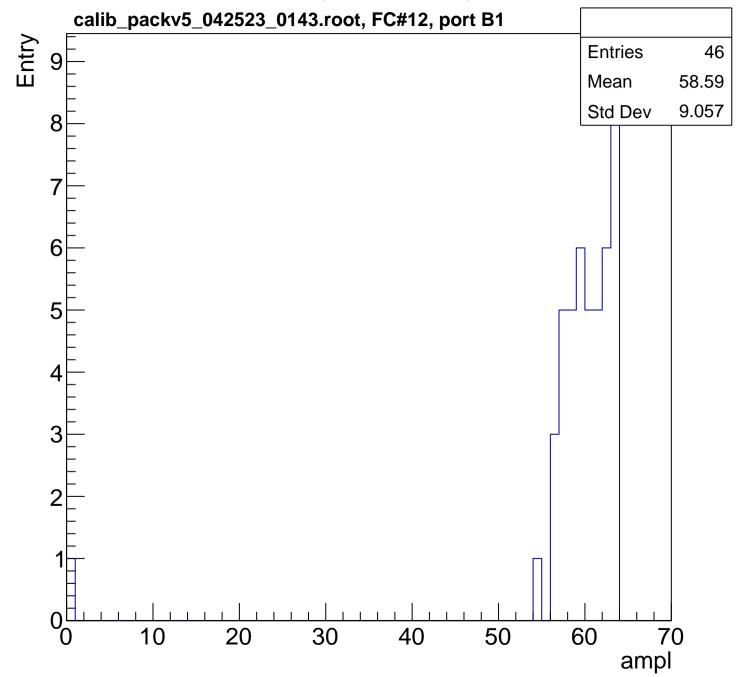


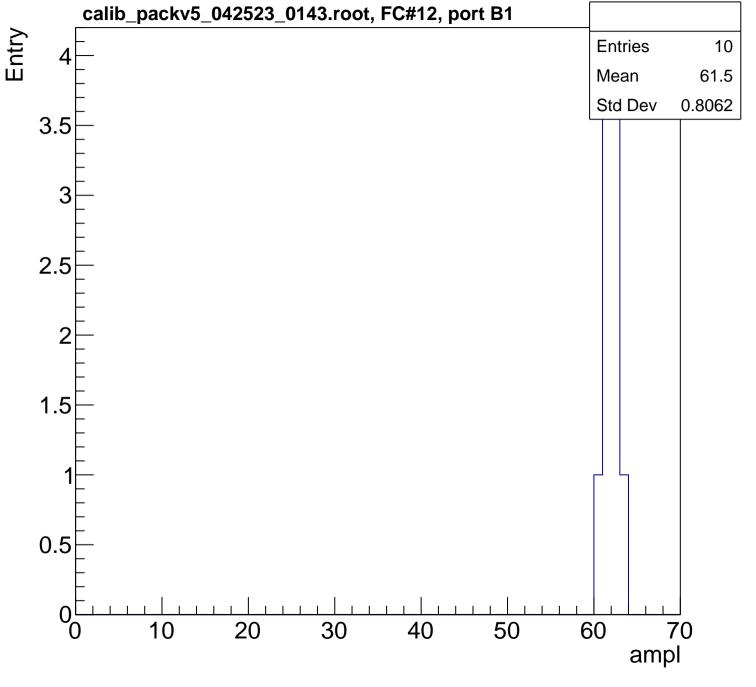




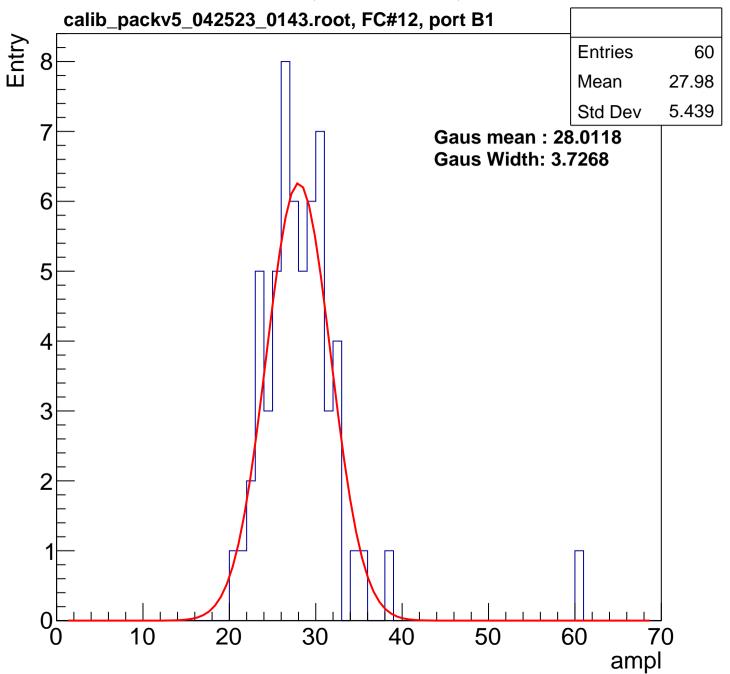


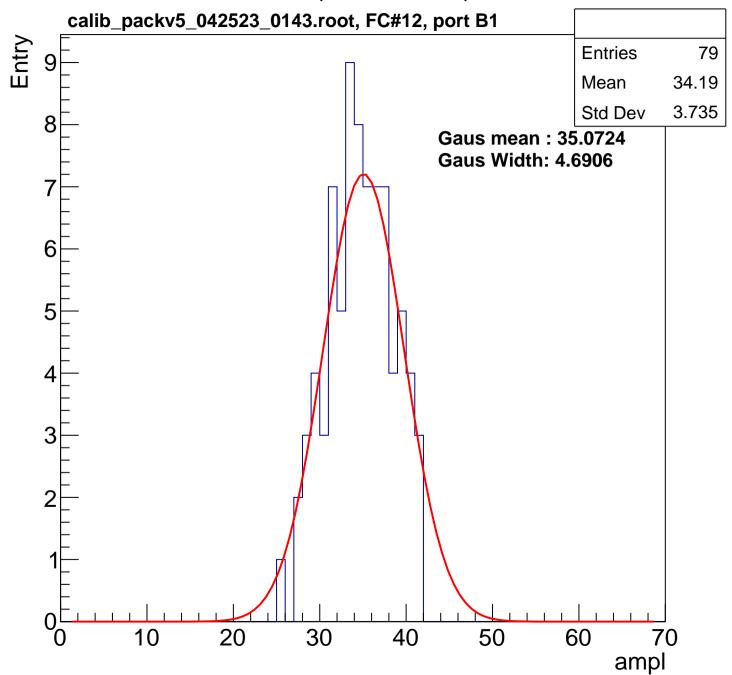


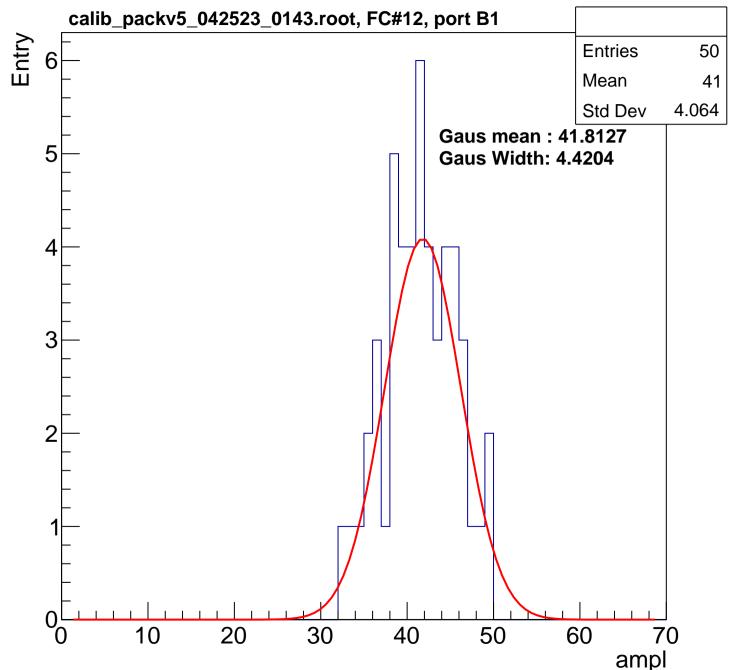


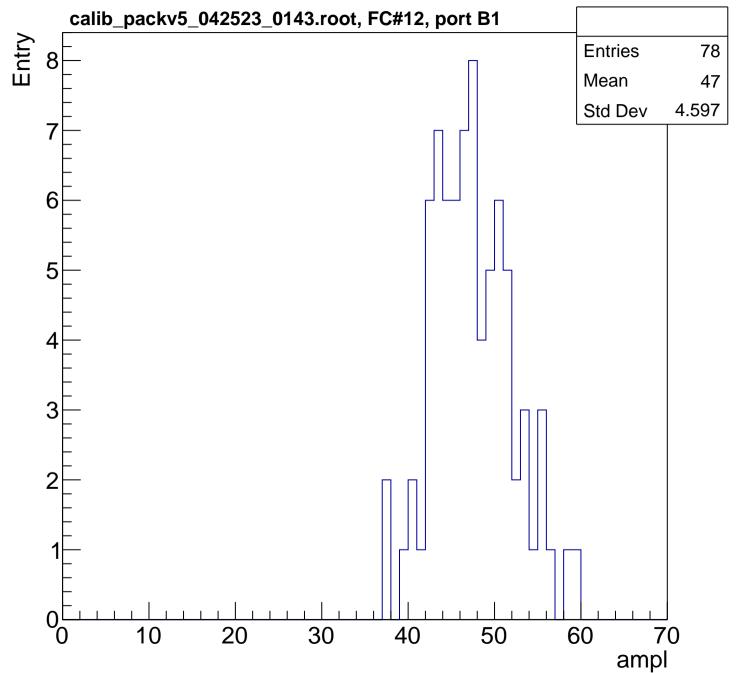


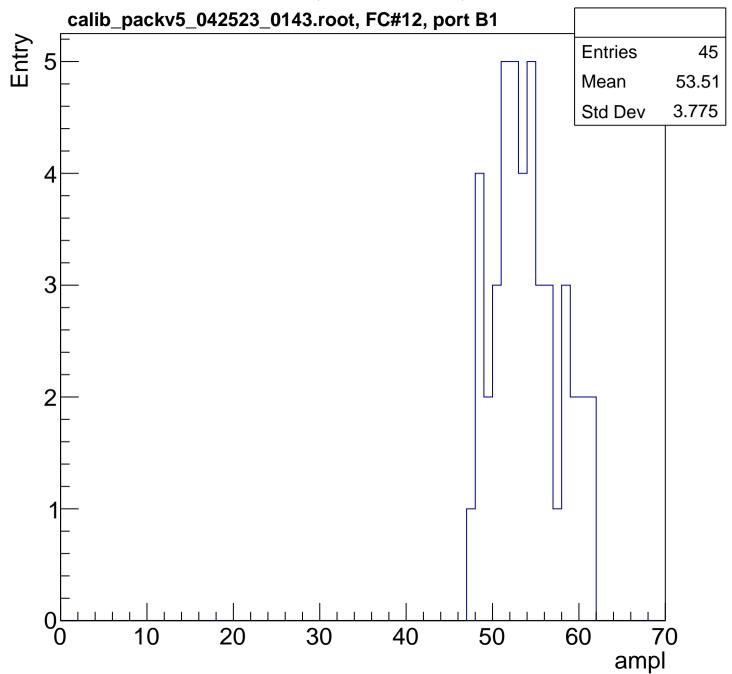
B0L102S, U7-ch89, adc7 calib_packv5_042523_0143.root, FC#12, port B1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

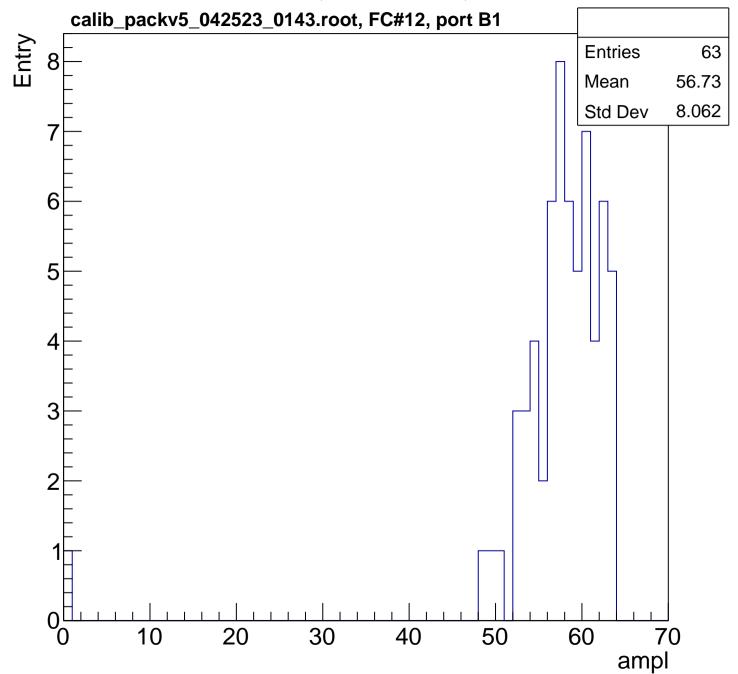


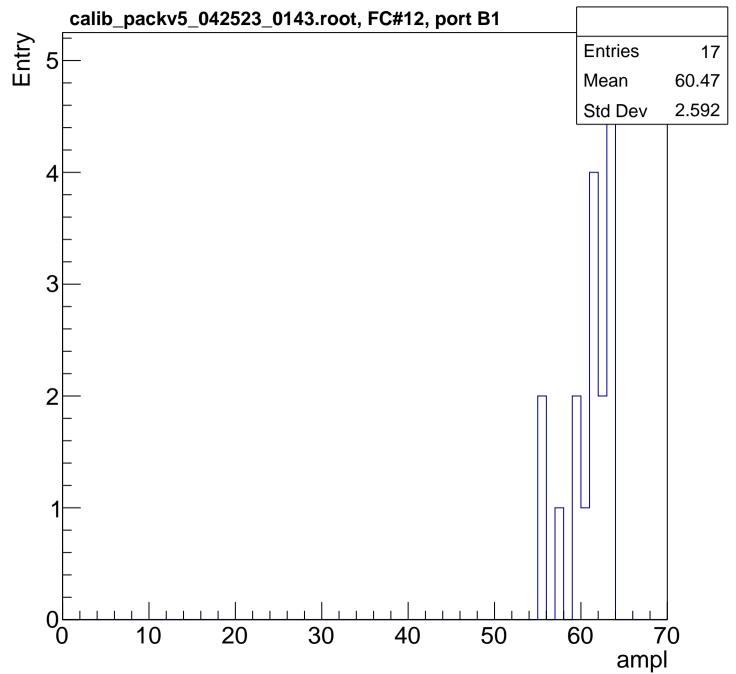


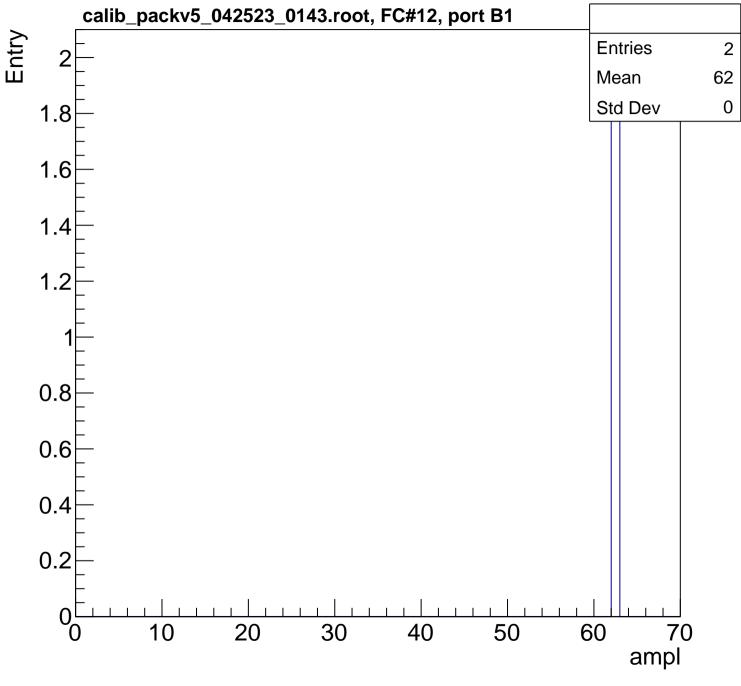


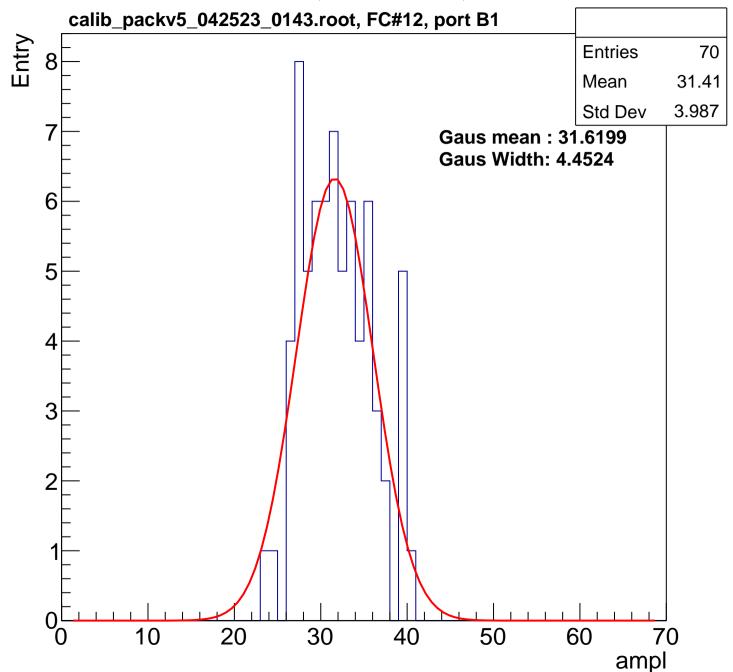


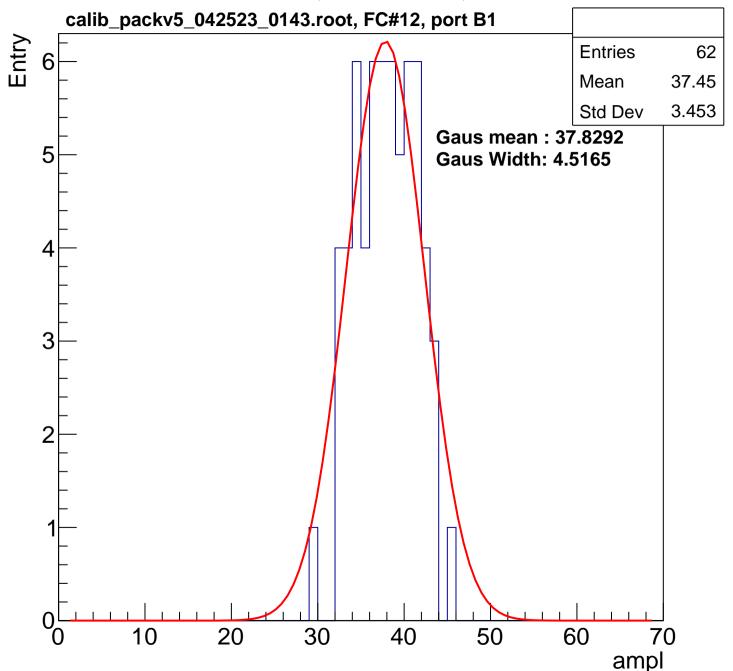


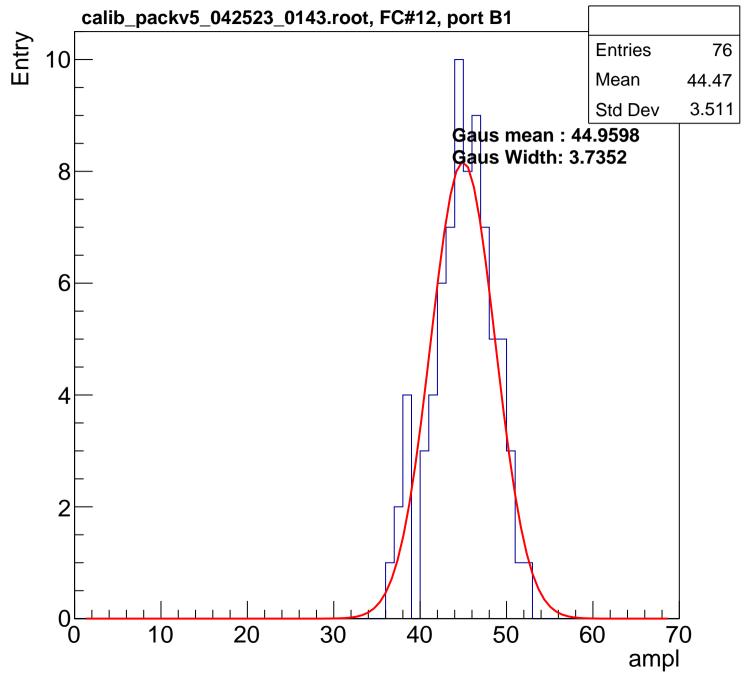


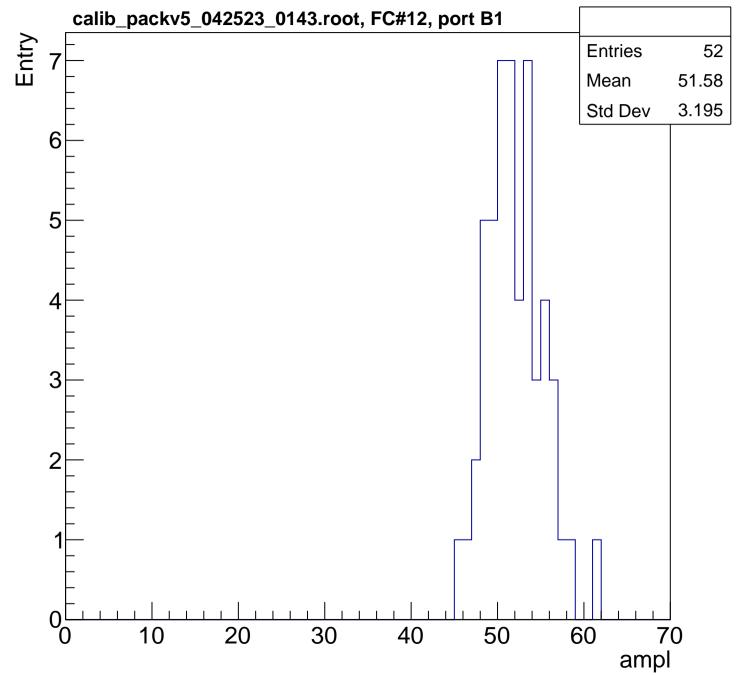


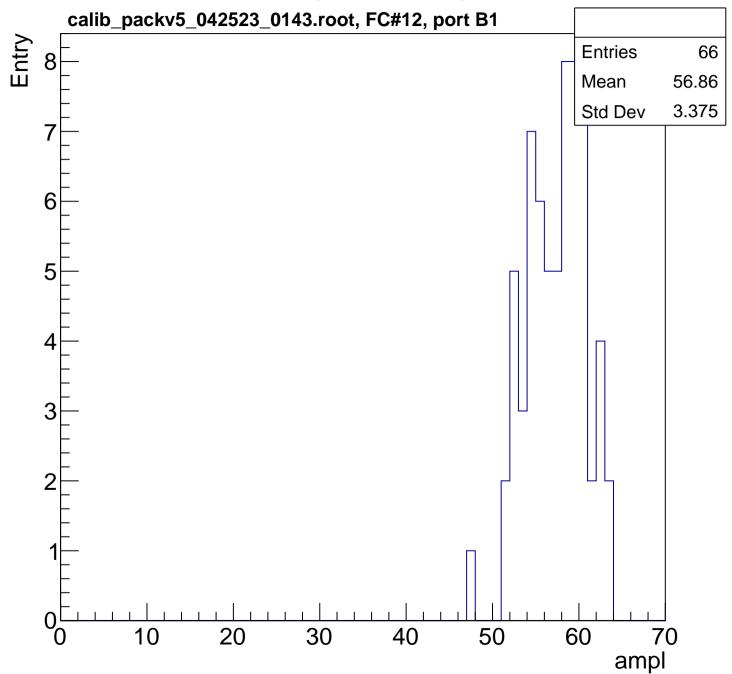


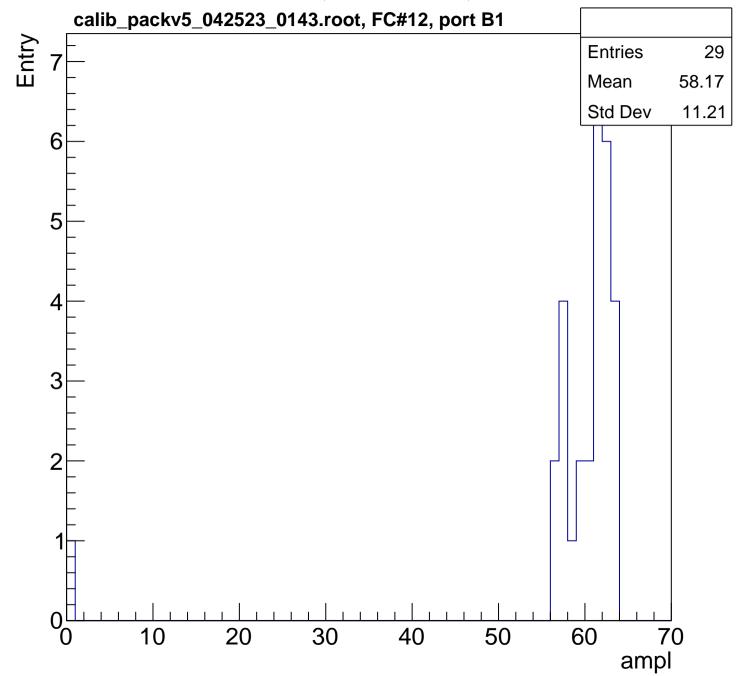


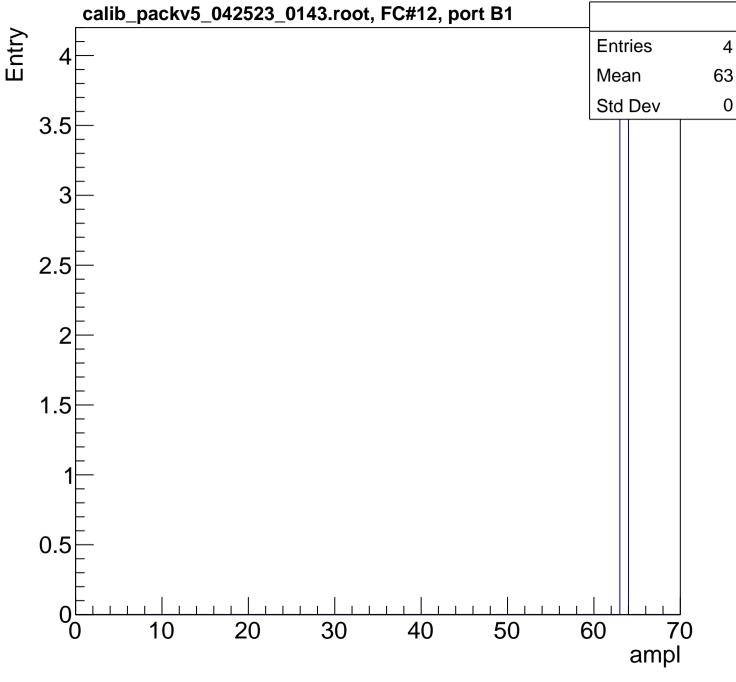




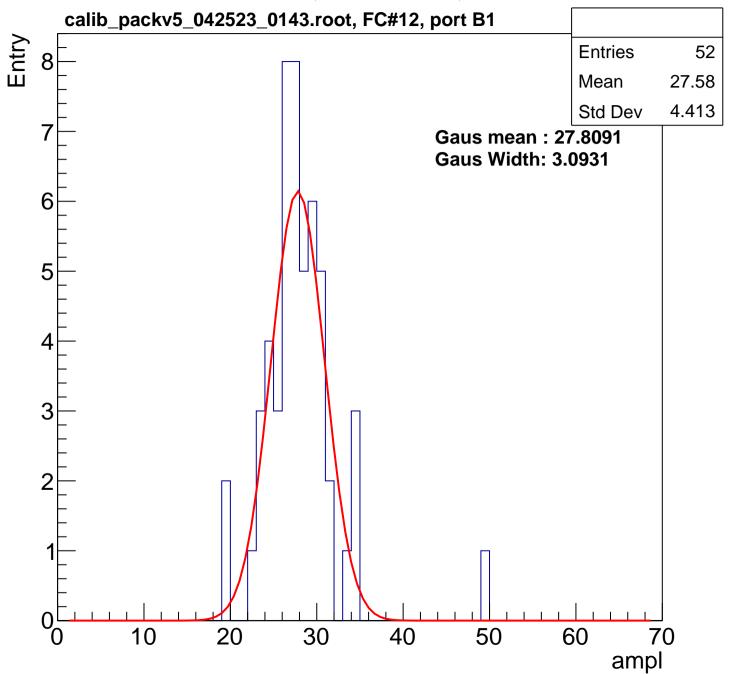


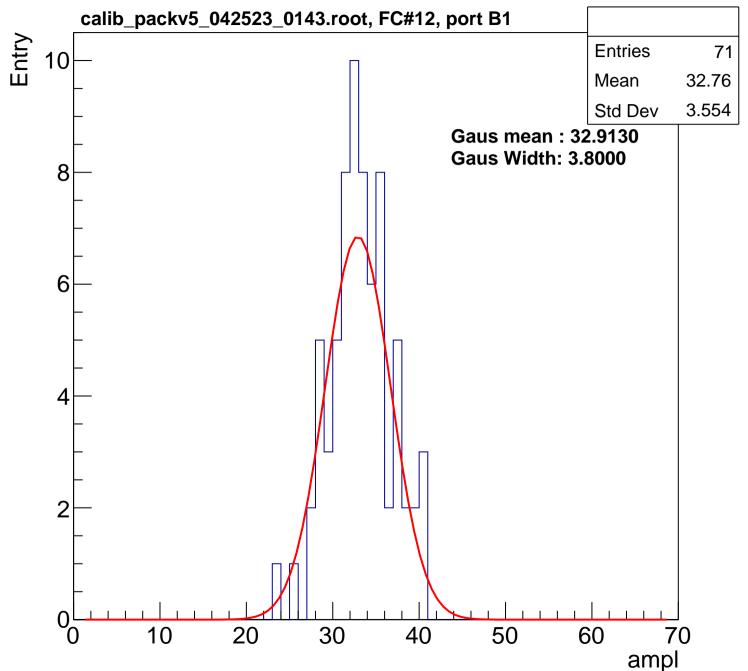


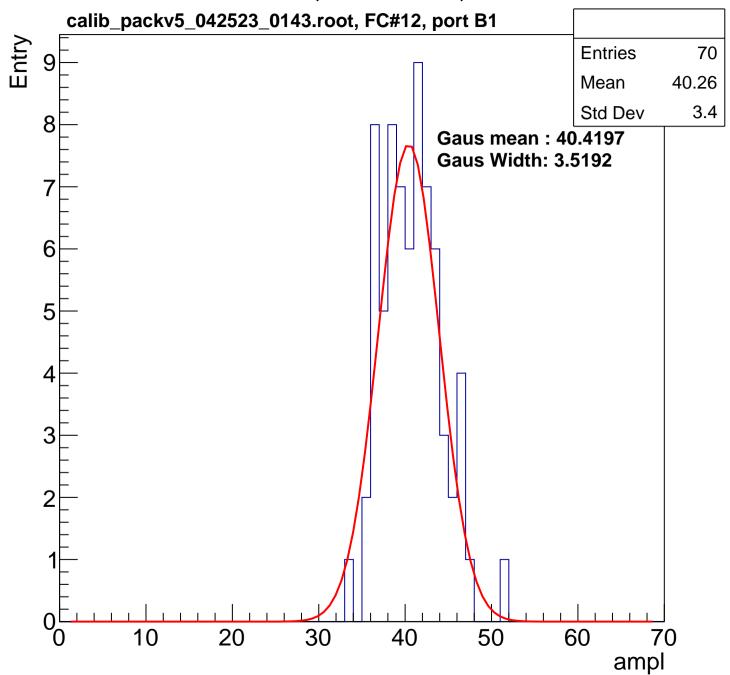


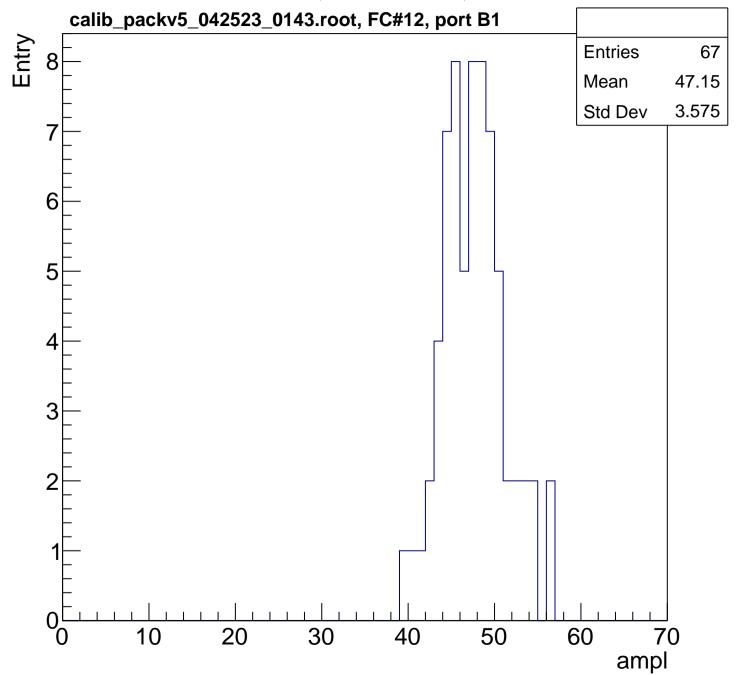


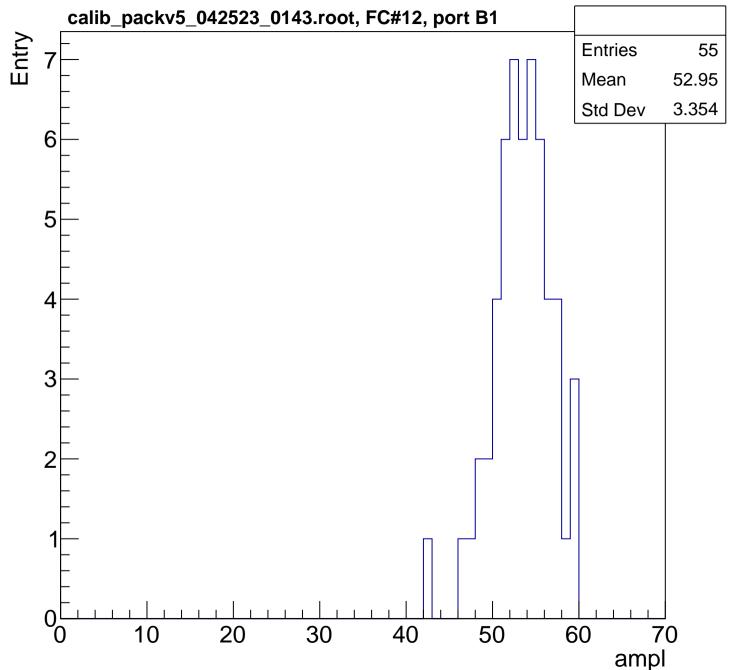


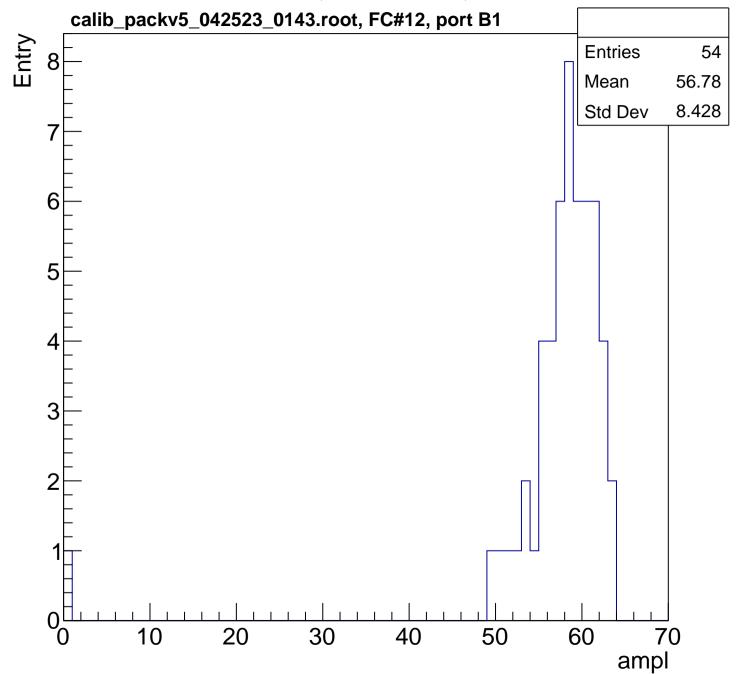


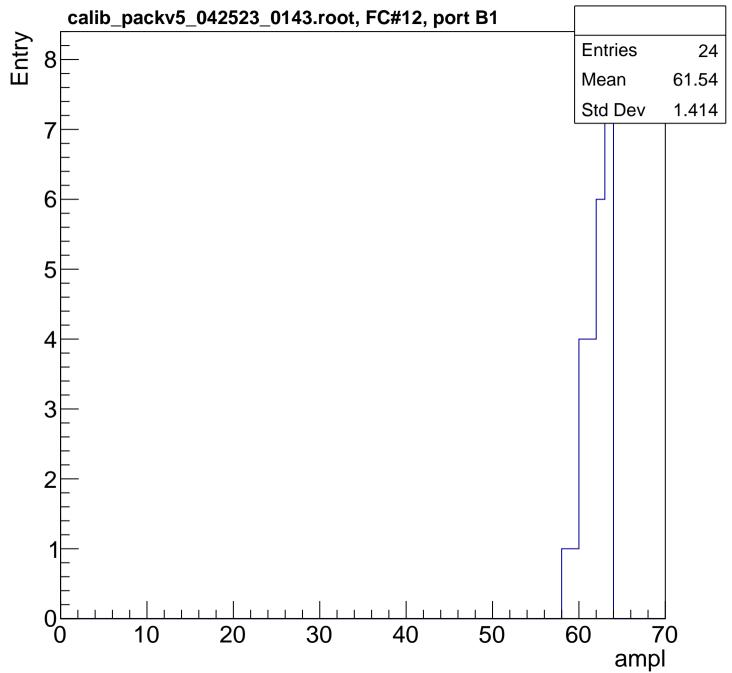












B0L102S, U7-ch92, adc7 calib_packv5_042523_0143.root, FC#12, port B1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70

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