



# B1L101S, U18-ch0, adc0

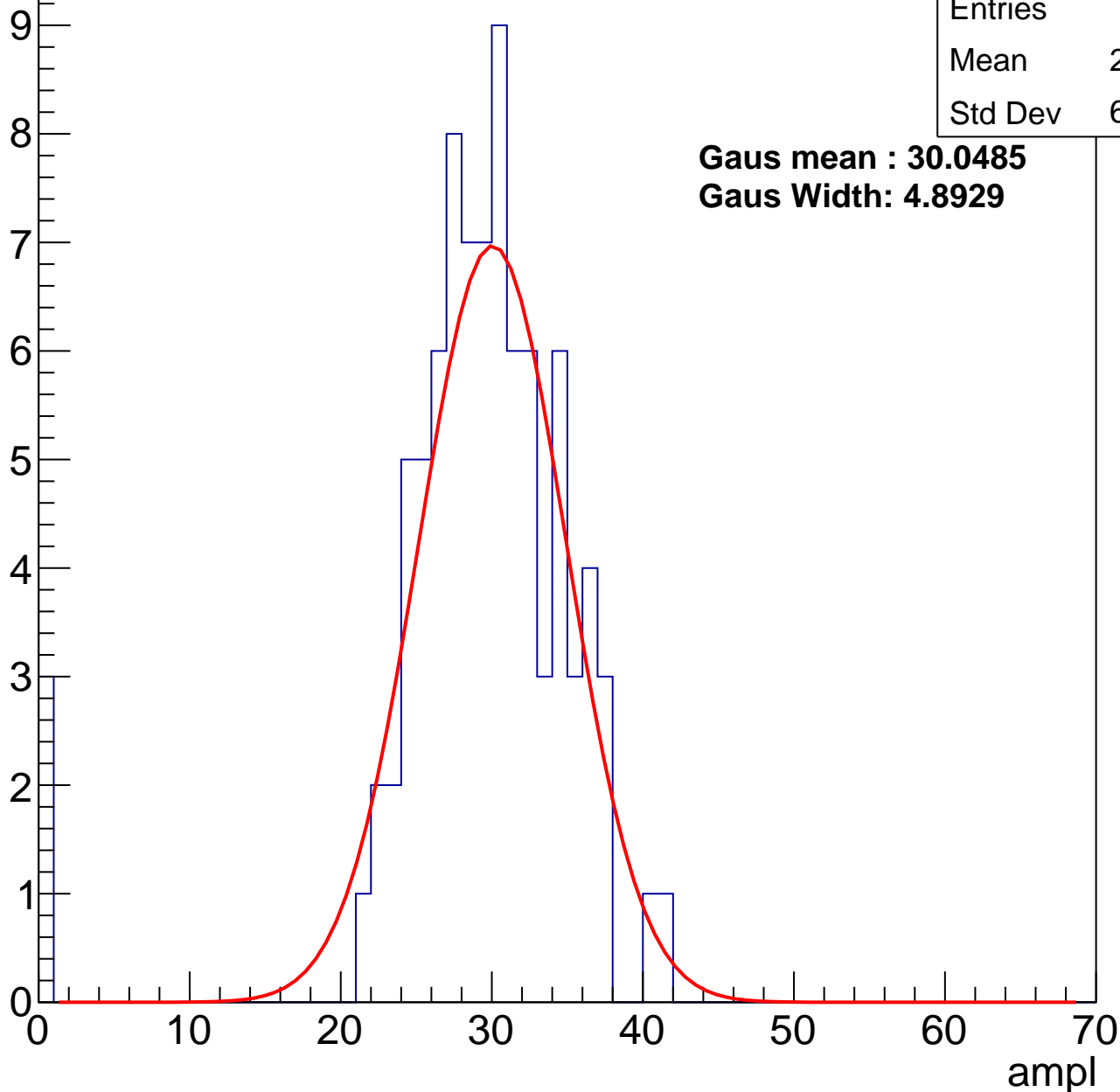
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	88
Mean	28.62
Std Dev	6.816

**Gaus mean : 30.0485**

**Gaus Width: 4.8929**



# B1L101S, U18-ch0, adc1

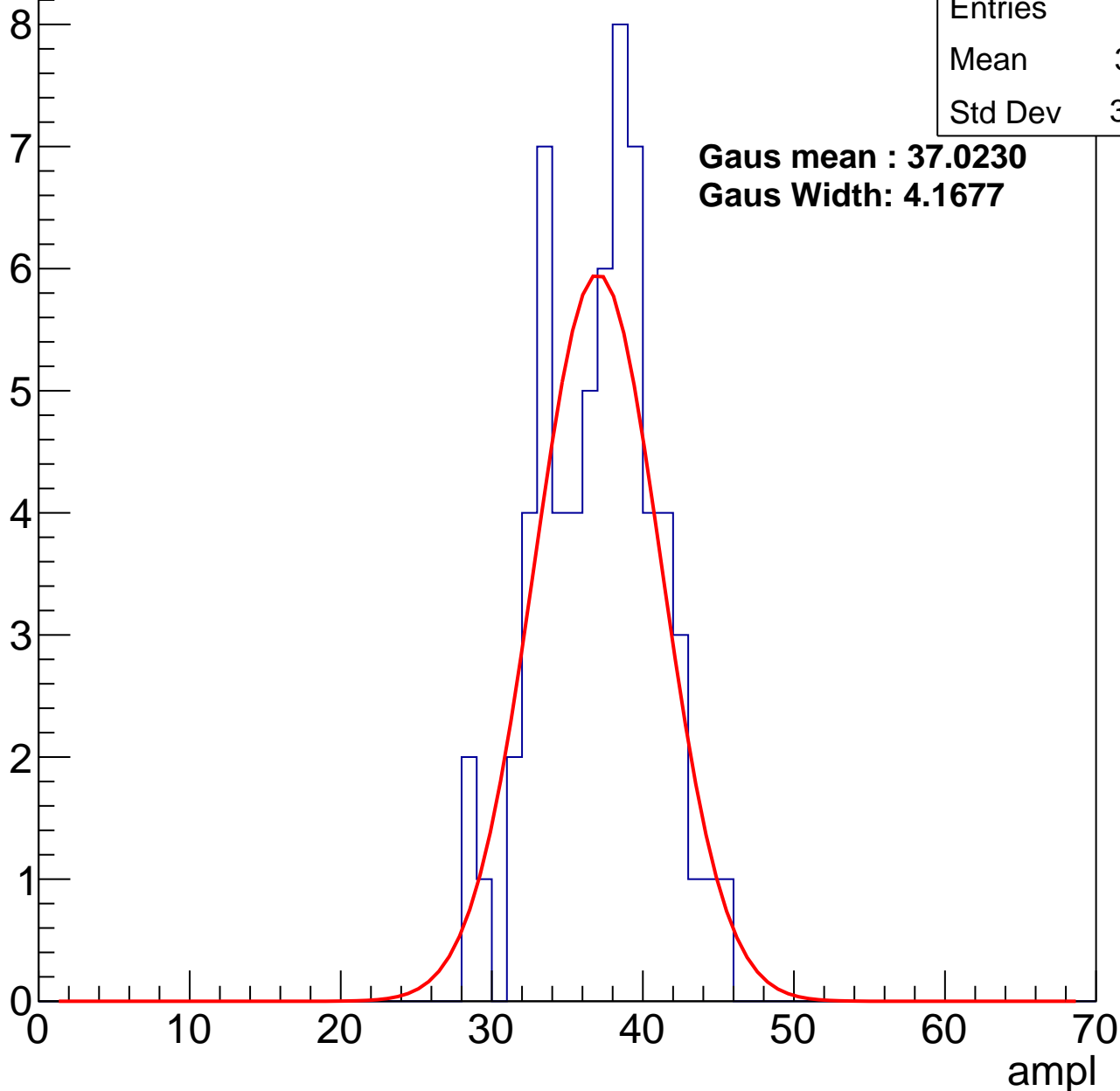
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	36.61
Std Dev	3.786

**Gaus mean : 37.0230**

**Gaus Width: 4.1677**



# B1L101S, U18-ch0, adc2

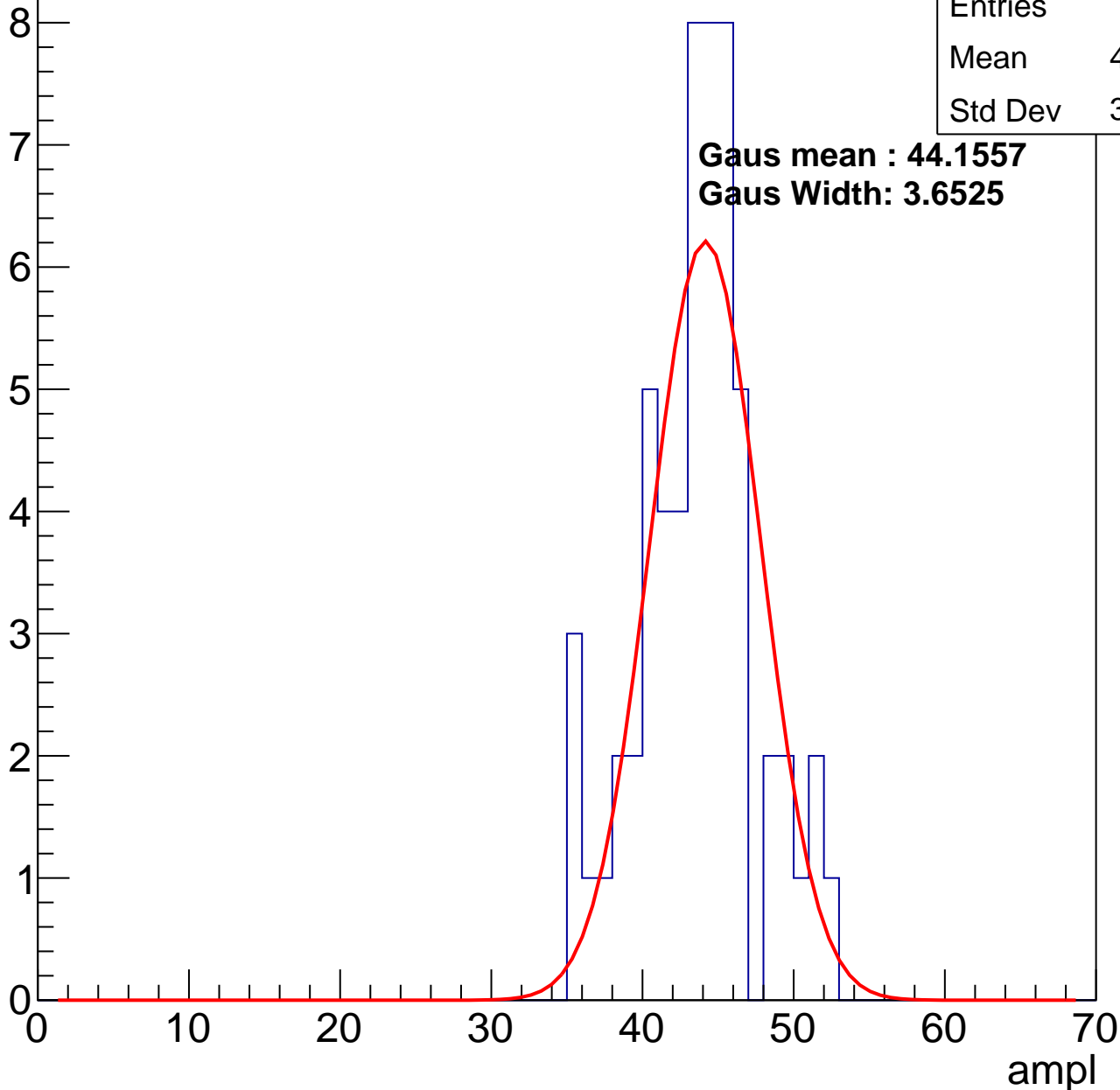
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	43.19
Std Dev	3.877

**Gaus mean : 44.1557**

**Gaus Width: 3.6525**

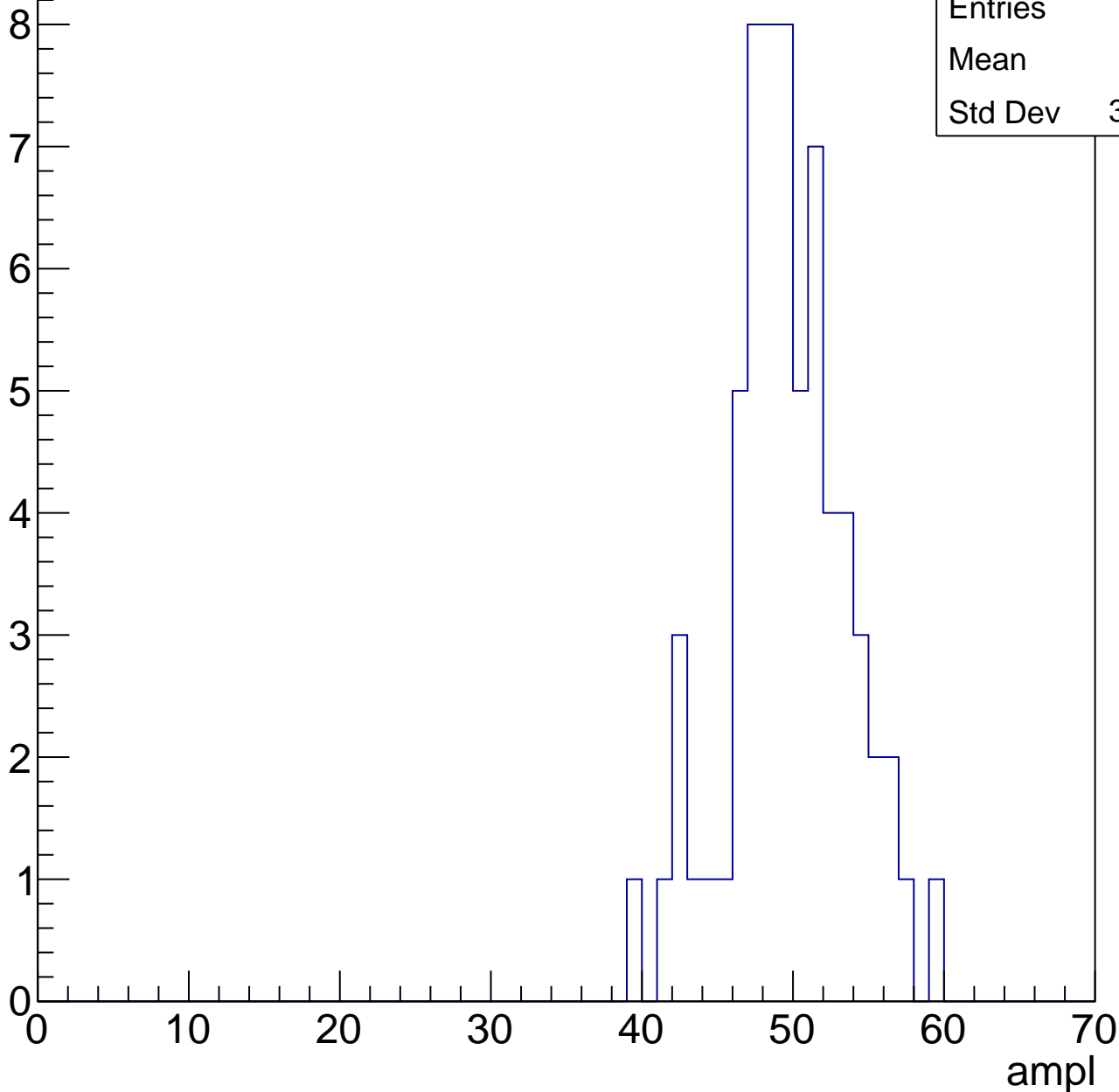


# B1L101S, U18-ch0, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	49.2
Std Dev	3.917

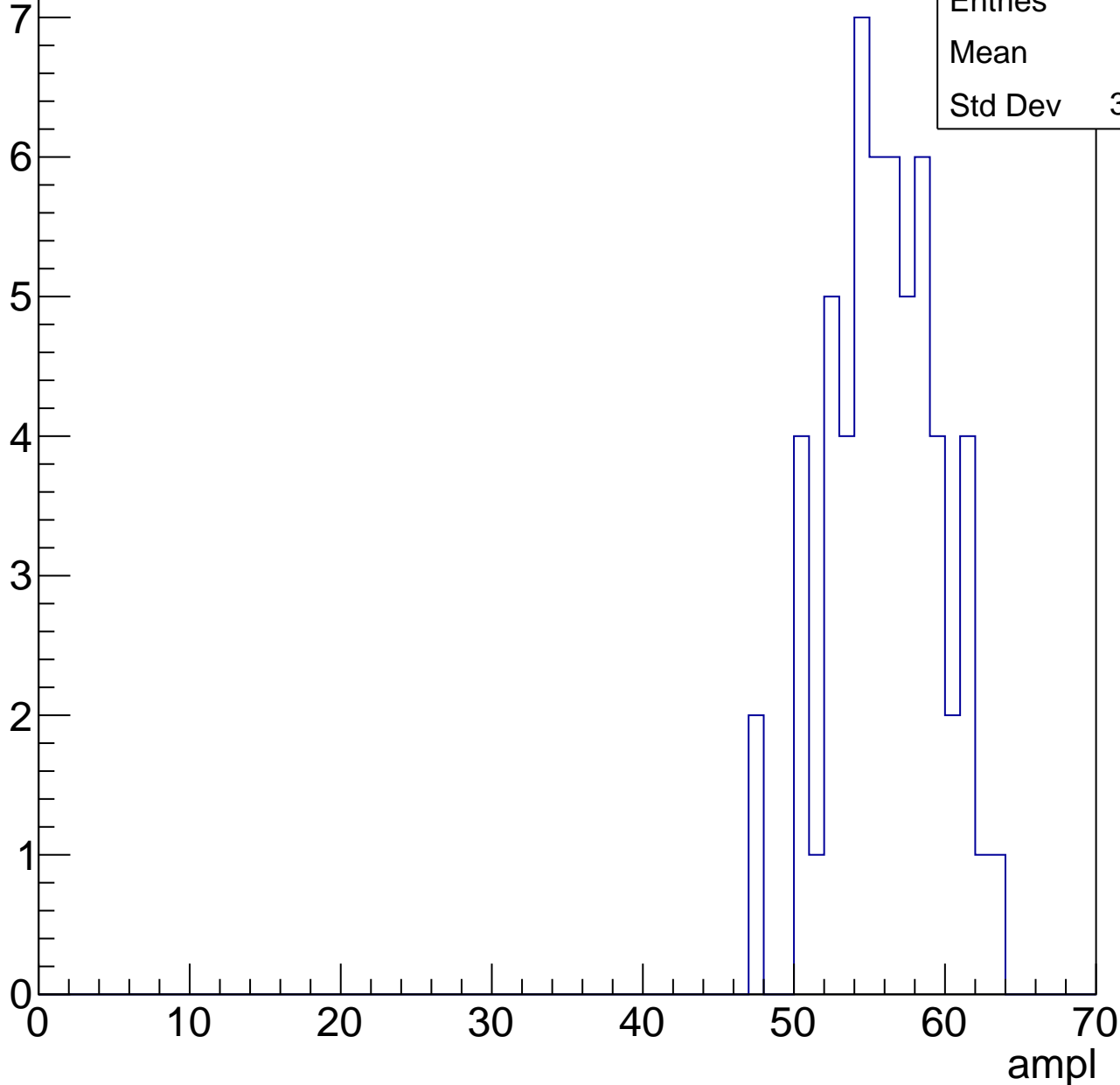


# B1L101S, U18-ch0, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

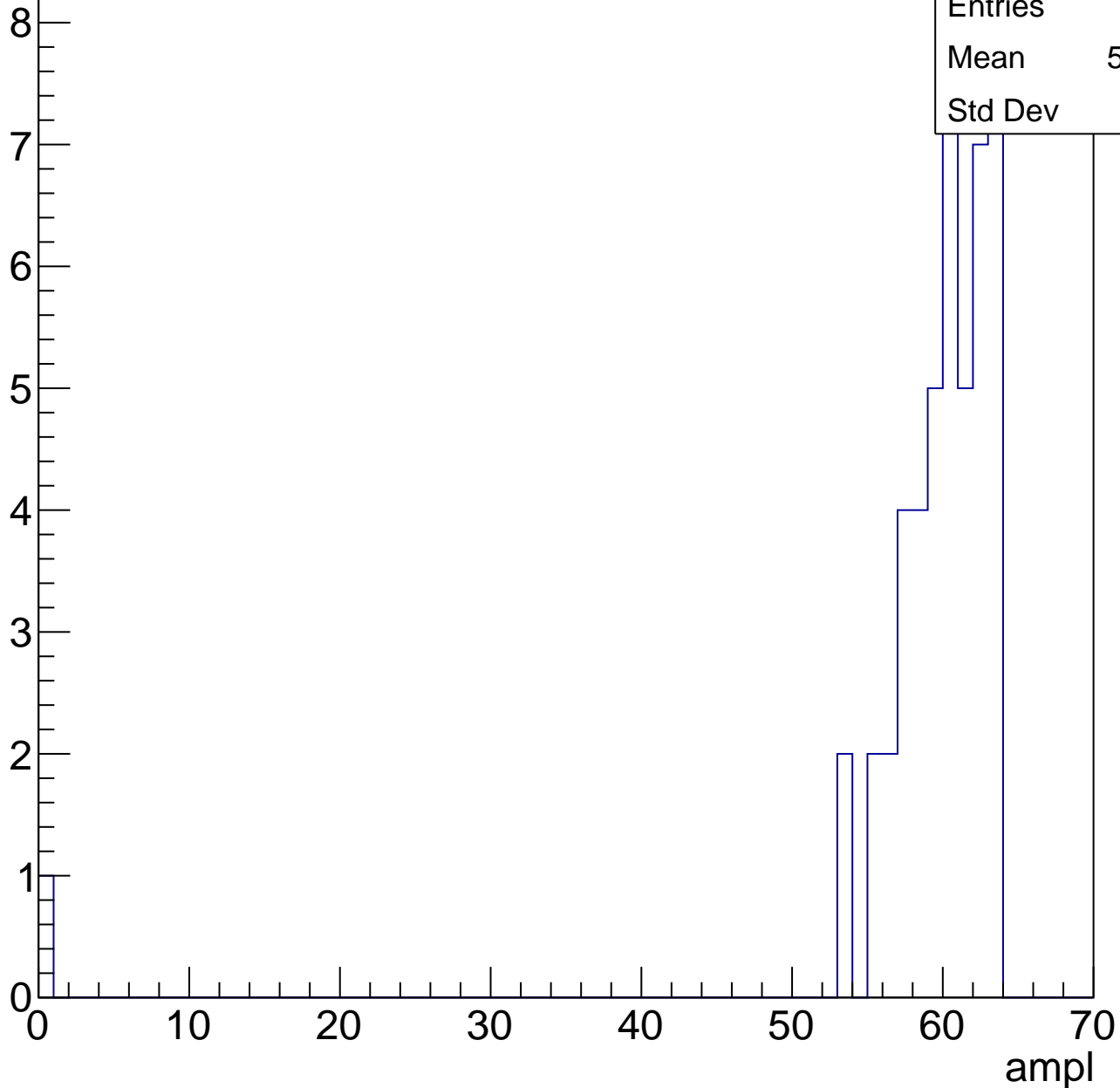
Entries	58
Mean	55.5
Std Dev	3.592



# B1L101S, U18-ch0, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch0, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	62
Std Dev	0.7071

ampl

0 10 20 30 40 50 60 70



# B1L101S, U18-ch0, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U18-ch1, adc0

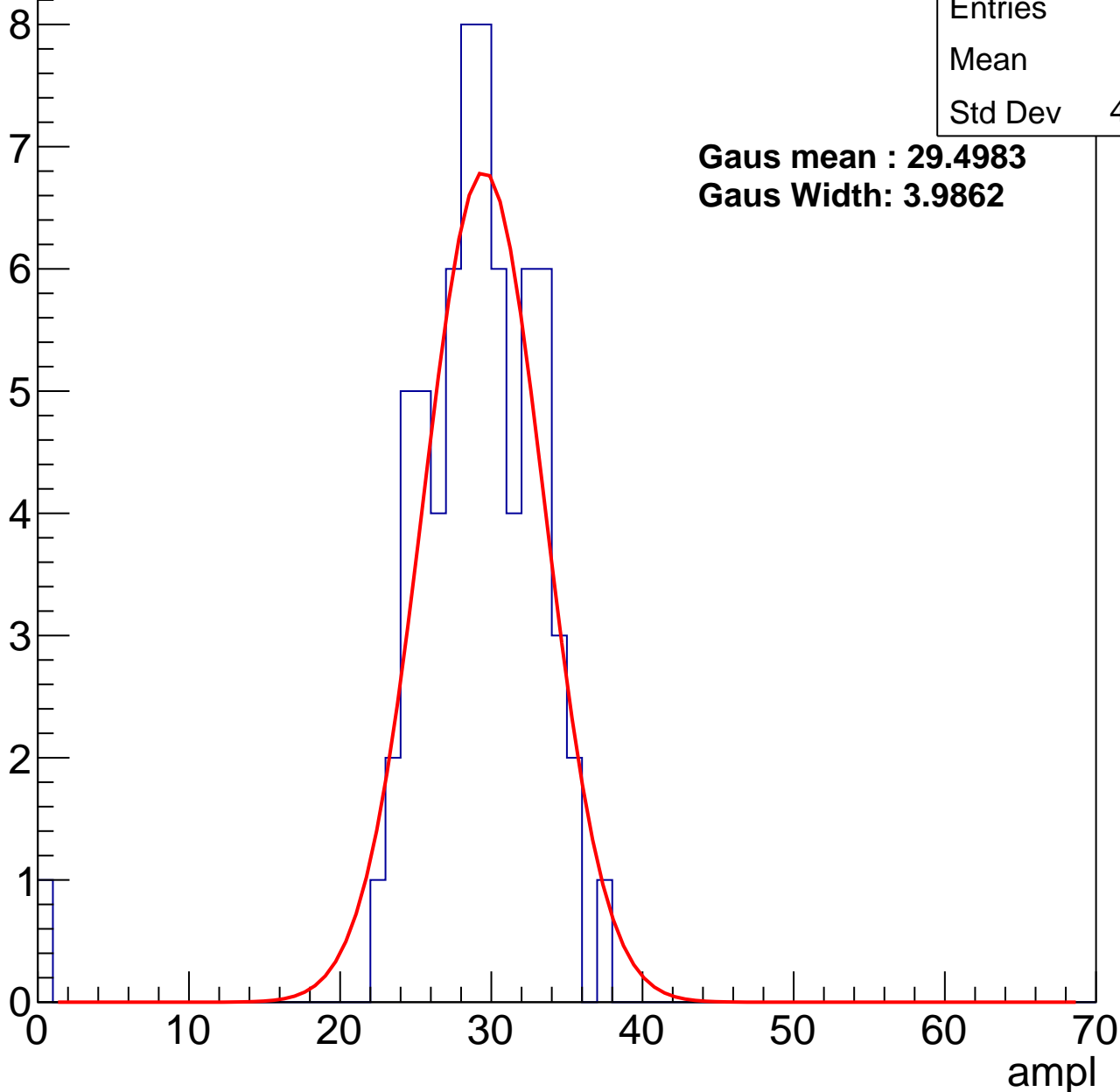
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	28.5
Std Dev	4.852

**Gaus mean : 29.4983**

**Gaus Width: 3.9862**



# B1L101S, U18-ch1, adc1

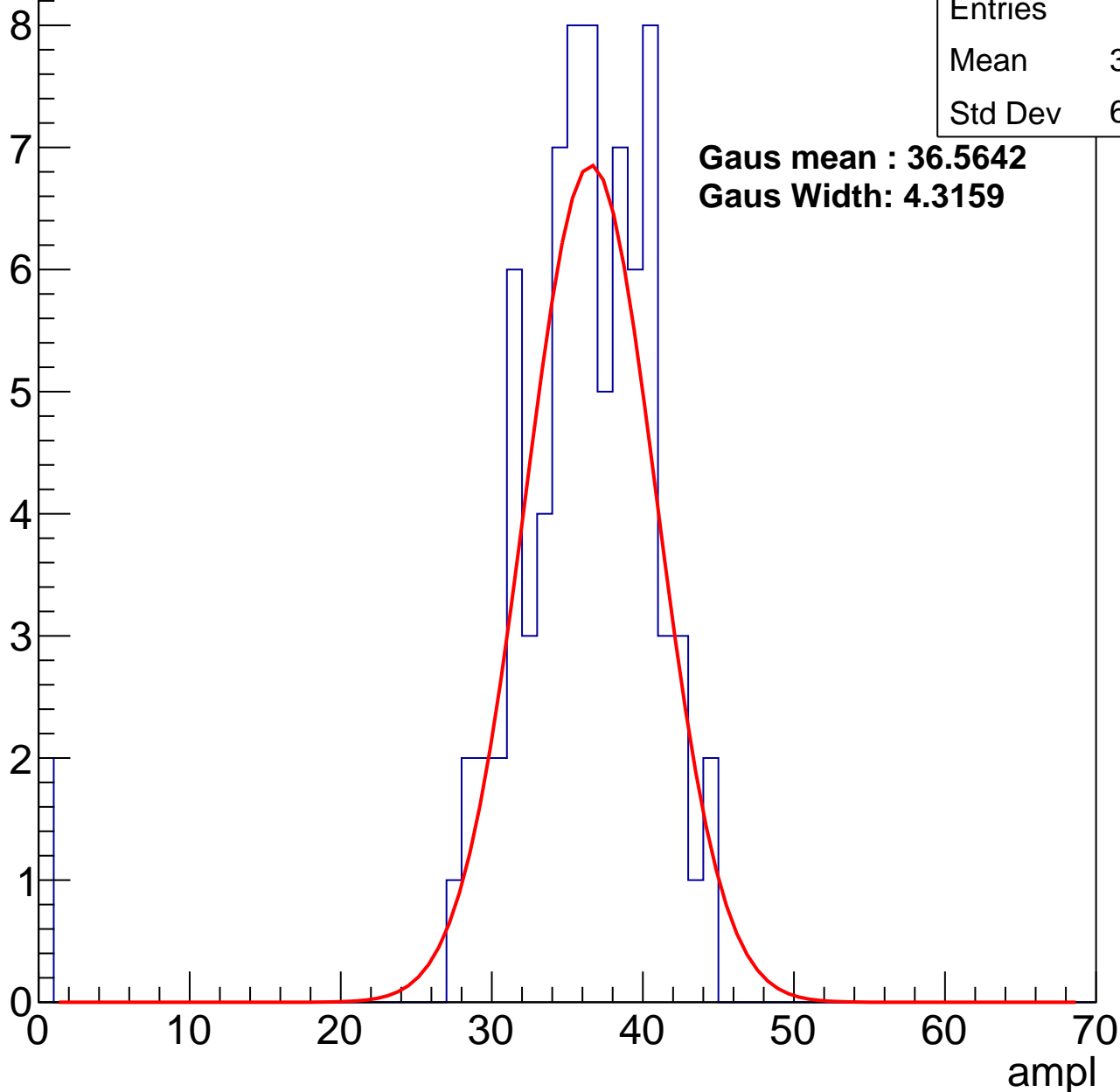
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	80
Mean	35.08
Std Dev	6.844

**Gaus mean : 36.5642**

**Gaus Width: 4.3159**



# B1L101S, U18-ch1, adc2

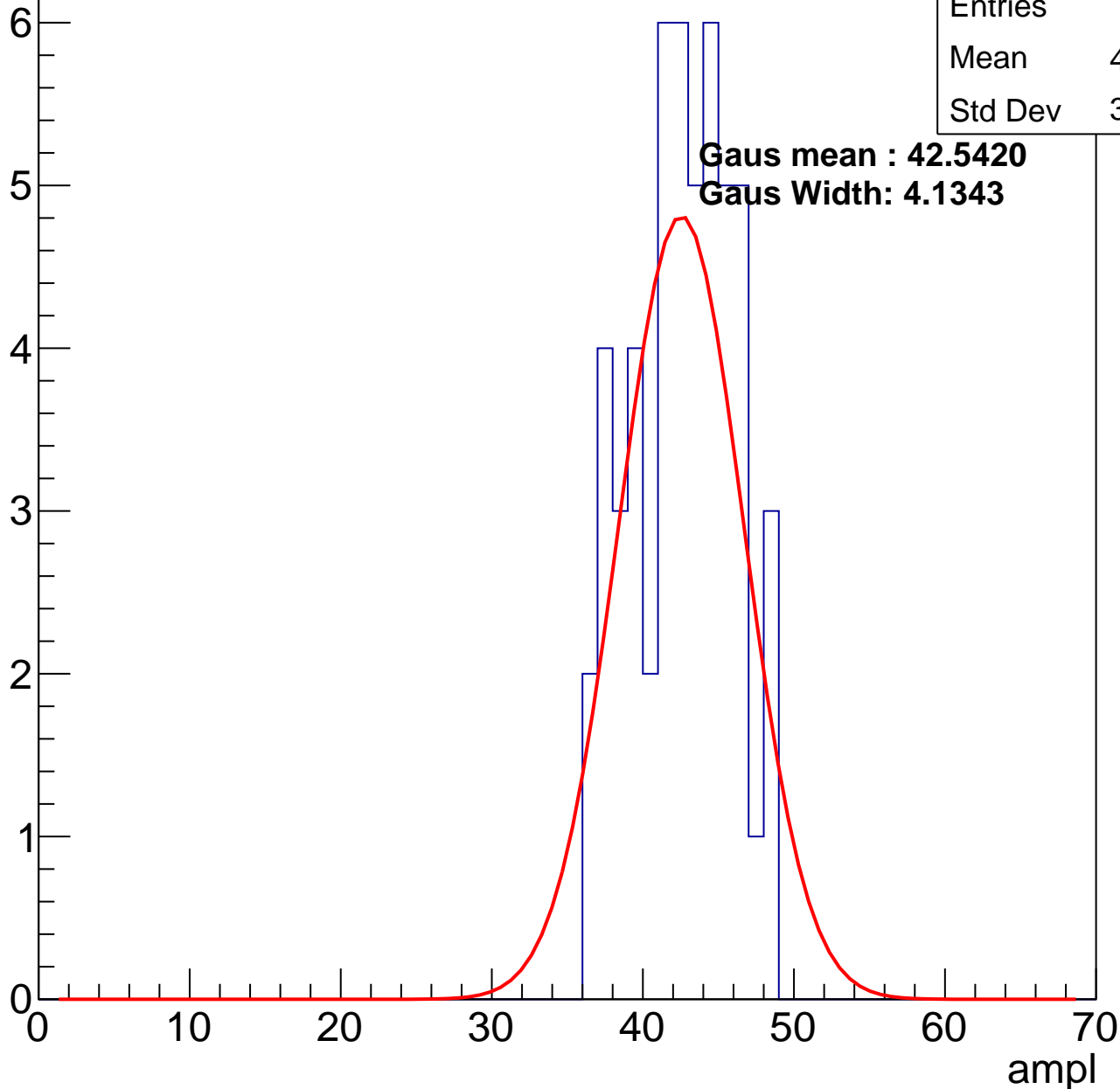
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	42.17
Std Dev	3.268

**Gaus mean : 42.5420**

**Gaus Width: 4.1343**

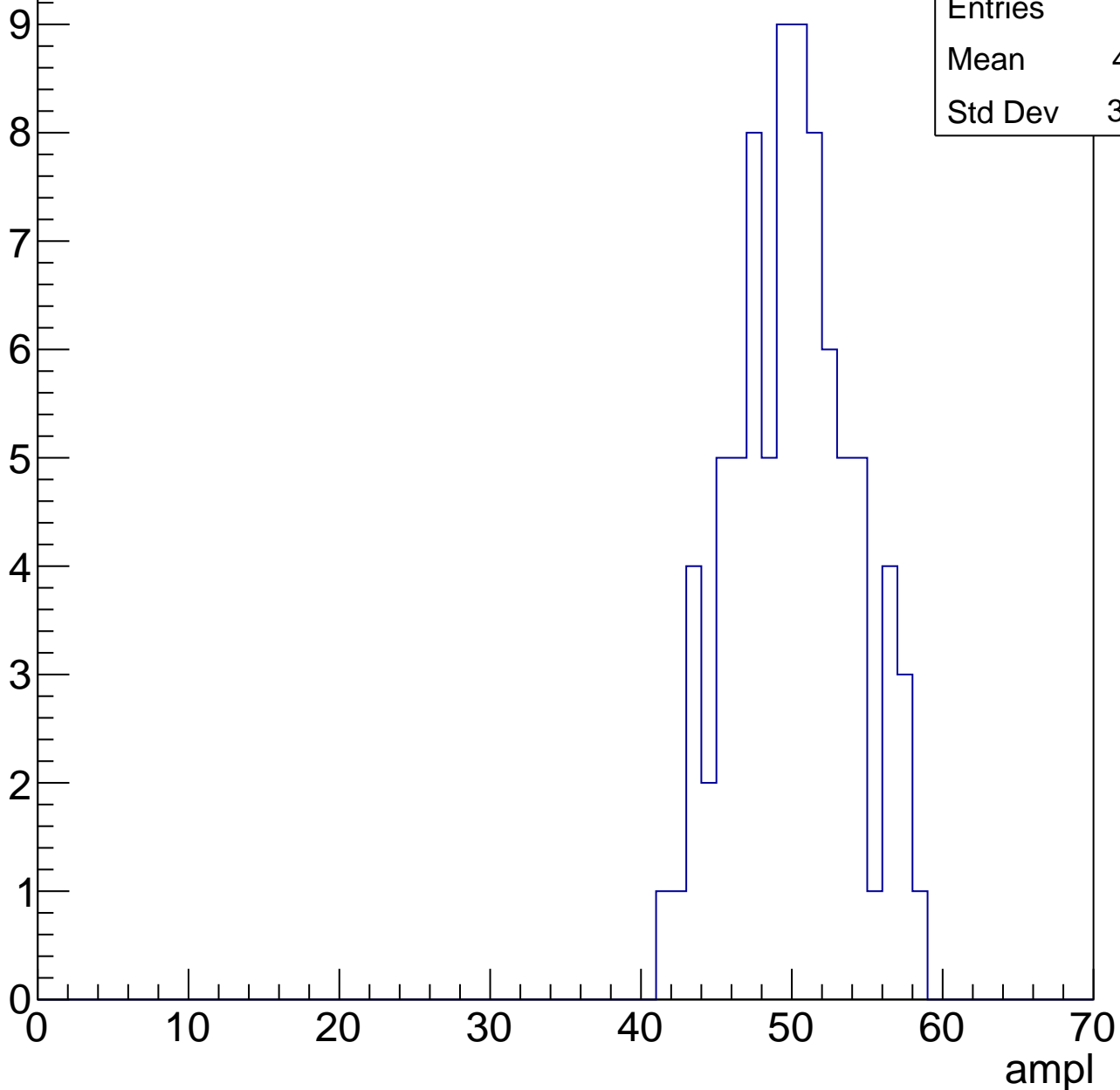


# B1L101S, U18-ch1, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	82
Mean	49.61
Std Dev	3.894

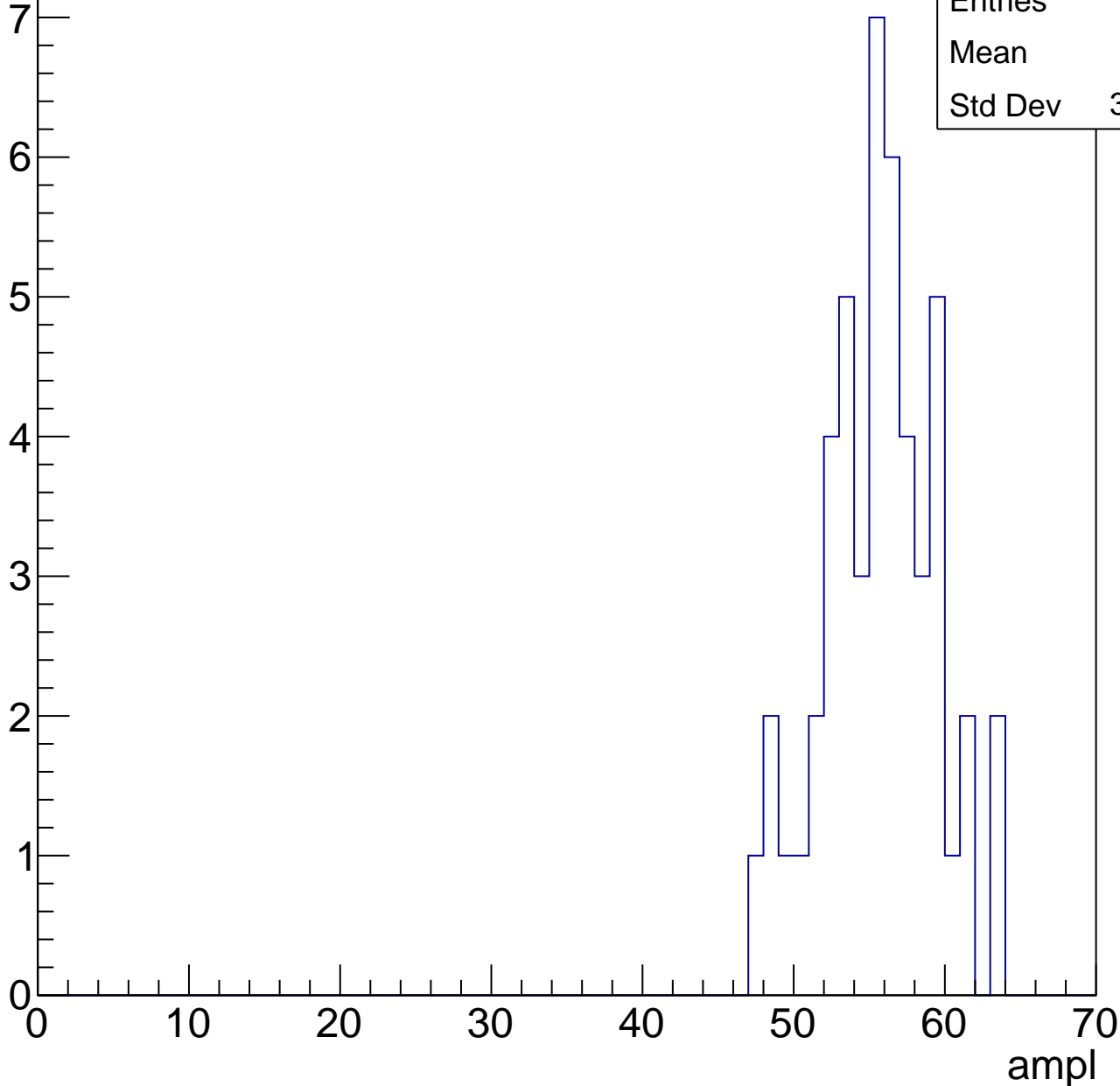


# B1L101S, U18-ch1, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	49
Mean	55.2
Std Dev	3.687

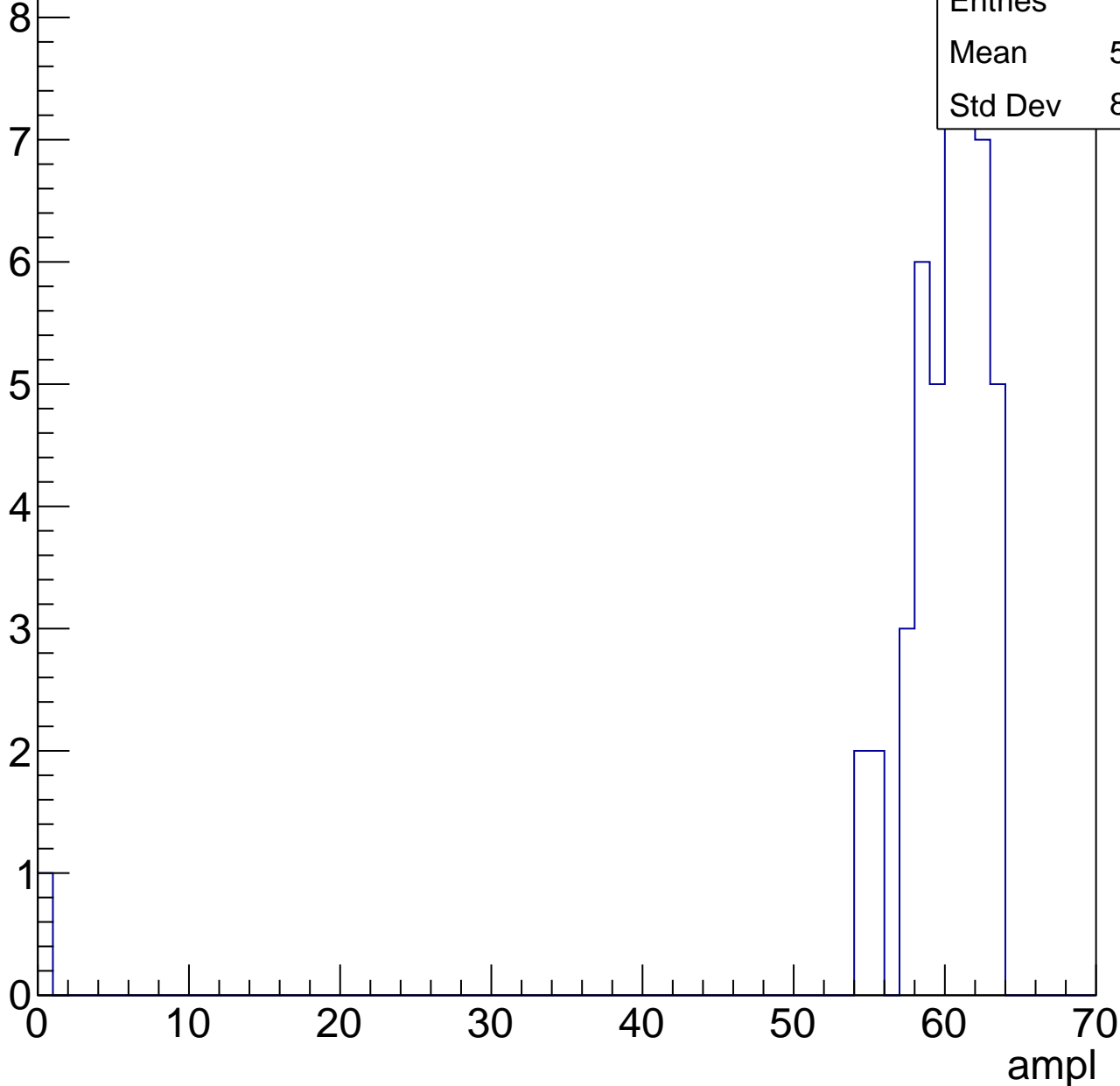


# B1L101S, U18-ch1, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	47
Mean	58.49
Std Dev	8.934



# B1L101S, U18-ch1, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch1, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch2, adc0

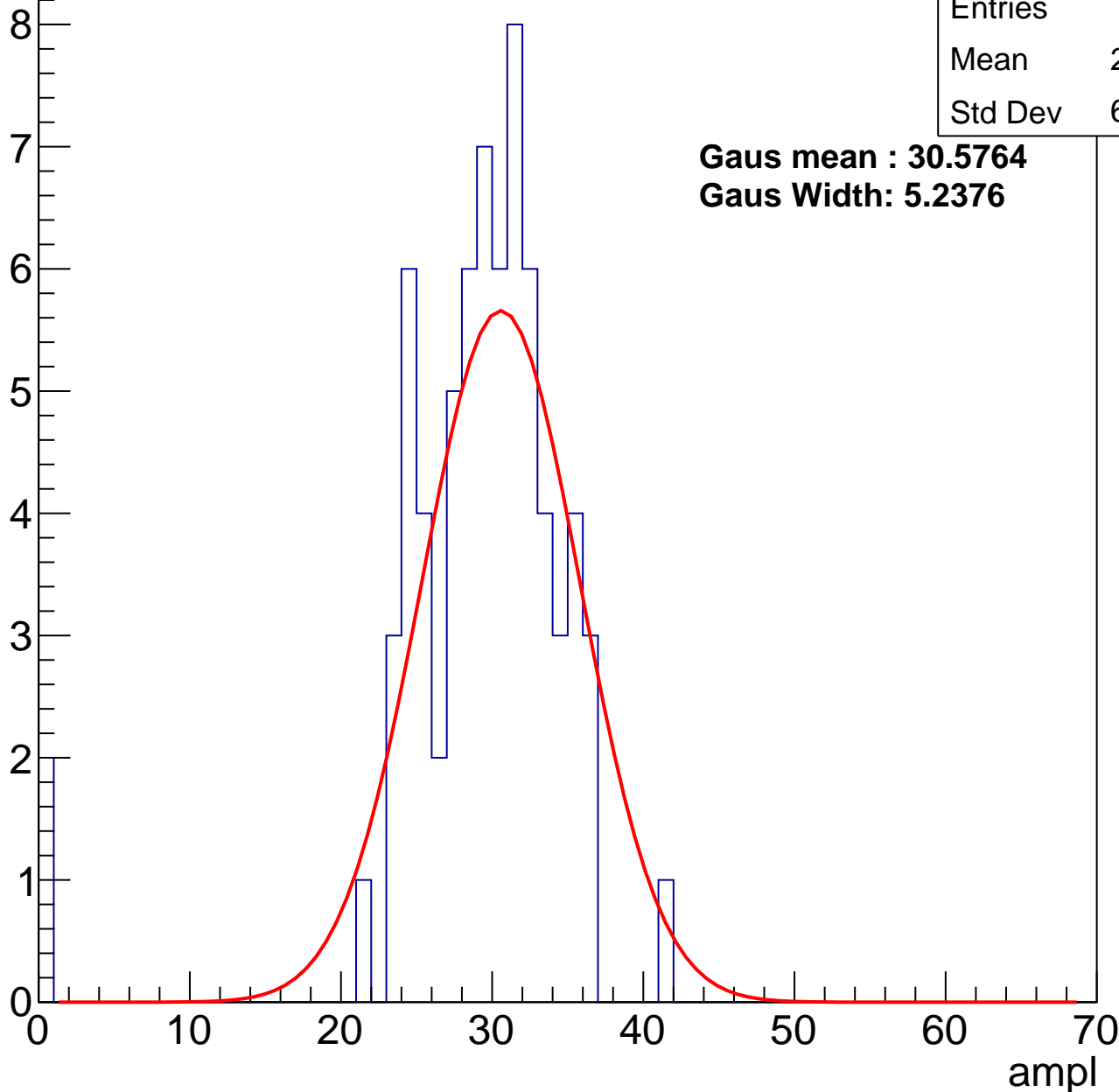
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	28.66
Std Dev	6.246

**Gaus mean : 30.5764**

**Gaus Width: 5.2376**



# B1L101S, U18-ch2, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	63
Mean	36.03
Std Dev	3.29

**Gaus mean : 36.3265**

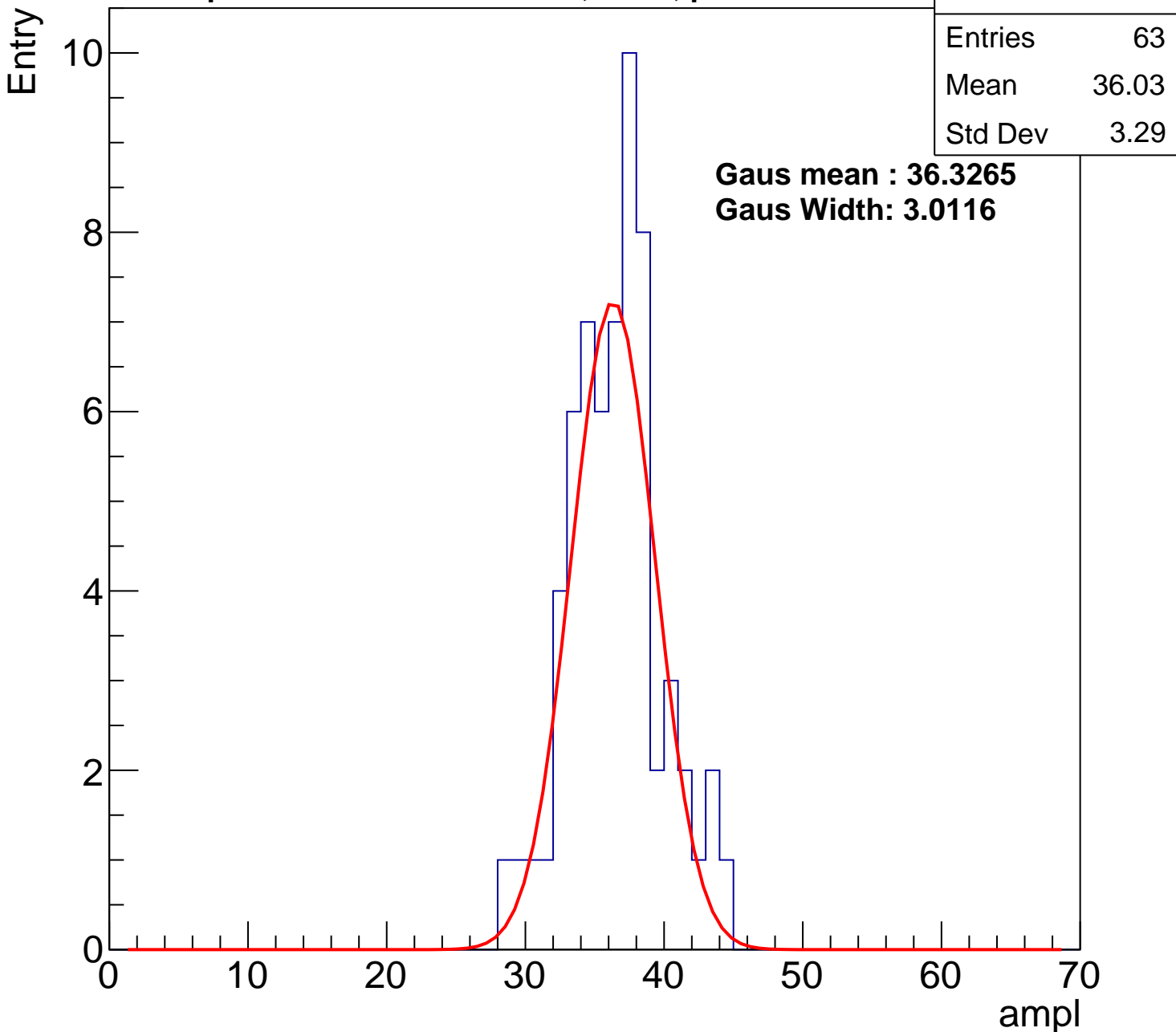
**Gaus Width: 3.0116**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L101S, U18-ch2, adc2

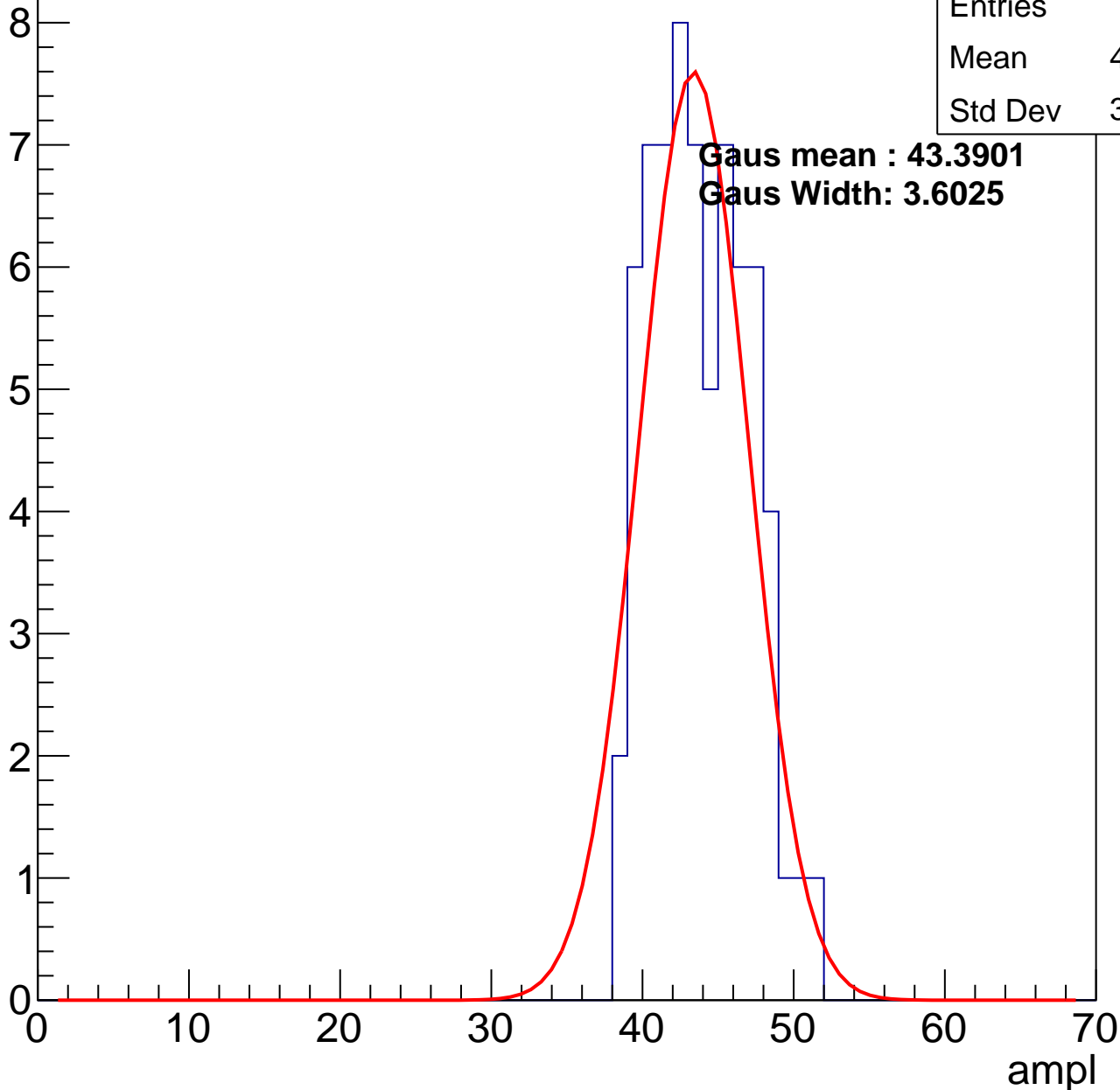
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	43.37
Std Dev	3.134

**Gaus mean : 43.3901**

**Gaus Width: 3.6025**

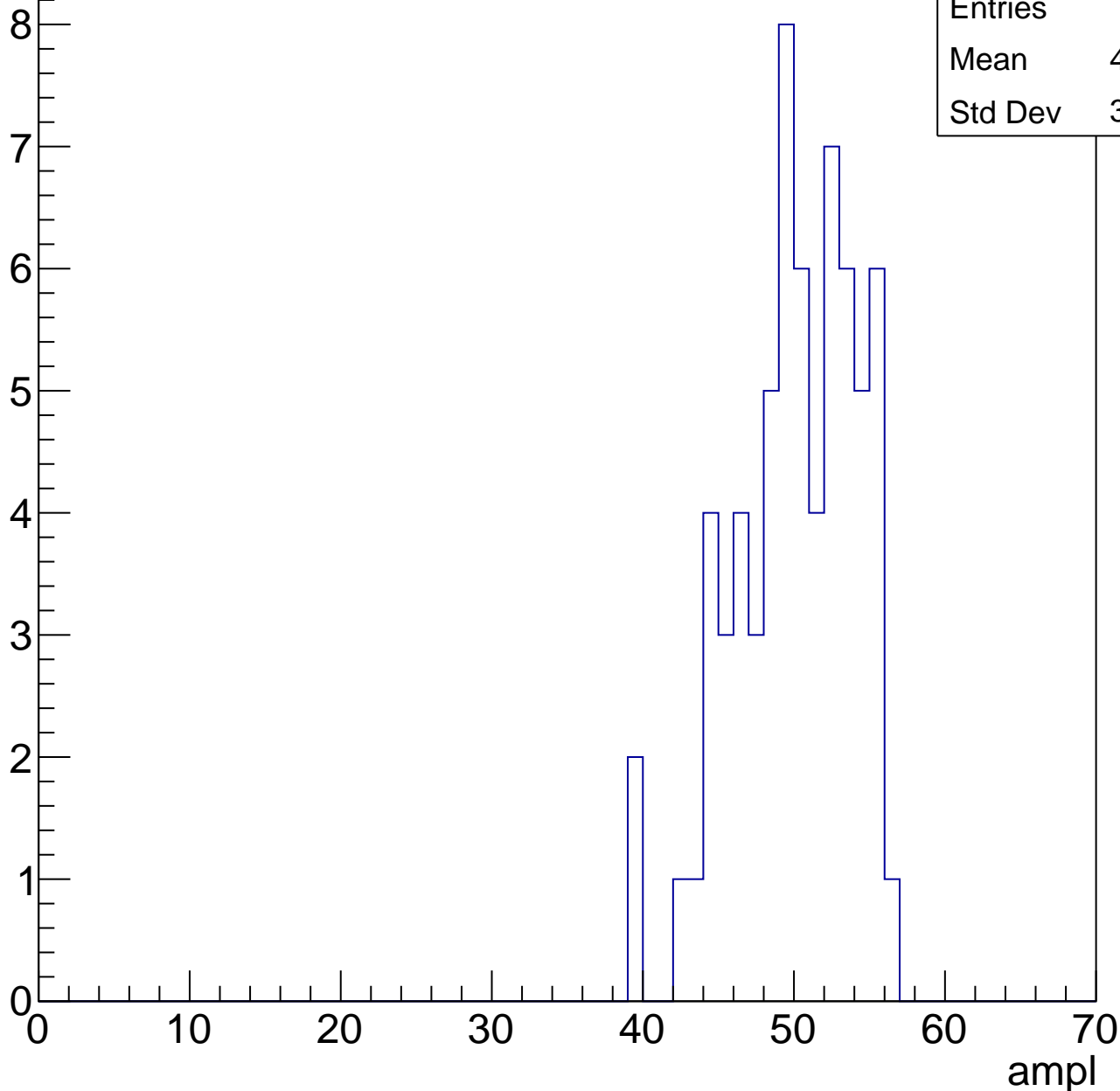


# B1L101S, U18-ch2, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	49.59
Std Dev	3.958

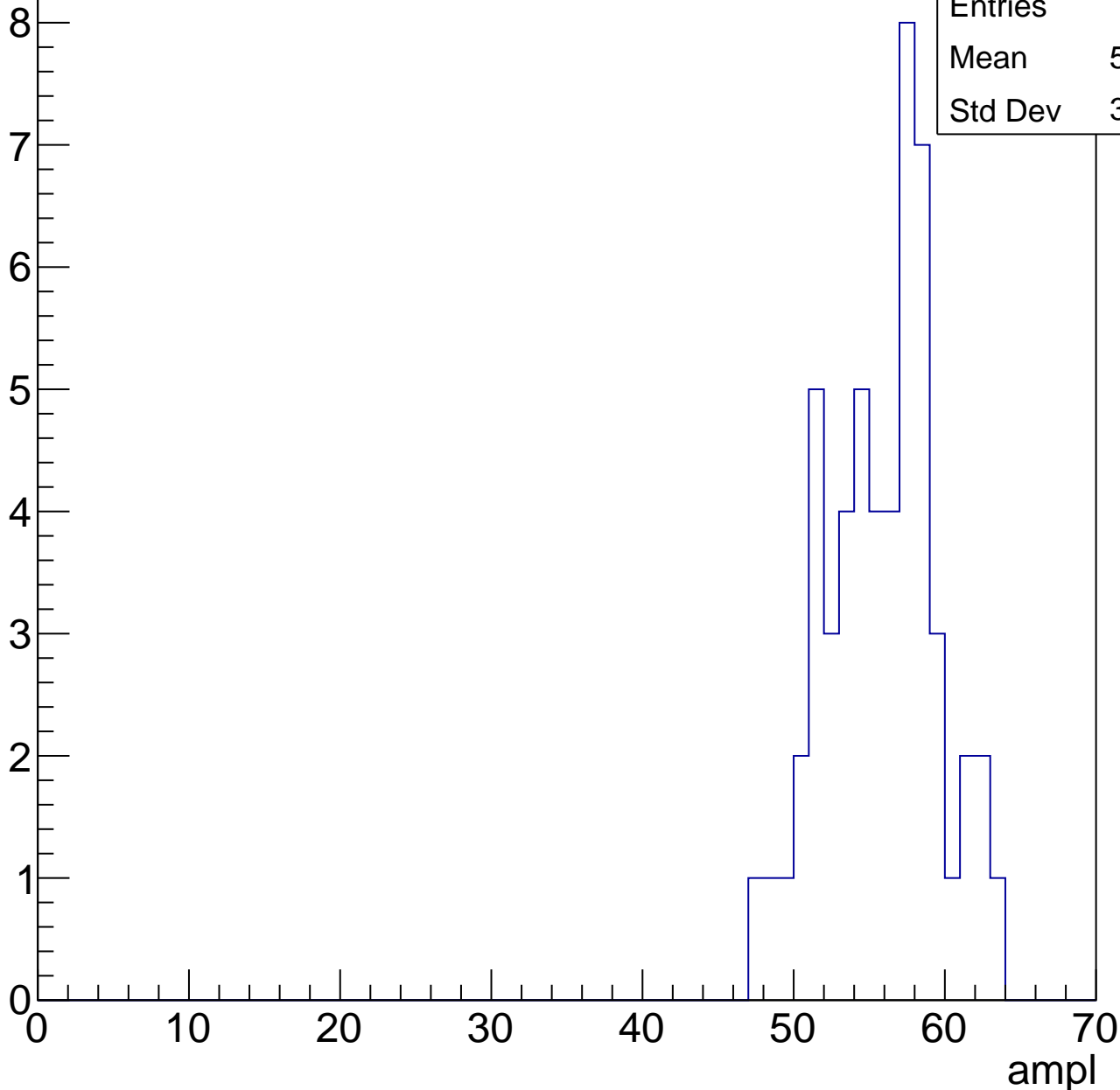


# B1L101S, U18-ch2, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

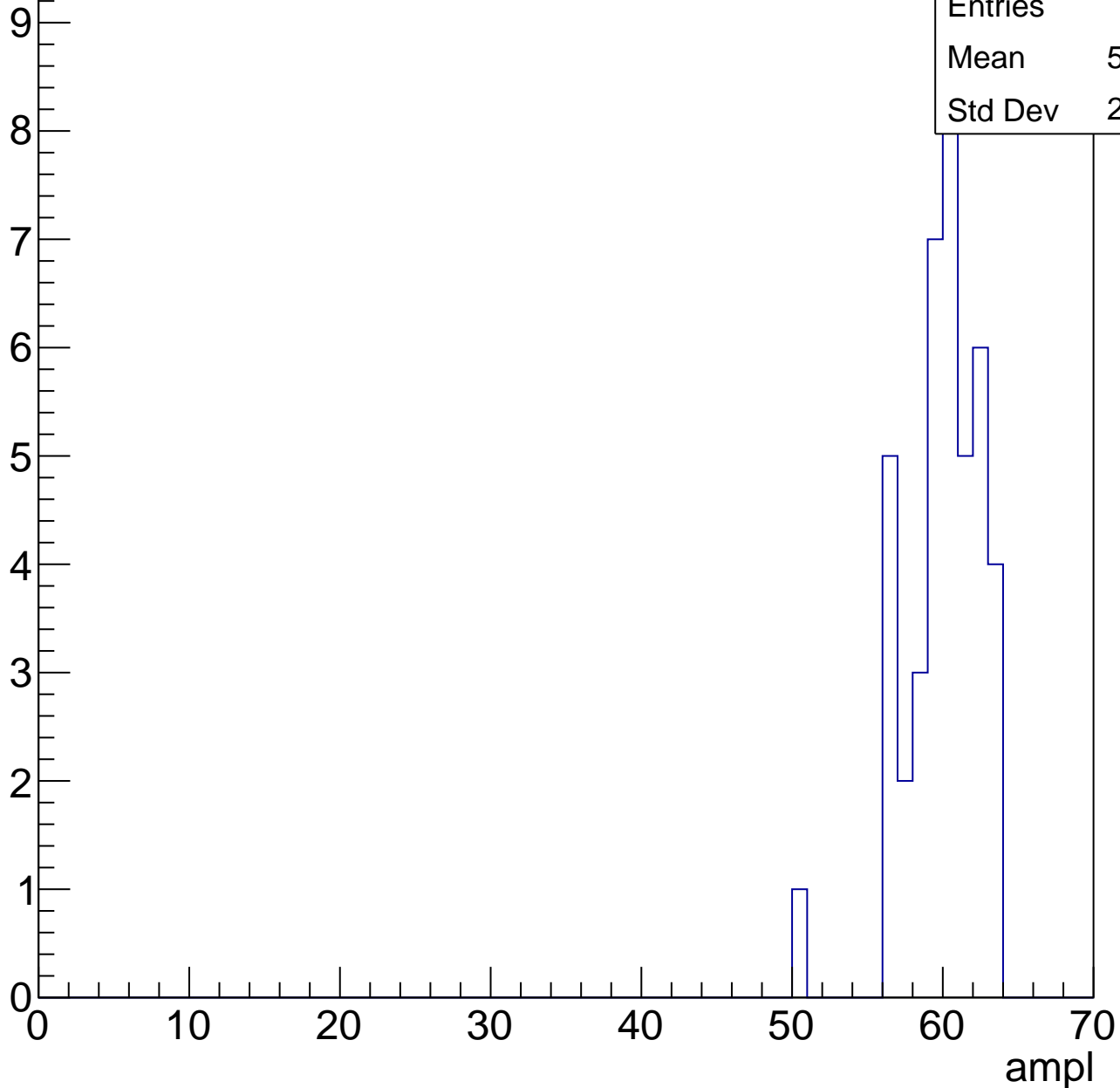
Entries	54
Mean	55.35
Std Dev	3.667



# B1L101S, U18-ch2, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

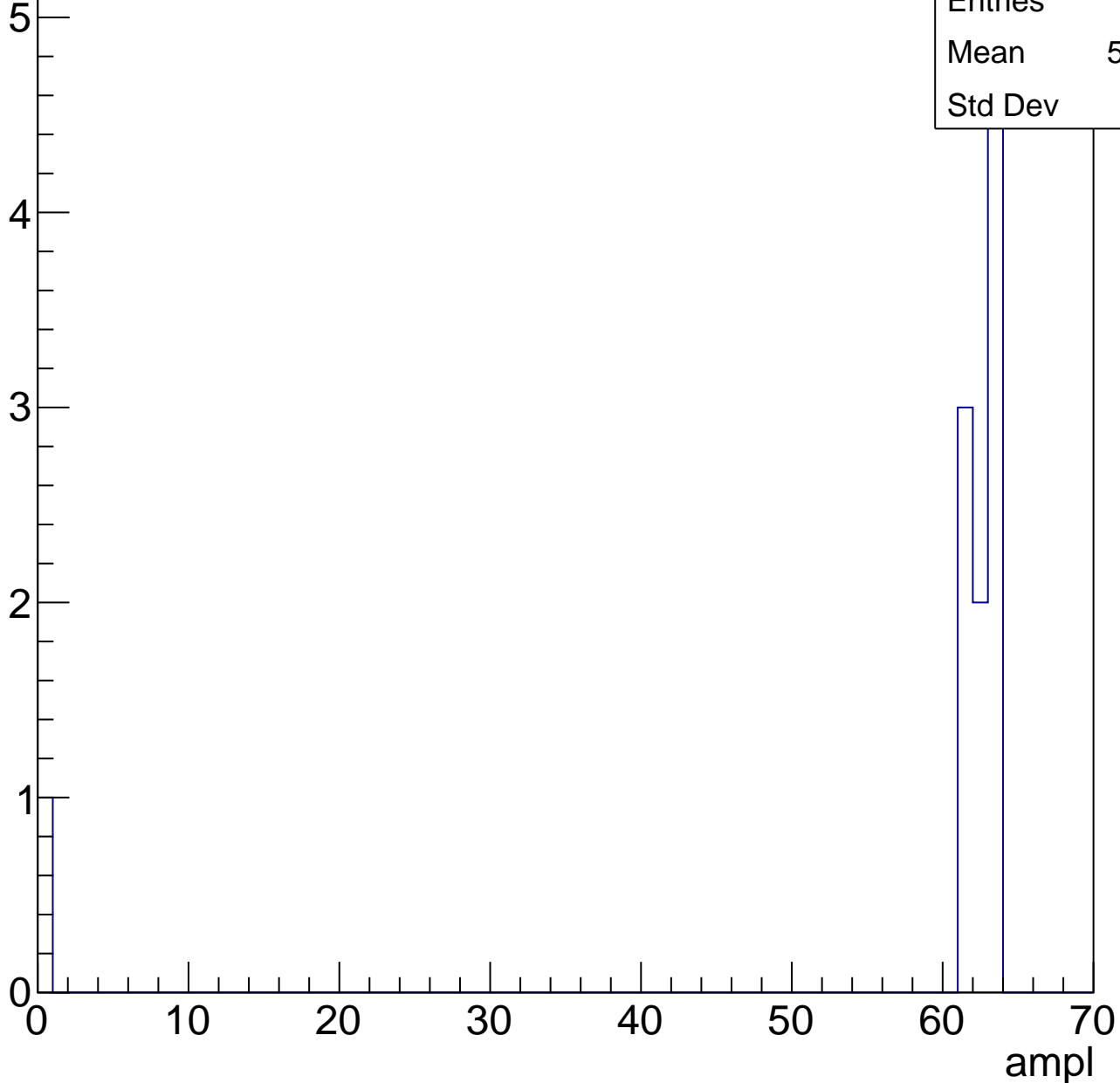


# B1L101S, U18-ch2, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	11
Mean	56.55
Std Dev	17.9





# B1L101S, U18-ch2, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U18-ch3, adc0

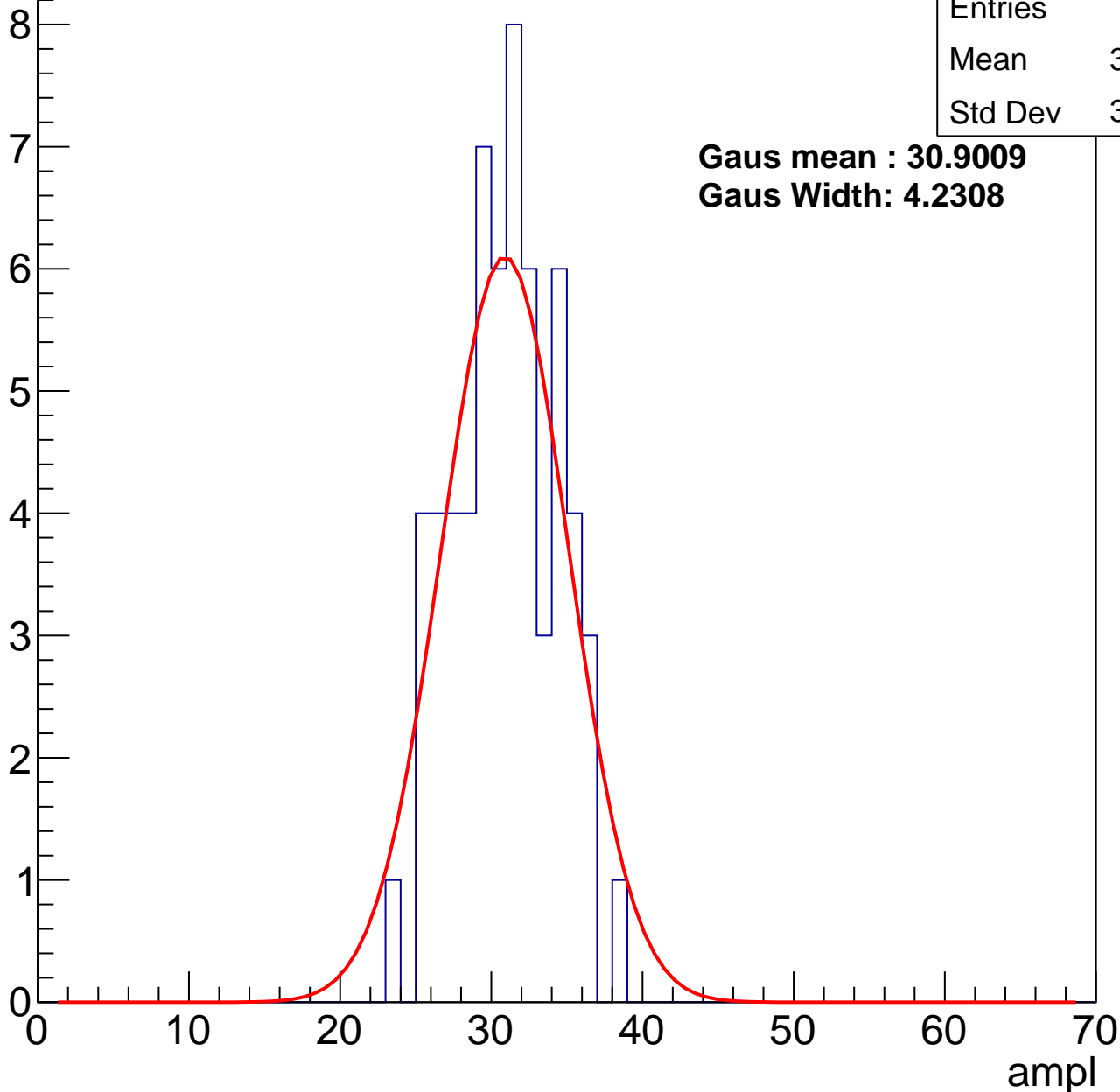
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	30.48
Std Dev	3.352

**Gaus mean : 30.9009**

**Gaus Width: 4.2308**



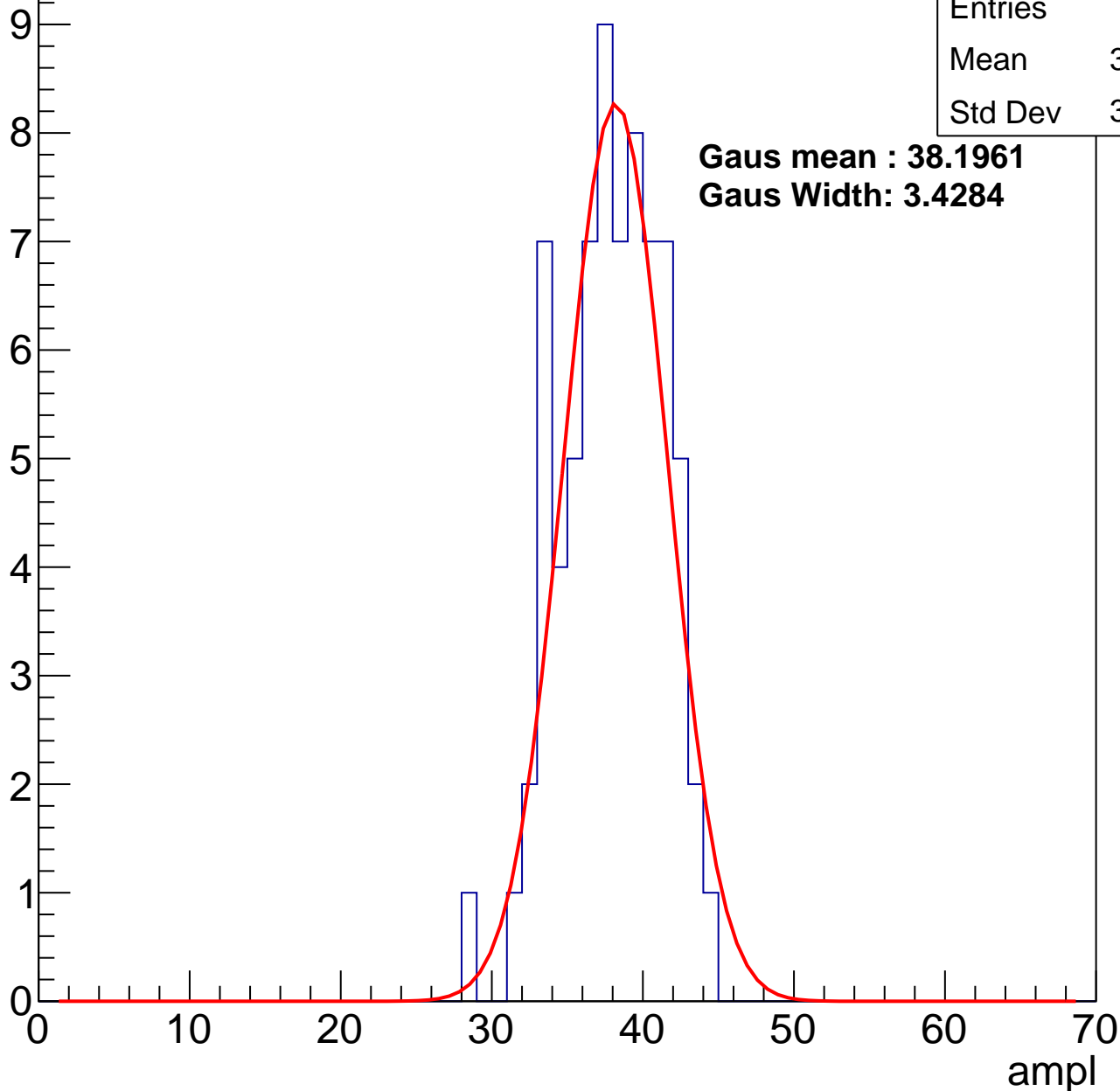
# B1L101S, U18-ch3, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	37.47
Std Dev	3.282

**Gaus mean : 38.1961**  
**Gaus Width: 3.4284**



# B1L101S, U18-ch3, adc2

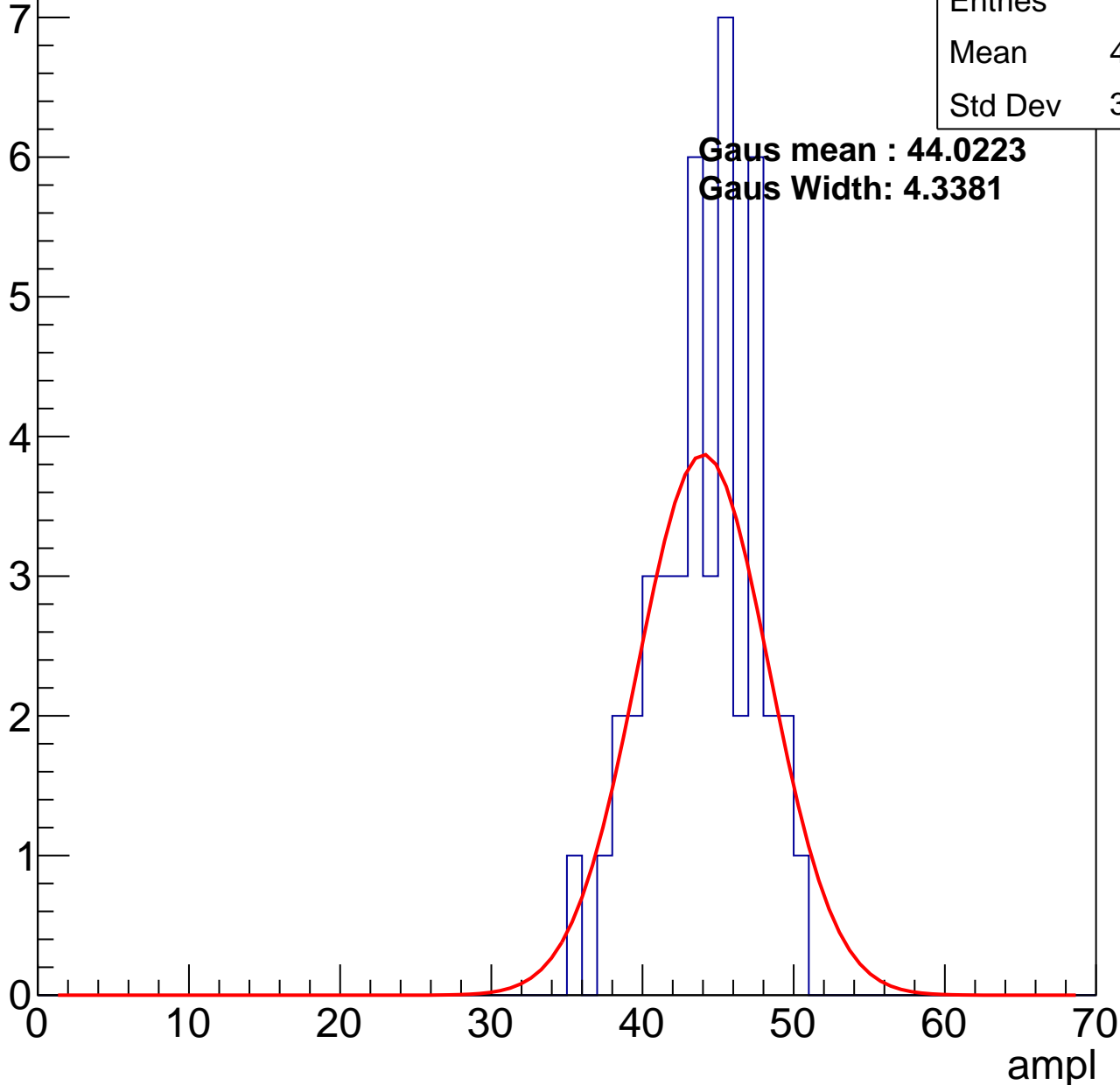
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	44
Mean	43.59
Std Dev	3.453

**Gaus mean : 44.0223**

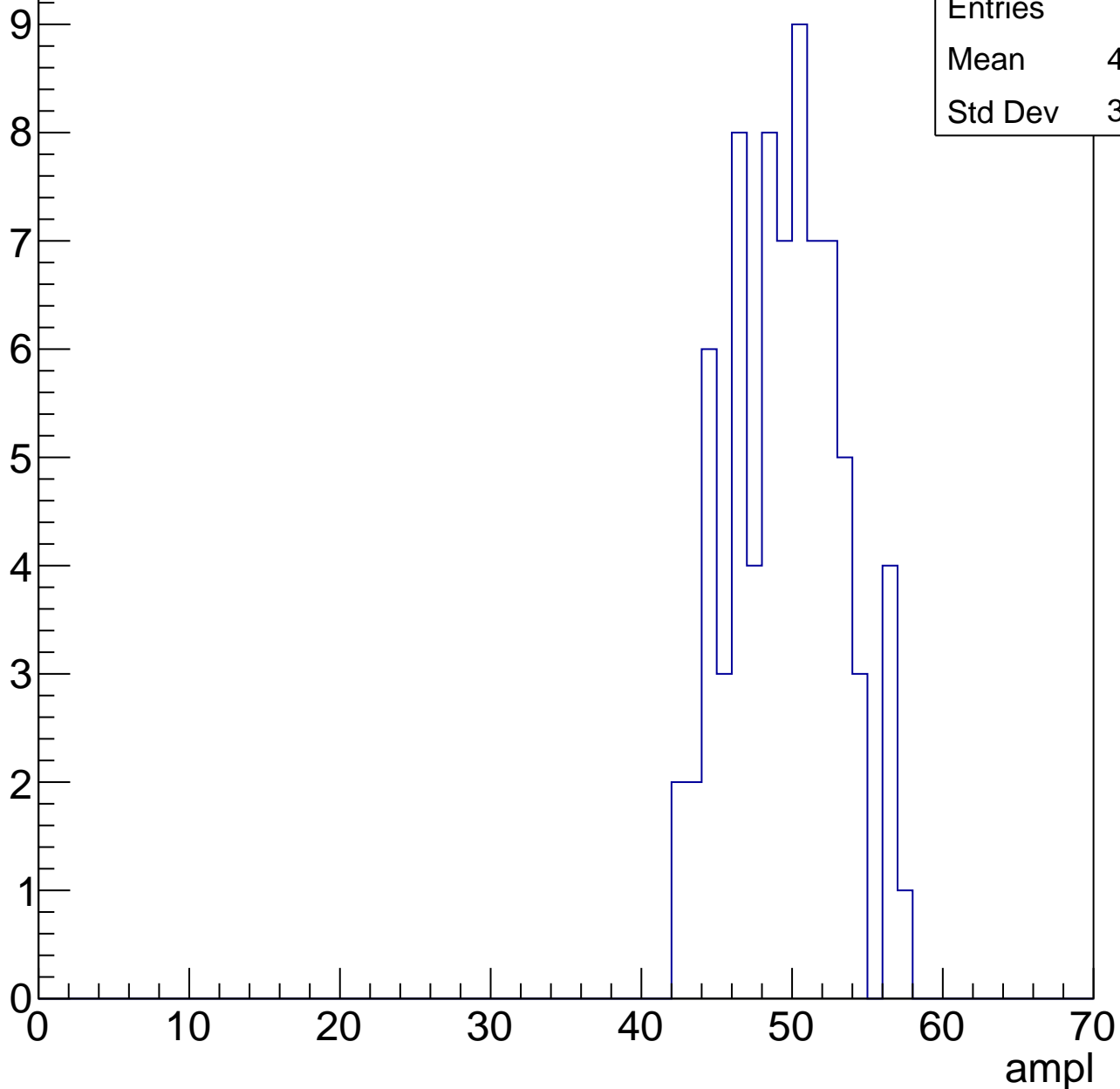
**Gaus Width: 4.3381**



# B1L101S, U18-ch3, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch3, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

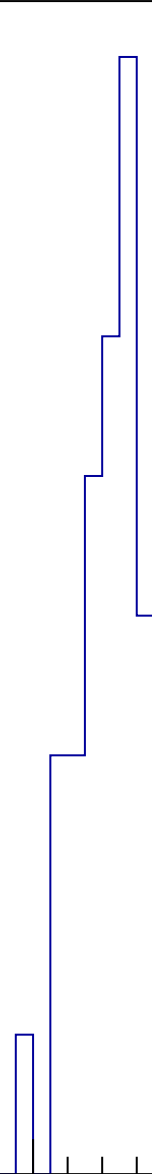
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	56
Mean	55.96
Std Dev	2.884

ampl

0 10 20 30 40 50 60 70

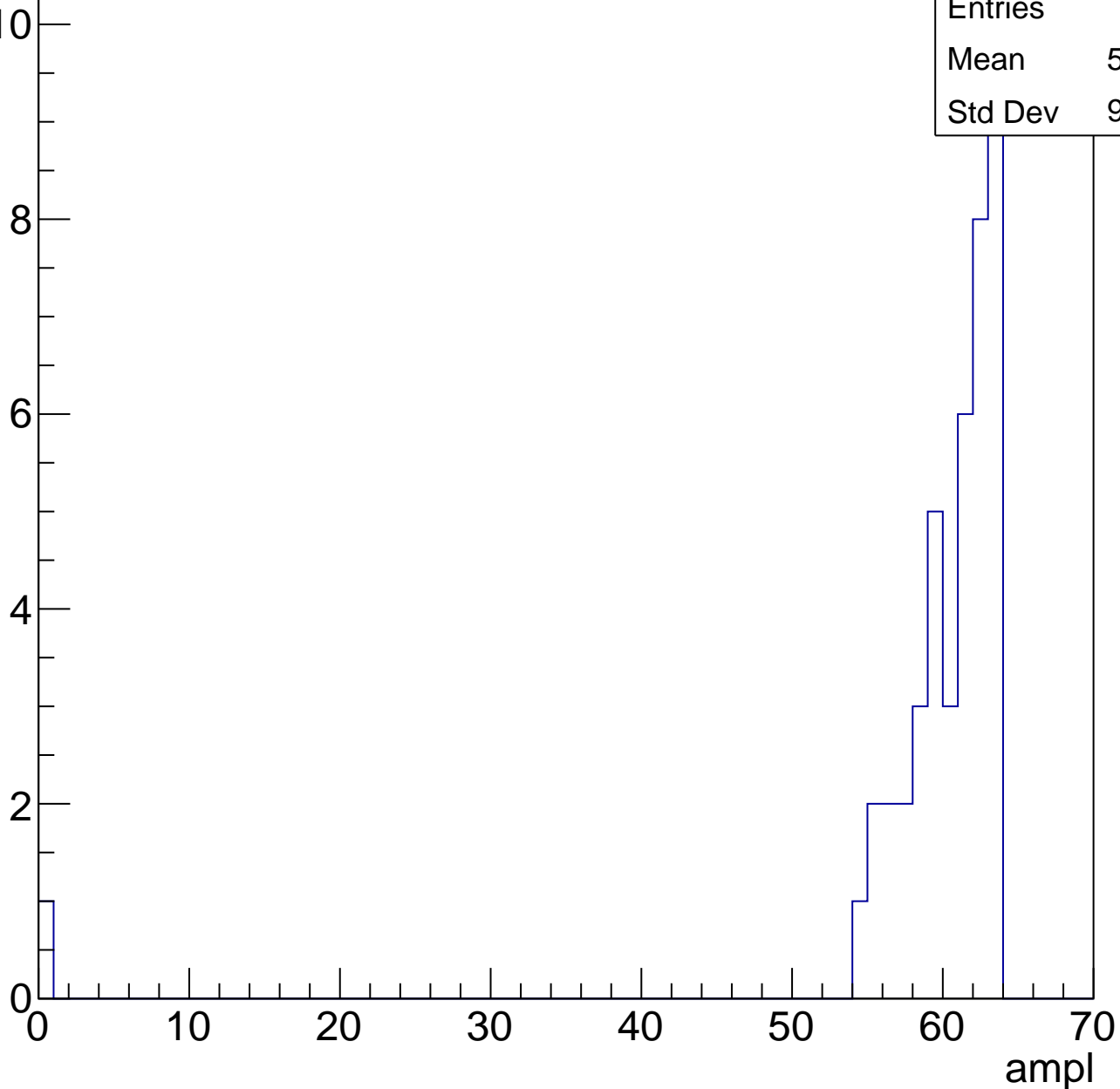


# B1L101S, U18-ch3, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	43
Mean	58.86
Std Dev	9.432



# B1L101S, U18-ch3, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

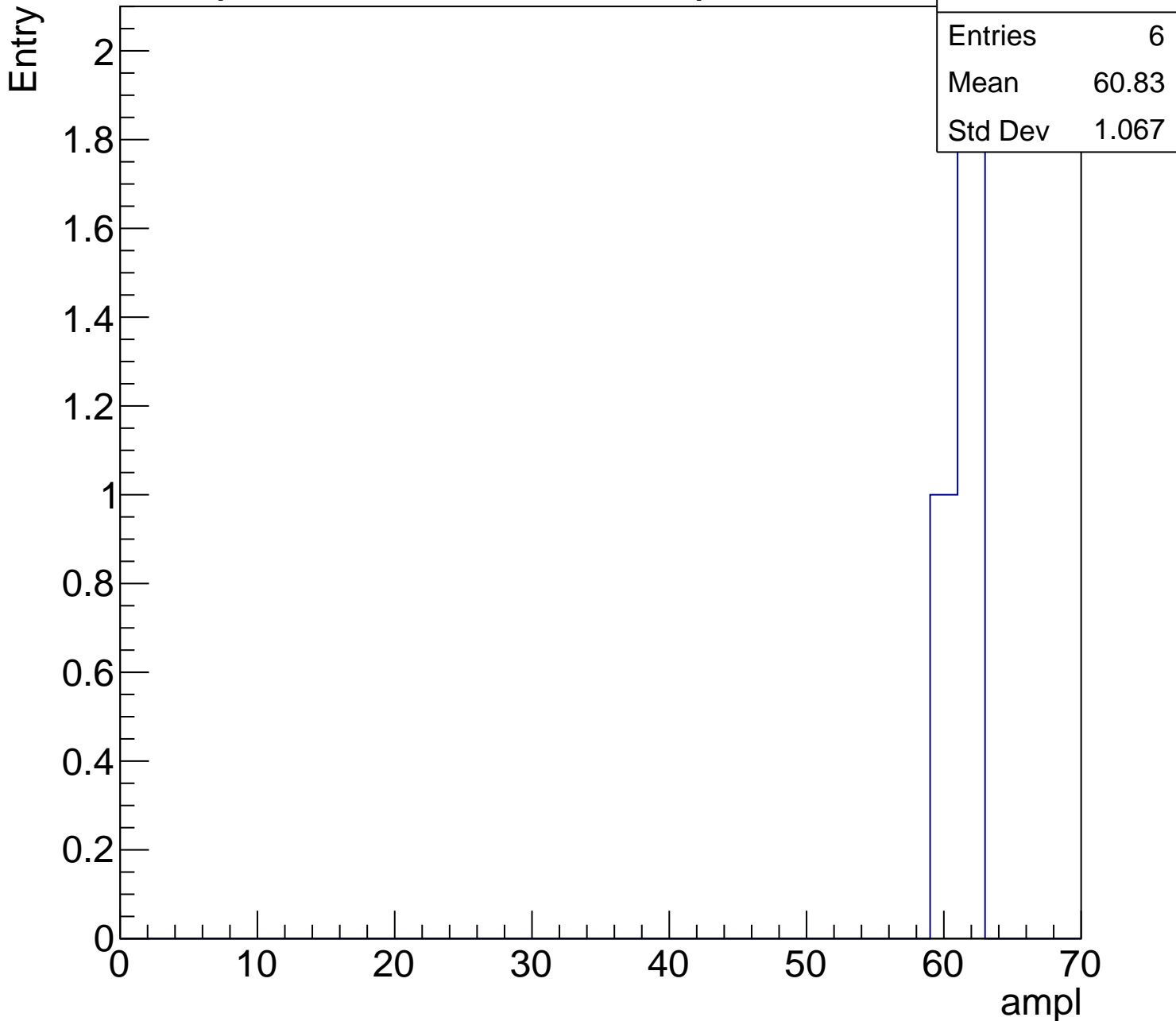
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	60.83
Std Dev	1.067

0 10 20 30 40 50 60 70

ampl





# B1L101S, U18-ch3, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U18-ch4, adc0

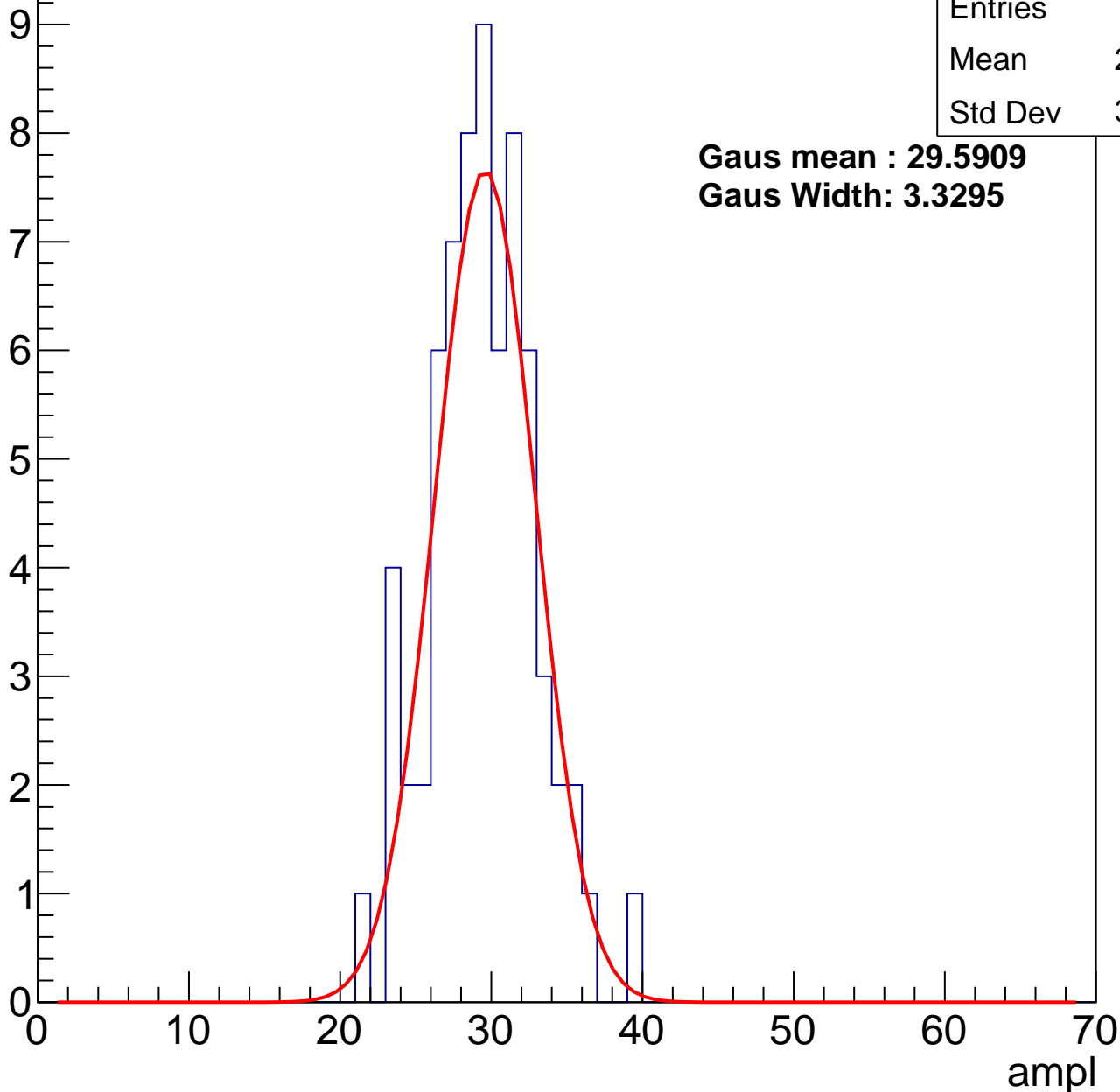
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	29.01
Std Dev	3.411

**Gaus mean : 29.5909**

**Gaus Width: 3.3295**



# B1L101S, U18-ch4, adc1

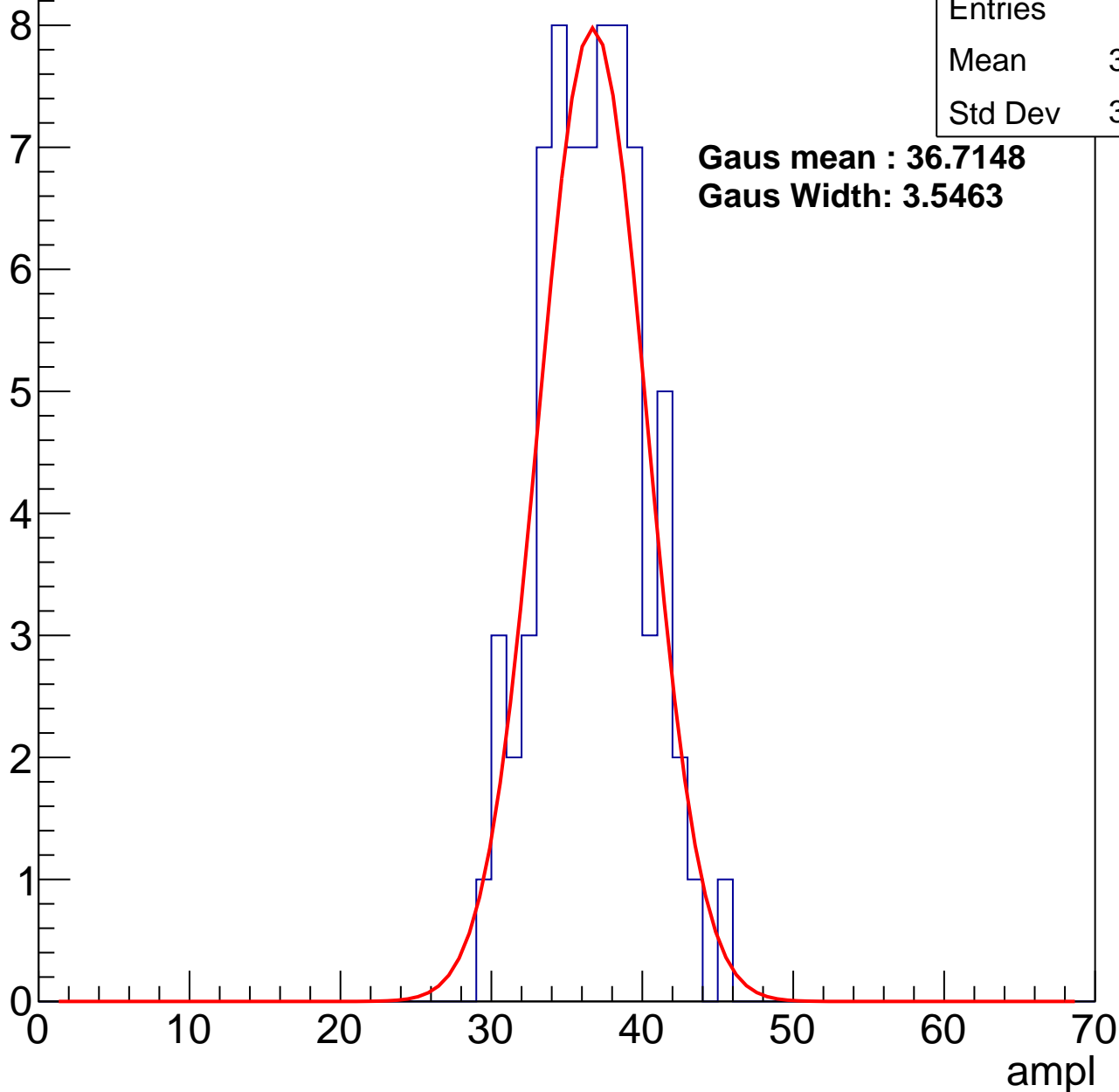
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	36.26
Std Dev	3.372

**Gaus mean : 36.7148**

**Gaus Width: 3.5463**



# B1L101S, U18-ch4, adc2

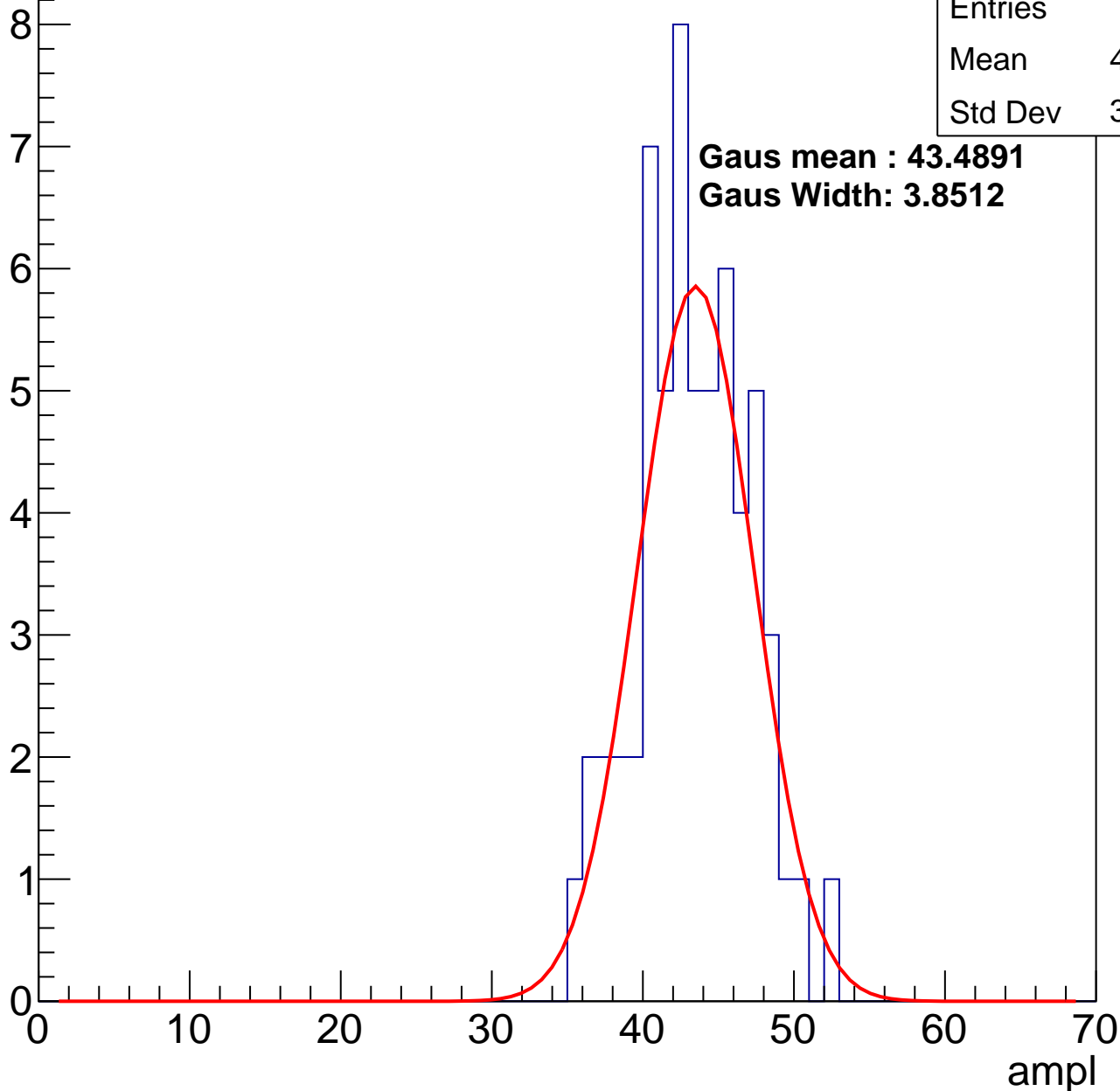
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	42.92
Std Dev	3.635

**Gaus mean : 43.4891**

**Gaus Width: 3.8512**

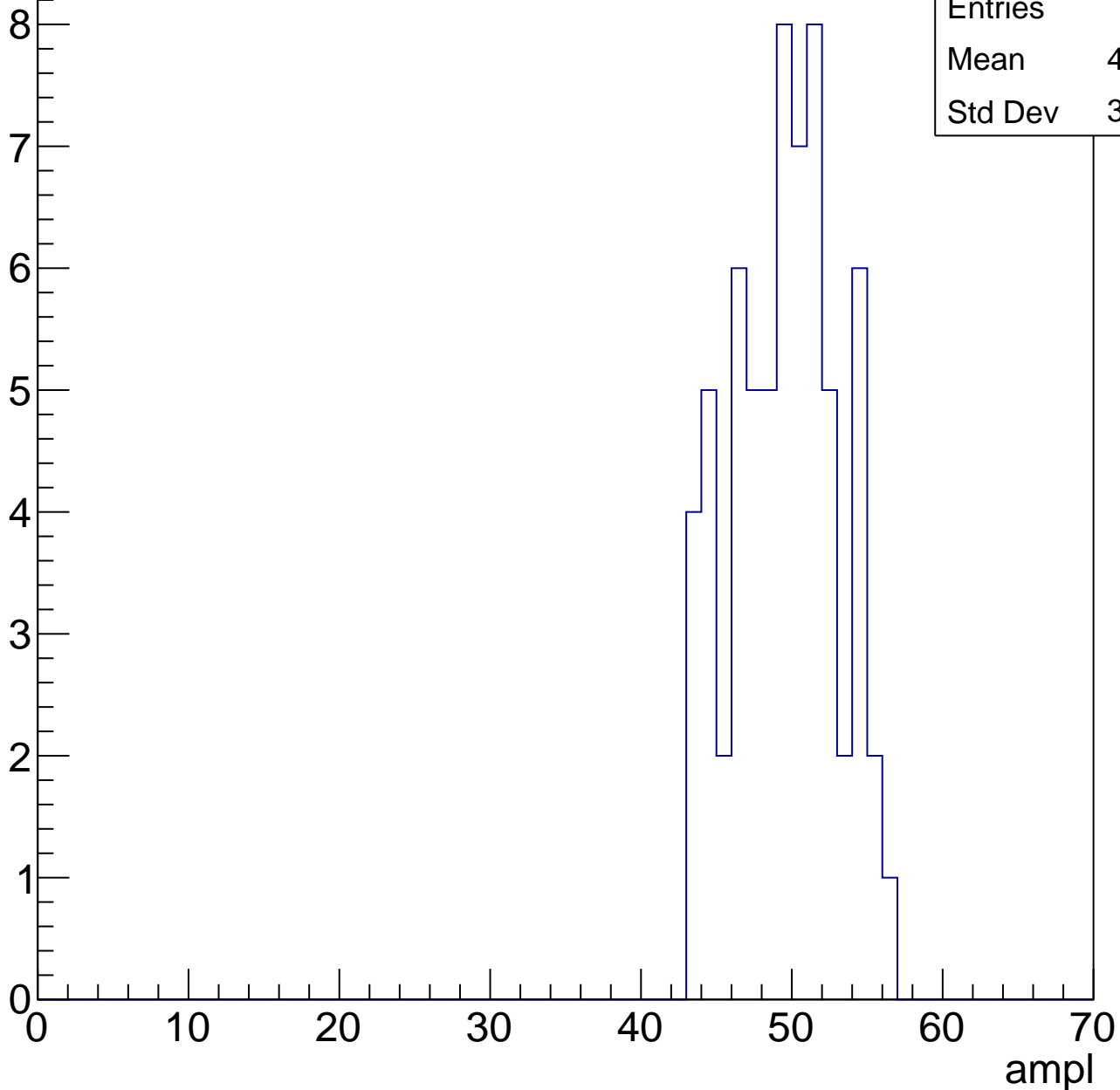


# B1L101S, U18-ch4, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	49.08
Std Dev	3.408

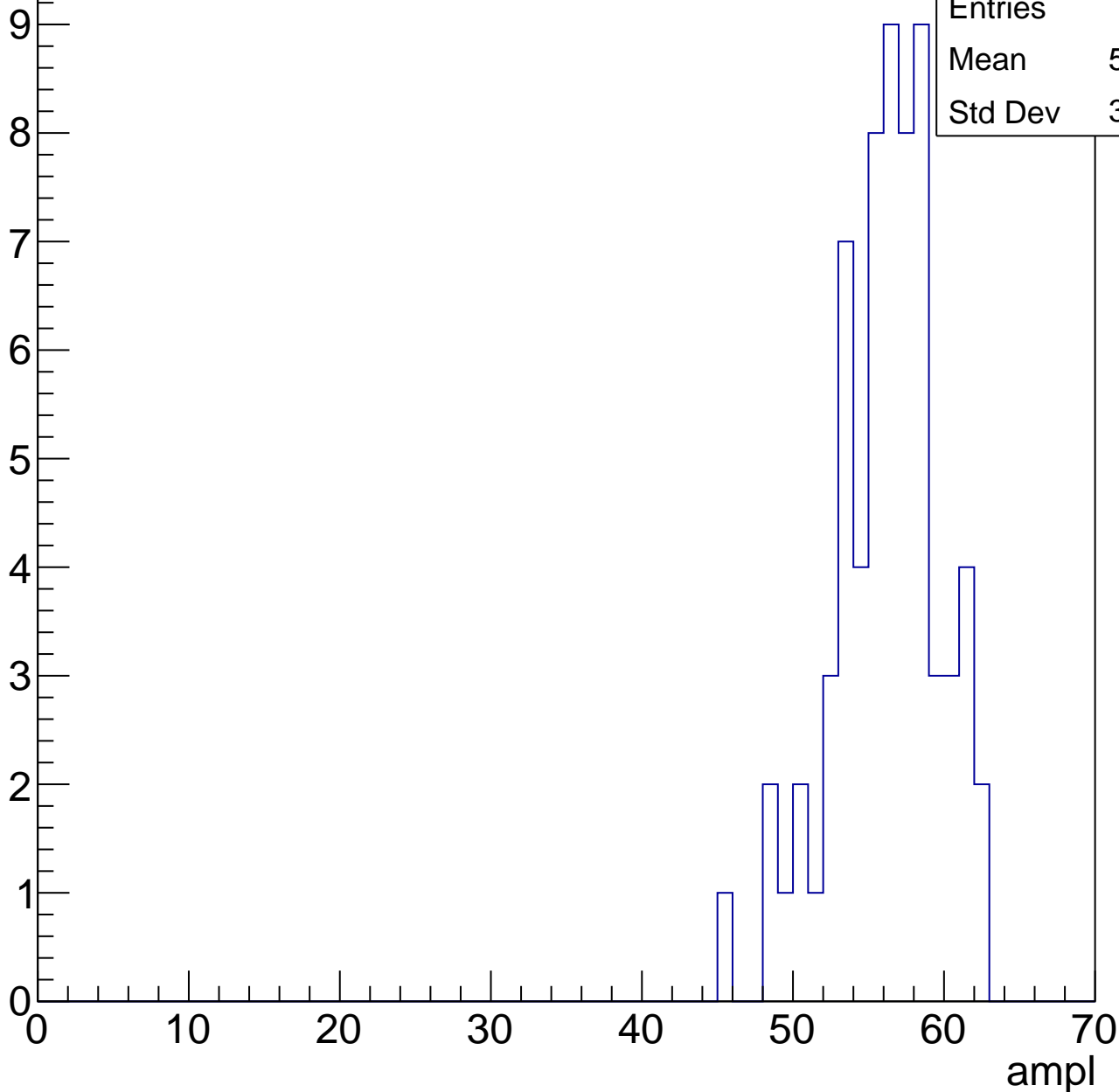


# B1L101S, U18-ch4, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	55.69
Std Dev	3.486

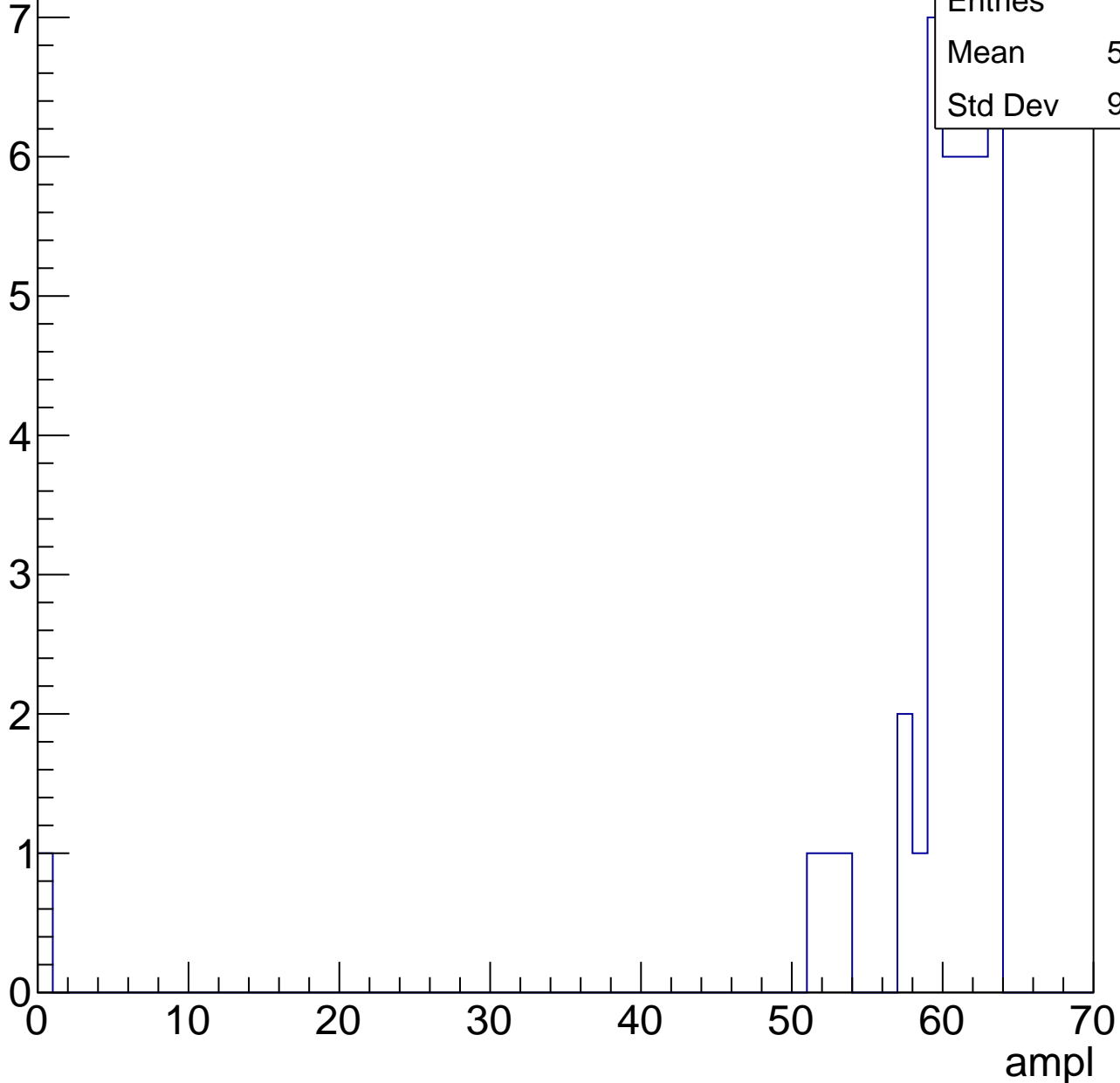


# B1L101S, U18-ch4, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	39
Mean	58.46
Std Dev	9.902



# B1L101S, U18-ch4, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch4, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	20
Std Dev	0

ampl

# B1L101S, U18-ch5, adc0

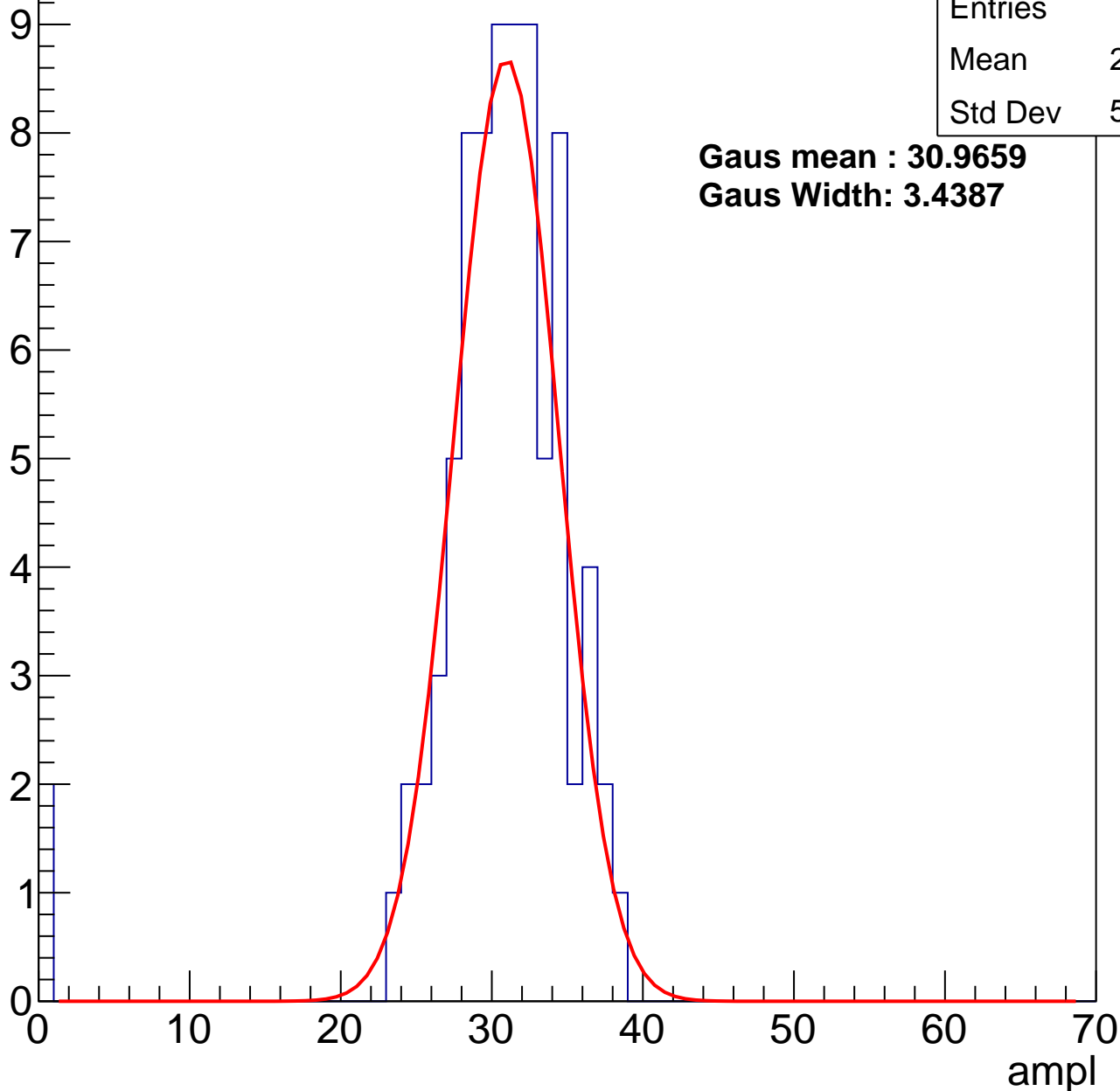
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	80
Mean	29.88
Std Dev	5.784

**Gaus mean : 30.9659**

**Gaus Width: 3.4387**



# B1L101S, U18-ch5, adc1

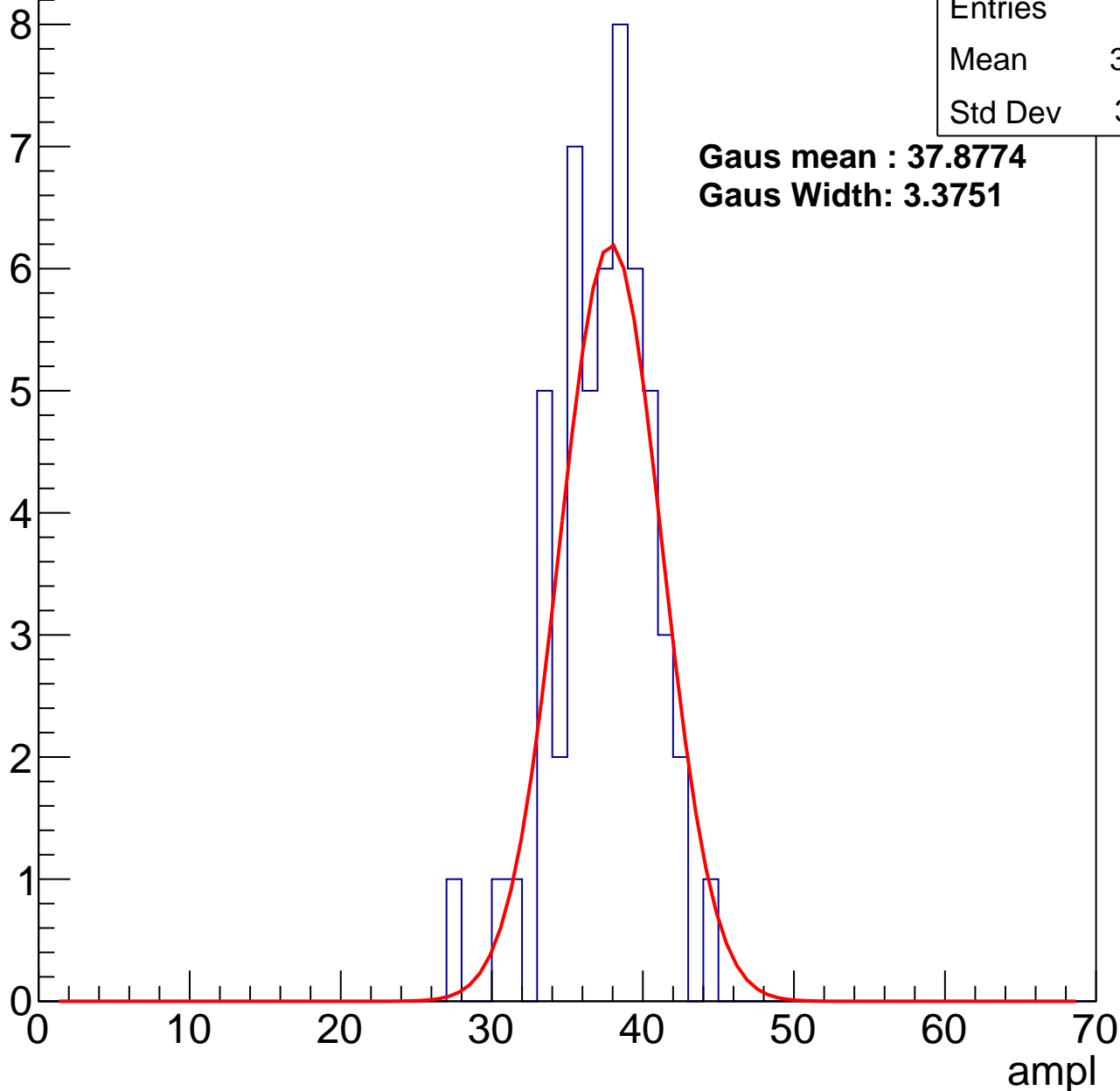
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	36.92
Std Dev	3.191

**Gaus mean : 37.8774**

**Gaus Width: 3.3751**



# B1L101S, U18-ch5, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	72
Mean	43.58
Std Dev	3.574

**Gaus mean : 44.3468**

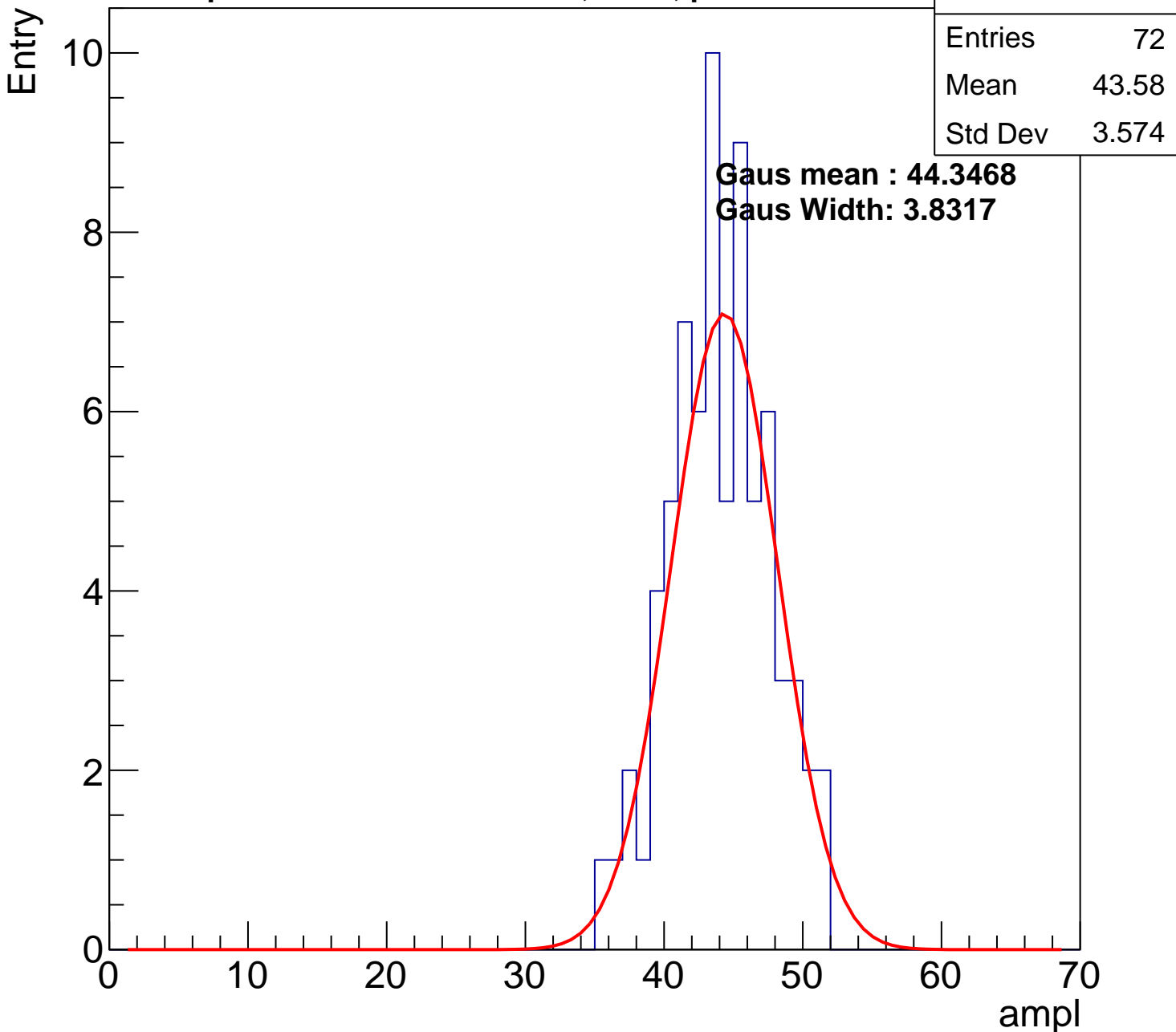
**Gaus Width: 3.8317**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

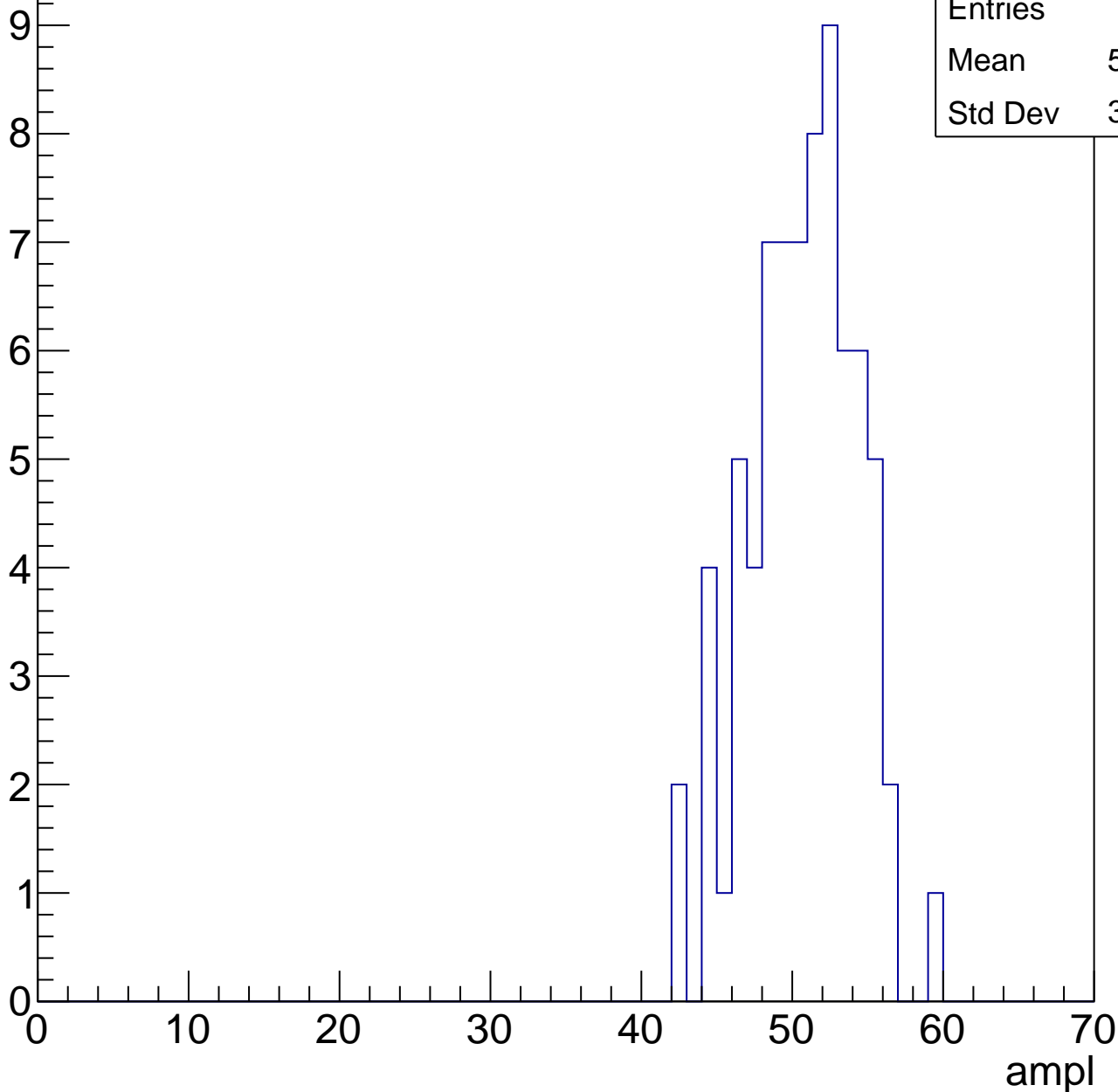


# B1L101S, U18-ch5, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	50.22
Std Dev	3.519

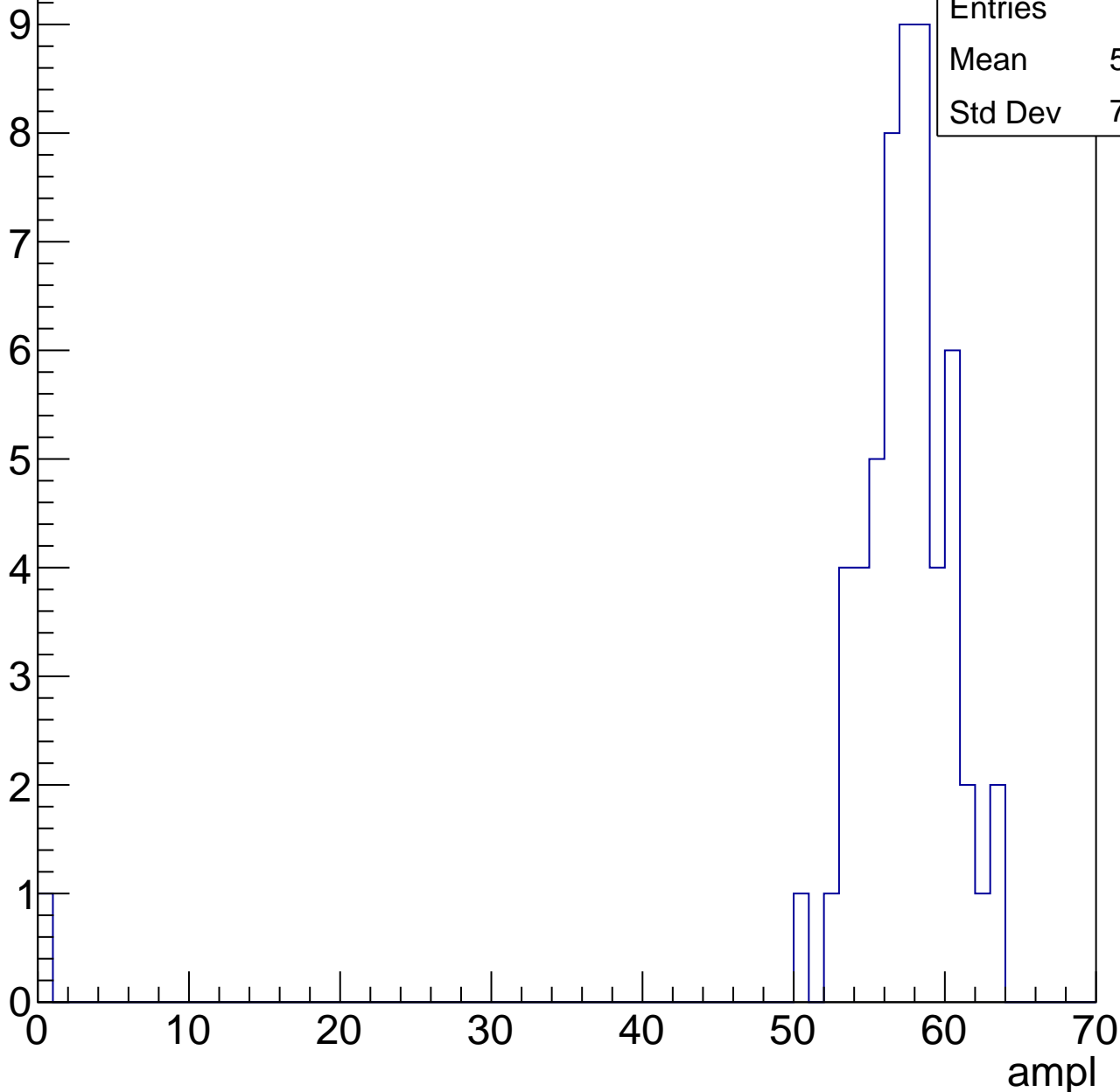


# B1L101S, U18-ch5, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	56.04
Std Dev	7.954



# B1L101S, U18-ch5, adc5

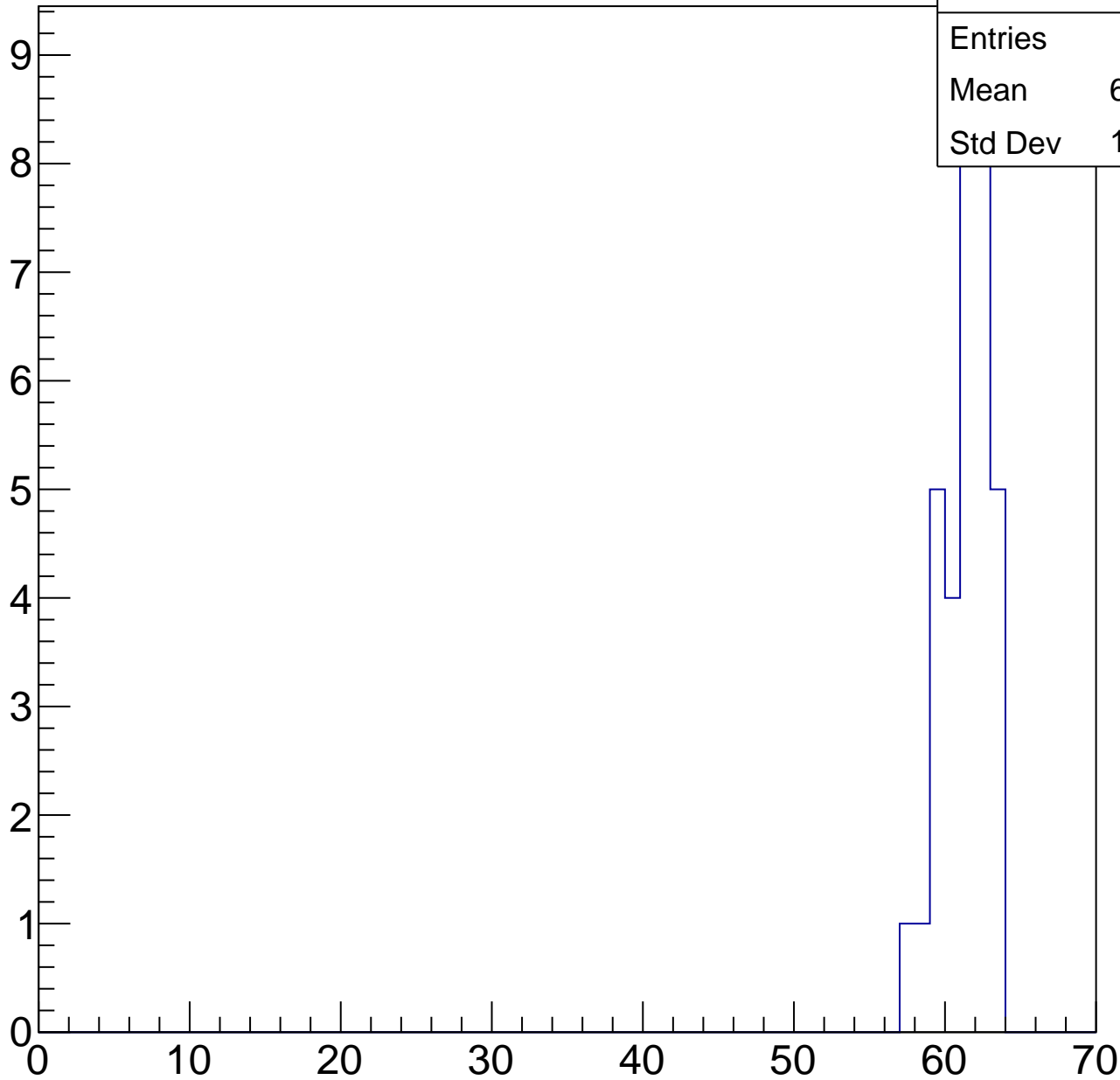
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	33
Mean	60.94
Std Dev	1.536

ampl



# B1L101S, U18-ch5, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch5, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U18-ch6, adc0

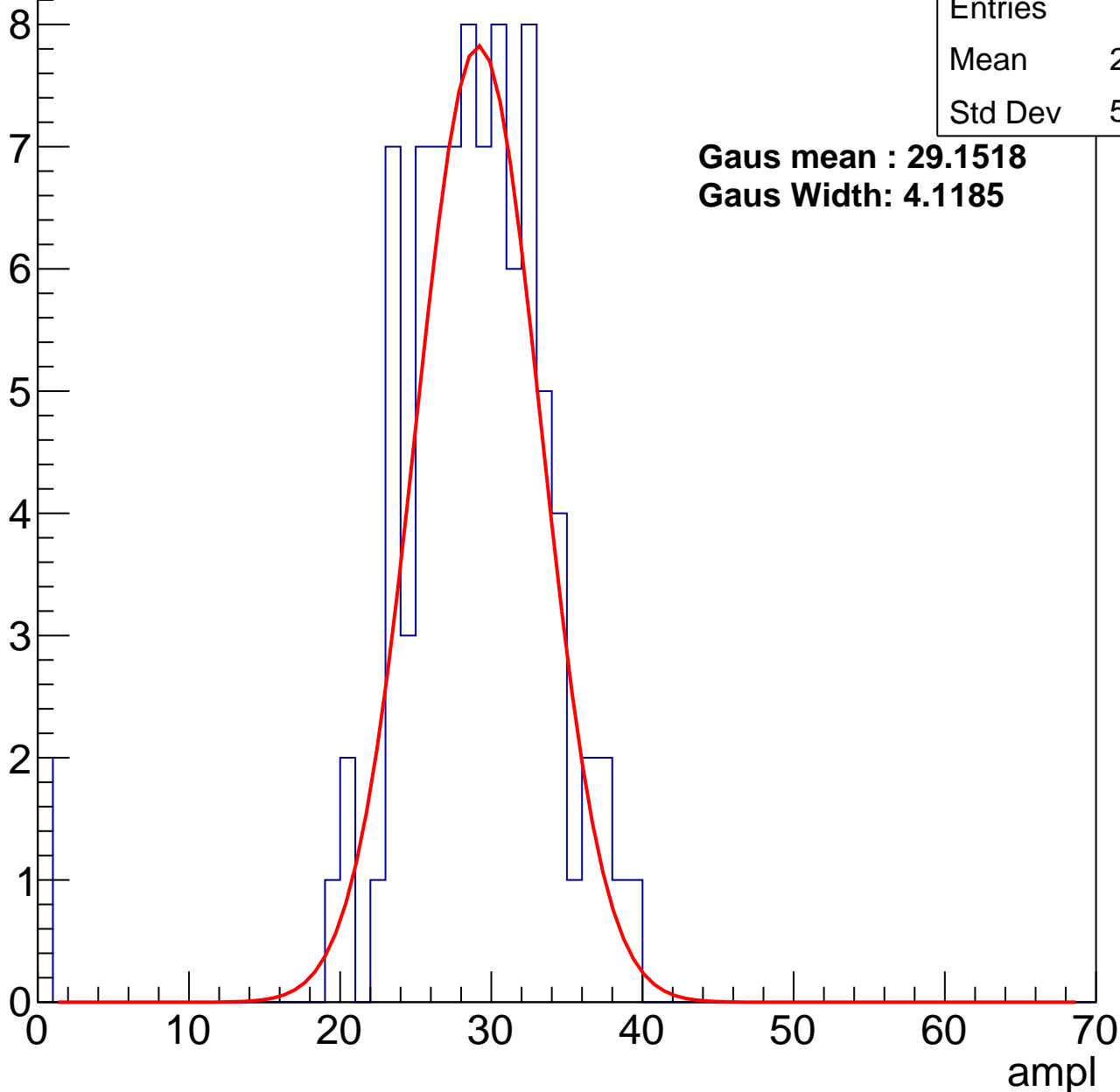
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	90
Mean	28.09
Std Dev	5.947

**Gaus mean : 29.1518**

**Gaus Width: 4.1185**



# B1L101S, U18-ch6, adc1

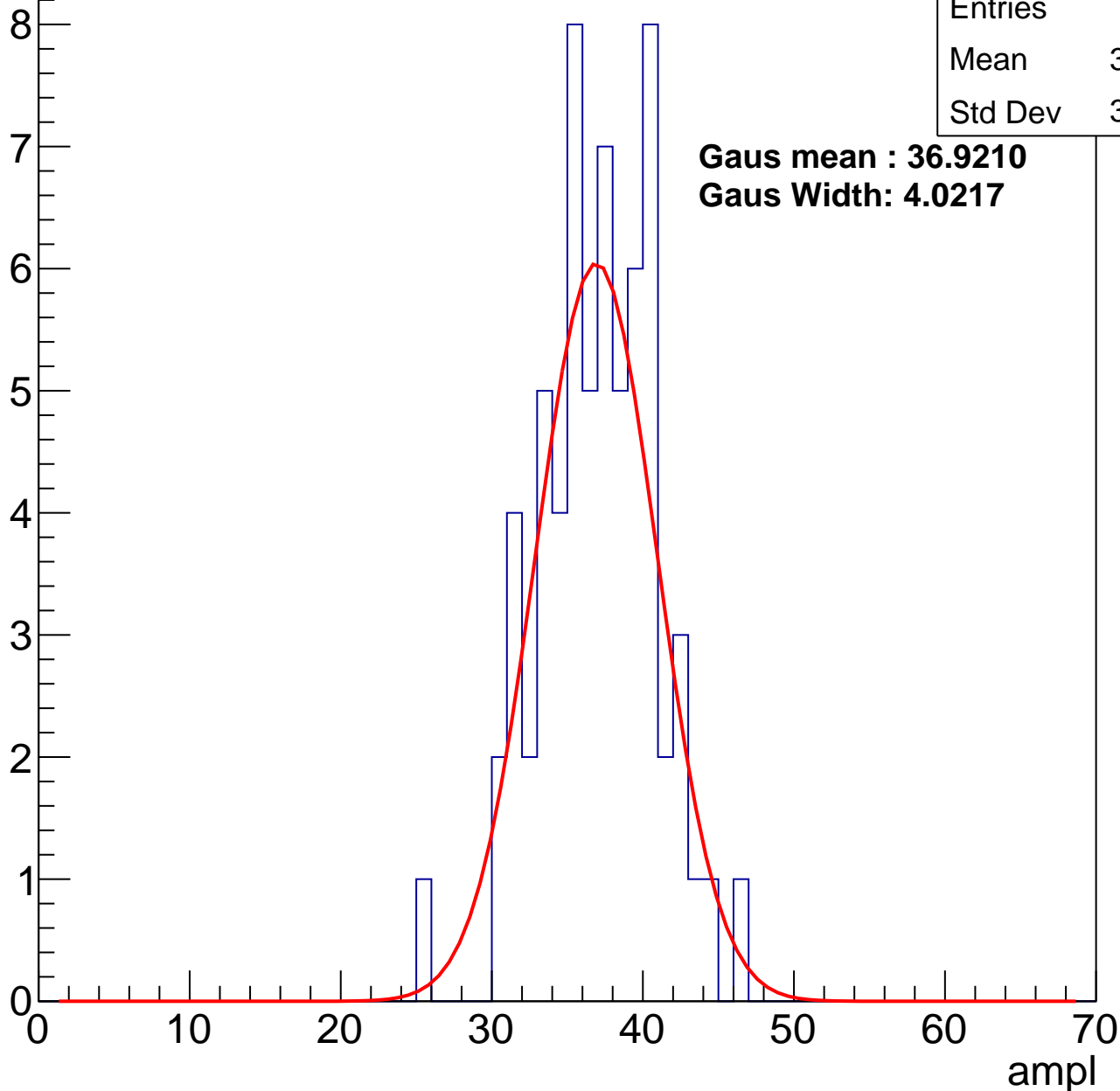
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	36.58
Std Dev	3.827

**Gaus mean : 36.9210**

**Gaus Width: 4.0217**



# B1L101S, U18-ch6, adc2

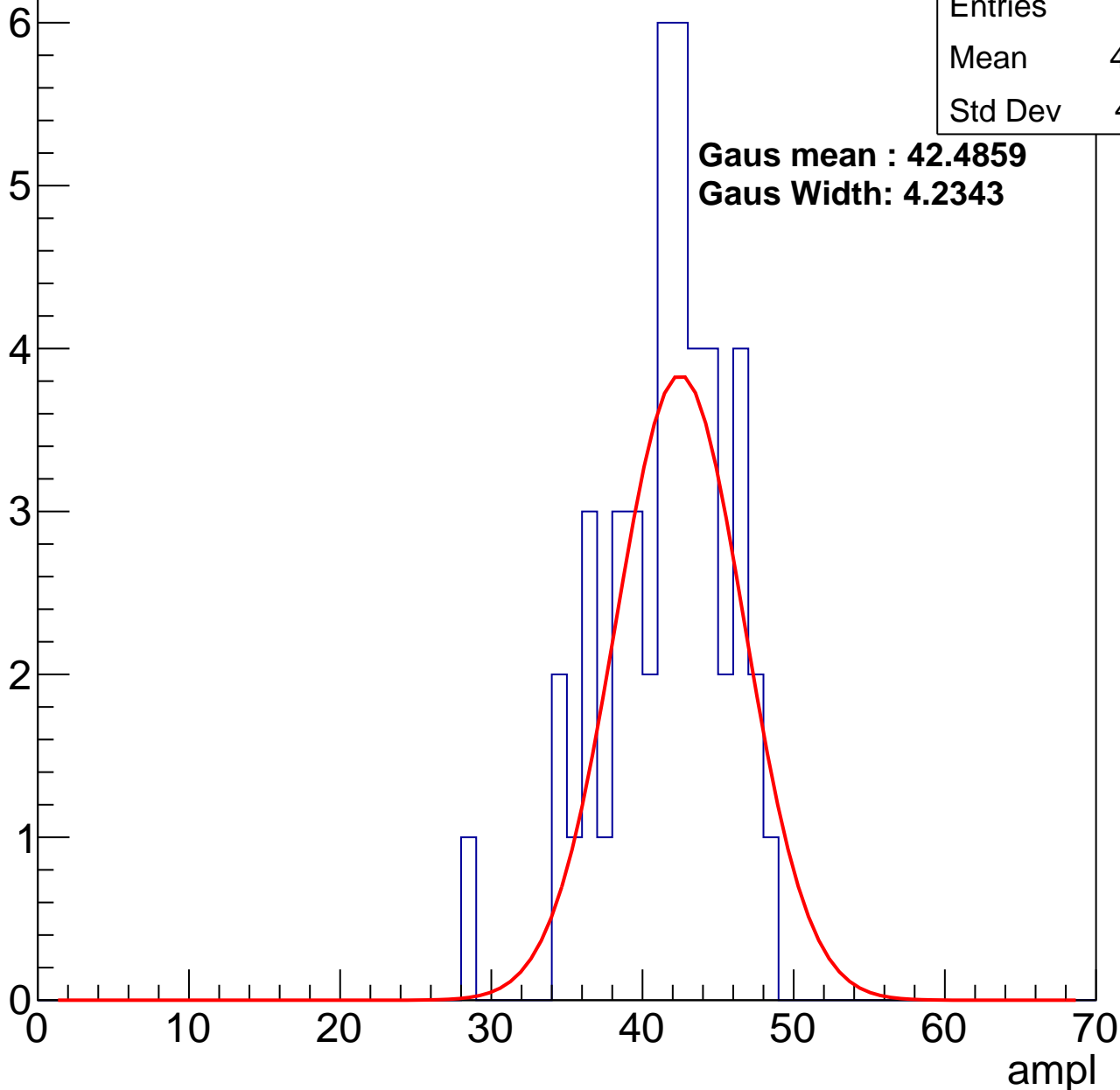
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	45
Mean	41.09
Std Dev	4.071

**Gaus mean : 42.4859**

**Gaus Width: 4.2343**

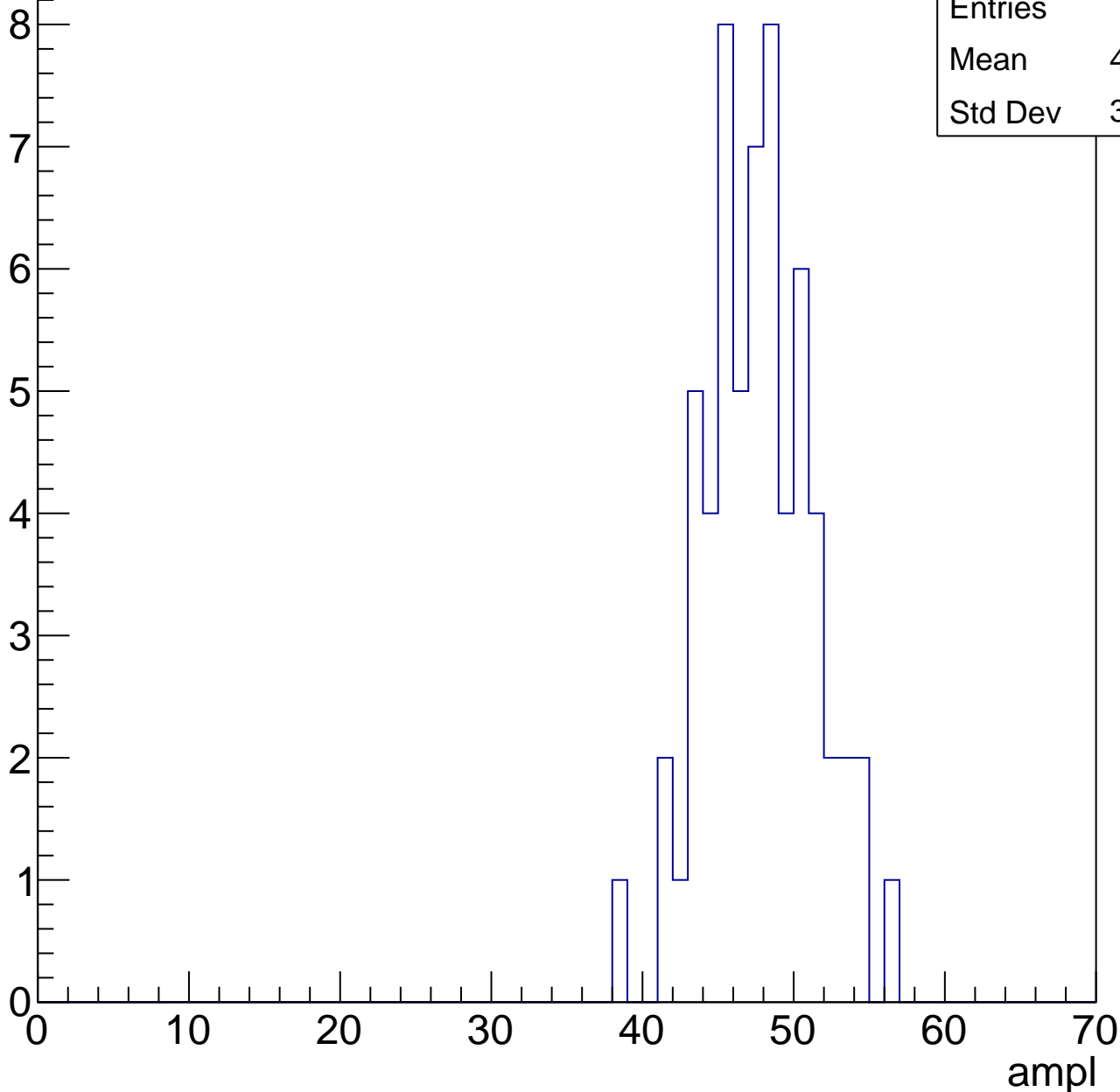


# B1L101S, U18-ch6, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	47.26
Std Dev	3.524

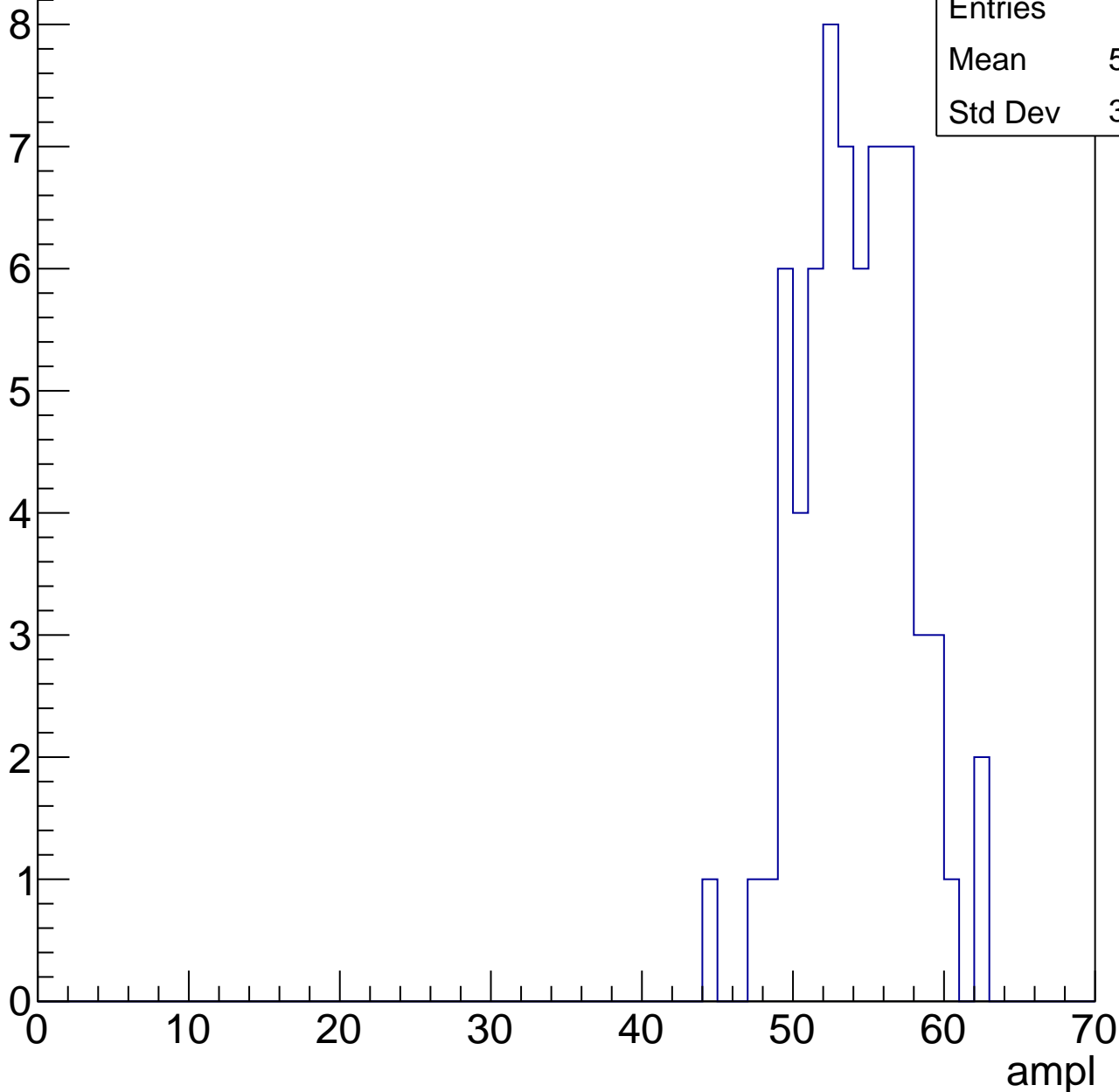


# B1L101S, U18-ch6, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

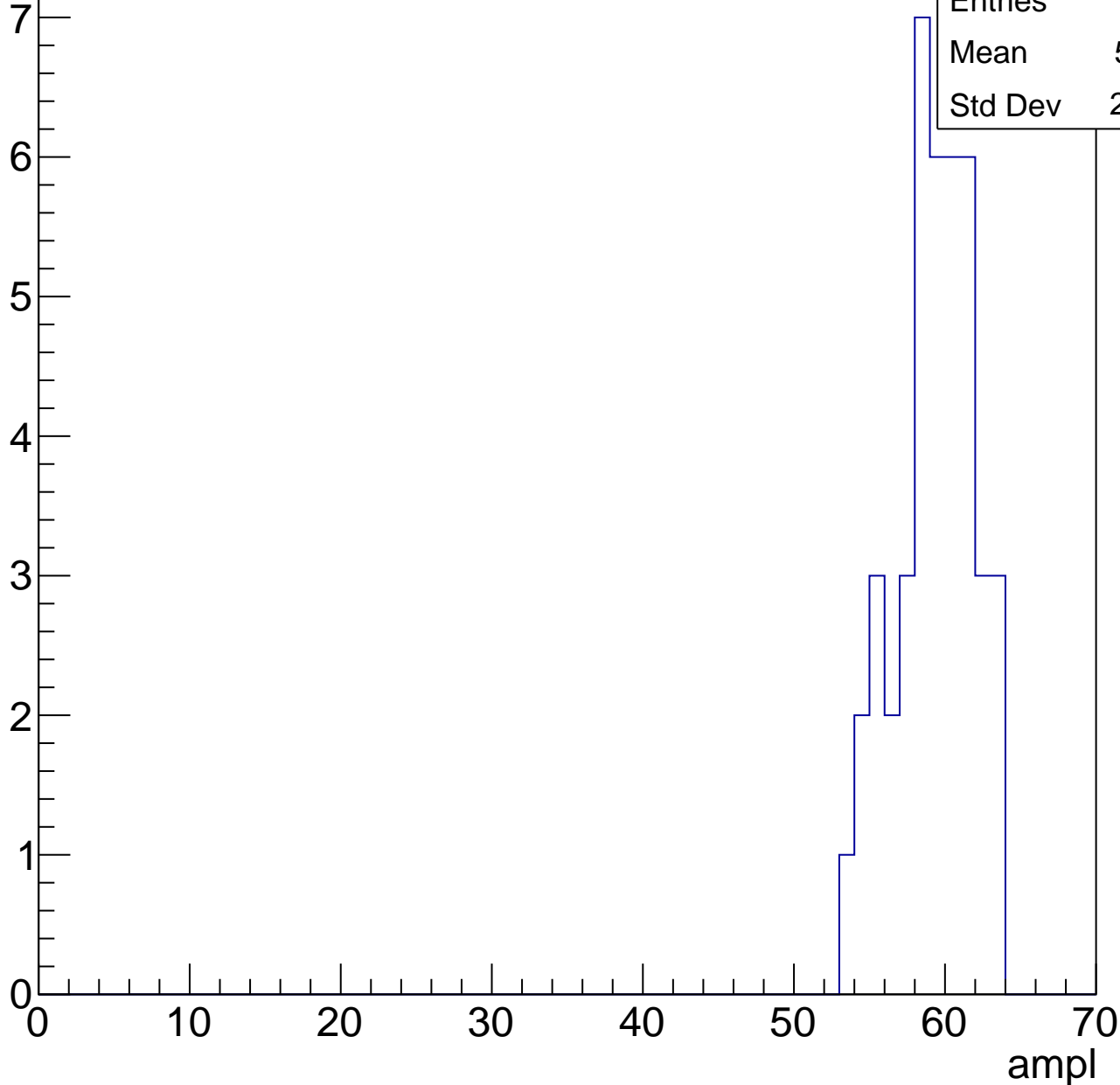
Entries	70
Mean	53.73
Std Dev	3.529



# B1L101S, U18-ch6, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

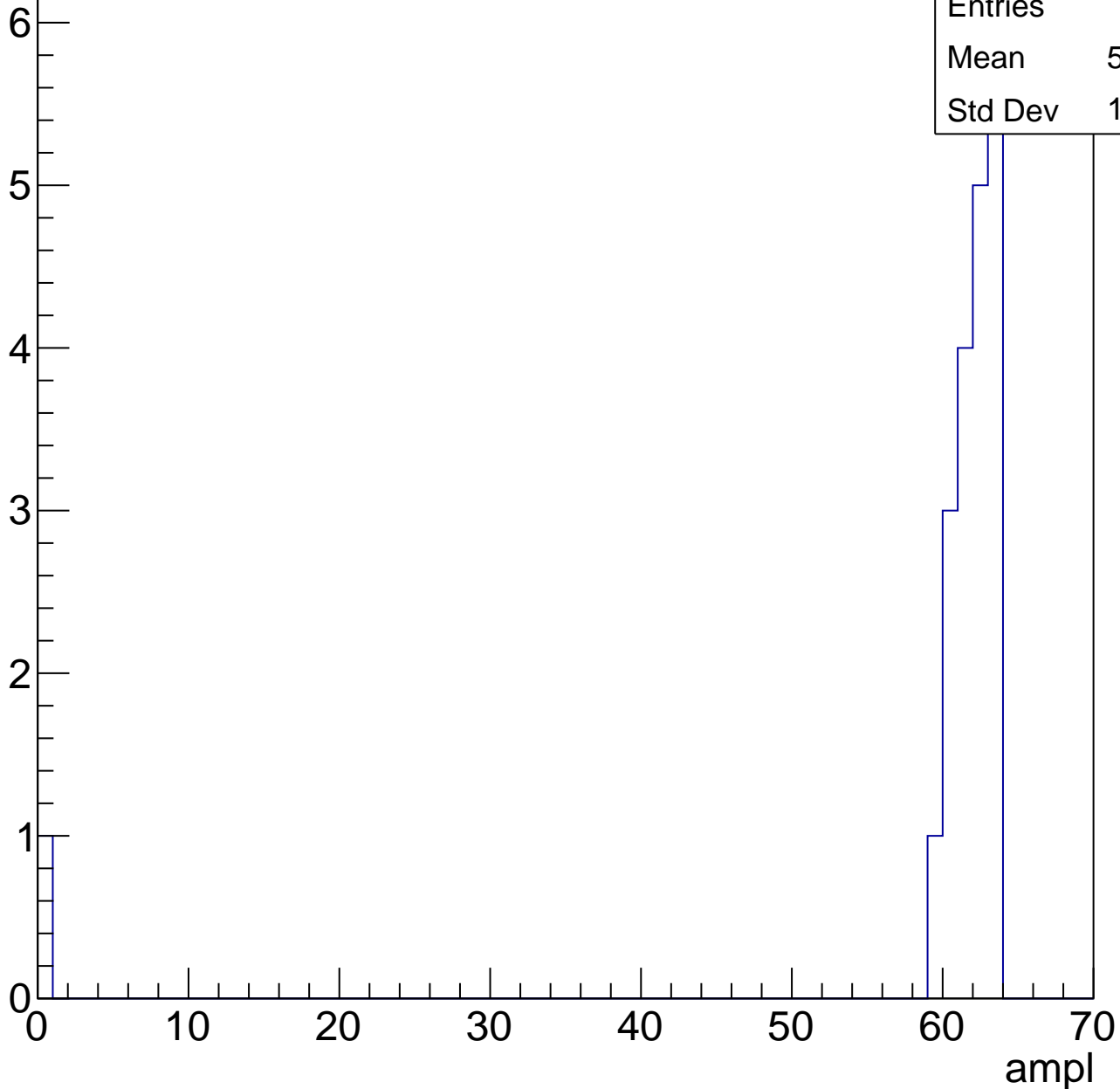


# B1L101S, U18-ch6, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	20
Mean	58.55
Std Dev	13.49





# B1L101S, U18-ch6, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch7, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	73
Mean	29.25
Std Dev	3.799

**Gaus mean : 29.1280**

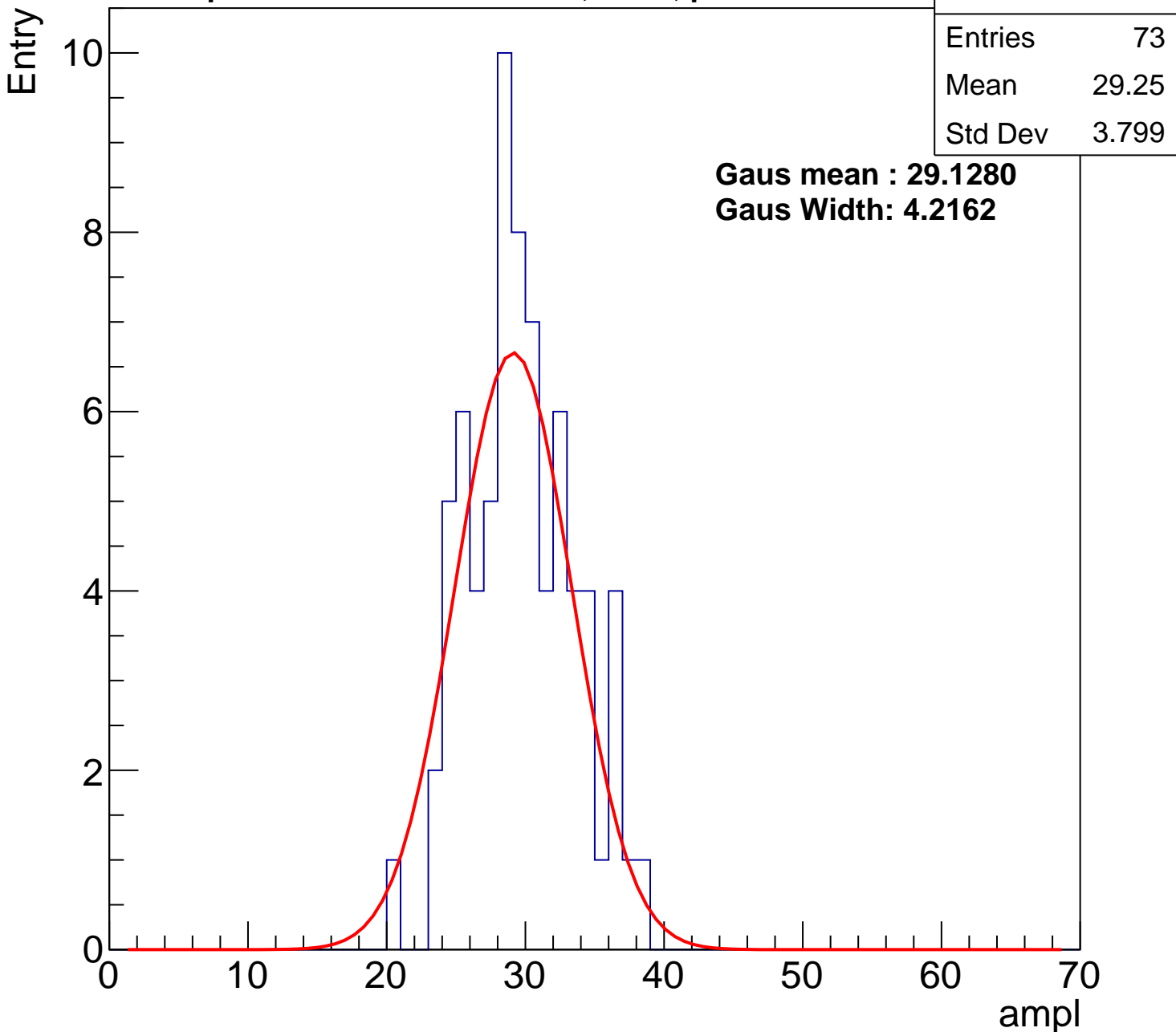
**Gaus Width: 4.2162**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U18-ch7, adc1

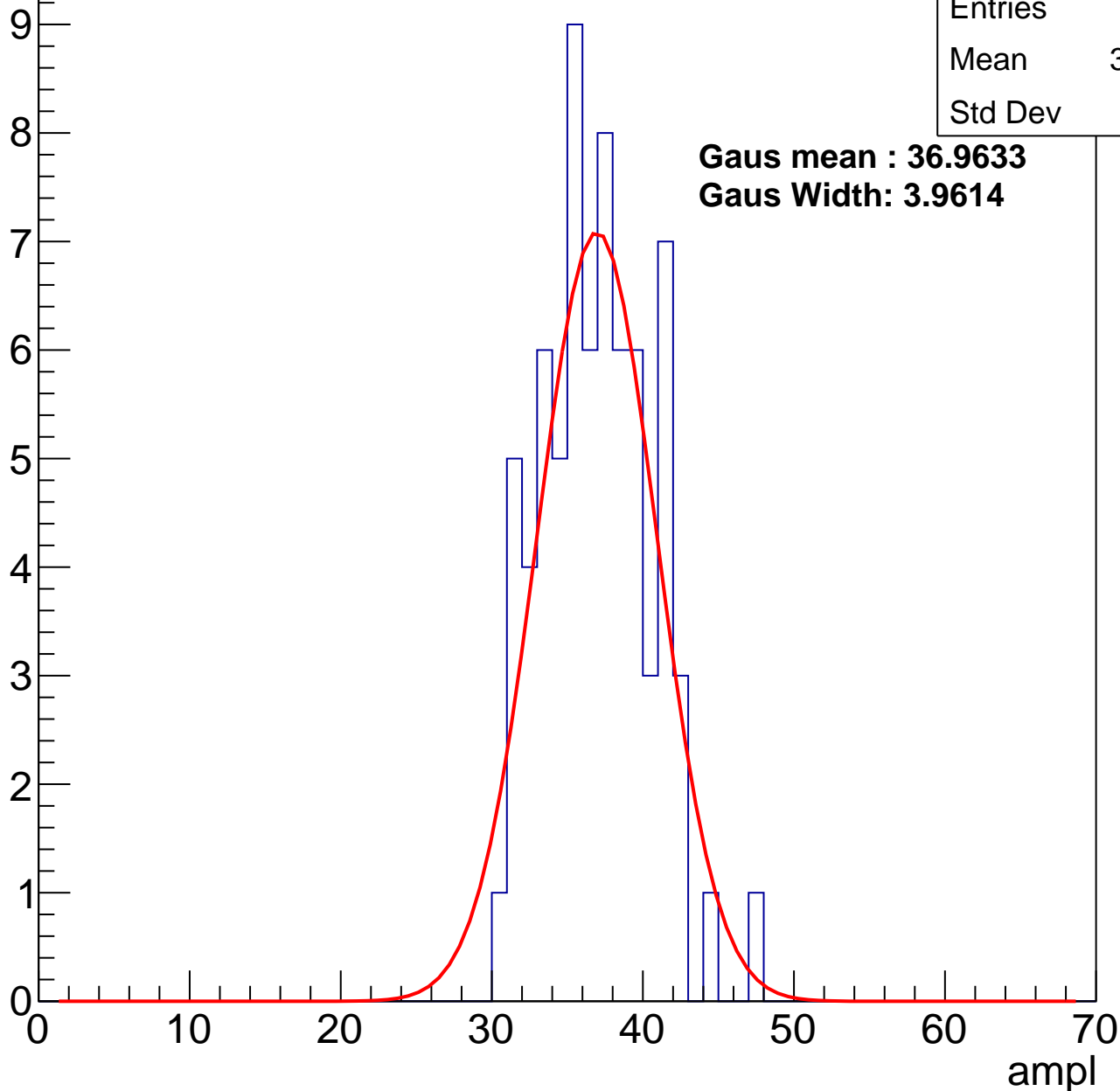
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	36.54
Std Dev	3.54

**Gaus mean : 36.9633**

**Gaus Width: 3.9614**



# B1L101S, U18-ch7, adc2

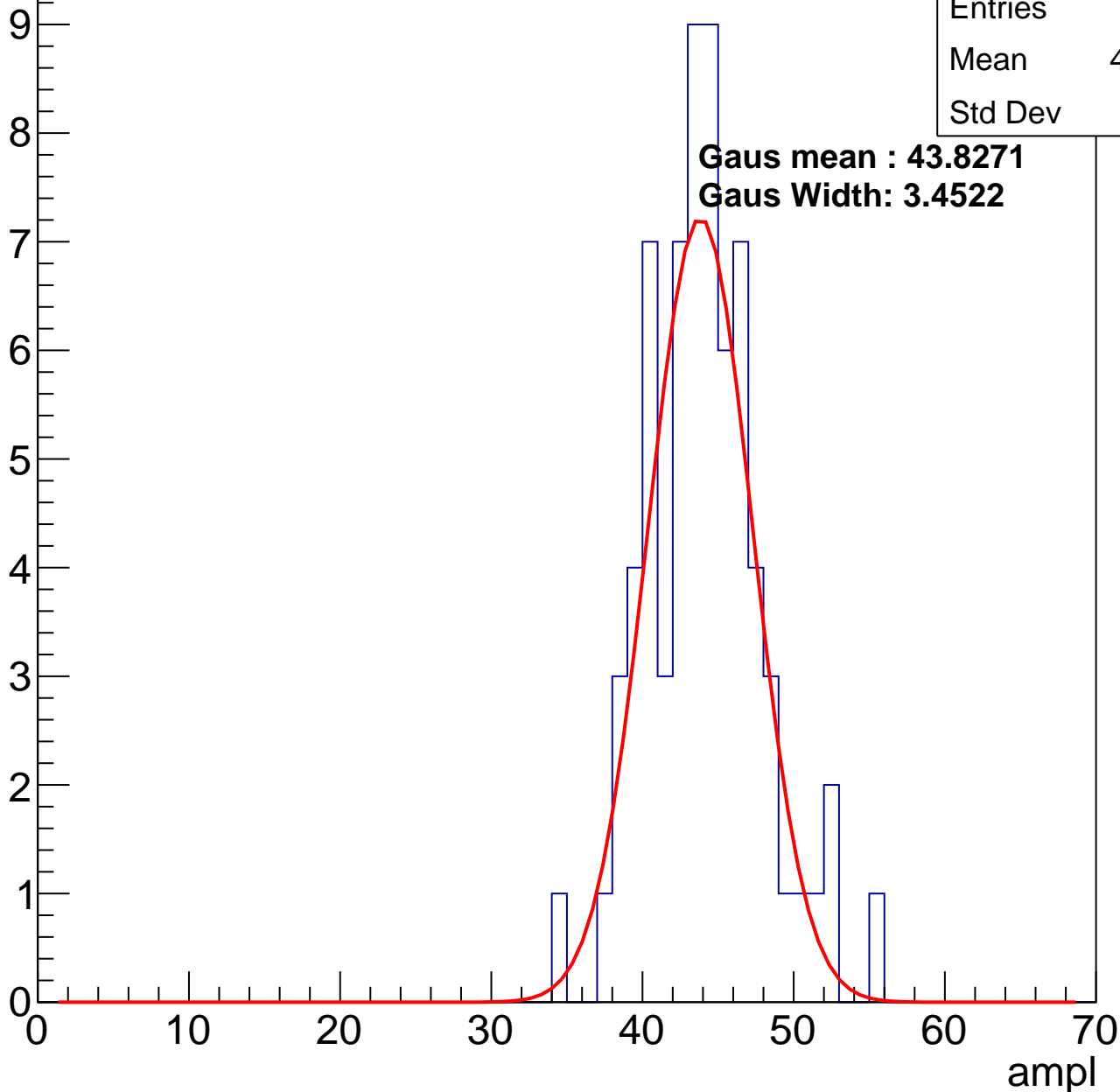
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	43.63
Std Dev	3.78

**Gaus mean : 43.8271**

**Gaus Width: 3.4522**

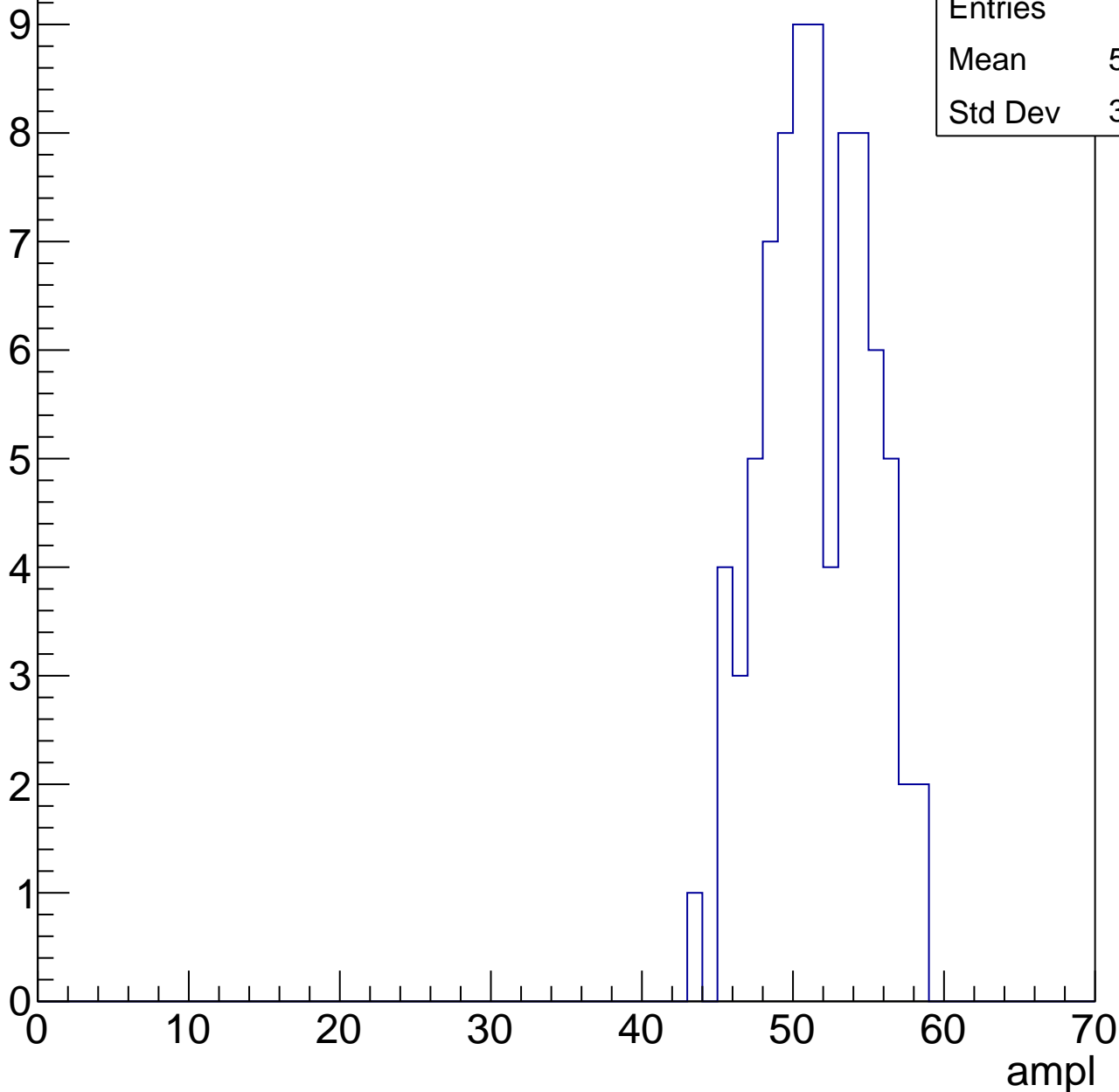


# B1L101S, U18-ch7, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	81
Mean	51.07
Std Dev	3.453

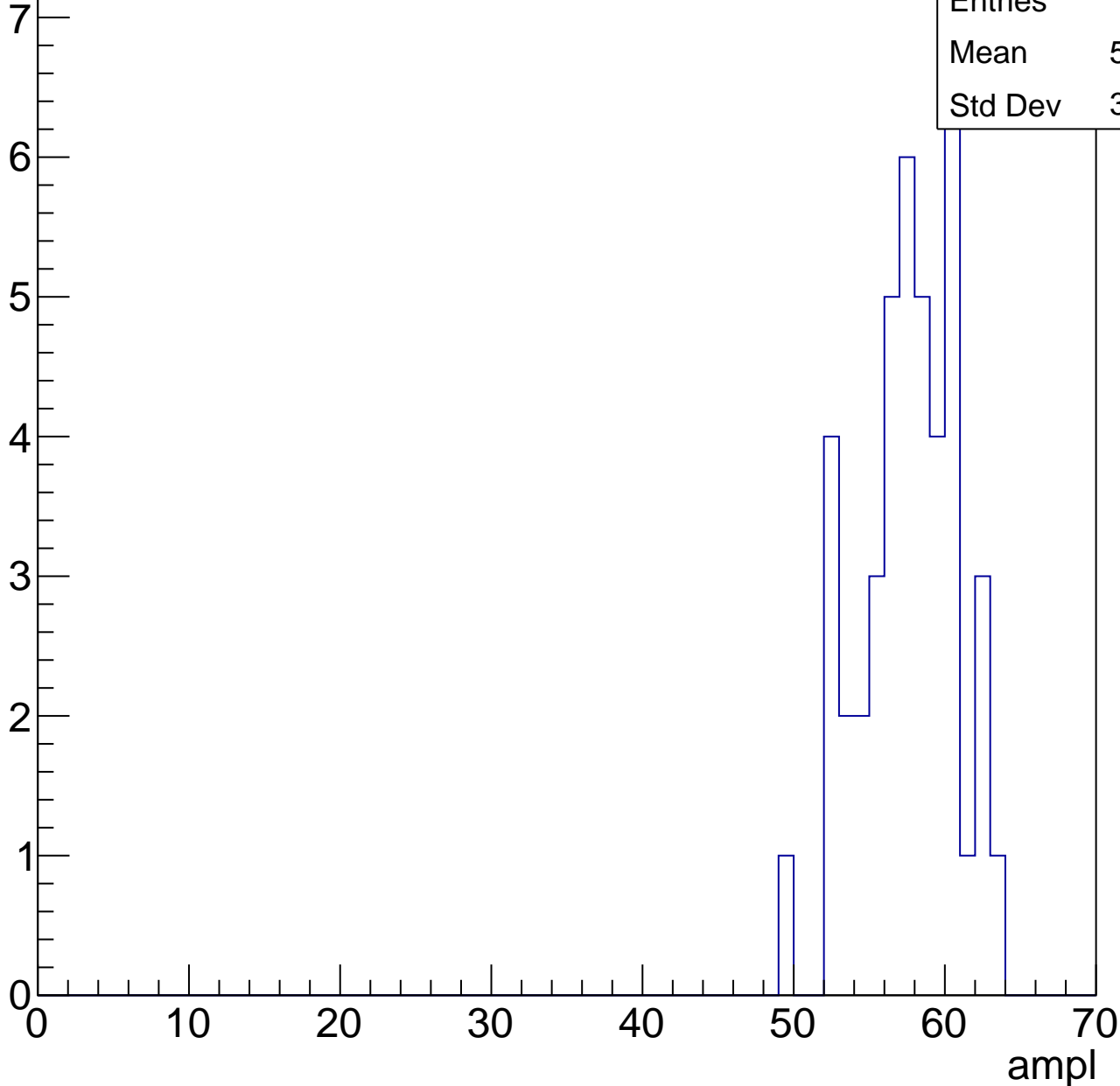


# B1L101S, U18-ch7, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	44
Mean	57.14
Std Dev	3.167

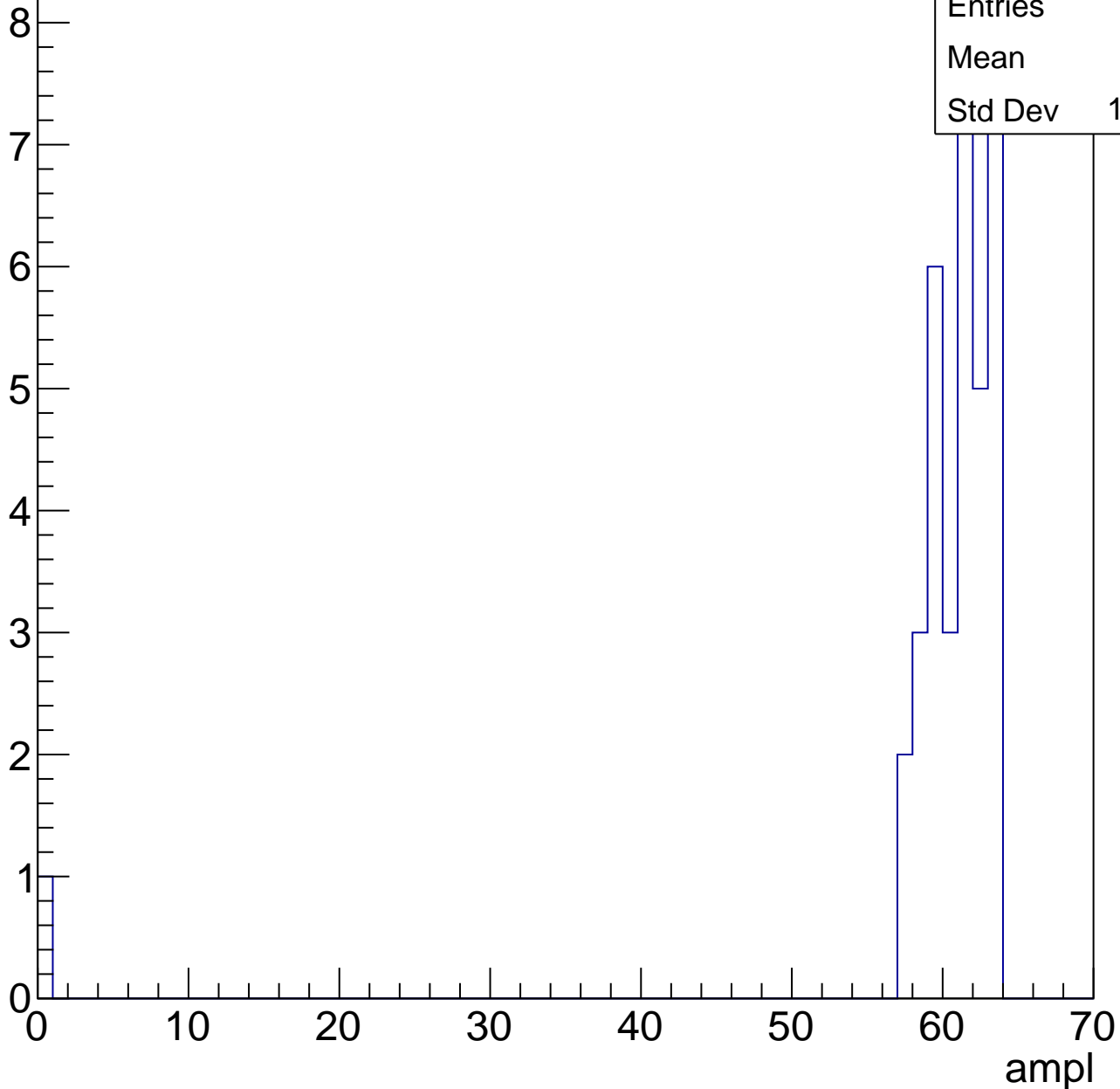


# B1L101S, U18-ch7, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

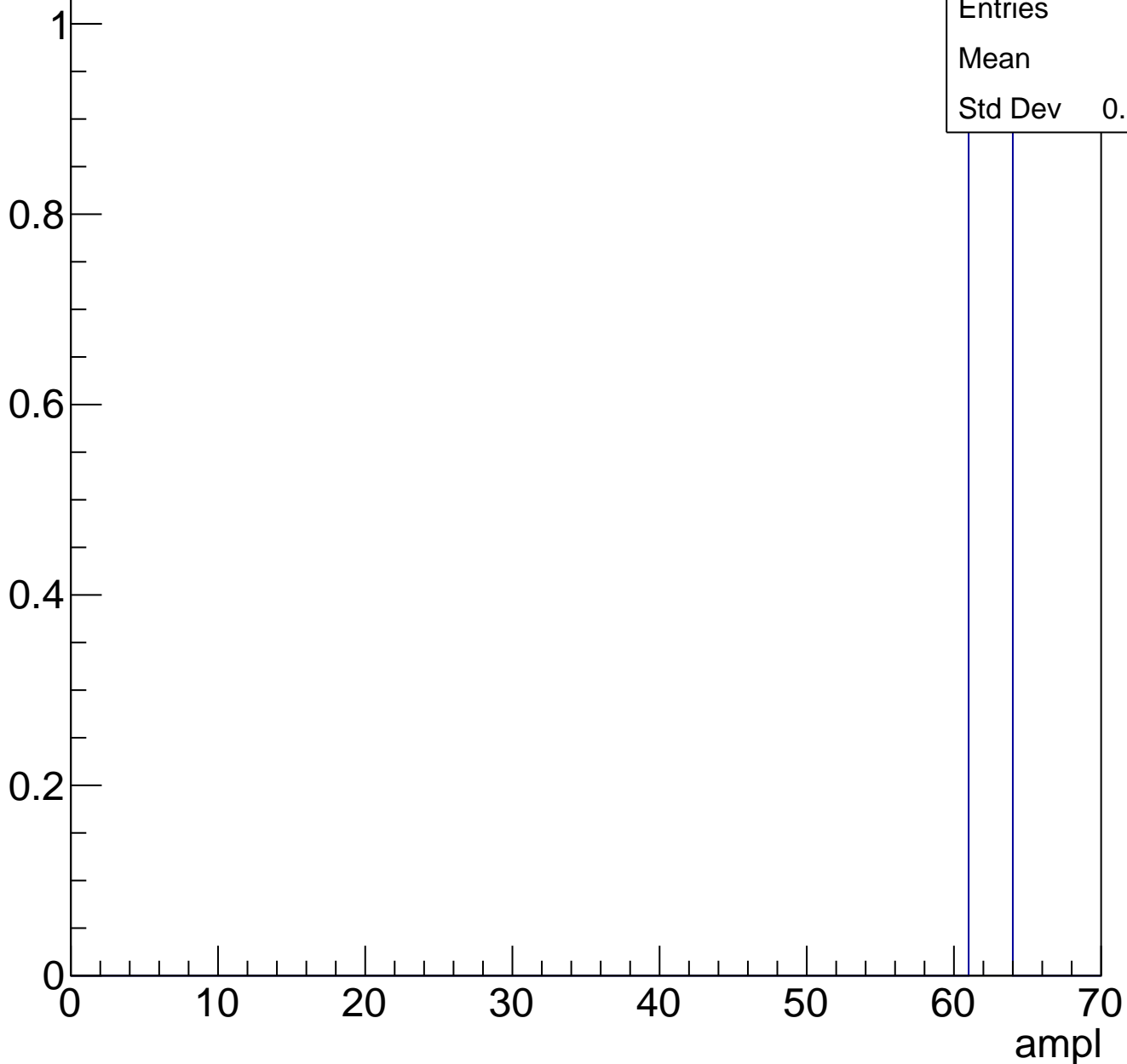
Entries	36
Mean	59
Std Dev	10.14



# B1L101S, U18-ch7, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch7, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch8, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	85
Mean	28.65
Std Dev	5.735

**Gaus mean : 30.0196**

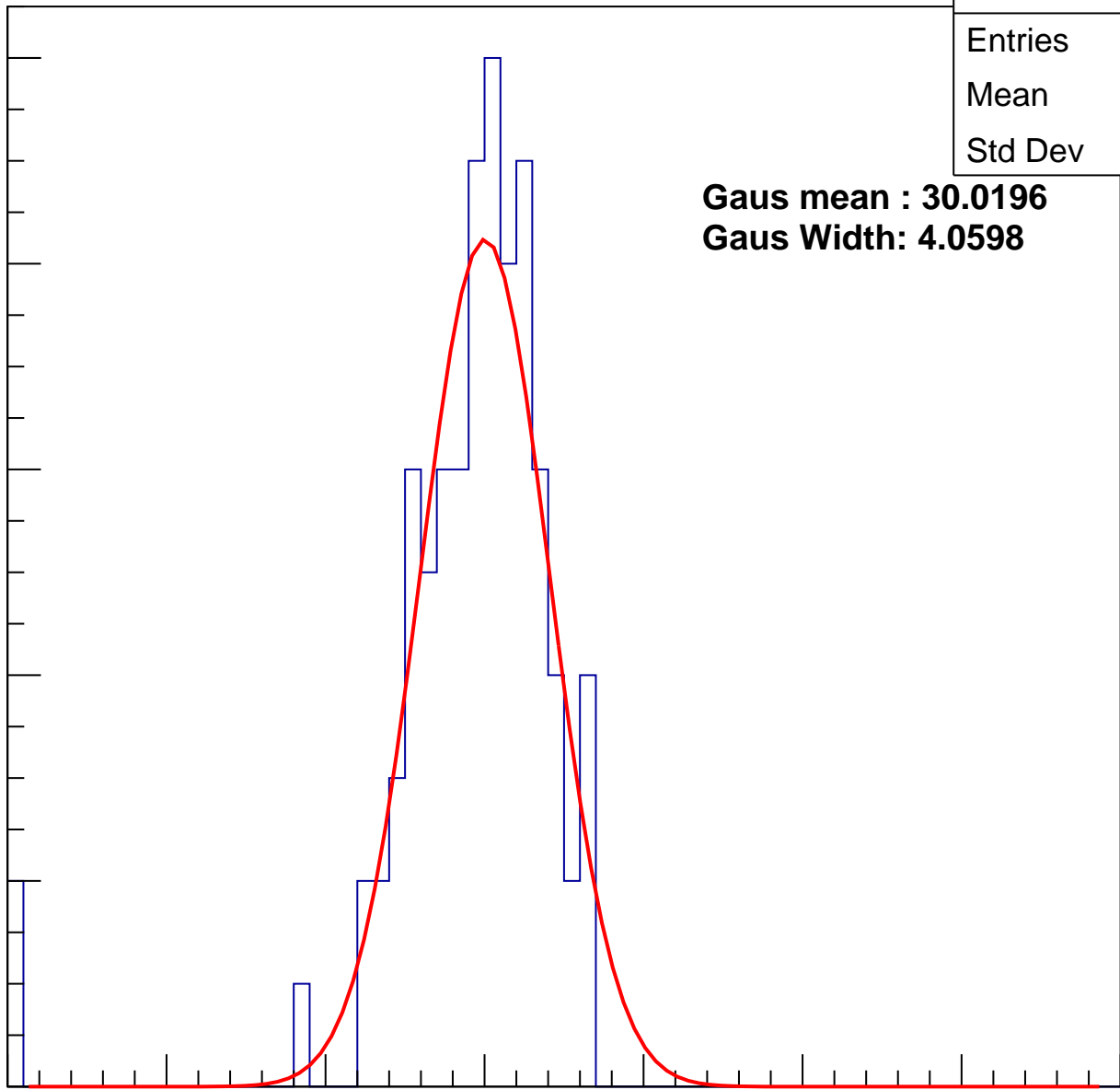
**Gaus Width: 4.0598**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U18-ch8, adc1

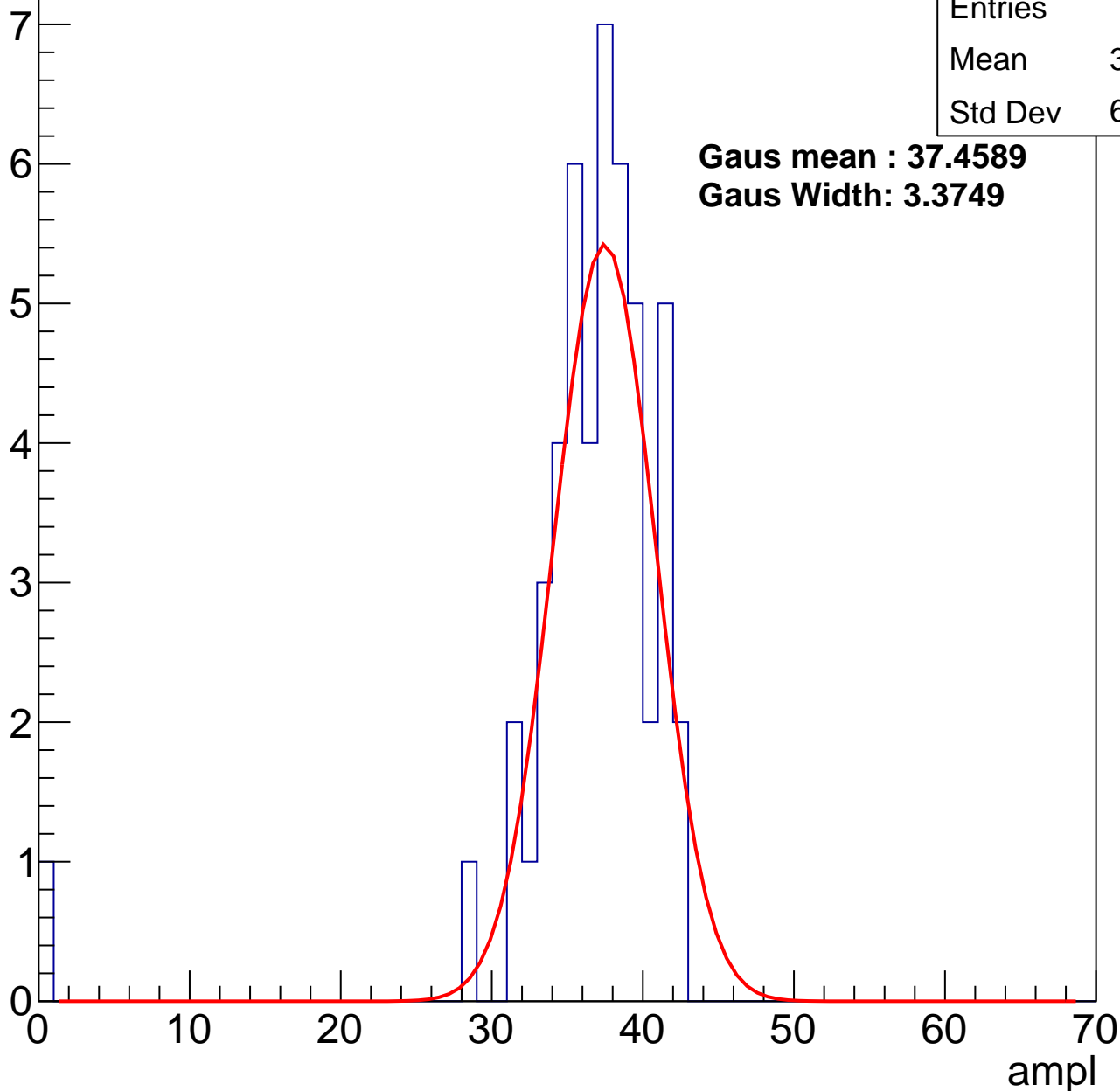
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	49
Mean	35.96
Std Dev	6.027

**Gaus mean : 37.4589**

**Gaus Width: 3.3749**

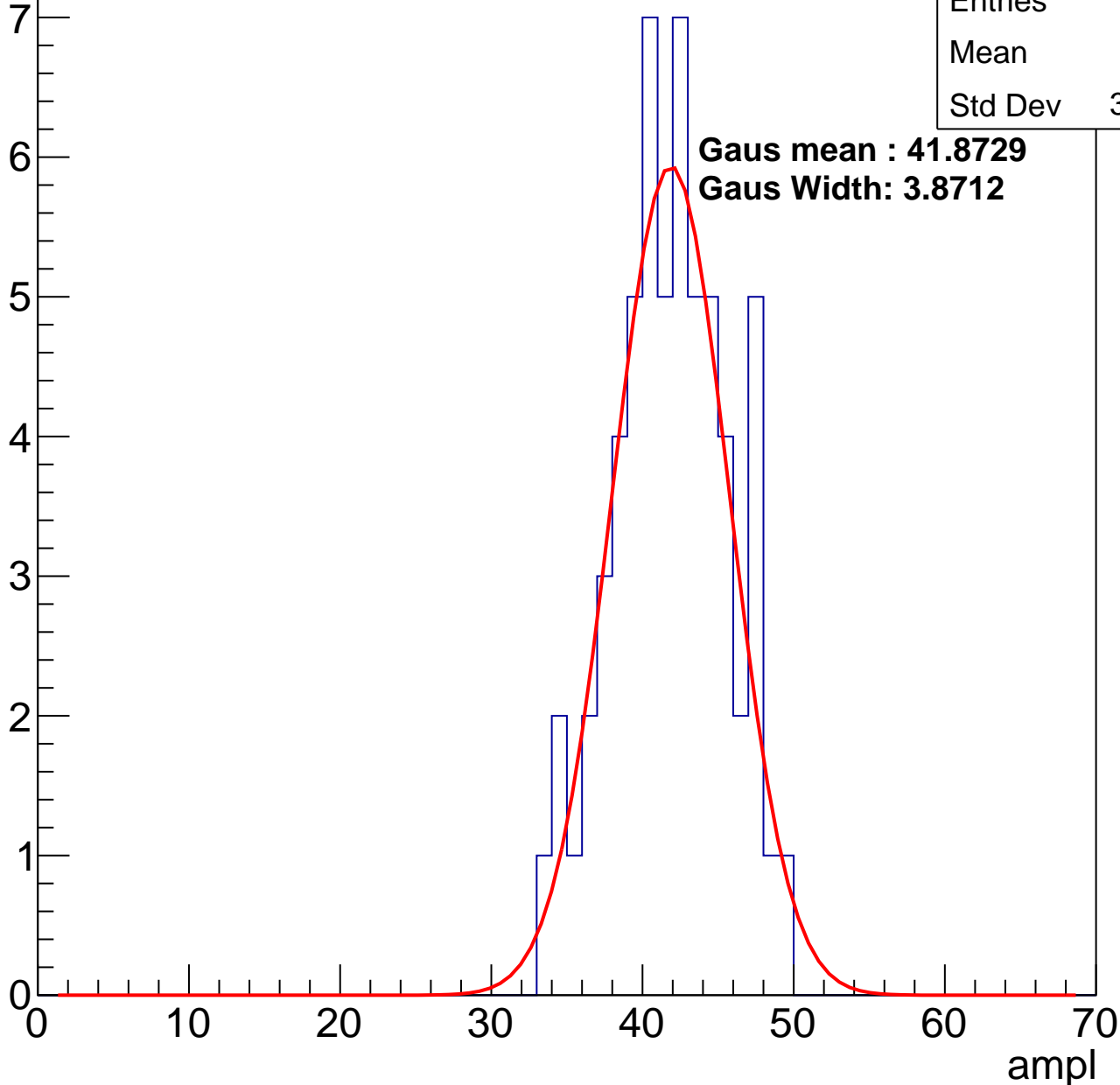


# B1L101S, U18-ch8, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	41.4
Std Dev	3.716

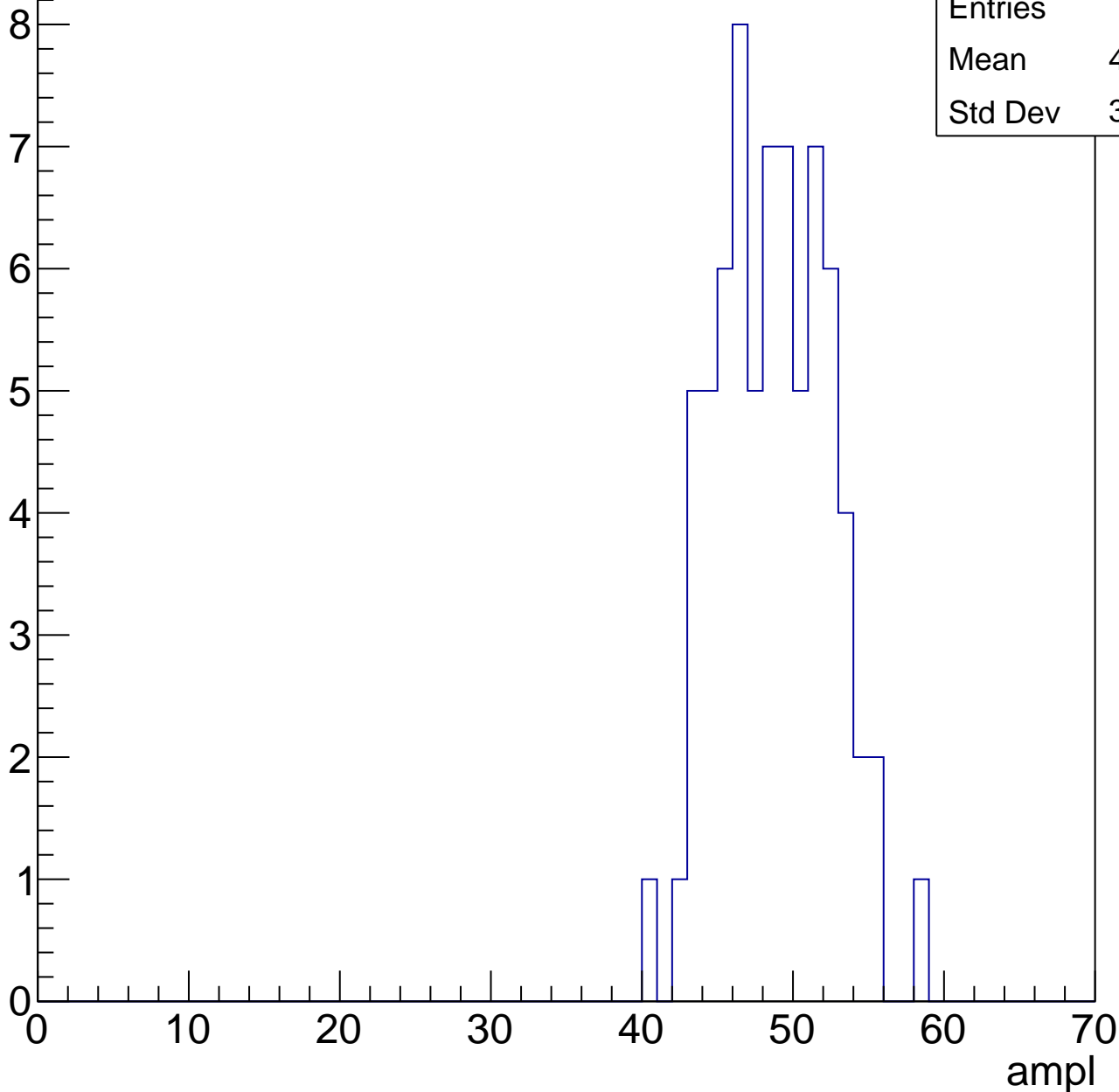


# B1L101S, U18-ch8, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

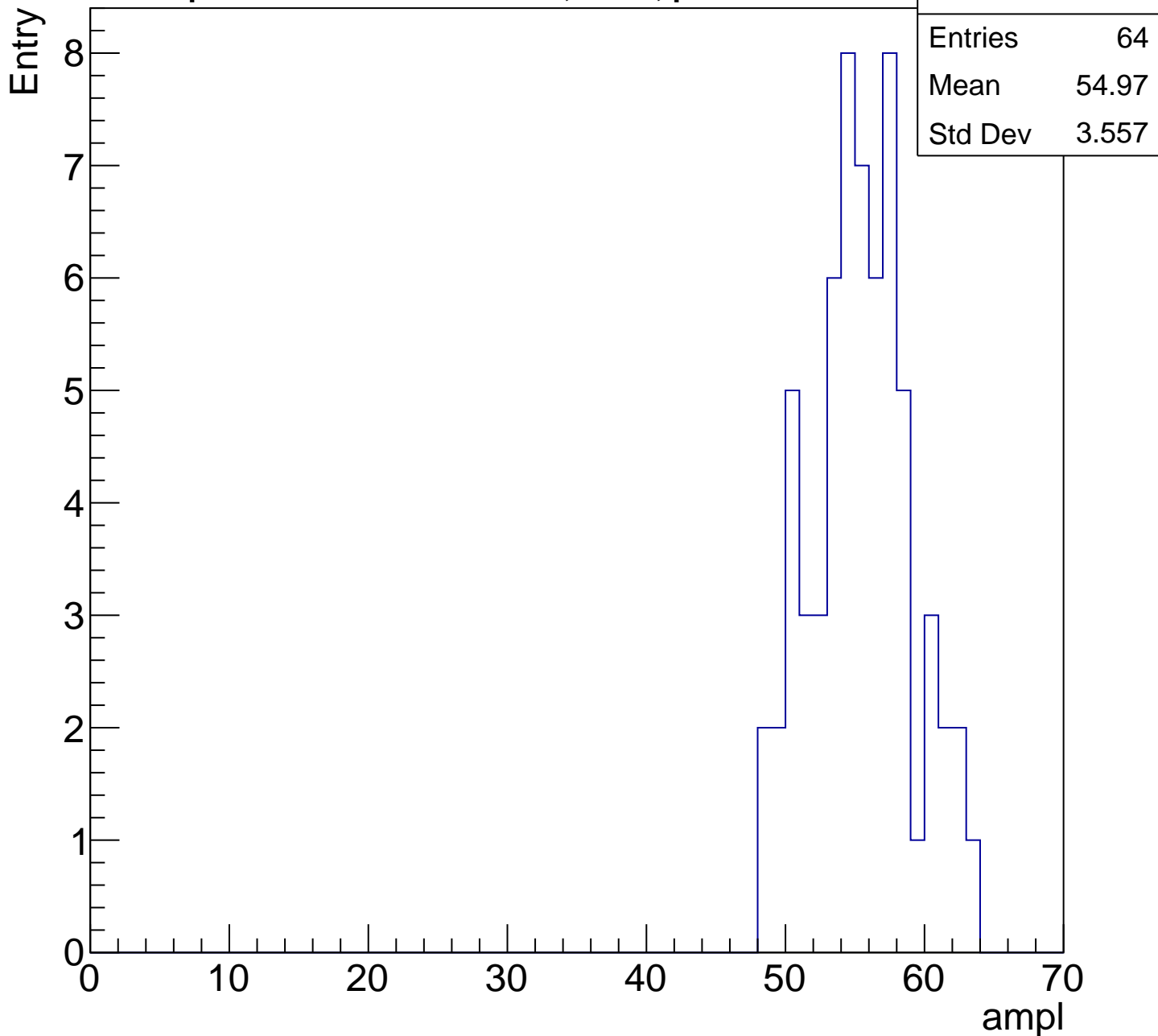
Entry

Entries	72
Mean	48.28
Std Dev	3.626



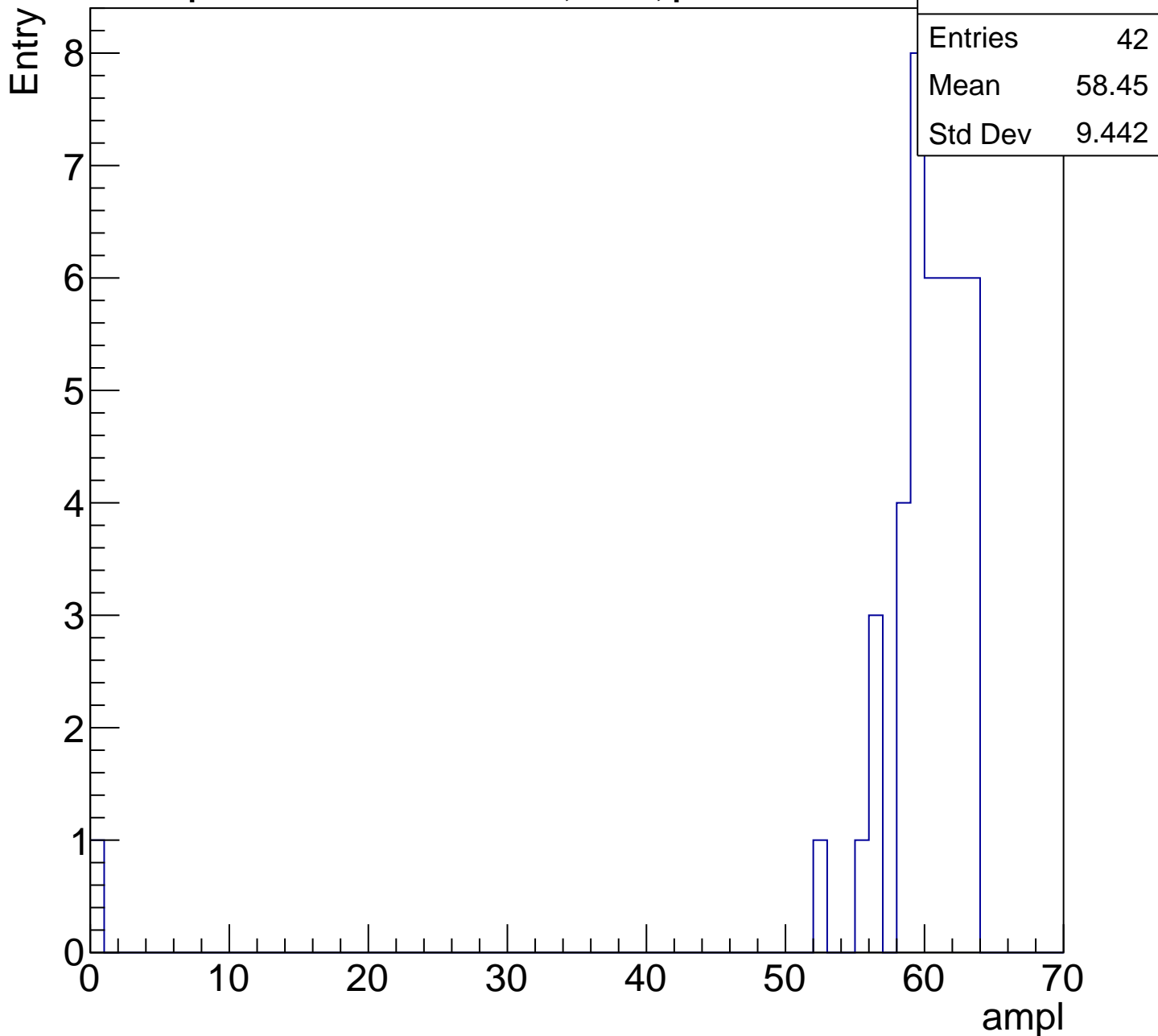
# B1L101S, U18-ch8, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U18-ch8, adc5

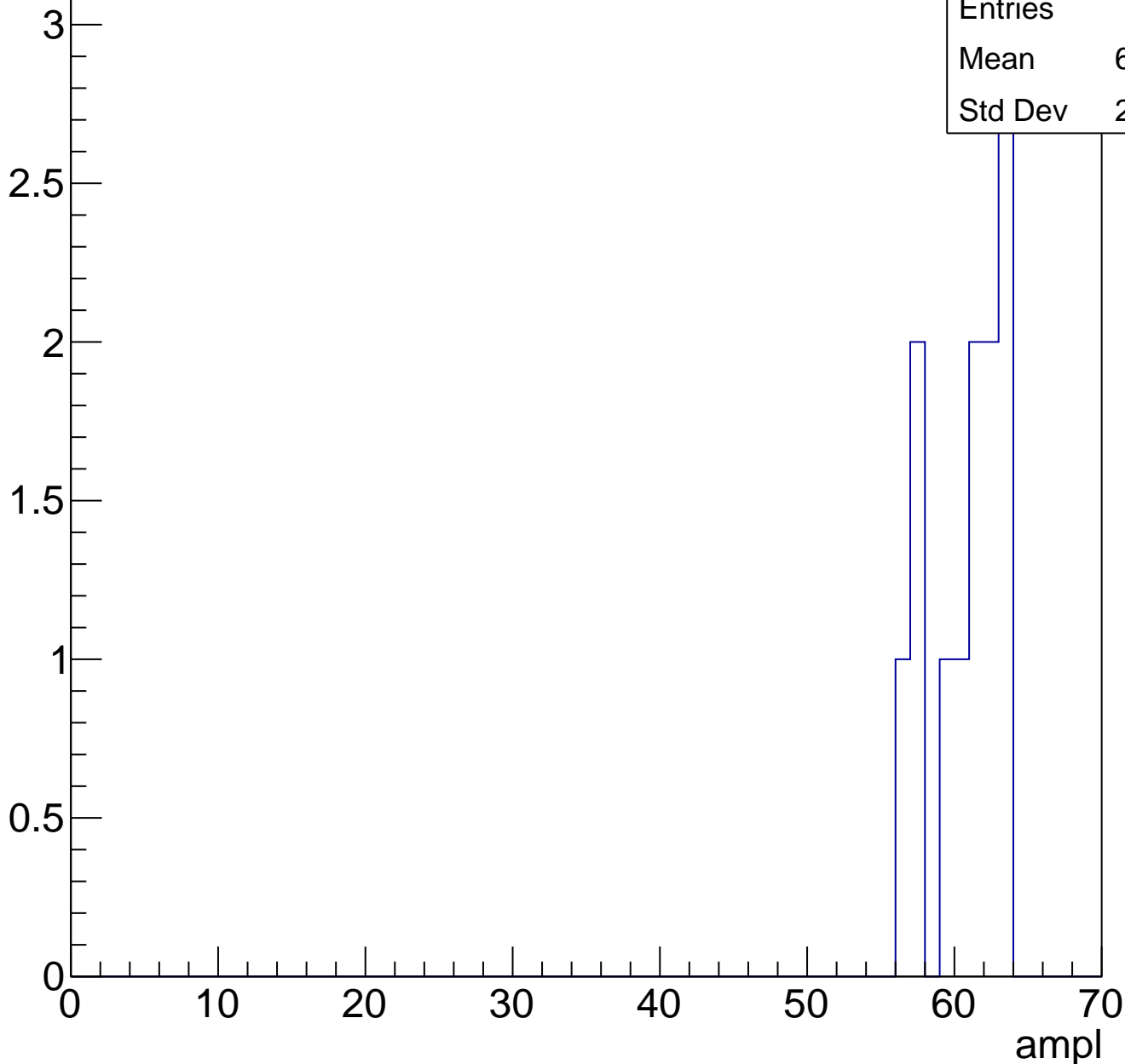
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U18-ch8, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch8, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U18-ch9, adc0

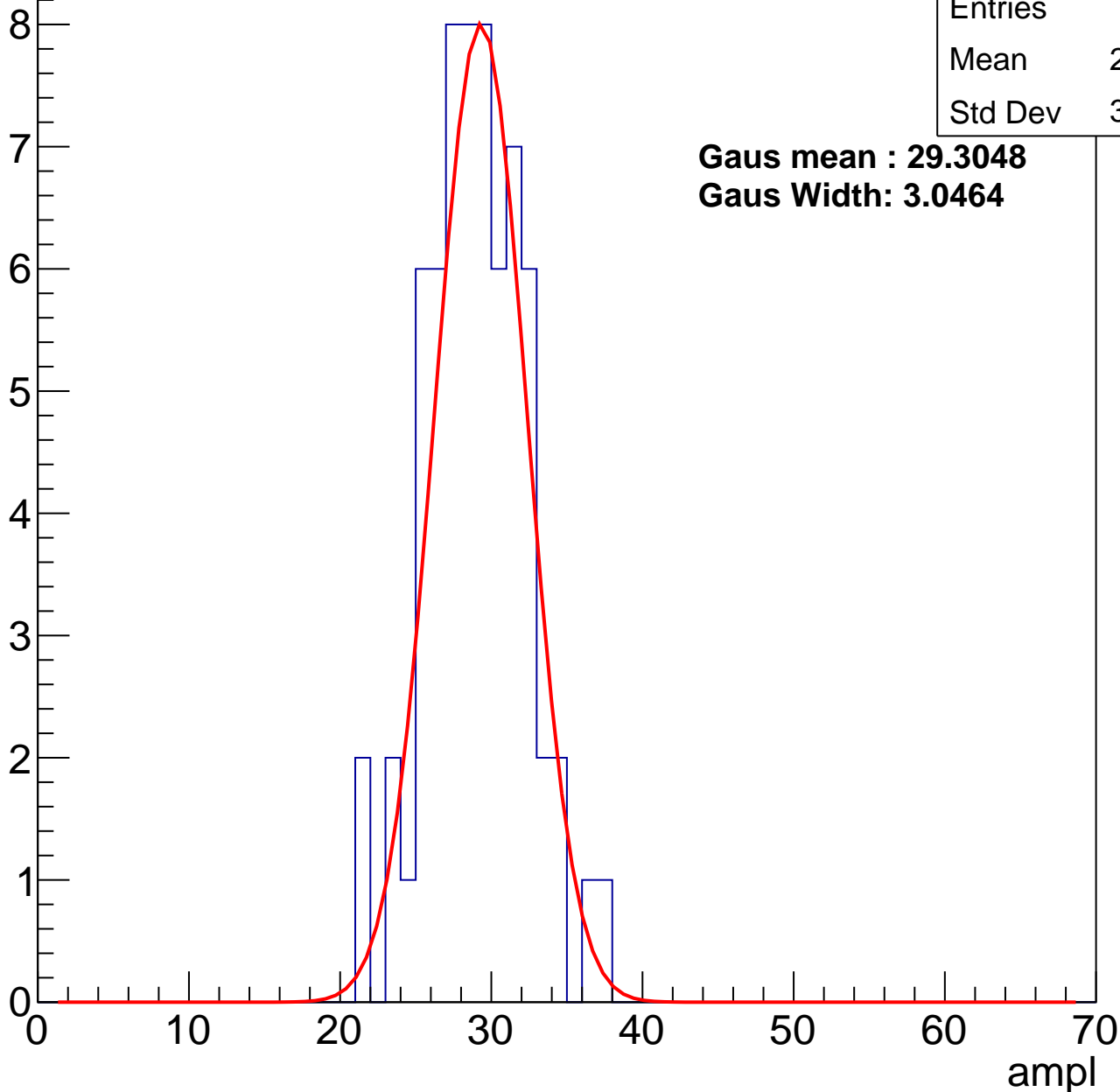
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	28.58
Std Dev	3.224

**Gaus mean : 29.3048**

**Gaus Width: 3.0464**



# B1L101S, U18-ch9, adc1

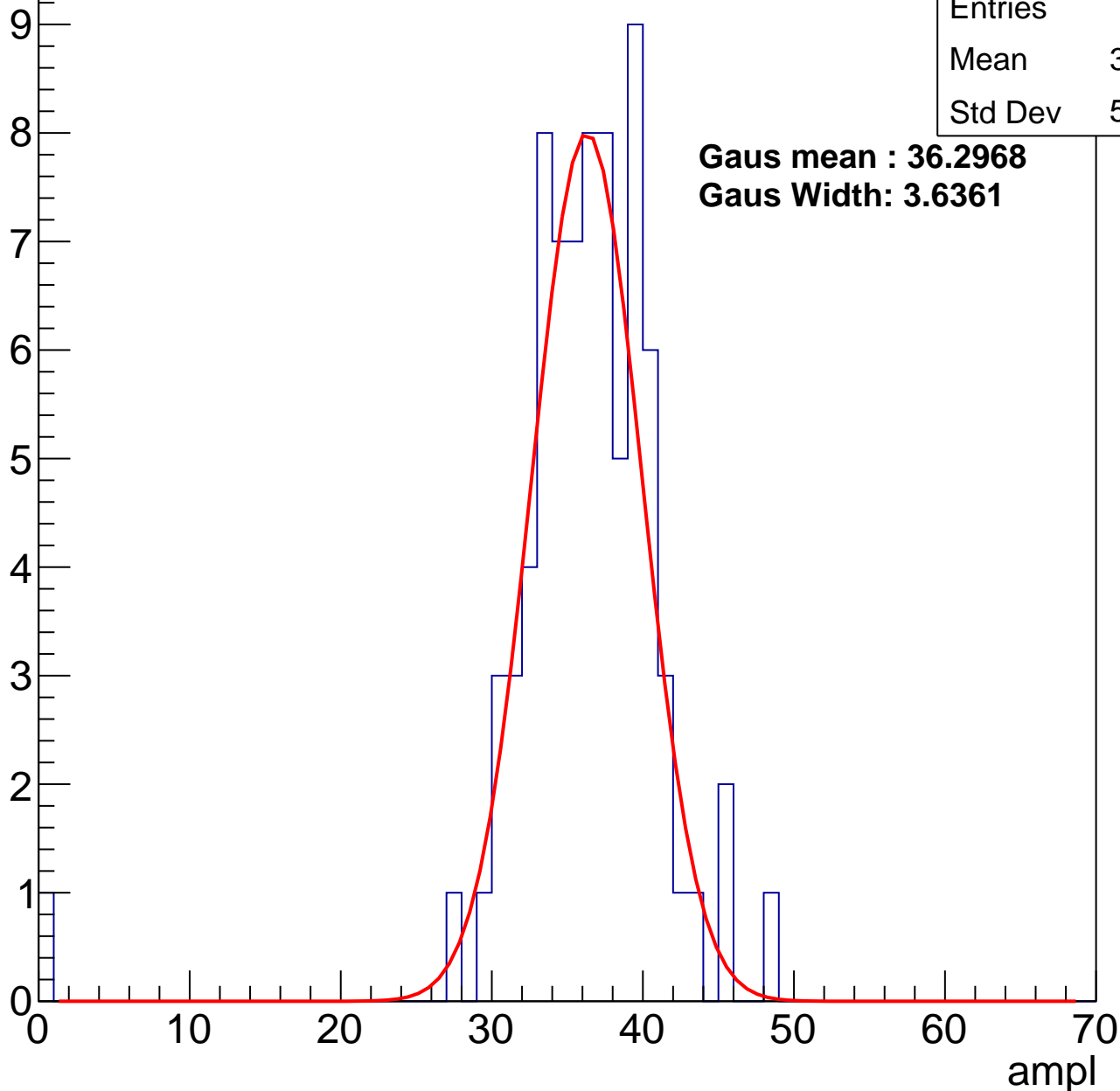
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	79
Mean	35.76
Std Dev	5.565

**Gaus mean : 36.2968**

**Gaus Width: 3.6361**



# B1L101S, U18-ch9, adc2

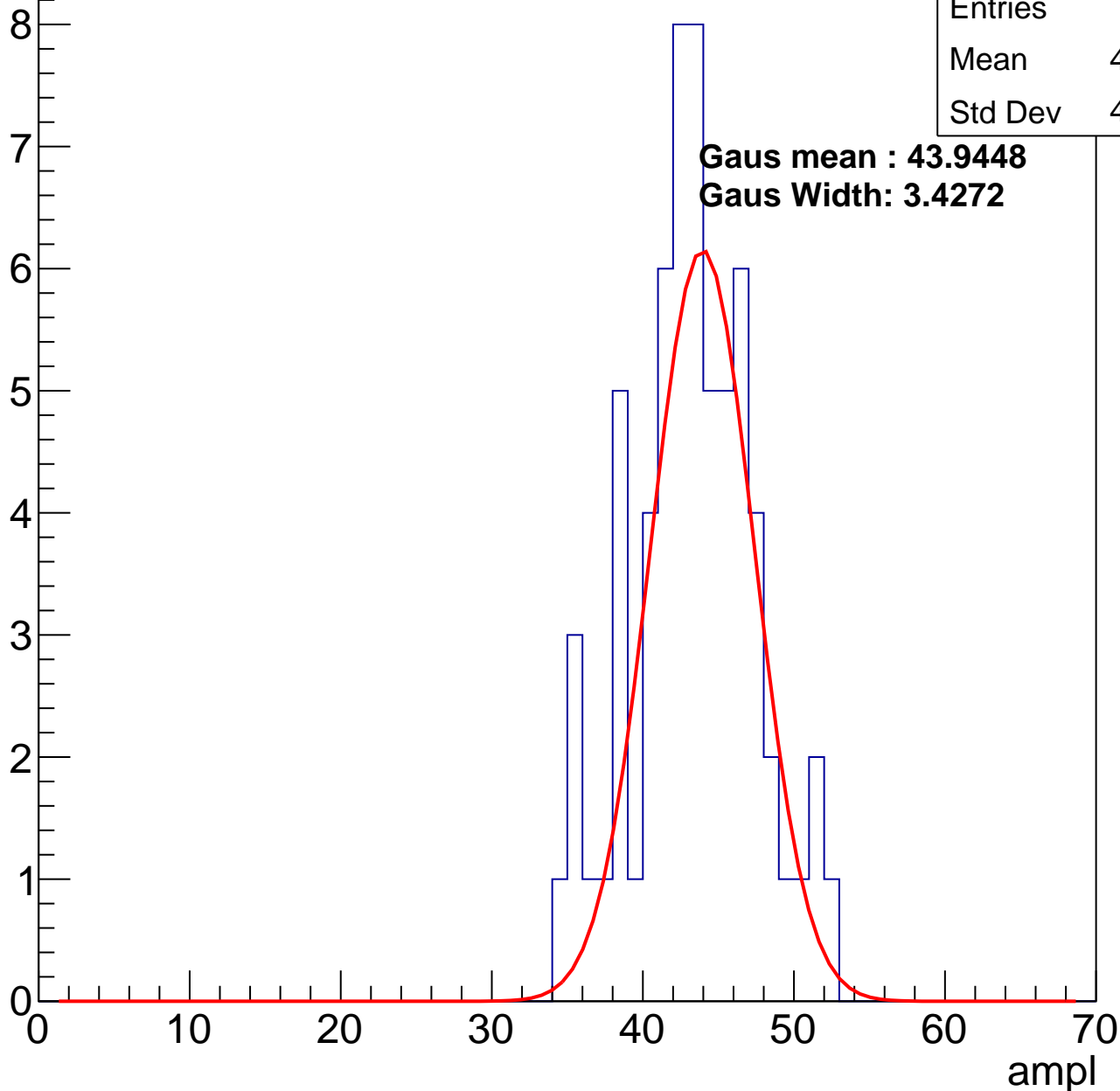
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	42.85
Std Dev	4.024

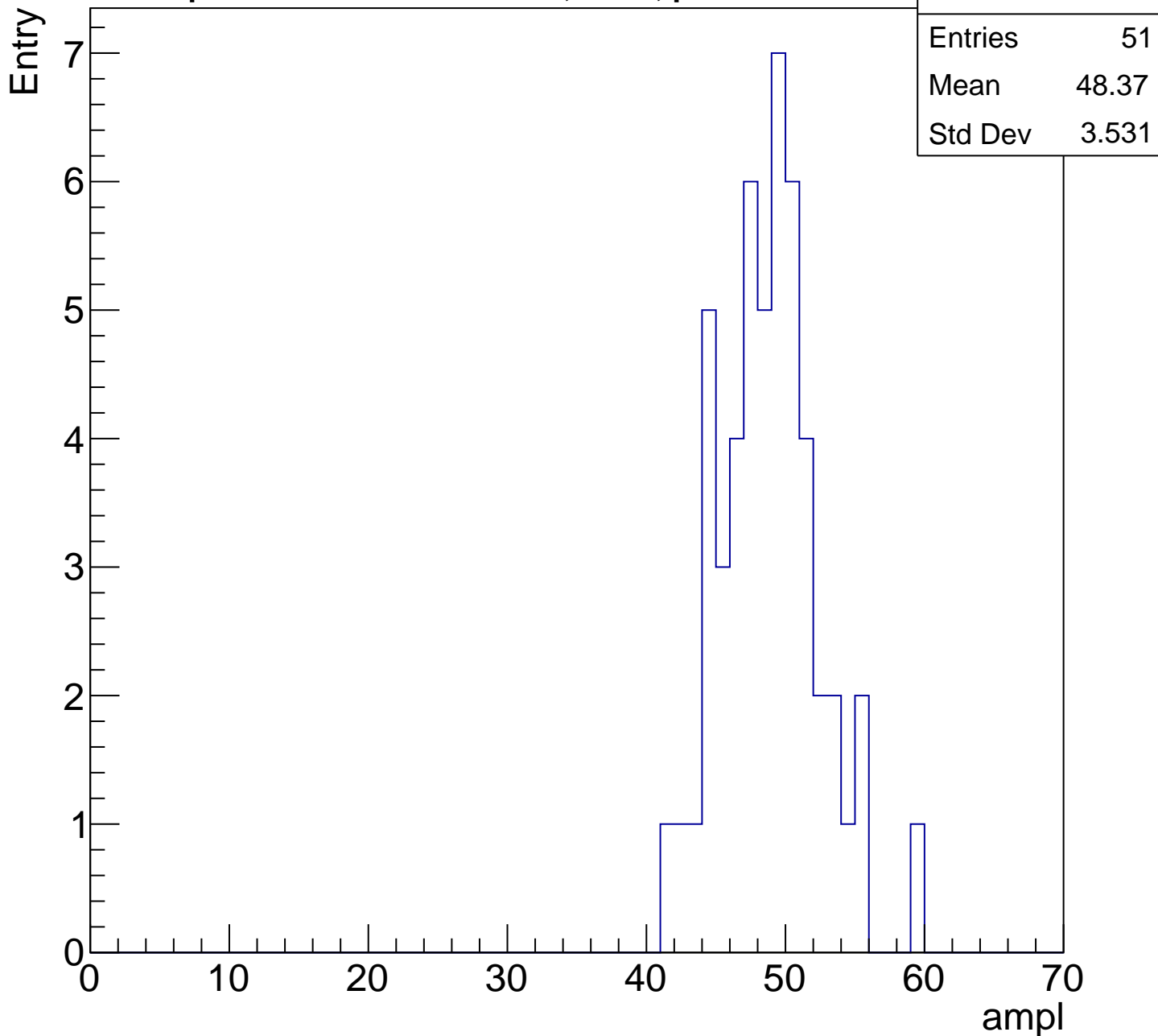
**Gaus mean : 43.9448**

**Gaus Width: 3.4272**



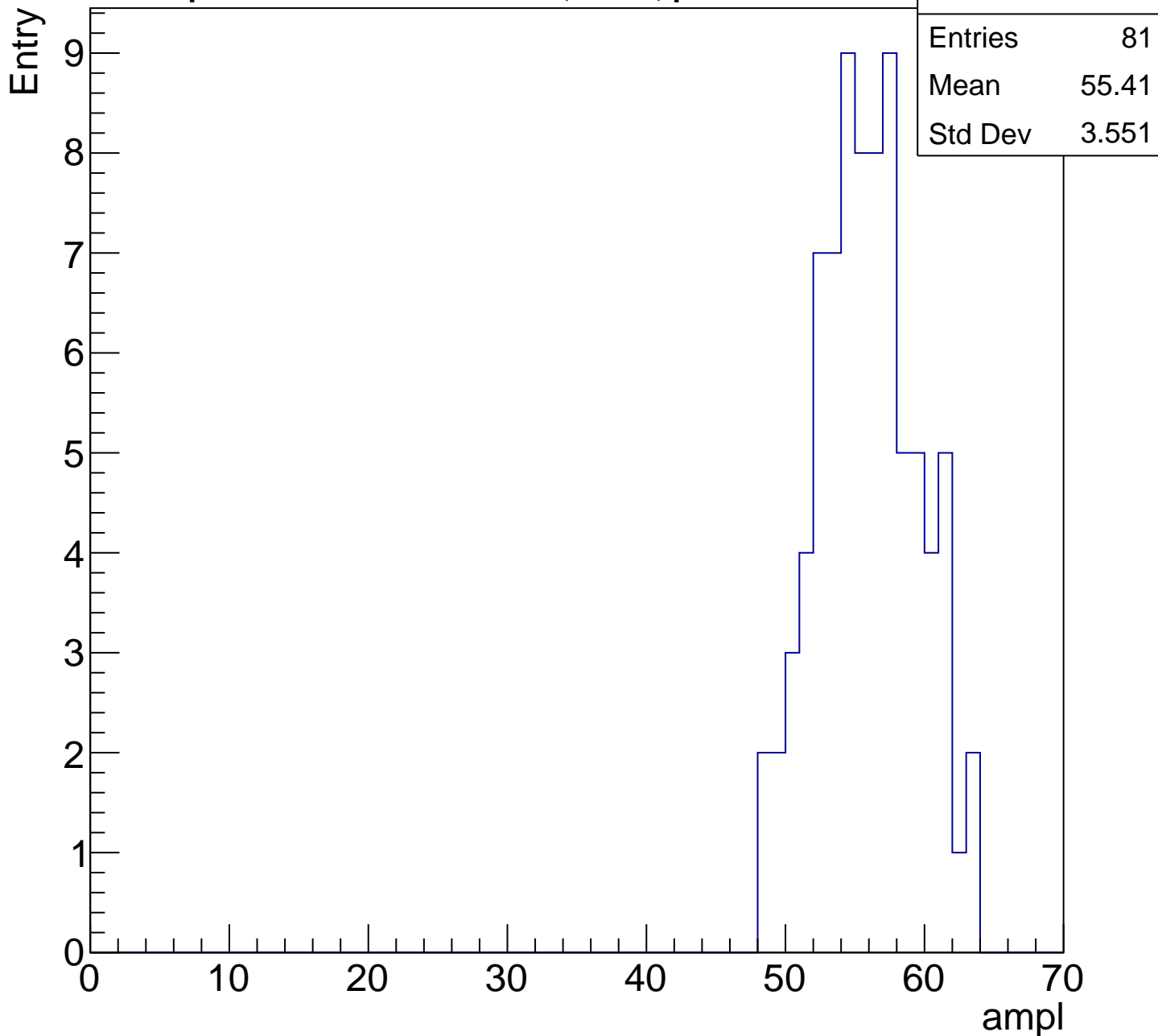
# B1L101S, U18-ch9, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U18-ch9, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

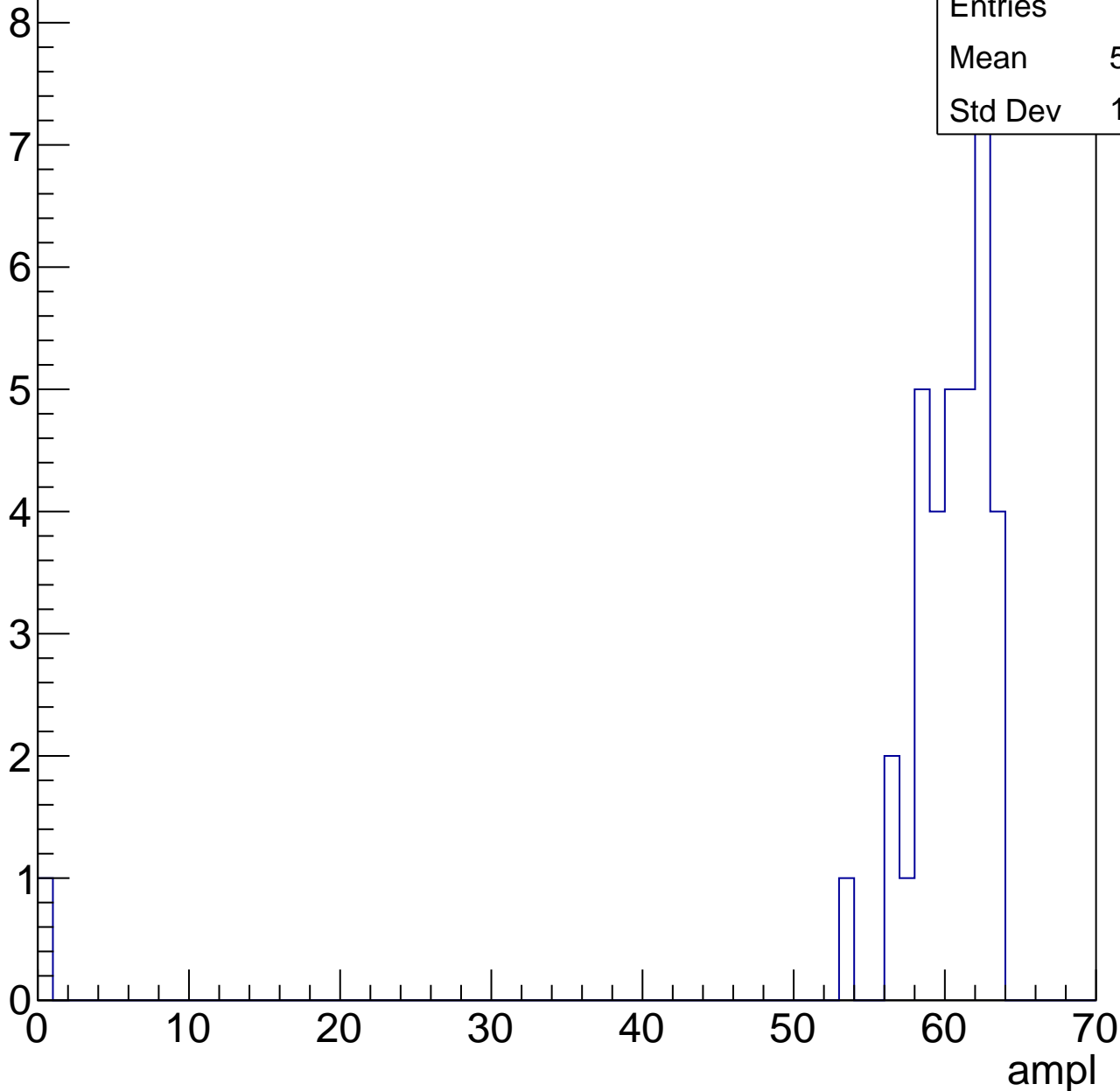


# B1L101S, U18-ch9, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

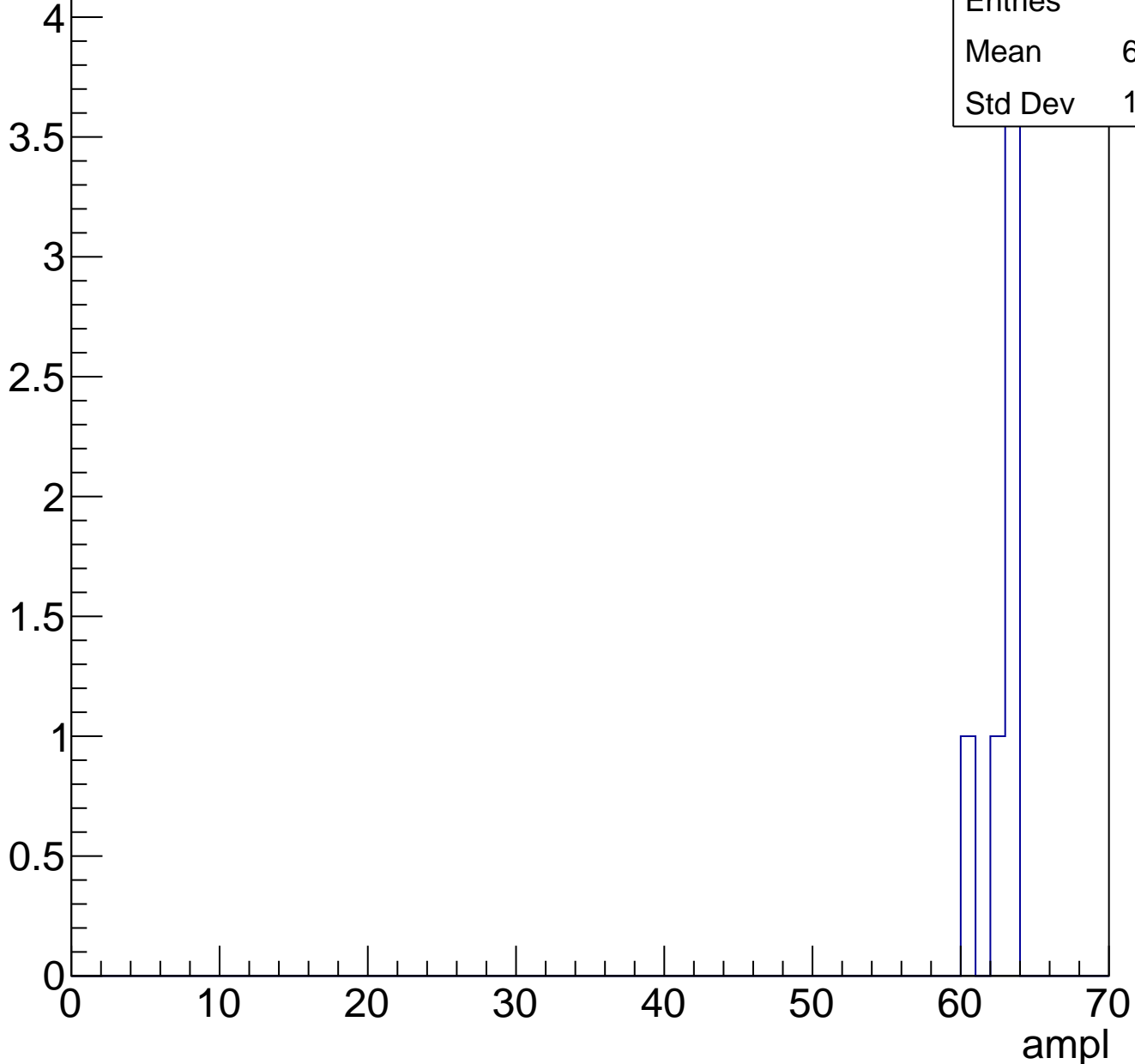
Entries	36
Mean	58.36
Std Dev	10.12



# B1L101S, U18-ch9, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch9, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U18-ch10, adc0

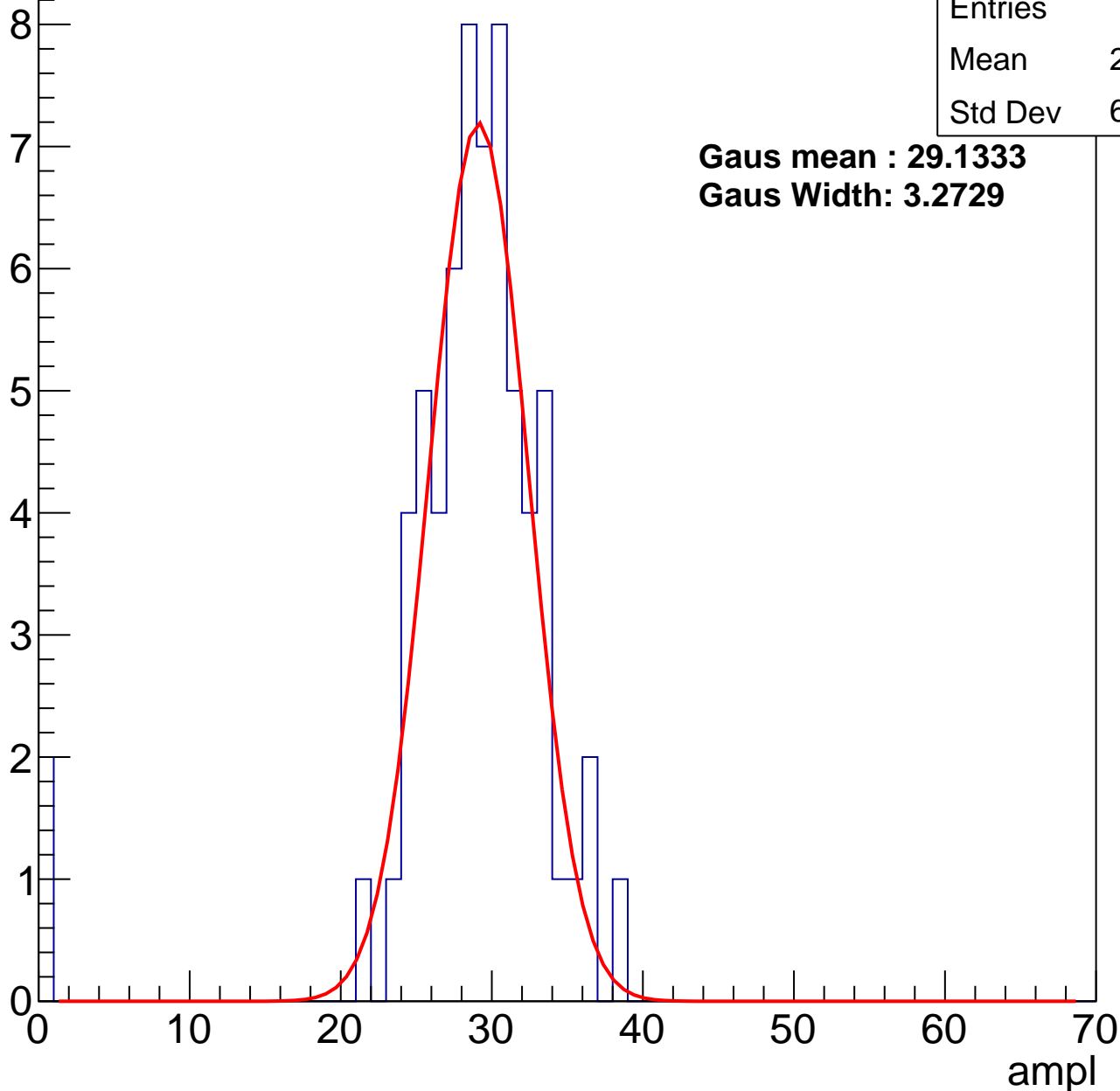
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	28.08
Std Dev	6.024

**Gaus mean : 29.1333**

**Gaus Width: 3.2729**



# B1L101S, U18-ch10, adc1

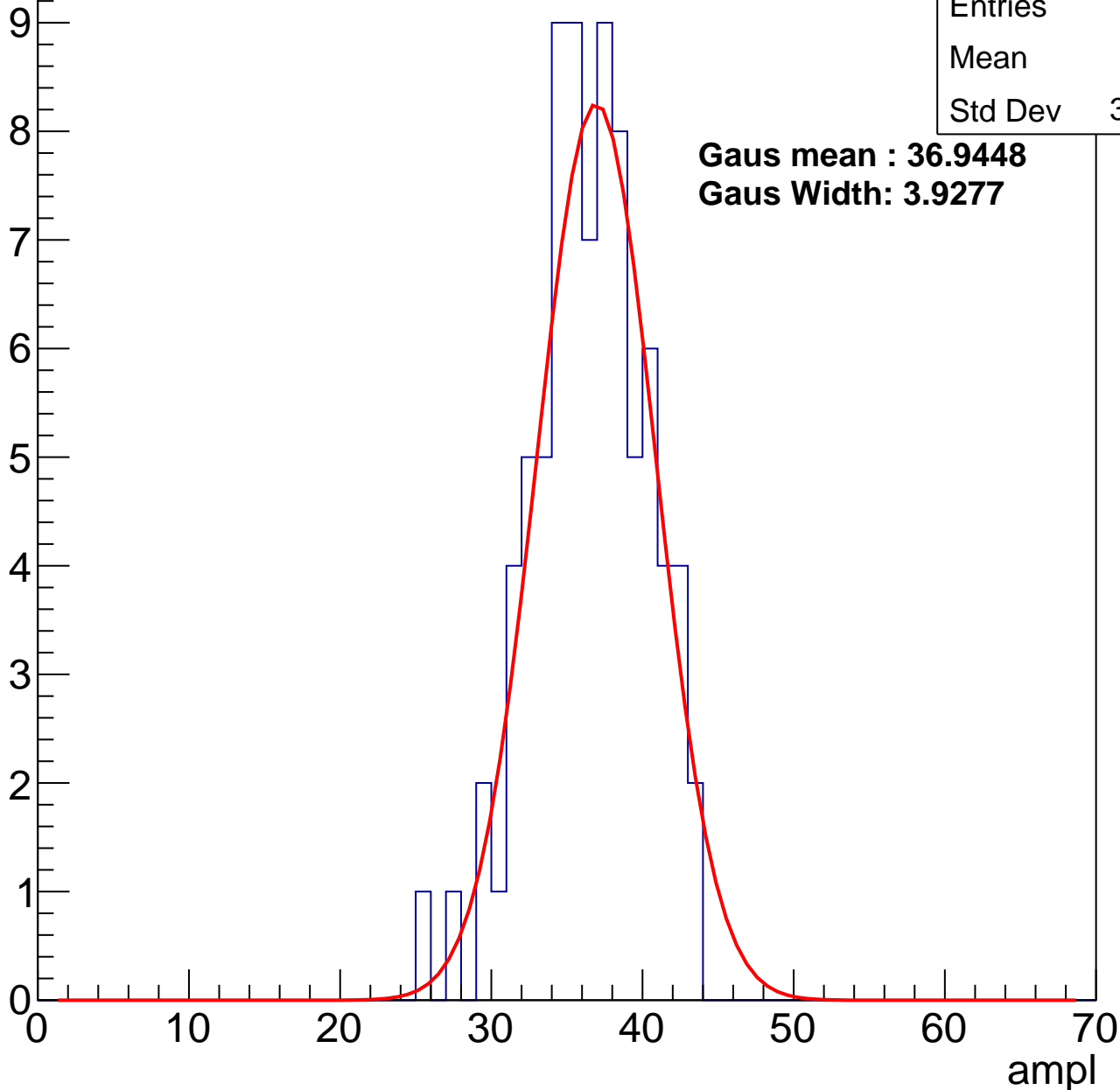
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	82
Mean	36
Std Dev	3.712

**Gaus mean : 36.9448**

**Gaus Width: 3.9277**



# B1L101S, U18-ch10, adc2

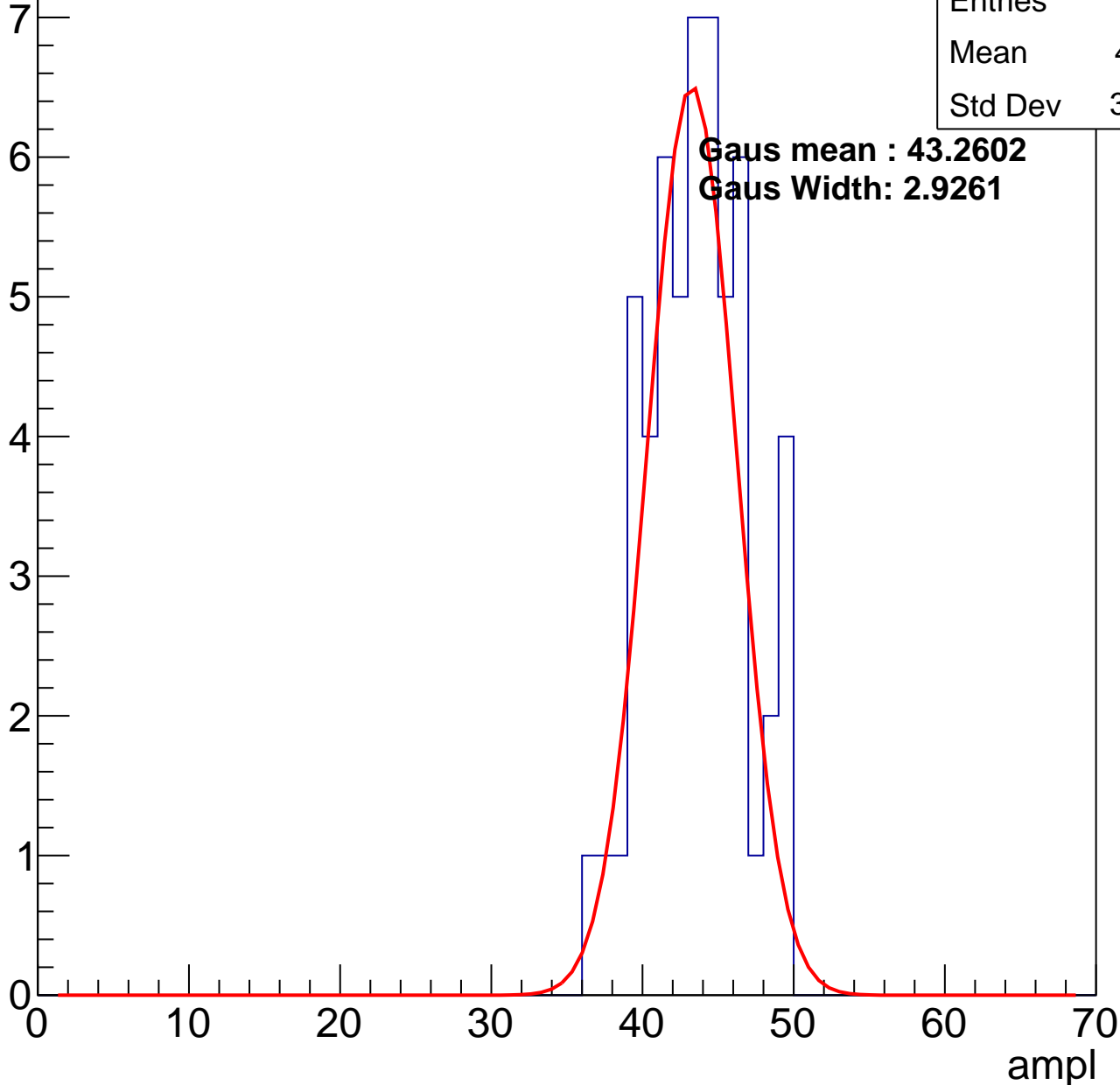
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	43.11
Std Dev	3.149

**Gaus mean : 43.2602**

**Gaus Width: 2.9261**

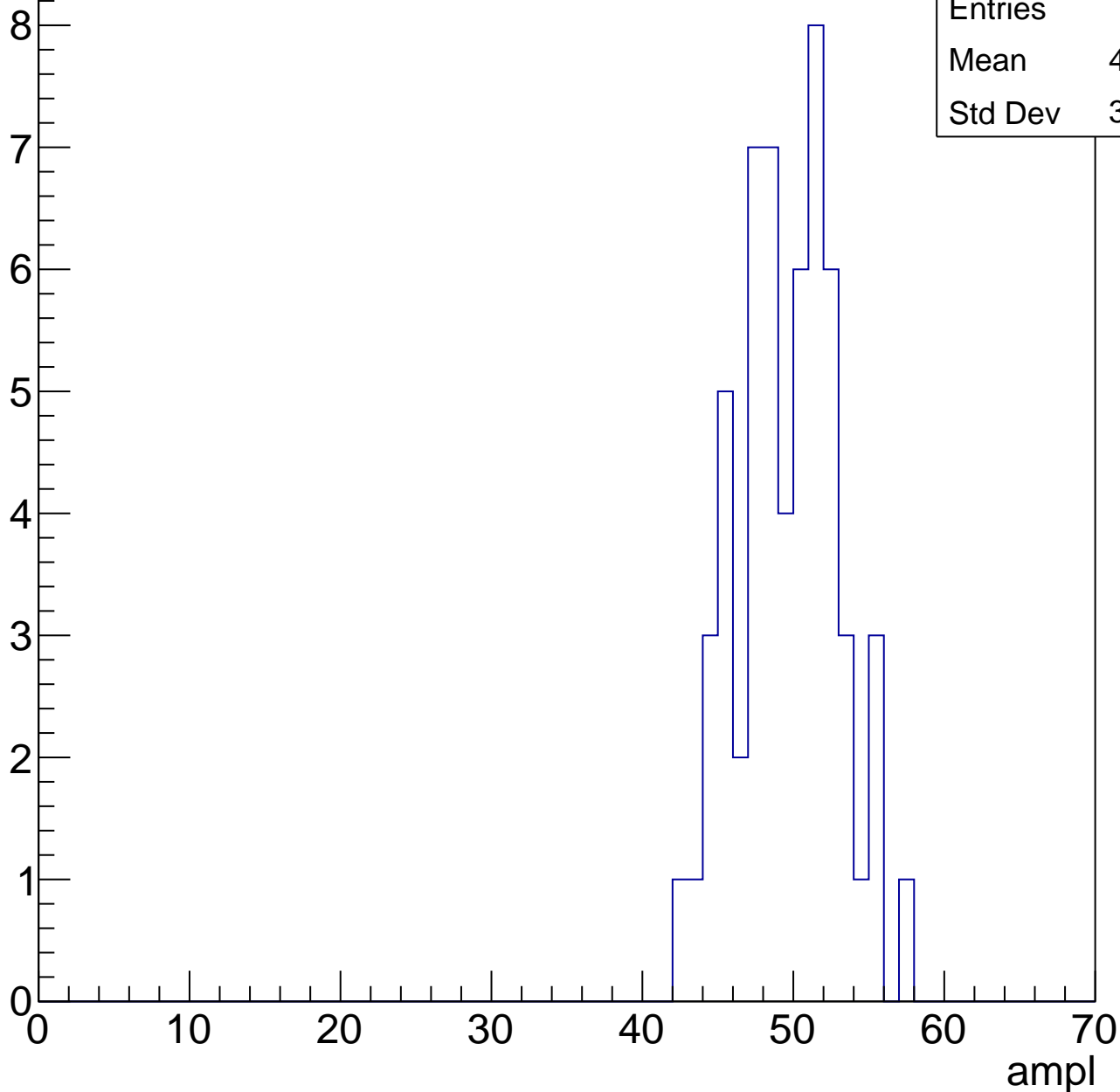


# B1L101S, U18-ch10, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

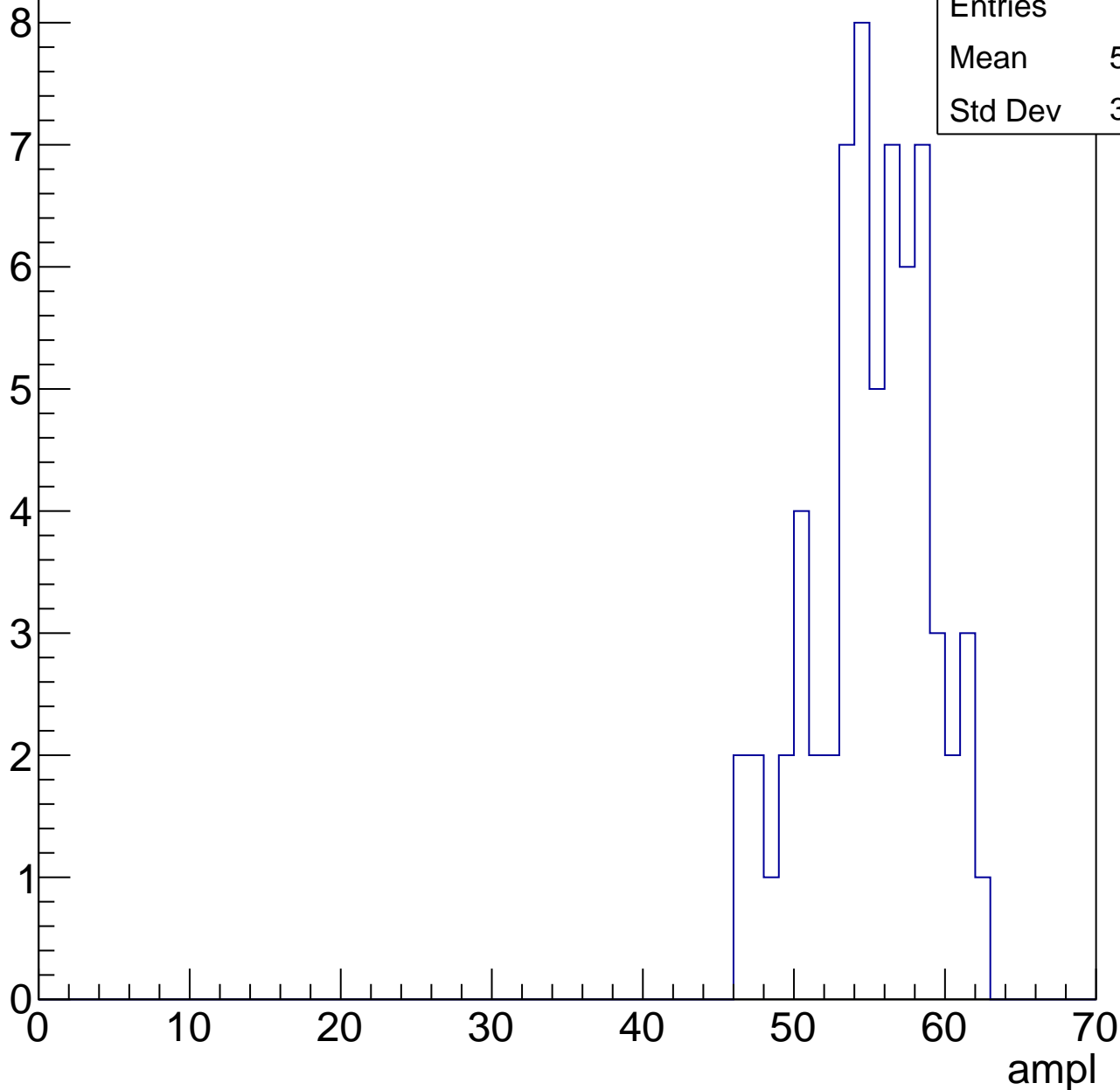
Entries	58
Mean	49.14
Std Dev	3.293



# B1L101S, U18-ch10, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	64
Mean	54.66
Std Dev	3.829

# B1L101S, U18-ch10, adc5

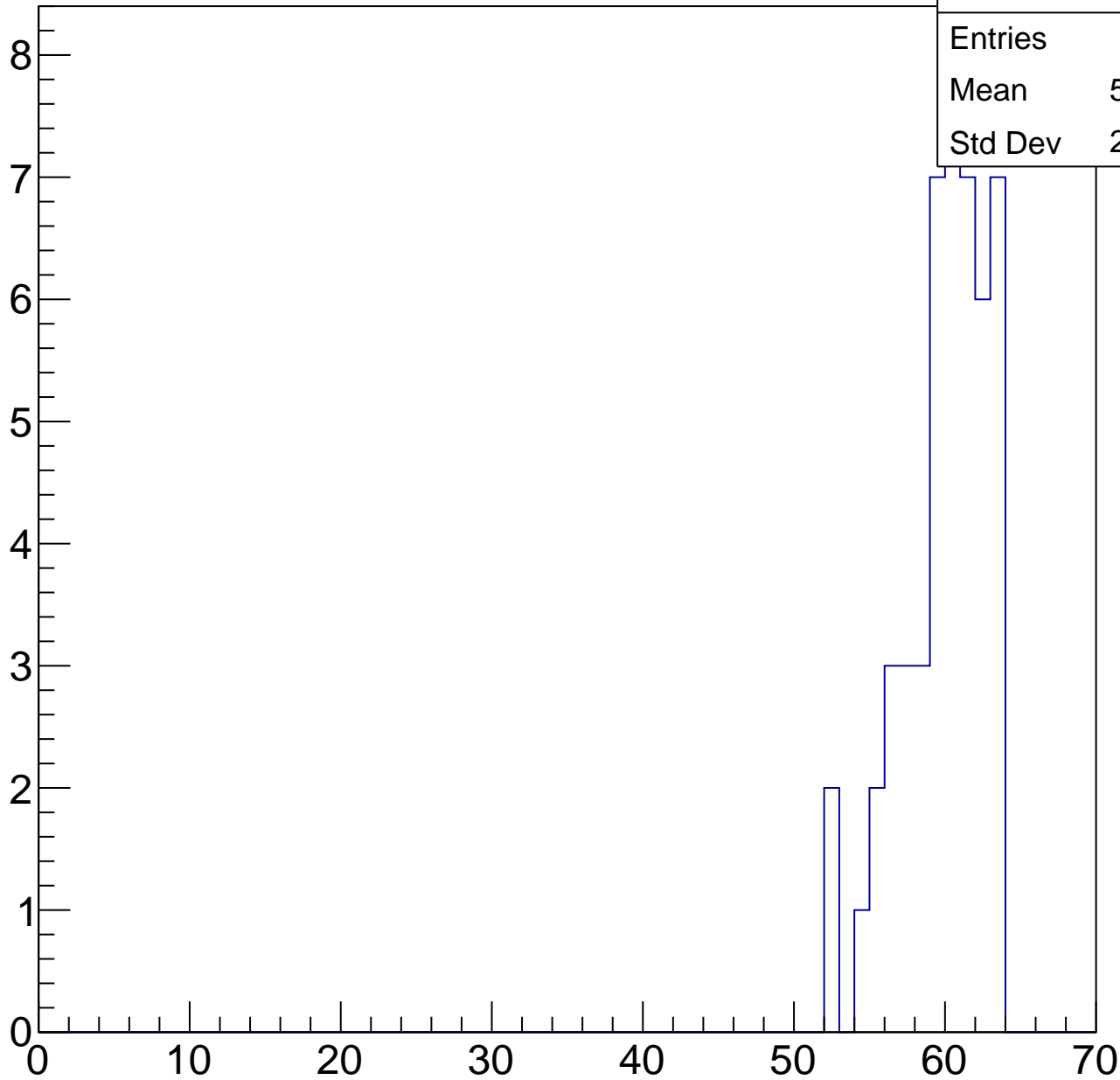
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	49
Mean	59.47
Std Dev	2.815

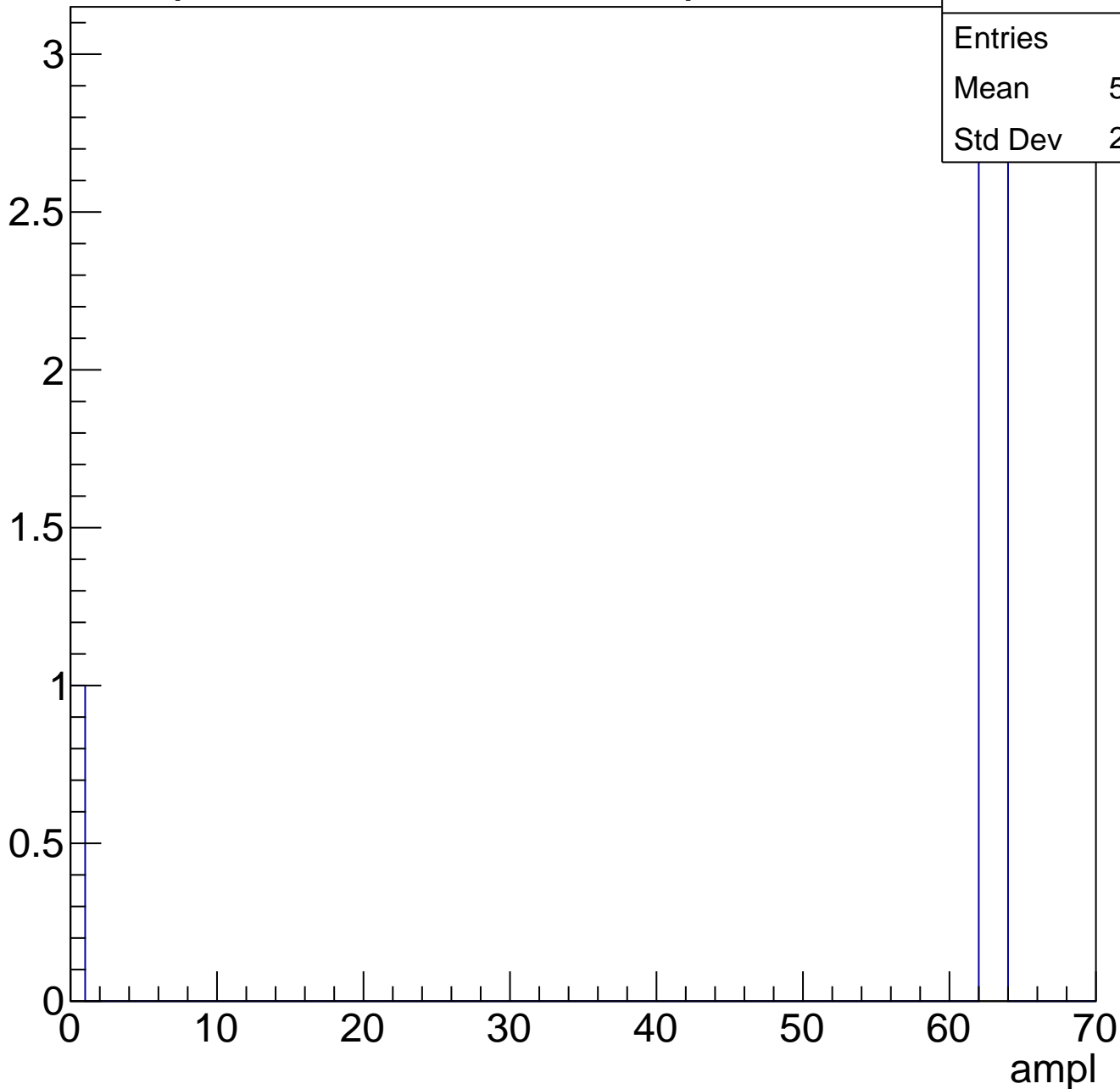
ampl



# B1L101S, U18-ch10, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch10, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U18-ch11, adc0

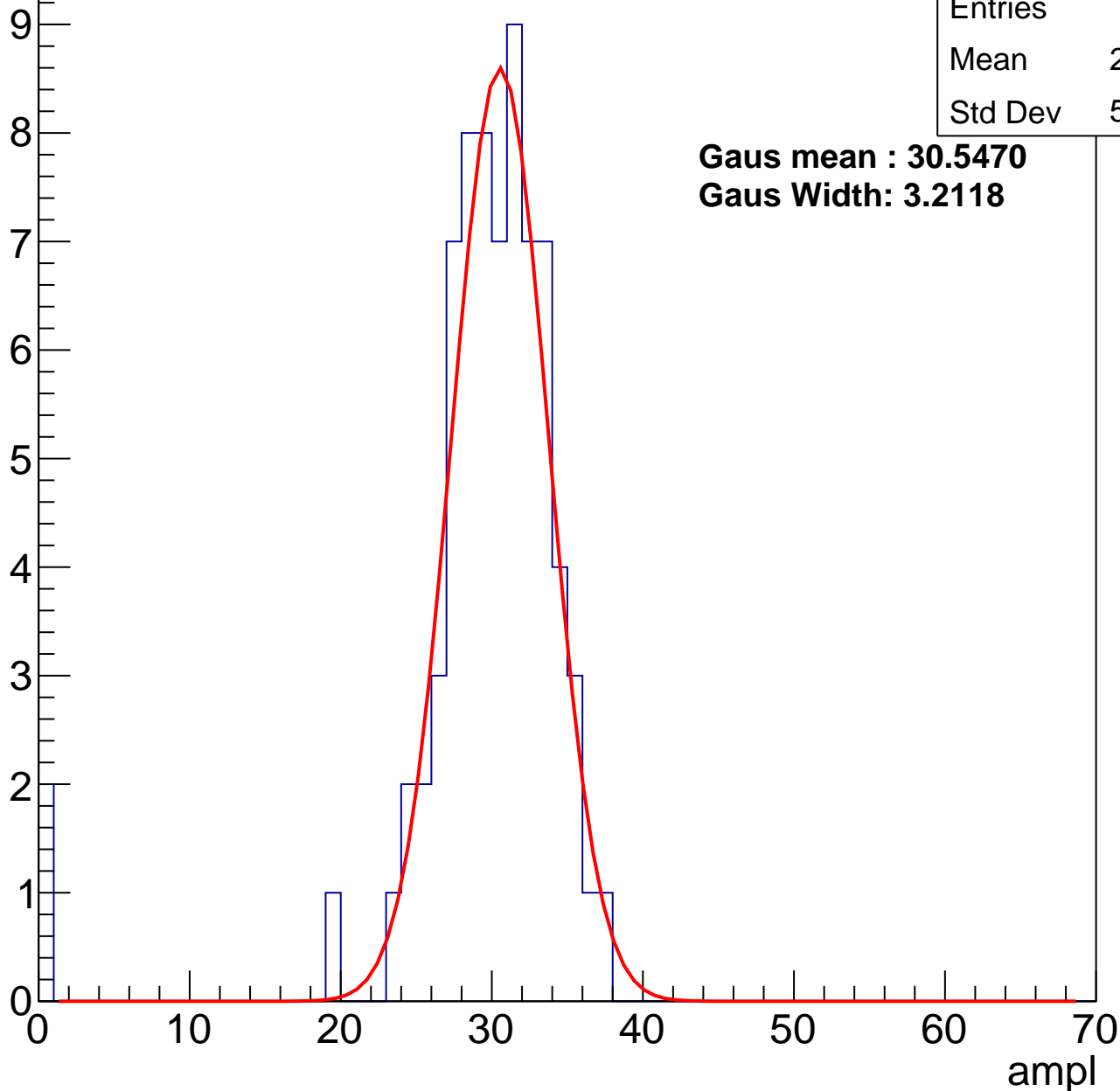
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	29.05
Std Dev	5.854

**Gaus mean : 30.5470**

**Gaus Width: 3.2118**



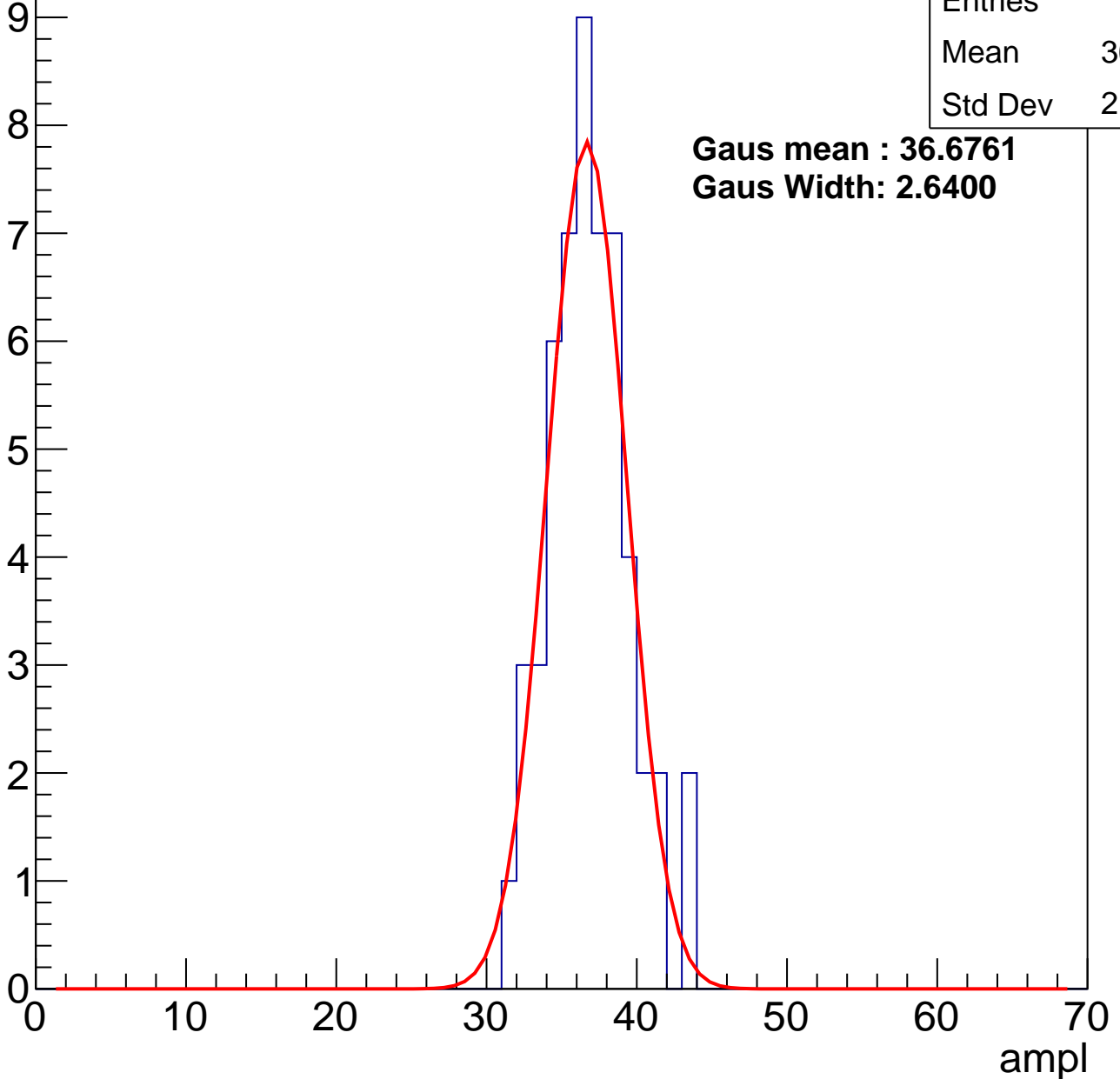
# B1L101S, U18-ch11, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	36.38
Std Dev	2.658

**Gaus mean : 36.6761**  
**Gaus Width: 2.6400**



# B1L101S, U18-ch11, adc2

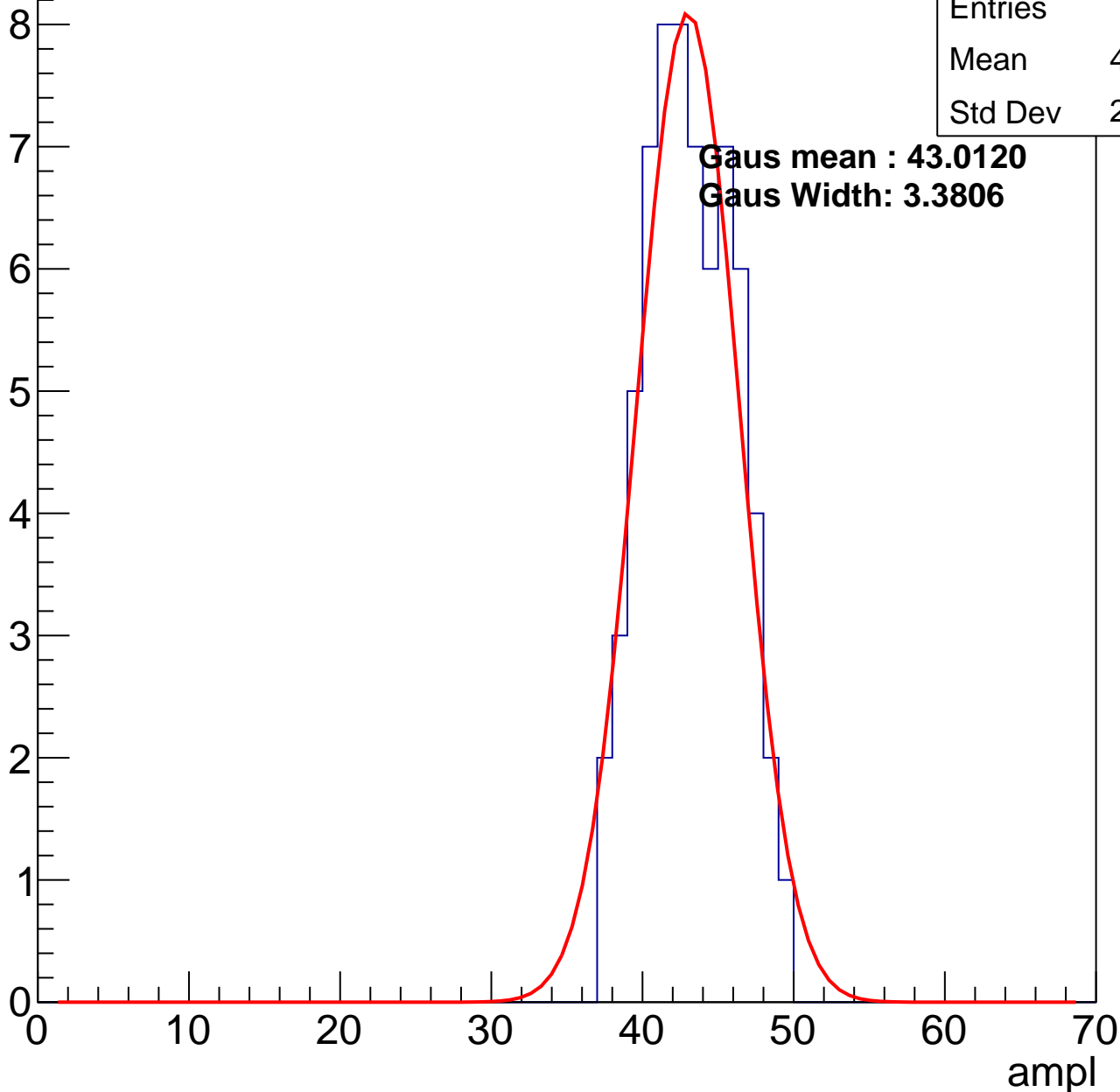
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	42.67
Std Dev	2.915

**Gaus mean : 43.0120**

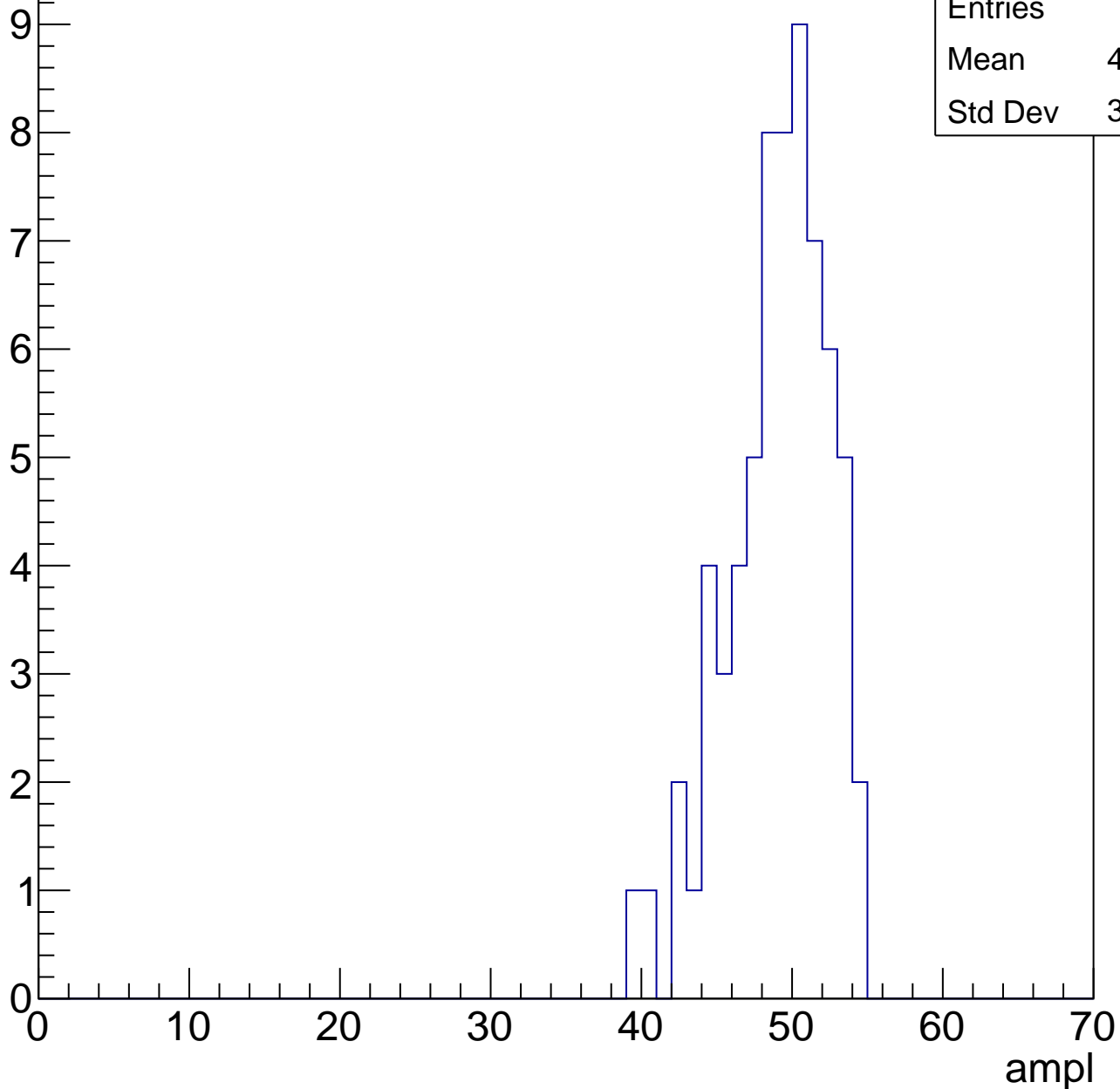
**Gaus Width: 3.3806**



# B1L101S, U18-ch11, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

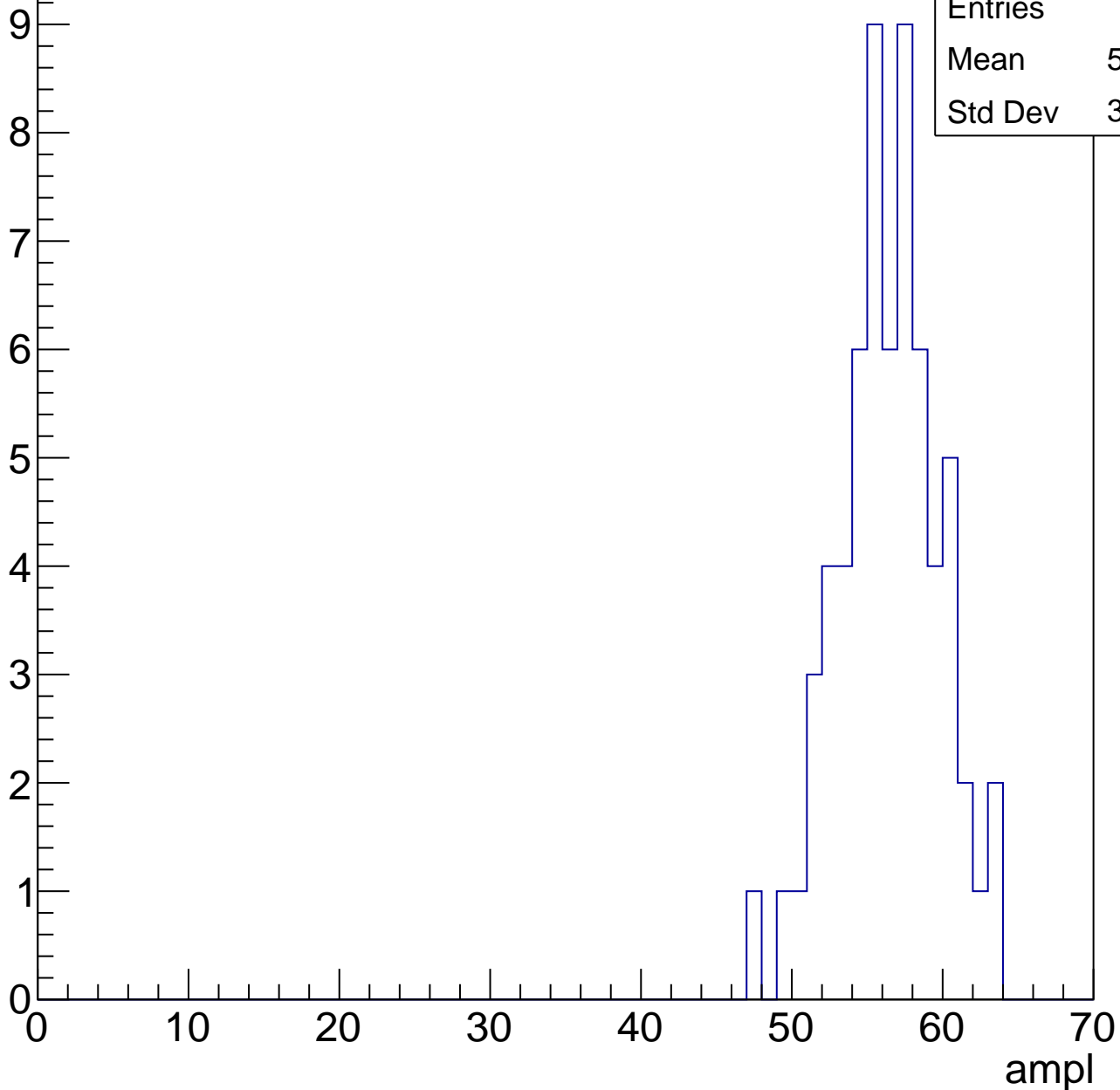


# B1L101S, U18-ch11, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	55.95
Std Dev	3.323

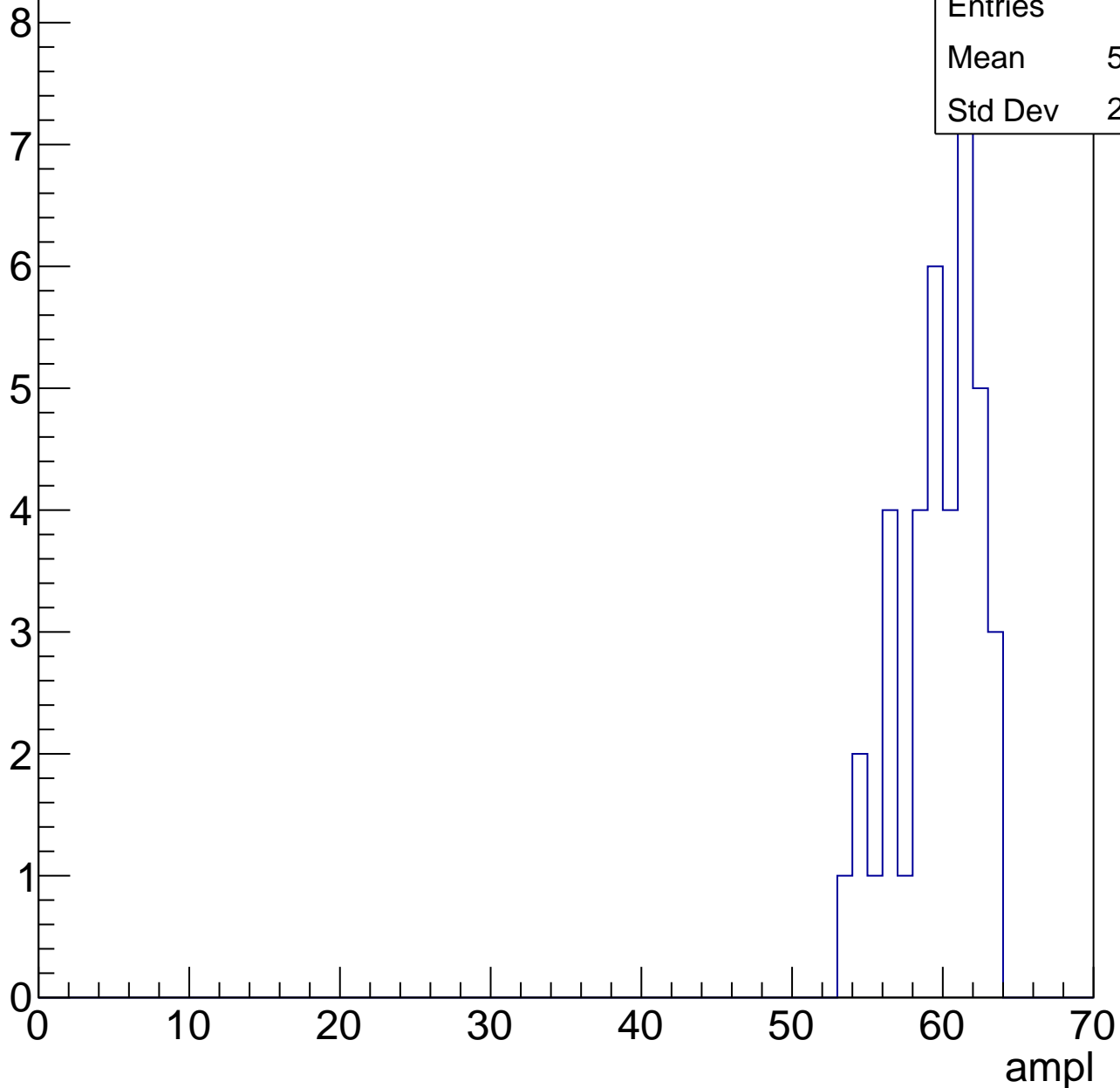


# B1L101S, U18-ch11, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	39
Mean	59.23
Std Dev	2.645

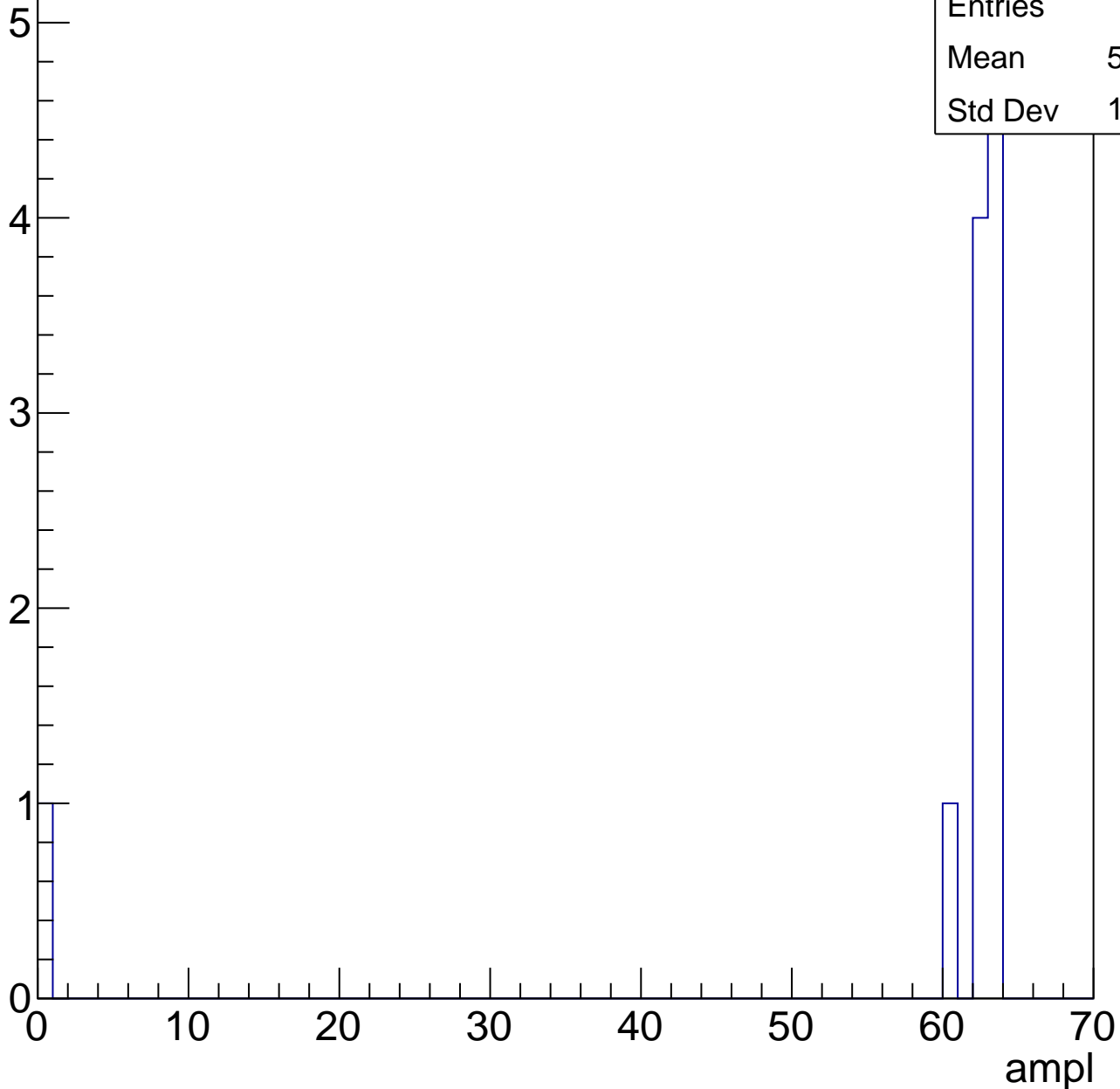


# B1L101S, U18-ch11, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	11
Mean	56.64
Std Dev	17.93





# B1L101S, U18-ch11, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U18-ch12, adc0

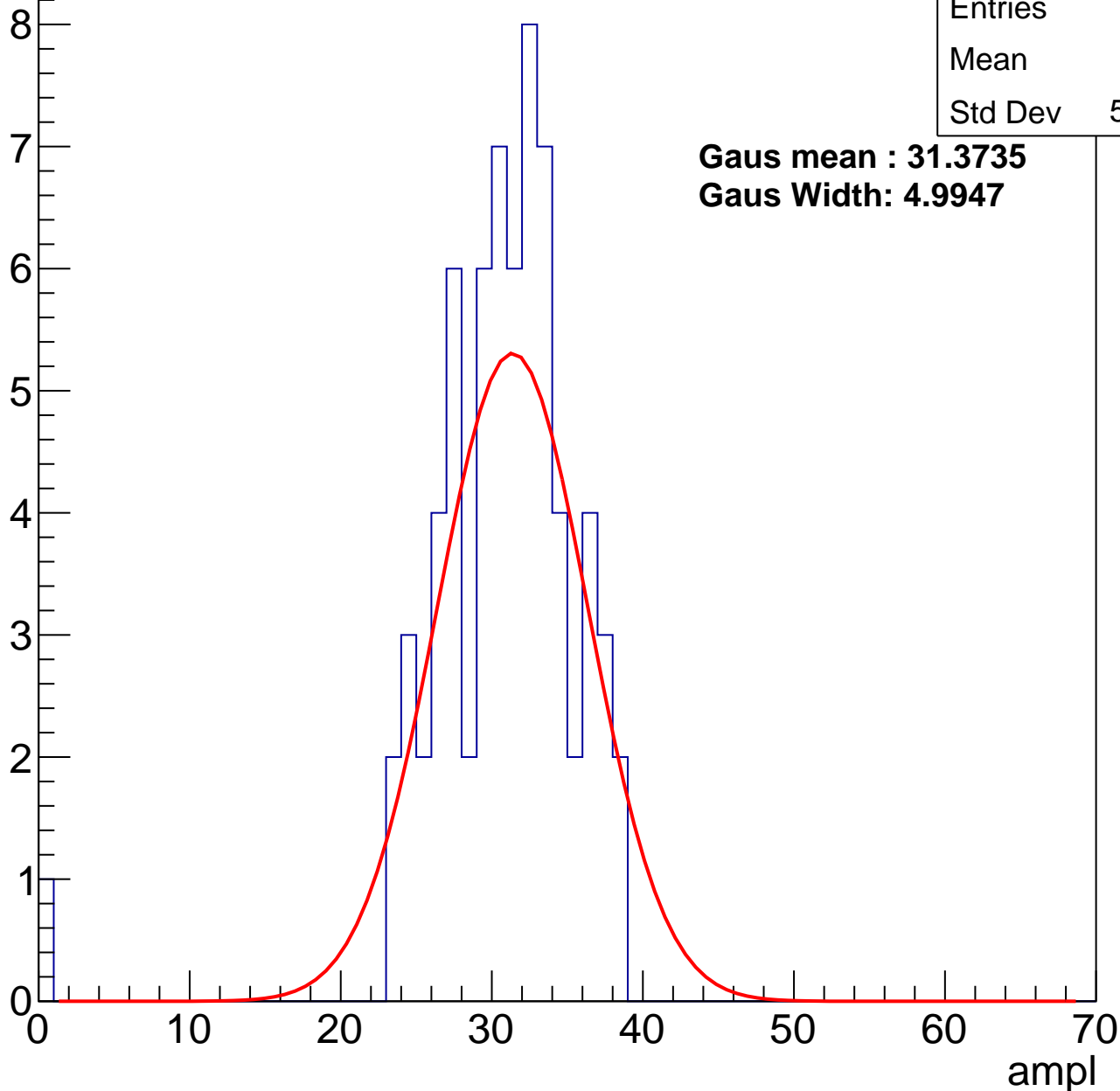
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	30.2
Std Dev	5.274

**Gaus mean : 31.3735**

**Gaus Width: 4.9947**



# B1L101S, U18-ch12, adc1

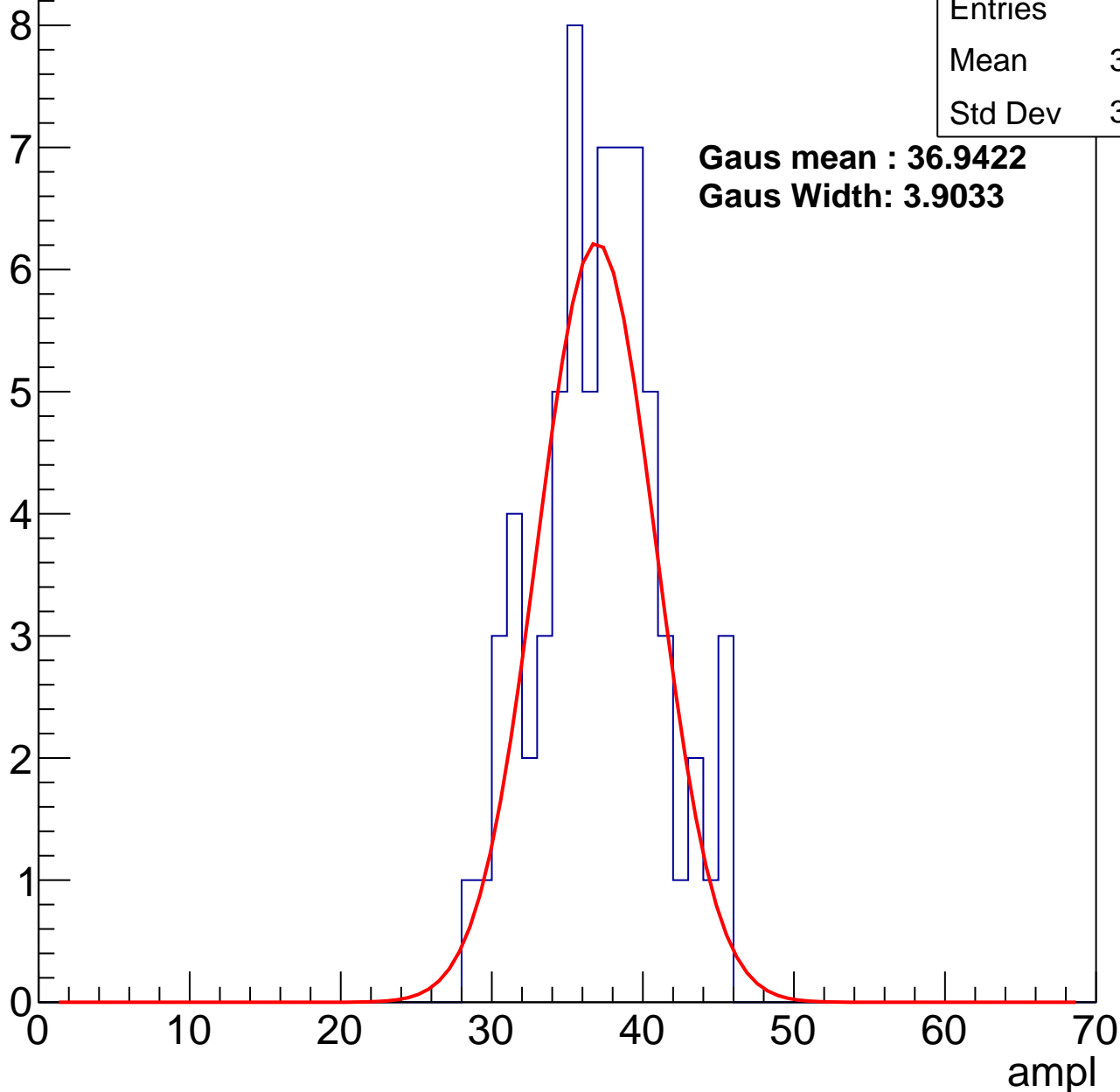
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	36.65
Std Dev	3.973

**Gaus mean : 36.9422**

**Gaus Width: 3.9033**



# B1L101S, U18-ch12, adc2

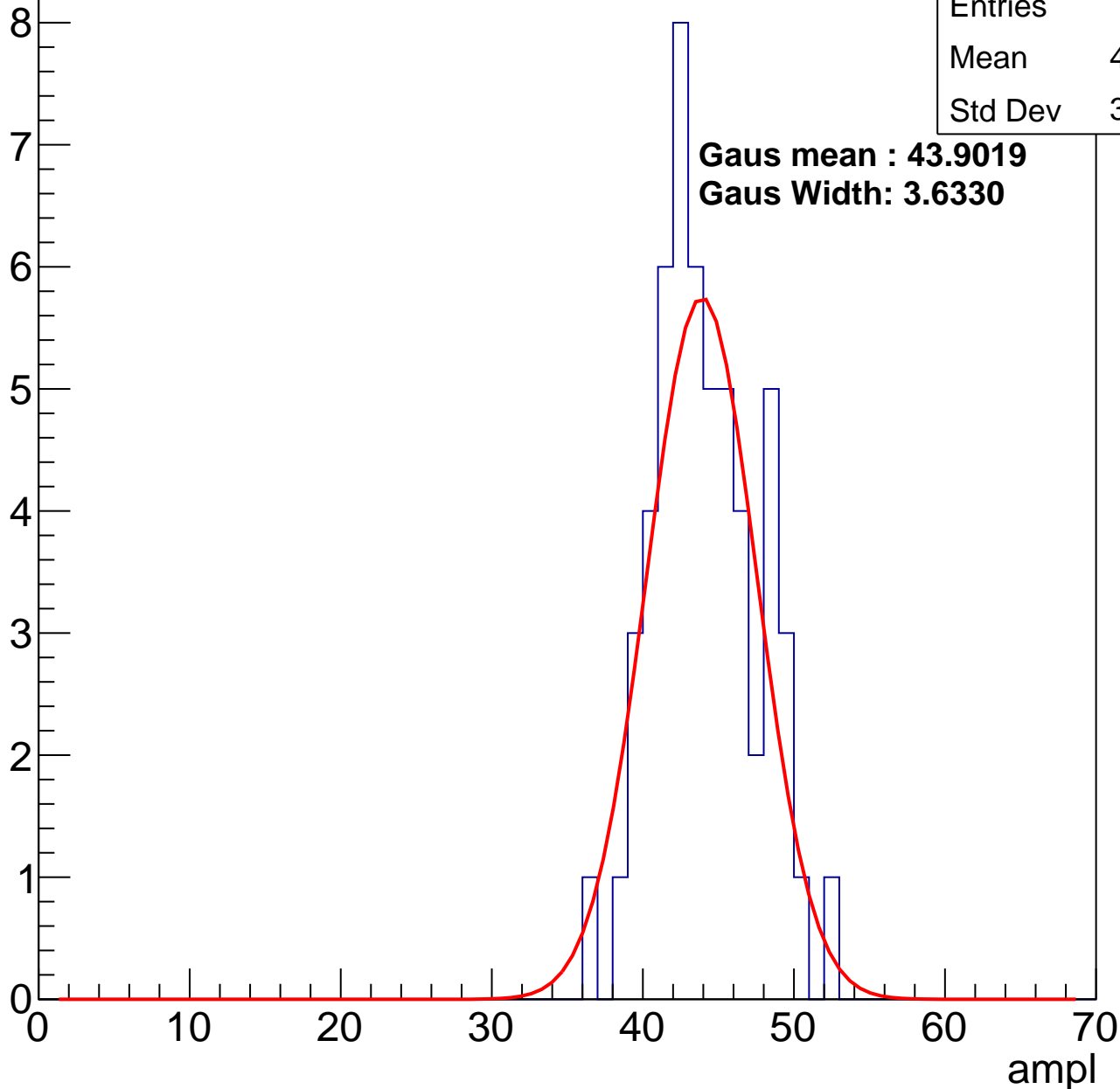
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	43.69
Std Dev	3.357

**Gaus mean : 43.9019**

**Gaus Width: 3.6330**

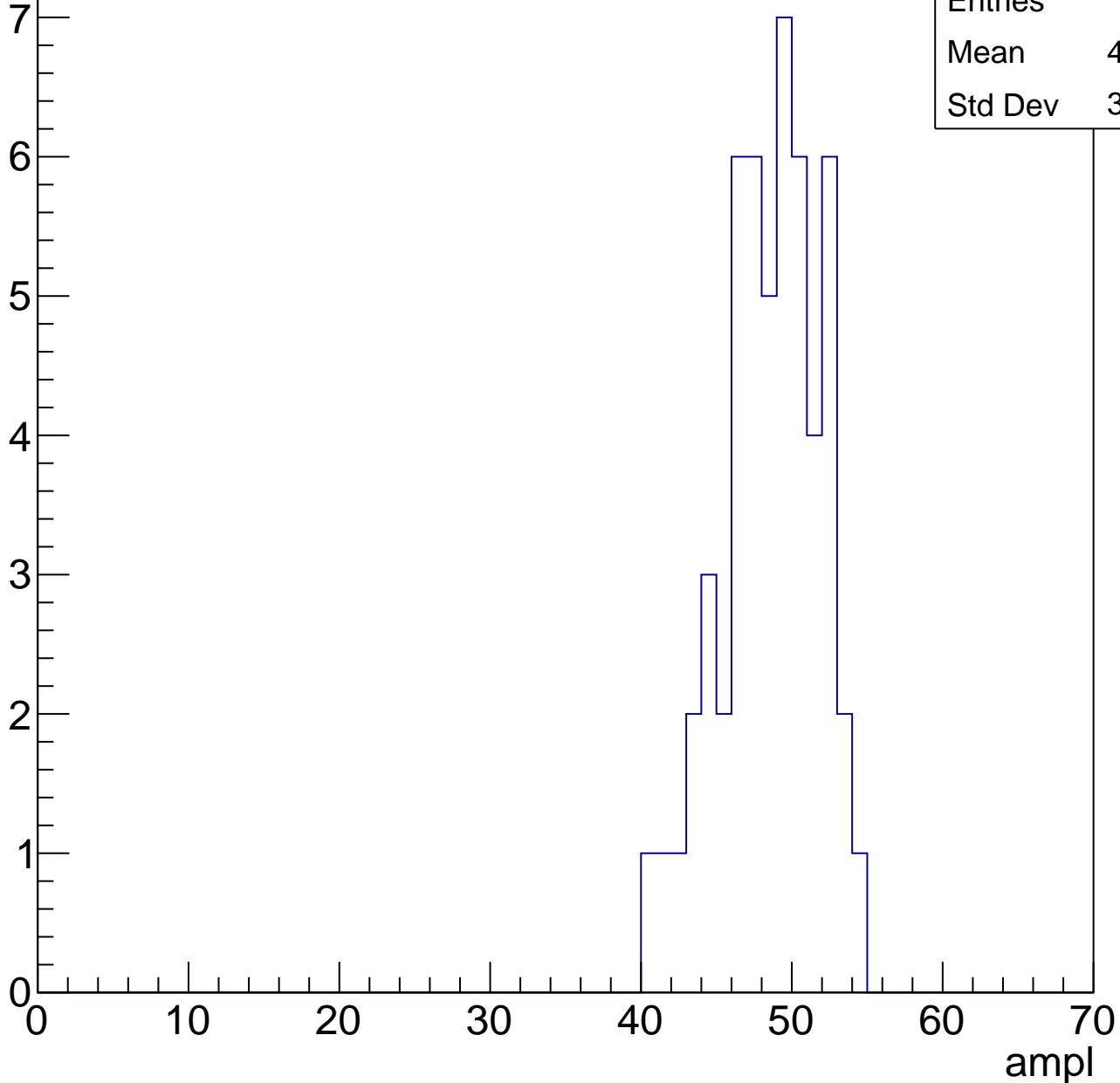


# B1L101S, U18-ch12, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	48.08
Std Dev	3.203

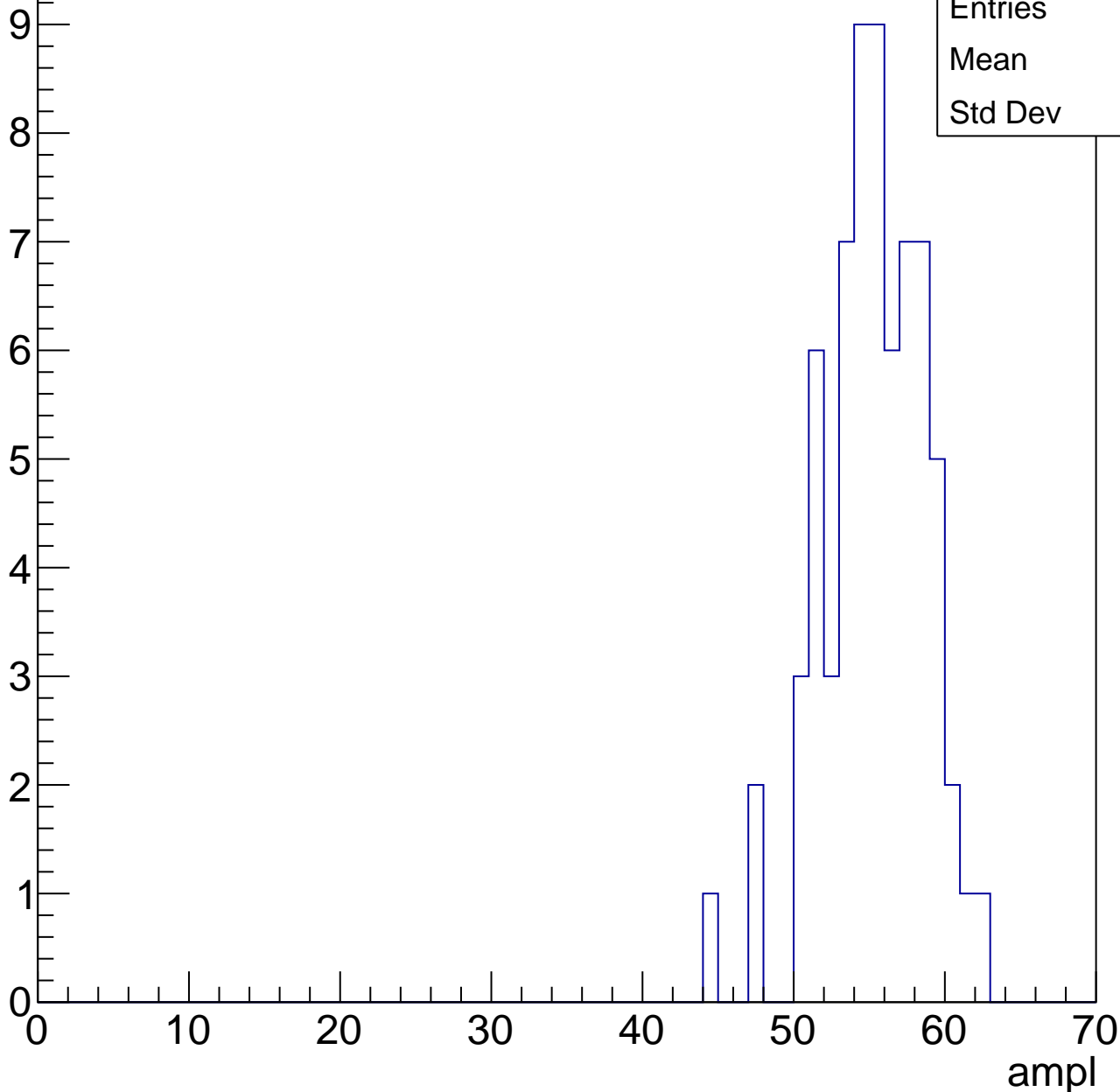


# B1L101S, U18-ch12, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	54.8
Std Dev	3.39



# B1L101S, U18-ch12, adc5

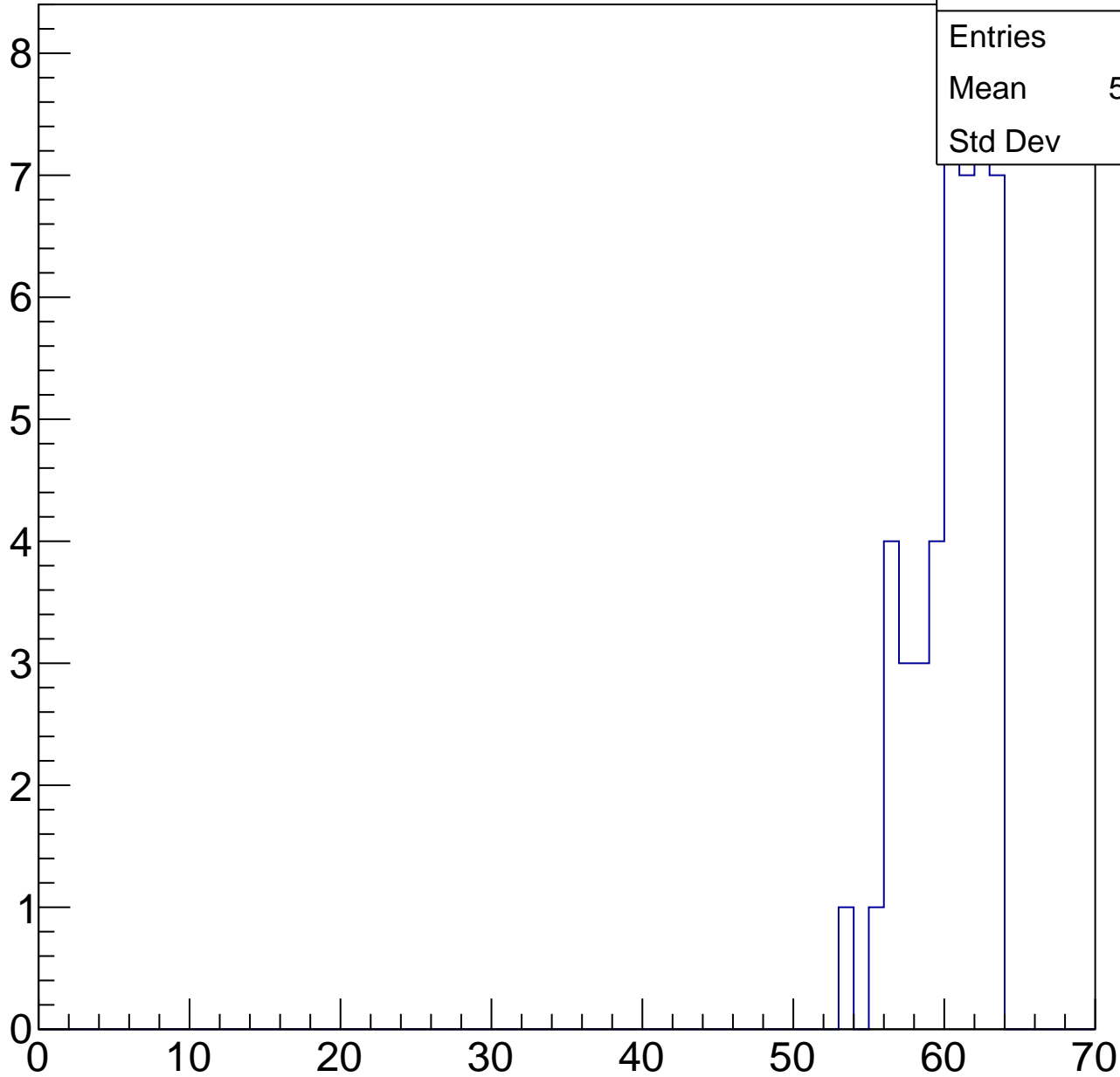
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	46
Mean	59.93
Std Dev	2.48

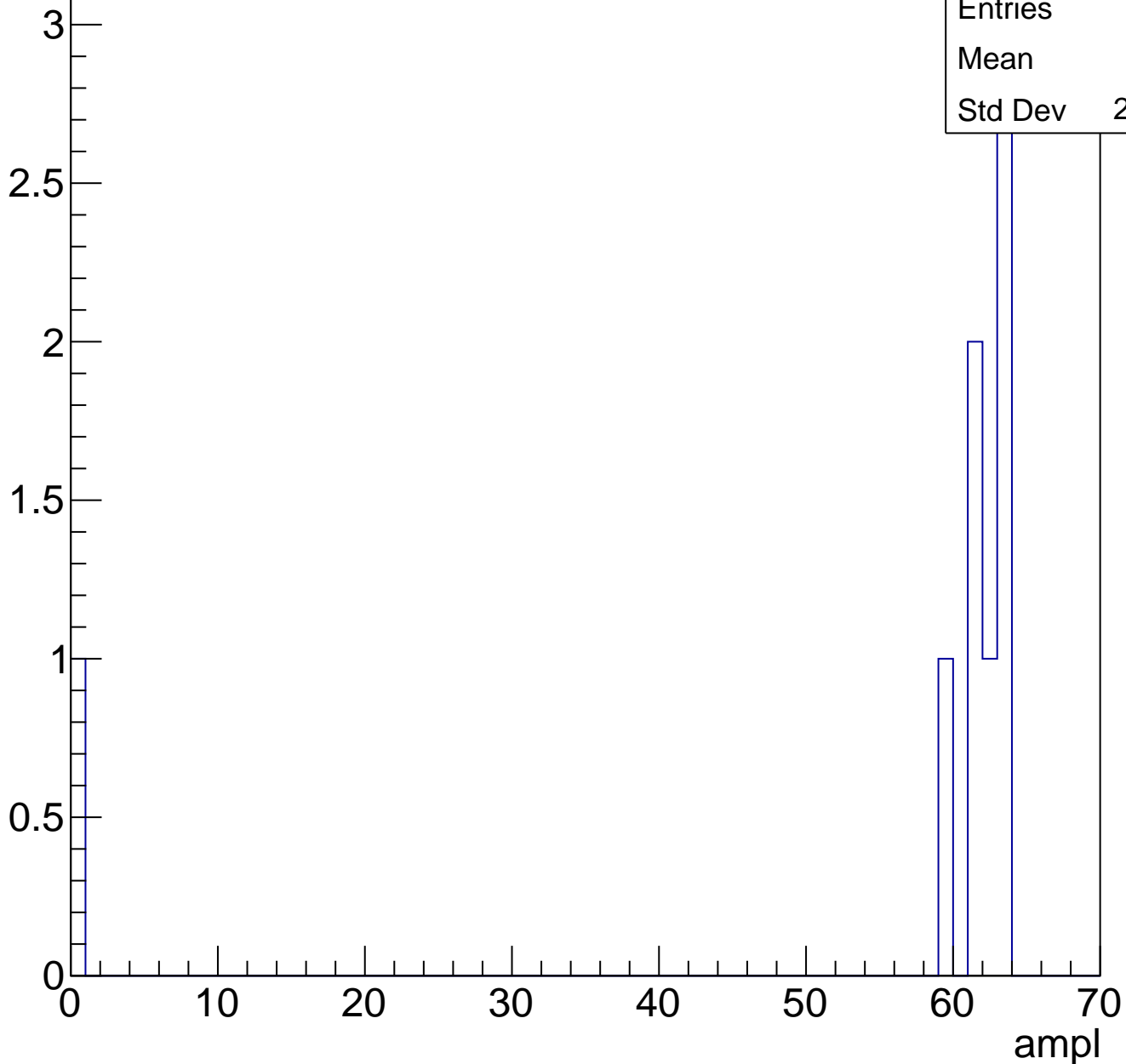
ampl



# B1L101S, U18-ch12, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch12, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U18-ch13, adc0

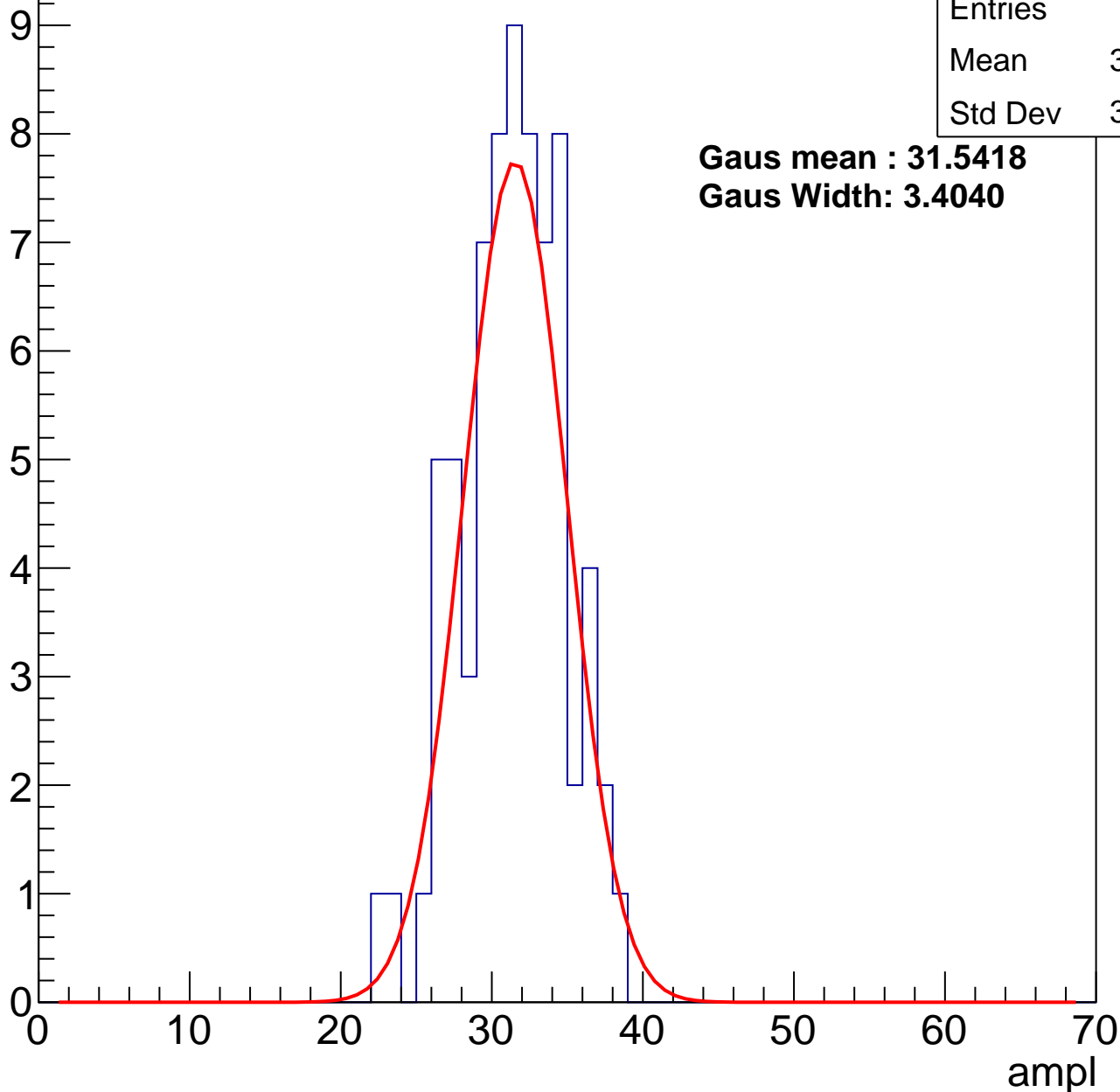
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	30.92
Std Dev	3.353

**Gaus mean : 31.5418**

**Gaus Width: 3.4040**



# B1L101S, U18-ch13, adc1

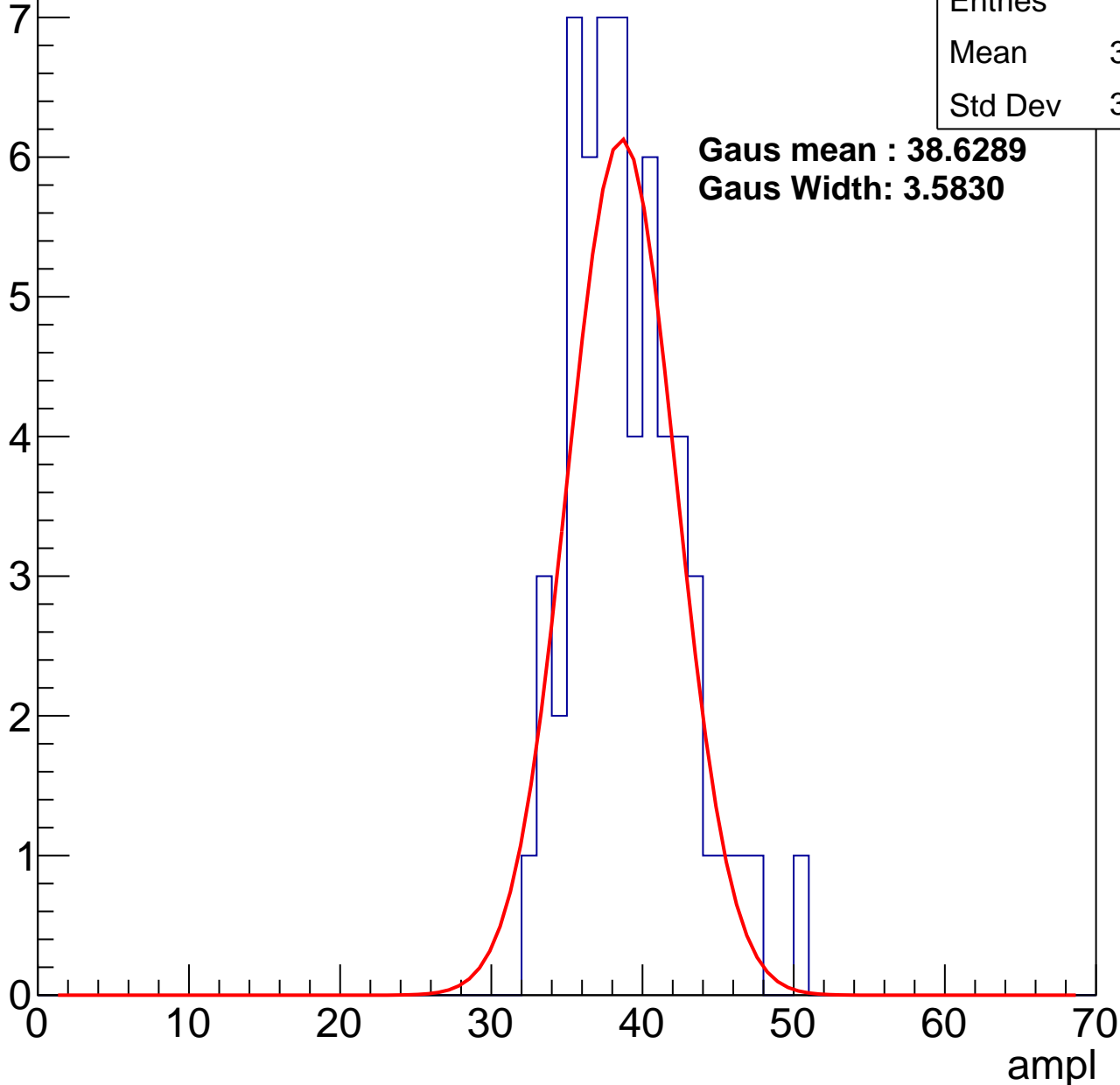
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	38.54
Std Dev	3.675

**Gaus mean : 38.6289**

**Gaus Width: 3.5830**



# B1L101S, U18-ch13, adc2

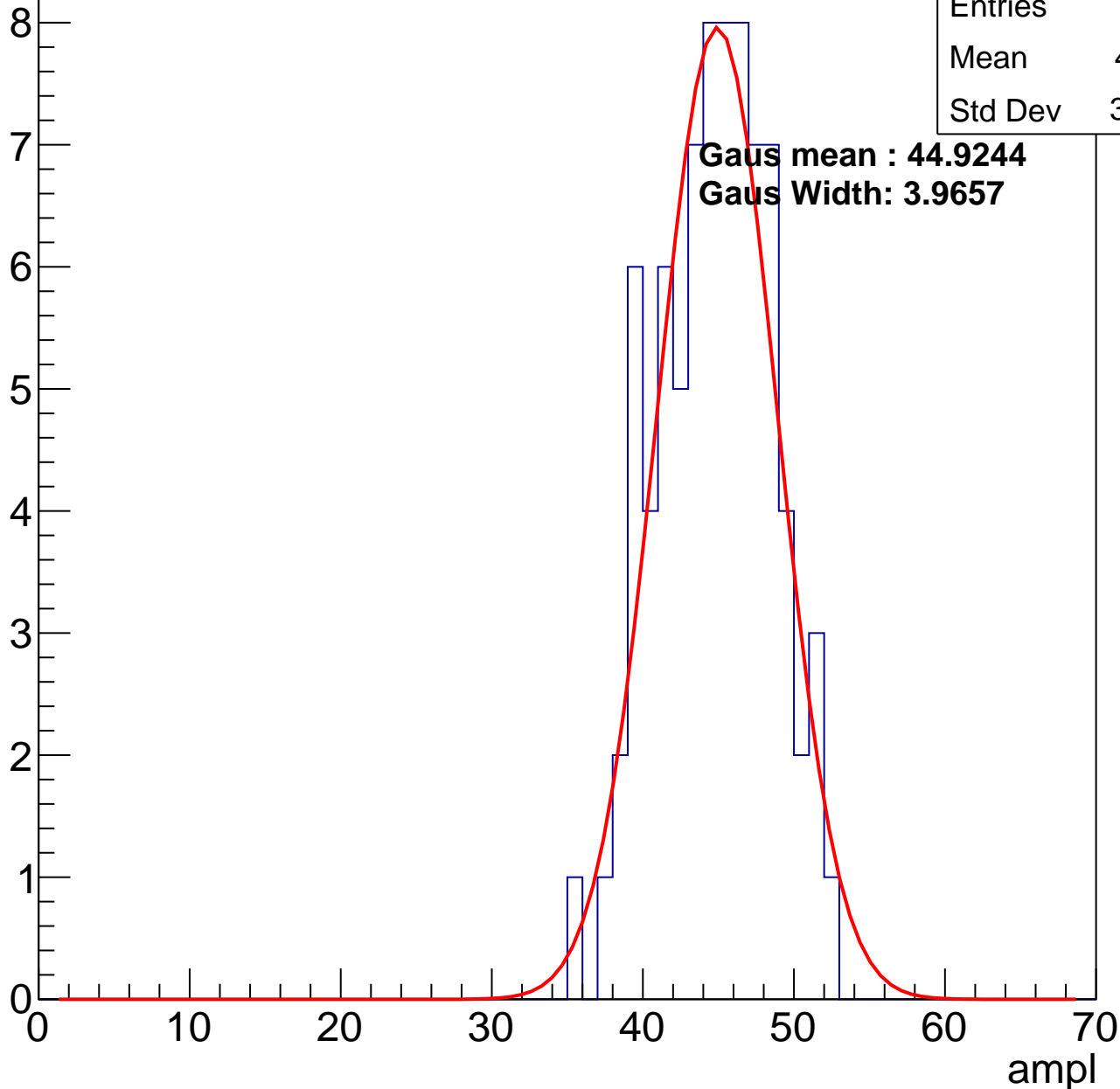
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	80
Mean	44.31
Std Dev	3.686

**Gaus mean : 44.9244**

**Gaus Width: 3.9657**

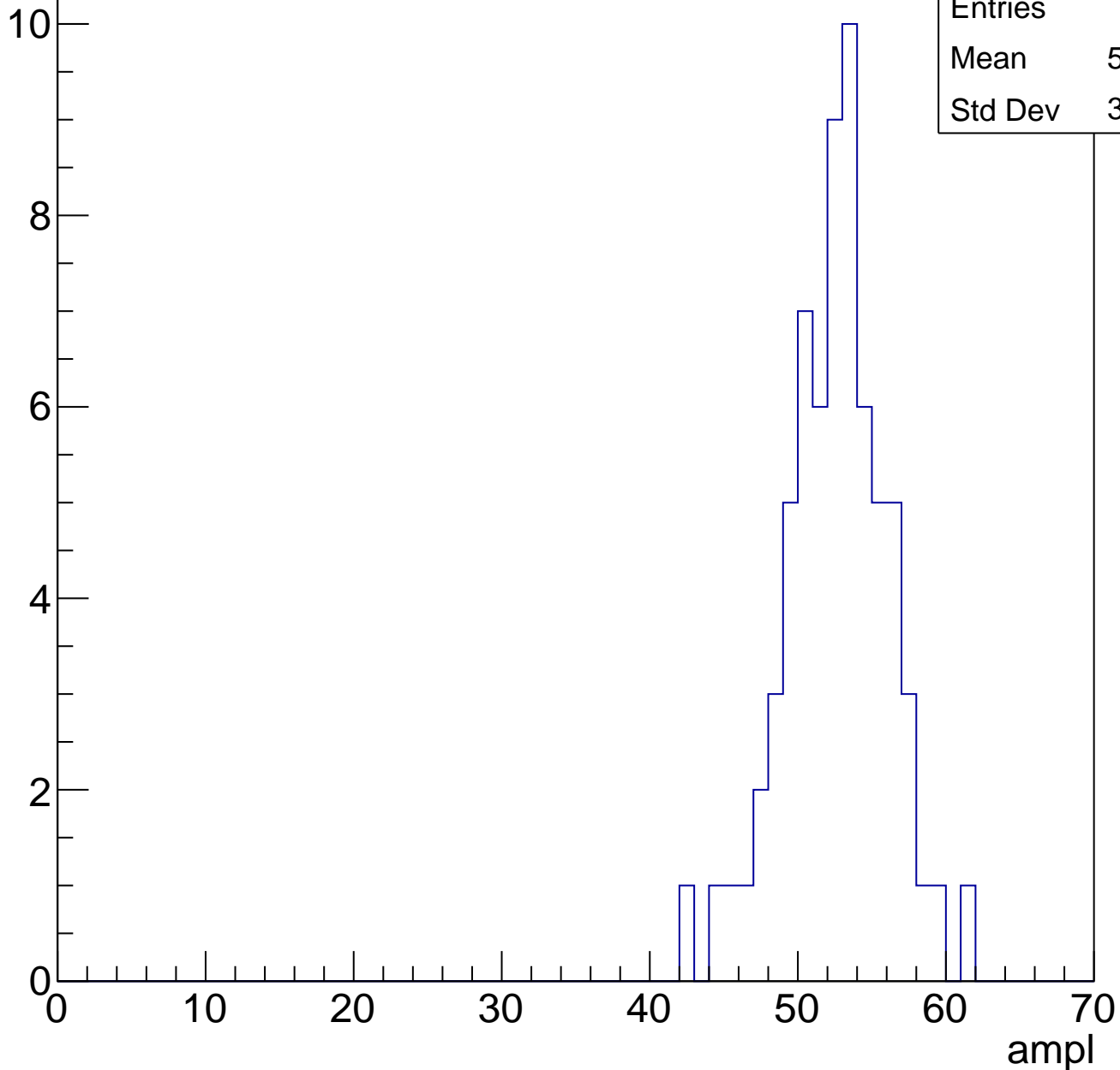


# B1L101S, U18-ch13, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	68
Mean	52.09
Std Dev	3.484

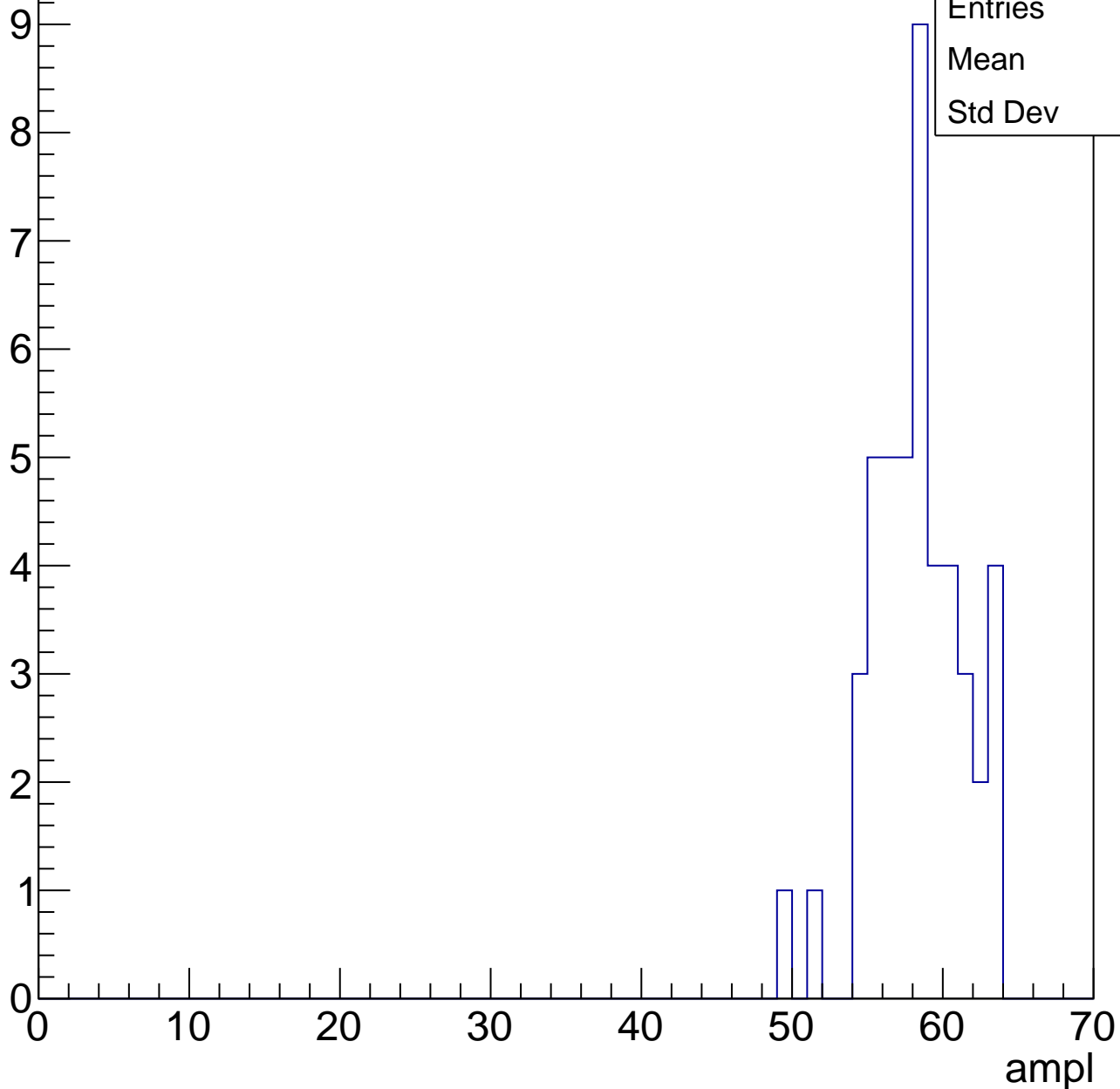
Entry



# B1L101S, U18-ch13, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

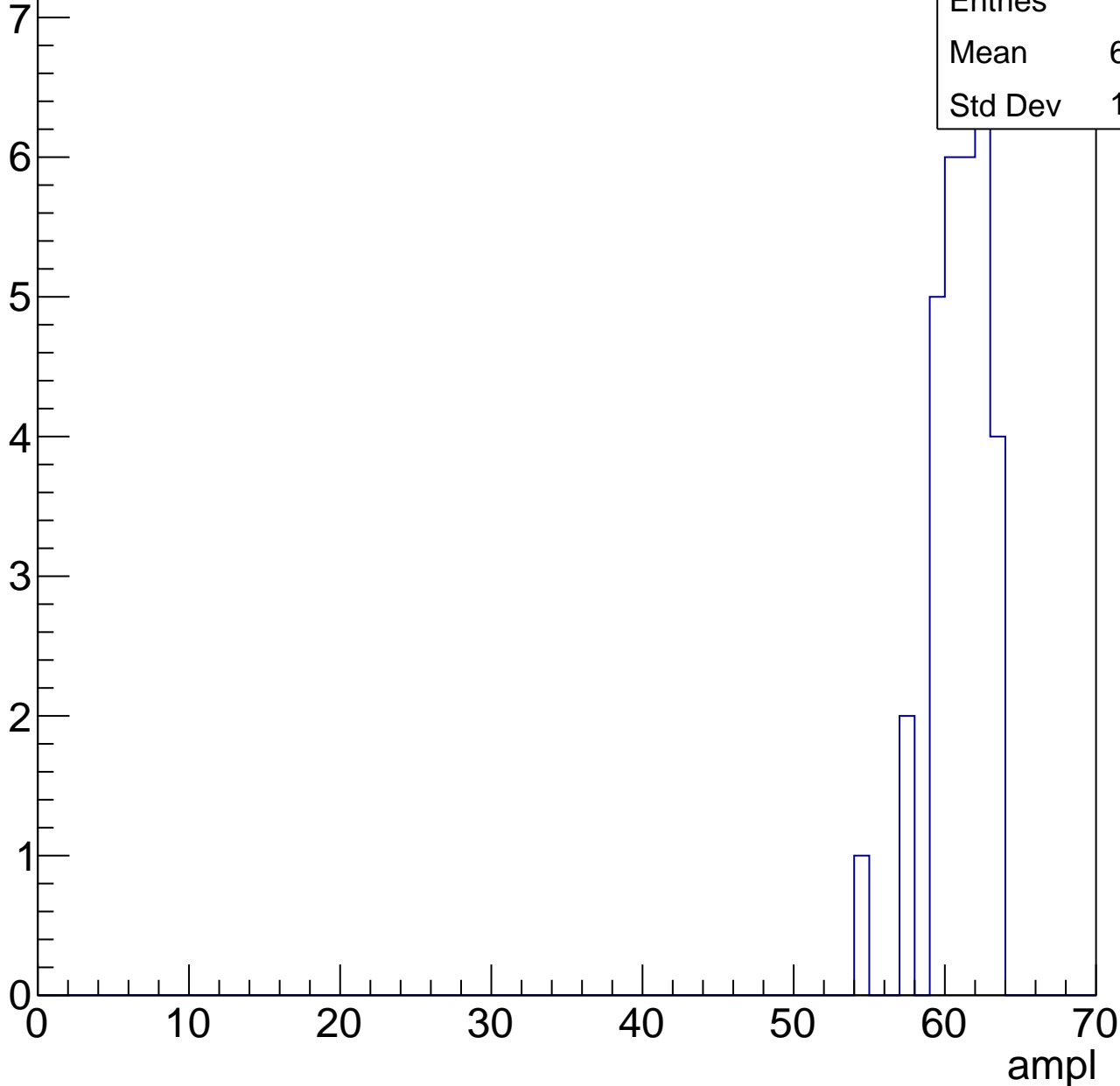


# B1L101S, U18-ch13, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	31
Mean	60.48
Std Dev	1.982



# B1L101S, U18-ch13, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch13, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch14, adc0

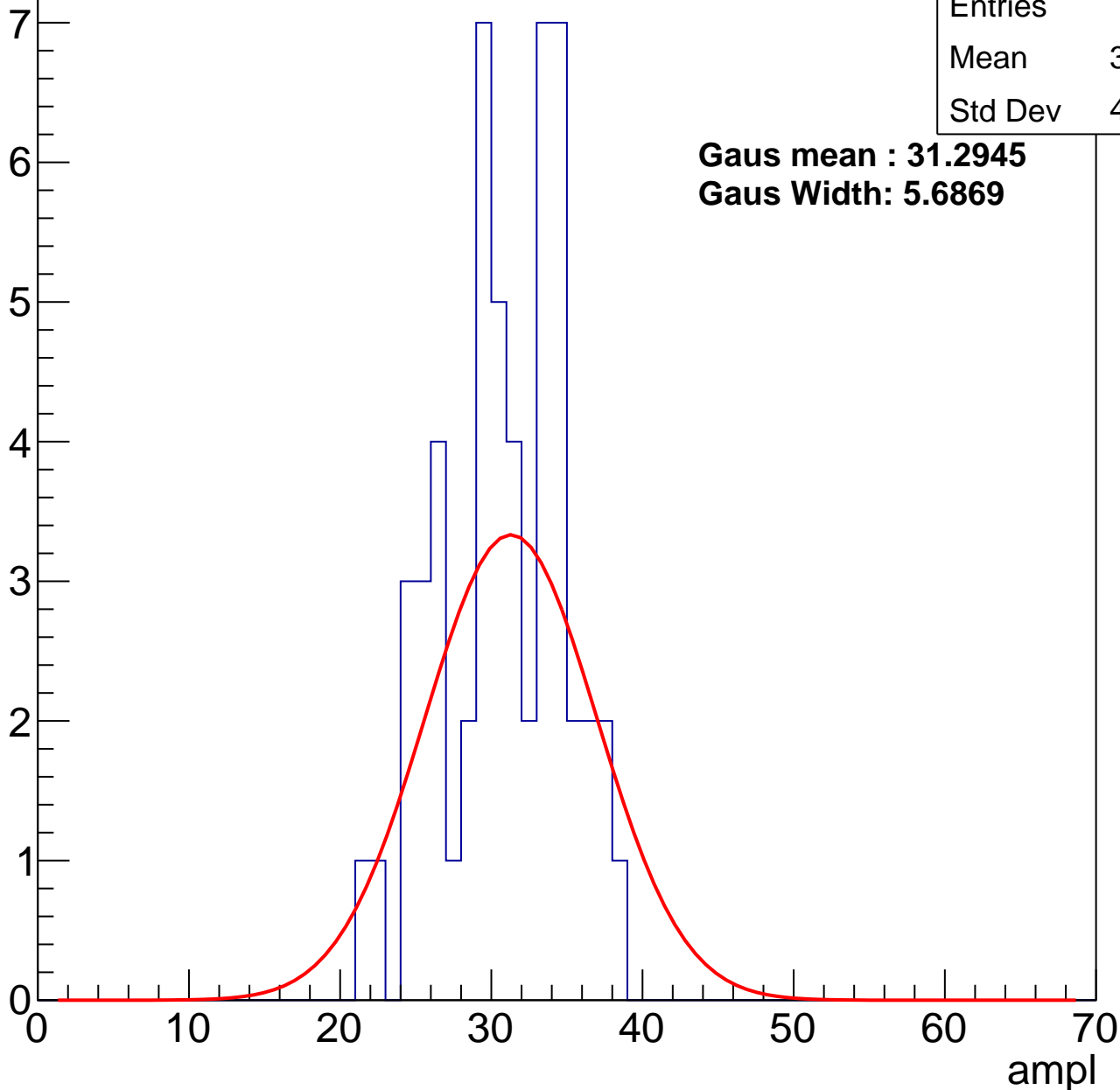
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	30.39
Std Dev	4.034

**Gaus mean : 31.2945**

**Gaus Width: 5.6869**



# B1L101S, U18-ch14, adc1

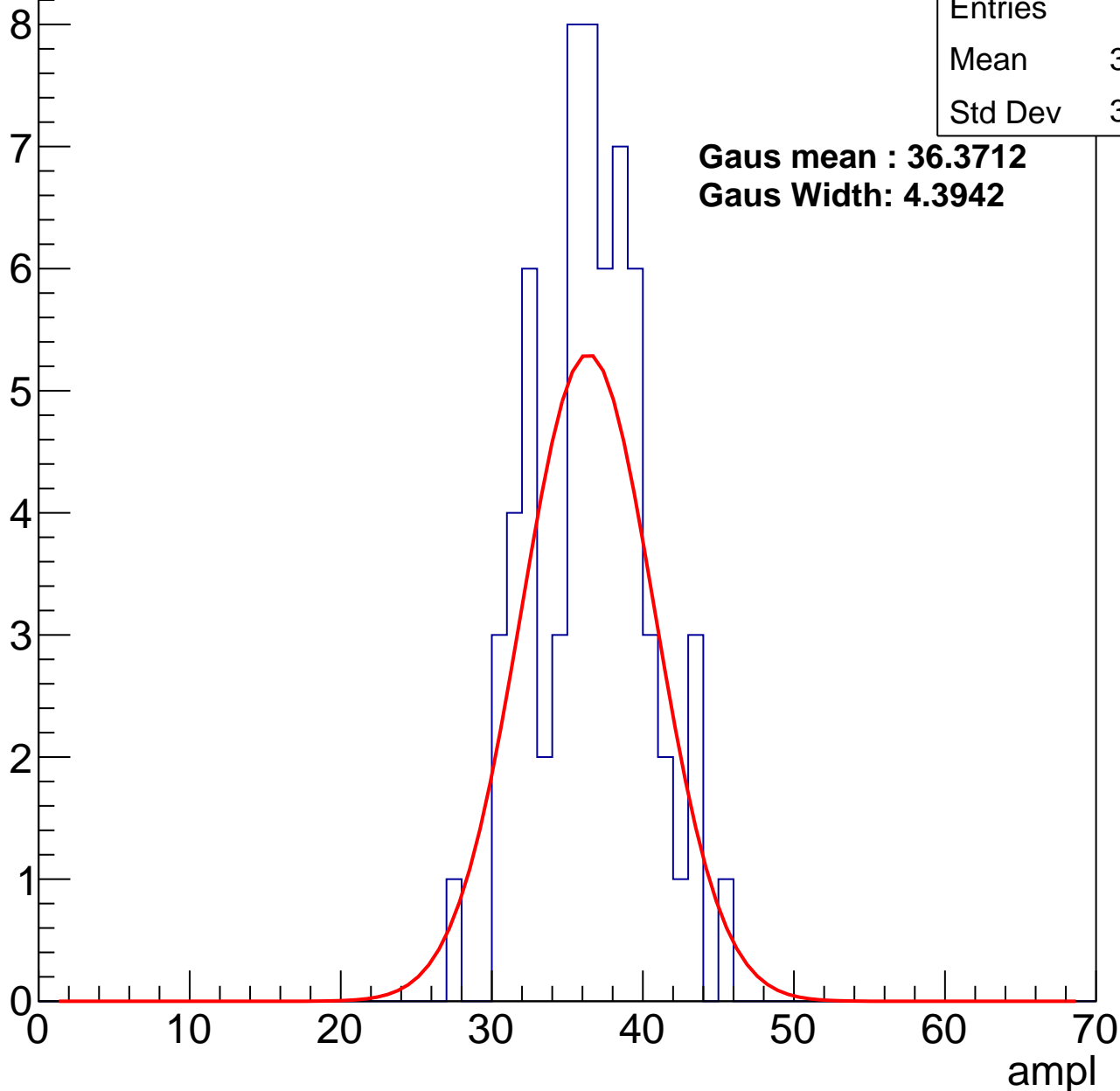
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	36.08
Std Dev	3.692

**Gaus mean : 36.3712**

**Gaus Width: 4.3942**



# B1L101S, U18-ch14, adc2

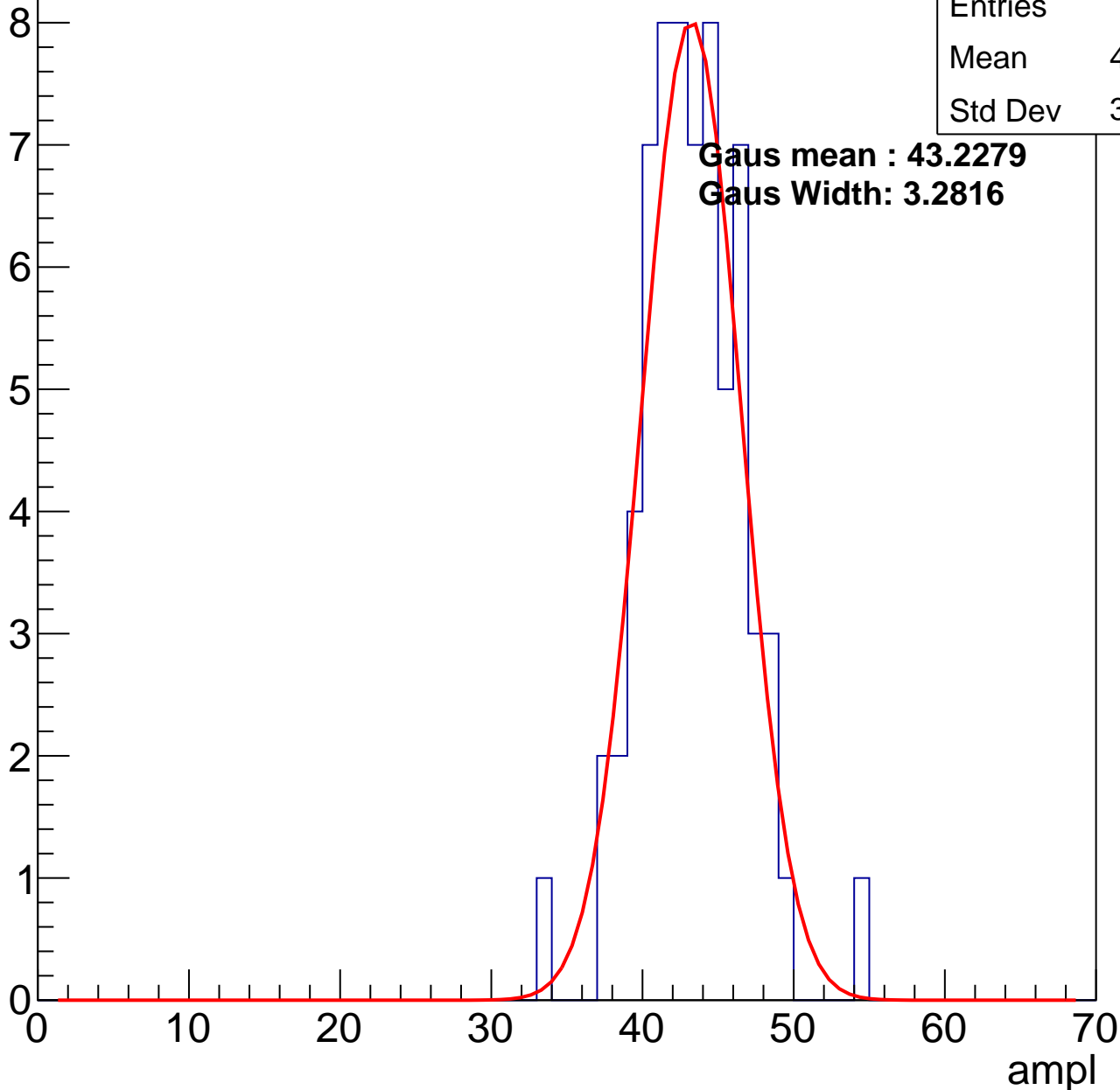
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	42.85
Std Dev	3.365

**Gaus mean : 43.2279**

**Gaus Width: 3.2816**

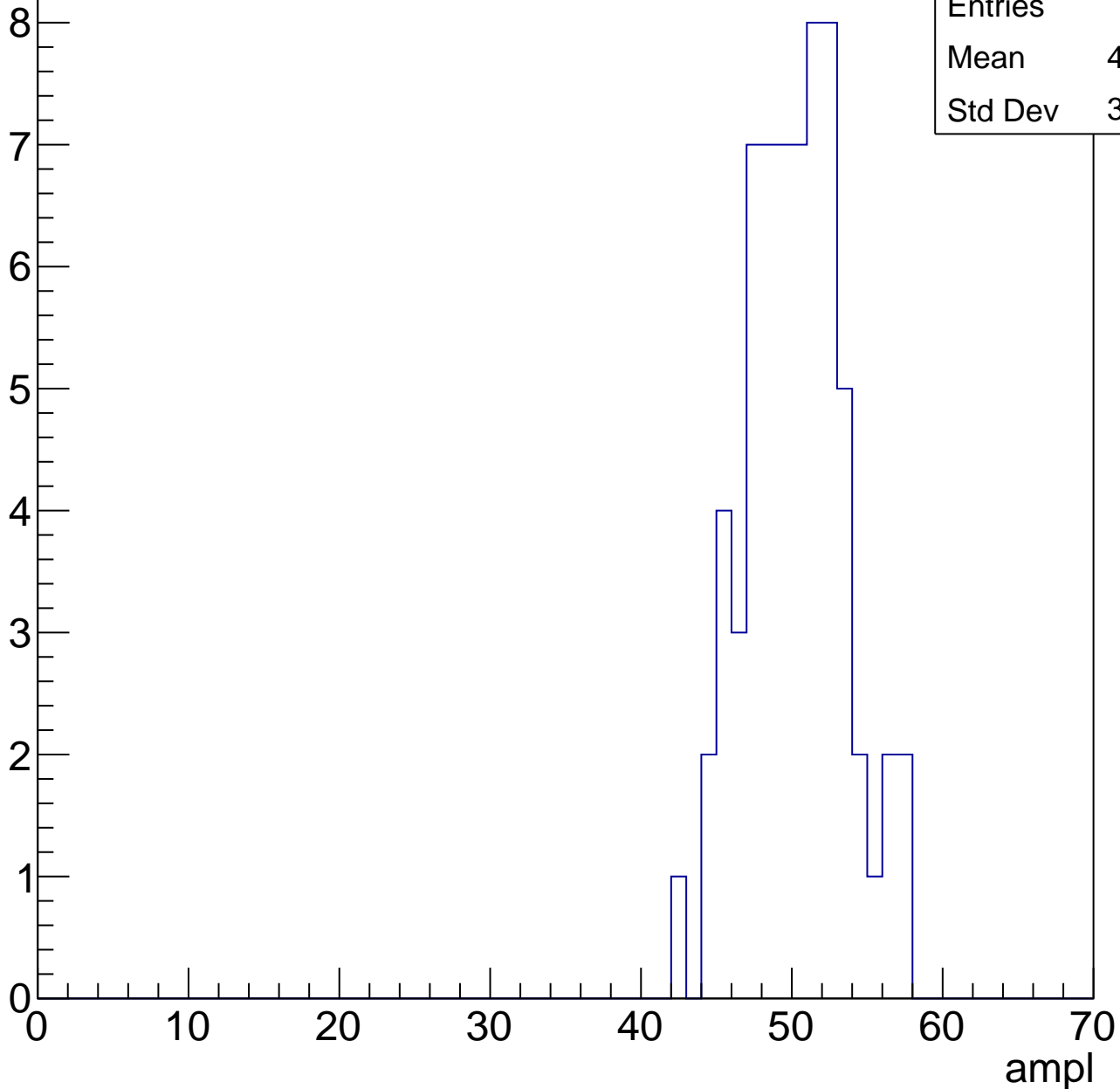


# B1L101S, U18-ch14, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	49.76
Std Dev	3.234

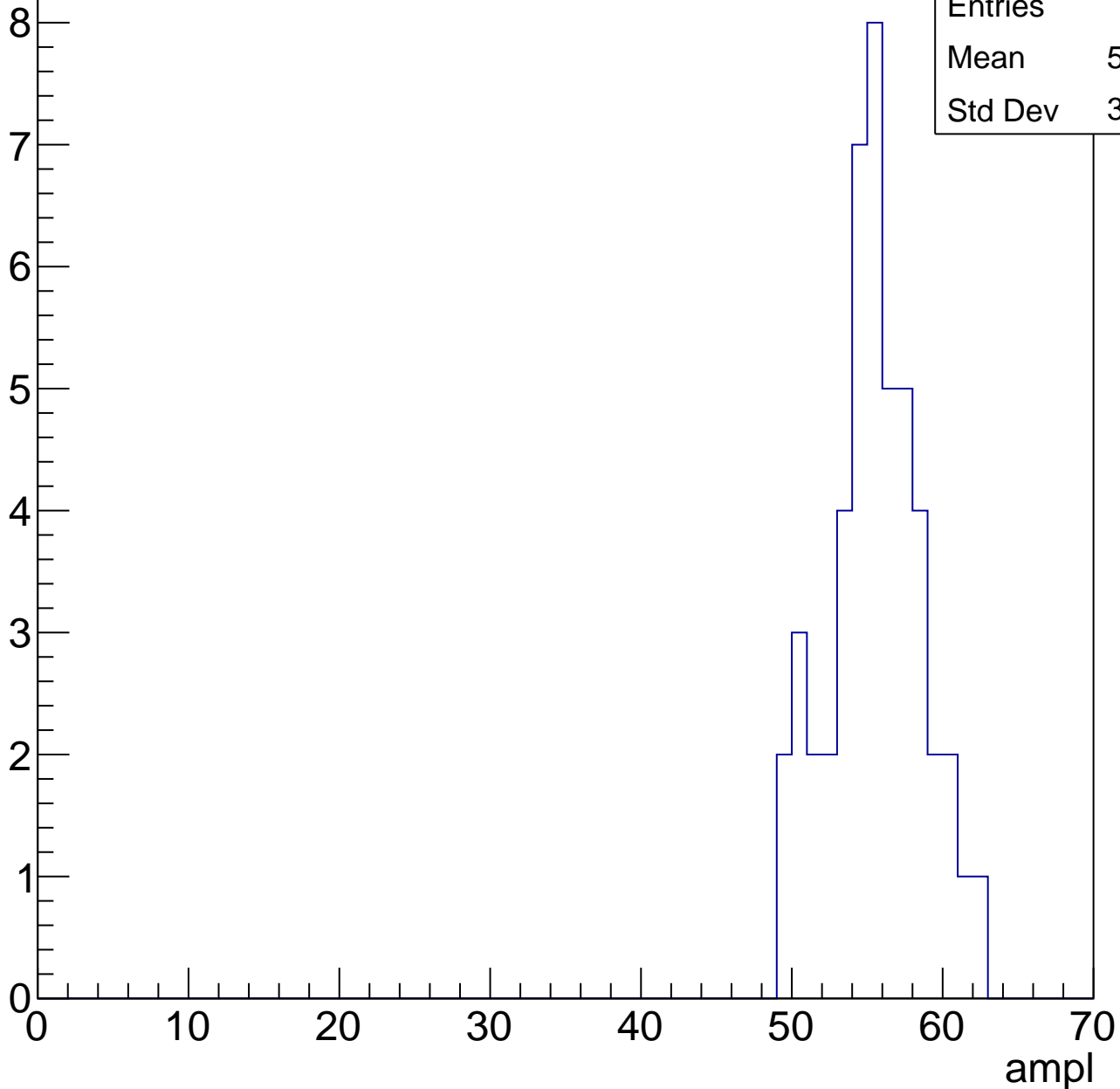


# B1L101S, U18-ch14, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	48
Mean	55.04
Std Dev	3.055

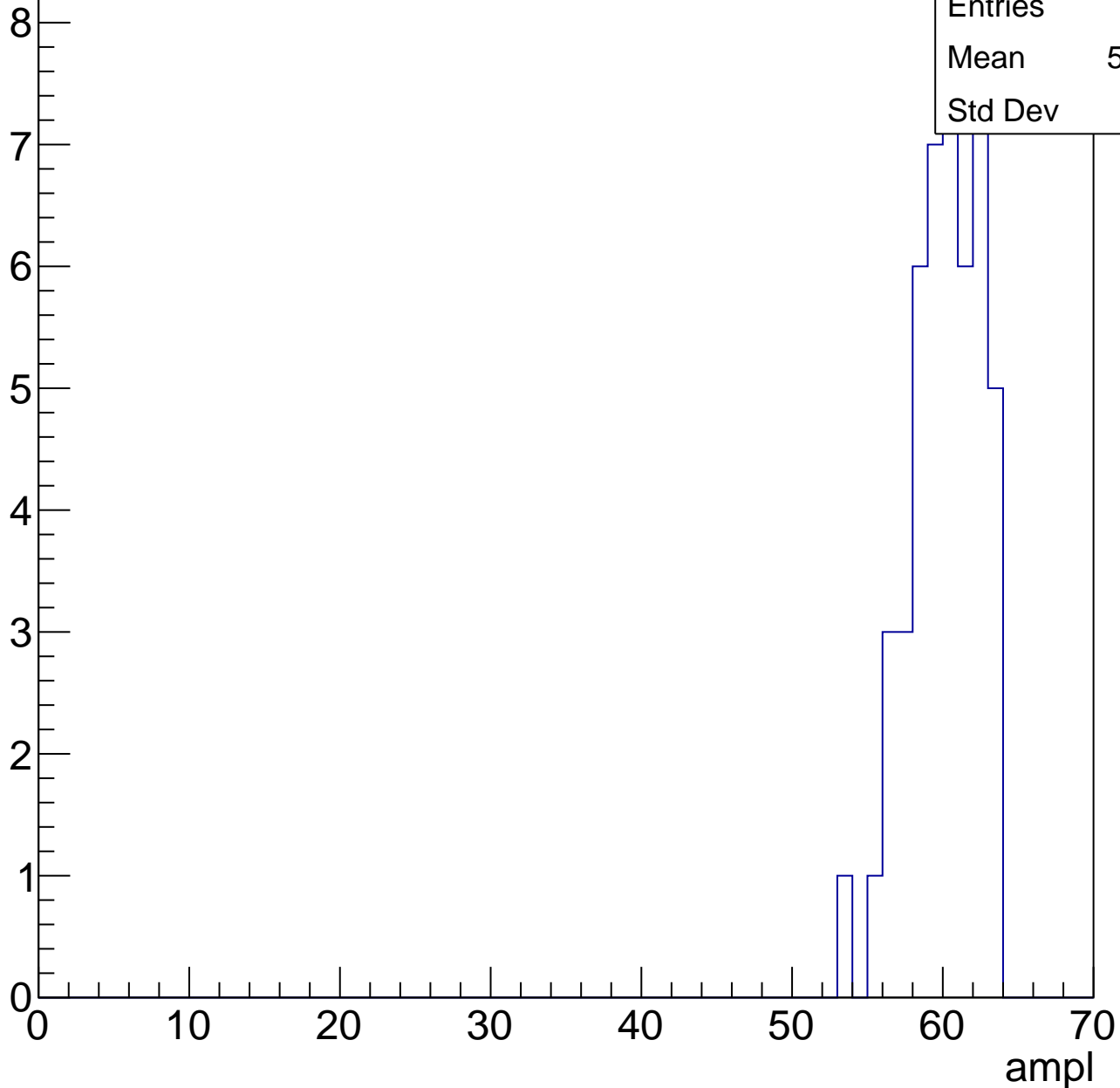


# B1L101S, U18-ch14, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	48
Mean	59.69
Std Dev	2.32

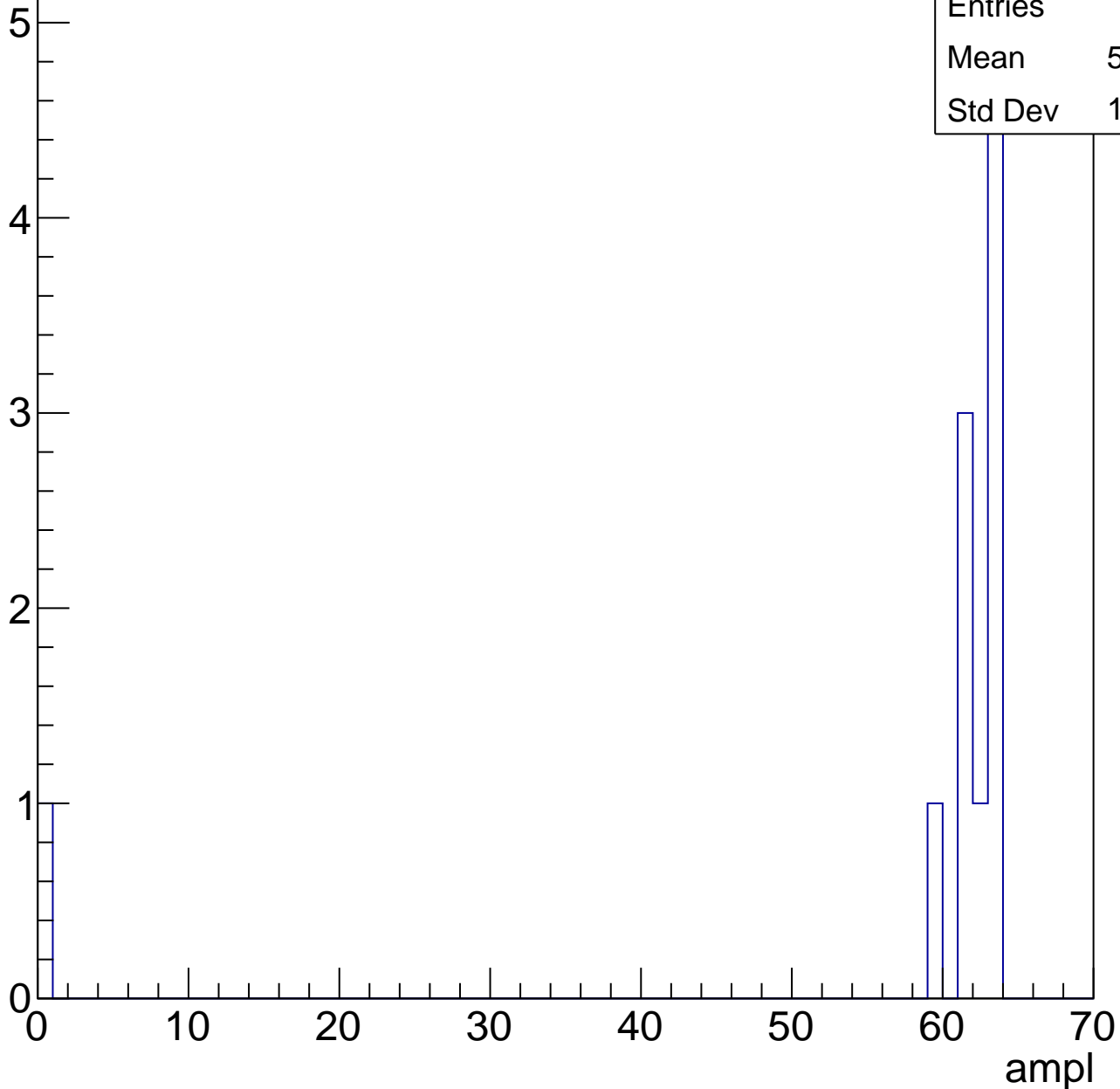


# B1L101S, U18-ch14, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	11
Mean	56.27
Std Dev	17.84





# B1L101S, U18-ch14, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch15, adc0

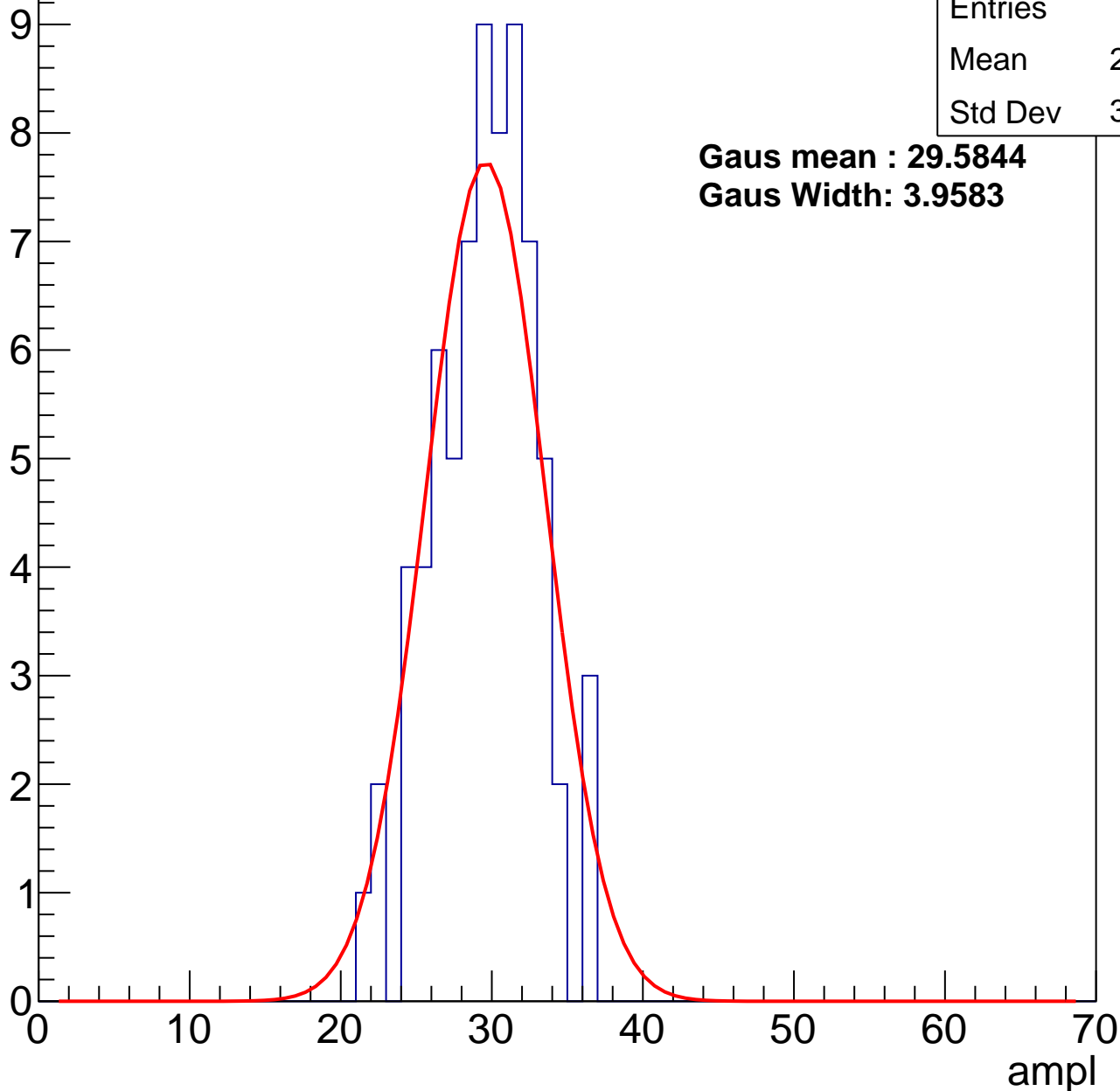
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	29.07
Std Dev	3.314

**Gaus mean : 29.5844**

**Gaus Width: 3.9583**



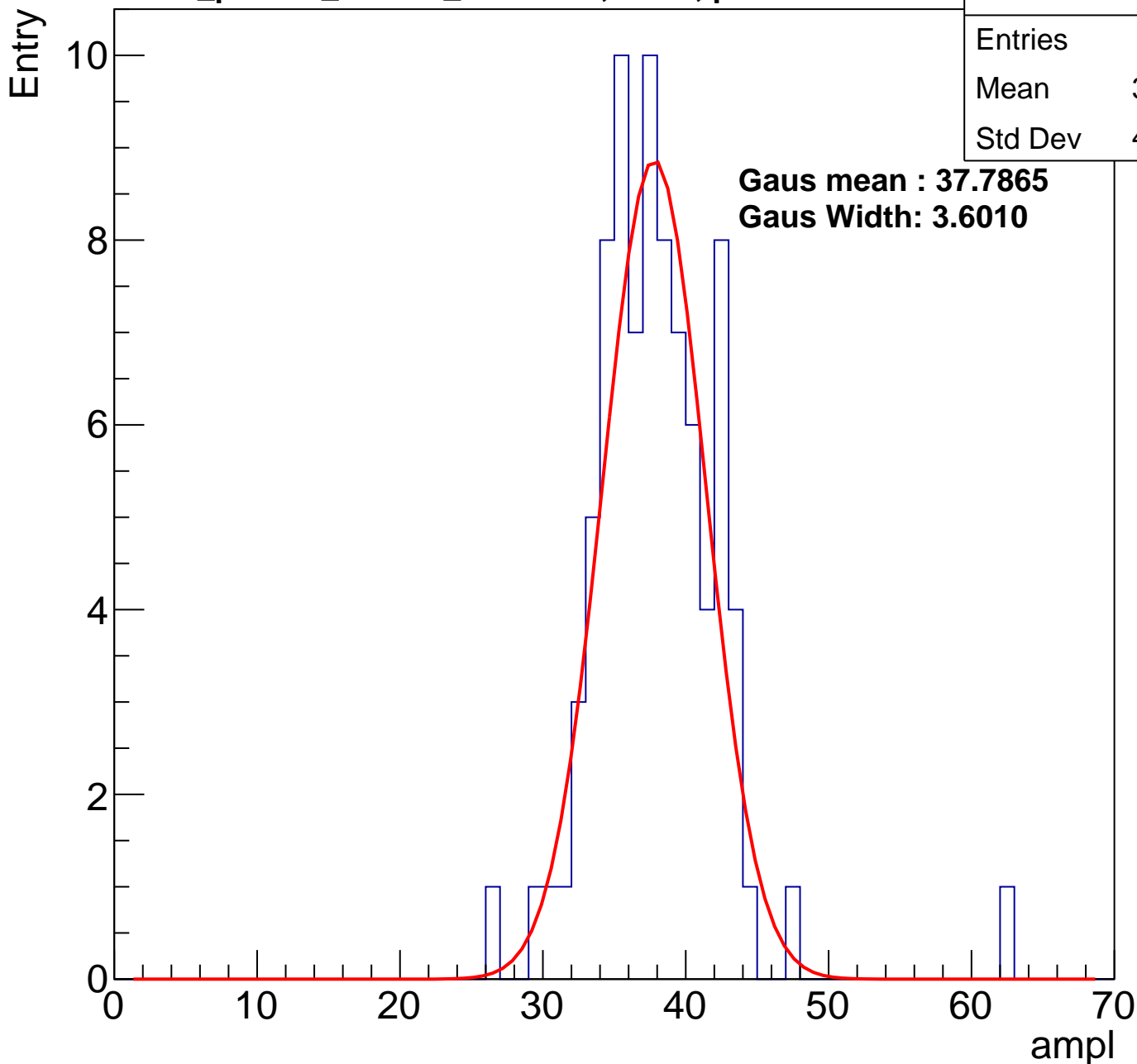
# B1L101S, U18-ch15, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	87
Mean	37.51
Std Dev	4.541

**Gaus mean : 37.7865**

**Gaus Width: 3.6010**



# B1L101S, U18-ch15, adc2

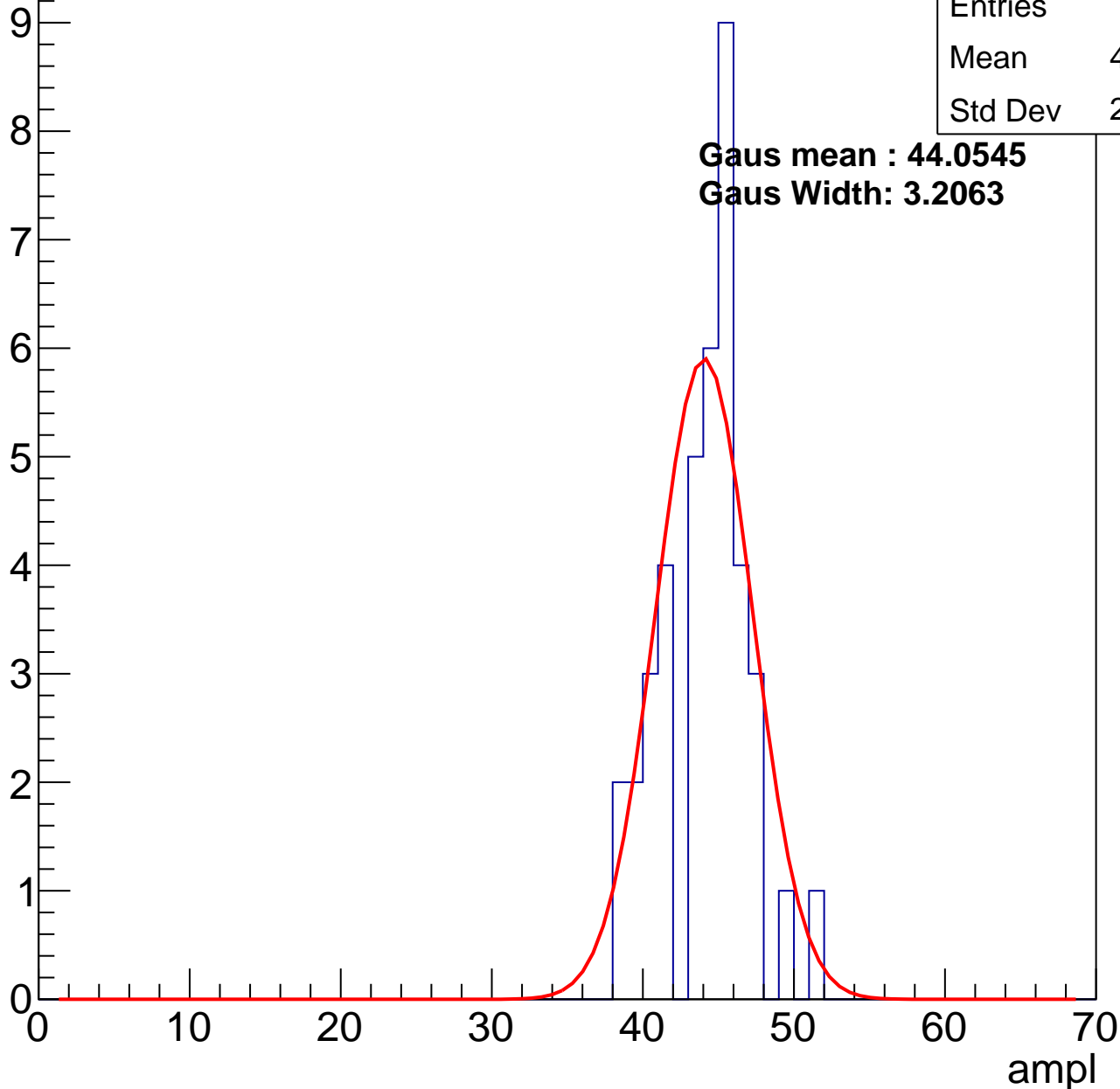
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	40
Mean	43.67
Std Dev	2.884

**Gaus mean : 44.0545**

**Gaus Width: 3.2063**

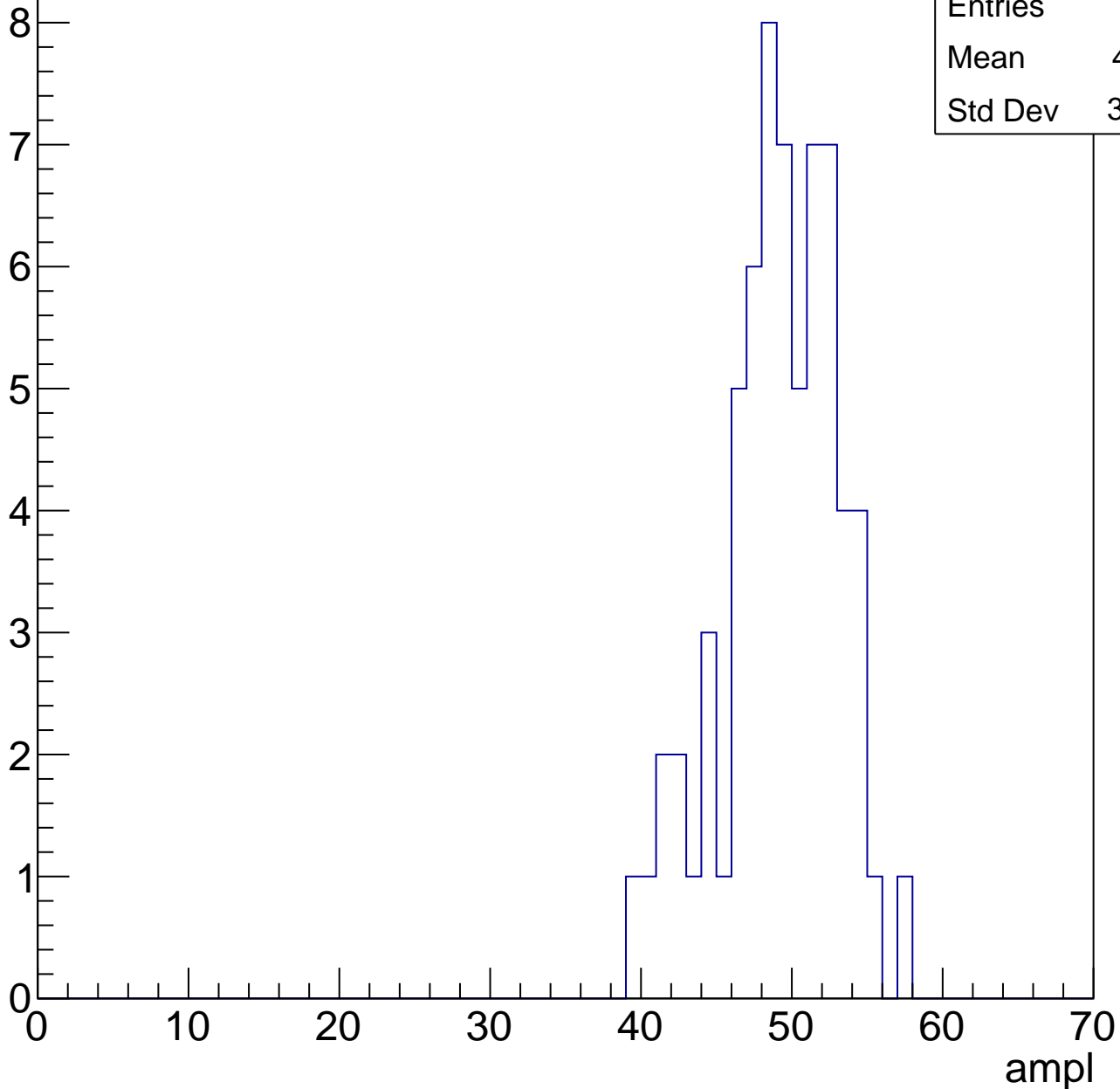


# B1L101S, U18-ch15, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

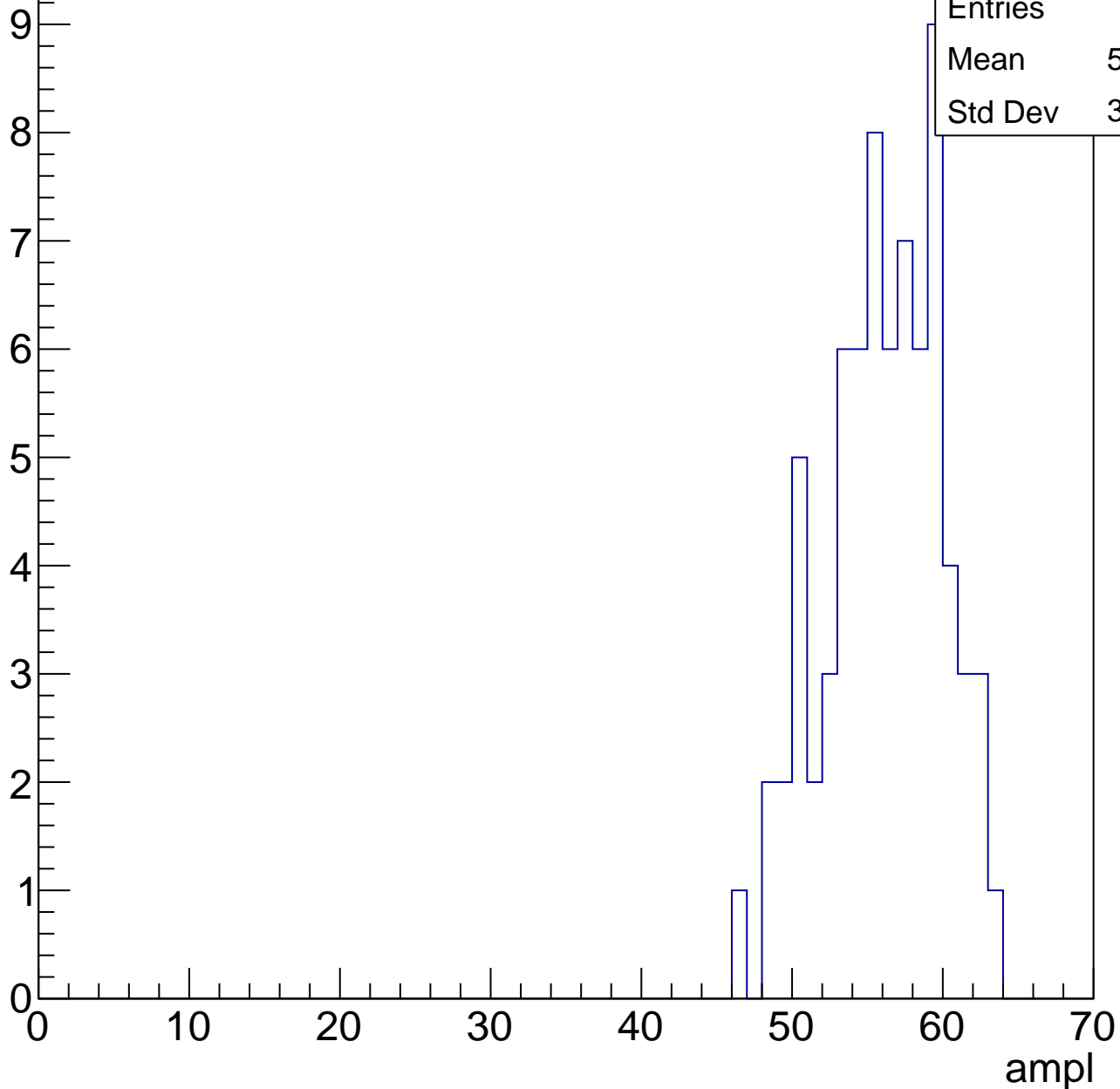
Entries	66
Mean	48.71
Std Dev	3.825



# B1L101S, U18-ch15, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



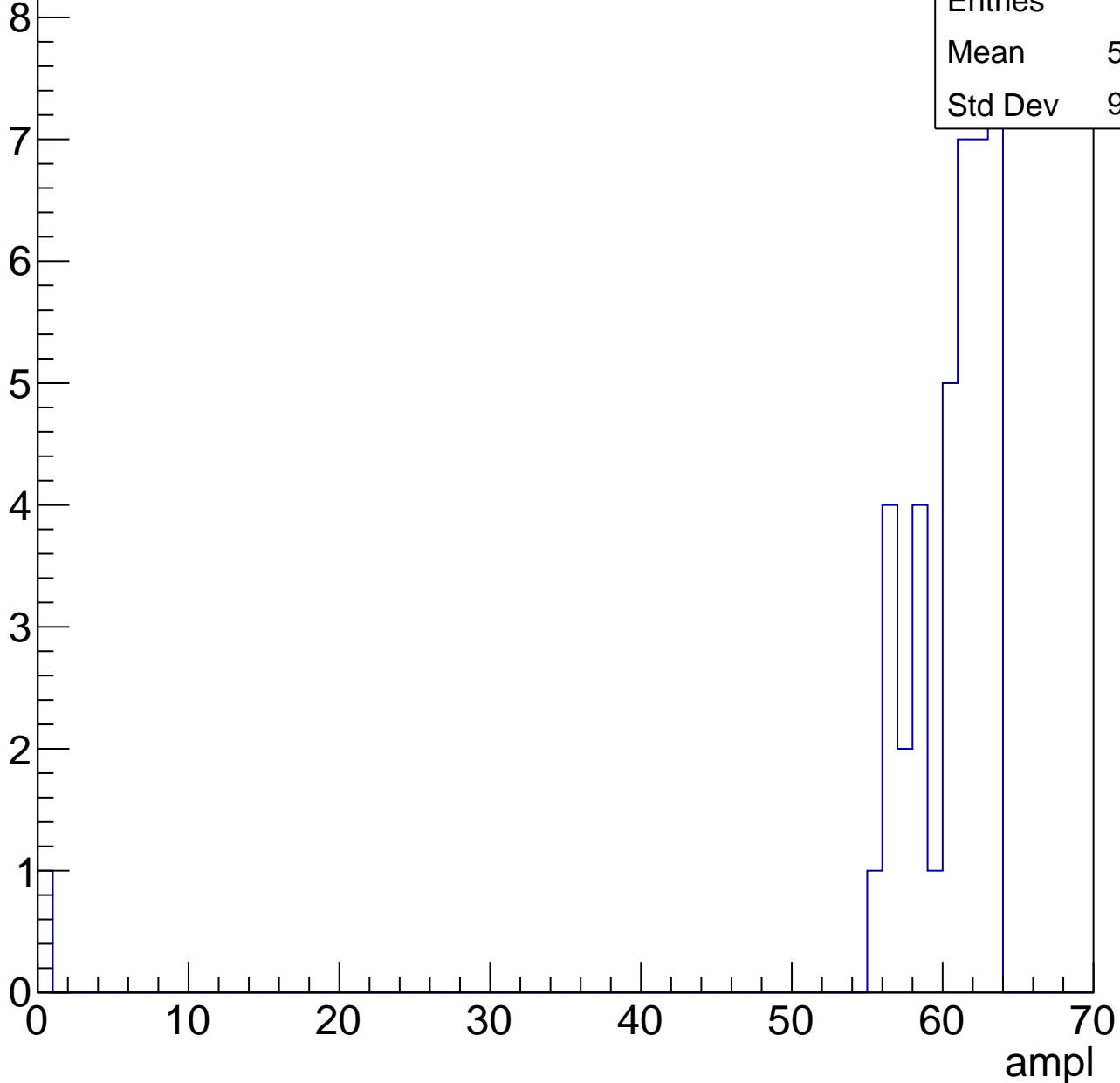
Entries	74
Mean	55.62
Std Dev	3.833

# B1L101S, U18-ch15, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	40
Mean	58.73
Std Dev	9.703



# B1L101S, U18-ch15, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch15, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch16, adc0

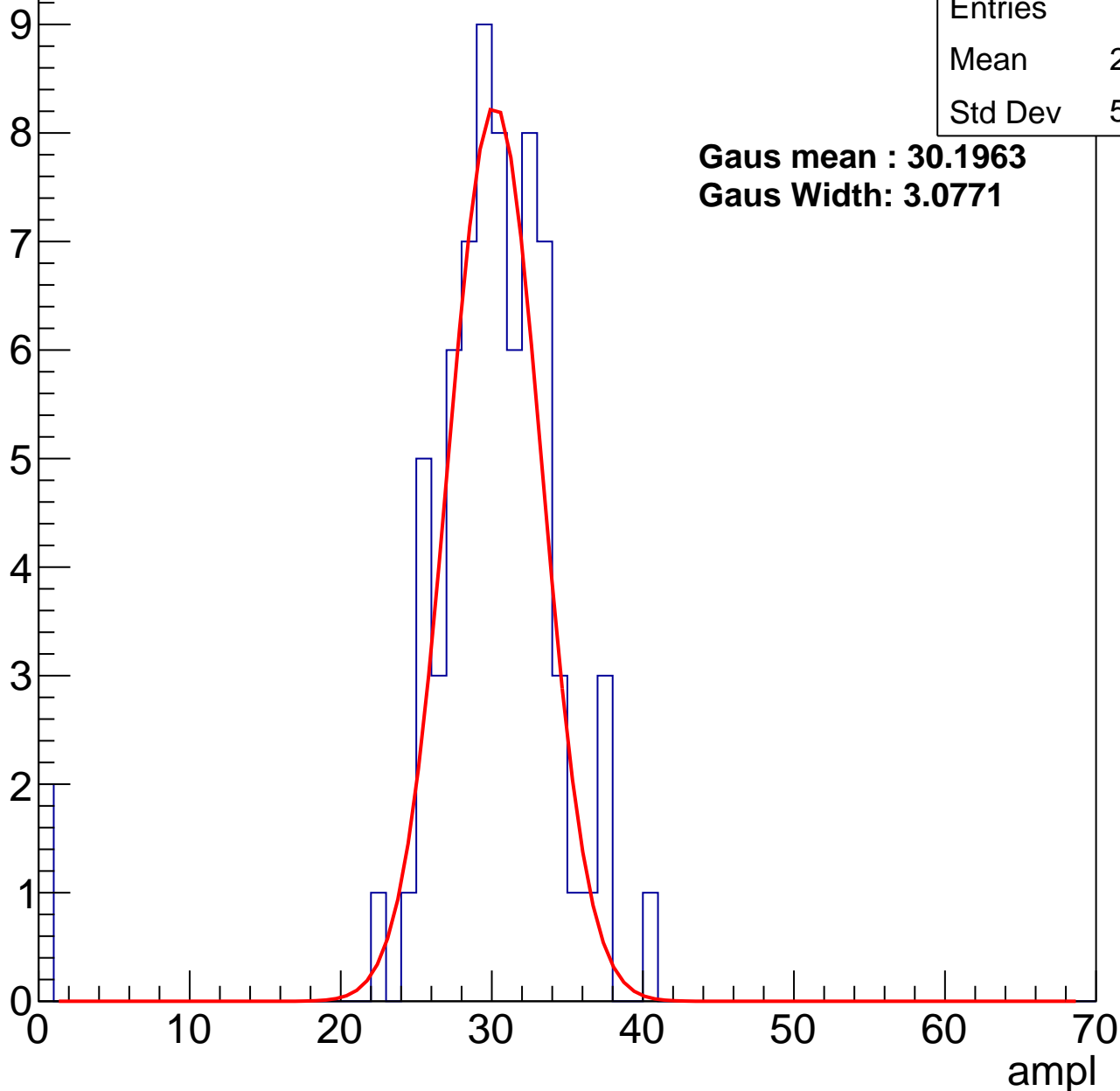
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	29.24
Std Dev	5.985

**Gaus mean : 30.1963**

**Gaus Width: 3.0771**



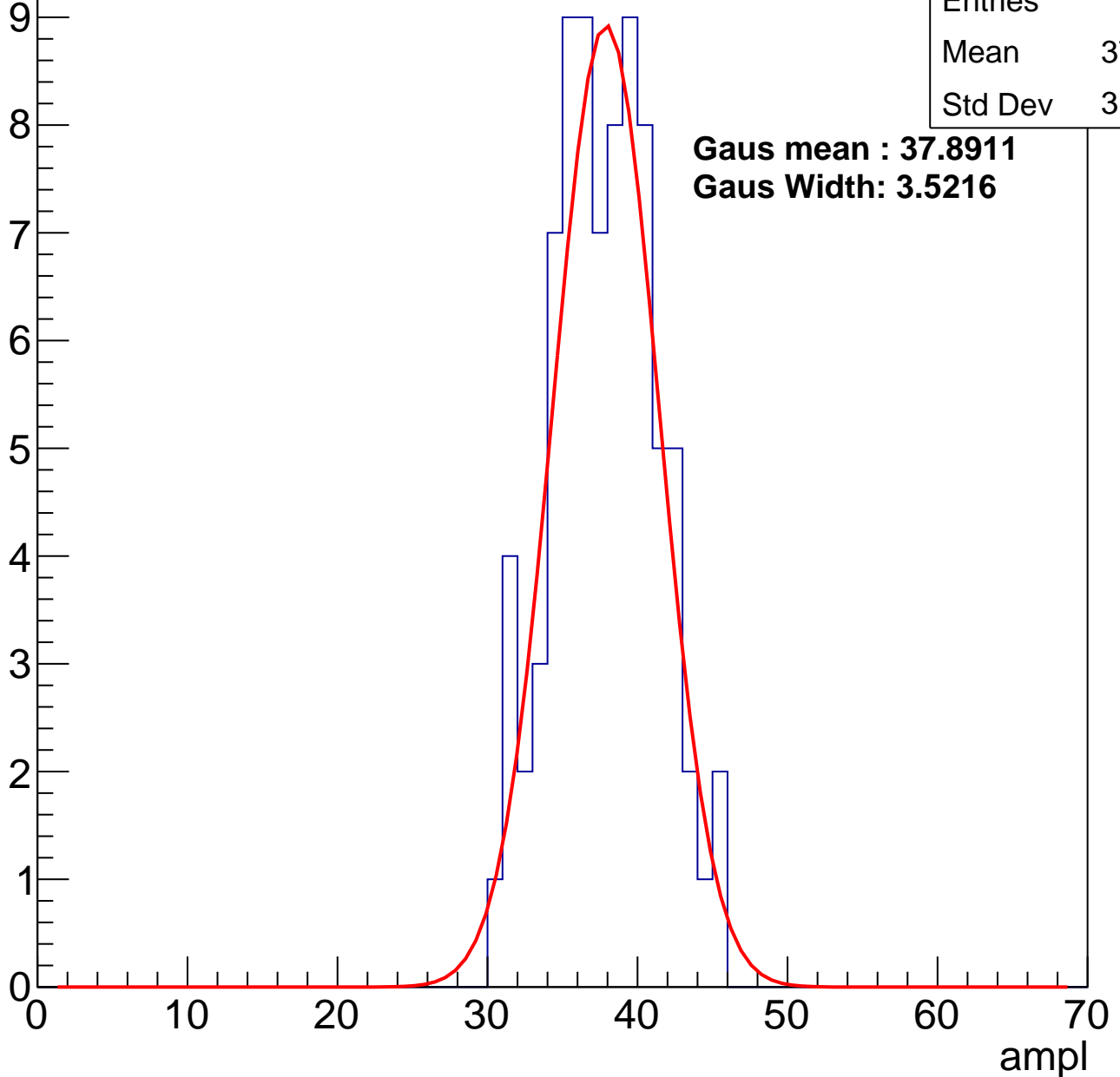
# B1L101S, U18-ch16, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	82
Mean	37.35
Std Dev	3.419

**Gaus mean : 37.8911**  
**Gaus Width: 3.5216**



# B1L101S, U18-ch16, adc2

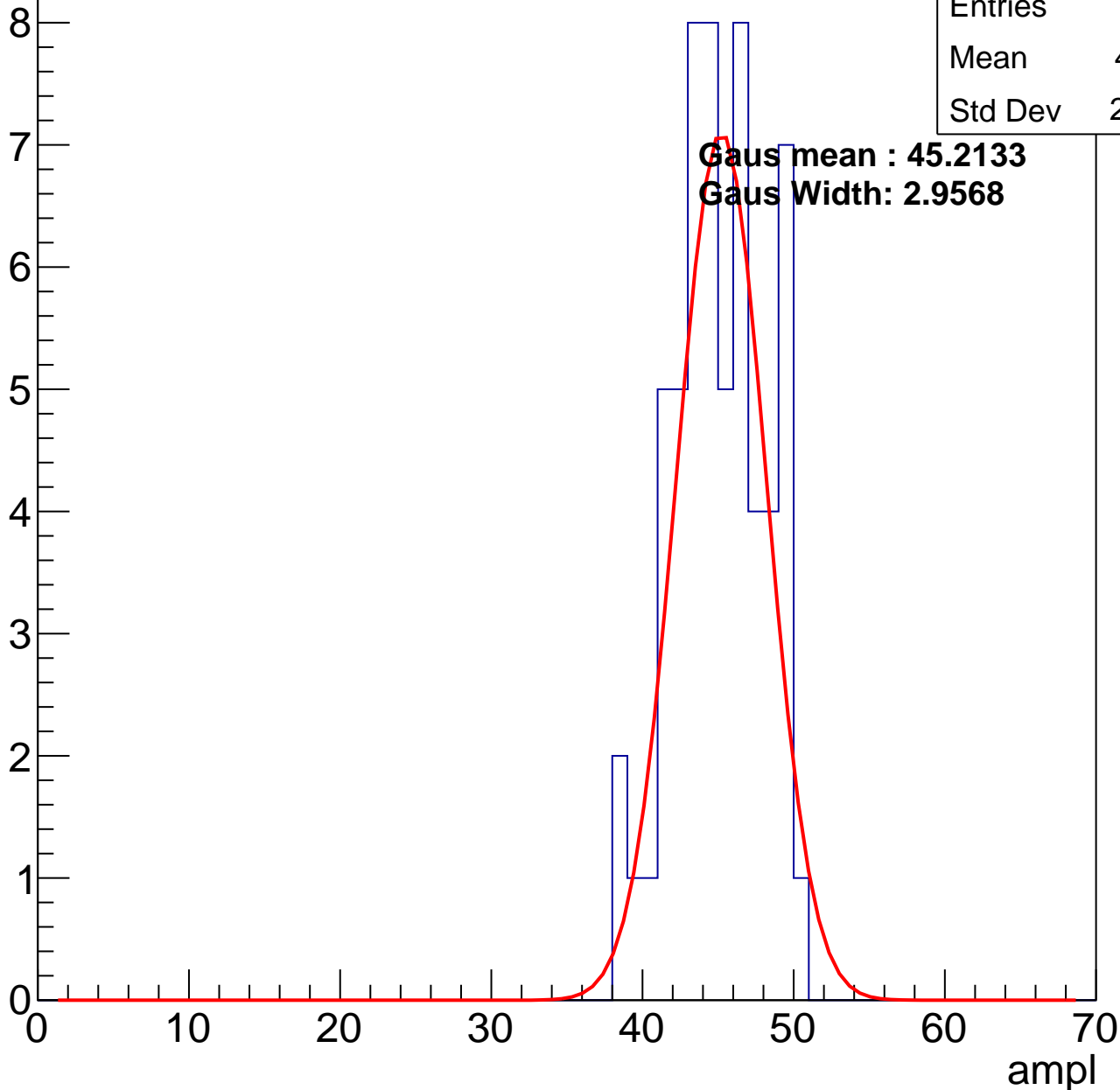
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	44.61
Std Dev	2.946

Gaus mean : 45.2133

Gaus Width: 2.9568

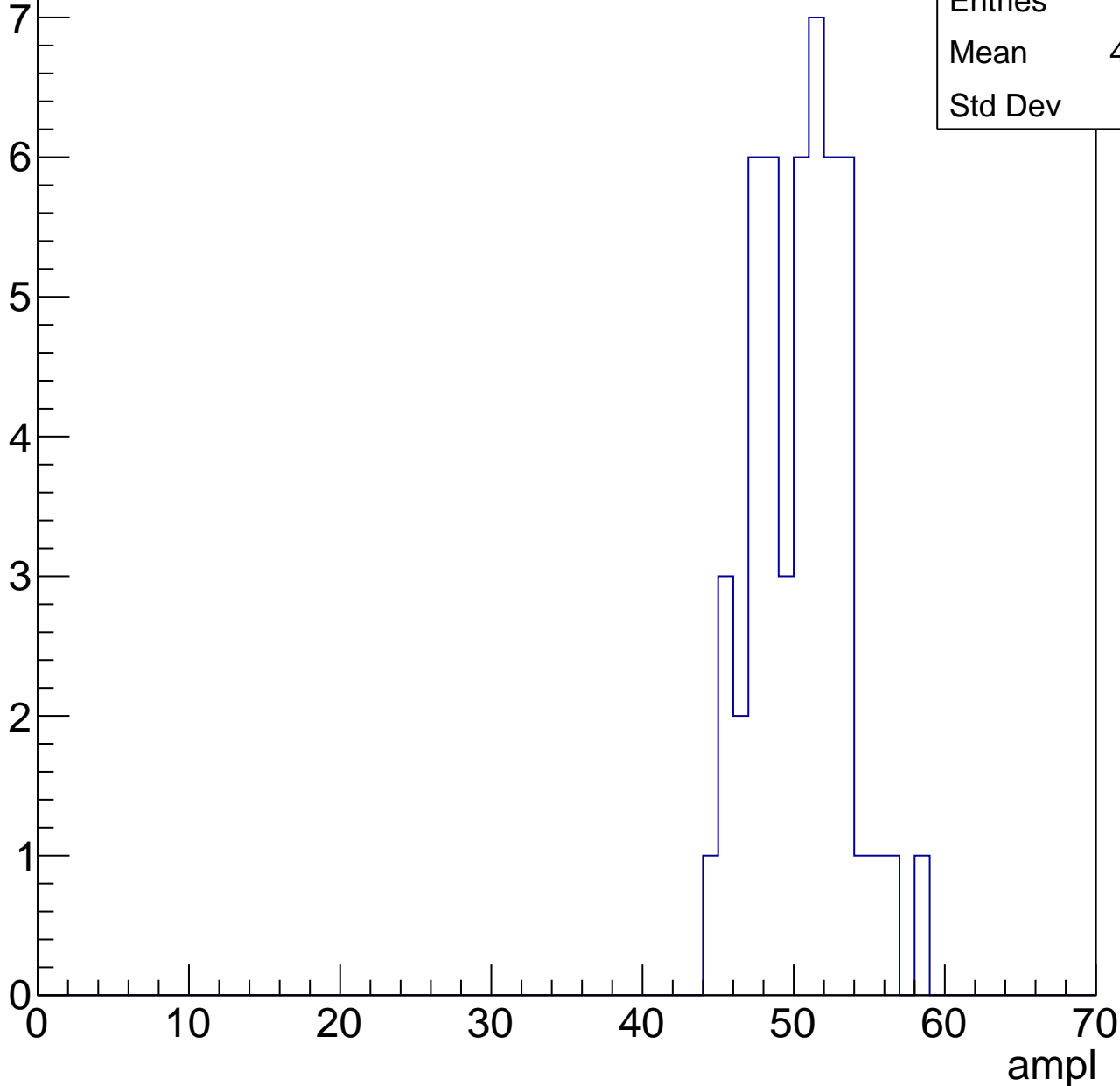


# B1L101S, U18-ch16, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	49.96
Std Dev	3

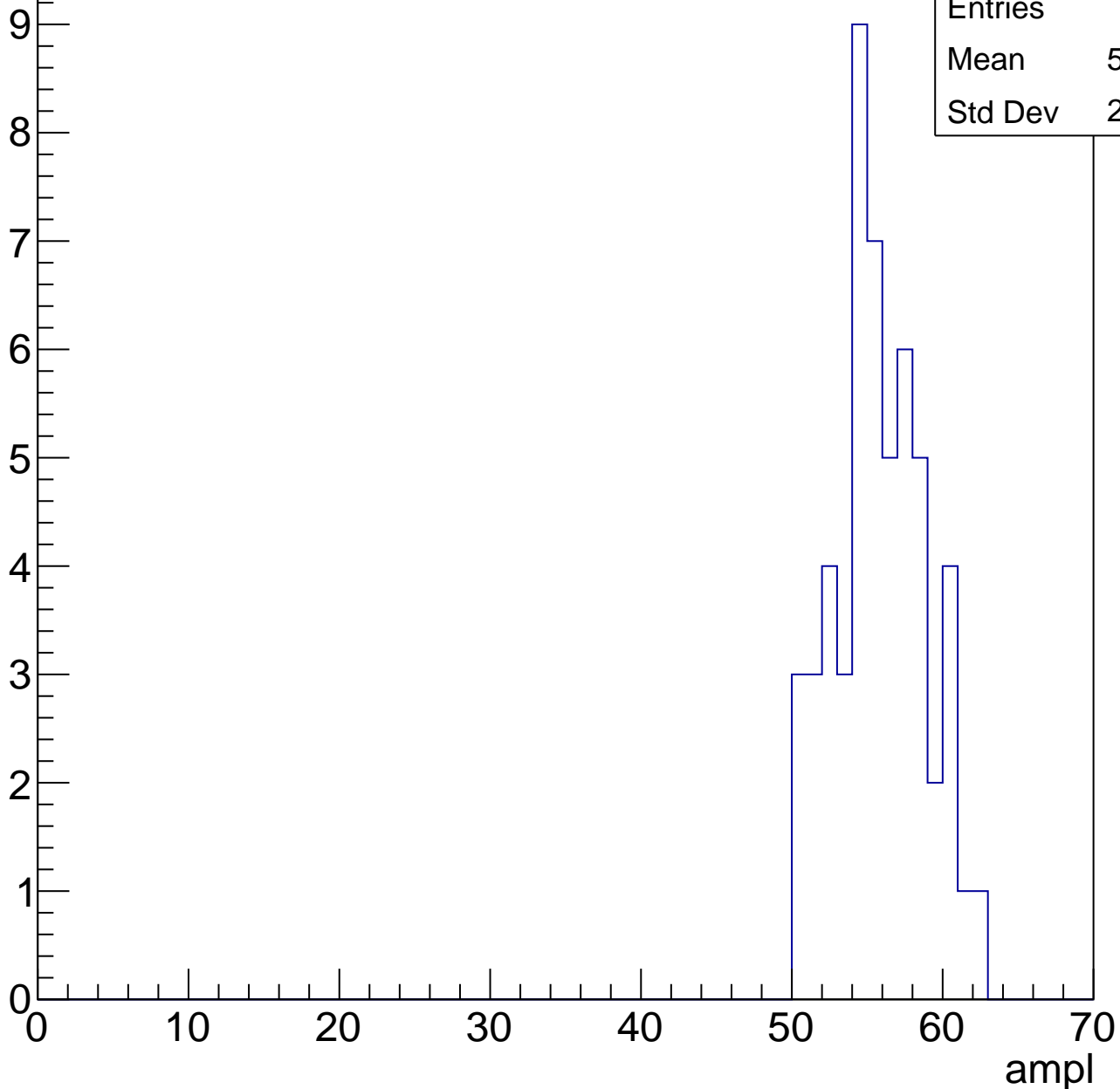


# B1L101S, U18-ch16, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	55.36
Std Dev	2.959



# B1L101S, U18-ch16, adc5

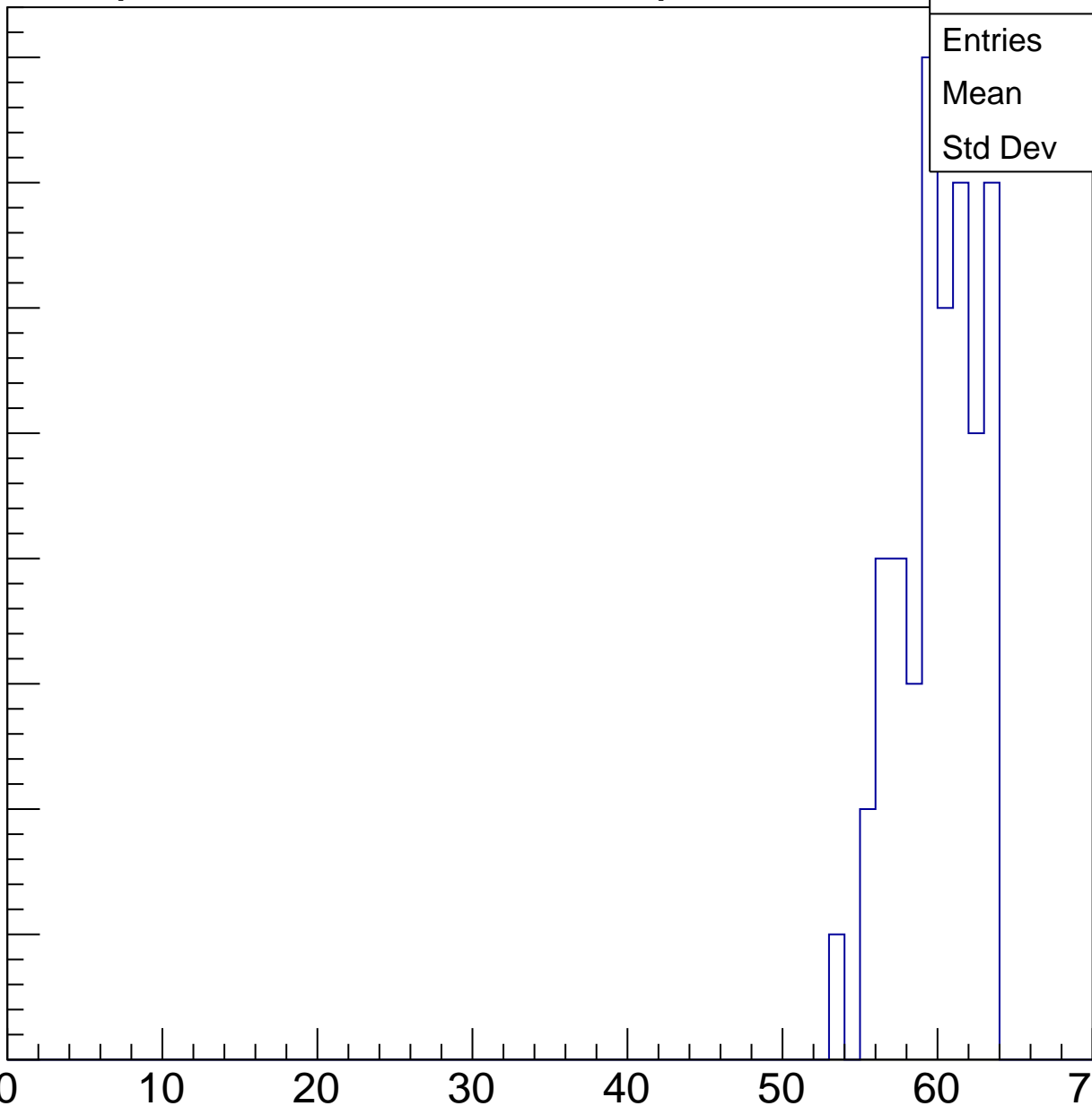
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	47
Mean	59.55
Std Dev	2.525

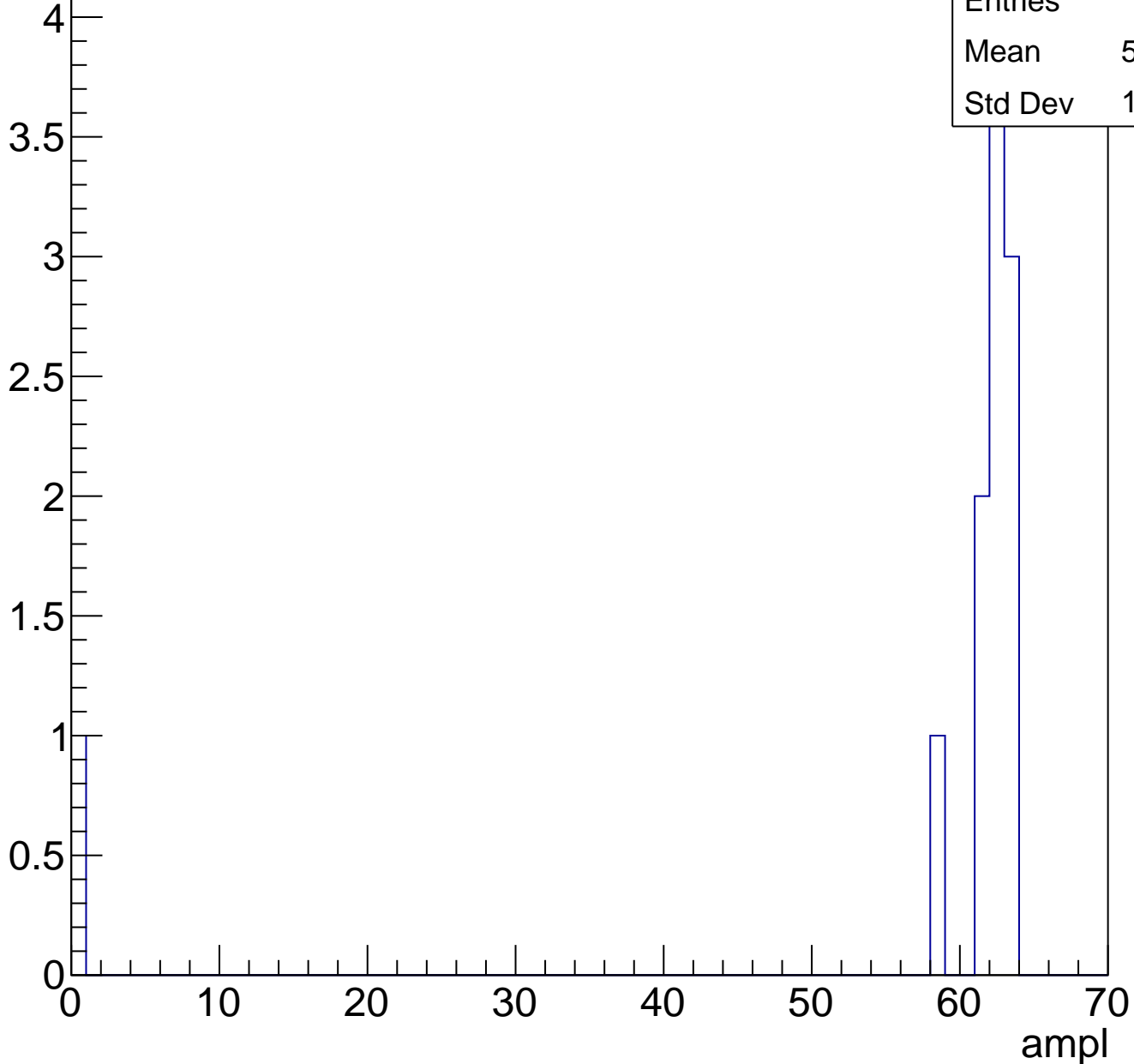
ampl



# B1L101S, U18-ch16, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch16, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch17, adc0

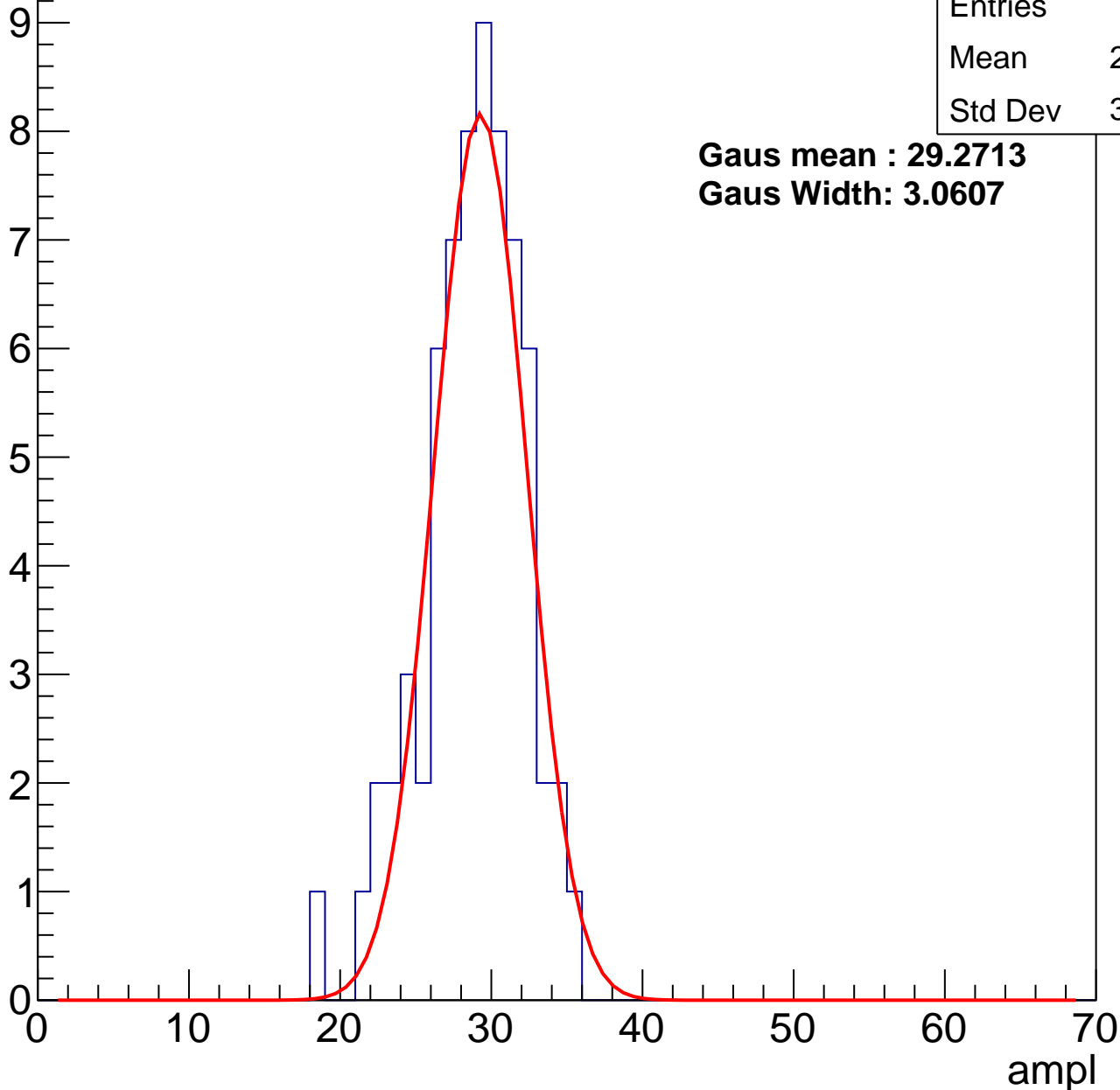
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	28.34
Std Dev	3.303

**Gaus mean : 29.2713**

**Gaus Width: 3.0607**



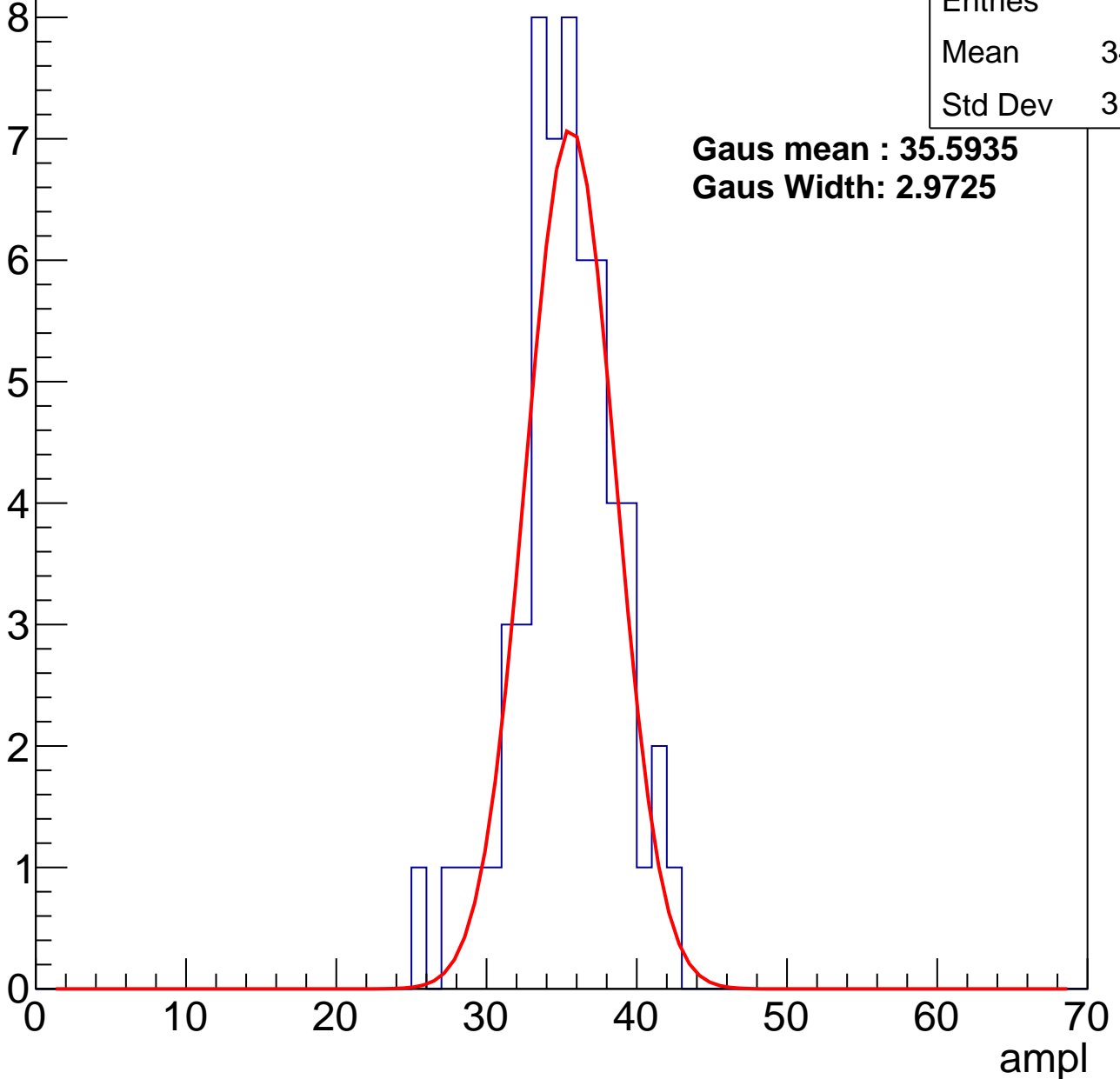
# B1L101S, U18-ch17, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	34.83
Std Dev	3.379

**Gaus mean : 35.5935**  
**Gaus Width: 2.9725**



# B1L101S, U18-ch17, adc2

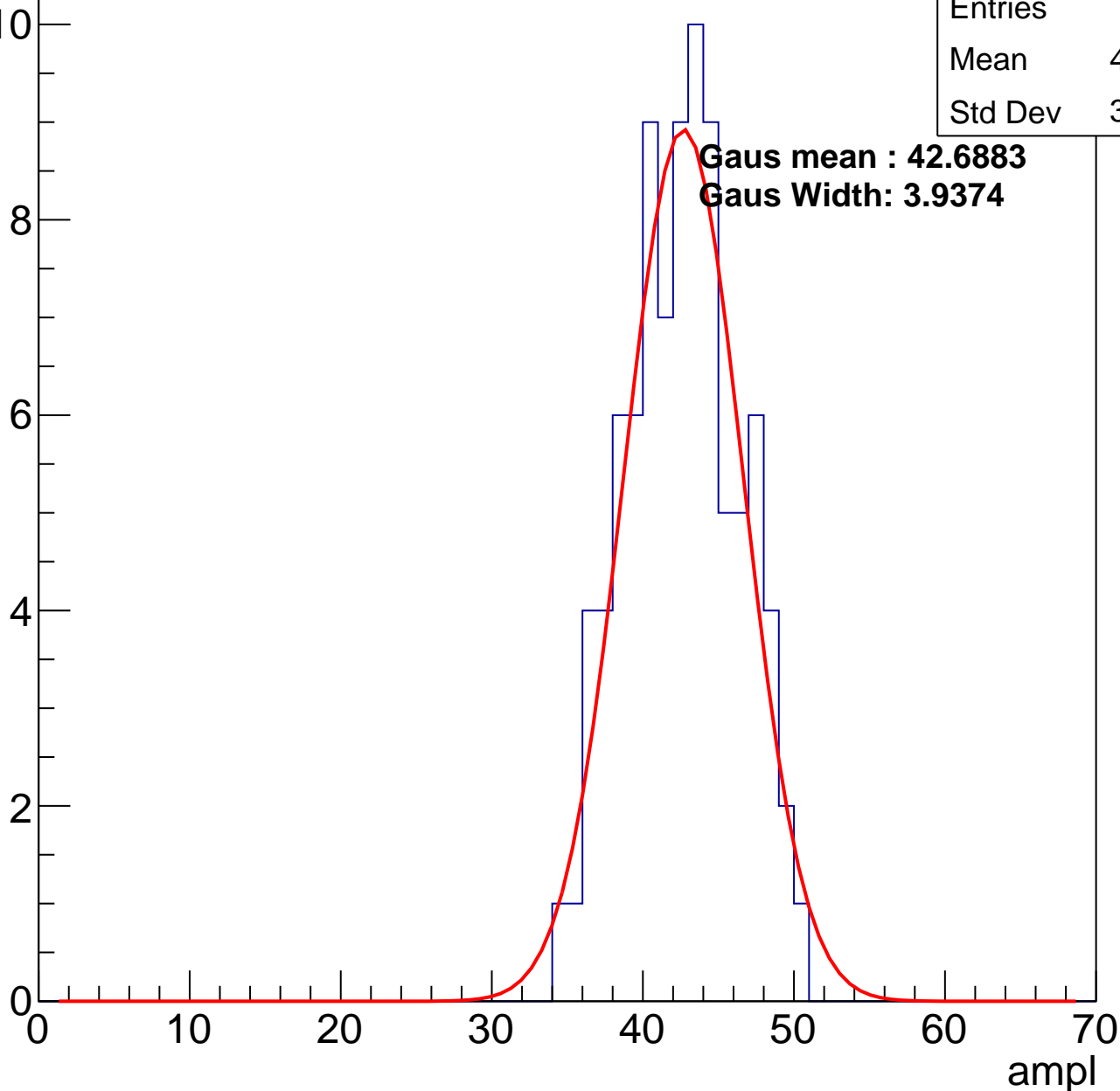
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	89
Mean	42.15
Std Dev	3.634

**Gaus mean : 42.6883**

**Gaus Width: 3.9374**

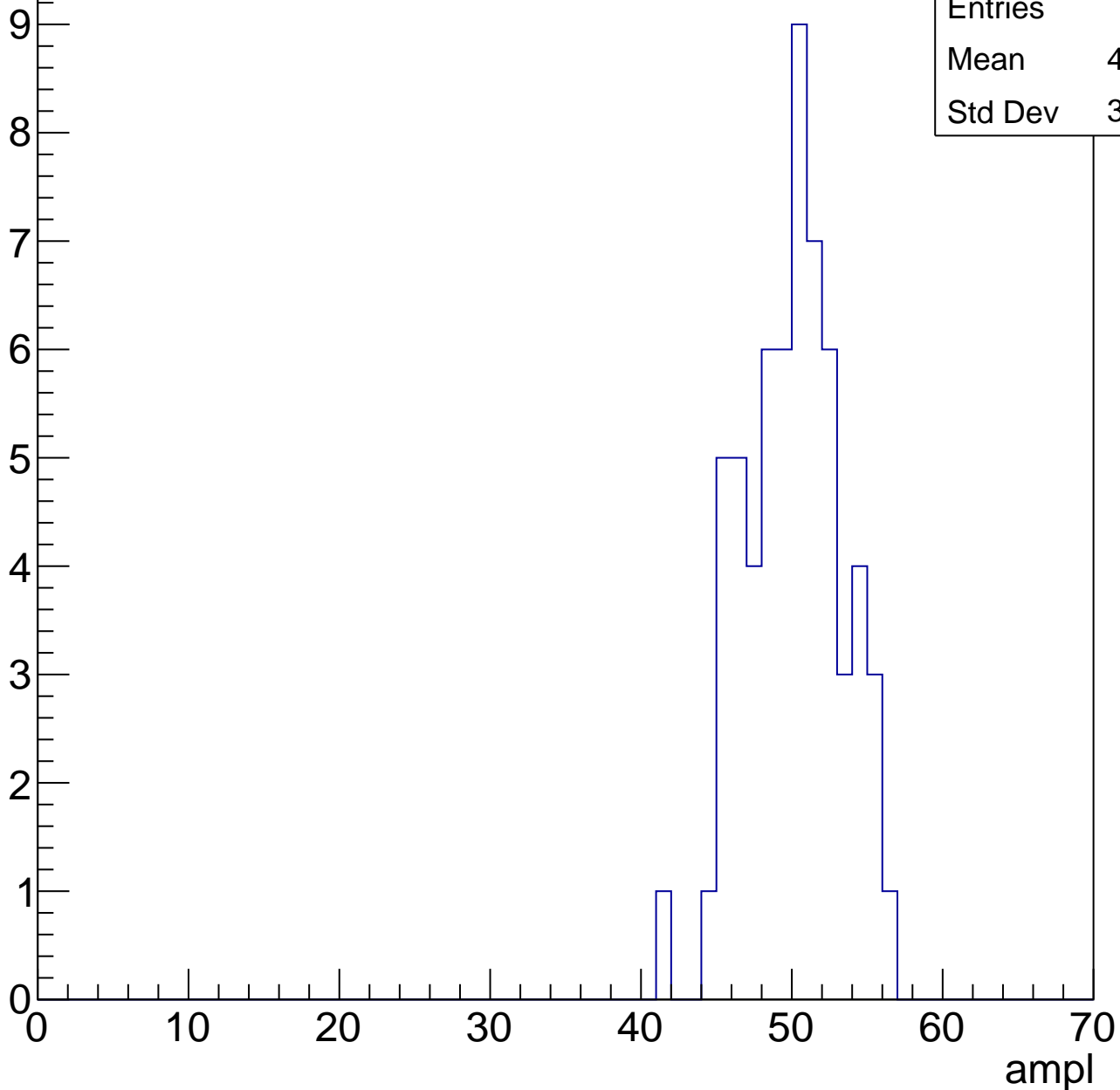


# B1L101S, U18-ch17, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	49.59
Std Dev	3.164



# B1L101S, U18-ch17, adc4

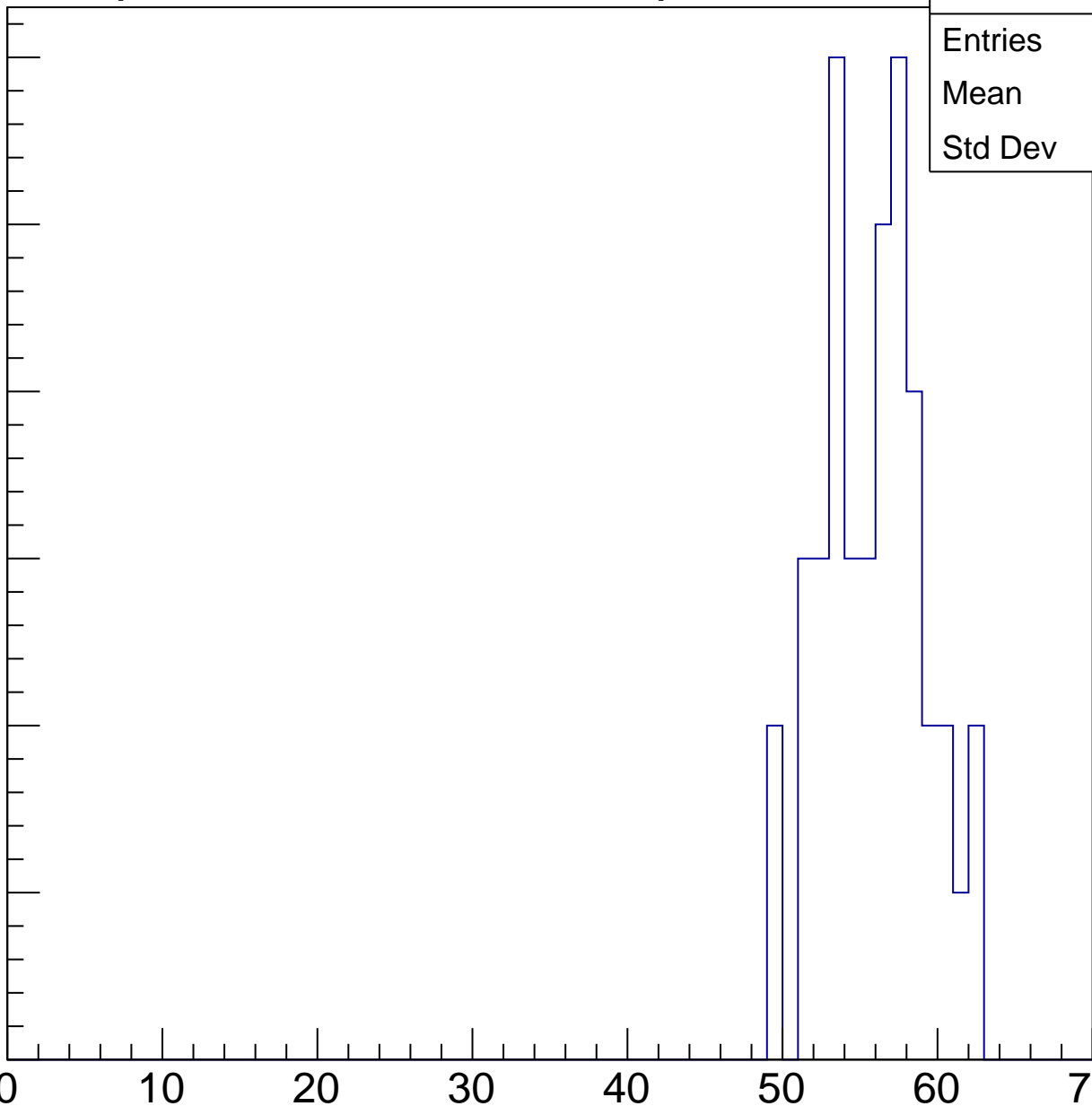
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

6  
5  
4  
3  
2  
1  
0

Entries	42
Mean	55.45
Std Dev	3.26

ampl



# B1L101S, U18-ch17, adc5

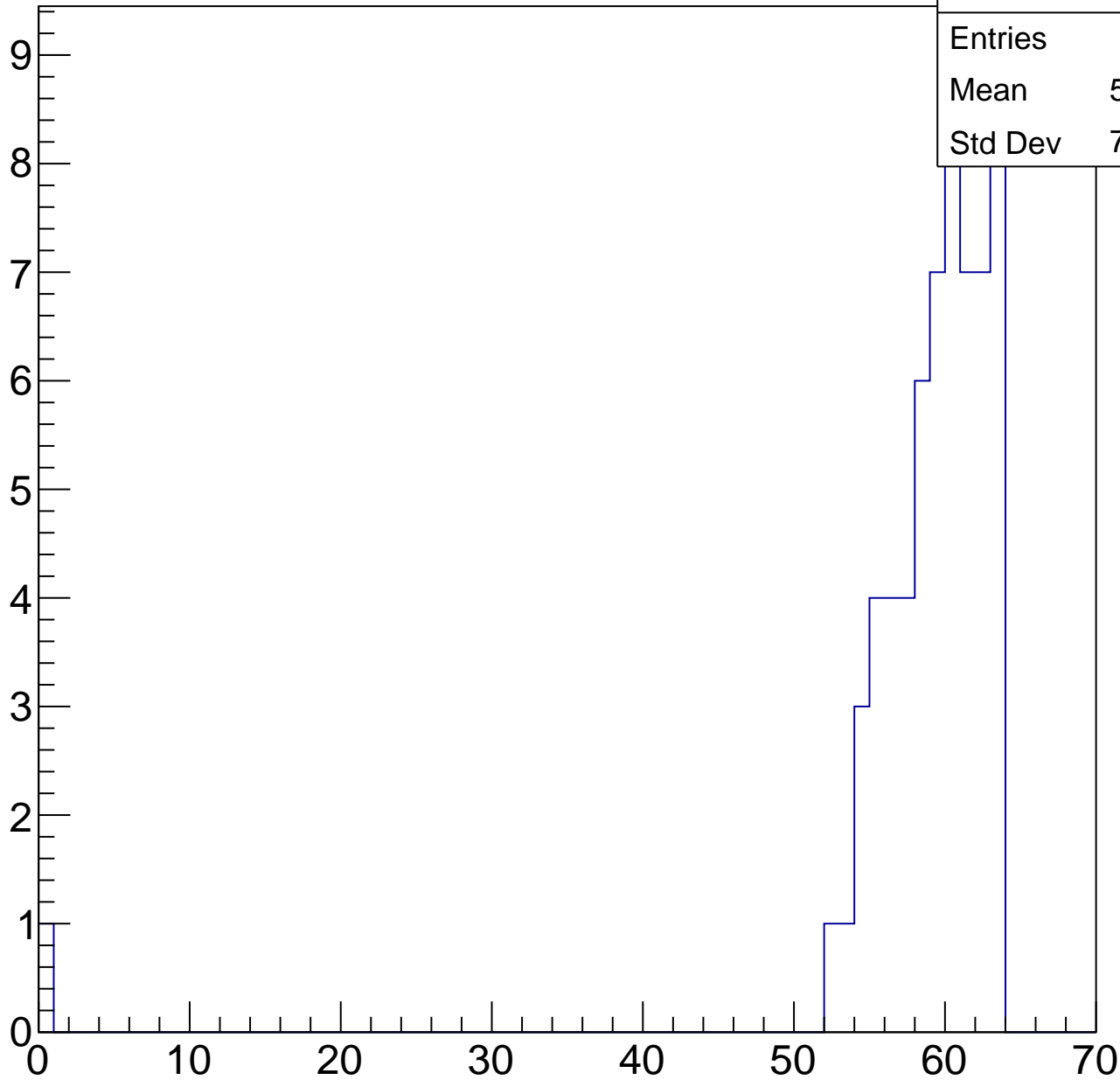
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	62
Mean	58.19
Std Dev	7.998

ampl



# B1L101S, U18-ch17, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

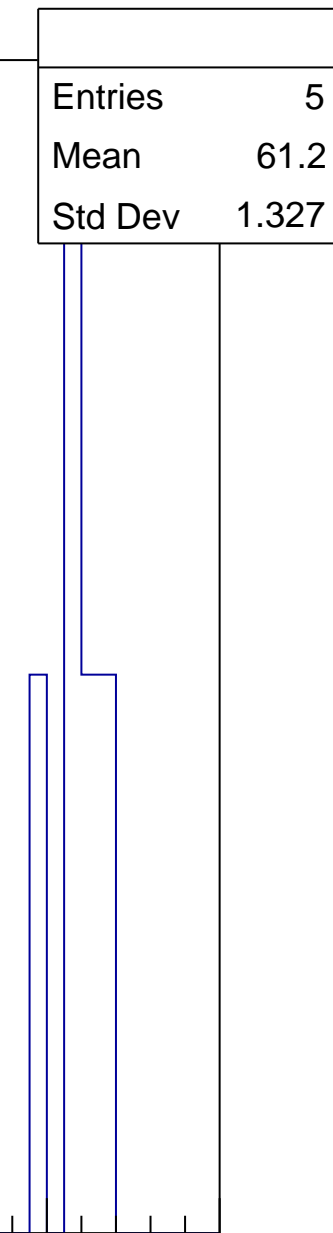
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	61.2
Std Dev	1.327

ampl

0 10 20 30 40 50 60 70





# B1L101S, U18-ch17, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U18-ch18, adc0

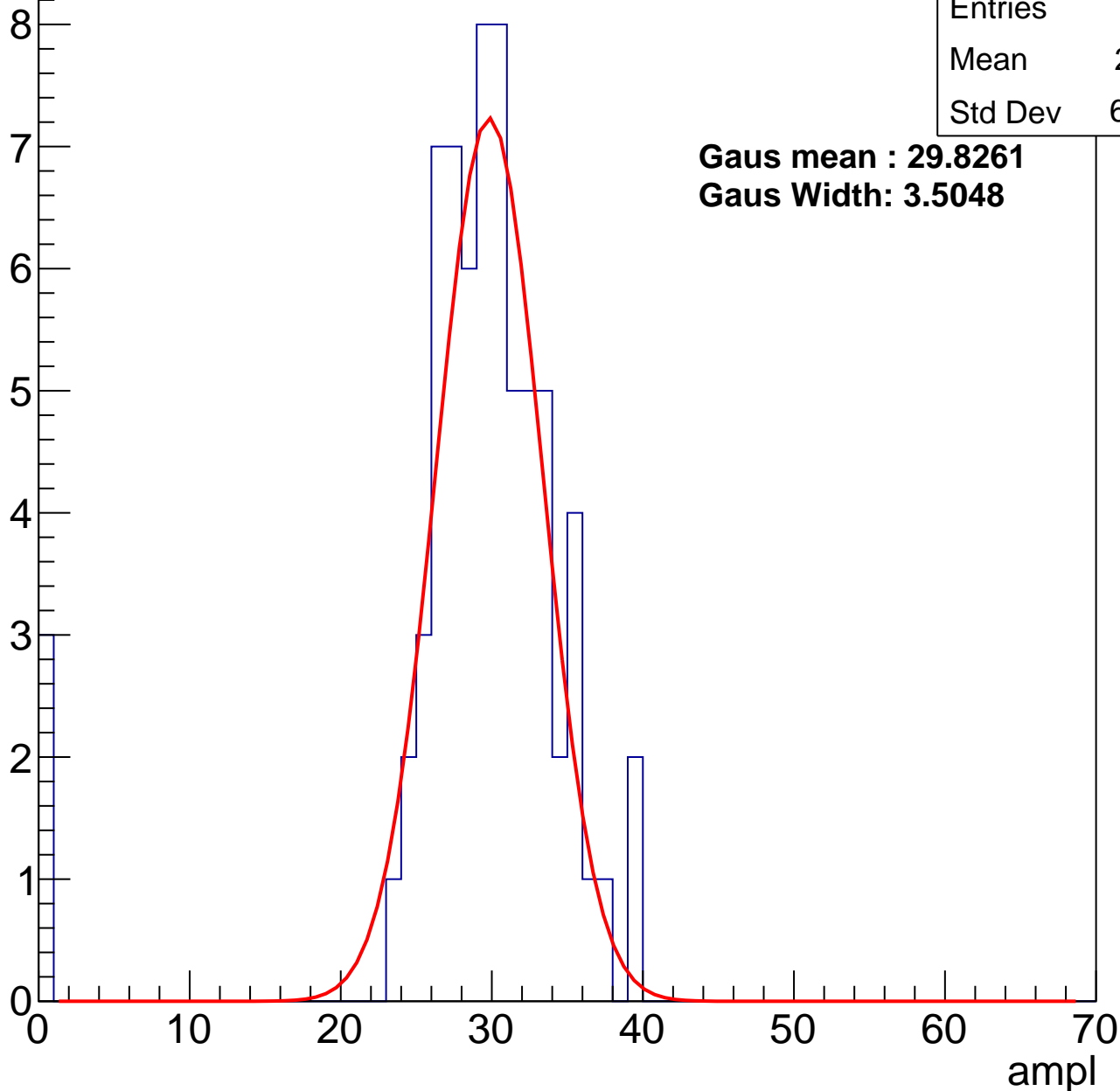
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	28.51
Std Dev	6.967

**Gaus mean : 29.8261**

**Gaus Width: 3.5048**



# B1L101S, U18-ch18, adc1

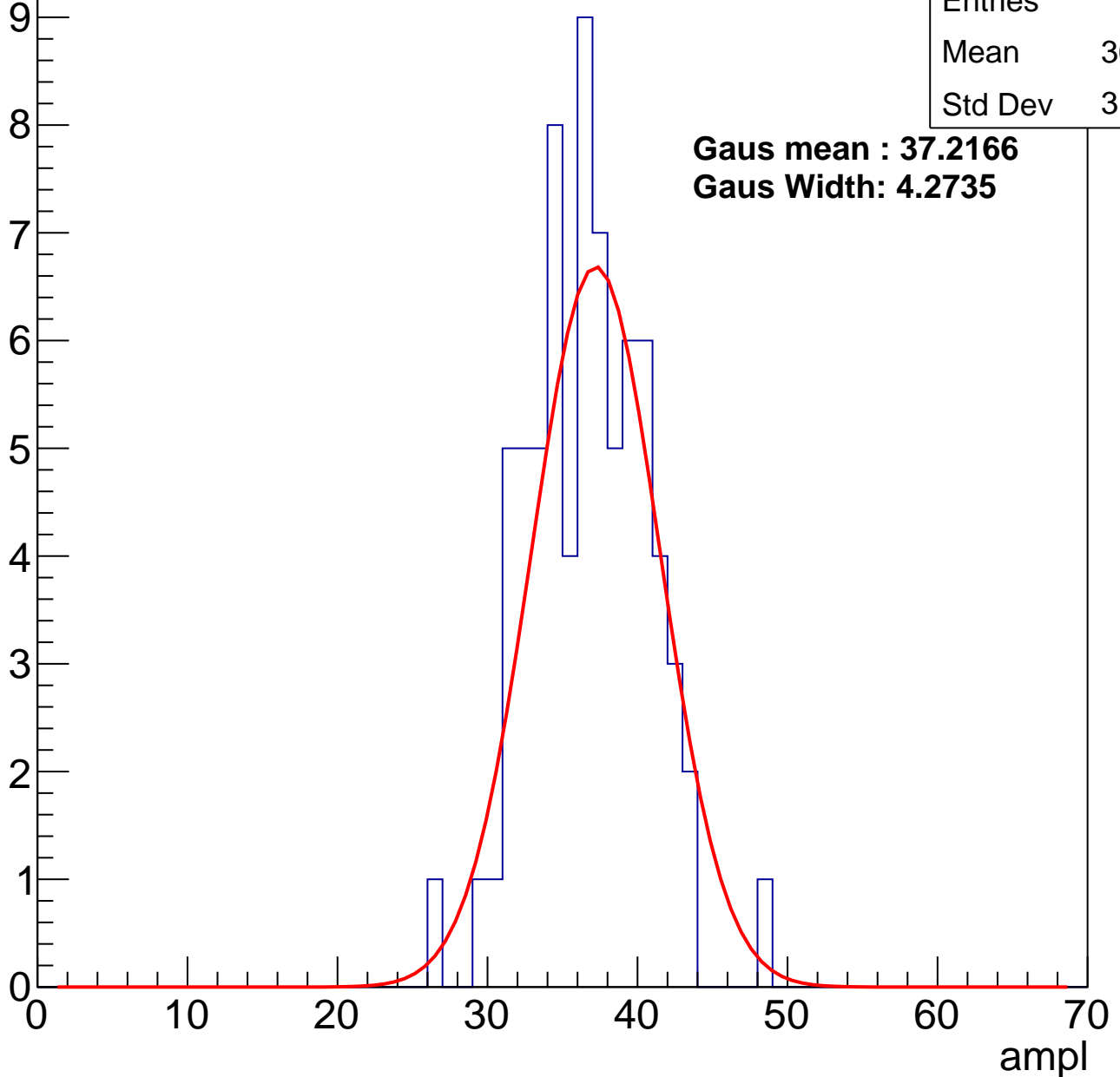
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	36.27
Std Dev	3.869

**Gaus mean : 37.2166**

**Gaus Width: 4.2735**



# B1L101S, U18-ch18, adc2

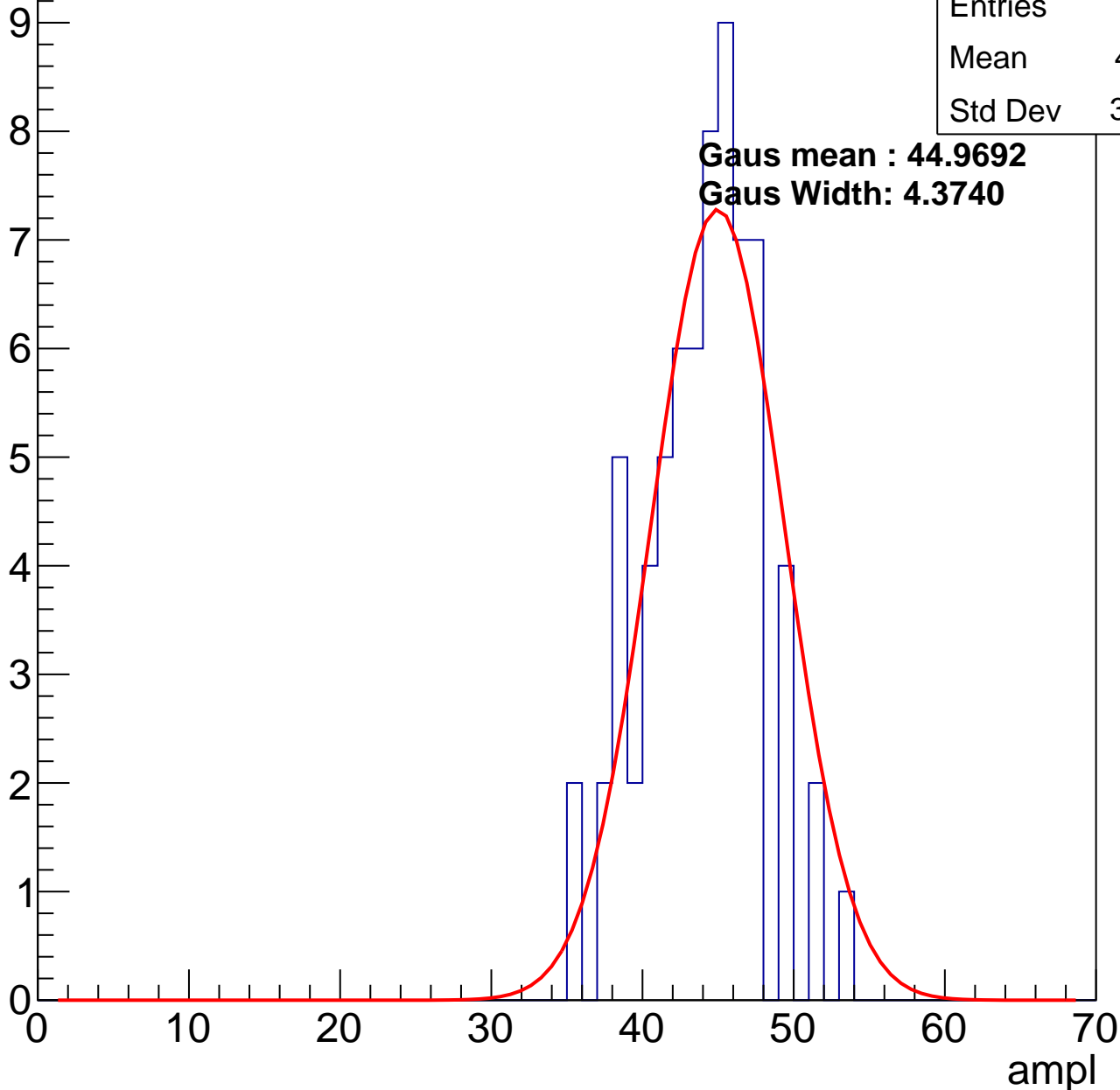
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	43.51
Std Dev	3.764

**Gaus mean : 44.9692**

**Gaus Width: 4.3740**



# B1L101S, U18-ch18, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	62
Mean	49.81
Std Dev	3.473

Entry

10

8

6

4

2

0

0

10

20

30

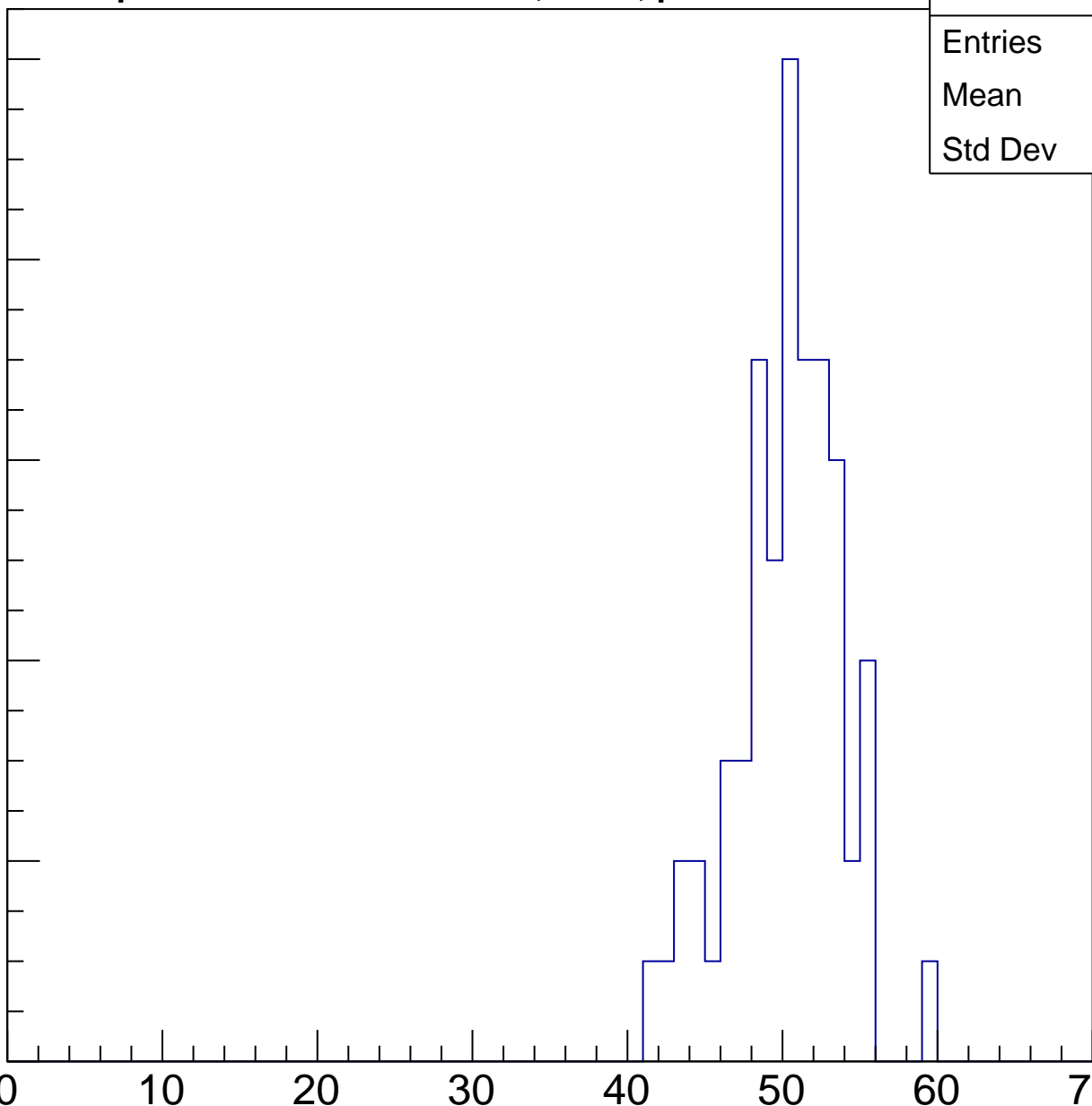
40

50

60

70

ampl



# B1L101S, U18-ch18, adc4

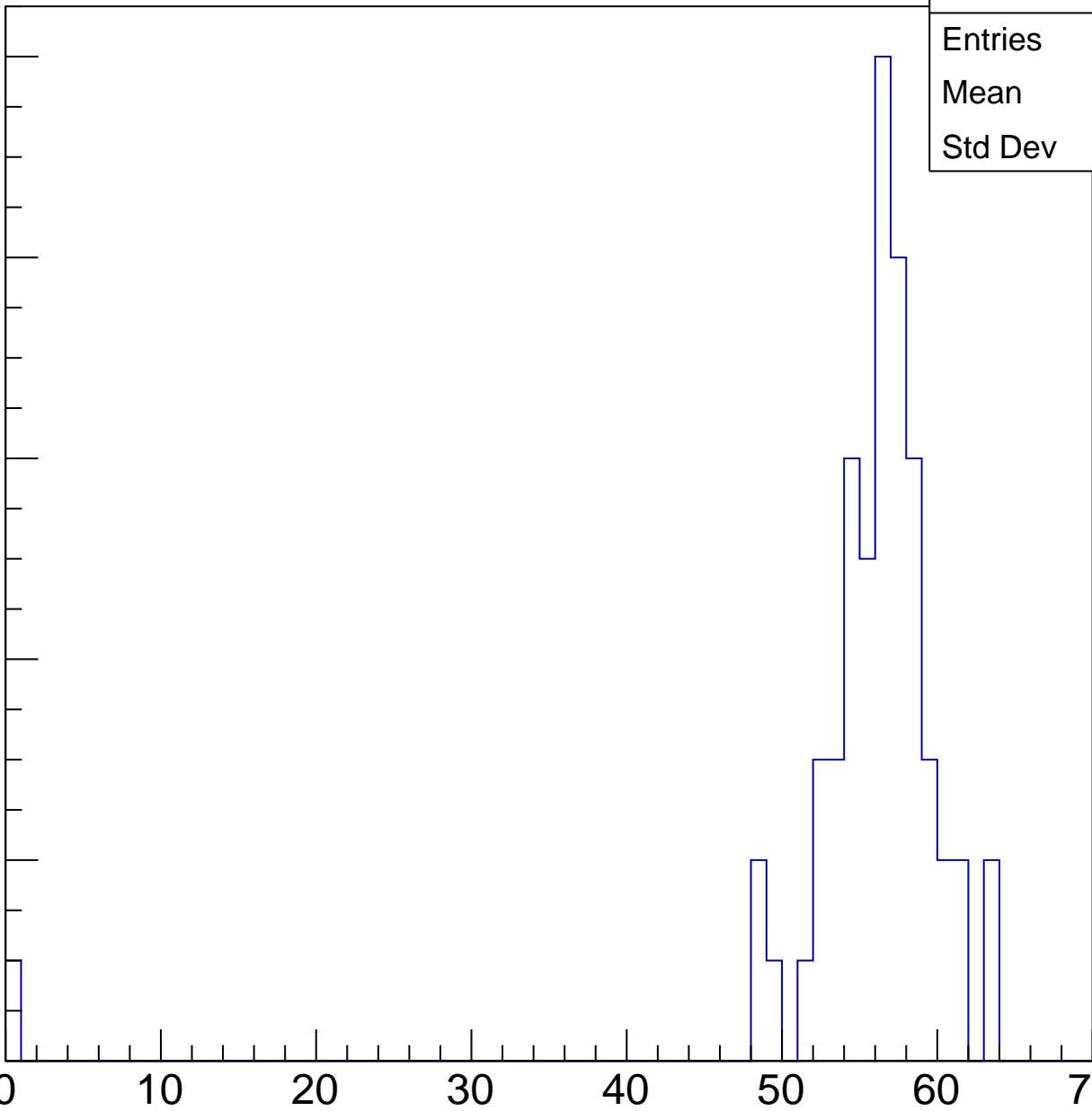
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	55
Mean	54.89
Std Dev	8.105

Entry

10  
8  
6  
4  
2  
0

ampl

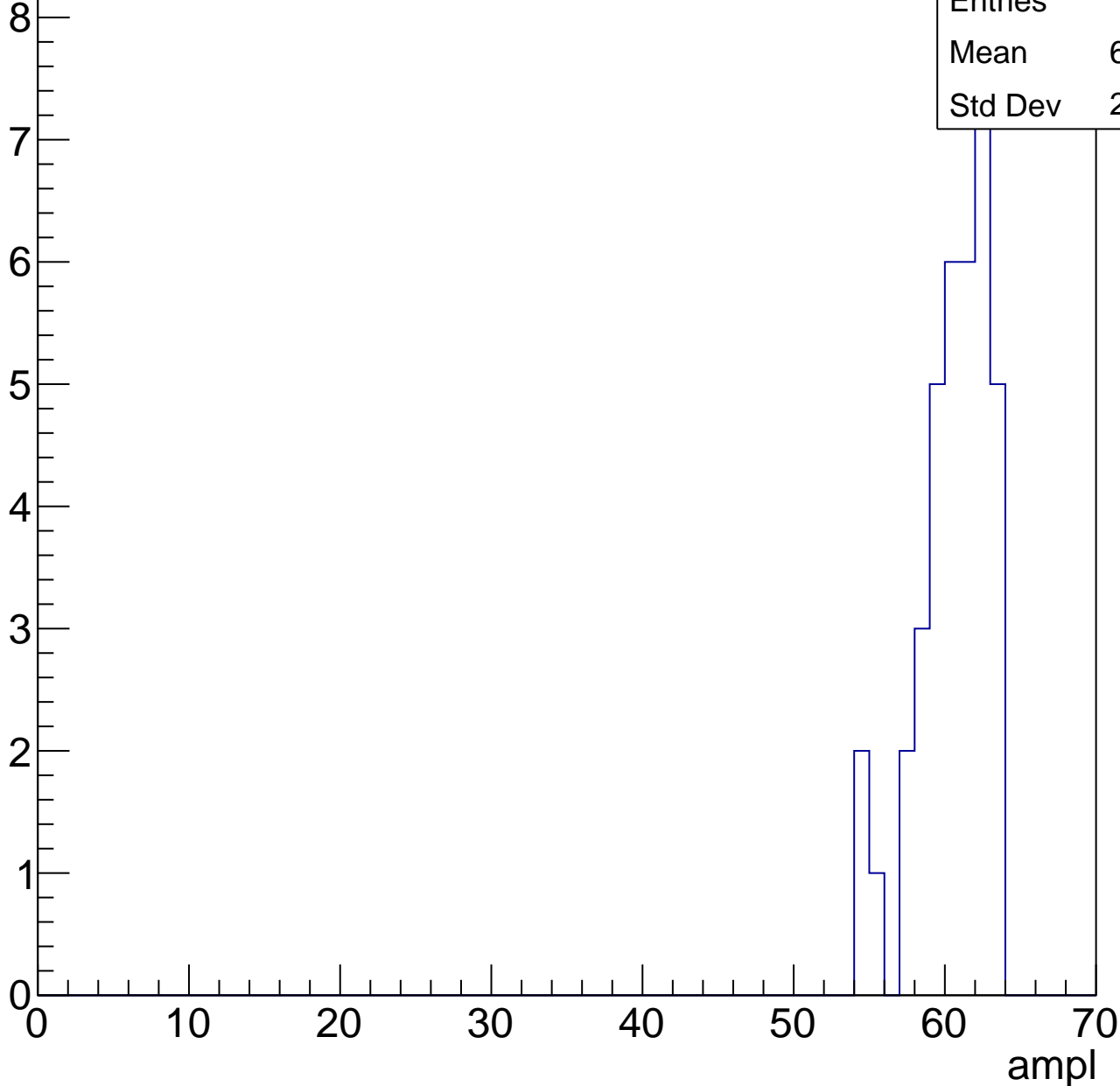


# B1L101S, U18-ch18, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

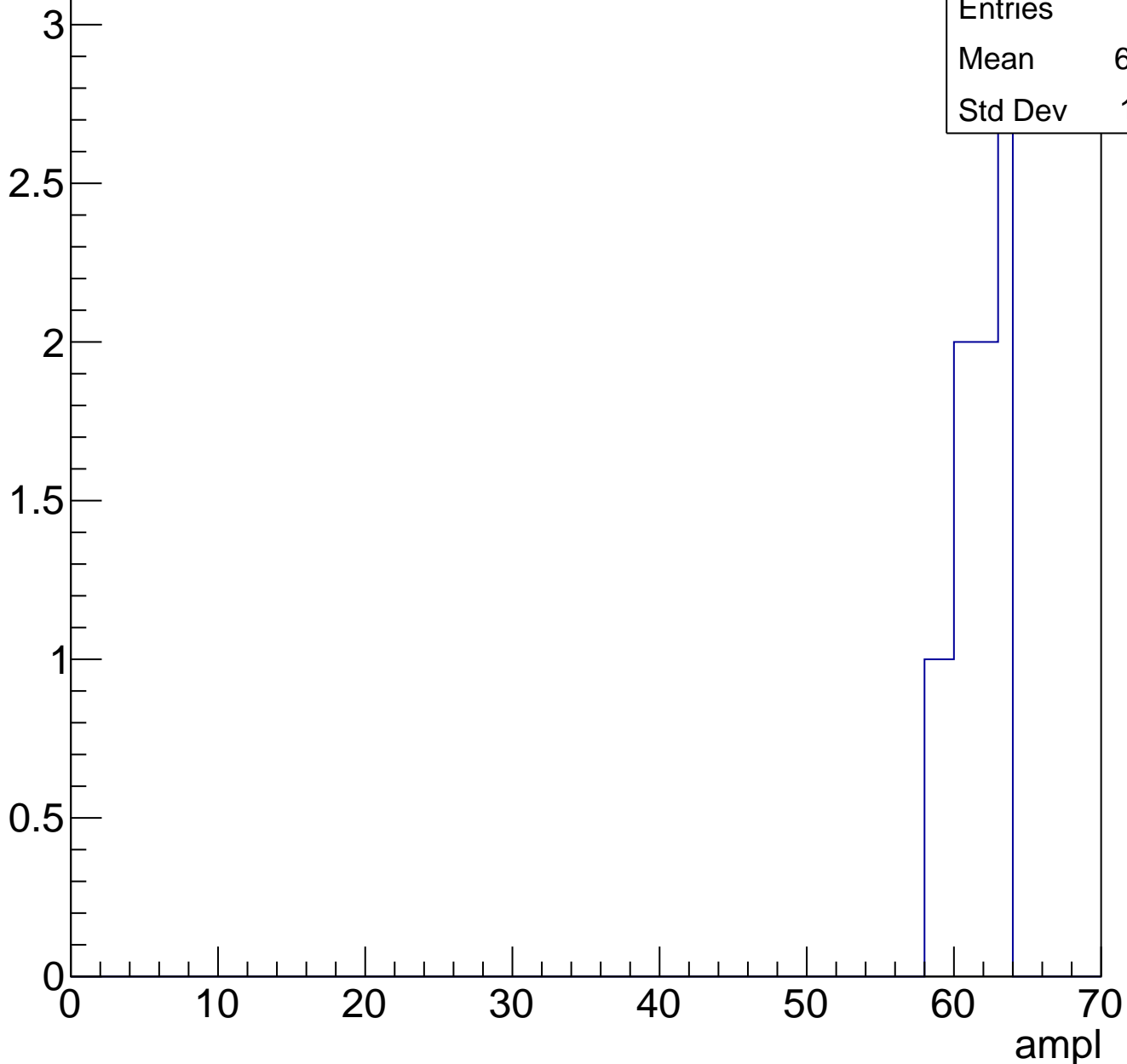
Entries	38
Mean	60.08
Std Dev	2.377



# B1L101S, U18-ch18, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch18, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	7
Std Dev	9.899

# B1L101S, U18-ch19, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	71
Mean	26.46
Std Dev	4.657

**Gaus mean : 27.6783**

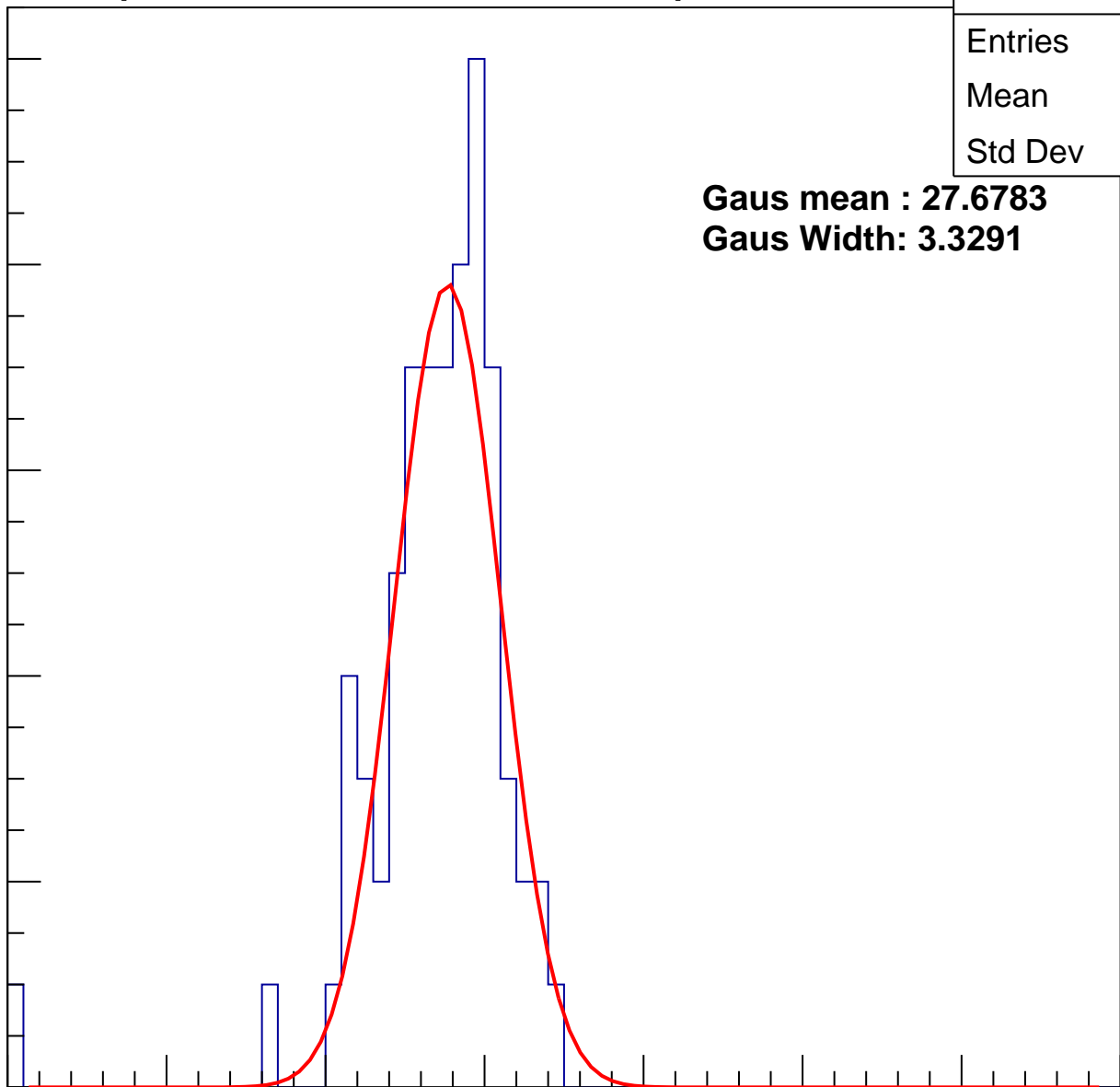
**Gaus Width: 3.3291**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U18-ch19, adc1

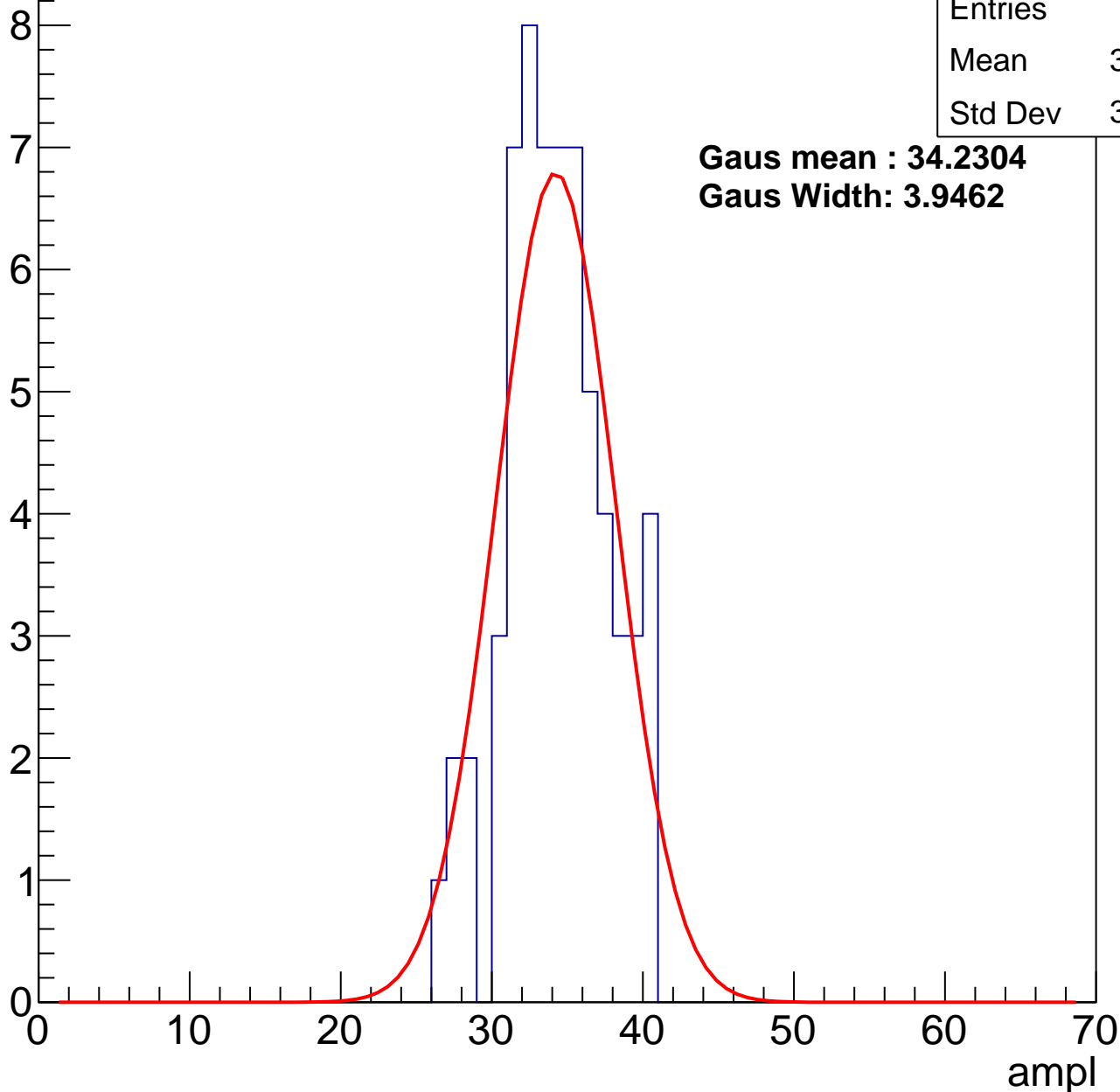
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	33.84
Std Dev	3.363

**Gaus mean : 34.2304**

**Gaus Width: 3.9462**



# B1L101S, U18-ch19, adc2

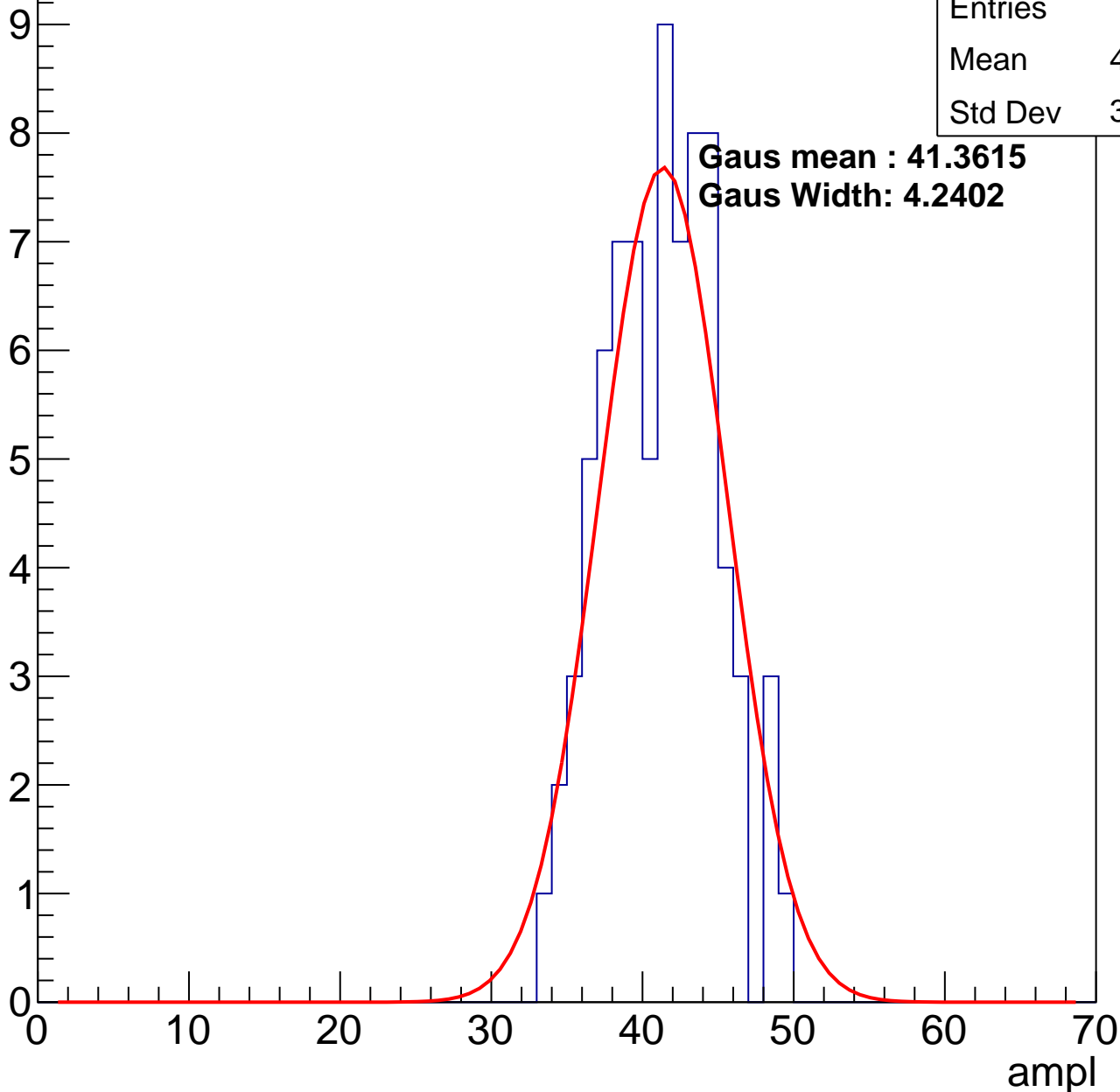
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	79
Mean	40.72
Std Dev	3.632

**Gaus mean : 41.3615**

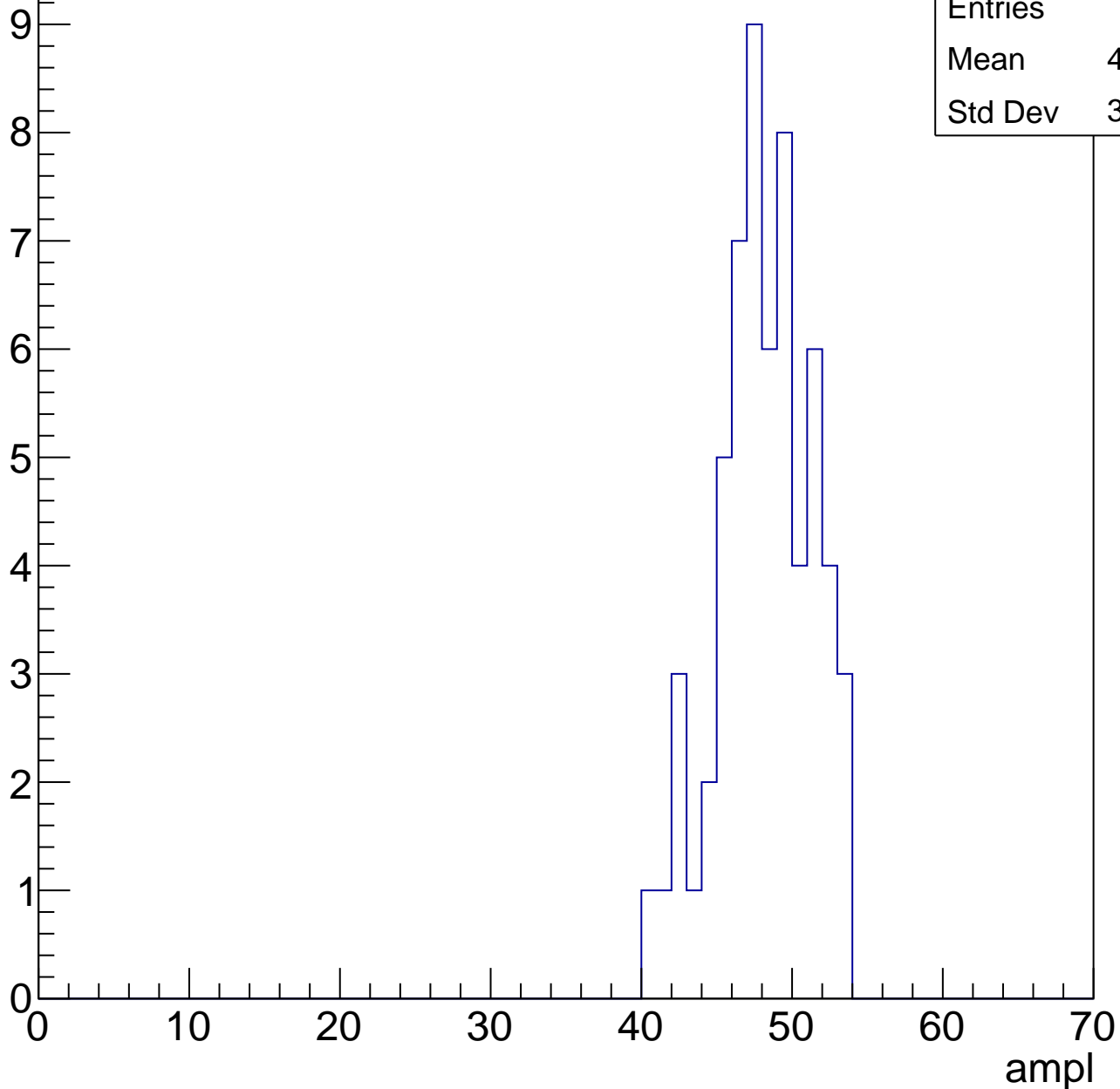
**Gaus Width: 4.2402**



# B1L101S, U18-ch19, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



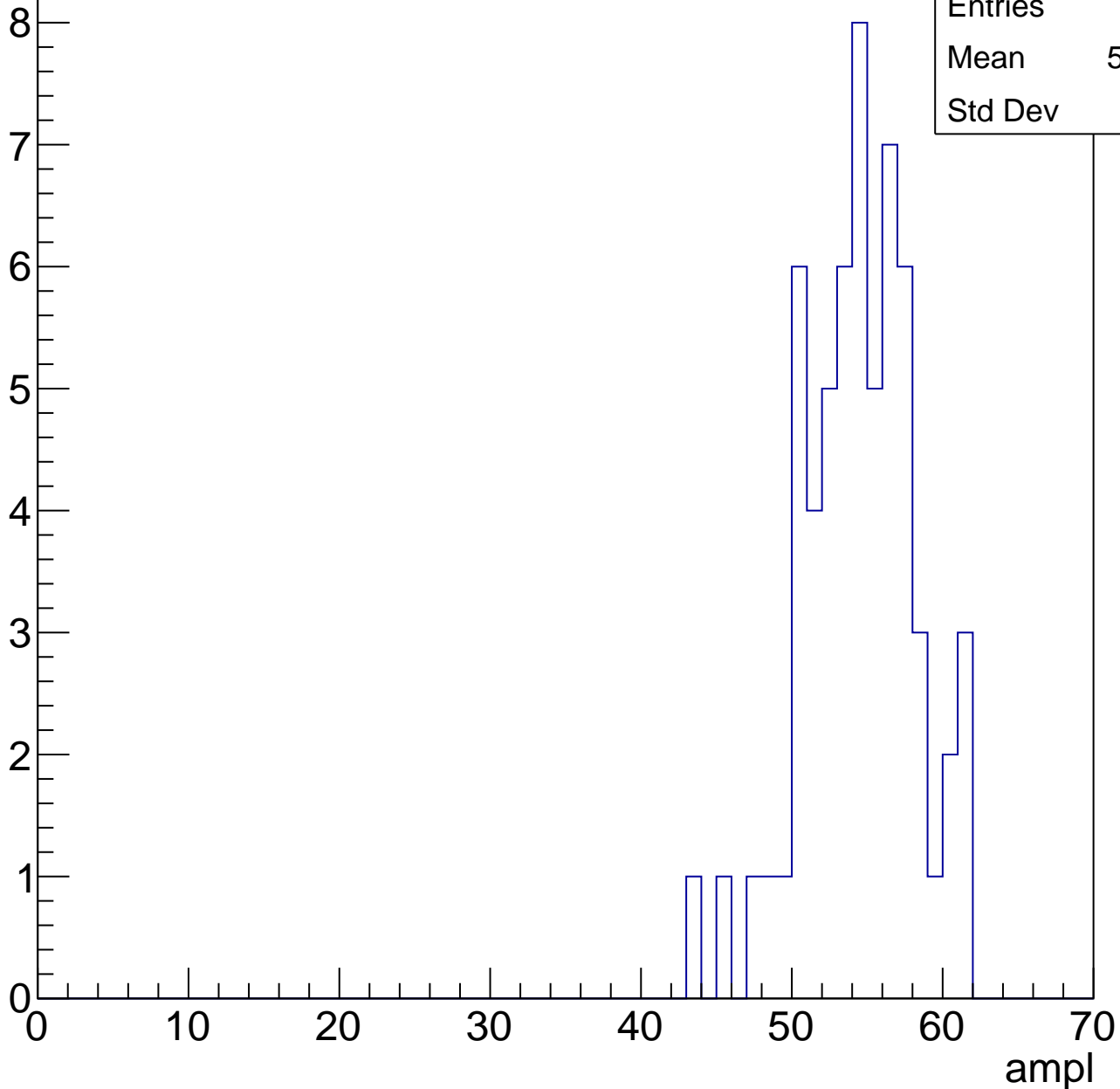
Entries	60
Mean	47.68
Std Dev	3.085

# B1L101S, U18-ch19, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

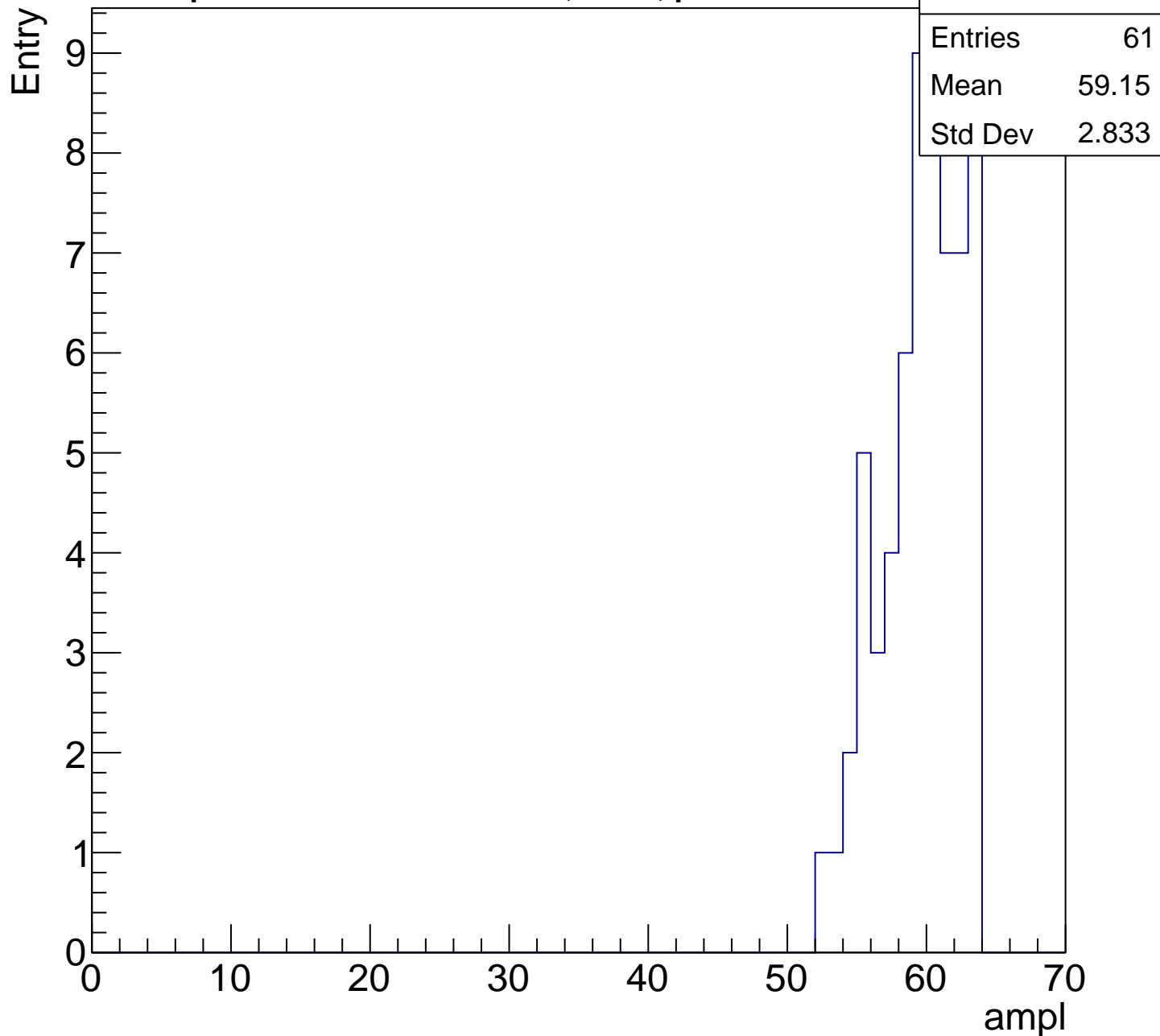
Entry

Entries	61
Mean	53.95
Std Dev	3.73



# B1L101S, U18-ch19, adc5

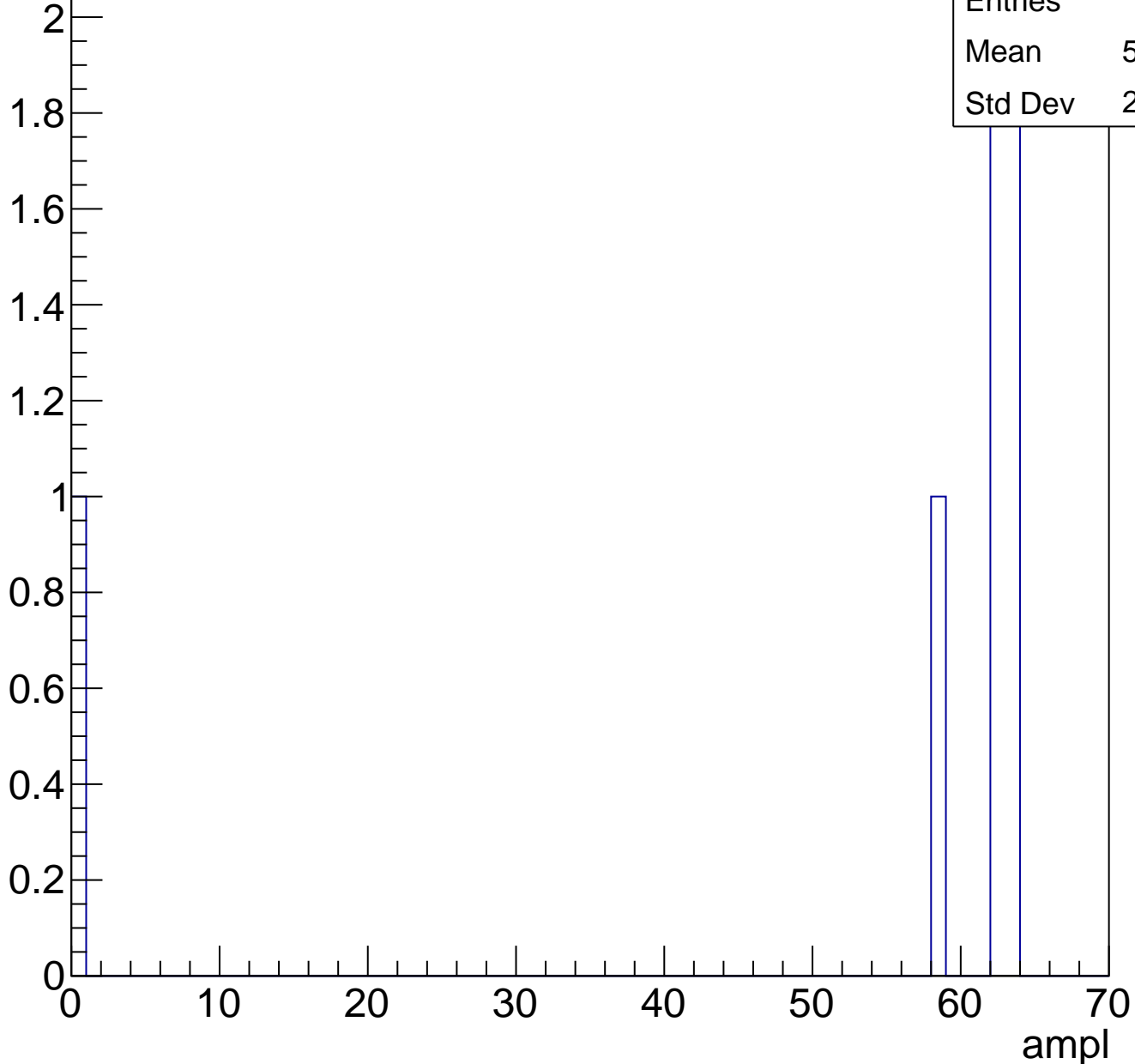
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U18-ch19, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



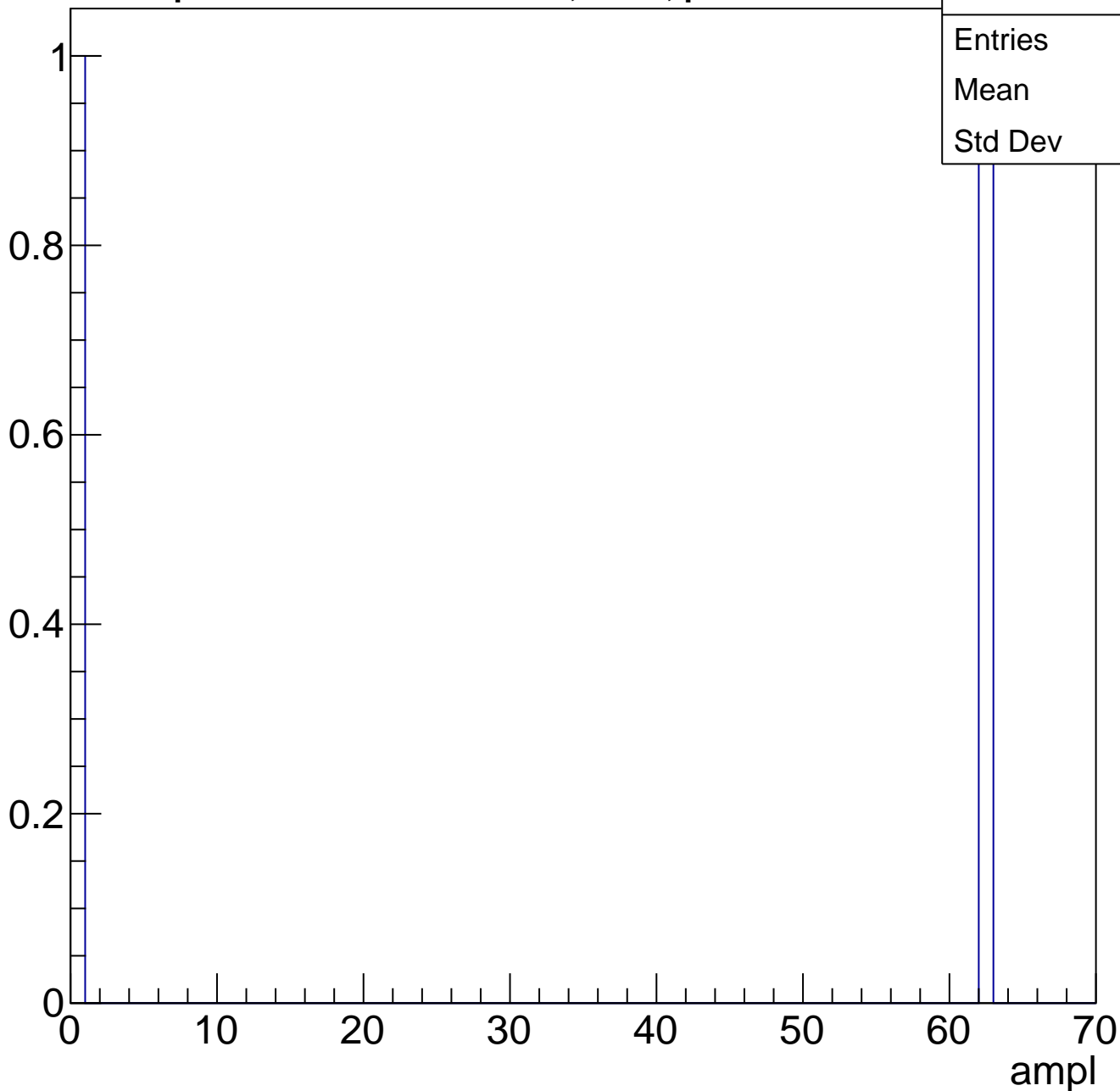
Entries	6
Mean	51.33
Std Dev	23.02



# B1L101S, U18-ch19, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch20, adc0

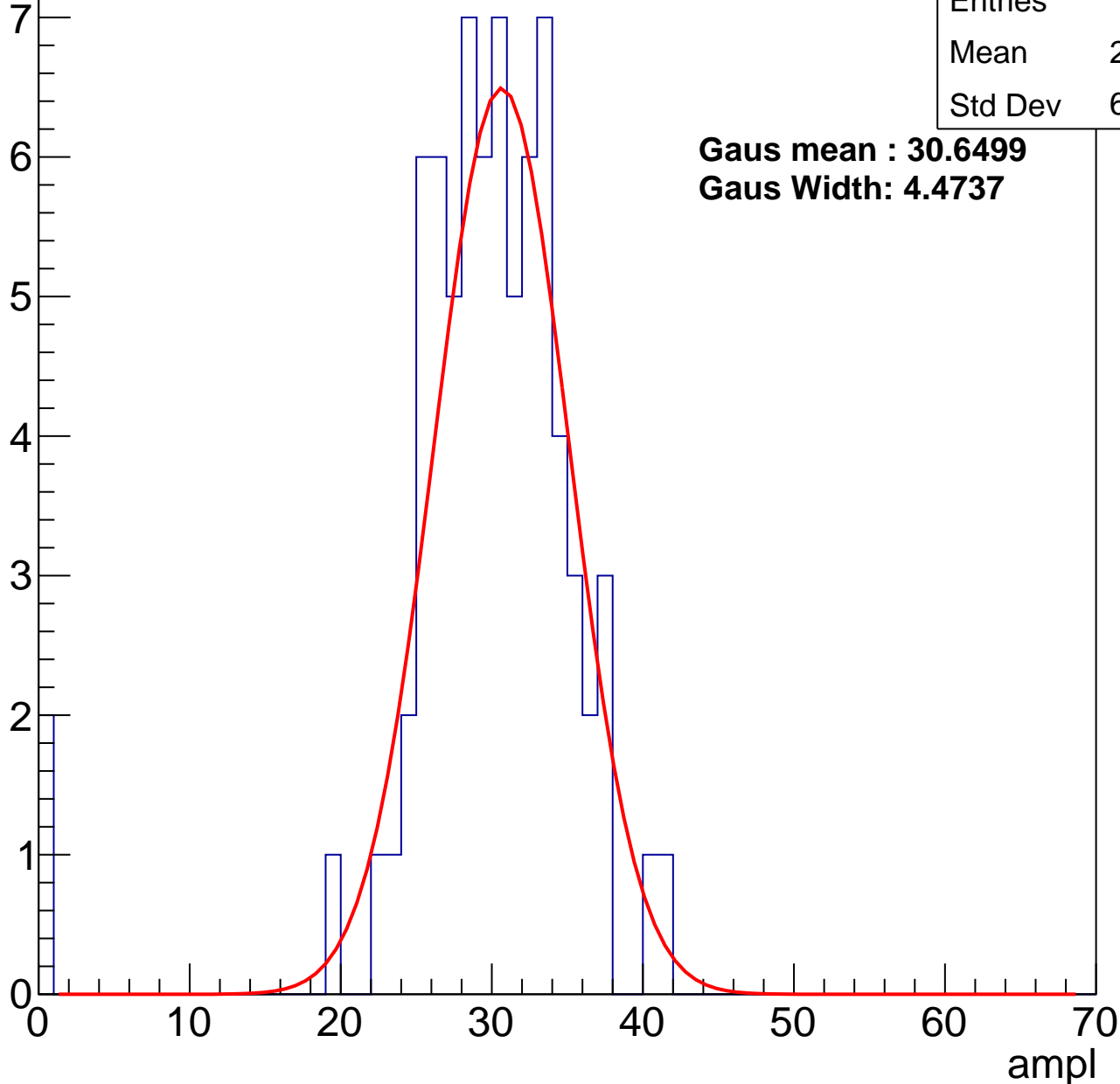
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	29.16
Std Dev	6.333

**Gaus mean : 30.6499**

**Gaus Width: 4.4737**



# B1L101S, U18-ch20, adc1

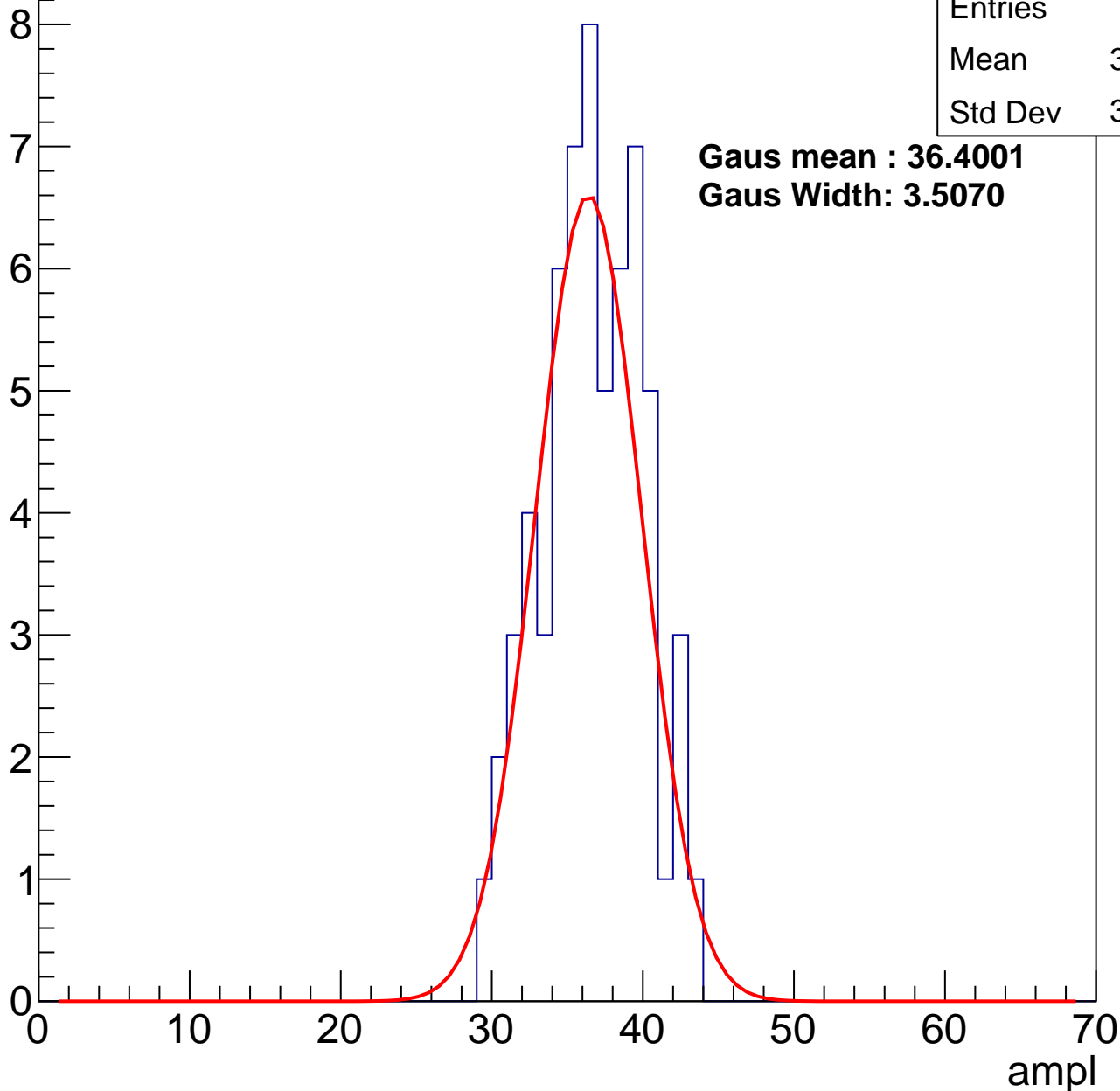
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	36.16
Std Dev	3.288

**Gaus mean : 36.4001**

**Gaus Width: 3.5070**



# B1L101S, U18-ch20, adc2

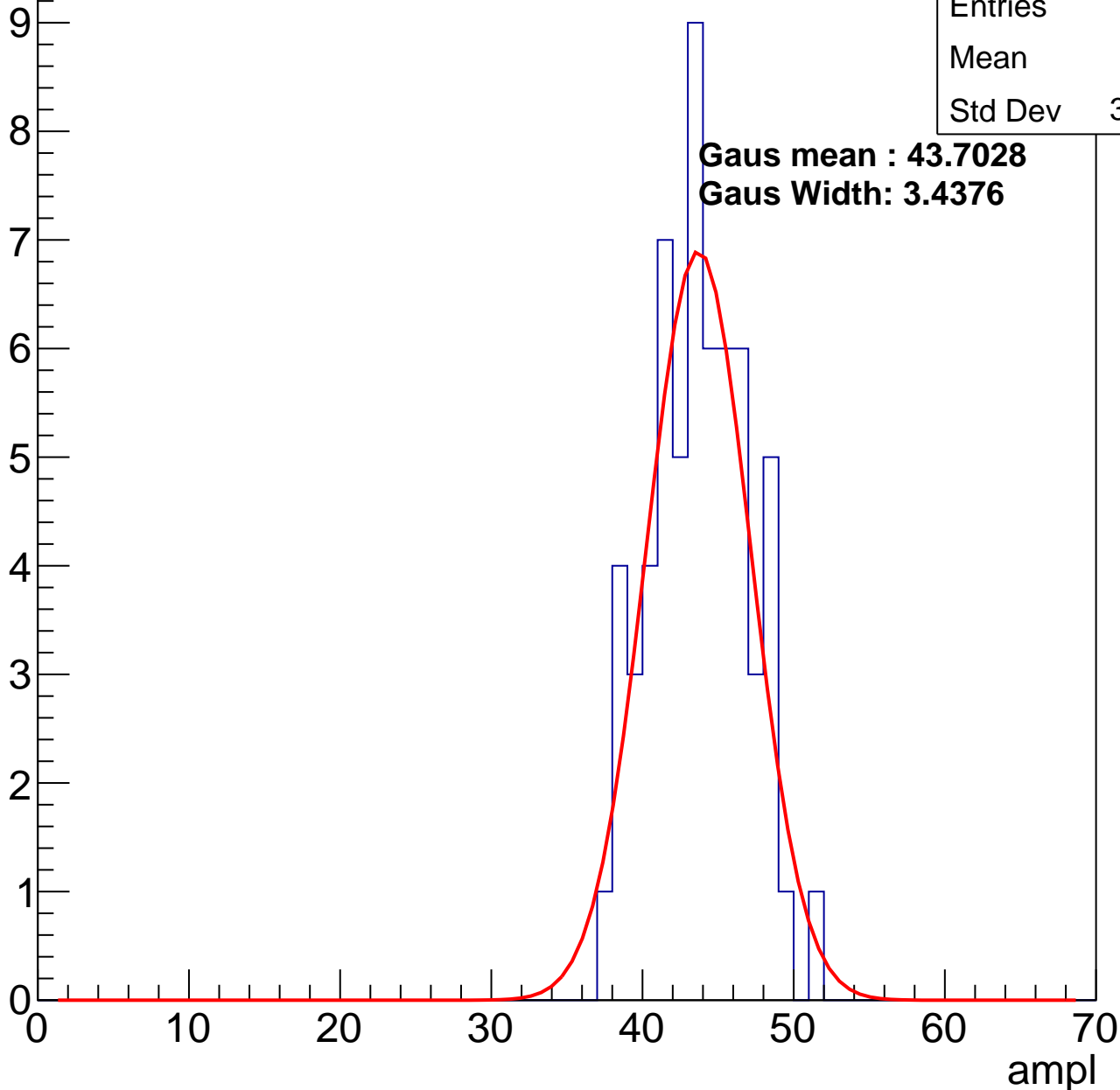
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	43.3
Std Dev	3.148

**Gaus mean : 43.7028**

**Gaus Width: 3.4376**

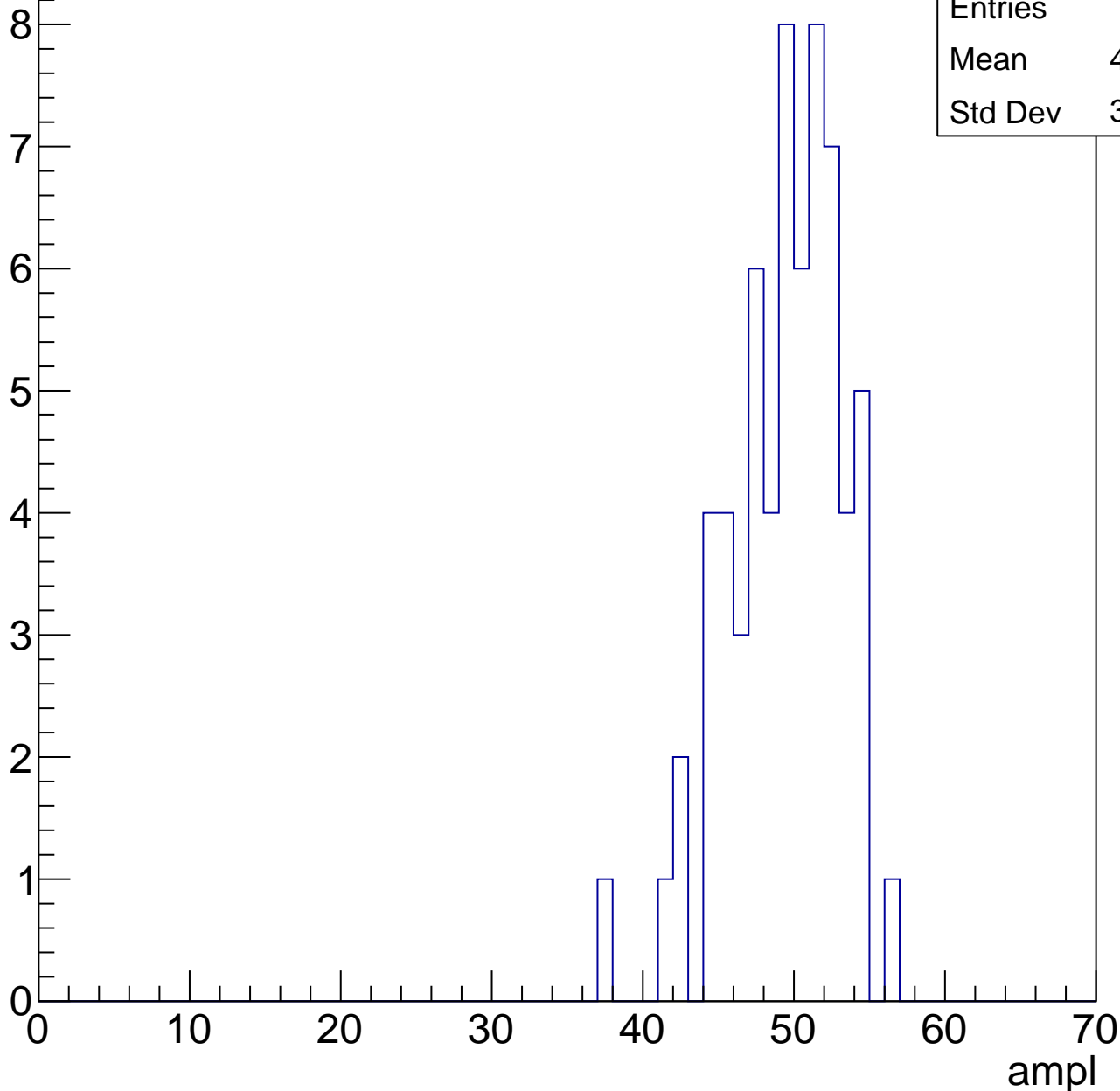


# B1L101S, U18-ch20, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

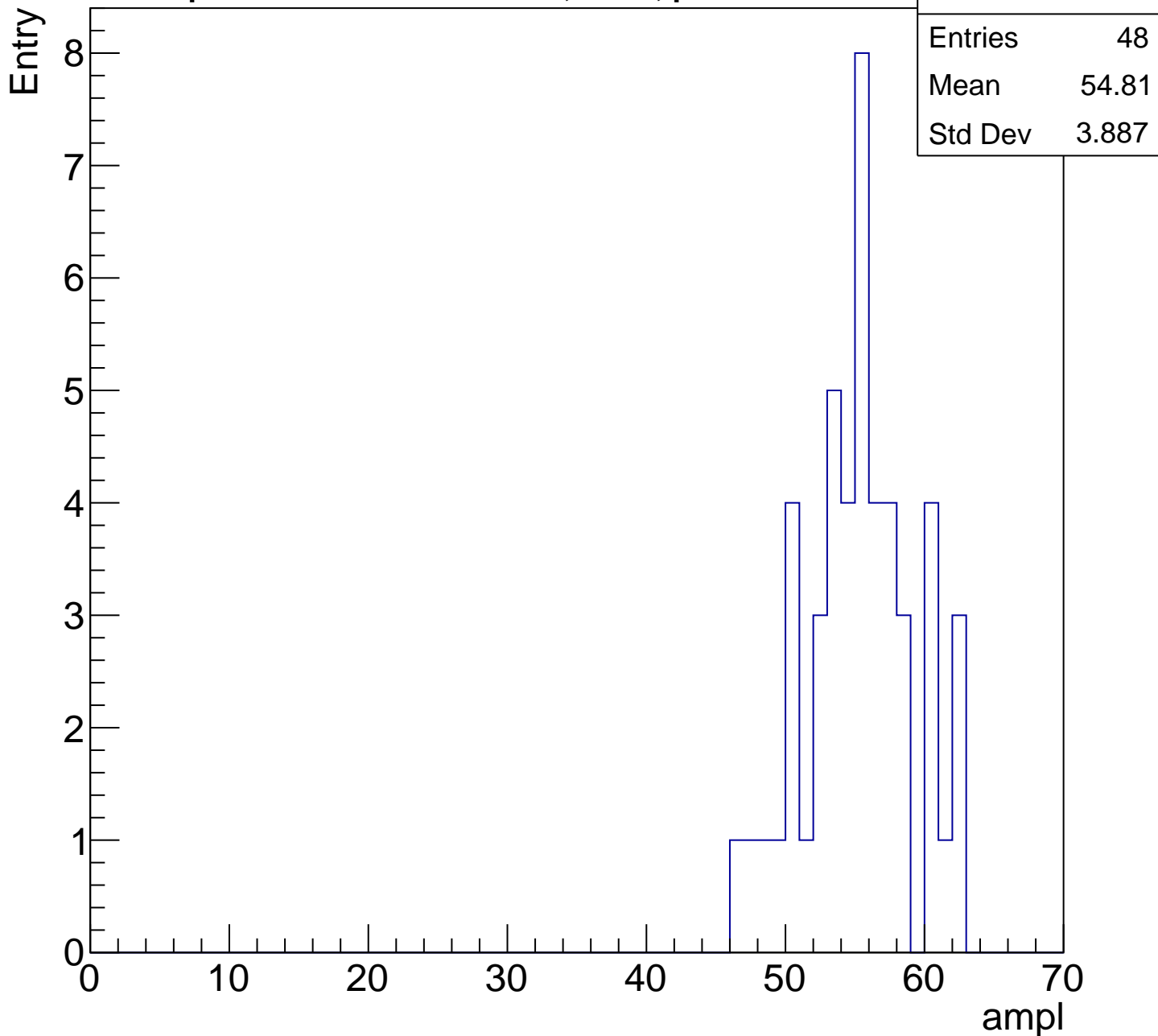
Entry

Entries	64
Mean	48.94
Std Dev	3.674



# B1L101S, U18-ch20, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U18-ch20, adc5

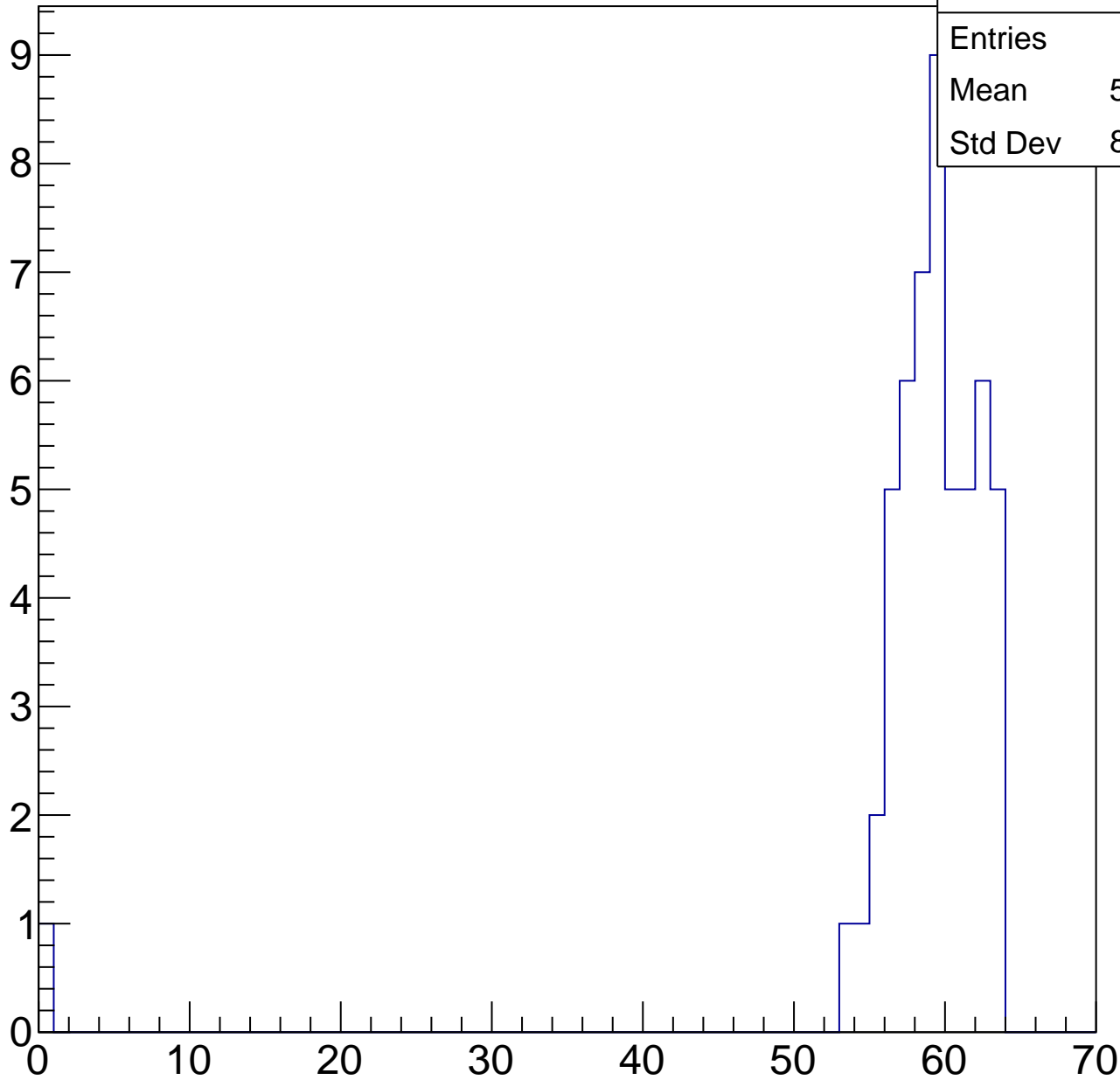
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	53
Mean	57.89
Std Dev	8.404

ampl

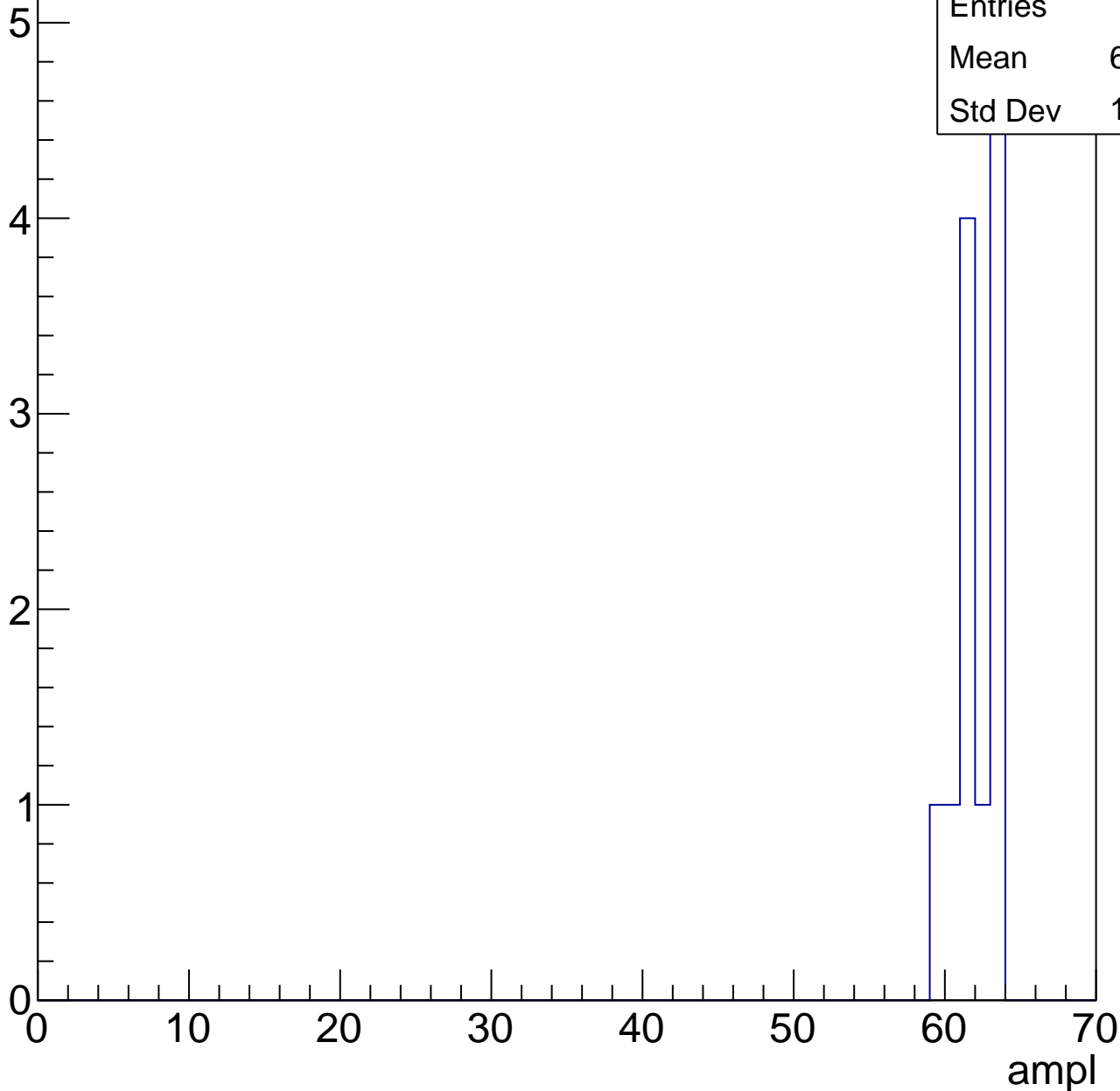


# B1L101S, U18-ch20, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	12
Mean	61.67
Std Dev	1.312





# B1L101S, U18-ch20, adc7

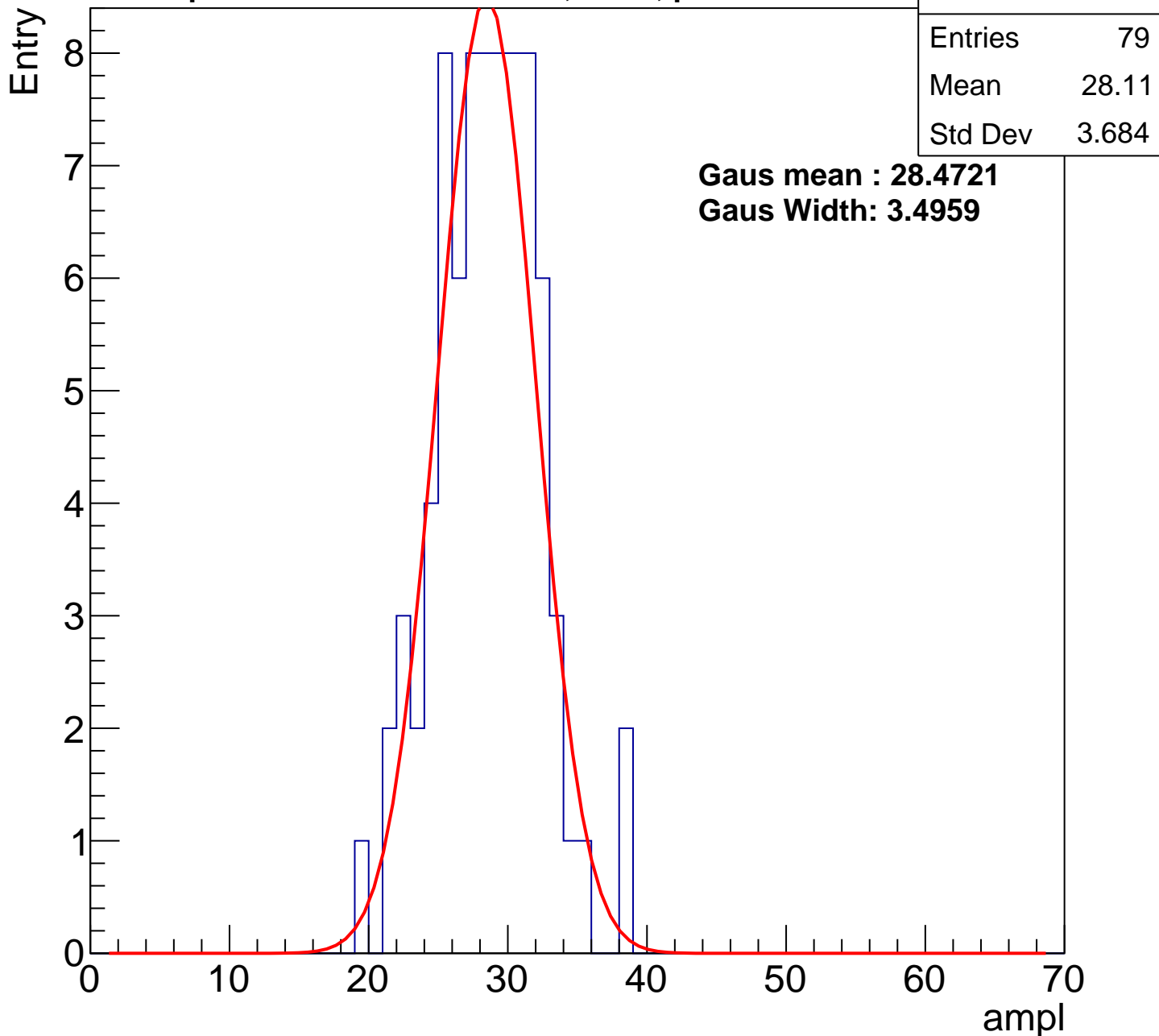
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch21, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U18-ch21, adc1

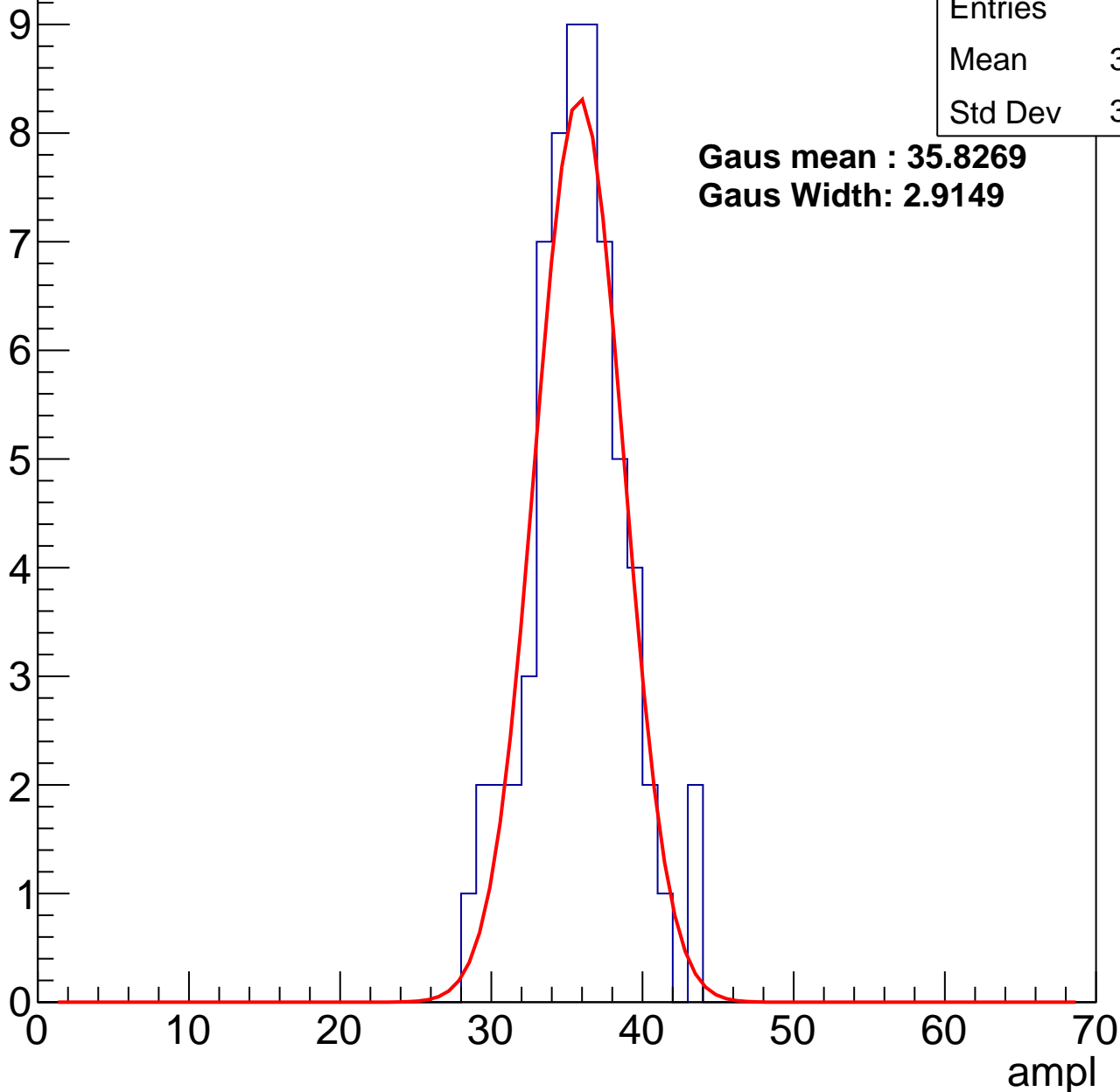
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	35.28
Std Dev	3.115

**Gaus mean : 35.8269**

**Gaus Width: 2.9149**



# B1L101S, U18-ch21, adc2

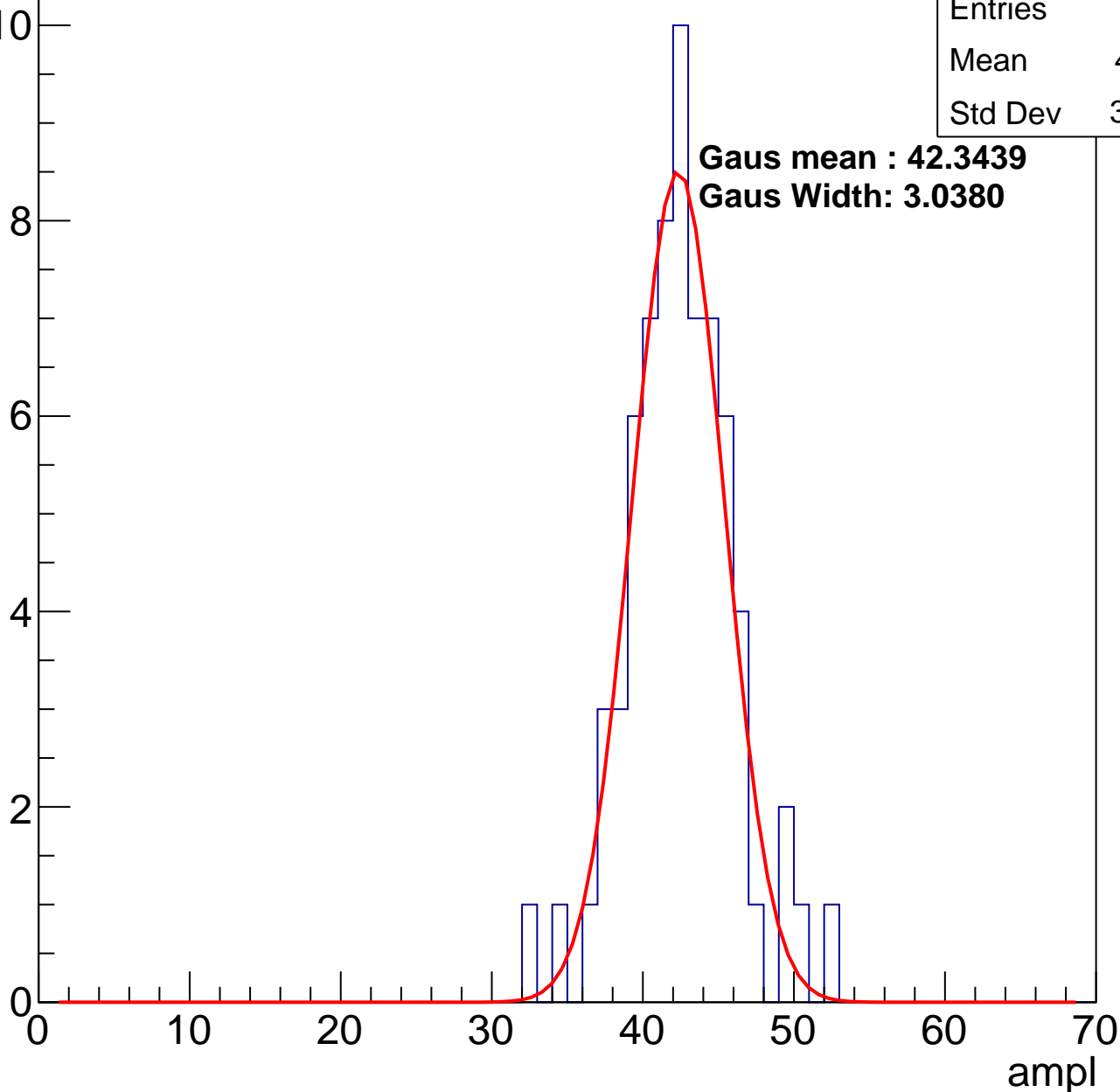
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	42.01
Std Dev	3.516

**Gaus mean : 42.3439**

**Gaus Width: 3.0380**

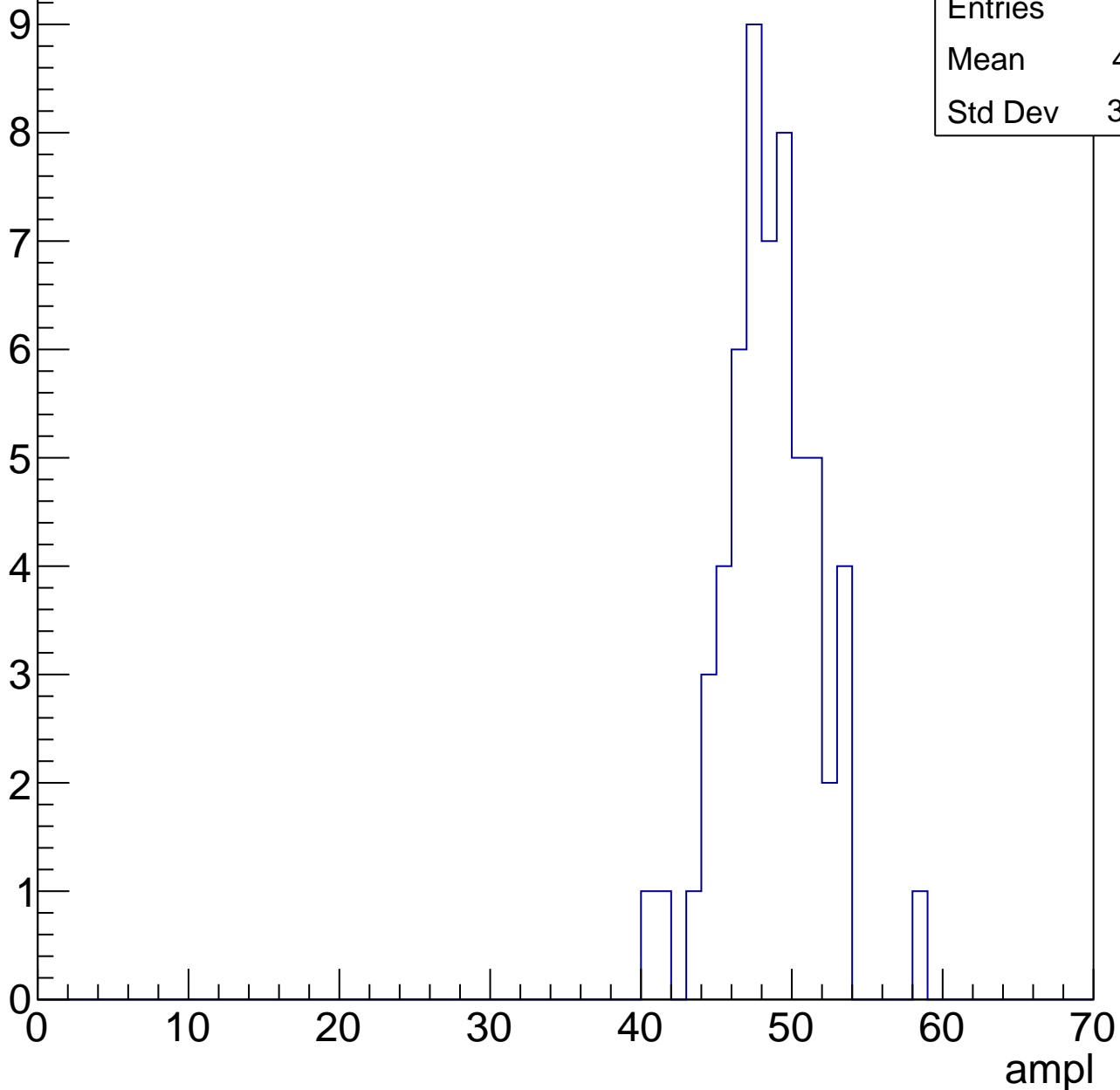


# B1L101S, U18-ch21, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	48.11
Std Dev	3.133

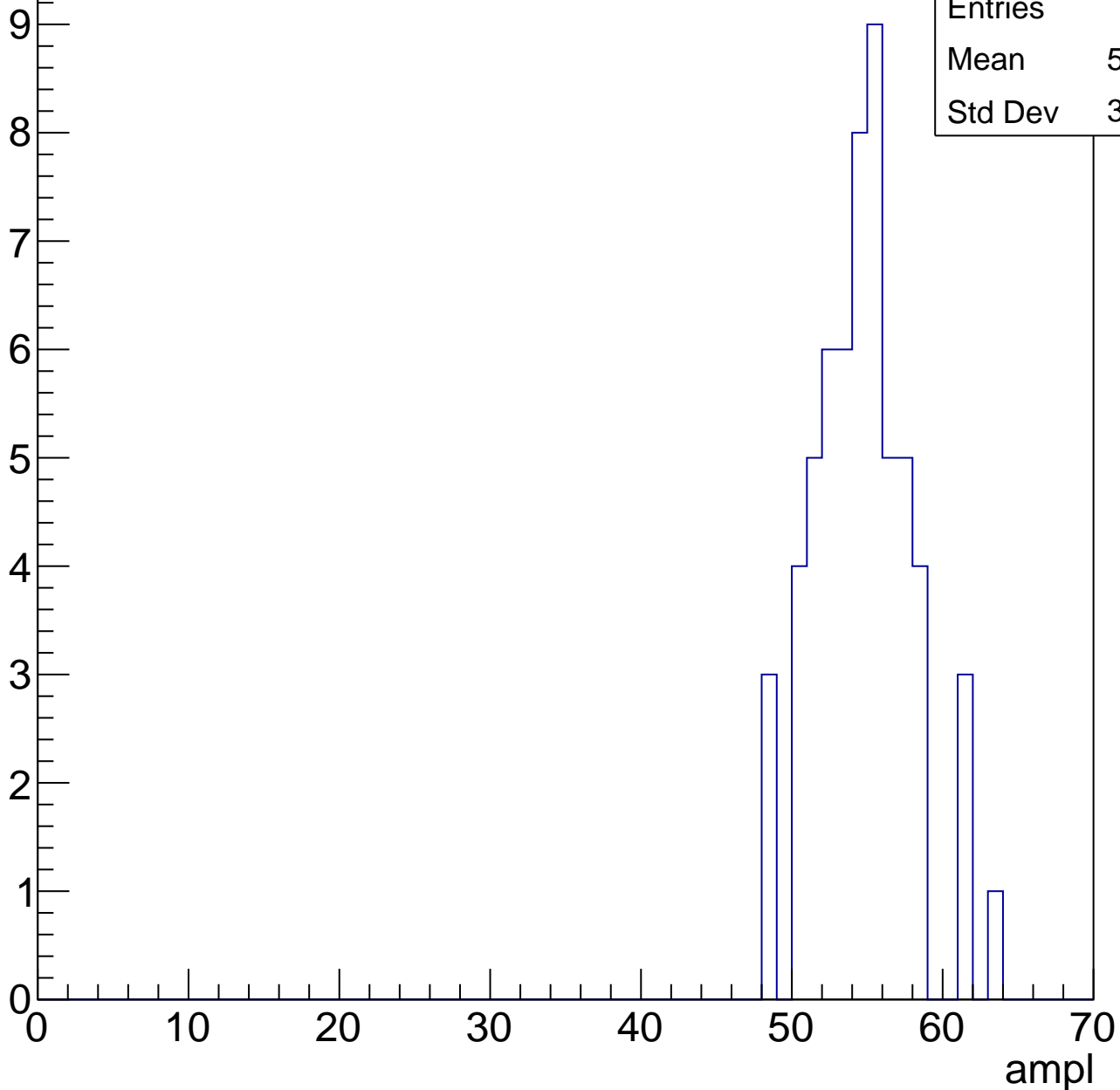


# B1L101S, U18-ch21, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

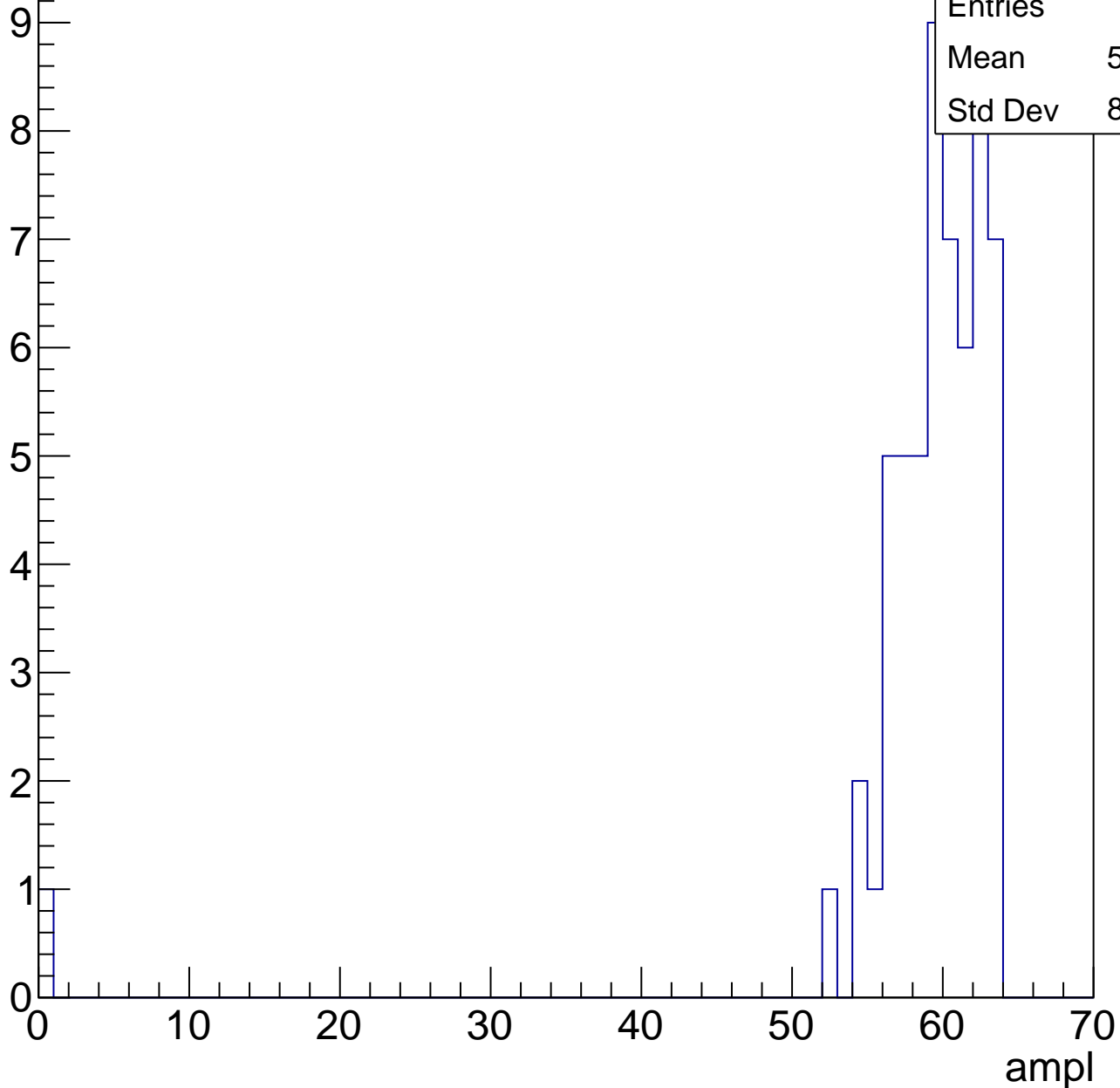
Entries	59
Mean	54.22
Std Dev	3.216



# B1L101S, U18-ch21, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

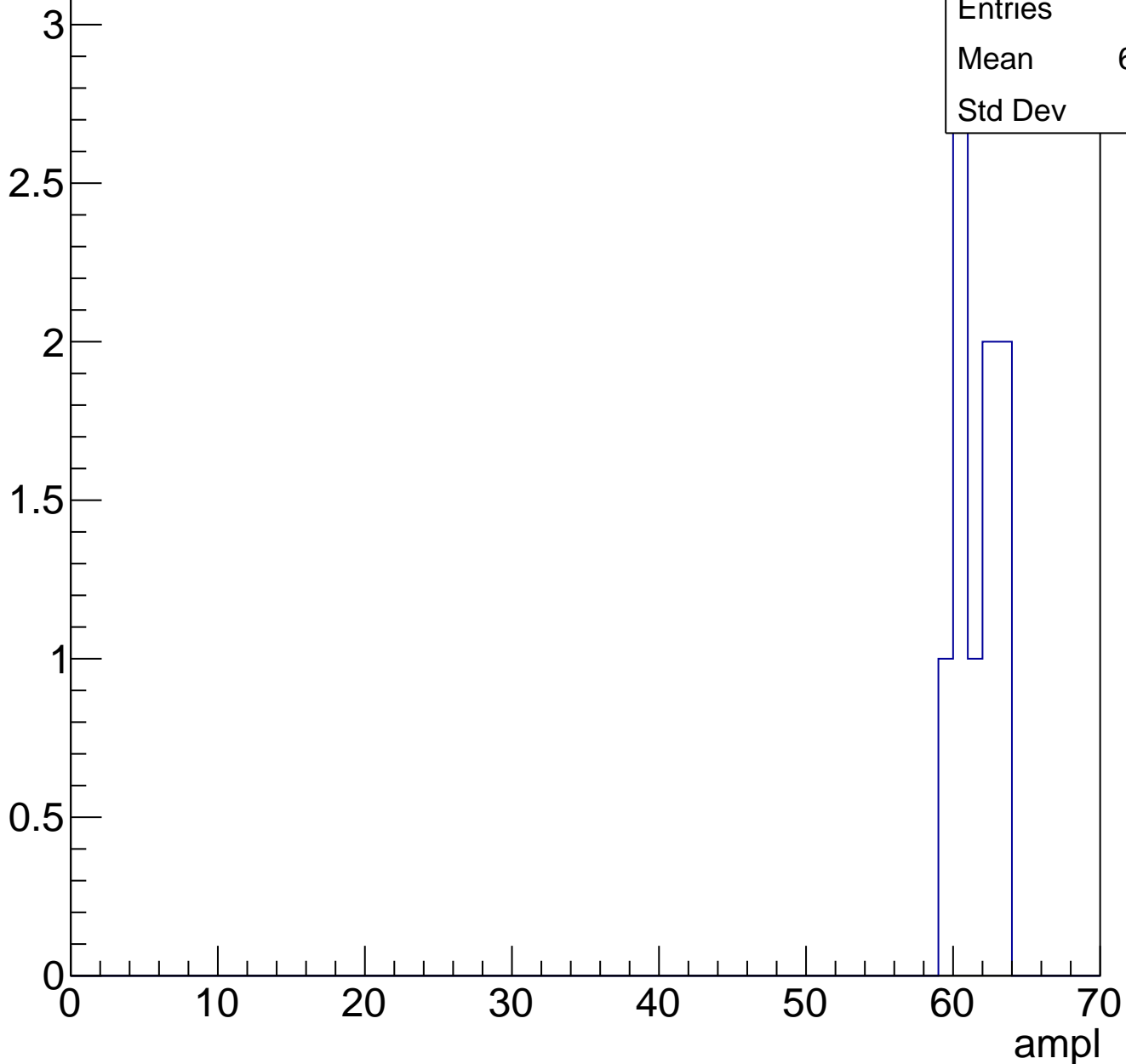
Entry



# B1L101S, U18-ch21, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch21, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch22, adc0

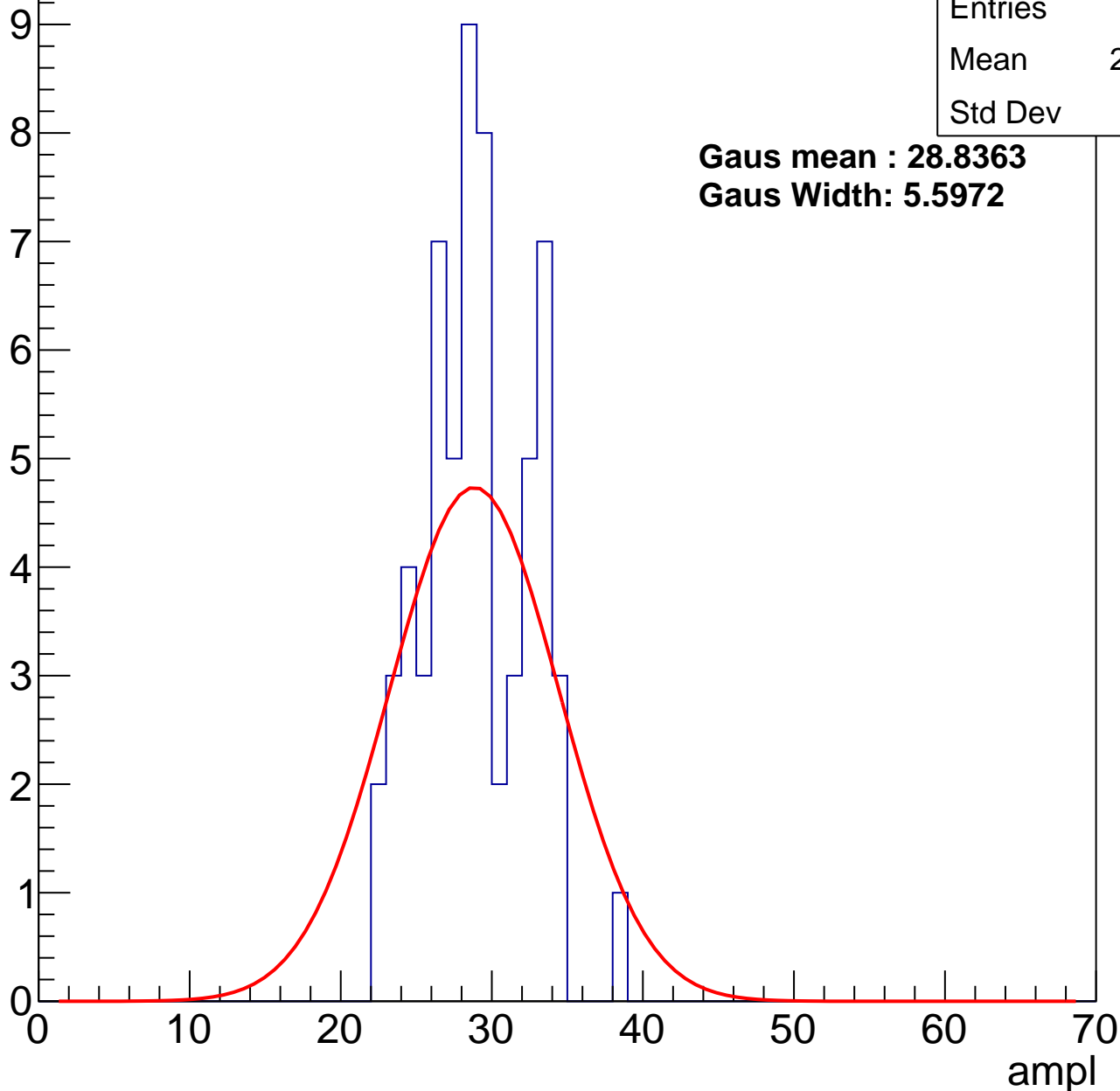
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	28.53
Std Dev	3.5

**Gaus mean : 28.8363**

**Gaus Width: 5.5972**



# B1L101S, U18-ch22, adc1

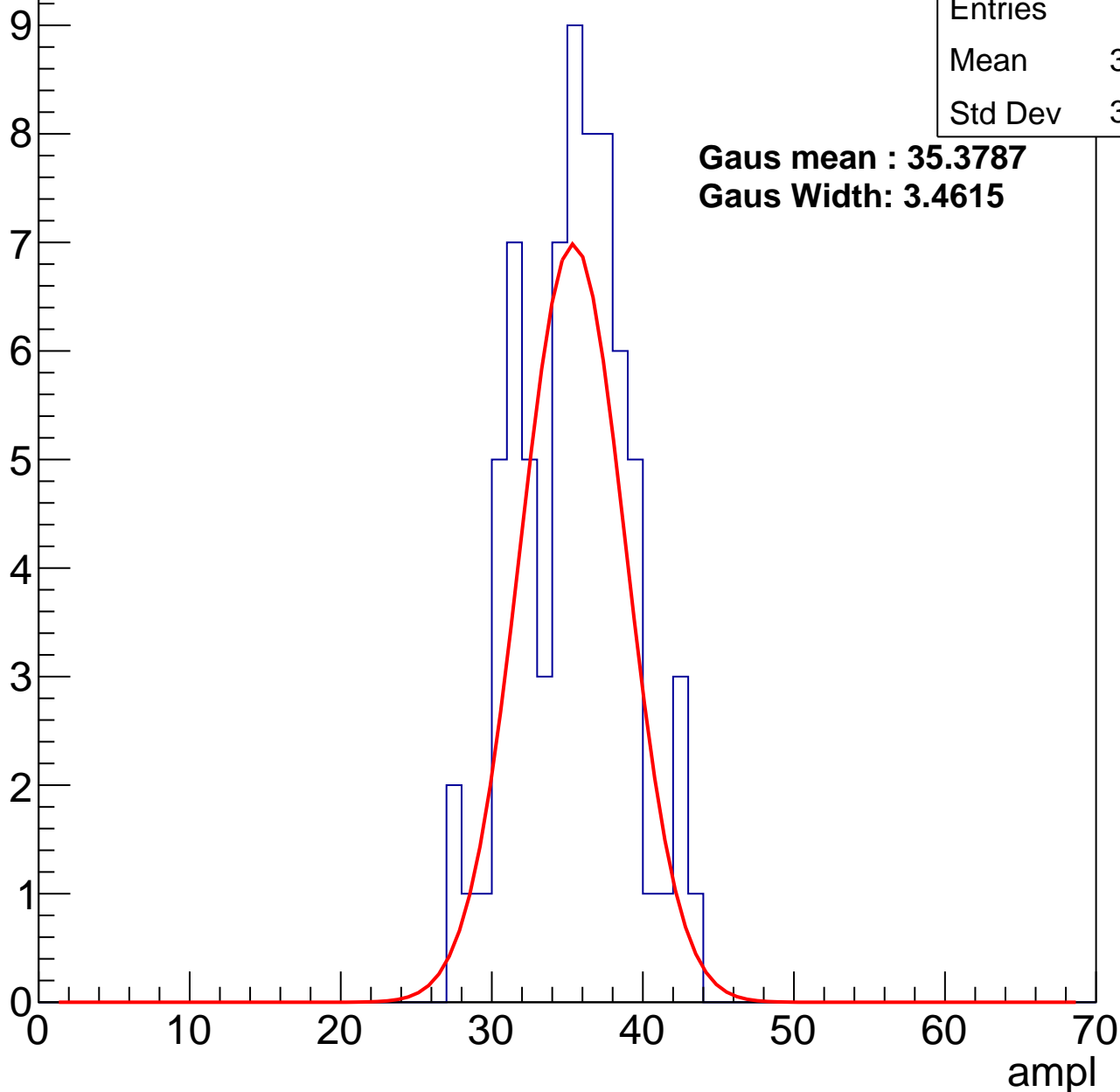
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	34.89
Std Dev	3.625

**Gaus mean : 35.3787**

**Gaus Width: 3.4615**



# B1L101S, U18-ch22, adc2

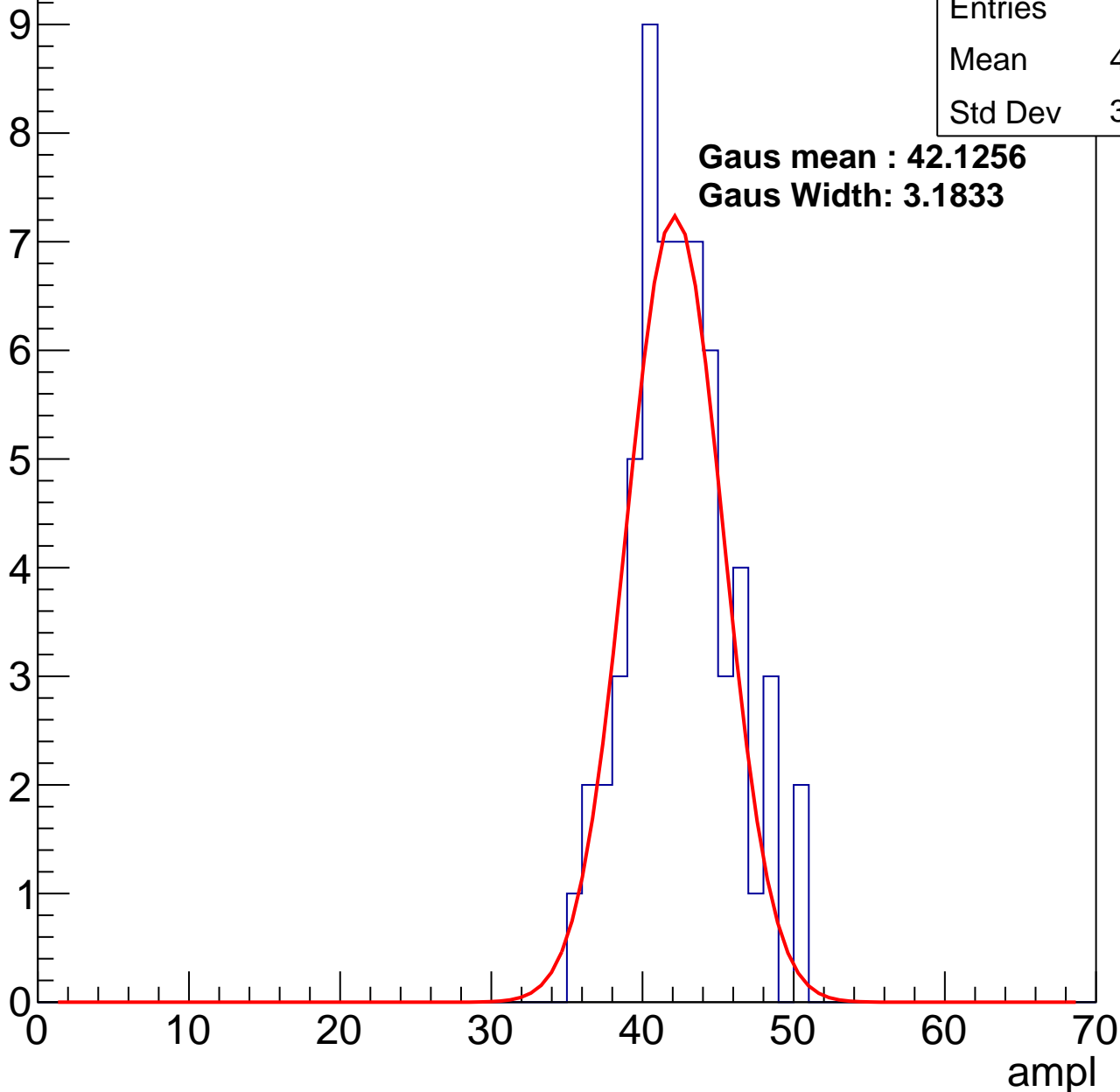
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	42.03
Std Dev	3.336

**Gaus mean : 42.1256**

**Gaus Width: 3.1833**



# B1L101S, U18-ch22, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	85
Mean	49.18
Std Dev	3.676

Entry

10

8

6

4

2

0

0

10

20

30

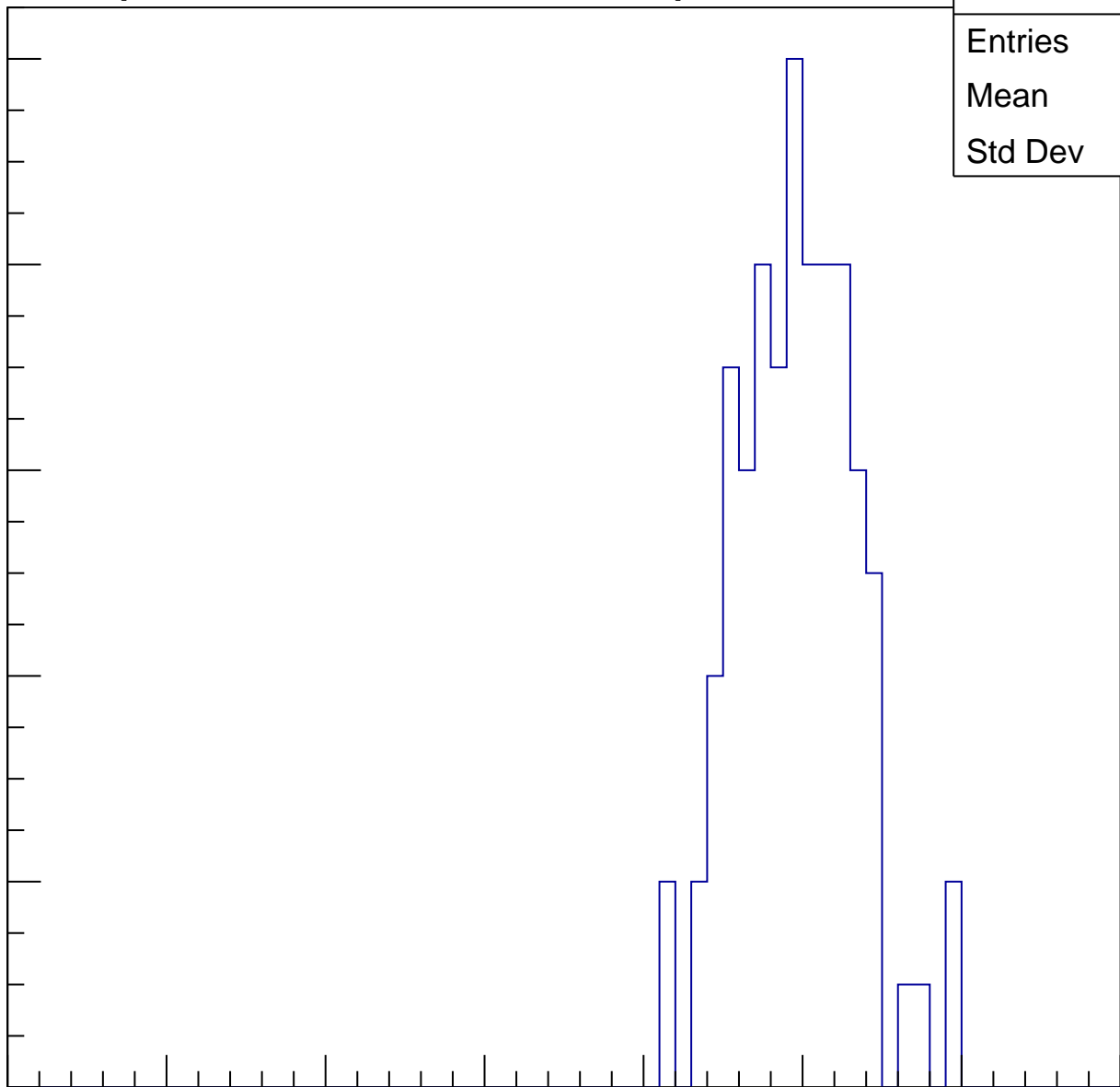
40

50

60

ampl

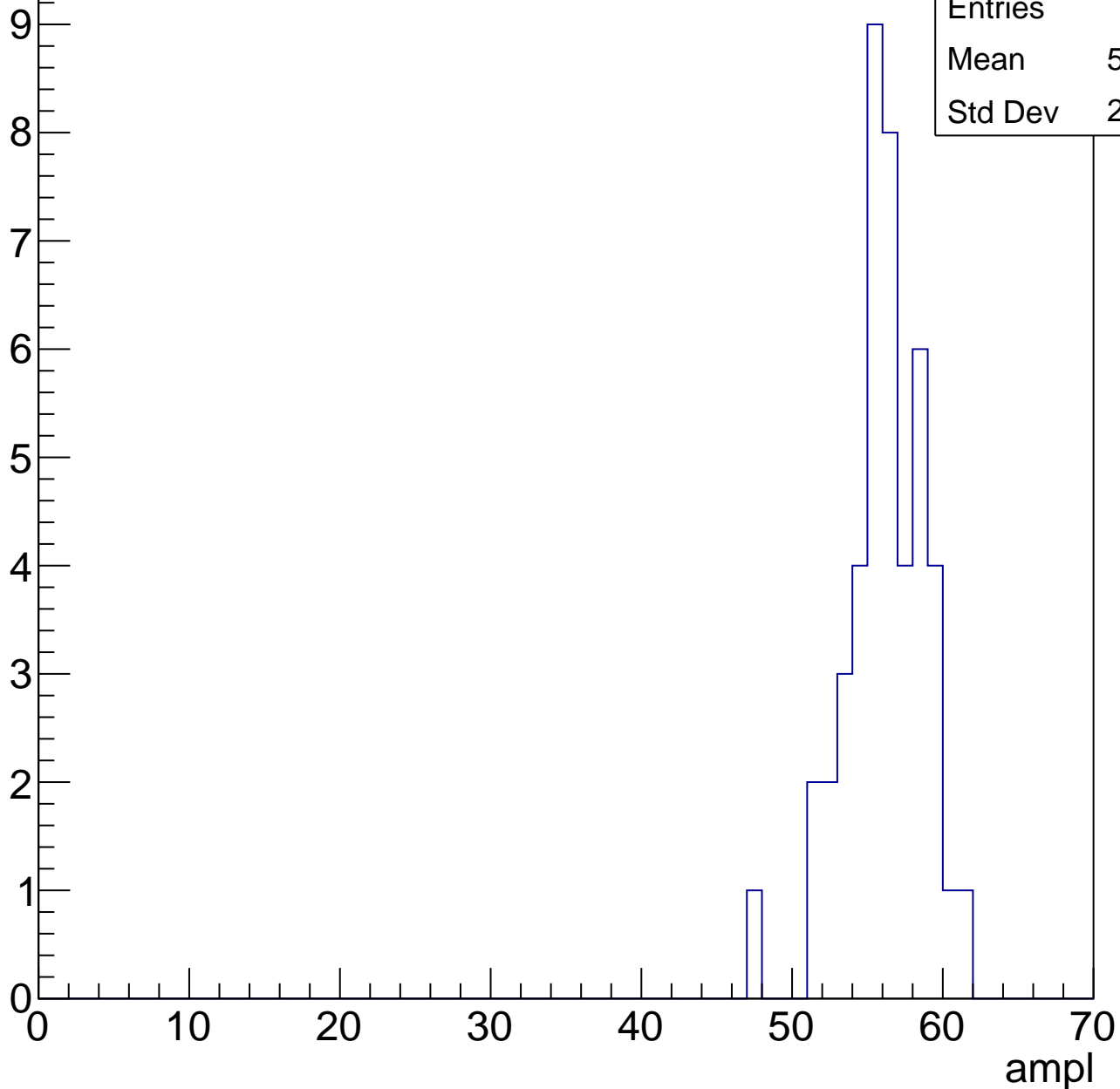
70



# B1L101S, U18-ch22, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

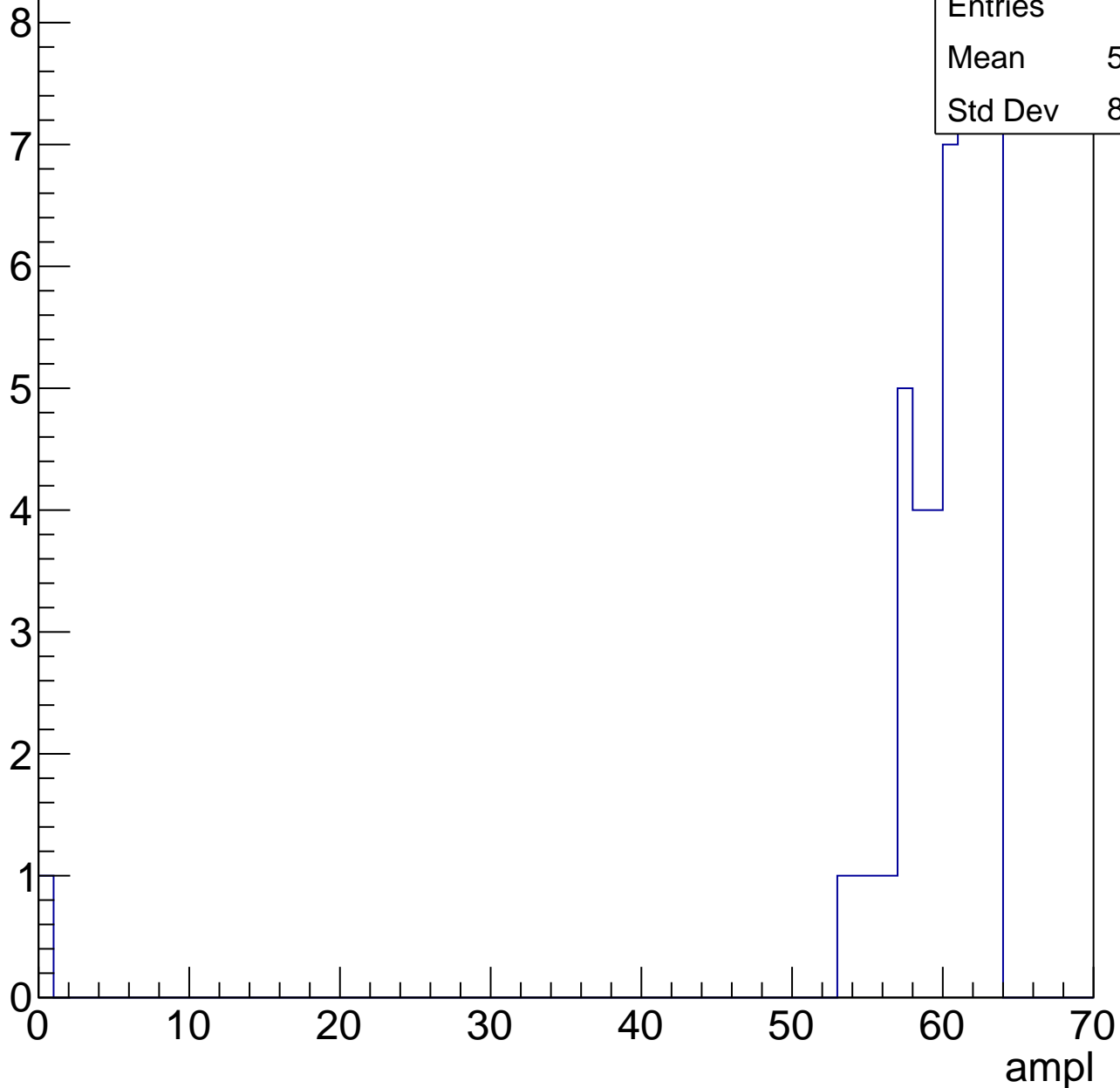


Entries	45
Mean	55.64
Std Dev	2.643

# B1L101S, U18-ch22, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch22, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	7
Mean	61.57
Std Dev	1.178

ampl



# B1L101S, U18-ch22, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch23, adc0

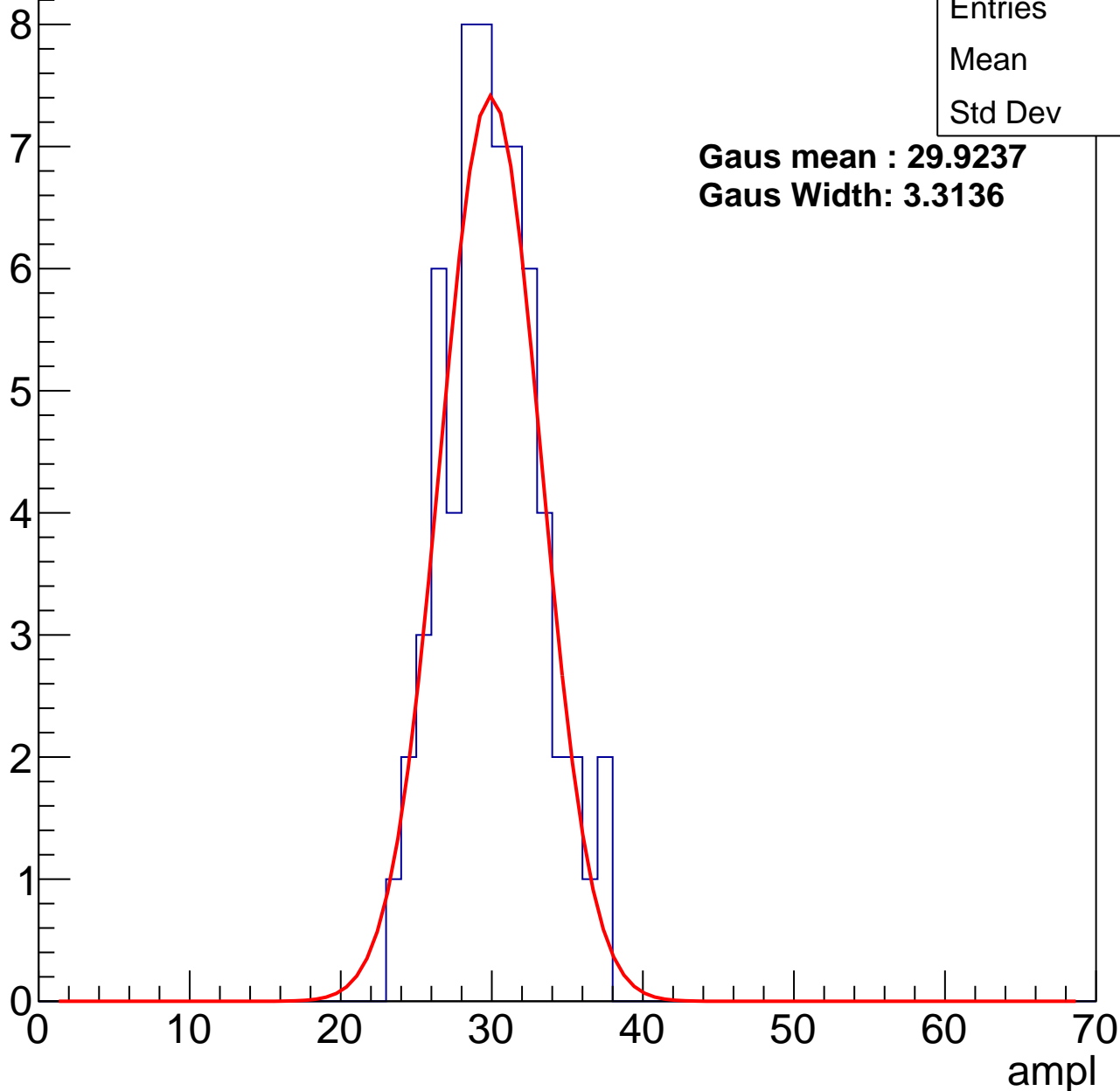
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	29.6
Std Dev	3.19

**Gaus mean : 29.9237**

**Gaus Width: 3.3136**



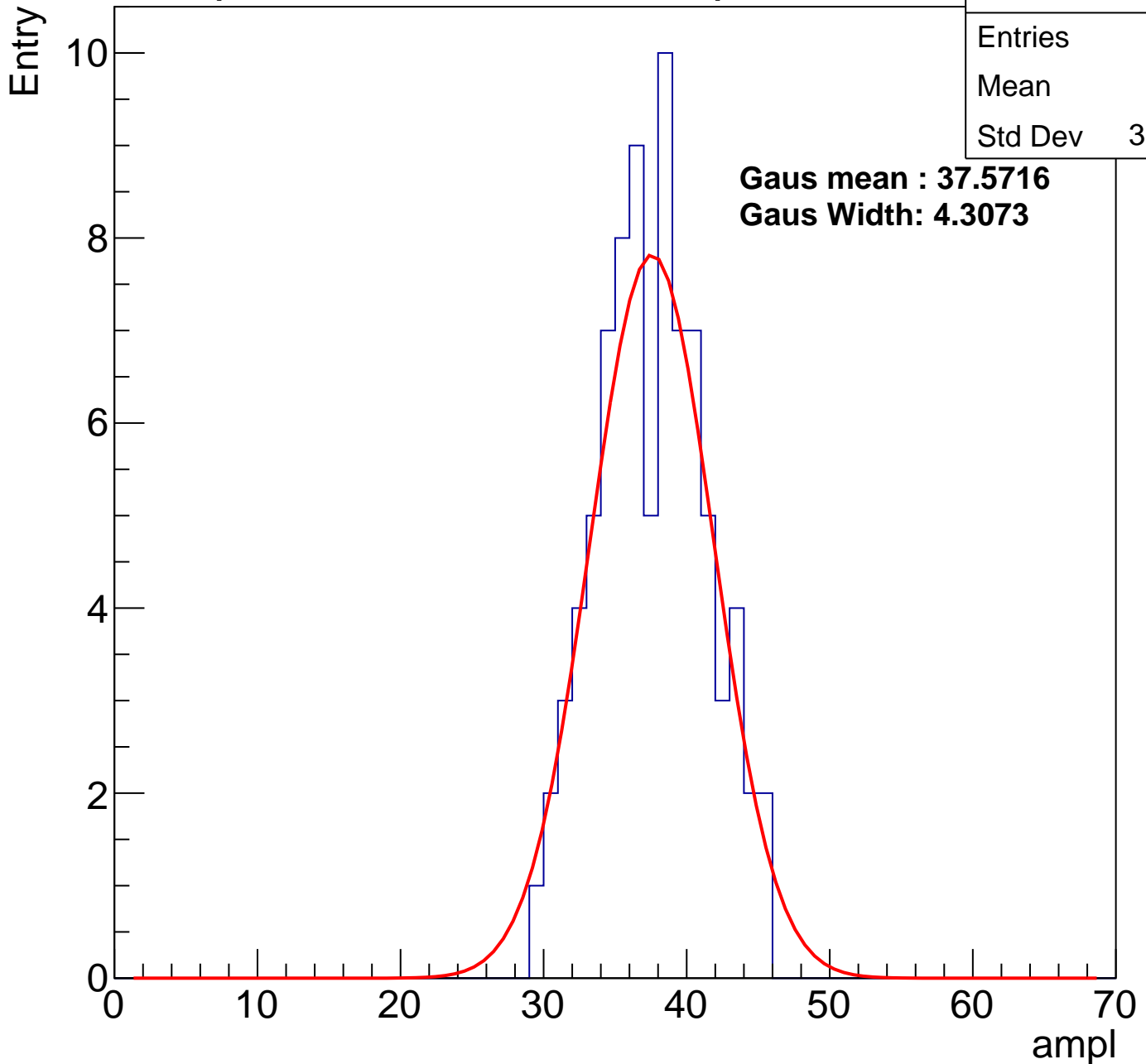
# B1L101S, U18-ch23, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	84
Mean	37.1
Std Dev	3.747

**Gaus mean : 37.5716**

**Gaus Width: 4.3073**



# B1L101S, U18-ch23, adc2

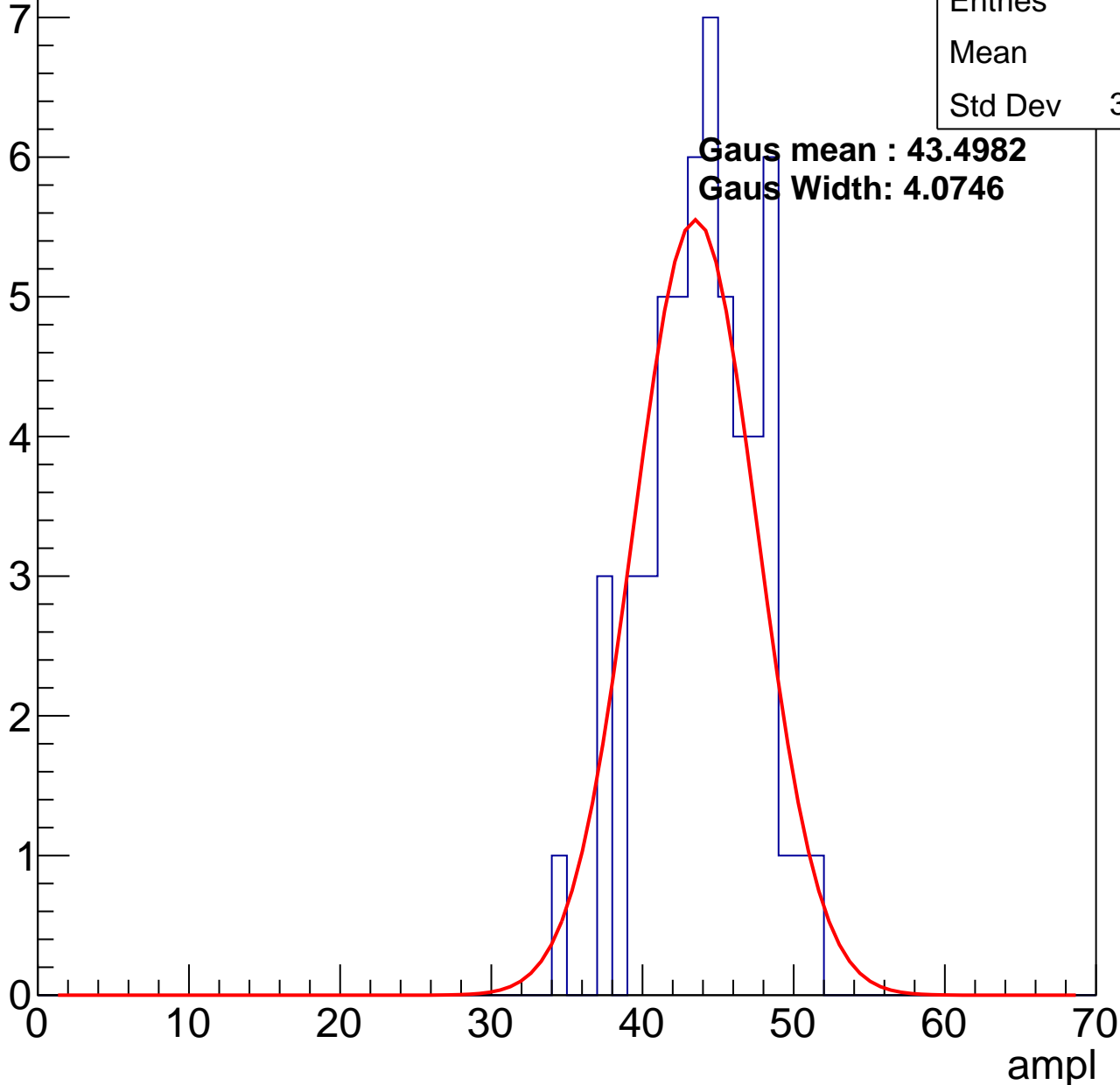
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	43.6
Std Dev	3.555

**Gaus mean : 43.4982**

**Gaus Width: 4.0746**

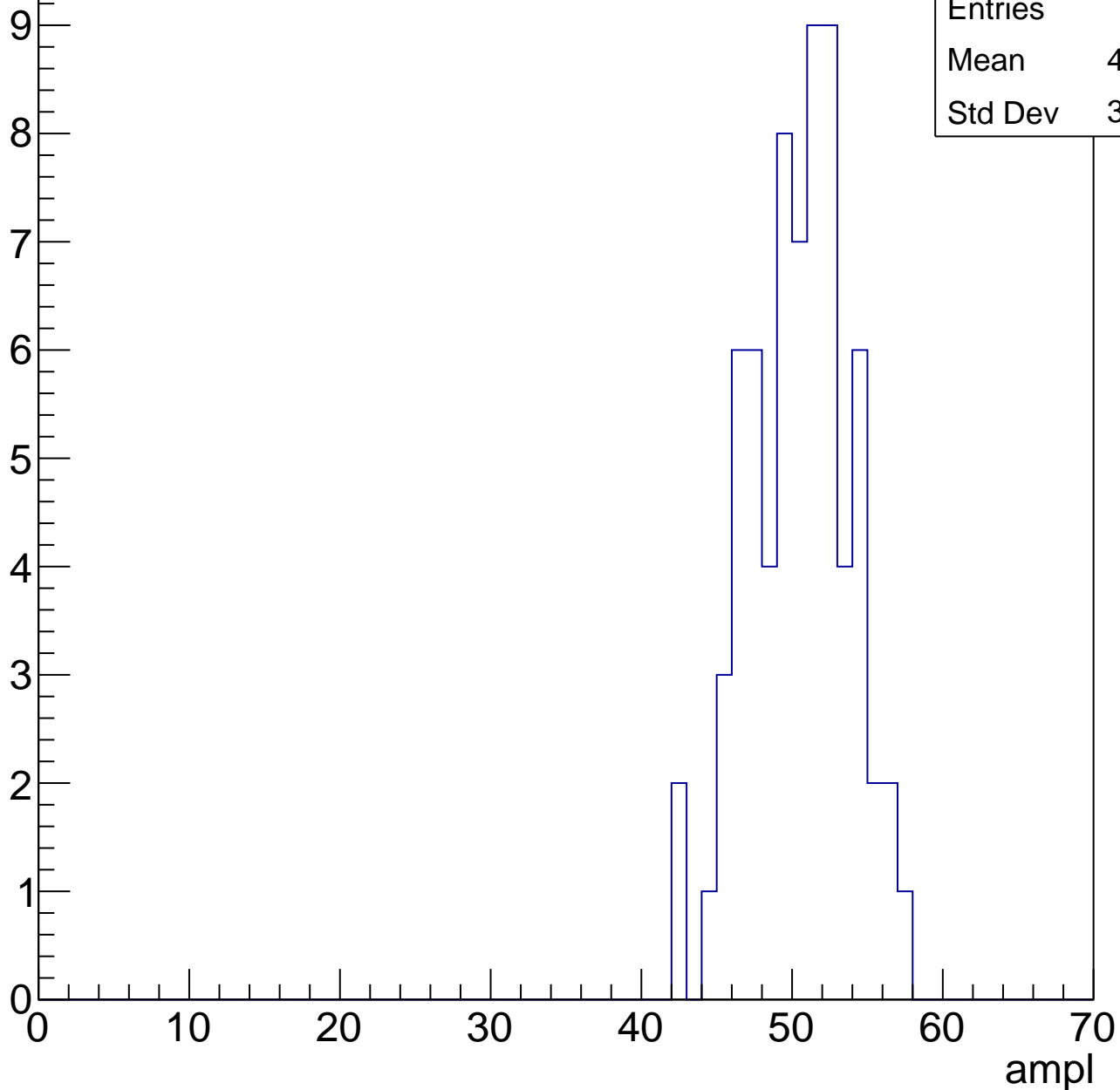


# B1L101S, U18-ch23, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	49.96
Std Dev	3.297

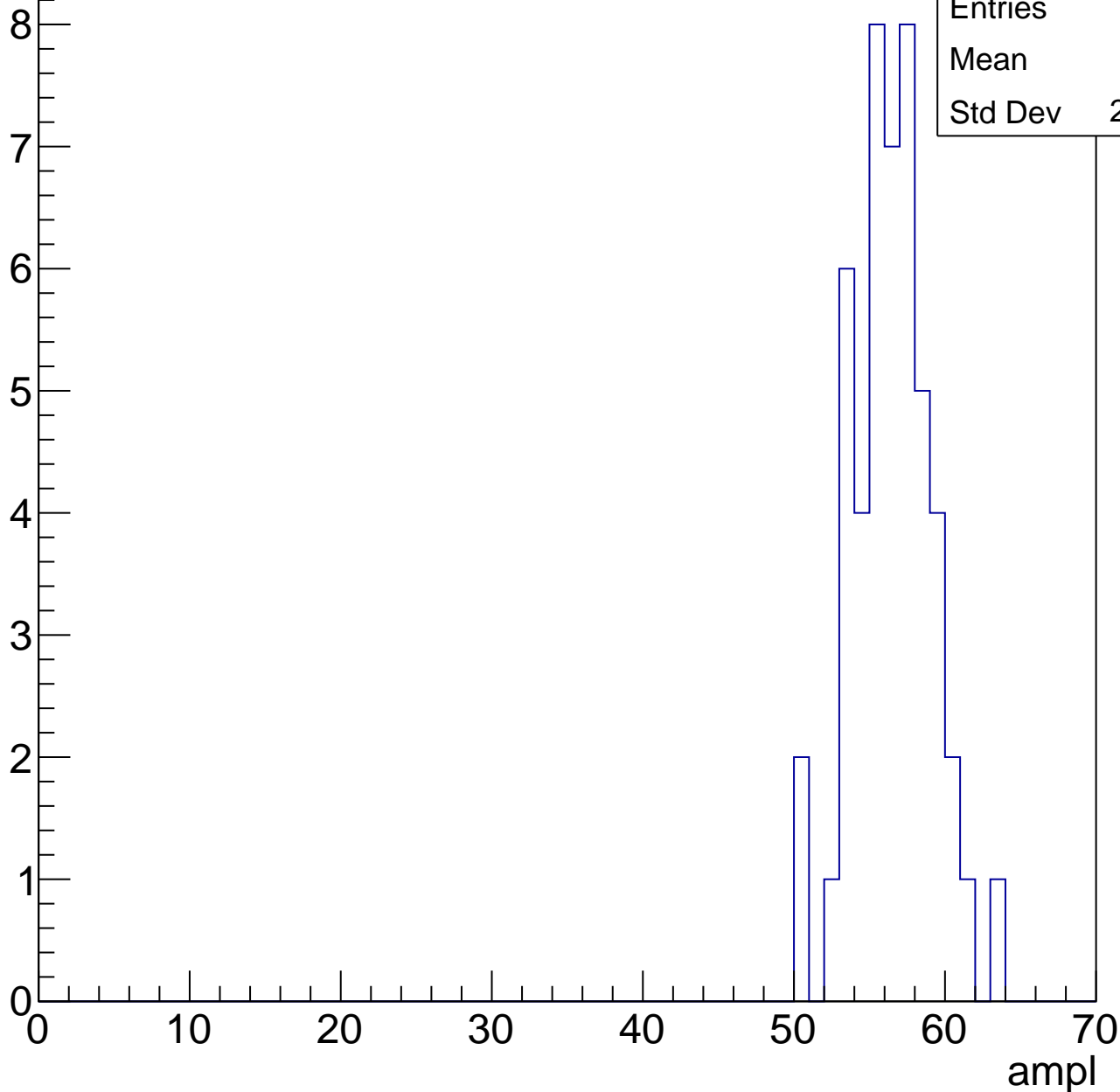


# B1L101S, U18-ch23, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

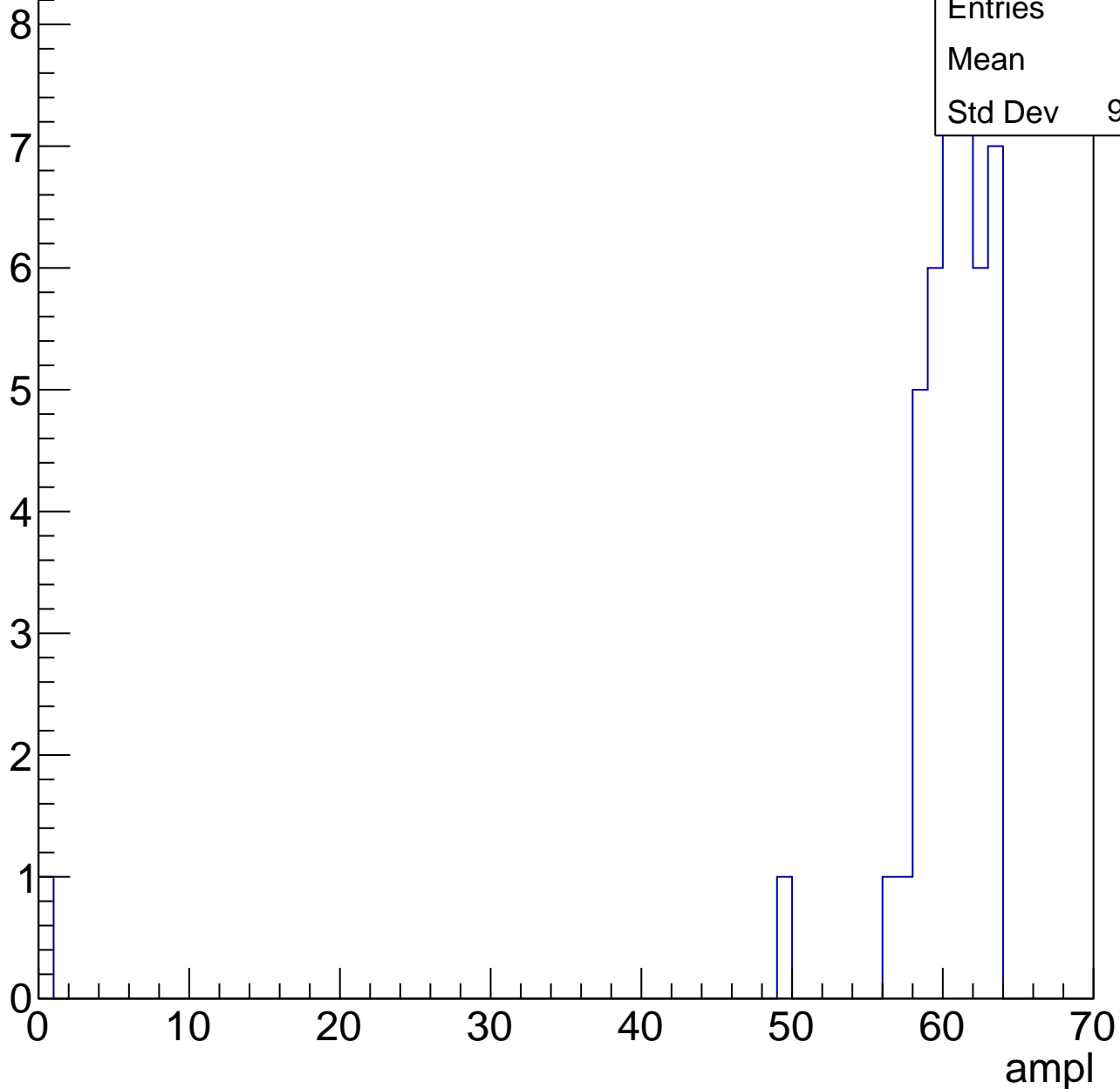
Entries	49
Mean	56
Std Dev	2.619



# B1L101S, U18-ch23, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch23, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch23, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U18-ch24, adc0

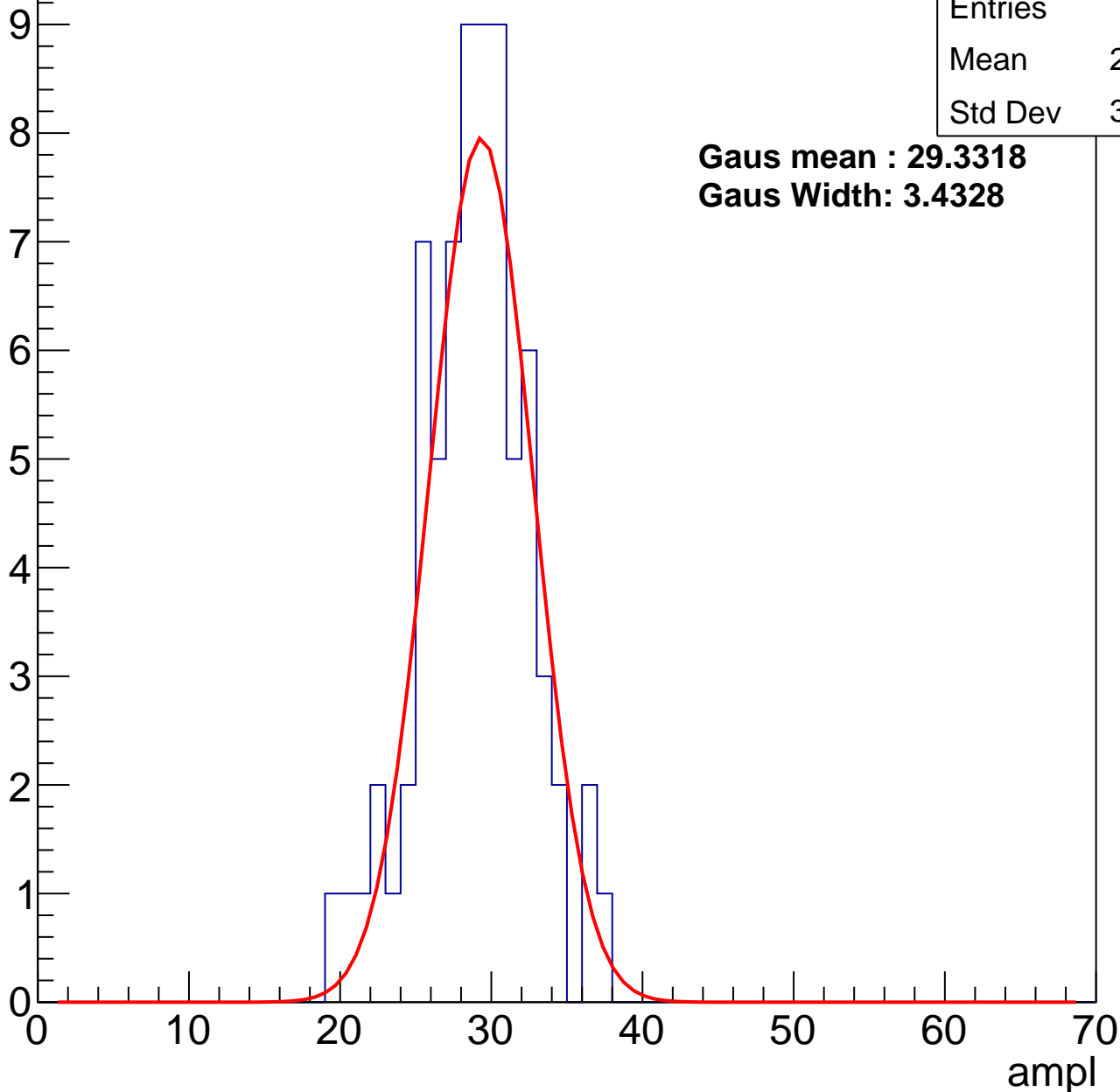
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	28.42
Std Dev	3.592

**Gaus mean : 29.3318**

**Gaus Width: 3.4328**



# B1L101S, U18-ch24, adc1

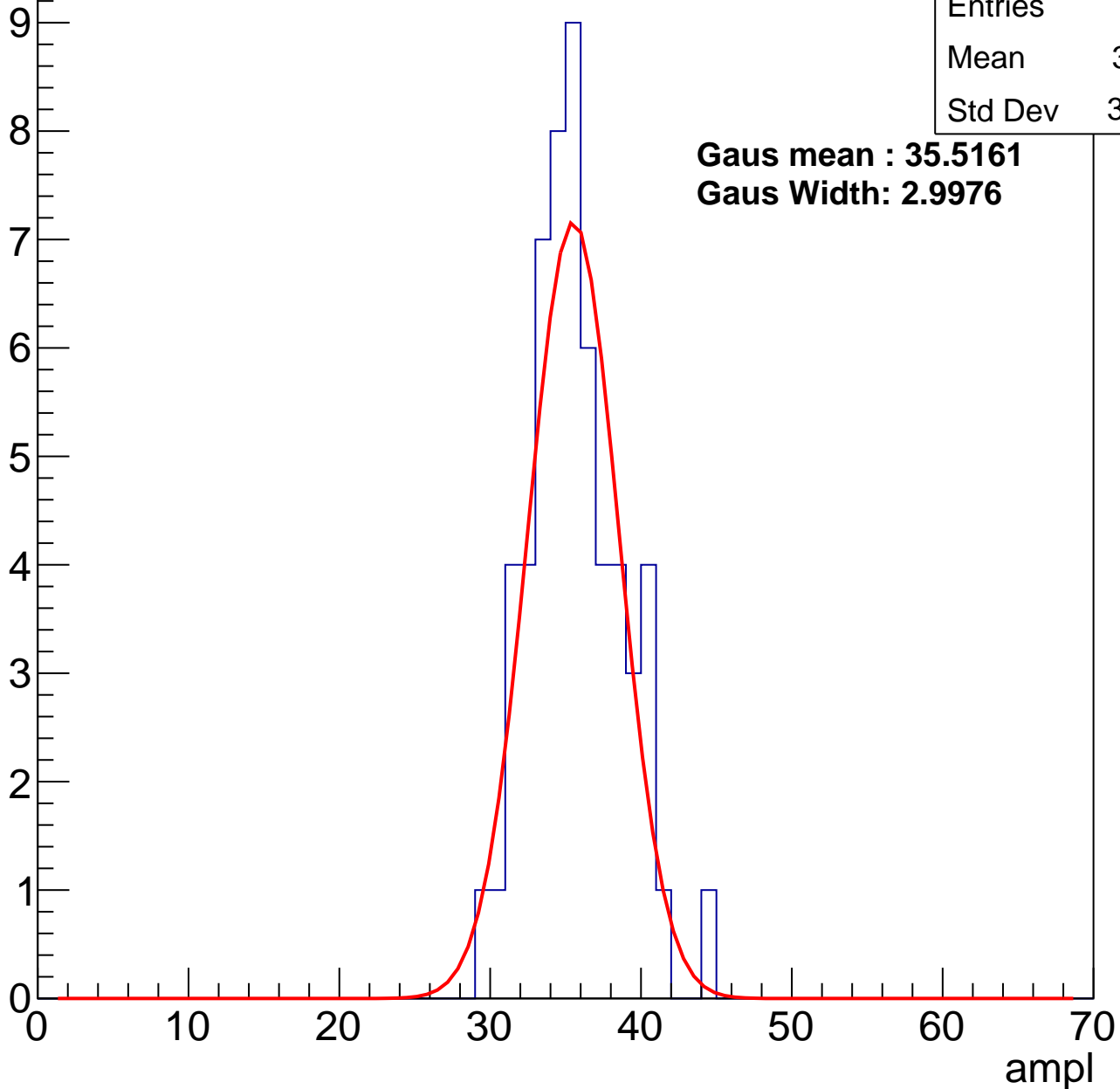
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	35.21
Std Dev	3.013

**Gaus mean : 35.5161**

**Gaus Width: 2.9976**



# B1L101S, U18-ch24, adc2

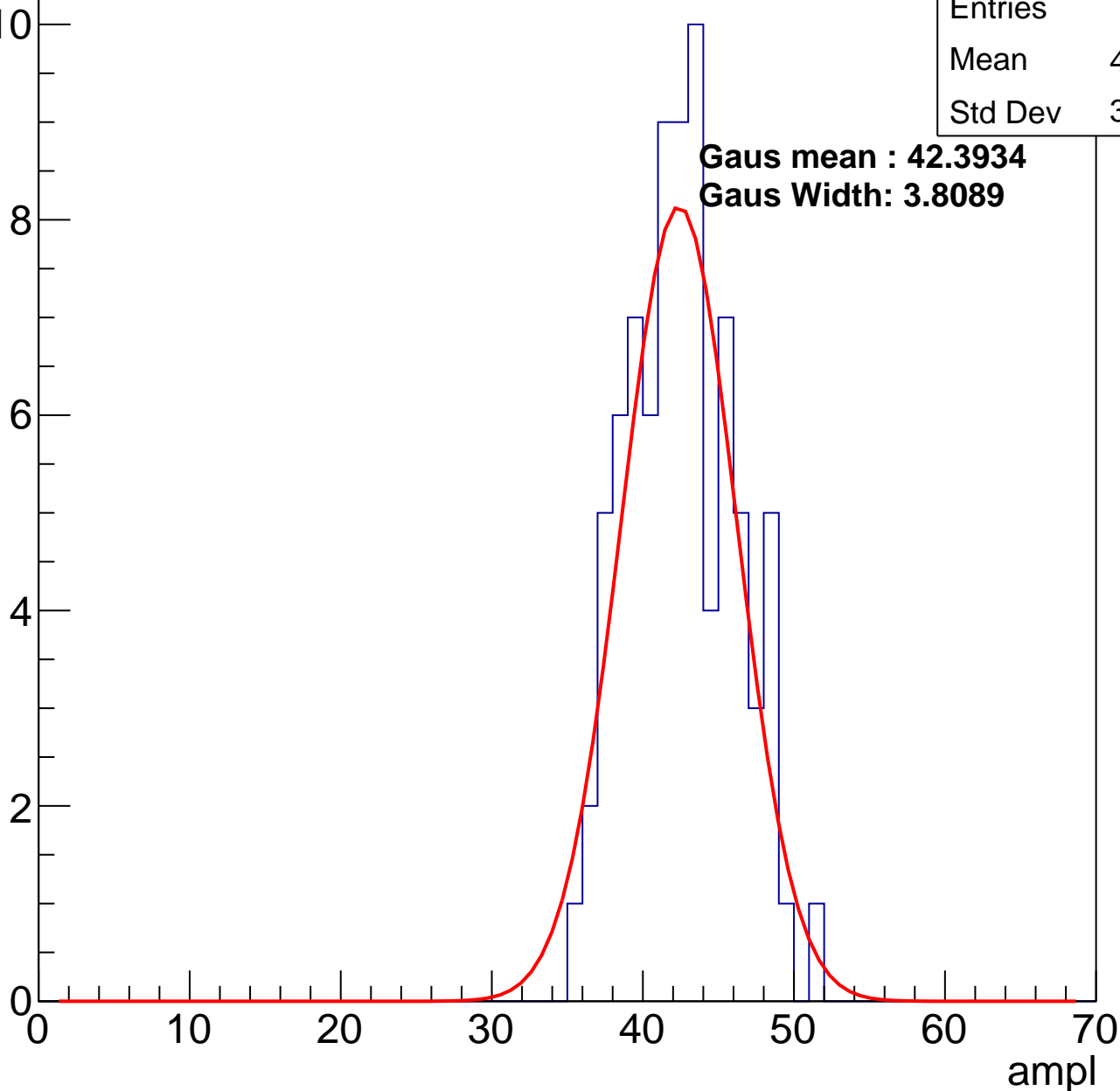
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	81
Mean	42.12
Std Dev	3.497

**Gaus mean : 42.3934**

**Gaus Width: 3.8089**



# B1L101S, U18-ch24, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

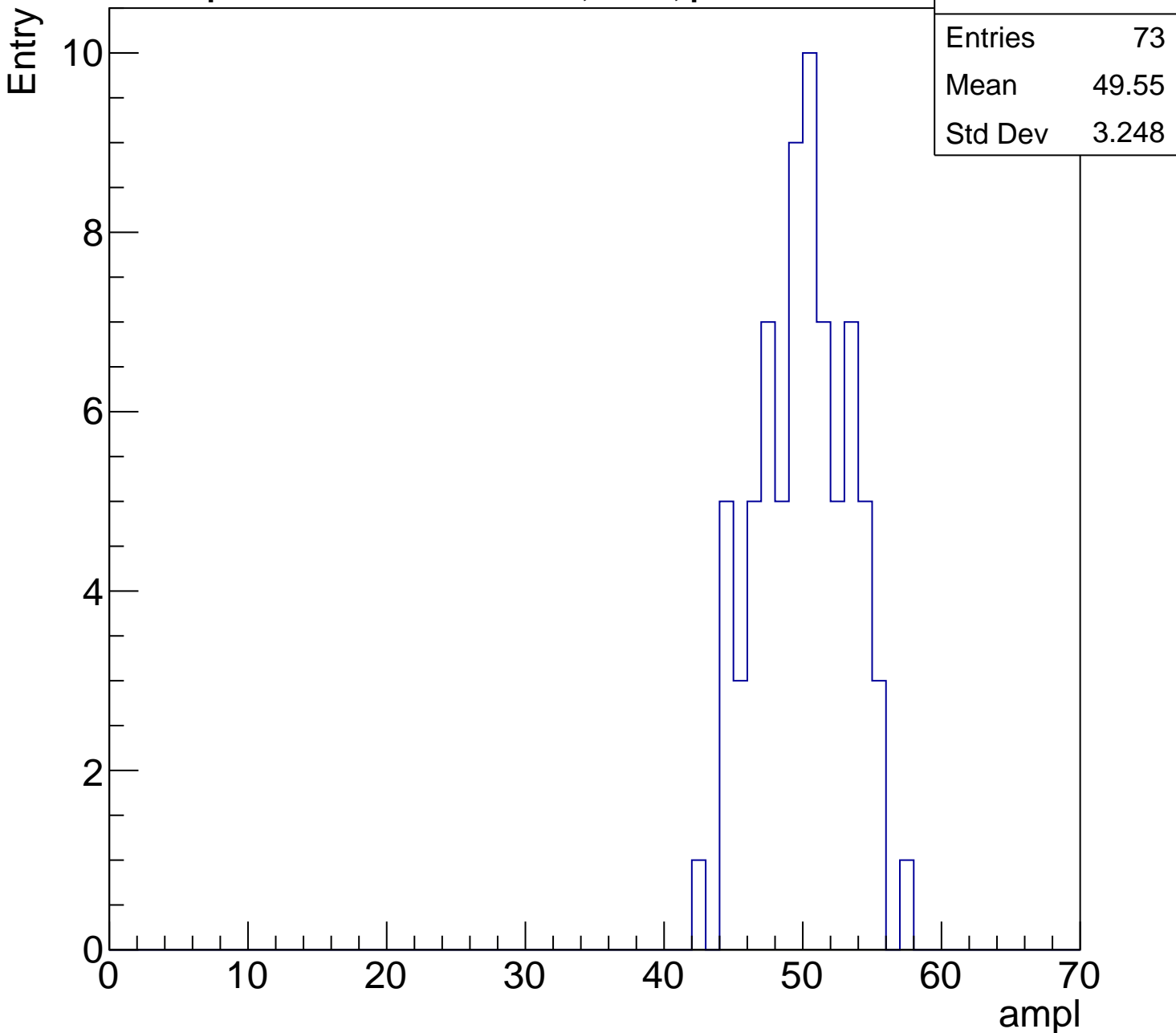
Entries	73
Mean	49.55
Std Dev	3.248

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

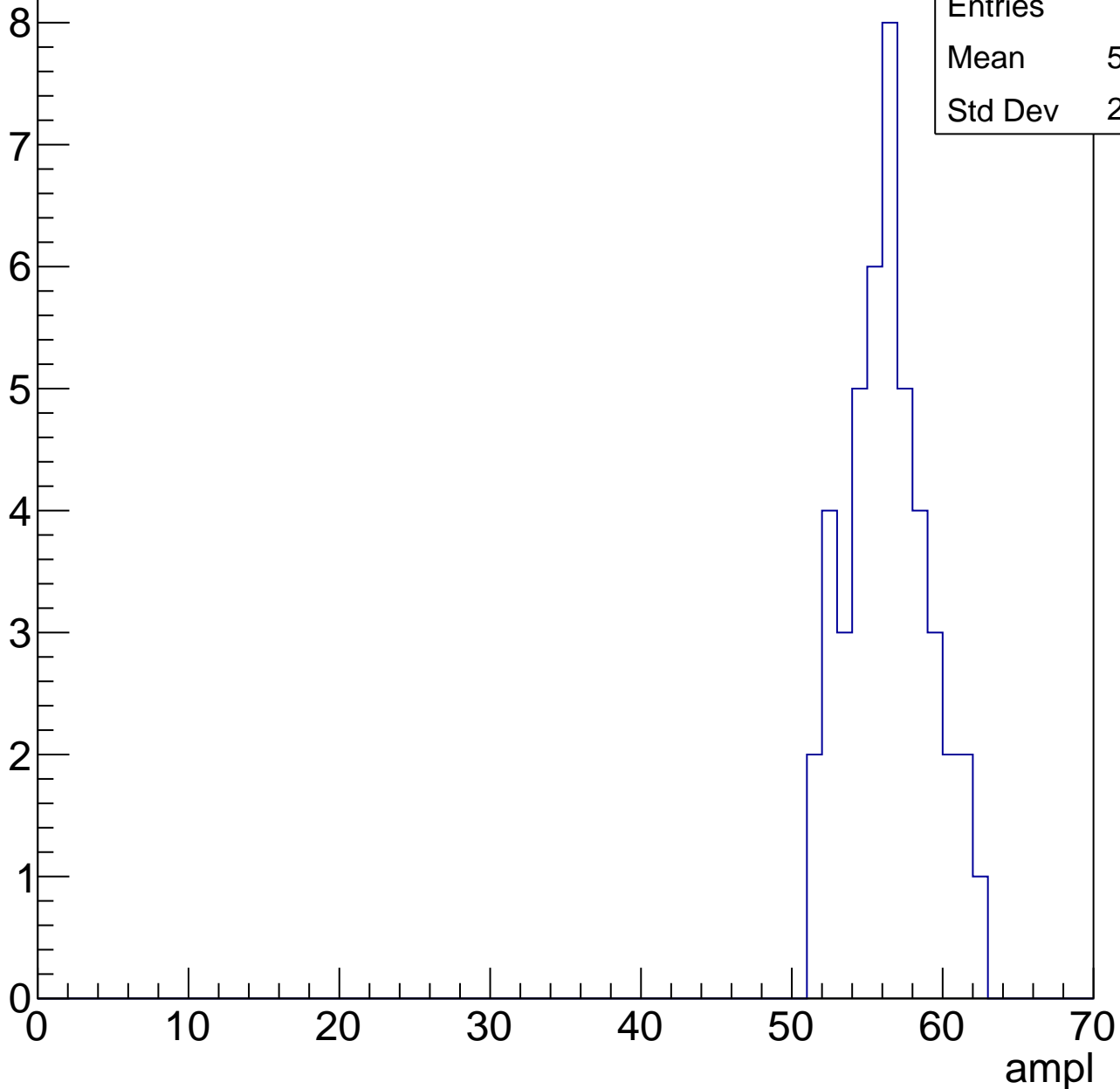


# B1L101S, U18-ch24, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	45
Mean	55.89
Std Dev	2.718

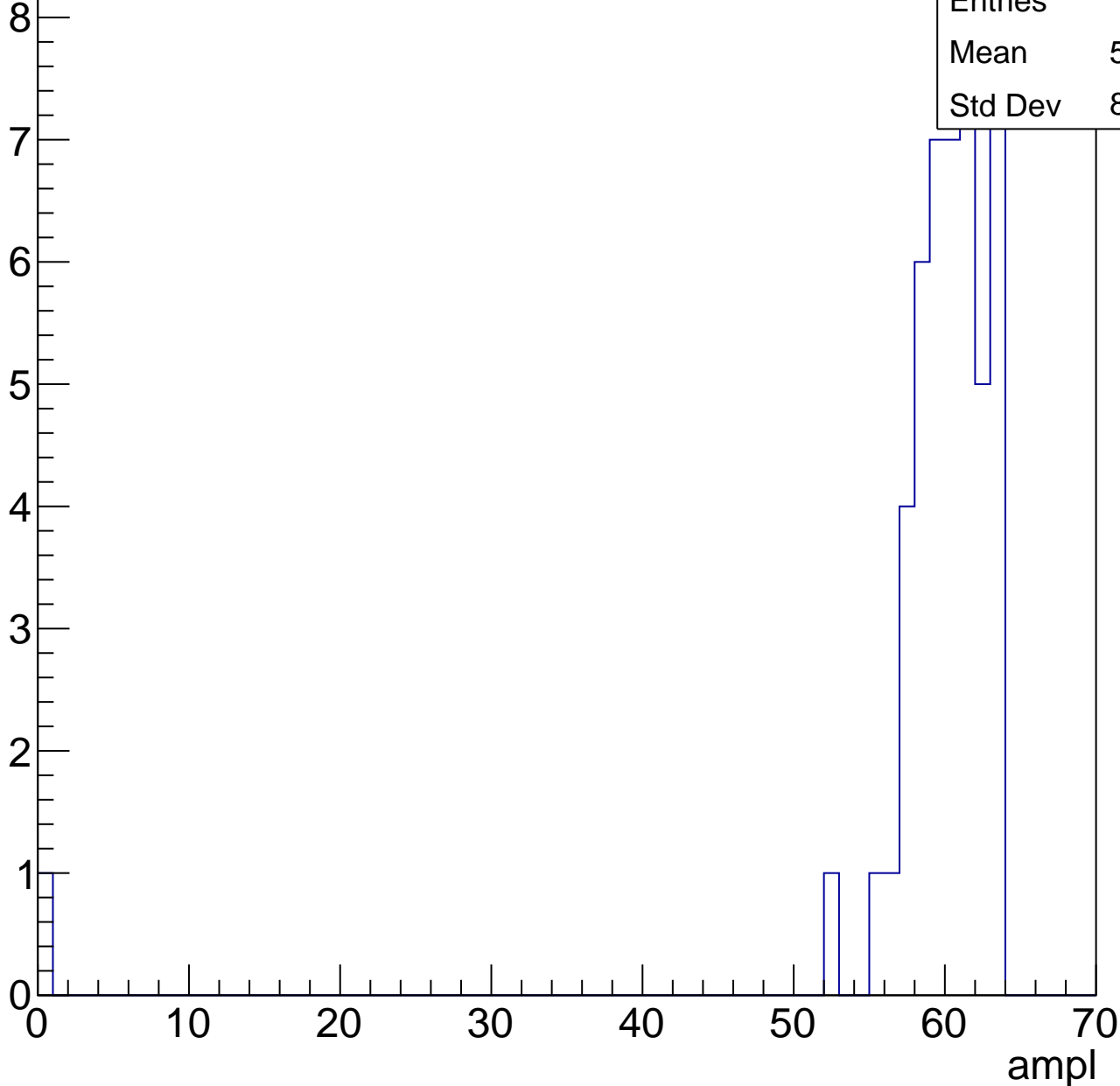


# B1L101S, U18-ch24, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

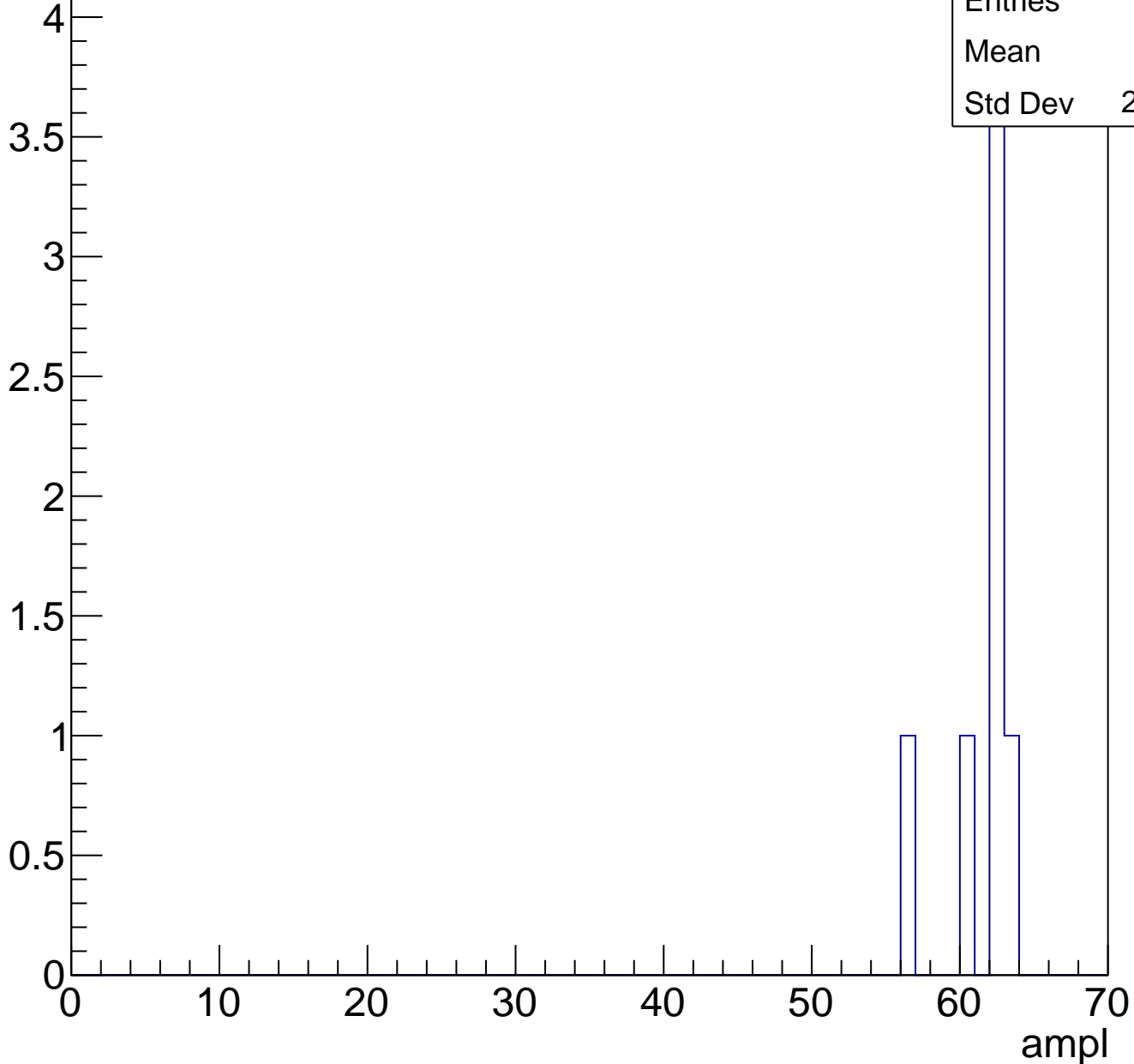
Entries	49
Mean	58.65
Std Dev	8.787



# B1L101S, U18-ch24, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch24, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch25, adc0

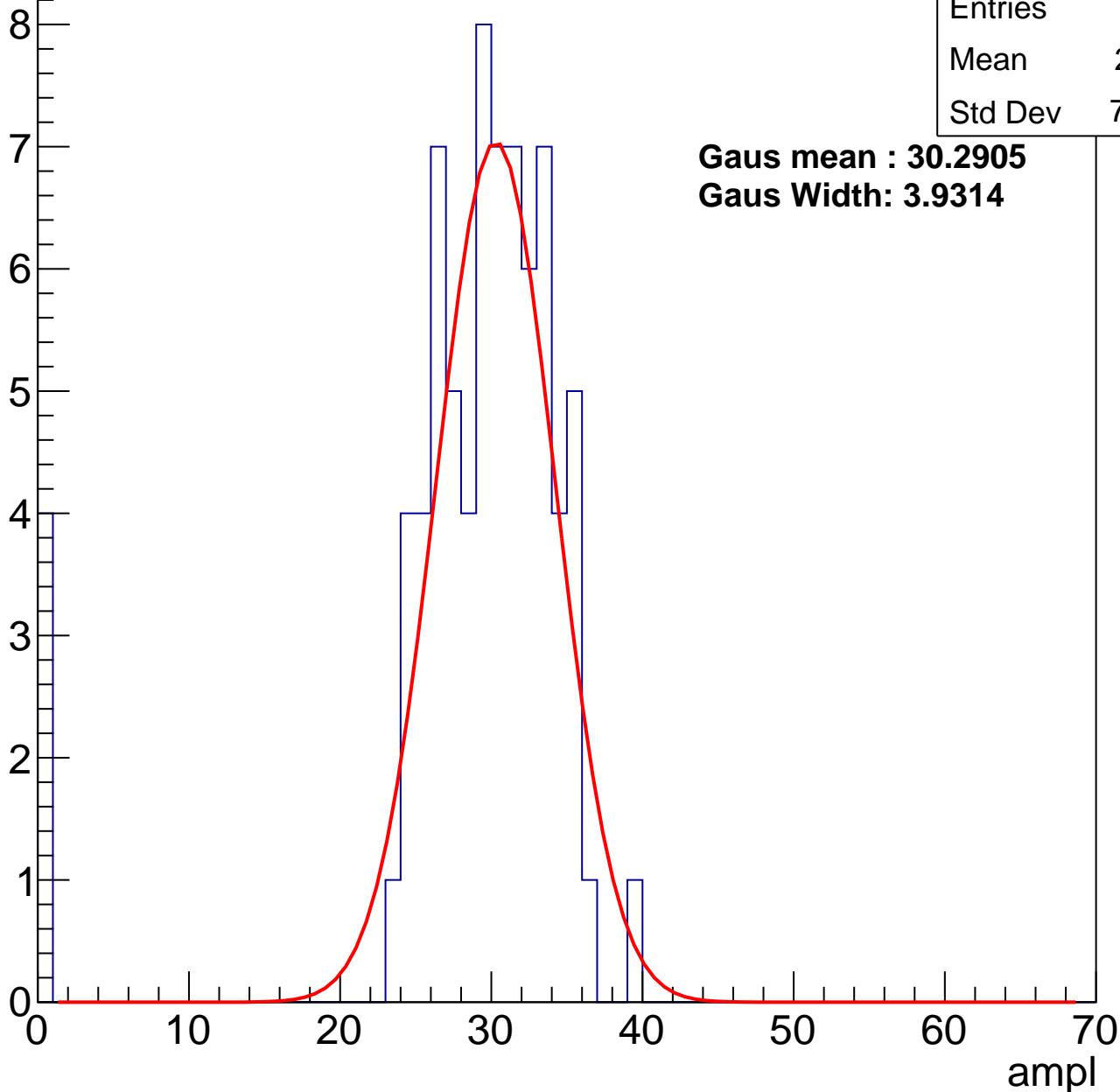
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	28.21
Std Dev	7.514

**Gaus mean : 30.2905**

**Gaus Width: 3.9314**



# B1L101S, U18-ch25, adc1

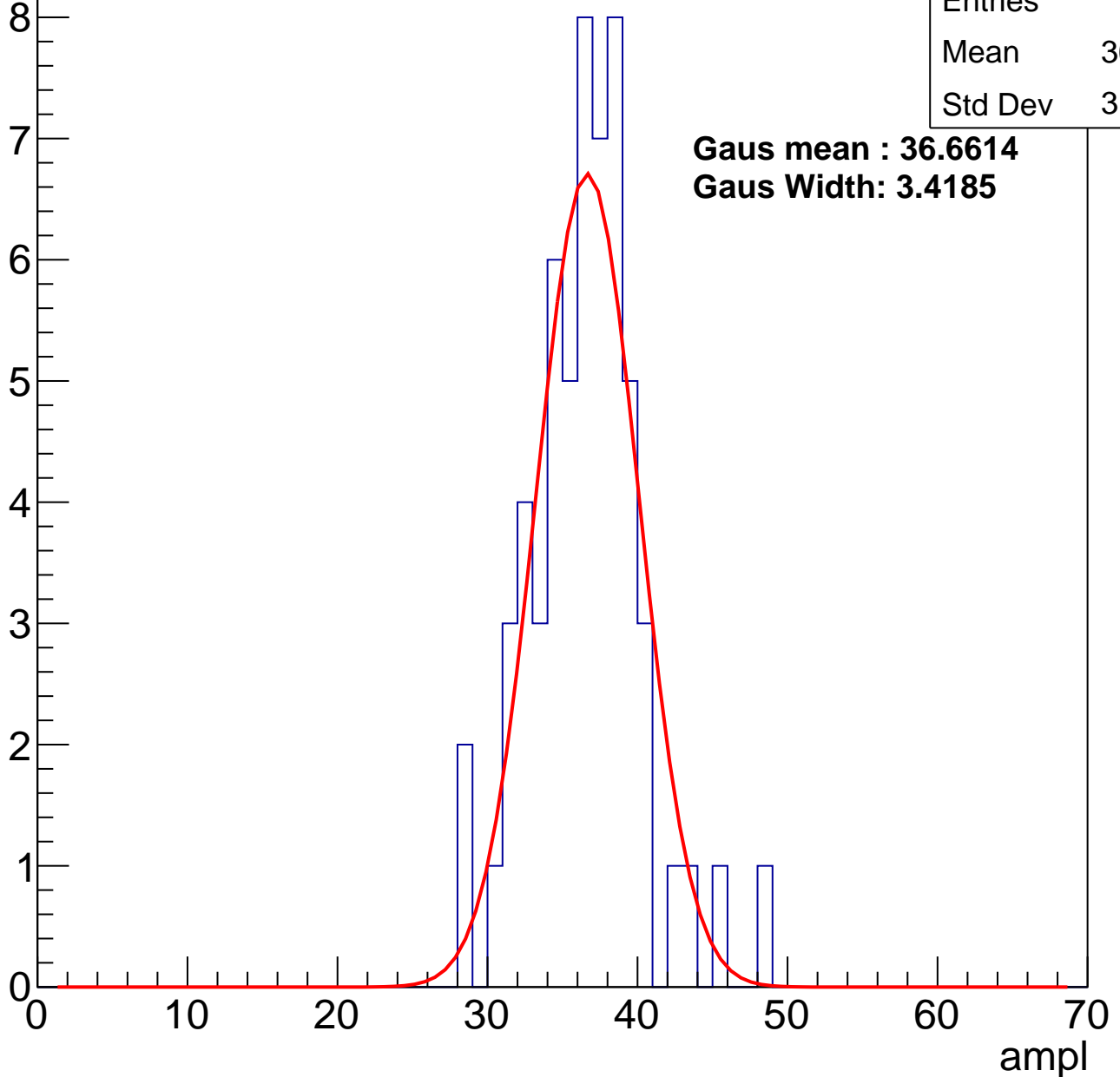
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	36.08
Std Dev	3.684

**Gaus mean : 36.6614**

**Gaus Width: 3.4185**



# B1L101S, U18-ch25, adc2

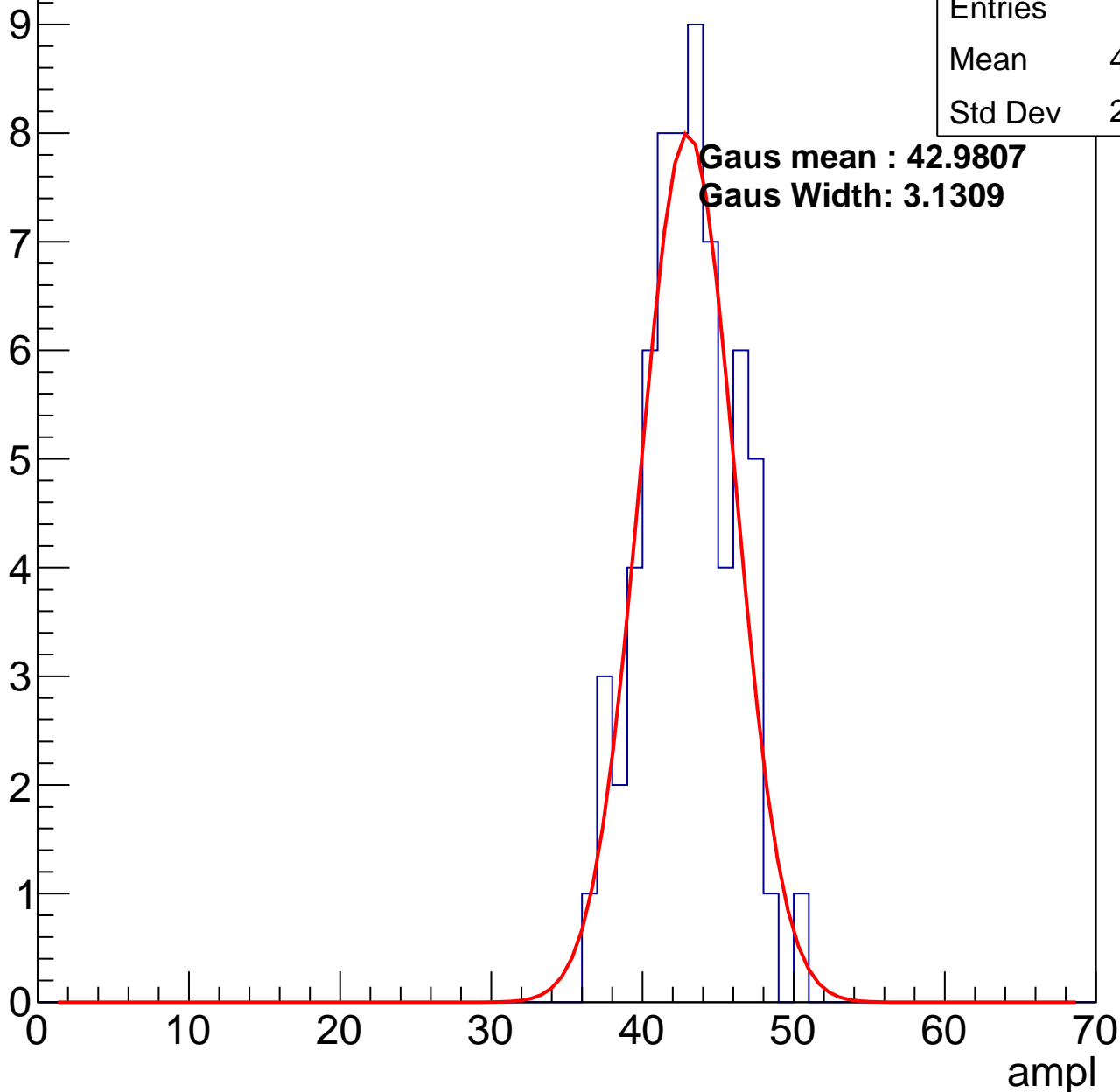
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	42.57
Std Dev	2.997

**Gaus mean : 42.9807**

**Gaus Width: 3.1309**



# B1L101S, U18-ch25, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

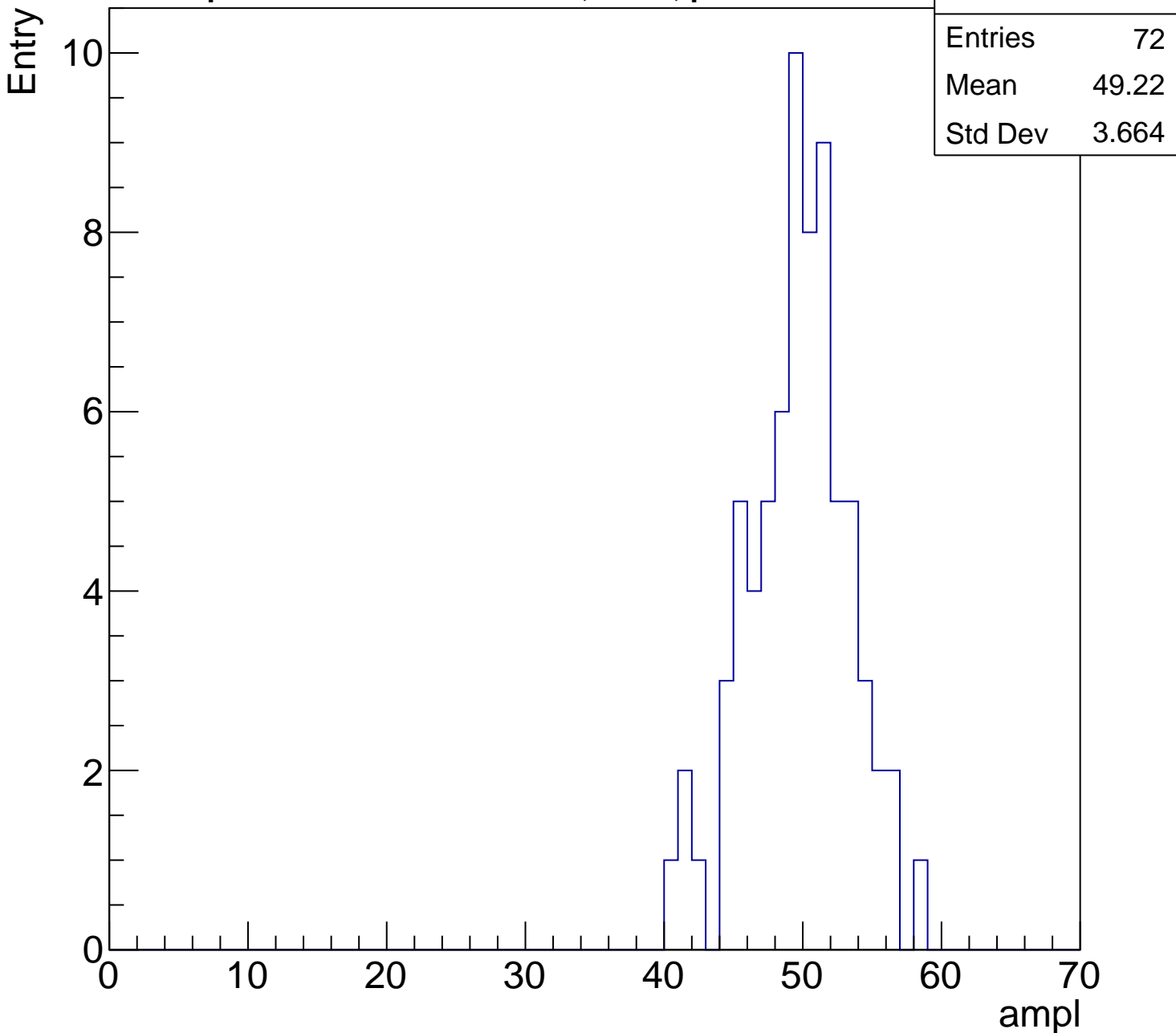
Entries	72
Mean	49.22
Std Dev	3.664

Entry

10  
8  
6  
4  
2  
0

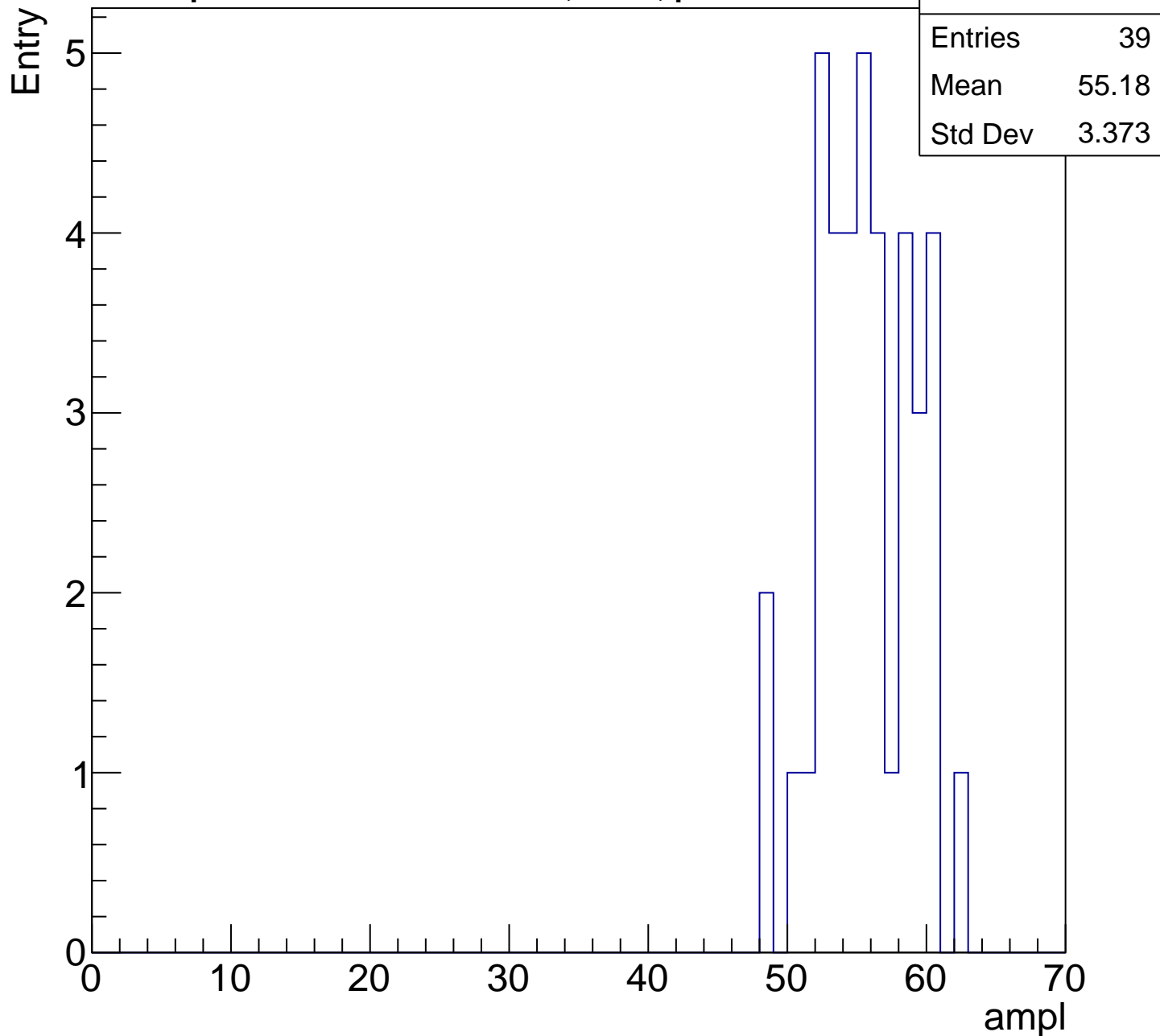
0 10 20 30 40 50 60 70

ampl



# B1L101S, U18-ch25, adc4

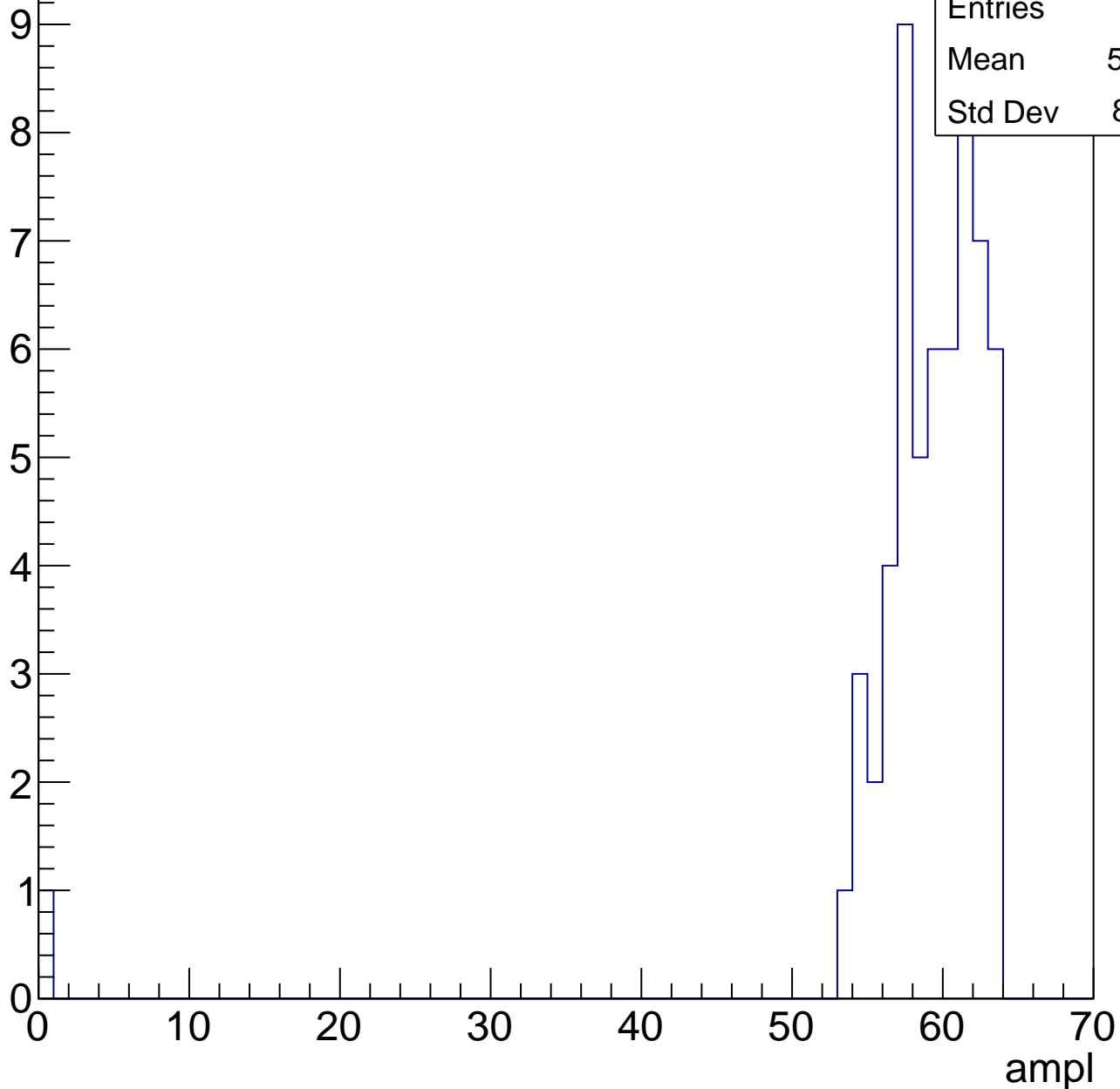
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U18-ch25, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

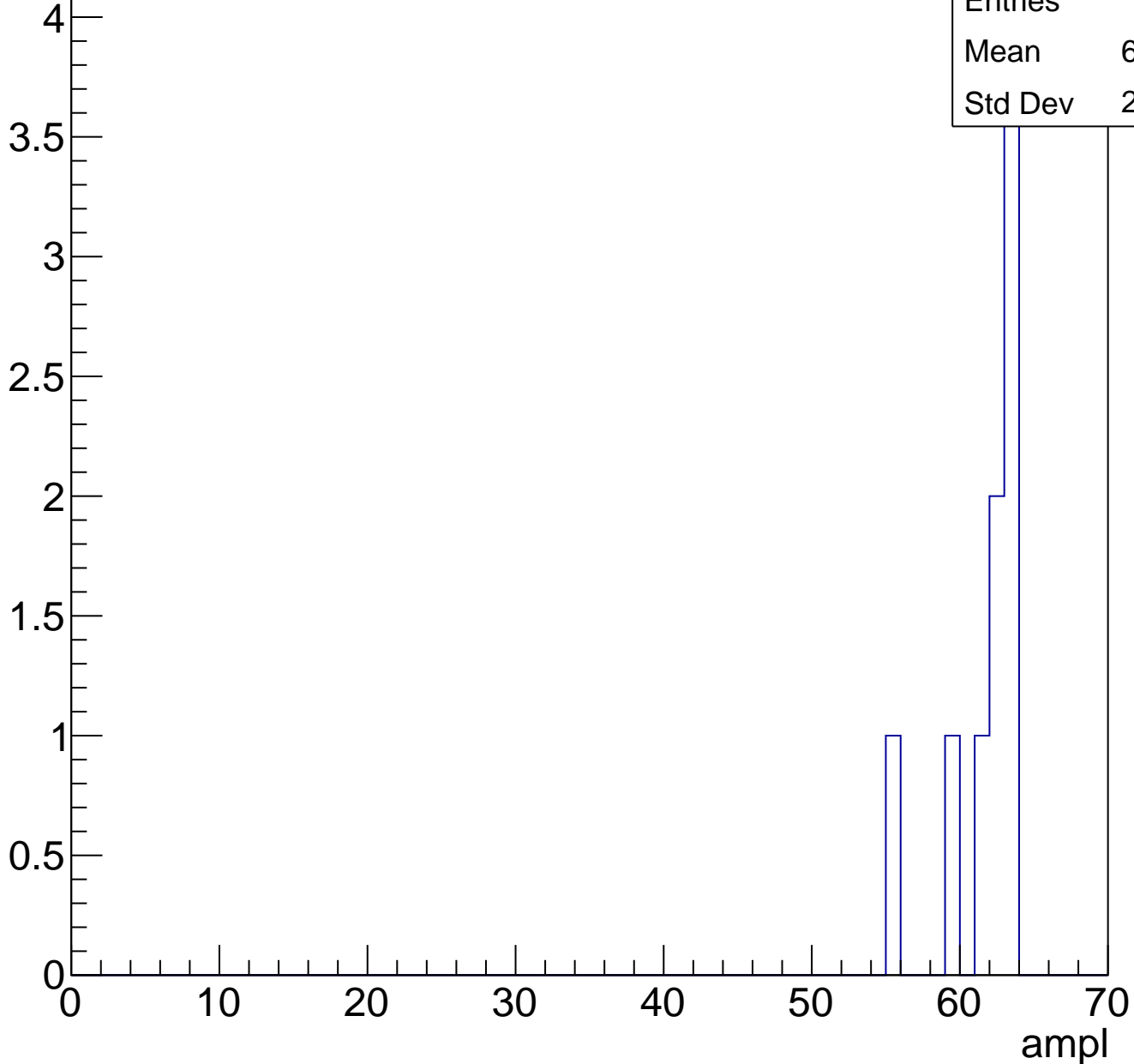
Entry



# B1L101S, U18-ch25, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

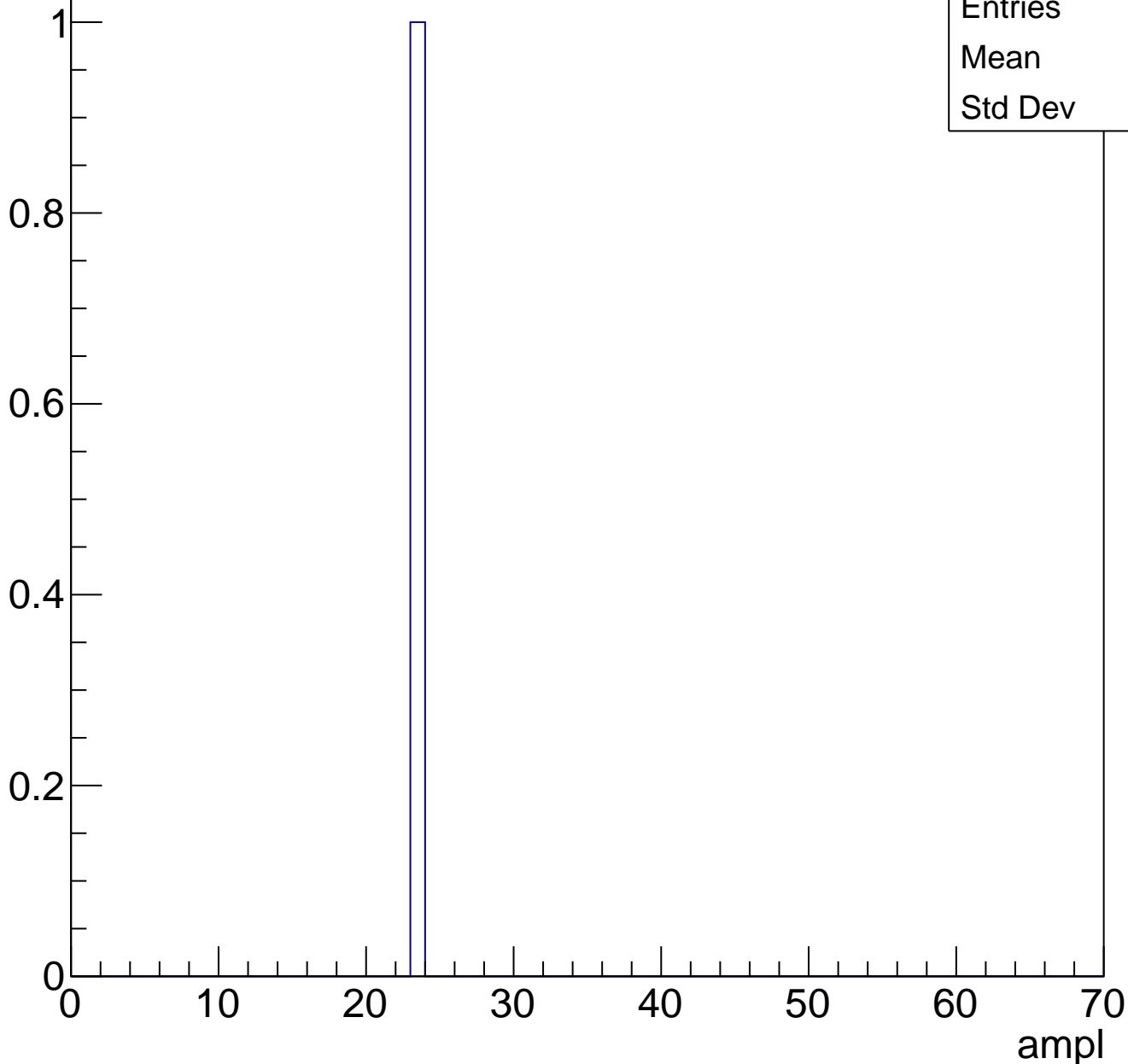




# B1L101S, U18-ch25, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch26, adc0

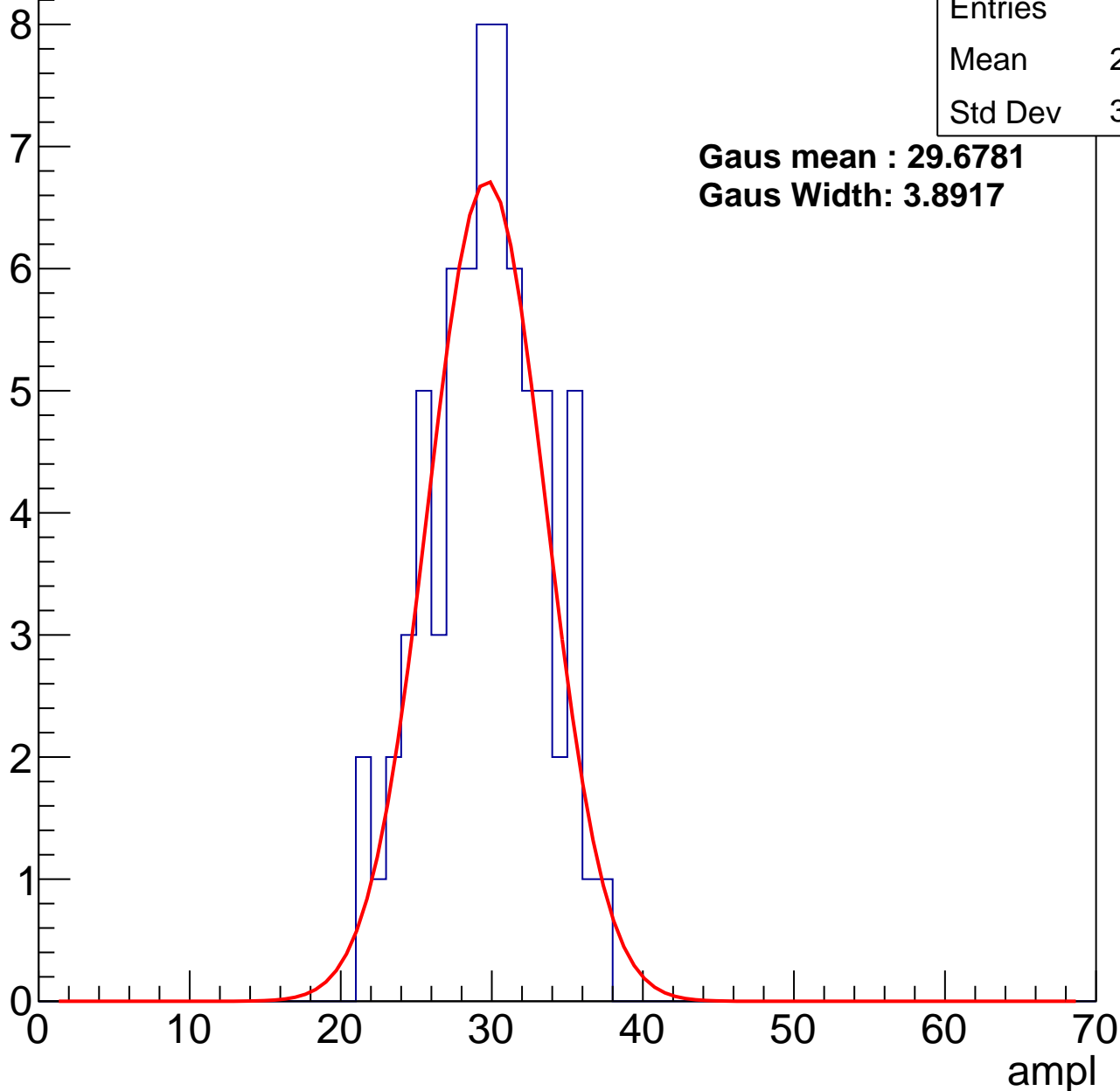
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	29.19
Std Dev	3.727

**Gaus mean : 29.6781**

**Gaus Width: 3.8917**



# B1L101S, U18-ch26, adc1

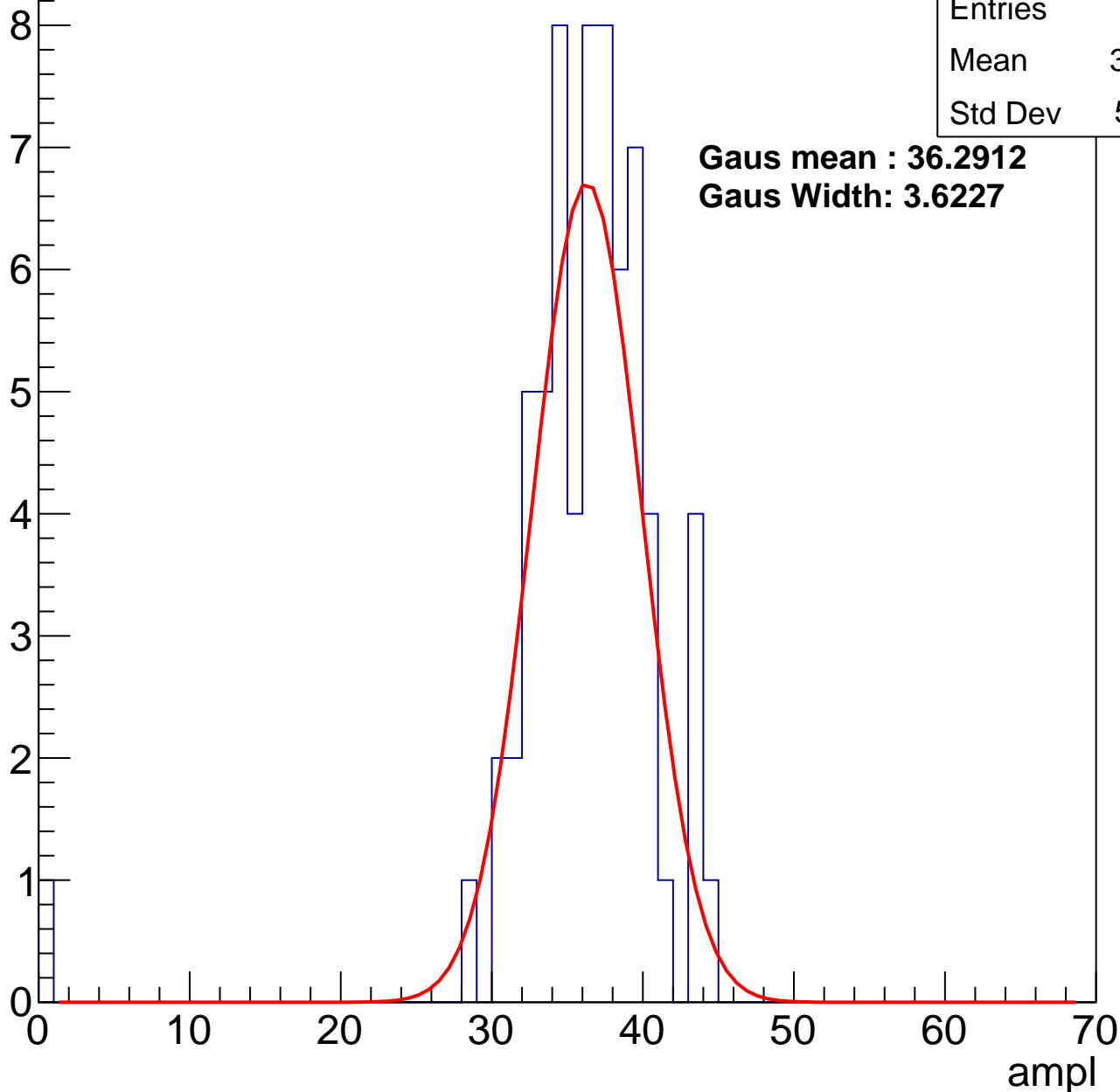
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	35.66
Std Dev	5.571

**Gaus mean : 36.2912**

**Gaus Width: 3.6227**



# B1L101S, U18-ch26, adc2

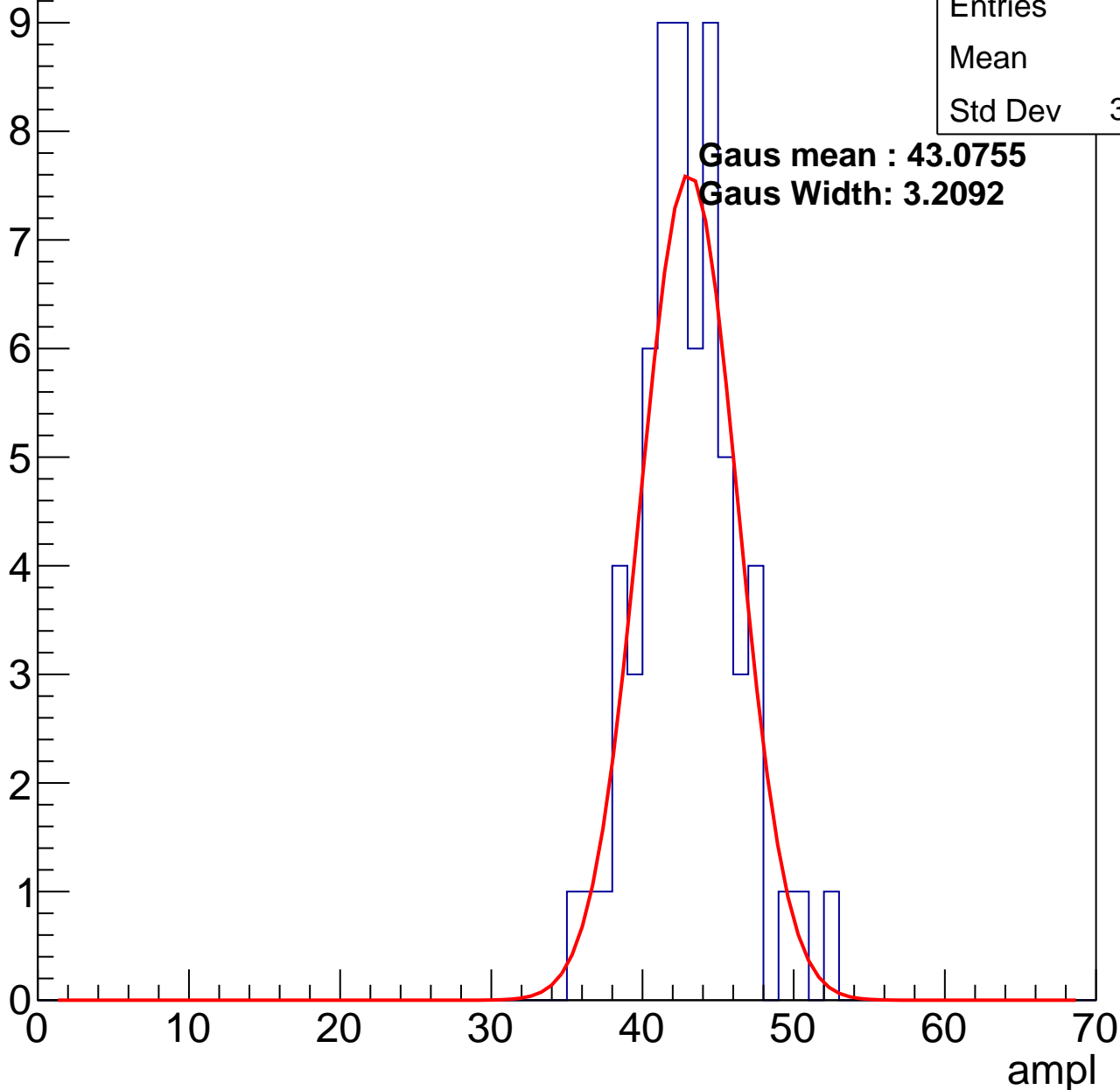
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	42.5
Std Dev	3.226

**Gaus mean : 43.0755**

**Gaus Width: 3.2092**

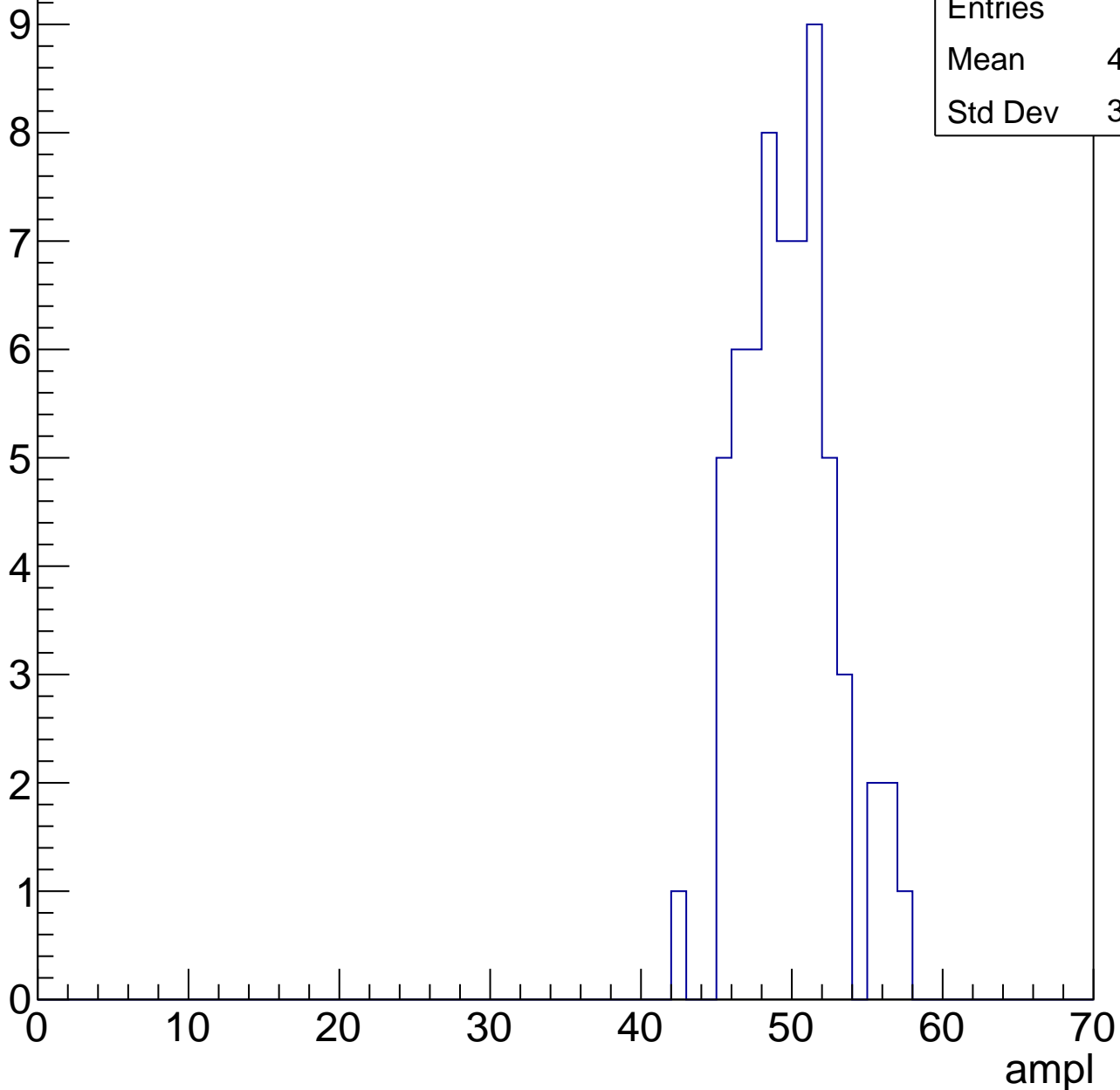


# B1L101S, U18-ch26, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	49.34
Std Dev	3.053

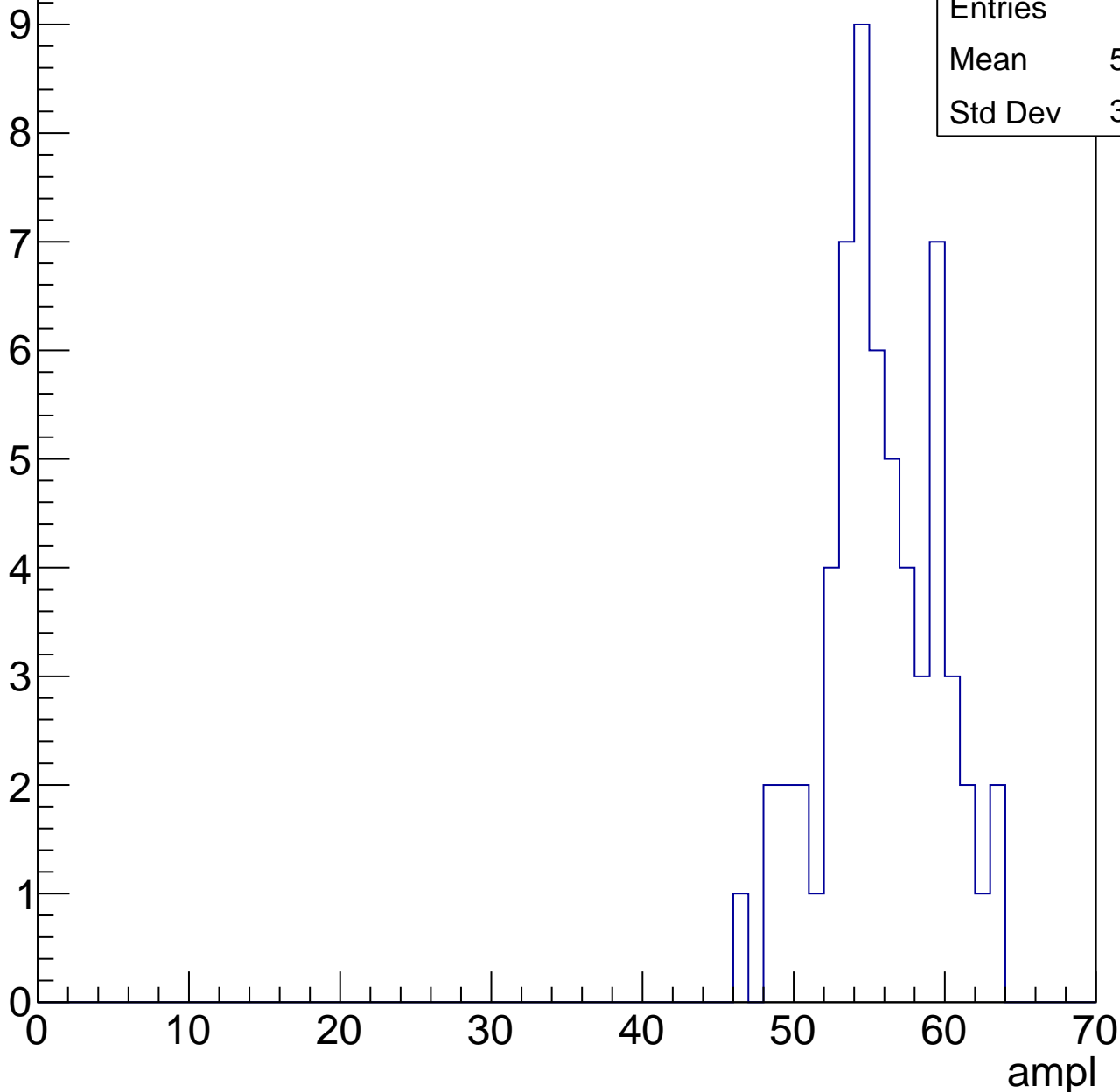


# B1L101S, U18-ch26, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	55.26
Std Dev	3.776



# B1L101S, U18-ch26, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

7

6

5

4

3

2

1

0

Entries 43

Mean 58

Std Dev 9.276

ampl

0

10

20

30

40

50

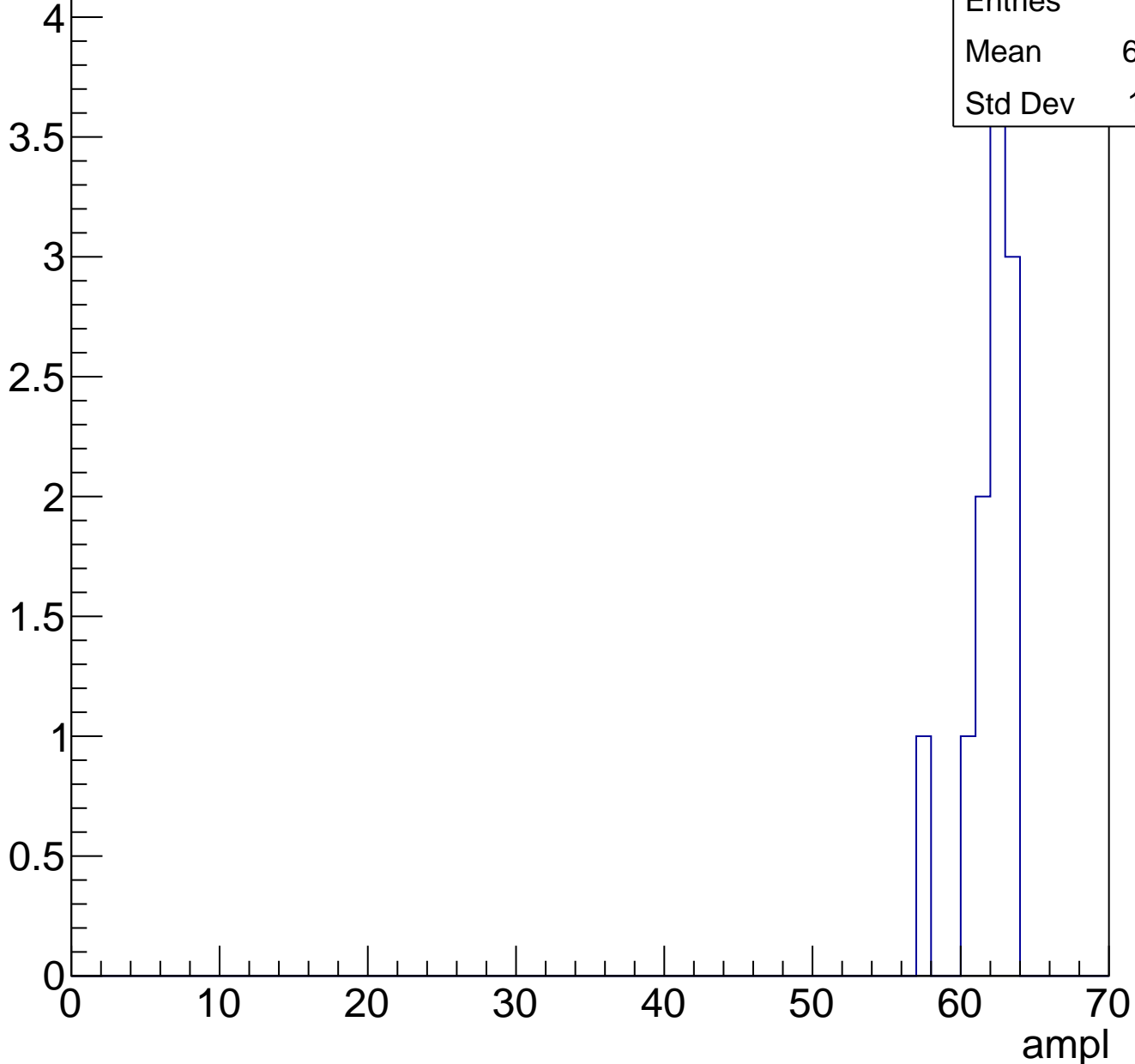
60

70

# B1L101S, U18-ch26, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch26, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U18-ch27, adc0

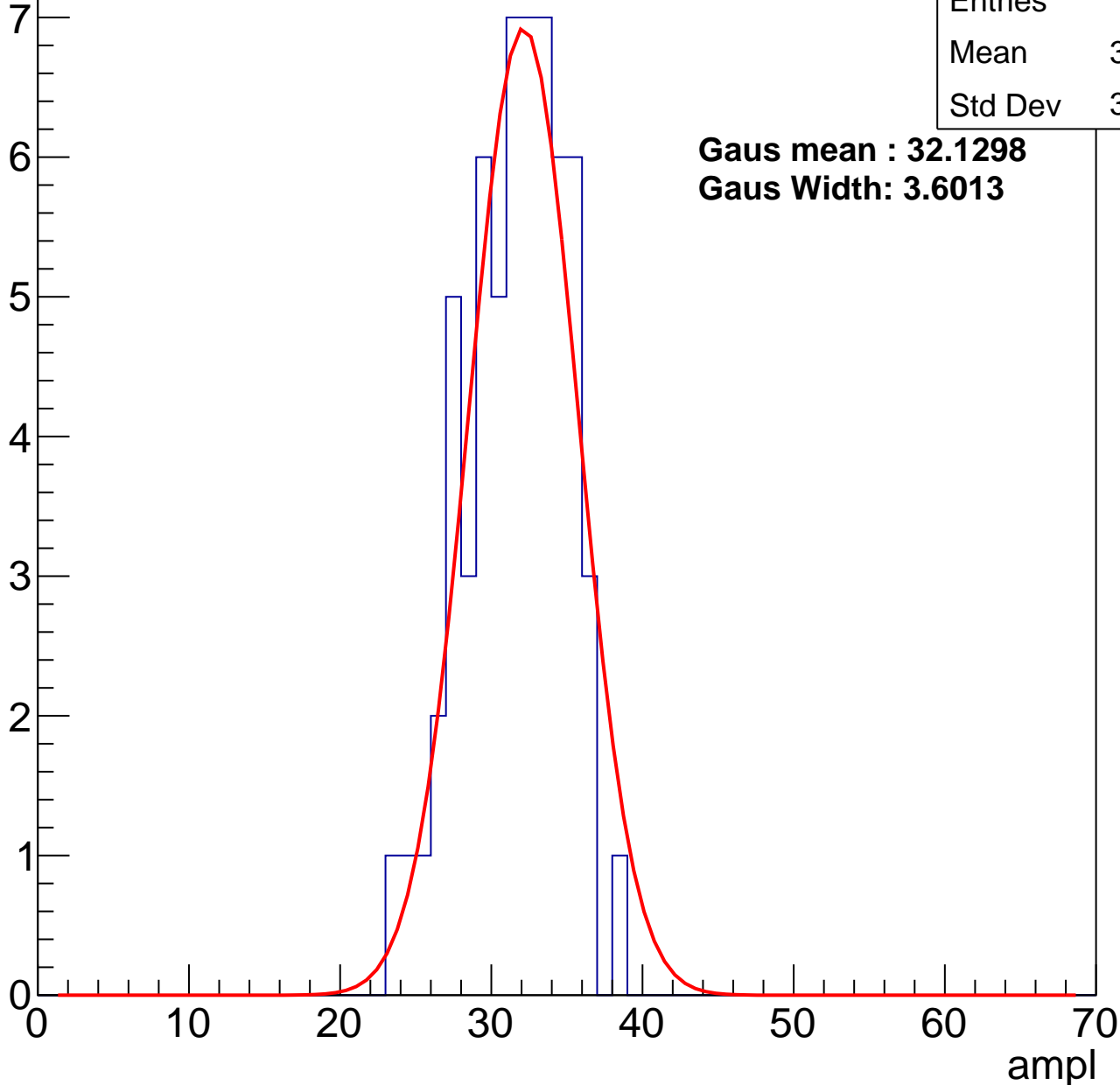
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	31.13
Std Dev	3.247

**Gaus mean : 32.1298**

**Gaus Width: 3.6013**

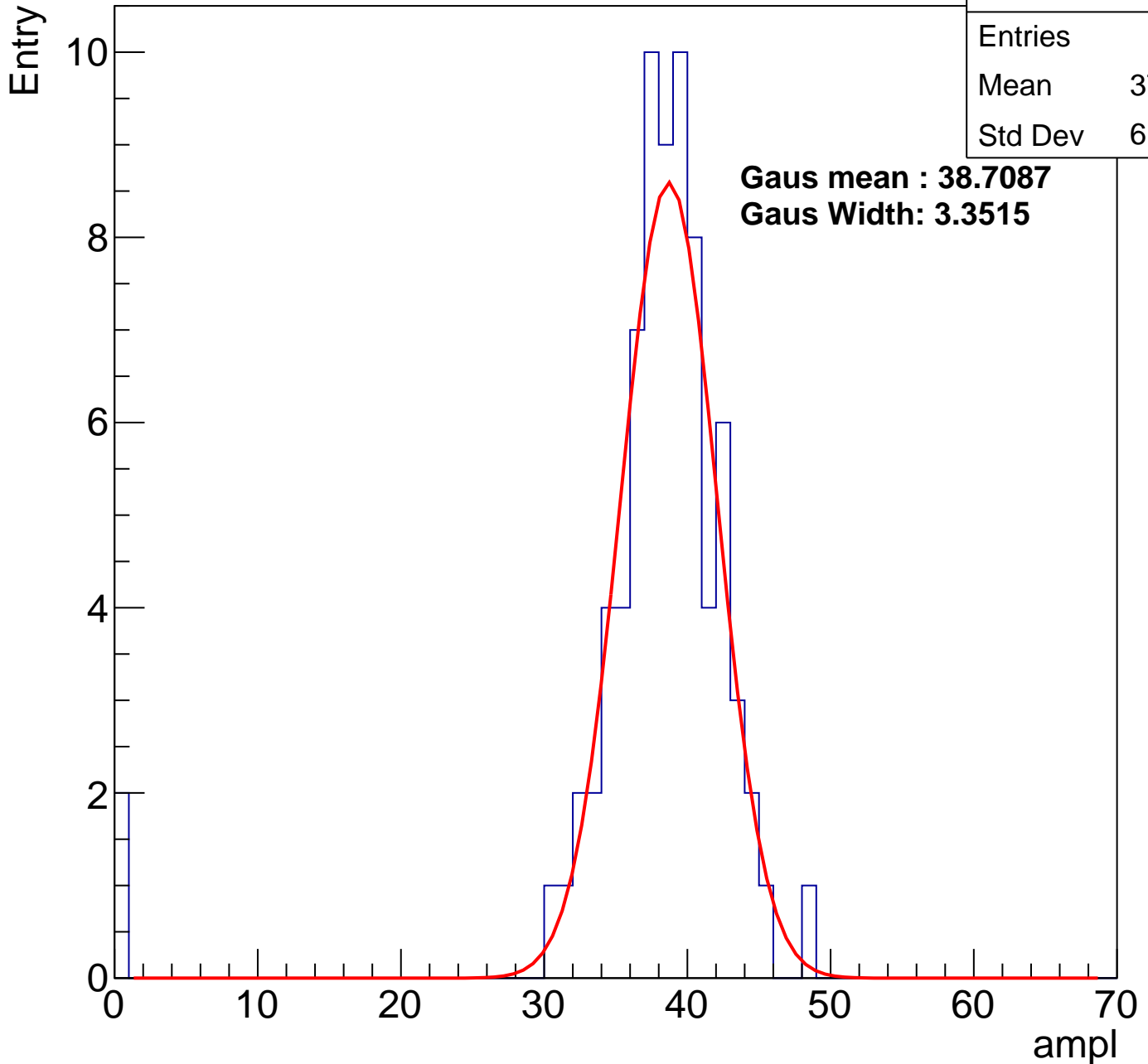


# B1L101S, U18-ch27, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

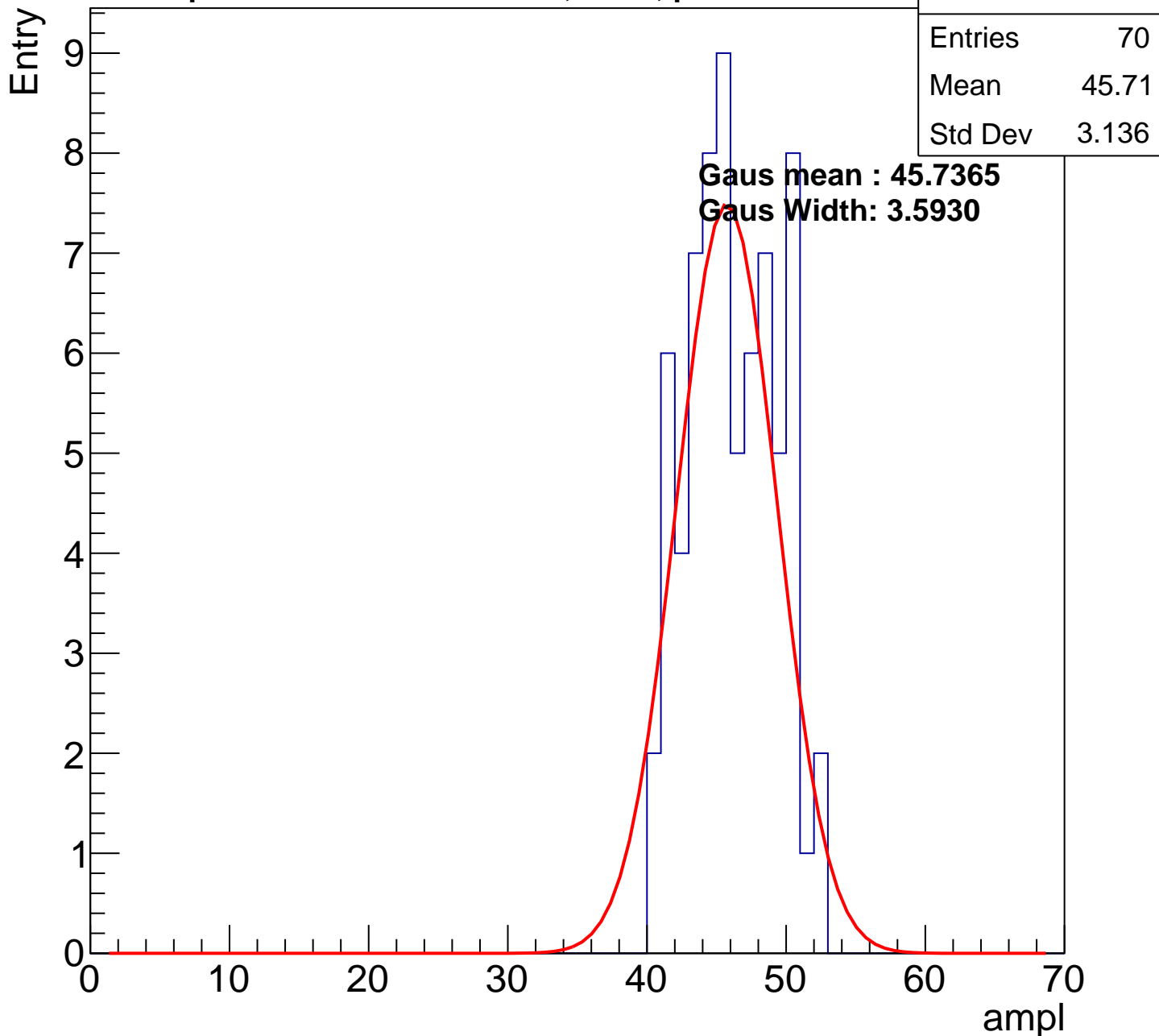
Entries	77
Mean	37.23
Std Dev	6.919

**Gaus mean : 38.7087**  
**Gaus Width: 3.3515**



# B1L101S, U18-ch27, adc2

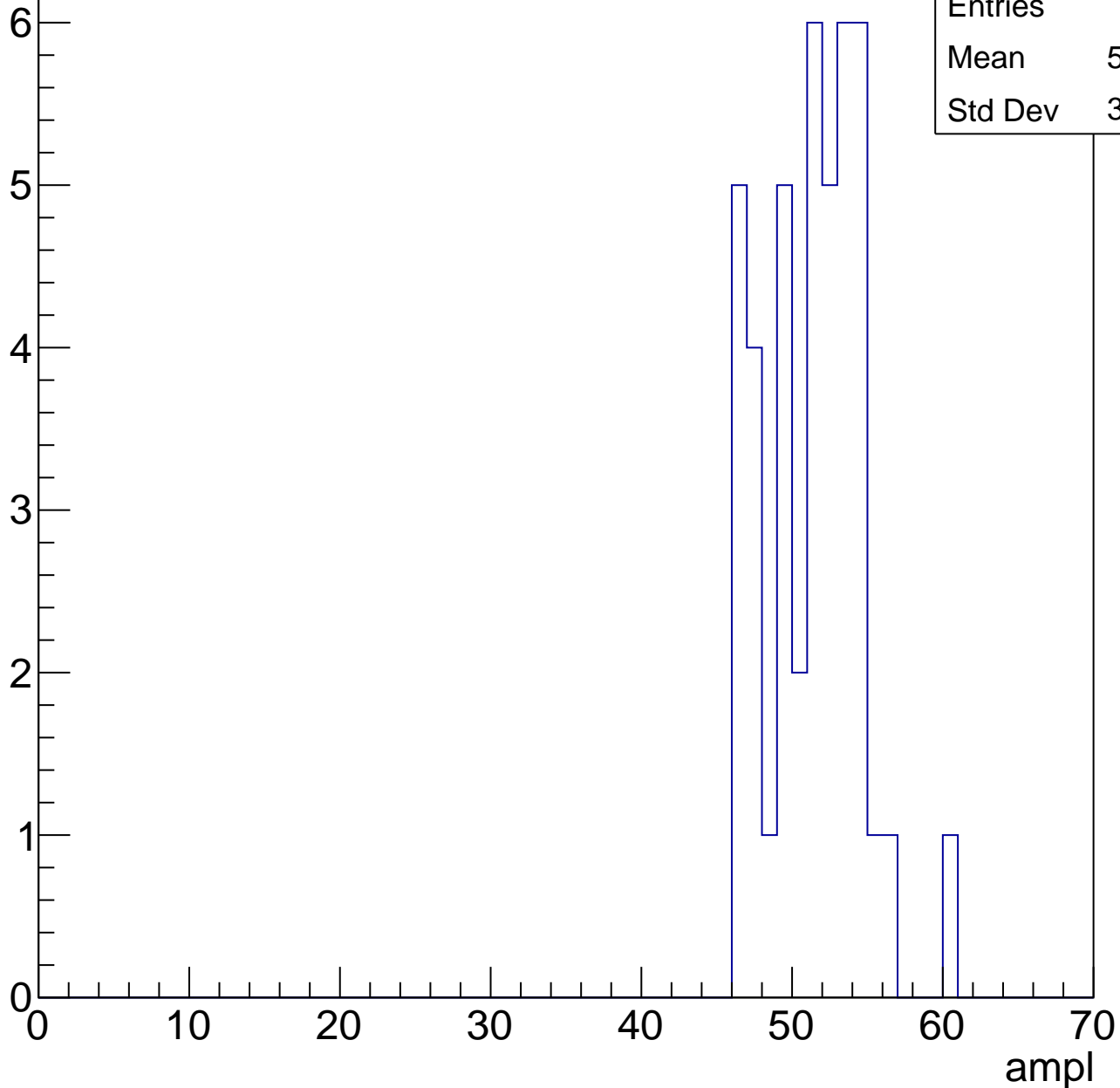
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U18-ch27, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



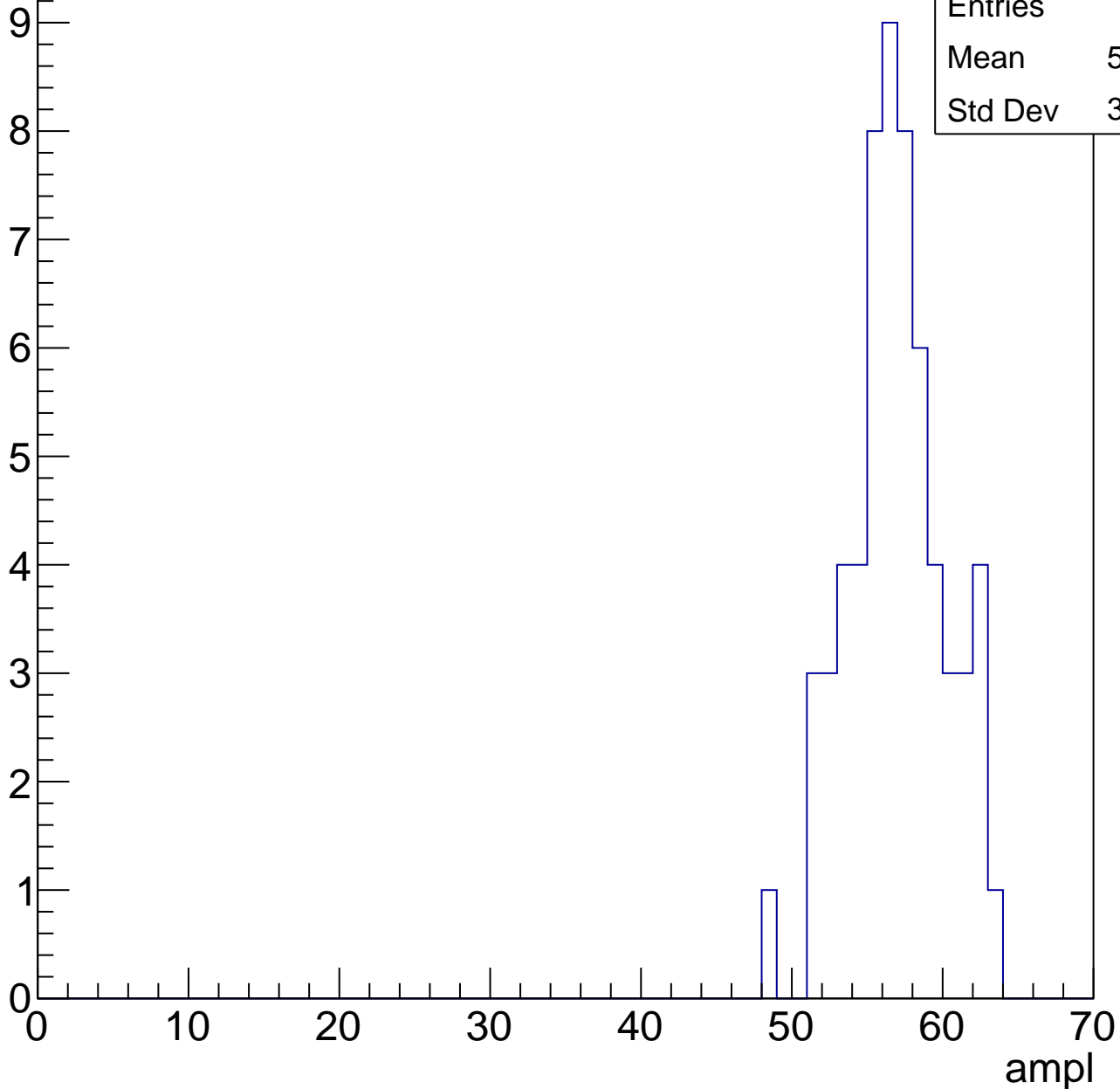
Entries	43
Mean	50.93
Std Dev	3.143

# B1L101S, U18-ch27, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	56.44
Std Dev	3.186

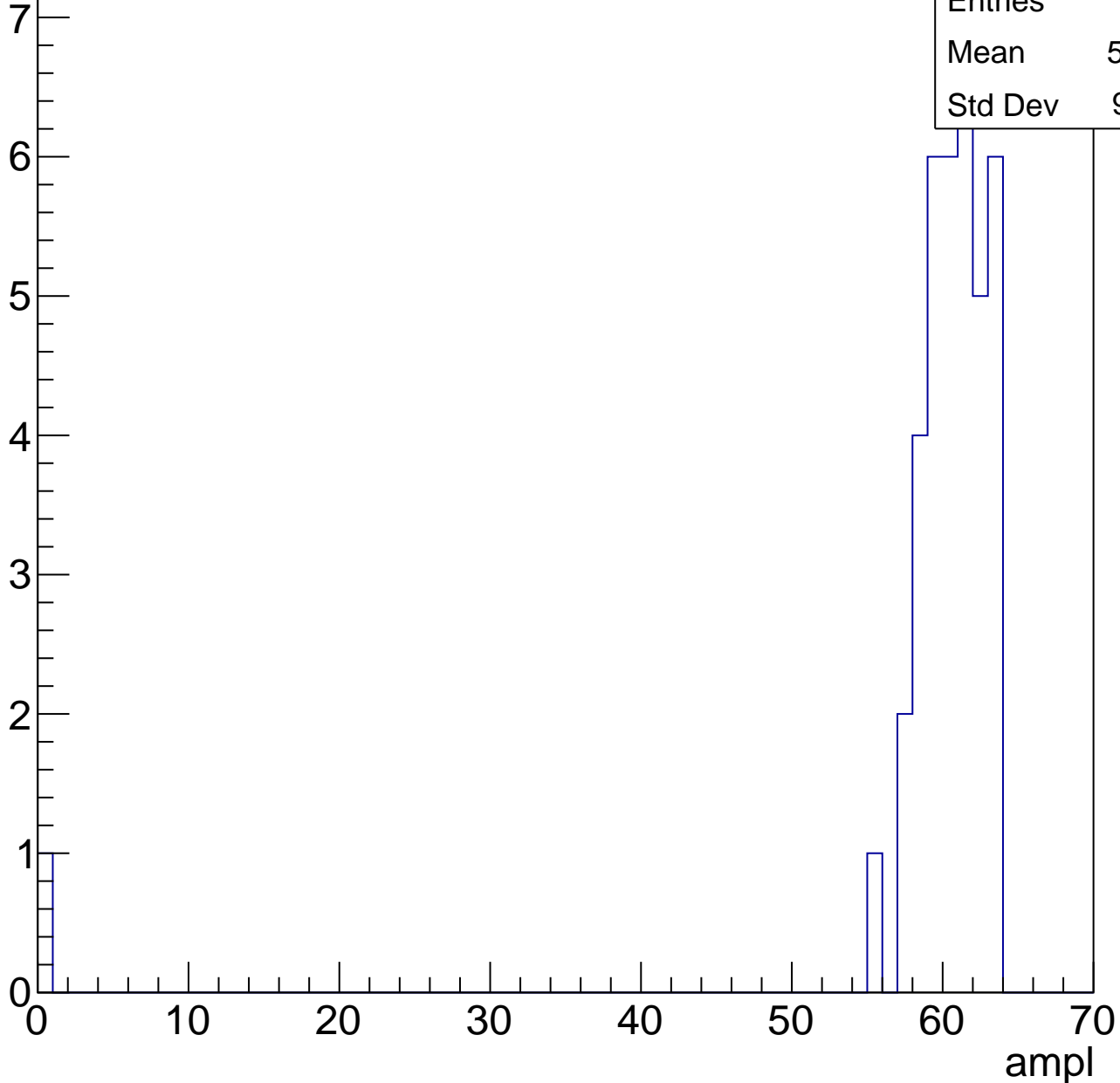


# B1L101S, U18-ch27, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	38
Mean	58.68
Std Dev	9.841



# B1L101S, U18-ch27, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch27, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U18-ch28, adc0

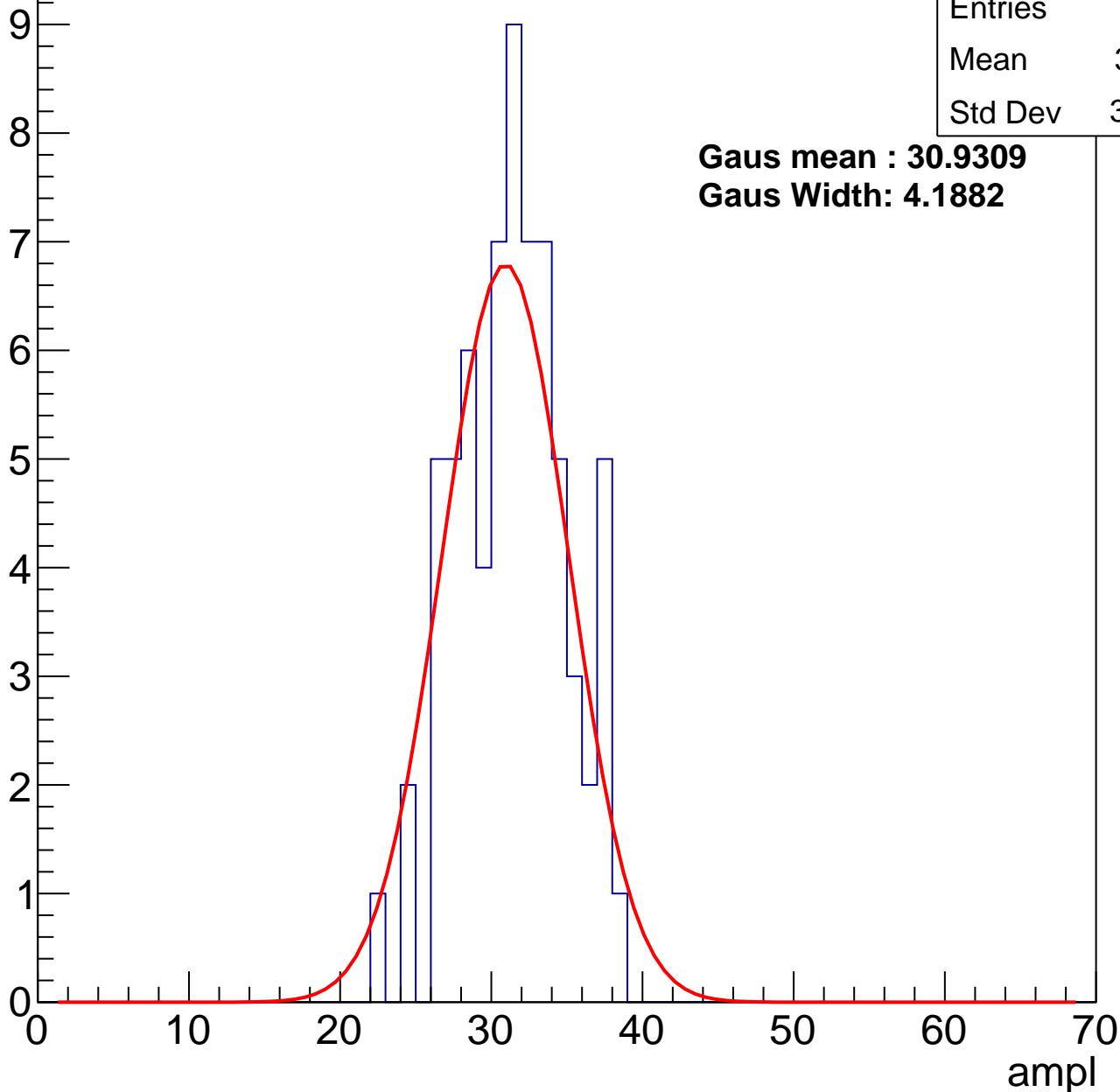
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	30.91
Std Dev	3.546

**Gaus mean : 30.9309**

**Gaus Width: 4.1882**



# B1L101S, U18-ch28, adc1

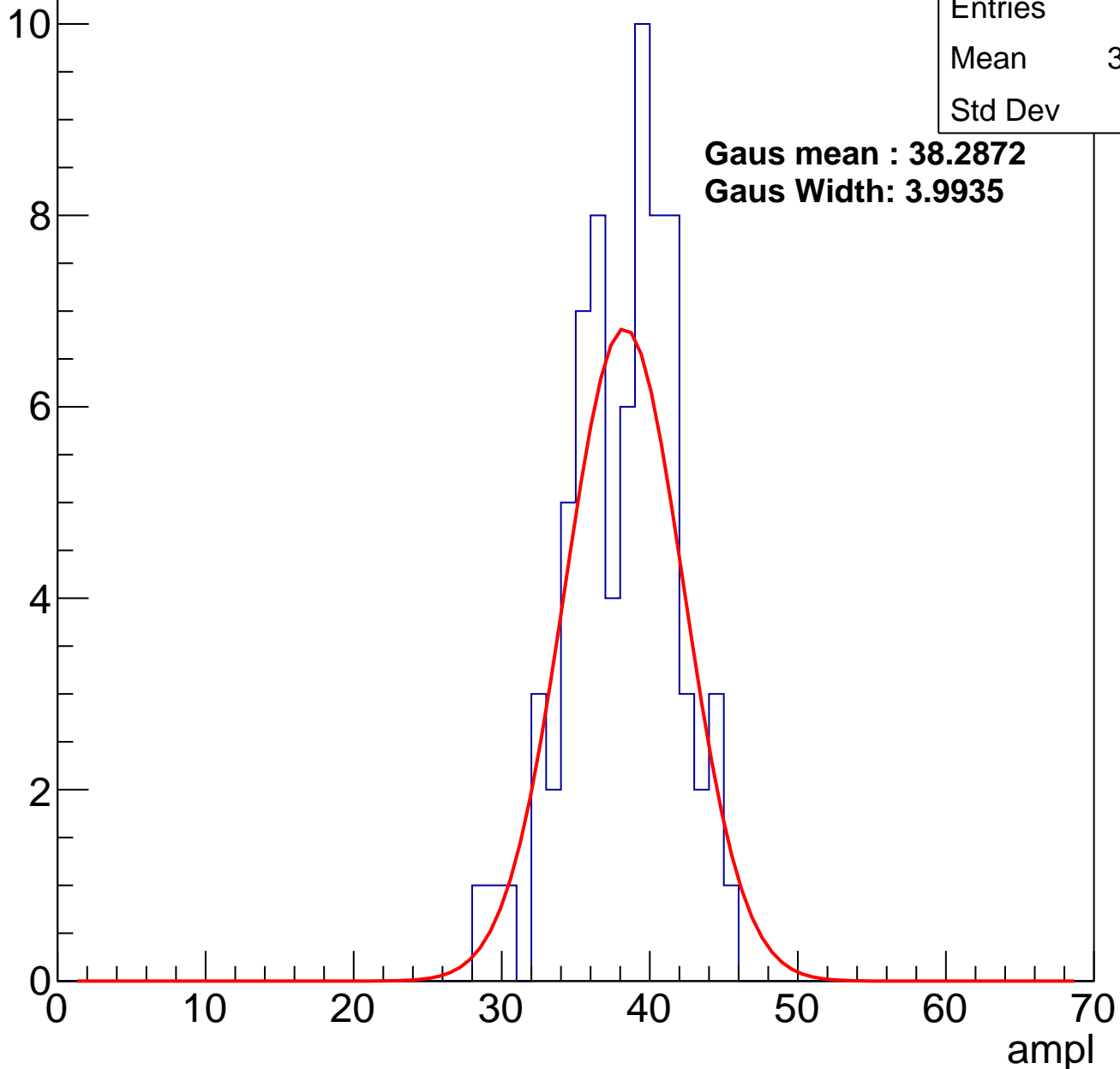
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	73
Mean	37.74
Std Dev	3.6

**Gaus mean : 38.2872**

**Gaus Width: 3.9935**

Entry



# B1L101S, U18-ch28, adc2

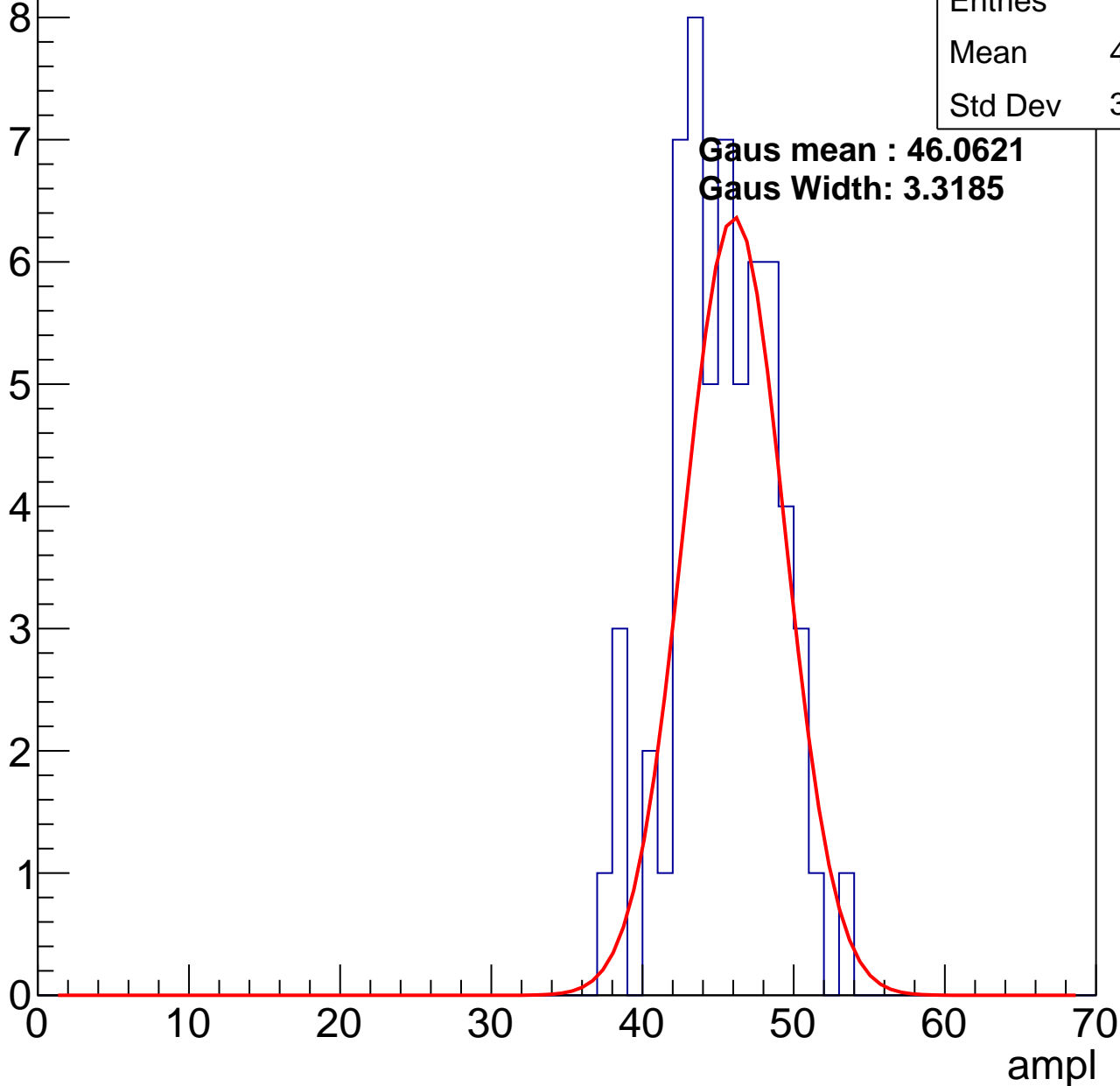
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	44.92
Std Dev	3.412

**Gaus mean : 46.0621**

**Gaus Width: 3.3185**

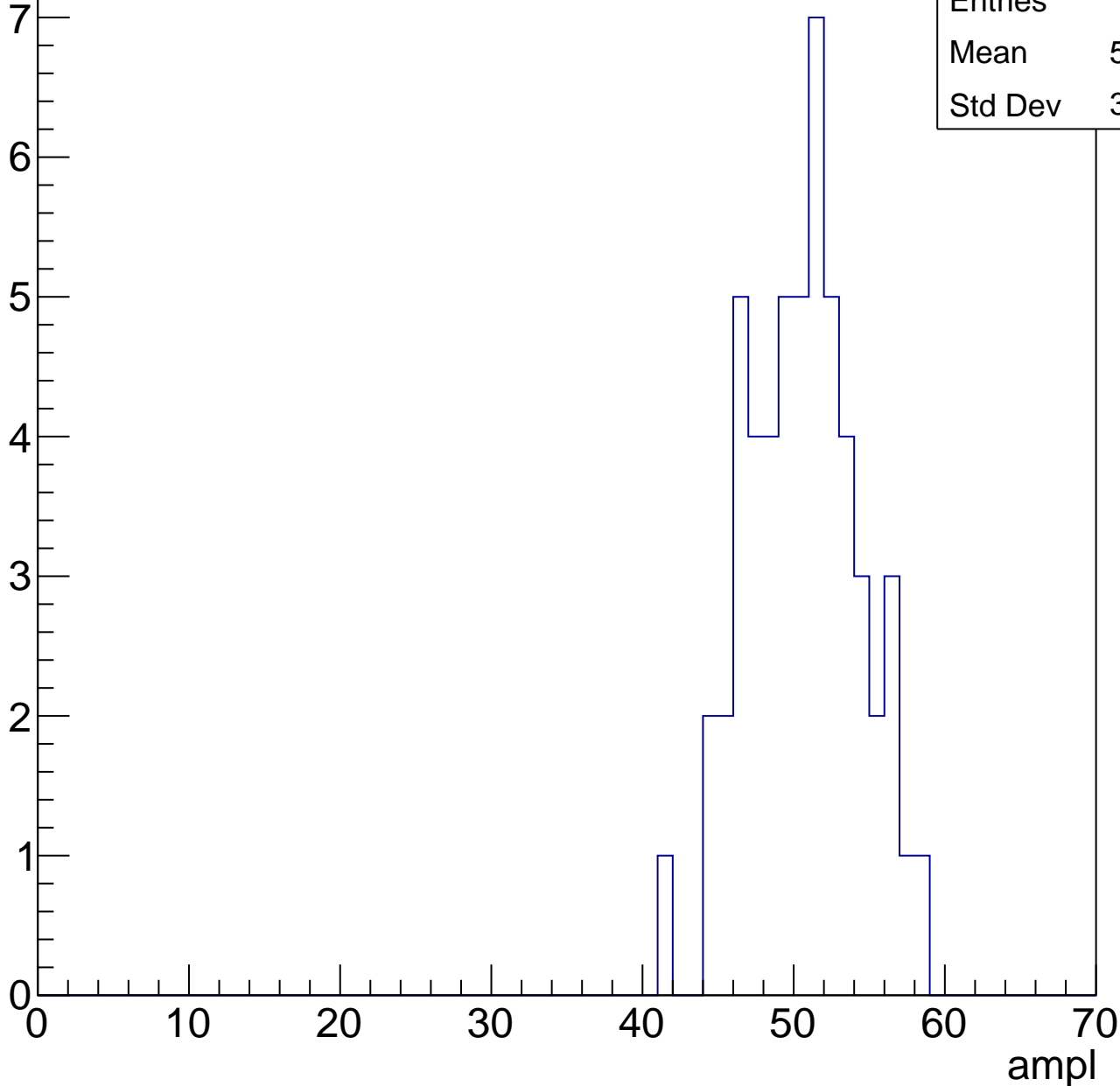


# B1L101S, U18-ch28, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	50.15
Std Dev	3.654

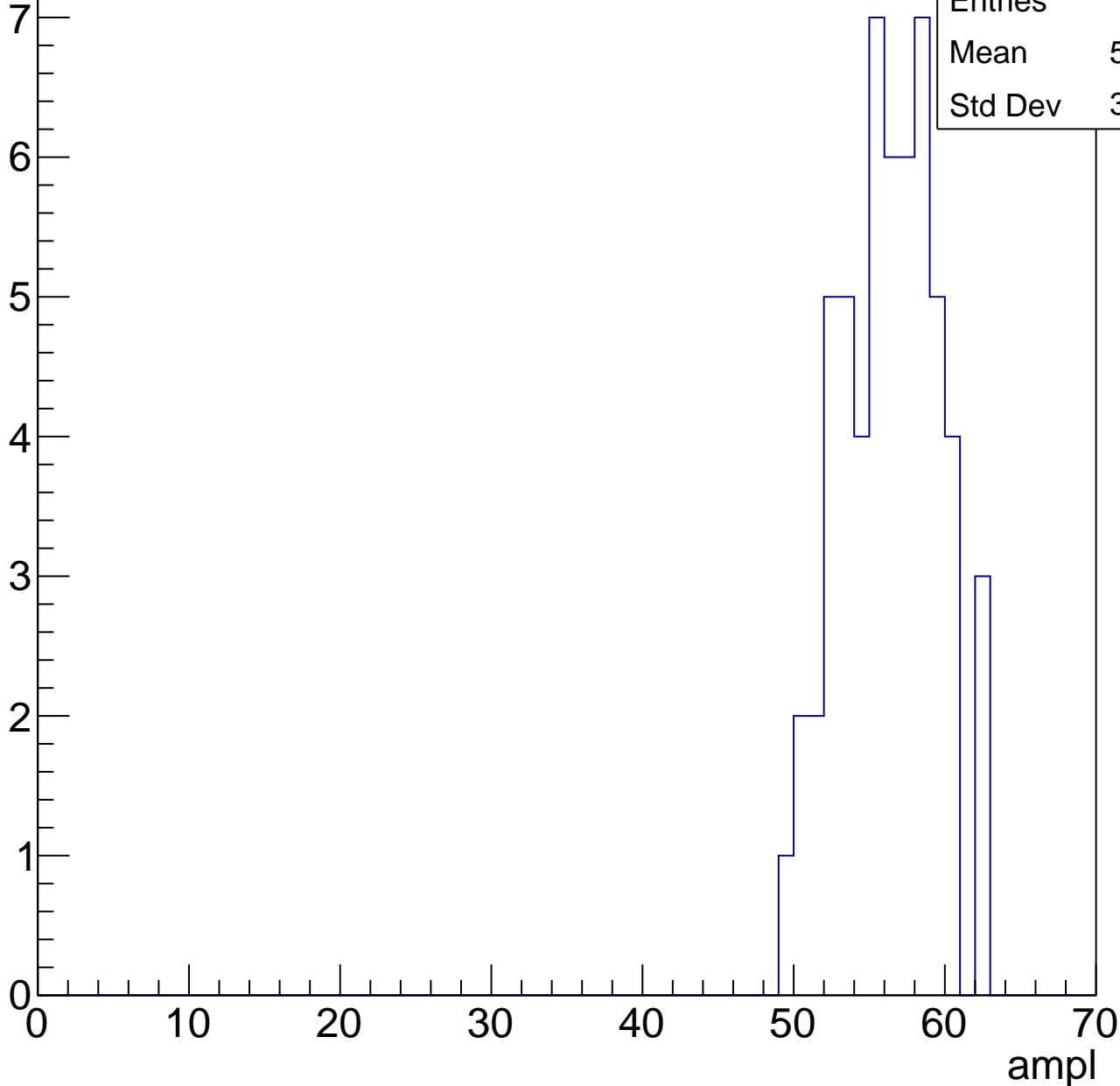


# B1L101S, U18-ch28, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	55.82
Std Dev	3.157



# B1L101S, U18-ch28, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

ampl

Entries	48
Mean	58.96
Std Dev	8.972

Entry

8

6

4

2

0

0

10

20

30

40

50

60

ampl

# B1L101S, U18-ch28, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	59
Std Dev	0



# B1L101S, U18-ch28, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch29, adc0

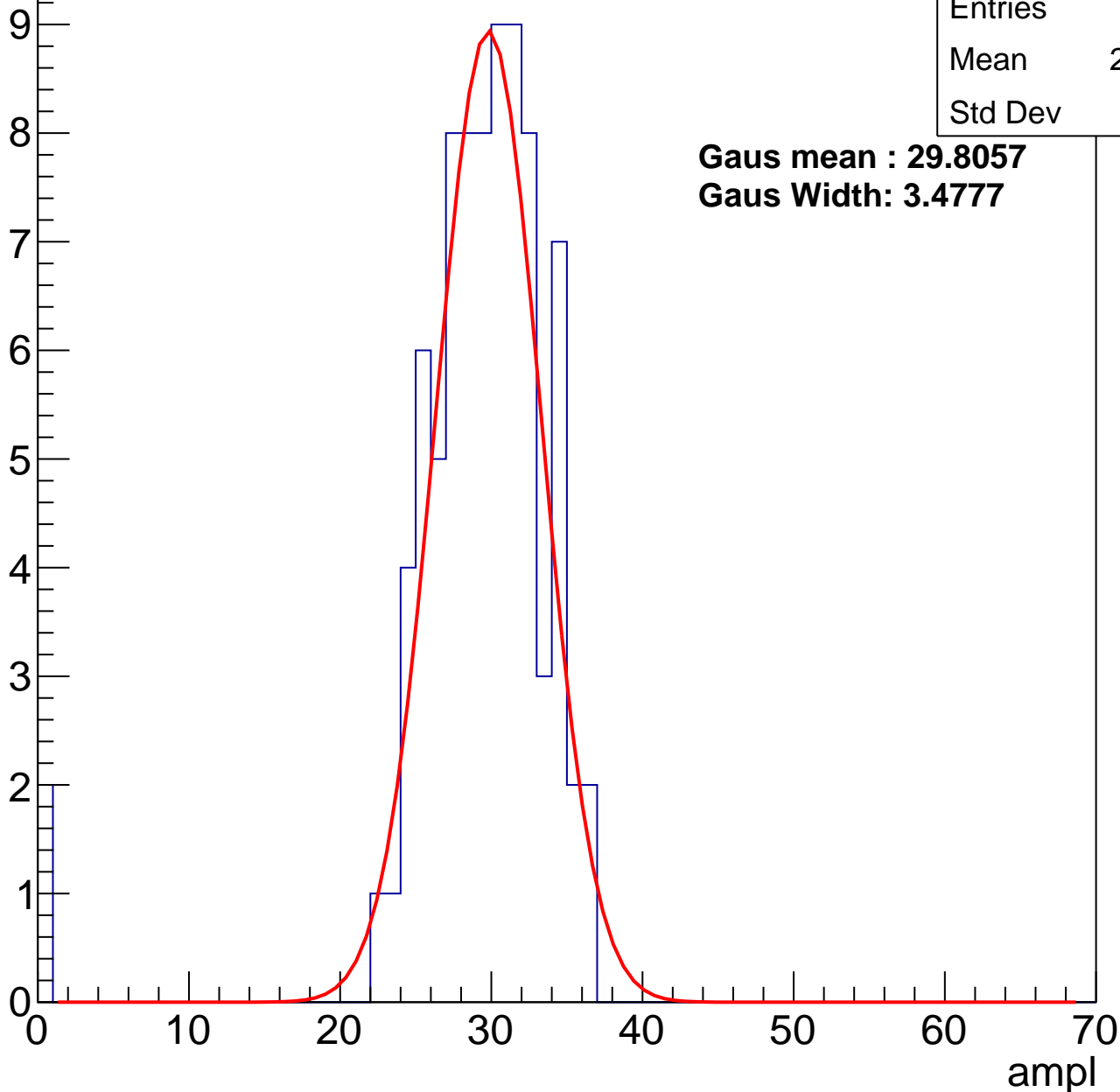
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	83
Mean	28.64
Std Dev	5.54

**Gaus mean : 29.8057**

**Gaus Width: 3.4777**



# B1L101S, U18-ch29, adc1

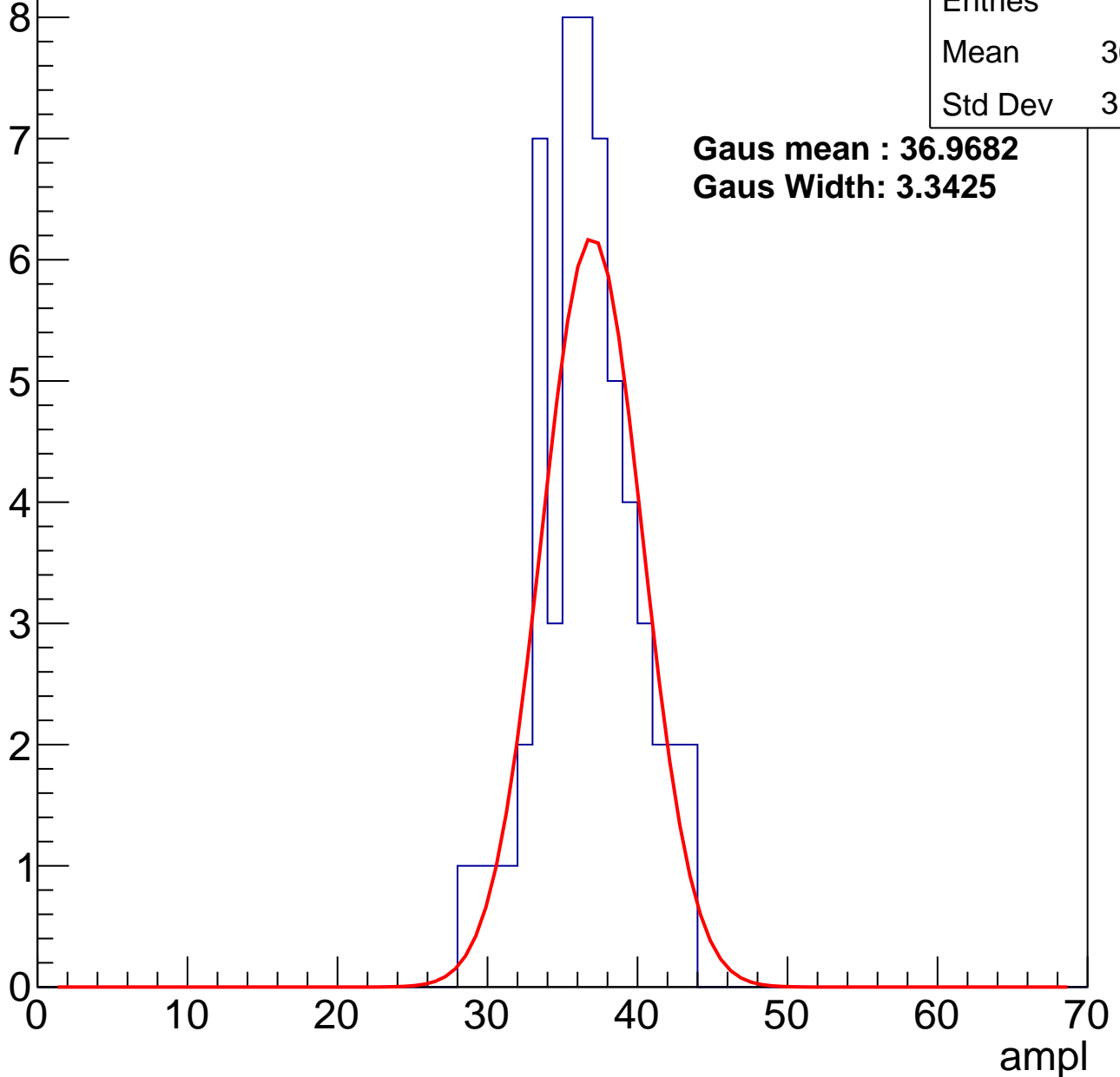
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	36.14
Std Dev	3.295

**Gaus mean : 36.9682**

**Gaus Width: 3.3425**



# B1L101S, U18-ch29, adc2

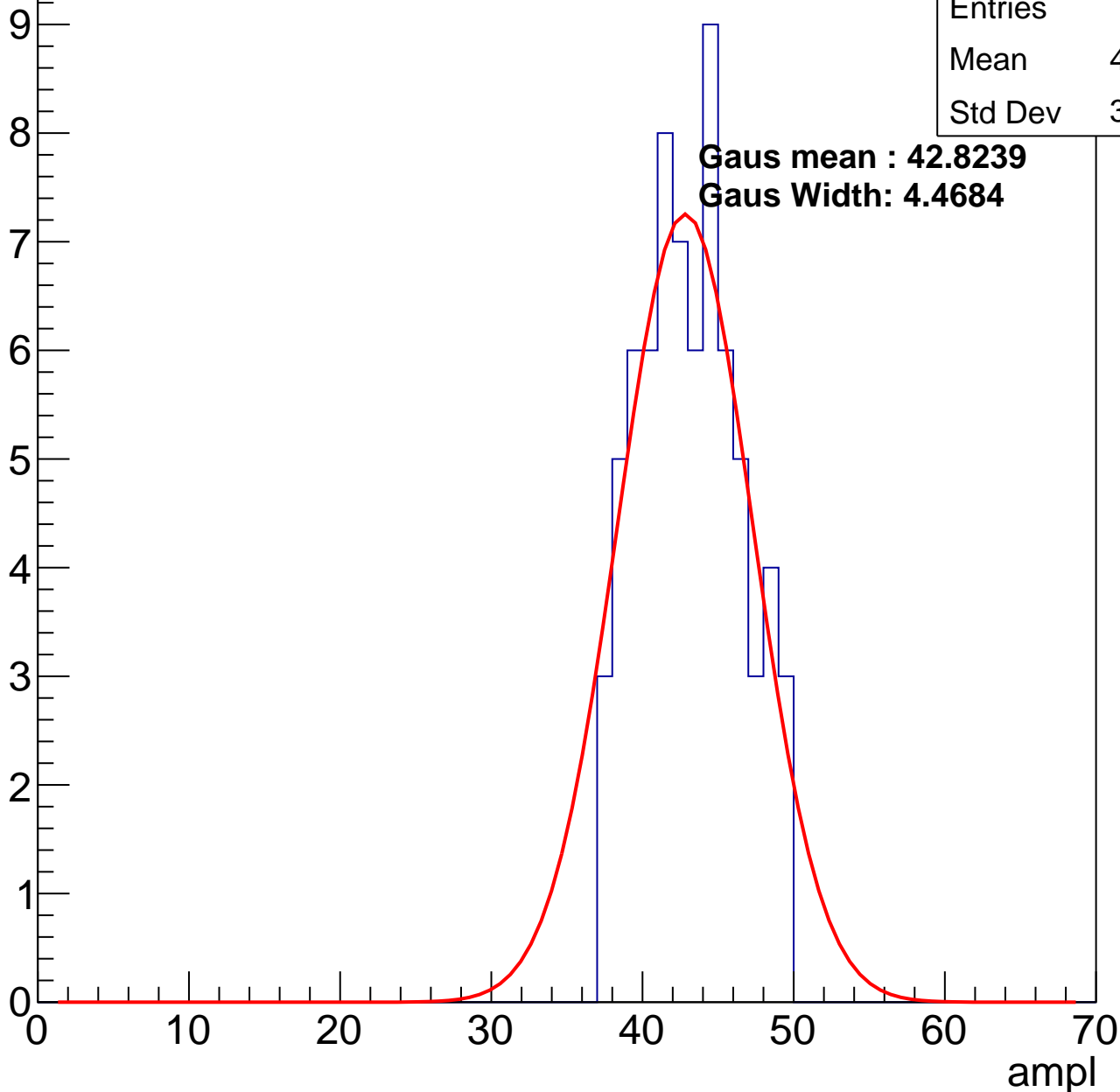
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	42.69
Std Dev	3.248

**Gaus mean : 42.8239**

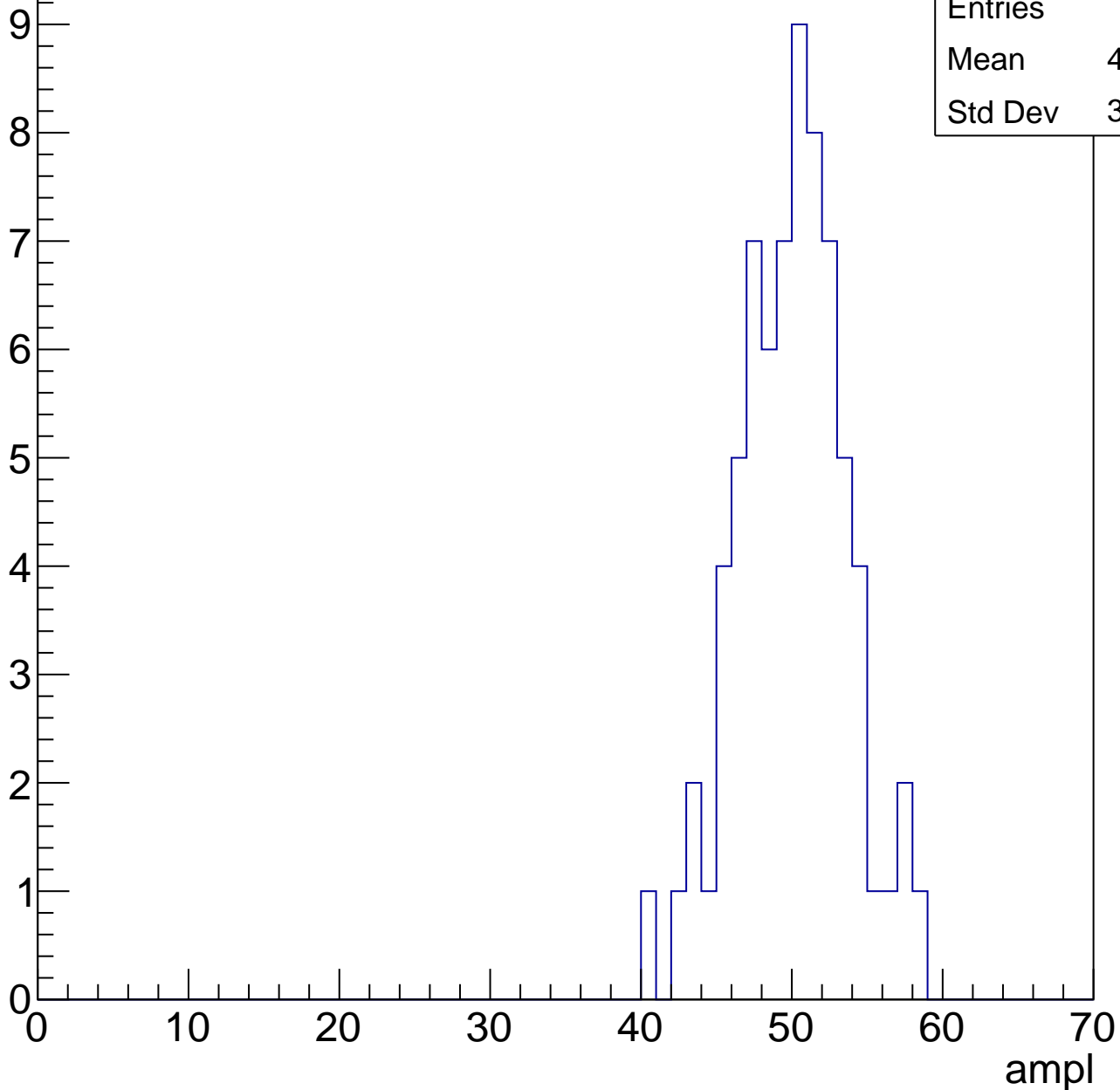
**Gaus Width: 4.4684**



# B1L101S, U18-ch29, adc3

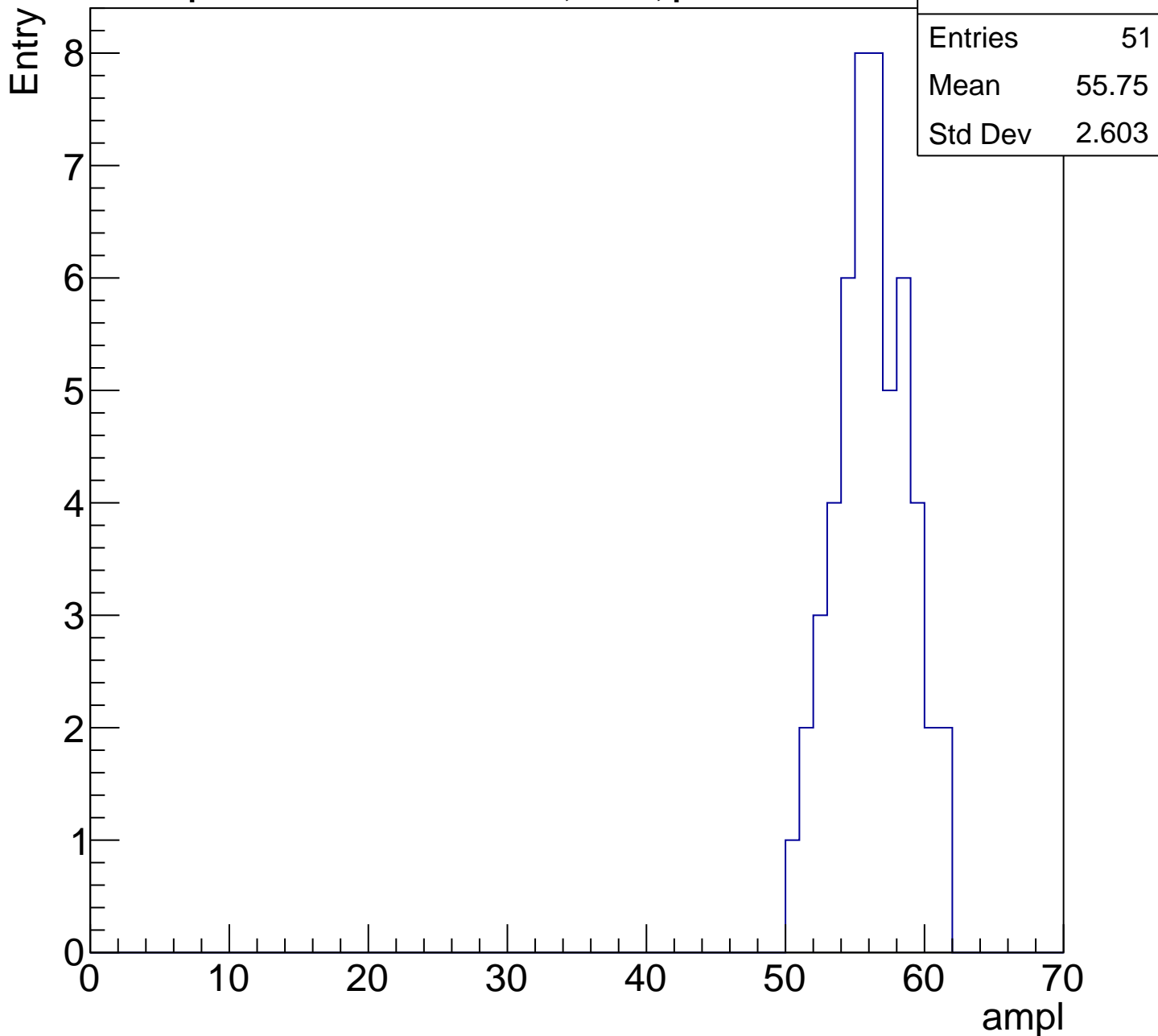
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch29, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U18-ch29, adc5

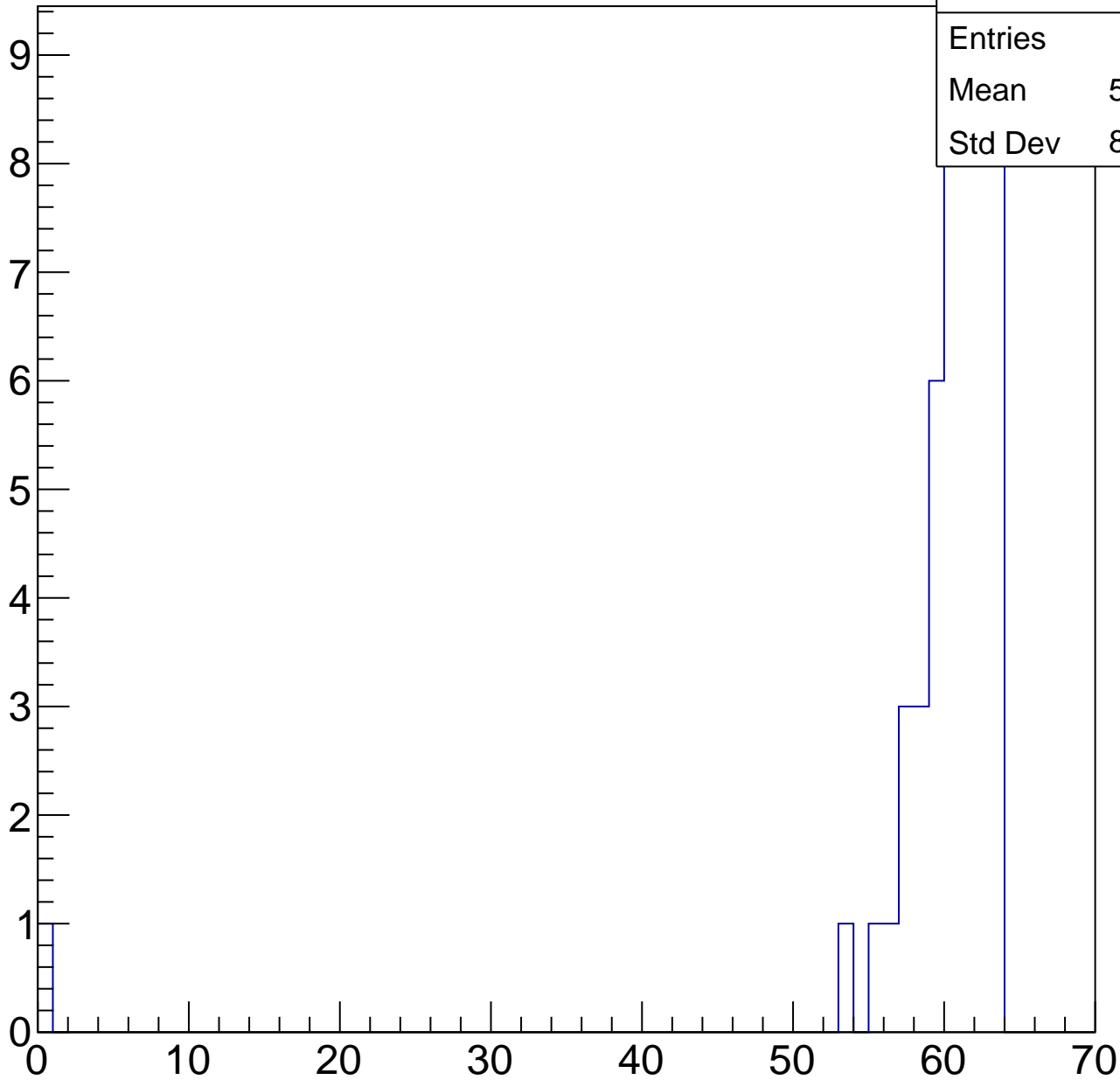
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	49
Mean	59.04
Std Dev	8.813

ampl



# B1L101S, U18-ch29, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.67
Std Dev	0.4714

ampl

0 10 20 30 40 50 60 70



# B1L101S, U18-ch29, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch30, adc0

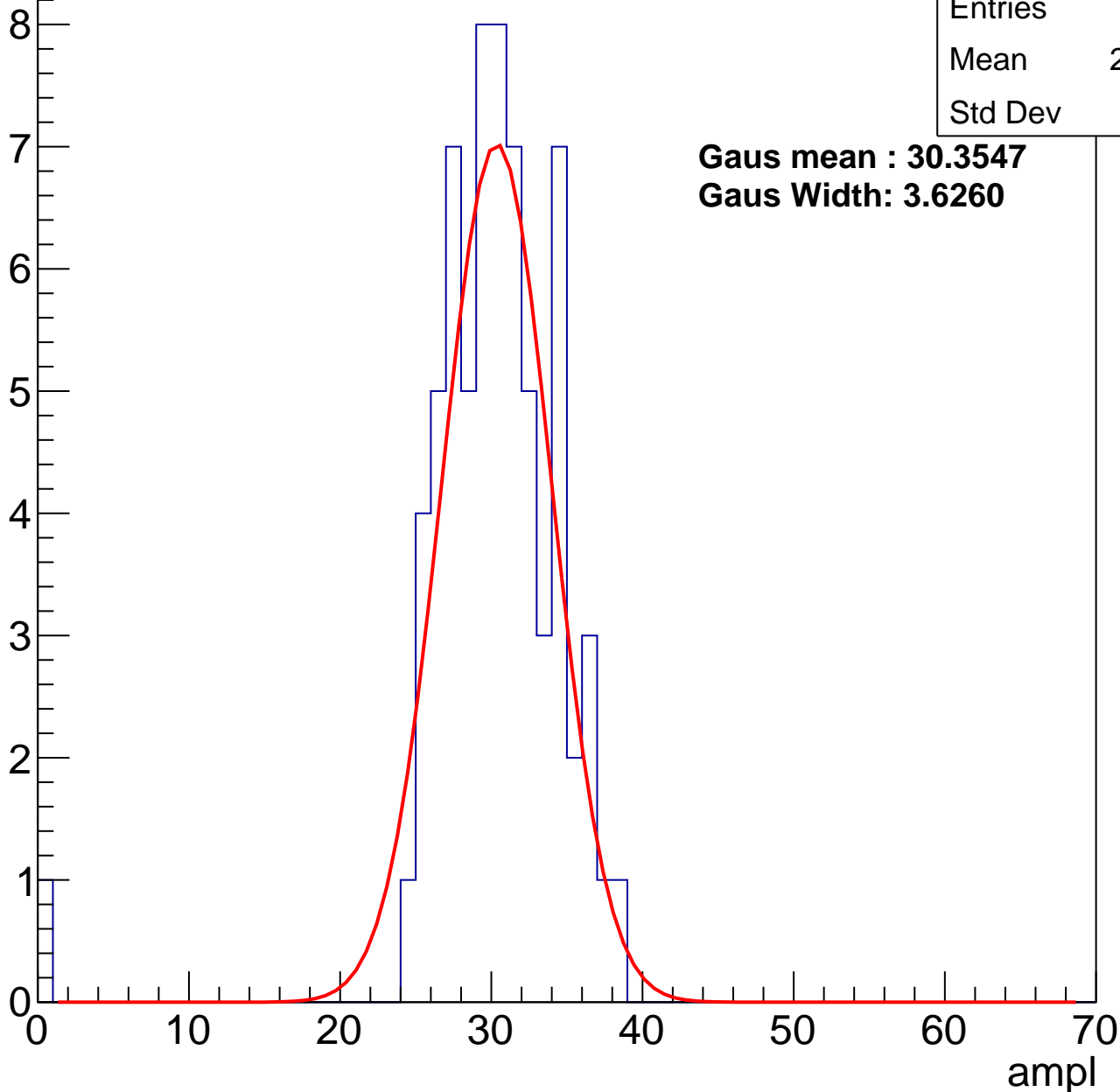
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	29.74
Std Dev	4.91

**Gaus mean : 30.3547**

**Gaus Width: 3.6260**



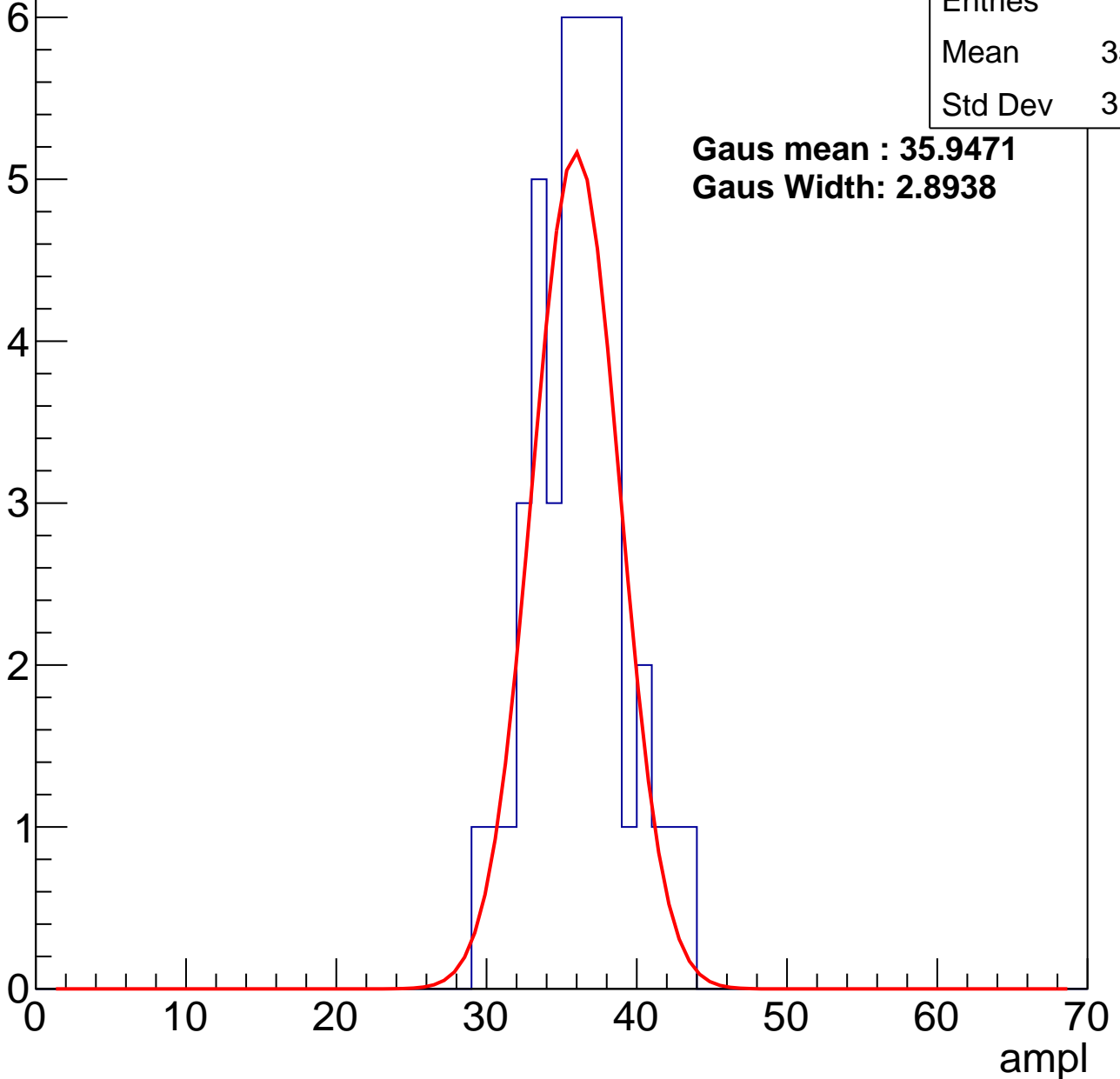
# B1L101S, U18-ch30, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	44
Mean	35.77
Std Dev	3.014

**Gaus mean : 35.9471**  
**Gaus Width: 2.8938**



# B1L101S, U18-ch30, adc2

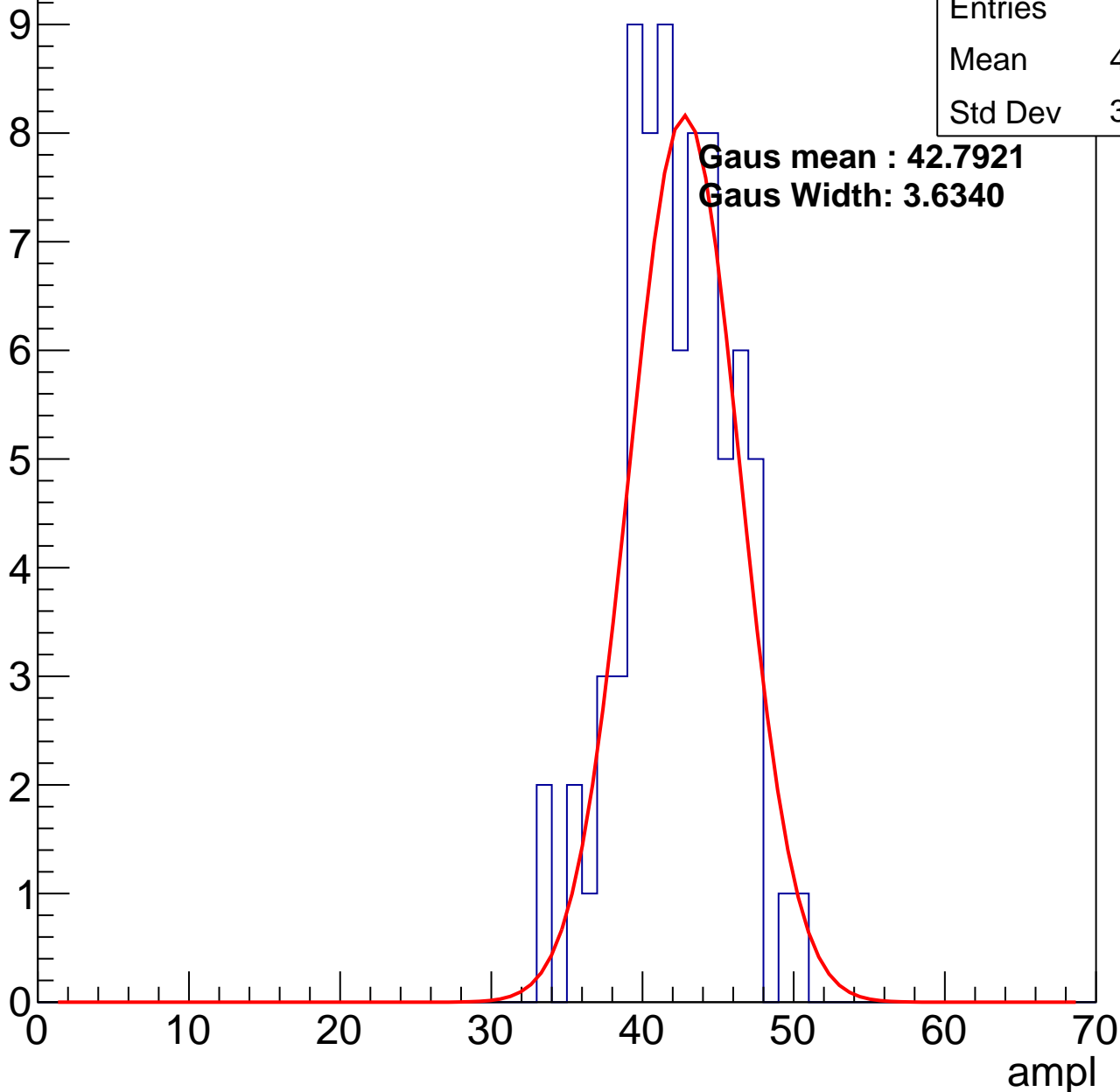
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	41.82
Std Dev	3.526

**Gaus mean : 42.7921**

**Gaus Width: 3.6340**

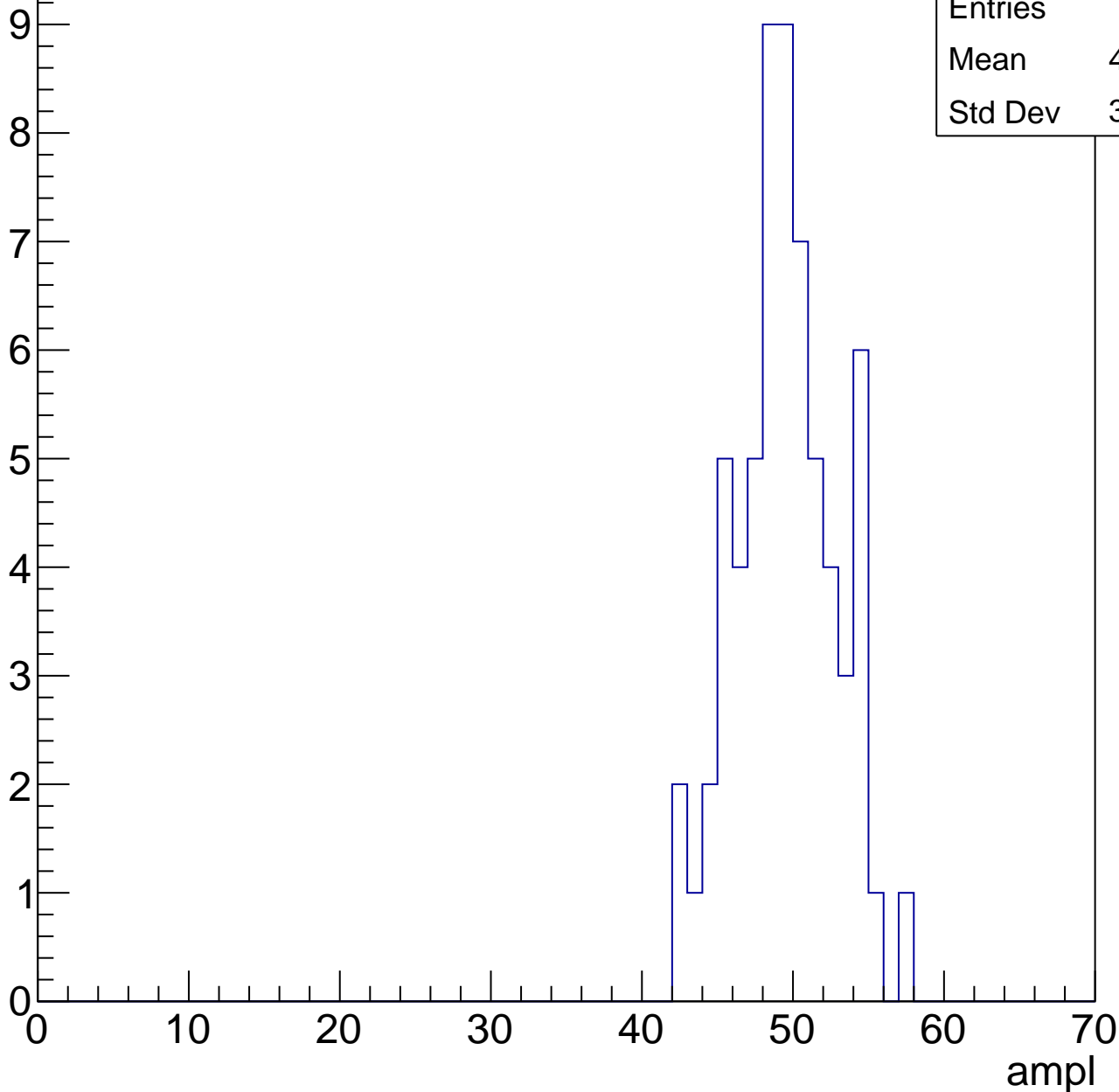


# B1L101S, U18-ch30, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	49.06
Std Dev	3.283

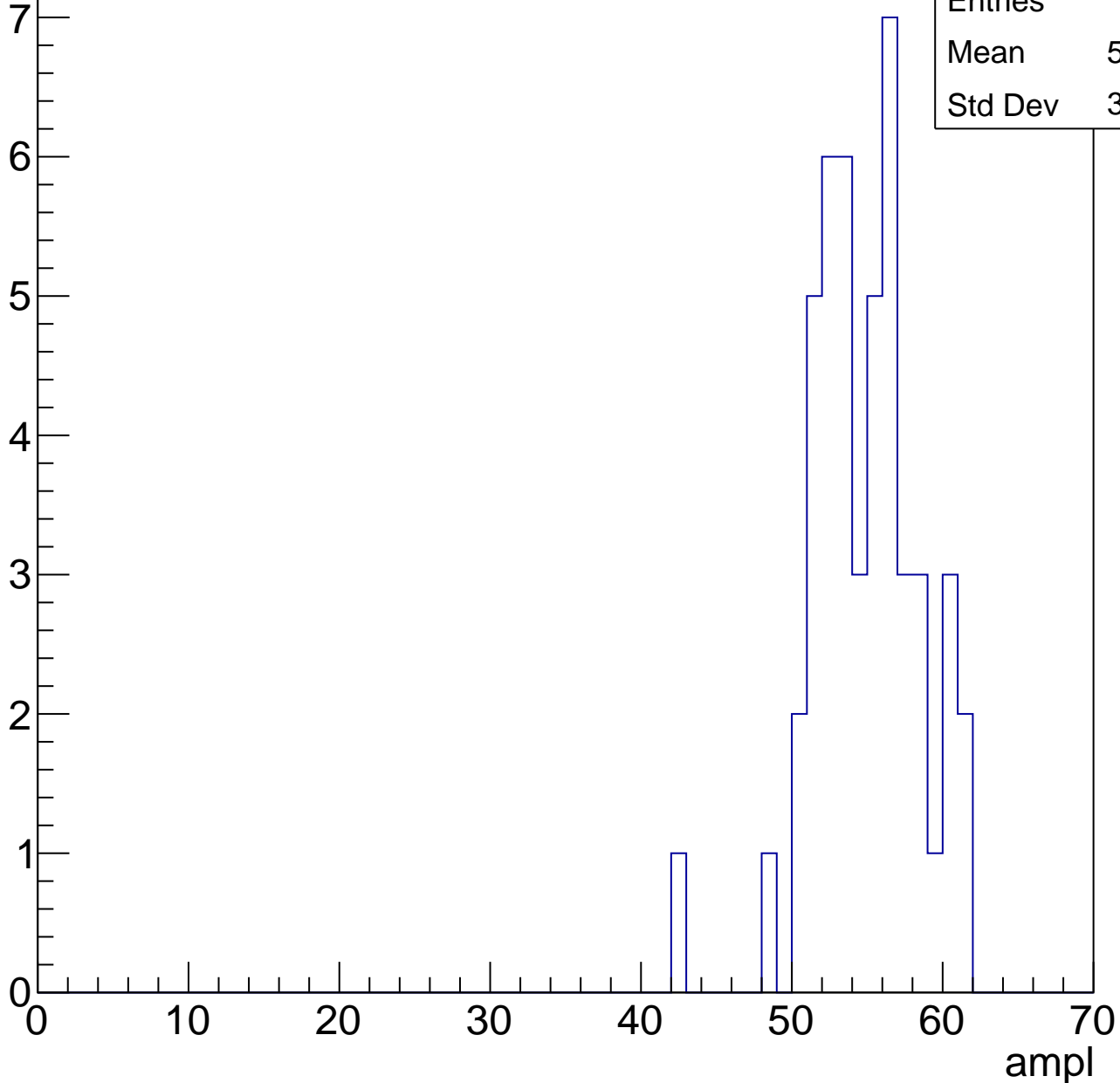


# B1L101S, U18-ch30, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	48
Mean	54.38
Std Dev	3.592



# B1L101S, U18-ch30, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

10

Entries 62

Mean 58.45

Std Dev 7.924

8

6

4

2

0

ampl

0

10

20

30

40

50

60

70

# B1L101S, U18-ch30, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	61.6
Std Dev	1.2

ampl



# B1L101S, U18-ch30, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch31, adc0

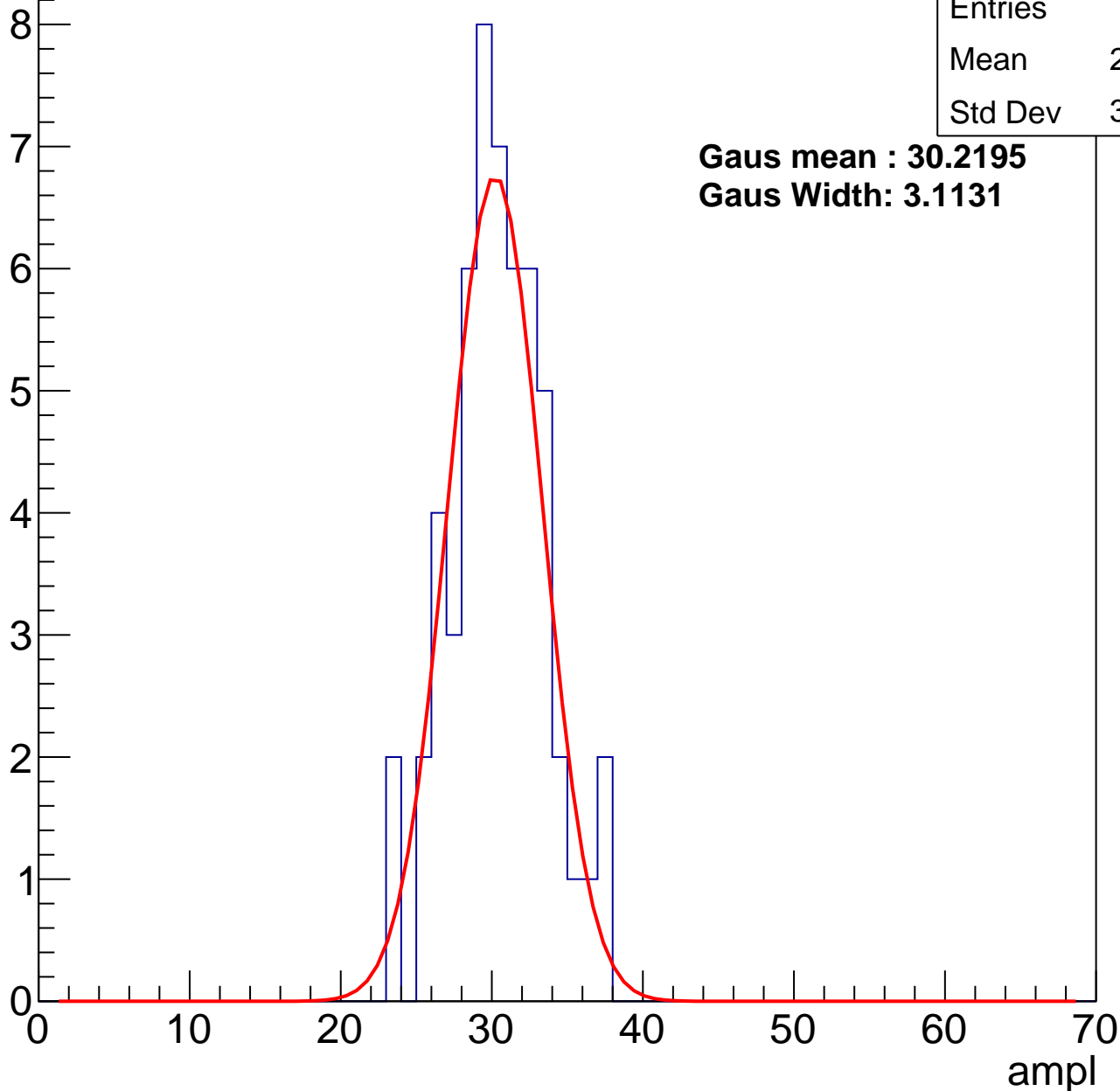
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	29.95
Std Dev	3.124

**Gaus mean : 30.2195**

**Gaus Width: 3.1131**



# B1L101S, U18-ch31, adc1

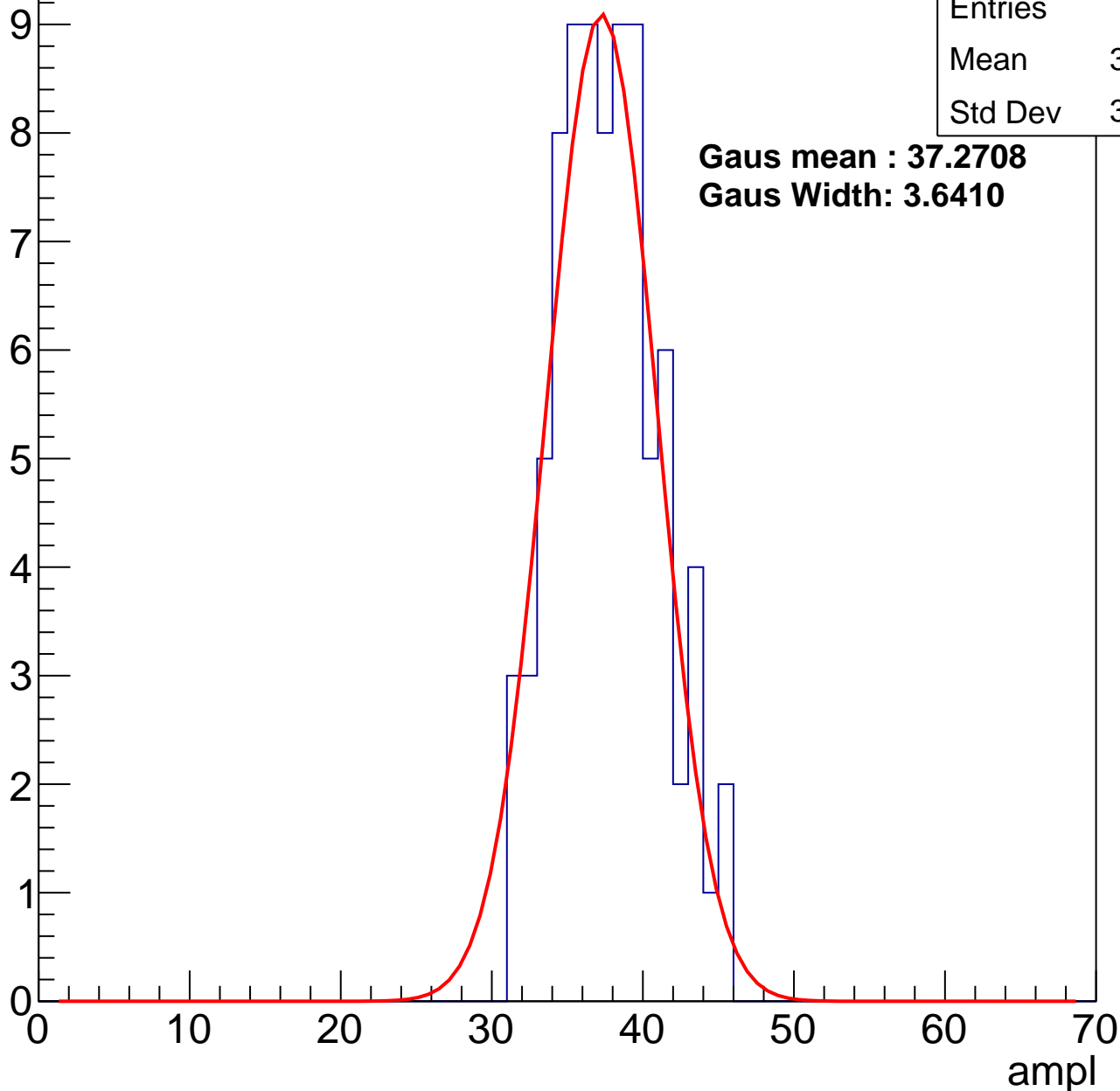
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	83
Mean	37.23
Std Dev	3.352

**Gaus mean : 37.2708**

**Gaus Width: 3.6410**



# B1L101S, U18-ch31, adc2

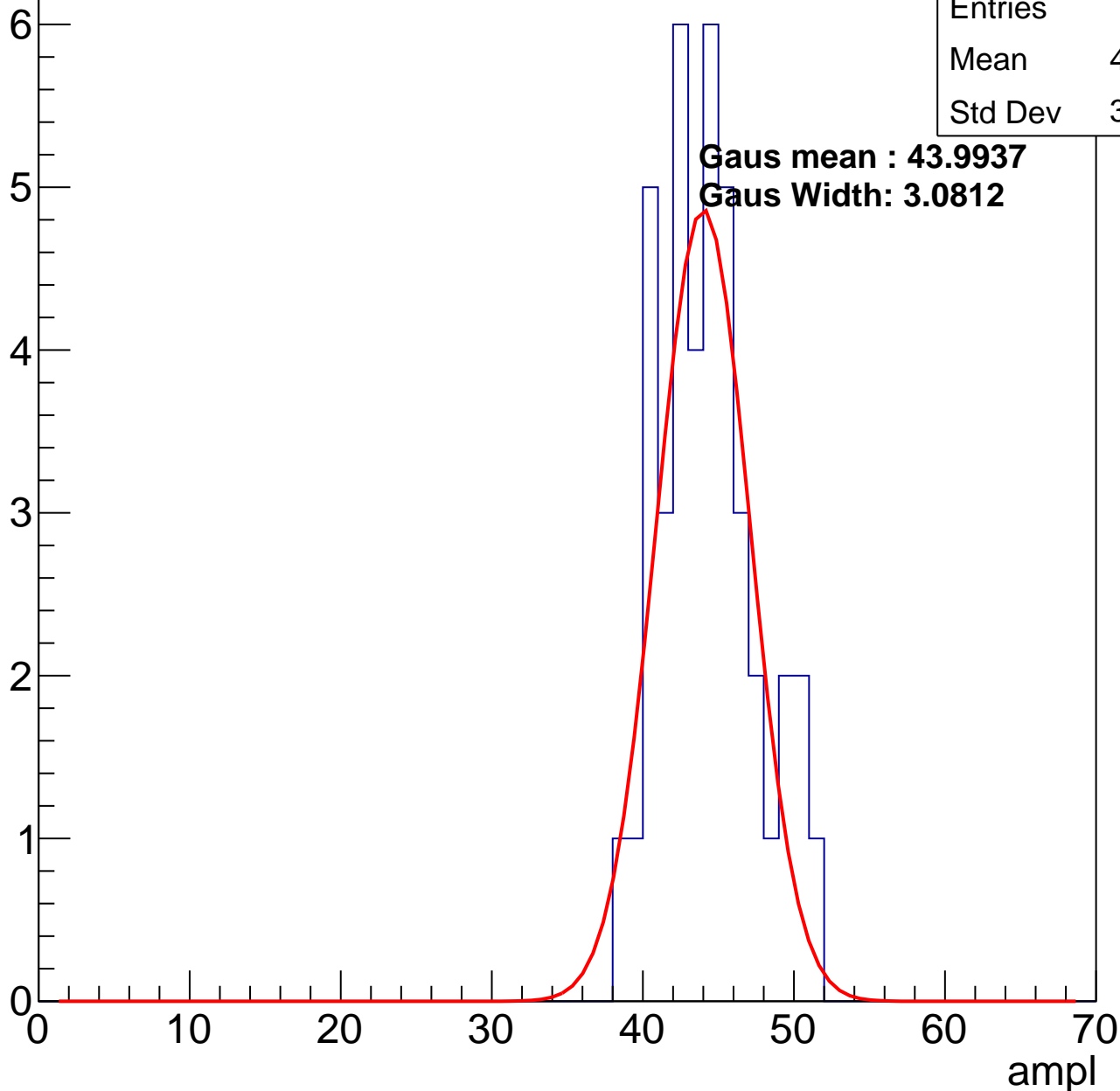
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	42
Mean	43.86
Std Dev	3.152

**Gaus mean : 43.9937**

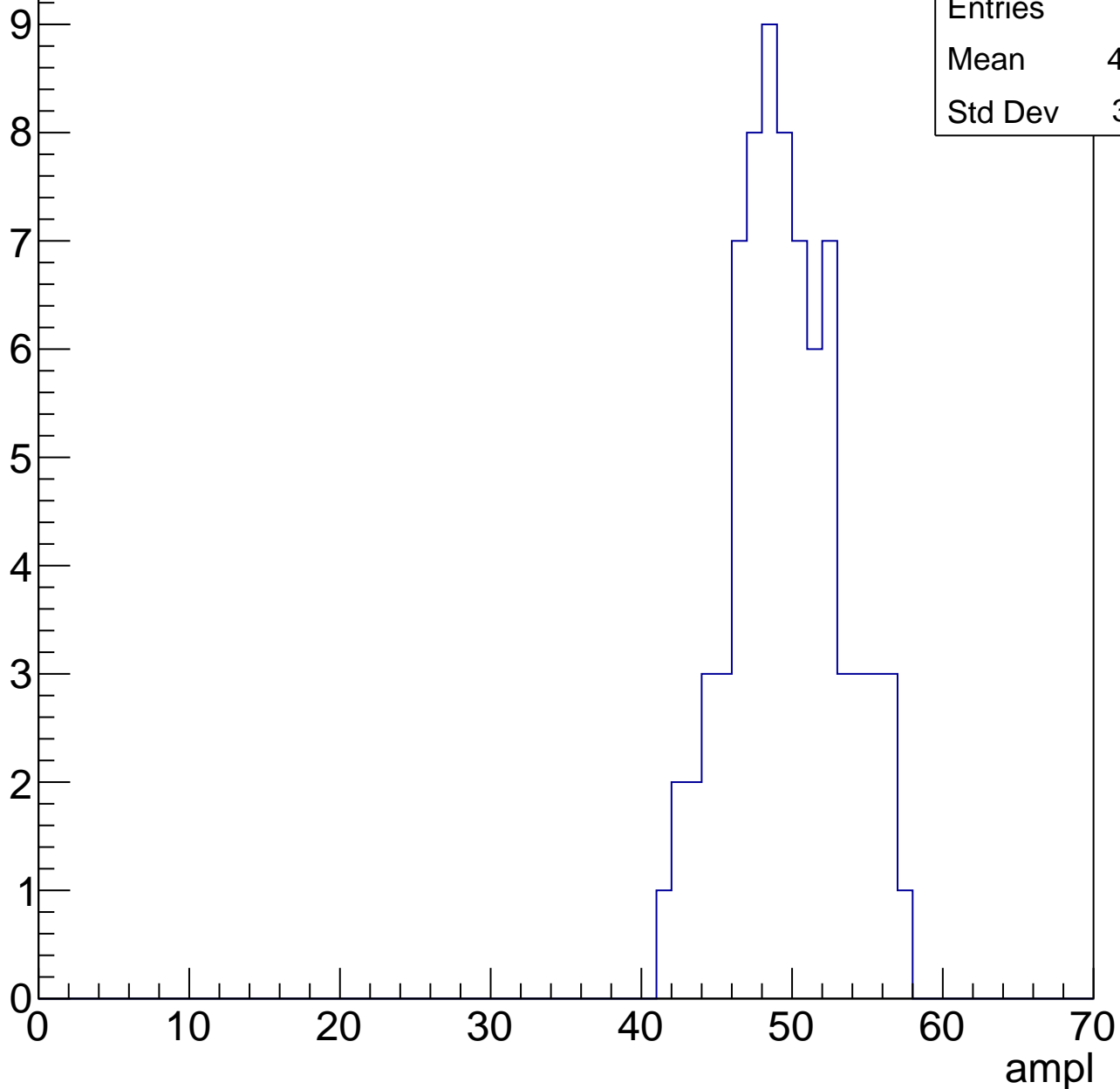
**Gaus Width: 3.0812**



# B1L101S, U18-ch31, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



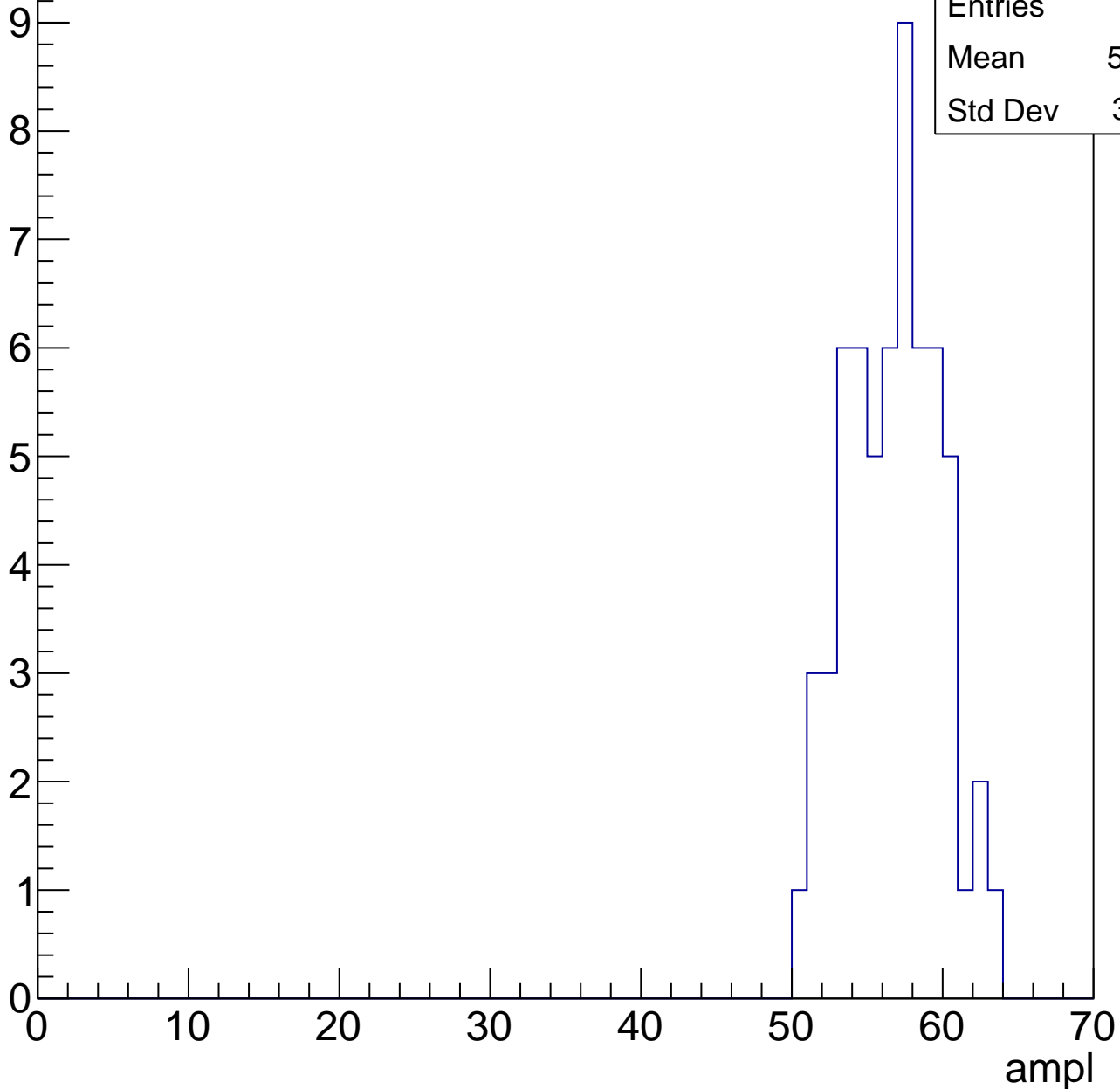
Entries	76
Mean	49.09
Std Dev	3.621

# B1L101S, U18-ch31, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

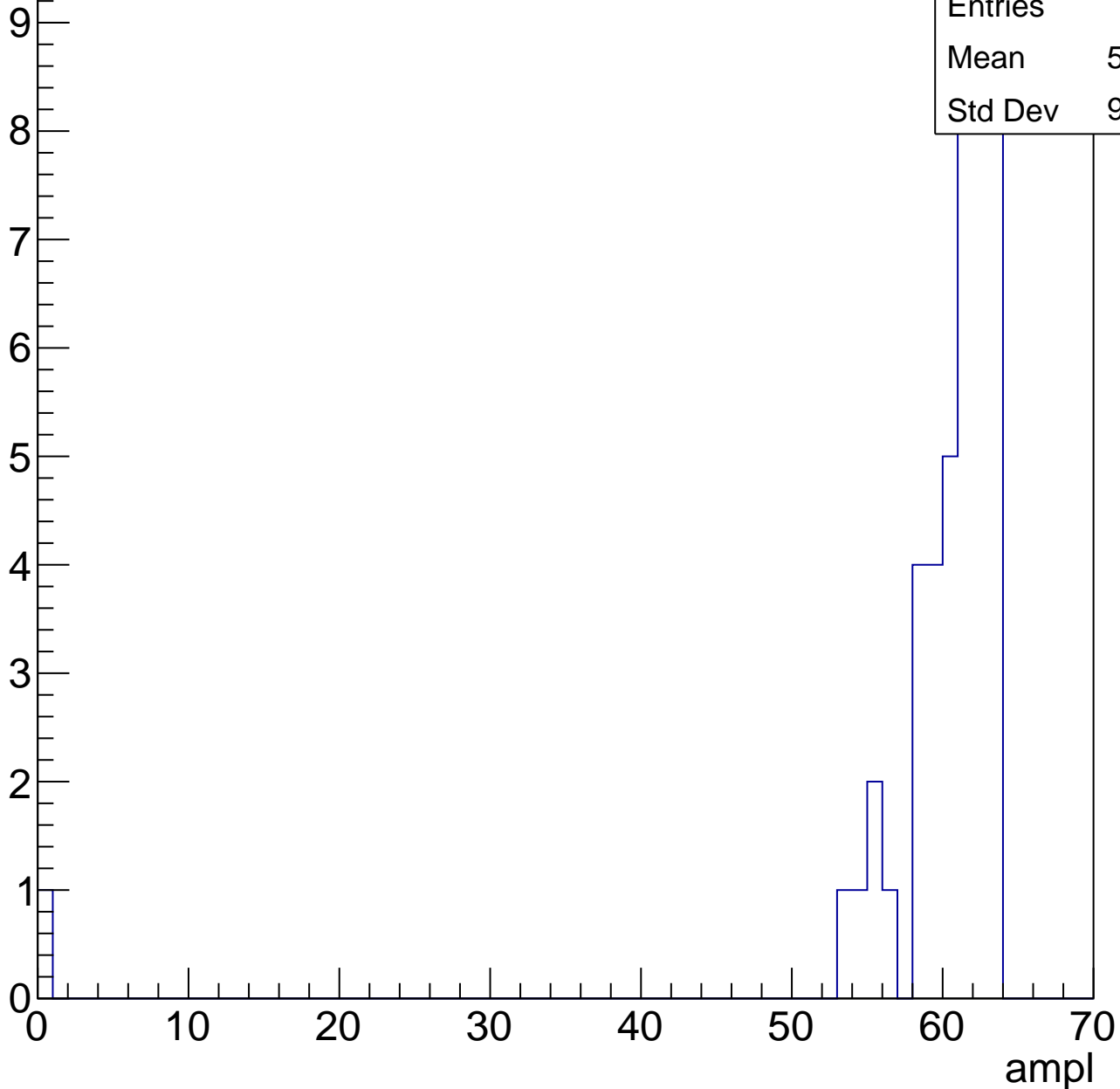
Entries	60
Mean	56.25
Std Dev	3.031



# B1L101S, U18-ch31, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch31, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	63
Std Dev	0



# B1L101S, U18-ch31, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch32, adc0

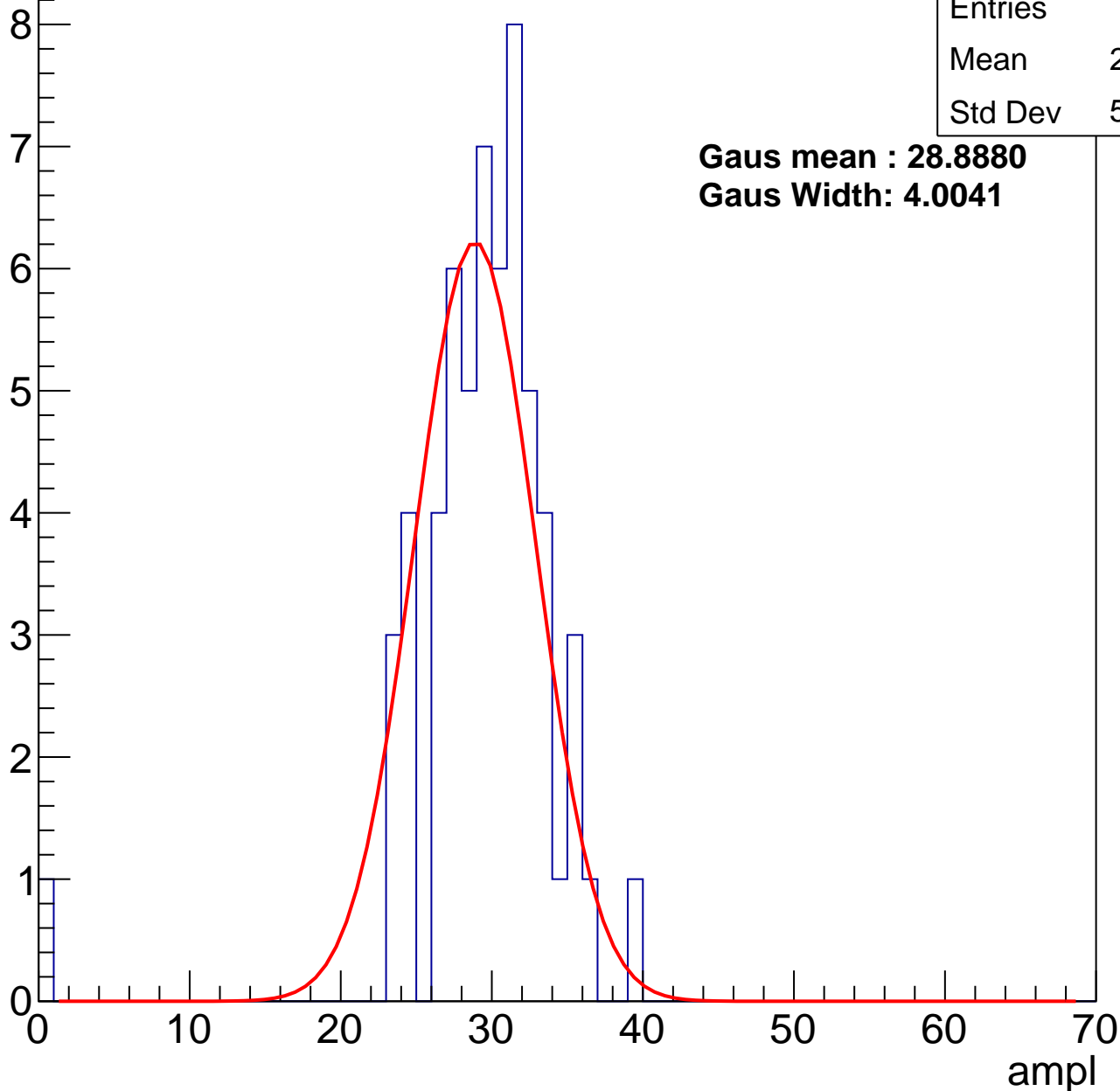
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	28.95
Std Dev	5.114

**Gaus mean : 28.8880**

**Gaus Width: 4.0041**



# B1L101S, U18-ch32, adc1

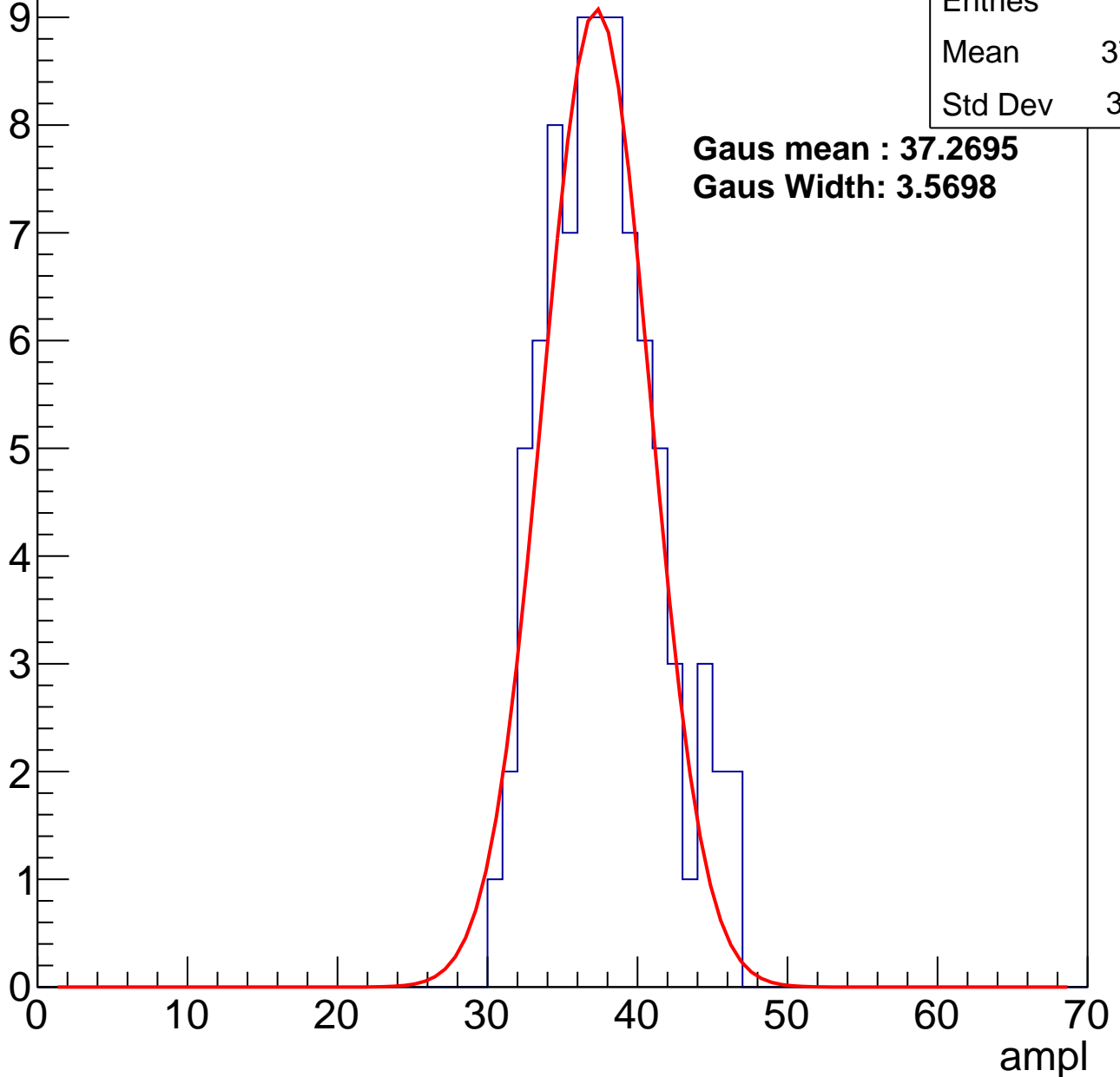
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	85
Mean	37.26
Std Dev	3.701

**Gaus mean : 37.2695**

**Gaus Width: 3.5698**



# B1L101S, U18-ch32, adc2

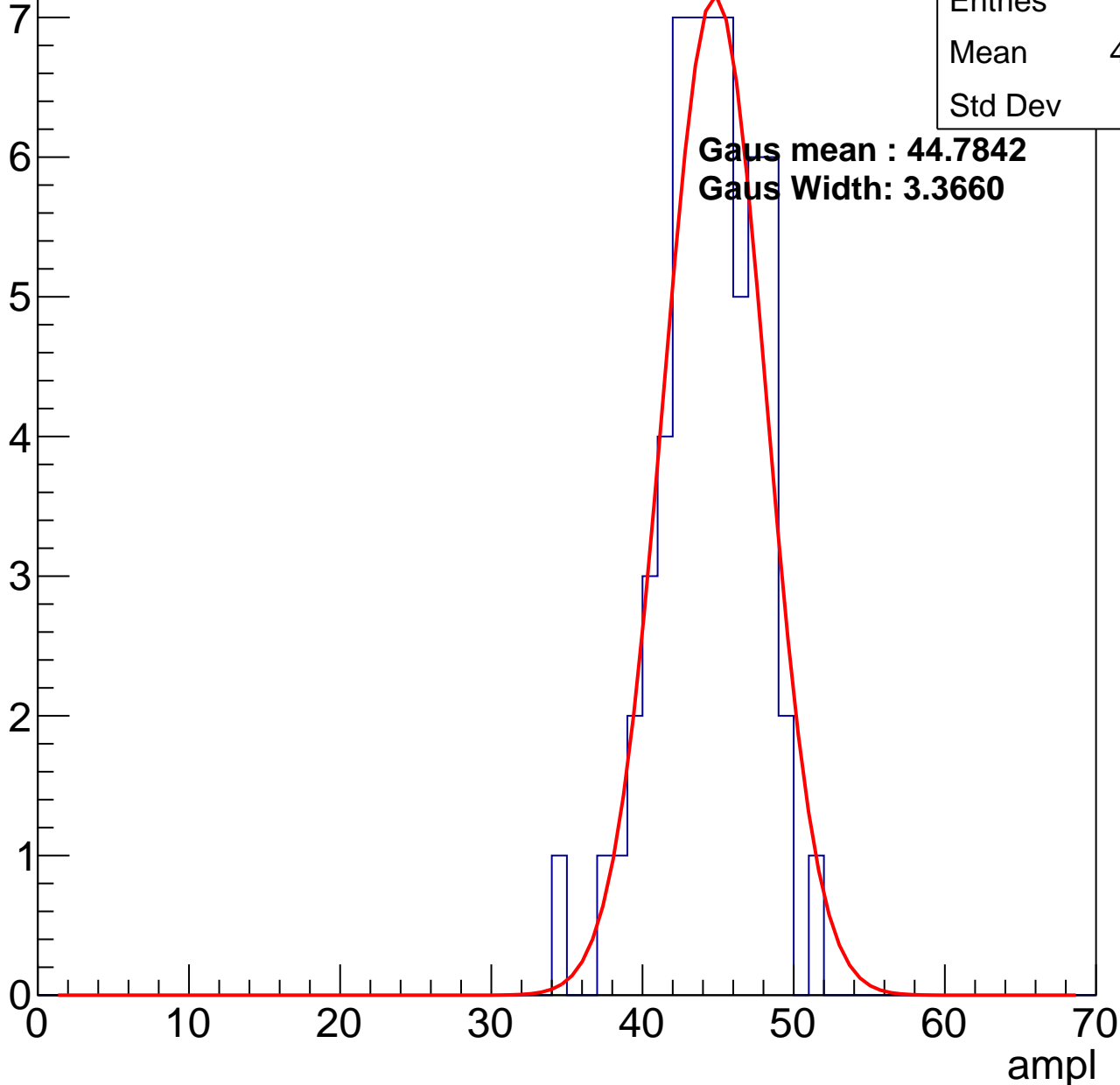
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	43.97
Std Dev	3.24

**Gaus mean : 44.7842**

**Gaus Width: 3.3660**

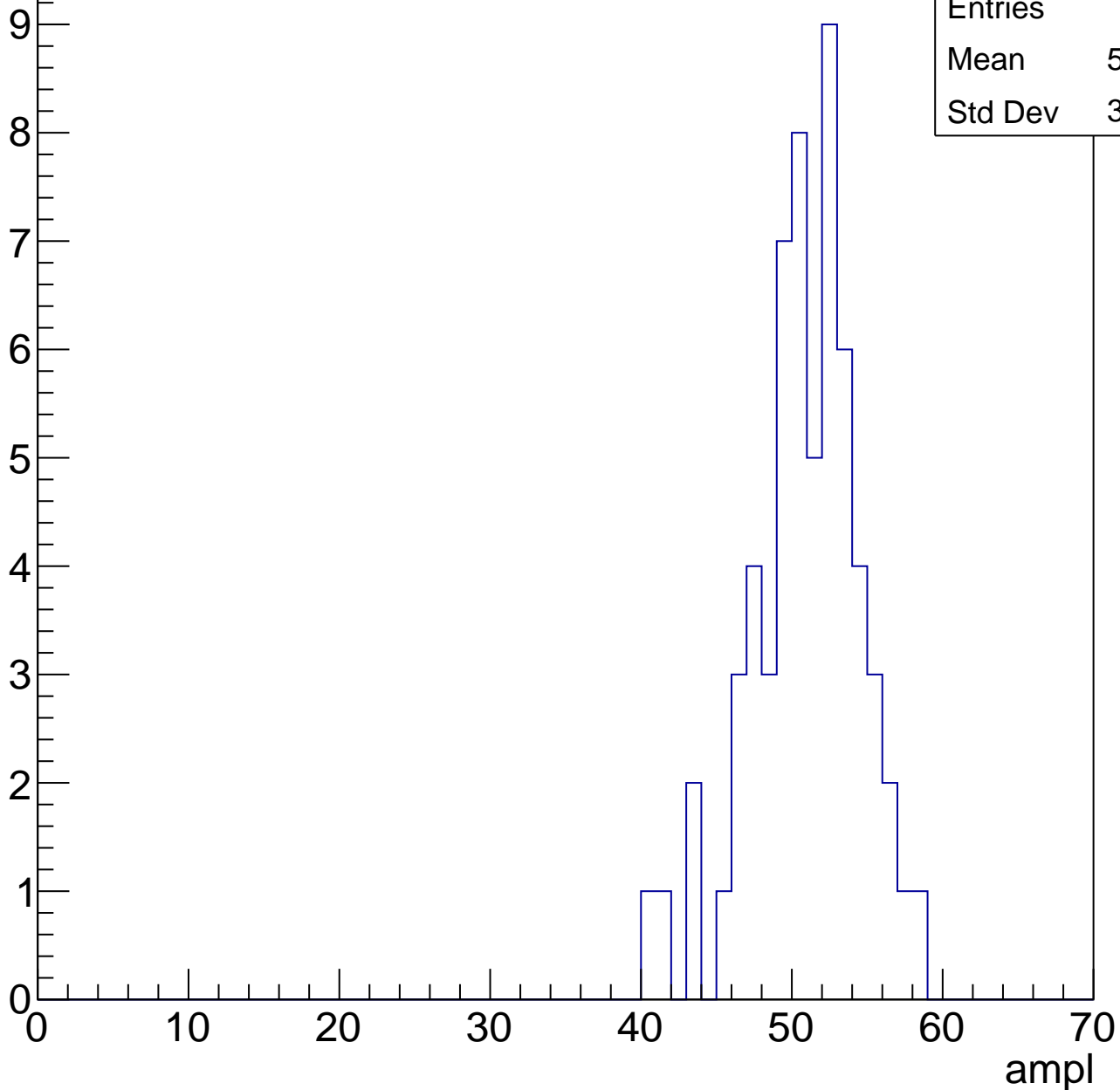


# B1L101S, U18-ch32, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	50.39
Std Dev	3.659

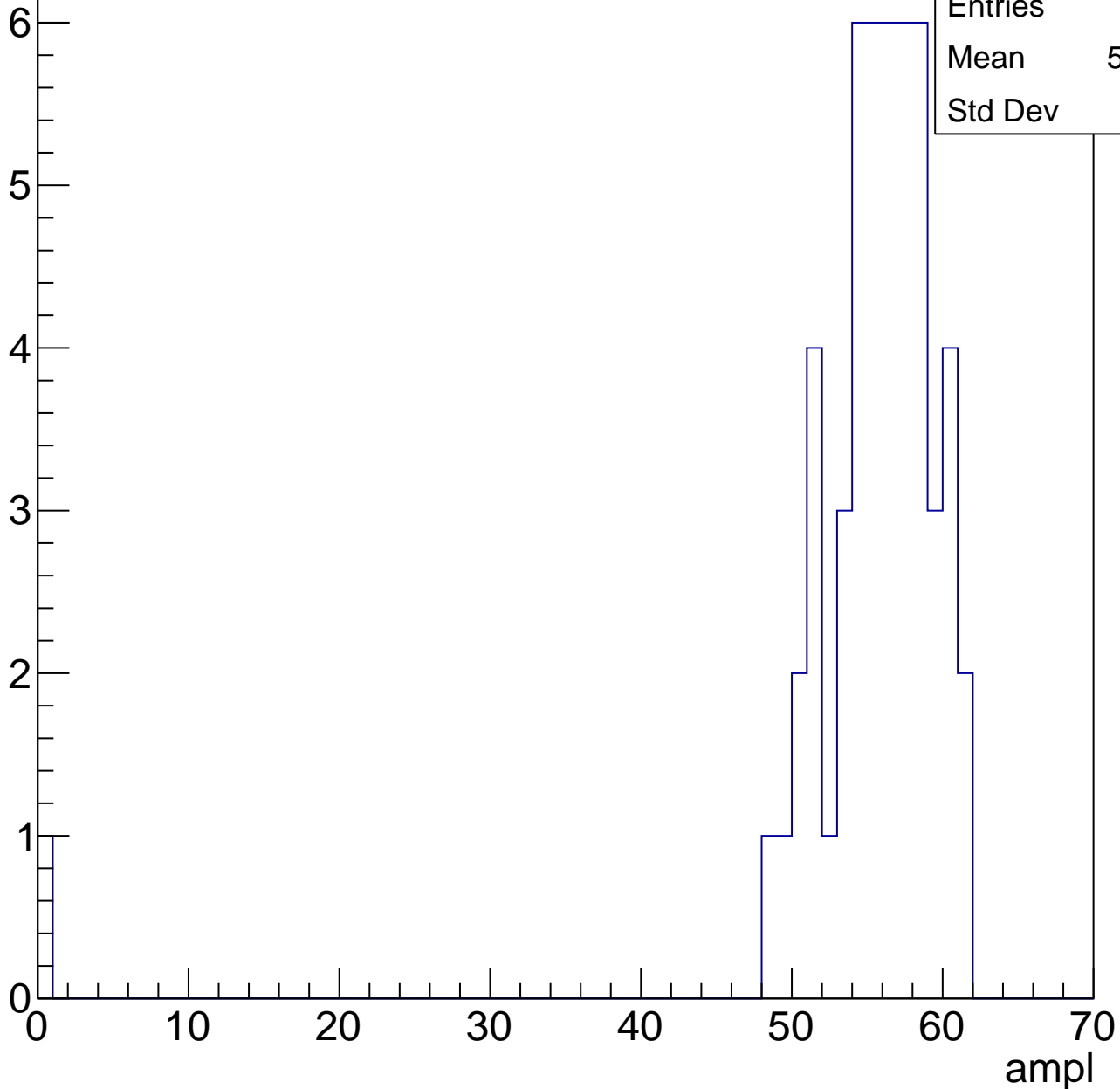


# B1L101S, U18-ch32, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	54.44
Std Dev	8.25



# B1L101S, U18-ch32, adc5

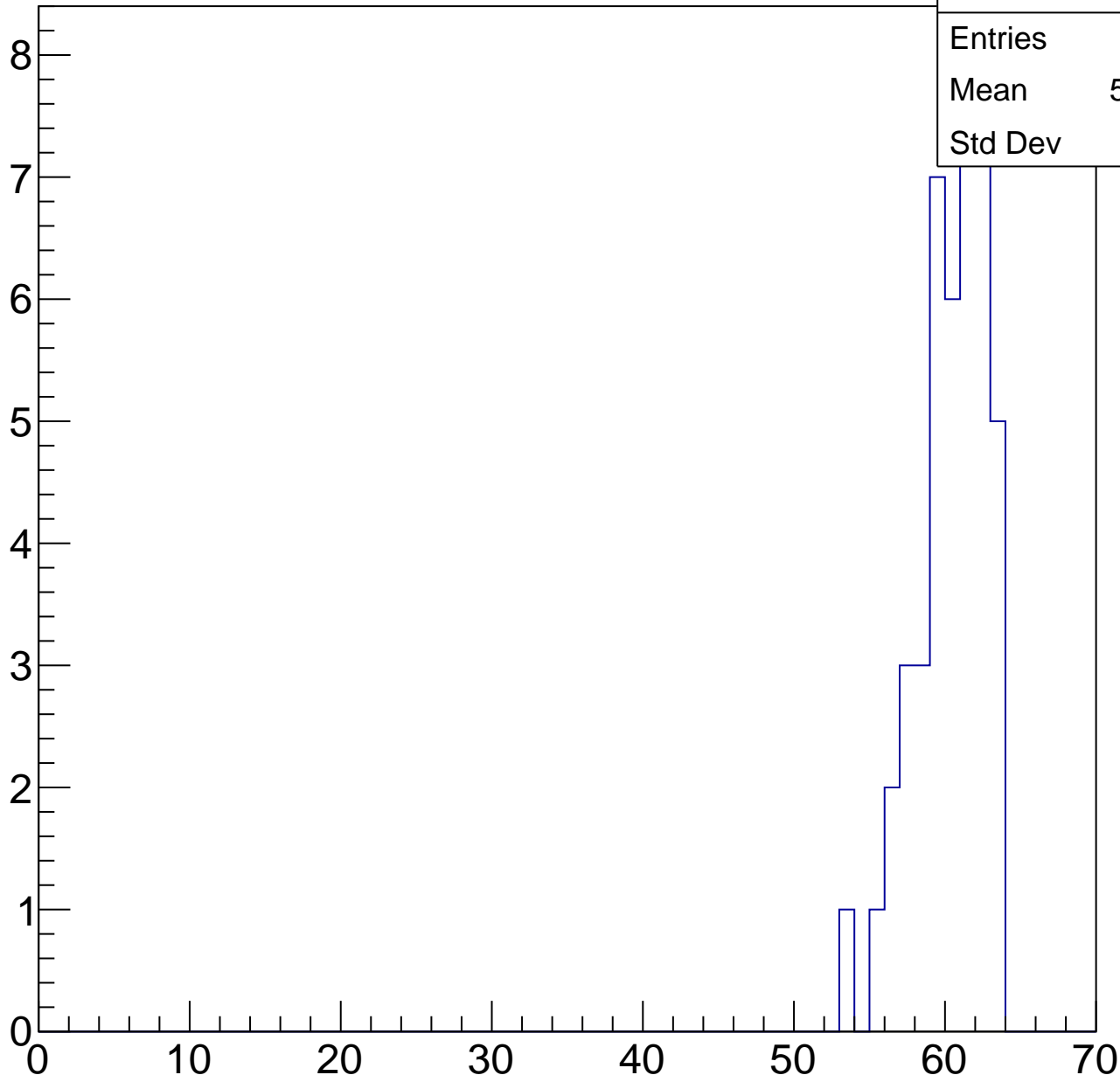
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	44
Mean	59.93
Std Dev	2.32

ampl

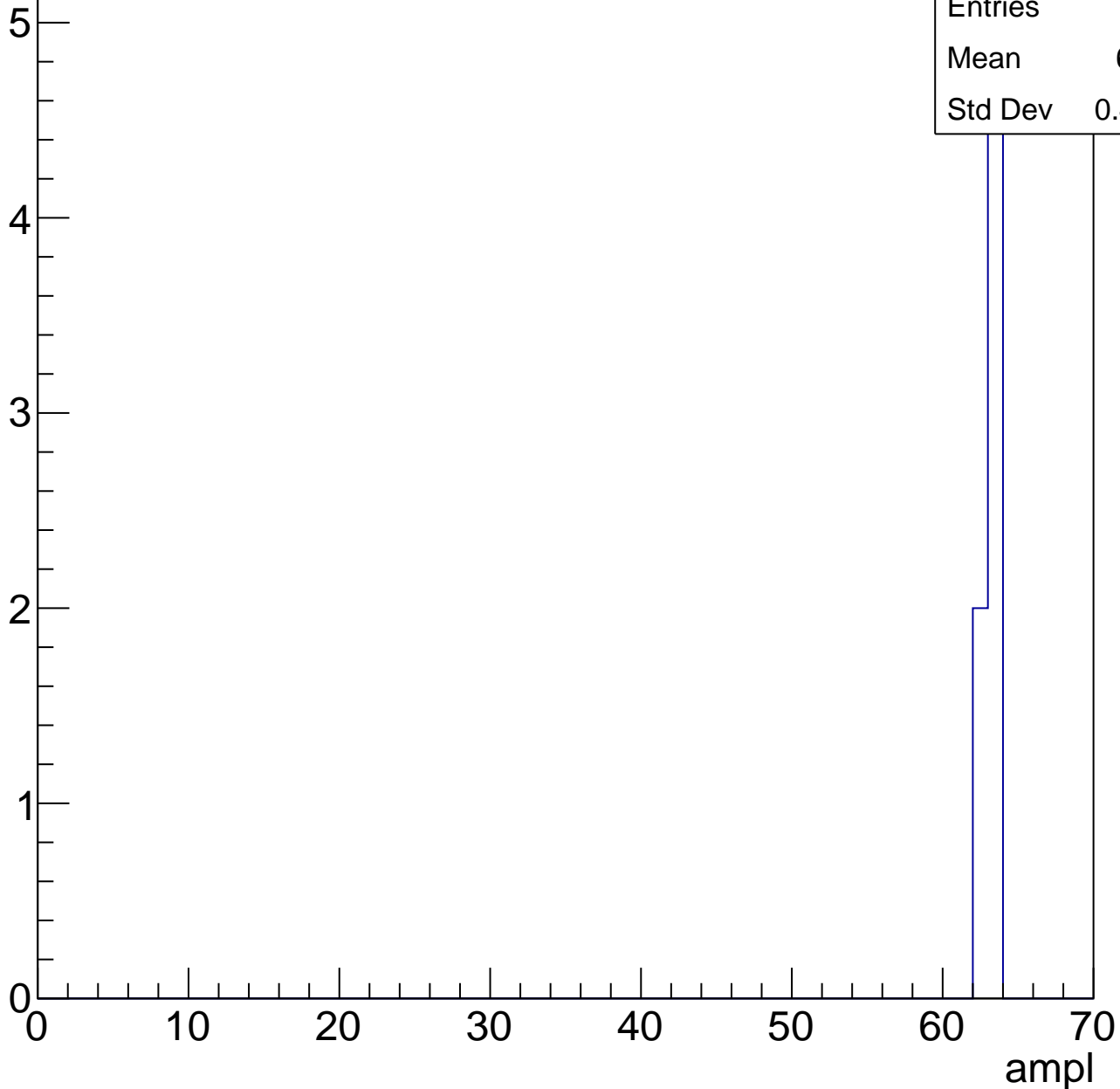


# B1L101S, U18-ch32, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	7
Mean	62.71
Std Dev	0.4518





# B1L101S, U18-ch32, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U18-ch33, adc0

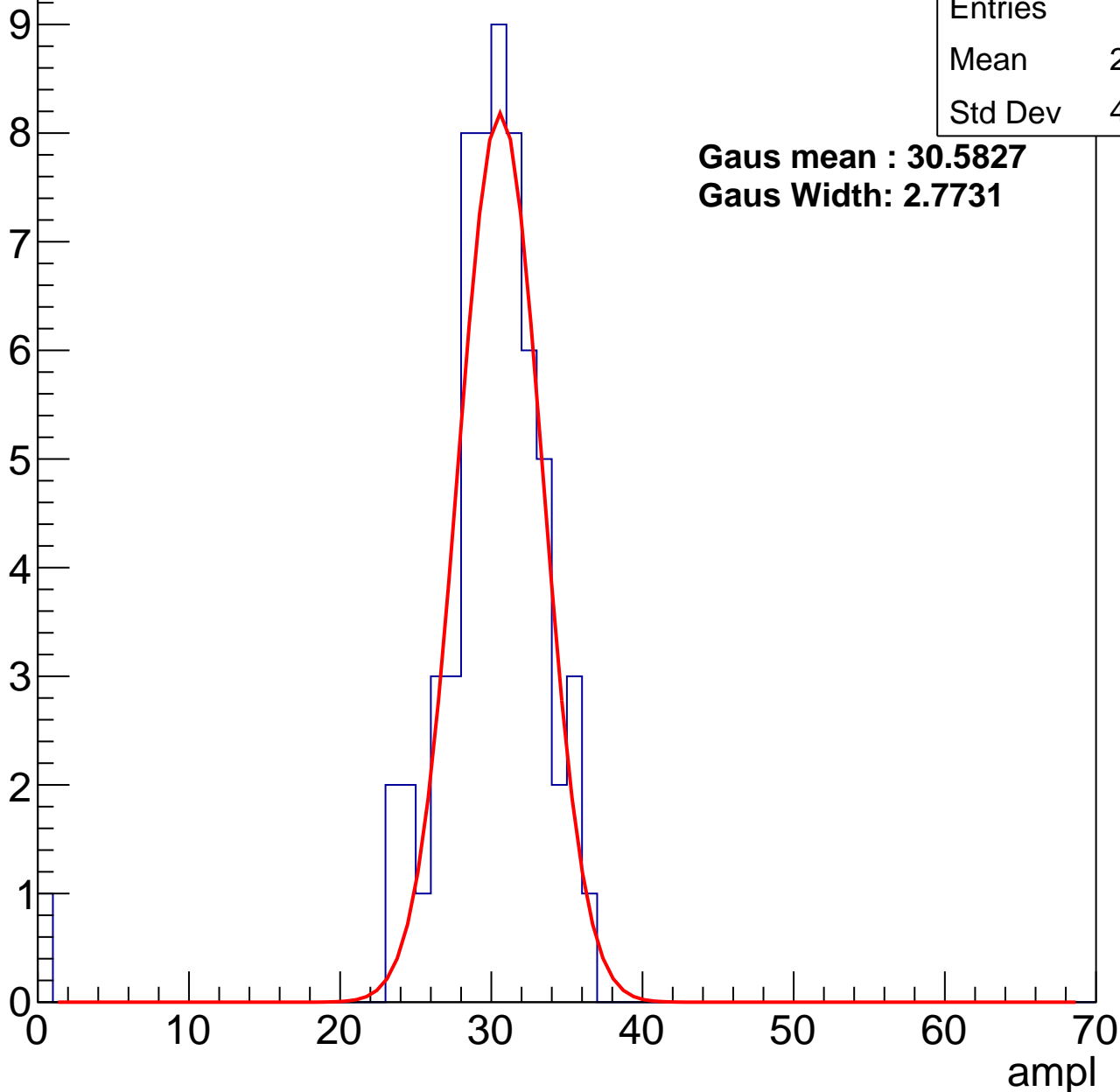
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	29.32
Std Dev	4.755

**Gaus mean : 30.5827**

**Gaus Width: 2.7731**



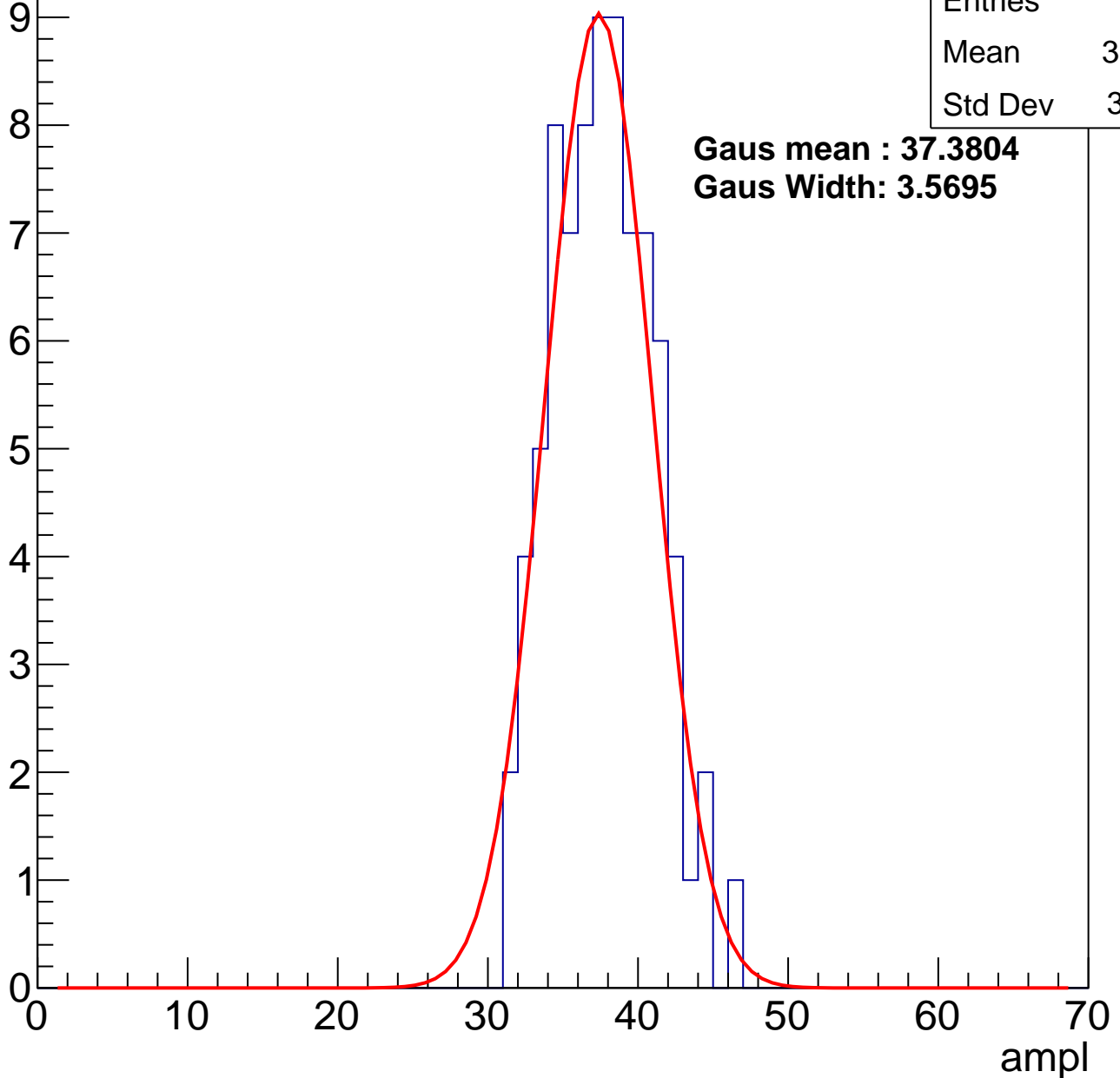
# B1L101S, U18-ch33, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	80
Mean	37.24
Std Dev	3.291

**Gaus mean : 37.3804**  
**Gaus Width: 3.5695**



# B1L101S, U18-ch33, adc2

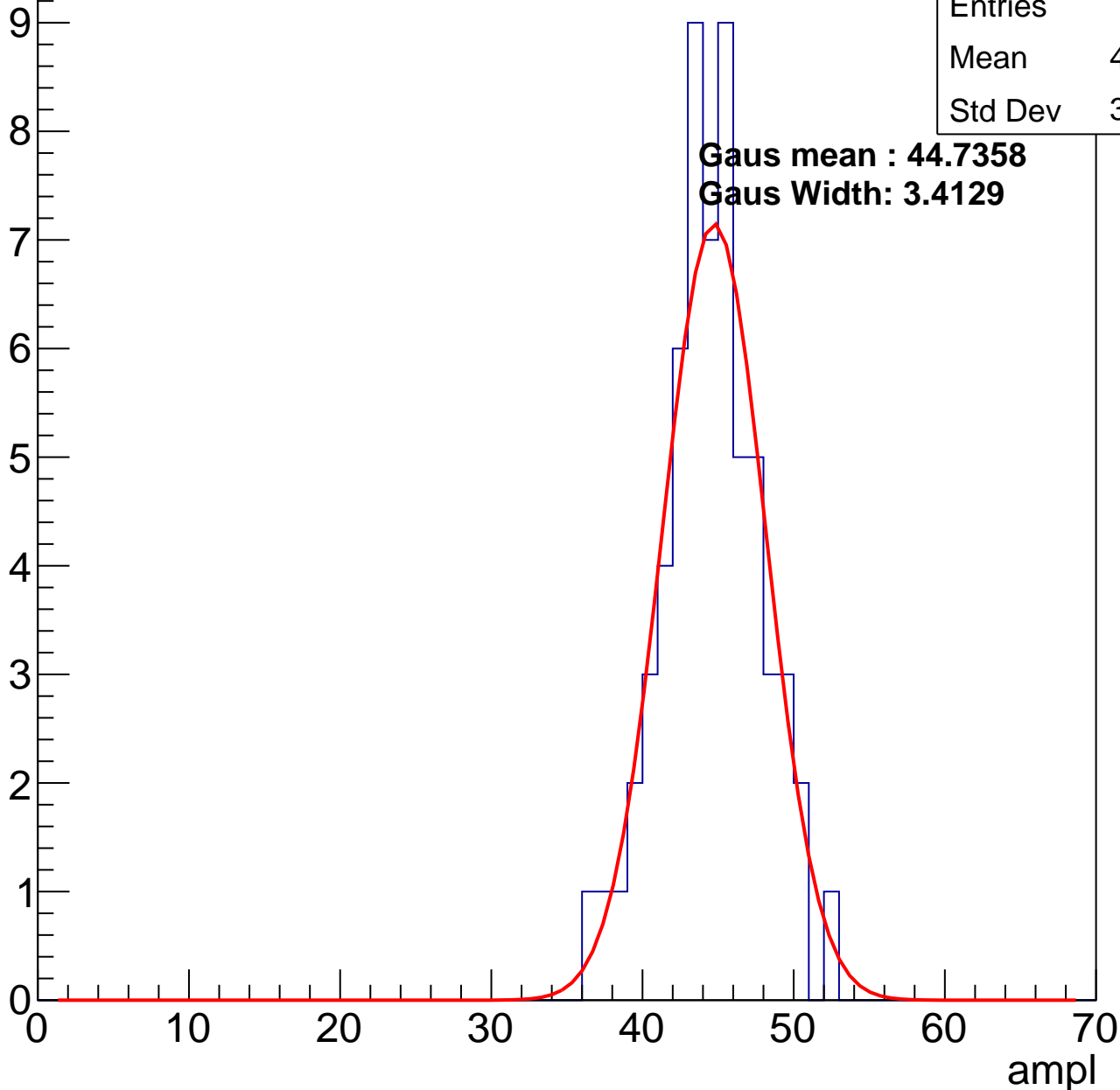
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	44.08
Std Dev	3.234

**Gaus mean : 44.7358**

**Gaus Width: 3.4129**

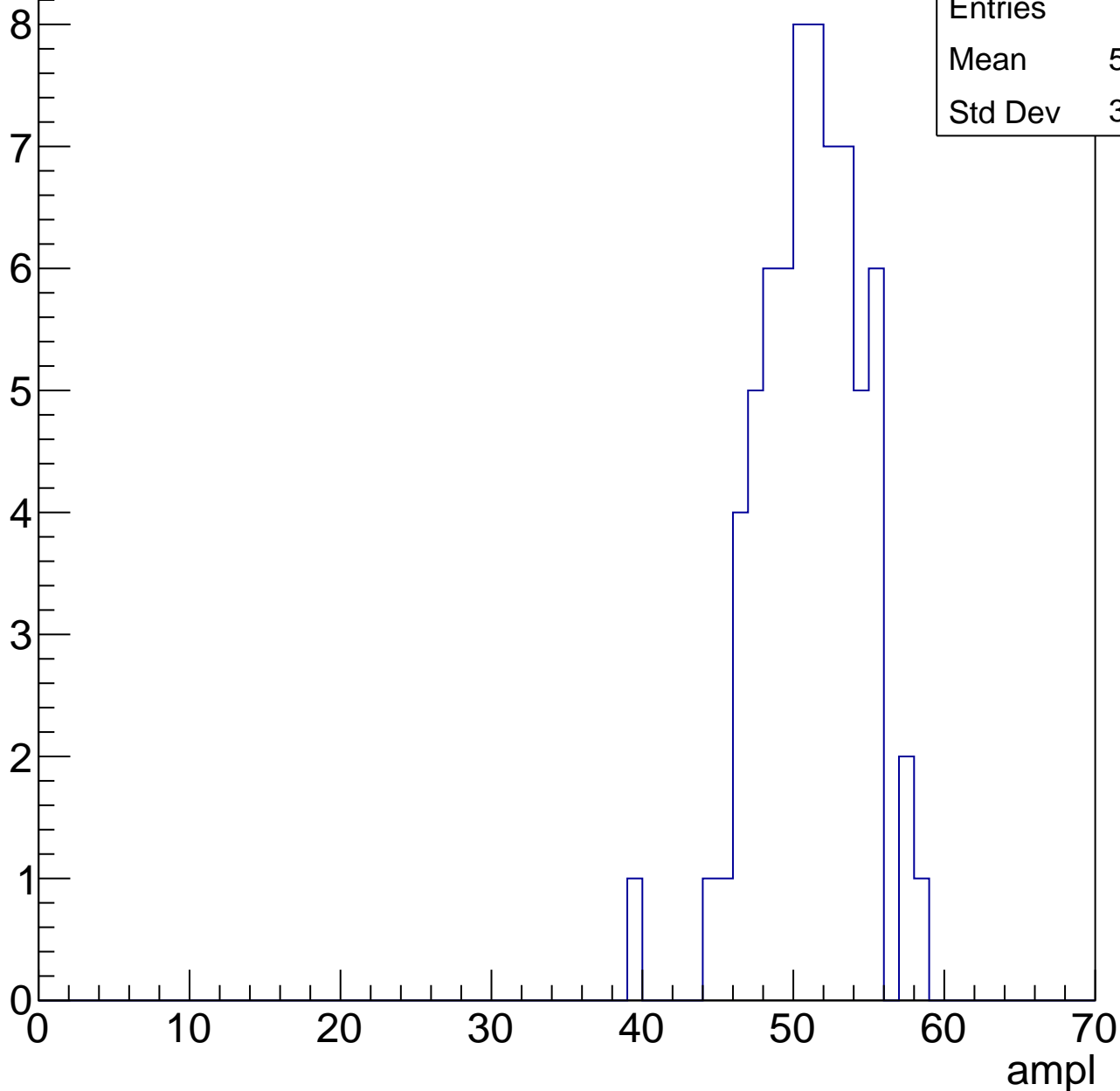


# B1L101S, U18-ch33, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	50.65
Std Dev	3.394



# B1L101S, U18-ch33, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

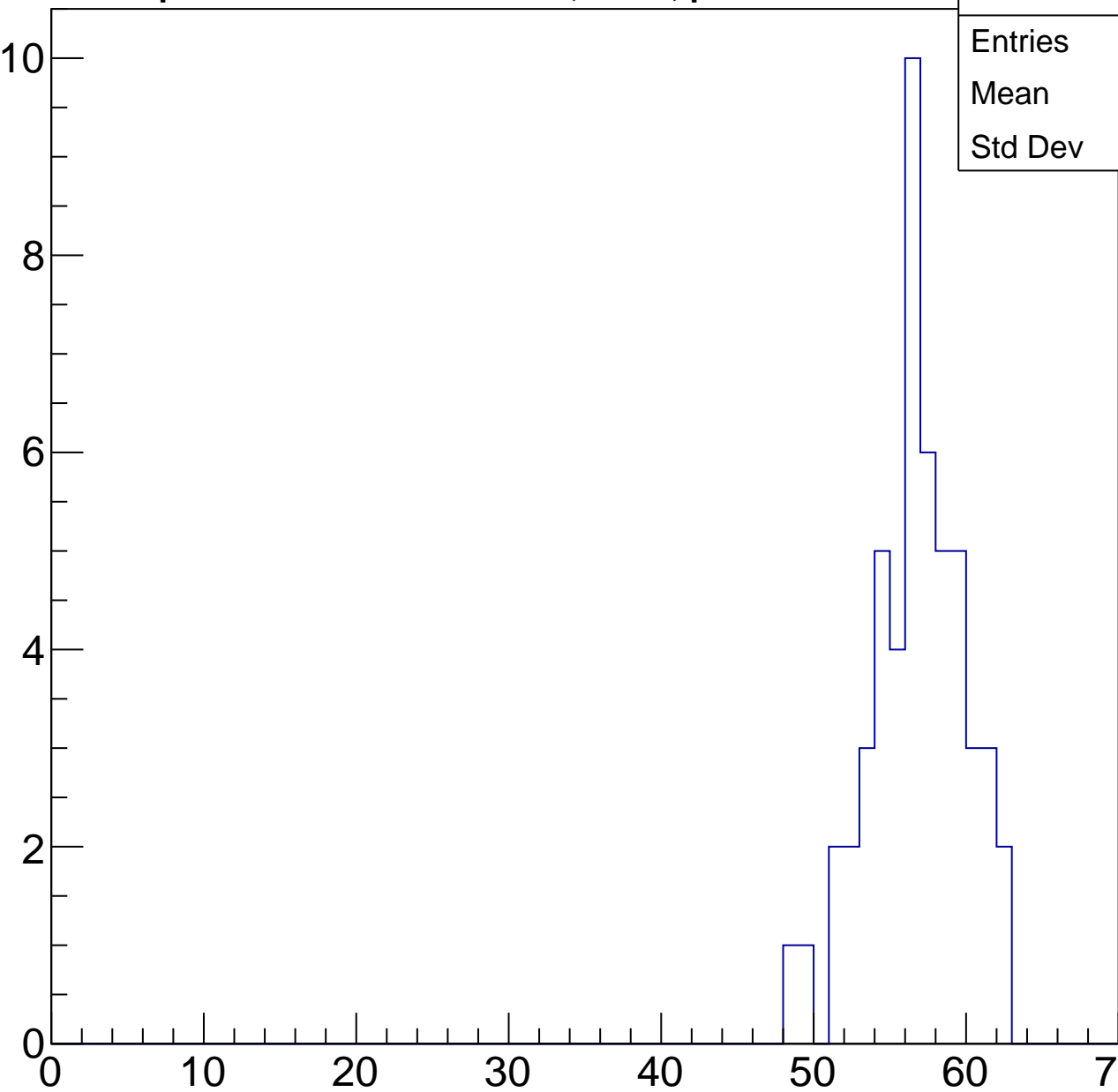
Entries	52
Mean	56.27
Std Dev	3.126

Entry

10  
8  
6  
4  
2  
0

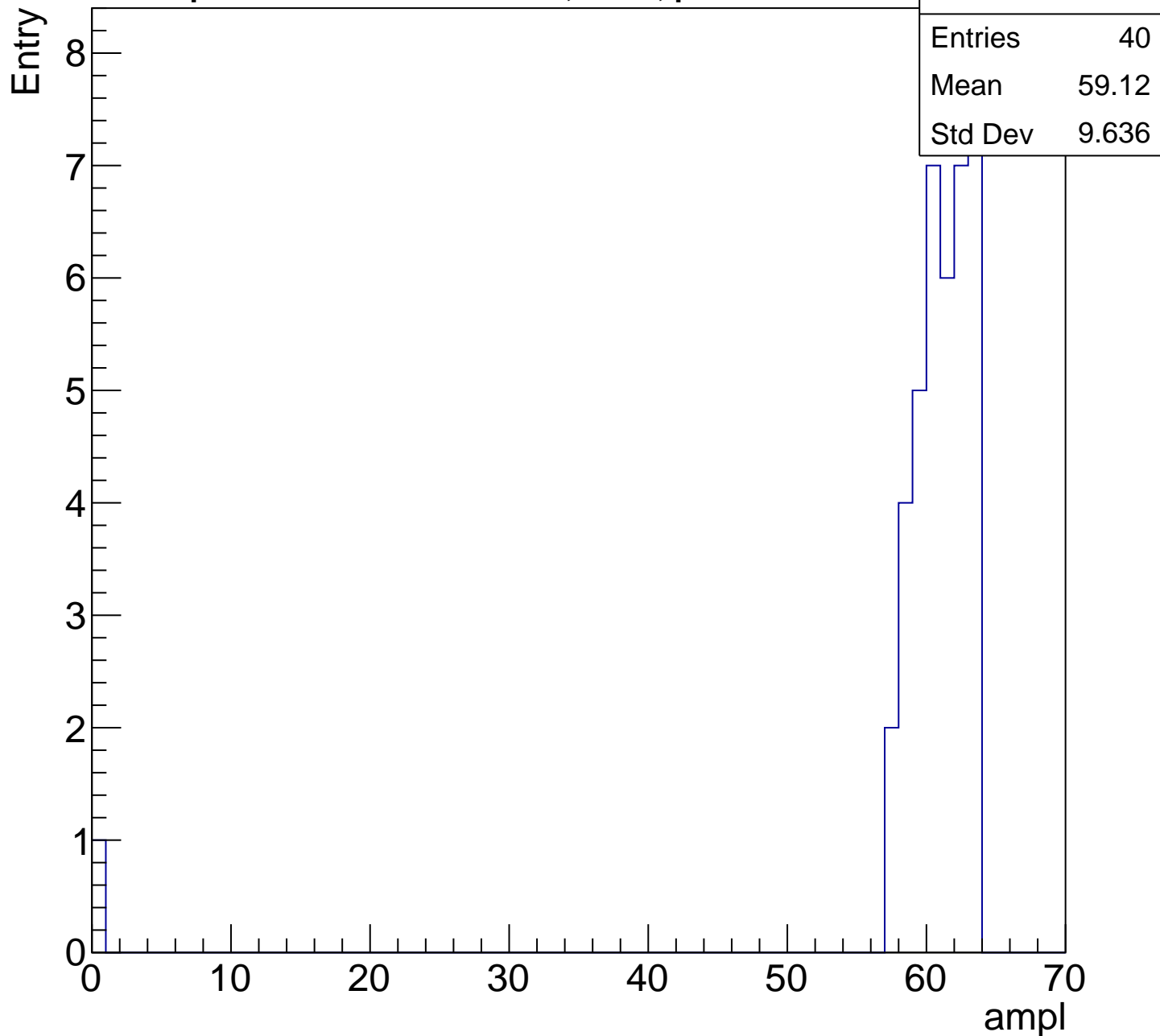
0 10 20 30 40 50 60 70

ampl



# B1L101S, U18-ch33, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U18-ch33, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch33, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U18-ch34, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	70
Mean	29.33
Std Dev	2.827

**Gaus mean : 30.0976**

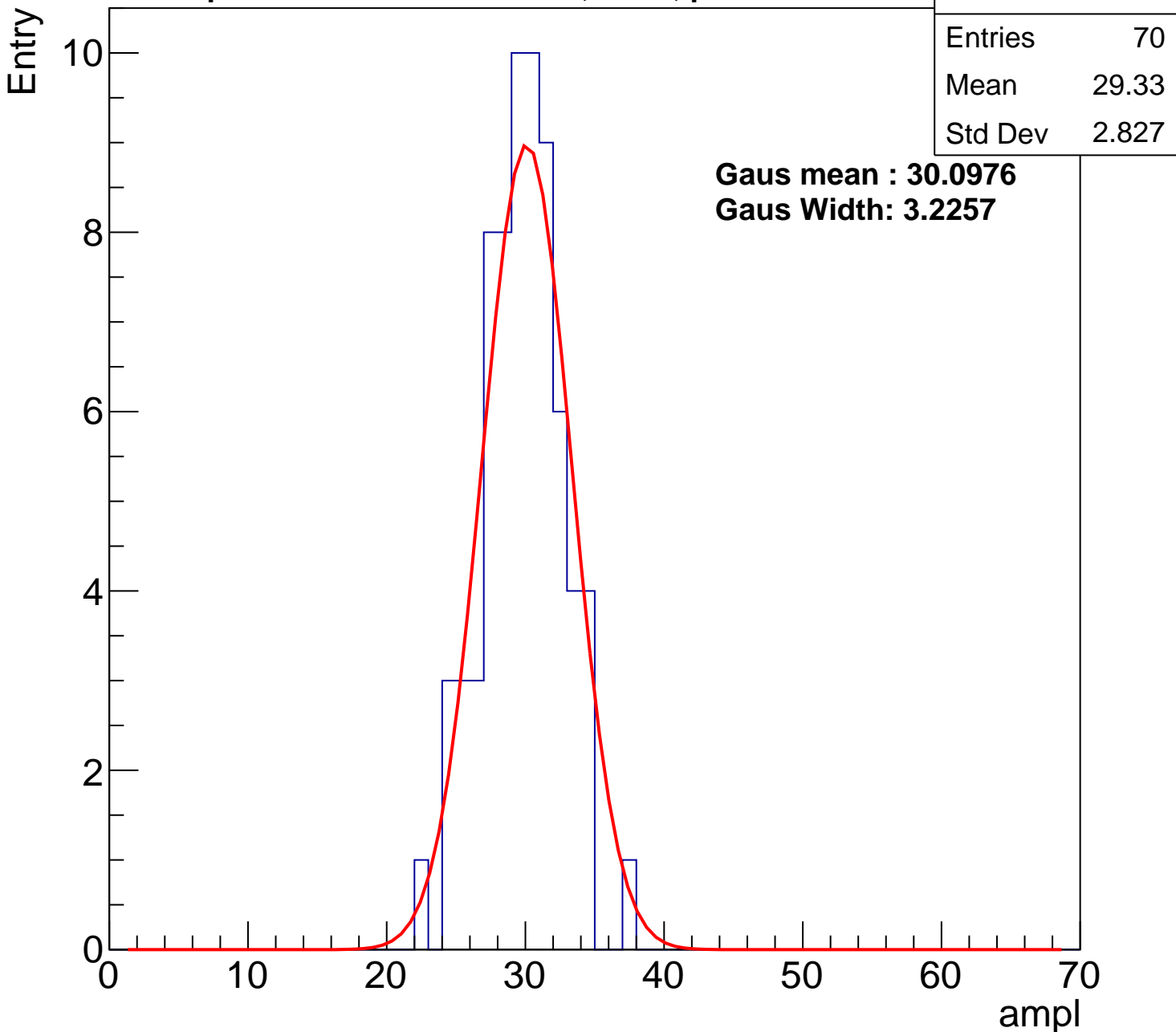
**Gaus Width: 3.2257**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U18-ch34, adc1

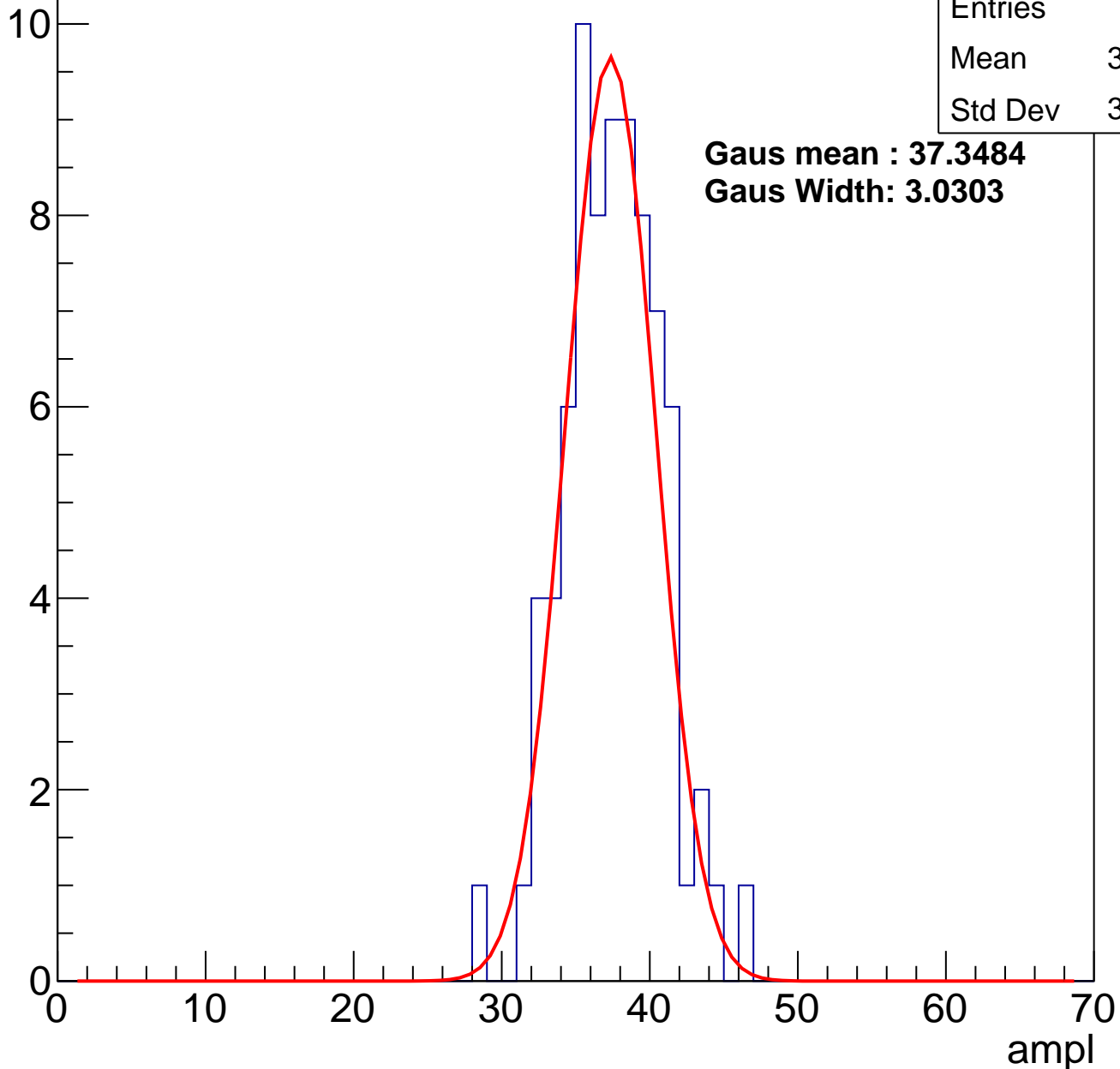
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	78
Mean	37.08
Std Dev	3.222

**Gaus mean : 37.3484**

**Gaus Width: 3.0303**

Entry



# B1L101S, U18-ch34, adc2

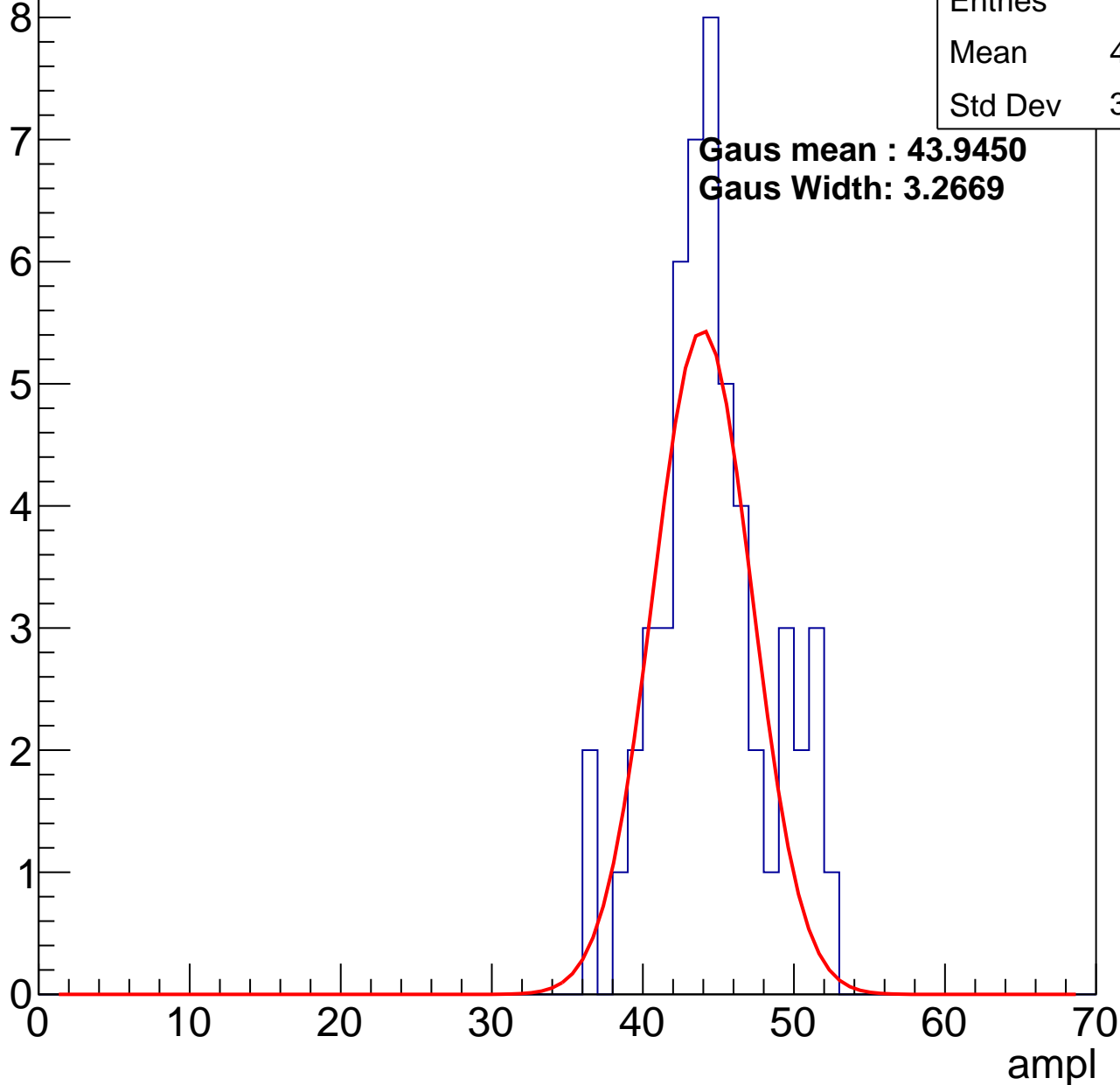
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	44.13
Std Dev	3.717

**Gaus mean : 43.9450**

**Gaus Width: 3.2669**

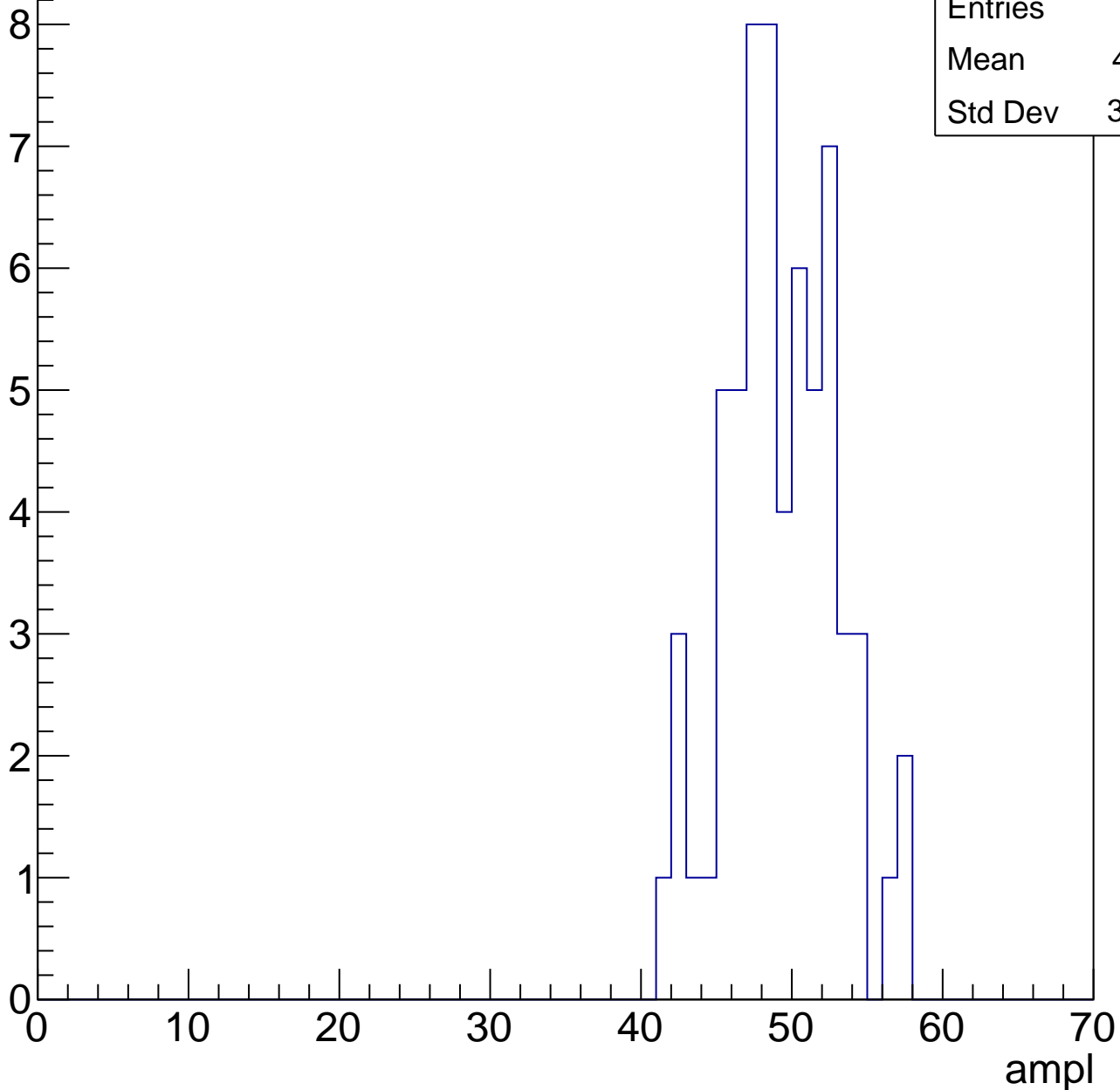


# B1L101S, U18-ch34, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	48.81
Std Dev	3.616

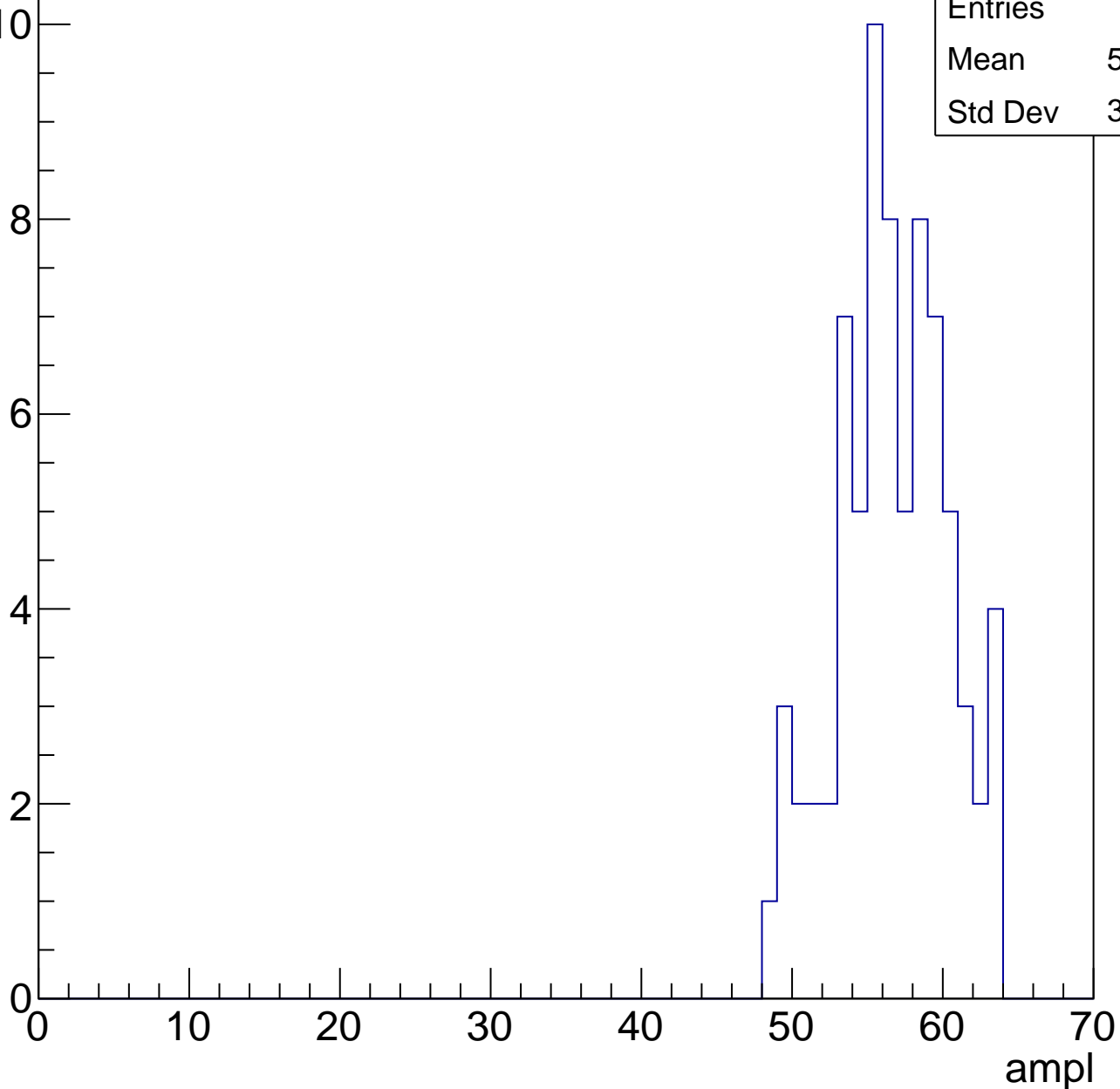


# B1L101S, U18-ch34, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	56.23
Std Dev	3.634

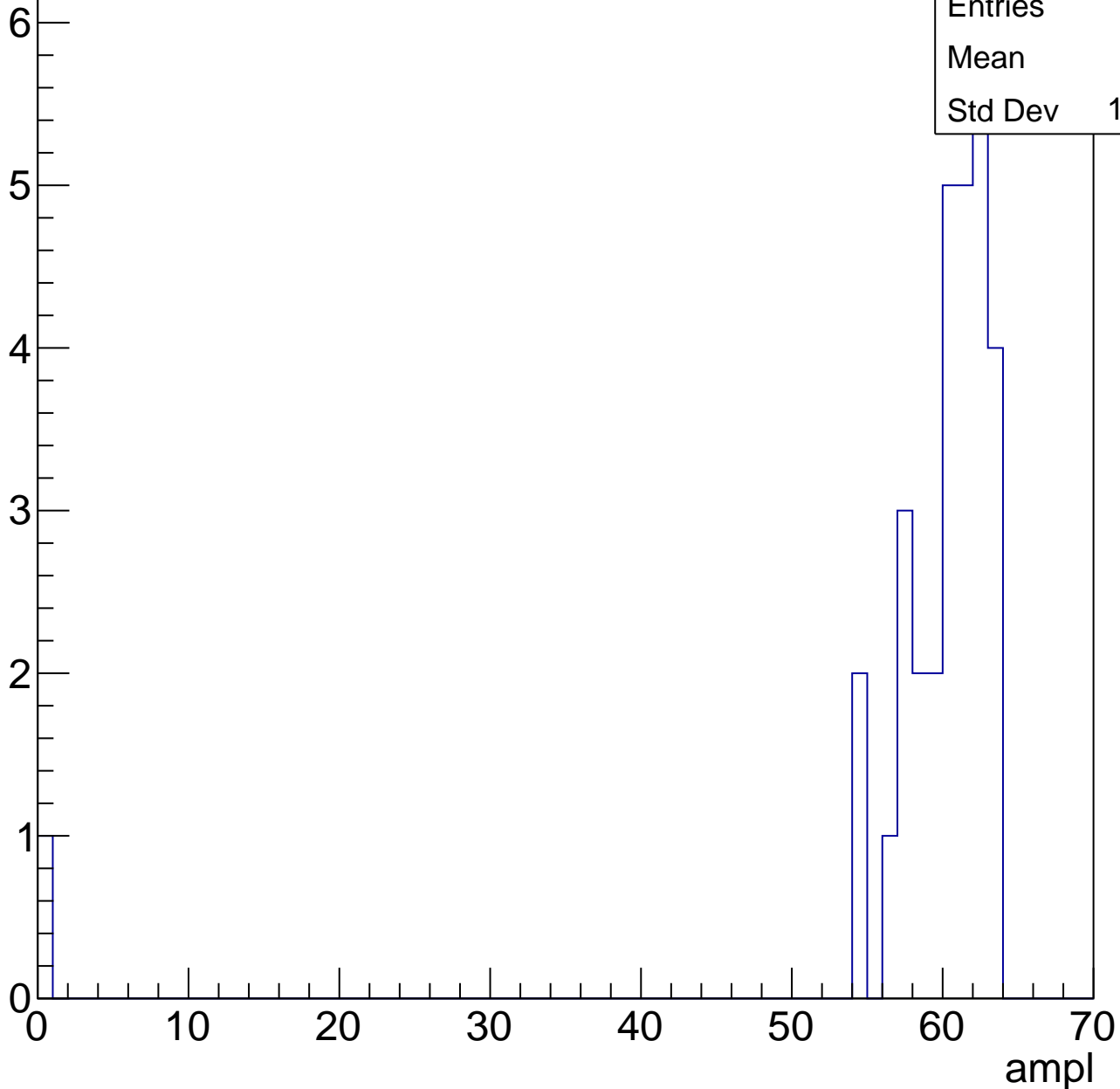


# B1L101S, U18-ch34, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

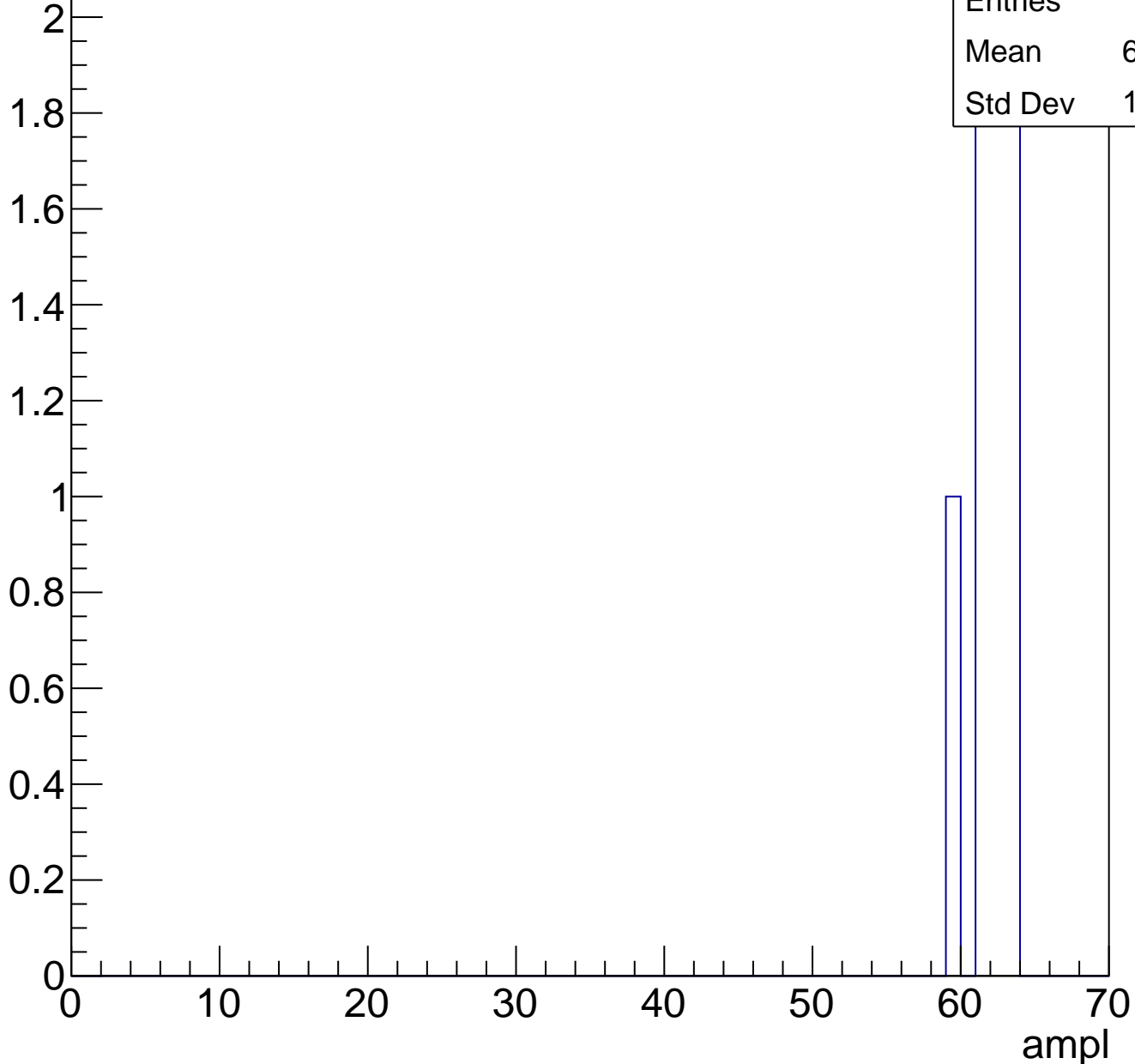
Entries	31
Mean	58
Std Dev	10.87



# B1L101S, U18-ch34, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch34, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U18-ch35, adc0

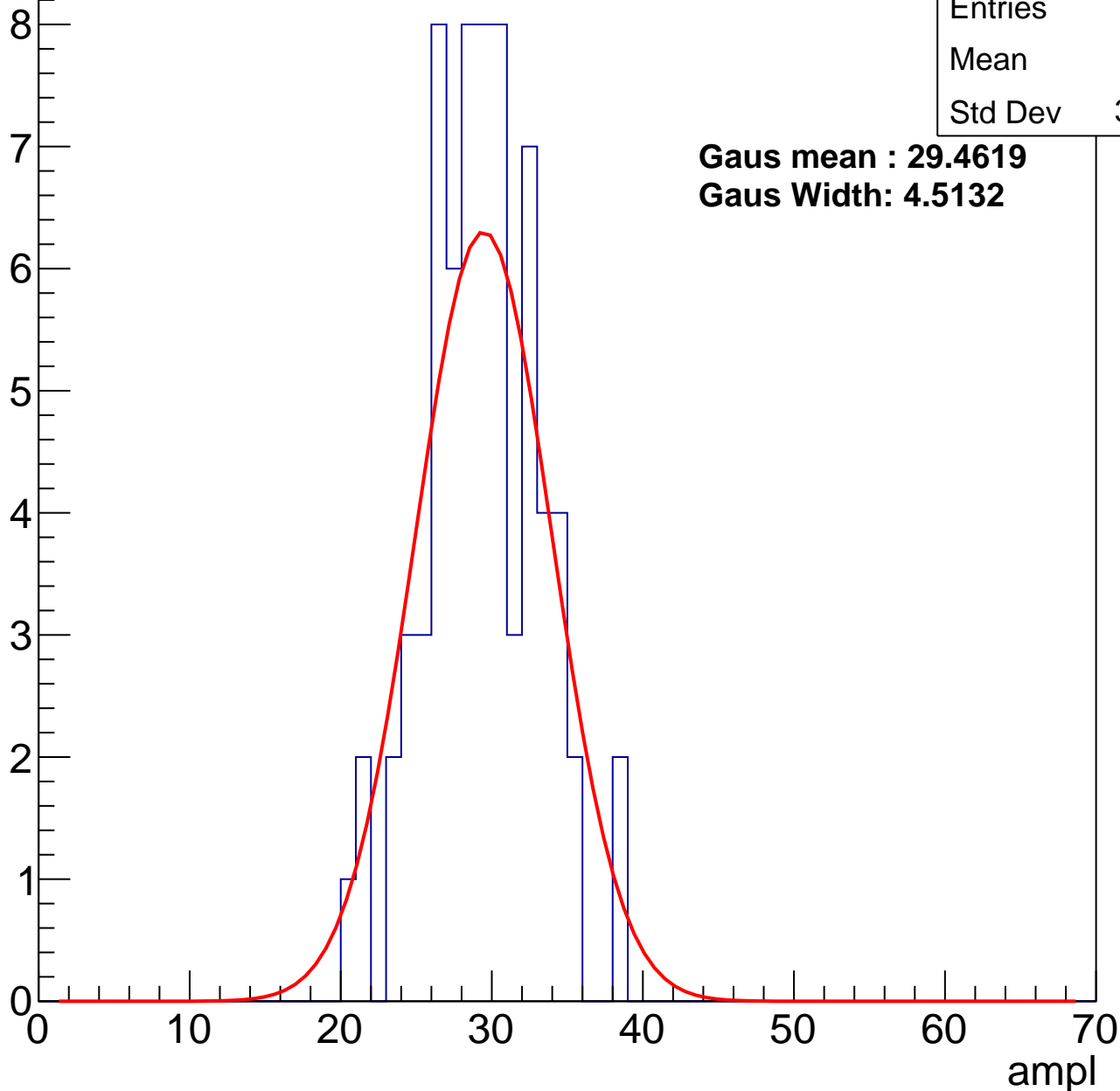
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	28.9
Std Dev	3.731

**Gaus mean : 29.4619**

**Gaus Width: 4.5132**



# B1L101S, U18-ch35, adc1

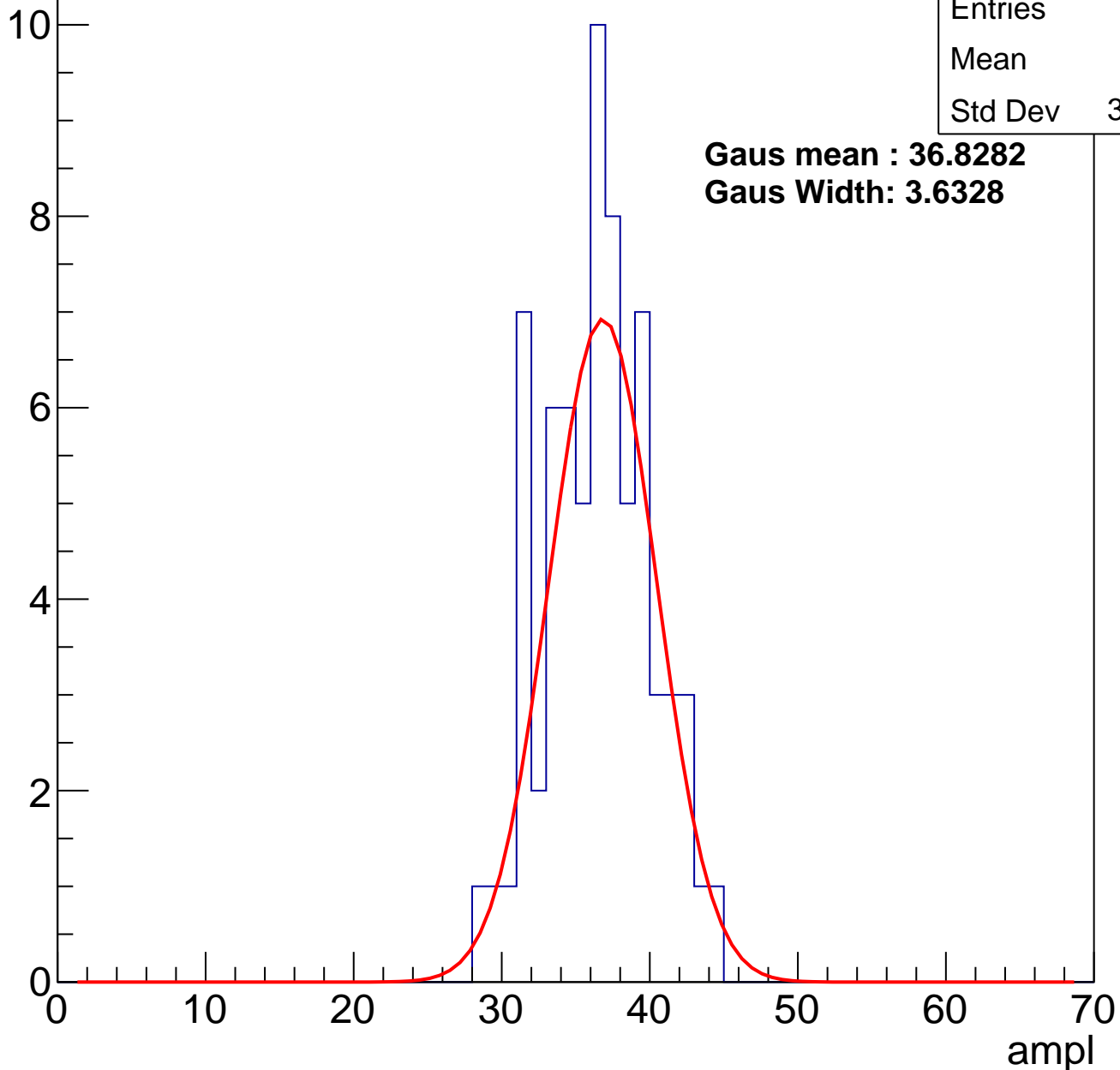
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	70
Mean	36
Std Dev	3.534

**Gaus mean : 36.8282**

**Gaus Width: 3.6328**

Entry



# B1L101S, U18-ch35, adc2

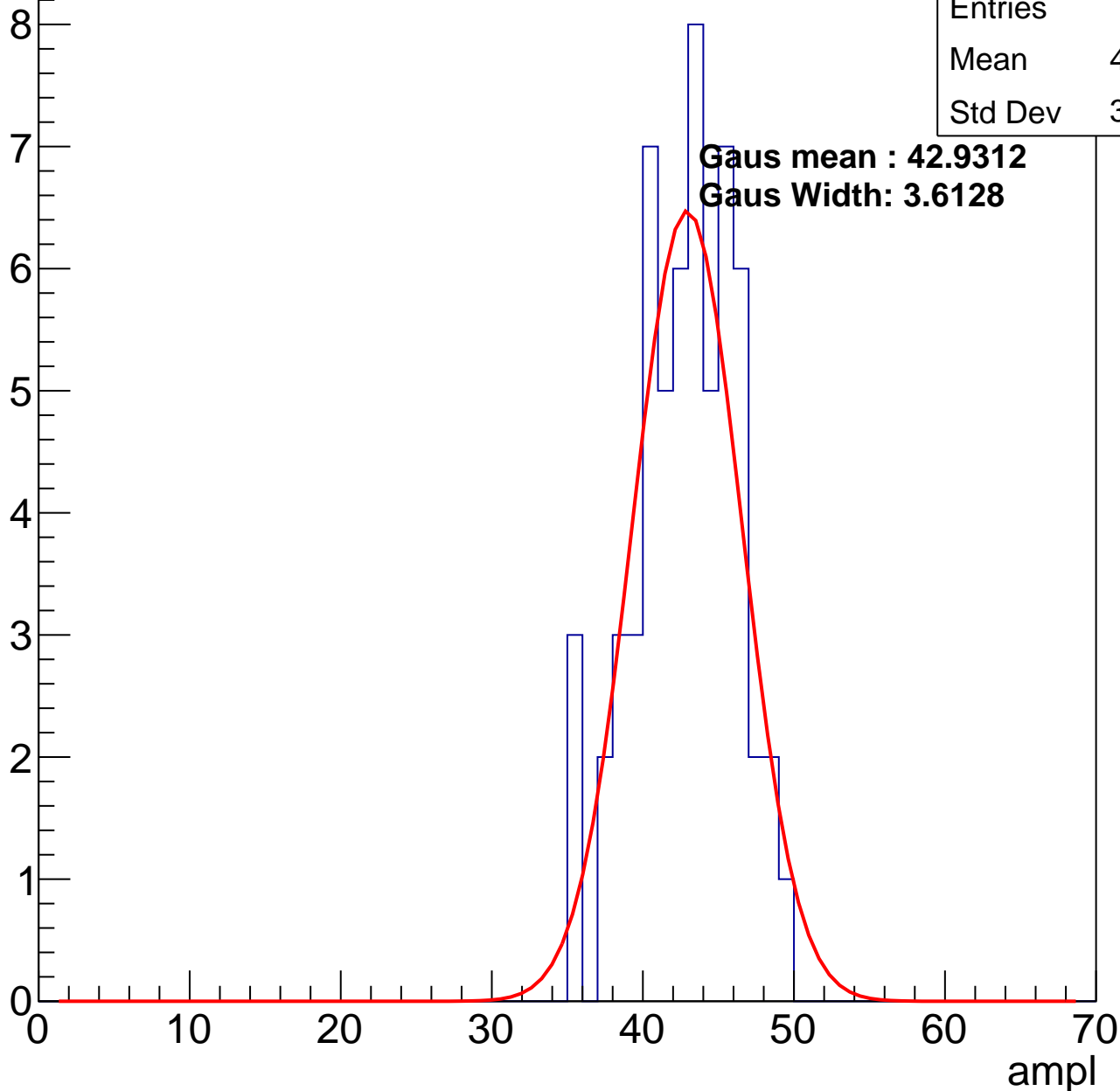
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	42.35
Std Dev	3.306

**Gaus mean : 42.9312**

**Gaus Width: 3.6128**

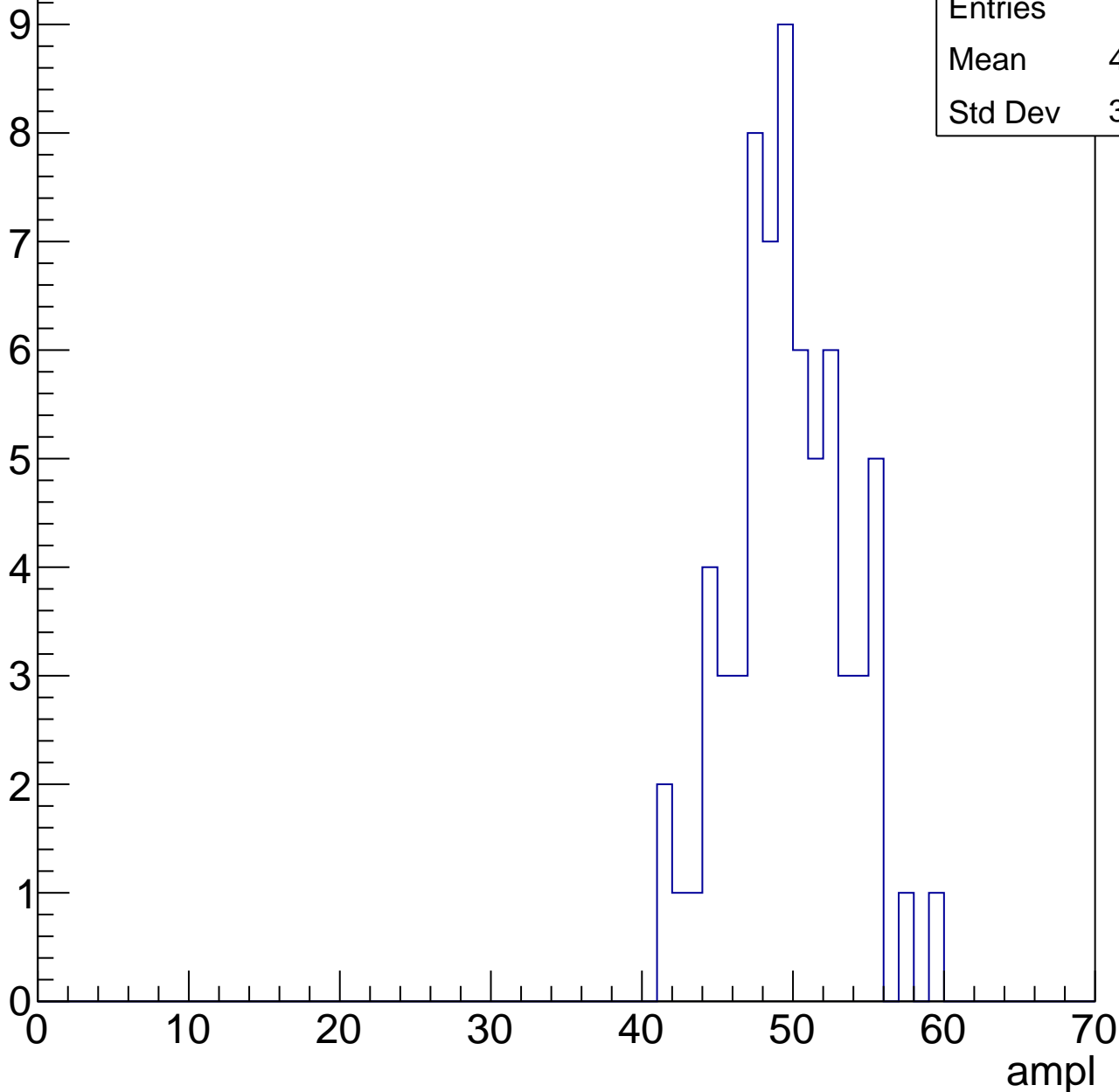


# B1L101S, U18-ch35, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	49.24
Std Dev	3.777

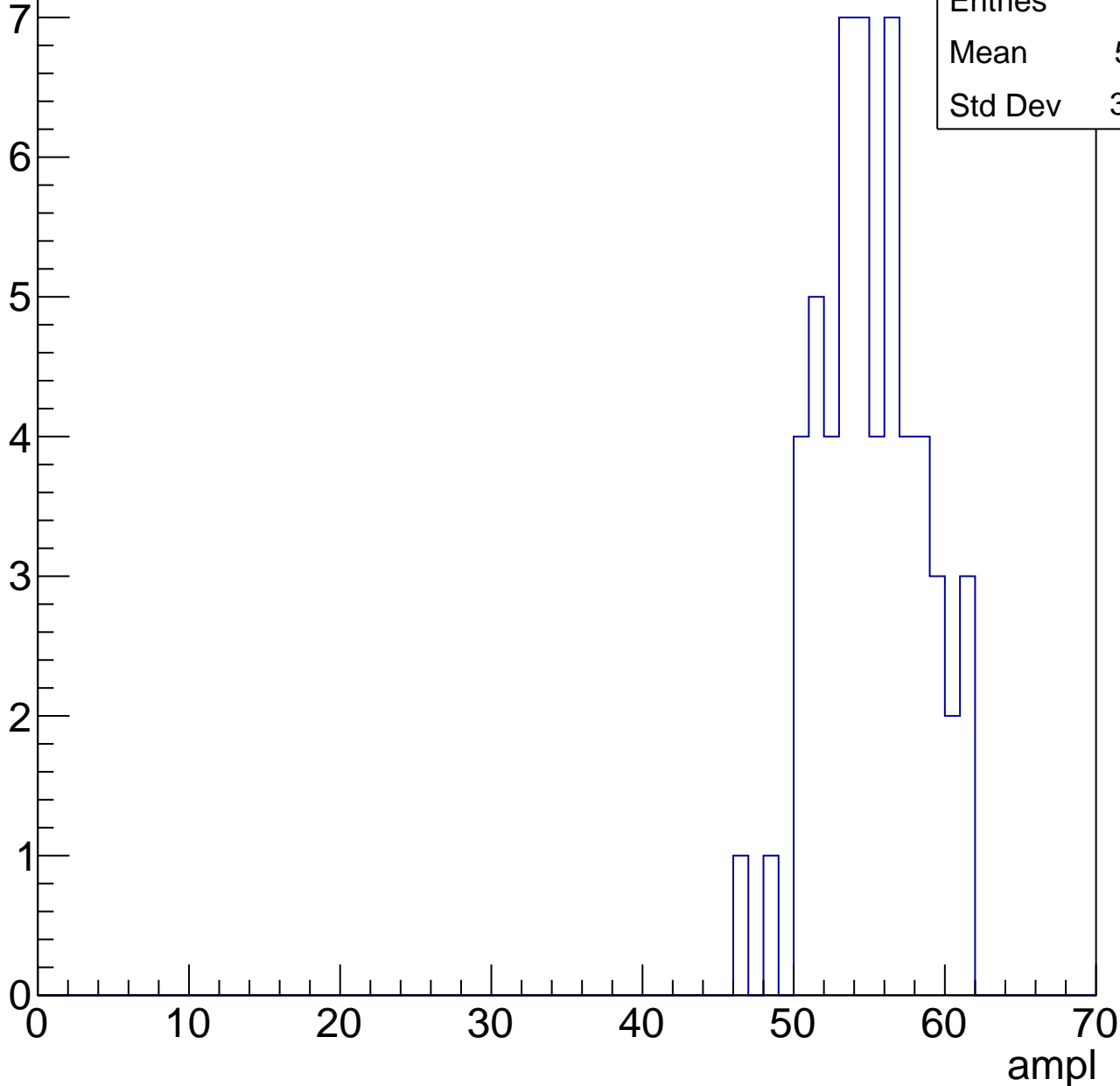


# B1L101S, U18-ch35, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	54.61
Std Dev	3.374

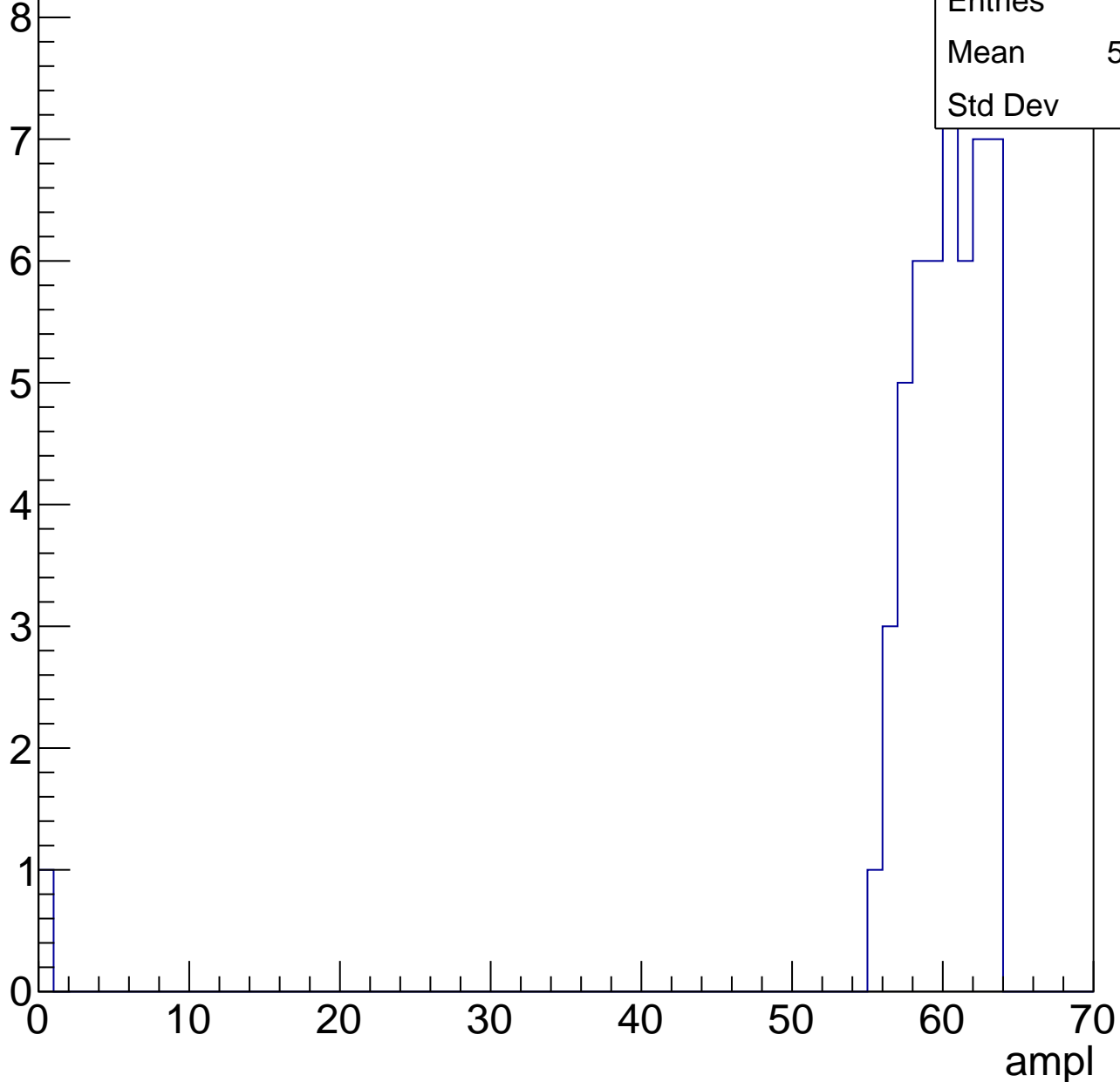


# B1L101S, U18-ch35, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	58.62
Std Dev	8.66



# B1L101S, U18-ch35, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch35, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U18-ch36, adc0

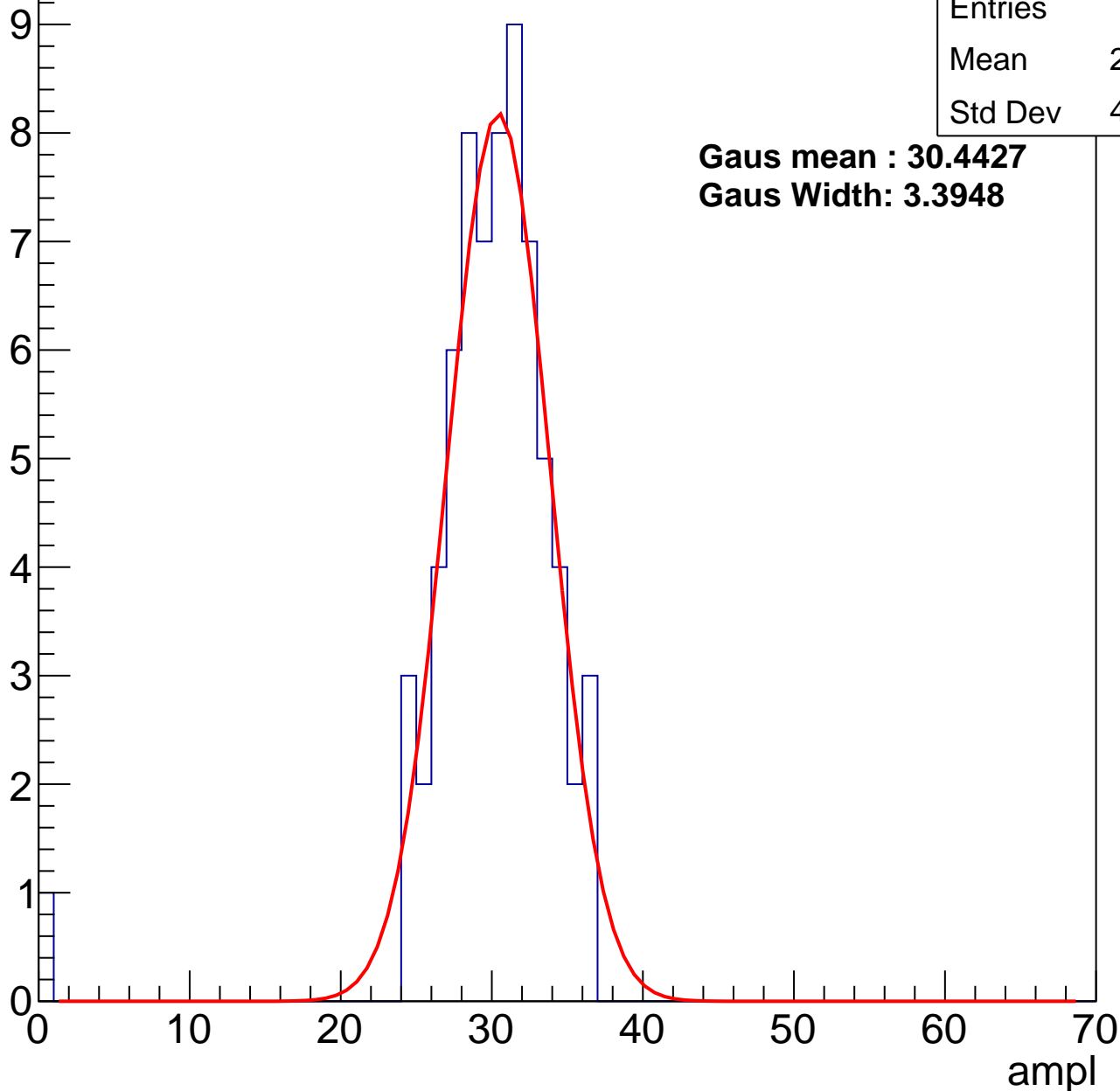
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	29.52
Std Dev	4.668

**Gaus mean : 30.4427**

**Gaus Width: 3.3948**



# B1L101S, U18-ch36, adc1

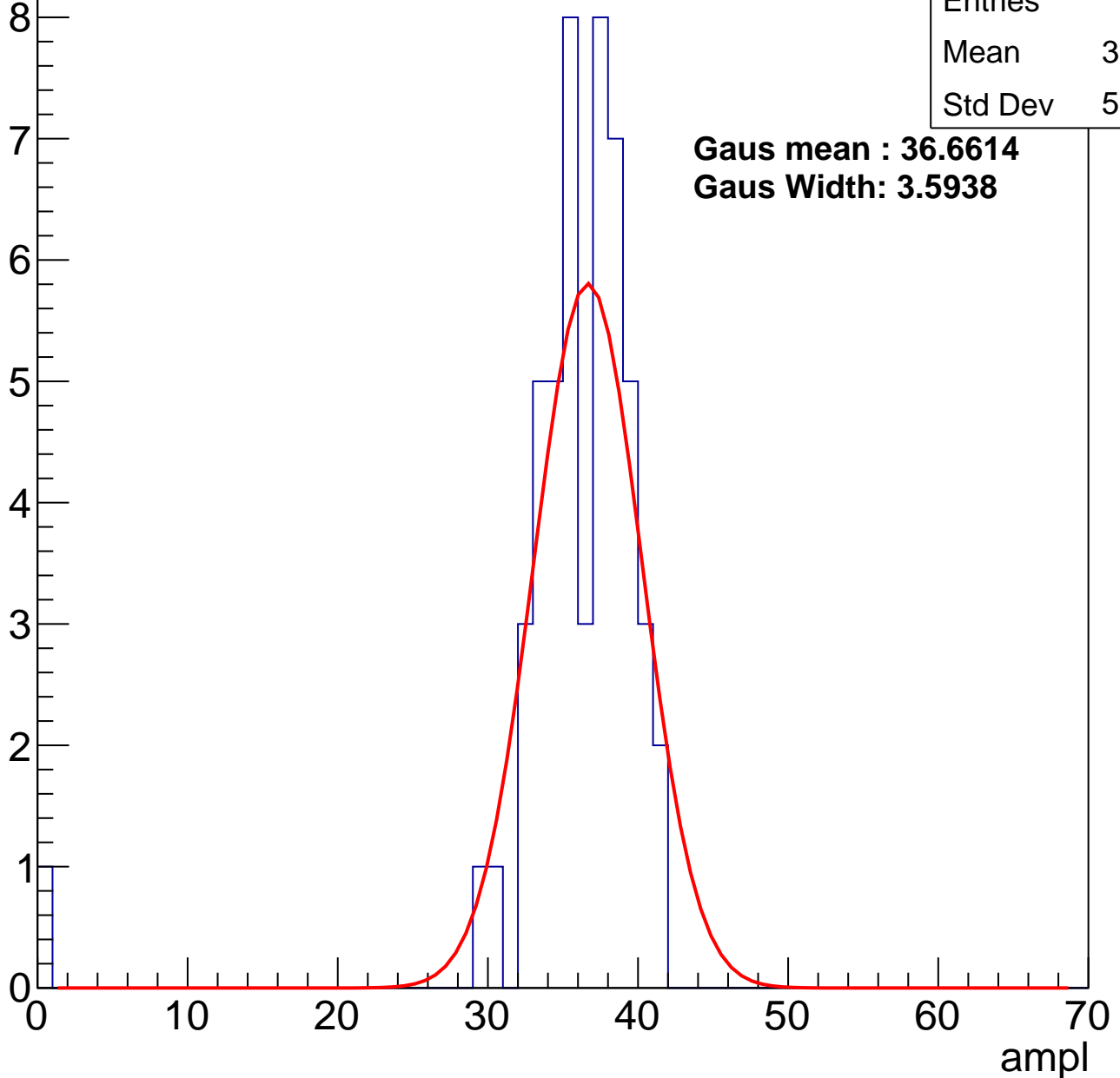
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	35.33
Std Dev	5.646

**Gaus mean : 36.6614**

**Gaus Width: 3.5938**



# B1L101S, U18-ch36, adc2

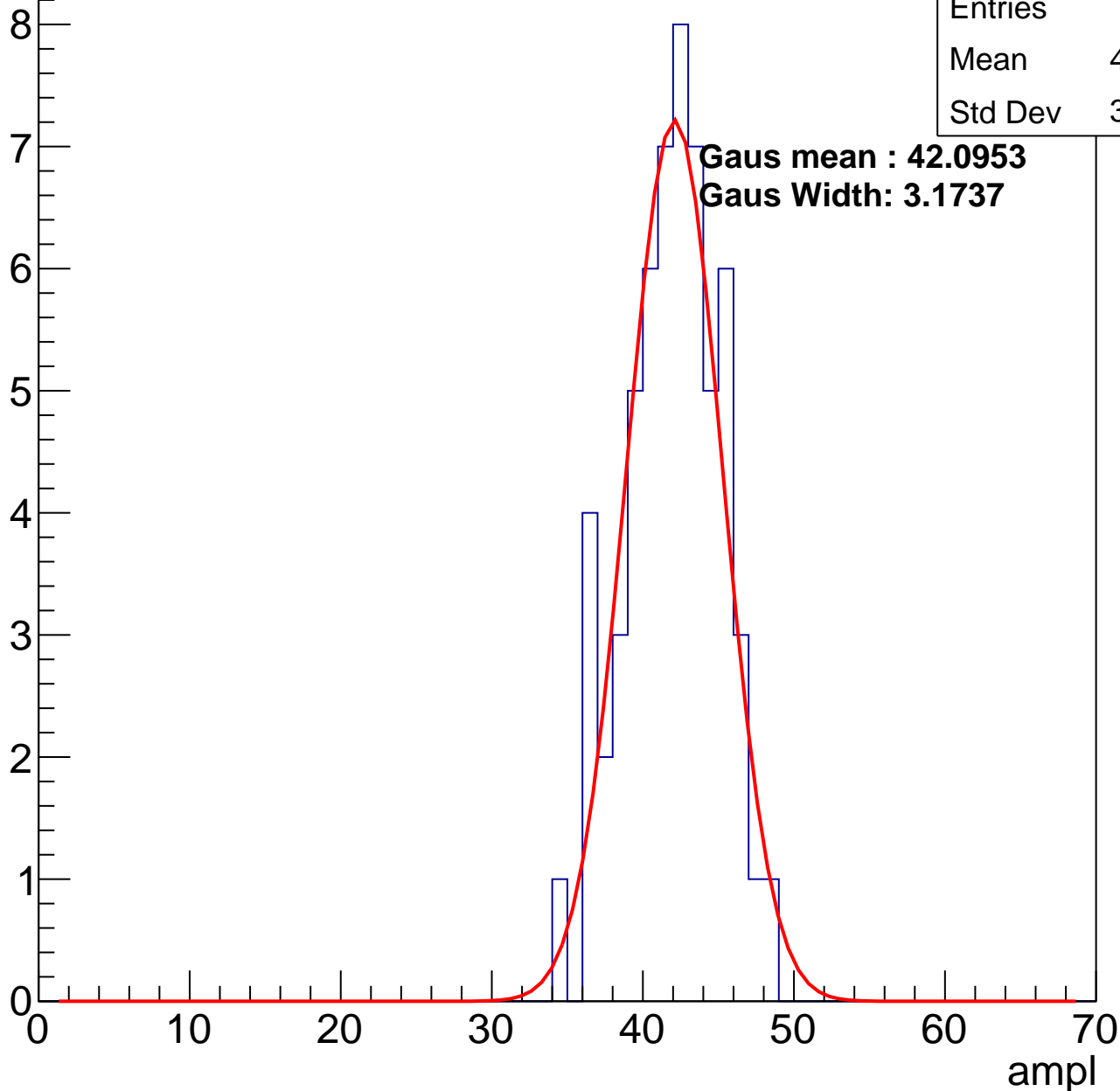
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	41.49
Std Dev	3.072

**Gaus mean : 42.0953**

**Gaus Width: 3.1737**



# B1L101S, U18-ch36, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	87
Mean	49
Std Dev	3.93

Entry

10

8

6

4

2

0

0

10

20

30

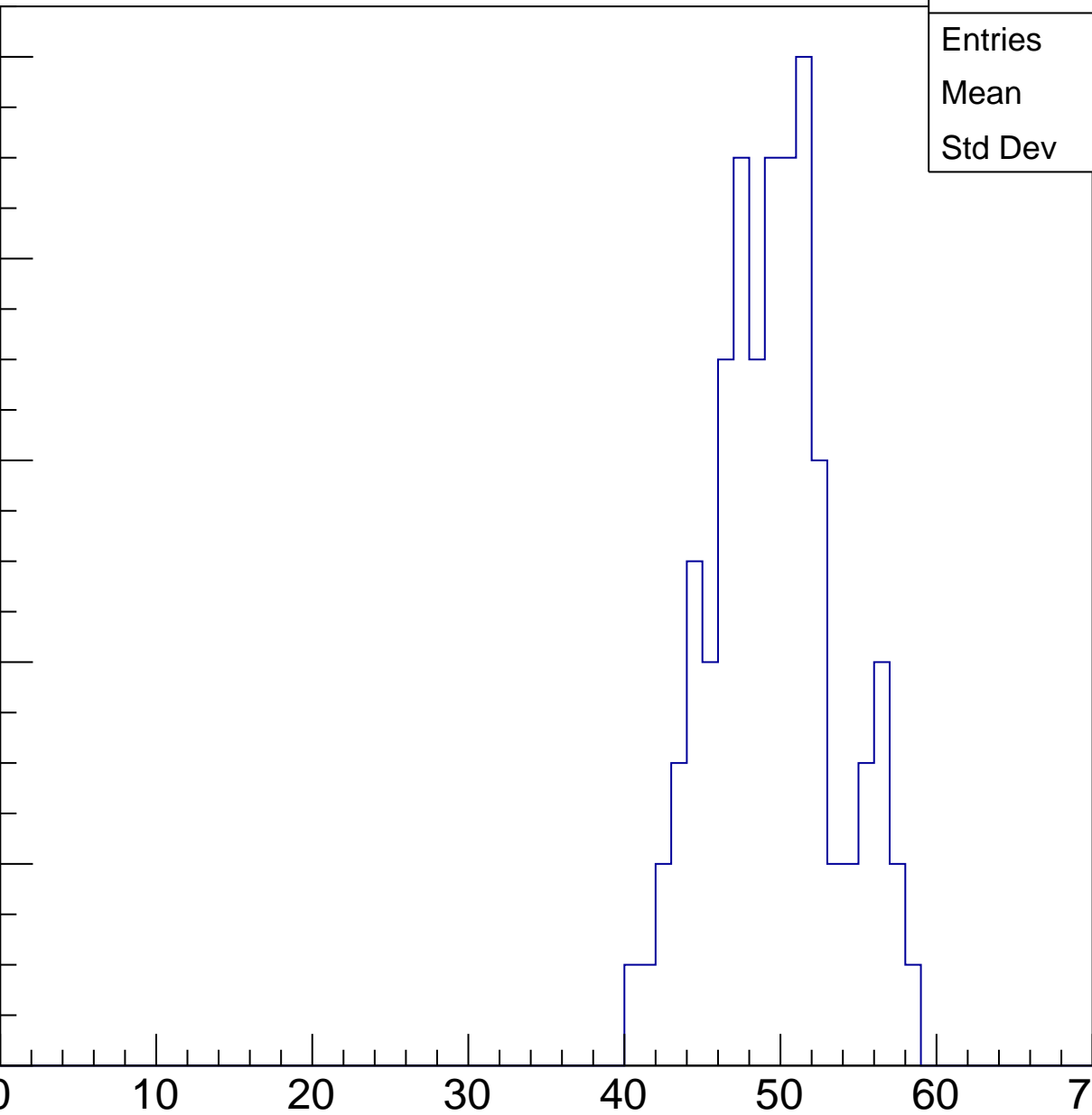
40

50

60

ampl

70

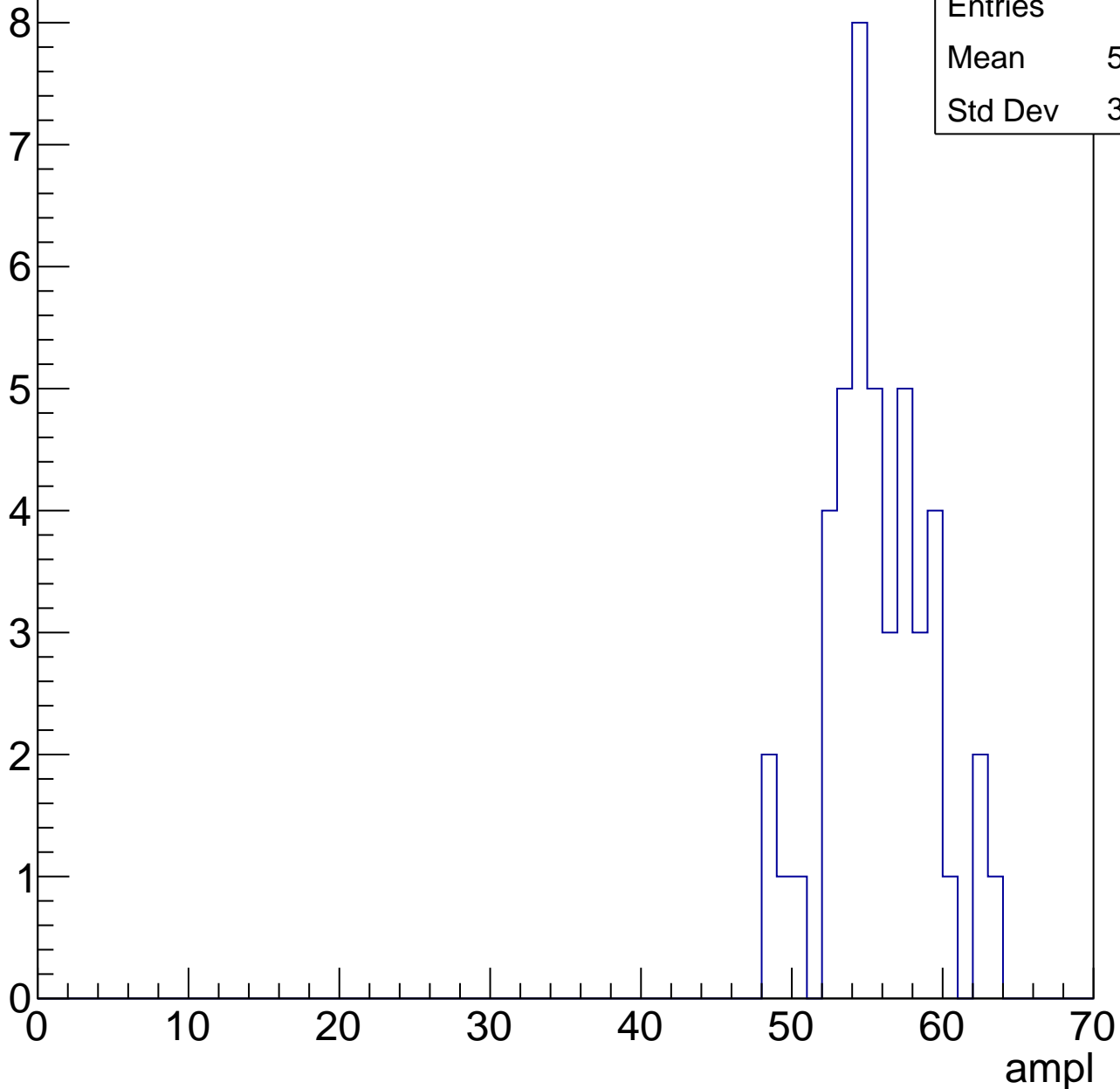


# B1L101S, U18-ch36, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	45
Mean	55.22
Std Dev	3.405

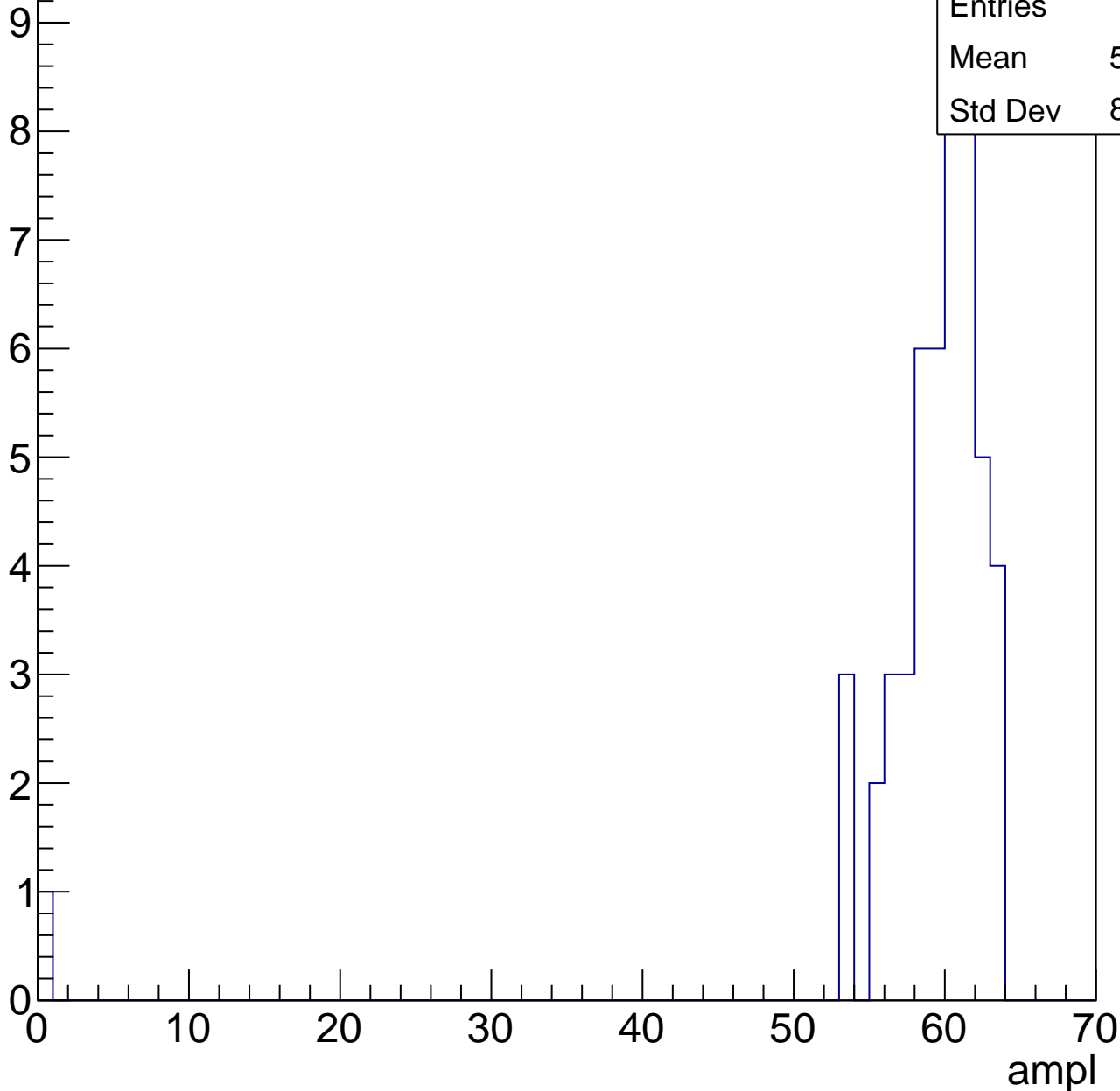


# B1L101S, U18-ch36, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	58.06
Std Dev	8.603

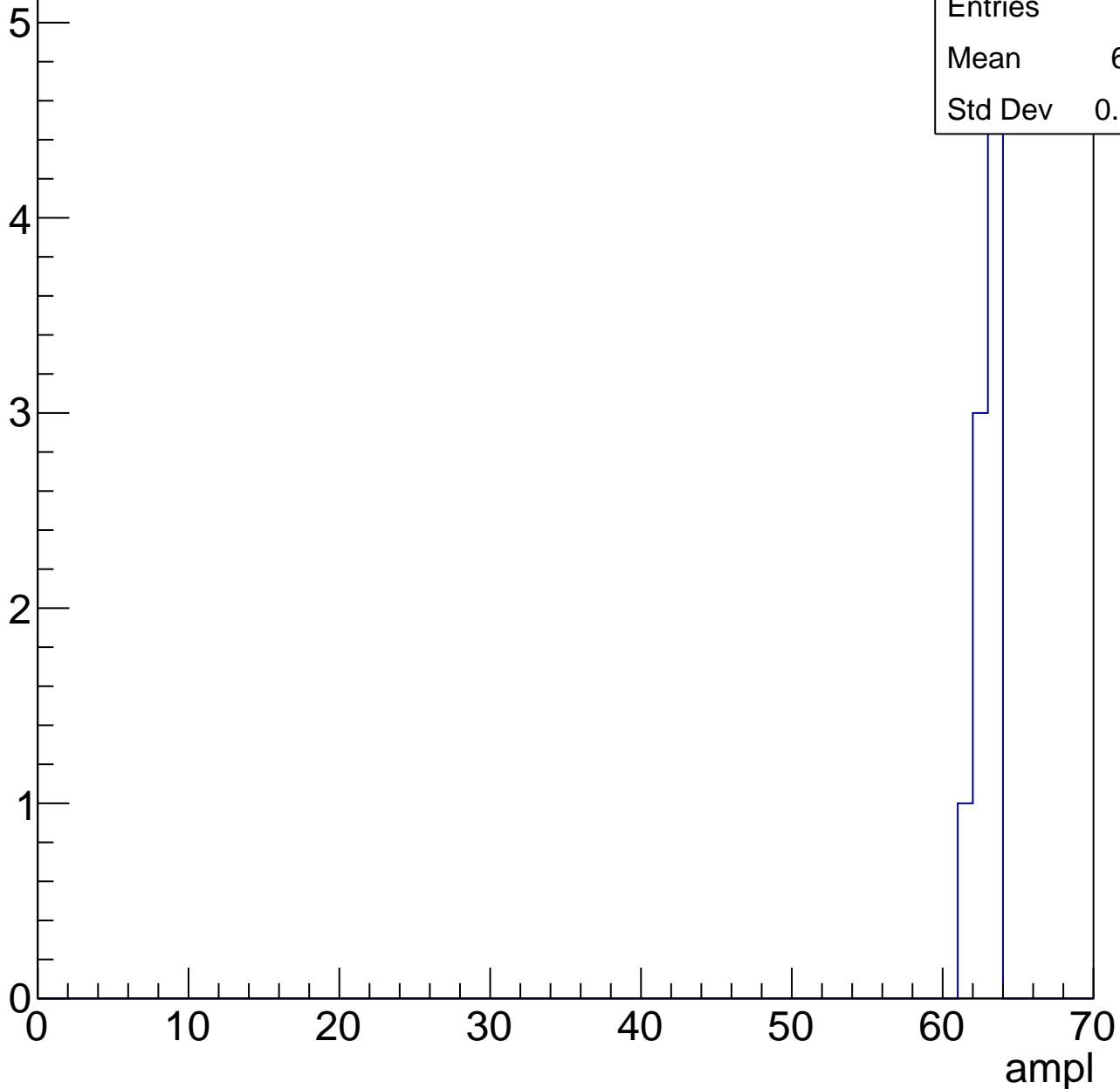


# B1L101S, U18-ch36, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	9
Mean	62.44
Std Dev	0.6849





# B1L101S, U18-ch36, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U18-ch37, adc0

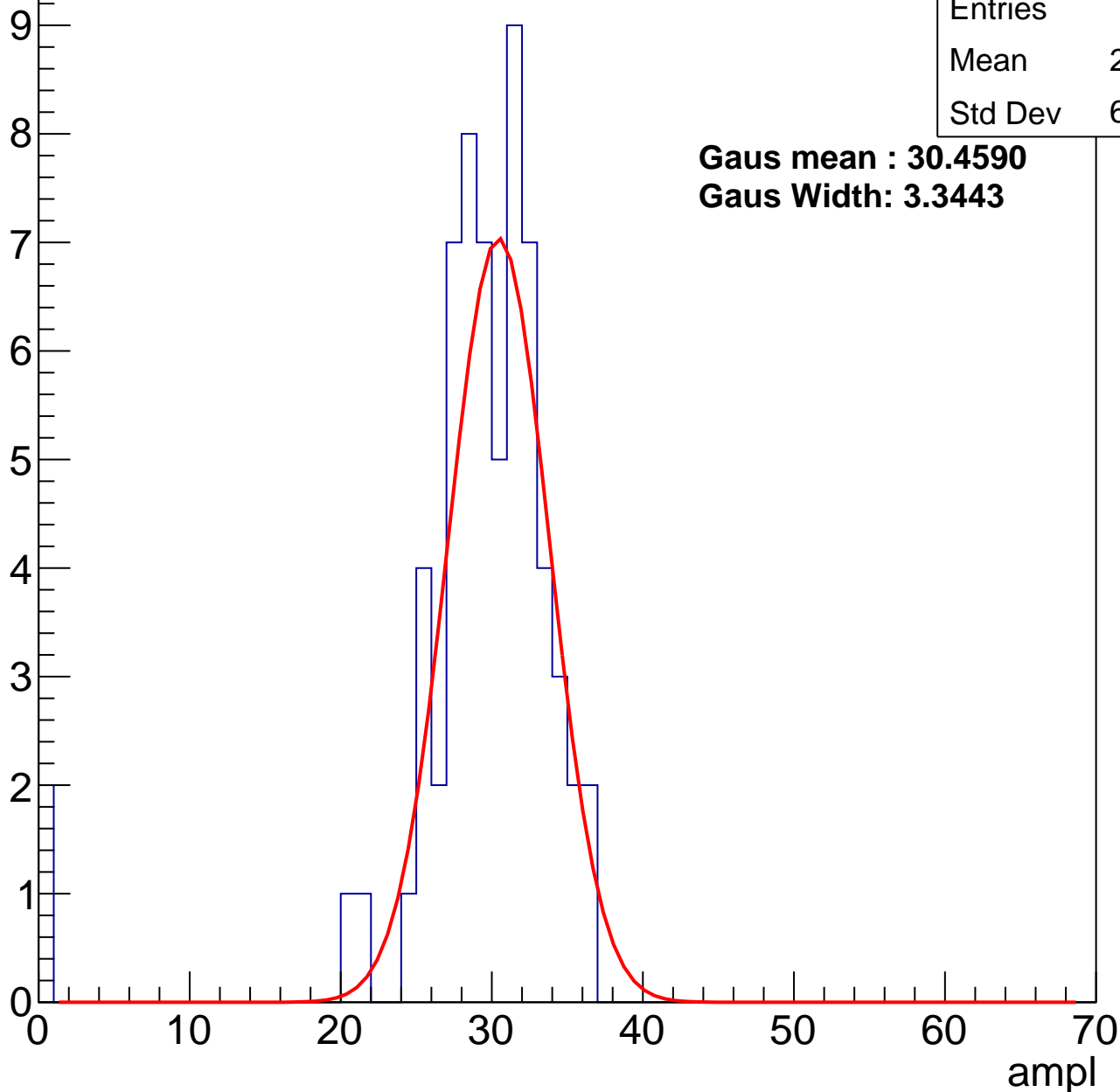
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	28.65
Std Dev	6.045

**Gaus mean : 30.4590**

**Gaus Width: 3.3443**



# B1L101S, U18-ch37, adc1

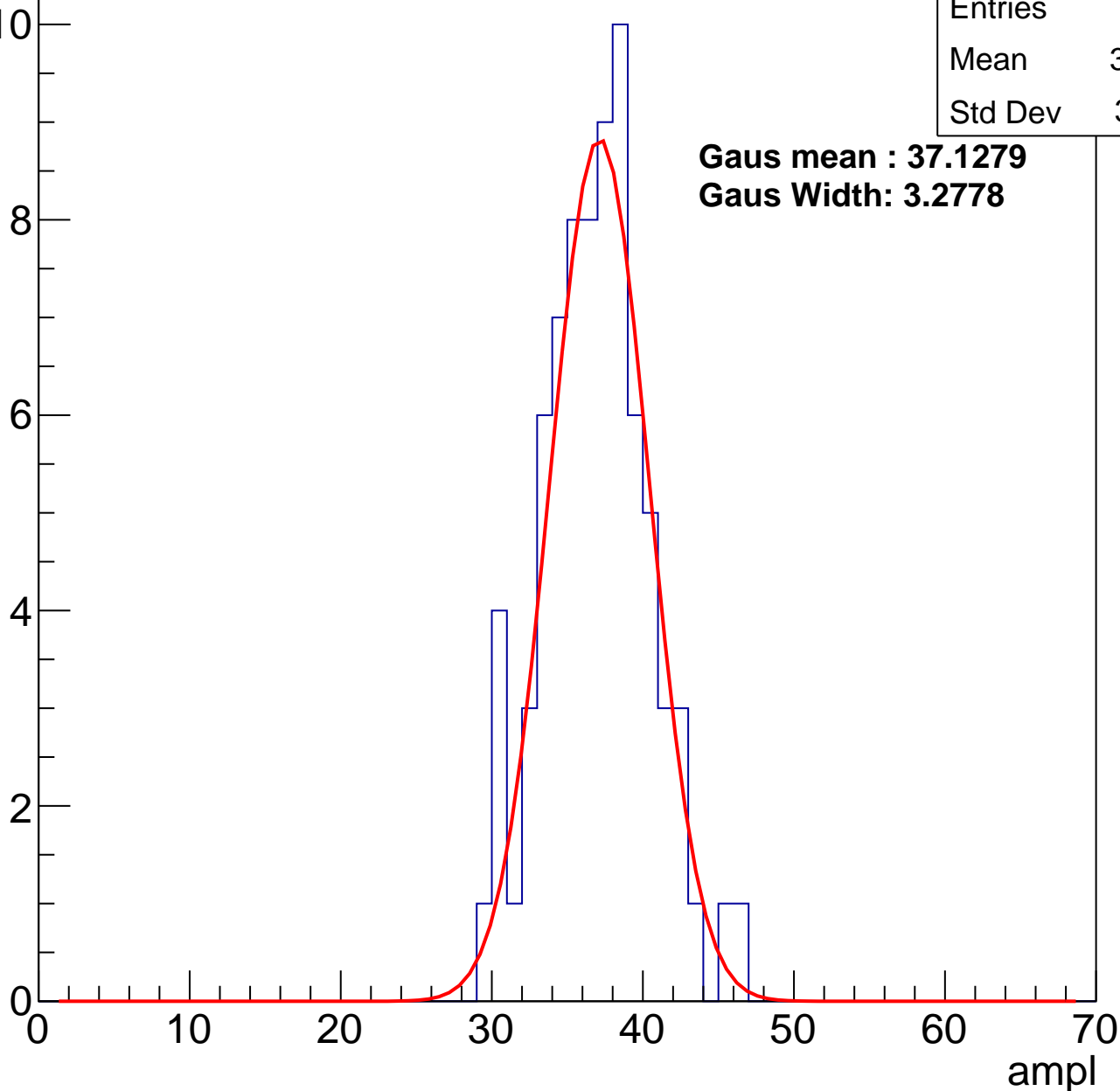
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	36.49
Std Dev	3.481

**Gaus mean : 37.1279**

**Gaus Width: 3.2778**



# B1L101S, U18-ch37, adc2

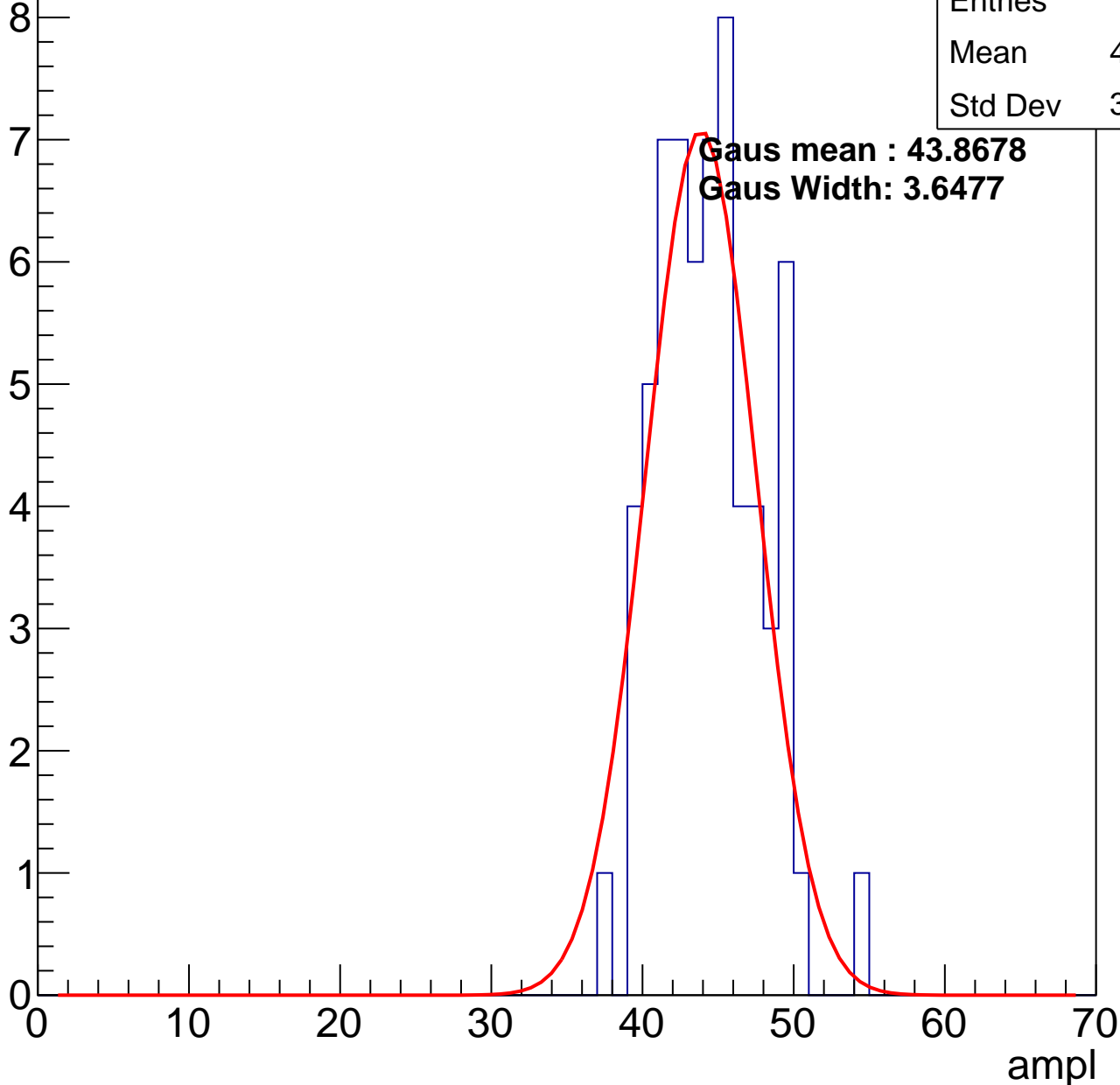
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	43.97
Std Dev	3.354

**Gaus mean : 43.8678**

**Gaus Width: 3.6477**



# B1L101S, U18-ch37, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

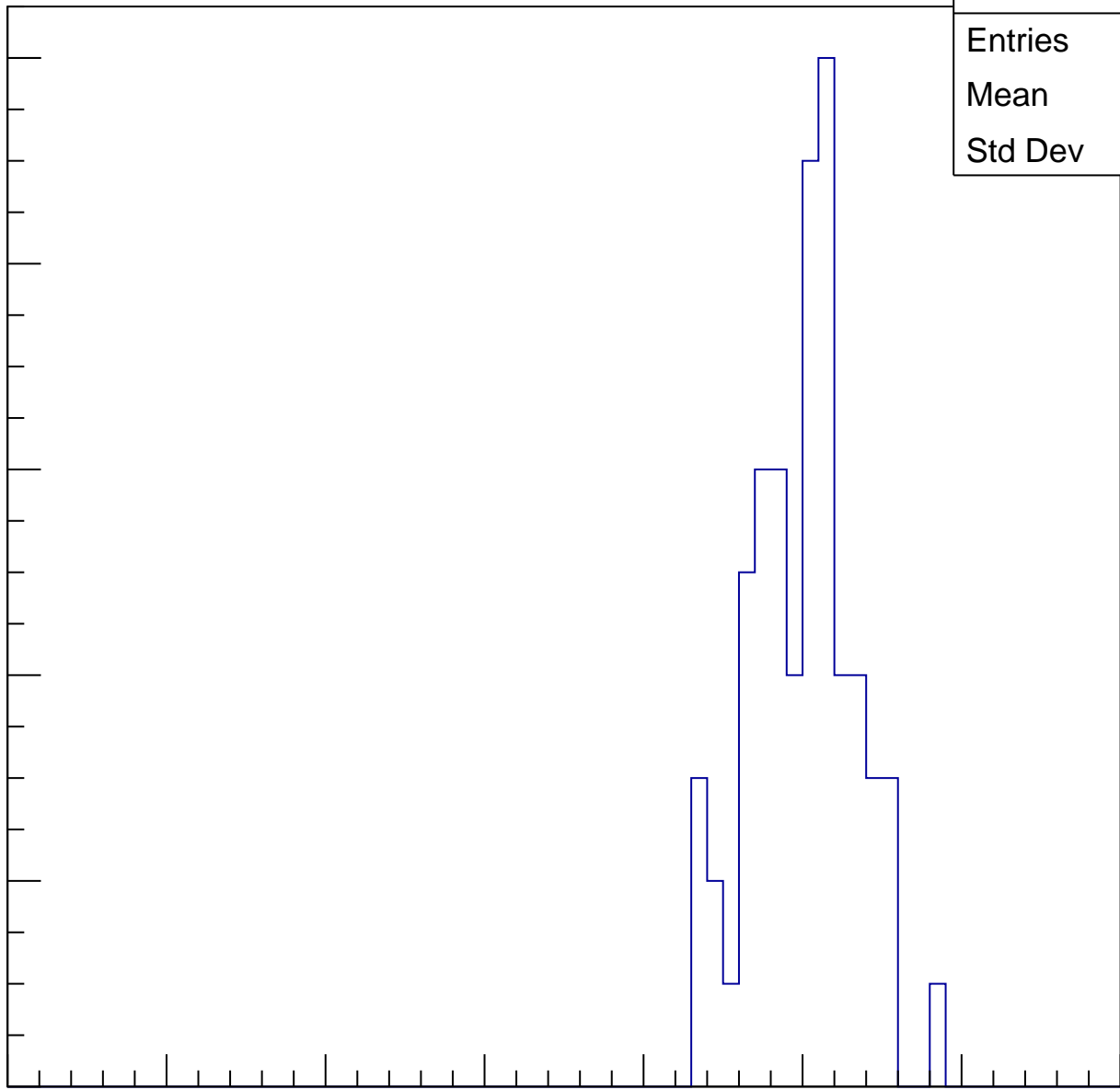
Entries	61
Mean	49.56
Std Dev	3.247

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

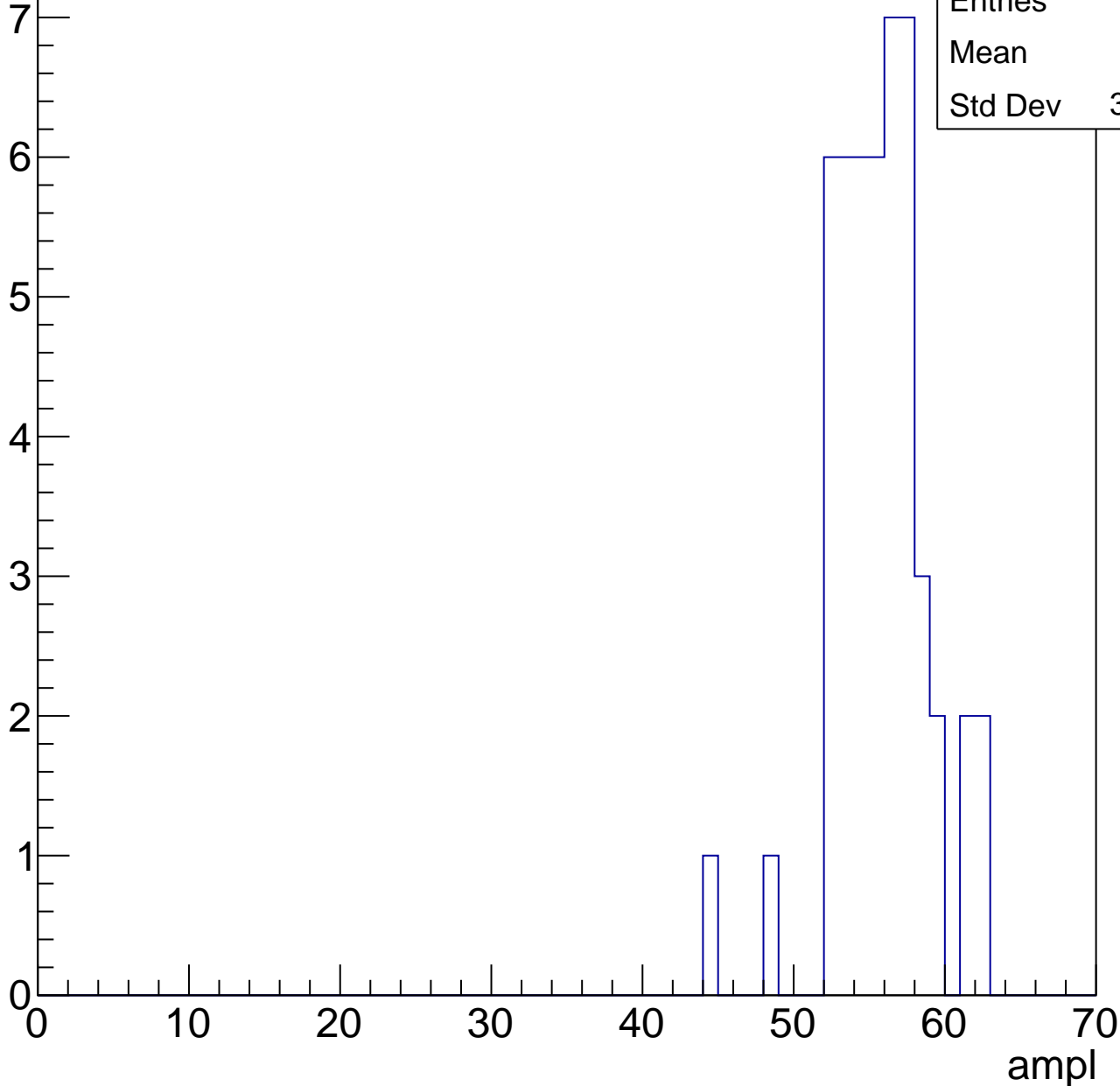


# B1L101S, U18-ch37, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

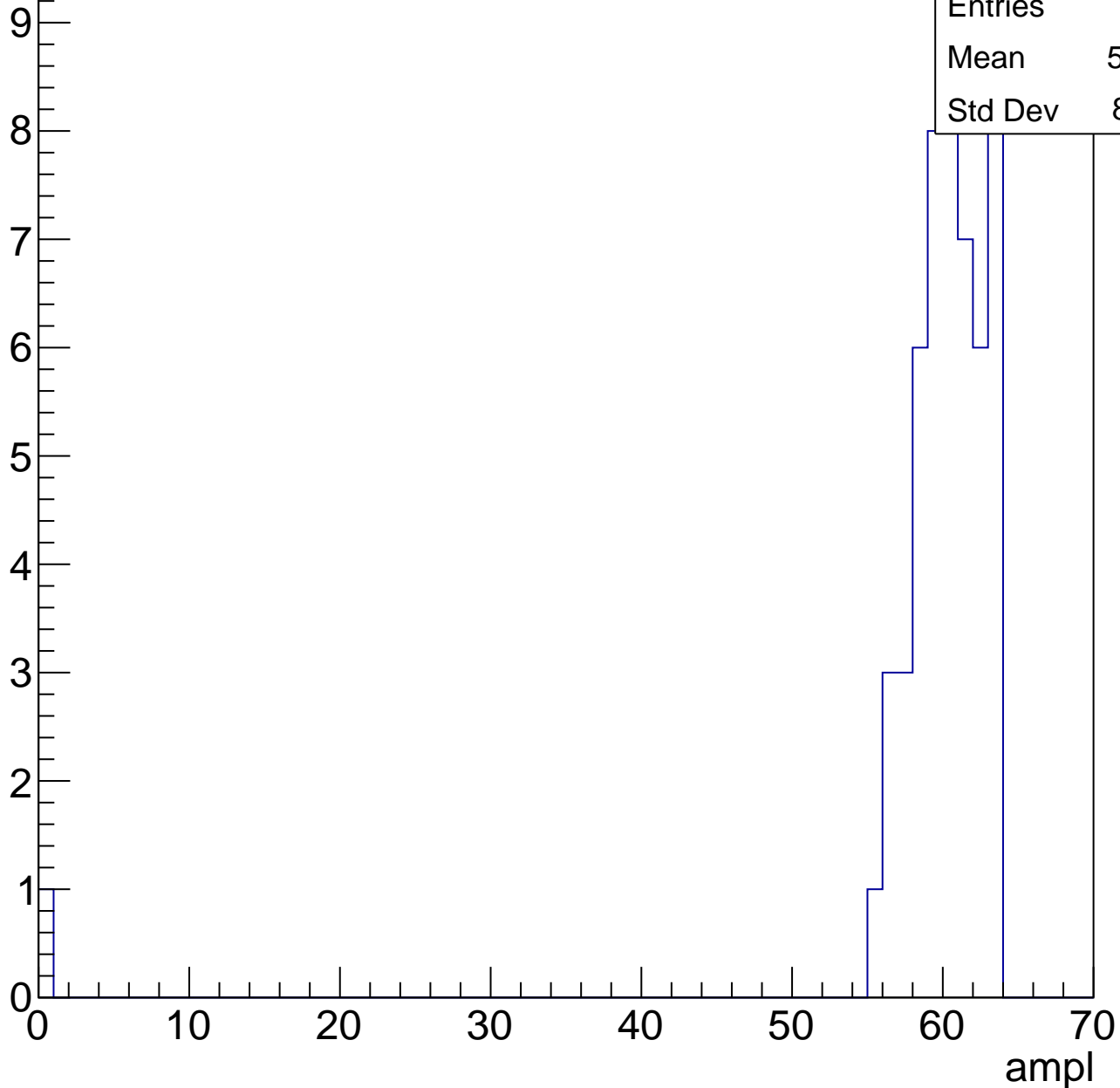
Entries	49
Mean	55.2
Std Dev	3.245



# B1L101S, U18-ch37, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch37, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	5
Mean	61.6
Std Dev	1.02



# B1L101S, U18-ch37, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U18-ch38, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	74
Mean	30.12
Std Dev	6.043

**Gaus mean : 31.8594**

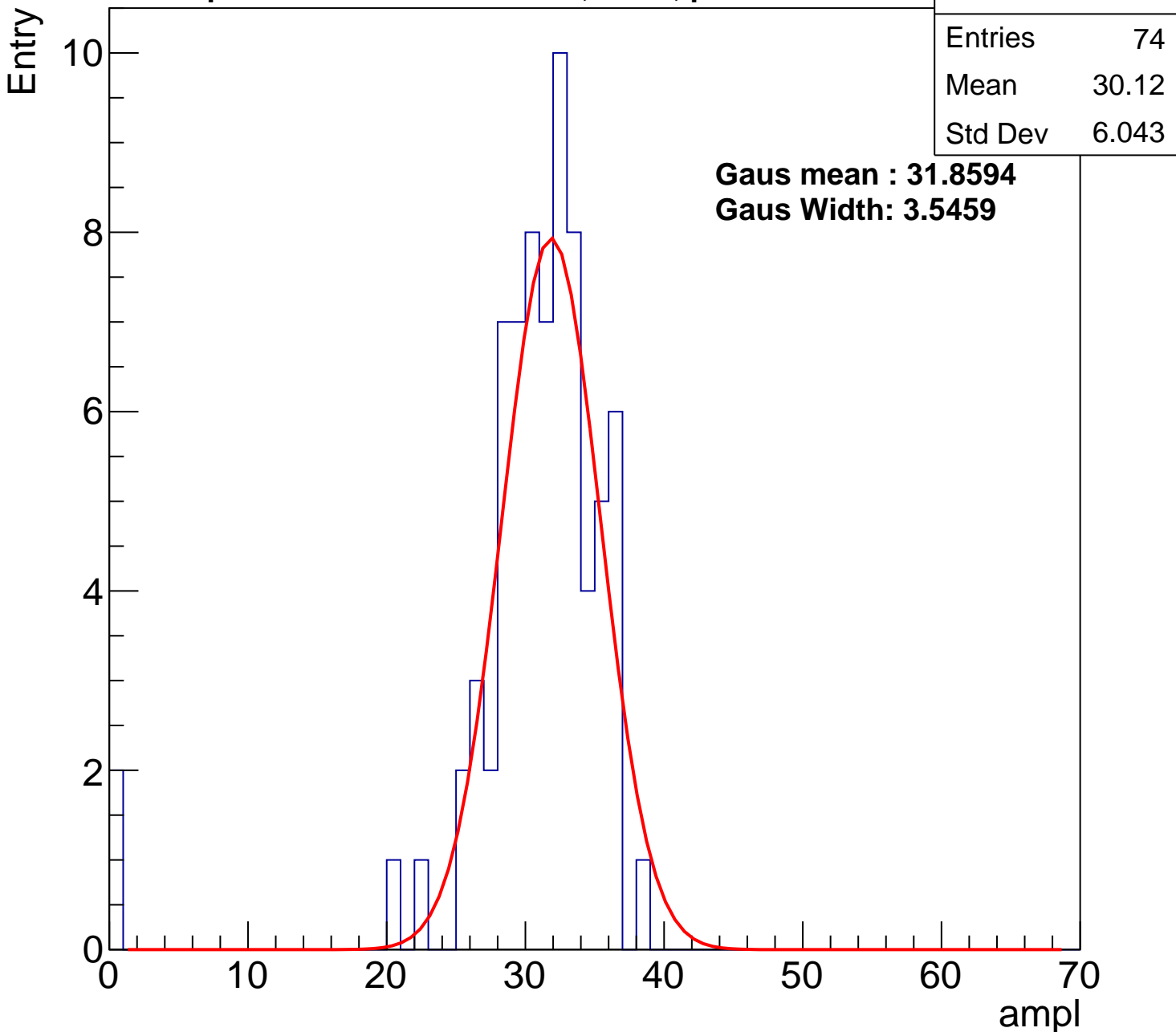
**Gaus Width: 3.5459**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U18-ch38, adc1

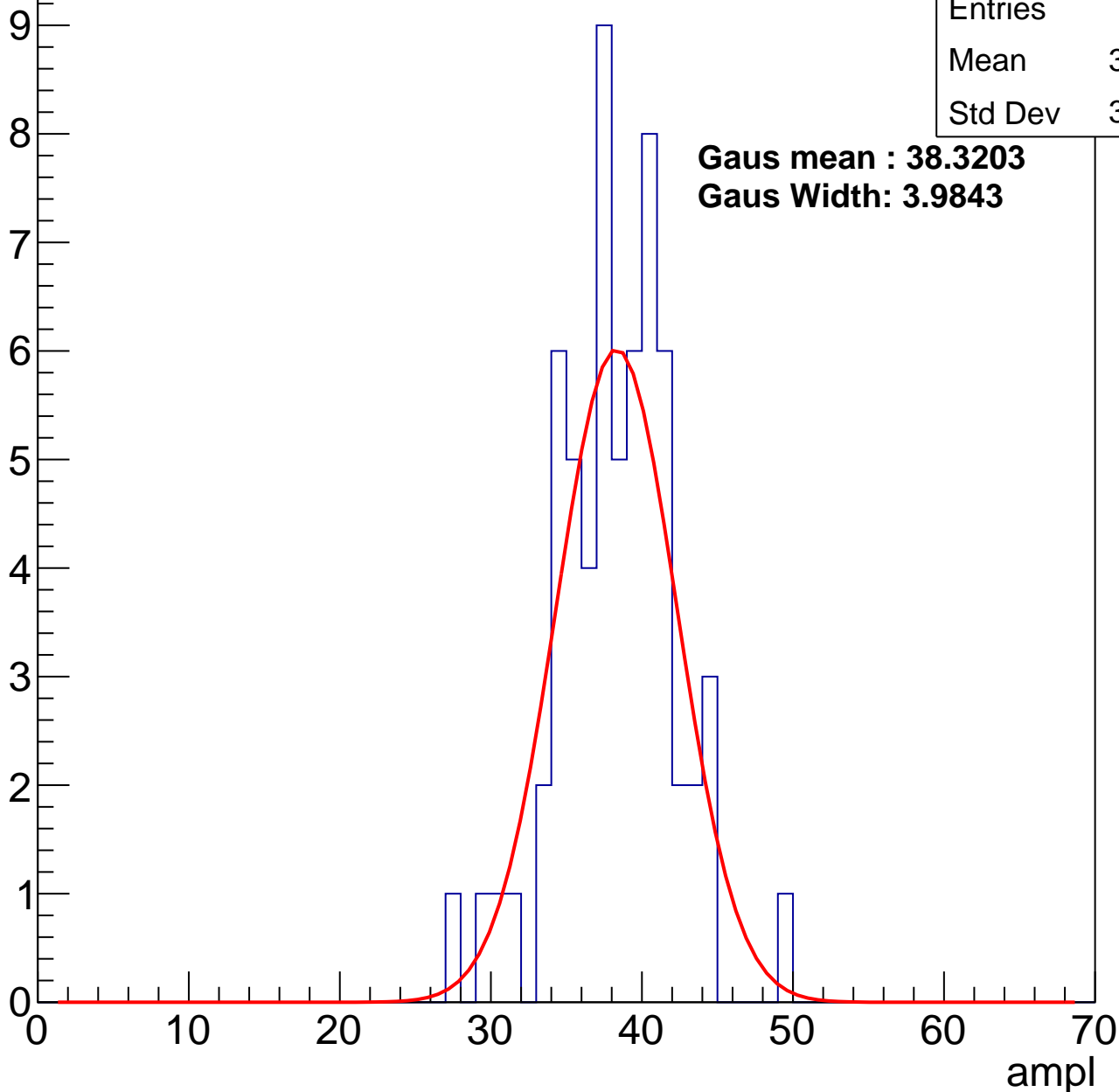
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	37.78
Std Dev	3.844

**Gaus mean : 38.3203**

**Gaus Width: 3.9843**



# B1L101S, U18-ch38, adc2

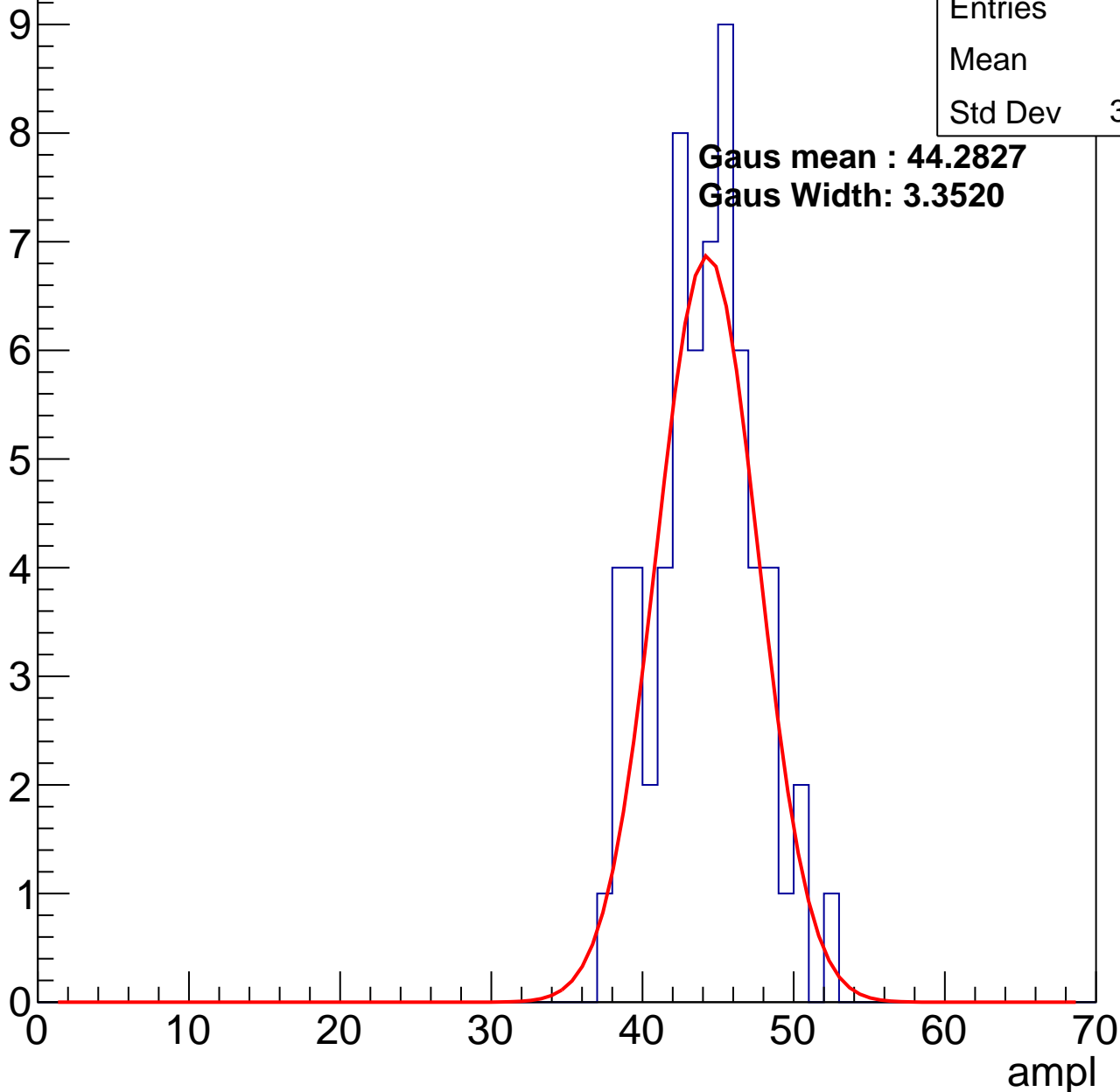
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	43.7
Std Dev	3.303

**Gaus mean : 44.2827**

**Gaus Width: 3.3520**

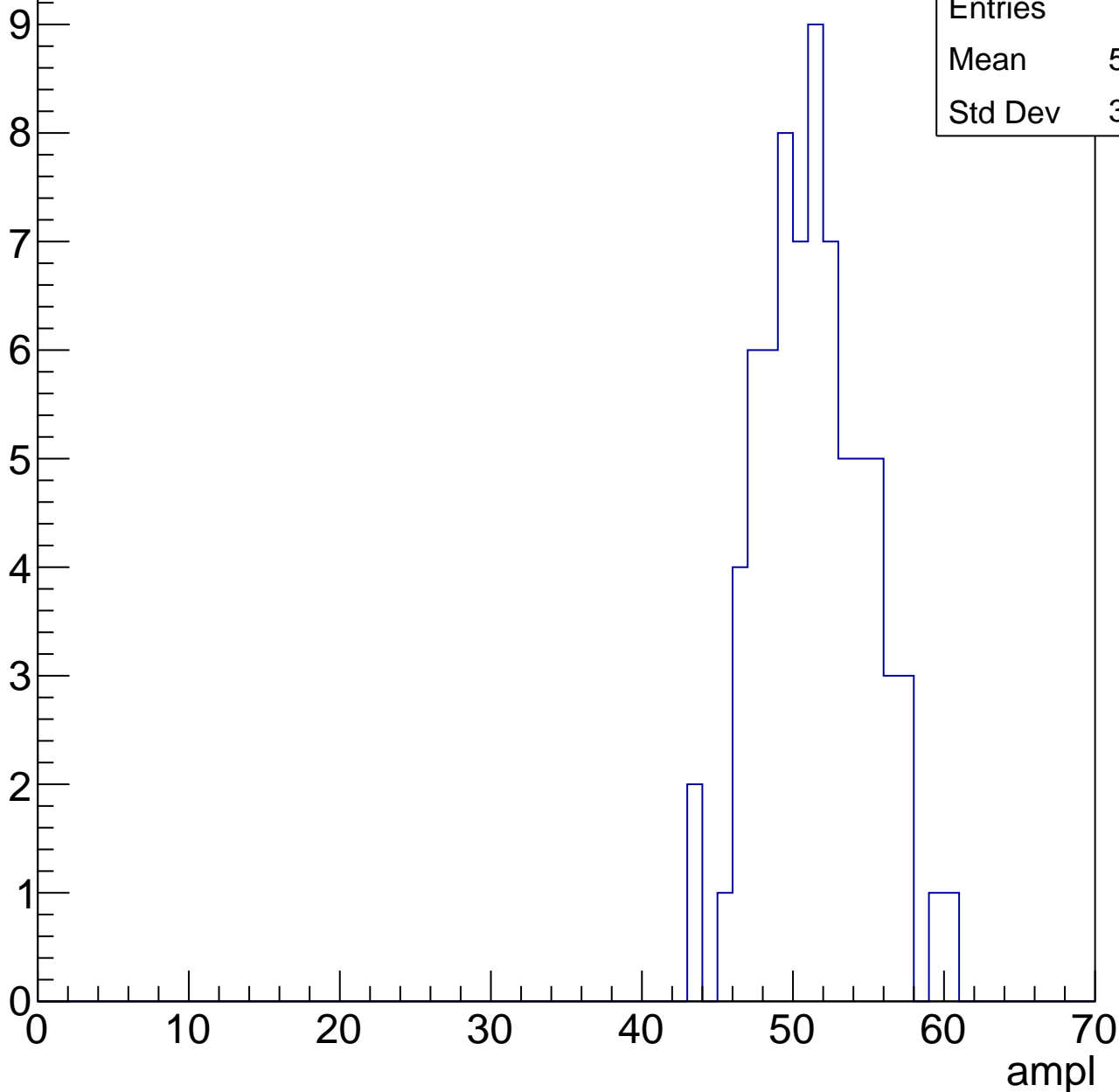


# B1L101S, U18-ch38, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

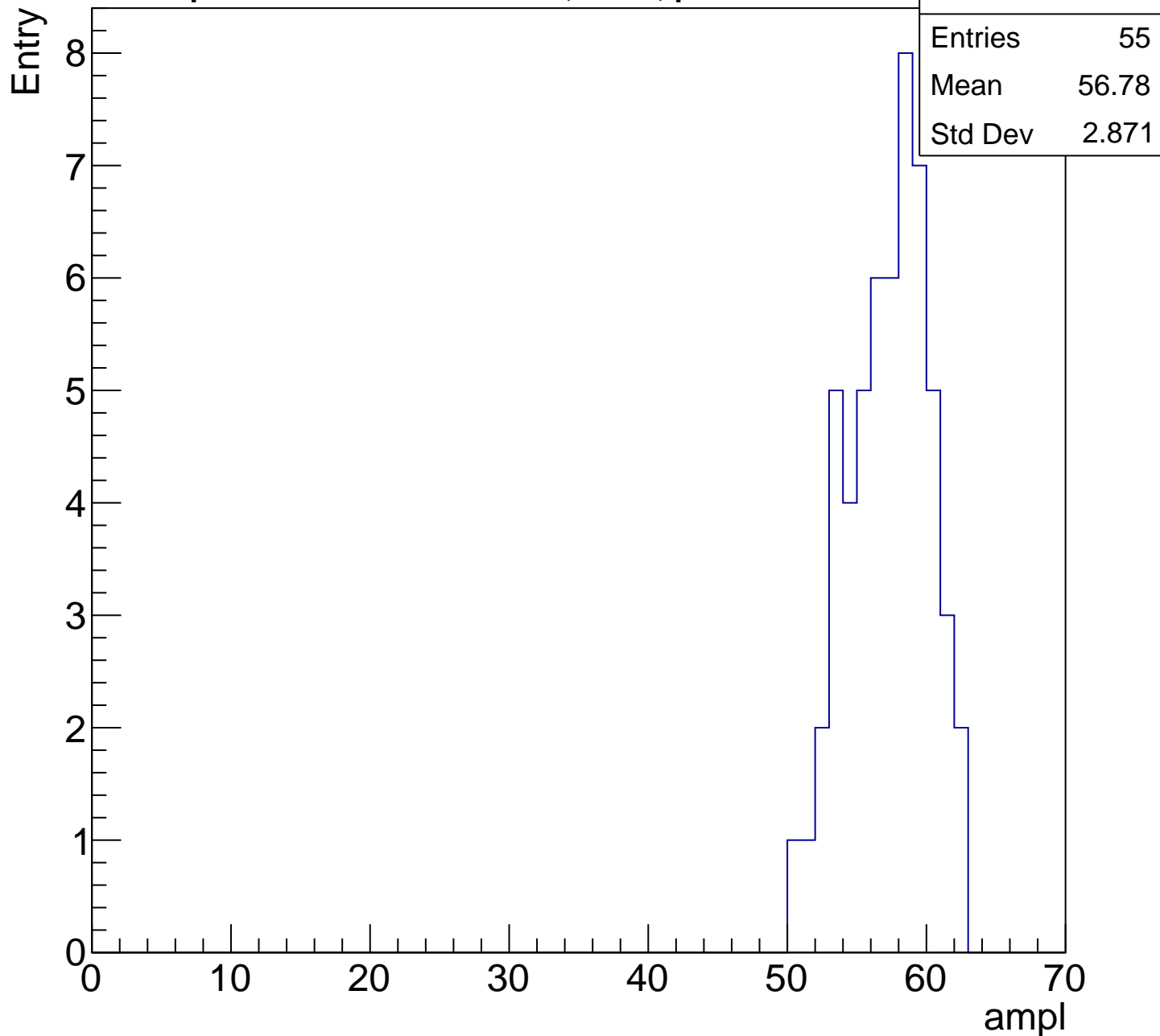
Entry

Entries	73
Mean	50.93
Std Dev	3.574



# B1L101S, U18-ch38, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

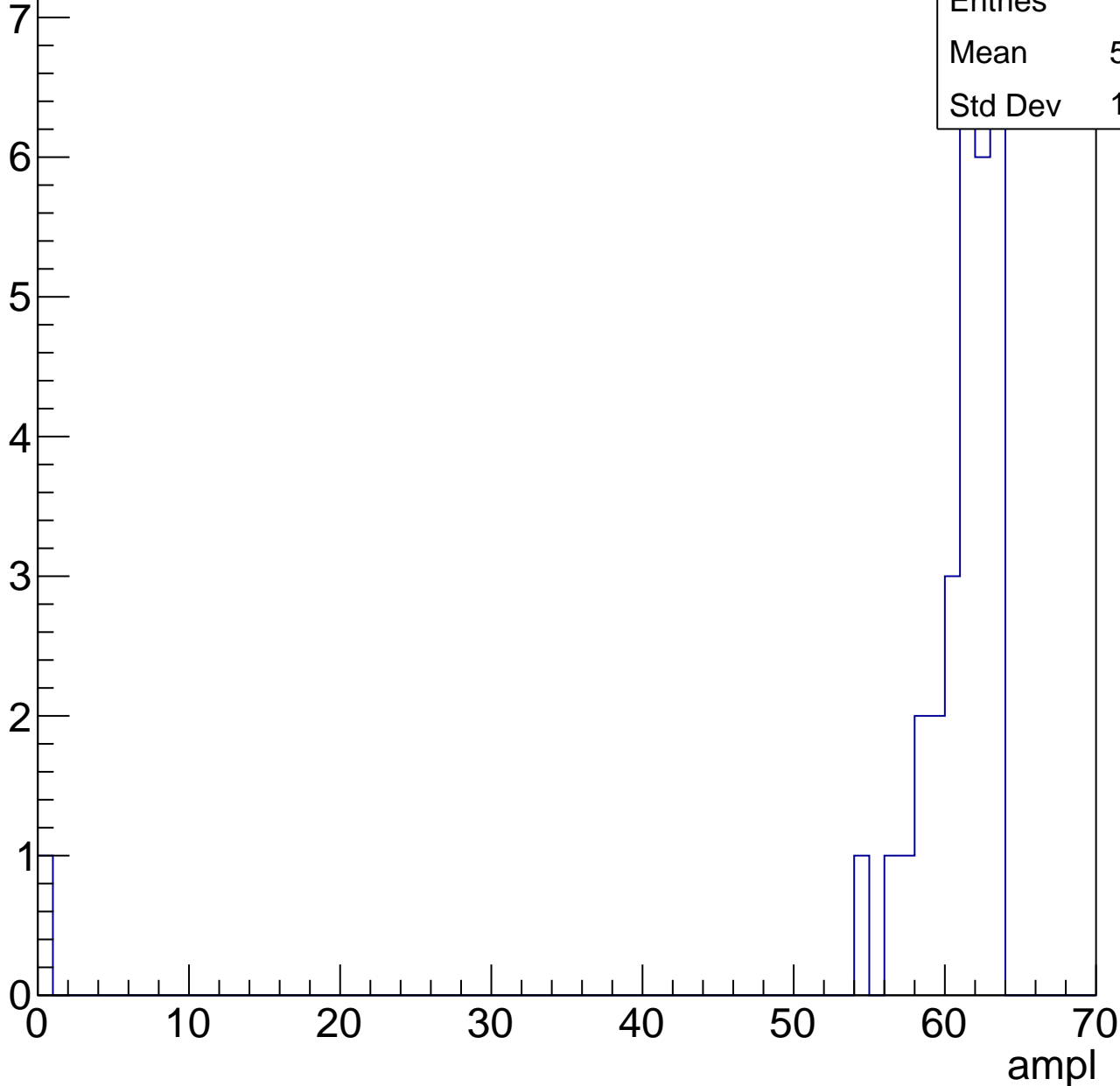


# B1L101S, U18-ch38, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

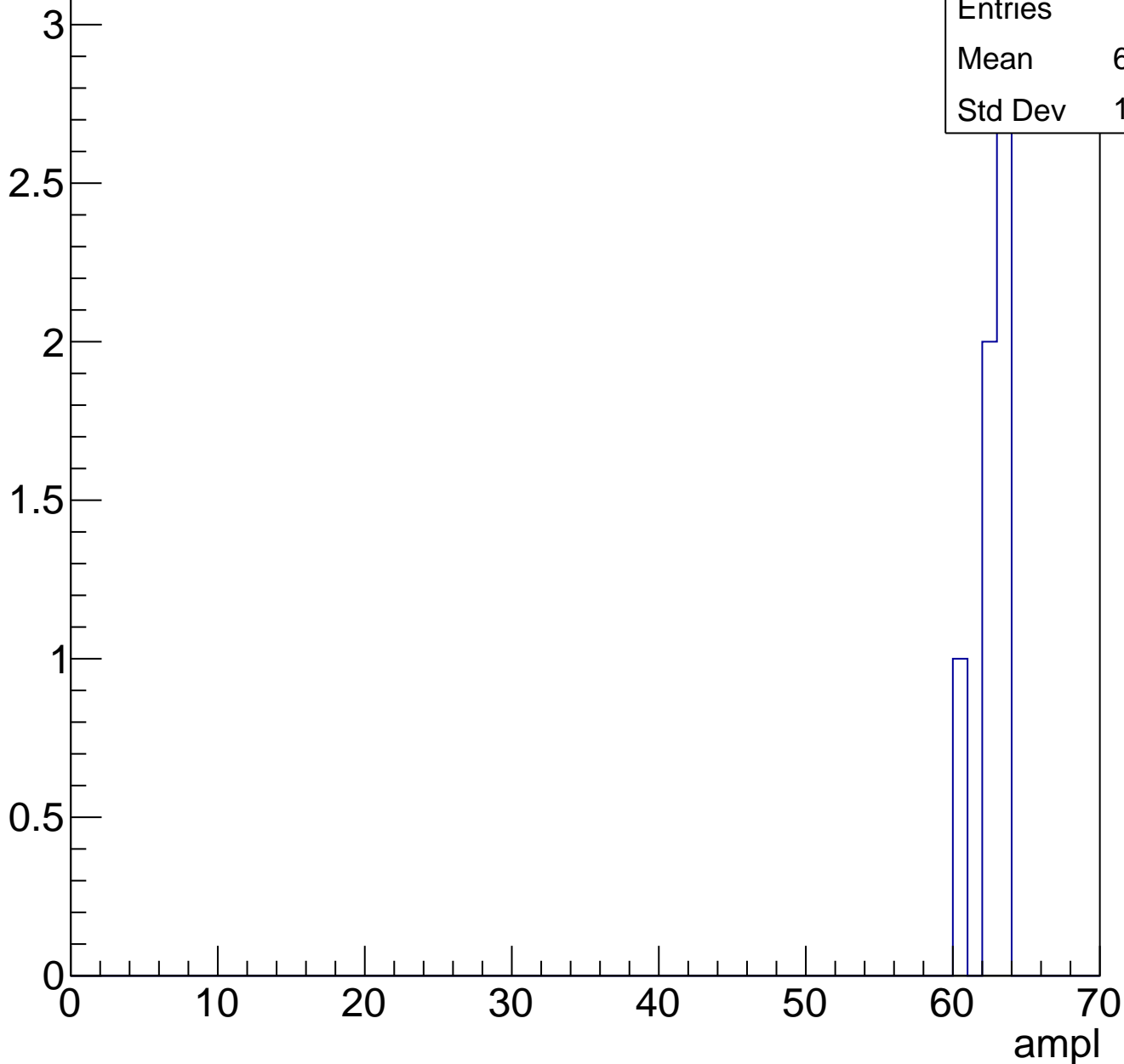
Entries	31
Mean	58.74
Std Dev	10.95



# B1L101S, U18-ch38, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch38, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U18-ch39, adc0

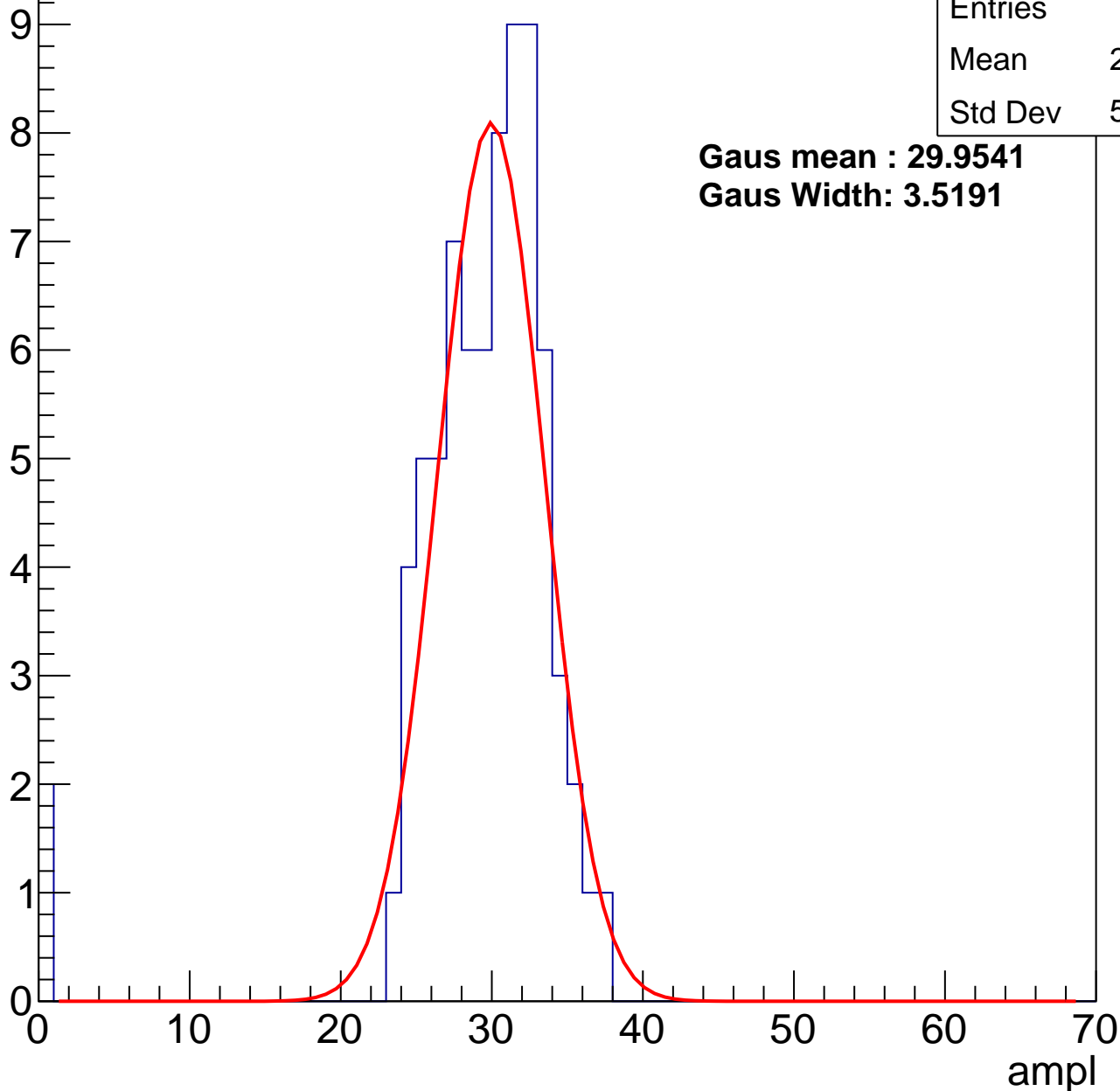
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	28.73
Std Dev	5.719

**Gaus mean : 29.9541**

**Gaus Width: 3.5191**



# B1L101S, U18-ch39, adc1

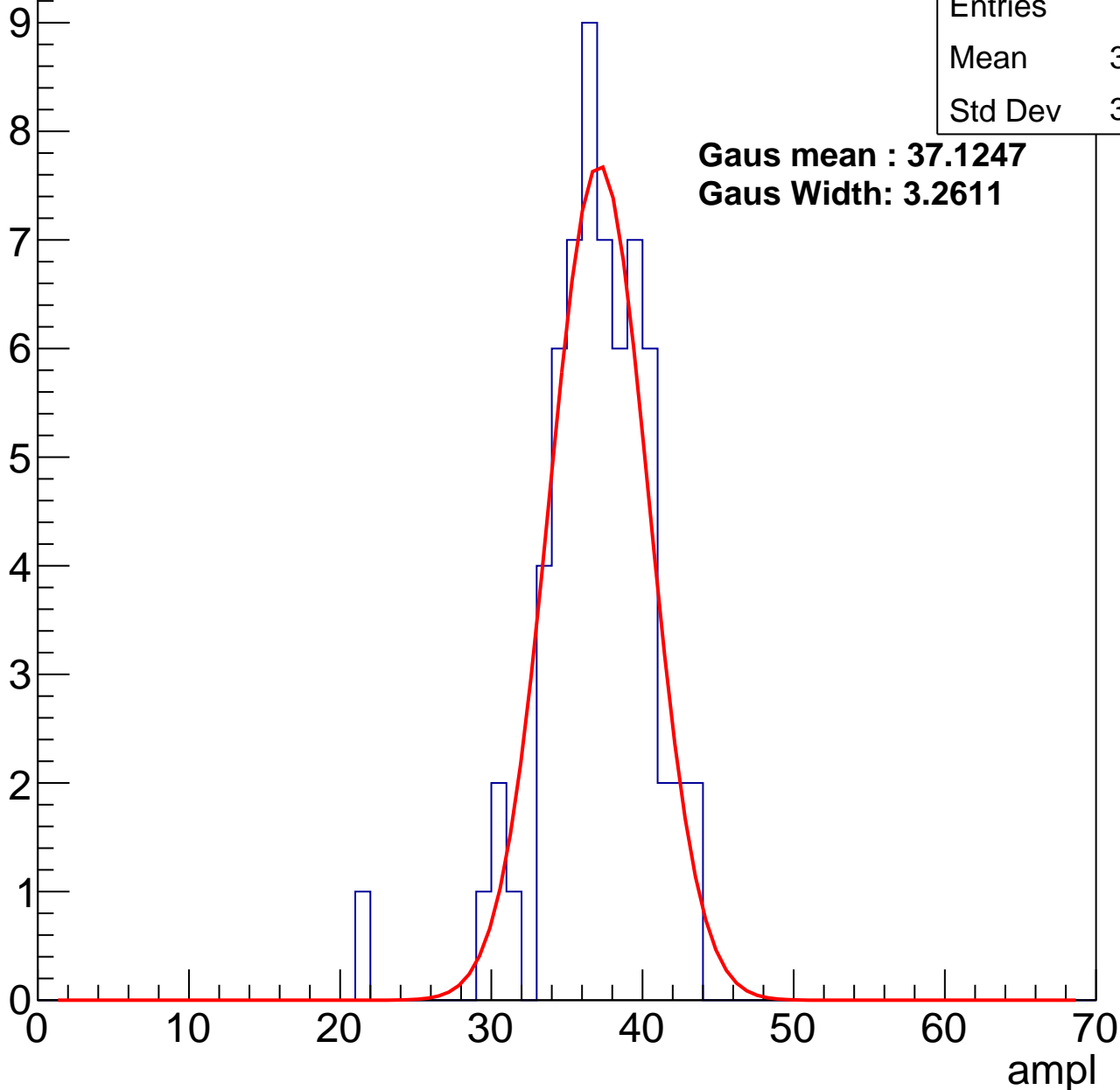
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	36.48
Std Dev	3.638

**Gaus mean : 37.1247**

**Gaus Width: 3.2611**



# B1L101S, U18-ch39, adc2

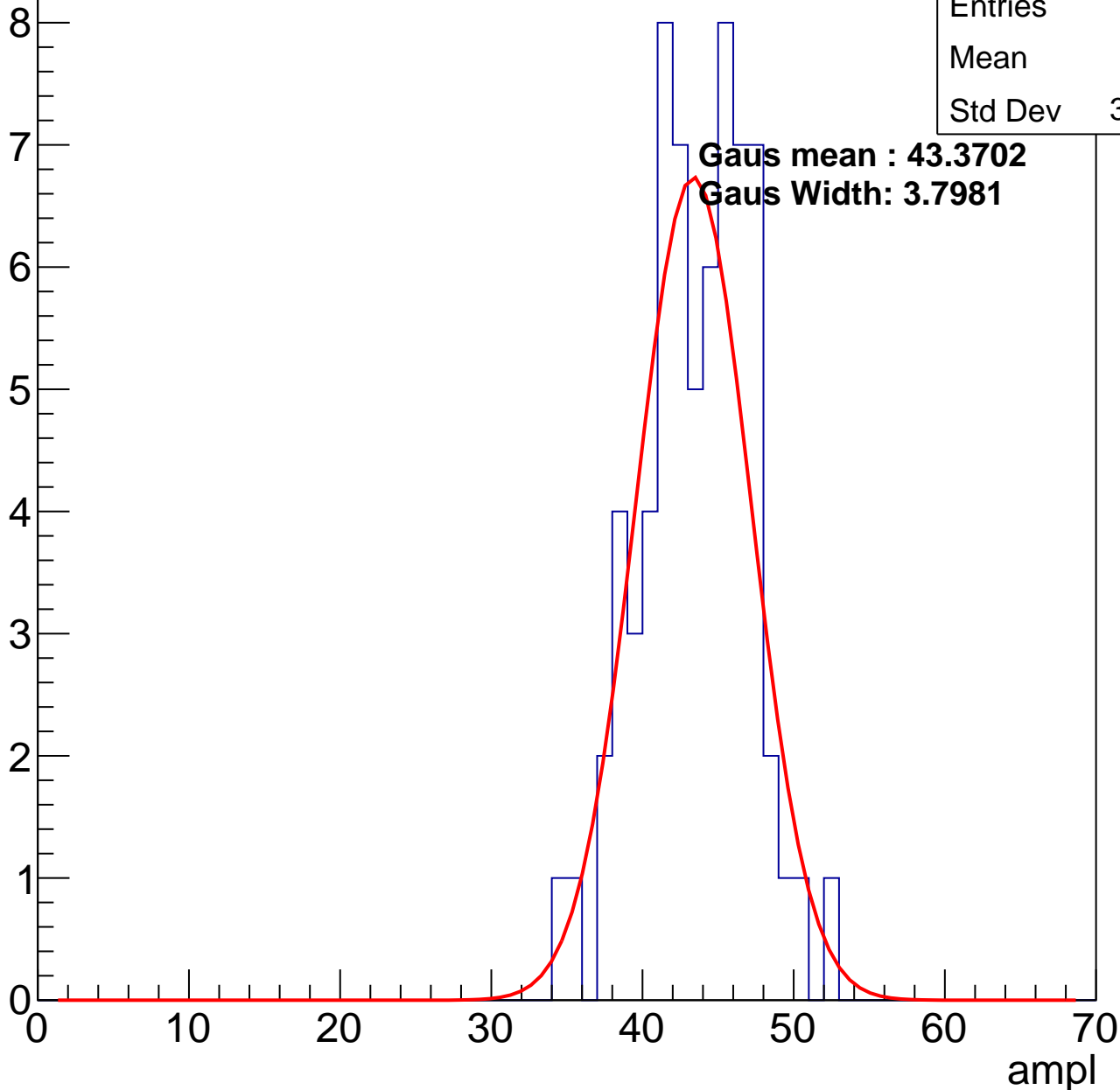
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	43.1
Std Dev	3.573

**Gaus mean : 43.3702**

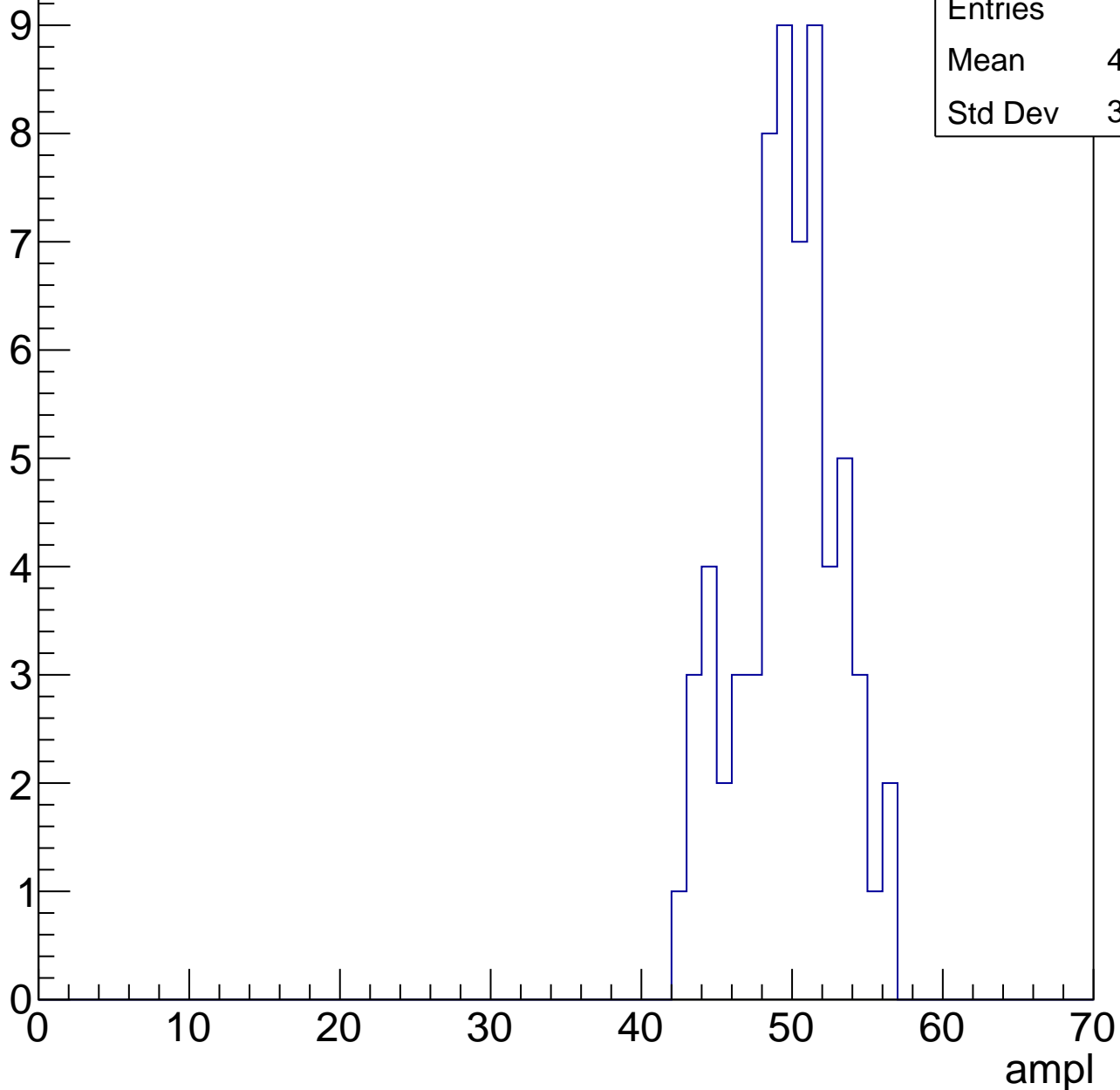
**Gaus Width: 3.7981**



# B1L101S, U18-ch39, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

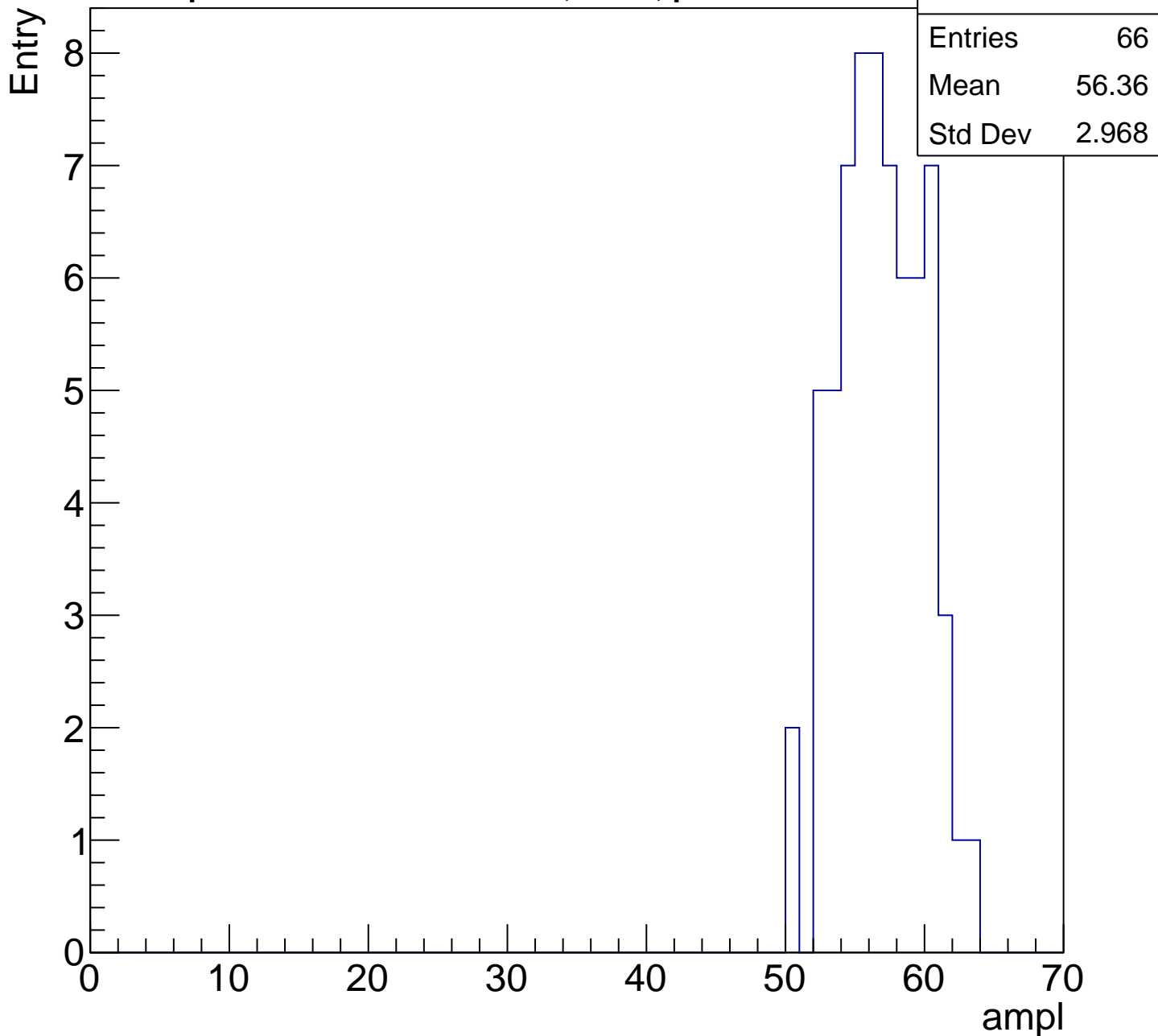
Entry



Entries	64
Mean	49.25
Std Dev	3.307

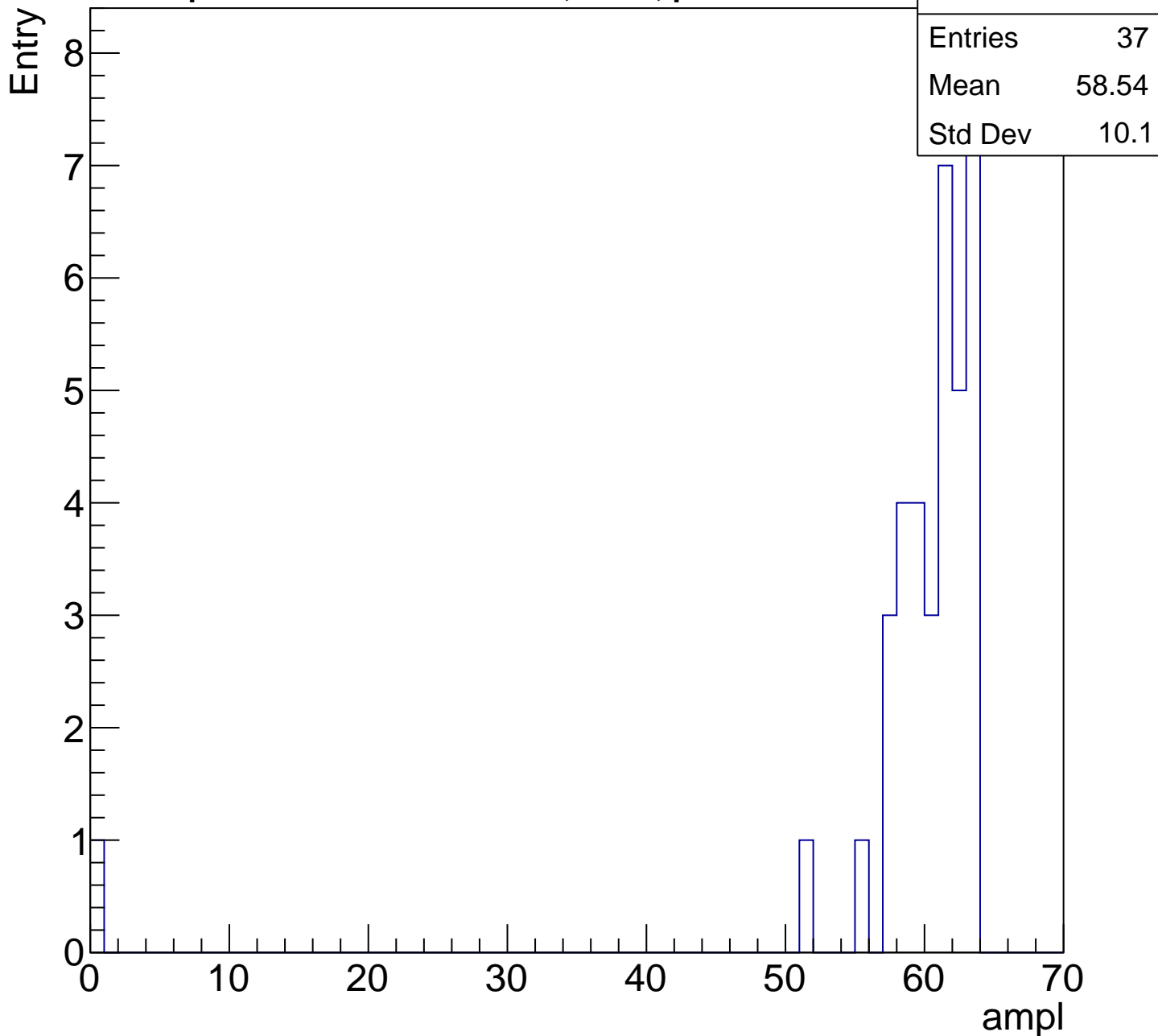
# B1L101S, U18-ch39, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U18-ch39, adc5

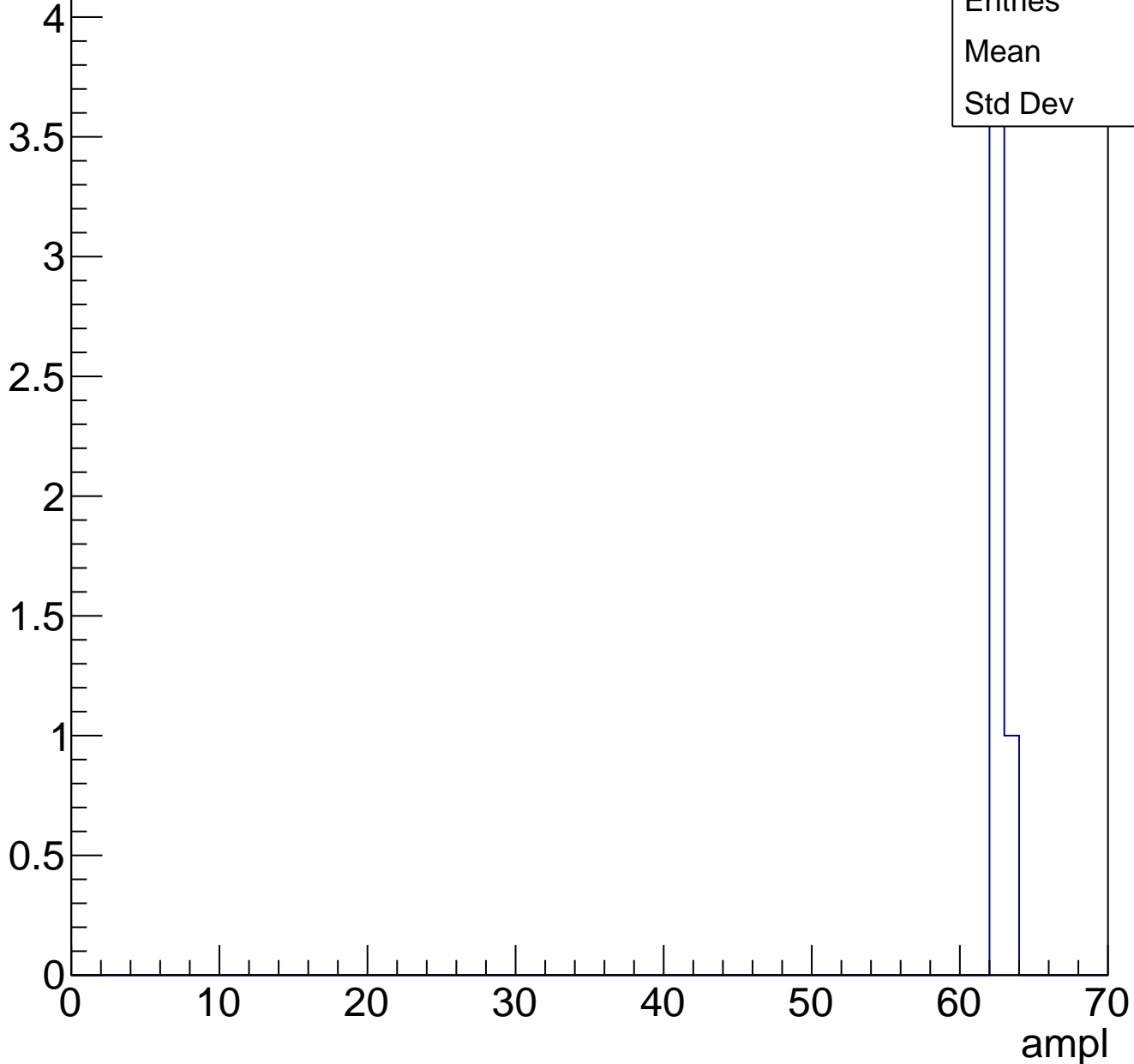
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U18-ch39, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch39, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U18-ch40, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	79
Mean	28.68
Std Dev	4.163

**Gaus mean : 29.3967**

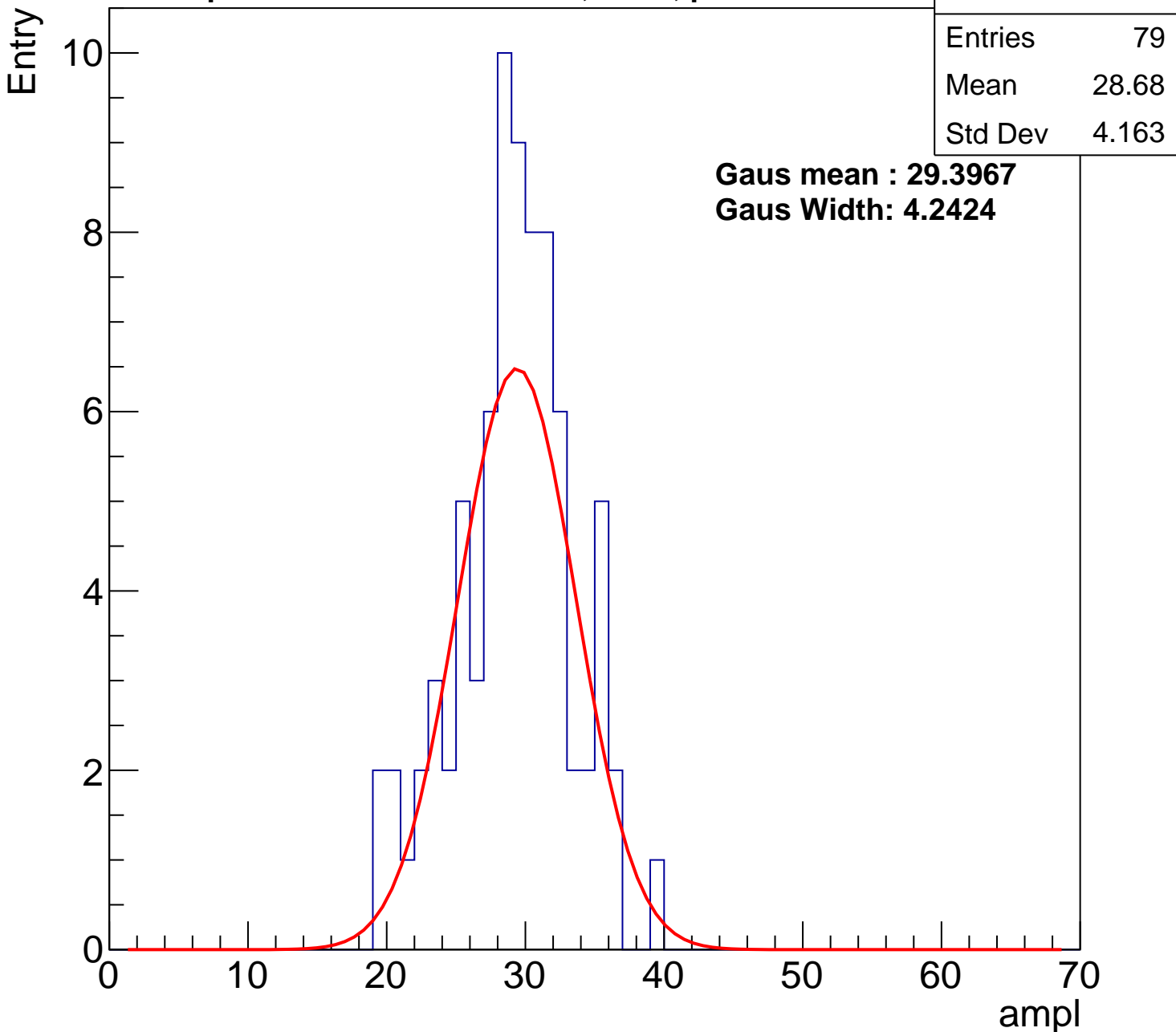
**Gaus Width: 4.2424**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U18-ch40, adc1

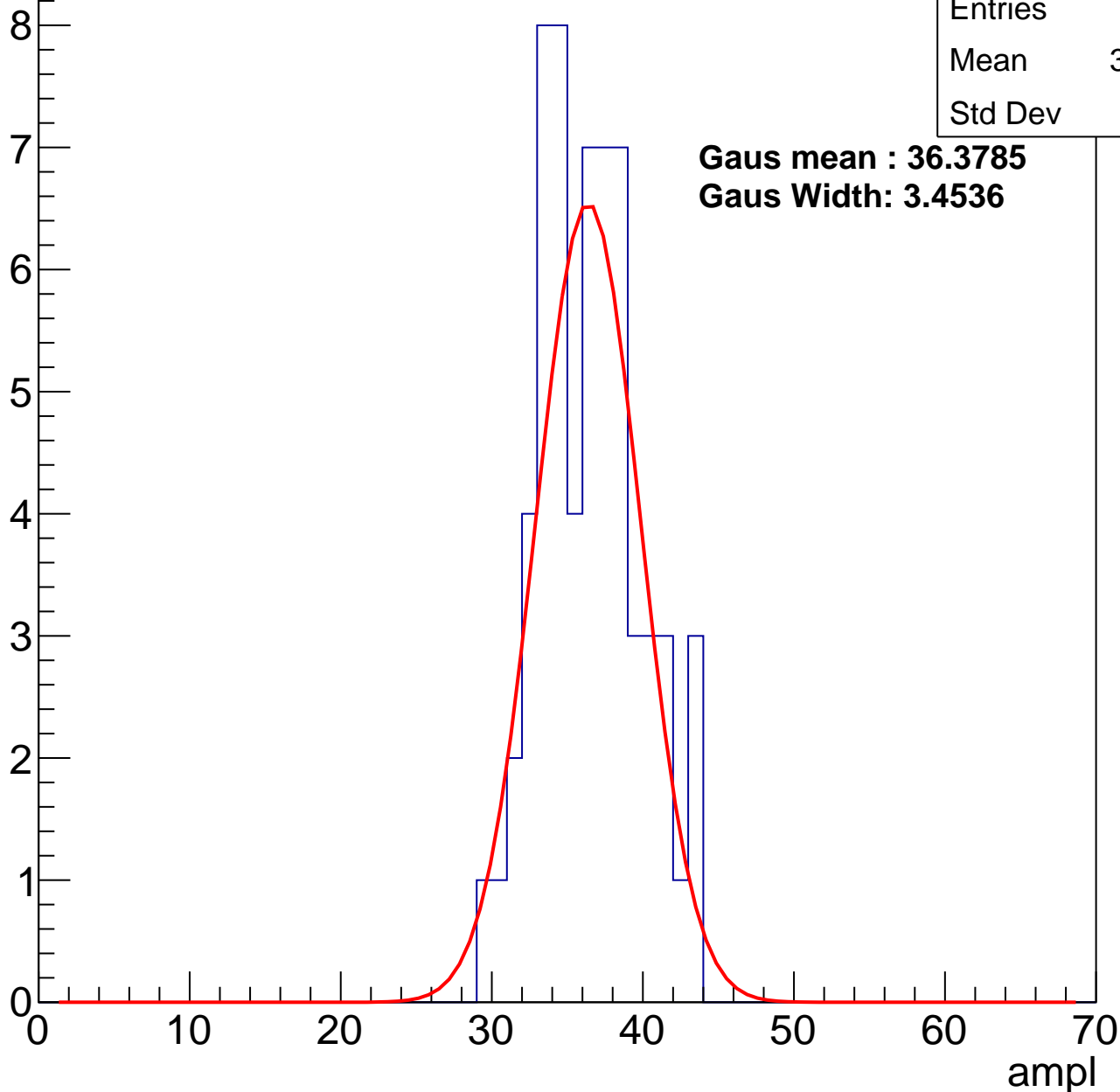
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	36.02
Std Dev	3.3

**Gaus mean : 36.3785**

**Gaus Width: 3.4536**



# B1L101S, U18-ch40, adc2

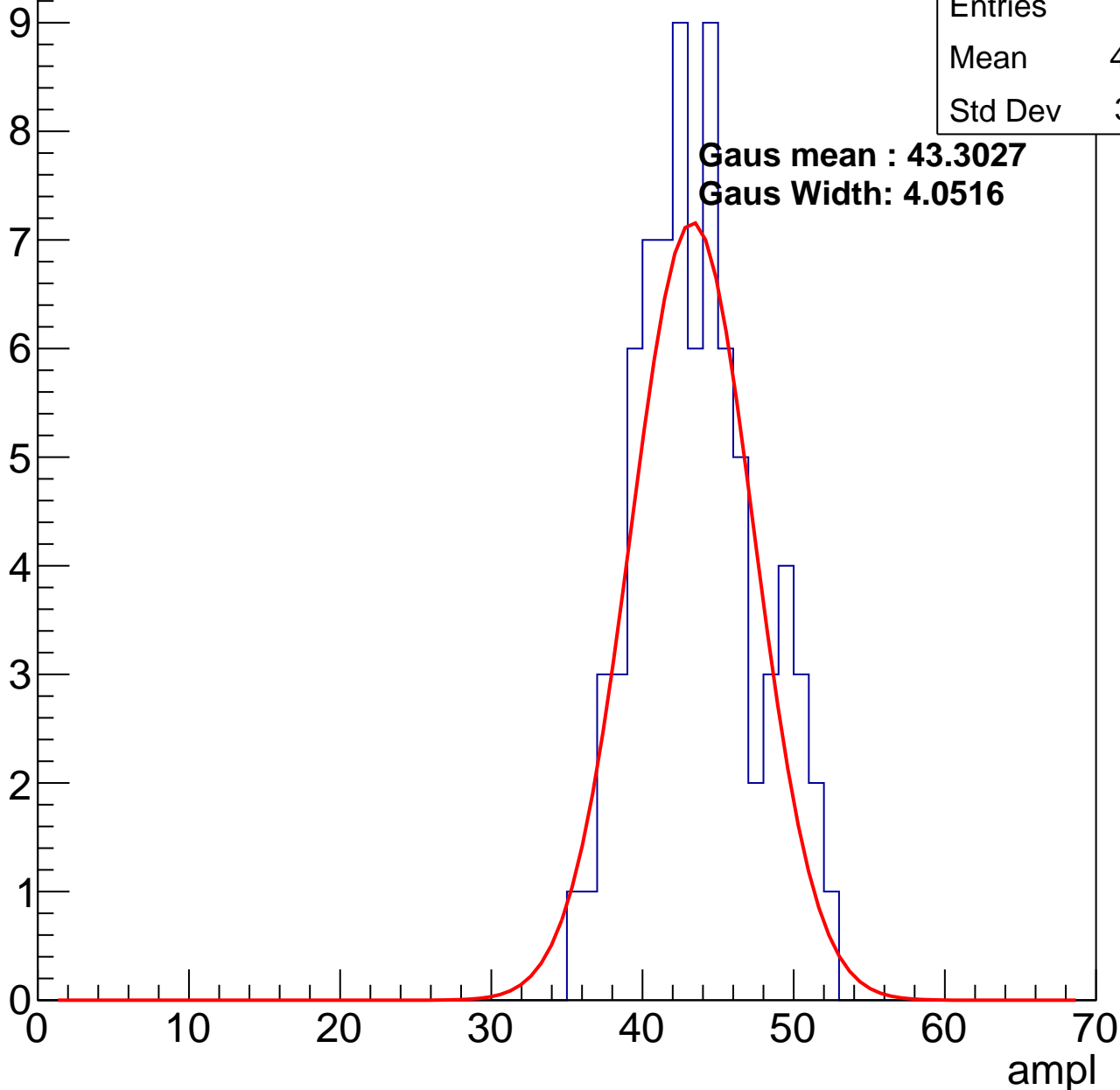
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	78
Mean	43.17
Std Dev	3.881

**Gaus mean : 43.3027**

**Gaus Width: 4.0516**

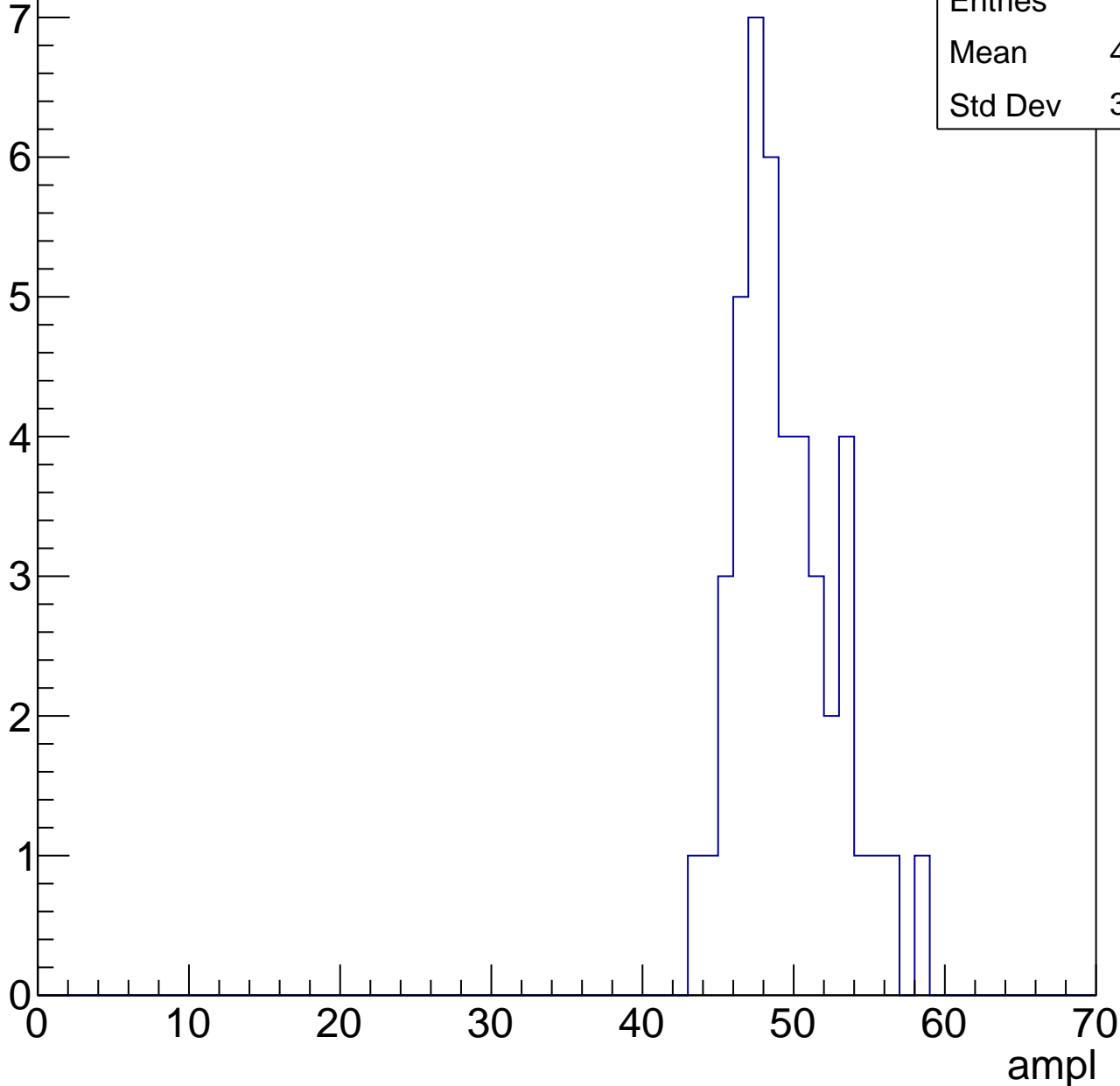


# B1L101S, U18-ch40, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	44
Mean	49.02
Std Dev	3.292

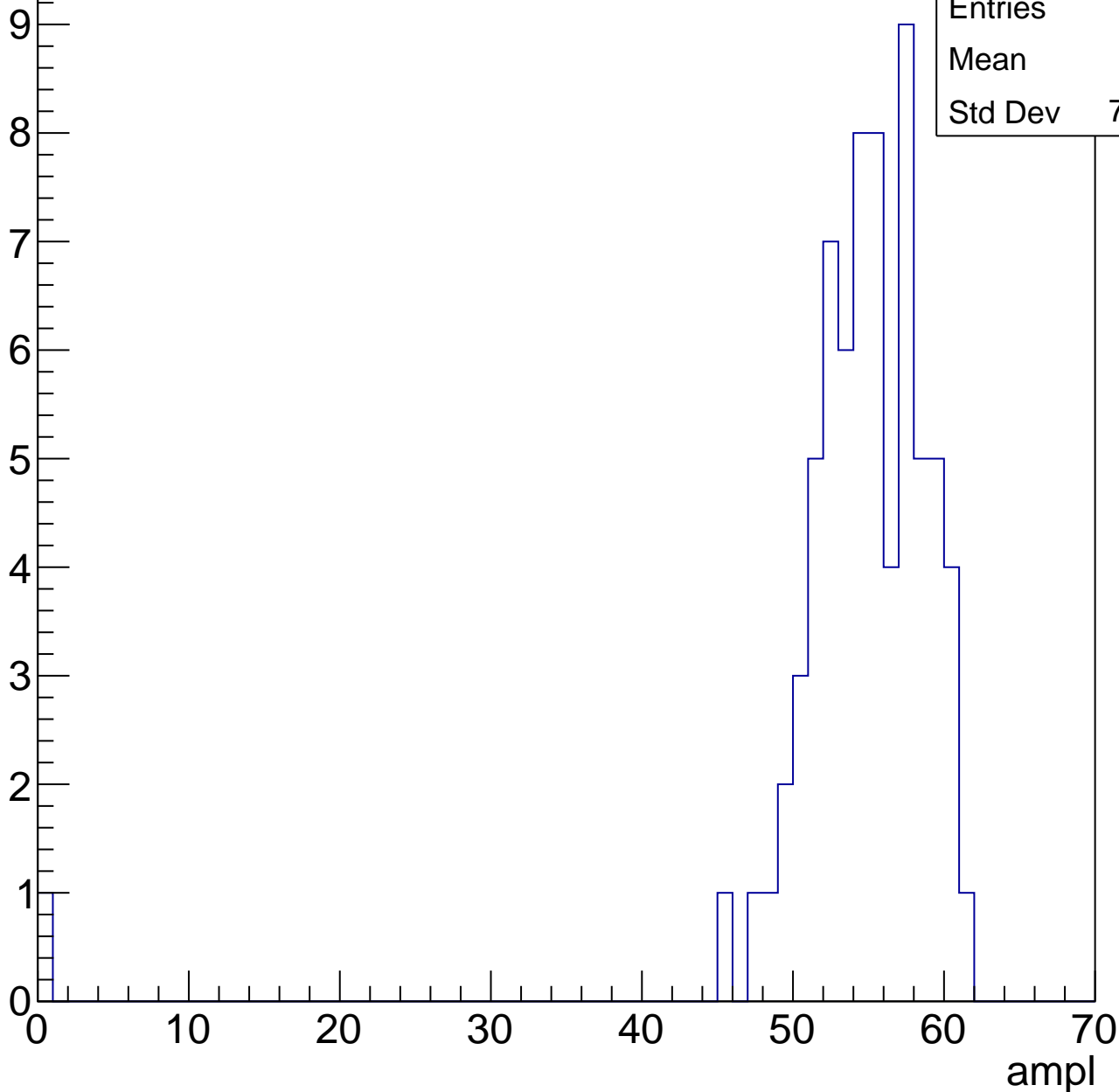


# B1L101S, U18-ch40, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	53.8
Std Dev	7.276

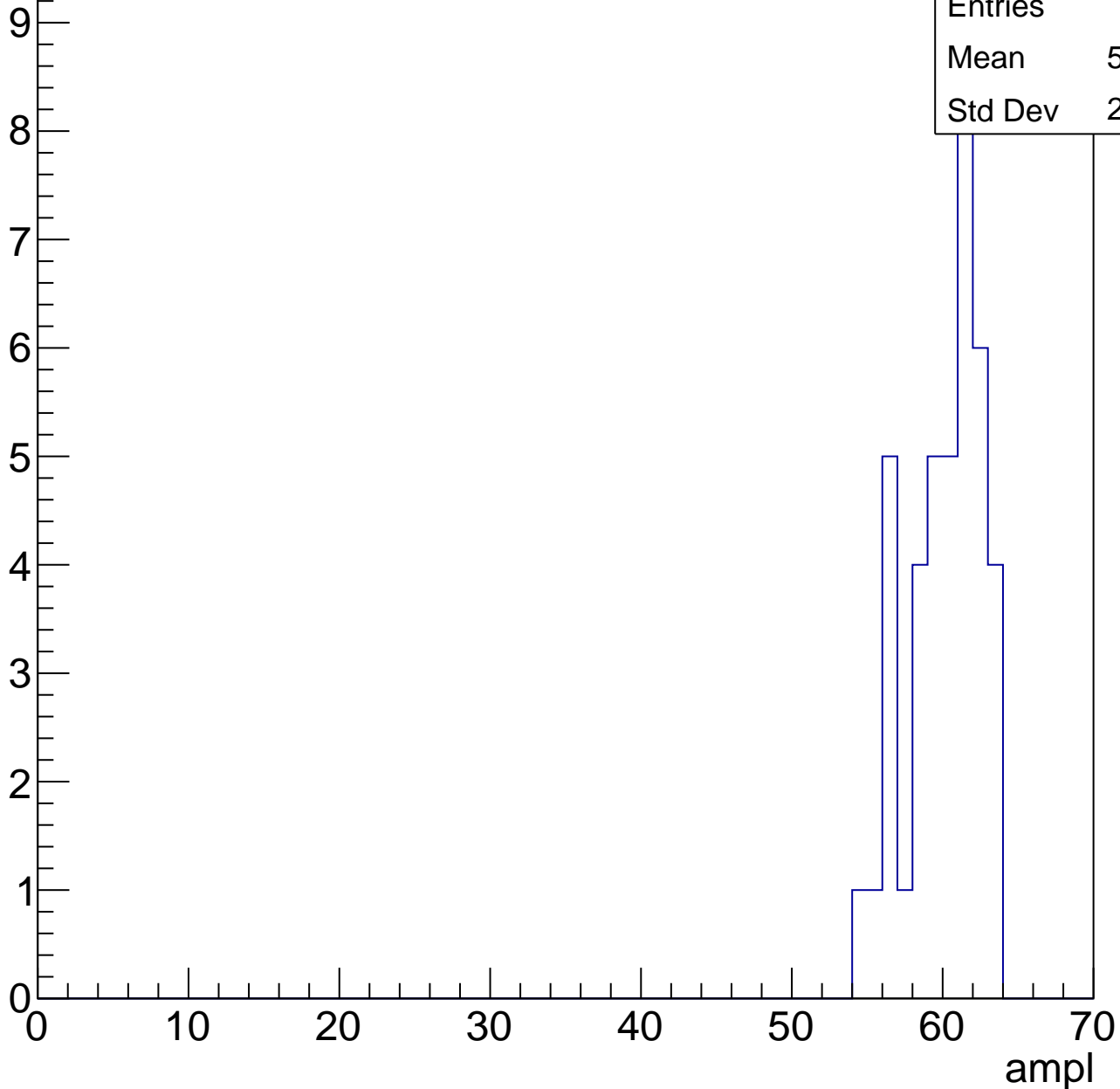


# B1L101S, U18-ch40, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	41
Mean	59.66
Std Dev	2.395

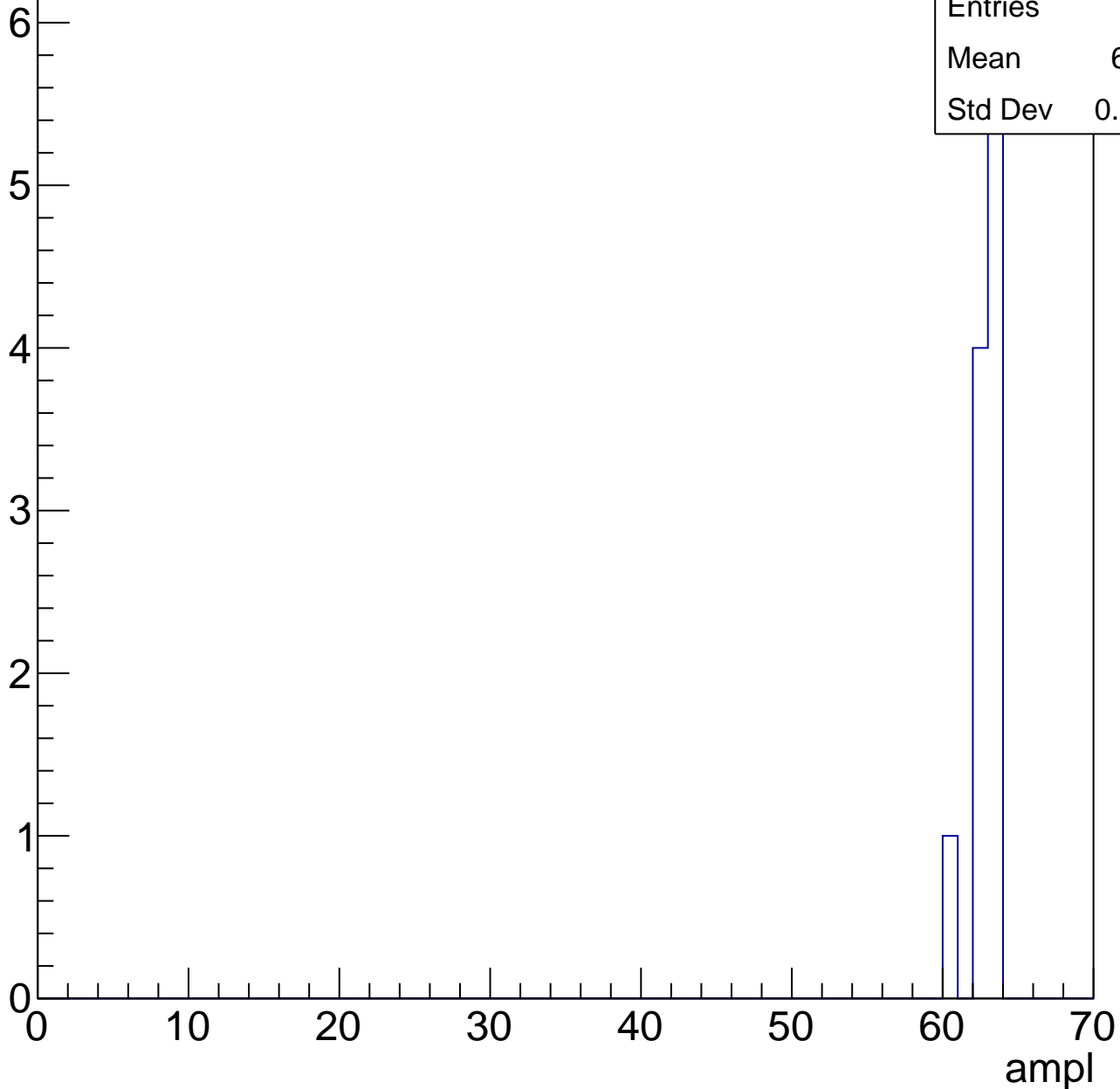


# B1L101S, U18-ch40, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	11
Mean	62.36
Std Dev	0.8814





# B1L101S, U18-ch40, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U18-ch41, adc0

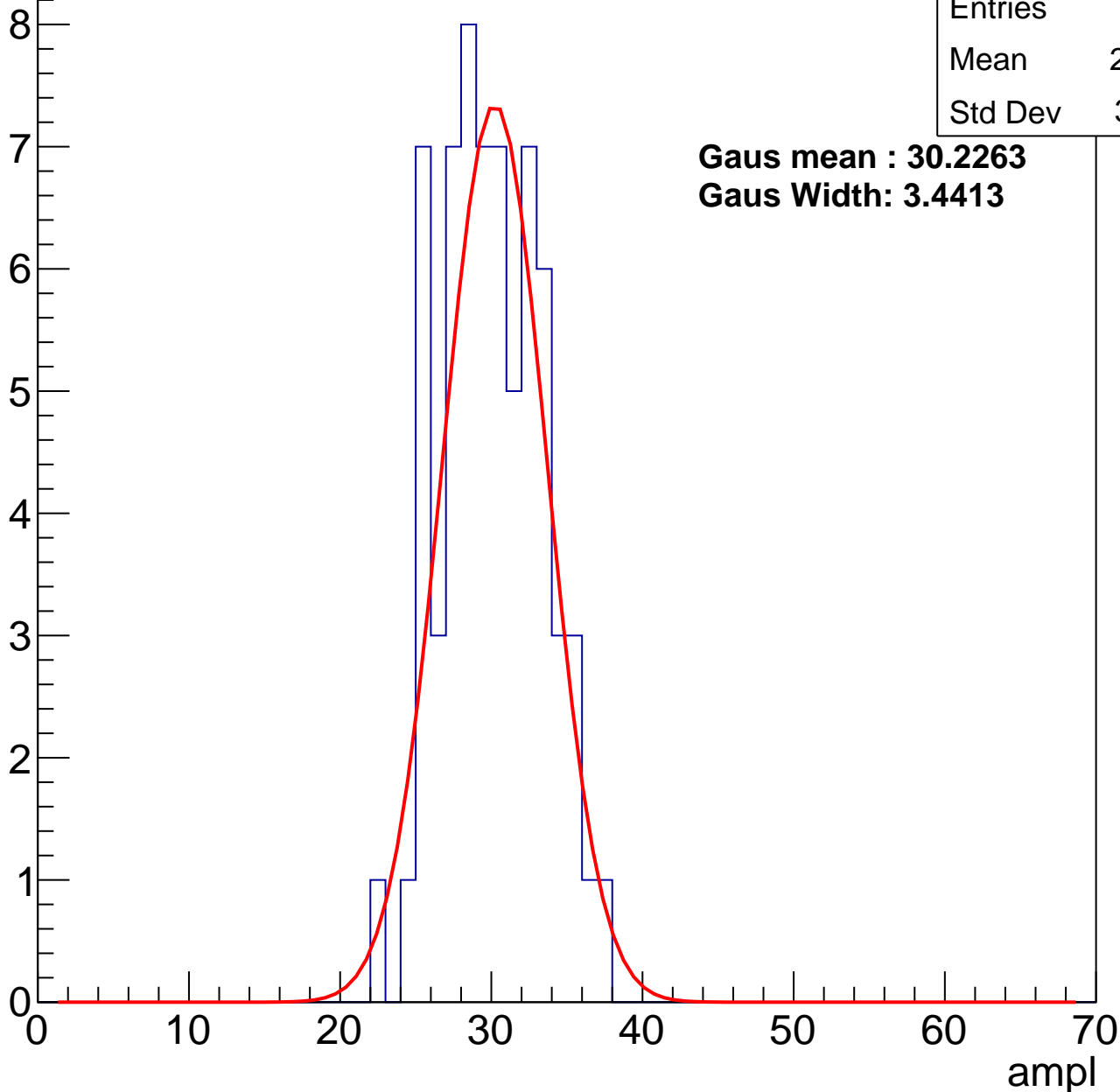
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	29.58
Std Dev	3.251

**Gaus mean : 30.2263**

**Gaus Width: 3.4413**



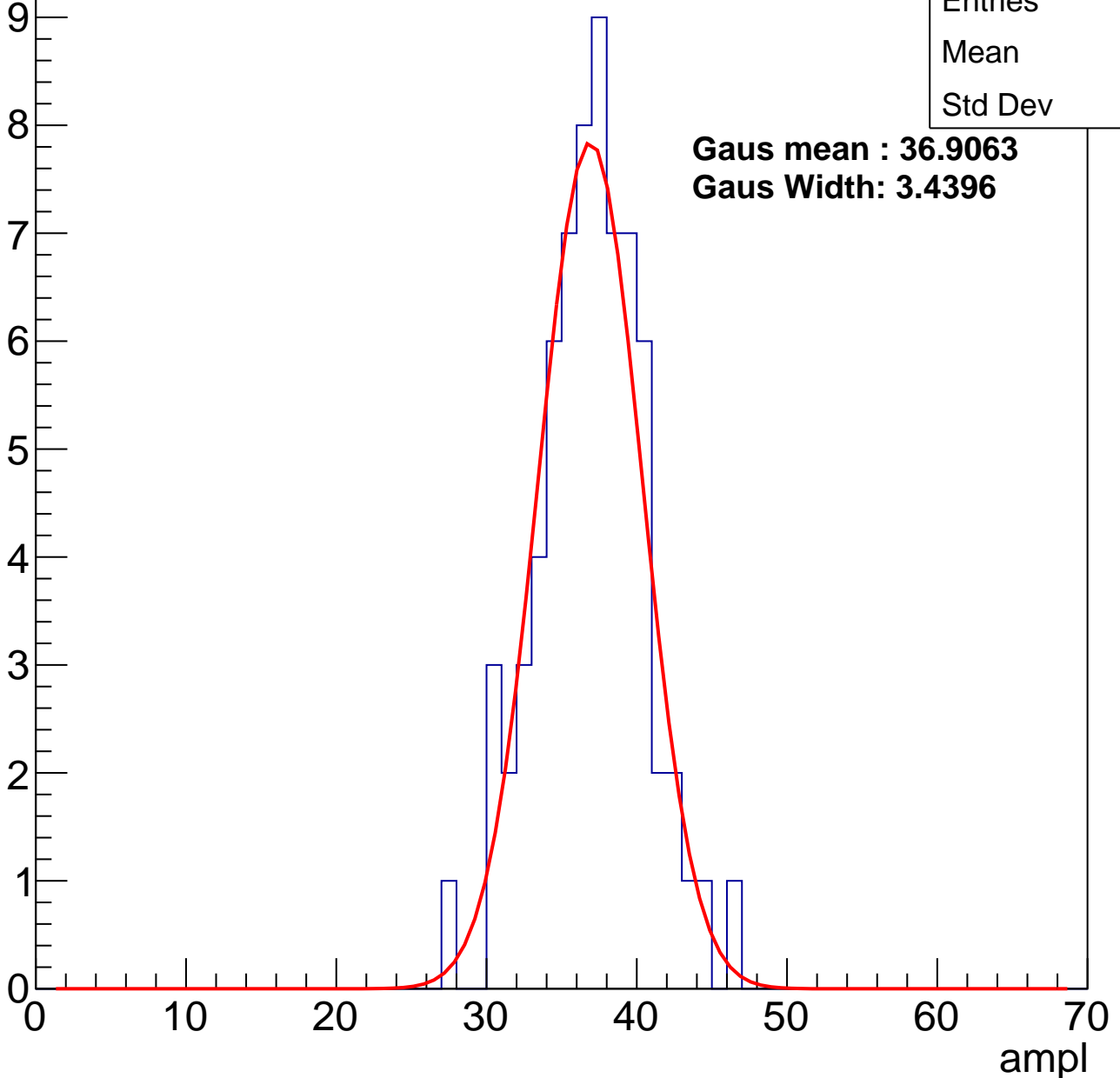
# B1L101S, U18-ch41, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	36.5
Std Dev	3.52

**Gaus mean : 36.9063**  
**Gaus Width: 3.4396**



# B1L101S, U18-ch41, adc2

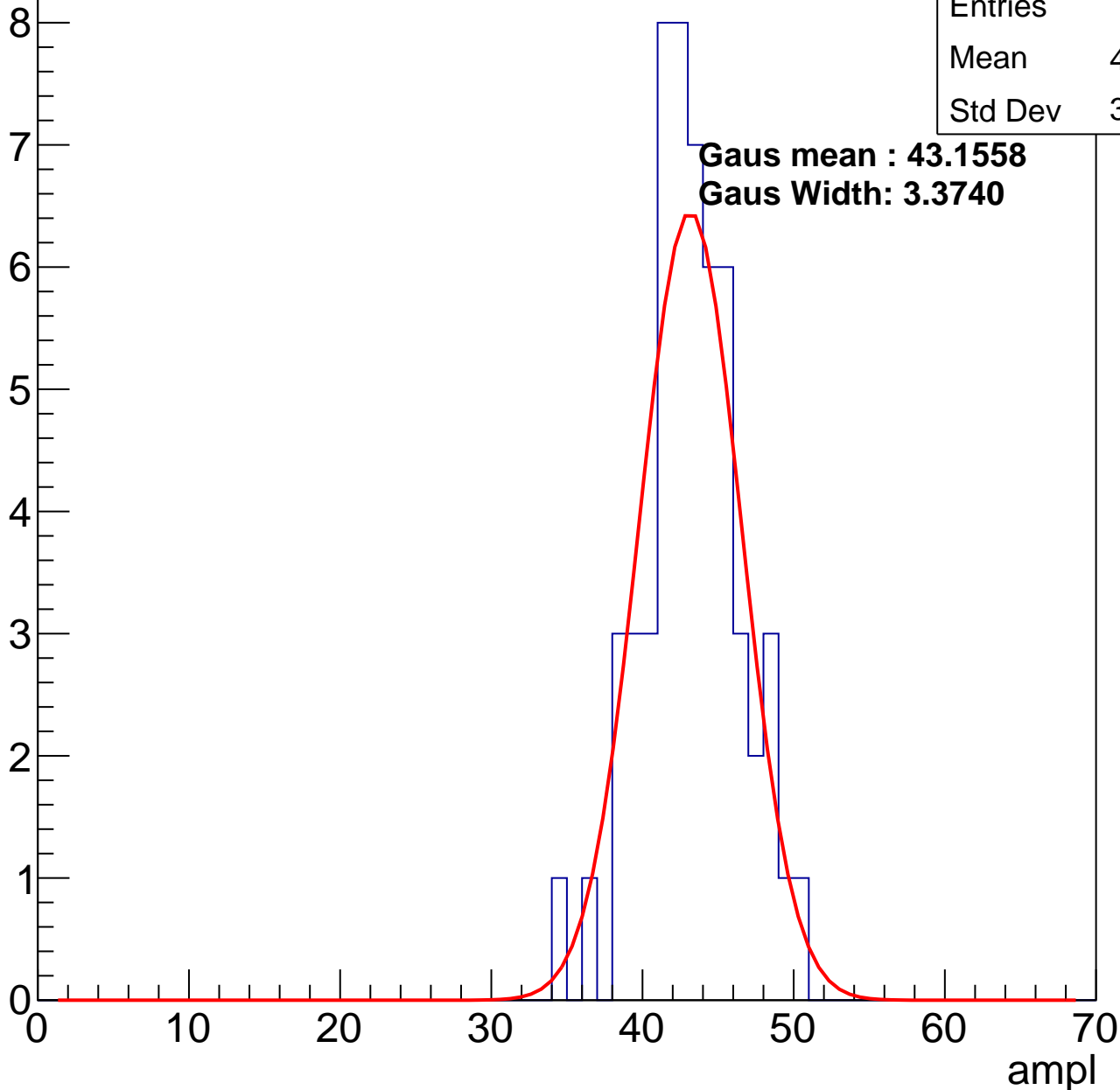
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	42.77
Std Dev	3.179

**Gaus mean : 43.1558**

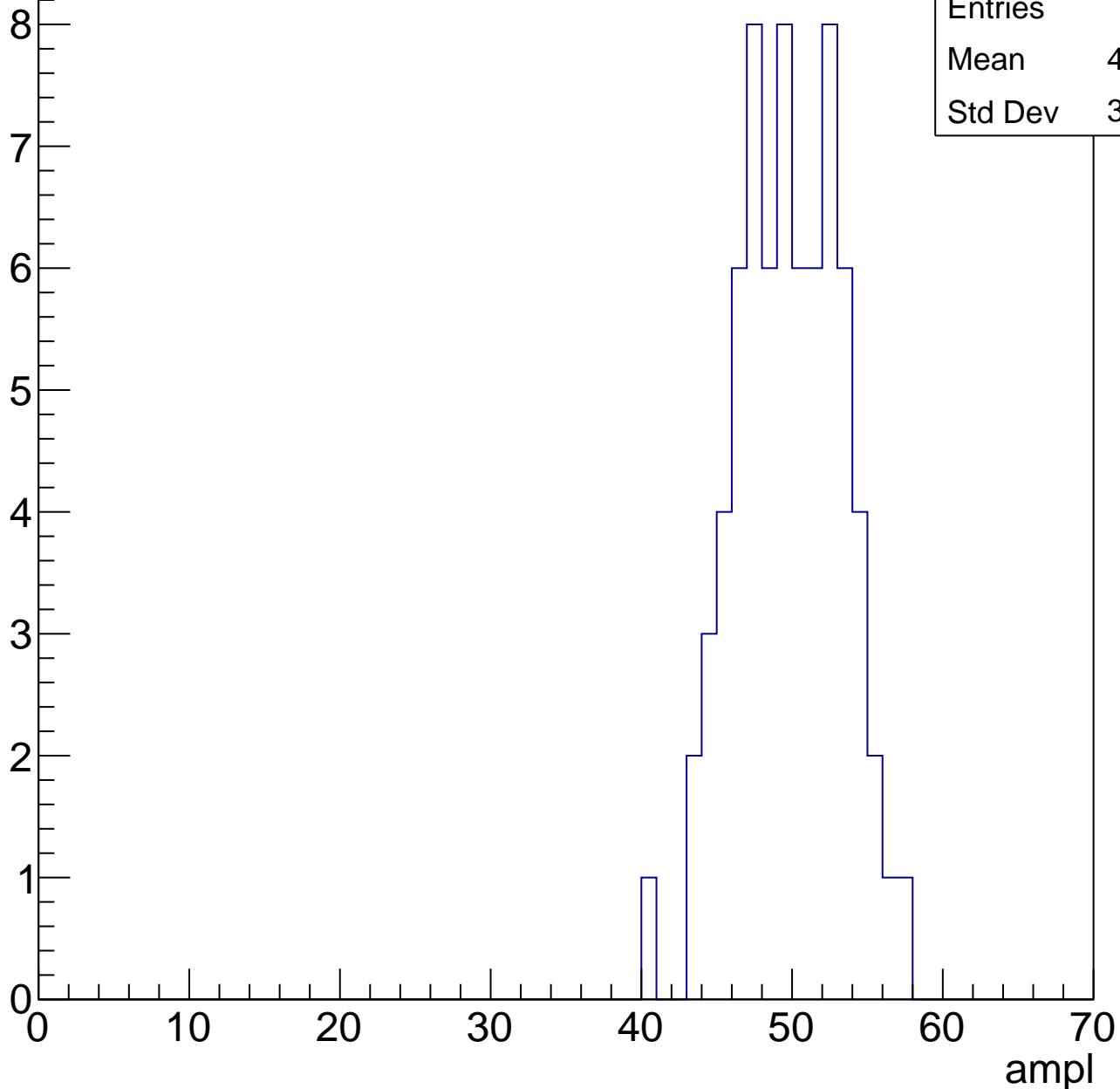
**Gaus Width: 3.3740**



# B1L101S, U18-ch41, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



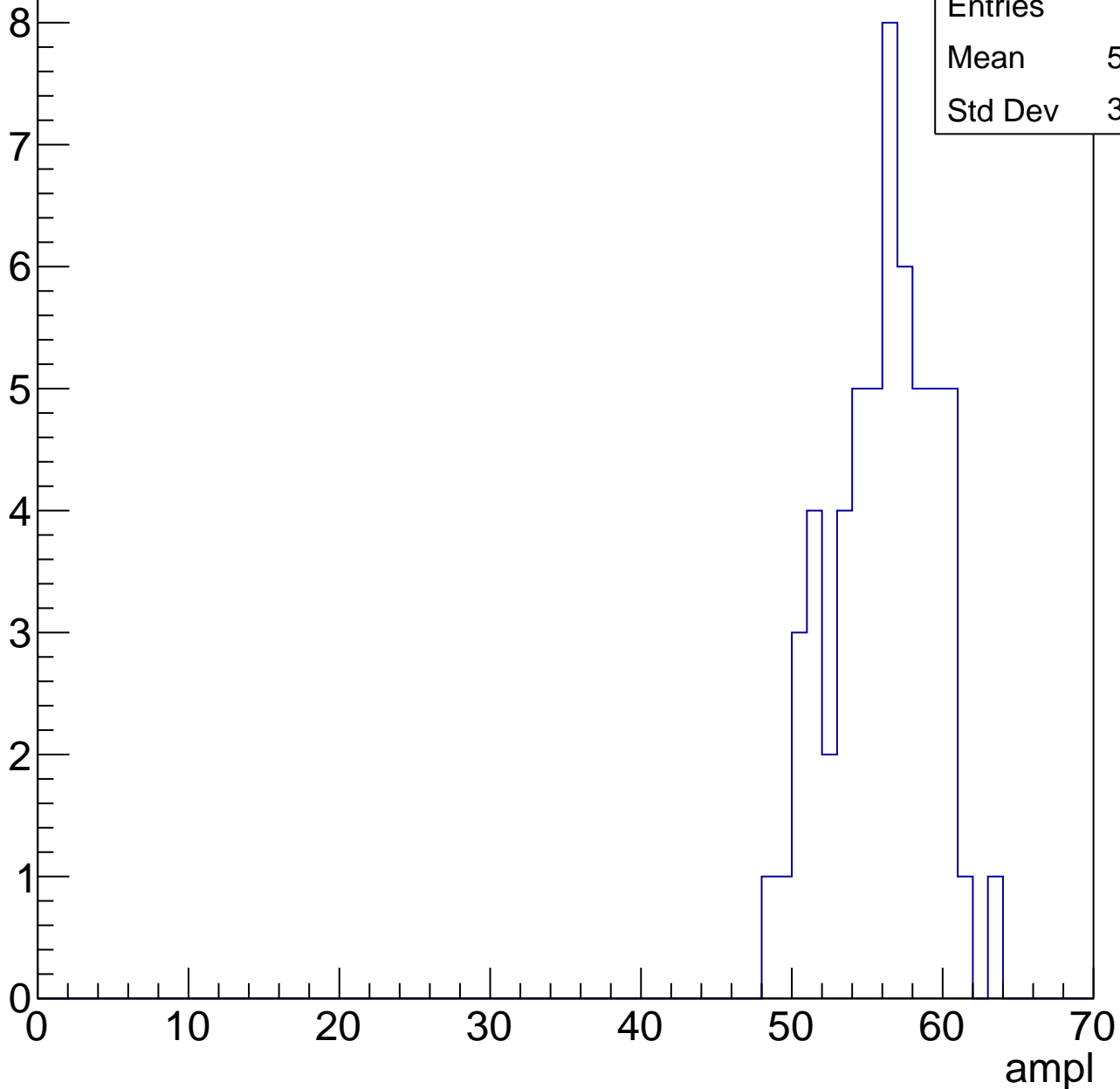
Entries	72
Mean	49.29
Std Dev	3.458

# B1L101S, U18-ch41, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	55.55
Std Dev	3.348



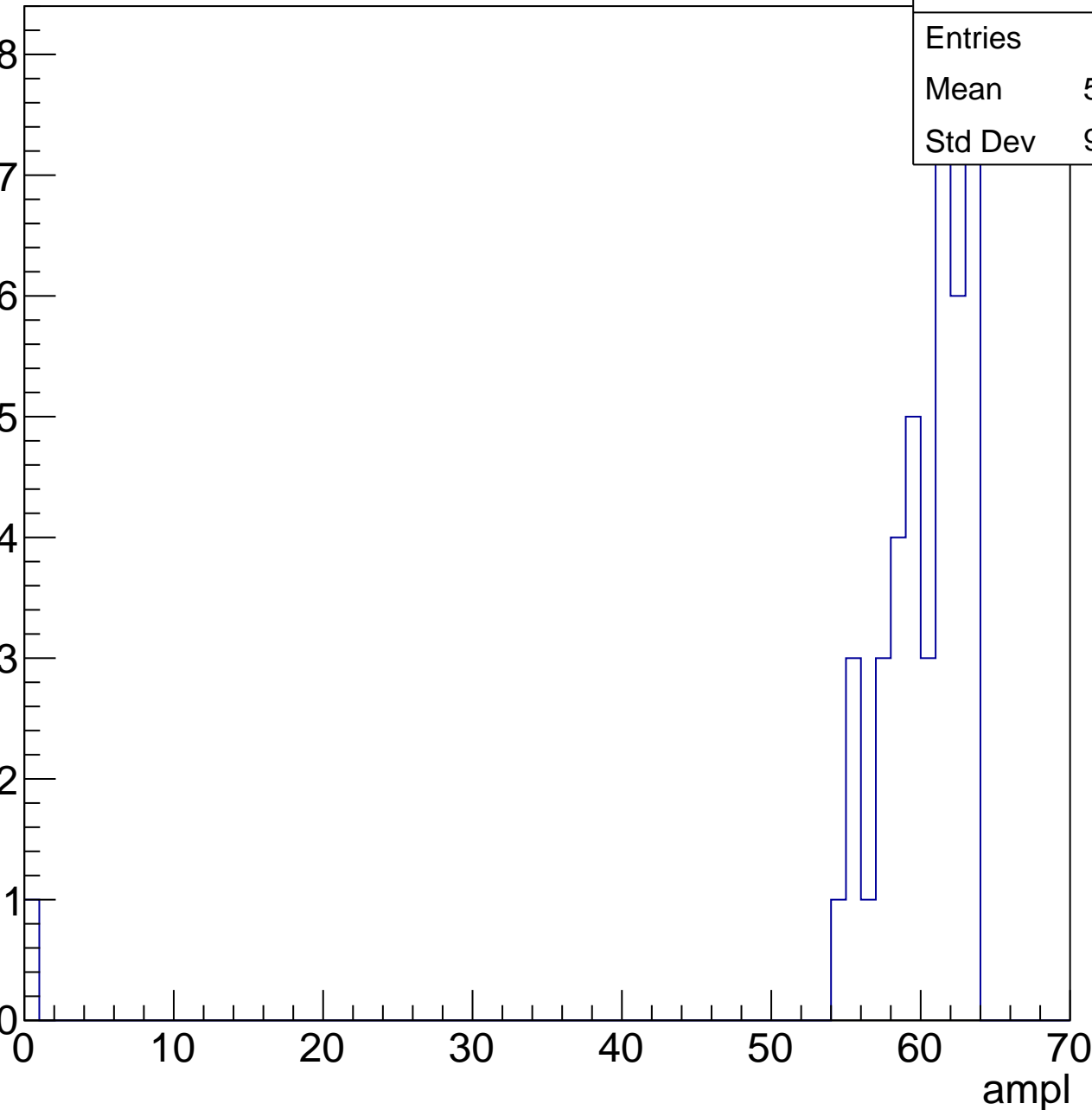
# B1L101S, U18-ch41, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	43
Mean	58.53
Std Dev	9.384

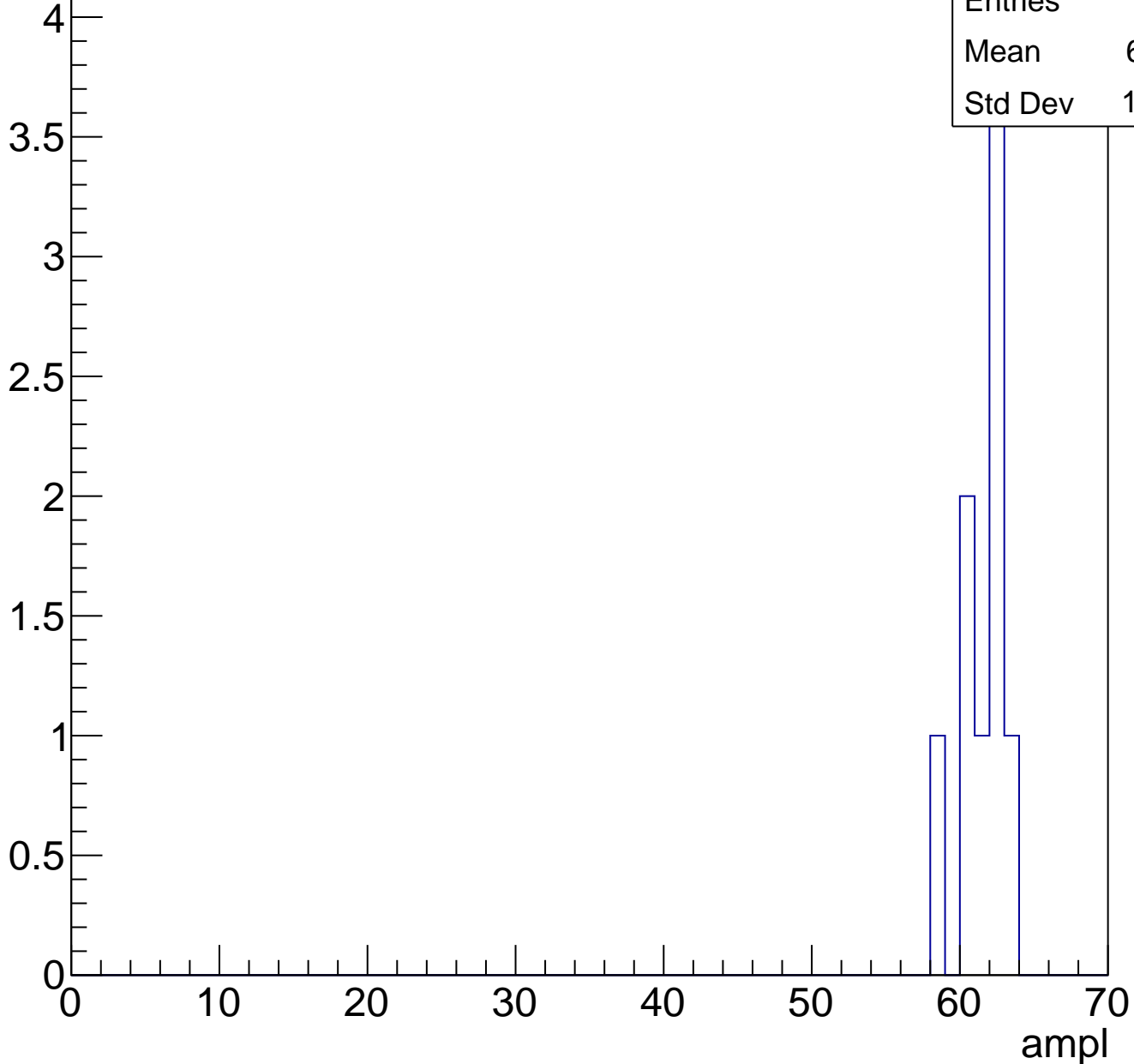
8  
7  
6  
5  
4  
3  
2  
1  
0



# B1L101S, U18-ch41, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch41, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U18-ch42, adc0

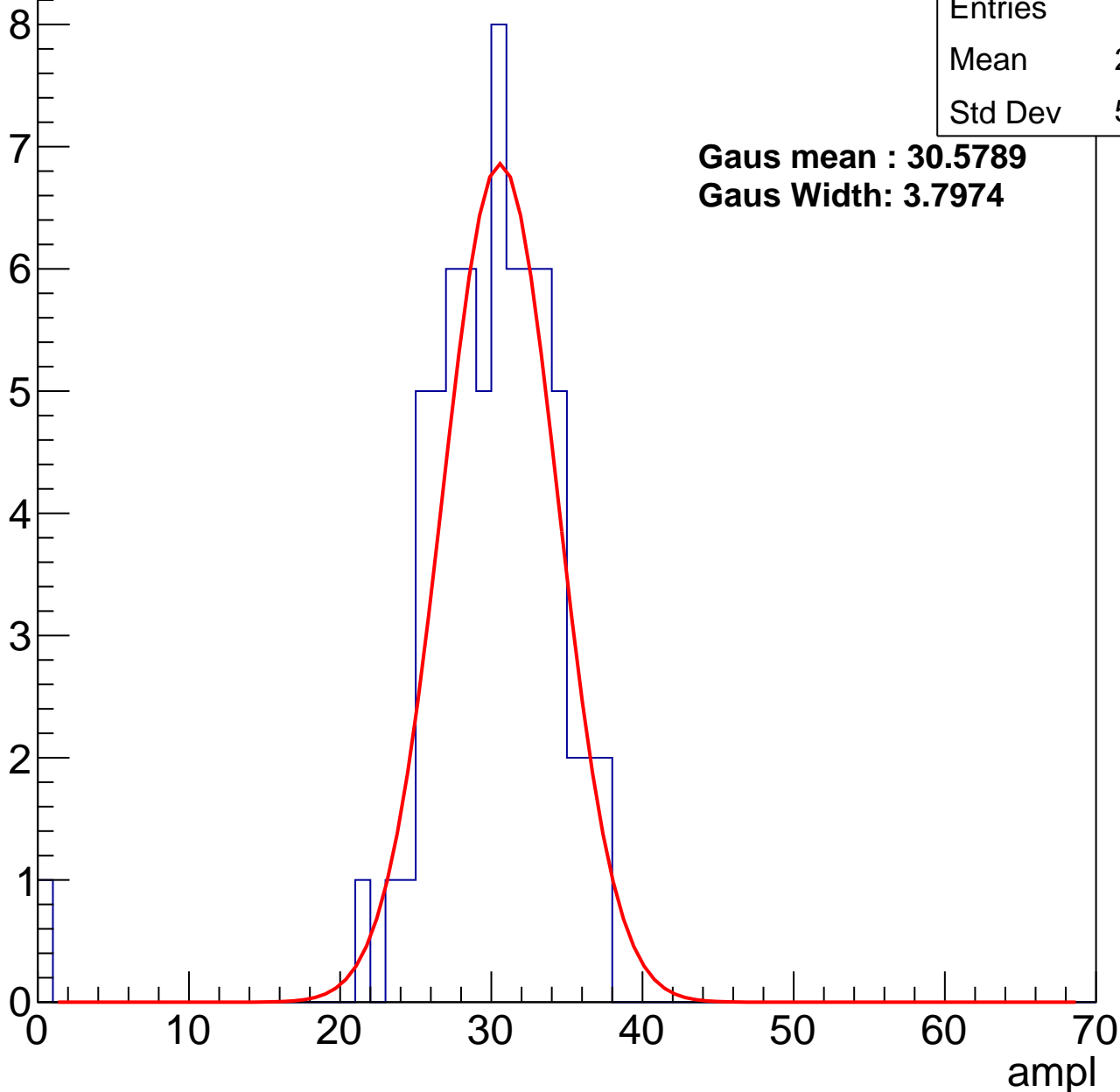
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	29.41
Std Dev	5.021

**Gaus mean : 30.5789**

**Gaus Width: 3.7974**



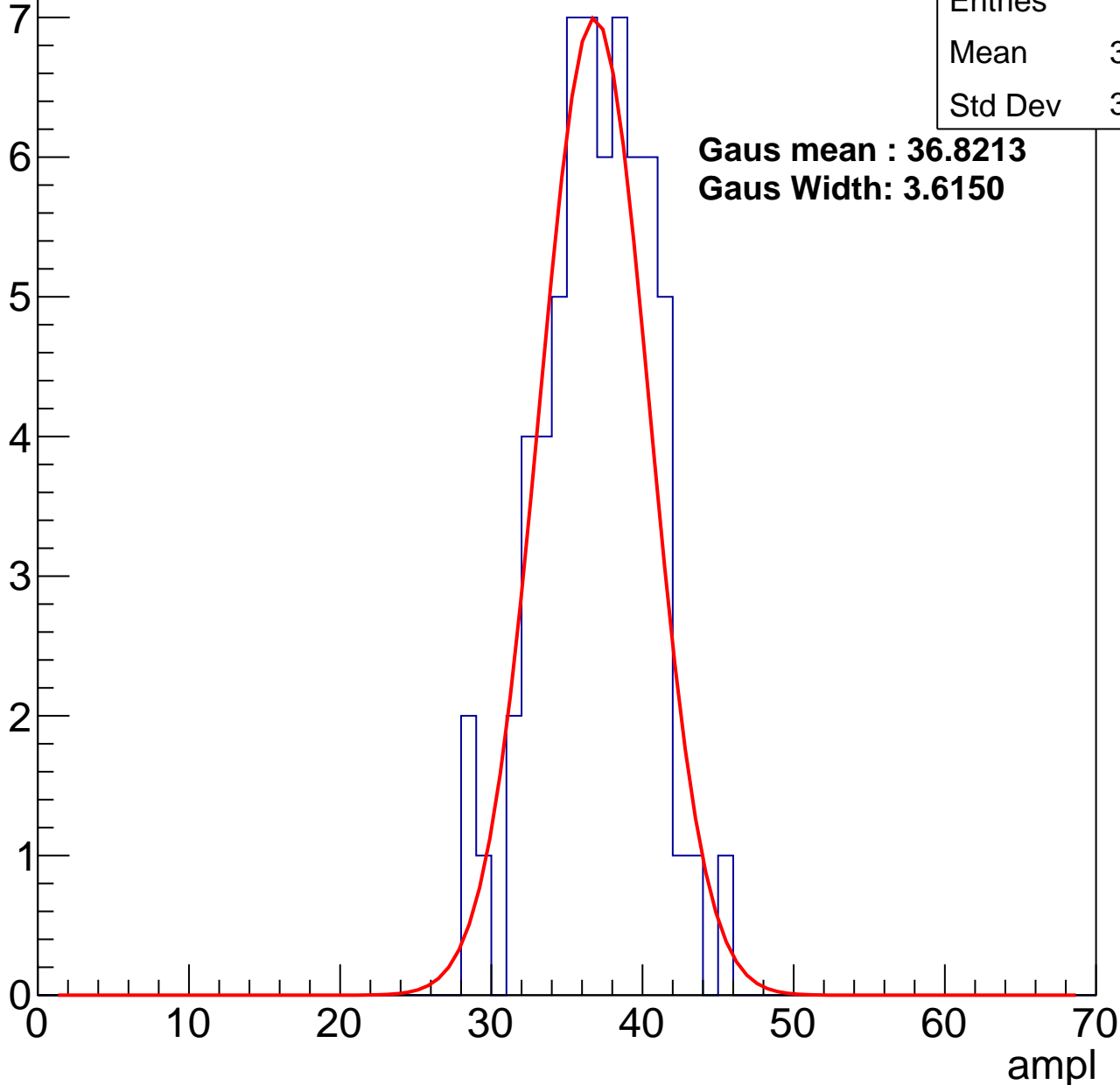
# B1L101S, U18-ch42, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	36.48
Std Dev	3.539

**Gaus mean : 36.8213**  
**Gaus Width: 3.6150**



# B1L101S, U18-ch42, adc2

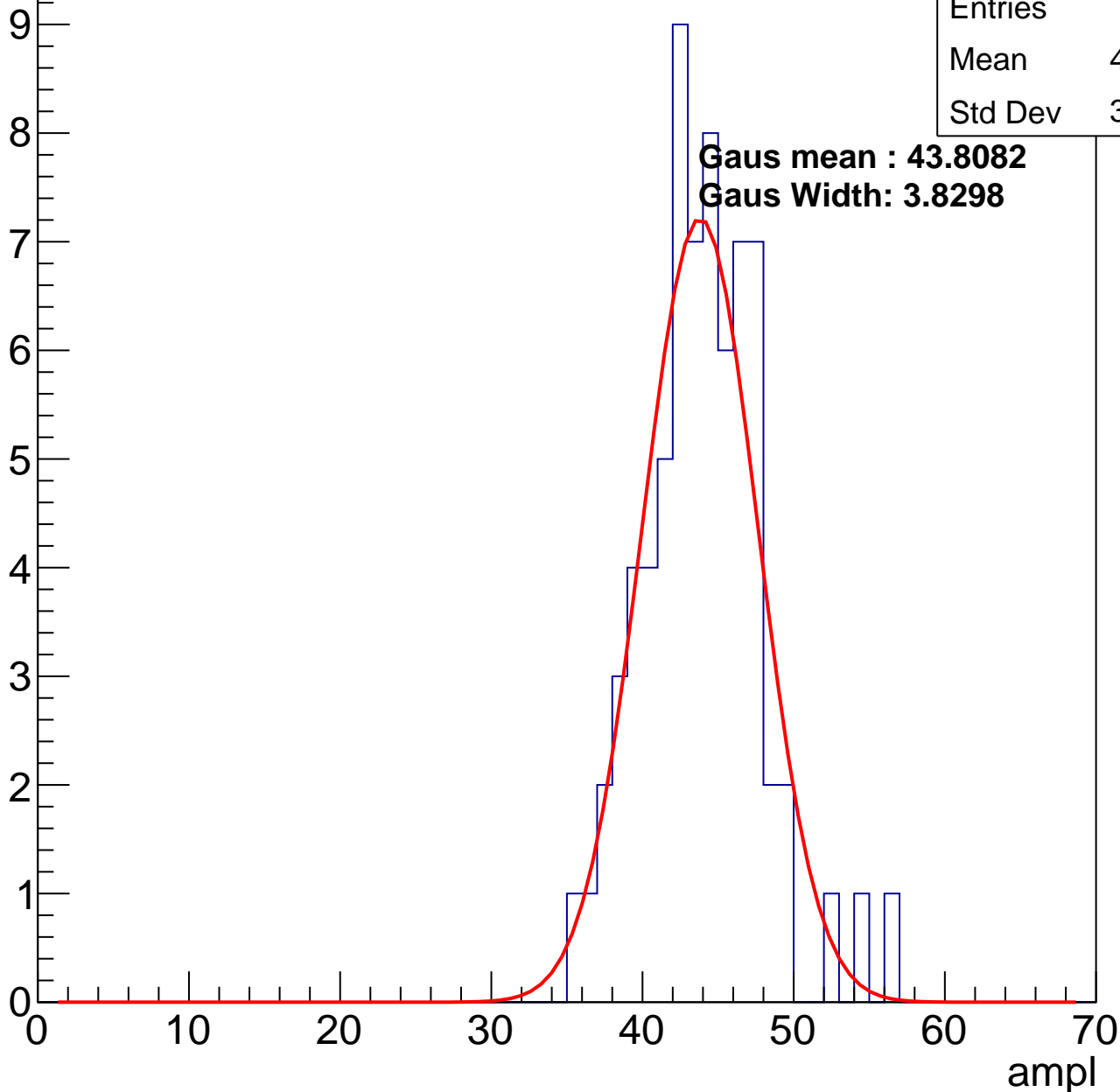
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	43.49
Std Dev	3.885

**Gaus mean : 43.8082**

**Gaus Width: 3.8298**

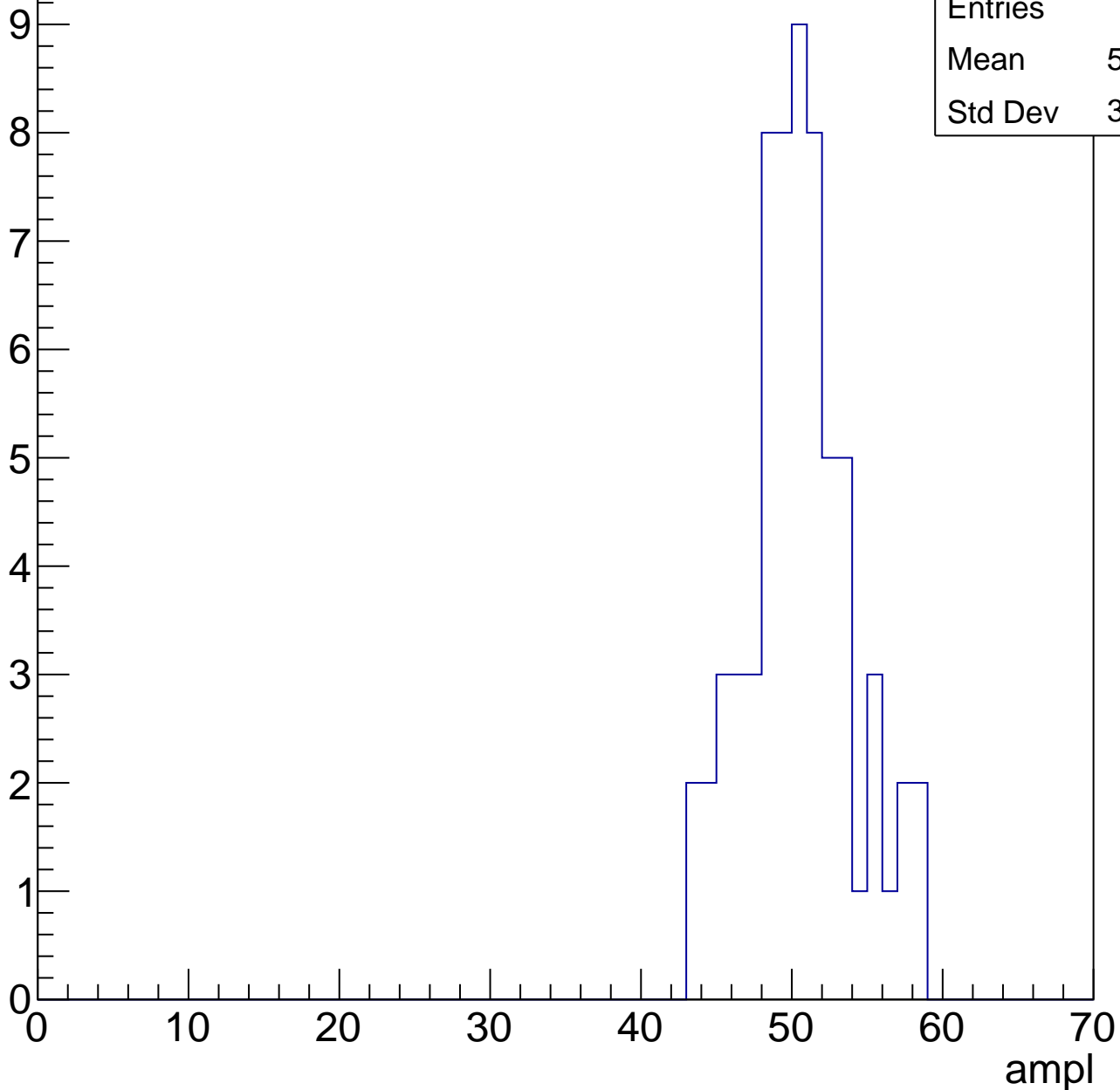


# B1L101S, U18-ch42, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

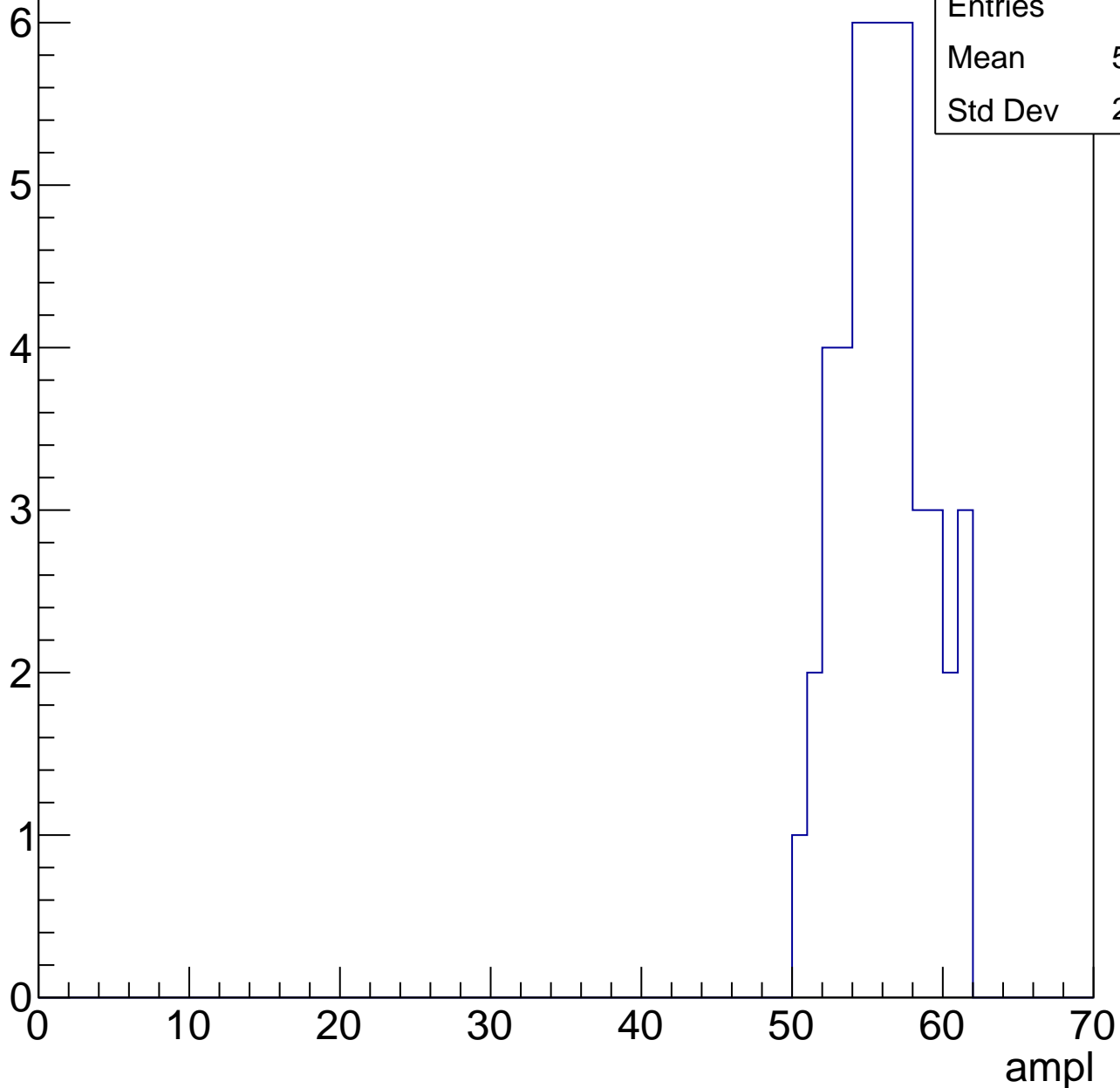
Entries	65
Mean	50.03
Std Dev	3.477



# B1L101S, U18-ch42, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	46
Mean	55.61
Std Dev	2.801

# B1L101S, U18-ch42, adc5

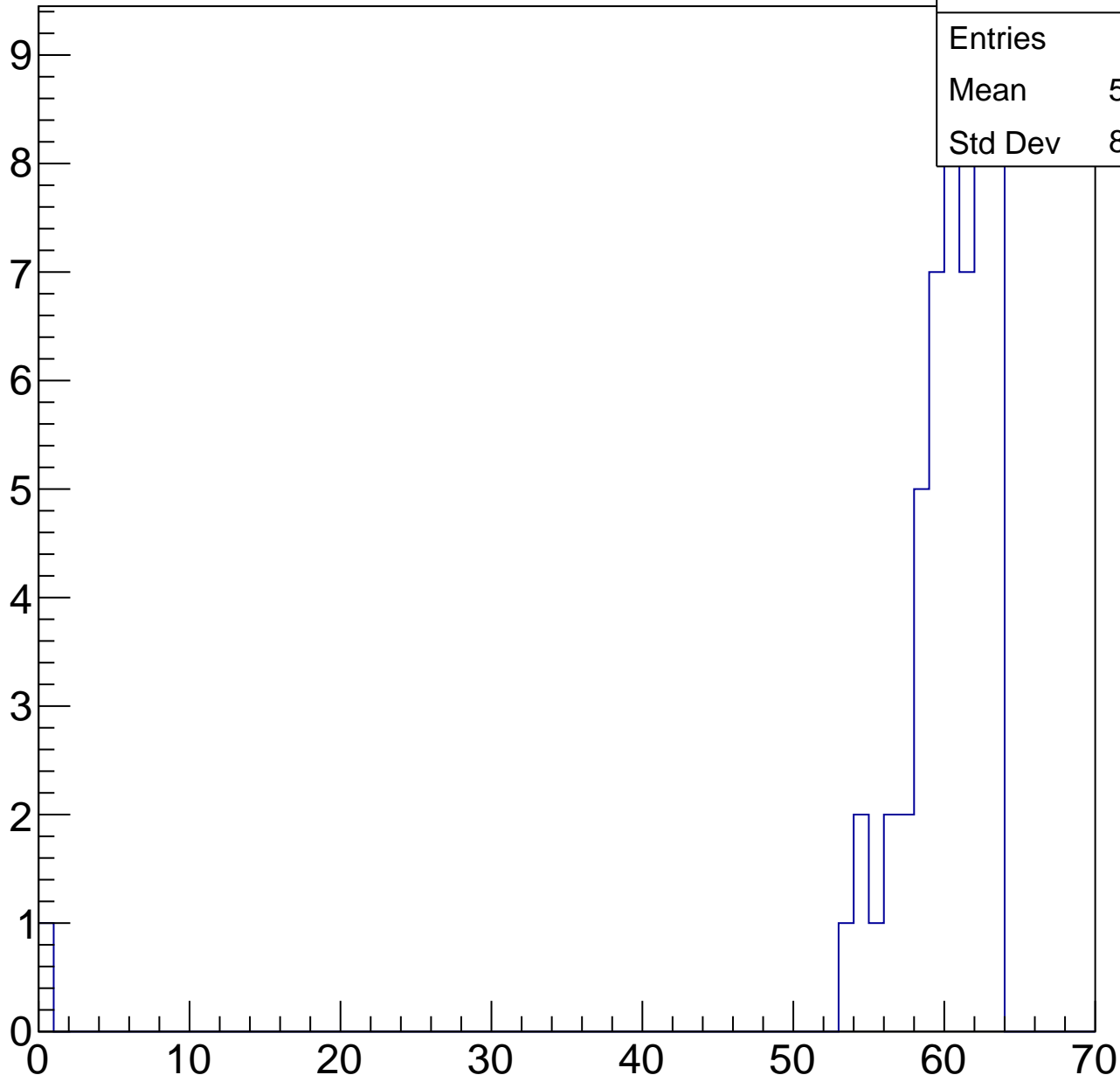
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	53
Mean	58.77
Std Dev	8.538

ampl



# B1L101S, U18-ch42, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.33
Std Dev	0.4714

ampl





# B1L101S, U18-ch42, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch43, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	86
Mean	29.88
Std Dev	7.532

**Gaus mean : 32.3614**

**Gaus Width: 3.3222**

Entry

10  
8  
6  
4  
2  
0

ampl

0

10

20

30

40

50

60

70

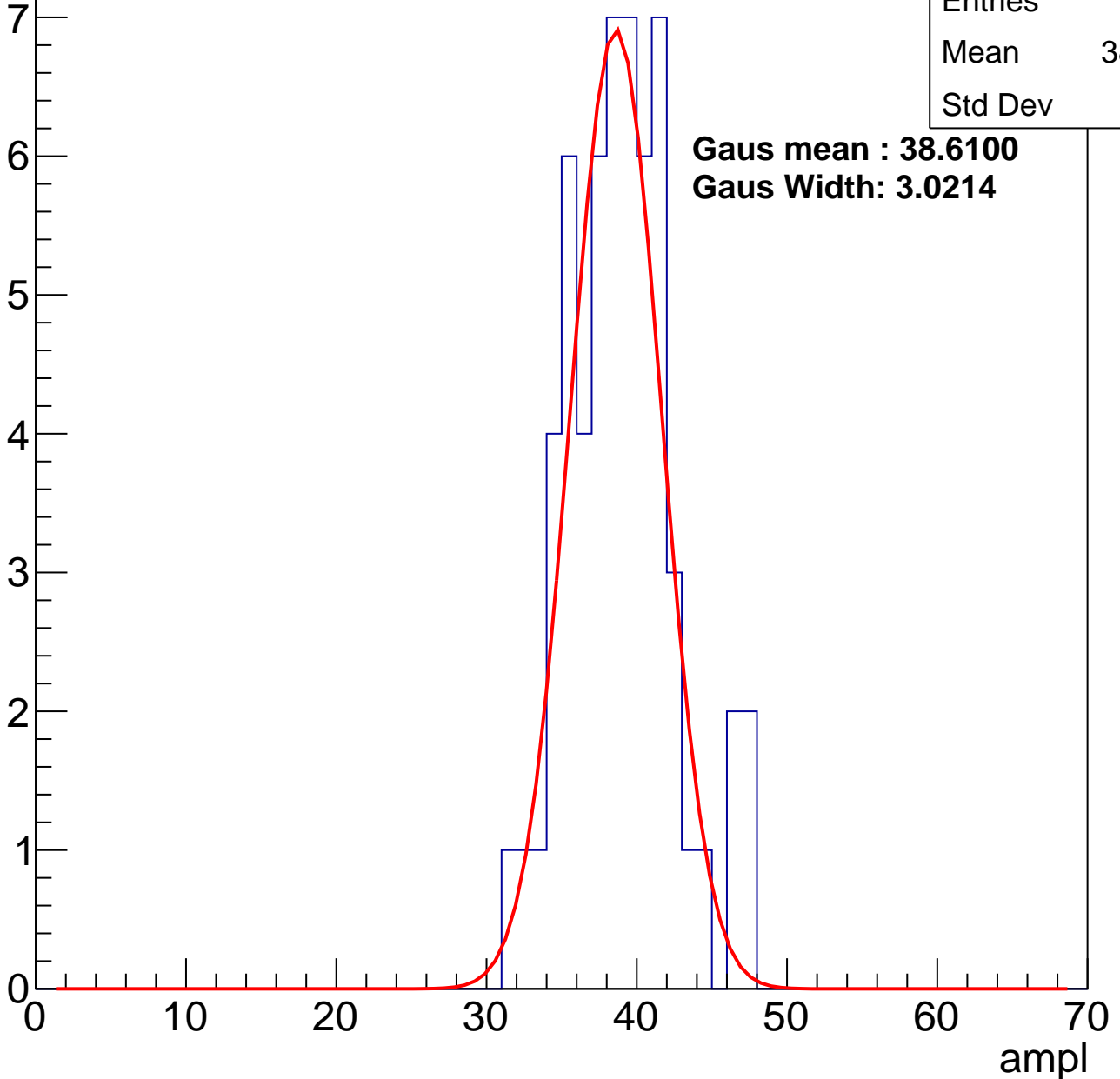
# B1L101S, U18-ch43, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	38.53
Std Dev	3.51

**Gaus mean : 38.6100**  
**Gaus Width: 3.0214**



# B1L101S, U18-ch43, adc2

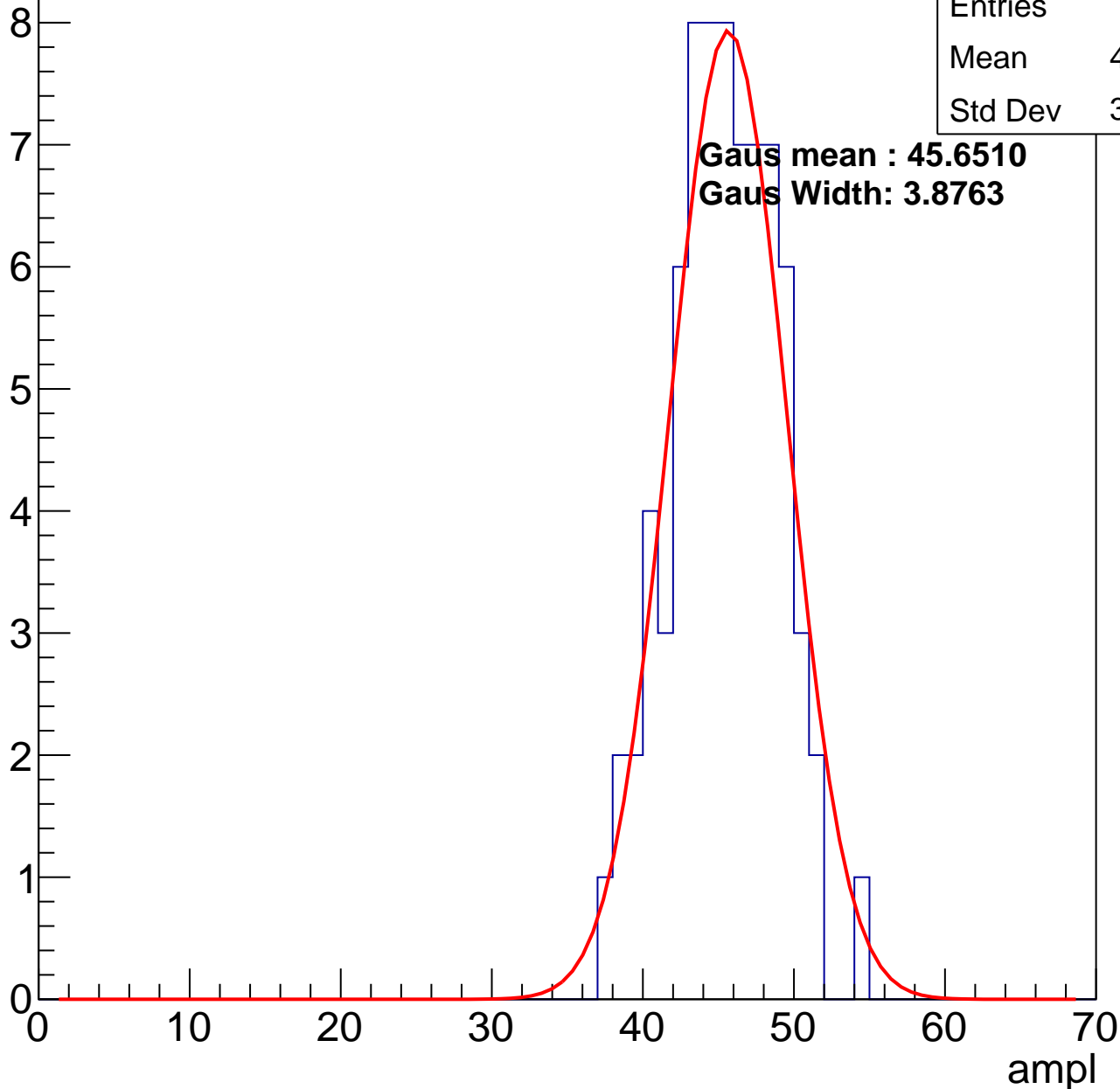
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	44.92
Std Dev	3.459

**Gaus mean : 45.6510**

**Gaus Width: 3.8763**

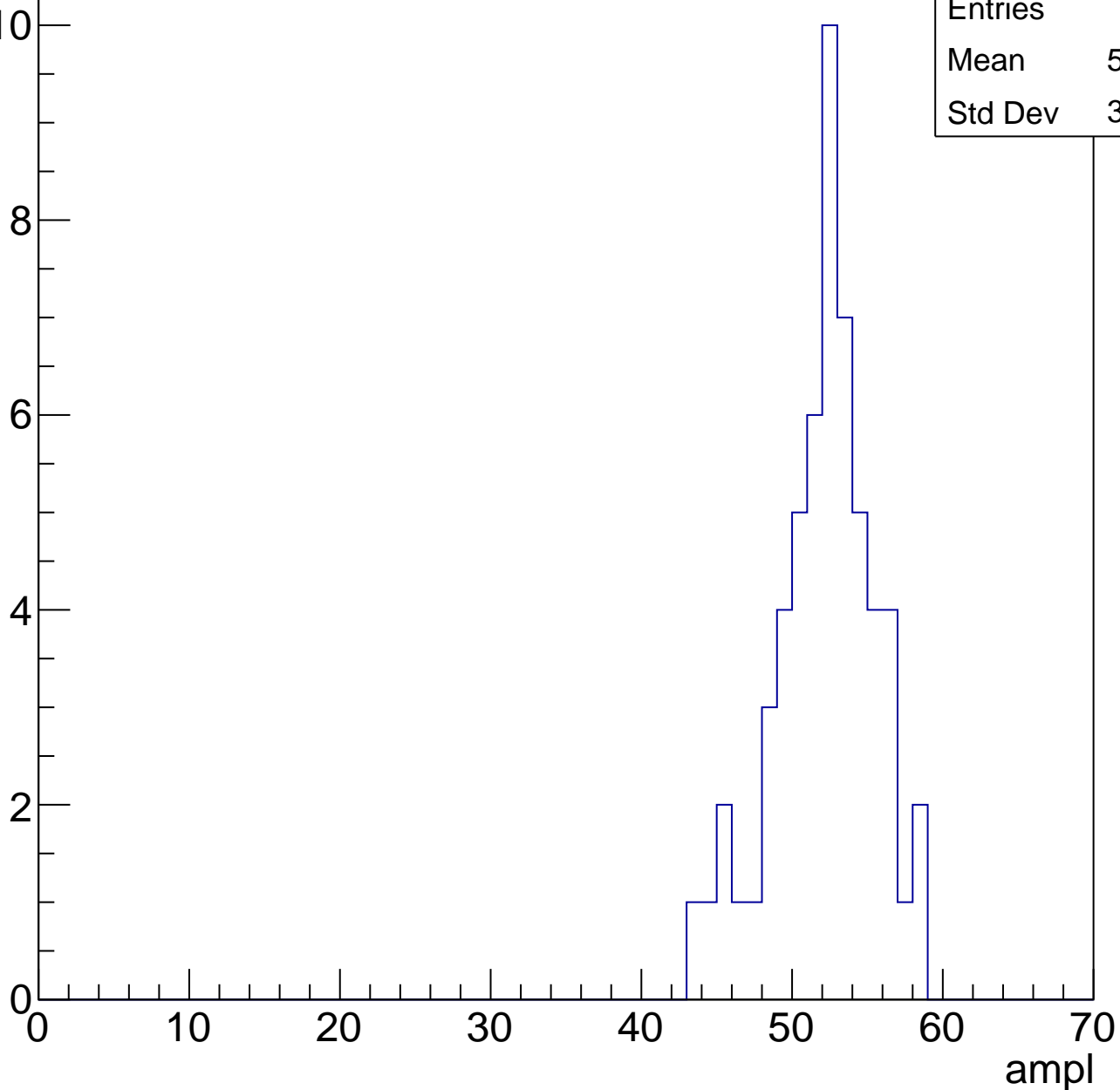


# B1L101S, U18-ch43, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	51.65
Std Dev	3.327

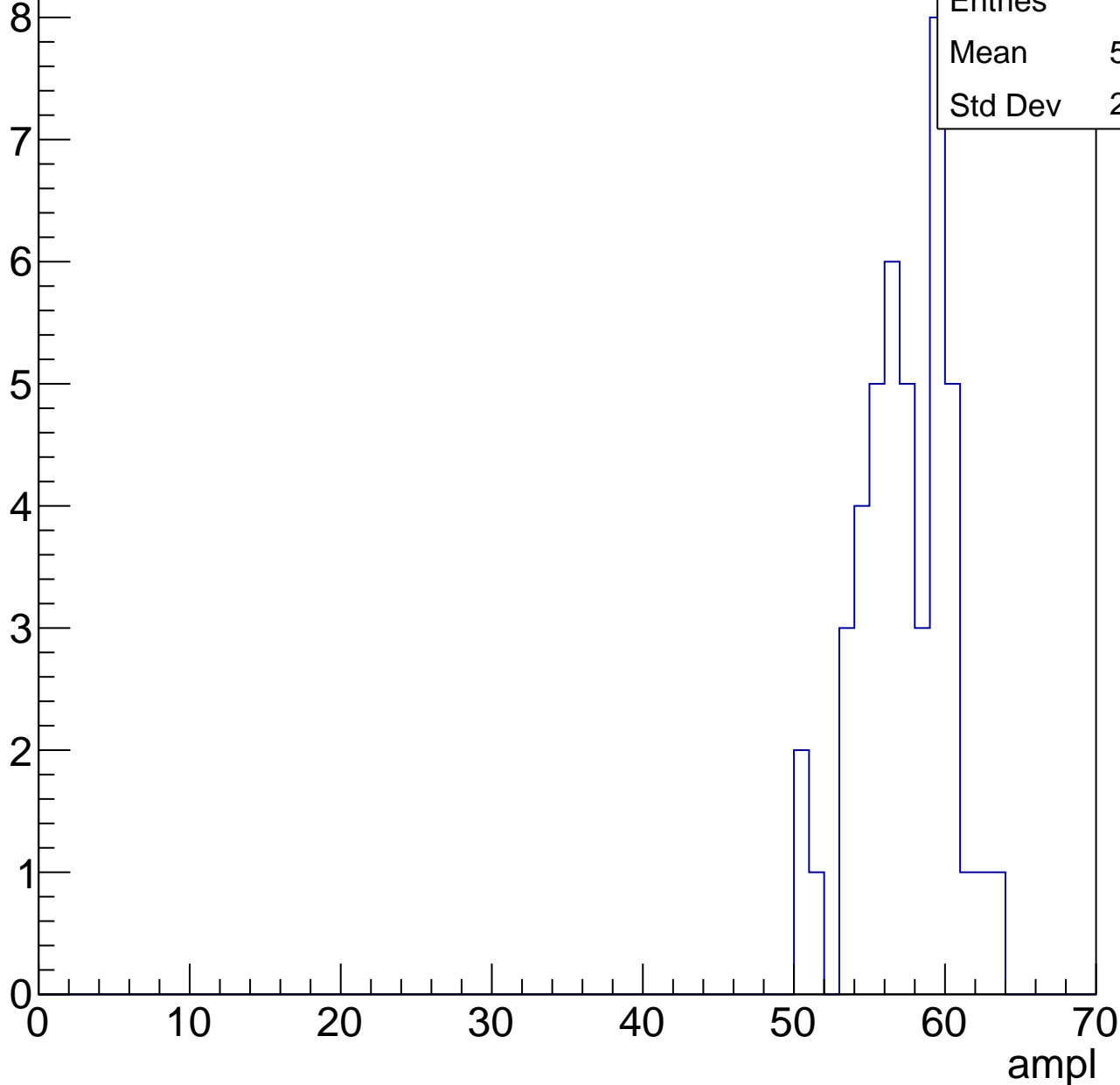


# B1L101S, U18-ch43, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	45
Mean	56.76
Std Dev	2.975

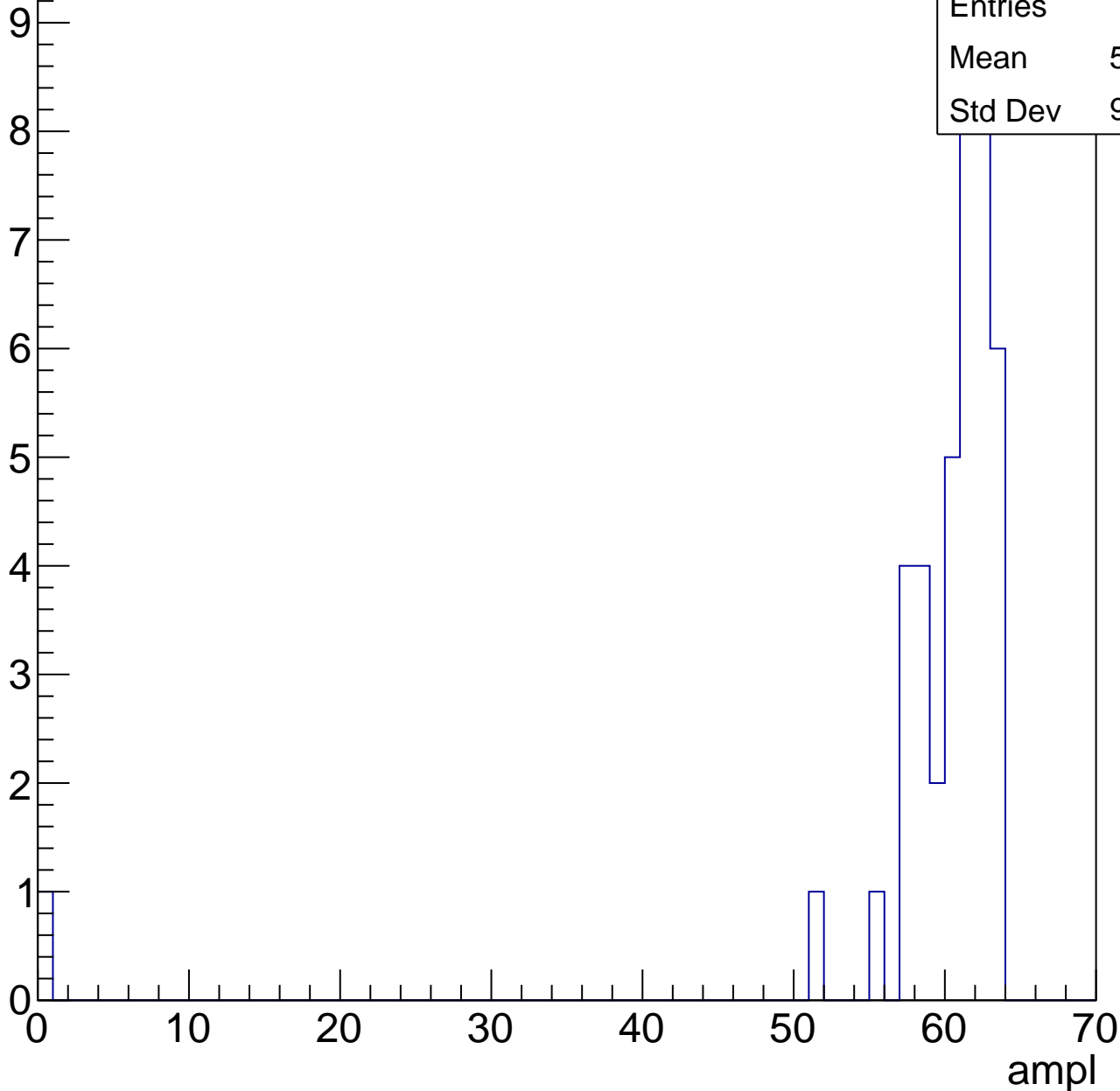


# B1L101S, U18-ch43, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

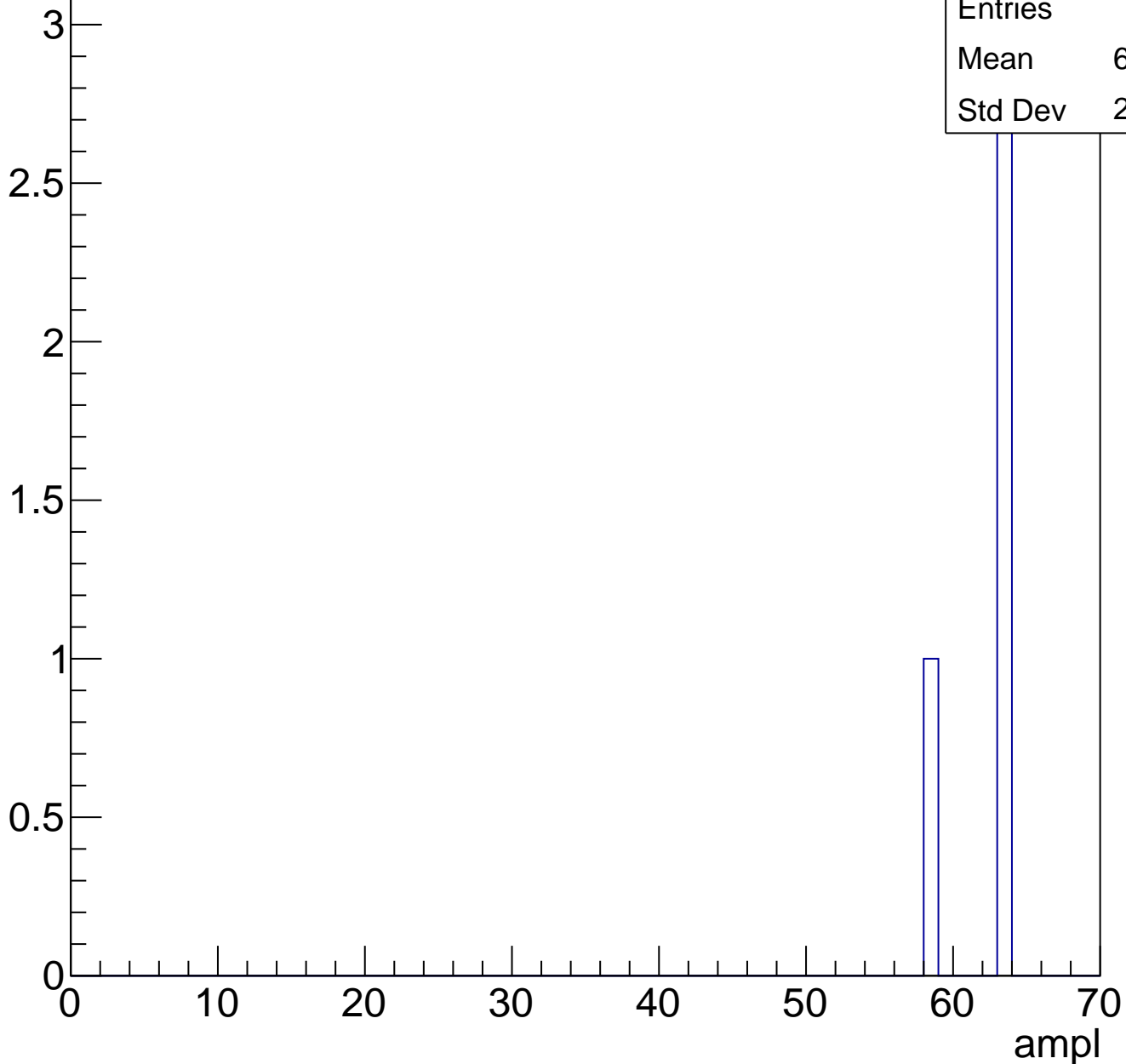
Entries	42
Mean	58.79
Std Dev	9.508



# B1L101S, U18-ch43, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch43, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U18-ch44, adc0

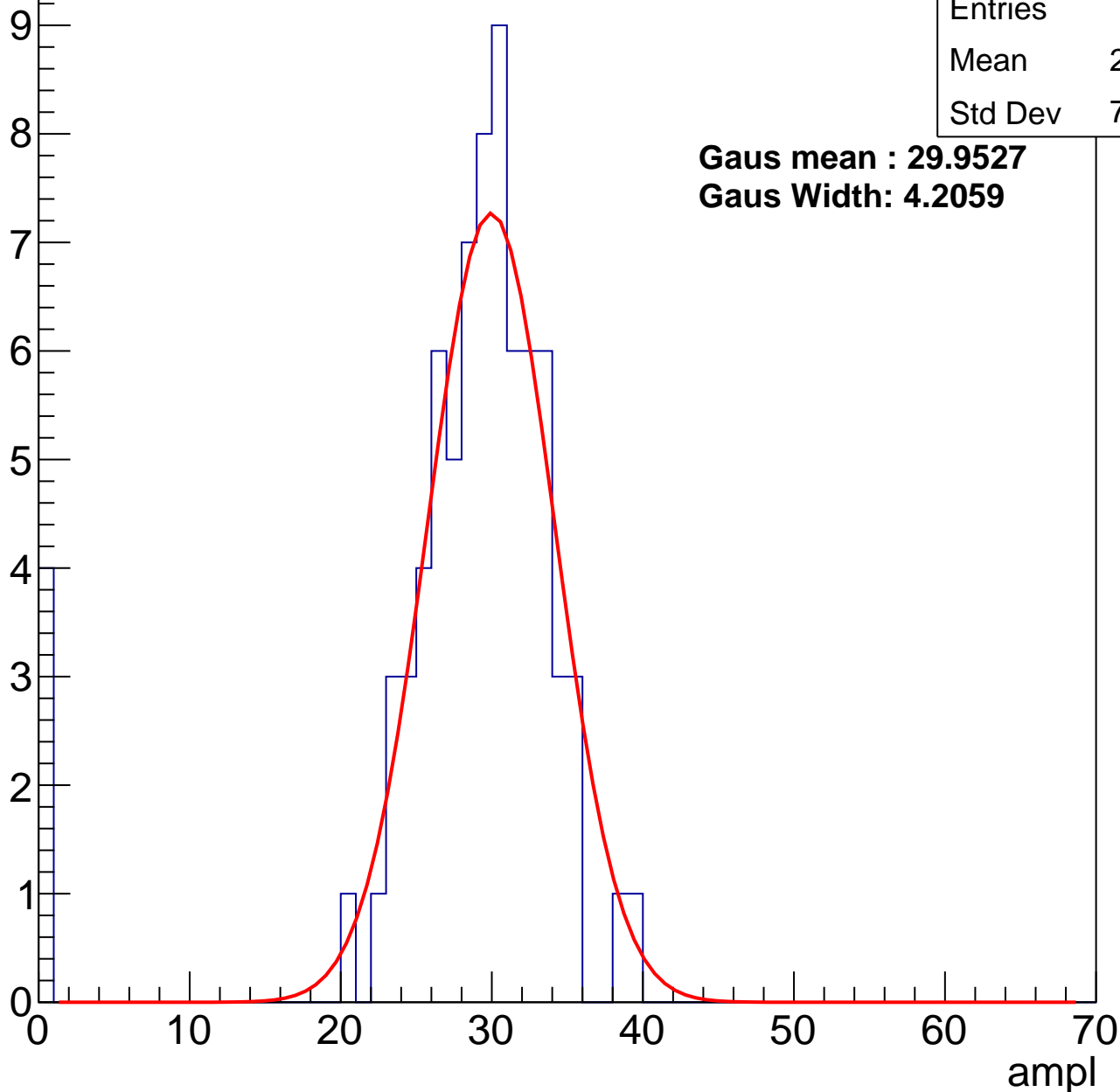
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	27.69
Std Dev	7.418

**Gaus mean : 29.9527**

**Gaus Width: 4.2059**



# B1L101S, U18-ch44, adc1

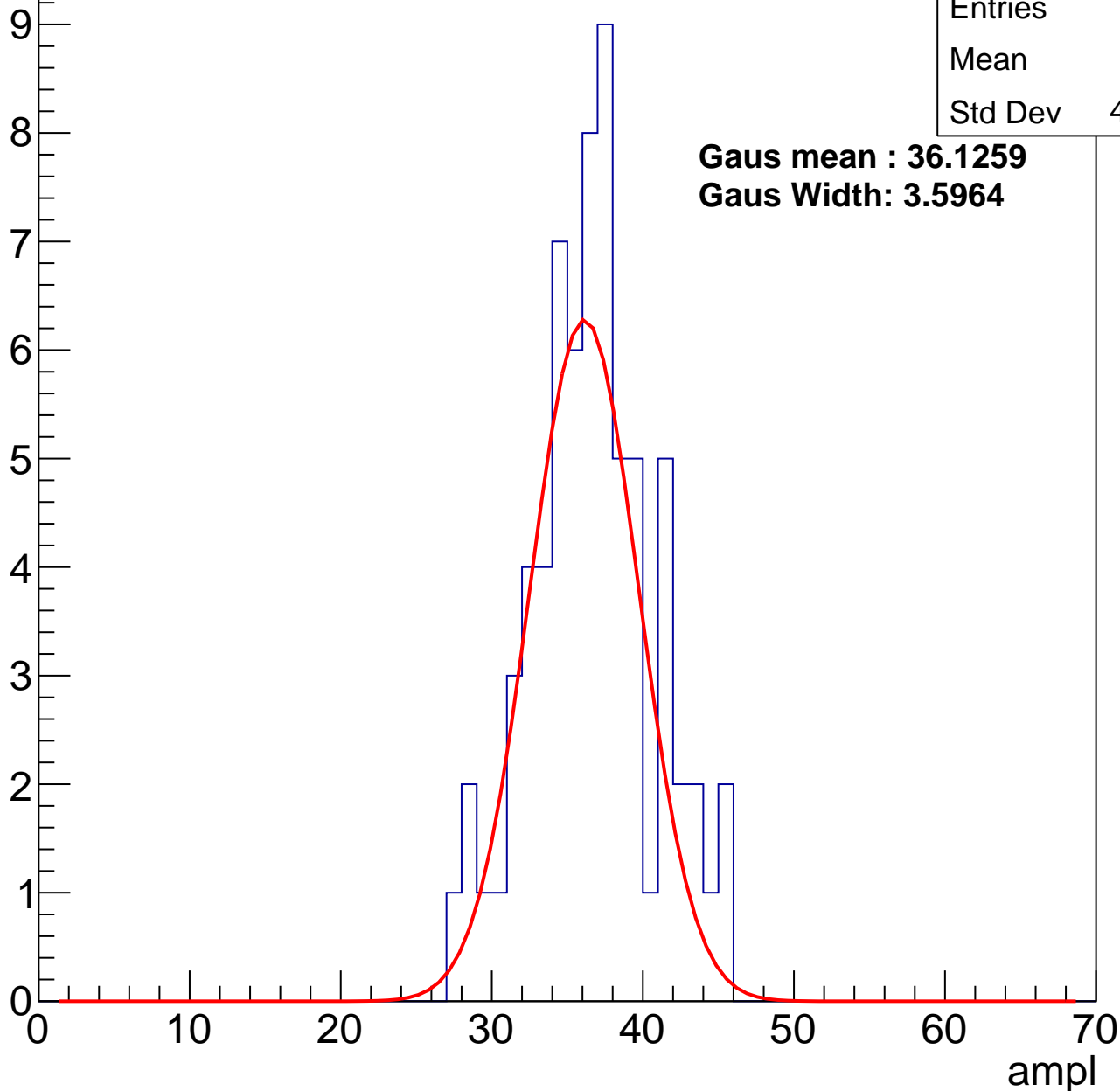
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	36.2
Std Dev	4.013

**Gaus mean : 36.1259**

**Gaus Width: 3.5964**



# B1L101S, U18-ch44, adc2

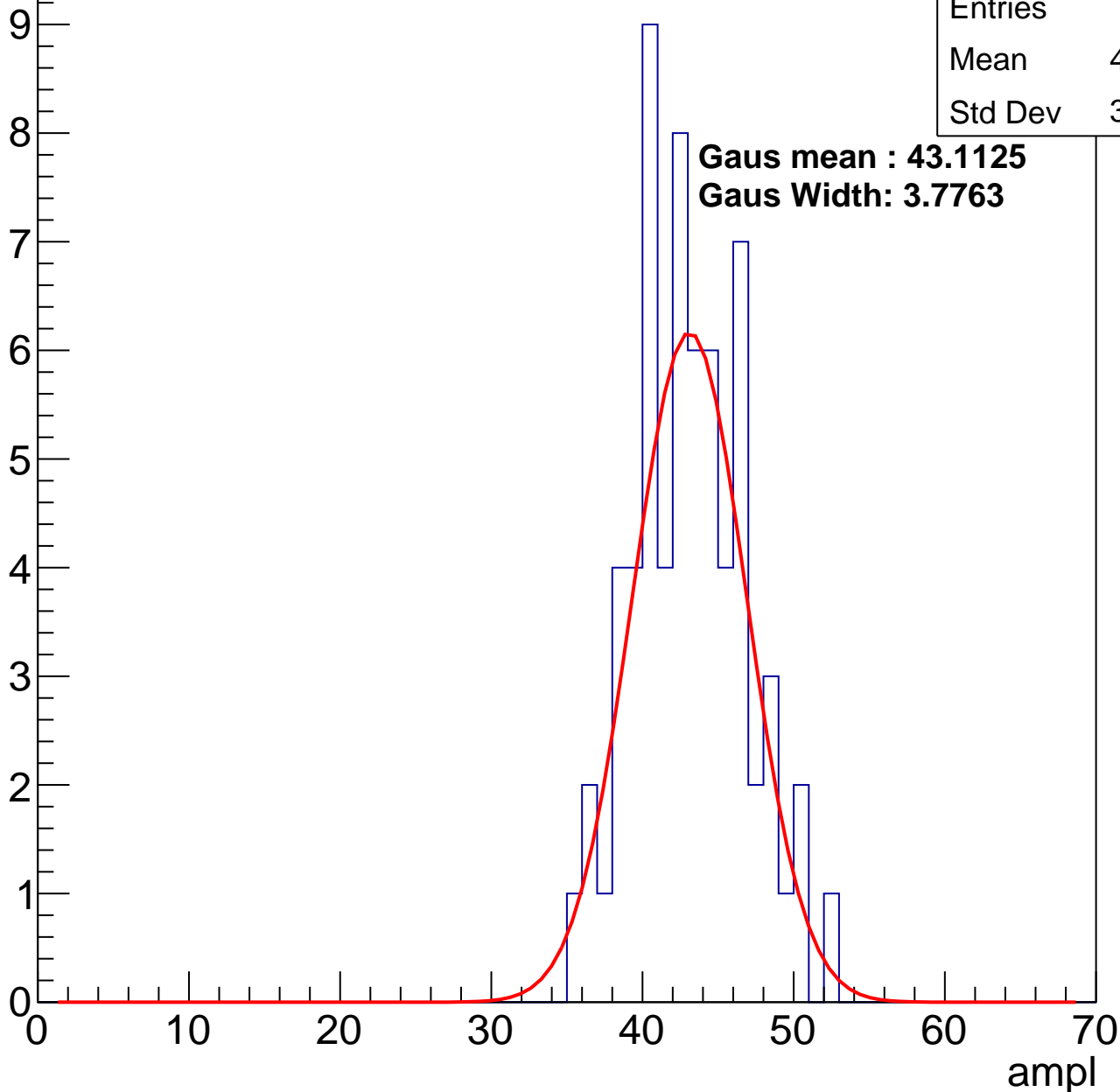
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	42.69
Std Dev	3.654

**Gaus mean : 43.1125**

**Gaus Width: 3.7763**

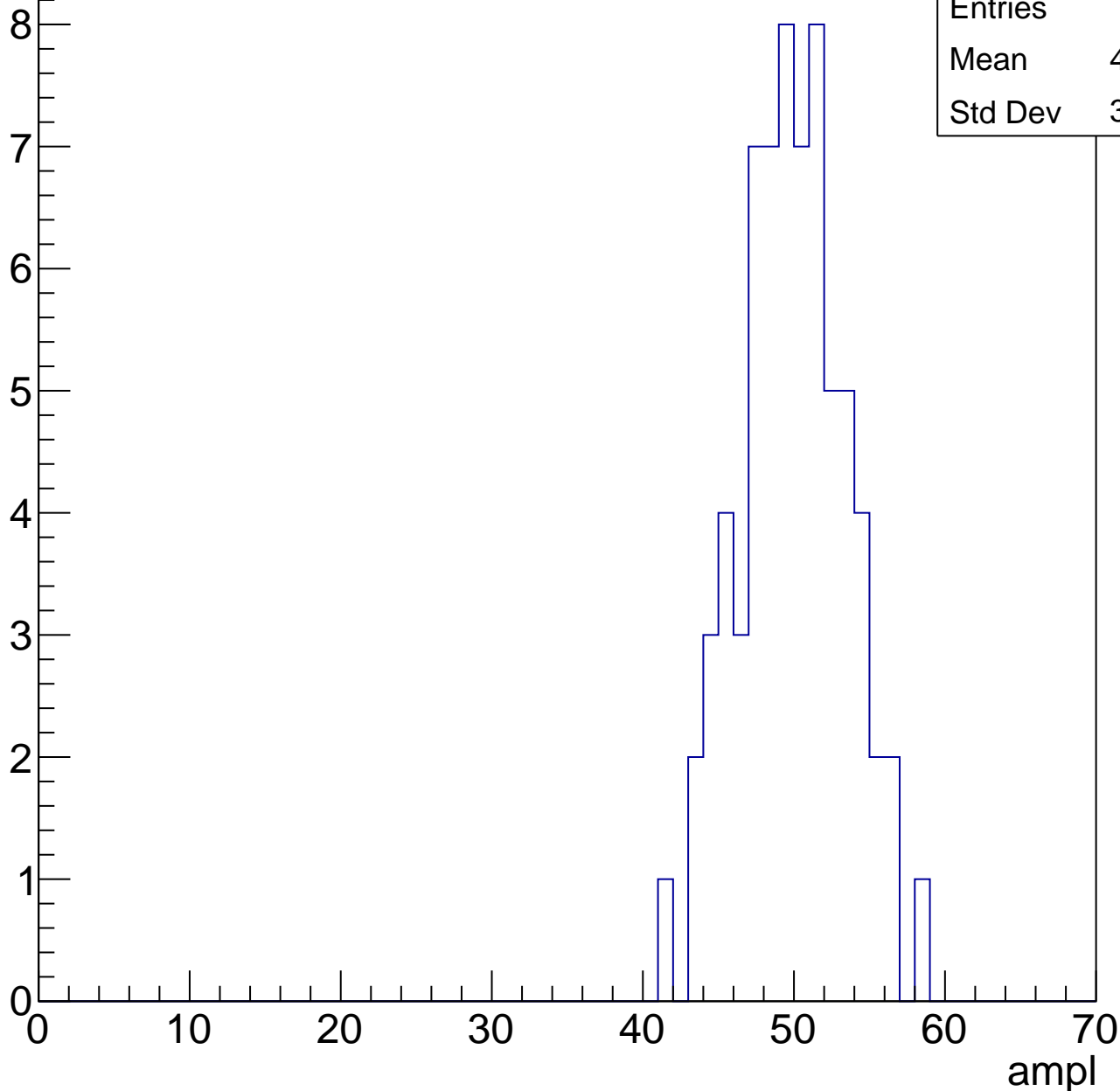


# B1L101S, U18-ch44, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	49.46
Std Dev	3.483

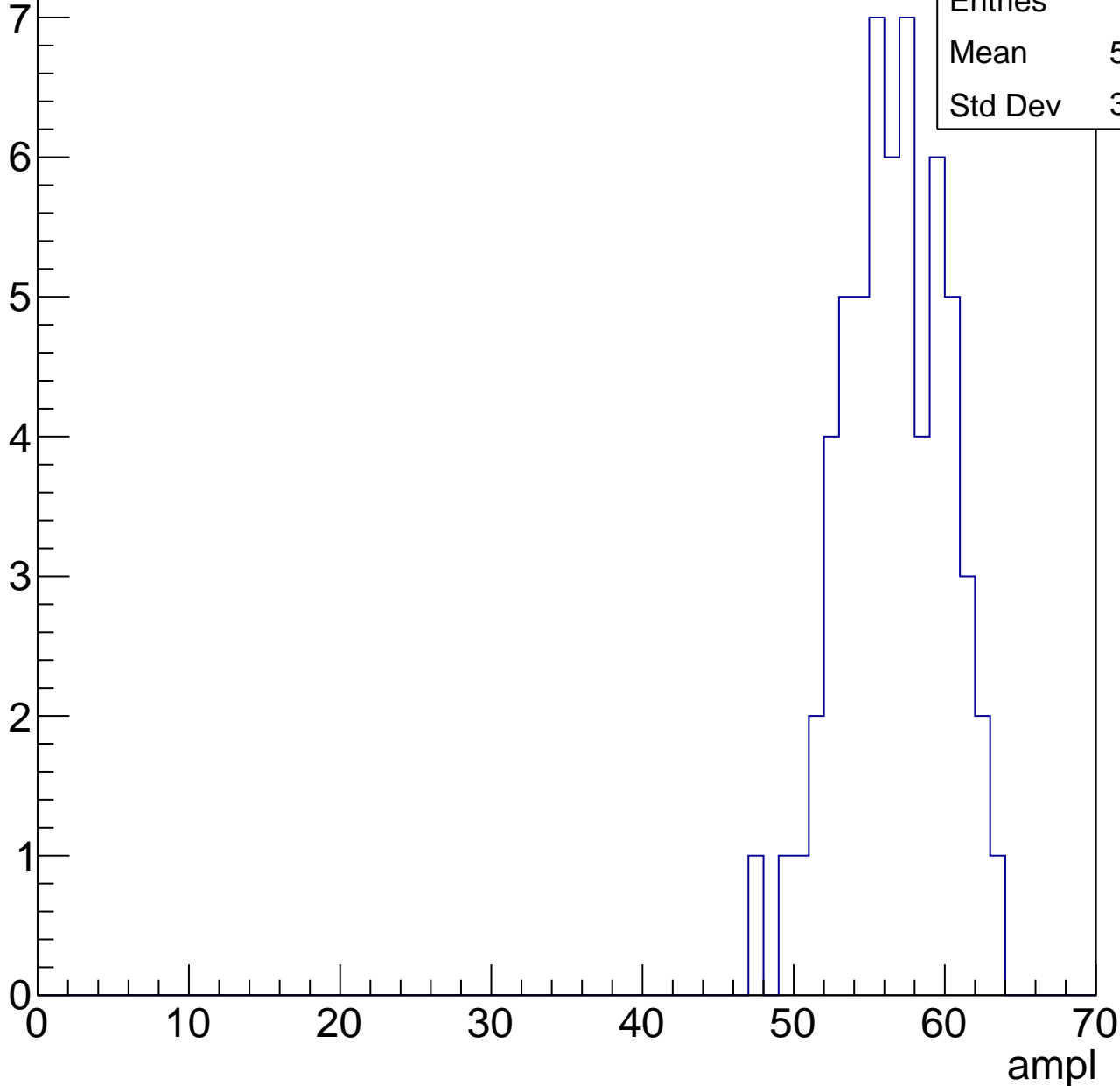


# B1L101S, U18-ch44, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	56.12
Std Dev	3.426

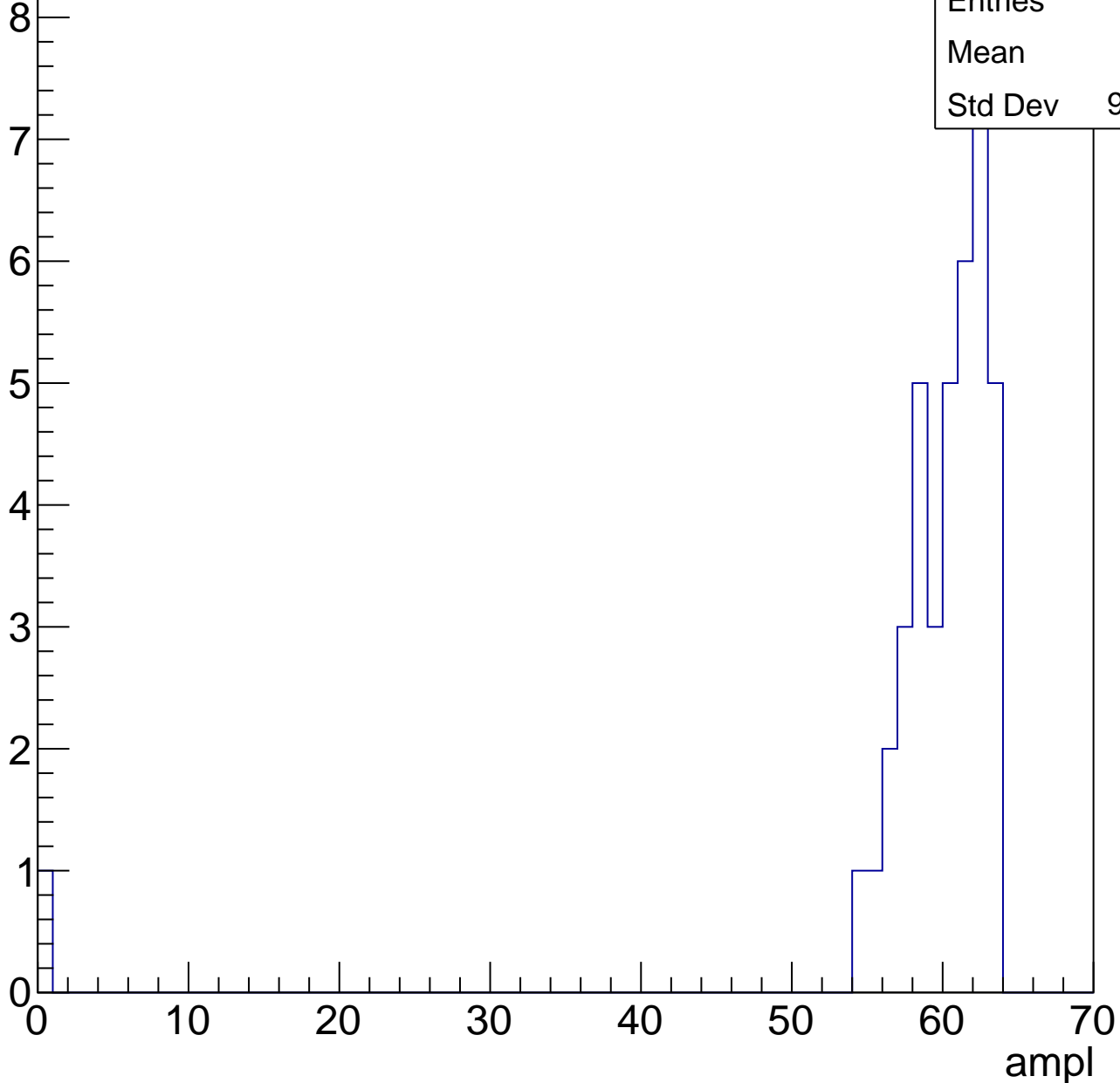


# B1L101S, U18-ch44, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

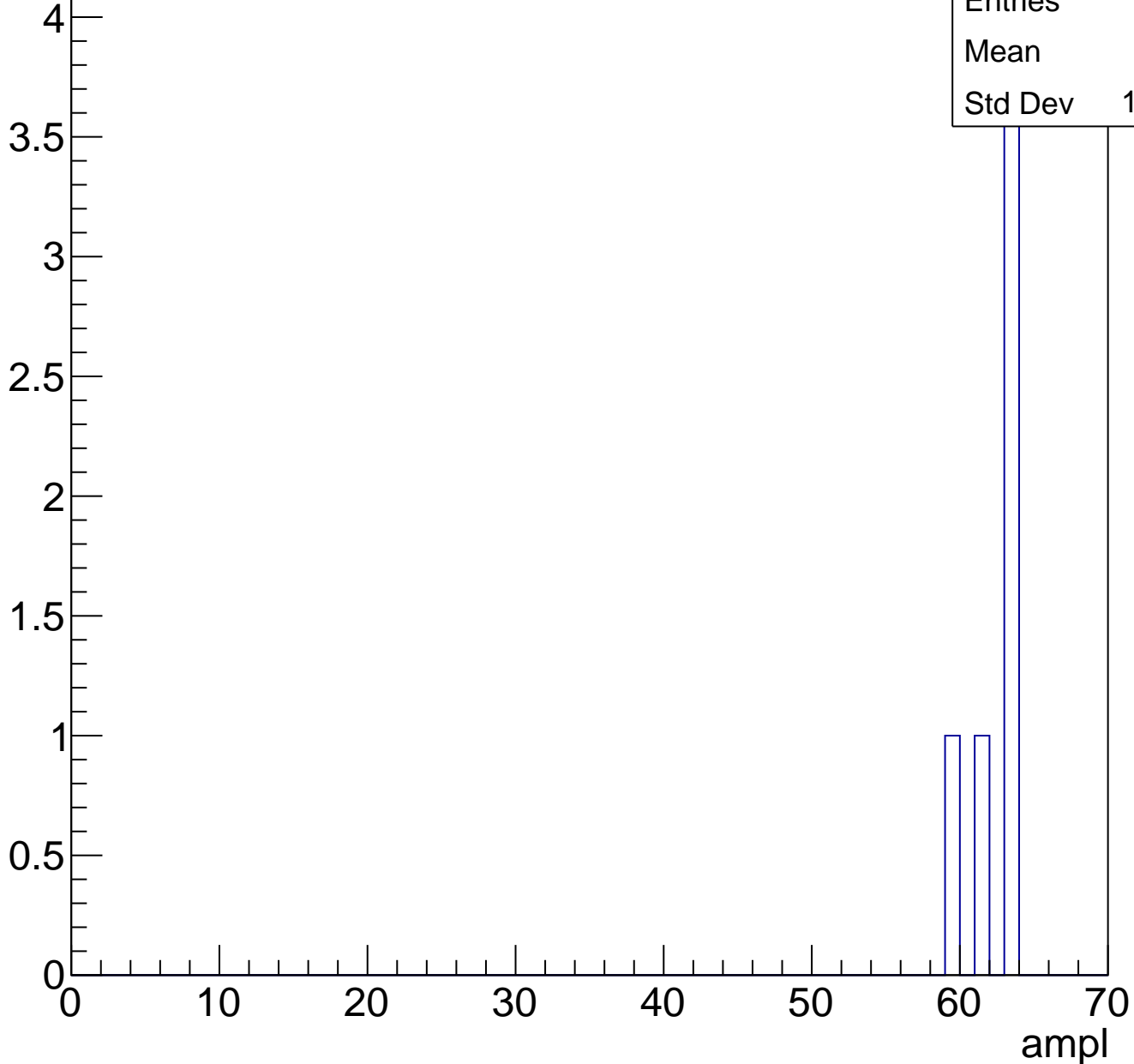
Entries	40
Mean	58.4
Std Dev	9.648



# B1L101S, U18-ch44, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch44, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L101S, U18-ch45, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	79
Mean	29.76
Std Dev	4.827

**Gaus mean : 30.3528**

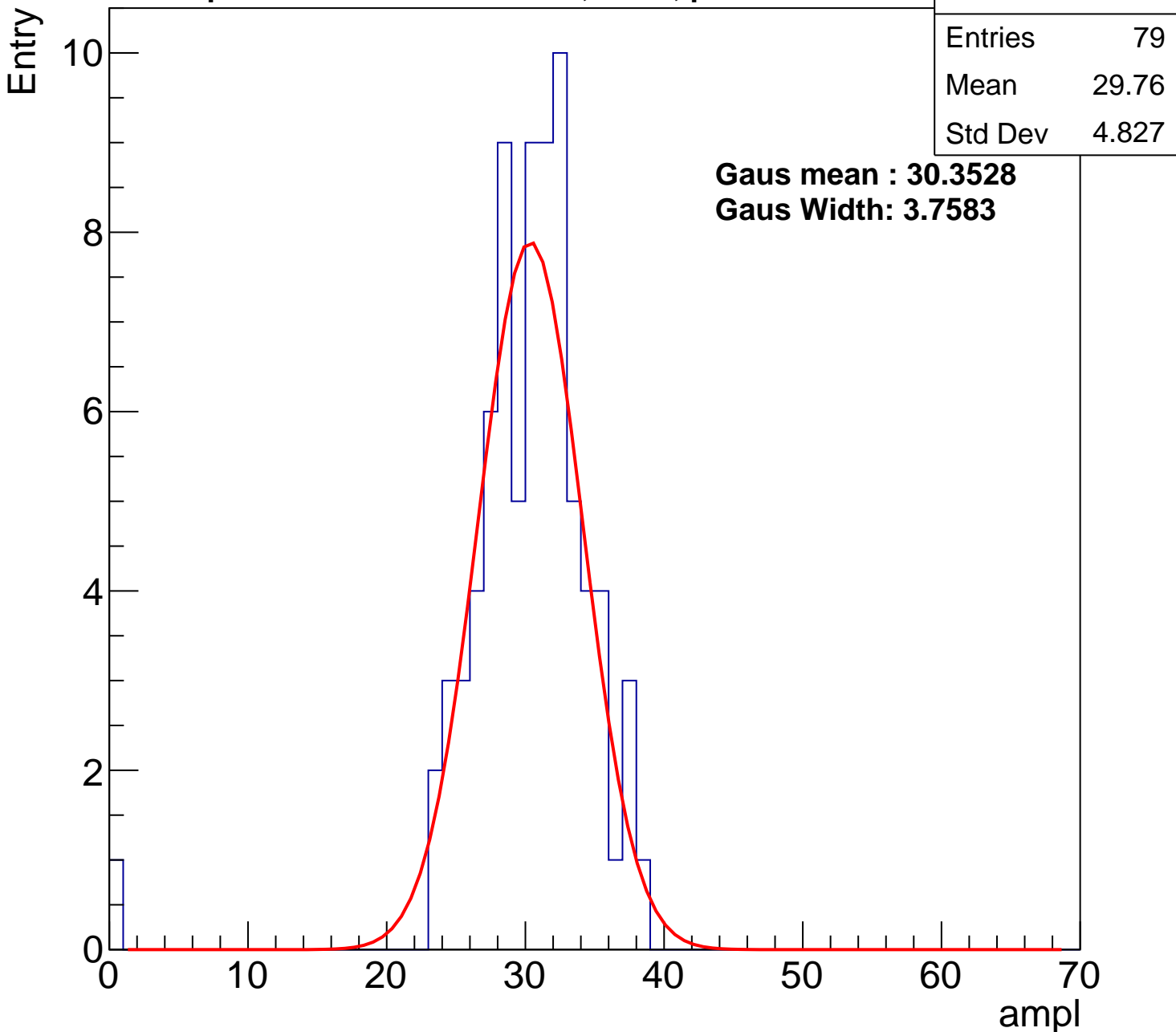
**Gaus Width: 3.7583**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U18-ch45, adc1

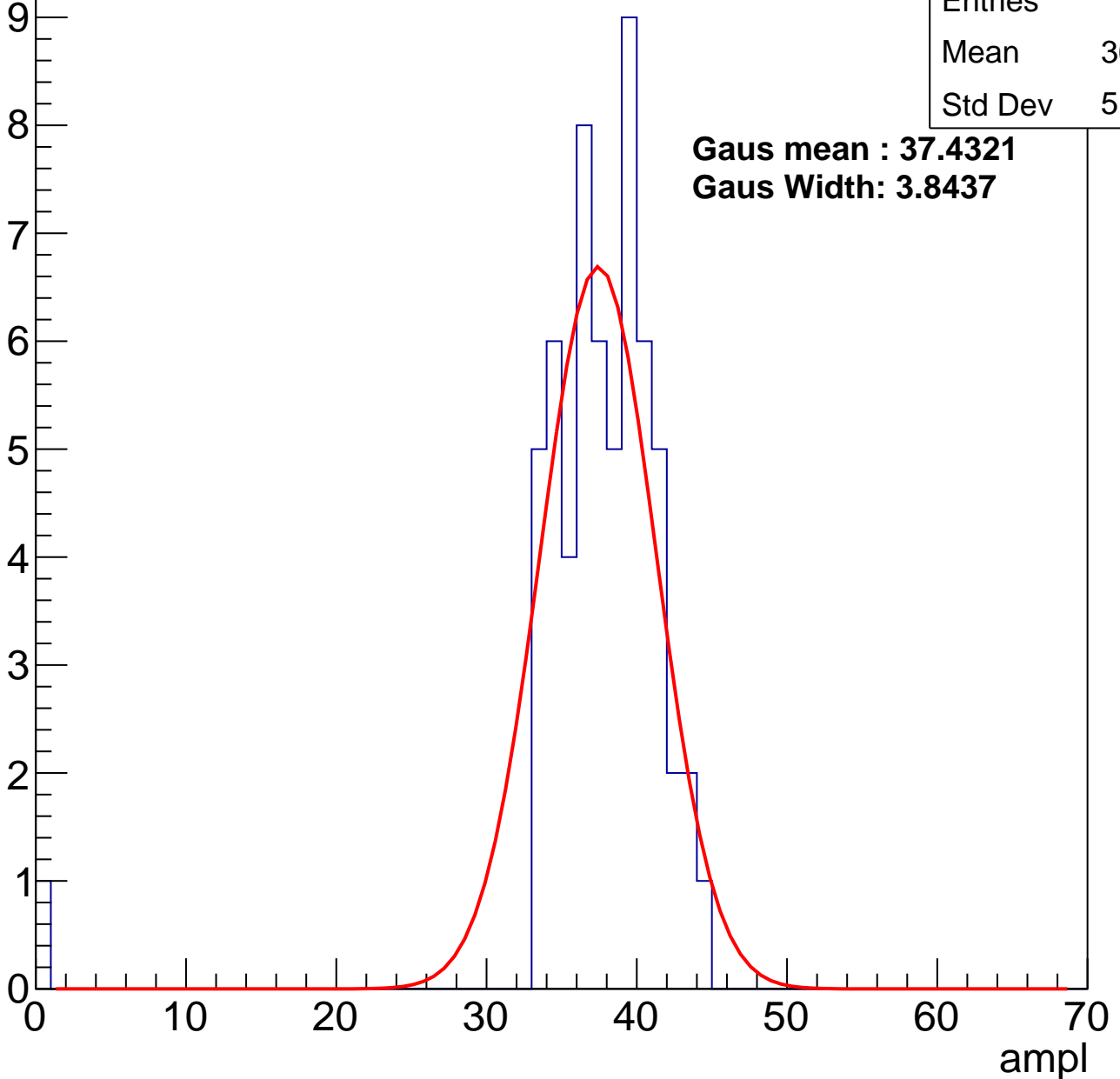
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	36.98
Std Dev	5.587

**Gaus mean : 37.4321**

**Gaus Width: 3.8437**



# B1L101S, U18-ch45, adc2

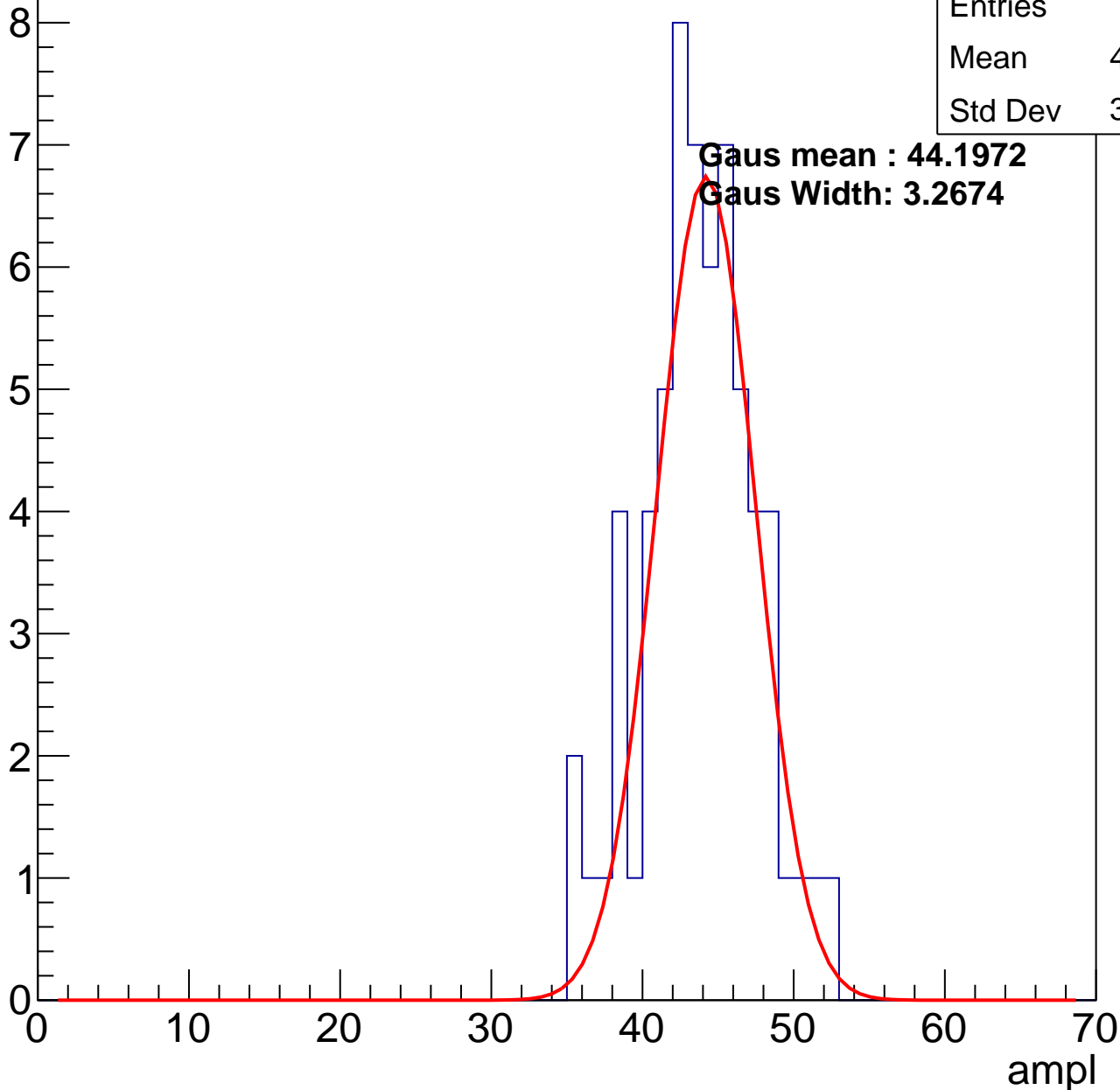
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	43.29
Std Dev	3.697

**Gaus mean : 44.1972**

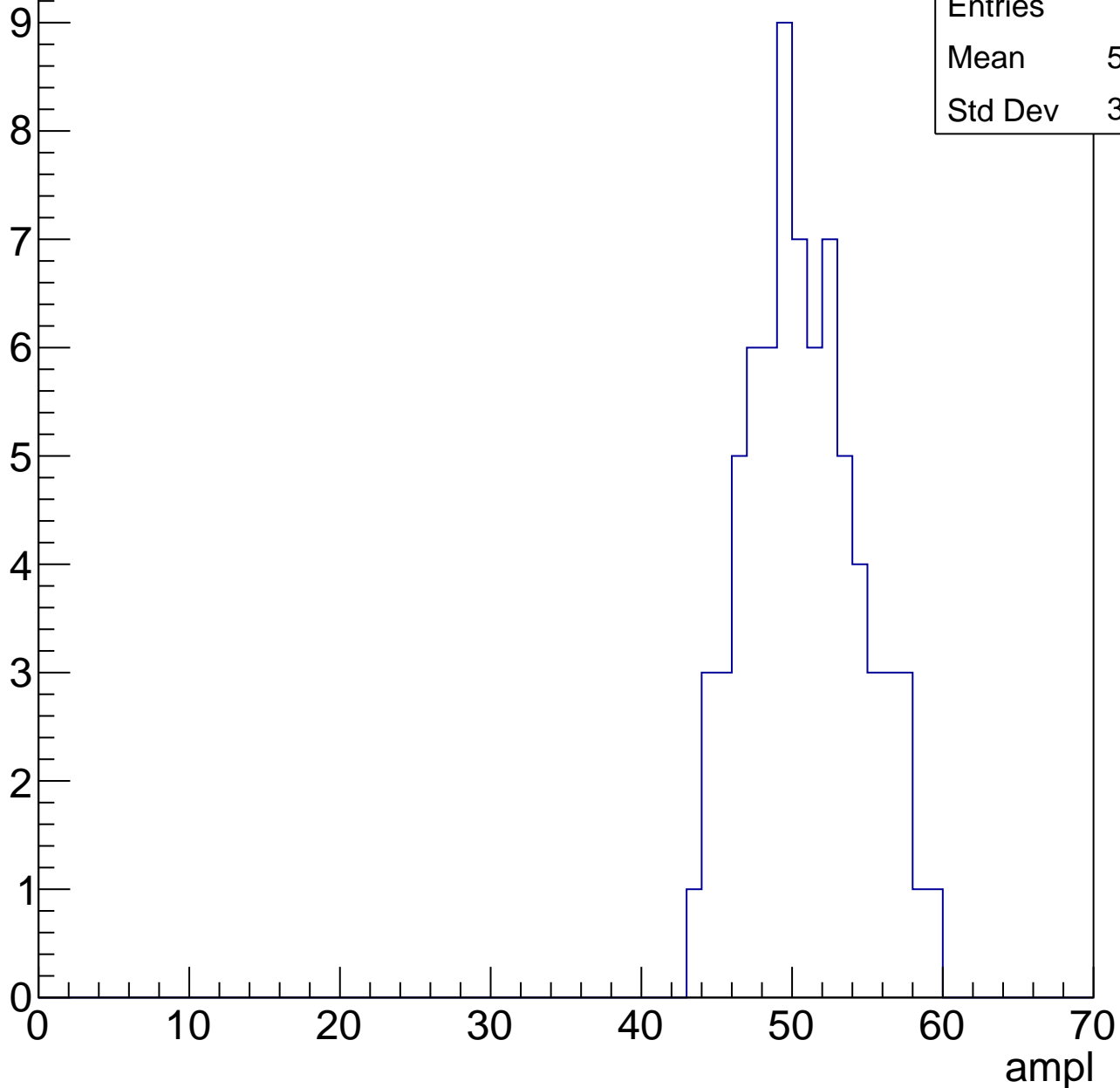
**Gaus Width: 3.2674**



# B1L101S, U18-ch45, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

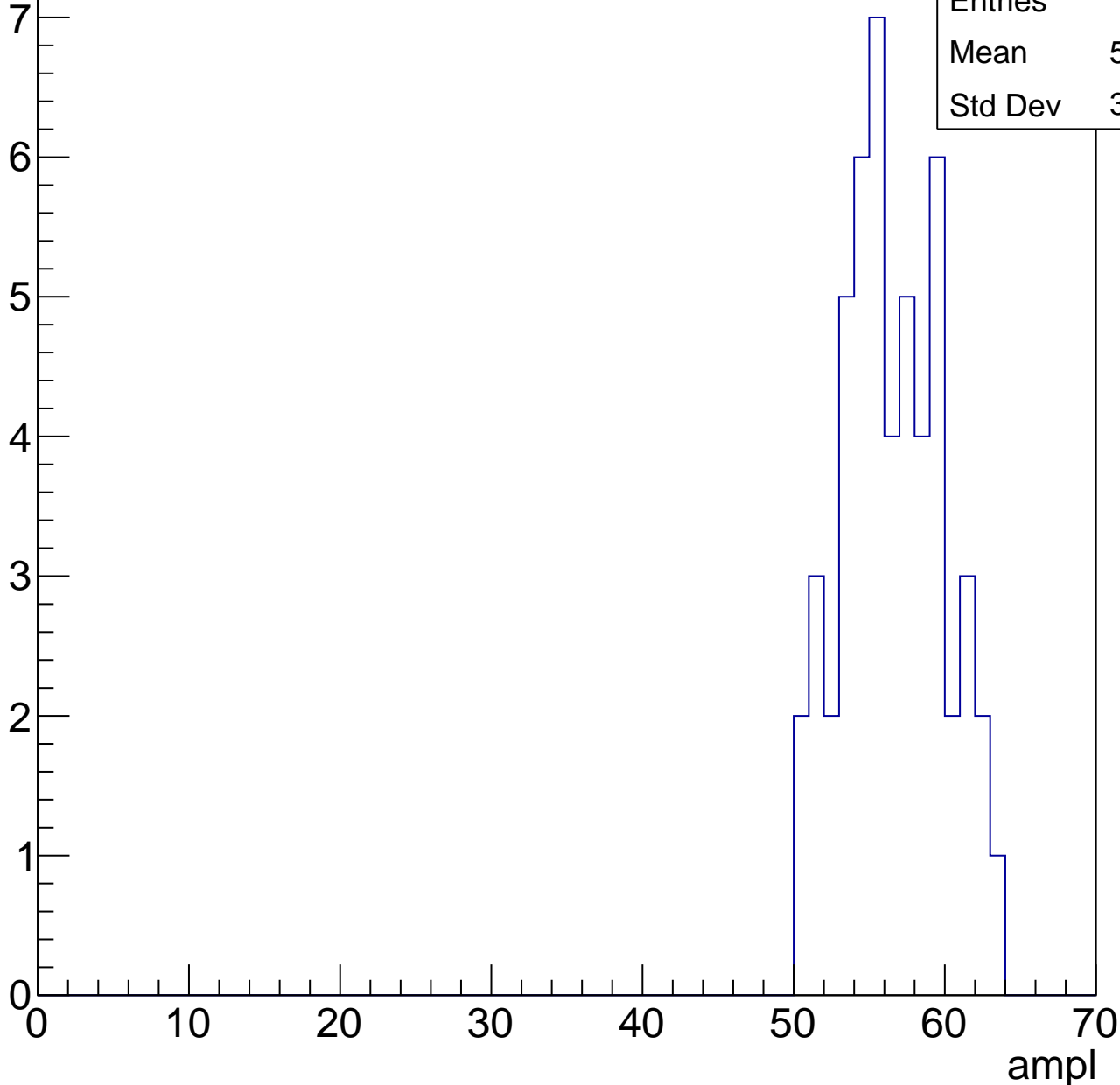


# B1L101S, U18-ch45, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

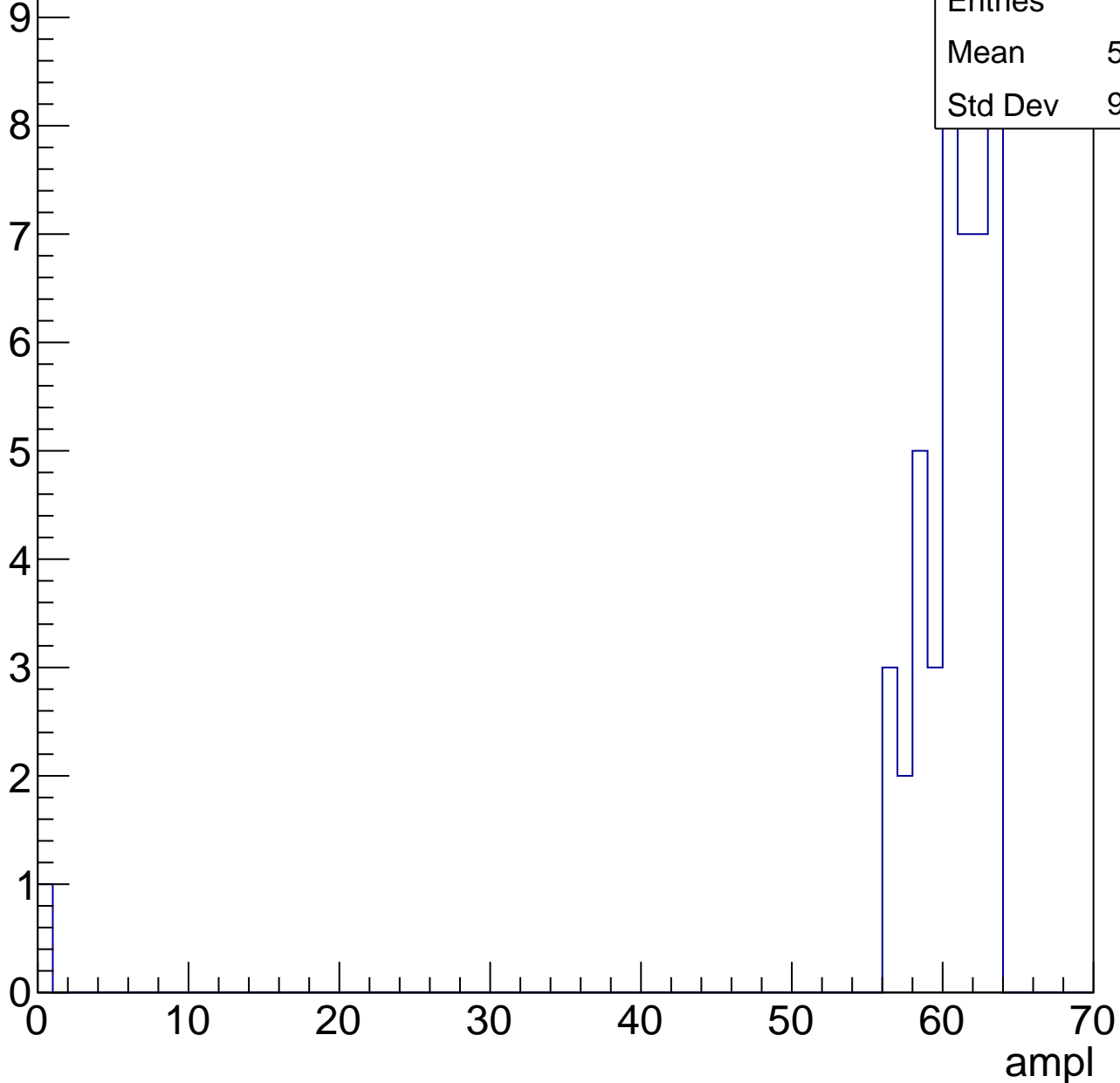
Entries	52
Mean	56.08
Std Dev	3.275



# B1L101S, U18-ch45, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch45, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch45, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch46, adc0

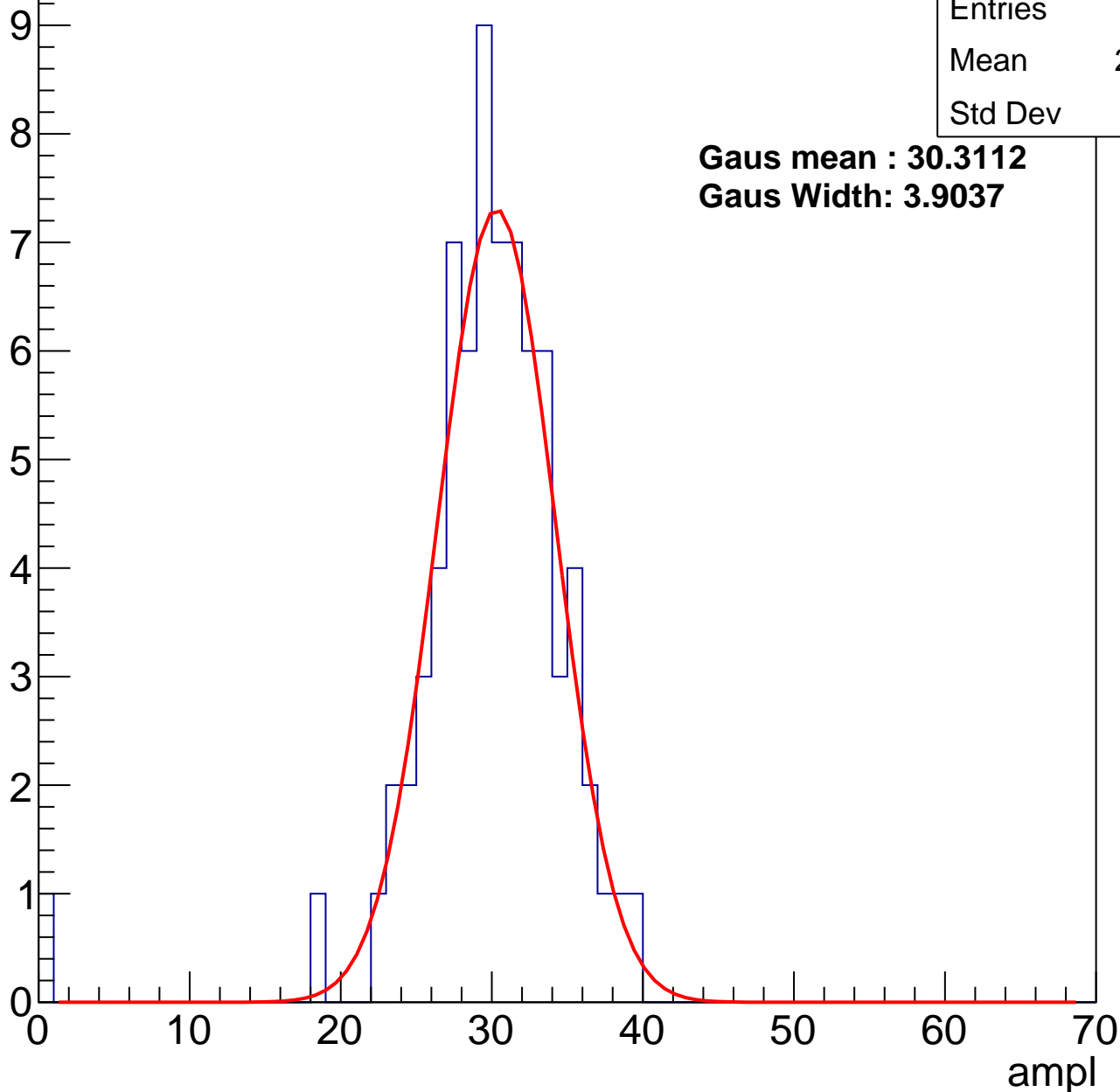
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	29.41
Std Dev	5.18

**Gaus mean : 30.3112**

**Gaus Width: 3.9037**



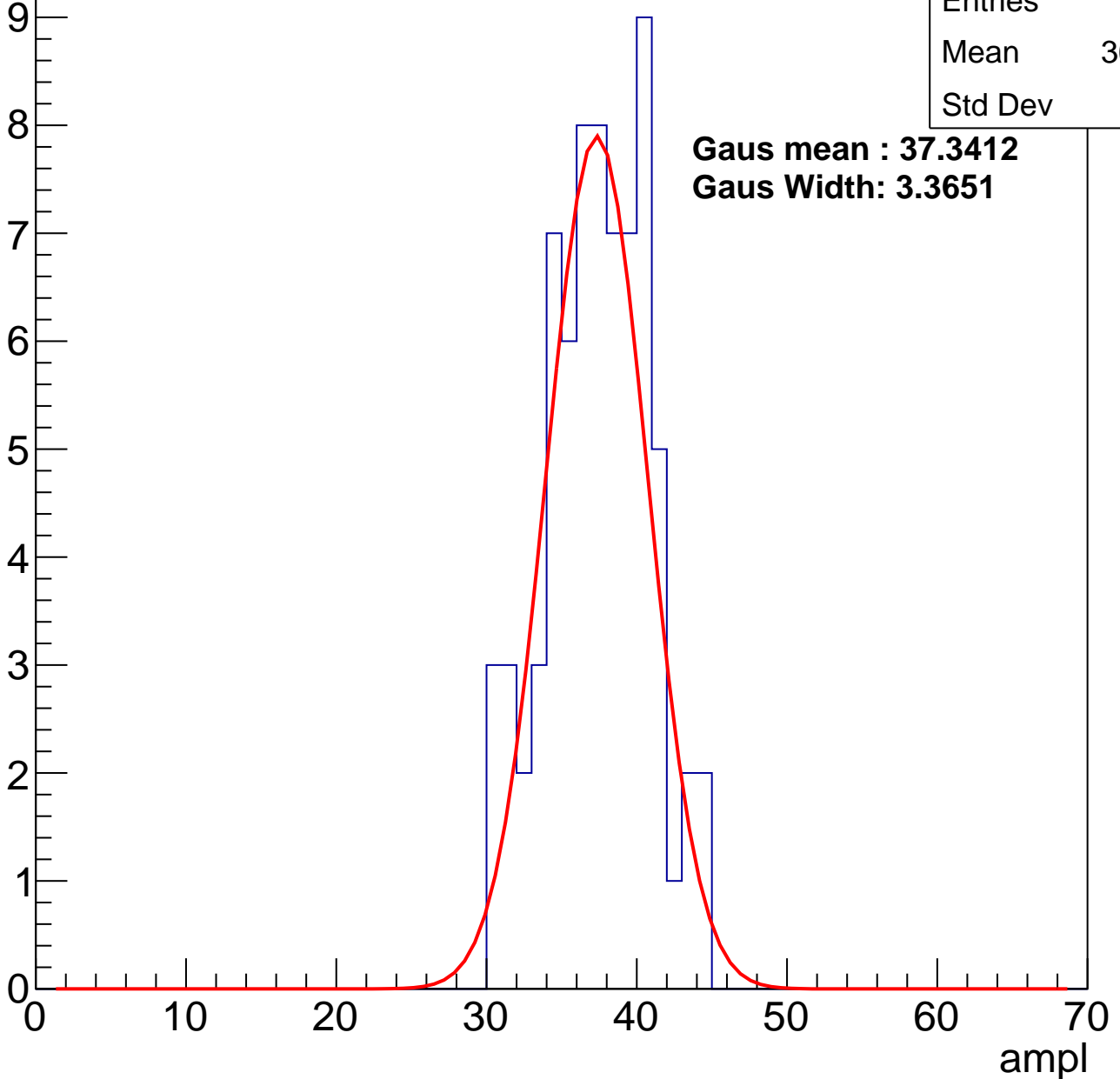
# B1L101S, U18-ch46, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	36.96
Std Dev	3.39

**Gaus mean : 37.3412**  
**Gaus Width: 3.3651**

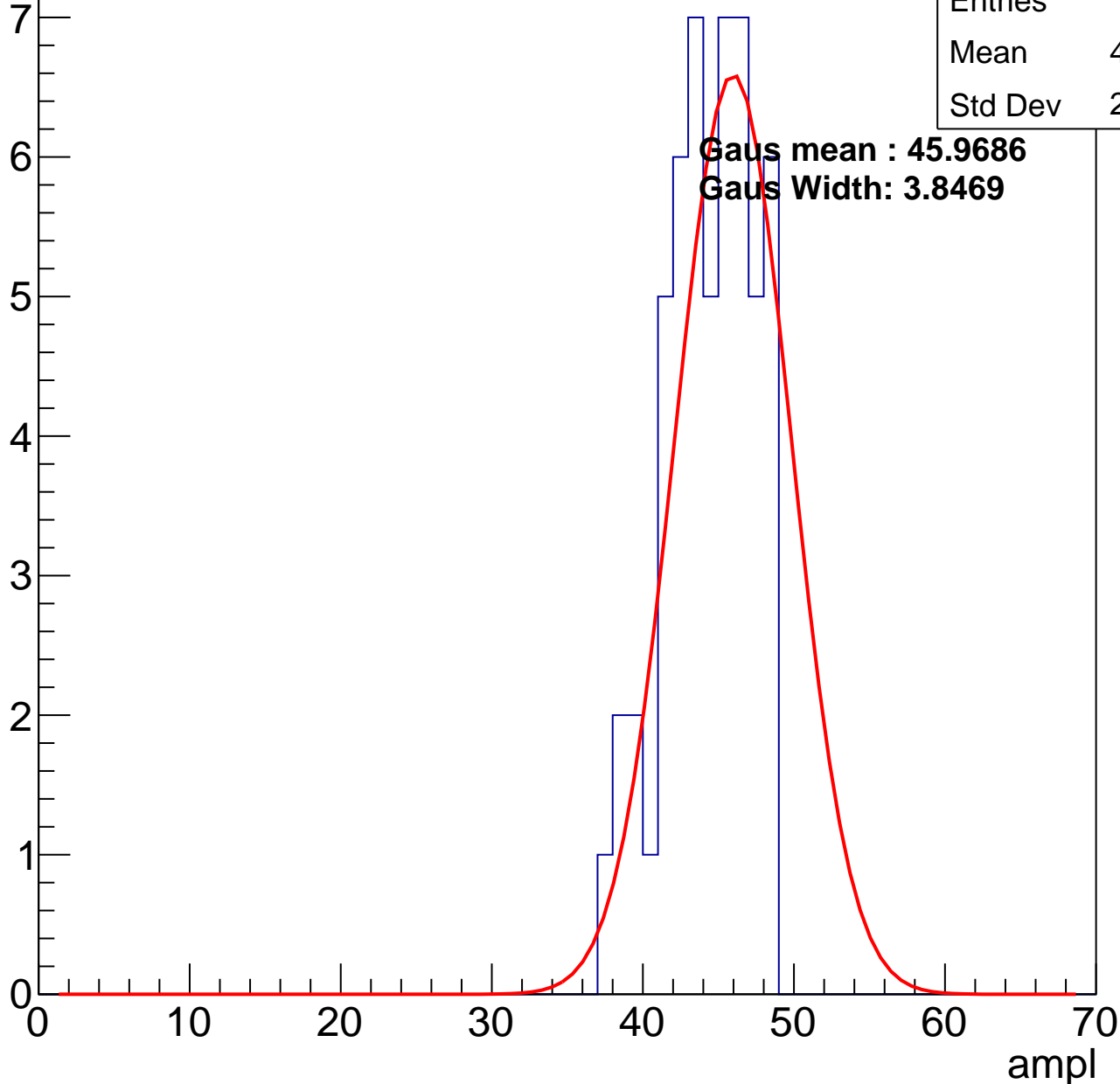


# B1L101S, U18-ch46, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	43.87
Std Dev	2.848



# B1L101S, U18-ch46, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

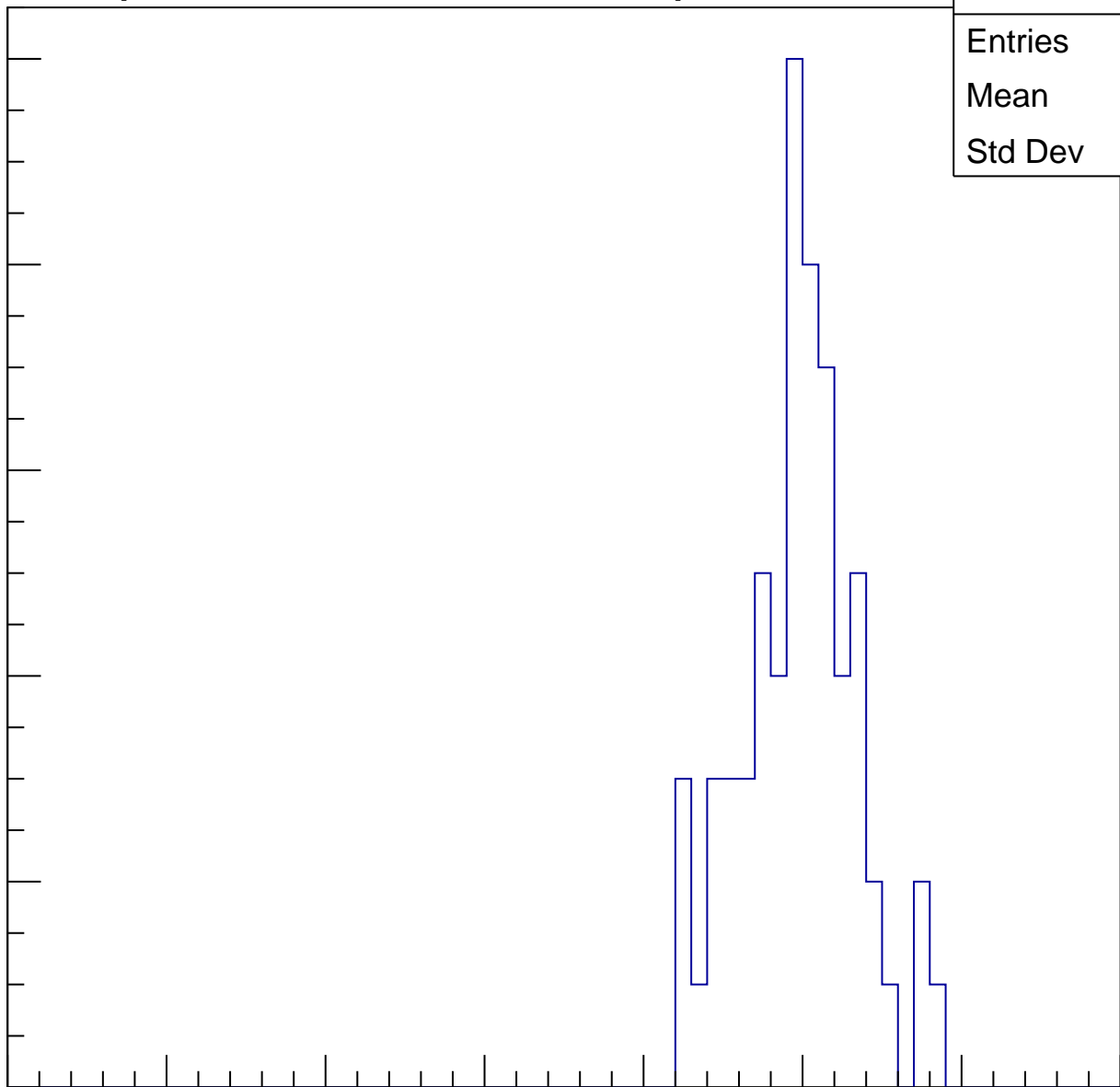
Entries	62
Mean	49.29
Std Dev	3.589

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

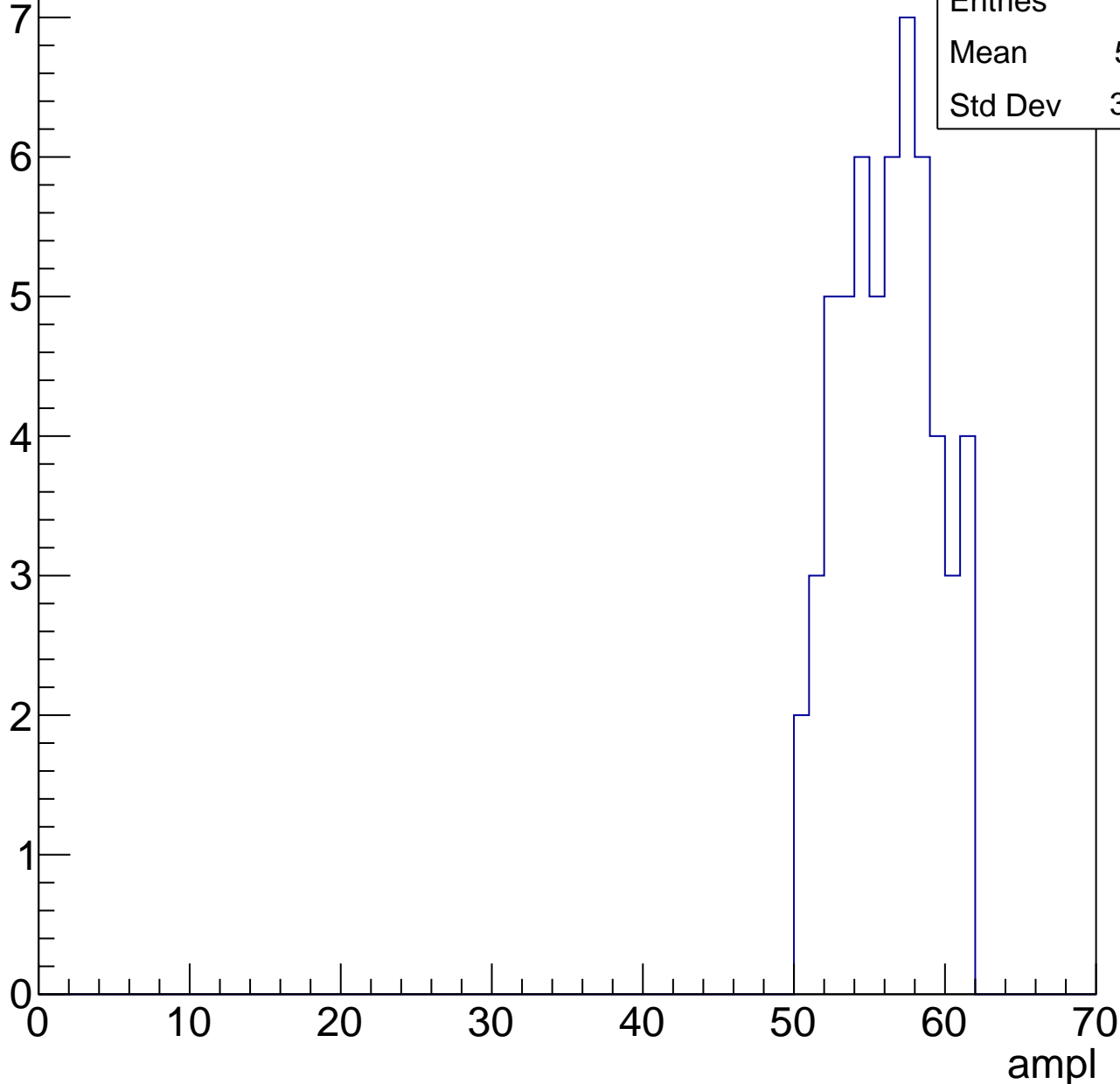
ampl



# B1L101S, U18-ch46, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

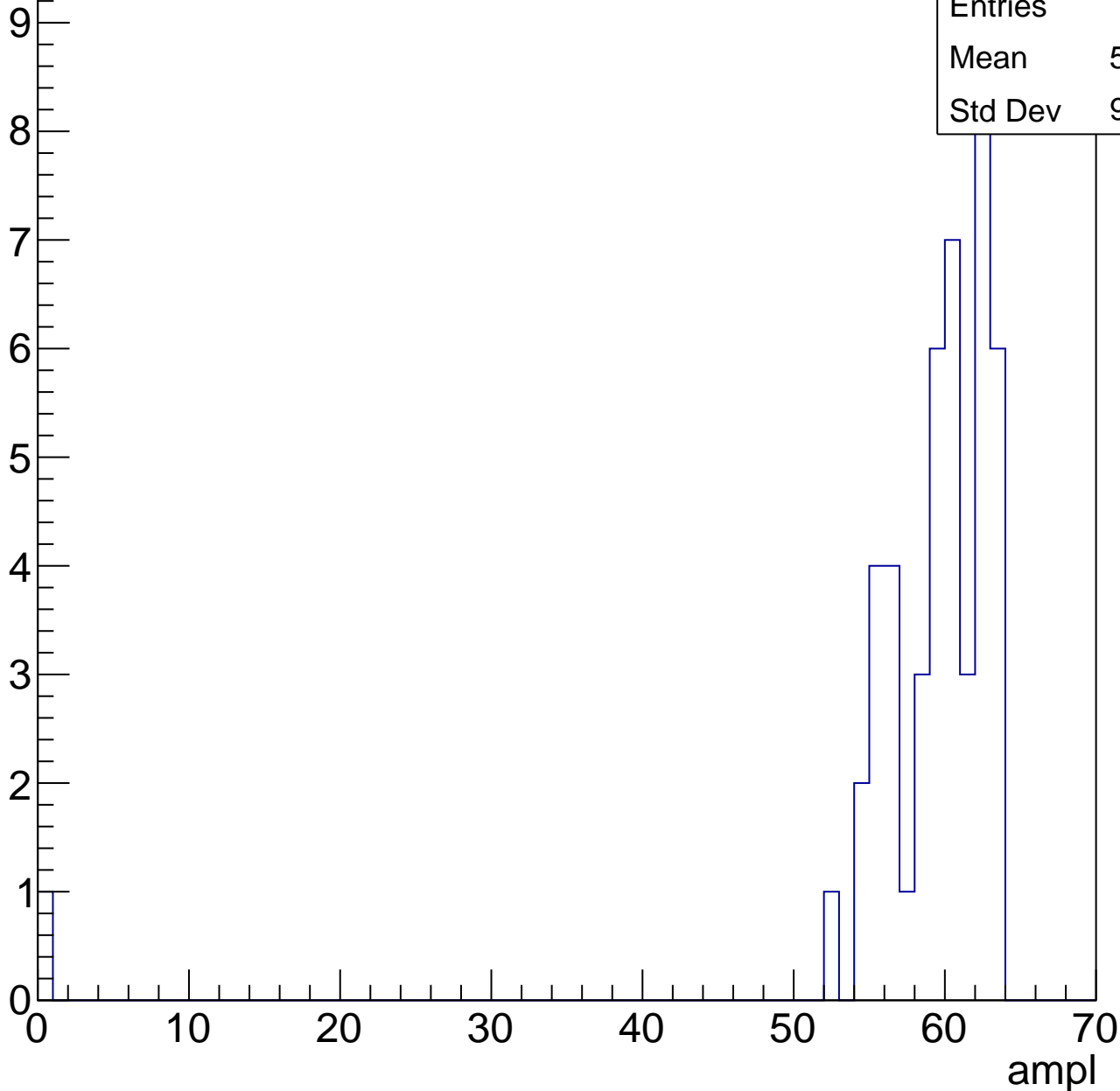


# B1L101S, U18-ch46, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

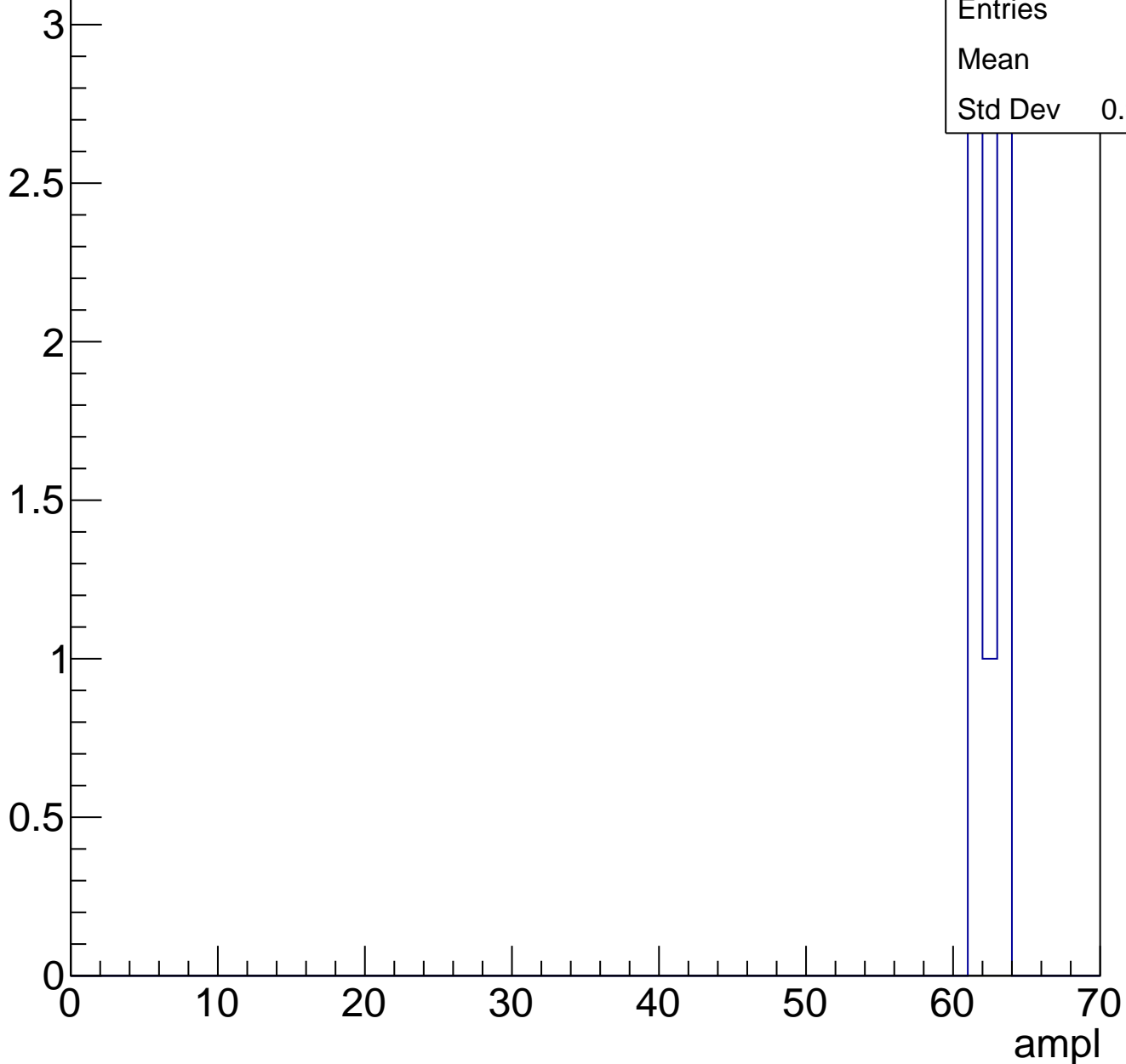
Entries	47
Mean	58.04
Std Dev	9.039



# B1L101S, U18-ch46, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch46, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch47, adc0

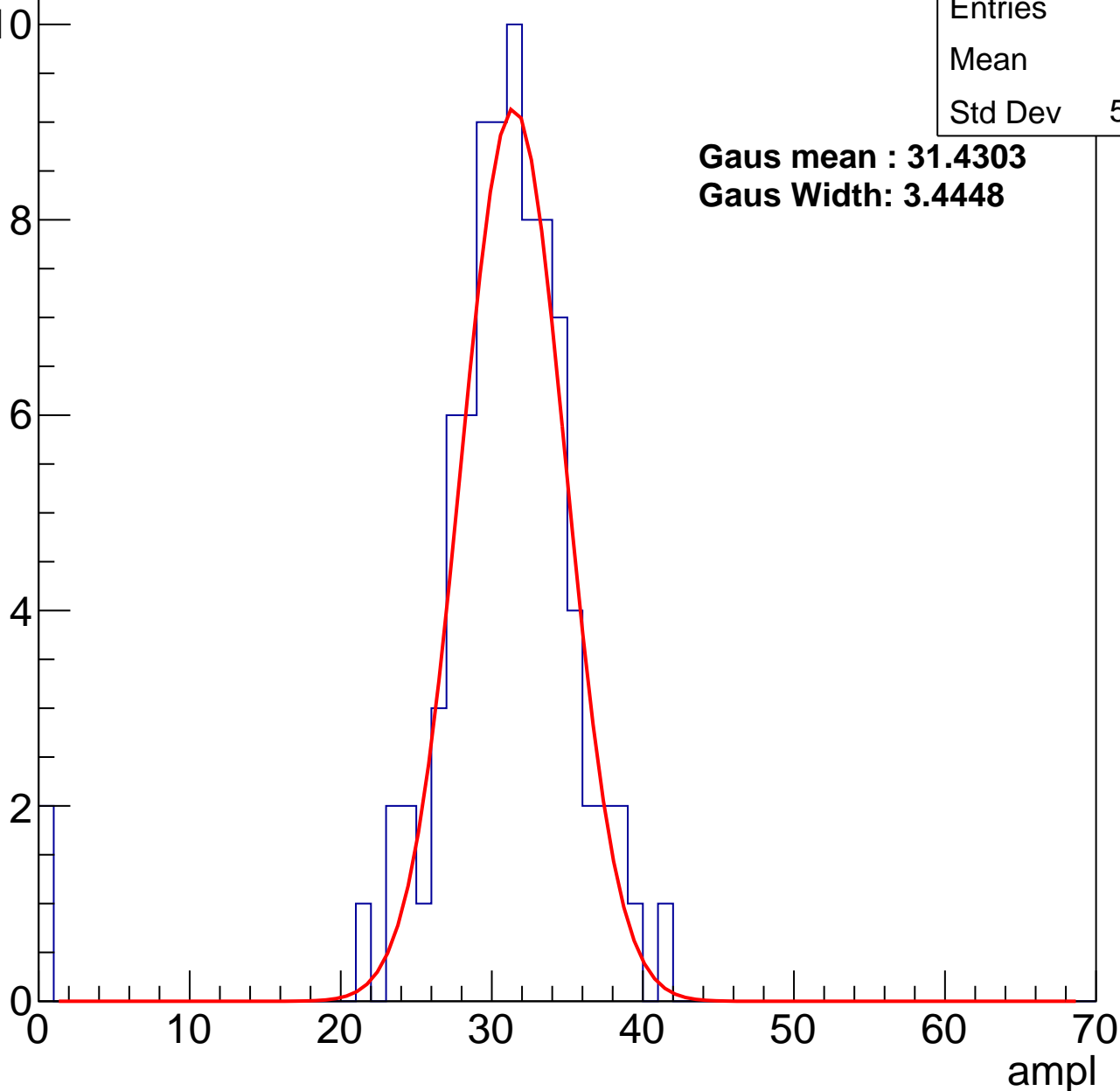
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	86
Mean	30.1
Std Dev	5.942

**Gaus mean : 31.4303**

**Gaus Width: 3.4448**



# B1L101S, U18-ch47, adc1

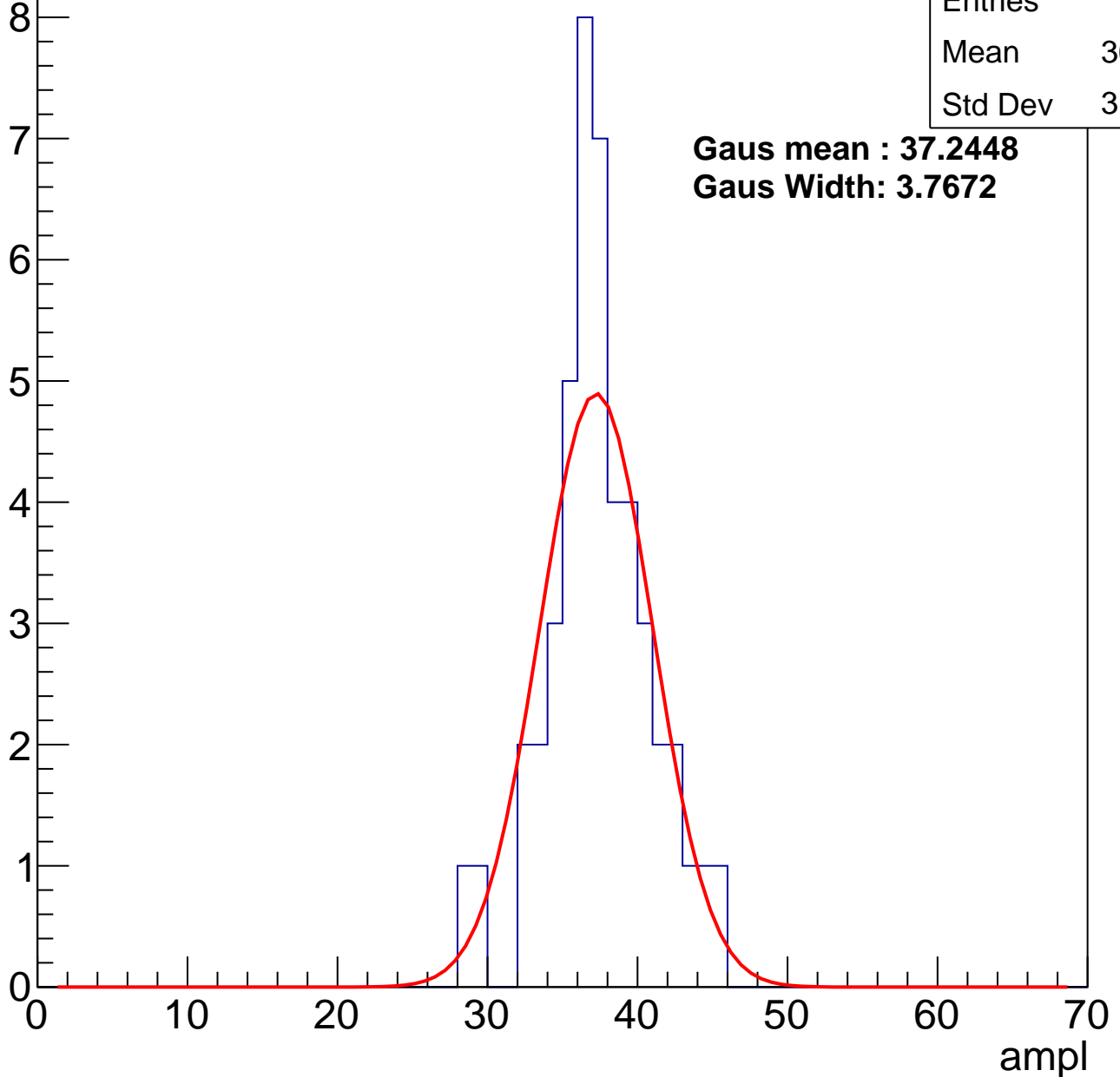
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	47
Mean	36.96
Std Dev	3.452

**Gaus mean : 37.2448**

**Gaus Width: 3.7672**



# B1L101S, U18-ch47, adc2

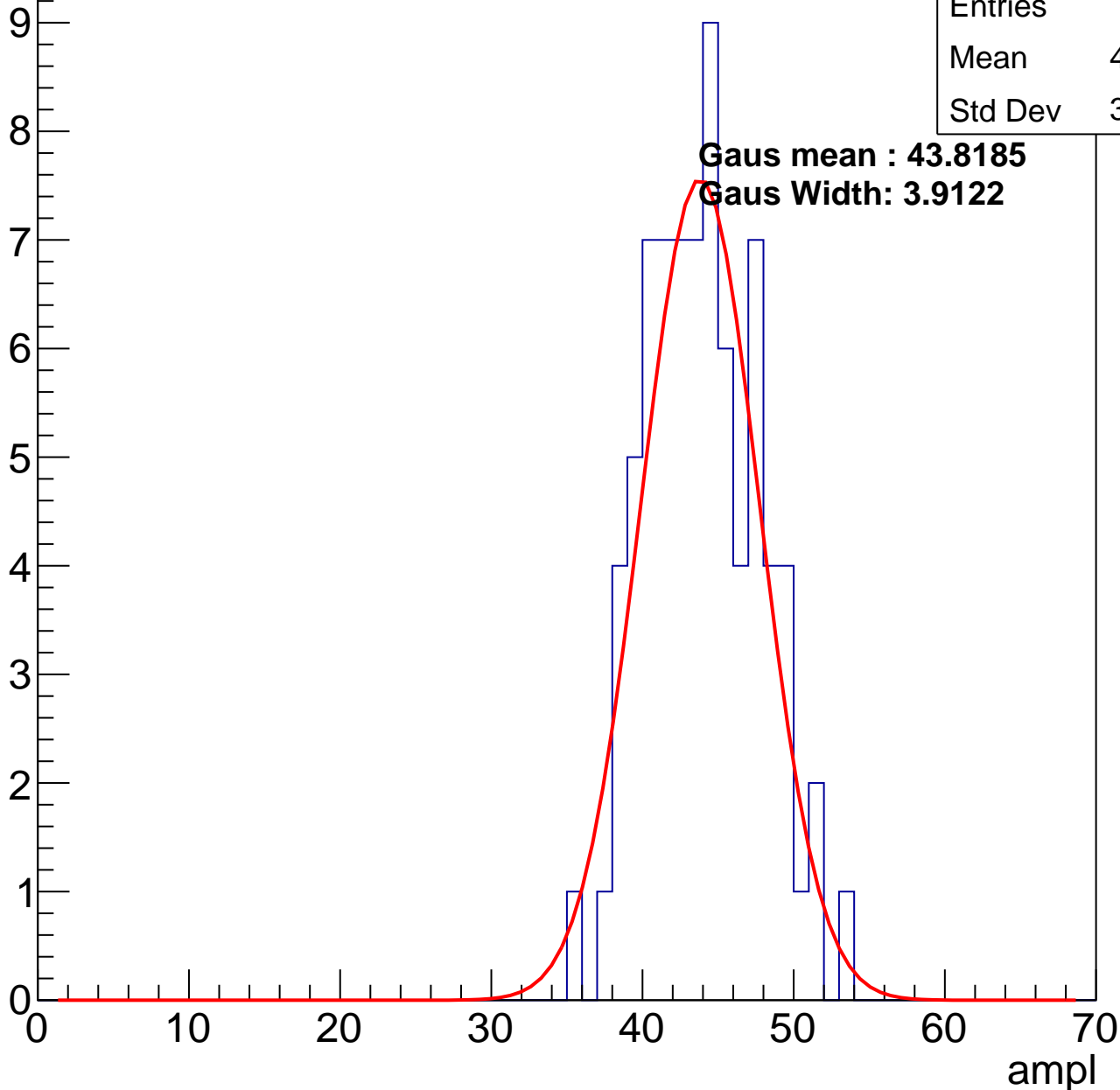
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	43.55
Std Dev	3.705

**Gaus mean : 43.8185**

**Gaus Width: 3.9122**

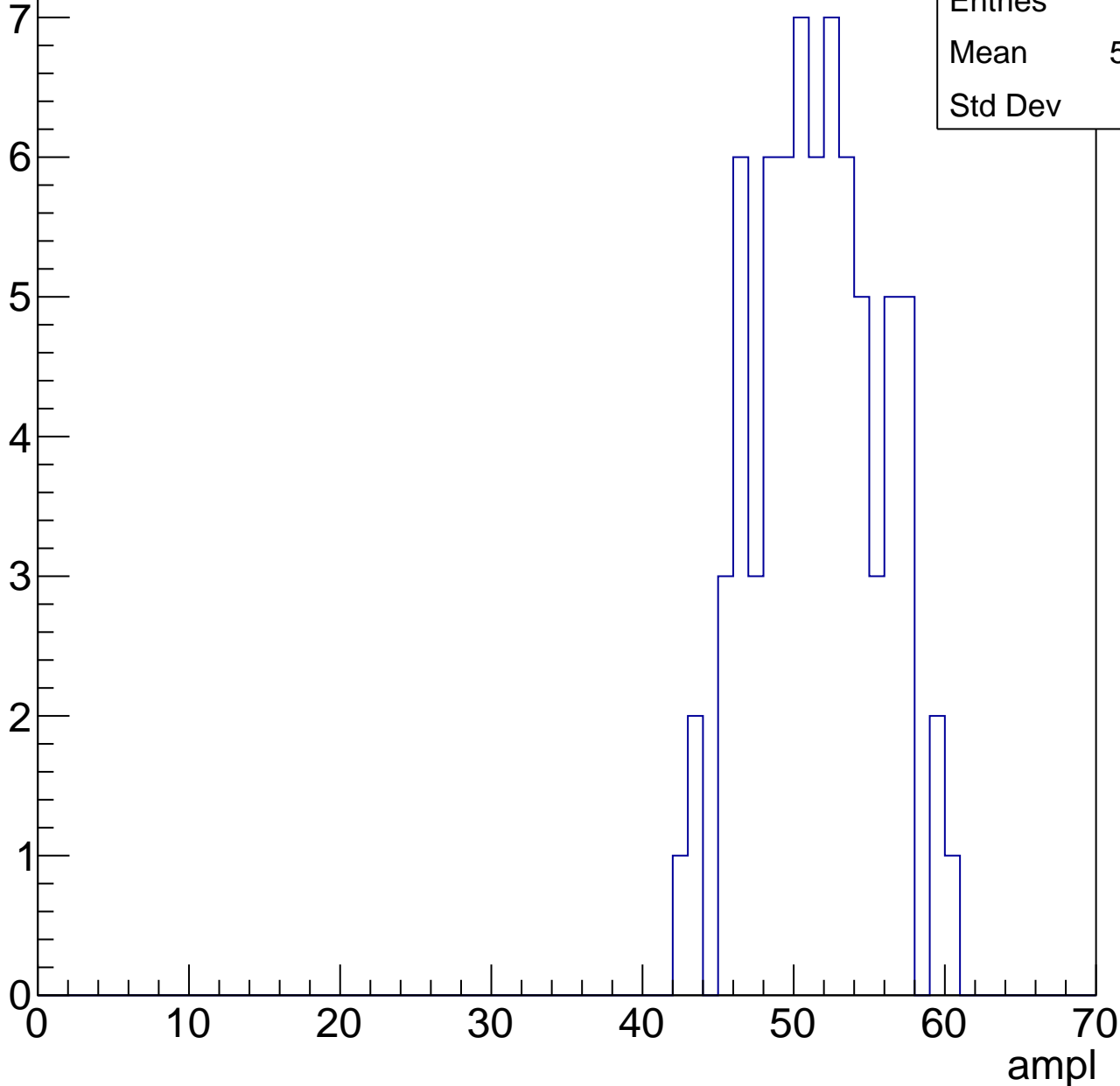


# B1L101S, U18-ch47, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

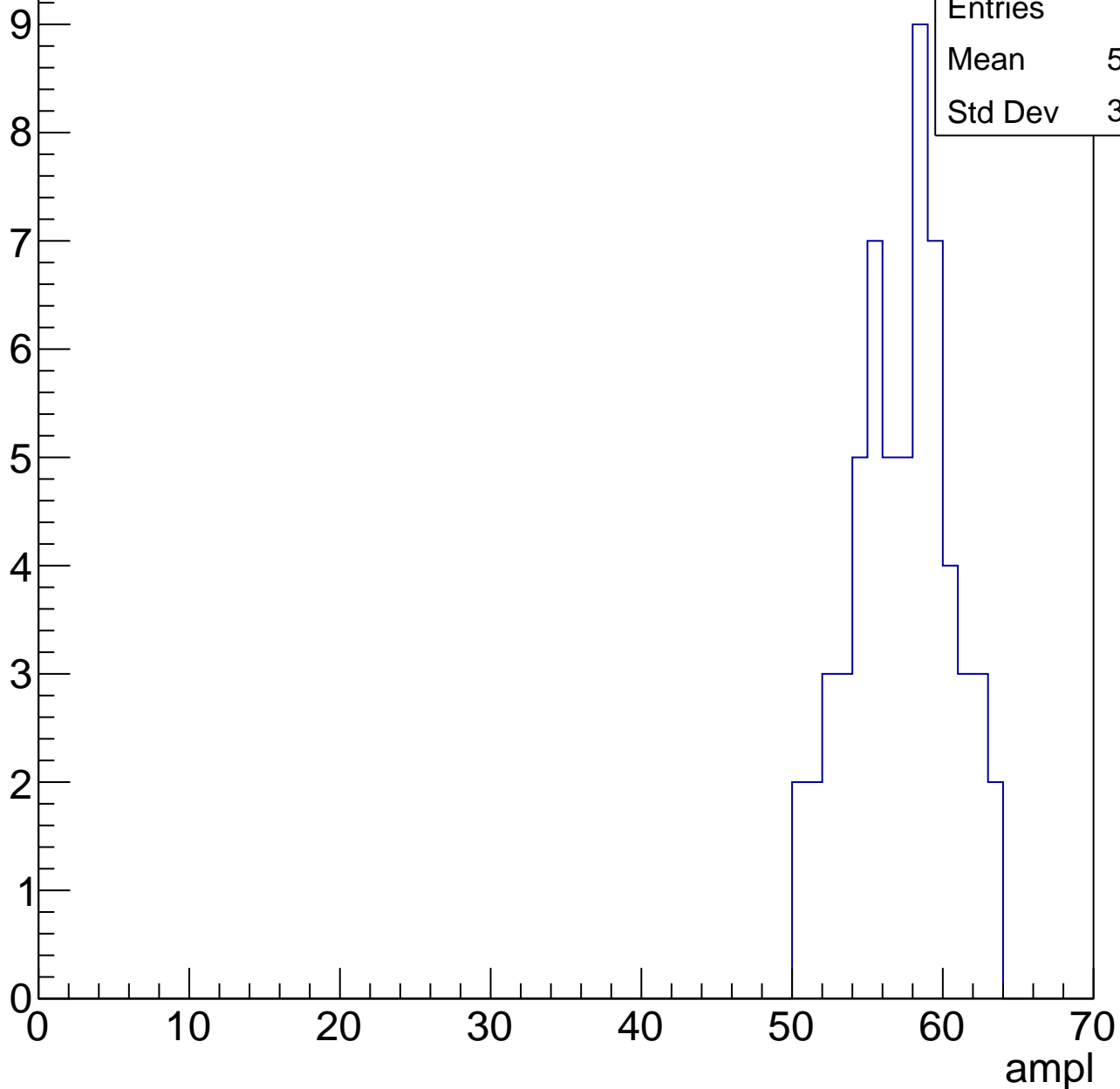
Entries	74
Mean	51.05
Std Dev	4.09



# B1L101S, U18-ch47, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch47, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

7

6

5

4

3

2

1

0

Entries 25

Mean 61.32

Std Dev 1.378

0

10

20

30

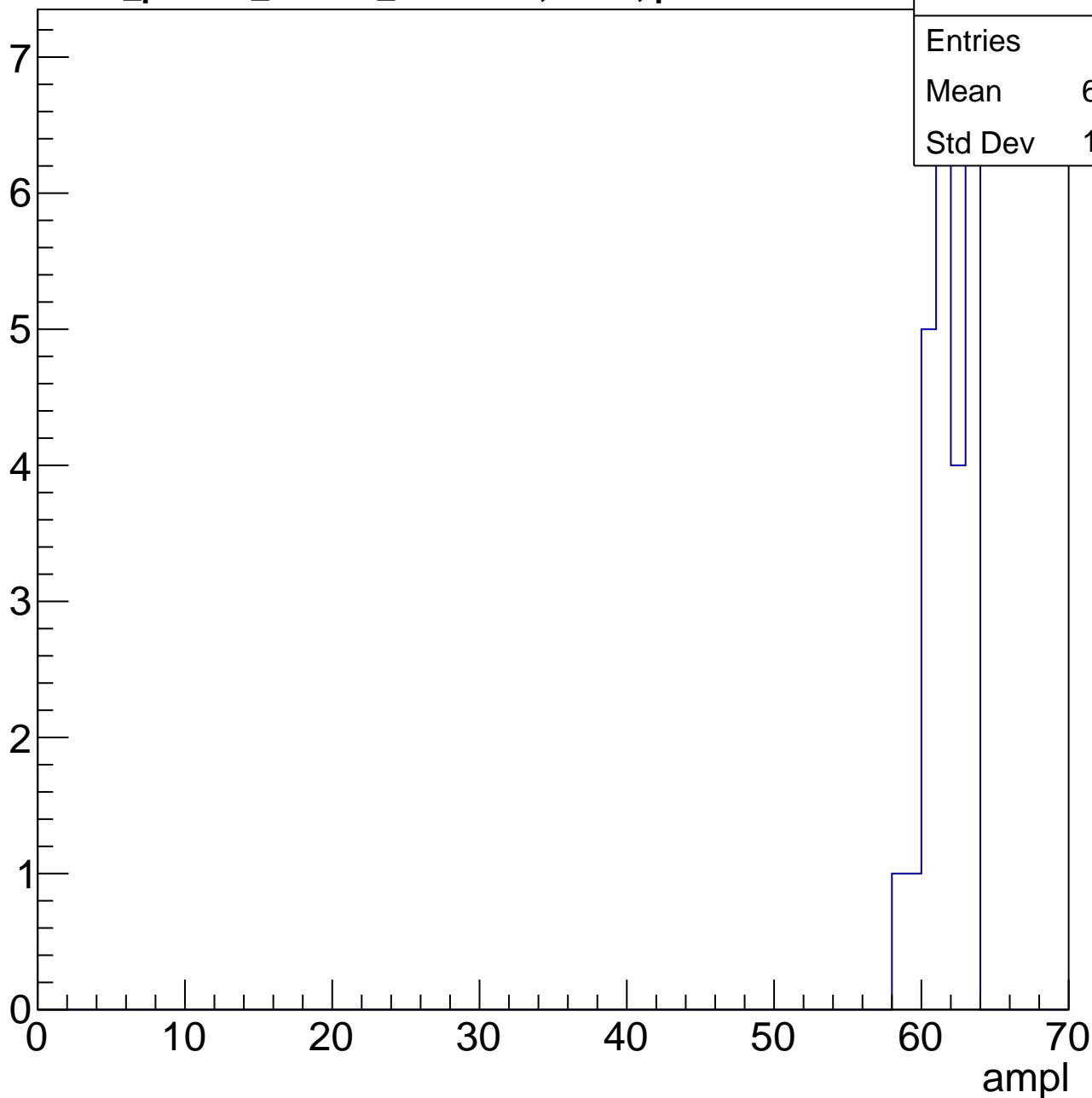
40

50

60

70

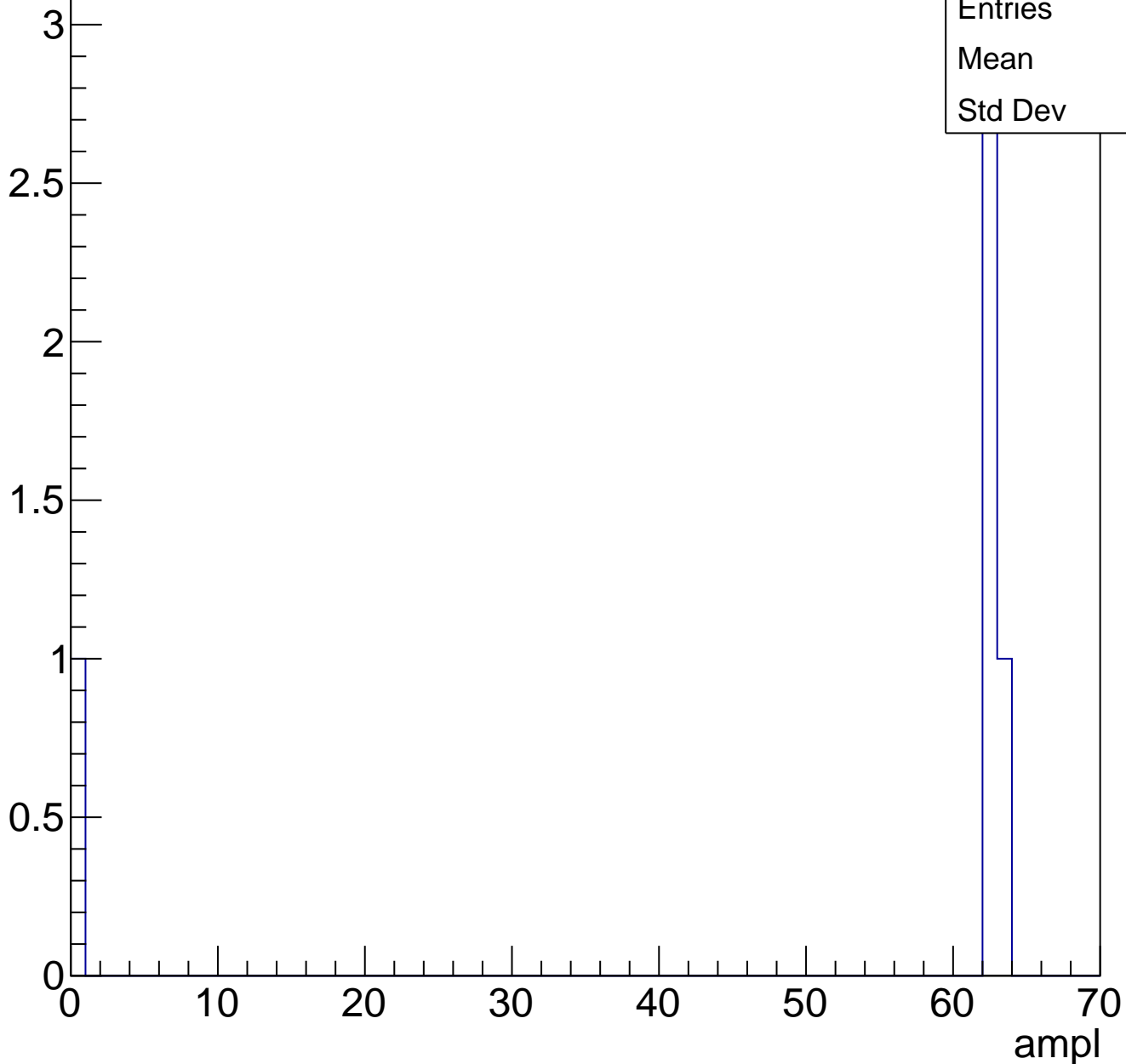
ampl



# B1L101S, U18-ch47, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch47, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U18-ch48, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	82
Mean	29.5
Std Dev	3.936

**Gaus mean : 29.8259**

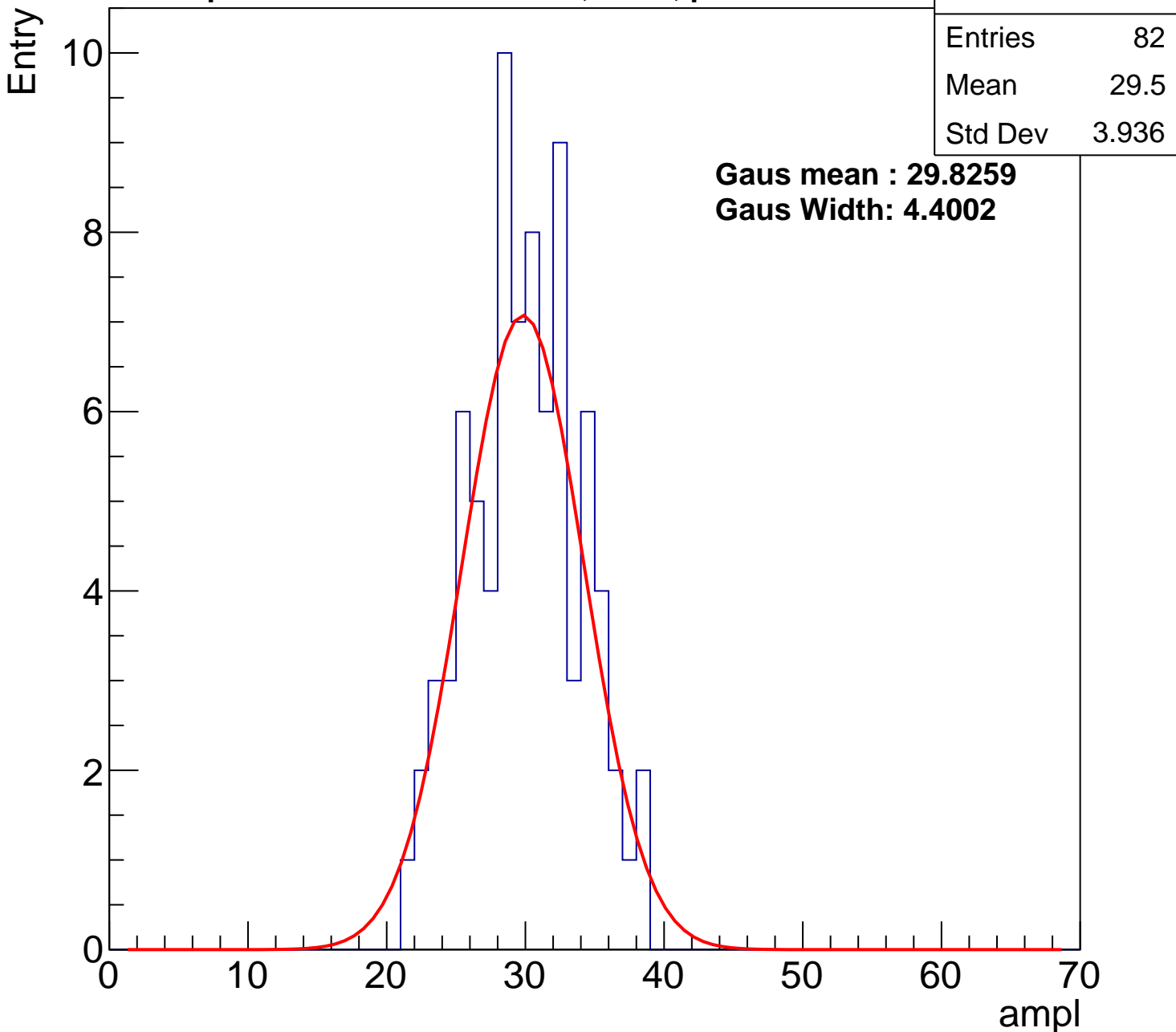
**Gaus Width: 4.4002**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U18-ch48, adc1

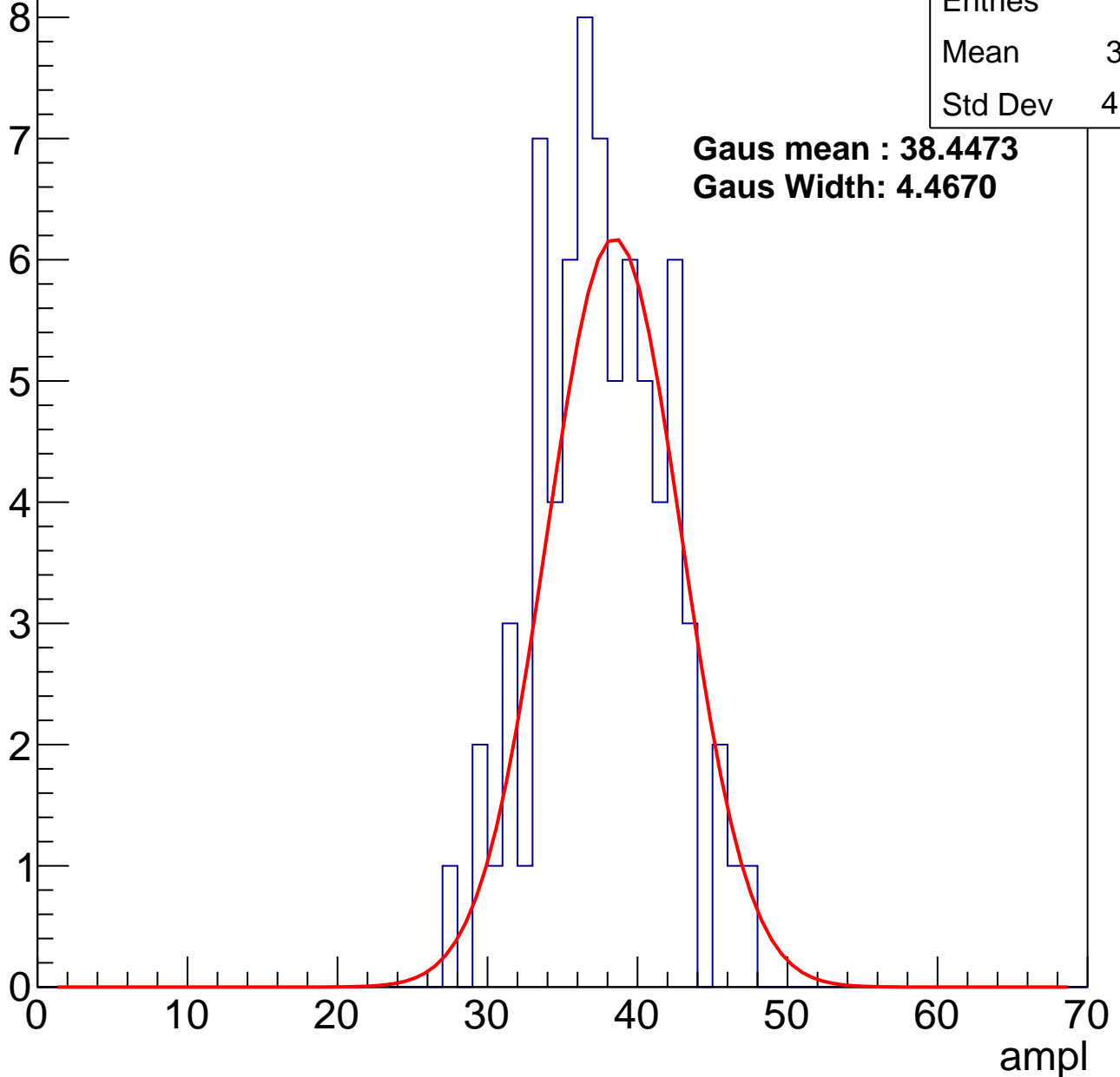
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	37.21
Std Dev	4.207

**Gaus mean : 38.4473**

**Gaus Width: 4.4670**



# B1L101S, U18-ch48, adc2

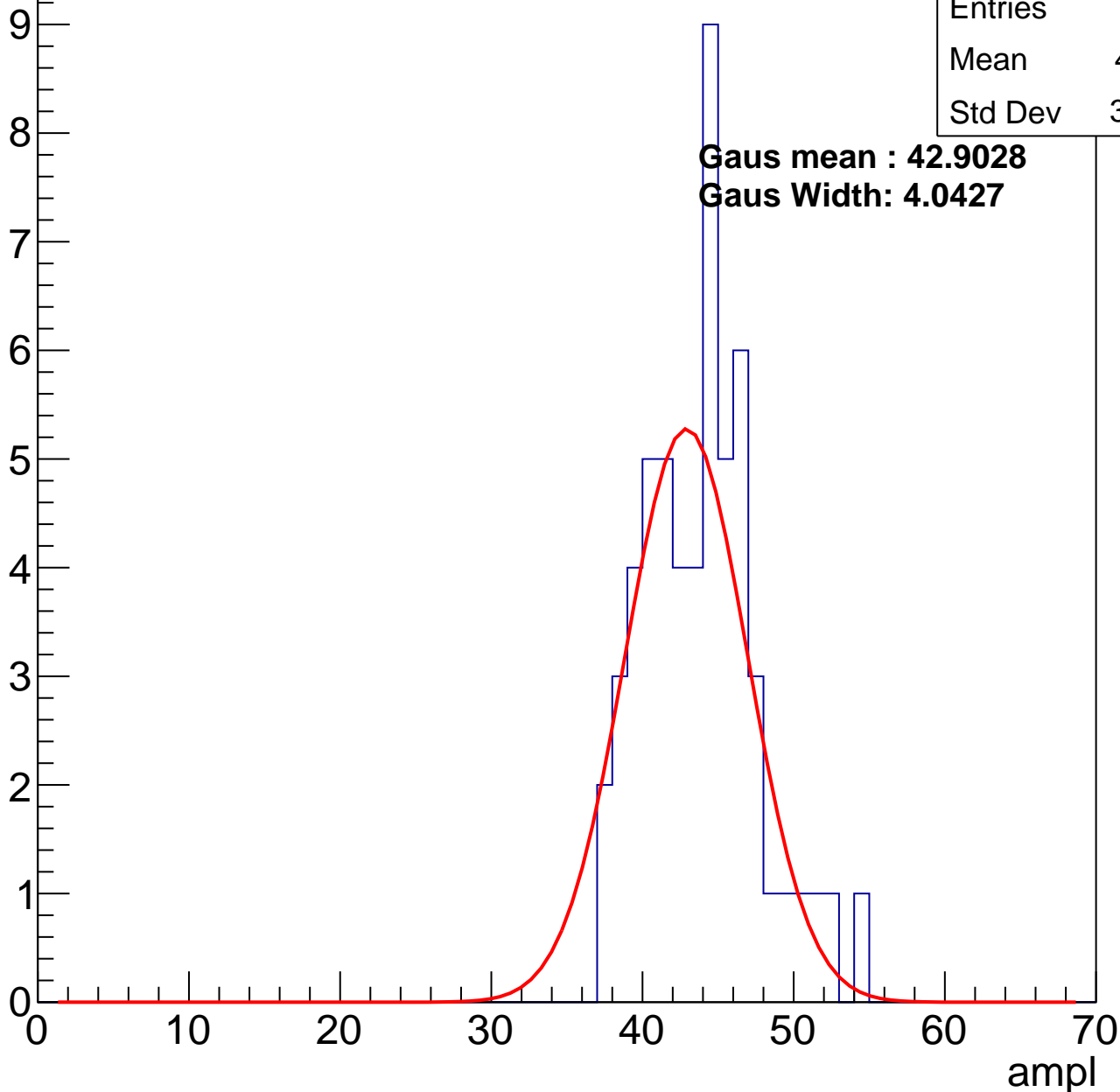
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	43.41
Std Dev	3.726

**Gaus mean : 42.9028**

**Gaus Width: 4.0427**

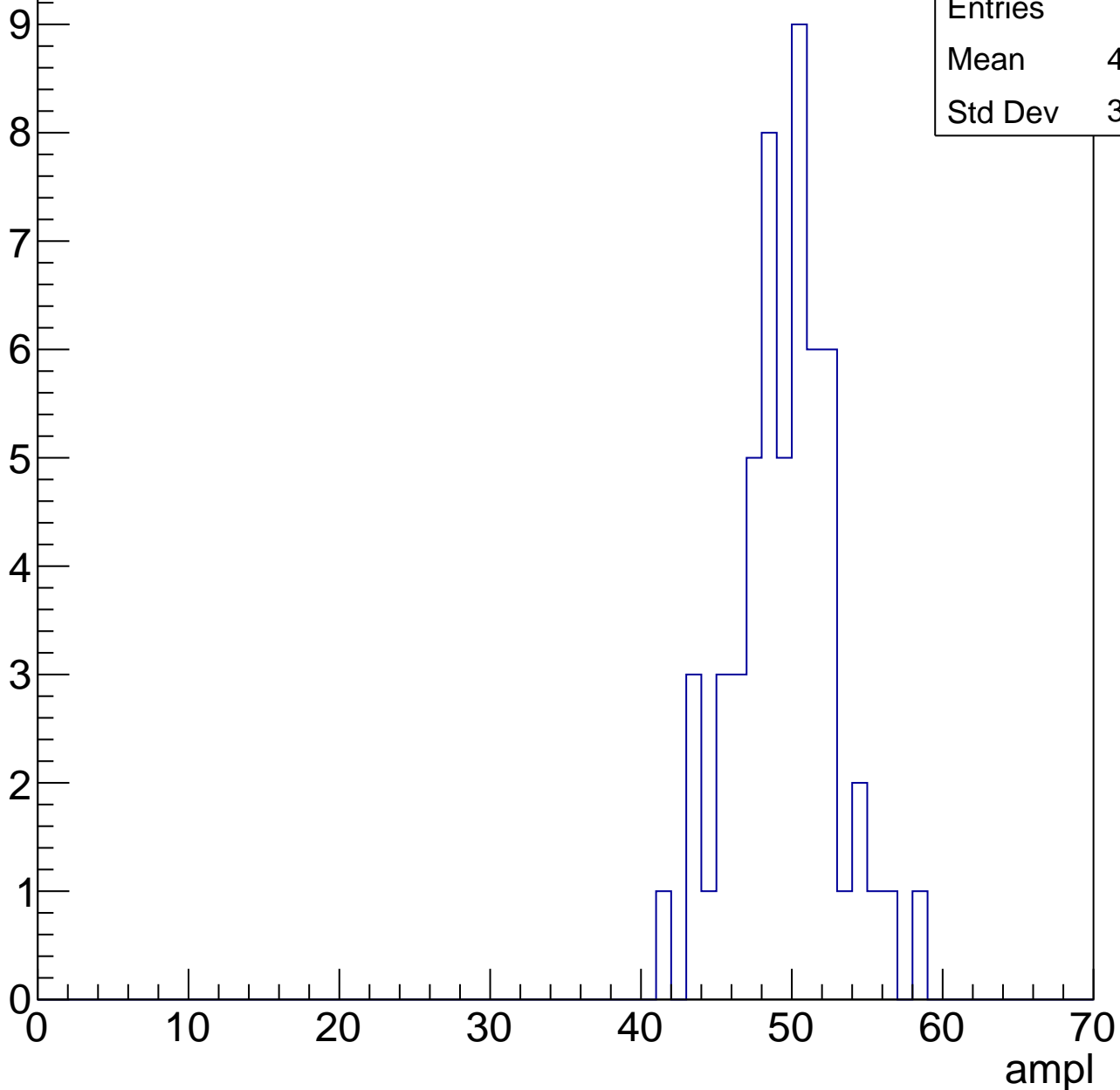


# B1L101S, U18-ch48, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	49.09
Std Dev	3.323

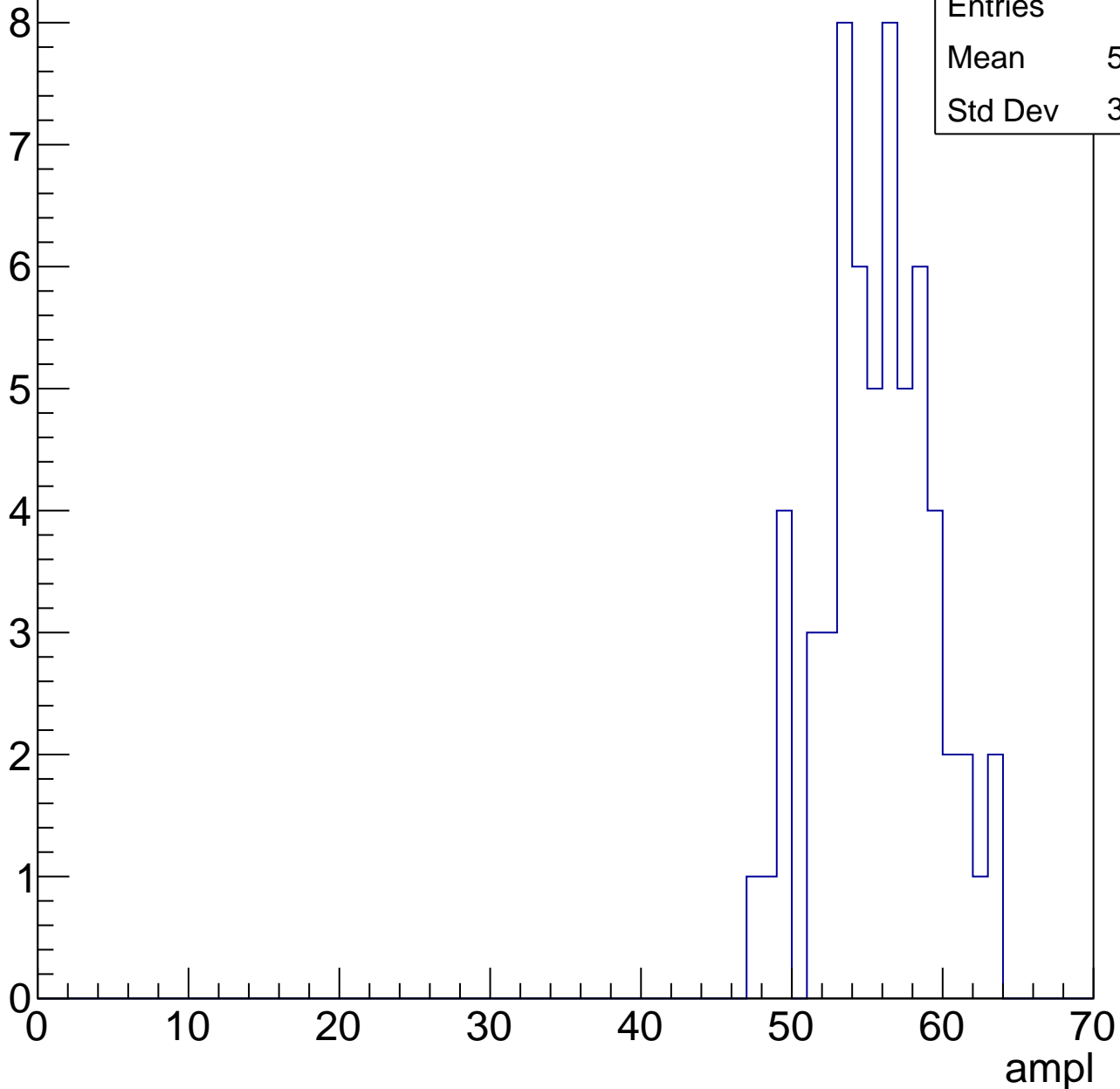


# B1L101S, U18-ch48, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	55.25
Std Dev	3.647

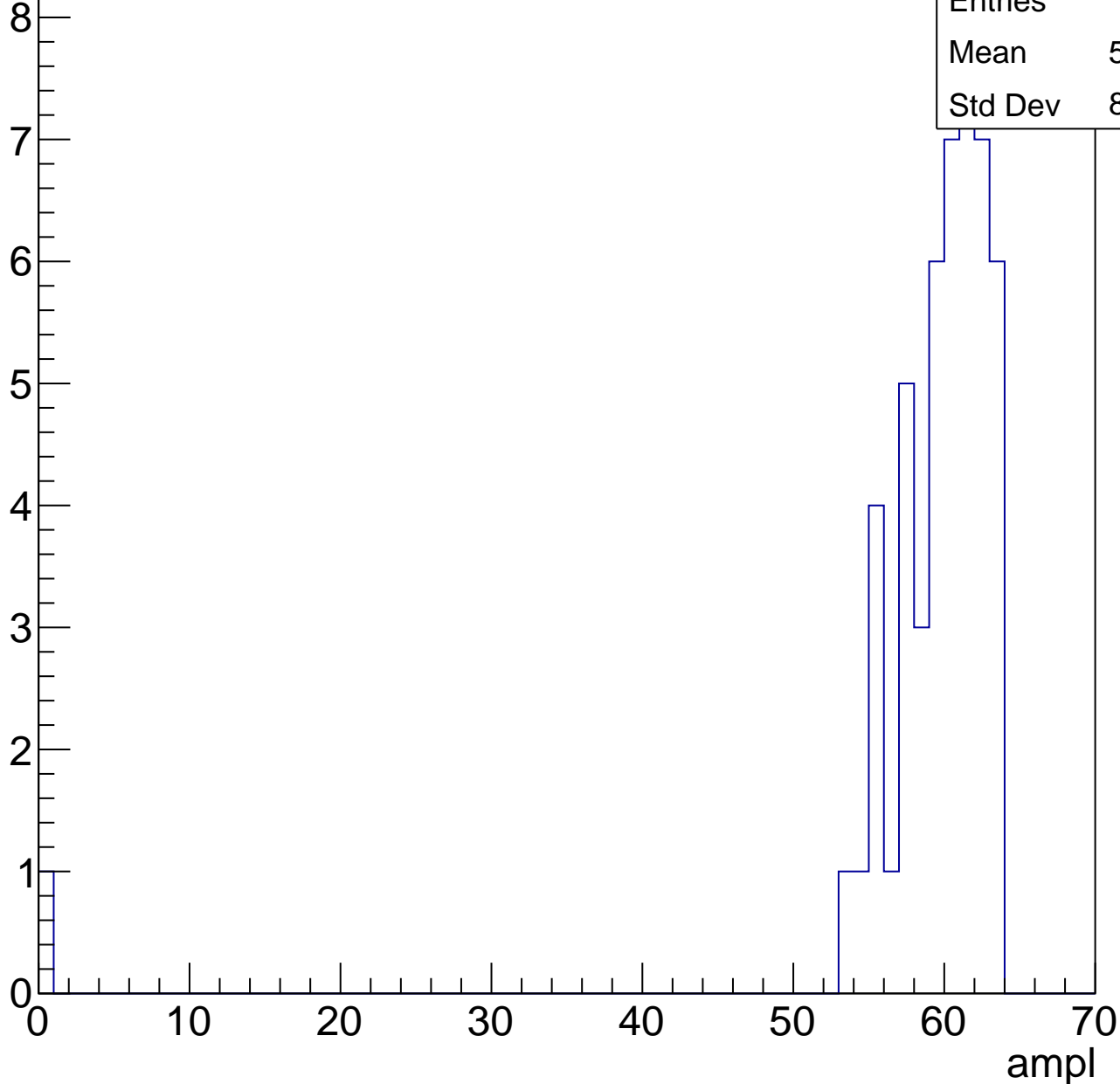


# B1L101S, U18-ch48, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	58.32
Std Dev	8.733



# B1L101S, U18-ch48, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch48, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U18-ch49, adc0

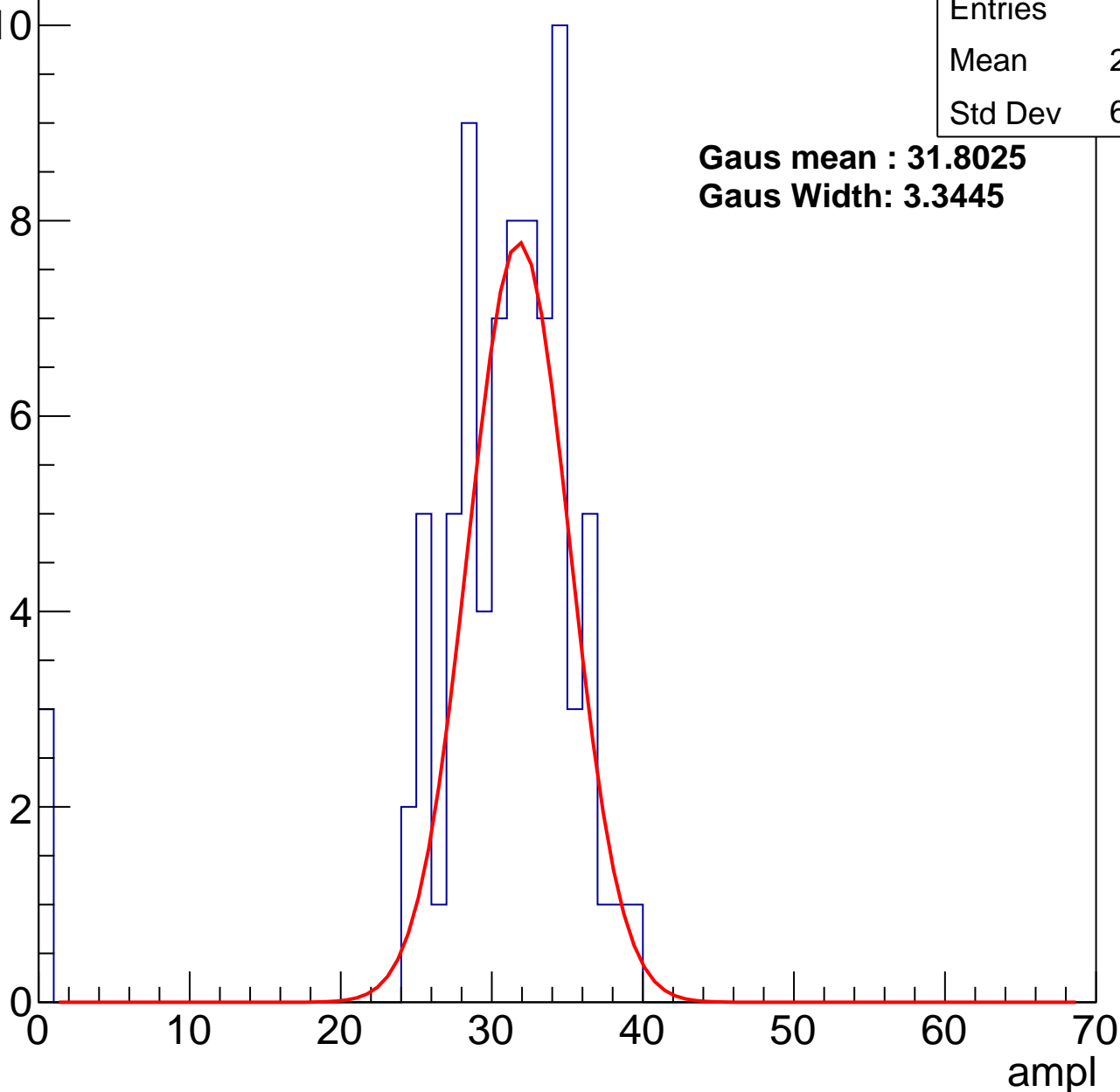
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	80
Mean	29.82
Std Dev	6.808

**Gaus mean : 31.8025**

**Gaus Width: 3.3445**



# B1L101S, U18-ch49, adc1

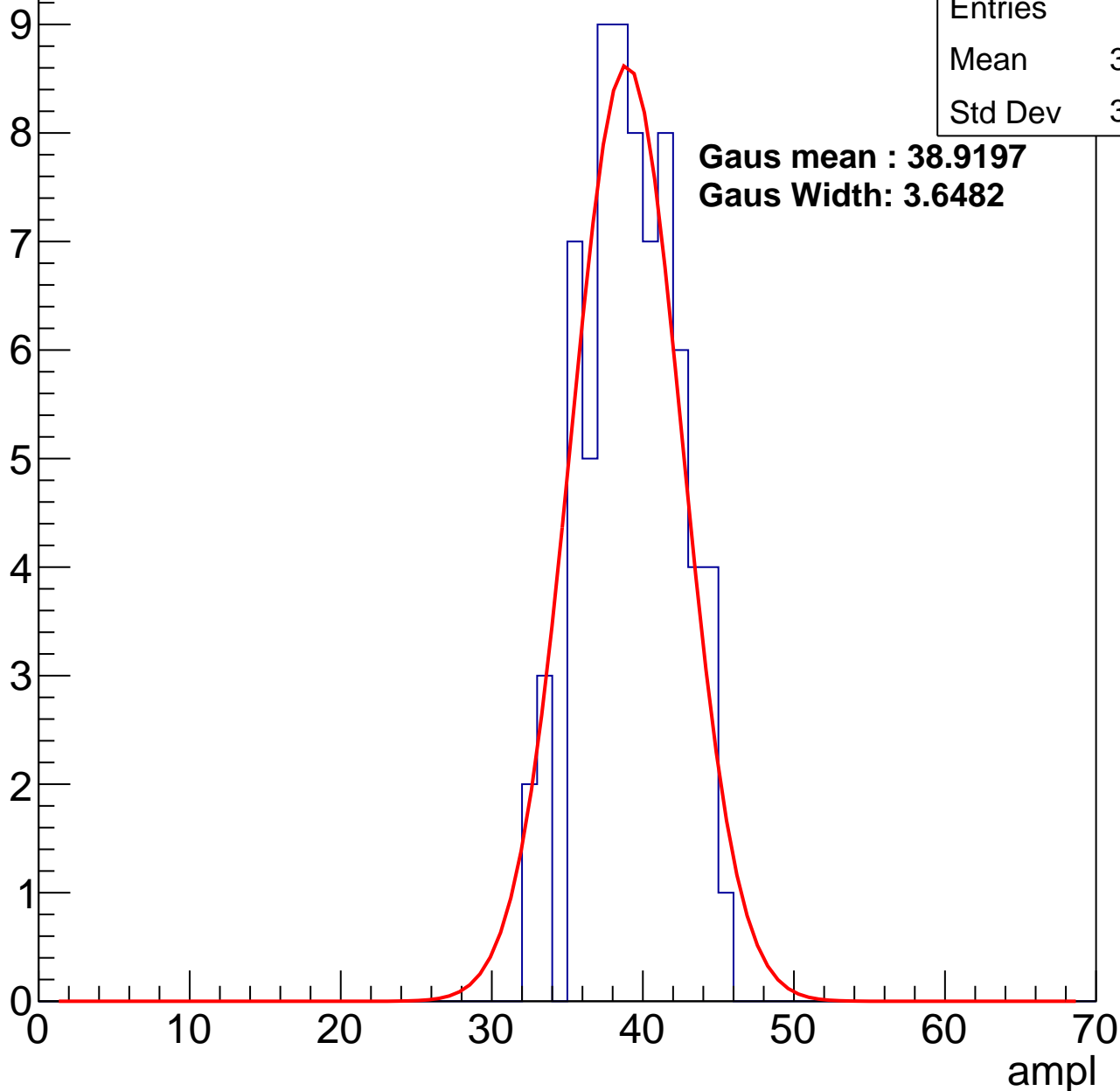
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	38.74
Std Dev	3.088

**Gaus mean : 38.9197**

**Gaus Width: 3.6482**



# B1L101S, U18-ch49, adc2

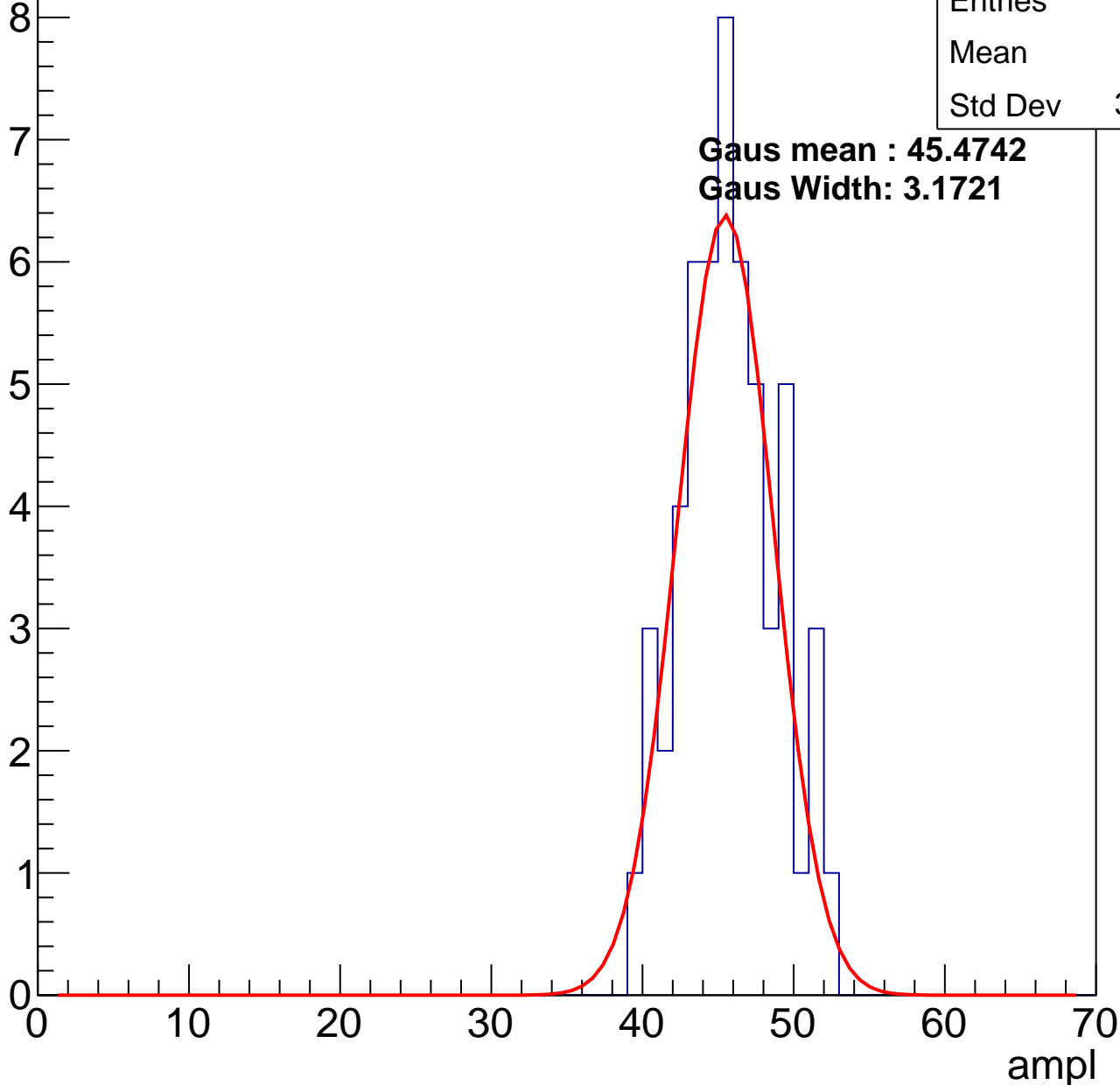
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	45.3
Std Dev	3.101

**Gaus mean : 45.4742**

**Gaus Width: 3.1721**

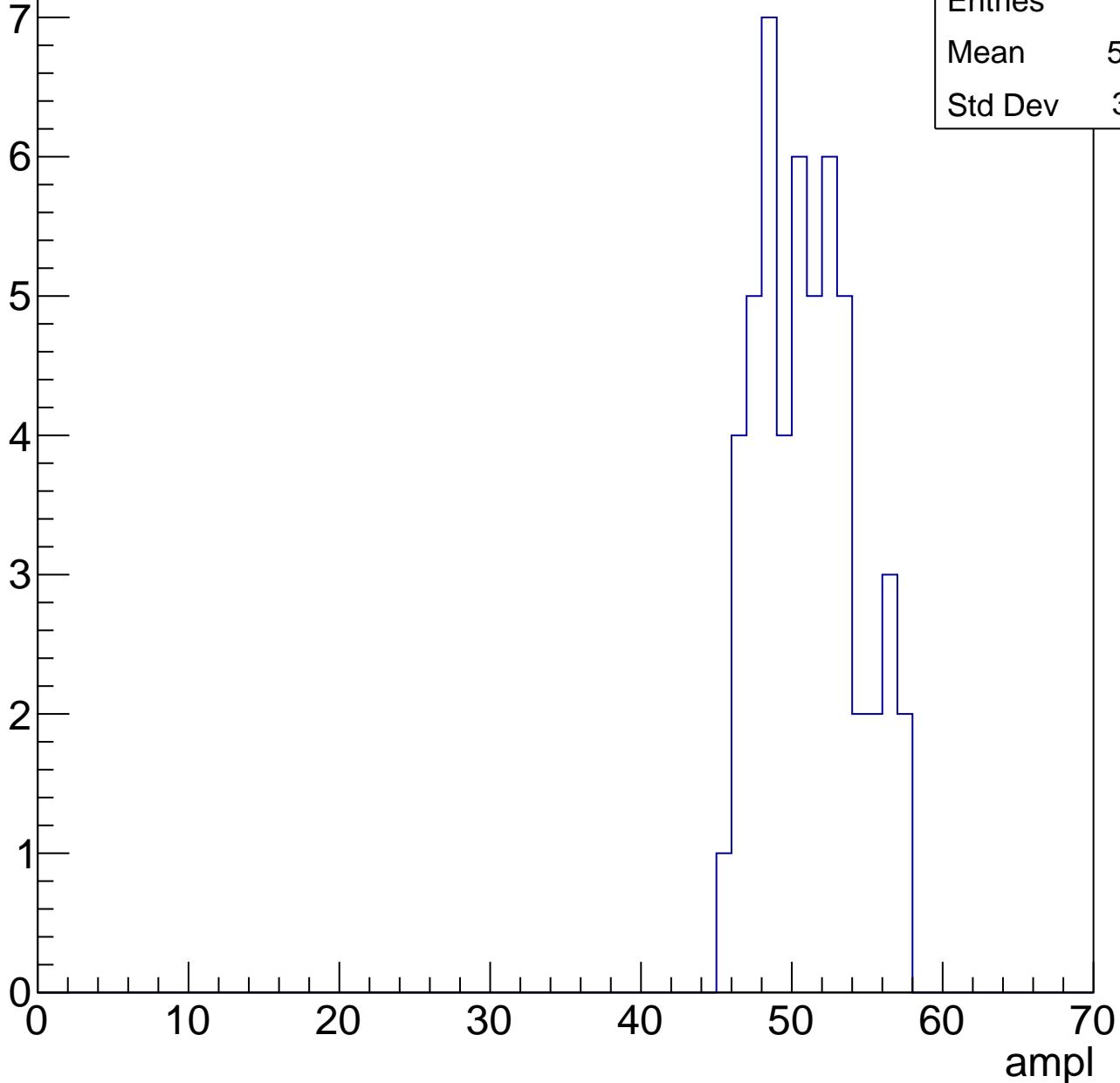


# B1L101S, U18-ch49, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

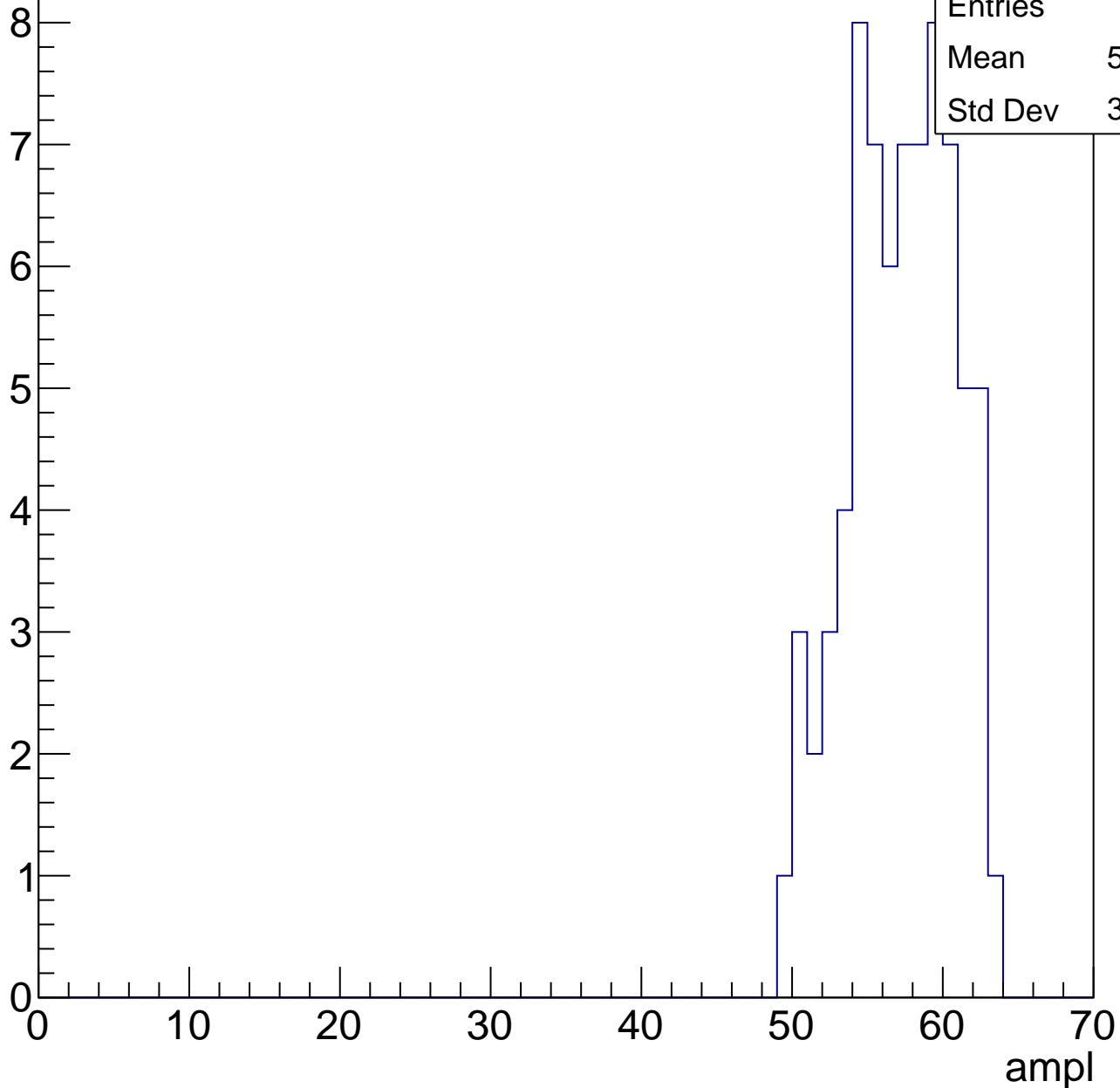
Entries	52
Mean	50.54
Std Dev	3.141



# B1L101S, U18-ch49, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



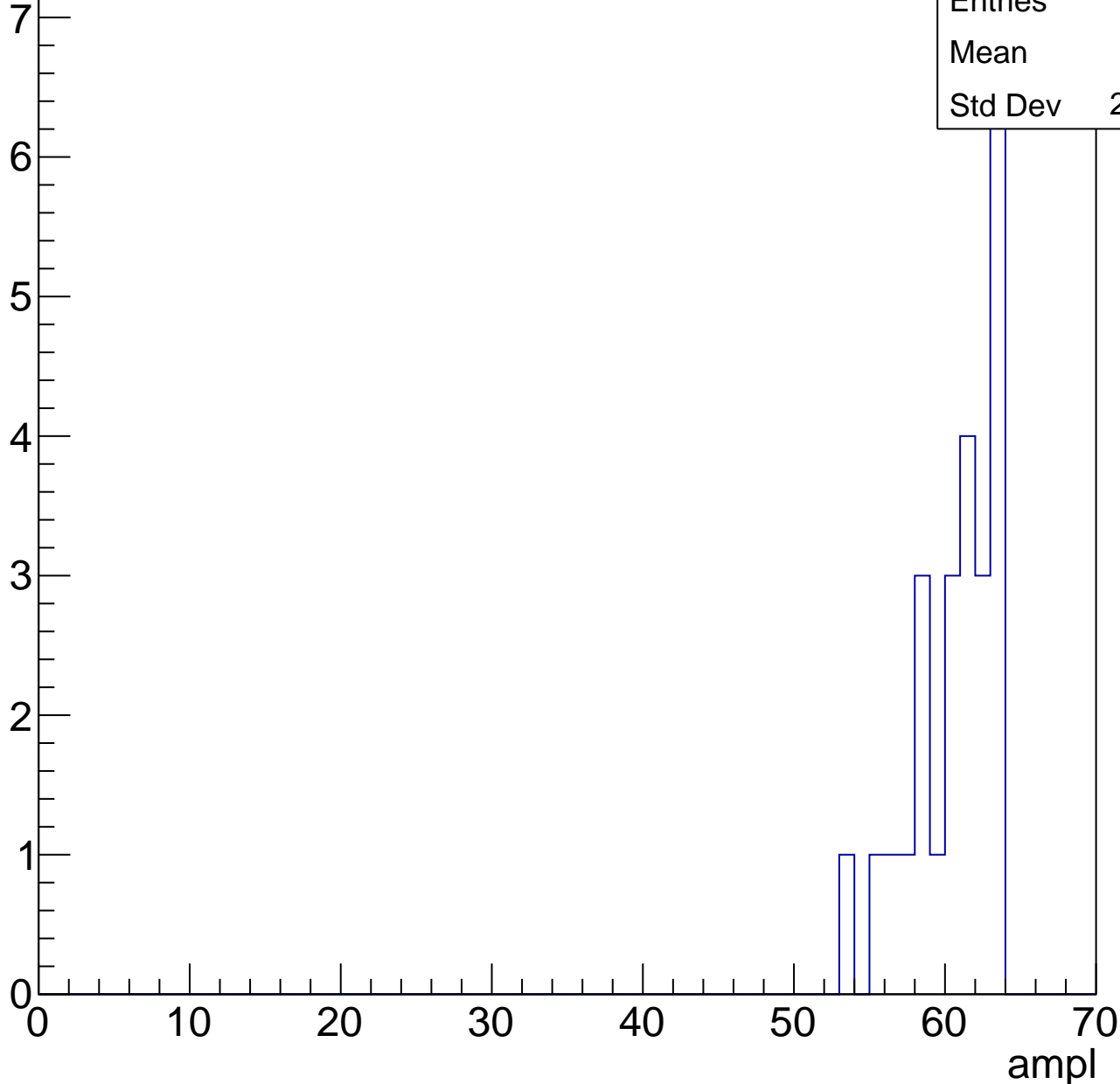
Entries	74
Mean	56.72
Std Dev	3.419

# B1L101S, U18-ch49, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	25
Mean	60.2
Std Dev	2.757



# B1L101S, U18-ch49, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

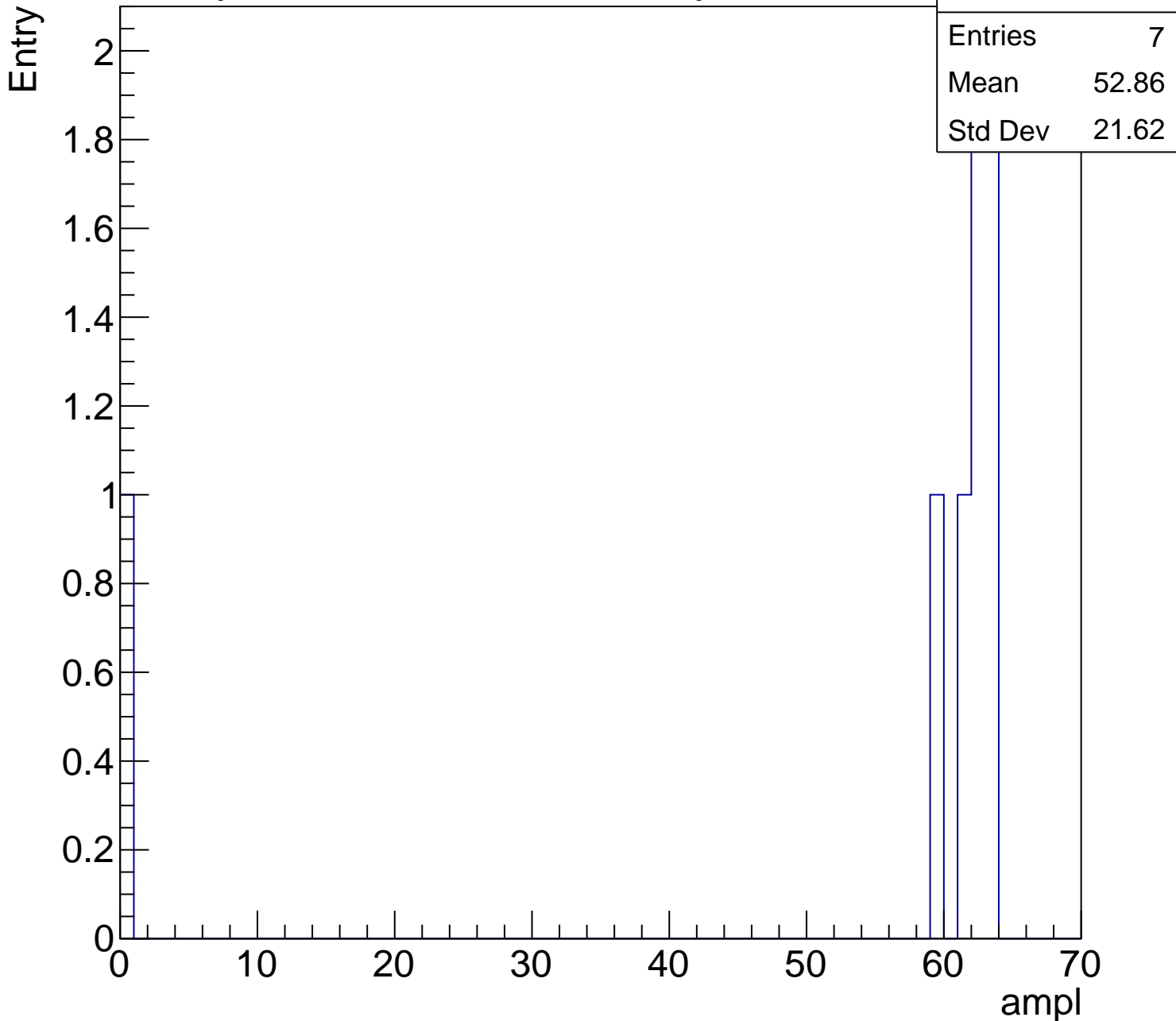
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	7
Mean	52.86
Std Dev	21.62

0 10 20 30 40 50 60 70

ampl





# B1L101S, U18-ch49, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch50, adc0

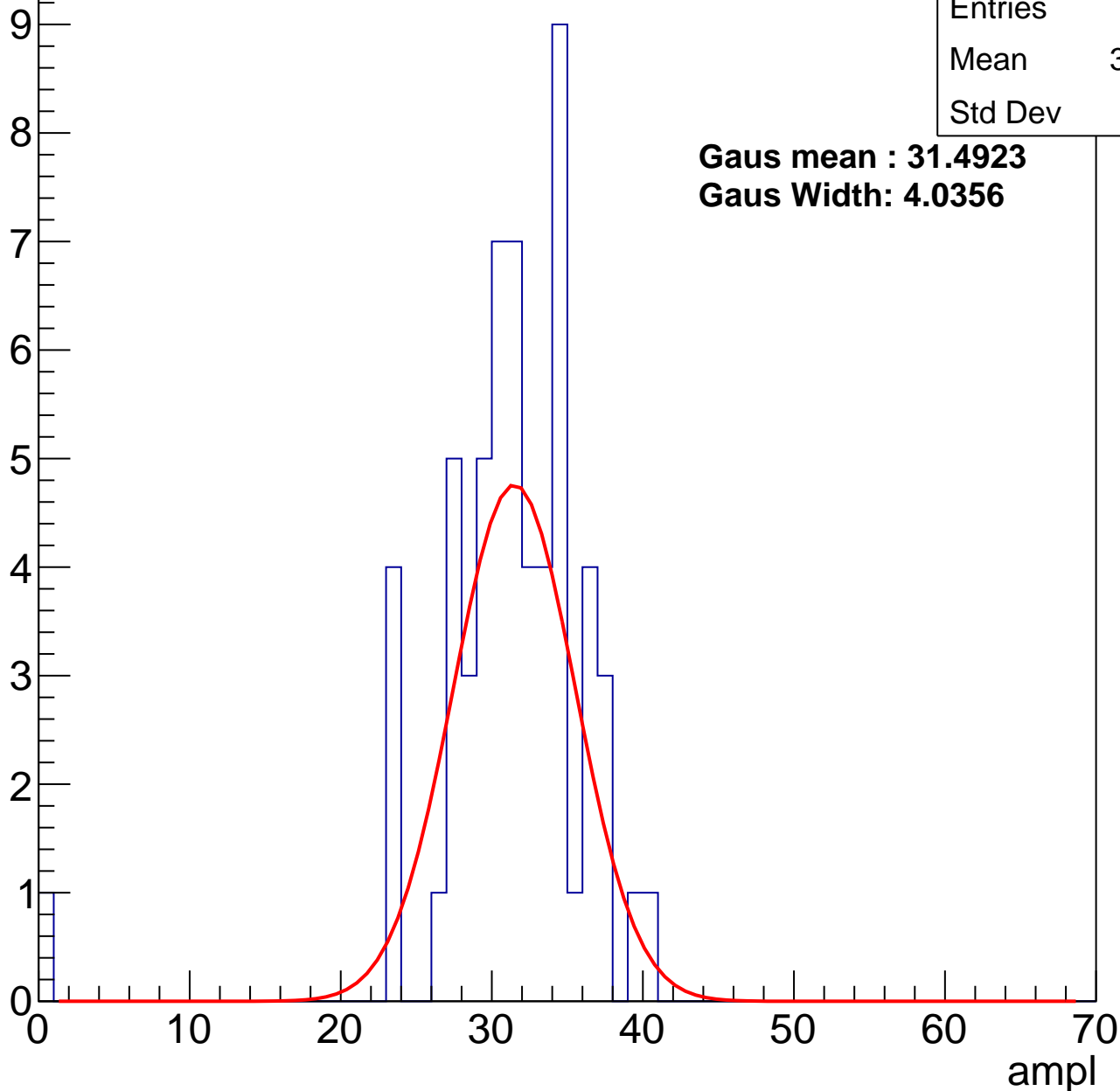
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	30.73
Std Dev	5.54

**Gaus mean : 31.4923**

**Gaus Width: 4.0356**



# B1L101S, U18-ch50, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	65
Mean	37.12
Std Dev	5.576

**Gaus mean : 38.7865**

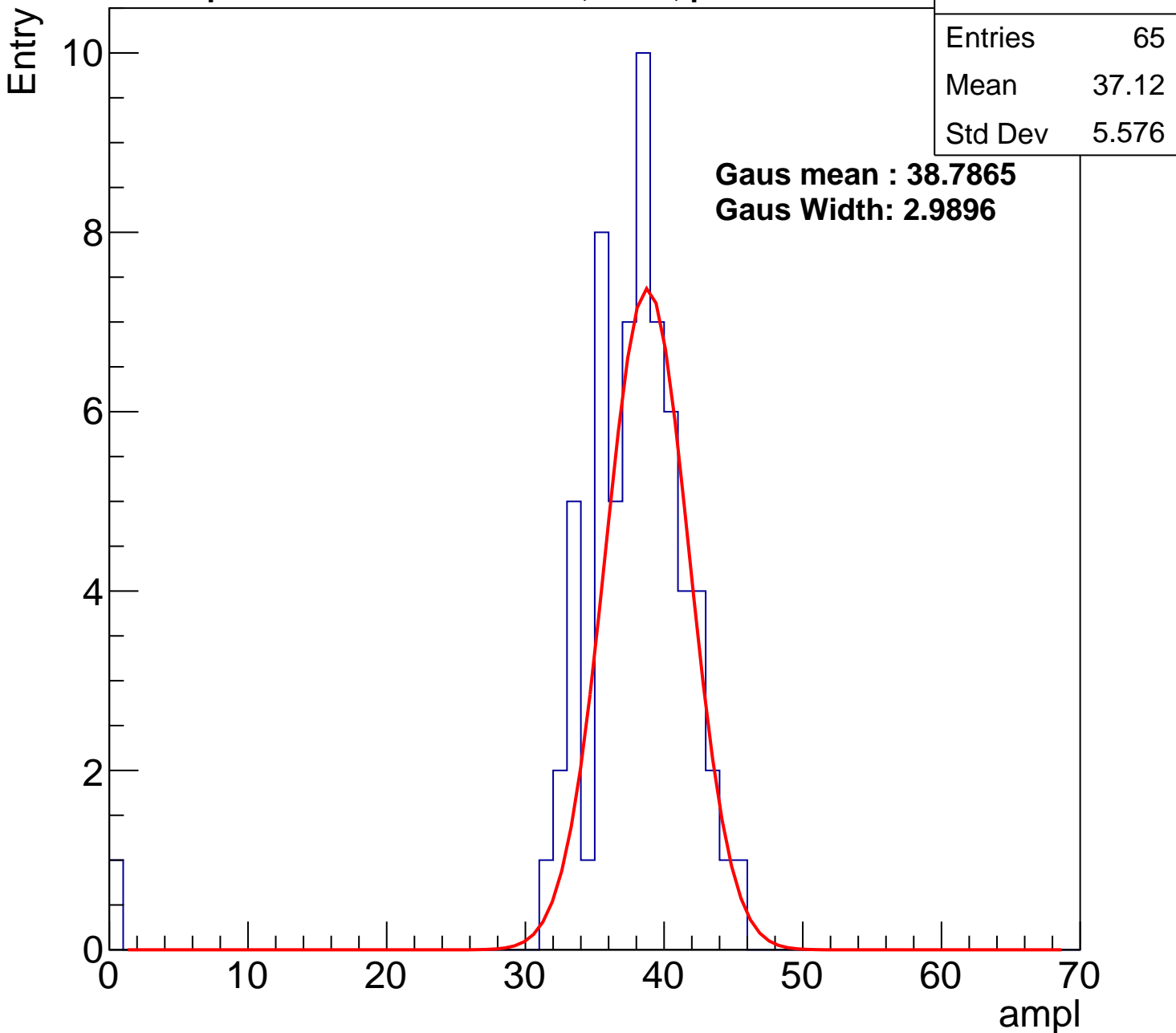
**Gaus Width: 2.9896**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U18-ch50, adc2

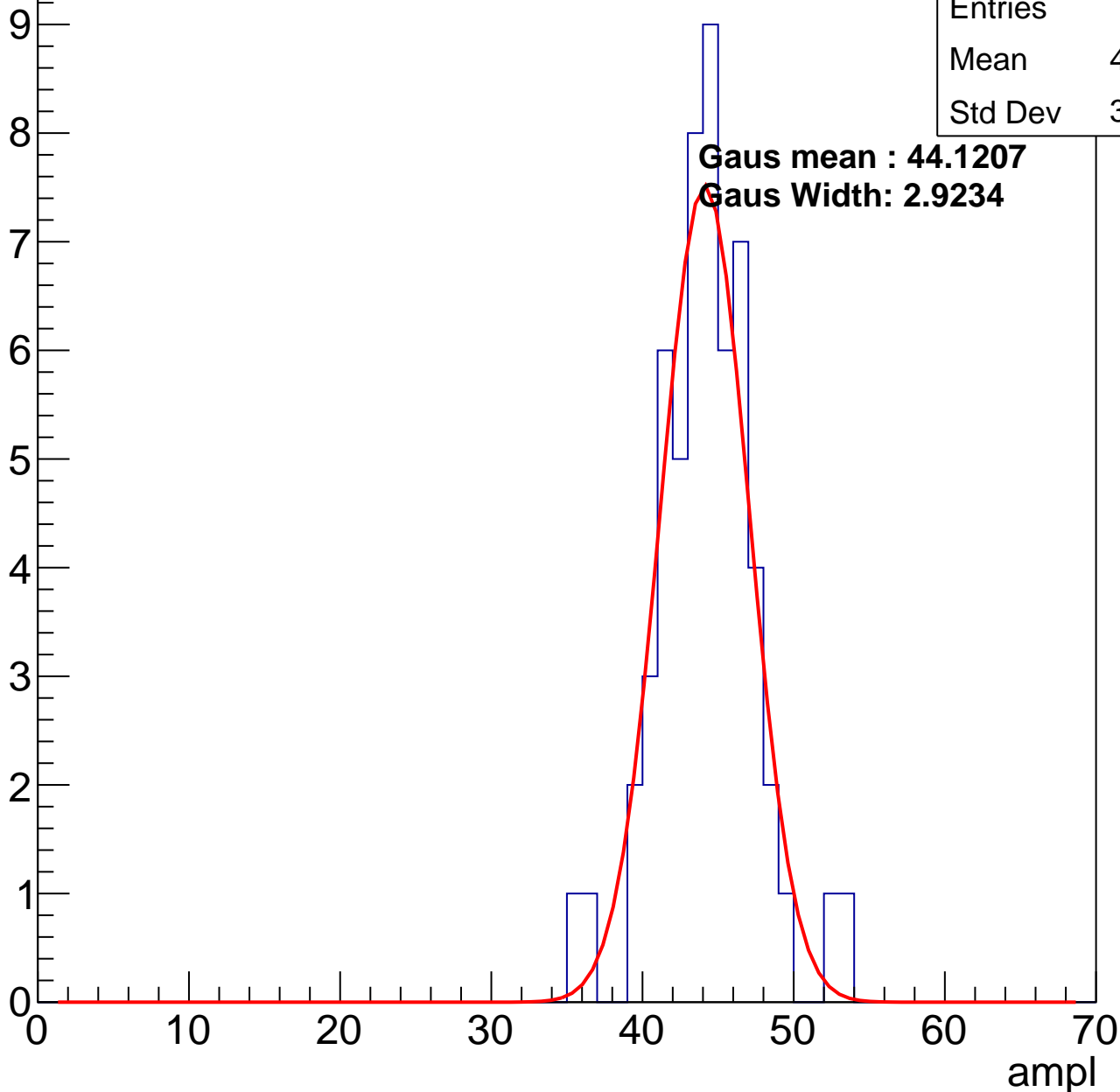
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	43.77
Std Dev	3.228

**Gaus mean : 44.1207**

**Gaus Width: 2.9234**

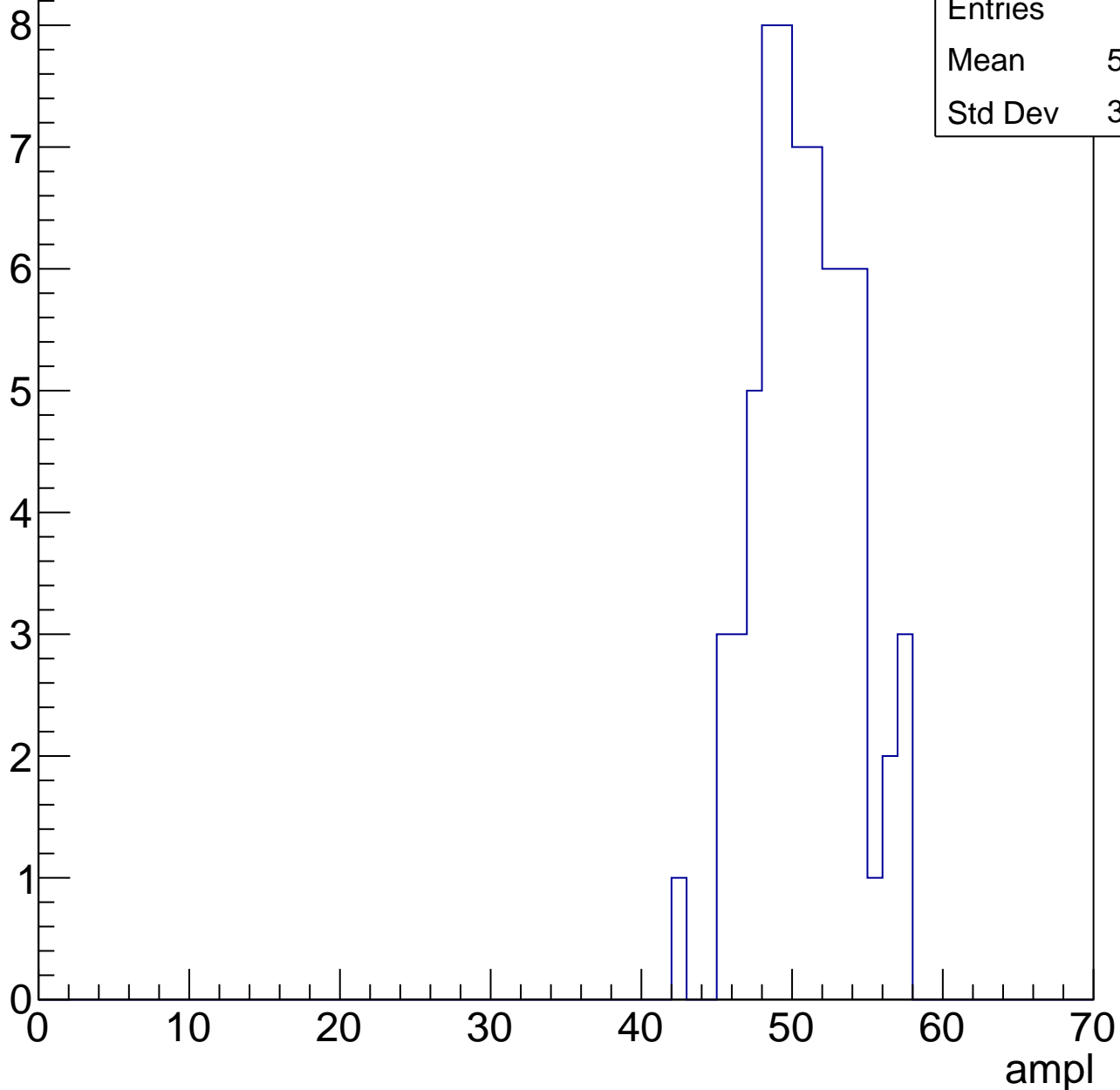


# B1L101S, U18-ch50, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

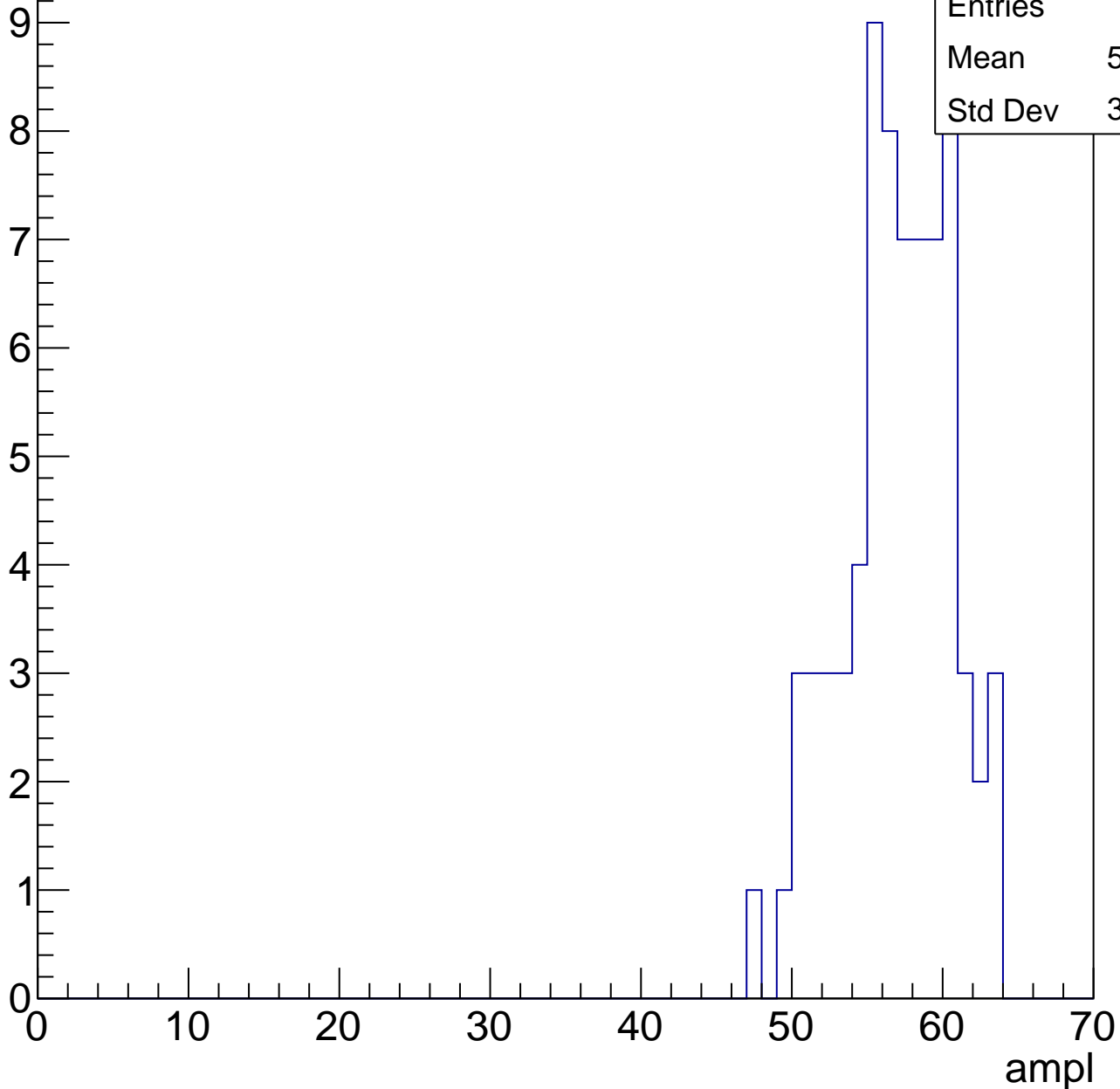
Entries	66
Mean	50.38
Std Dev	3.228



# B1L101S, U18-ch50, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

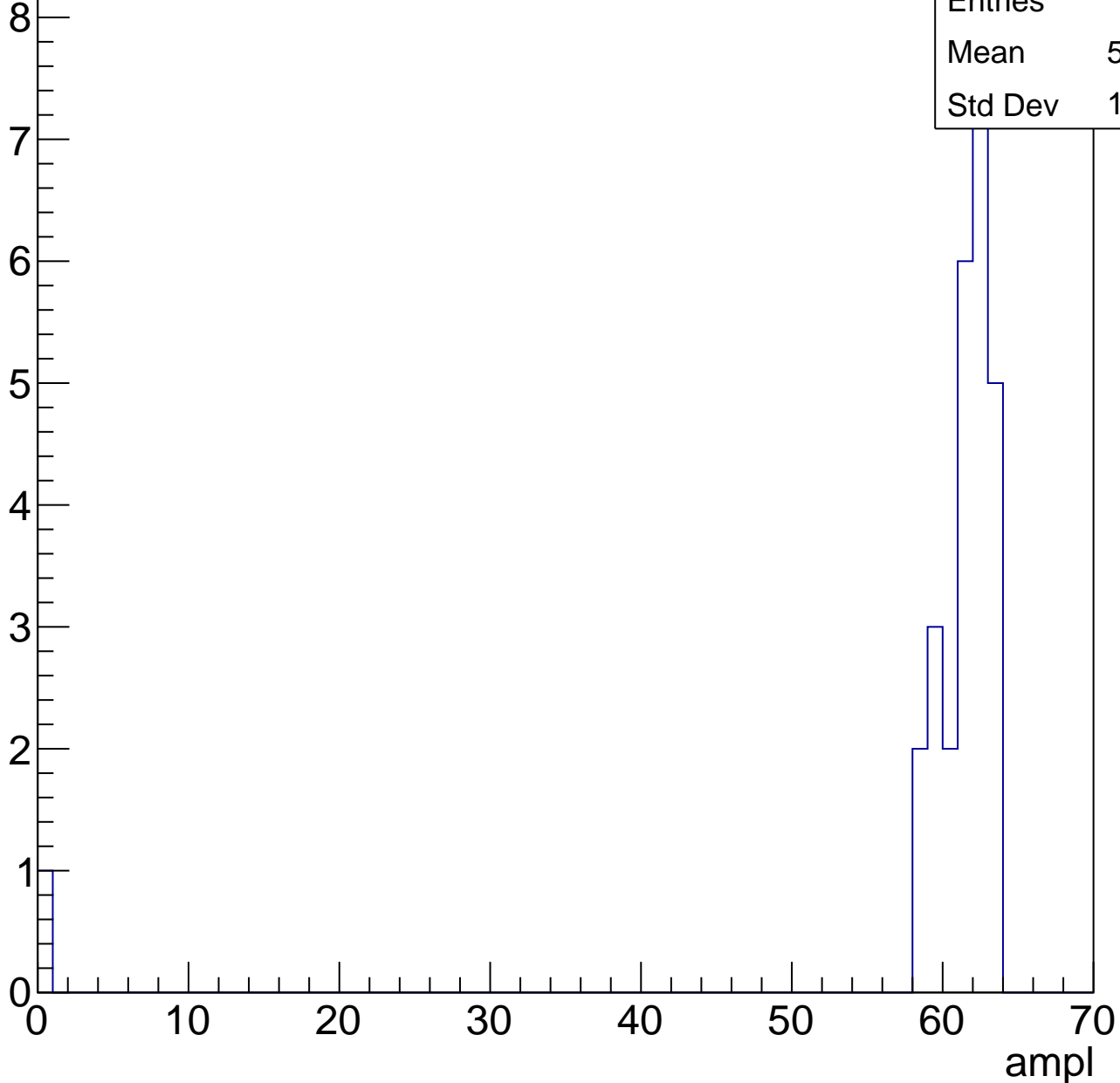


# B1L101S, U18-ch50, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

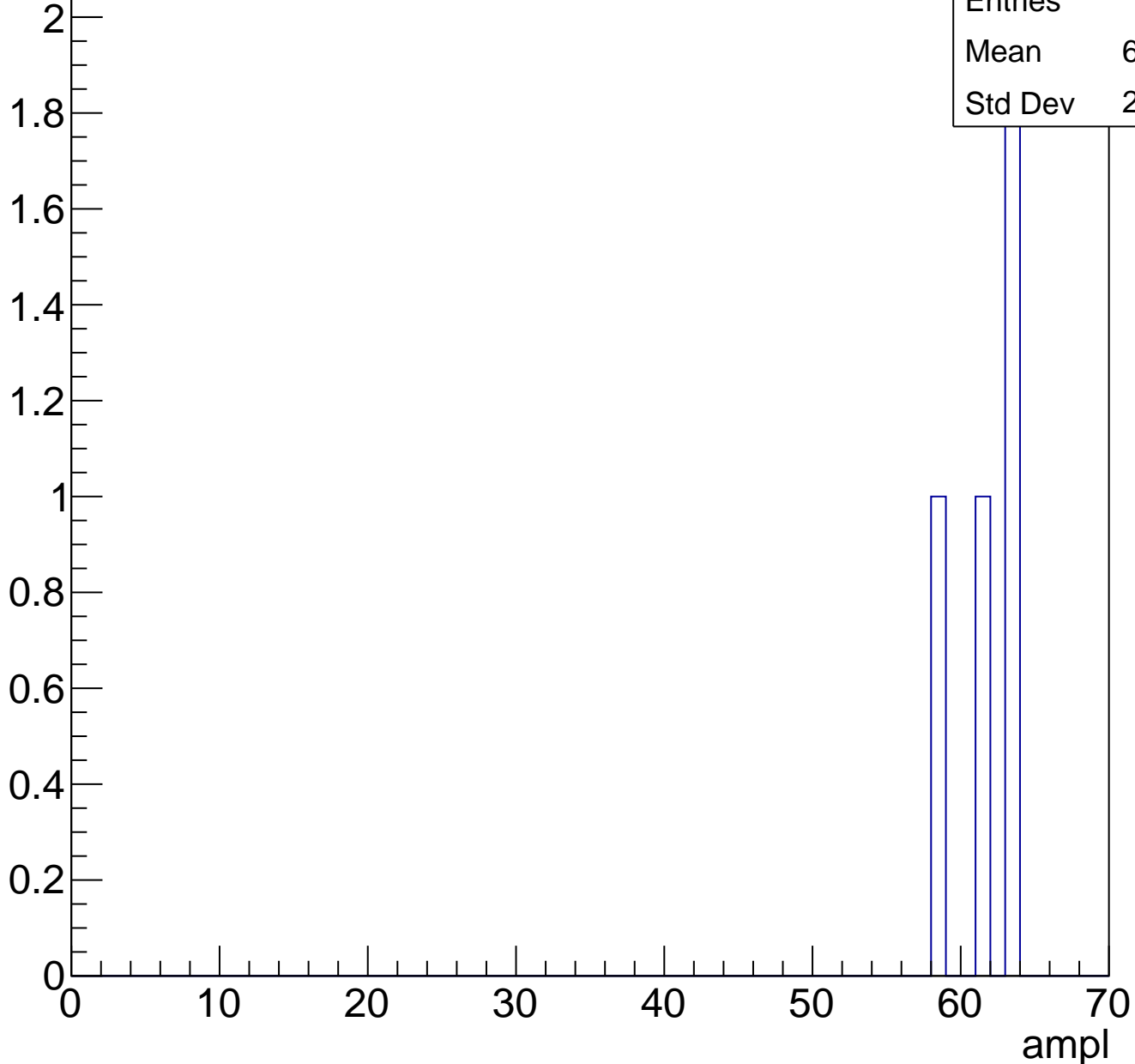
Entries	27
Mean	58.89
Std Dev	11.64



# B1L101S, U18-ch50, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch50, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U18-ch51, adc0

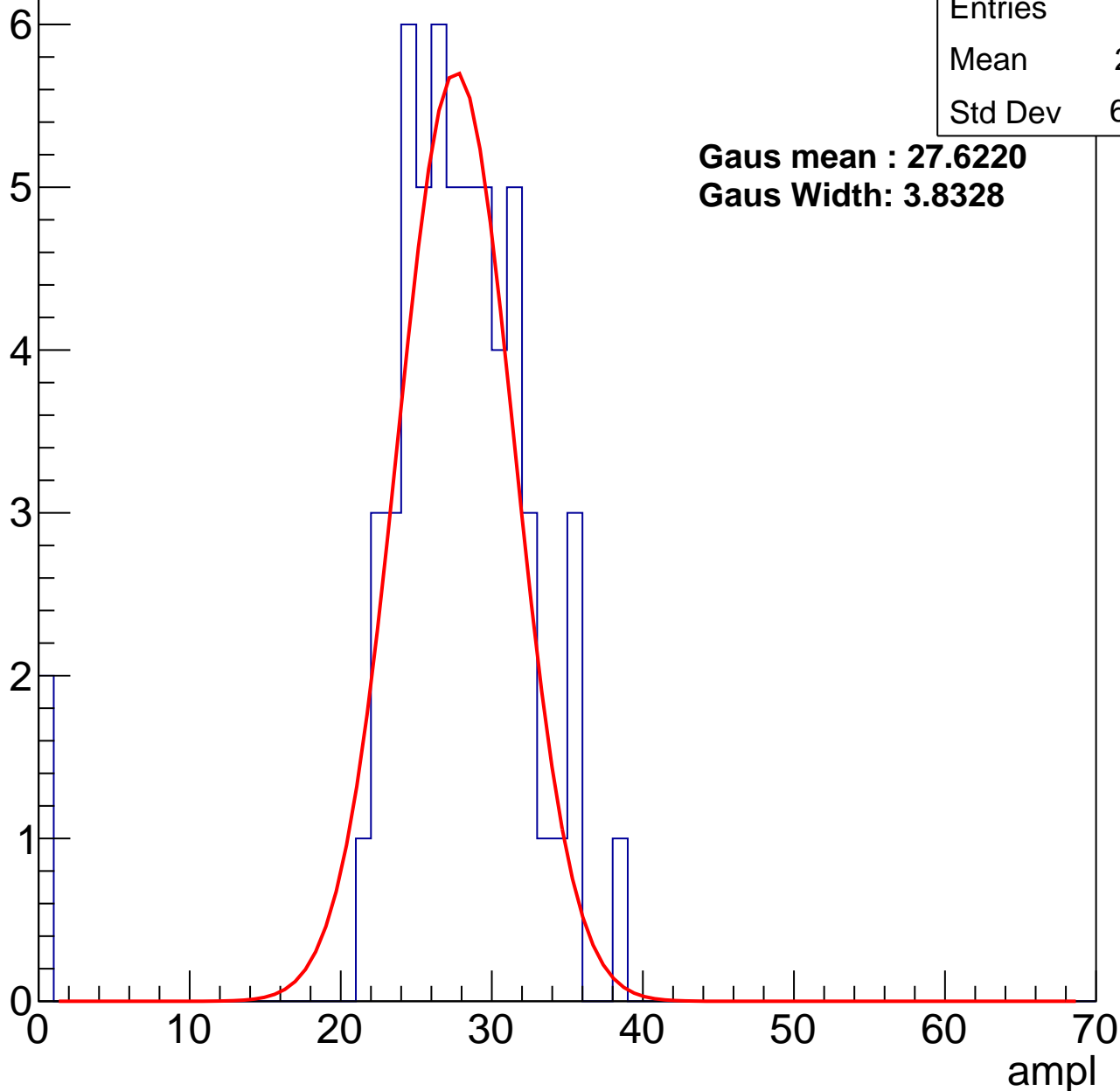
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	26.81
Std Dev	6.256

**Gaus mean : 27.6220**

**Gaus Width: 3.8328**



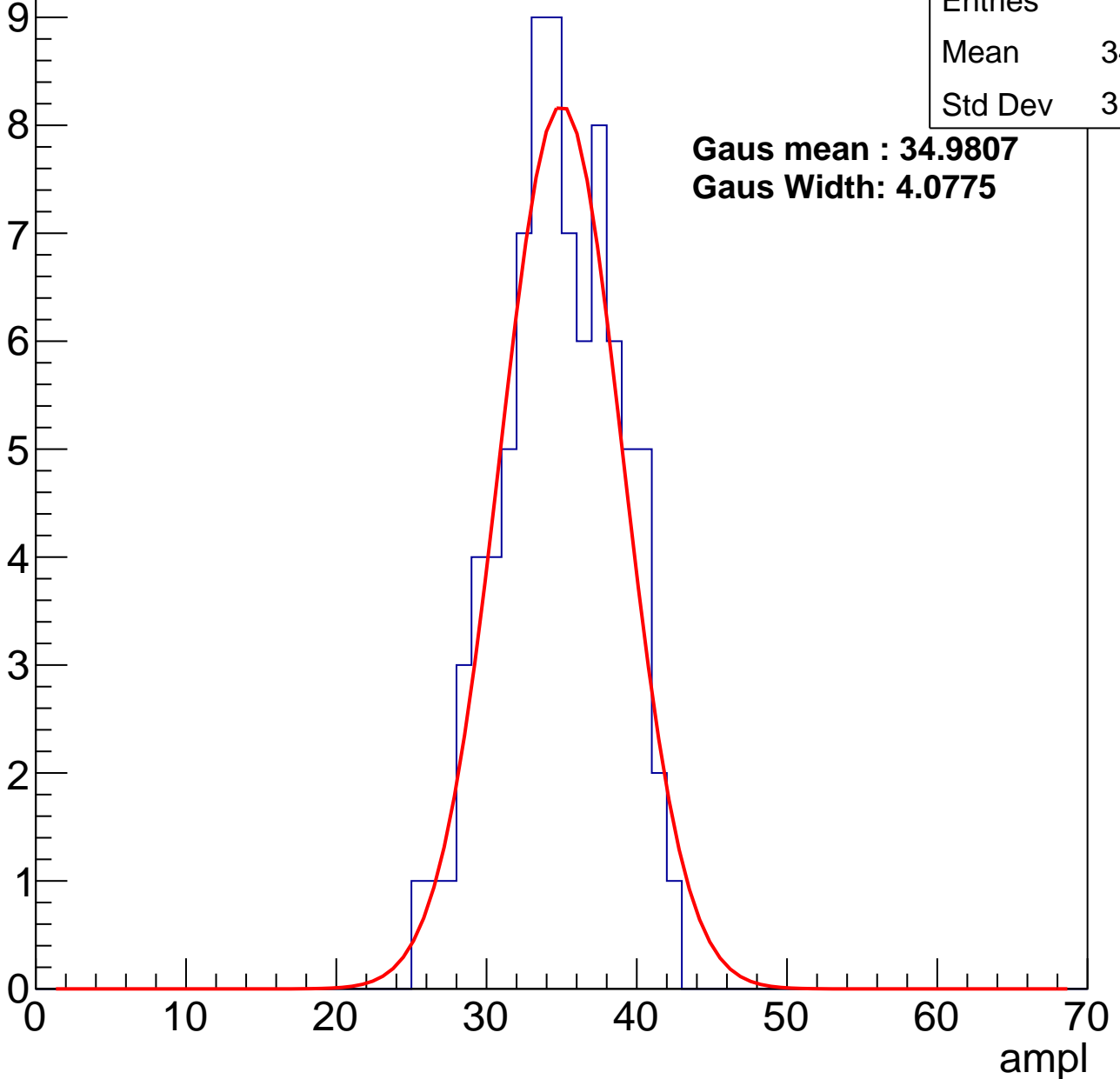
# B1L101S, U18-ch51, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	84
Mean	34.33
Std Dev	3.787

**Gaus mean : 34.9807**  
**Gaus Width: 4.0775**



# B1L101S, U18-ch51, adc2

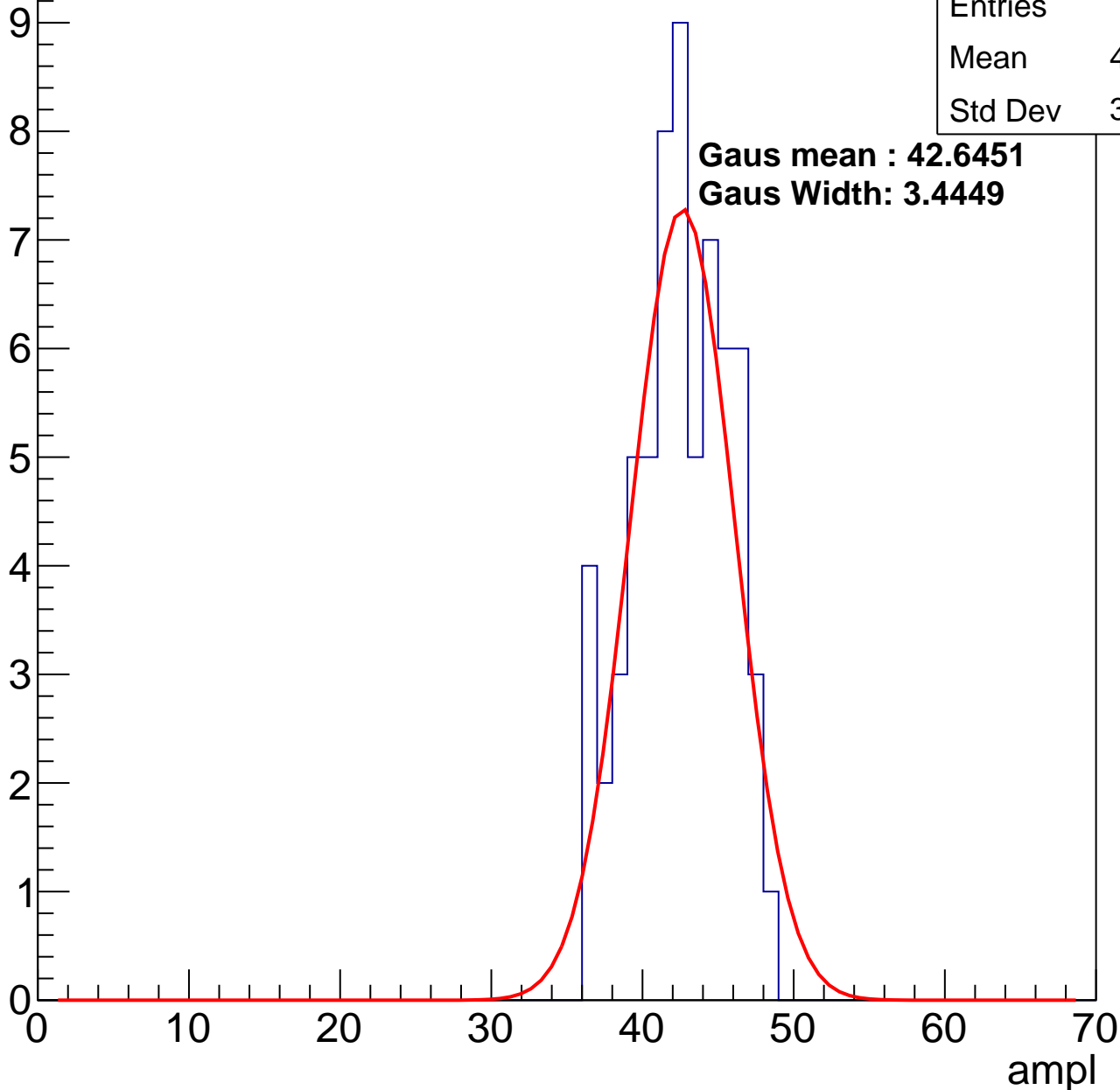
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	42.05
Std Dev	3.084

**Gaus mean : 42.6451**

**Gaus Width: 3.4449**

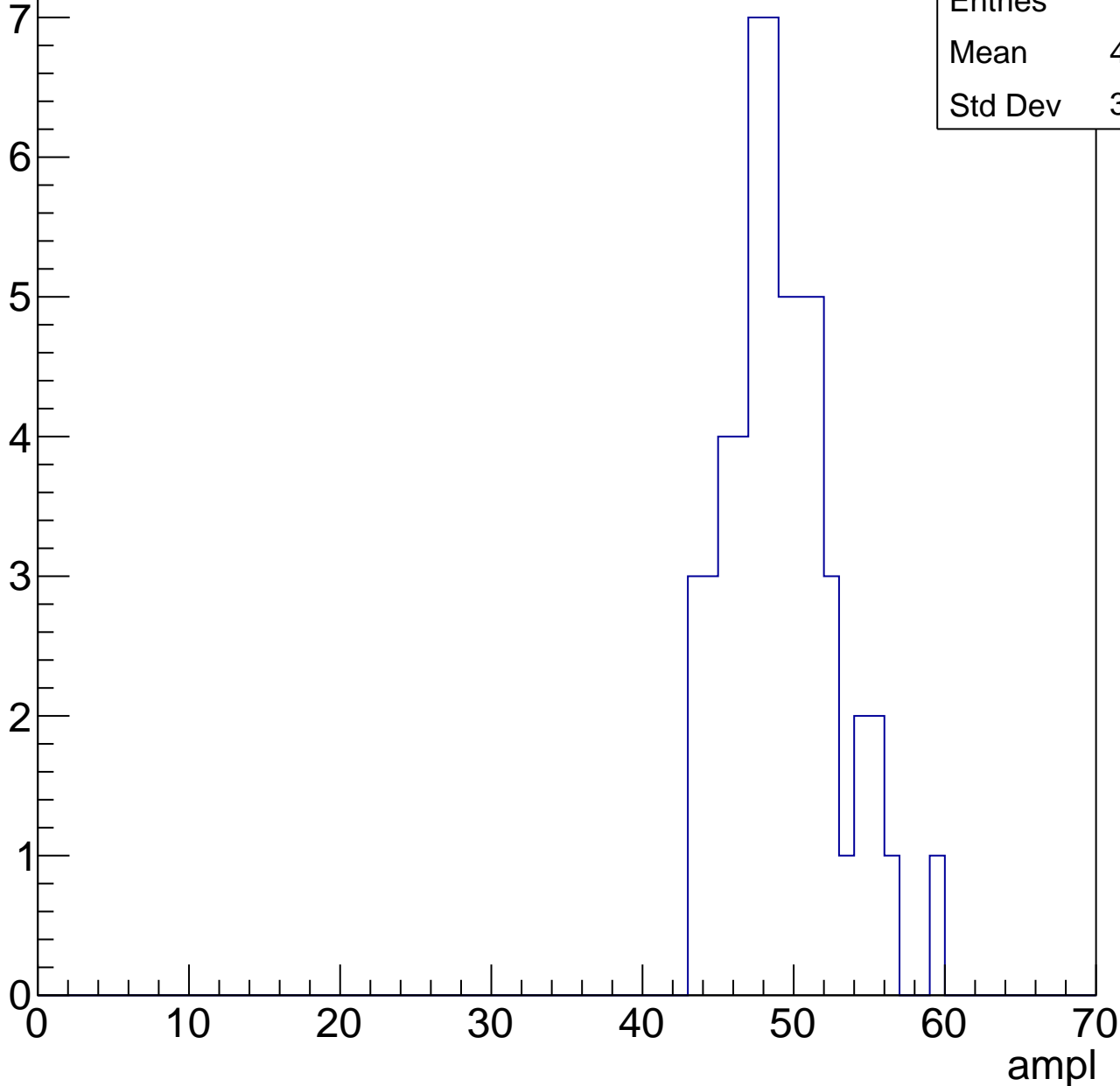


# B1L101S, U18-ch51, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

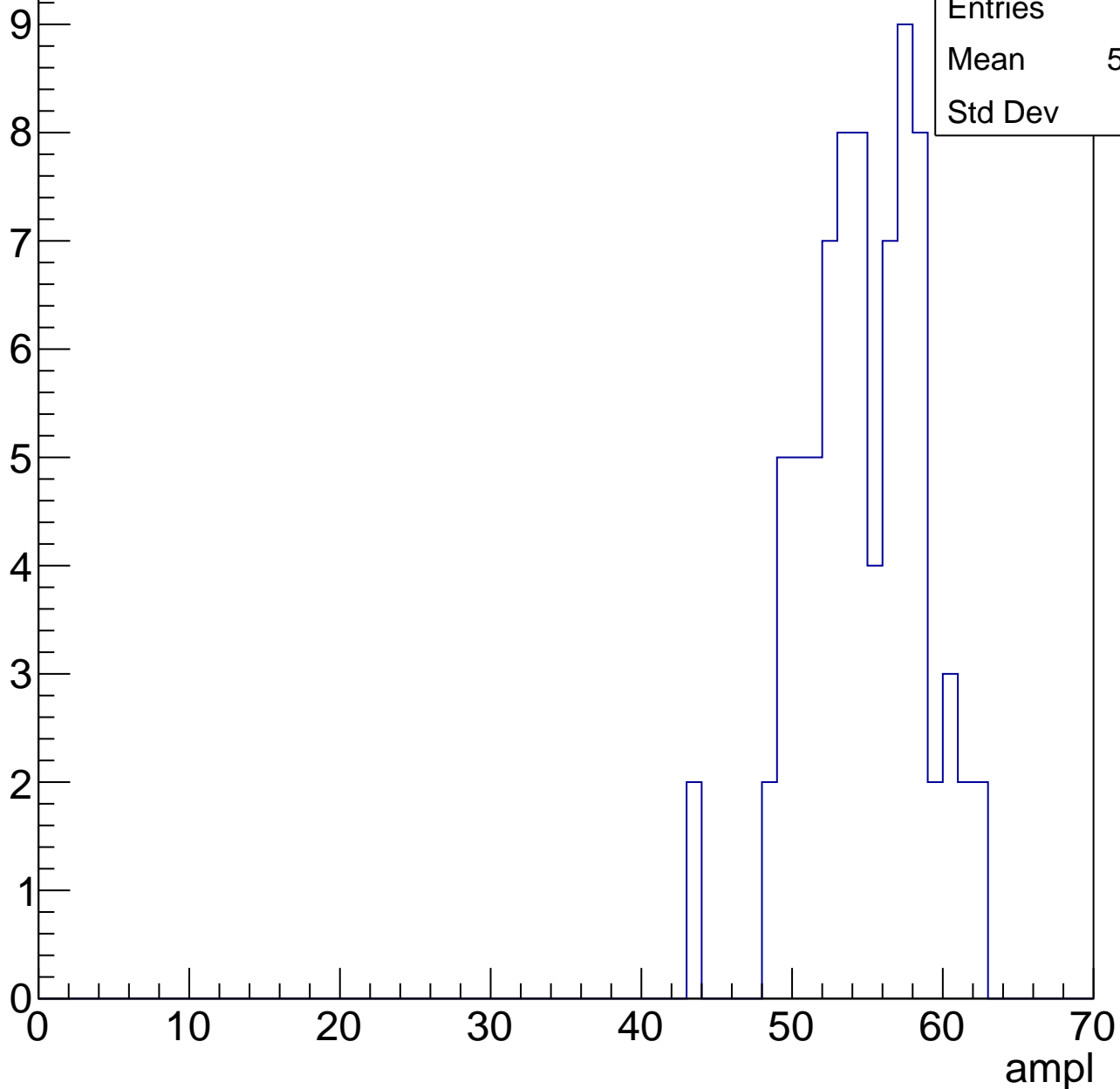
Entries	53
Mean	48.72
Std Dev	3.509



# B1L101S, U18-ch51, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

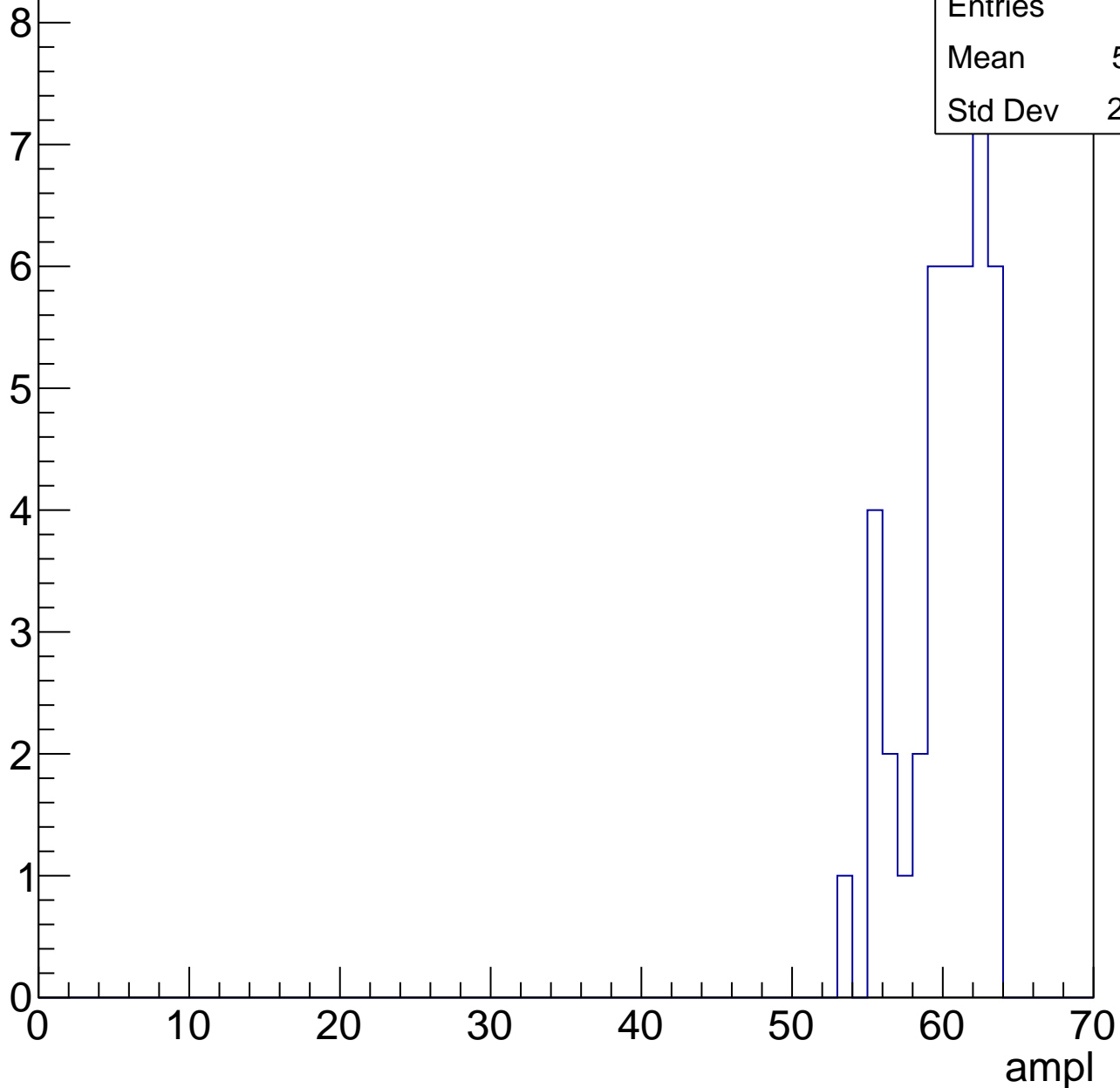


# B1L101S, U18-ch51, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

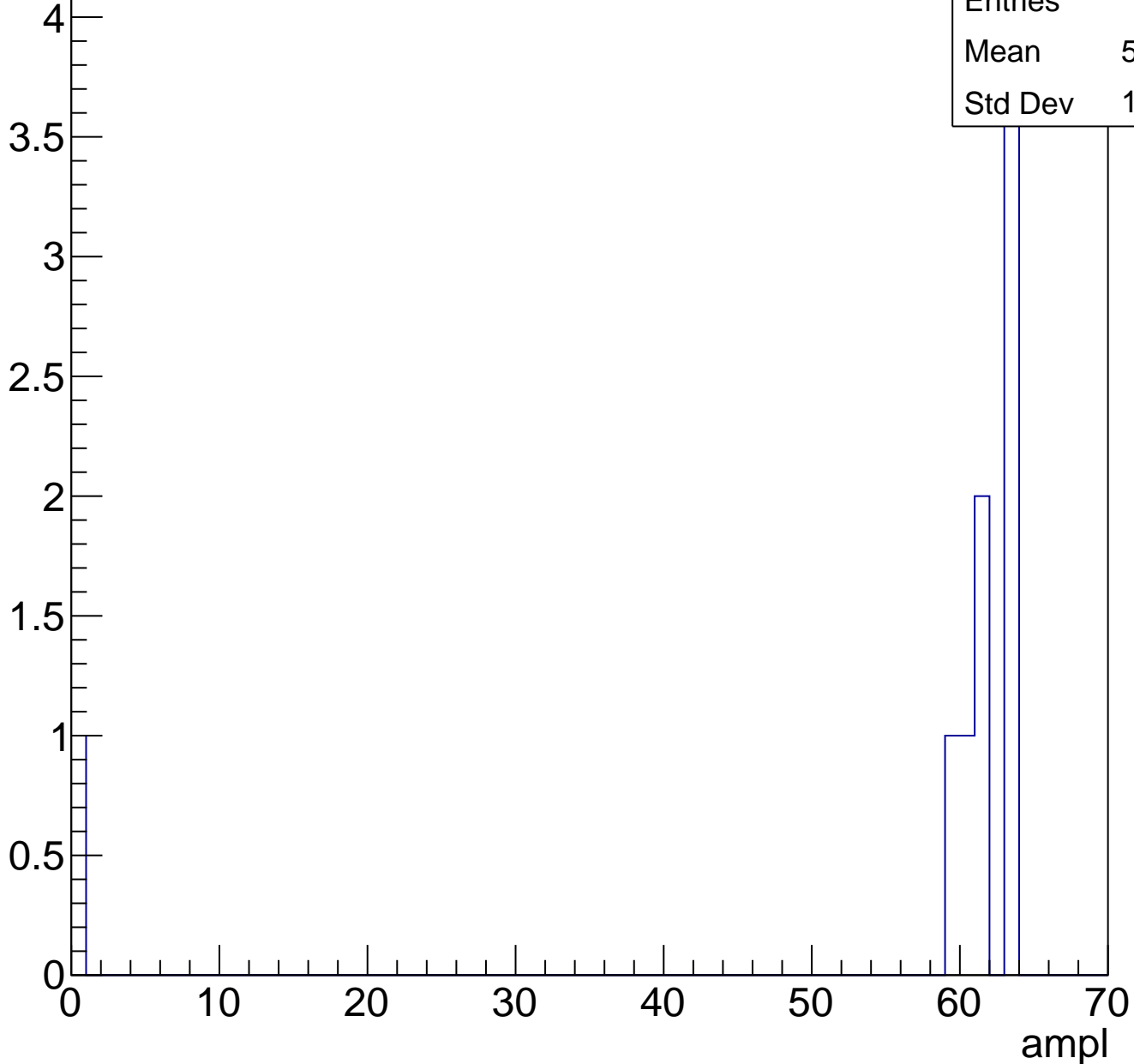
Entries	42
Mean	59.81
Std Dev	2.648



# B1L101S, U18-ch51, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch51, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L101S, U18-ch52, adc0

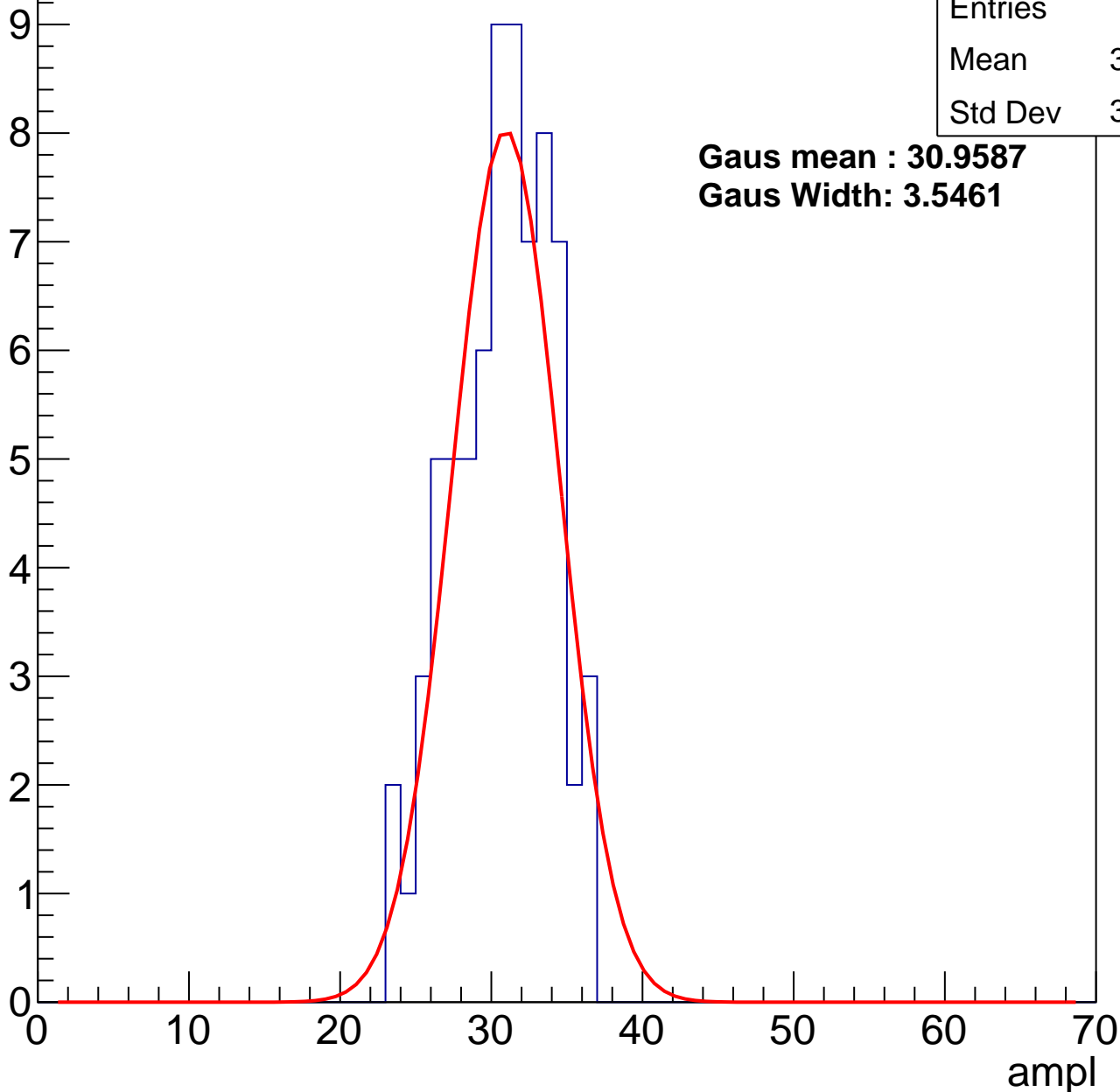
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	30.24
Std Dev	3.195

**Gaus mean : 30.9587**

**Gaus Width: 3.5461**



# B1L101S, U18-ch52, adc1

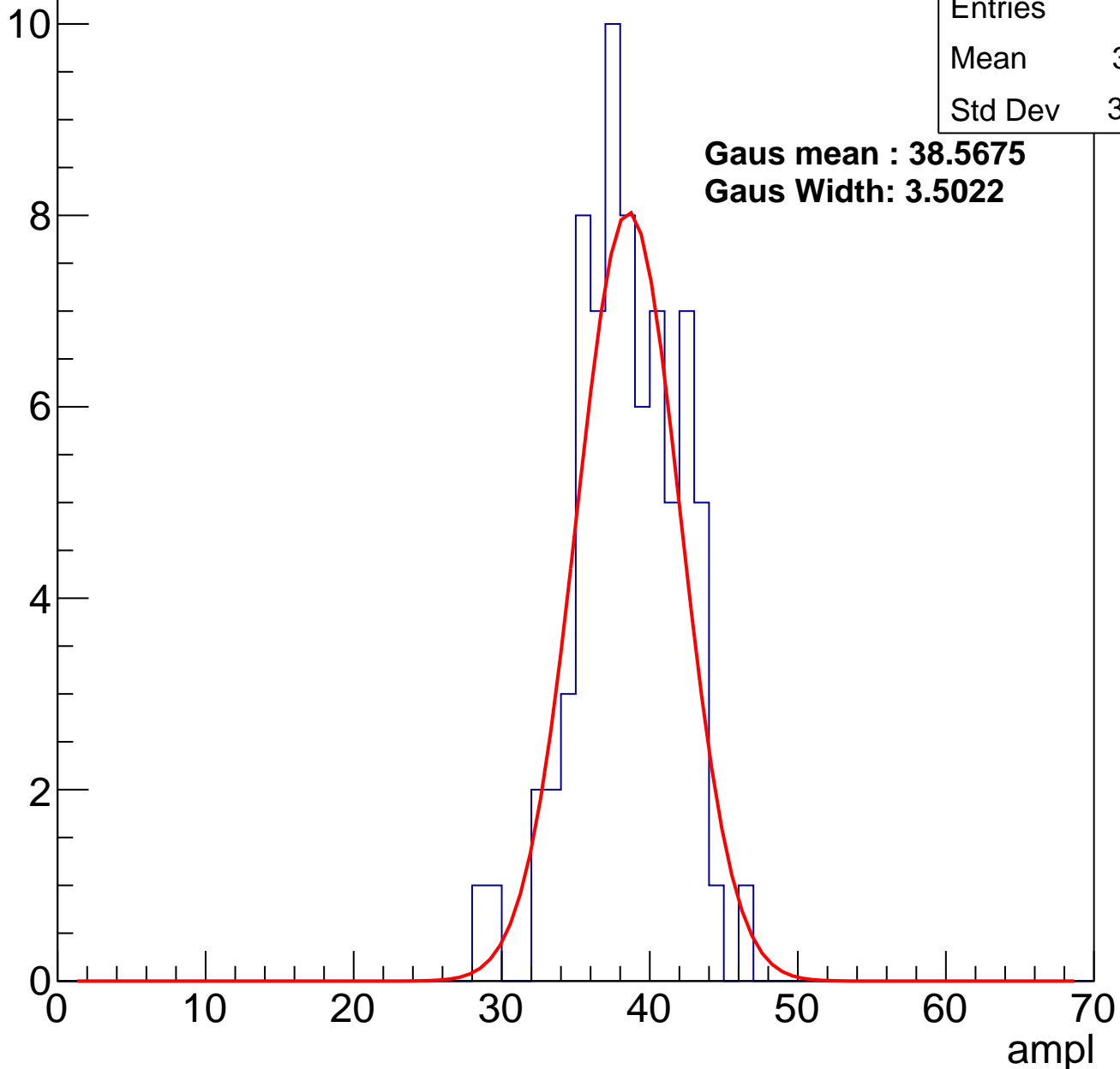
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	74
Mean	38.01
Std Dev	3.443

**Gaus mean : 38.5675**

**Gaus Width: 3.5022**

Entry



# B1L101S, U18-ch52, adc2

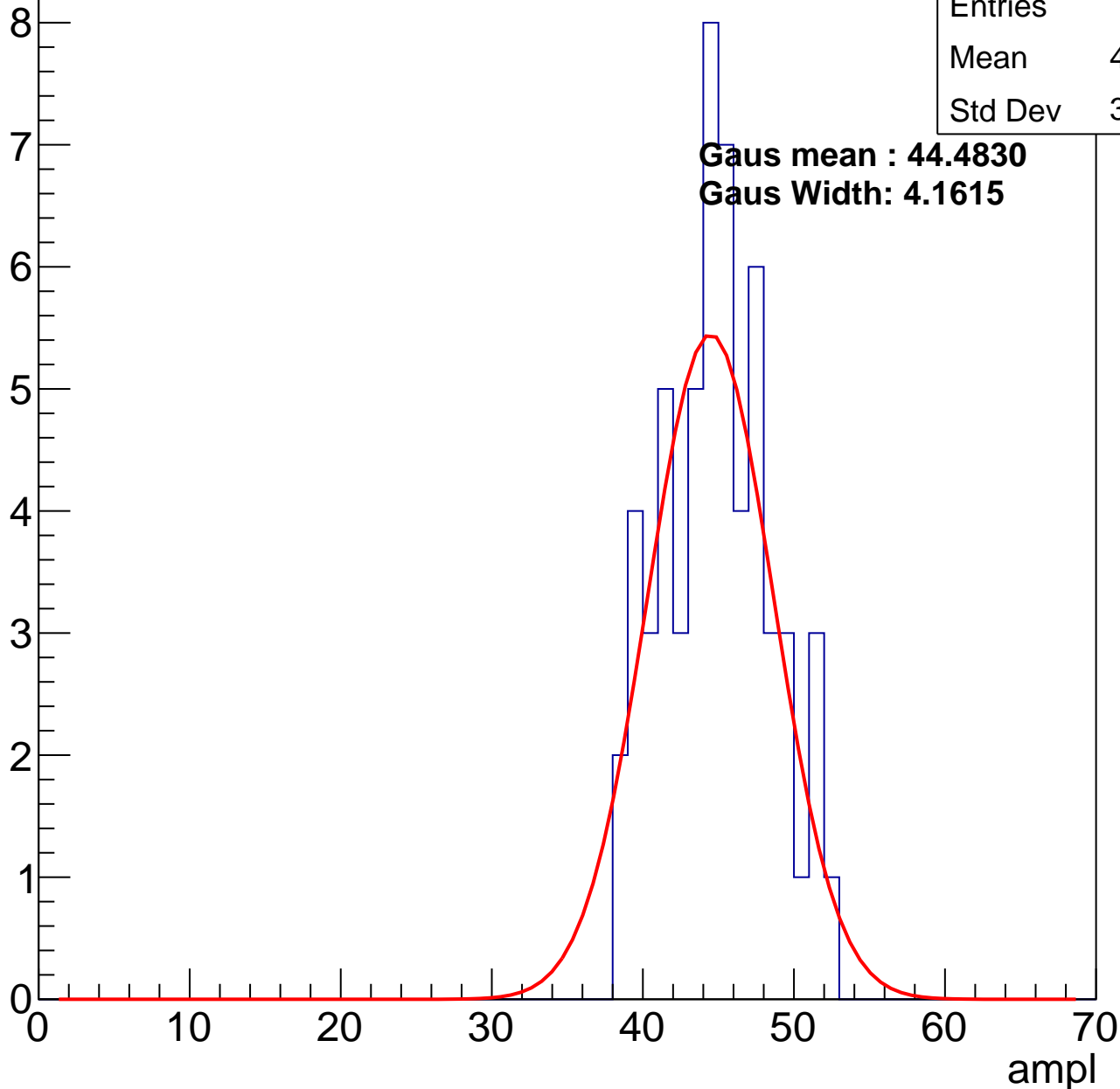
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	44.43
Std Dev	3.519

**Gaus mean : 44.4830**

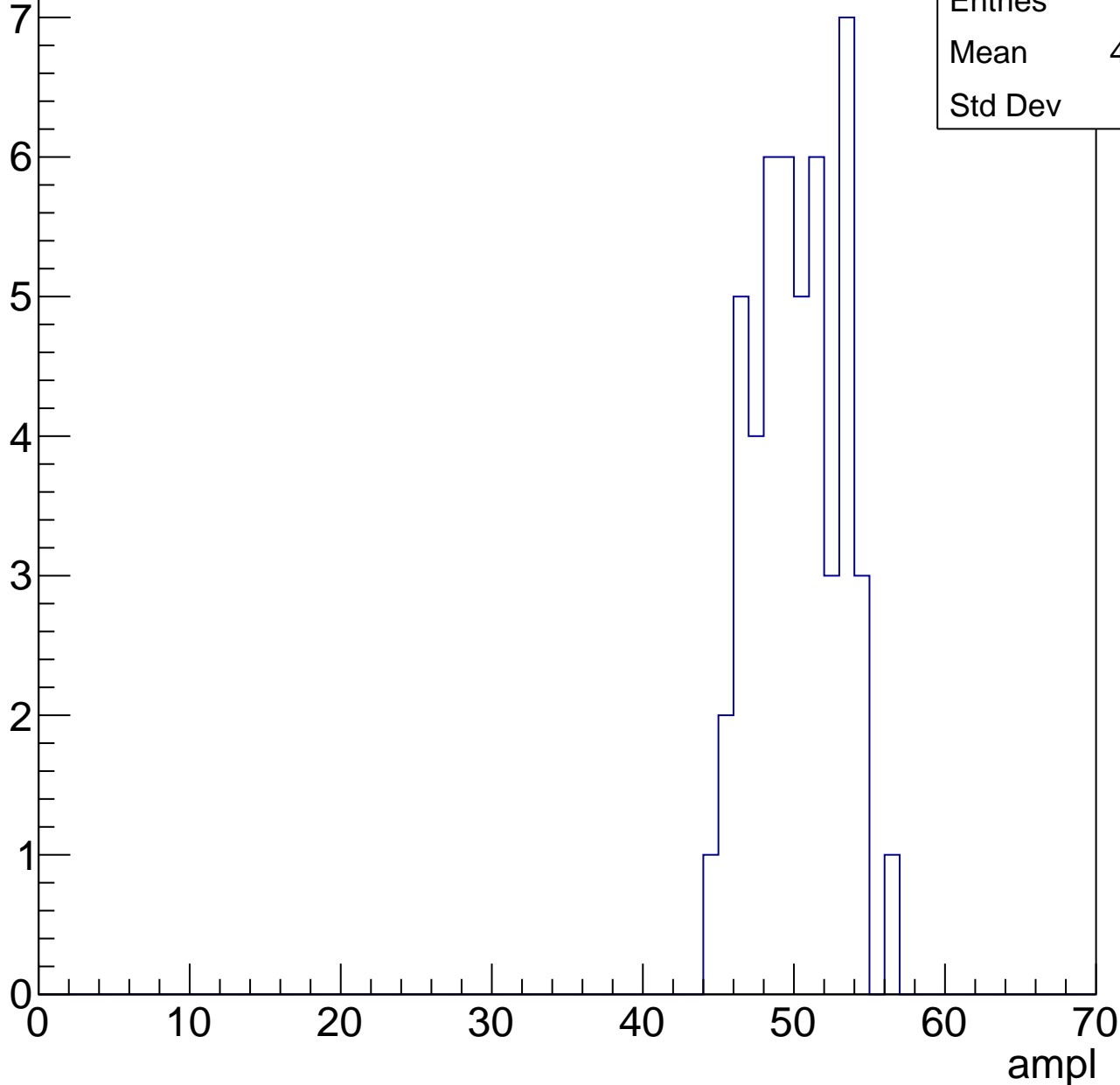
**Gaus Width: 4.1615**



# B1L101S, U18-ch52, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



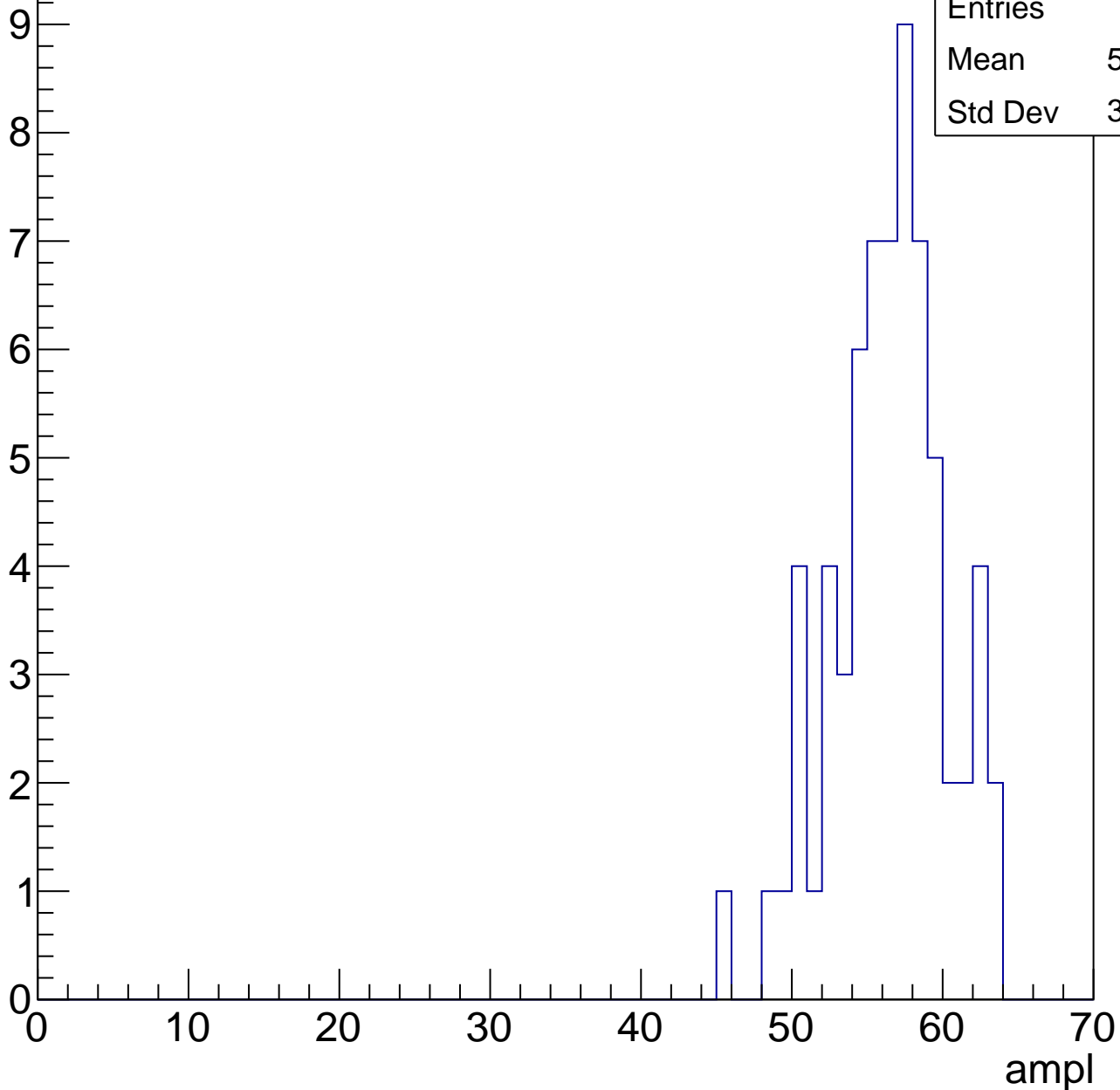
Entries	49
Mean	49.69
Std Dev	2.83

# B1L101S, U18-ch52, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	55.92
Std Dev	3.755



# B1L101S, U18-ch52, adc5

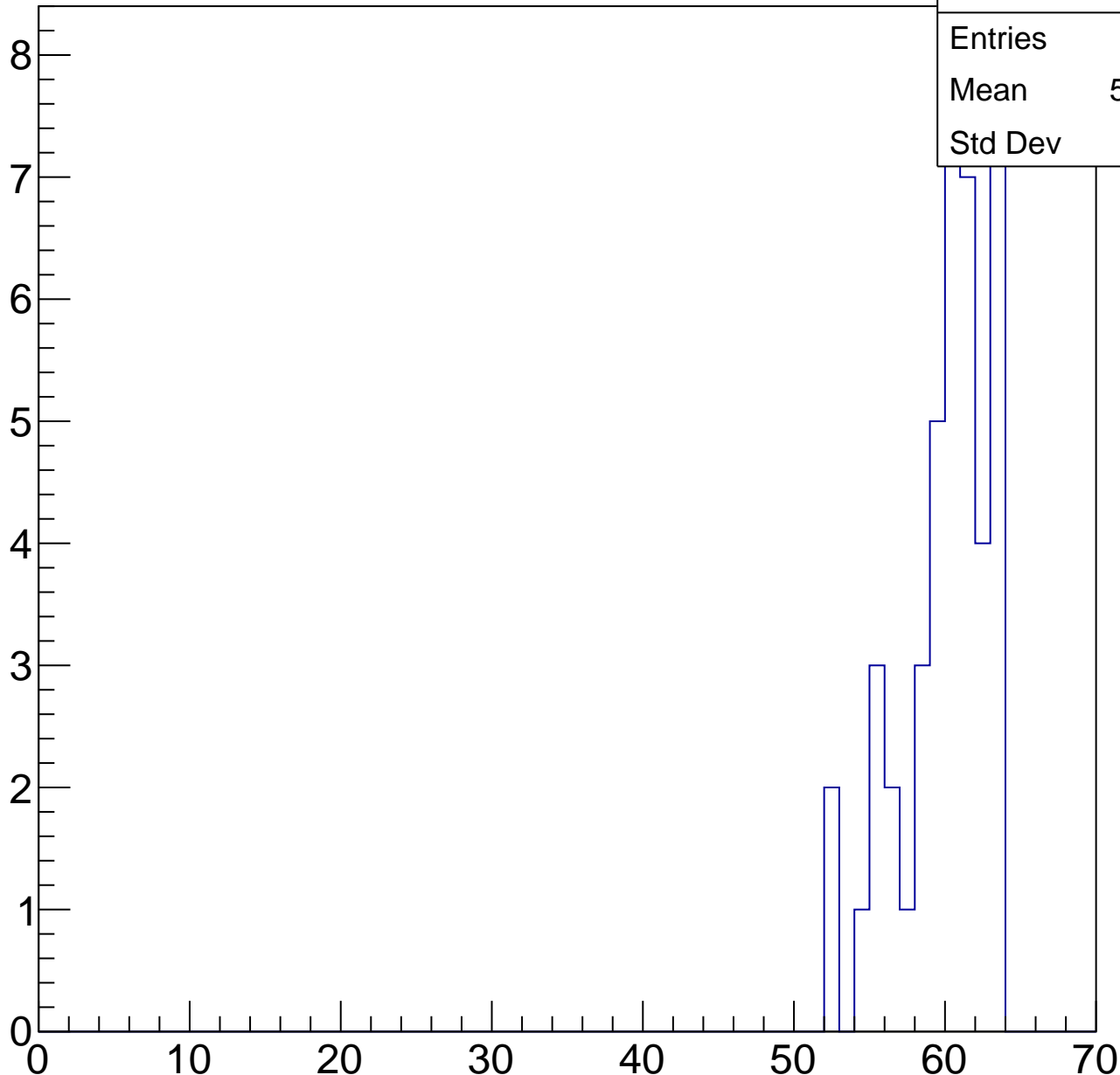
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	44
Mean	59.55
Std Dev	2.95

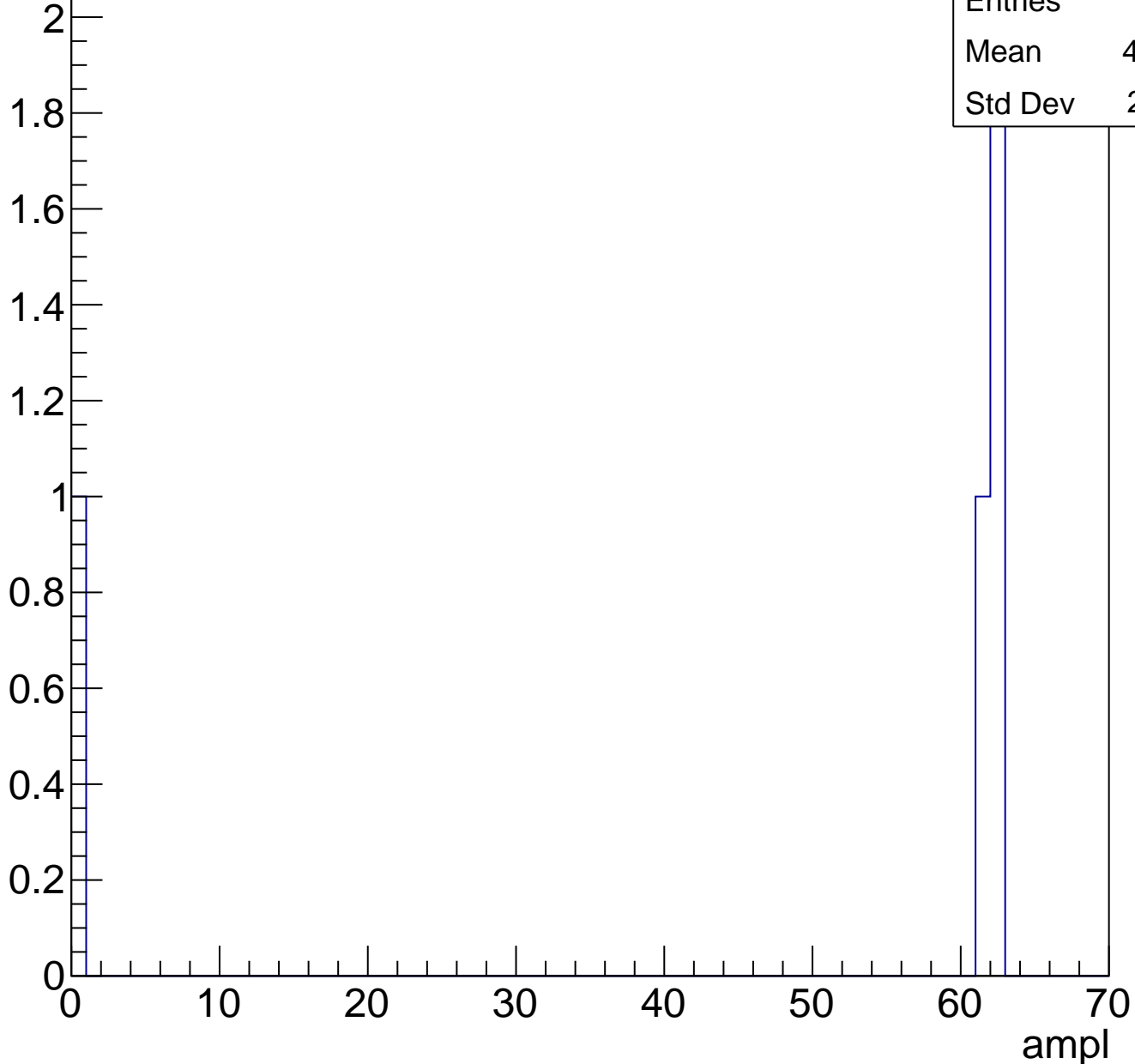
ampl



# B1L101S, U18-ch52, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch52, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U18-ch53, adc0

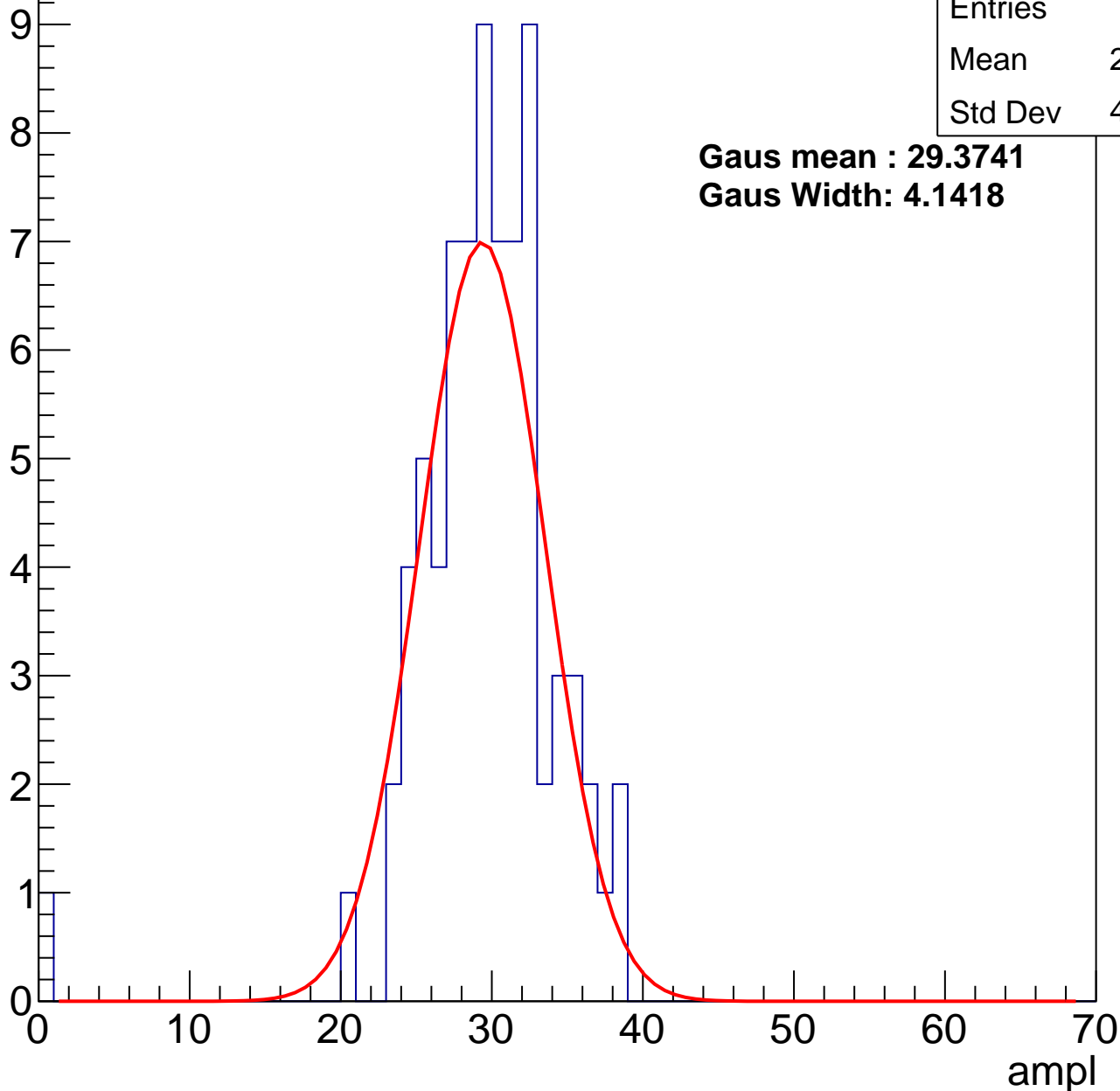
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	29.08
Std Dev	4.999

**Gaus mean : 29.3741**

**Gaus Width: 4.1418**



# B1L101S, U18-ch53, adc1

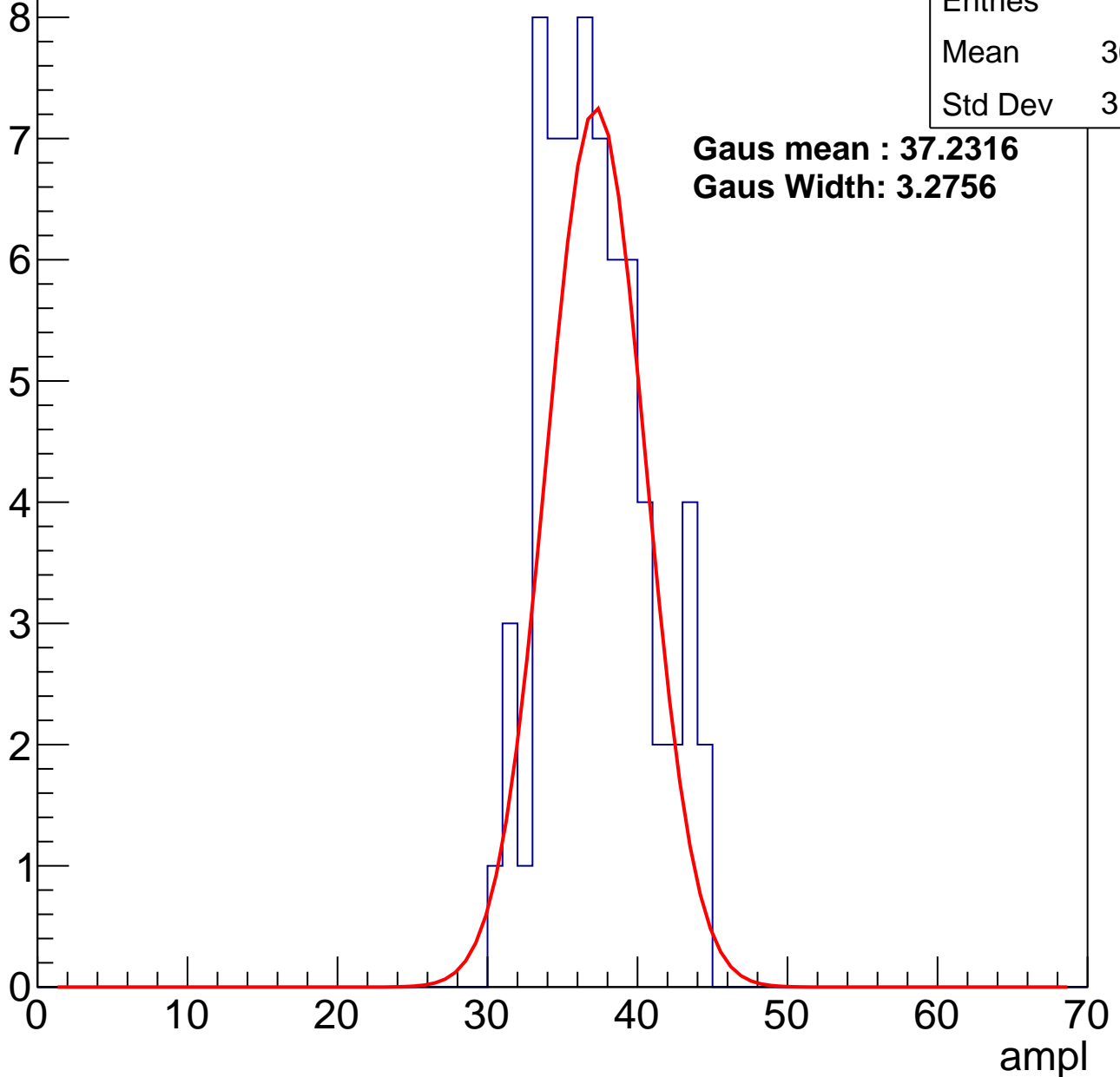
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	36.72
Std Dev	3.416

**Gaus mean : 37.2316**

**Gaus Width: 3.2756**



# B1L101S, U18-ch53, adc2

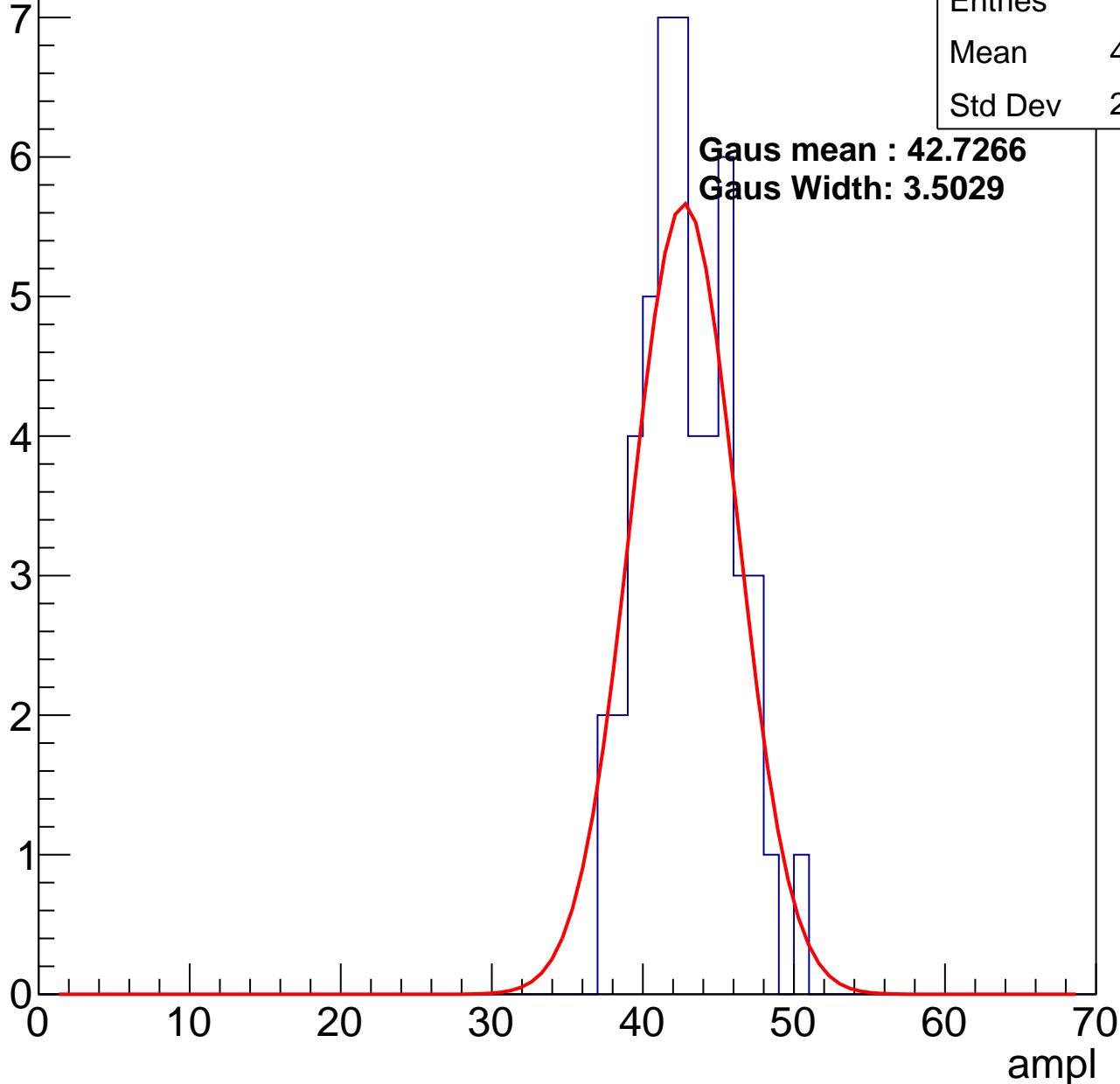
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	49
Mean	42.49
Std Dev	2.963

**Gaus mean : 42.7266**

**Gaus Width: 3.5029**



# B1L101S, U18-ch53, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

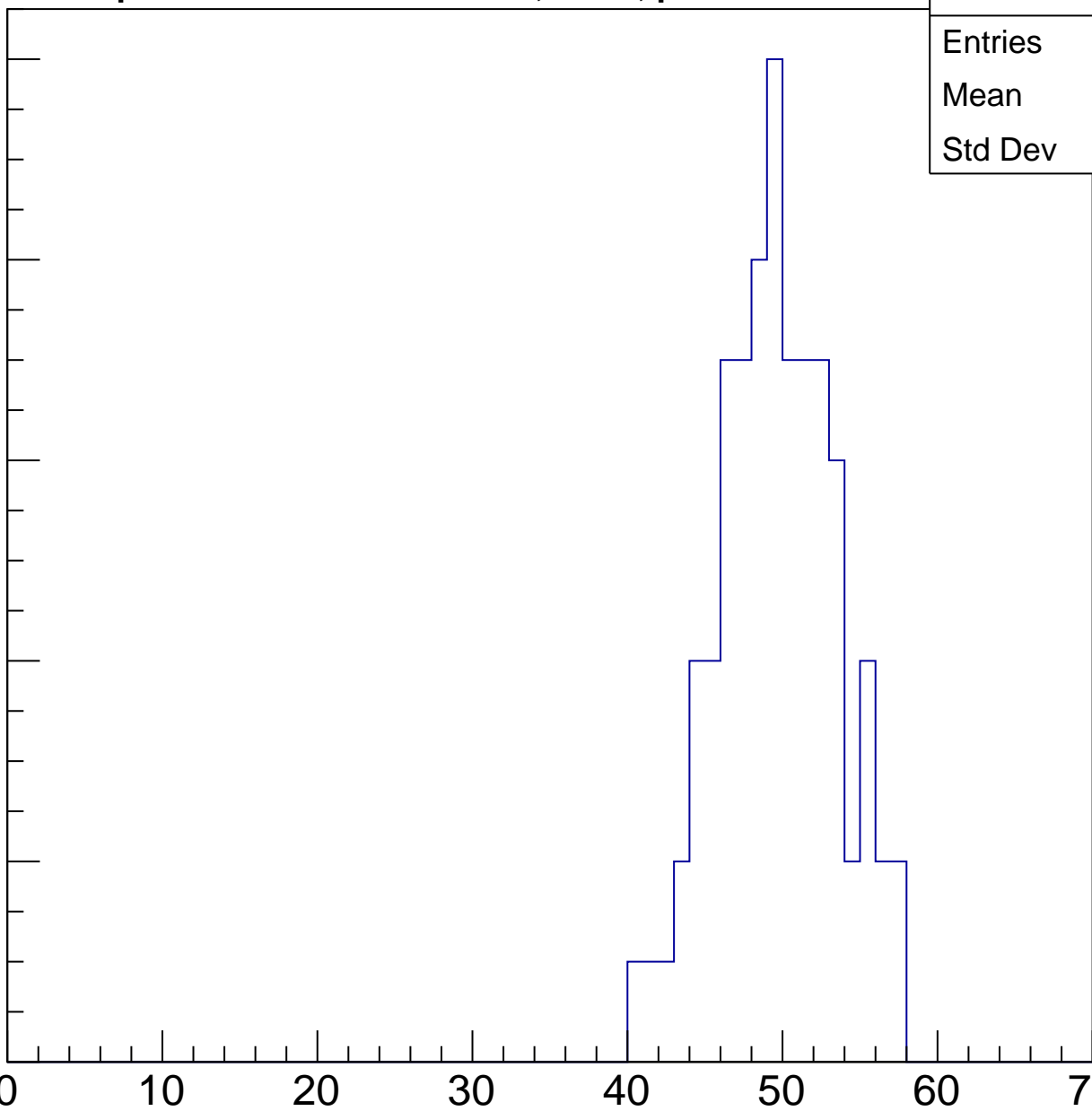
Entries	82
Mean	49.18
Std Dev	3.729

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

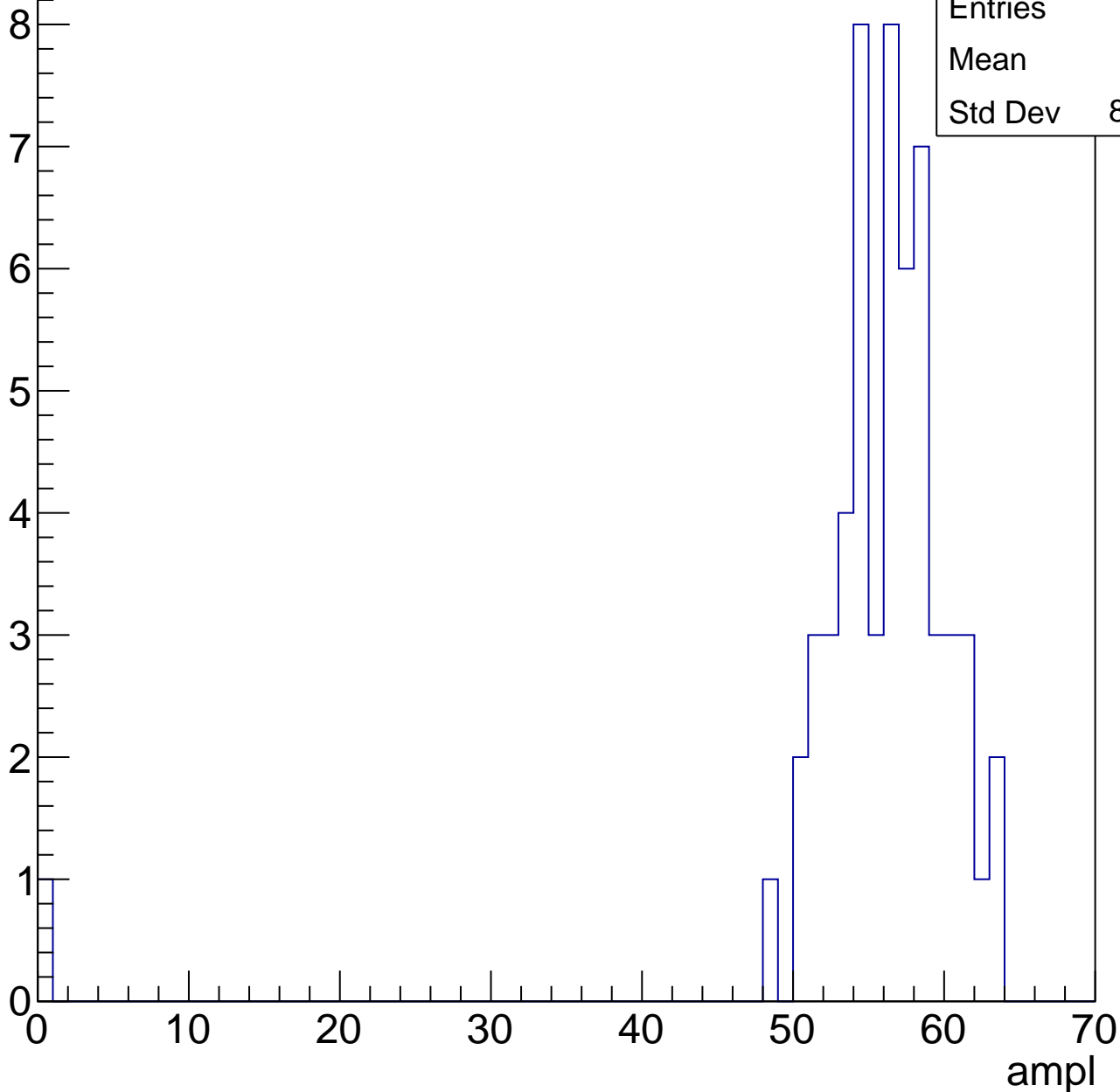


# B1L101S, U18-ch53, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	55
Std Dev	8.015

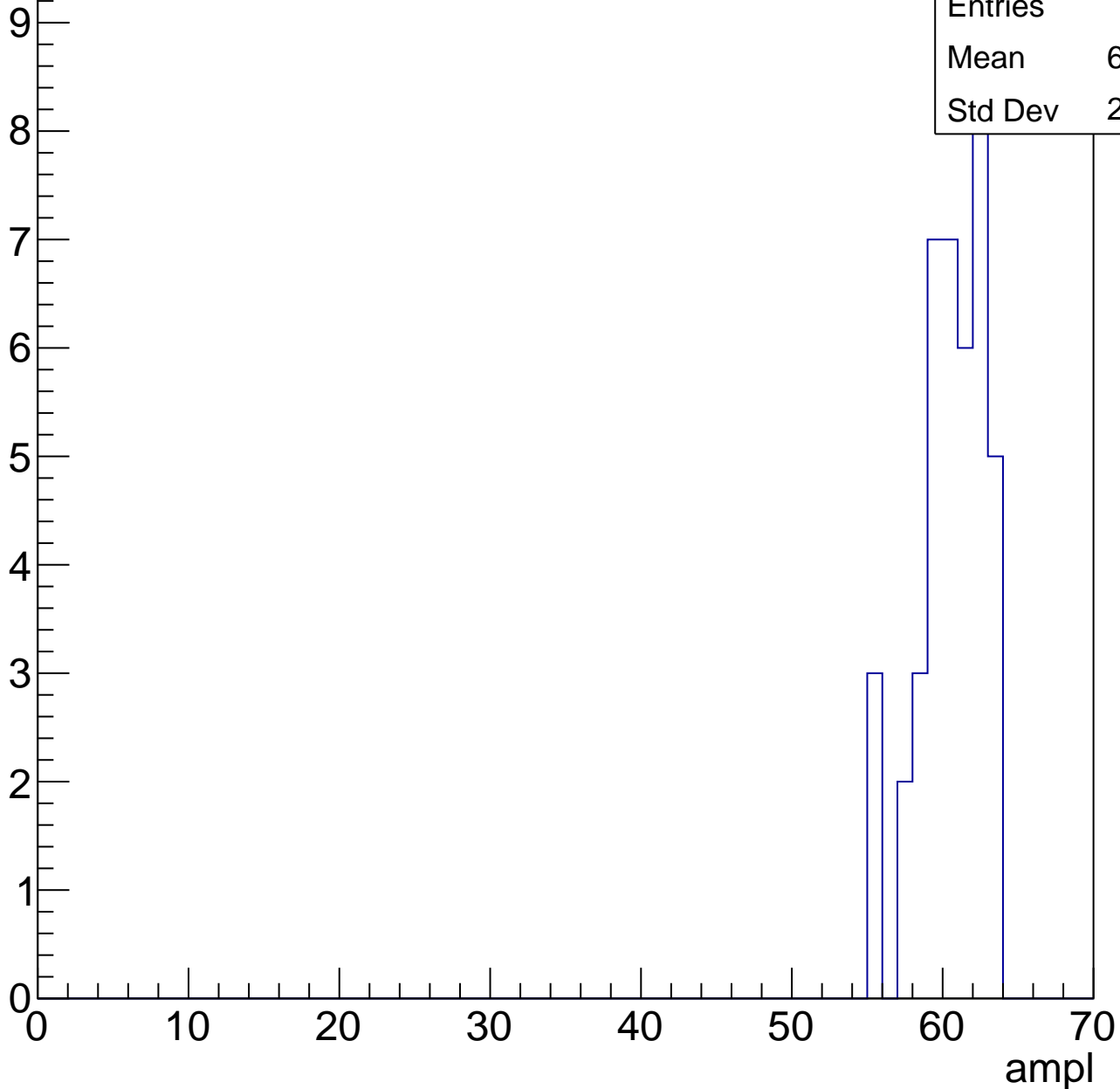


# B1L101S, U18-ch53, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	42
Mean	60.12
Std Dev	2.173



# B1L101S, U18-ch53, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch53, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U18-ch54, adc0

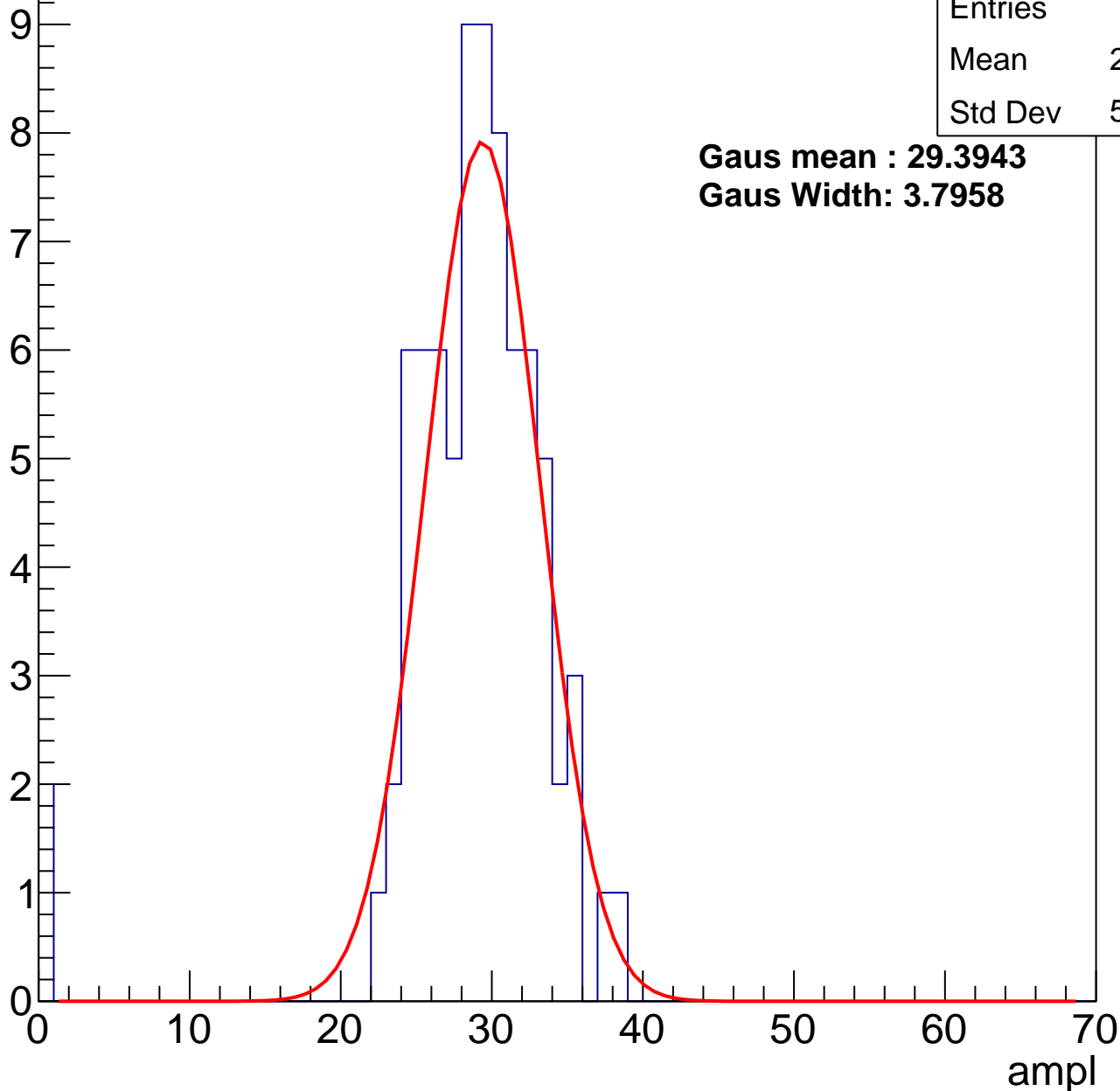
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	78
Mean	28.17
Std Dev	5.714

**Gaus mean : 29.3943**

**Gaus Width: 3.7958**



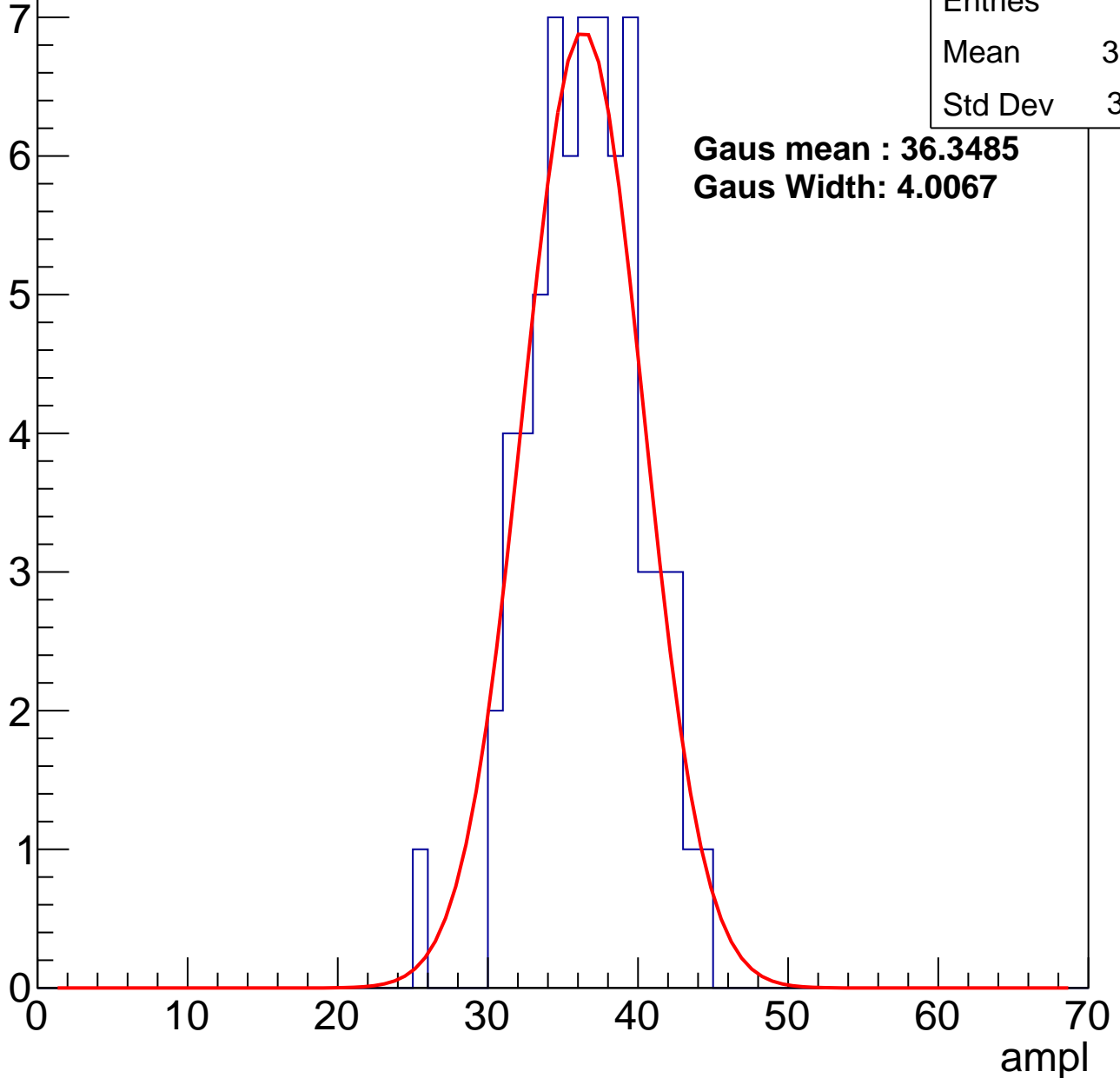
# B1L101S, U18-ch54, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	36.09
Std Dev	3.611

**Gaus mean : 36.3485**  
**Gaus Width: 4.0067**



# B1L101S, U18-ch54, adc2

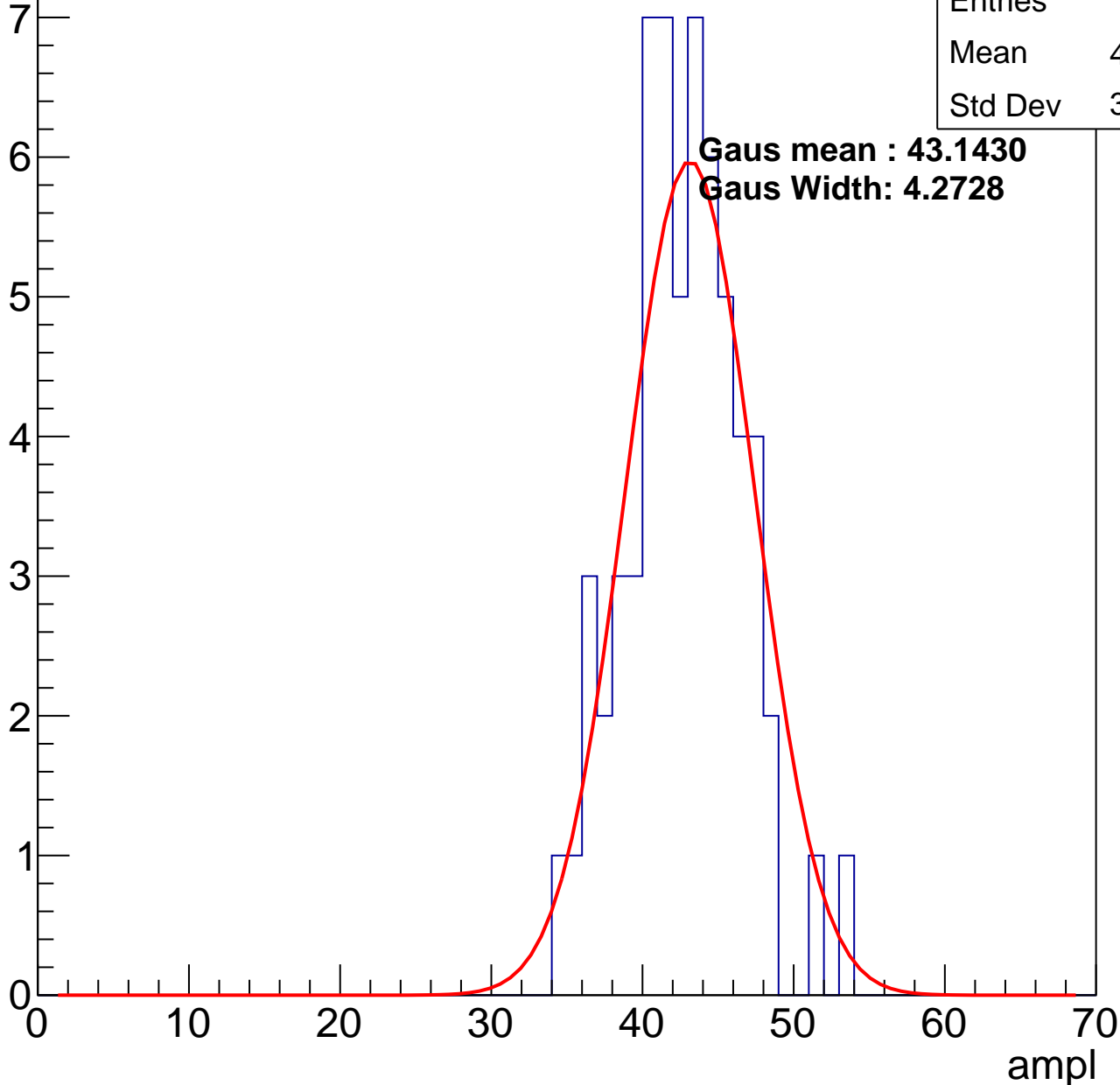
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	42.27
Std Dev	3.789

**Gaus mean : 43.1430**

**Gaus Width: 4.2728**

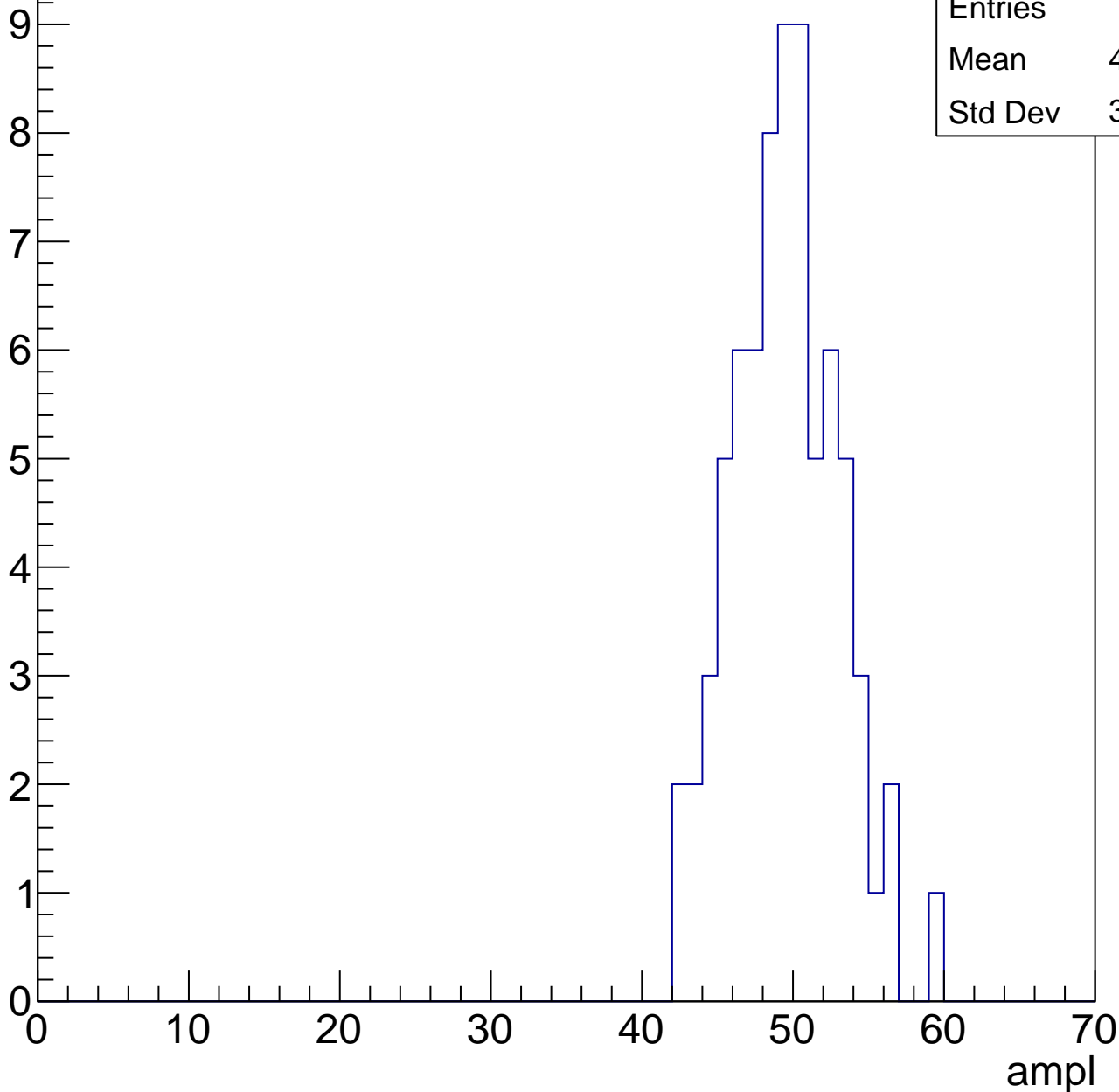


# B1L101S, U18-ch54, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

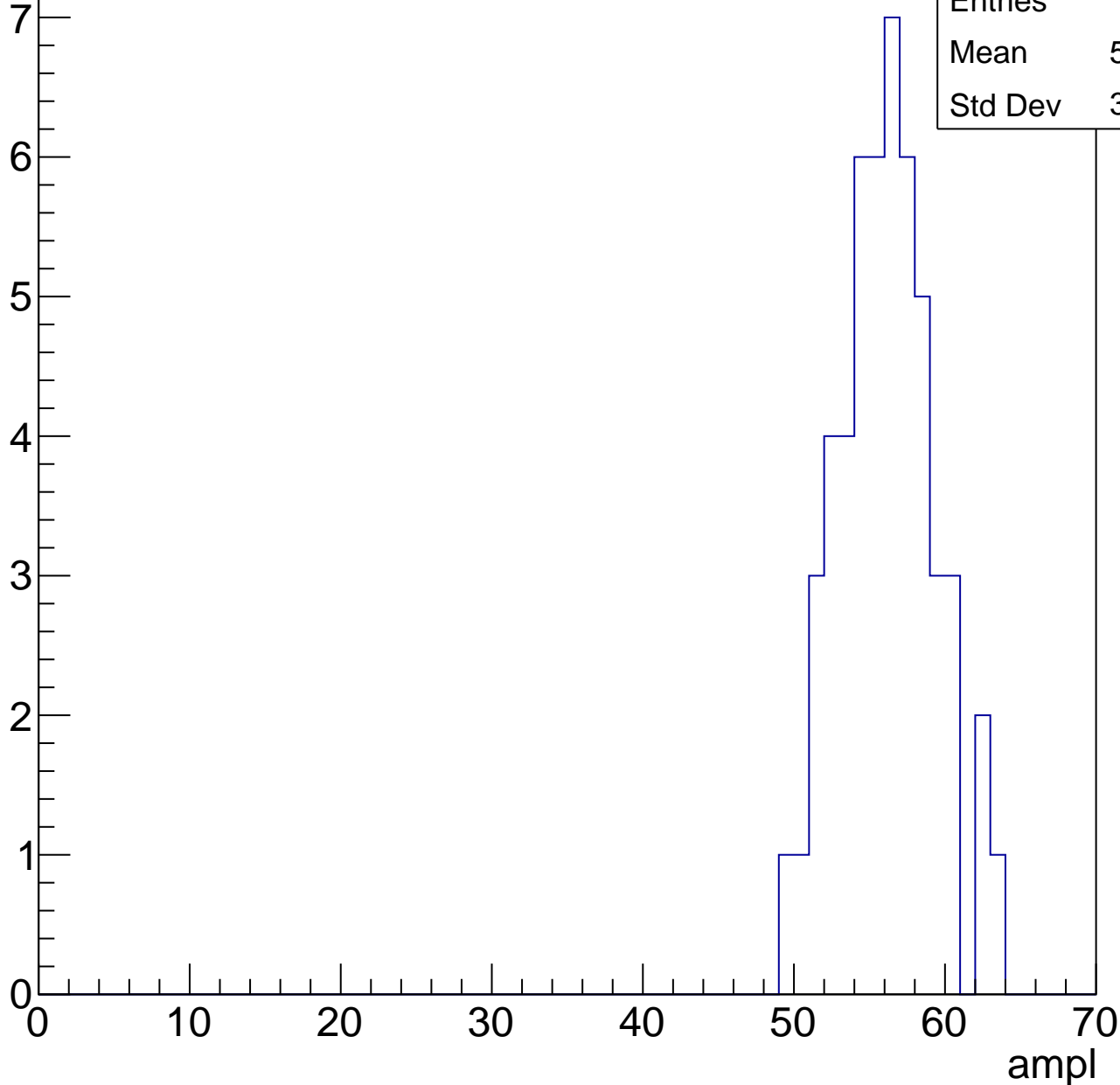
Entries	73
Mean	49.04
Std Dev	3.478



# B1L101S, U18-ch54, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



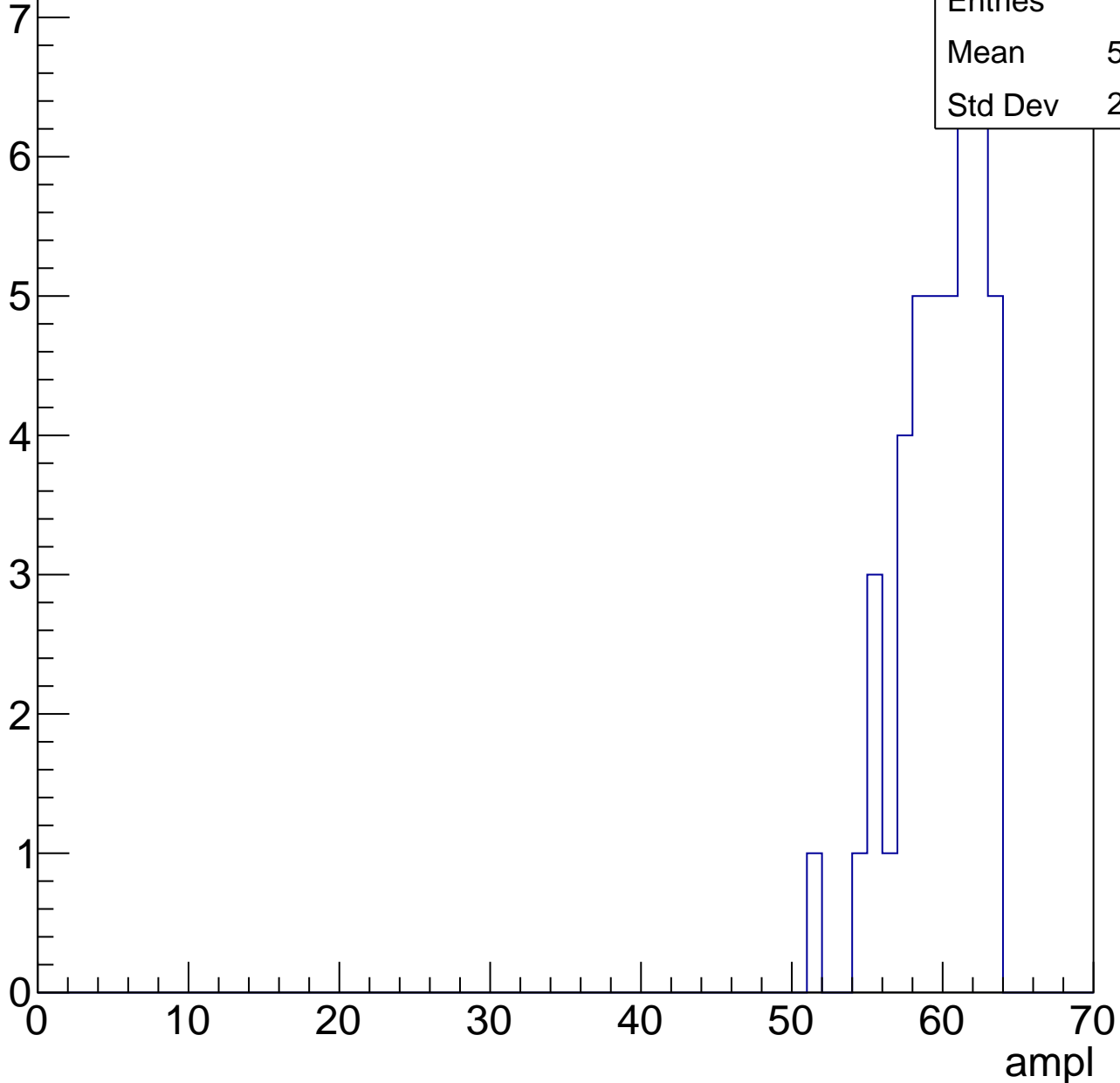
Entries	52
Mean	55.65
Std Dev	3.119

# B1L101S, U18-ch54, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

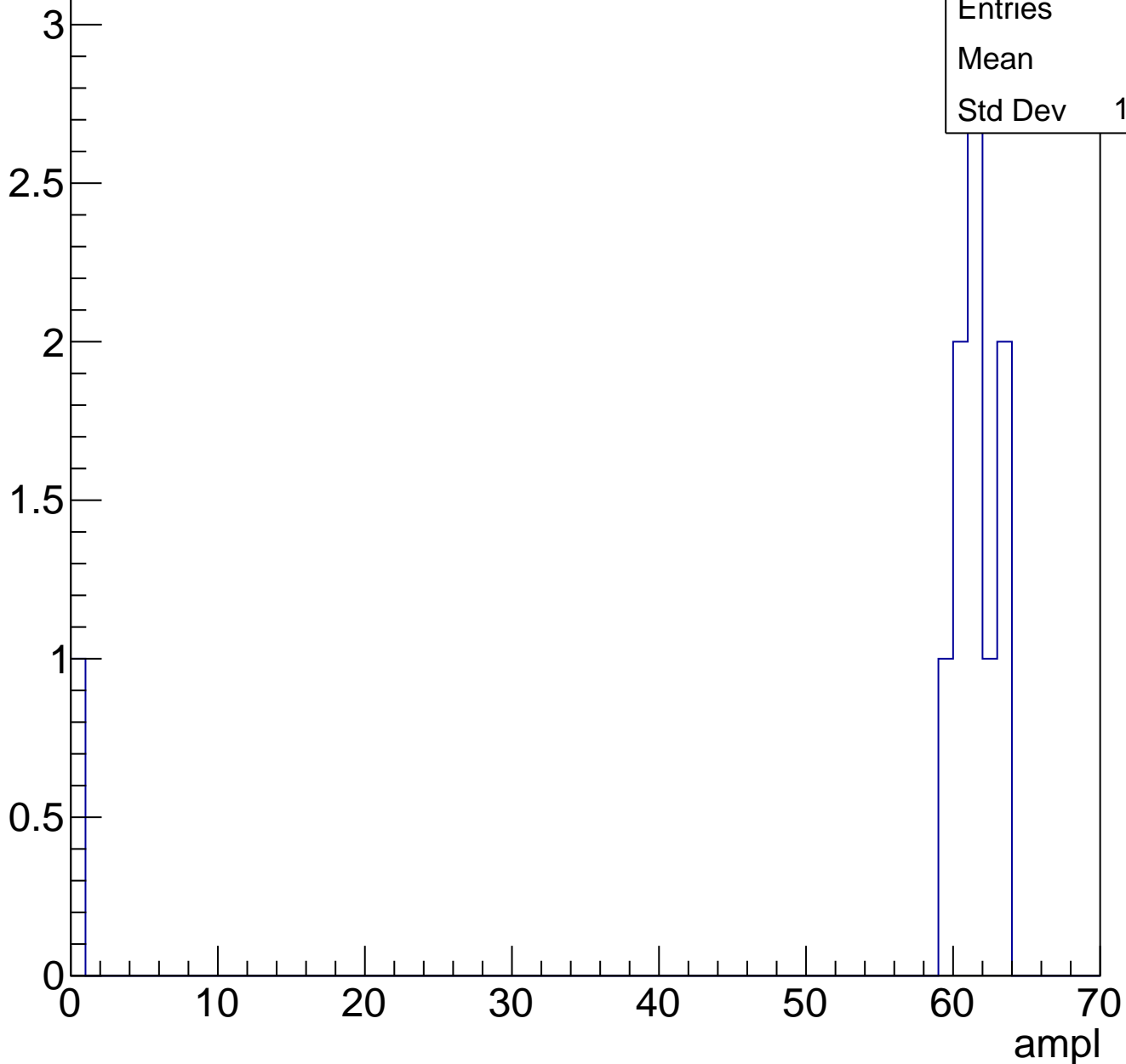
Entries	44
Mean	59.43
Std Dev	2.758



# B1L101S, U18-ch54, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

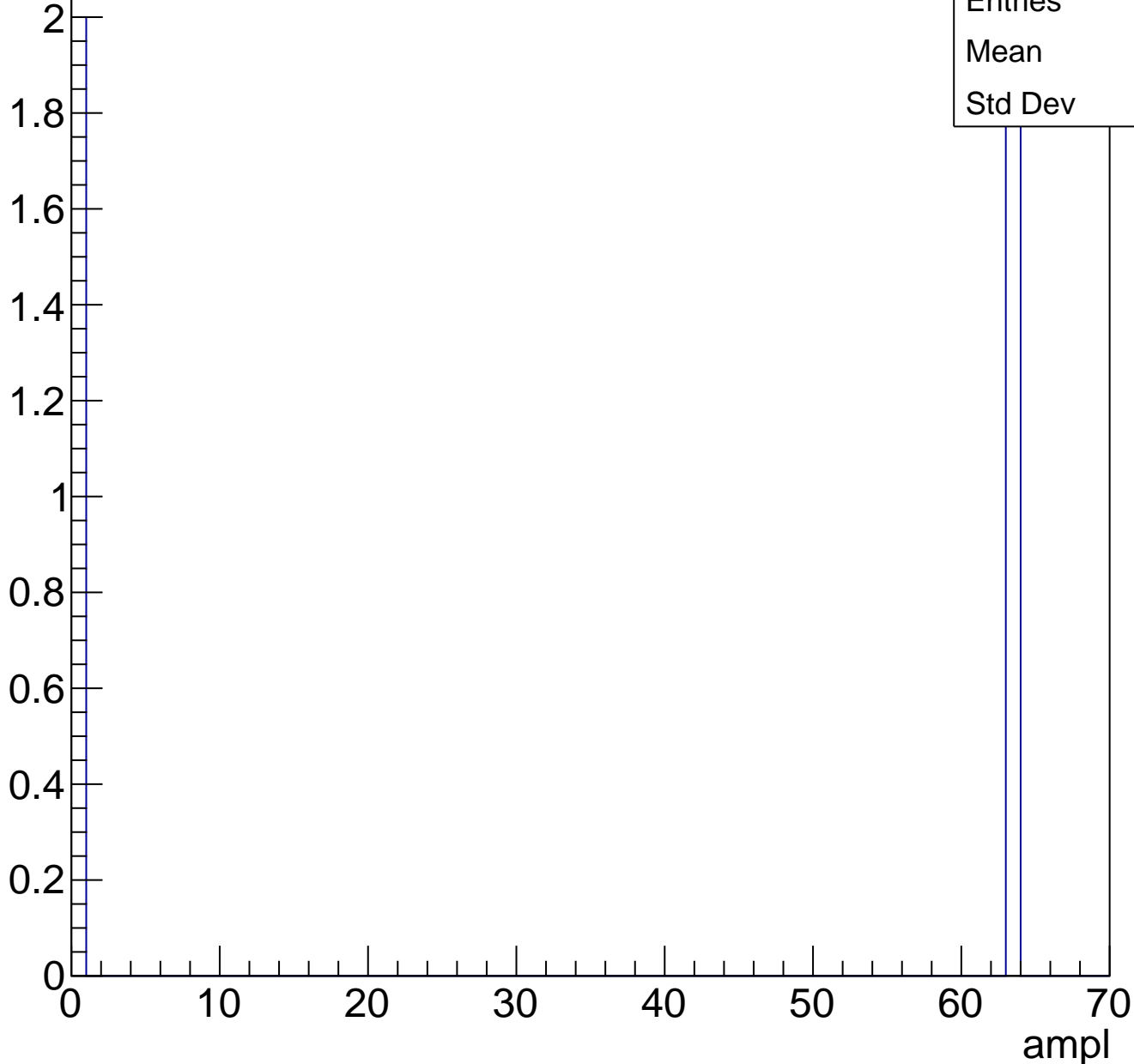




# B1L101S, U18-ch54, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch55, adc0

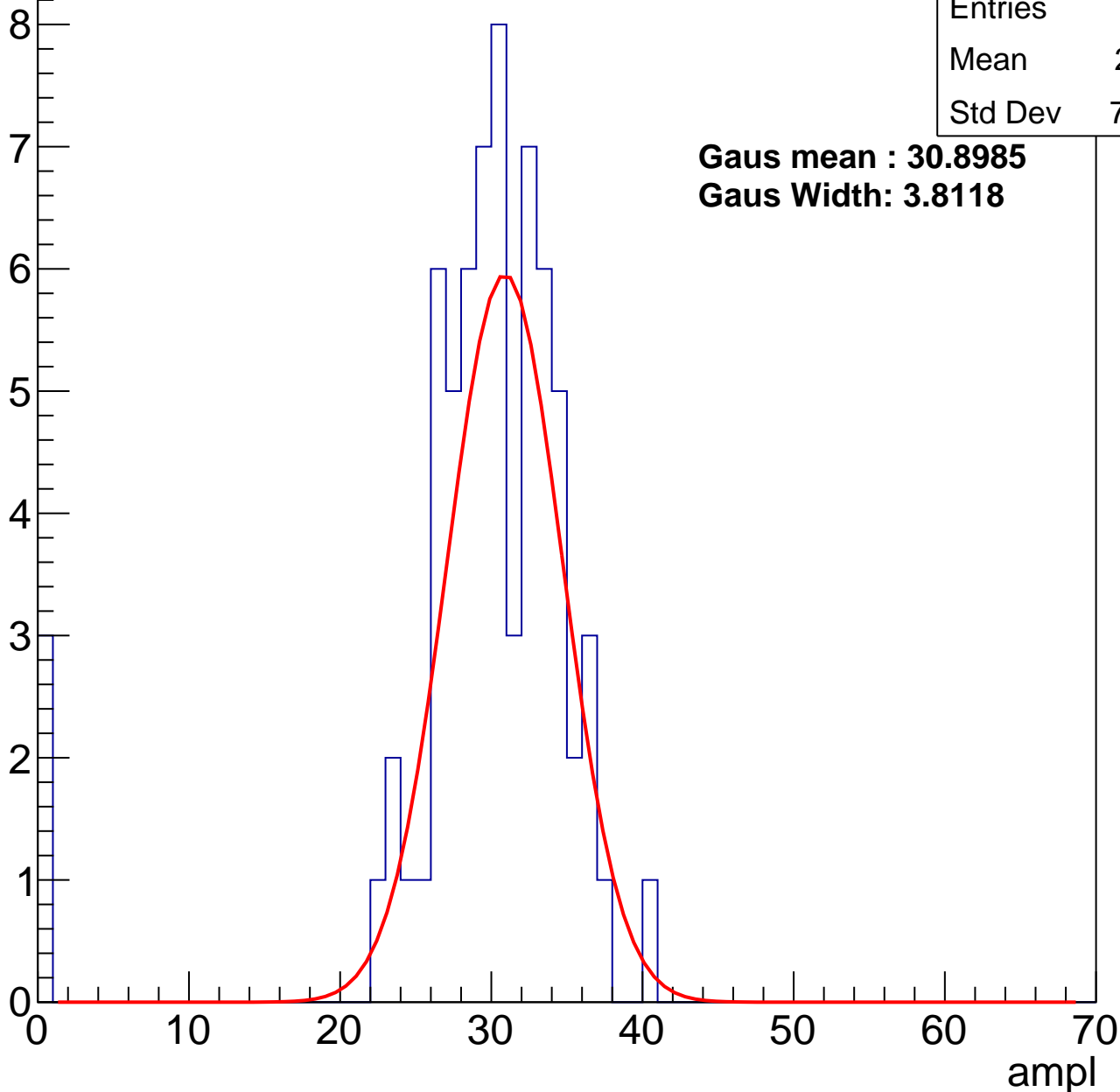
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	28.81
Std Dev	7.144

**Gaus mean : 30.8985**

**Gaus Width: 3.8118**



# B1L101S, U18-ch55, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	80
Mean	37.49
Std Dev	3.765

**Gaus mean : 37.9213**

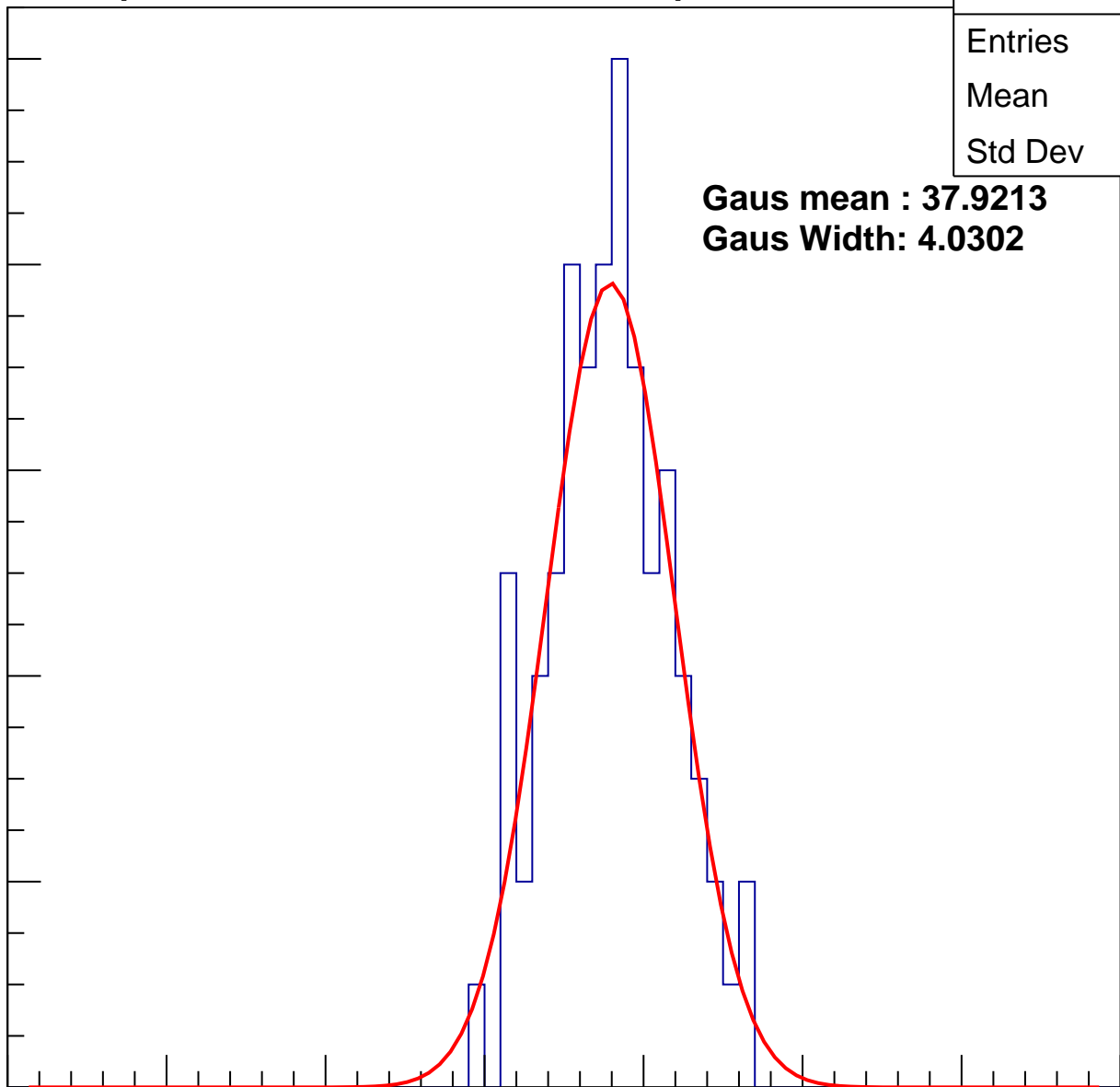
**Gaus Width: 4.0302**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L101S, U18-ch55, adc2

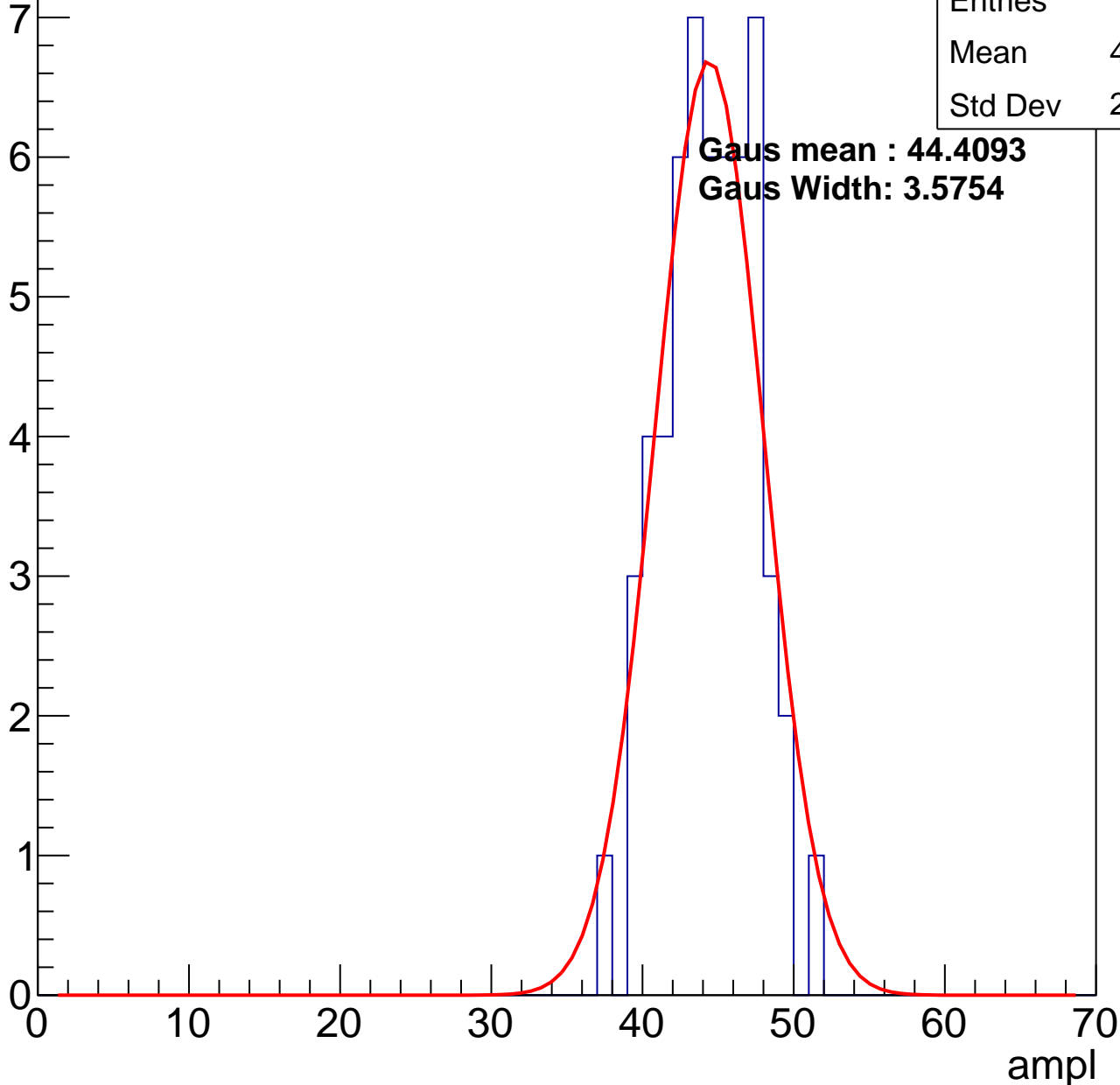
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	43.98
Std Dev	2.973

**Gaus mean : 44.4093**

**Gaus Width: 3.5754**

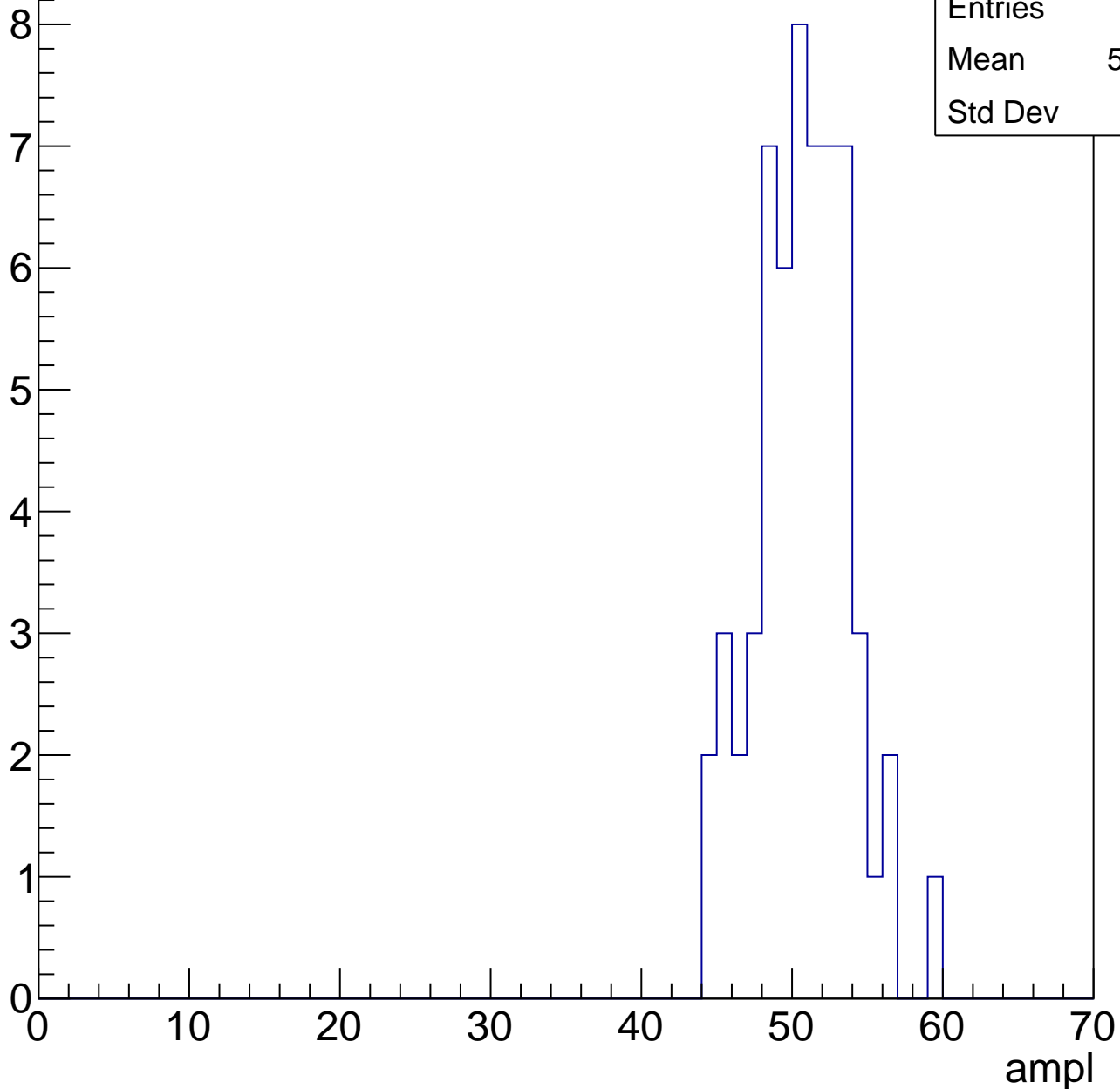


# B1L101S, U18-ch55, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

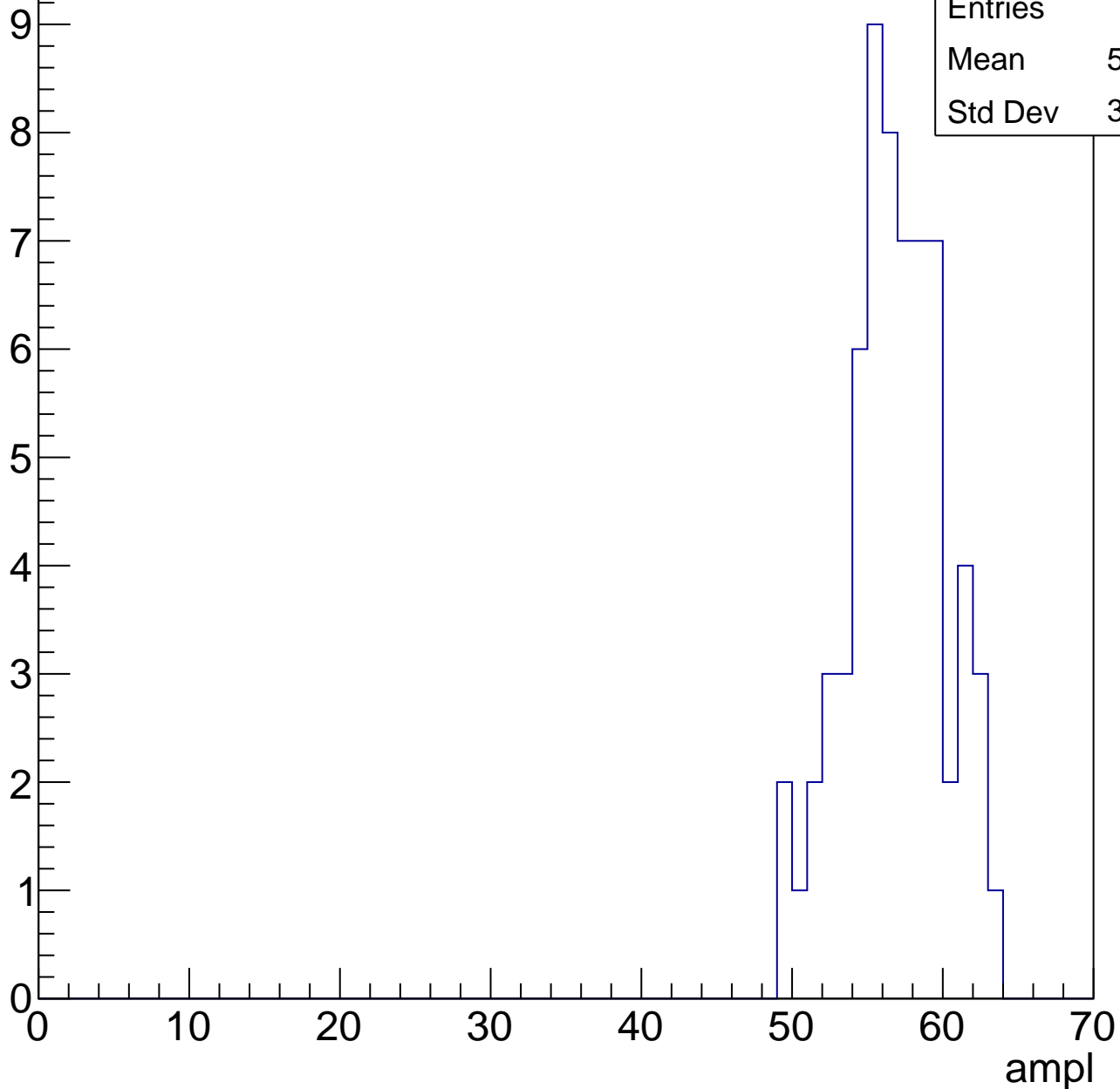
Entries	59
Mean	50.27
Std Dev	3.08



# B1L101S, U18-ch55, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch55, adc5

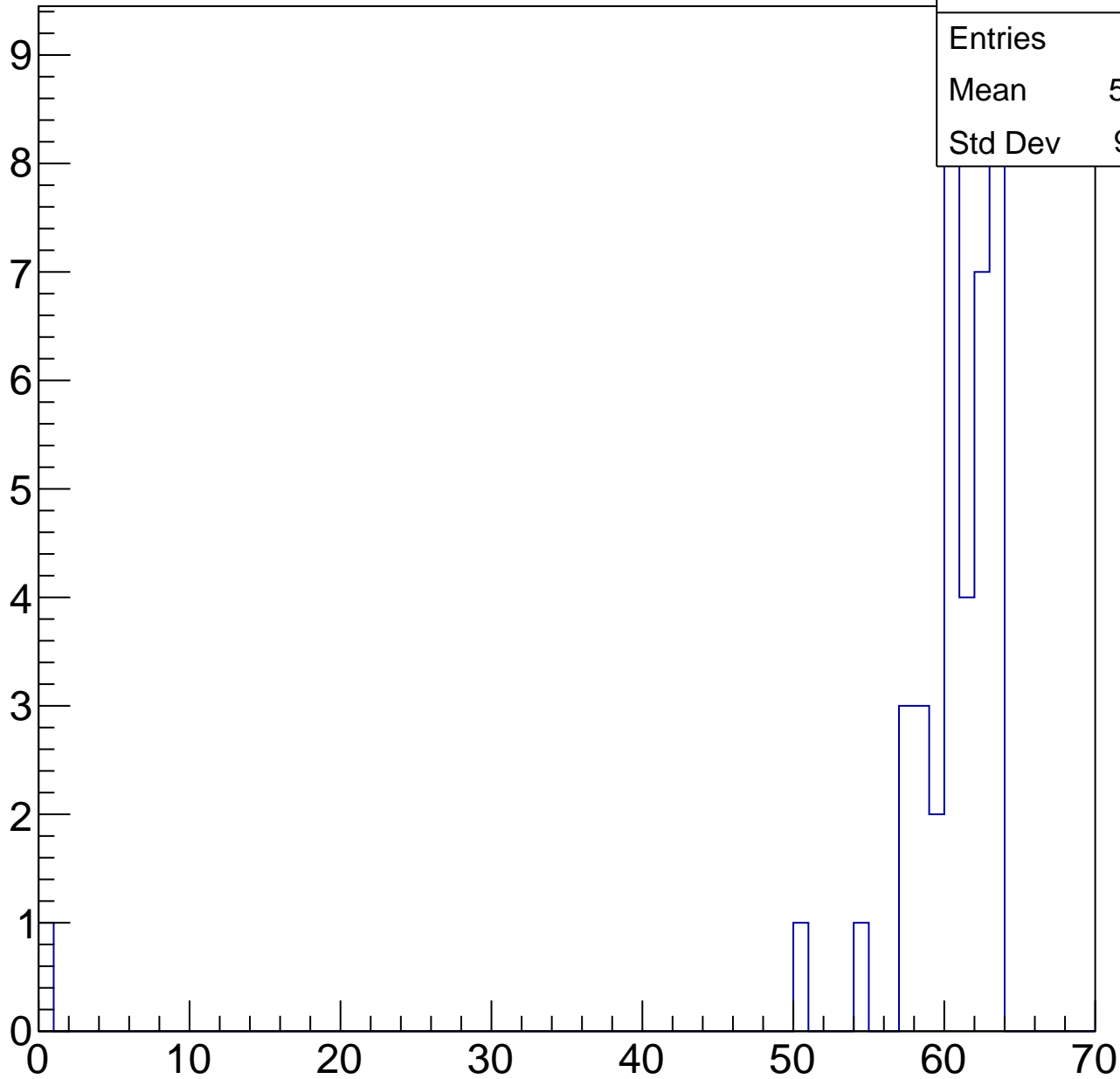
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	39
Mean	58.77
Std Dev	9.911

ampl



# B1L101S, U18-ch55, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	61
Std Dev	0

ampl



# B1L101S, U18-ch55, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch56, adc0

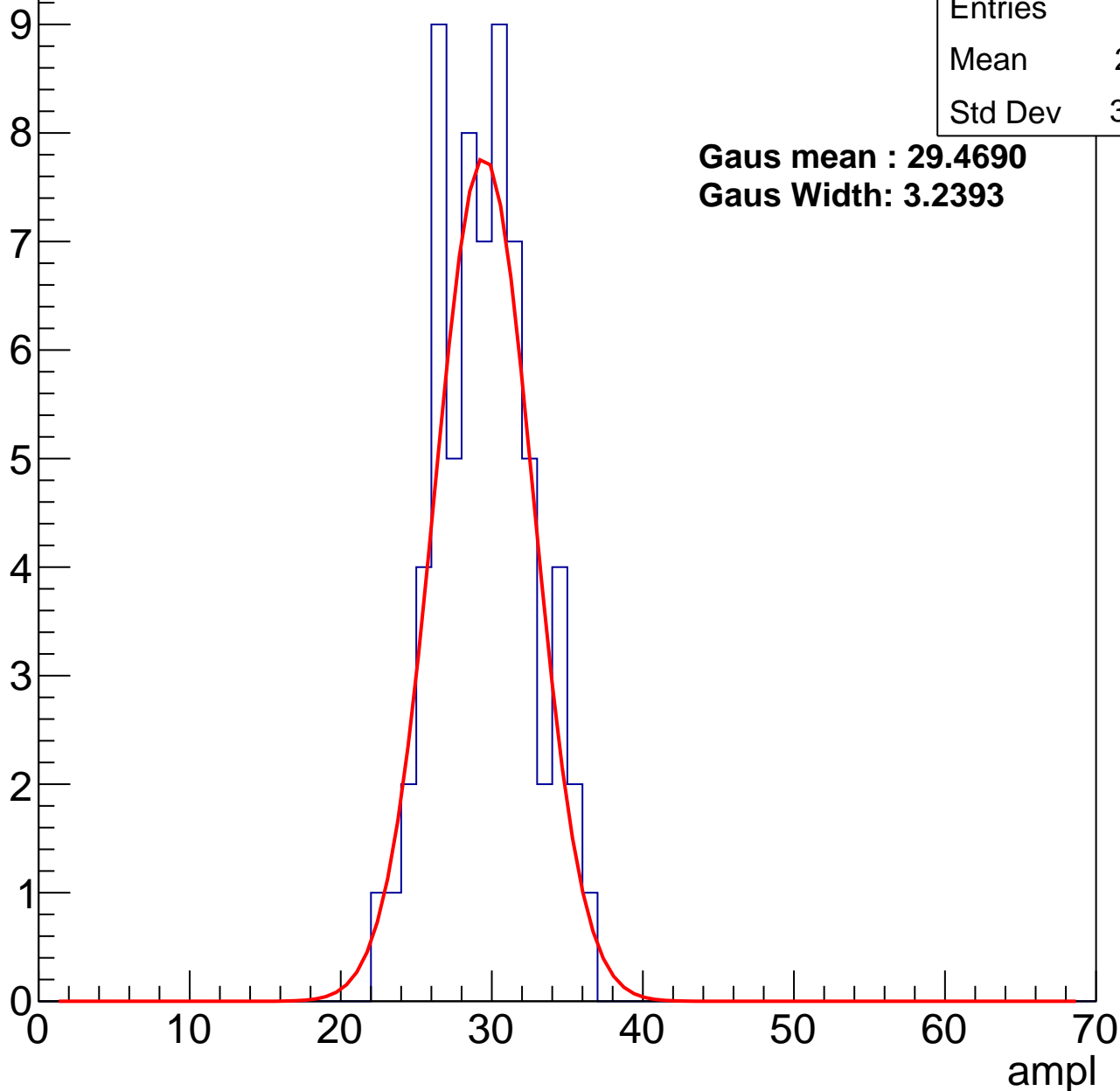
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	29.01
Std Dev	3.098

**Gaus mean : 29.4690**

**Gaus Width: 3.2393**



# B1L101S, U18-ch56, adc1

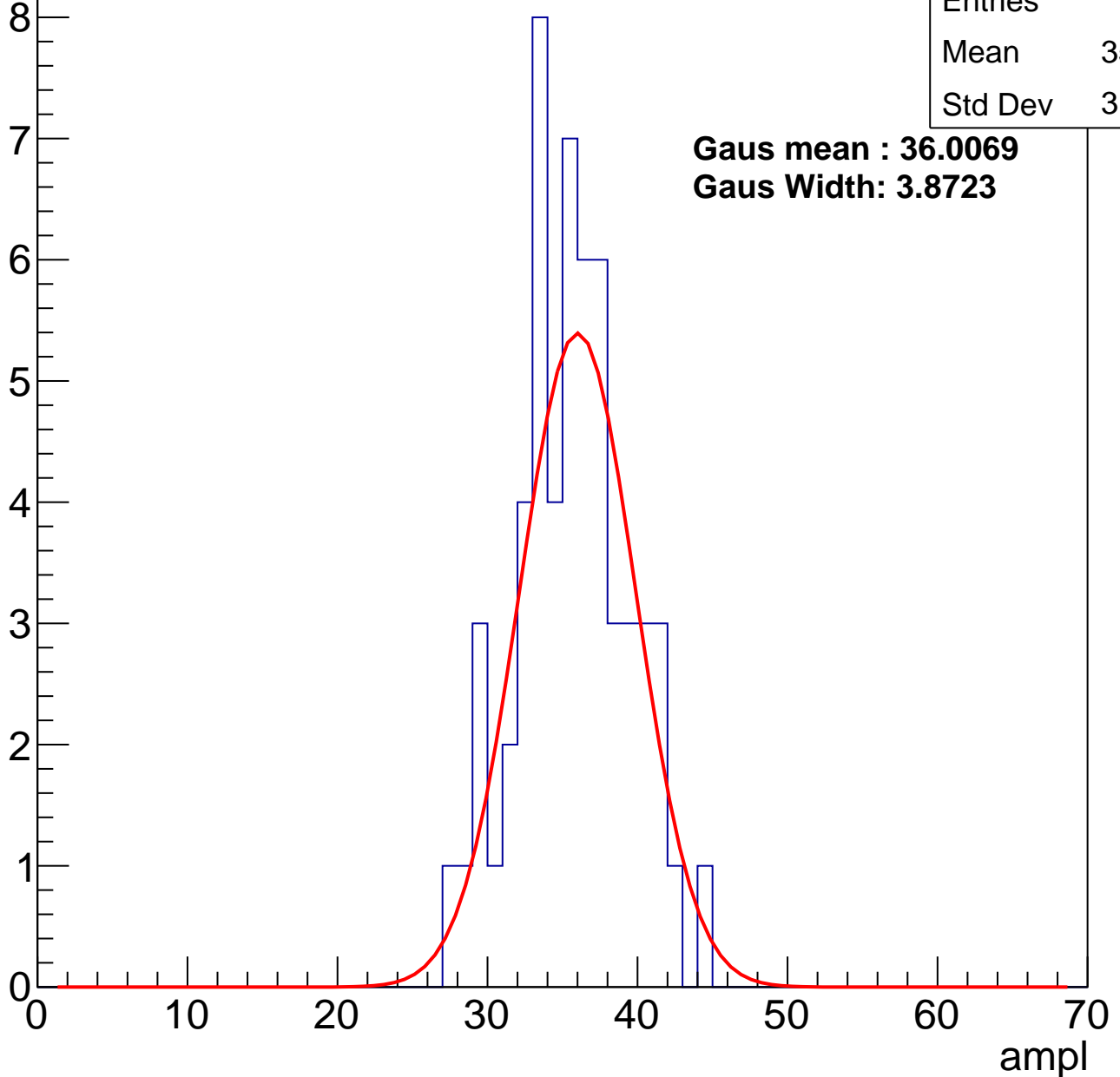
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	35.18
Std Dev	3.666

**Gaus mean : 36.0069**

**Gaus Width: 3.8723**



# B1L101S, U18-ch56, adc2

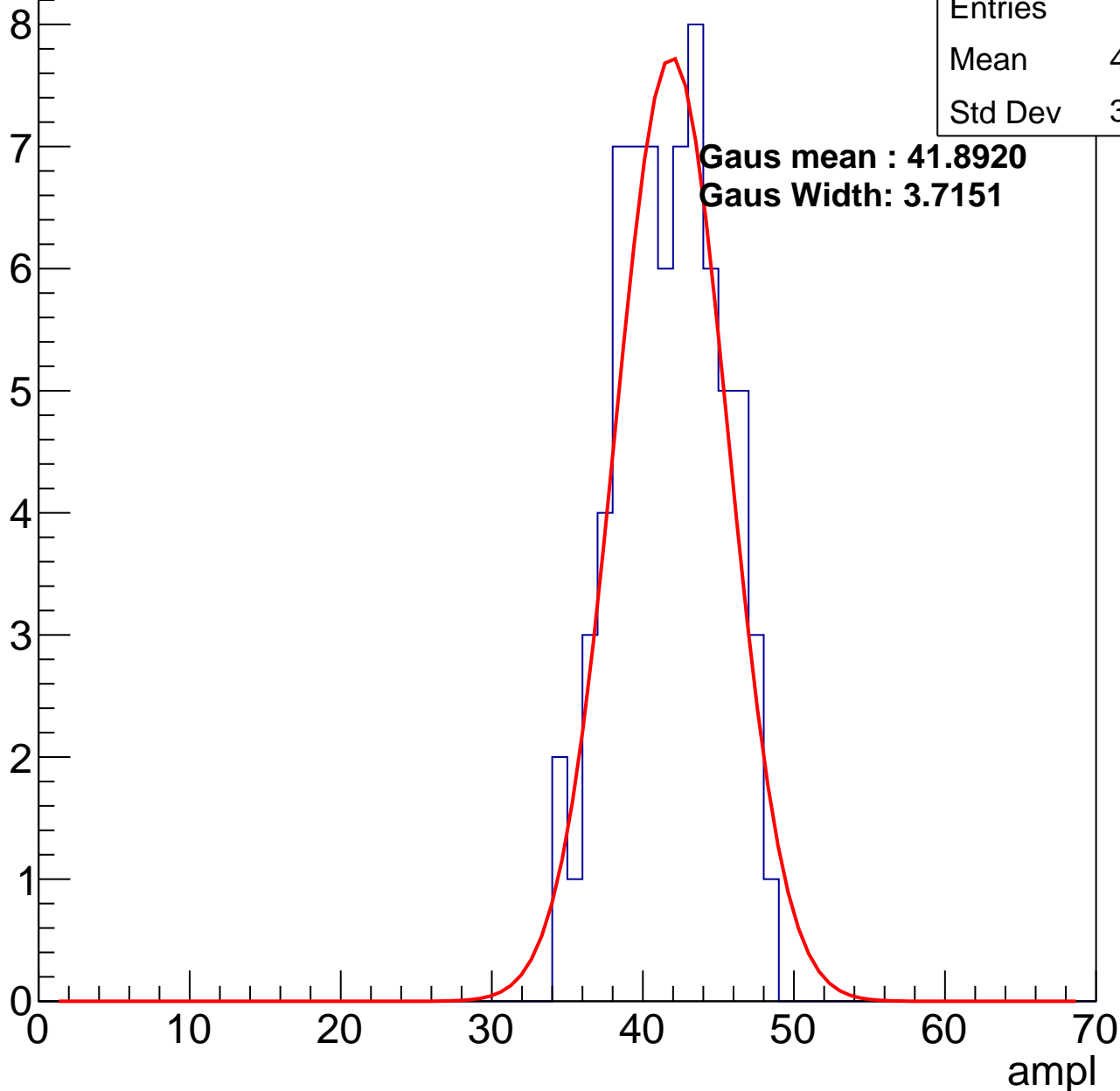
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	41.25
Std Dev	3.378

**Gaus mean : 41.8920**

**Gaus Width: 3.7151**

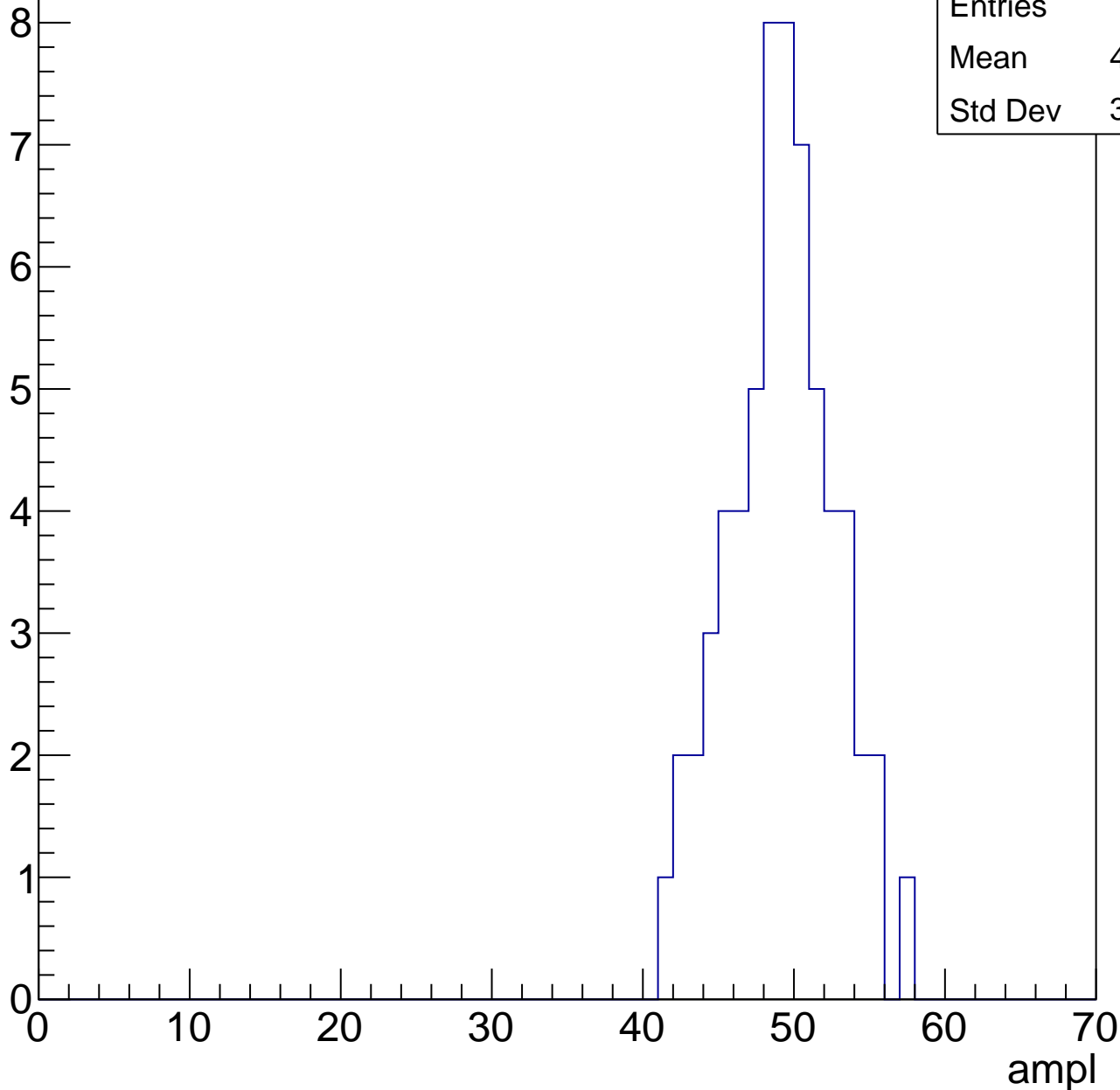


# B1L101S, U18-ch56, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	48.68
Std Dev	3.463

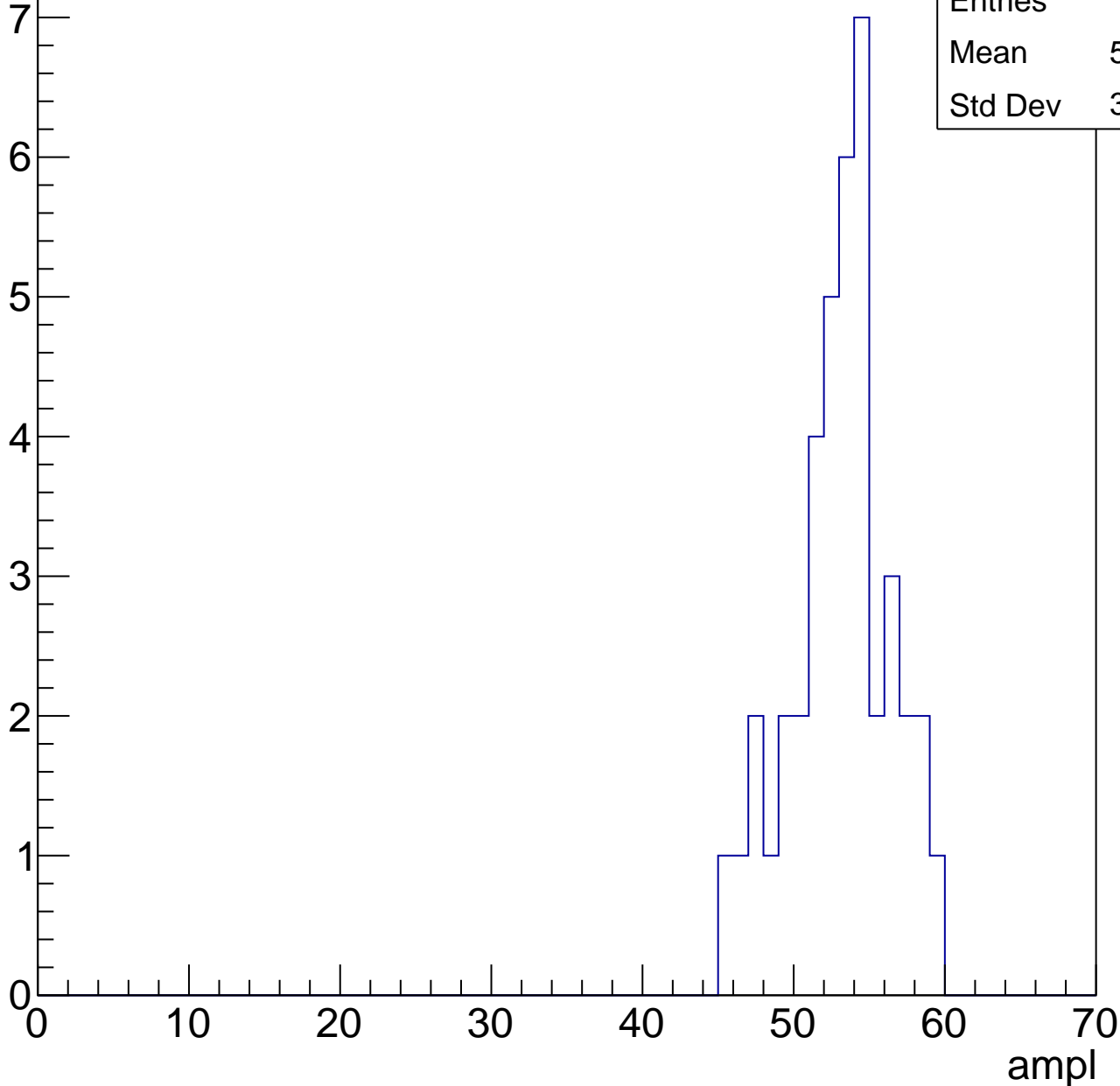


# B1L101S, U18-ch56, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	41
Mean	52.63
Std Dev	3.259

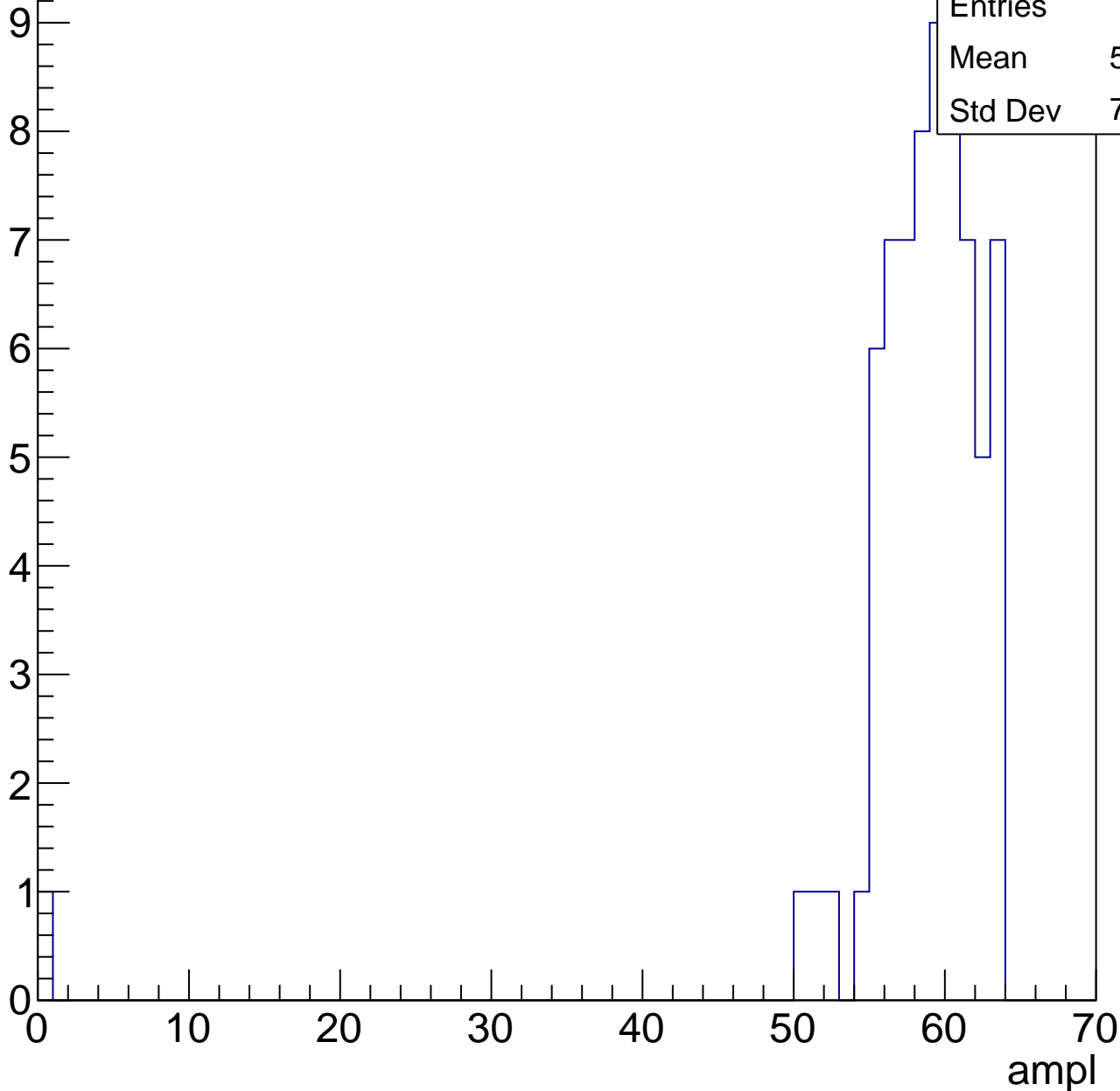


# B1L101S, U18-ch56, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	57.73
Std Dev	7.536

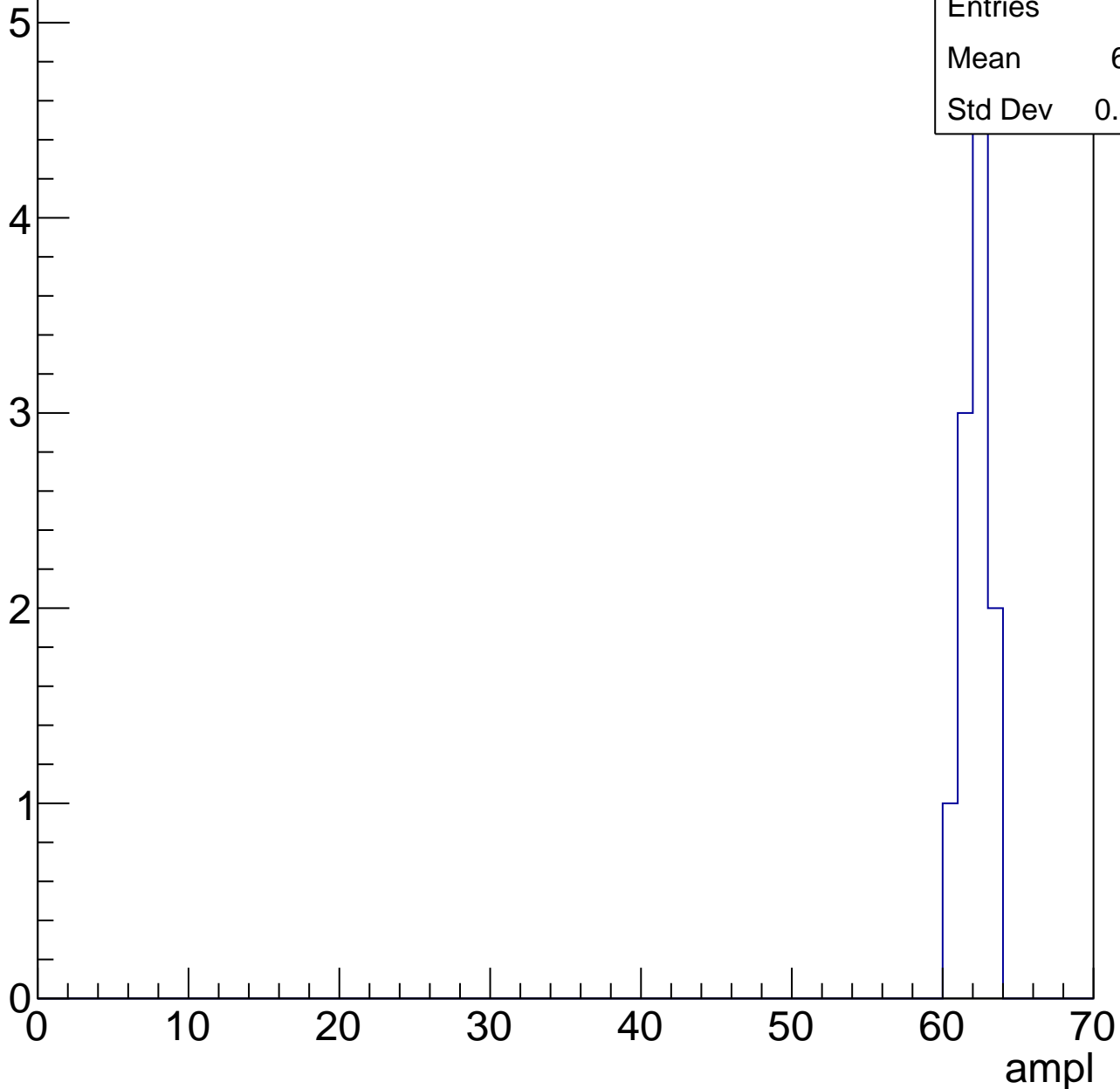


# B1L101S, U18-ch56, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	11
Mean	61.73
Std Dev	0.8624





# B1L101S, U18-ch56, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch57, adc0

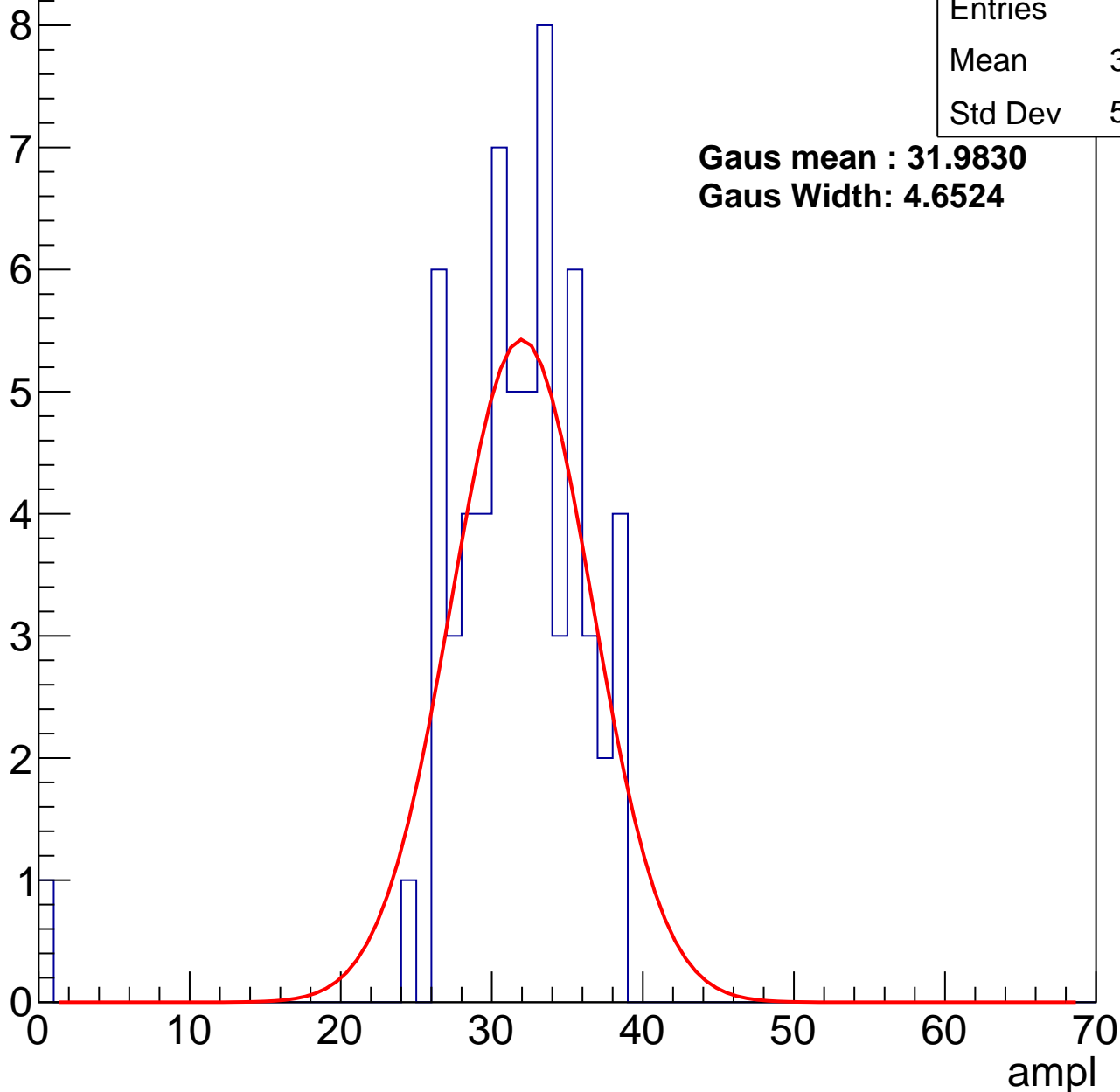
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	31.03
Std Dev	5.343

**Gaus mean : 31.9830**

**Gaus Width: 4.6524**



# B1L101S, U18-ch57, adc1

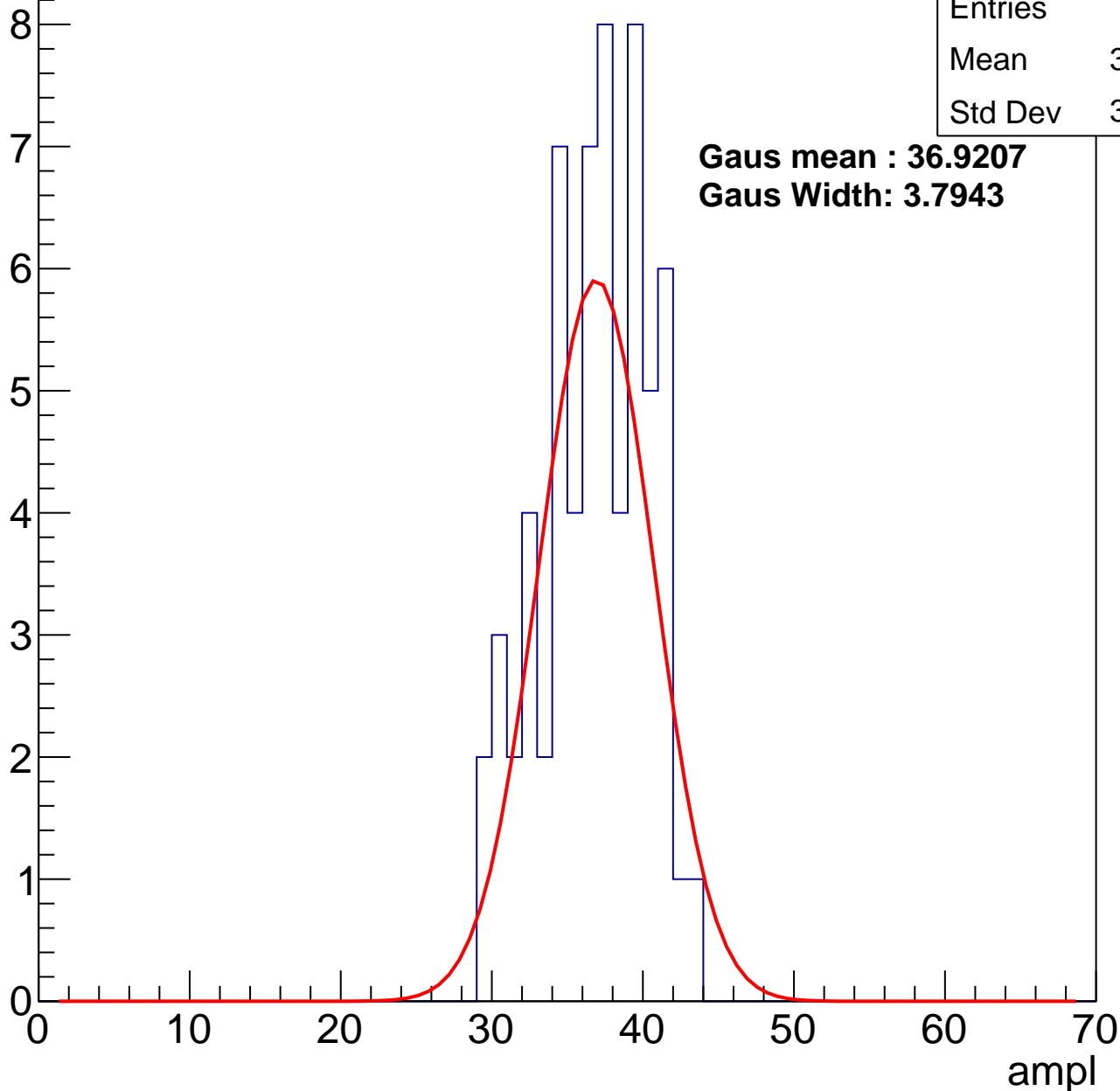
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	36.33
Std Dev	3.478

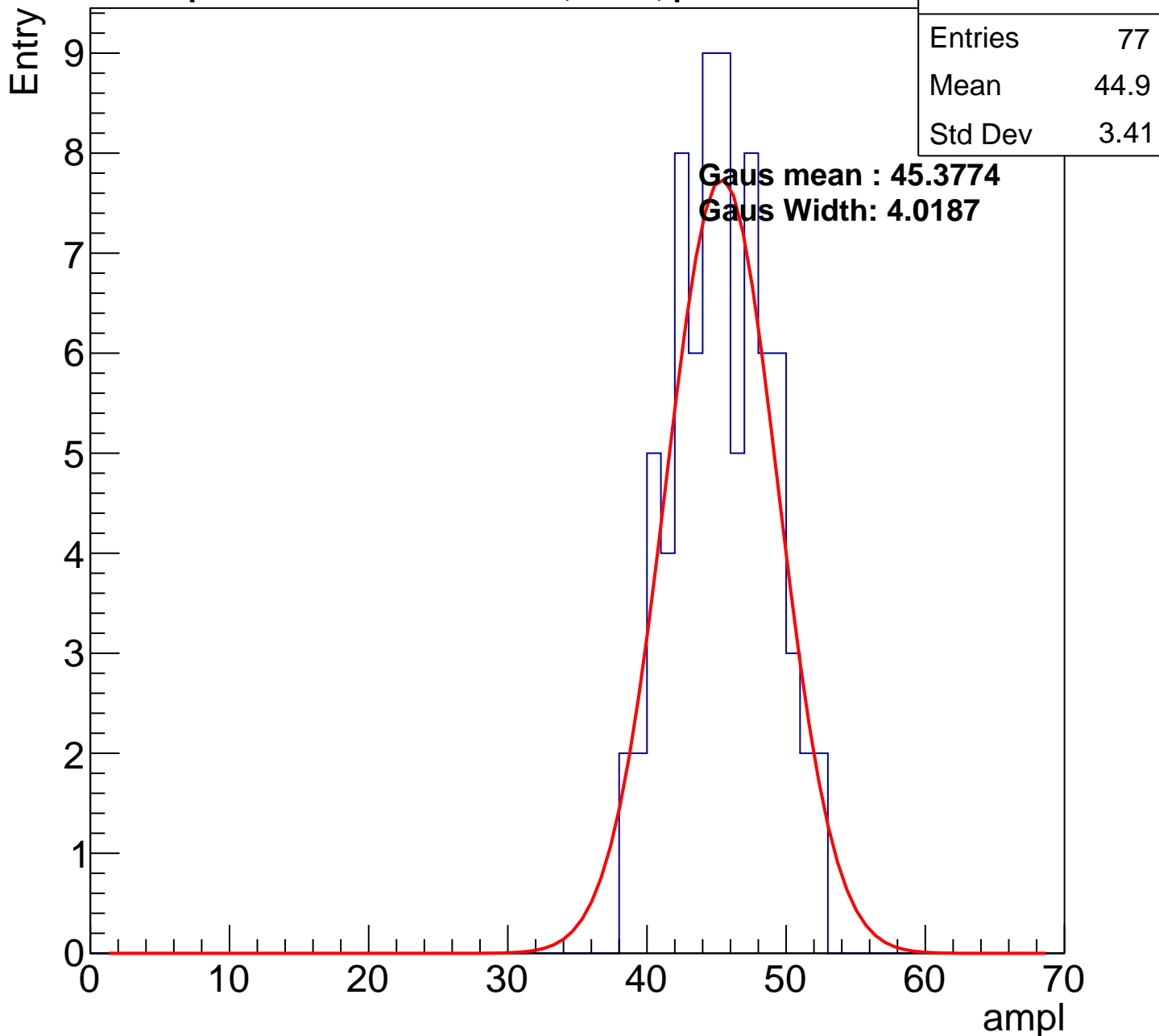
**Gaus mean : 36.9207**

**Gaus Width: 3.7943**



# B1L101S, U18-ch57, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

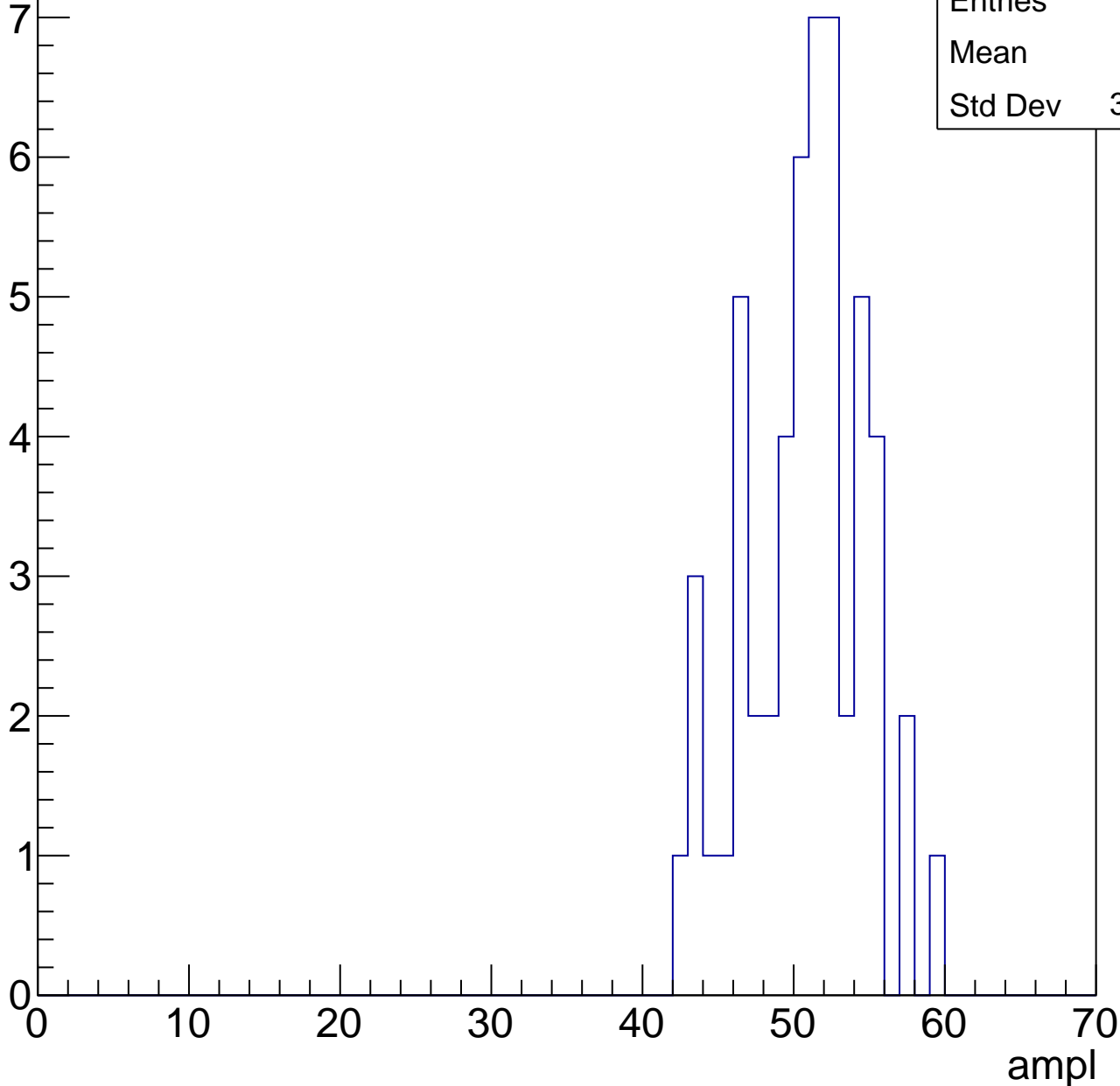


# B1L101S, U18-ch57, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	50.3
Std Dev	3.859

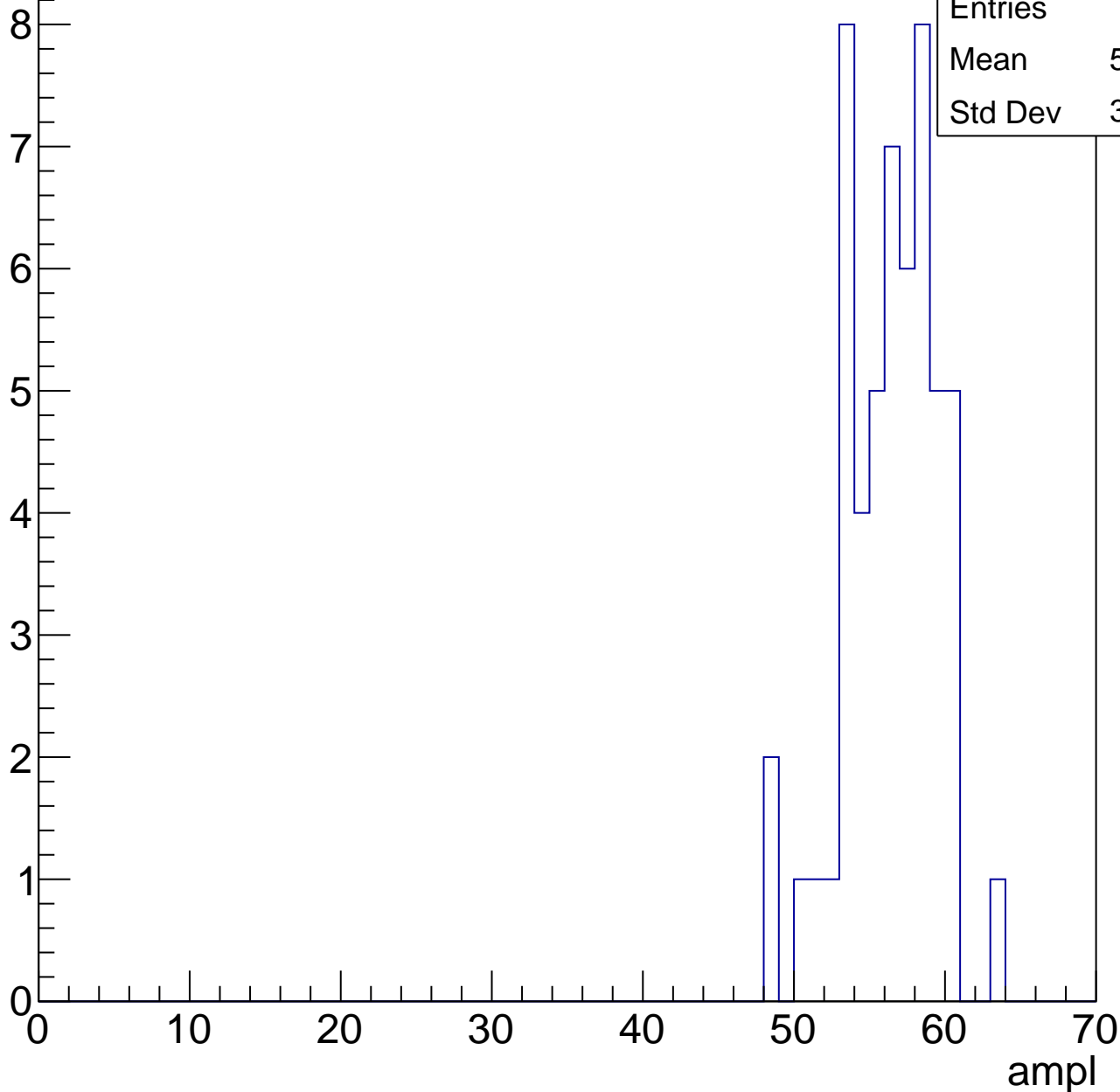


# B1L101S, U18-ch57, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

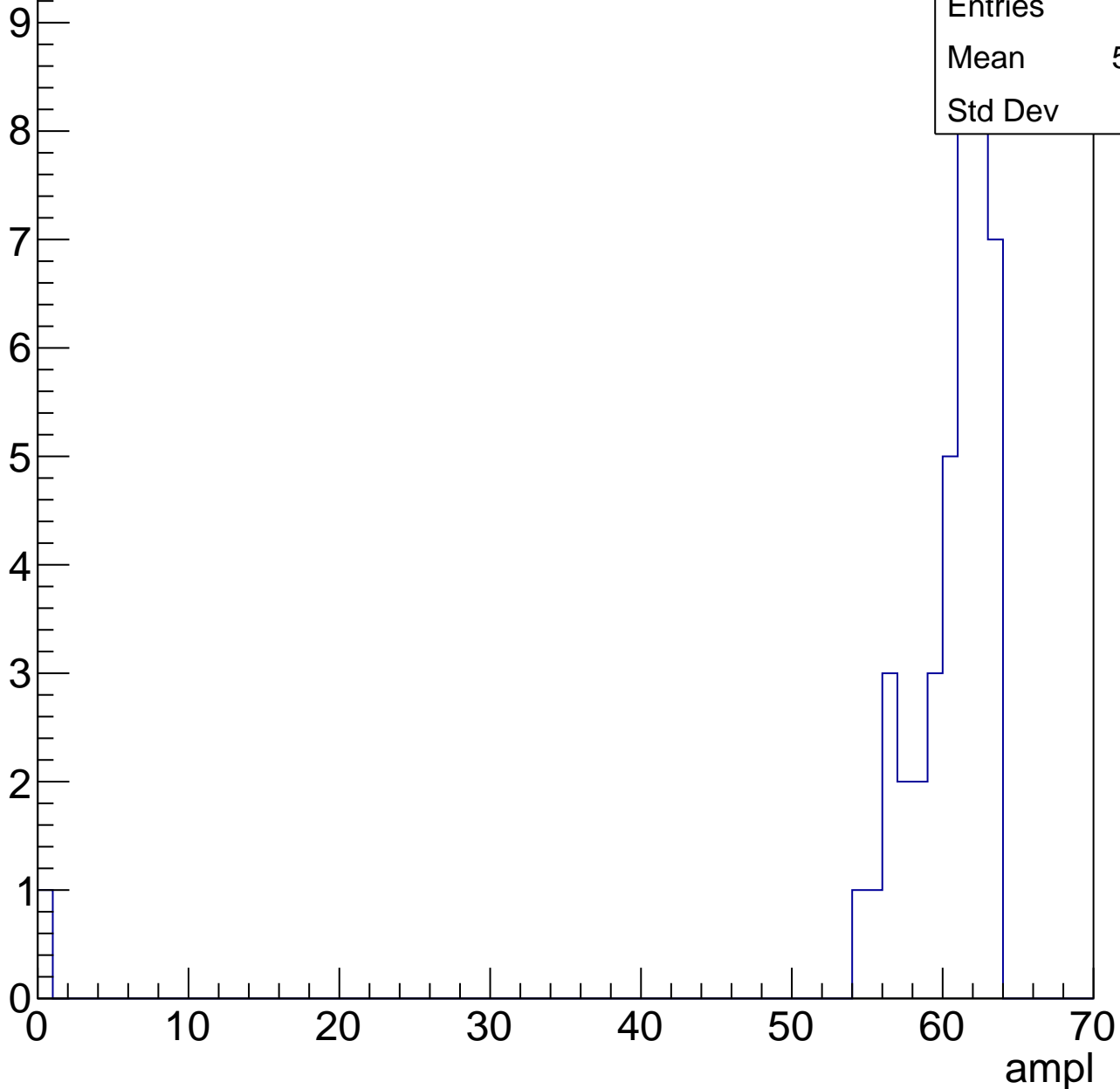
Entries	54
Mean	55.93
Std Dev	3.072



# B1L101S, U18-ch57, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch57, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

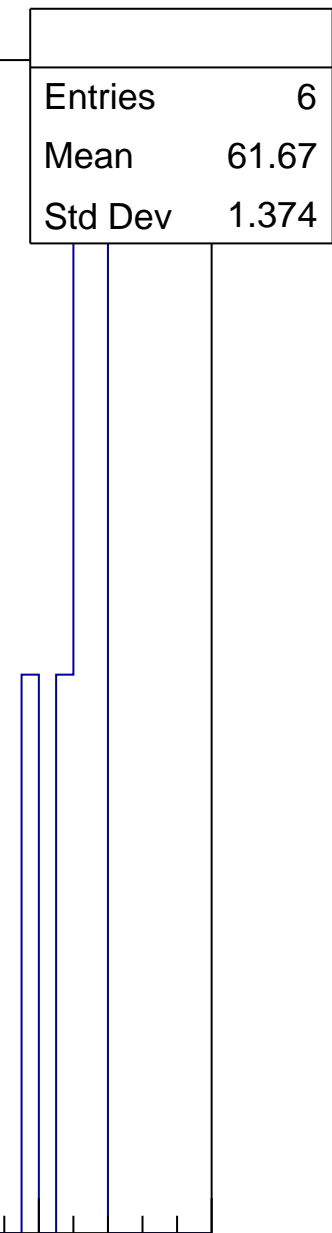
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	61.67
Std Dev	1.374

0 10 20 30 40 50 60 70

ampl





# B1L101S, U18-ch57, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch58, adc0

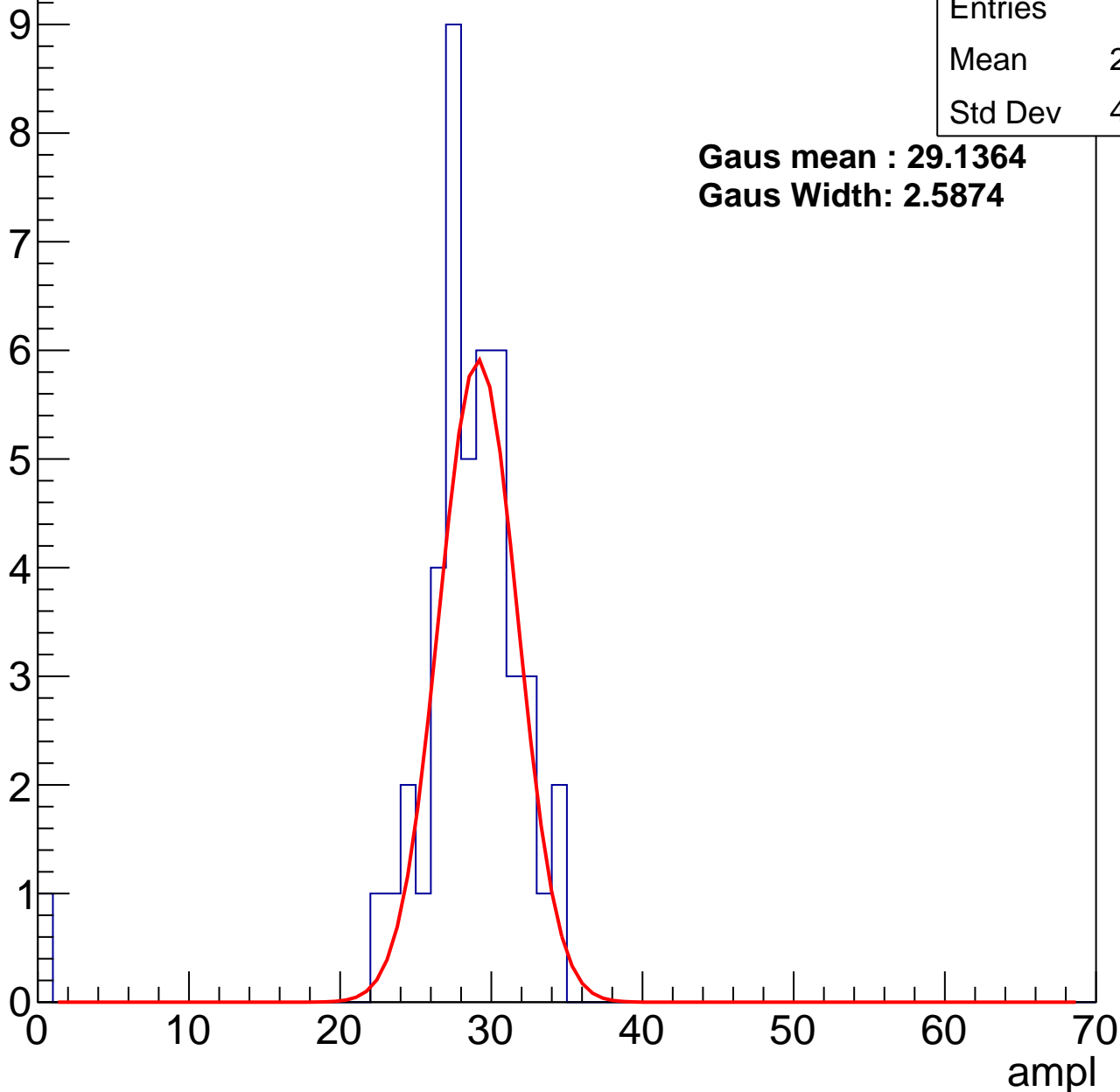
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	45
Mean	27.76
Std Dev	4.967

**Gaus mean : 29.1364**

**Gaus Width: 2.5874**



# B1L101S, U18-ch58, adc1

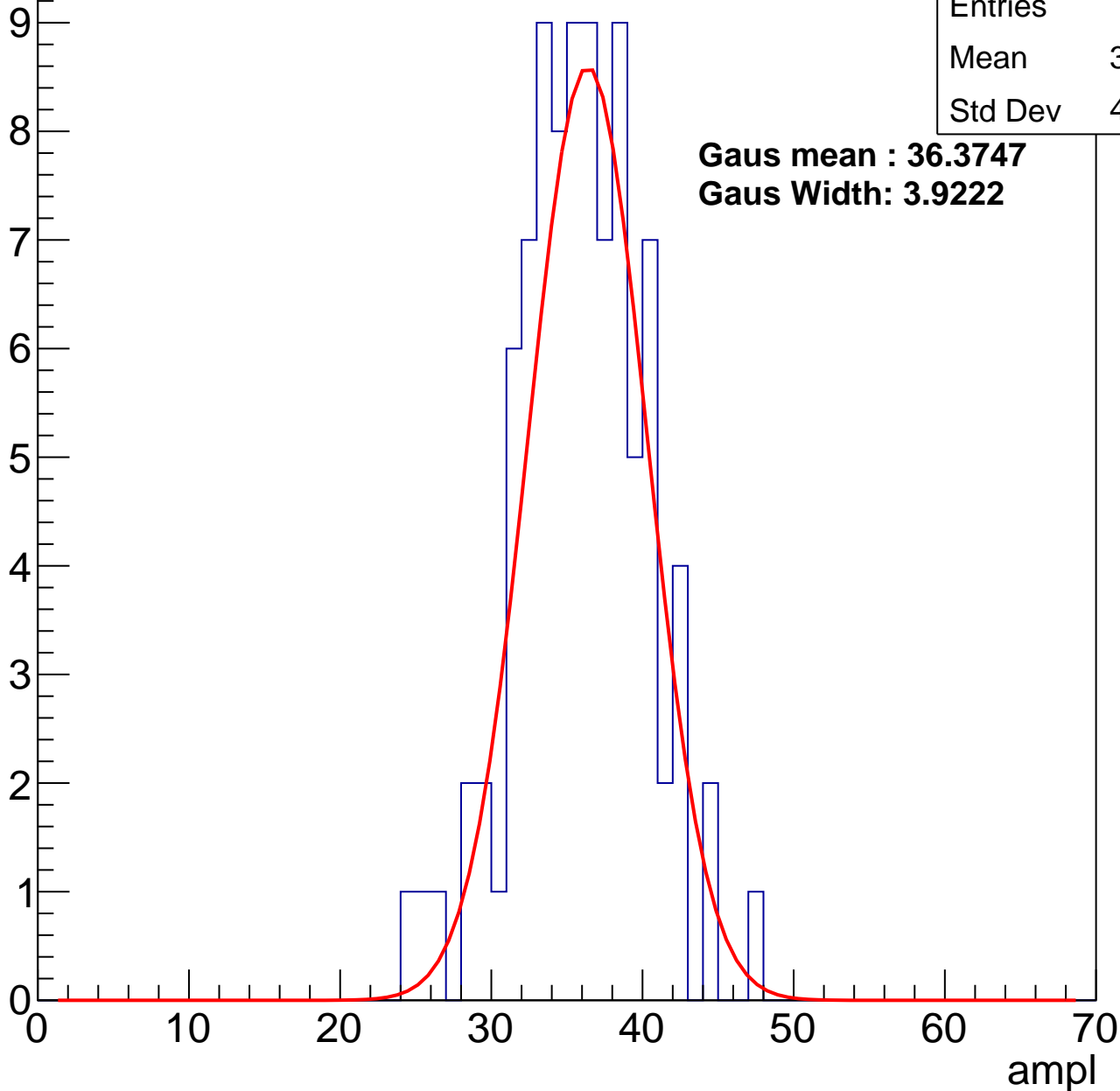
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	93
Mean	35.46
Std Dev	4.183

**Gaus mean : 36.3747**

**Gaus Width: 3.9222**



# B1L101S, U18-ch58, adc2

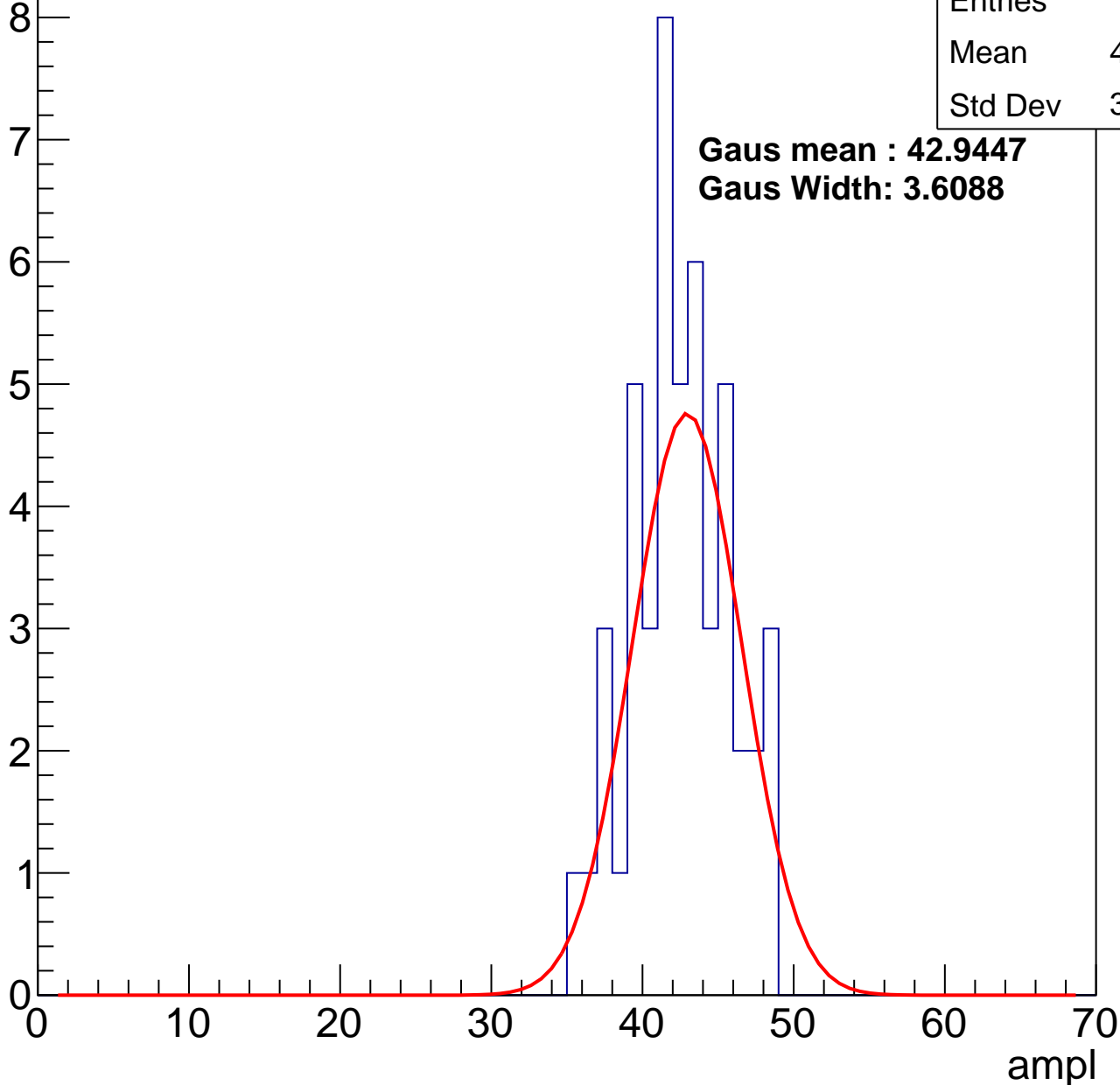
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	48
Mean	42.04
Std Dev	3.208

**Gaus mean : 42.9447**

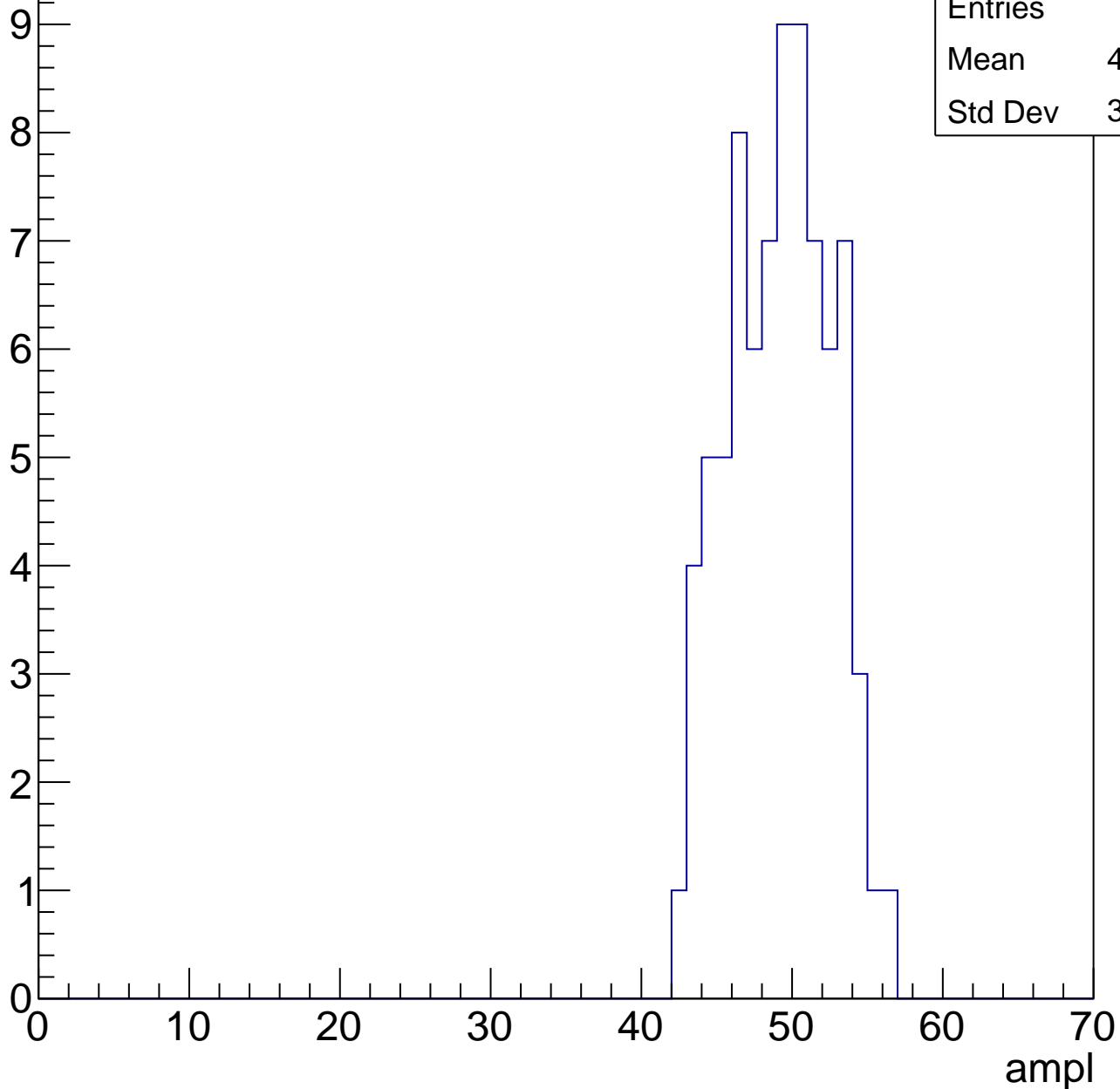
**Gaus Width: 3.6088**



# B1L101S, U18-ch58, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

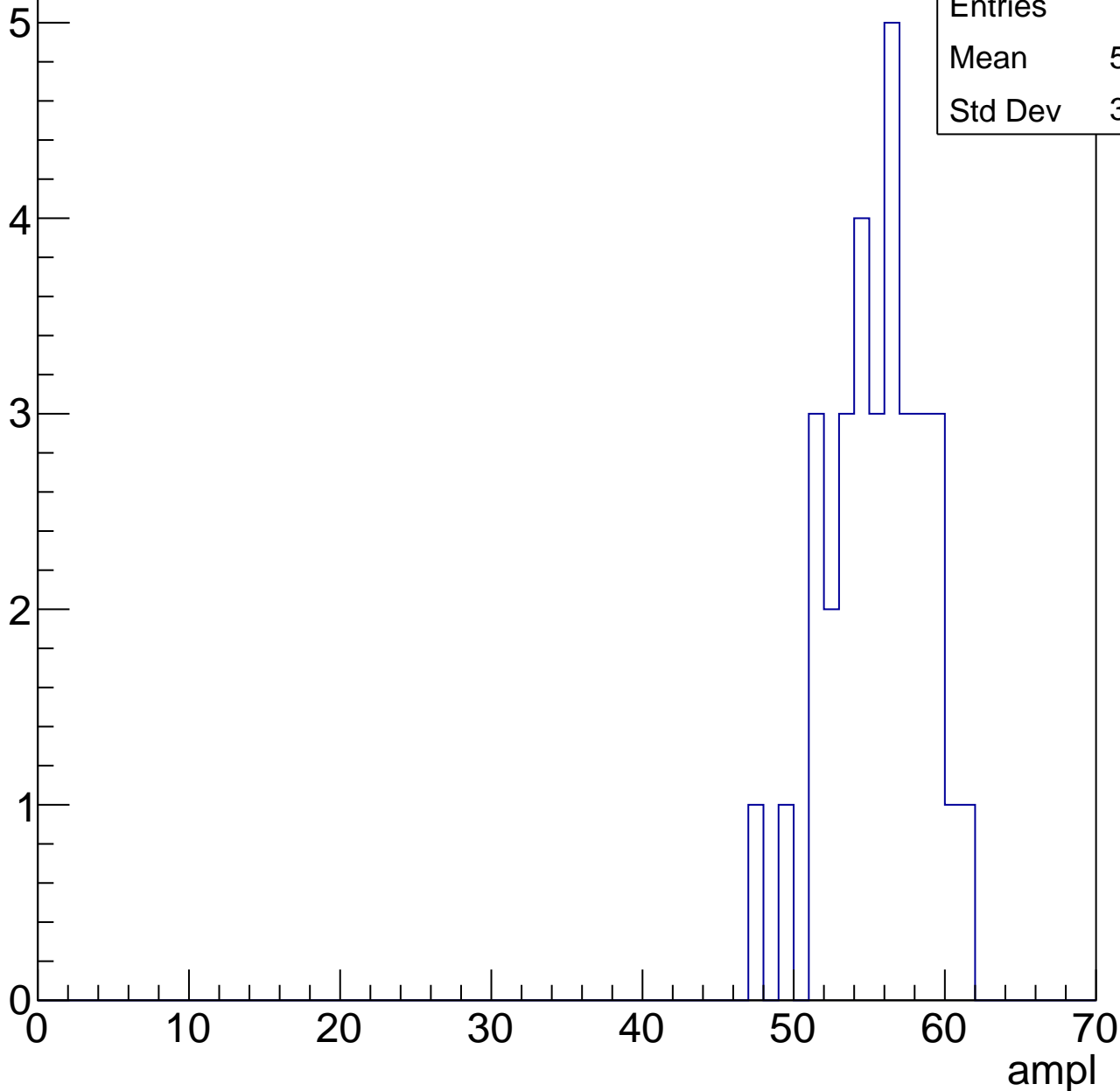


# B1L101S, U18-ch58, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	33
Mean	55.03
Std Dev	3.186

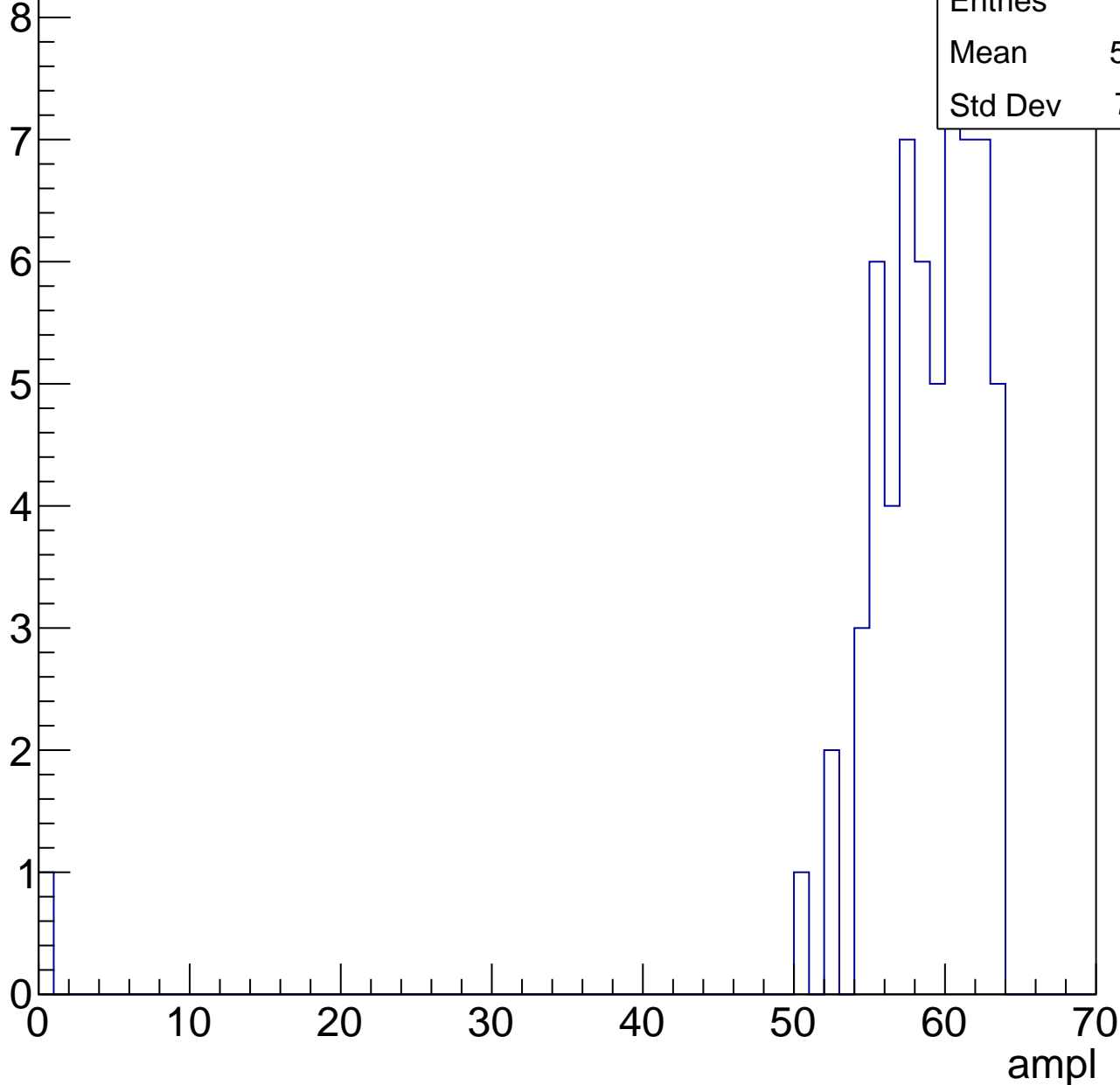


# B1L101S, U18-ch58, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	57.55
Std Dev	7.981

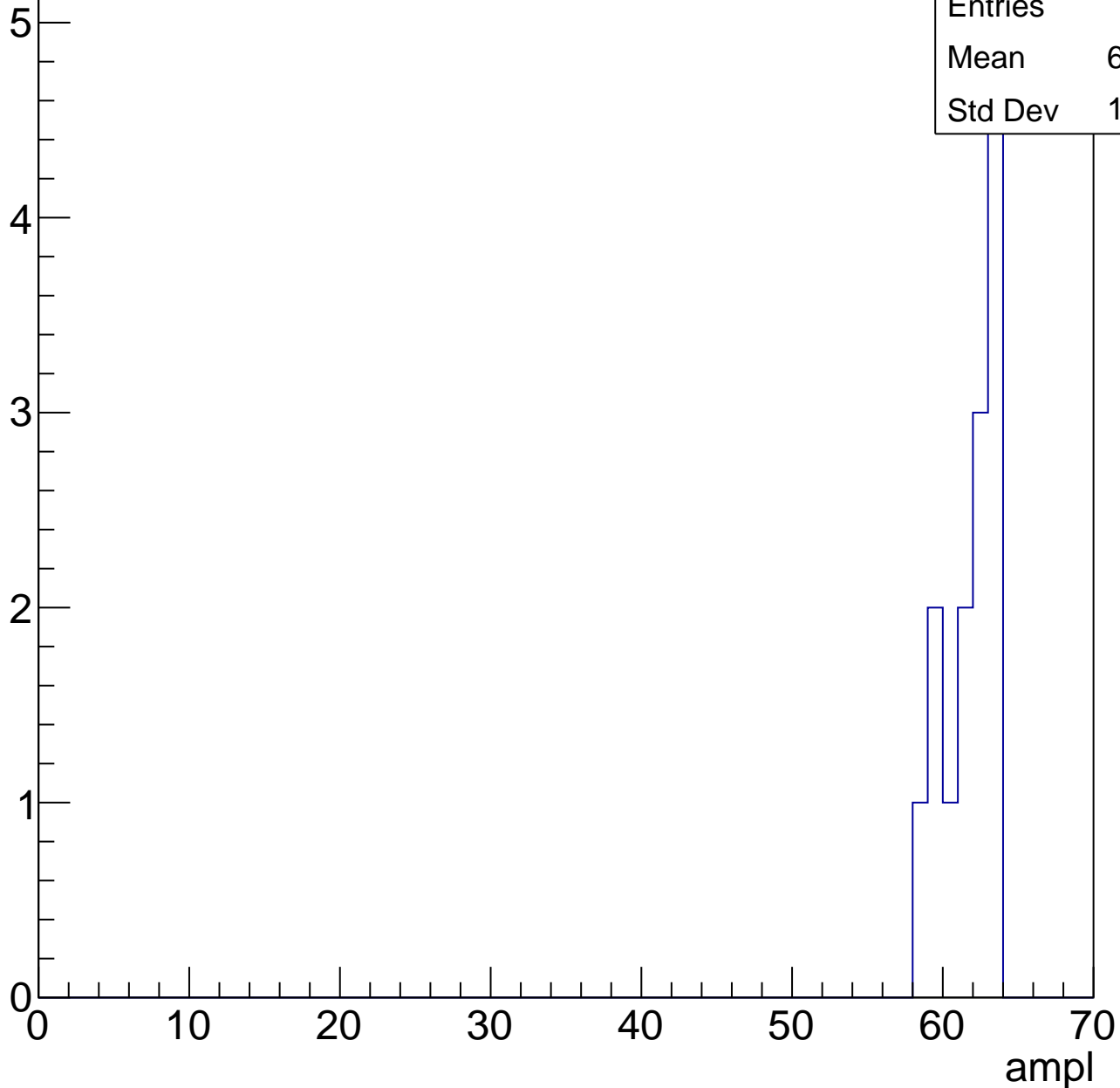


# B1L101S, U18-ch58, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	14
Mean	61.36
Std Dev	1.674





# B1L101S, U18-ch58, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U18-ch59, adc0

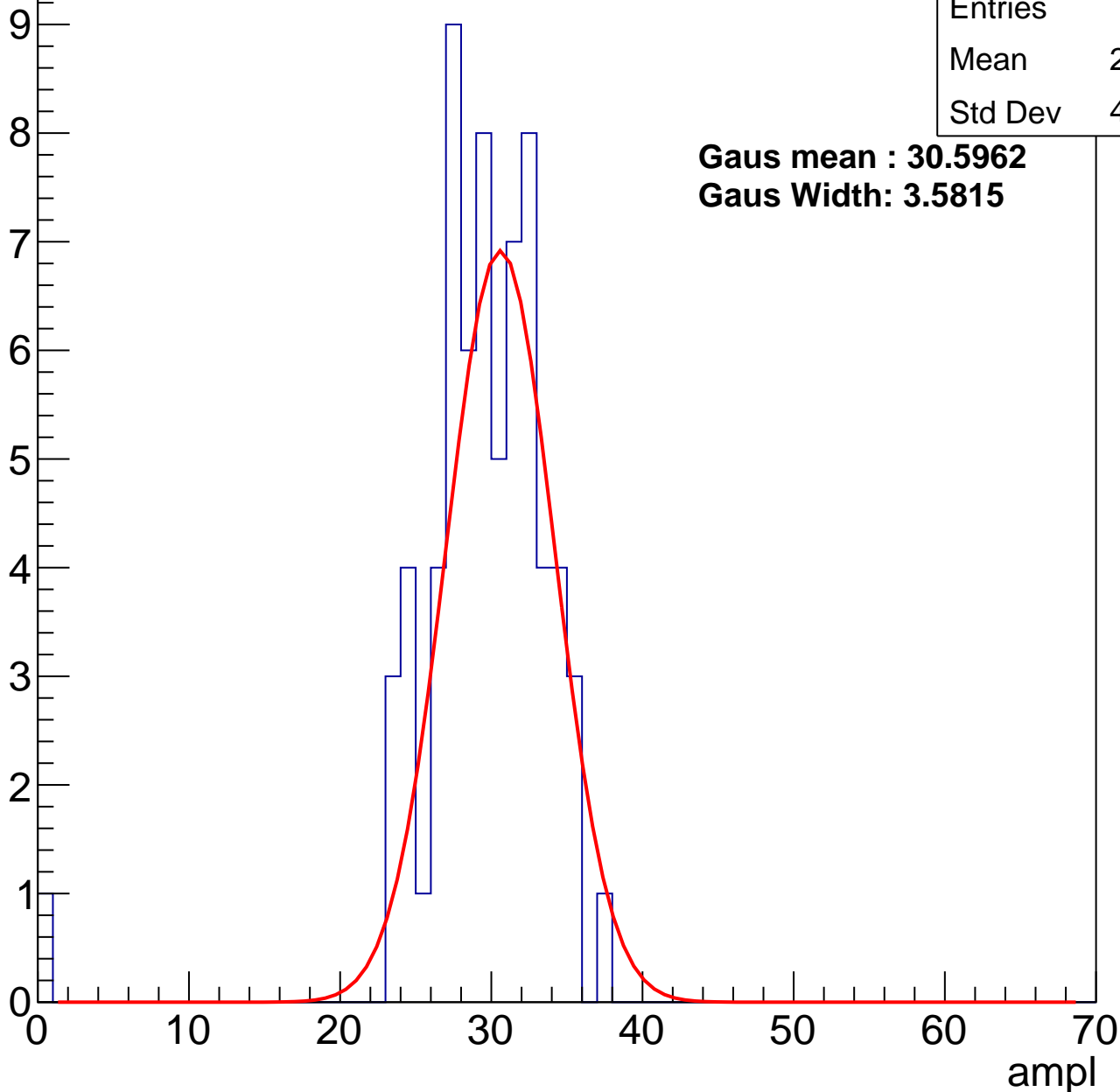
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	28.97
Std Dev	4.826

**Gaus mean : 30.5962**

**Gaus Width: 3.5815**



# B1L101S, U18-ch59, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	79
Mean	37.76
Std Dev	3.583

**Gaus mean : 38.1632**

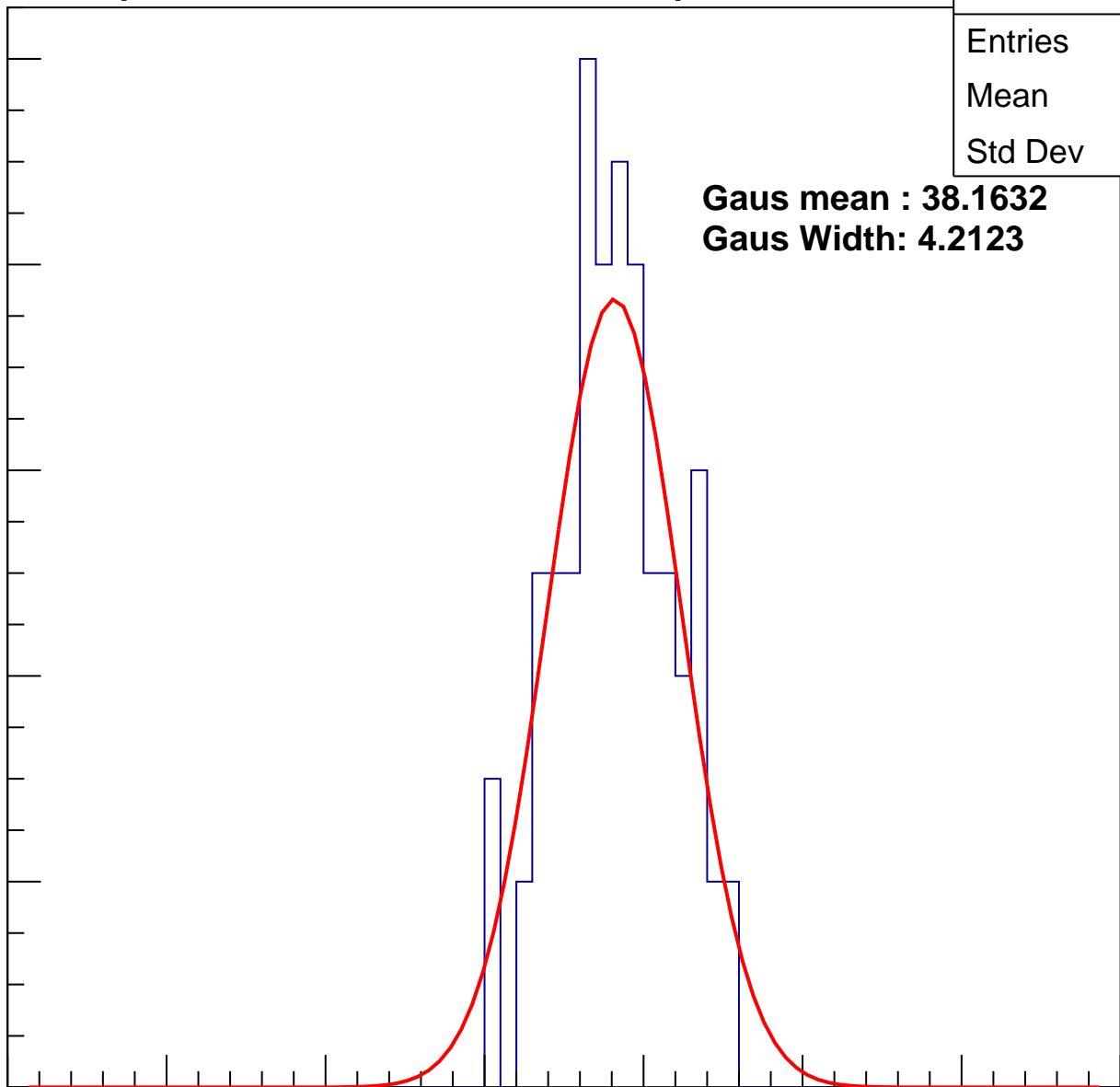
**Gaus Width: 4.2123**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L101S, U18-ch59, adc2

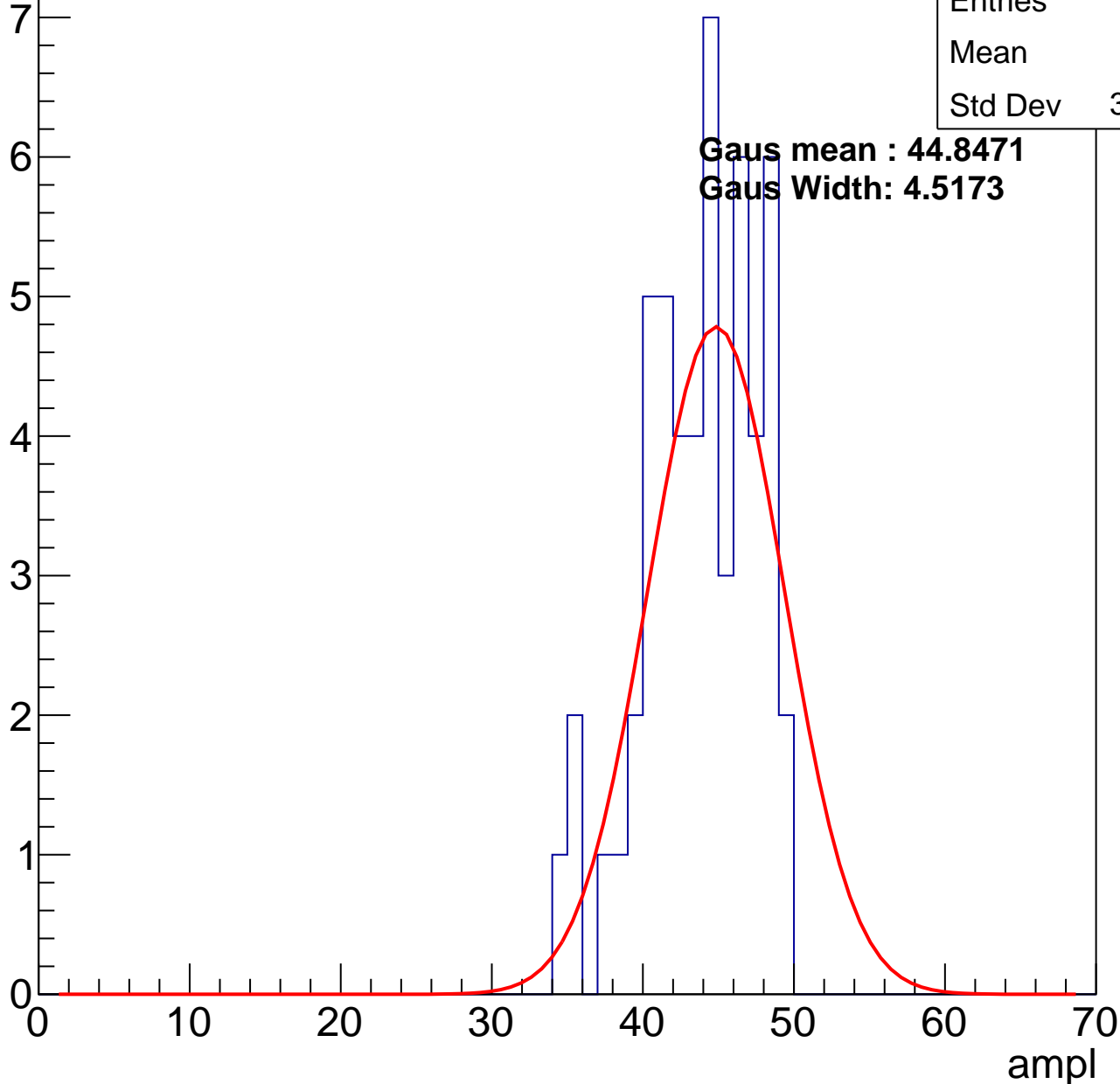
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	43.3
Std Dev	3.699

**Gaus mean : 44.8471**

**Gaus Width: 4.5173**



# B1L101S, U18-ch59, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	75
Mean	50.25
Std Dev	3.6

Entry

10

8

6

4

2

0

0

10

20

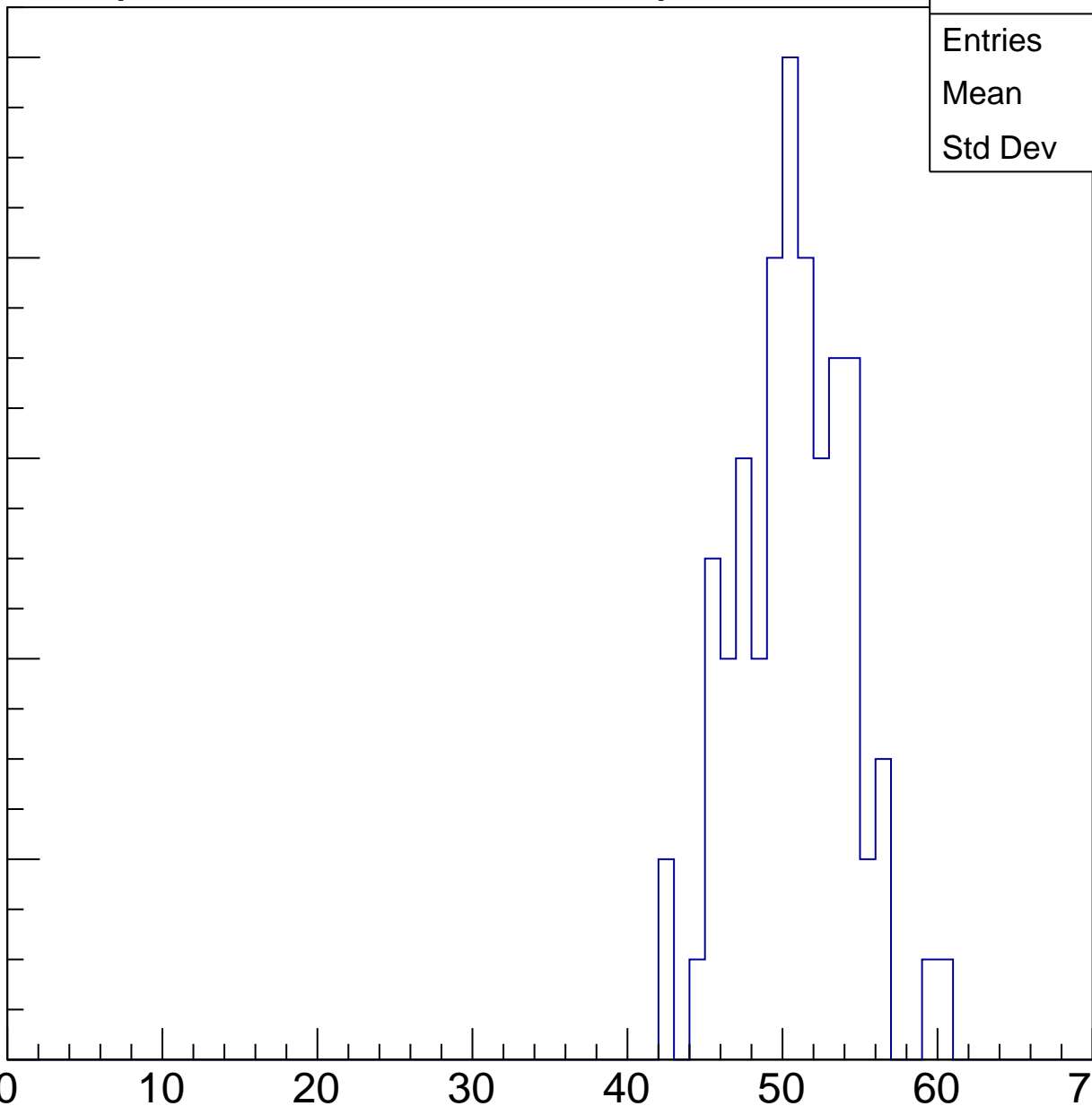
30

40

50

60

ampl

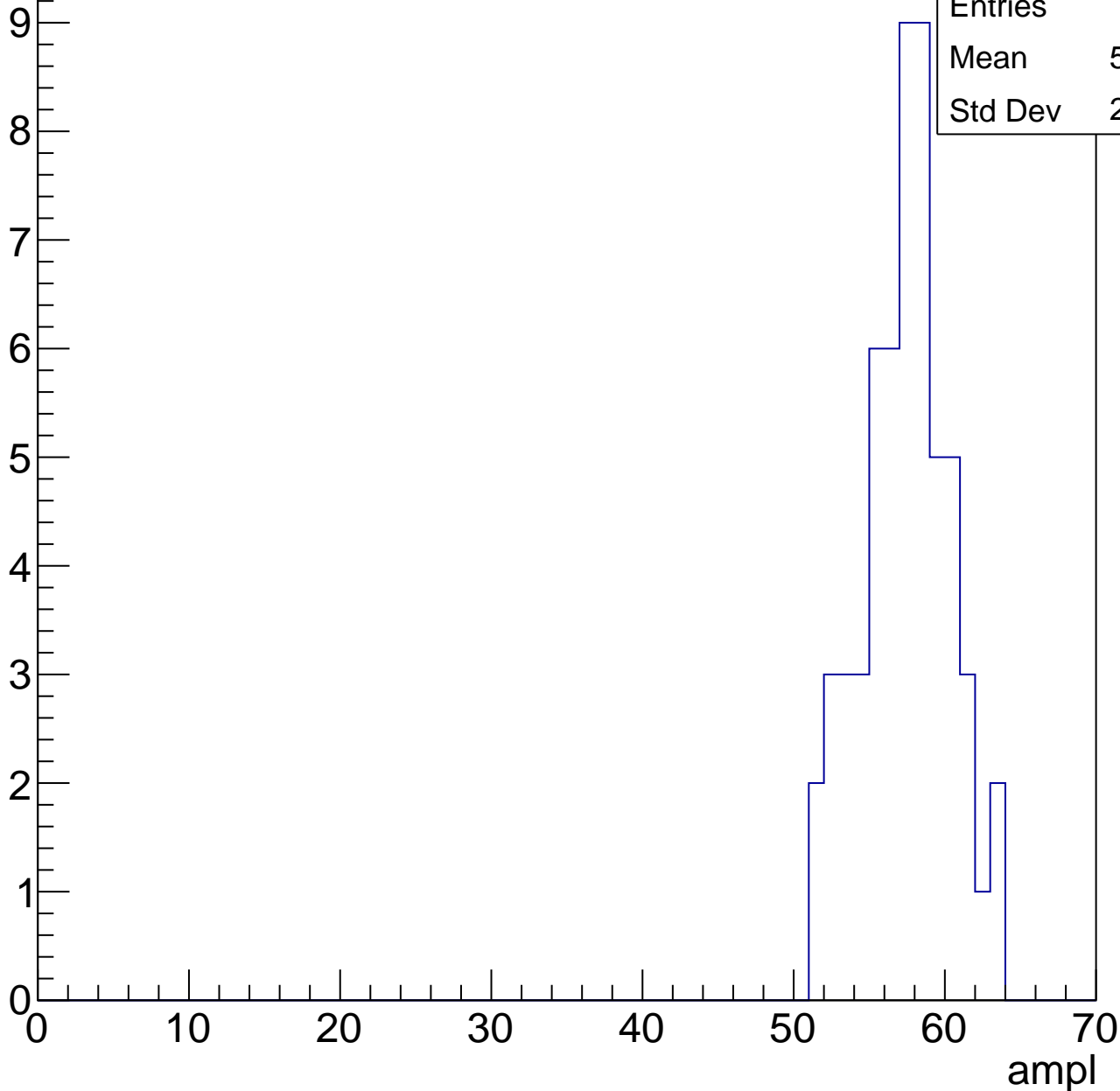


# B1L101S, U18-ch59, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	56.95
Std Dev	2.874

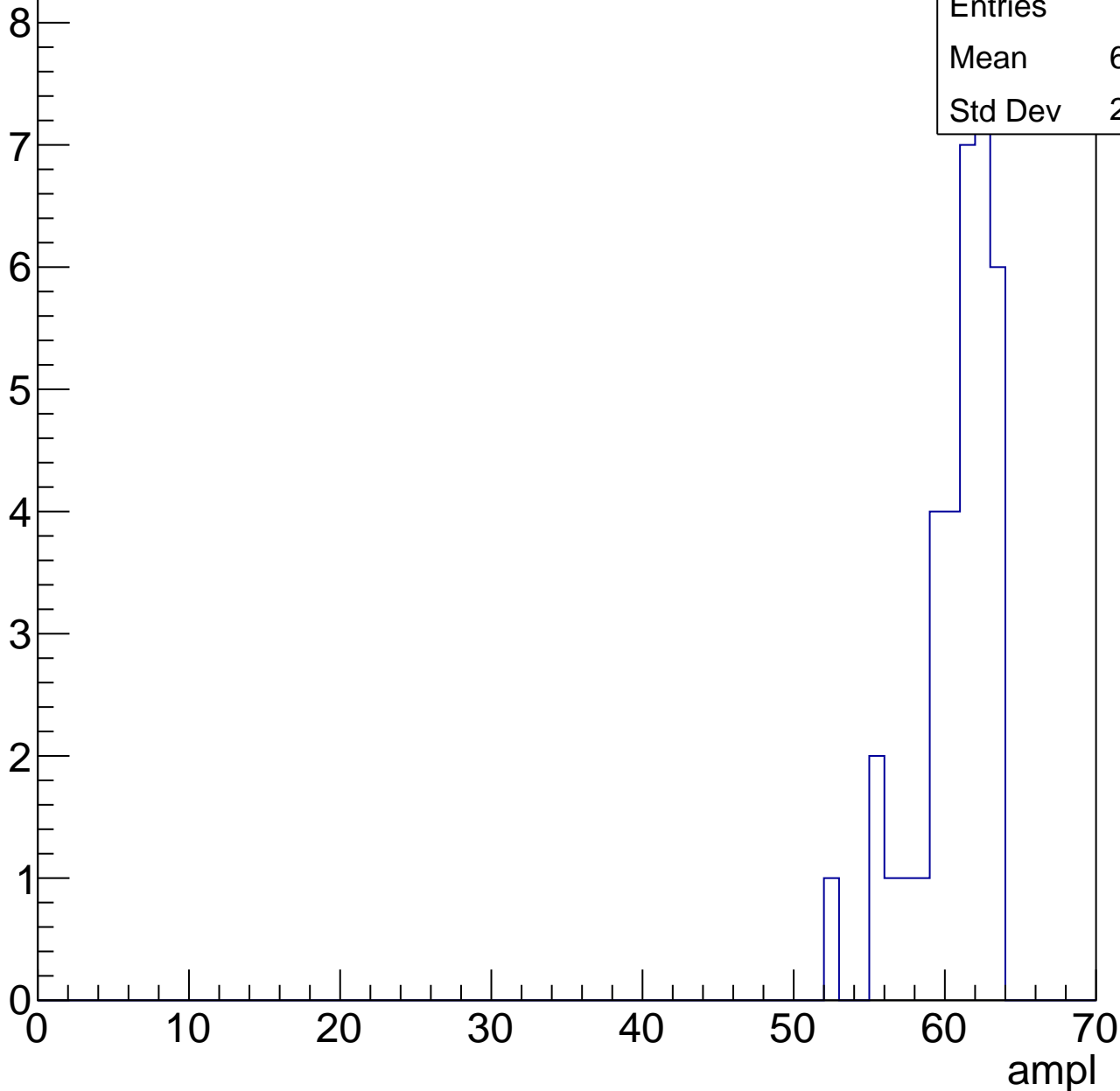


# B1L101S, U18-ch59, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	35
Mean	60.29
Std Dev	2.603



# B1L101S, U18-ch59, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch59, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	4
Mean	0
Std Dev	0

# B1L101S, U18-ch60, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	78
Mean	27.13
Std Dev	4.781

**Gaus mean : 28.2556**

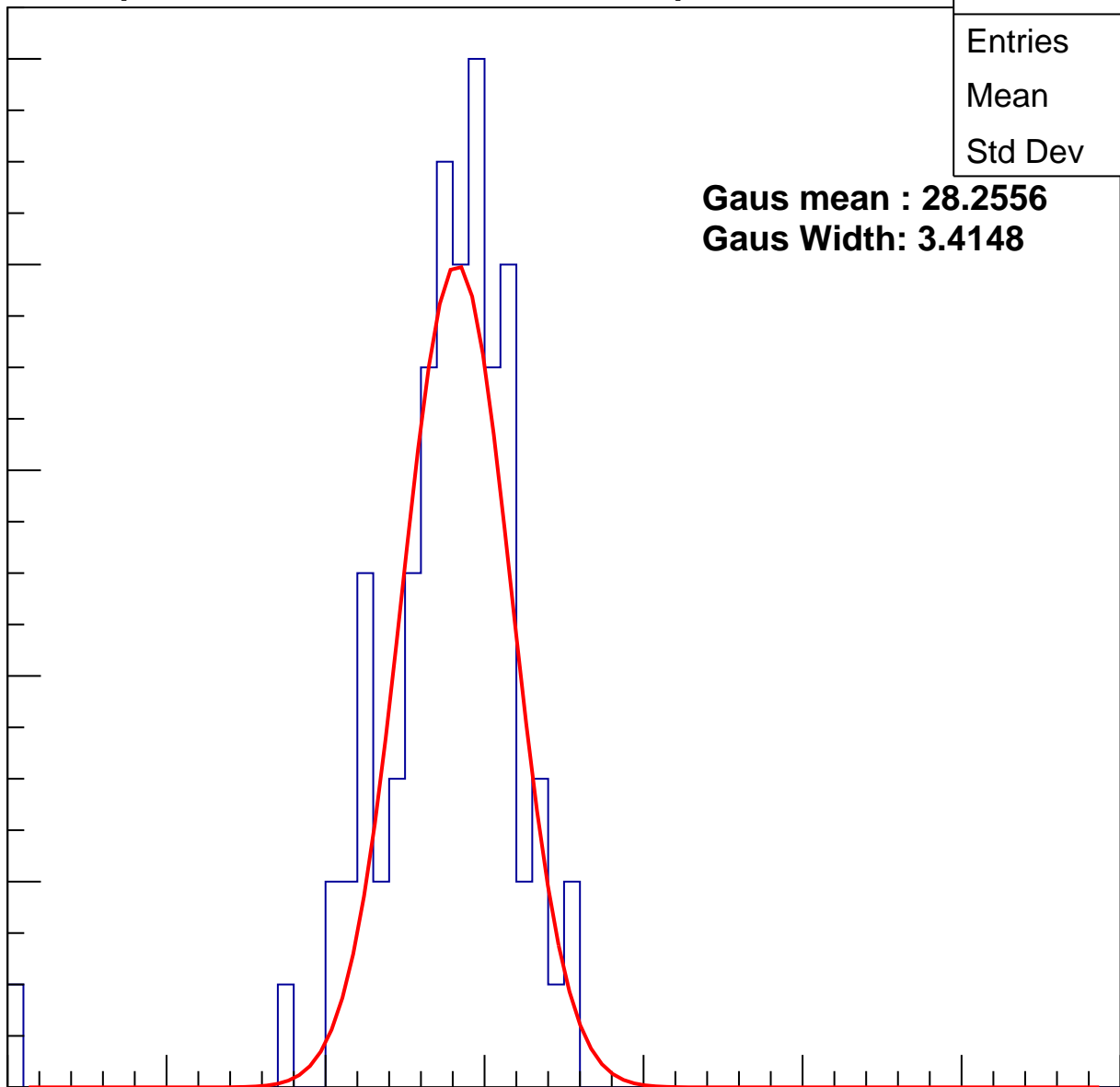
**Gaus Width: 3.4148**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U18-ch60, adc1

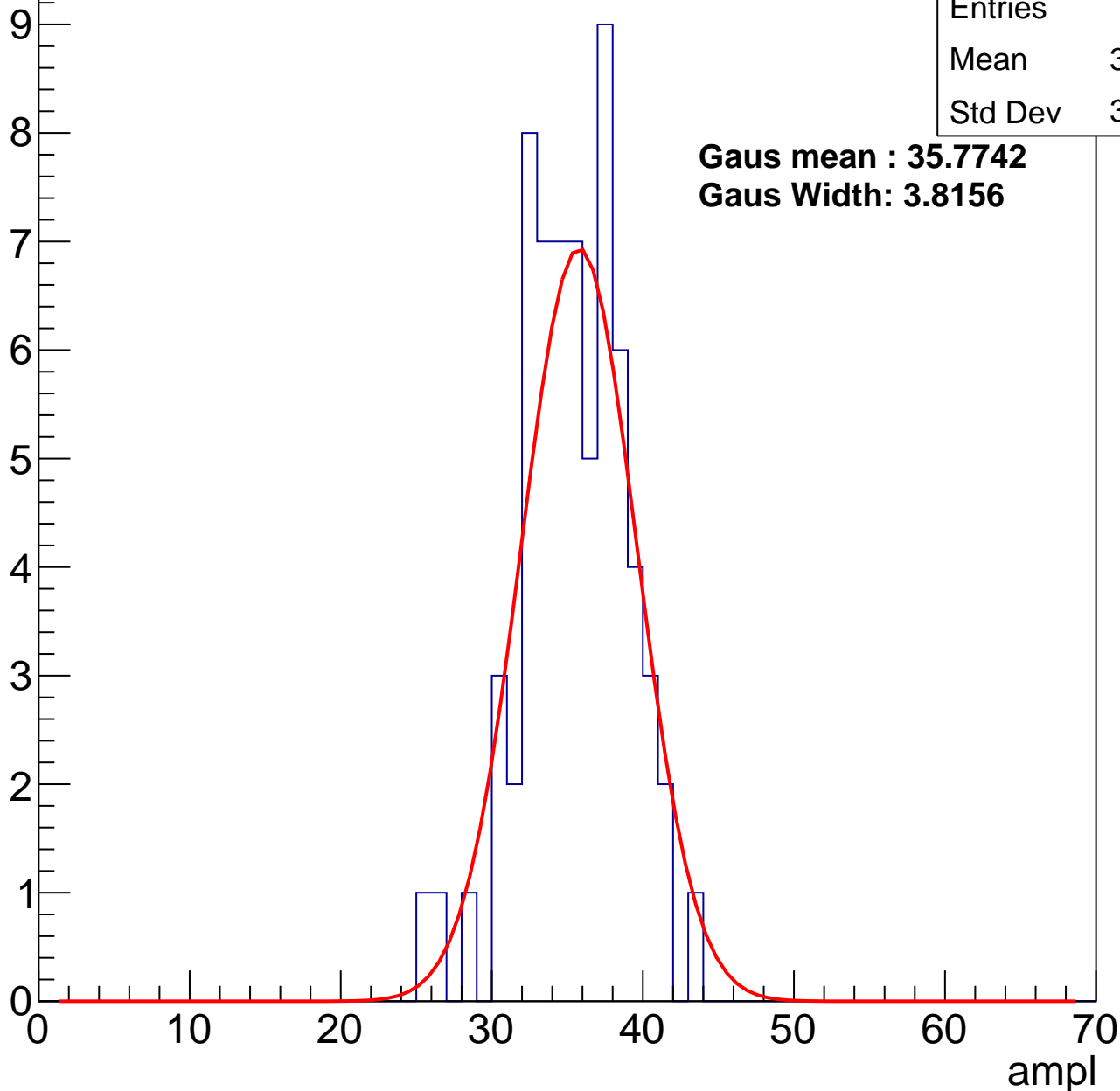
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	34.97
Std Dev	3.485

**Gaus mean : 35.7742**

**Gaus Width: 3.8156**



# B1L101S, U18-ch60, adc2

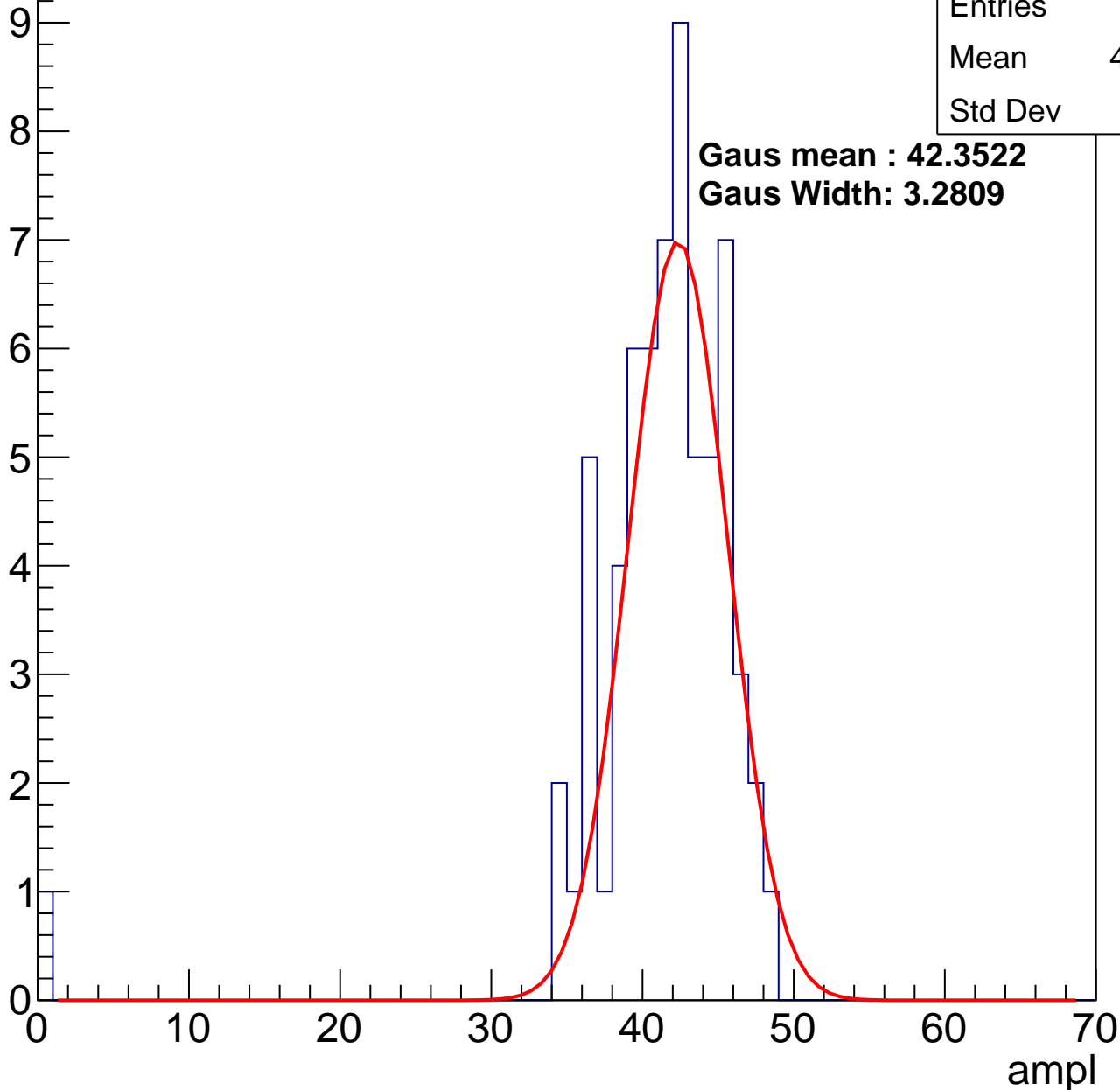
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	40.63
Std Dev	6.07

**Gaus mean : 42.3522**

**Gaus Width: 3.2809**

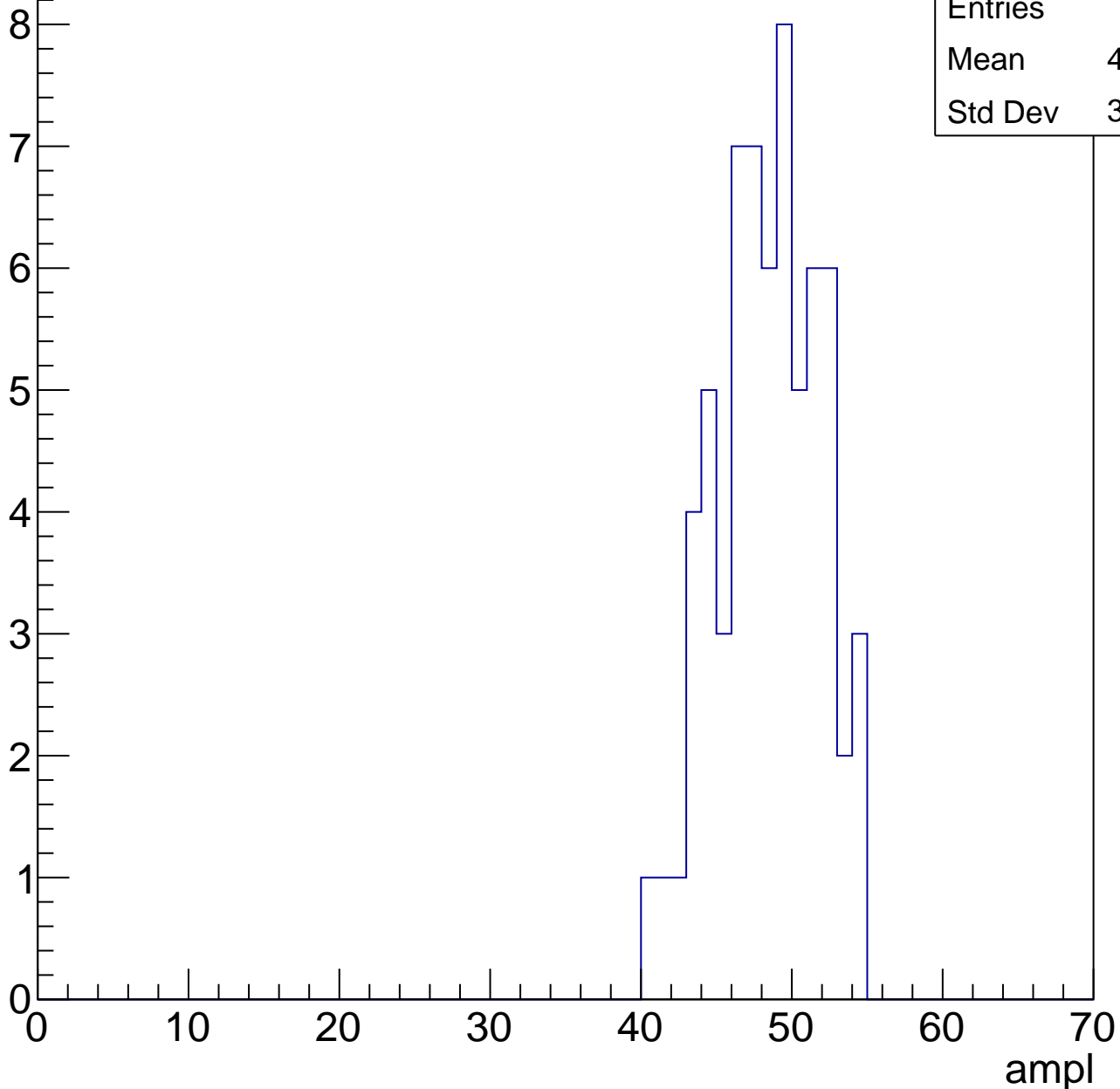


# B1L101S, U18-ch60, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	47.95
Std Dev	3.344

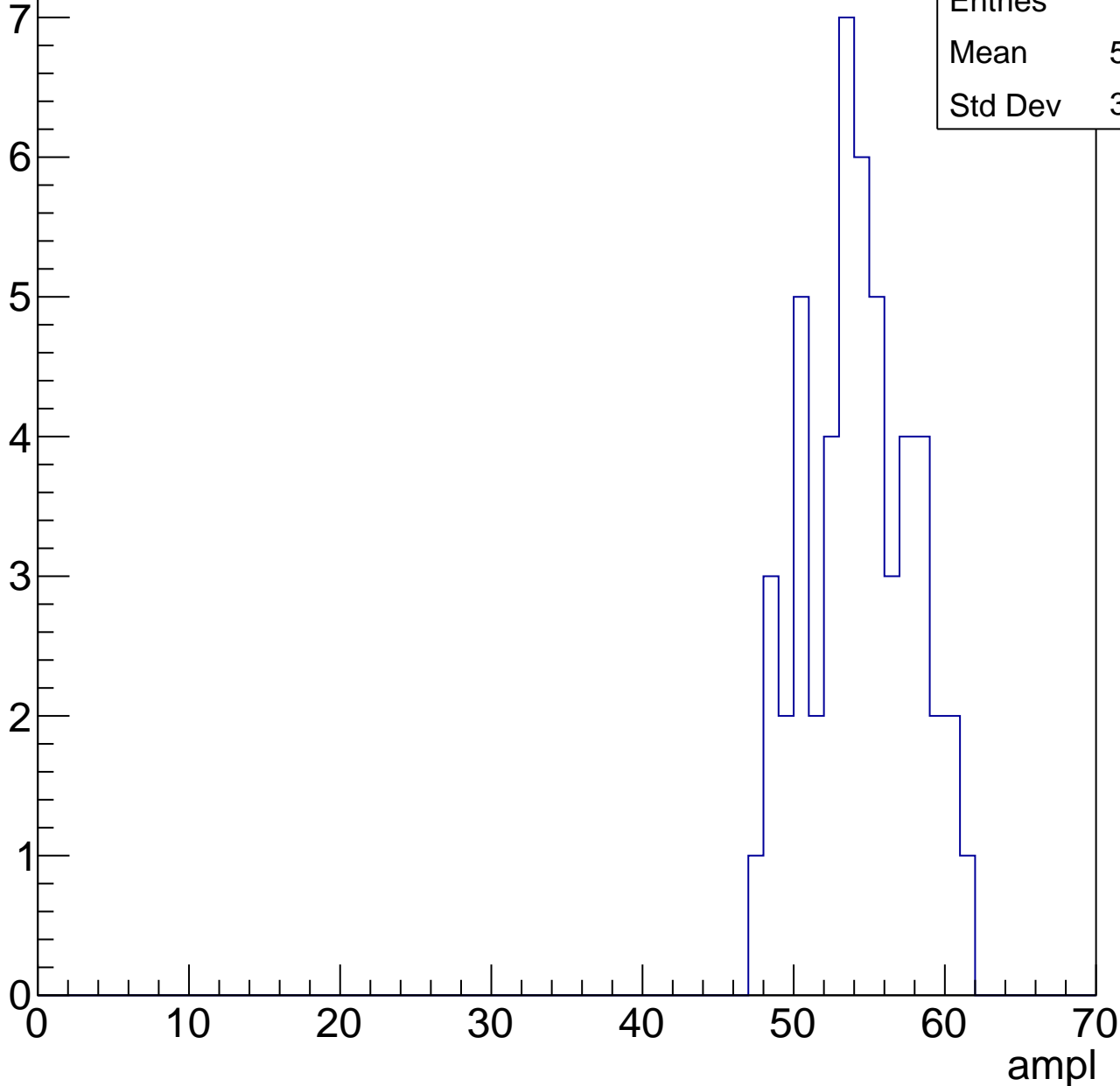


# B1L101S, U18-ch60, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	53.84
Std Dev	3.472

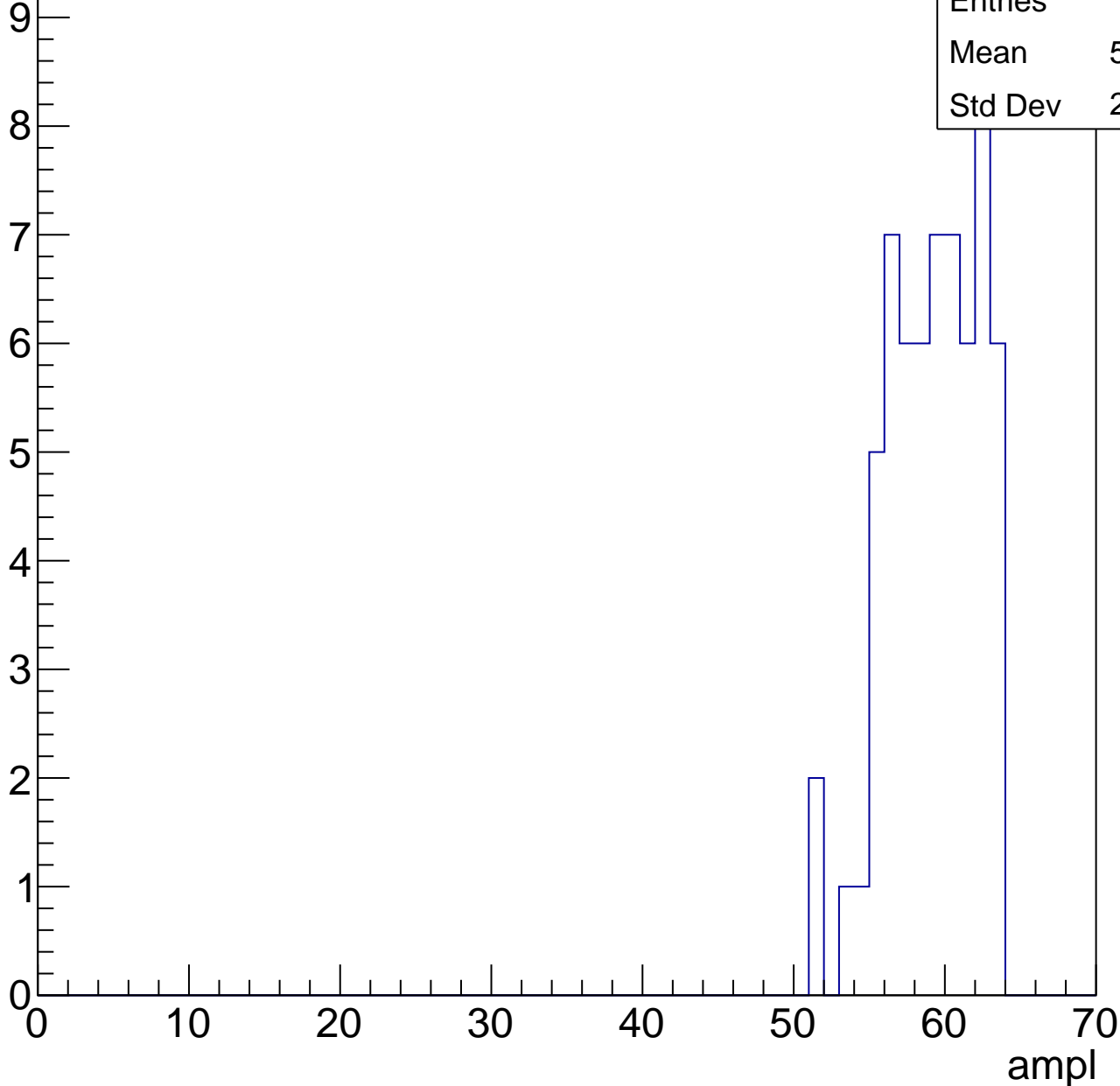


# B1L101S, U18-ch60, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

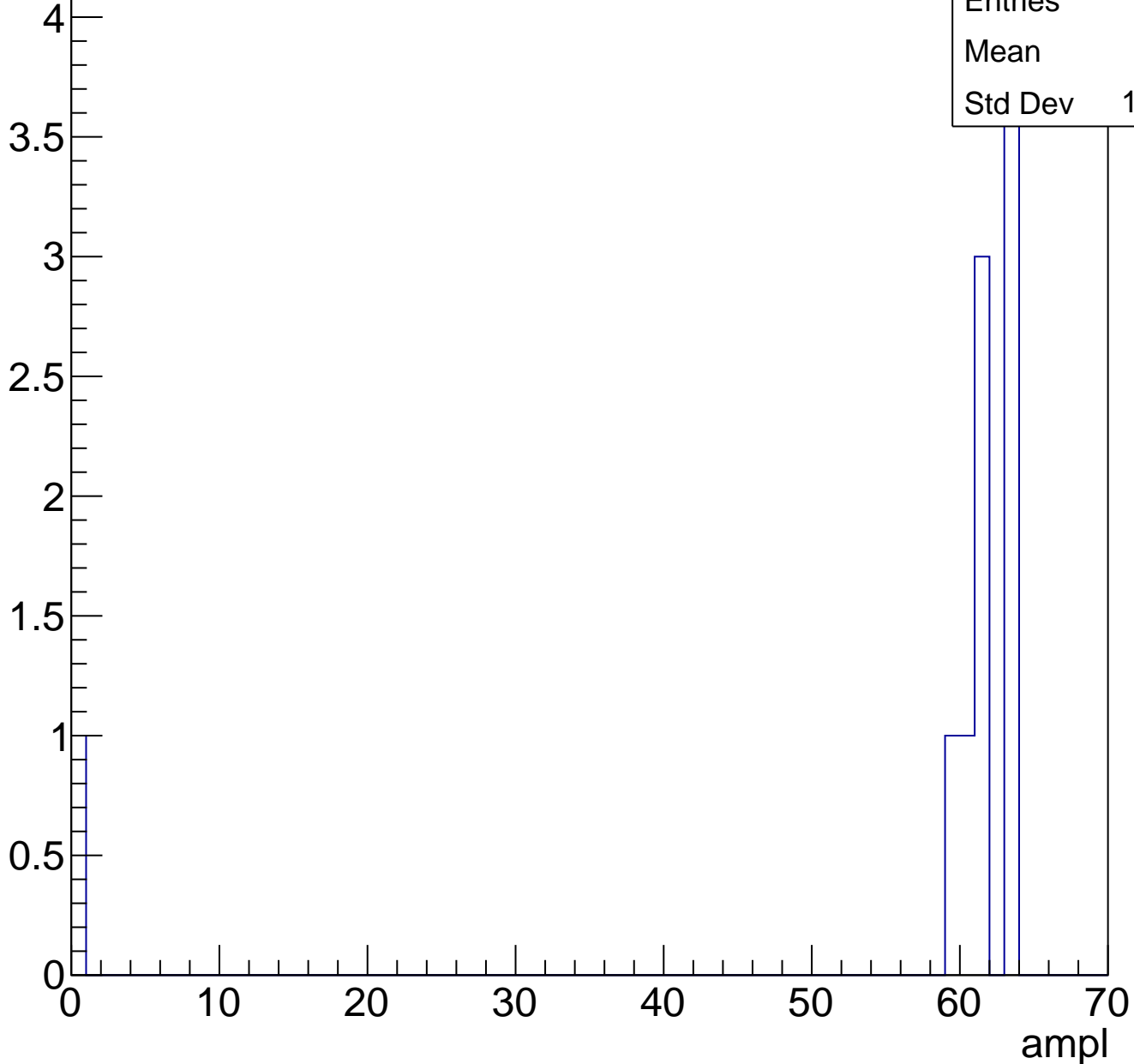
Entries	63
Mean	58.75
Std Dev	2.997



# B1L101S, U18-ch60, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch60, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch61, adc0

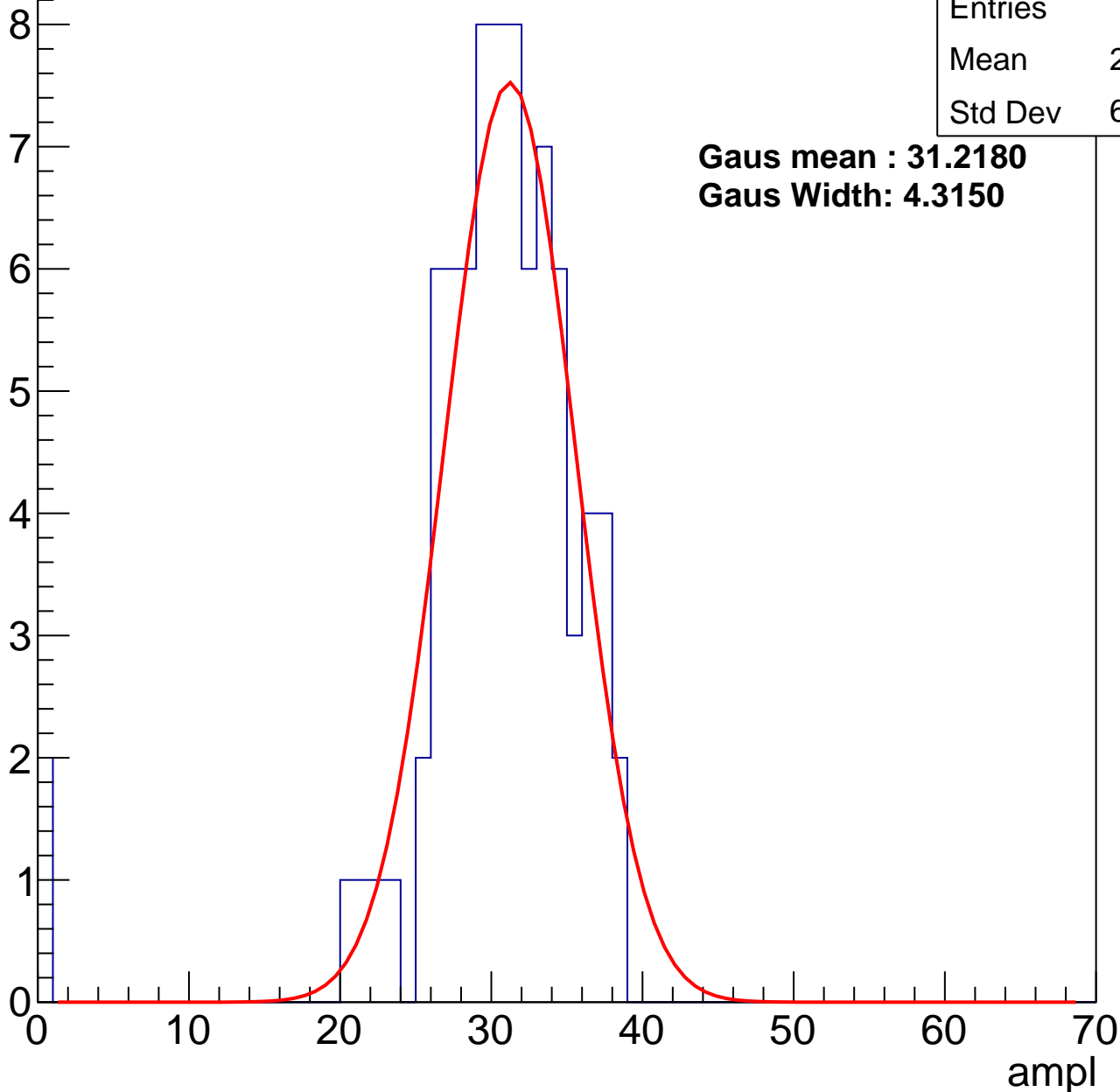
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	82
Mean	29.78
Std Dev	6.105

**Gaus mean : 31.2180**

**Gaus Width: 4.3150**



# B1L101S, U18-ch61, adc1

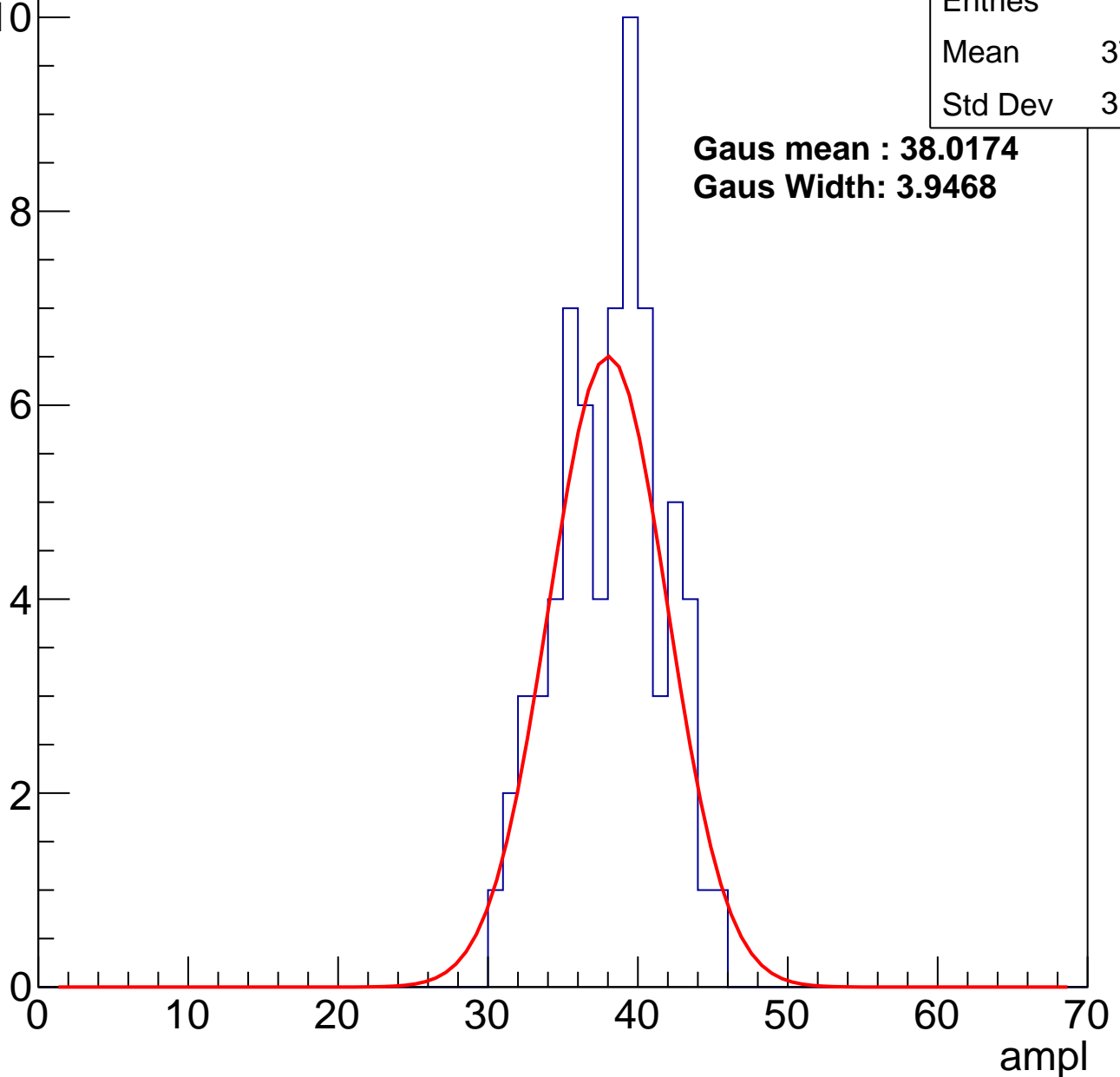
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	37.68
Std Dev	3.479

**Gaus mean : 38.0174**

**Gaus Width: 3.9468**



# B1L101S, U18-ch61, adc2

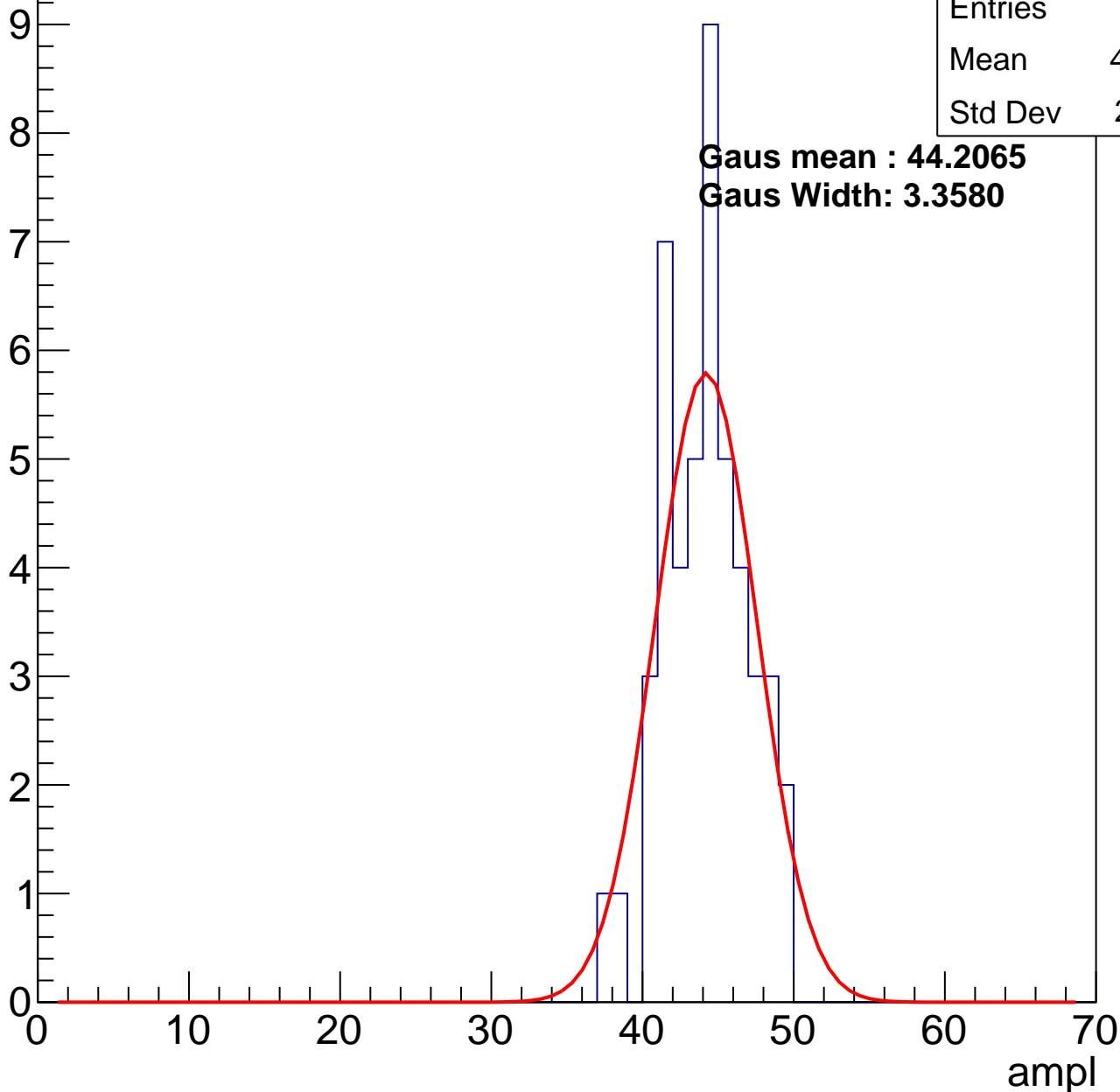
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	47
Mean	43.68
Std Dev	2.761

**Gaus mean : 44.2065**

**Gaus Width: 3.3580**

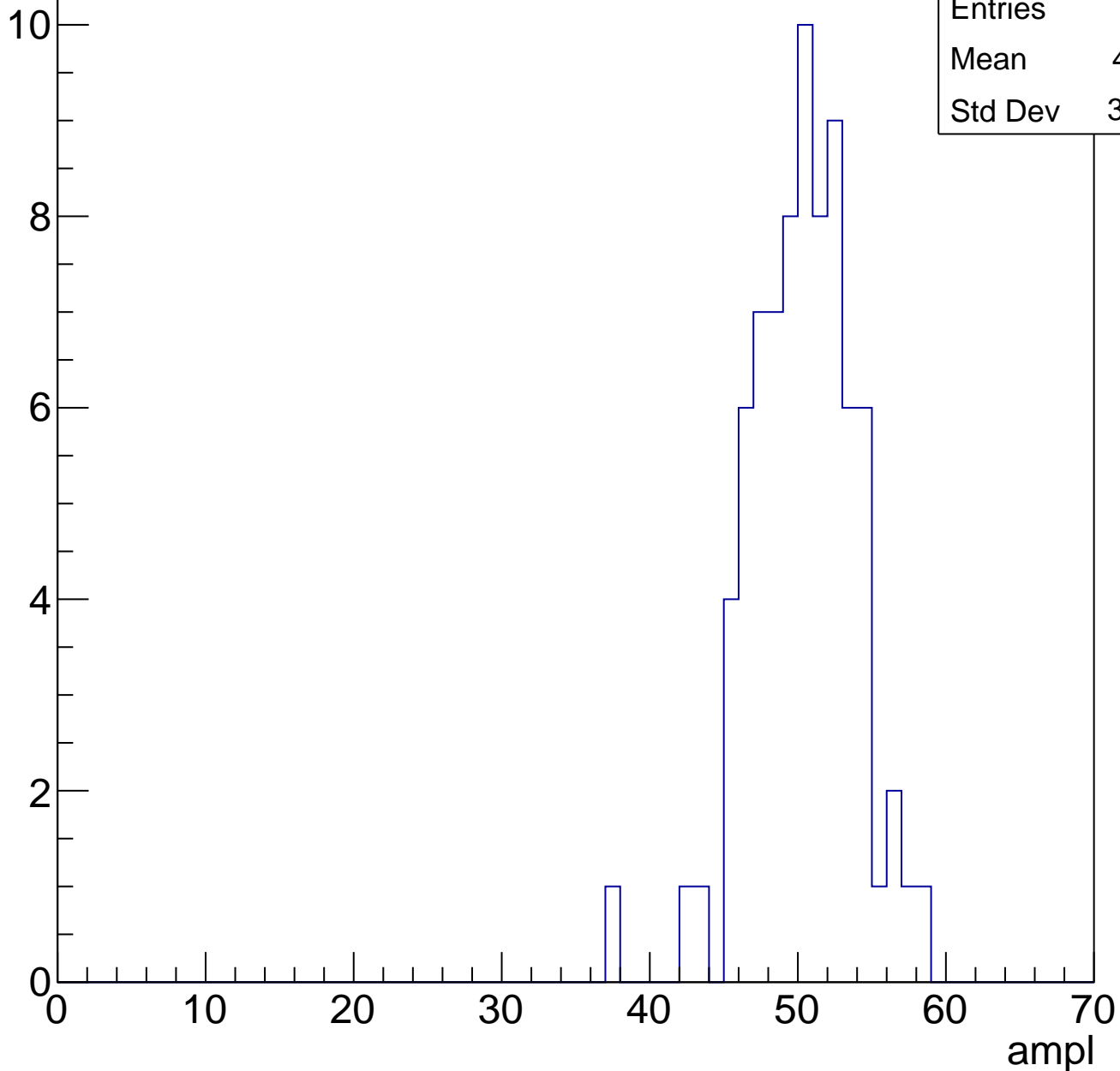


# B1L101S, U18-ch61, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

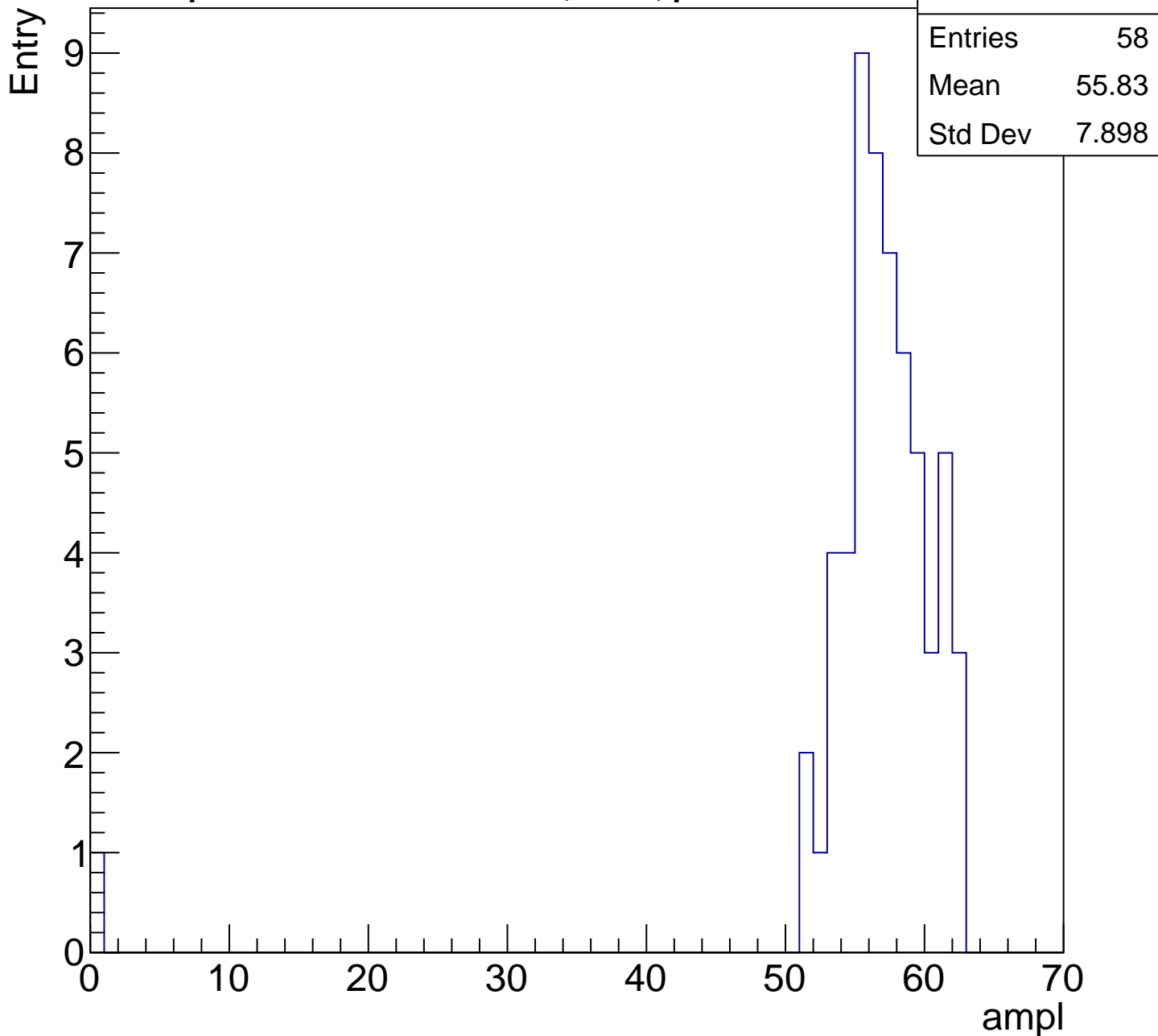
Entries	79
Mean	49.81
Std Dev	3.519

Entry



# B1L101S, U18-ch61, adc4

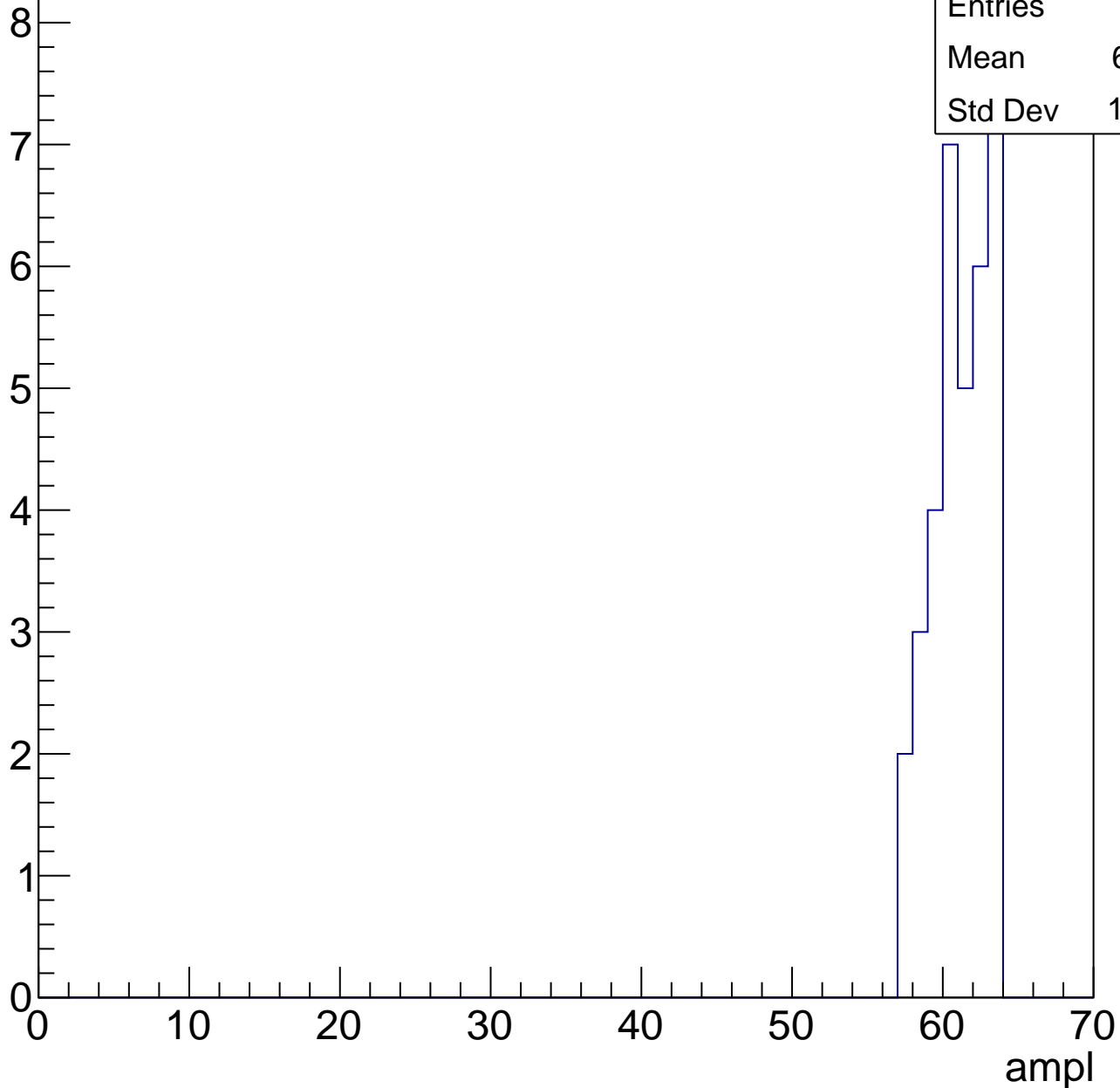
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U18-ch61, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	35
Mean	60.71
Std Dev	1.829

# B1L101S, U18-ch61, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch61, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U18-ch62, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	75
Mean	29.31
Std Dev	4.921

**Gaus mean : 30.1192**

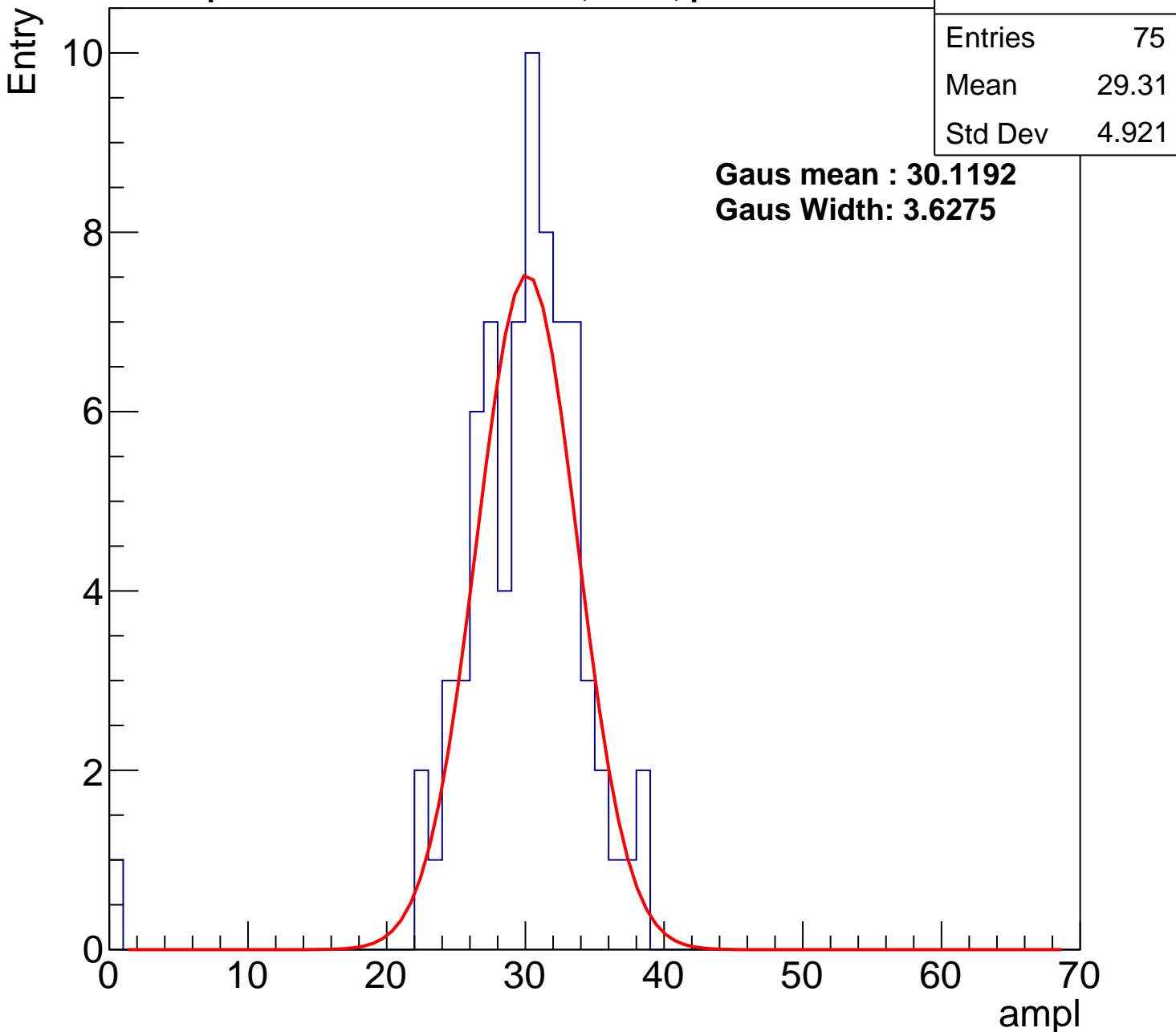
**Gaus Width: 3.6275**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U18-ch62, adc1

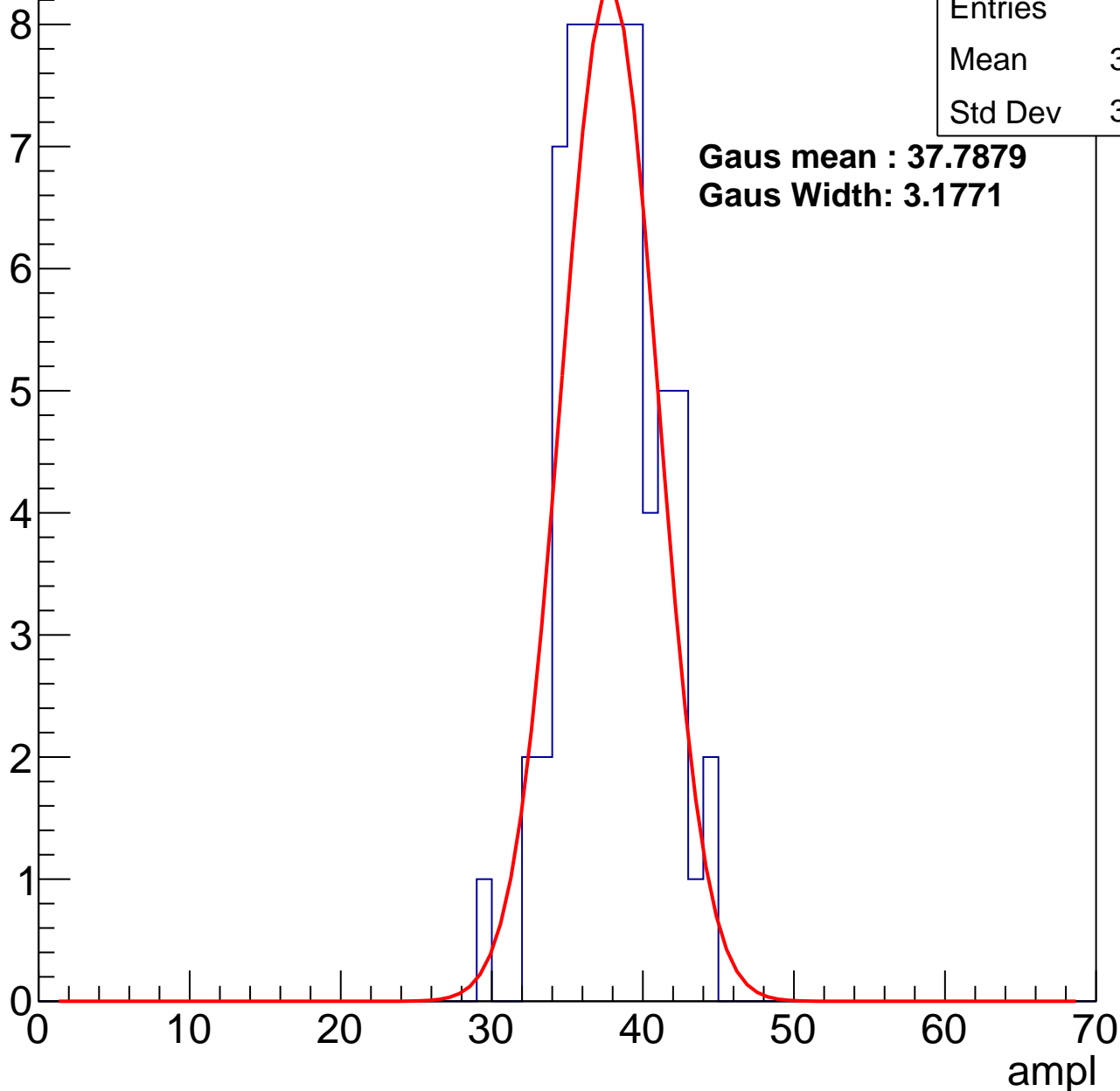
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	37.43
Std Dev	3.072

**Gaus mean : 37.7879**

**Gaus Width: 3.1771**



# B1L101S, U18-ch62, adc2

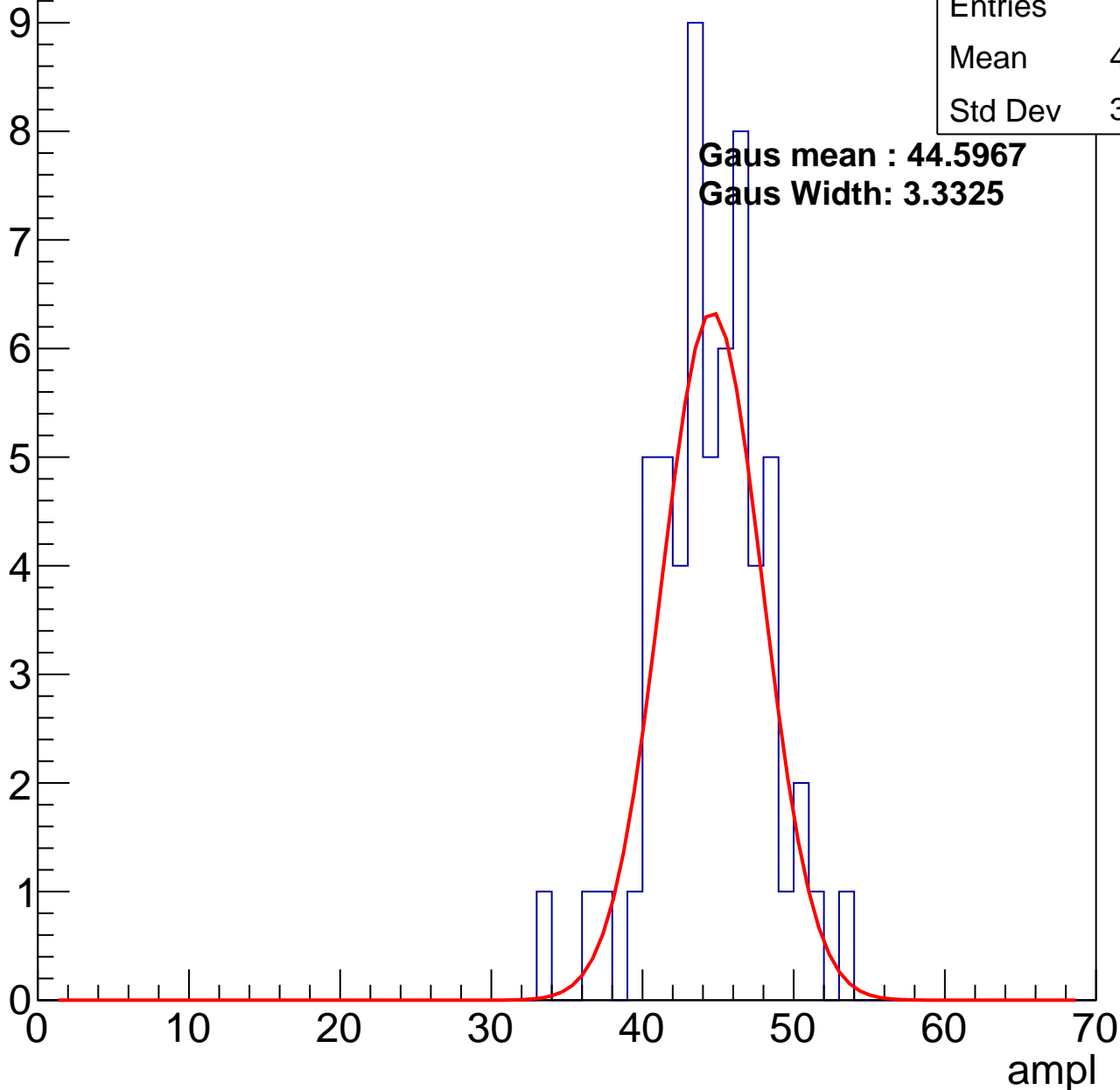
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	44.07
Std Dev	3.628

**Gaus mean : 44.5967**

**Gaus Width: 3.3325**

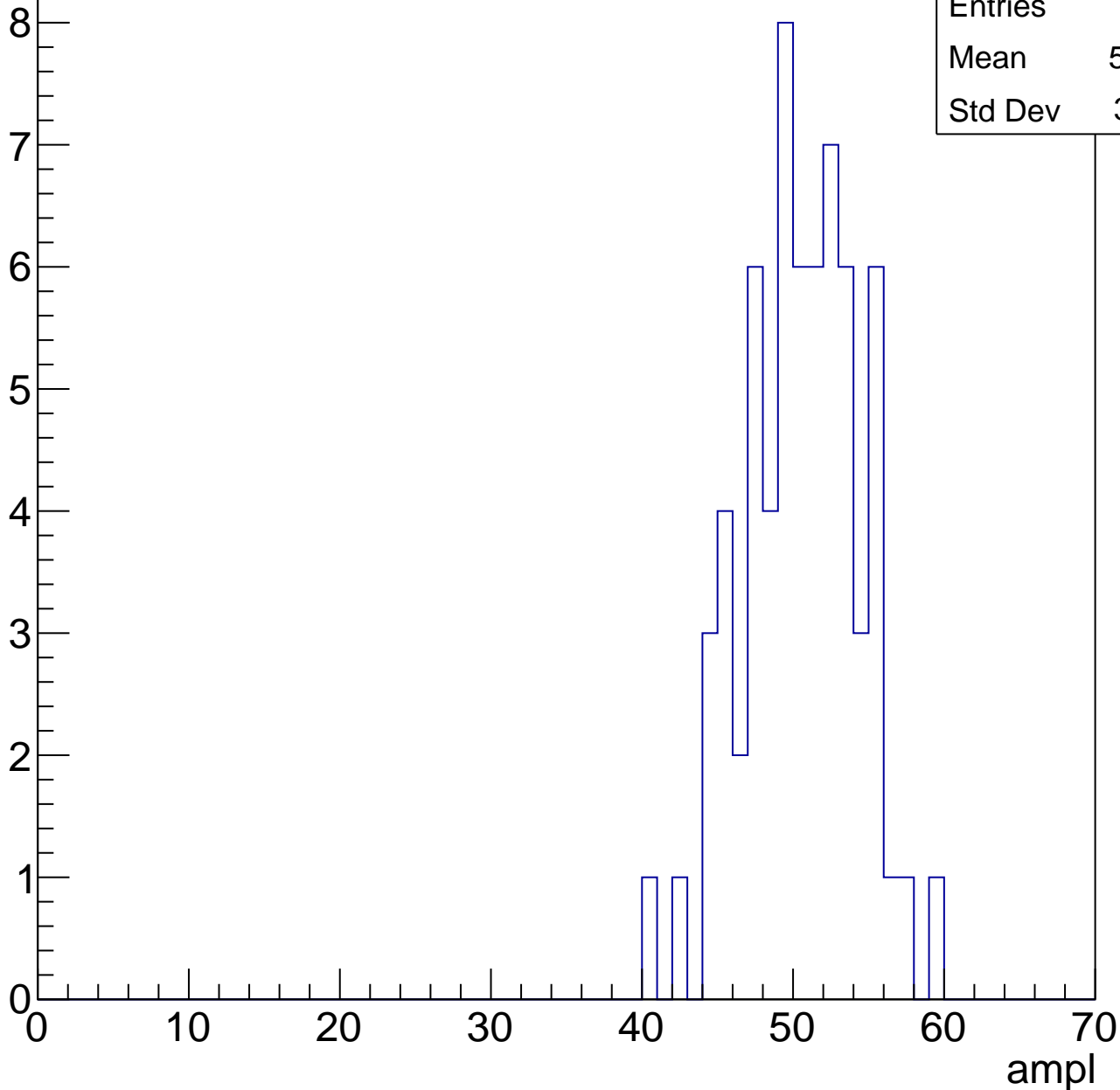


# B1L101S, U18-ch62, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	50.06
Std Dev	3.761

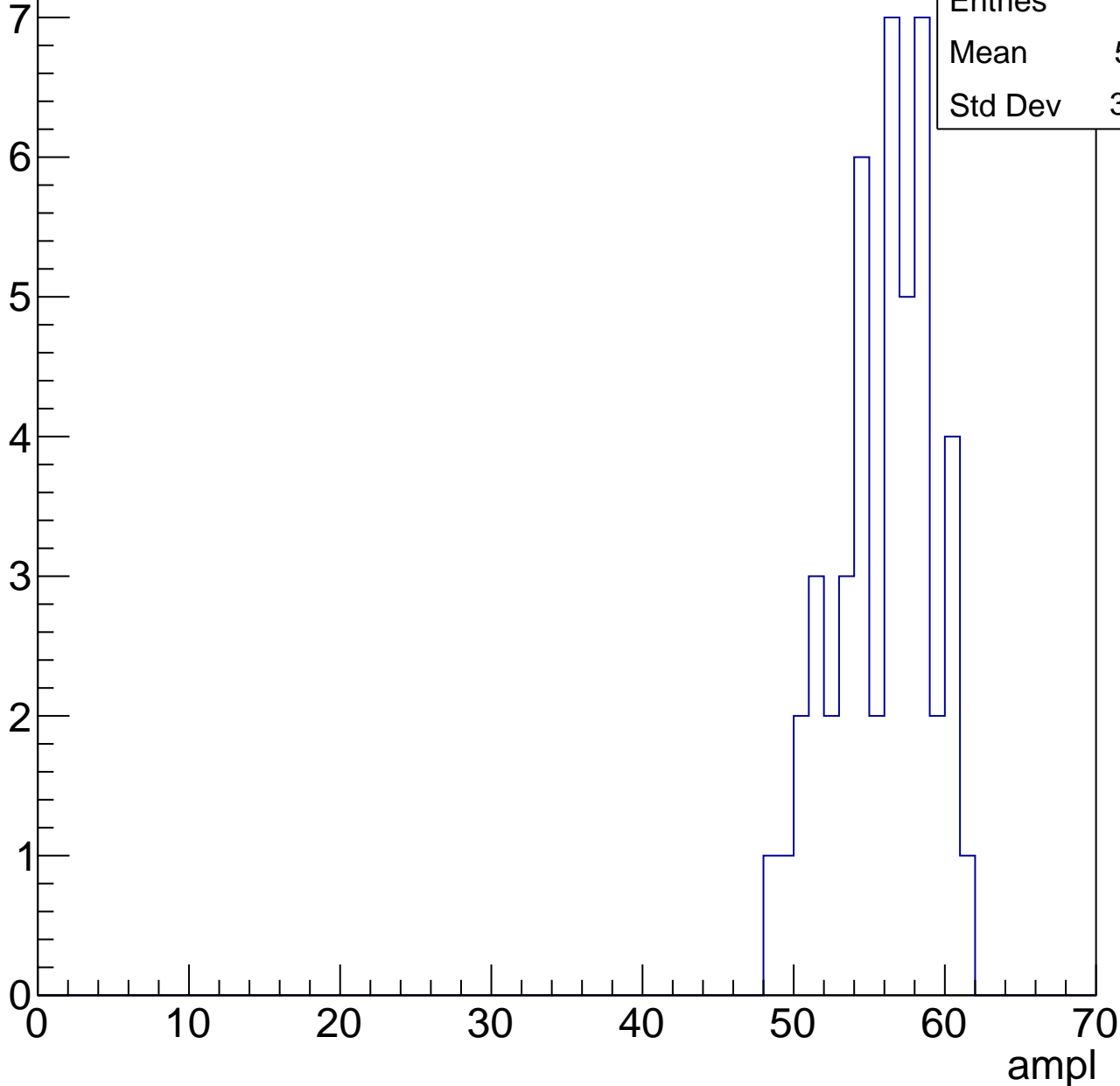


# B1L101S, U18-ch62, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	46
Mean	55.41
Std Dev	3.194

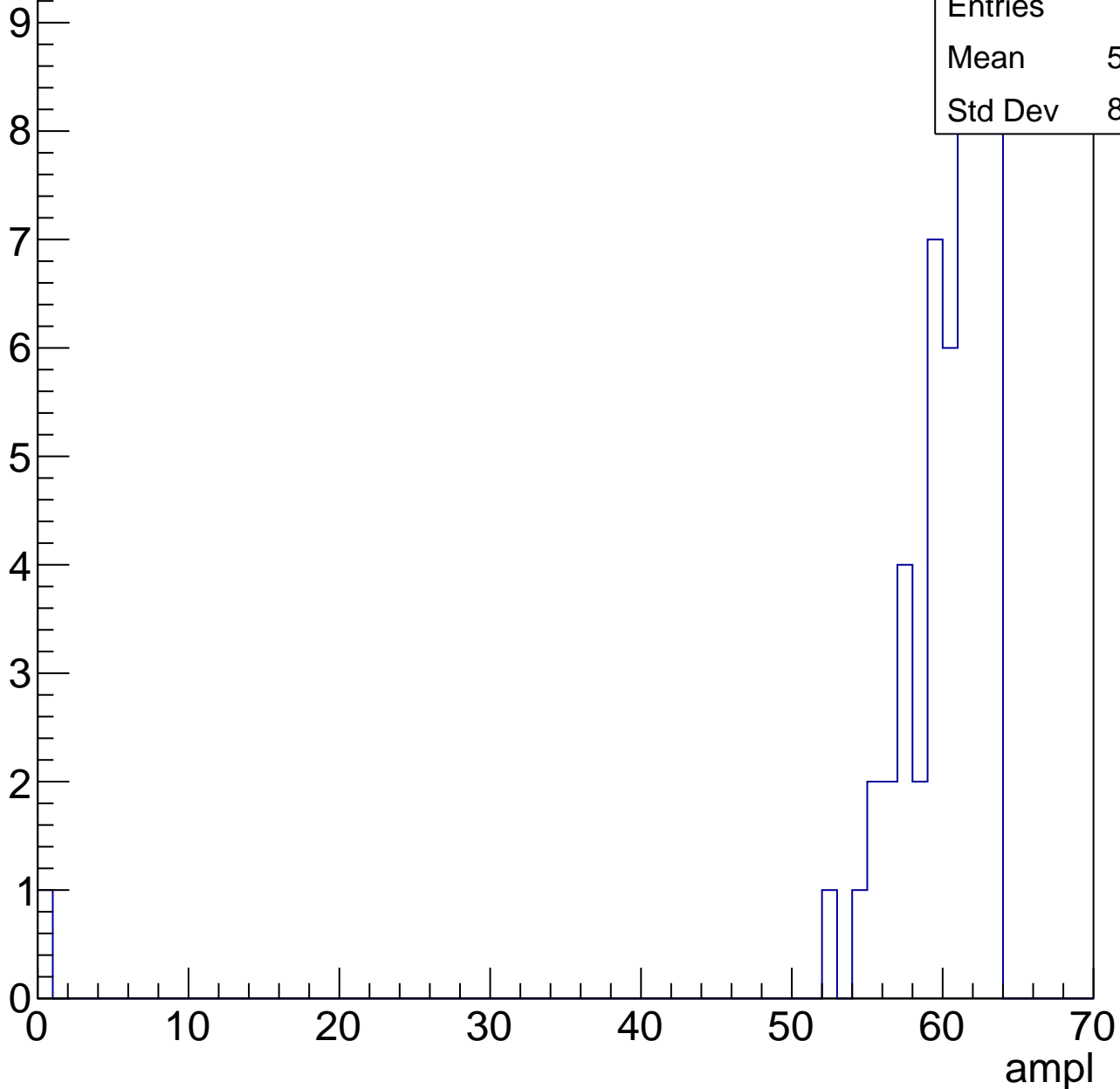


# B1L101S, U18-ch62, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

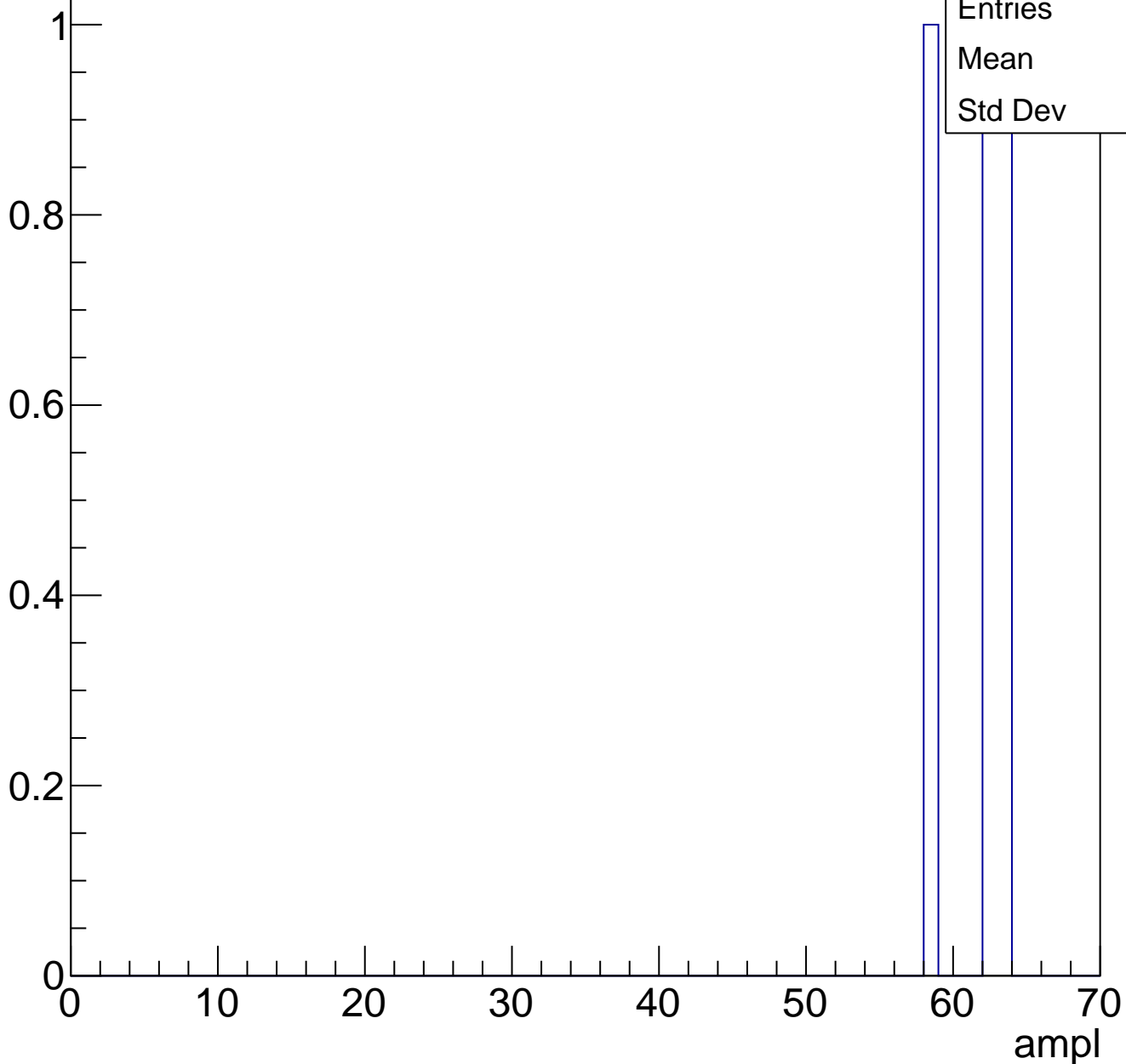
Entries	53
Mean	58.85
Std Dev	8.566



# B1L101S, U18-ch62, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch62, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U18-ch63, adc0

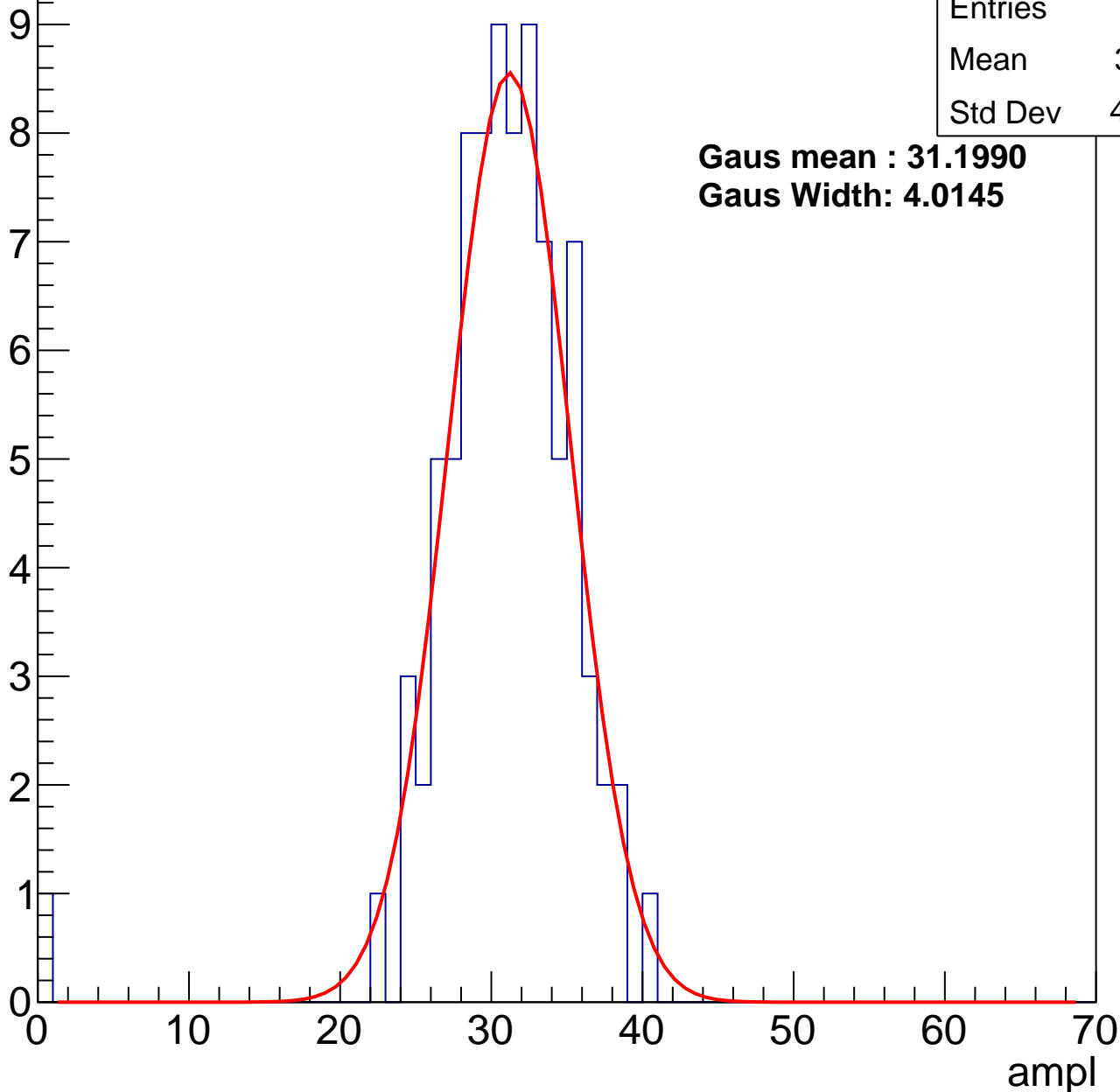
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	86
Mean	30.41
Std Dev	4.905

**Gaus mean : 31.1990**

**Gaus Width: 4.0145**



# B1L101S, U18-ch63, adc1

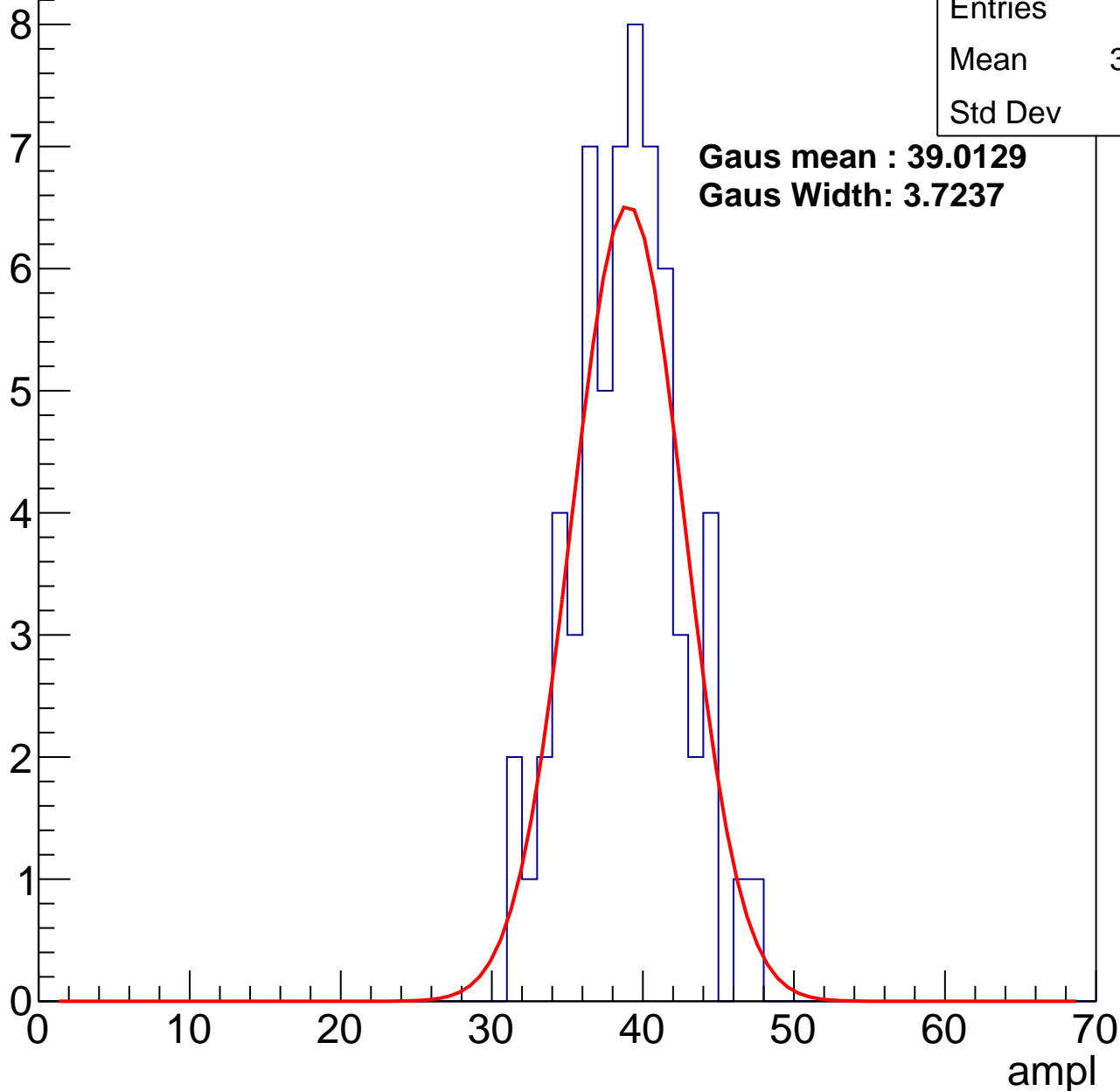
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	38.46
Std Dev	3.5

**Gaus mean : 39.0129**

**Gaus Width: 3.7237**



# B1L101S, U18-ch63, adc2

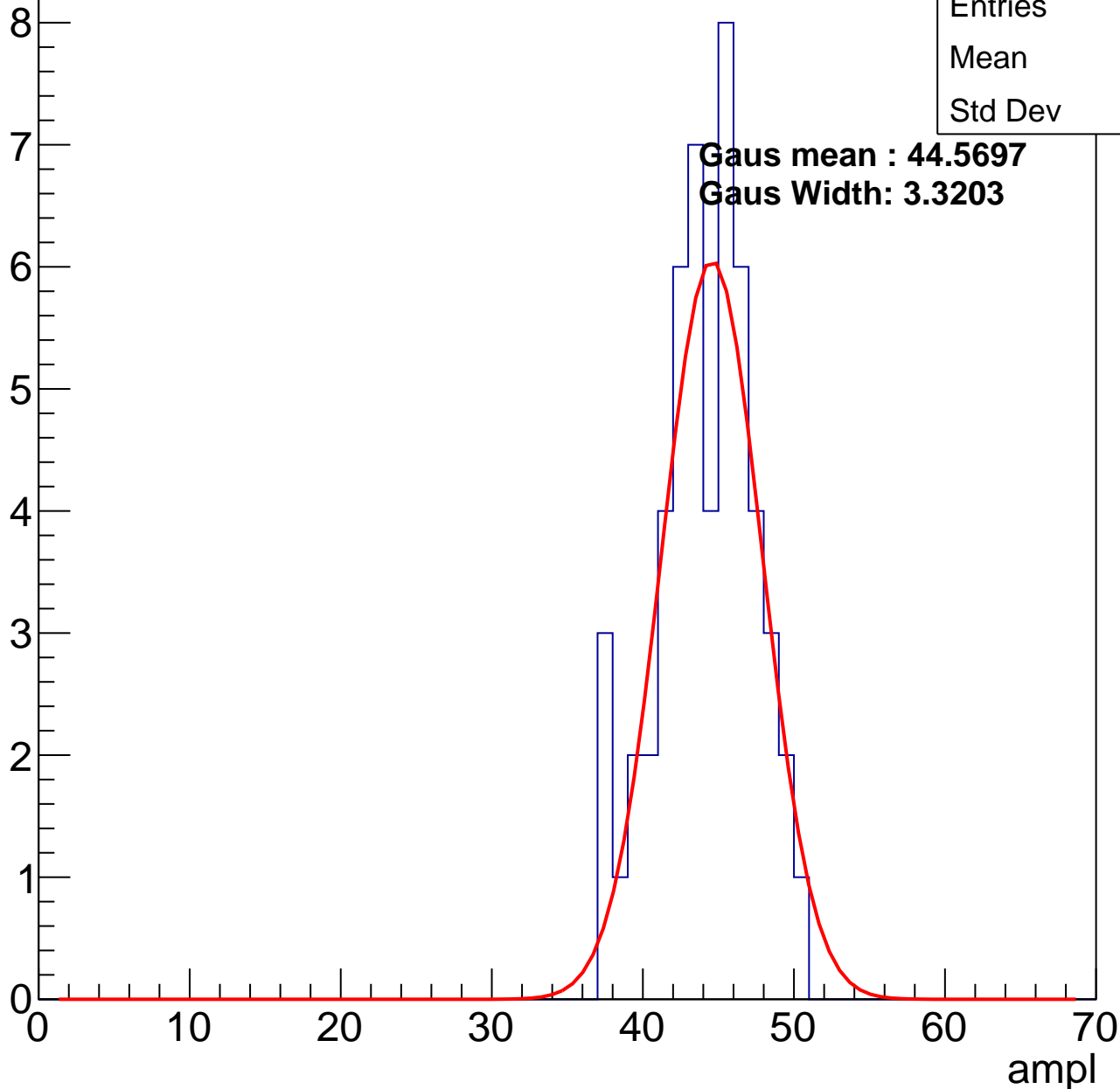
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	43.7
Std Dev	3.16

**Gaus mean : 44.5697**

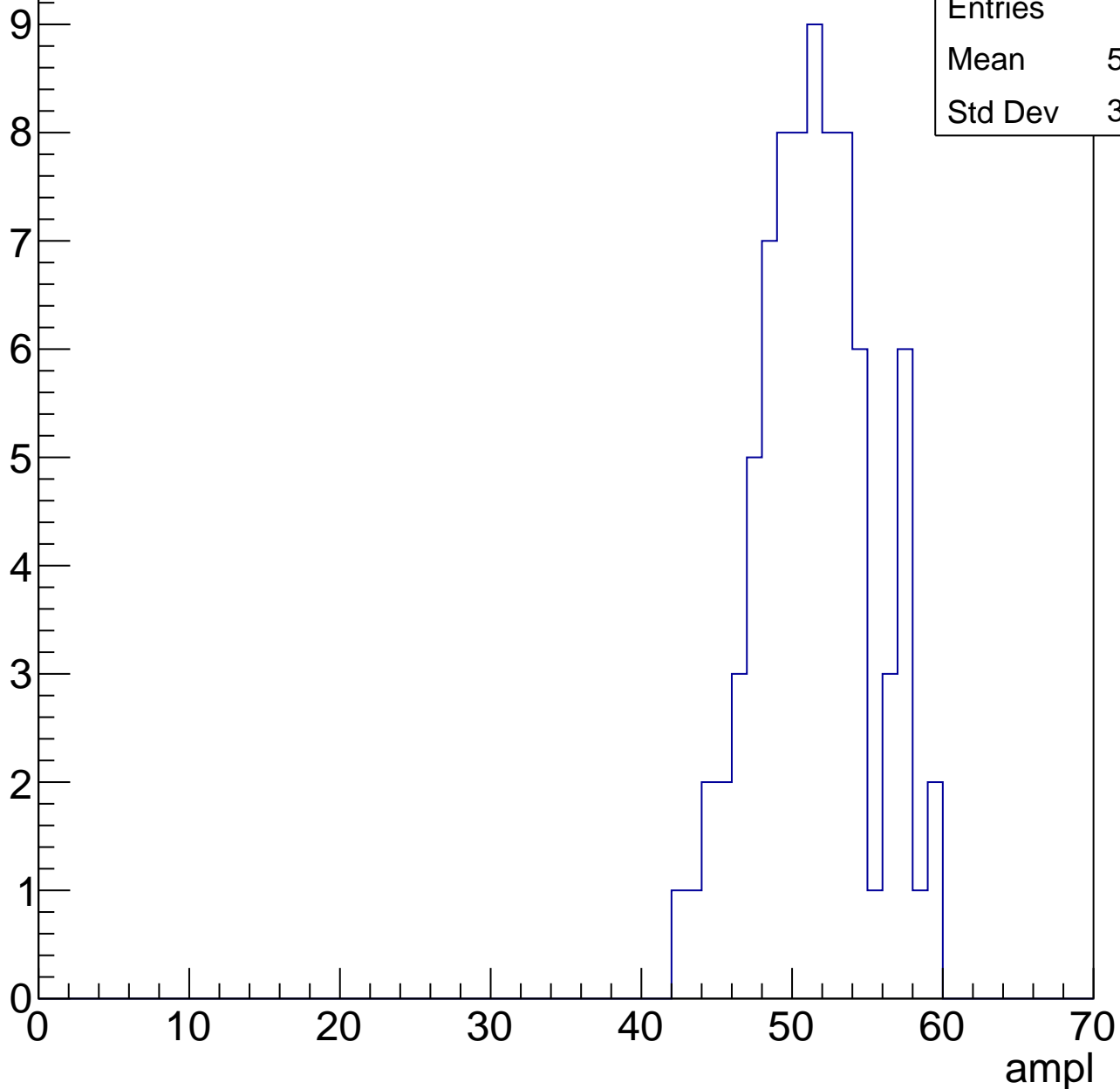
**Gaus Width: 3.3203**



# B1L101S, U18-ch63, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

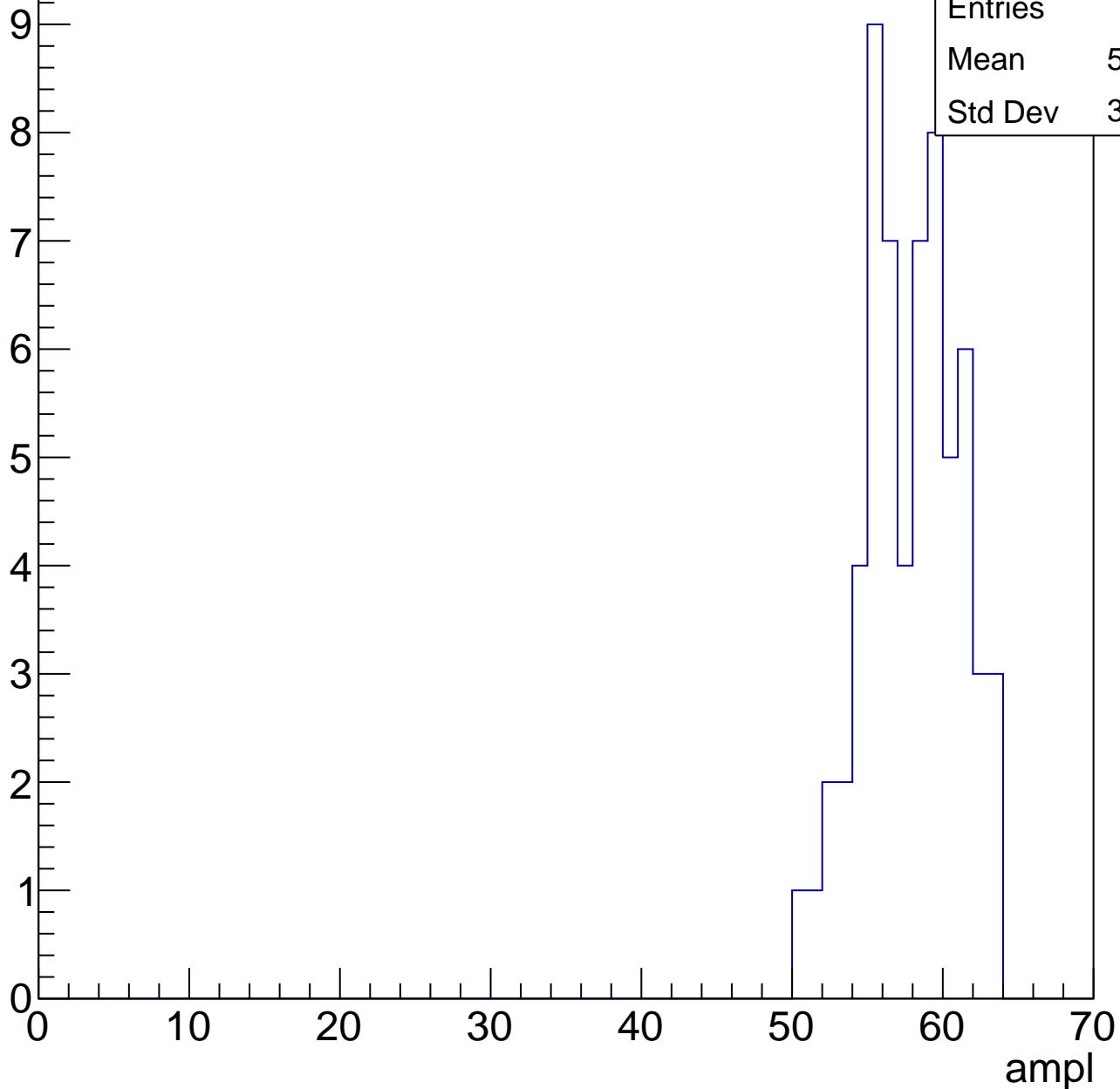


Entries	81
Mean	50.96
Std Dev	3.769

# B1L101S, U18-ch63, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

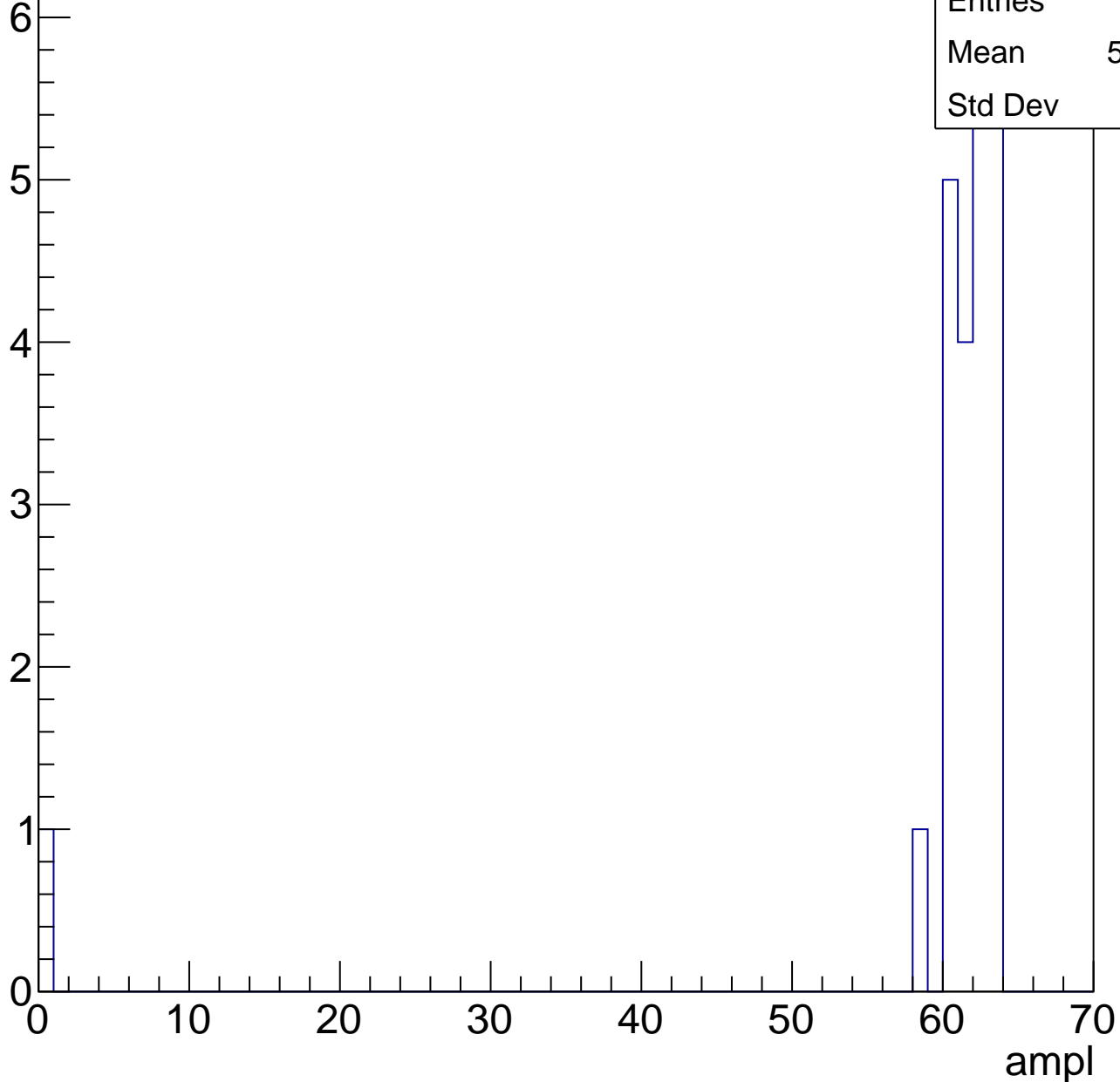


Entries	62
Mean	57.44
Std Dev	3.104

# B1L101S, U18-ch63, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

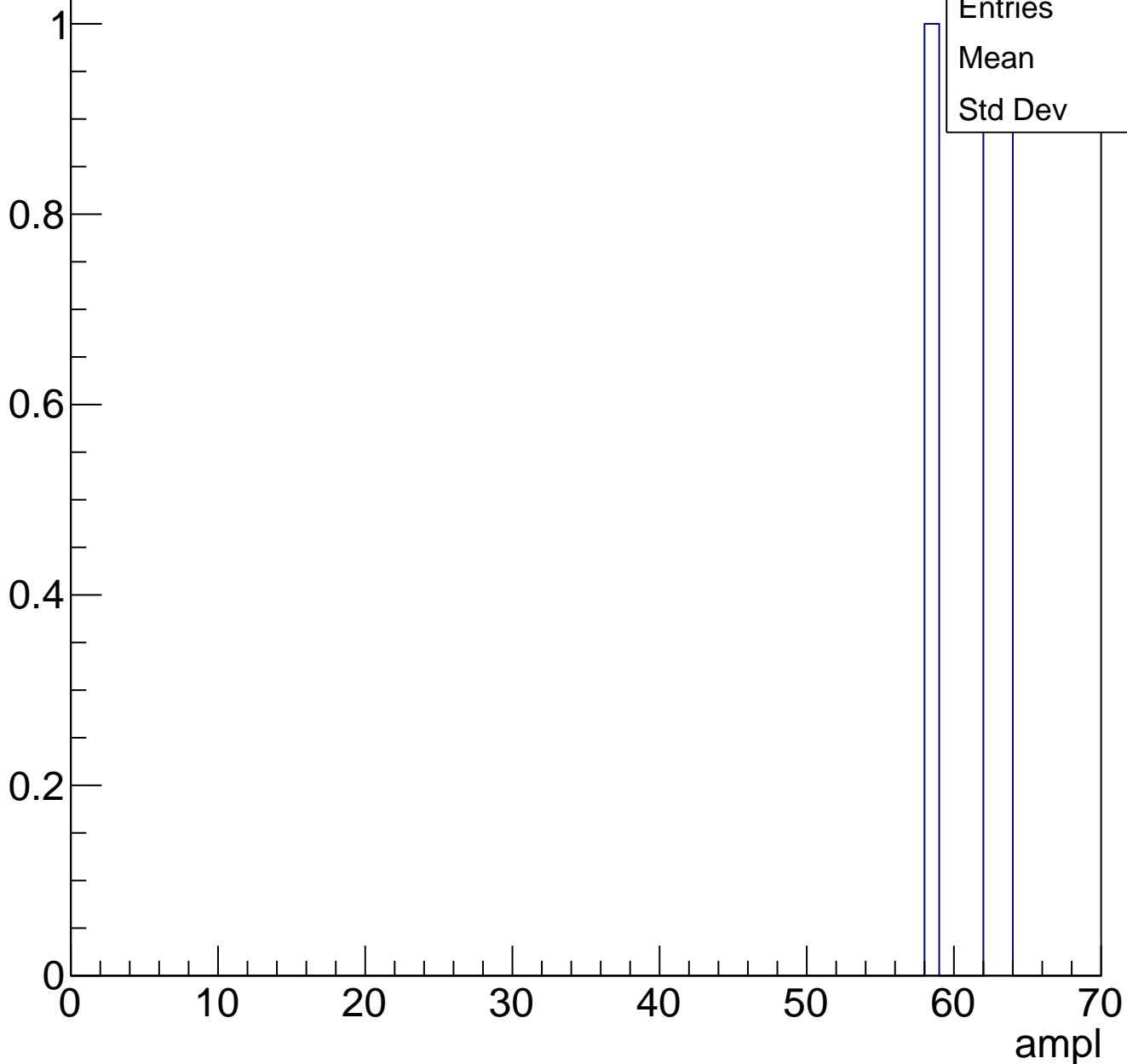
Entry



# B1L101S, U18-ch63, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch63, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U18-ch64, adc0

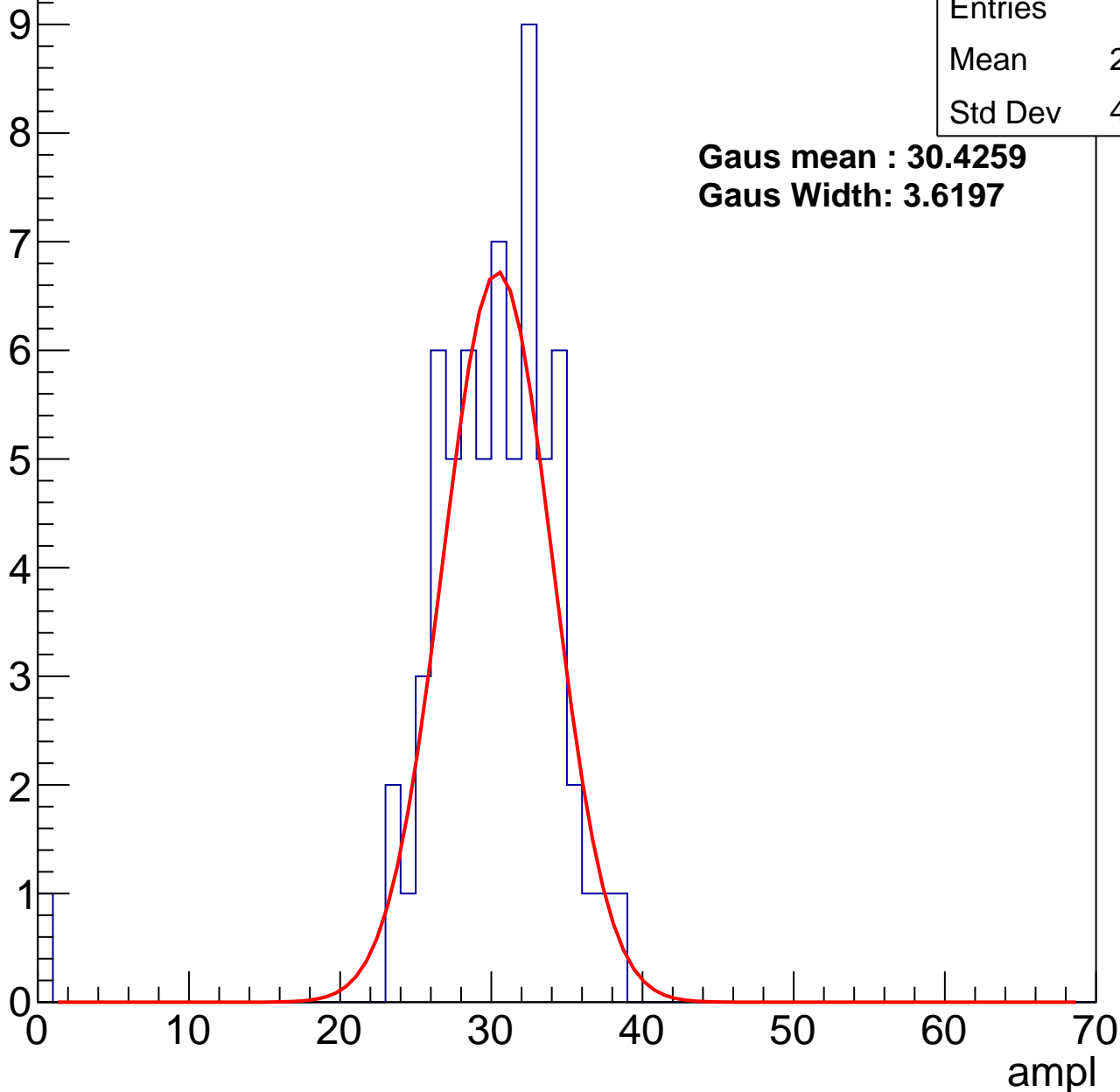
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	29.58
Std Dev	4.997

**Gaus mean : 30.4259**

**Gaus Width: 3.6197**



# B1L101S, U18-ch64, adc1

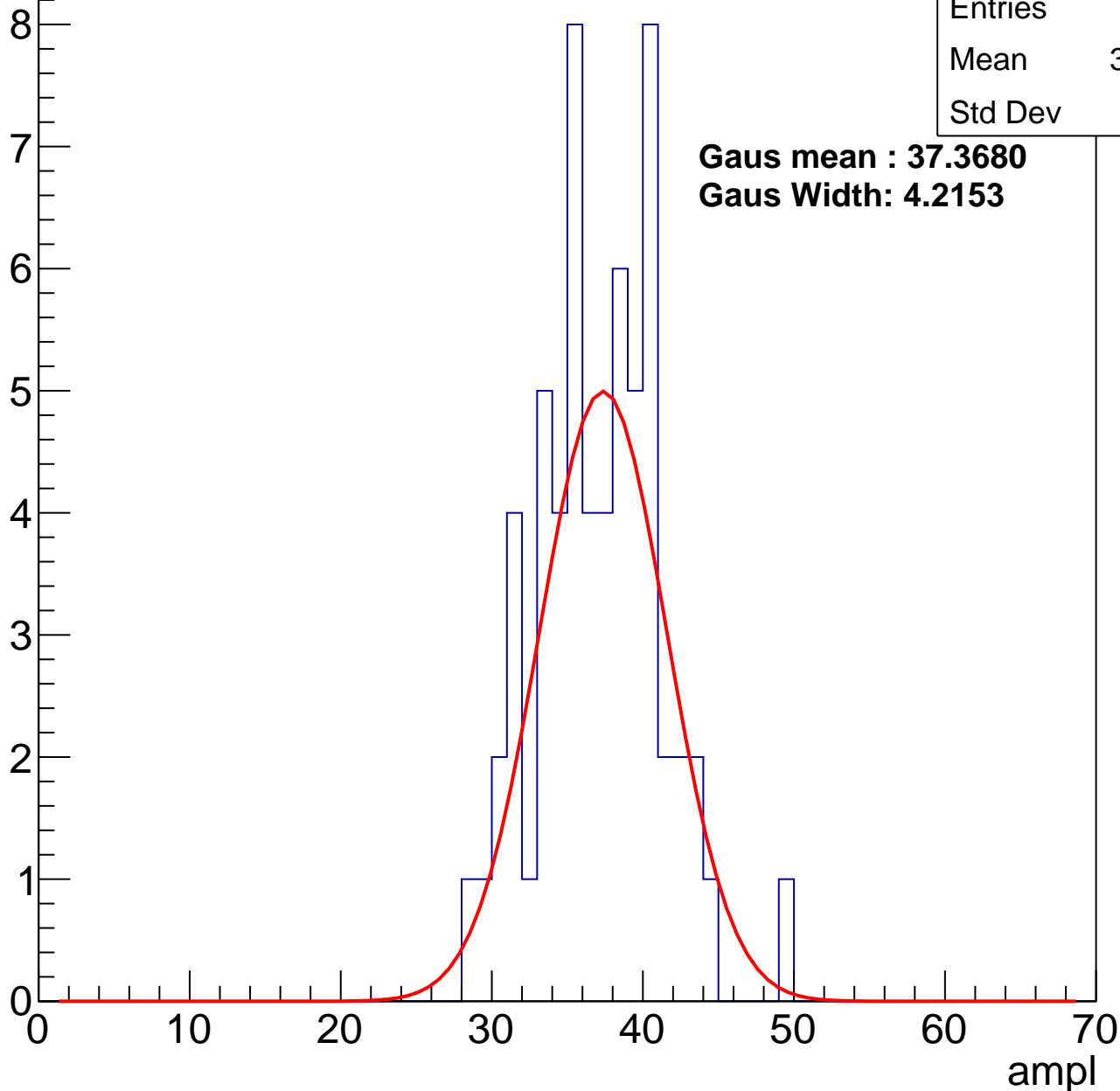
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	36.62
Std Dev	4.05

**Gaus mean : 37.3680**

**Gaus Width: 4.2153**



# B1L101S, U18-ch64, adc2

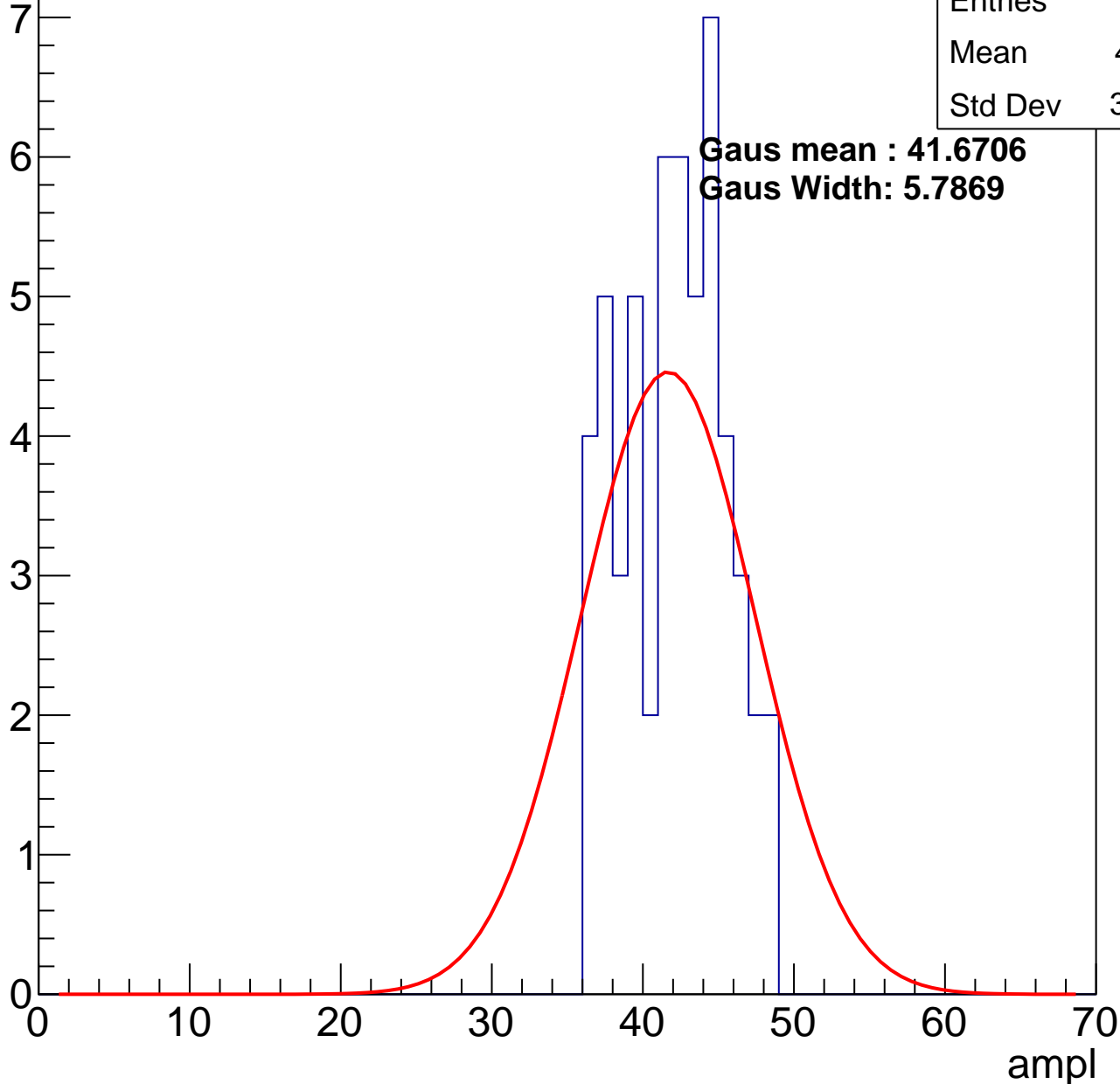
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	41.61
Std Dev	3.352

**Gaus mean : 41.6706**

**Gaus Width: 5.7869**

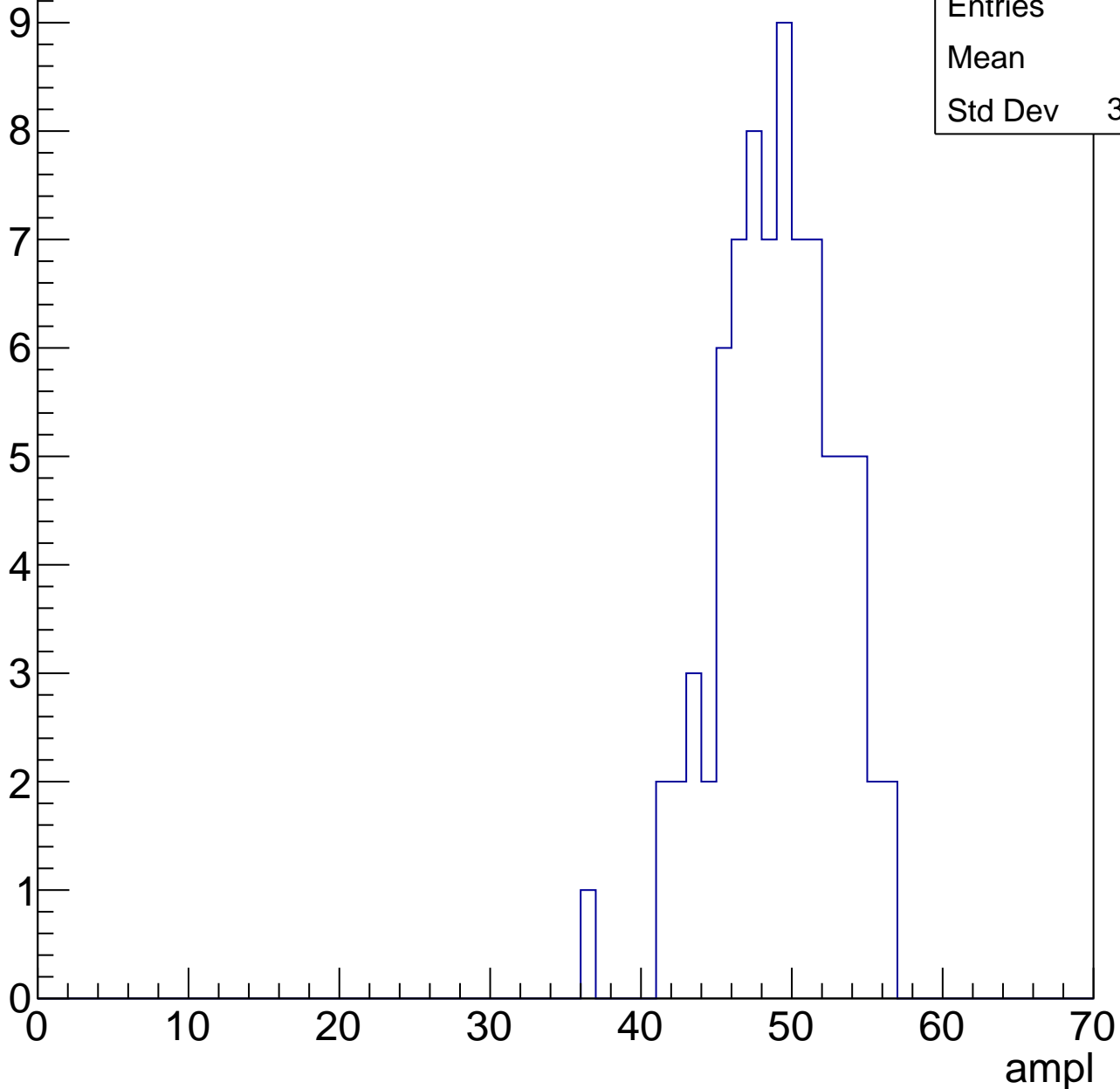


# B1L101S, U18-ch64, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	80
Mean	48.6
Std Dev	3.862

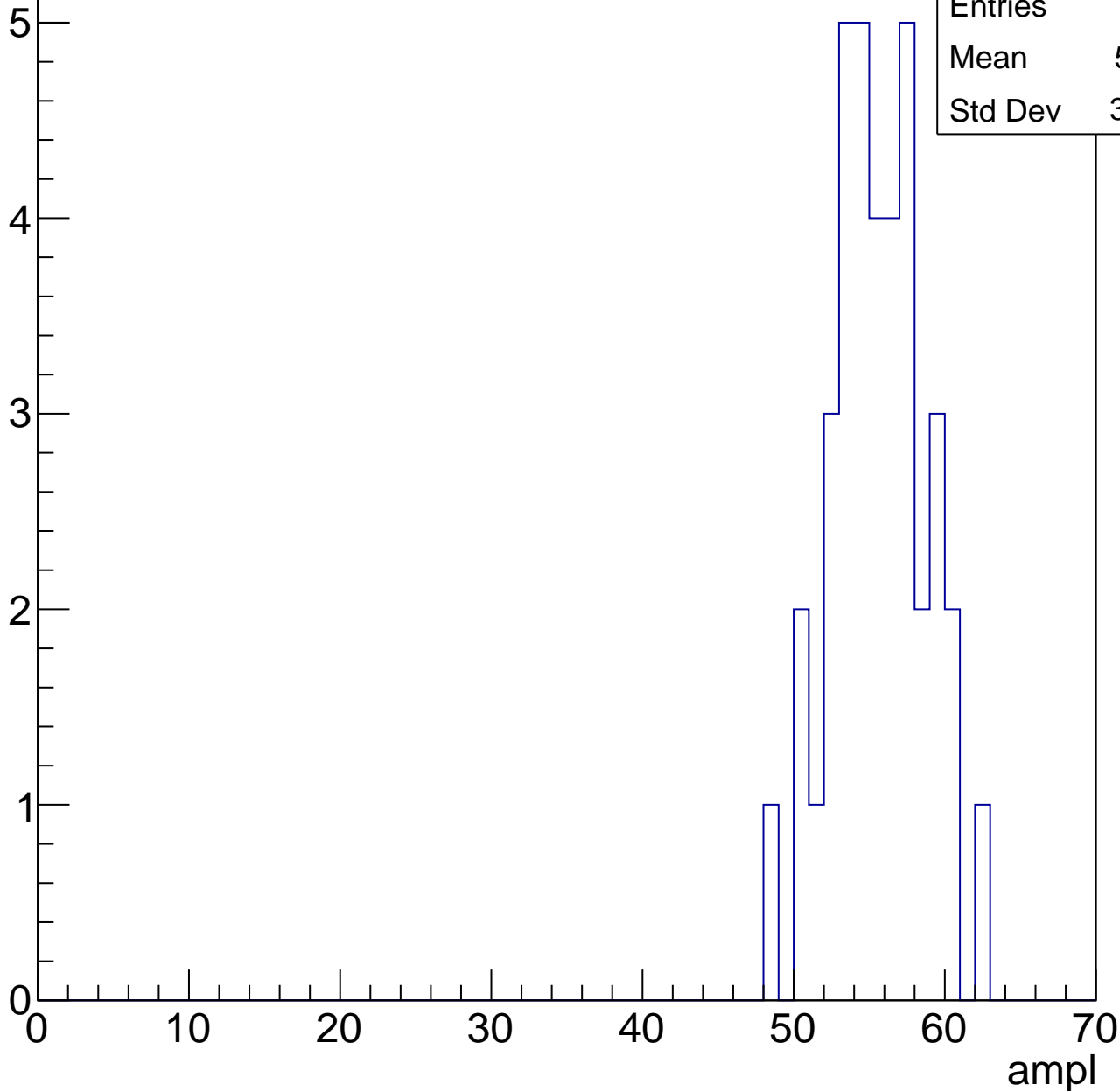


# B1L101S, U18-ch64, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	38
Mean	55.11
Std Dev	3.059



# B1L101S, U18-ch64, adc5

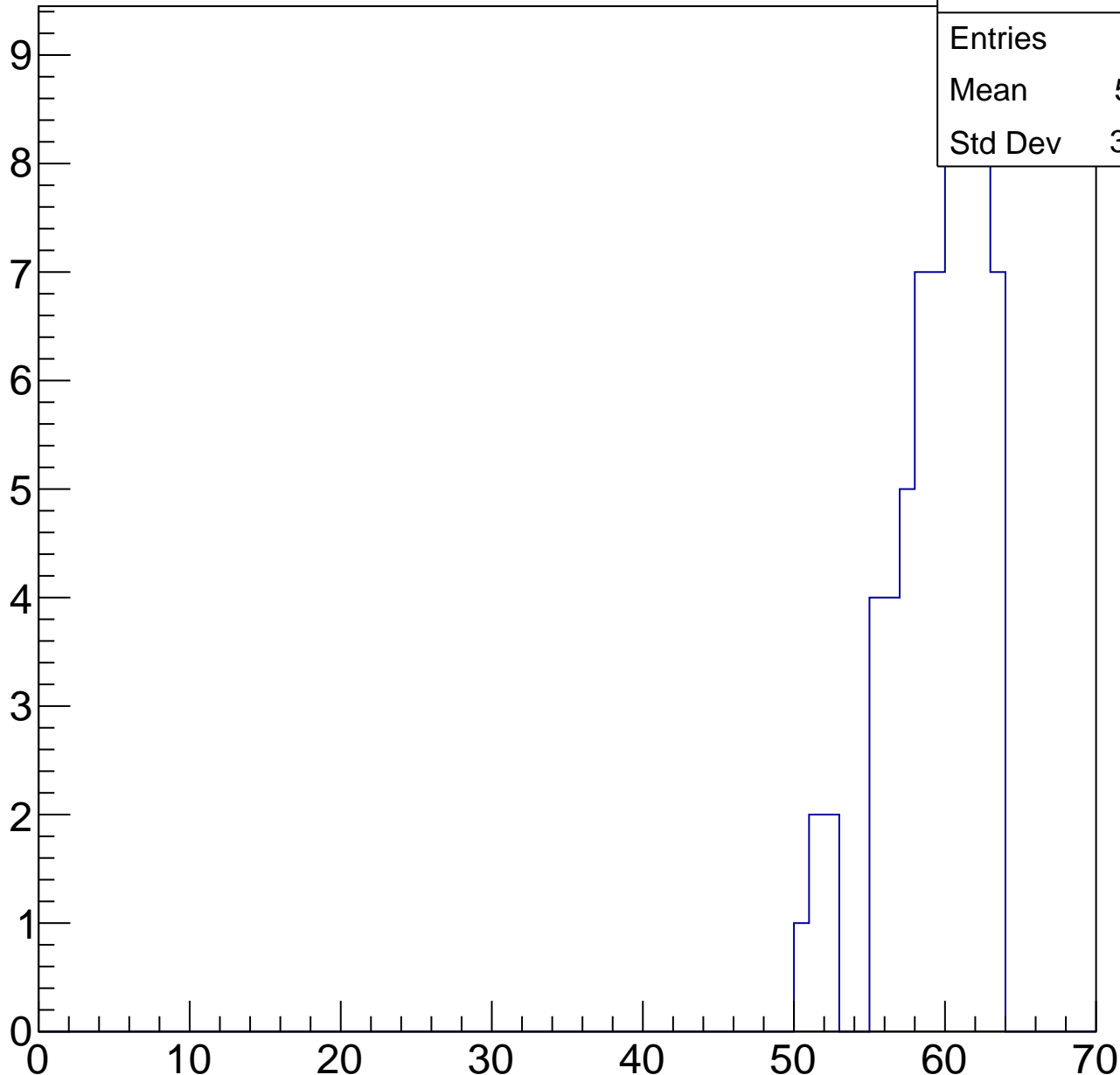
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	64
Mean	58.91
Std Dev	3.215

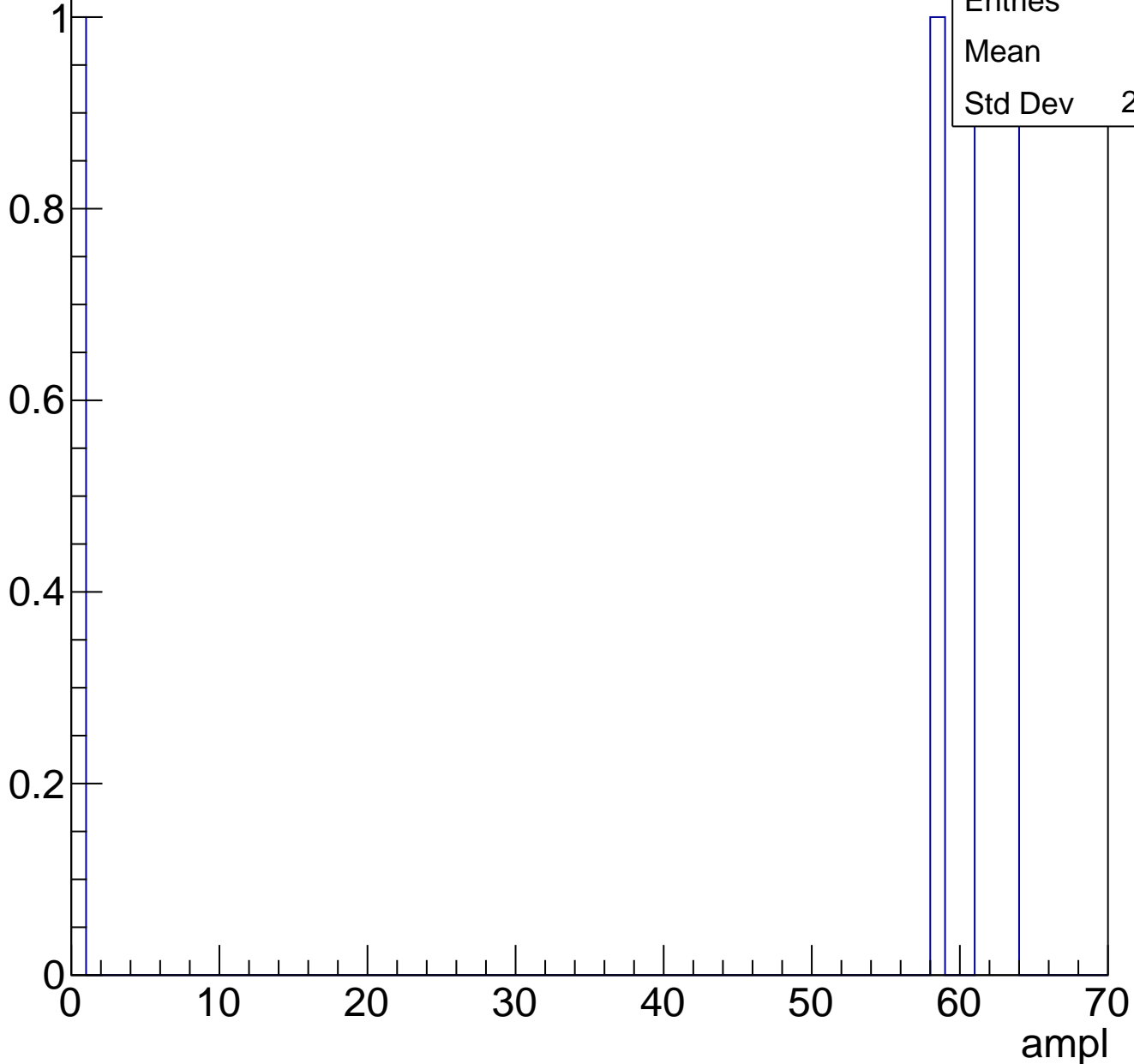
ampl



# B1L101S, U18-ch64, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch64, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch65, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	101
Mean	30.97
Std Dev	4.067

**Gaus mean : 31.6909**

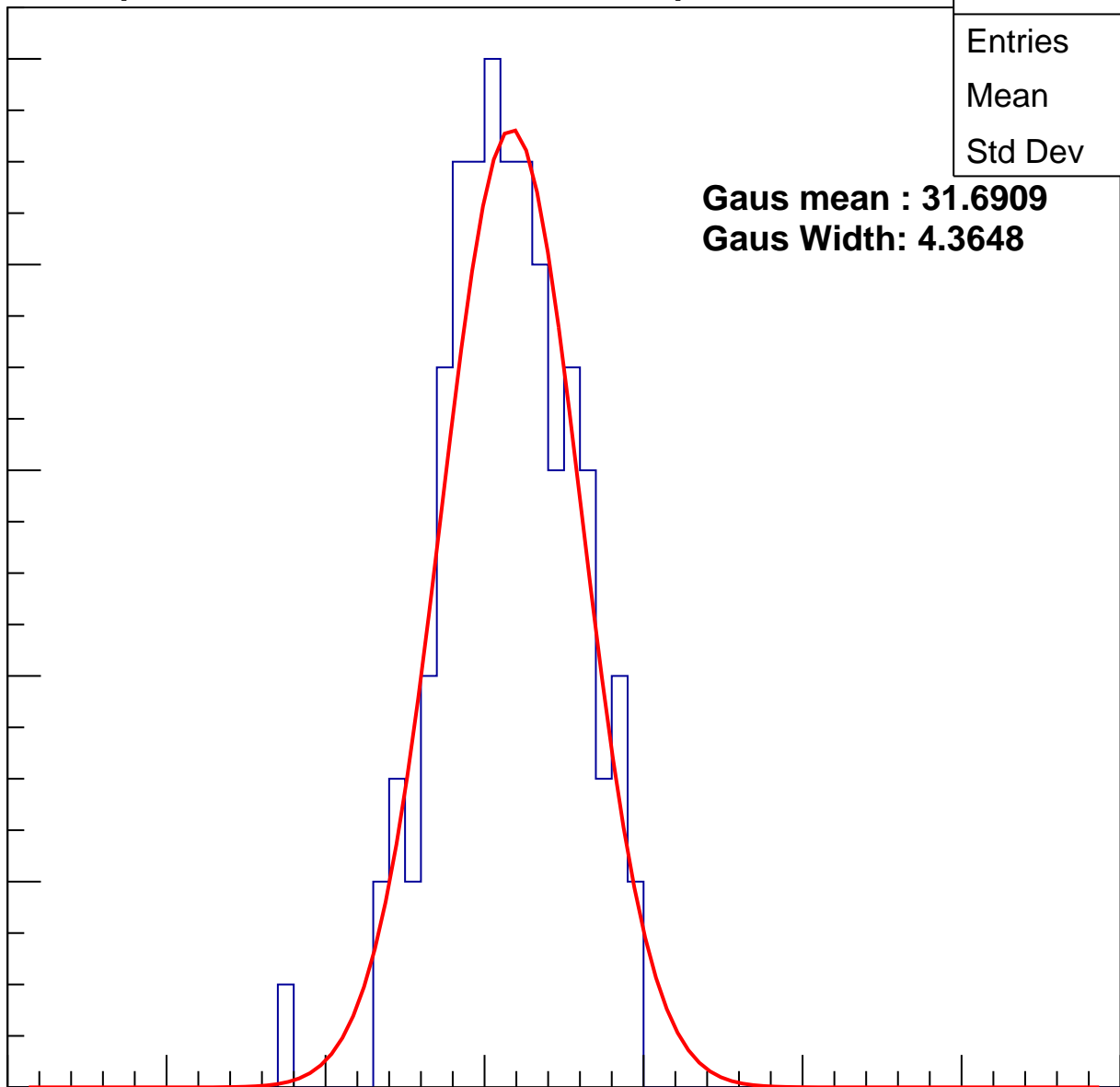
**Gaus Width: 4.3648**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U18-ch65, adc1

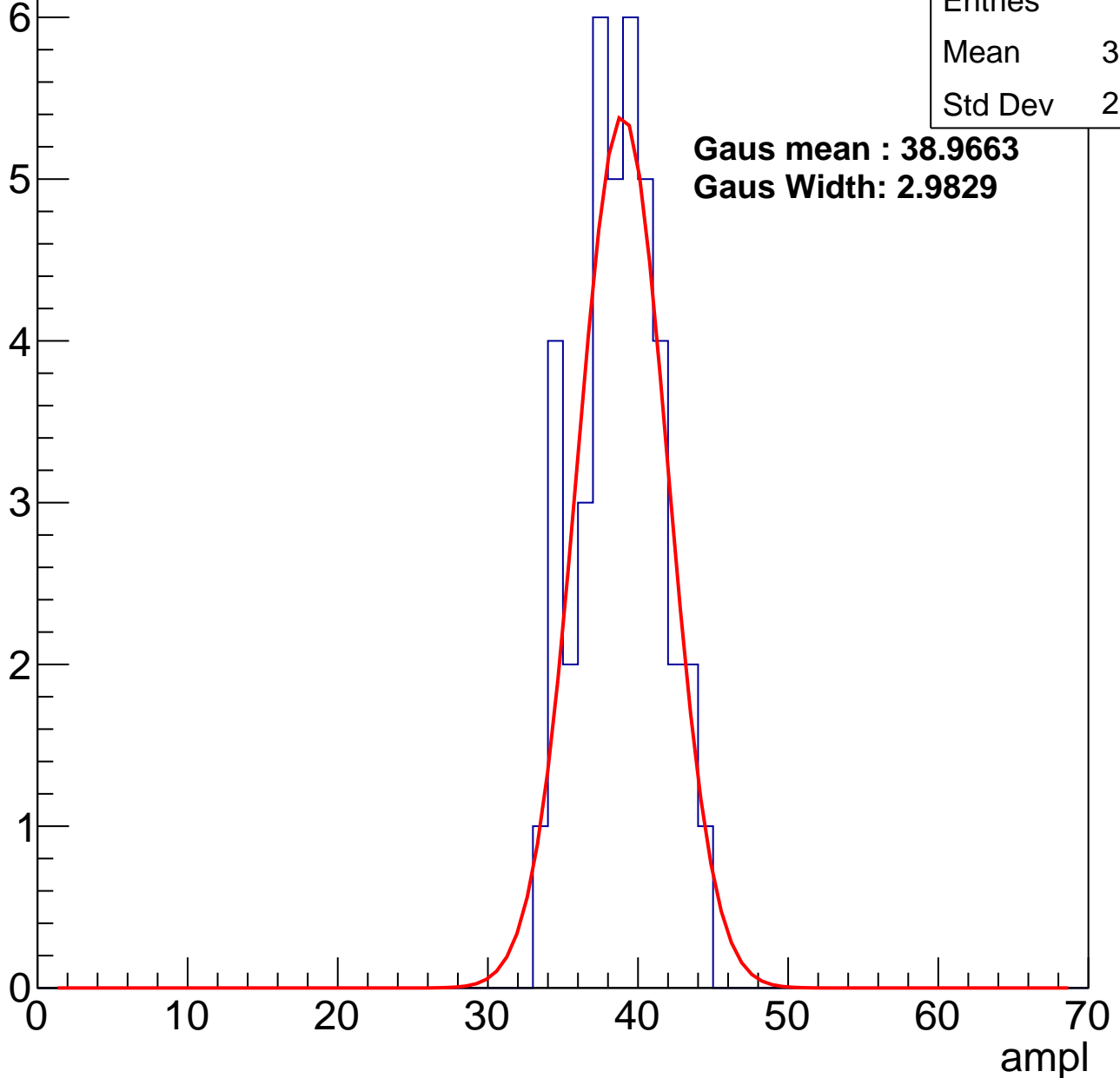
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	41
Mean	38.32
Std Dev	2.709

**Gaus mean : 38.9663**

**Gaus Width: 2.9829**

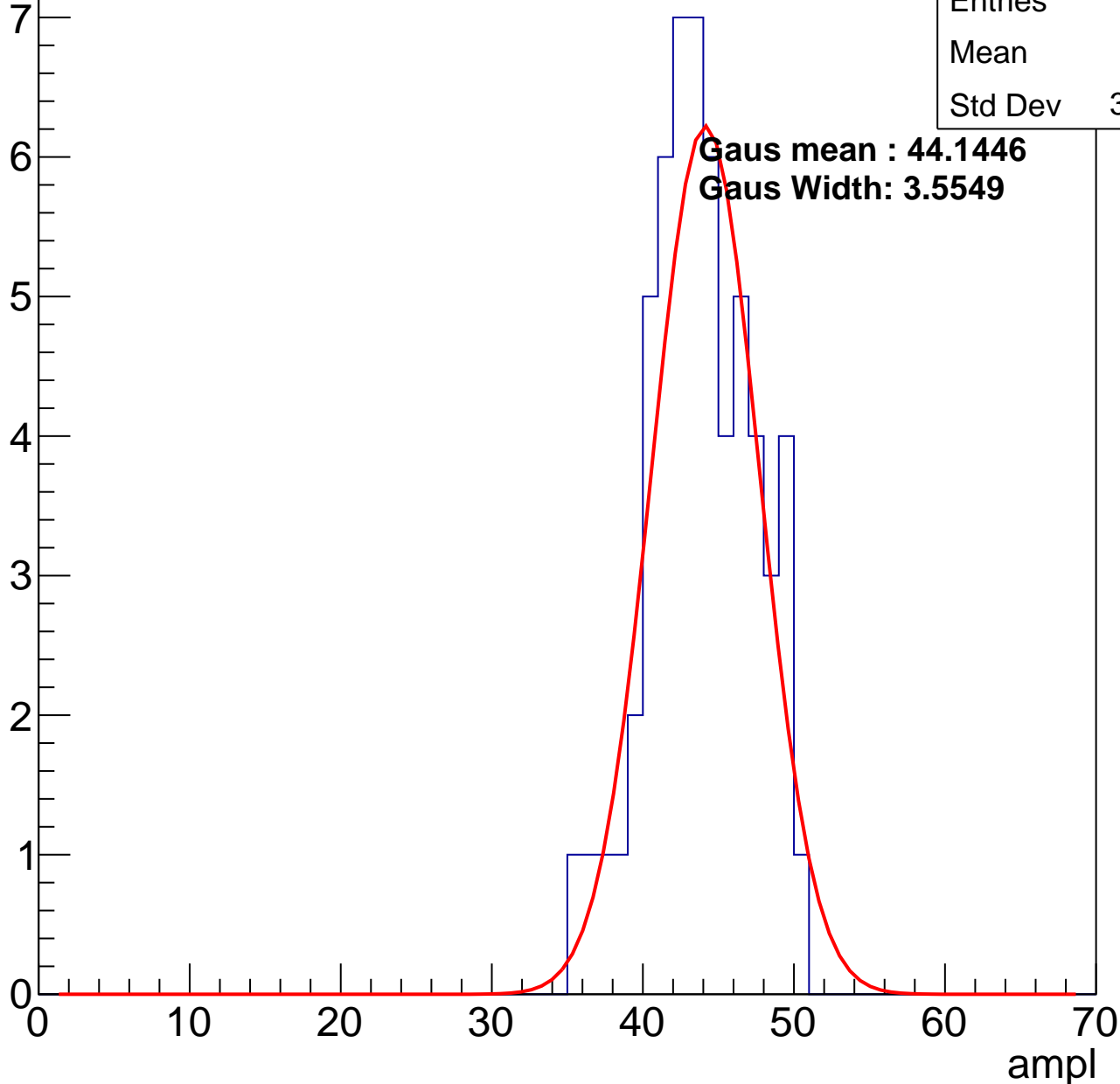


# B1L101S, U18-ch65, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	43.4
Std Dev	3.404

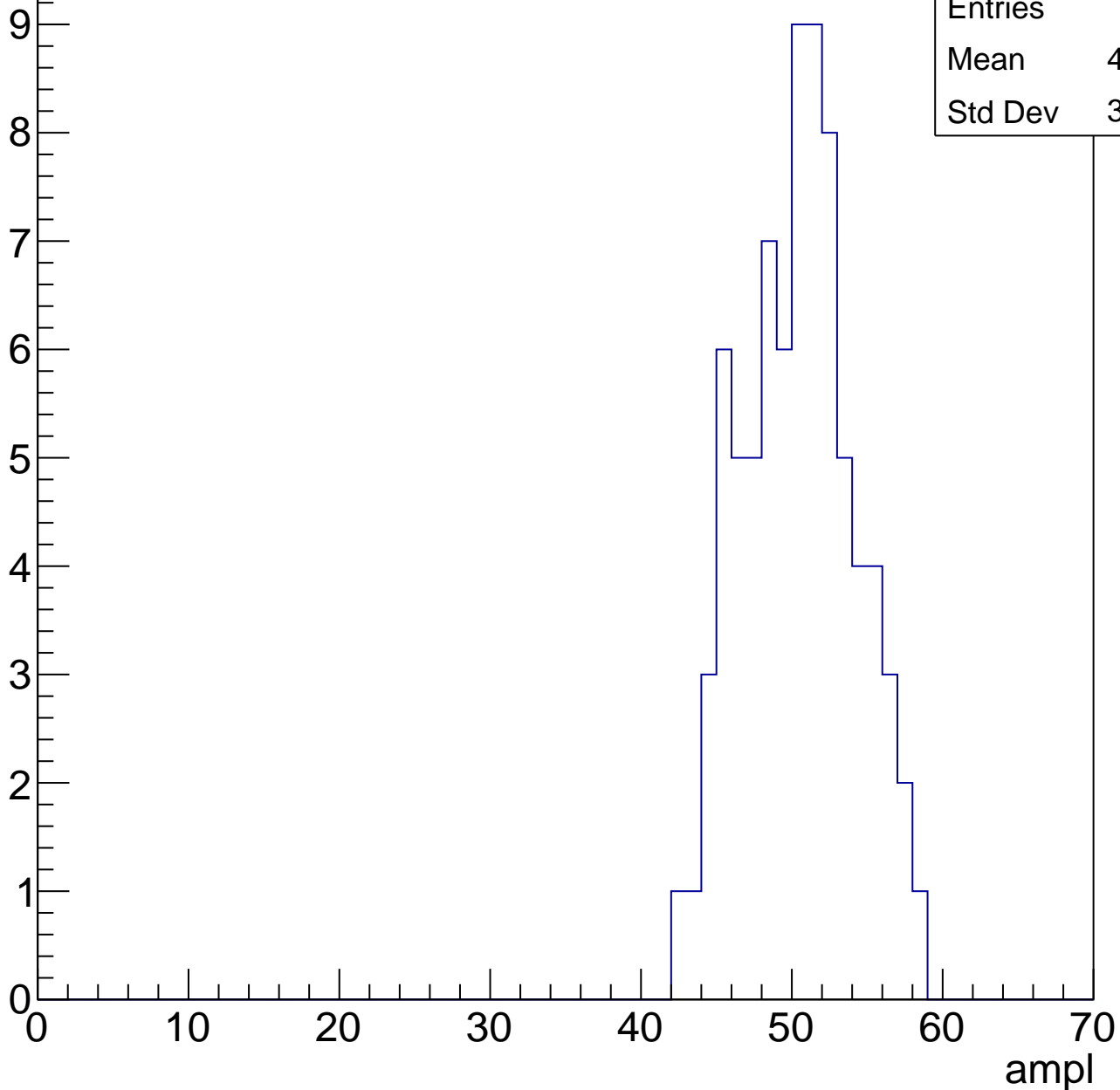


# B1L101S, U18-ch65, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	79
Mean	49.97
Std Dev	3.646

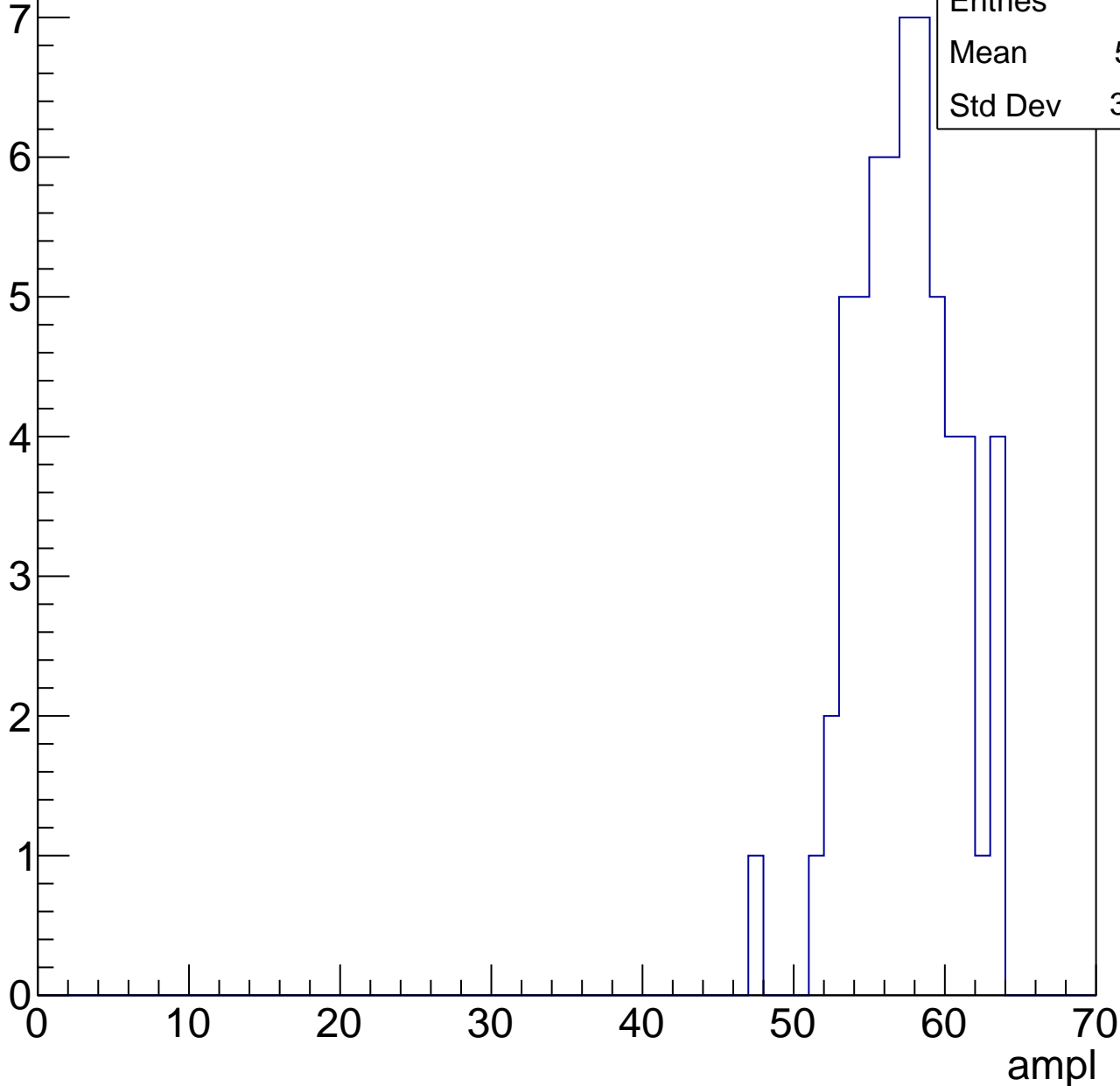


# B1L101S, U18-ch65, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	56.91
Std Dev	3.313

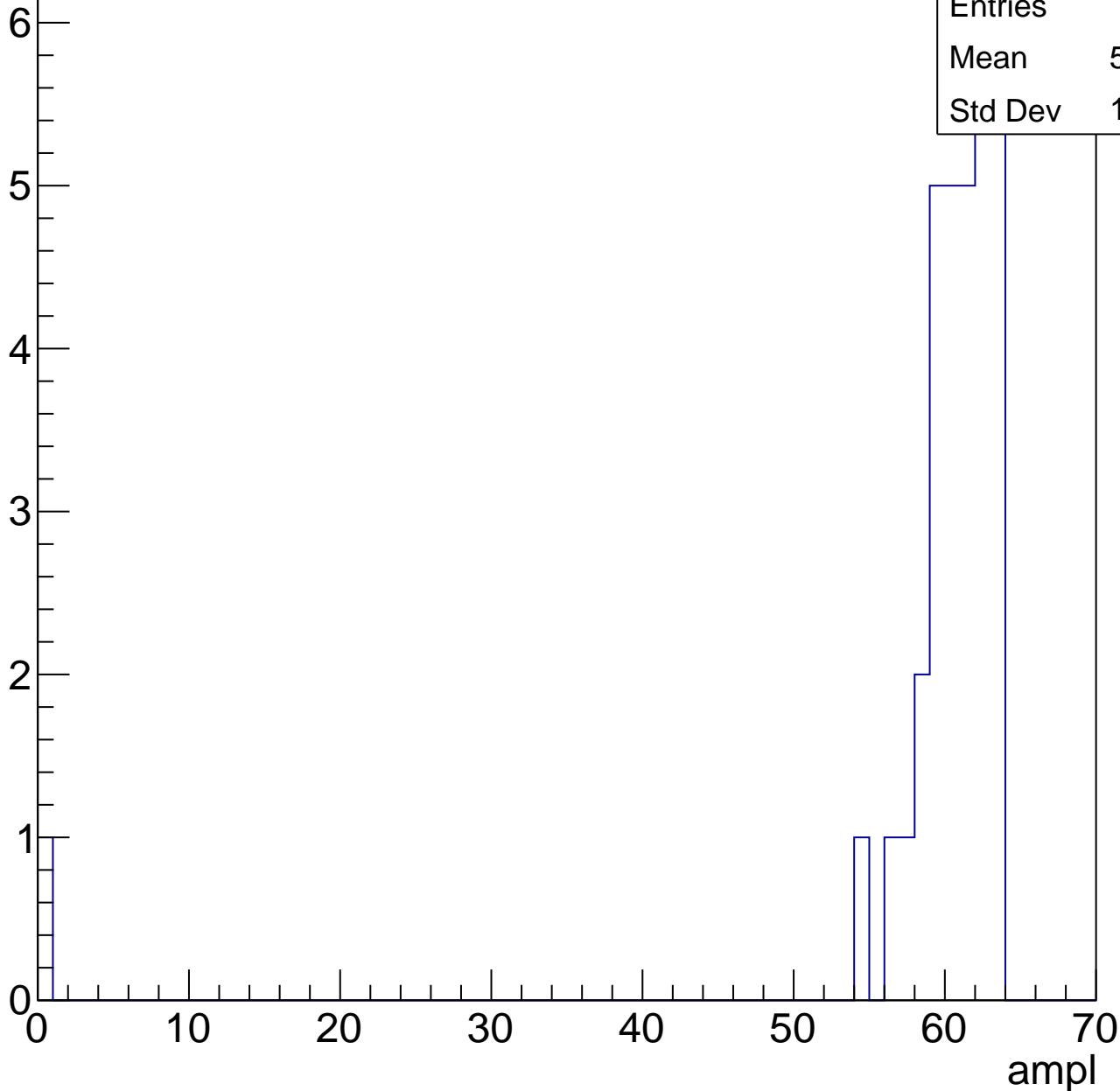


# B1L101S, U18-ch65, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

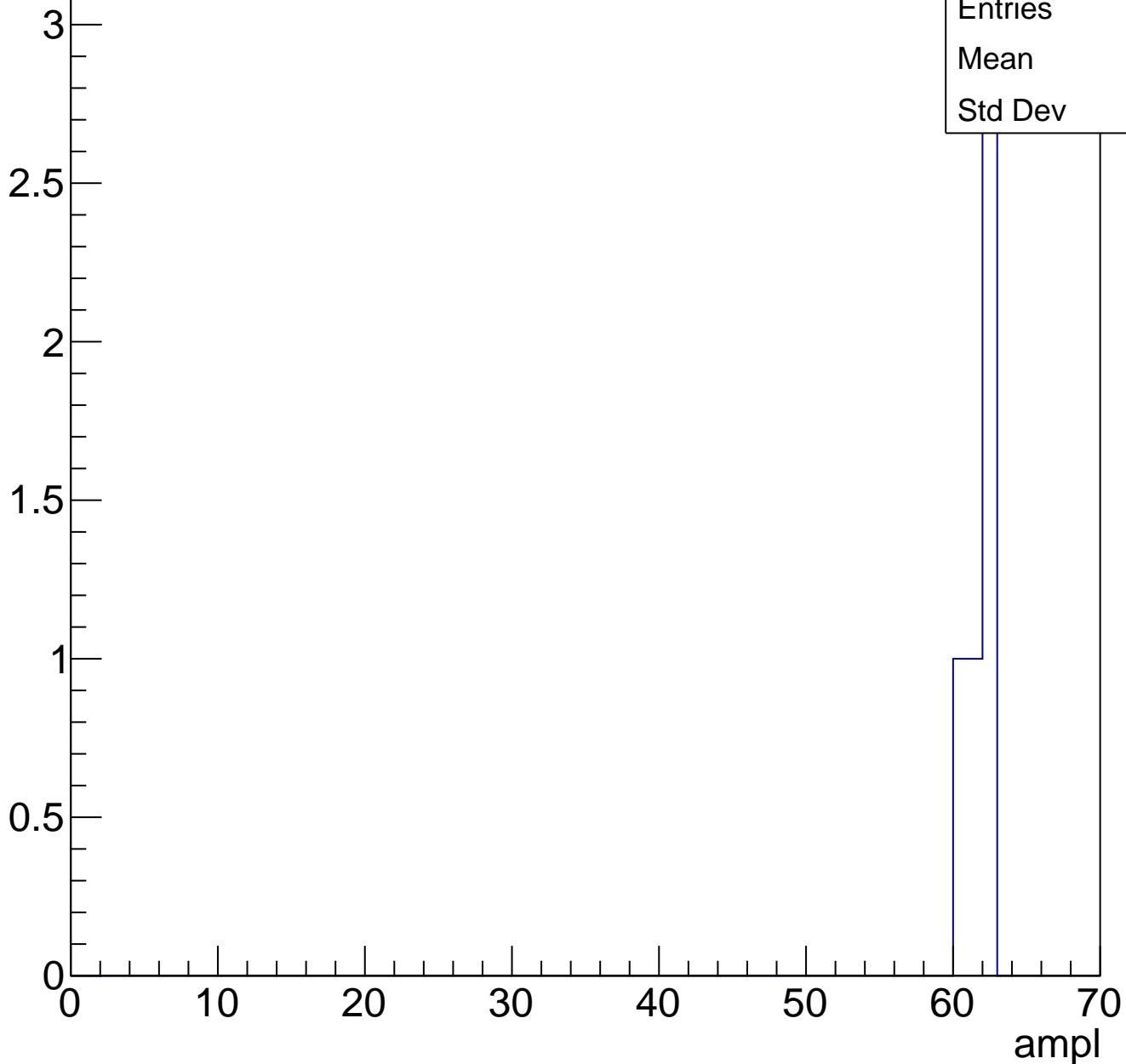
Entries	33
Mean	58.58
Std Dev	10.57



# B1L101S, U18-ch65, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch65, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U18-ch66, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	79
Mean	28.32
Std Dev	6.793

**Gaus mean : 30.0343**

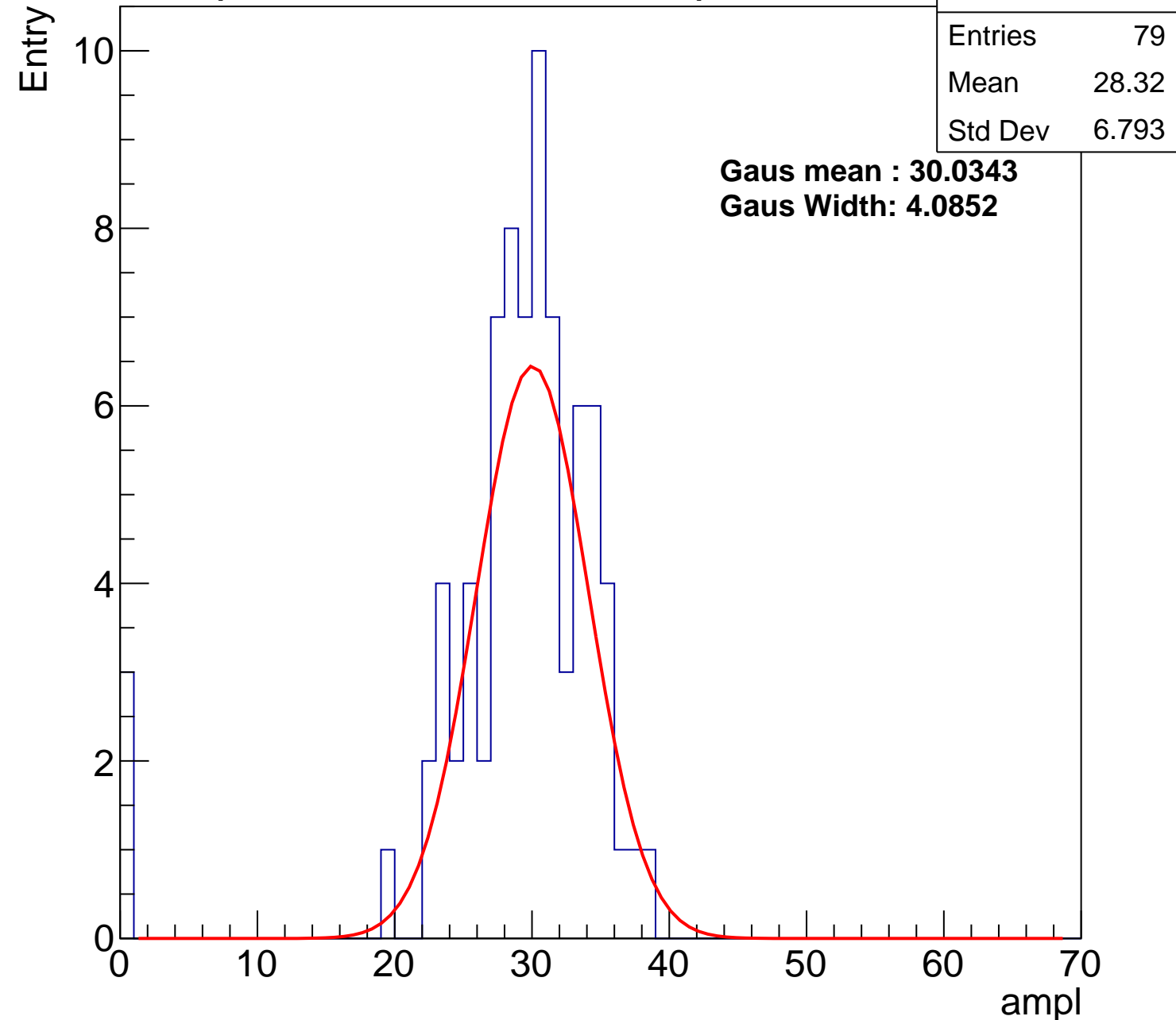
**Gaus Width: 4.0852**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U18-ch66, adc1

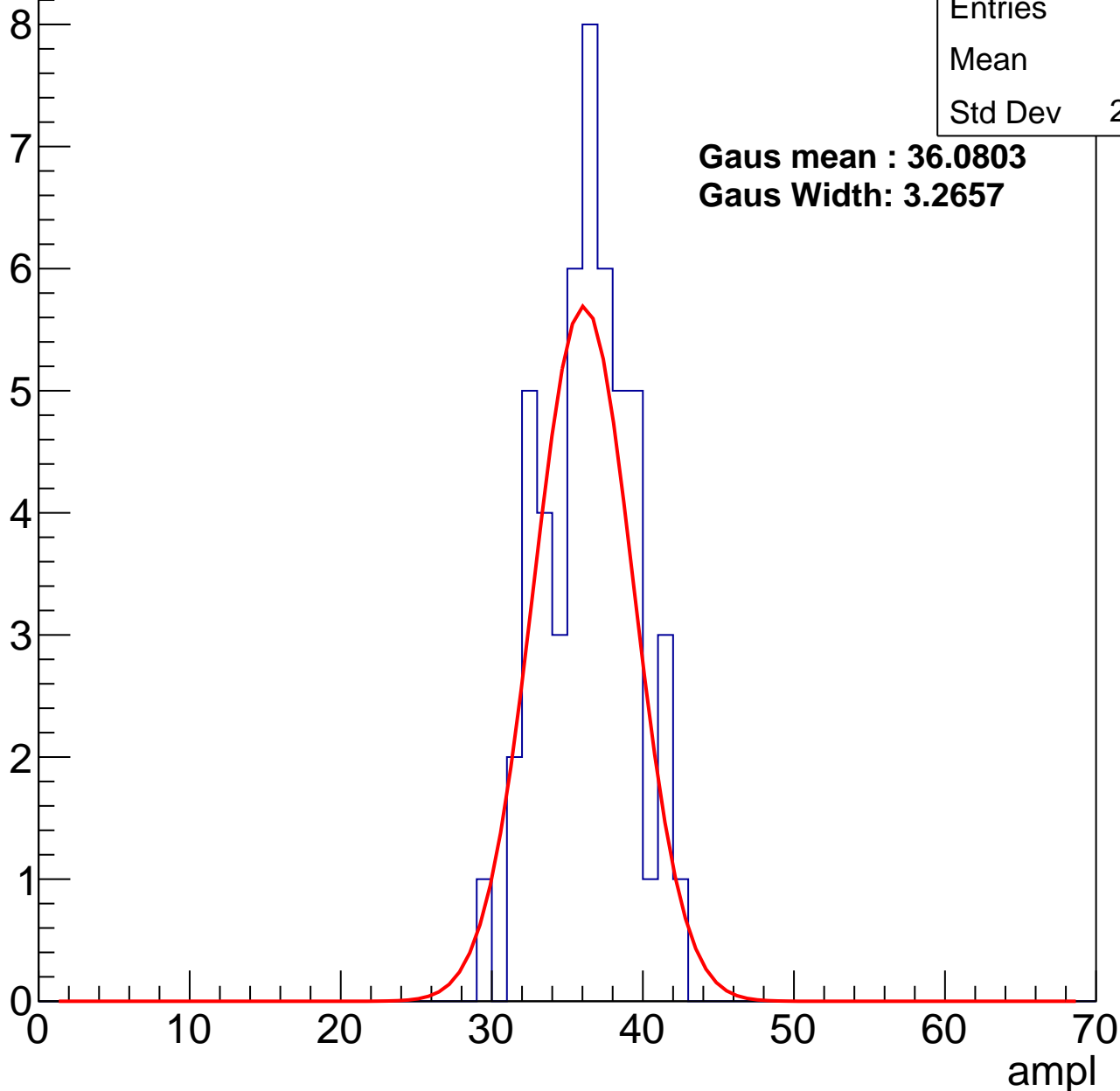
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	35.9
Std Dev	2.934

**Gaus mean : 36.0803**

**Gaus Width: 3.2657**



# B1L101S, U18-ch66, adc2

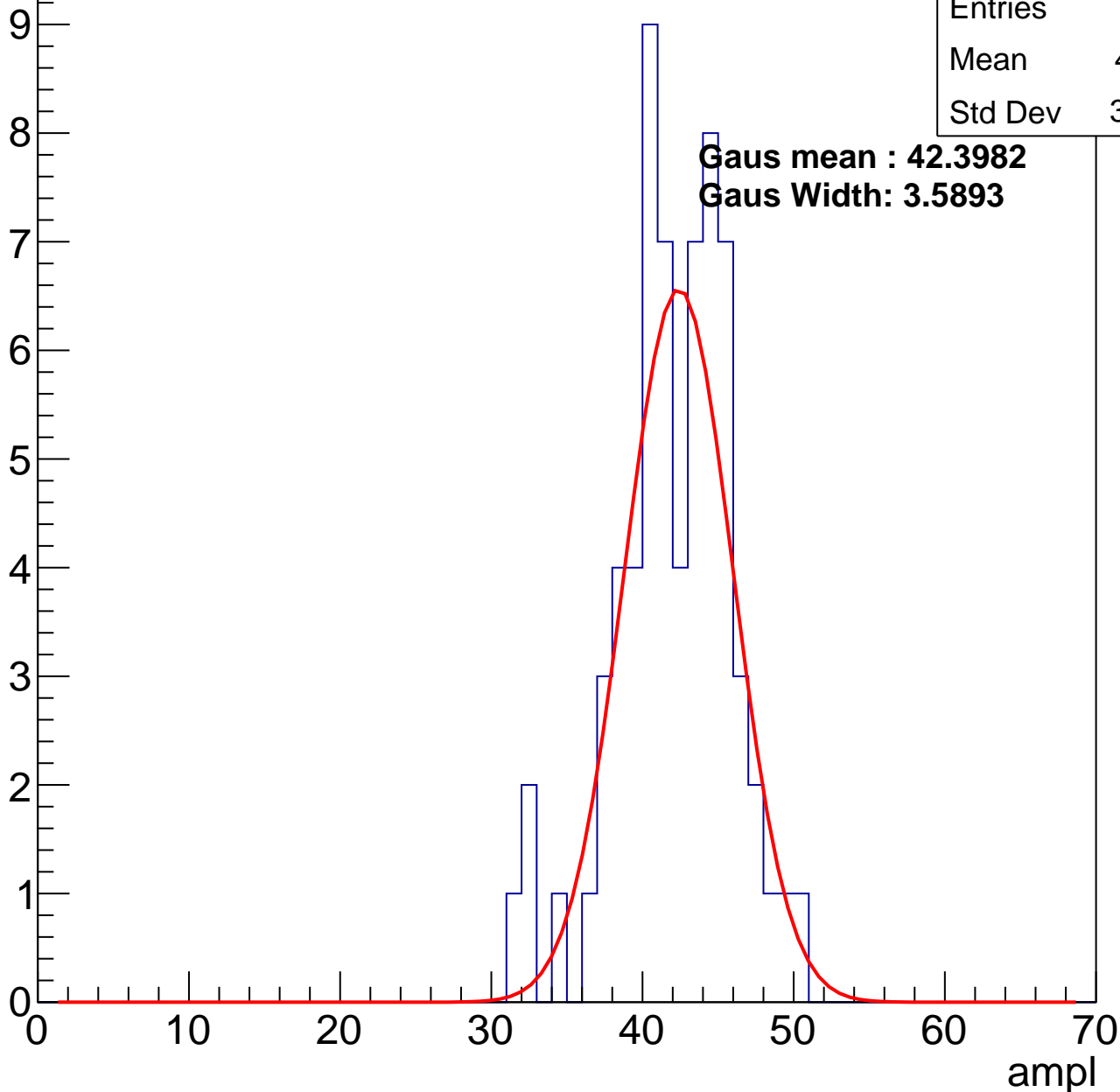
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	41.61
Std Dev	3.849

**Gaus mean : 42.3982**

**Gaus Width: 3.5893**

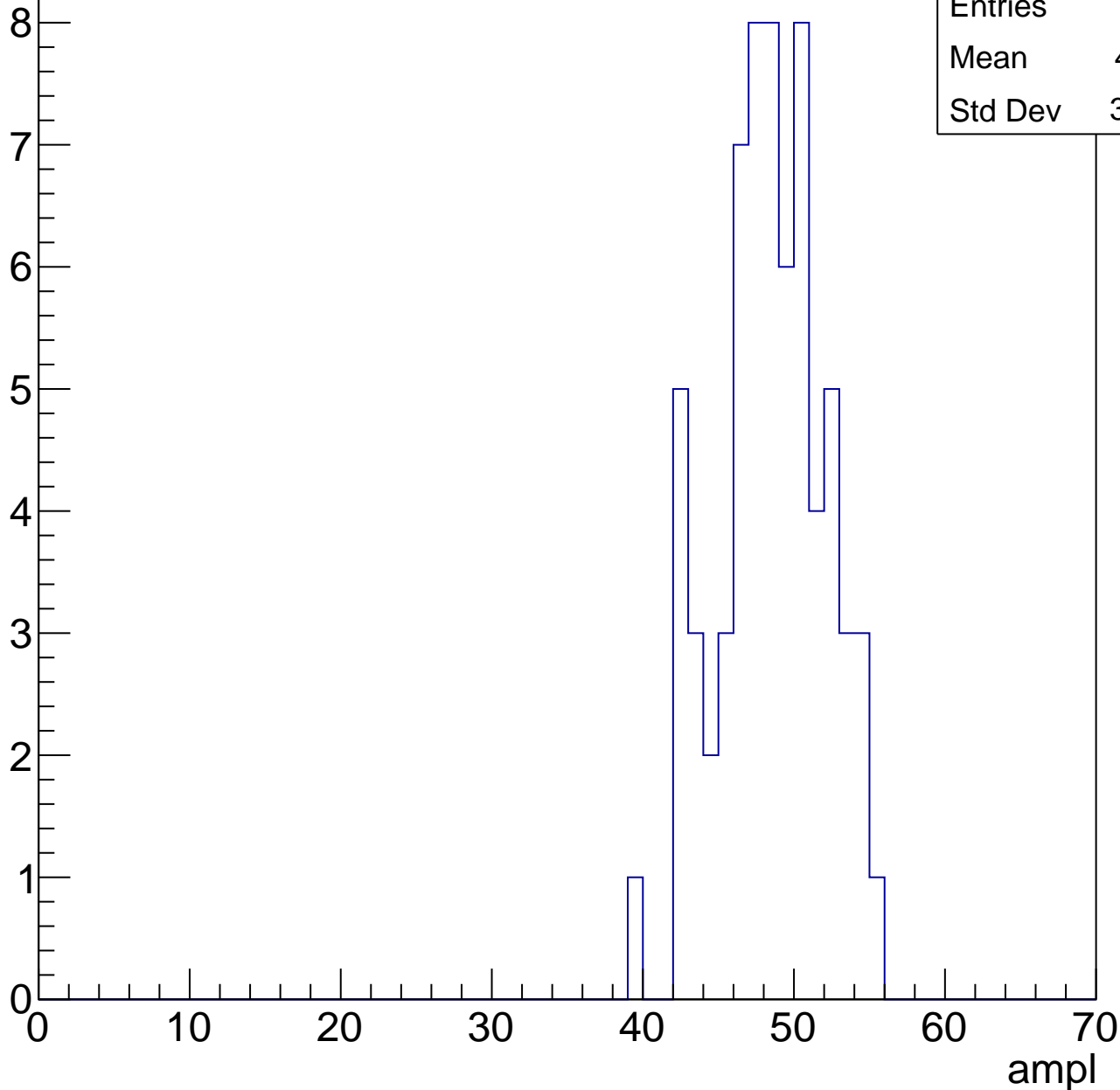


# B1L101S, U18-ch66, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

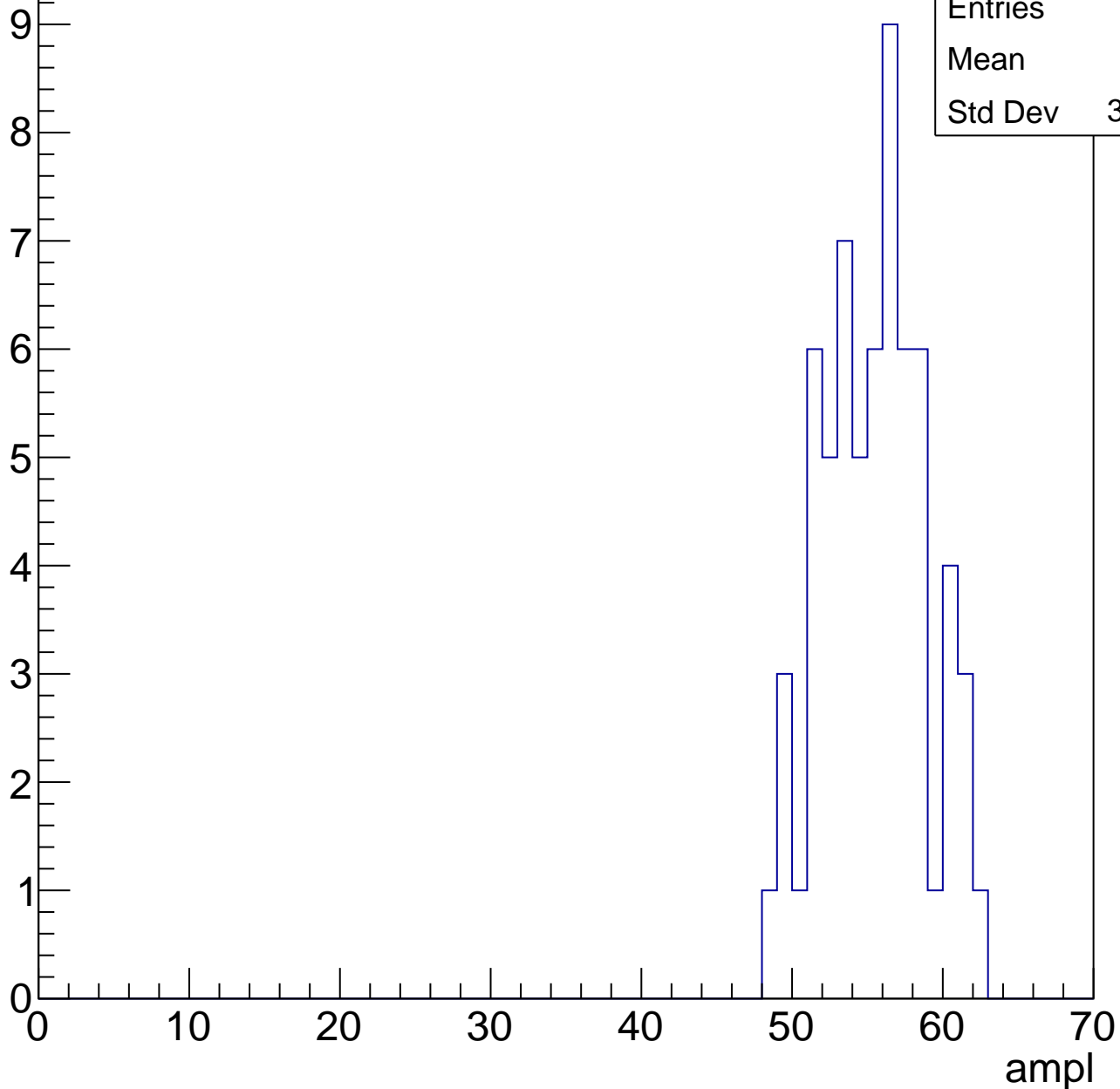
Entries	67
Mean	48.01
Std Dev	3.492



# B1L101S, U18-ch66, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

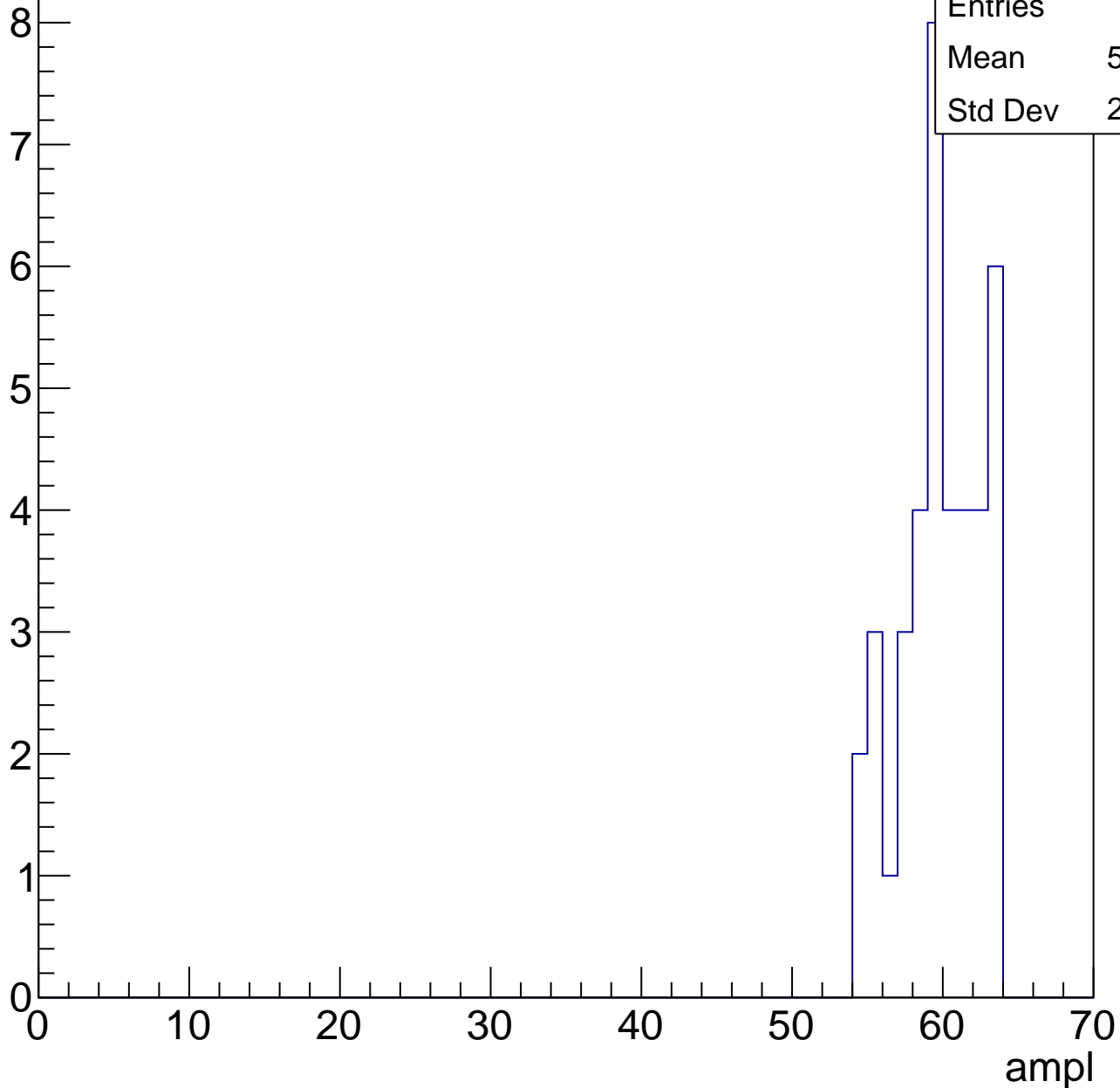
Entry



# B1L101S, U18-ch66, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



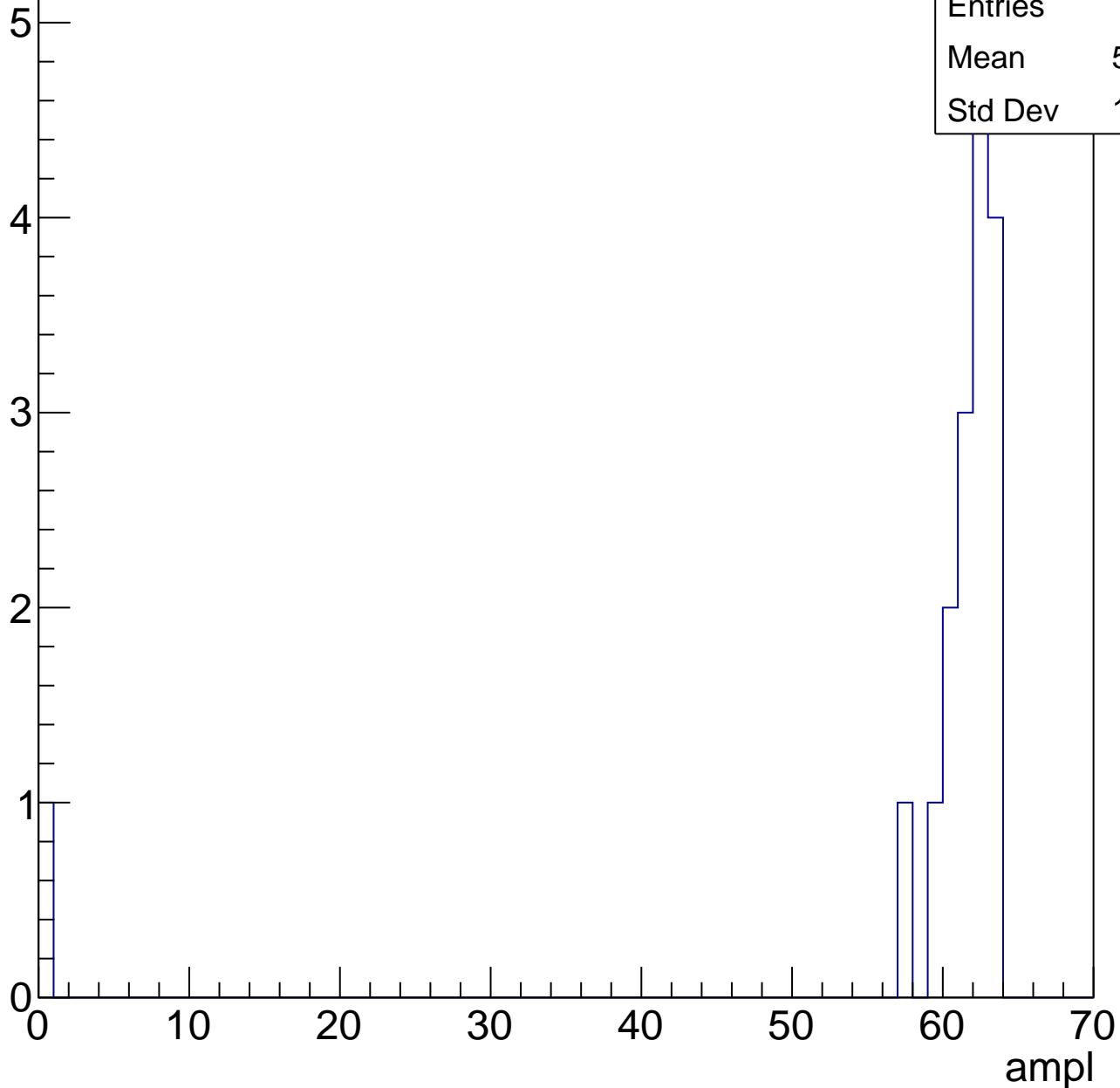
Entries	39
Mean	59.33
Std Dev	2.634

# B1L101S, U18-ch66, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	17
Mean	57.71
Std Dev	14.51





# B1L101S, U18-ch66, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch67, adc0

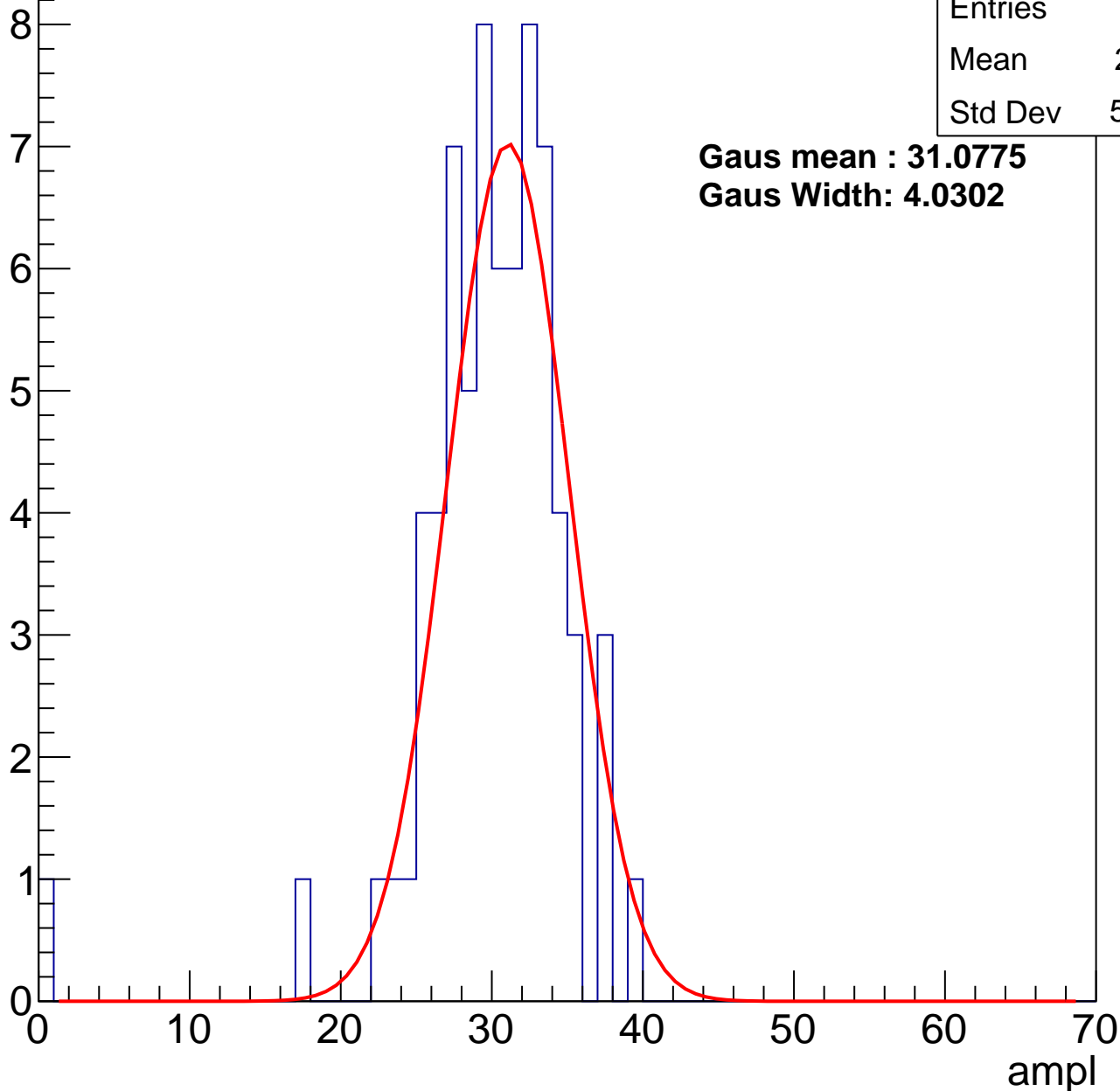
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	29.51
Std Dev	5.205

**Gaus mean : 31.0775**

**Gaus Width: 4.0302**



# B1L101S, U18-ch67, adc1

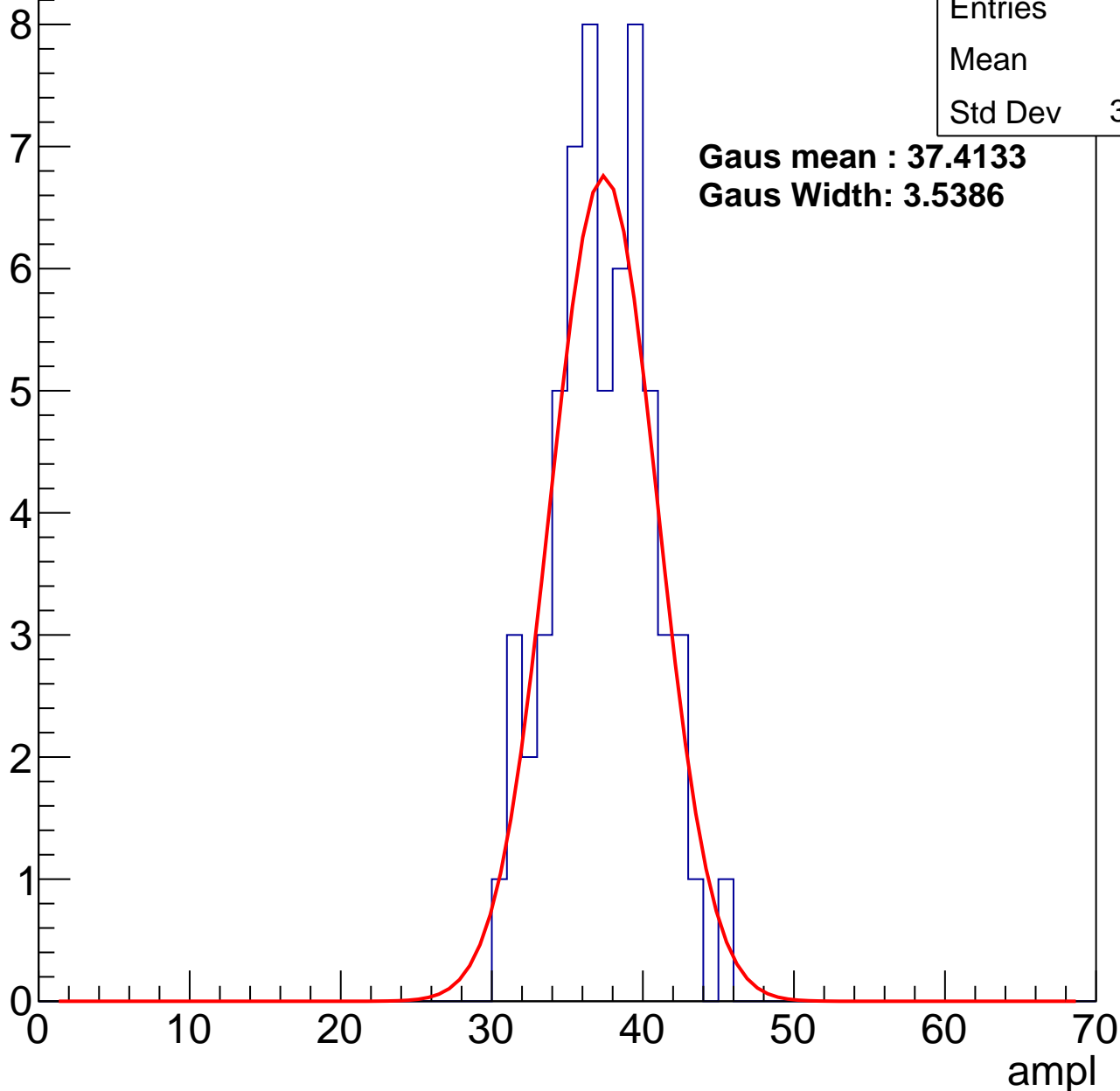
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	36.9
Std Dev	3.243

**Gaus mean : 37.4133**

**Gaus Width: 3.5386**



# B1L101S, U18-ch67, adc2

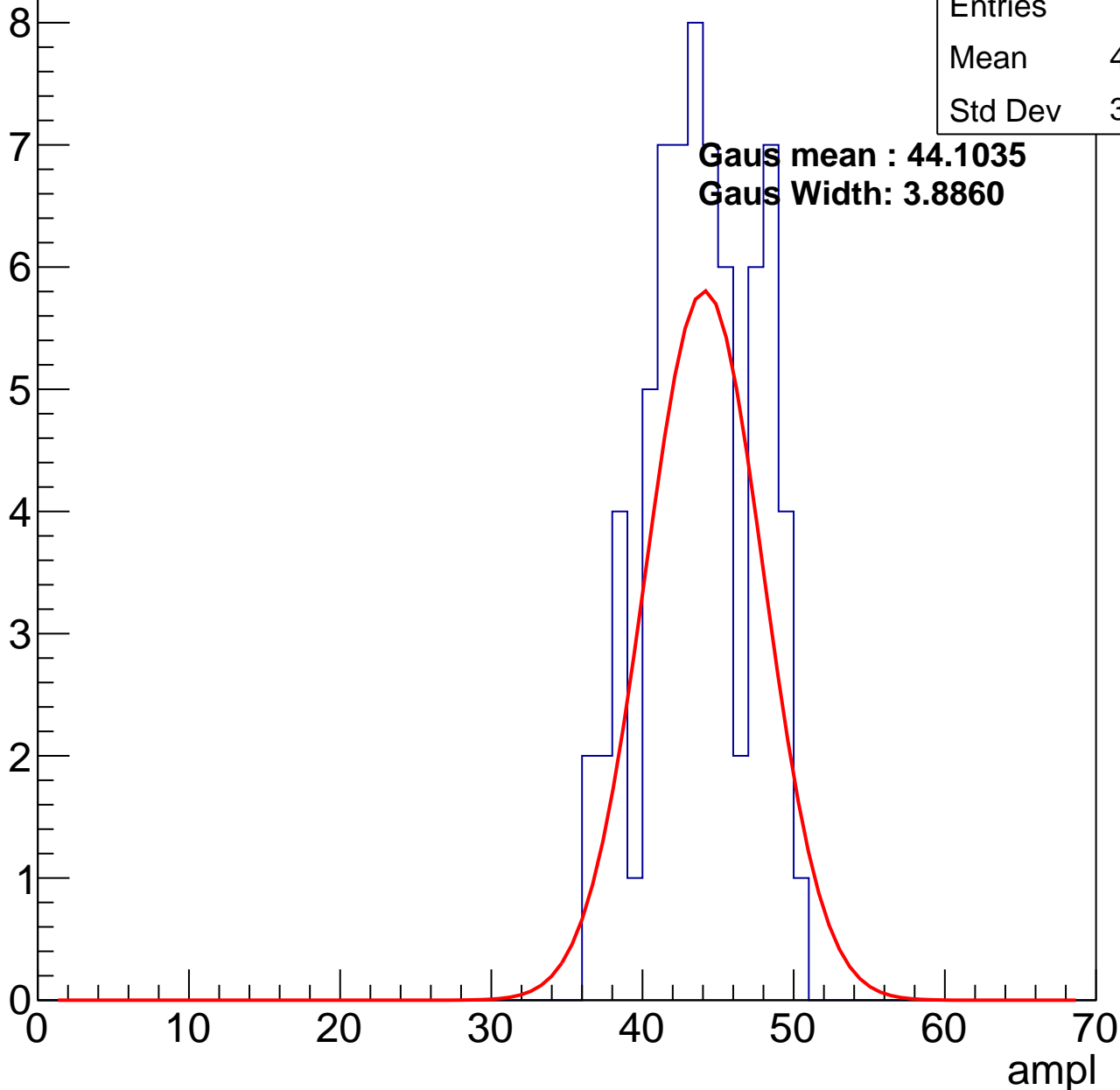
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	43.42
Std Dev	3.544

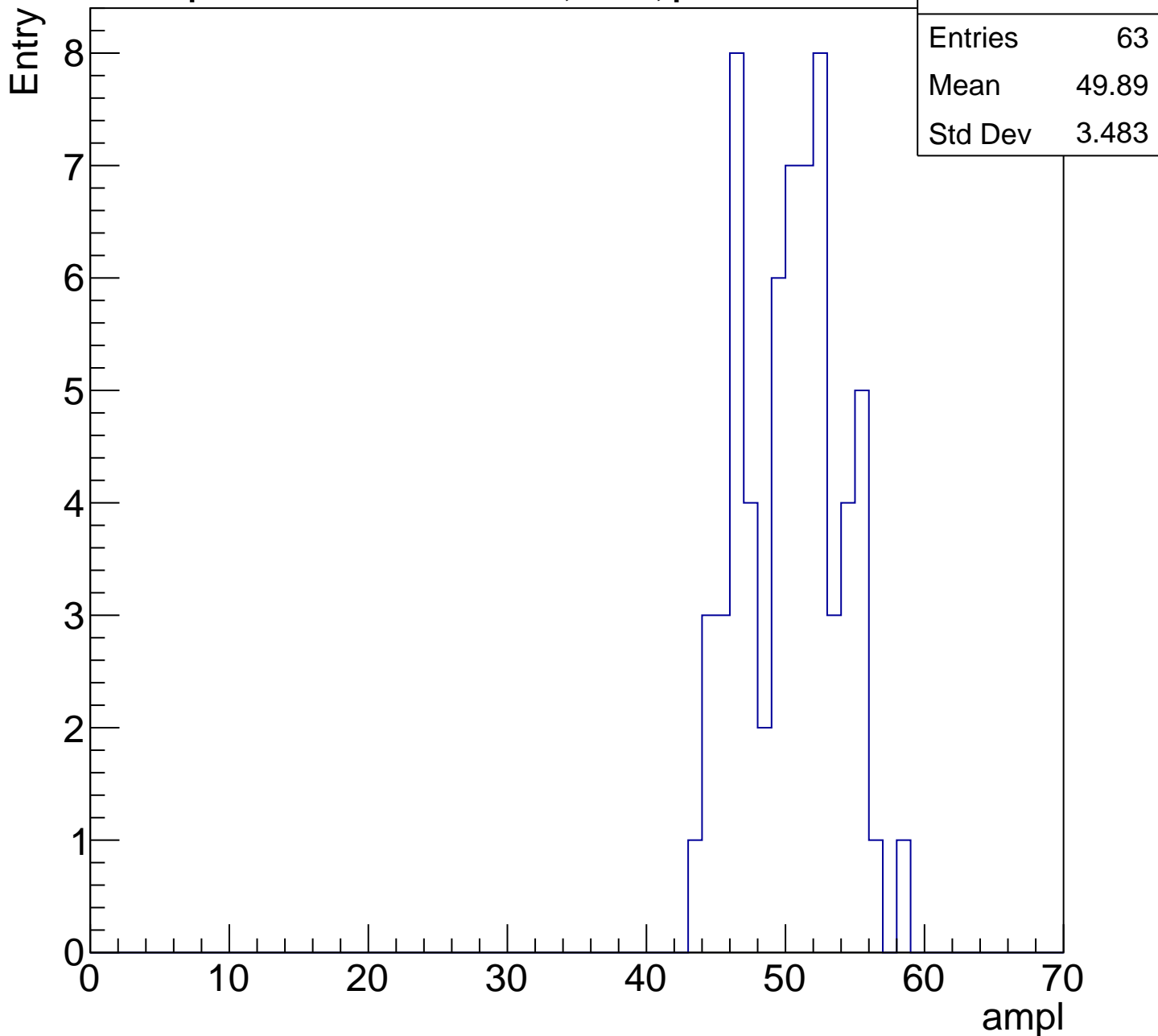
**Gaus mean : 44.1035**

**Gaus Width: 3.8860**



# B1L101S, U18-ch67, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

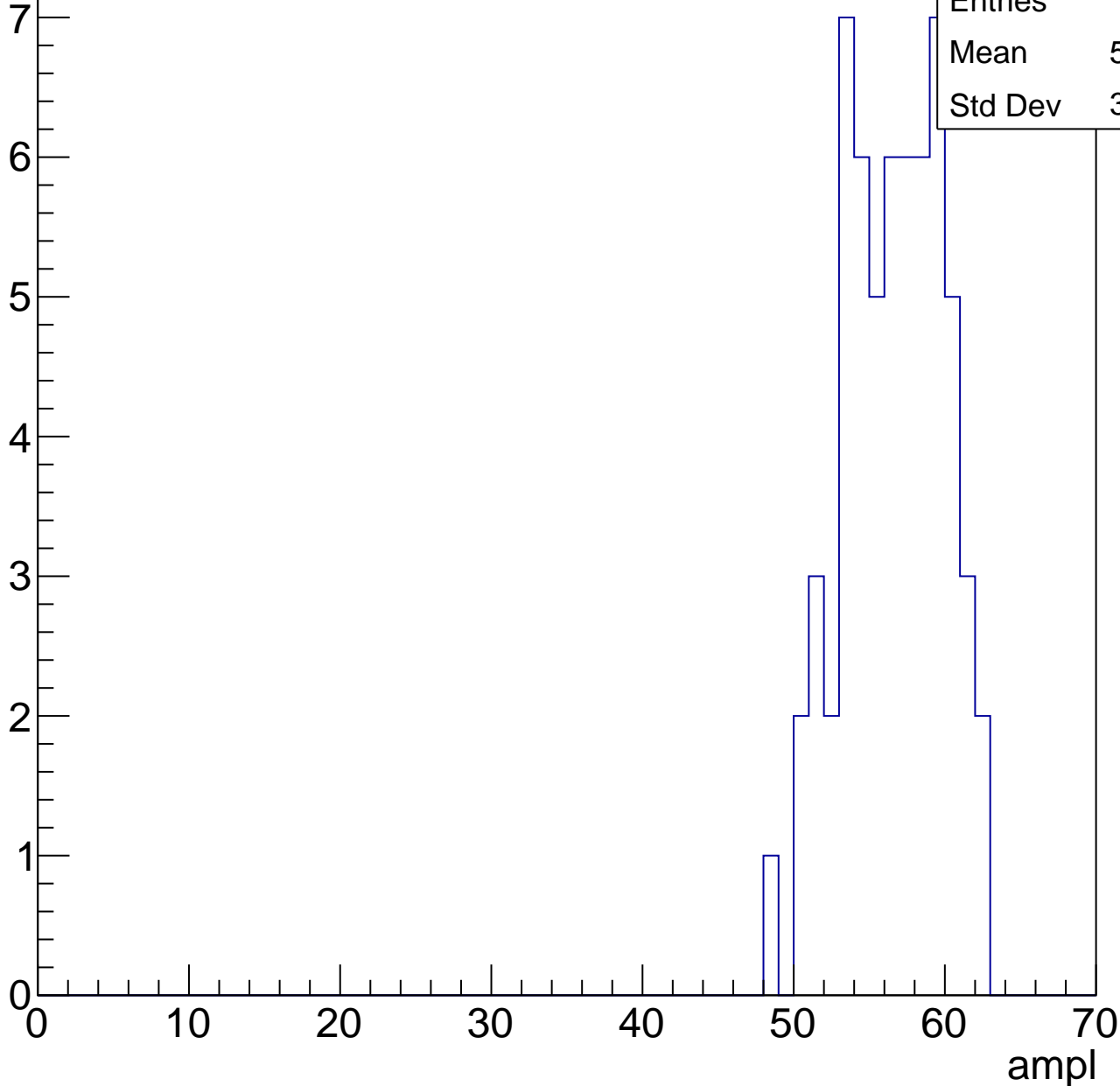


# B1L101S, U18-ch67, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

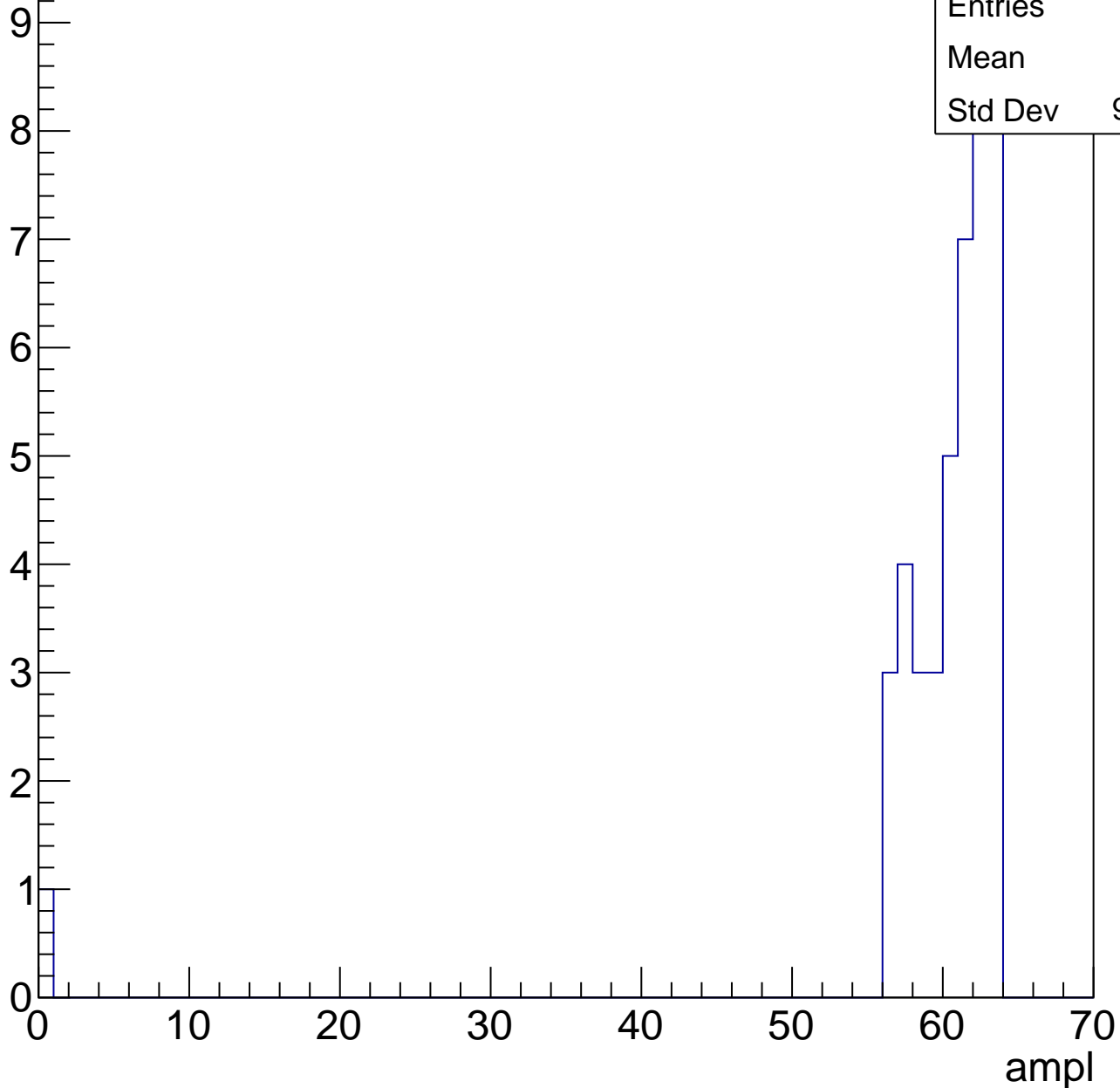
Entries	61
Mean	56.08
Std Dev	3.276



# B1L101S, U18-ch67, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch67, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch67, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch68, adc0

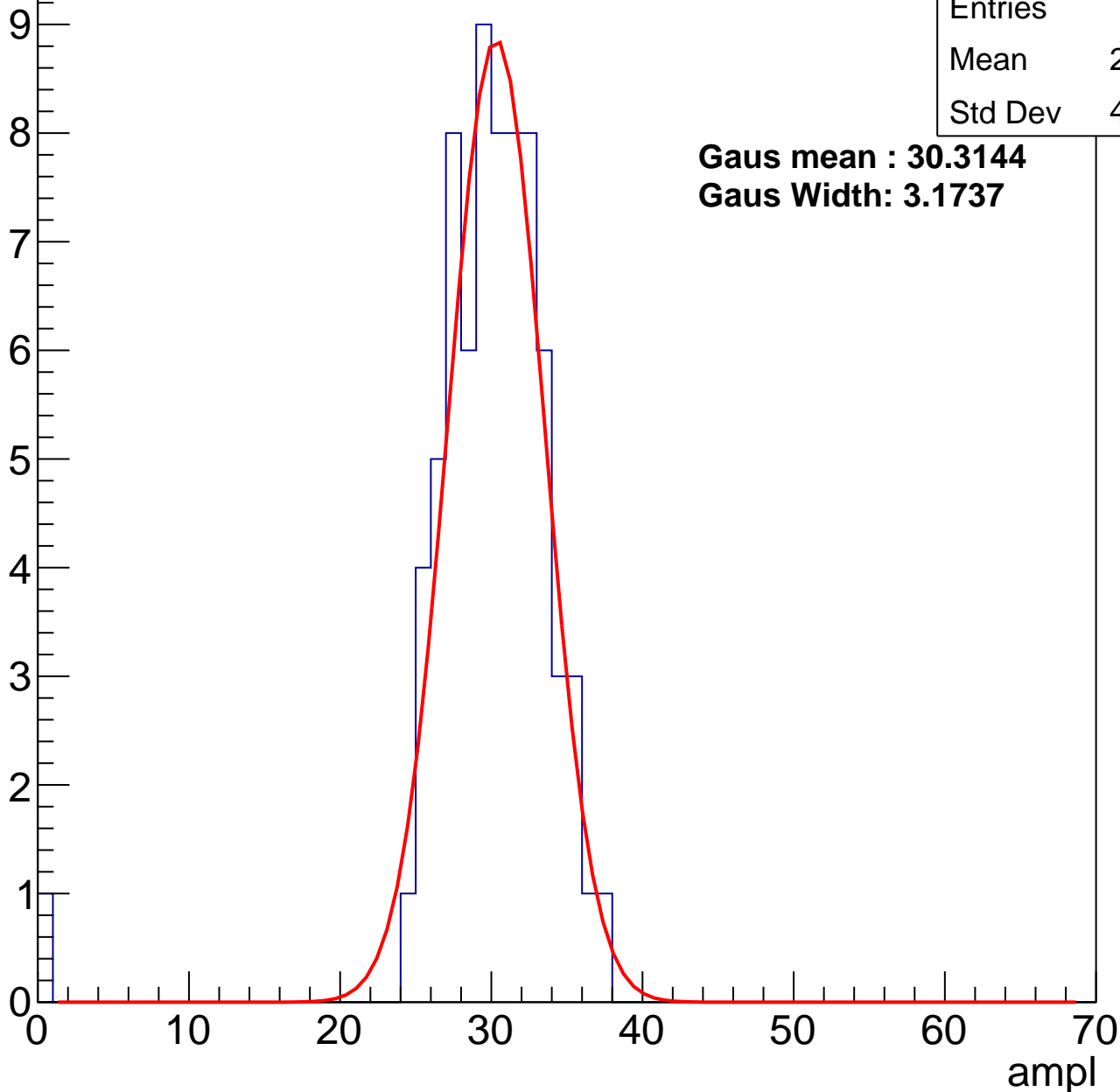
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	29.46
Std Dev	4.567

**Gaus mean : 30.3144**

**Gaus Width: 3.1737**



# B1L101S, U18-ch68, adc1

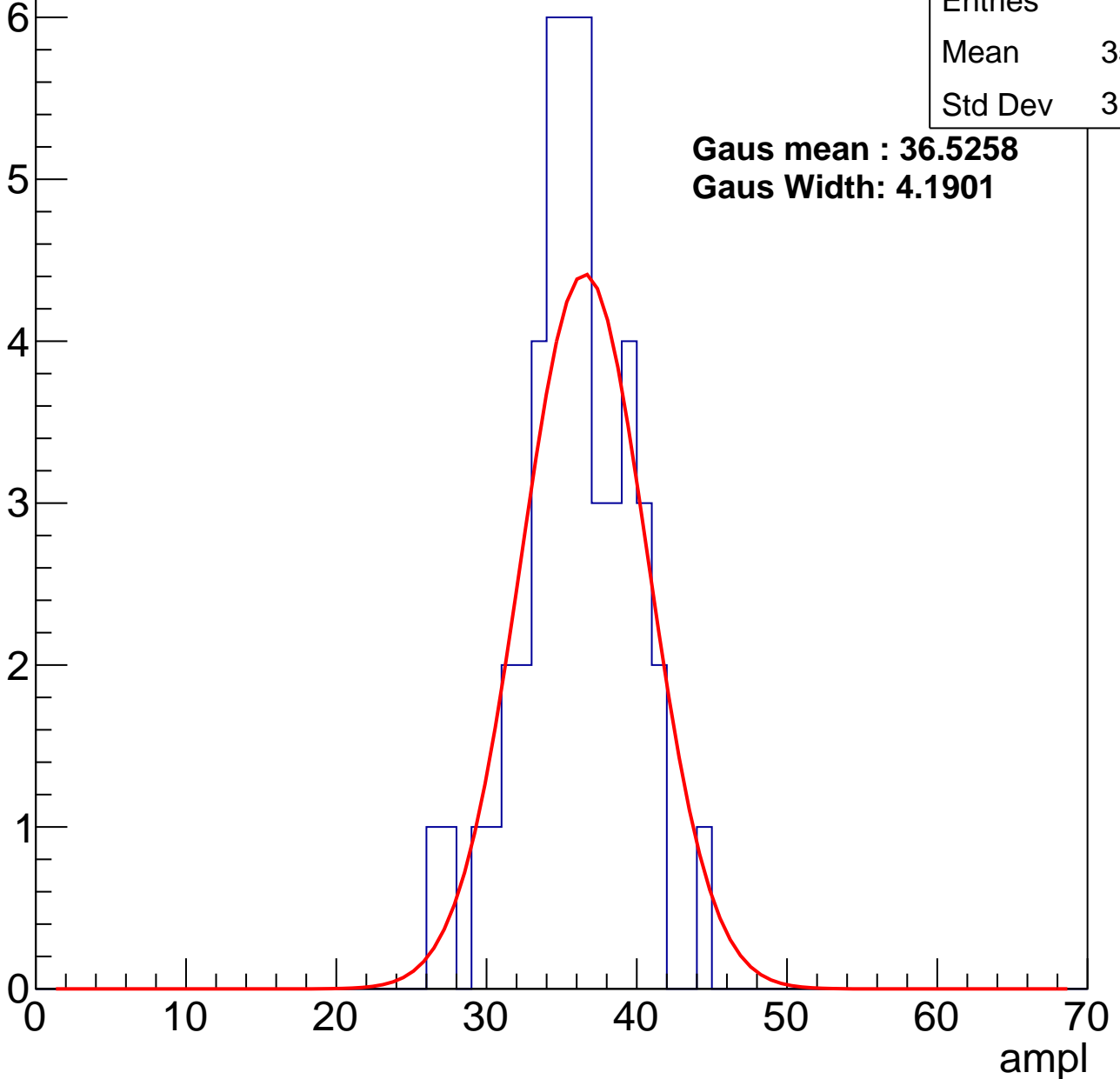
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	46
Mean	35.37
Std Dev	3.638

**Gaus mean : 36.5258**

**Gaus Width: 4.1901**



# B1L101S, U18-ch68, adc2

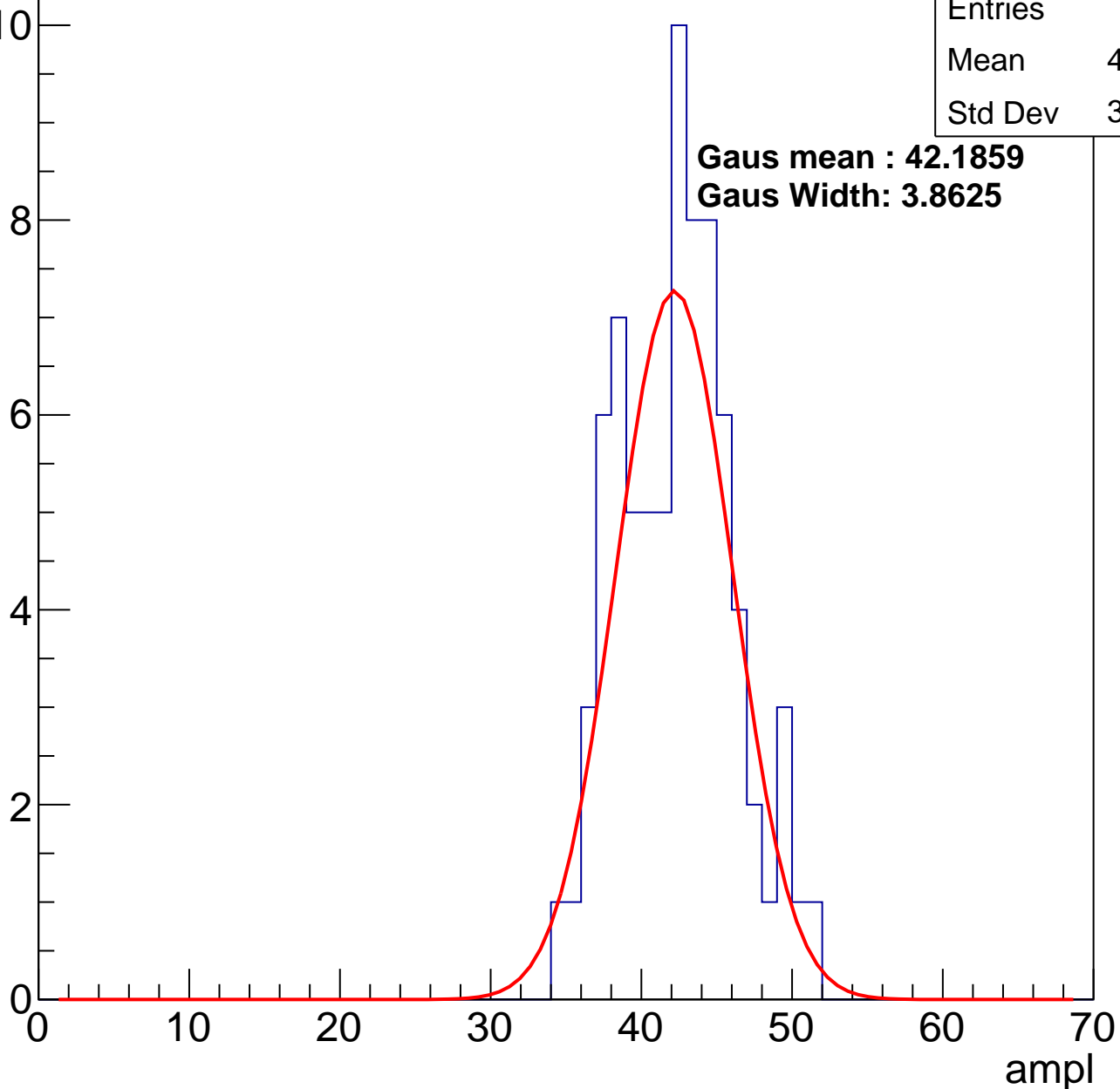
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	41.88
Std Dev	3.759

**Gaus mean : 42.1859**

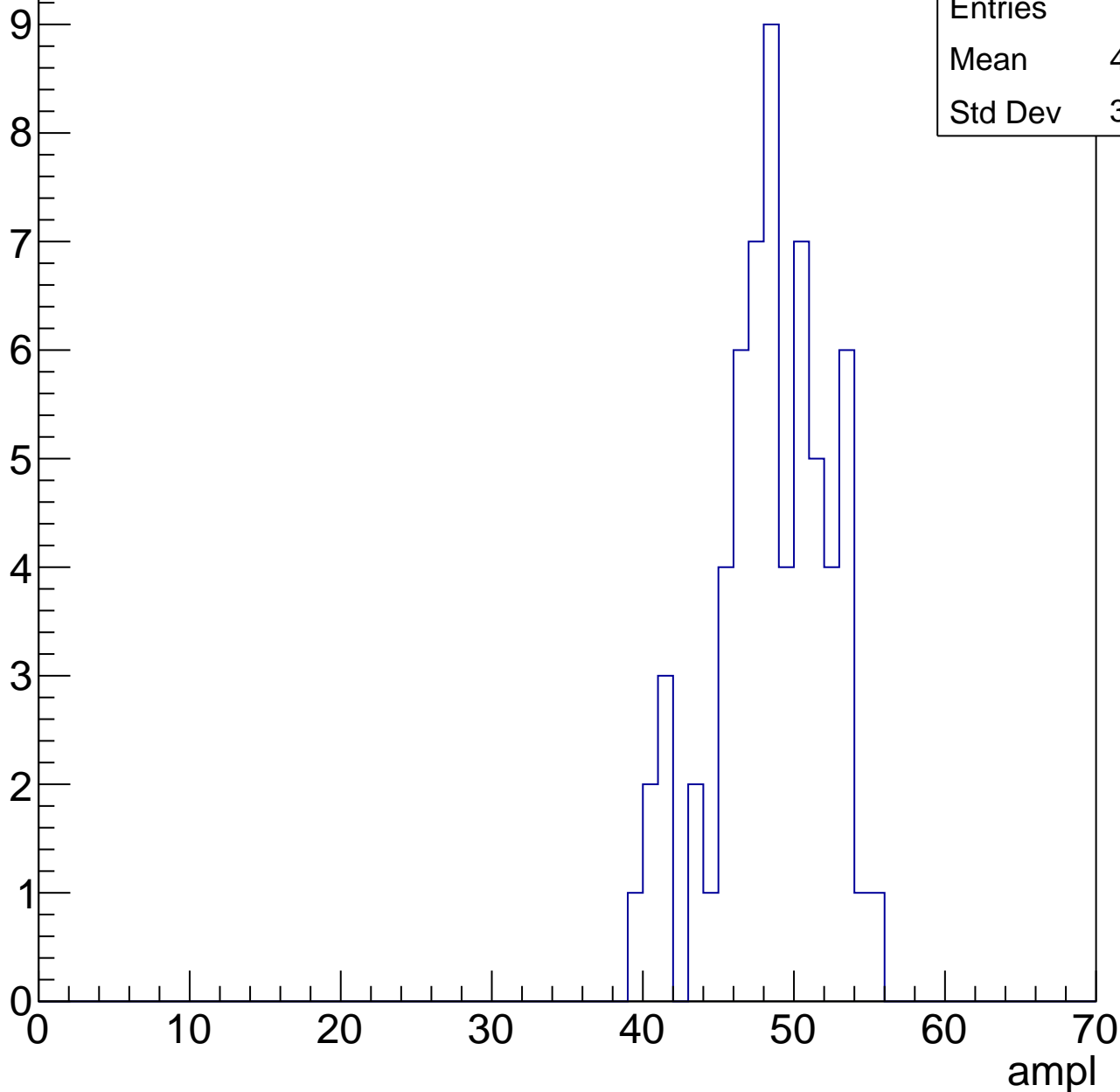
**Gaus Width: 3.8625**



# B1L101S, U18-ch68, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

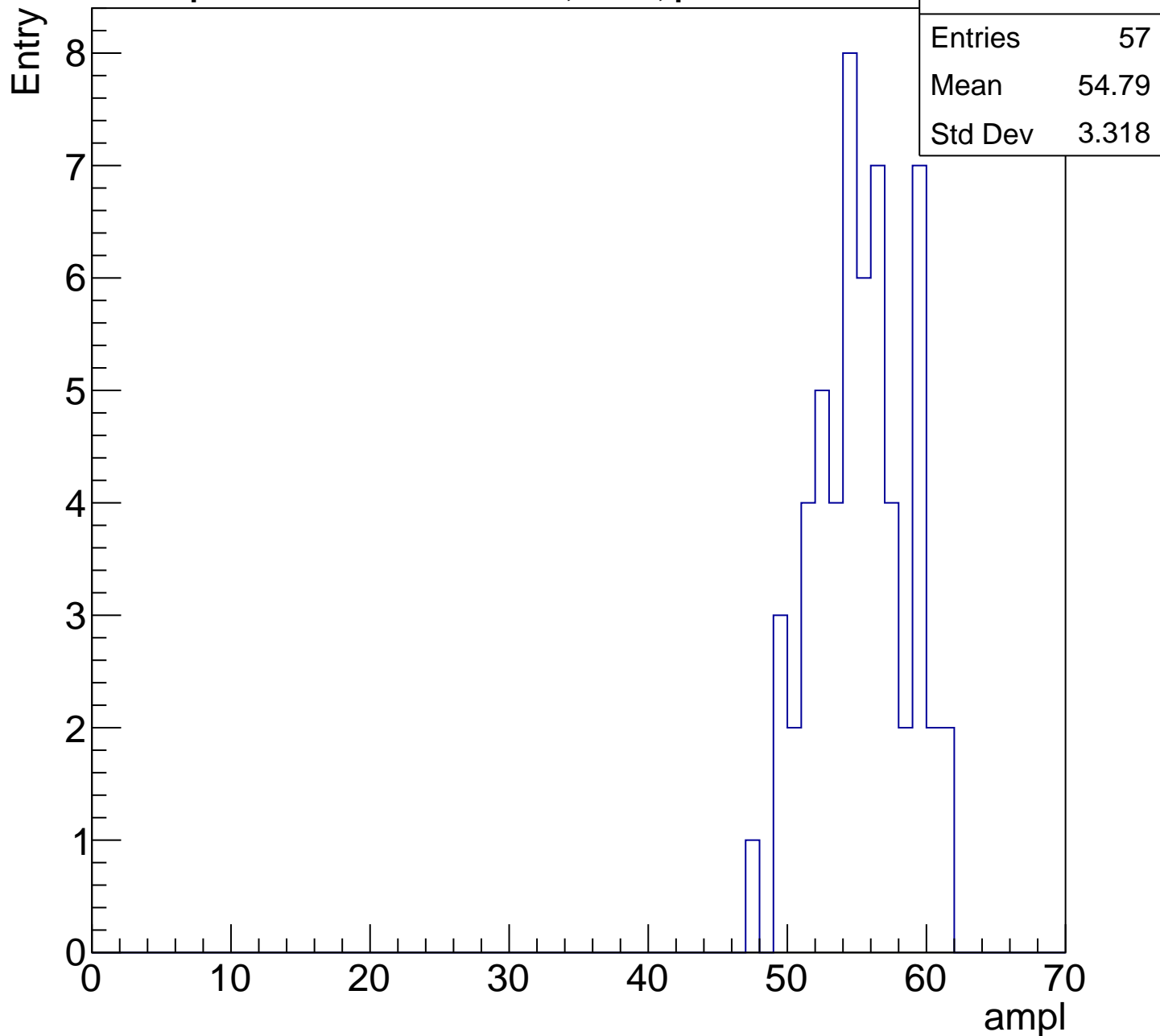
Entry



Entries	63
Mean	48.02
Std Dev	3.705

# B1L101S, U18-ch68, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

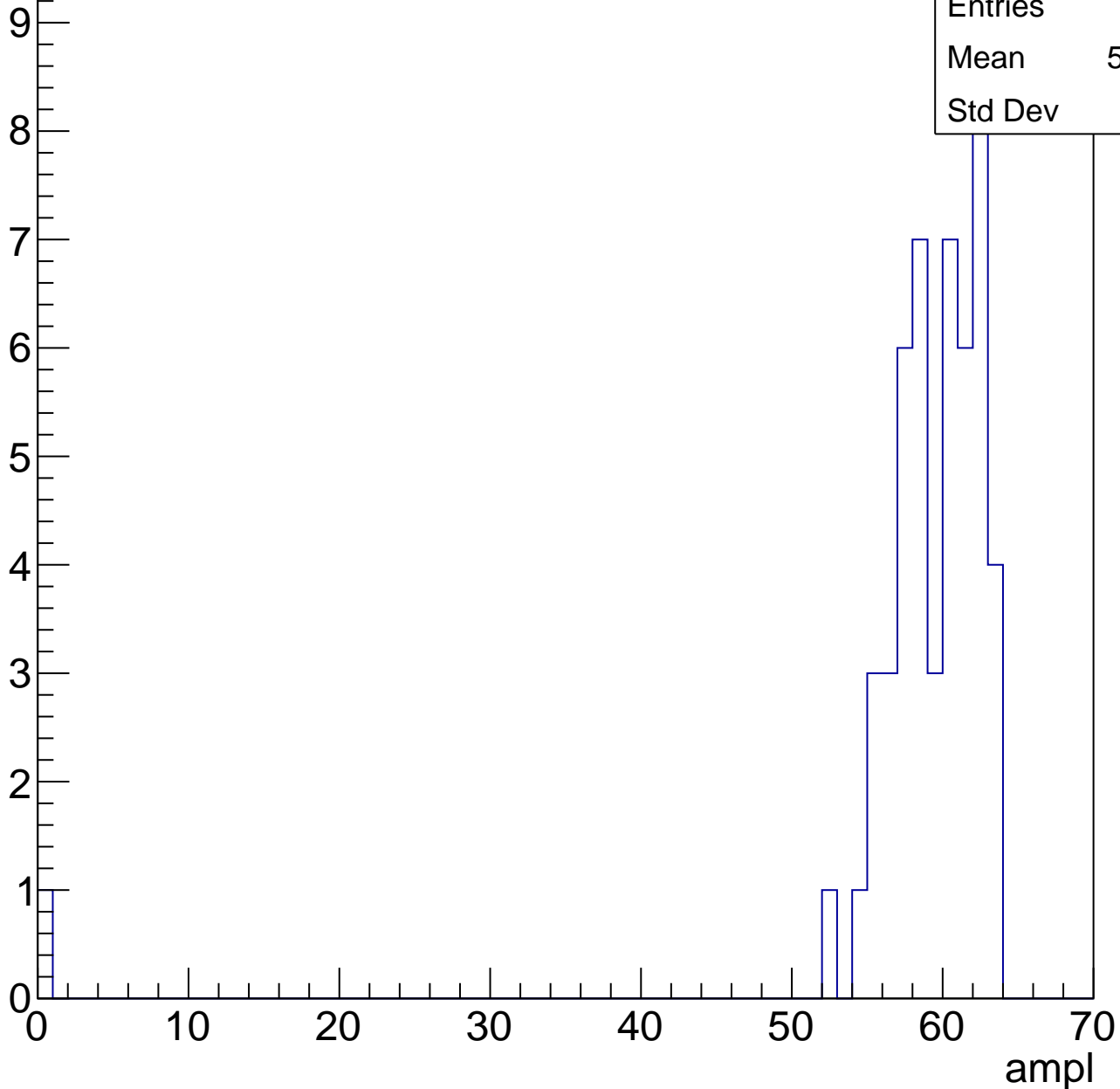


# B1L101S, U18-ch68, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	58.04
Std Dev	8.62

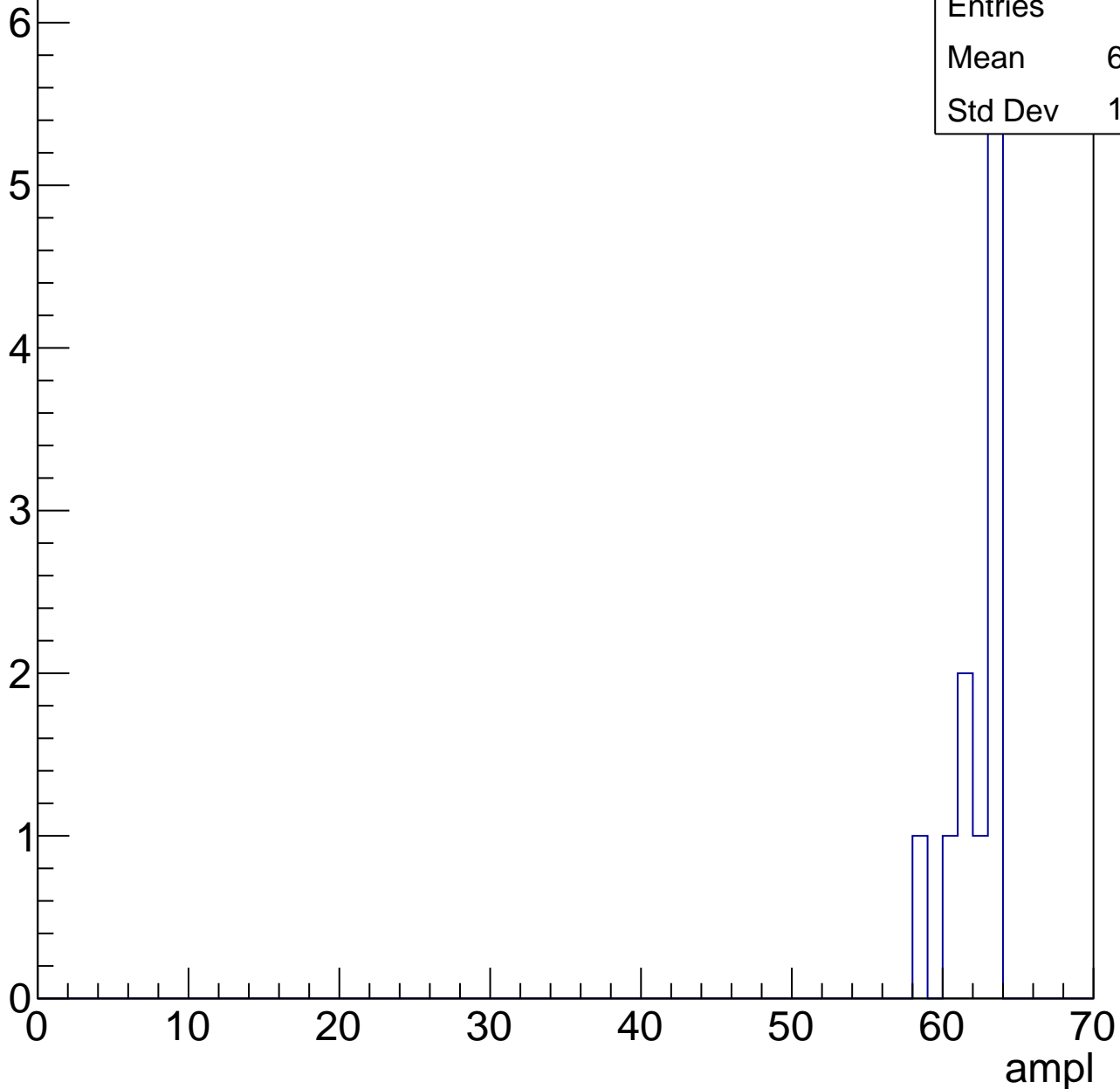


# B1L101S, U18-ch68, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	11
Mean	61.82
Std Dev	1.585

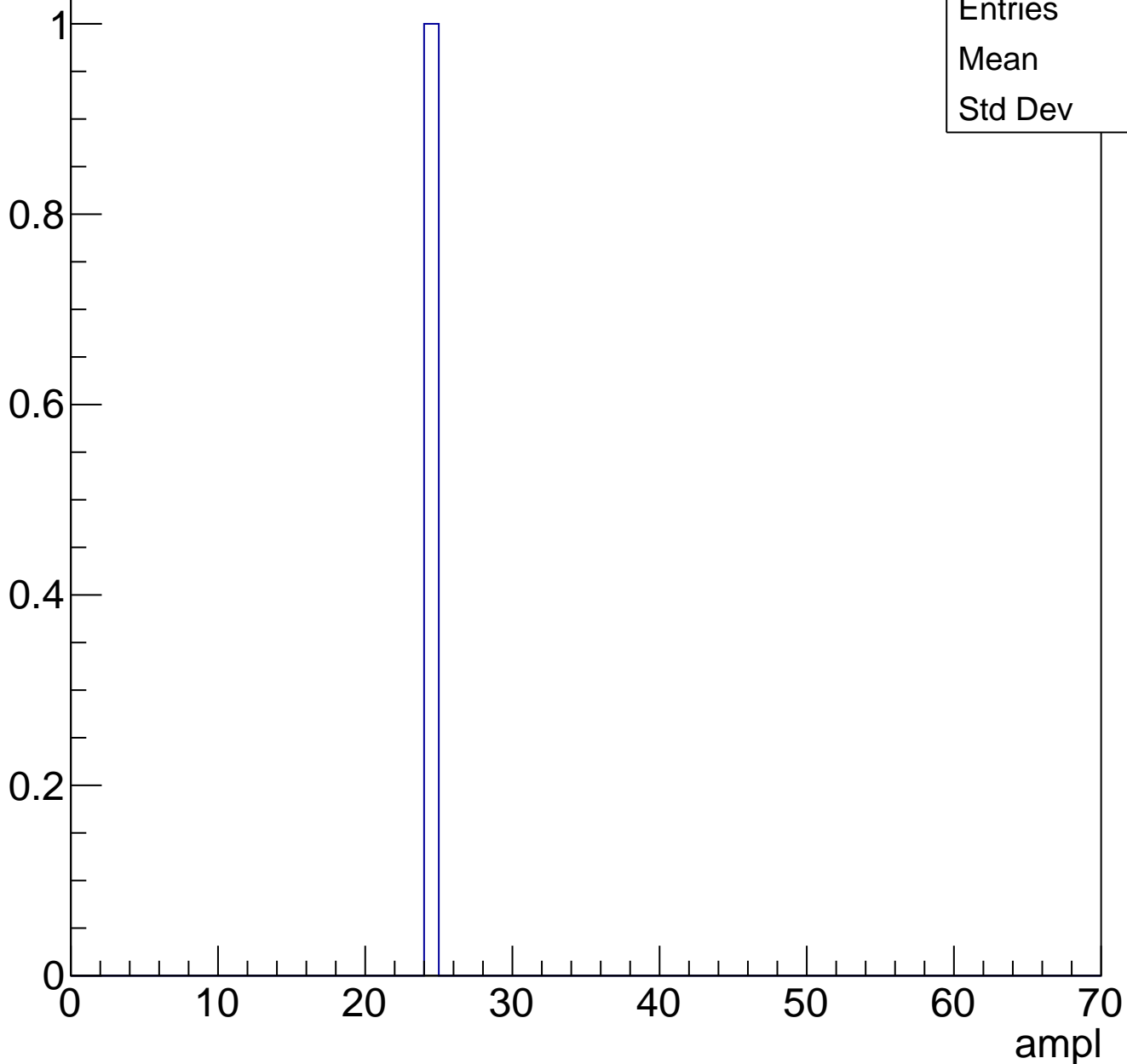




# B1L101S, U18-ch68, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch69, adc0

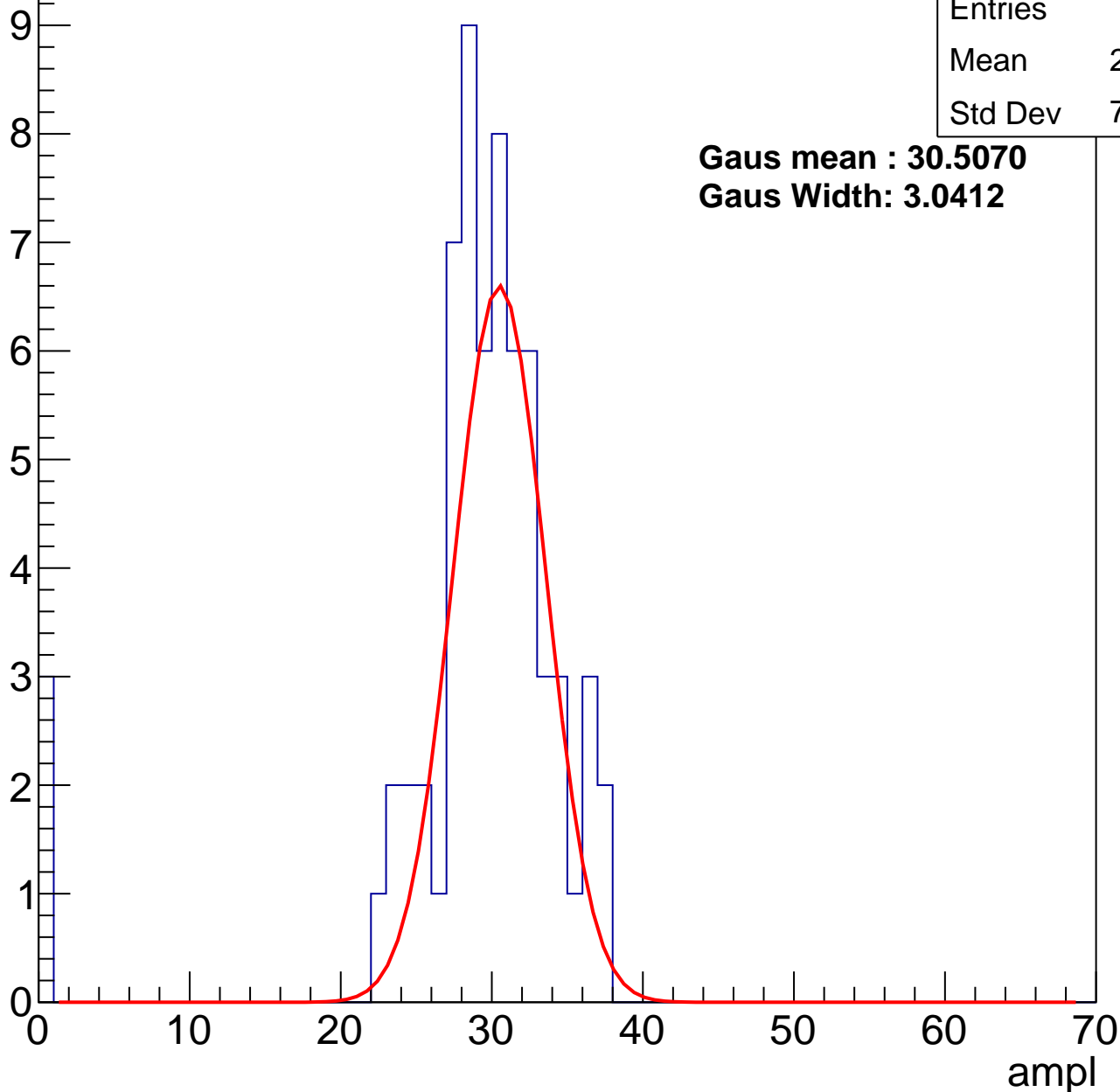
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	28.35
Std Dev	7.087

**Gaus mean : 30.5070**

**Gaus Width: 3.0412**



# B1L101S, U18-ch69, adc1

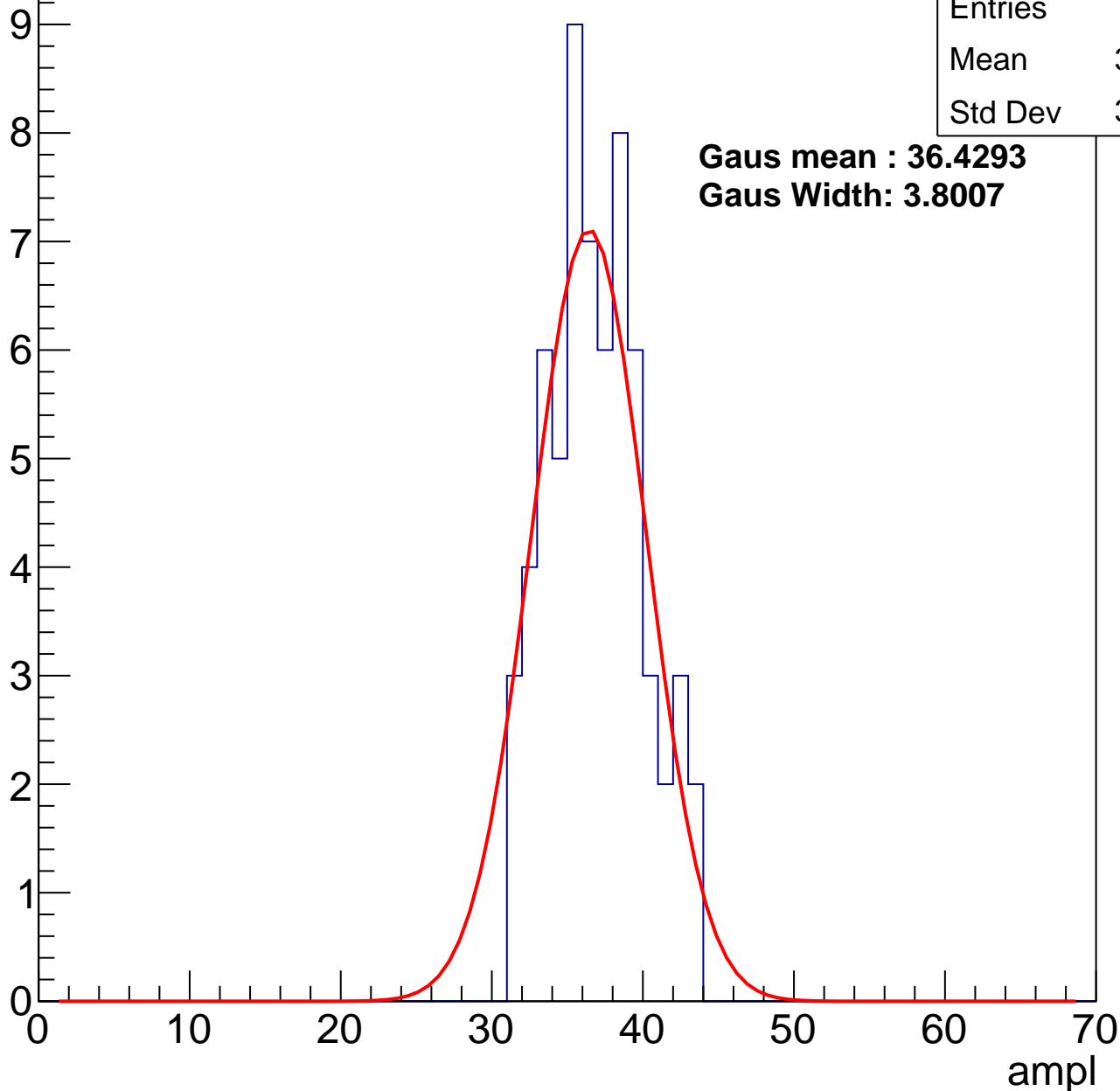
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	36.41
Std Dev	3.081

**Gaus mean : 36.4293**

**Gaus Width: 3.8007**



# B1L101S, U18-ch69, adc2

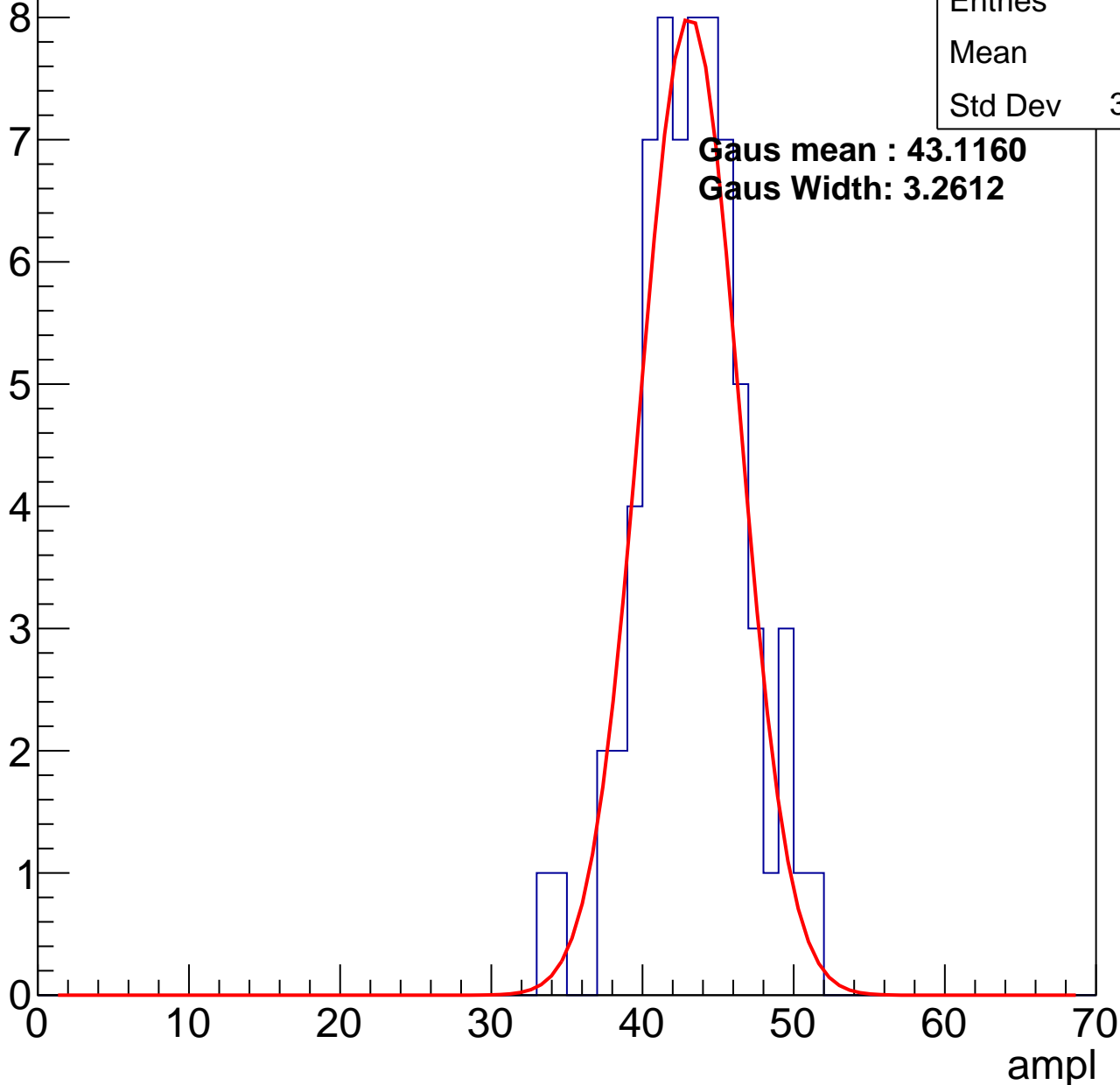
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	42.8
Std Dev	3.492

**Gaus mean : 43.1160**

**Gaus Width: 3.2612**

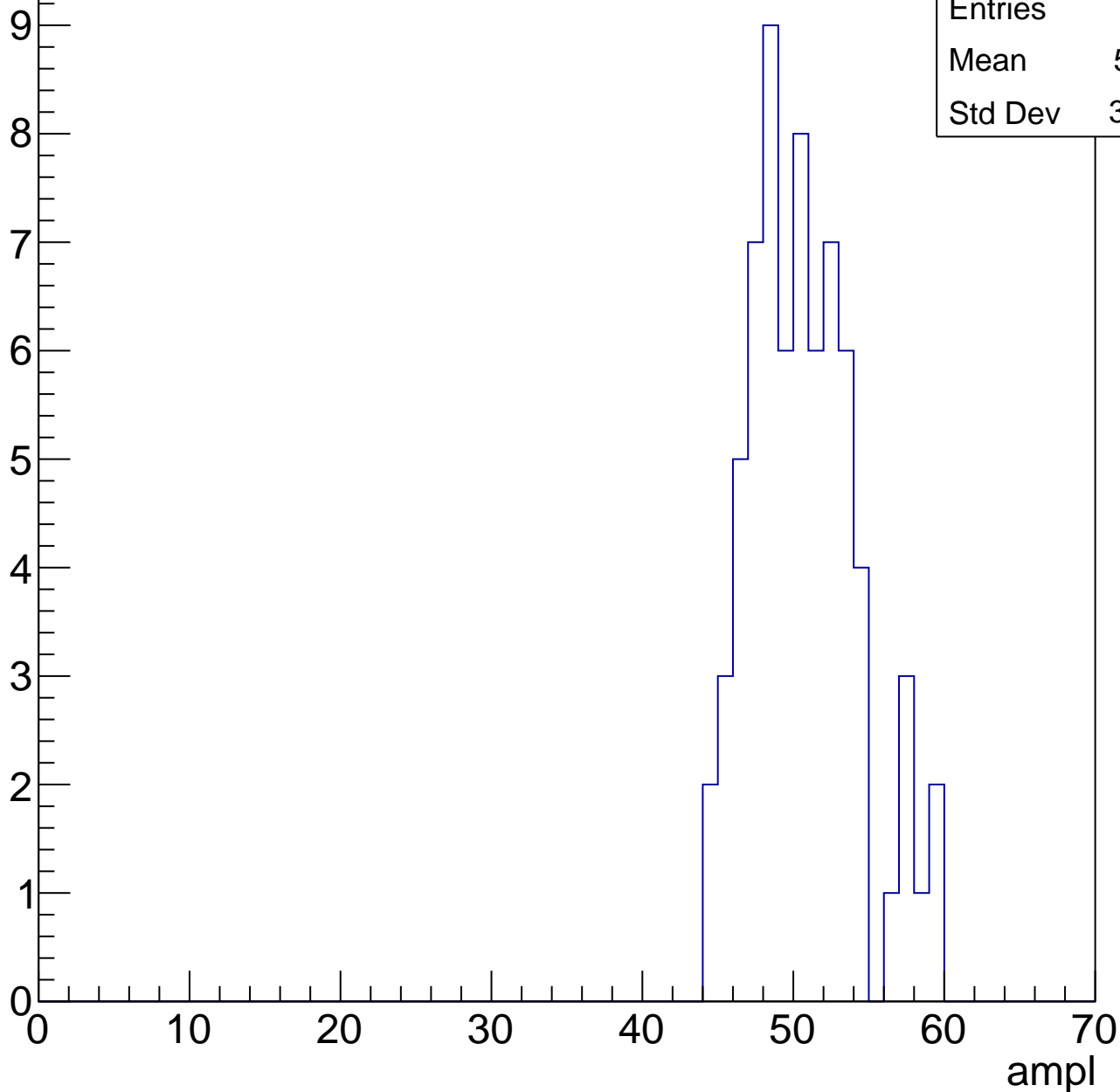


# B1L101S, U18-ch69, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	50.21
Std Dev	3.565



# B1L101S, U18-ch69, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	53
Mean	55.89
Std Dev	3.357

Entry

10

8

6

4

2

0

0

10

20

30

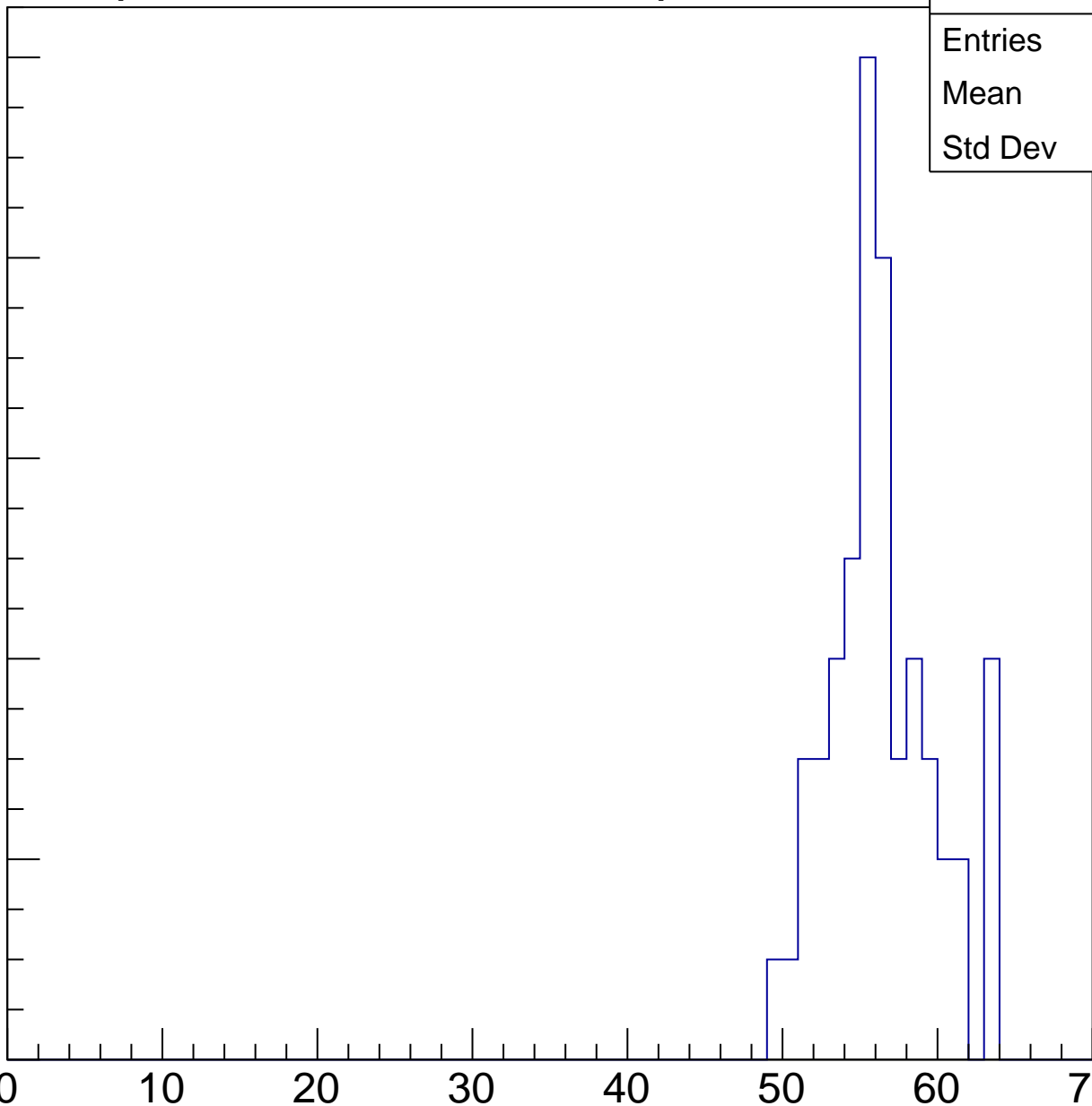
40

50

60

70

ampl

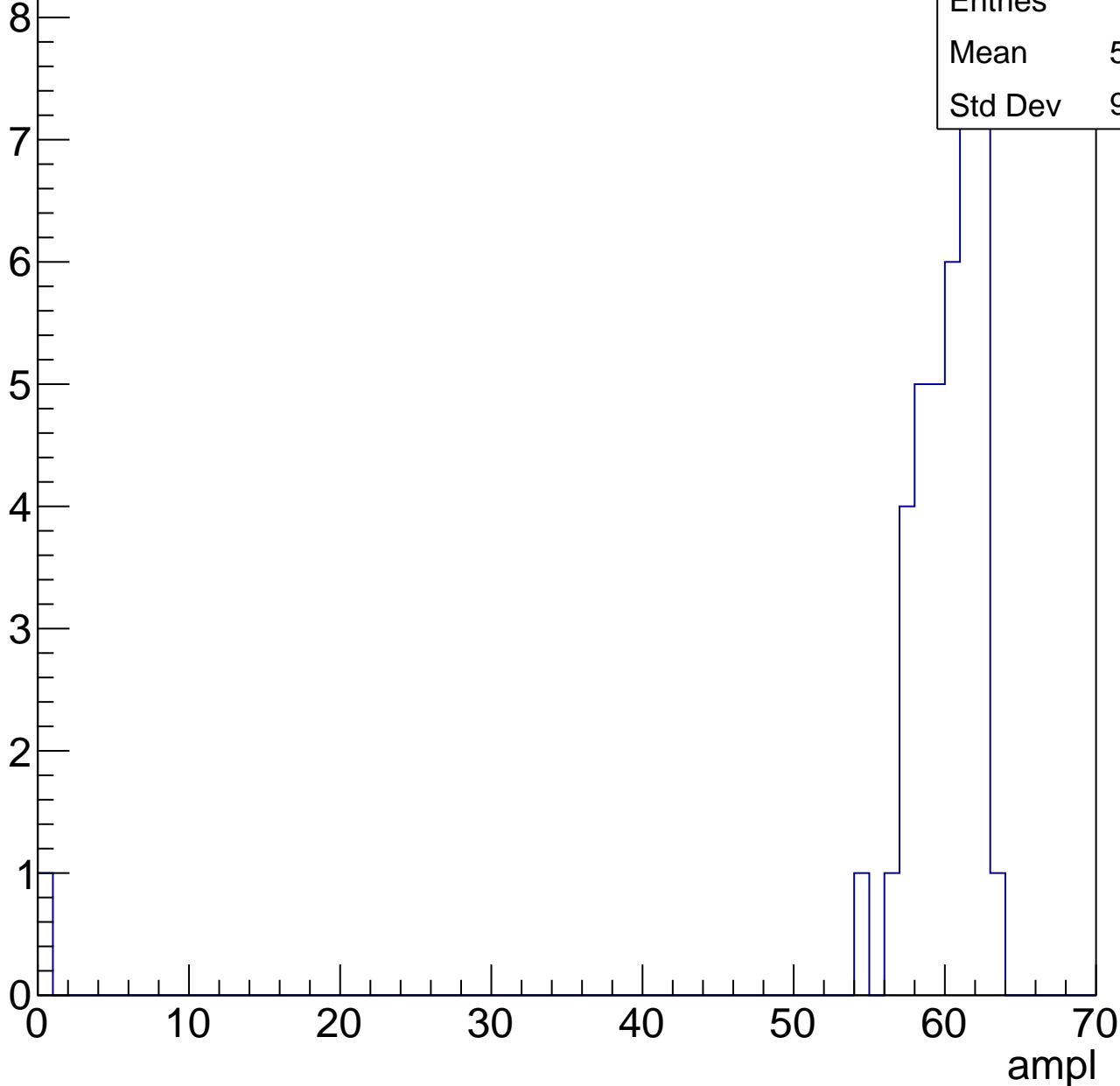


# B1L101S, U18-ch69, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	40
Mean	58.25
Std Dev	9.539

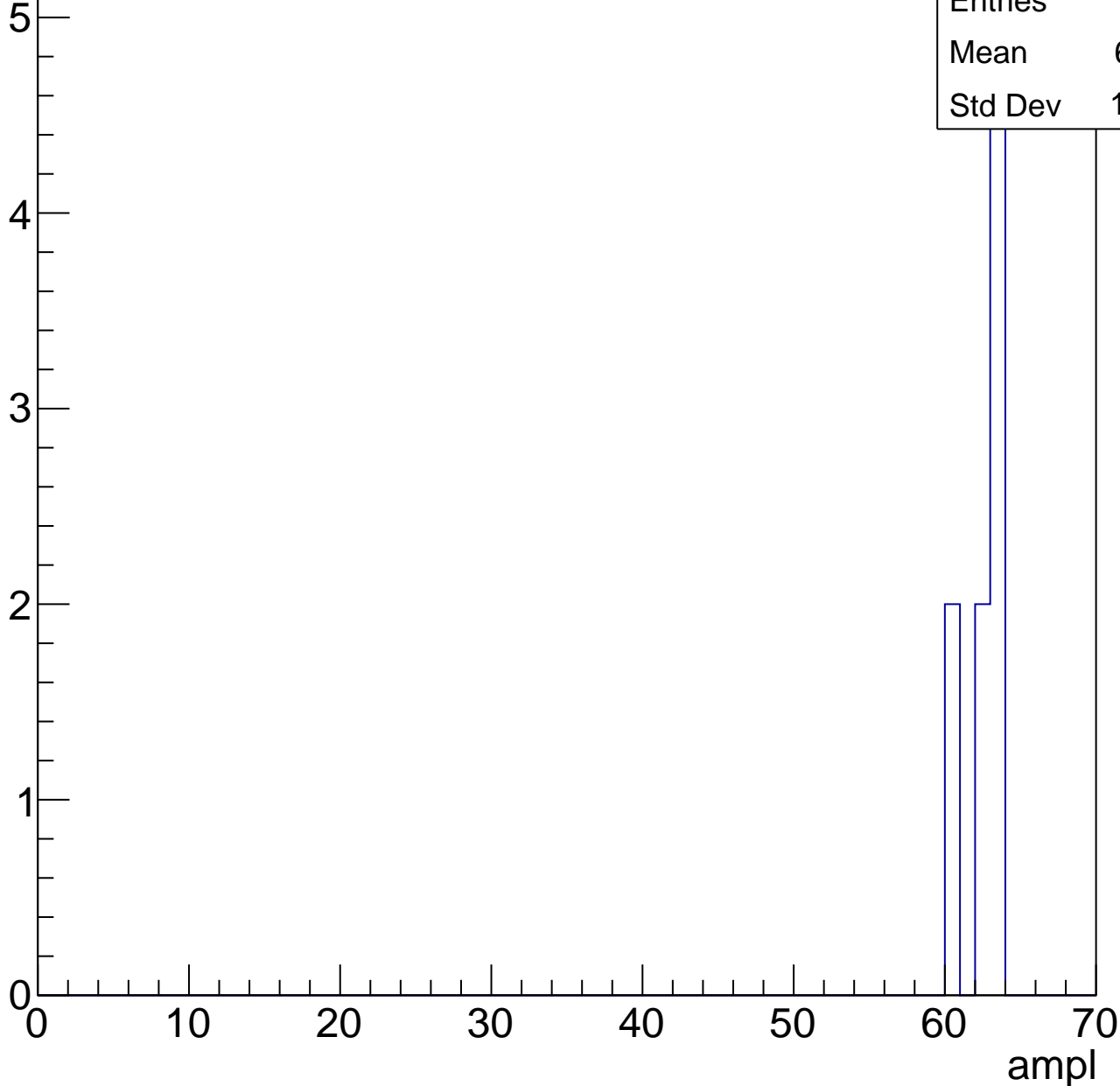


# B1L101S, U18-ch69, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	9
Mean	62.11
Std Dev	1.197

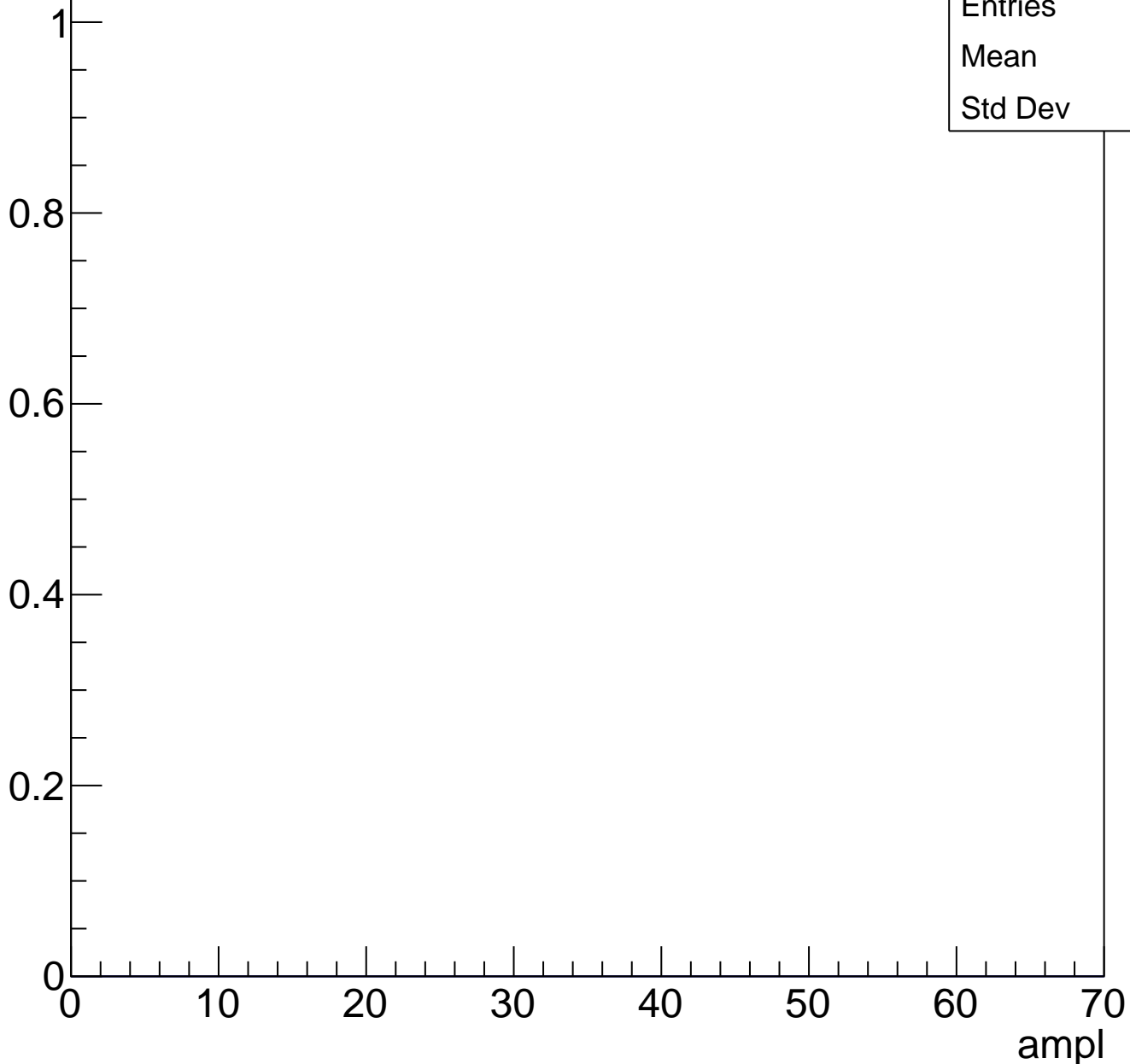




# B1L101S, U18-ch69, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U18-ch70, adc0

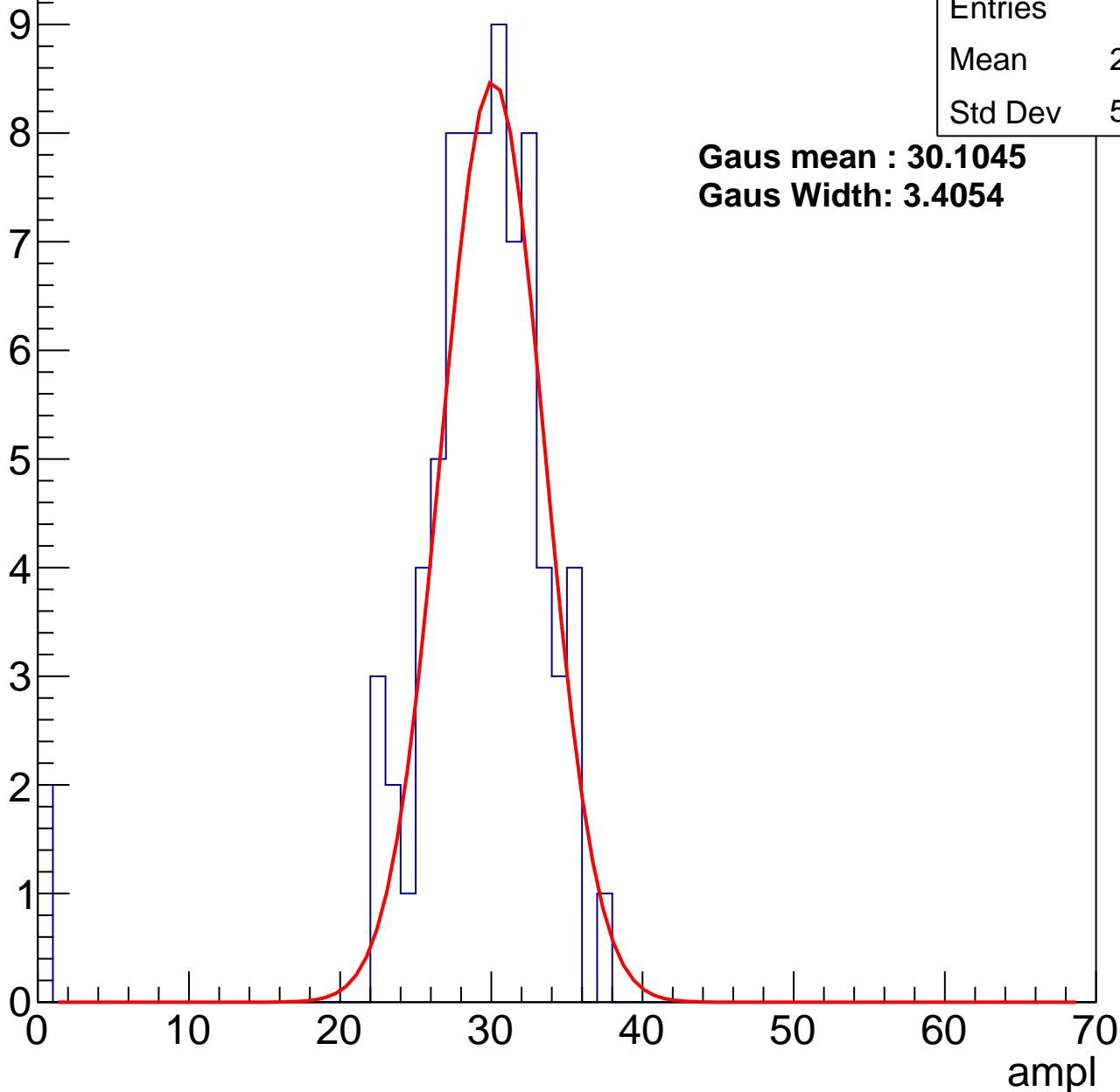
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	28.47
Std Dev	5.708

**Gaus mean : 30.1045**

**Gaus Width: 3.4054**



# B1L101S, U18-ch70, adc1

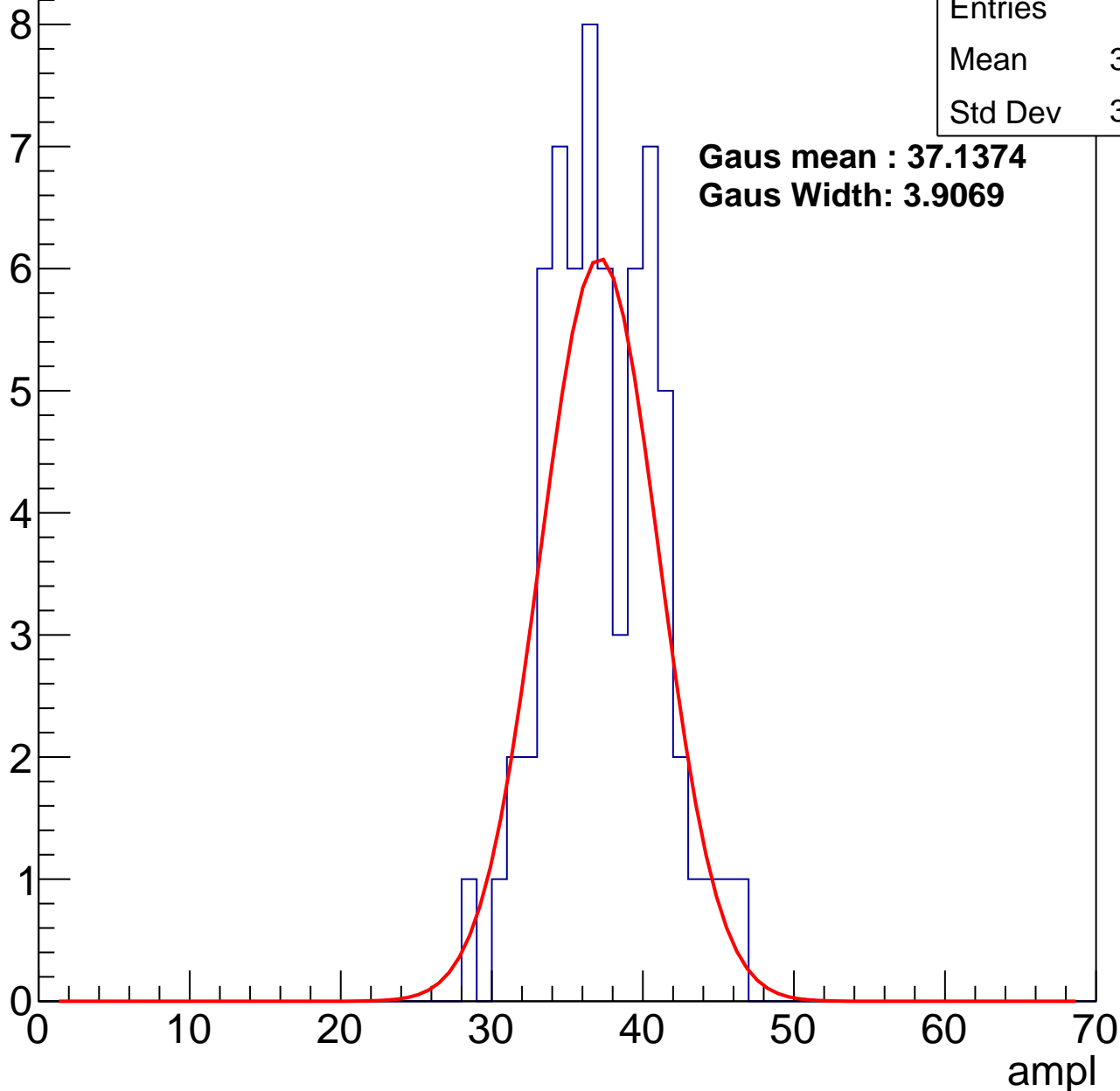
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	36.89
Std Dev	3.677

**Gaus mean : 37.1374**

**Gaus Width: 3.9069**



# B1L101S, U18-ch70, adc2

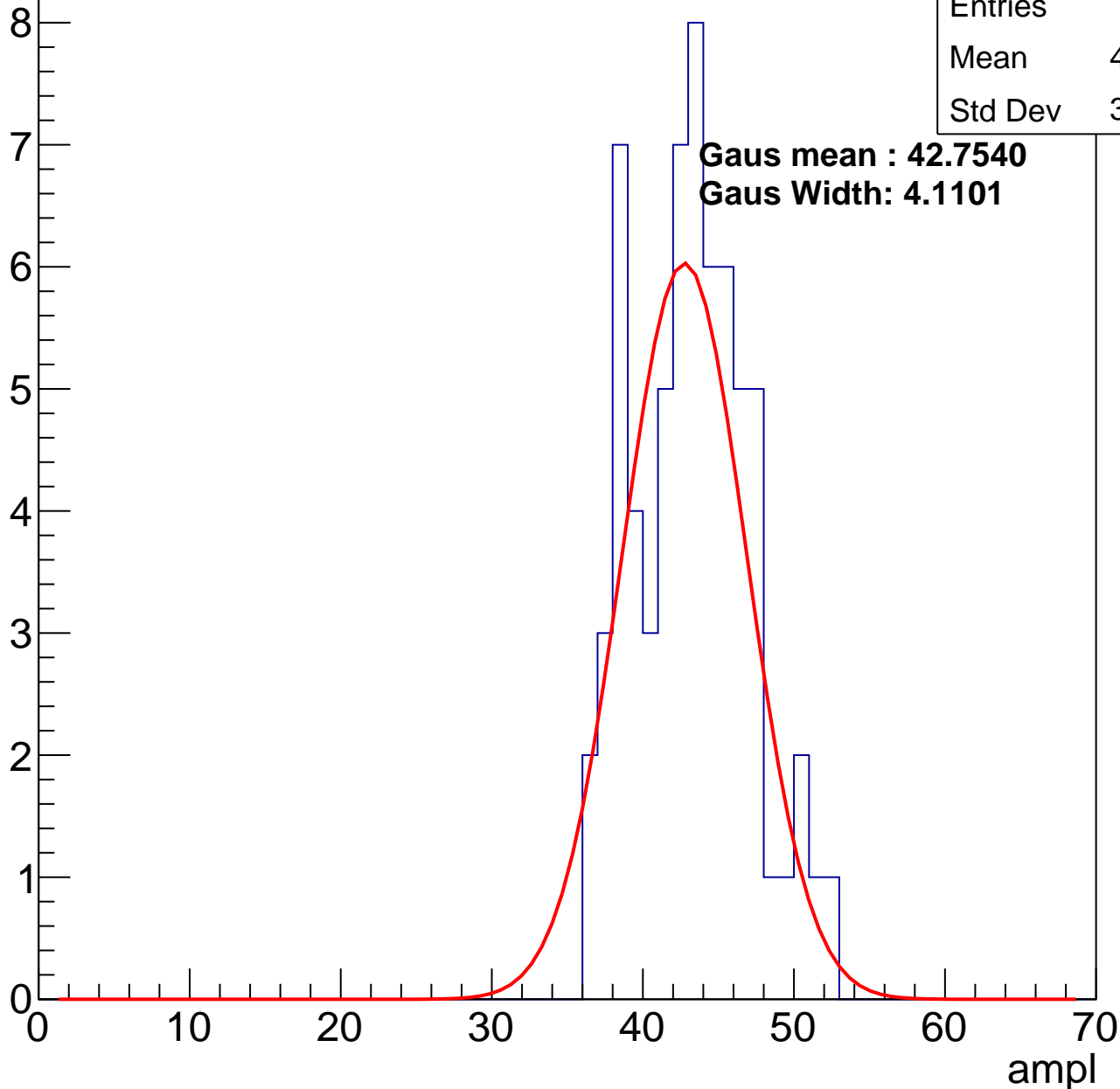
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	42.79
Std Dev	3.776

**Gaus mean : 42.7540**

**Gaus Width: 4.1101**

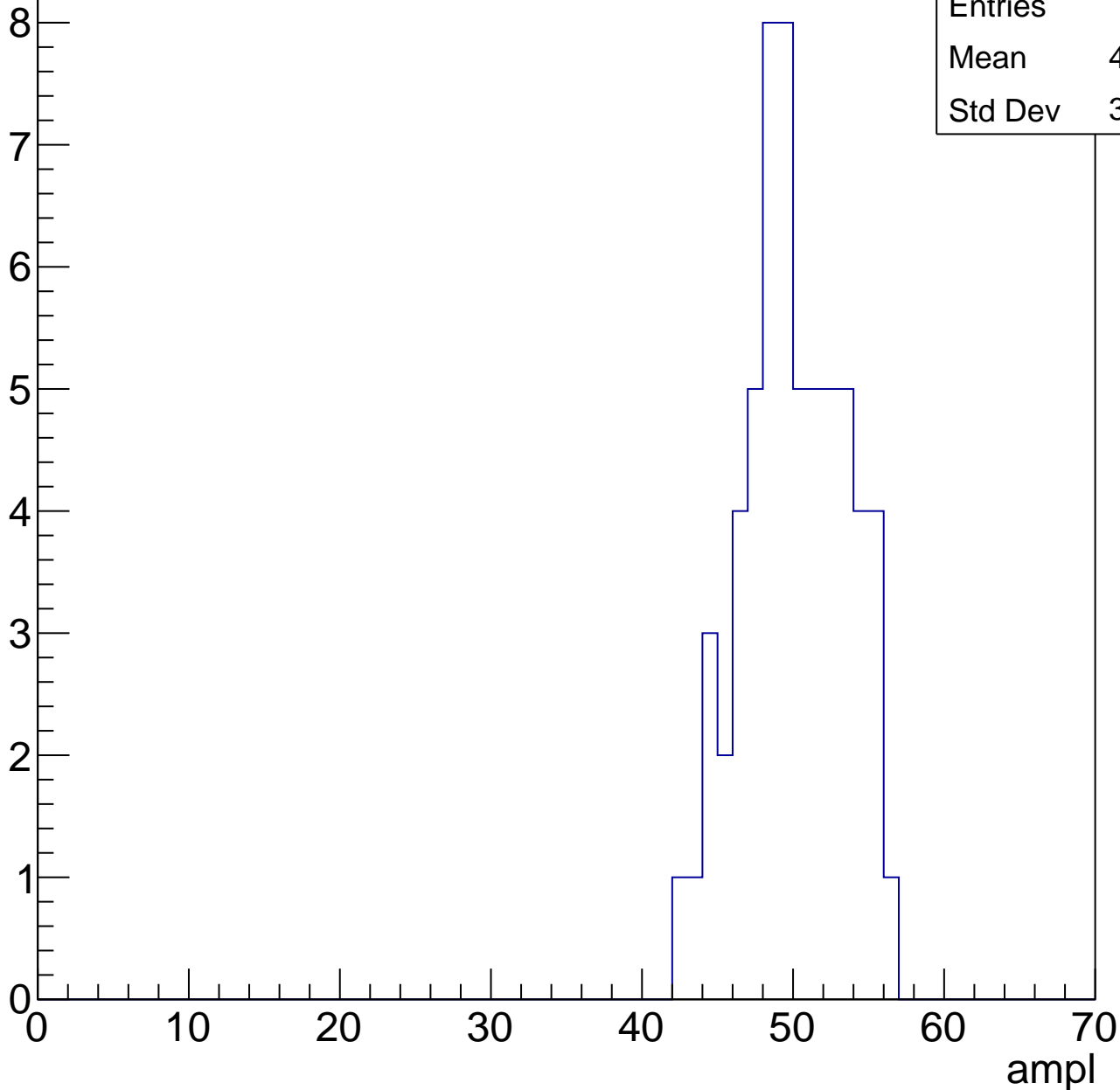


# B1L101S, U18-ch70, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	49.57
Std Dev	3.336

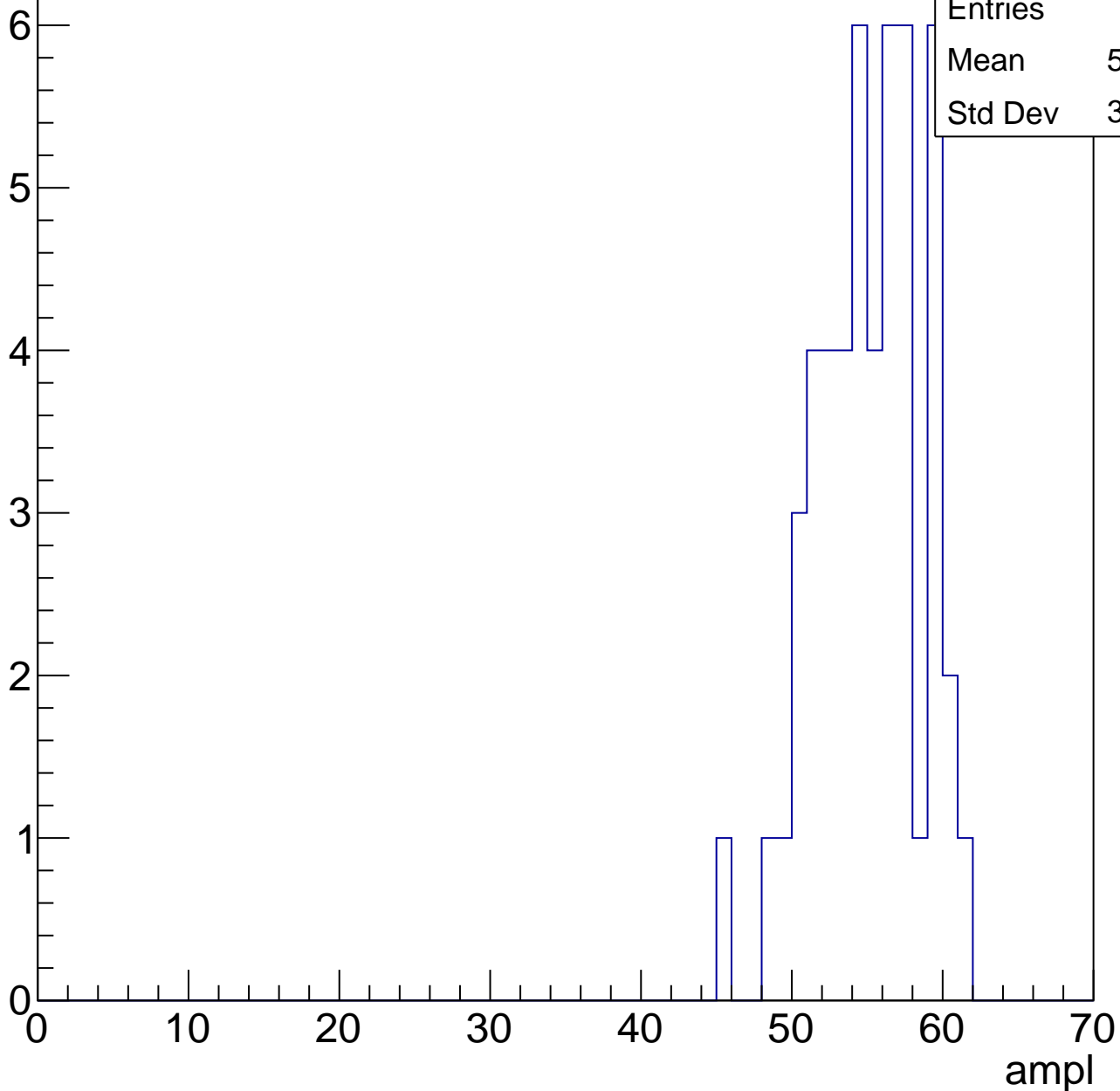


# B1L101S, U18-ch70, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	54.62
Std Dev	3.452



# B1L101S, U18-ch70, adc5

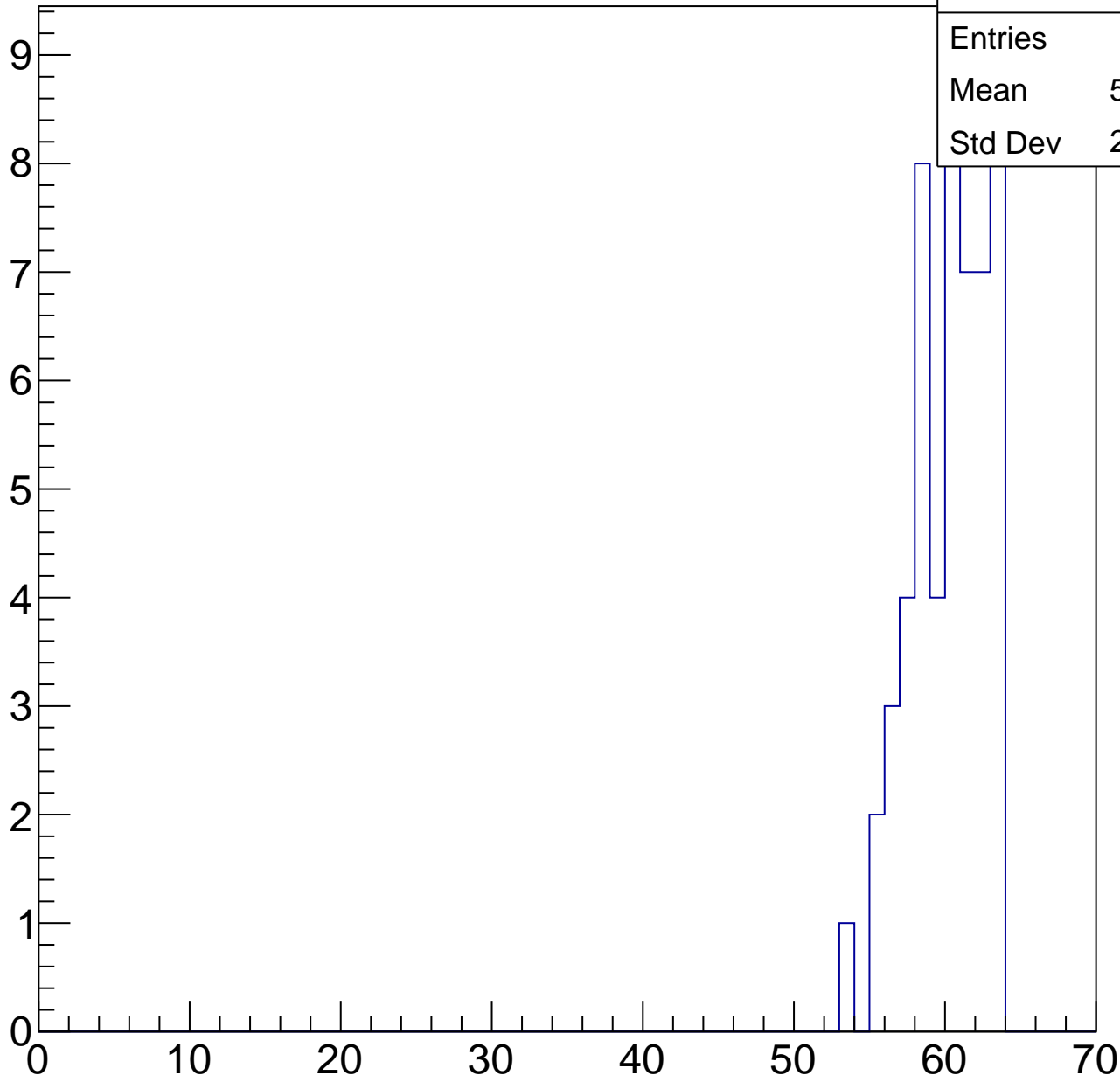
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	53
Mean	59.75
Std Dev	2.502

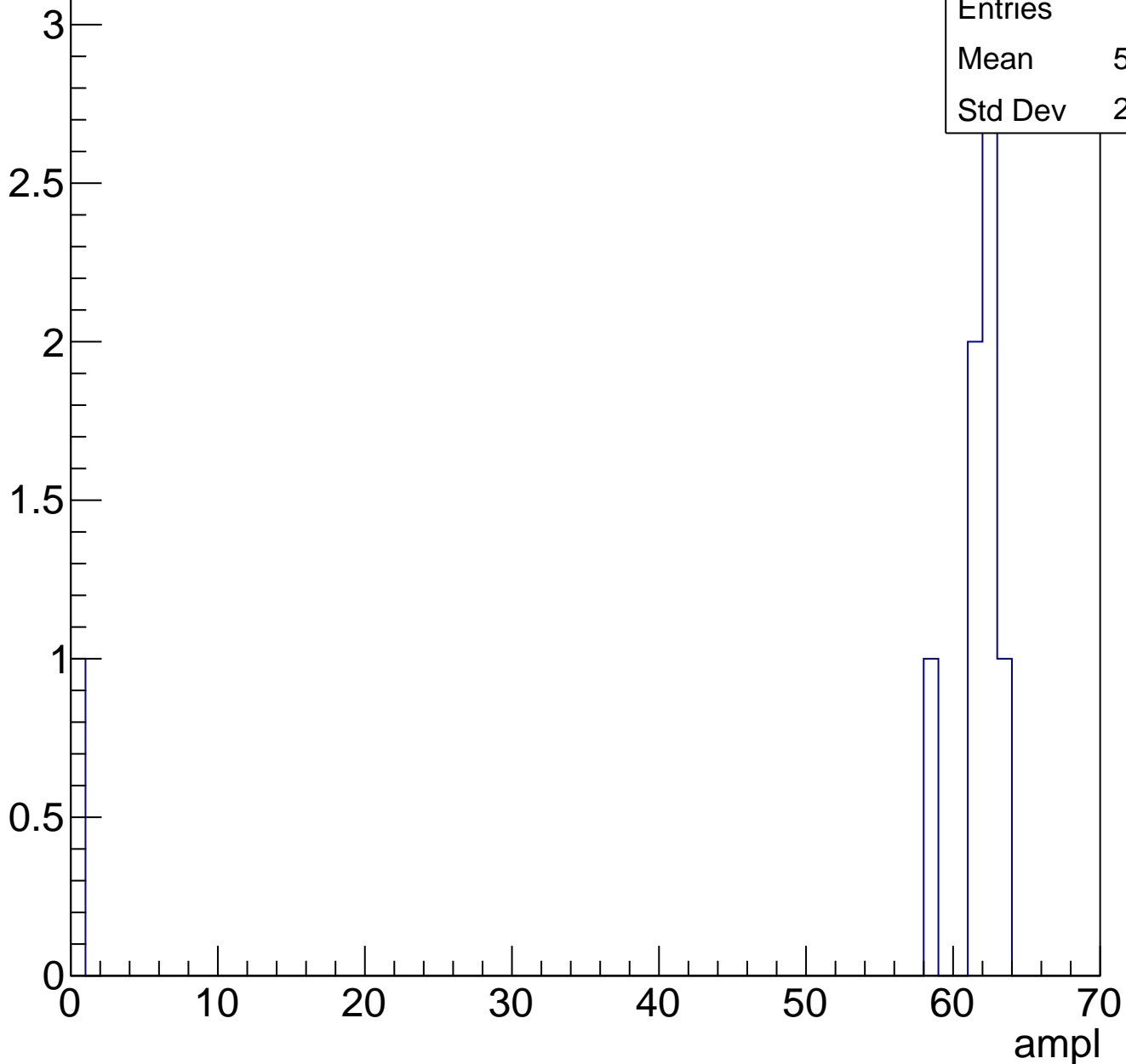
ampl



# B1L101S, U18-ch70, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch70, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	4
Mean	0
Std Dev	0

# B1L101S, U18-ch71, adc0

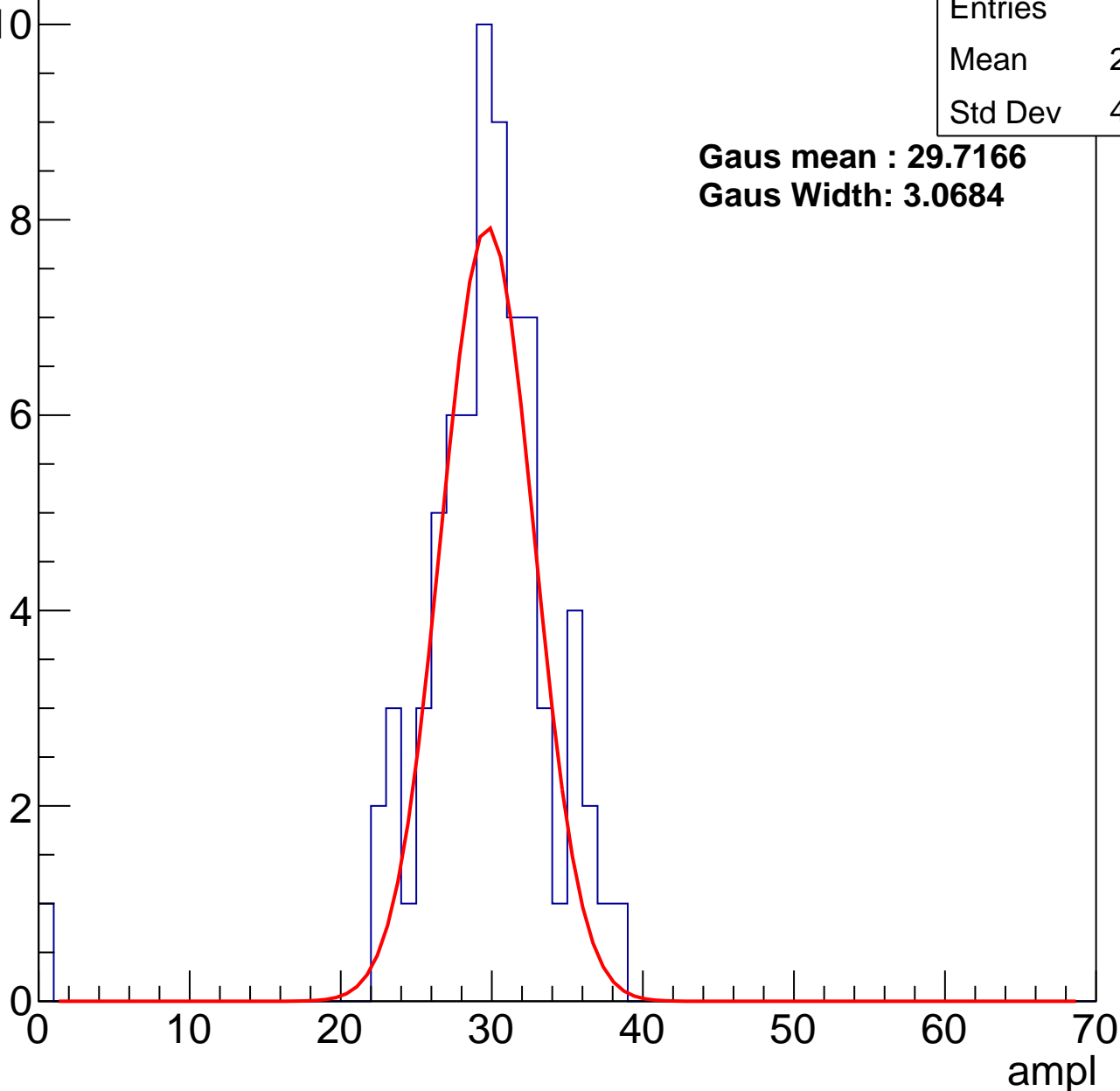
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	29.07
Std Dev	4.937

**Gaus mean : 29.7166**

**Gaus Width: 3.0684**



# B1L101S, U18-ch71, adc1

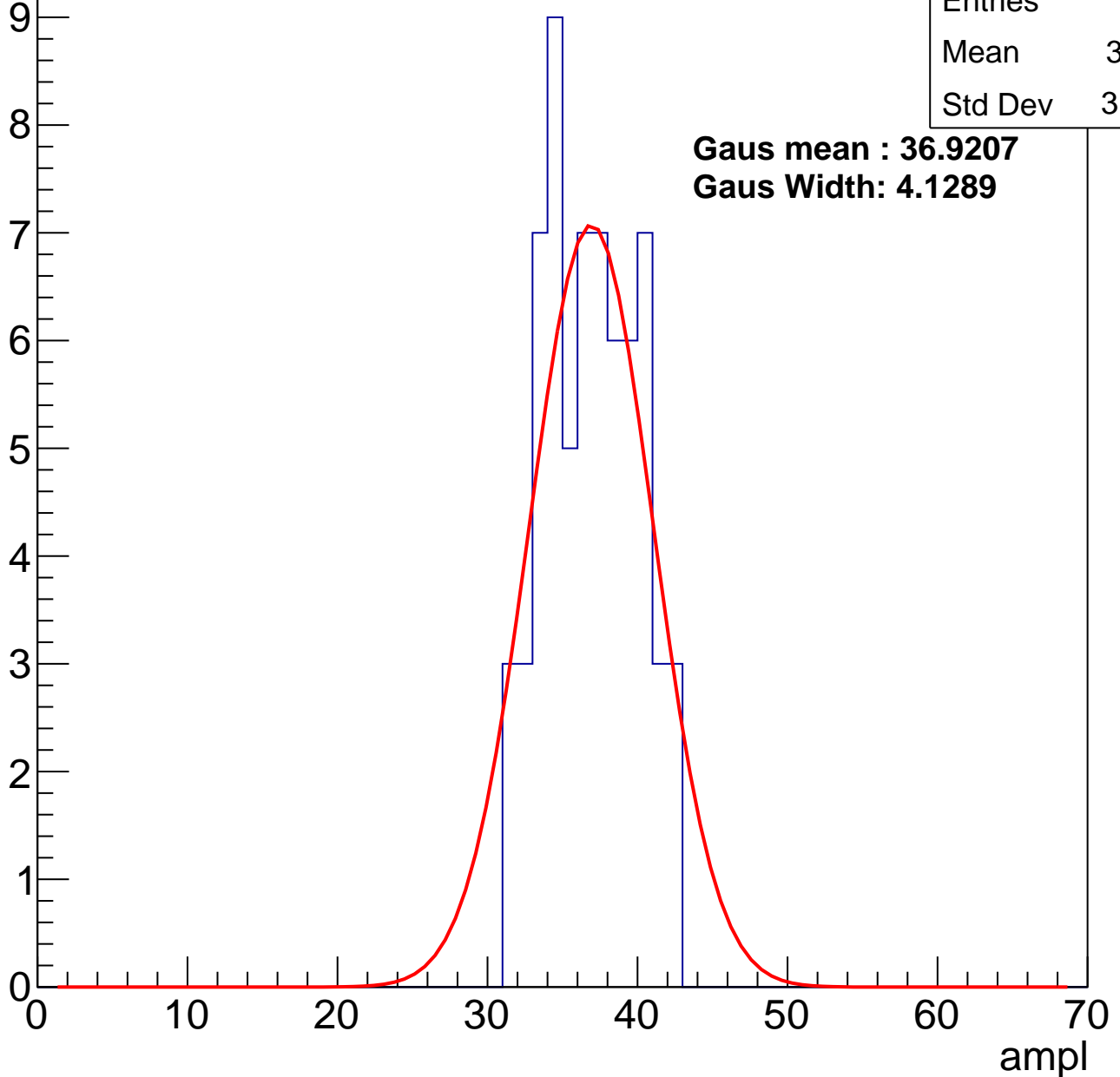
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	36.41
Std Dev	3.005

**Gaus mean : 36.9207**

**Gaus Width: 4.1289**



# B1L101S, U18-ch71, adc2

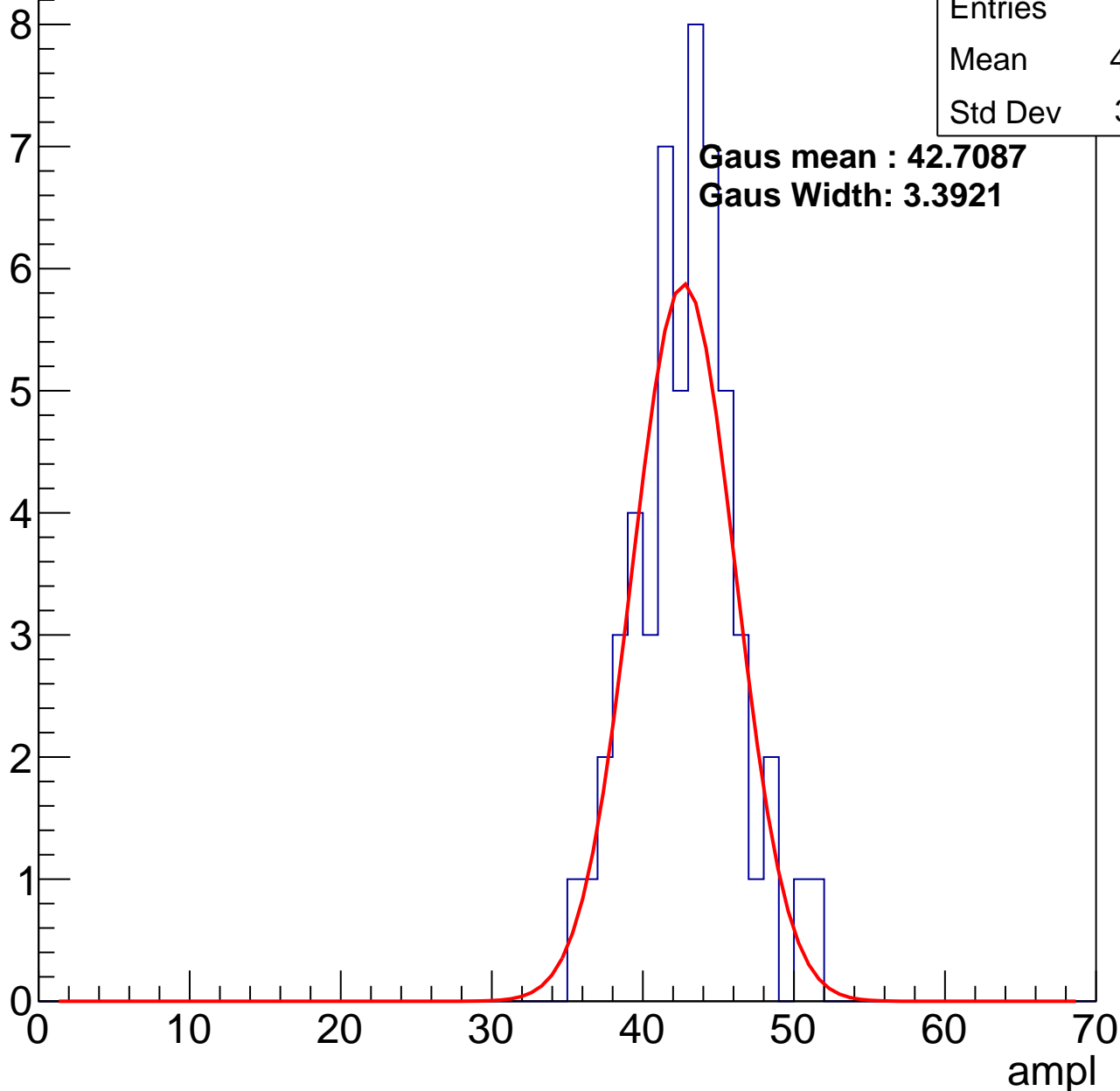
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	42.43
Std Dev	3.331

**Gaus mean : 42.7087**

**Gaus Width: 3.3921**

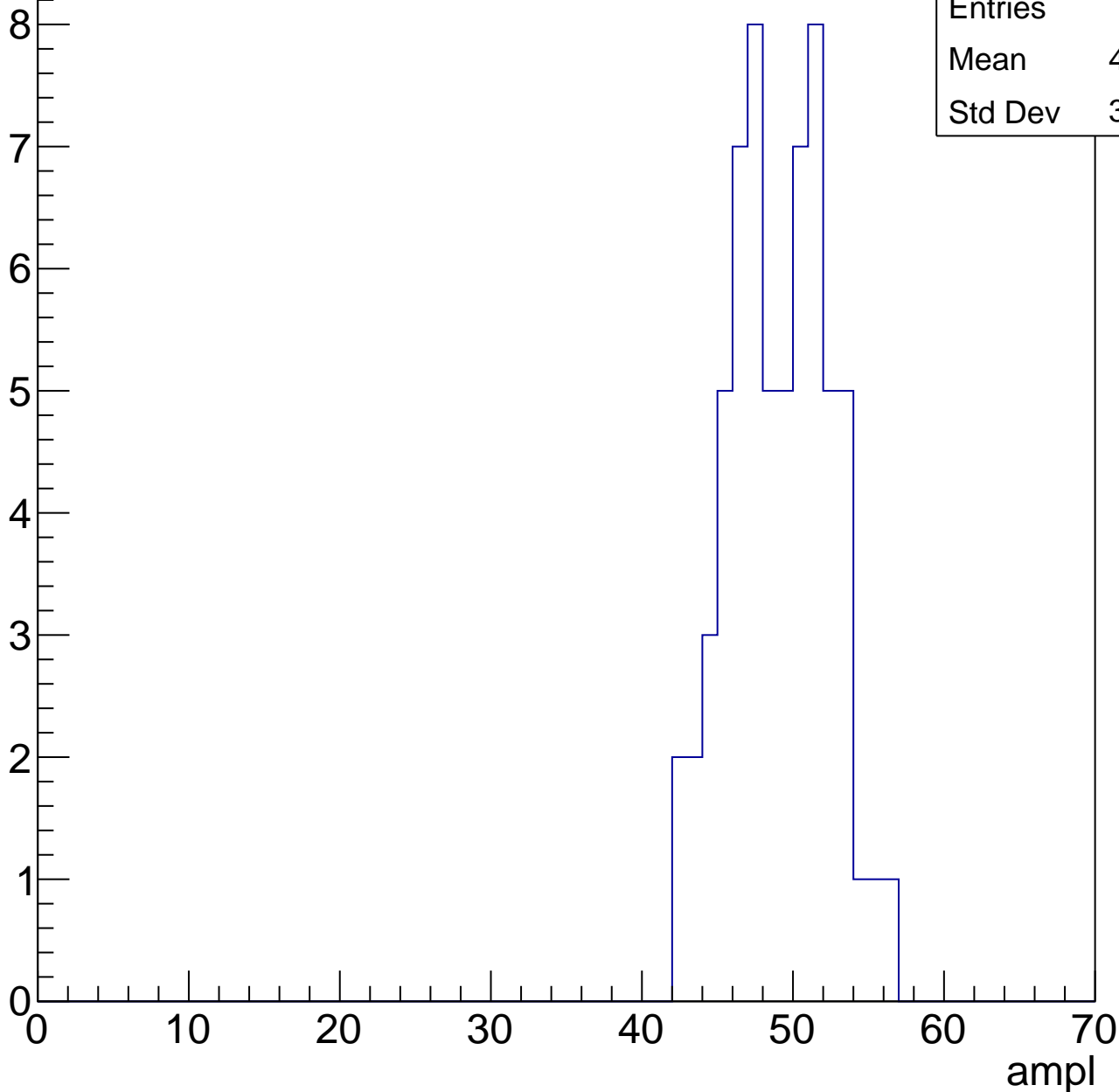


# B1L101S, U18-ch71, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	48.58
Std Dev	3.253

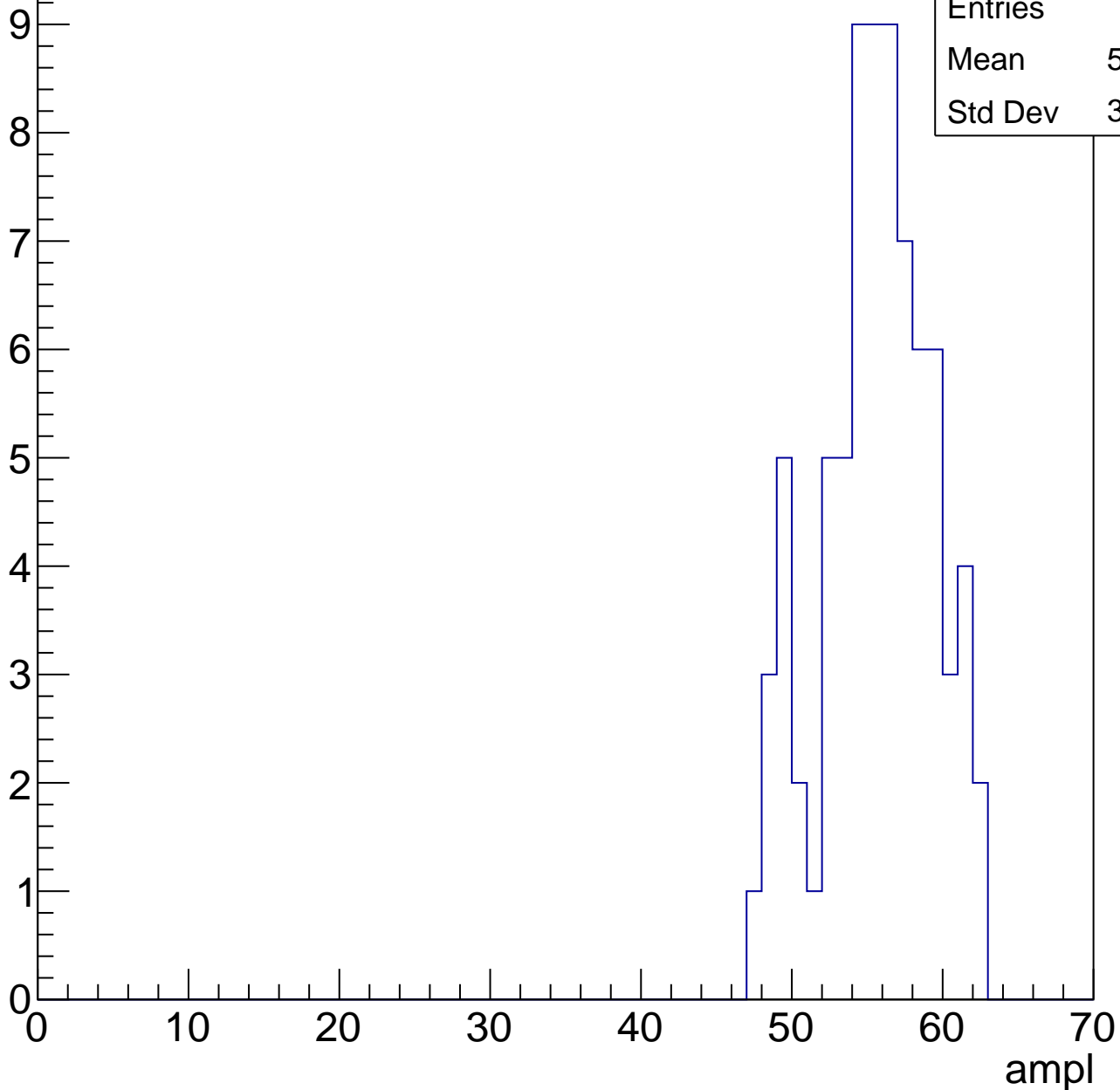


# B1L101S, U18-ch71, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	55.14
Std Dev	3.663



# B1L101S, U18-ch71, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	38
Mean	58.95
Std Dev	9.875

ampl

0

10

20

30

40

50

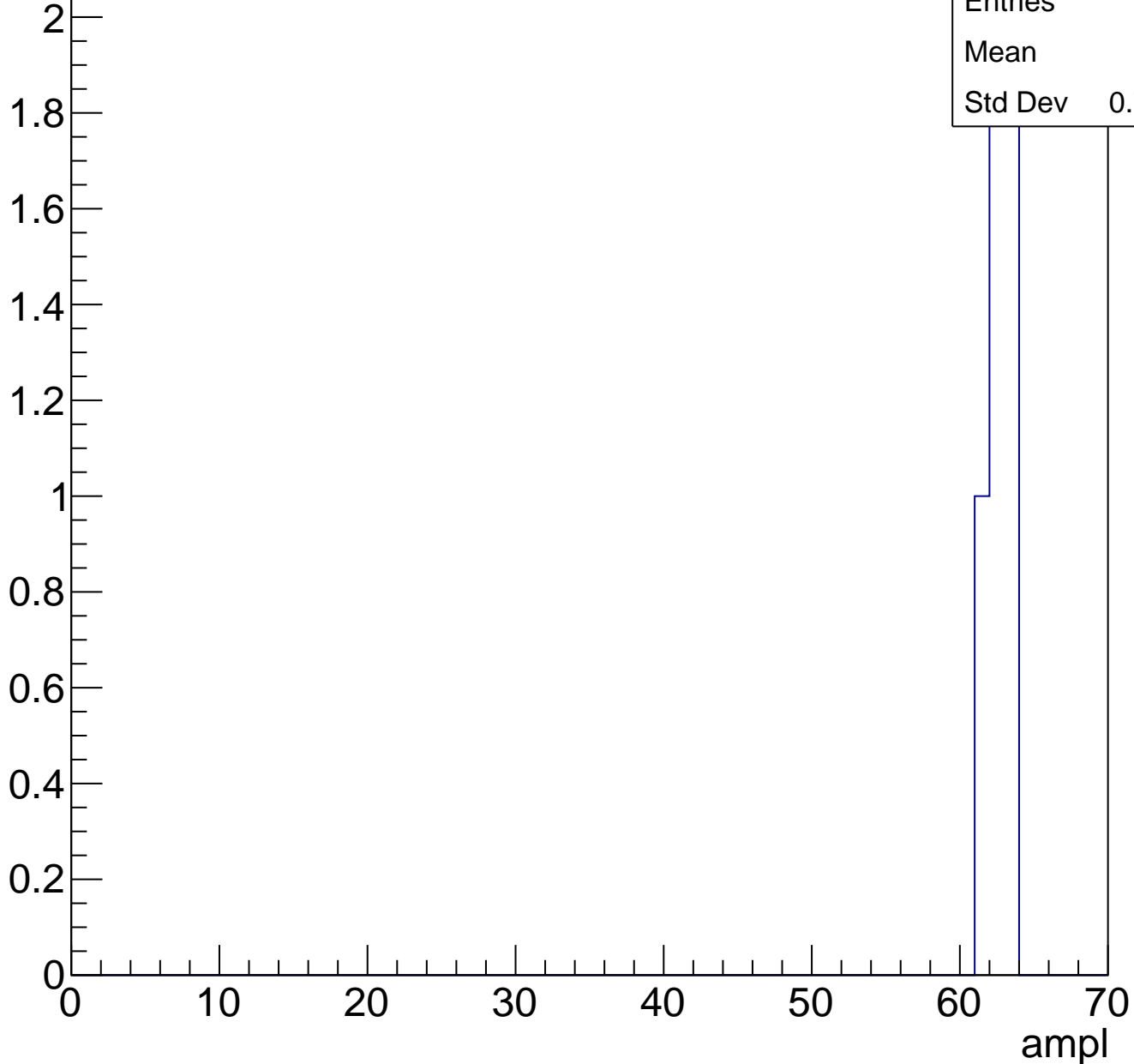
60

70

# B1L101S, U18-ch71, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch71, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch72, adc0

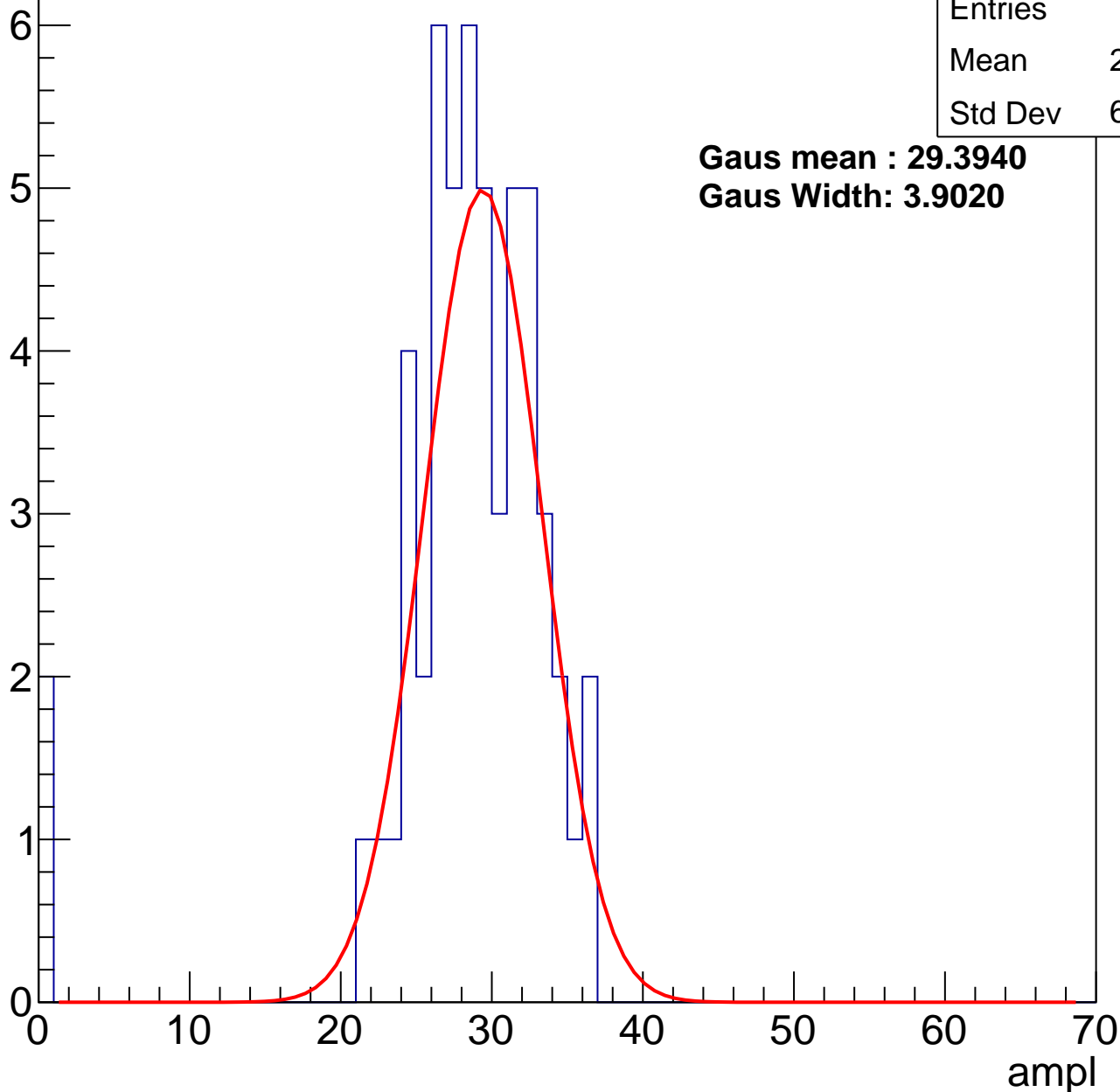
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	27.69
Std Dev	6.454

**Gaus mean : 29.3940**

**Gaus Width: 3.9020**



# B1L101S, U18-ch72, adc1

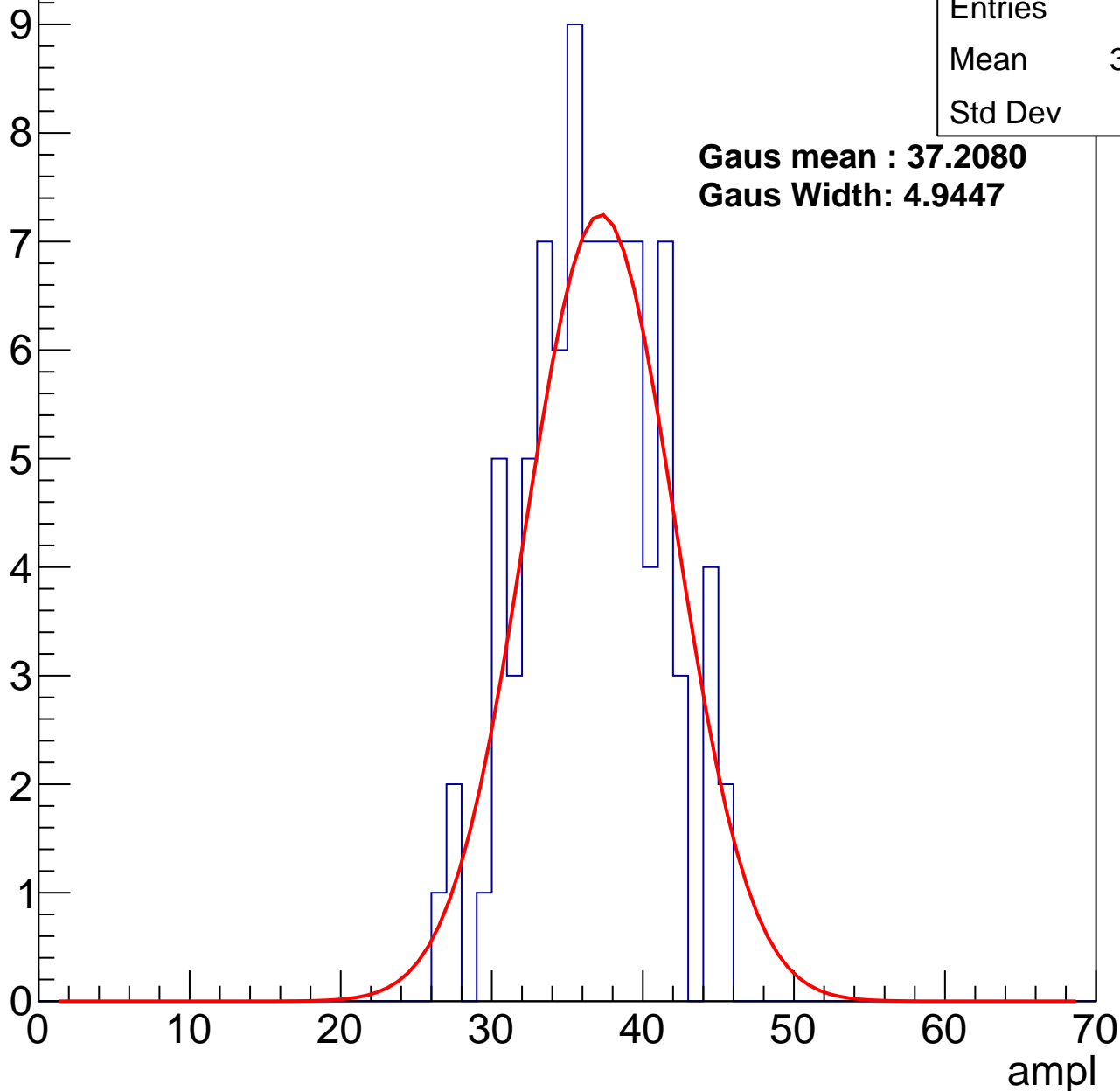
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	87
Mean	36.22
Std Dev	4.29

**Gaus mean : 37.2080**

**Gaus Width: 4.9447**



# B1L101S, U18-ch72, adc2

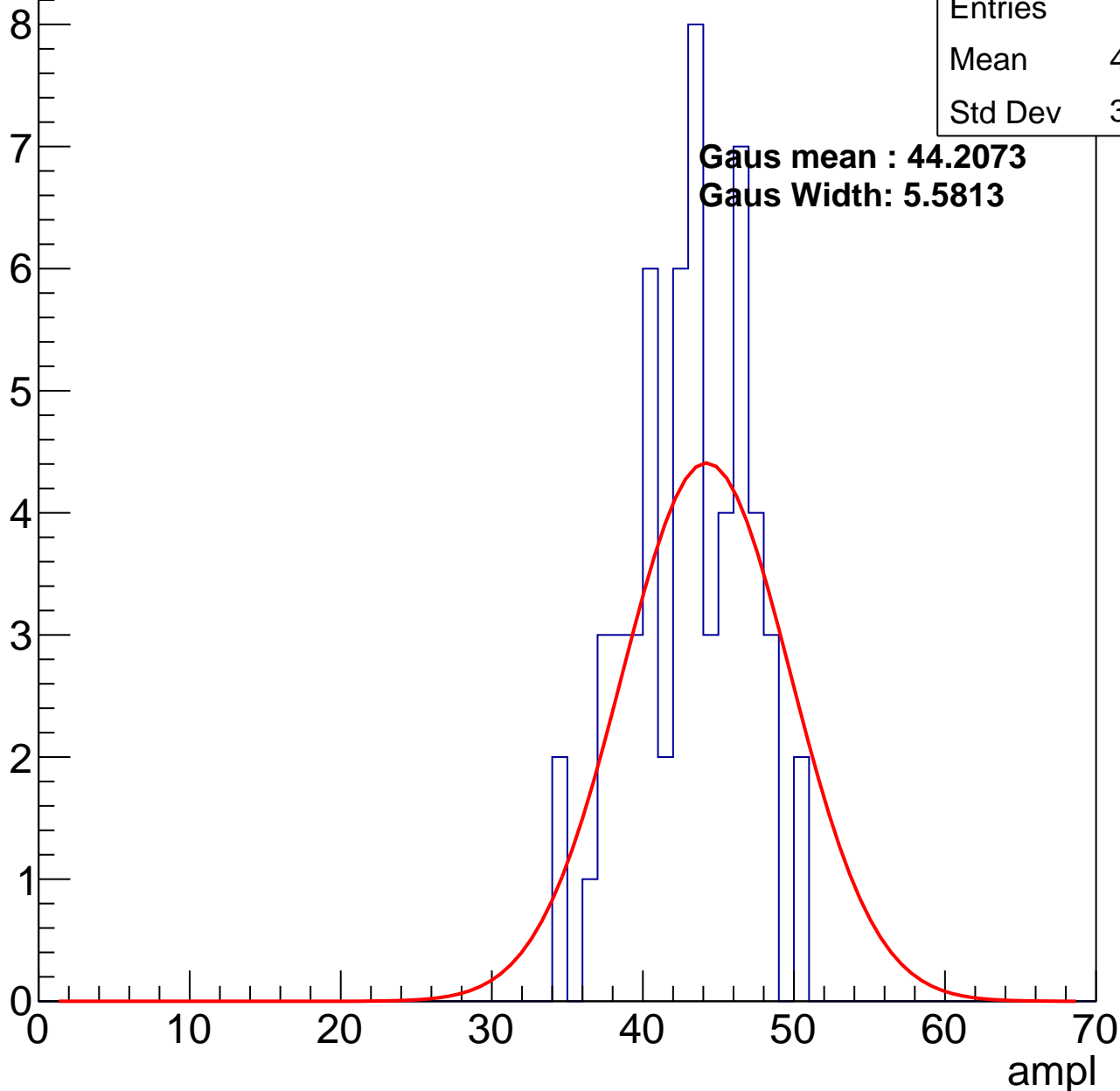
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	42.63
Std Dev	3.796

**Gaus mean : 44.2073**

**Gaus Width: 5.5813**

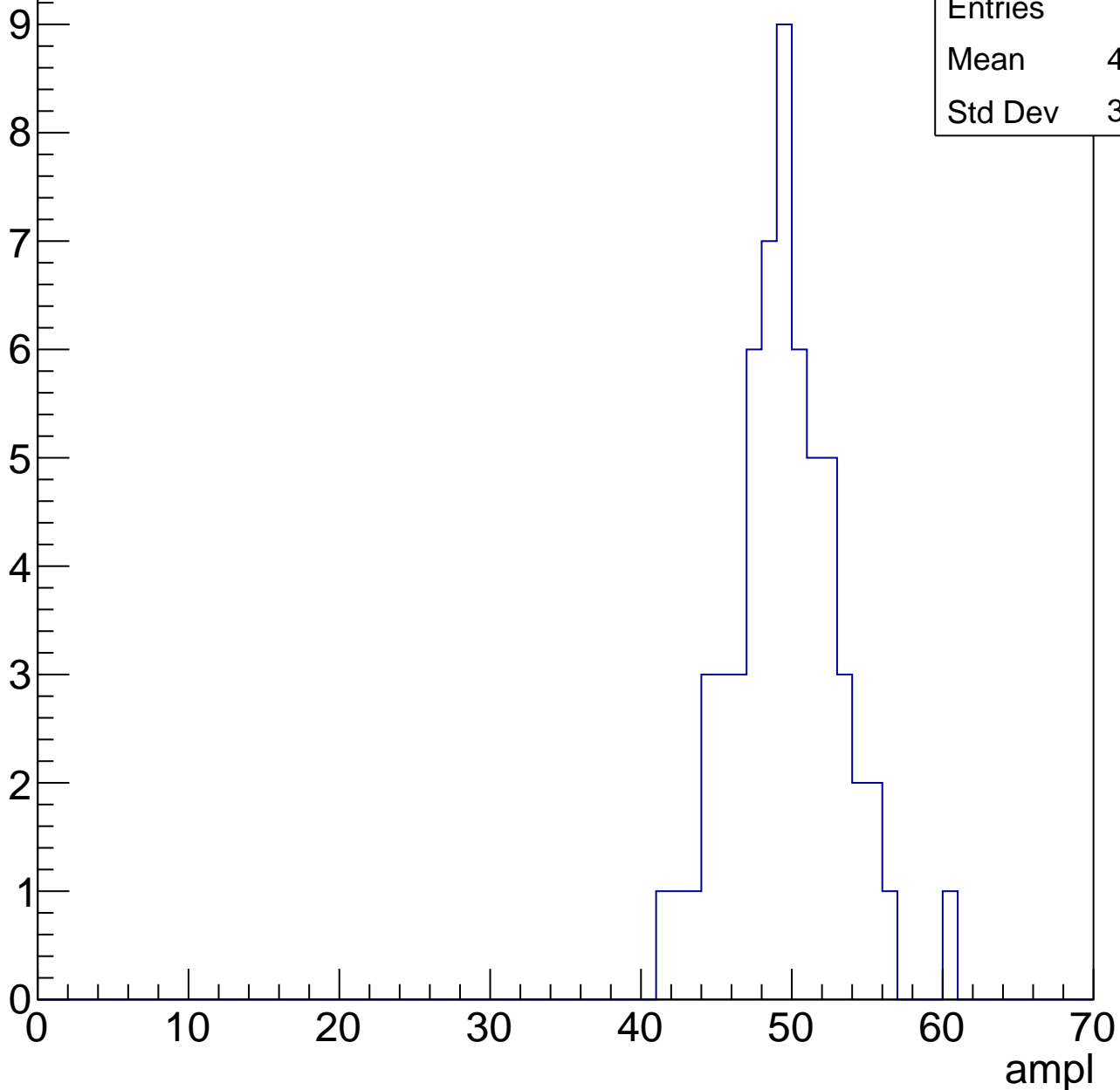


# B1L101S, U18-ch72, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	49.12
Std Dev	3.542

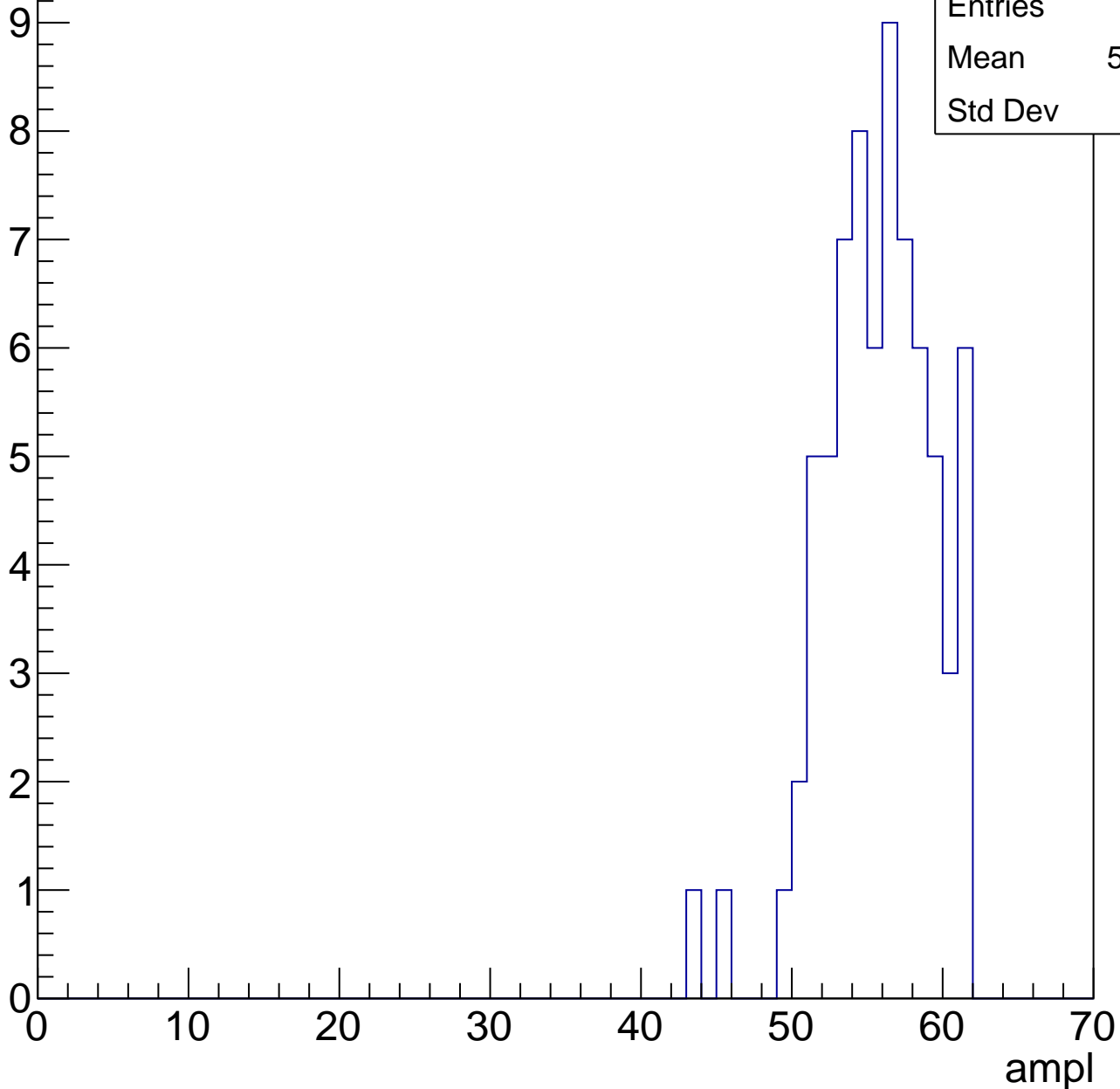


# B1L101S, U18-ch72, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

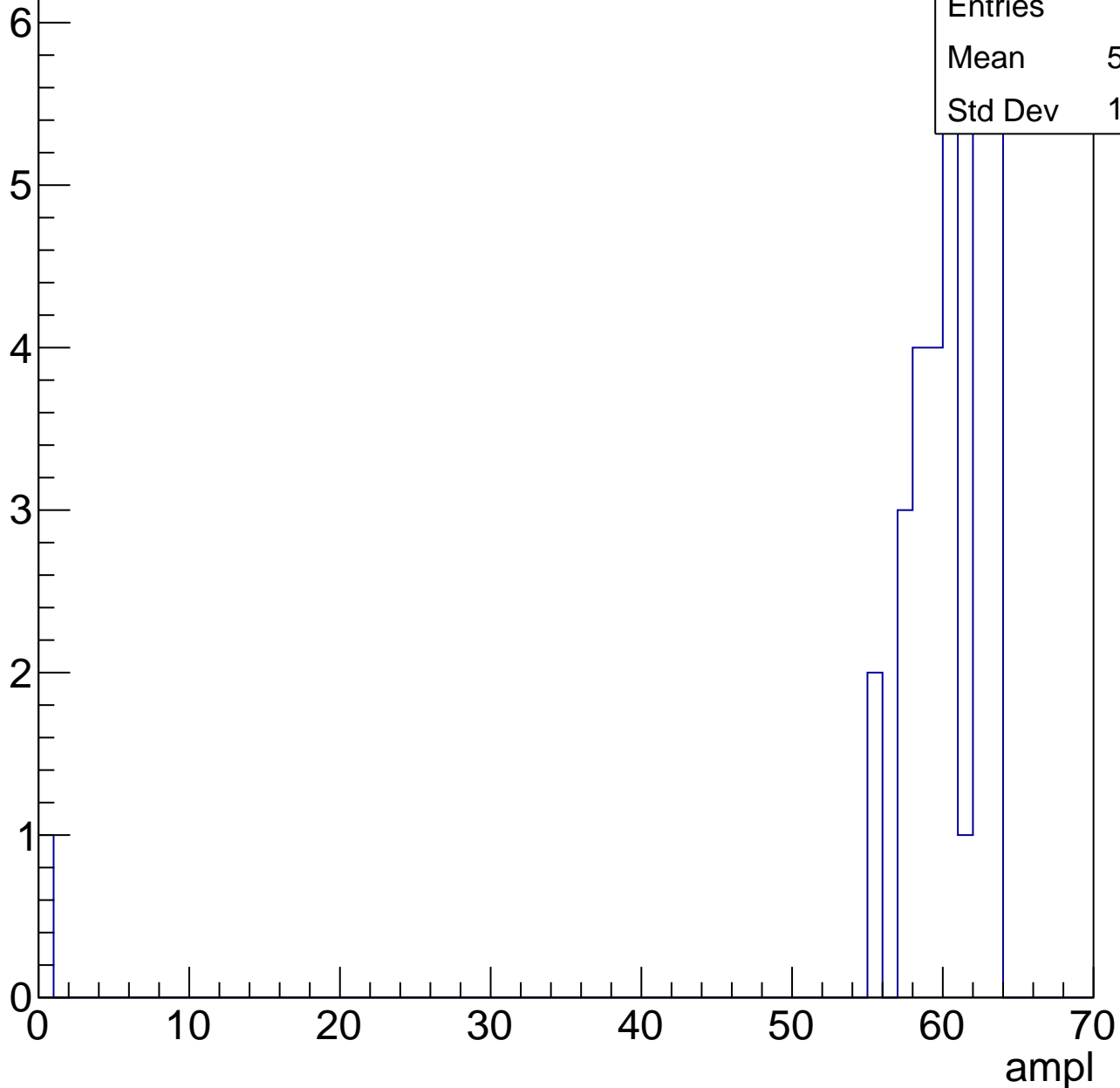
Entries	72
Mean	55.24
Std Dev	3.63



# B1L101S, U18-ch72, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

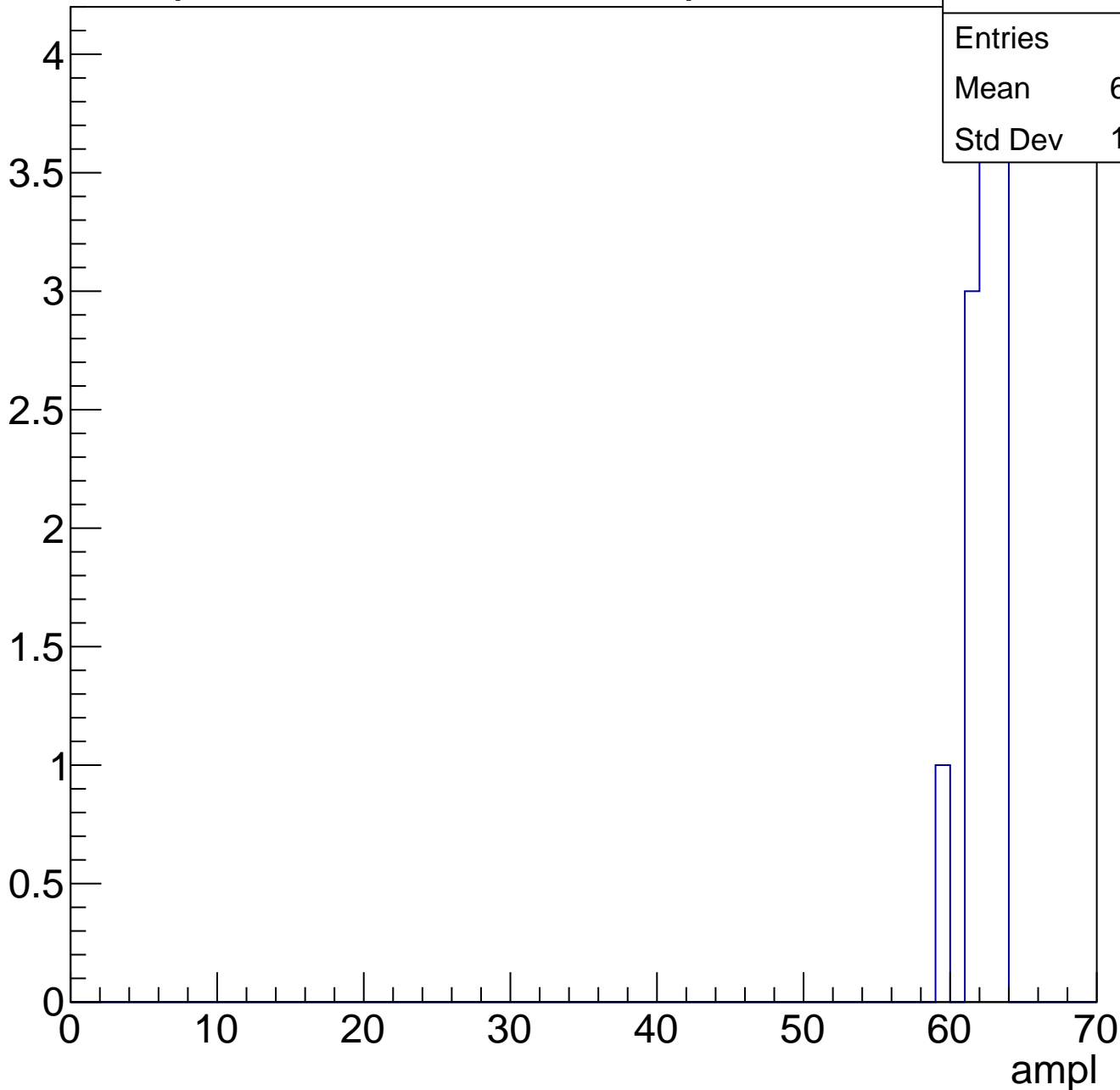
Entry



# B1L101S, U18-ch72, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch72, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch73, adc0

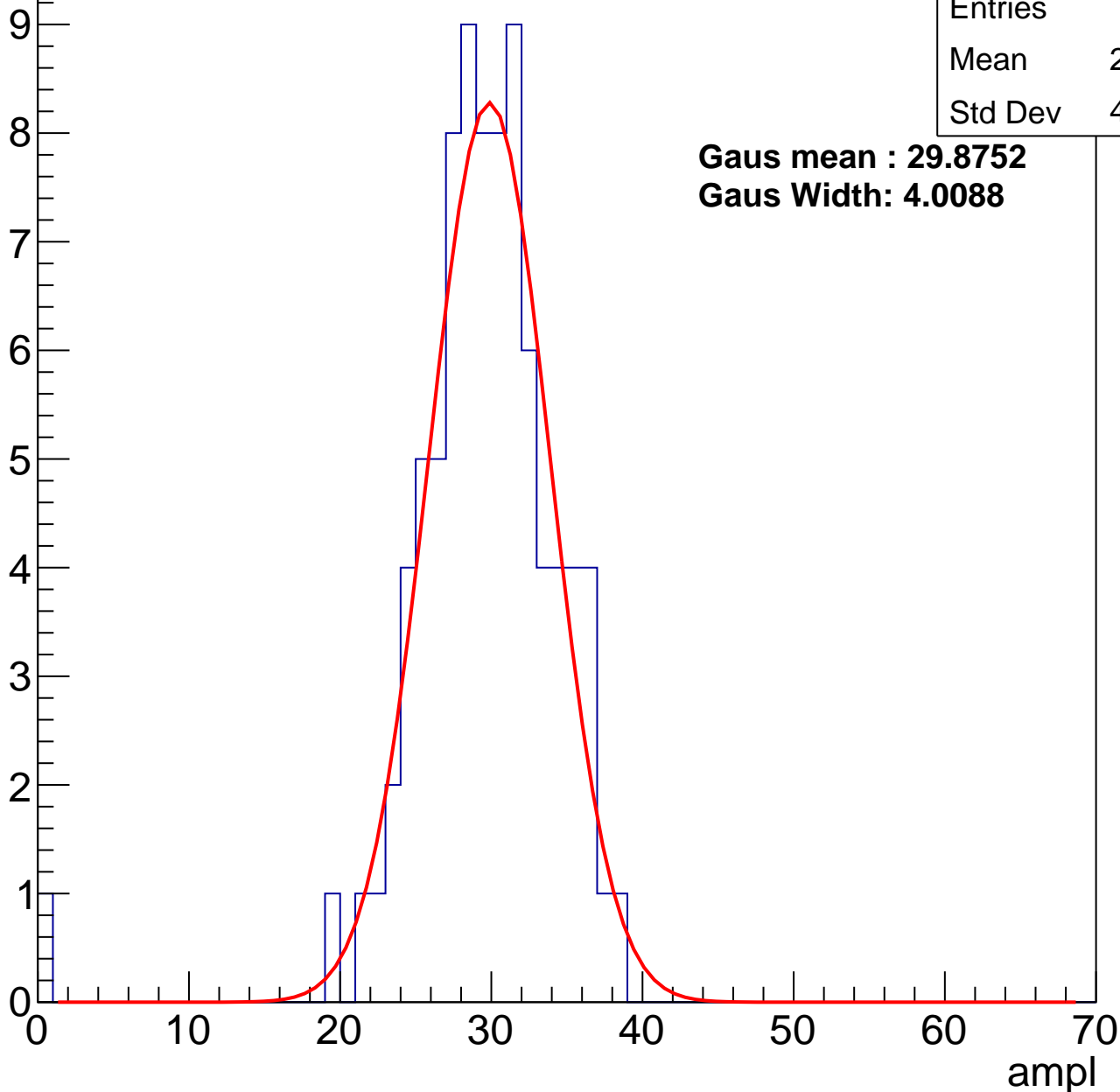
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	86
Mean	29.03
Std Dev	4.987

**Gaus mean : 29.8752**

**Gaus Width: 4.0088**



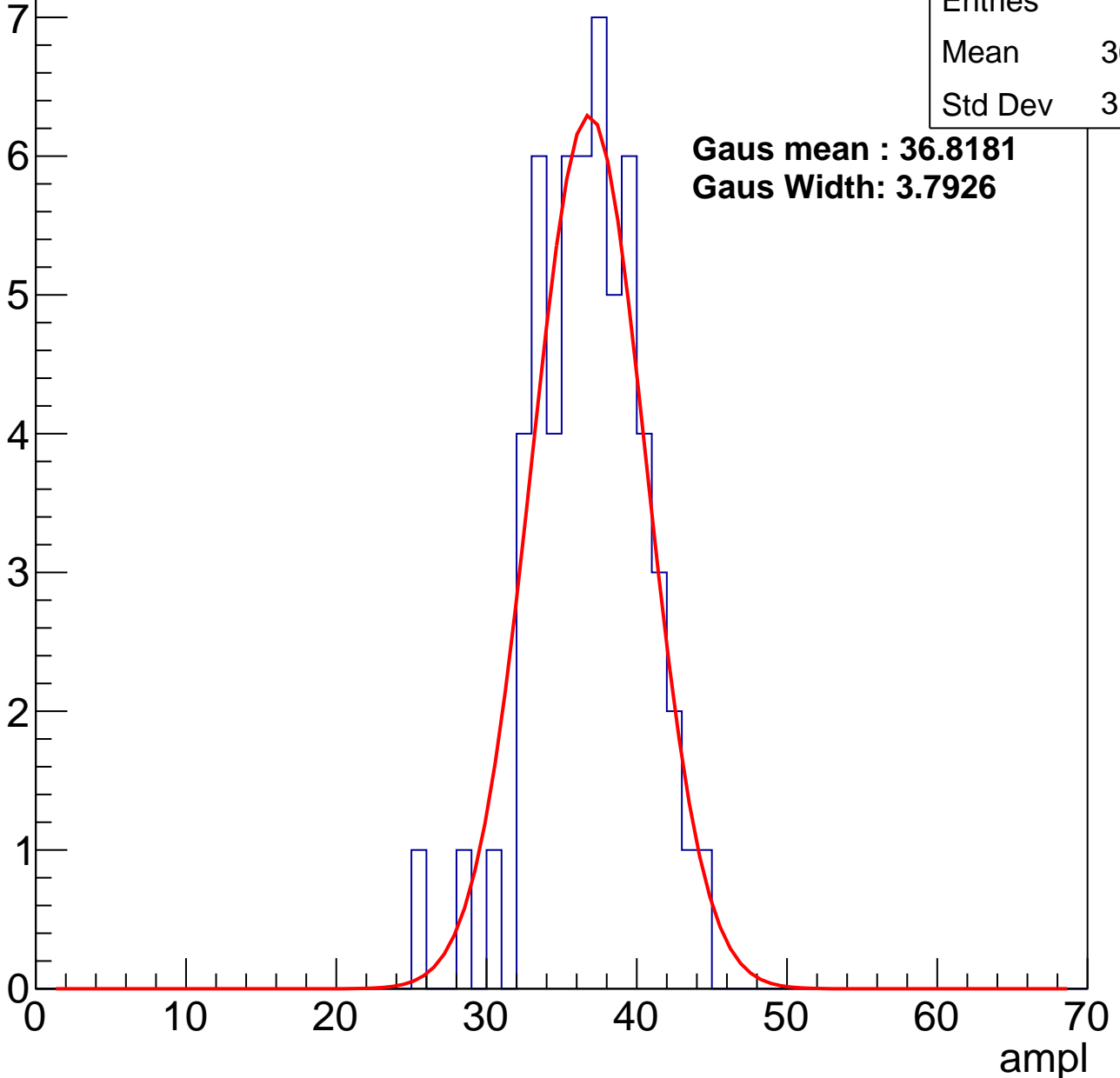
# B1L101S, U18-ch73, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

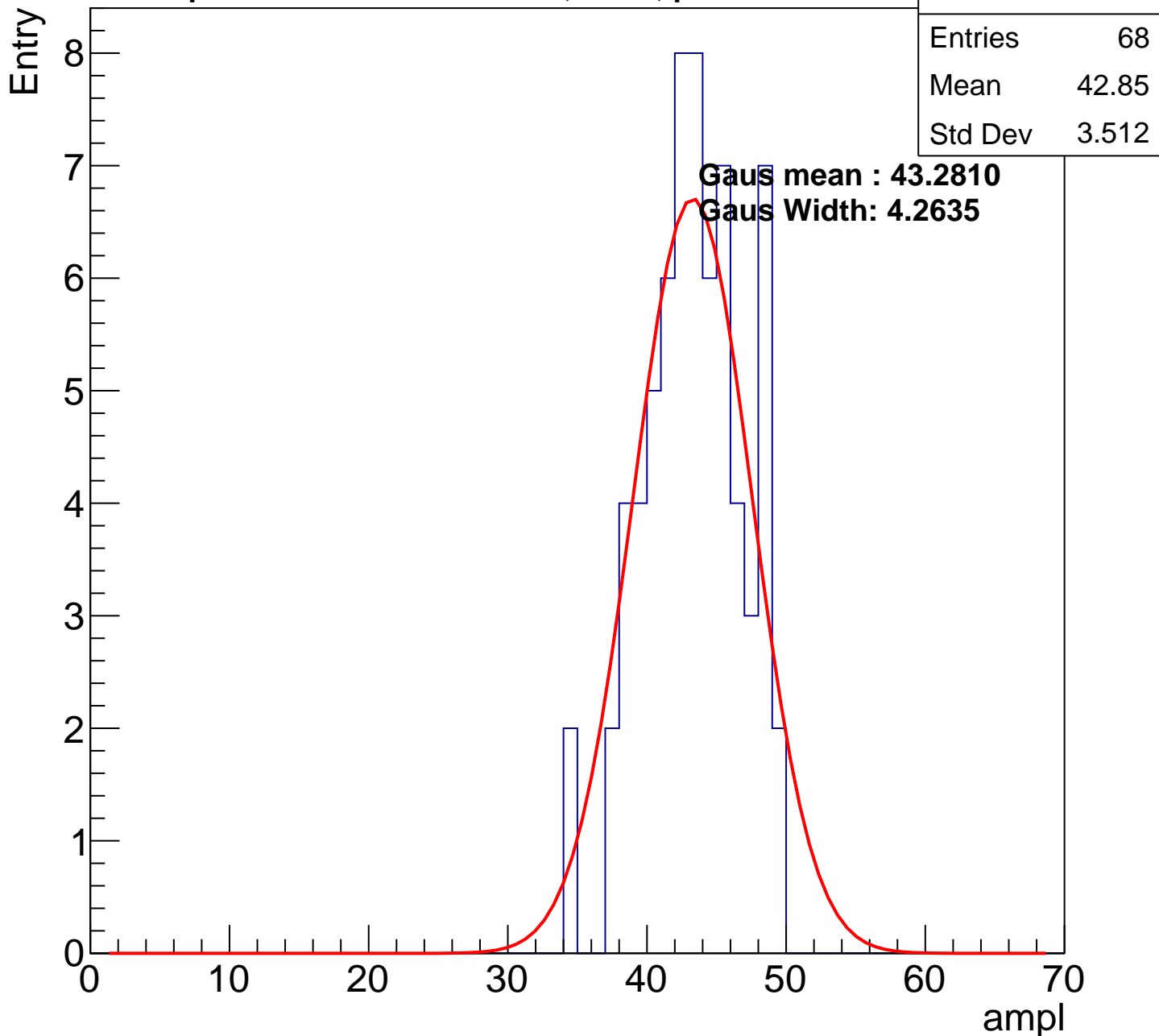
Entries	58
Mean	36.34
Std Dev	3.618

**Gaus mean : 36.8181**  
**Gaus Width: 3.7926**



# B1L101S, U18-ch73, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

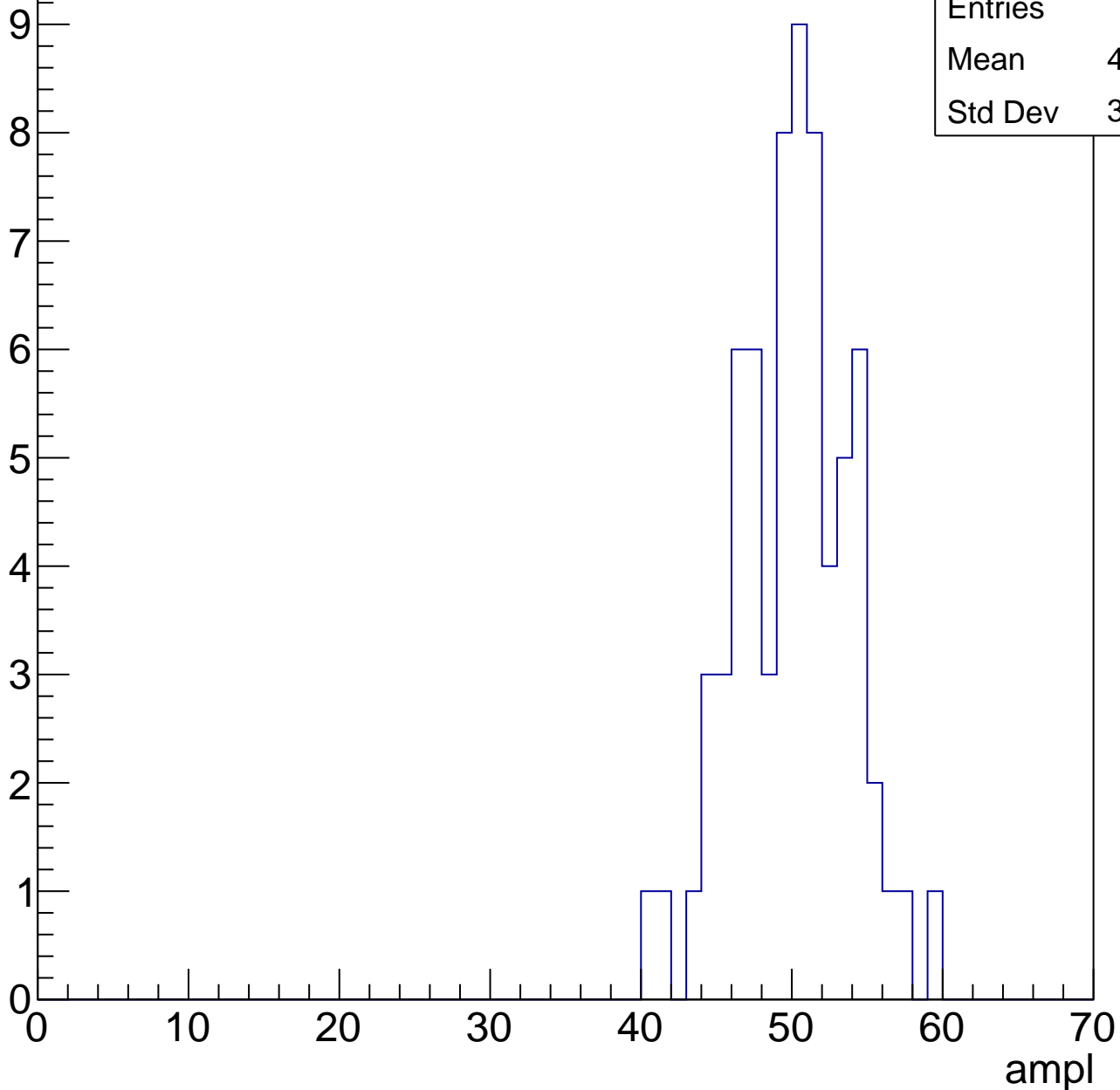


# B1L101S, U18-ch73, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	49.59
Std Dev	3.716

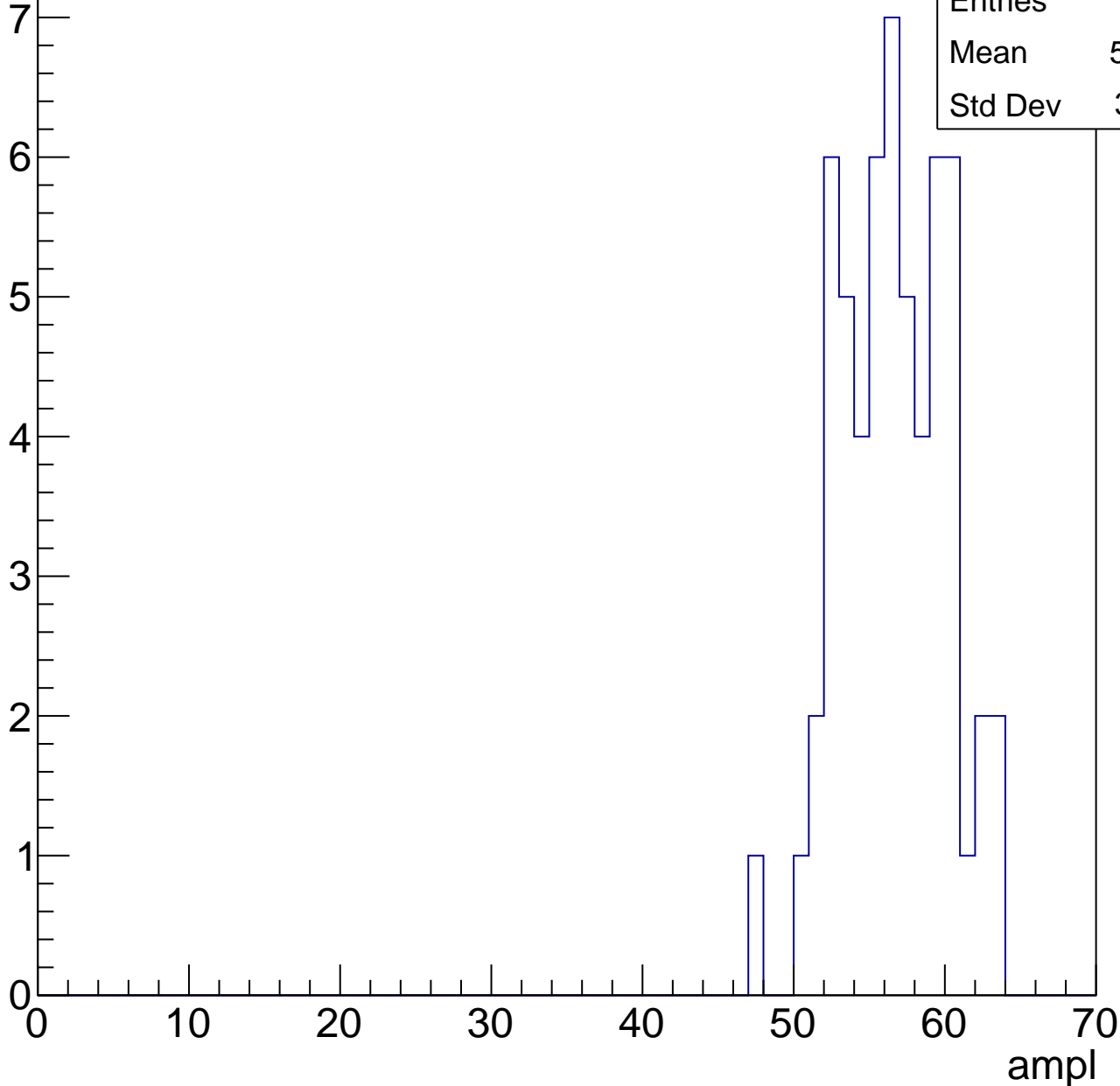


# B1L101S, U18-ch73, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	56.14
Std Dev	3.461

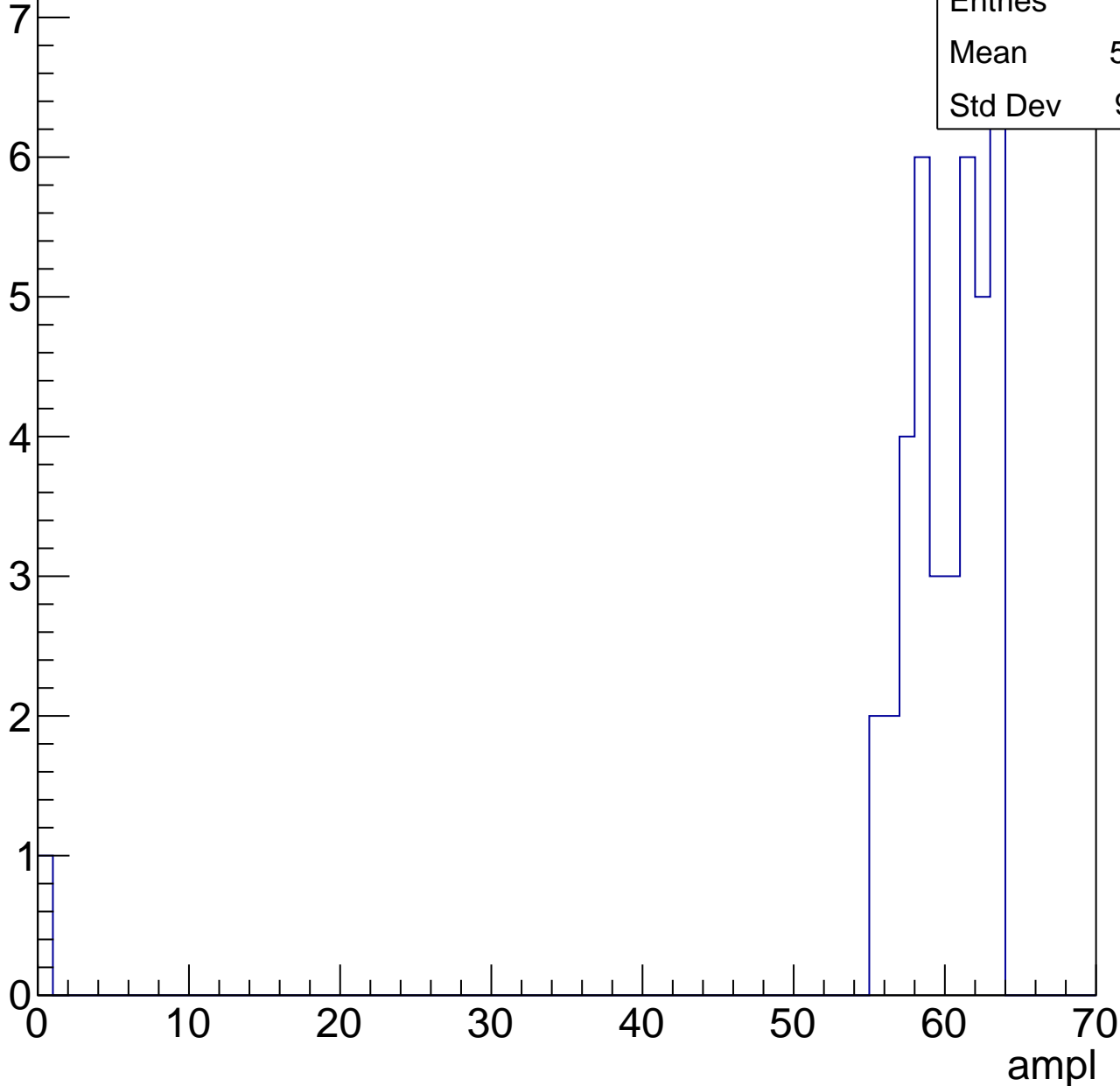


# B1L101S, U18-ch73, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

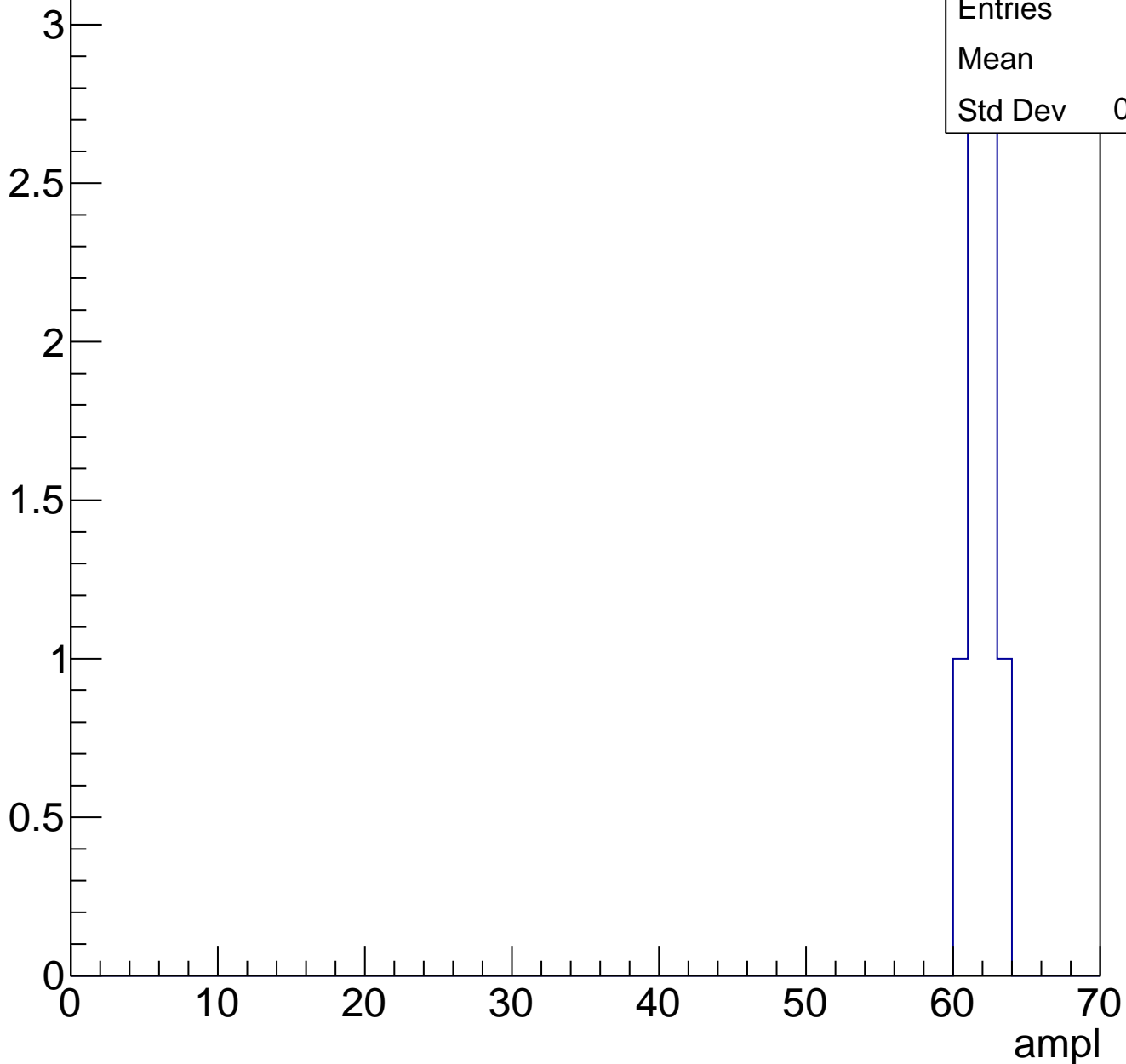
Entries	39
Mean	58.26
Std Dev	9.761



# B1L101S, U18-ch73, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch73, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch74, adc0

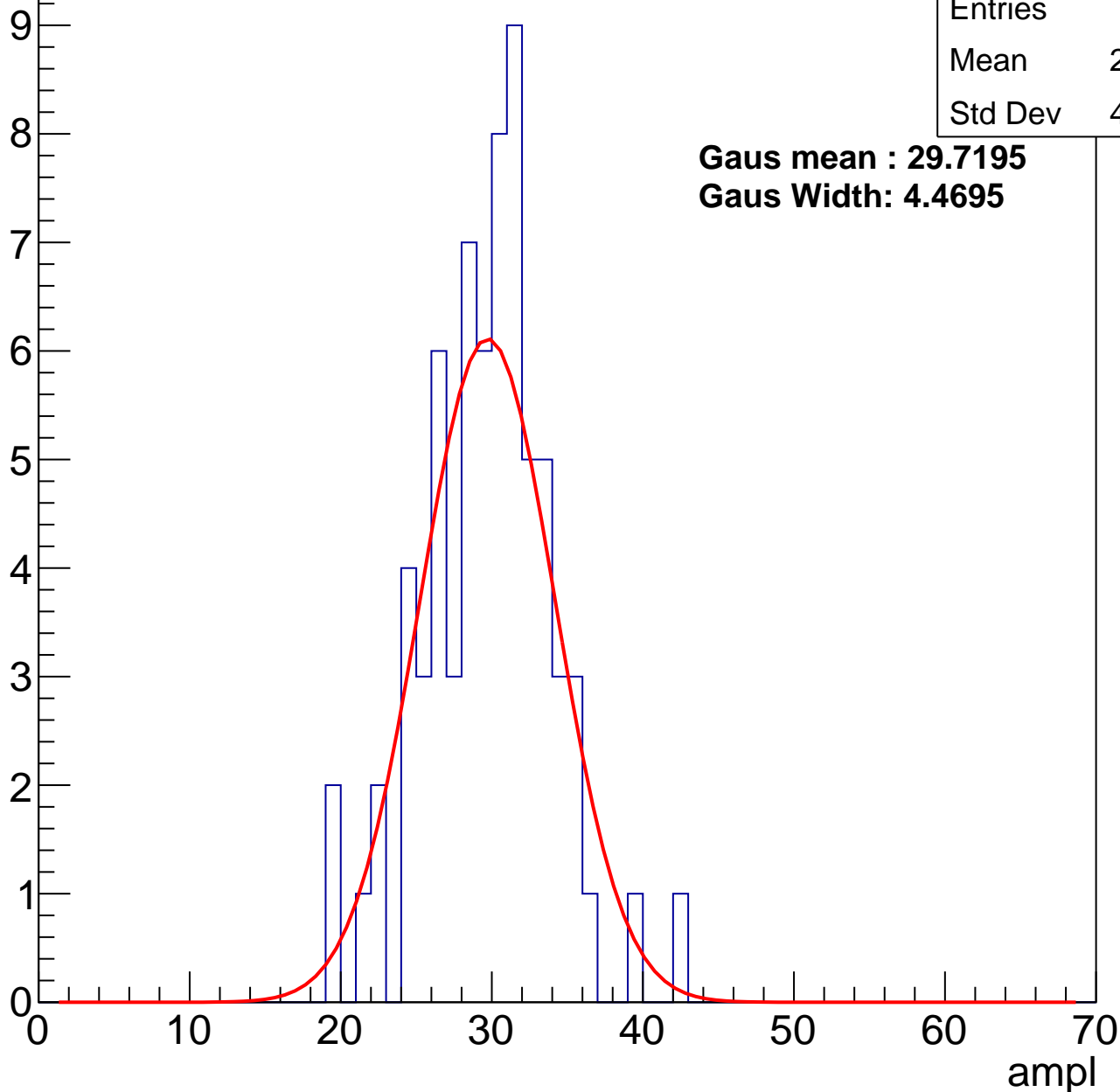
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	29.27
Std Dev	4.222

**Gaus mean : 29.7195**

**Gaus Width: 4.4695**



# B1L101S, U18-ch74, adc1

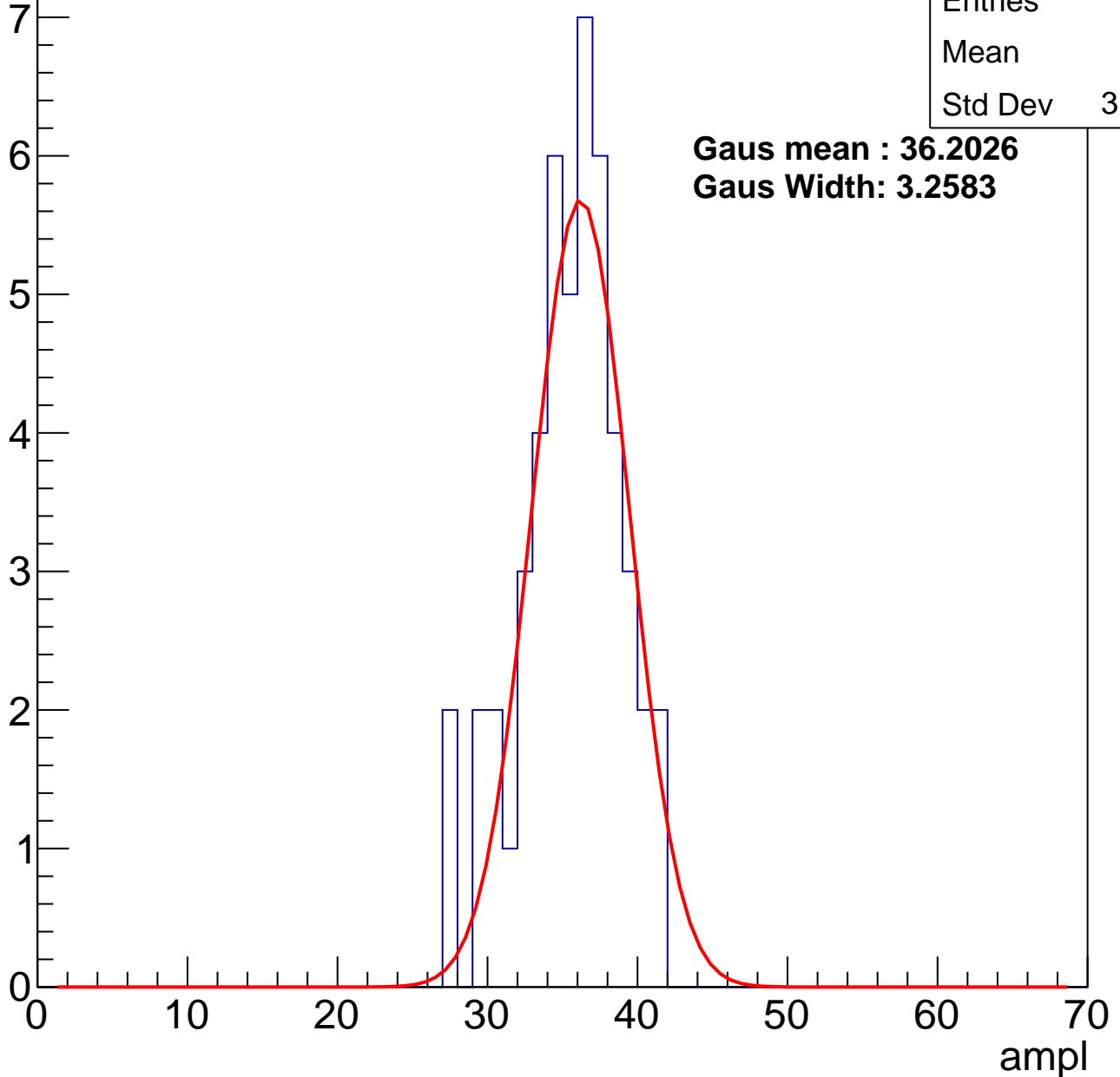
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	49
Mean	35
Std Dev	3.356

**Gaus mean : 36.2026**

**Gaus Width: 3.2583**



# B1L101S, U18-ch74, adc2

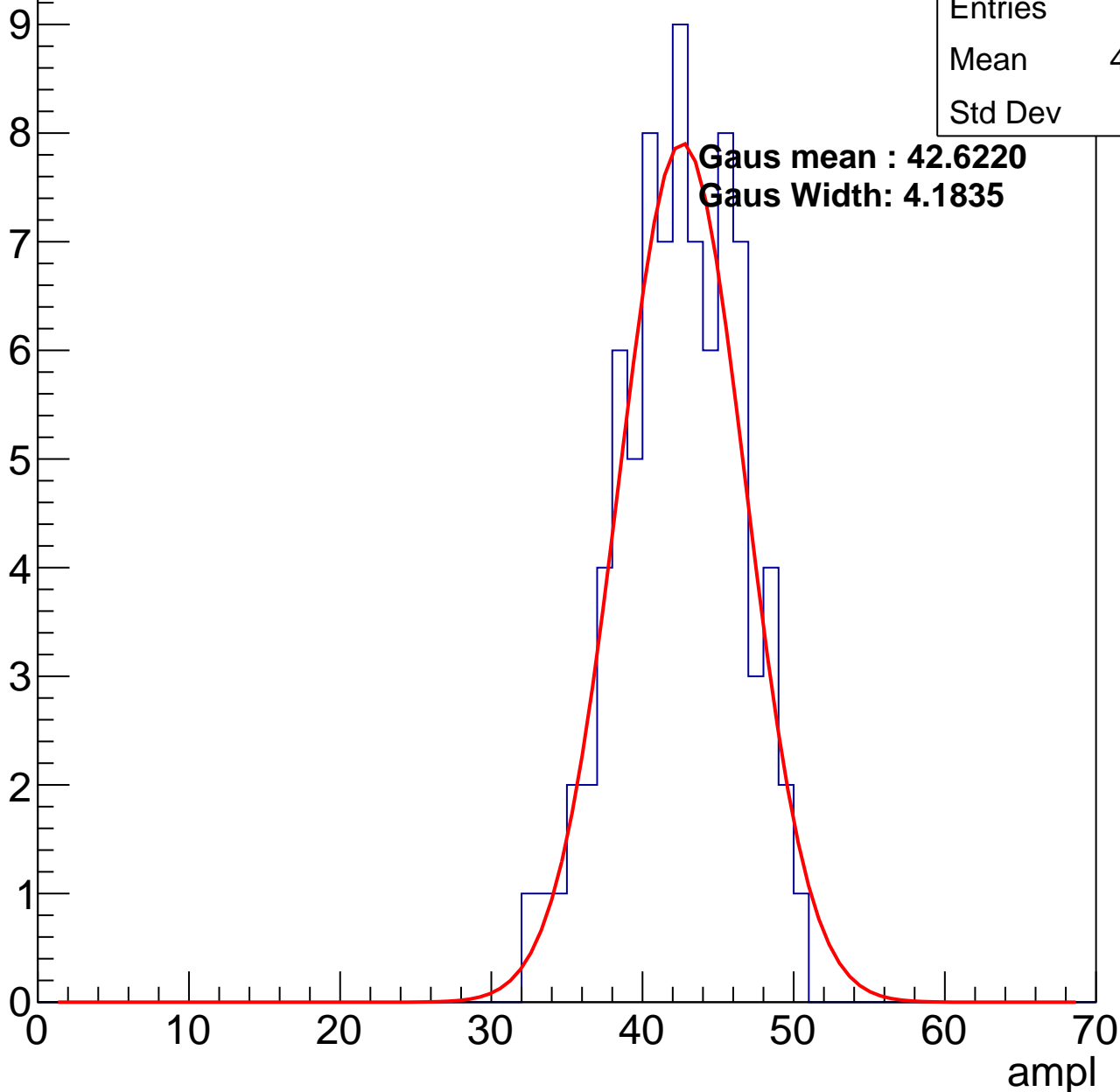
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	84
Mean	41.96
Std Dev	3.92

**Gaus mean : 42.6220**

**Gaus Width: 4.1835**

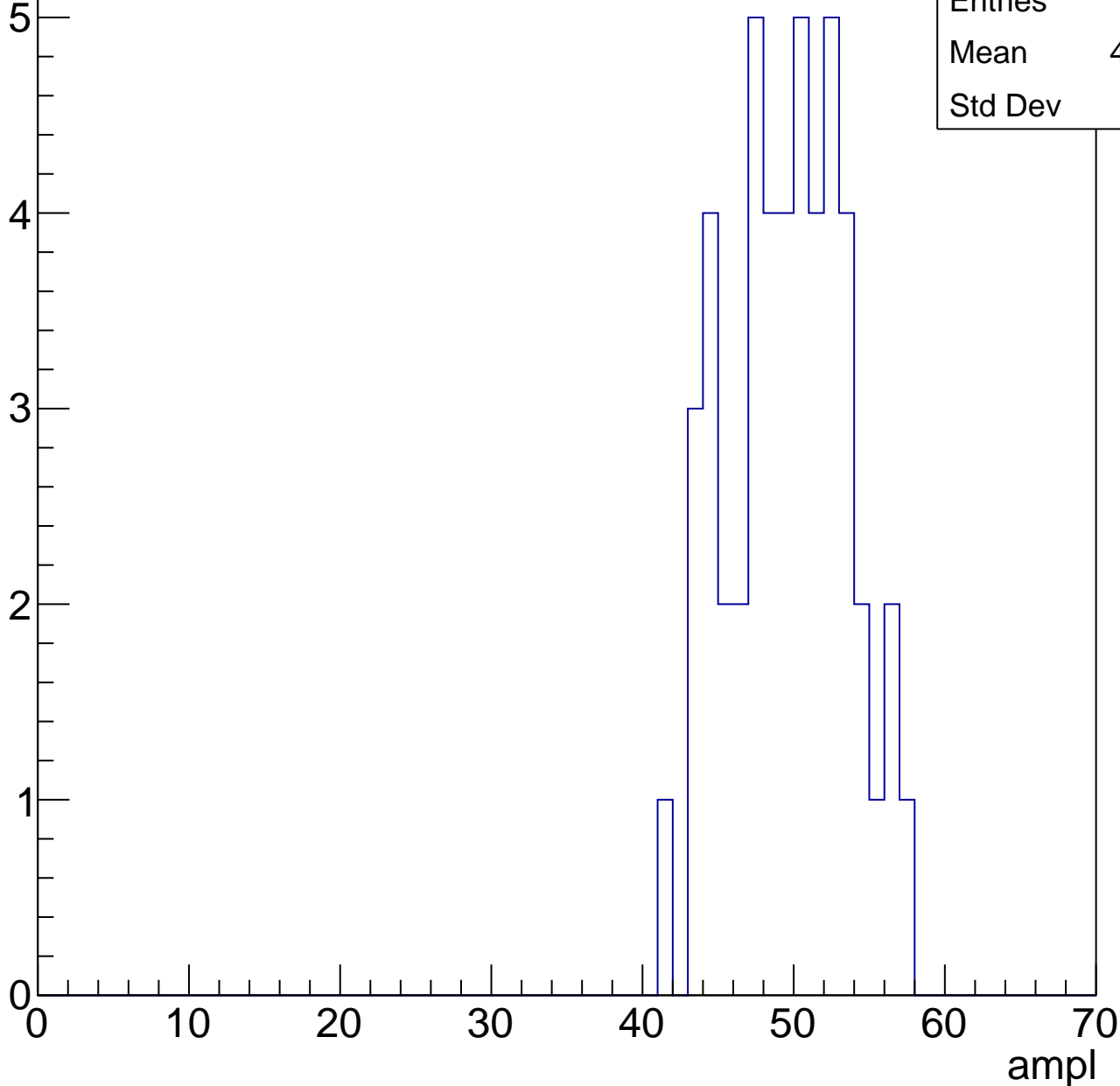


# B1L101S, U18-ch74, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	49
Mean	49.16
Std Dev	3.84

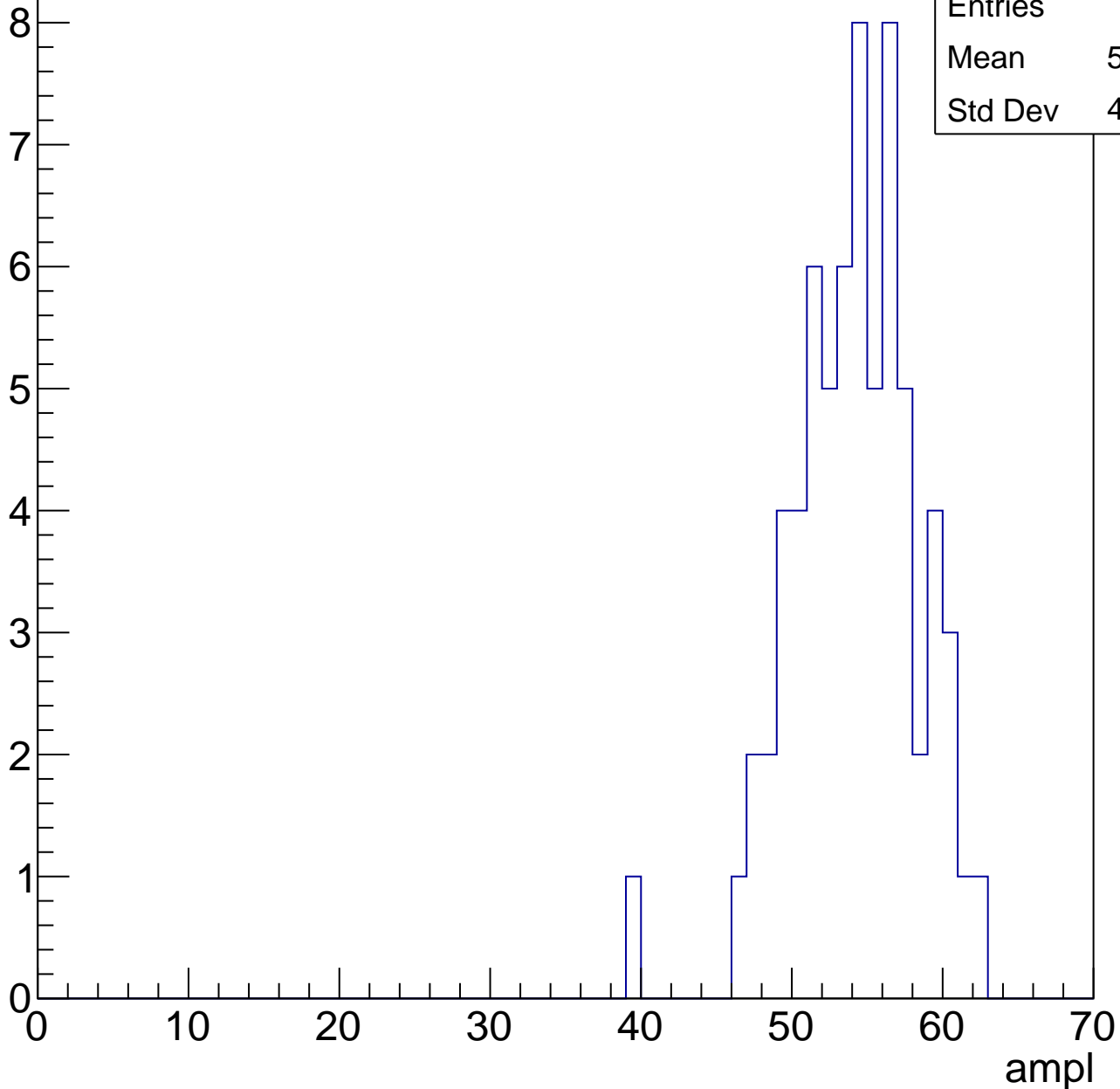


# B1L101S, U18-ch74, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	53.68
Std Dev	4.078

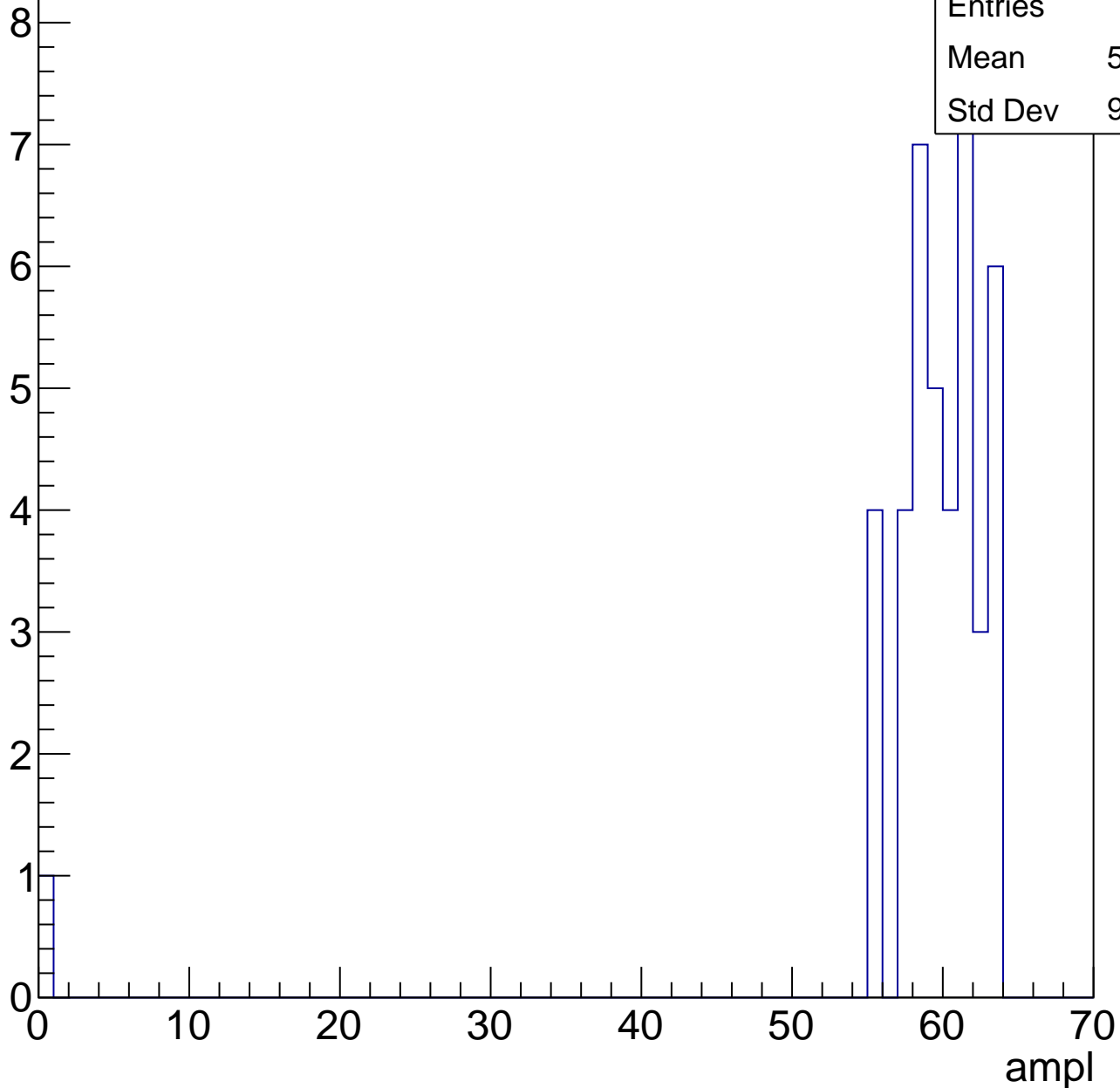


# B1L101S, U18-ch74, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	42
Mean	58.12
Std Dev	9.379

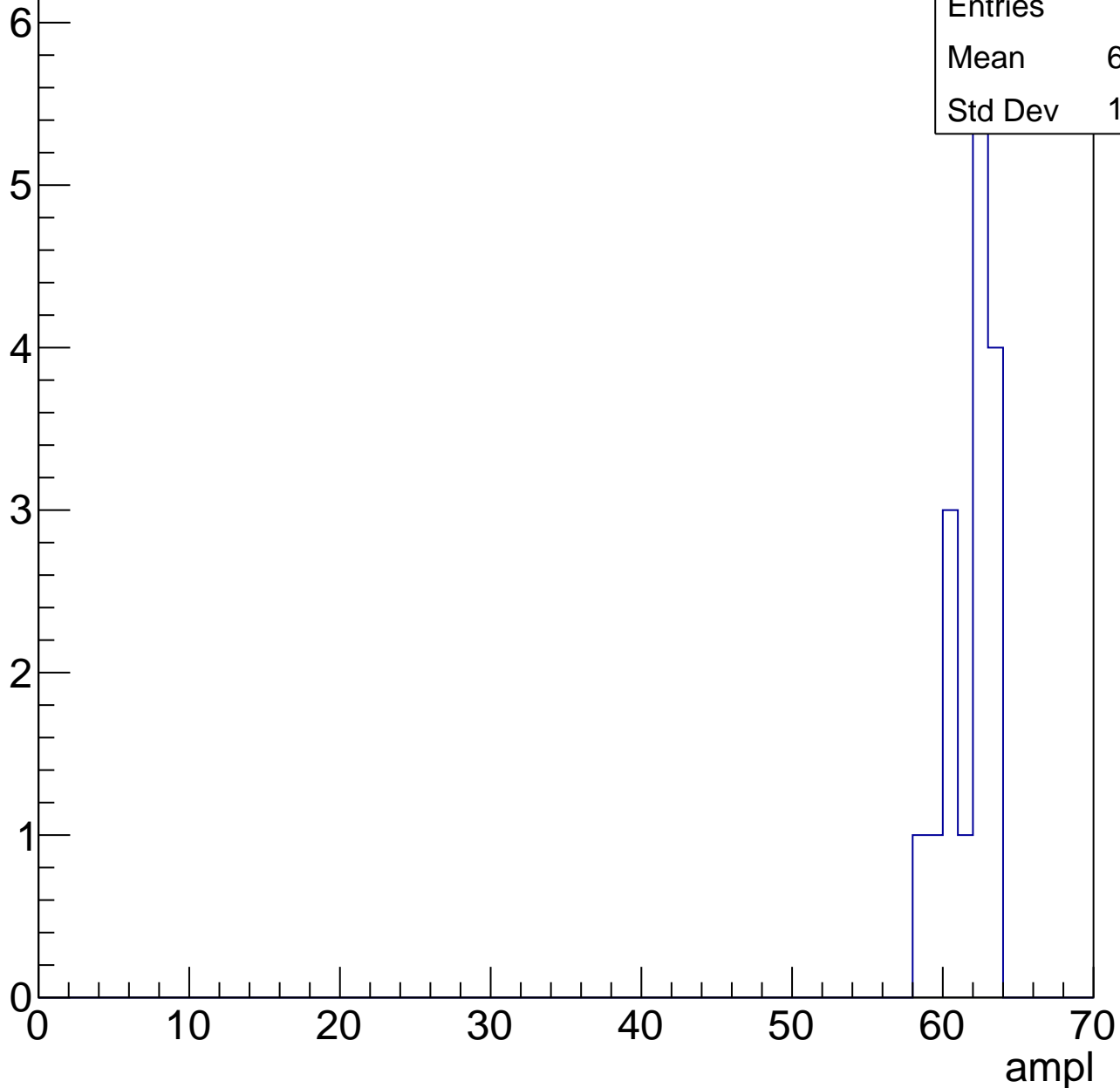


# B1L101S, U18-ch74, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	16
Mean	61.38
Std Dev	1.495





# B1L101S, U18-ch74, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U18-ch75, adc0

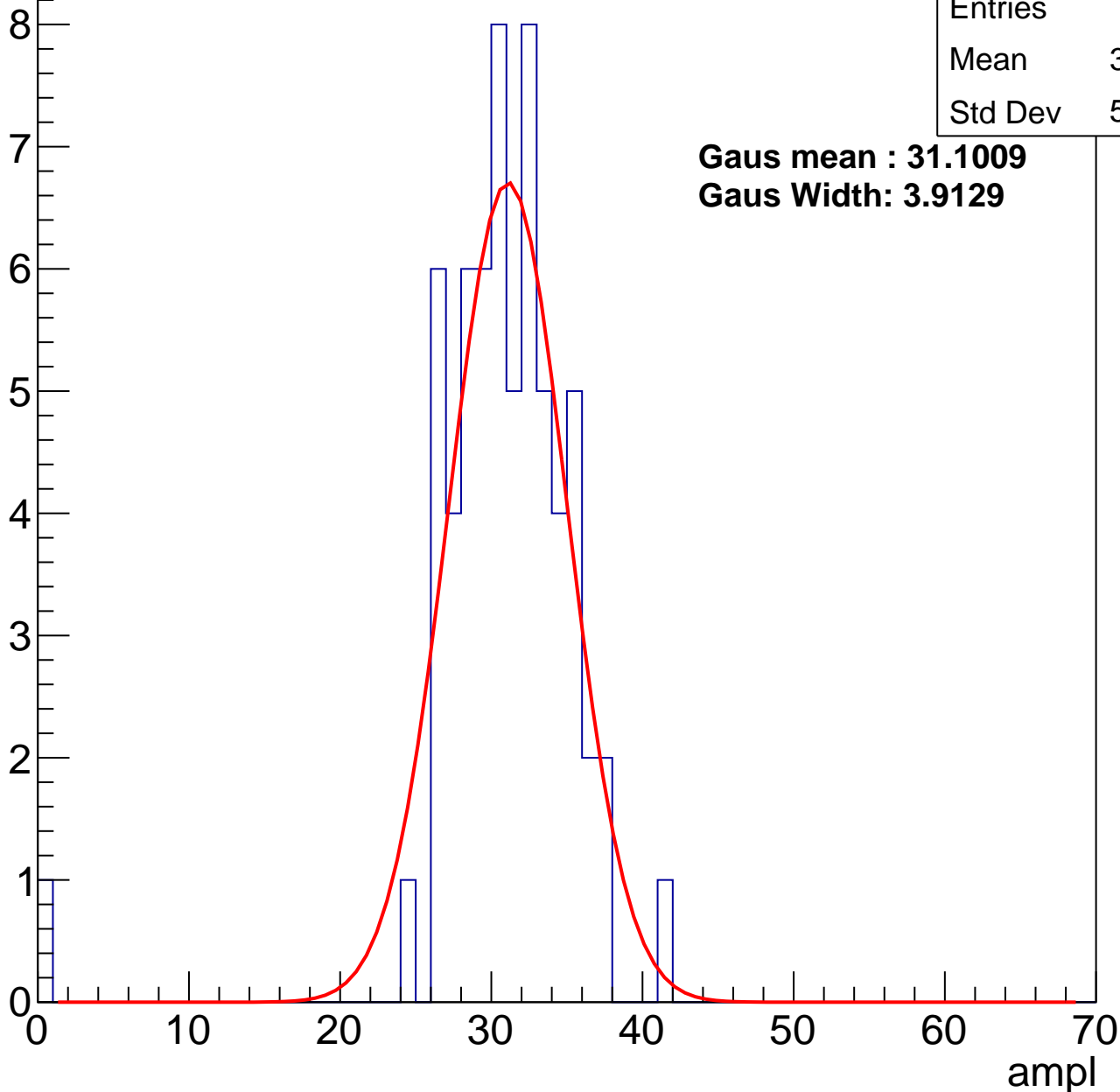
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	30.38
Std Dev	5.079

**Gaus mean : 31.1009**

**Gaus Width: 3.9129**



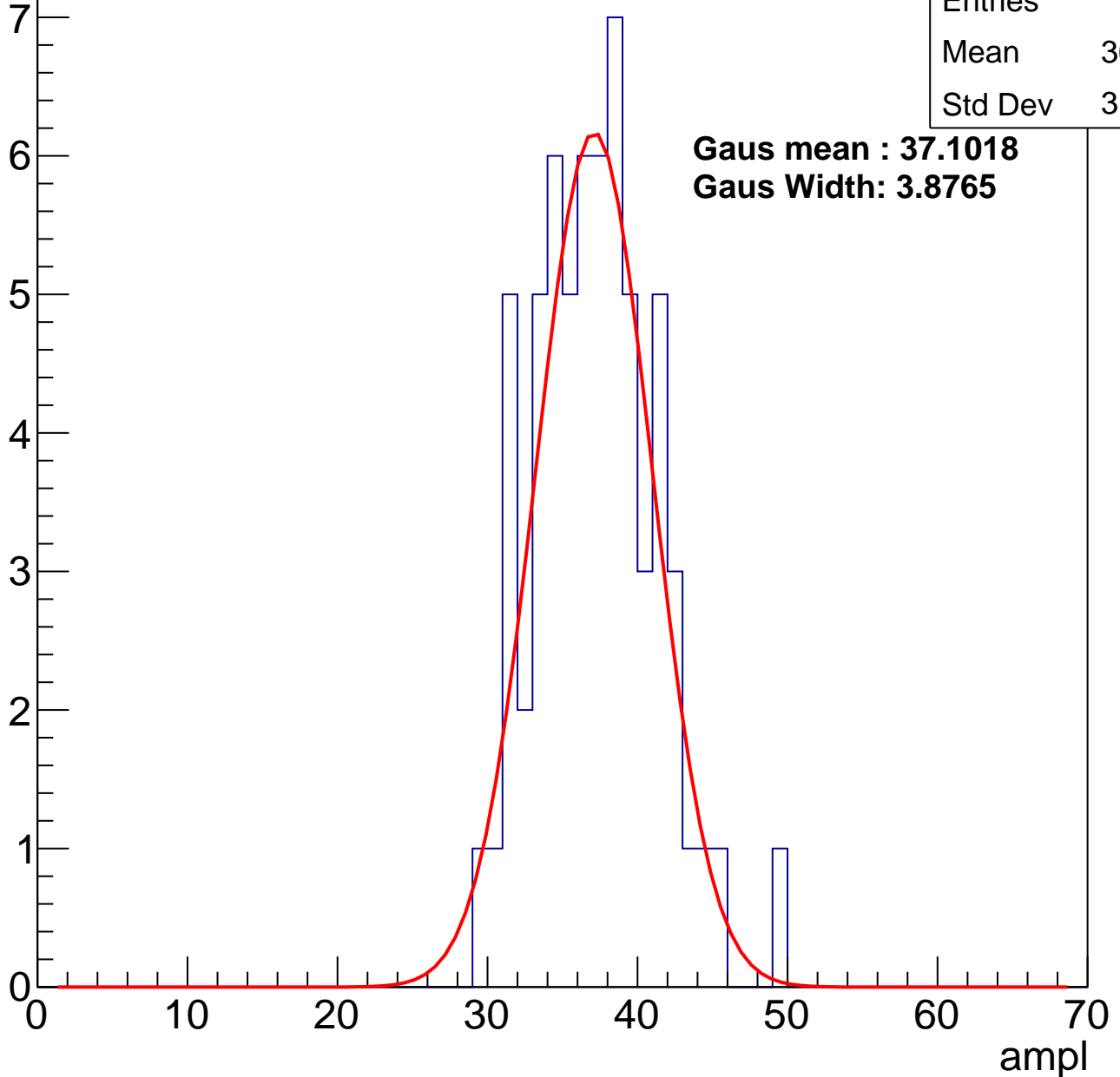
# B1L101S, U18-ch75, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	36.77
Std Dev	3.956

**Gaus mean : 37.1018**  
**Gaus Width: 3.8765**



# B1L101S, U18-ch75, adc2

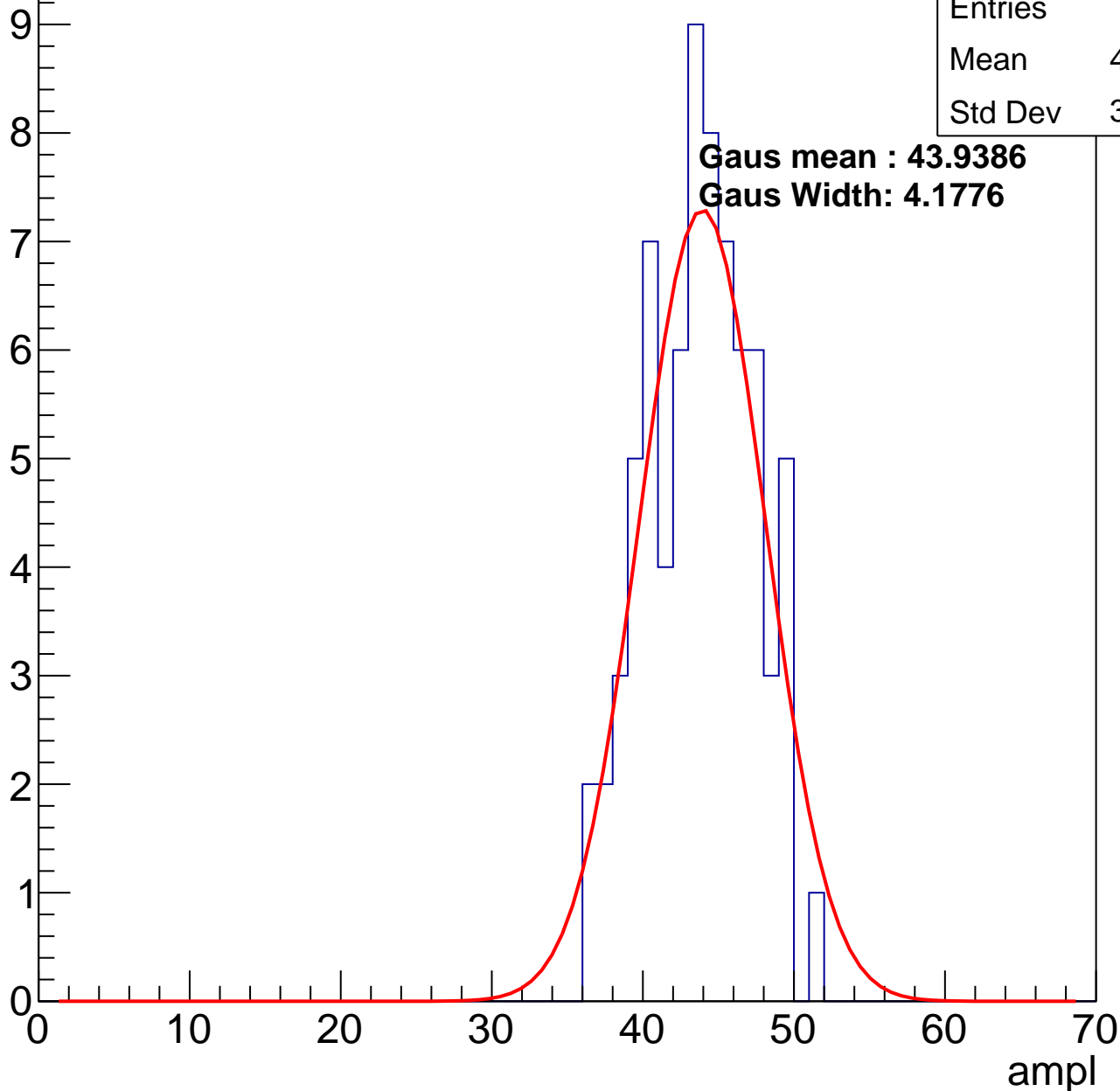
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	43.28
Std Dev	3.505

**Gaus mean : 43.9386**

**Gaus Width: 4.1776**

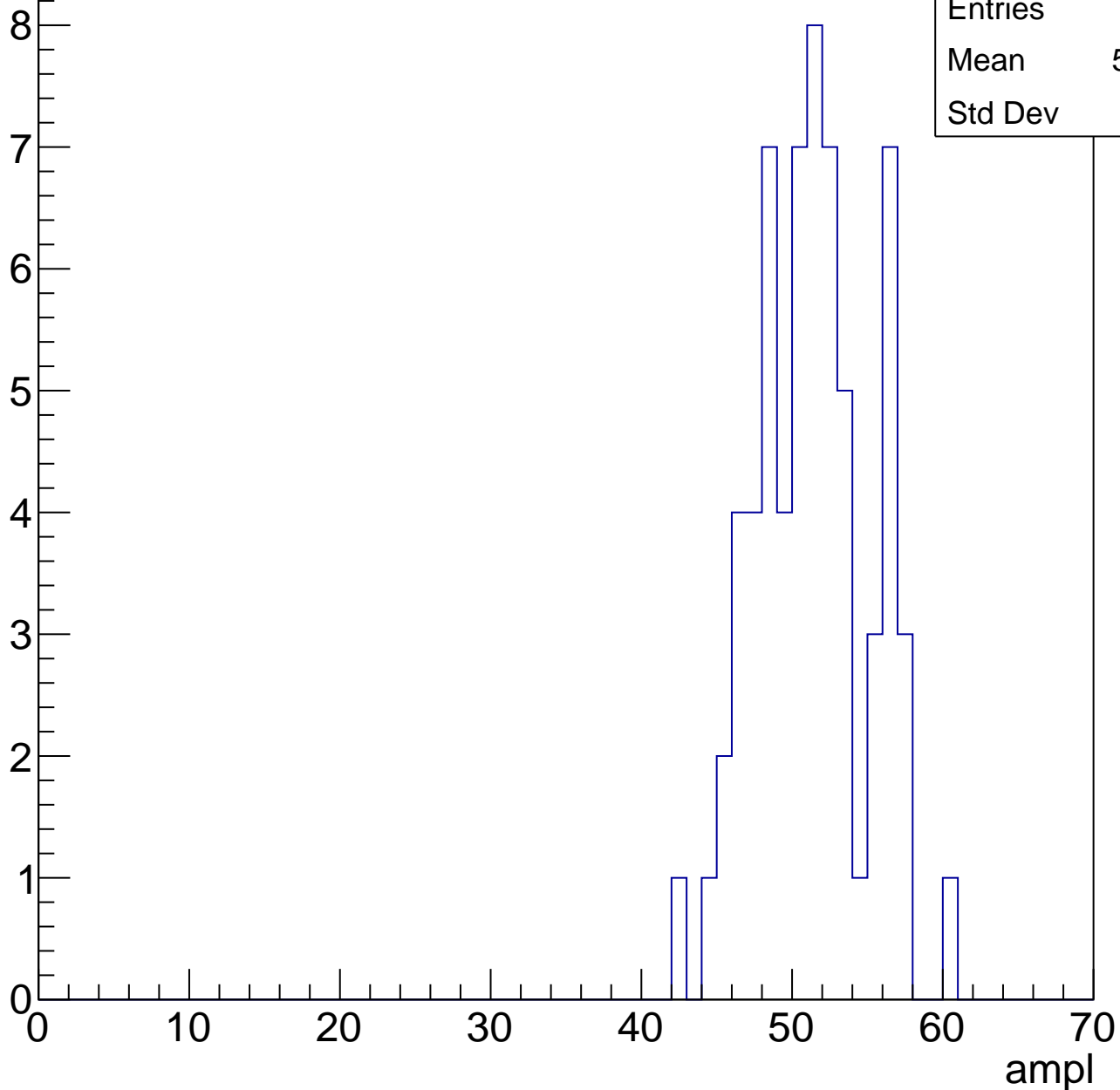


# B1L101S, U18-ch75, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	50.91
Std Dev	3.72

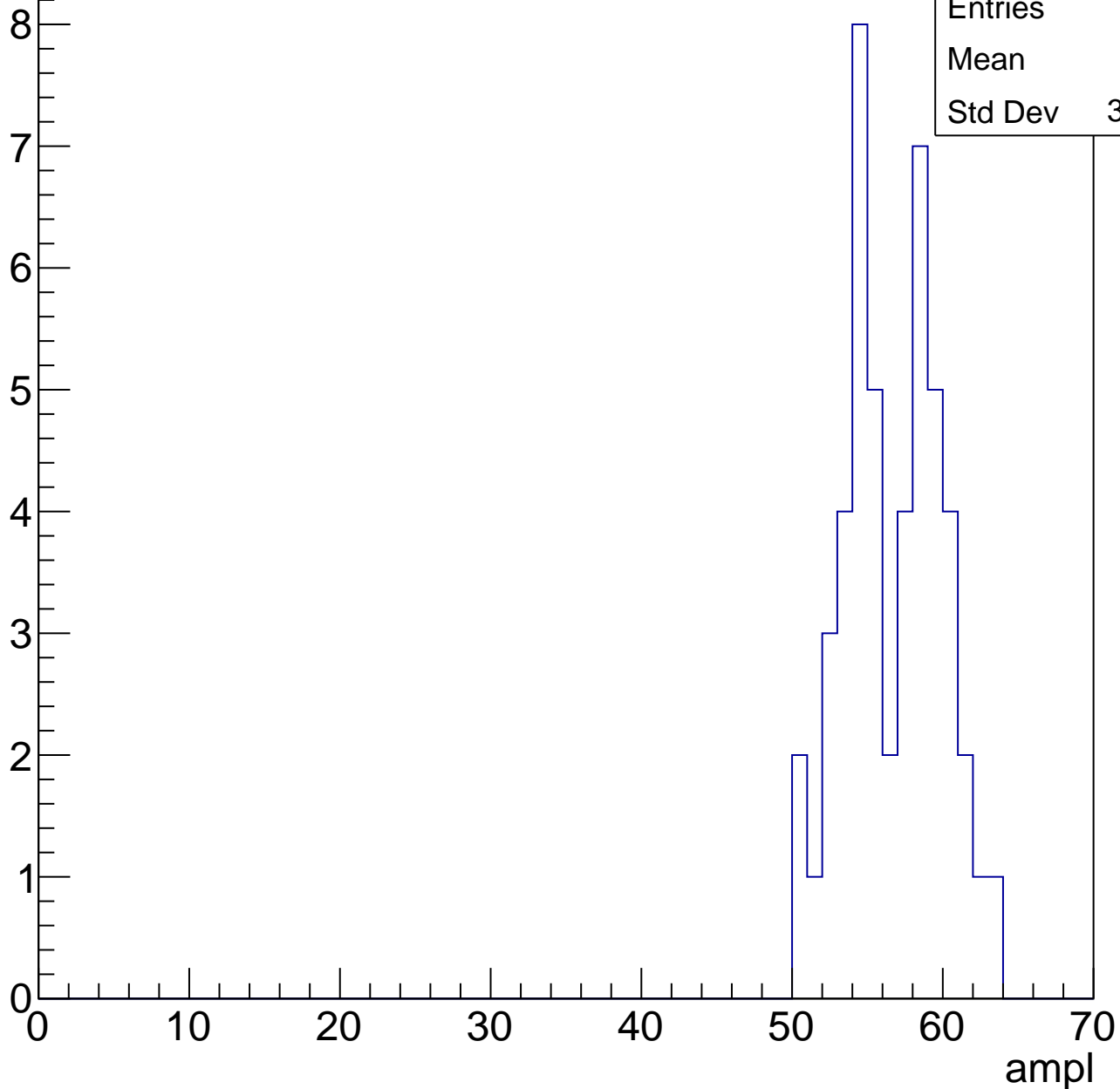


# B1L101S, U18-ch75, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	49
Mean	56.2
Std Dev	3.169

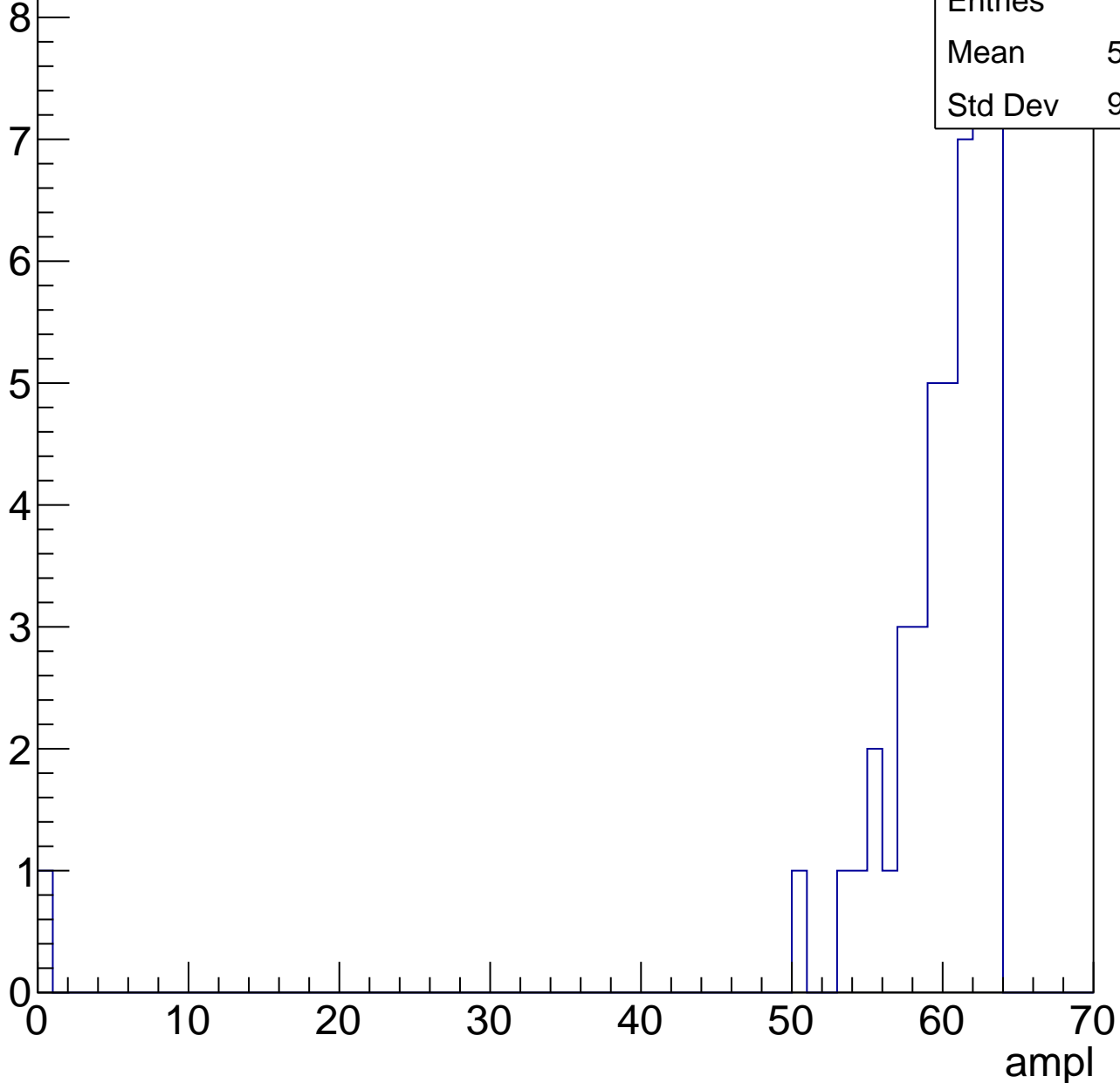


# B1L101S, U18-ch75, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	46
Mean	58.48
Std Dev	9.207



# B1L101S, U18-ch75, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

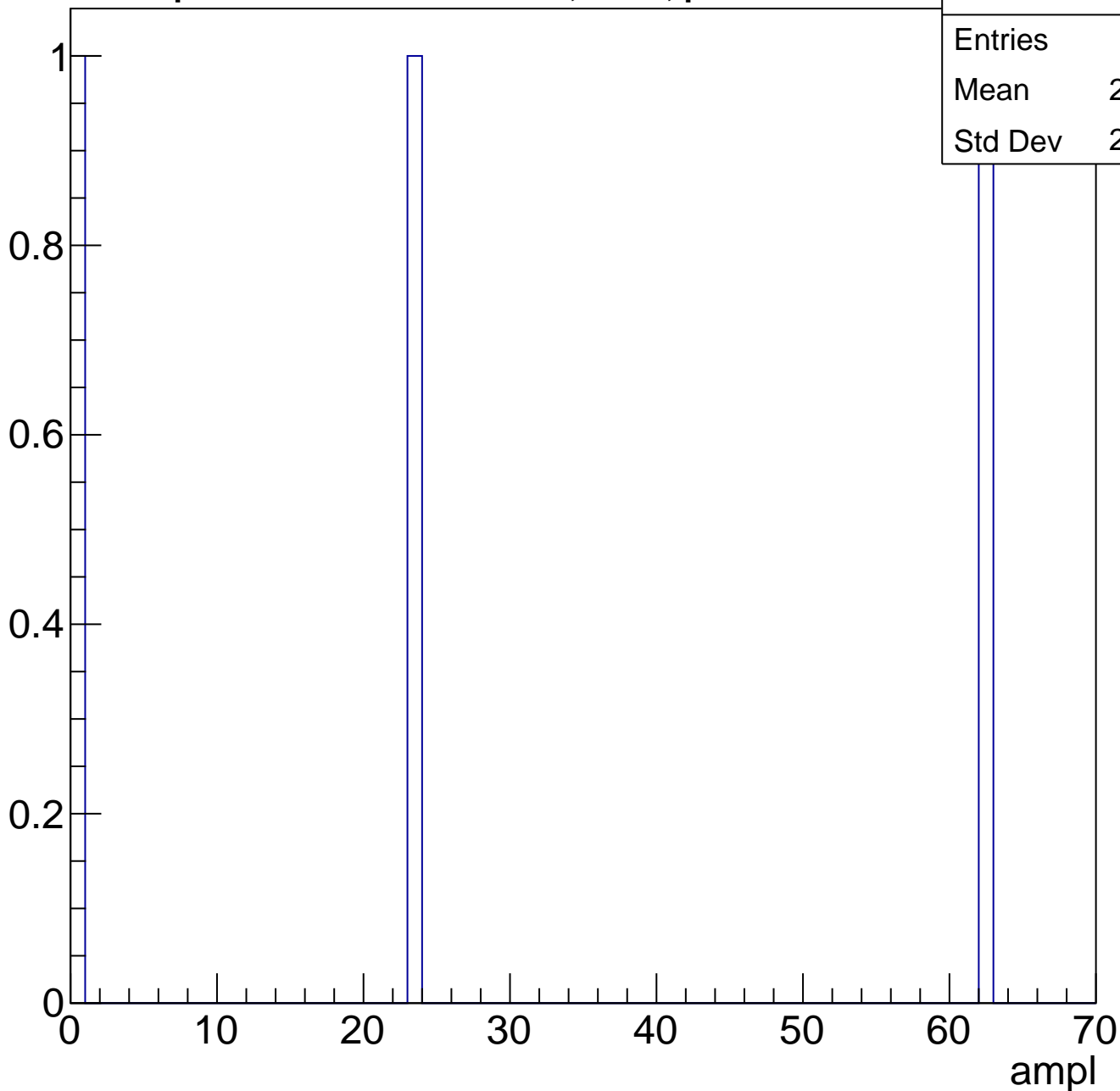




# B1L101S, U18-ch75, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	28.33
Std Dev	25.59

# B1L101S, U18-ch76, adc0

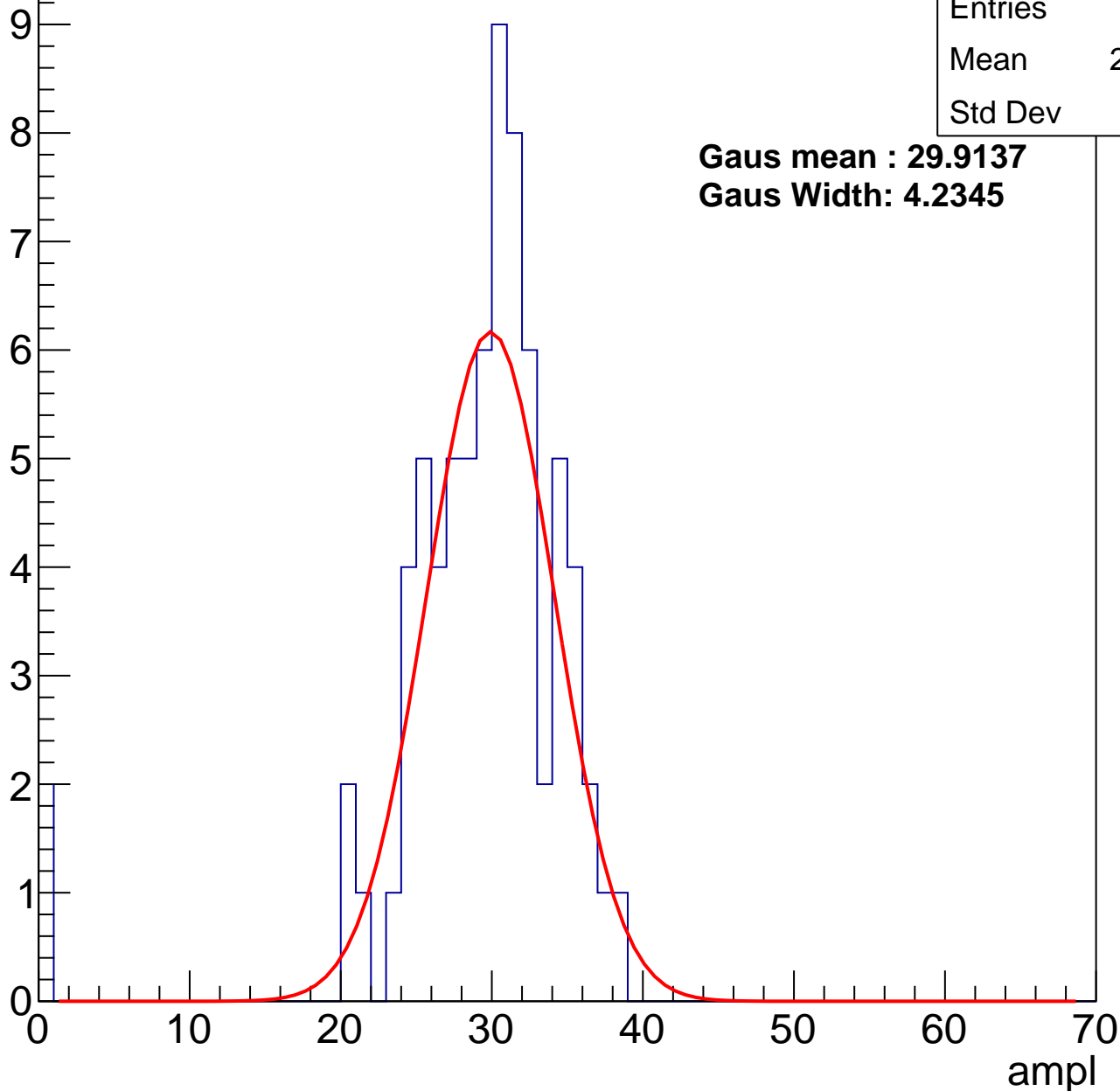
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	28.64
Std Dev	6.21

**Gaus mean : 29.9137**

**Gaus Width: 4.2345**



# B1L101S, U18-ch76, adc1

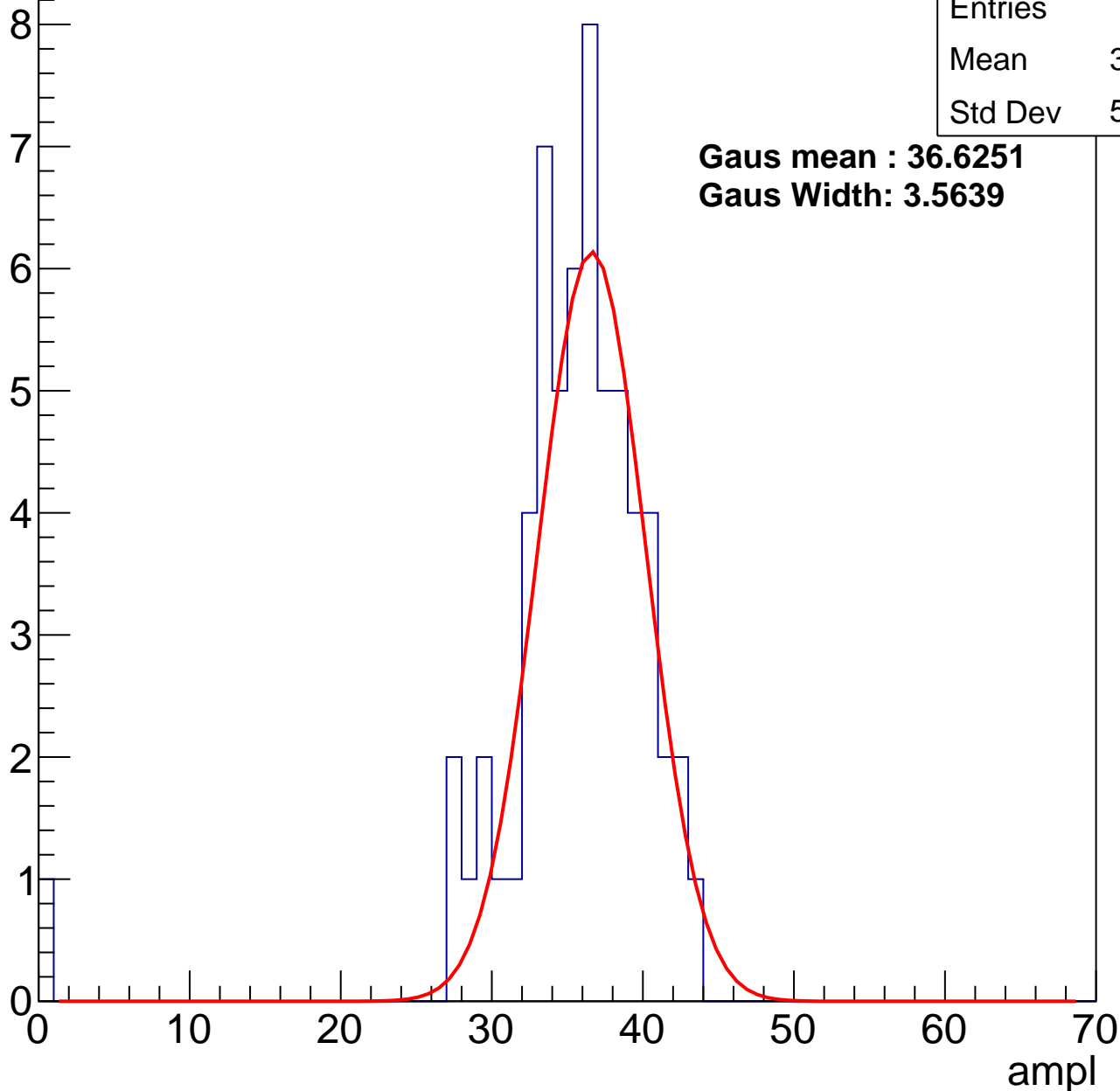
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	34.89
Std Dev	5.803

**Gaus mean : 36.6251**

**Gaus Width: 3.5639**



# B1L101S, U18-ch76, adc2

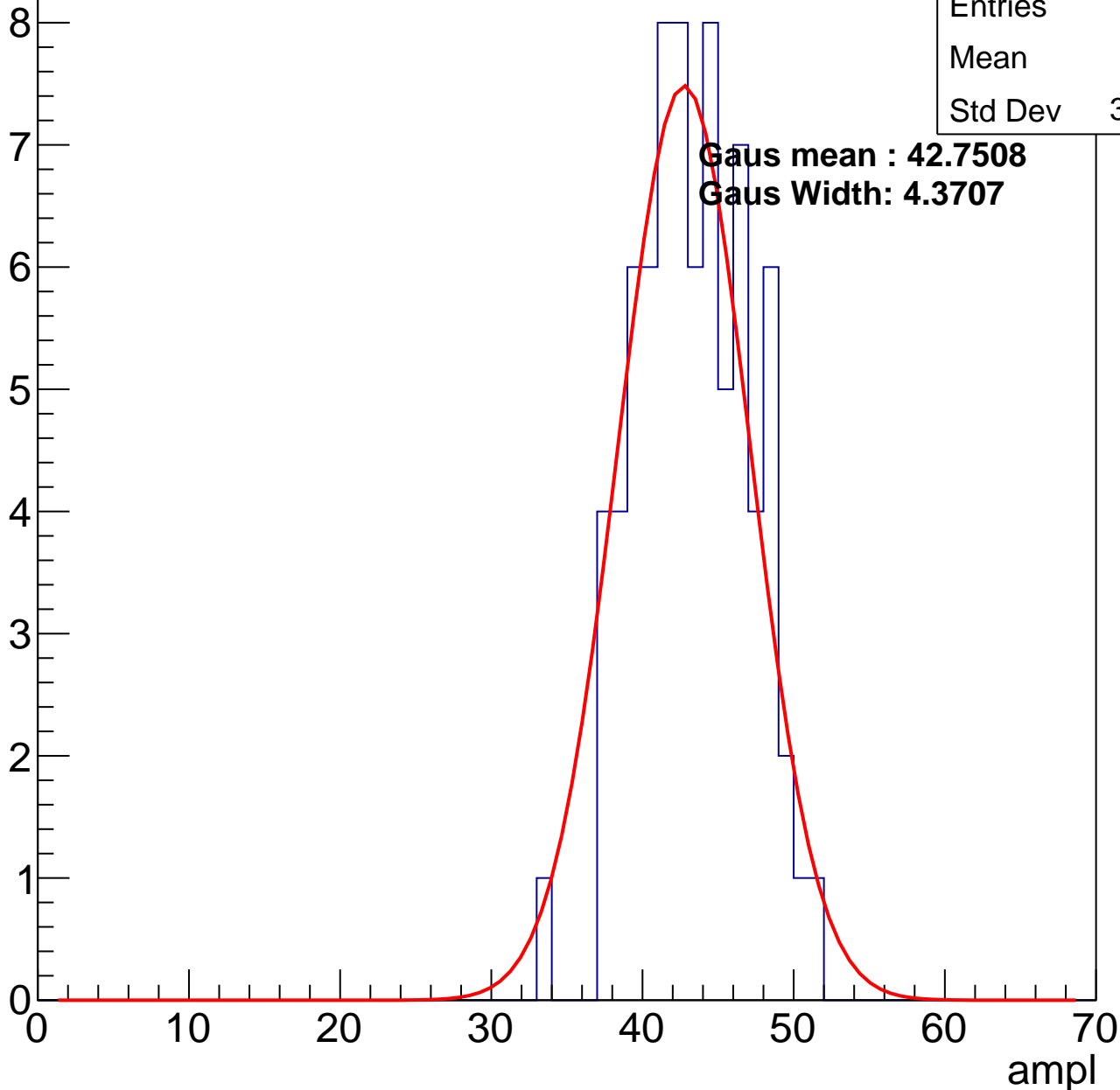
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	42.9
Std Dev	3.645

**Gaus mean : 42.7508**

**Gaus Width: 4.3707**

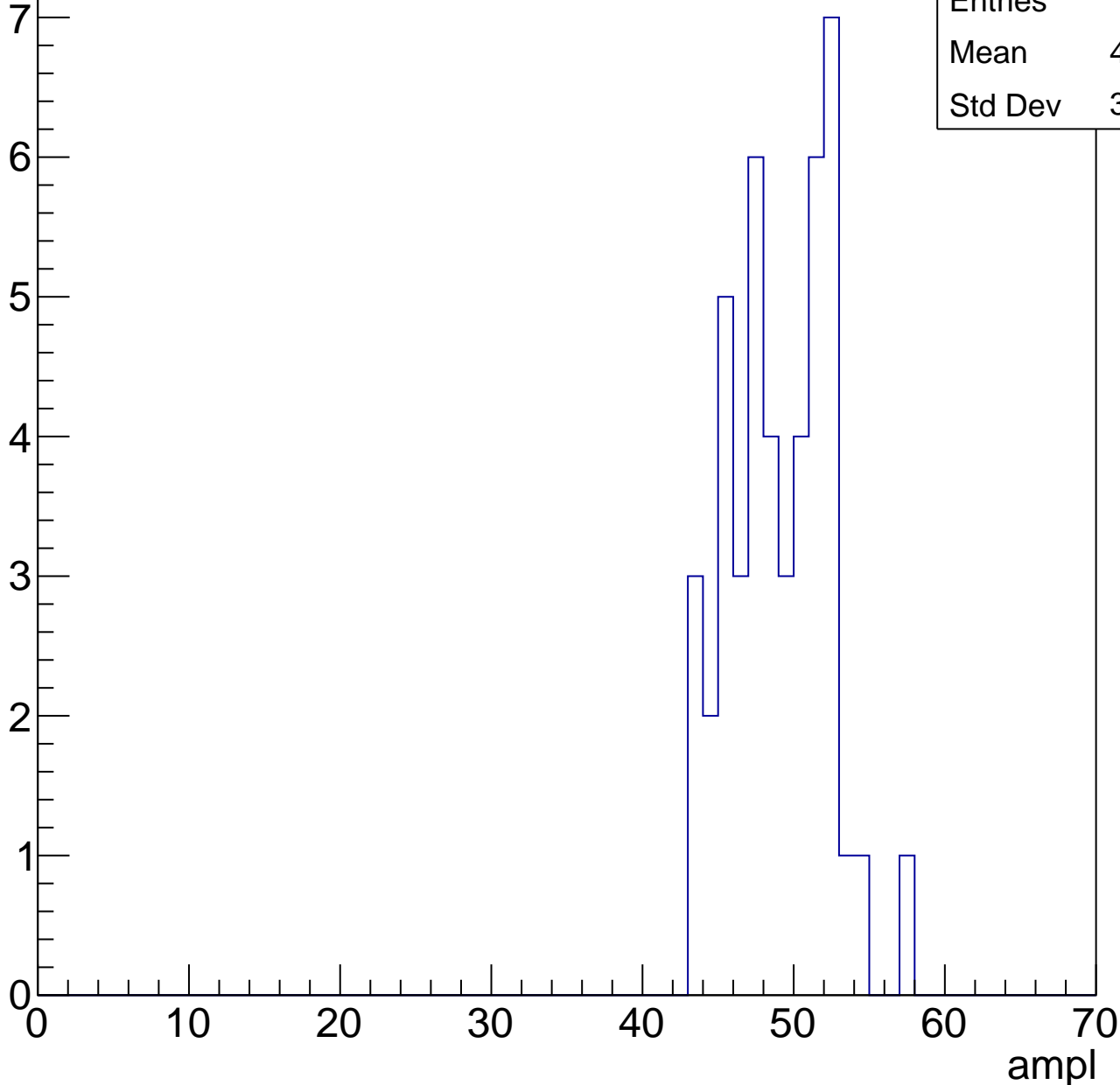


# B1L101S, U18-ch76, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

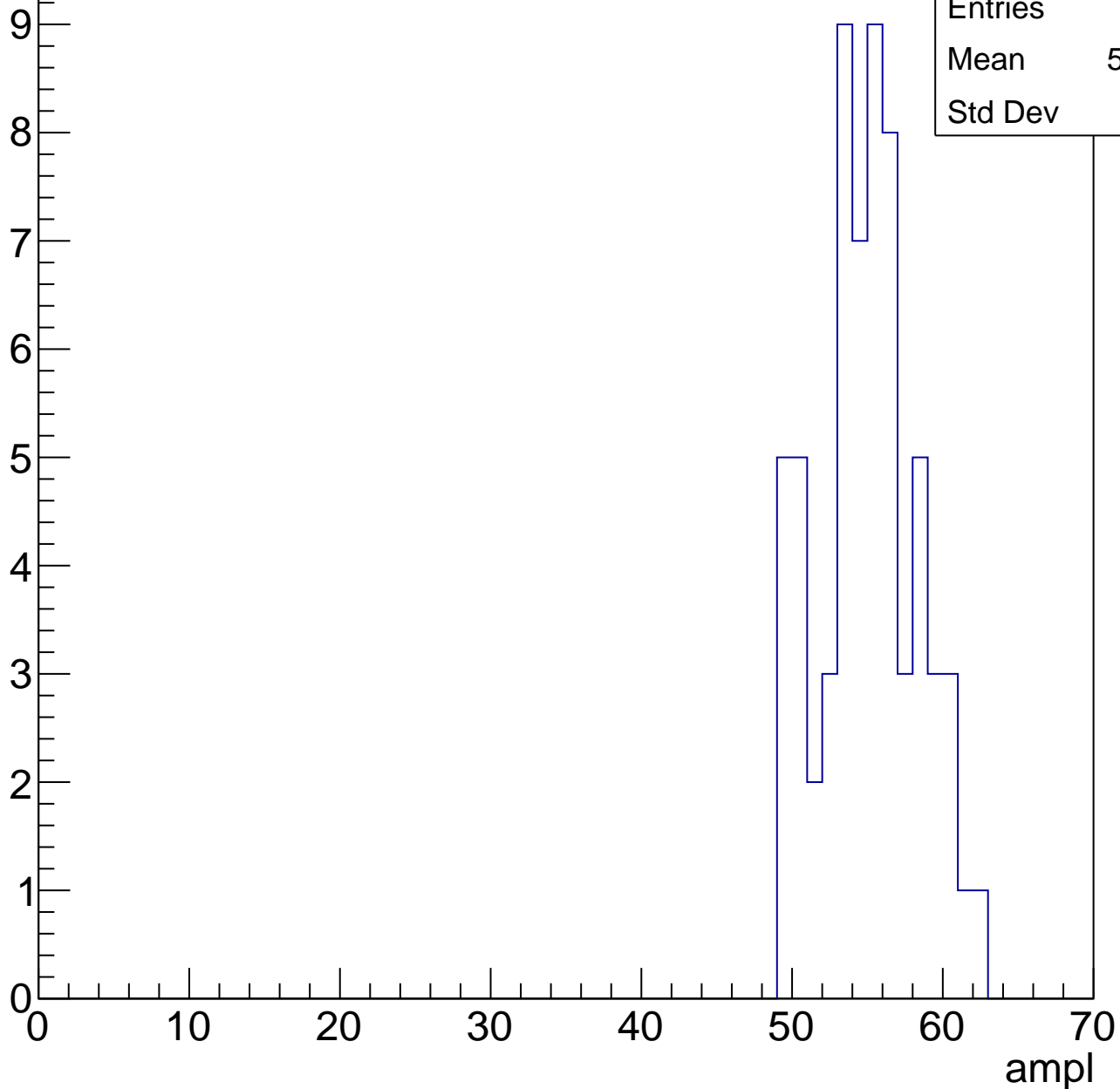
Entries	46
Mean	48.59
Std Dev	3.234



# B1L101S, U18-ch76, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



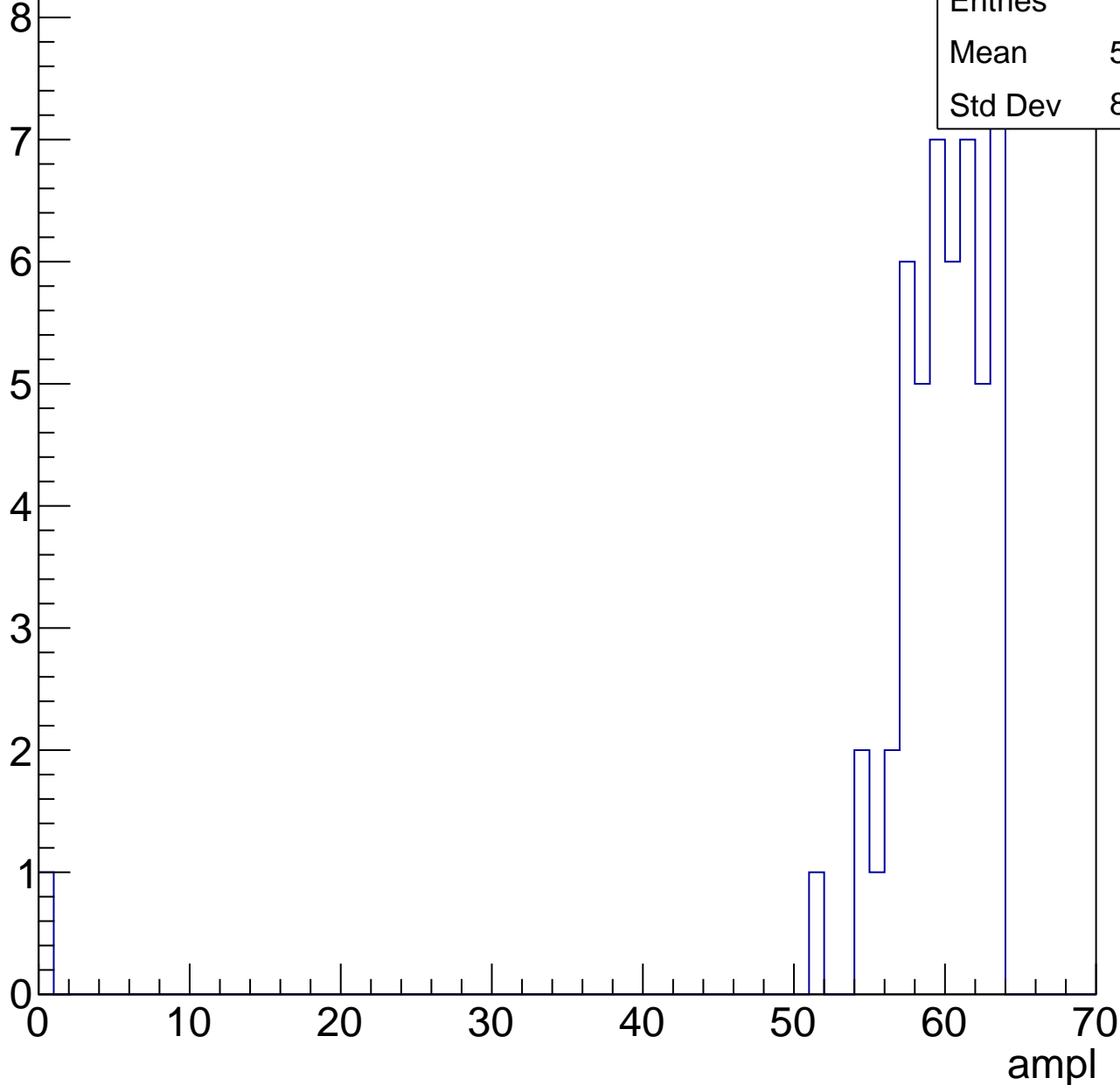
Entries	64
Mean	54.56
Std Dev	3.23

# B1L101S, U18-ch76, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

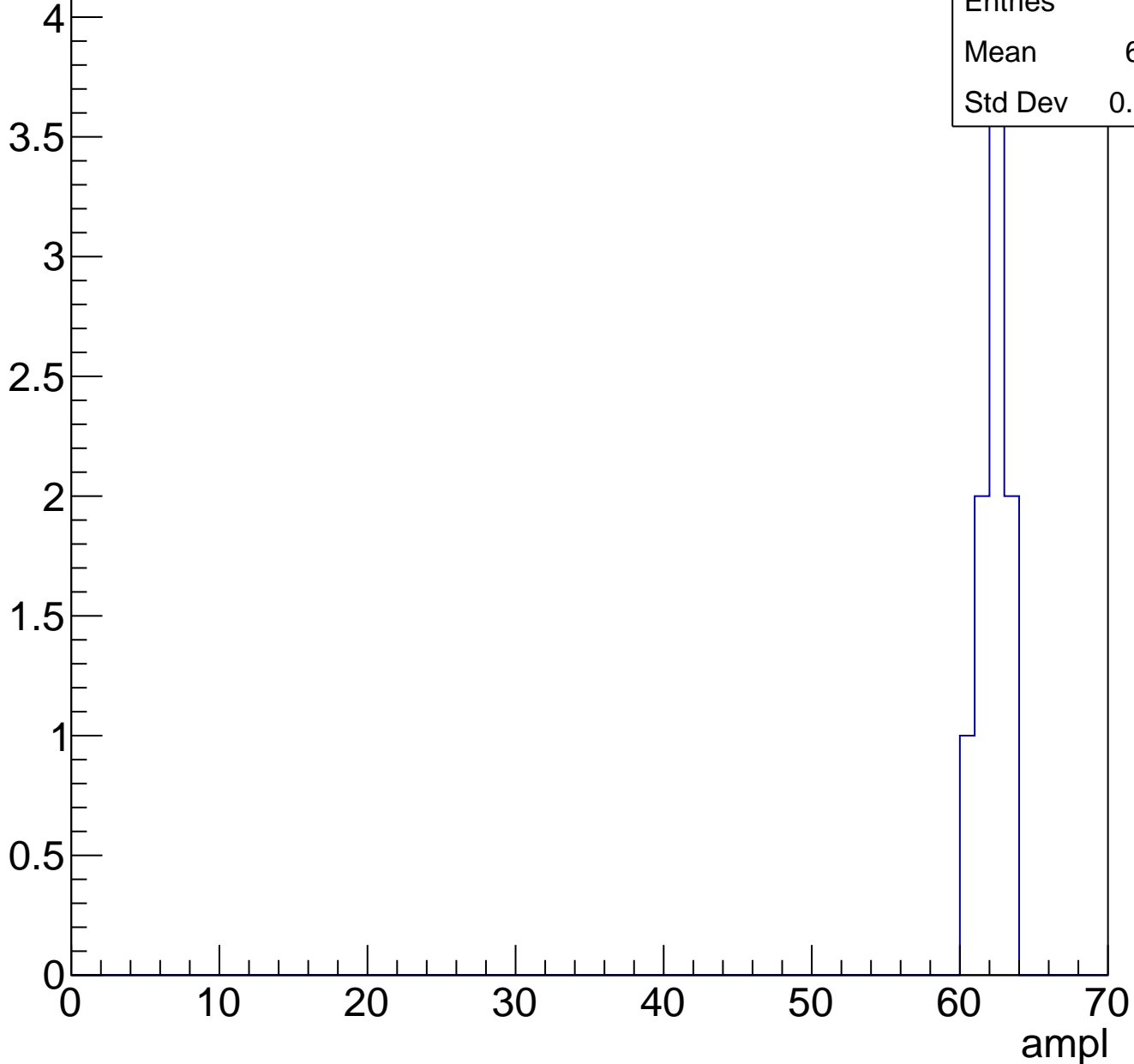
Entries	51
Mean	58.27
Std Dev	8.675



# B1L101S, U18-ch76, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch76, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch77, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	98
Mean	29.47
Std Dev	5.553

**Gaus mean : 30.9486**

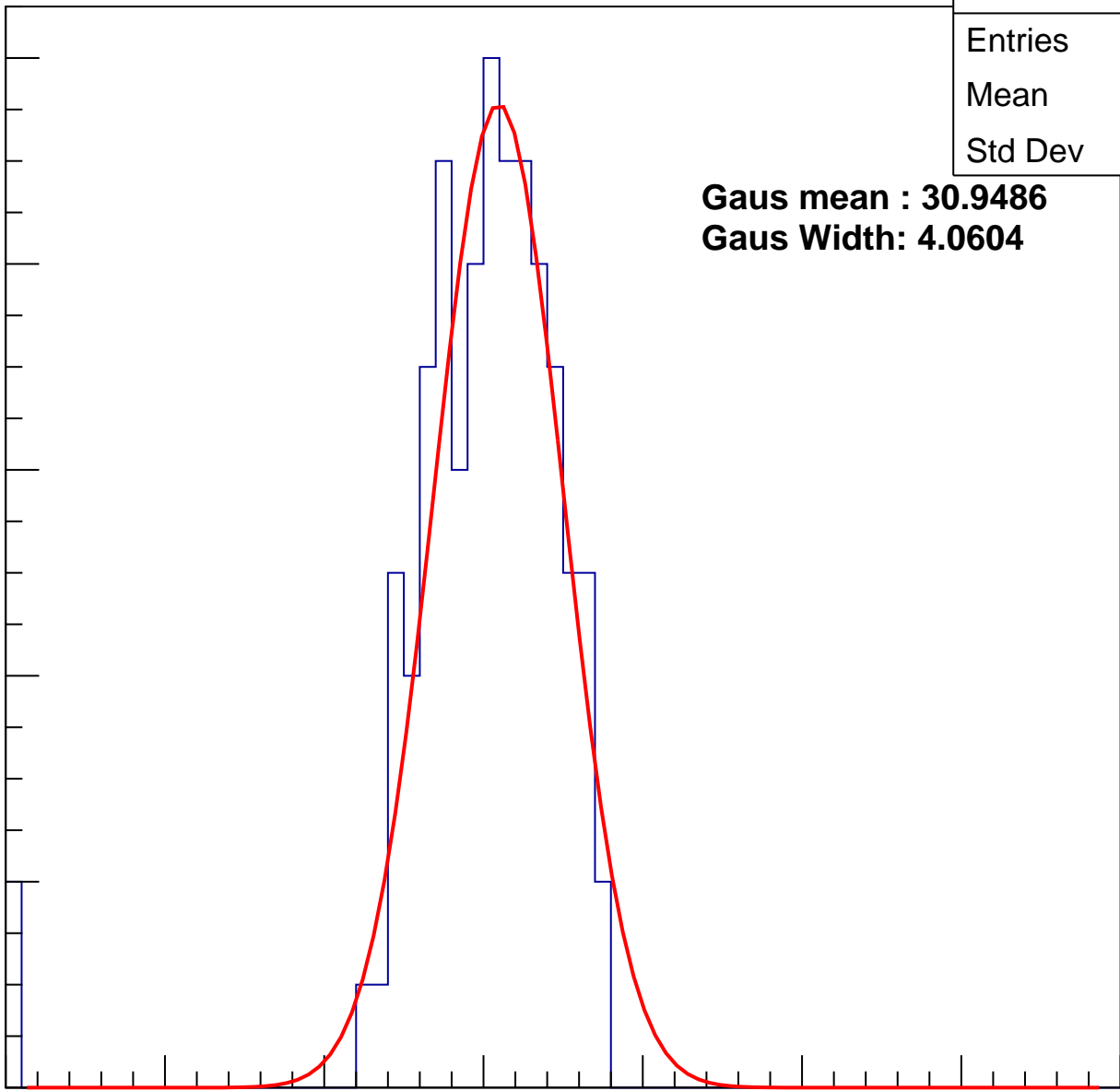
**Gaus Width: 4.0604**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U18-ch77, adc1

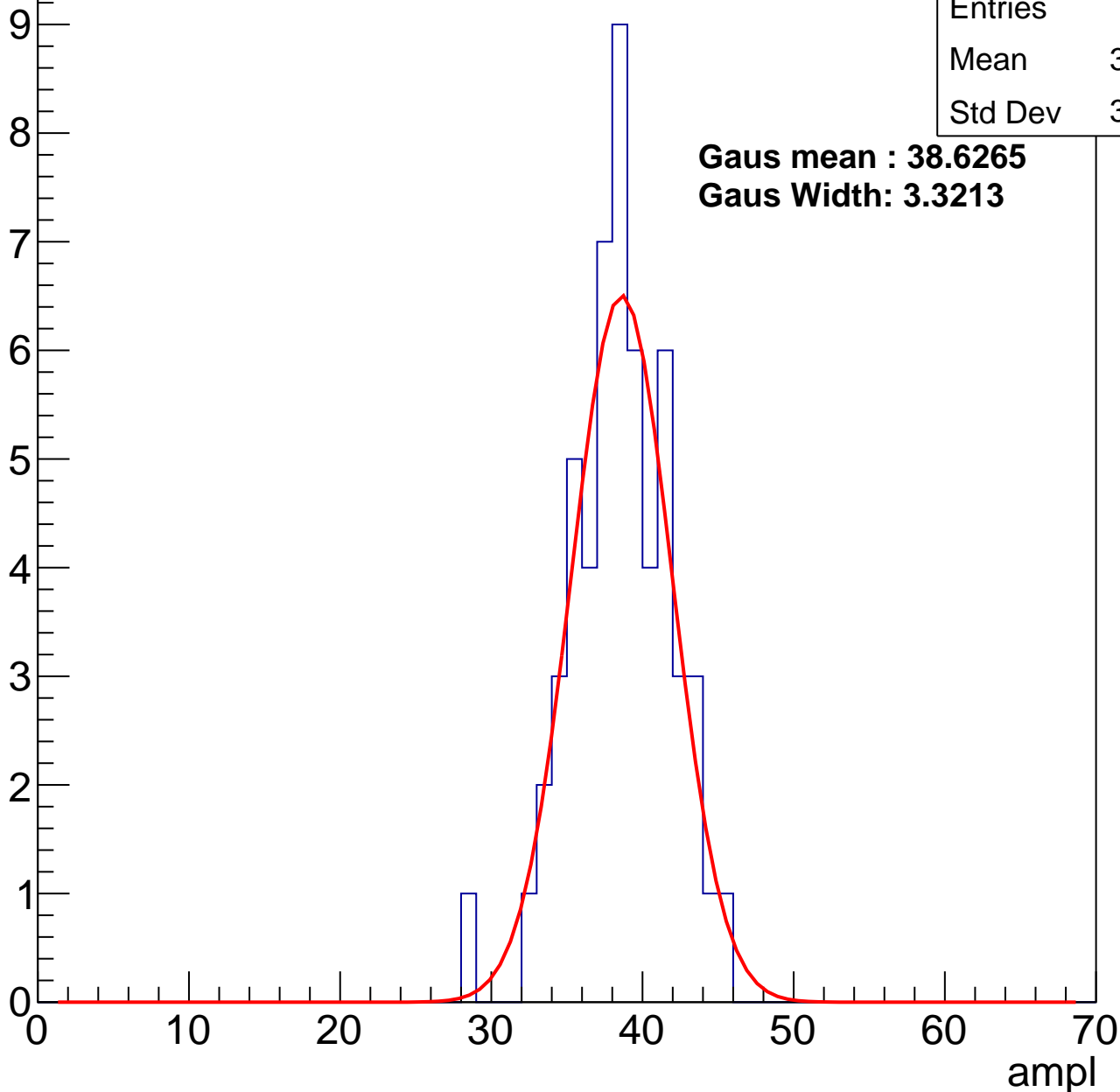
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	38.07
Std Dev	3.234

**Gaus mean : 38.6265**

**Gaus Width: 3.3213**



# B1L101S, U18-ch77, adc2

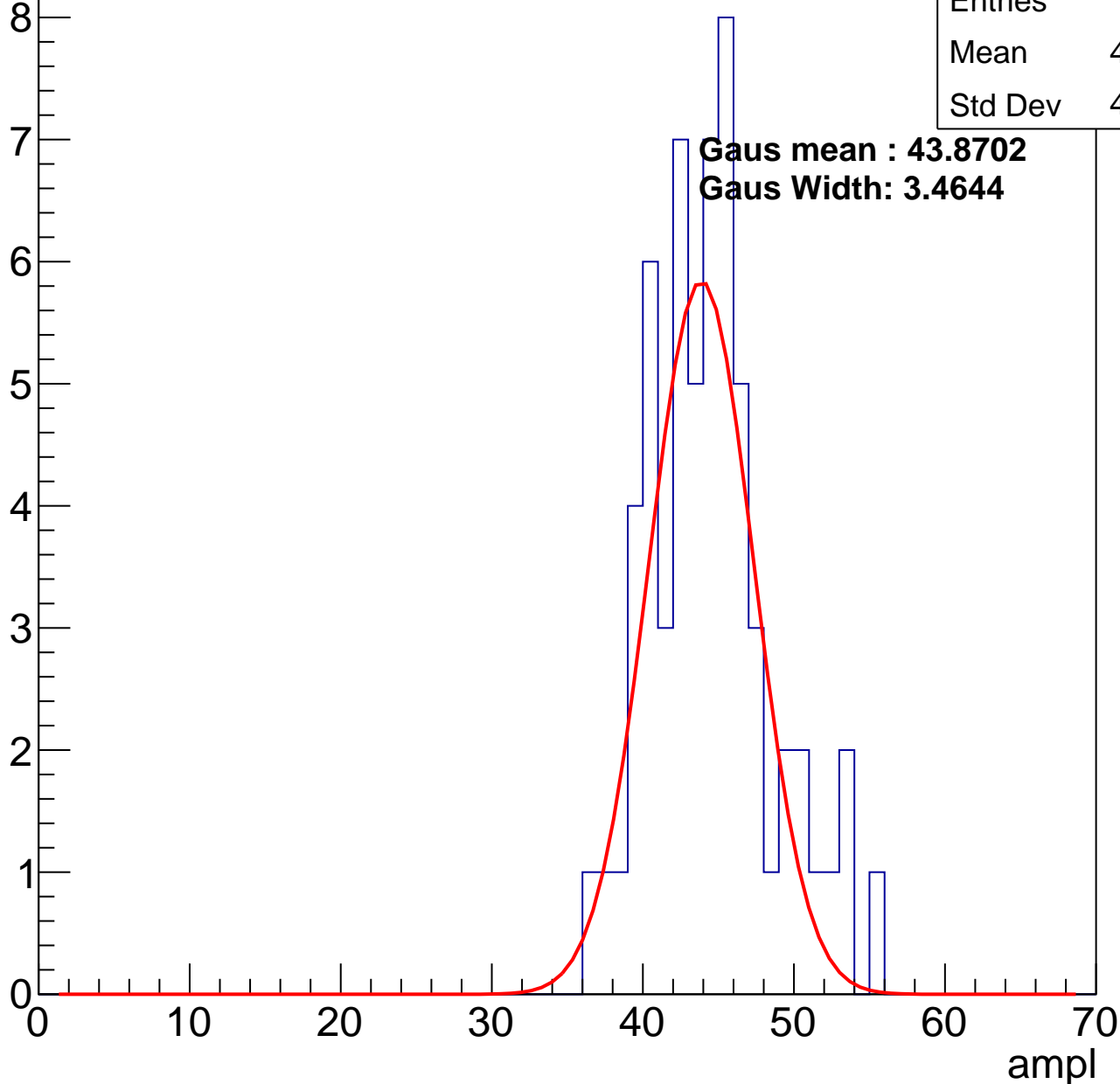
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	44.07
Std Dev	4.036

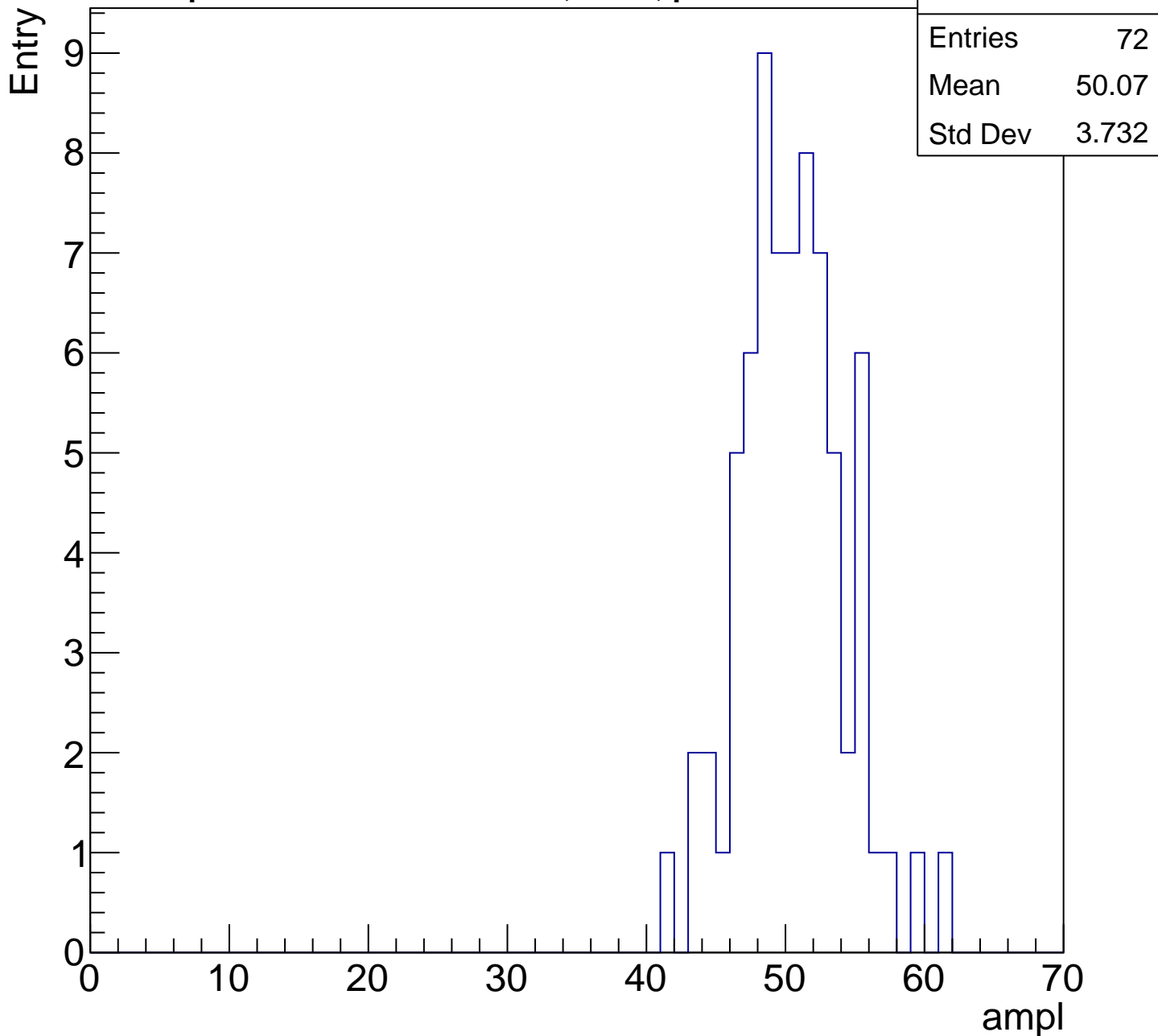
**Gaus mean : 43.8702**

**Gaus Width: 3.4644**



# B1L101S, U18-ch77, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

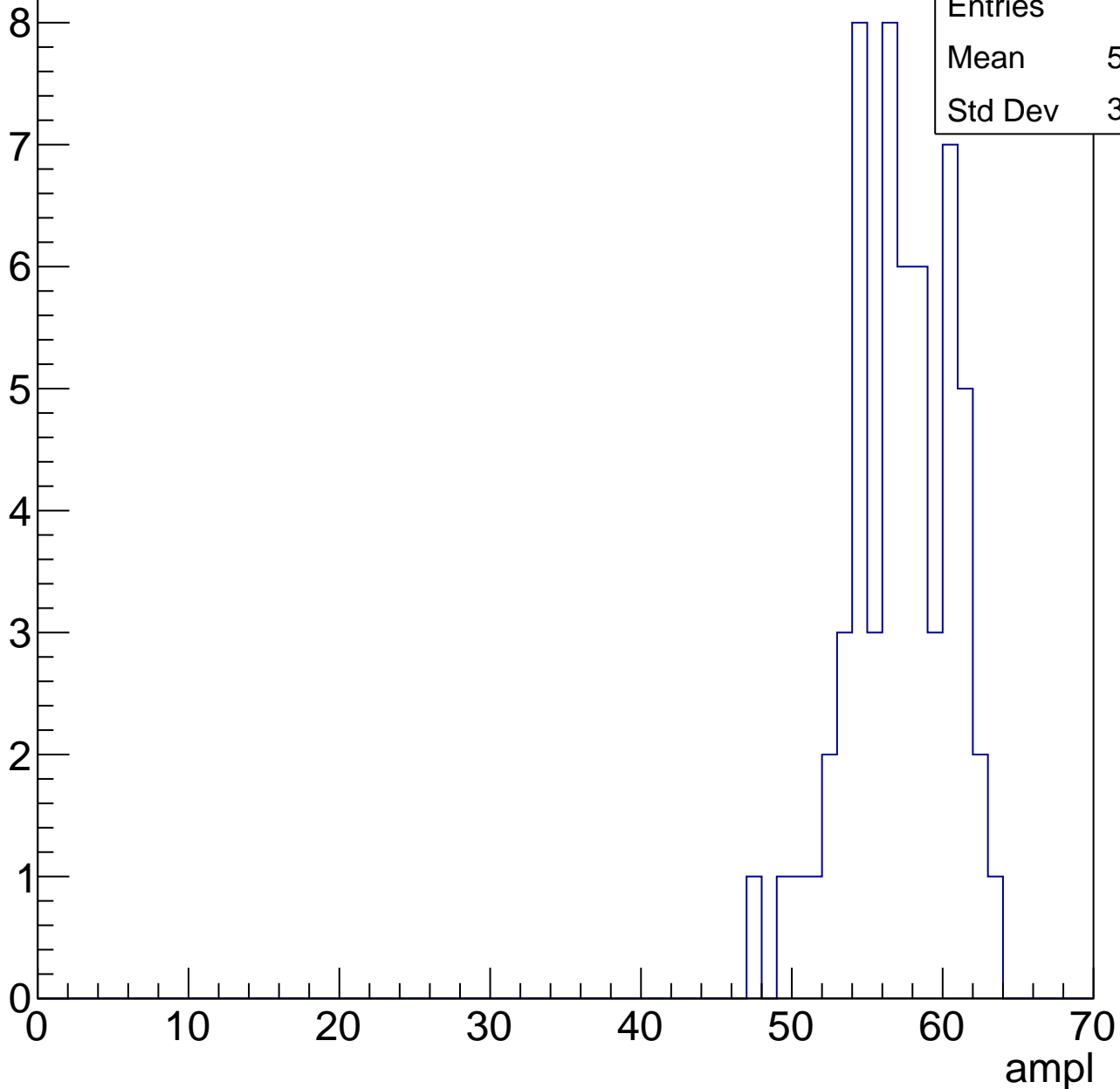


# B1L101S, U18-ch77, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	56.62
Std Dev	3.418

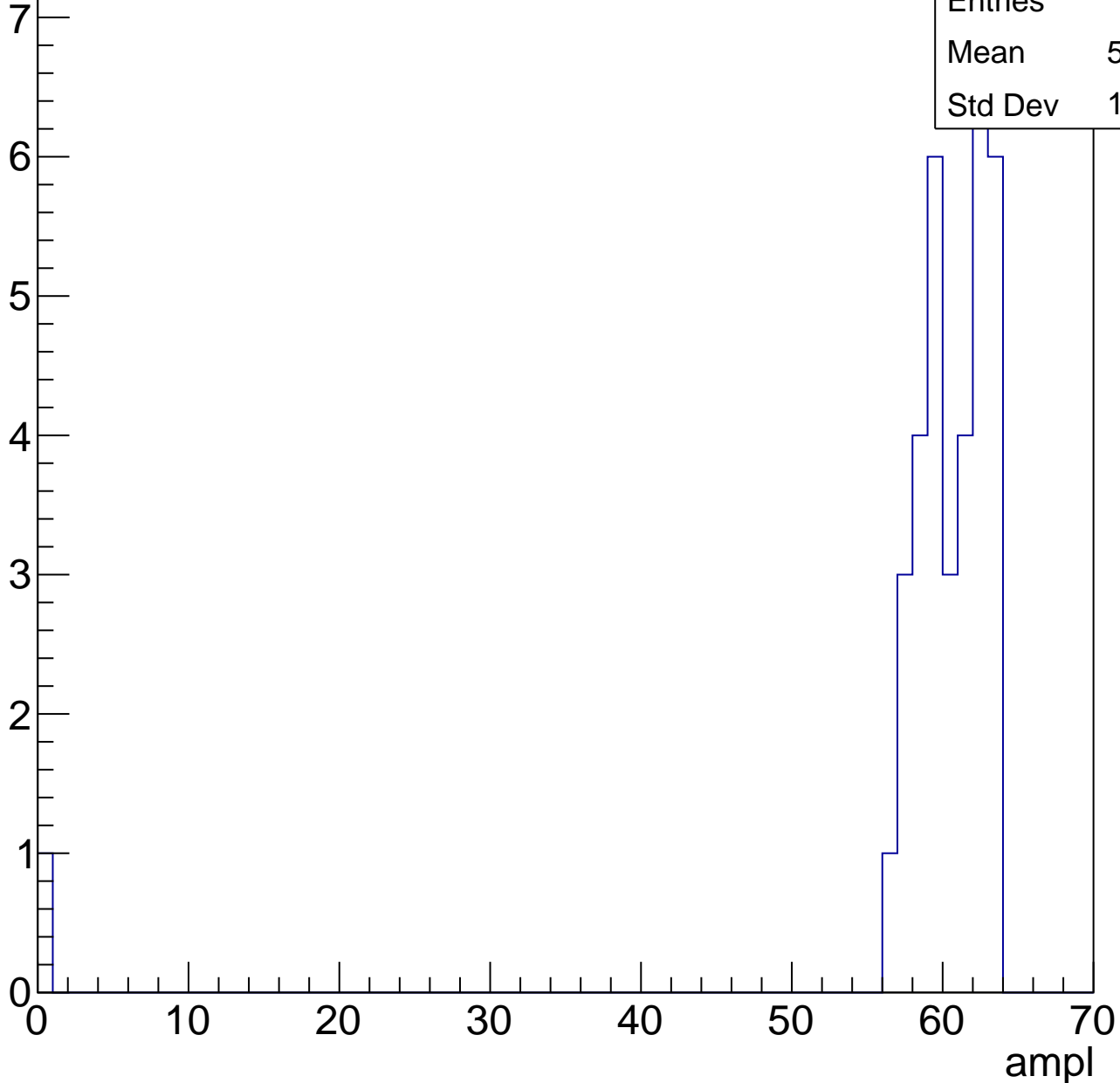


# B1L101S, U18-ch77, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	35
Mean	58.54
Std Dev	10.25



# B1L101S, U18-ch77, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch77, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch78, adc0

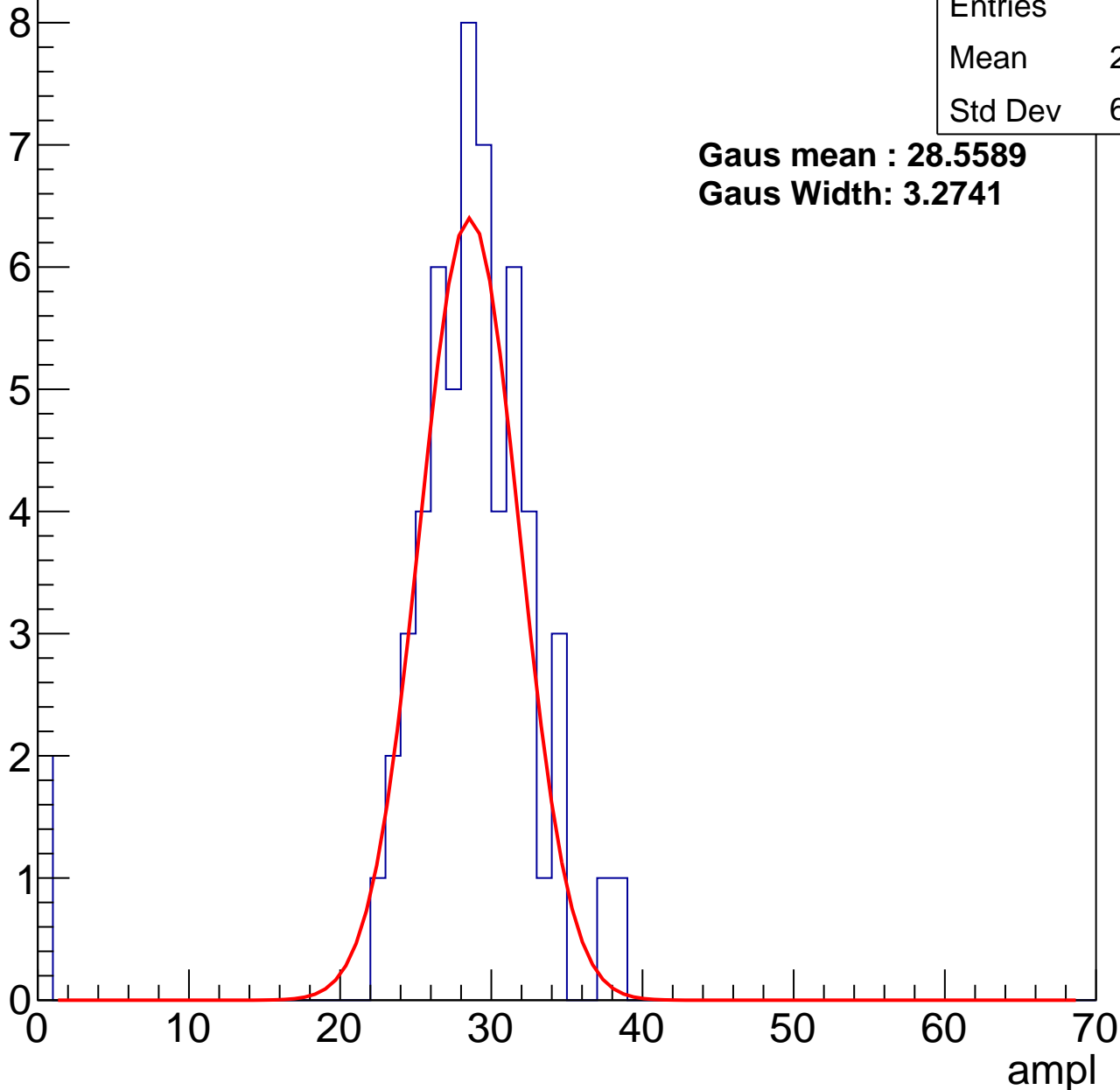
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	27.62
Std Dev	6.178

**Gaus mean : 28.5589**

**Gaus Width: 3.2741**



# B1L101S, U18-ch78, adc1

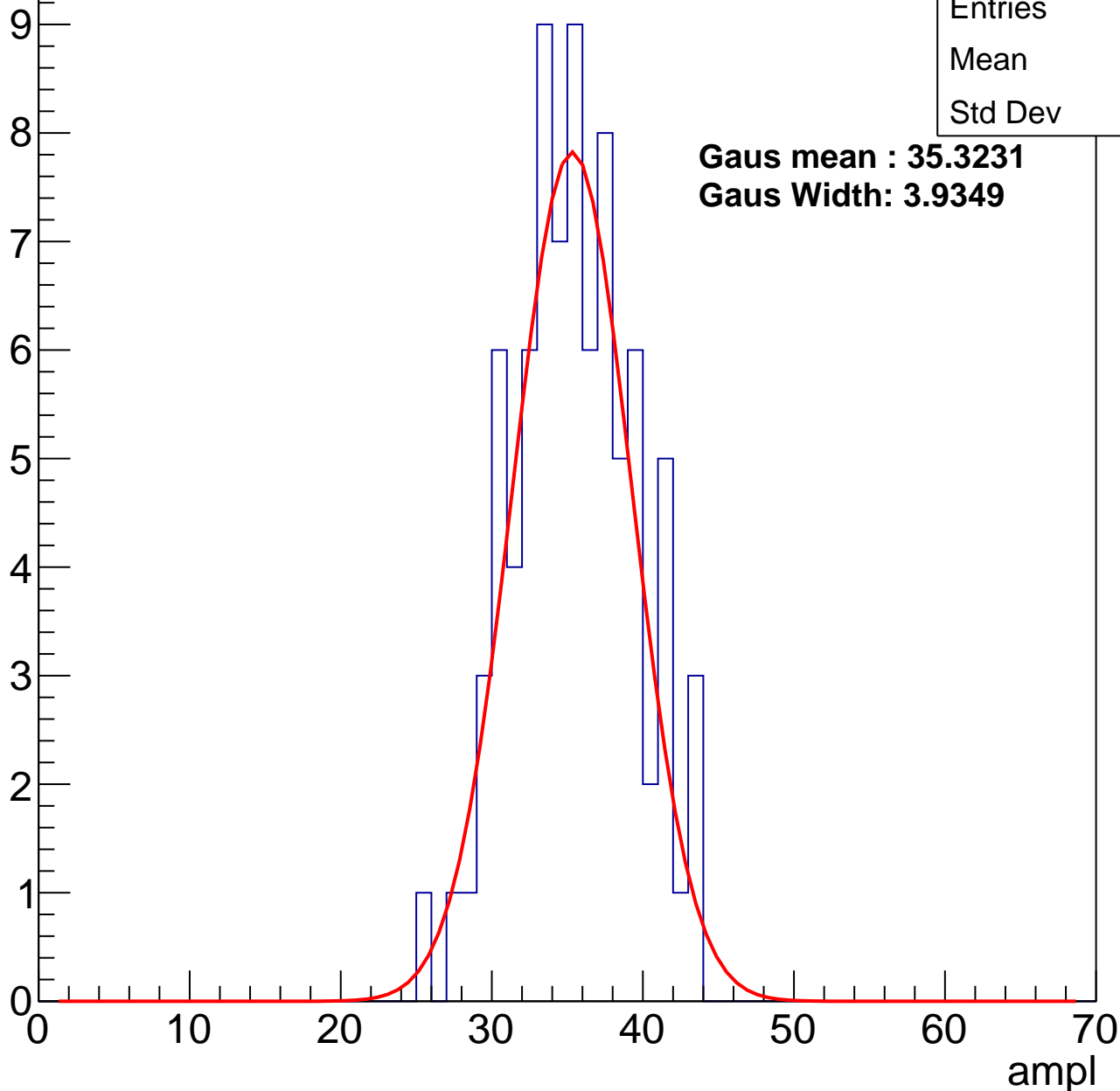
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	83
Mean	35
Std Dev	3.93

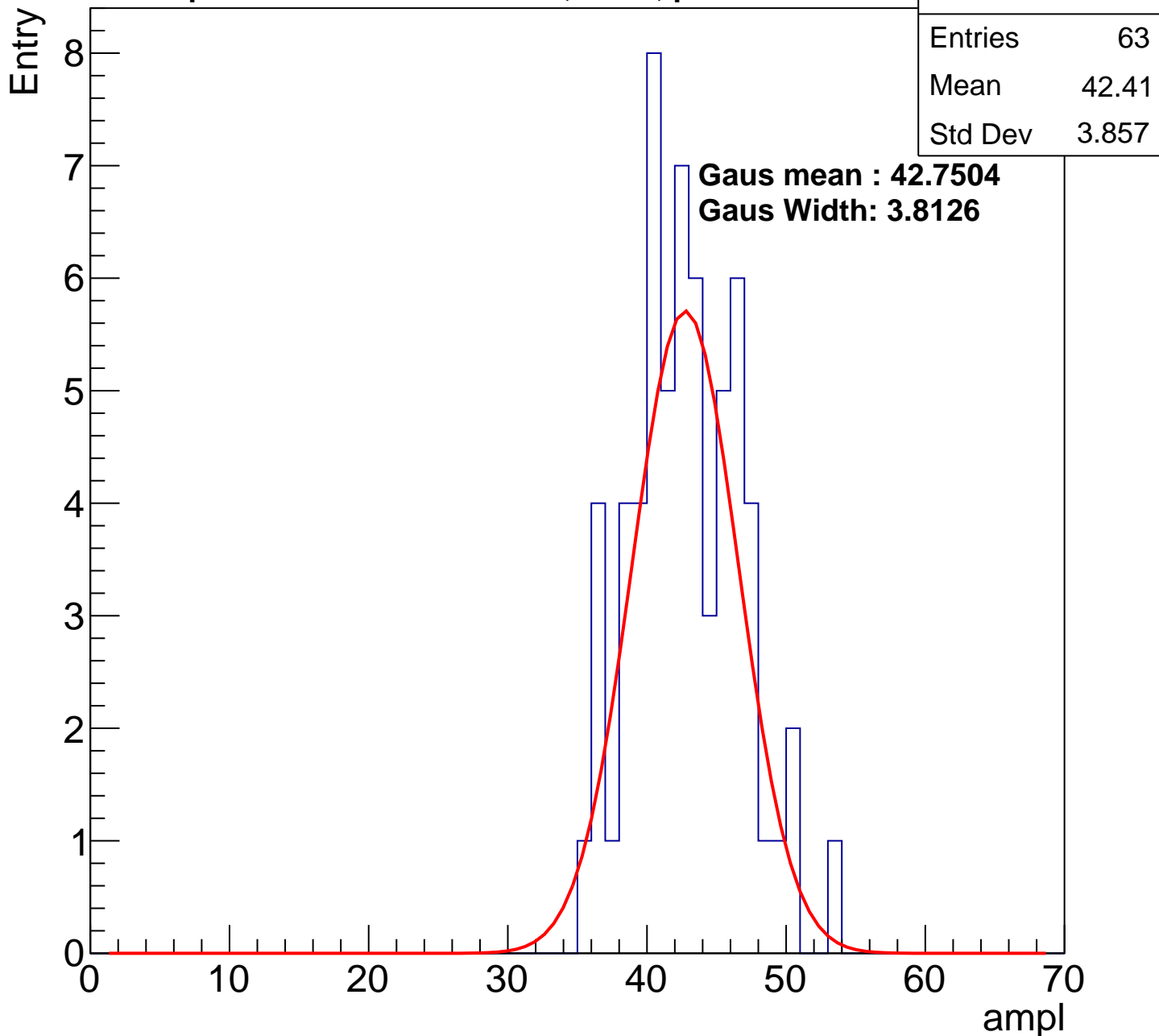
**Gaus mean : 35.3231**

**Gaus Width: 3.9349**



# B1L101S, U18-ch78, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

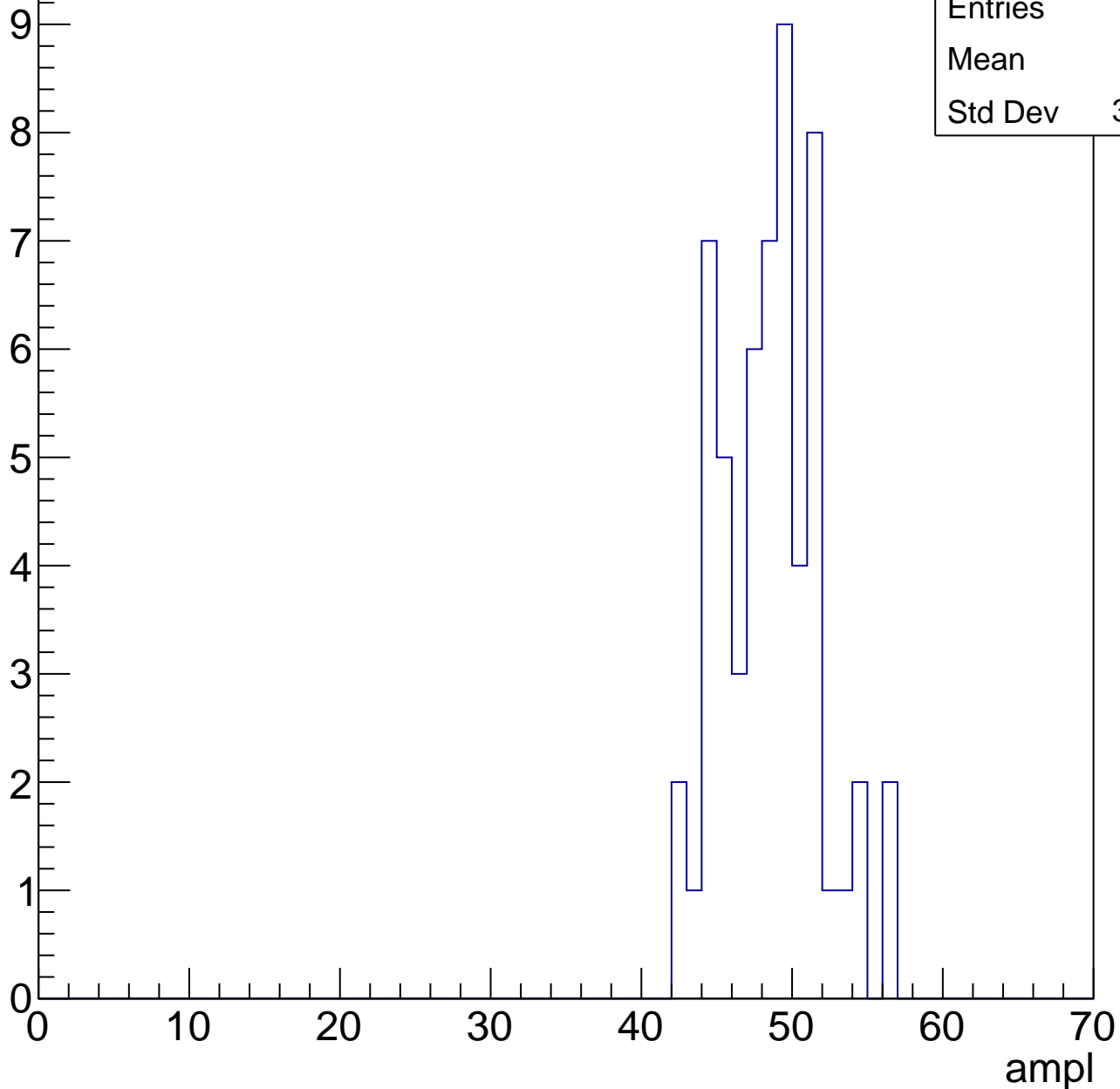


# B1L101S, U18-ch78, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

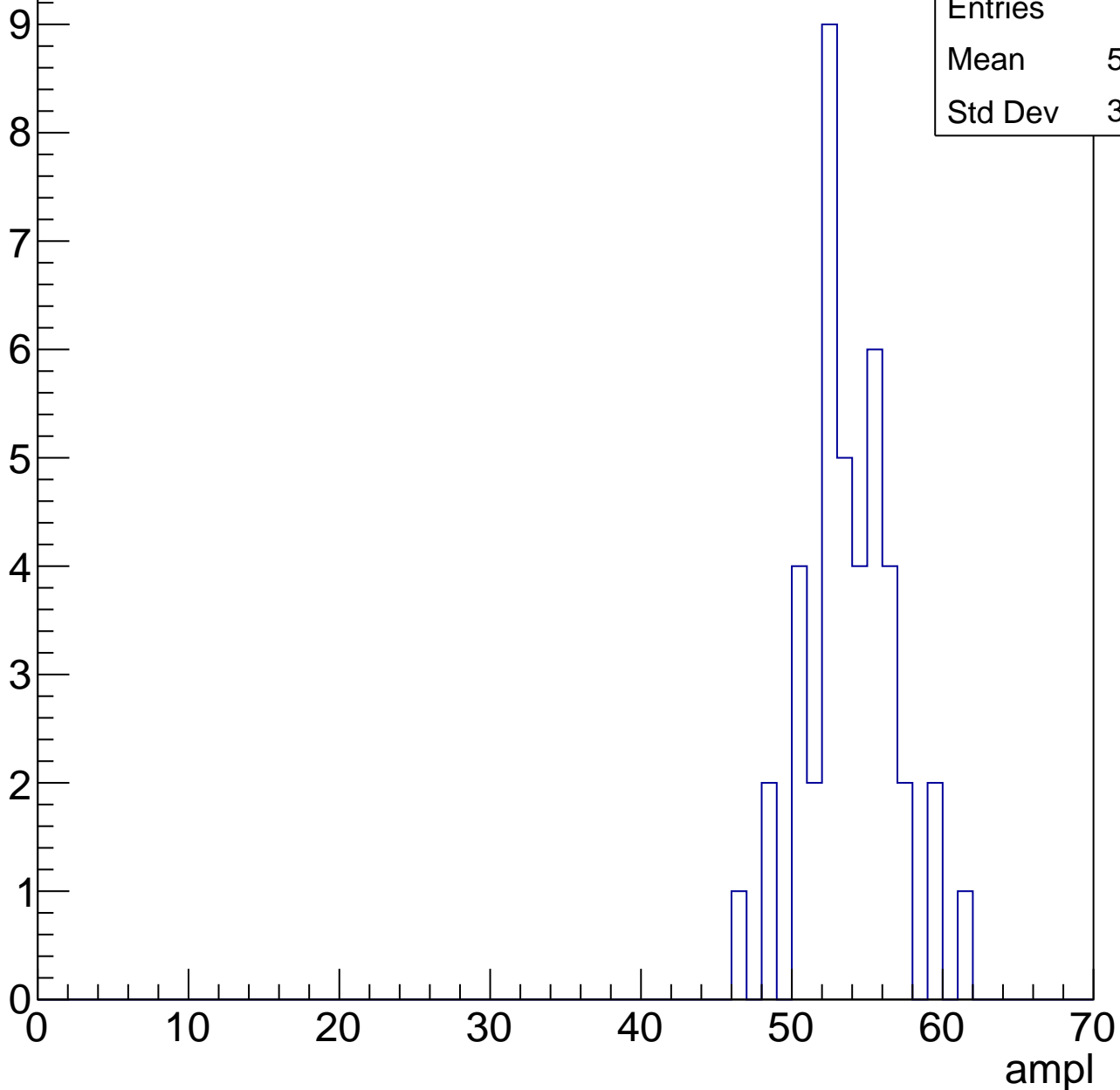
Entries	58
Mean	48.1
Std Dev	3.241



# B1L101S, U18-ch78, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch78, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

10

Entries 74

Mean 57.93

Std Dev 7.301

8

6

4

2

0

0

10

20

30

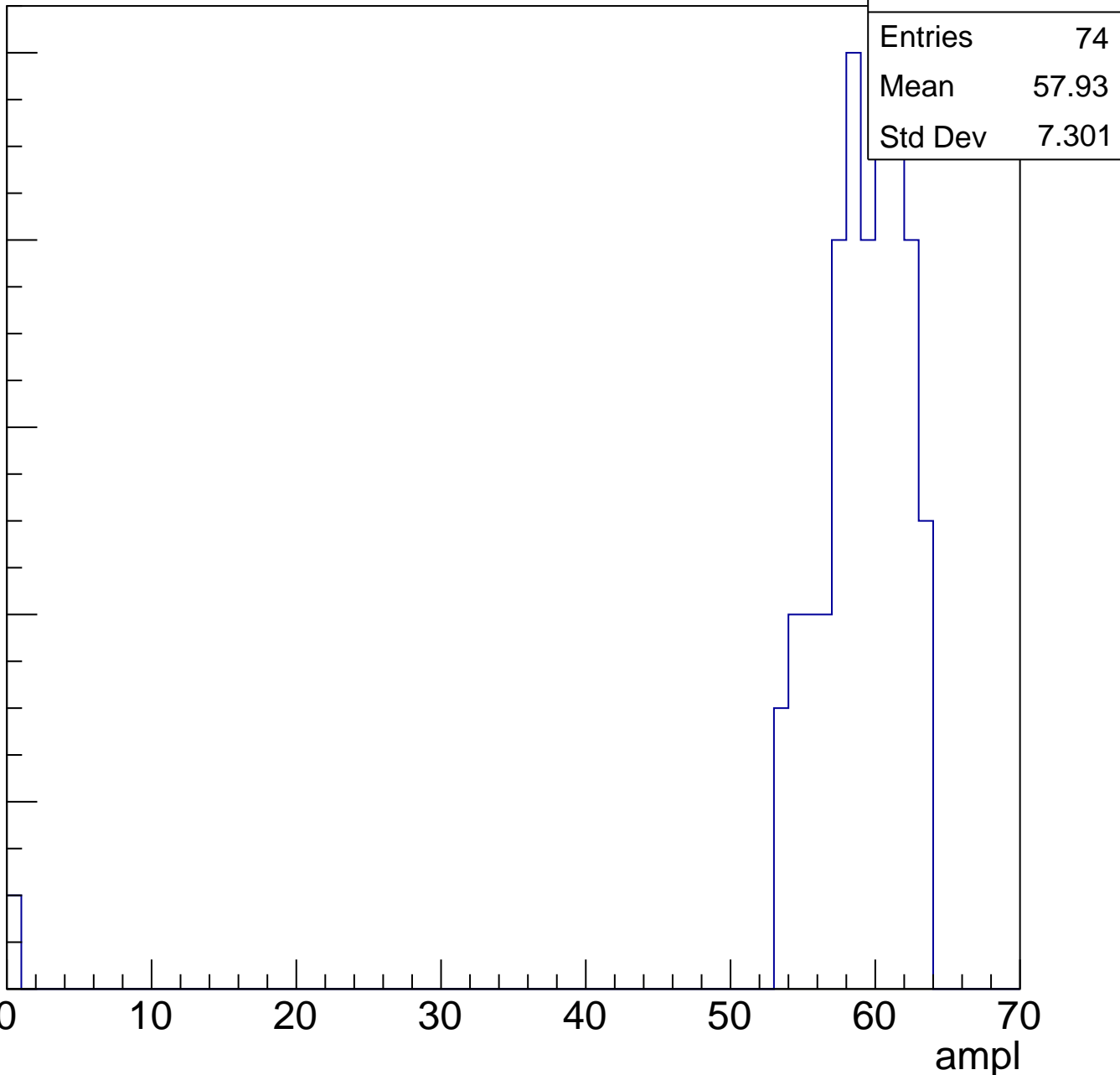
40

50

60

70

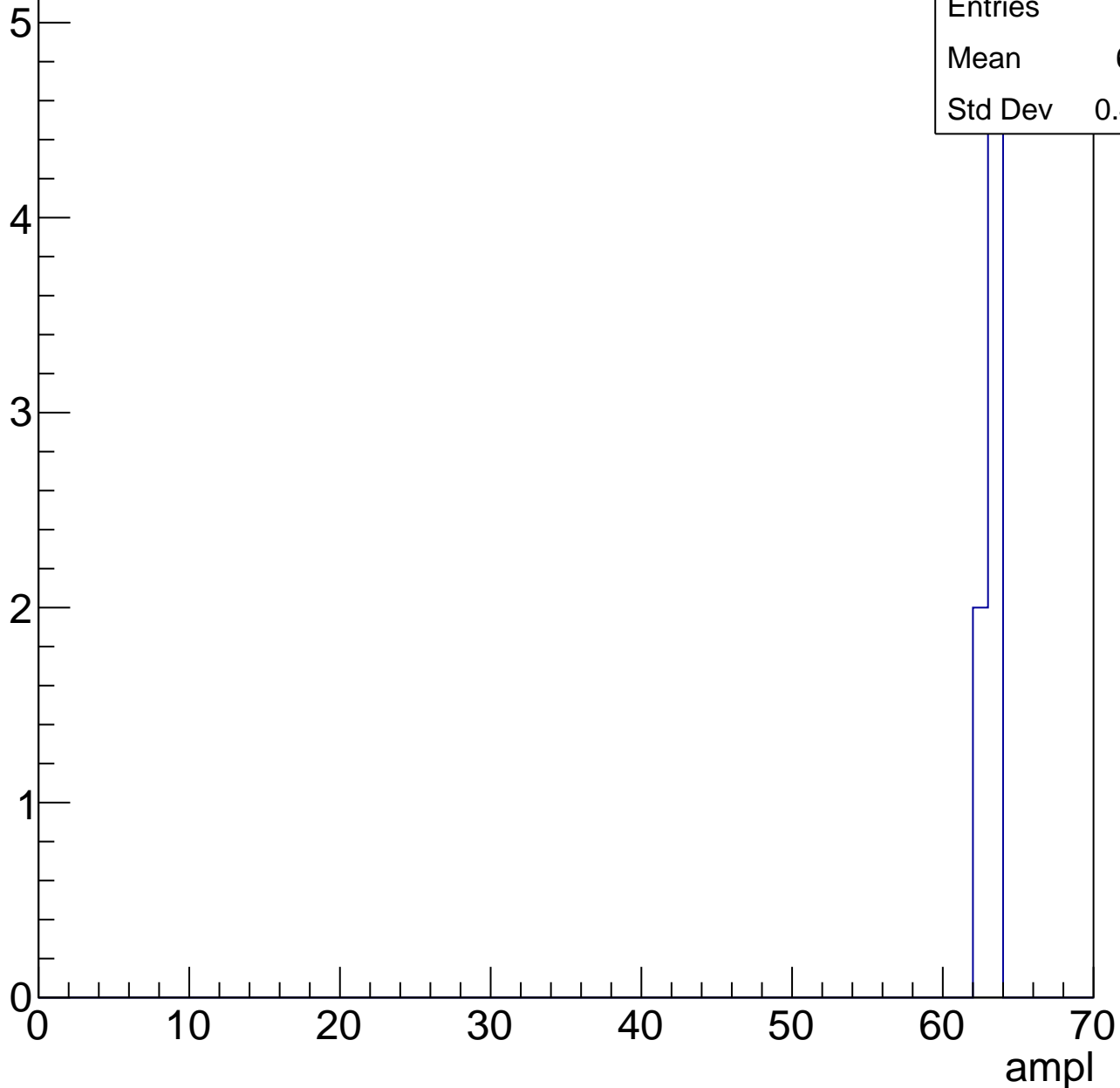
ampl



# B1L101S, U18-ch78, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch78, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U18-ch79, adc0

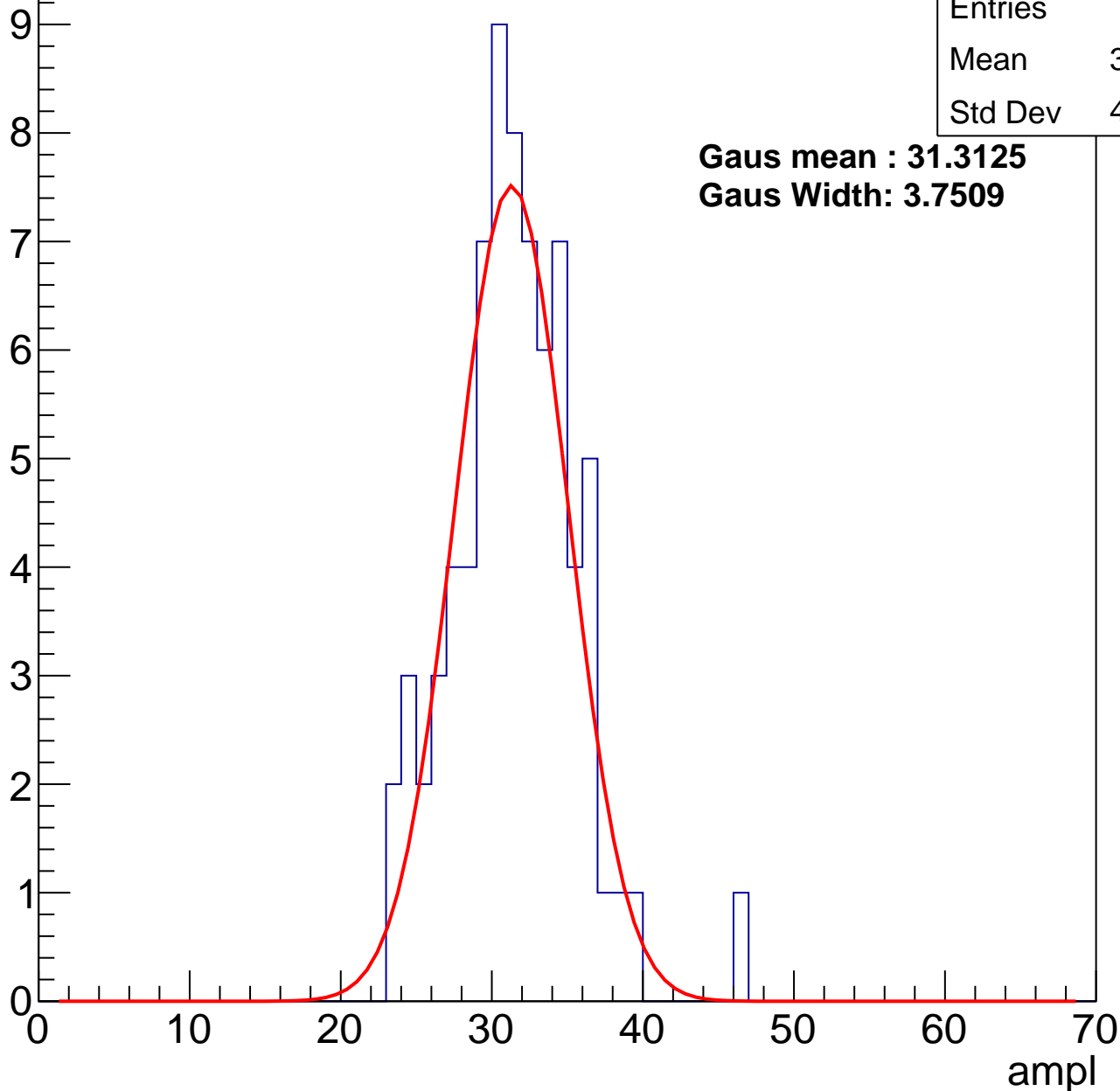
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	31.03
Std Dev	4.026

**Gaus mean : 31.3125**

**Gaus Width: 3.7509**



# B1L101S, U18-ch79, adc1

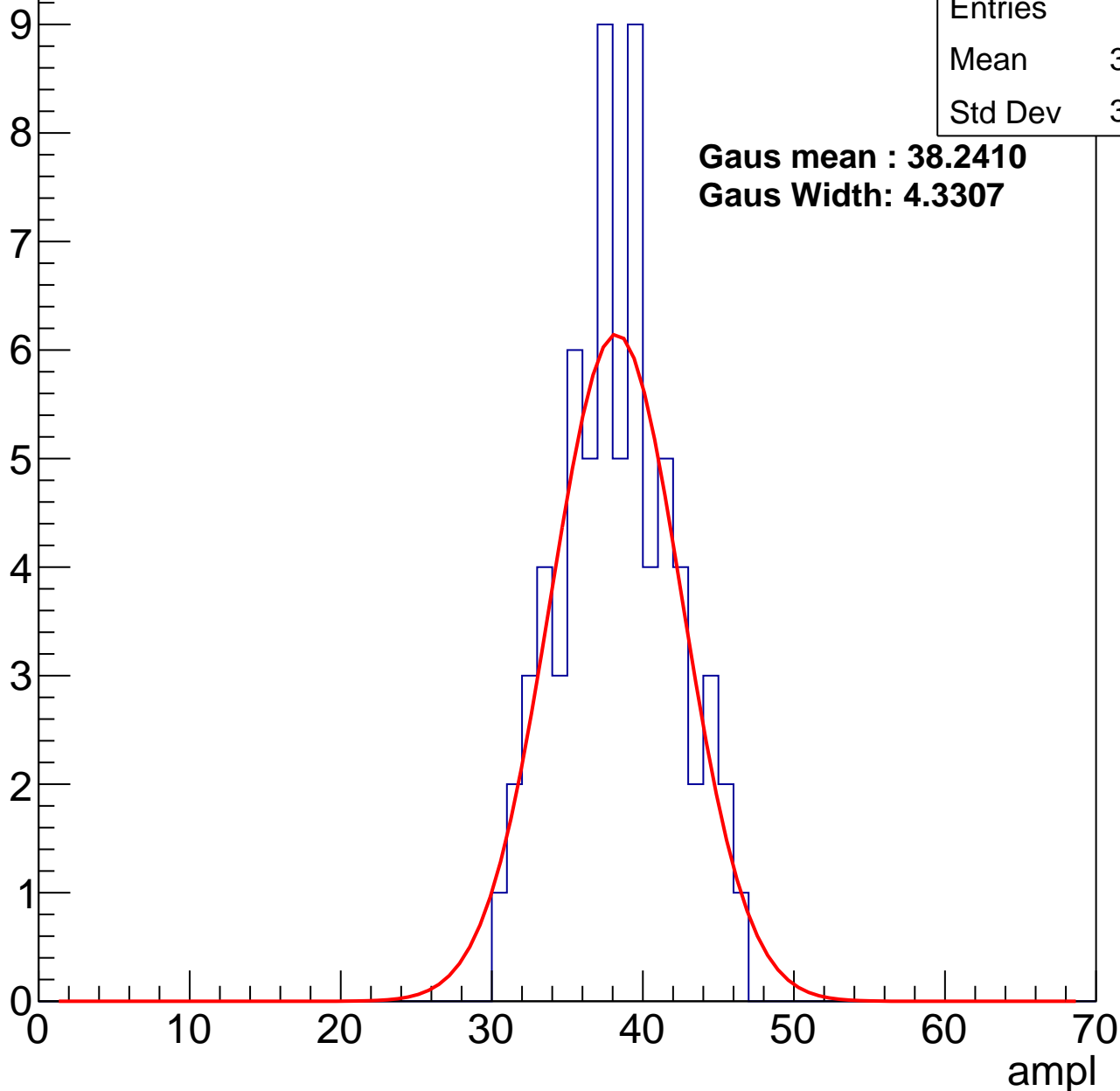
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	37.84
Std Dev	3.744

**Gaus mean : 38.2410**

**Gaus Width: 4.3307**



# B1L101S, U18-ch79, adc2

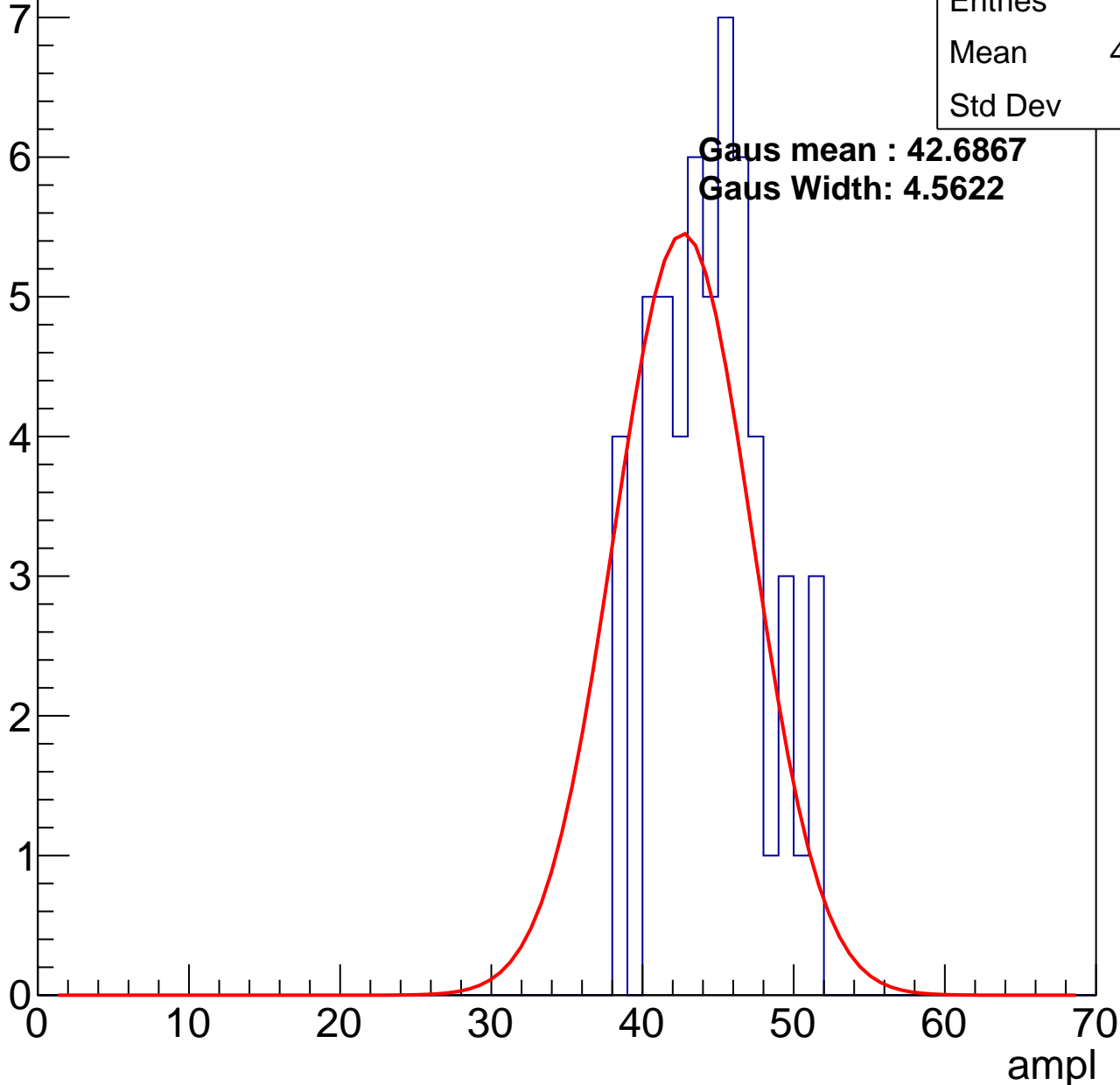
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	44.07
Std Dev	3.42

**Gaus mean : 42.6867**

**Gaus Width: 4.5622**

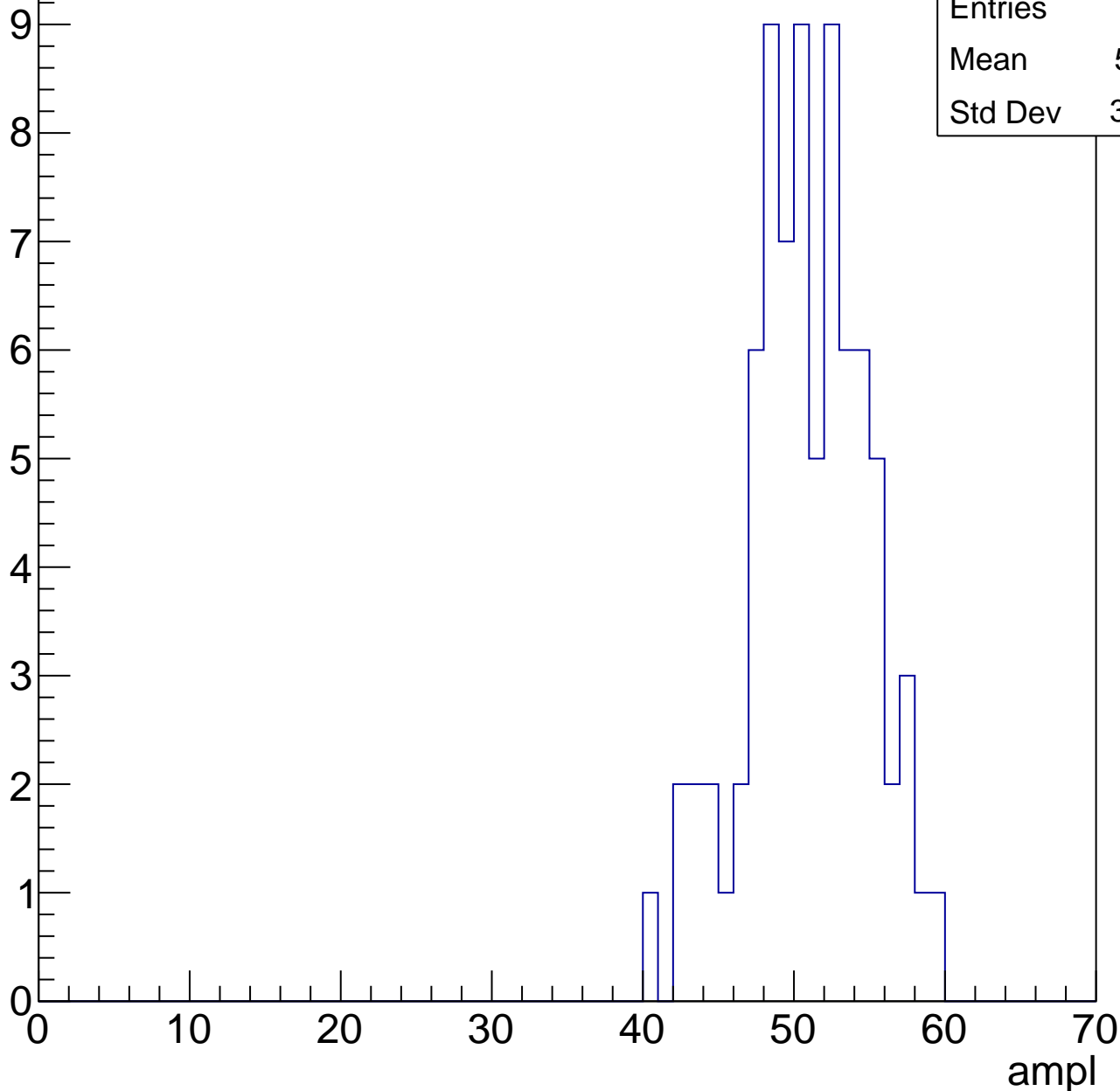


# B1L101S, U18-ch79, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	79
Mean	50.41
Std Dev	3.928

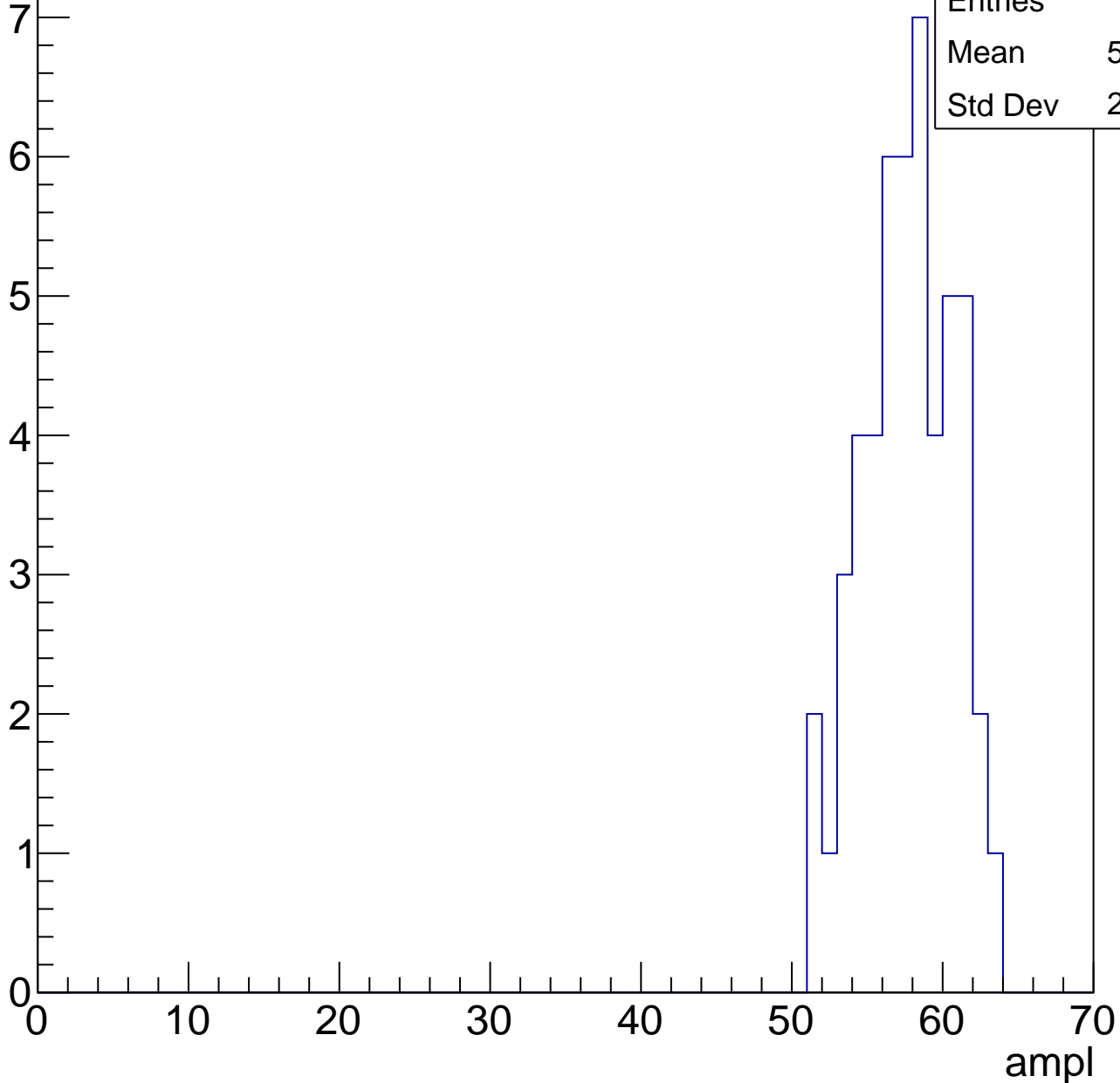


# B1L101S, U18-ch79, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	57.22
Std Dev	2.948

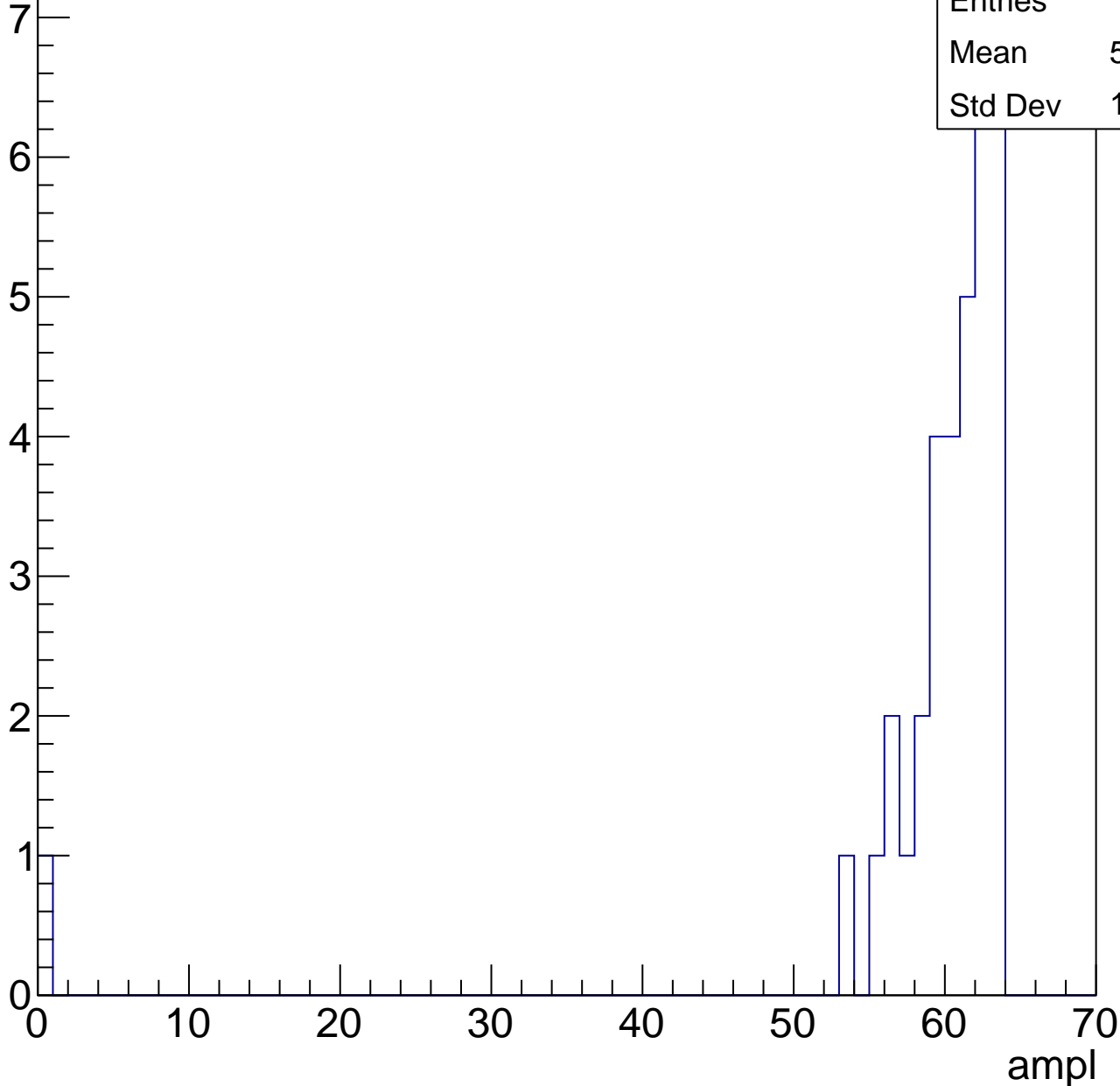


# B1L101S, U18-ch79, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	35
Mean	58.54
Std Dev	10.35



# B1L101S, U18-ch79, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

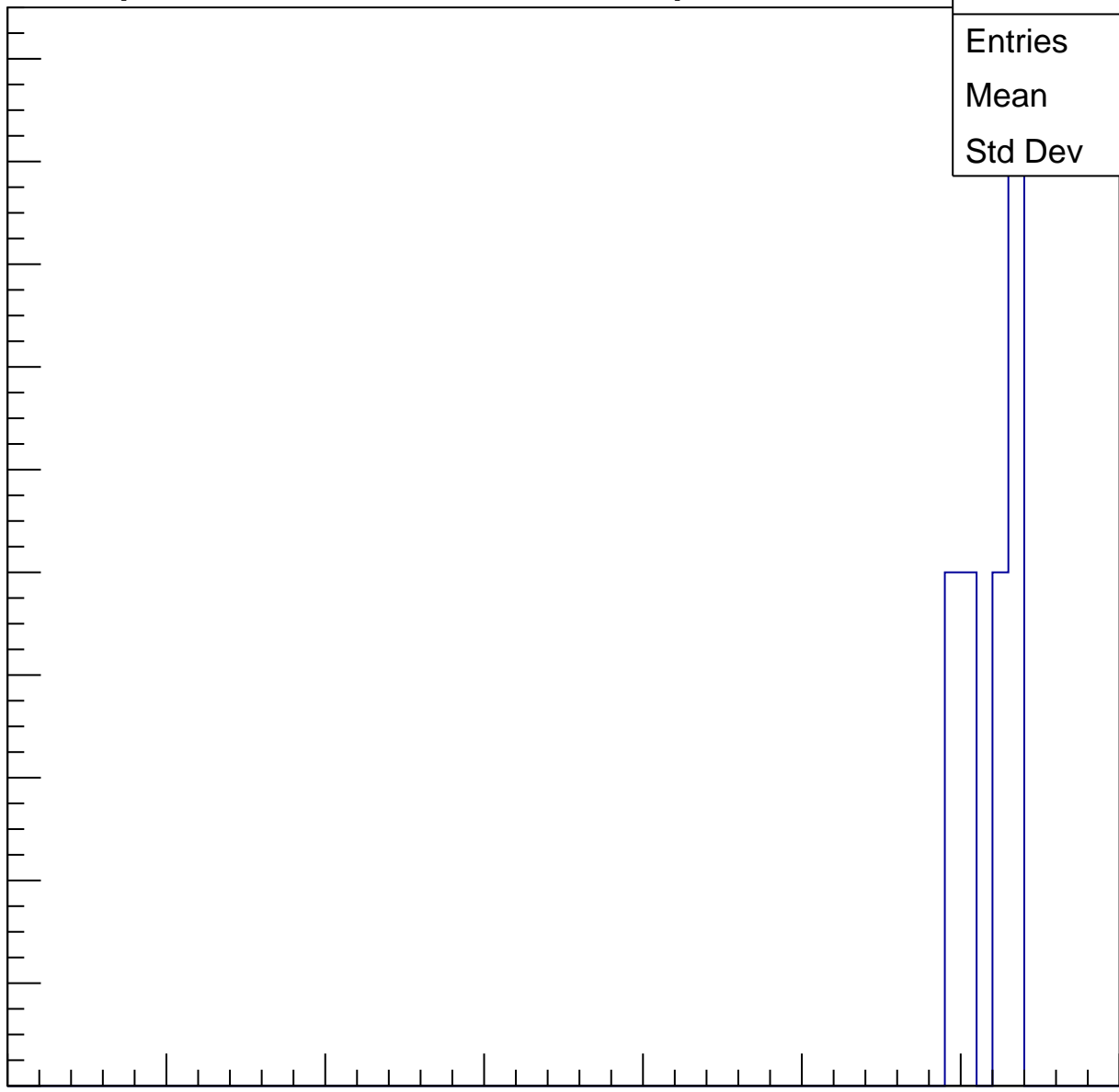
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	61.4
Std Dev	1.625

ampl

0 10 20 30 40 50 60 70





# B1L101S, U18-ch79, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch80, adc0

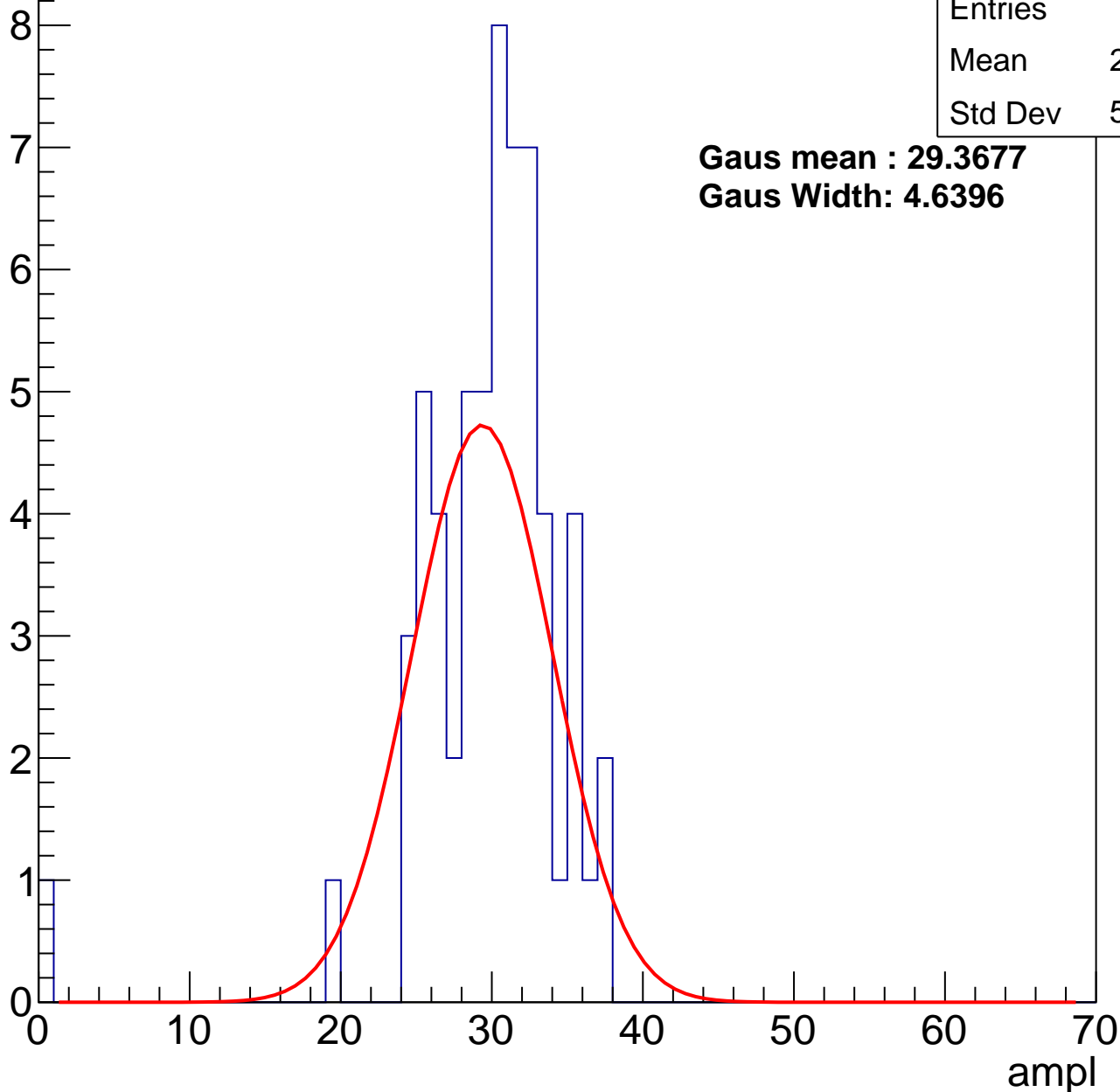
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	29.27
Std Dev	5.244

**Gaus mean : 29.3677**

**Gaus Width: 4.6396**



# B1L101S, U18-ch80, adc1

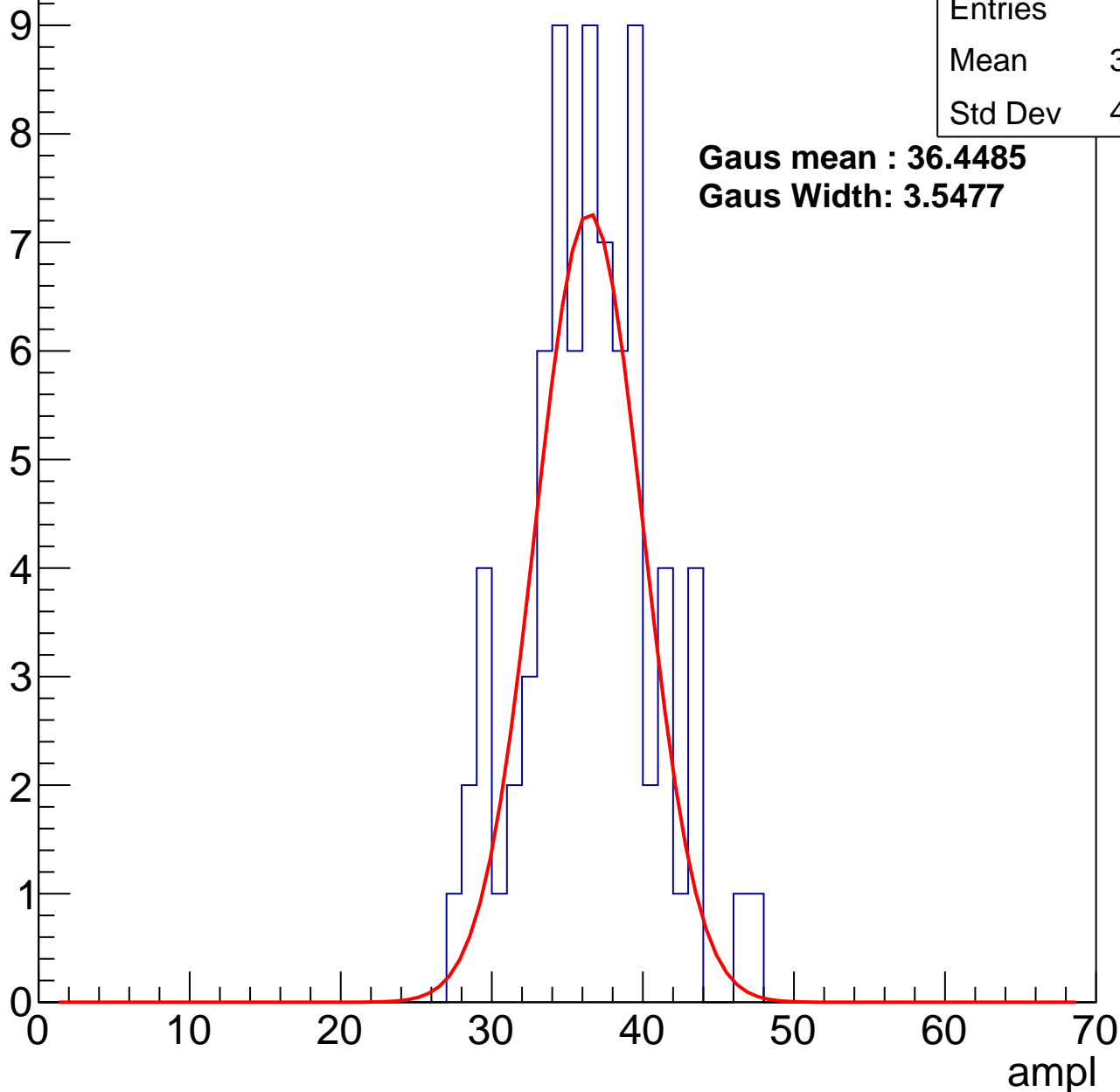
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	78
Mean	36.08
Std Dev	4.132

**Gaus mean : 36.4485**

**Gaus Width: 3.5477**



# B1L101S, U18-ch80, adc2

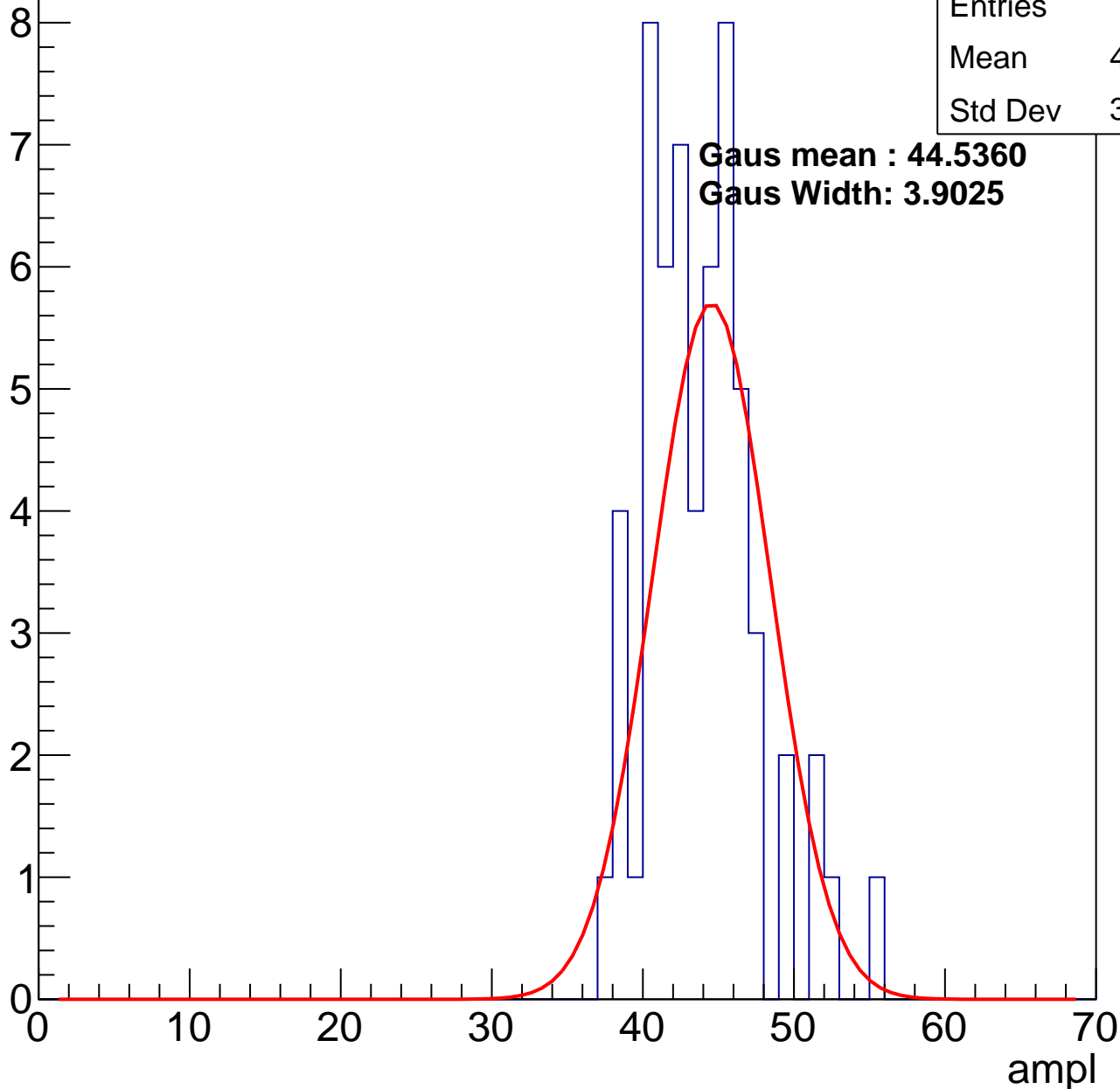
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	43.42
Std Dev	3.683

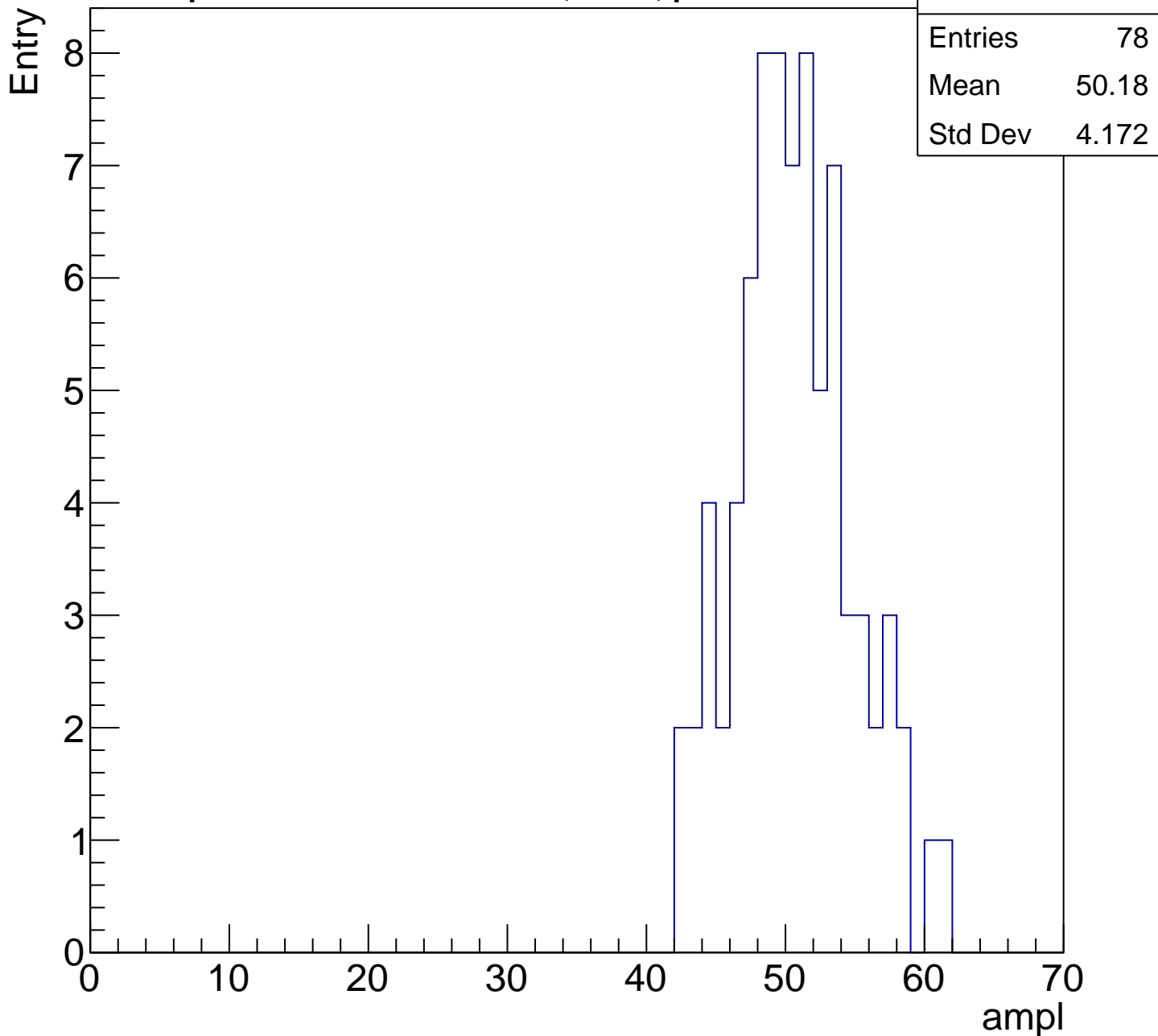
**Gaus mean : 44.5360**

**Gaus Width: 3.9025**



# B1L101S, U18-ch80, adc3

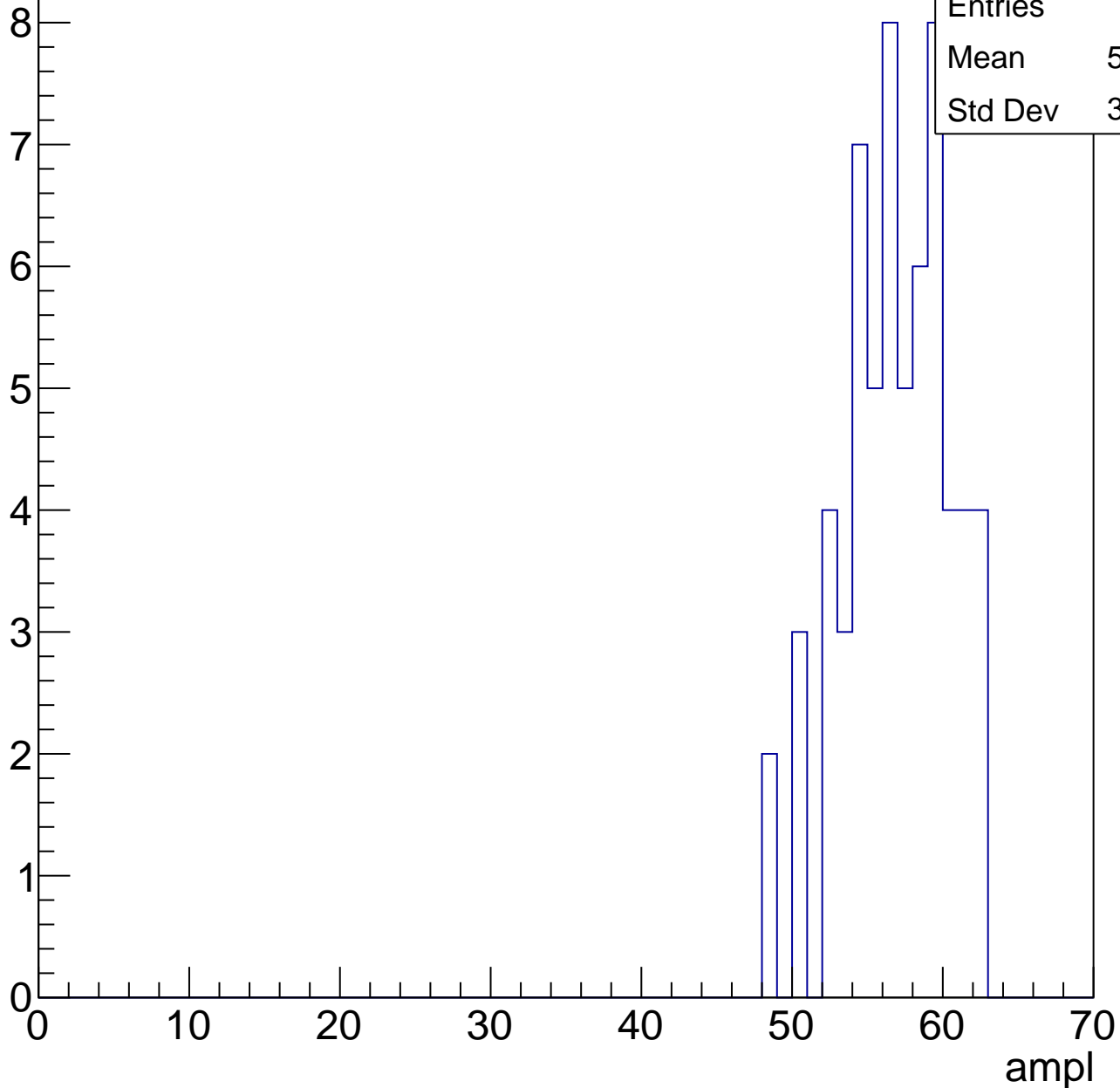
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U18-ch80, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



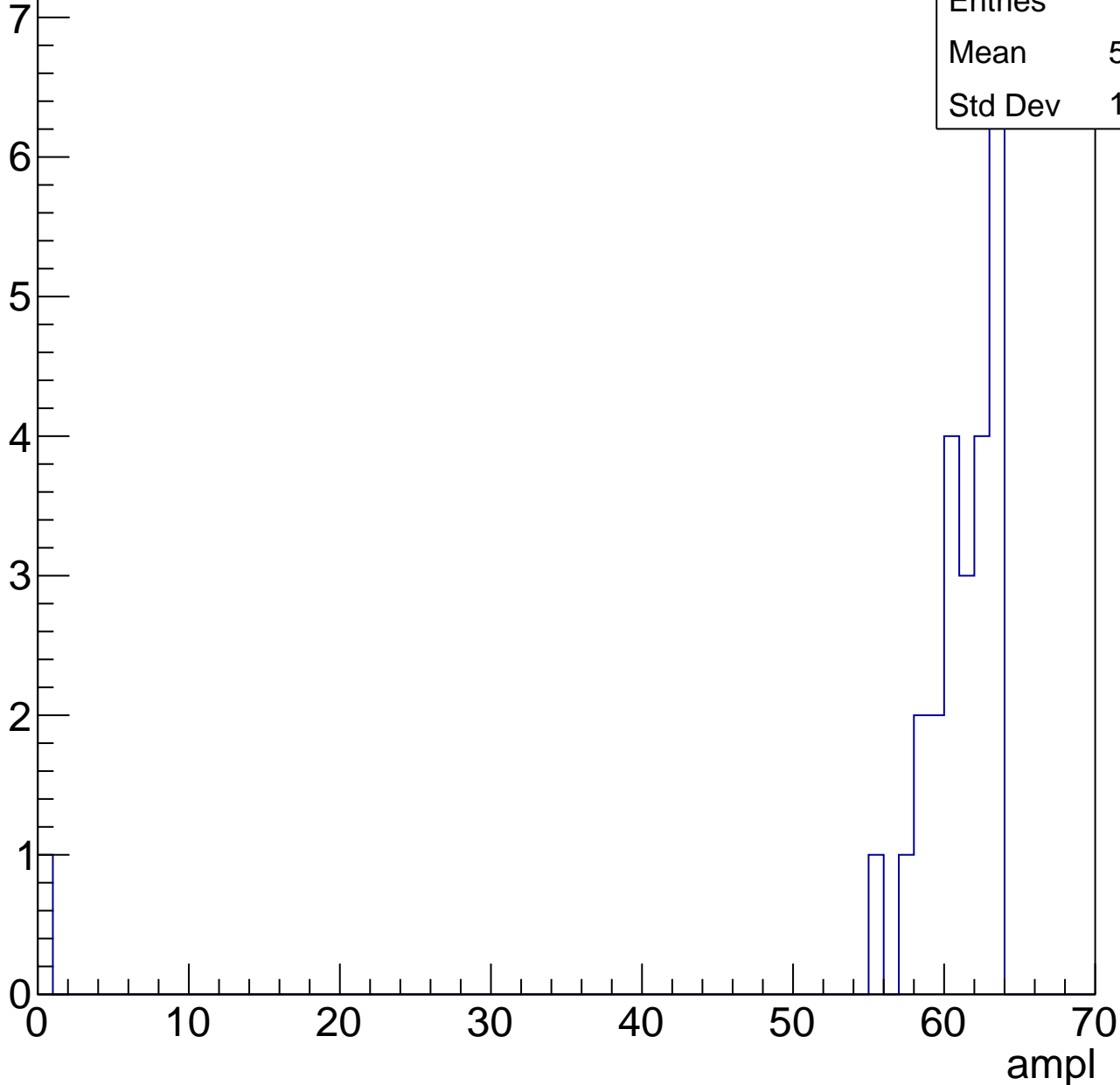
Entries	63
Mean	56.37
Std Dev	3.475

# B1L101S, U18-ch80, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

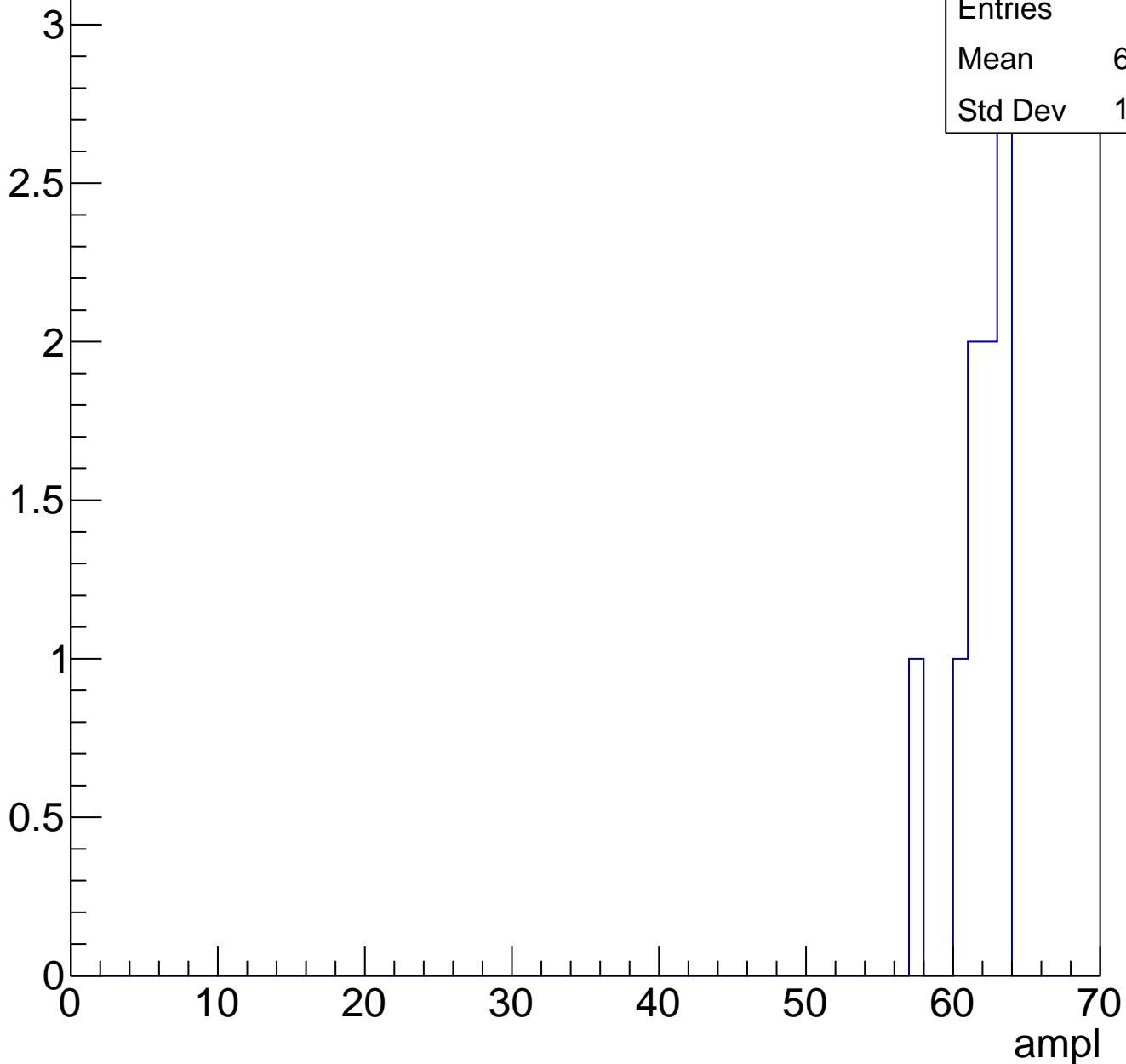
Entries	25
Mean	58.32
Std Dev	12.09



# B1L101S, U18-ch80, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch80, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch81, adc0

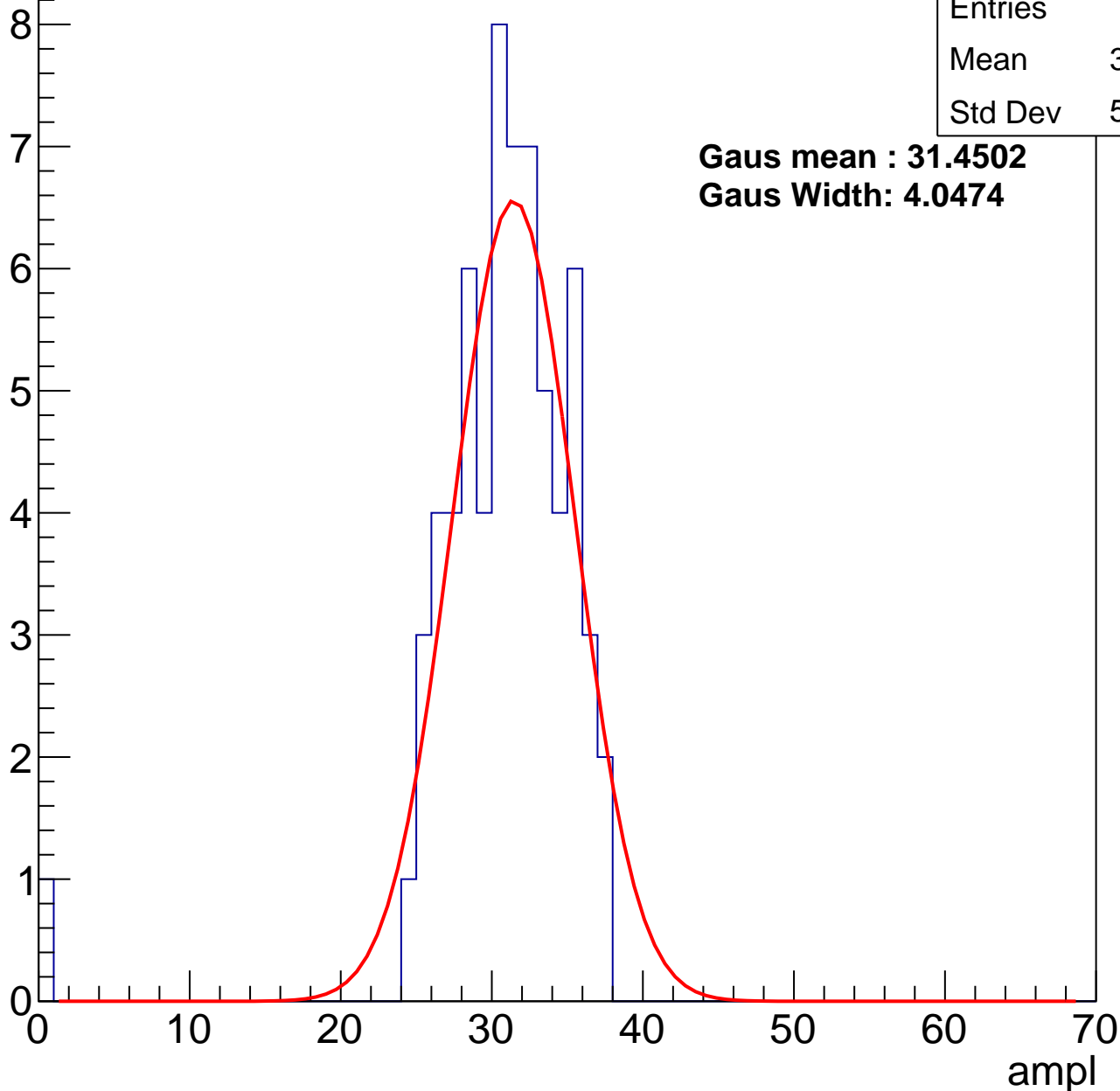
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	30.29
Std Dev	5.013

**Gaus mean : 31.4502**

**Gaus Width: 4.0474**



# B1L101S, U18-ch81, adc1

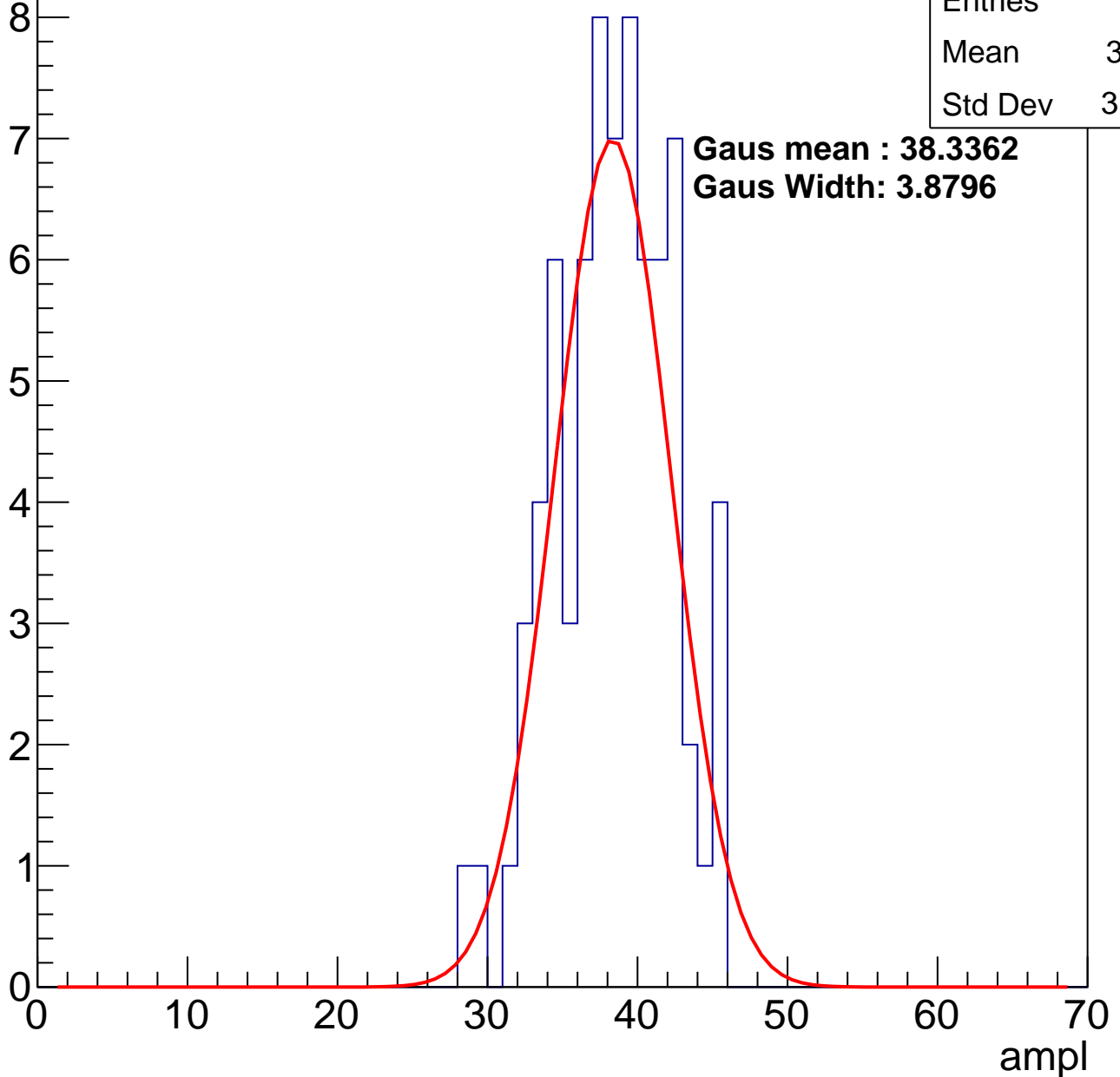
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	37.91
Std Dev	3.807

**Gaus mean : 38.3362**

**Gaus Width: 3.8796**



# B1L101S, U18-ch81, adc2

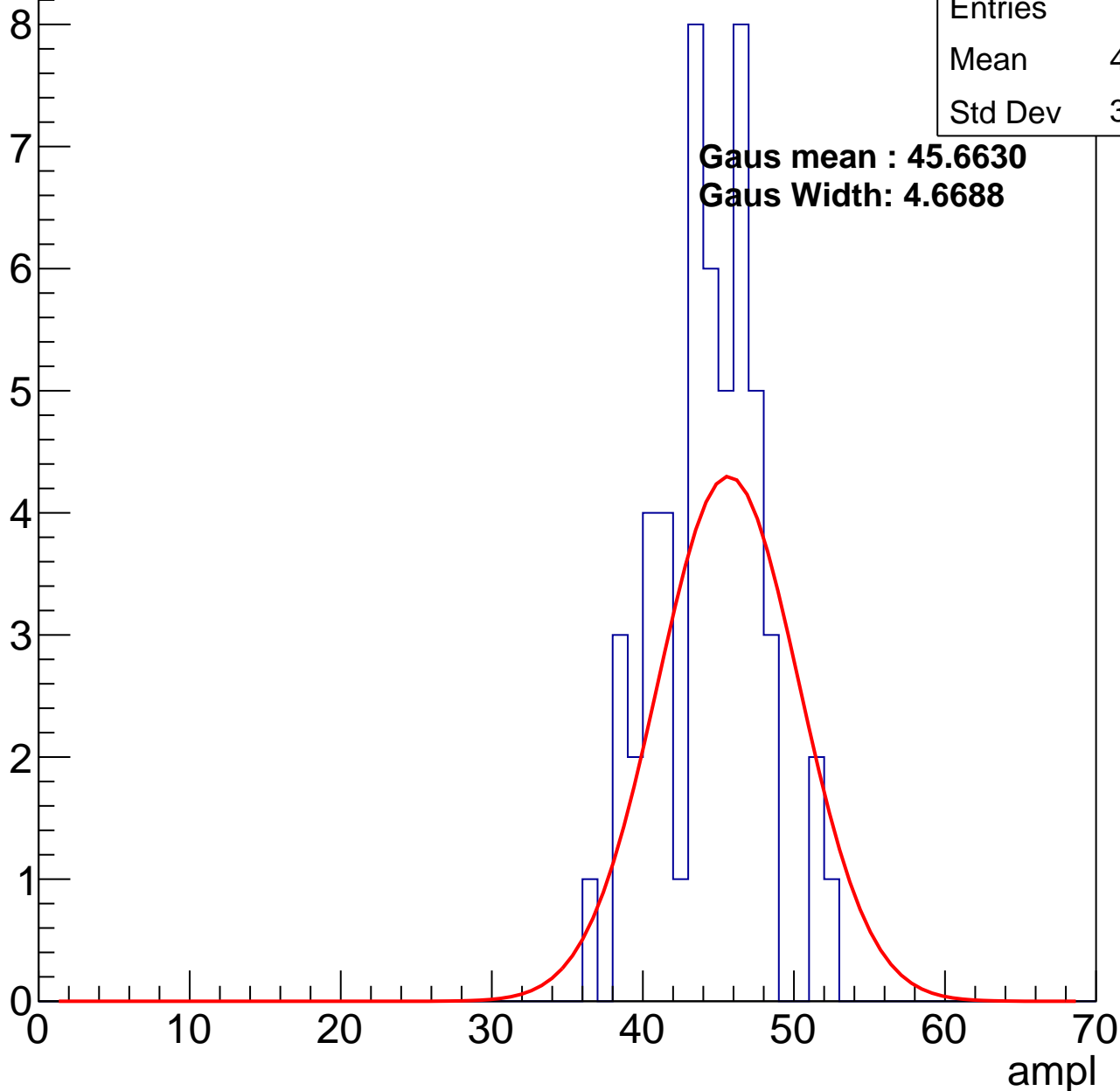
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	43.92
Std Dev	3.436

**Gaus mean : 45.6630**

**Gaus Width: 4.6688**

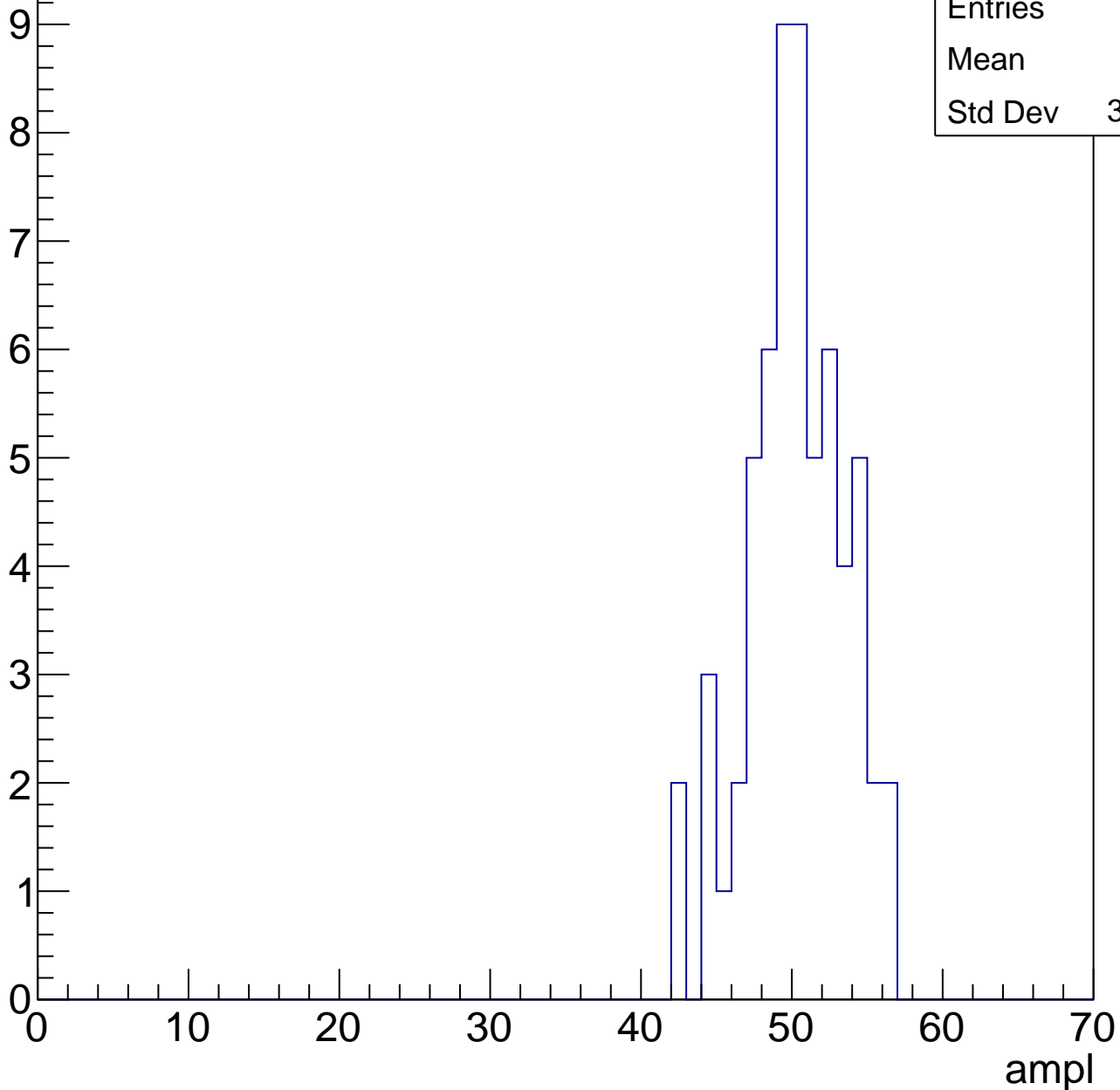


# B1L101S, U18-ch81, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	49.8
Std Dev	3.228



# B1L101S, U18-ch81, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	66
Mean	56.2
Std Dev	3.367

Entry

10

8

6

4

2

0

0

10

20

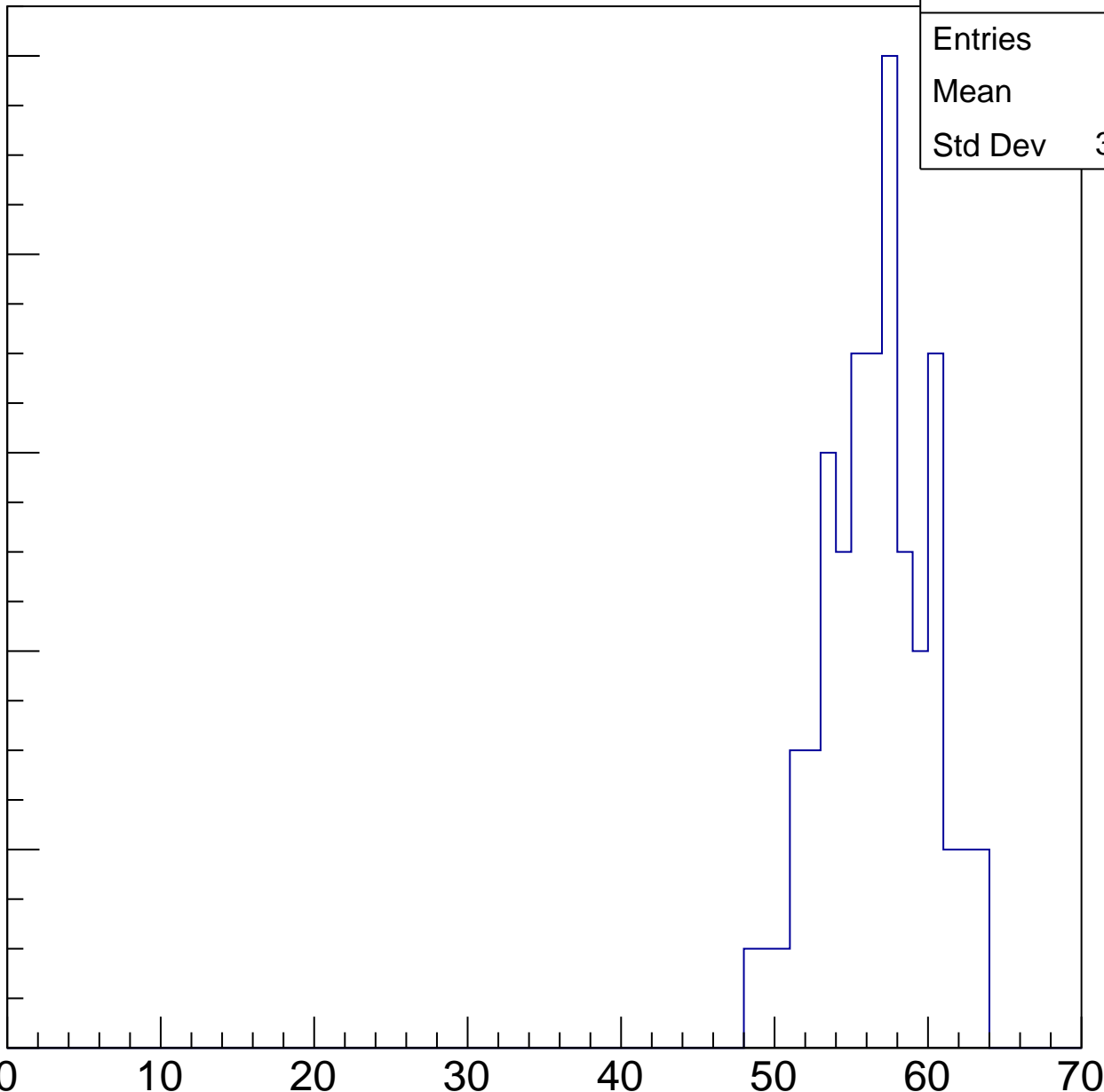
30

40

50

60

ampl

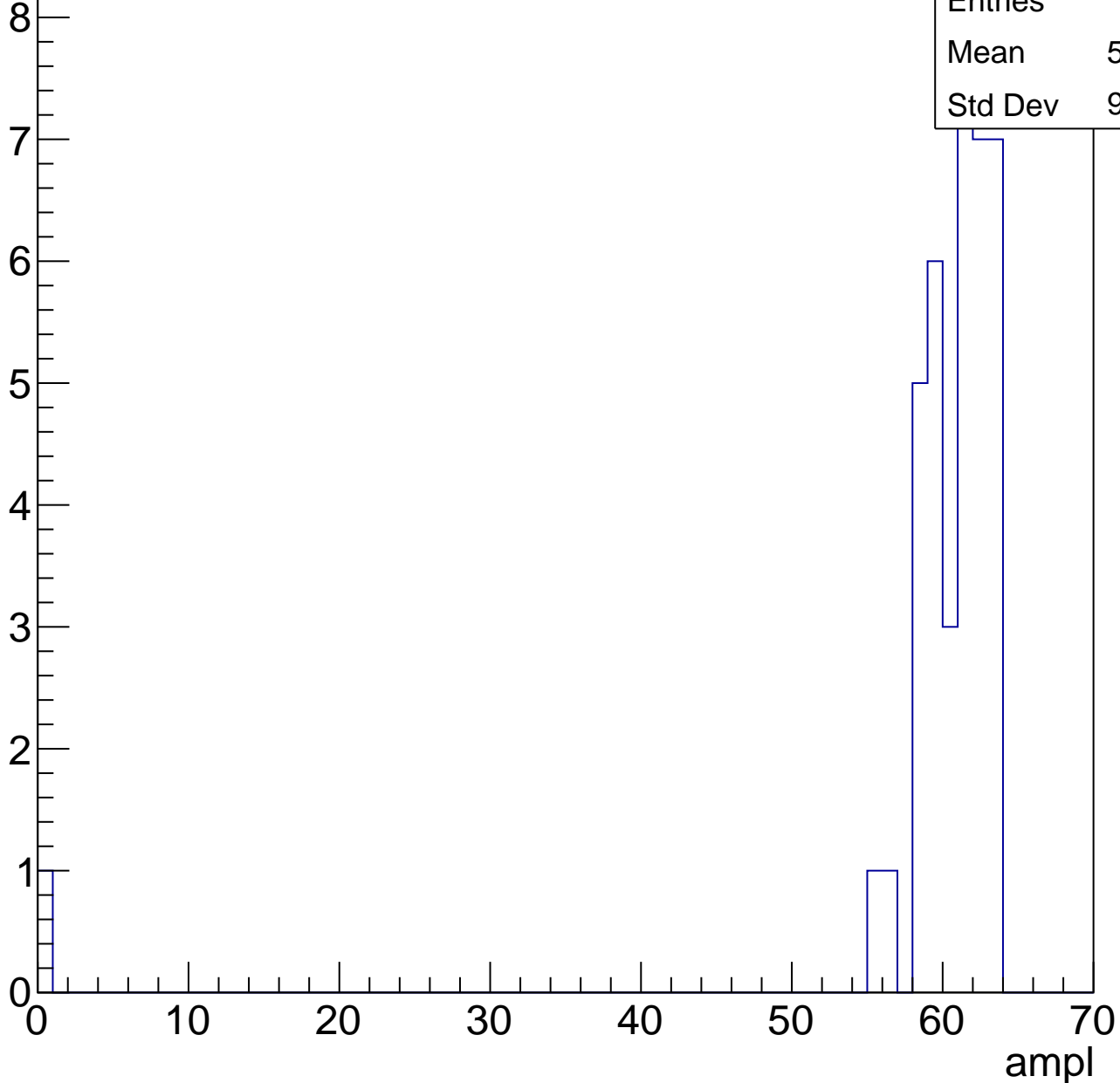


# B1L101S, U18-ch81, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	39
Mean	58.92
Std Dev	9.768



# B1L101S, U18-ch81, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch81, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U18-ch82, adc0

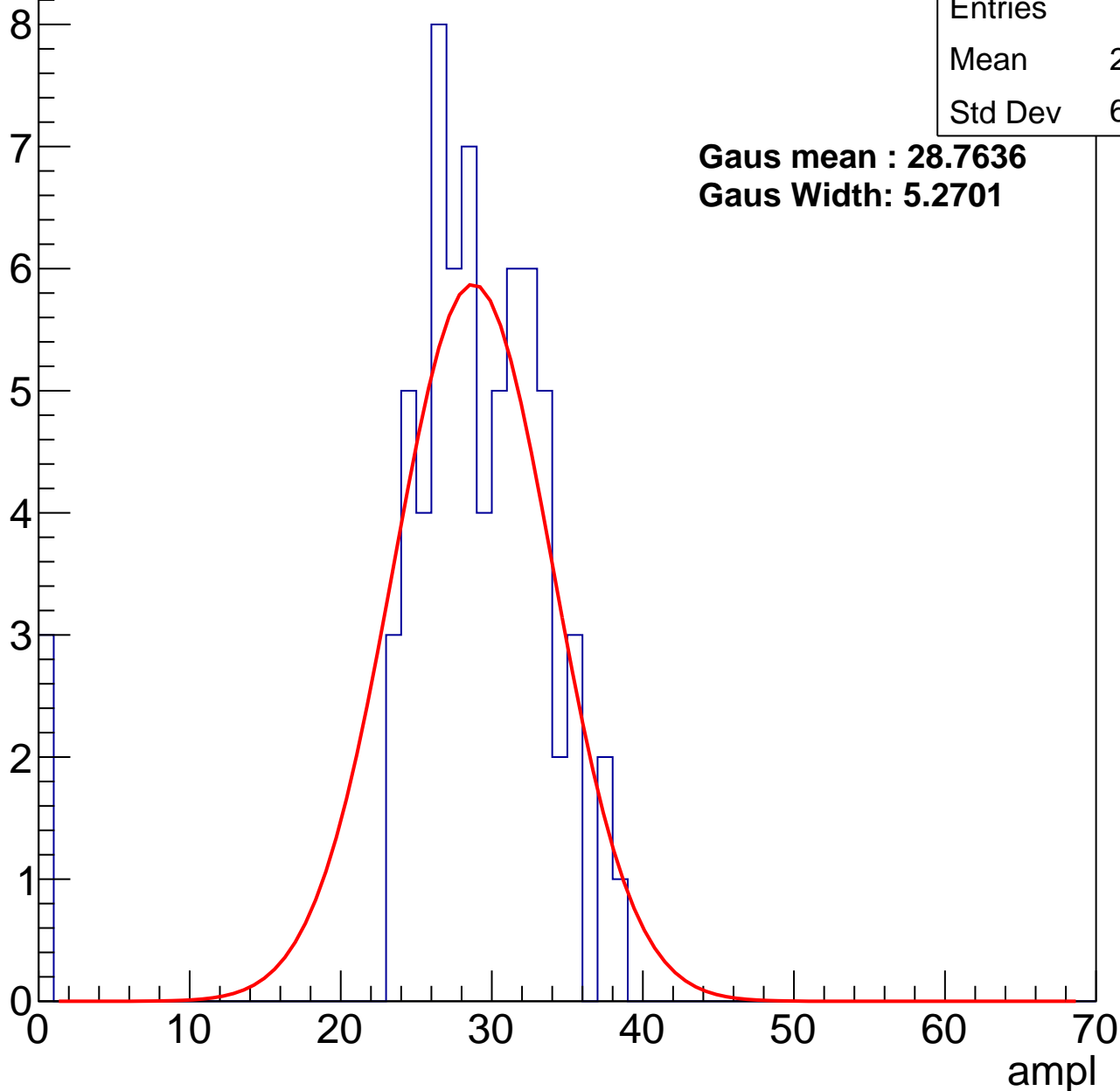
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	27.84
Std Dev	6.927

**Gaus mean : 28.7636**

**Gaus Width: 5.2701**



# B1L101S, U18-ch82, adc1

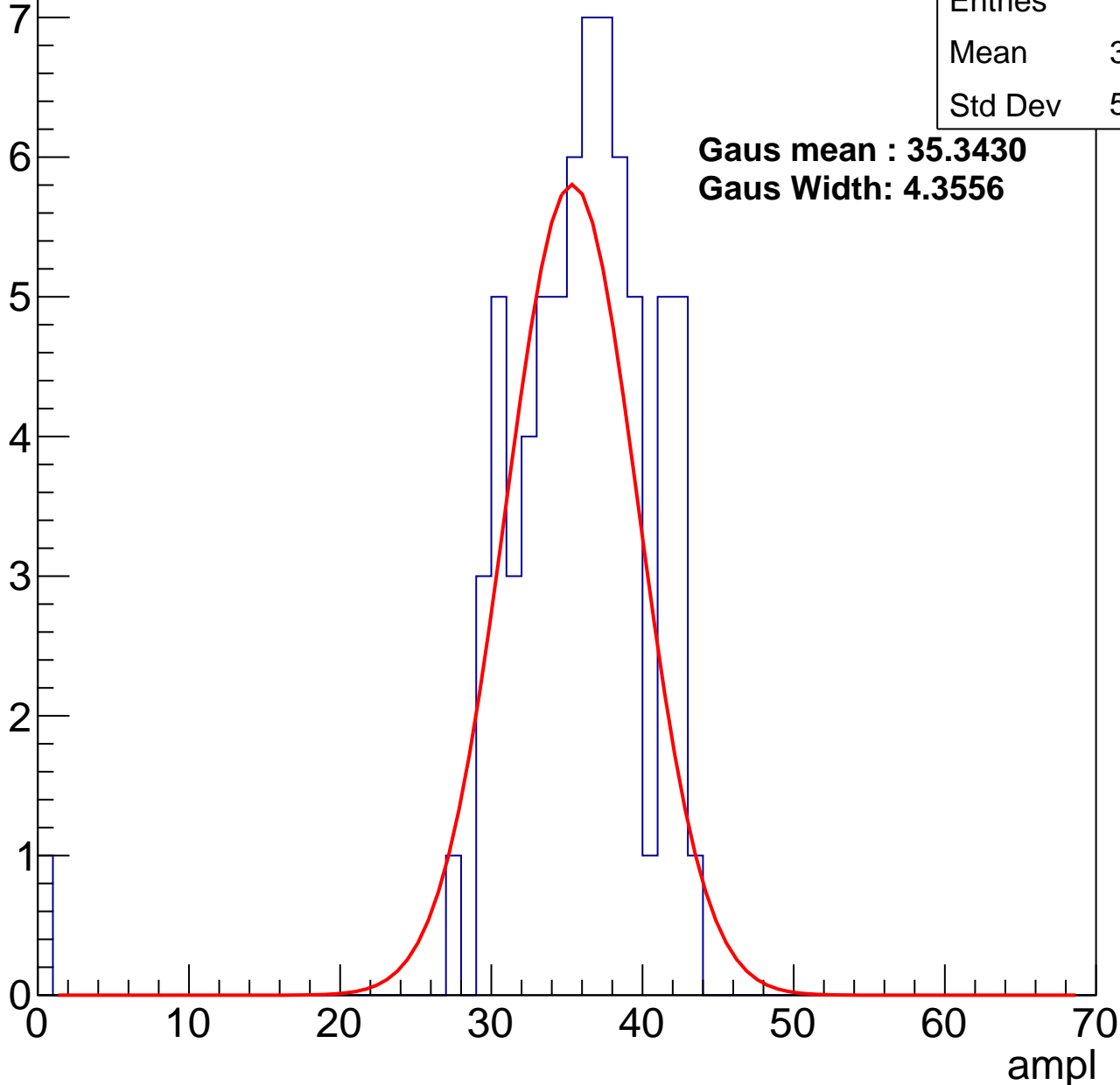
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	35.17
Std Dev	5.747

**Gaus mean : 35.3430**

**Gaus Width: 4.3556**



# B1L101S, U18-ch82, adc2

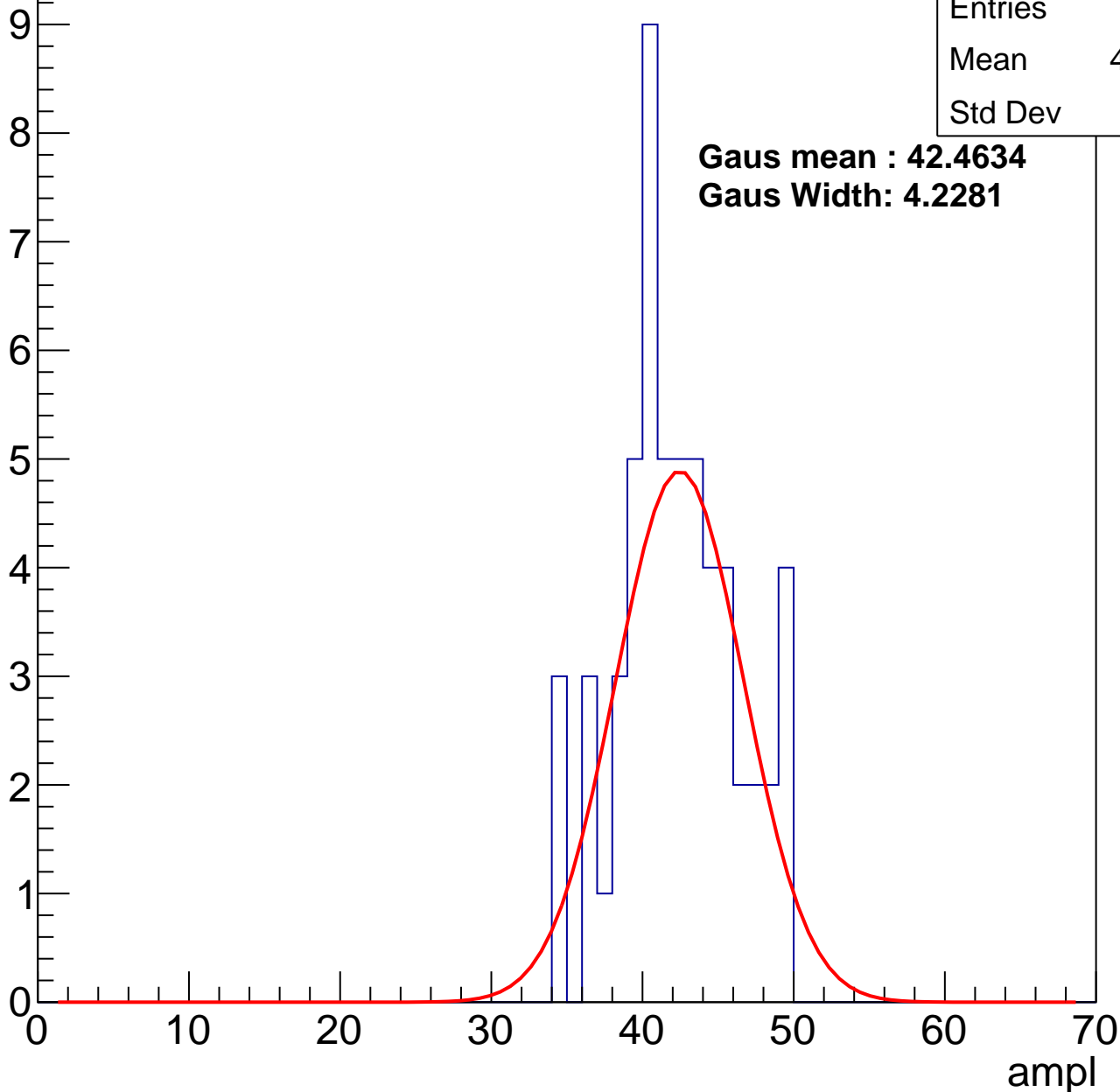
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	41.75
Std Dev	3.89

**Gaus mean : 42.4634**

**Gaus Width: 4.2281**

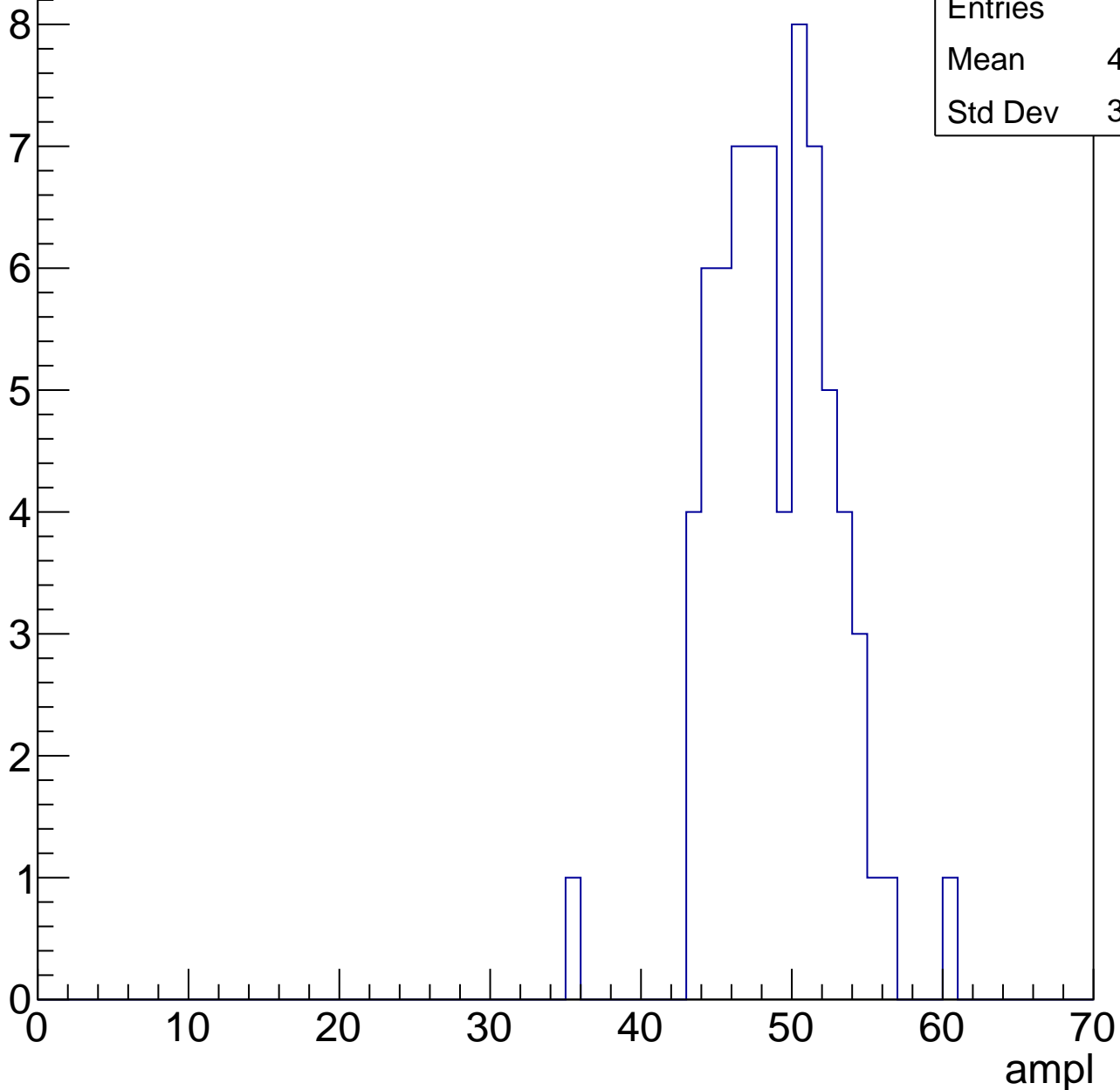


# B1L101S, U18-ch82, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	48.42
Std Dev	3.883

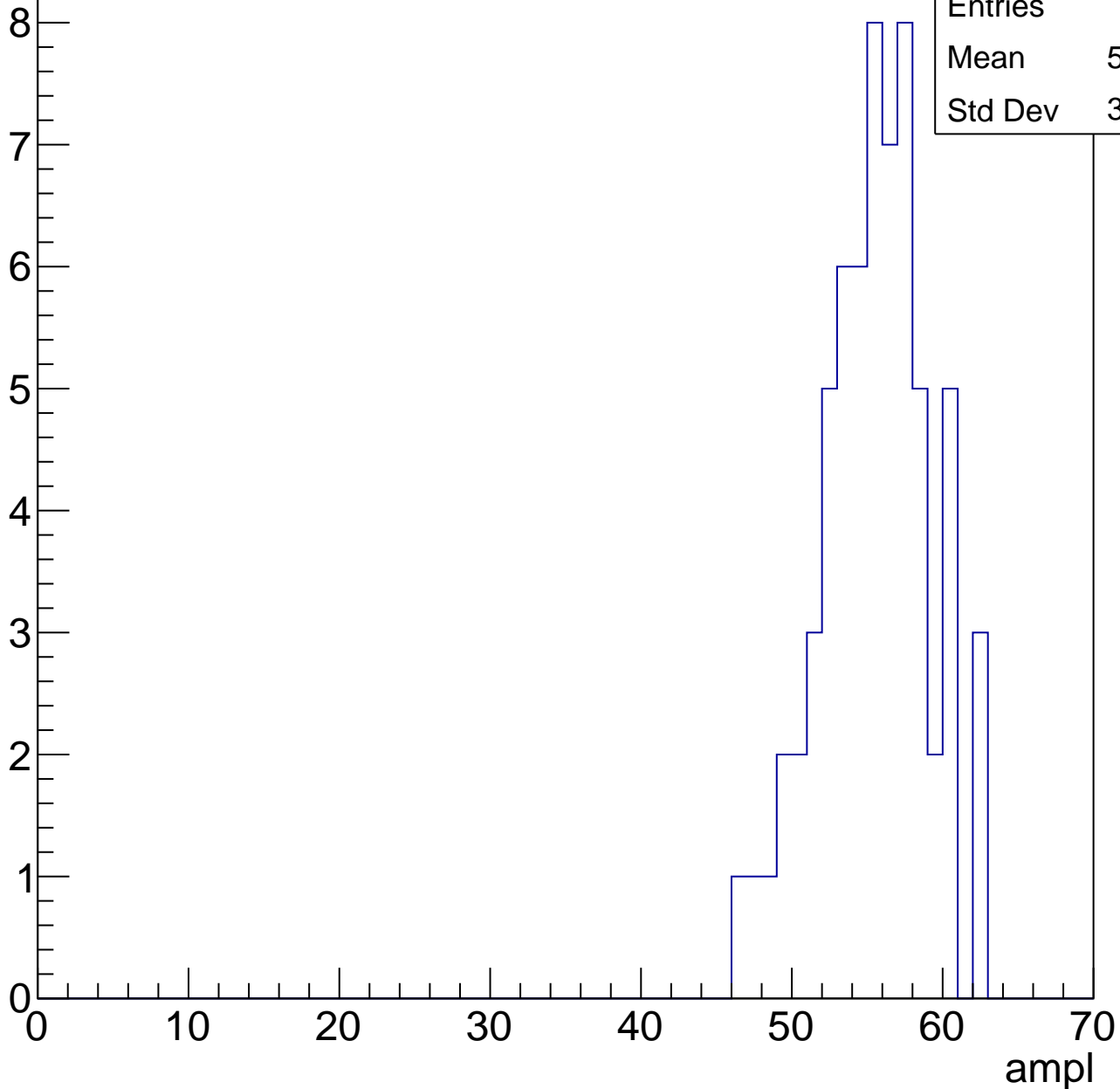


# B1L101S, U18-ch82, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	55.02
Std Dev	3.567

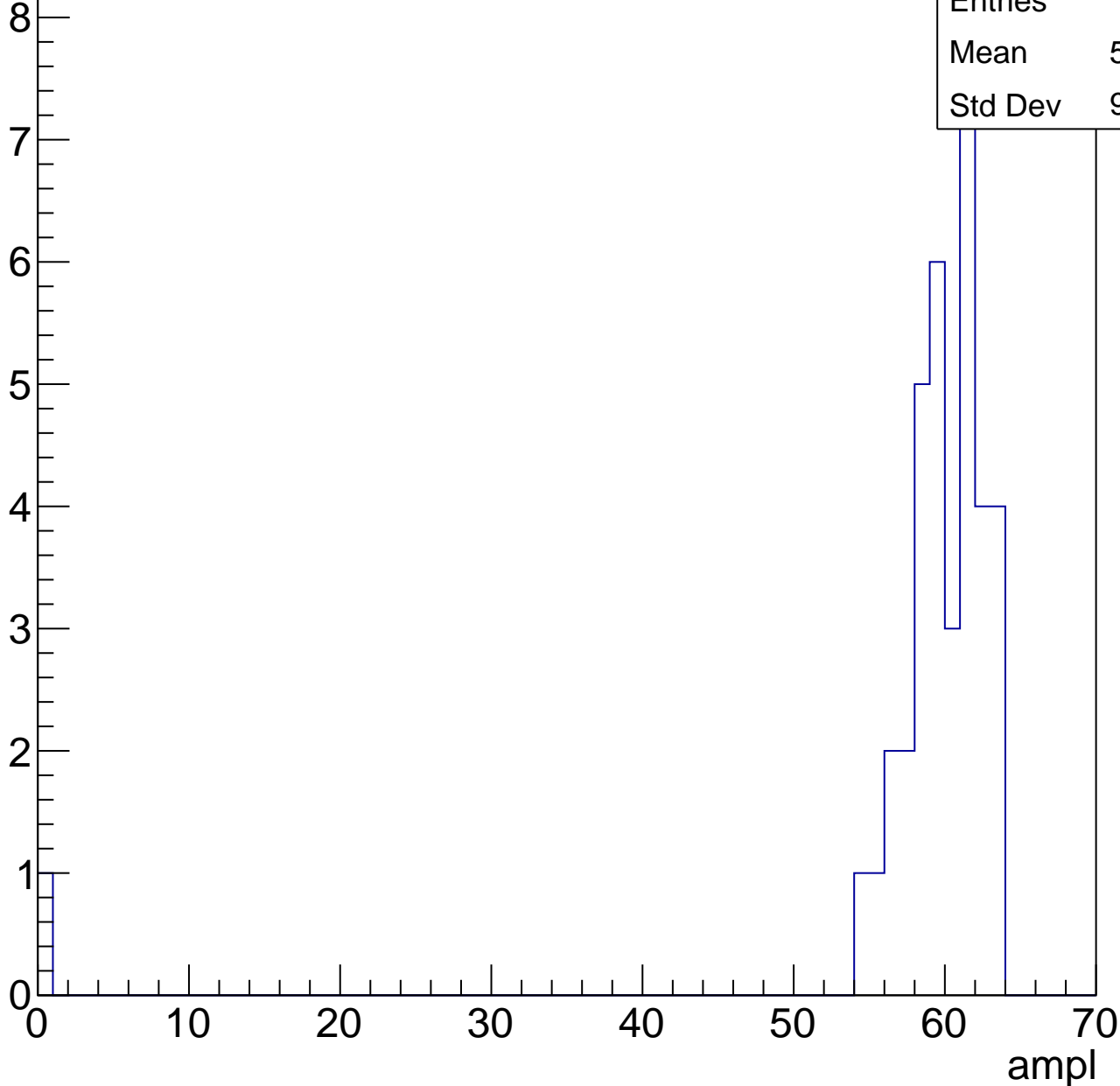


# B1L101S, U18-ch82, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

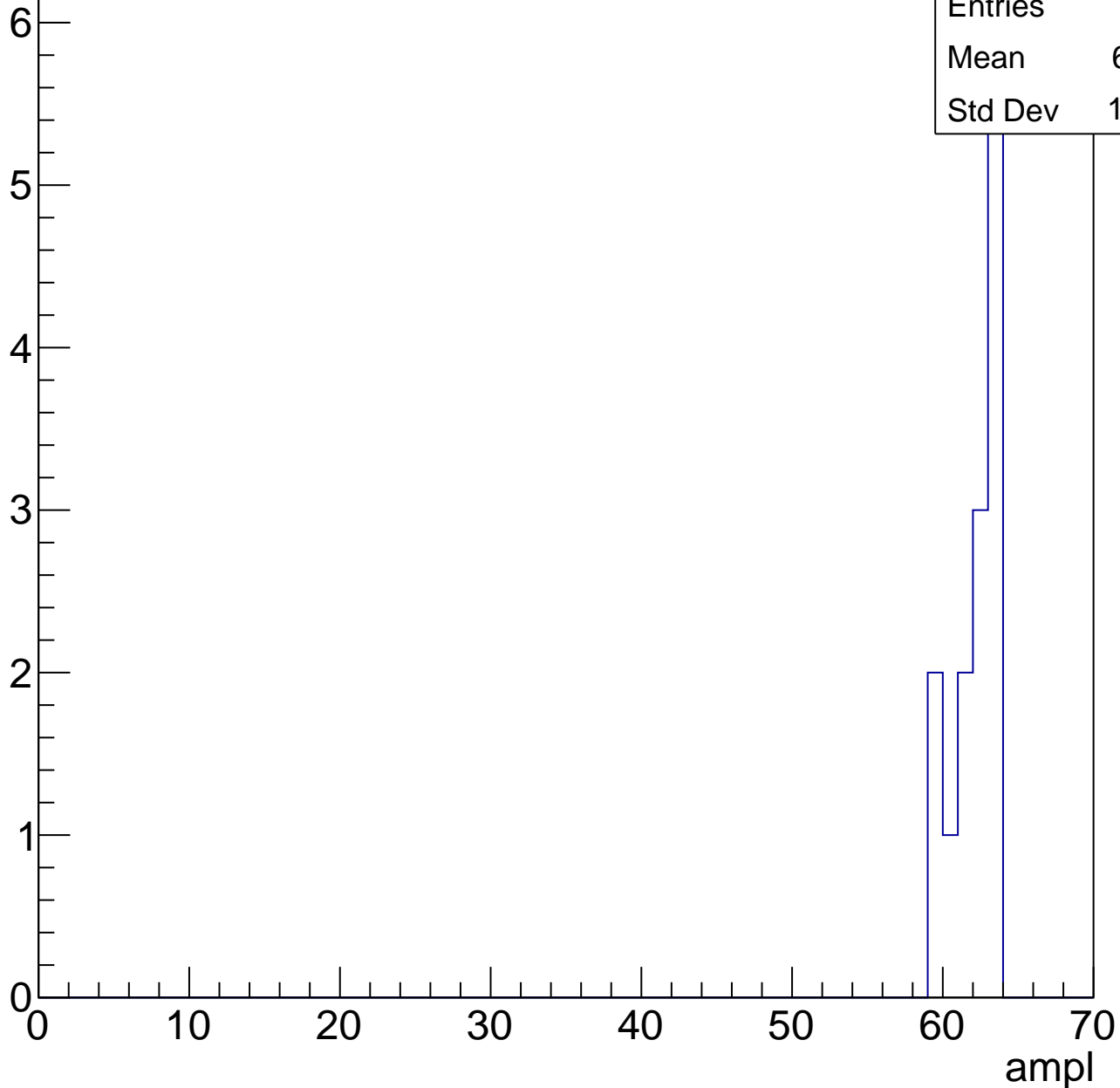
Entries	37
Mean	58.03
Std Dev	9.936



# B1L101S, U18-ch82, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	14
Mean	61.71
Std Dev	1.436



# B1L101S, U18-ch82, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U18-ch83, adc0

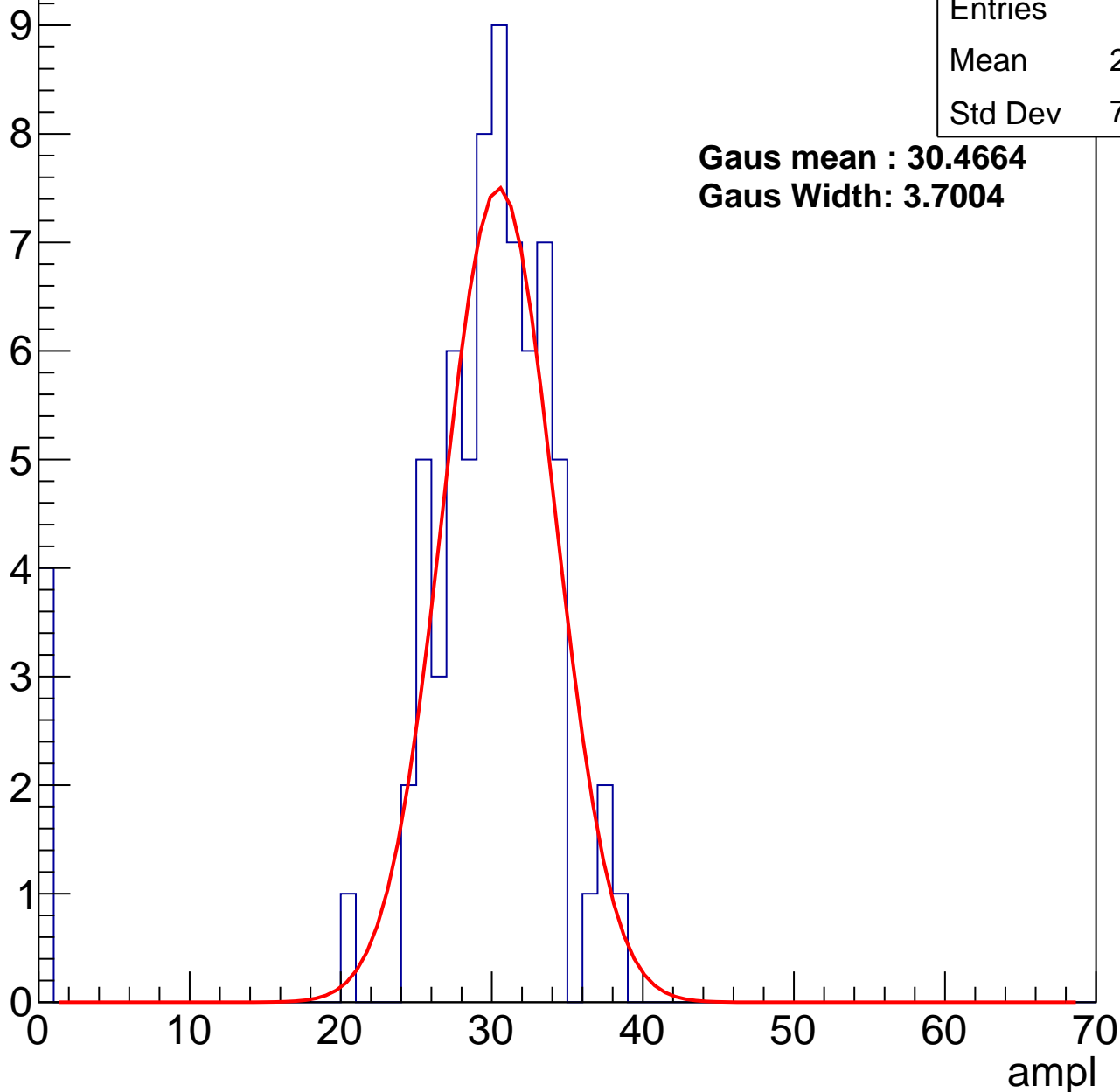
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	28.24
Std Dev	7.615

**Gaus mean : 30.4664**

**Gaus Width: 3.7004**



# B1L101S, U18-ch83, adc1

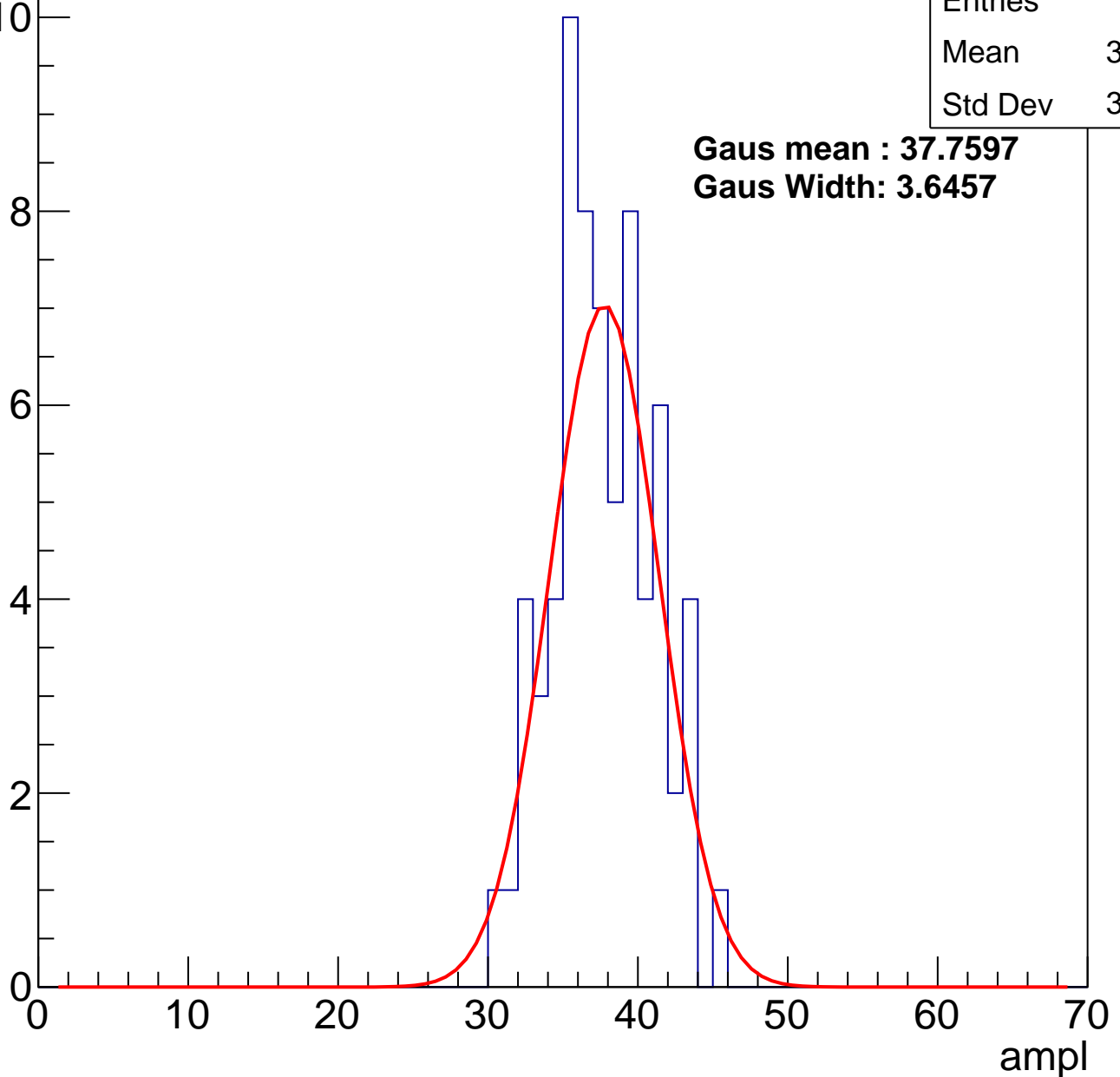
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	37.21
Std Dev	3.301

**Gaus mean : 37.7597**

**Gaus Width: 3.6457**



# B1L101S, U18-ch83, adc2

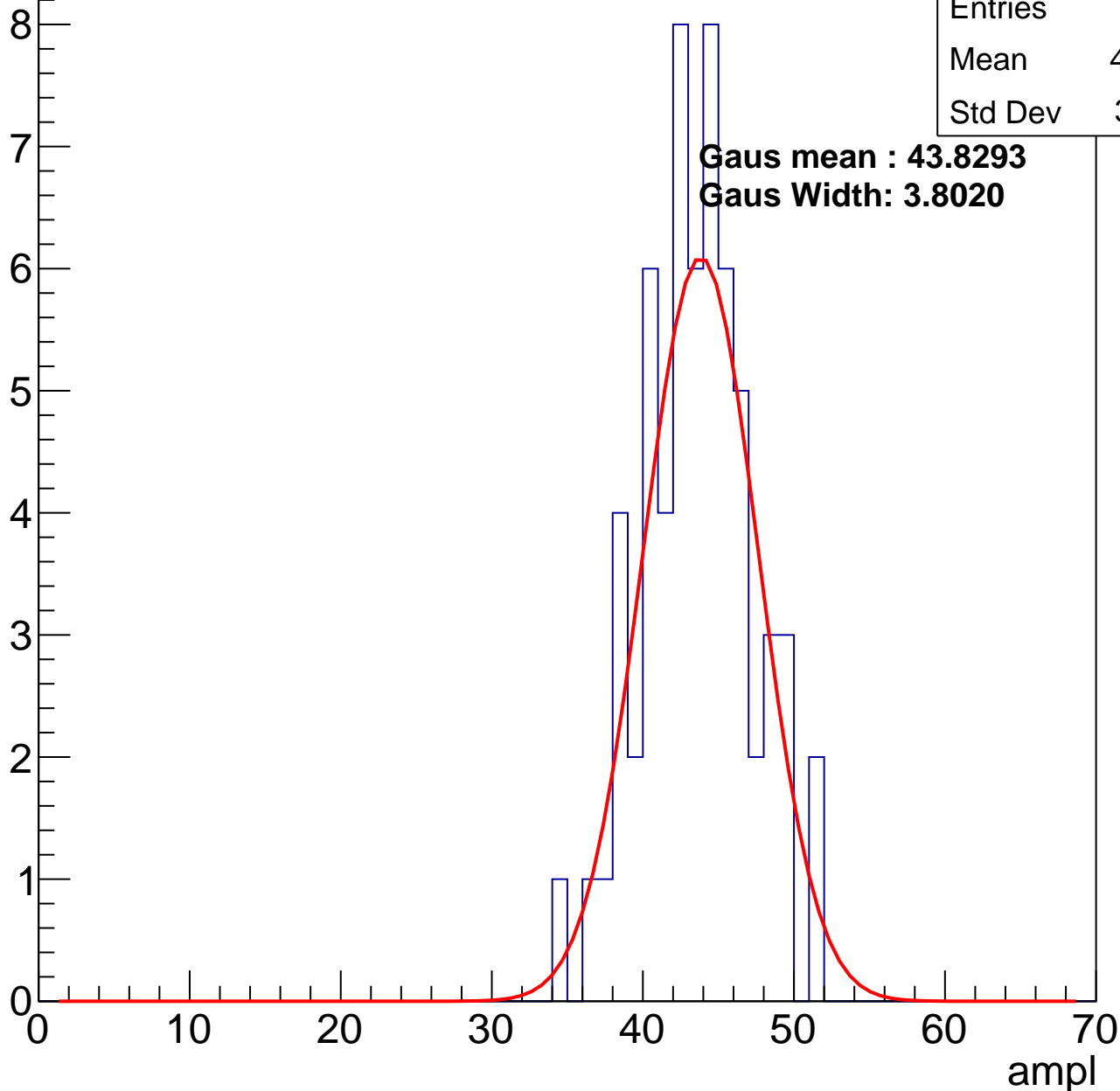
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	43.13
Std Dev	3.581

**Gaus mean : 43.8293**

**Gaus Width: 3.8020**

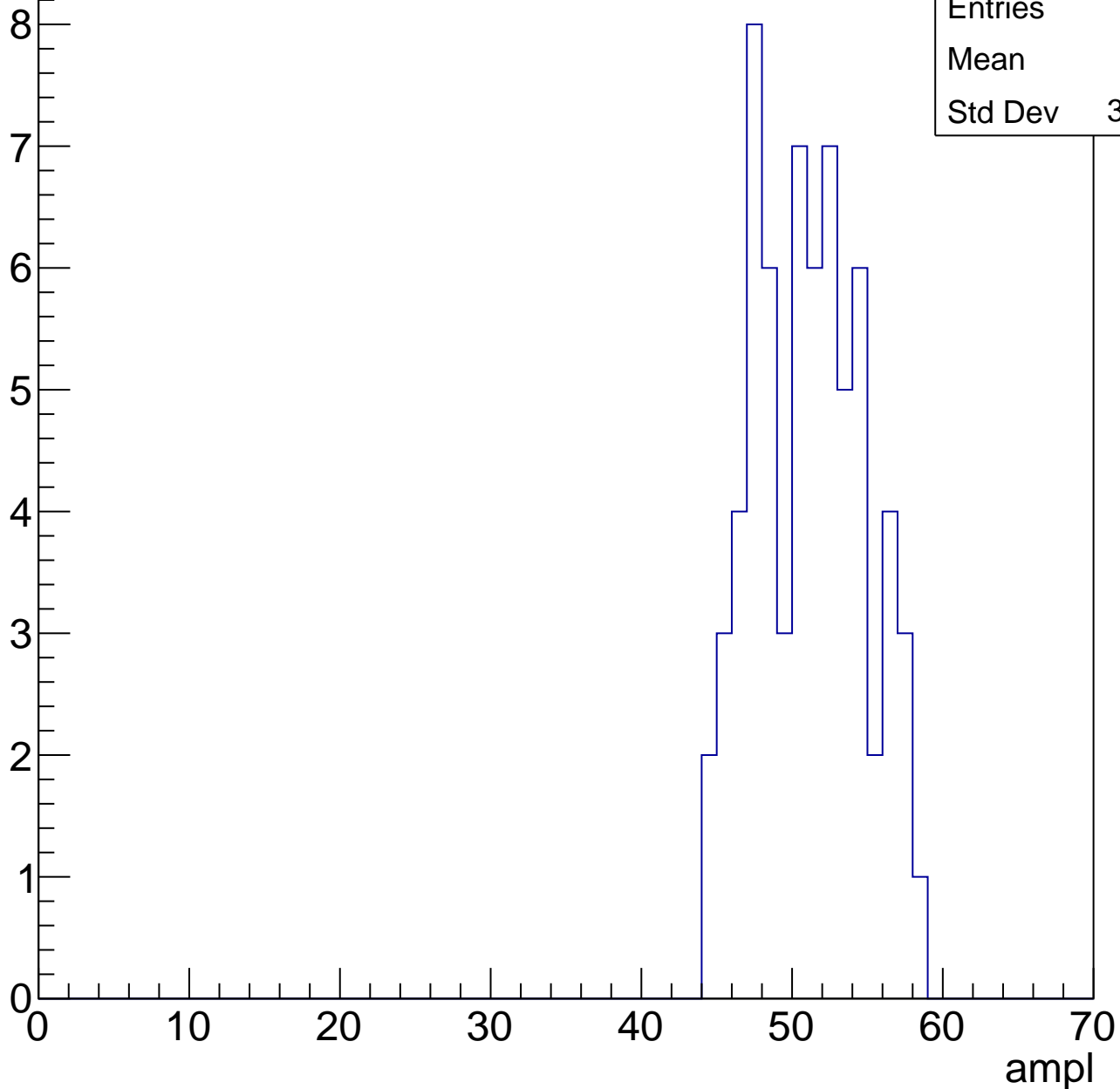


# B1L101S, U18-ch83, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	50.6
Std Dev	3.595

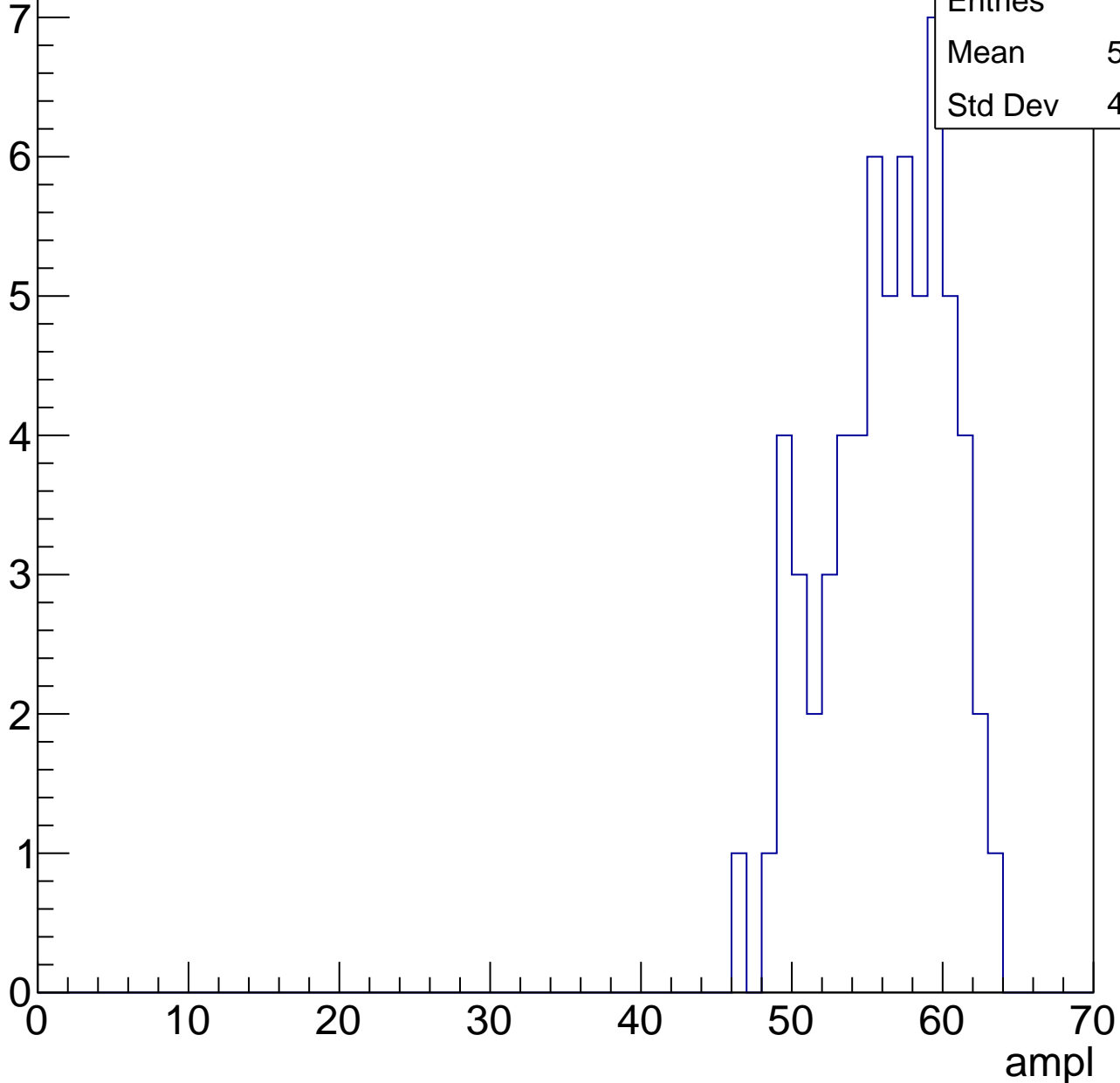


# B1L101S, U18-ch83, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

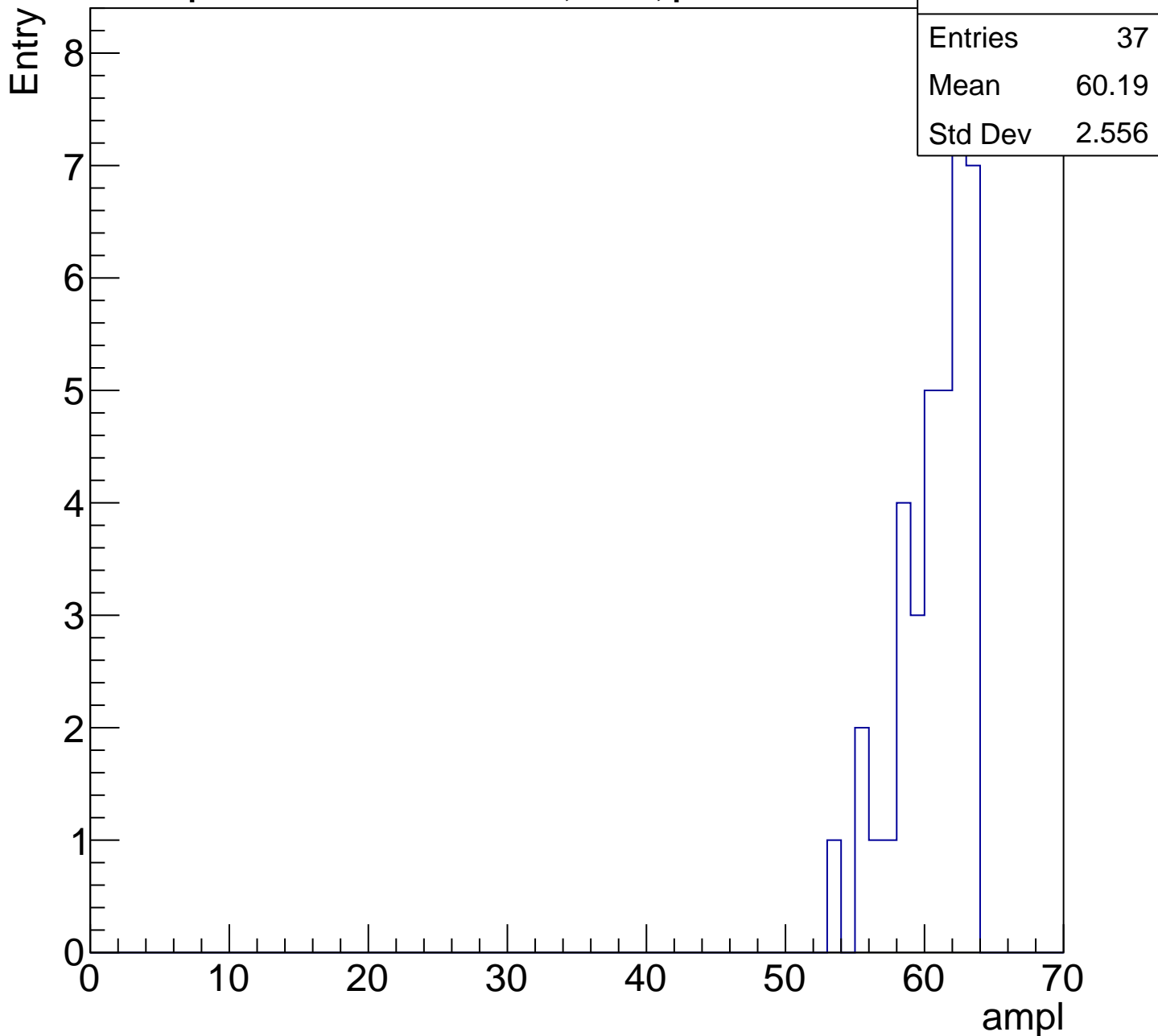
Entry

Entries	63
Mean	55.75
Std Dev	4.004



# B1L101S, U18-ch83, adc5

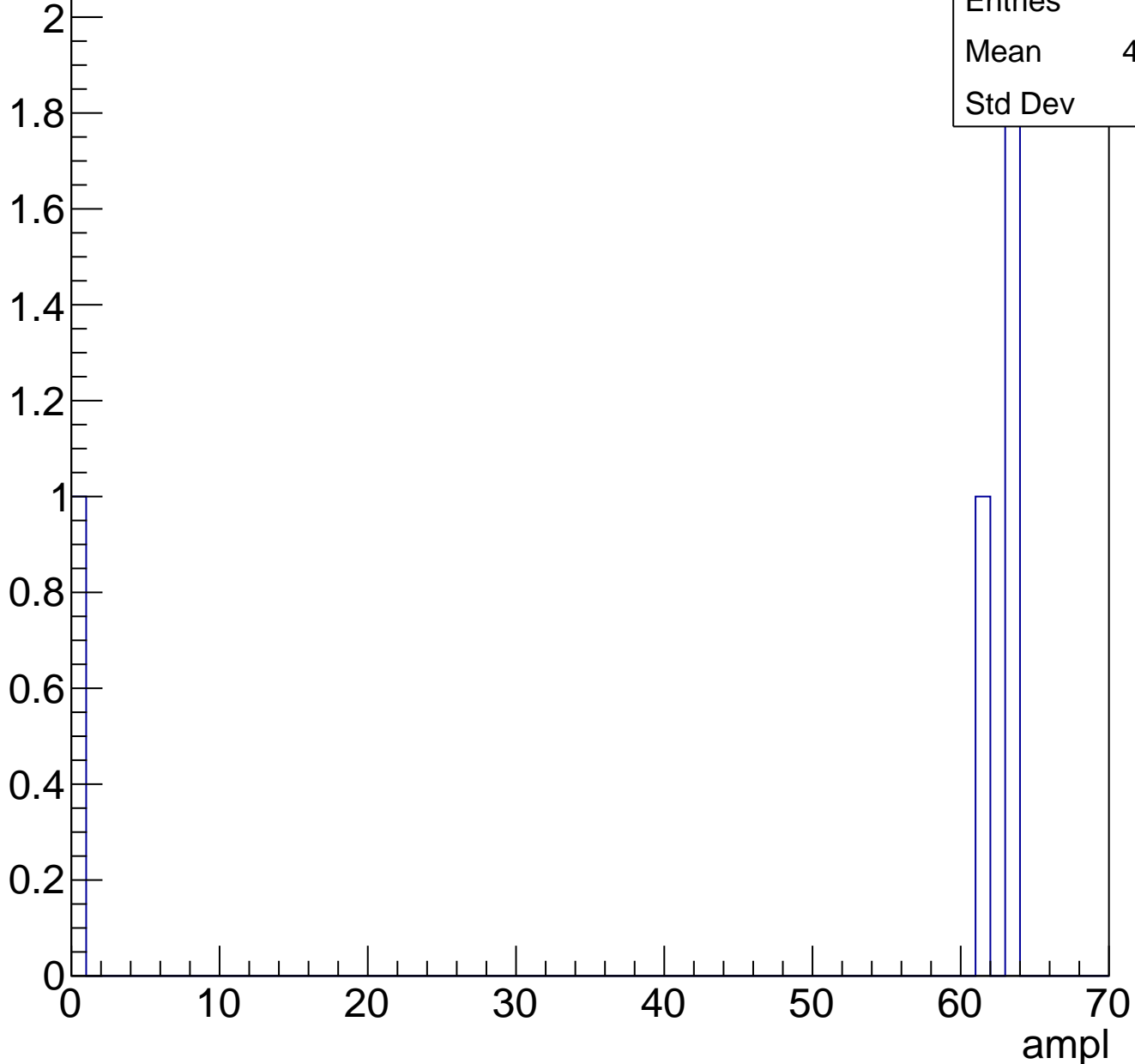
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U18-ch83, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	4
Mean	46.75
Std Dev	27



# B1L101S, U18-ch83, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L101S, U18-ch84, adc0

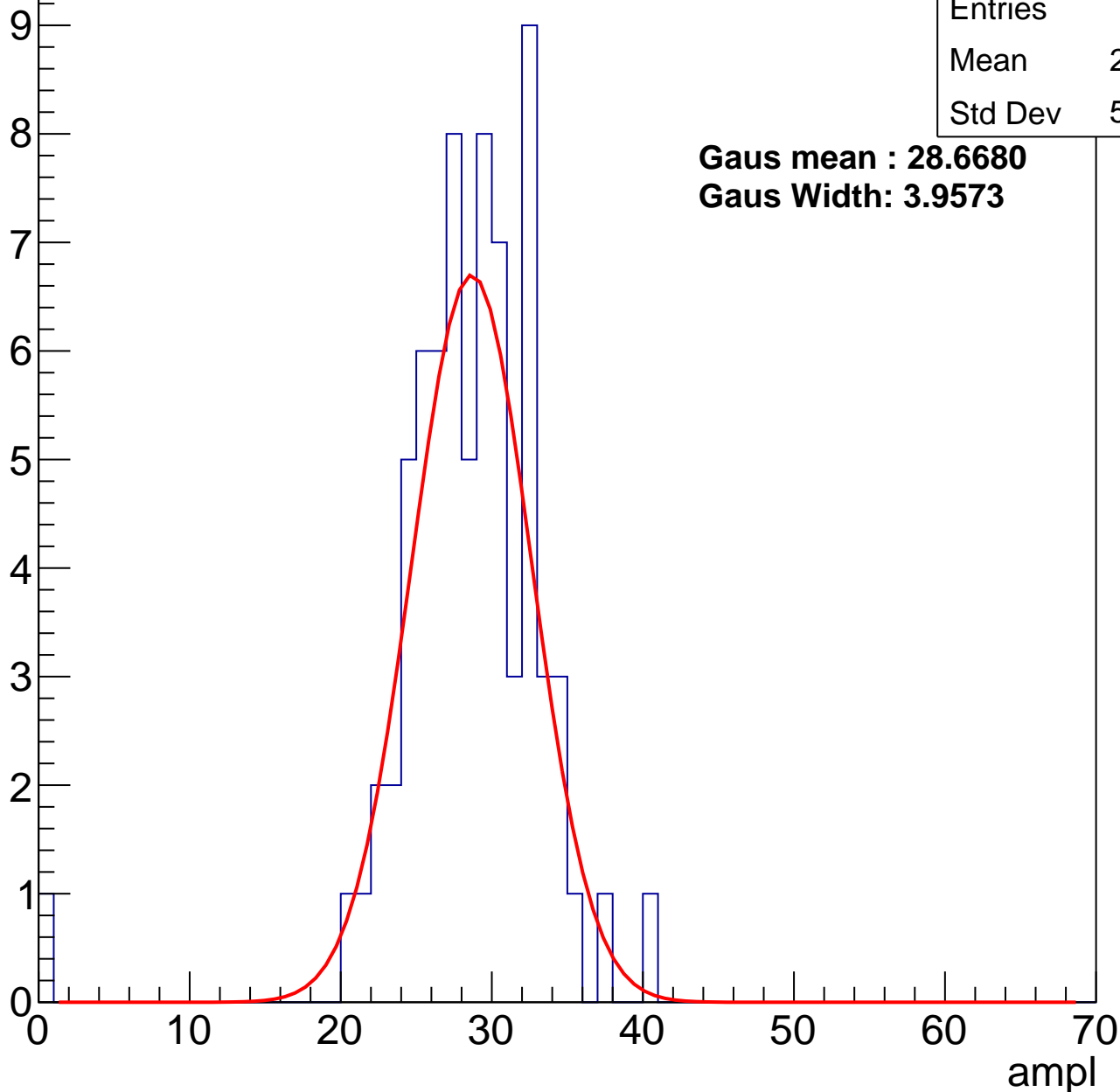
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	28.07
Std Dev	5.032

**Gaus mean : 28.6680**

**Gaus Width: 3.9573**



# B1L101S, U18-ch84, adc1

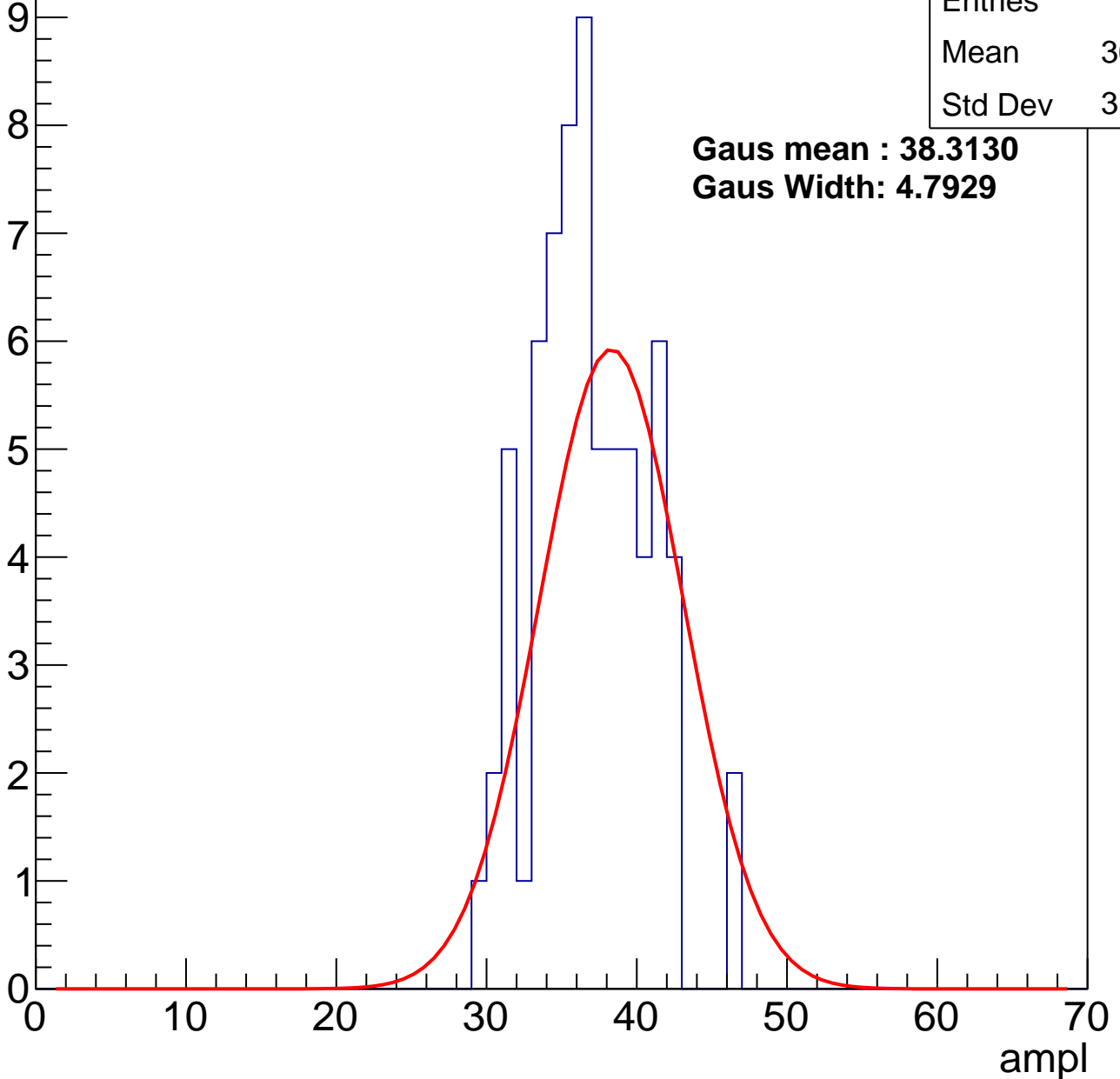
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	36.46
Std Dev	3.714

**Gaus mean : 38.3130**

**Gaus Width: 4.7929**



# B1L101S, U18-ch84, adc2

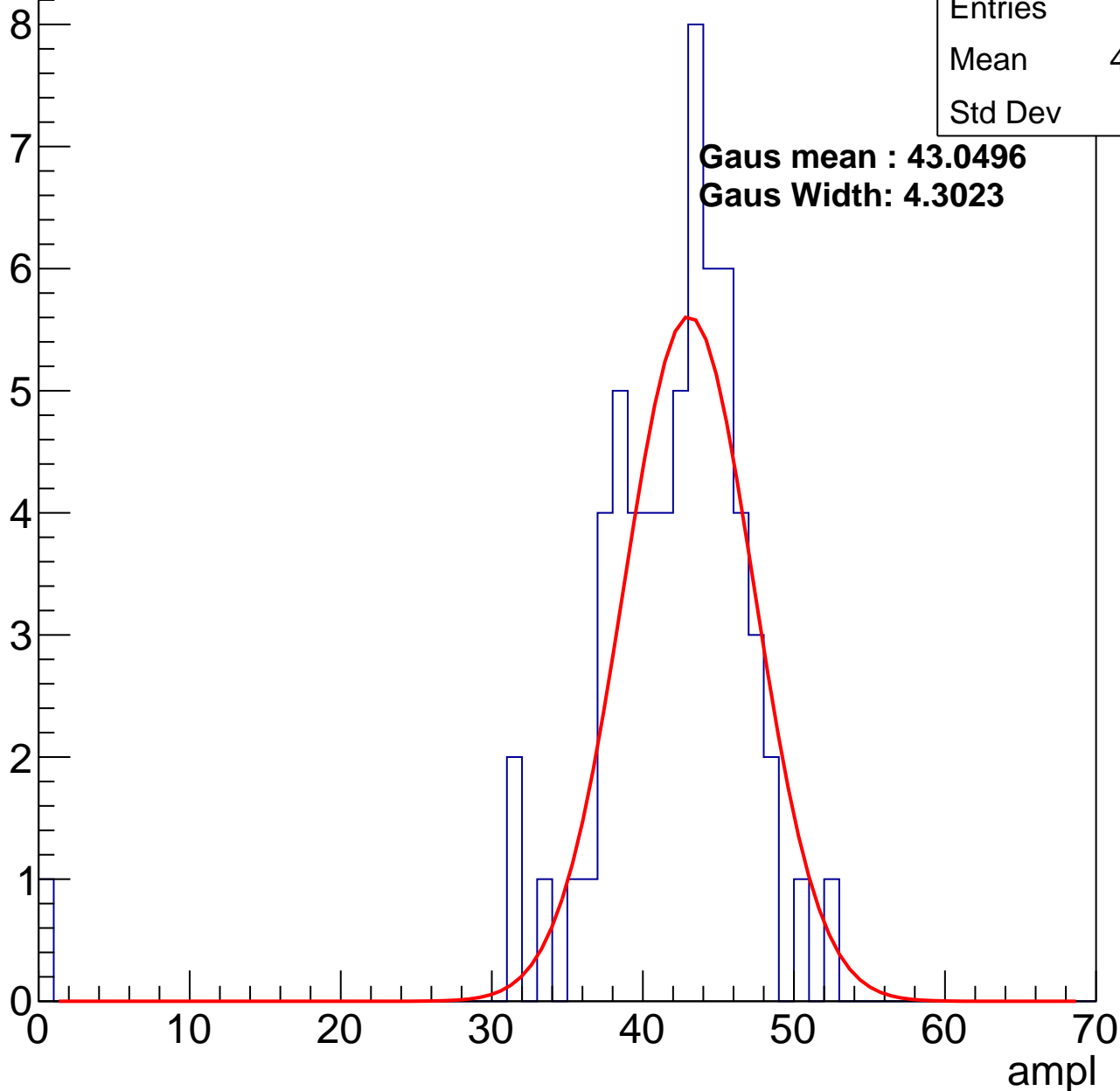
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	41.19
Std Dev	6.7

**Gaus mean : 43.0496**

**Gaus Width: 4.3023**

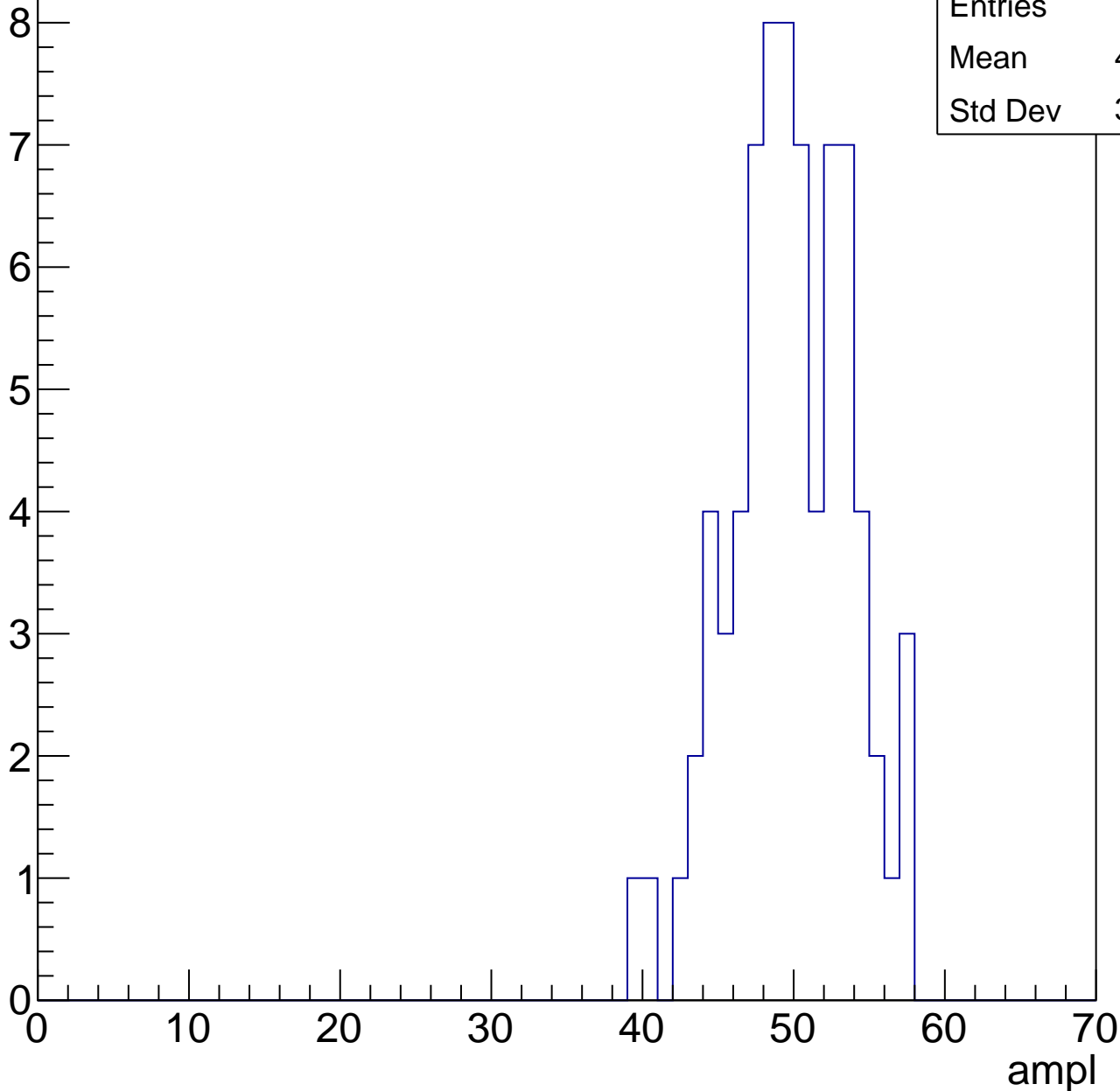


# B1L101S, U18-ch84, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	49.31
Std Dev	3.901

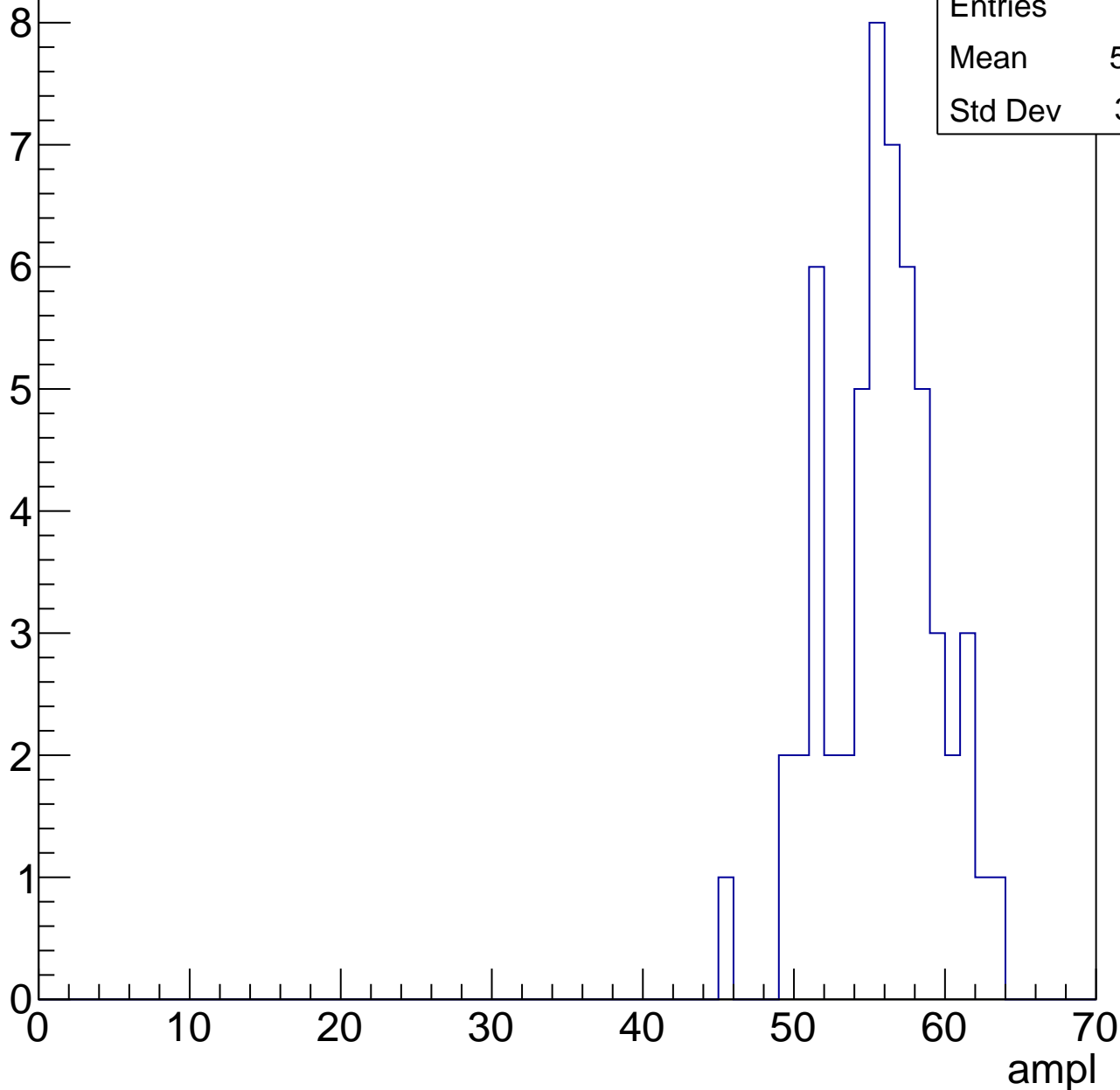


# B1L101S, U18-ch84, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	55.32
Std Dev	3.631

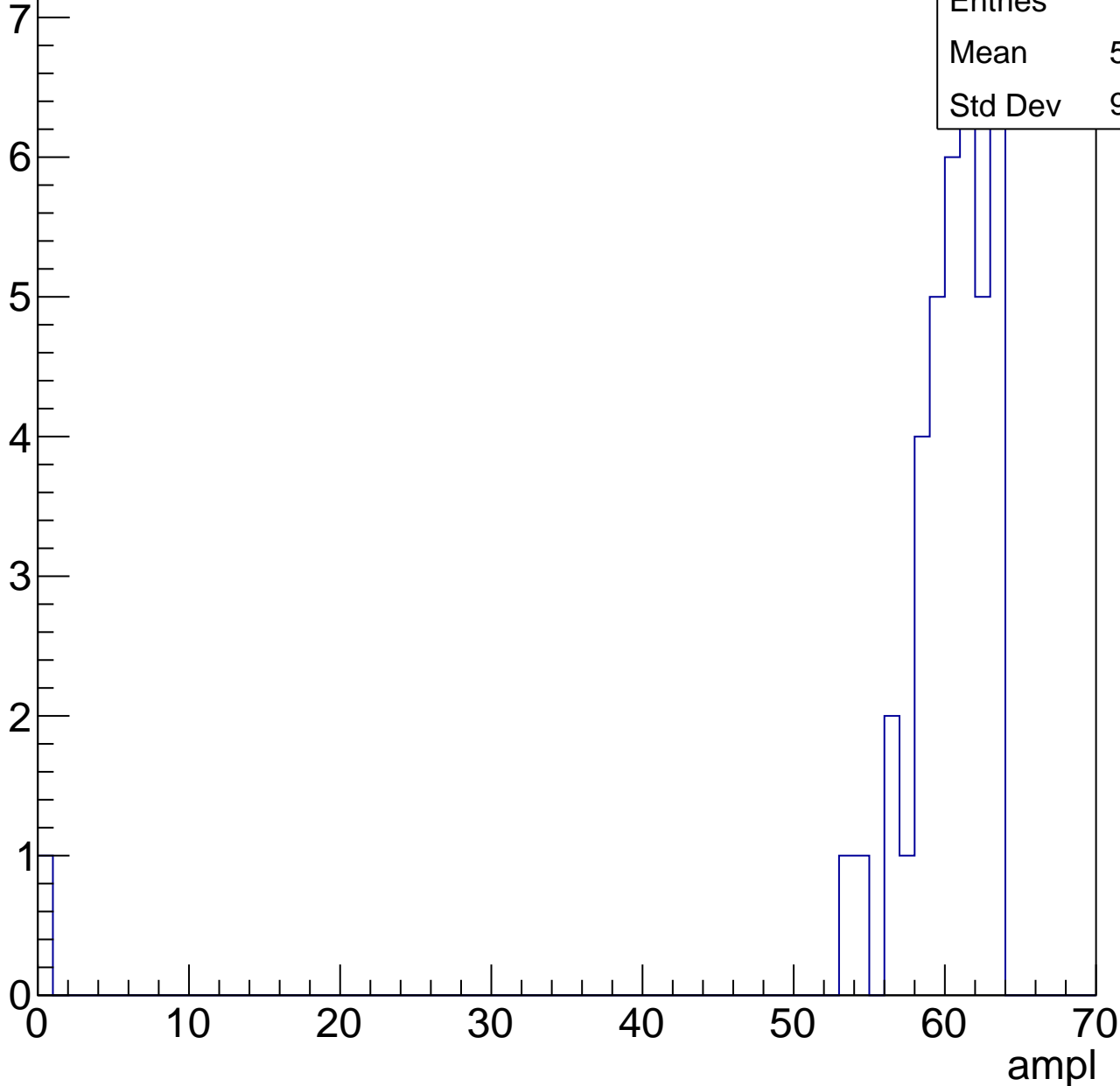


# B1L101S, U18-ch84, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

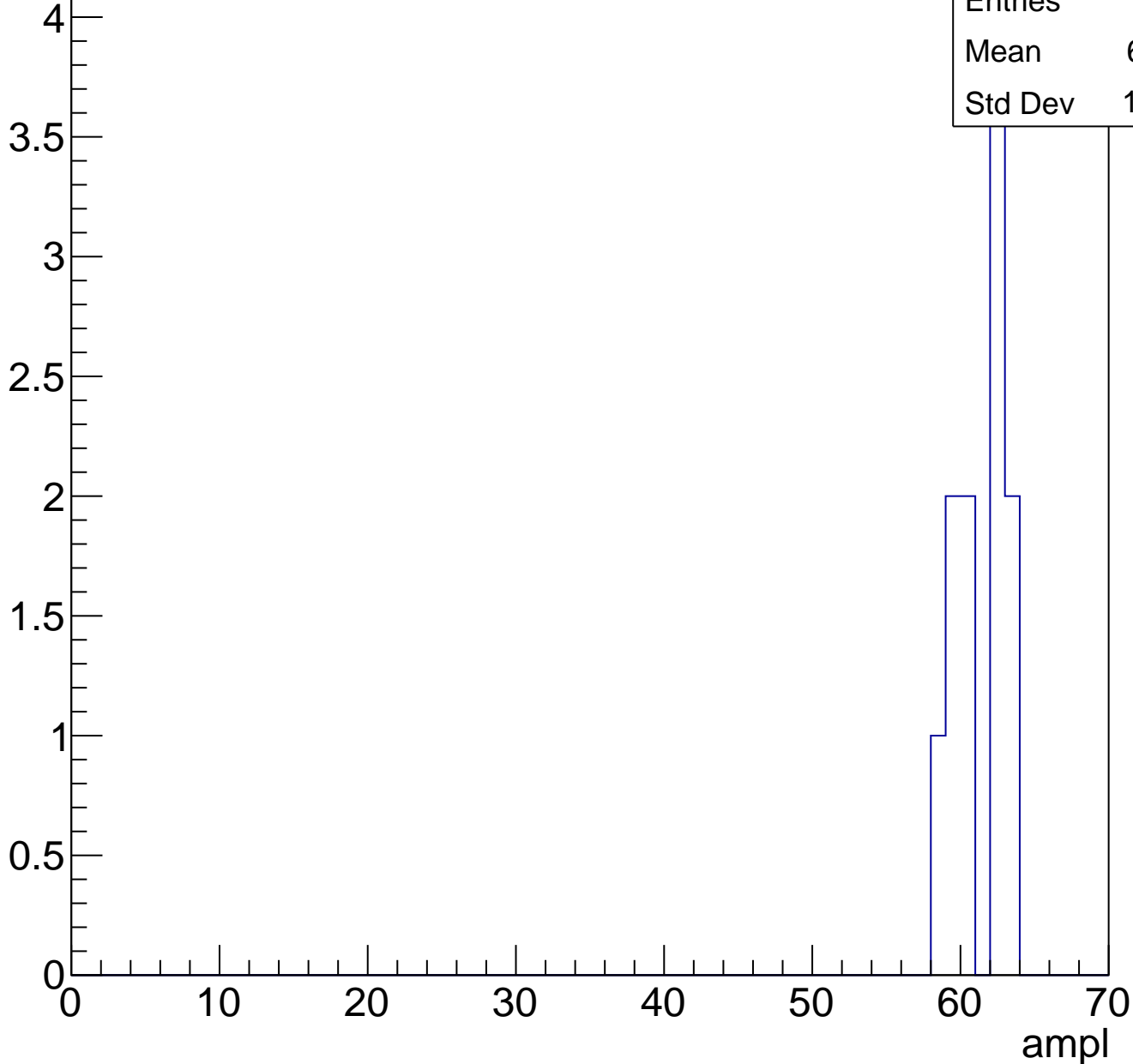
Entries	40
Mean	58.52
Std Dev	9.682



# B1L101S, U18-ch84, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch84, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U18-ch85, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	67
Mean	27.67
Std Dev	8.613

**Gaus mean : 30.4442**

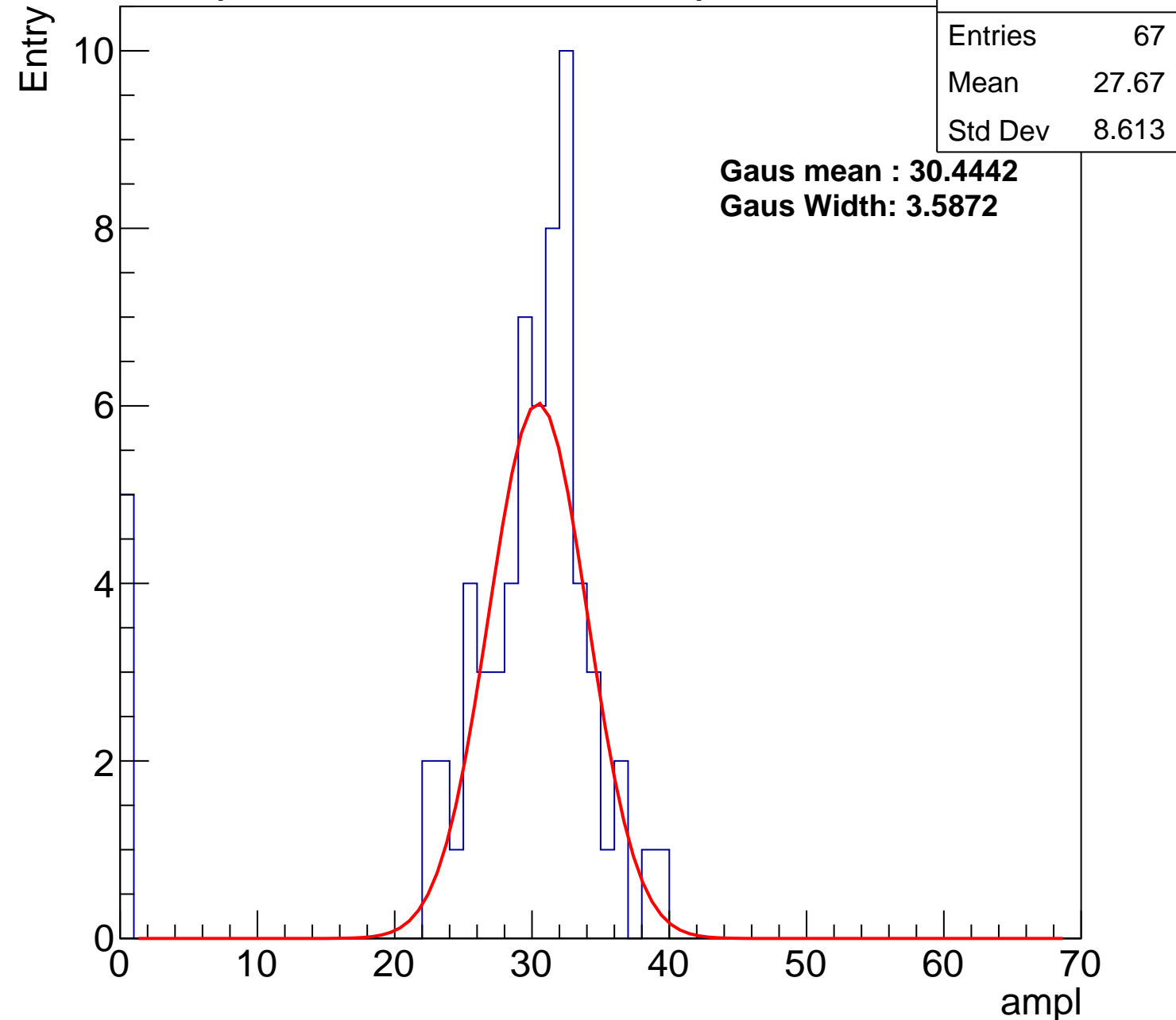
**Gaus Width: 3.5872**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



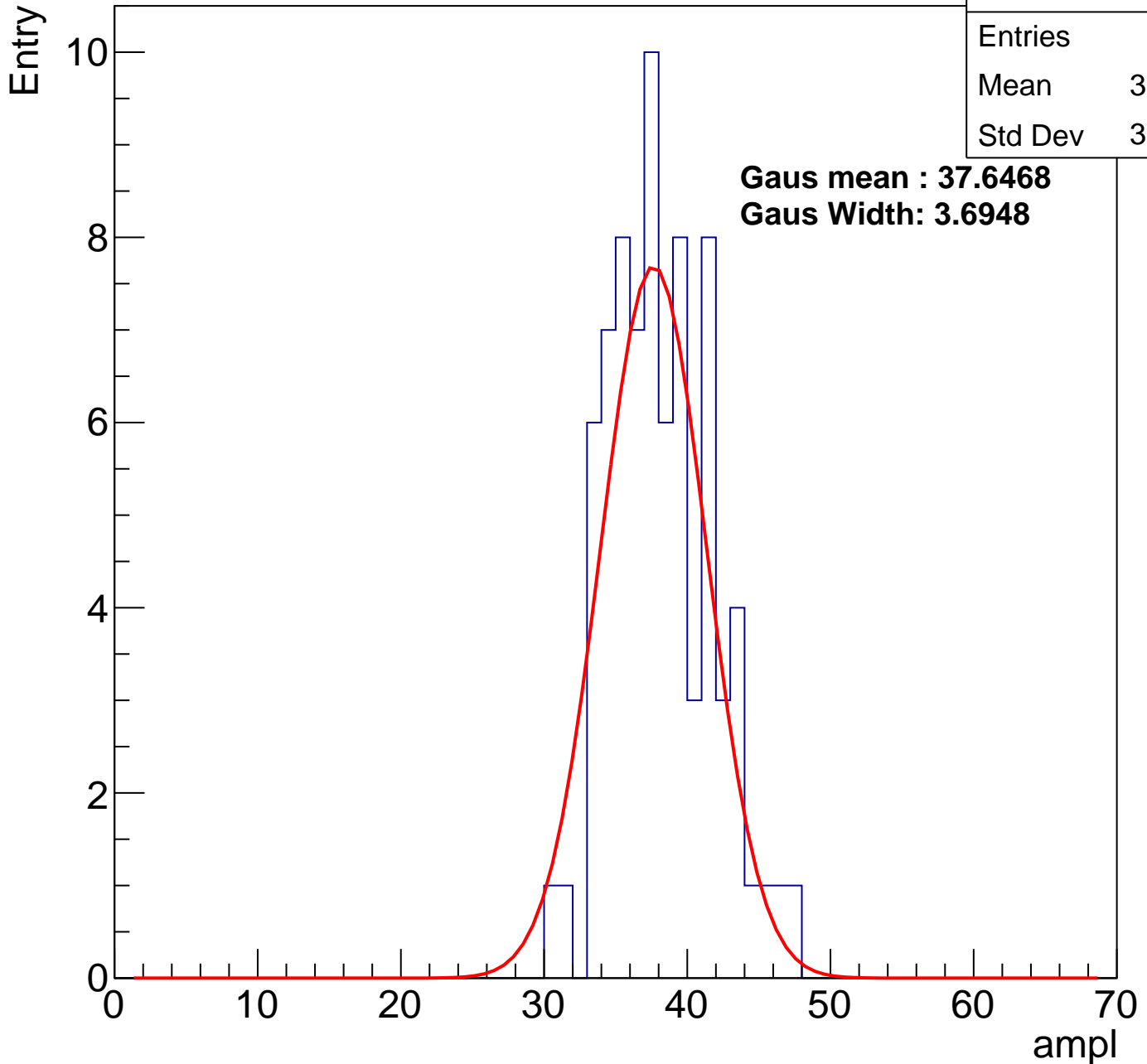
# B1L101S, U18-ch85, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	76
Mean	37.72
Std Dev	3.534

**Gaus mean : 37.6468**

**Gaus Width: 3.6948**



# B1L101S, U18-ch85, adc2

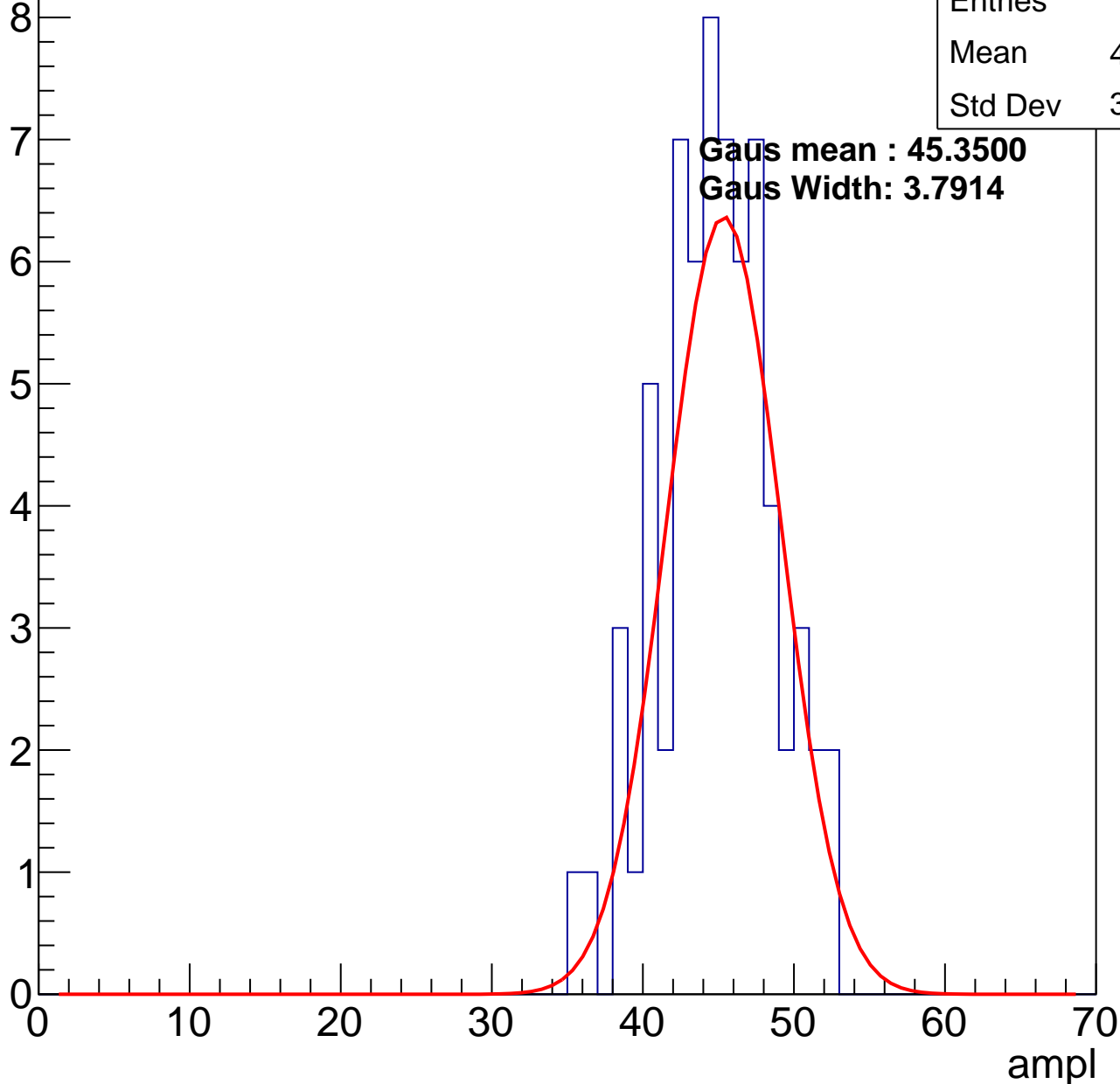
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	44.42
Std Dev	3.746

**Gaus mean : 45.3500**

**Gaus Width: 3.7914**

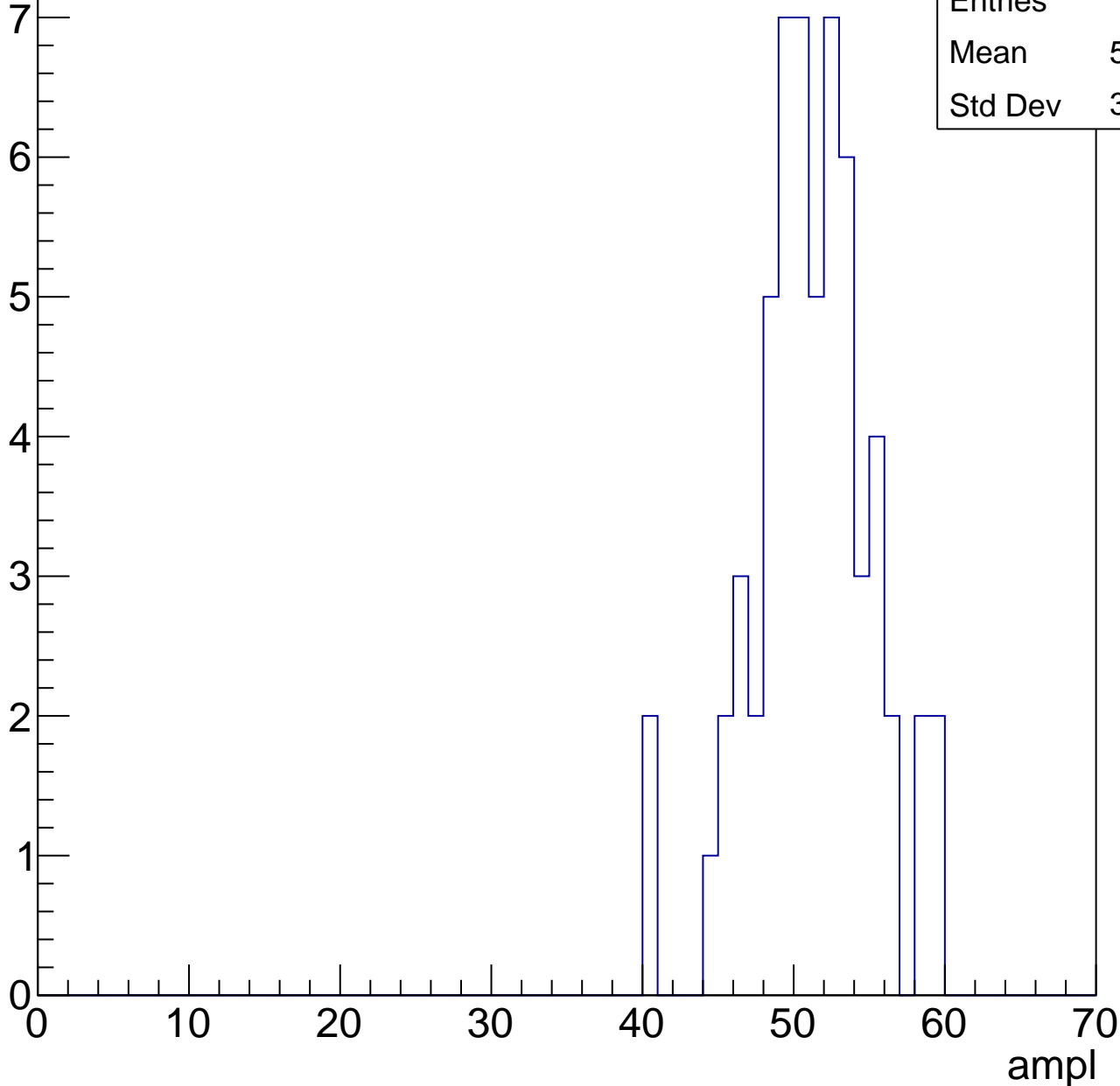


# B1L101S, U18-ch85, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	50.73
Std Dev	3.966

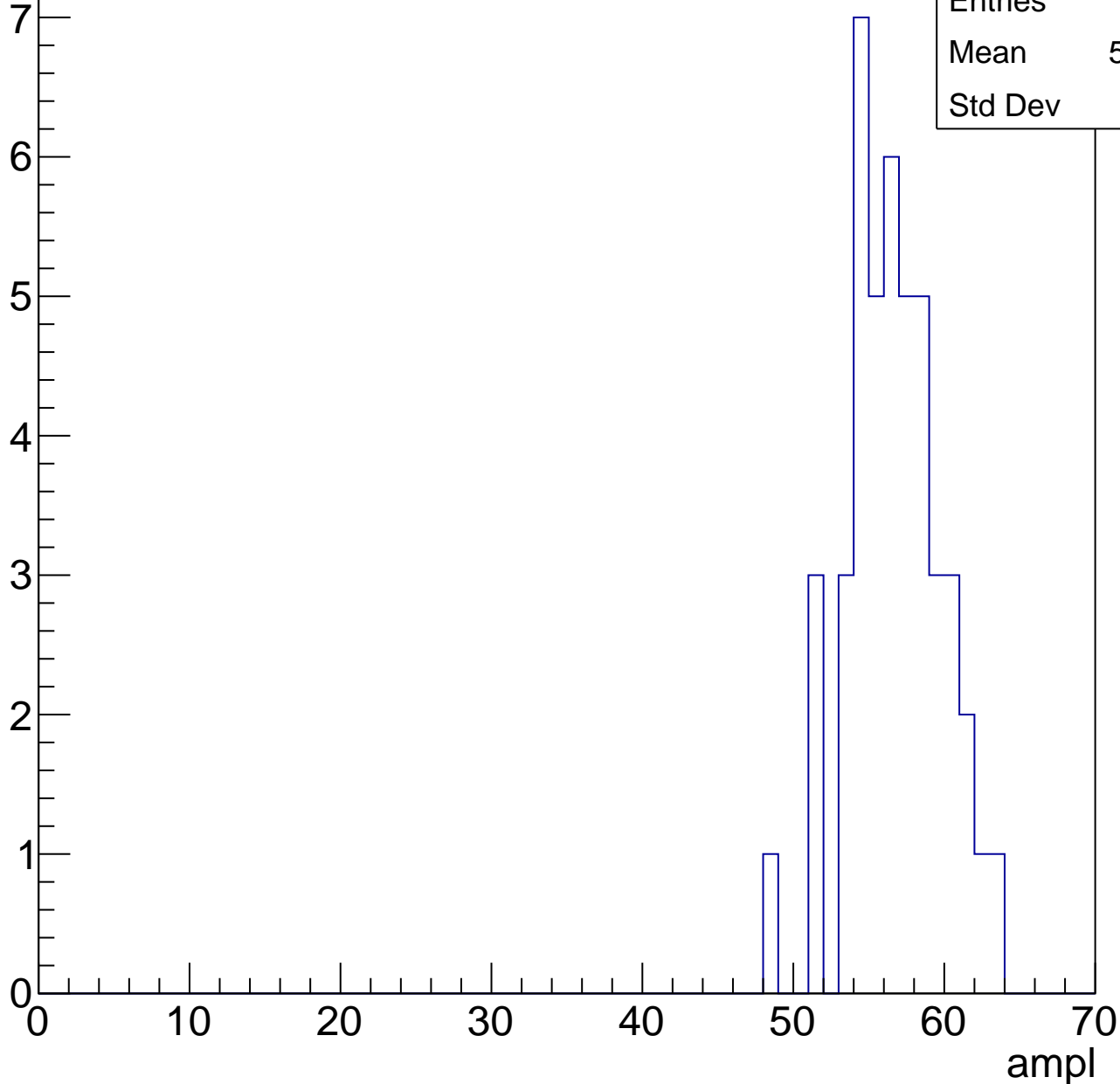


# B1L101S, U18-ch85, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	45
Mean	56.18
Std Dev	3.1

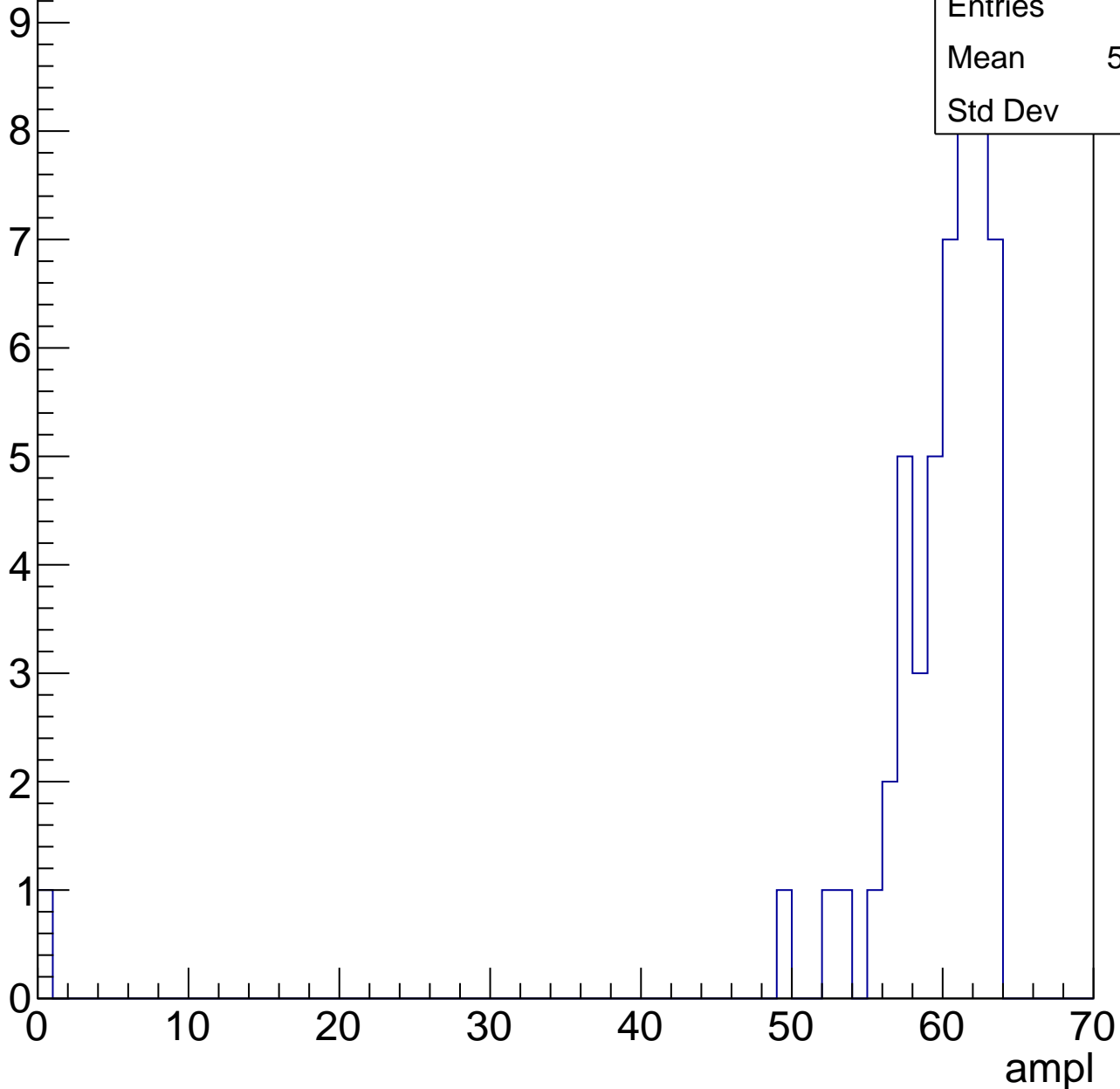


# B1L101S, U18-ch85, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	58.47
Std Dev	8.79



# B1L101S, U18-ch85, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch85, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U18-ch86, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	69
Mean	29.33
Std Dev	4.817

**Gaus mean : 30.2753**

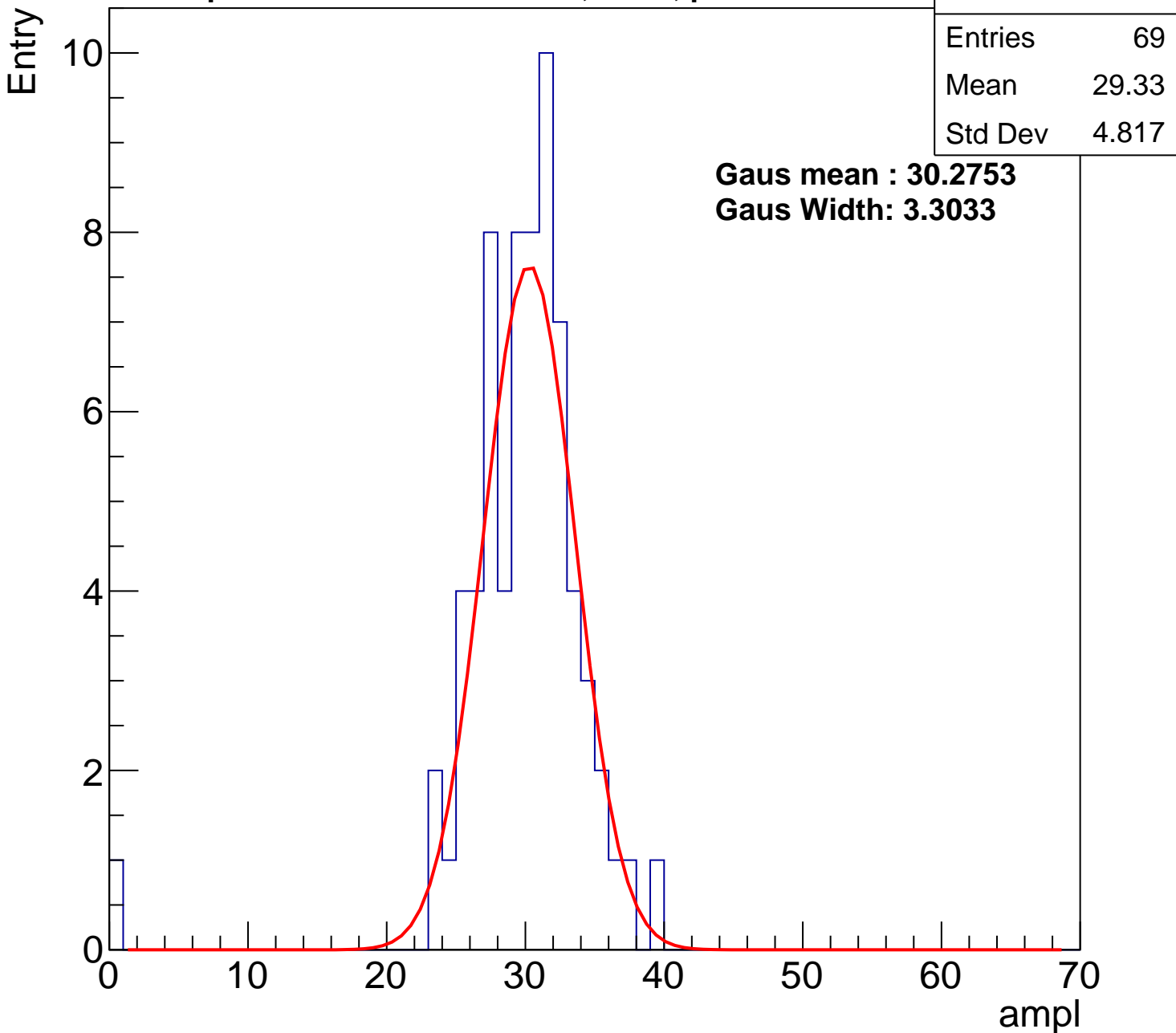
**Gaus Width: 3.3033**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U18-ch86, adc1

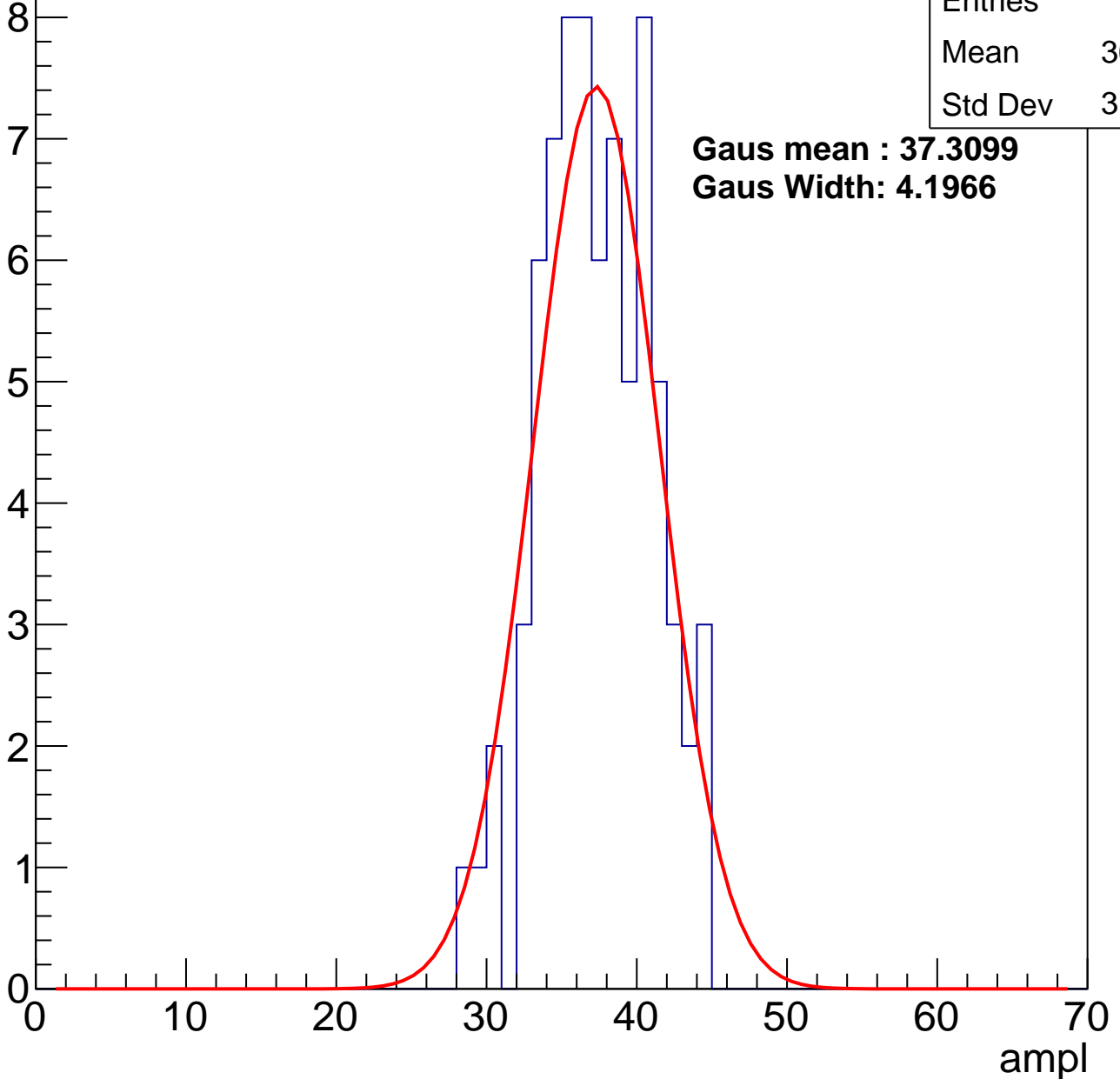
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	36.92
Std Dev	3.632

**Gaus mean : 37.3099**

**Gaus Width: 4.1966**



# B1L101S, U18-ch86, adc2

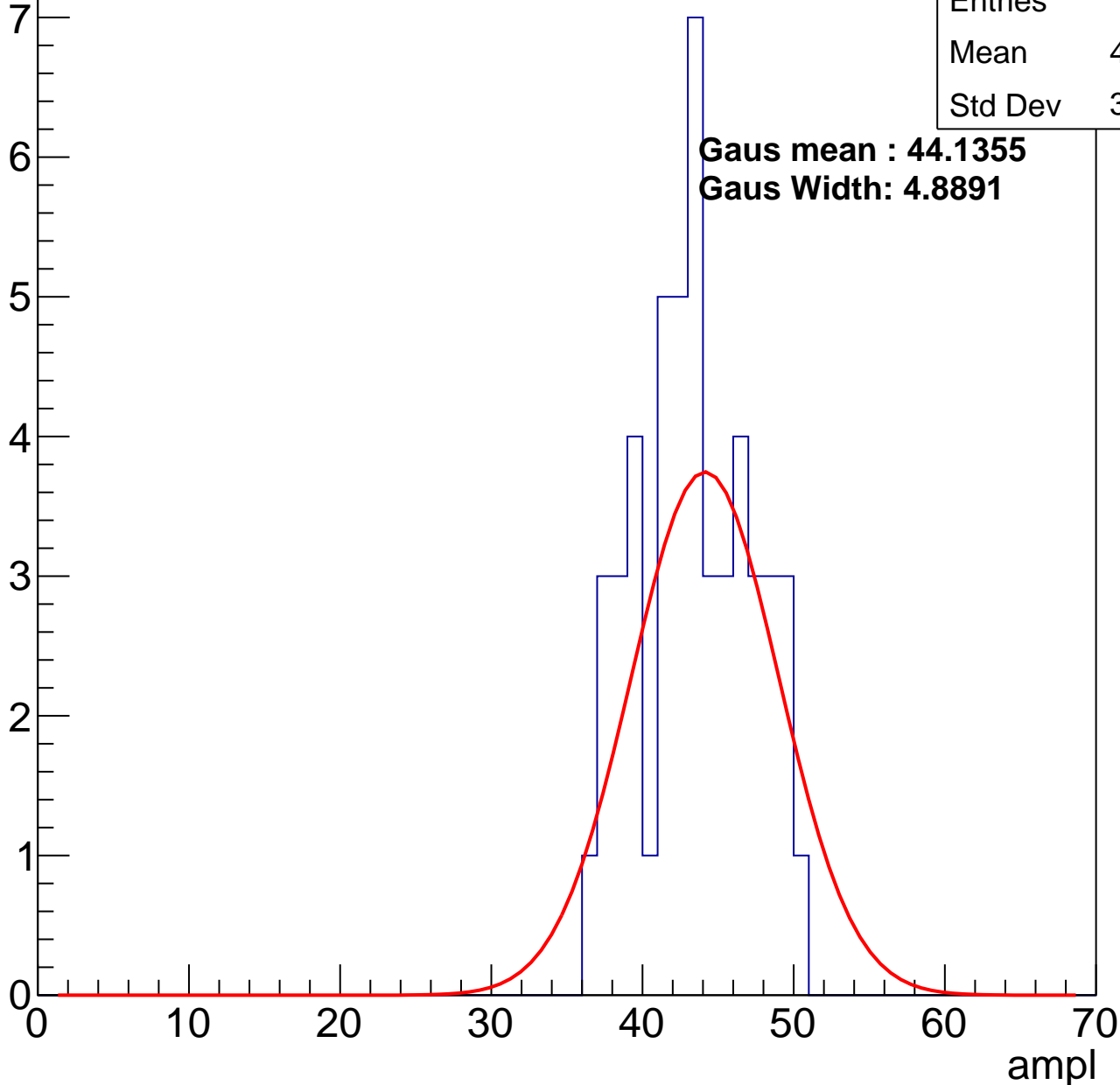
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	49
Mean	42.98
Std Dev	3.673

**Gaus mean : 44.1355**

**Gaus Width: 4.8891**

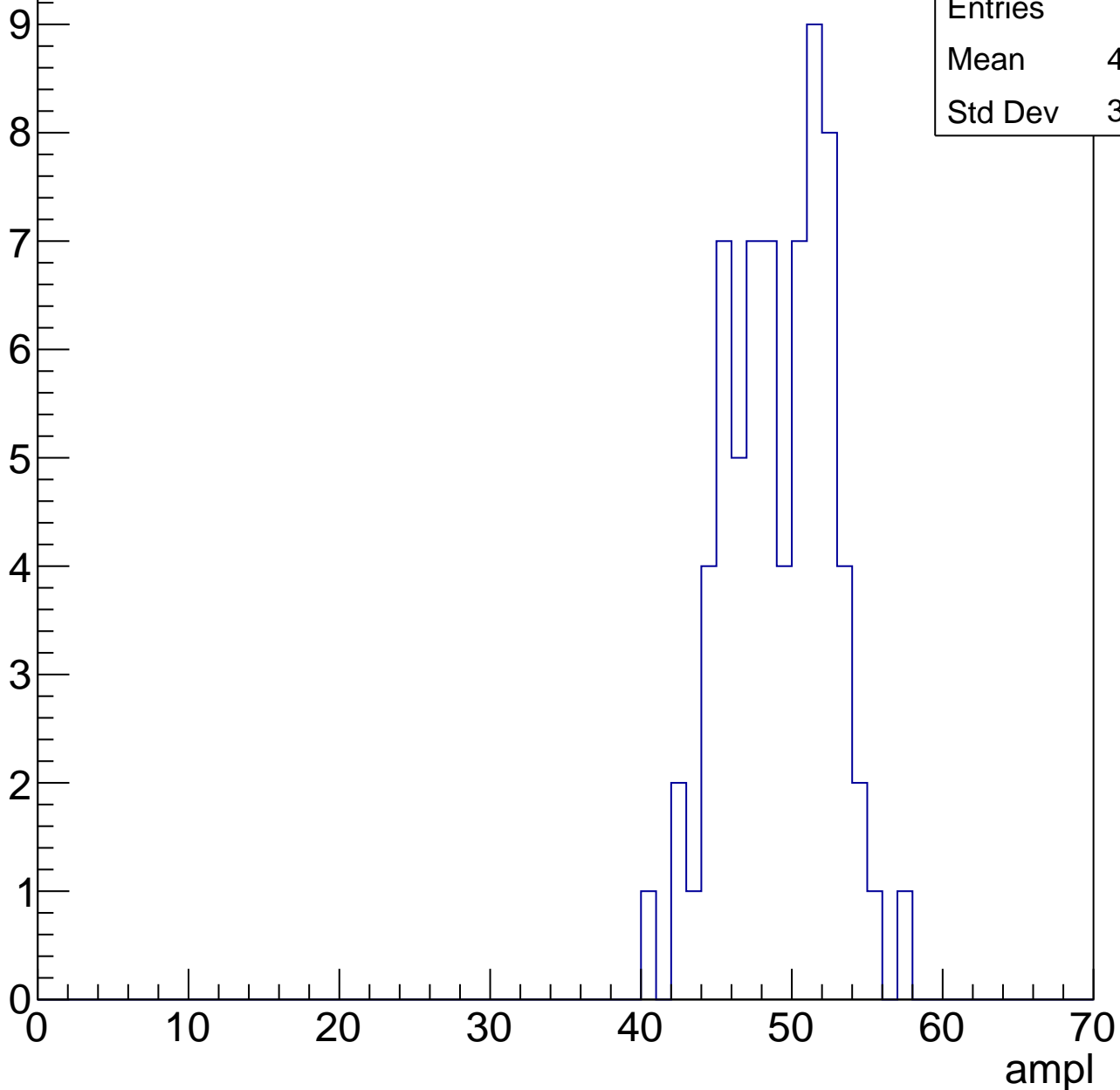


# B1L101S, U18-ch86, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	48.66
Std Dev	3.439

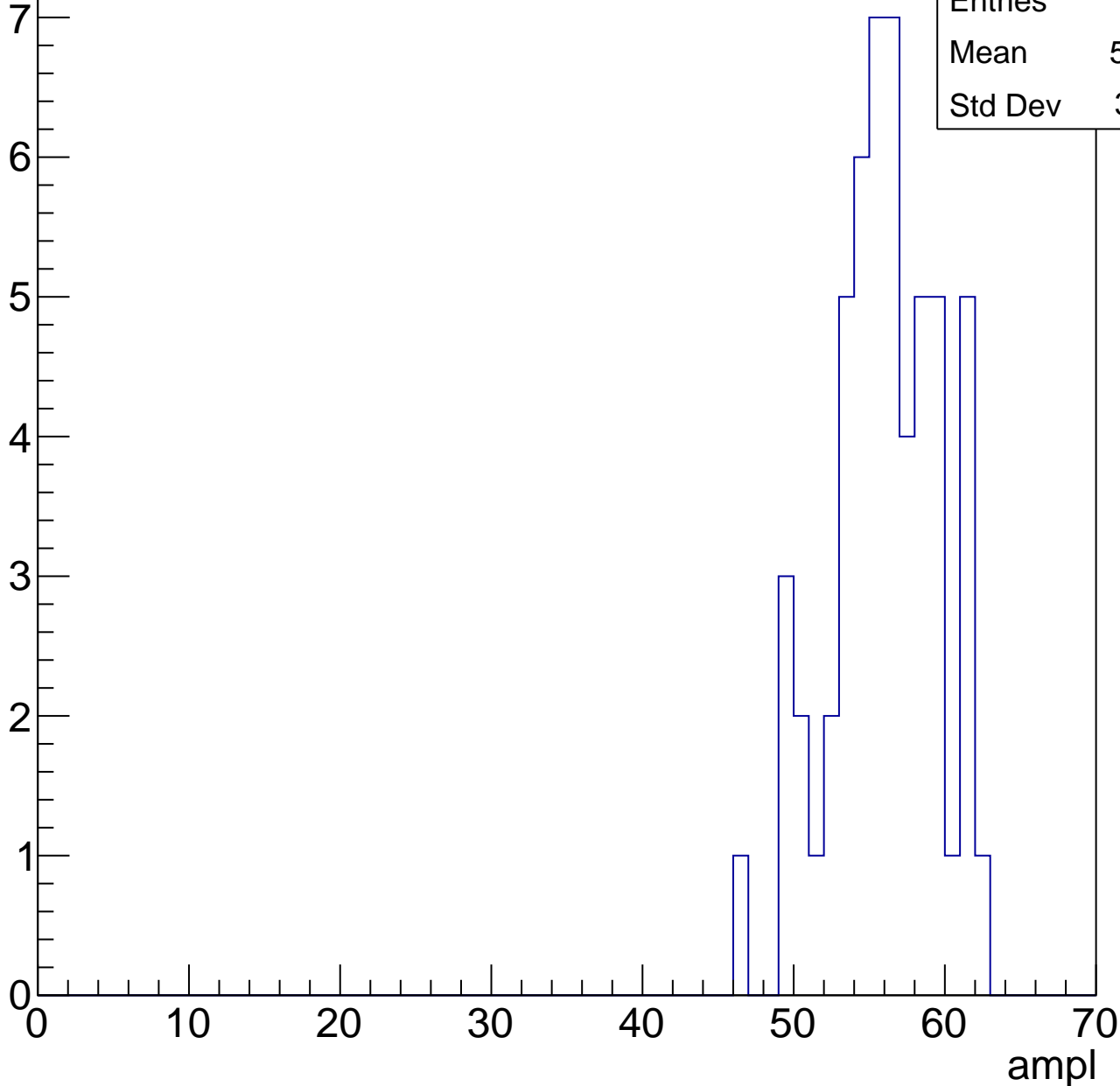


# B1L101S, U18-ch86, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

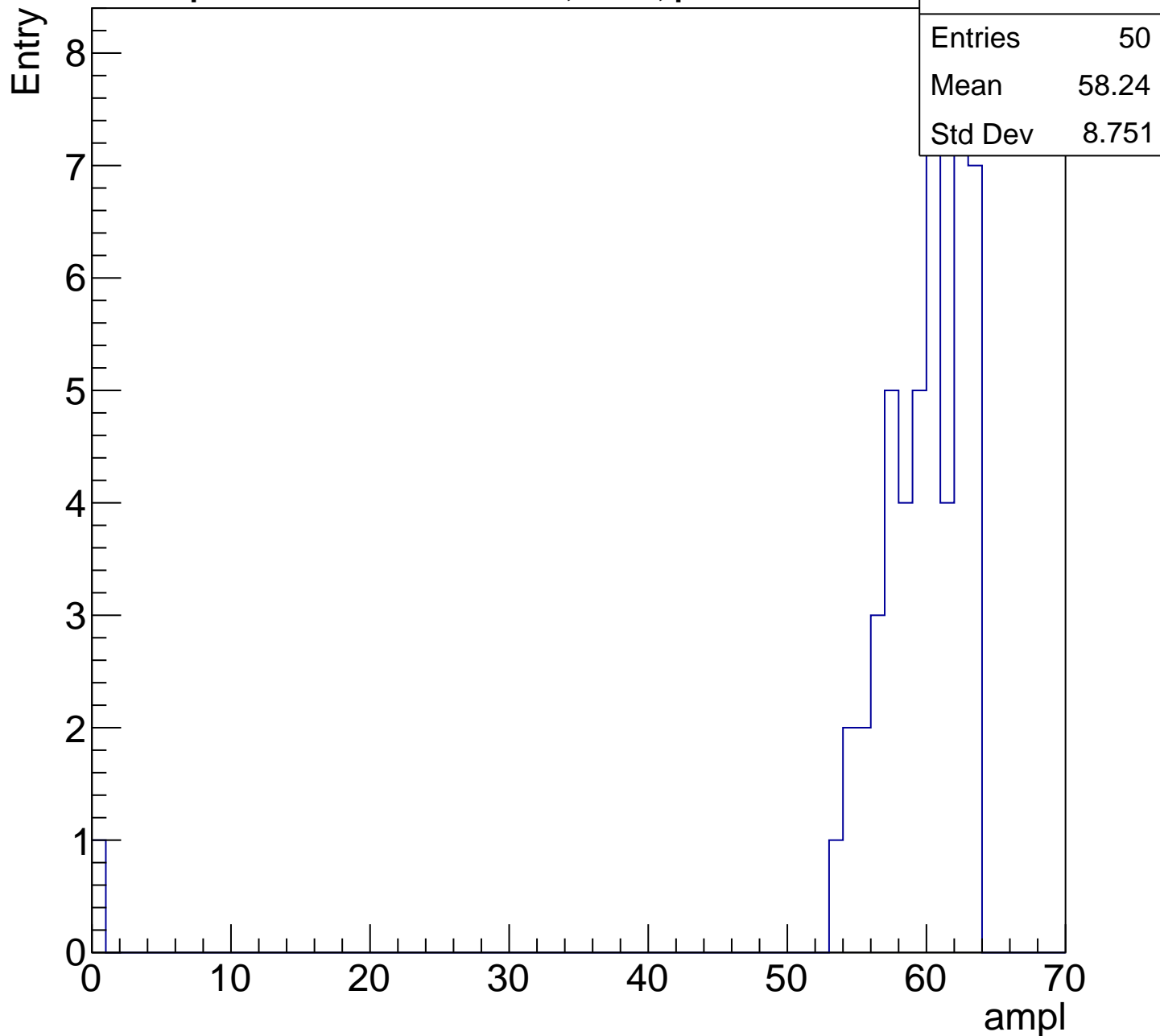
Entry

Entries	55
Mean	55.53
Std Dev	3.531



# B1L101S, U18-ch86, adc5

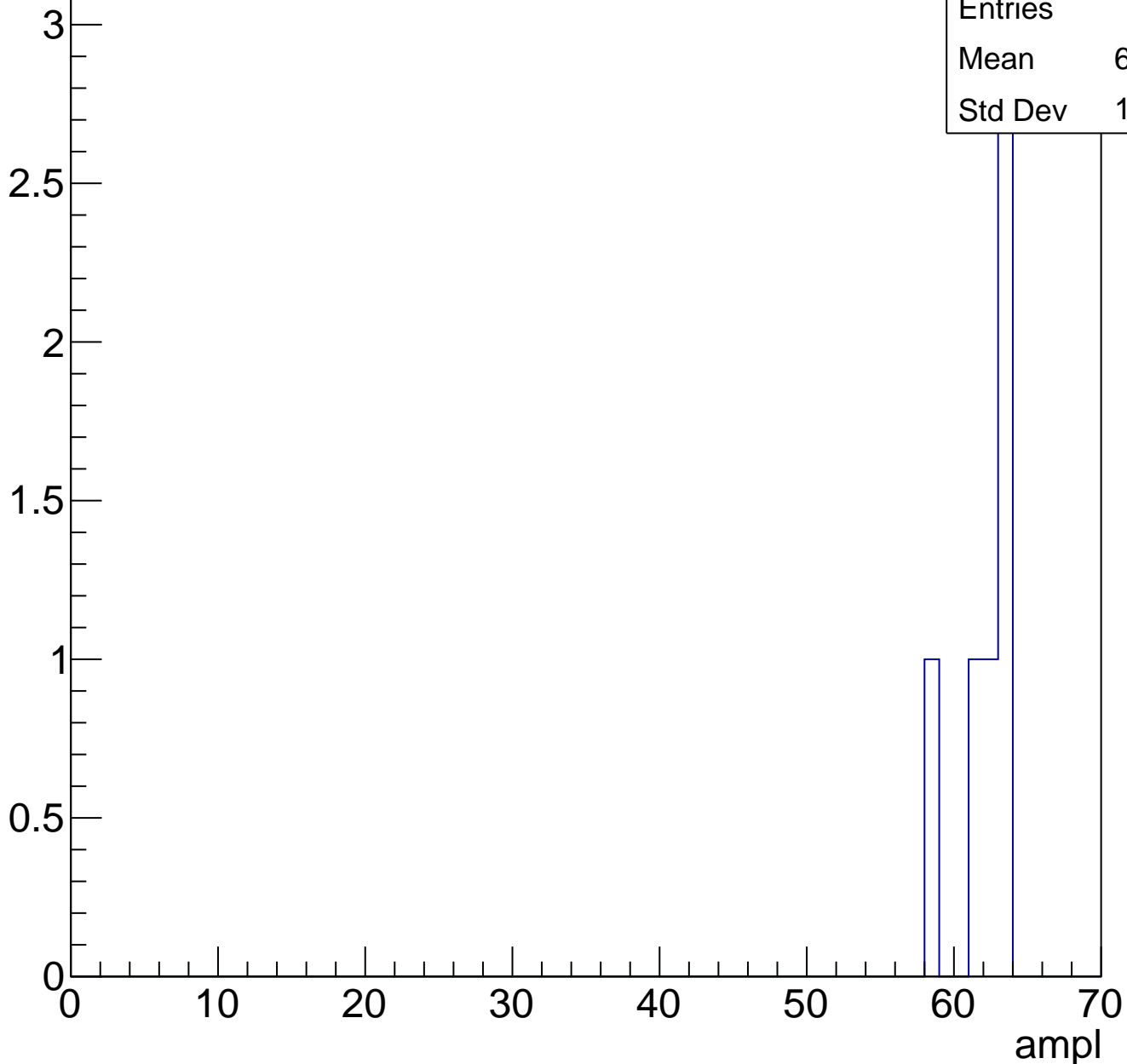
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U18-ch86, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

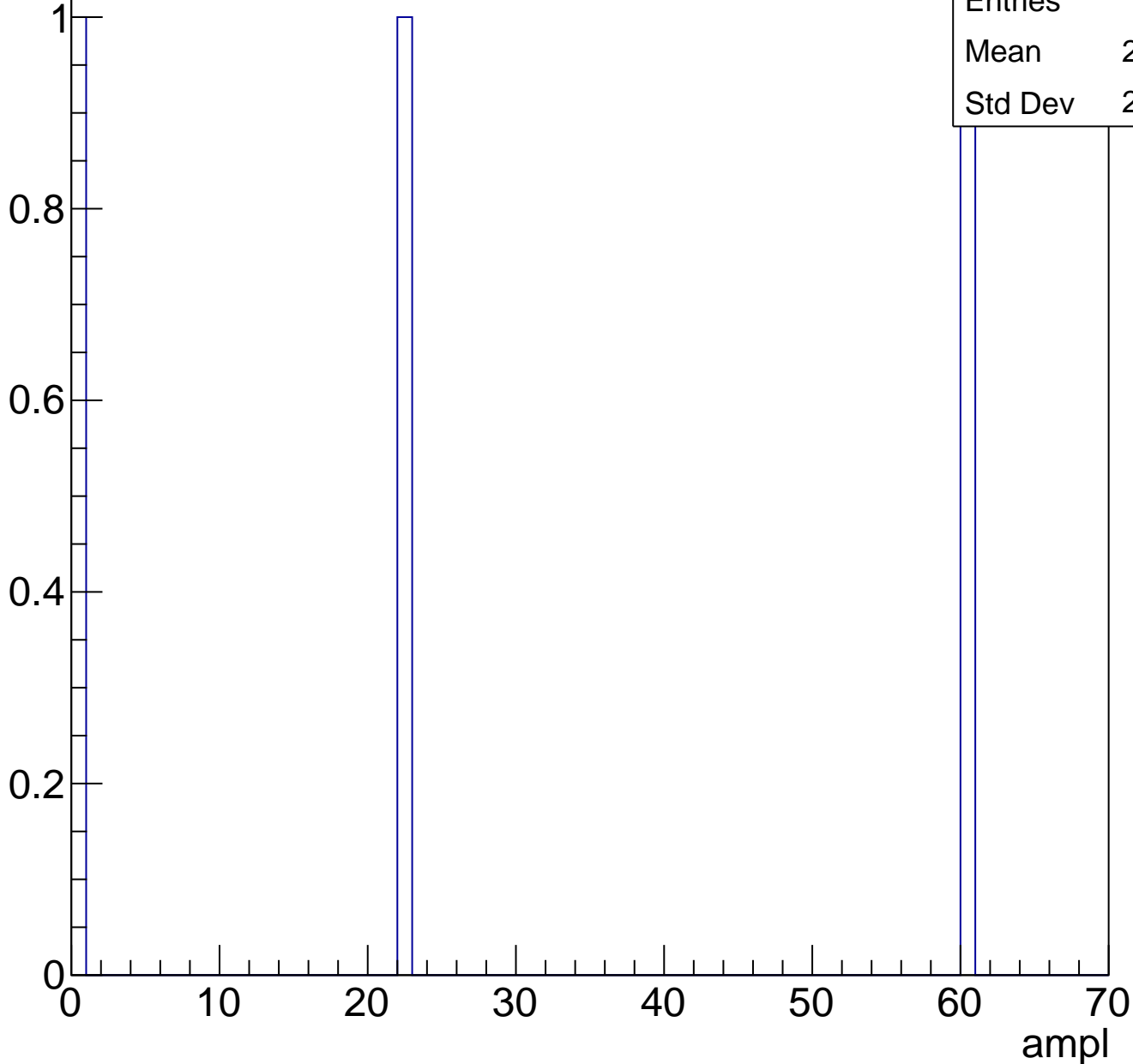




# B1L101S, U18-ch86, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	27.33
Std Dev	24.78

# B1L101S, U18-ch87, adc0

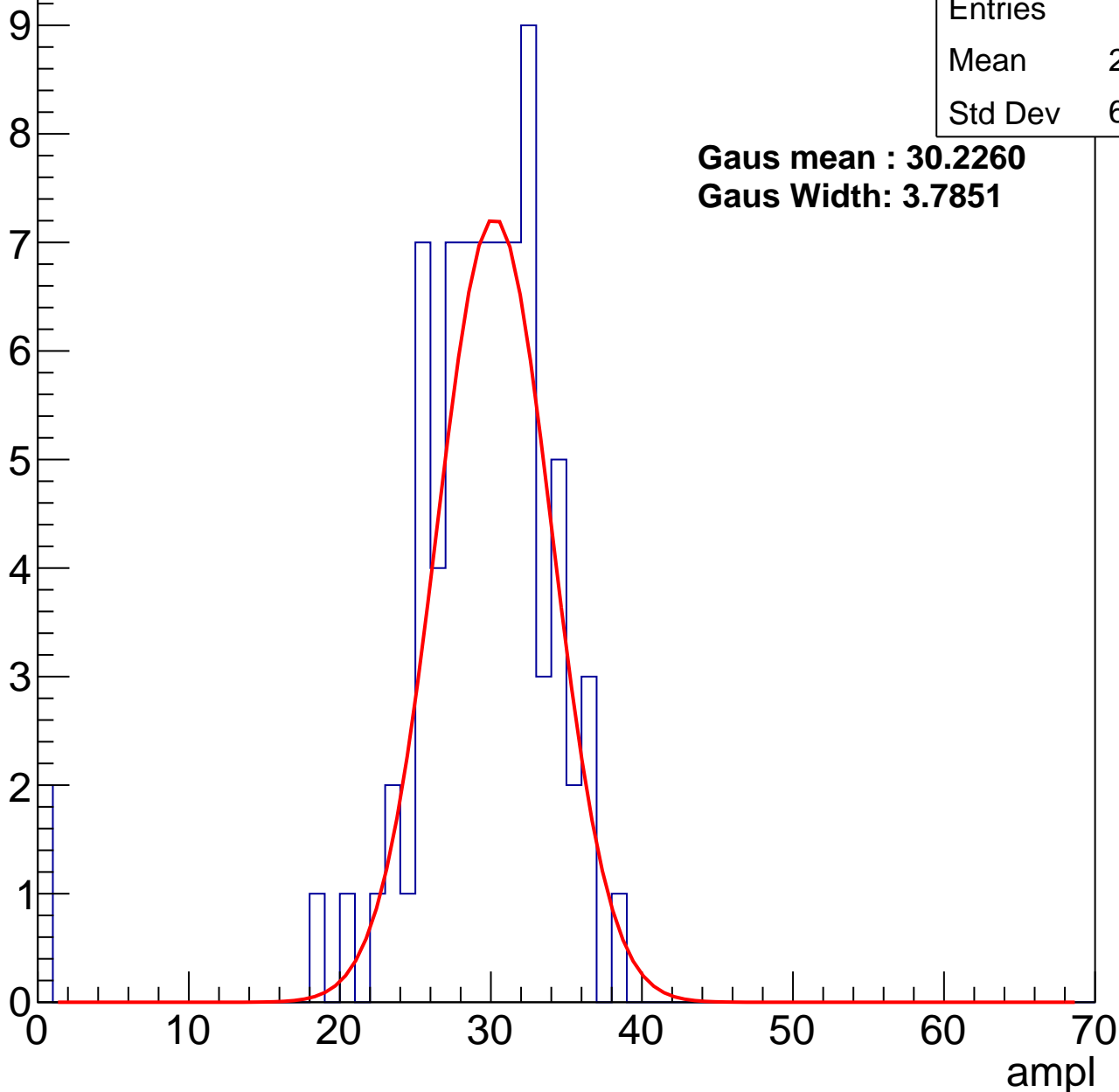
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	28.53
Std Dev	6.014

**Gaus mean : 30.2260**

**Gaus Width: 3.7851**



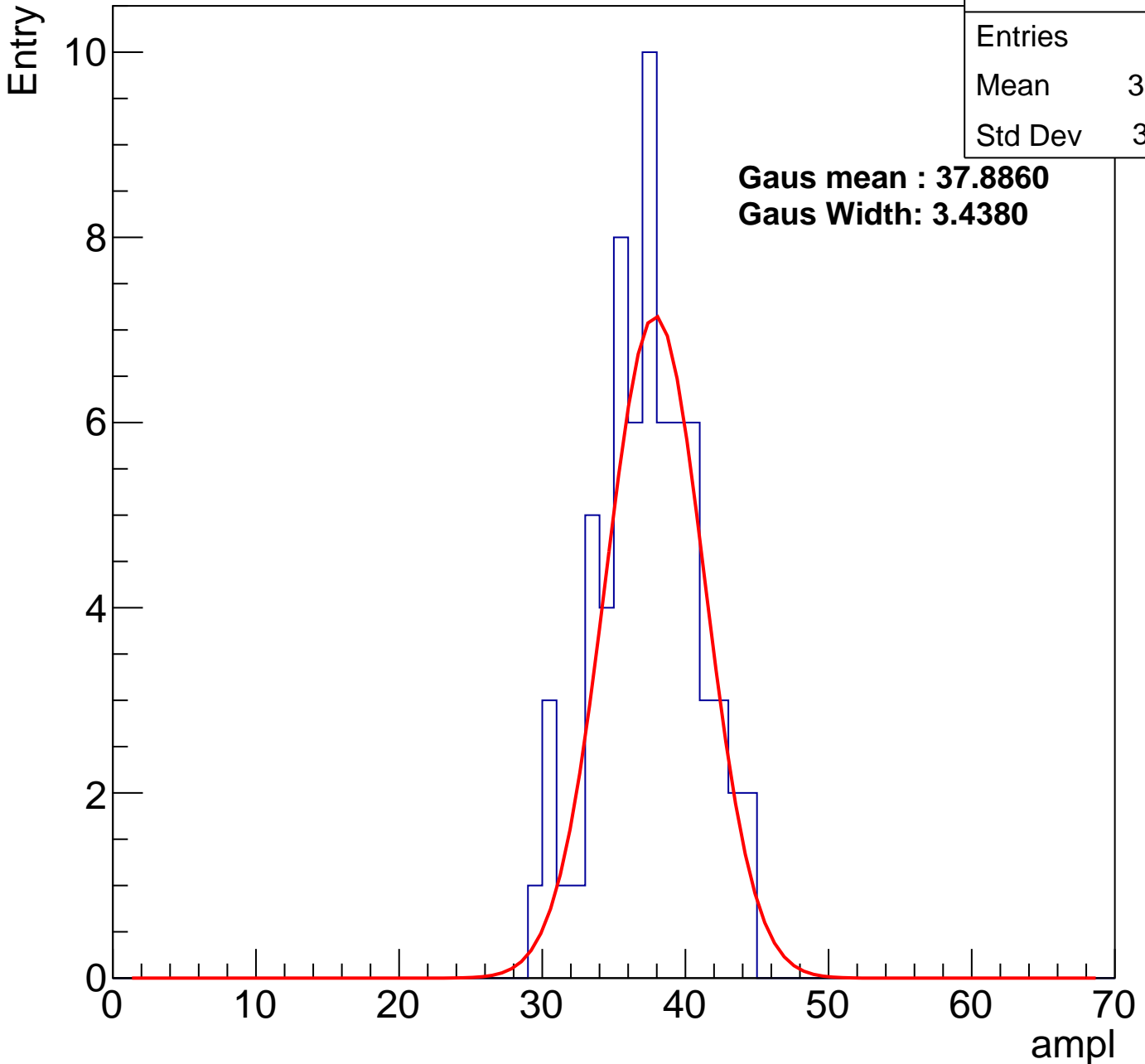
# B1L101S, U18-ch87, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	67
Mean	36.93
Std Dev	3.461

**Gaus mean : 37.8860**

**Gaus Width: 3.4380**



# B1L101S, U18-ch87, adc2

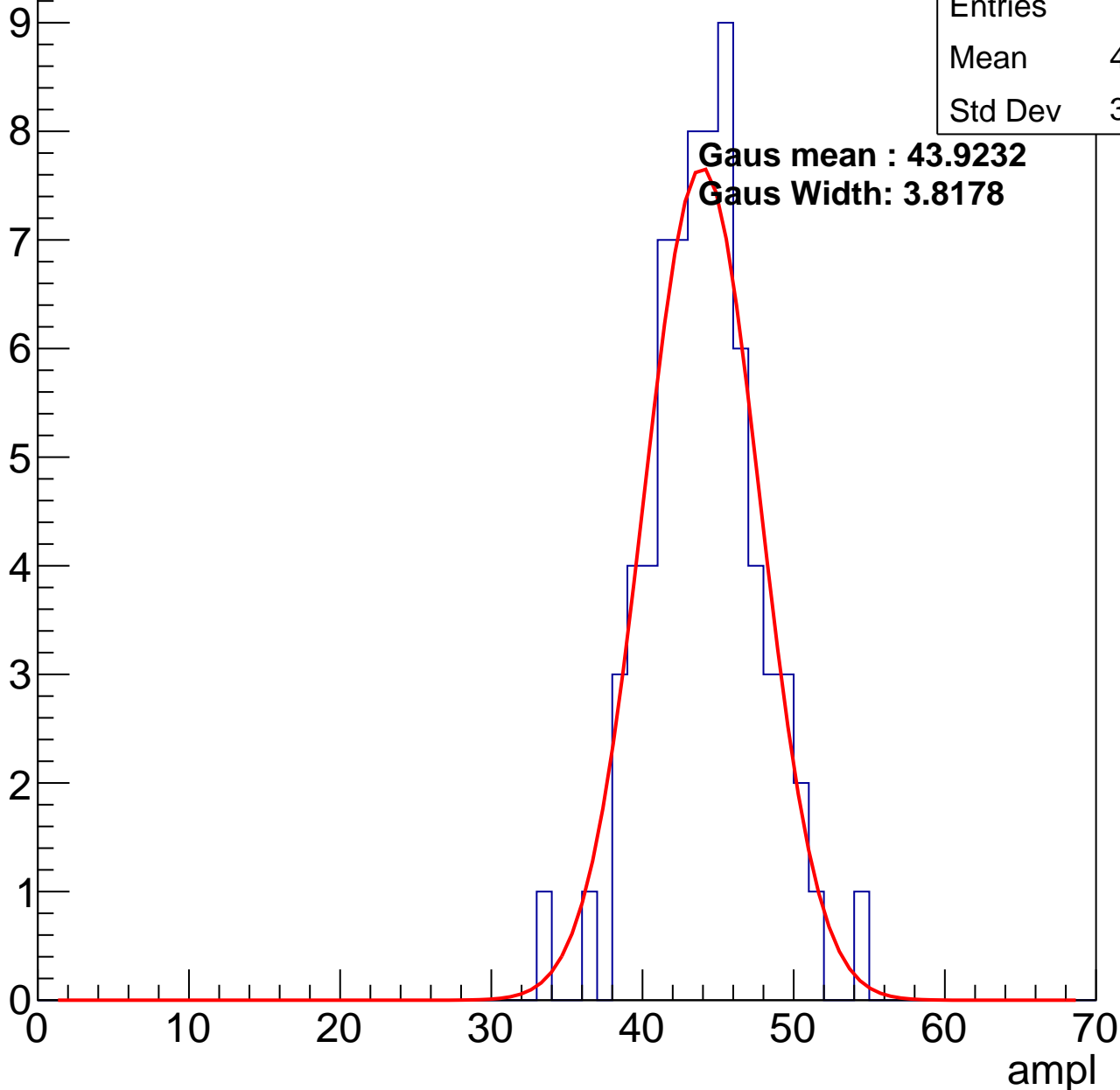
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	43.62
Std Dev	3.649

**Gaus mean : 43.9232**

**Gaus Width: 3.8178**

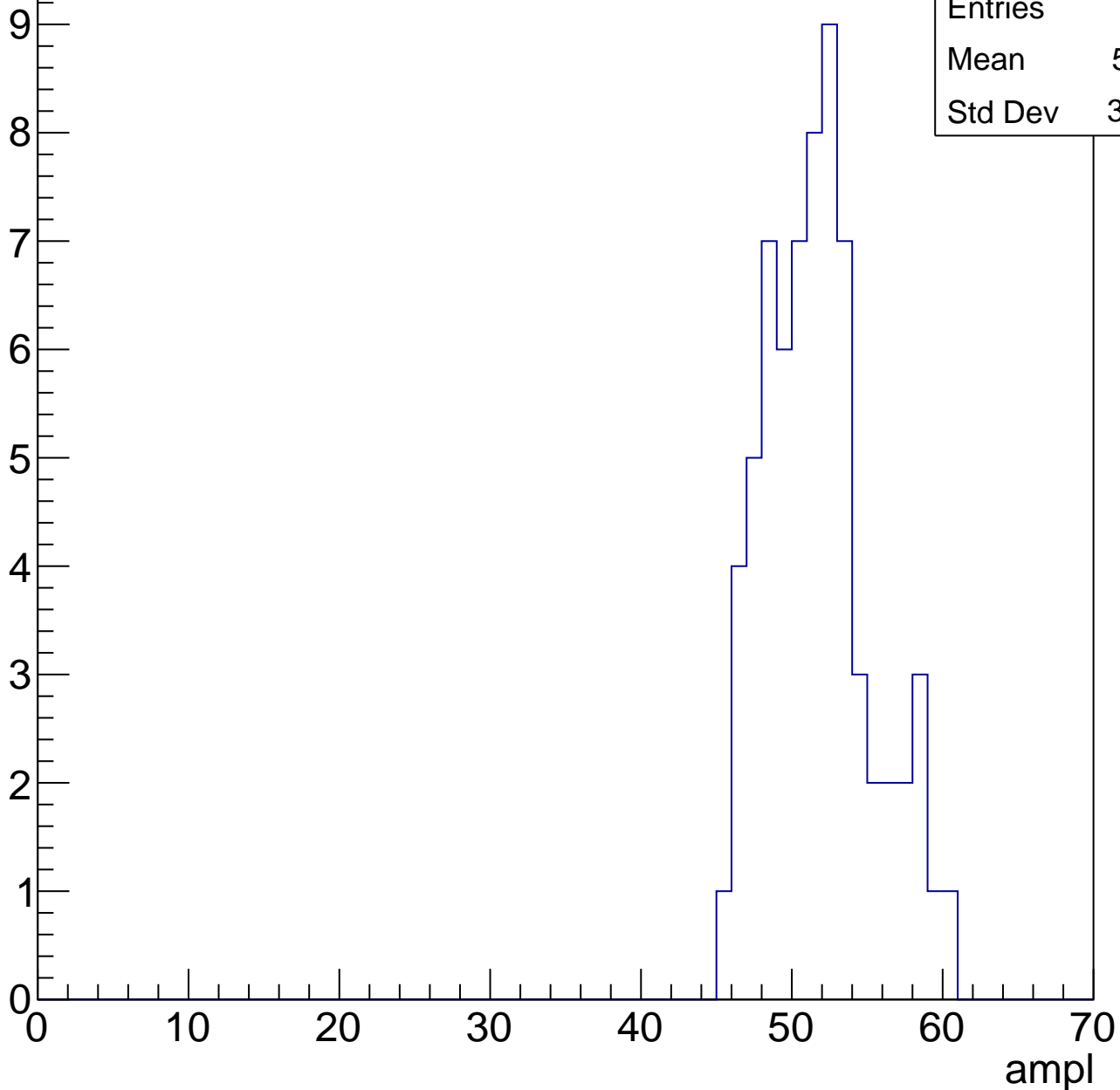


# B1L101S, U18-ch87, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	51.21
Std Dev	3.466

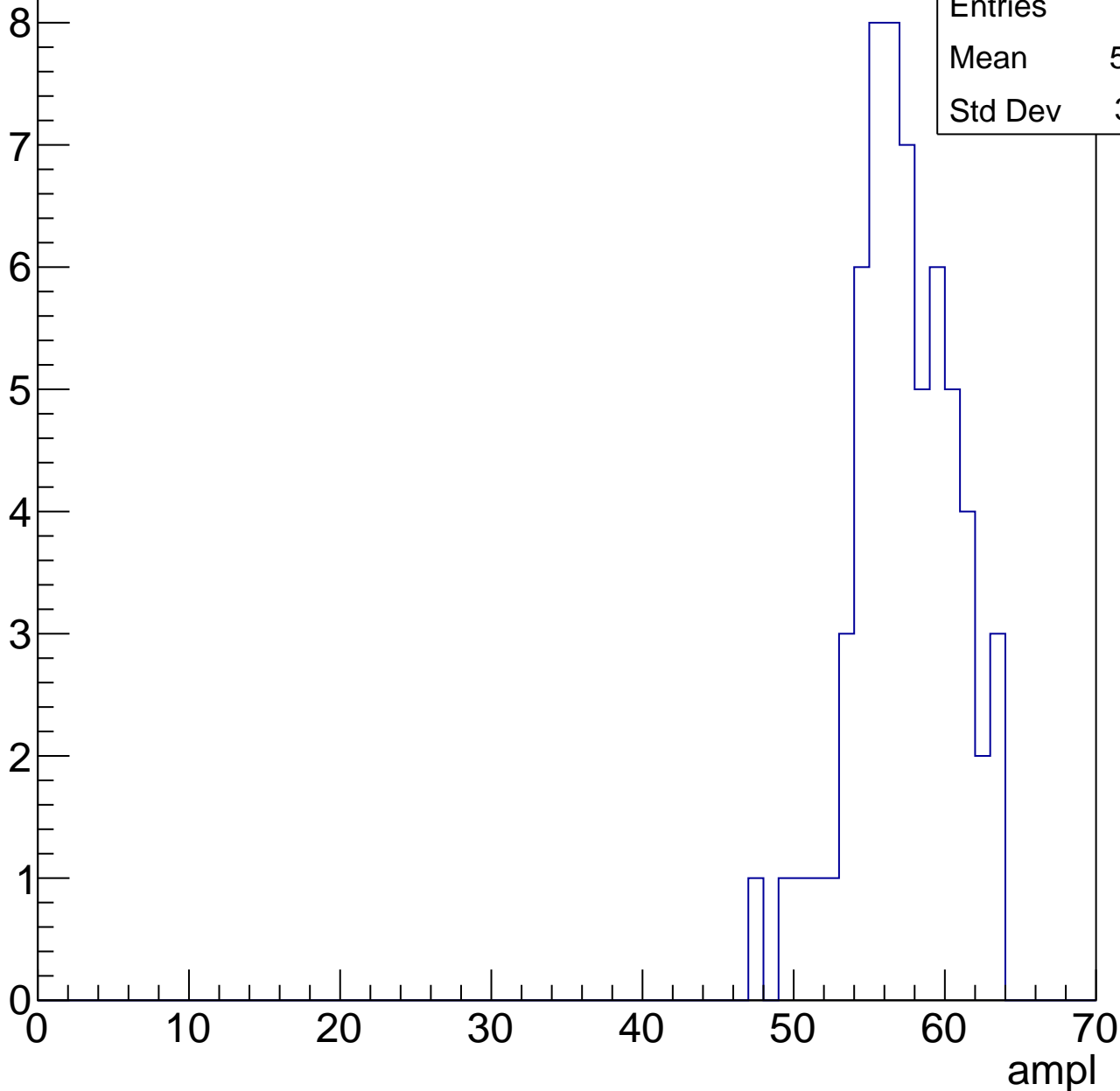


# B1L101S, U18-ch87, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	56.77
Std Dev	3.381

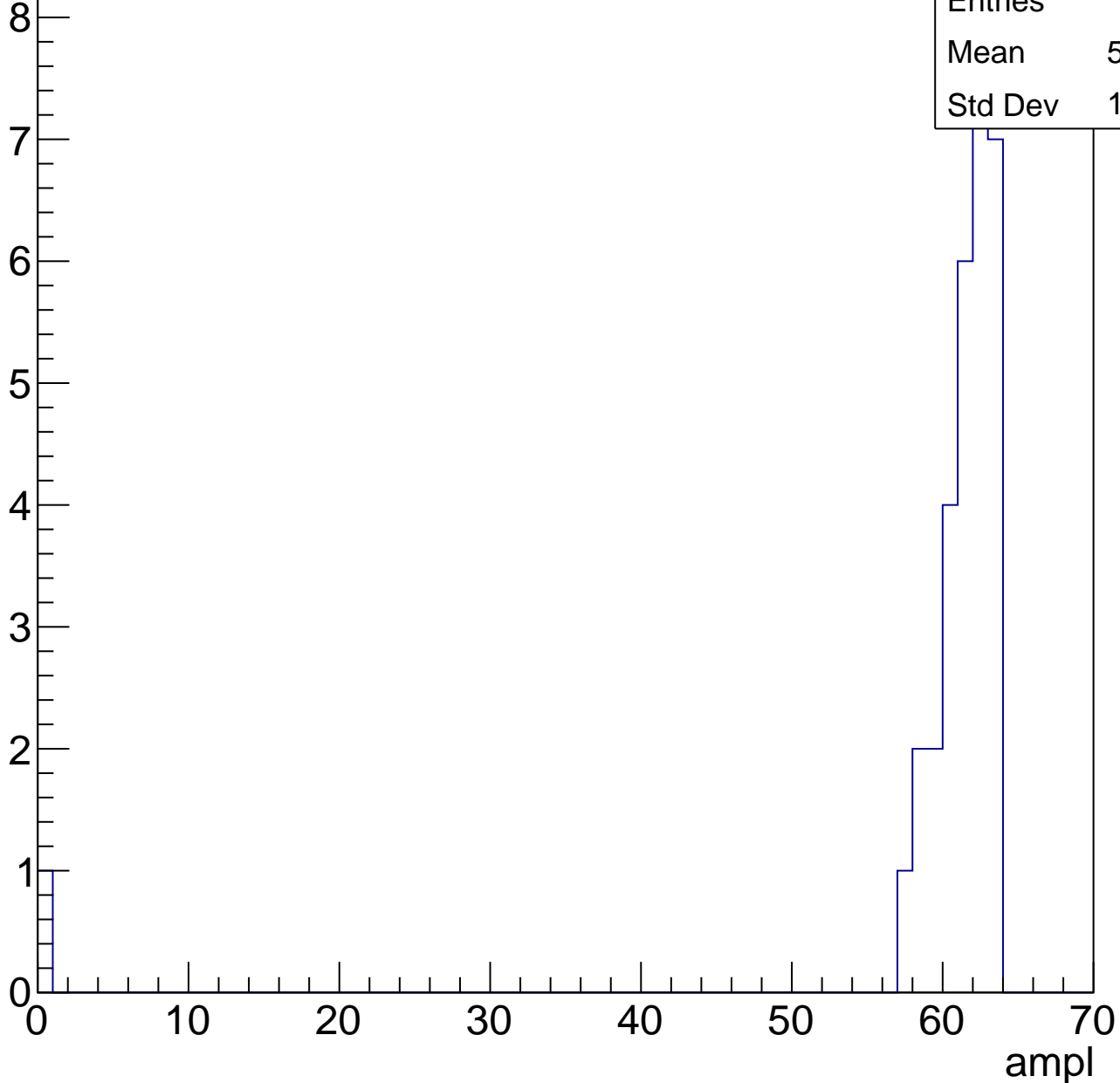


# B1L101S, U18-ch87, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	31
Mean	59.16
Std Dev	10.92



# B1L101S, U18-ch87, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

ampl

Entries	1
Mean	59
Std Dev	0



# B1L101S, U18-ch87, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U18-ch88, adc0

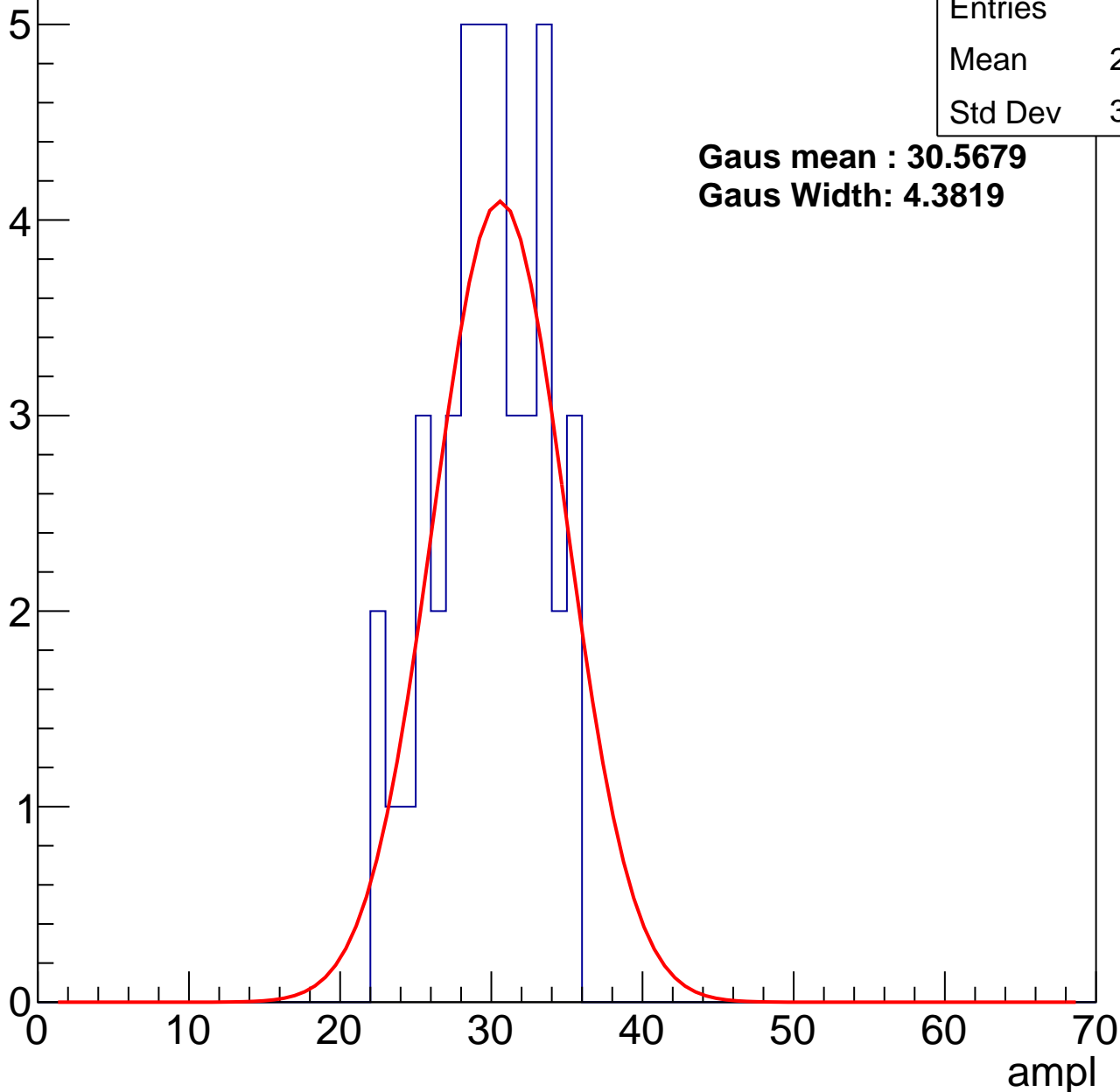
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	43
Mean	29.33
Std Dev	3.476

**Gaus mean : 30.5679**

**Gaus Width: 4.3819**



# B1L101S, U18-ch88, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	86
Mean	36.6
Std Dev	4.21

**Gaus mean : 36.5563**

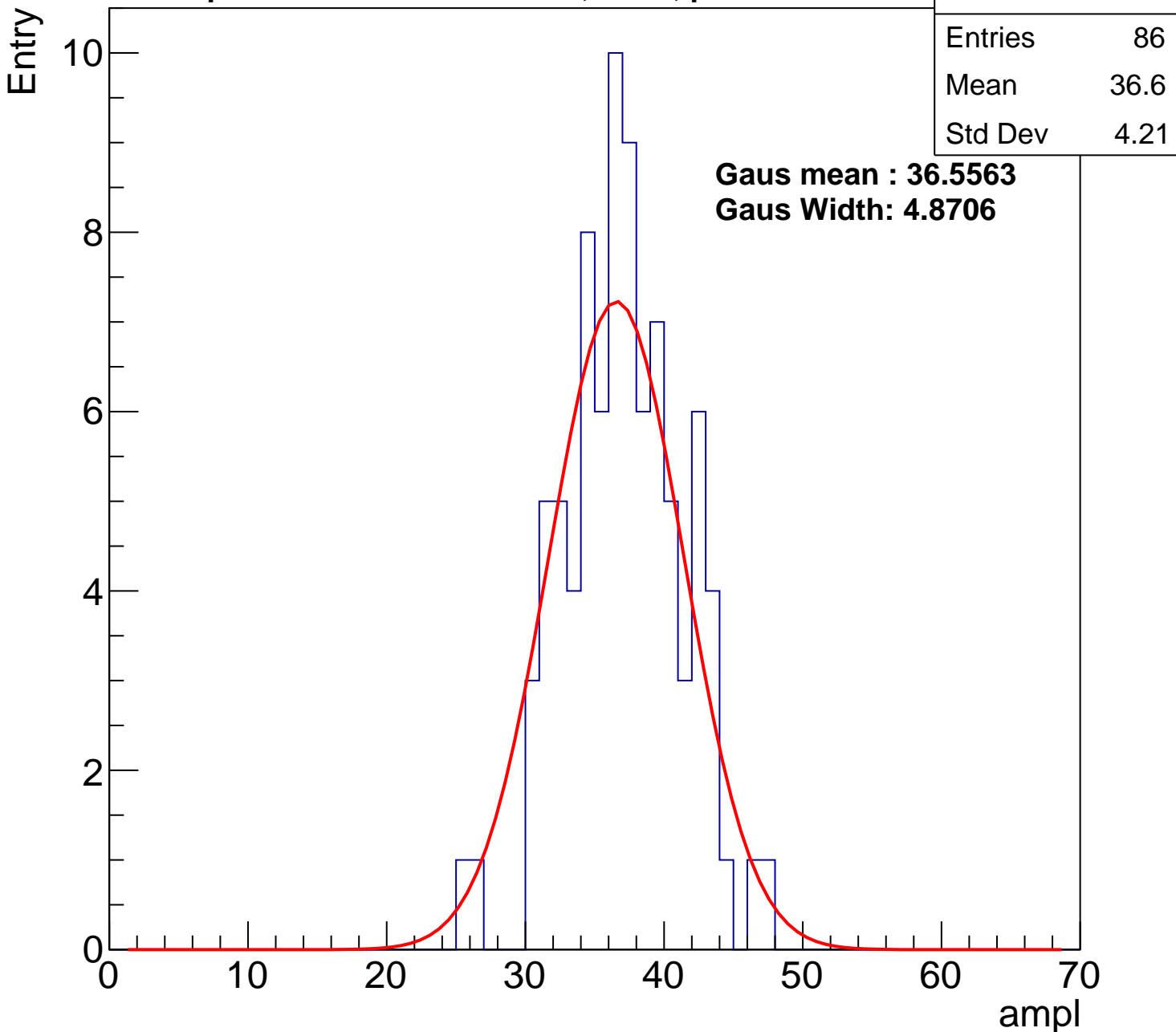
**Gaus Width: 4.8706**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U18-ch88, adc2

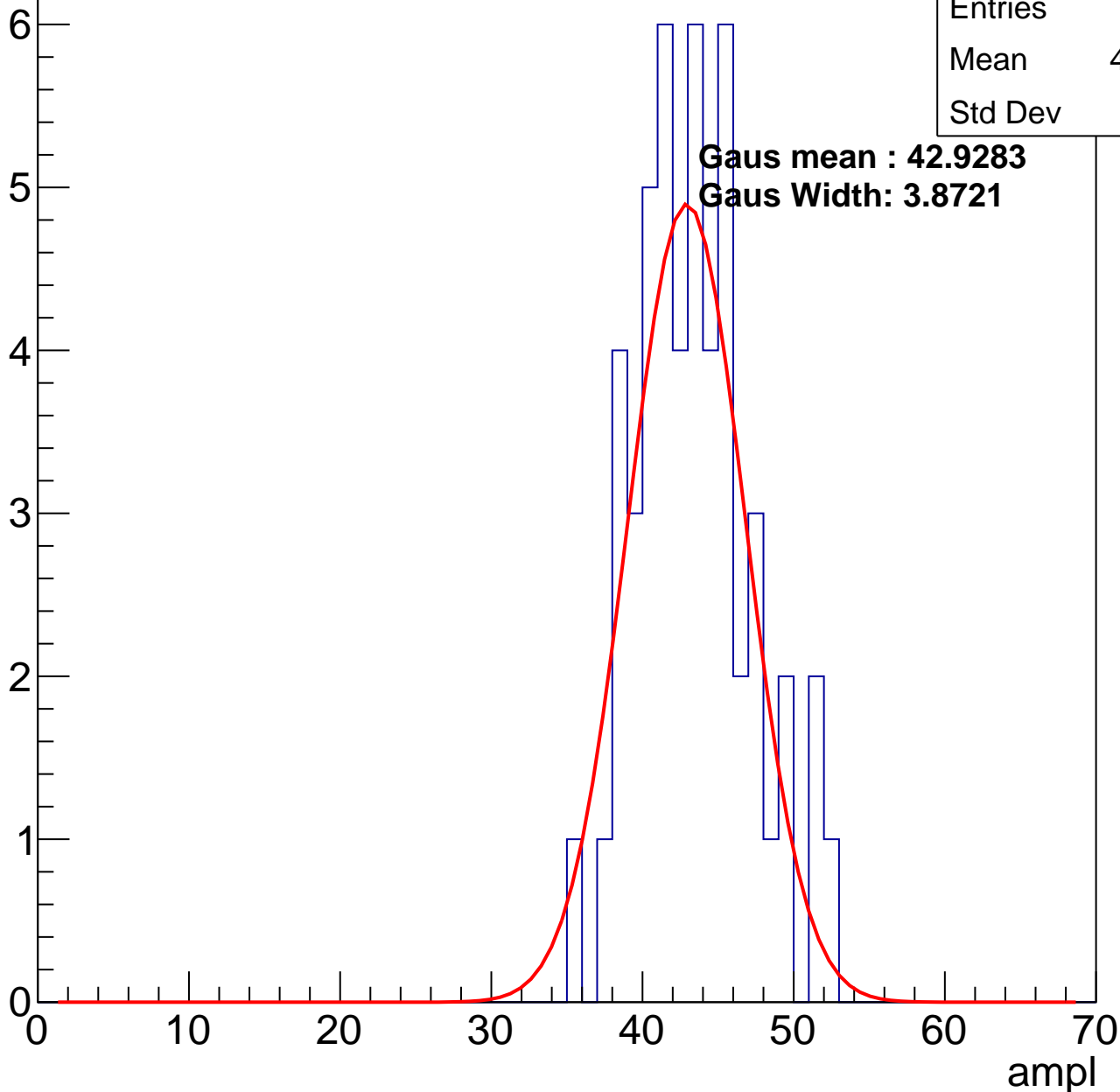
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	42.98
Std Dev	3.76

**Gaus mean : 42.9283**

**Gaus Width: 3.8721**

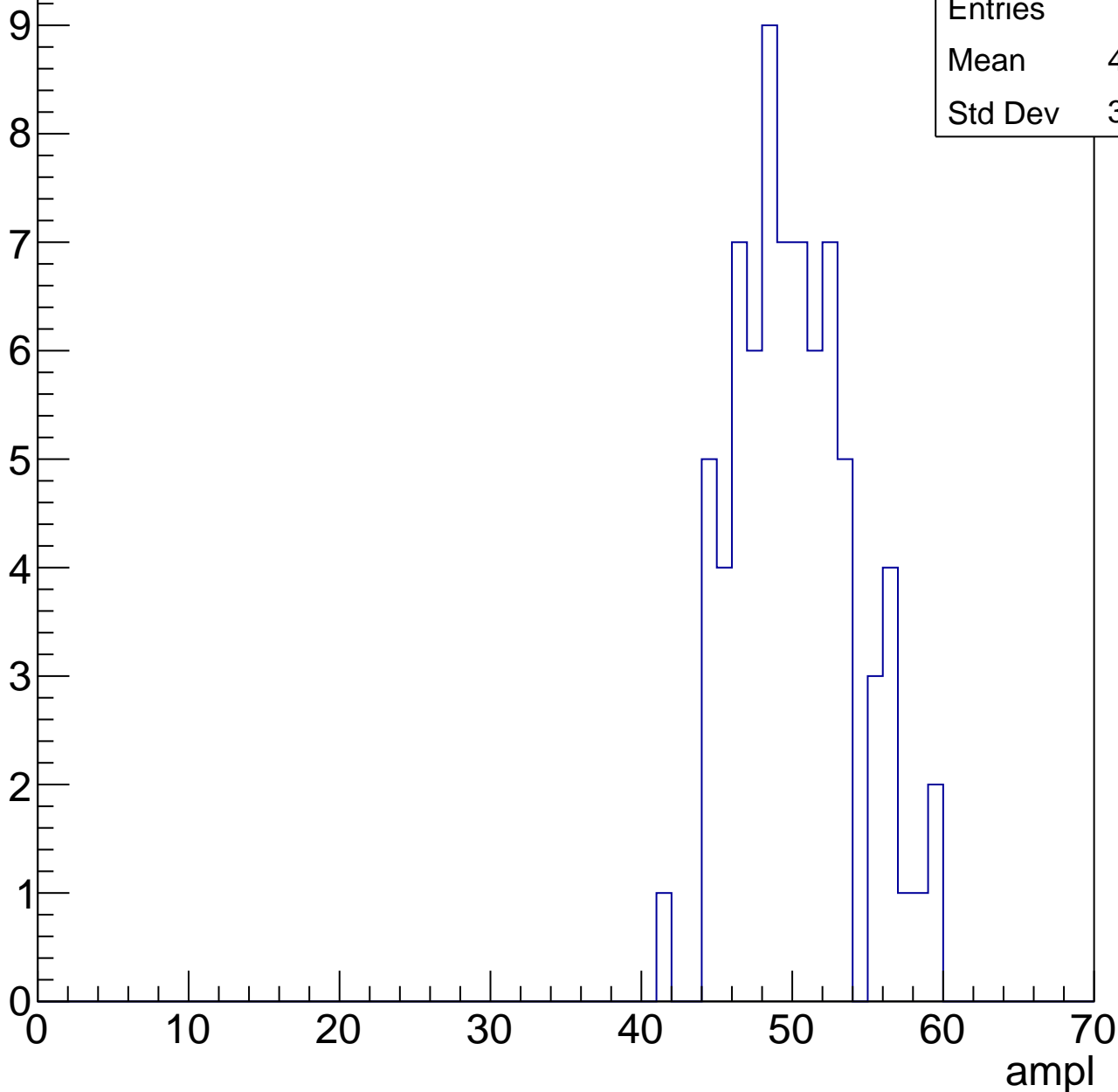


# B1L101S, U18-ch88, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	49.69
Std Dev	3.892



# B1L101S, U18-ch88, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

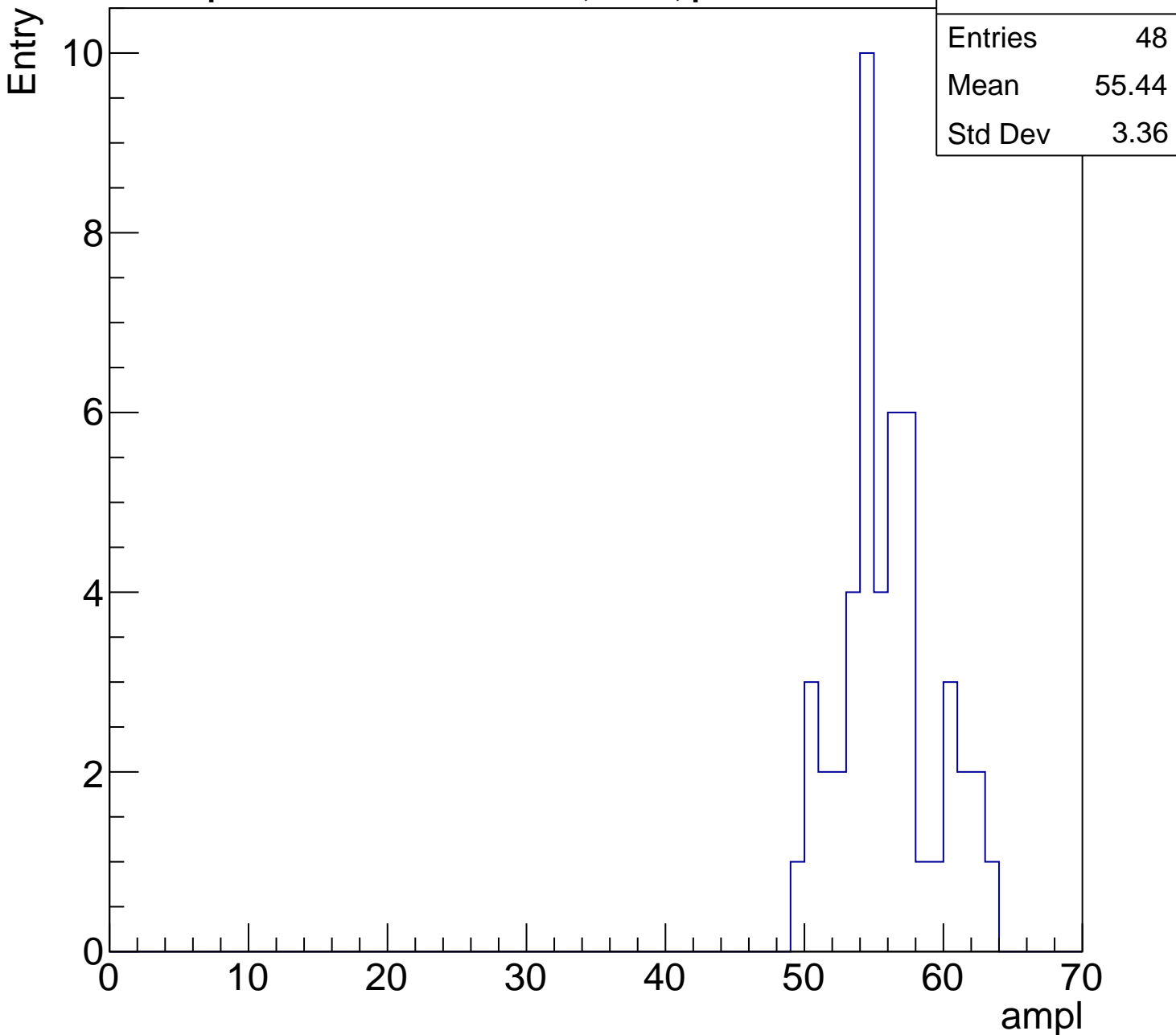
Entries	48
Mean	55.44
Std Dev	3.36

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

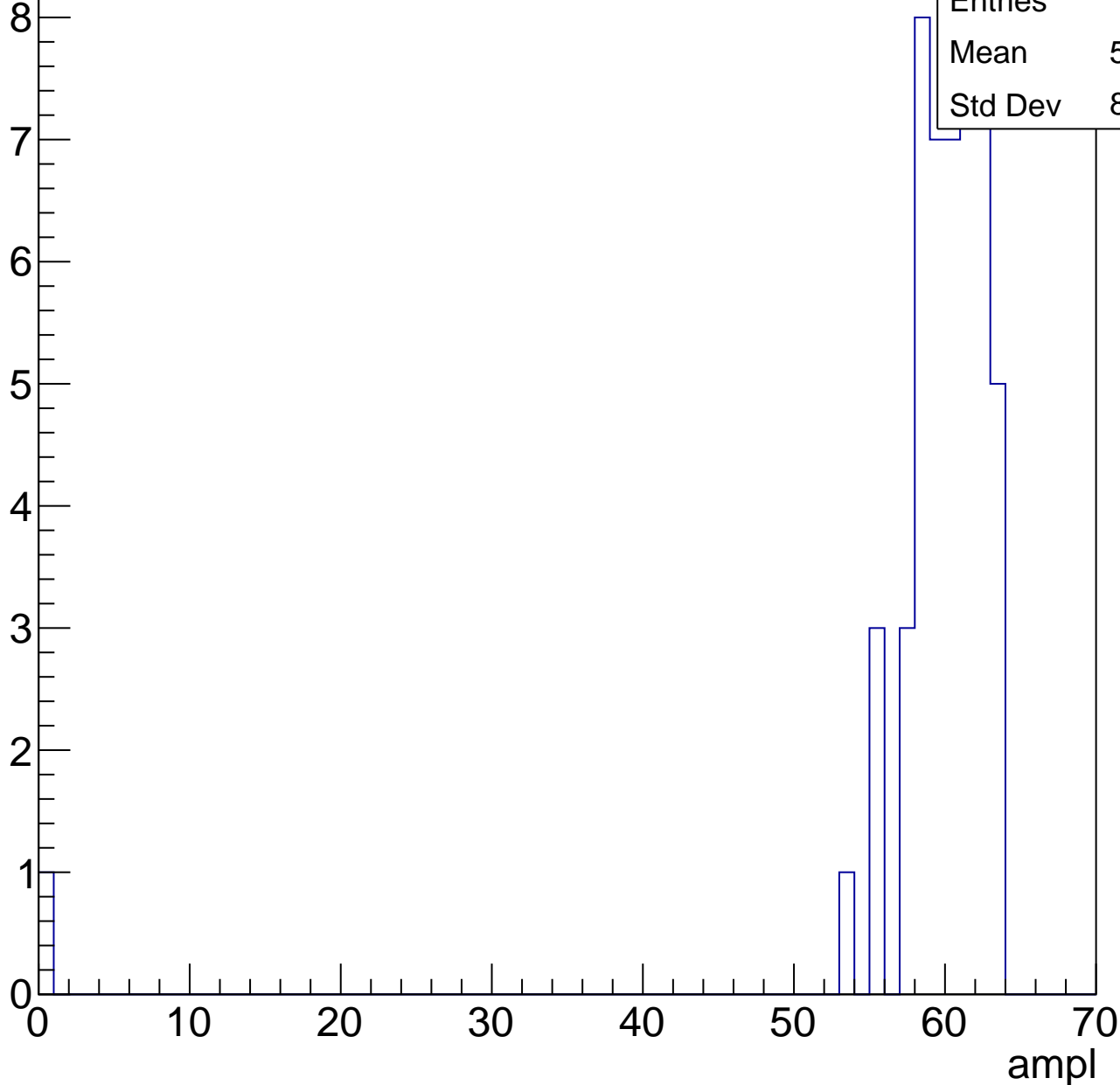


# B1L101S, U18-ch88, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

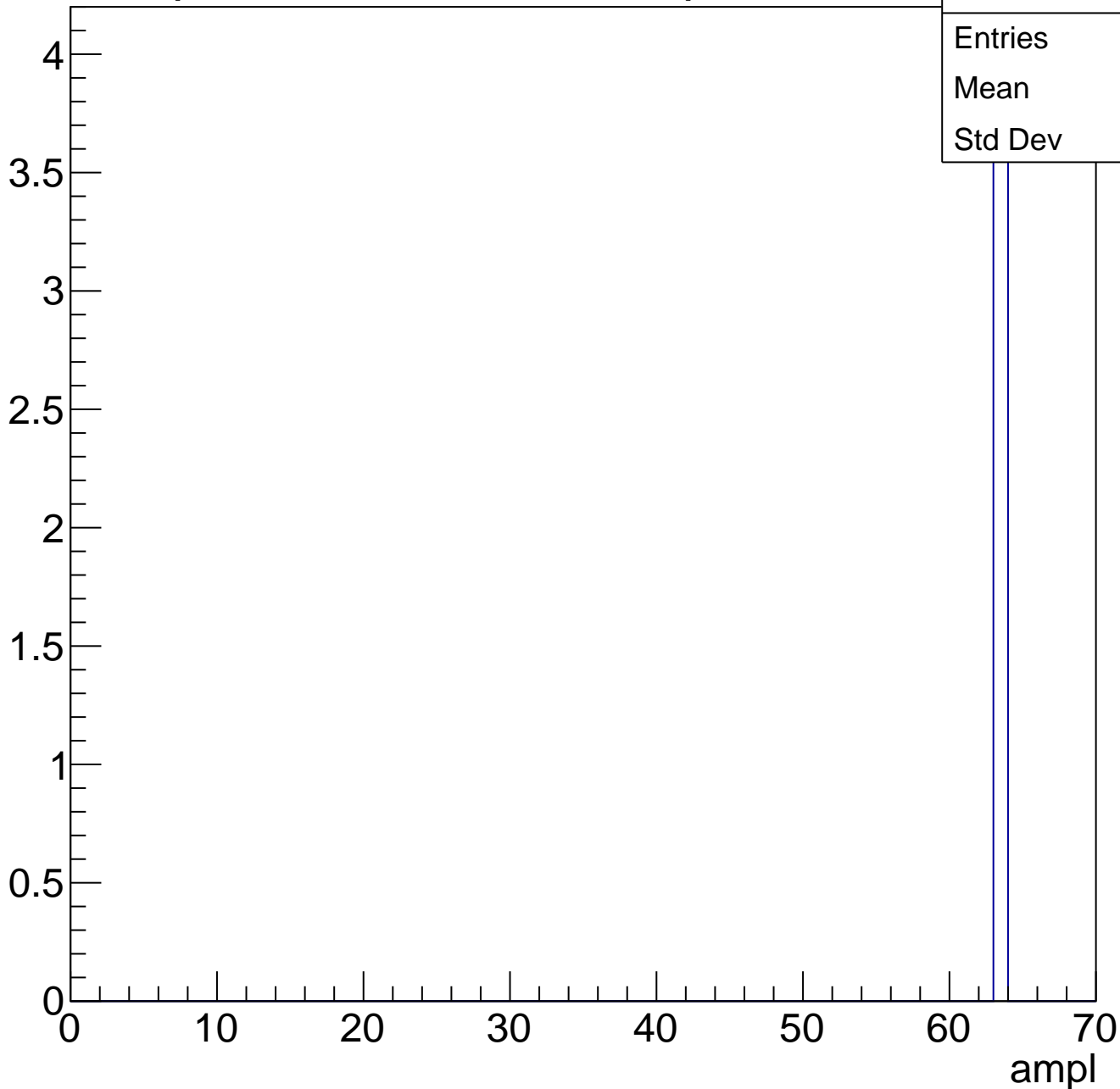
Entries	51
Mean	58.53
Std Dev	8.592



# B1L101S, U18-ch88, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch88, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch89, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	85
Mean	31.84
Std Dev	6.195

**Gaus mean : 33.4825**

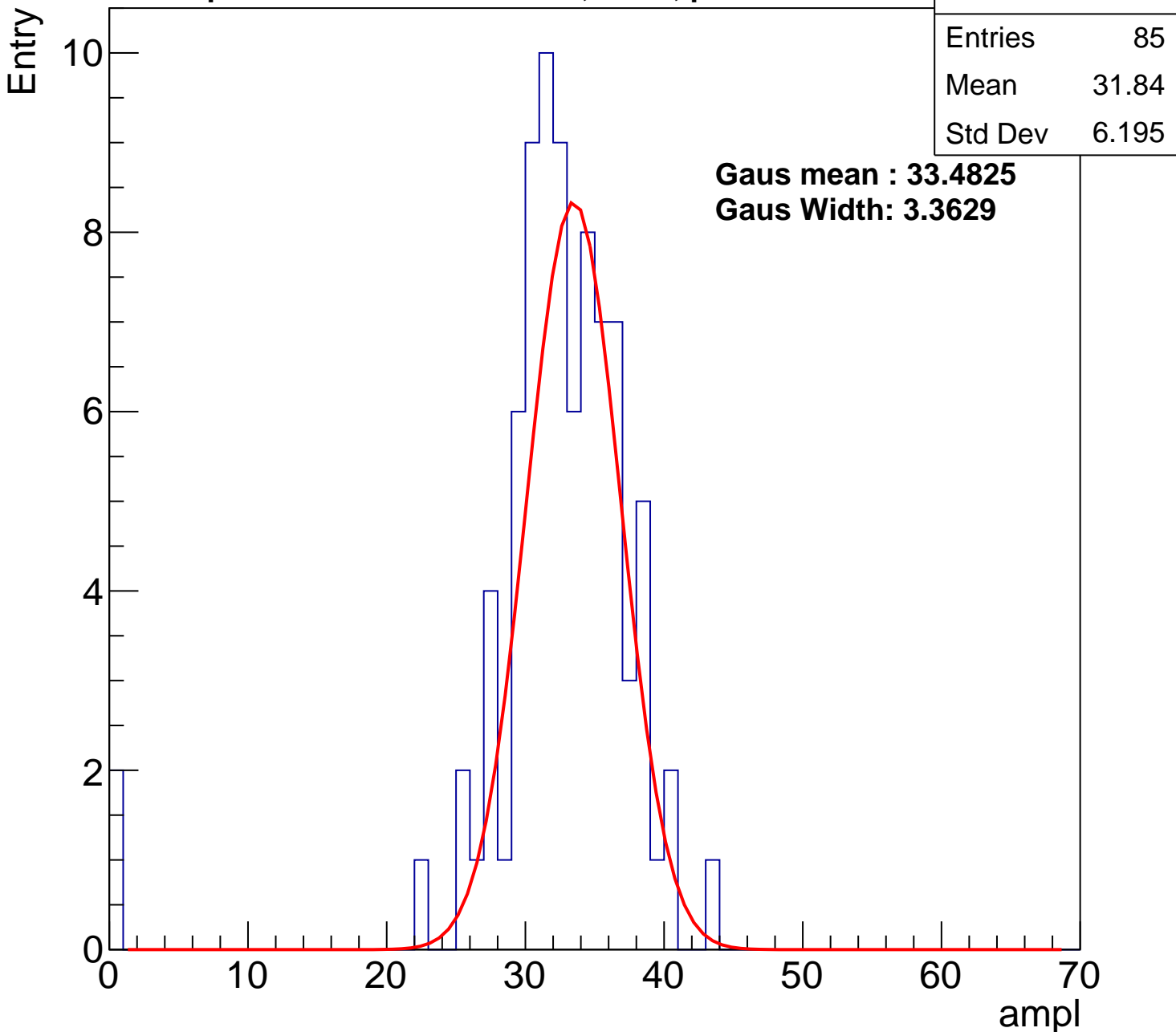
**Gaus Width: 3.3629**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



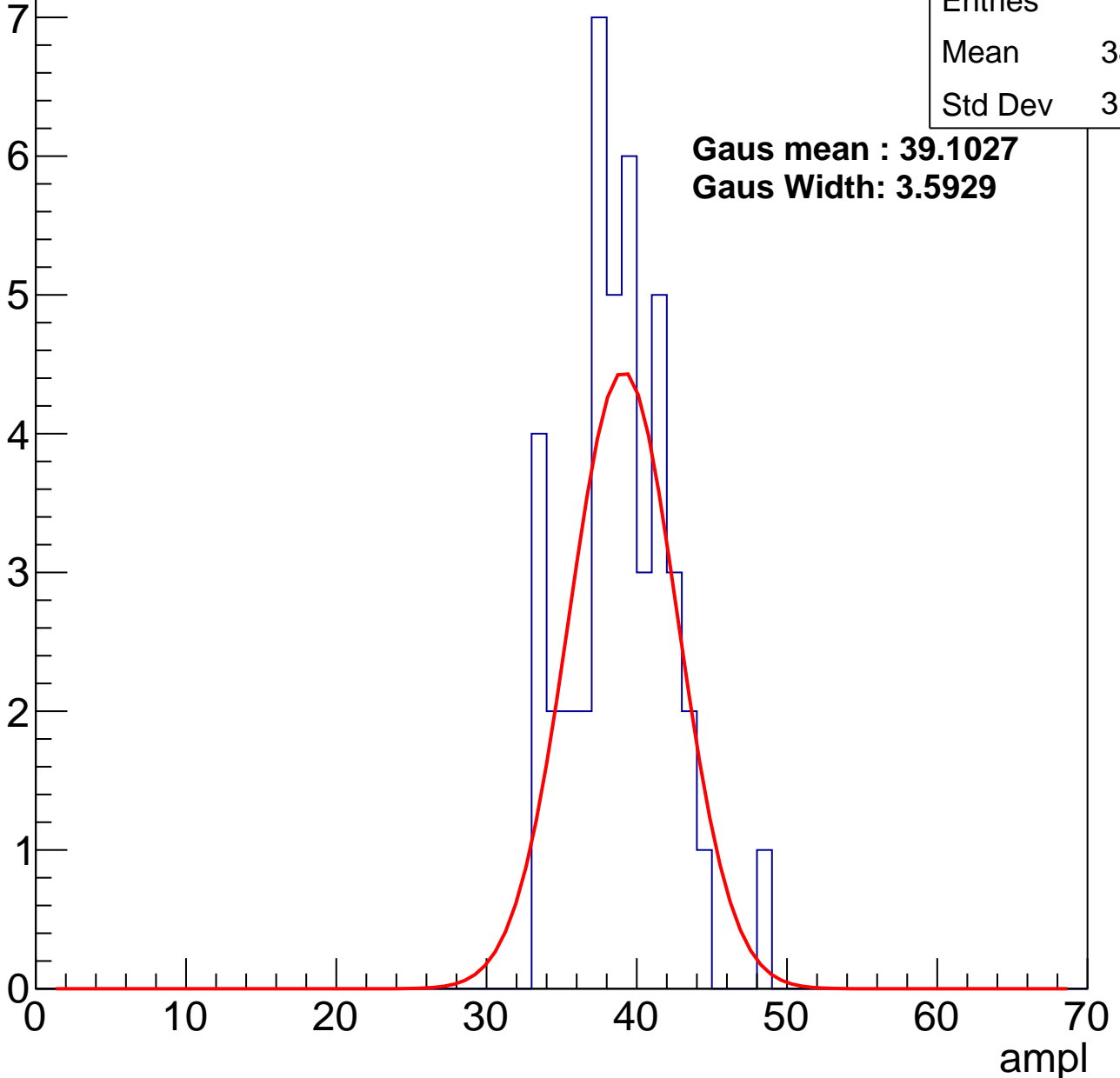
# B1L101S, U18-ch89, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	43
Mean	38.47
Std Dev	3.245

**Gaus mean : 39.1027**  
**Gaus Width: 3.5929**



# B1L101S, U18-ch89, adc2

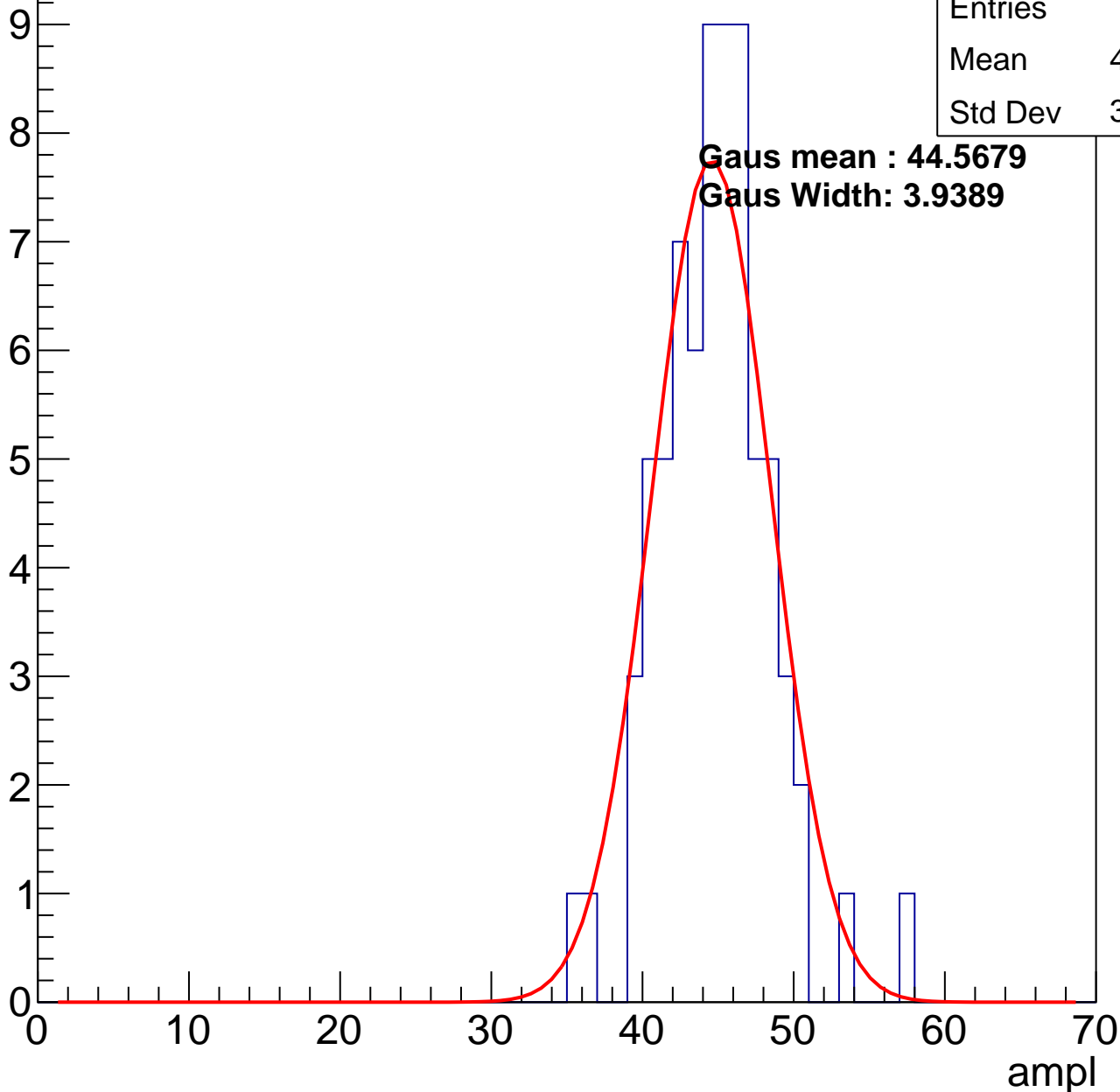
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	44.33
Std Dev	3.609

**Gaus mean : 44.5679**

**Gaus Width: 3.9389**

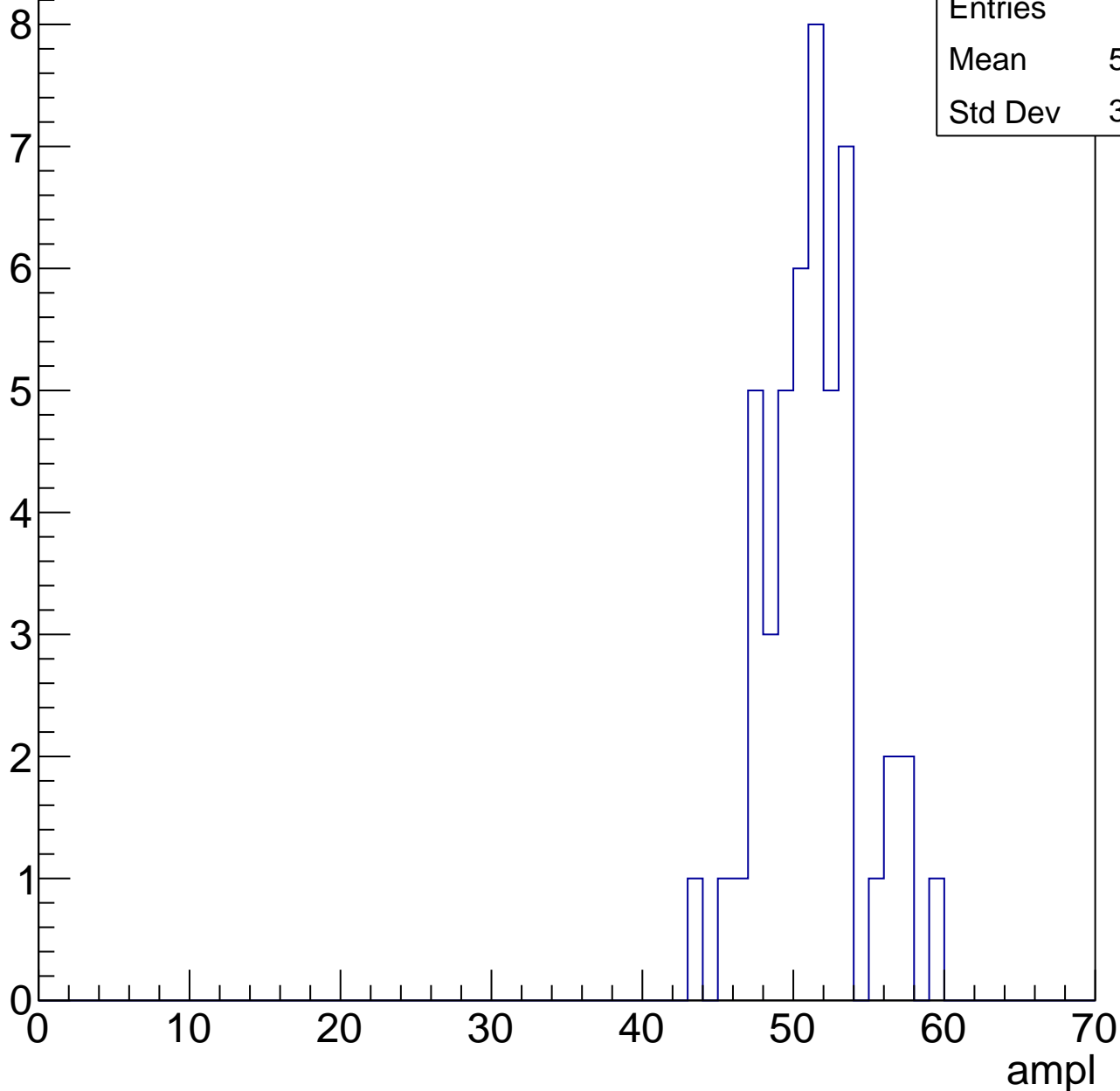


# B1L101S, U18-ch89, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	48
Mean	50.77
Std Dev	3.197



# B1L101S, U18-ch89, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	74
Mean	56.19
Std Dev	3.513

Entry

10

8

6

4

2

0

0

10

20

30

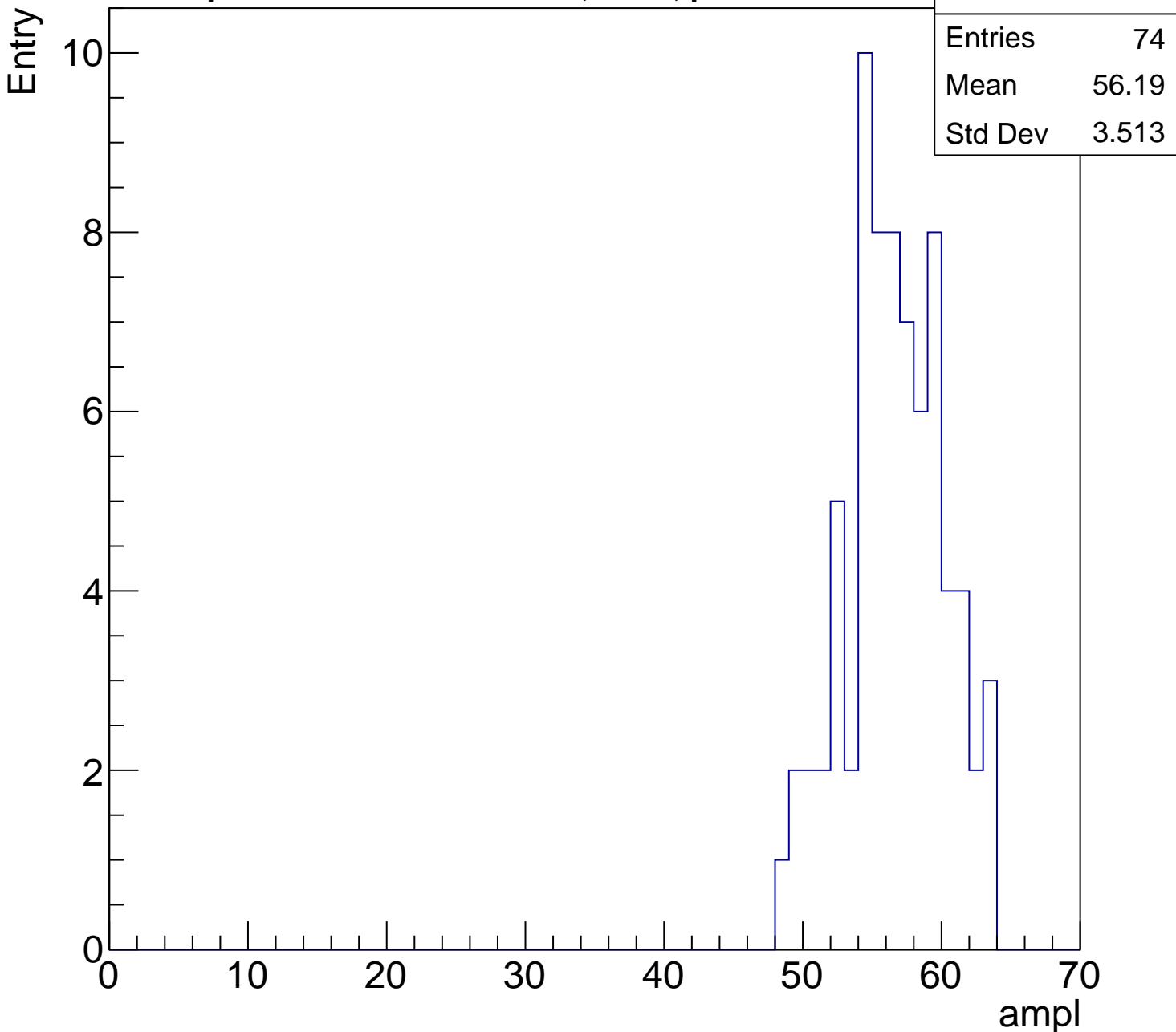
40

50

60

ampl

70

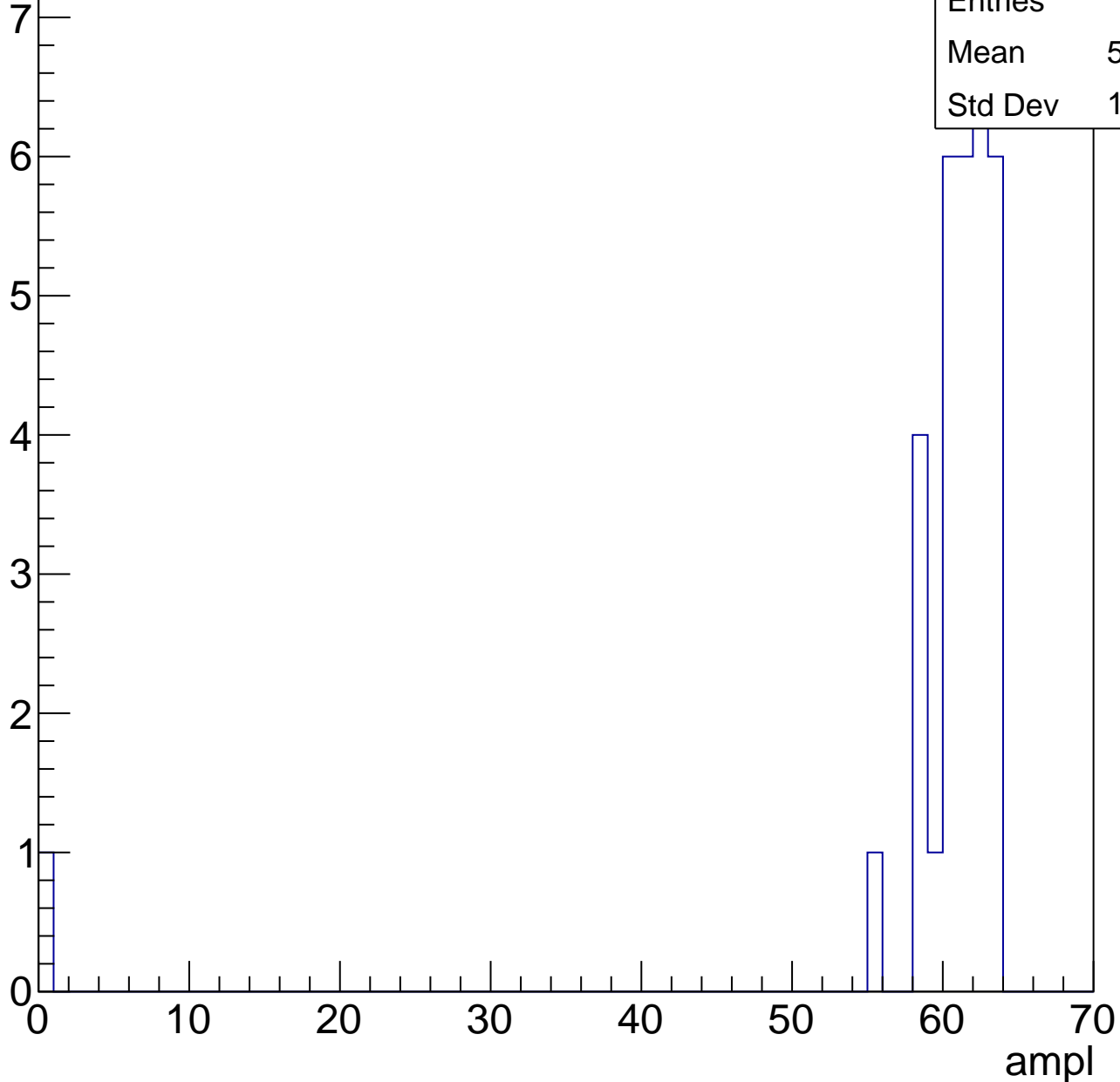


# B1L101S, U18-ch89, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	32
Mean	58.88
Std Dev	10.74



# B1L101S, U18-ch89, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch89, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U18-ch90, adc0

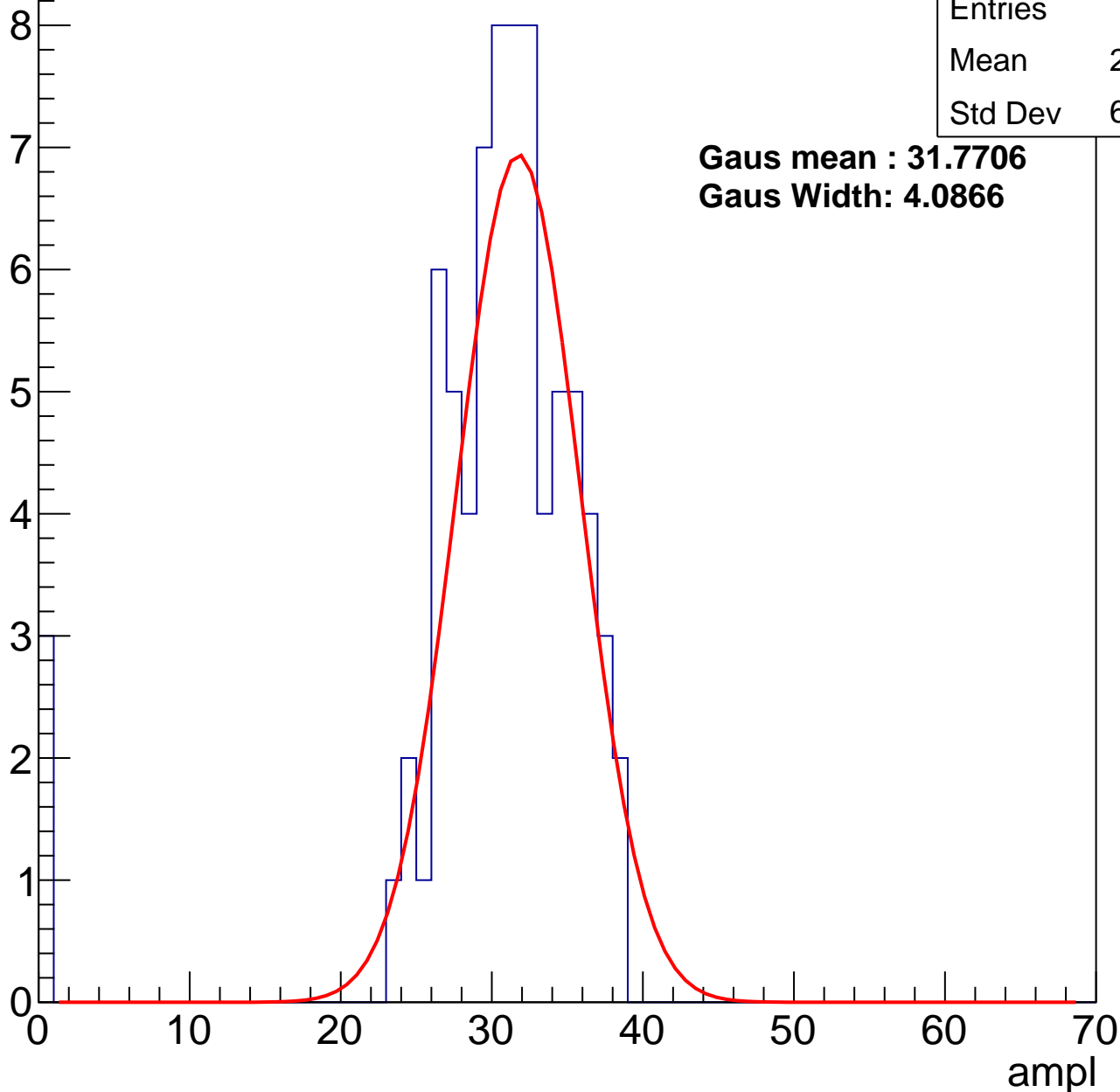
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	29.66
Std Dev	6.978

**Gaus mean : 31.7706**

**Gaus Width: 4.0866**



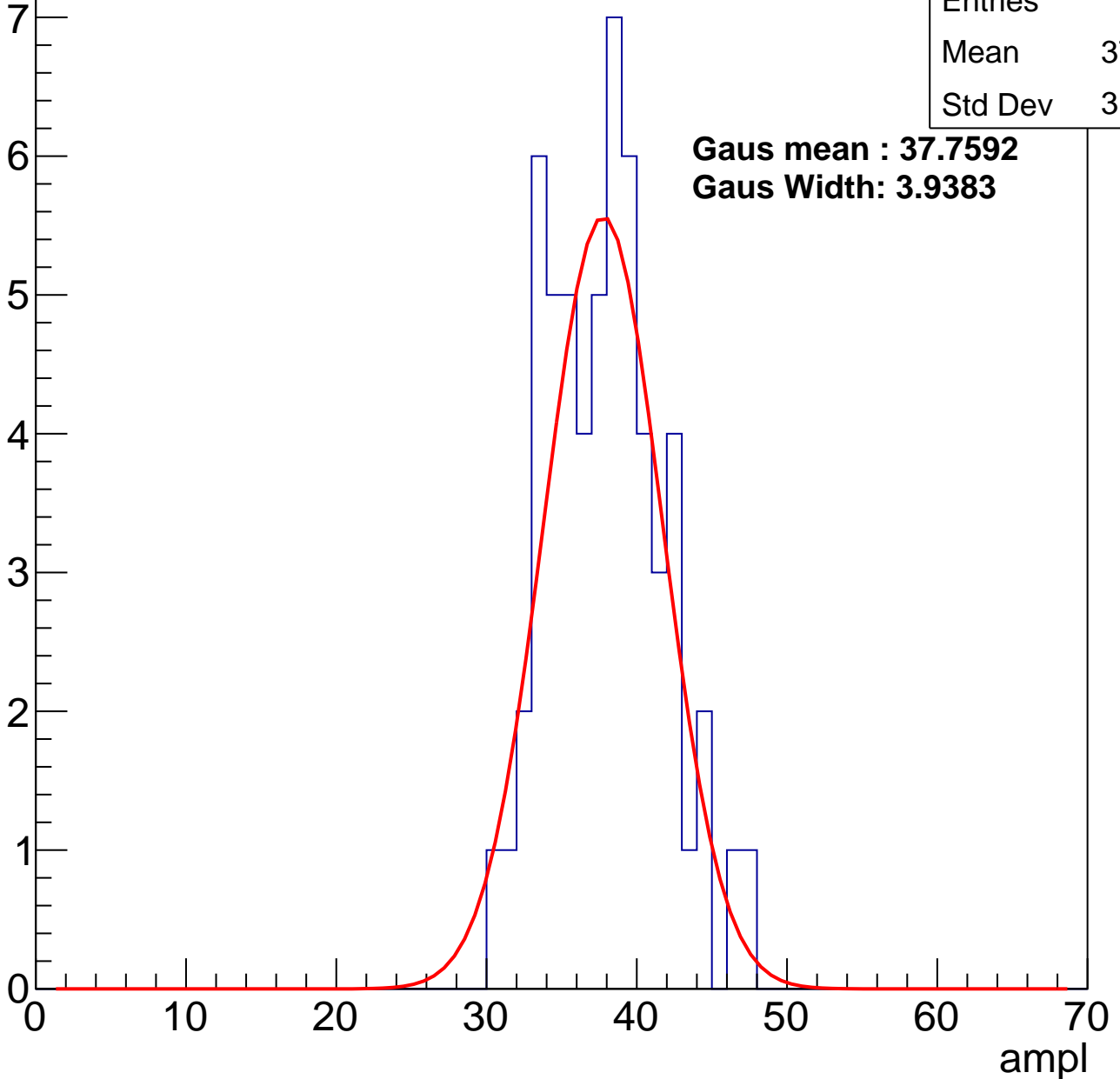
# B1L101S, U18-ch90, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	37.45
Std Dev	3.756

**Gaus mean : 37.7592**  
**Gaus Width: 3.9383**



# B1L101S, U18-ch90, adc2

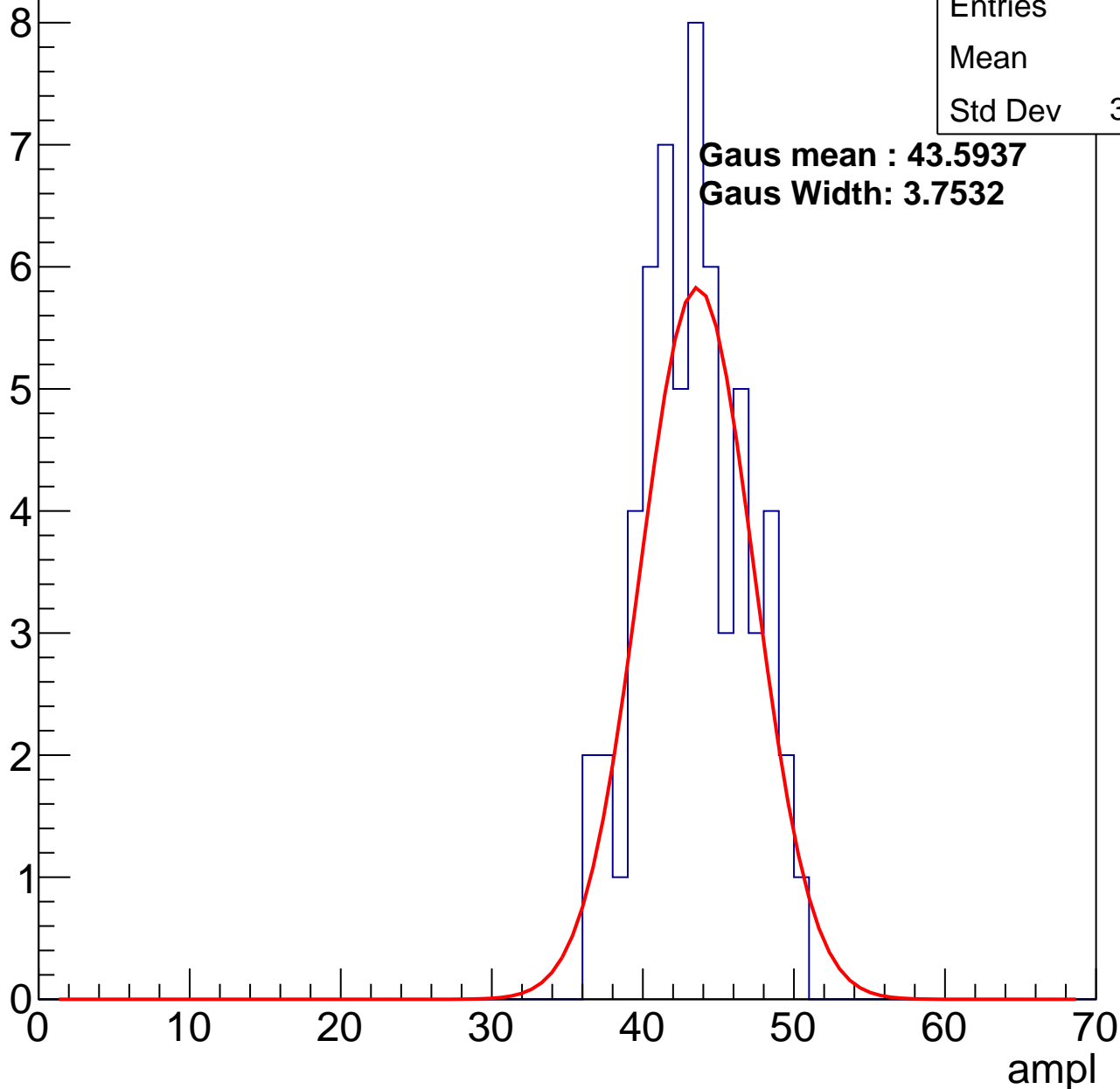
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	42.9
Std Dev	3.388

**Gaus mean : 43.5937**

**Gaus Width: 3.7532**

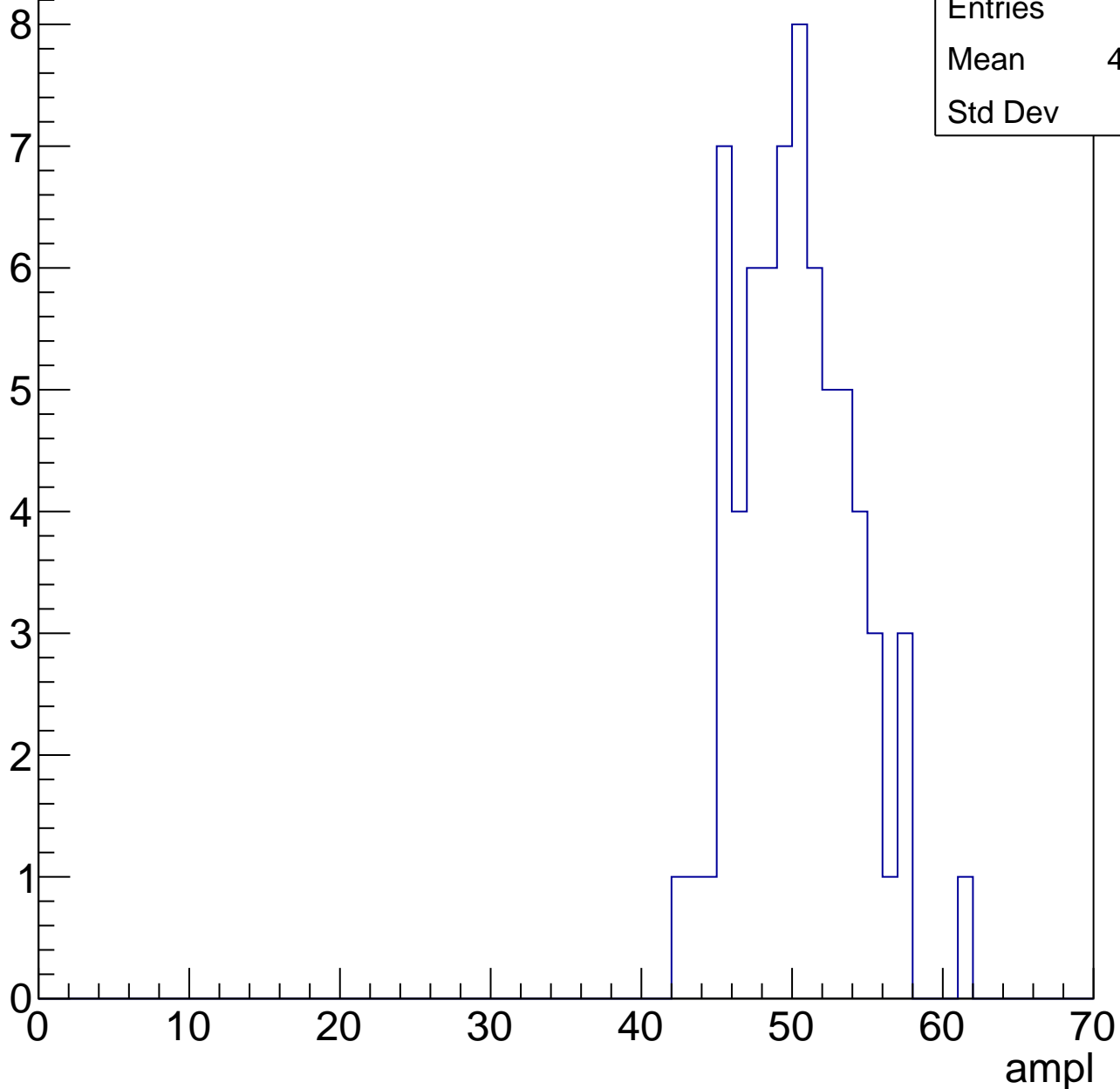


# B1L101S, U18-ch90, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	49.87
Std Dev	3.78

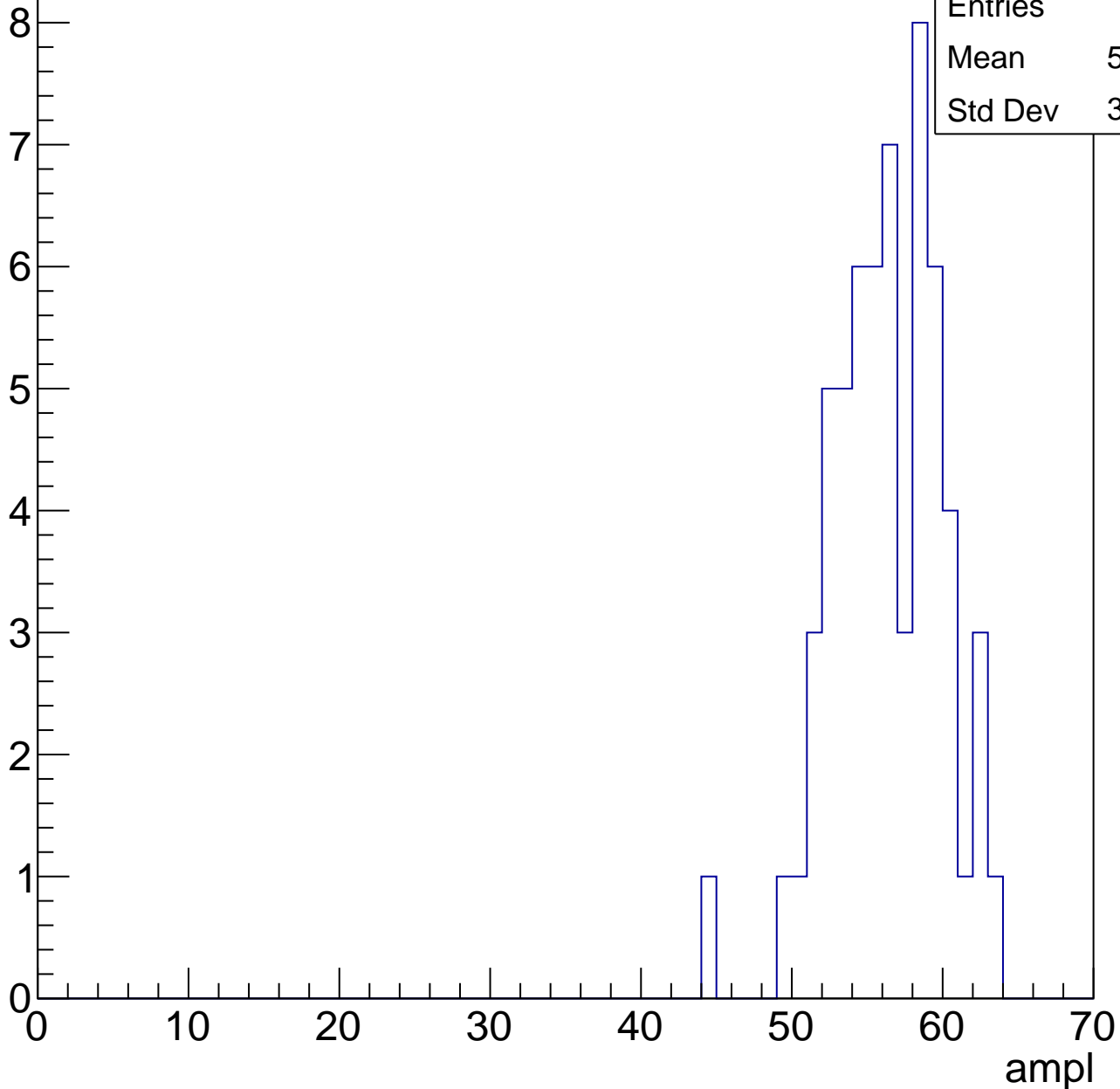


# B1L101S, U18-ch90, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	55.84
Std Dev	3.604

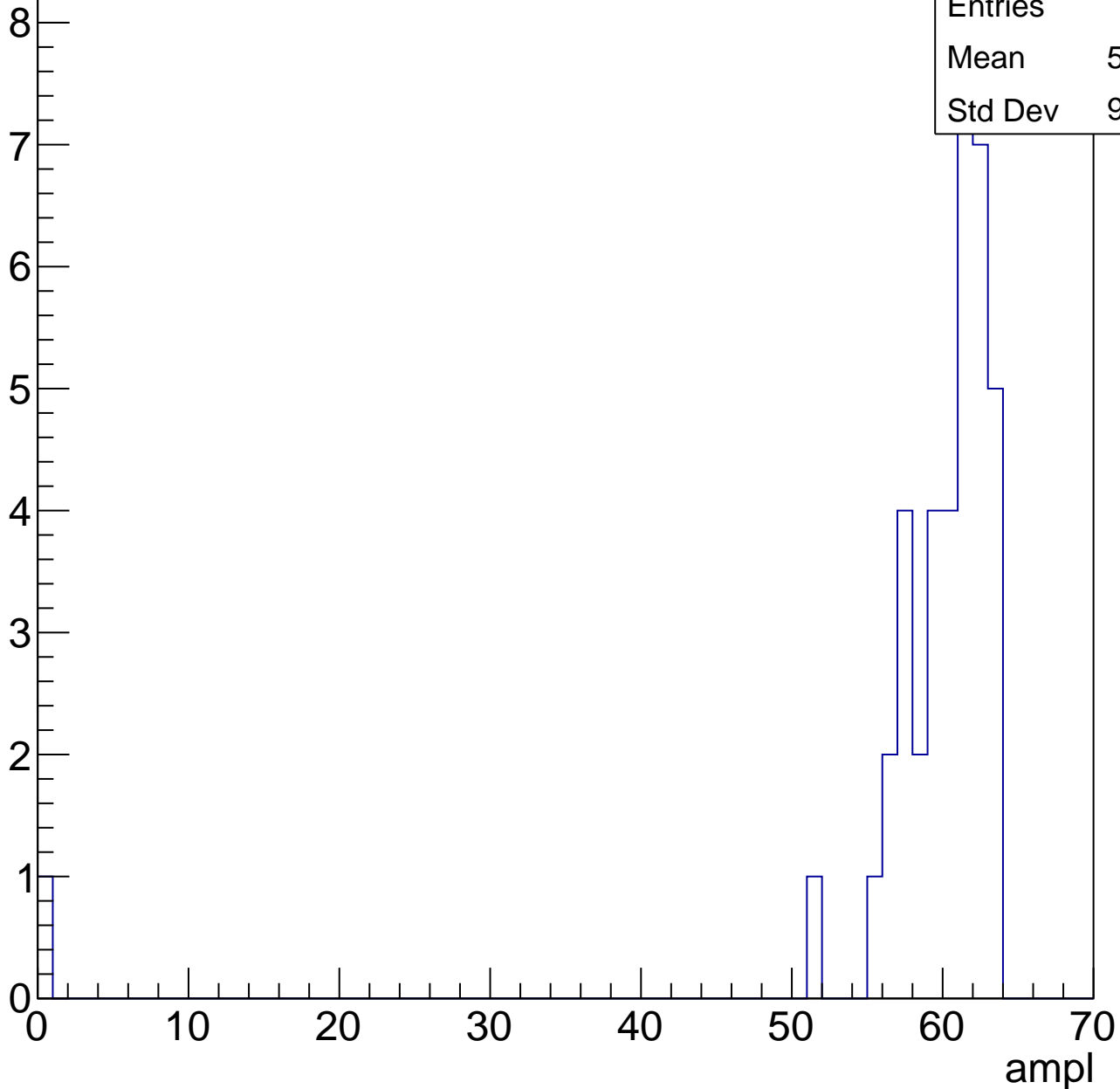


# B1L101S, U18-ch90, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

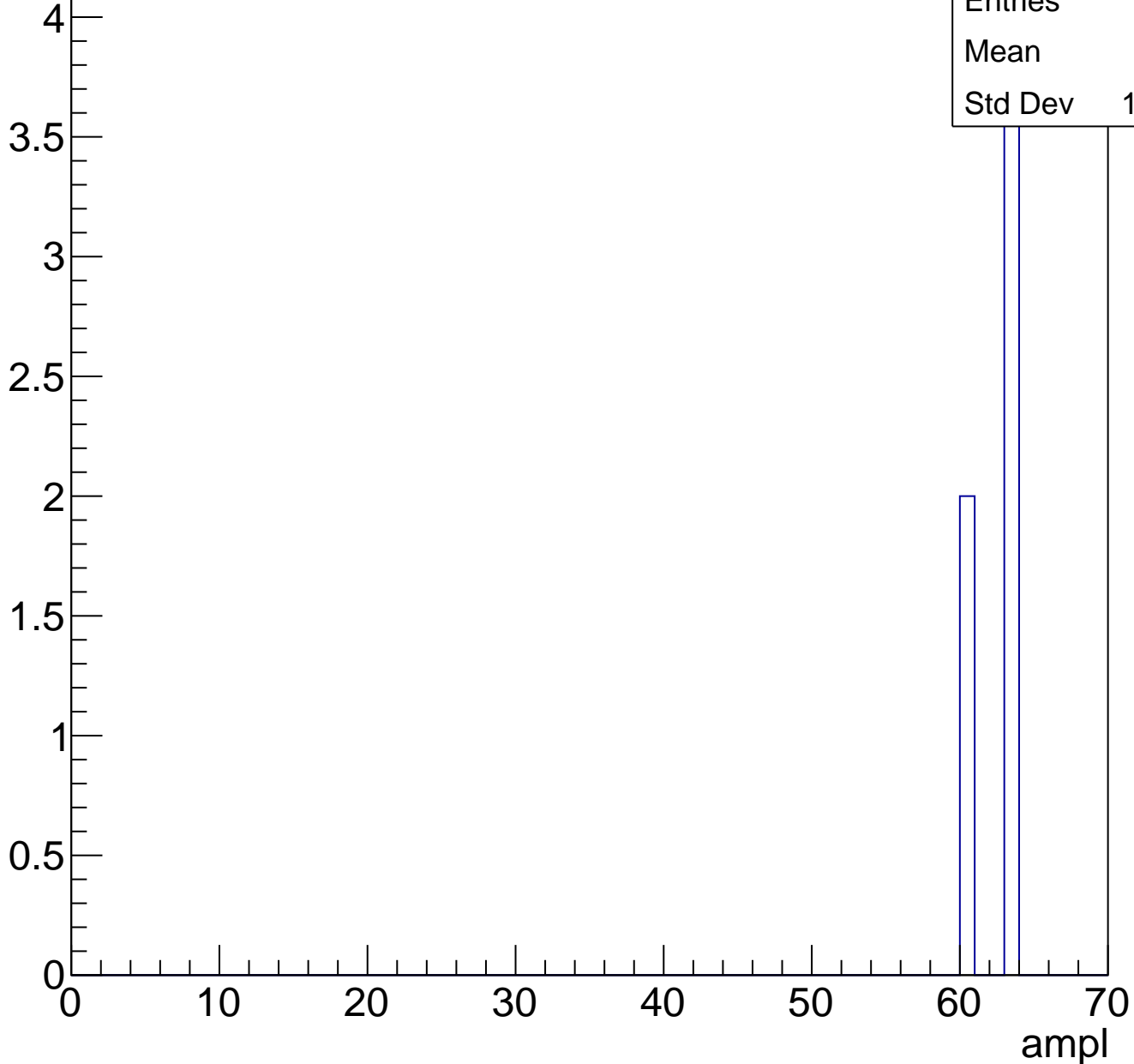
Entries	39
Mean	58.33
Std Dev	9.817



# B1L101S, U18-ch90, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

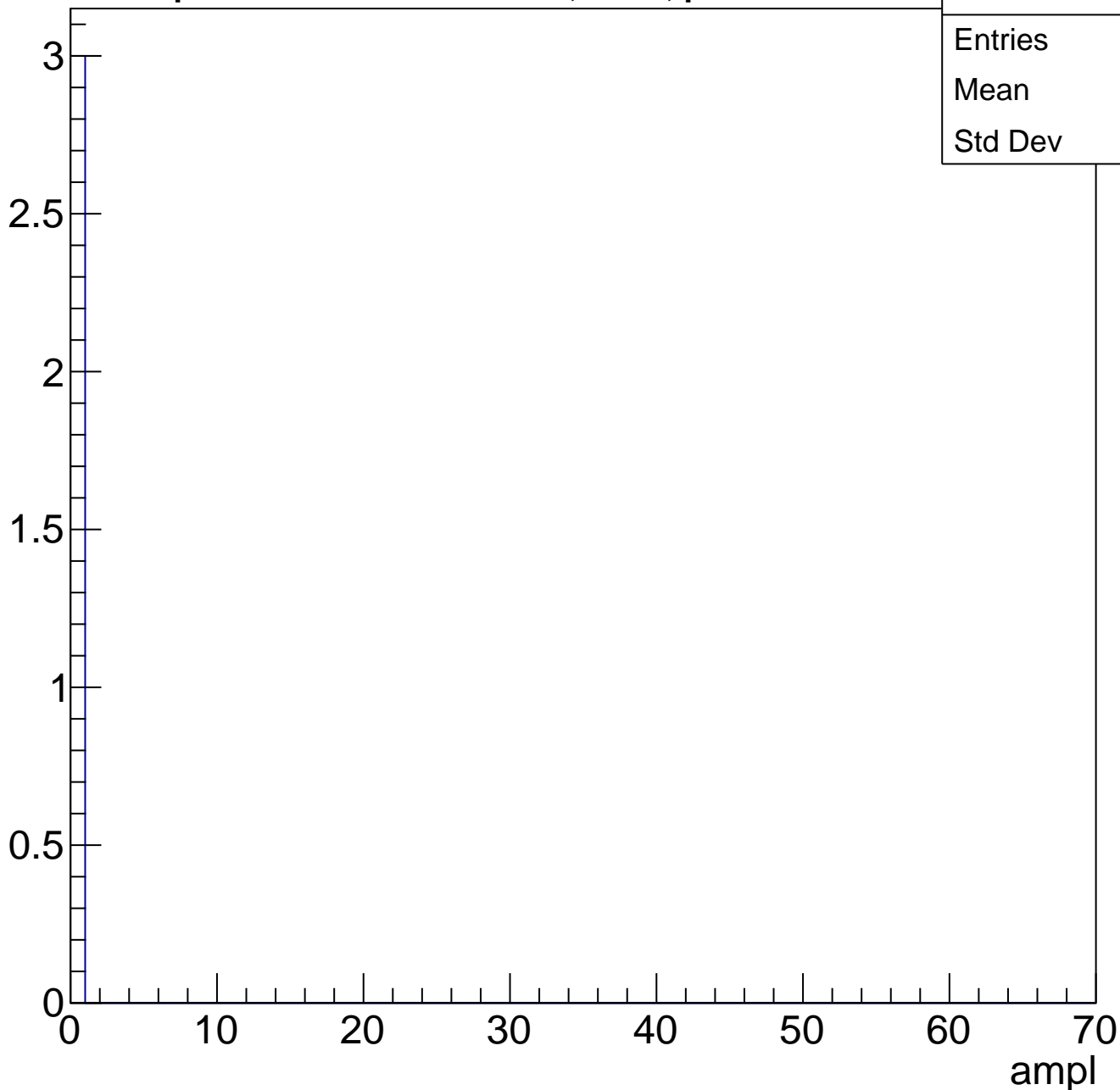




# B1L101S, U18-ch90, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L101S, U18-ch91, adc0

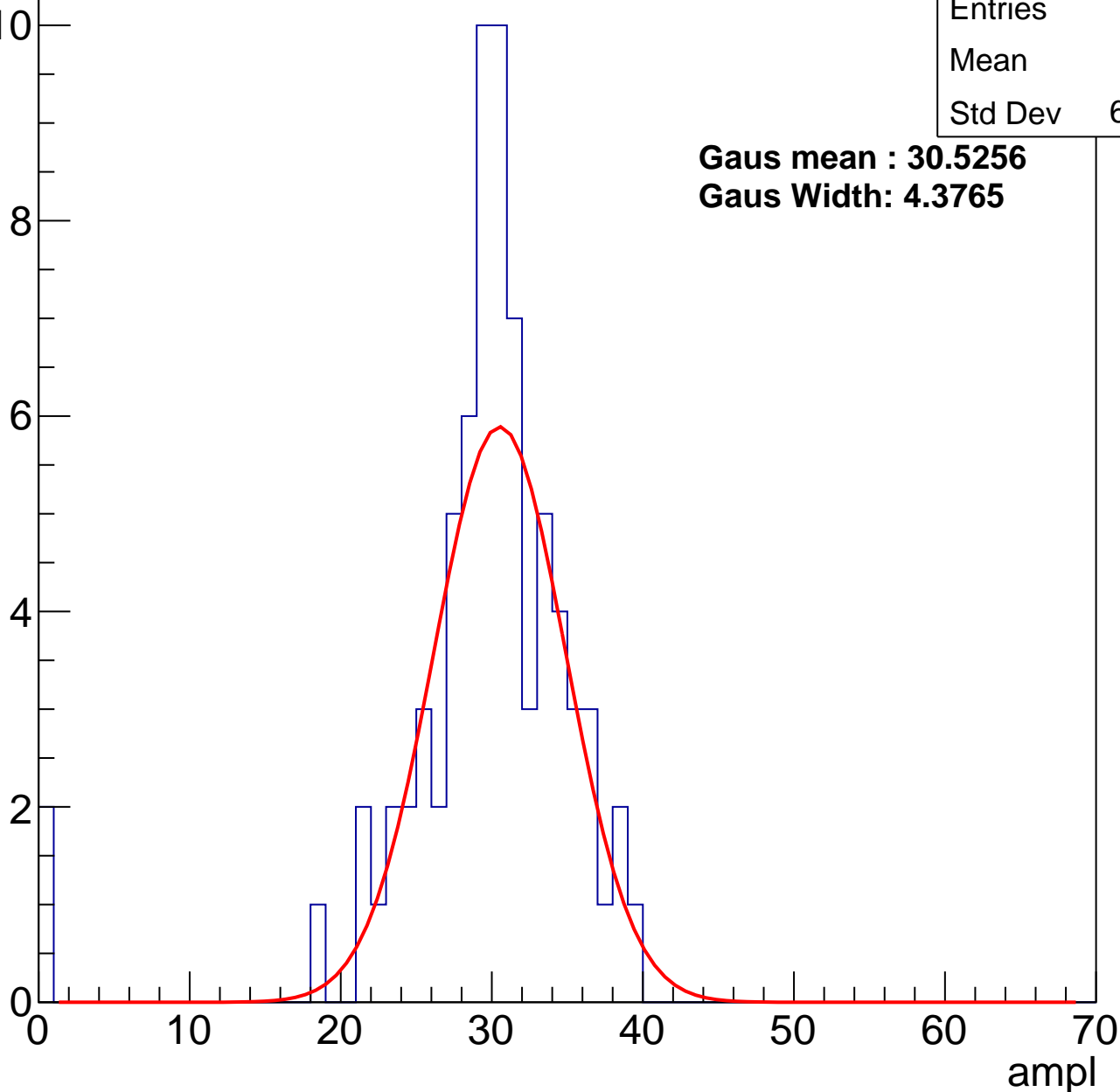
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	29
Std Dev	6.346

**Gaus mean : 30.5256**

**Gaus Width: 4.3765**



# B1L101S, U18-ch91, adc1

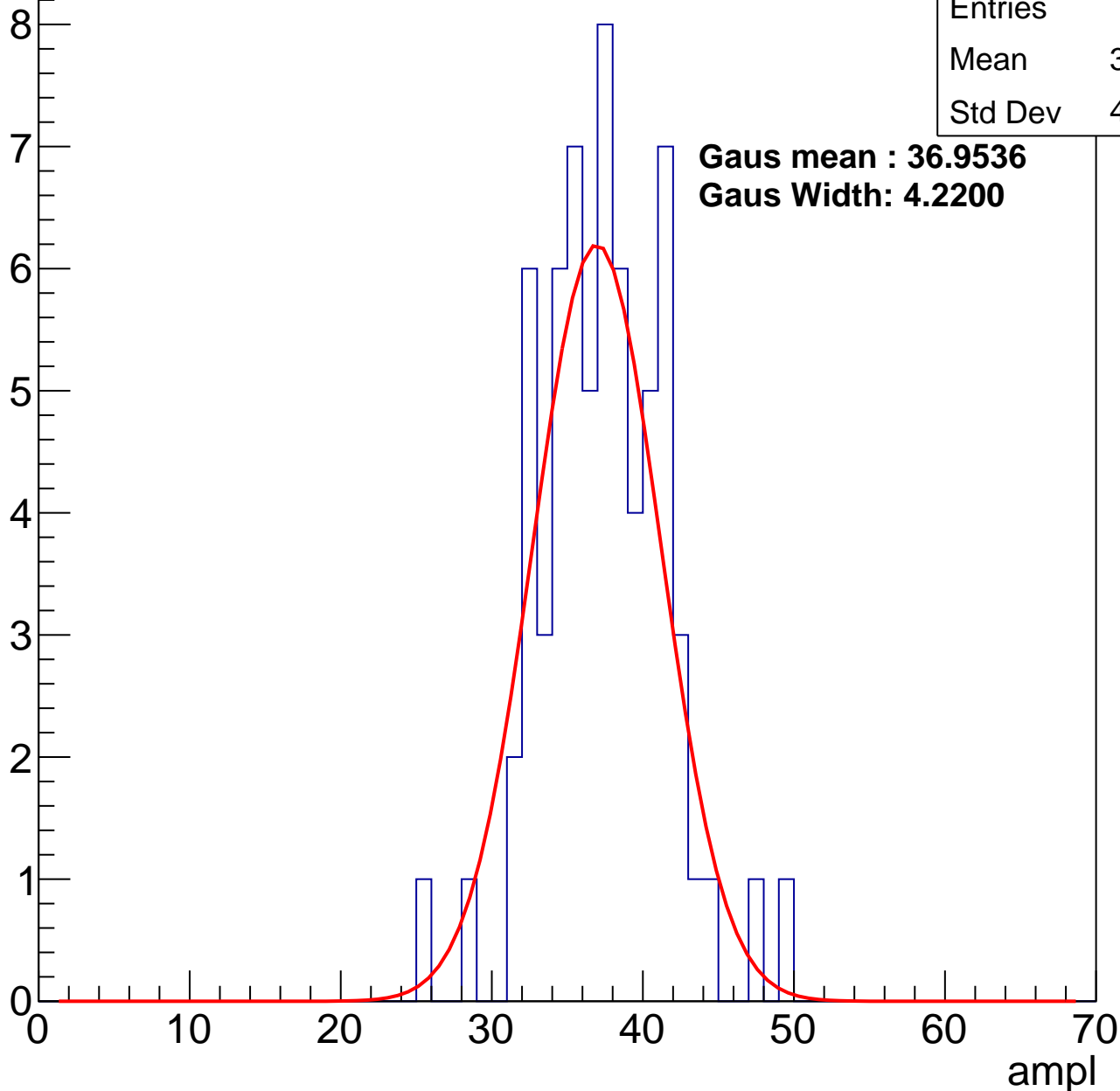
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	36.93
Std Dev	4.138

**Gaus mean : 36.9536**

**Gaus Width: 4.2200**



# B1L101S, U18-ch91, adc2

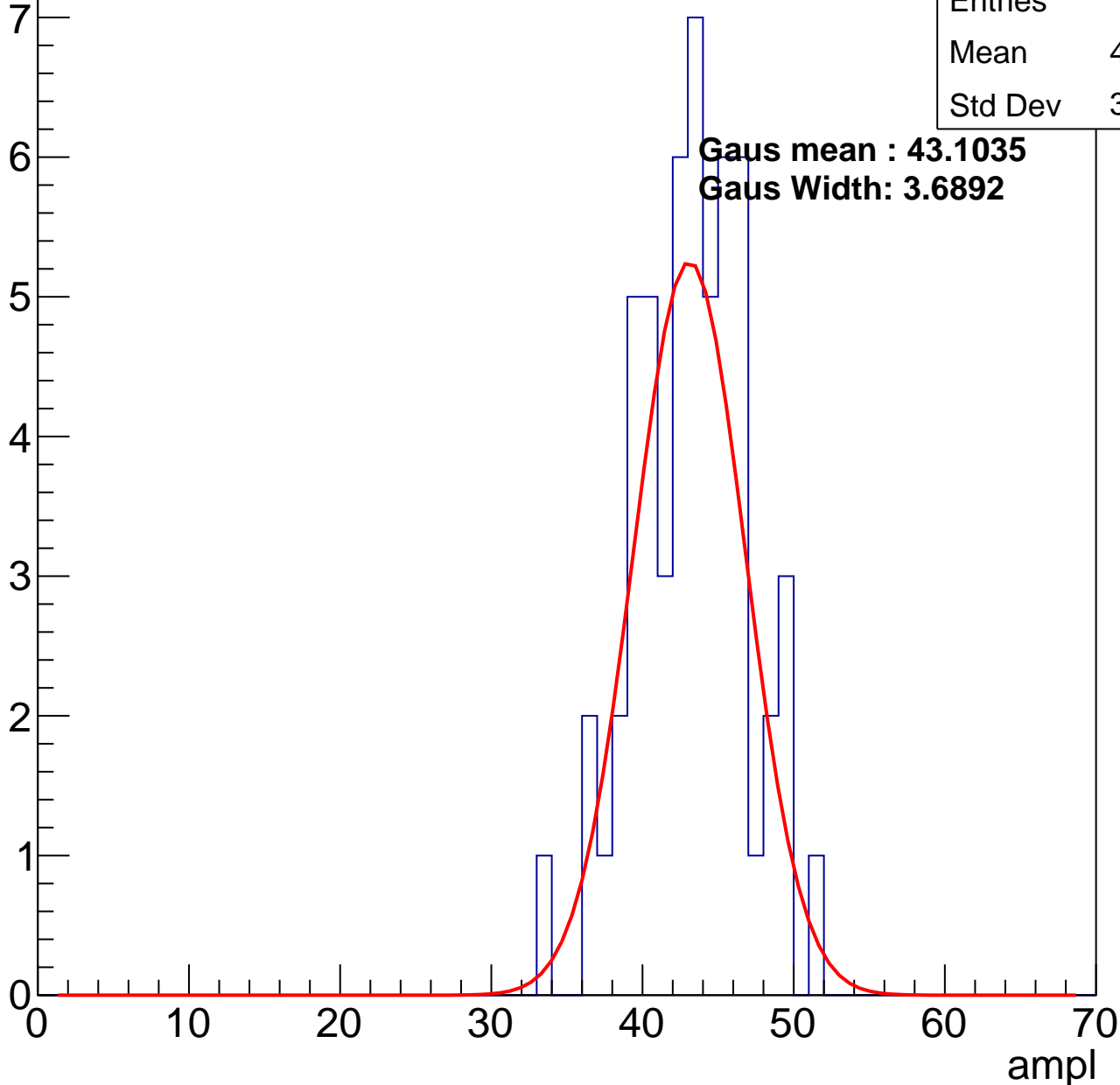
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	42.79
Std Dev	3.648

**Gaus mean : 43.1035**

**Gaus Width: 3.6892**

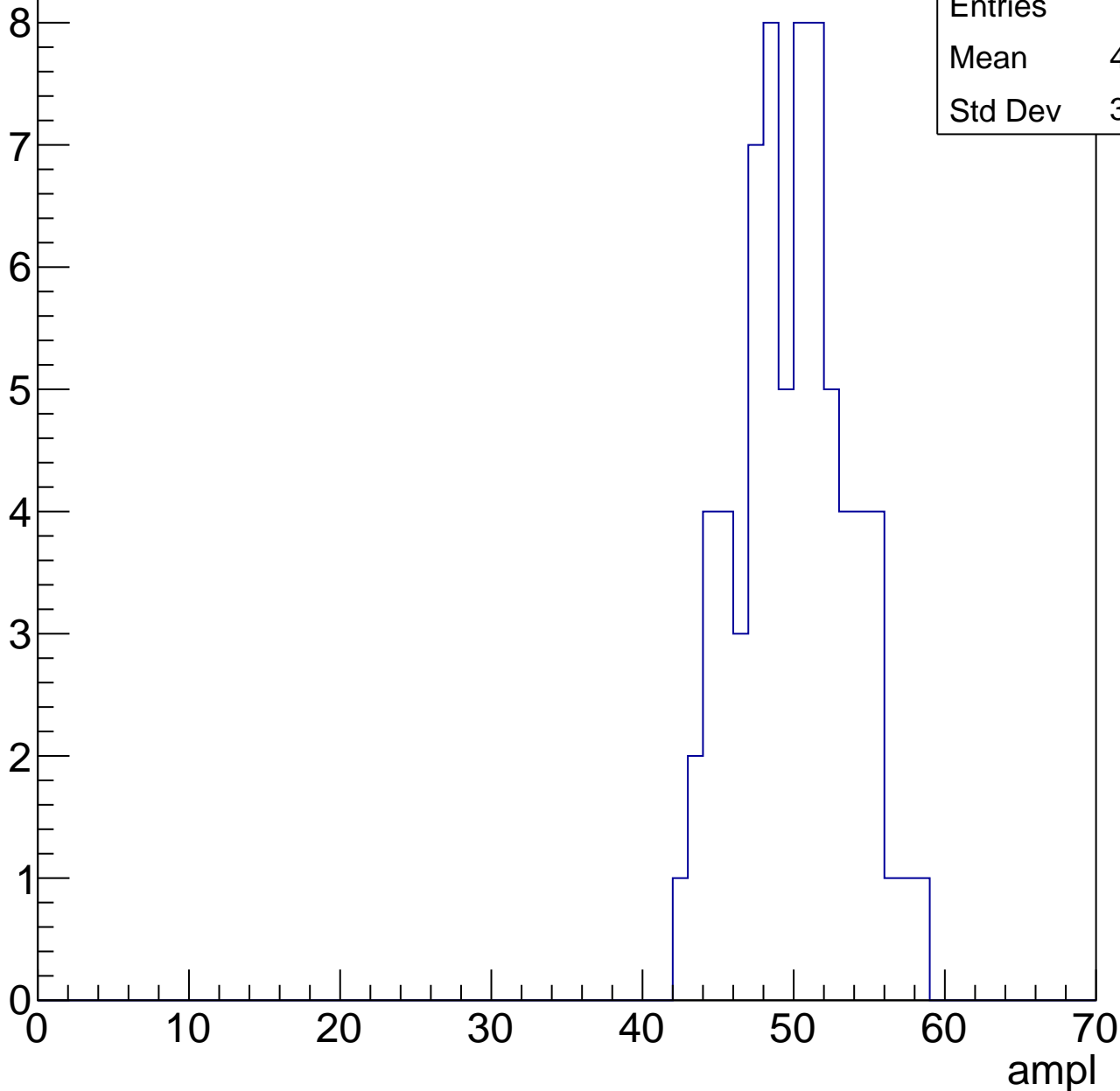


# B1L101S, U18-ch91, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	49.53
Std Dev	3.616

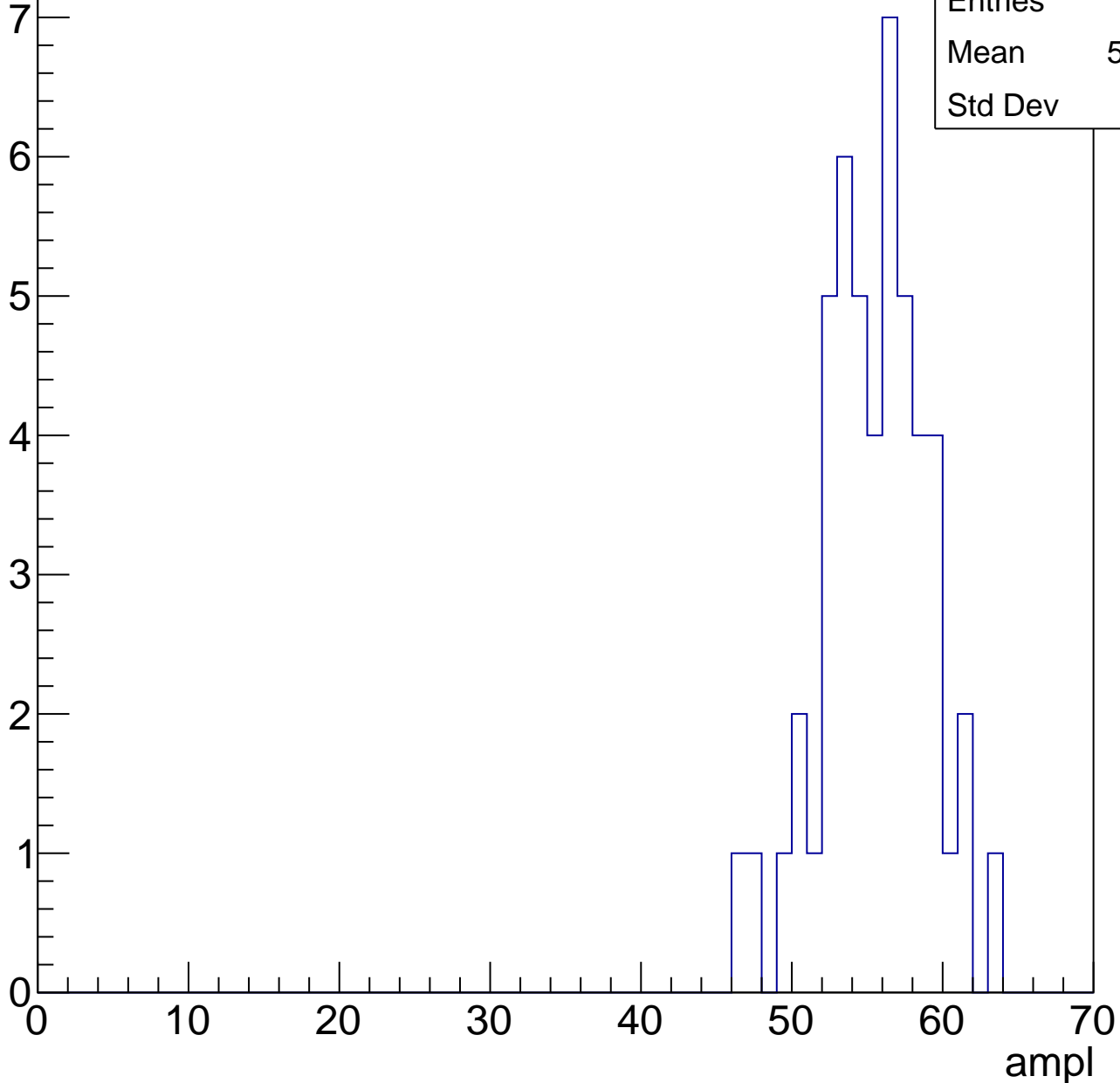


# B1L101S, U18-ch91, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	55.02
Std Dev	3.49

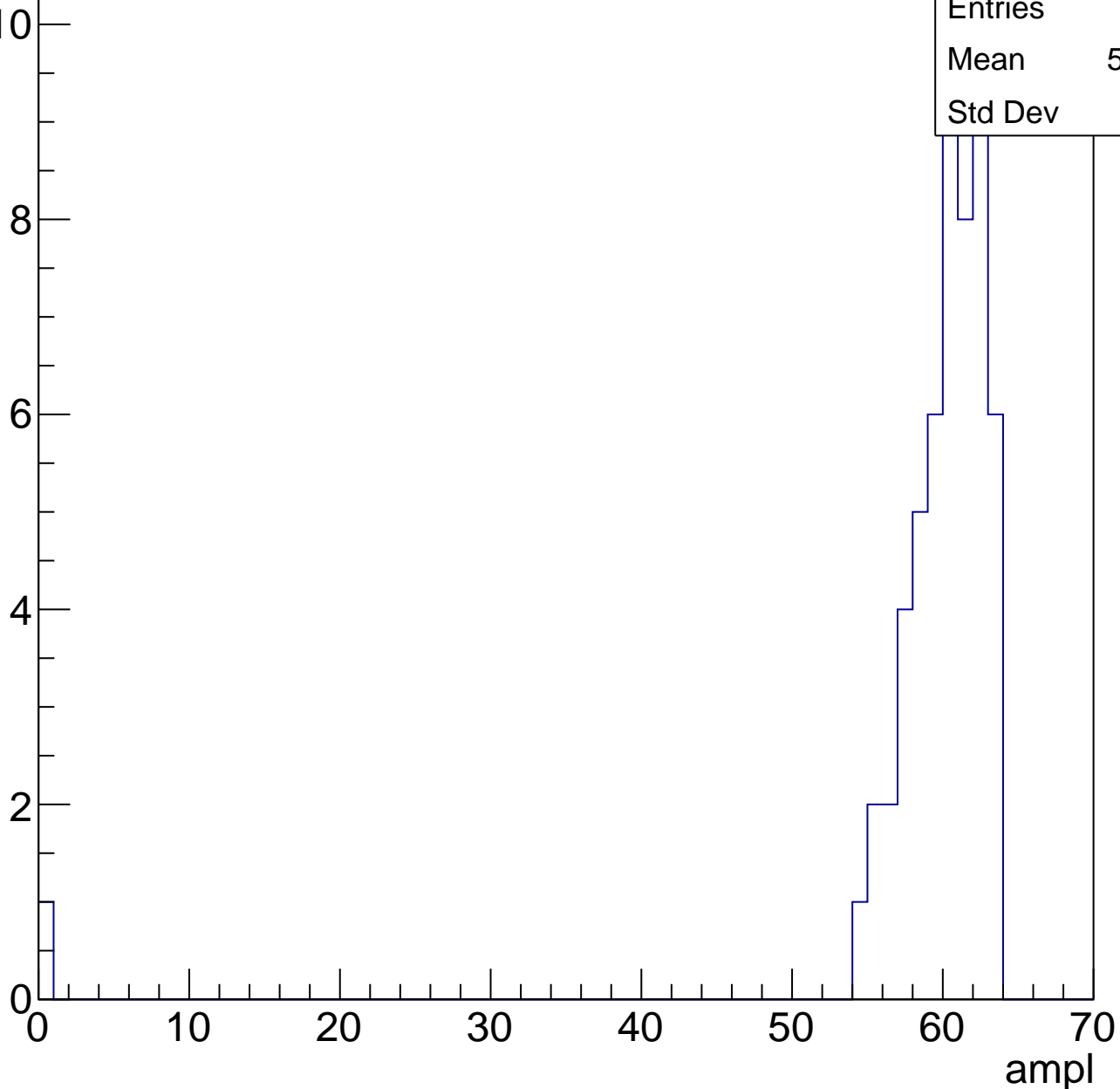


# B1L101S, U18-ch91, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	58.78
Std Dev	8.39



# B1L101S, U18-ch91, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch91, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch92, adc0

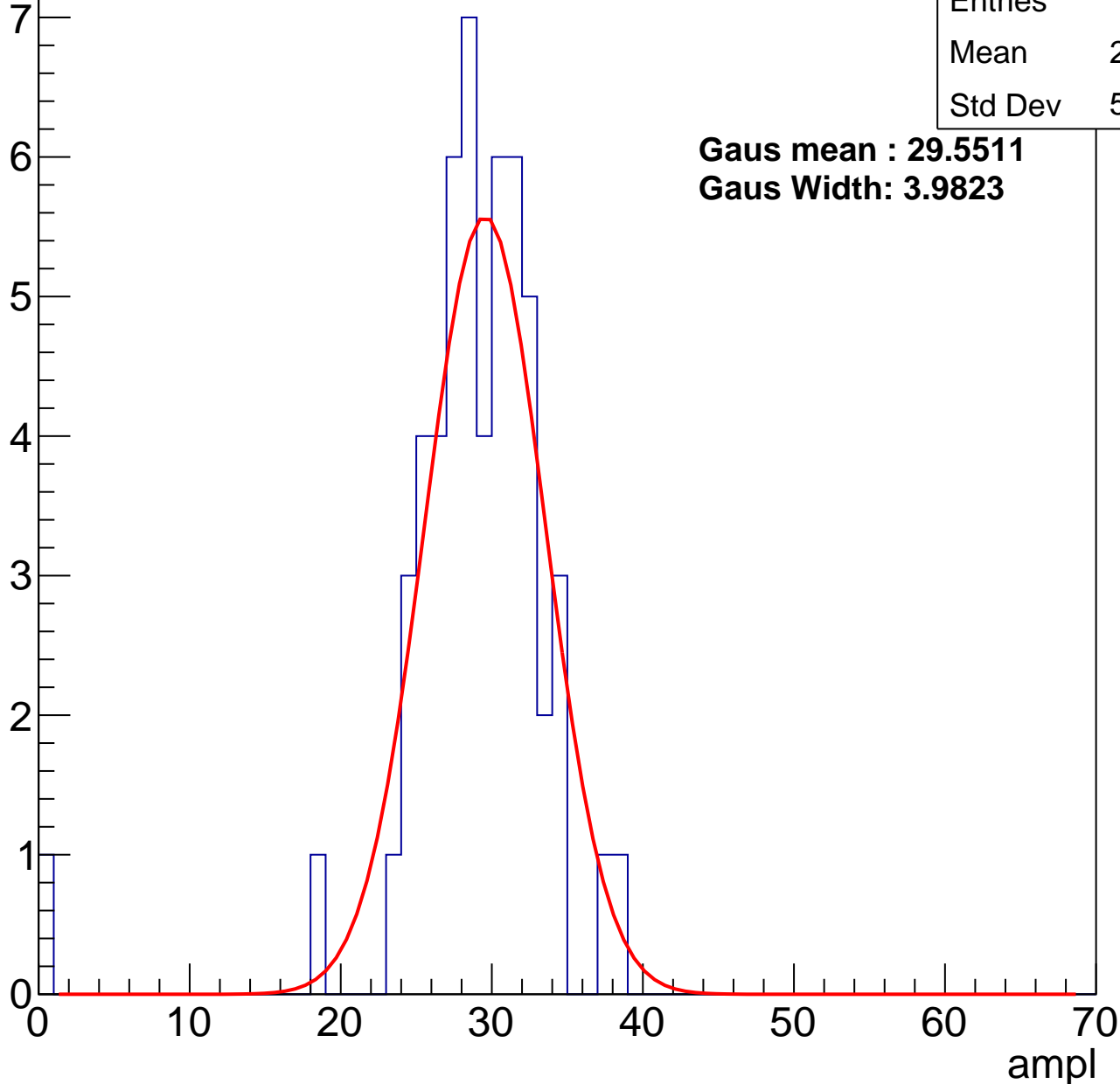
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	28.36
Std Dev	5.237

**Gaus mean : 29.5511**

**Gaus Width: 3.9823**



# B1L101S, U18-ch92, adc1

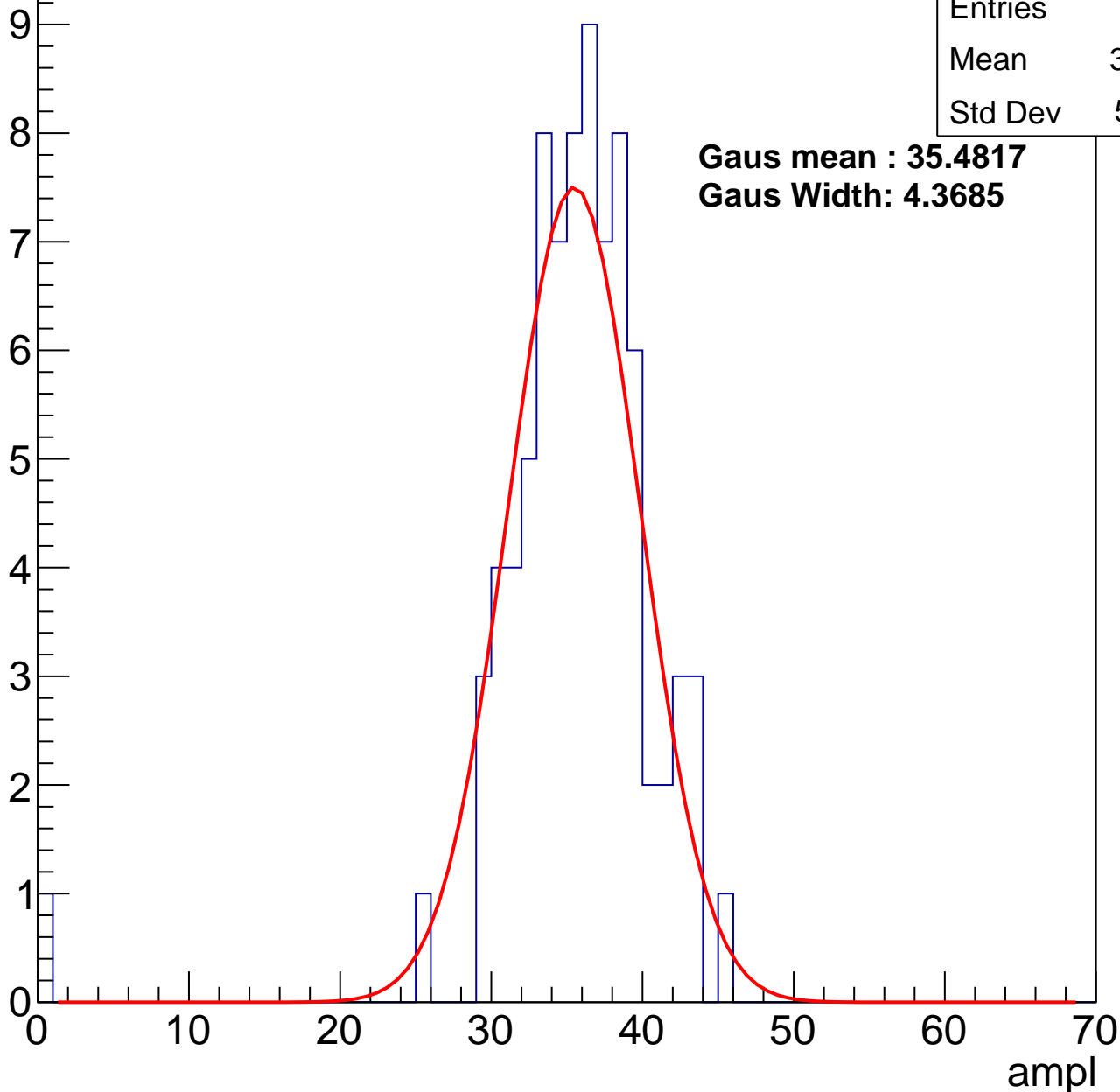
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	82
Mean	35.13
Std Dev	5.461

**Gaus mean : 35.4817**

**Gaus Width: 4.3685**



# B1L101S, U18-ch92, adc2

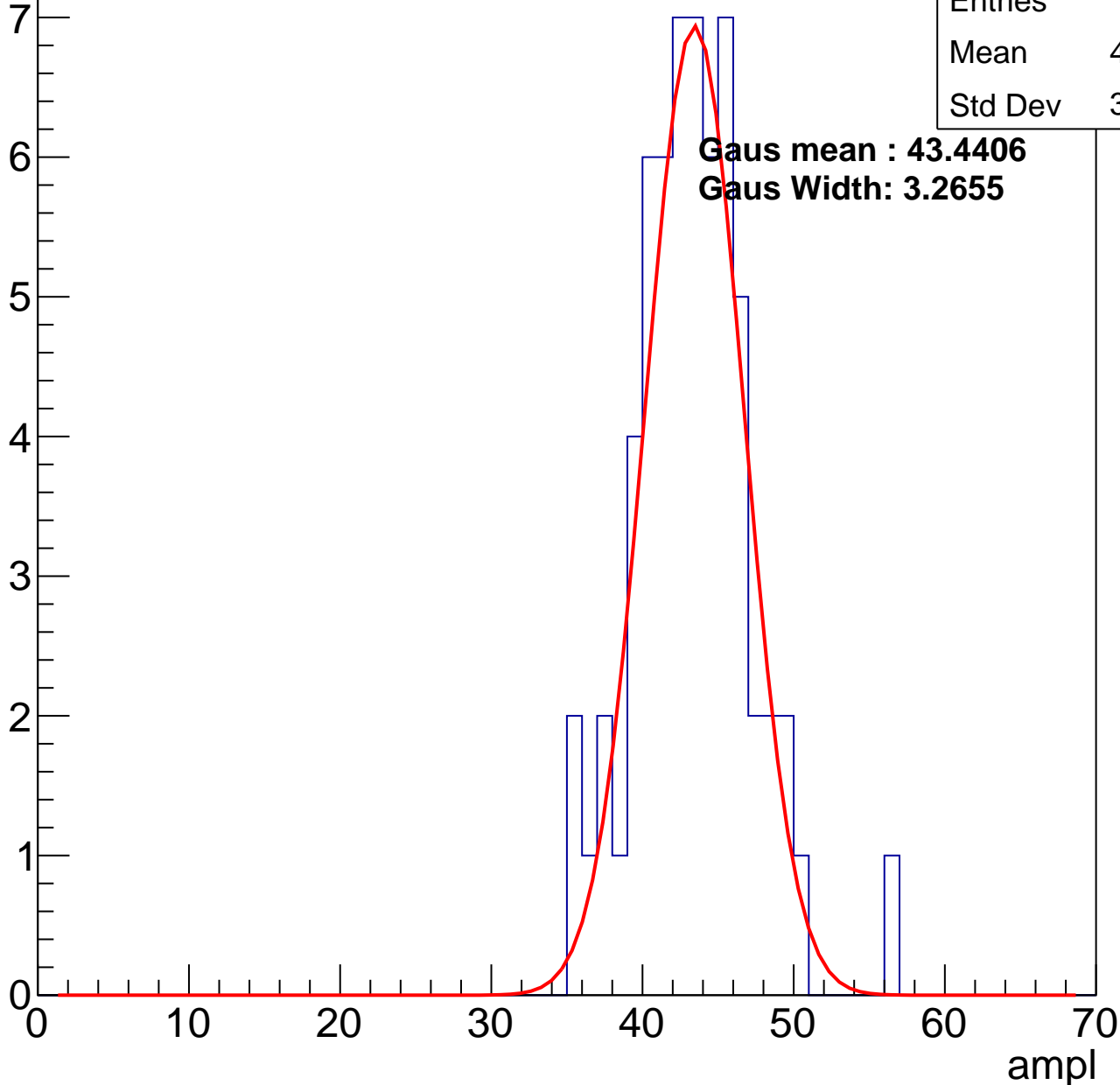
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	42.87
Std Dev	3.752

**Gaus mean : 43.4406**

**Gaus Width: 3.2655**

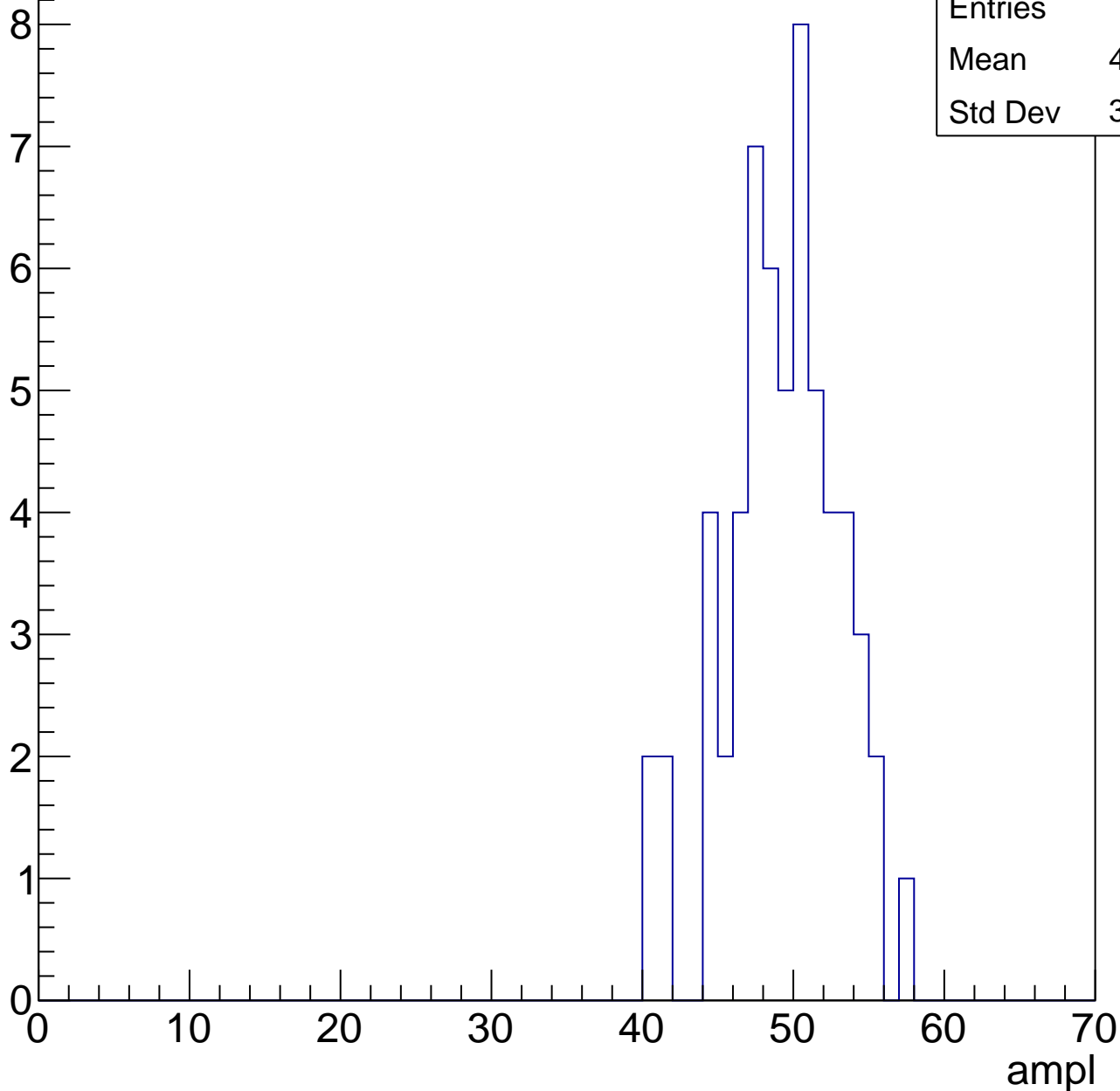


# B1L101S, U18-ch92, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	48.78
Std Dev	3.746

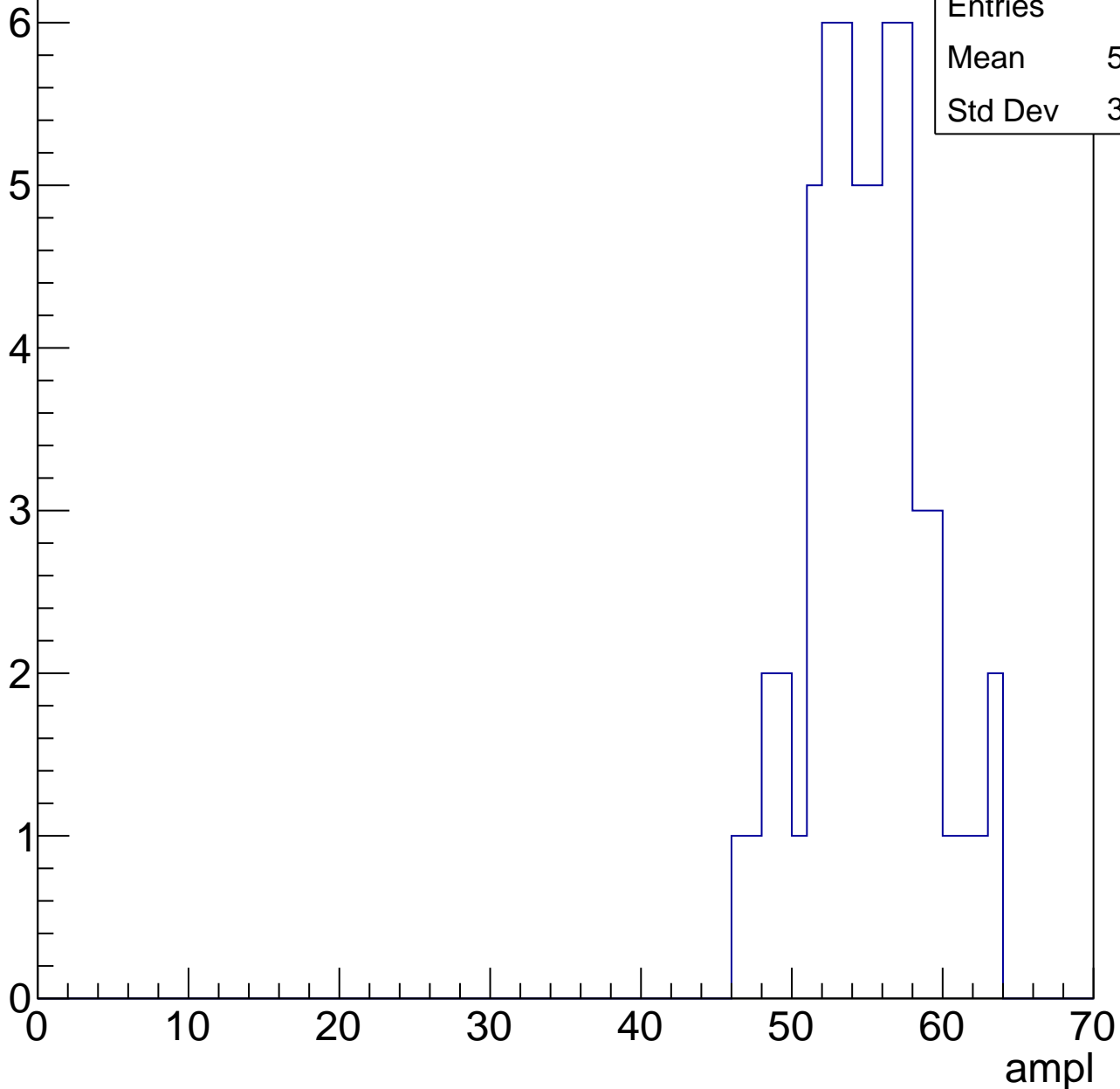


# B1L101S, U18-ch92, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	54.47
Std Dev	3.816

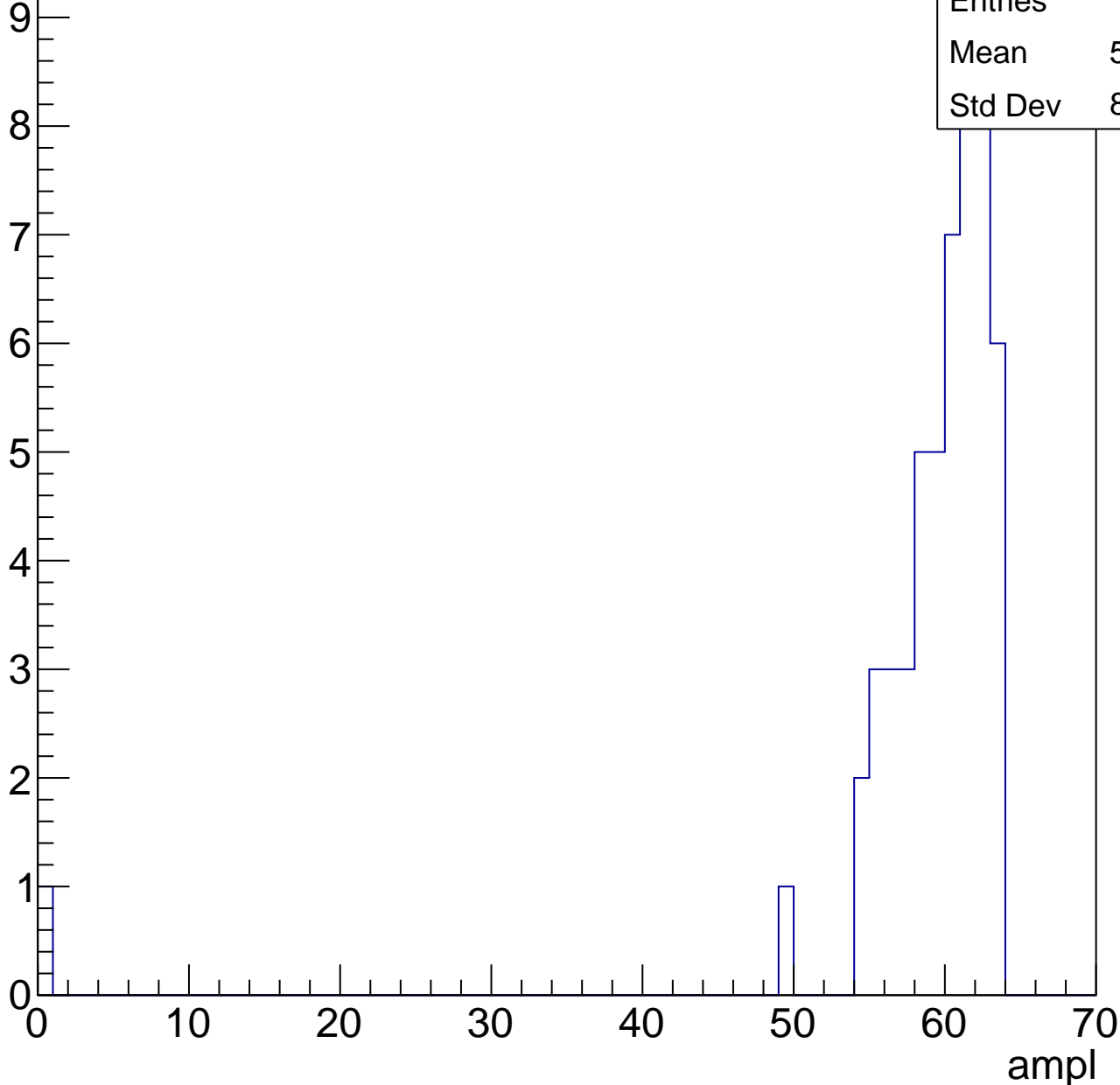


# B1L101S, U18-ch92, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	58.28
Std Dev	8.586



# B1L101S, U18-ch92, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

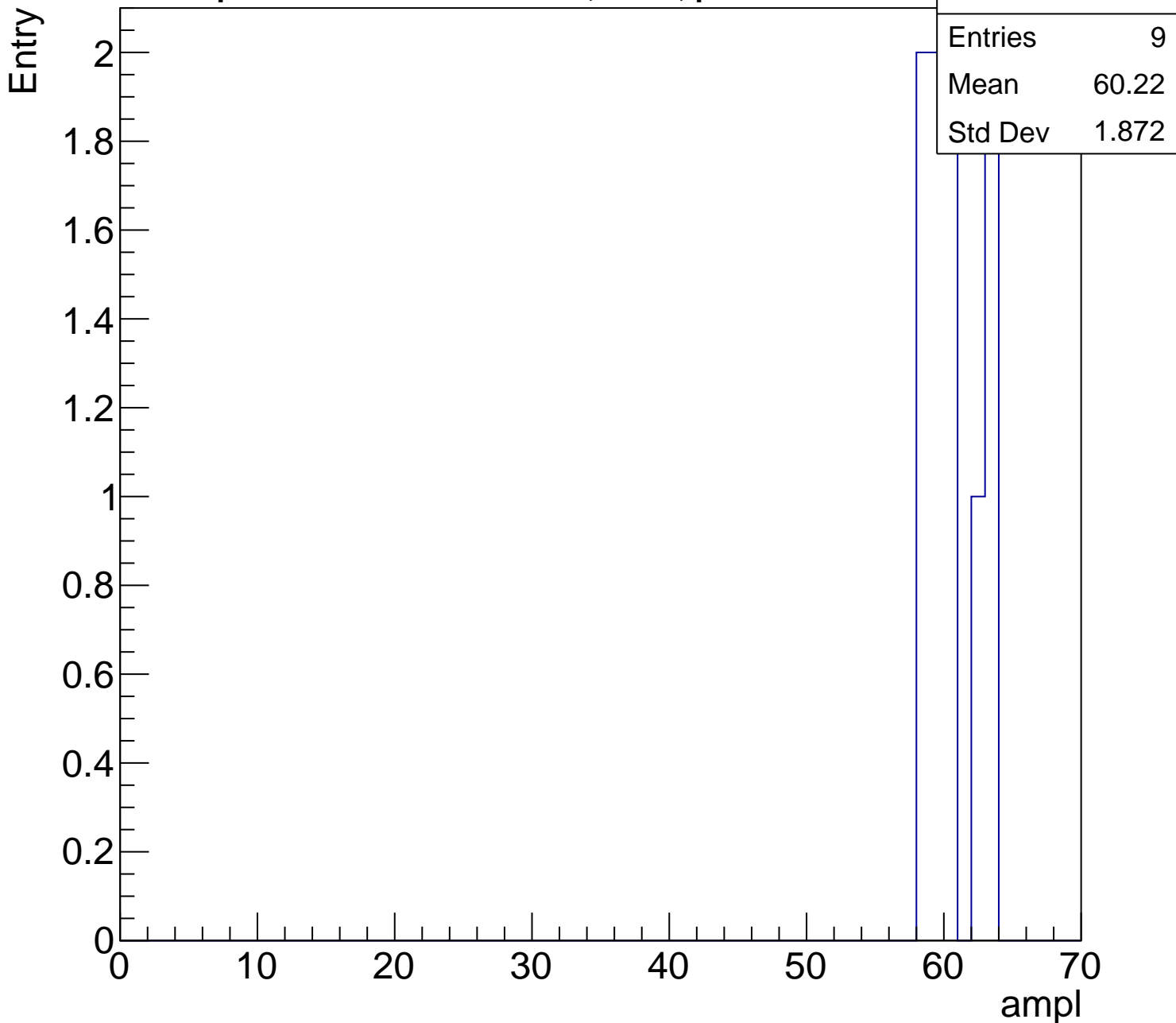
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	9
Mean	60.22
Std Dev	1.872

0 10 20 30 40 50 60 70

ampl





# B1L101S, U18-ch92, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U18-ch93, adc0

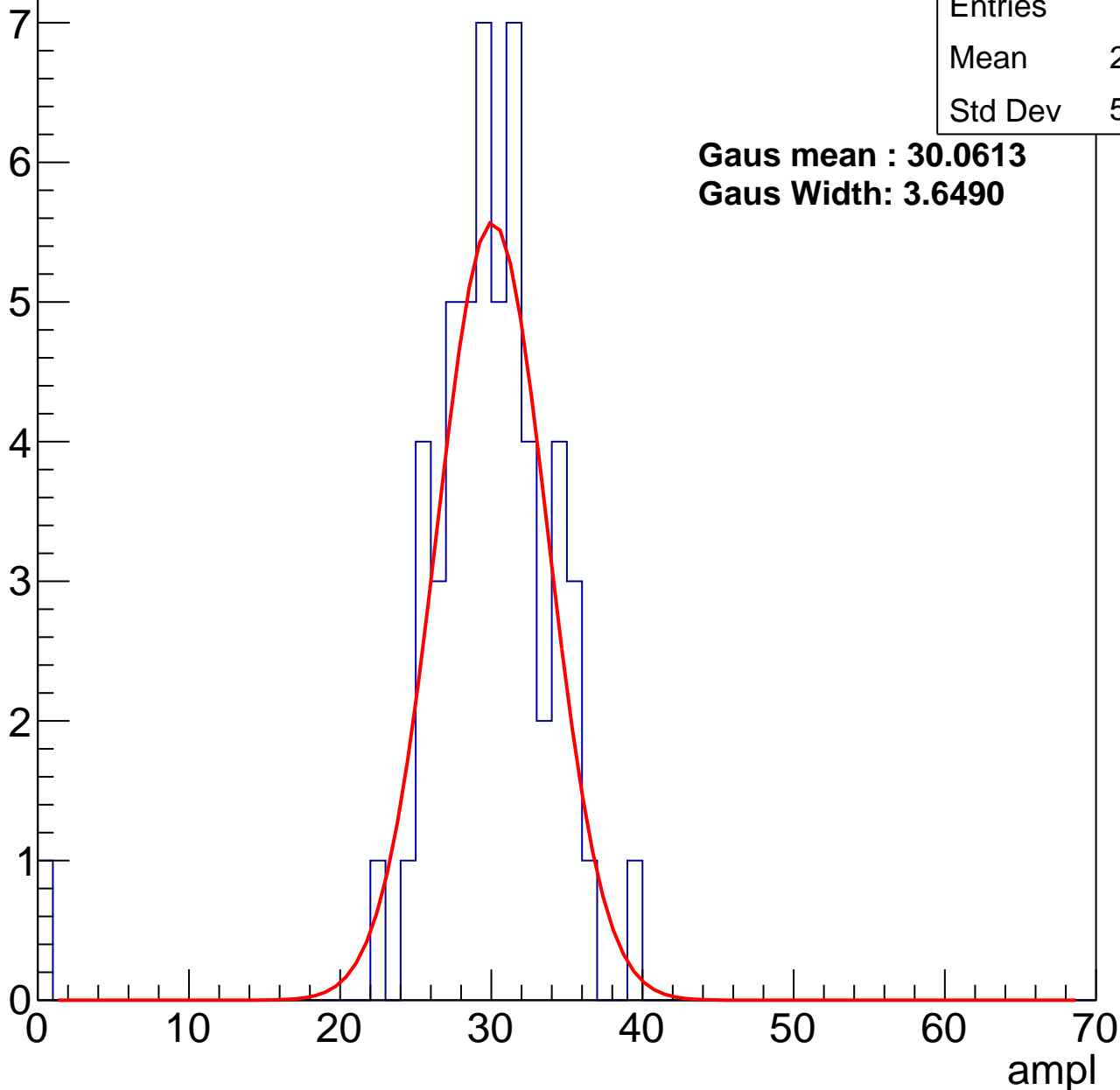
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	29.24
Std Dev	5.246

**Gaus mean : 30.0613**

**Gaus Width: 3.6490**



# B1L101S, U18-ch93, adc1

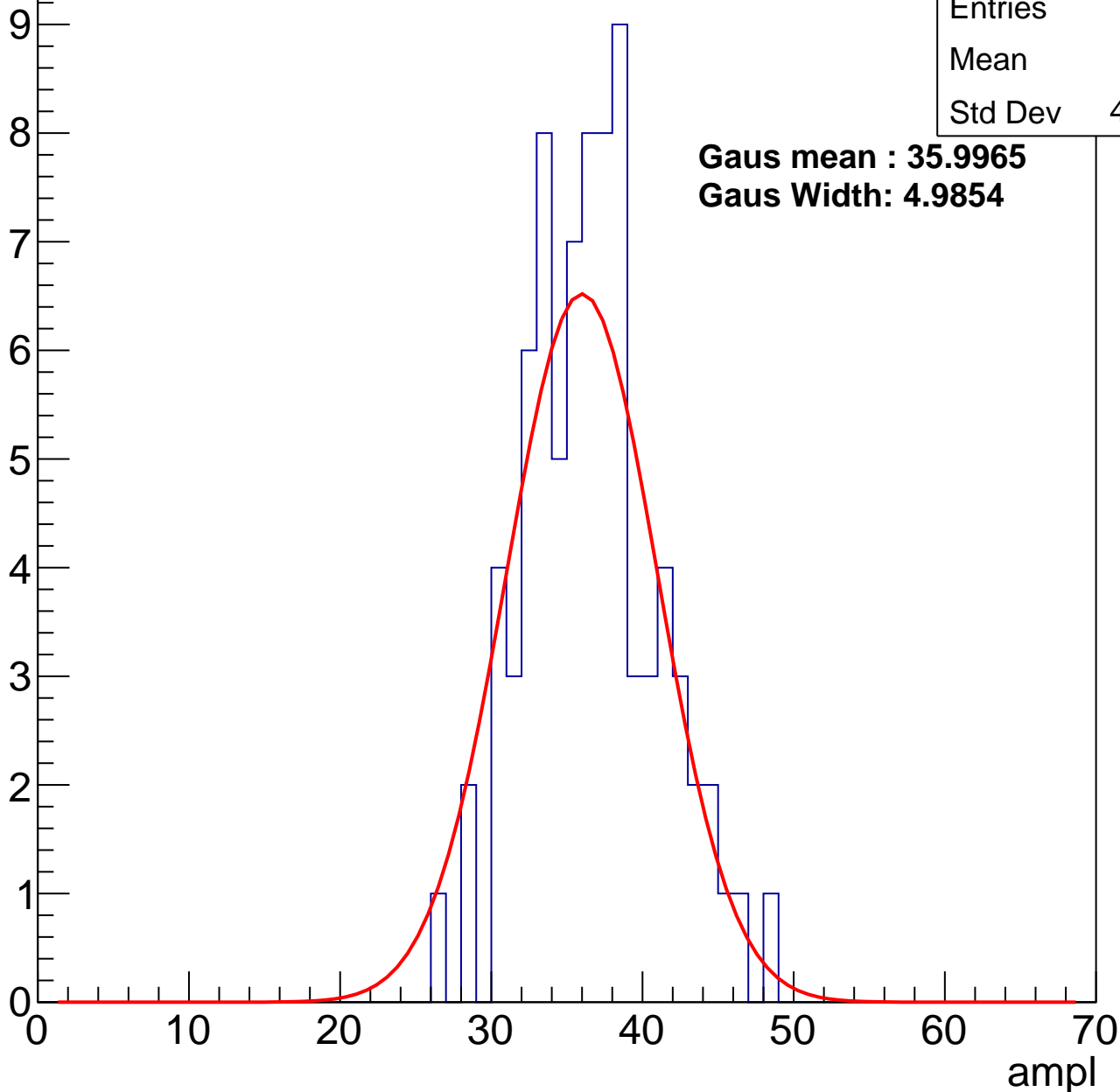
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	81
Mean	36.2
Std Dev	4.327

**Gaus mean : 35.9965**

**Gaus Width: 4.9854**



# B1L101S, U18-ch93, adc2

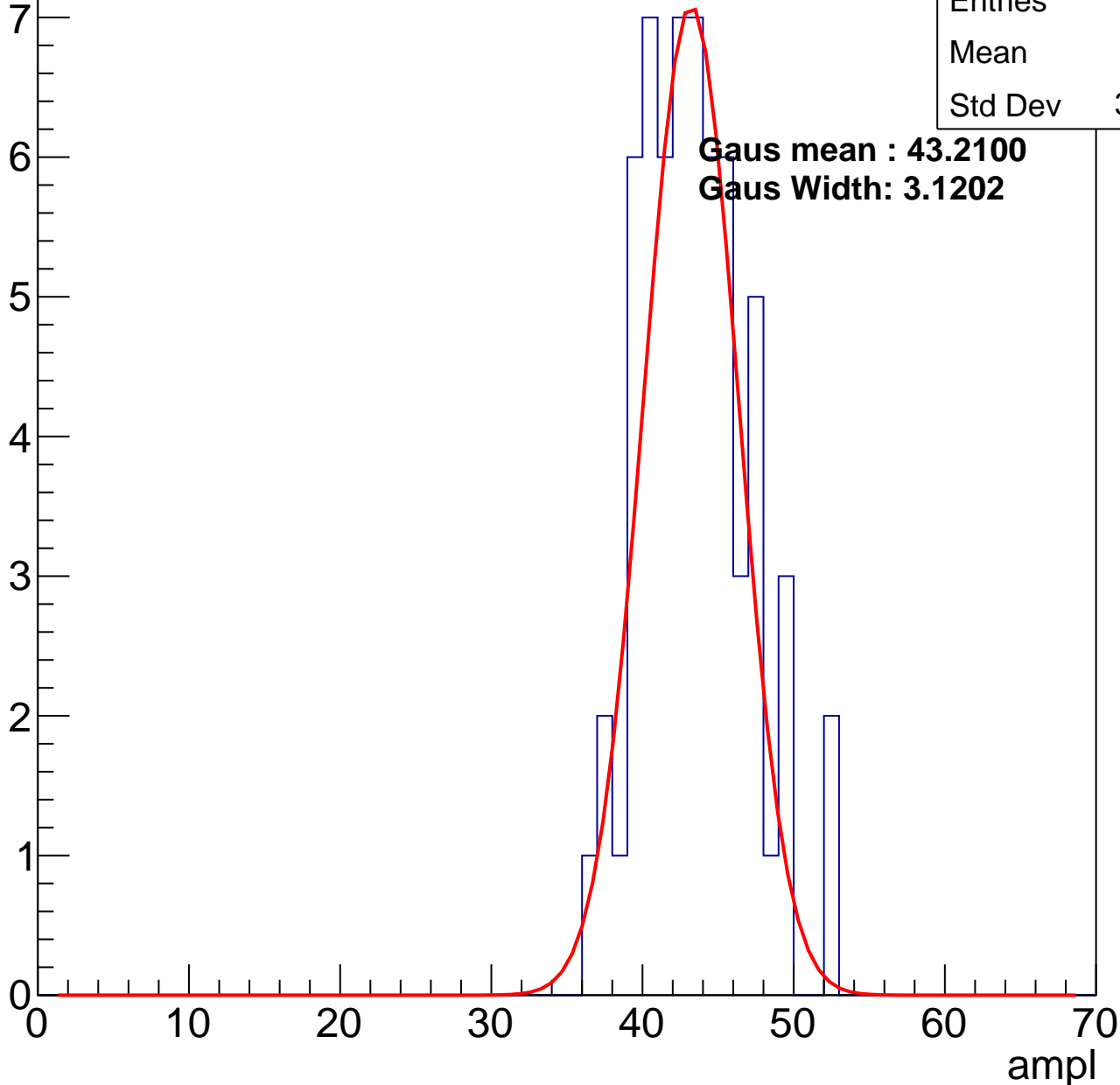
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	43
Std Dev	3.491

**Gaus mean : 43.2100**

**Gaus Width: 3.1202**

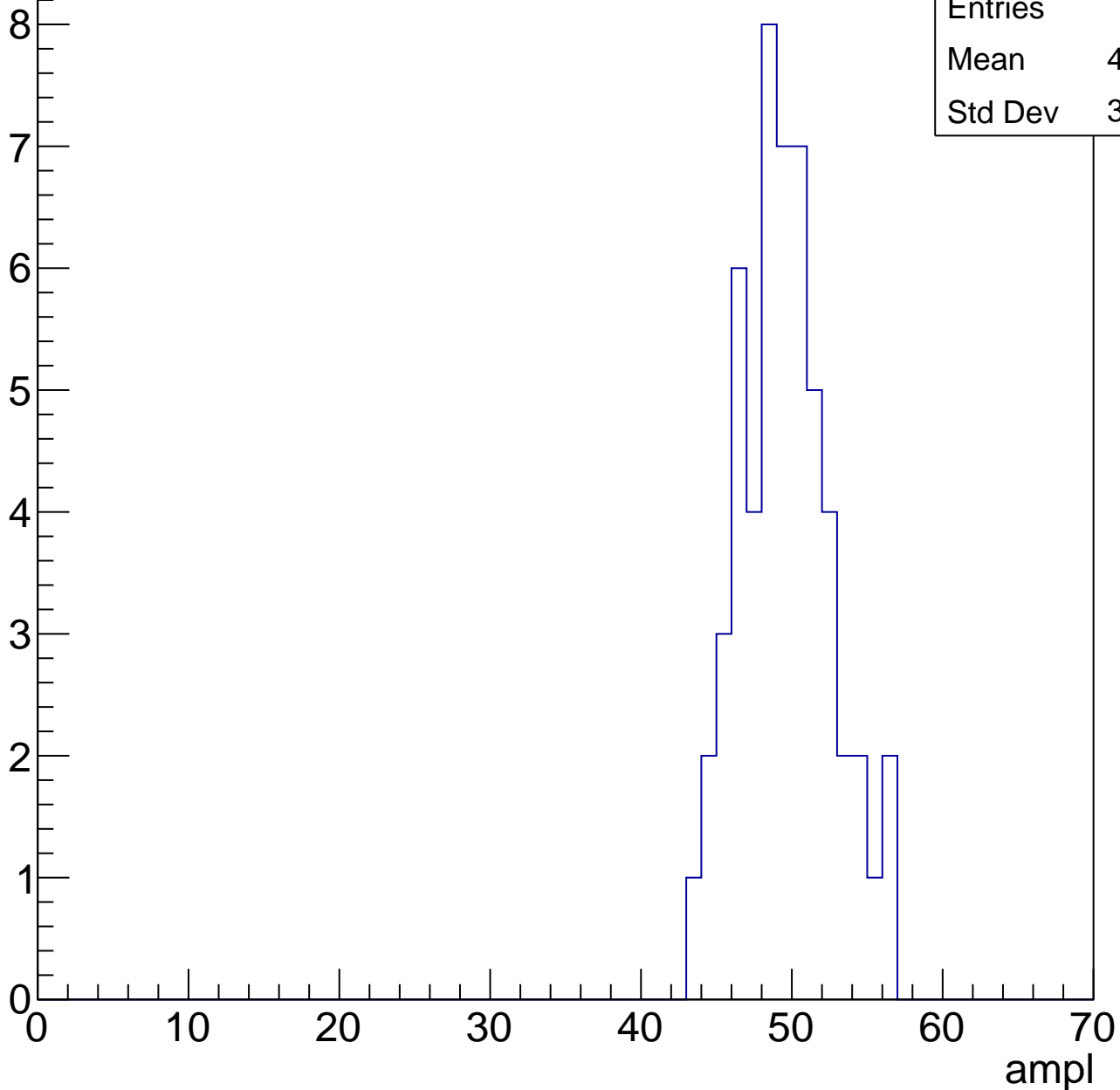


# B1L101S, U18-ch93, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	49.09
Std Dev	3.014

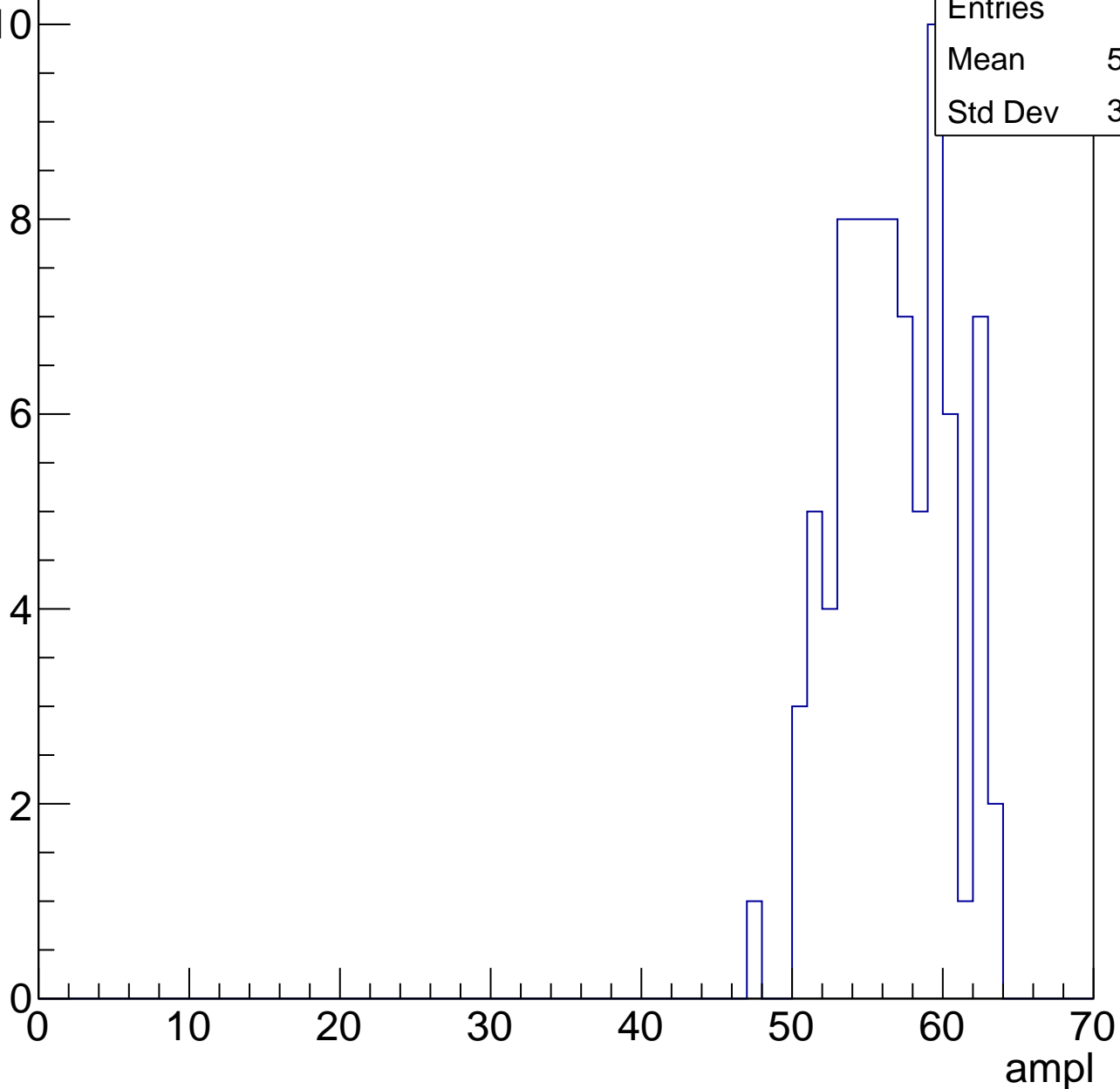


# B1L101S, U18-ch93, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	83
Mean	56.19
Std Dev	3.599

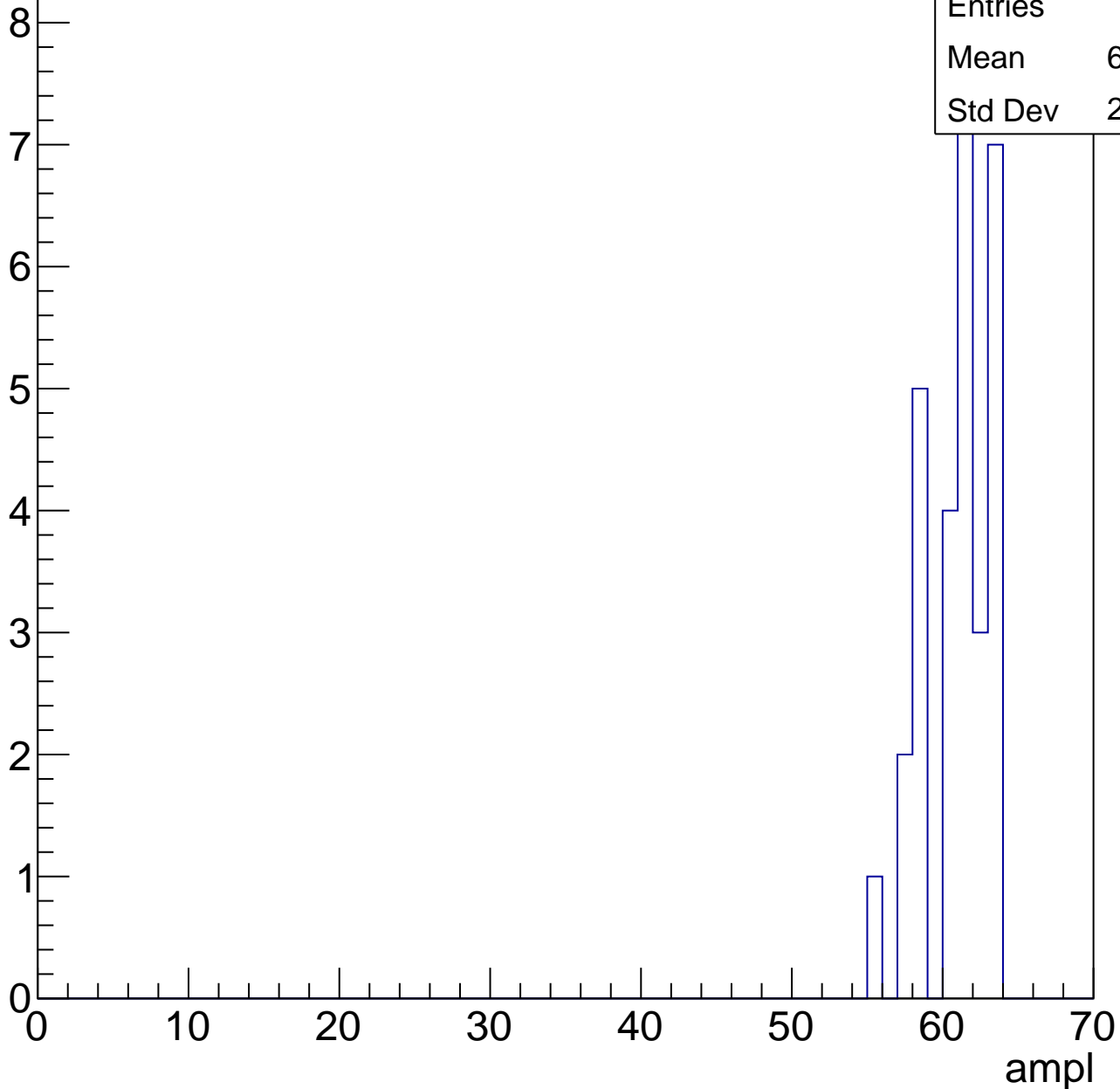


# B1L101S, U18-ch93, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

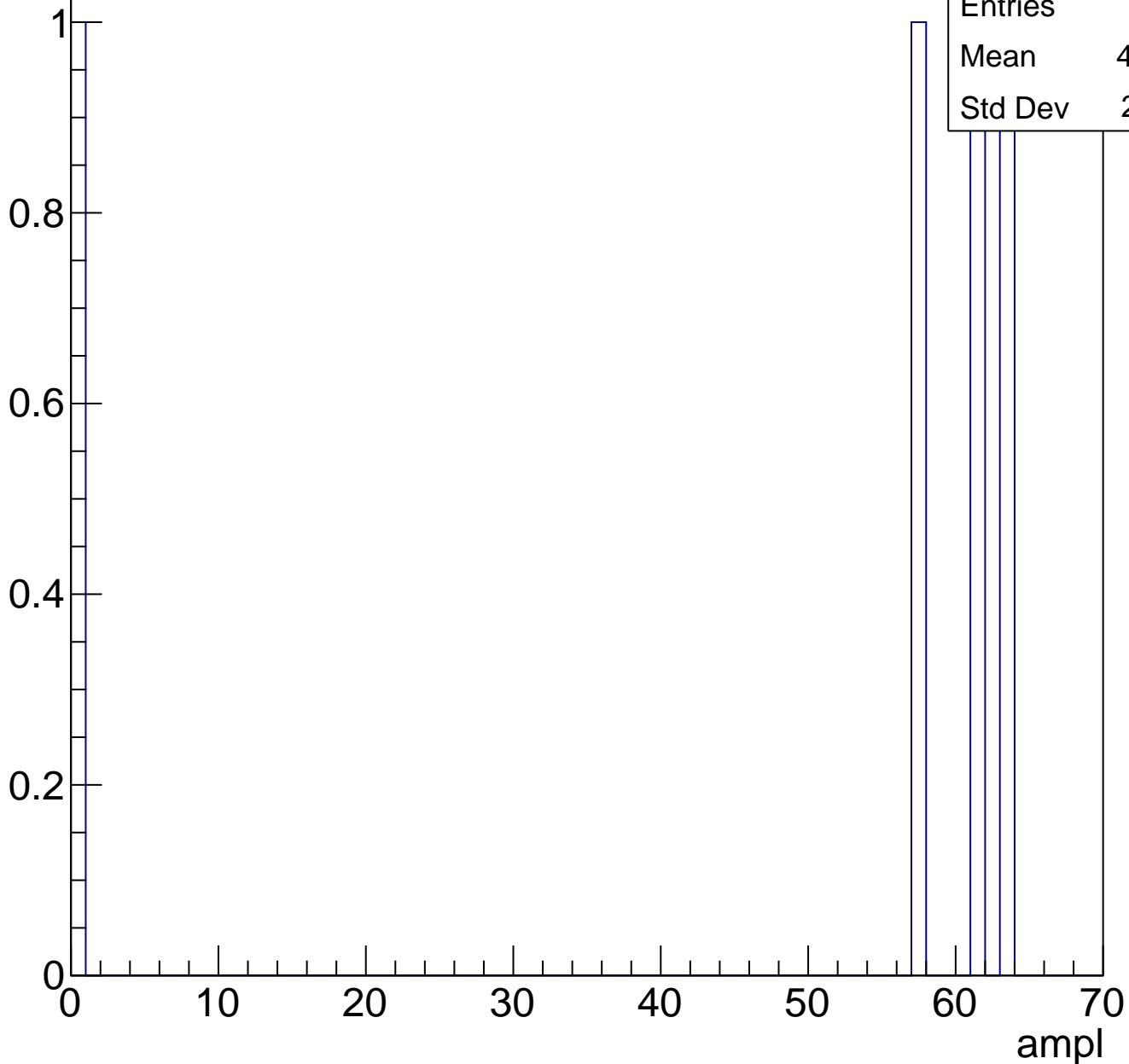
Entries	30
Mean	60.47
Std Dev	2.156



# B1L101S, U18-ch93, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch93, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U18-ch94, adc0

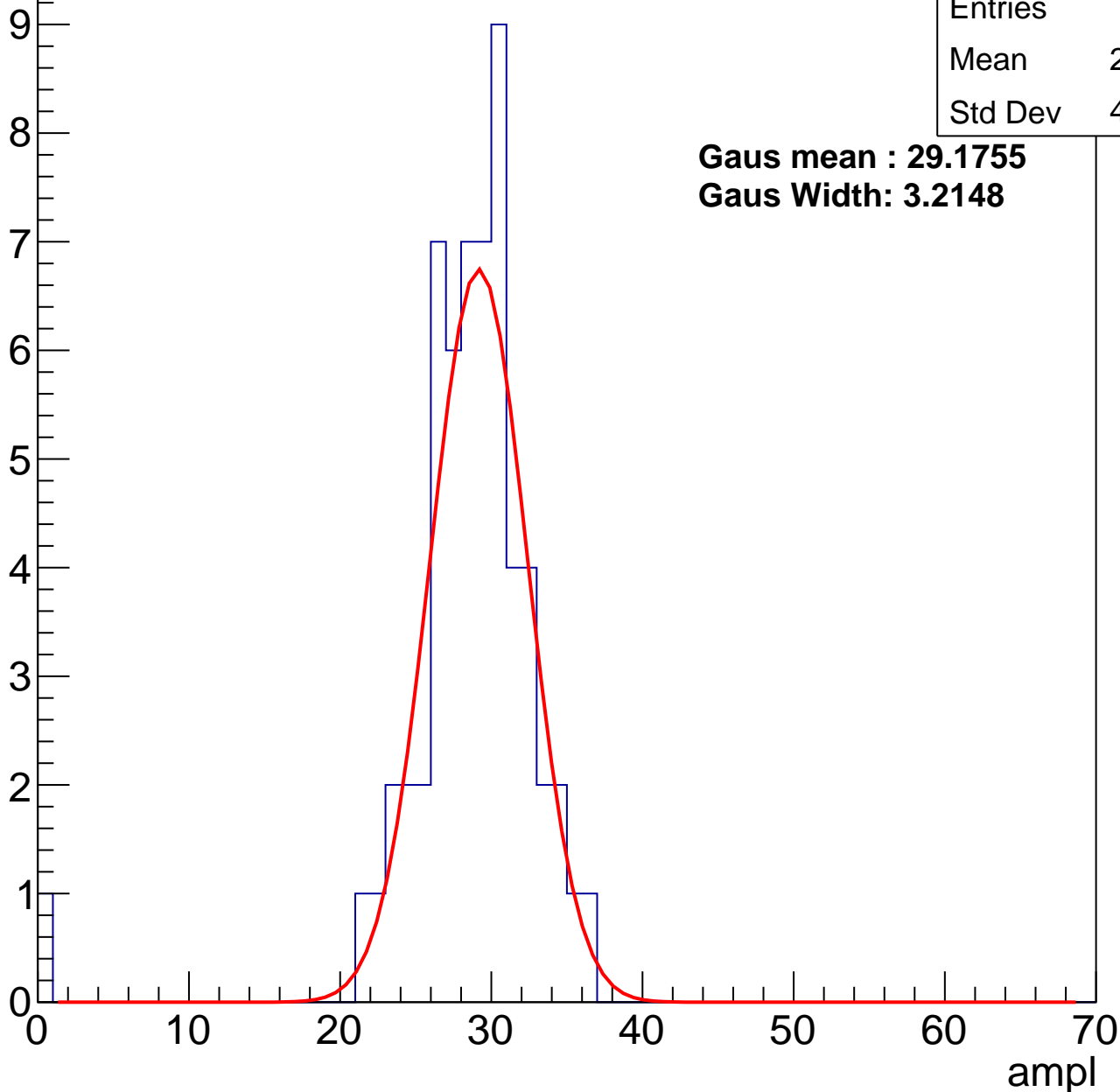
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	28.08
Std Dev	4.837

**Gaus mean : 29.1755**

**Gaus Width: 3.2148**



# B1L101S, U18-ch94, adc1

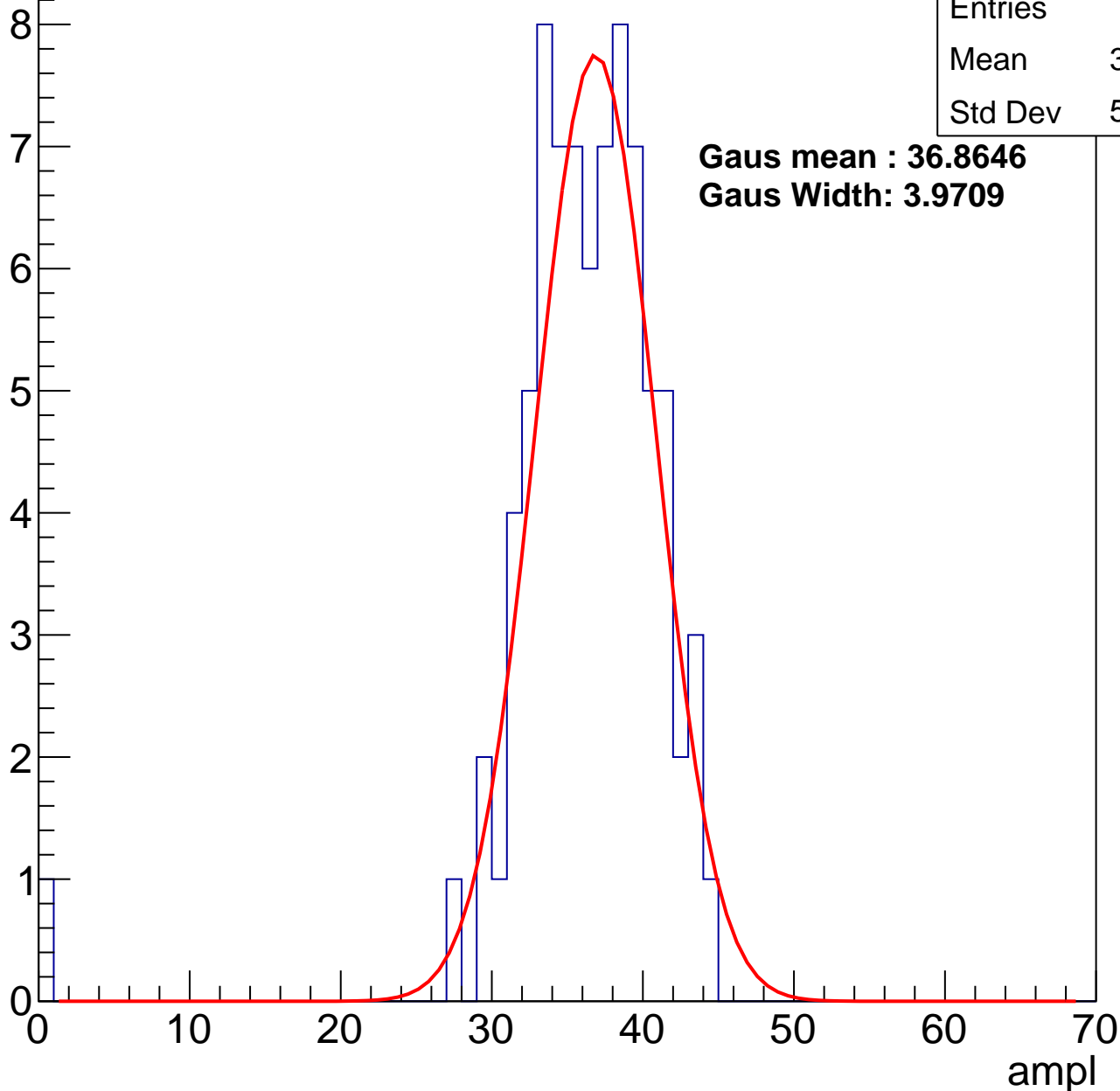
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	80
Mean	35.75
Std Dev	5.458

**Gaus mean : 36.8646**

**Gaus Width: 3.9709**



# B1L101S, U18-ch94, adc2

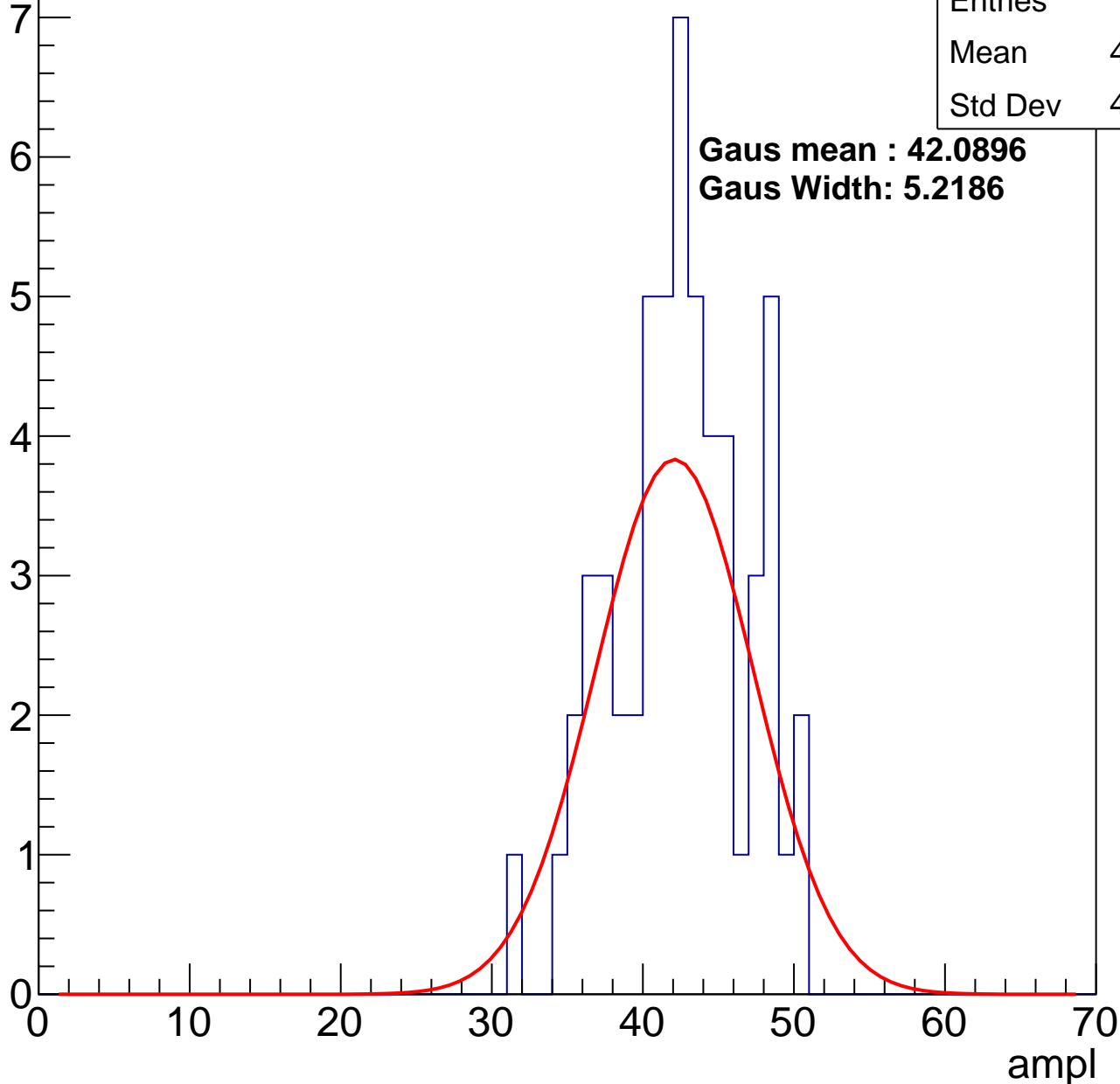
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	42.04
Std Dev	4.322

**Gaus mean : 42.0896**

**Gaus Width: 5.2186**



# B1L101S, U18-ch94, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	73
Mean	49.16
Std Dev	4.181

Entry

10

8

6

4

2

0

0

10

20

30

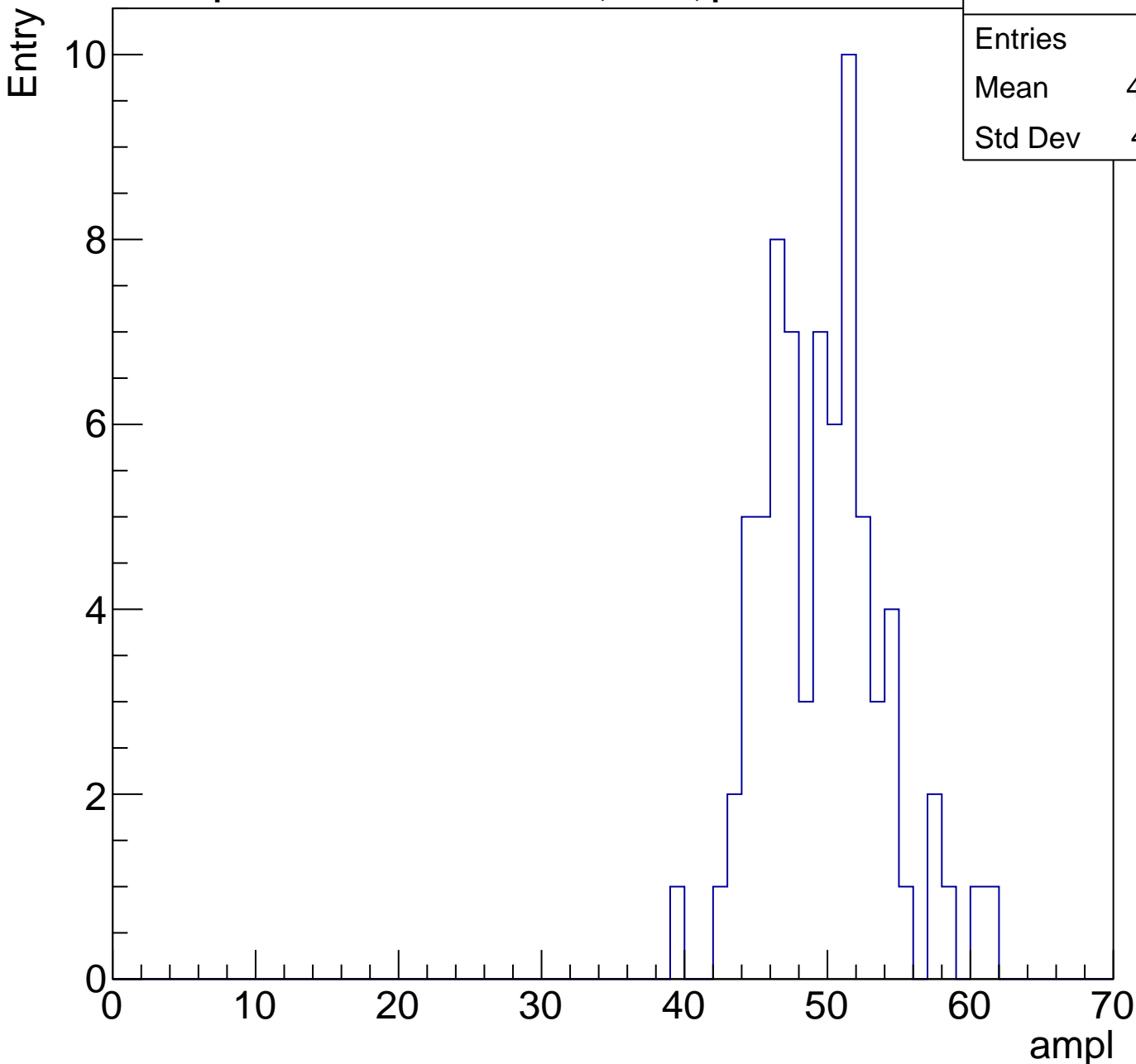
40

50

60

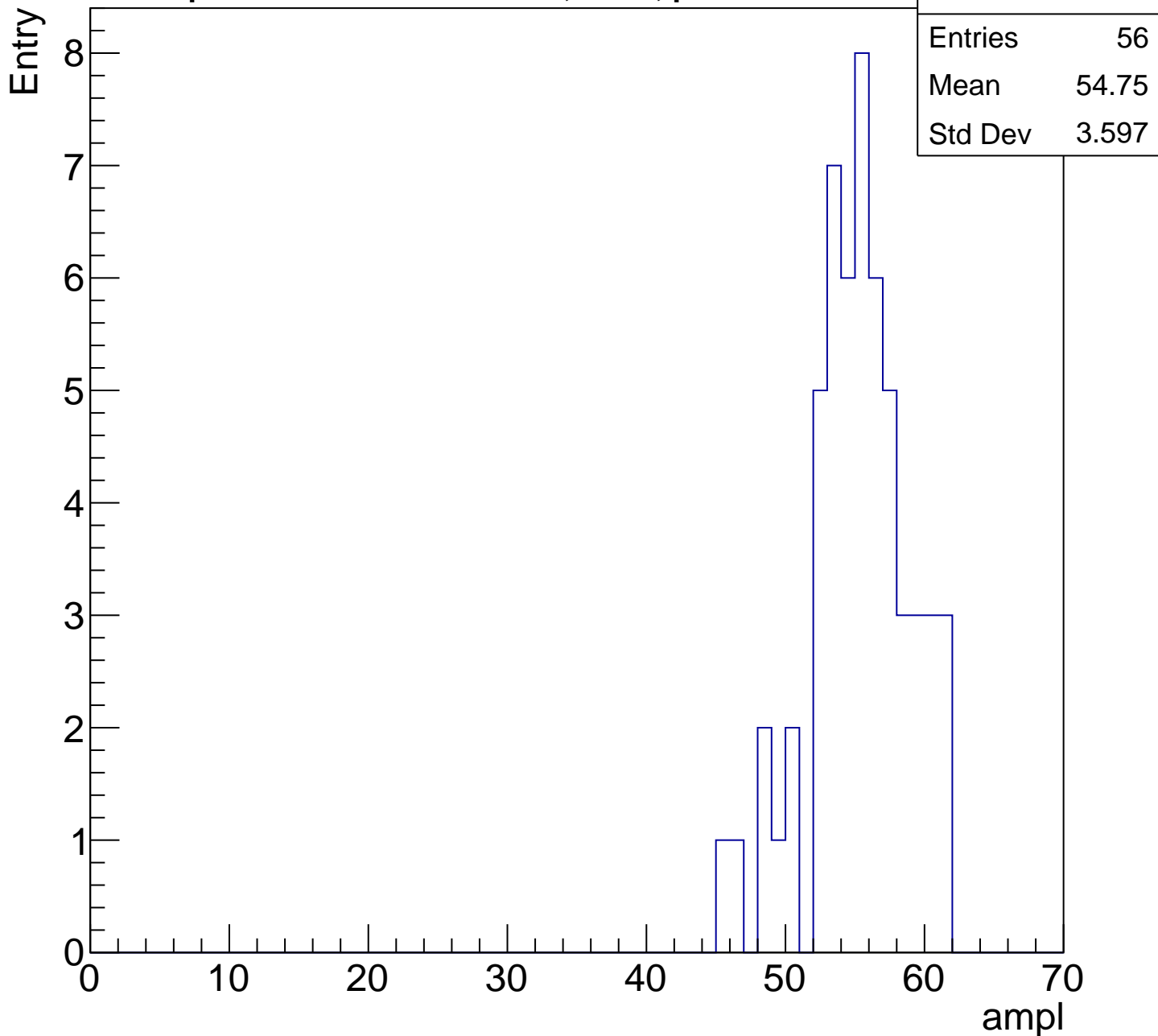
ampl

70



# B1L101S, U18-ch94, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

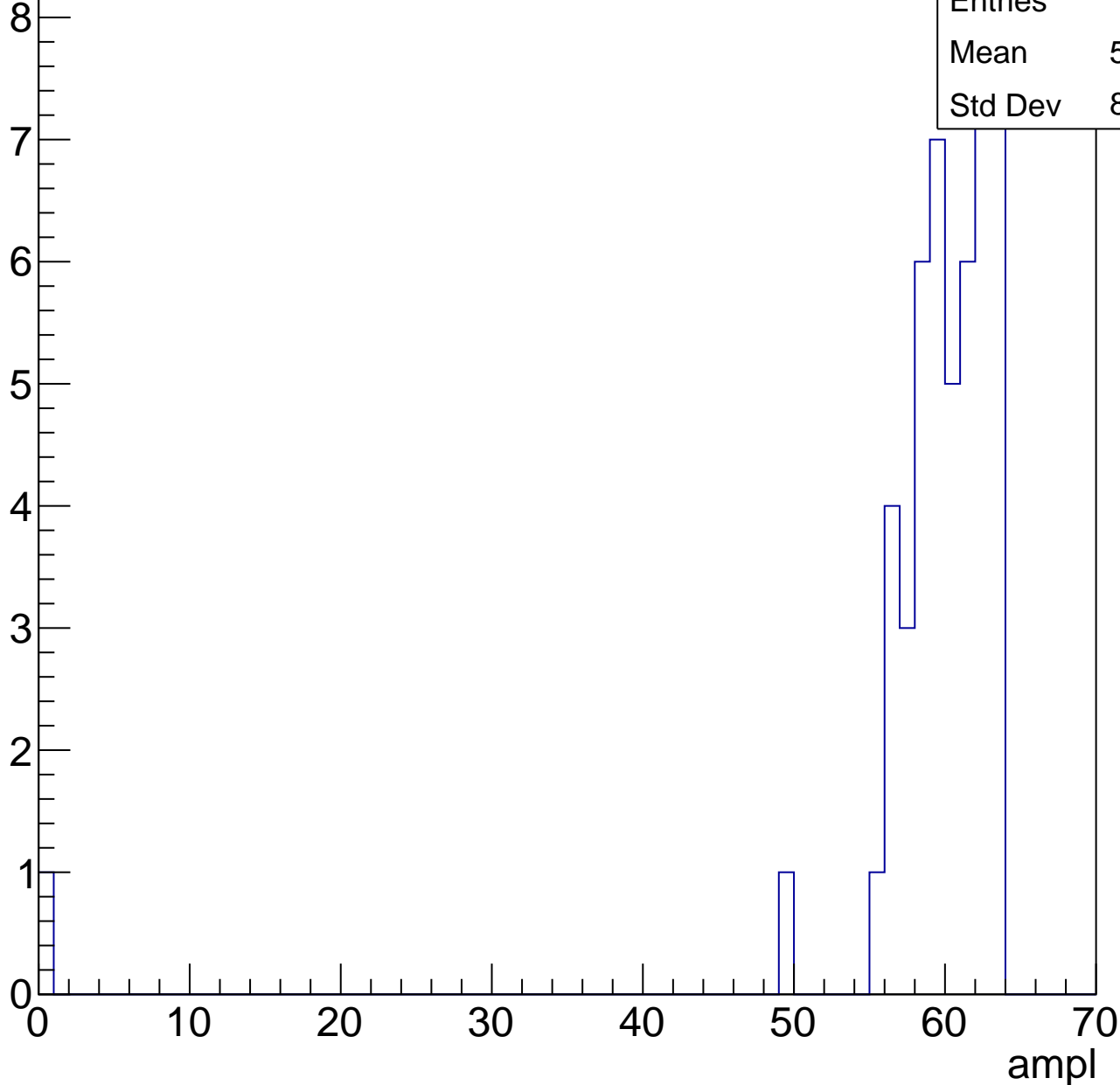


# B1L101S, U18-ch94, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	58.52
Std Dev	8.796



# B1L101S, U18-ch94, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

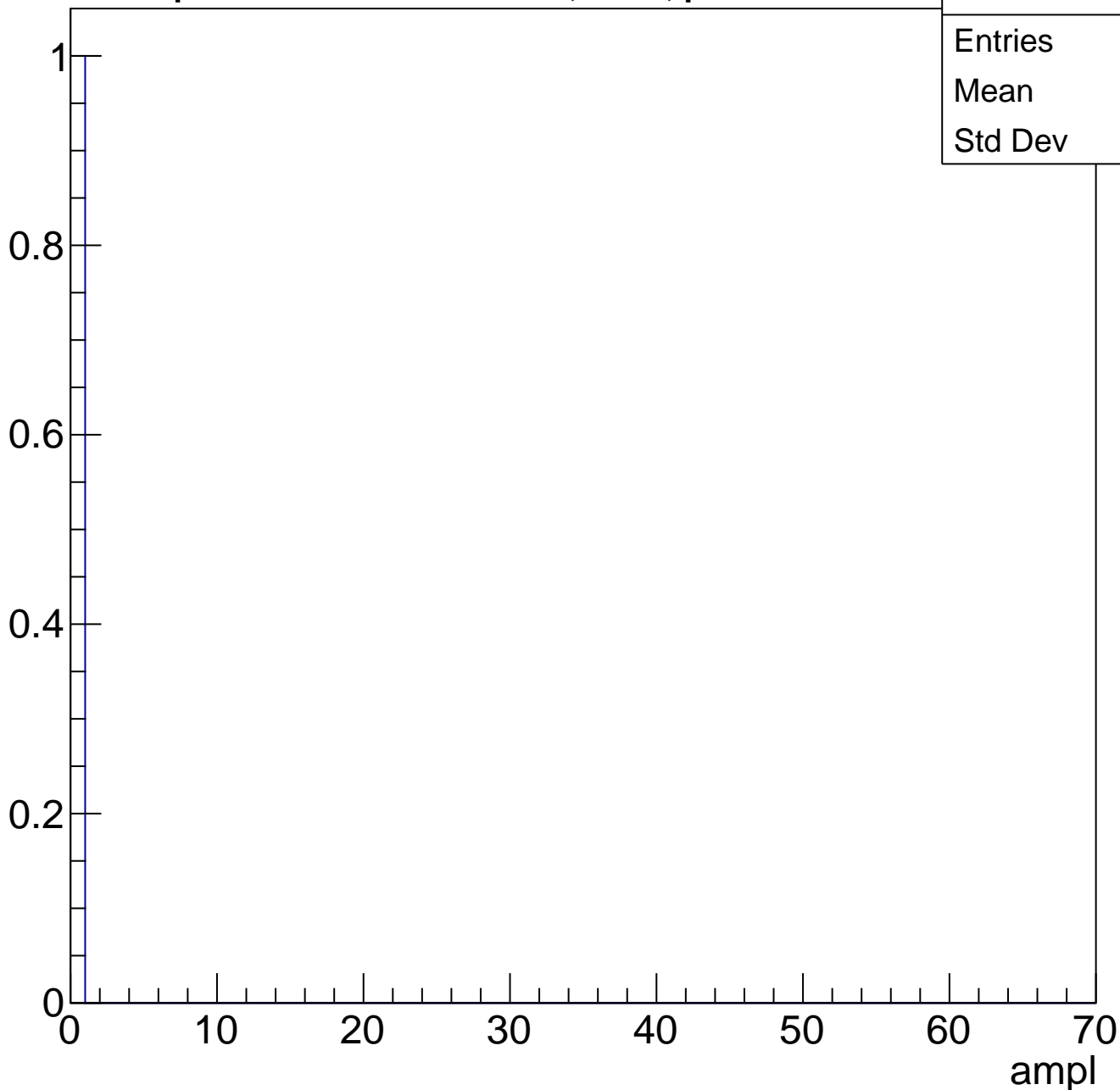




# B1L101S, U18-ch94, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U18-ch95, adc0

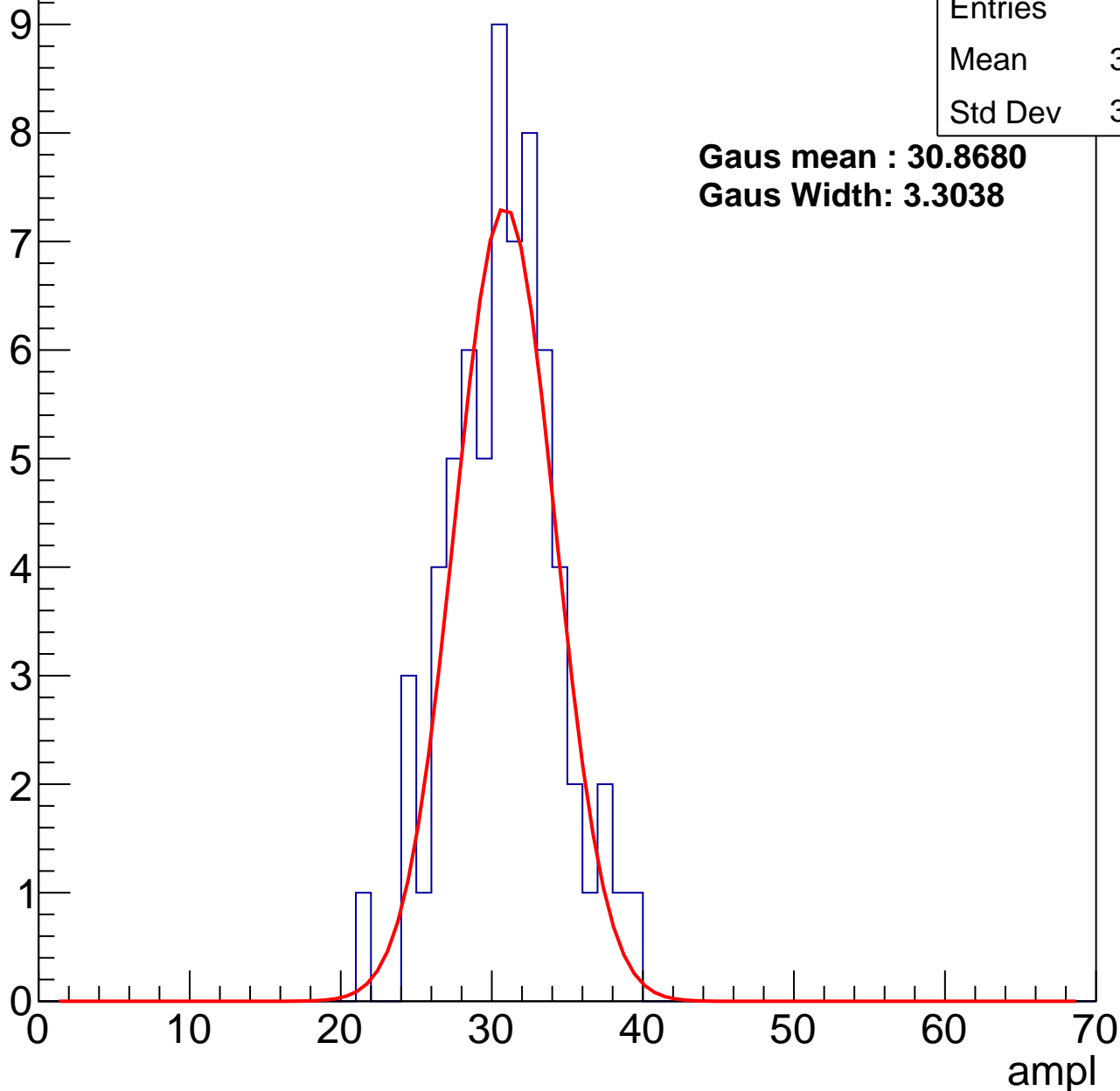
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	30.36
Std Dev	3.545

**Gaus mean : 30.8680**

**Gaus Width: 3.3038**



# B1L101S, U18-ch95, adc1

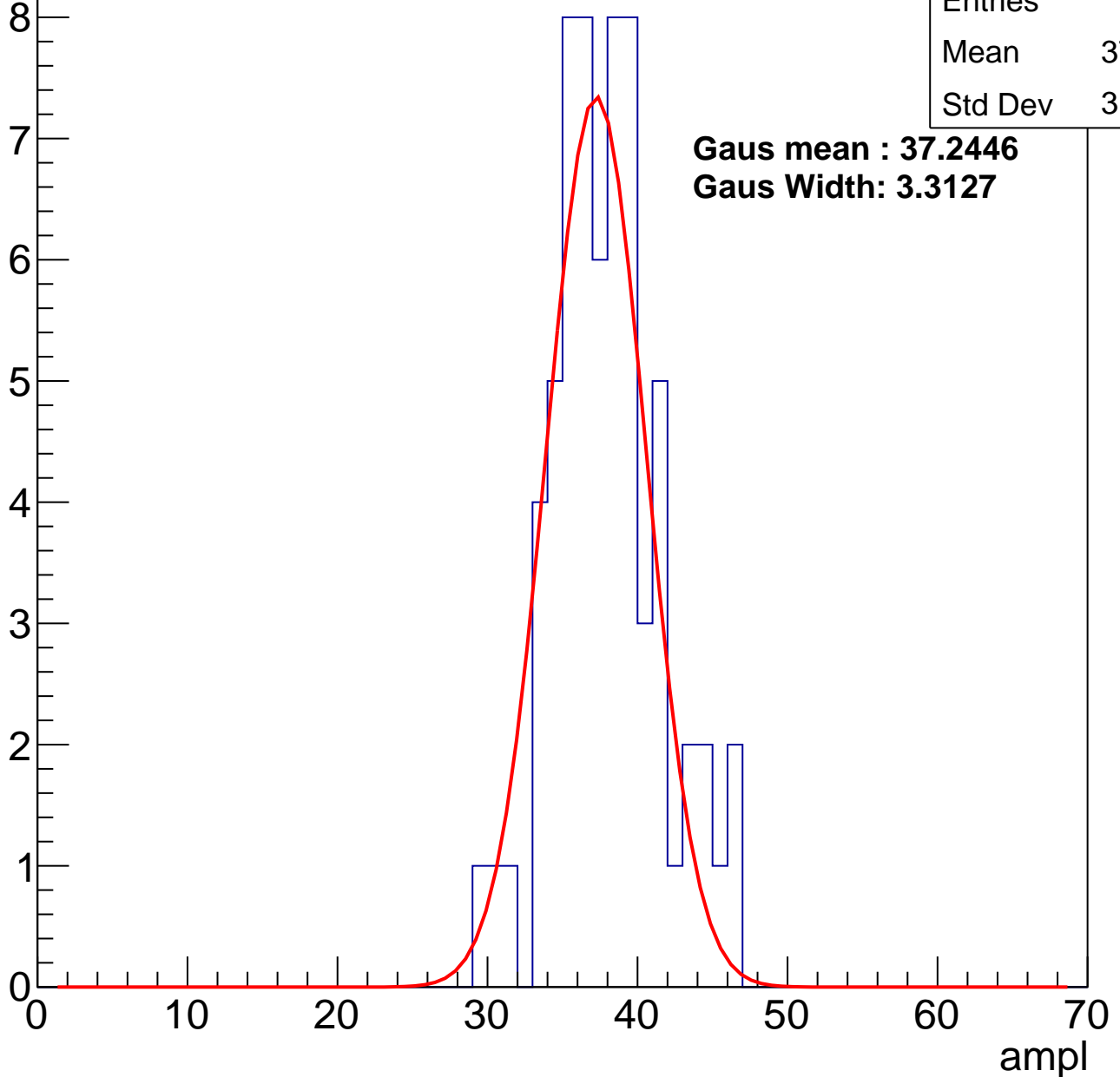
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	37.52
Std Dev	3.586

**Gaus mean : 37.2446**

**Gaus Width: 3.3127**



# B1L101S, U18-ch95, adc2

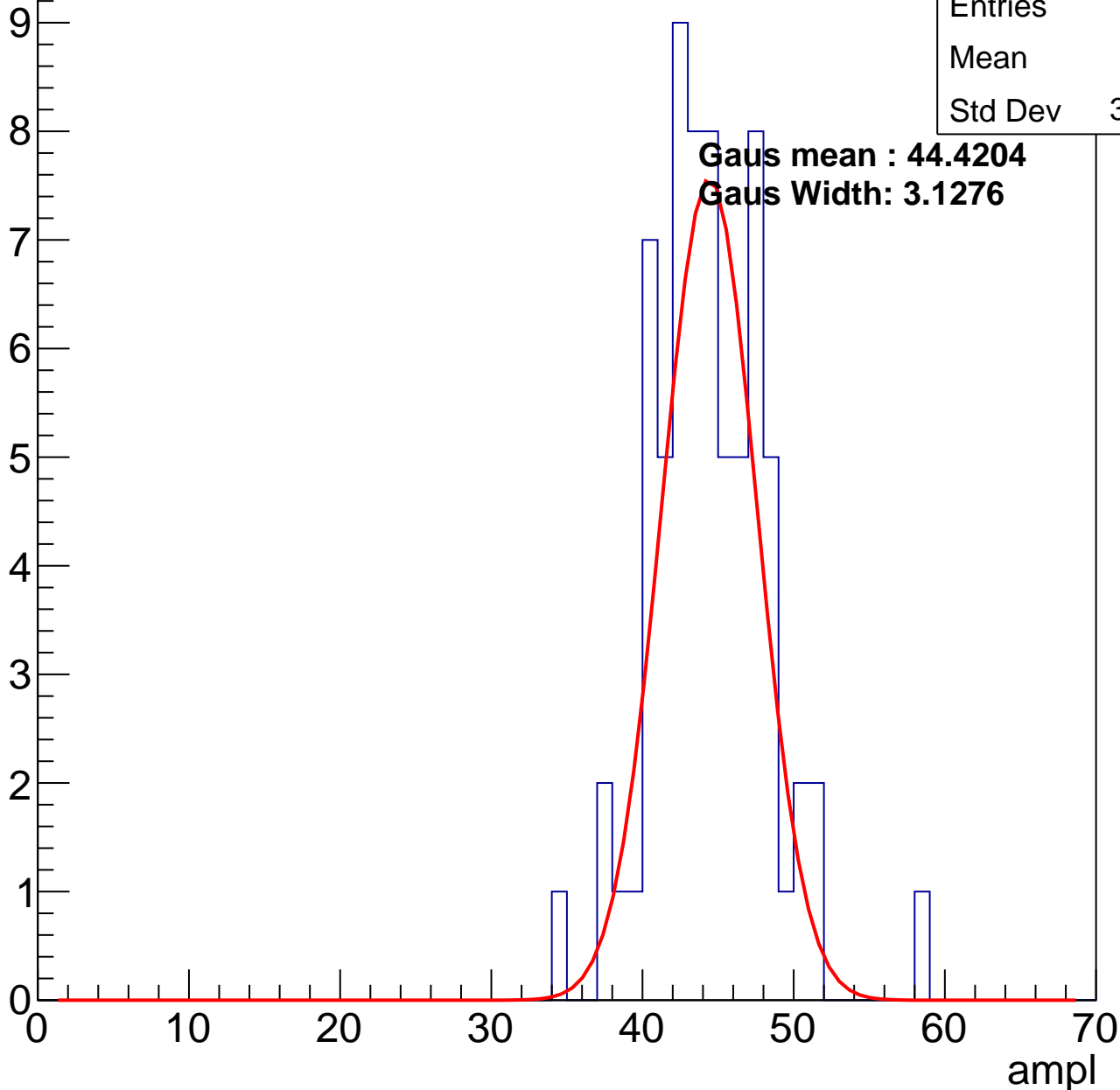
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	44
Std Dev	3.805

**Gaus mean : 44.4204**

**Gaus Width: 3.1276**

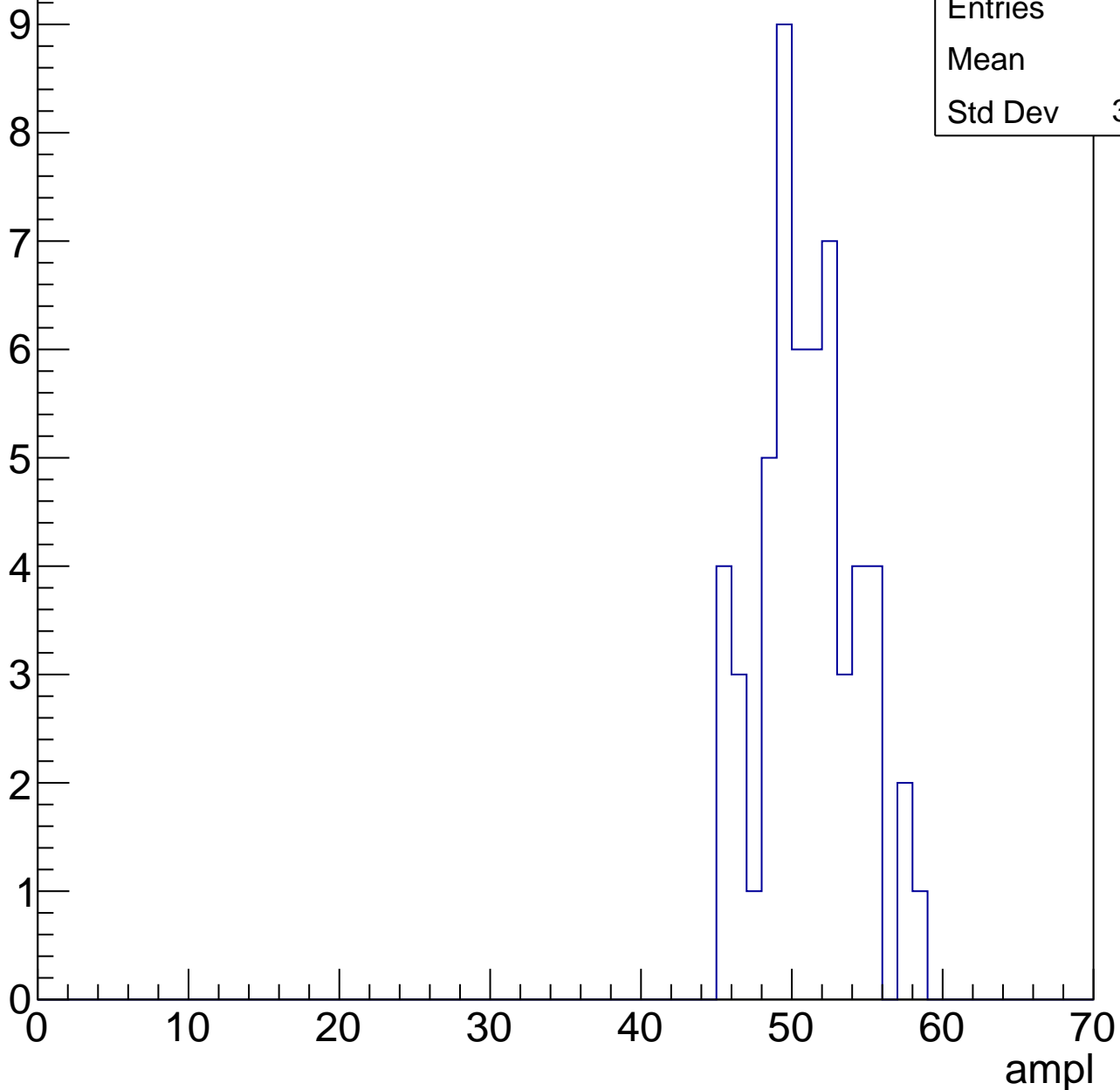


# B1L101S, U18-ch95, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	50.6
Std Dev	3.171

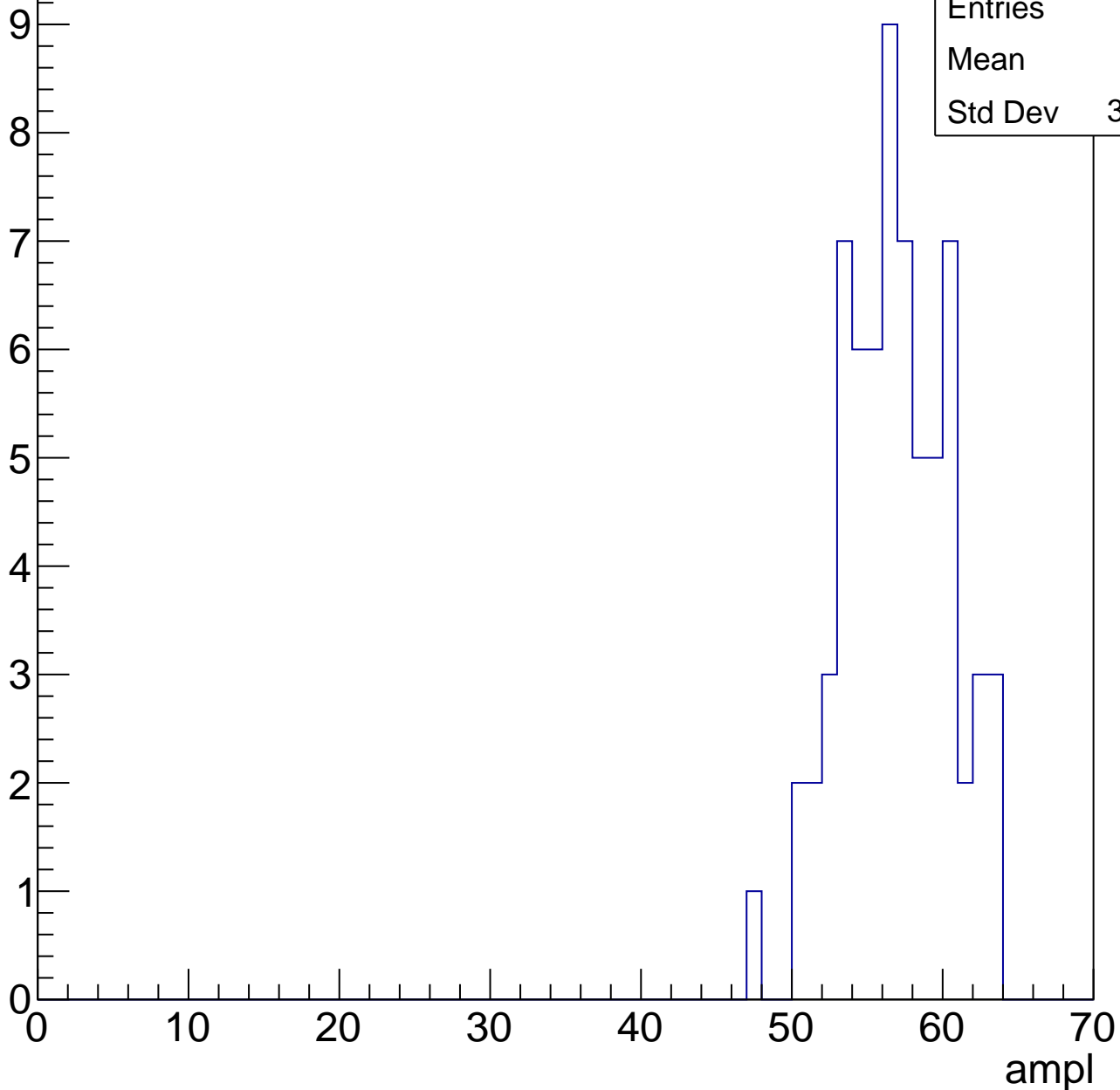


# B1L101S, U18-ch95, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	56.4
Std Dev	3.477

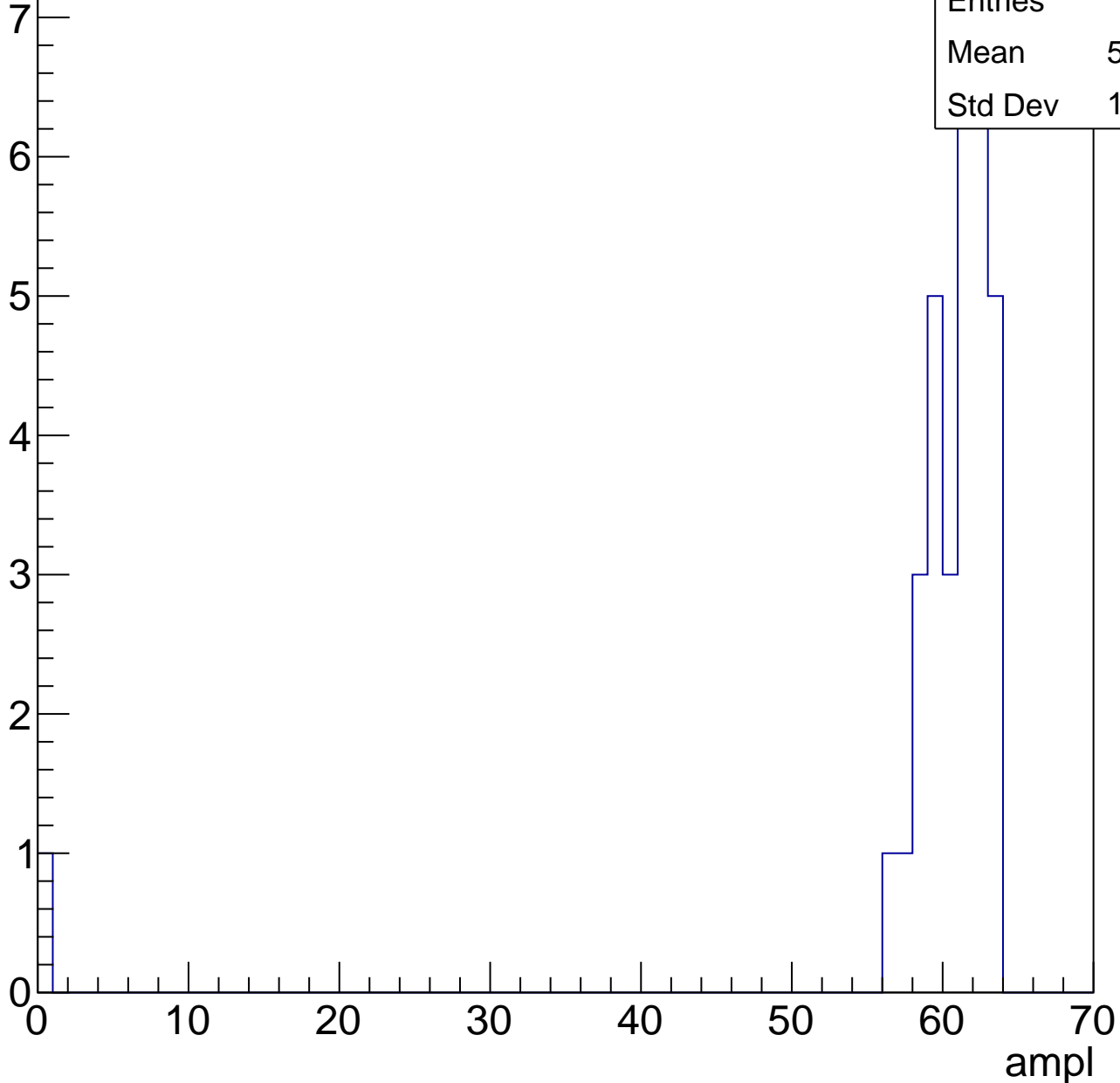


# B1L101S, U18-ch95, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	33
Mean	58.73
Std Dev	10.54



# B1L101S, U18-ch95, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch95, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch96, adc0

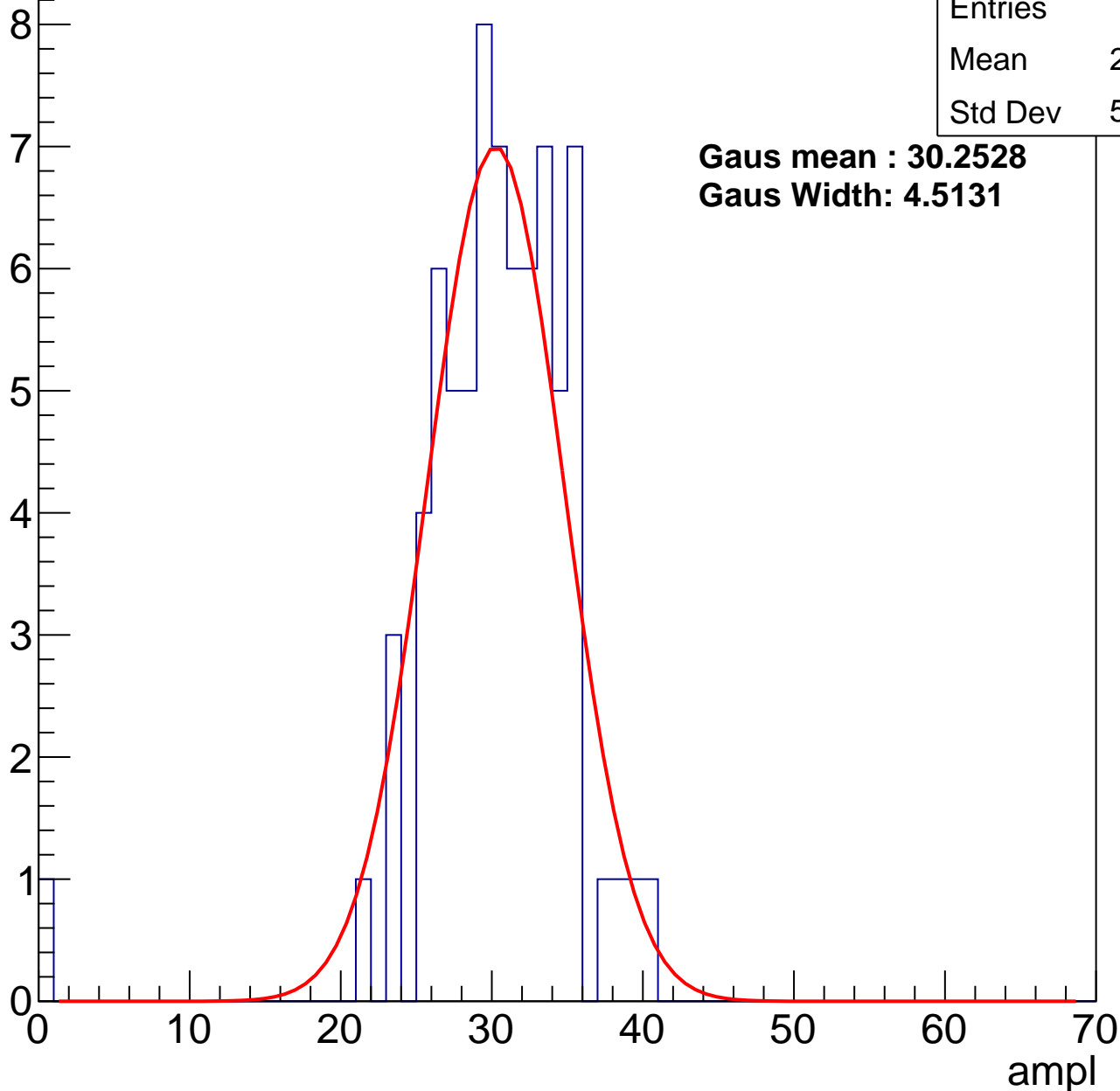
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	29.88
Std Dev	5.213

**Gaus mean : 30.2528**

**Gaus Width: 4.5131**



# B1L101S, U18-ch96, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	68
Mean	37
Std Dev	6.024

**Gaus mean : 37.6093**

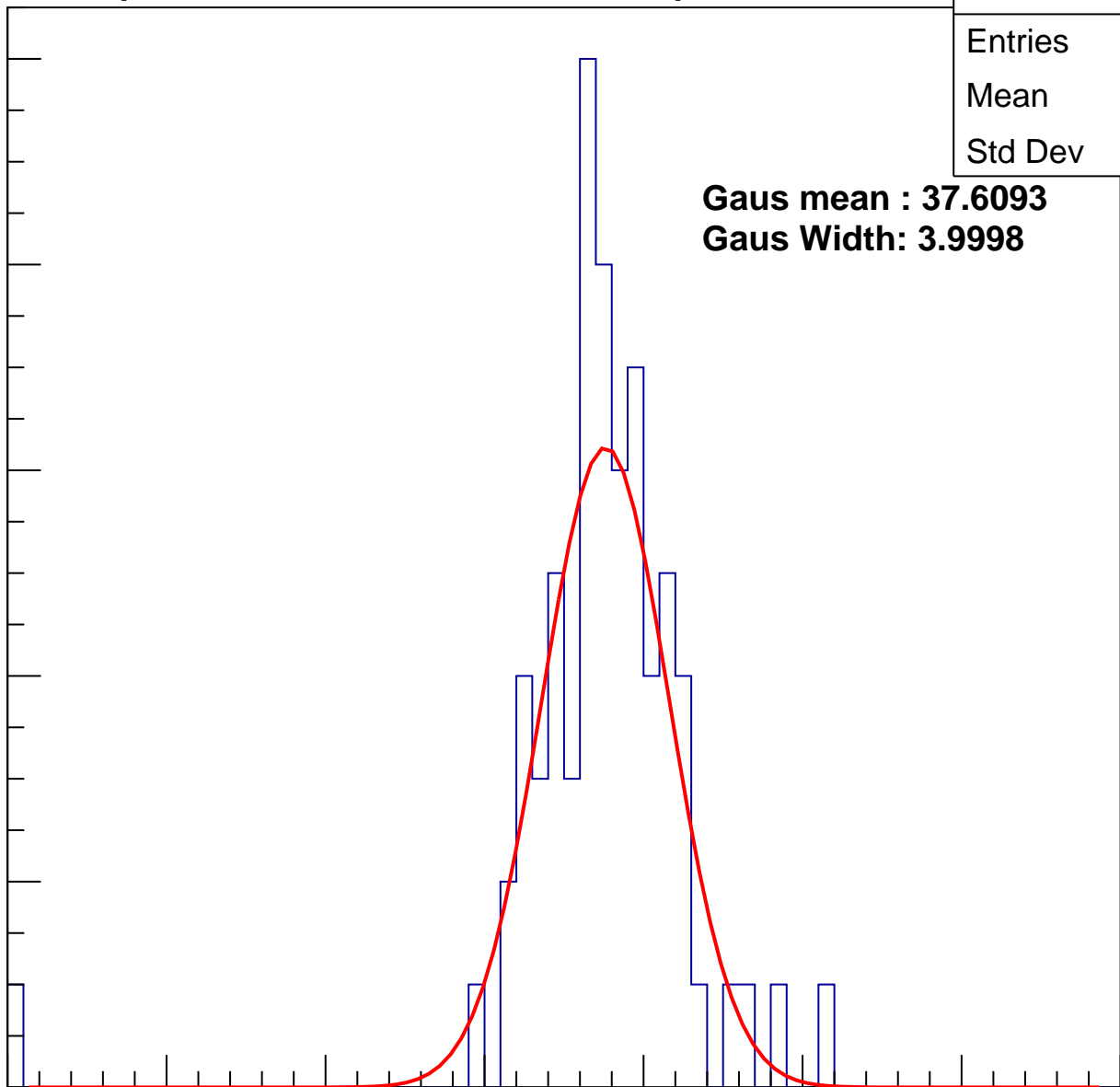
**Gaus Width: 3.9998**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U18-ch96, adc2

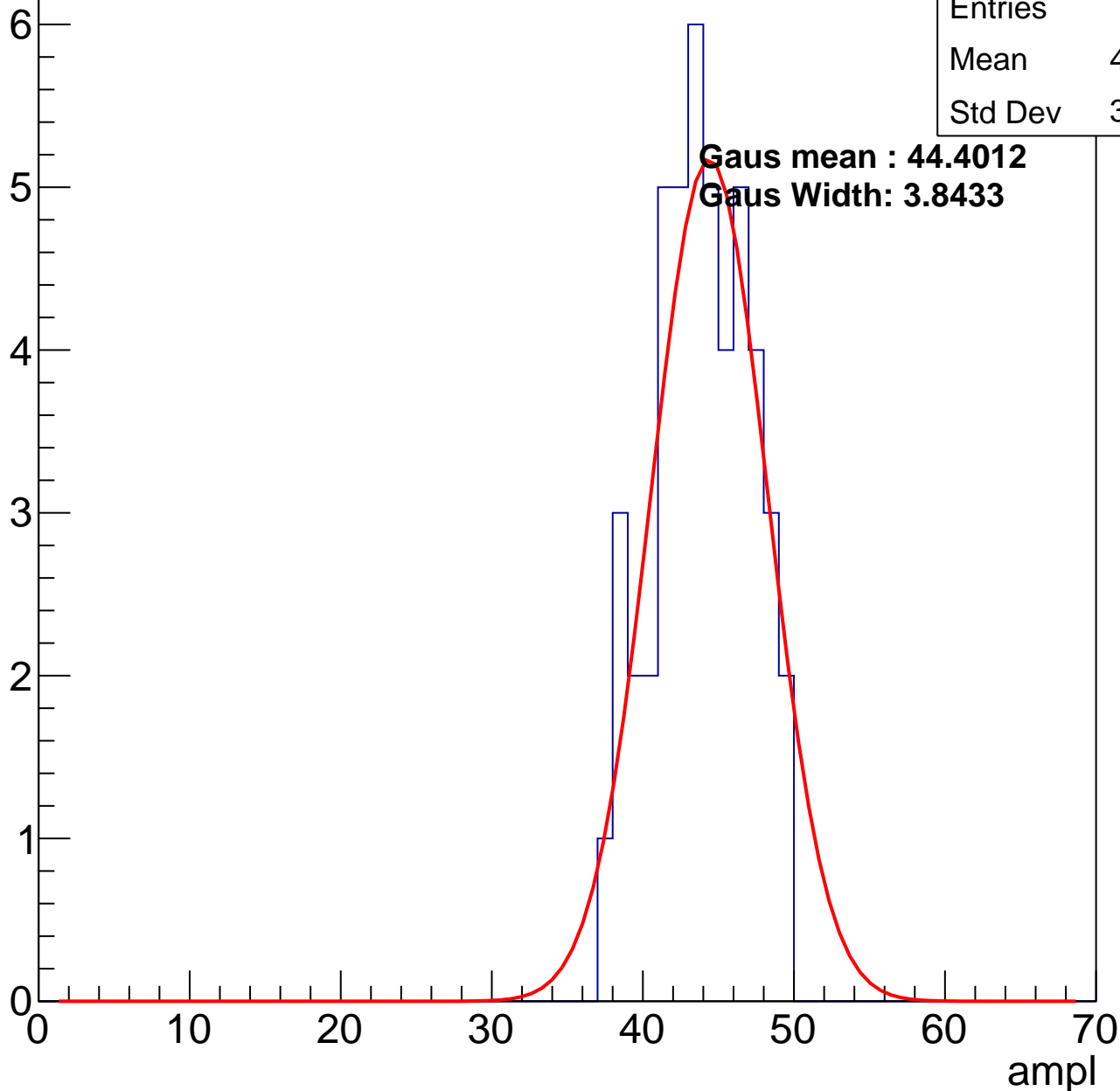
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	47
Mean	43.45
Std Dev	3.107

**Gaus mean : 44.4012**

**Gaus Width: 3.8433**

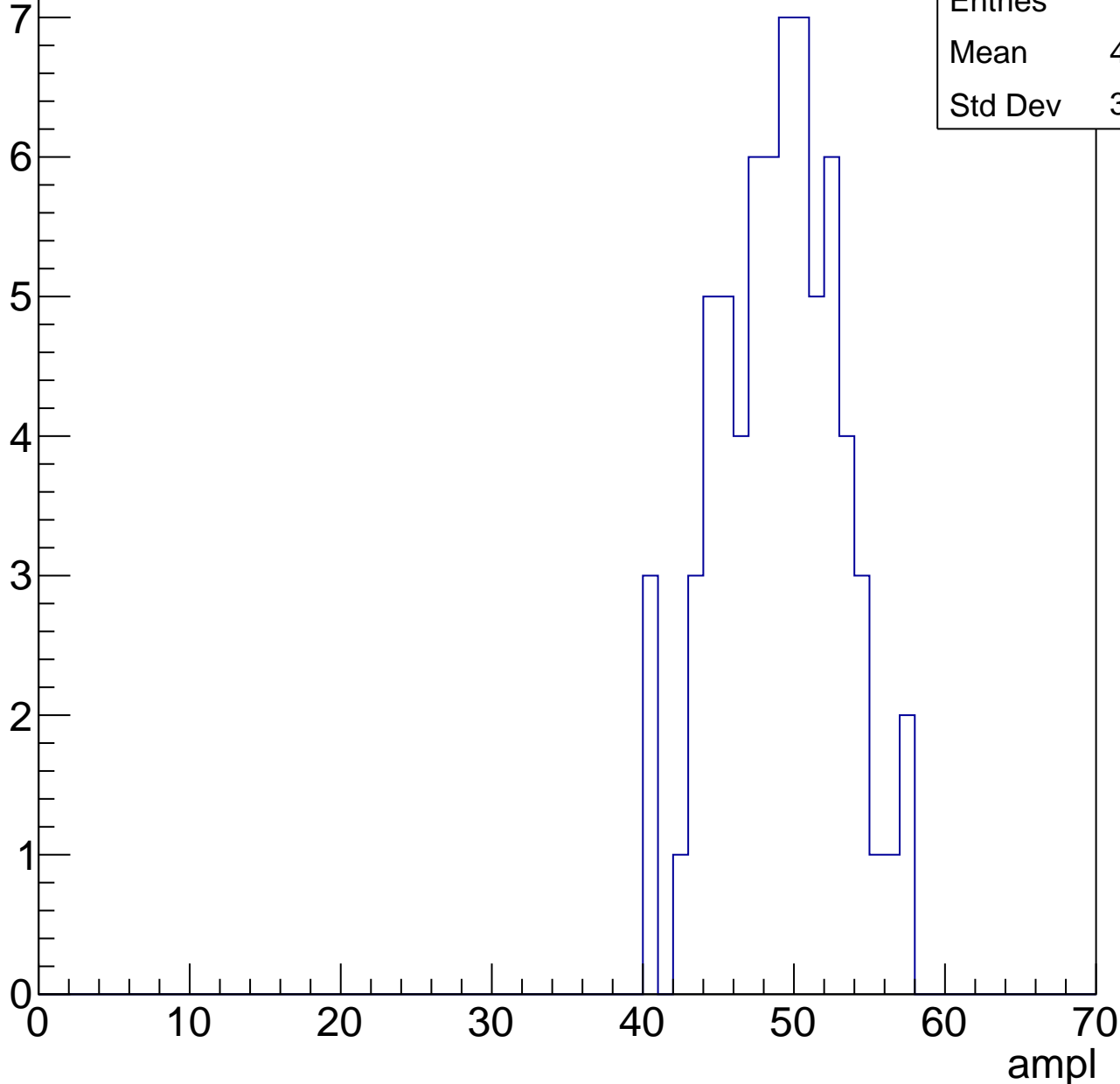


# B1L101S, U18-ch96, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

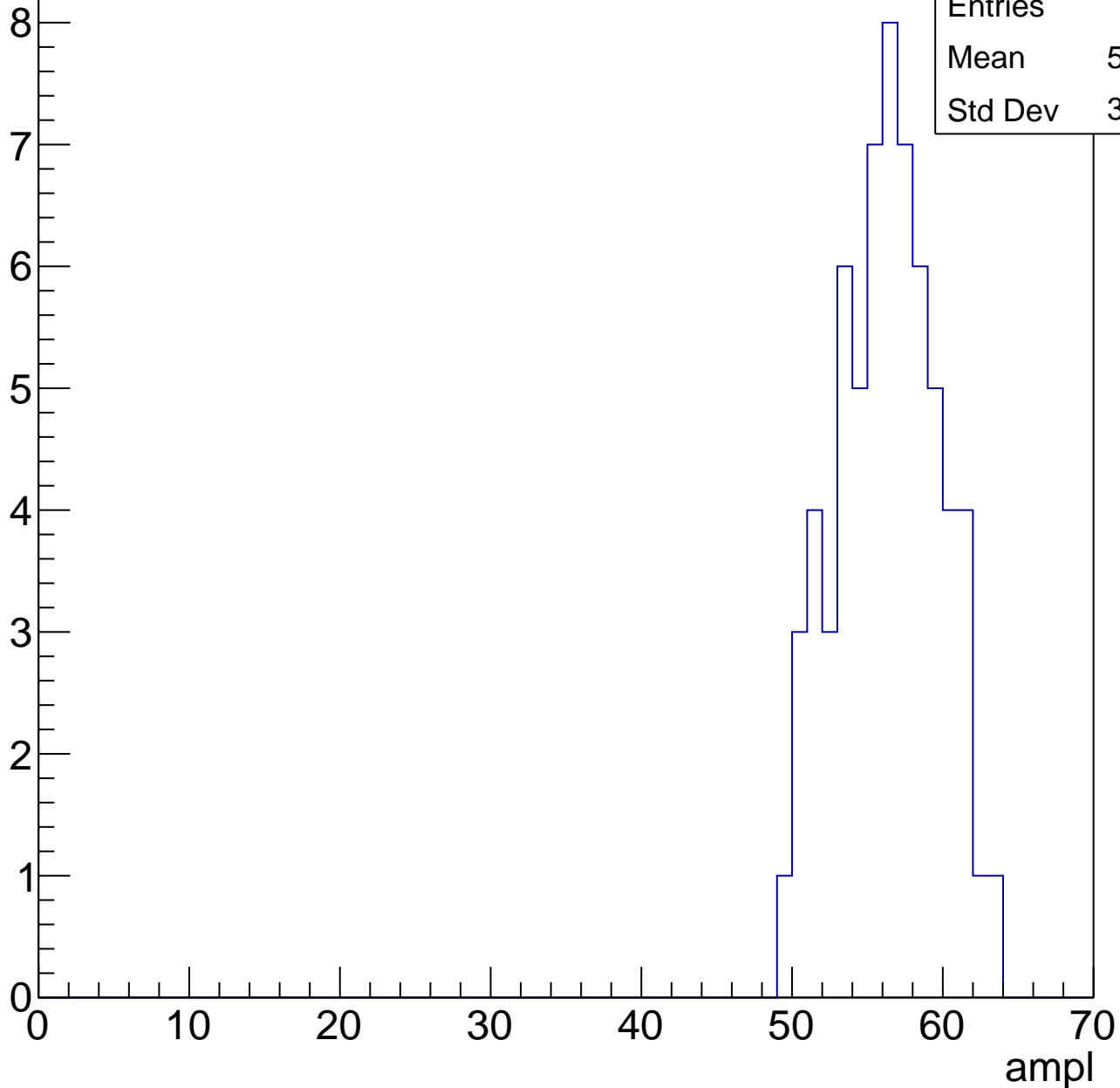
Entries	69
Mean	48.54
Std Dev	3.973



# B1L101S, U18-ch96, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

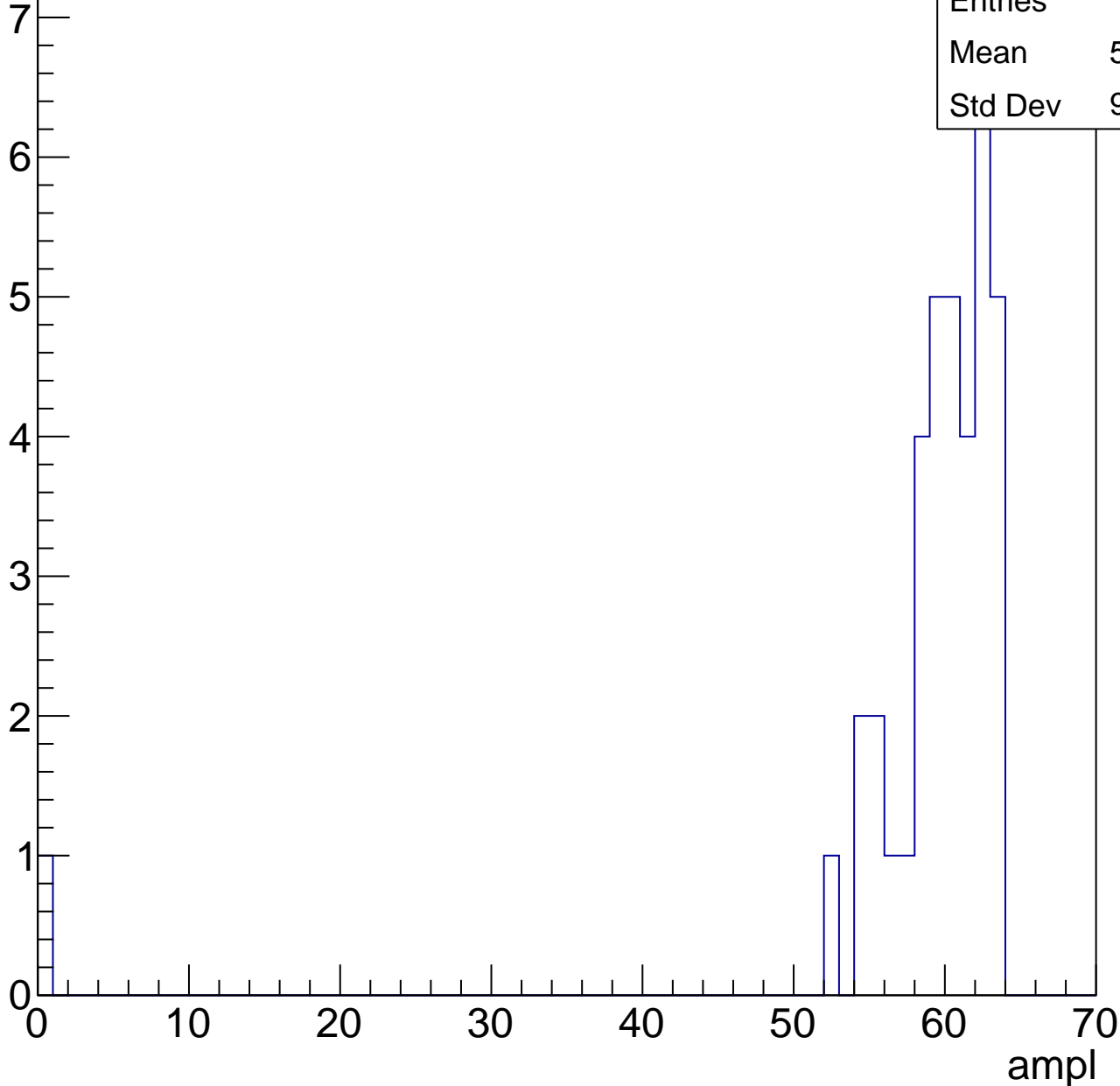


# B1L101S, U18-ch96, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	38
Mean	57.97
Std Dev	9.938



# B1L101S, U18-ch96, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

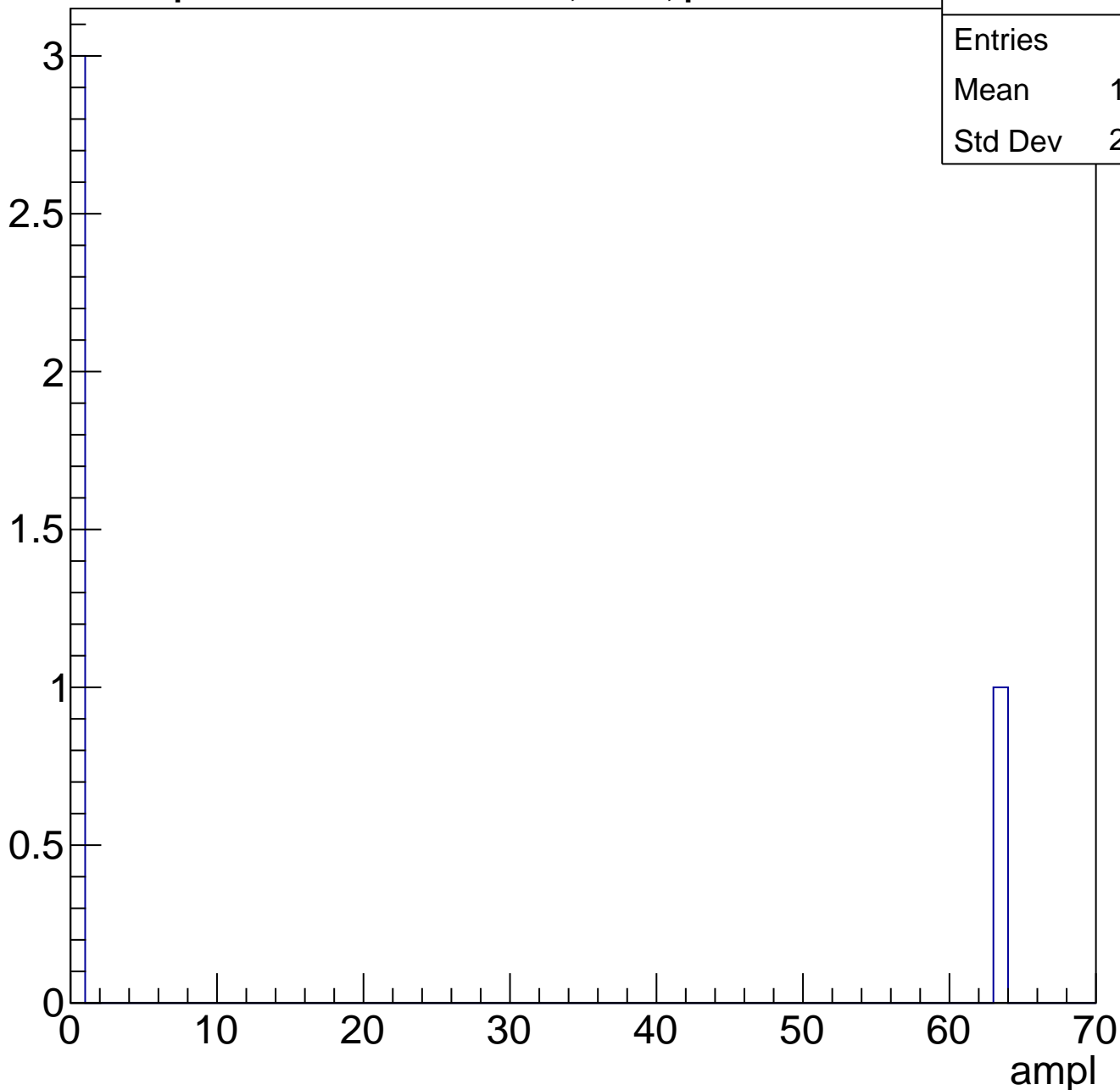




# B1L101S, U18-ch96, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	4
Mean	15.75
Std Dev	27.28

# B1L101S, U18-ch97, adc0

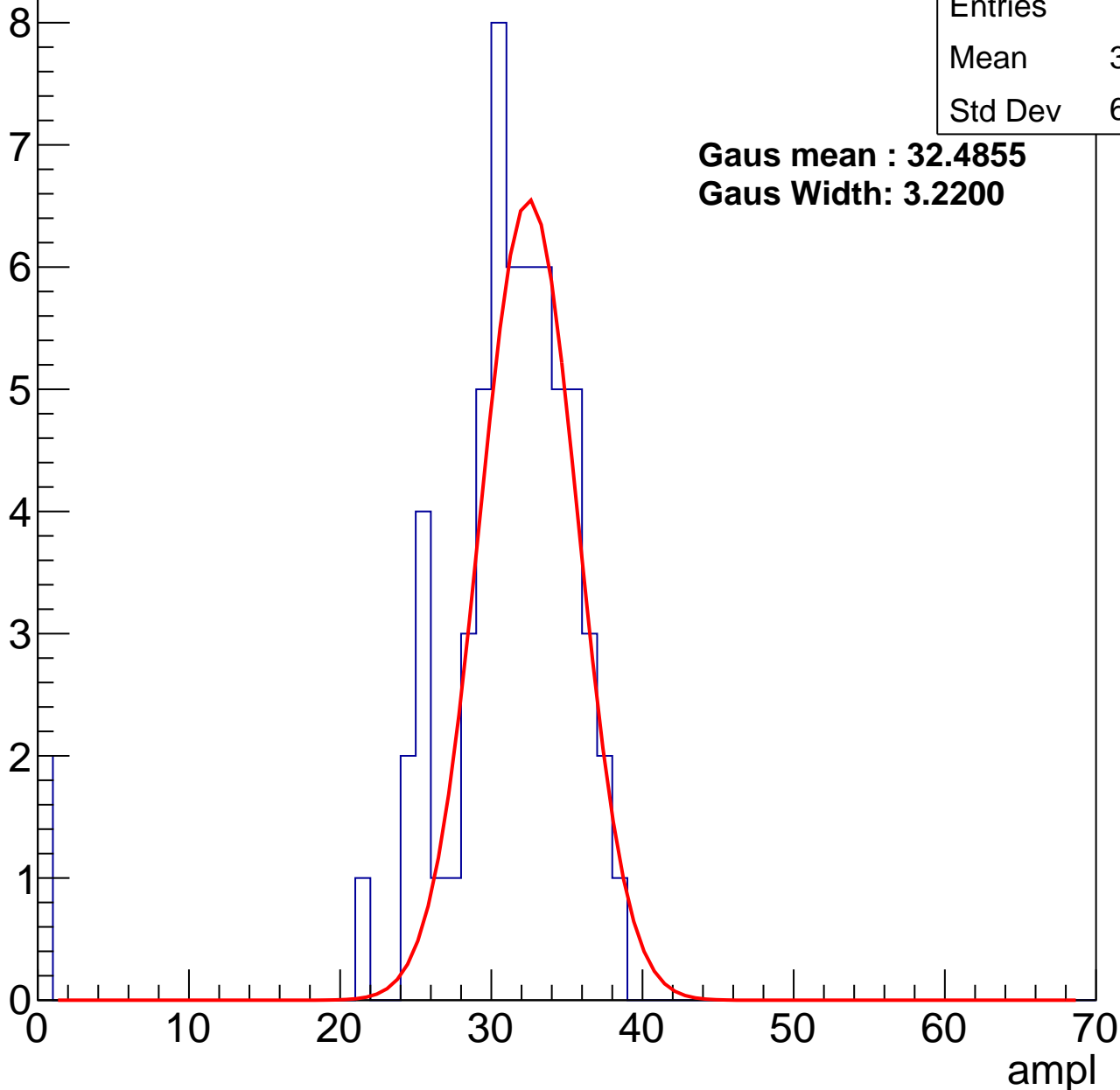
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	30.03
Std Dev	6.596

**Gaus mean : 32.4855**

**Gaus Width: 3.2200**



# B1L101S, U18-ch97, adc1

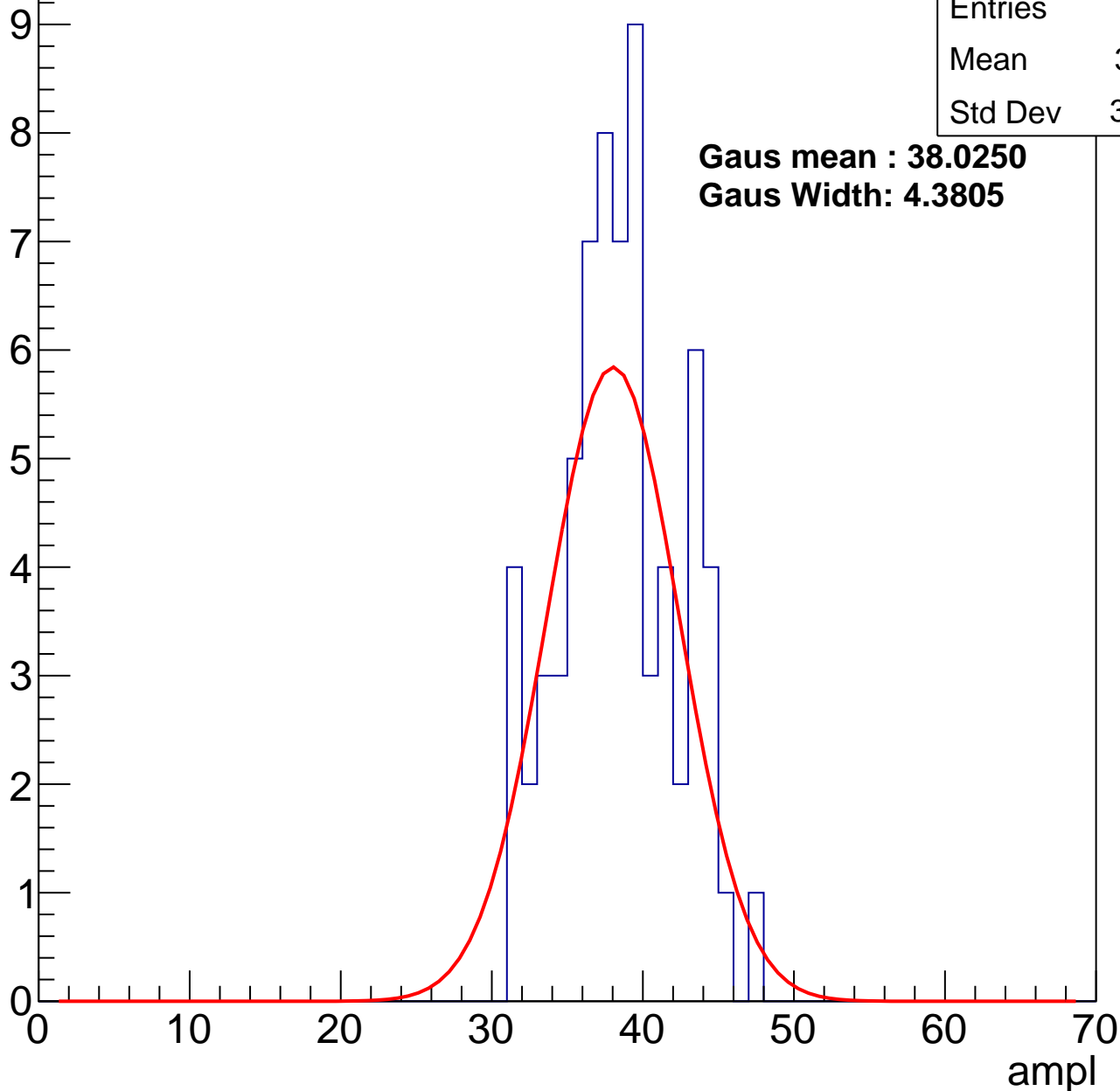
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	38.01
Std Dev	3.778

**Gaus mean : 38.0250**

**Gaus Width: 4.3805**



# B1L101S, U18-ch97, adc2

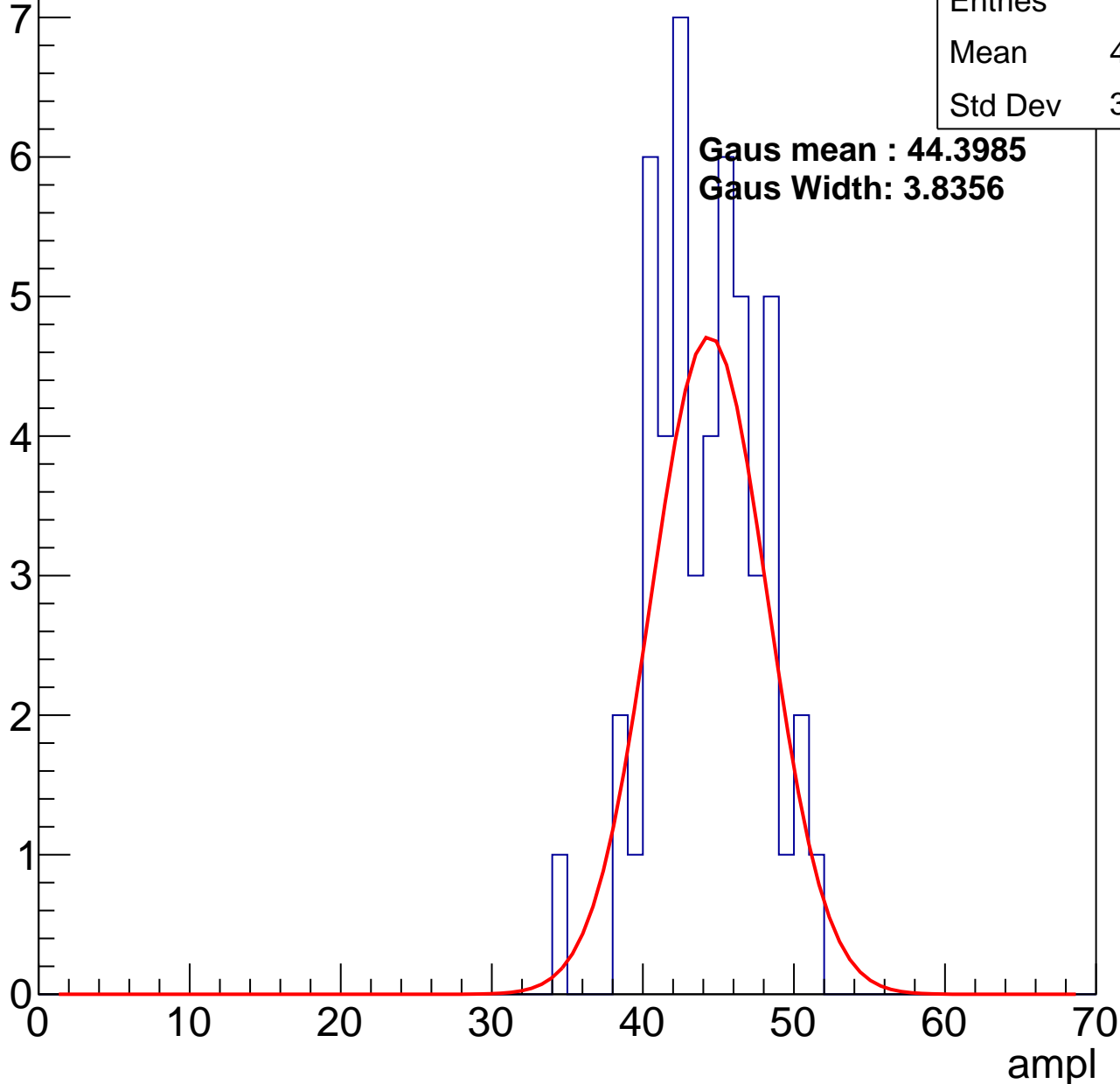
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	43.78
Std Dev	3.533

**Gaus mean : 44.3985**

**Gaus Width: 3.8356**

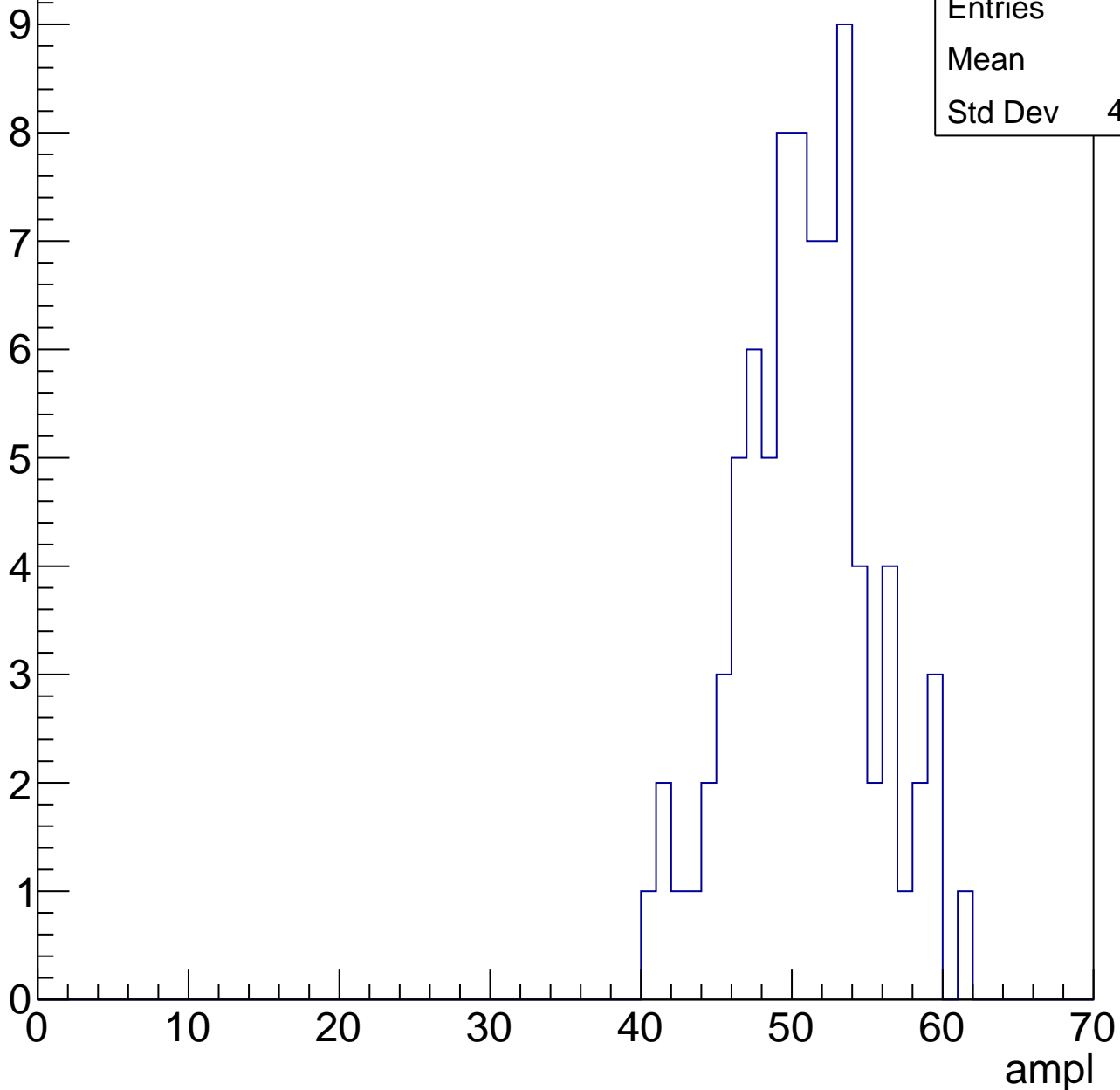


# B1L101S, U18-ch97, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	82
Mean	50.4
Std Dev	4.398

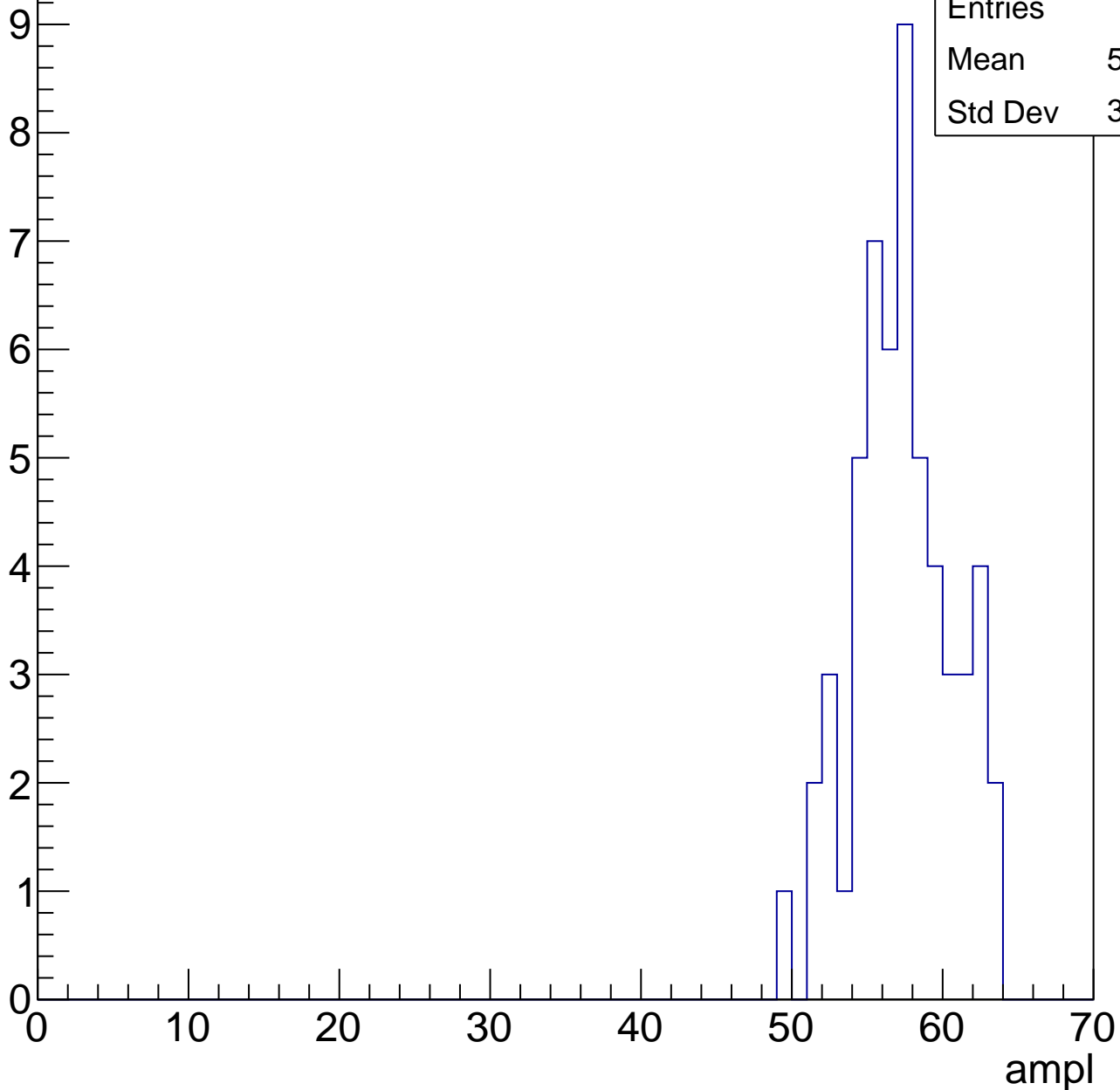


# B1L101S, U18-ch97, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	56.85
Std Dev	3.227

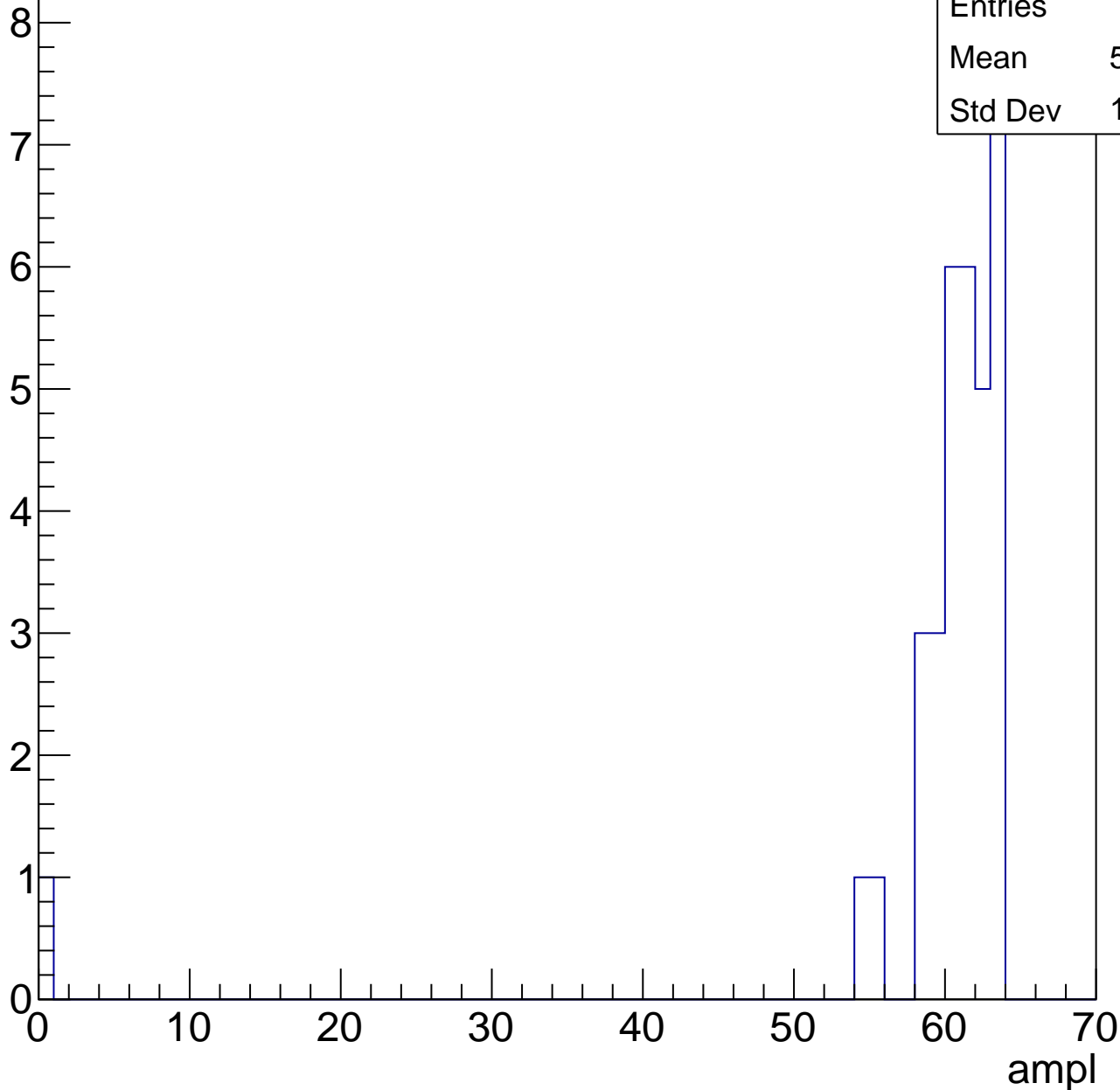


# B1L101S, U18-ch97, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	34
Mean	58.82
Std Dev	10.47



# B1L101S, U18-ch97, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch97, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch98, adc0

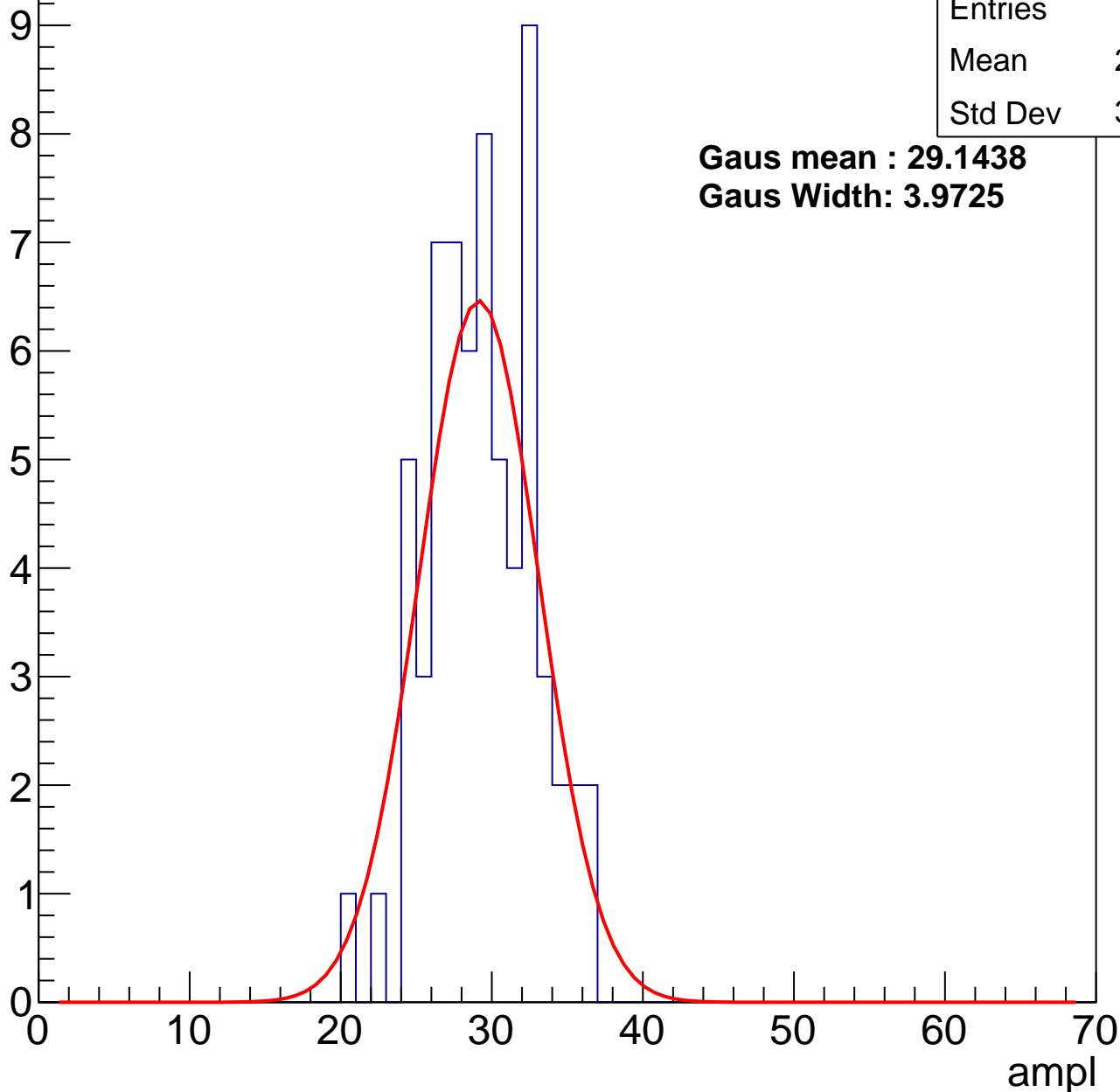
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	28.91
Std Dev	3.441

**Gaus mean : 29.1438**

**Gaus Width: 3.9725**



# B1L101S, U18-ch98, adc1

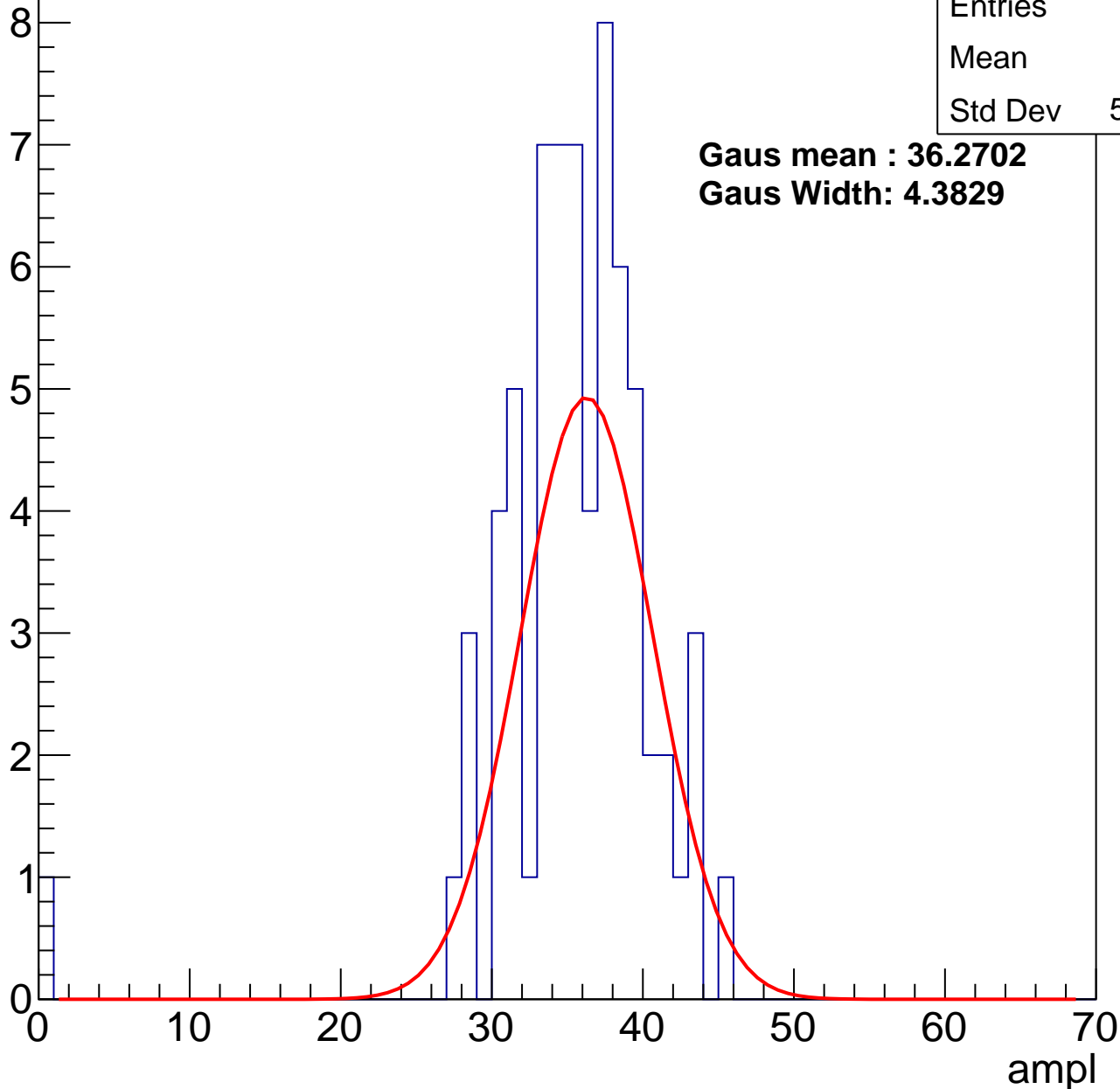
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	34.9
Std Dev	5.806

**Gaus mean : 36.2702**

**Gaus Width: 4.3829**



# B1L101S, U18-ch98, adc2

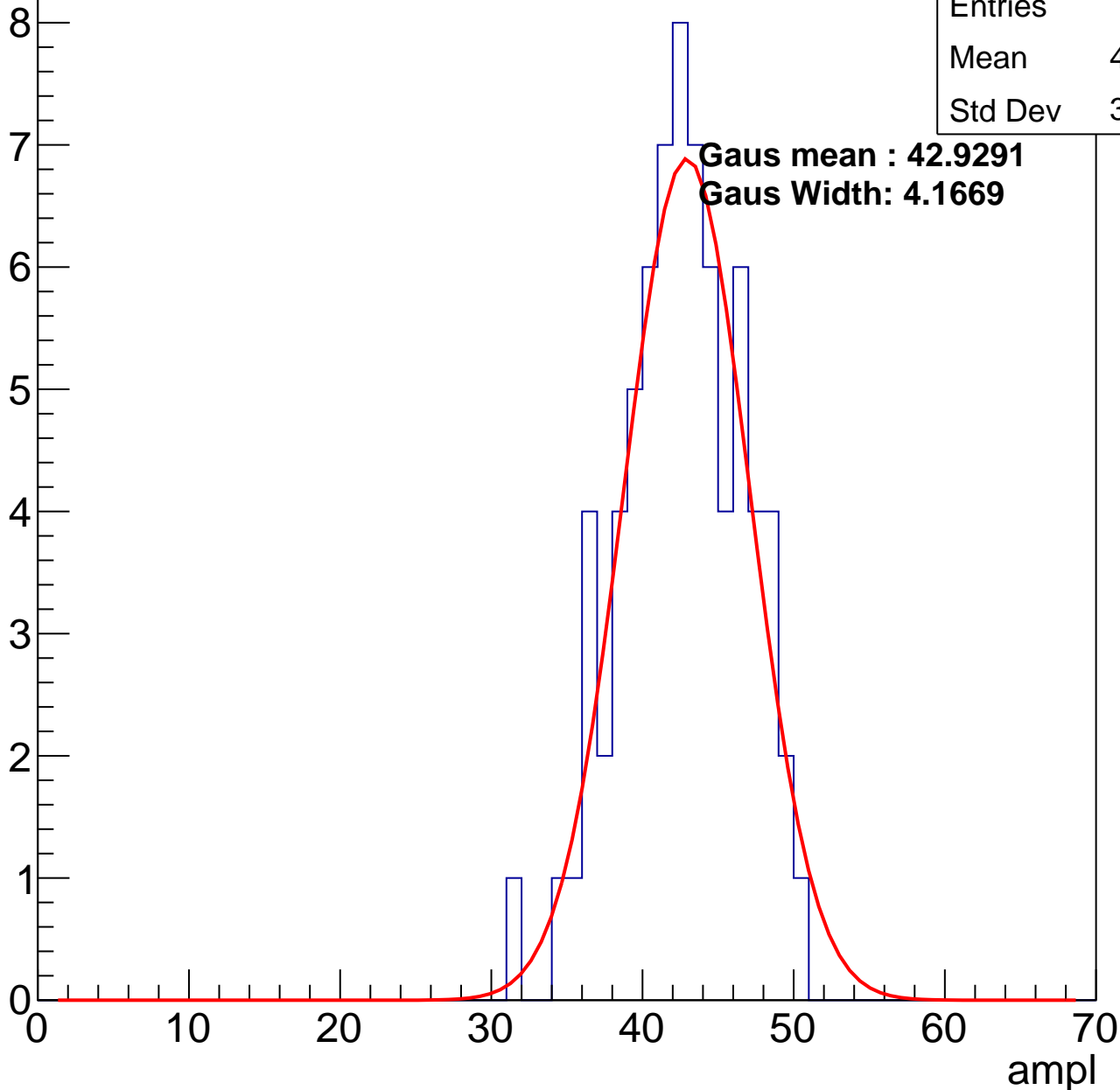
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	42.15
Std Dev	3.944

**Gaus mean : 42.9291**

**Gaus Width: 4.1669**

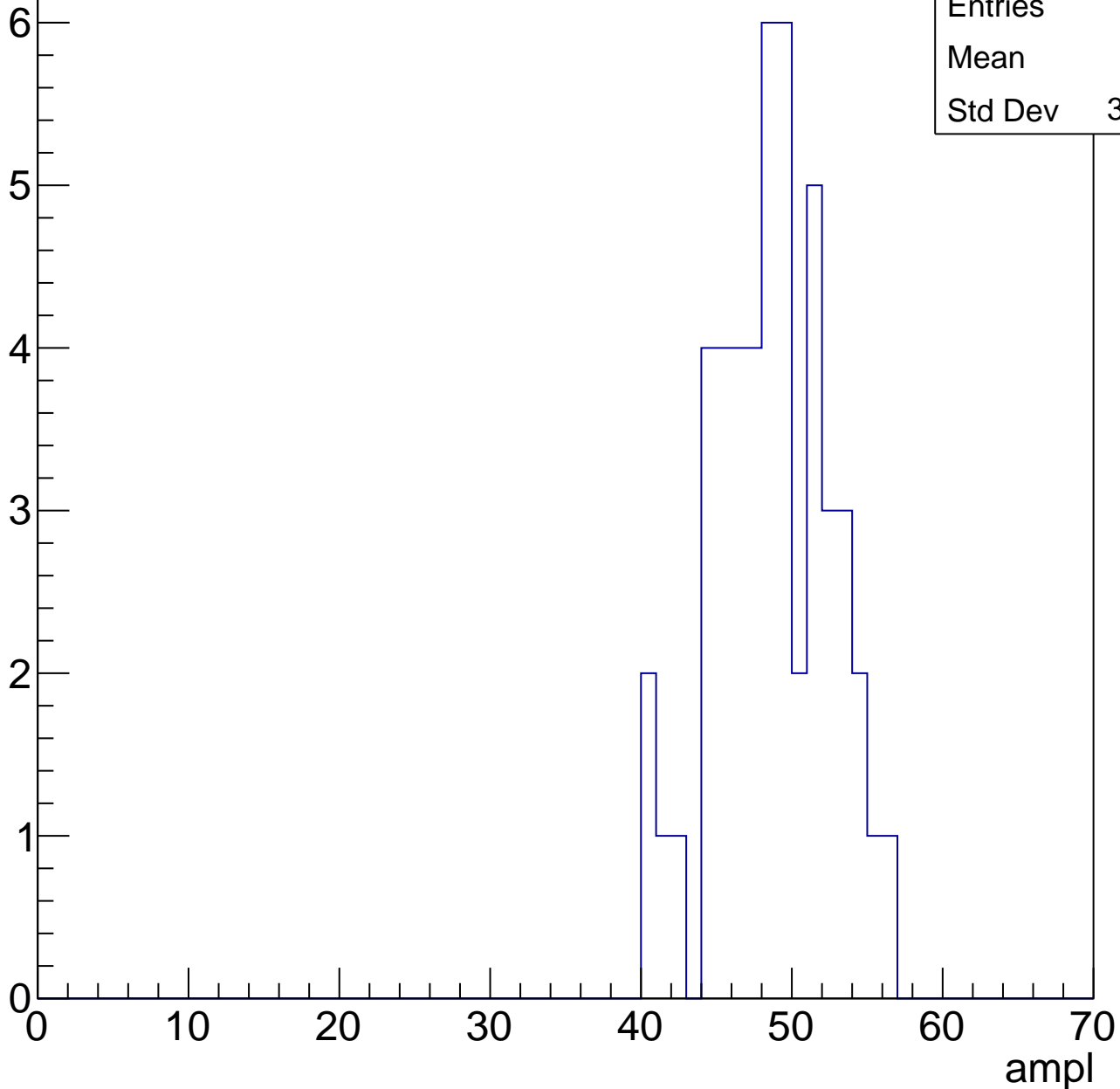


# B1L101S, U18-ch98, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

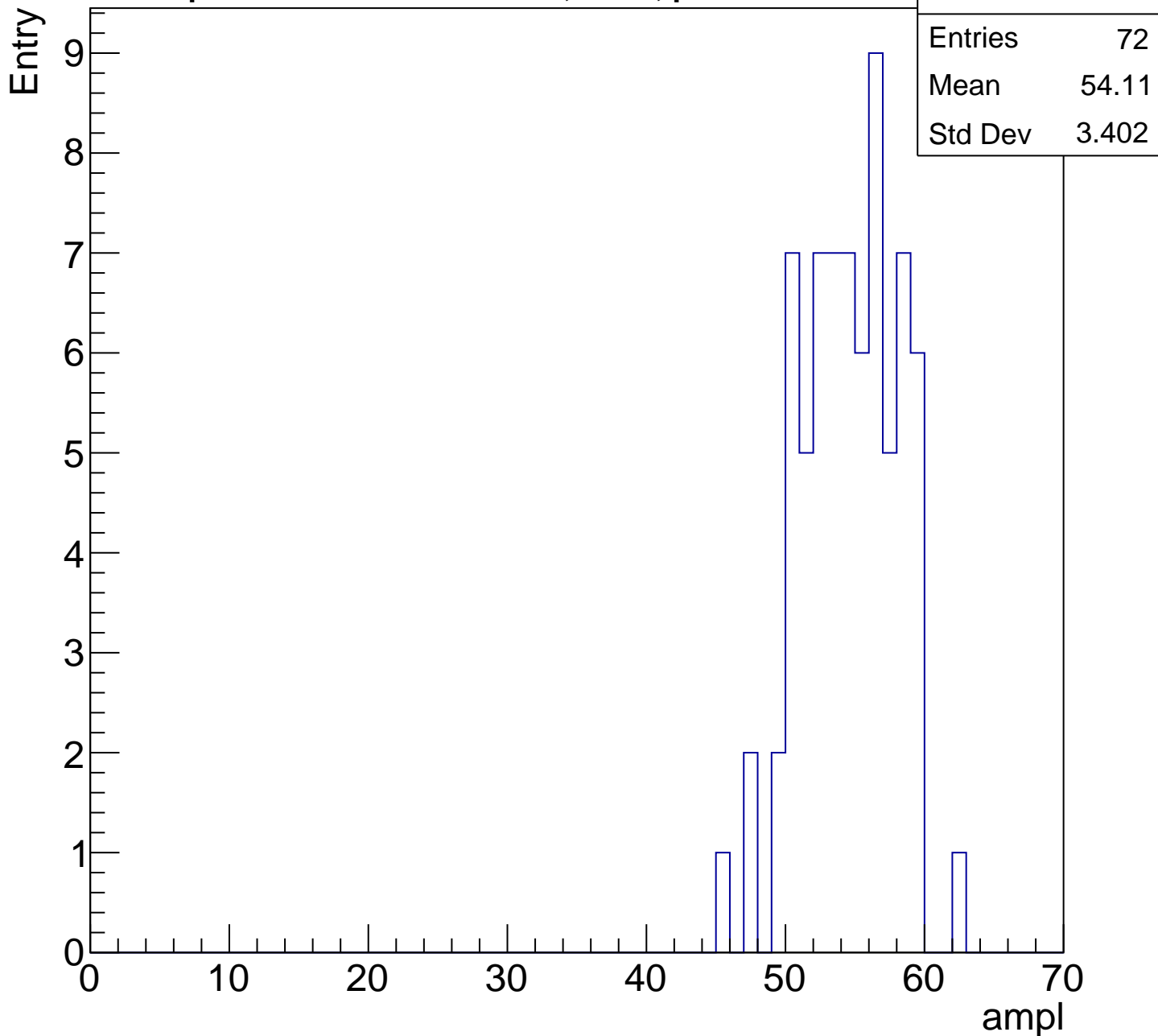
Entry

Entries	49
Mean	48.2
Std Dev	3.774



# B1L101S, U18-ch98, adc4

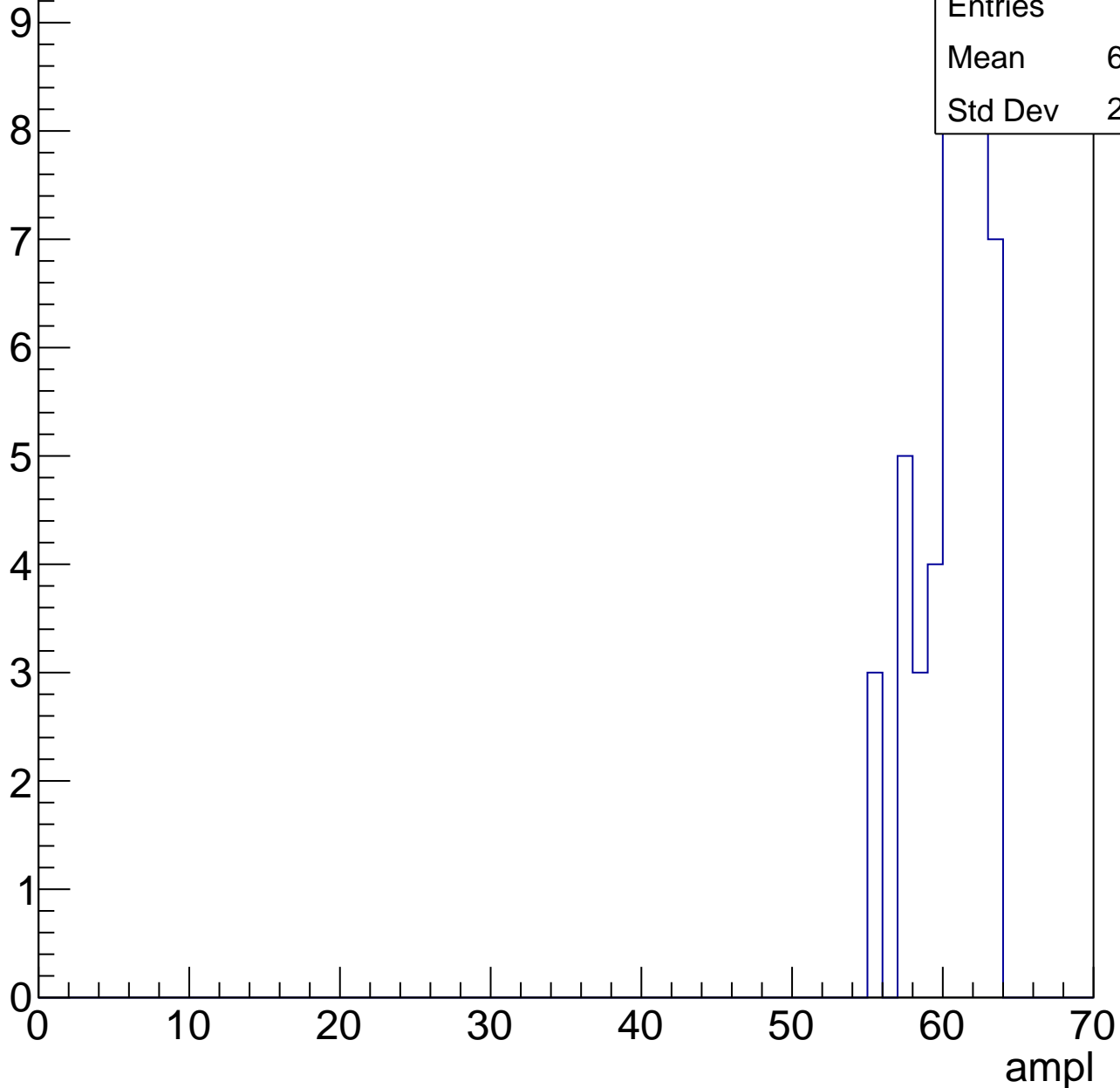
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U18-ch98, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

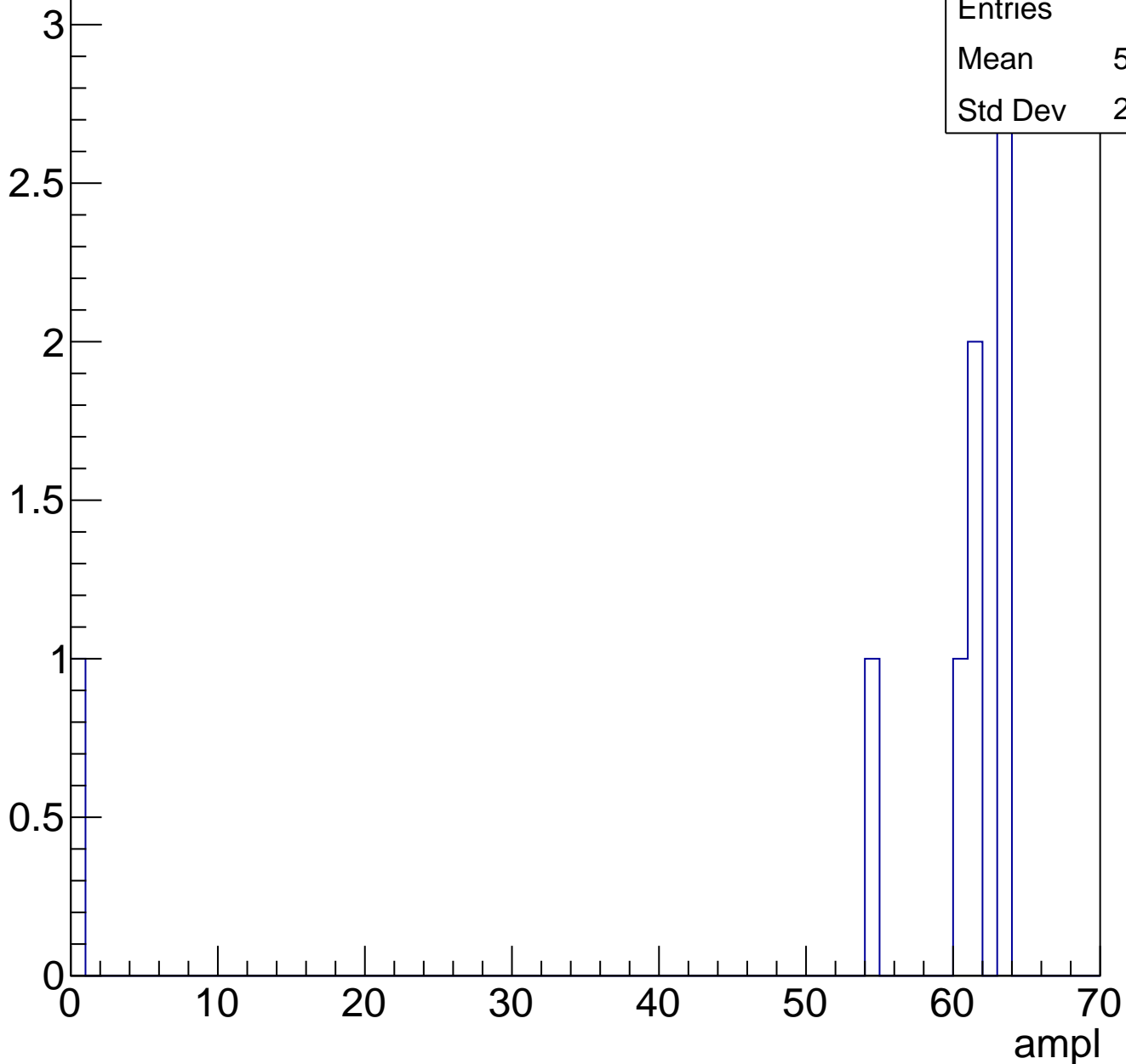
Entry



# B1L101S, U18-ch98, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch98, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U18-ch99, adc0

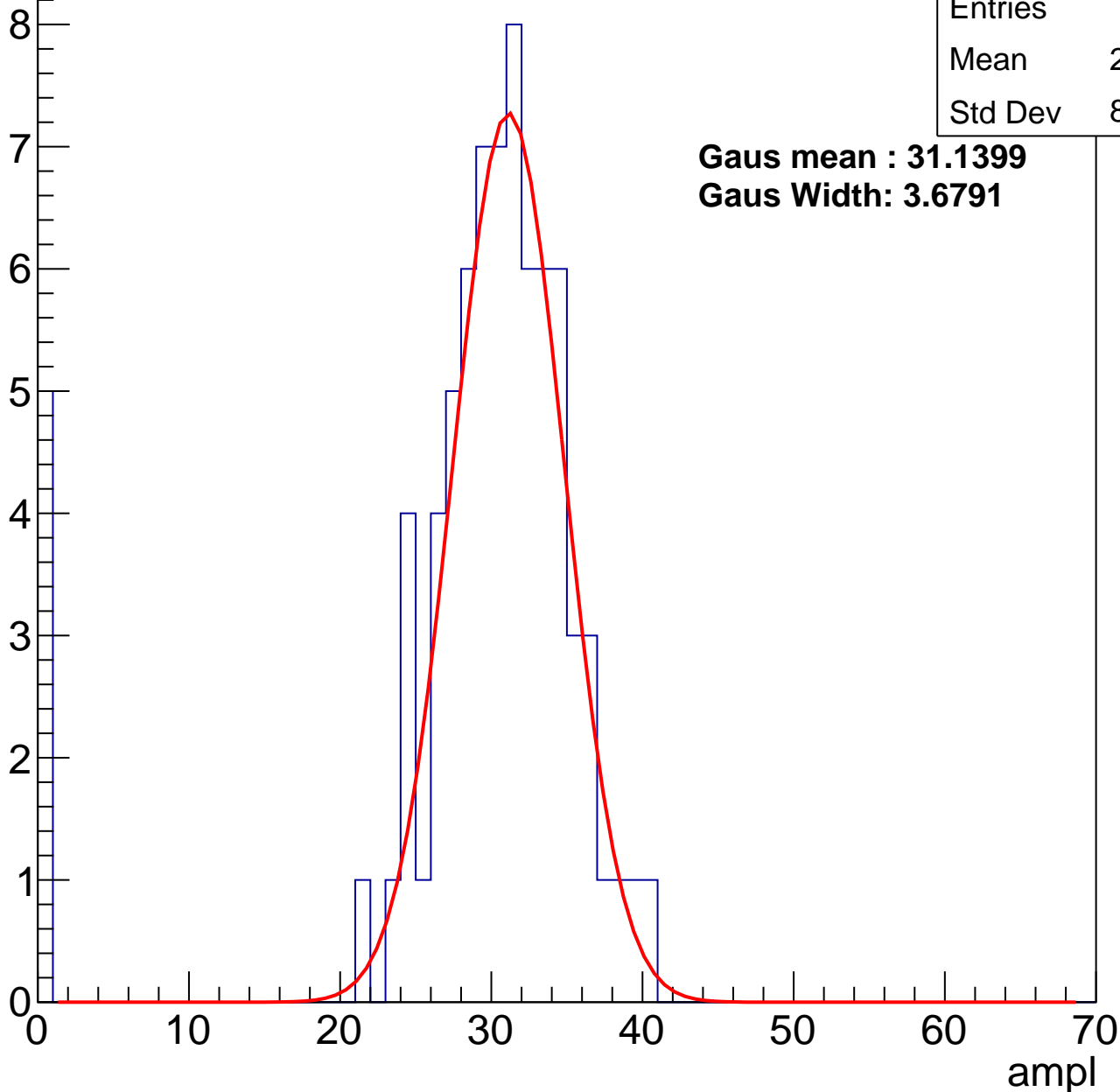
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	28.49
Std Dev	8.392

**Gaus mean : 31.1399**

**Gaus Width: 3.6791**



# B1L101S, U18-ch99, adc1

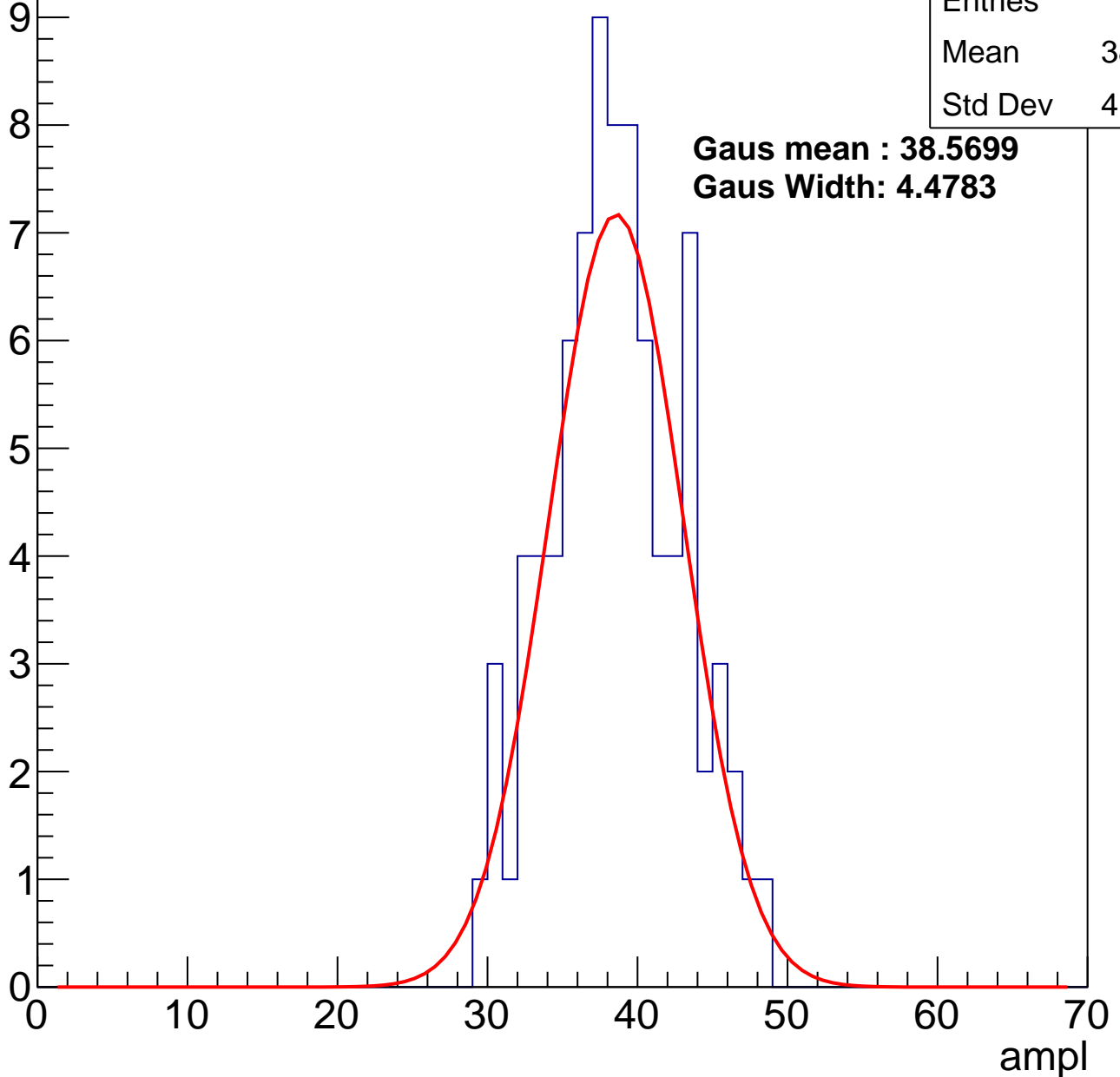
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	85
Mean	38.12
Std Dev	4.277

**Gaus mean : 38.5699**

**Gaus Width: 4.4783**



# B1L101S, U18-ch99, adc2

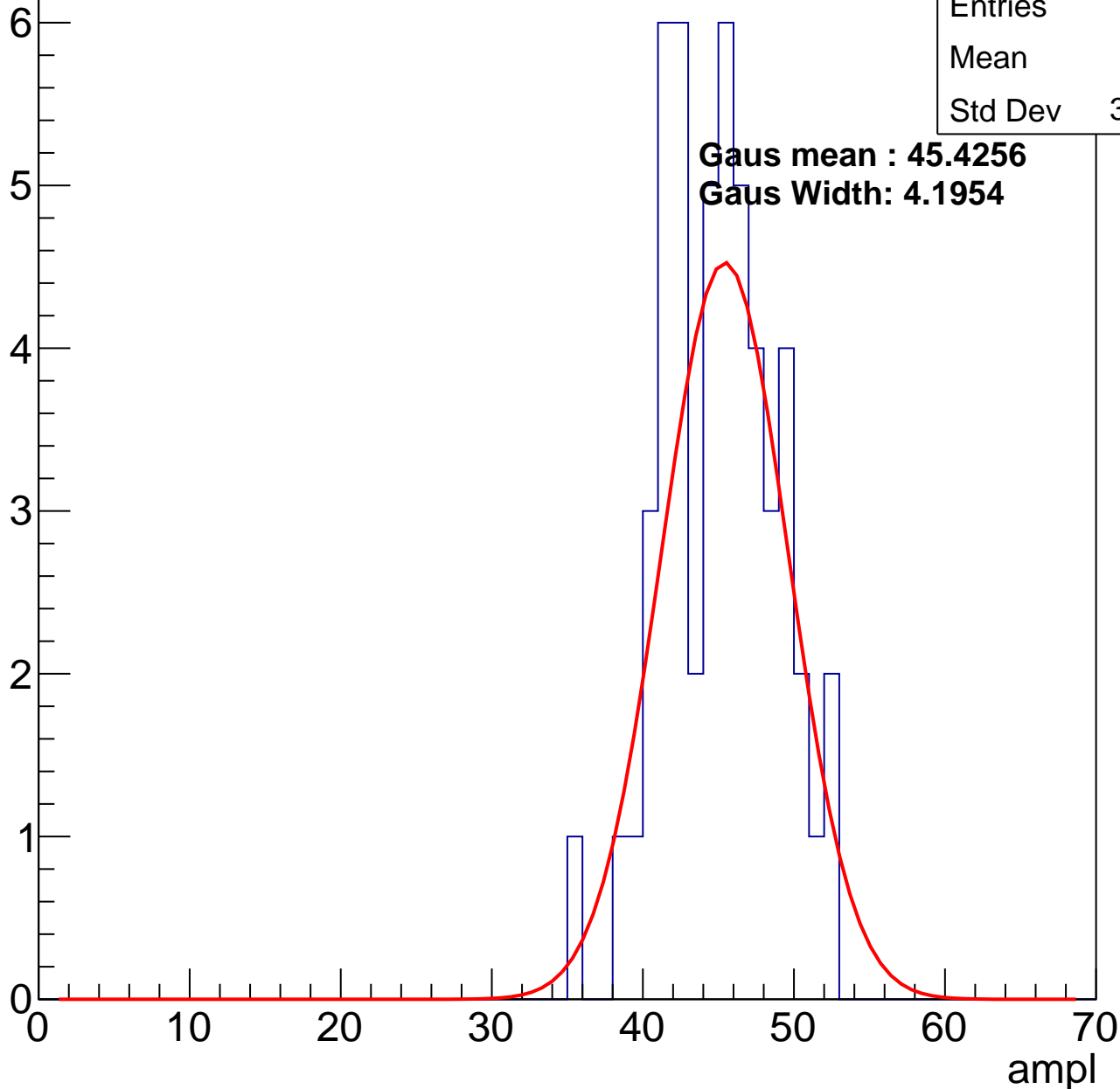
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	44.6
Std Dev	3.696

**Gaus mean : 45.4256**

**Gaus Width: 4.1954**

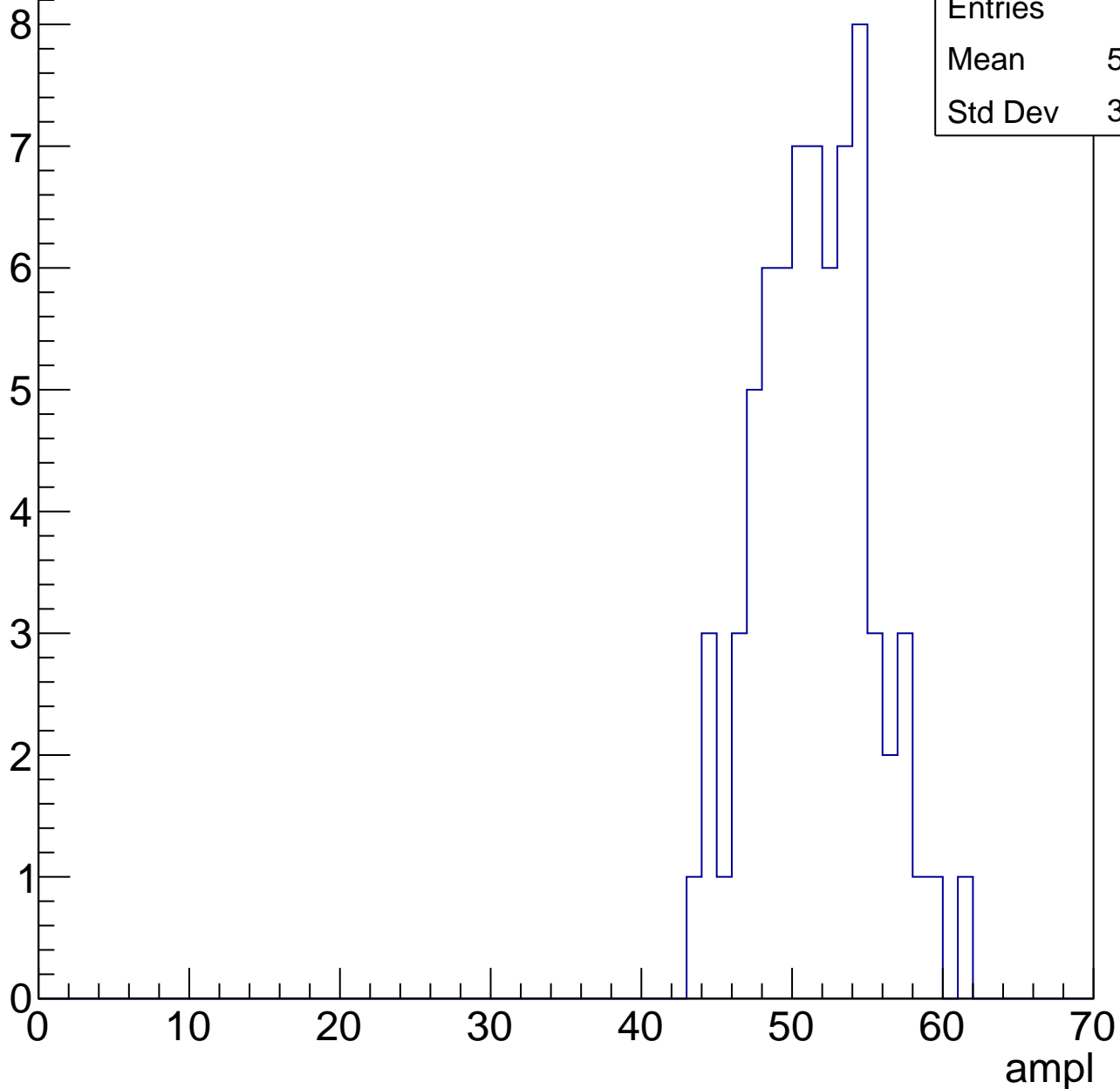


# B1L101S, U18-ch99, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	51.03
Std Dev	3.775

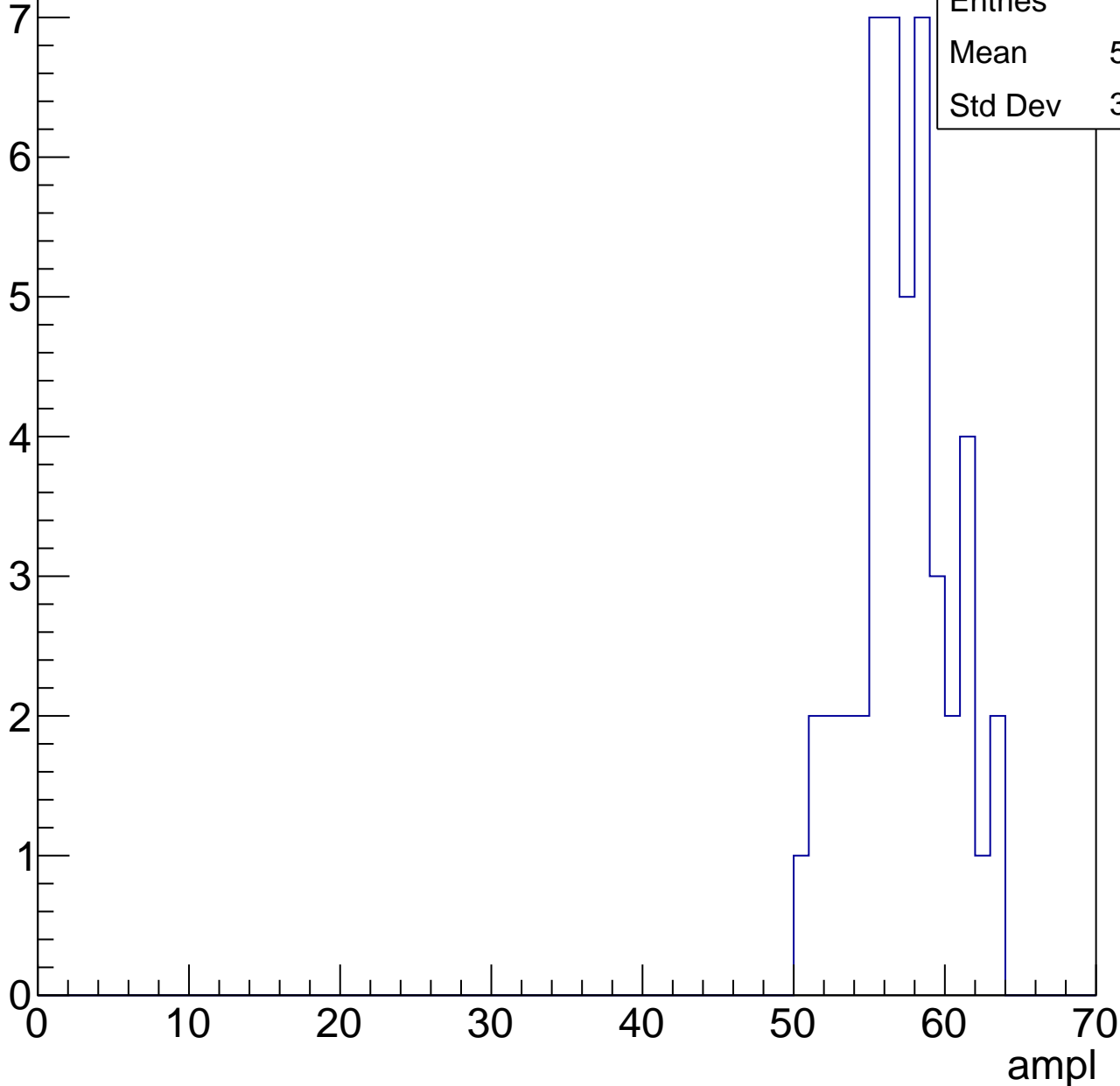


# B1L101S, U18-ch99, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	47
Mean	56.74
Std Dev	3.097

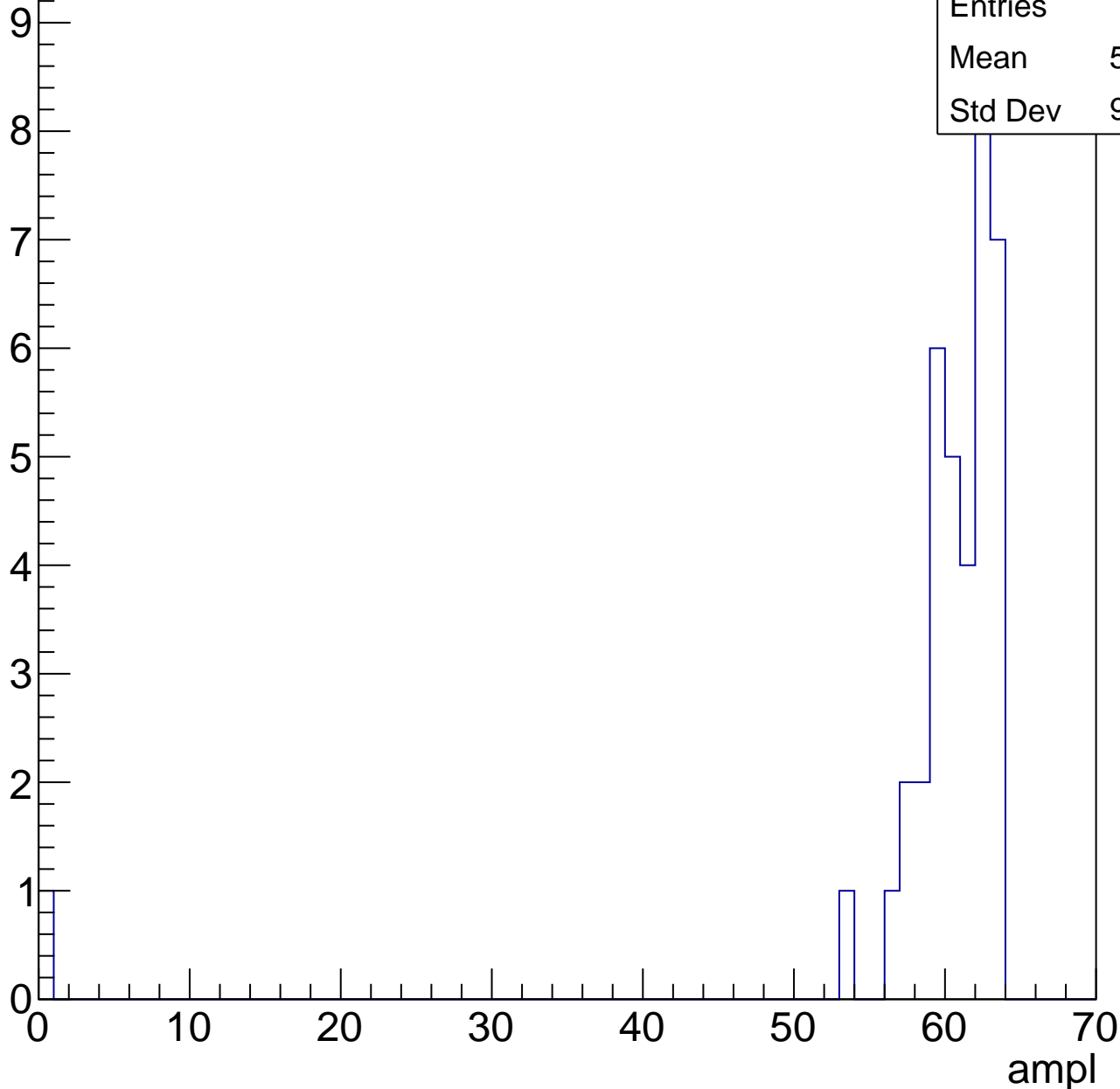


# B1L101S, U18-ch99, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

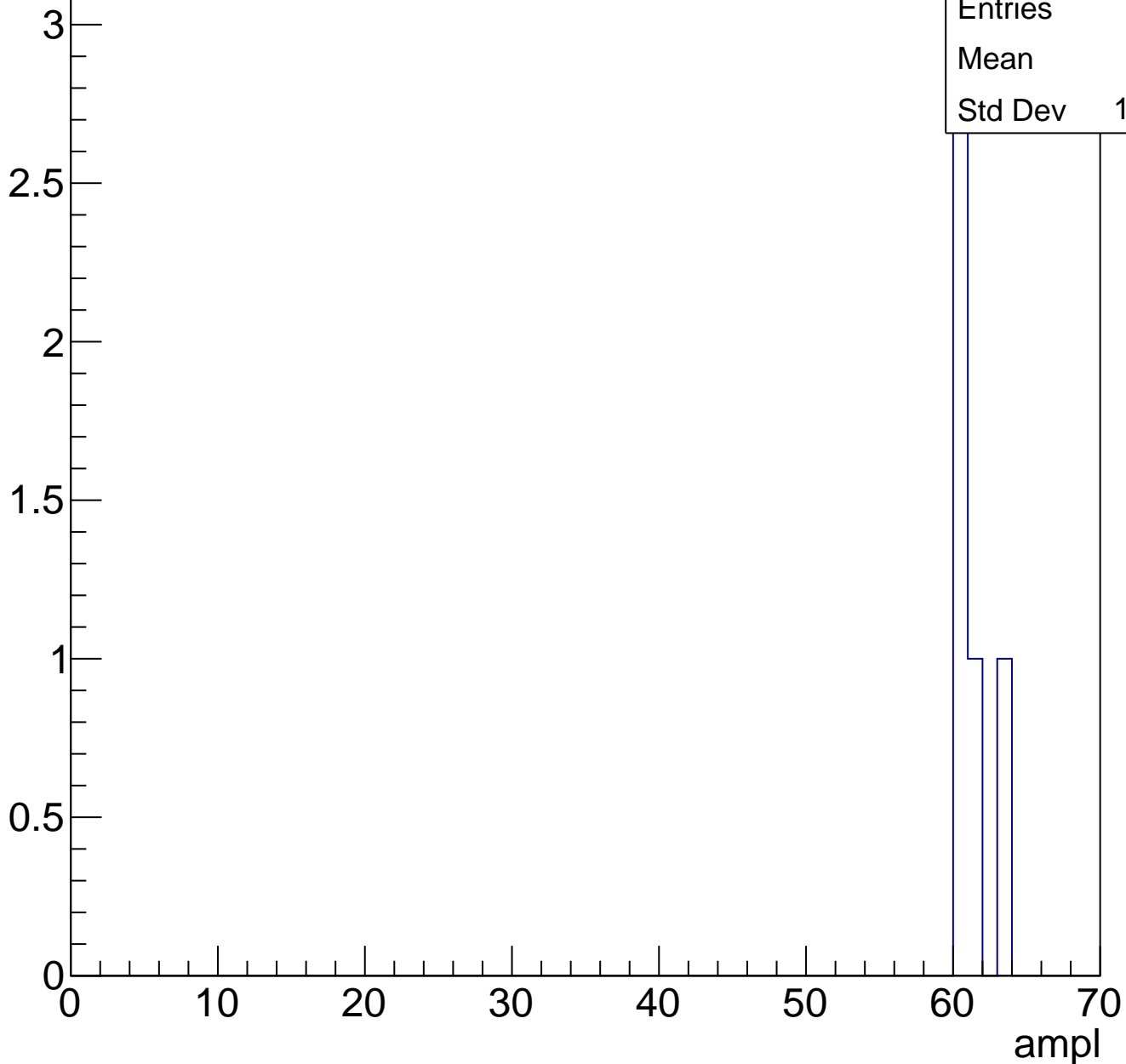
Entries	38
Mean	58.84
Std Dev	9.933



# B1L101S, U18-ch99, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch99, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch100, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	68
Mean	28.6
Std Dev	7.889

**Gaus mean : 30.6543**

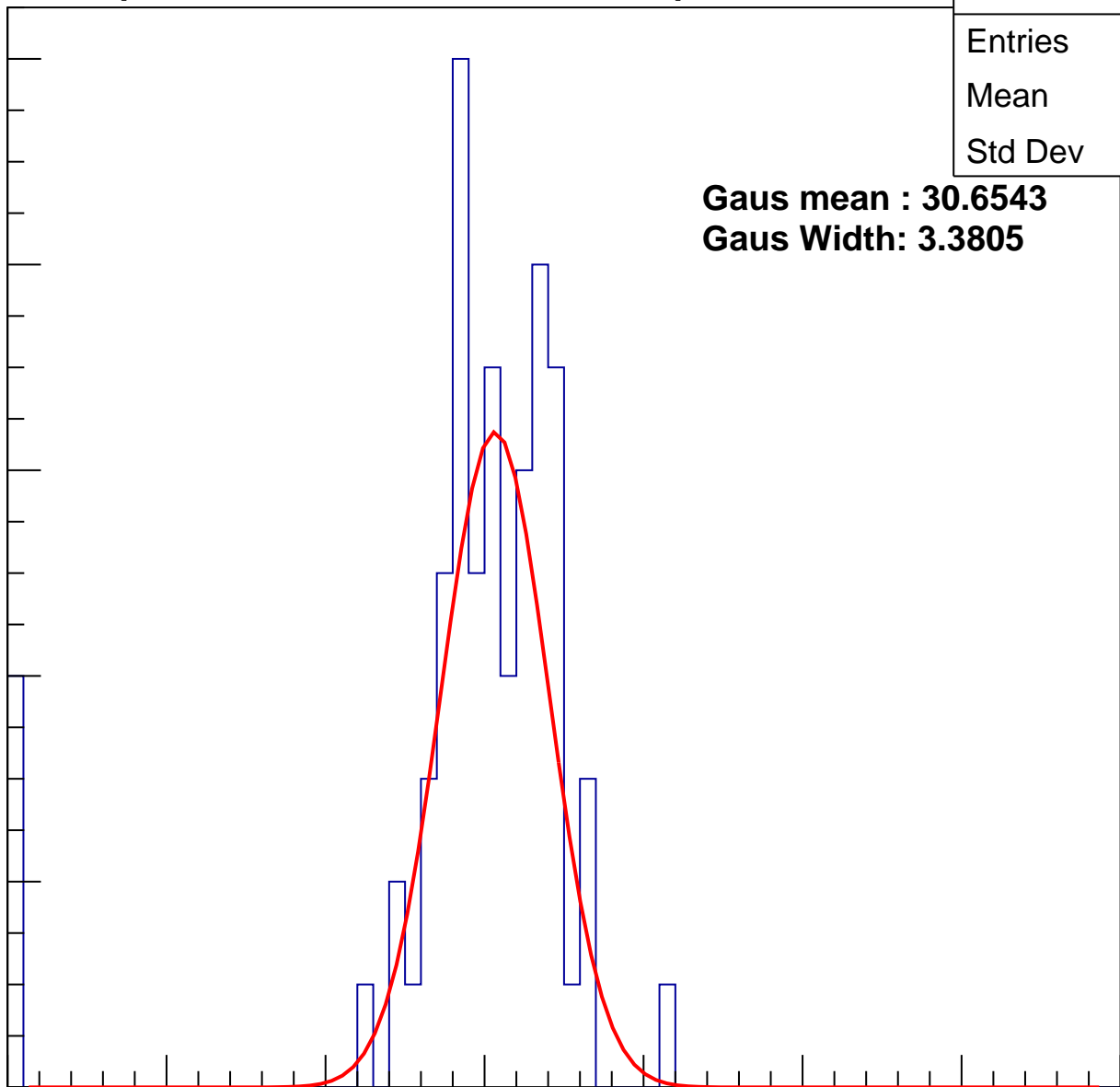
**Gaus Width: 3.3805**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L101S, U18-ch100, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

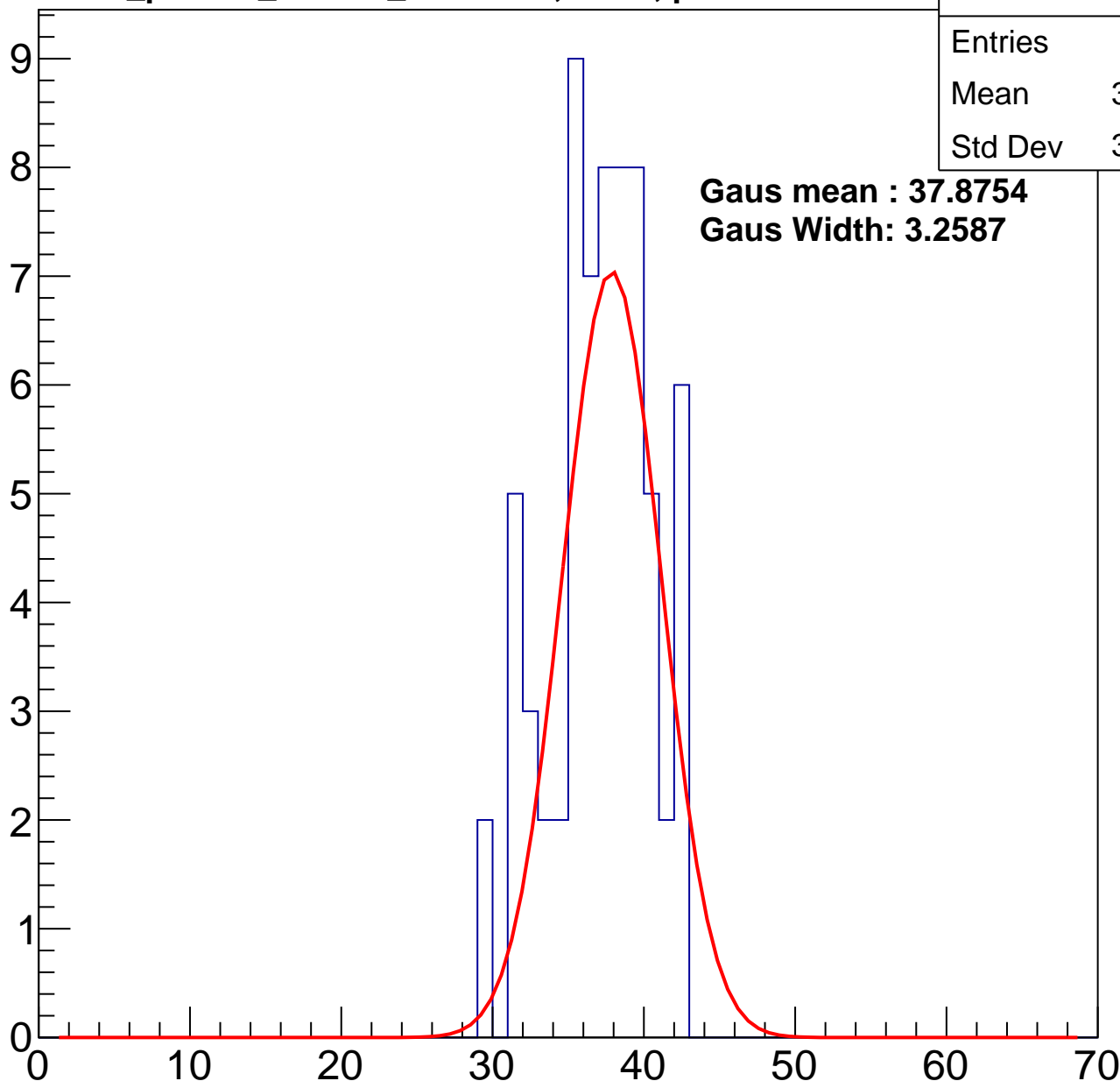
9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	67
Mean	36.66
Std Dev	3.312

**Gaus mean : 37.8754**

**Gaus Width: 3.2587**

ampl



# B1L101S, U18-ch100, adc2

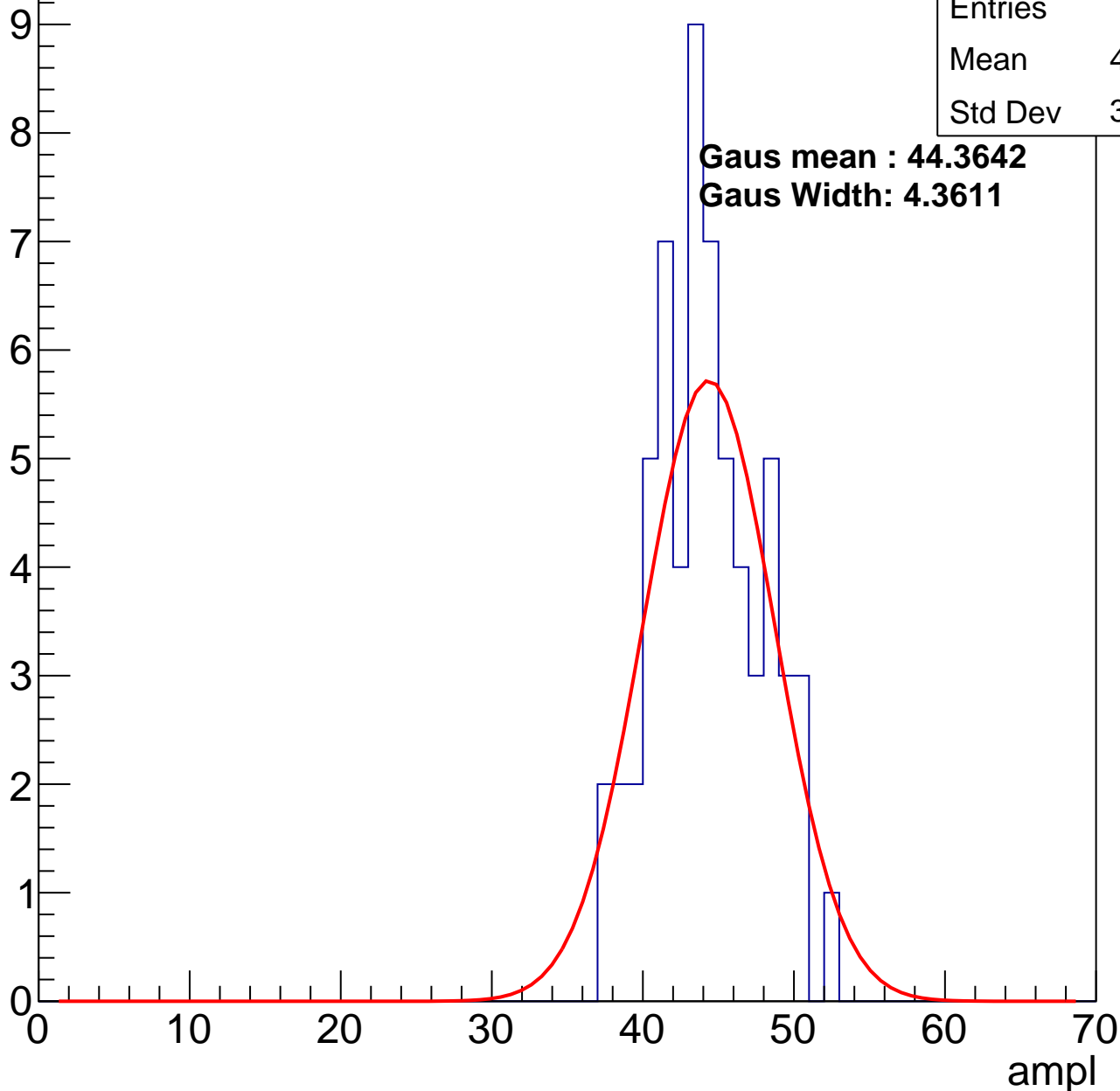
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	43.82
Std Dev	3.504

**Gaus mean : 44.3642**

**Gaus Width: 4.3611**

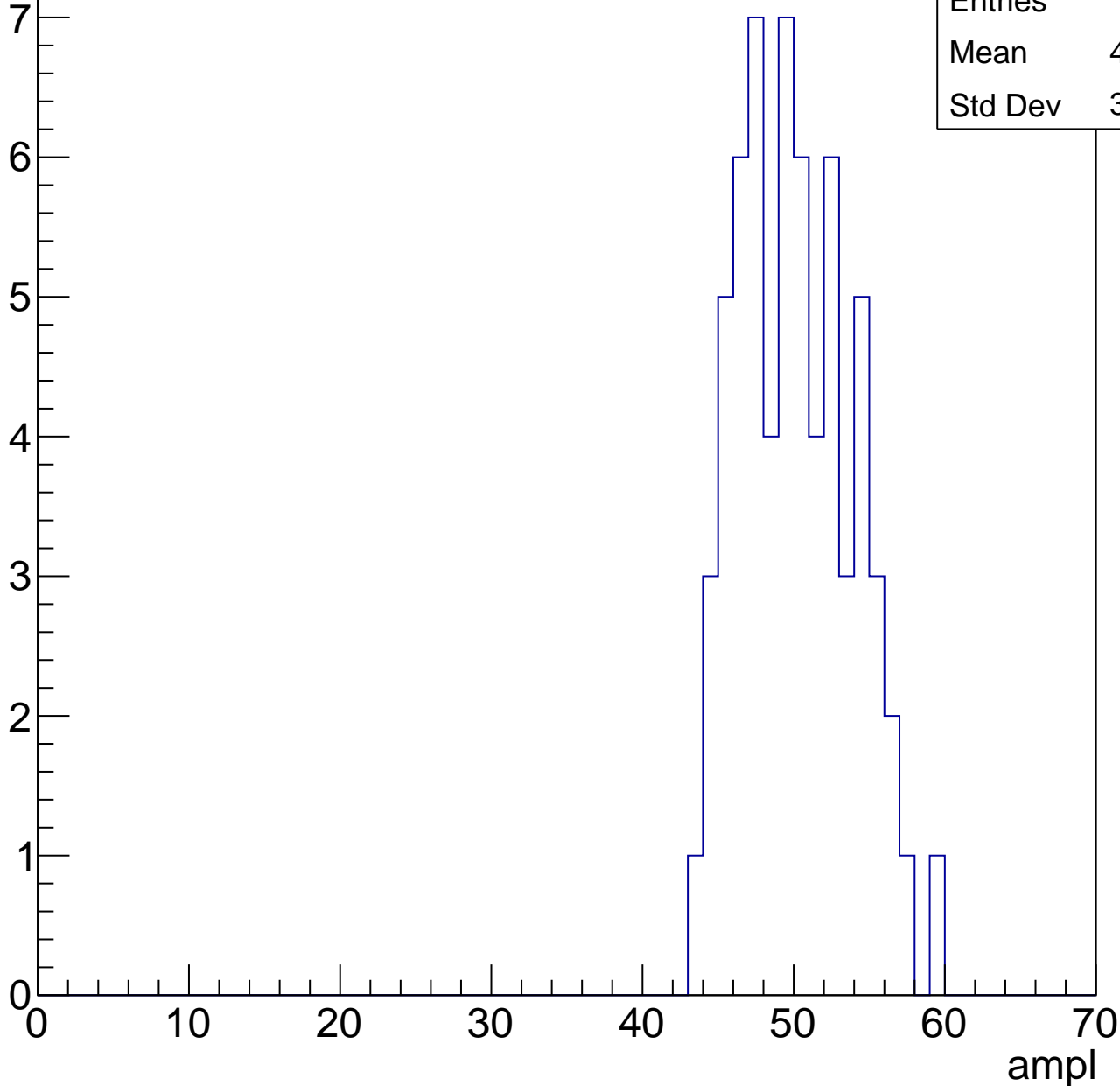


# B1L101S, U18-ch100, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	49.66
Std Dev	3.684

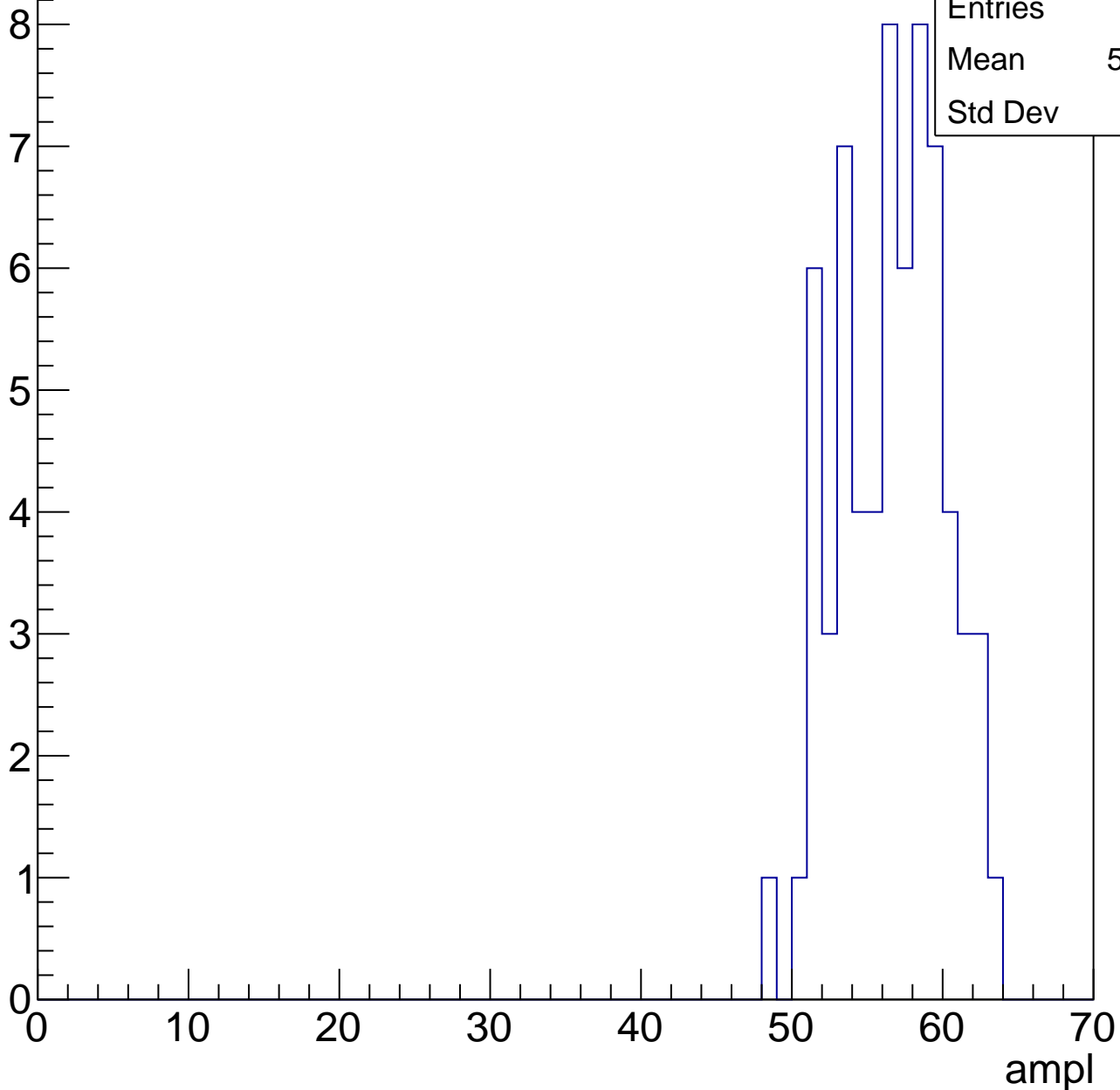


# B1L101S, U18-ch100, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	56.15
Std Dev	3.43

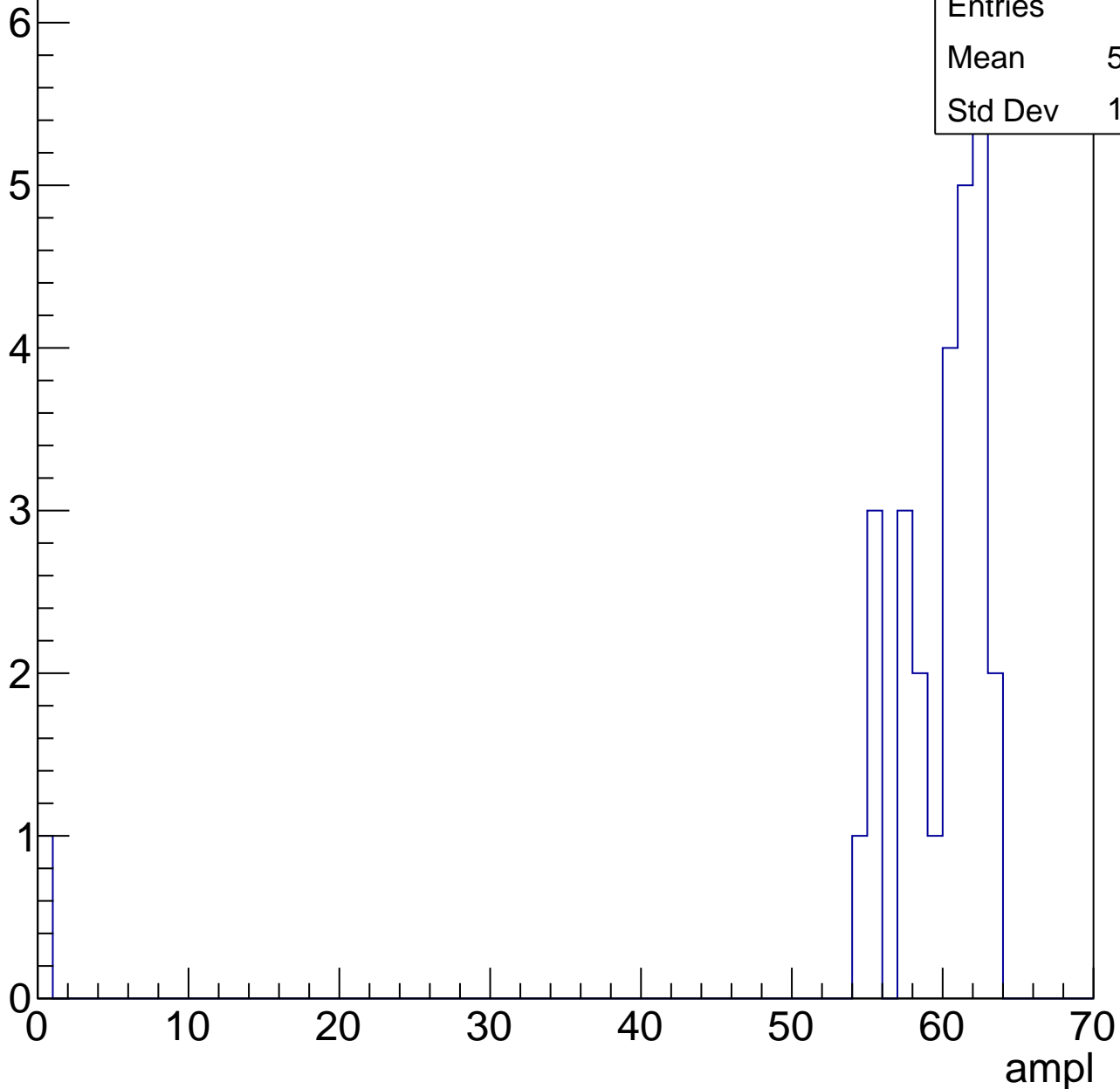


# B1L101S, U18-ch100, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	28
Mean	57.43
Std Dev	11.35

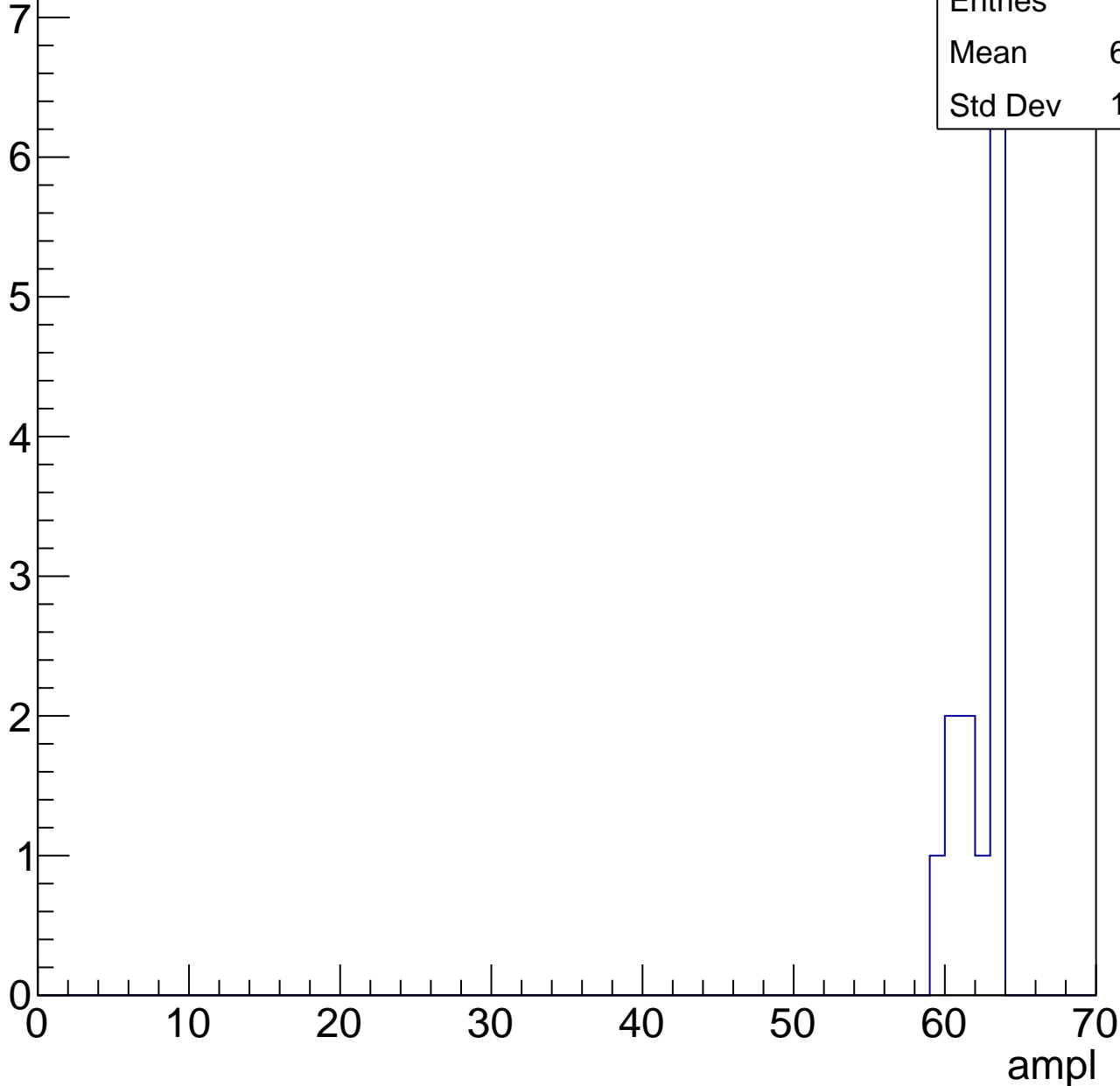


# B1L101S, U18-ch100, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	13
Mean	61.85
Std Dev	1.406





# B1L101S, U18-ch100, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U18-ch101, adc0

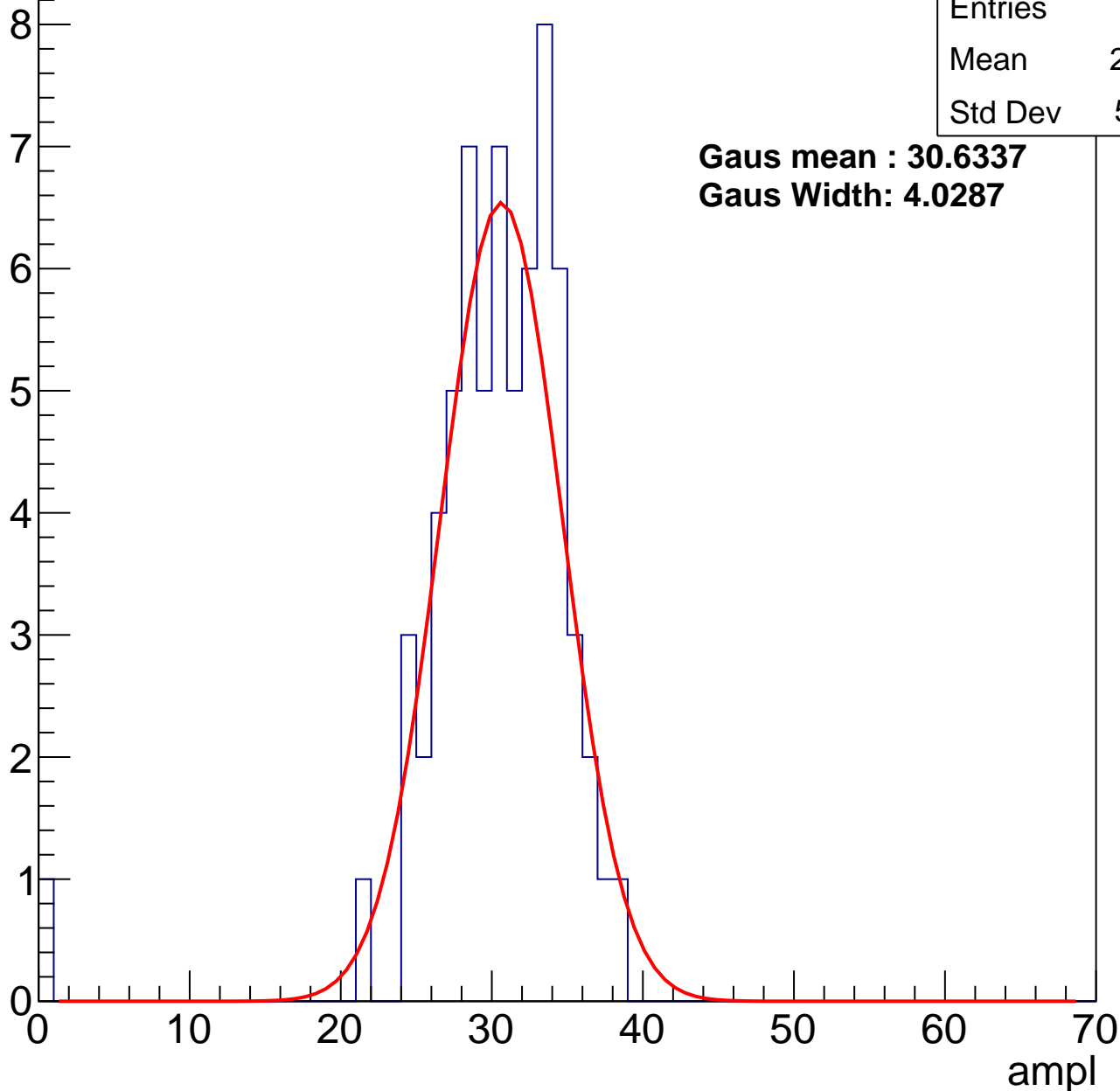
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	29.85
Std Dev	5.091

**Gaus mean : 30.6337**

**Gaus Width: 4.0287**



# B1L101S, U18-ch101, adc1

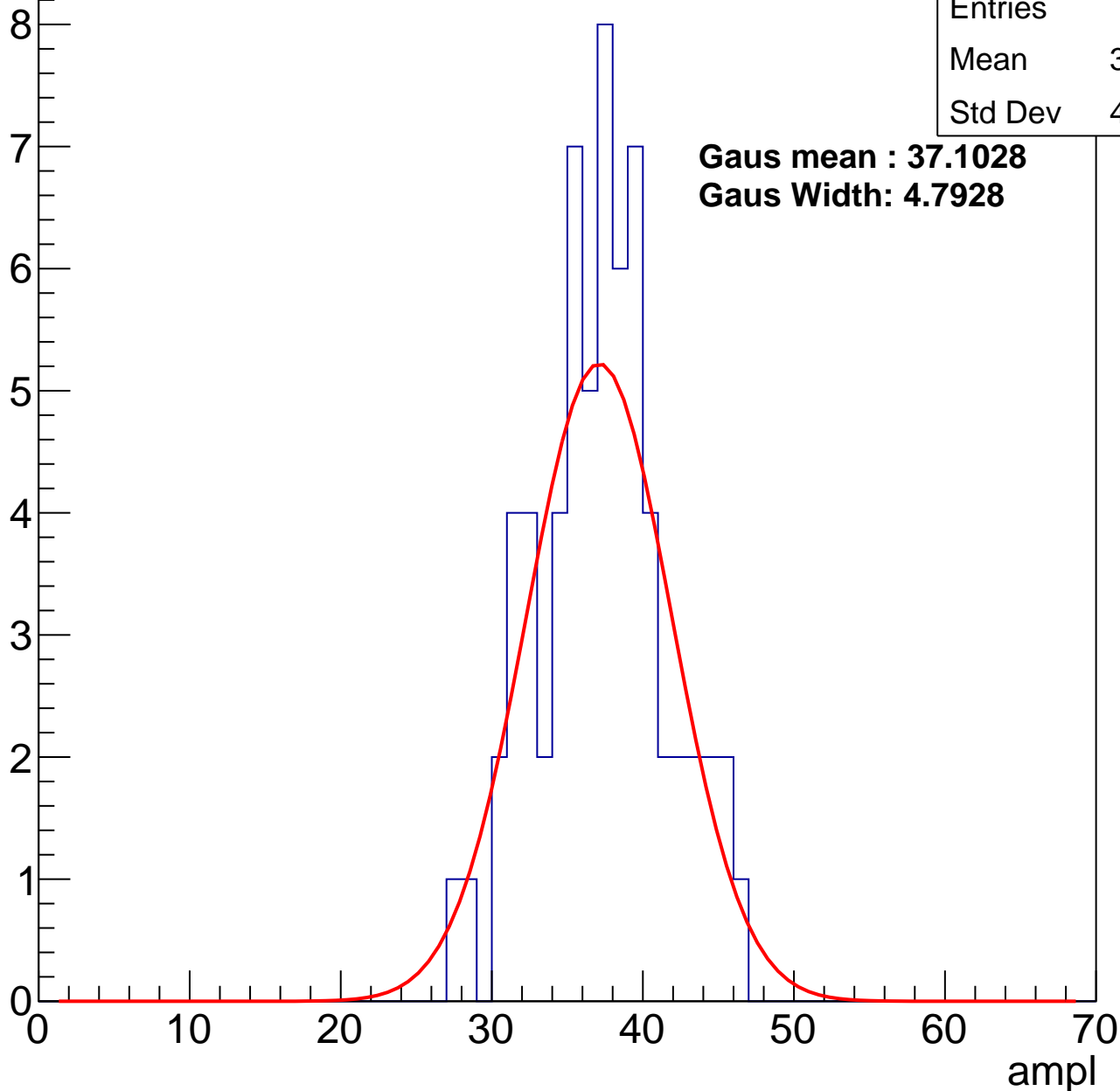
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	36.77
Std Dev	4.177

**Gaus mean : 37.1028**

**Gaus Width: 4.7928**



# B1L101S, U18-ch101, adc2

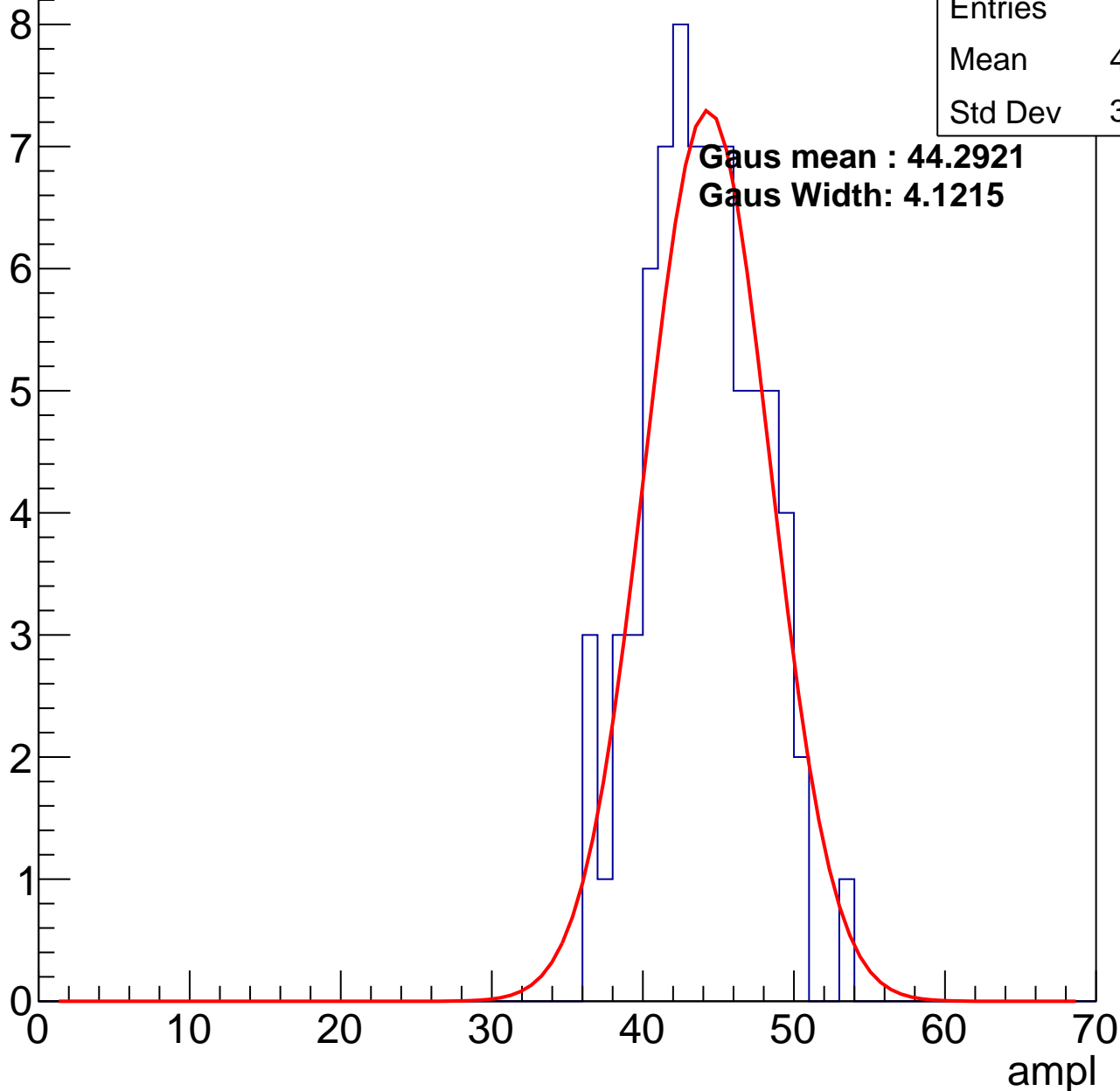
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	43.47
Std Dev	3.688

**Gaus mean : 44.2921**

**Gaus Width: 4.1215**

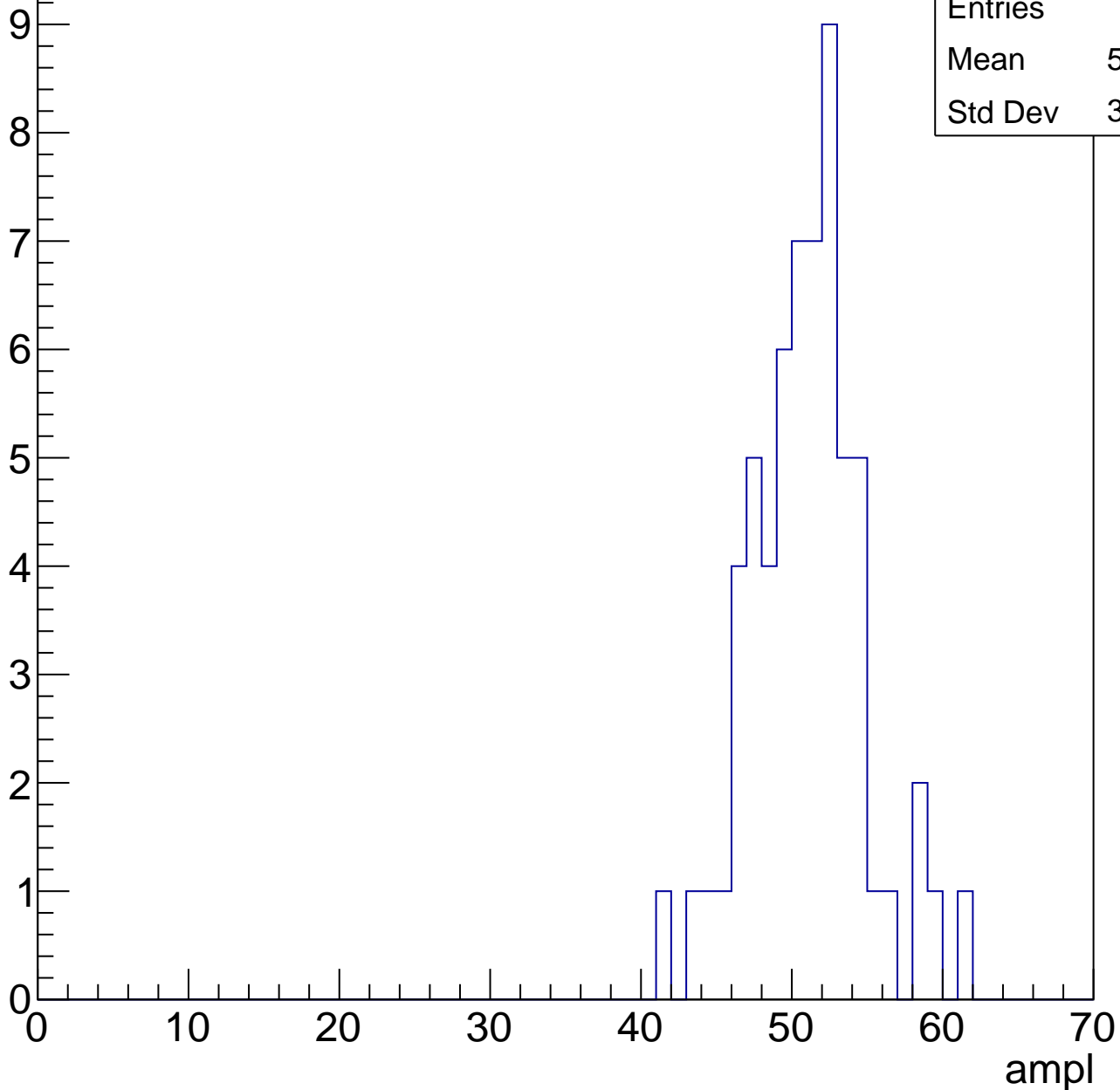


# B1L101S, U18-ch101, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	50.56
Std Dev	3.727

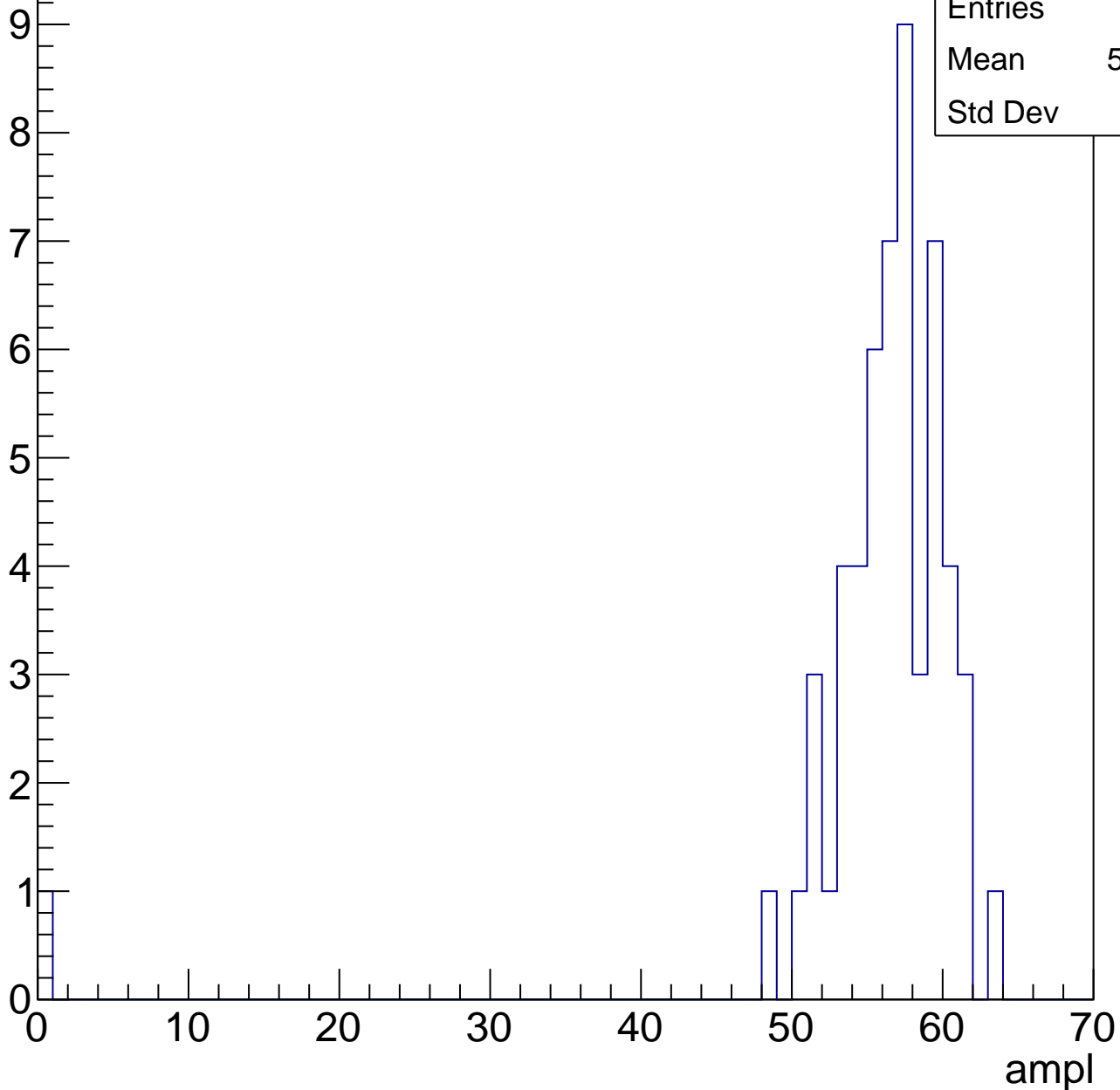


# B1L101S, U18-ch101, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	55.25
Std Dev	8.12

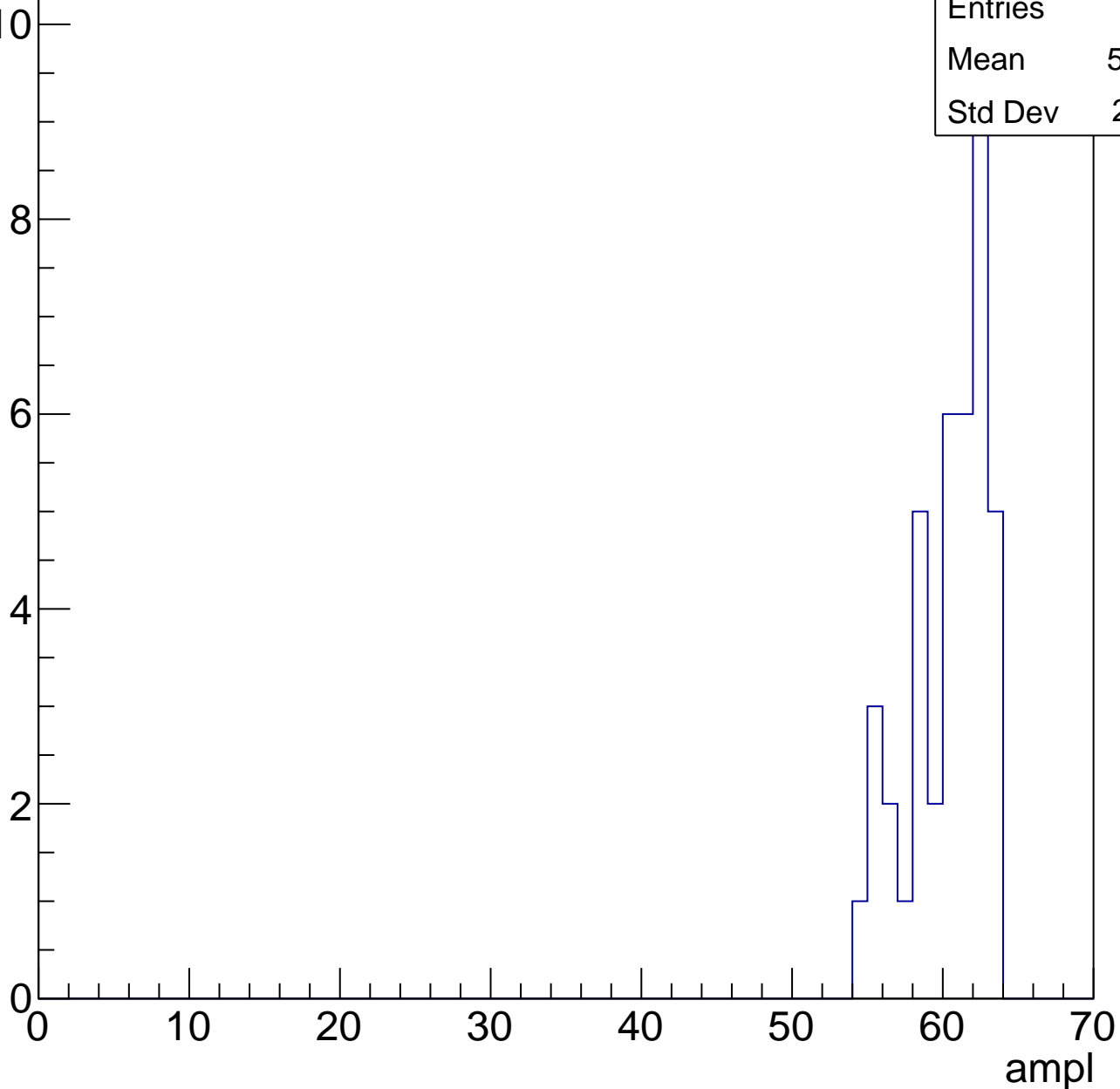


# B1L101S, U18-ch101, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	41
Mean	59.93
Std Dev	2.541



# B1L101S, U18-ch101, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch101, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U18-ch102, adc0

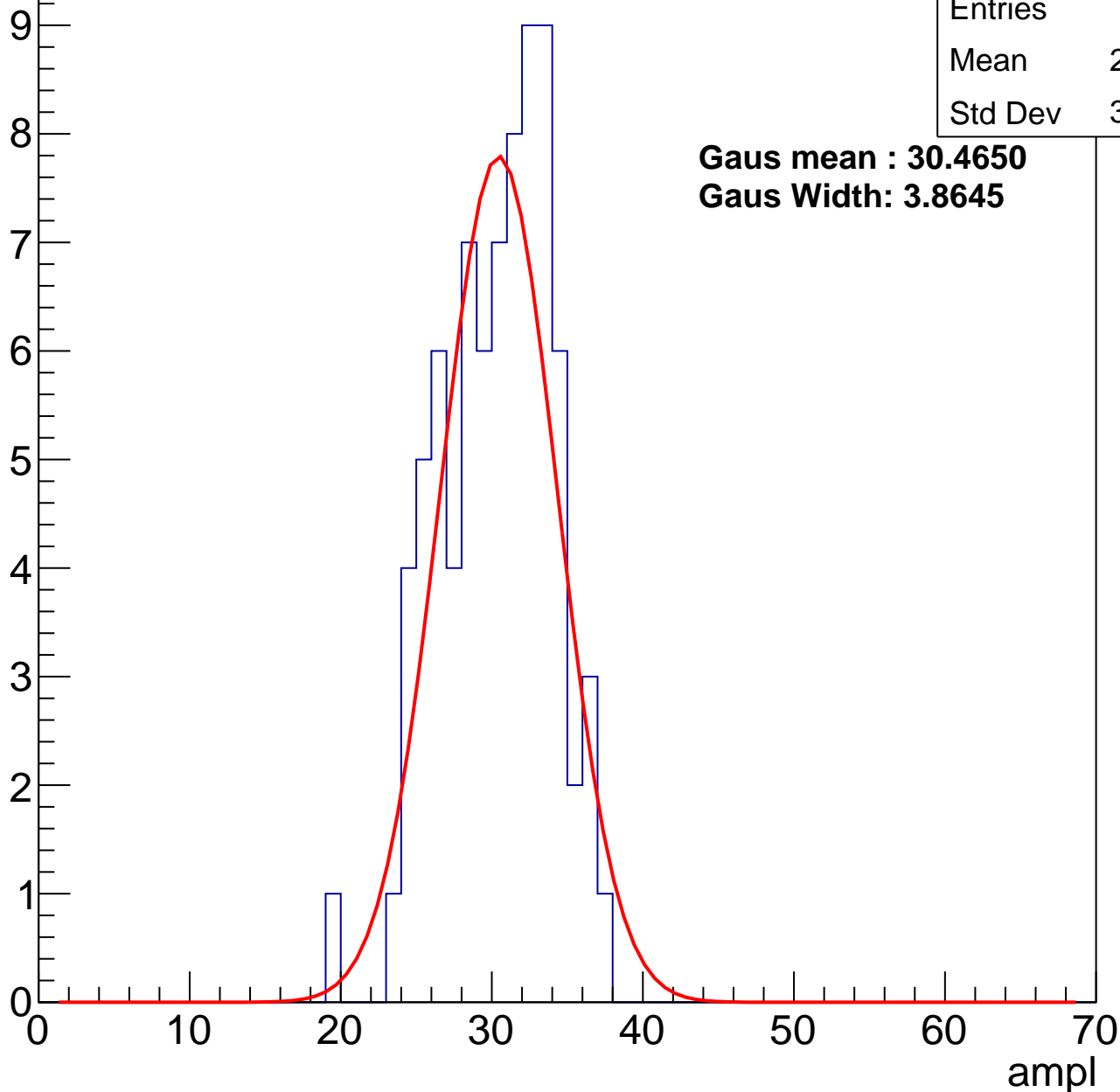
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	79
Mean	29.86
Std Dev	3.613

**Gaus mean : 30.4650**

**Gaus Width: 3.8645**



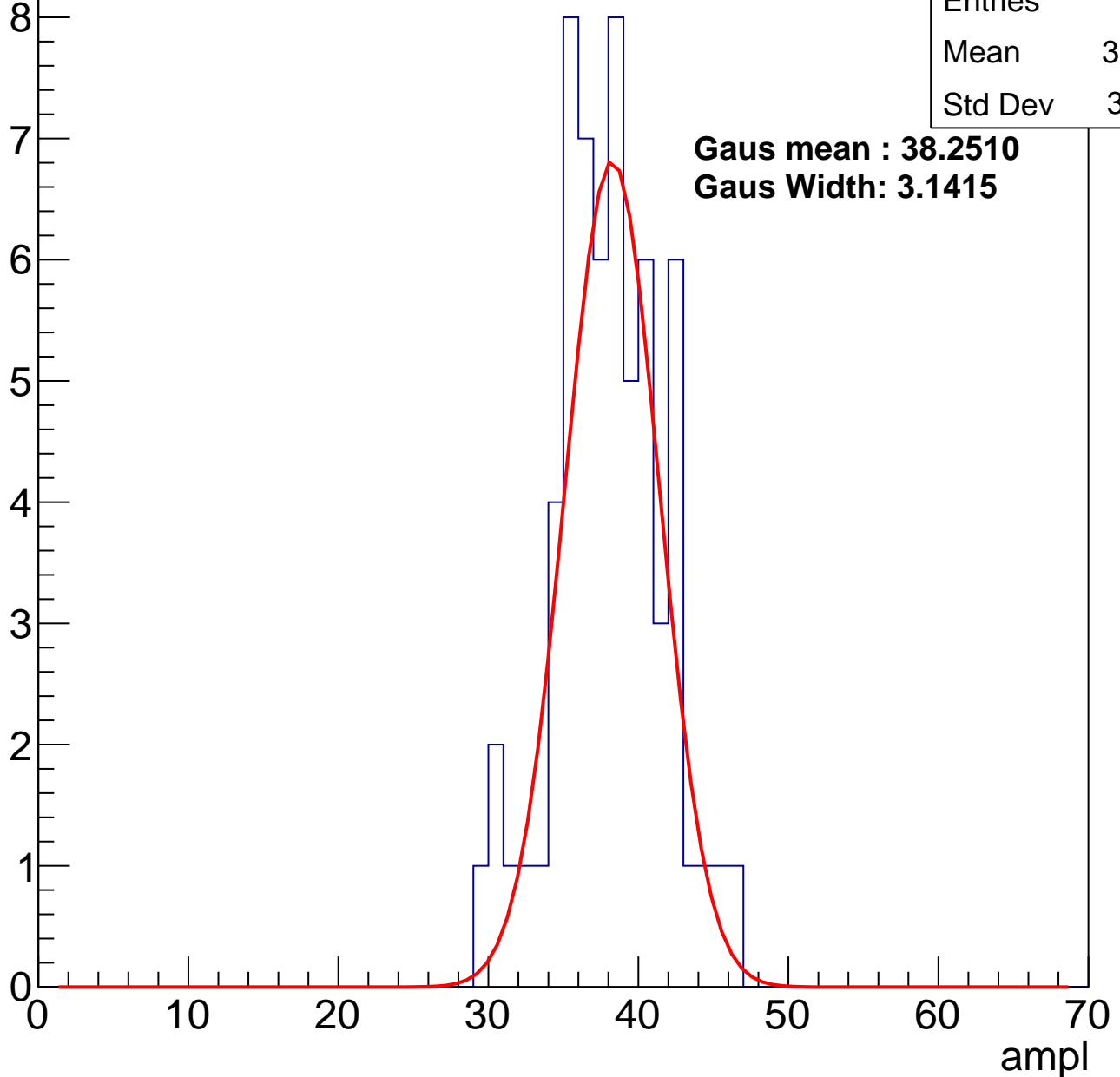
# B1L101S, U18-ch102, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	37.57
Std Dev	3.571

**Gaus mean : 38.2510**  
**Gaus Width: 3.1415**



# B1L101S, U18-ch102, adc2

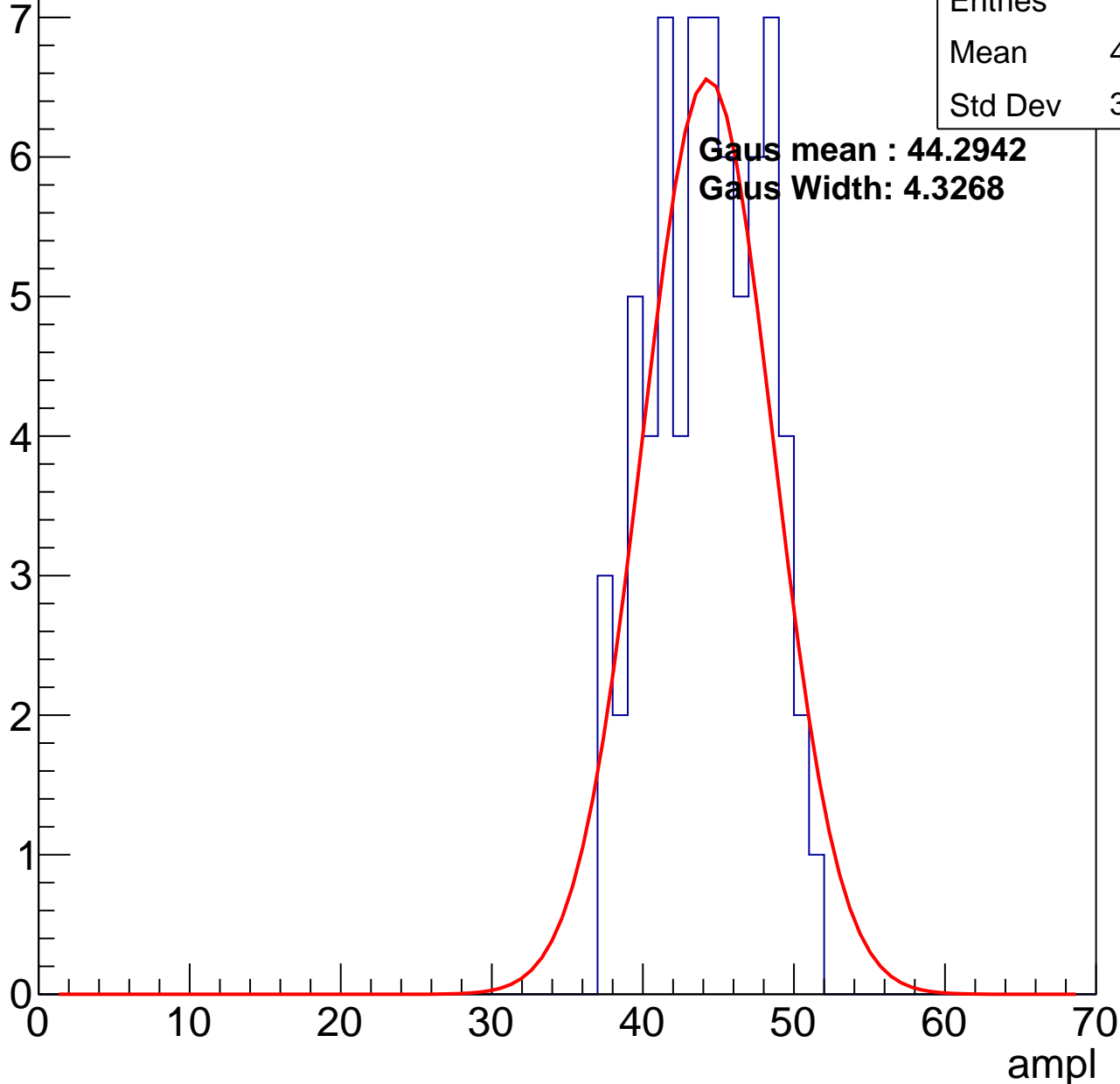
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	43.87
Std Dev	3.597

**Gaus mean : 44.2942**

**Gaus Width: 4.3268**

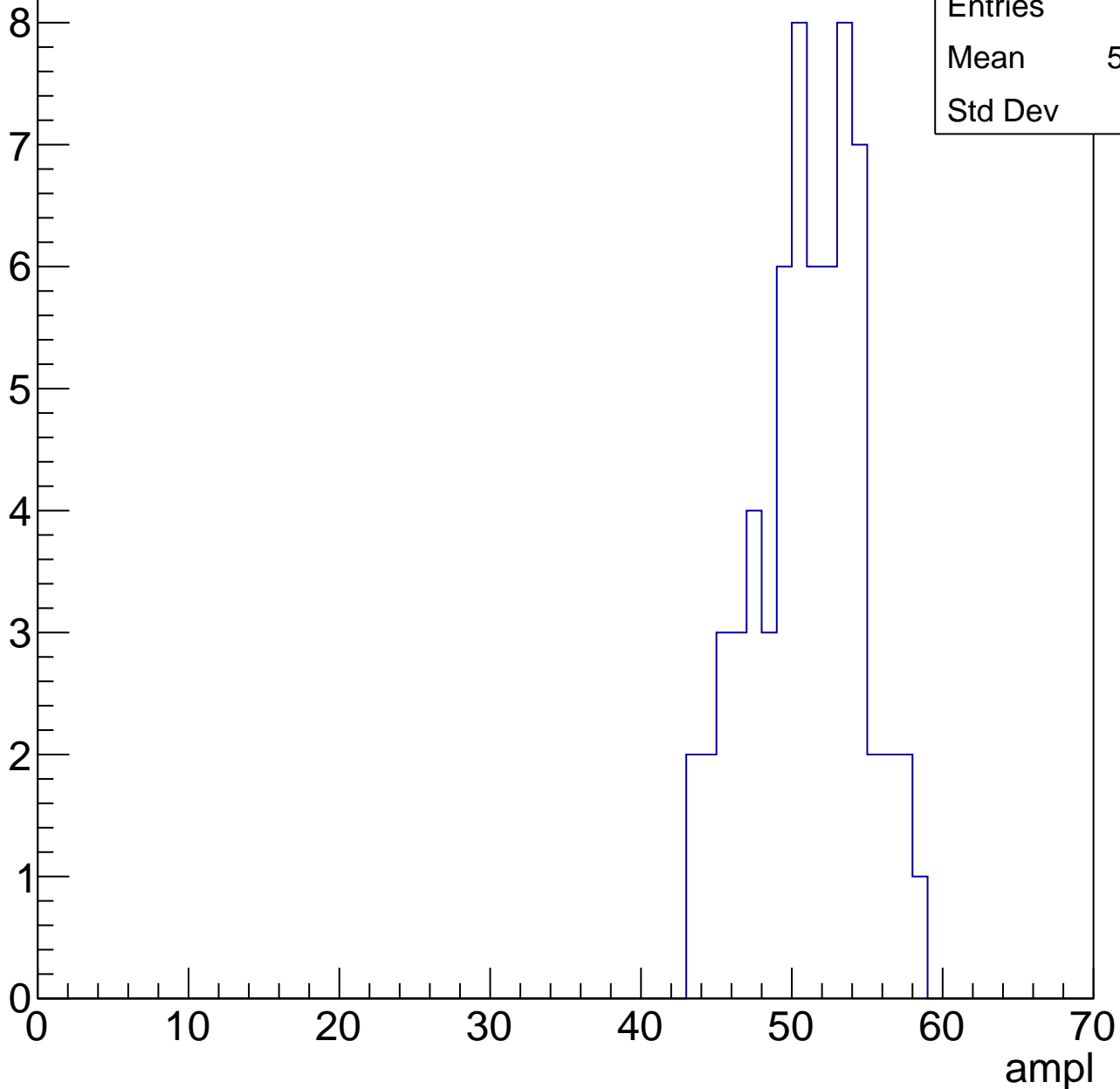


# B1L101S, U18-ch102, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

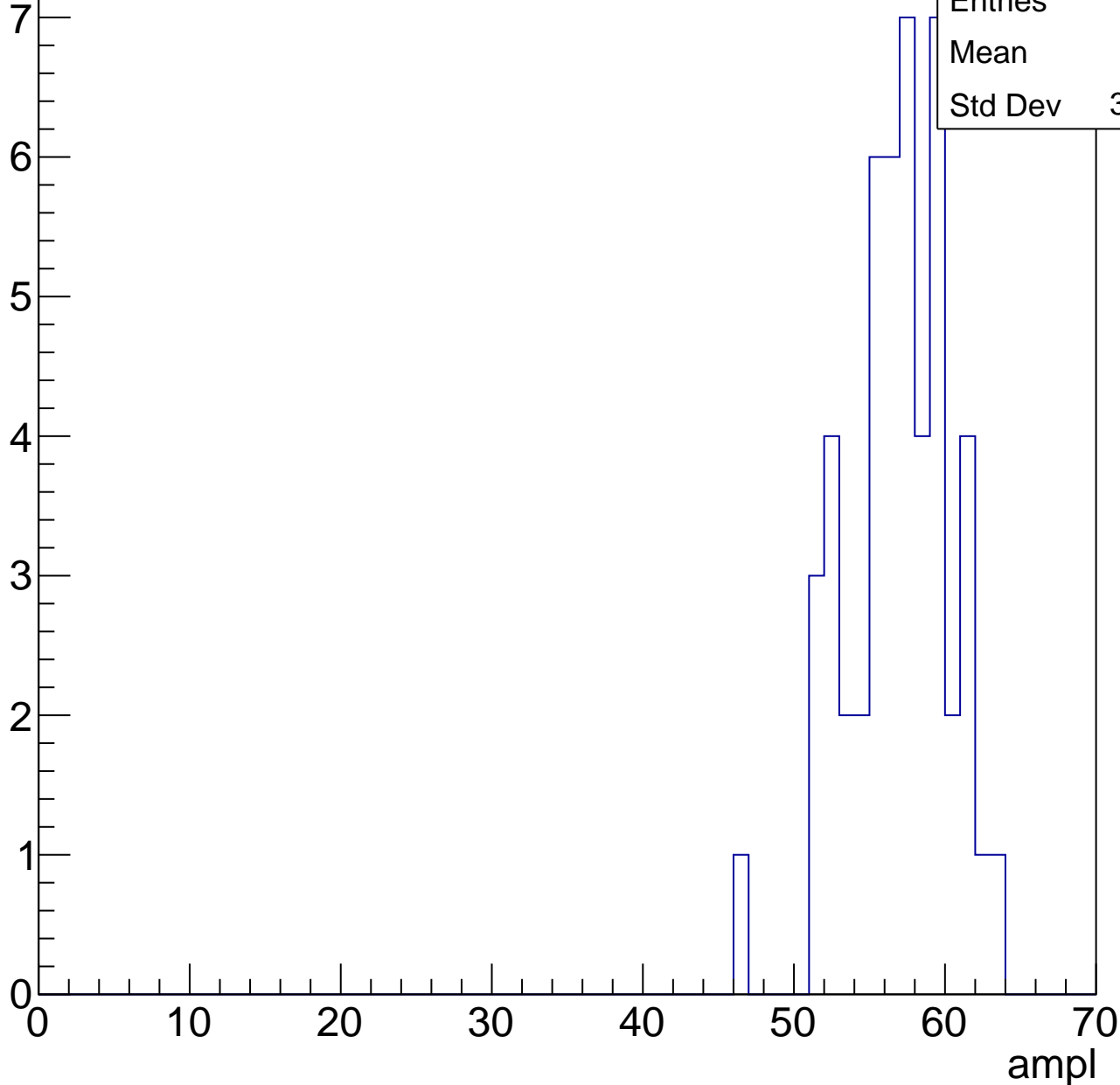
Entries	65
Mean	50.57
Std Dev	3.56



# B1L101S, U18-ch102, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

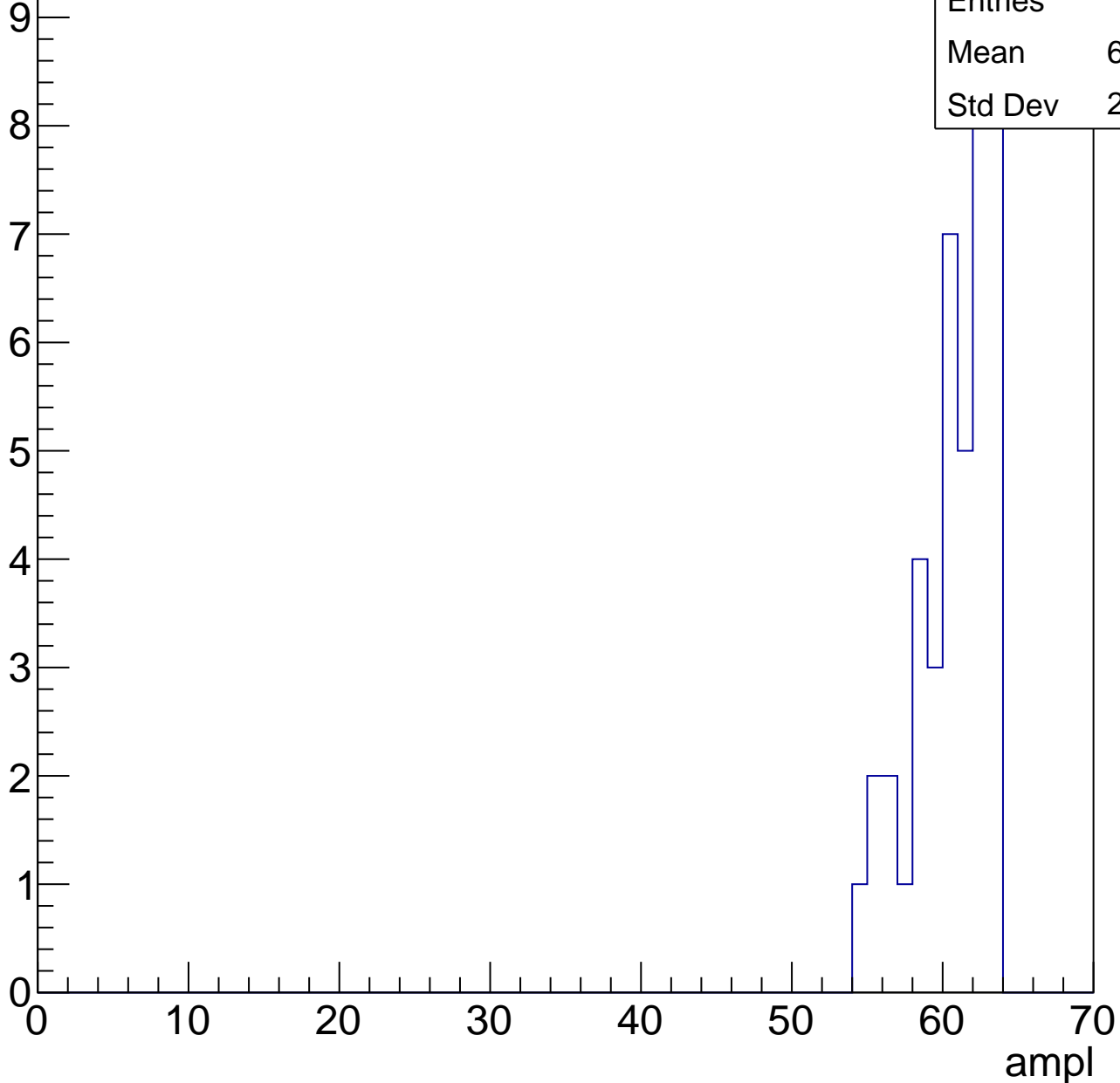


# B1L101S, U18-ch102, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

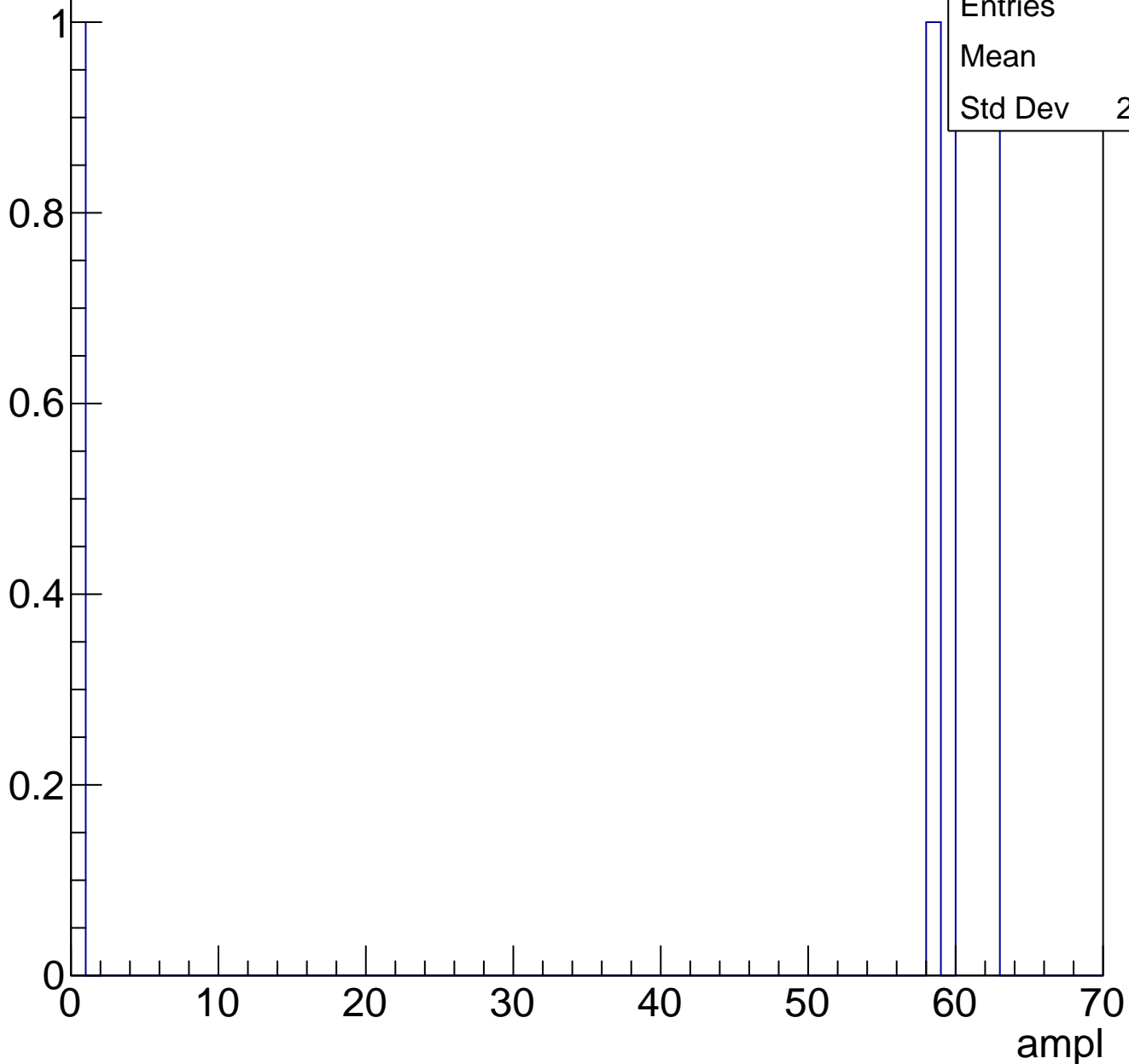
Entries	42
Mean	60.24
Std Dev	2.496



# B1L101S, U18-ch102, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch102, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U18-ch103, adc0

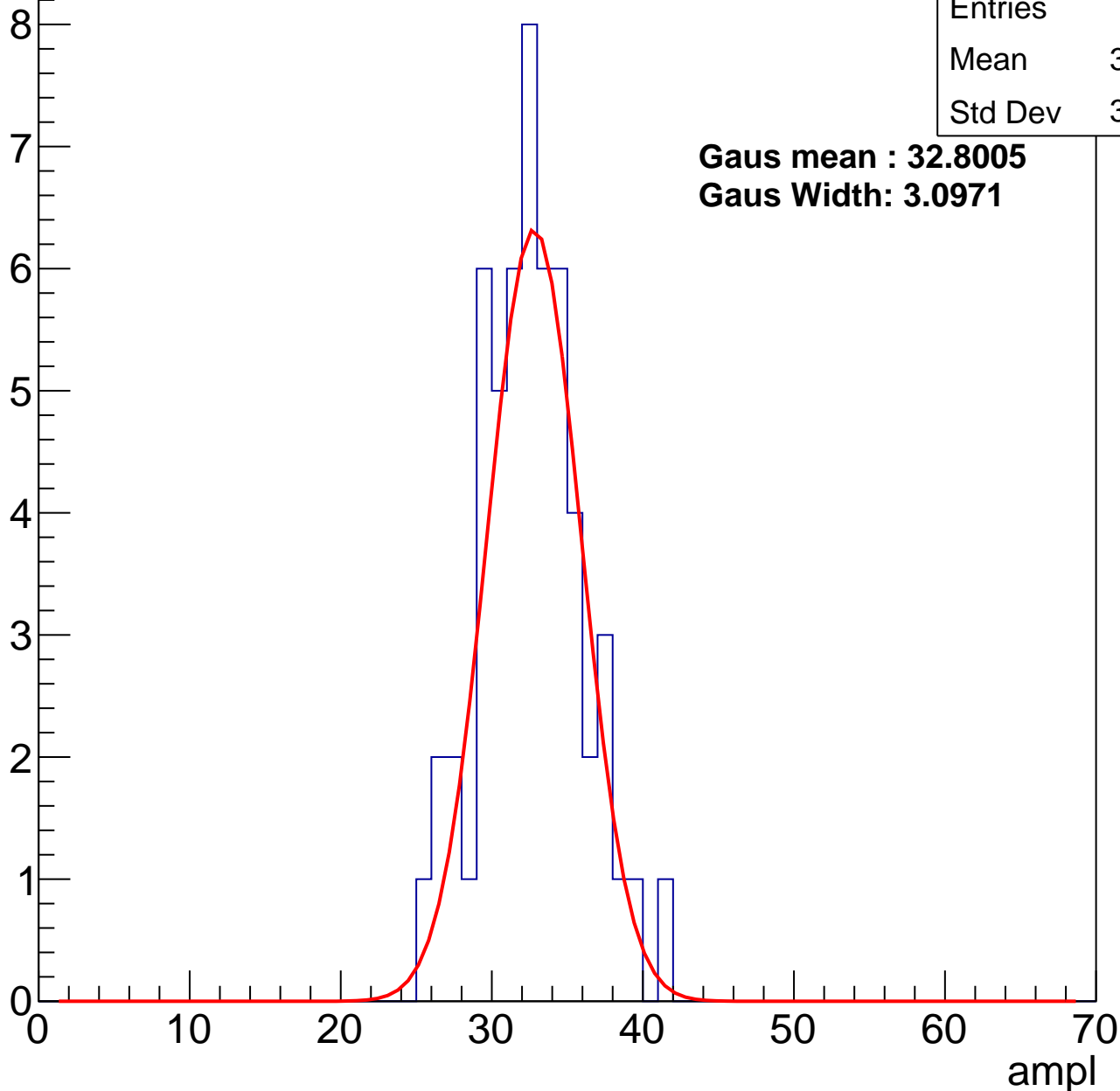
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	32.15
Std Dev	3.316

**Gaus mean : 32.8005**

**Gaus Width: 3.0971**



# B1L101S, U18-ch103, adc1

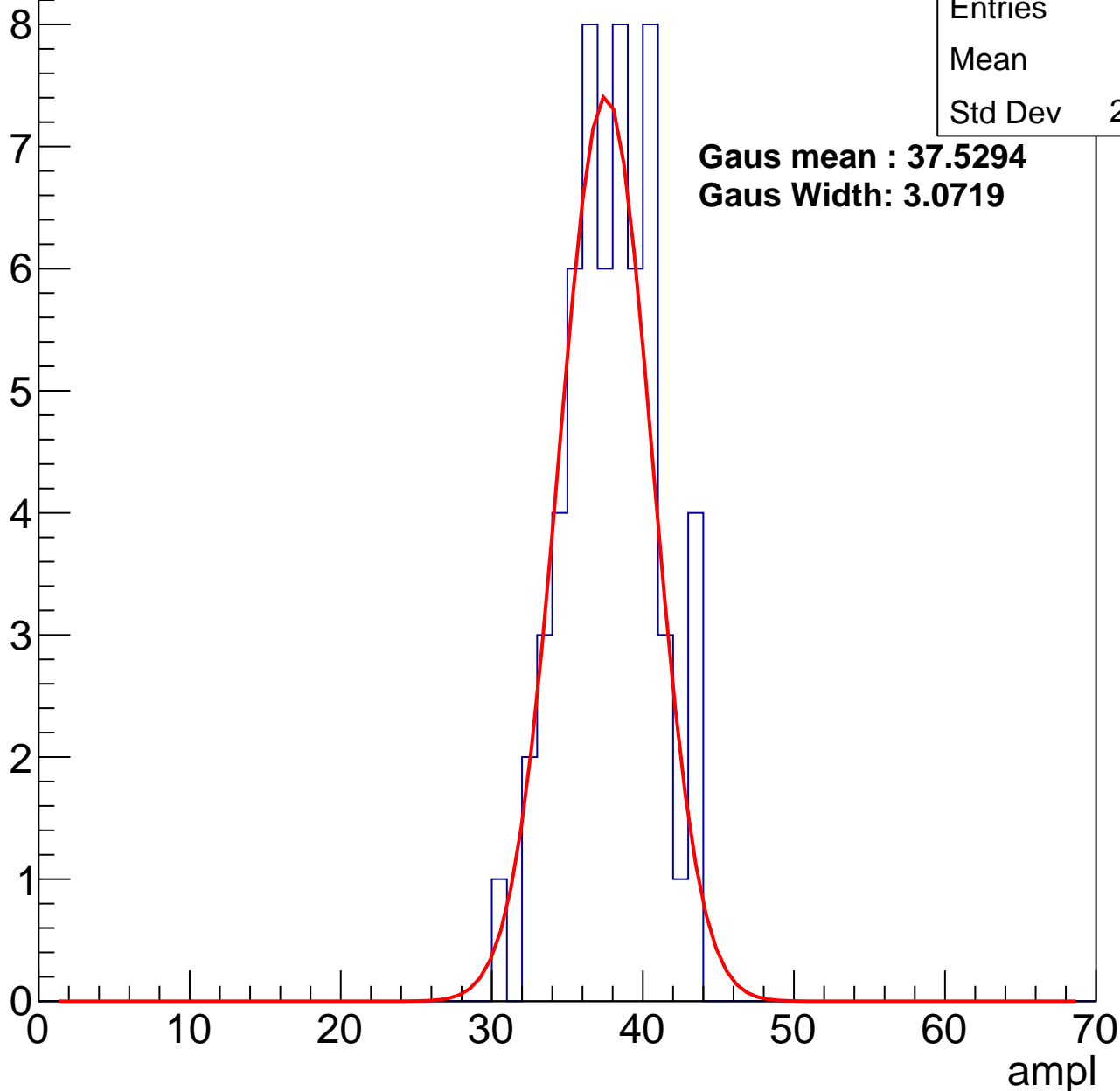
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	37.4
Std Dev	2.962

**Gaus mean : 37.5294**

**Gaus Width: 3.0719**



# B1L101S, U18-ch103, adc2

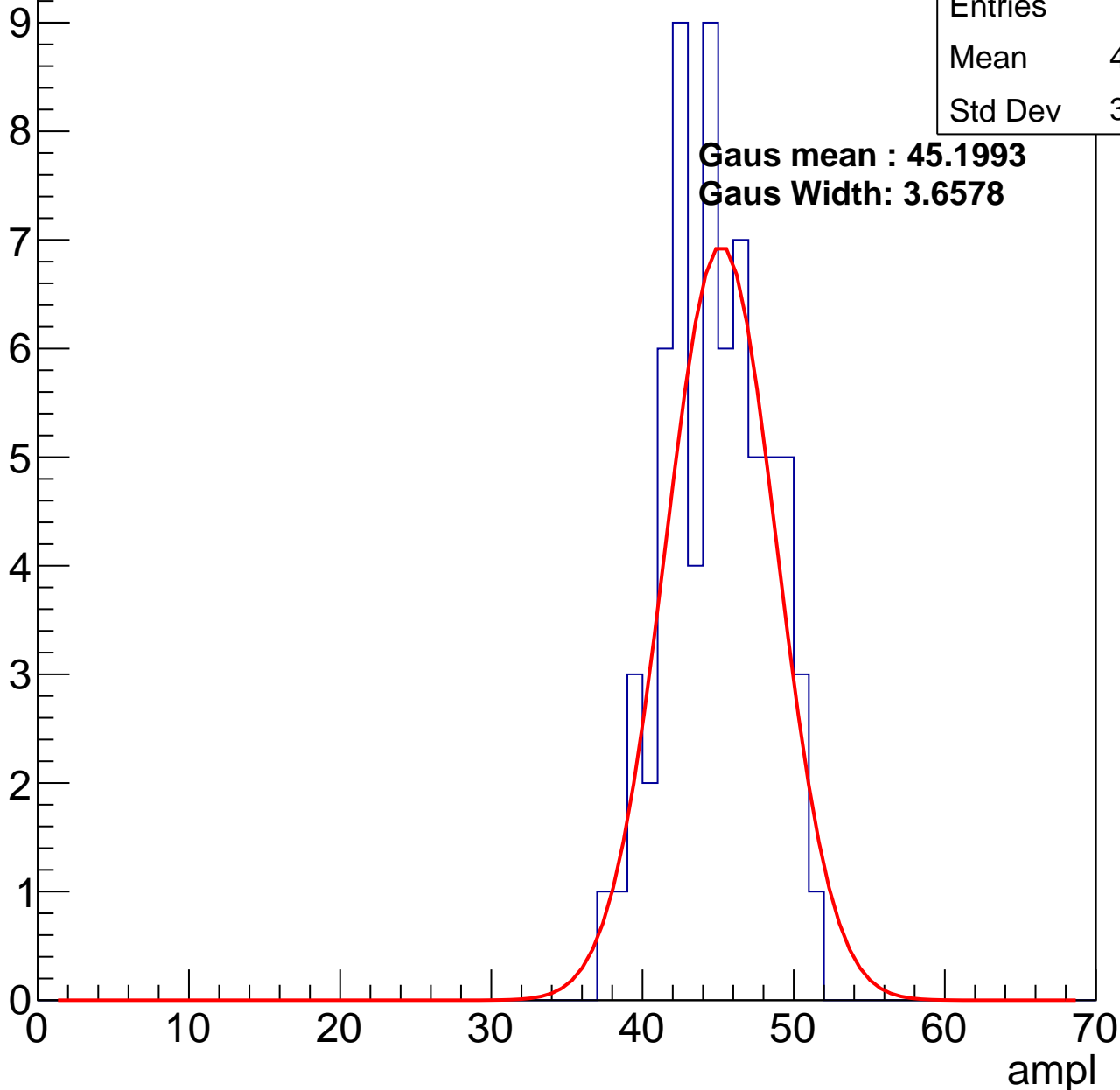
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	44.43
Std Dev	3.265

**Gaus mean : 45.1993**

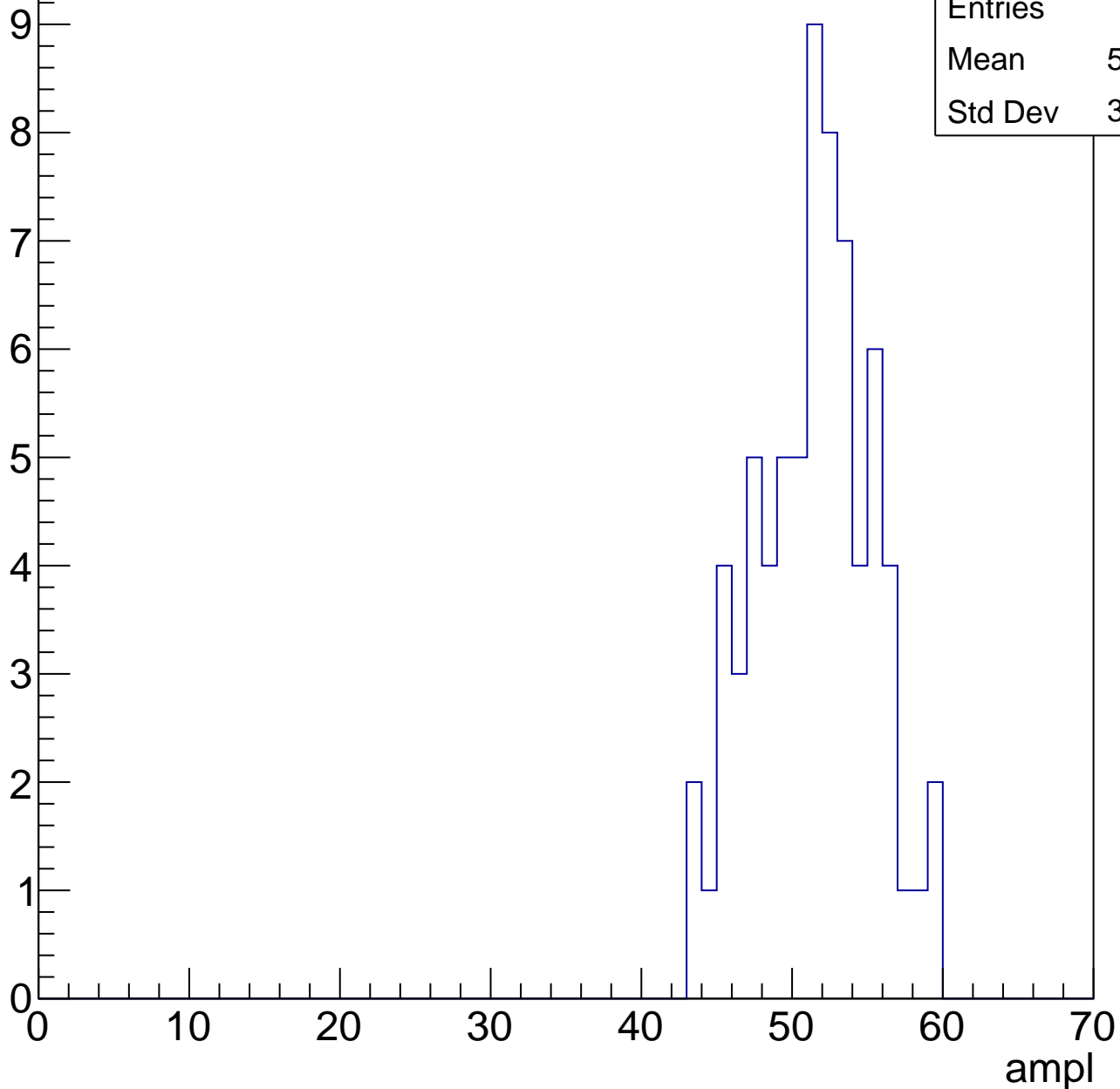
**Gaus Width: 3.6578**



# B1L101S, U18-ch103, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



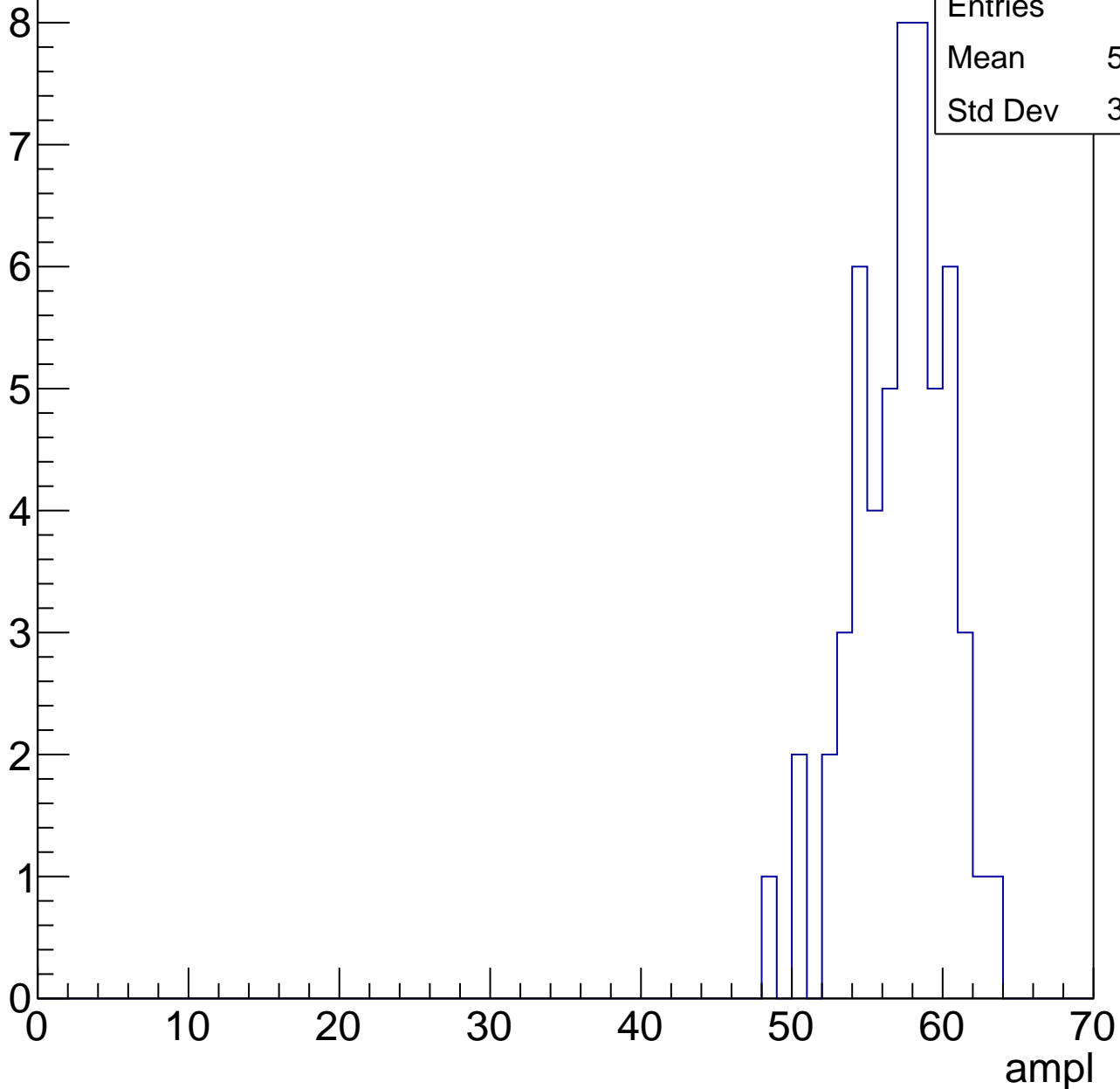
Entries	71
Mean	50.97
Std Dev	3.786

# B1L101S, U18-ch103, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	56.69
Std Dev	3.127

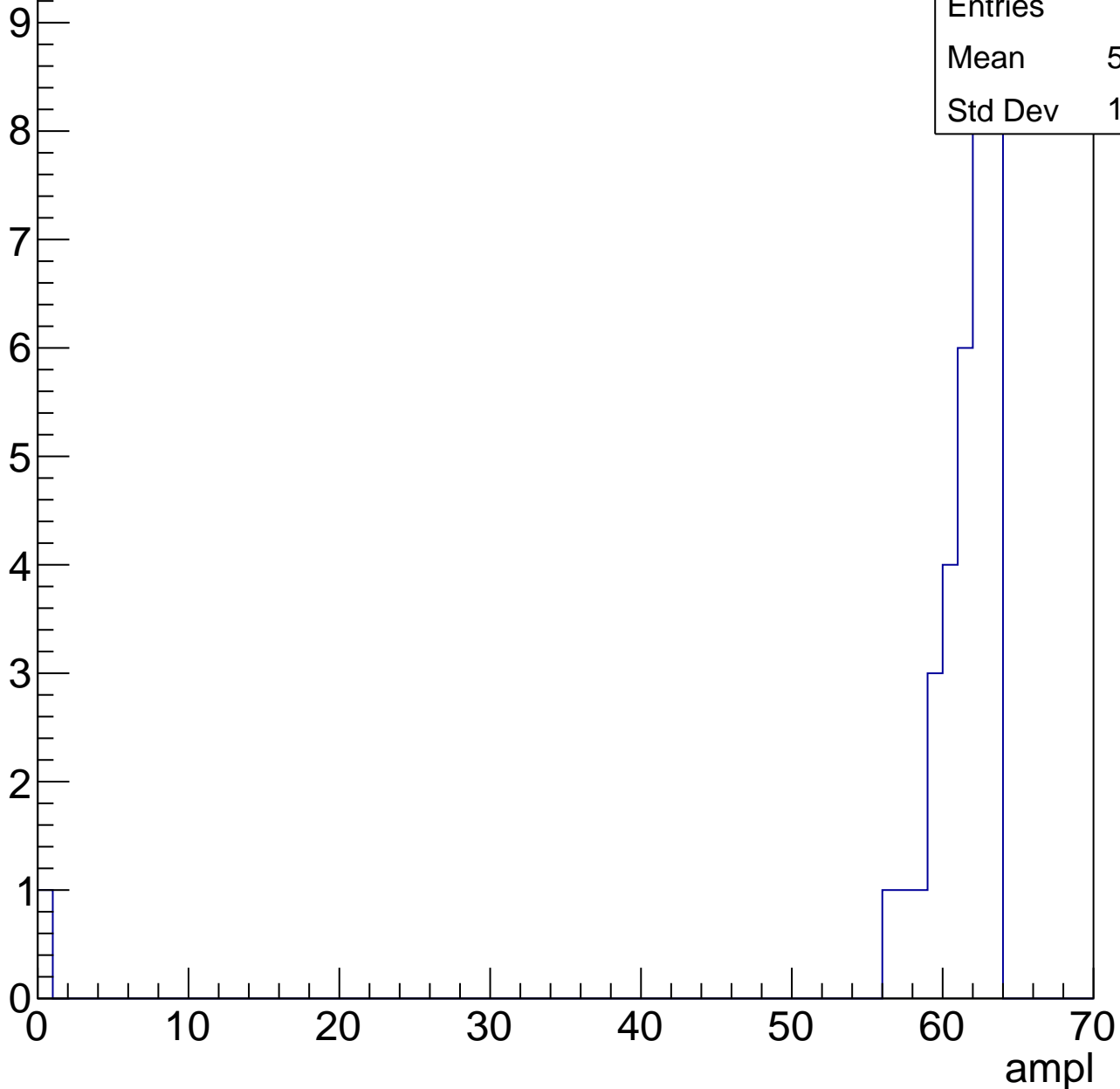


# B1L101S, U18-ch103, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

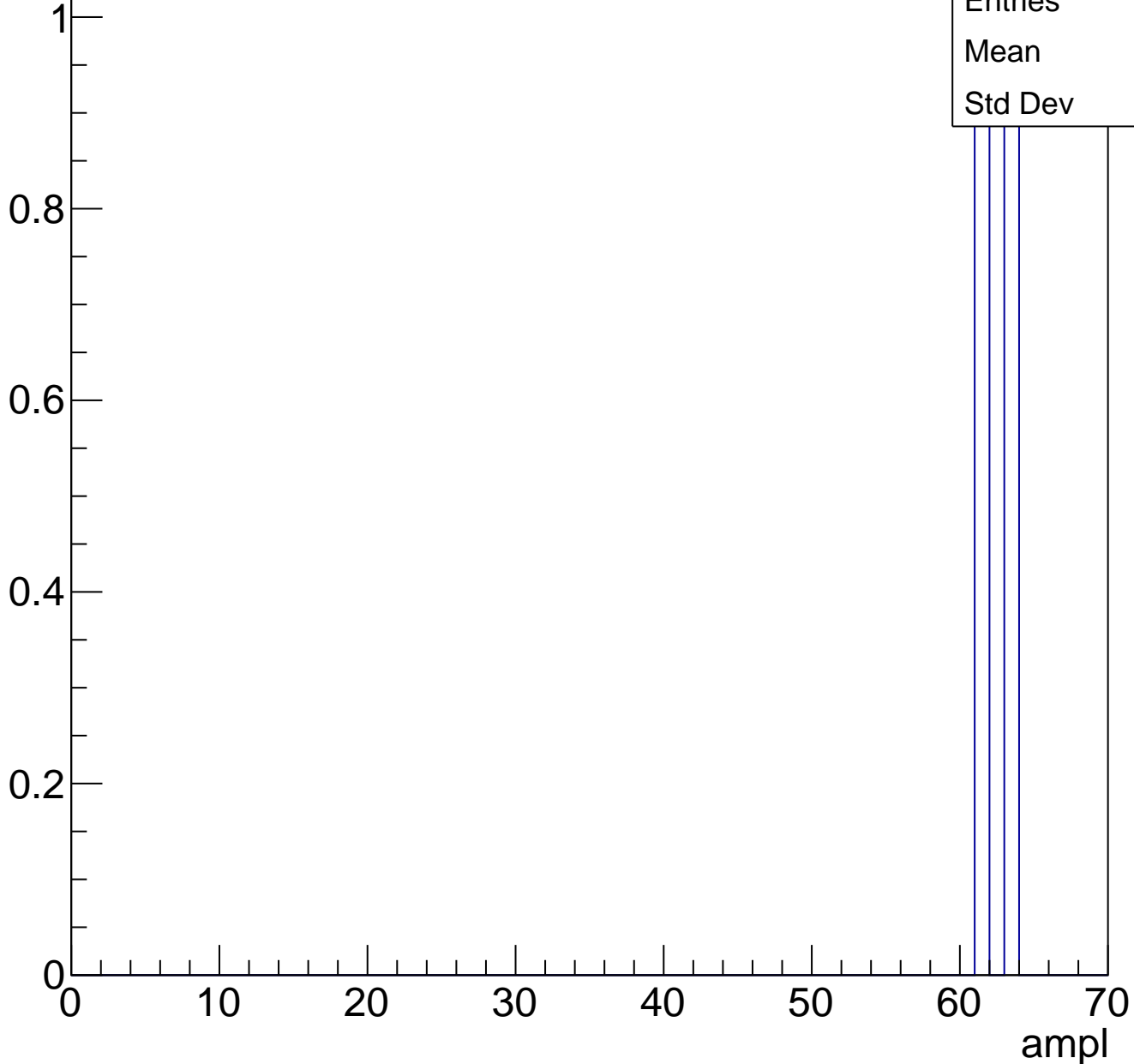
Entries	34
Mean	59.29
Std Dev	10.47



# B1L101S, U18-ch103, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch103, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch104, adc0

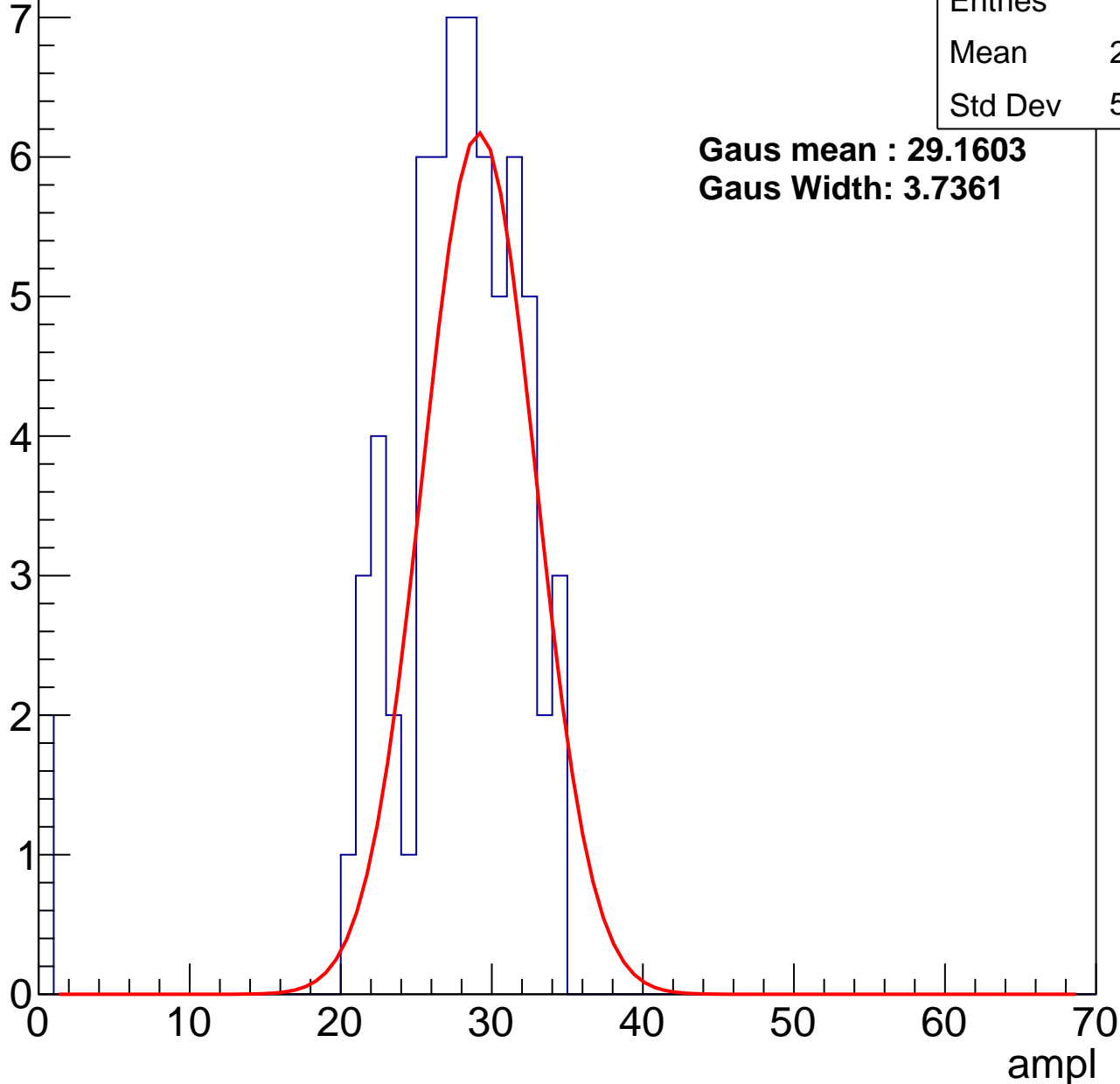
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	26.82
Std Dev	5.903

**Gaus mean : 29.1603**

**Gaus Width: 3.7361**



# B1L101S, U18-ch104, adc1

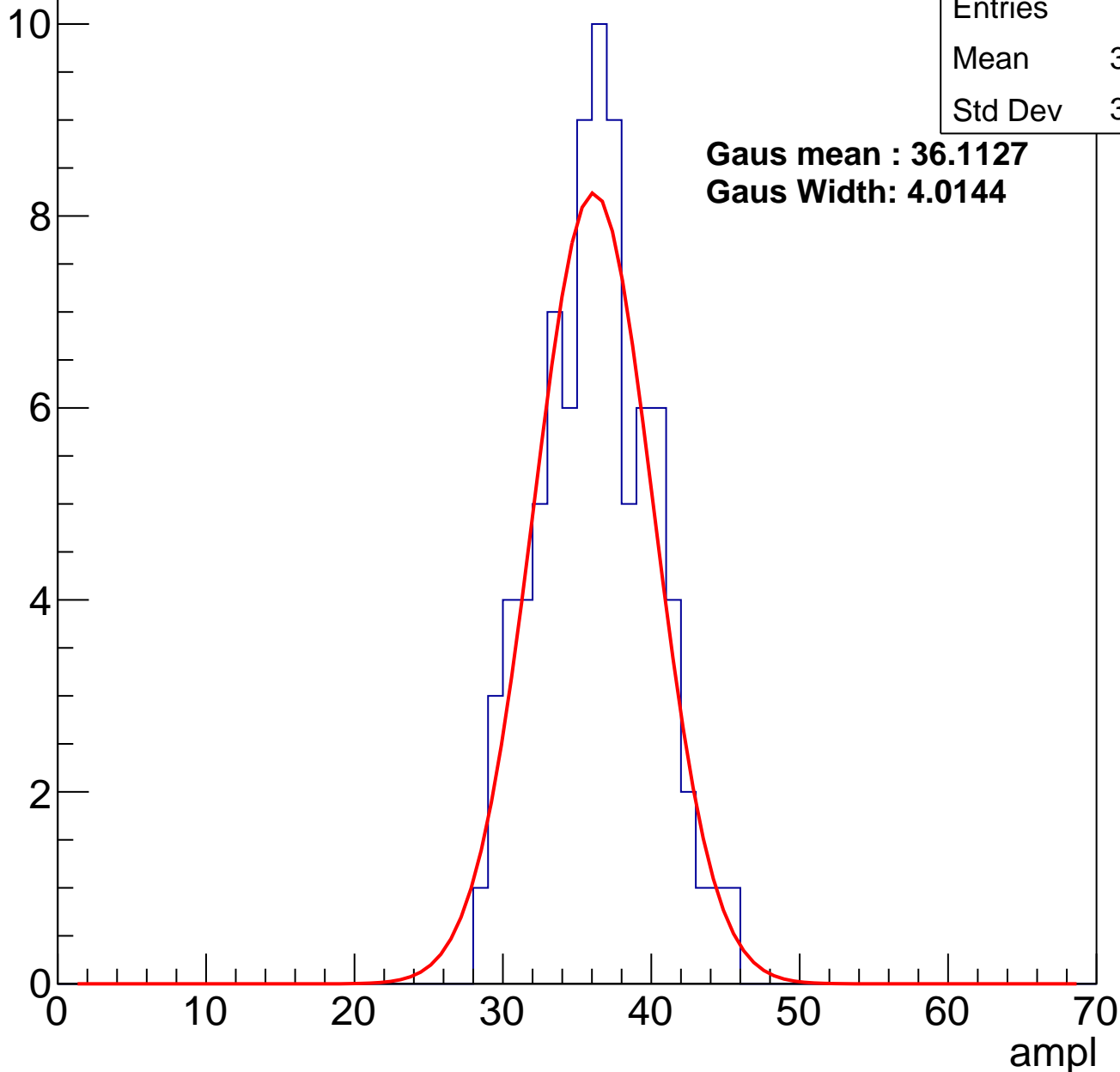
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	84
Mean	35.79
Std Dev	3.736

**Gaus mean : 36.1127**

**Gaus Width: 4.0144**

Entry



# B1L101S, U18-ch104, adc2

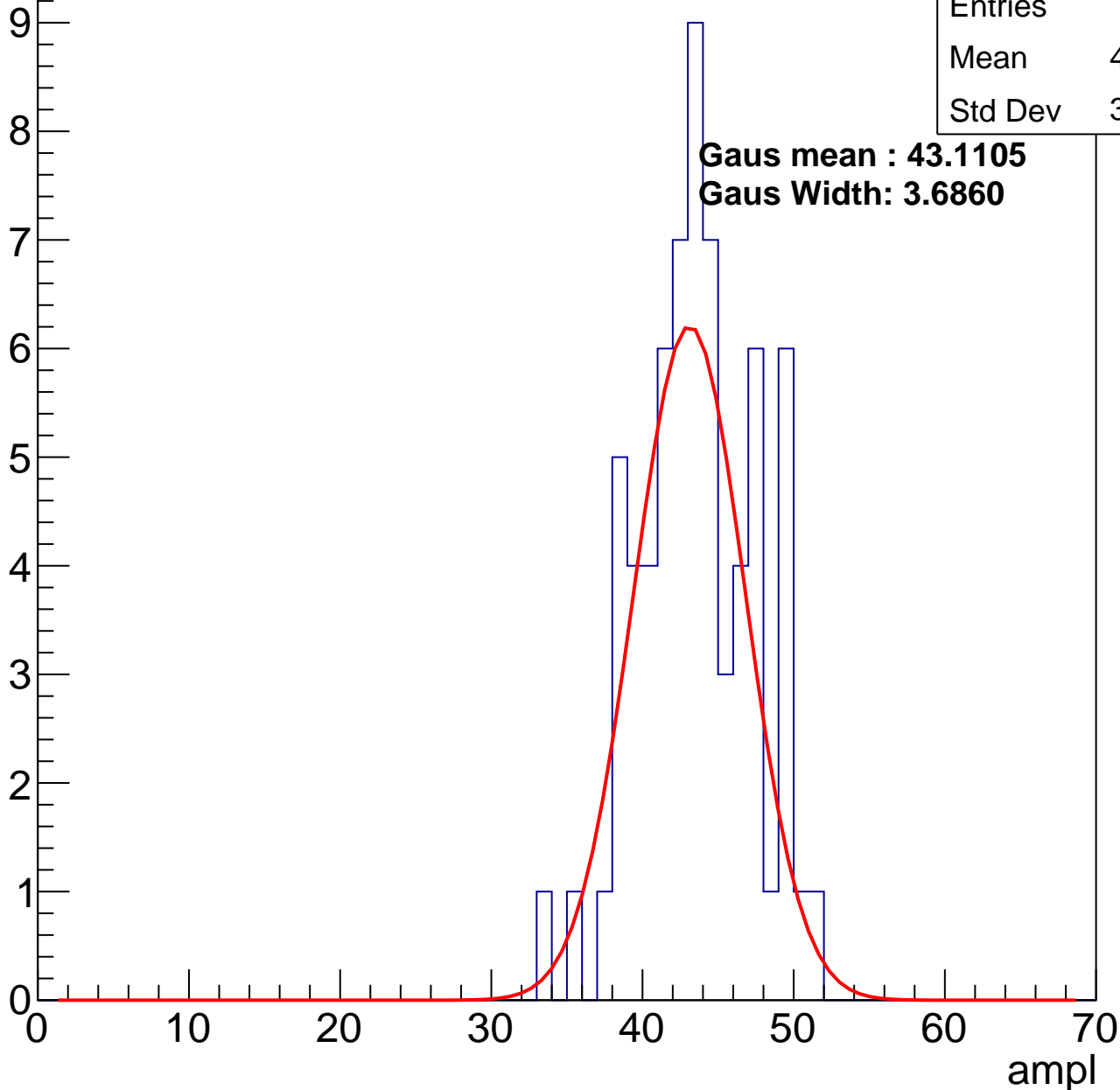
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	43.13
Std Dev	3.785

**Gaus mean : 43.1105**

**Gaus Width: 3.6860**

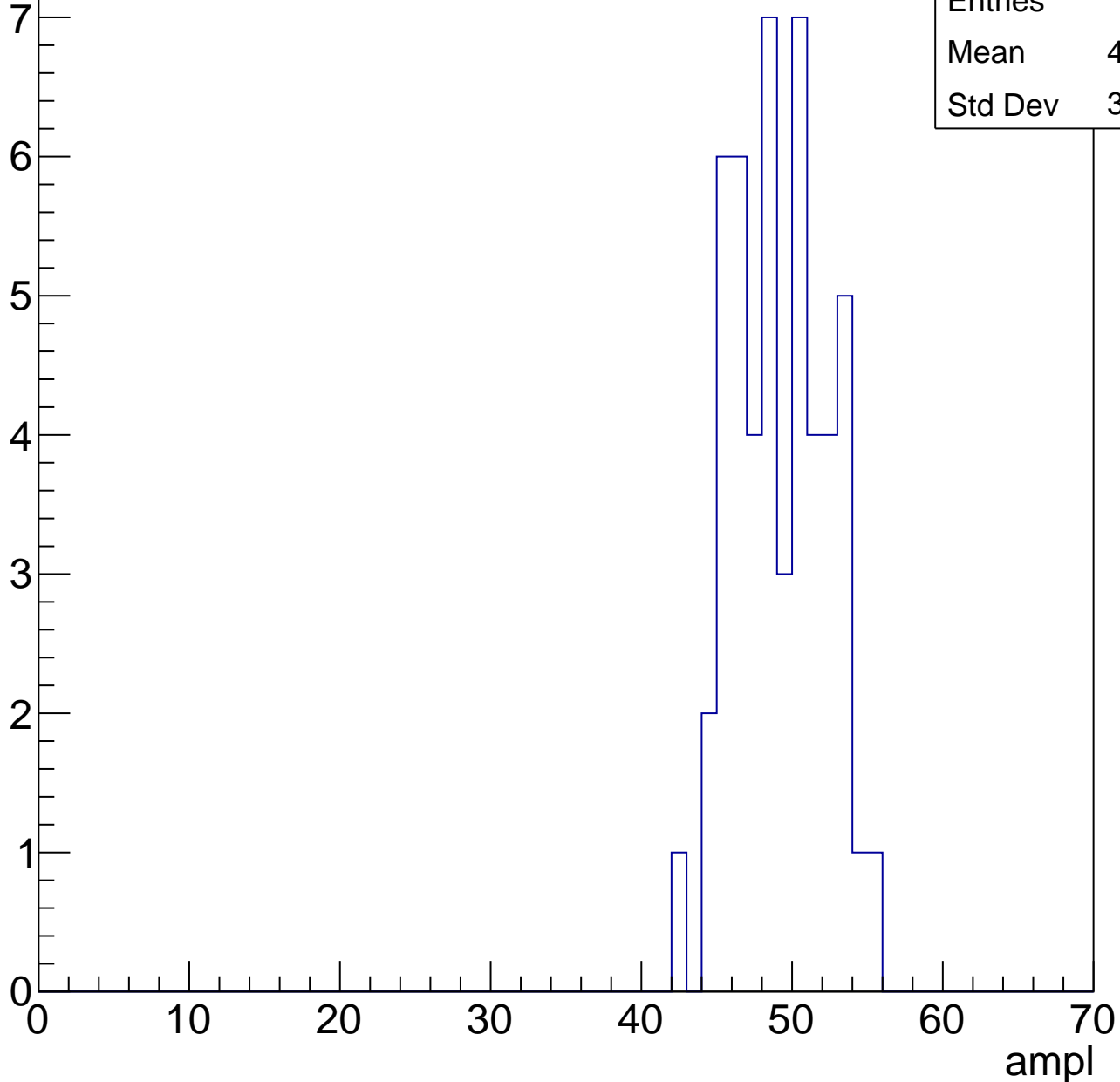


# B1L101S, U18-ch104, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	48.69
Std Dev	3.026

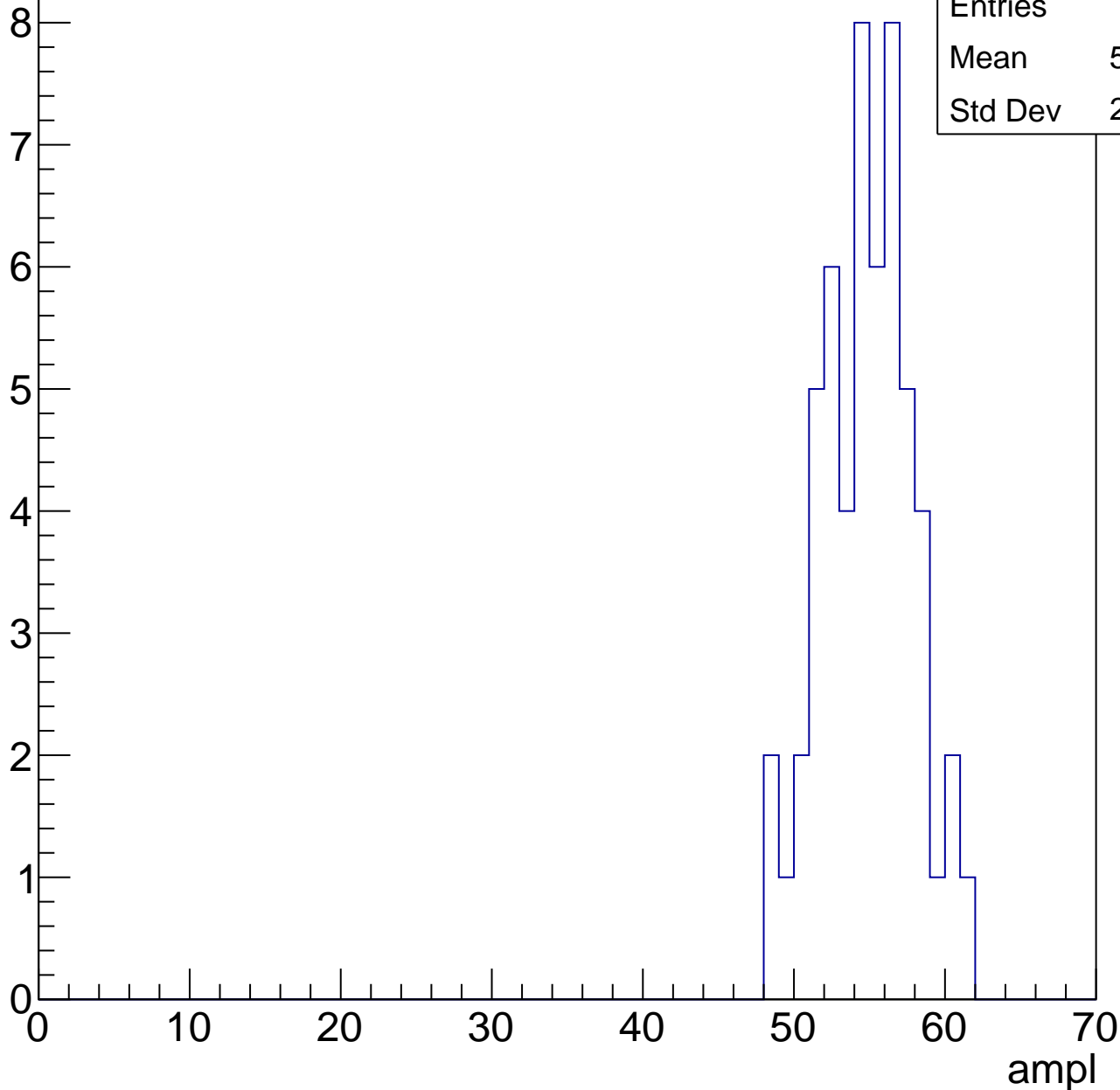


# B1L101S, U18-ch104, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	54.38
Std Dev	2.976

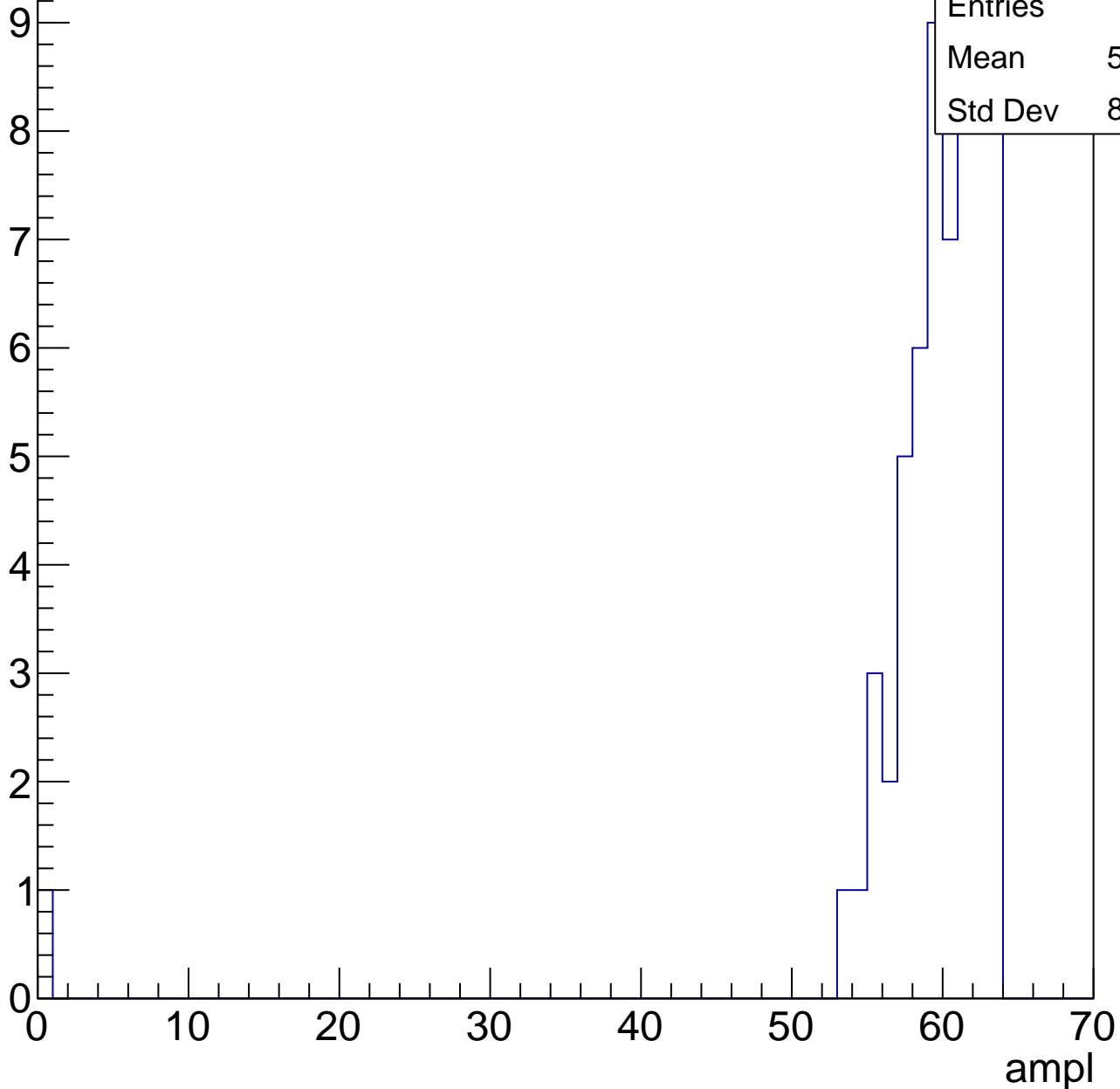


# B1L101S, U18-ch104, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

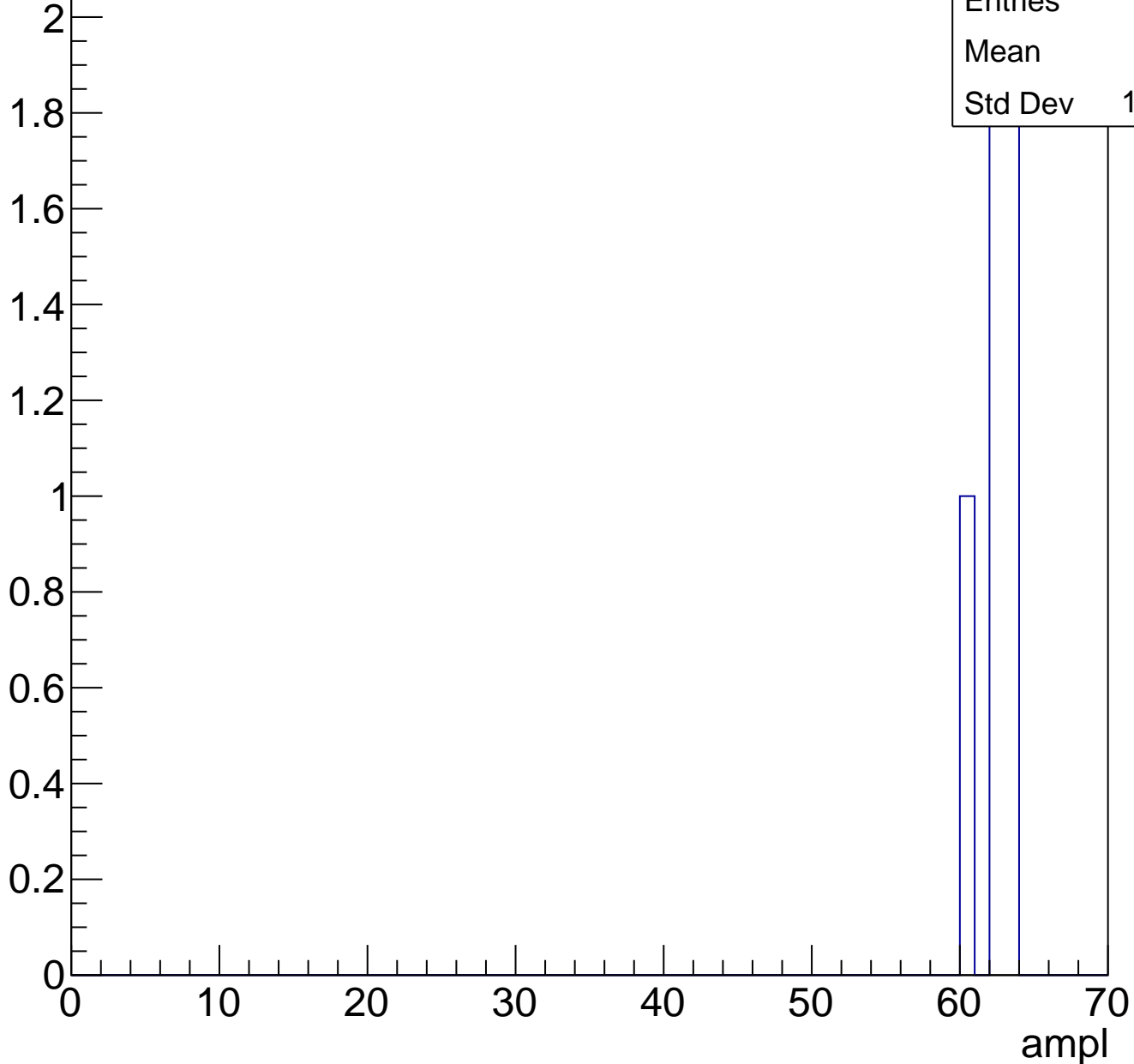
Entries	60
Mean	58.62
Std Dev	8.029



# B1L101S, U18-ch104, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch104, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U18-ch105, adc0

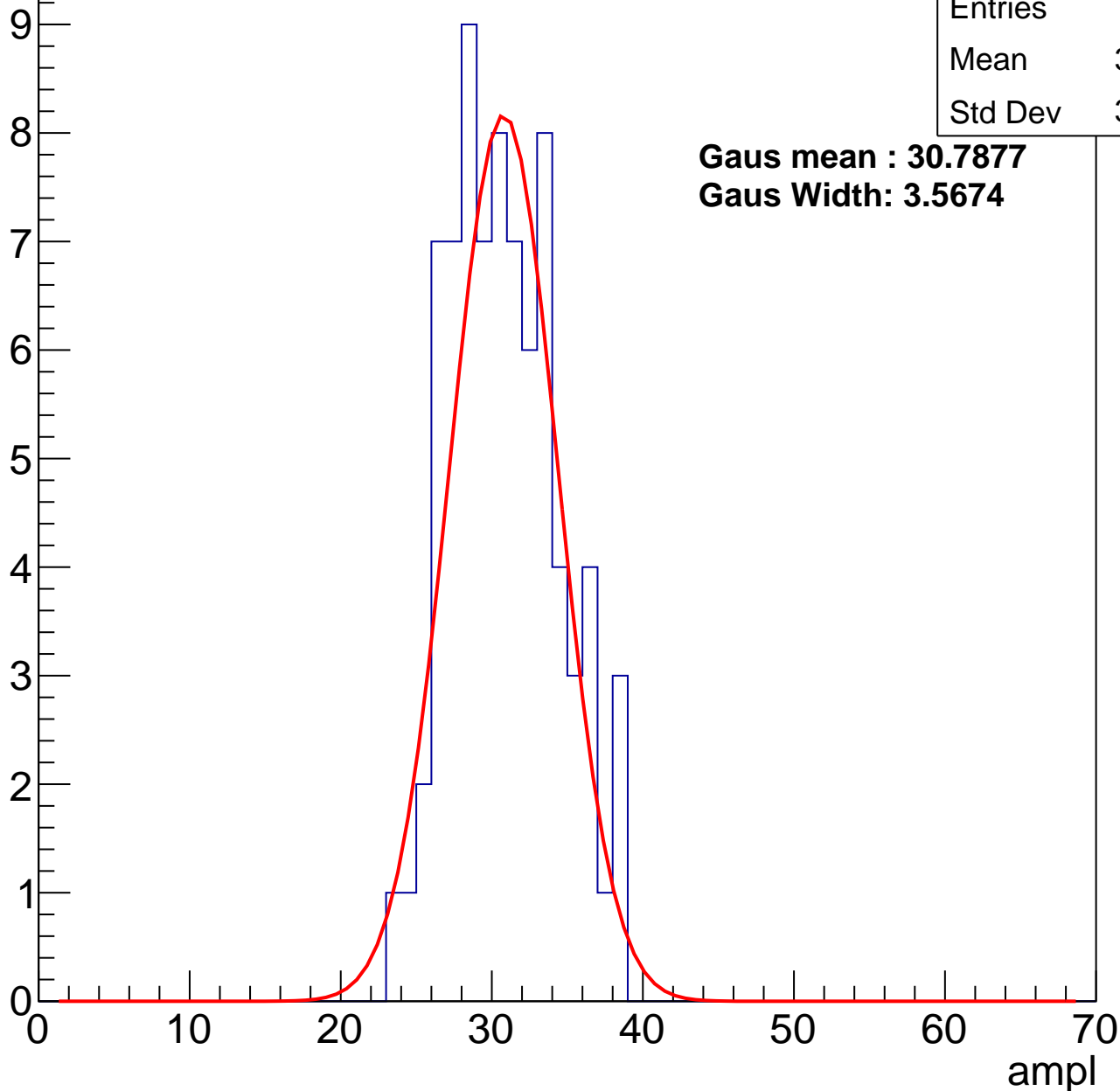
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	78
Mean	30.41
Std Dev	3.521

**Gaus mean : 30.7877**

**Gaus Width: 3.5674**



# B1L101S, U18-ch105, adc1

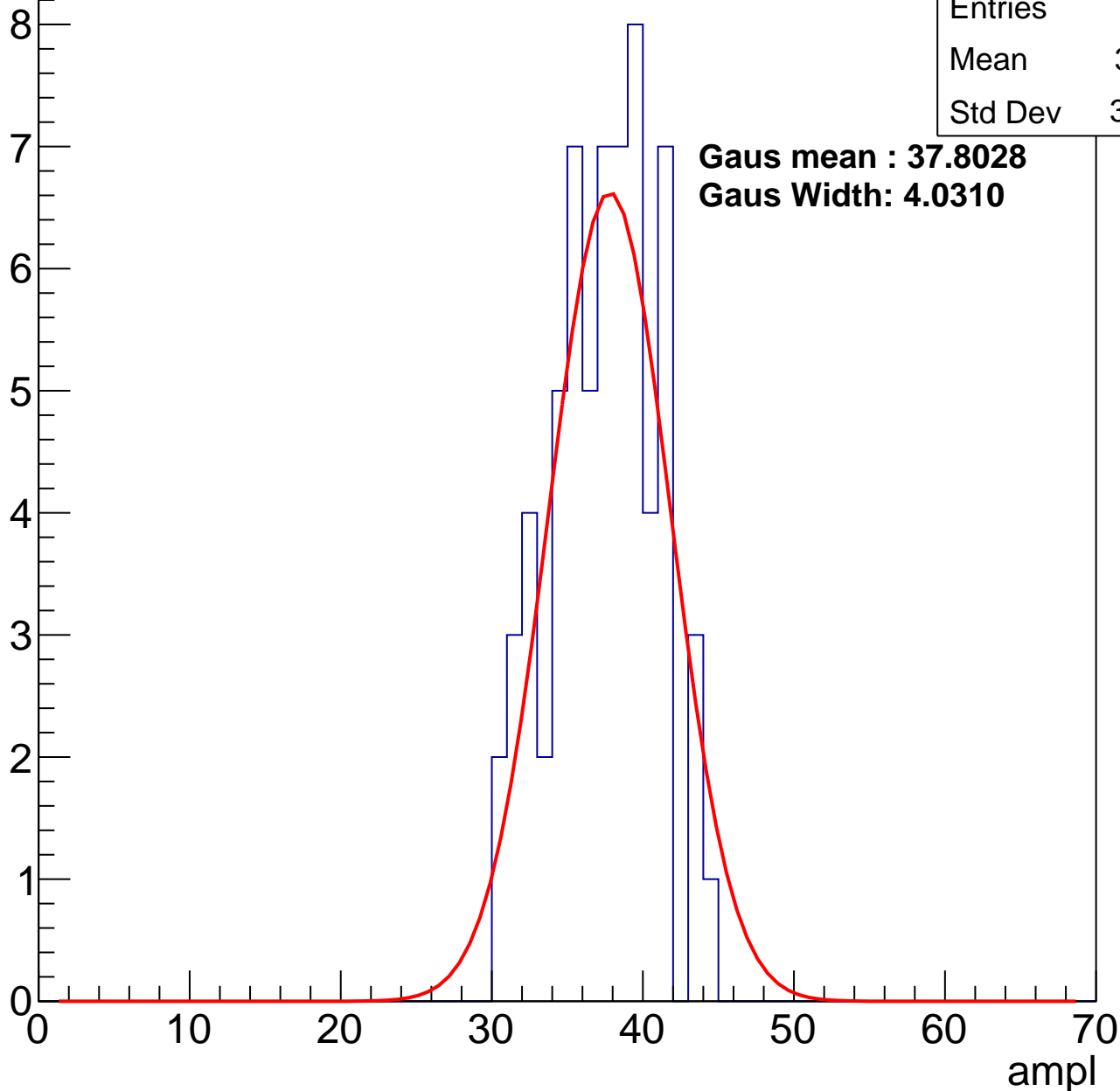
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	36.91
Std Dev	3.418

**Gaus mean : 37.8028**

**Gaus Width: 4.0310**



# B1L101S, U18-ch105, adc2

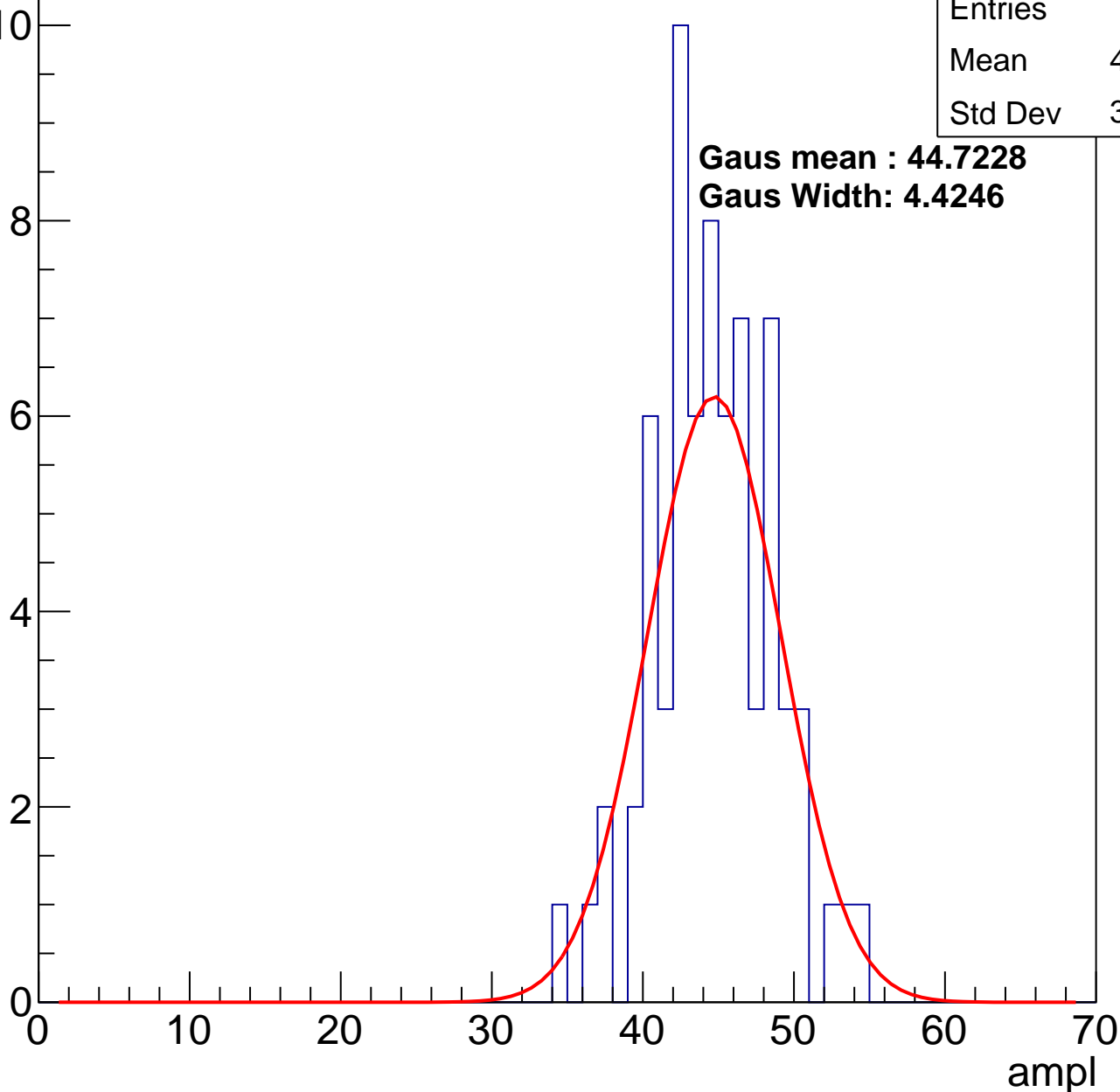
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	44.23
Std Dev	3.897

**Gaus mean : 44.7228**

**Gaus Width: 4.4246**

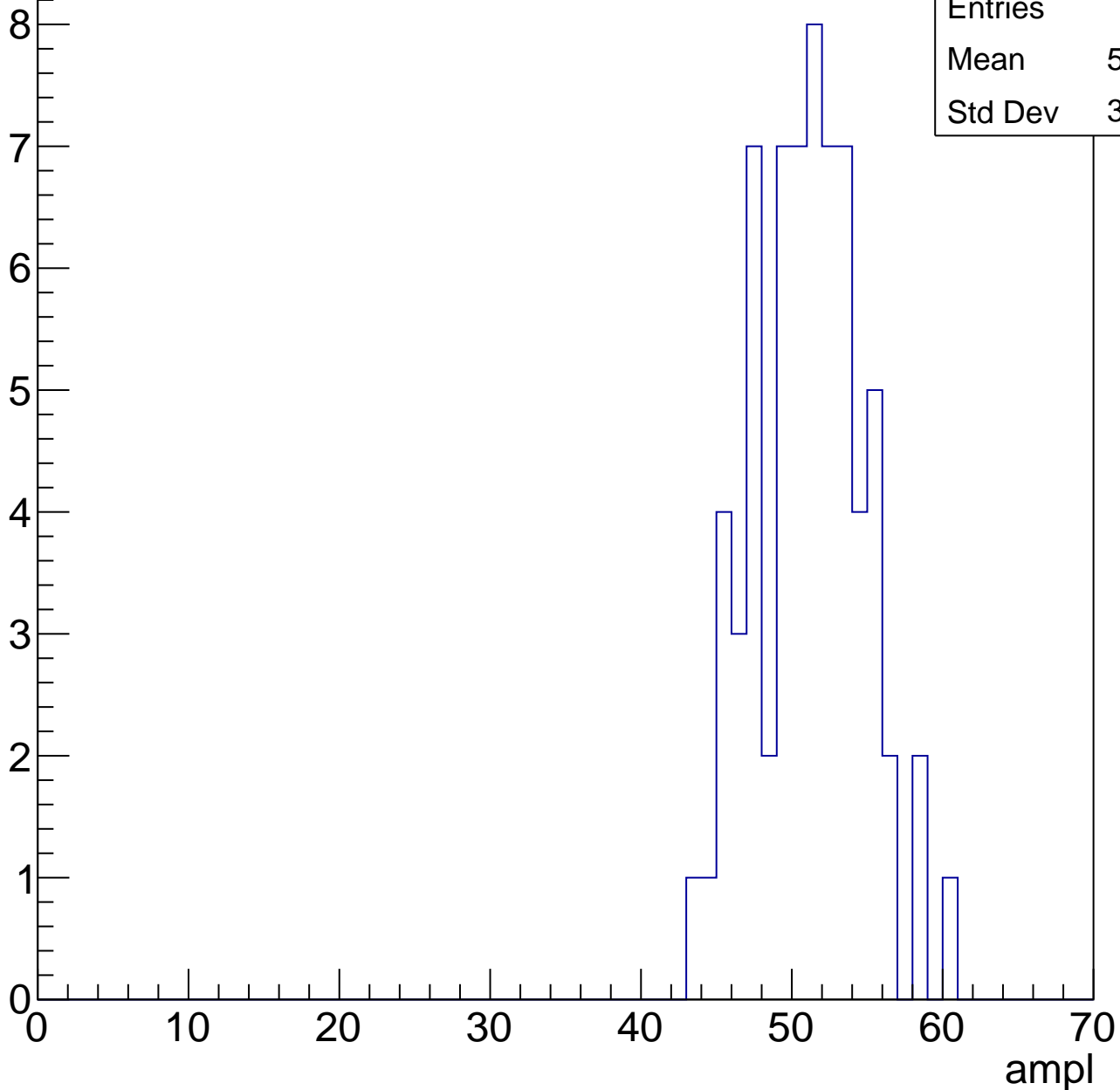


# B1L101S, U18-ch105, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	50.66
Std Dev	3.575

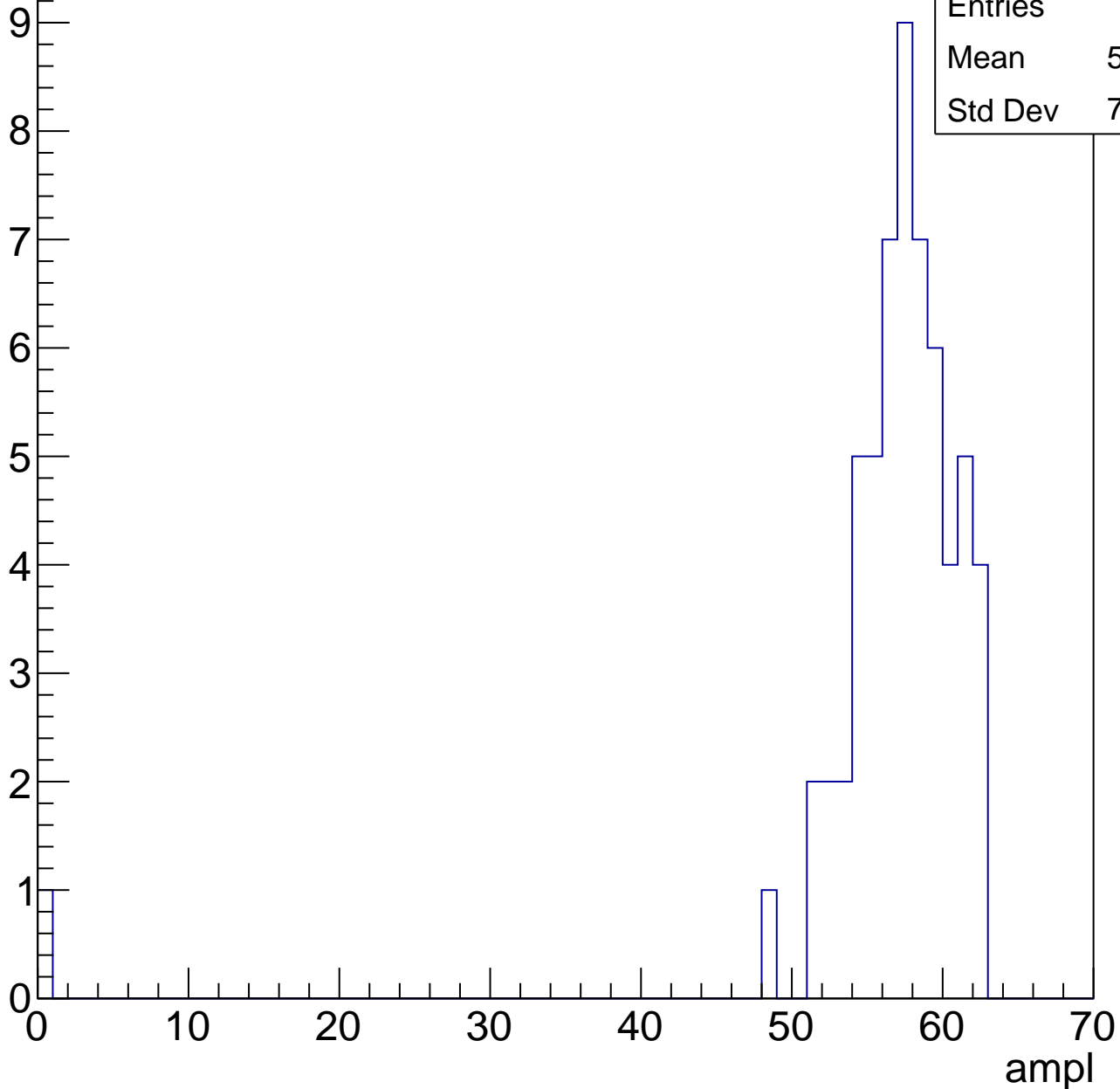


# B1L101S, U18-ch105, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	56.05
Std Dev	7.904

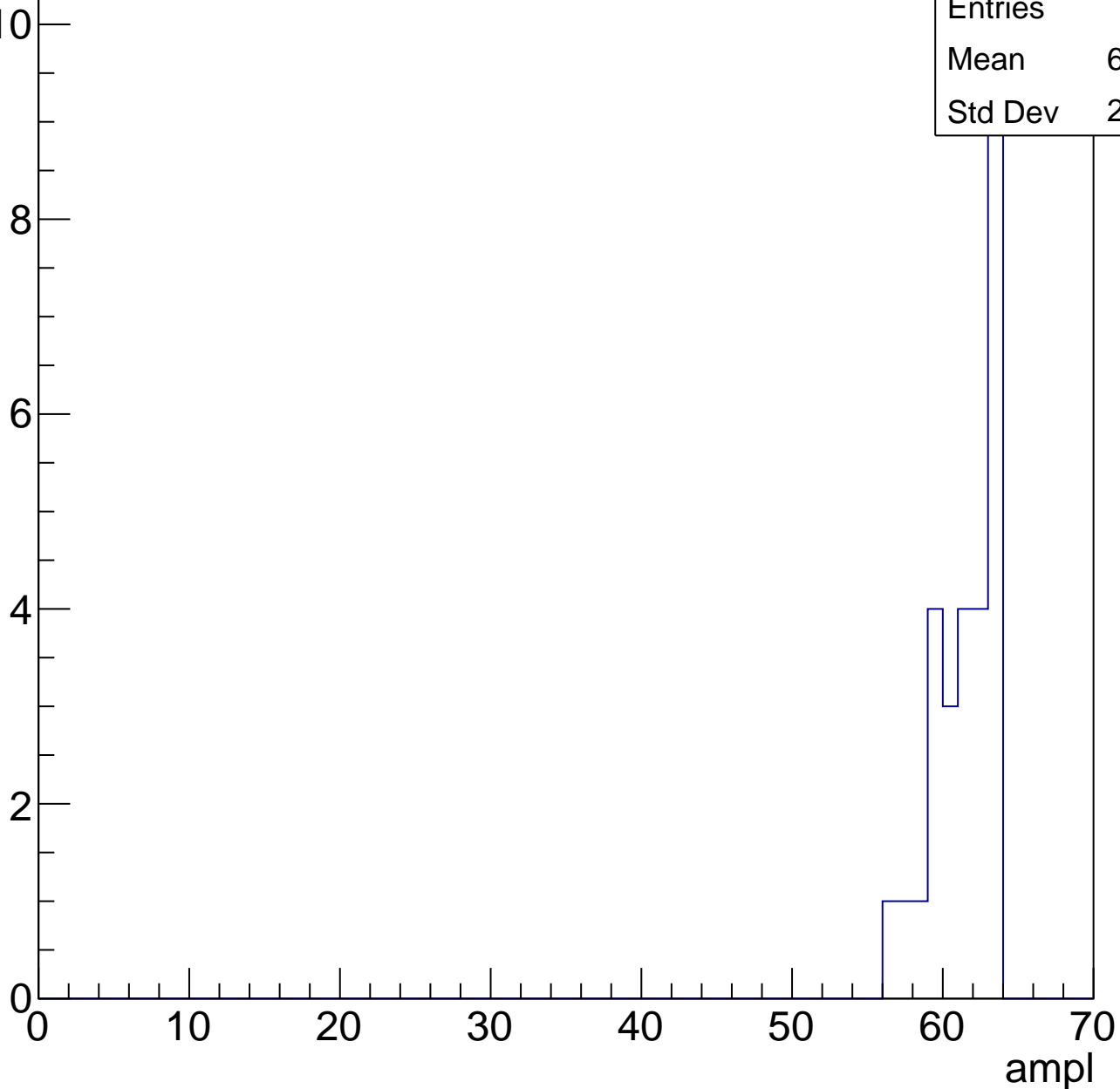


# B1L101S, U18-ch105, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	28
Mean	61.04
Std Dev	2.009



# B1L101S, U18-ch105, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	61
Std Dev	0.8944

ampl

0 10 20 30 40 50 60 70



# B1L101S, U18-ch105, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	11
Std Dev	11

# B1L101S, U18-ch106, adc0

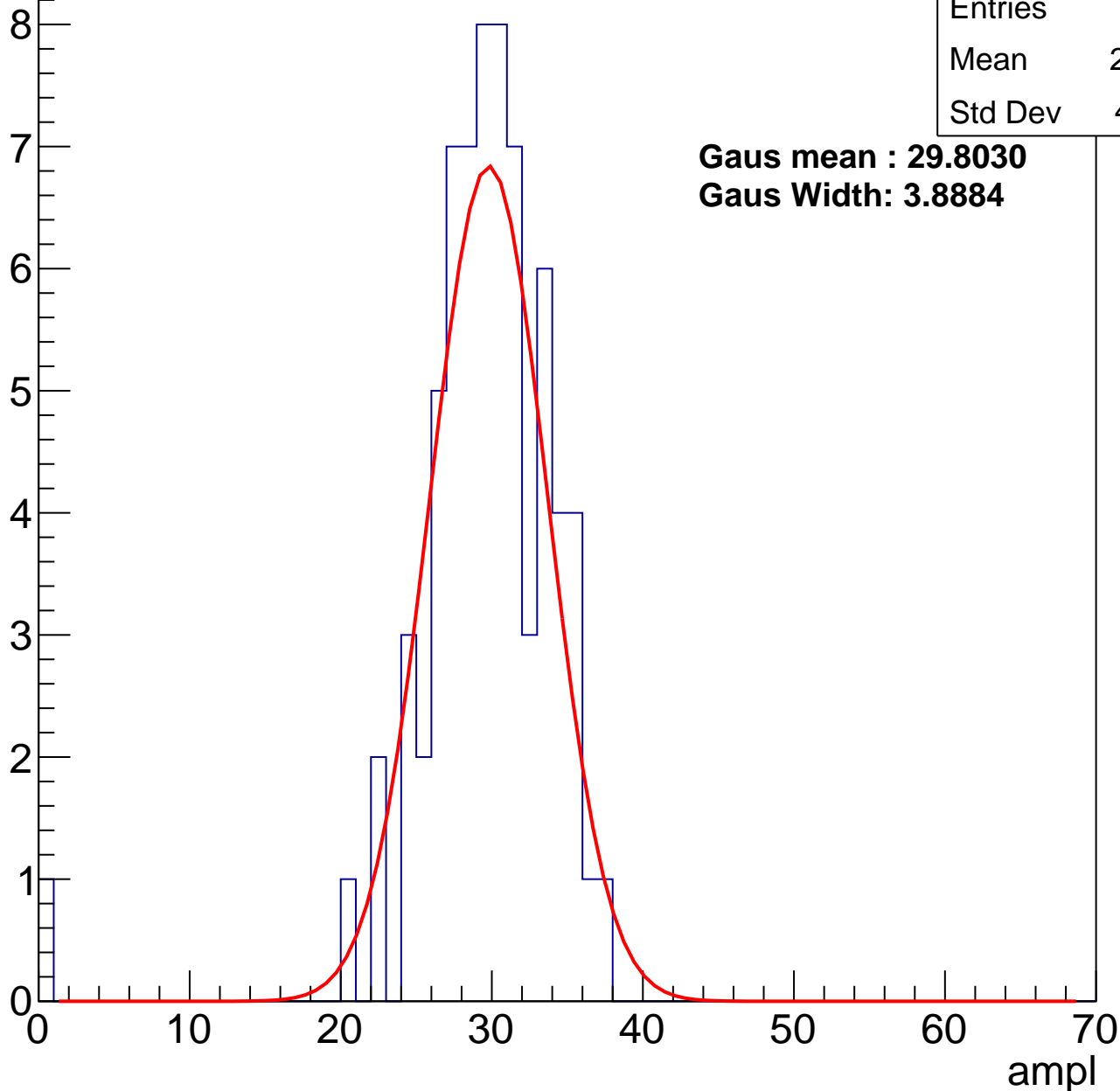
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	29.04
Std Dev	4.961

**Gaus mean : 29.8030**

**Gaus Width: 3.8884**



# B1L101S, U18-ch106, adc1

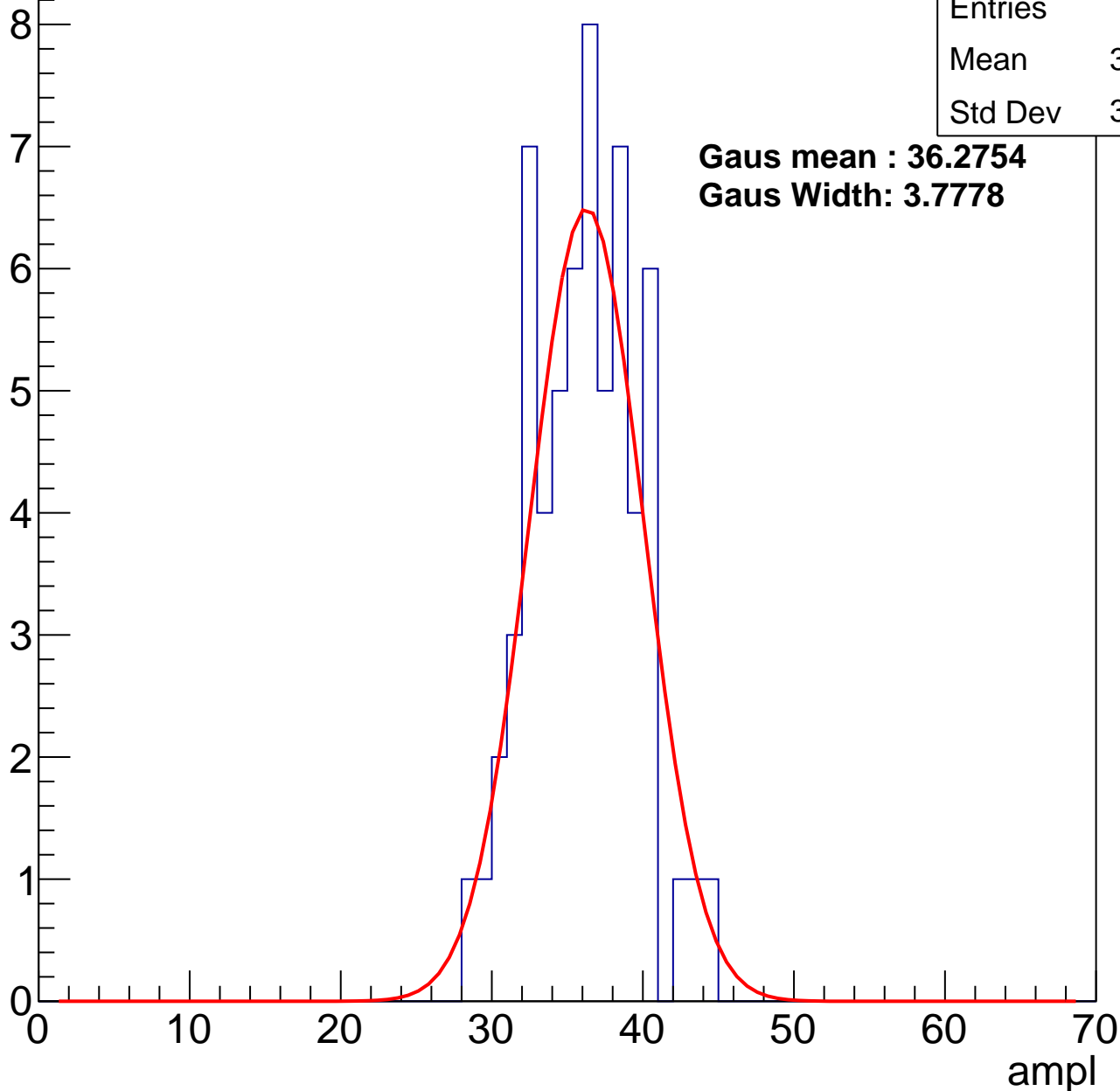
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	35.65
Std Dev	3.455

**Gaus mean : 36.2754**

**Gaus Width: 3.7778**



# B1L101S, U18-ch106, adc2

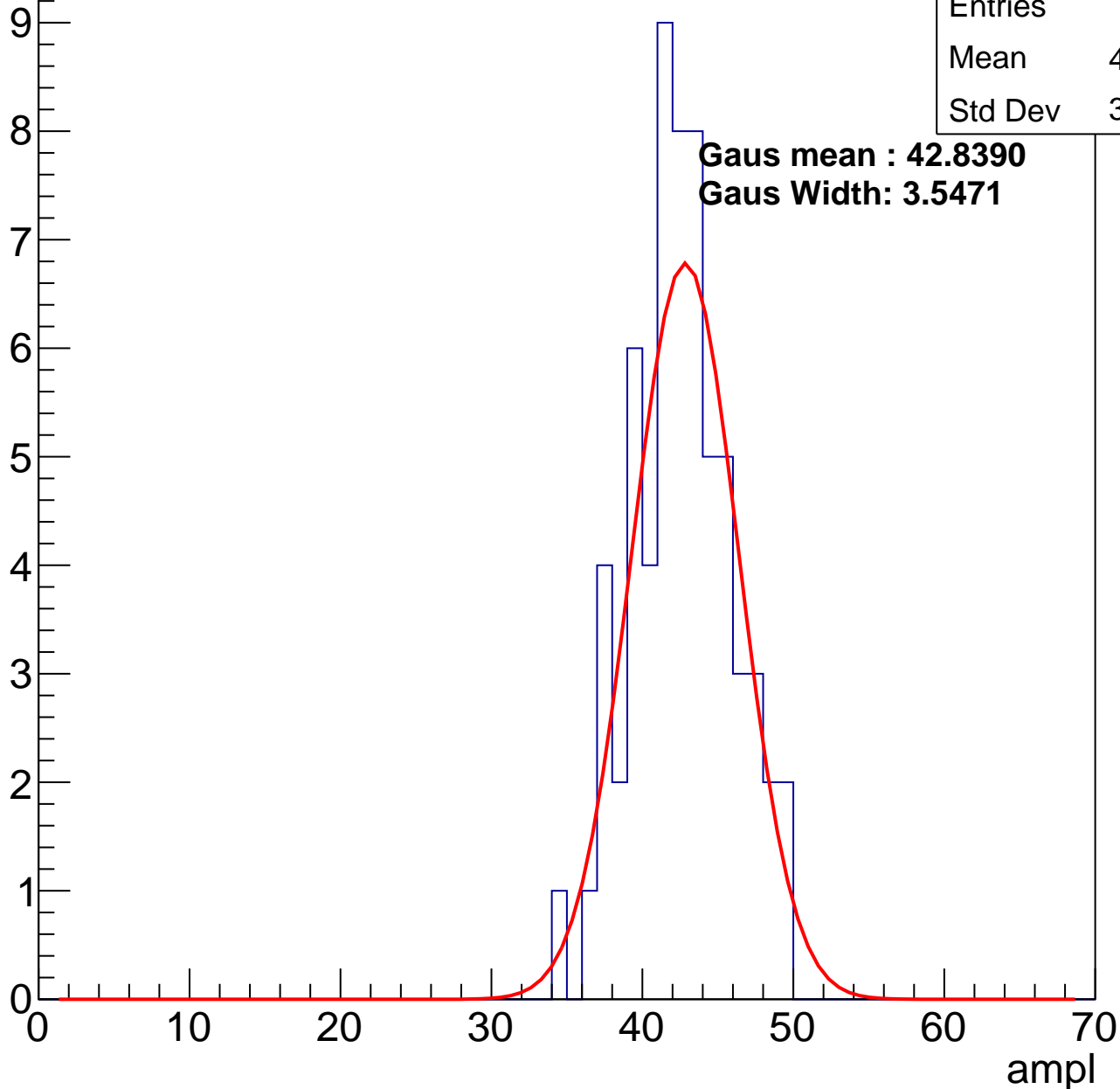
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	42.14
Std Dev	3.275

**Gaus mean : 42.8390**

**Gaus Width: 3.5471**

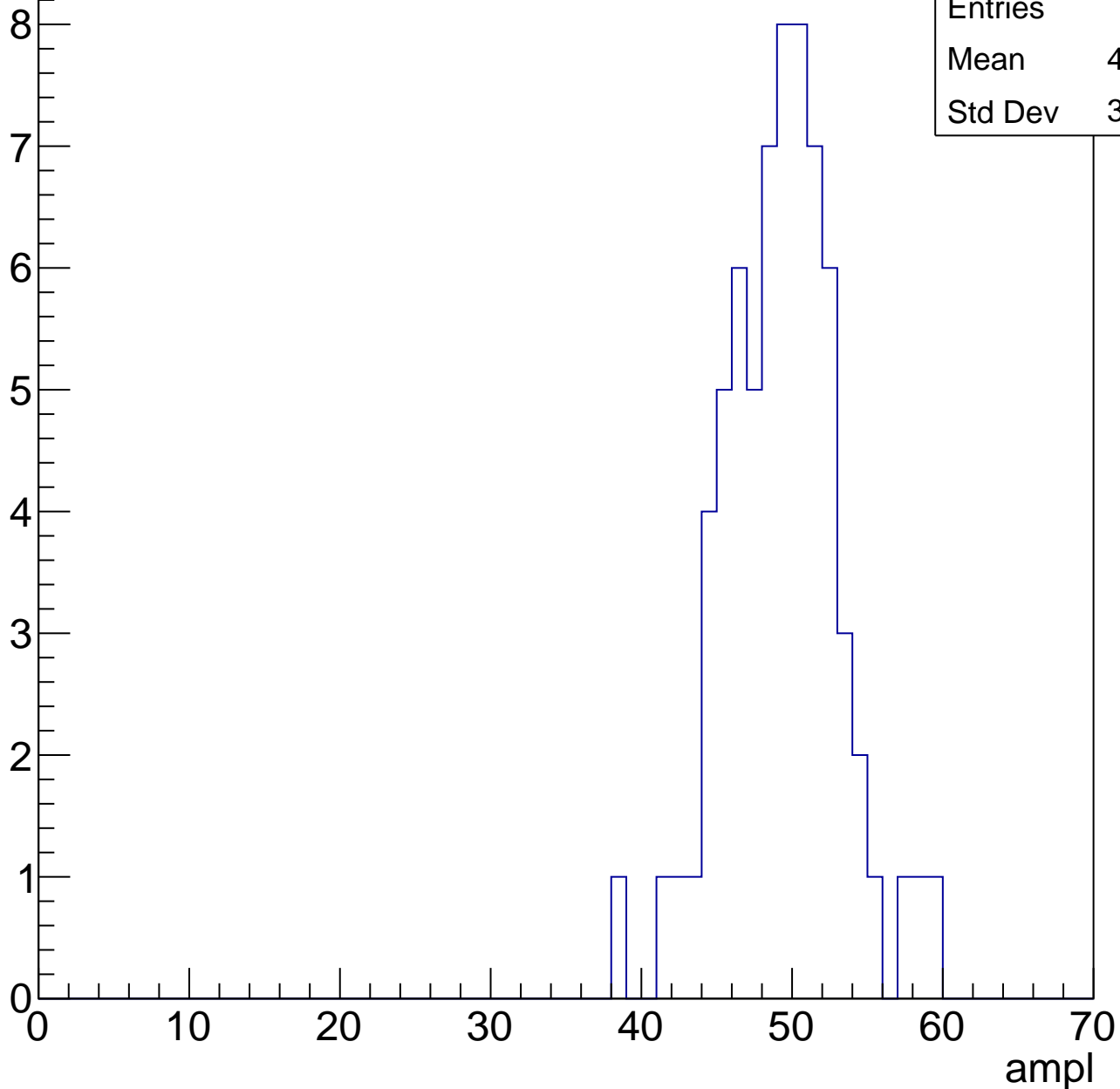


# B1L101S, U18-ch106, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	48.83
Std Dev	3.803

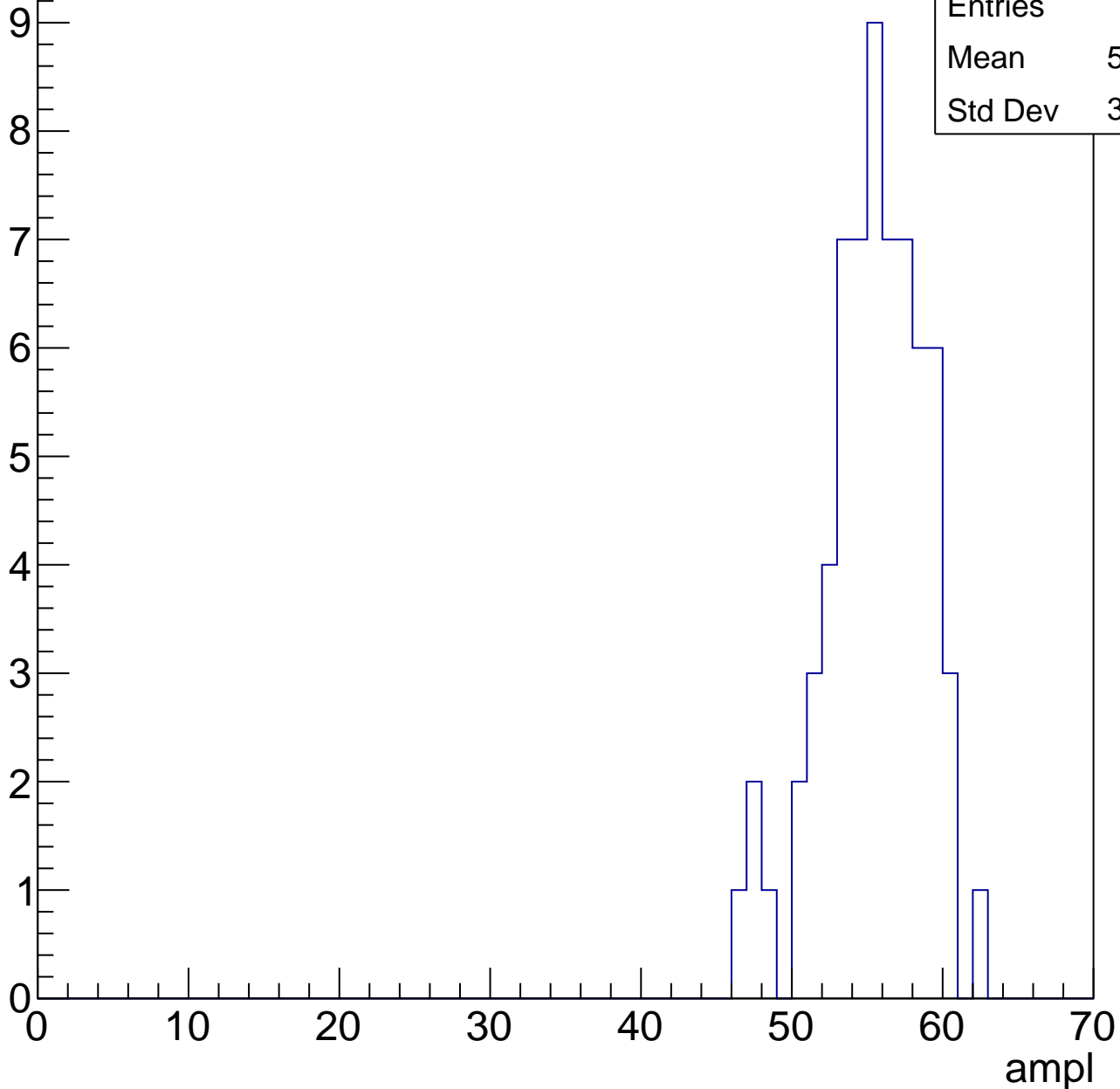


# B1L101S, U18-ch106, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	54.97
Std Dev	3.339

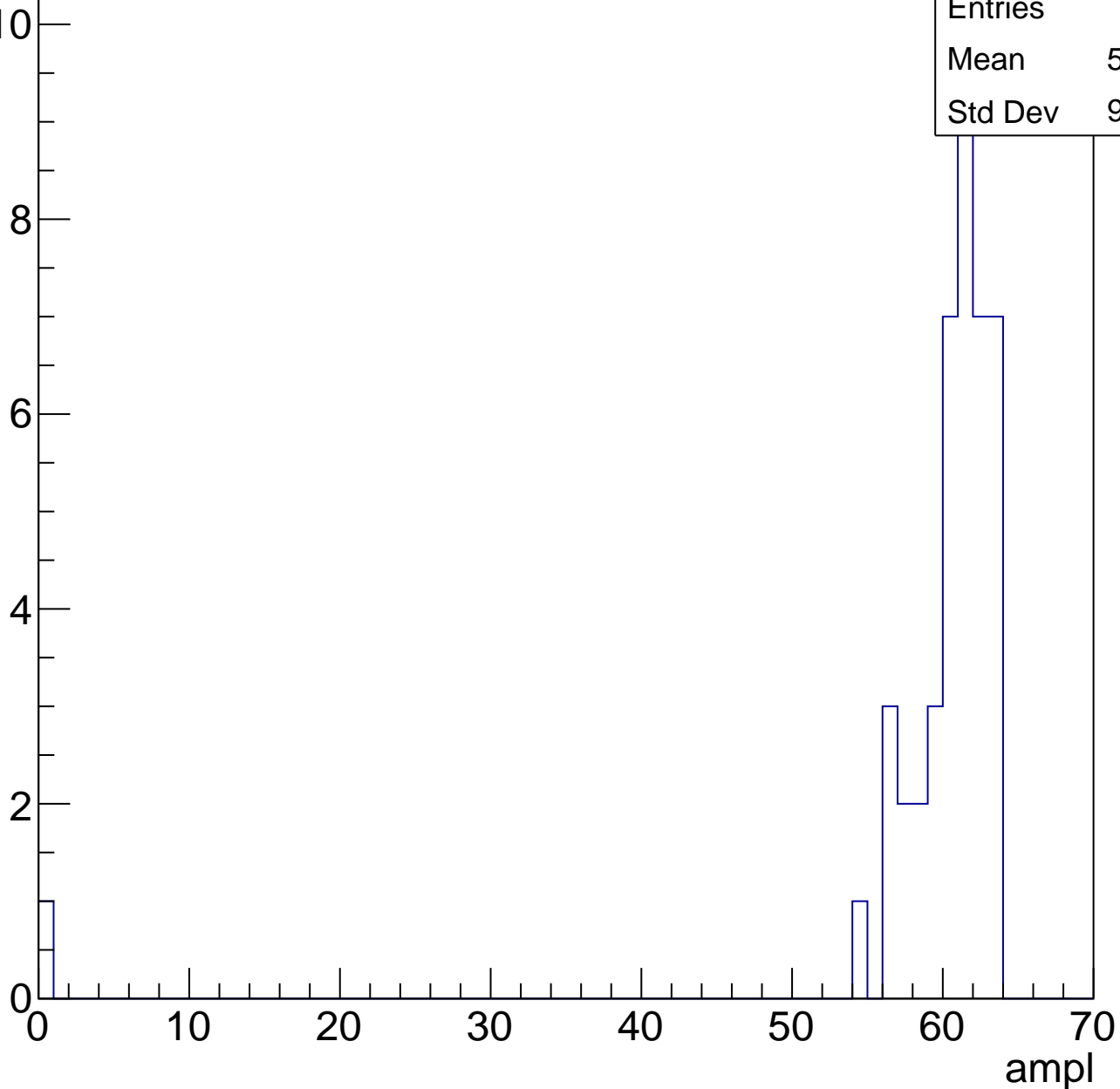


# B1L101S, U18-ch106, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

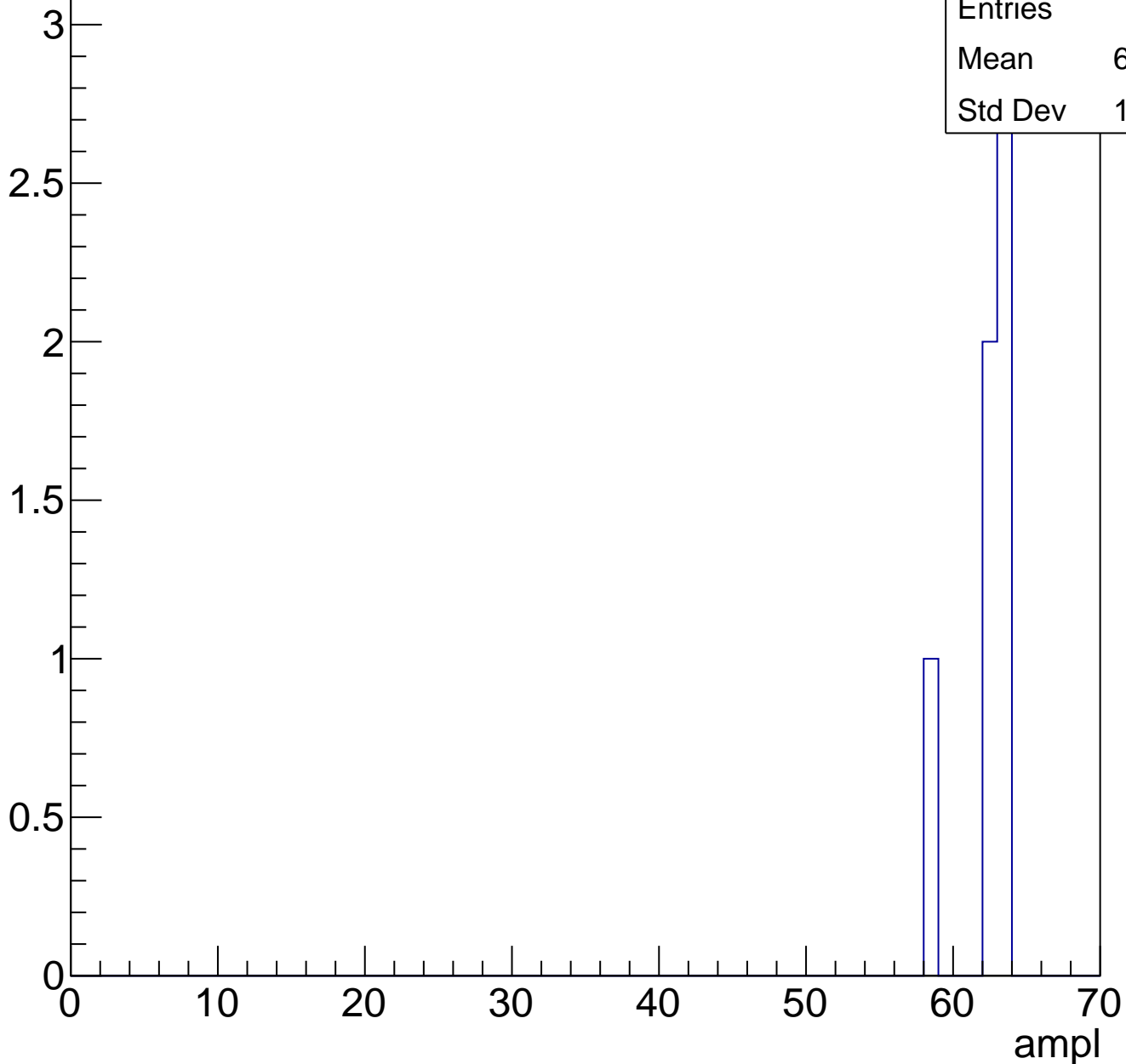
Entries	43
Mean	58.93
Std Dev	9.357



# B1L101S, U18-ch106, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch106, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch107, adc0

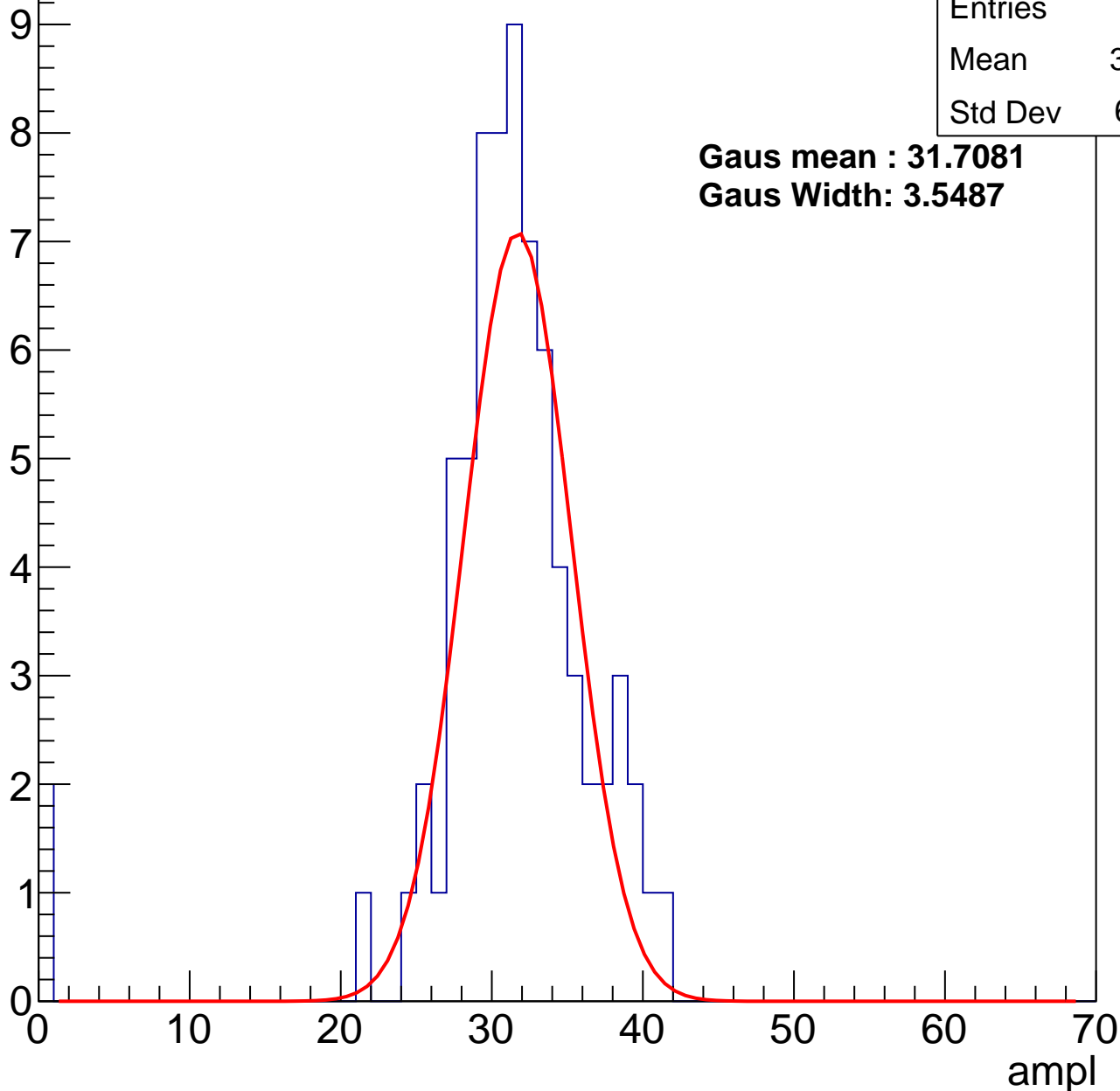
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	30.53
Std Dev	6.421

**Gaus mean : 31.7081**

**Gaus Width: 3.5487**



# B1L101S, U18-ch107, adc1

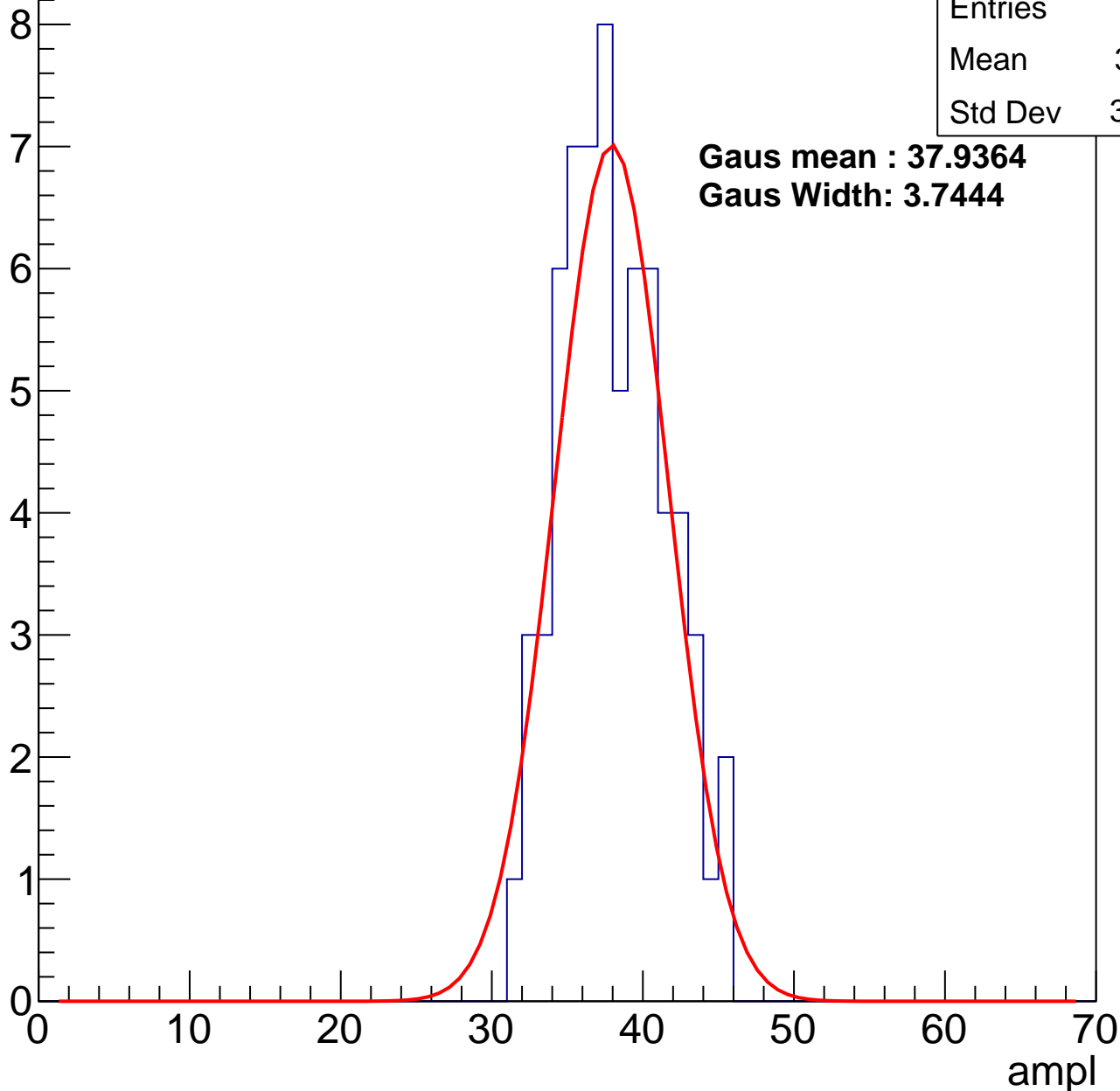
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	37.61
Std Dev	3.384

**Gaus mean : 37.9364**

**Gaus Width: 3.7444**



# B1L101S, U18-ch107, adc2

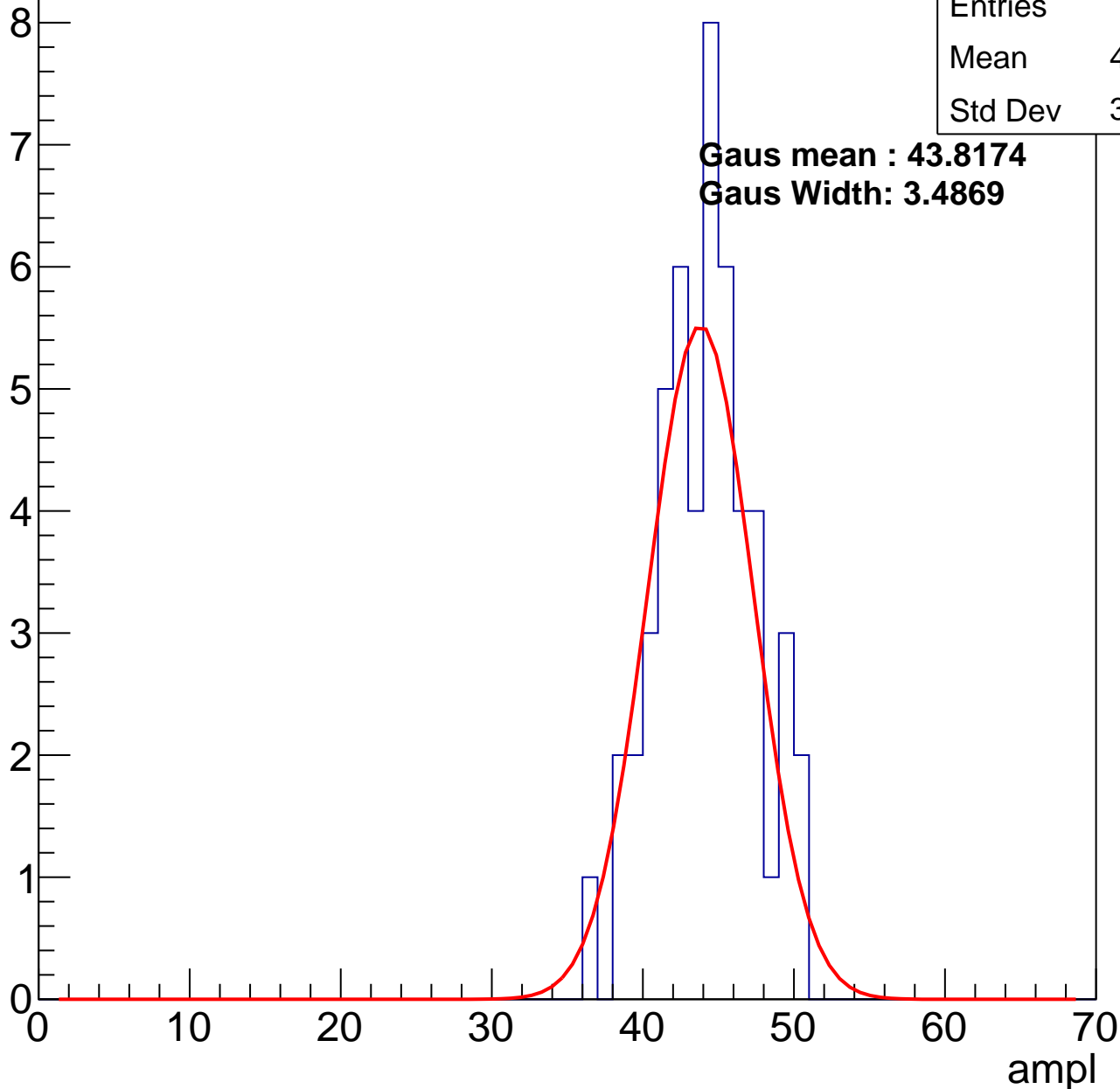
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	43.69
Std Dev	3.202

**Gaus mean : 43.8174**

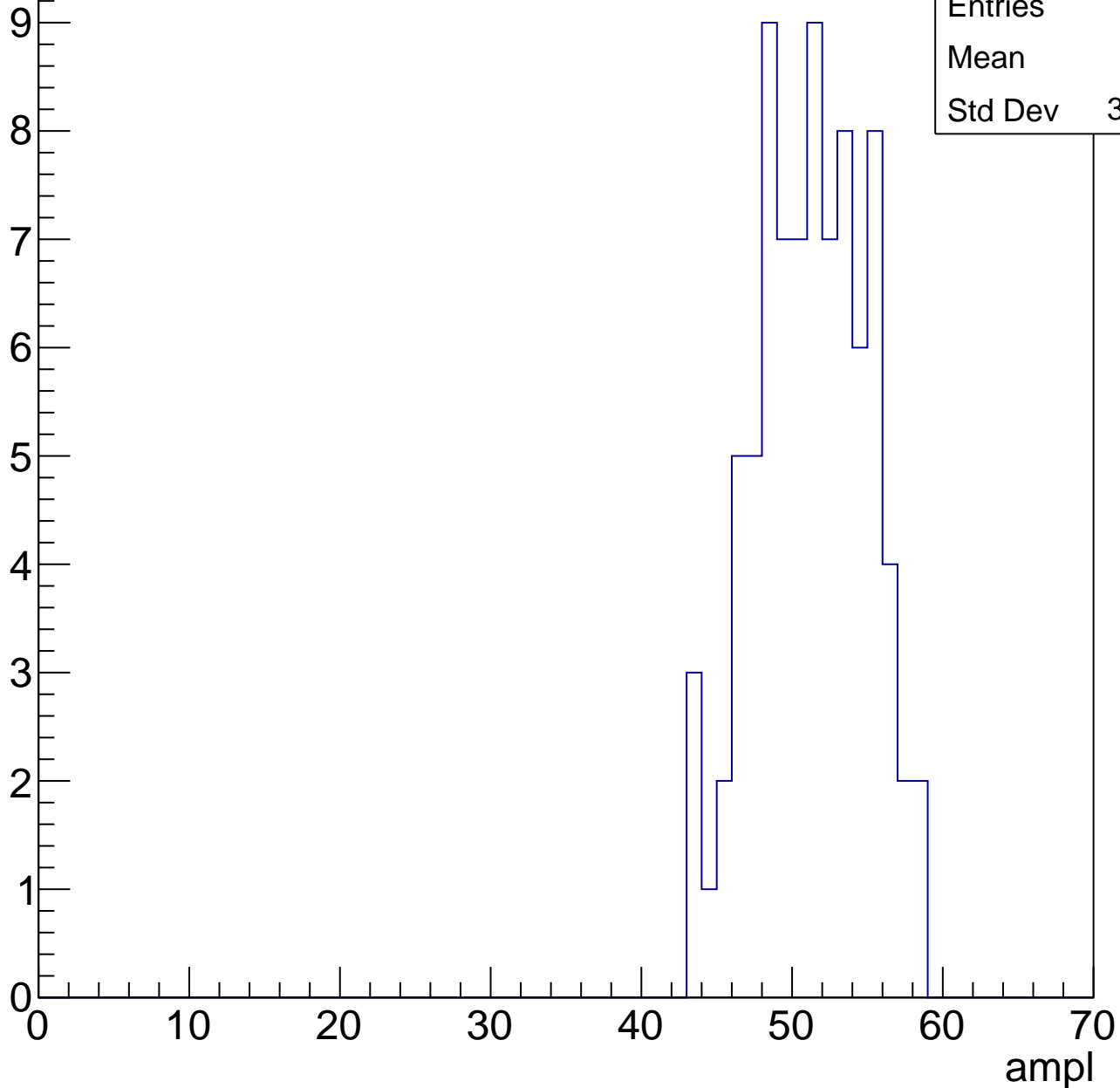
**Gaus Width: 3.4869**



# B1L101S, U18-ch107, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

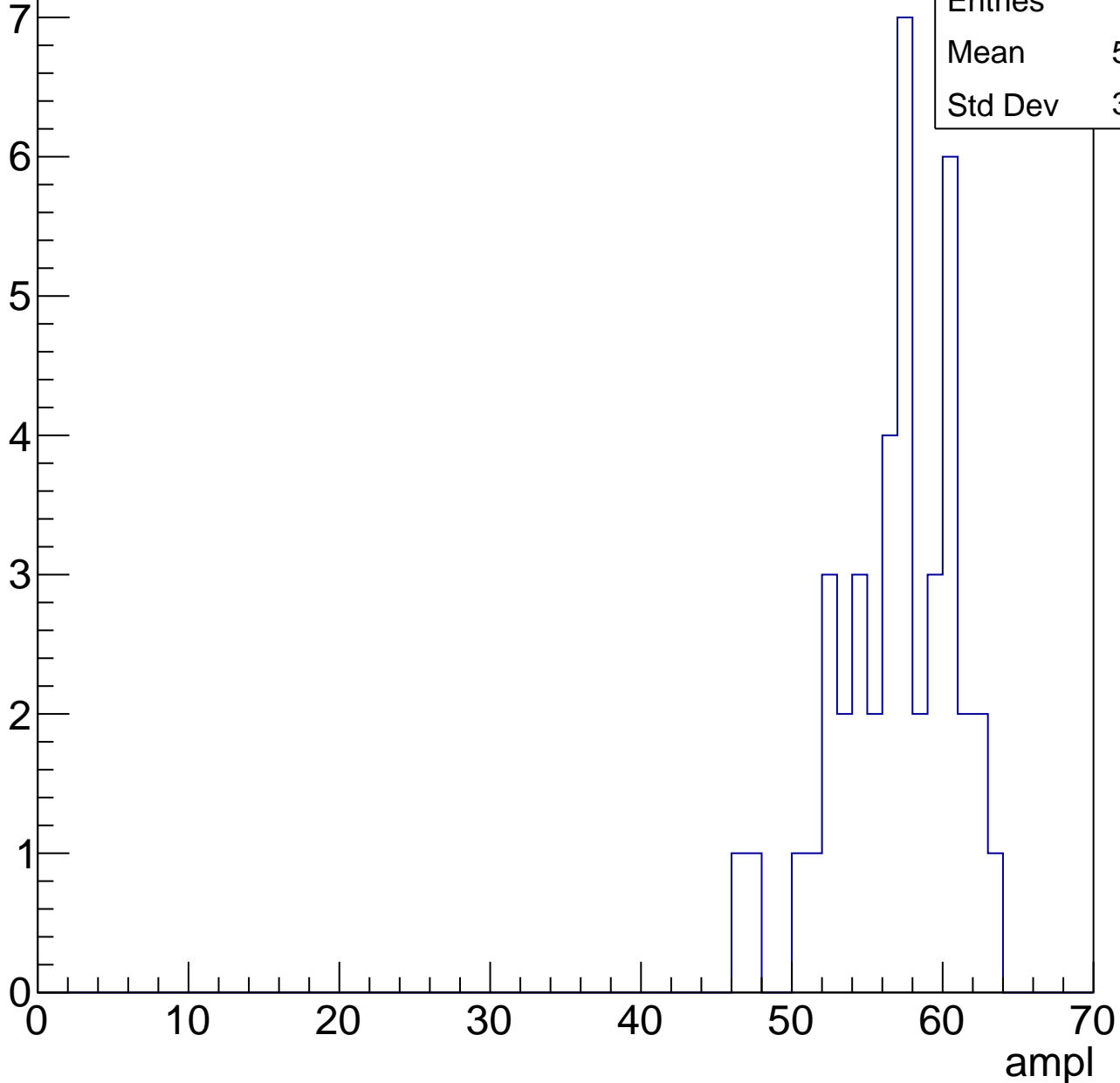


# B1L101S, U18-ch107, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	41
Mean	56.41
Std Dev	3.901

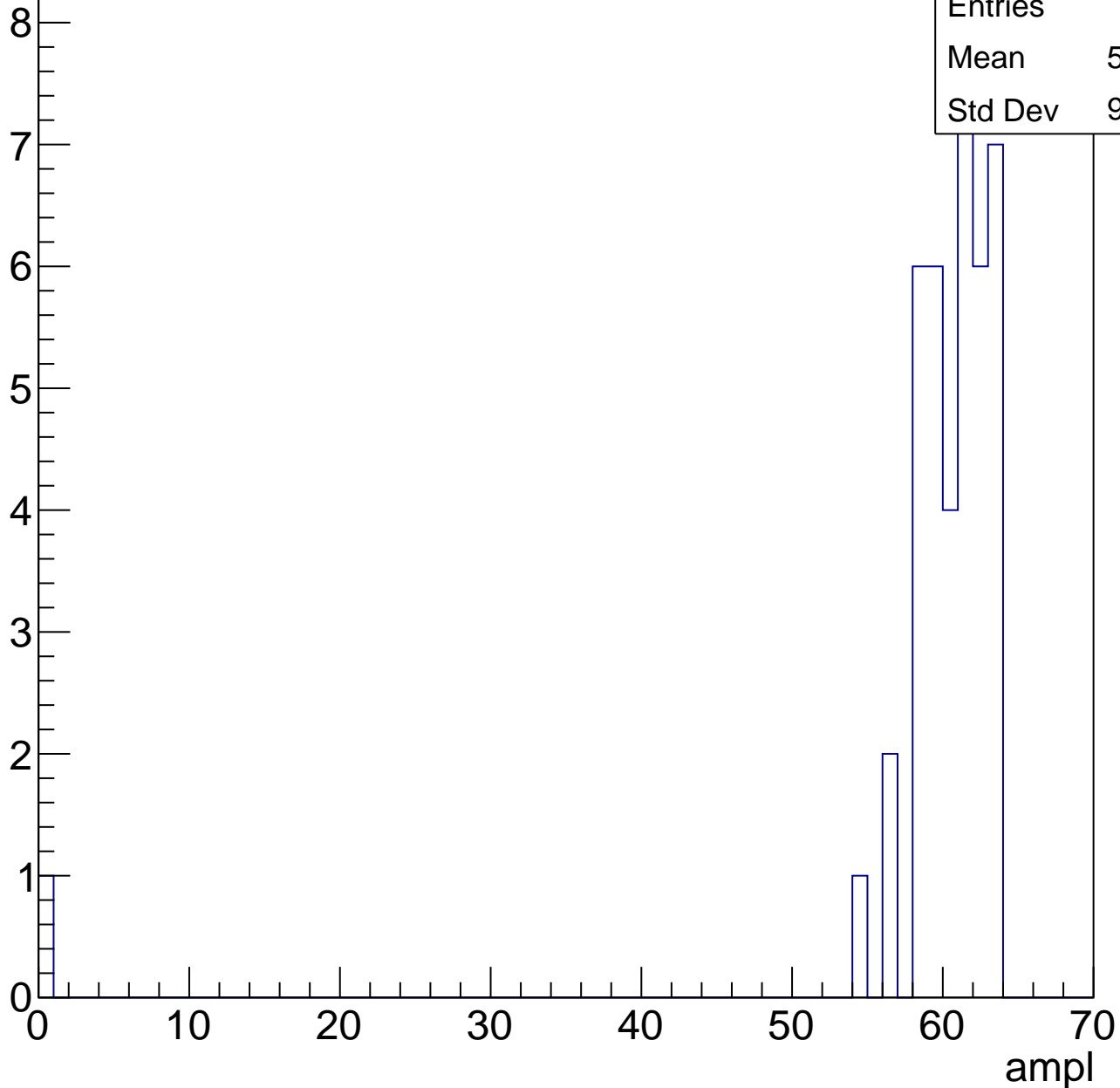


# B1L101S, U18-ch107, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

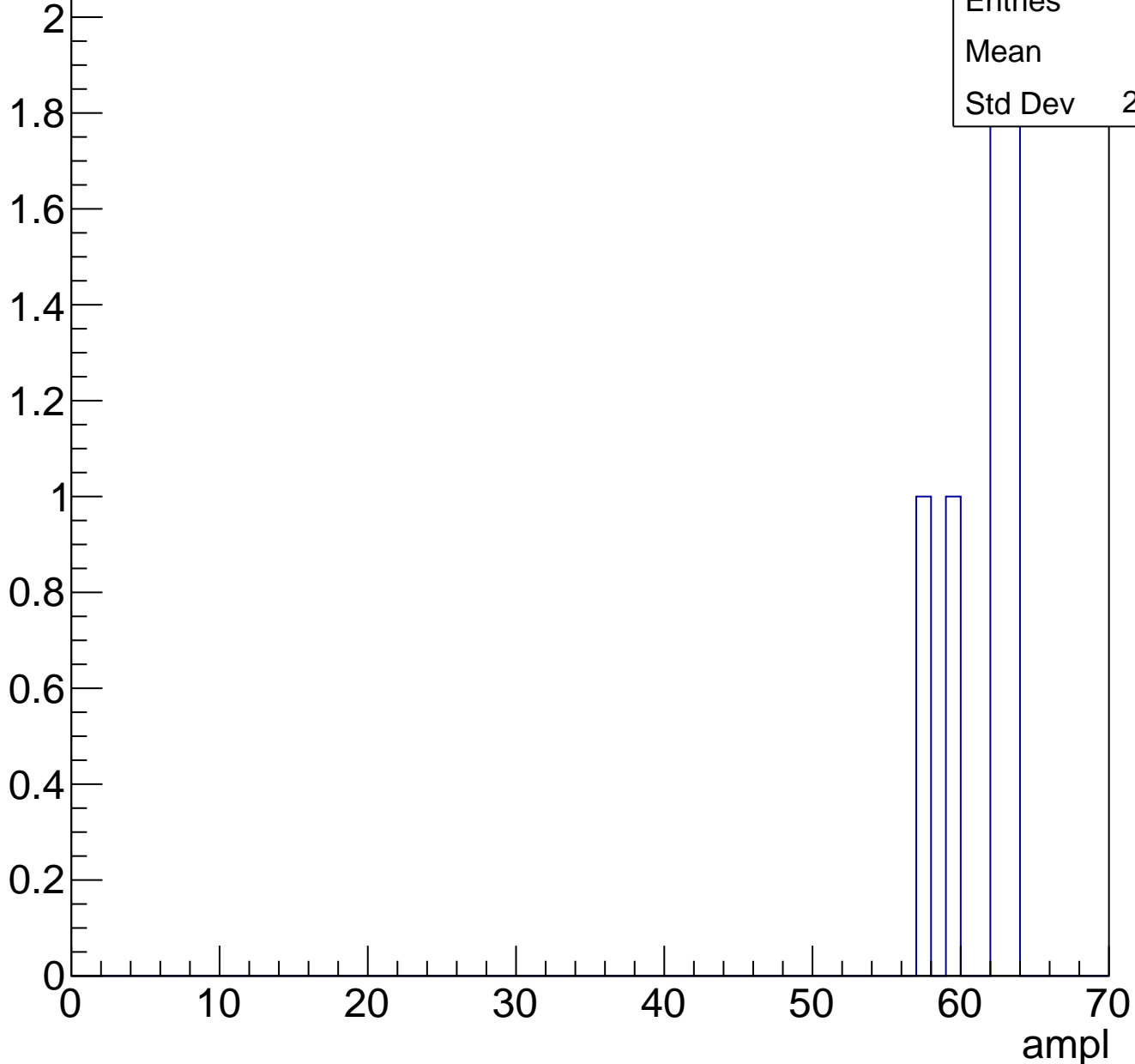
Entries	41
Mean	58.76
Std Dev	9.538



# B1L101S, U18-ch107, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	6
Mean	61
Std Dev	2.236



# B1L101S, U18-ch107, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch108, adc0

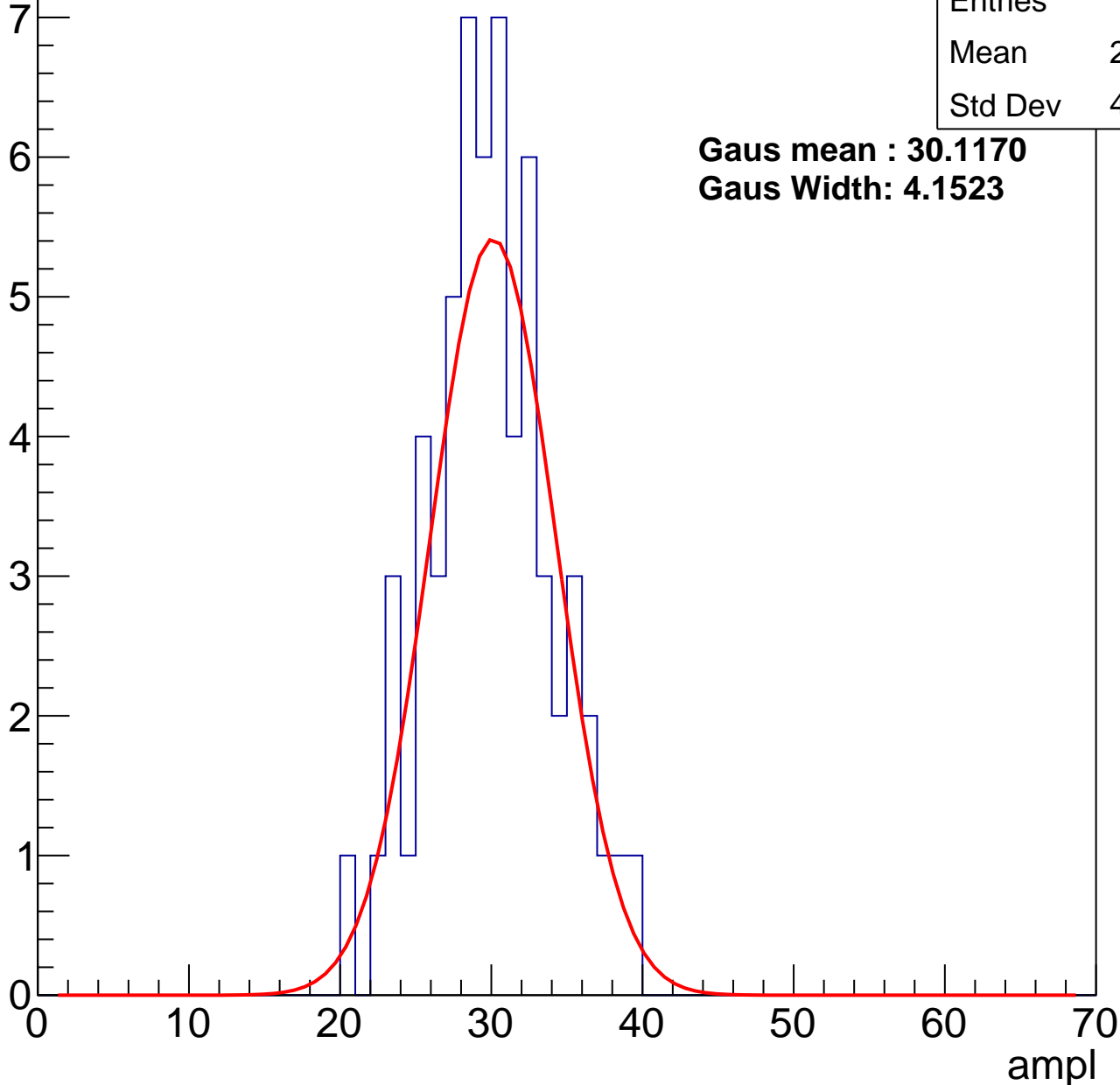
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	29.54
Std Dev	4.027

**Gaus mean : 30.1170**

**Gaus Width: 4.1523**



# B1L101S, U18-ch108, adc1

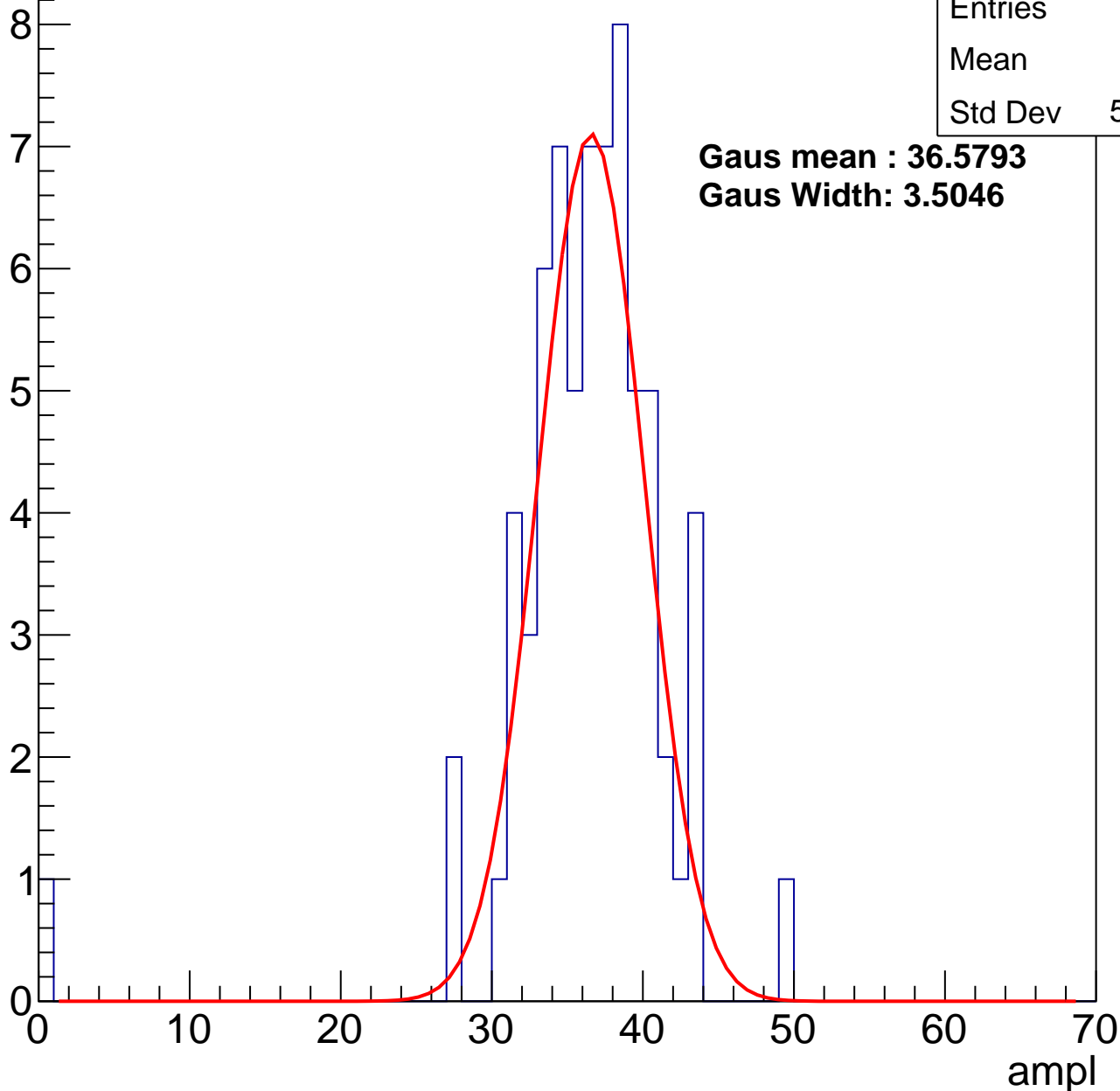
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	35.8
Std Dev	5.825

**Gaus mean : 36.5793**

**Gaus Width: 3.5046**



# B1L101S, U18-ch108, adc2

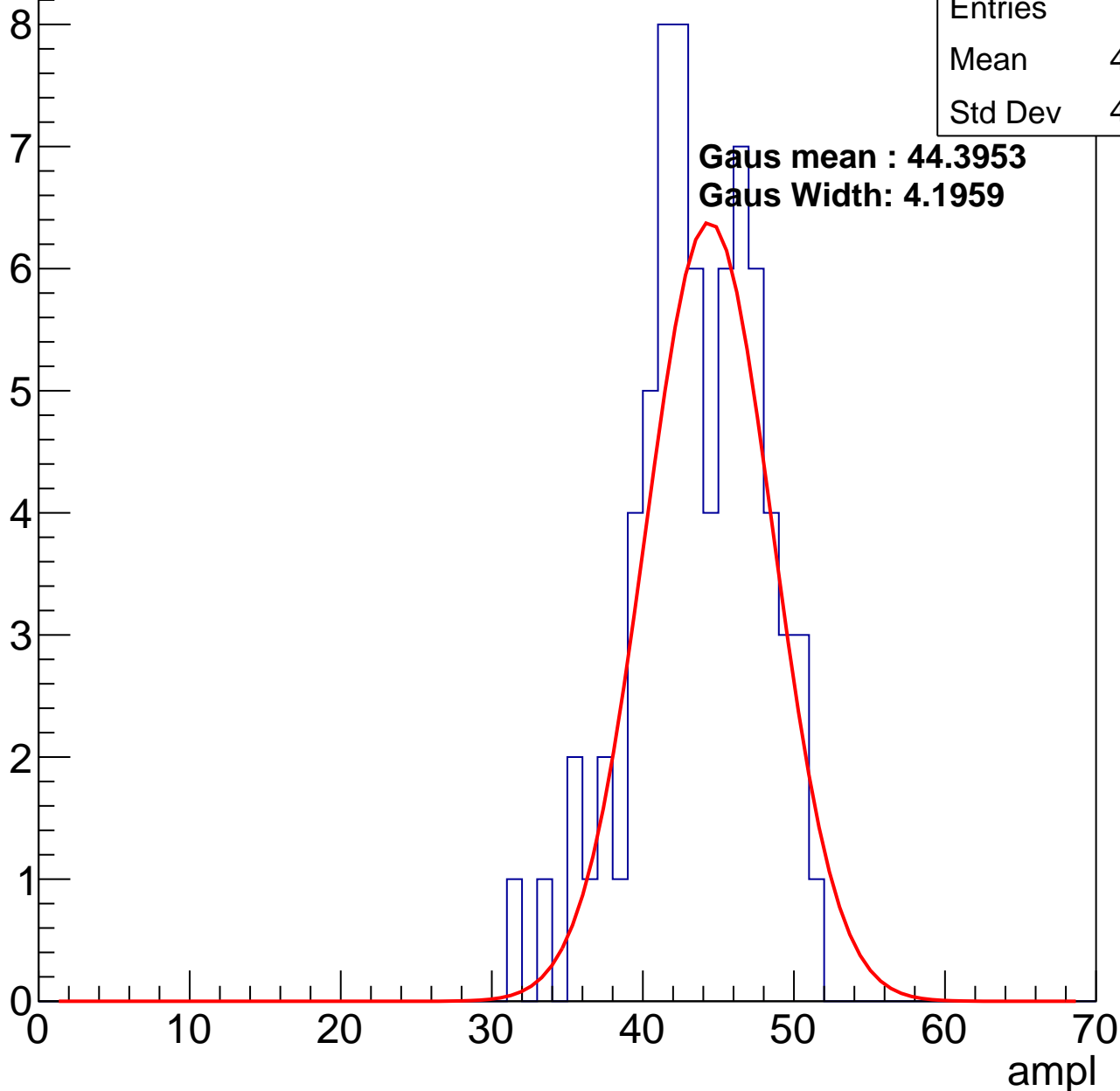
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	43.15
Std Dev	4.173

**Gaus mean : 44.3953**

**Gaus Width: 4.1959**

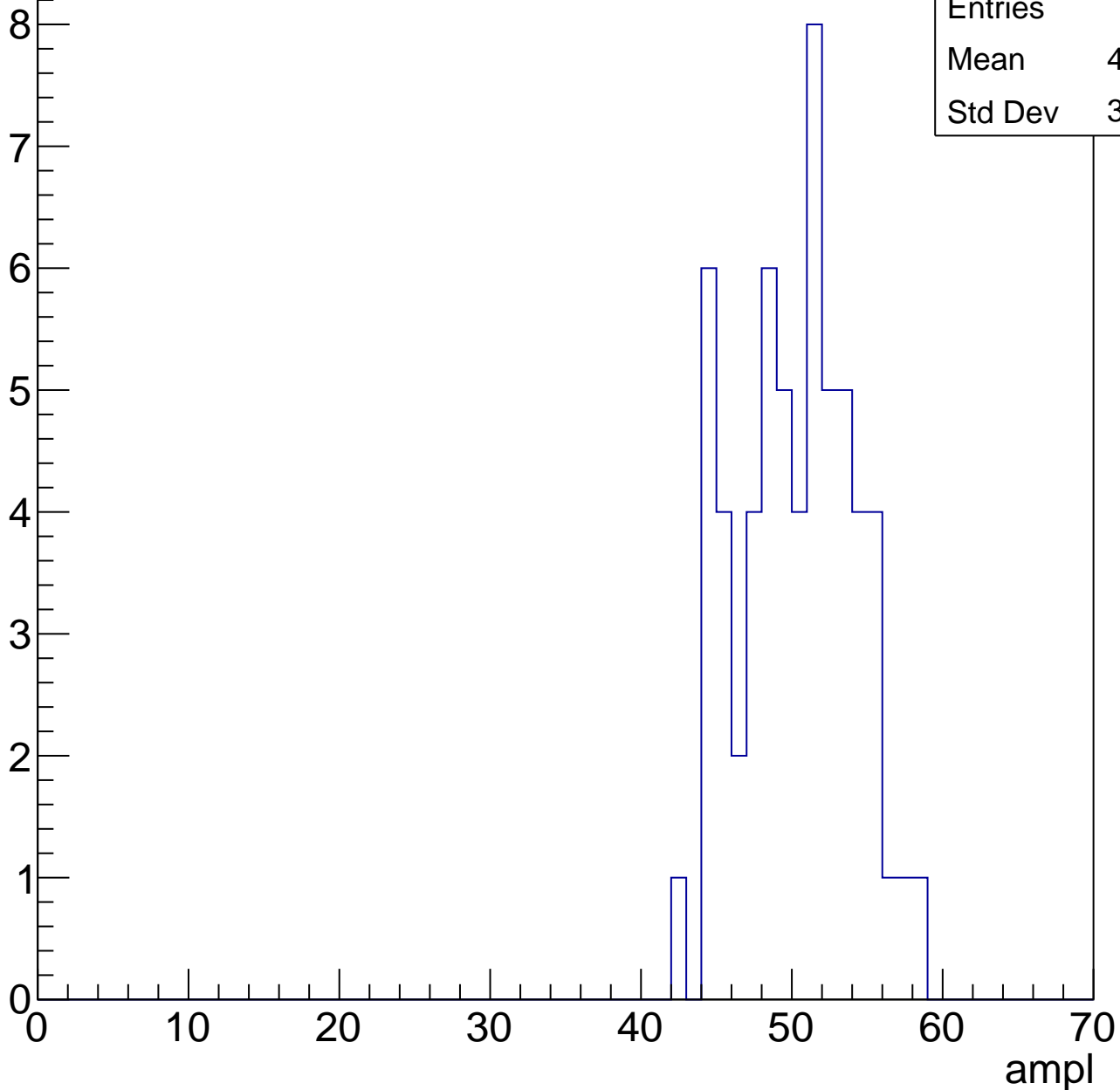


# B1L101S, U18-ch108, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	49.82
Std Dev	3.757

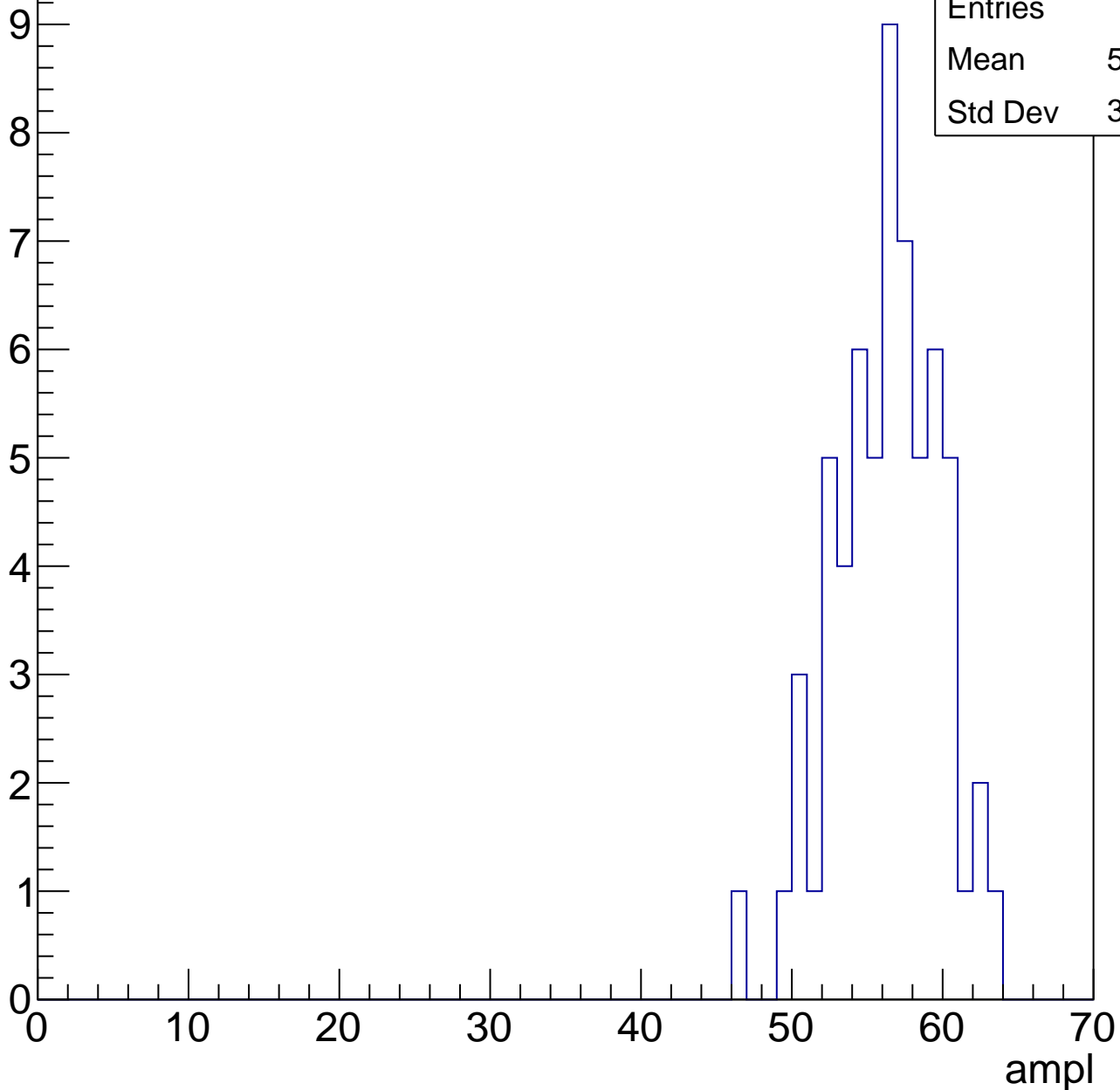


# B1L101S, U18-ch108, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	55.84
Std Dev	3.437

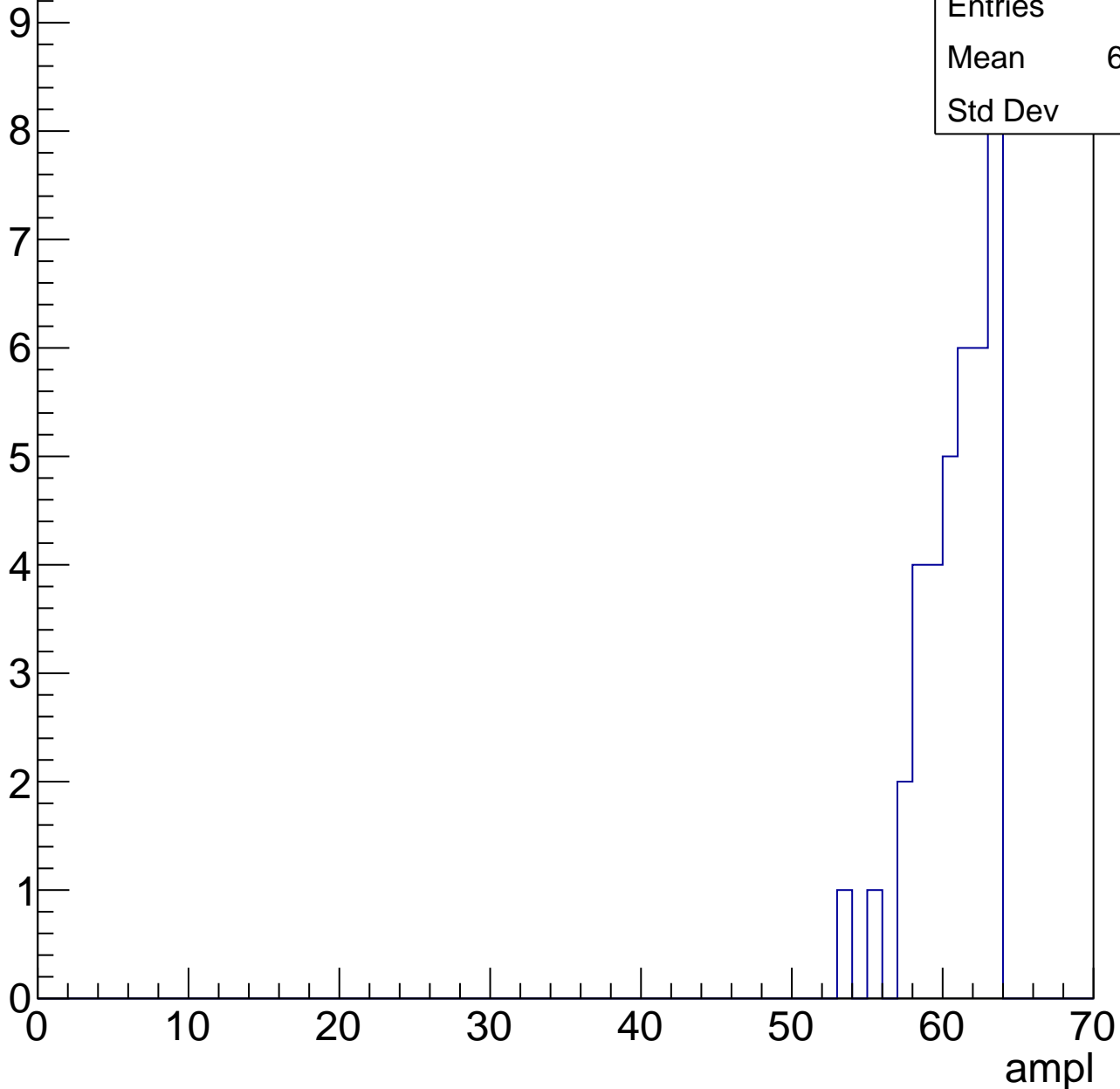


# B1L101S, U18-ch108, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

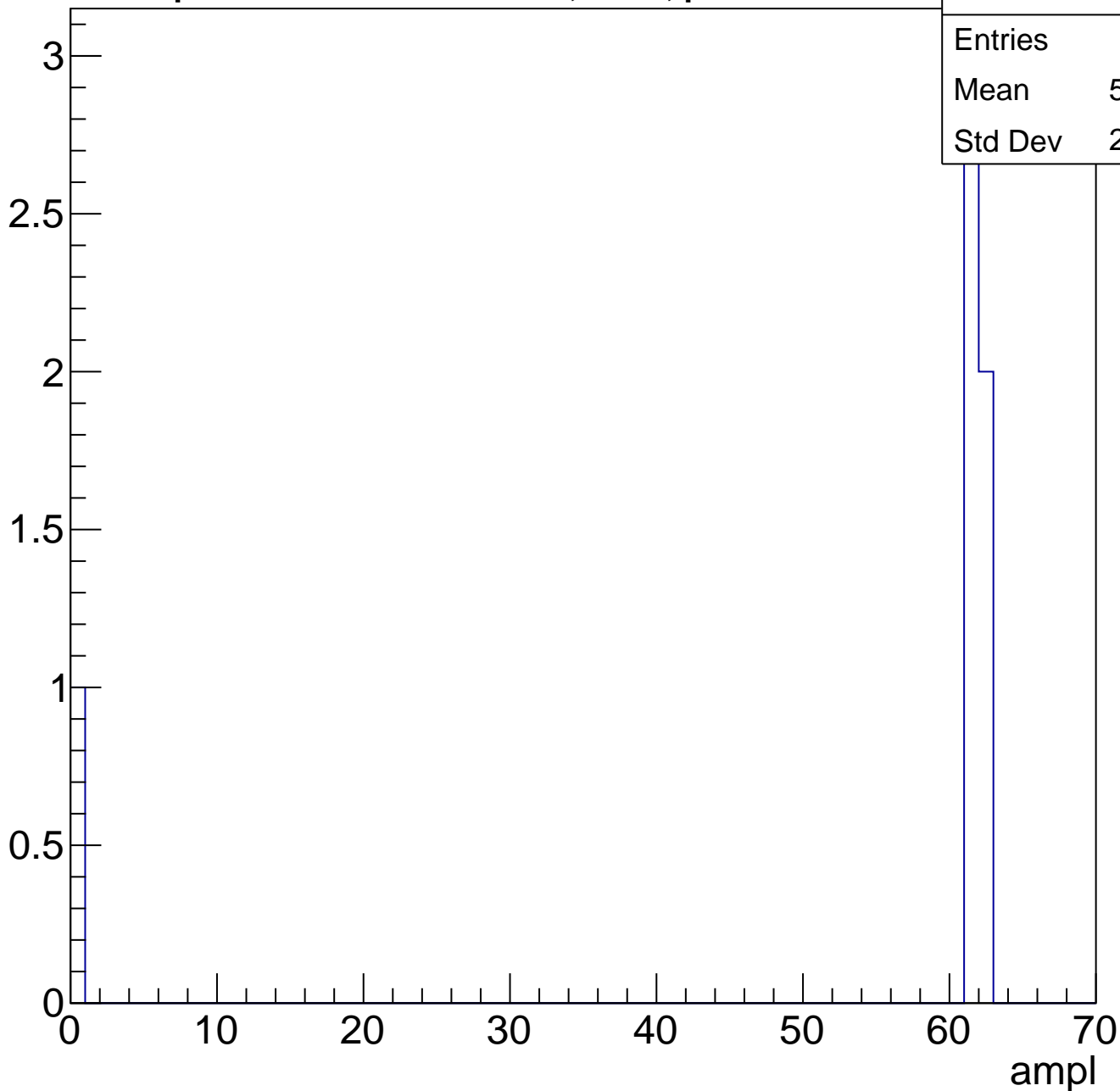
Entries	38
Mean	60.39
Std Dev	2.39



# B1L101S, U18-ch108, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch108, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch109, adc0

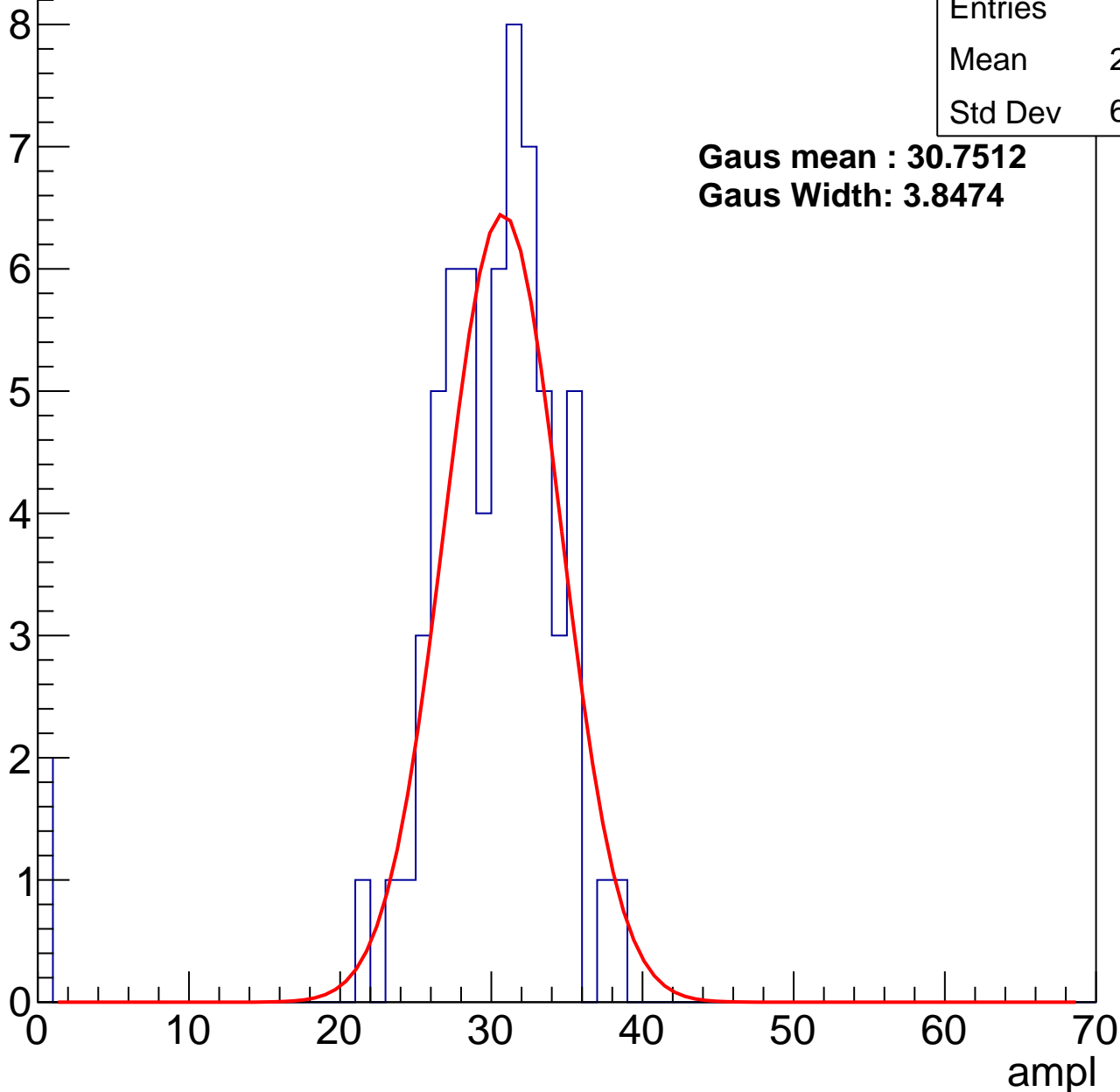
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	29.05
Std Dev	6.215

**Gaus mean : 30.7512**

**Gaus Width: 3.8474**



# B1L101S, U18-ch109, adc1

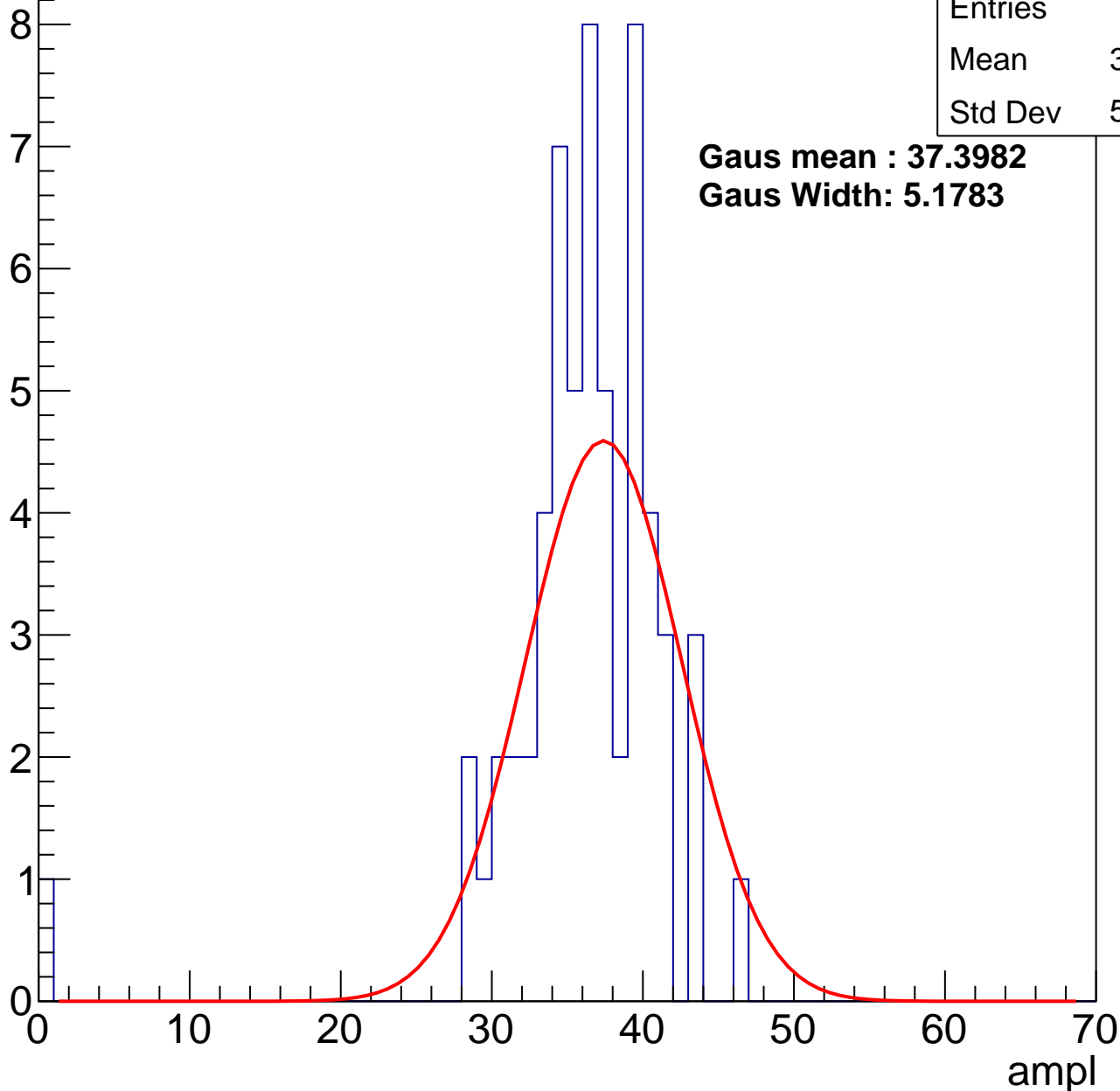
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	35.58
Std Dev	5.995

**Gaus mean : 37.3982**

**Gaus Width: 5.1783**



# B1L101S, U18-ch109, adc2

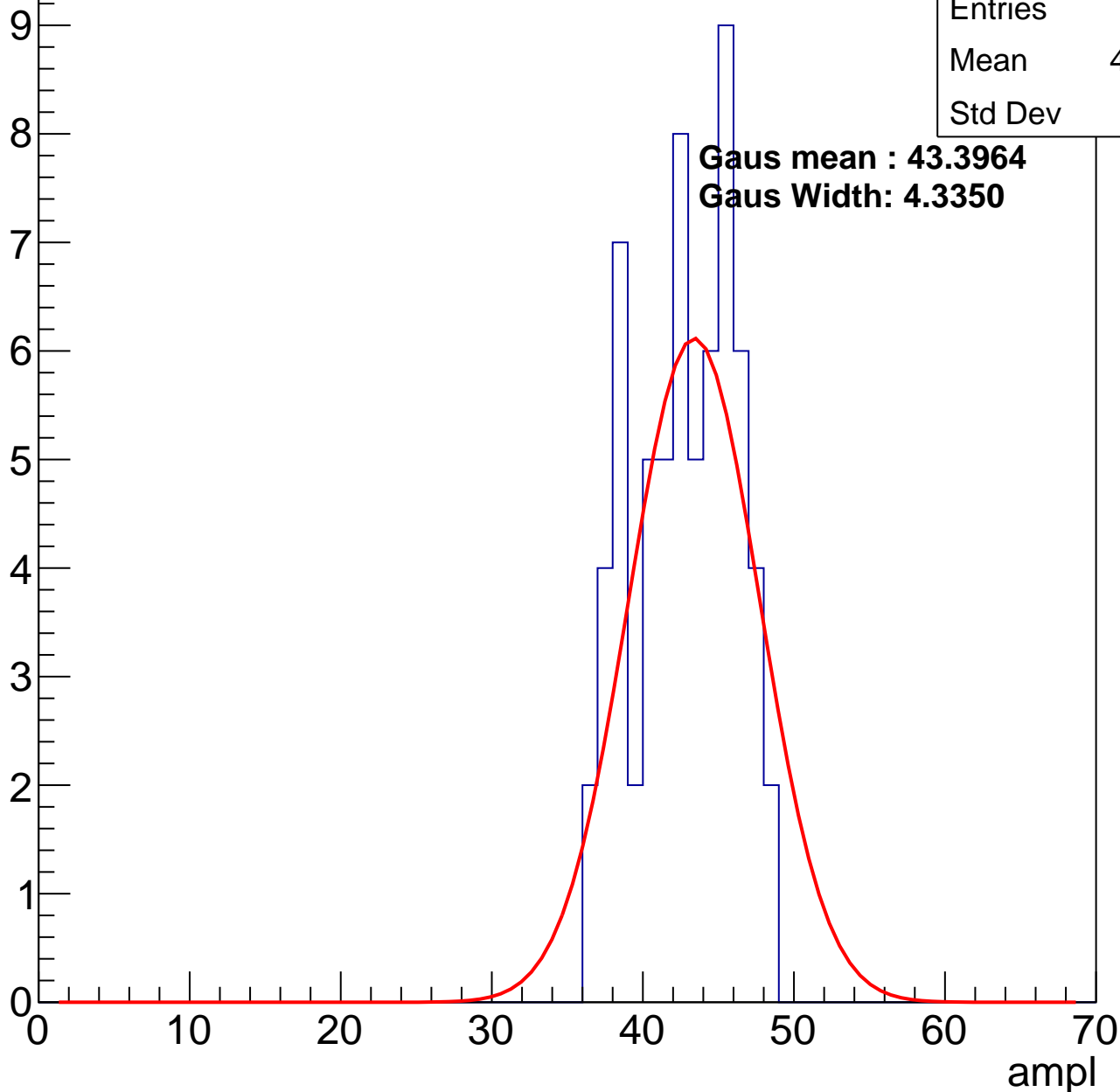
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	42.29
Std Dev	3.28

**Gaus mean : 43.3964**

**Gaus Width: 4.3350**



# B1L101S, U18-ch109, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

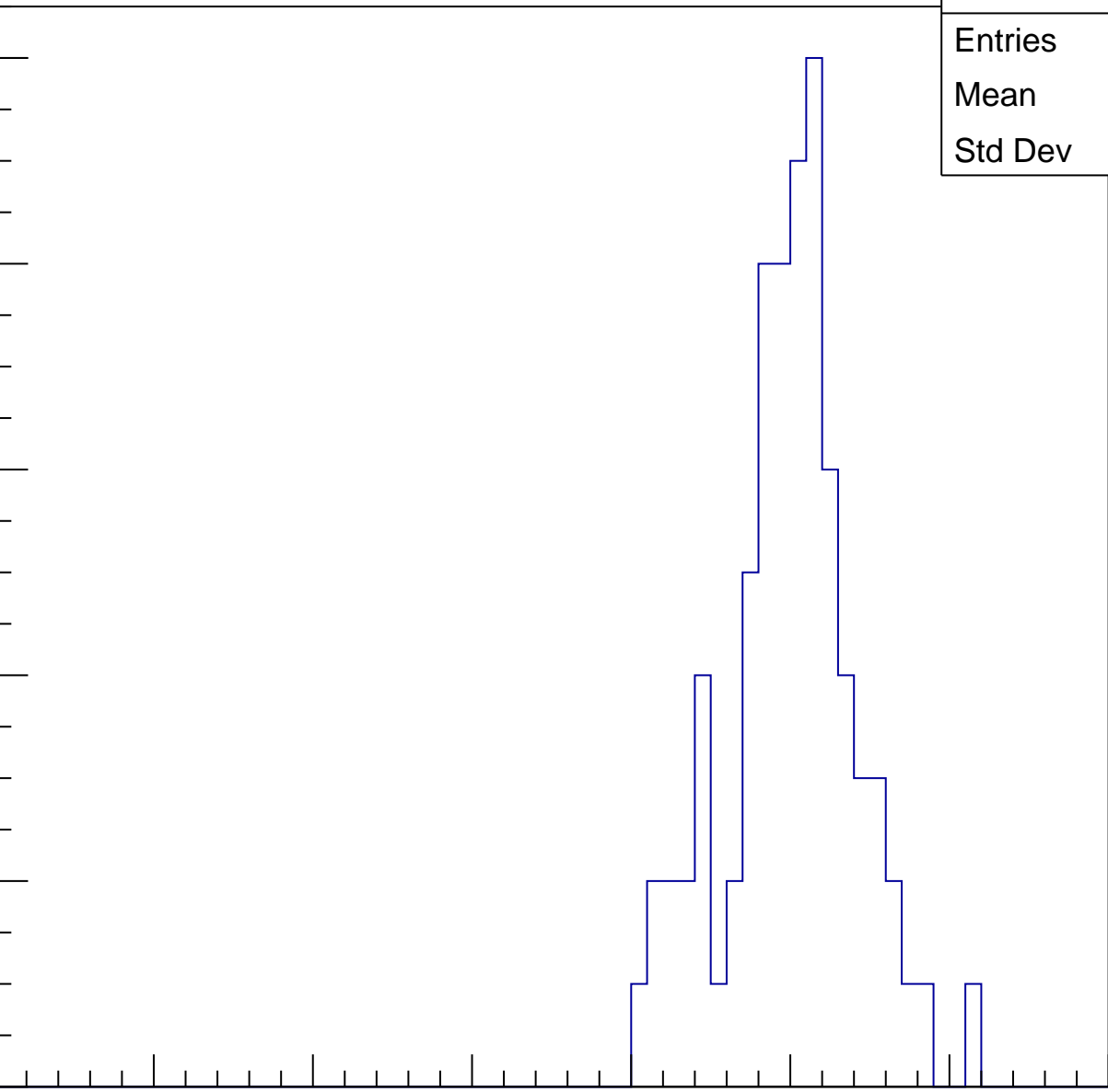
Entries	75
Mean	49.53
Std Dev	4.093

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

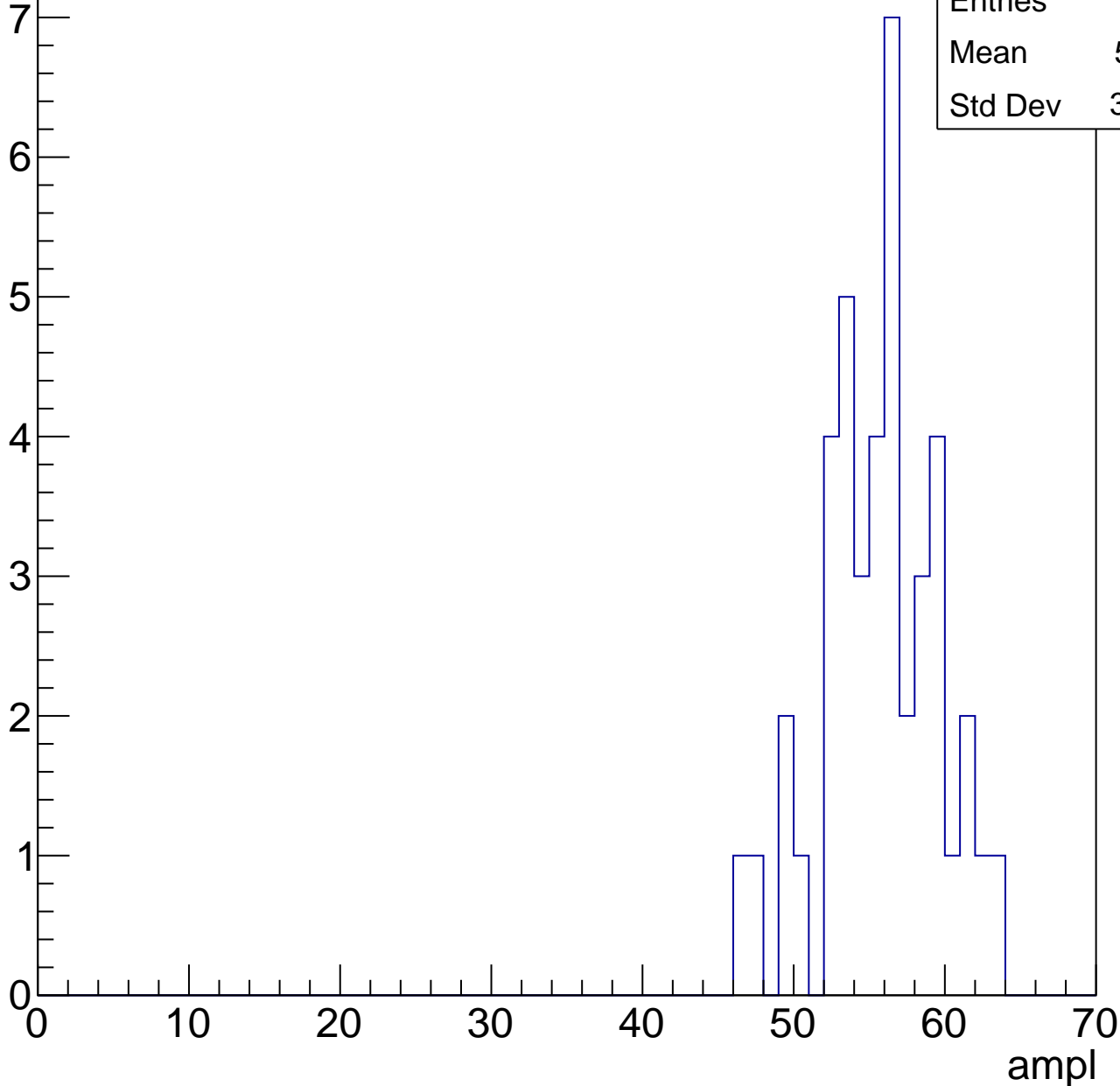


# B1L101S, U18-ch109, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

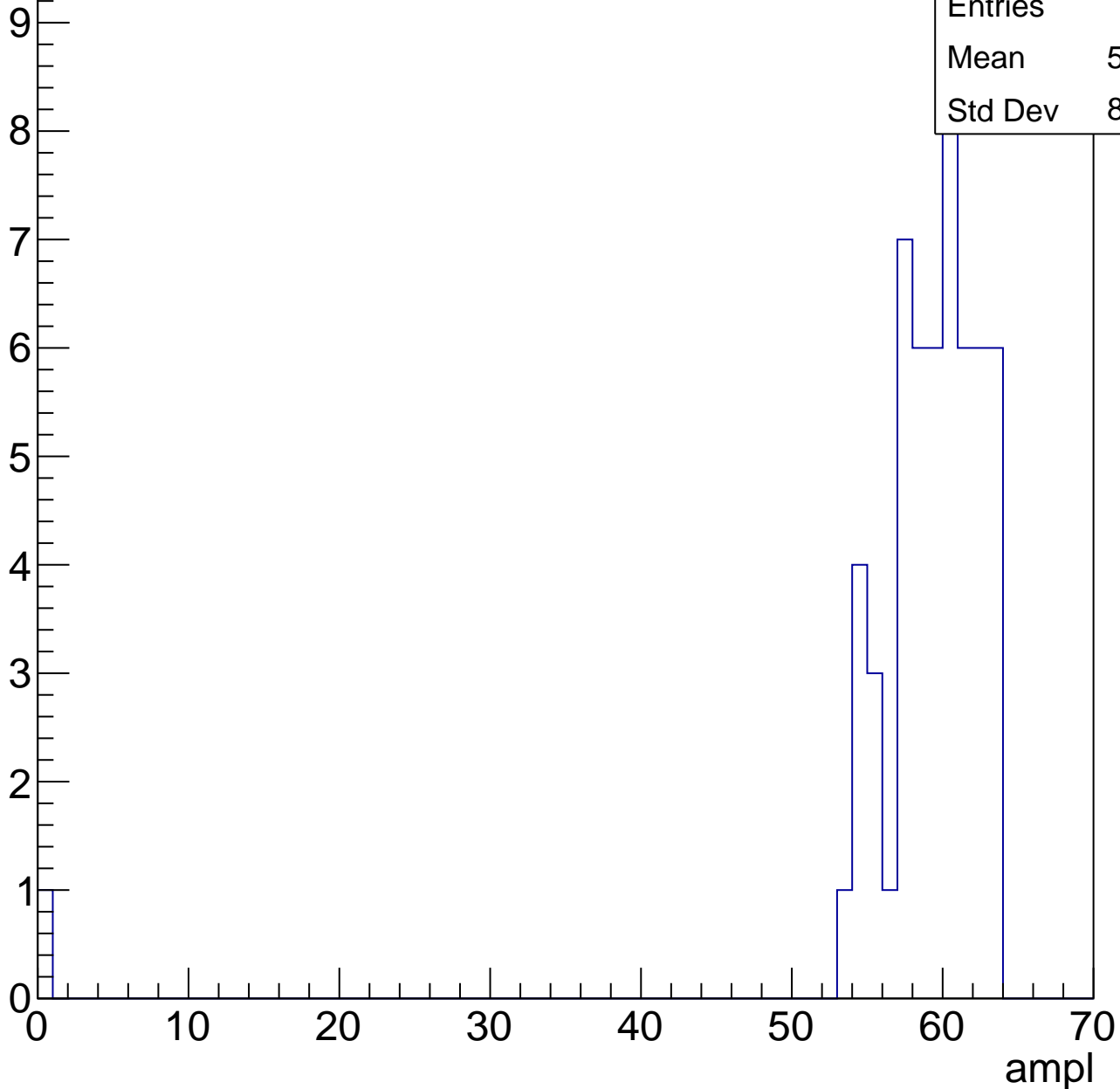
Entries	42
Mean	55.21
Std Dev	3.827



# B1L101S, U18-ch109, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

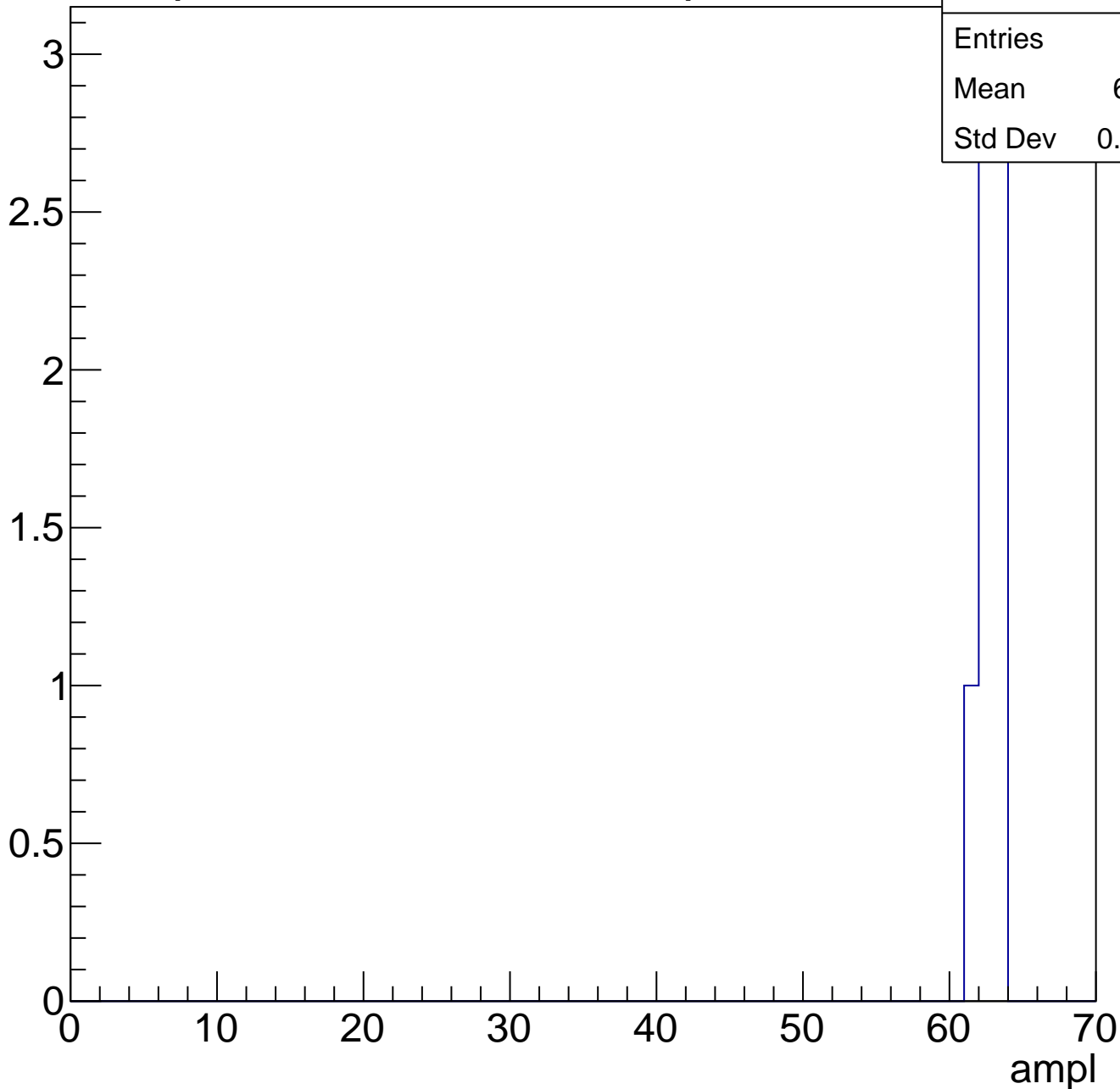
Entry



# B1L101S, U18-ch109, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch109, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U18-ch110, adc0

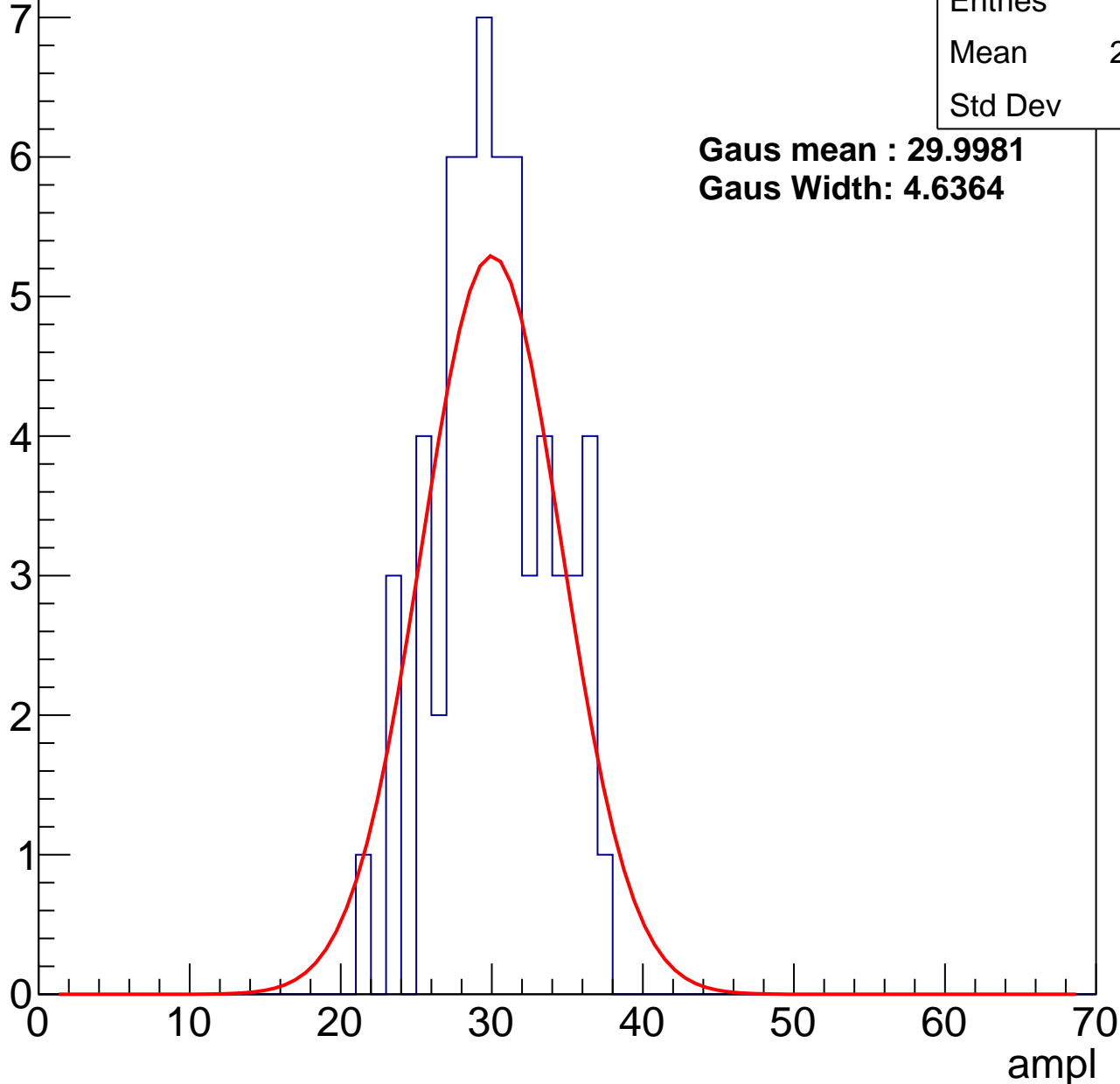
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	29.78
Std Dev	3.71

**Gaus mean : 29.9981**

**Gaus Width: 4.6364**



# B1L101S, U18-ch110, adc1

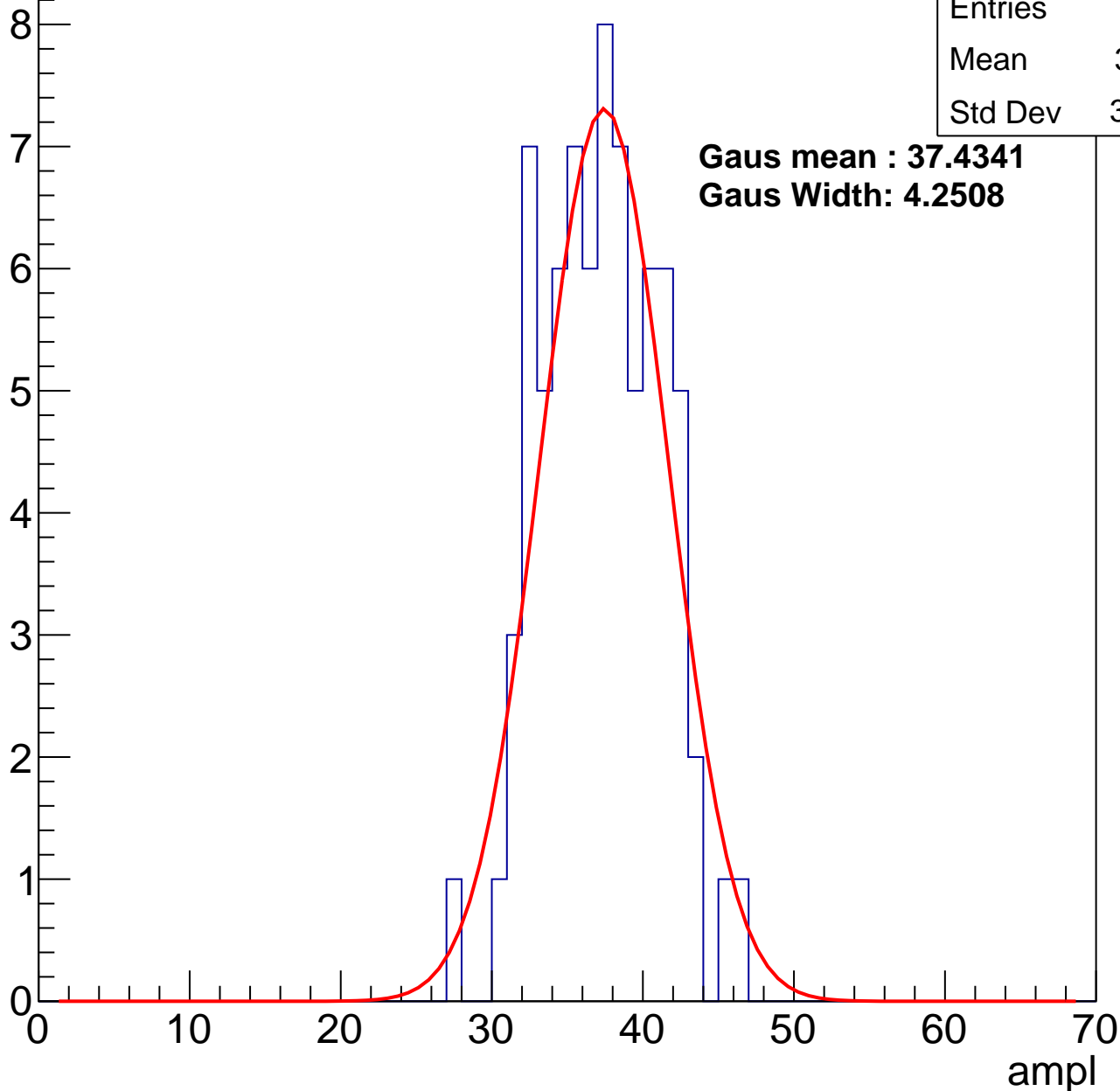
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	36.81
Std Dev	3.807

**Gaus mean : 37.4341**

**Gaus Width: 4.2508**



# B1L101S, U18-ch110, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	59
Mean	43.02
Std Dev	3.847

**Gaus mean : 43.9769**

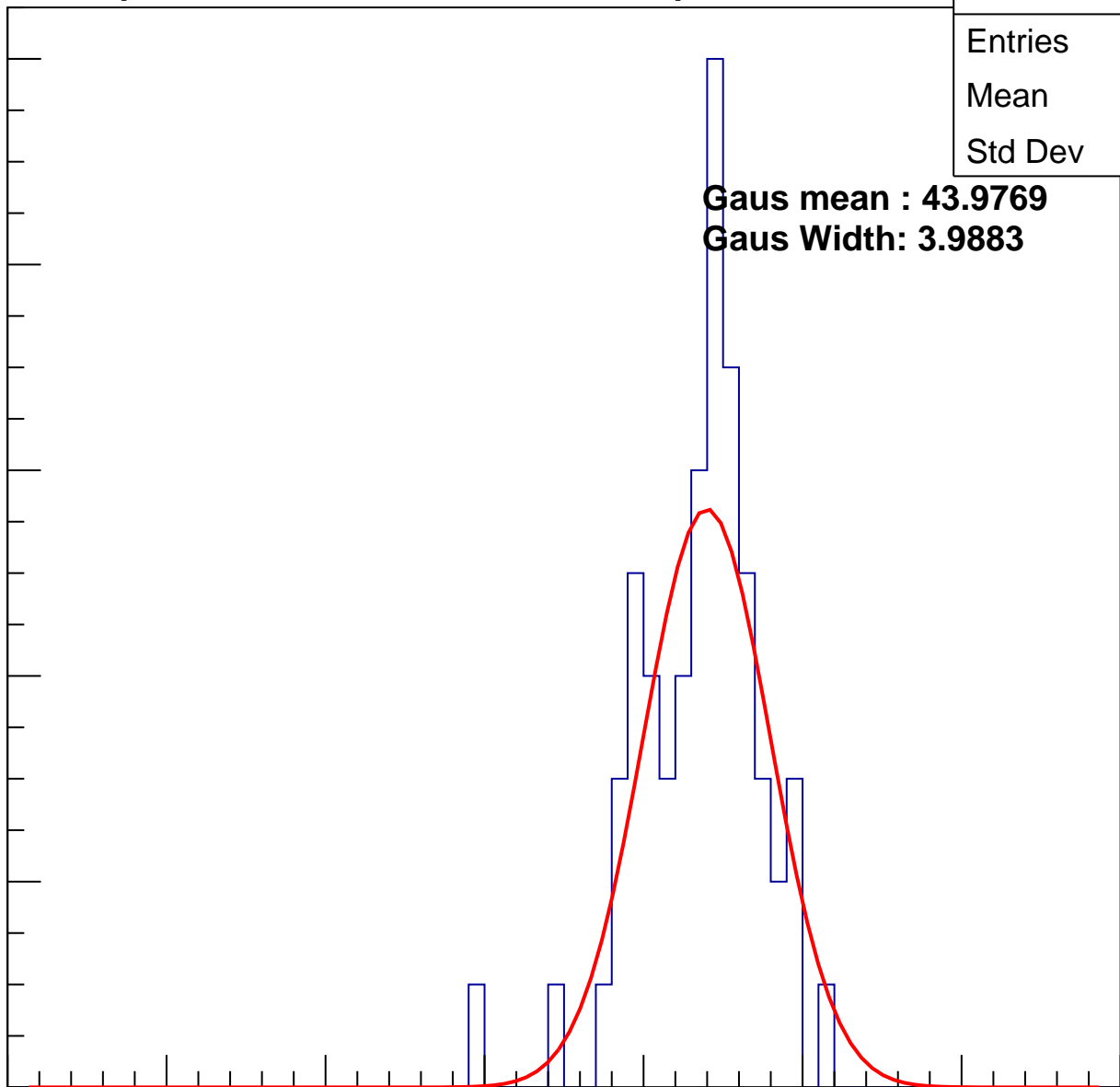
**Gaus Width: 3.9883**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

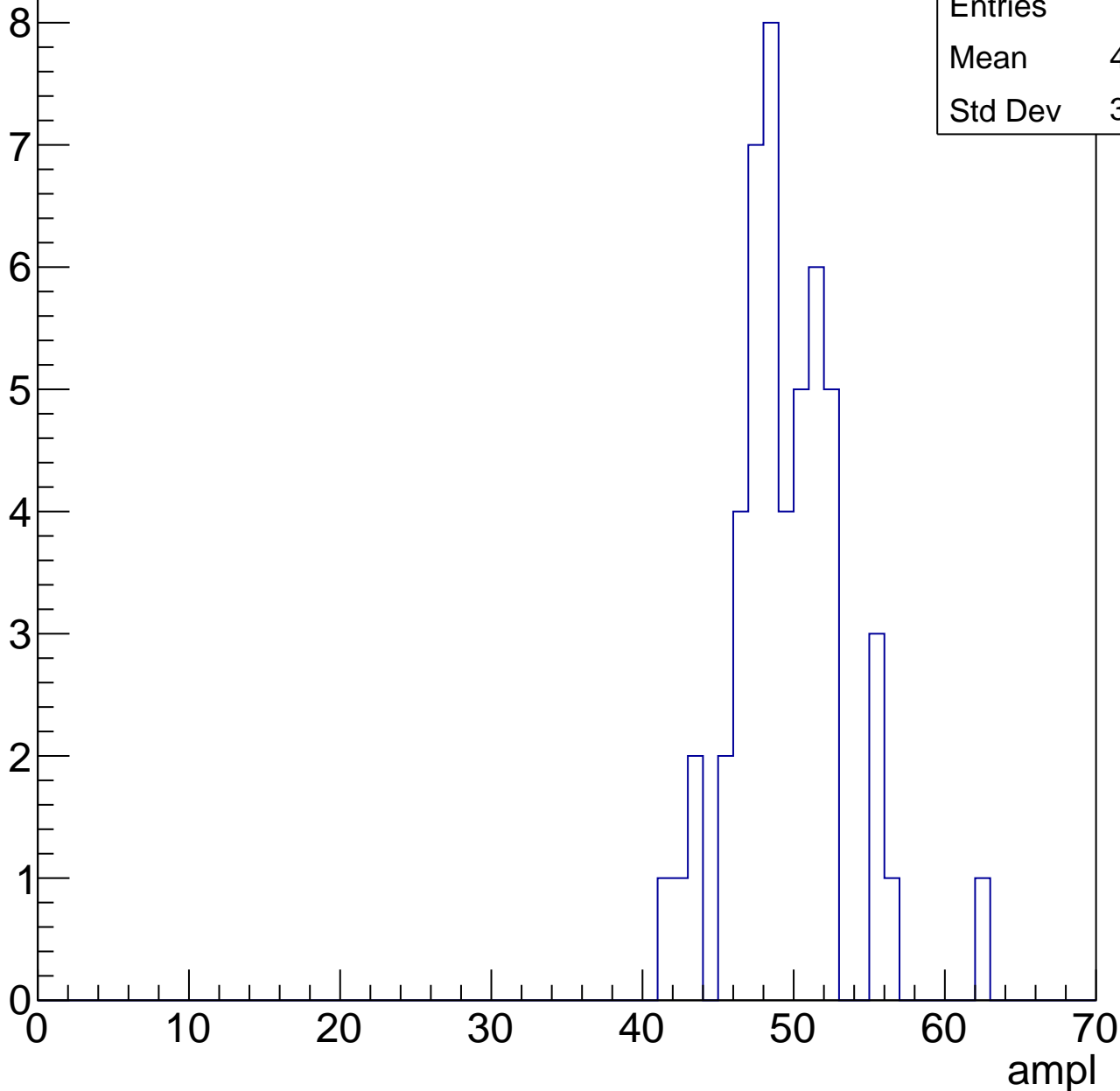


# B1L101S, U18-ch110, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	49.02
Std Dev	3.712

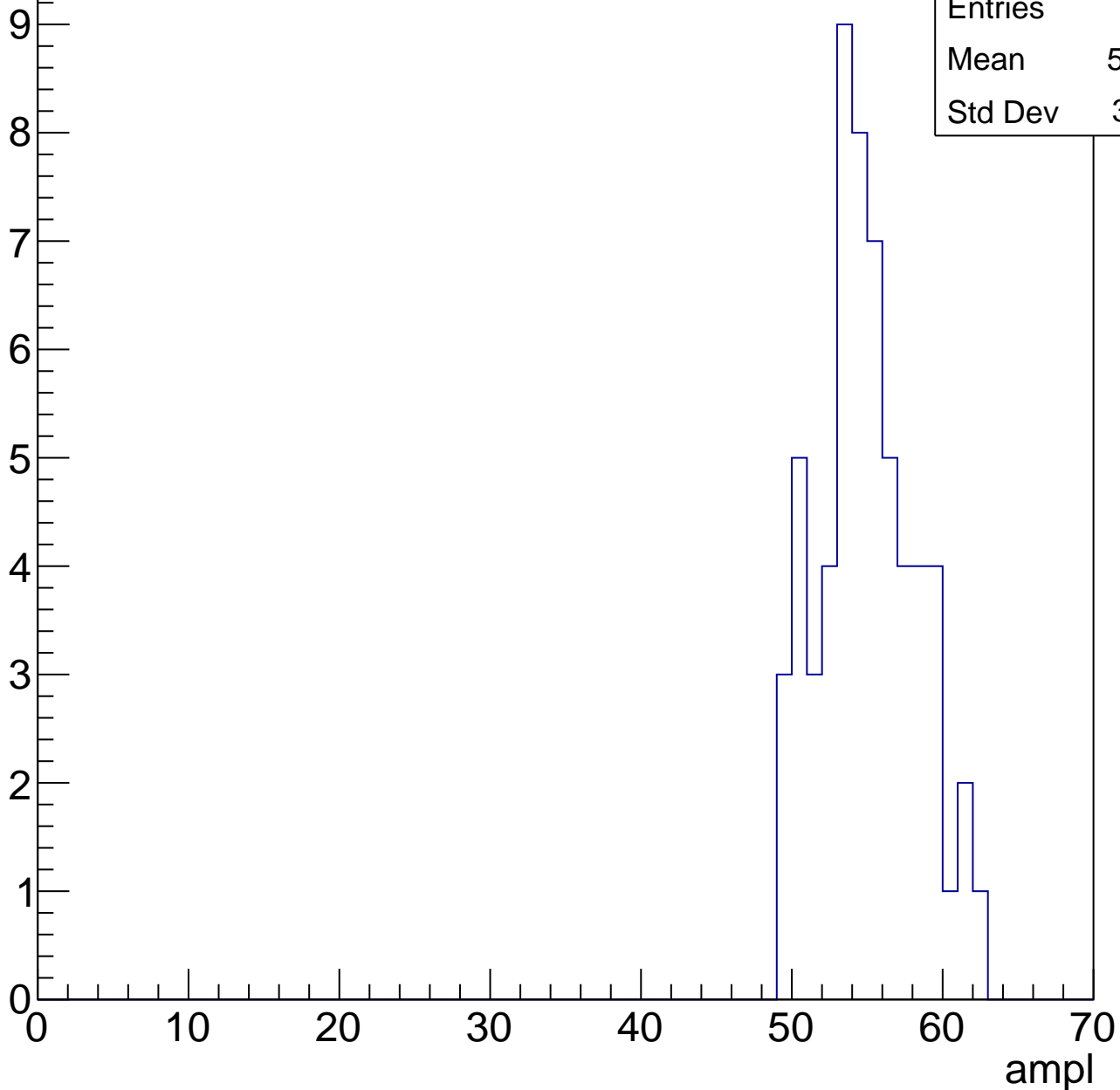


# B1L101S, U18-ch110, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	54.53
Std Dev	3.201

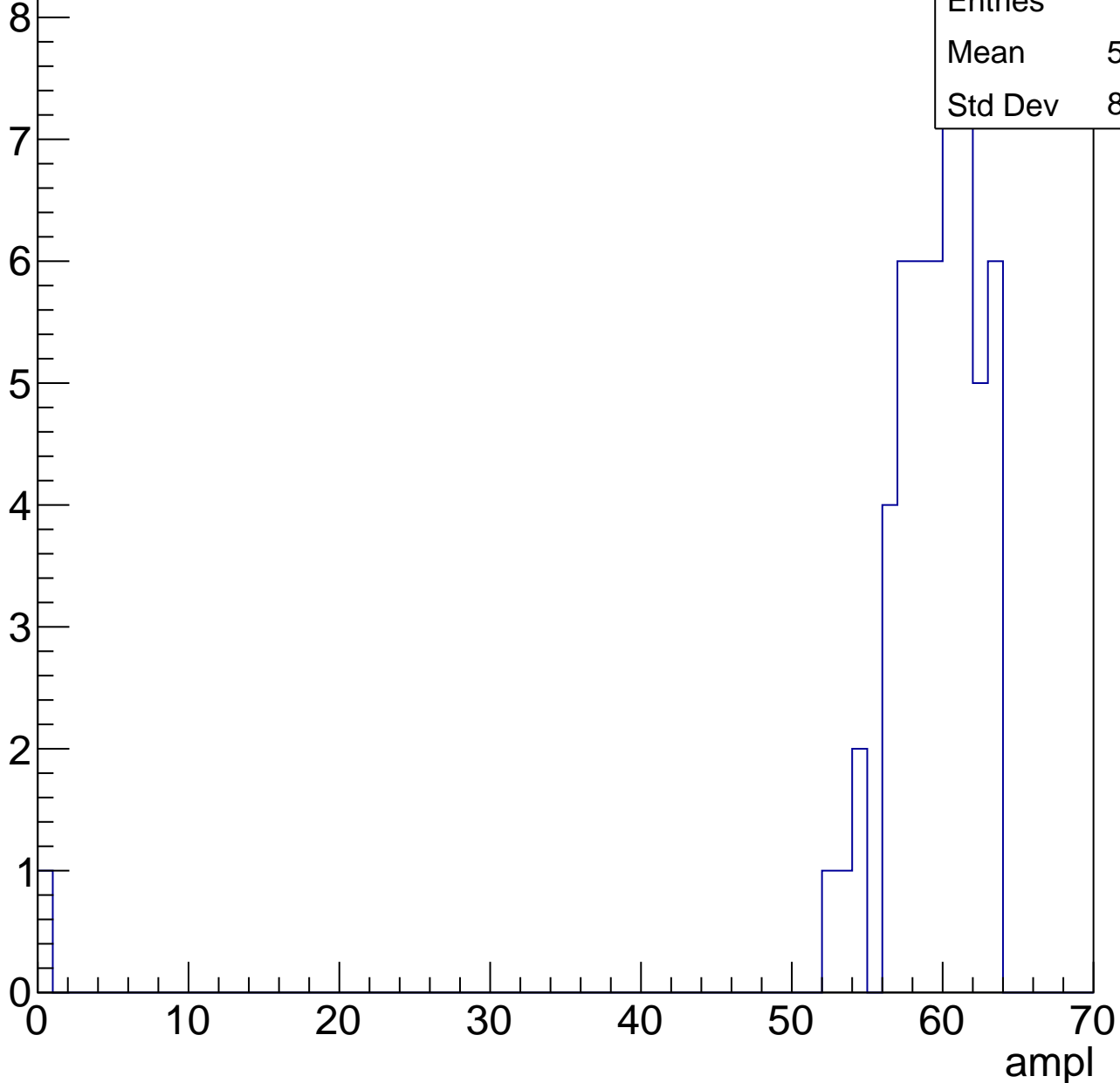


# B1L101S, U18-ch110, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

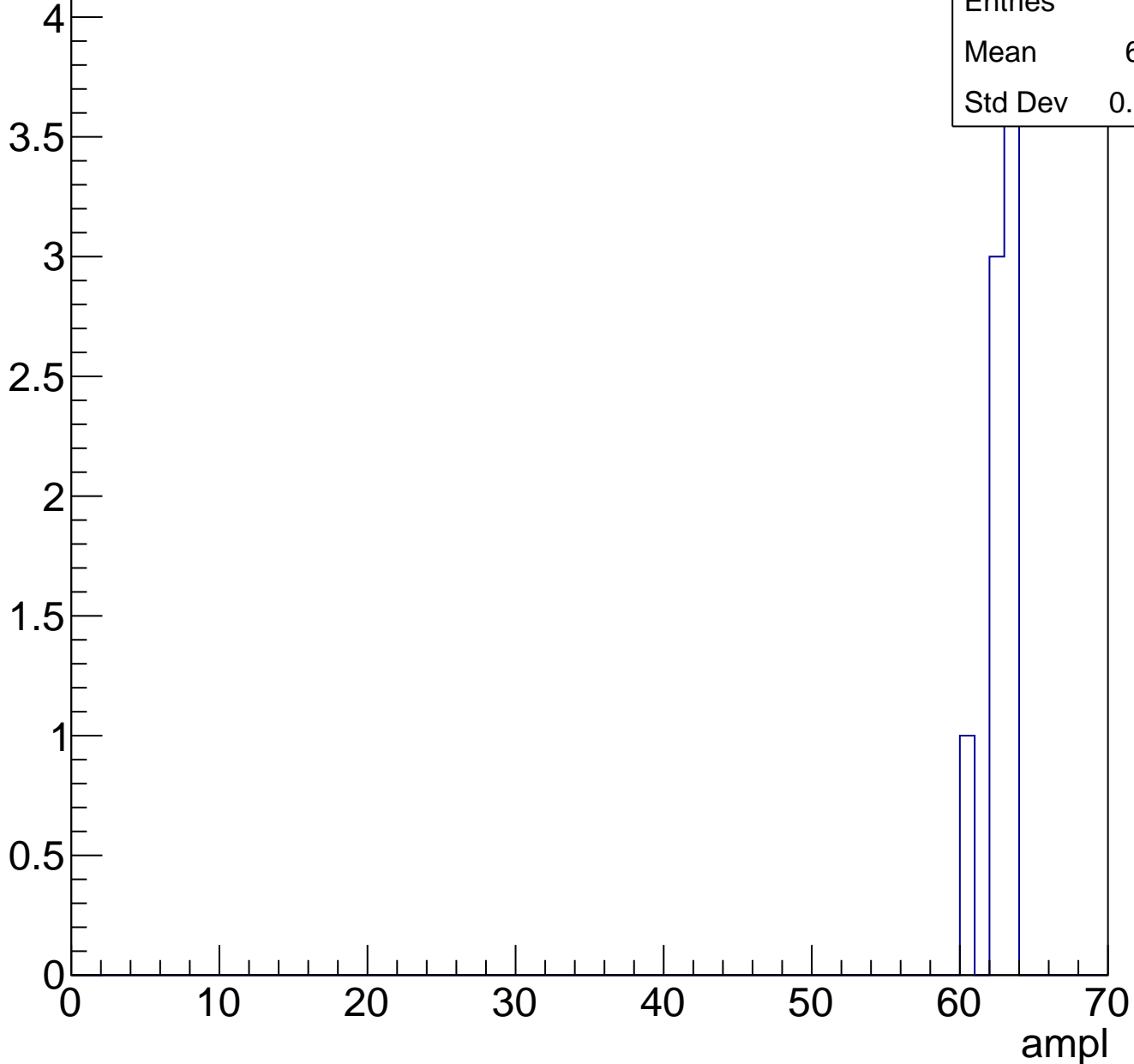
Entries	54
Mean	58.09
Std Dev	8.409



# B1L101S, U18-ch110, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch110, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U18-ch111, adc0

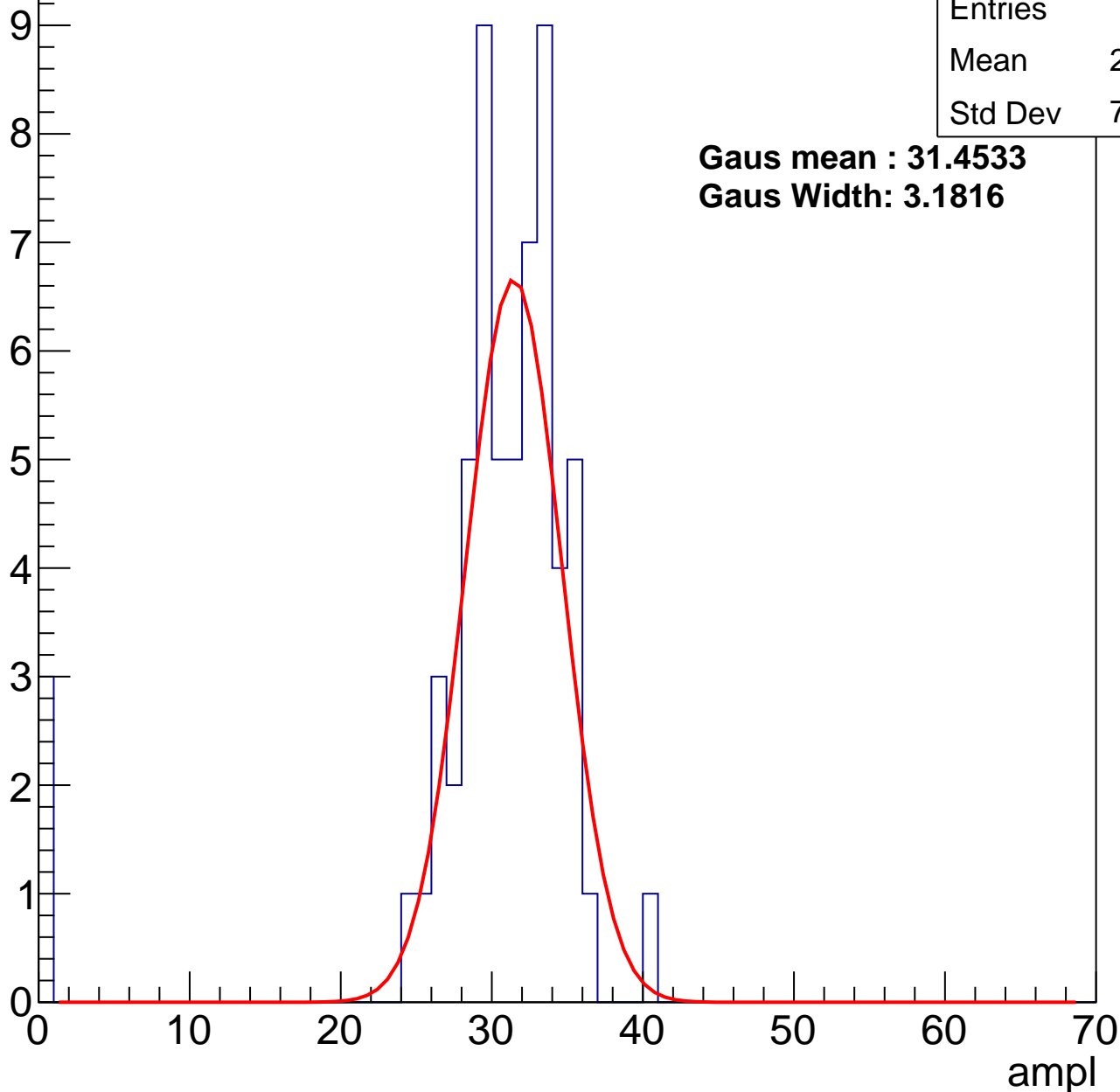
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	29.43
Std Dev	7.327

**Gaus mean : 31.4533**

**Gaus Width: 3.1816**



# B1L101S, U18-ch111, adc1

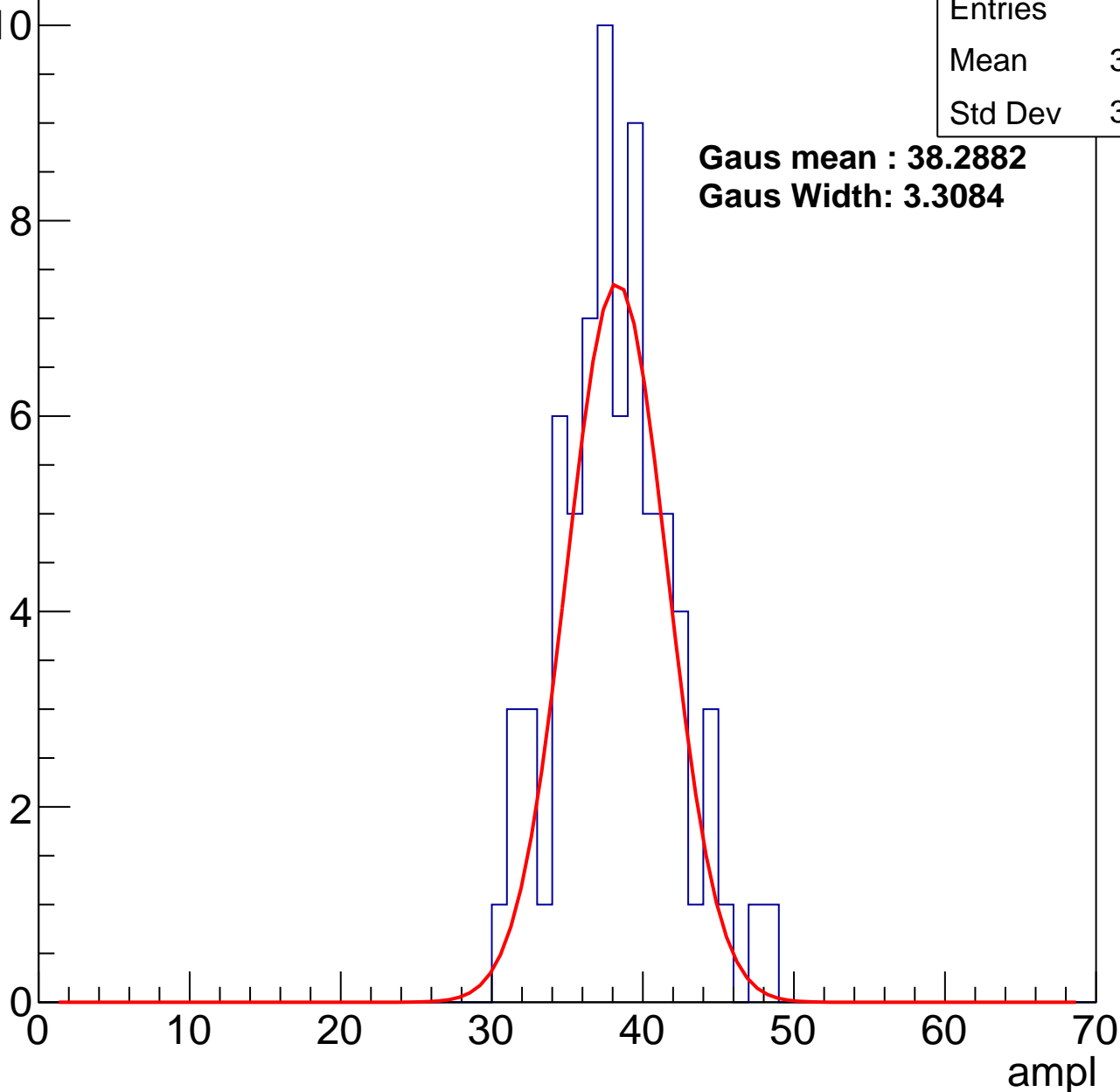
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	37.78
Std Dev	3.765

**Gaus mean : 38.2882**

**Gaus Width: 3.3084**



# B1L101S, U18-ch111, adc2

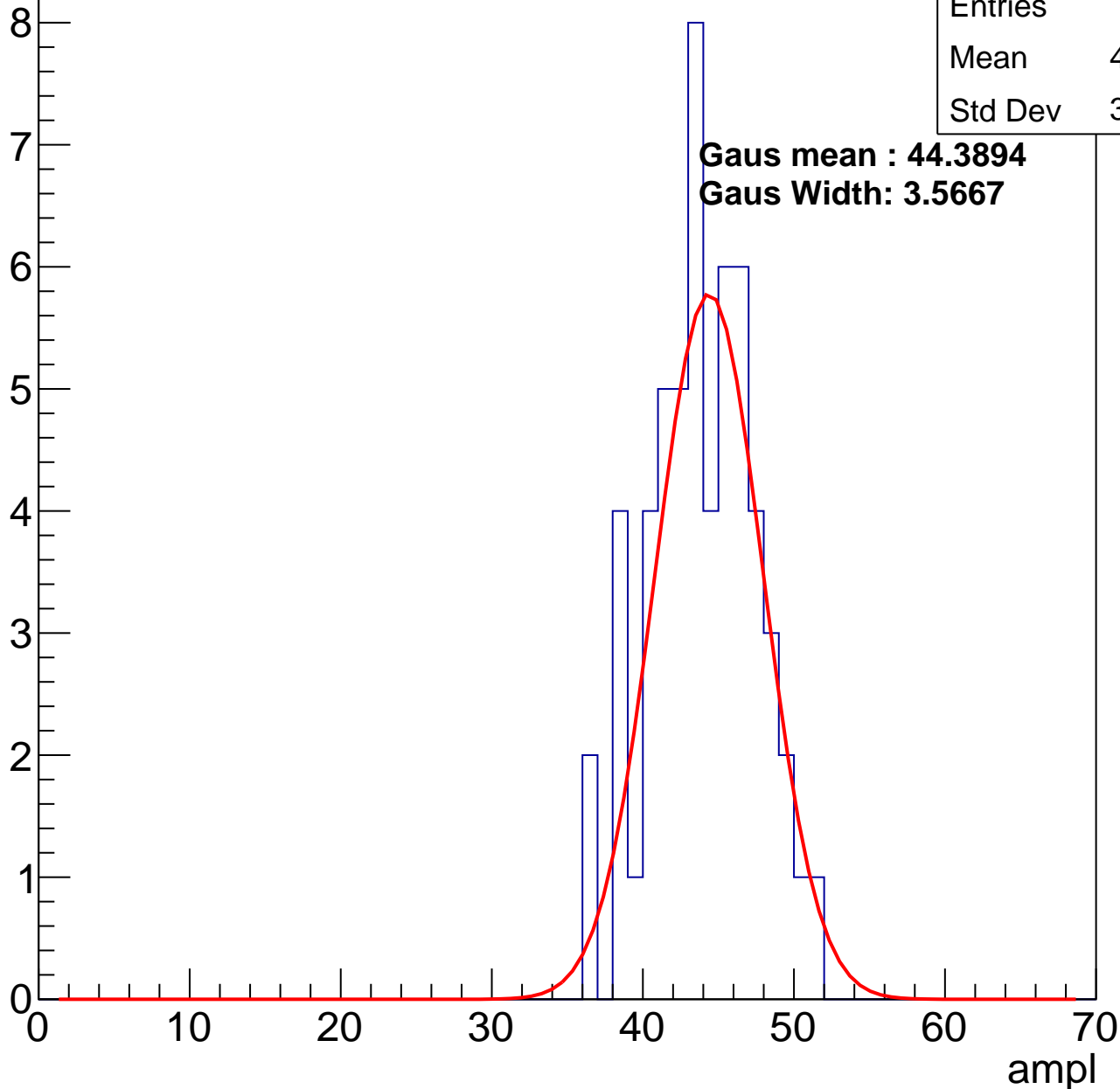
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	43.48
Std Dev	3.454

**Gaus mean : 44.3894**

**Gaus Width: 3.5667**

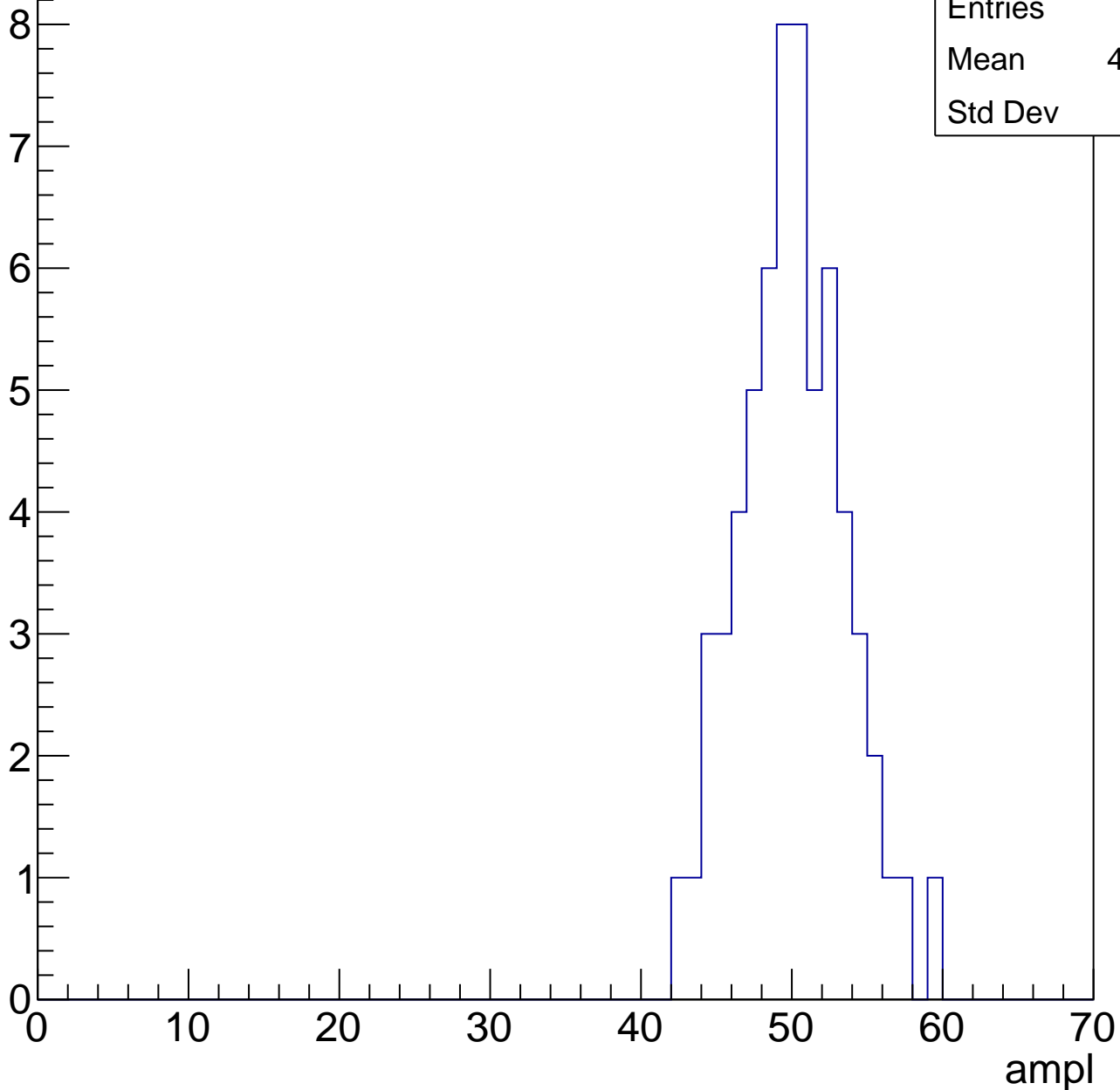


# B1L101S, U18-ch111, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	49.58
Std Dev	3.49

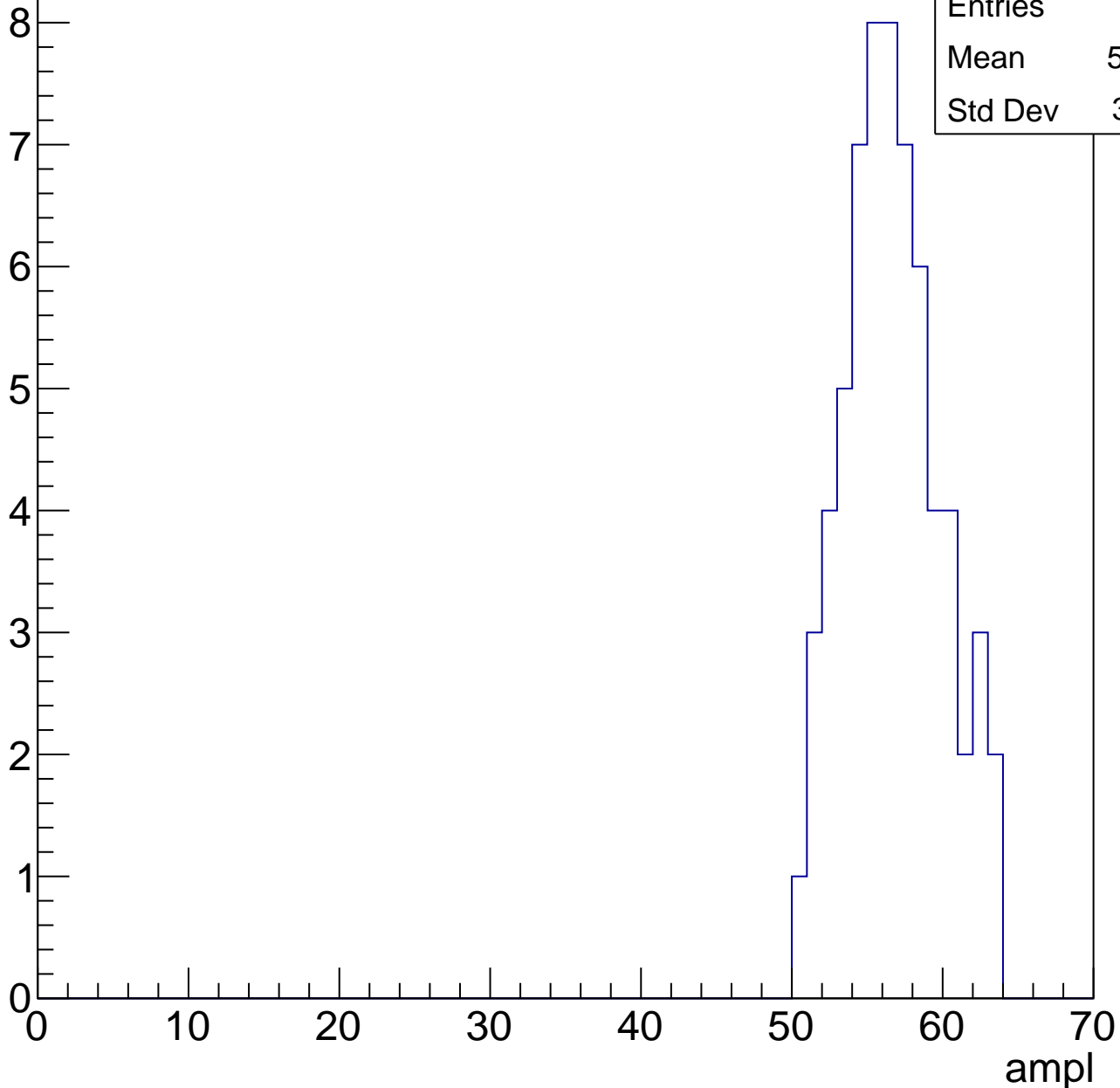


# B1L101S, U18-ch111, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	56.23
Std Dev	3.161

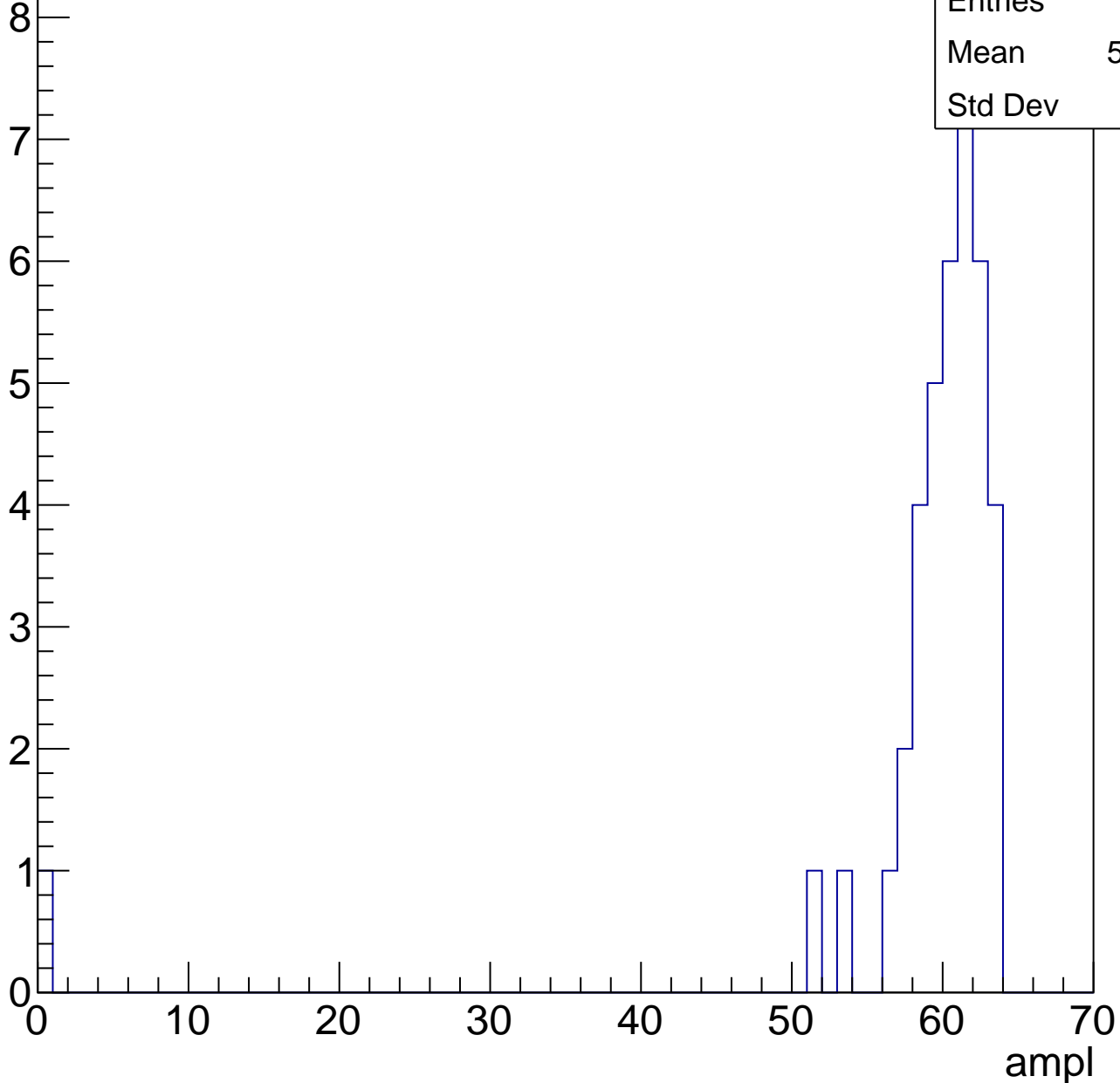


# B1L101S, U18-ch111, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	39
Mean	58.28
Std Dev	9.79



# B1L101S, U18-ch111, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch111, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U18-ch112, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	86
Mean	28.37
Std Dev	6.686

**Gaus mean : 29.9003**

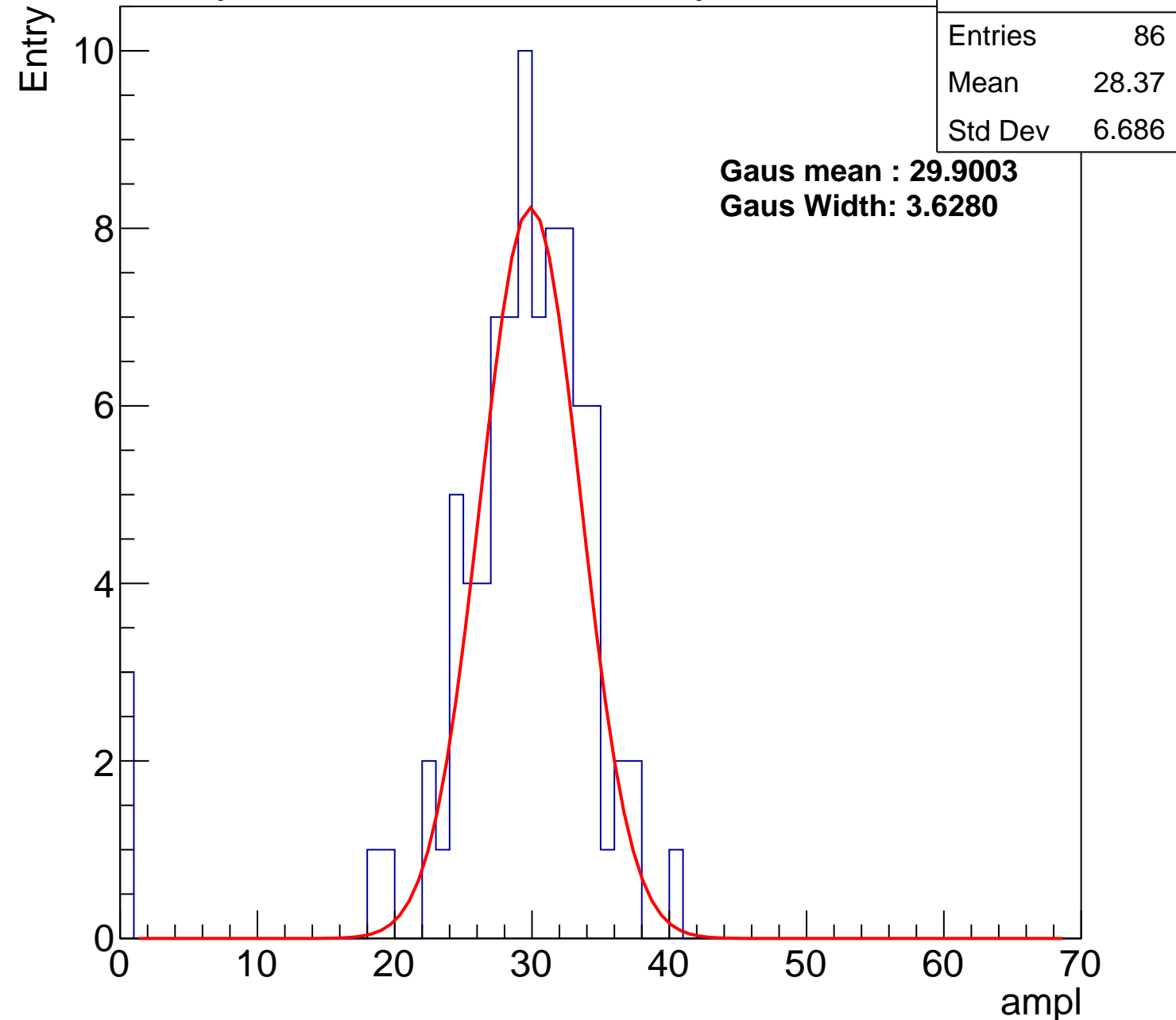
**Gaus Width: 3.6280**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U18-ch112, adc1

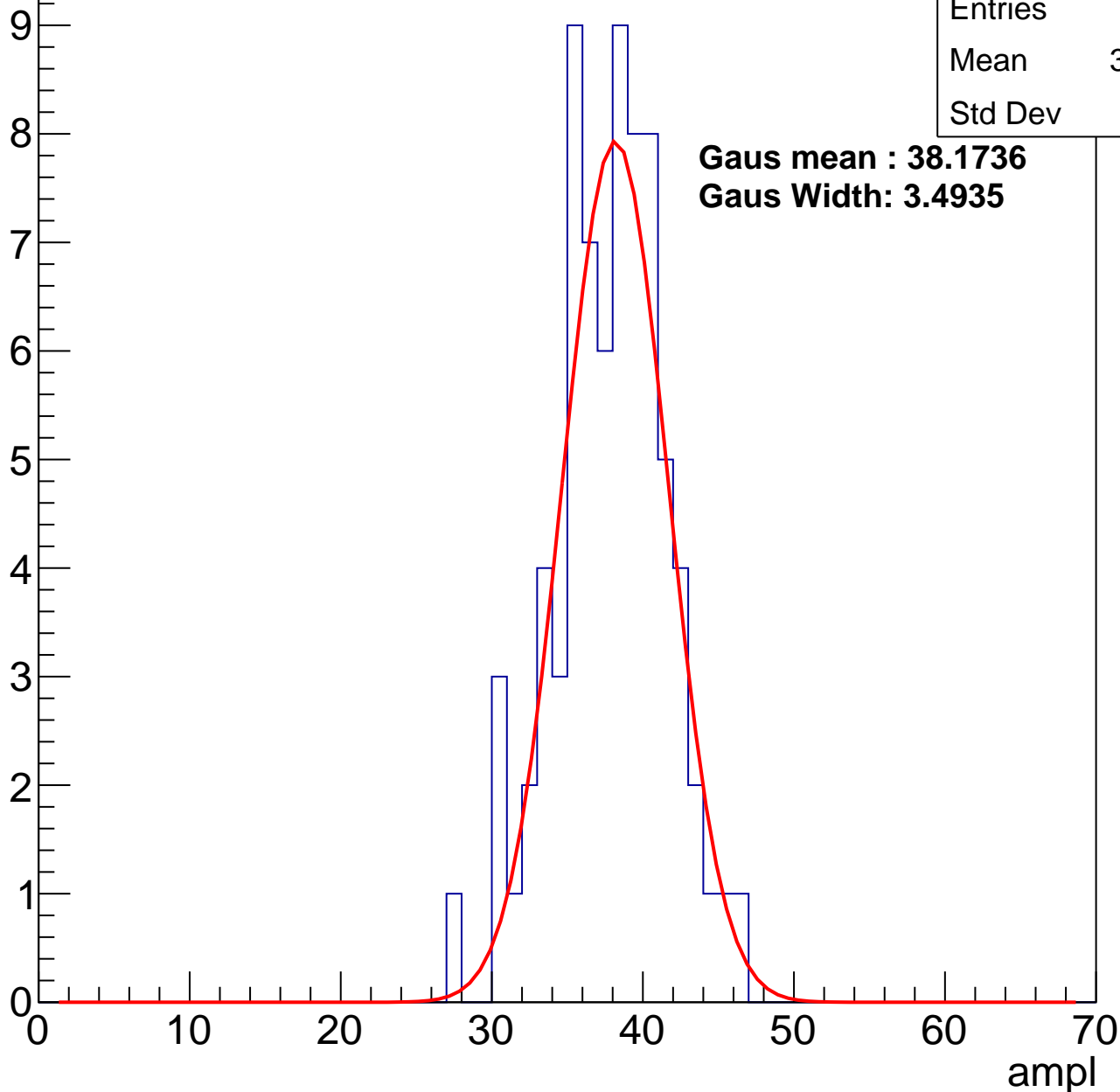
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	37.37
Std Dev	3.68

**Gaus mean : 38.1736**

**Gaus Width: 3.4935**



# B1L101S, U18-ch112, adc2

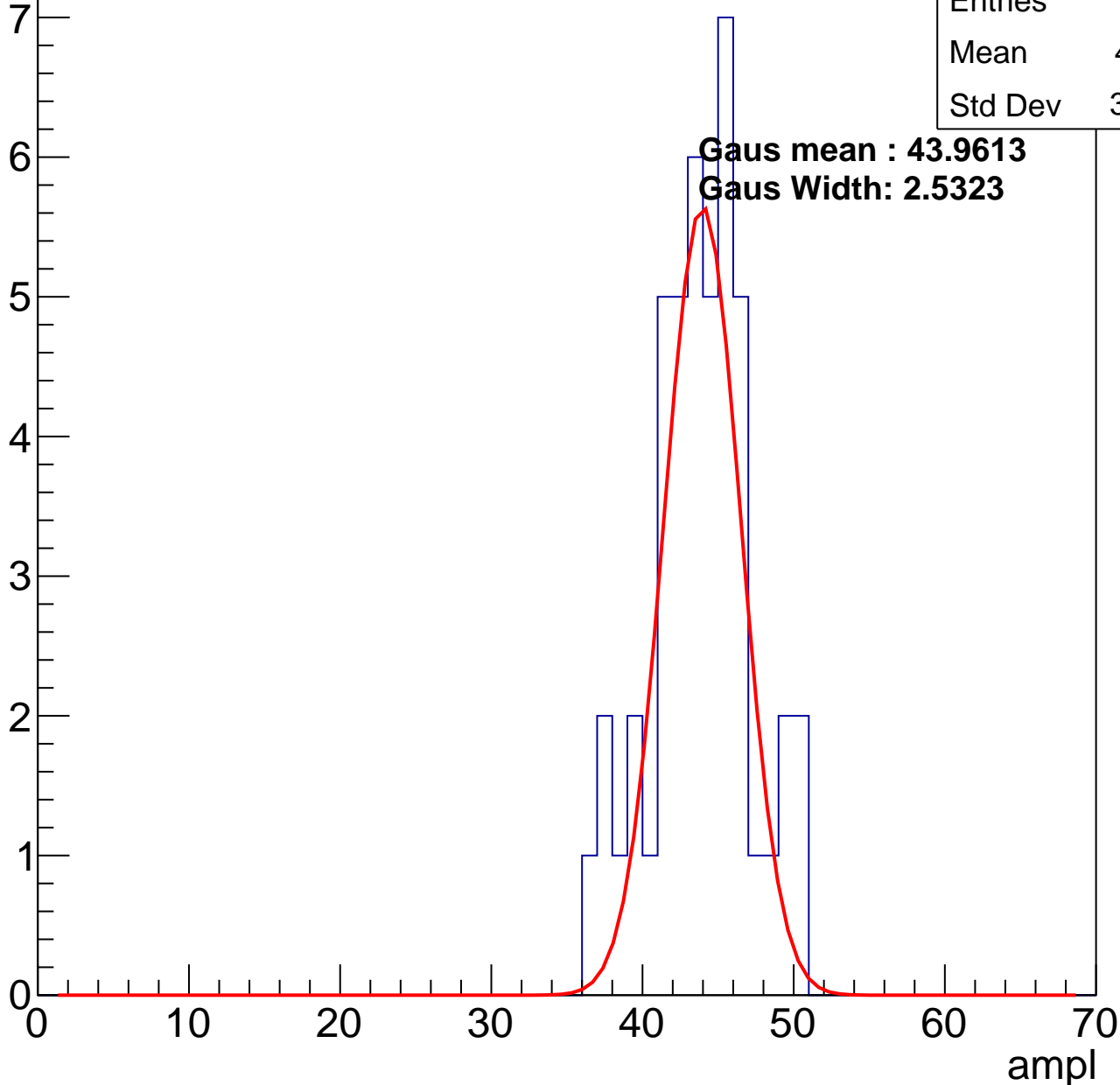
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	46
Mean	43.41
Std Dev	3.274

**Gaus mean : 43.9613**

**Gaus Width: 2.5323**

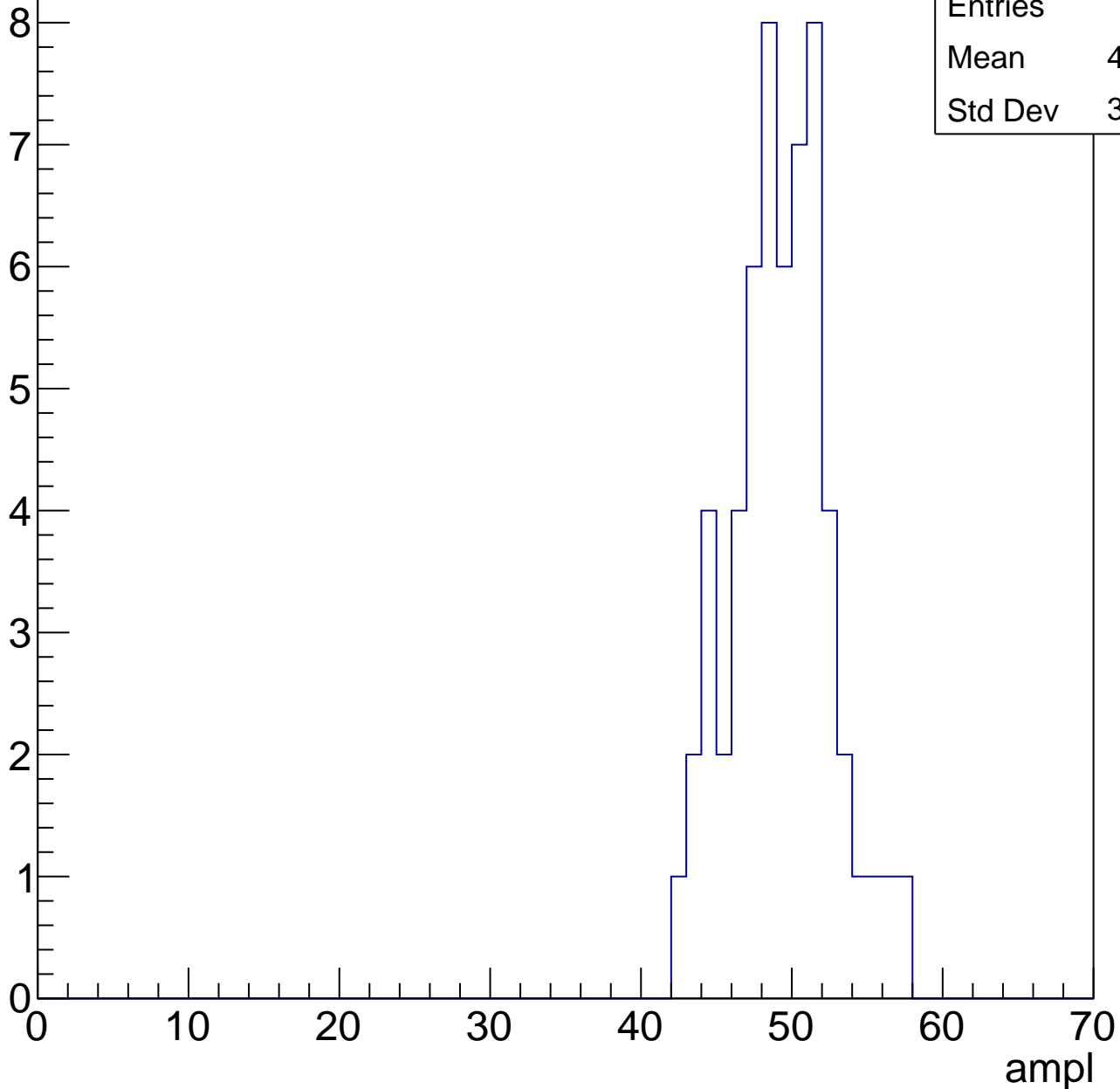


# B1L101S, U18-ch112, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	48.83
Std Dev	3.217

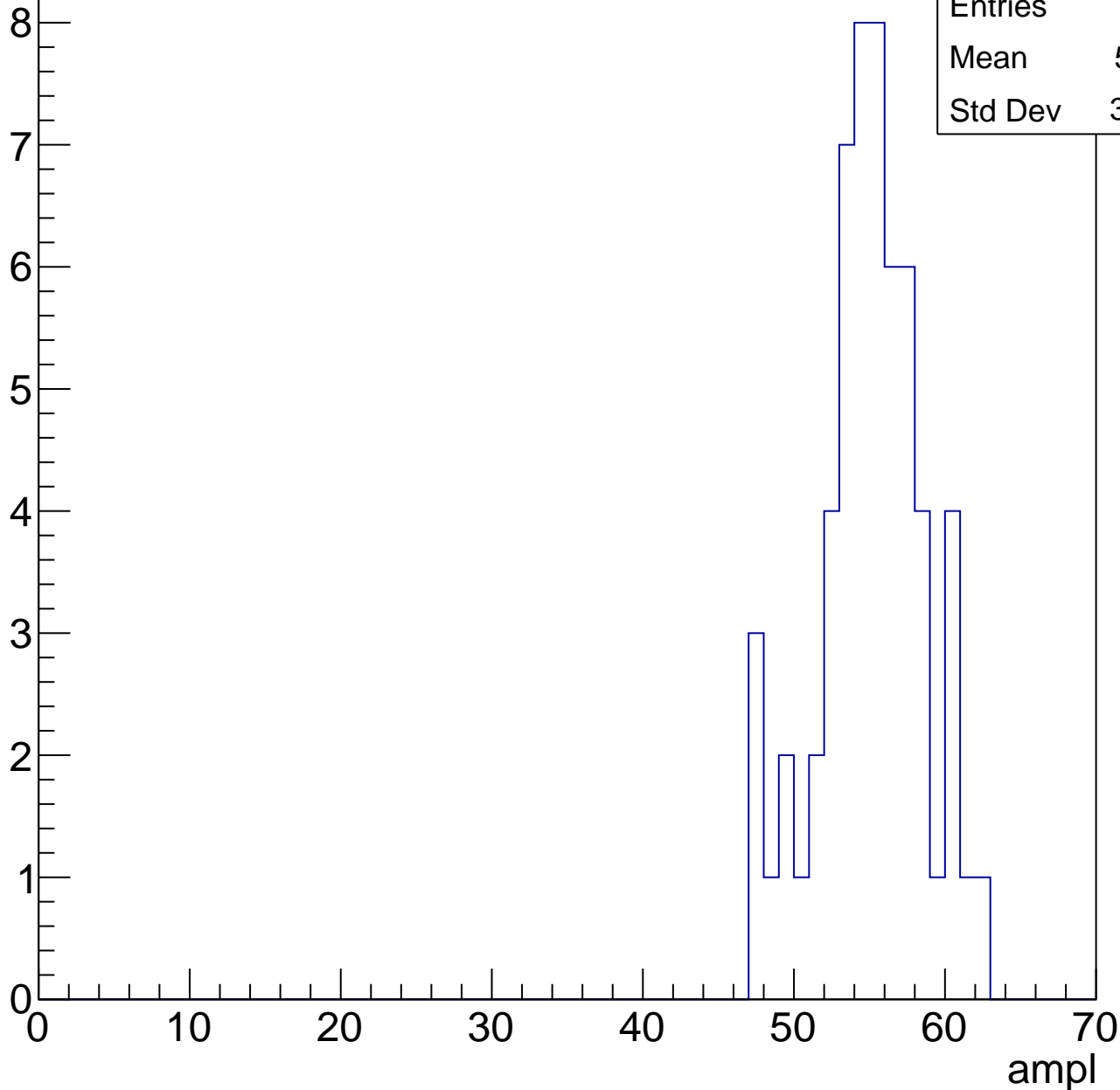


# B1L101S, U18-ch112, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	54.61
Std Dev	3.445

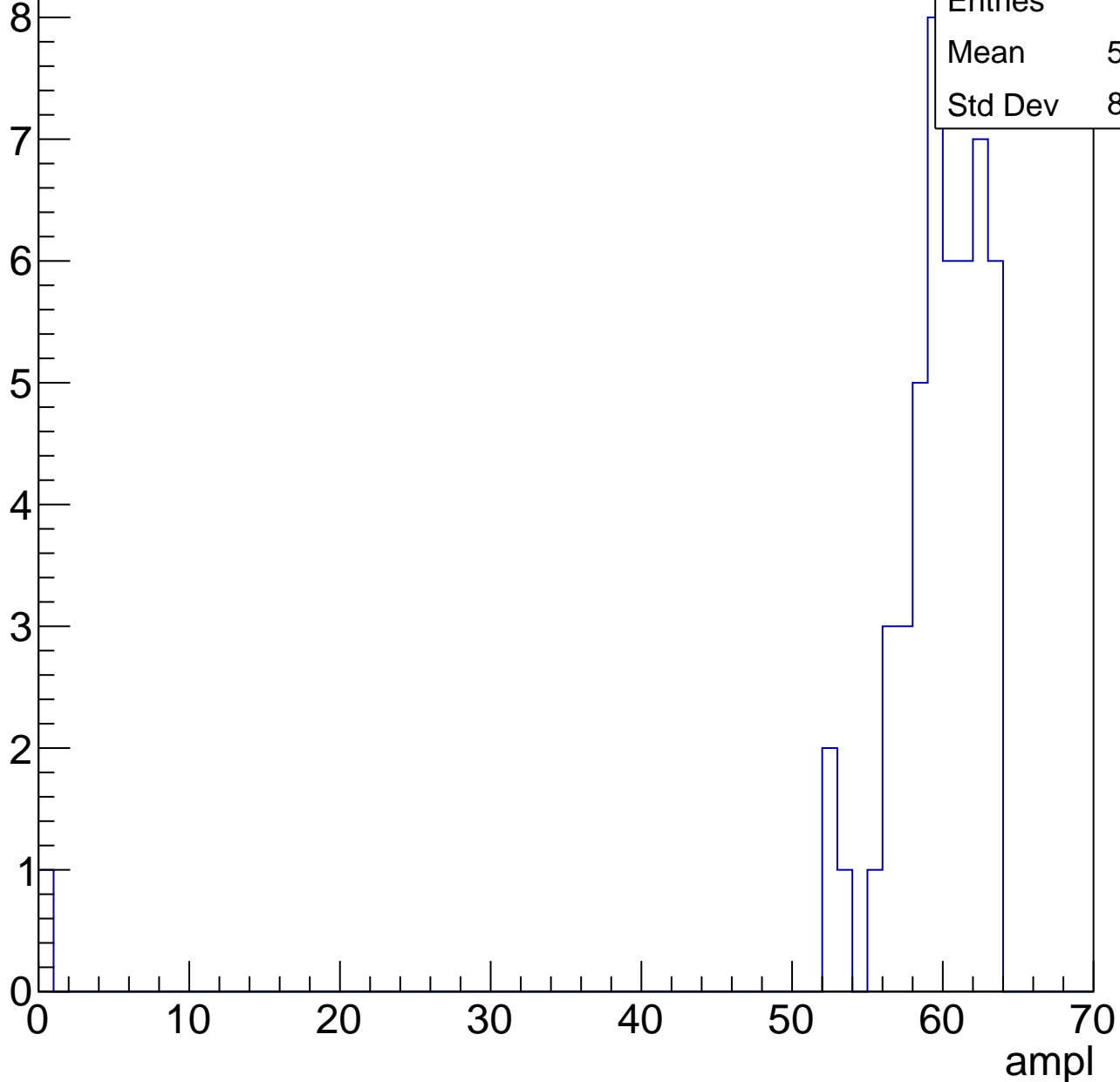


# B1L101S, U18-ch112, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

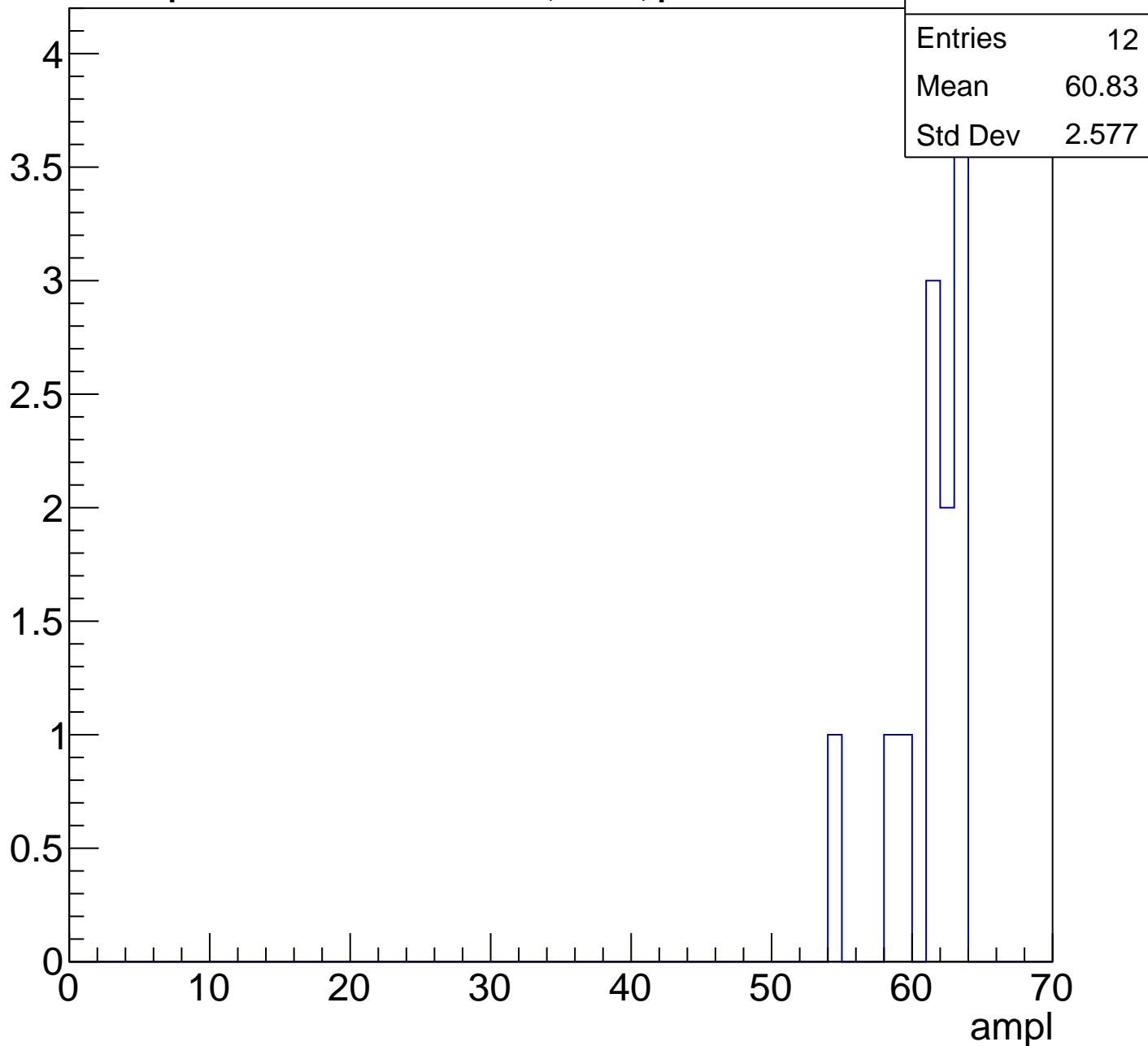
Entries	49
Mean	58.18
Std Dev	8.843



# B1L101S, U18-ch112, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch112, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch113, adc0

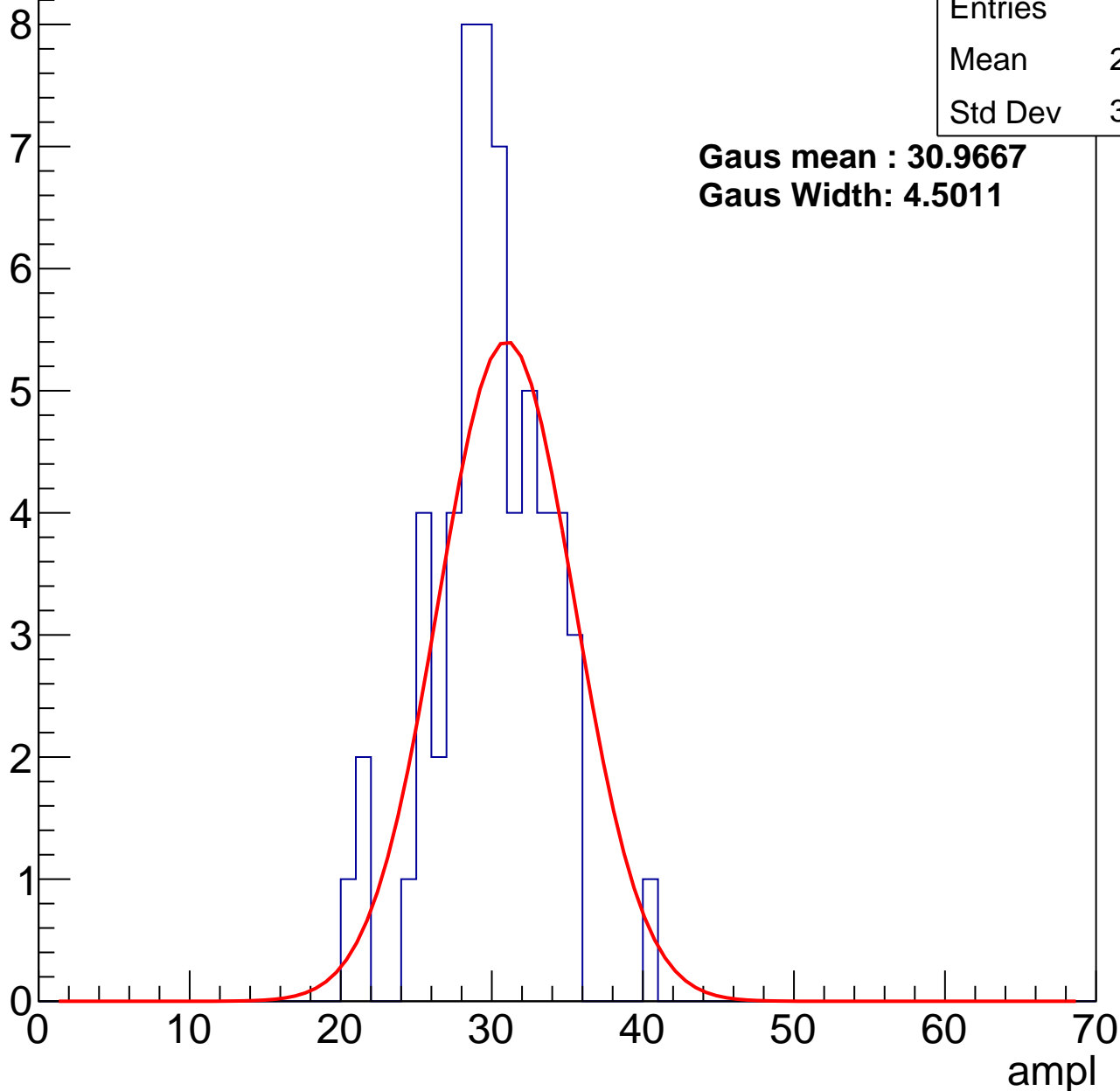
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	29.47
Std Dev	3.687

**Gaus mean : 30.9667**

**Gaus Width: 4.5011**



# B1L101S, U18-ch113, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	77
Mean	36.22
Std Dev	3.761

**Gaus mean : 36.8894**

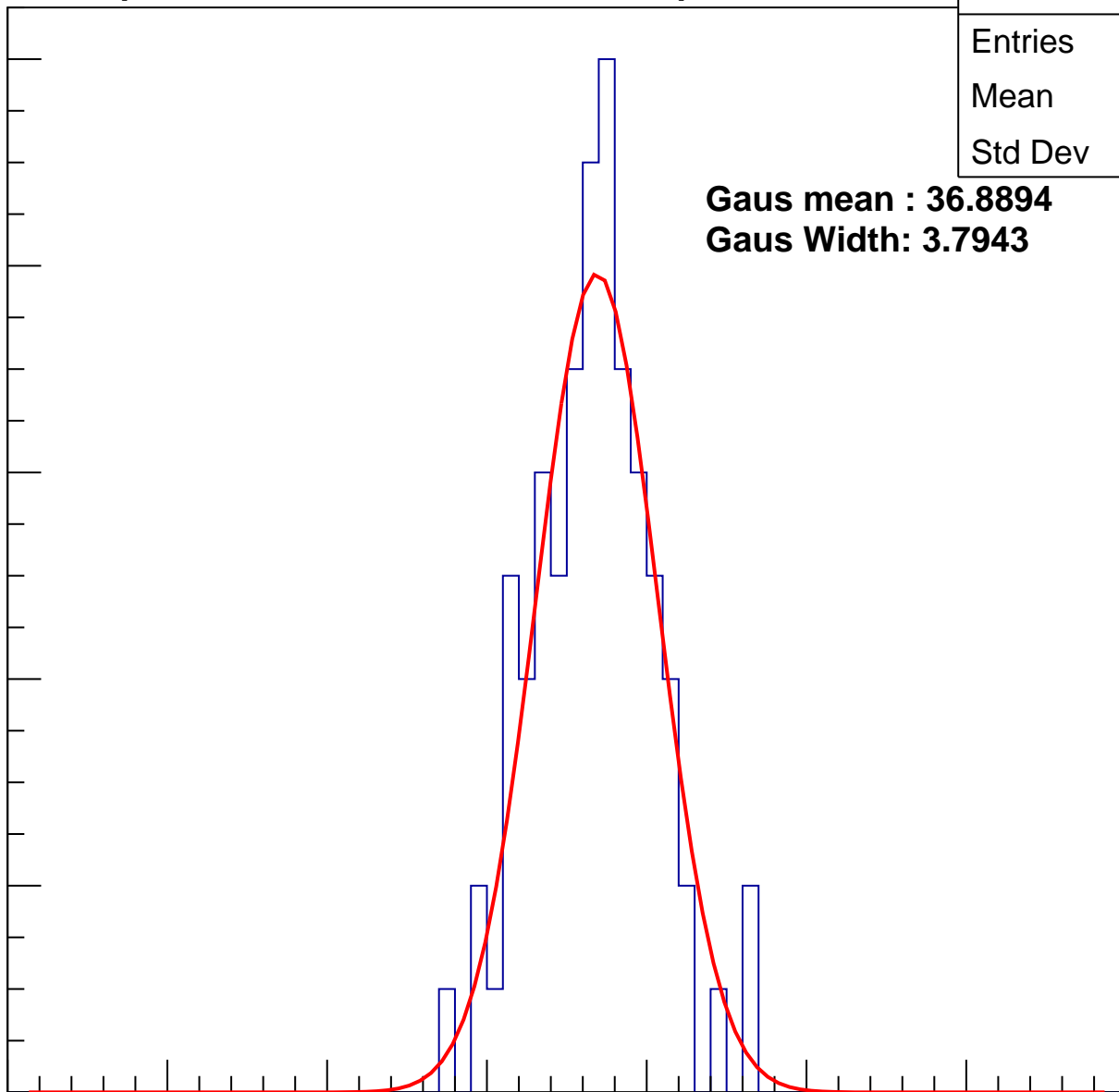
**Gaus Width: 3.7943**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L101S, U18-ch113, adc2

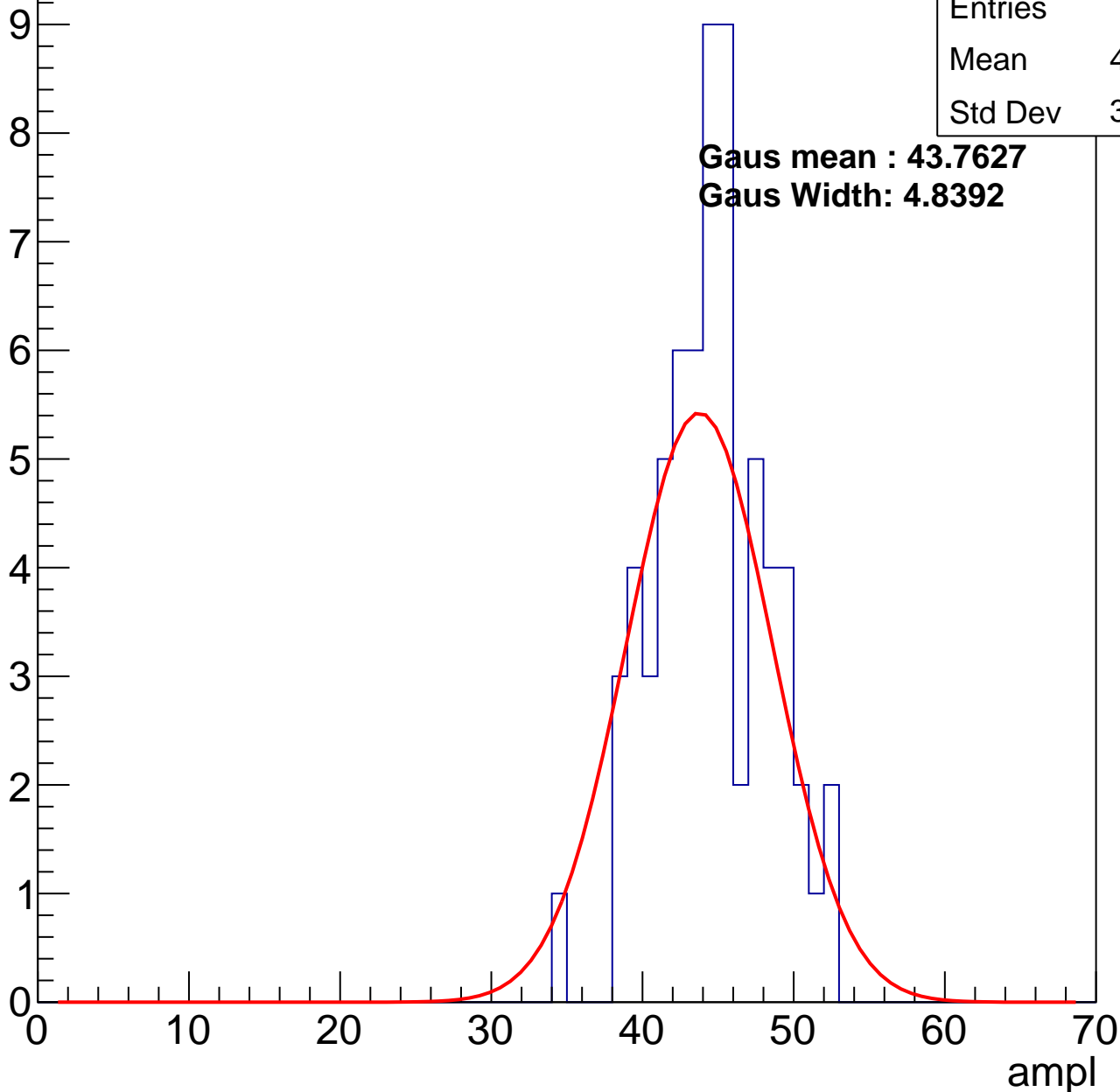
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	44.09
Std Dev	3.704

**Gaus mean : 43.7627**

**Gaus Width: 4.8392**

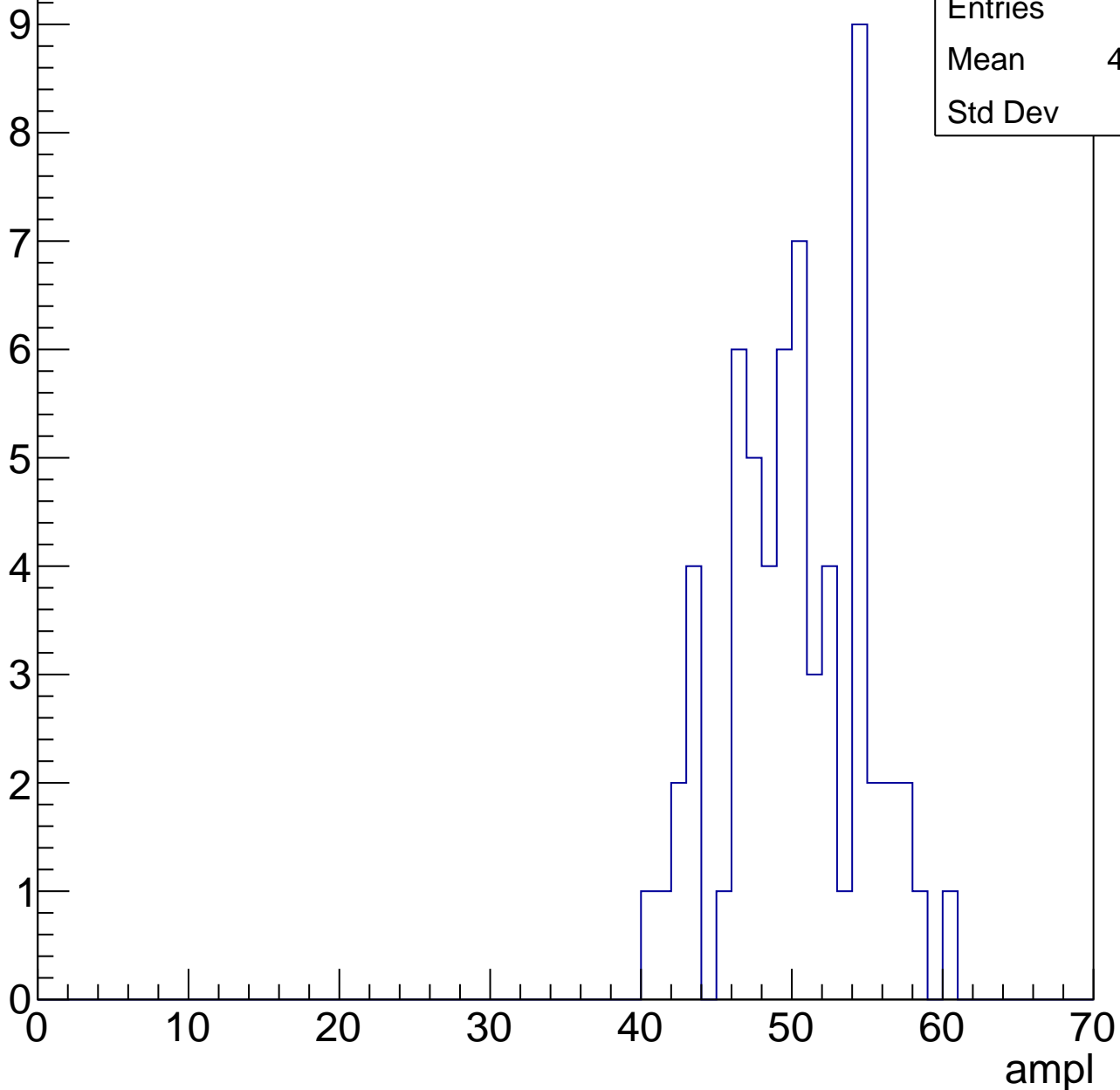


# B1L101S, U18-ch113, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	49.73
Std Dev	4.48

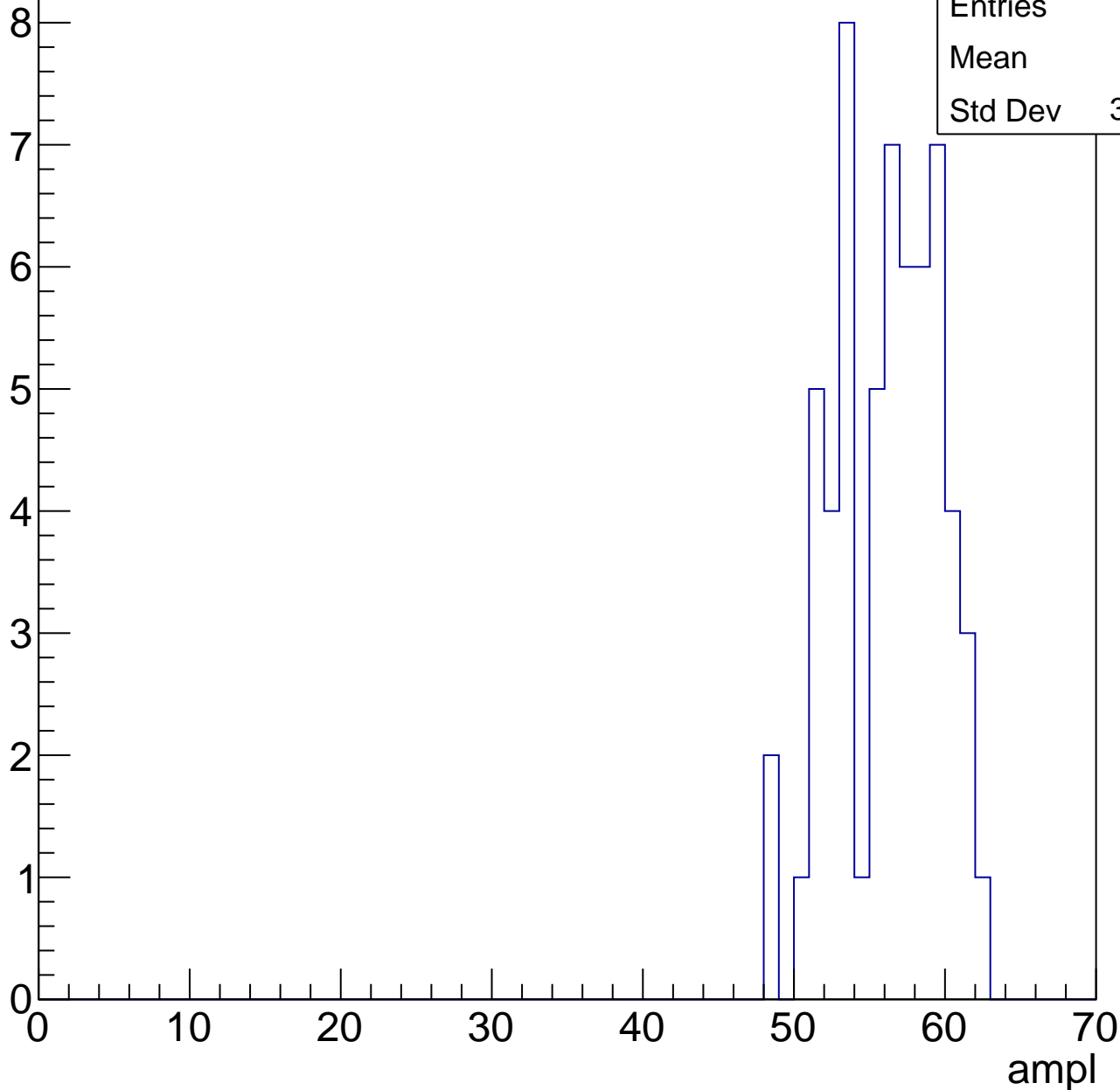


# B1L101S, U18-ch113, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	55.7
Std Dev	3.407

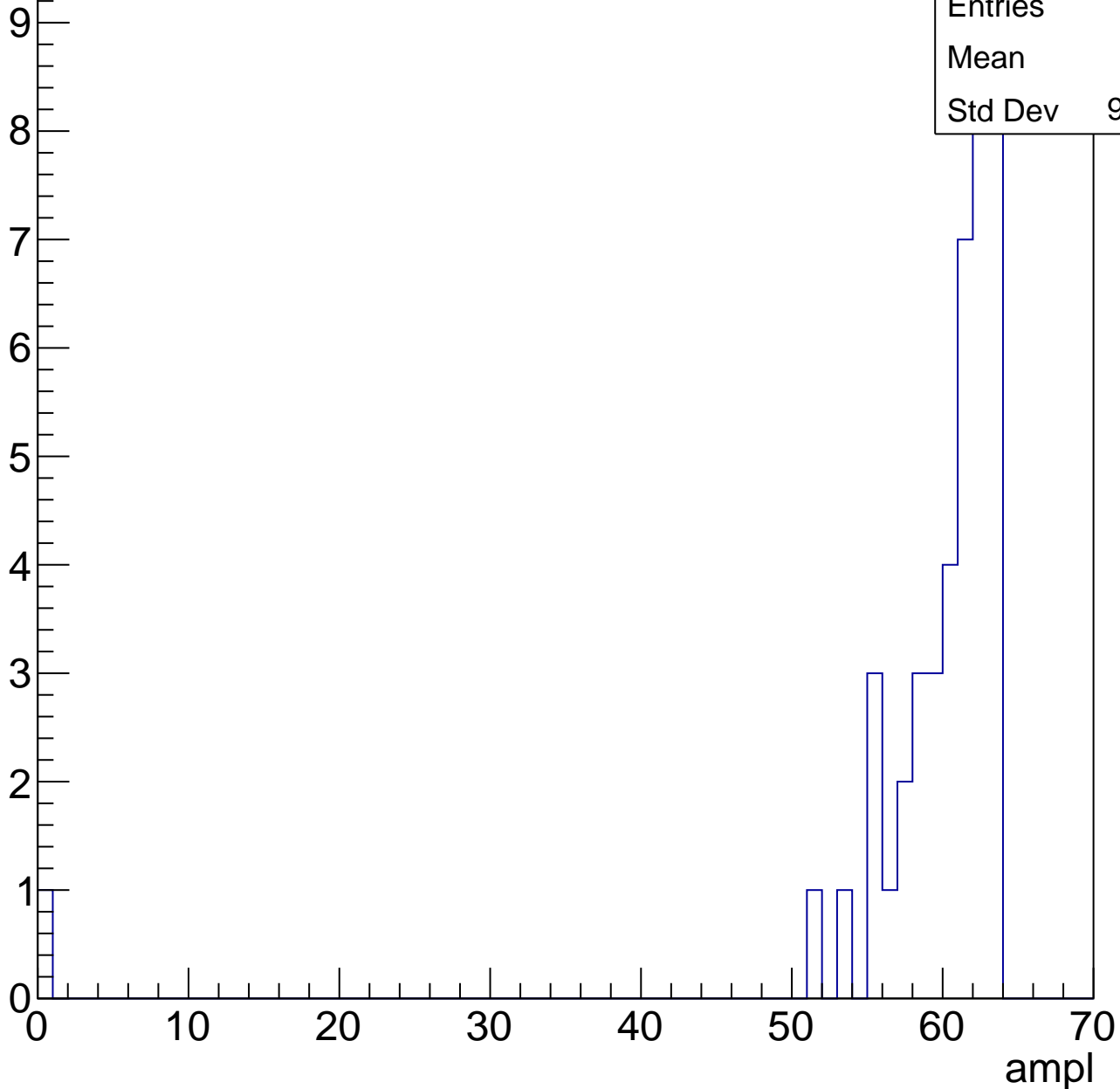


# B1L101S, U18-ch113, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	43
Mean	58.6
Std Dev	9.512



# B1L101S, U18-ch113, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch113, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U18-ch114, adc0

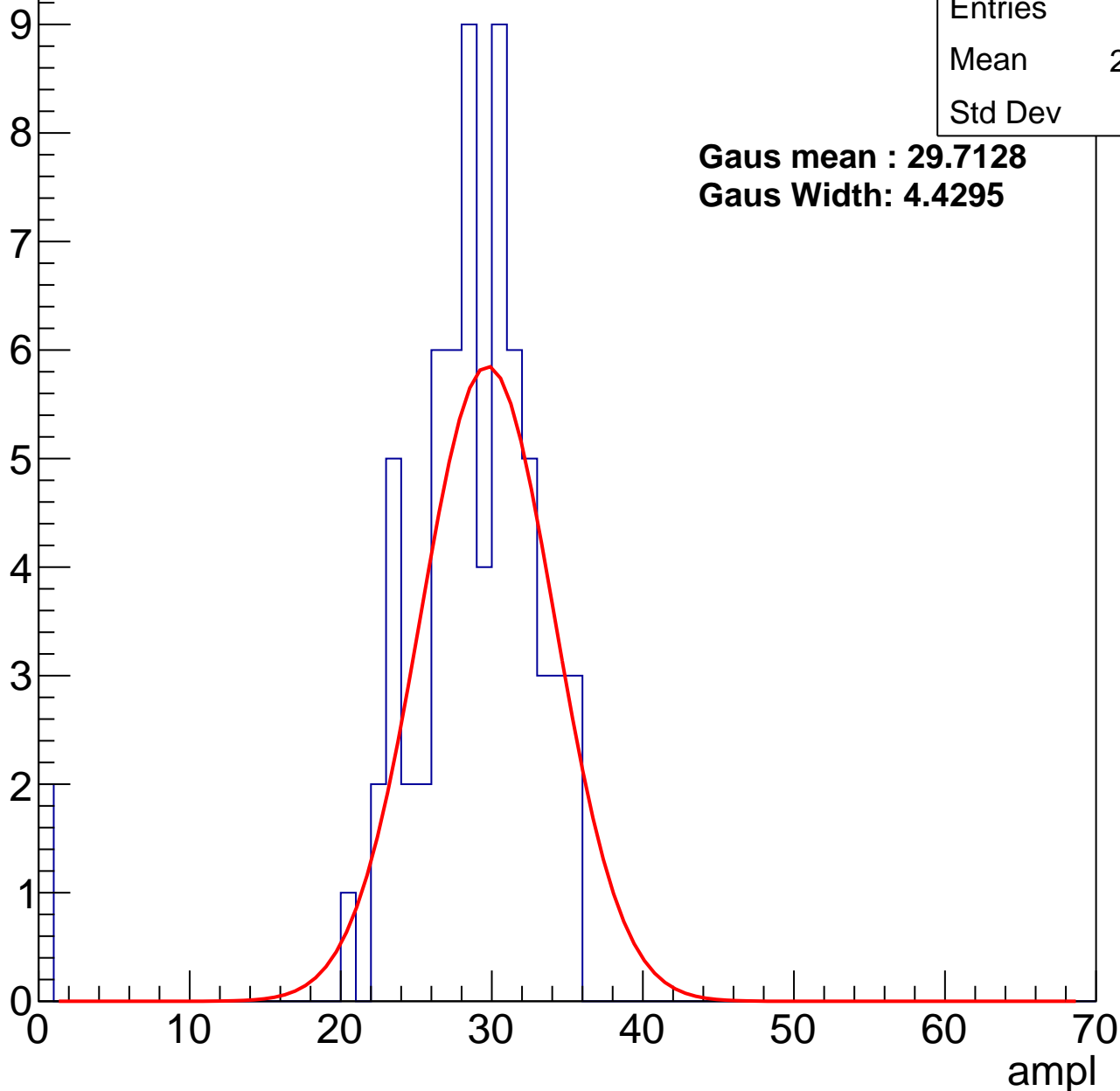
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	27.72
Std Dev	5.95

**Gaus mean : 29.7128**

**Gaus Width: 4.4295**



# B1L101S, U18-ch114, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	75
Mean	35.84
Std Dev	5.502

**Gaus mean : 36.5280**

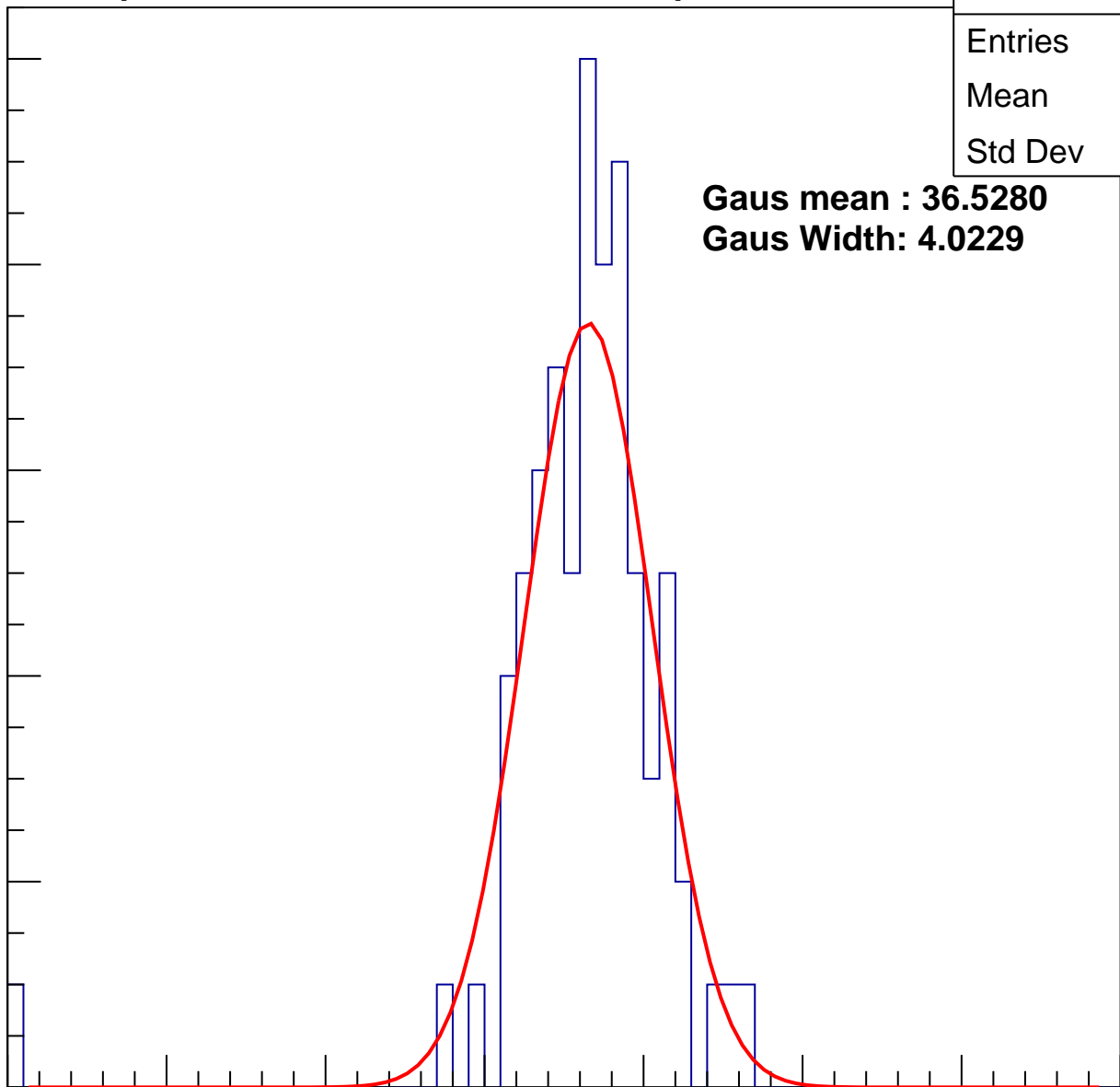
**Gaus Width: 4.0229**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U18-ch114, adc2

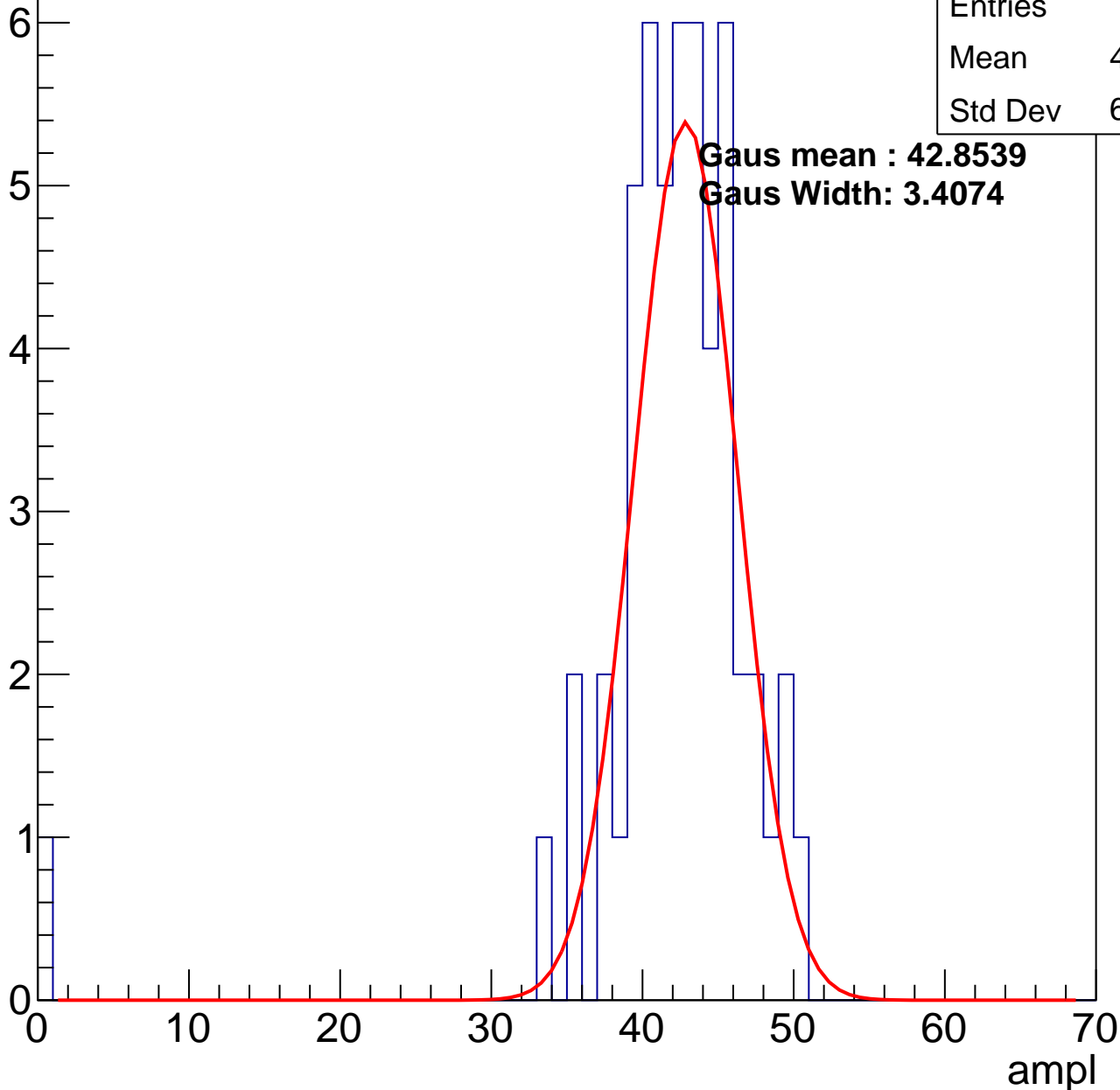
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	41.38
Std Dev	6.755

**Gaus mean : 42.8539**

**Gaus Width: 3.4074**

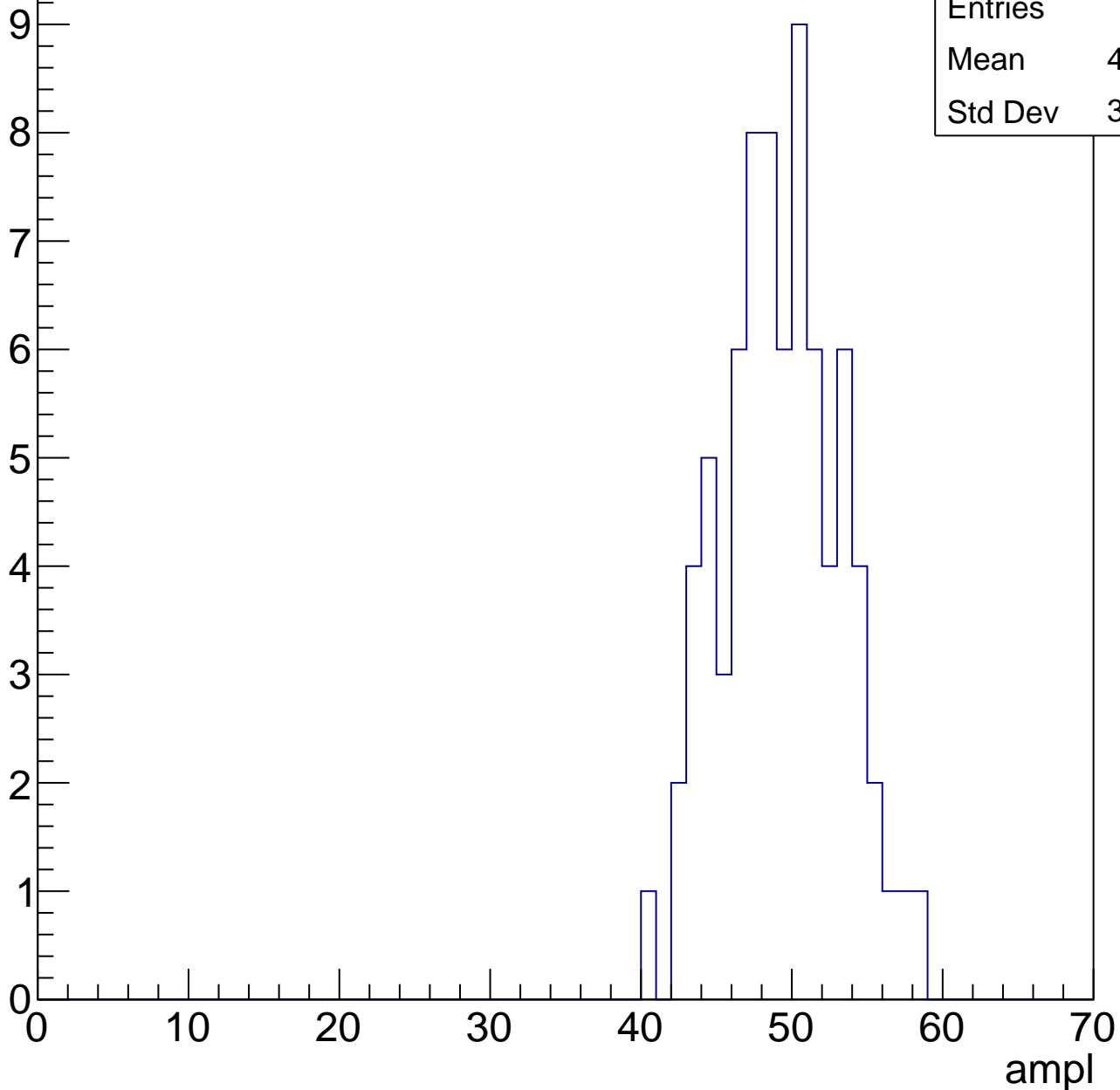


# B1L101S, U18-ch114, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	48.83
Std Dev	3.812

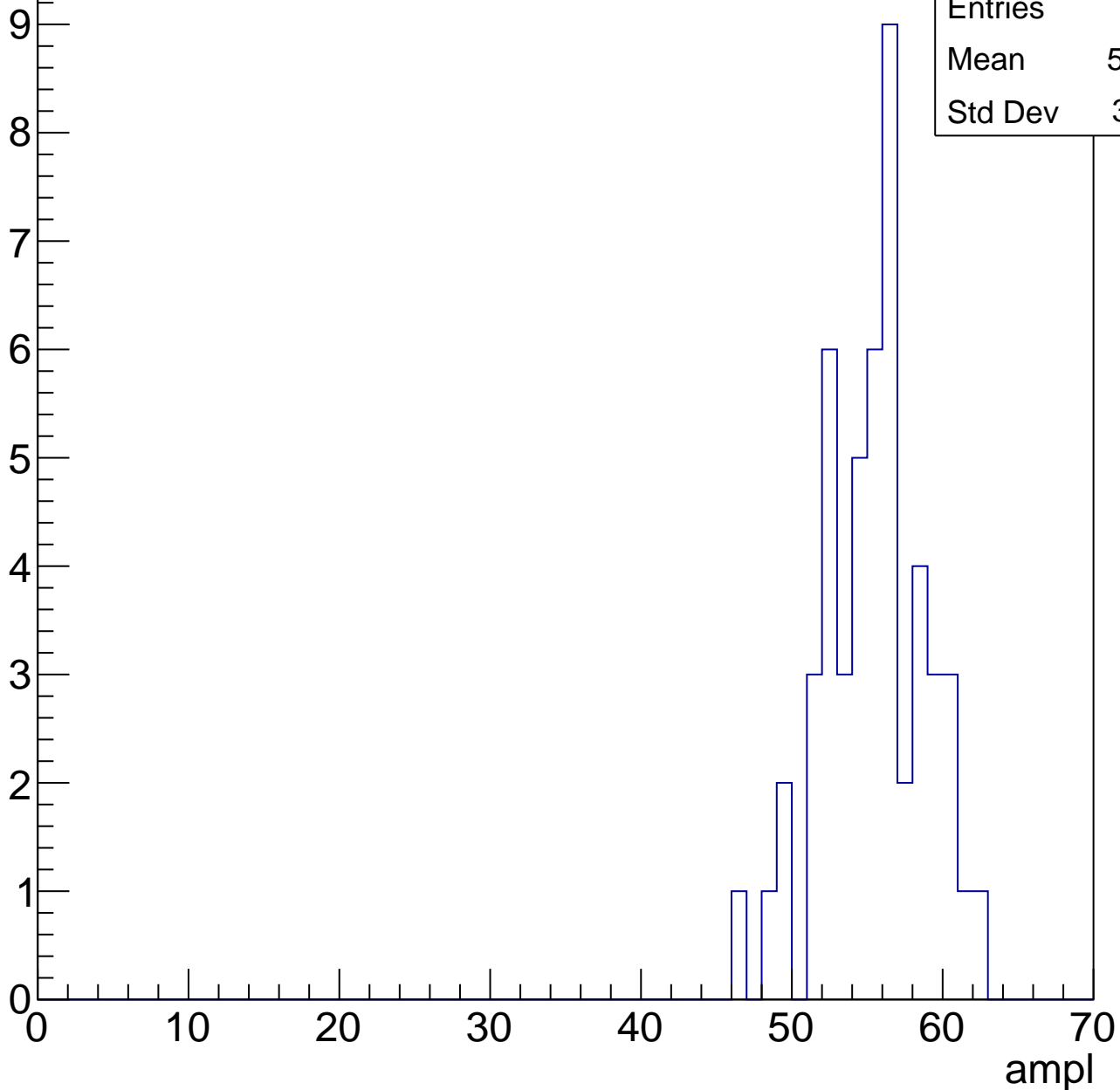


# B1L101S, U18-ch114, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	54.92
Std Dev	3.411

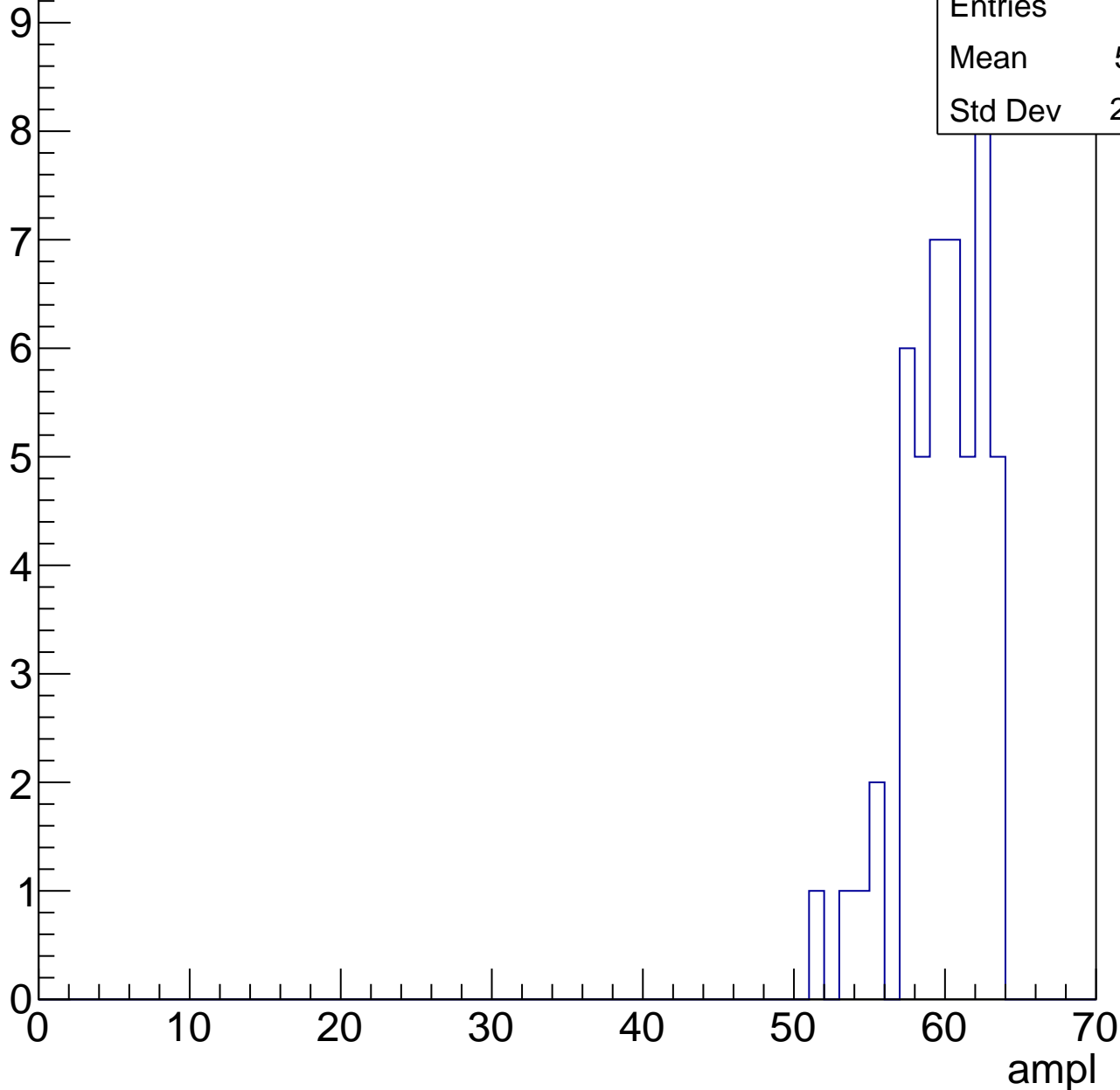


# B1L101S, U18-ch114, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	49
Mean	59.41
Std Dev	2.732

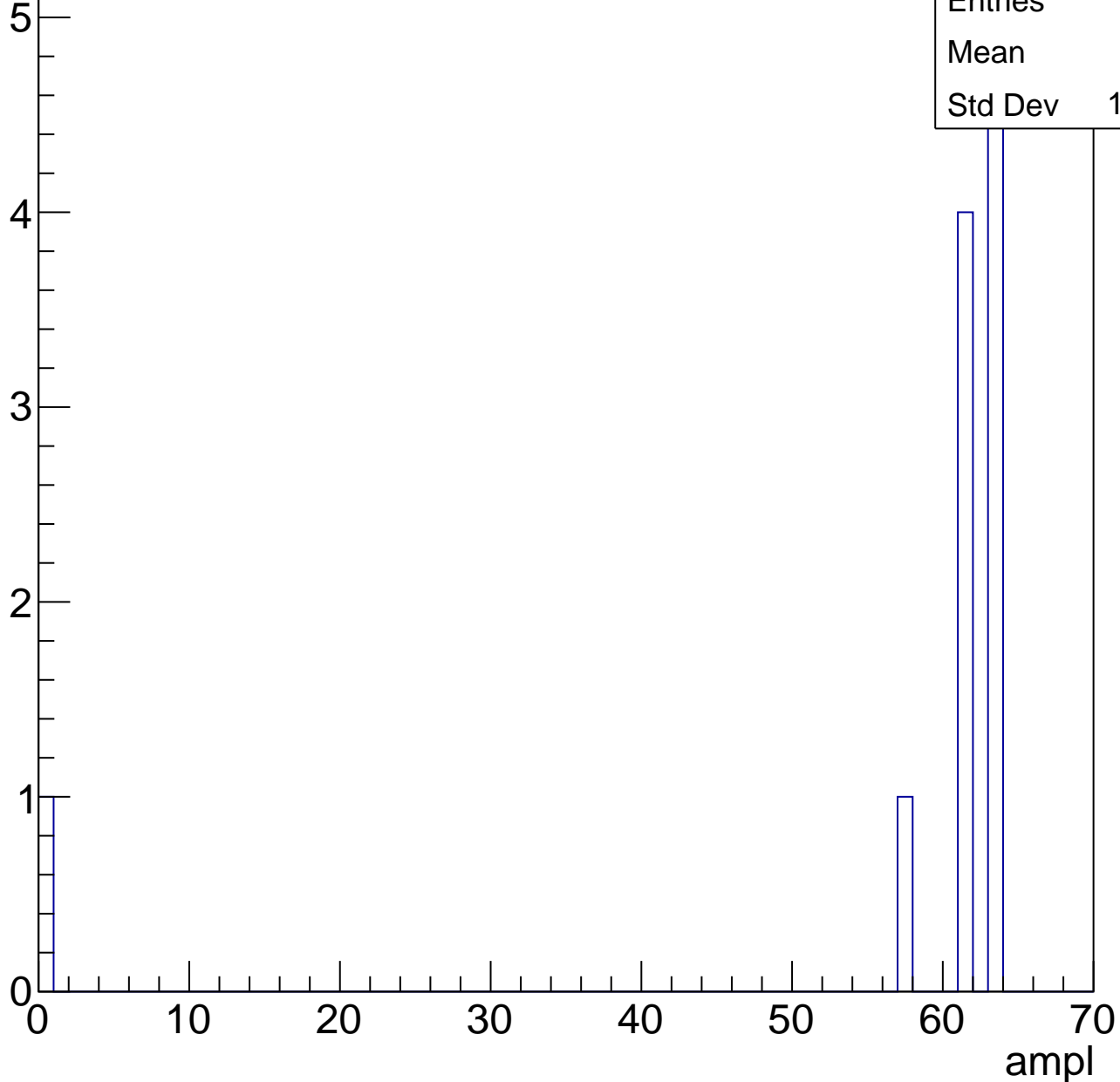


# B1L101S, U18-ch114, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	11
Mean	56
Std Dev	17.79





# B1L101S, U18-ch114, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U18-ch115, adc0

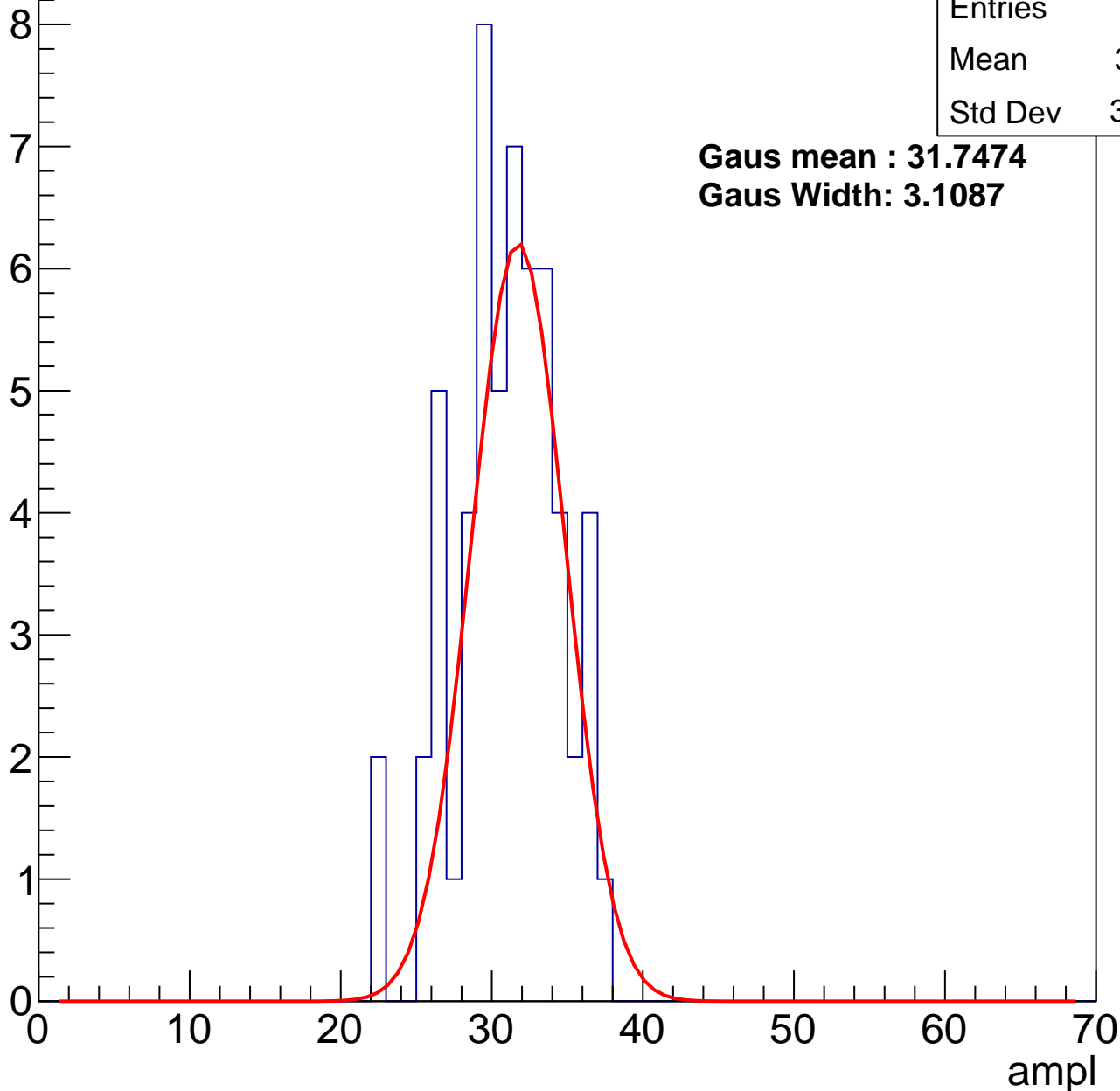
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	30.51
Std Dev	3.424

**Gaus mean : 31.7474**

**Gaus Width: 3.1087**



# B1L101S, U18-ch115, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	90
Mean	38.31
Std Dev	4.236

**Gaus mean : 37.8229**

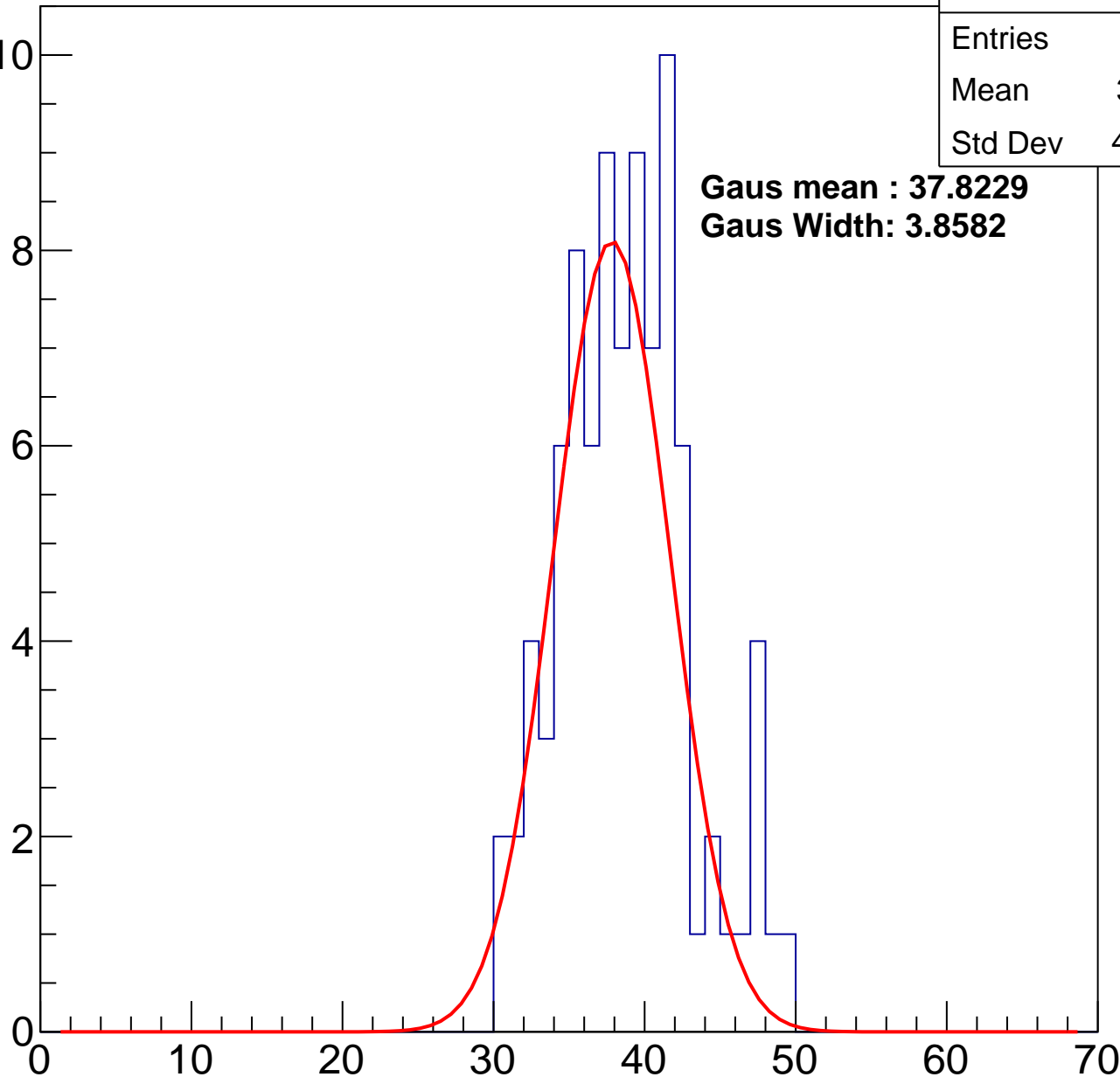
**Gaus Width: 3.8582**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L101S, U18-ch115, adc2

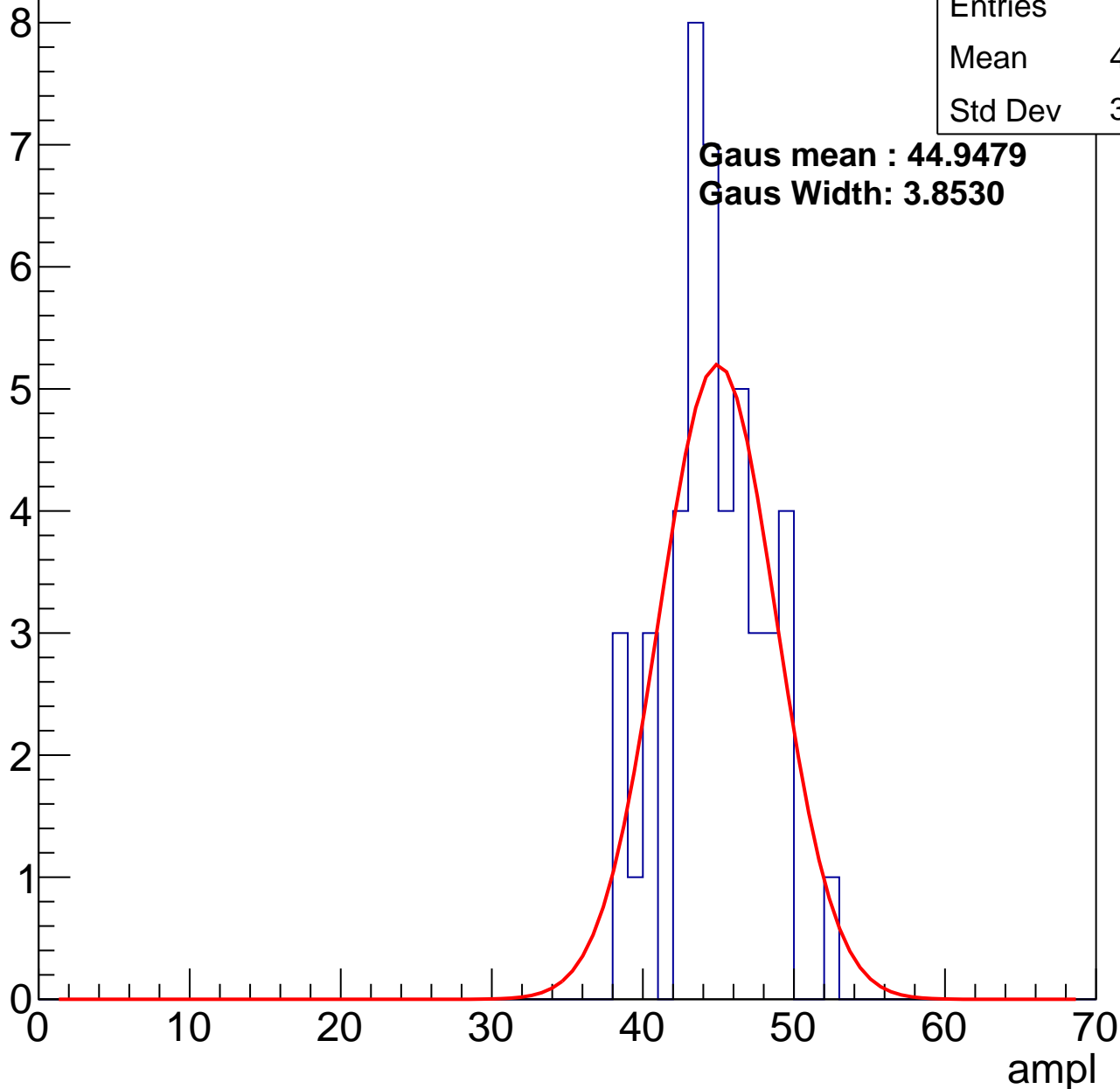
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	46
Mean	44.26
Std Dev	3.179

**Gaus mean : 44.9479**

**Gaus Width: 3.8530**

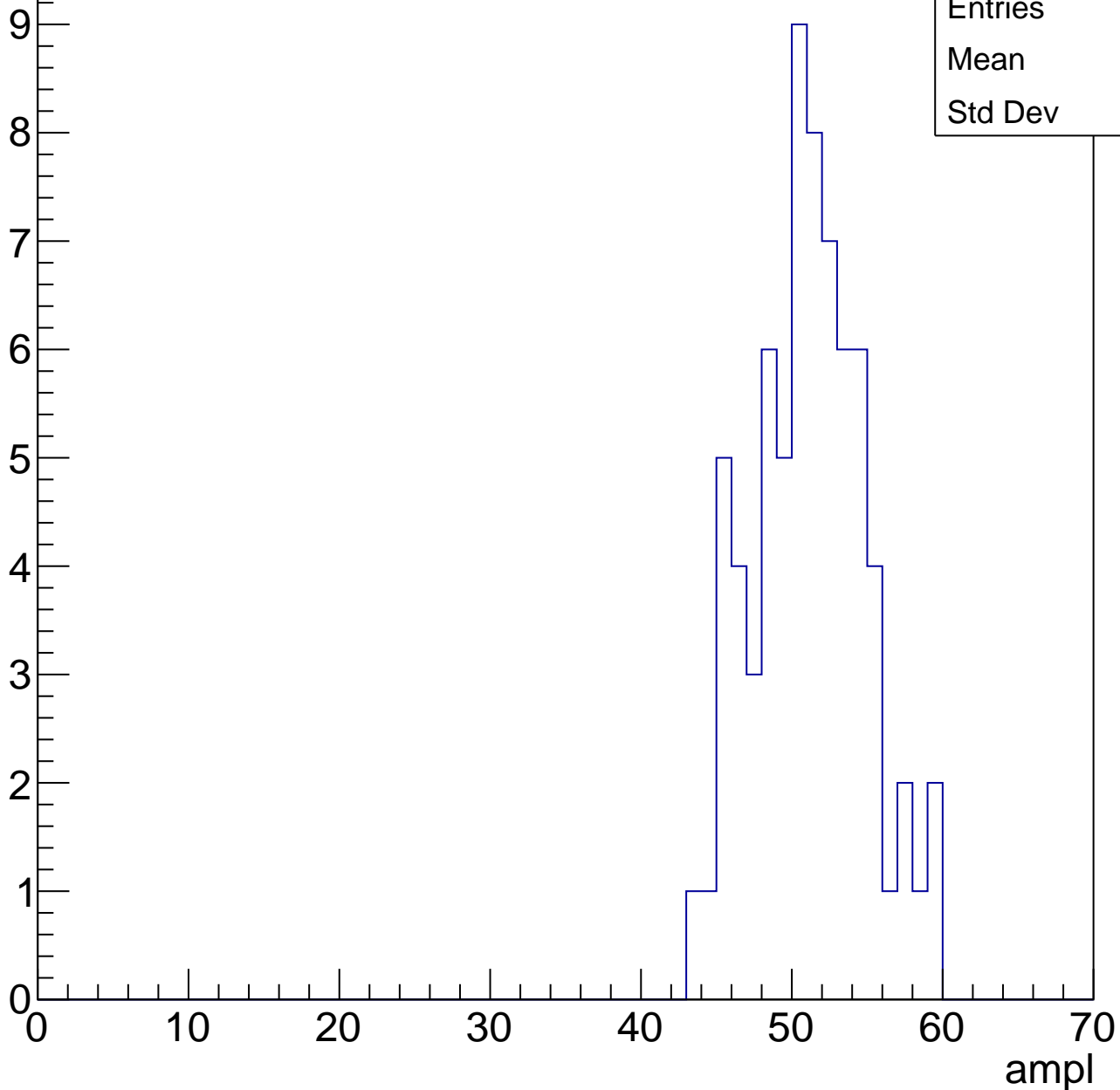


# B1L101S, U18-ch115, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	50.7
Std Dev	3.64

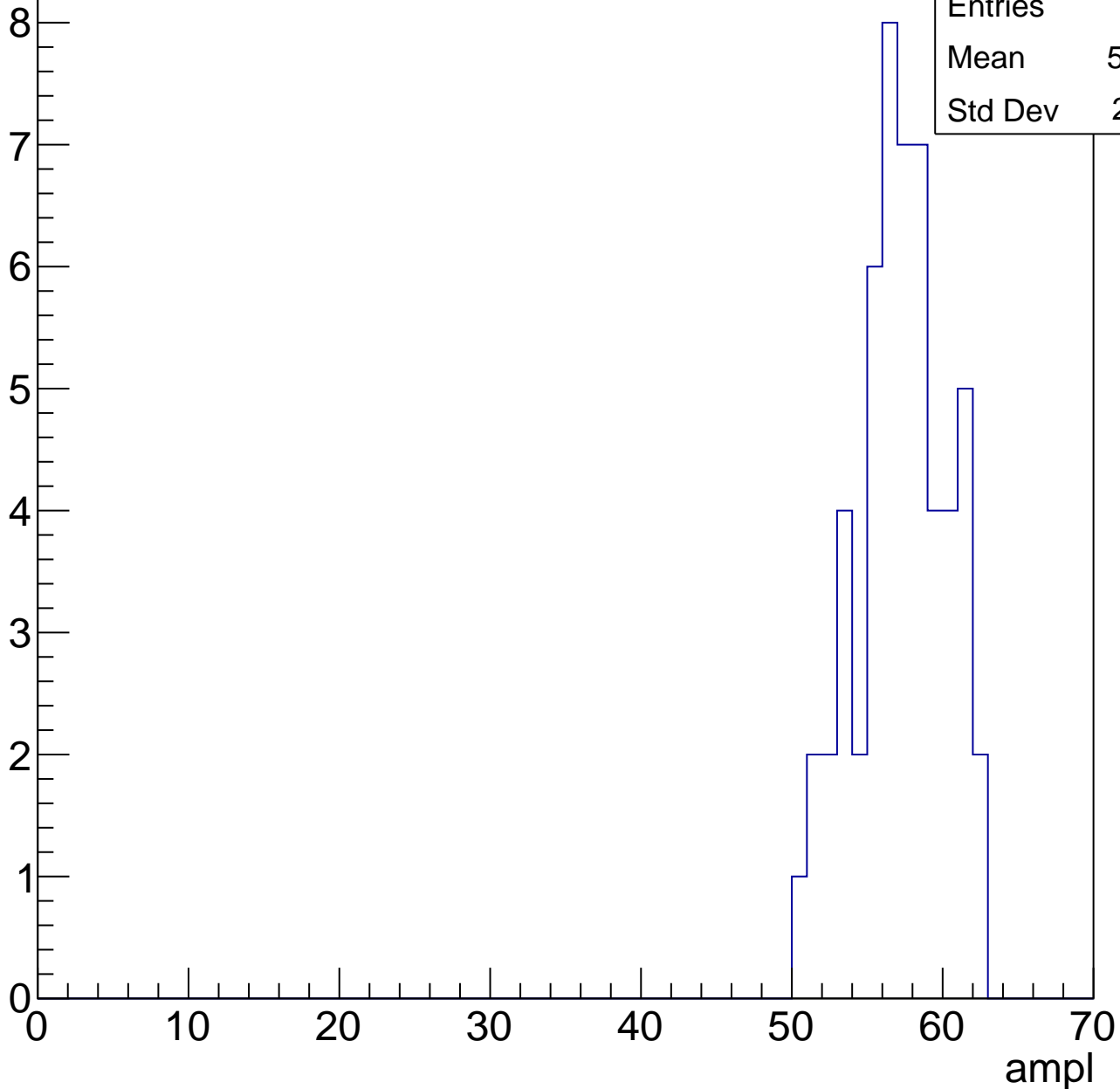


# B1L101S, U18-ch115, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	56.74
Std Dev	2.951

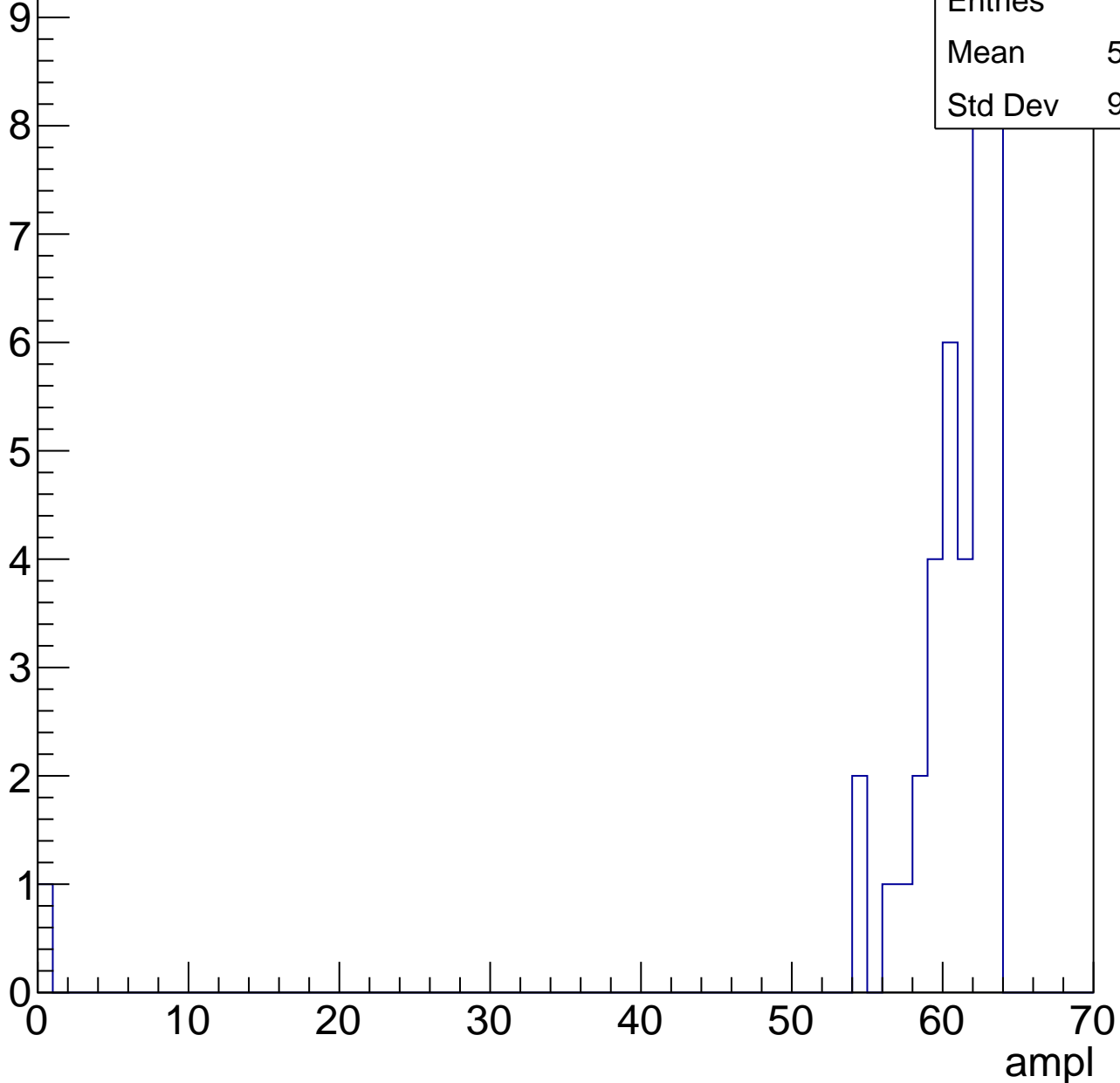


# B1L101S, U18-ch115, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

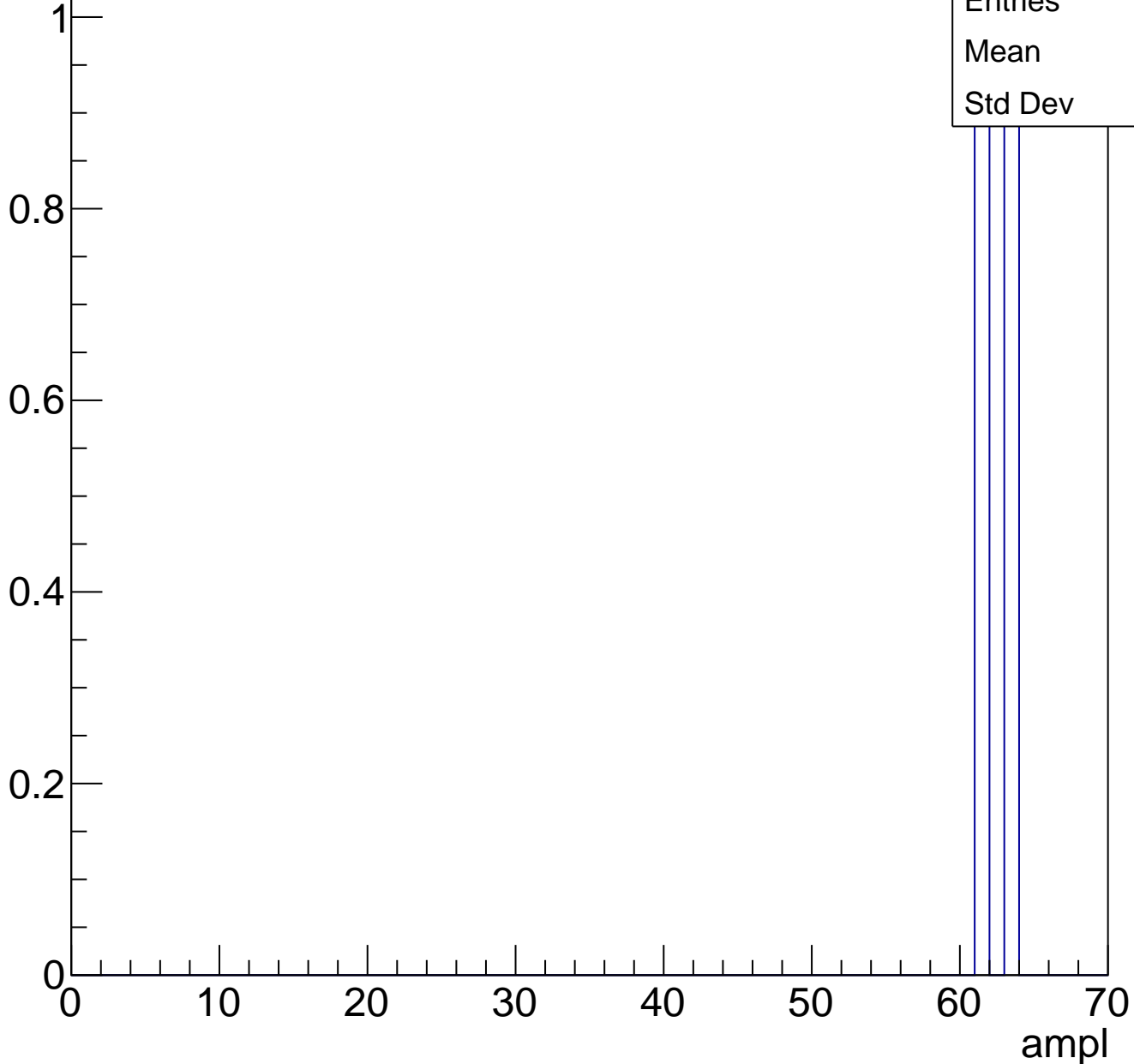
Entries	38
Mean	58.95
Std Dev	9.979



# B1L101S, U18-ch115, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch115, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U18-ch116, adc0

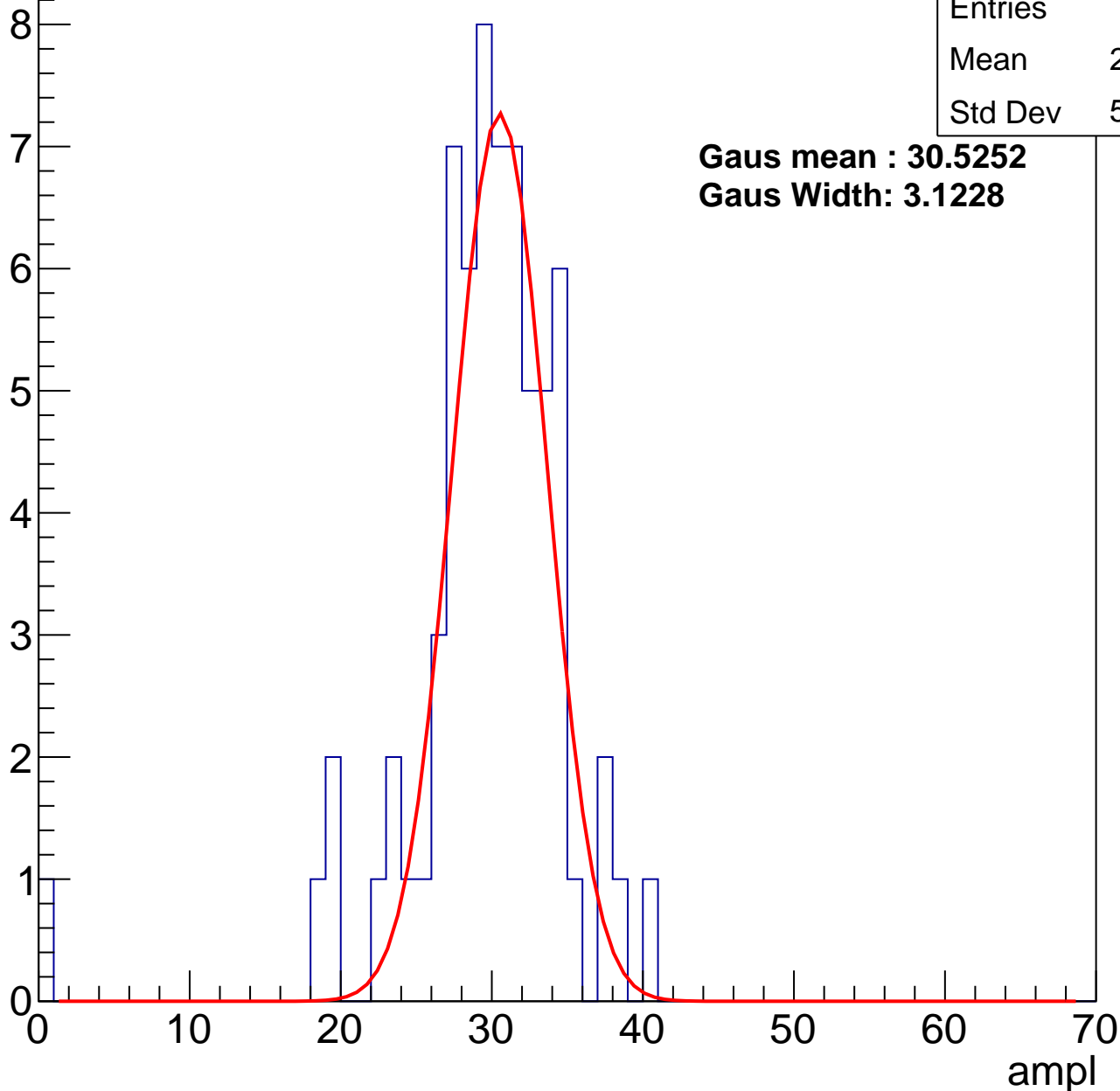
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	29.16
Std Dev	5.503

**Gaus mean : 30.5252**

**Gaus Width: 3.1228**



# B1L101S, U18-ch116, adc1

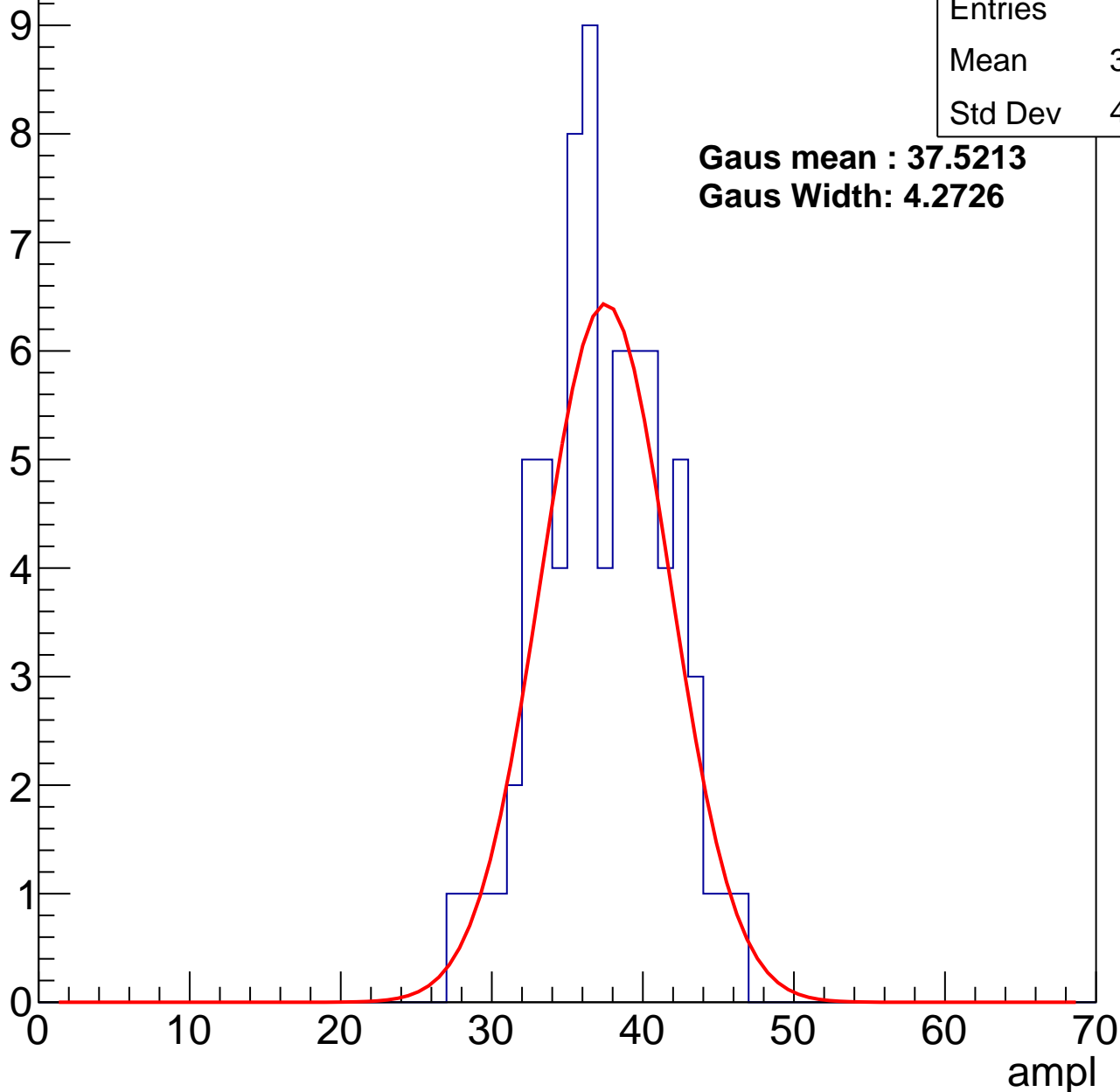
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	36.88
Std Dev	4.064

**Gaus mean : 37.5213**

**Gaus Width: 4.2726**



# B1L101S, U18-ch116, adc2

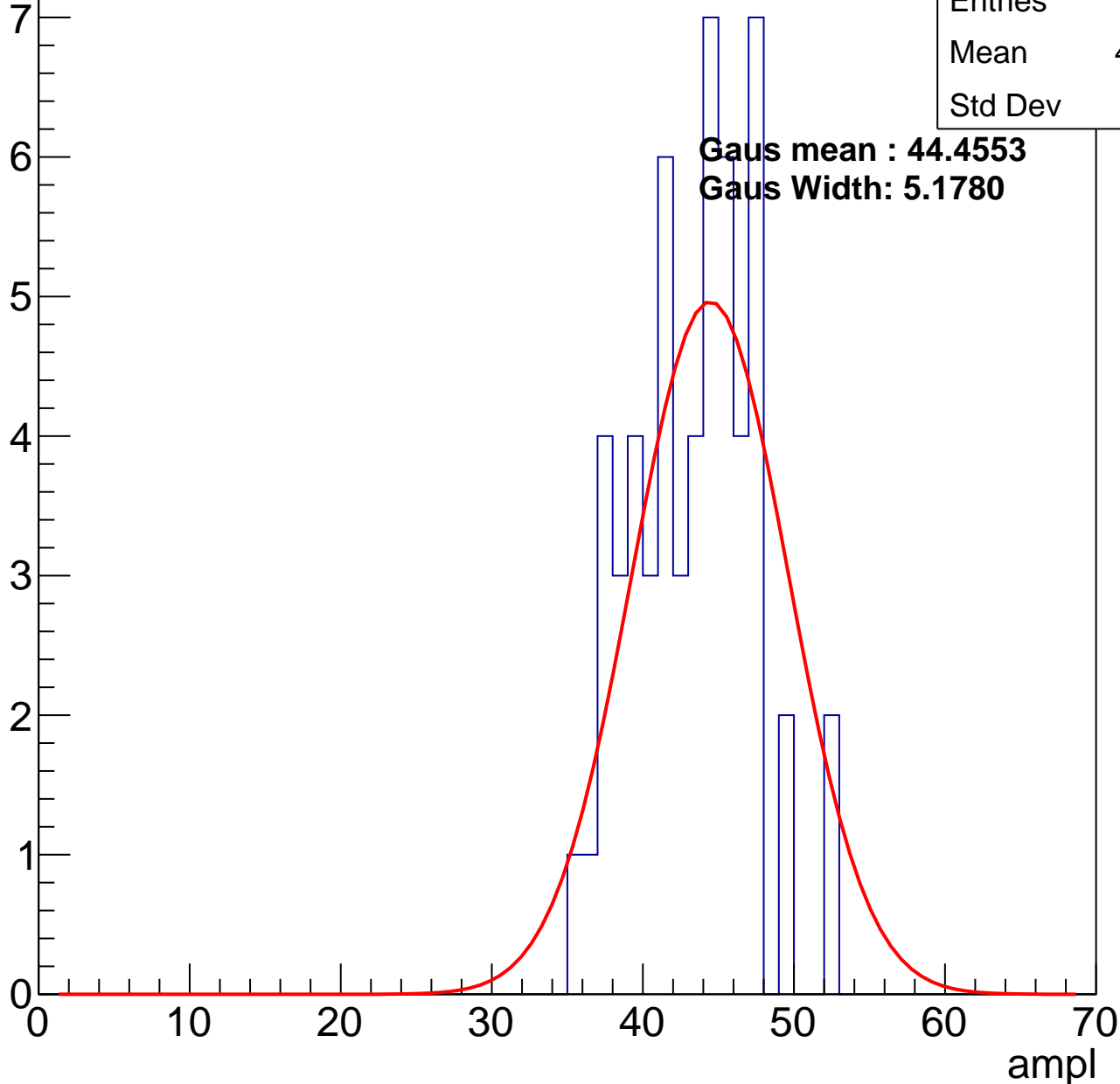
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	42.91
Std Dev	3.89

**Gaus mean : 44.4553**

**Gaus Width: 5.1780**

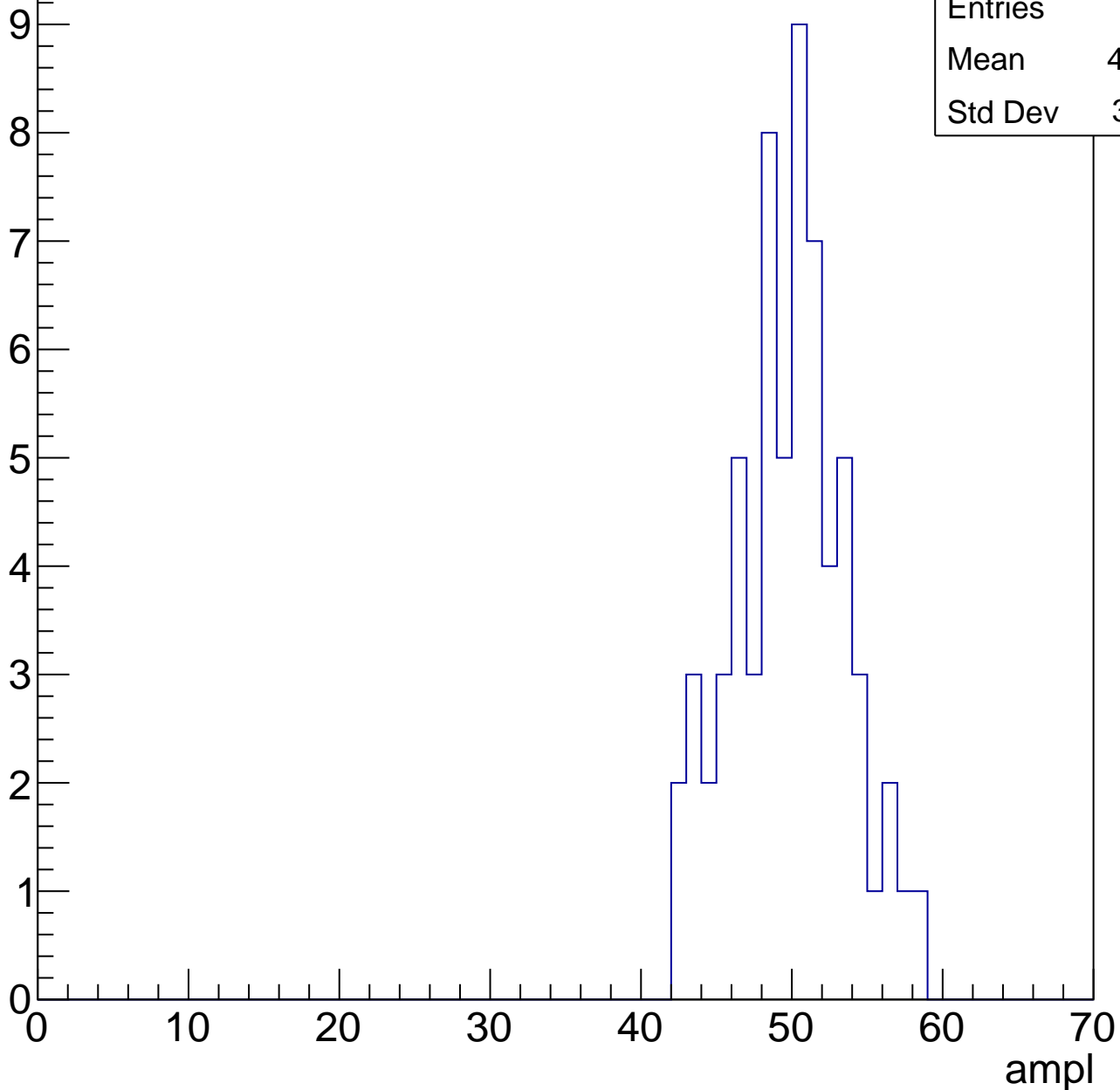


# B1L101S, U18-ch116, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	49.38
Std Dev	3.681

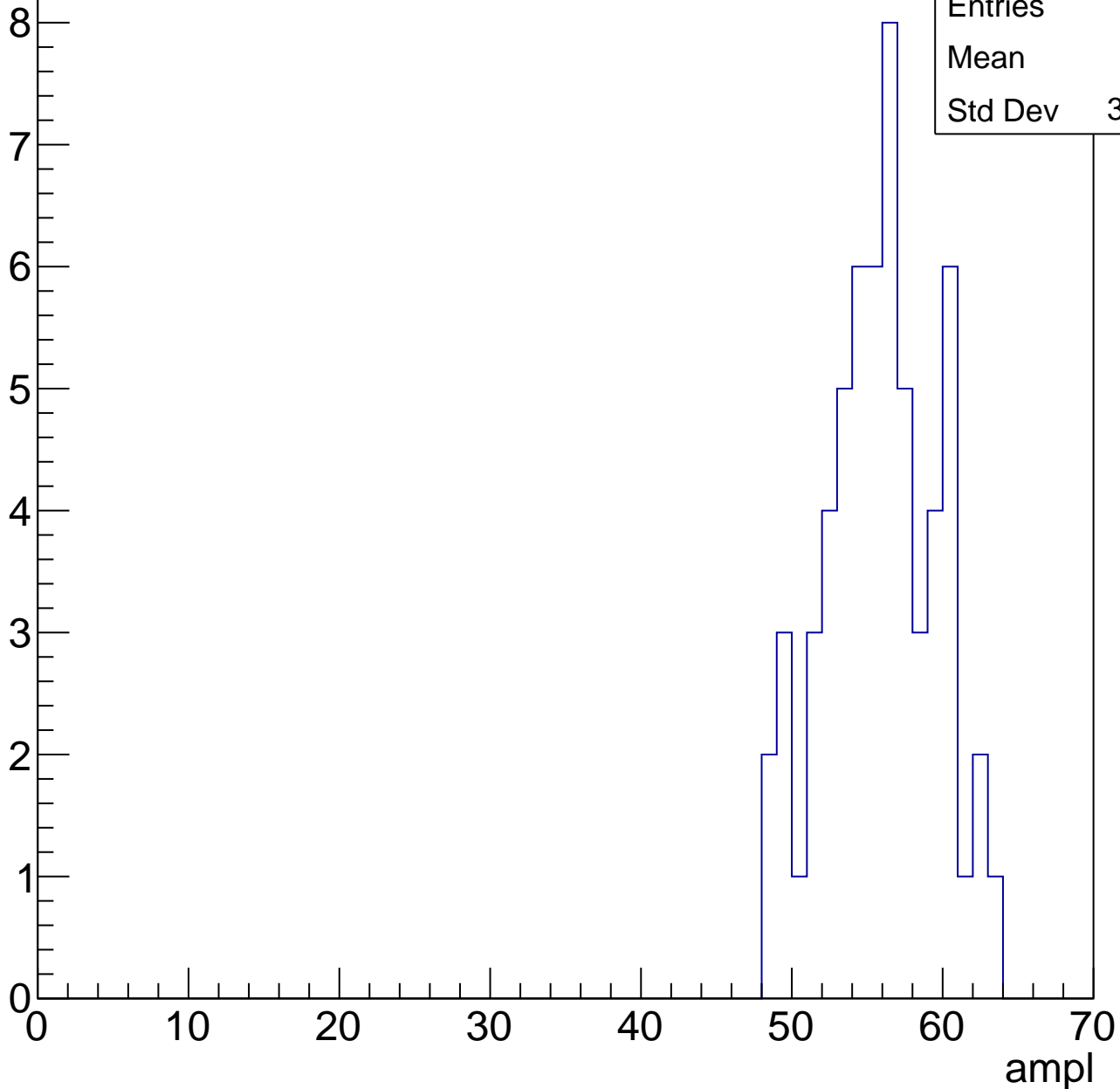


# B1L101S, U18-ch116, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	55.4
Std Dev	3.648

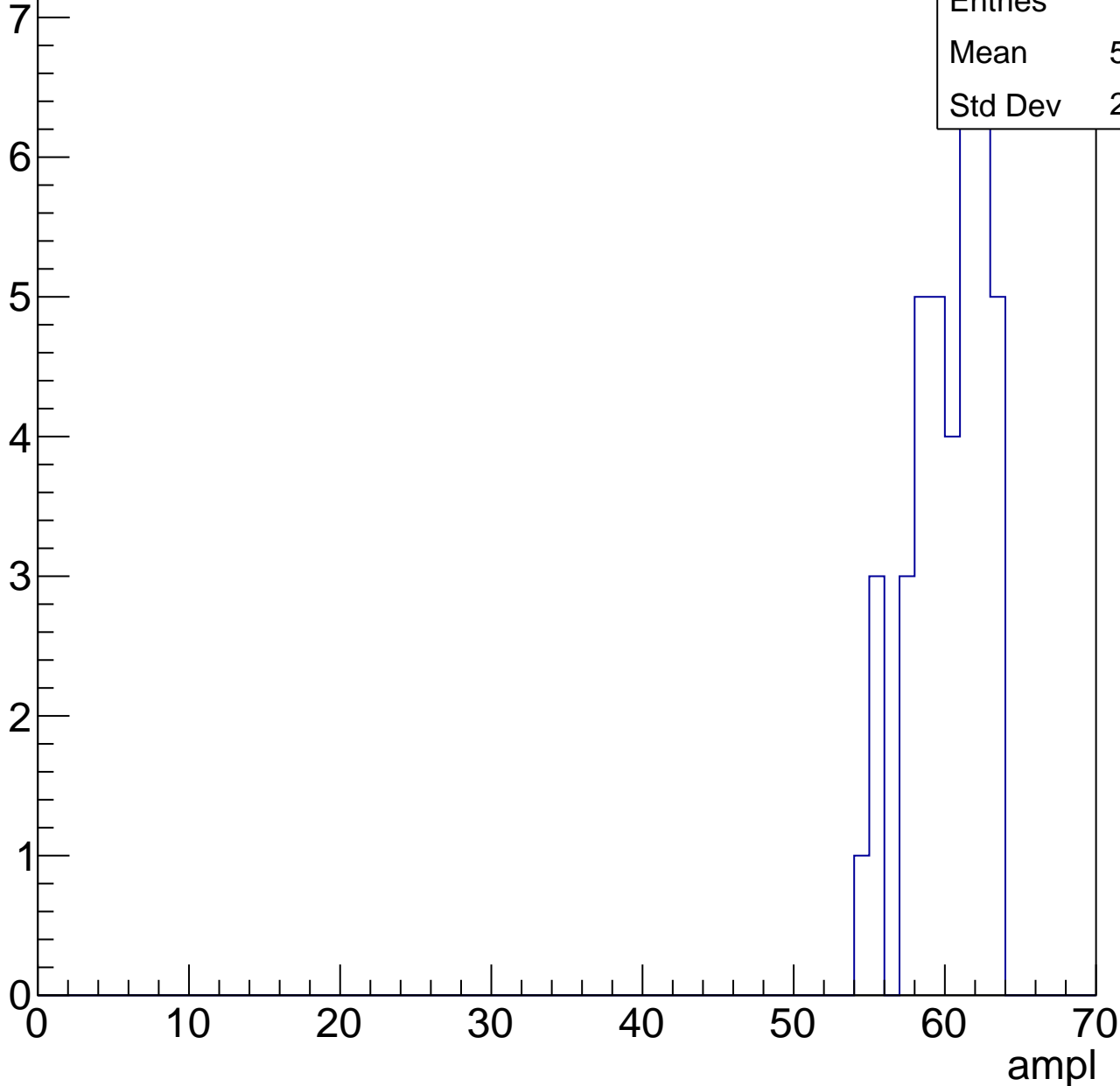


# B1L101S, U18-ch116, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

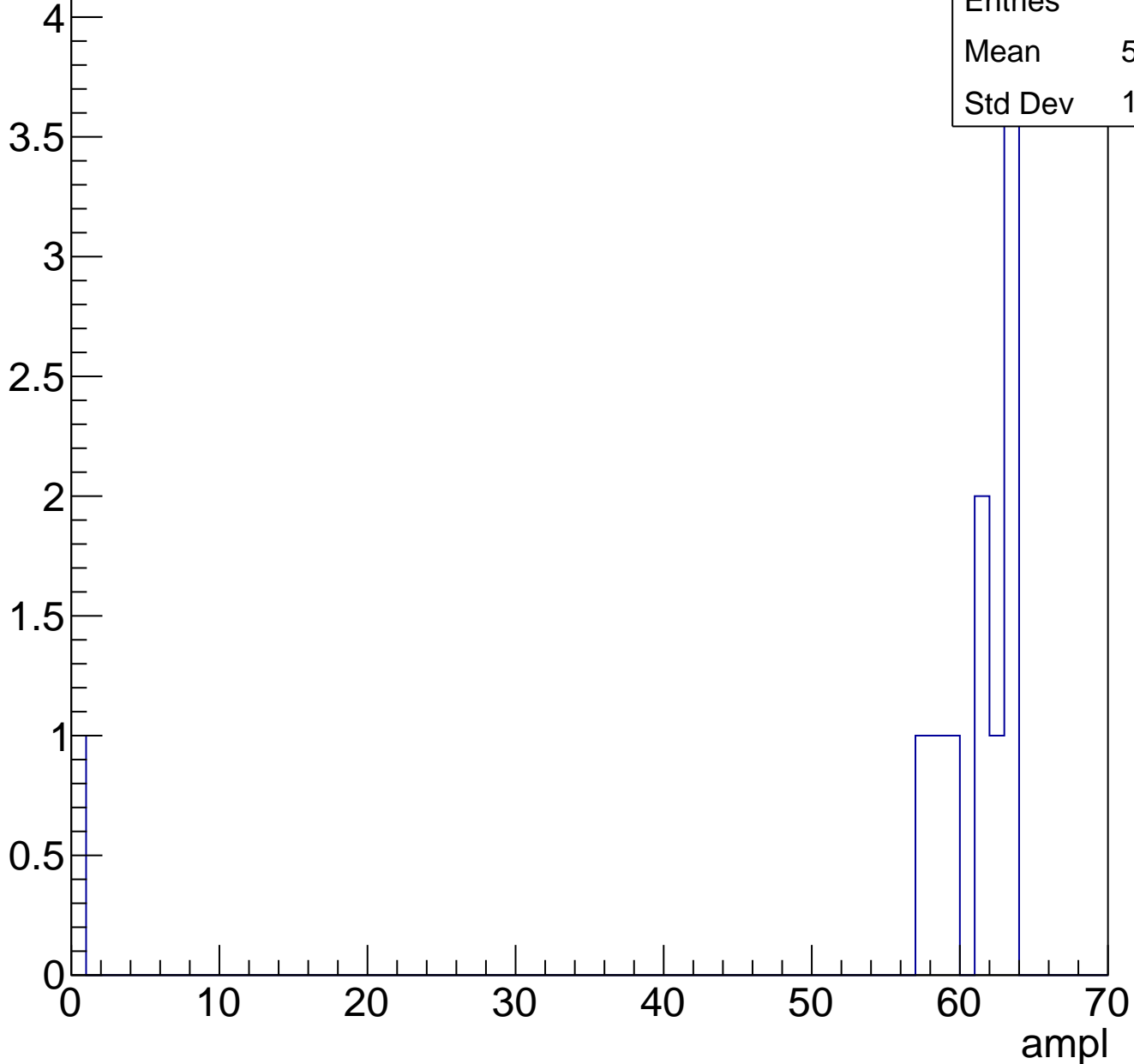
Entries	40
Mean	59.77
Std Dev	2.454



# B1L101S, U18-ch116, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch116, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U18-ch117, adc0

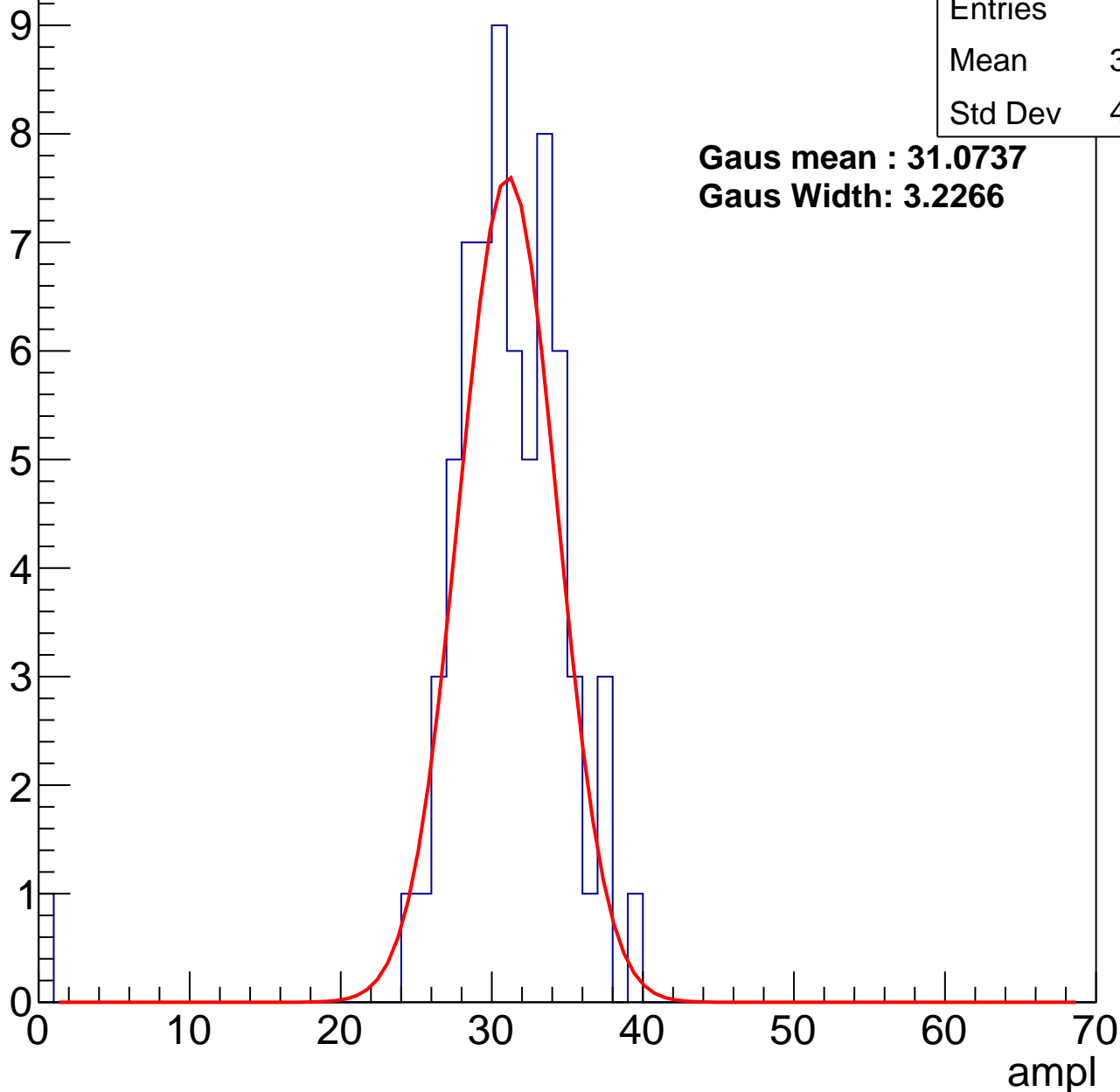
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	30.39
Std Dev	4.905

**Gaus mean : 31.0737**

**Gaus Width: 3.2266**



# B1L101S, U18-ch117, adc1

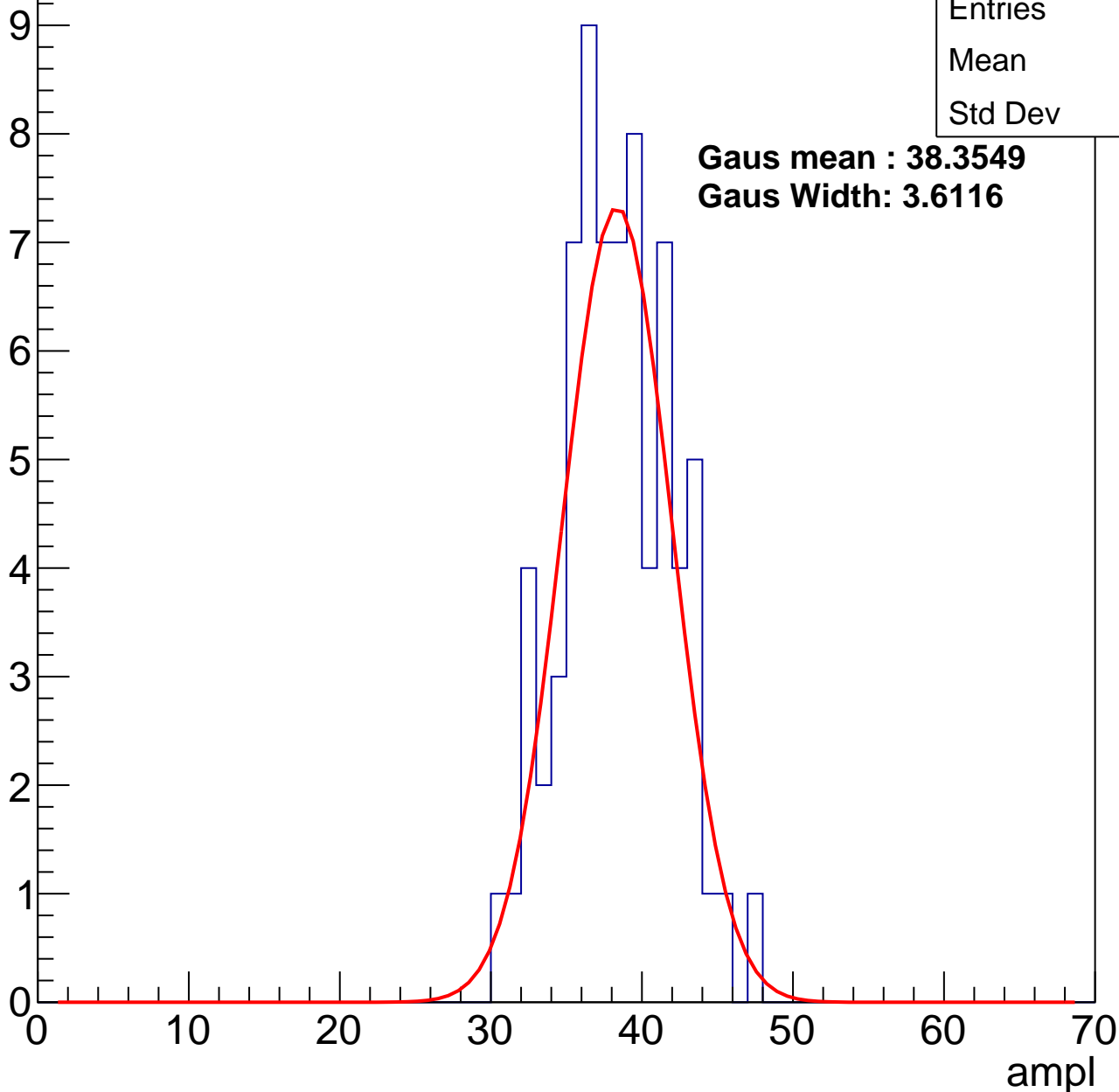
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	37.9
Std Dev	3.54

**Gaus mean : 38.3549**

**Gaus Width: 3.6116**



# B1L101S, U18-ch117, adc2

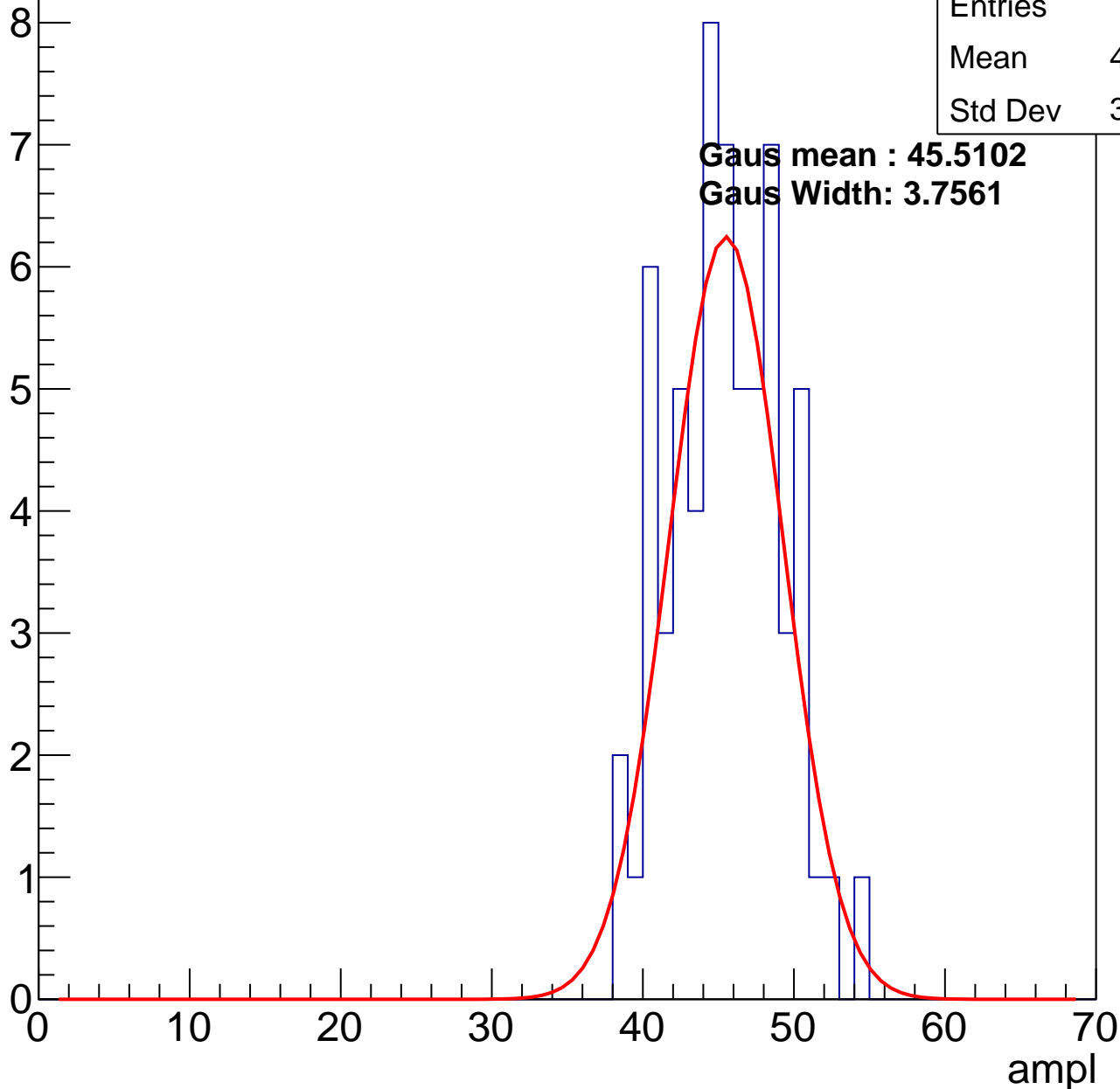
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	45.03
Std Dev	3.597

Gaus mean : 45.5102

Gaus Width: 3.7561

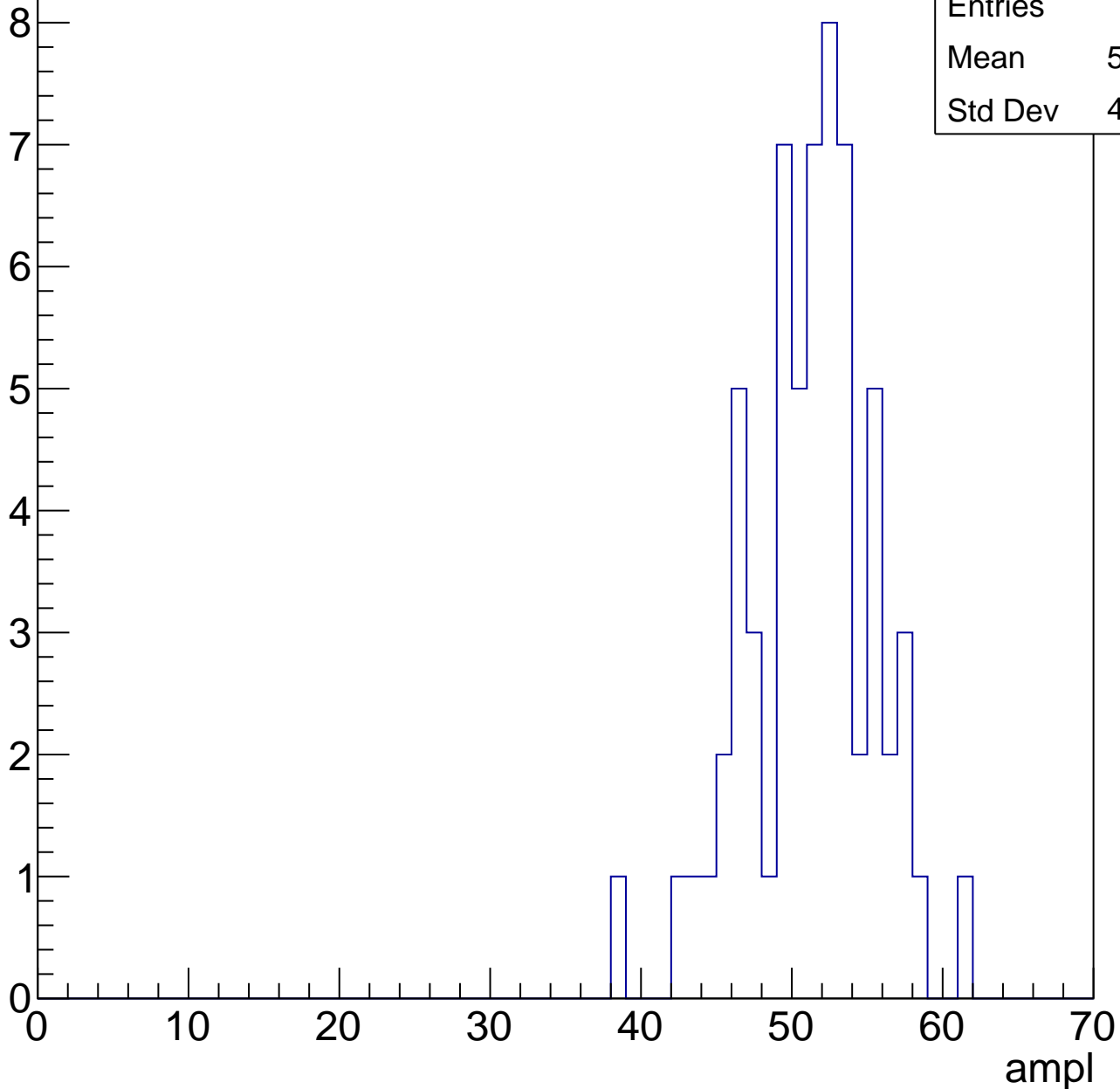


# B1L101S, U18-ch117, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	50.76
Std Dev	4.155

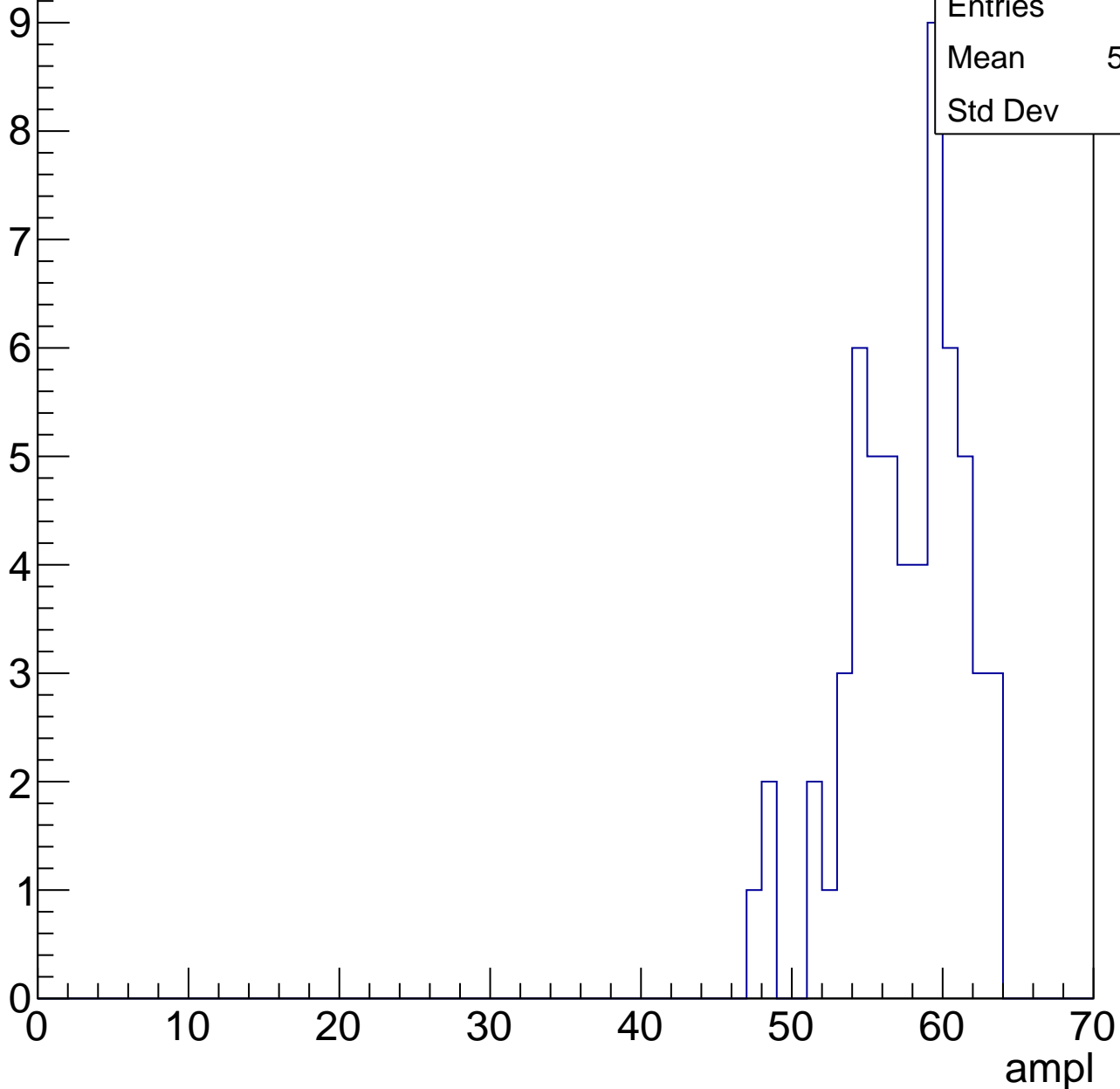


# B1L101S, U18-ch117, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	57.05
Std Dev	3.78

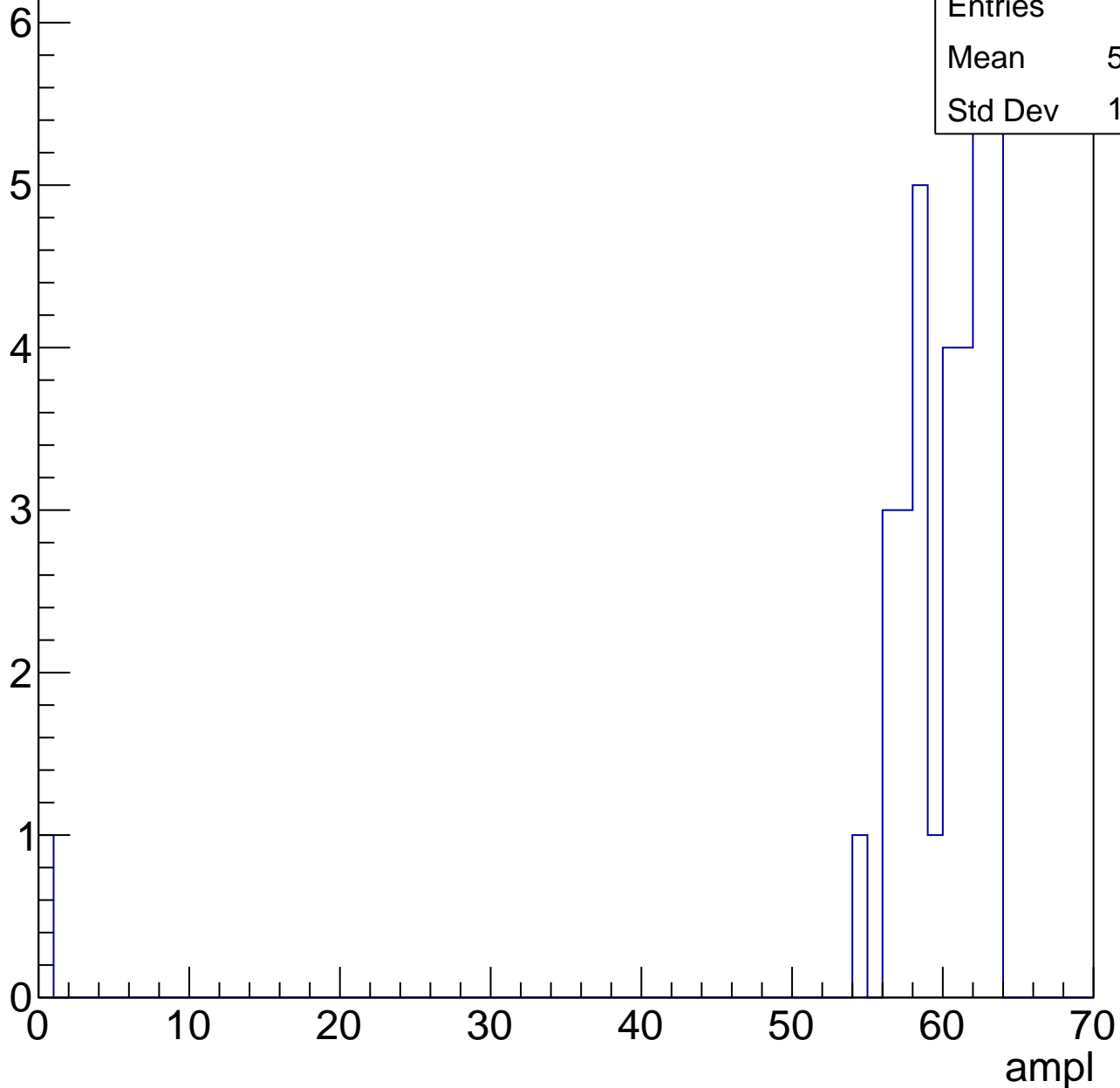


# B1L101S, U18-ch117, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	34
Mean	58.12
Std Dev	10.42



# B1L101S, U18-ch117, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch117, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch118, adc0

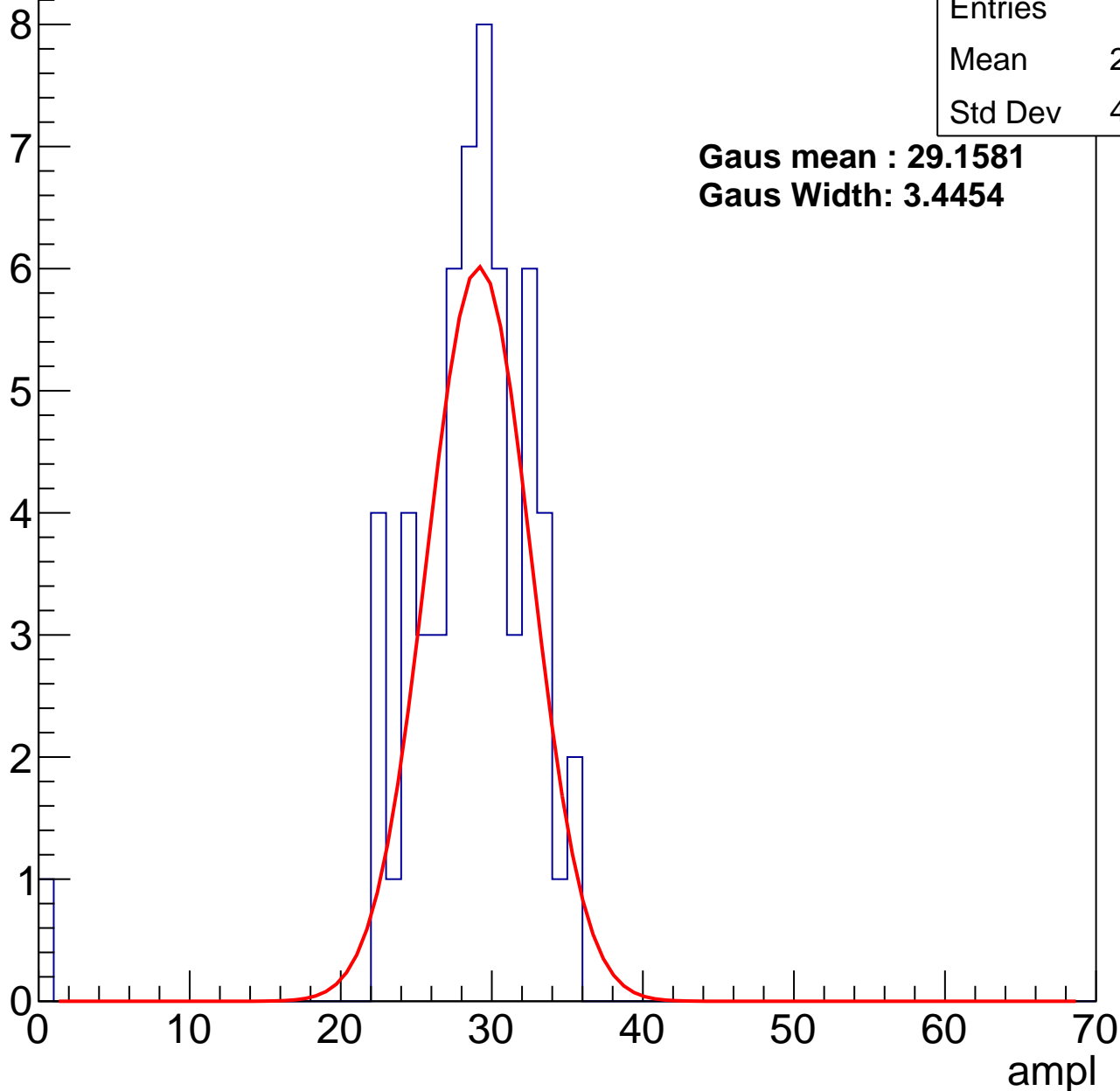
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	27.98
Std Dev	4.959

**Gaus mean : 29.1581**

**Gaus Width: 3.4454**



# B1L101S, U18-ch118, adc1

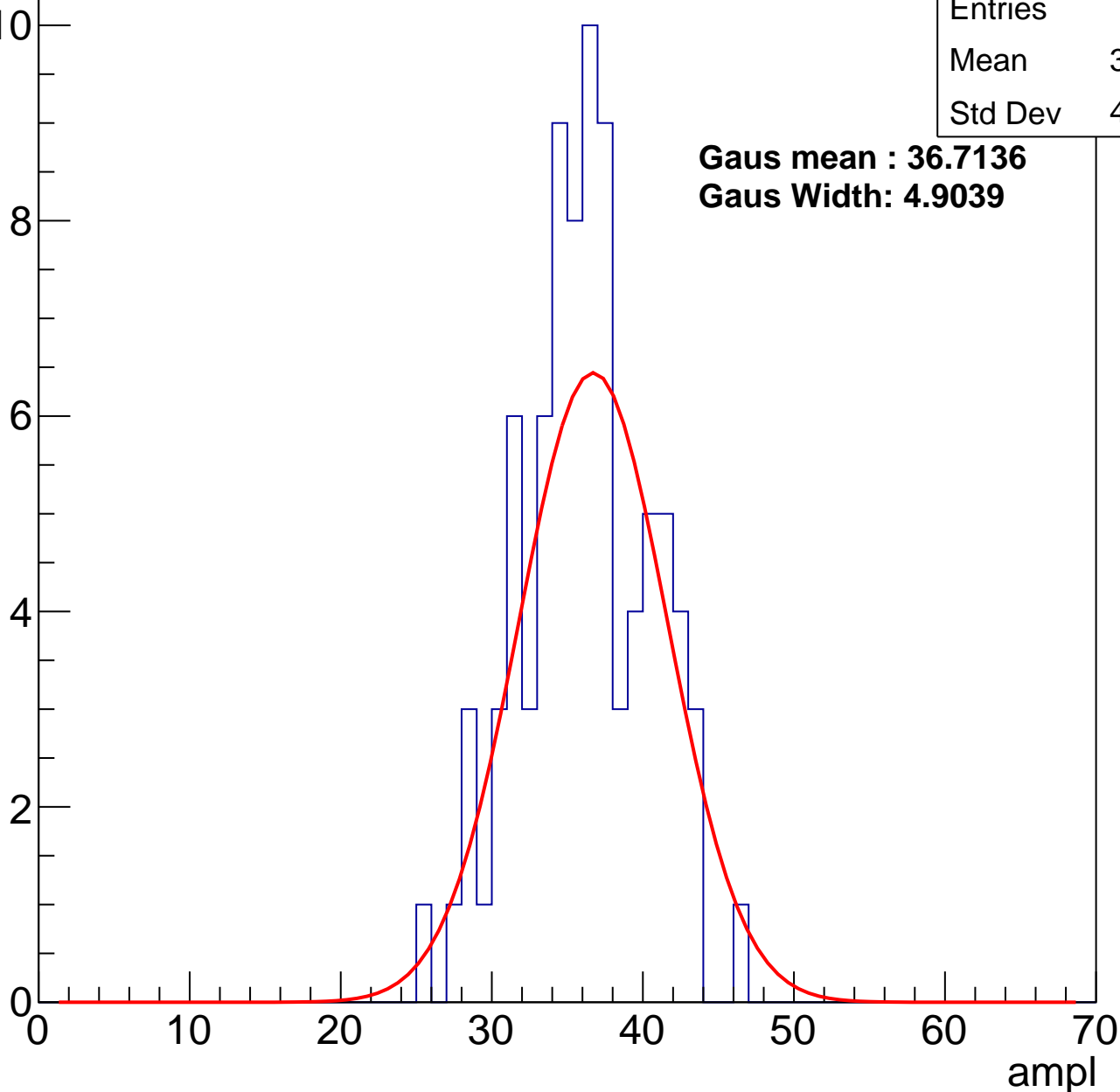
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	85
Mean	35.67
Std Dev	4.188

**Gaus mean : 36.7136**

**Gaus Width: 4.9039**



# B1L101S, U18-ch118, adc2

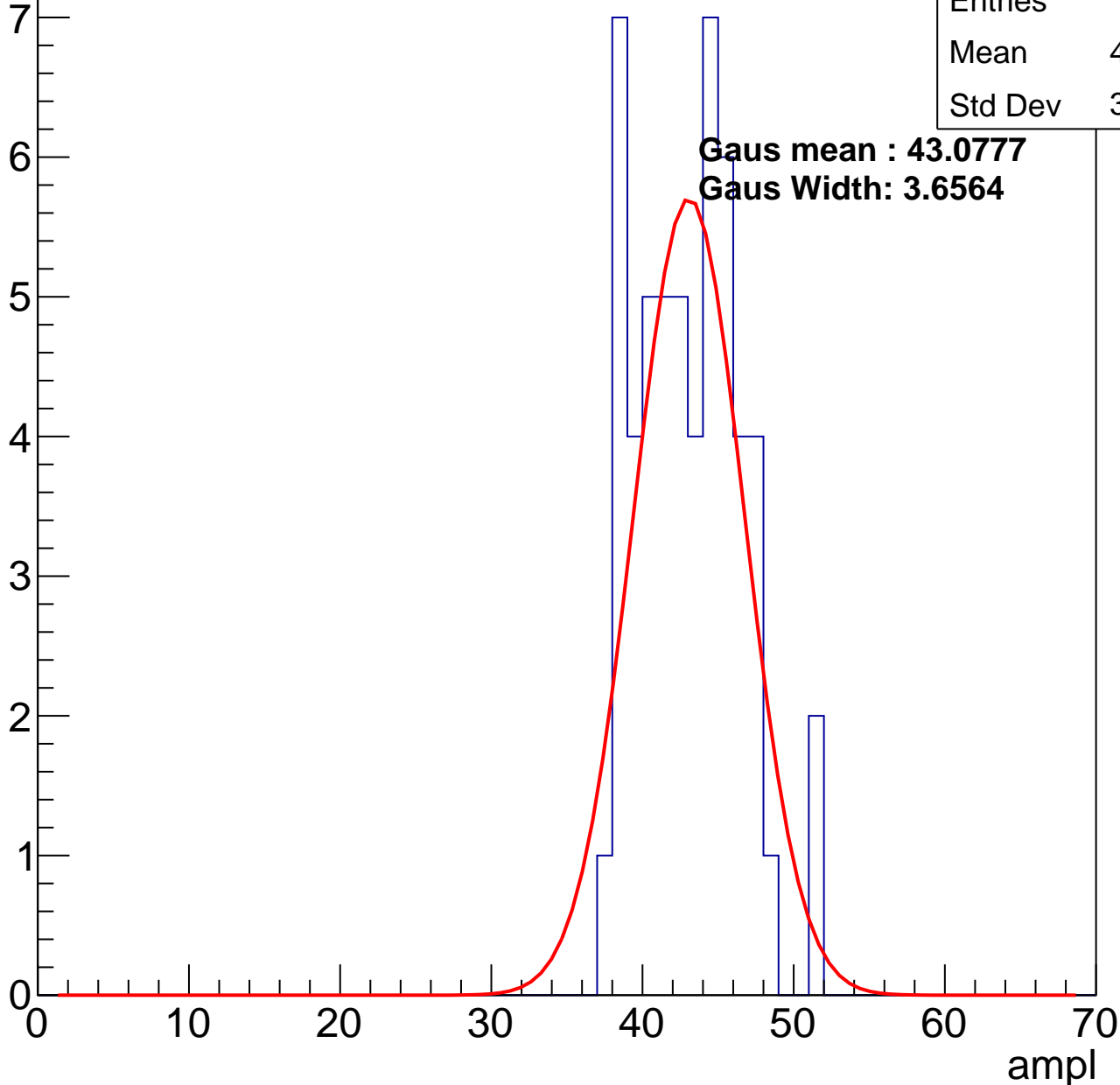
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	42.65
Std Dev	3.364

**Gaus mean : 43.0777**

**Gaus Width: 3.6564**

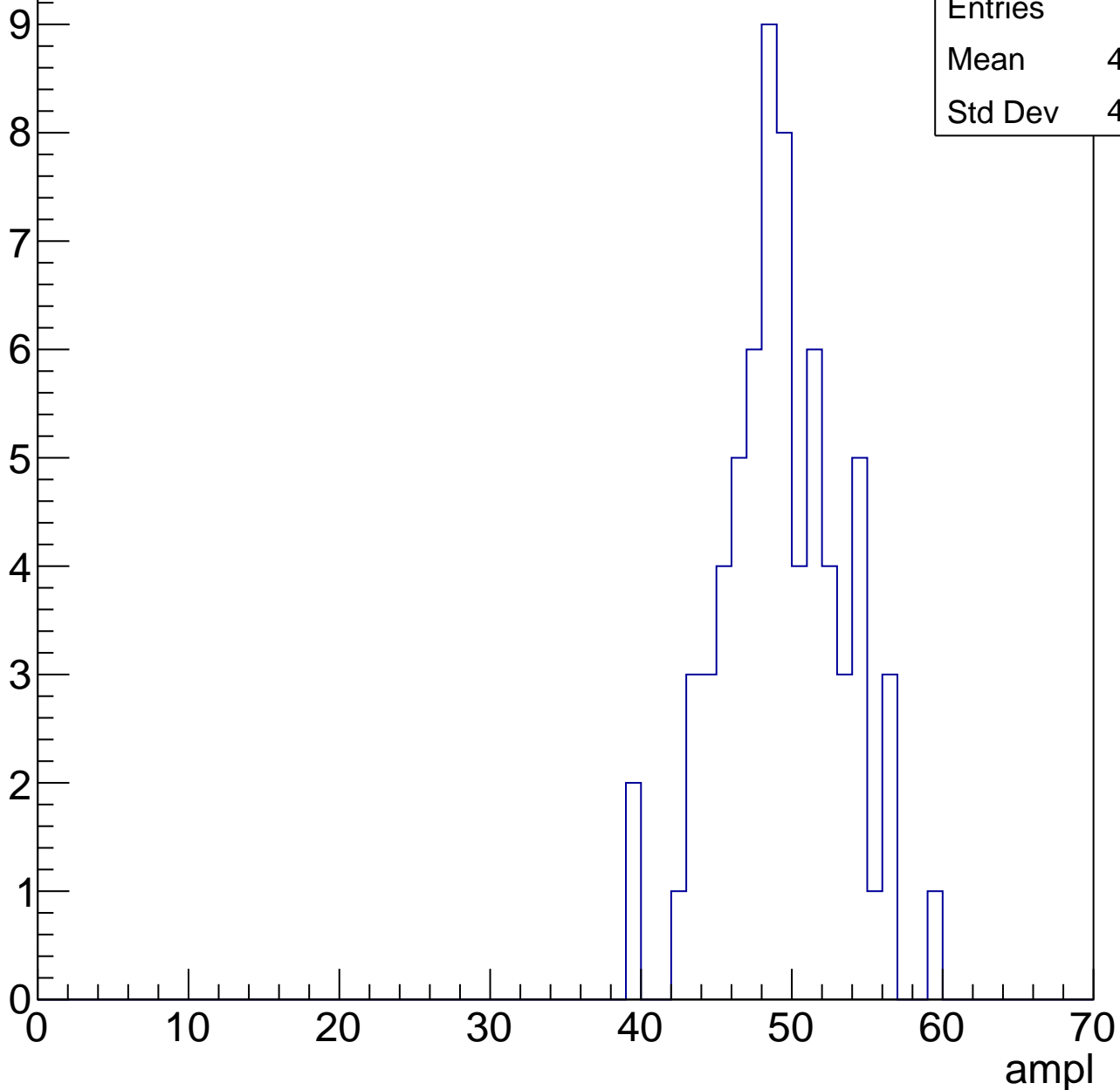


# B1L101S, U18-ch118, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

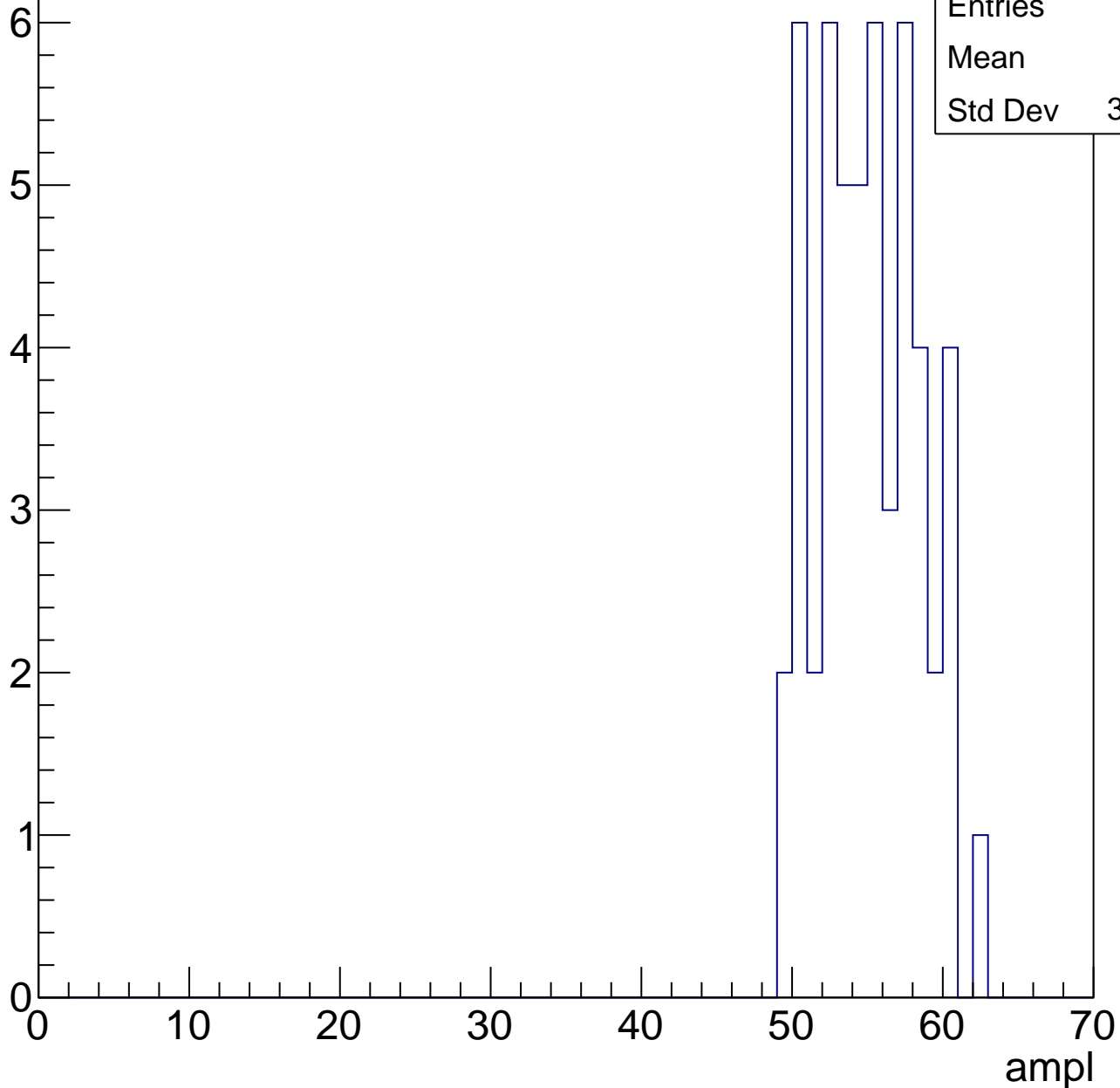
Entries	68
Mean	48.85
Std Dev	4.008



# B1L101S, U18-ch118, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



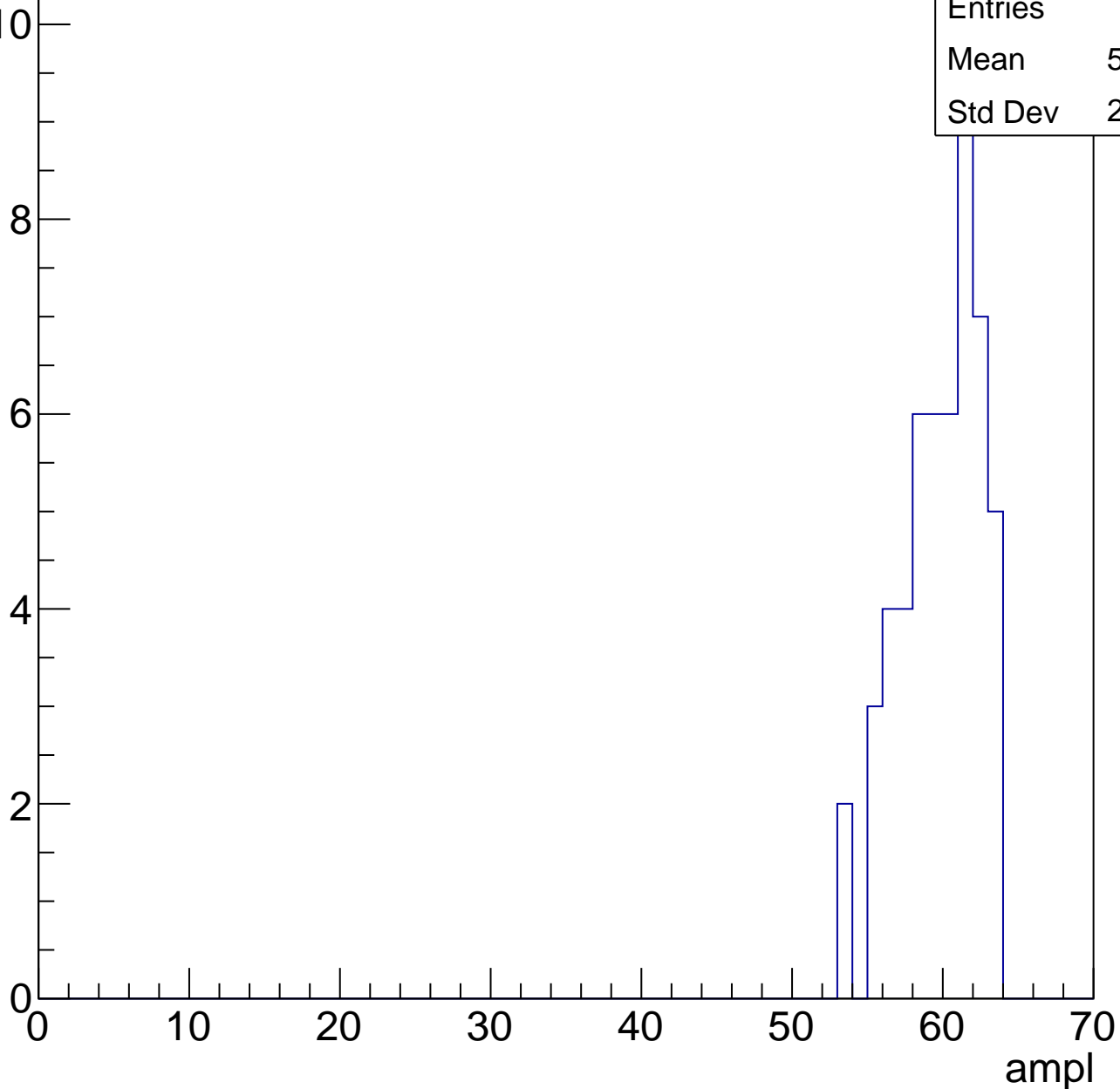
Entries	52
Mean	54.6
Std Dev	3.307

# B1L101S, U18-ch118, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	59.32
Std Dev	2.612

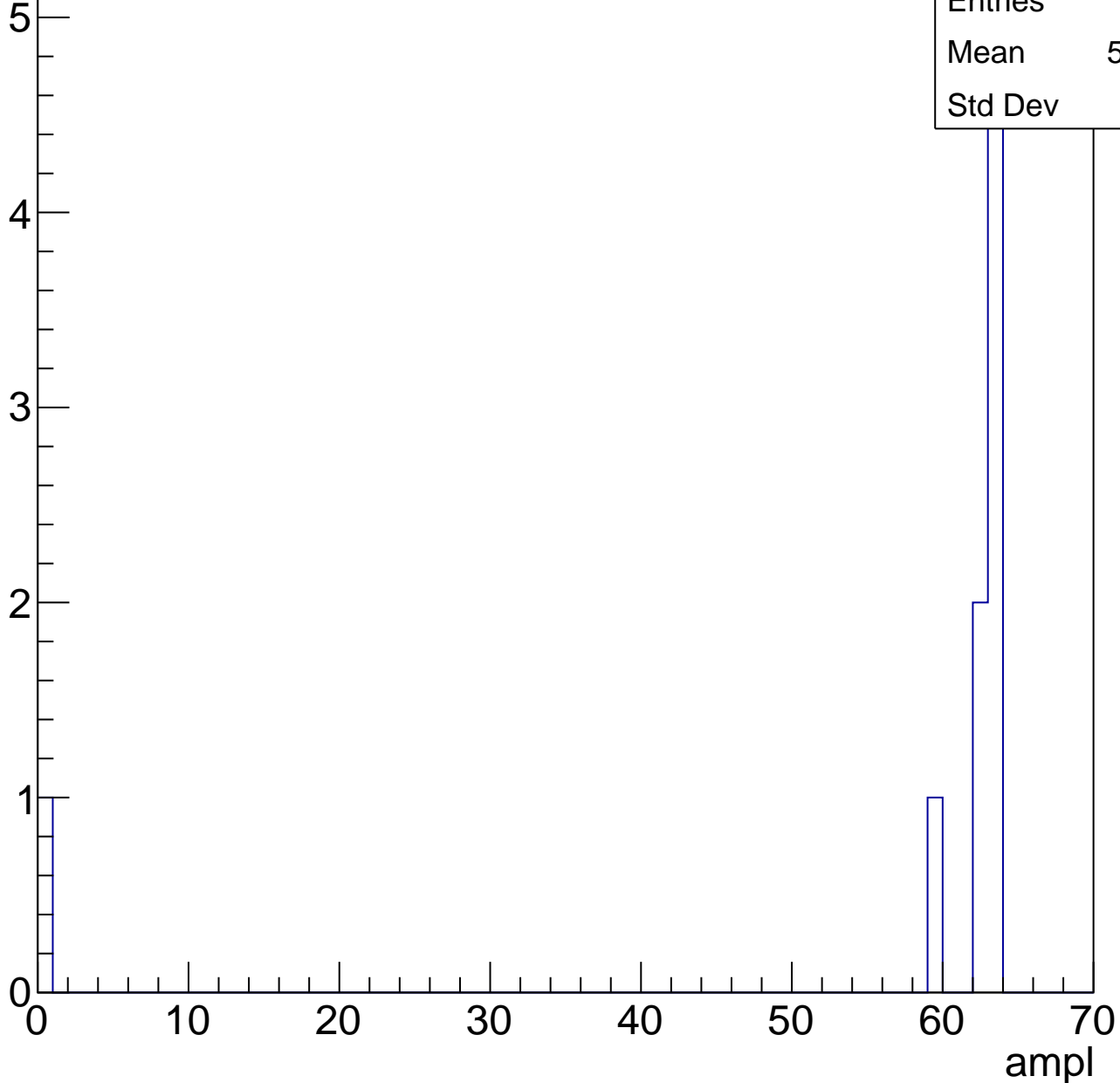


# B1L101S, U18-ch118, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	9
Mean	55.33
Std Dev	19.6





# B1L101S, U18-ch118, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U18-ch119, adc0

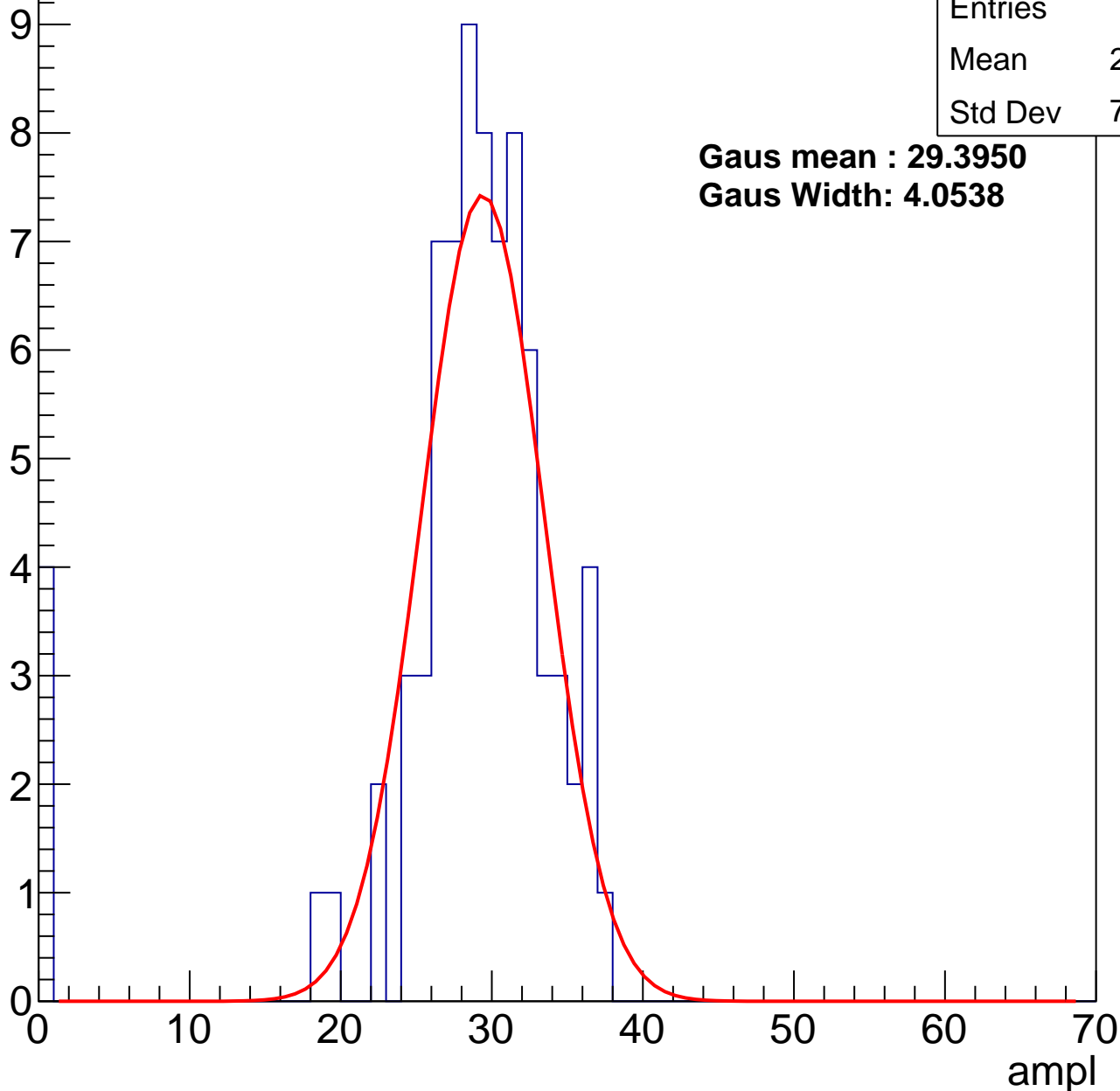
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	79
Mean	27.66
Std Dev	7.388

**Gaus mean : 29.3950**

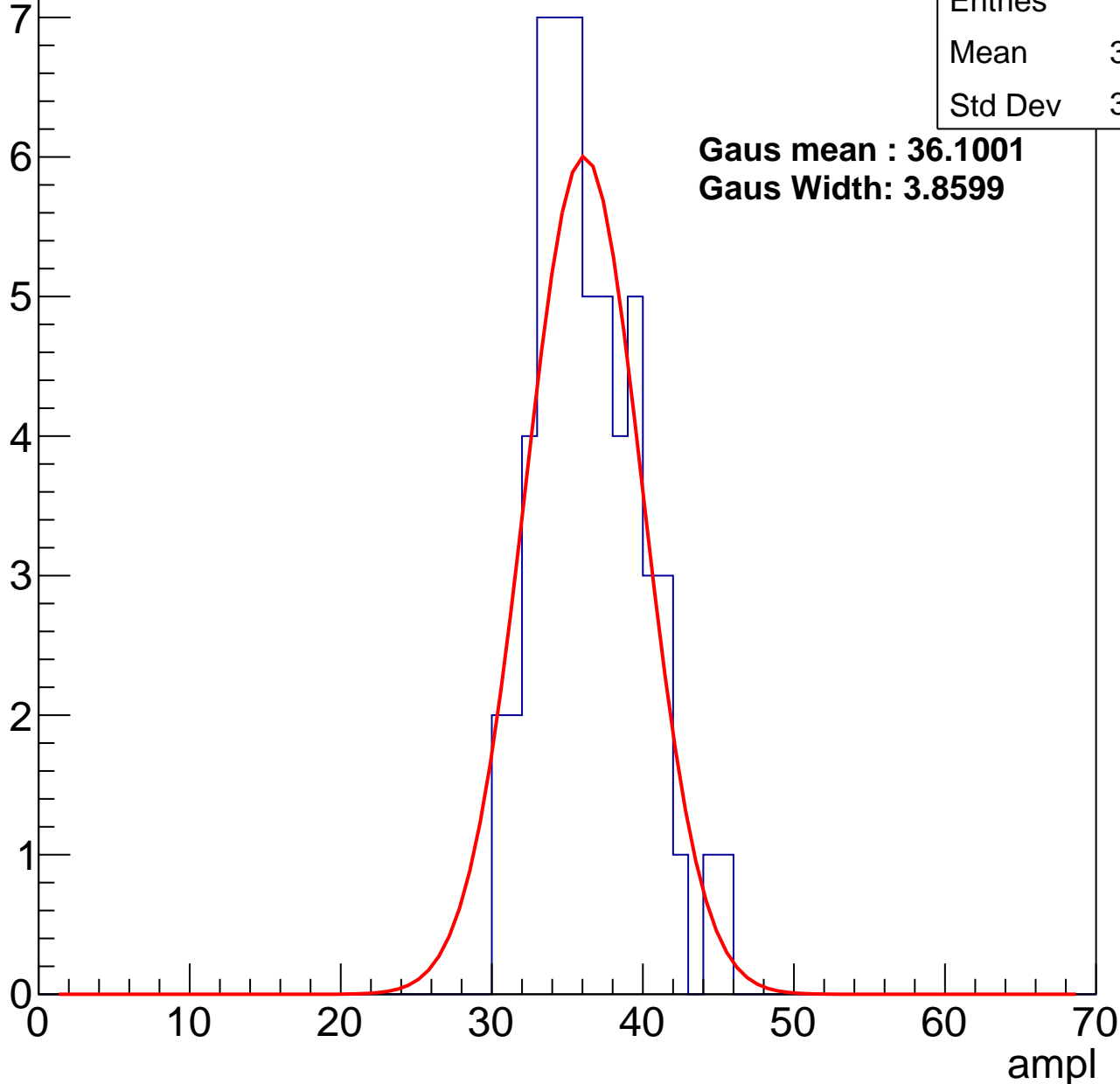
**Gaus Width: 4.0538**



# B1L101S, U18-ch119, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch119, adc2

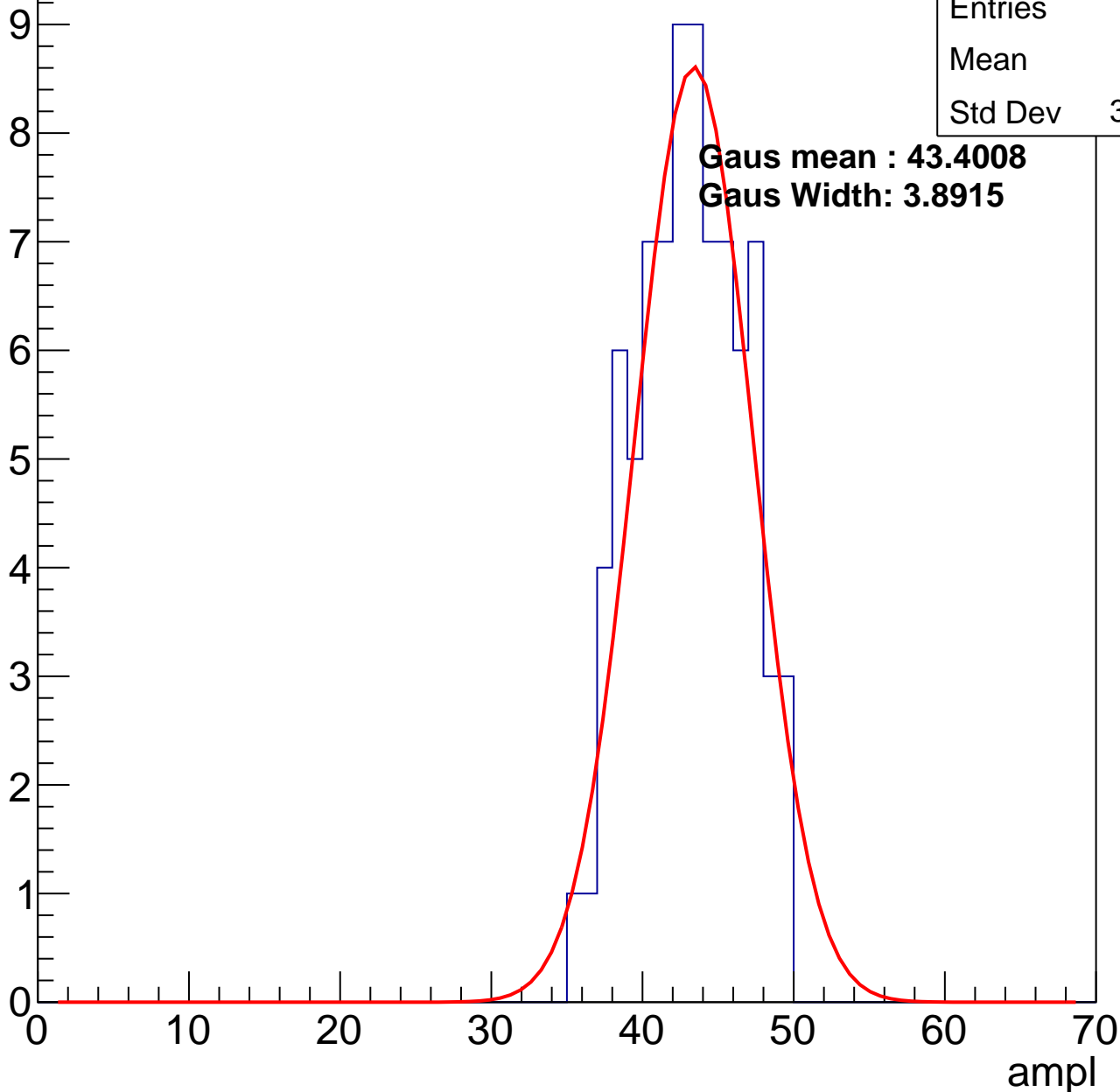
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	82
Mean	42.6
Std Dev	3.418

**Gaus mean : 43.4008**

**Gaus Width: 3.8915**

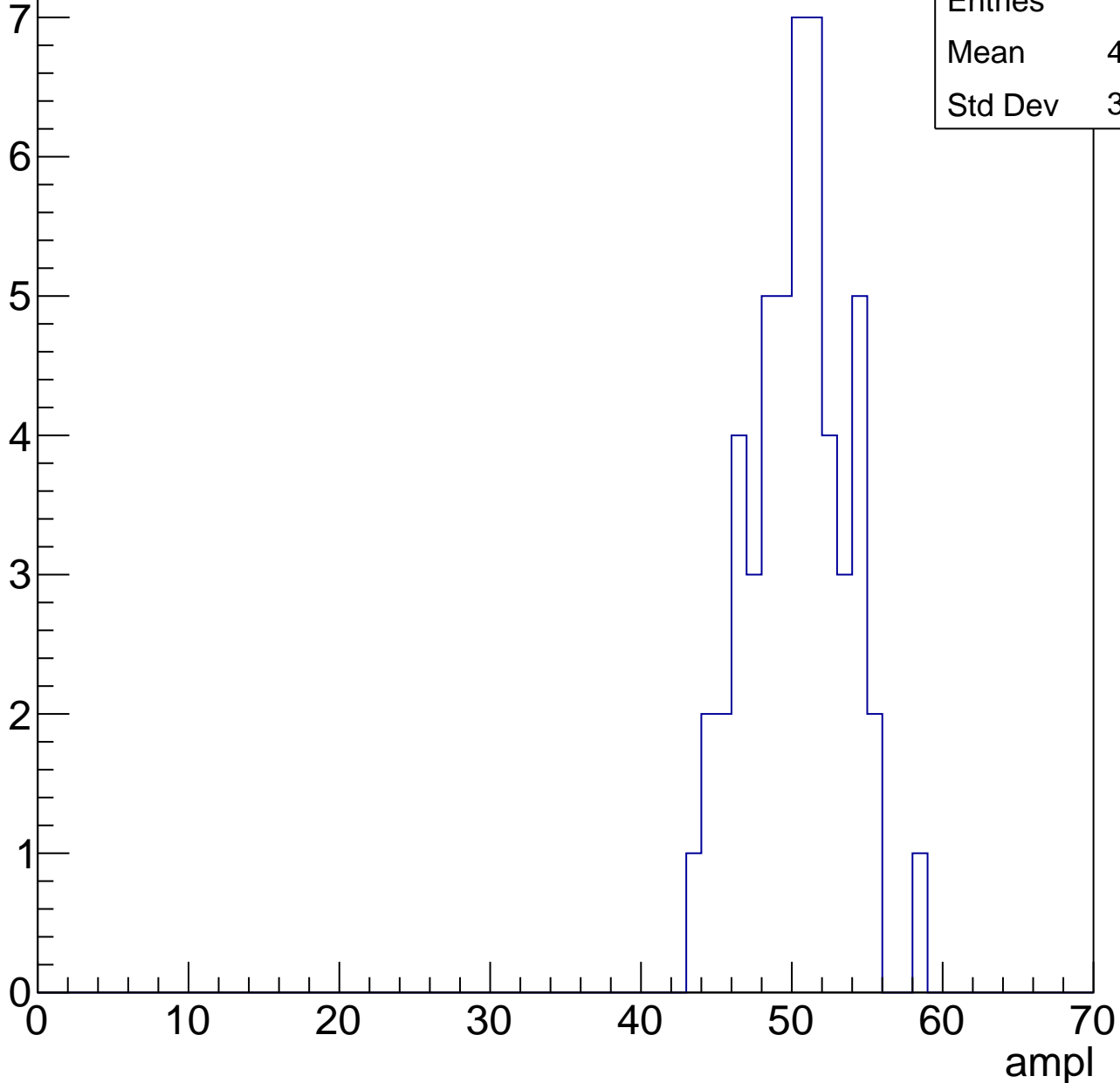


# B1L101S, U18-ch119, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	49.86
Std Dev	3.224

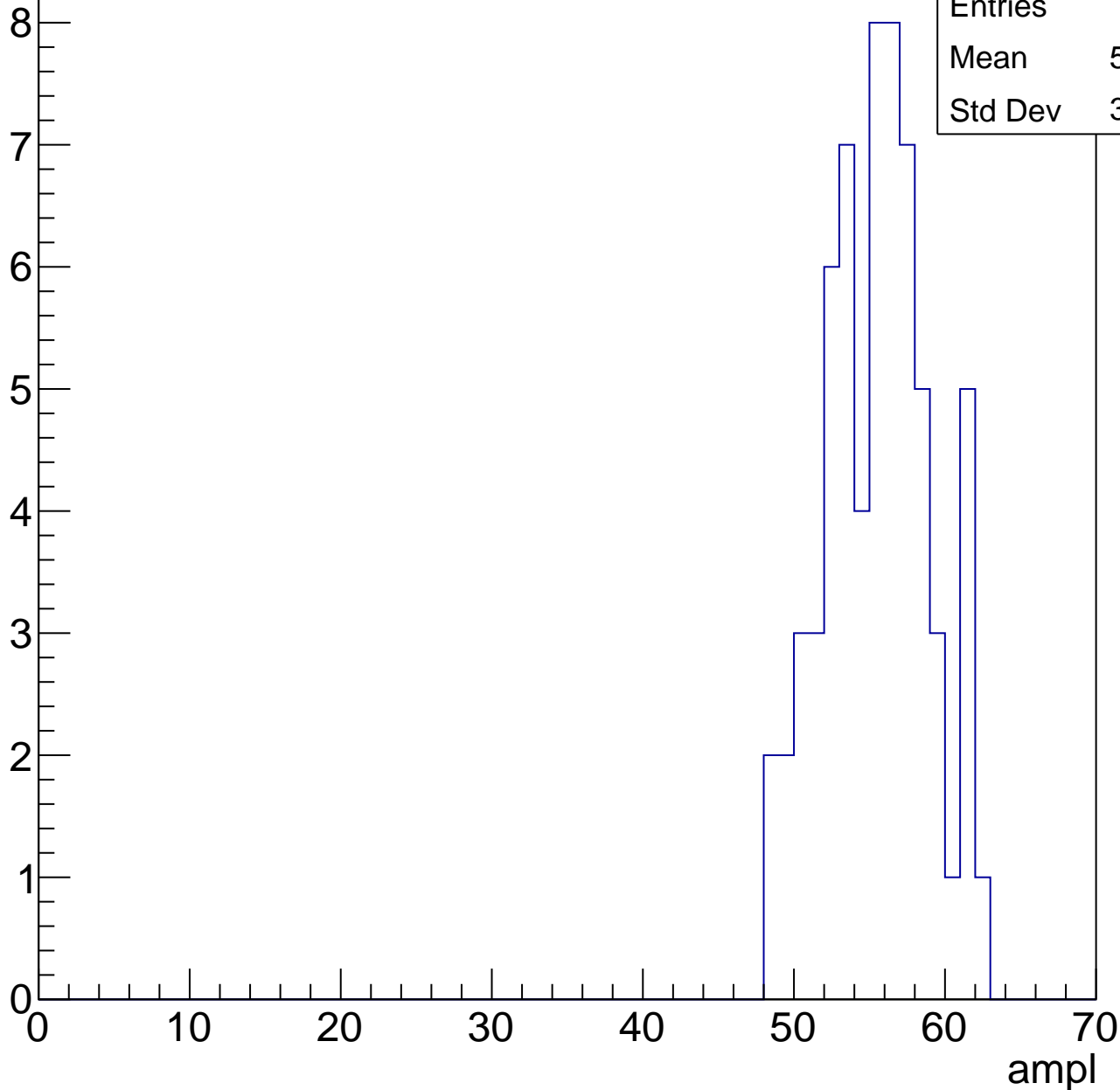


# B1L101S, U18-ch119, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	55.03
Std Dev	3.424

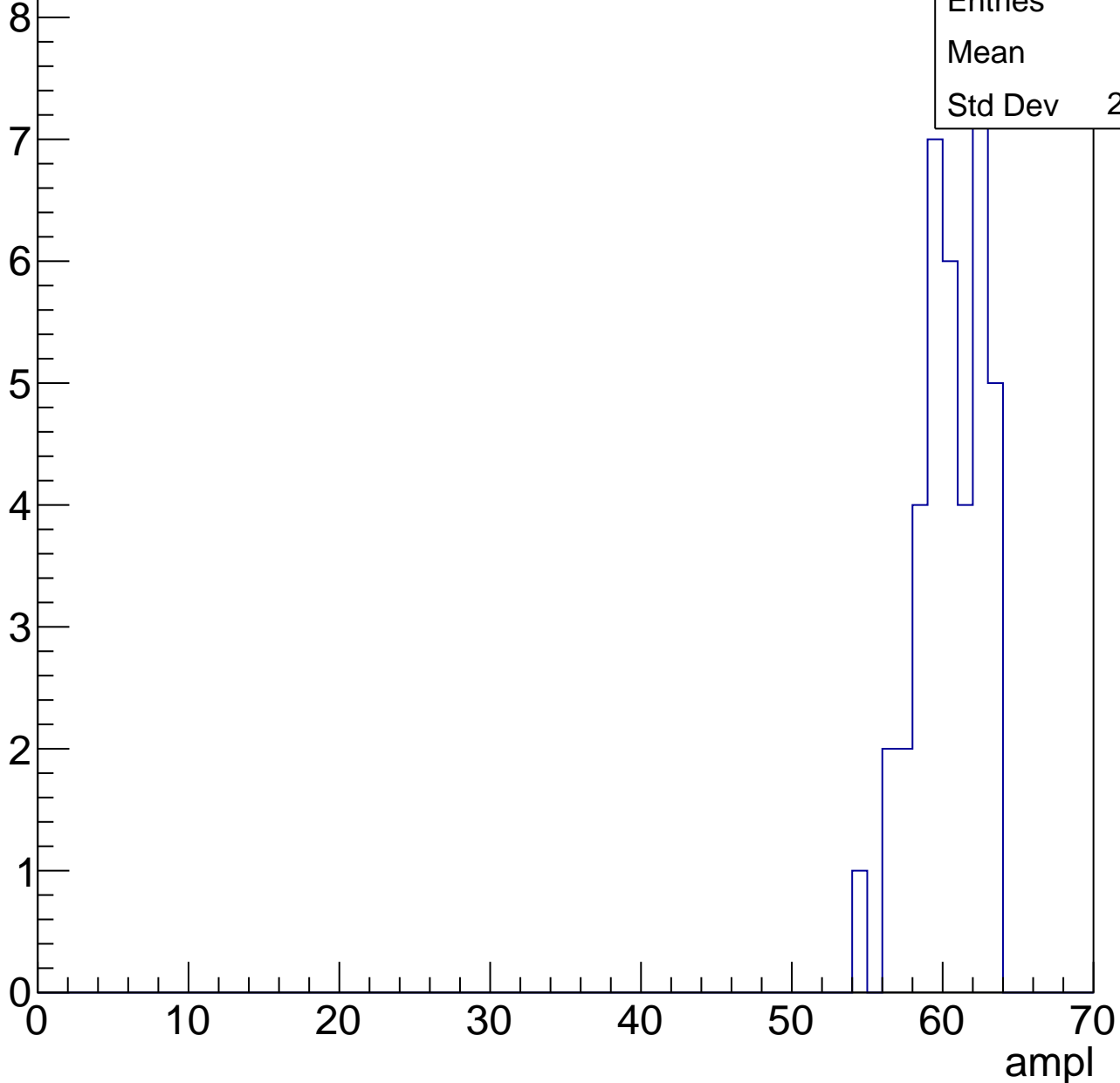


# B1L101S, U18-ch119, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

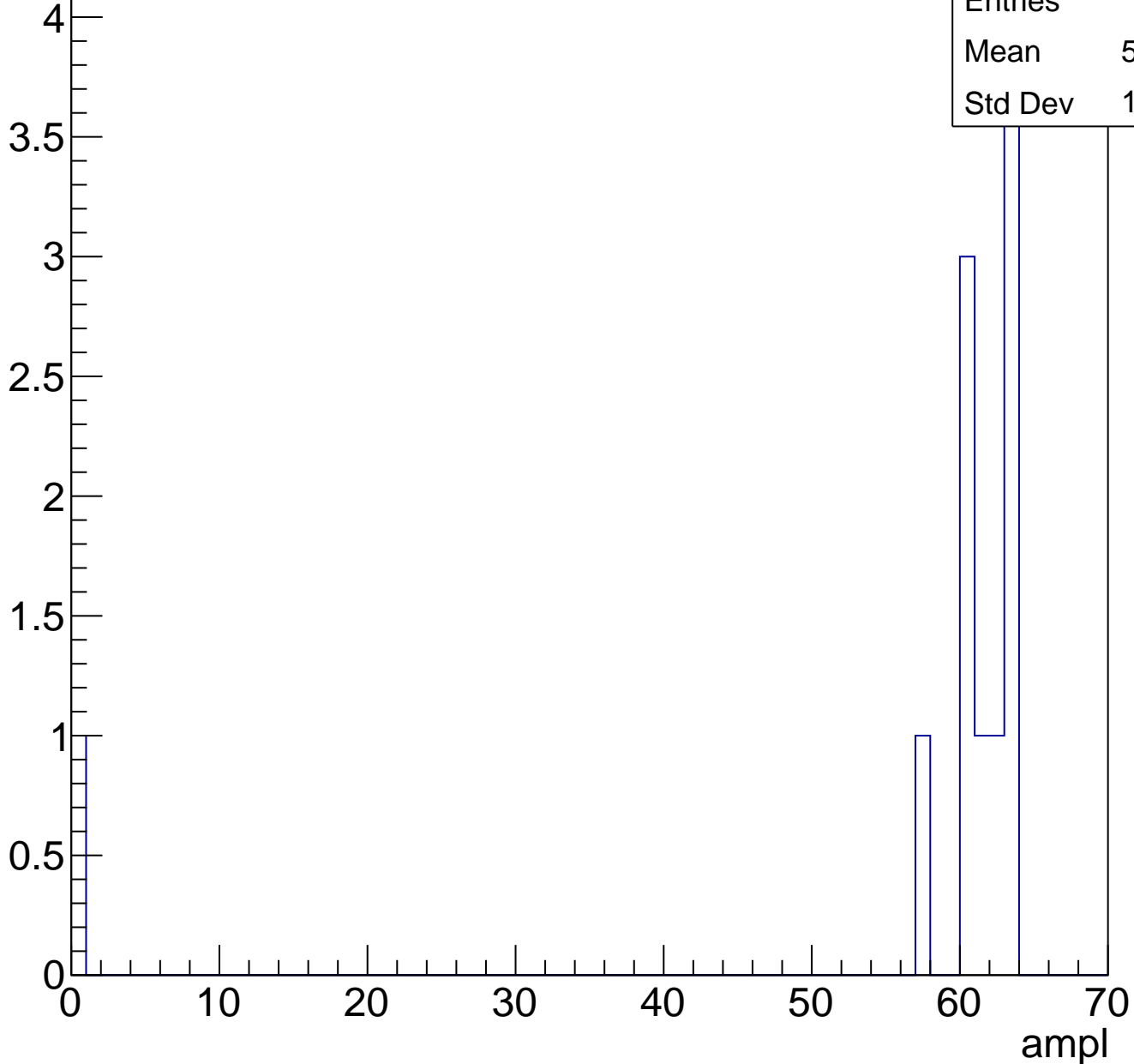
Entries	39
Mean	60
Std Dev	2.207



# B1L101S, U18-ch119, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch119, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch120, adc0

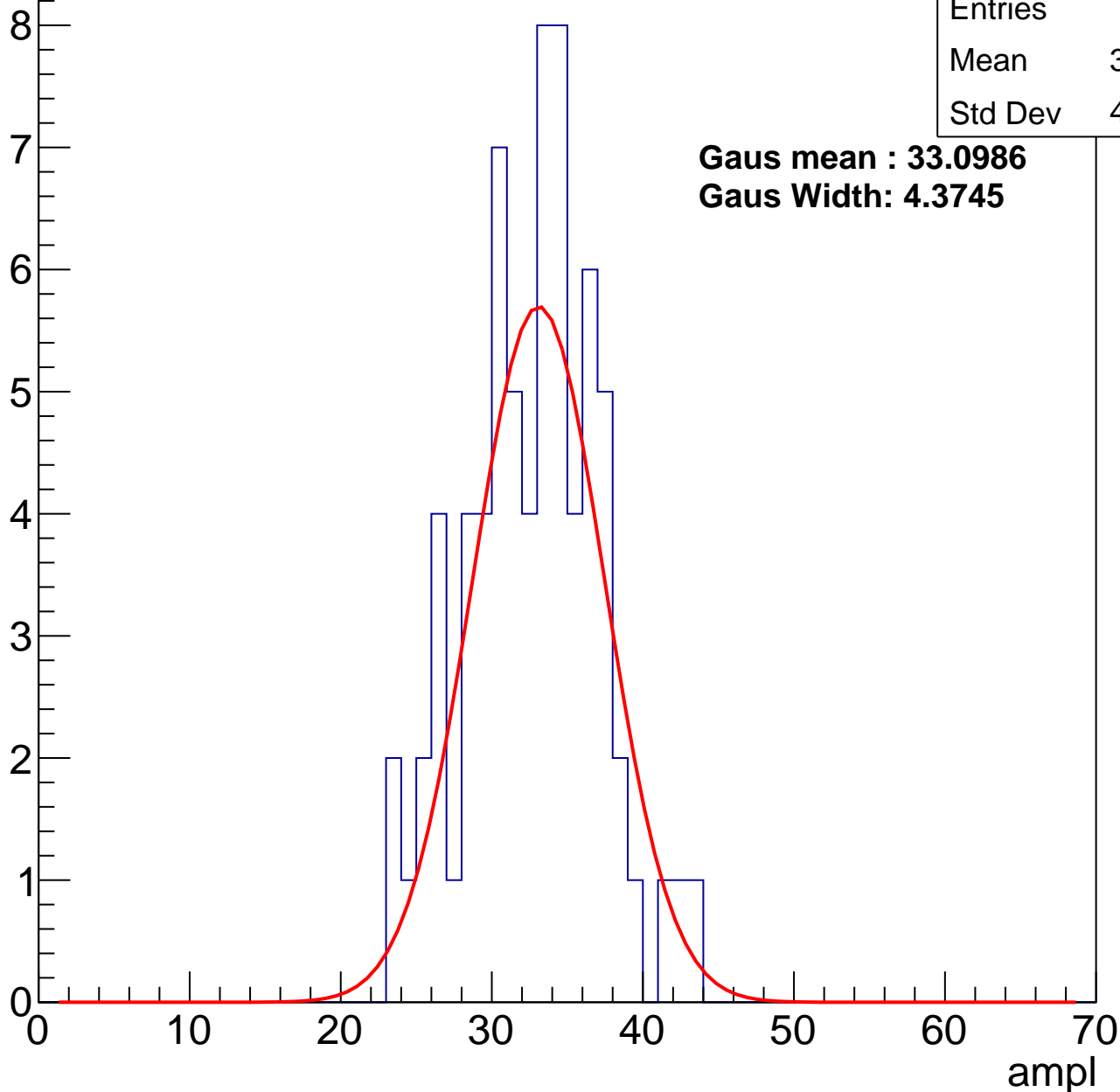
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	32.25
Std Dev	4.347

**Gaus mean : 33.0986**

**Gaus Width: 4.3745**



# B1L101S, U18-ch120, adc1

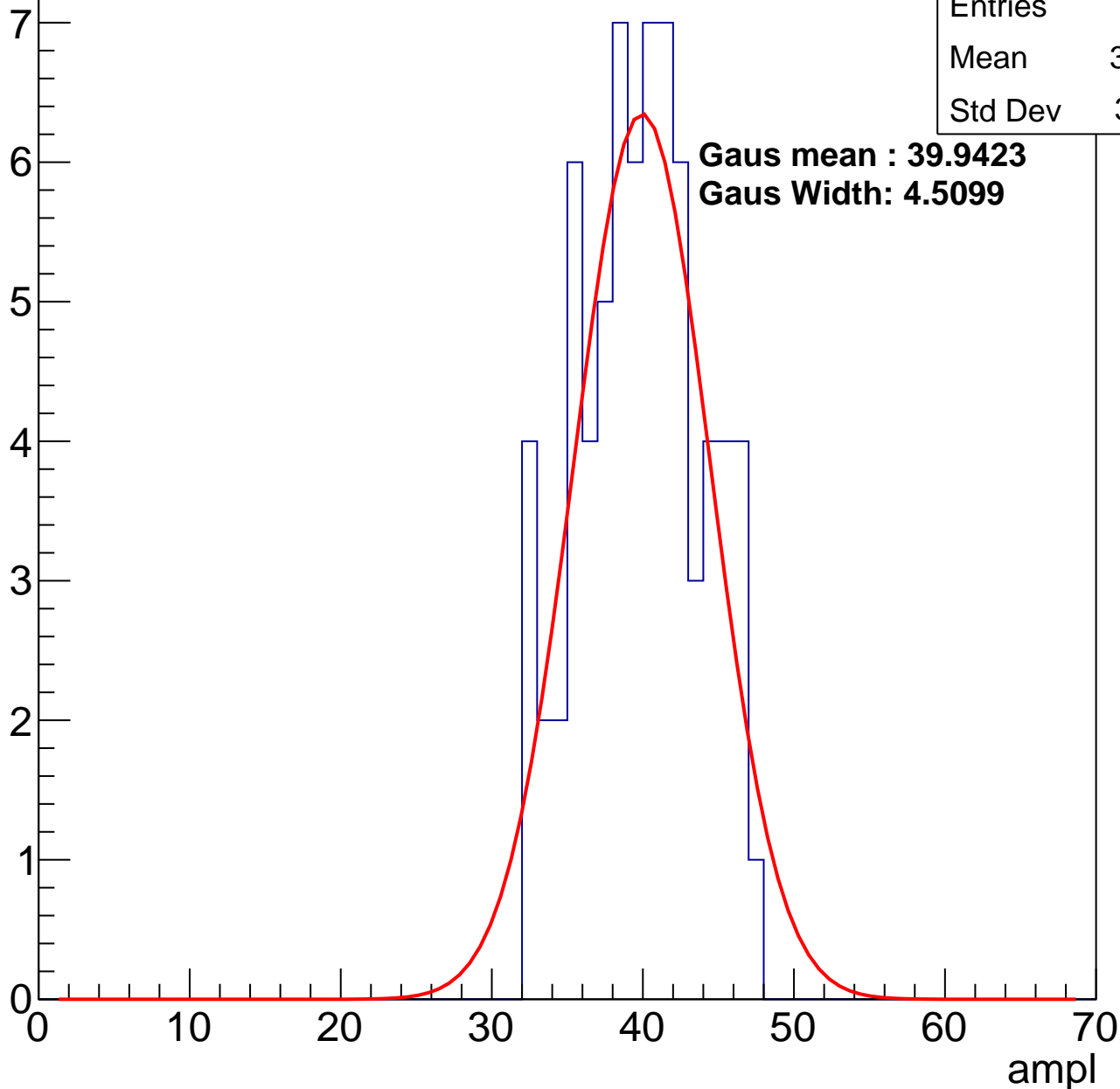
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	39.39
Std Dev	3.921

**Gaus mean : 39.9423**

**Gaus Width: 4.5099**



# B1L101S, U18-ch120, adc2

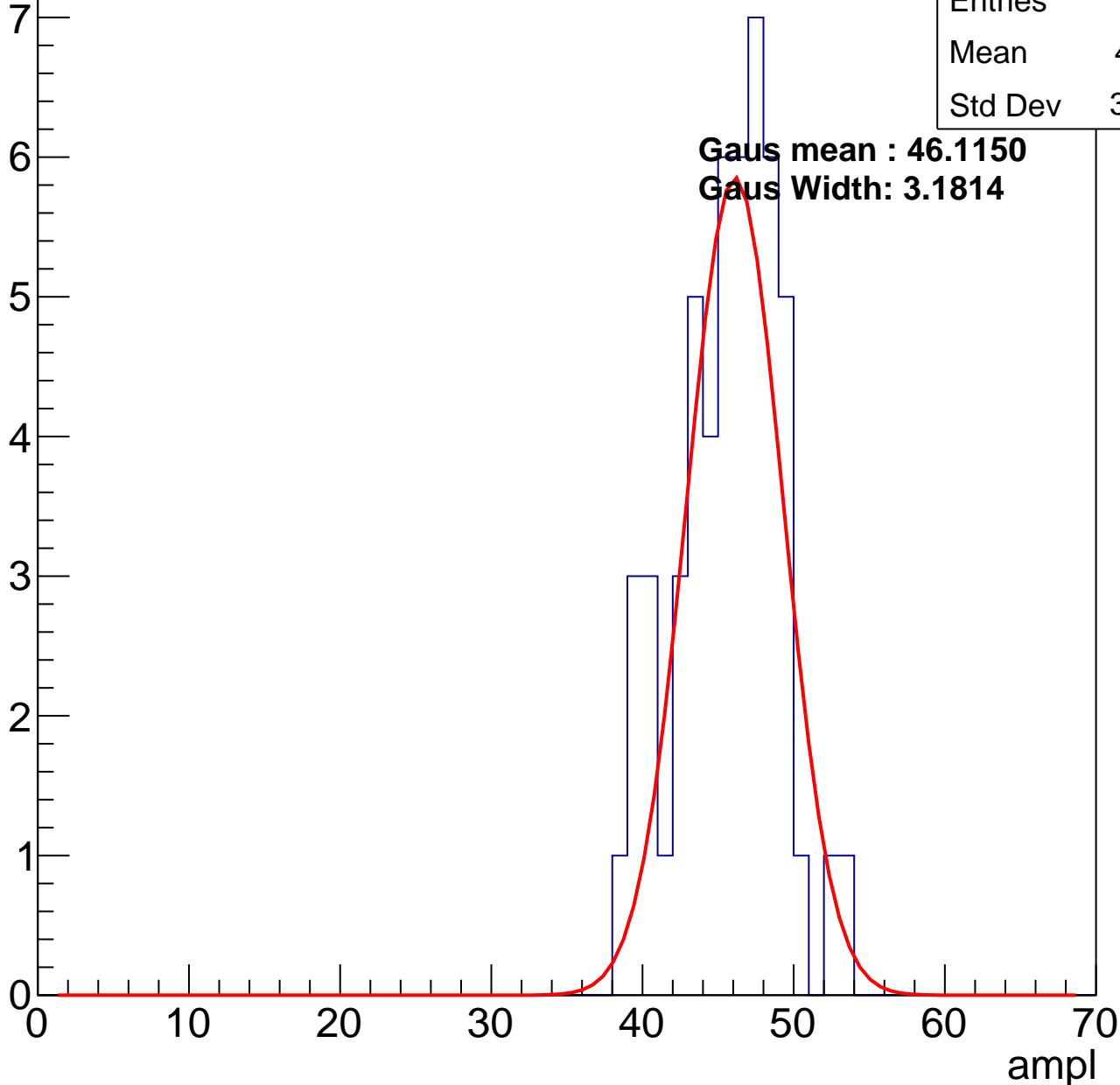
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	45.21
Std Dev	3.372

Gaus mean : 46.1150

Gaus Width: 3.1814

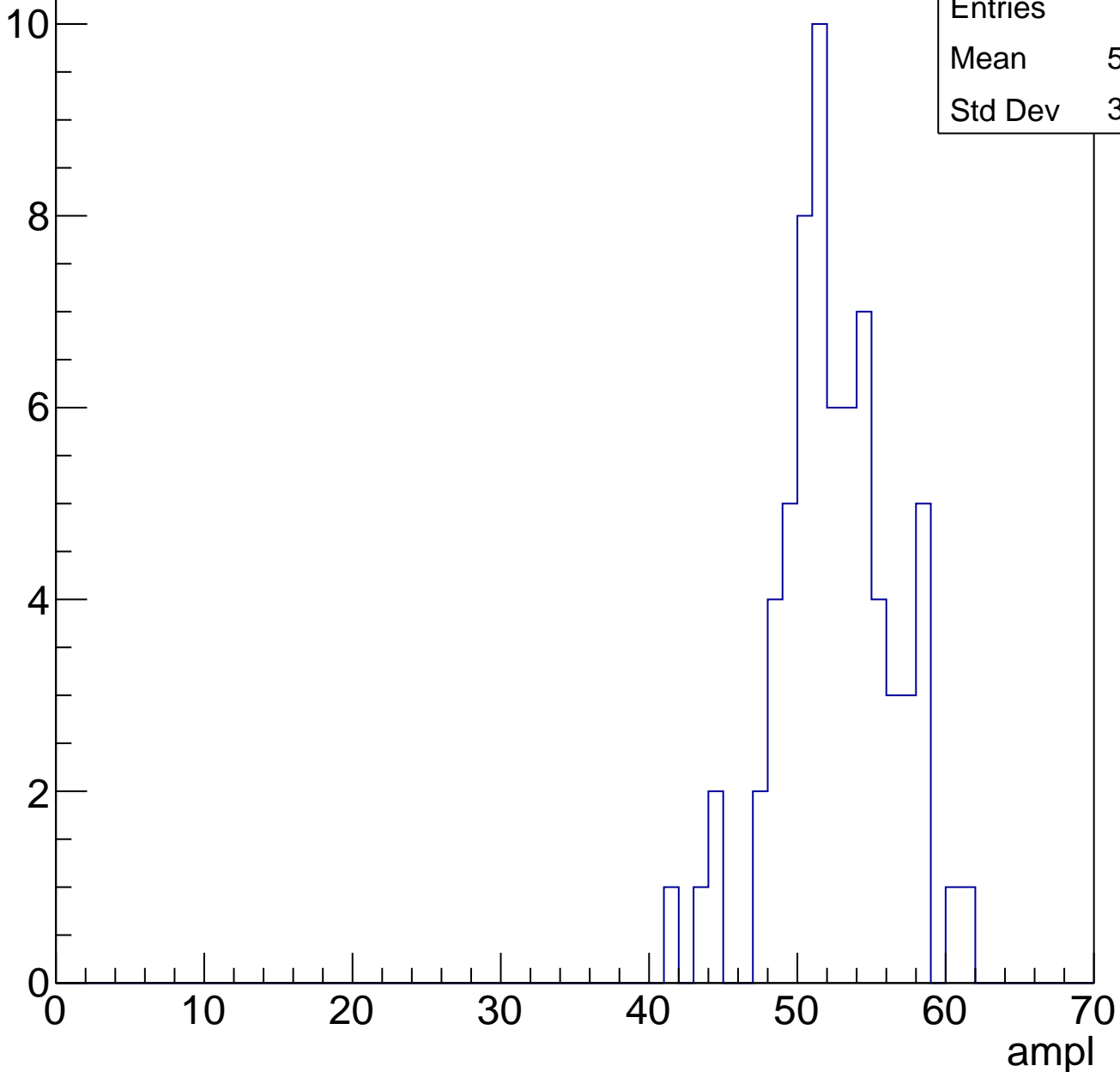


# B1L101S, U18-ch120, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	52.04
Std Dev	3.899

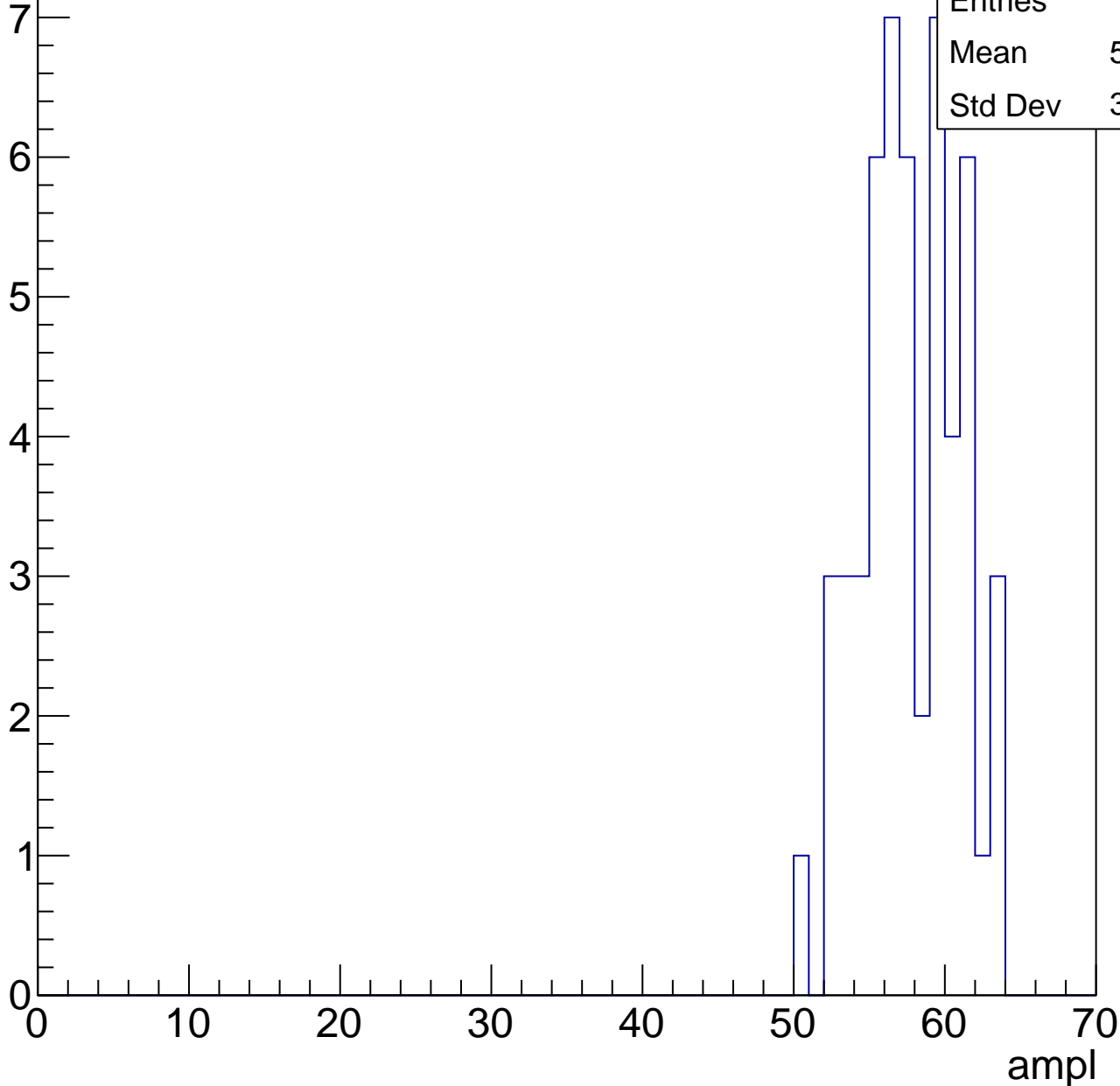


# B1L101S, U18-ch120, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	57.25
Std Dev	3.168

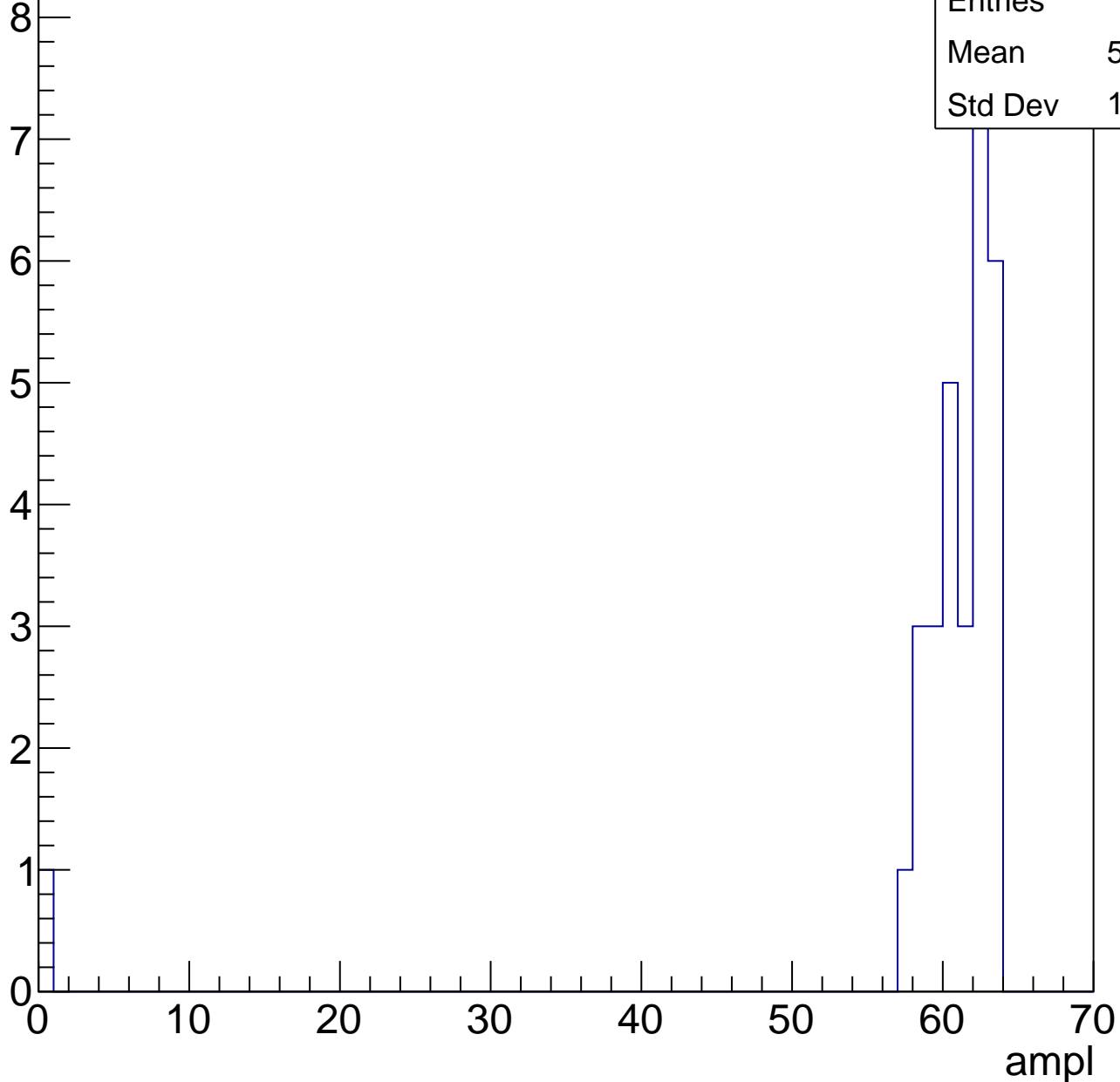


# B1L101S, U18-ch120, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	30
Mean	58.83
Std Dev	11.06



# B1L101S, U18-ch120, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch120, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U18-ch121, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	69
Mean	30.86
Std Dev	5.074

**Gaus mean : 31.7447**

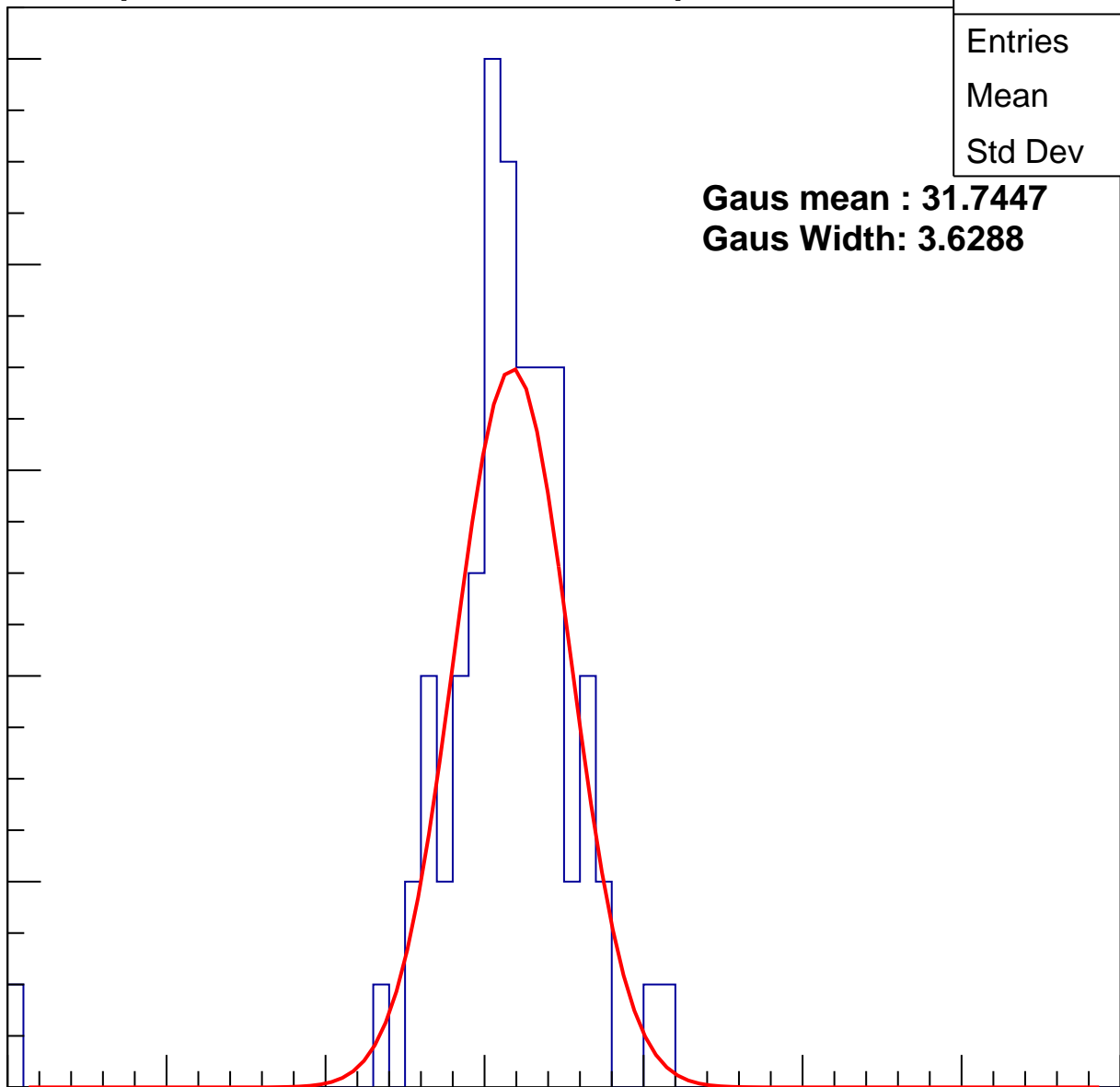
**Gaus Width: 3.6288**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U18-ch121, adc1

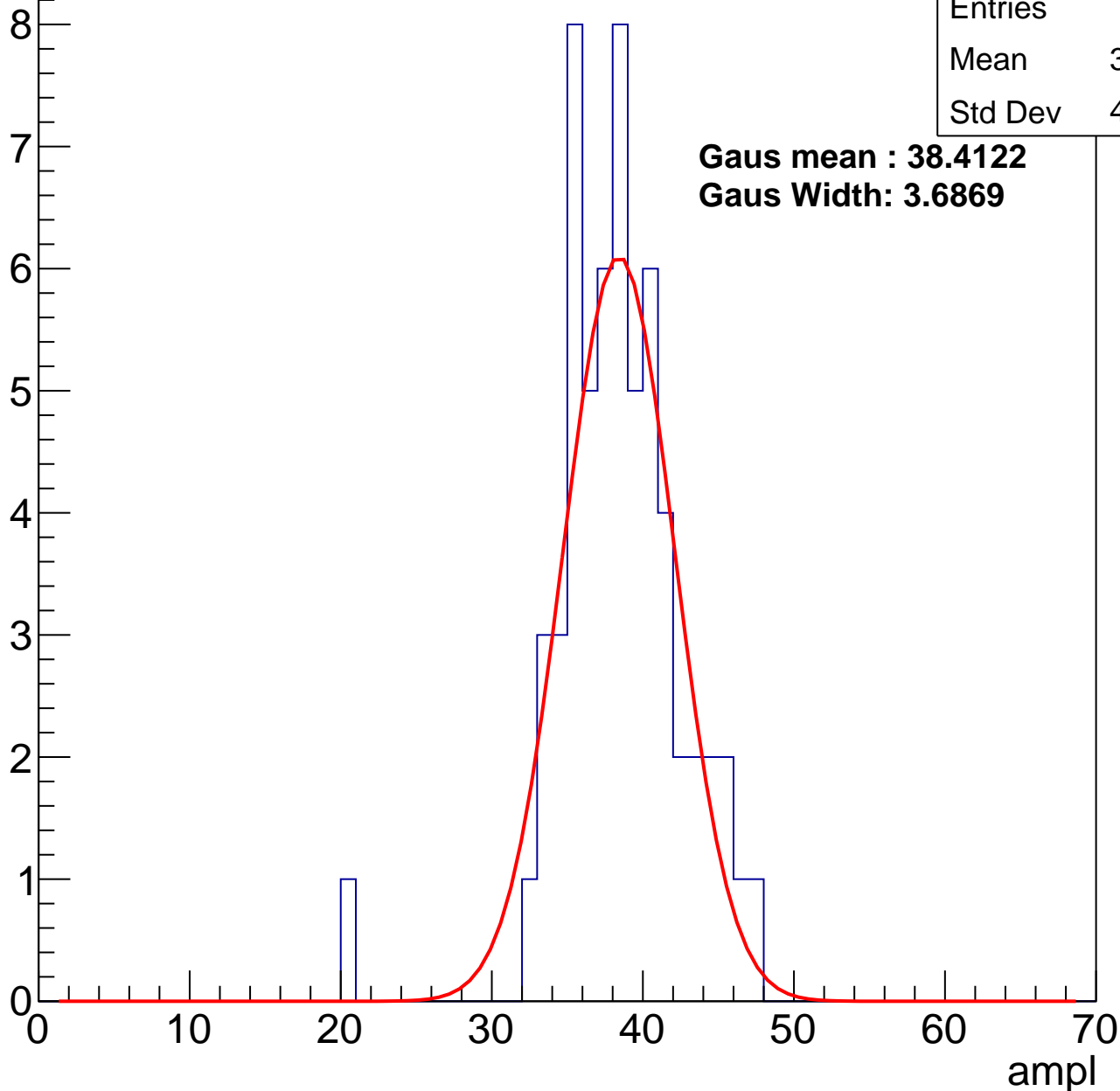
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	37.98
Std Dev	4.169

**Gaus mean : 38.4122**

**Gaus Width: 3.6869**



# B1L101S, U18-ch121, adc2

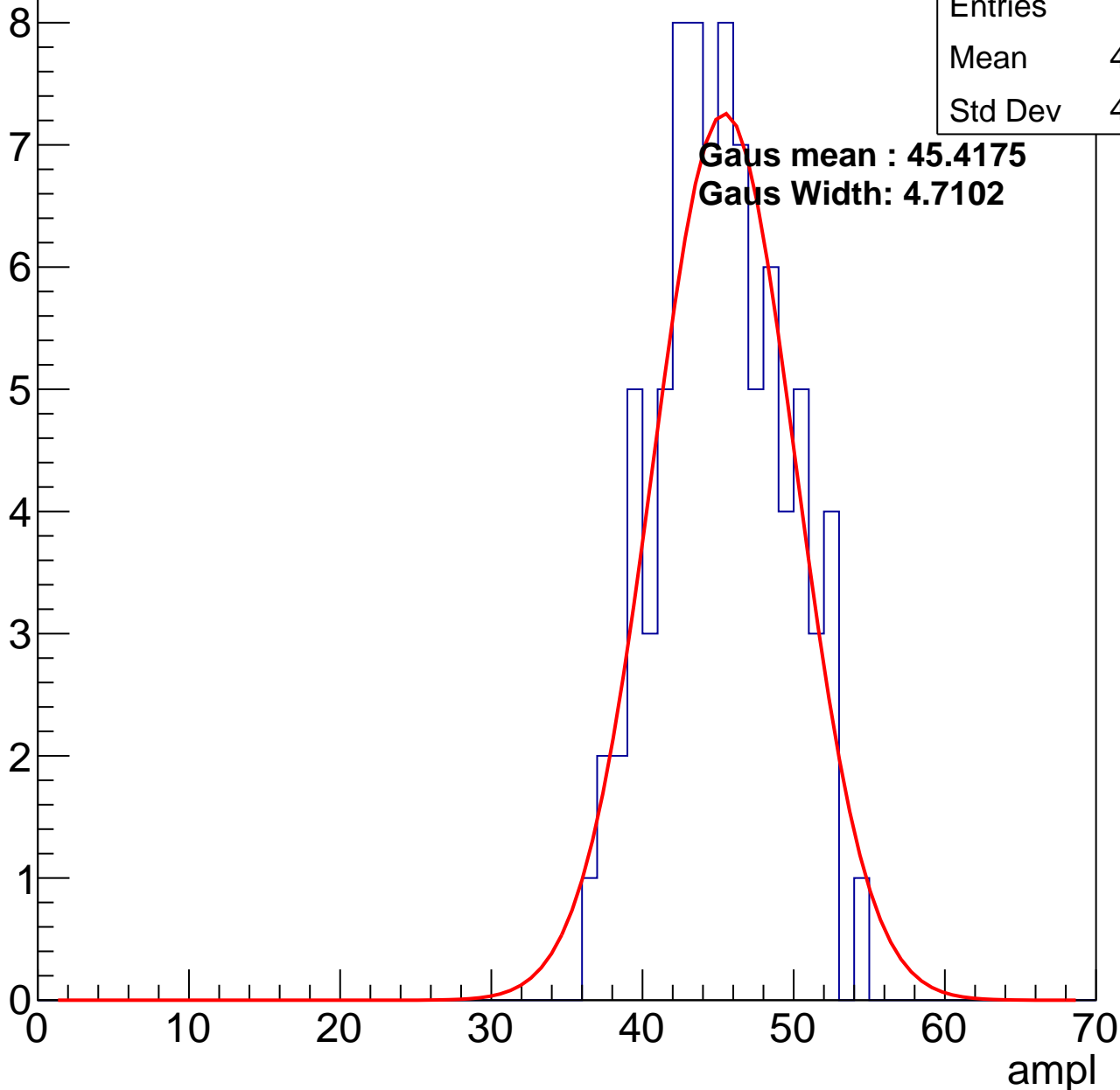
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	84
Mean	44.76
Std Dev	4.087

**Gaus mean : 45.4175**

**Gaus Width: 4.7102**

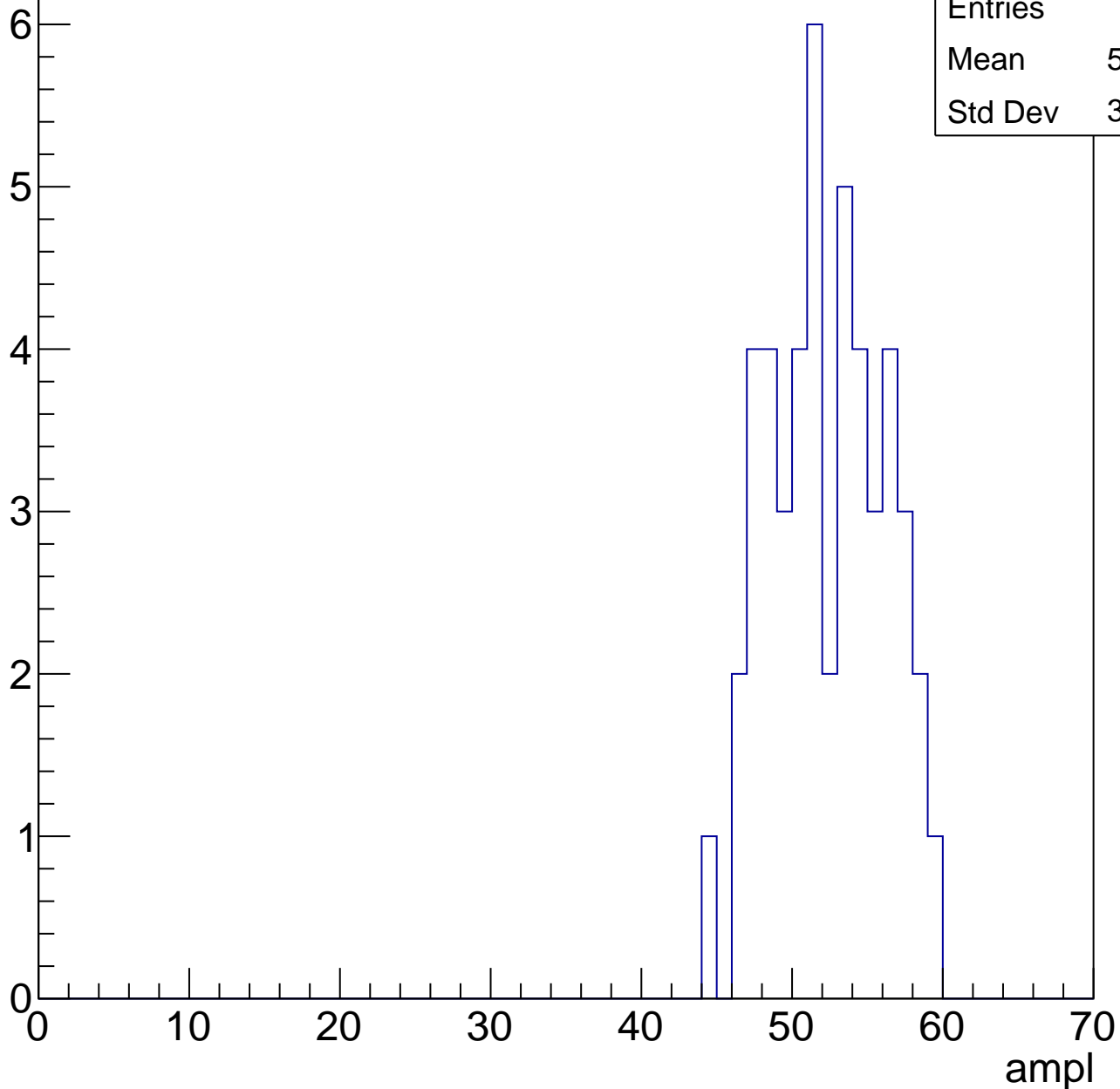


# B1L101S, U18-ch121, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	48
Mean	51.85
Std Dev	3.697

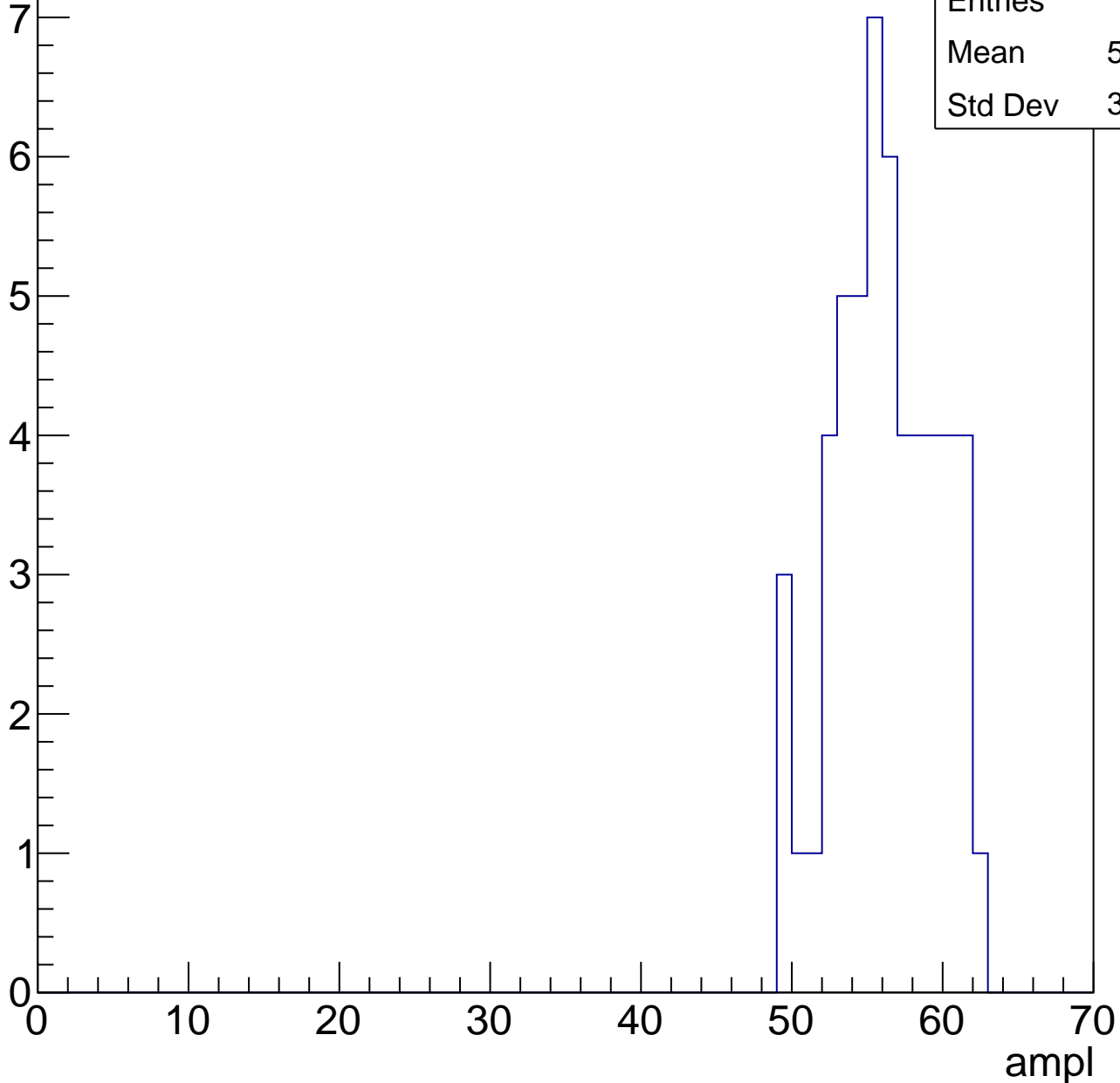


# B1L101S, U18-ch121, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	55.74
Std Dev	3.354

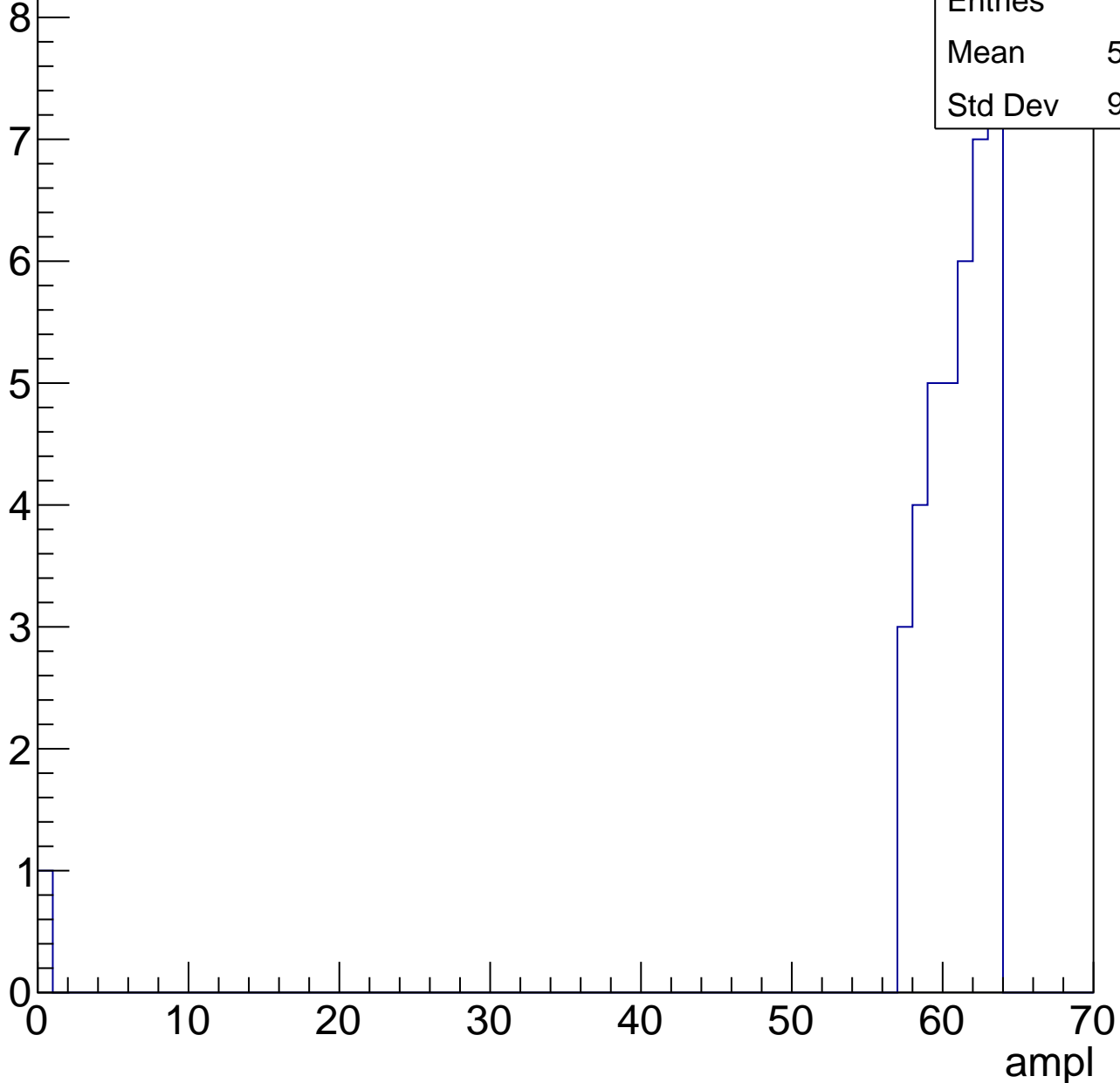


# B1L101S, U18-ch121, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	39
Mean	59.03
Std Dev	9.763



# B1L101S, U18-ch121, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

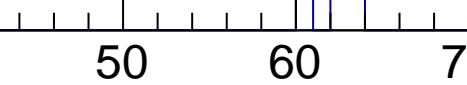
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	61.75
Std Dev	1.09

0 10 20 30 40 50 60 70

ampl





# B1L101S, U18-ch121, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch122, adc0

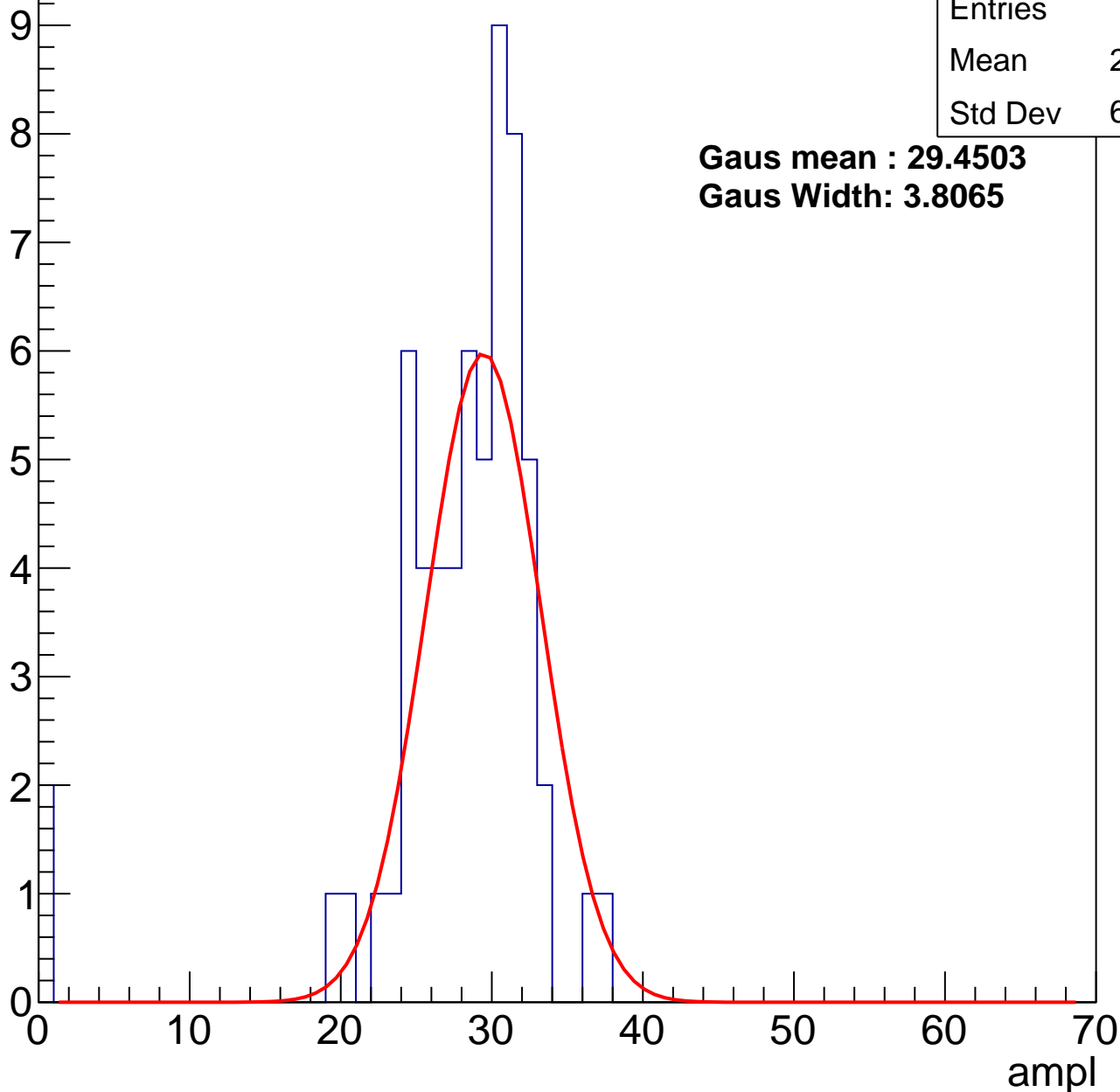
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	27.38
Std Dev	6.128

**Gaus mean : 29.4503**

**Gaus Width: 3.8065**



# B1L101S, U18-ch122, adc1

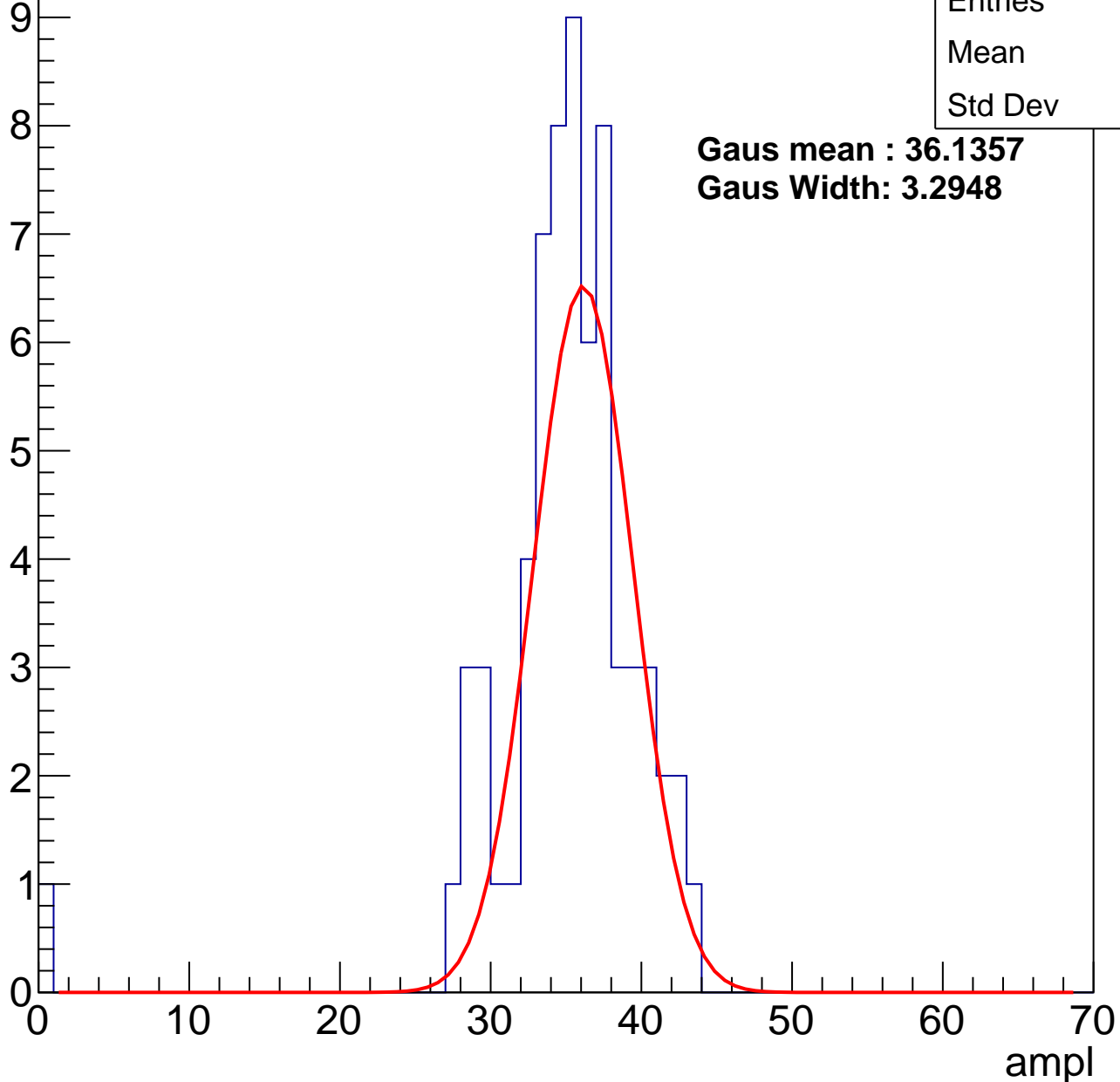
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	34.5
Std Dev	5.59

**Gaus mean : 36.1357**

**Gaus Width: 3.2948**



# B1L101S, U18-ch122, adc2

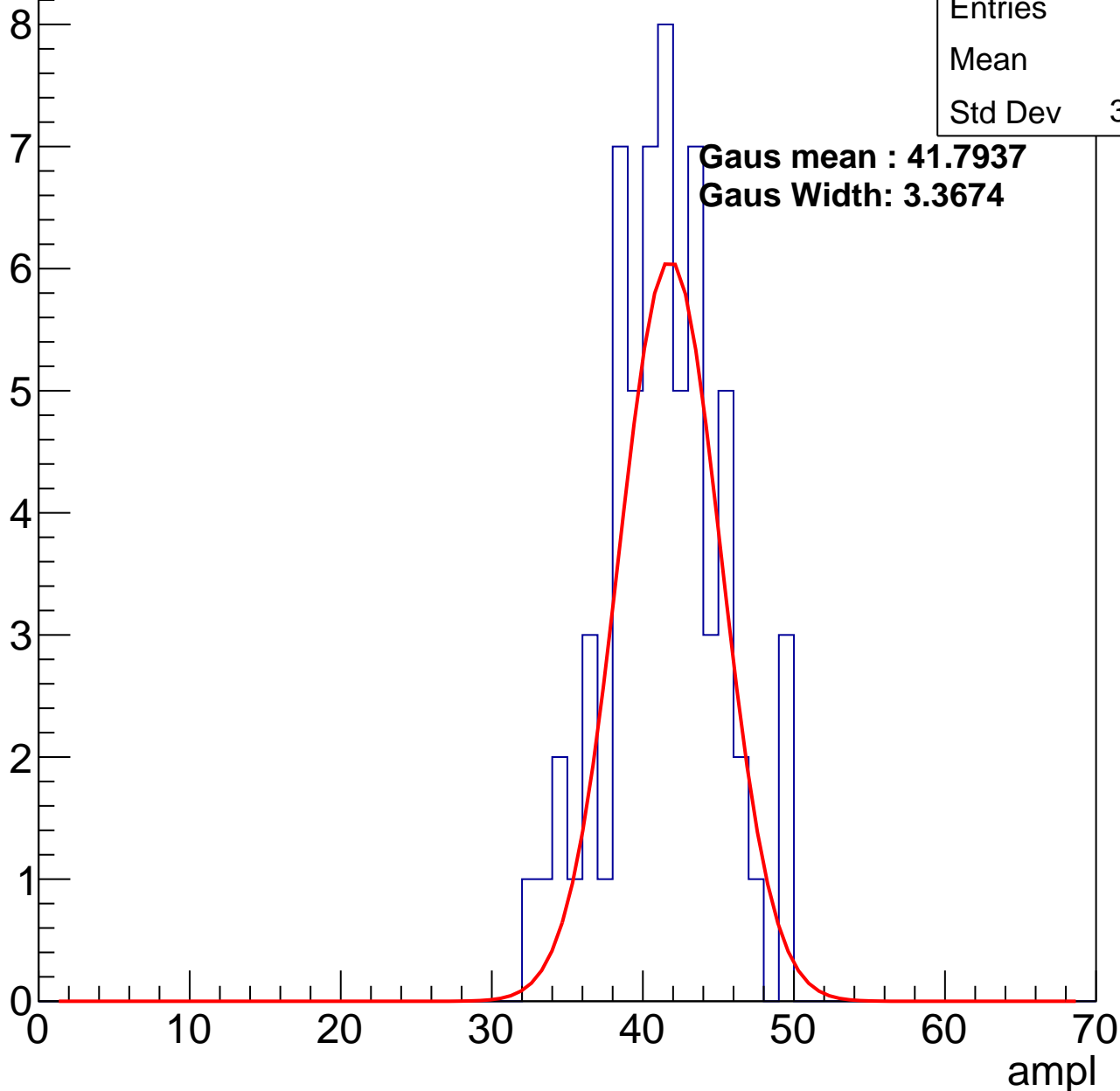
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	40.9
Std Dev	3.762

**Gaus mean : 41.7937**

**Gaus Width: 3.3674**

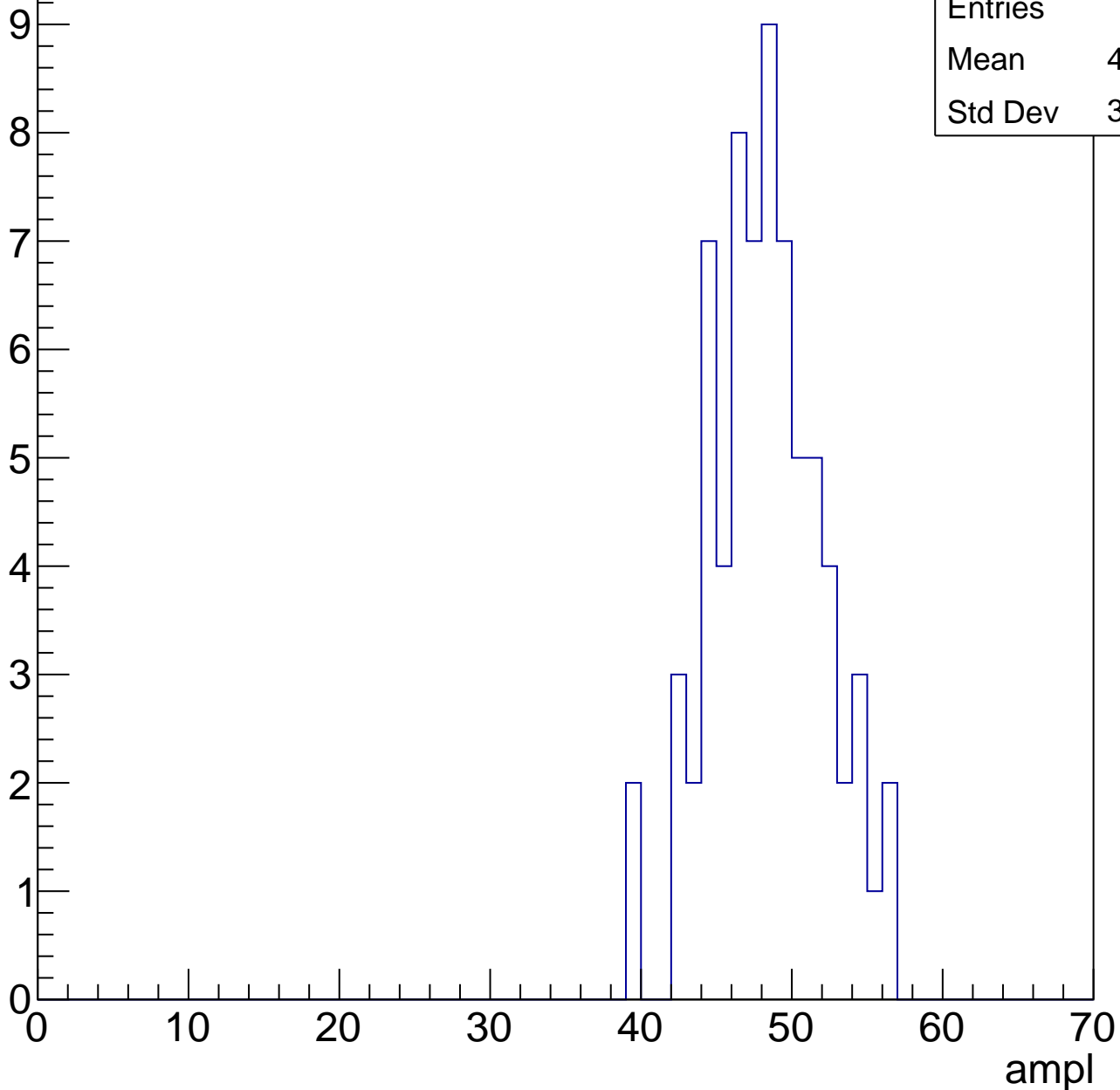


# B1L101S, U18-ch122, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	47.86
Std Dev	3.709

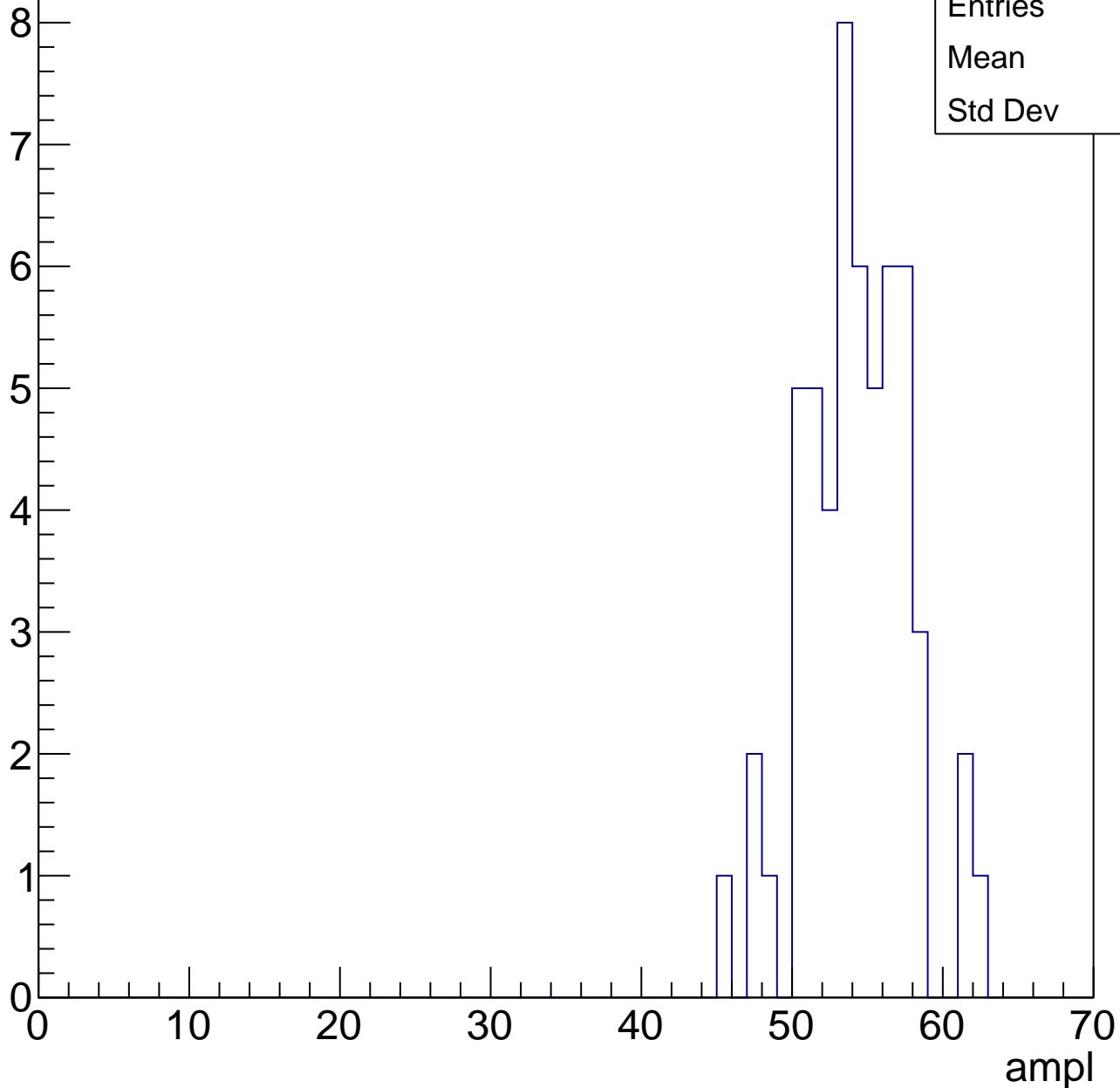


# B1L101S, U18-ch122, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	53.8
Std Dev	3.45



# B1L101S, U18-ch122, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	59.15
Std Dev	2.755

10

8

6

4

2

0

0

10

20

30

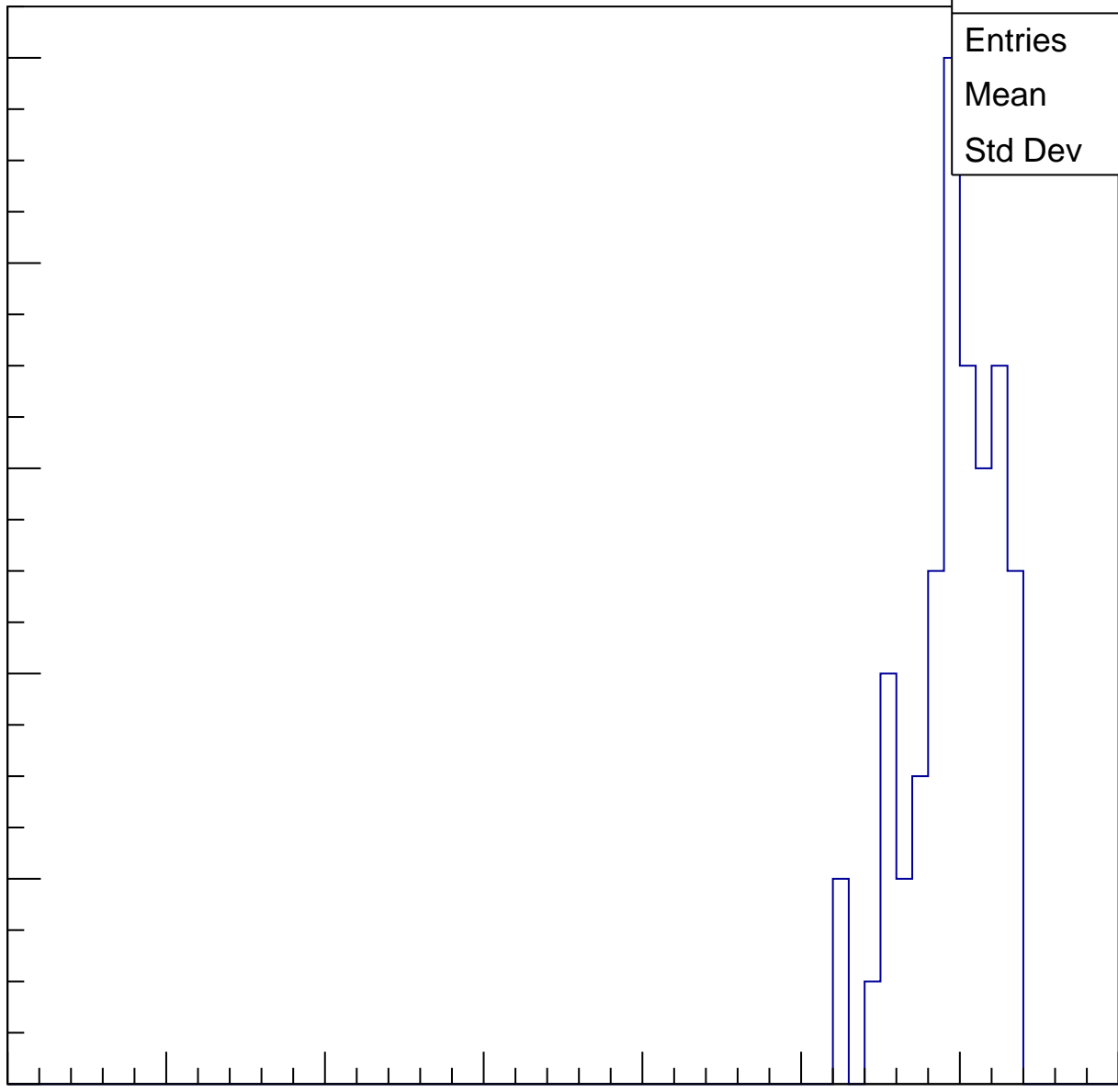
40

50

60

ampl

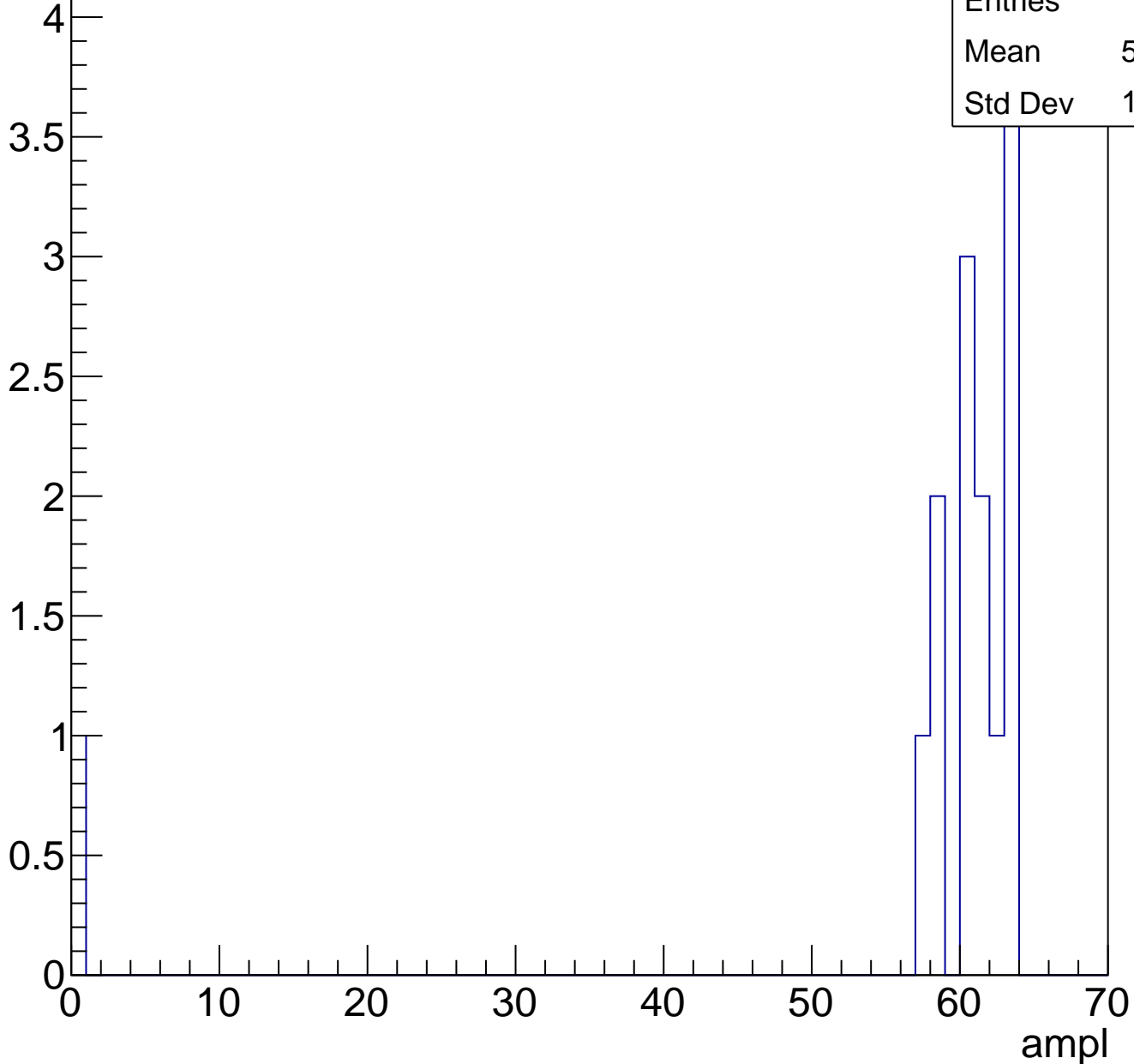
70



# B1L101S, U18-ch122, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

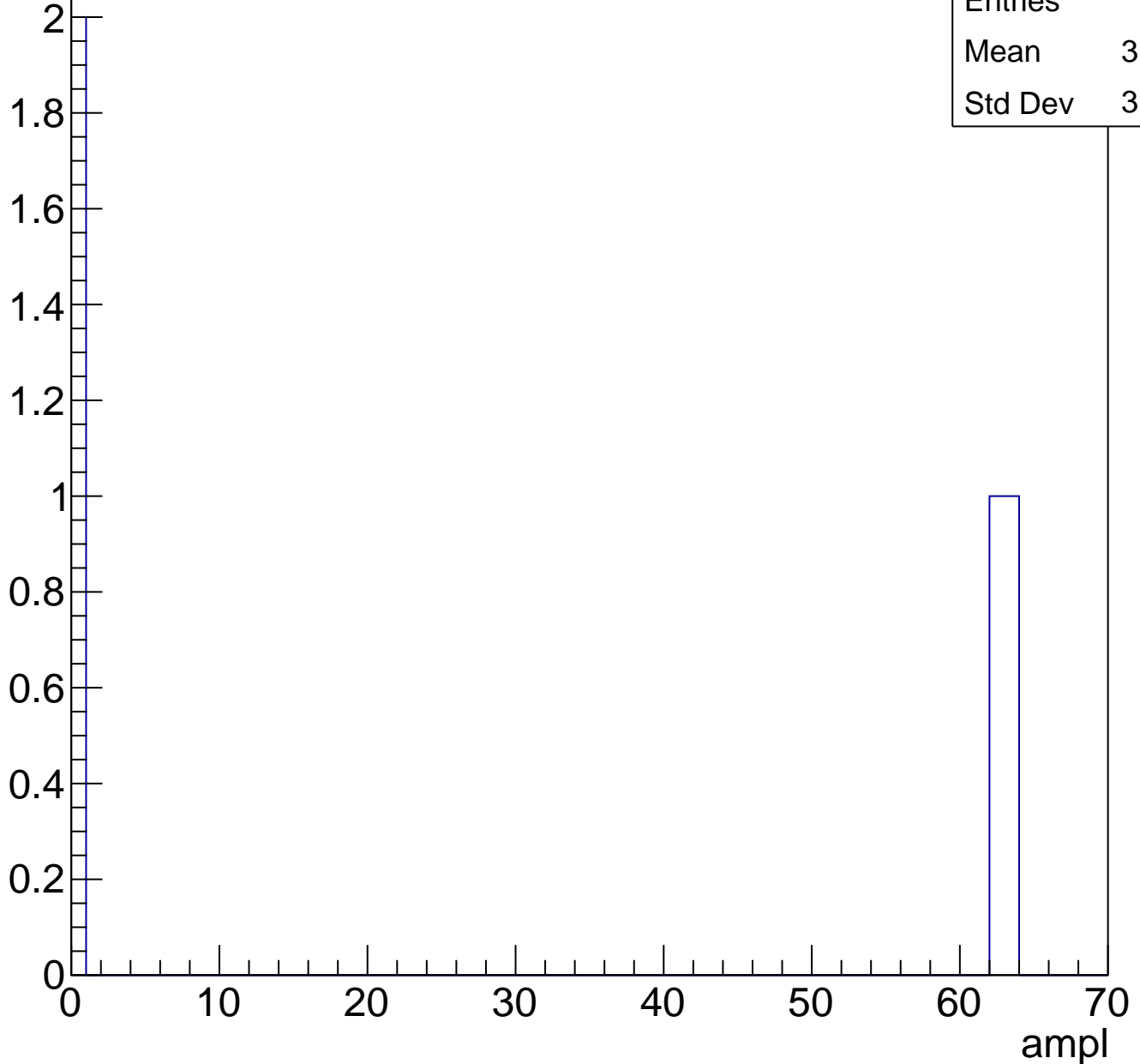




# B1L101S, U18-ch122, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch123, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	78
Mean	30.83
Std Dev	3.684

**Gaus mean : 31.5189**

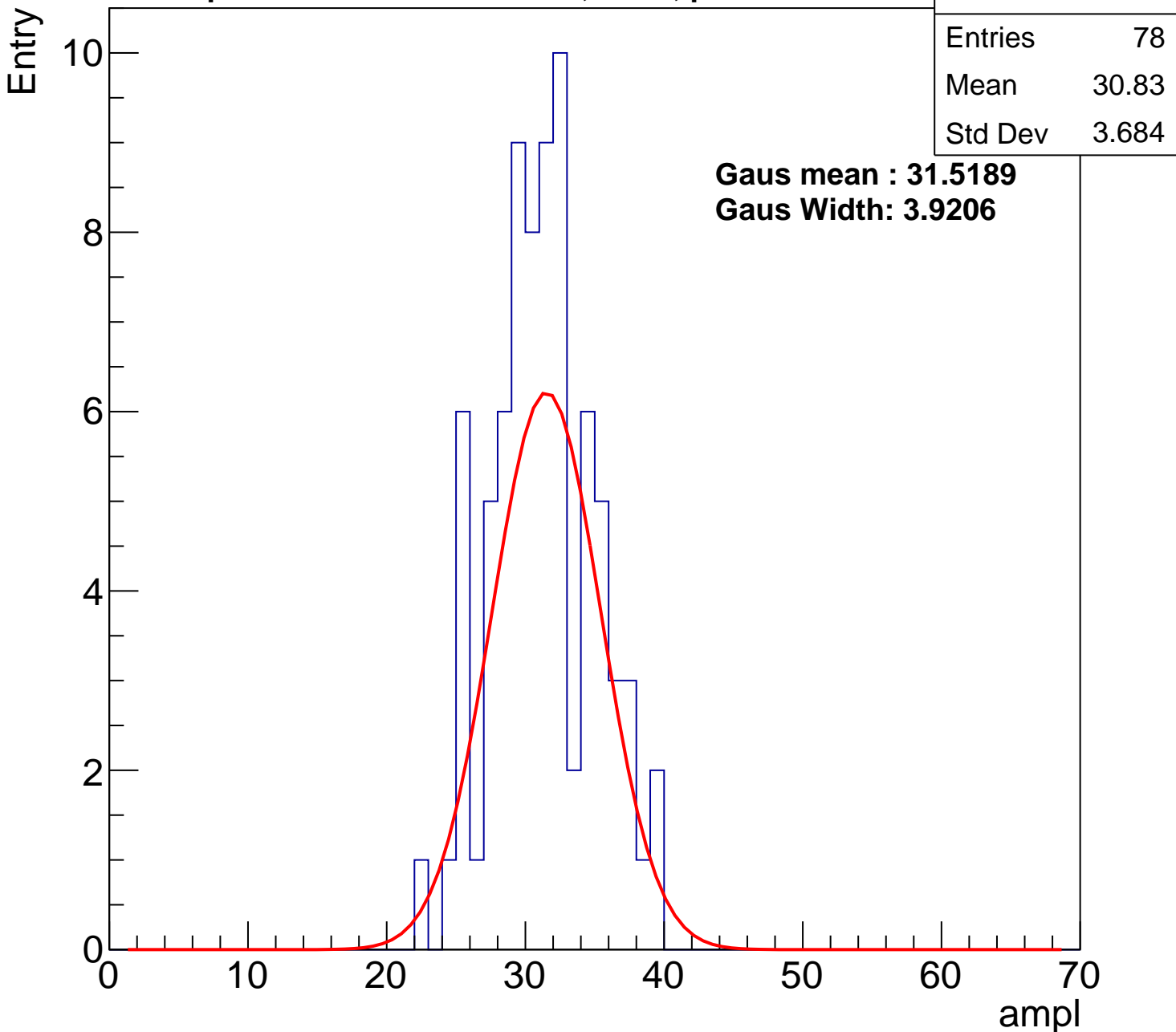
**Gaus Width: 3.9206**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U18-ch123, adc1

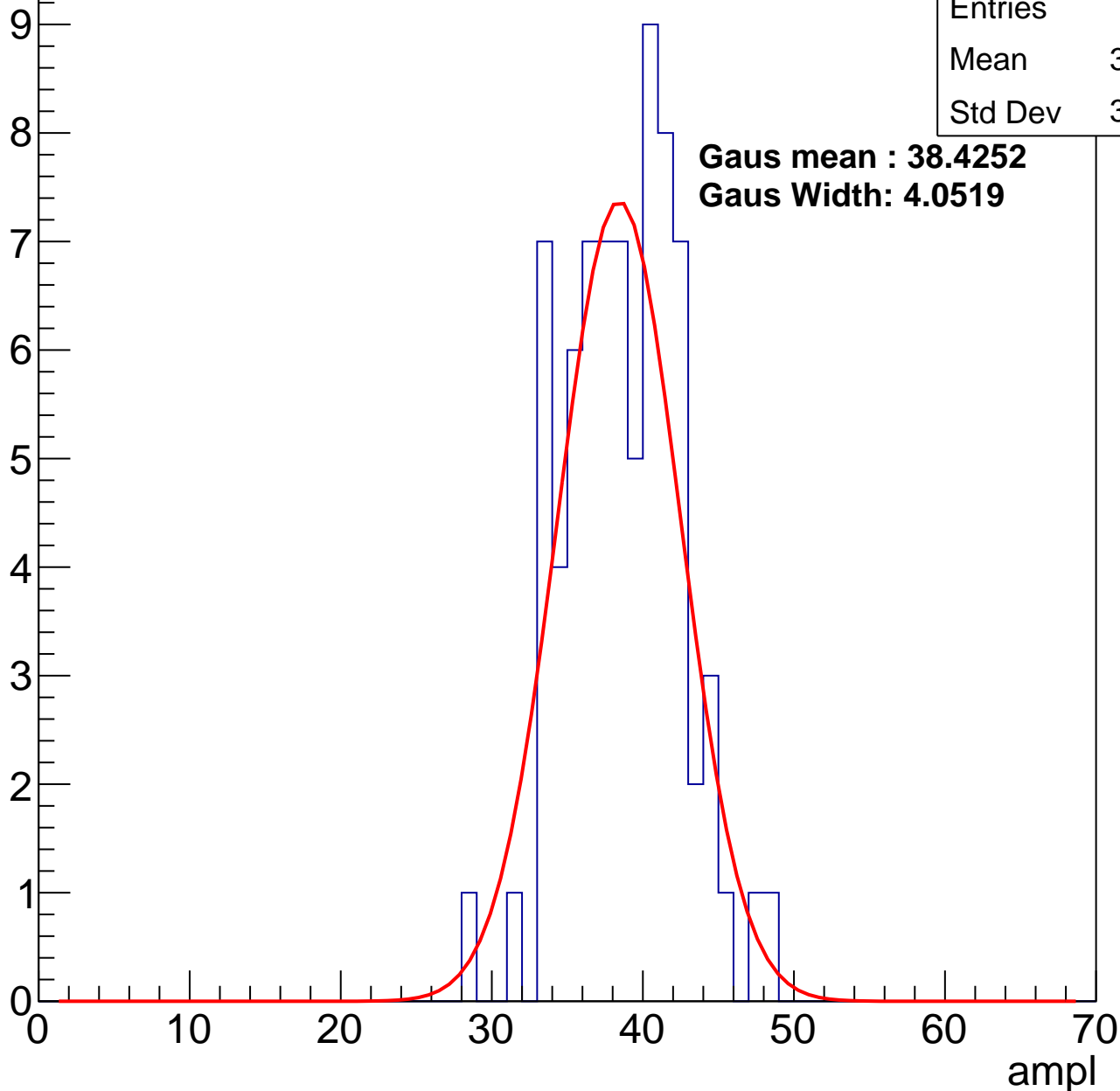
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	38.29
Std Dev	3.752

**Gaus mean : 38.4252**

**Gaus Width: 4.0519**



# B1L101S, U18-ch123, adc2

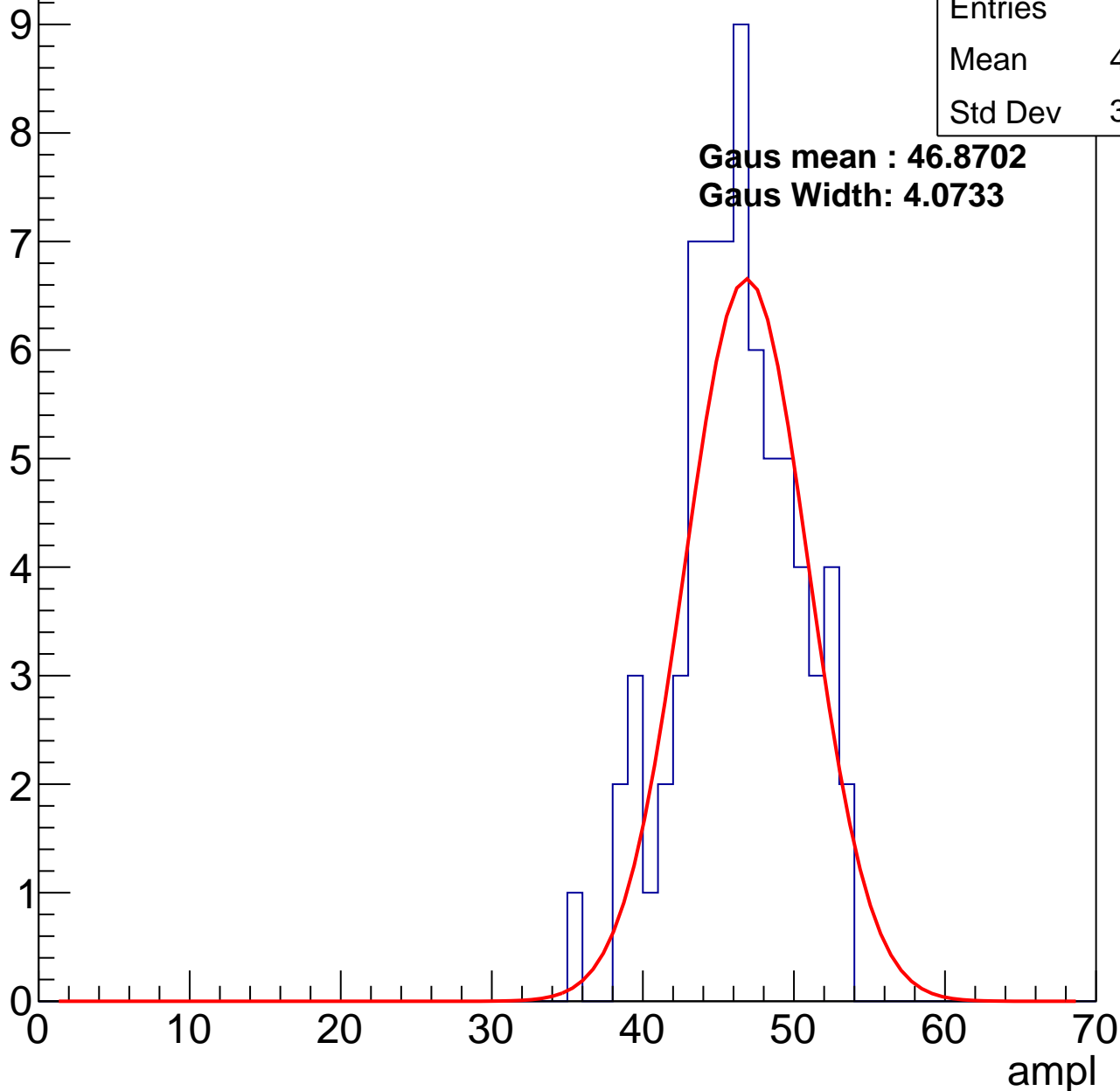
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	45.75
Std Dev	3.892

**Gaus mean : 46.8702**

**Gaus Width: 4.0733**

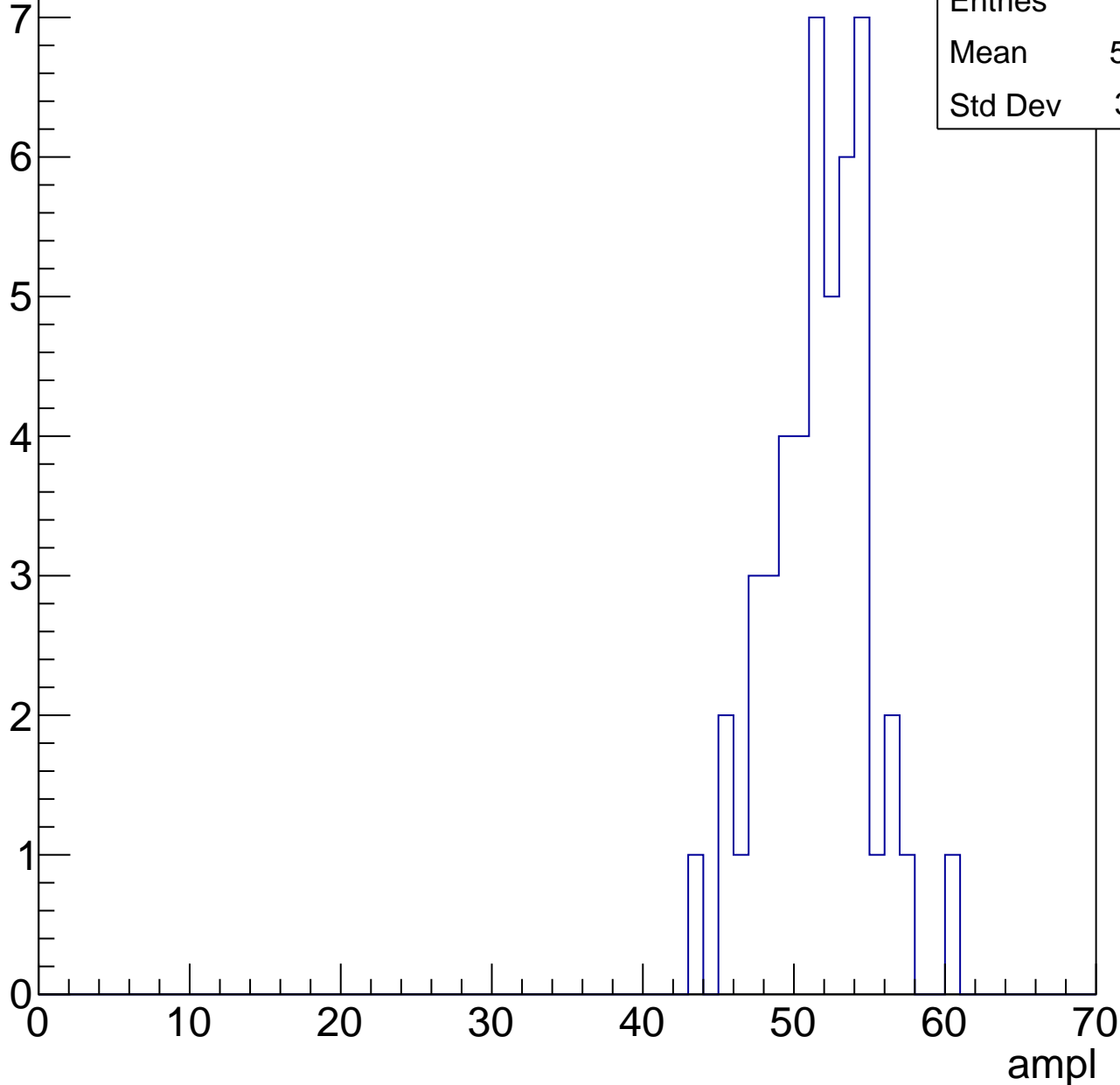


# B1L101S, U18-ch123, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	48
Mean	51.19
Std Dev	3.321

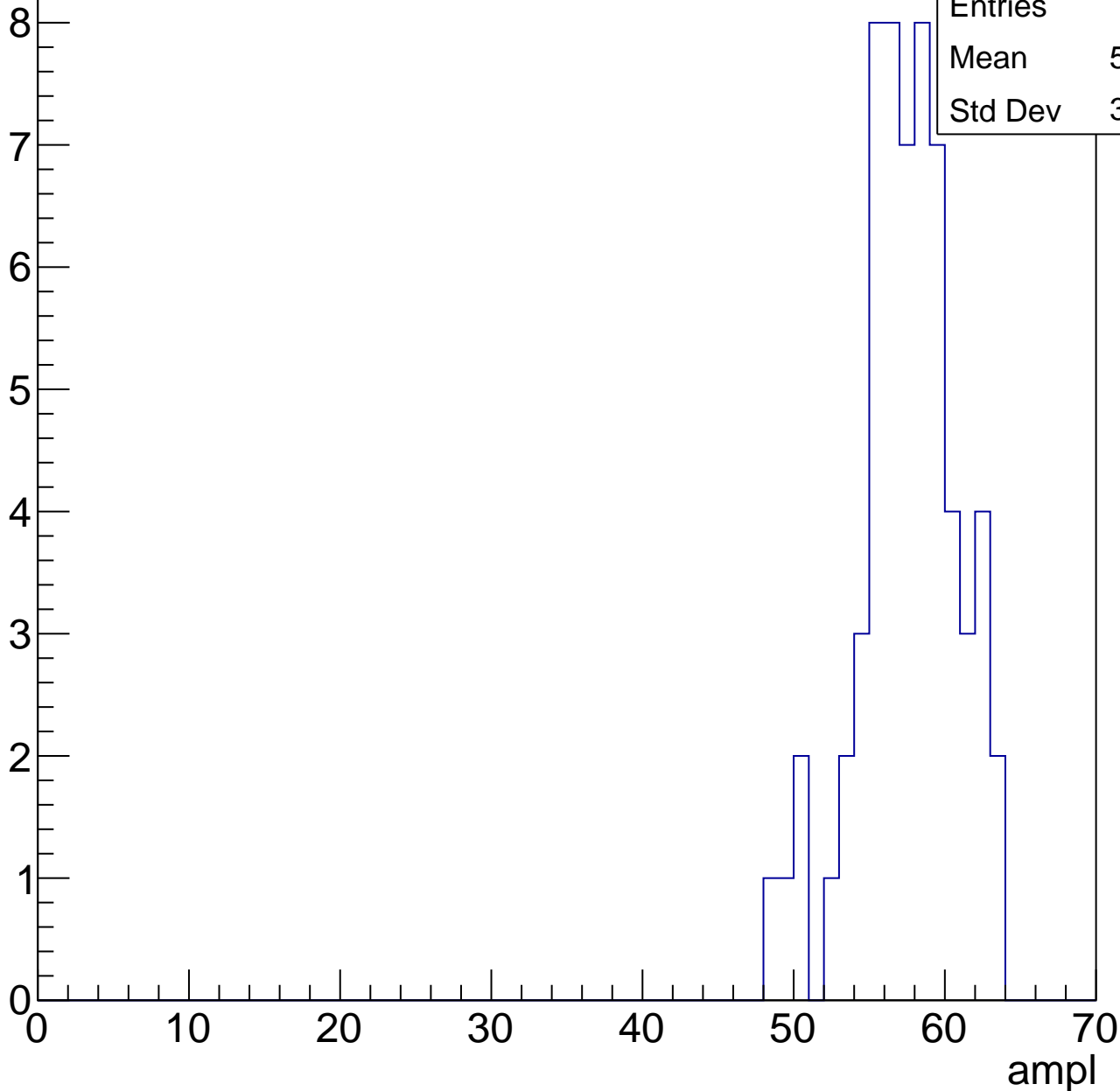


# B1L101S, U18-ch123, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	57.02
Std Dev	3.287

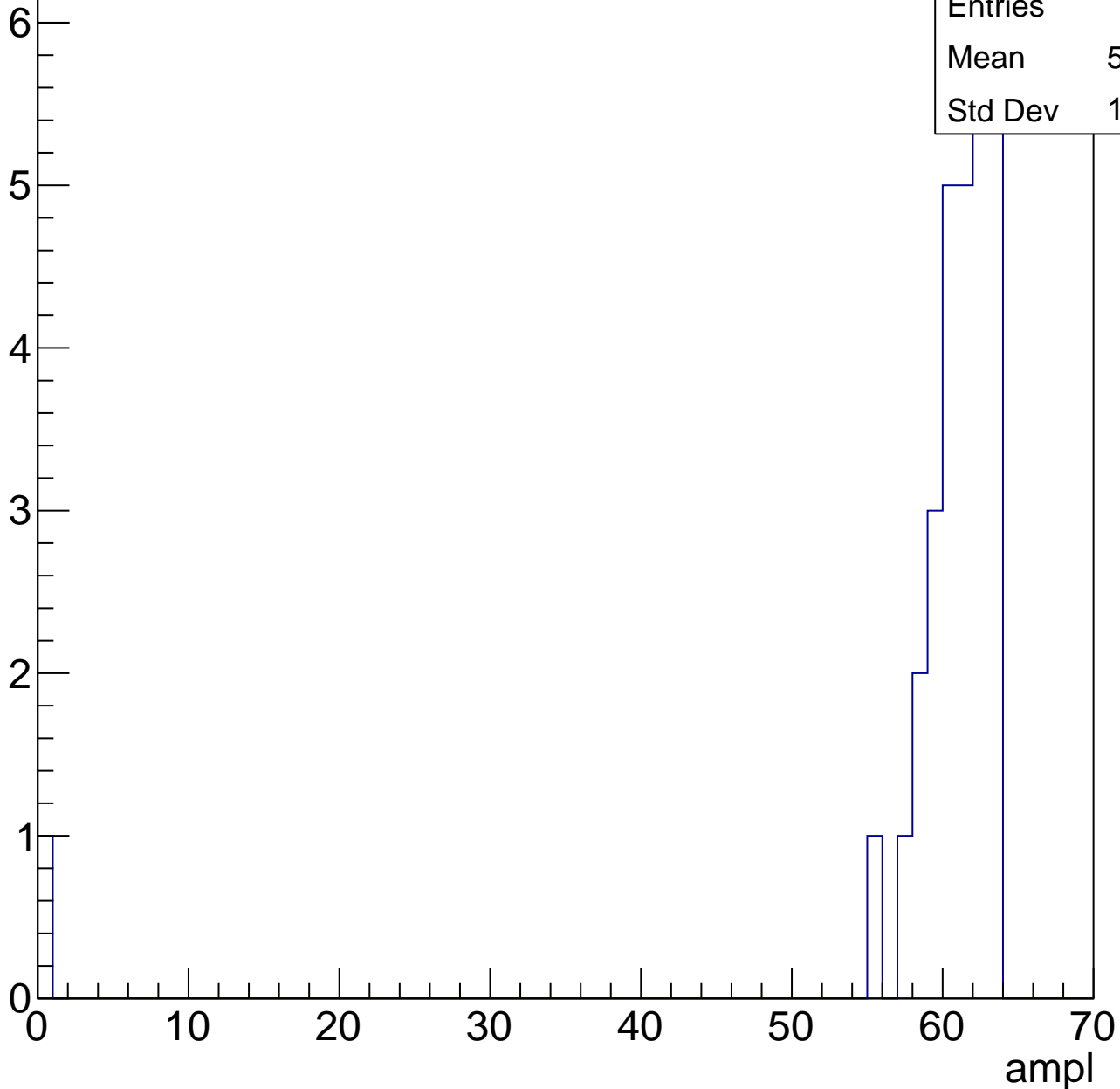


# B1L101S, U18-ch123, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

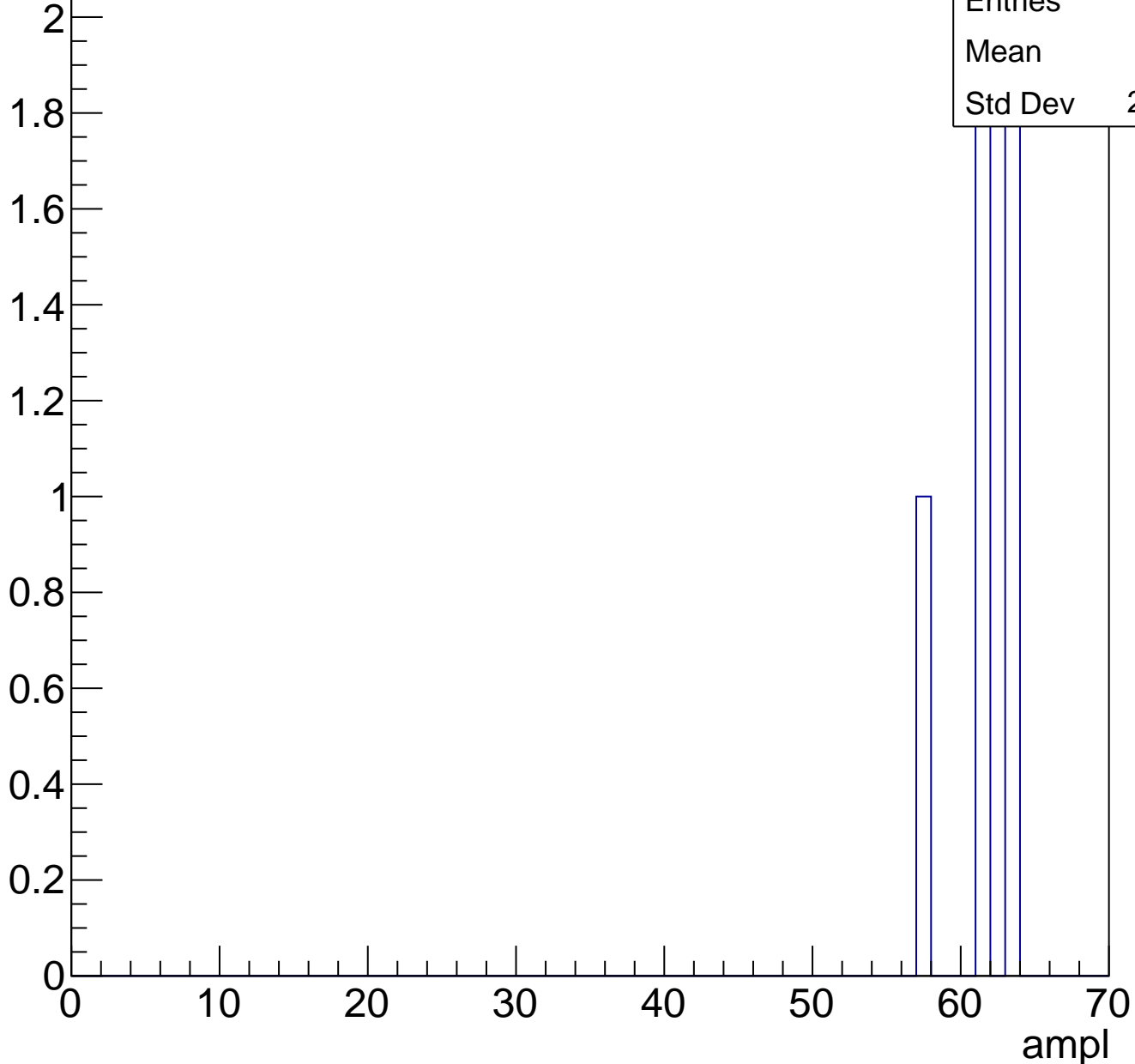
Entries	30
Mean	58.67
Std Dev	11.07



# B1L101S, U18-ch123, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

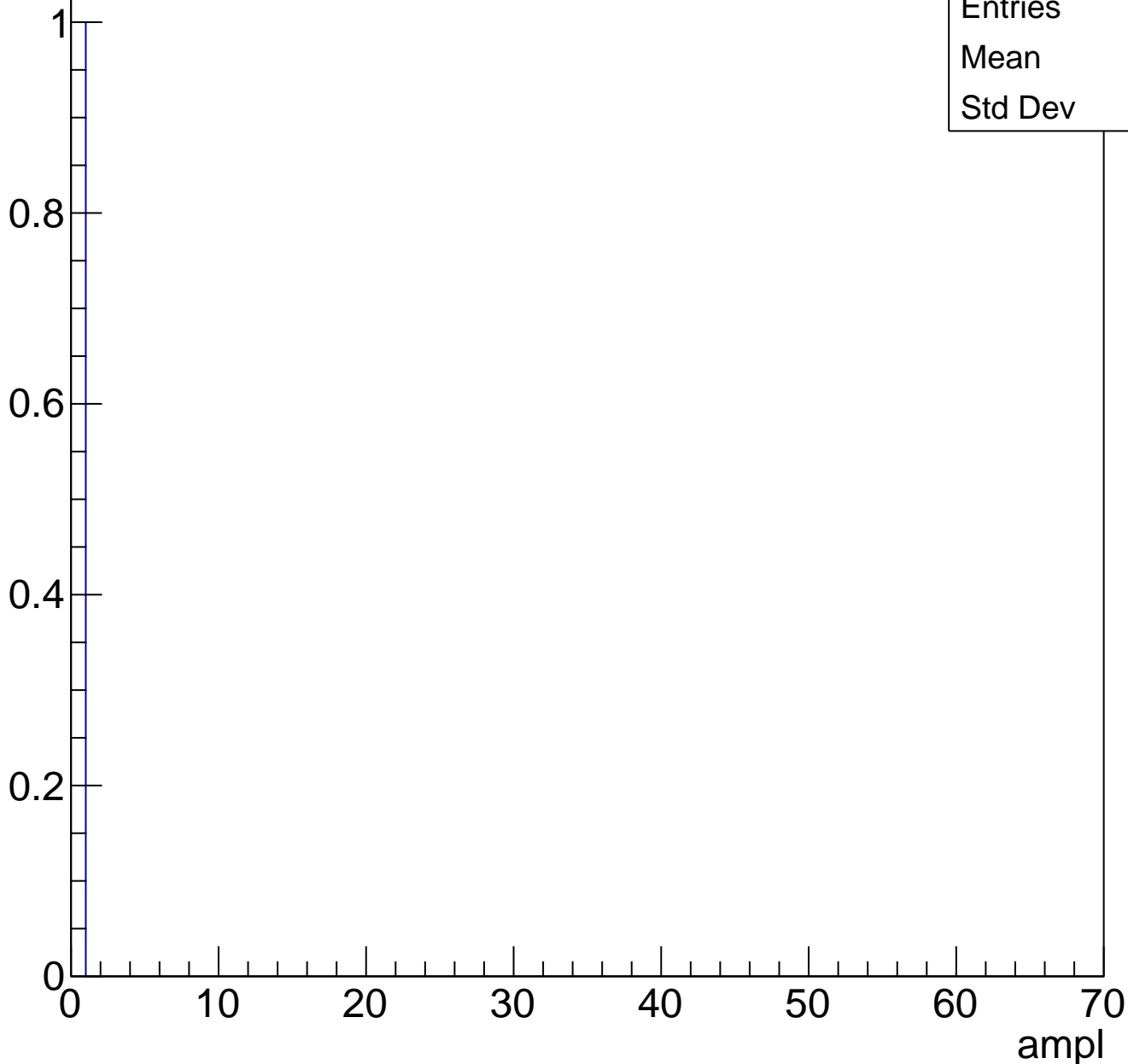




# B1L101S, U18-ch123, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch124, adc0

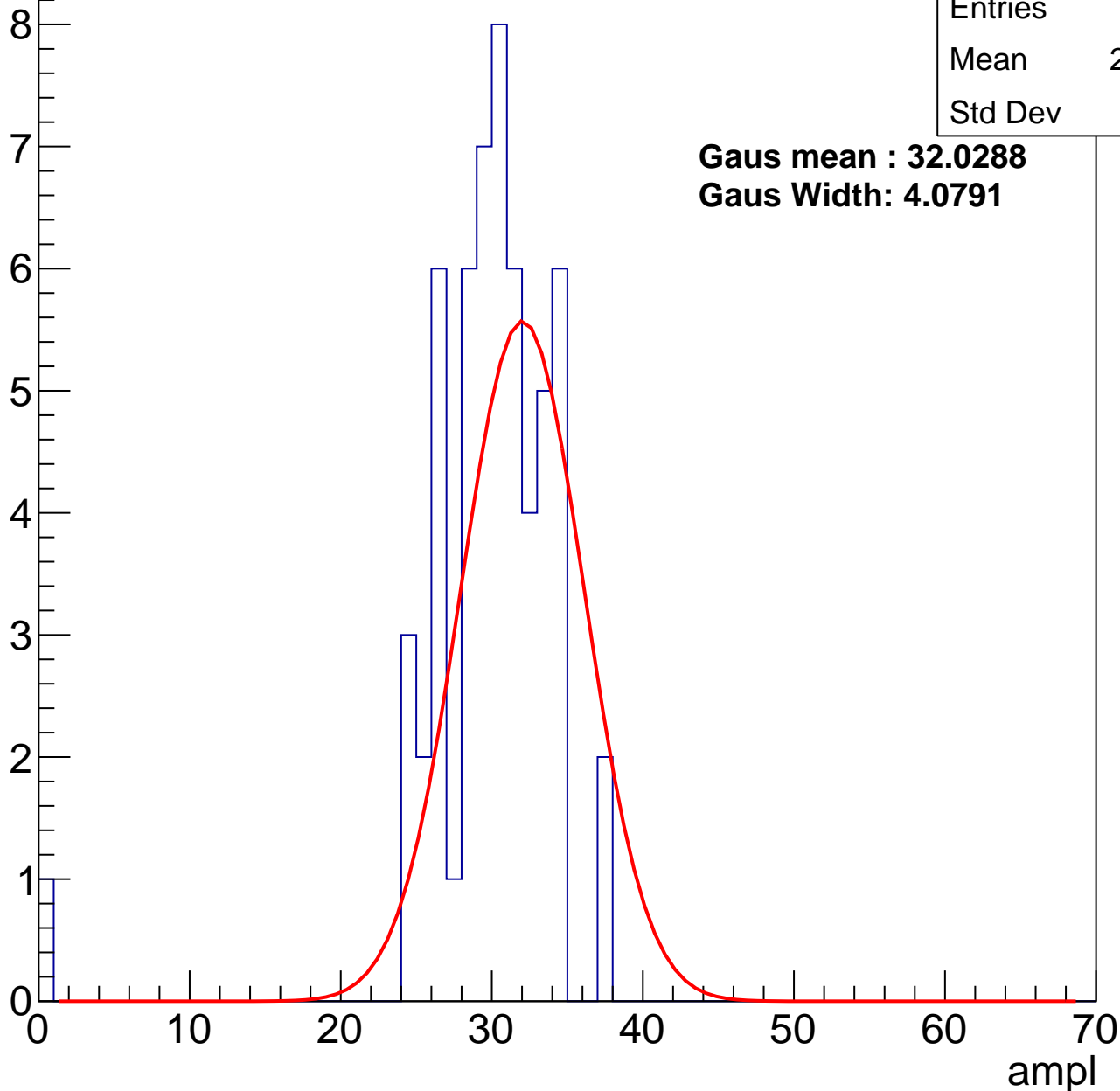
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	29.35
Std Dev	5.01

**Gaus mean : 32.0288**

**Gaus Width: 4.0791**



# B1L101S, U18-ch124, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	93
Mean	37.43
Std Dev	3.952

**Gaus mean : 38.2261**

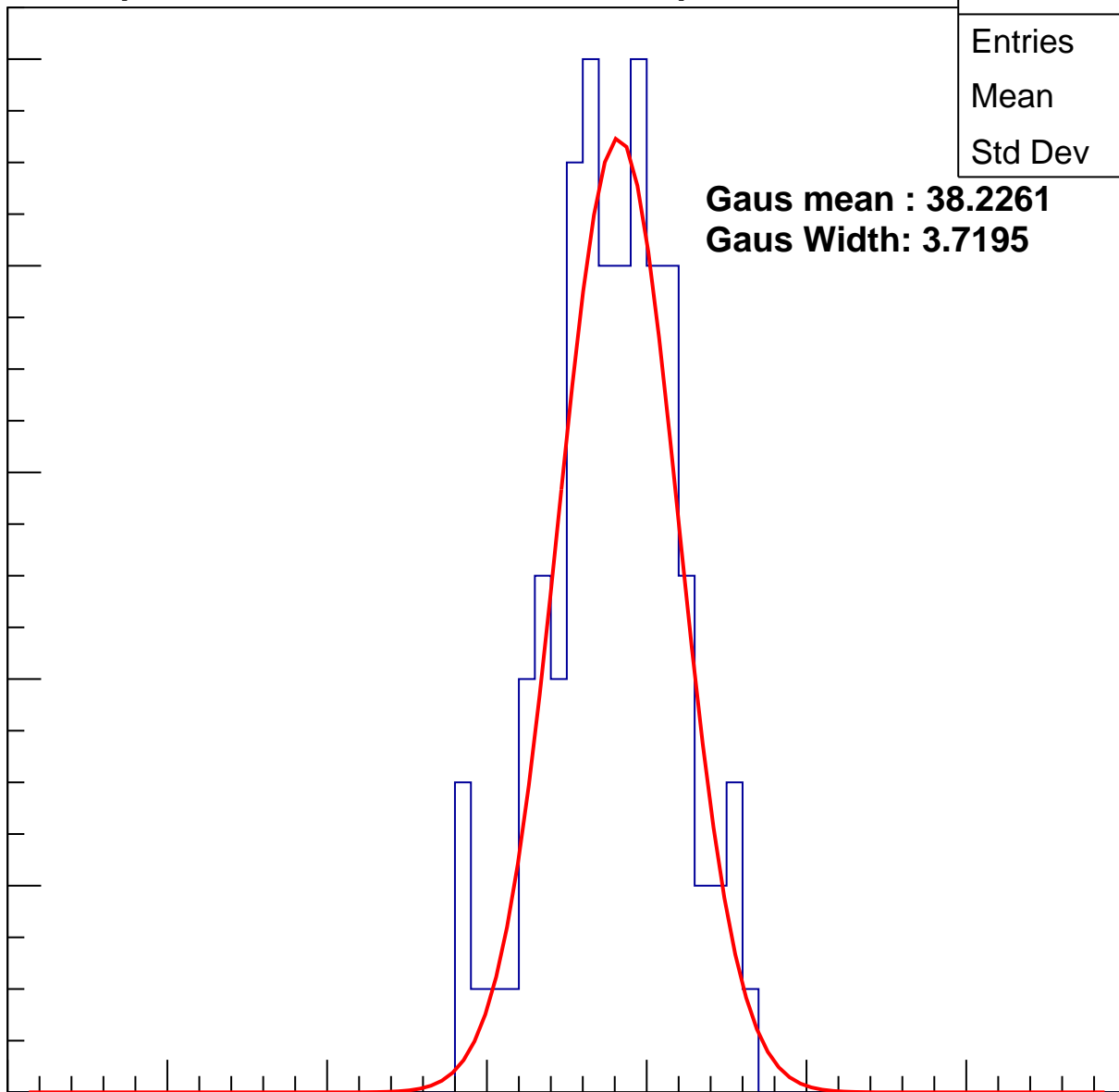
**Gaus Width: 3.7195**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L101S, U18-ch124, adc2

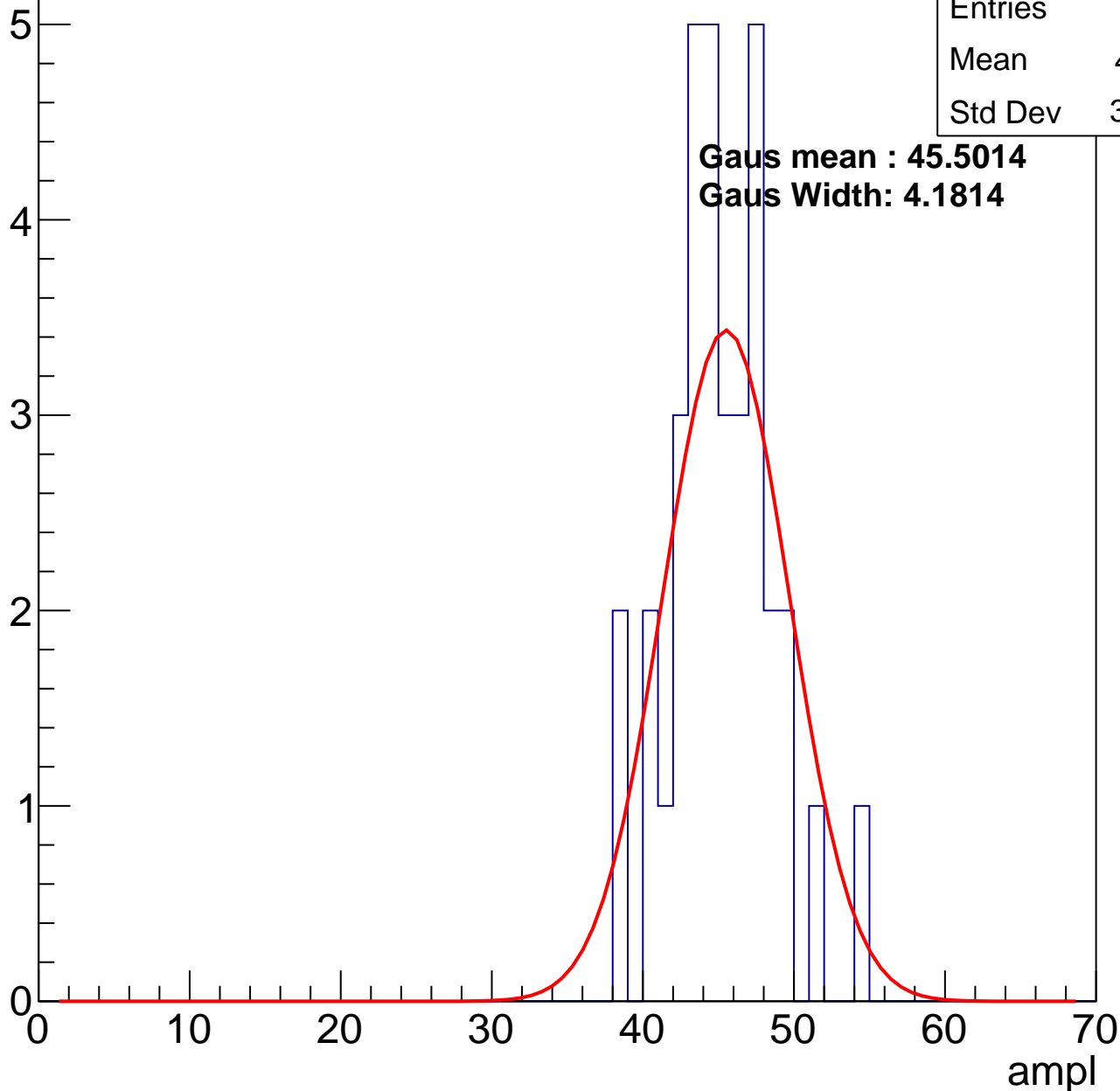
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	35
Mean	44.71
Std Dev	3.394

**Gaus mean : 45.5014**

**Gaus Width: 4.1814**

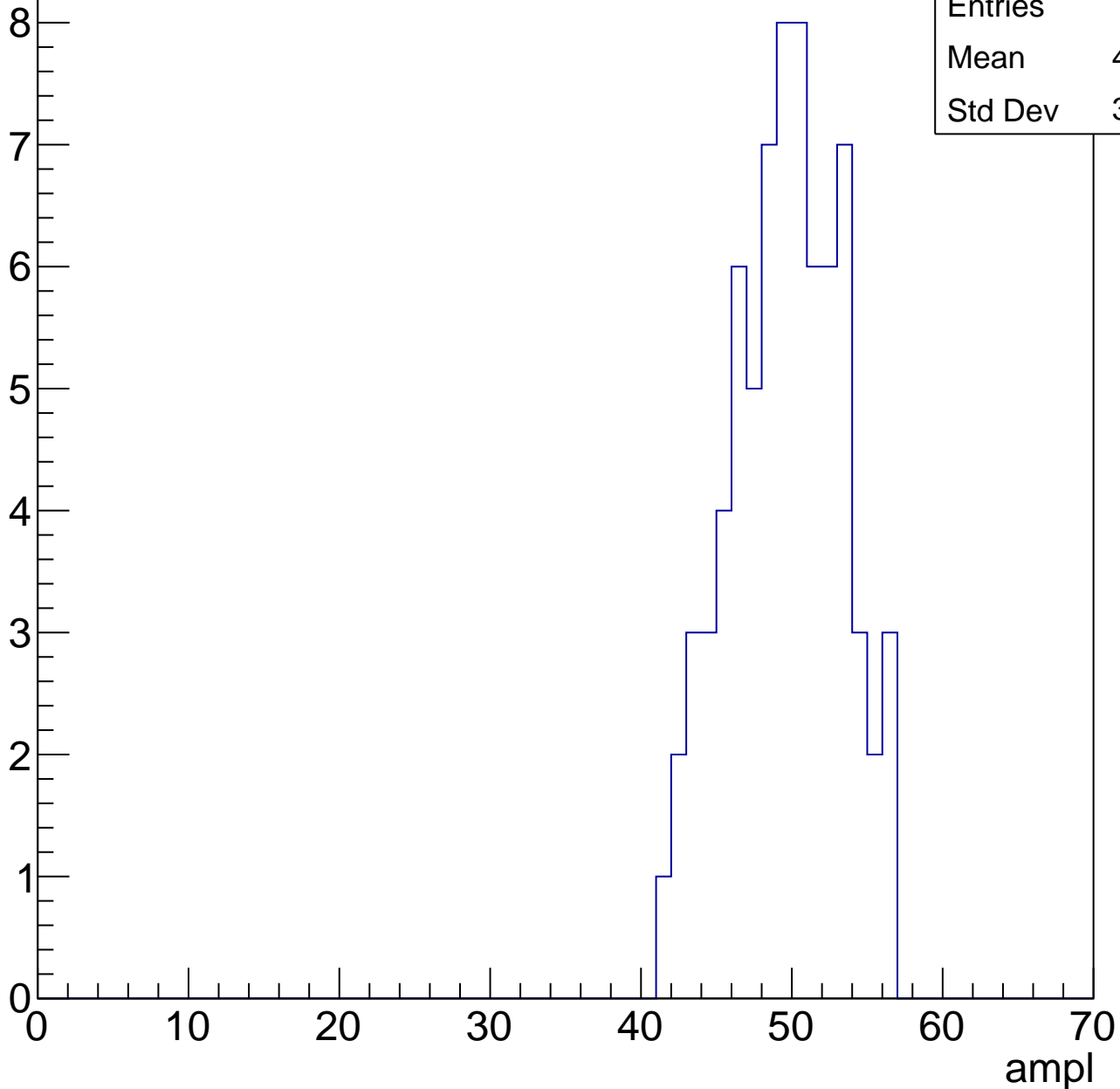


# B1L101S, U18-ch124, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	49.11
Std Dev	3.641

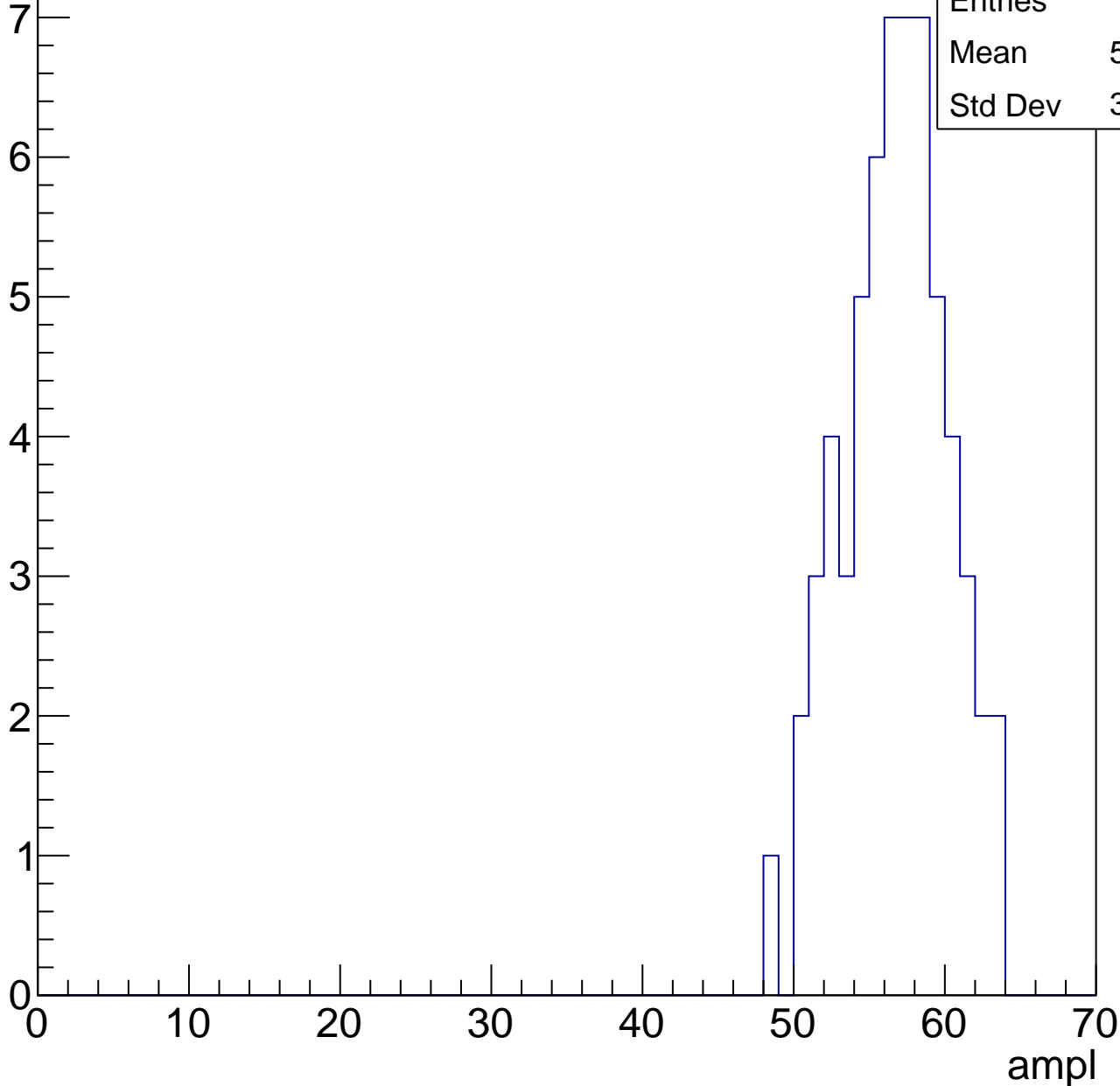


# B1L101S, U18-ch124, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	56.28
Std Dev	3.417

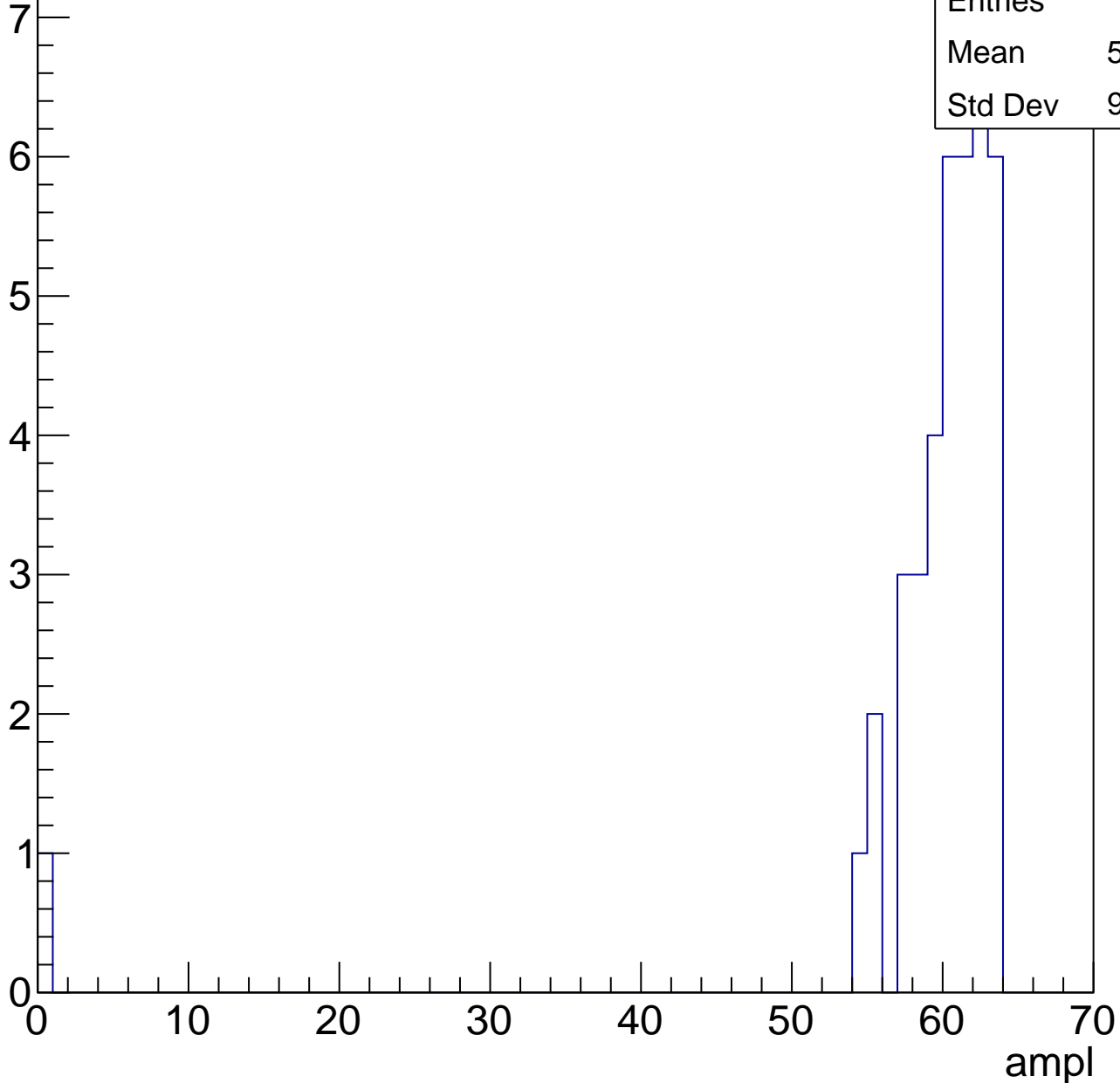


# B1L101S, U18-ch124, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	39
Mean	58.54
Std Dev	9.784



# B1L101S, U18-ch124, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

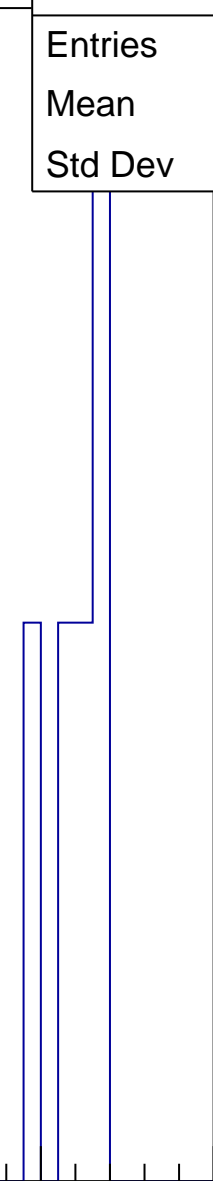
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	61.6
Std Dev	1.497

0 10 20 30 40 50 60 70

ampl





# B1L101S, U18-ch124, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U18-ch125, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	64
Mean	29.44
Std Dev	2.999

**Gaus mean : 30.0653**

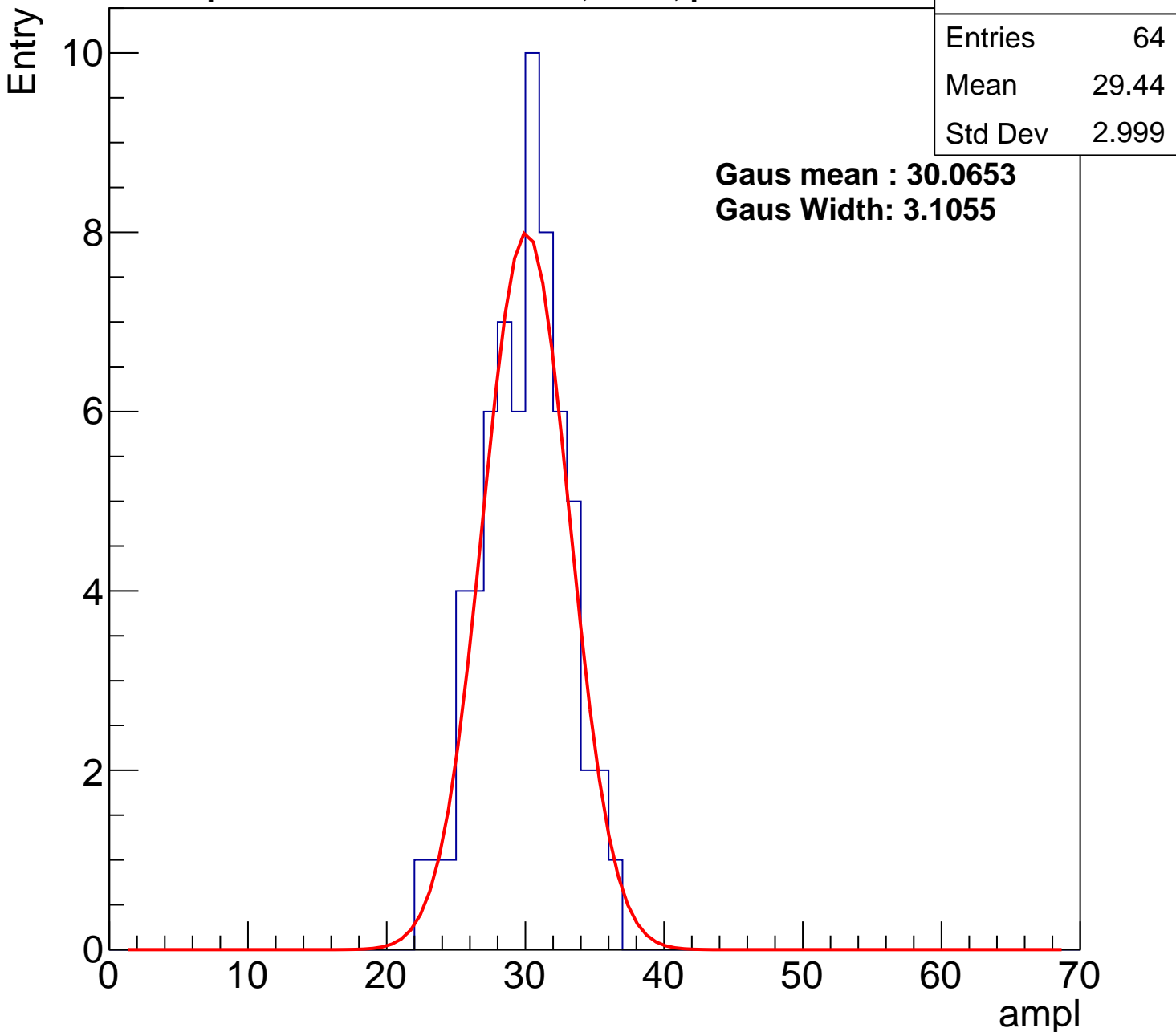
**Gaus Width: 3.1055**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U18-ch125, adc1

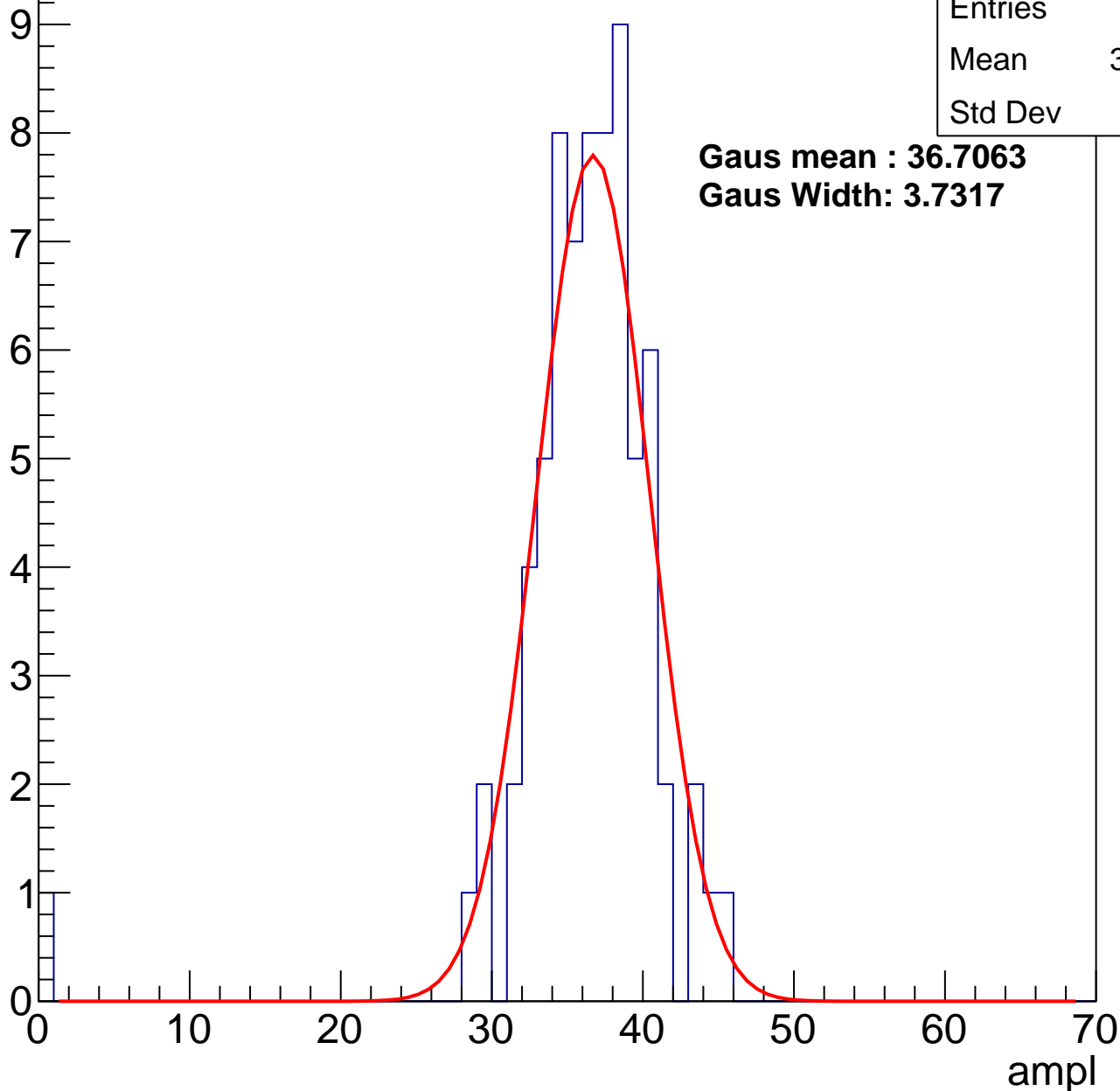
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	35.78
Std Dev	5.44

**Gaus mean : 36.7063**

**Gaus Width: 3.7317**



# B1L101S, U18-ch125, adc2

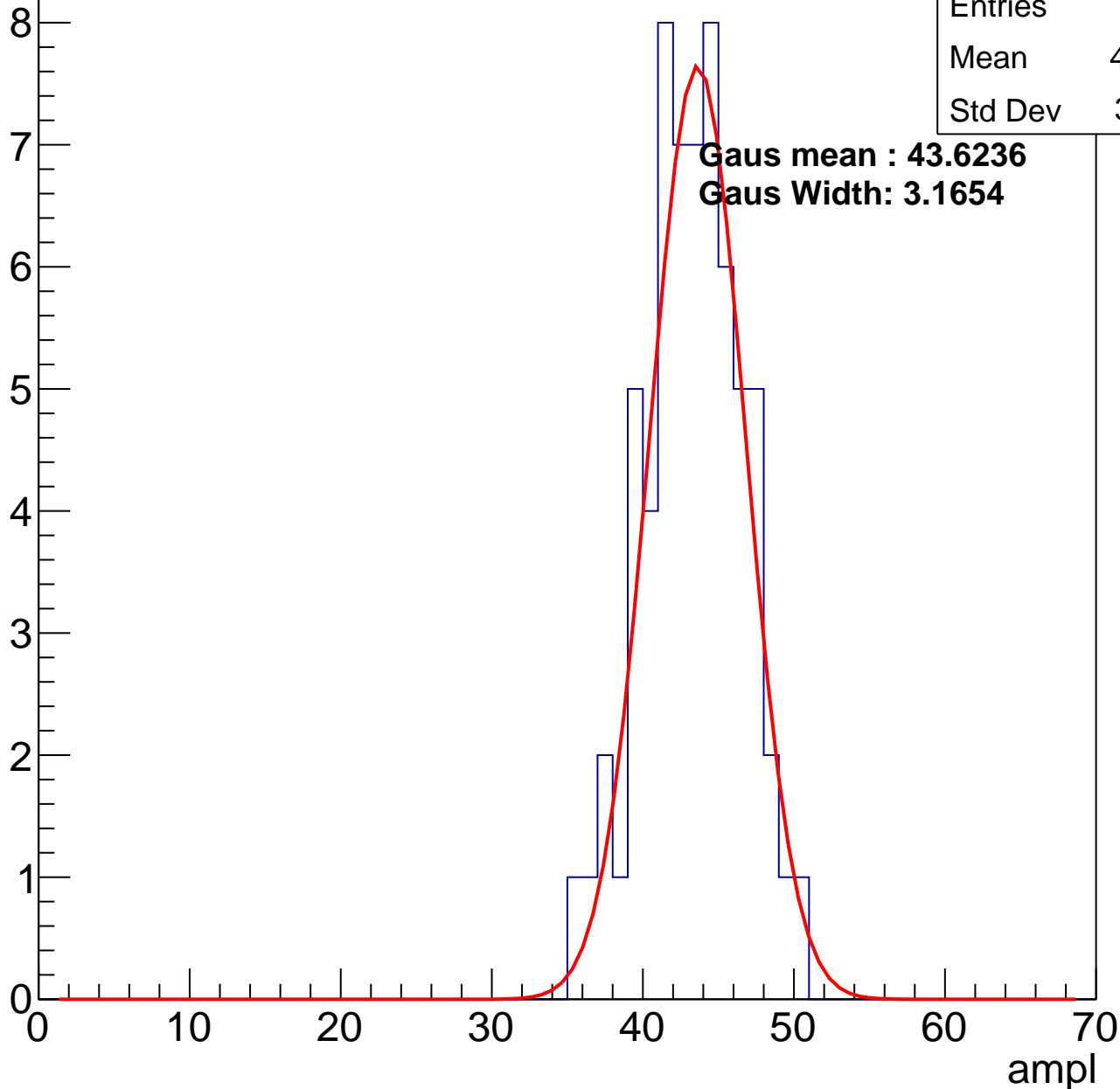
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	42.86
Std Dev	3.201

**Gaus mean : 43.6236**

**Gaus Width: 3.1654**

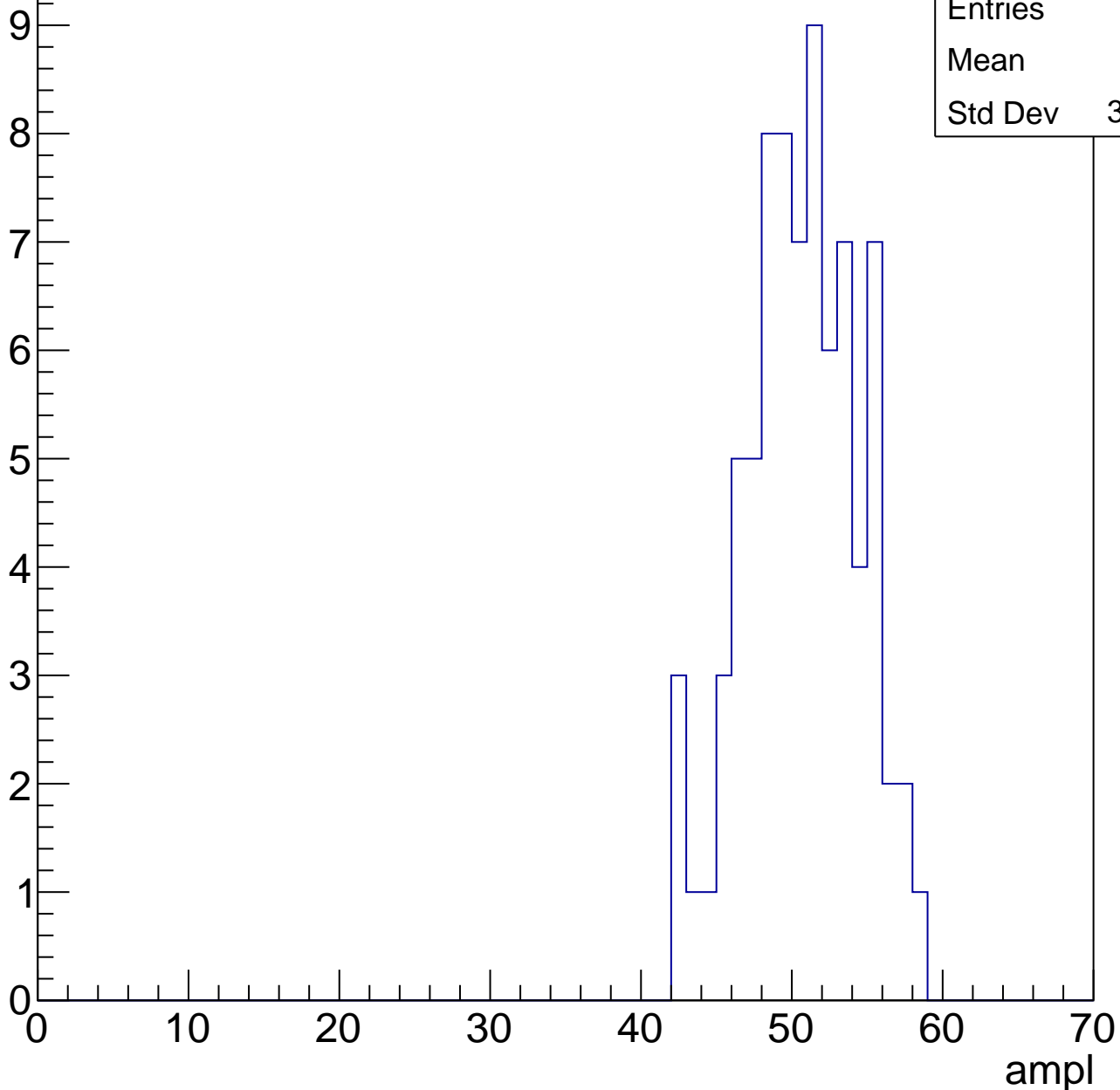


# B1L101S, U18-ch125, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	79
Mean	50.2
Std Dev	3.702

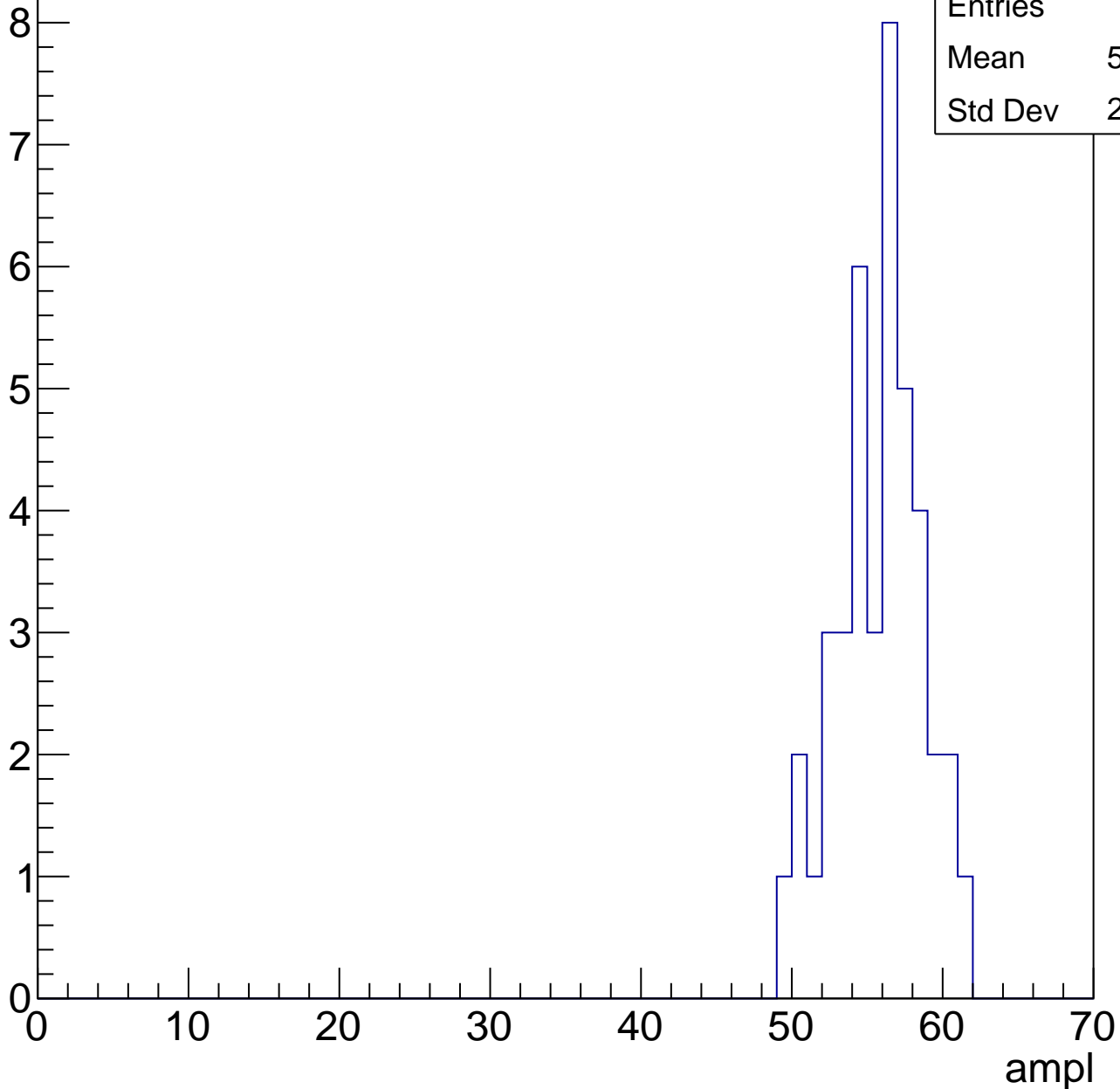


# B1L101S, U18-ch125, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	41
Mean	55.32
Std Dev	2.815



# B1L101S, U18-ch125, adc5

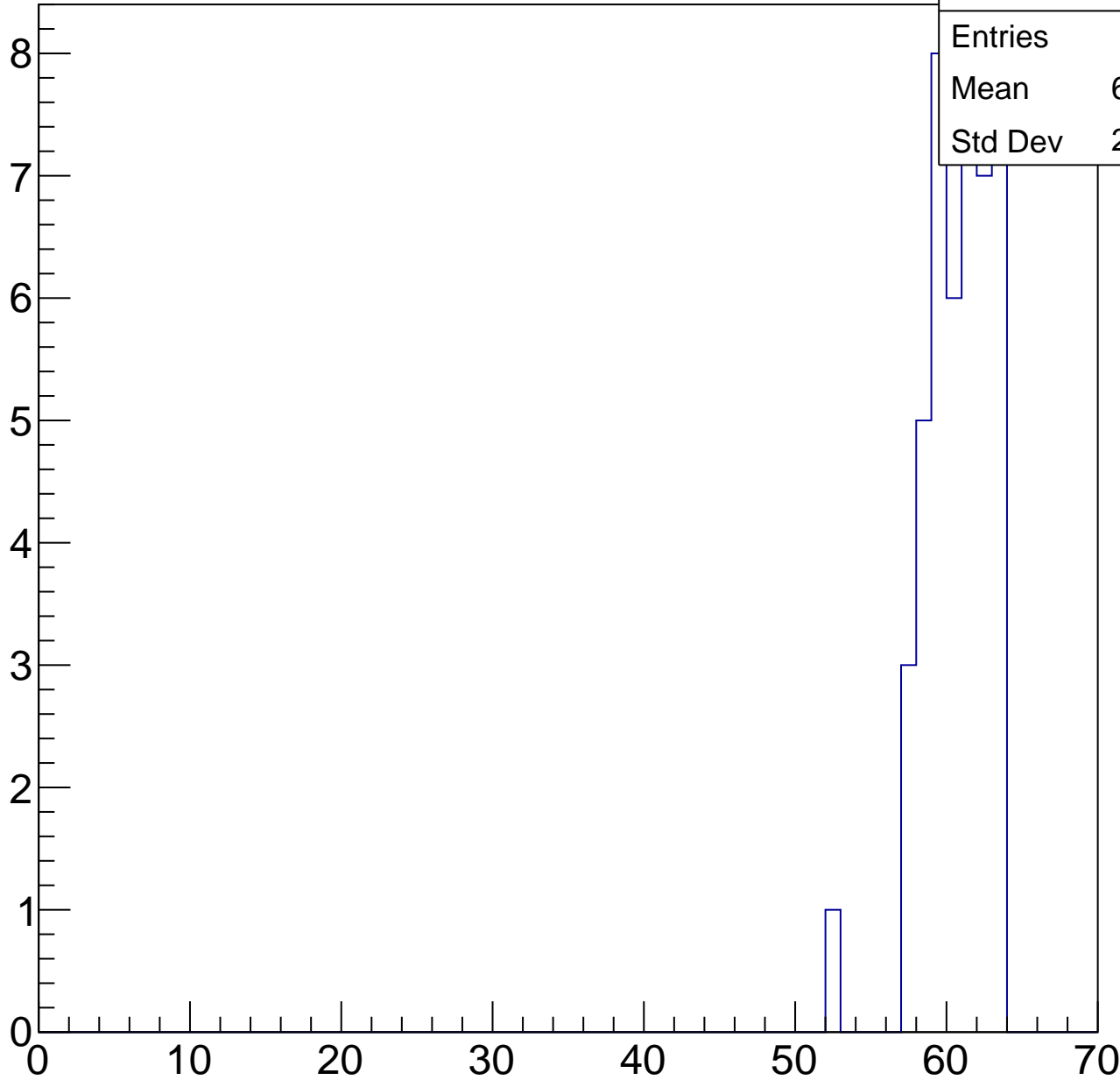
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	46
Mean	60.24
Std Dev	2.209

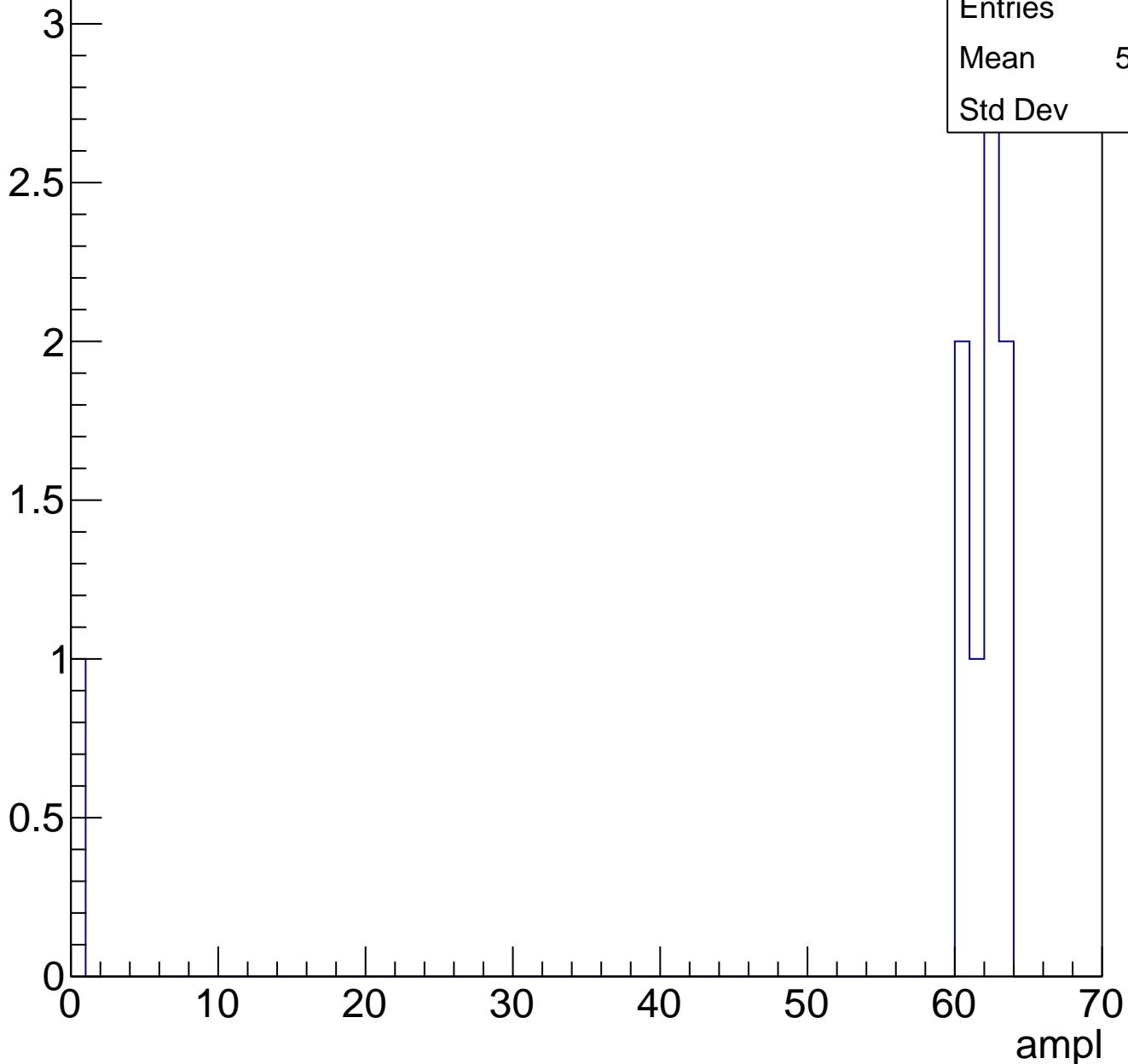
ampl



# B1L101S, U18-ch125, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	9
Mean	54.78
Std Dev	19.4



# B1L101S, U18-ch125, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U18-ch126, adc0

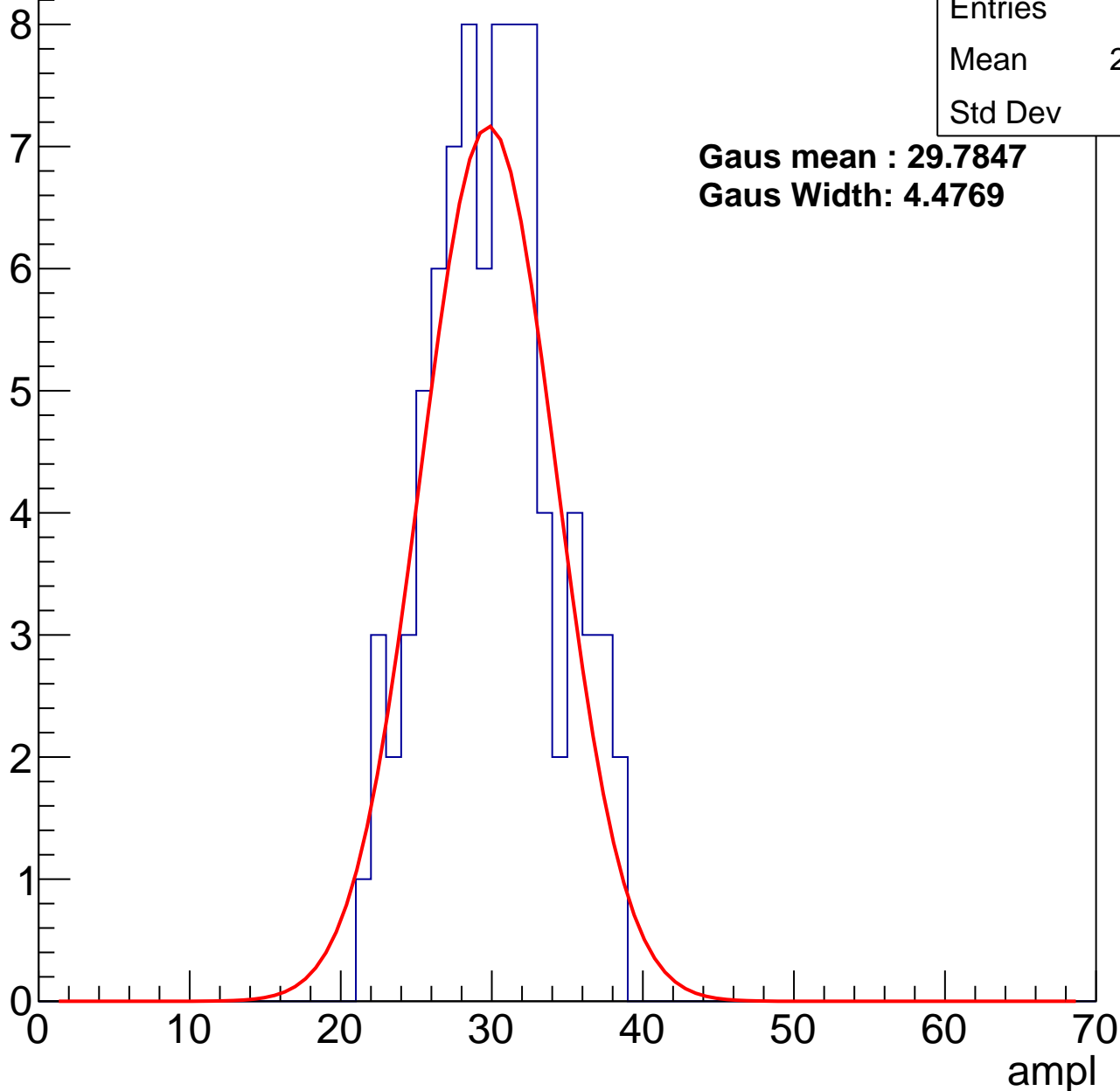
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	83
Mean	29.54
Std Dev	4.07

**Gaus mean : 29.7847**

**Gaus Width: 4.4769**



# B1L101S, U18-ch126, adc1

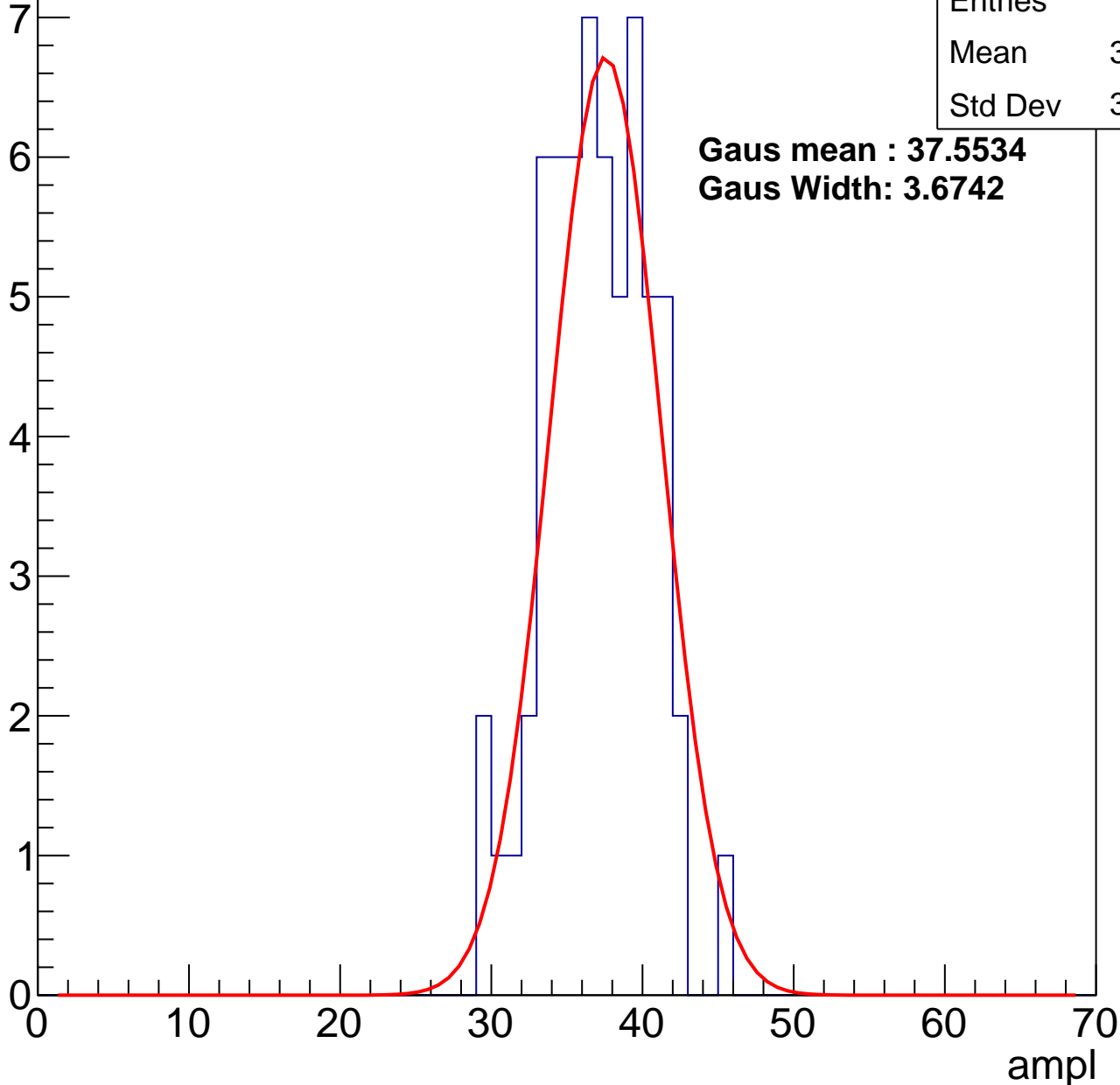
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	36.55
Std Dev	3.368

**Gaus mean : 37.5534**

**Gaus Width: 3.6742**



# B1L101S, U18-ch126, adc2

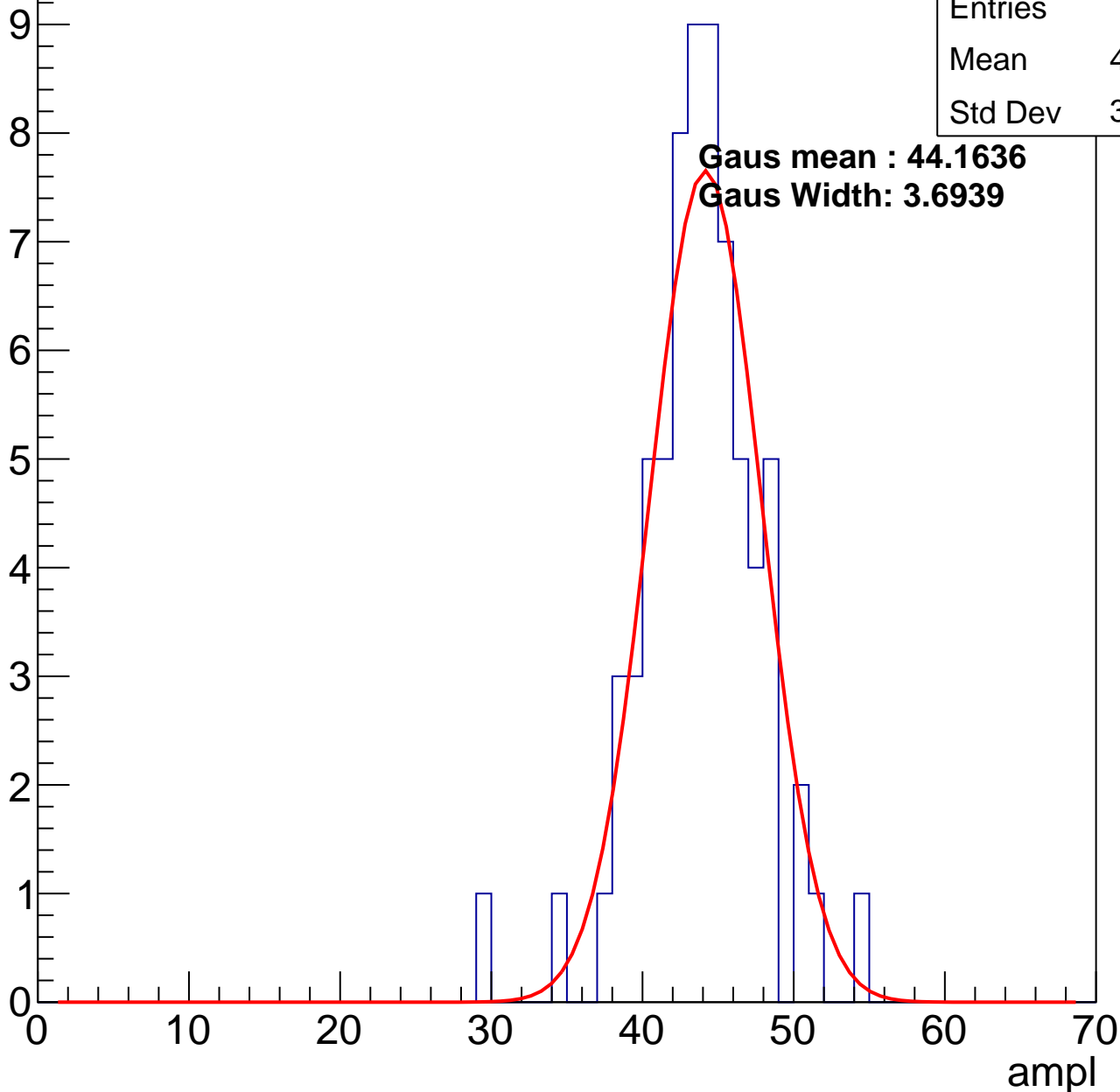
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	43.33
Std Dev	3.883

**Gaus mean : 44.1636**

**Gaus Width: 3.6939**

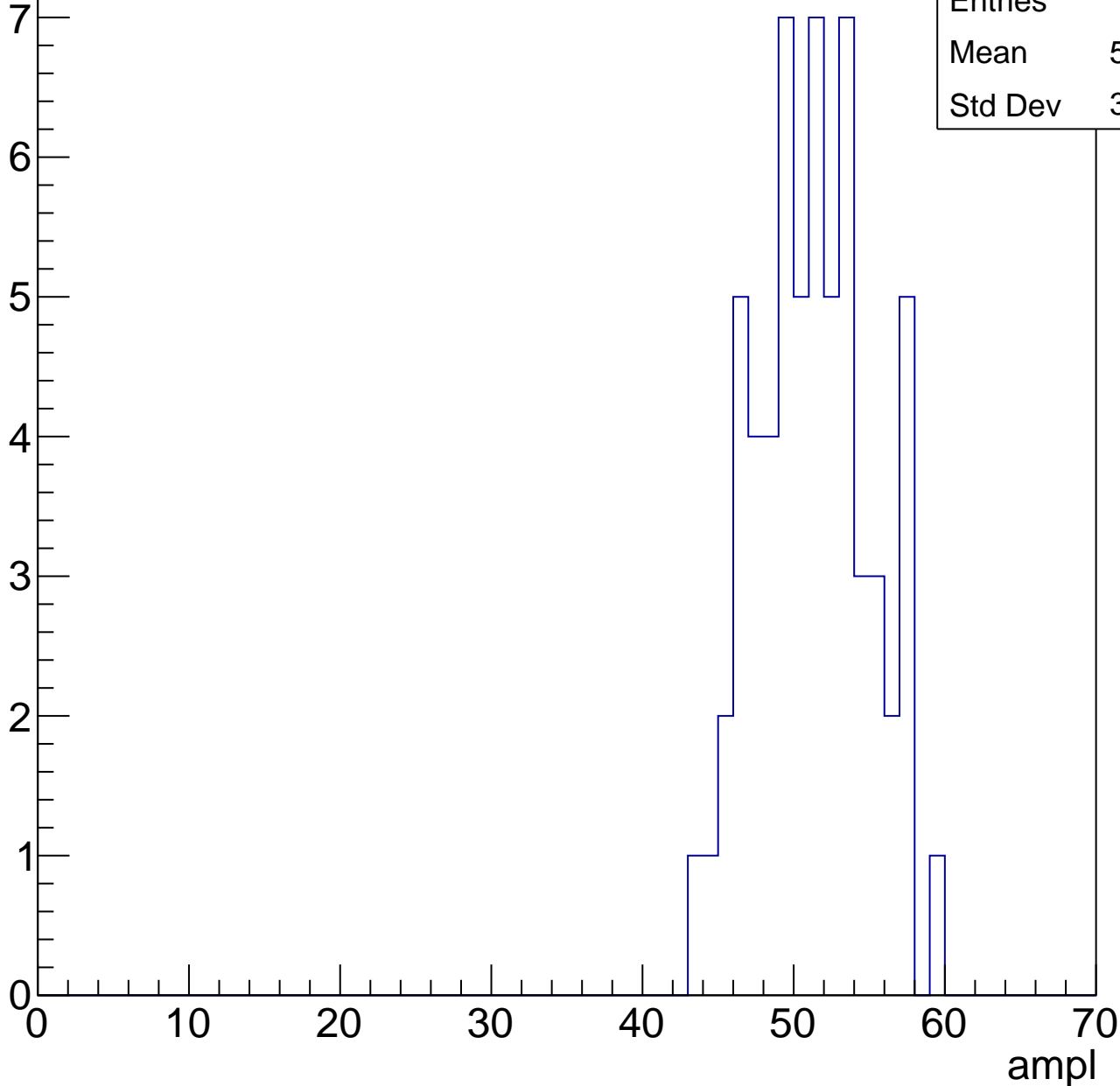


# B1L101S, U18-ch126, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

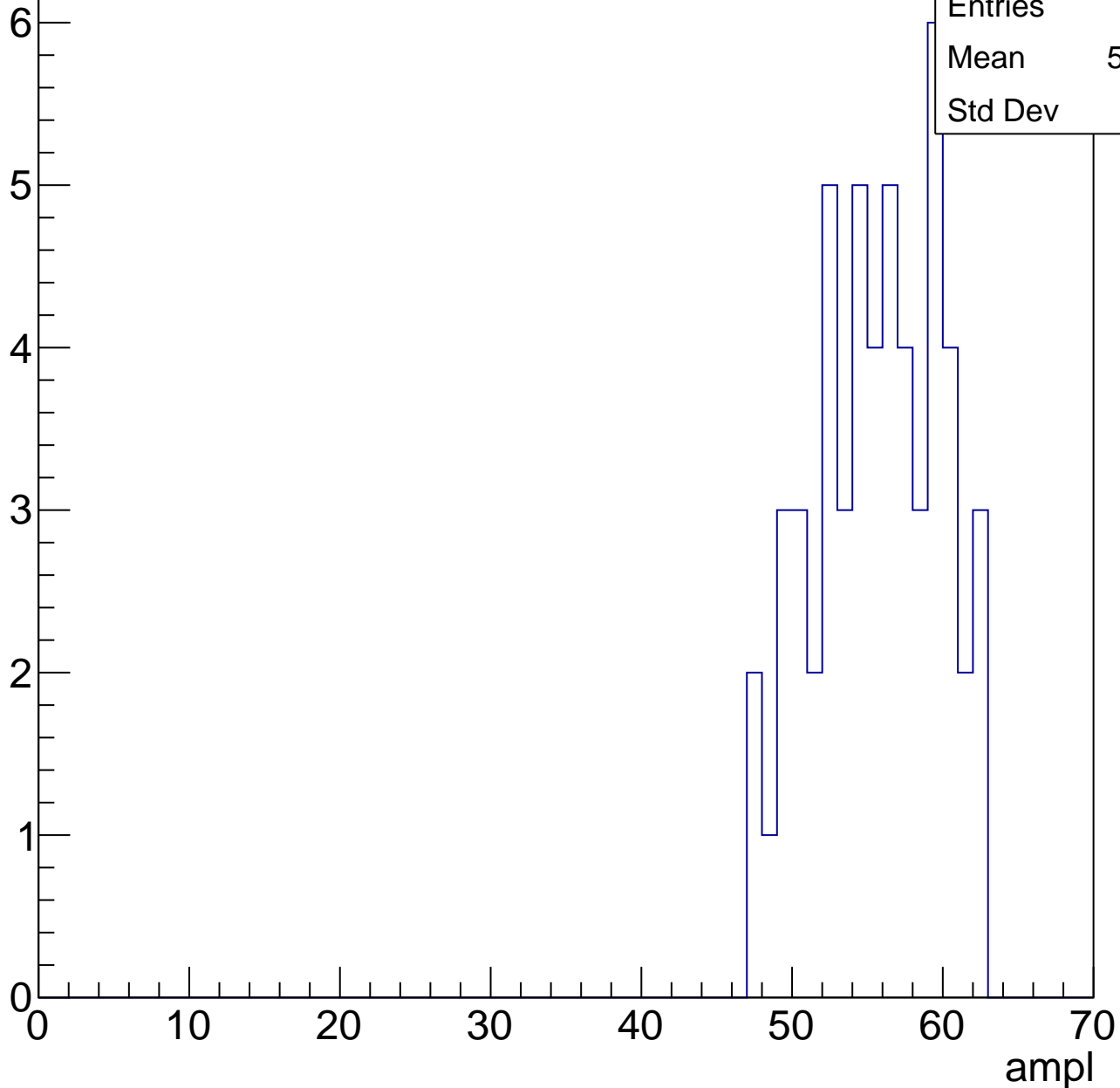
Entries	62
Mean	50.82
Std Dev	3.687



# B1L101S, U18-ch126, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

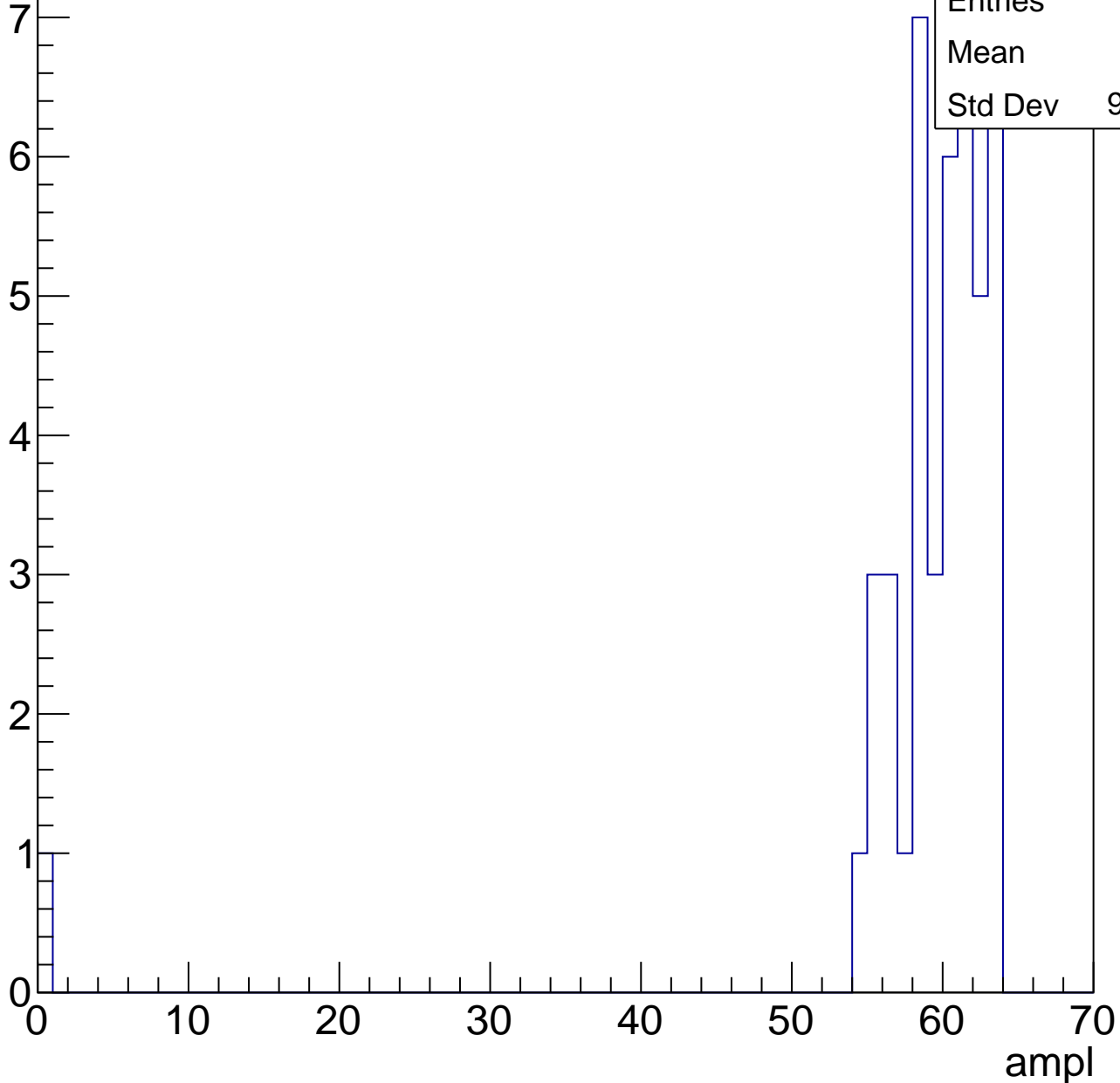


# B1L101S, U18-ch126, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

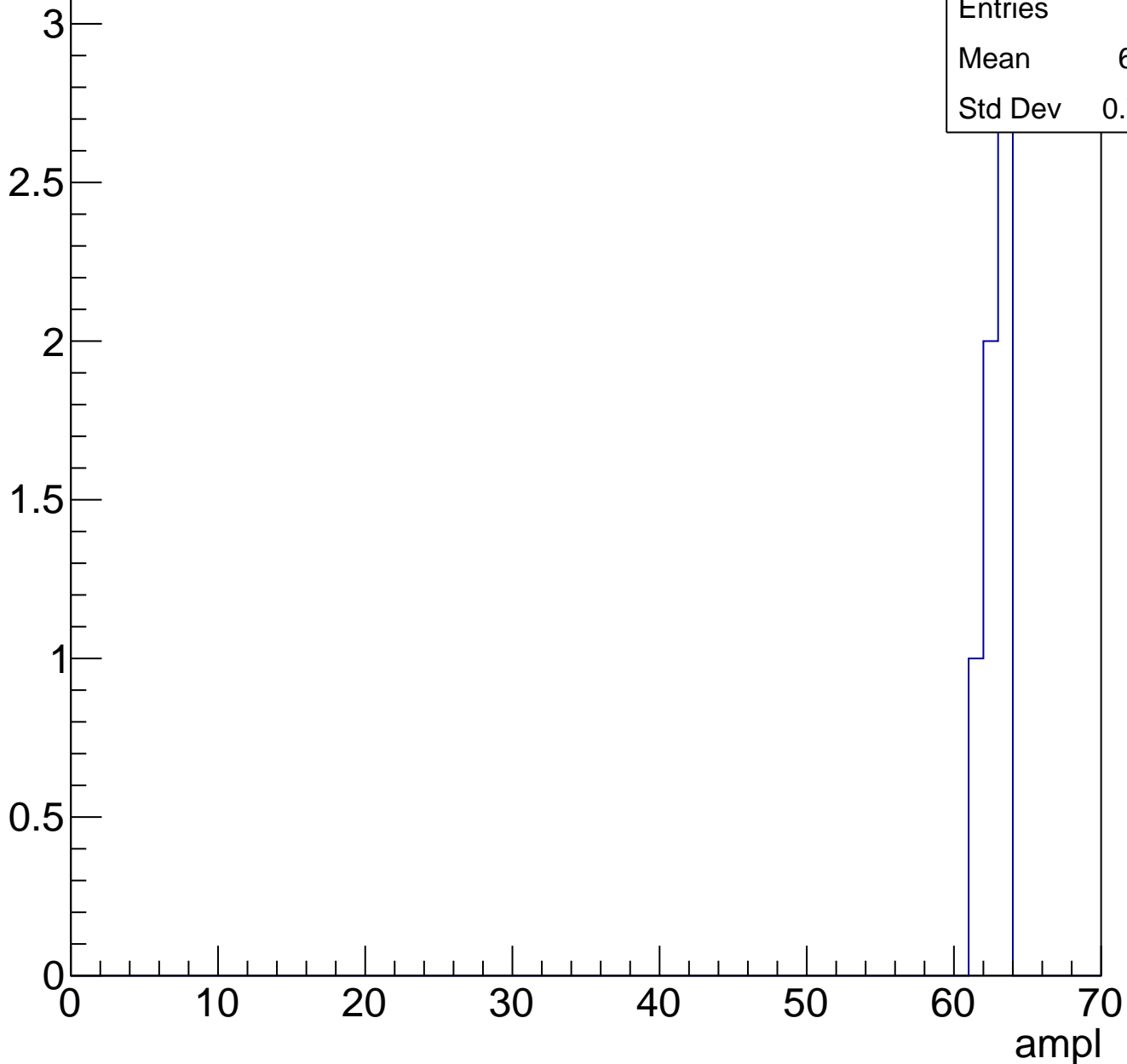
Entries	44
Mean	58.3
Std Dev	9.246



# B1L101S, U18-ch126, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U18-ch126, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U18-ch127, adc0

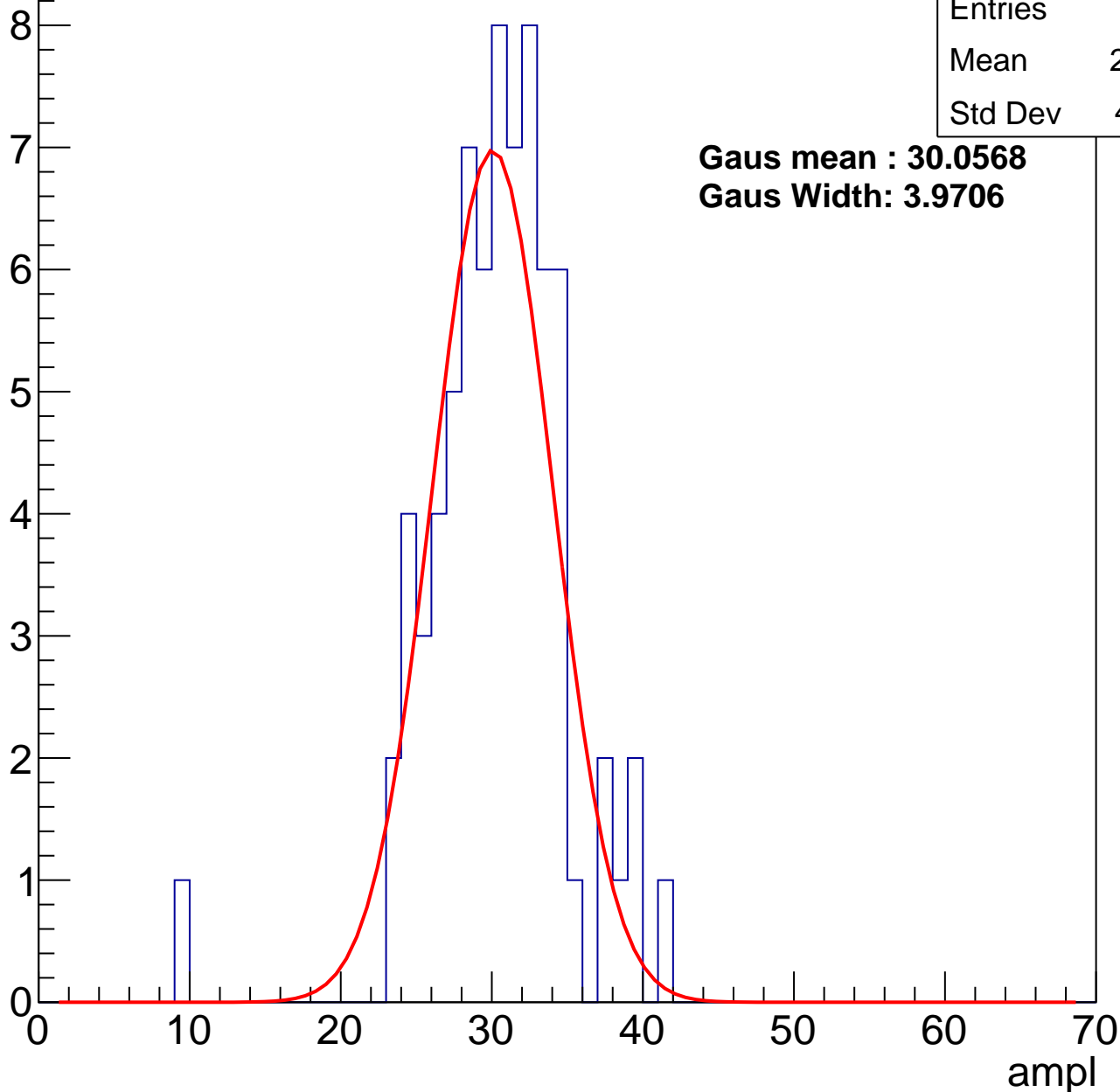
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	29.95
Std Dev	4.591

**Gaus mean : 30.0568**

**Gaus Width: 3.9706**



# B1L101S, U18-ch127, adc1

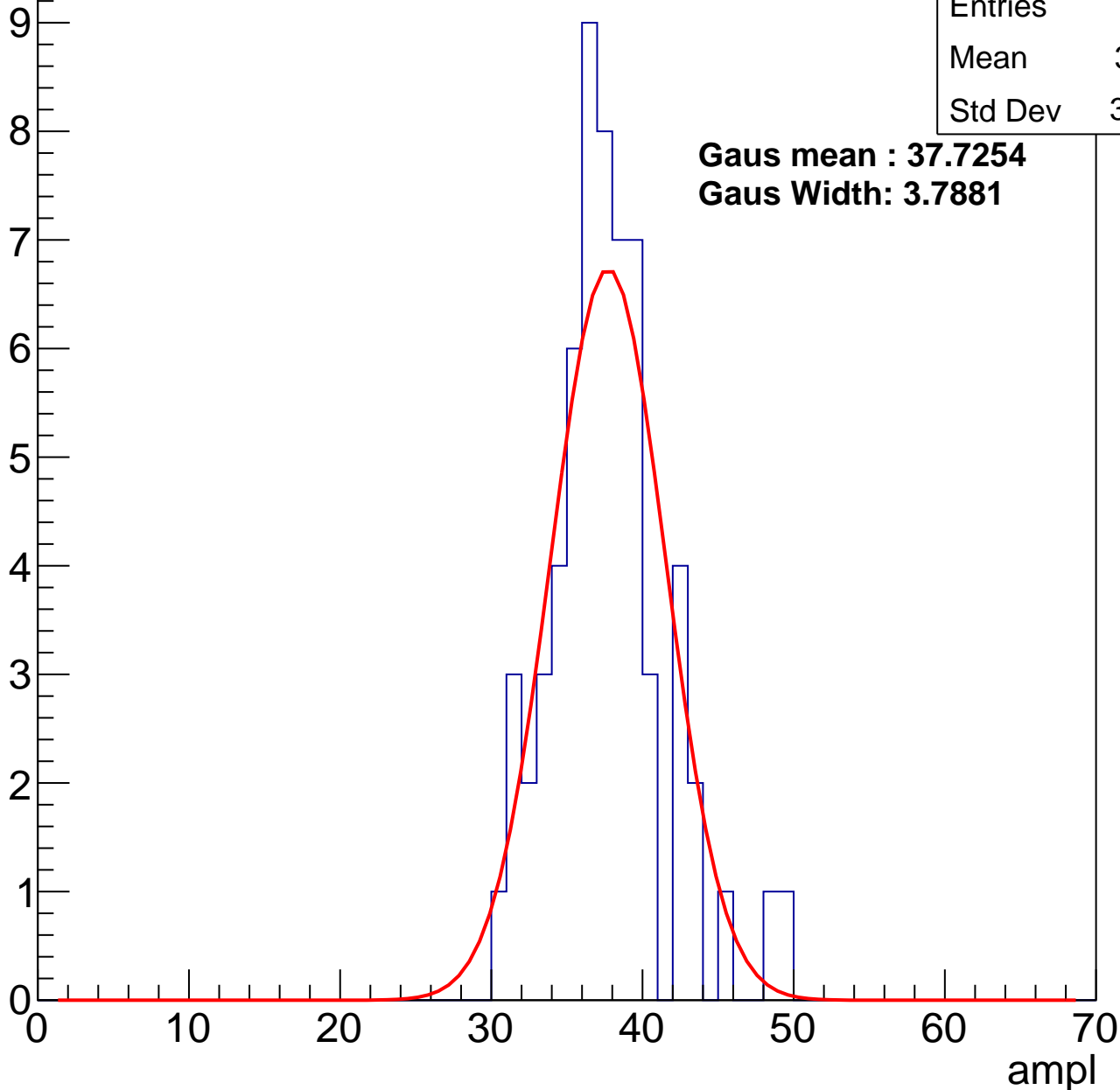
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	37.21
Std Dev	3.777

**Gaus mean : 37.7254**

**Gaus Width: 3.7881**



# B1L101S, U18-ch127, adc2

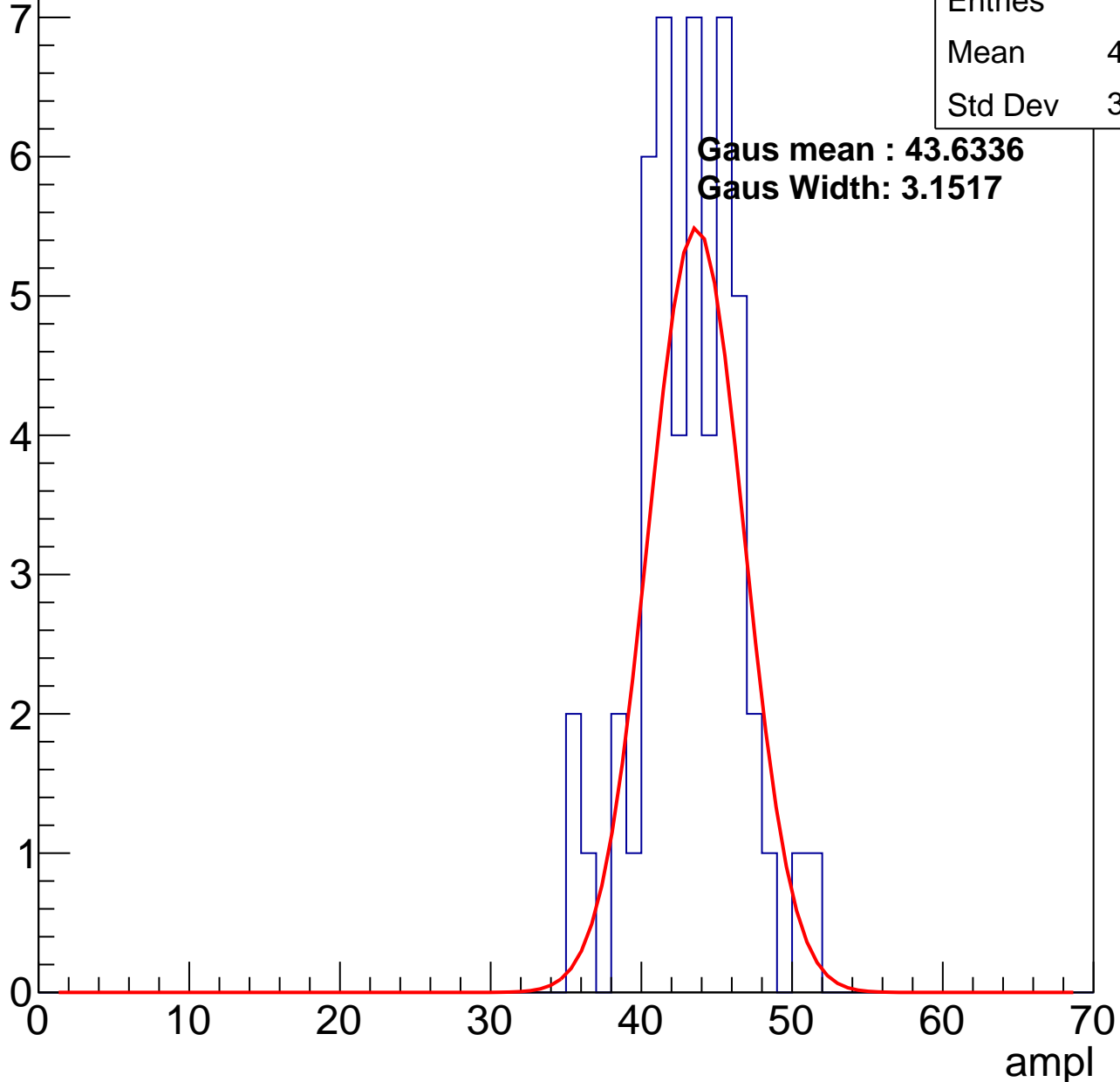
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	42.76
Std Dev	3.352

**Gaus mean : 43.6336**

**Gaus Width: 3.1517**

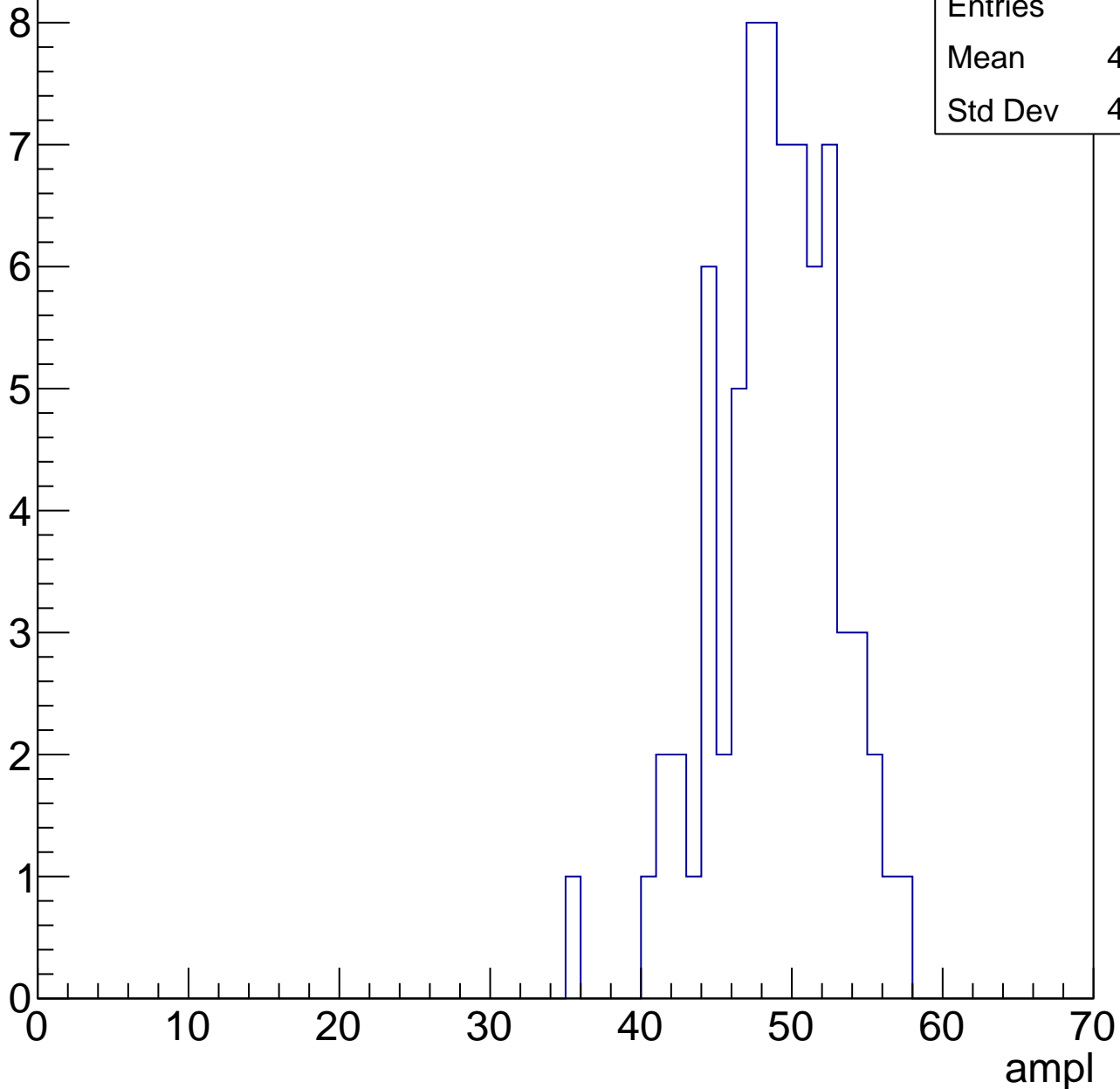


# B1L101S, U18-ch127, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	48.42
Std Dev	4.027

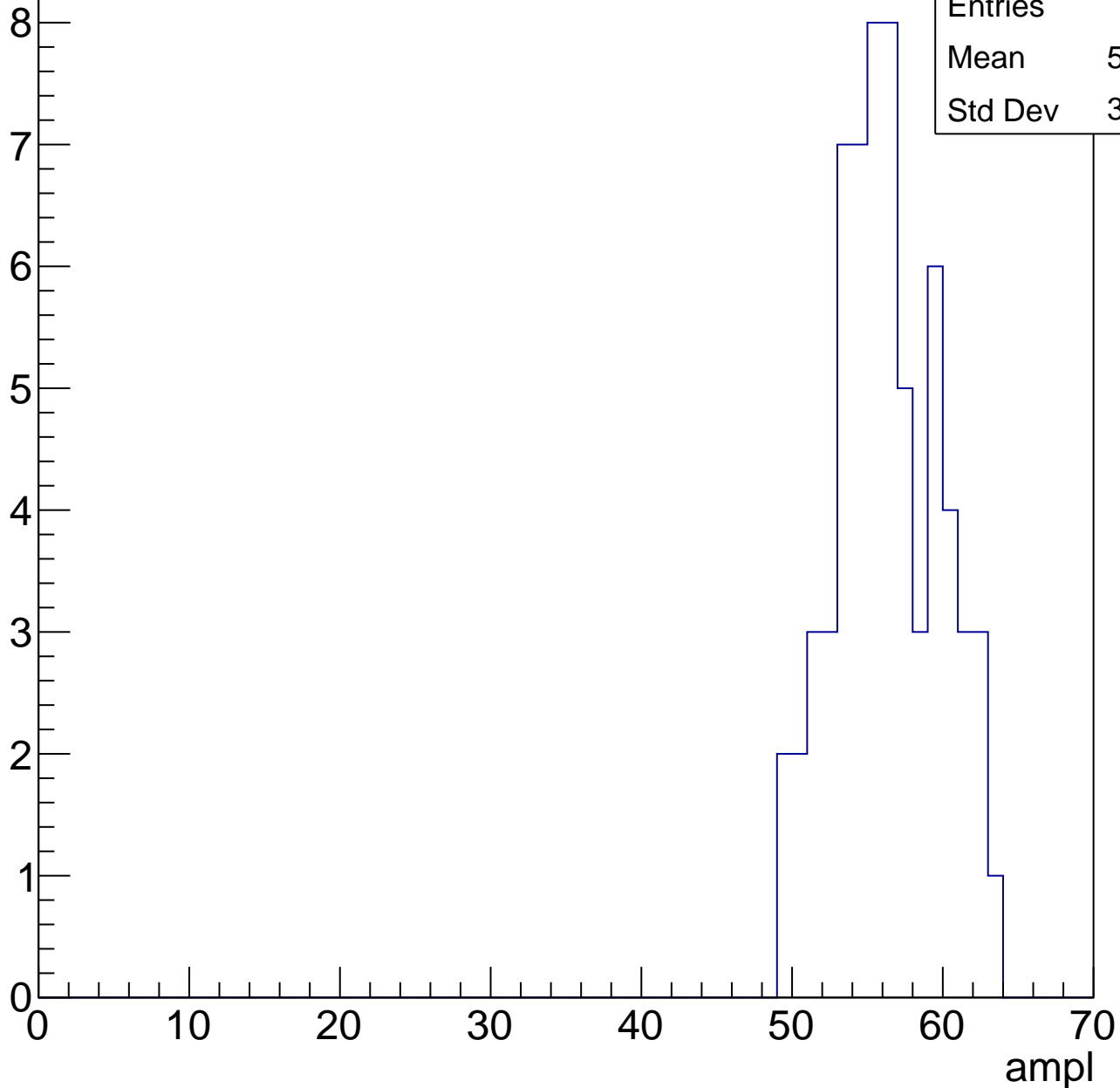


# B1L101S, U18-ch127, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	55.83
Std Dev	3.413

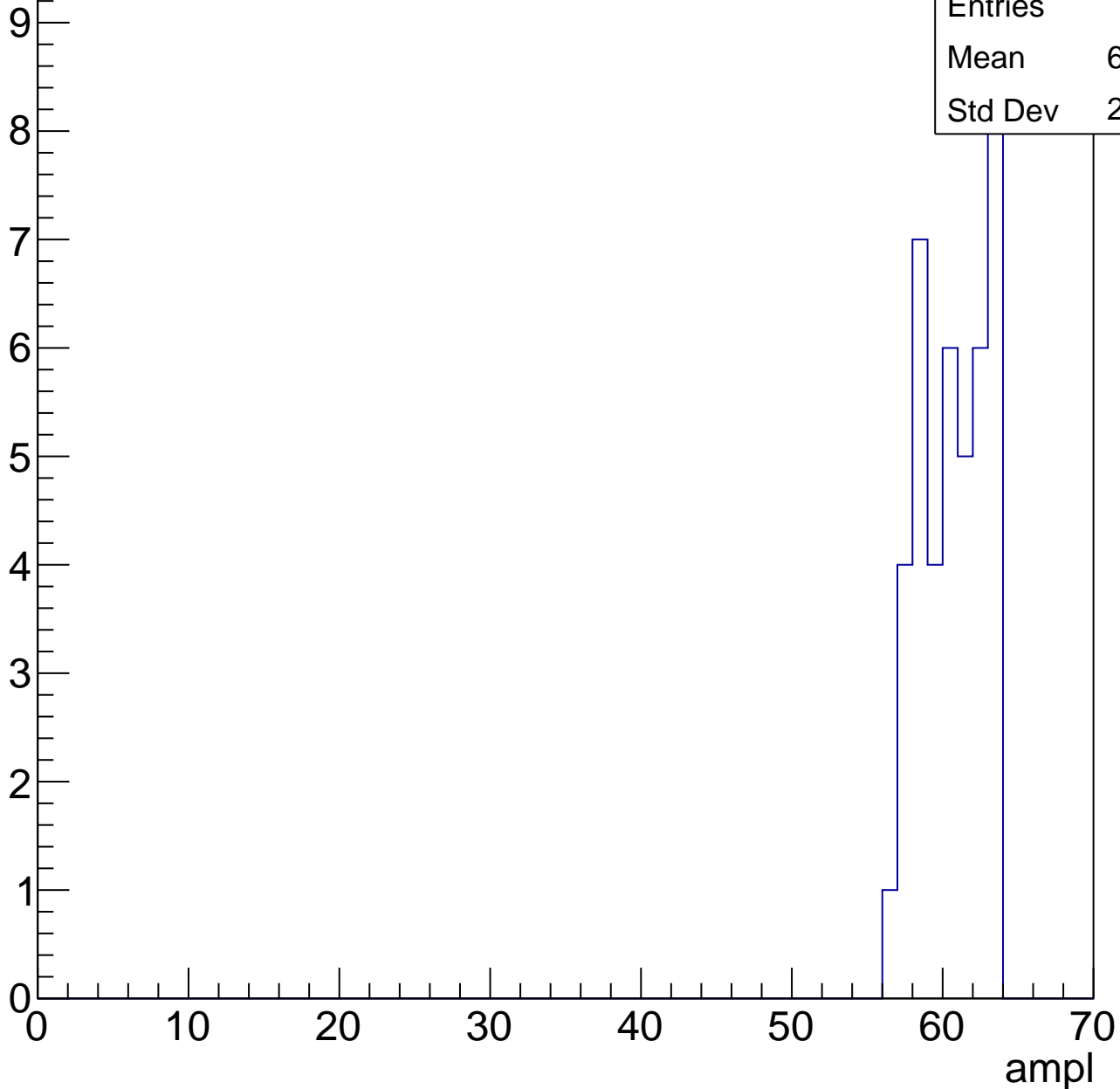


# B1L101S, U18-ch127, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	42
Mean	60.24
Std Dev	2.136



# B1L101S, U18-ch127, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	61.33
Std Dev	0.4714

ampl

0 10 20 30 40 50 60 70



# B1L101S, U18-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

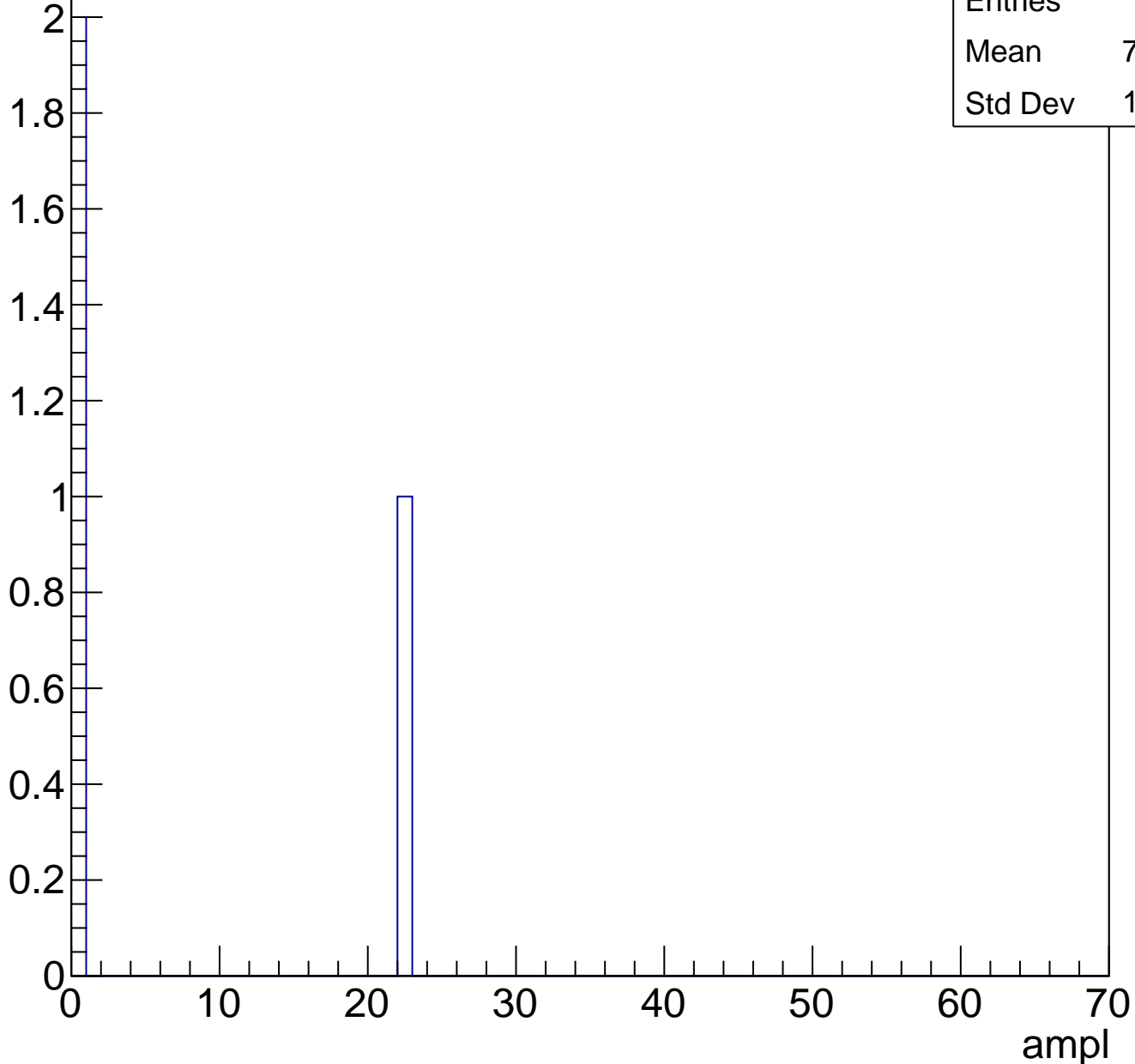


Entries	3
Mean	7.333
Std Dev	10.37

# B1L101S, U18-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	7.333
Std Dev	10.37