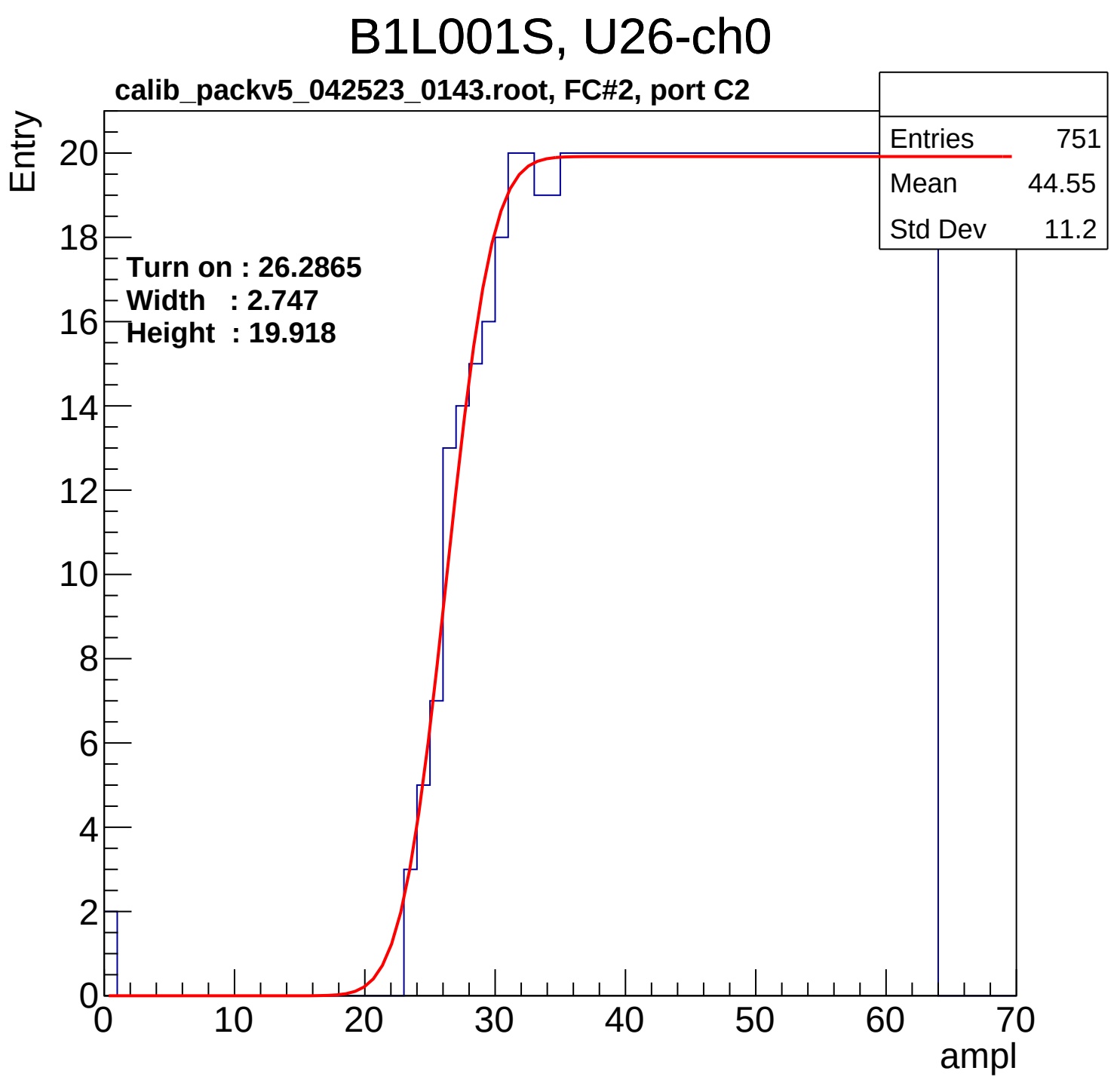
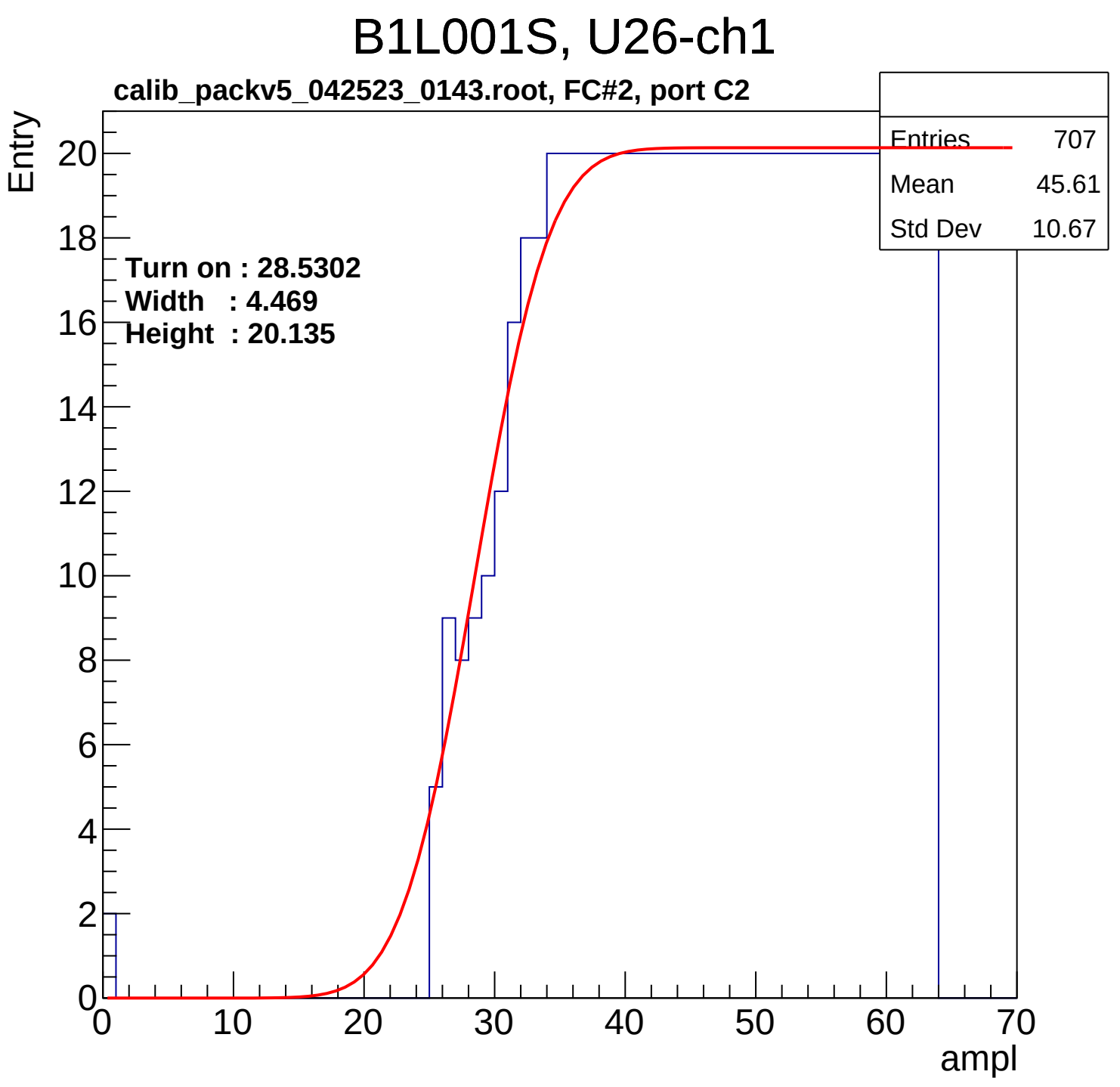
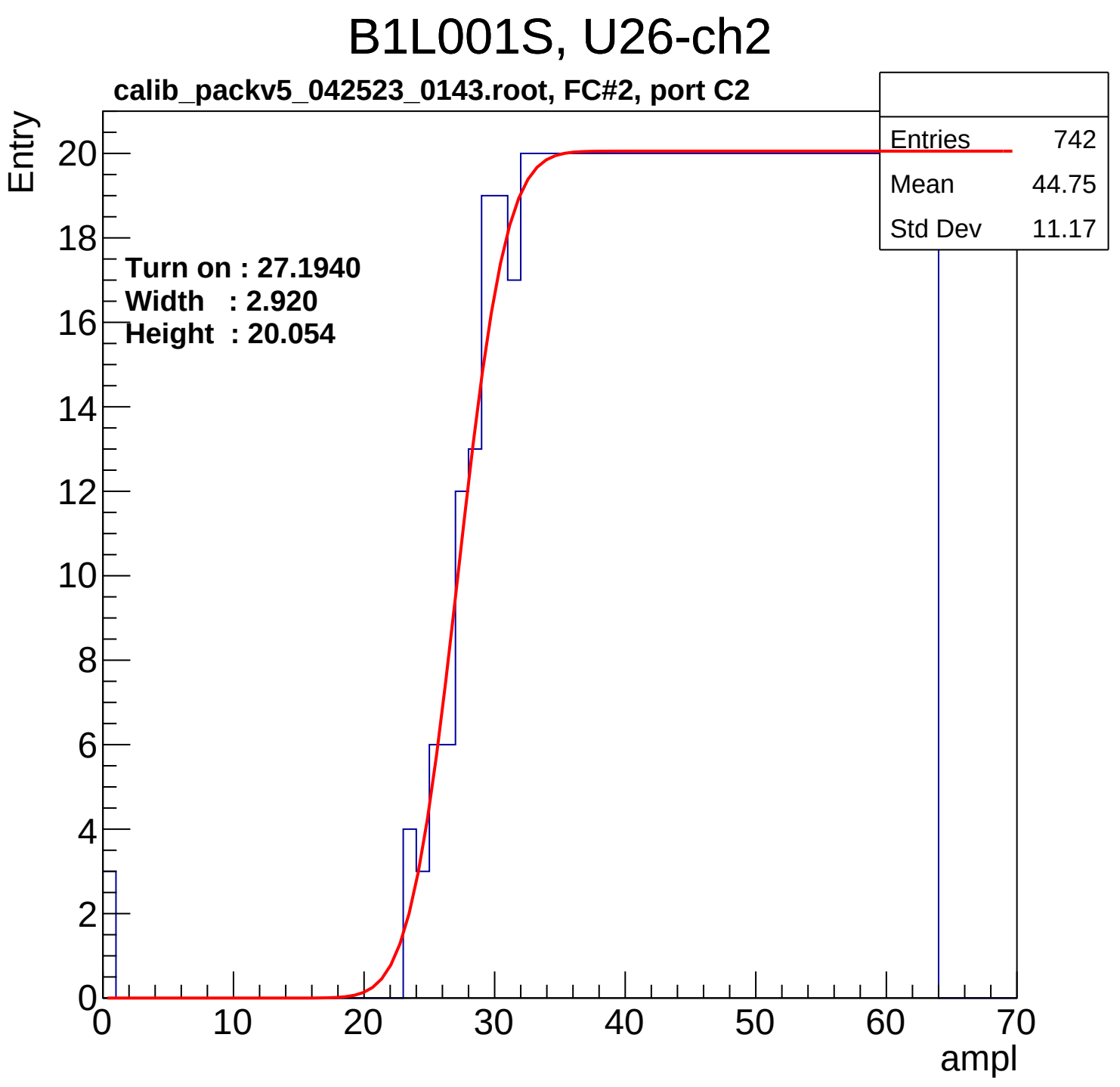
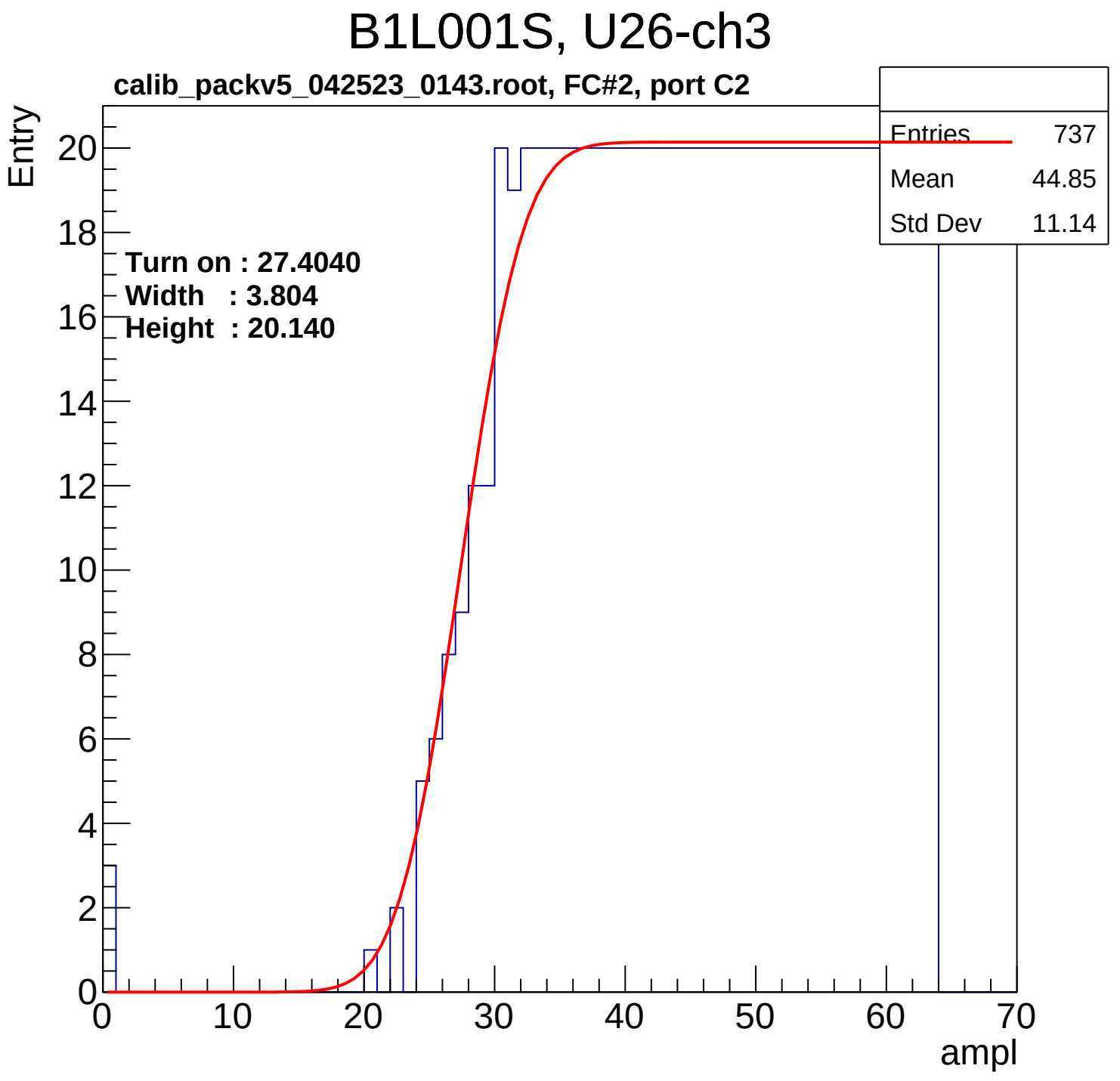
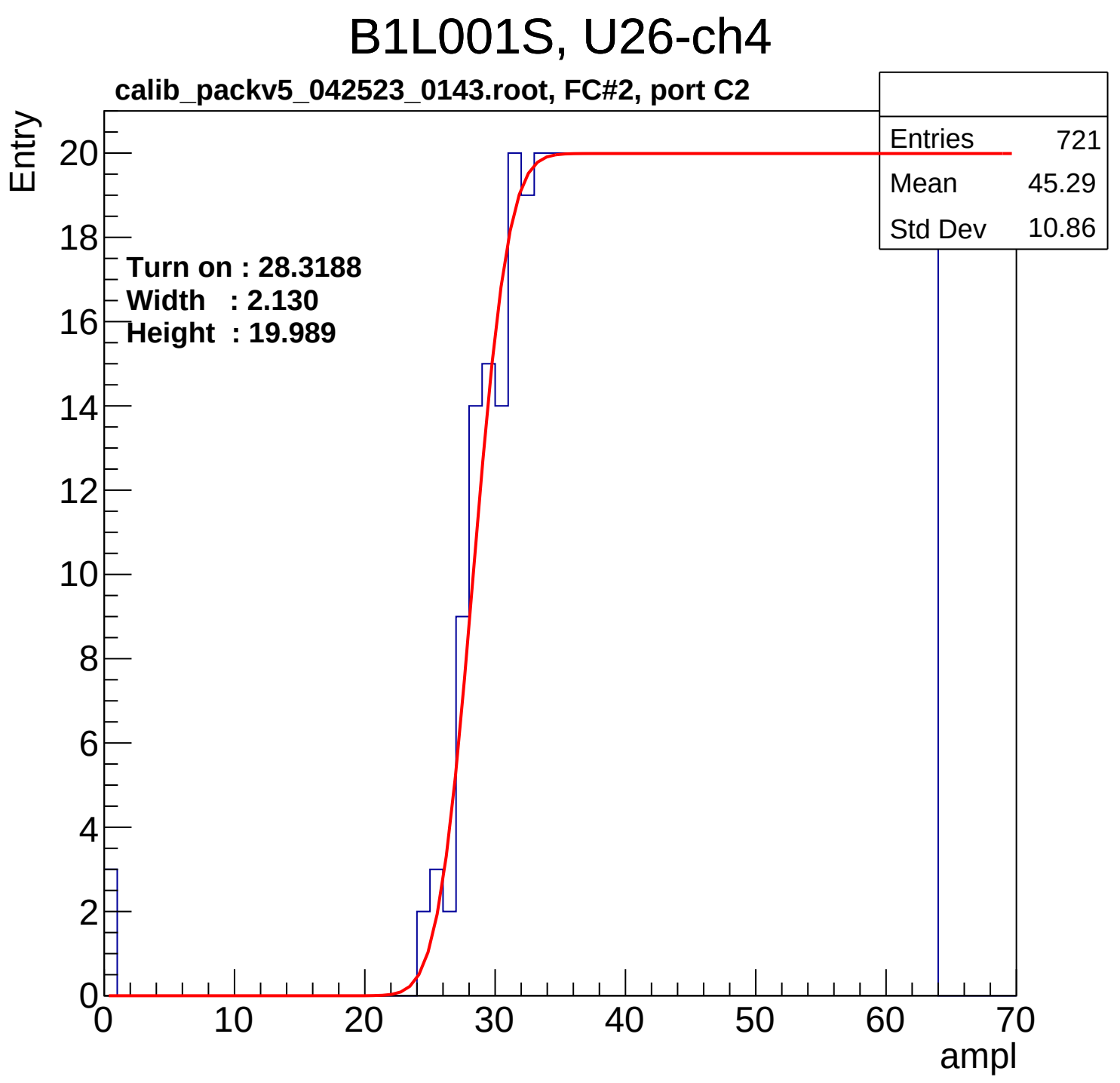
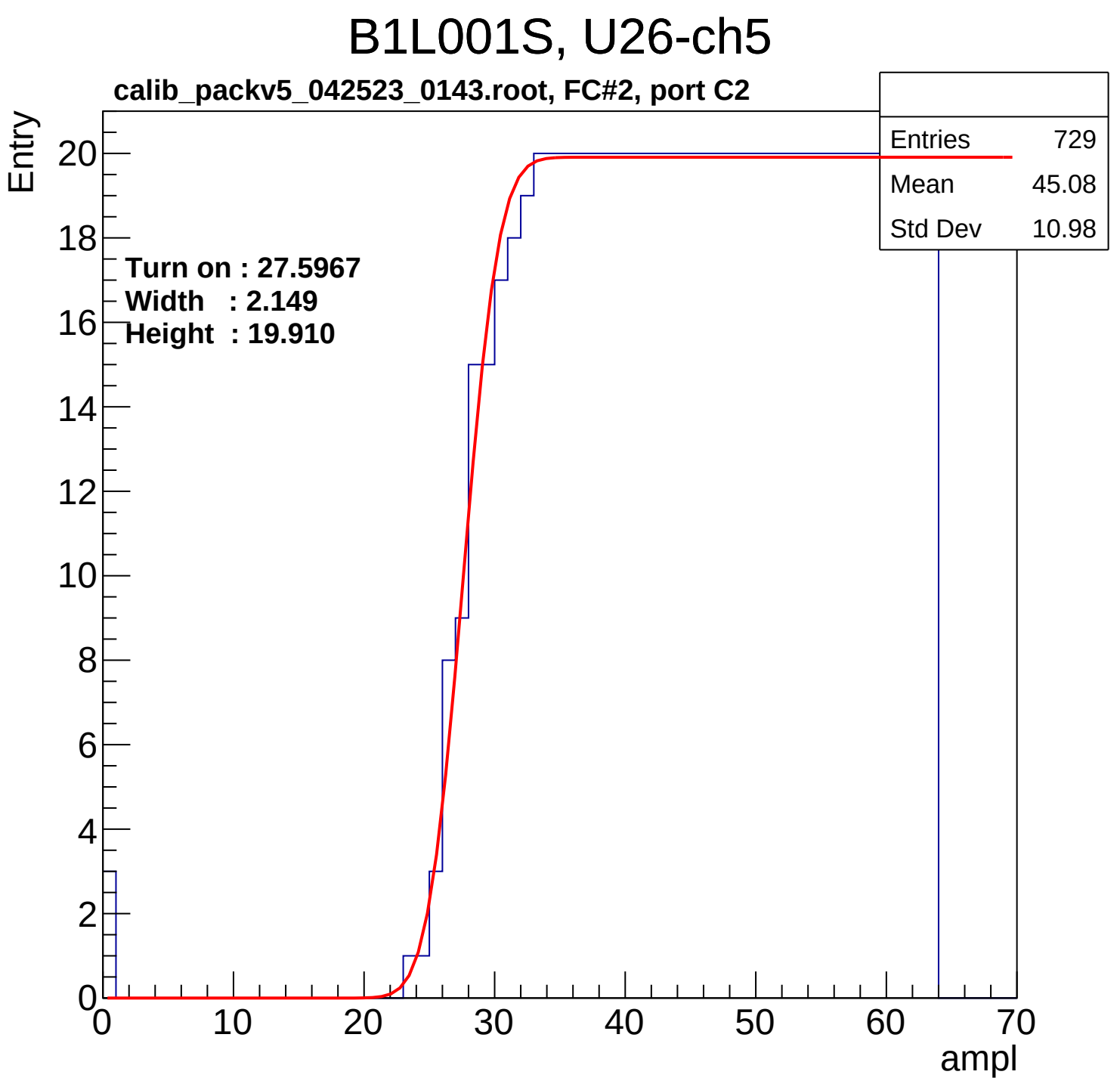

B1L001S, U26-ch0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 751
Mean 44.55
Std Dev 11.2
Turn on : 26.2865
Width : 2.747
Height : 19.918
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

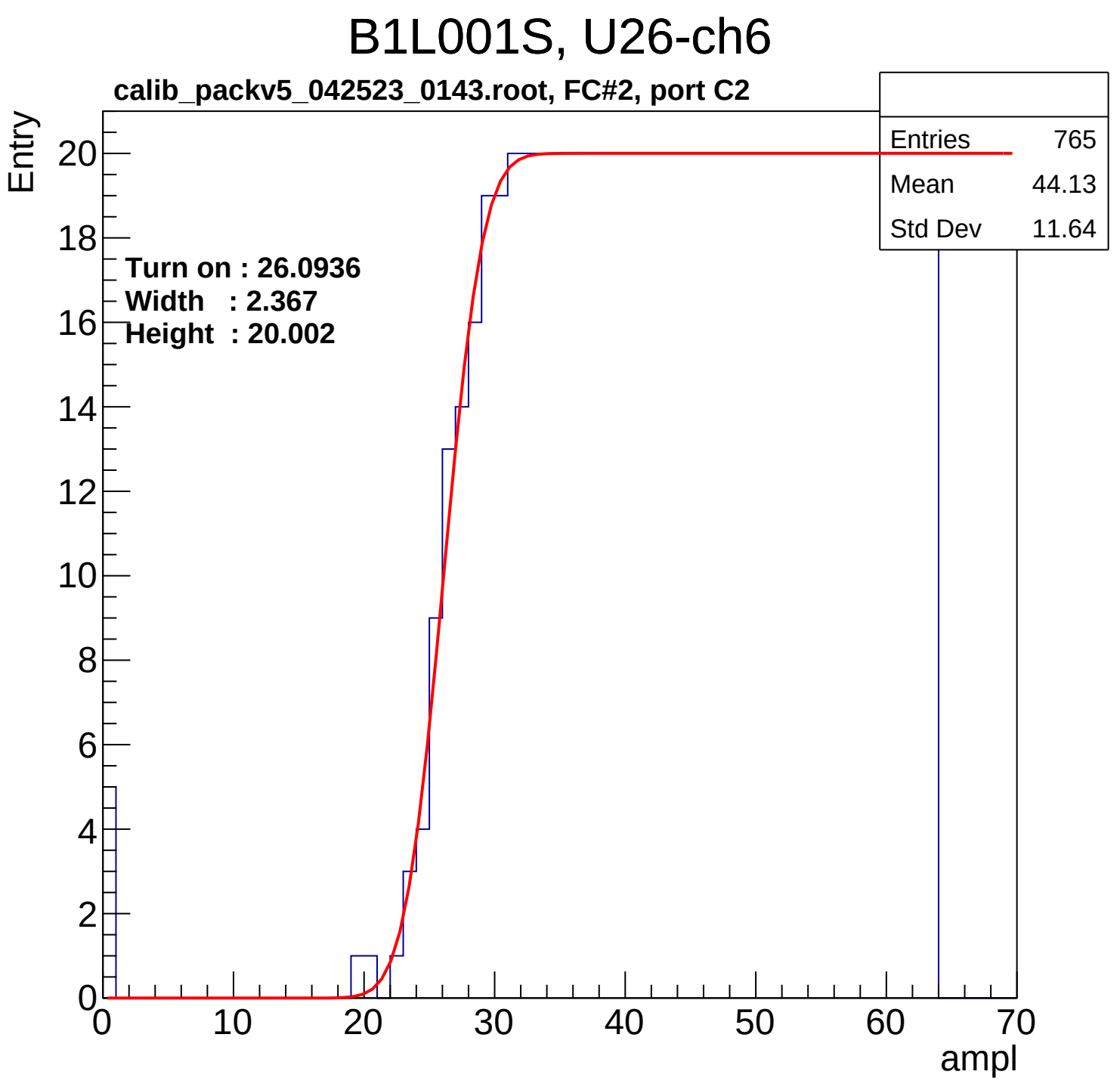

B1L001S, U26-ch1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 707
Mean 45.61
Std Dev 10.67
Turn on : 28.5302
Width : 4.469
Height : 20.135
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

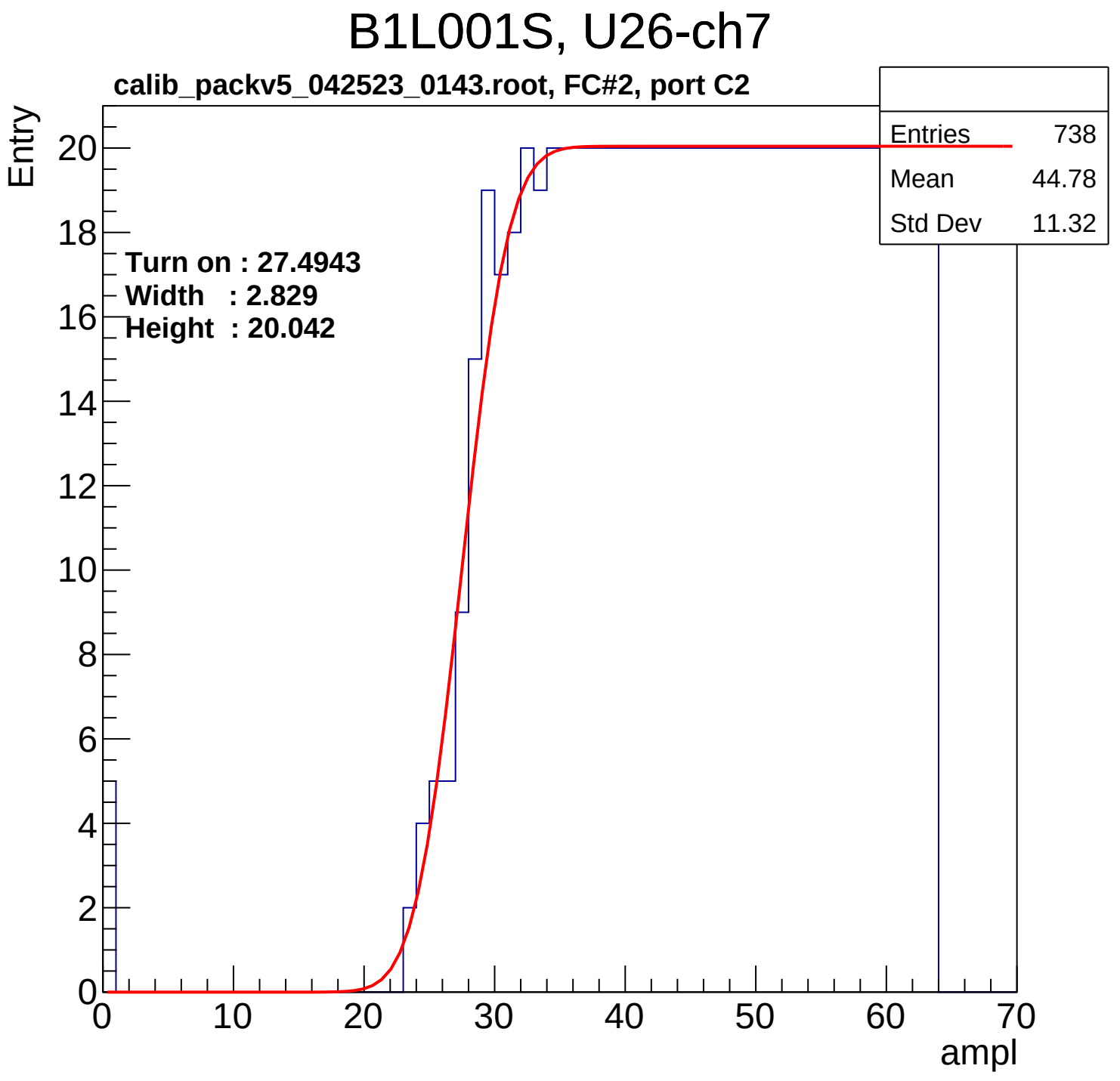

B1L001S, U26-ch2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 742
Mean 44.75
Std Dev 11.17
Turn on : 27.1940
Width : 2.920
Height : 20.054
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

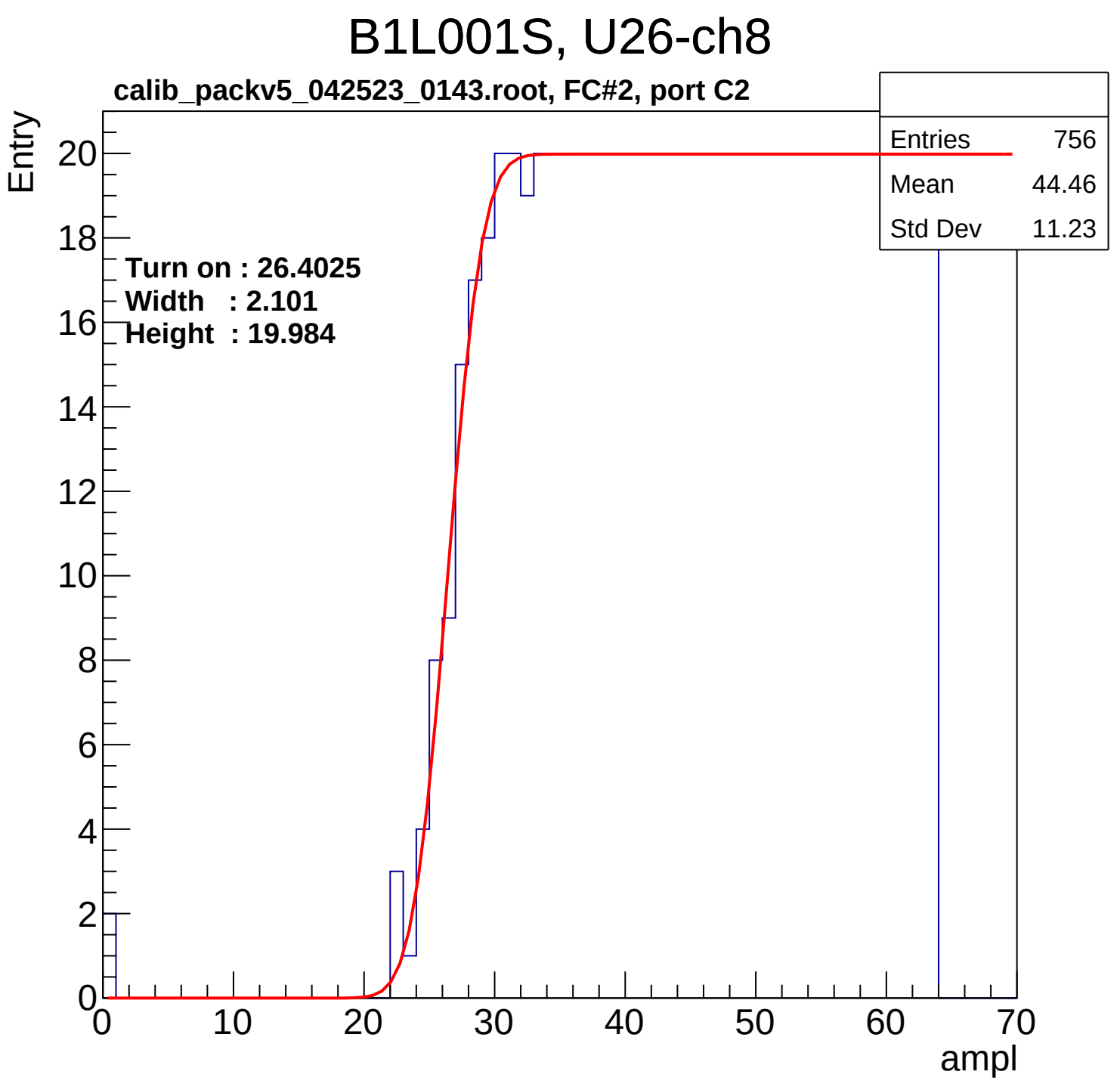

B1L001S, U26-ch3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 737
Mean 44.85
Std Dev 11.14
Turn on : 27.4040
Width : 3.804
Height : 20.140
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

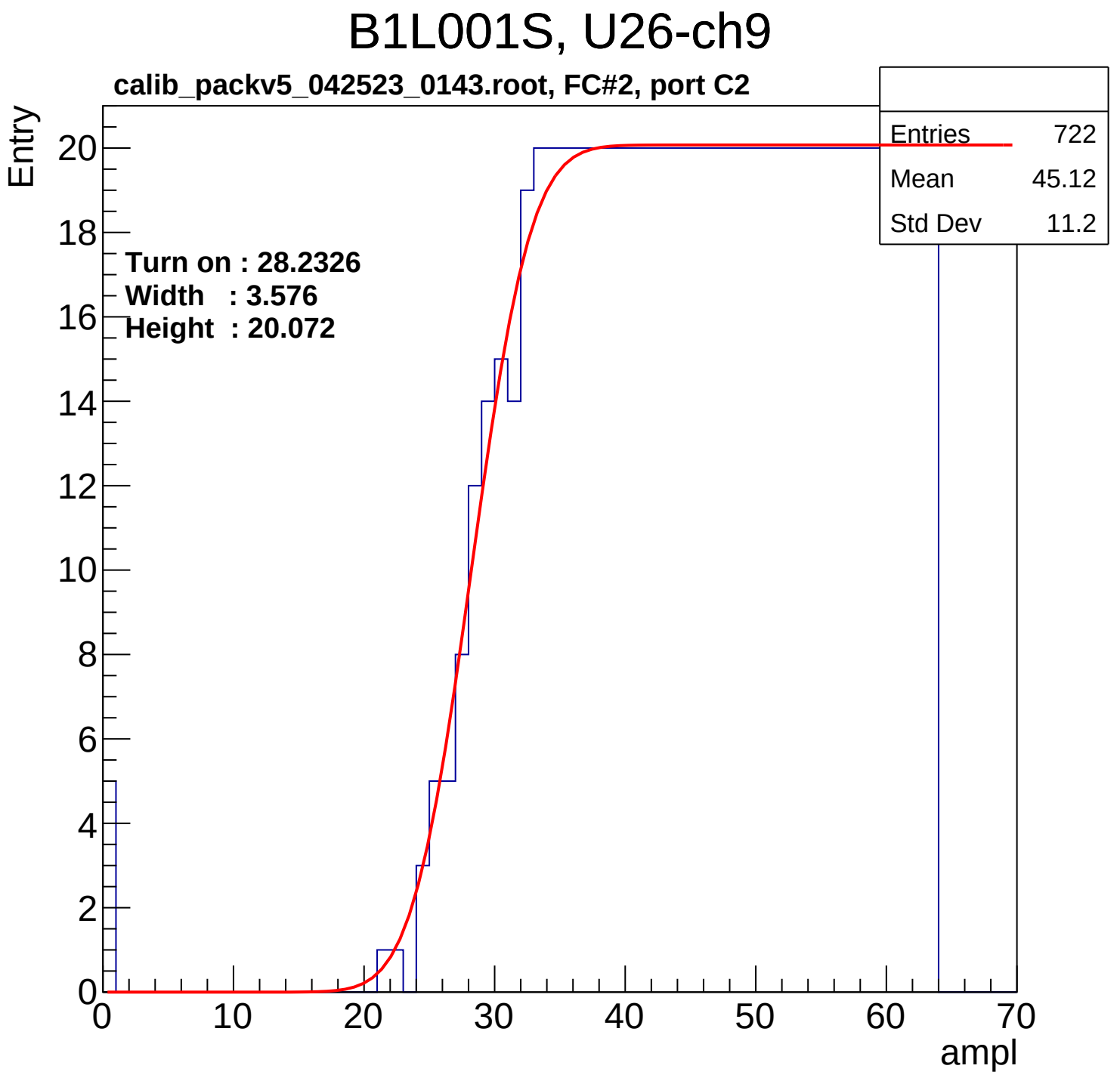

B1L001S, U26-ch4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 721
Mean 45.29
Std Dev 10.86
Turn on : 28.3188
Width : 2.130
Height : 19.989
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

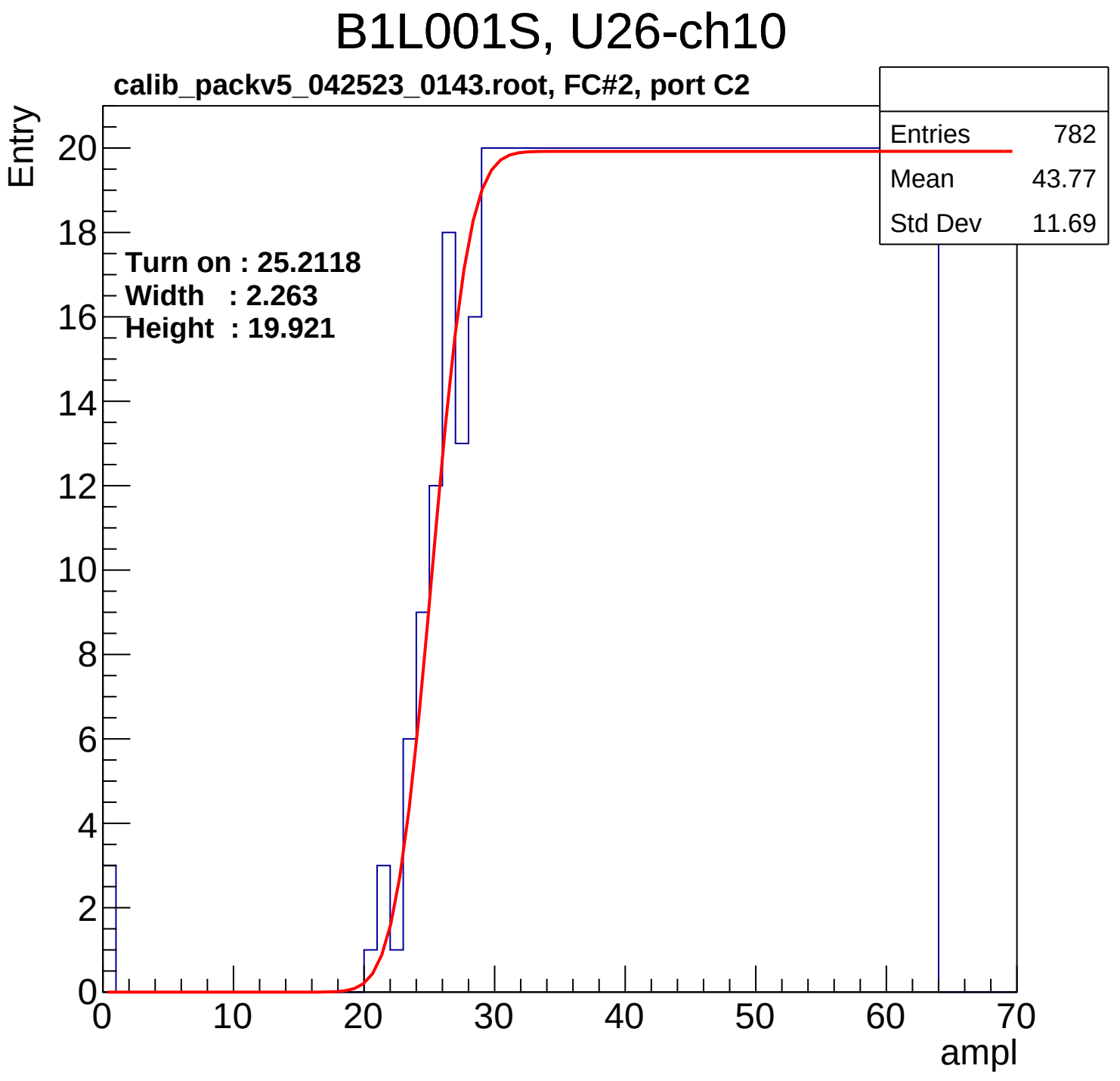

B1L001S, U26-ch5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 729
Mean 45.08
Std Dev 10.98
Turn on : 27.5967
Width : 2.149
Height : 19.910
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

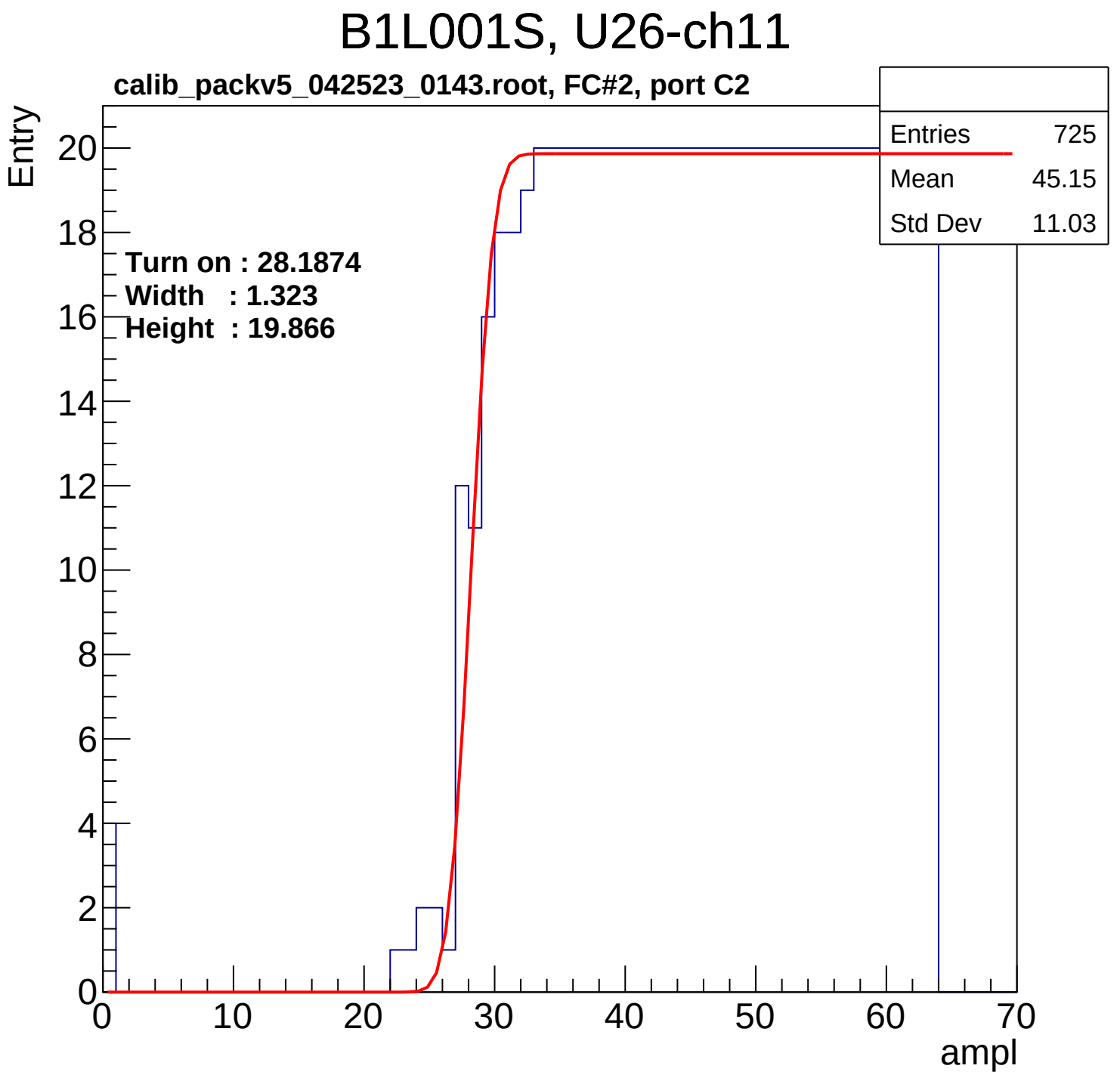

B1L001S, U26-ch6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 765
Mean 44.13
Std Dev 11.64
Turn on : 26.0936
Width : 2.367
Height : 20.002
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

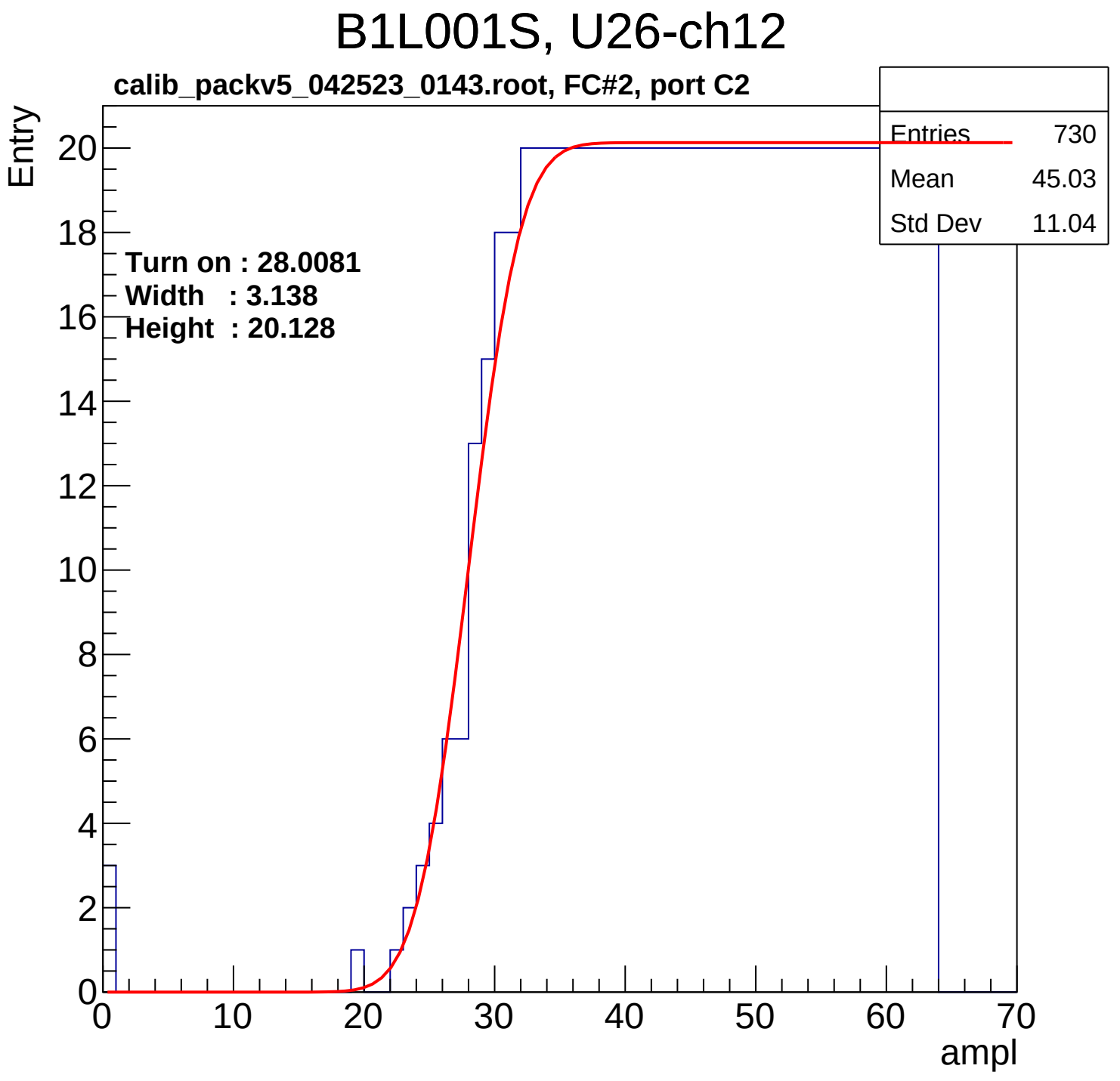

B1L001S, U26-ch7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 738
Mean 44.78
Std Dev 11.32
Turn on : 27.4943
Width : 2.829
Height : 20.042
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

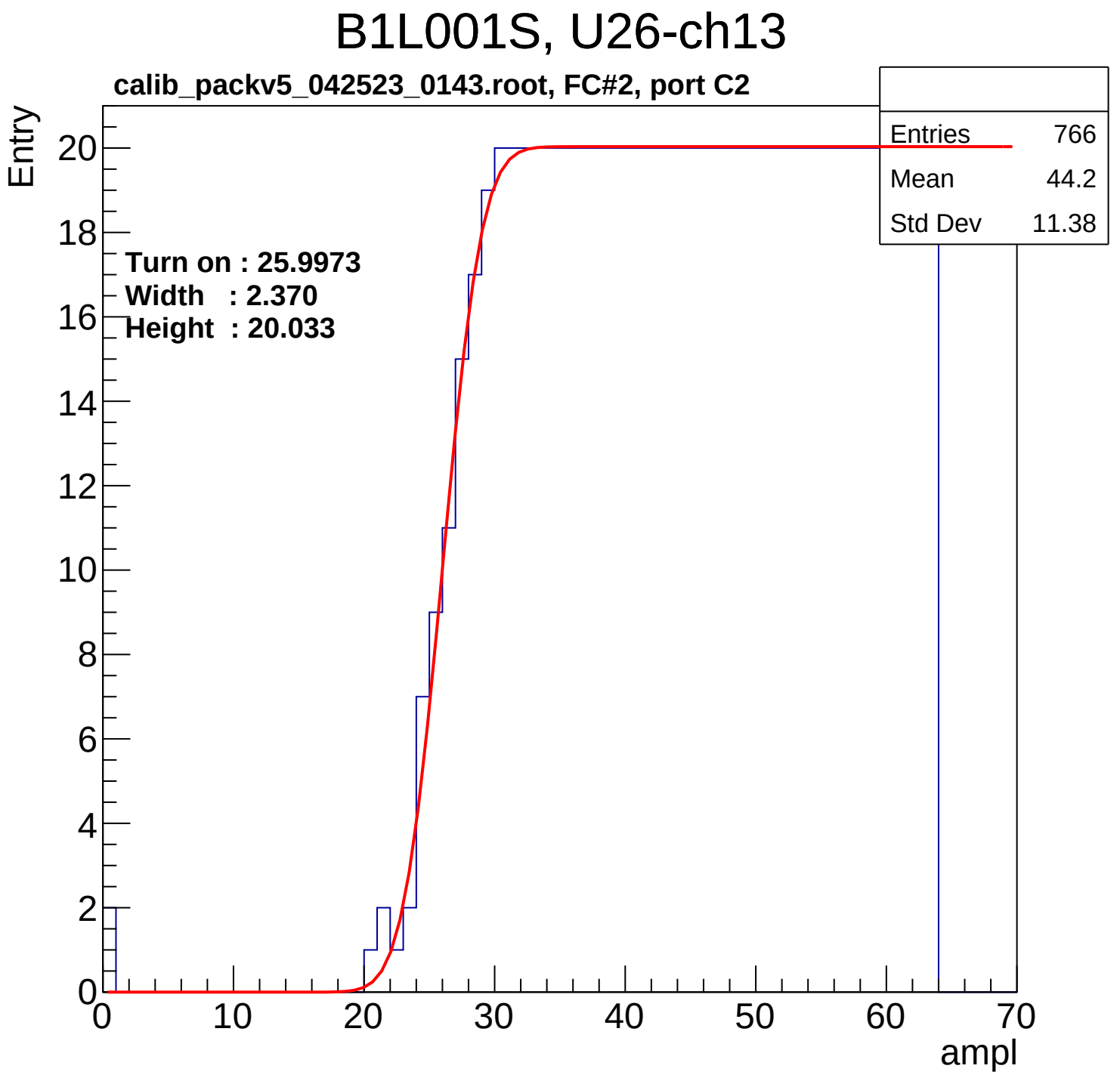

B1L001S, U26-ch8
calib_packv5_042523_0143.root, FC#2, port C2
Entries 756
Mean 44.46
Std Dev 11.23
Turn on : 26.4025
Width : 2.101
Height : 19.984
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

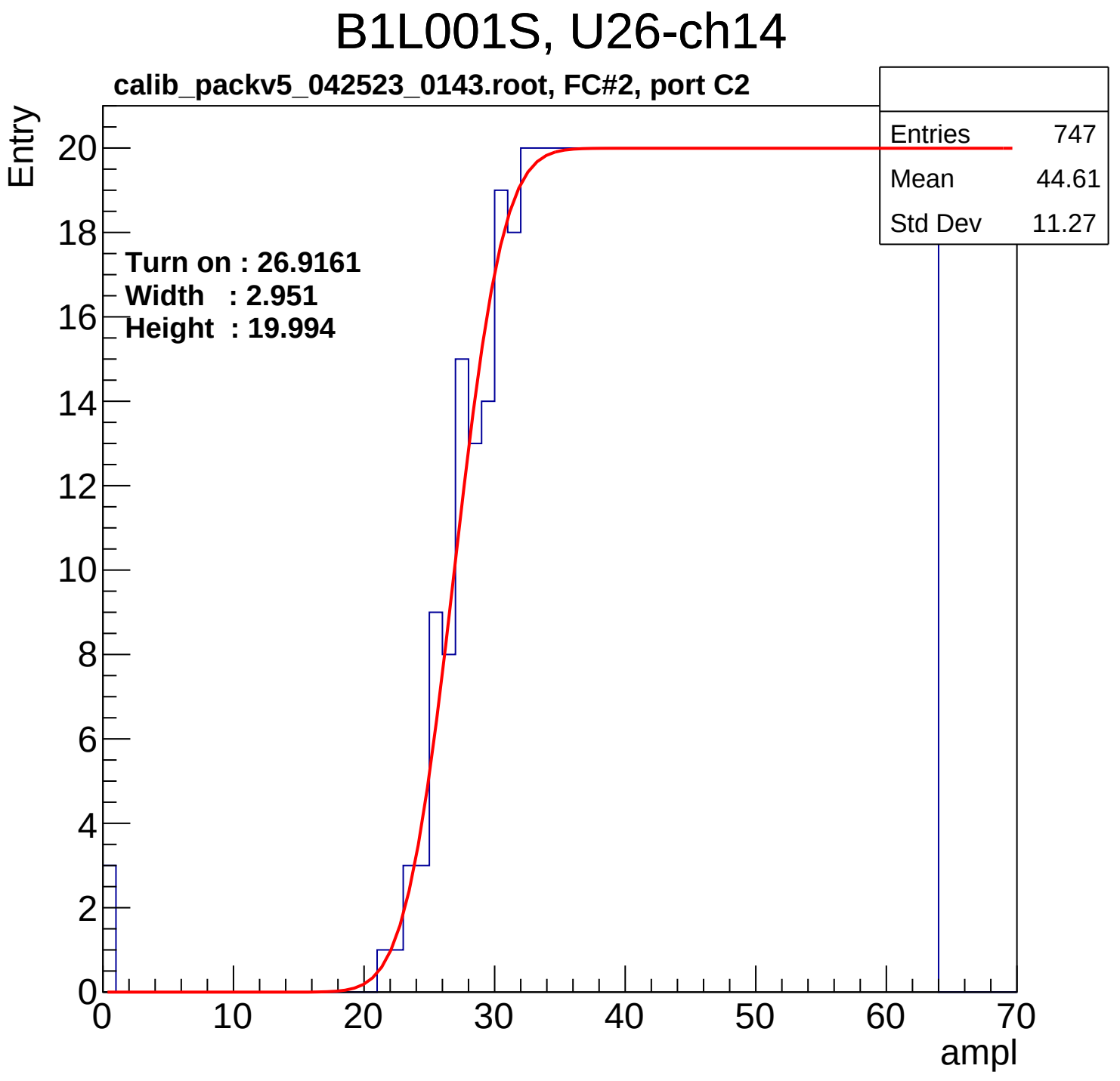

B1L001S, U26-ch9
calib_packv5_042523_0143.root, FC#2, port C2
Entries 722
Mean 45.12
Std Dev 11.2
Turn on : 28.2326
Width : 3.576
Height : 20.072
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

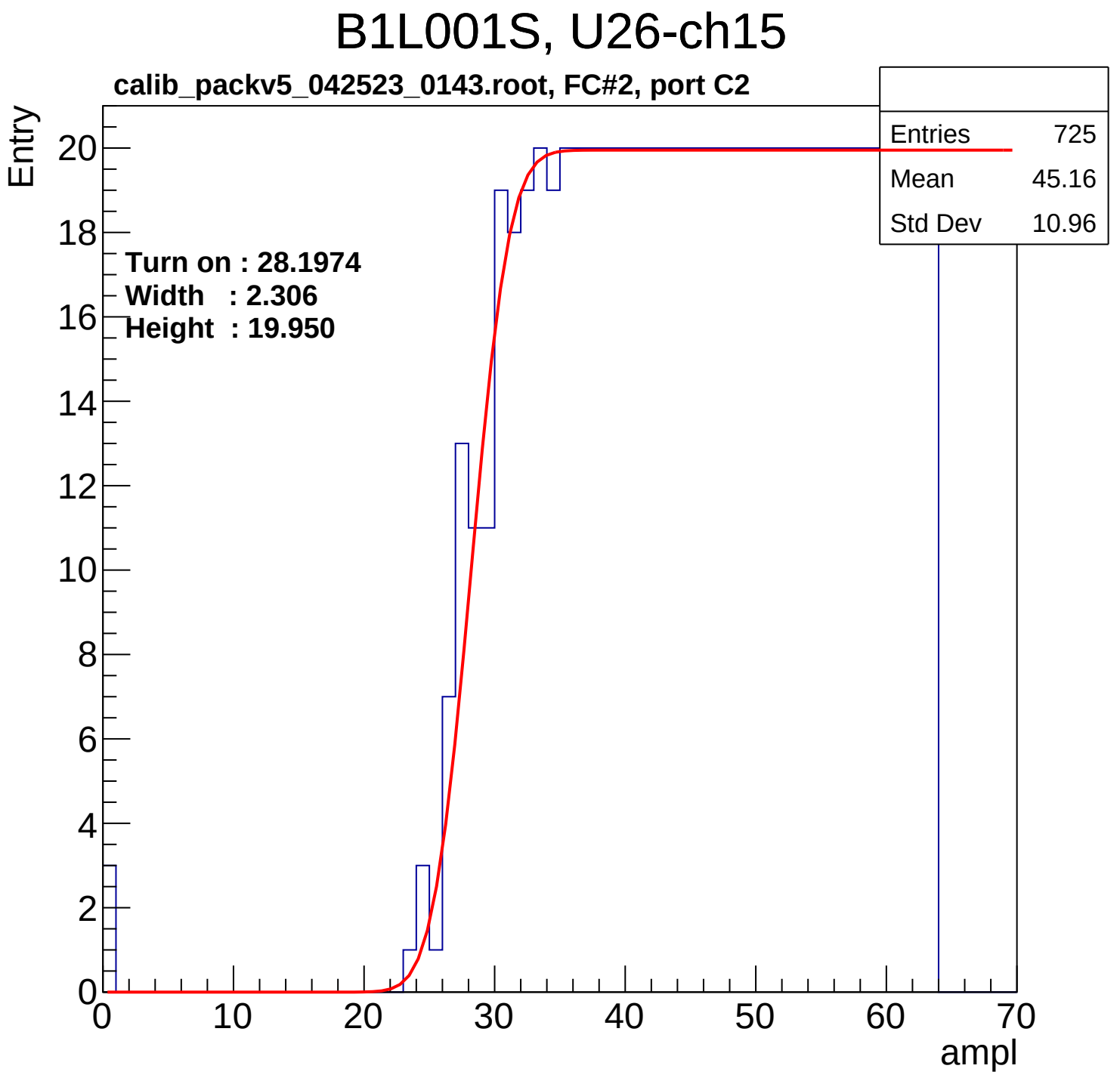

B1L001S, U26-ch10
calib_packv5_042523_0143.root, FC#2, port C2
Entries 782
Mean 43.77
Std Dev 11.69
Turn on : 25.2118
Width : 2.263
Height : 19.921
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

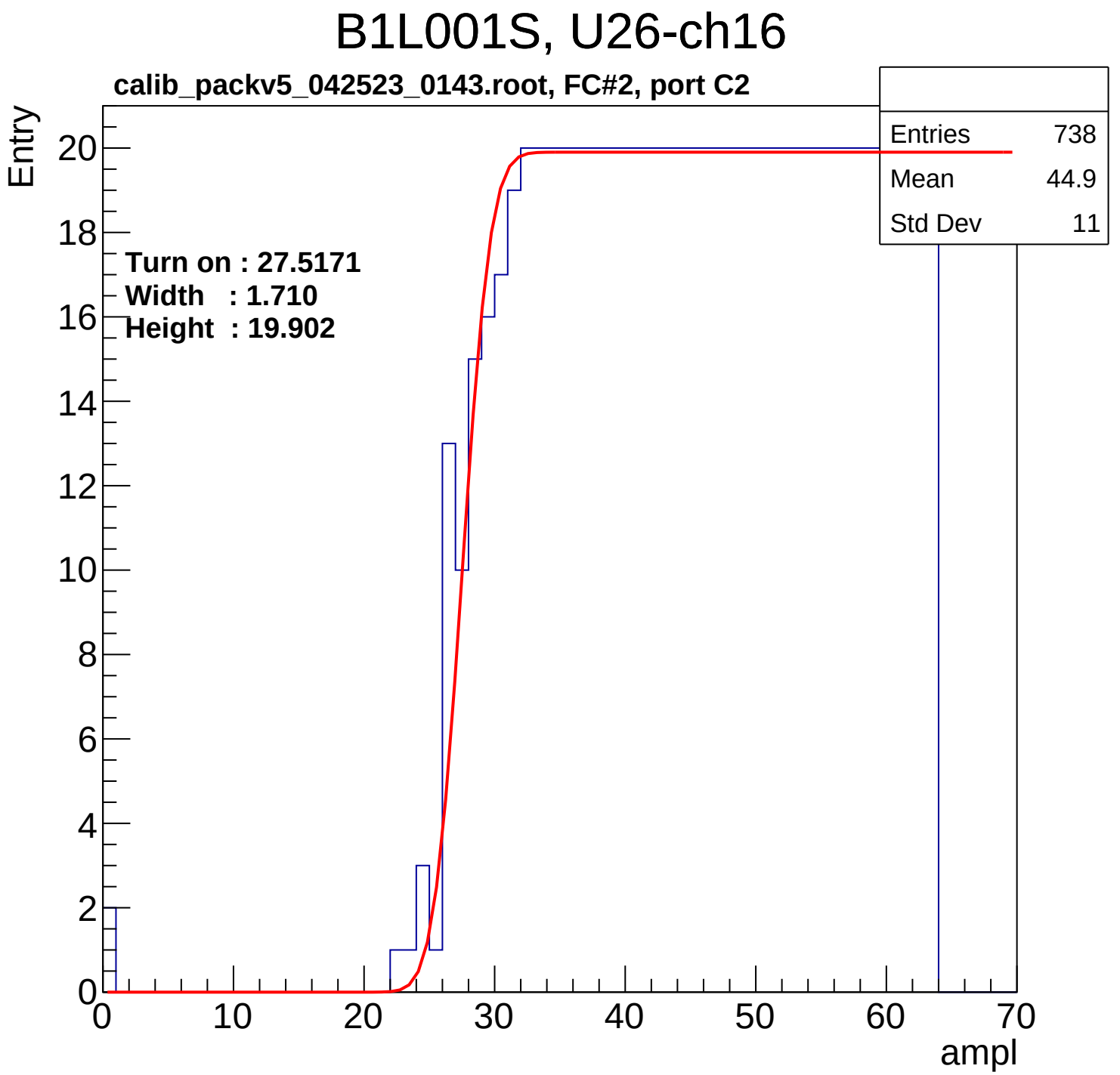

B1L001S, U26-ch11
calib_packv5_042523_0143.root, FC#2, port C2
Entries 725
Mean 45.15
Std Dev 11.03
Turn on : 28.1874
Width : 1.323
Height : 19.866
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

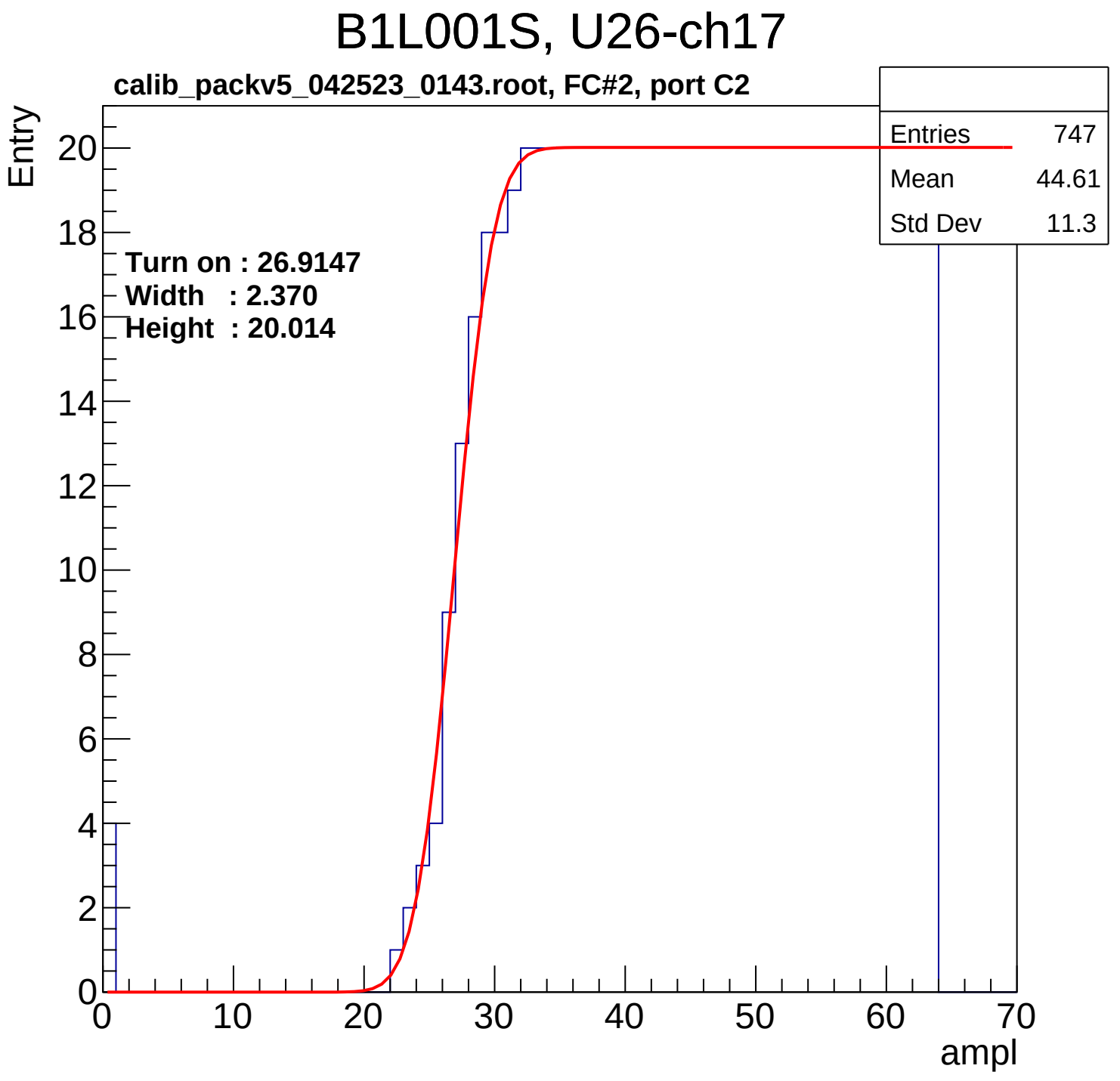

B1L001S, U26-ch12
calib_packv5_042523_0143.root, FC#2, port C2
Entries 730
Mean 45.03
Std Dev 11.04
Turn on : 28.0081
Width : 3.138
Height : 20.128
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

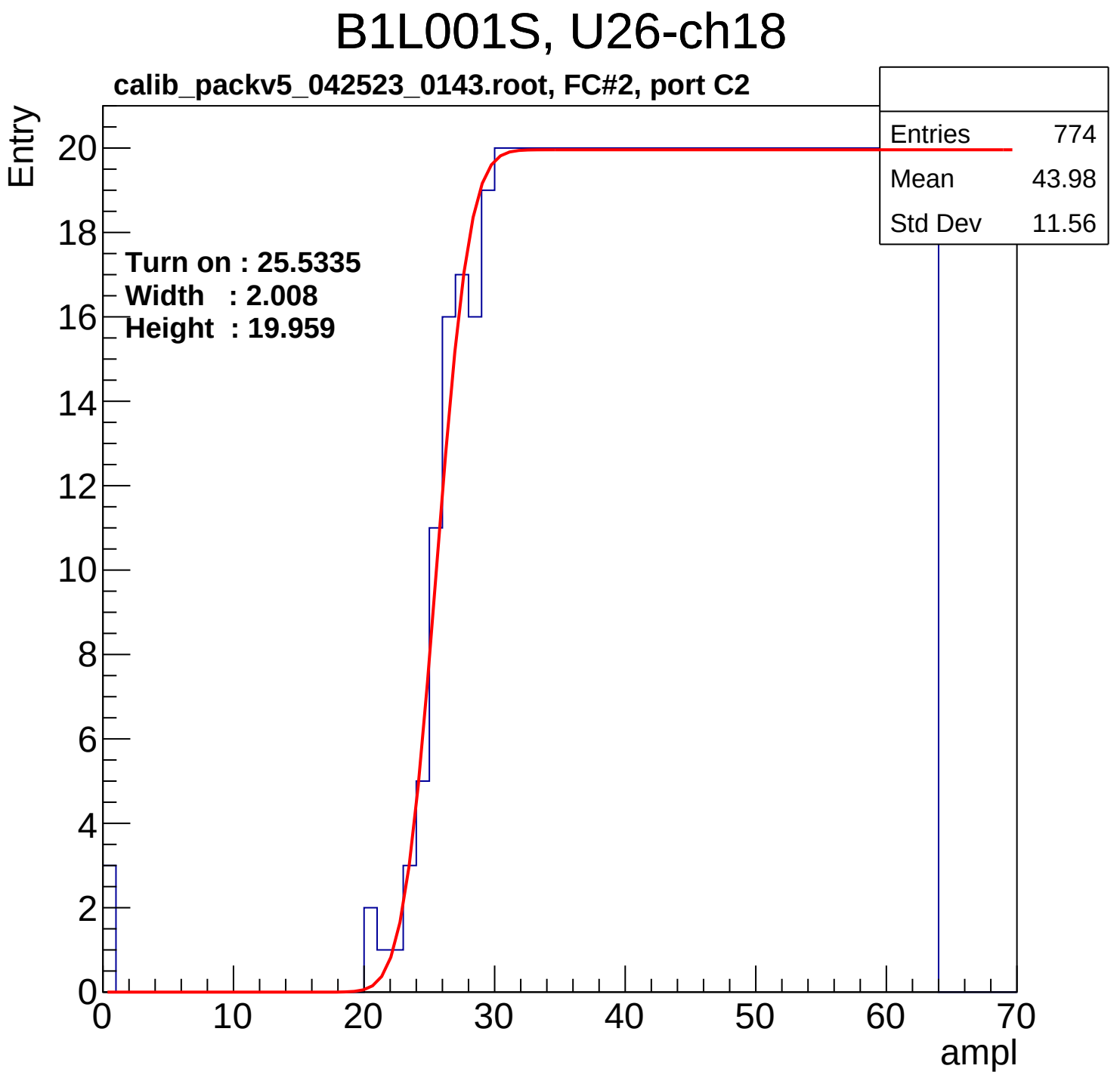

B1L001S, U26-ch13
calib_packv5_042523_0143.root, FC#2, port C2
Entries 766
Mean 44.2
Std Dev 11.38
Turn on : 25.9973
Width : 2.370
Height : 20.033
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

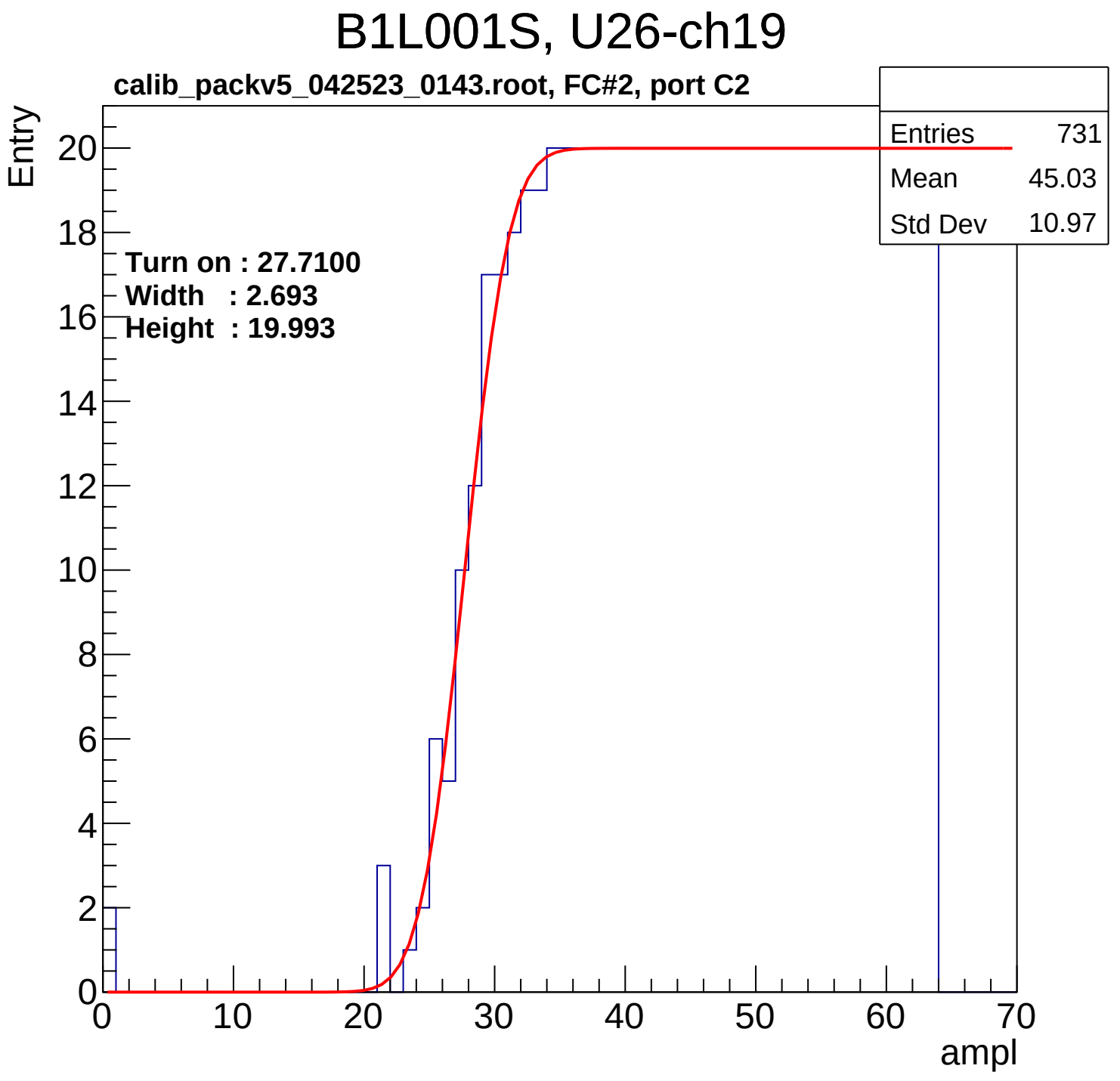

B1L001S, U26-ch14
calib_packv5_042523_0143.root, FC#2, port C2
Entries 747
Mean 44.61
Std Dev 11.27
Turn on : 26.9161
Width : 2.951
Height : 19.994
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

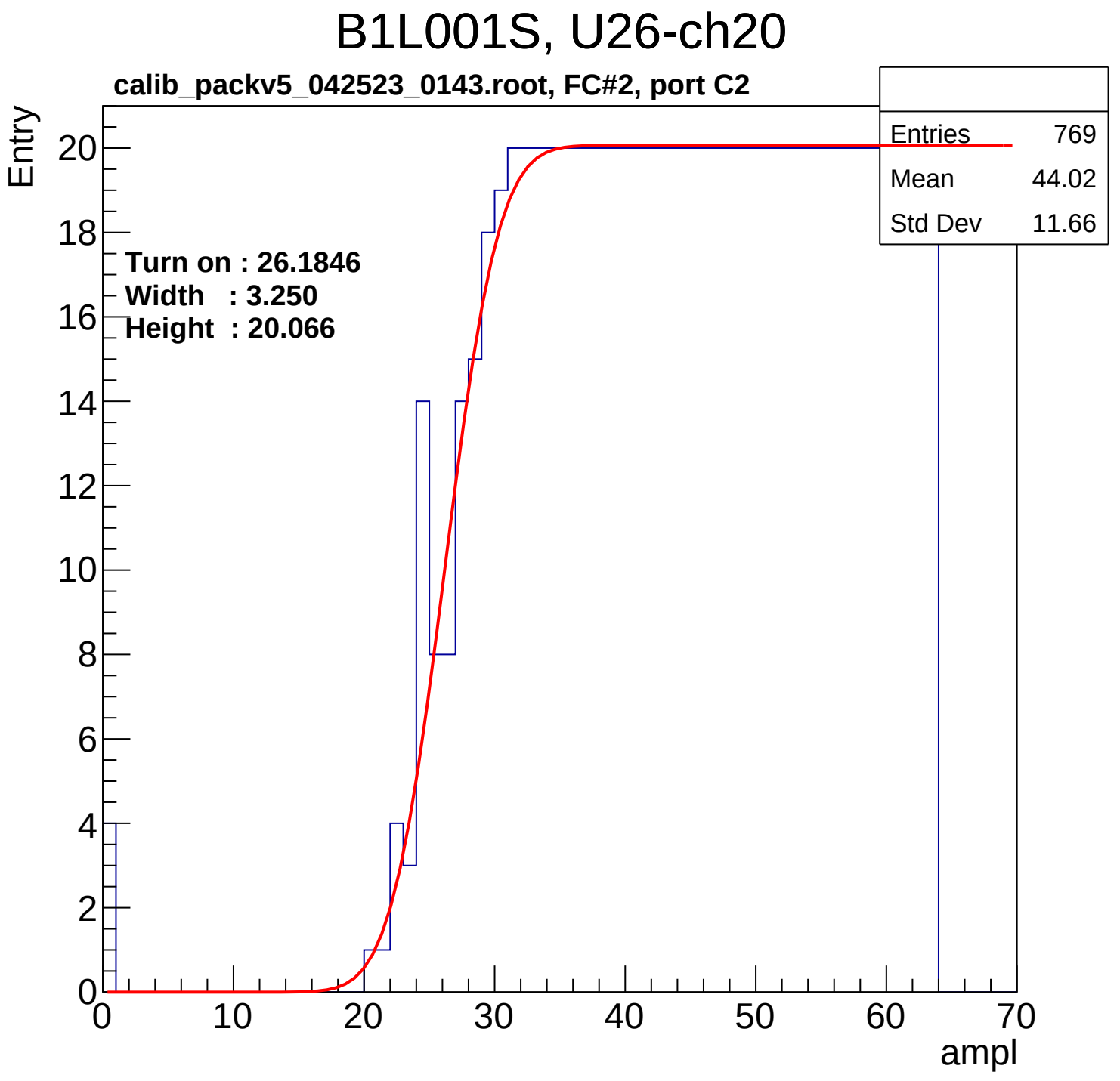

B1L001S, U26-ch15
calib_packv5_042523_0143.root, FC#2, port C2
Entries 725
Mean 45.16
Std Dev 10.96
Turn on : 28.1974
Width : 2.306
Height : 19.950
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

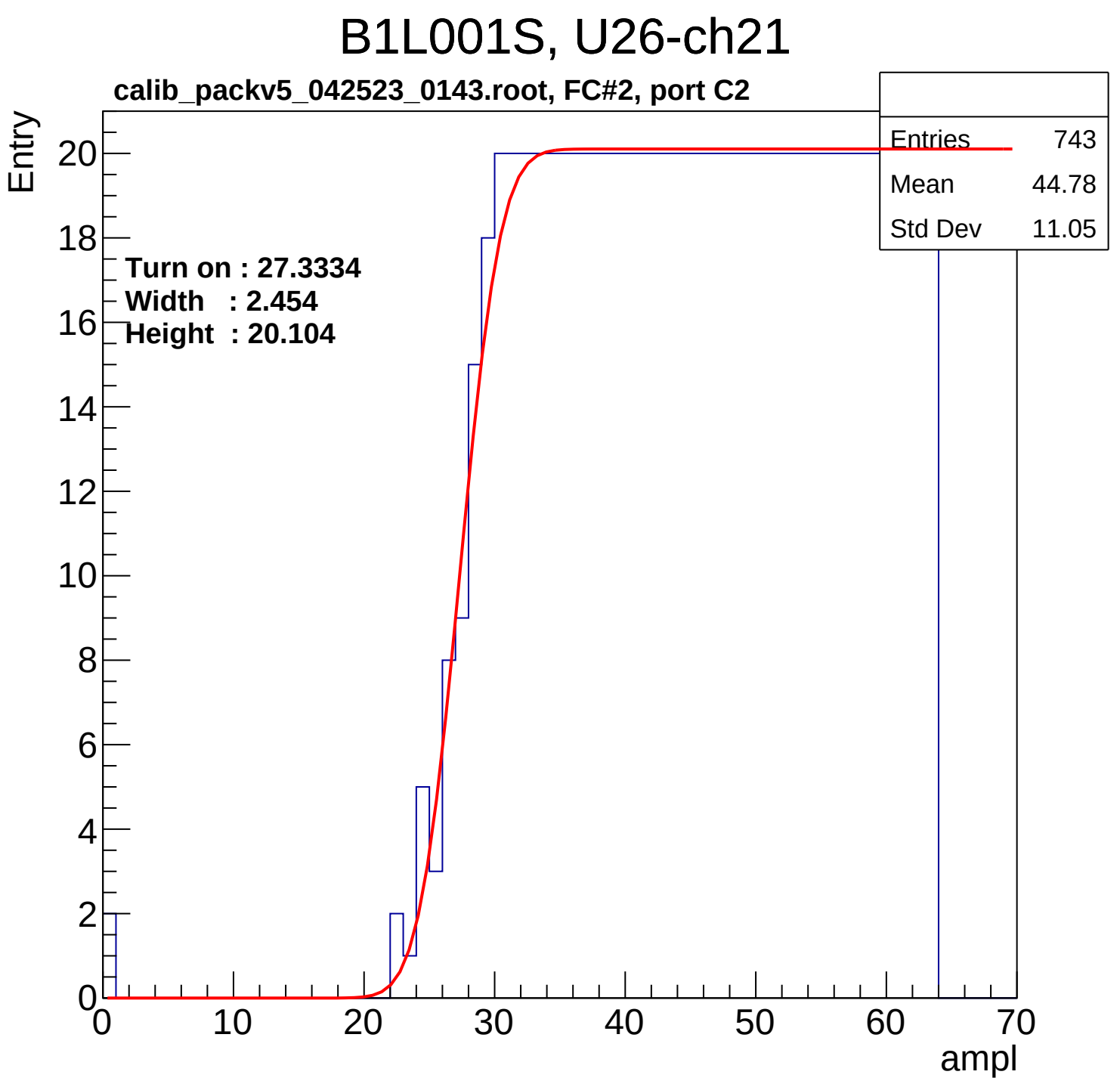

B1L001S, U26-ch16
calib_packv5_042523_0143.root, FC#2, port C2
Entries 738
Mean 44.9
Std Dev 11
Turn on : 27.5171
Width : 1.710
Height : 19.902
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

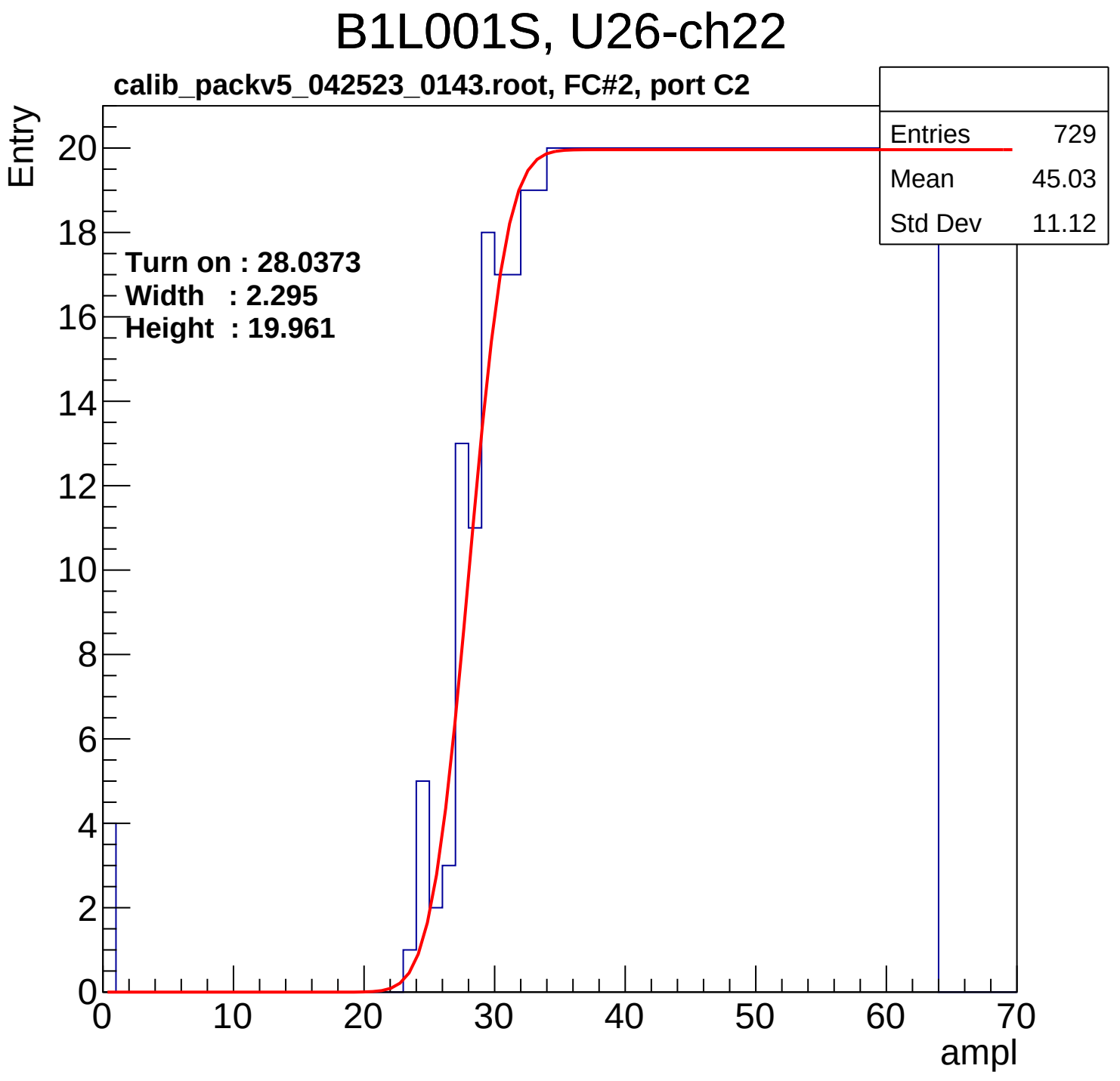

B1L001S, U26-ch17
calib_packv5_042523_0143.root, FC#2, port C2
Entries 747
Mean 44.61
Std Dev 11.3
Turn on : 26.9147
Width : 2.370
Height : 20.014
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

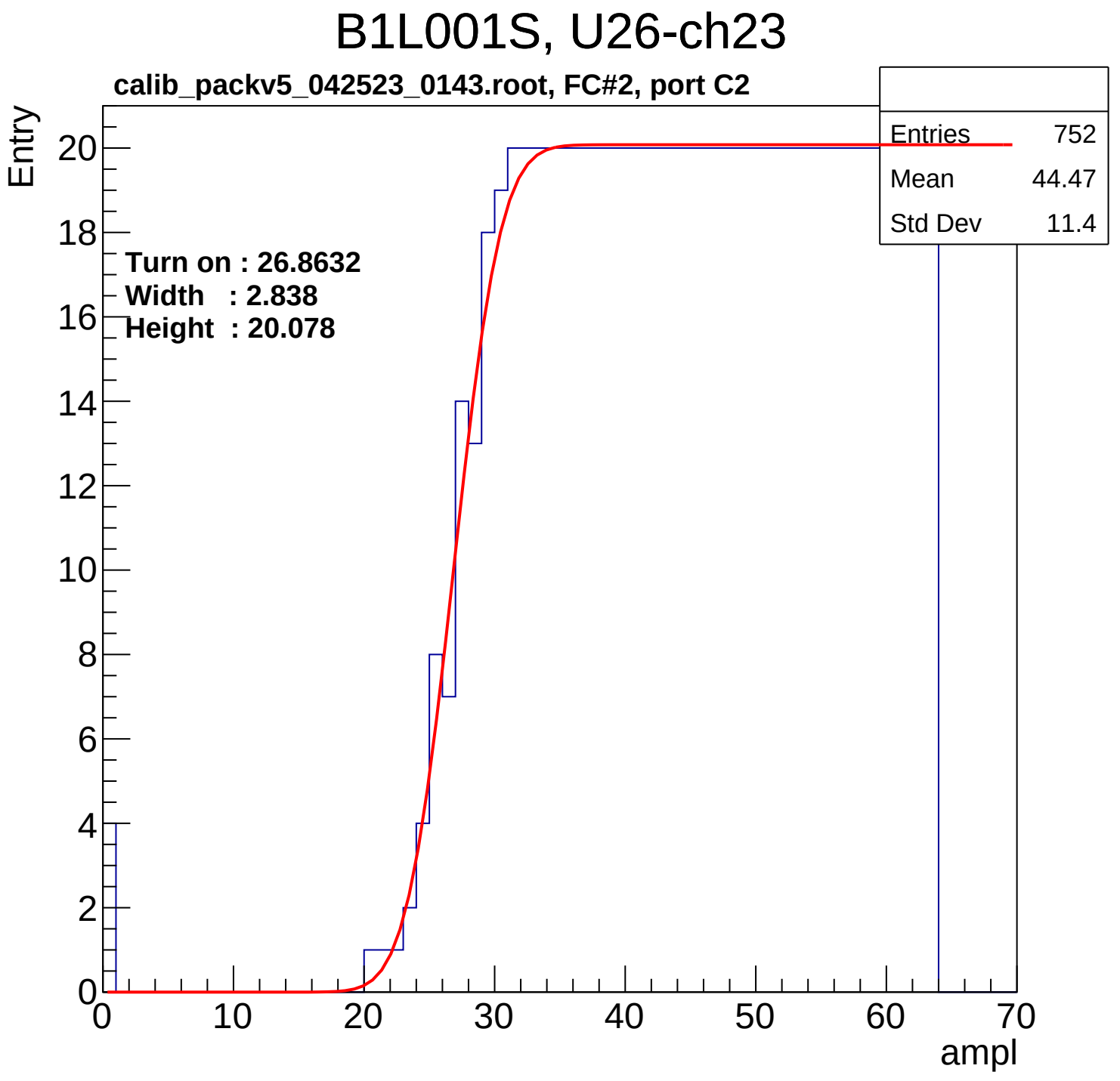

B1L001S, U26-ch18
calib_packv5_042523_0143.root, FC#2, port C2
Entries 774
Mean 43.98
Std Dev 11.56
Turn on : 25.5335
Width : 2.008
Height : 19.959
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

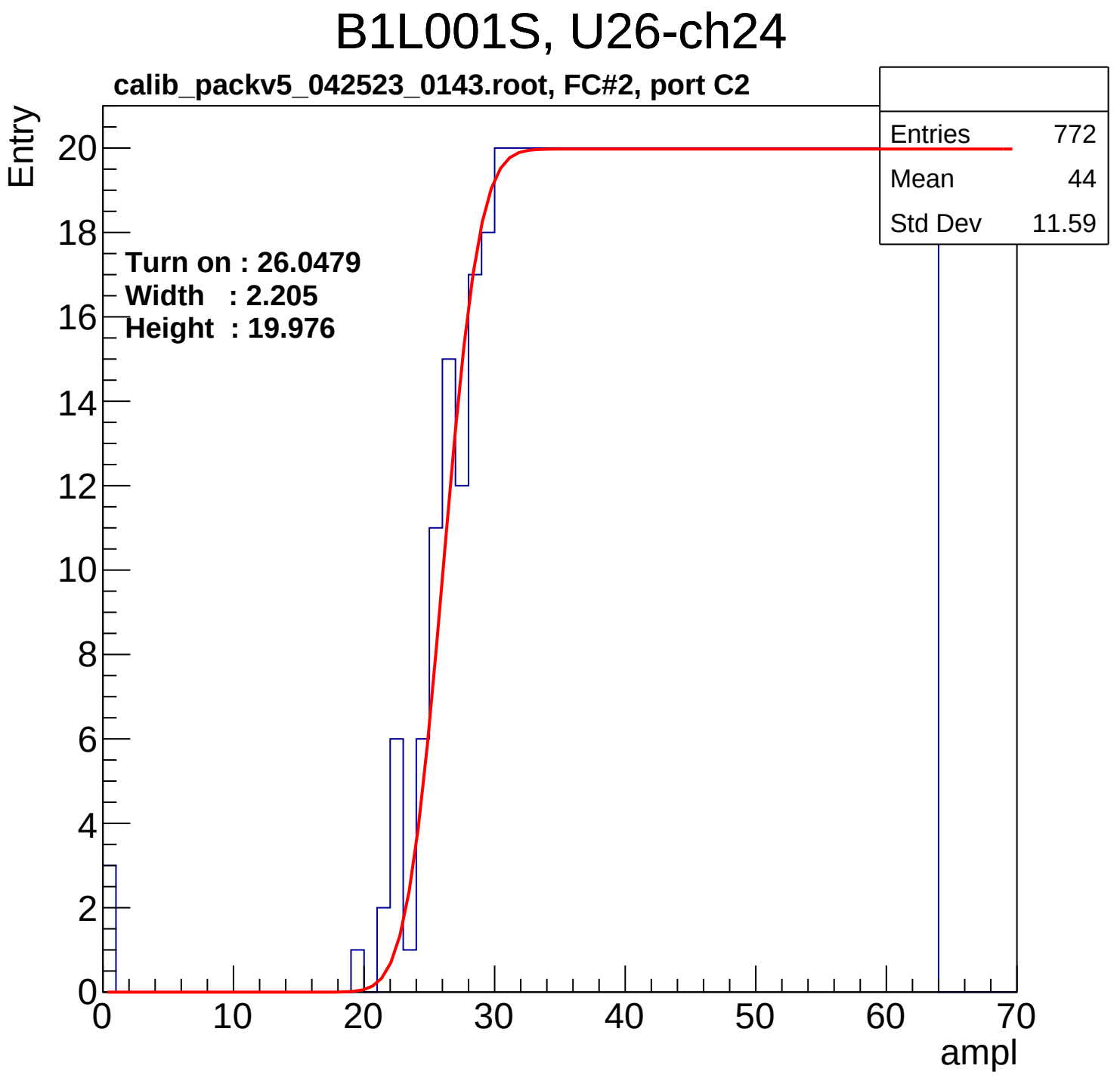

B1L001S, U26-ch19
calib_packv5_042523_0143.root, FC#2, port C2
Entries 731
Mean 45.03
Std Dev 10.97
Turn on : 27.7100
Width : 2.693
Height : 19.993
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

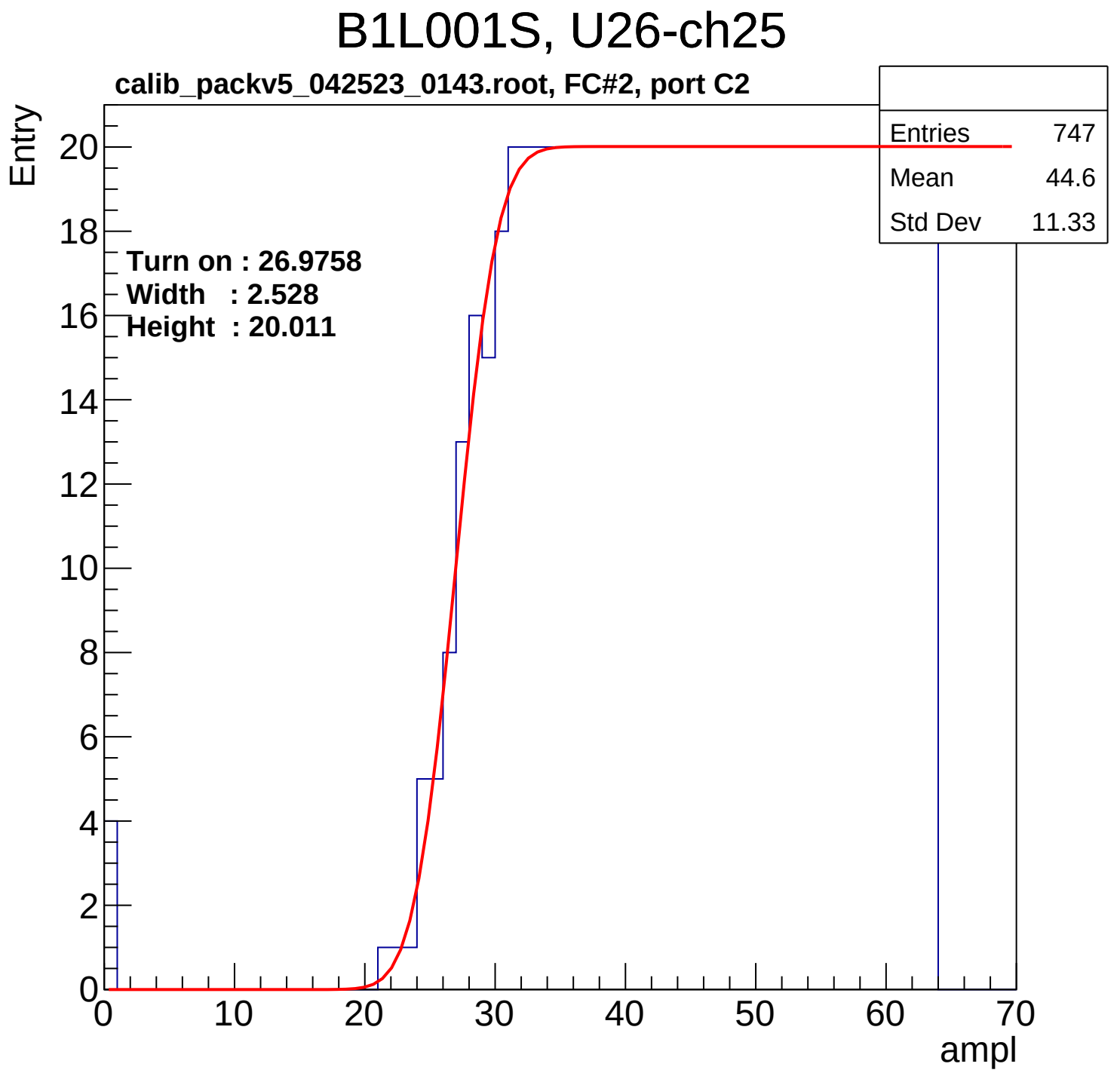

B1L001S, U26-ch20
calib_packv5_042523_0143.root, FC#2, port C2
Entries 769
Mean 44.02
Std Dev 11.66
Turn on : 26.1846
Width : 3.250
Height : 20.066
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

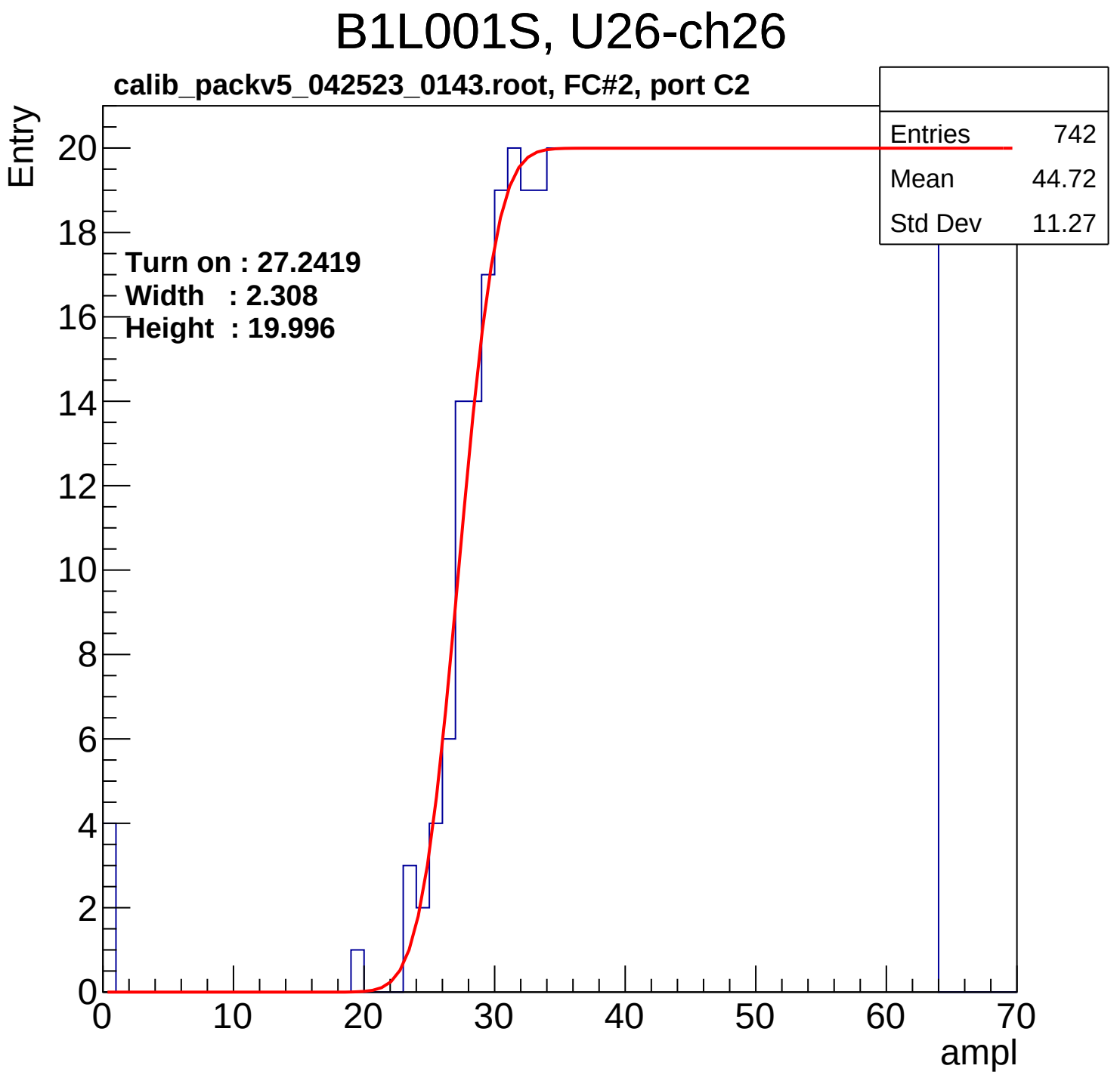

B1L001S, U26-ch21
calib_packv5_042523_0143.root, FC#2, port C2
Entries 743
Mean 44.78
Std Dev 11.05
Turn on : 27.3334
Width : 2.454
Height : 20.104
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

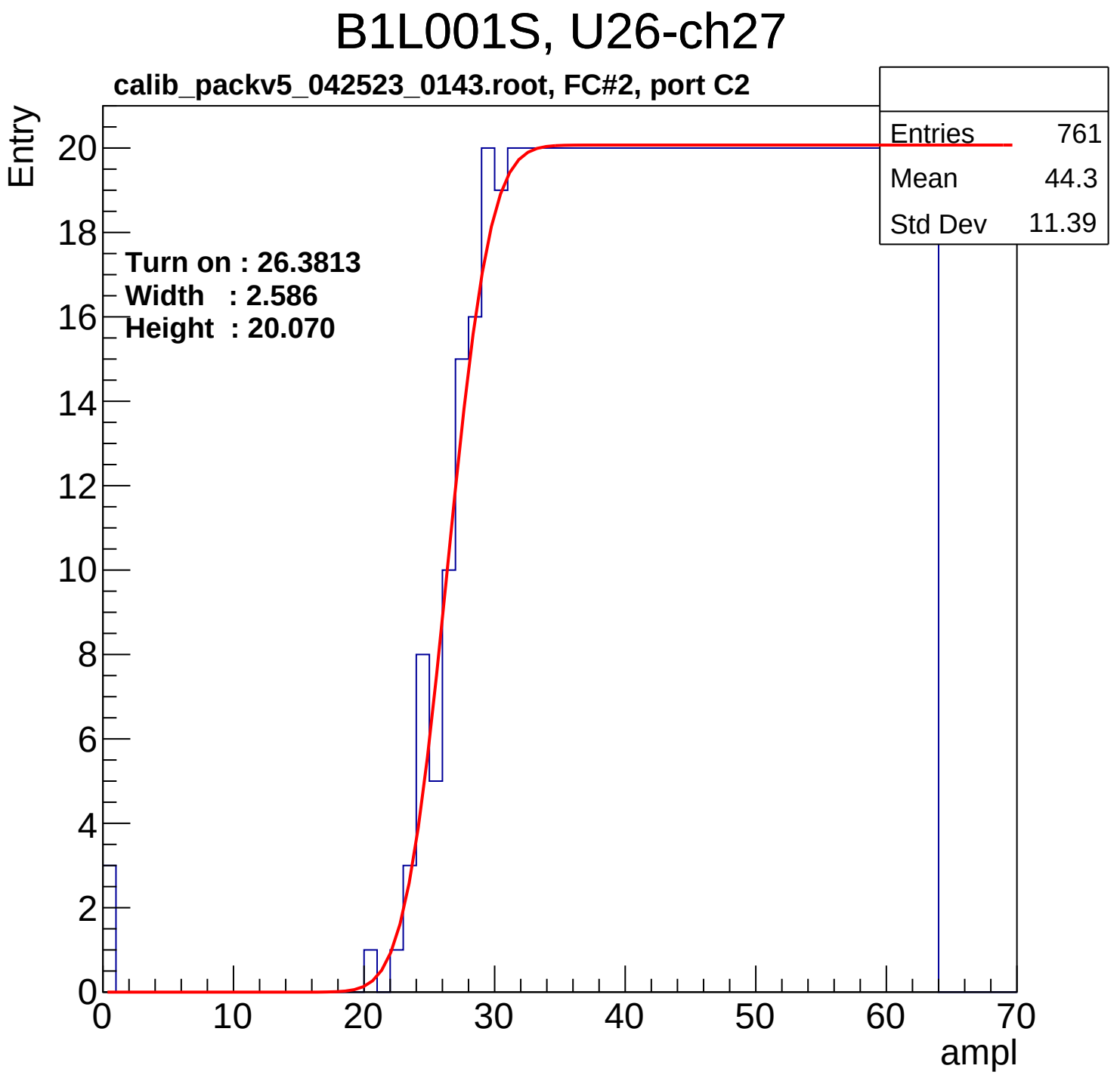

B1L001S, U26-ch22
calib_packv5_042523_0143.root, FC#2, port C2
Entries 729
Mean 45.03
Std Dev 11.12
Turn on : 28.0373
Width : 2.295
Height : 19.961
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

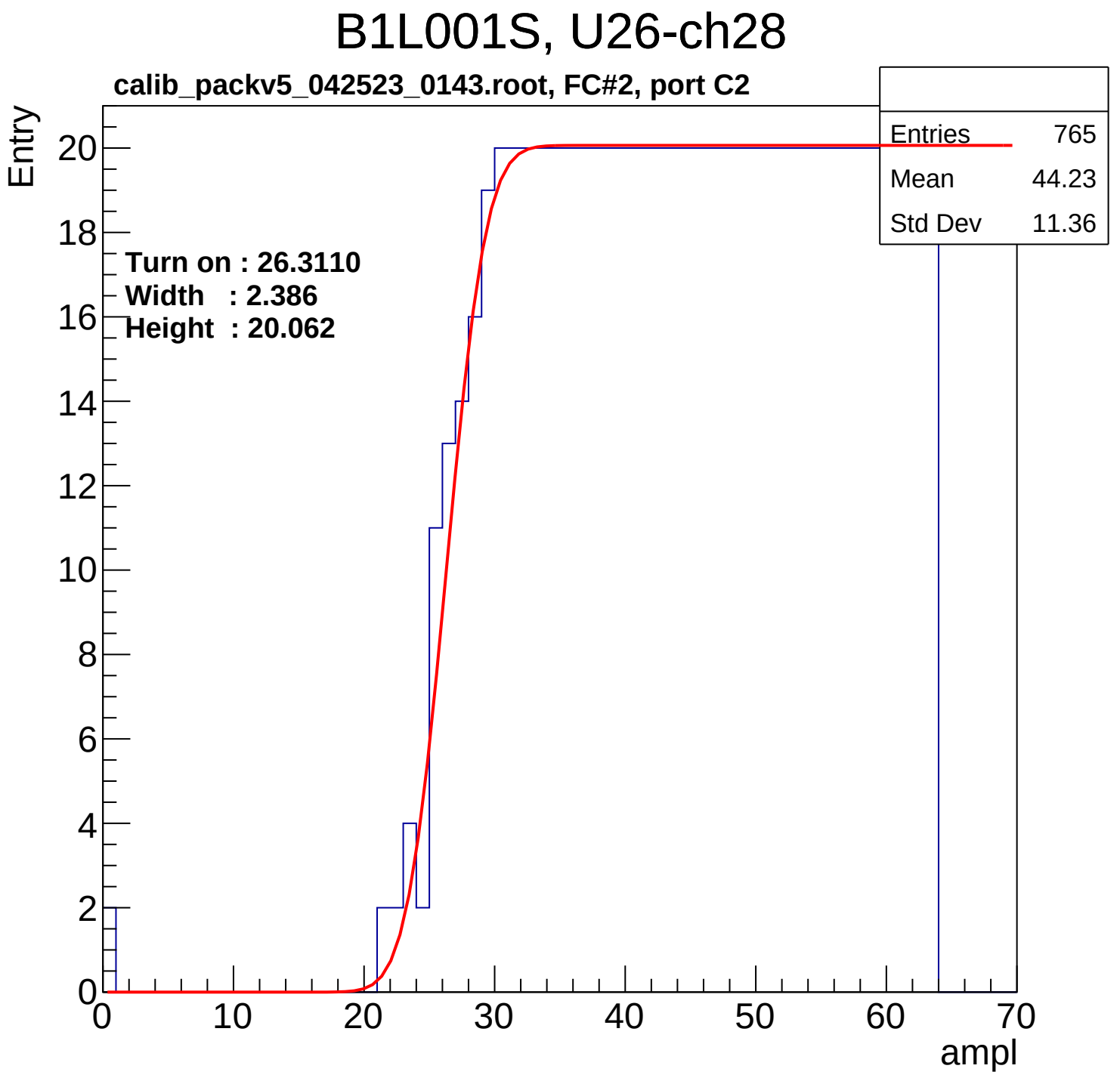

B1L001S, U26-ch23
calib_packv5_042523_0143.root, FC#2, port C2
Entries 752
Mean 44.47
Std Dev 11.4
Turn on : 26.8632
Width : 2.838
Height : 20.078
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

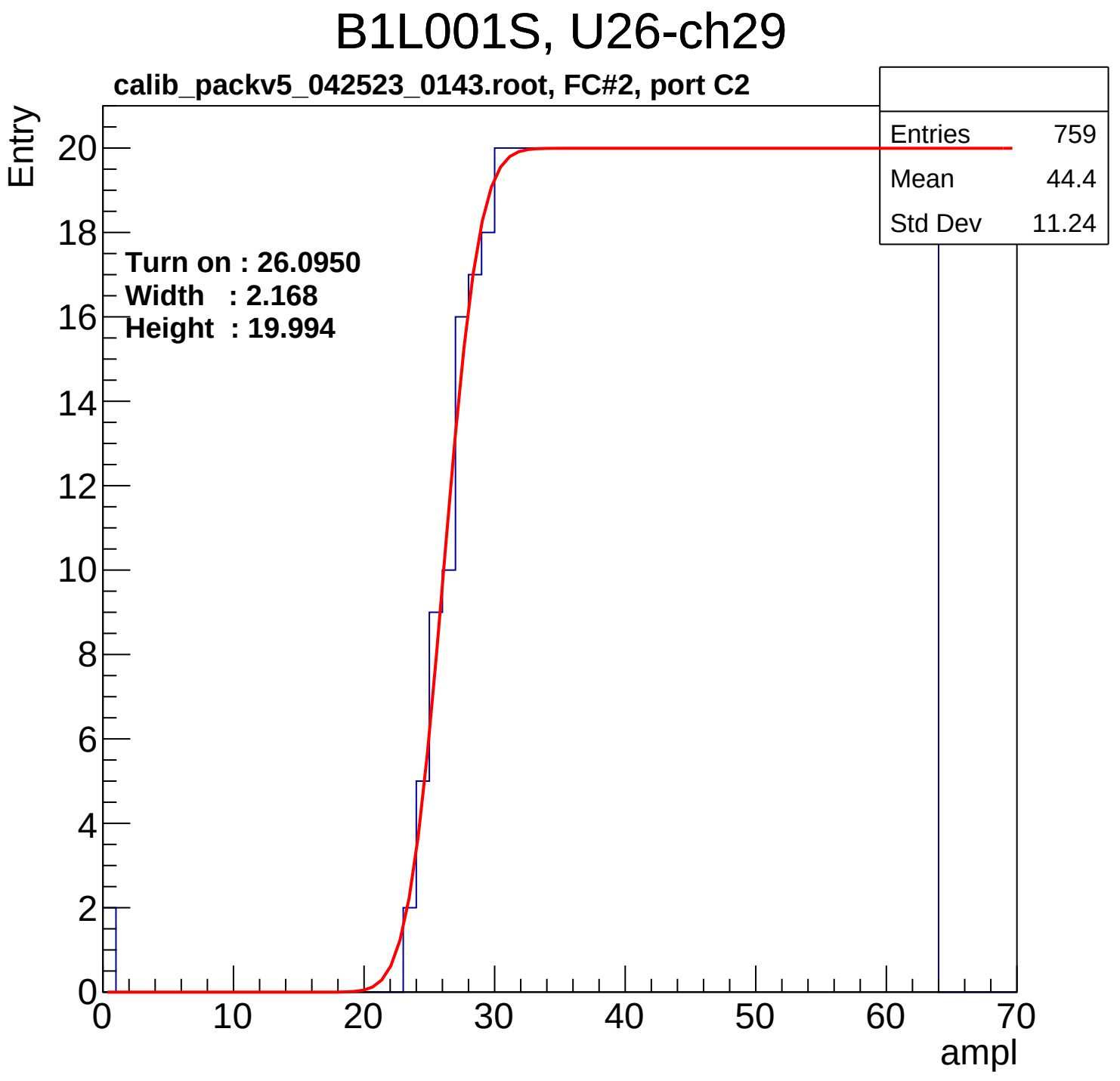

B1L001S, U26-ch24
calib_packv5_042523_0143.root, FC#2, port C2
Entries 772
Mean 44
Std Dev 11.59
Turn on : 26.0479
Width : 2.205
Height : 19.976
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

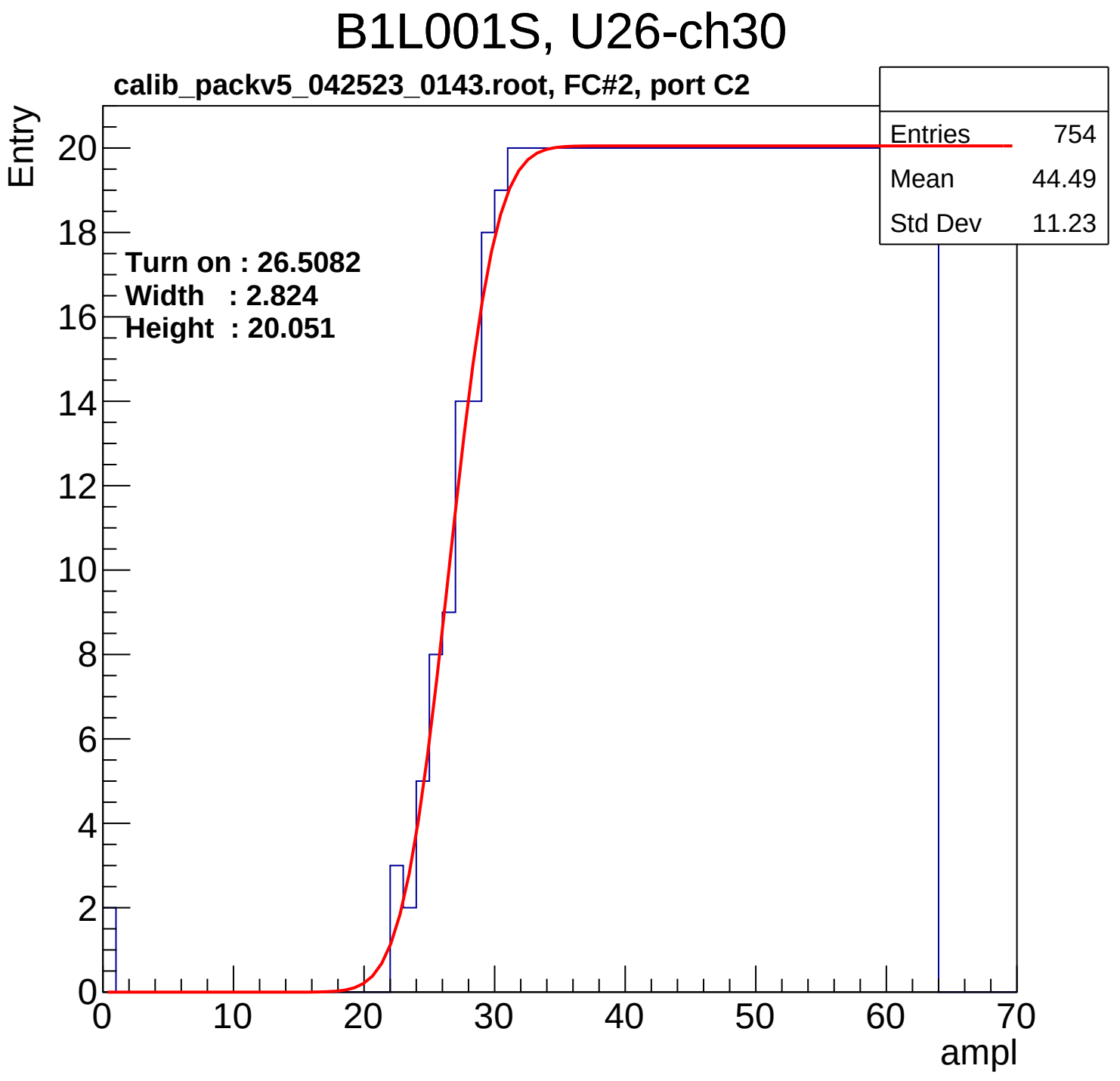

B1L001S, U26-ch25
calib_packv5_042523_0143.root, FC#2, port C2
Entries 747
Mean 44.6
Std Dev 11.33
Turn on : 26.9758
Width : 2.528
Height : 20.011
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

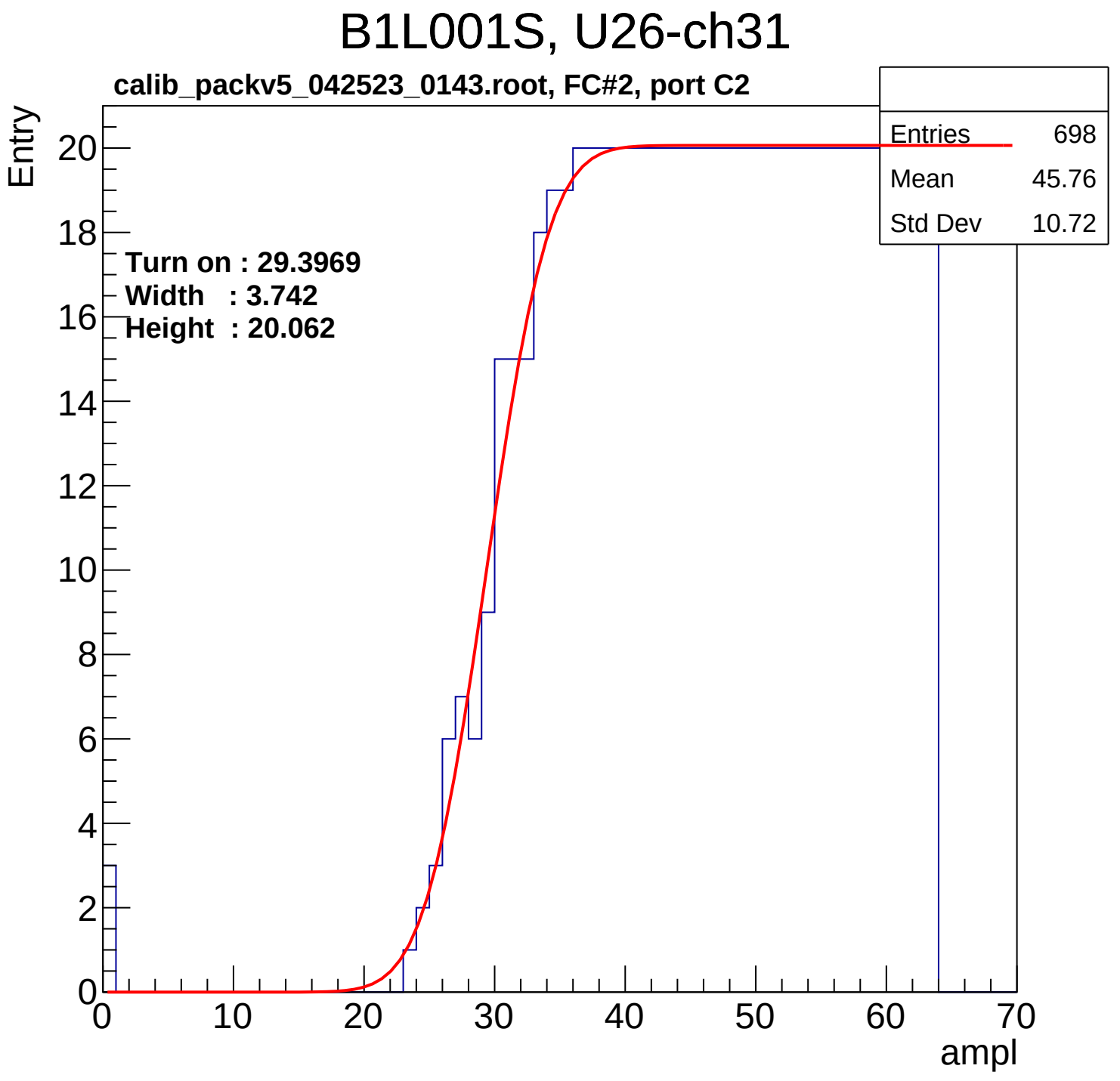

B1L001S, U26-ch26
calib_packv5_042523_0143.root, FC#2, port C2
Entries 742
Mean 44.72
Std Dev 11.27
Turn on : 27.2419
Width : 2.308
Height : 19.996
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

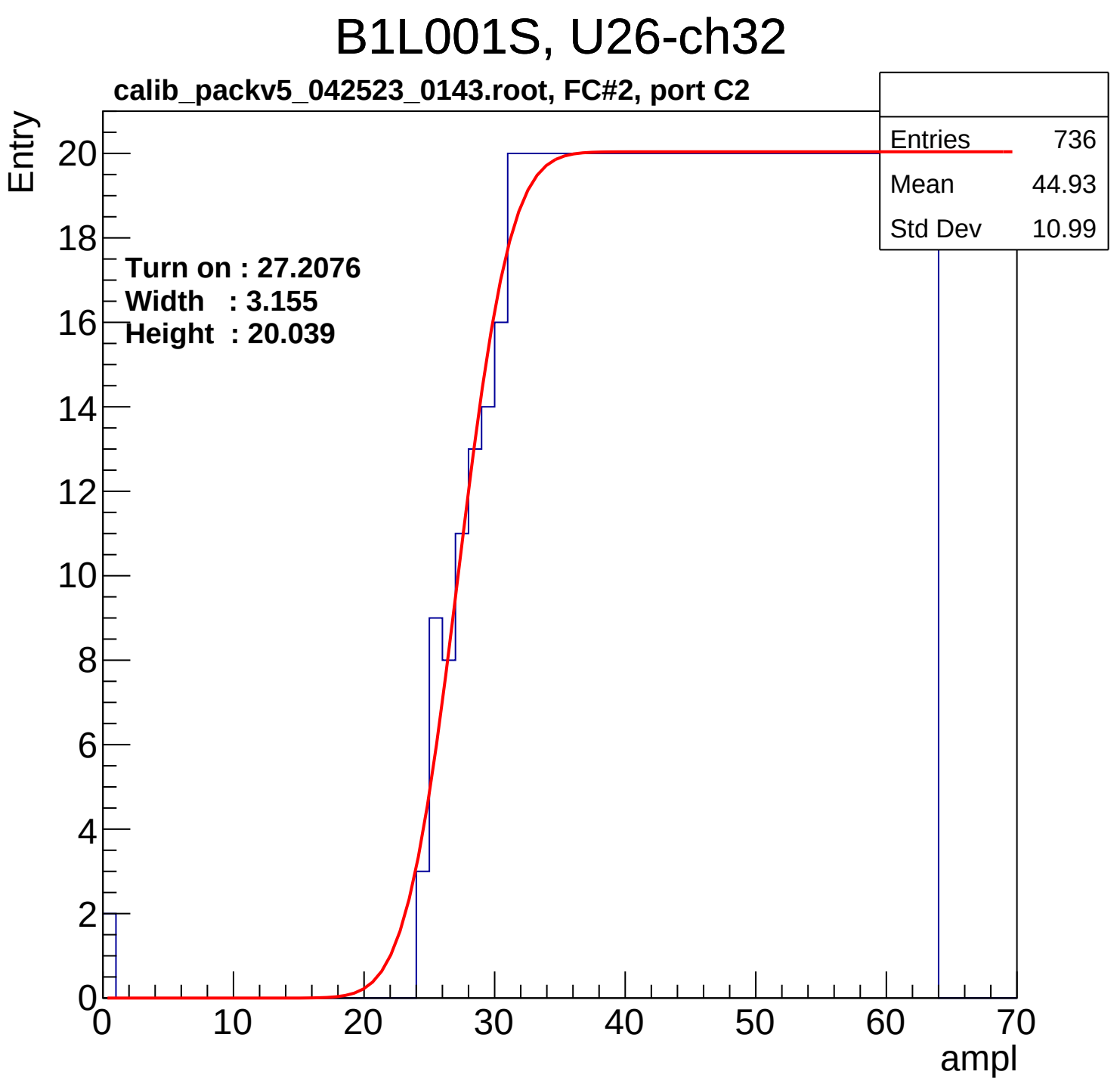

B1L001S, U26-ch27
calib_packv5_042523_0143.root, FC#2, port C2
Entries 761
Mean 44.3
Std Dev 11.39
Turn on : 26.3813
Width : 2.586
Height : 20.070
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

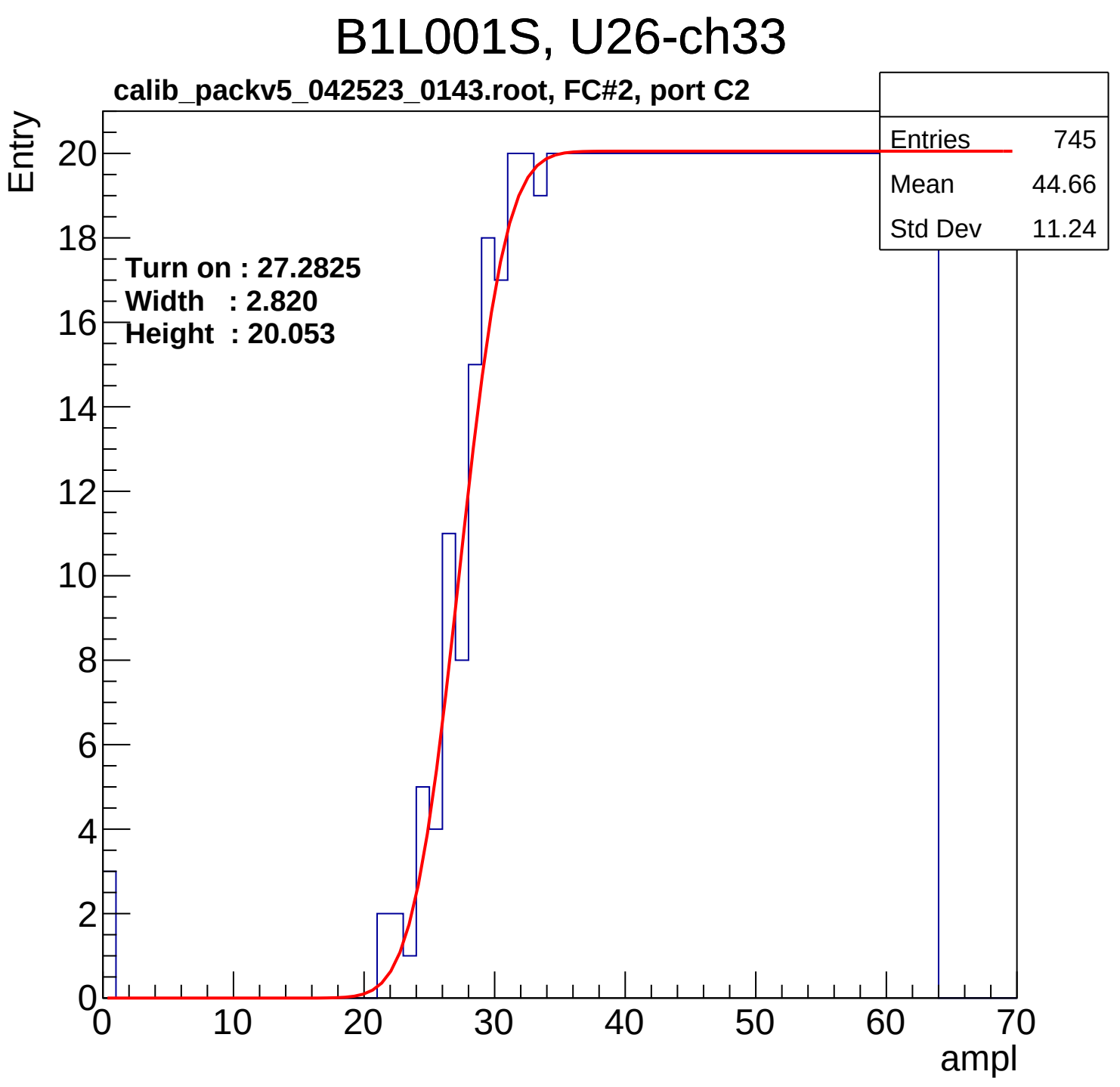

B1L001S, U26-ch28
calib_packv5_042523_0143.root, FC#2, port C2
Entries 765
Mean 44.23
Std Dev 11.36
Turn on : 26.3110
Width : 2.386
Height : 20.062
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

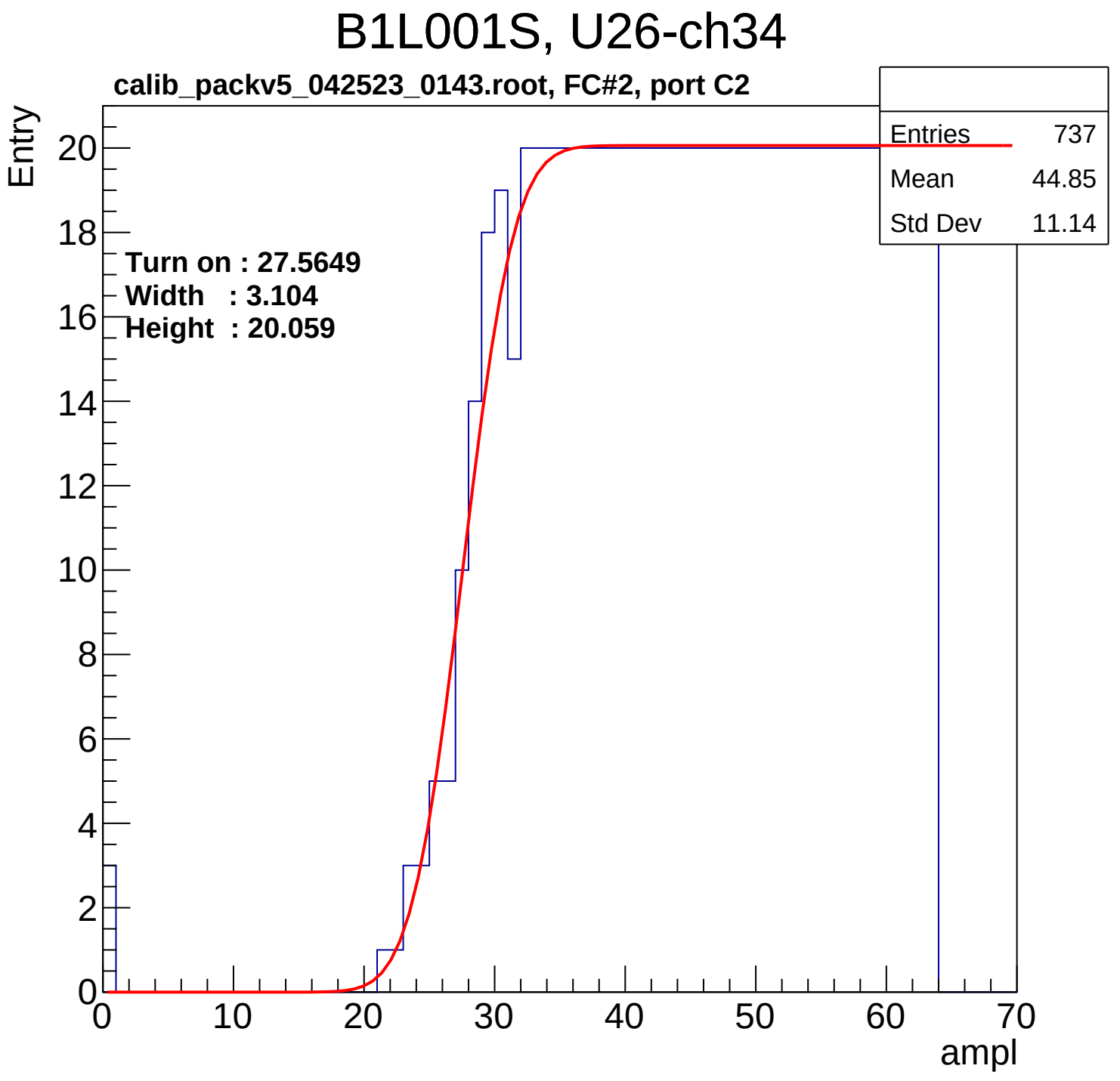

B1L001S, U26-ch29
calib_packv5_042523_0143.root, FC#2, port C2
Entries 759
Mean 44.4
Std Dev 11.24
Turn on : 26.0950
Width : 2.168
Height : 19.994
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

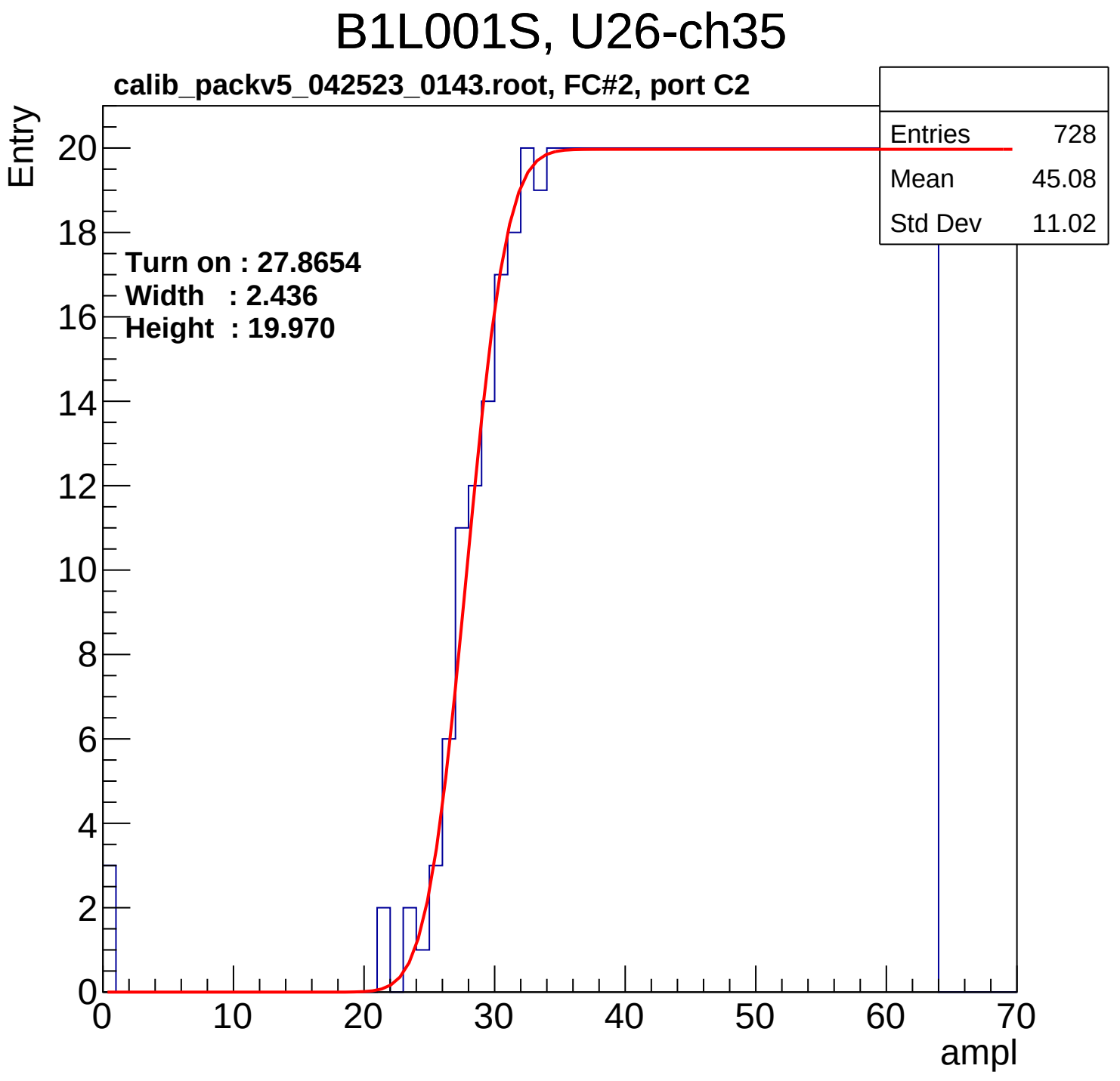

B1L001S, U26-ch30
calib_packv5_042523_0143.root, FC#2, port C2
Entries 754
Mean 44.49
Std Dev 11.23
Turn on : 26.5082
Width : 2.824
Height : 20.051
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

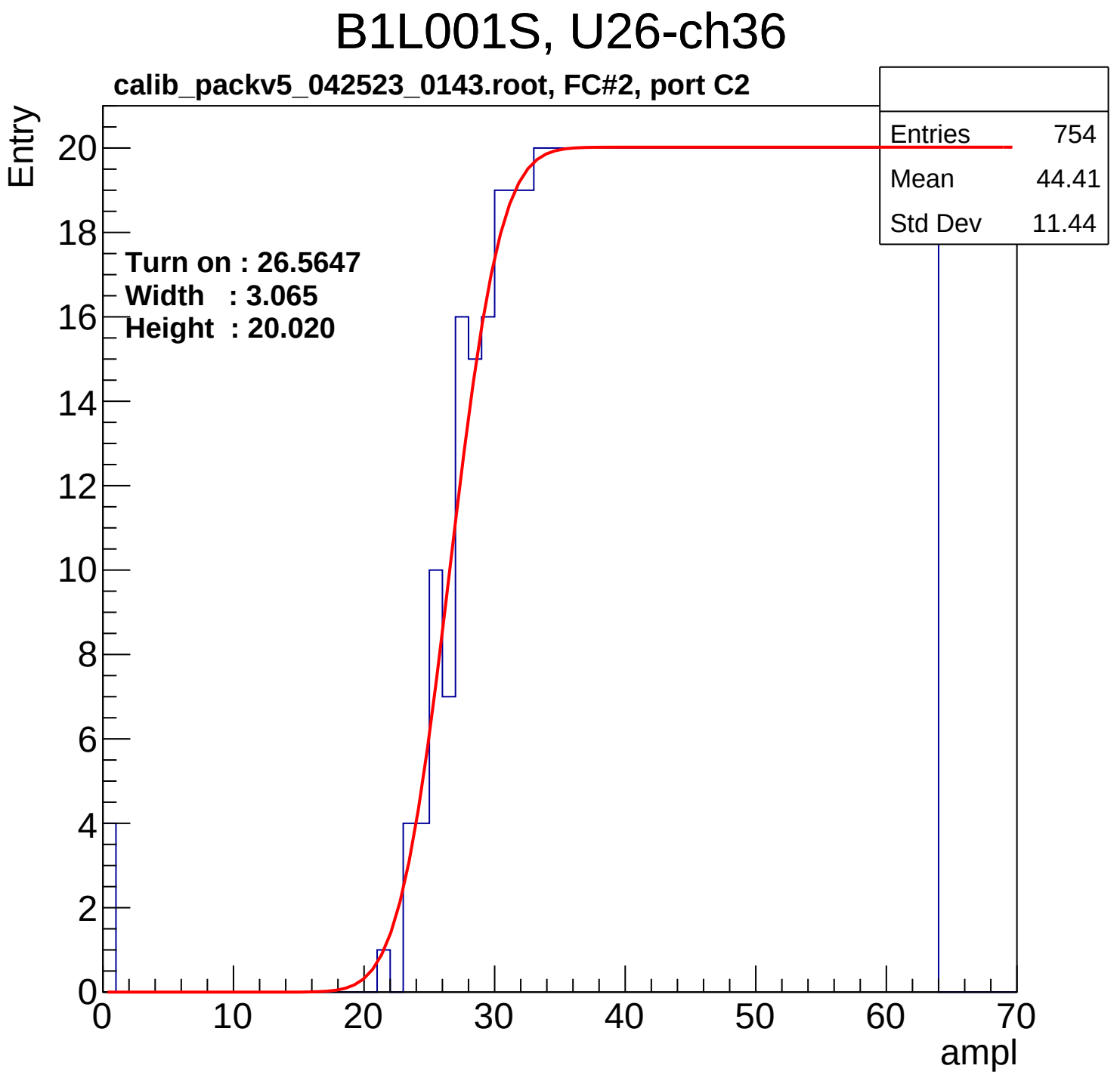

B1L001S, U26-ch31
calib_packv5_042523_0143.root, FC#2, port C2
Entries 698
Mean 45.76
Std Dev 10.72
Turn on : 29.3969
Width : 3.742
Height : 20.062
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

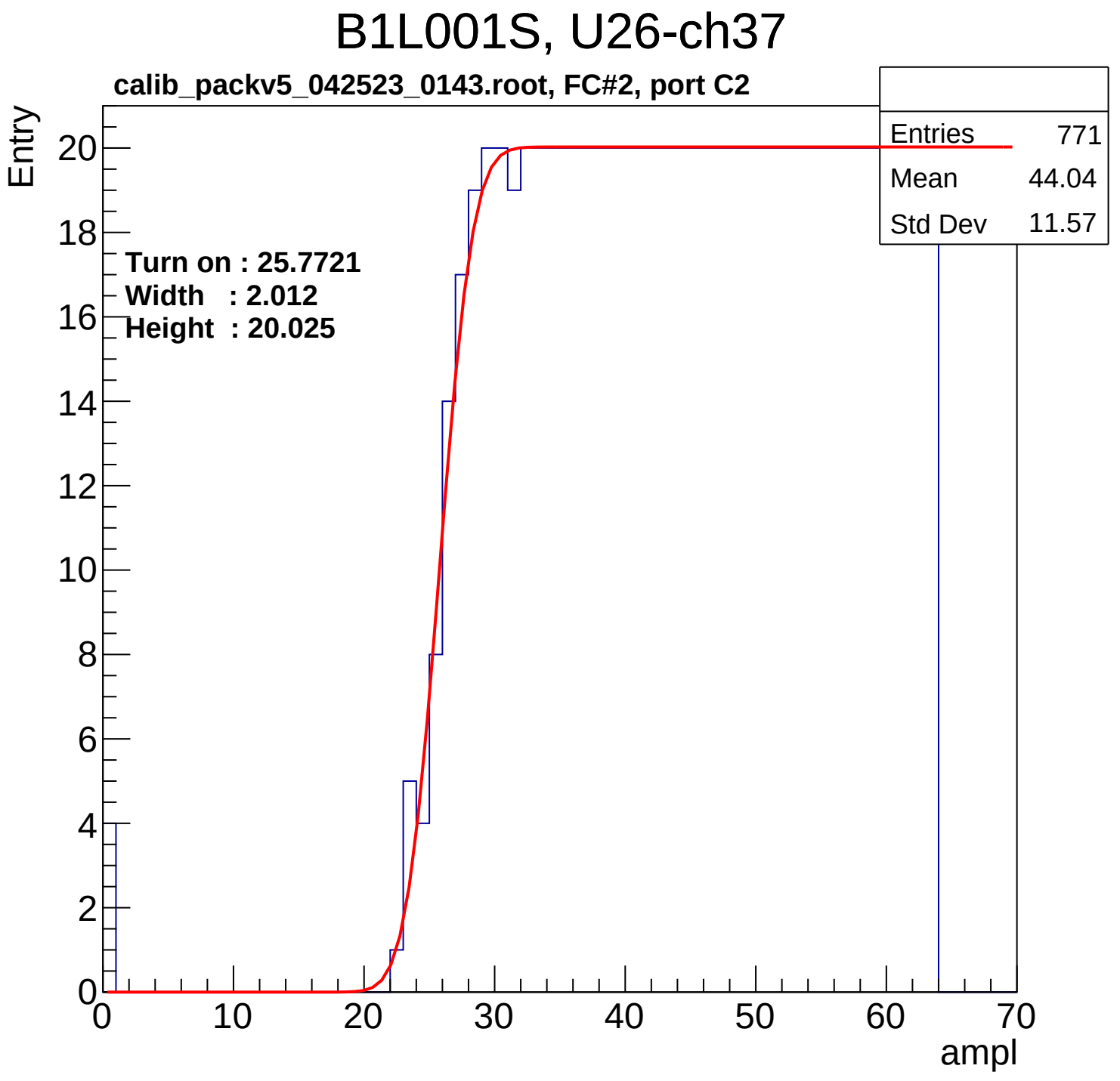

B1L001S, U26-ch32
calib_packv5_042523_0143.root, FC#2, port C2
Entries 736
Mean 44.93
Std Dev 10.99
Turn on : 27.2076
Width : 3.155
Height : 20.039
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

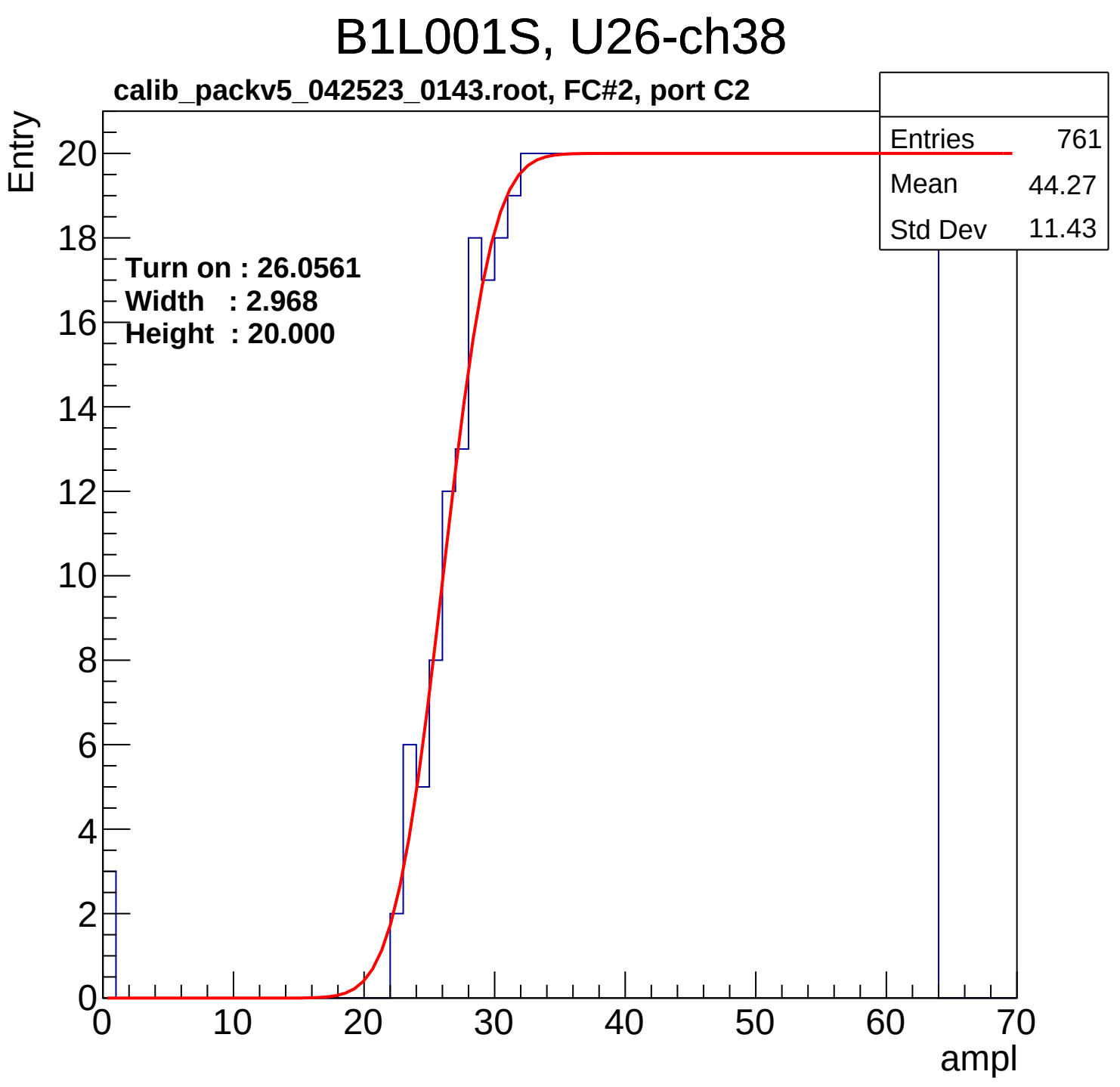

B1L001S, U26-ch33
calib_packv5_042523_0143.root, FC#2, port C2
Entries 745
Mean 44.66
Std Dev 11.24
Turn on : 27.2825
Width : 2.820
Height : 20.053
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

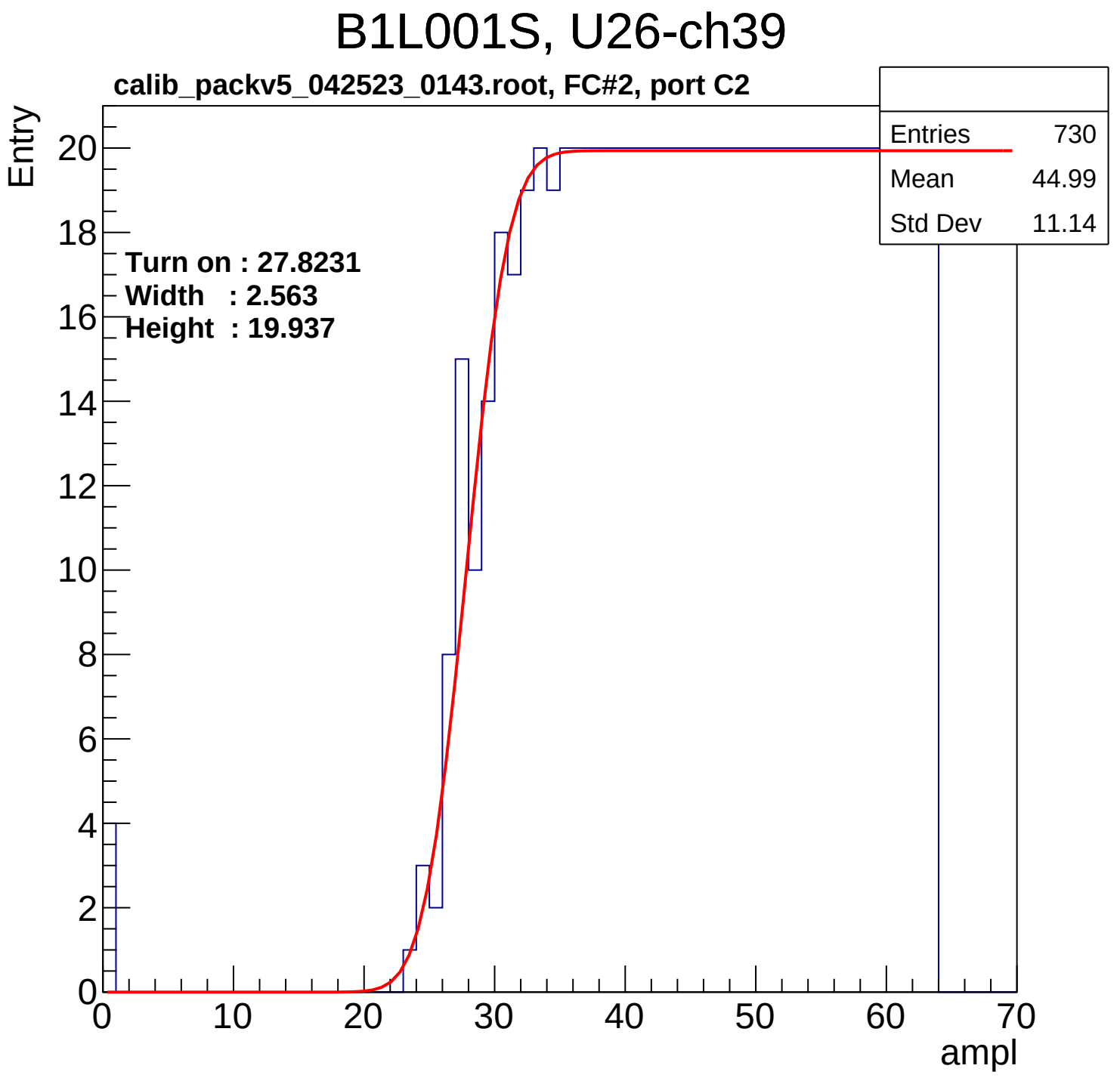

B1L001S, U26-ch34
calib_packv5_042523_0143.root, FC#2, port C2
Entries 737
Mean 44.85
Std Dev 11.14
Turn on : 27.5649
Width : 3.104
Height : 20.059
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

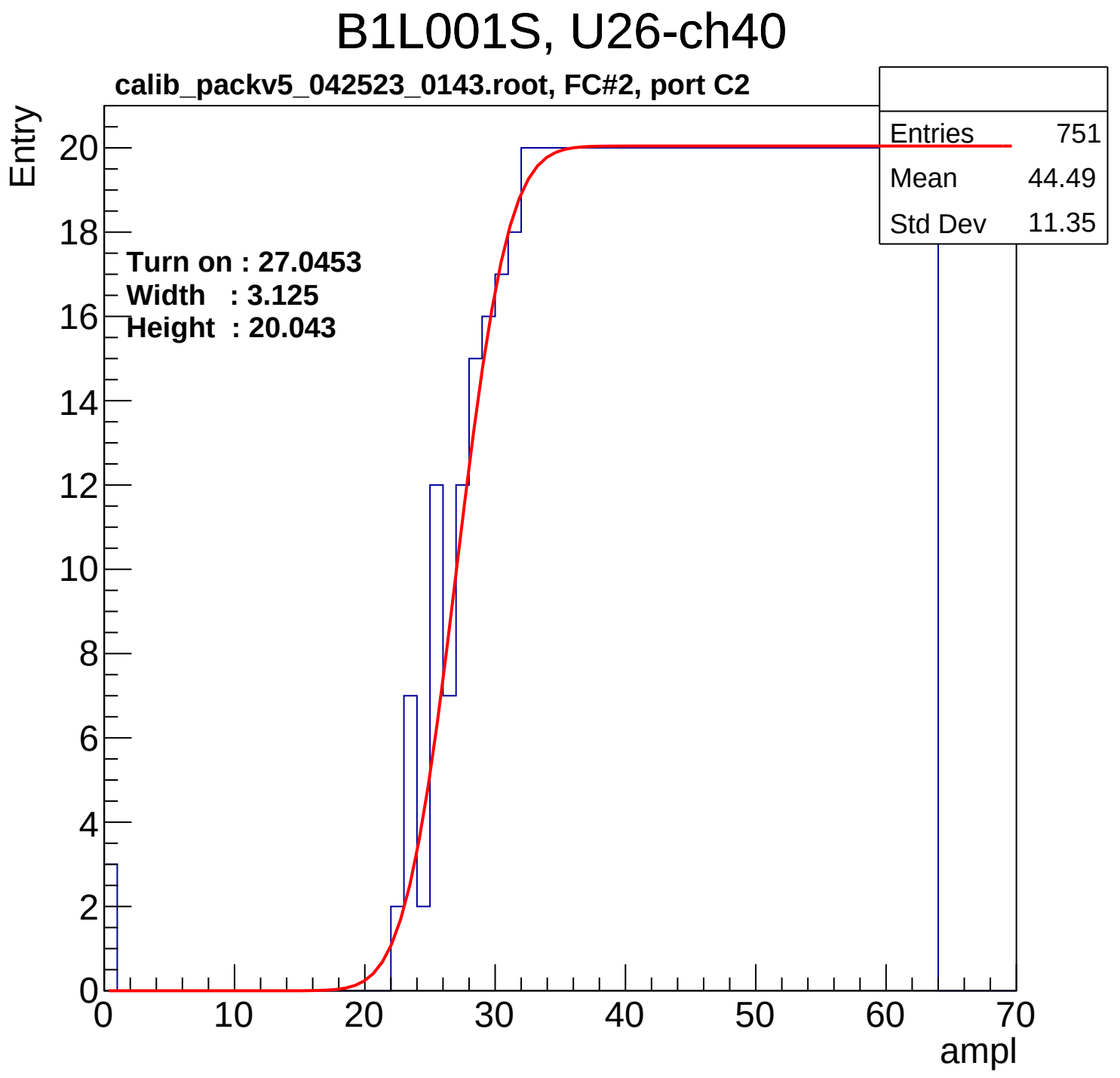

B1L001S, U26-ch35
calib_packv5_042523_0143.root, FC#2, port C2
Entries 728
Mean 45.08
Std Dev 11.02
Turn on : 27.8654
Width : 2.436
Height : 19.970
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

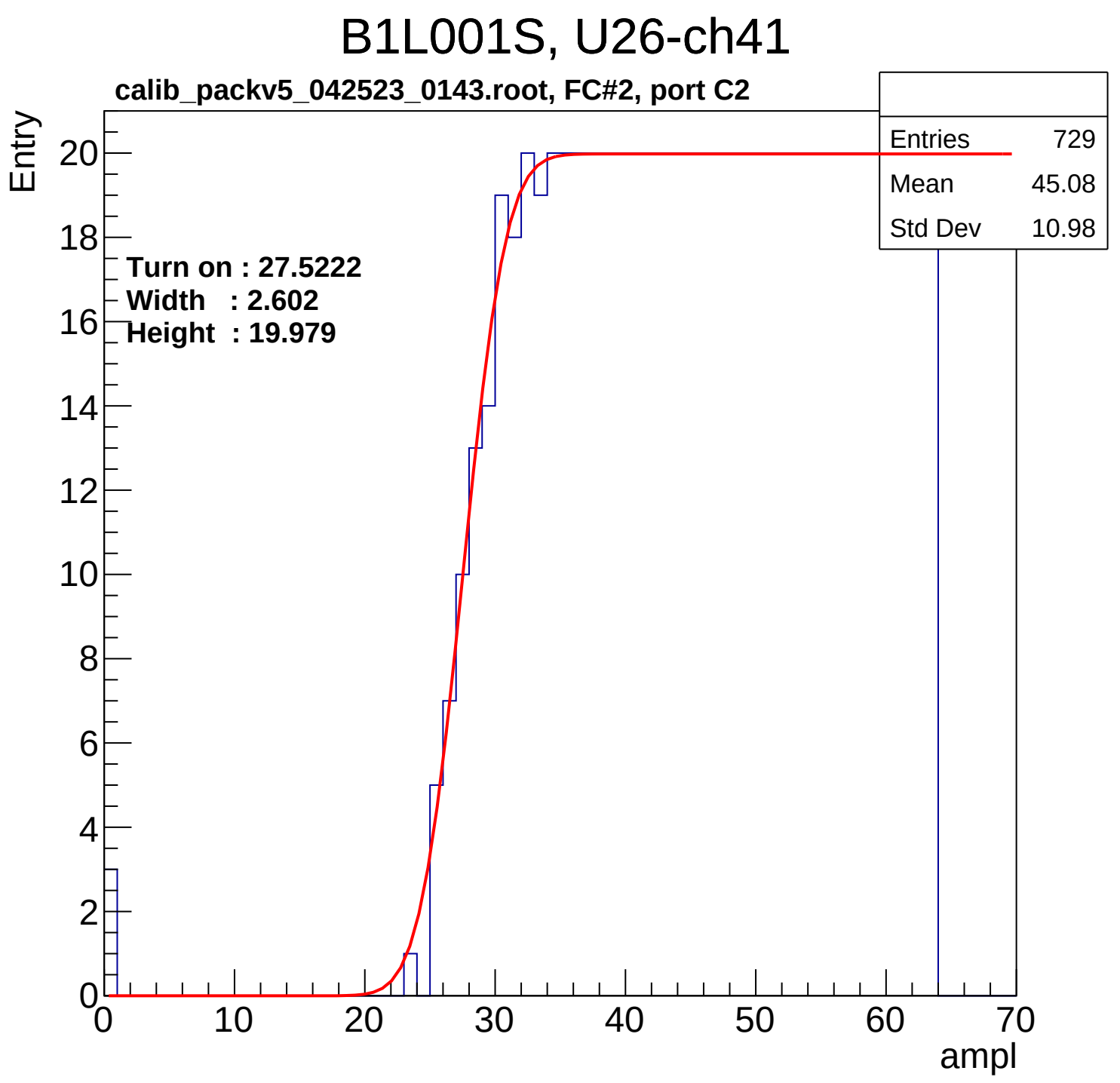

B1L001S, U26-ch36
calib_packv5_042523_0143.root, FC#2, port C2
Entries 754
Mean 44.41
Std Dev 11.44
Turn on : 26.5647
Width : 3.065
Height : 20.020
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

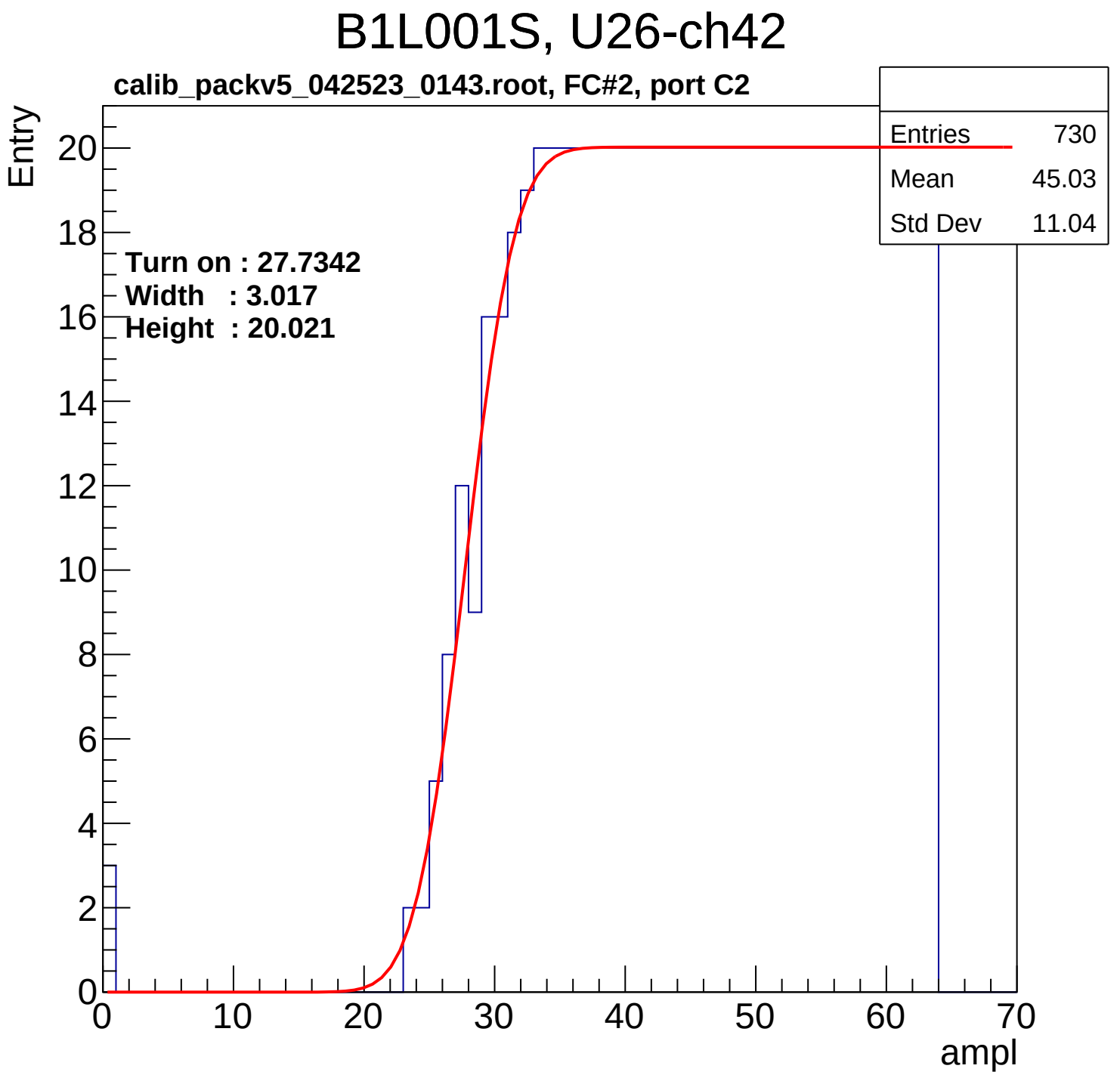

B1L001S, U26-ch37
calib_packv5_042523_0143.root, FC#2, port C2
Entries 771
Mean 44.04
Std Dev 11.57
Turn on : 25.7721
Width : 2.012
Height : 20.025
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

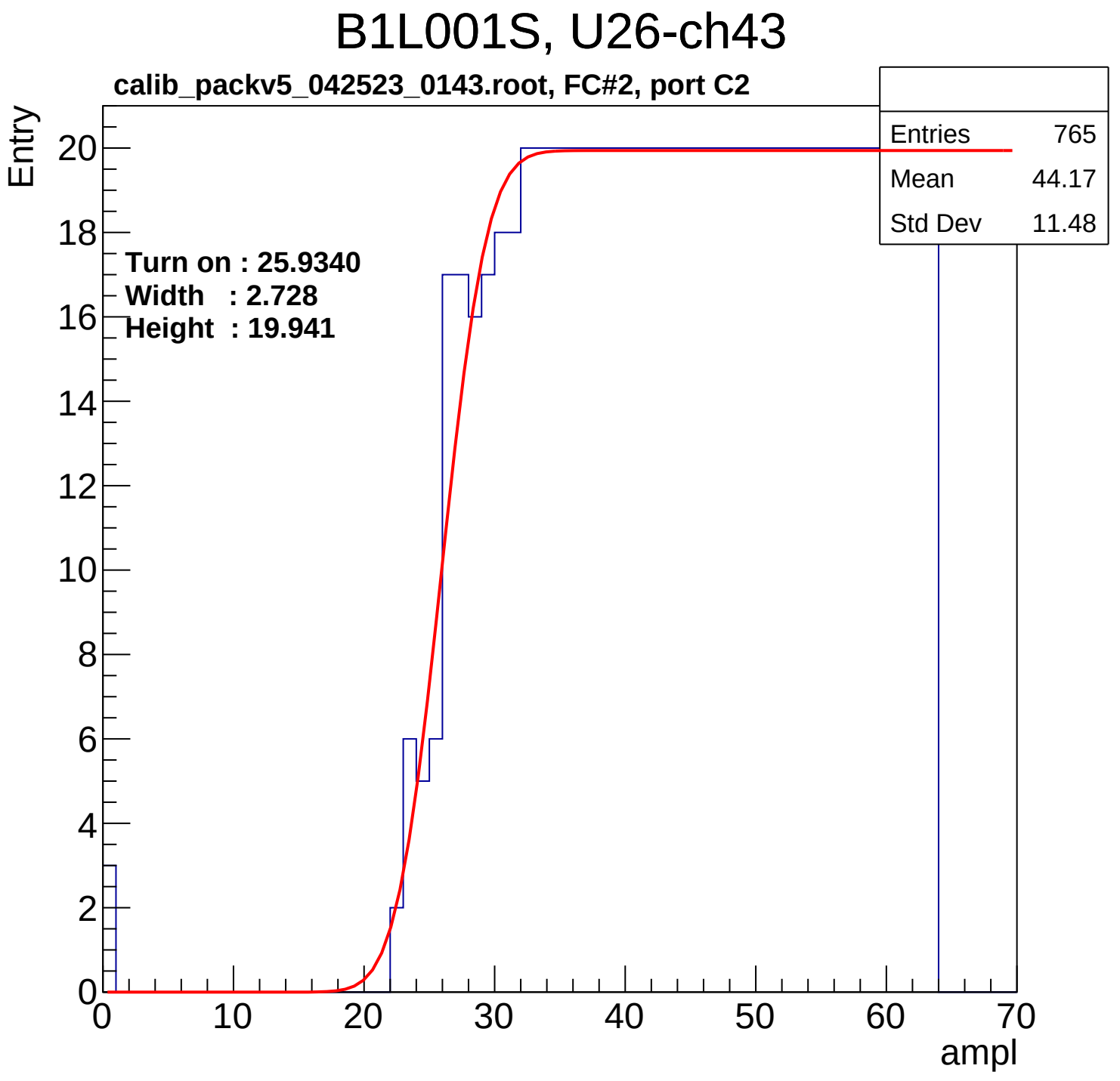

B1L001S, U26-ch38
calib_packv5_042523_0143.root, FC#2, port C2
Entries 761
Mean 44.27
Std Dev 11.43
Turn on : 26.0561
Width : 2.968
Height : 20.000
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

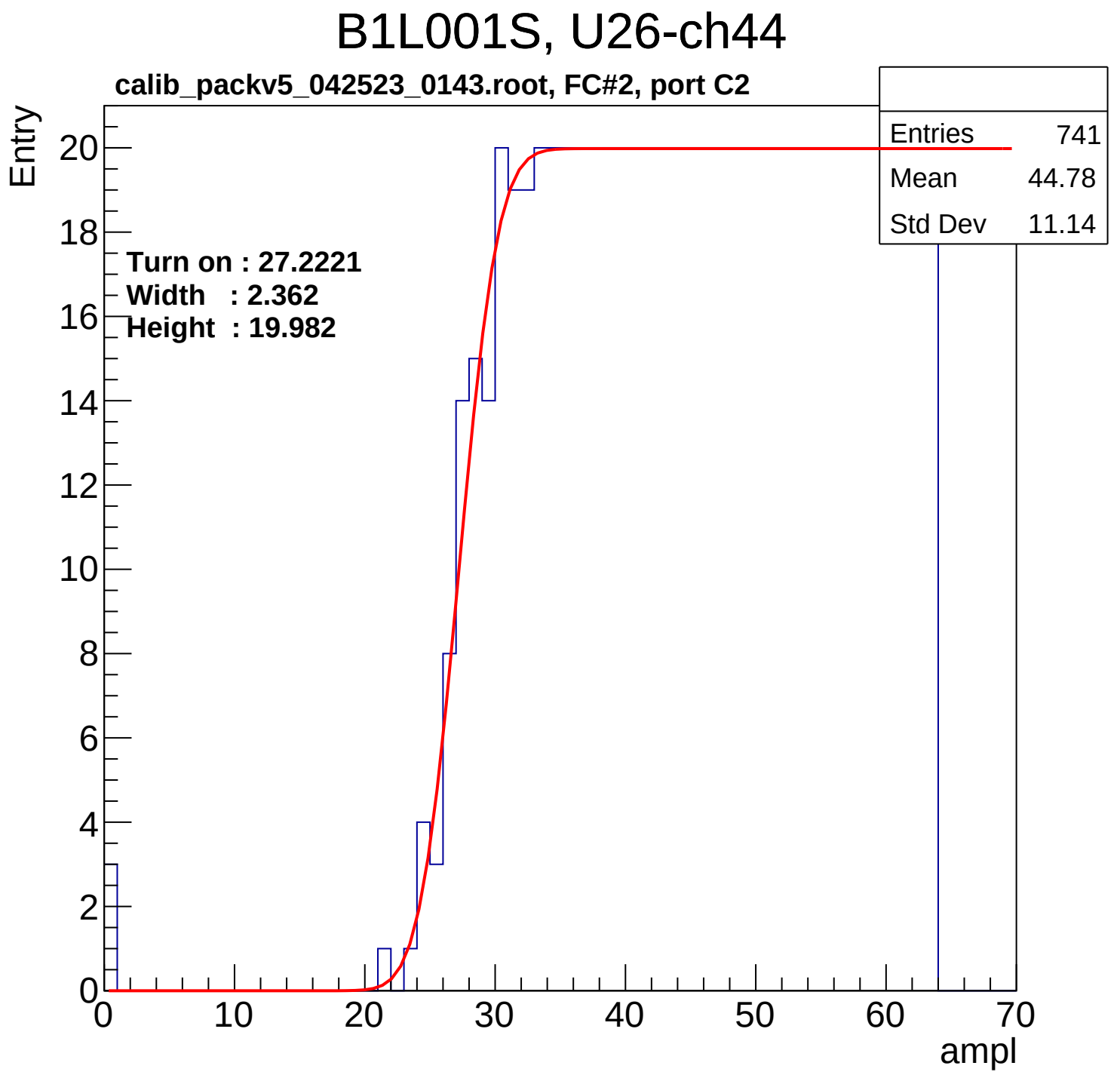

B1L001S, U26-ch39
calib_packv5_042523_0143.root, FC#2, port C2
Entries 730
Mean 44.99
Std Dev 11.14
Turn on : 27.8231
Width : 2.563
Height : 19.937
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

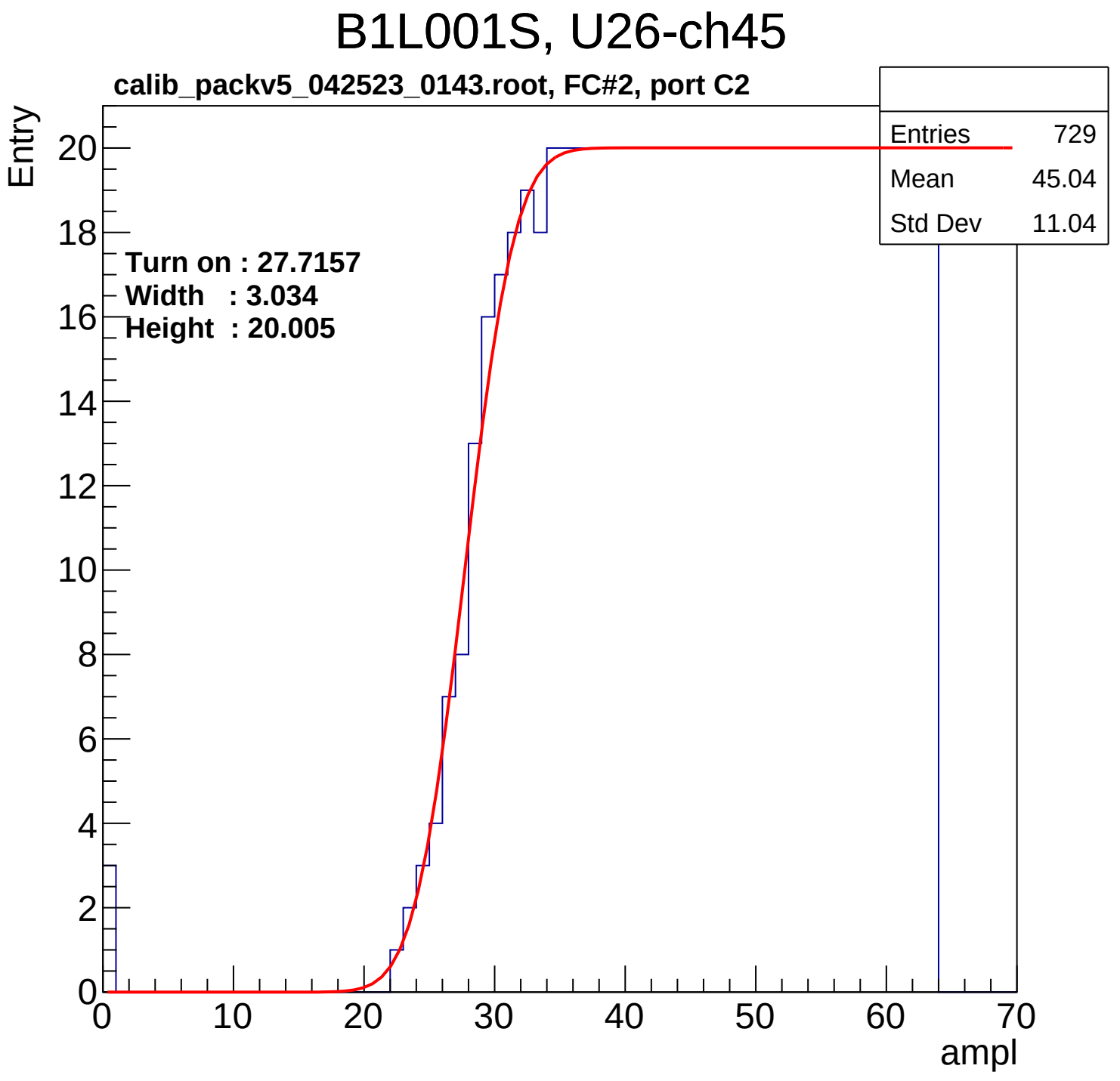

B1L001S, U26-ch40
calib_packv5_042523_0143.root, FC#2, port C2
Entries 751
Mean 44.49
Std Dev 11.35
Turn on : 27.0453
Width : 3.125
Height : 20.043
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

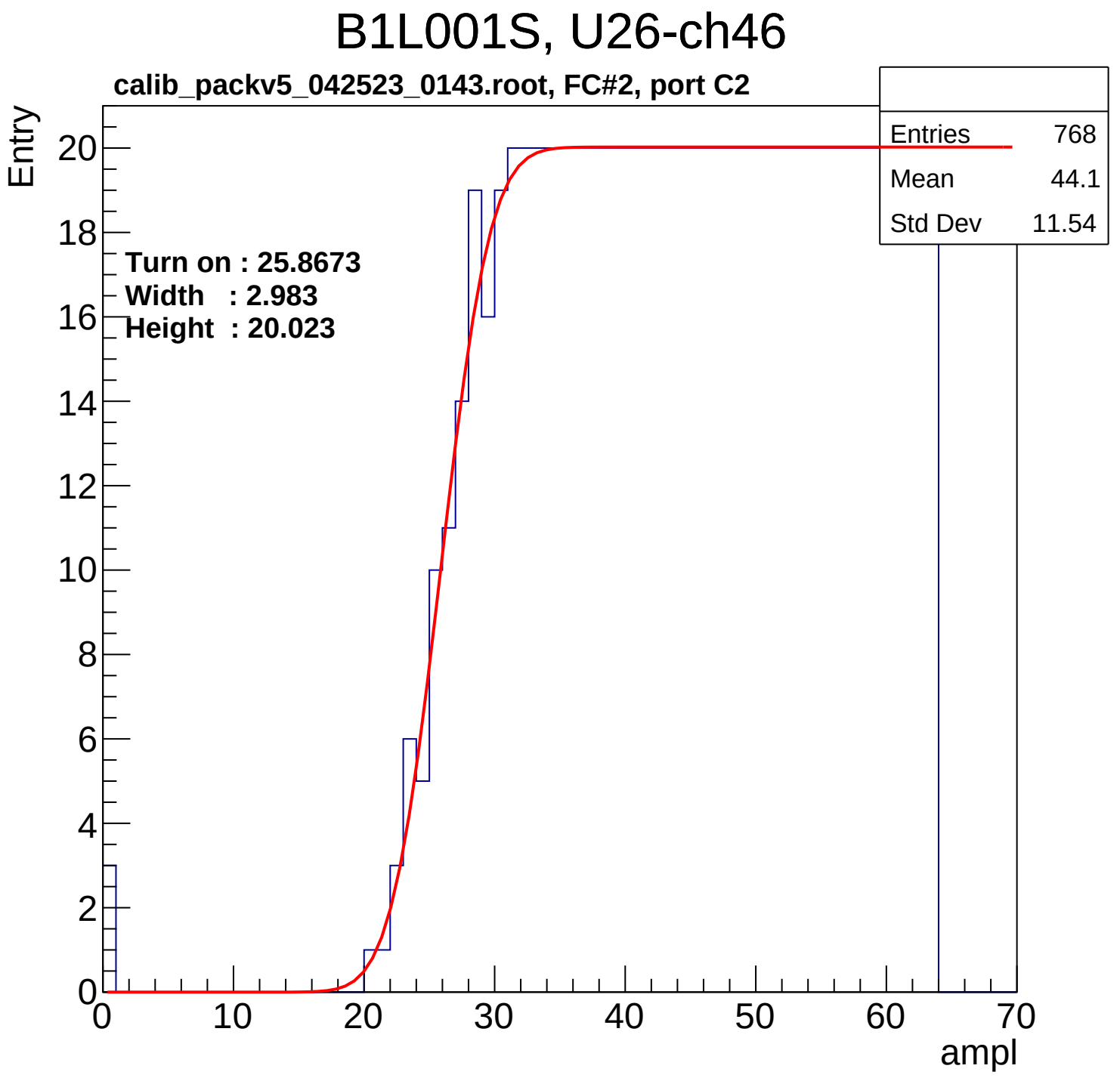

B1L001S, U26-ch41
calib_packv5_042523_0143.root, FC#2, port C2
Entries 729
Mean 45.08
Std Dev 10.98
Turn on : 27.5222
Width : 2.602
Height : 19.979
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

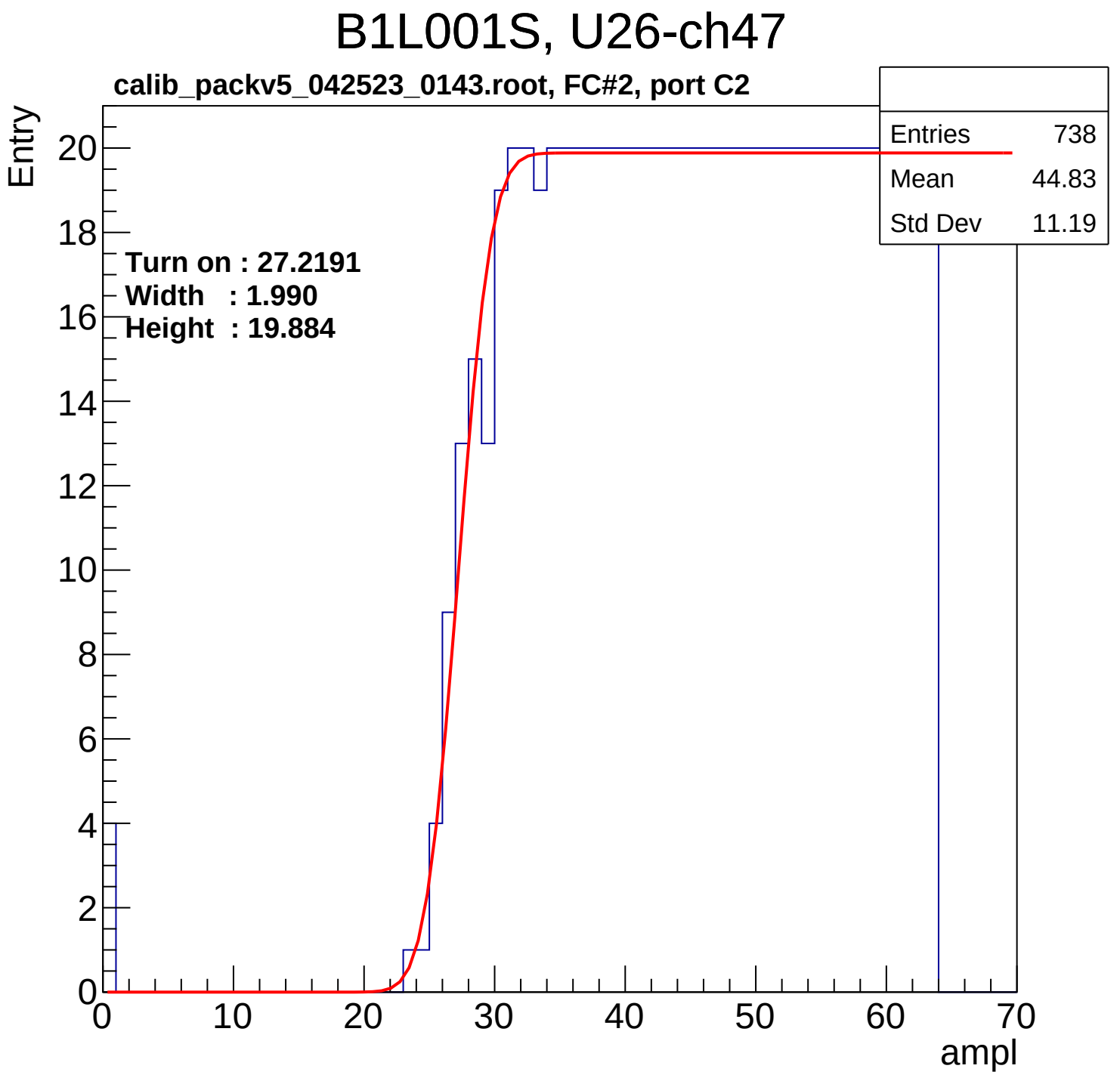

B1L001S, U26-ch42
calib_packv5_042523_0143.root, FC#2, port C2
Entries 730
Mean 45.03
Std Dev 11.04
Turn on : 27.7342
Width : 3.017
Height : 20.021
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

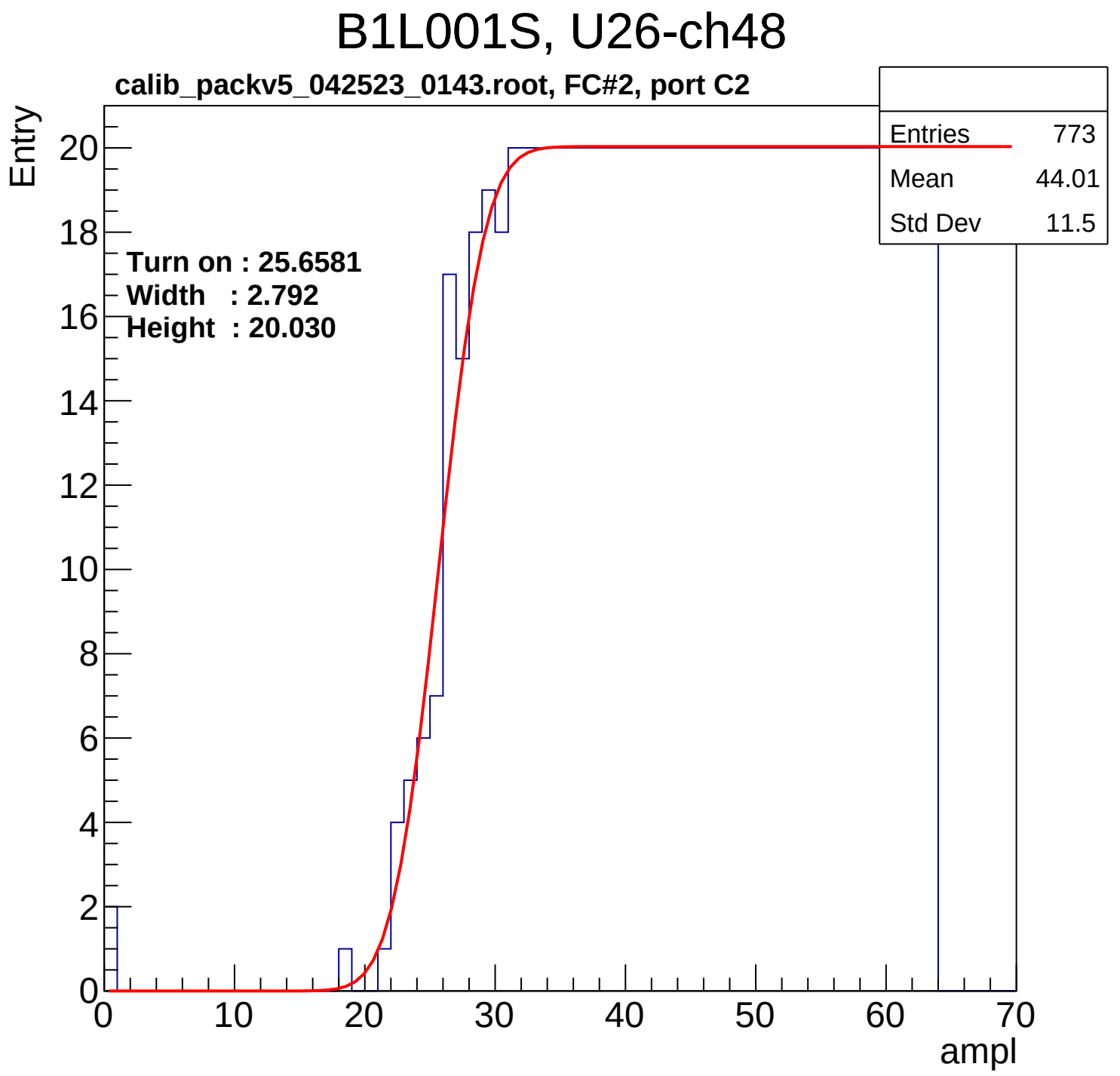

B1L001S, U26-ch43
calib_packv5_042523_0143.root, FC#2, port C2
Entries 765
Mean 44.17
Std Dev 11.48
Turn on : 25.9340
Width : 2.728
Height : 19.941
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

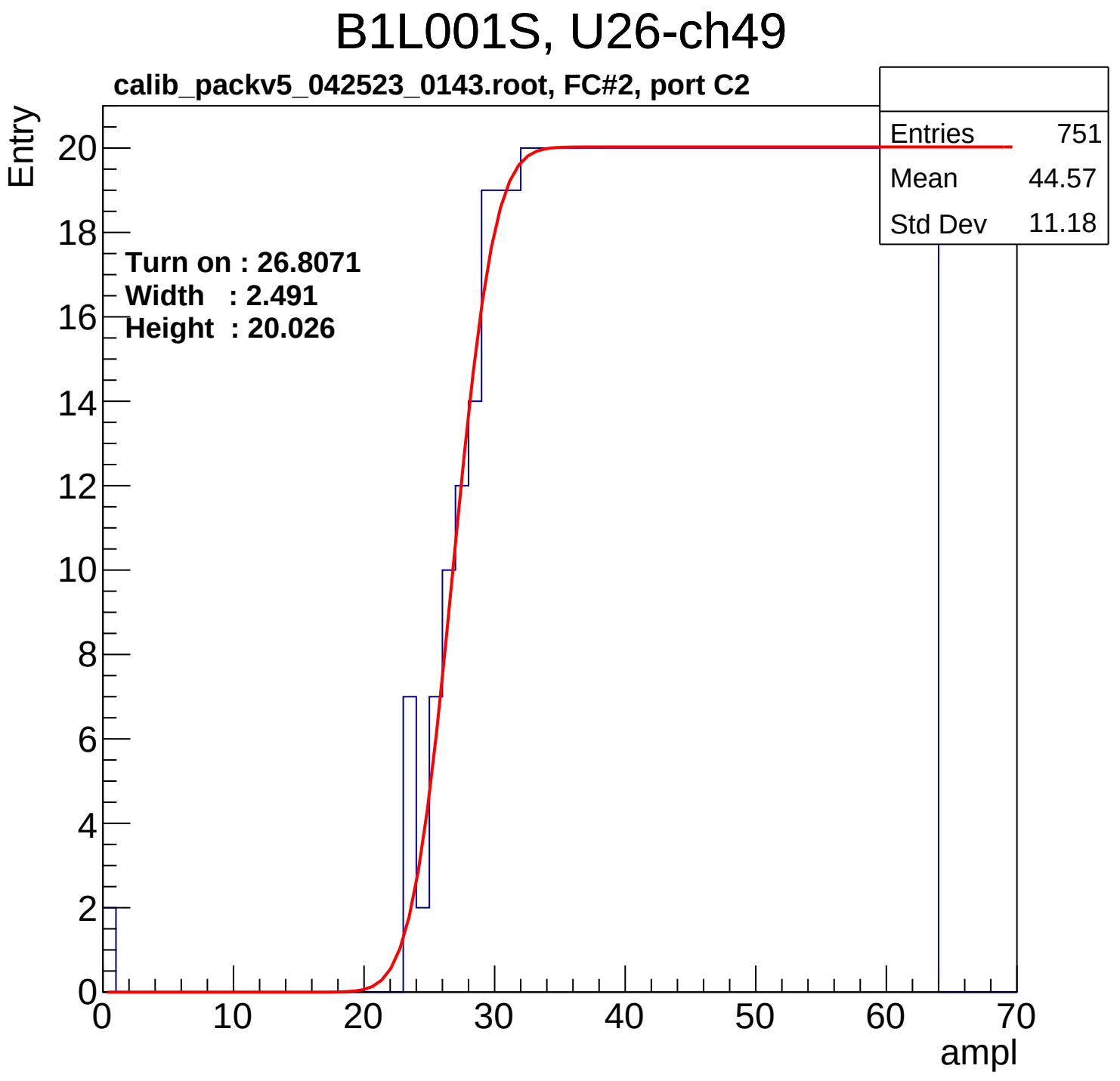

B1L001S, U26-ch44
calib_packv5_042523_0143.root, FC#2, port C2
Entries 741
Mean 44.78
Std Dev 11.14
Turn on : 27.2221
Width : 2.362
Height : 19.982
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

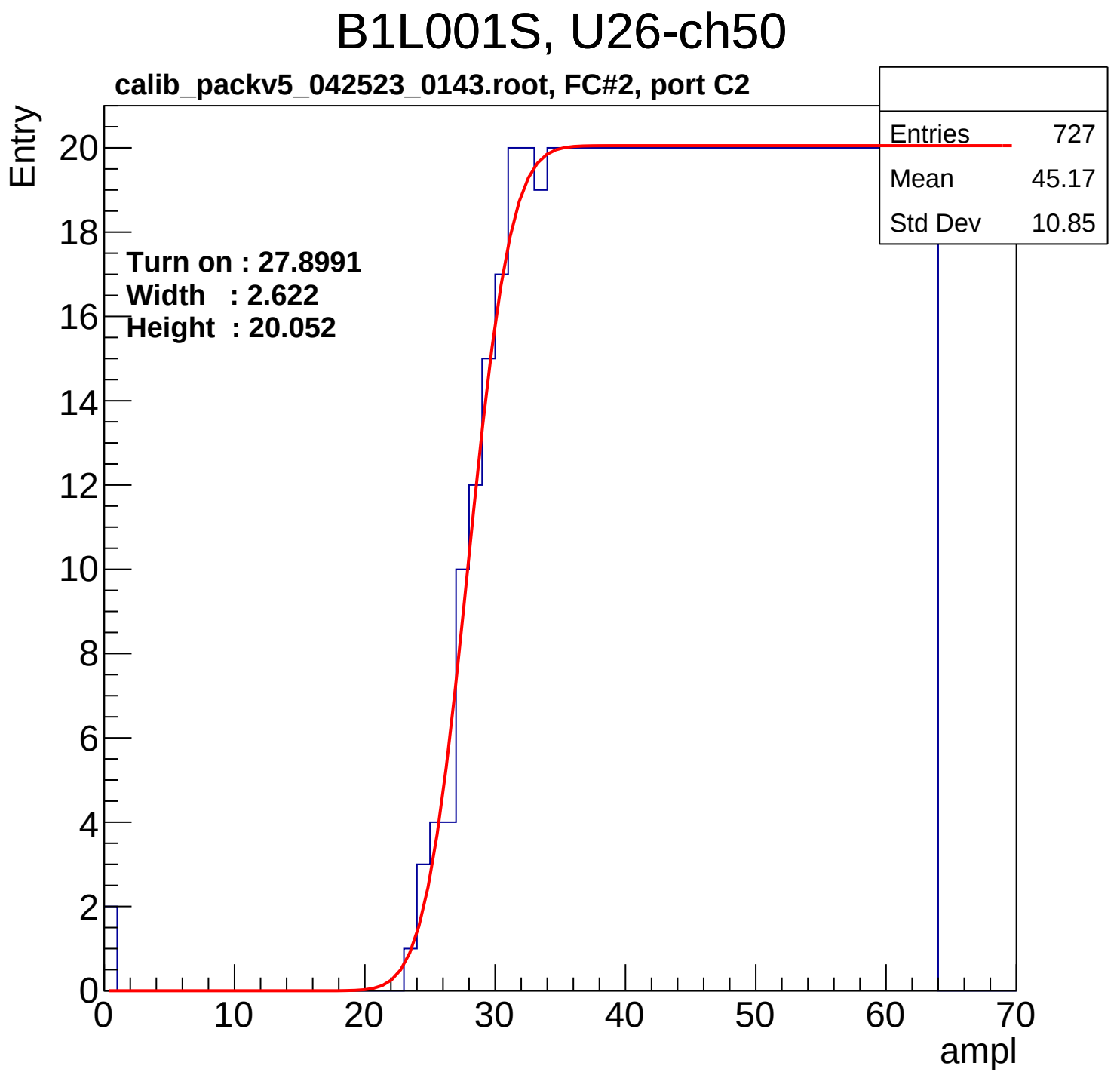

B1L001S, U26-ch45
calib_packv5_042523_0143.root, FC#2, port C2
Entries 729
Mean 45.04
Std Dev 11.04
Turn on : 27.7157
Width : 3.034
Height : 20.005
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

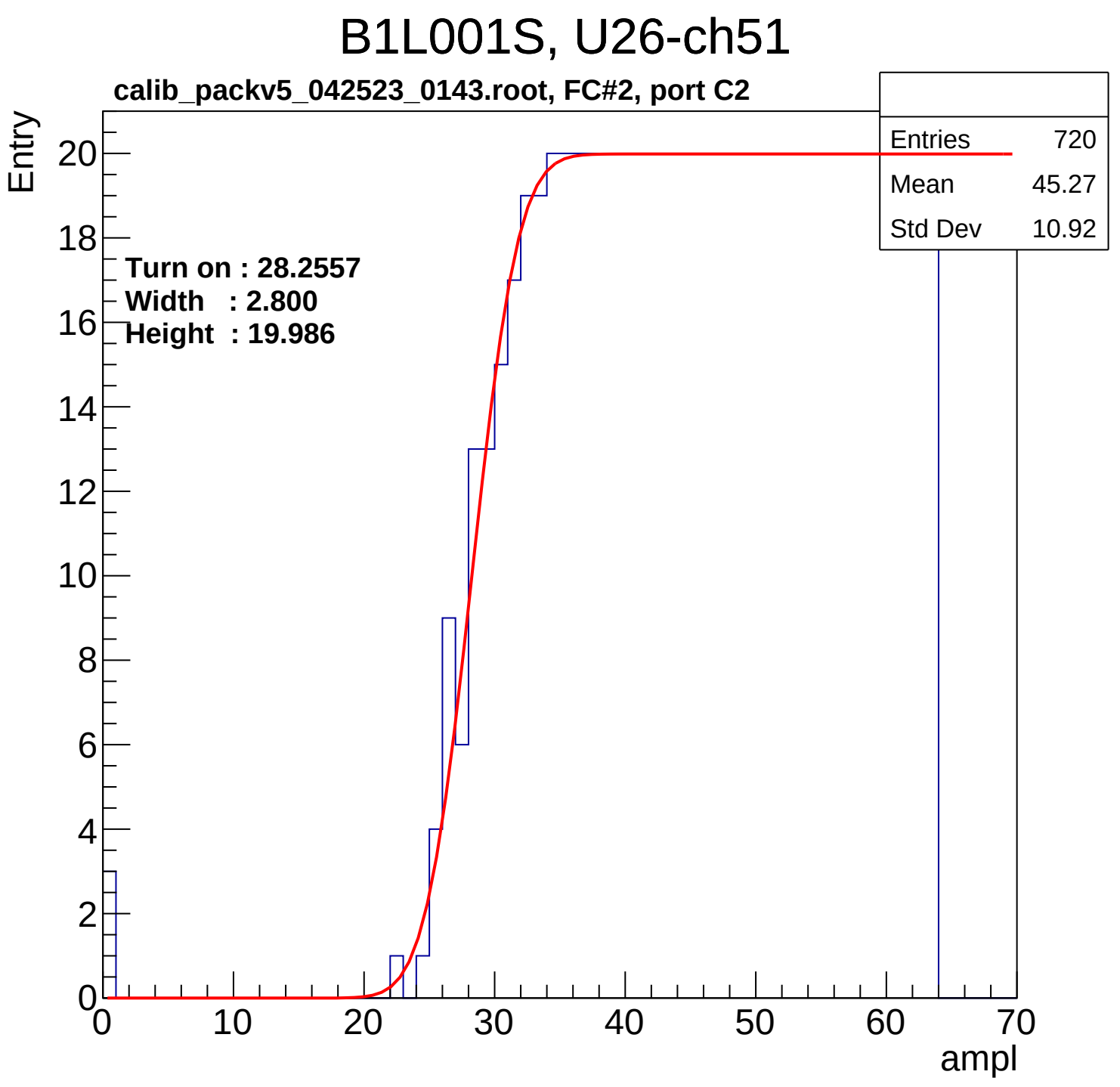

B1L001S, U26-ch46
calib_packv5_042523_0143.root, FC#2, port C2
Entries 768
Mean 44.1
Std Dev 11.54
Turn on : 25.8673
Width : 2.983
Height : 20.023
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

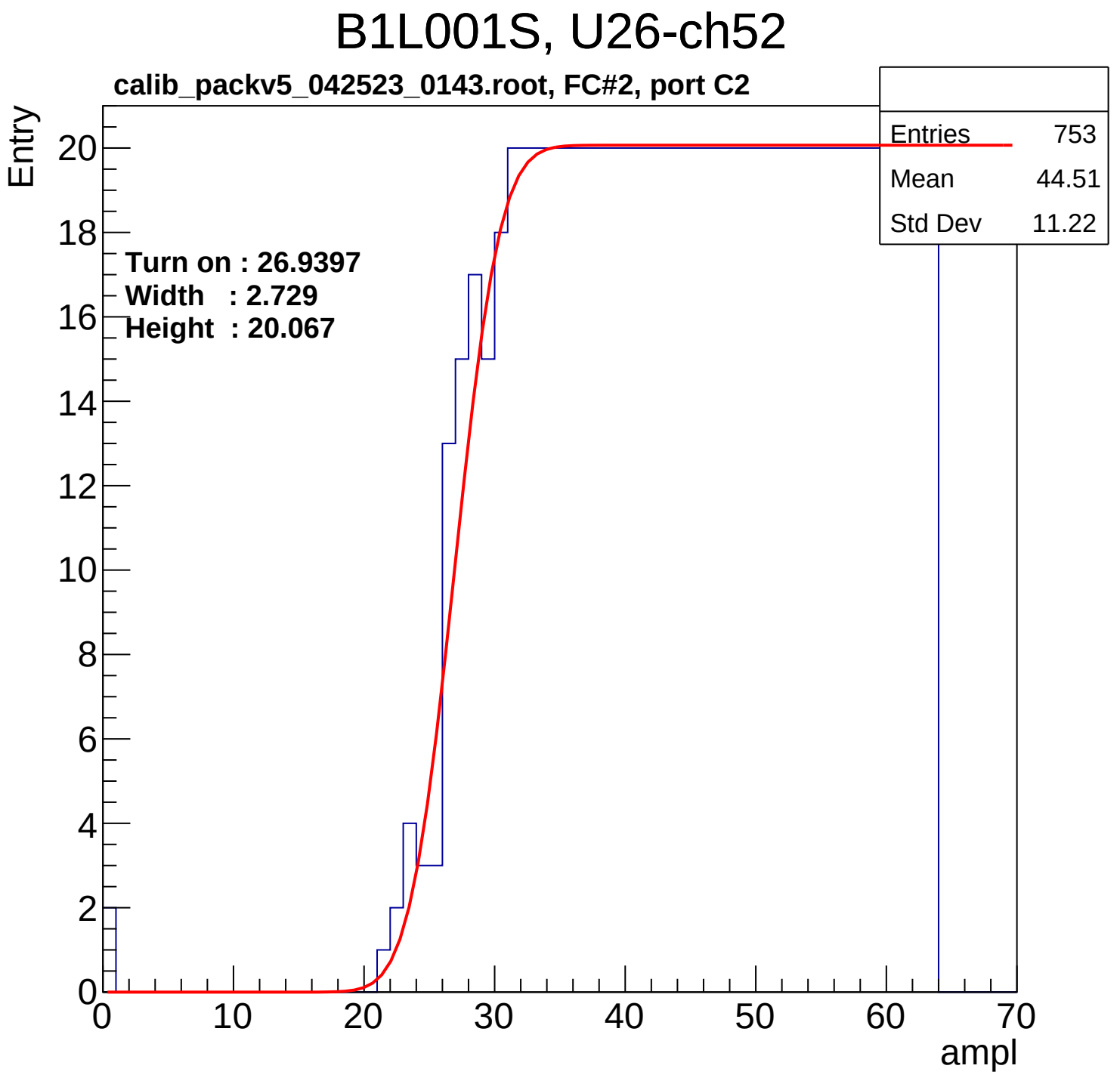

B1L001S, U26-ch47
calib_packv5_042523_0143.root, FC#2, port C2
Entries 738
Mean 44.83
Std Dev 11.19
Turn on : 27.2191
Width : 1.990
Height : 19.884
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

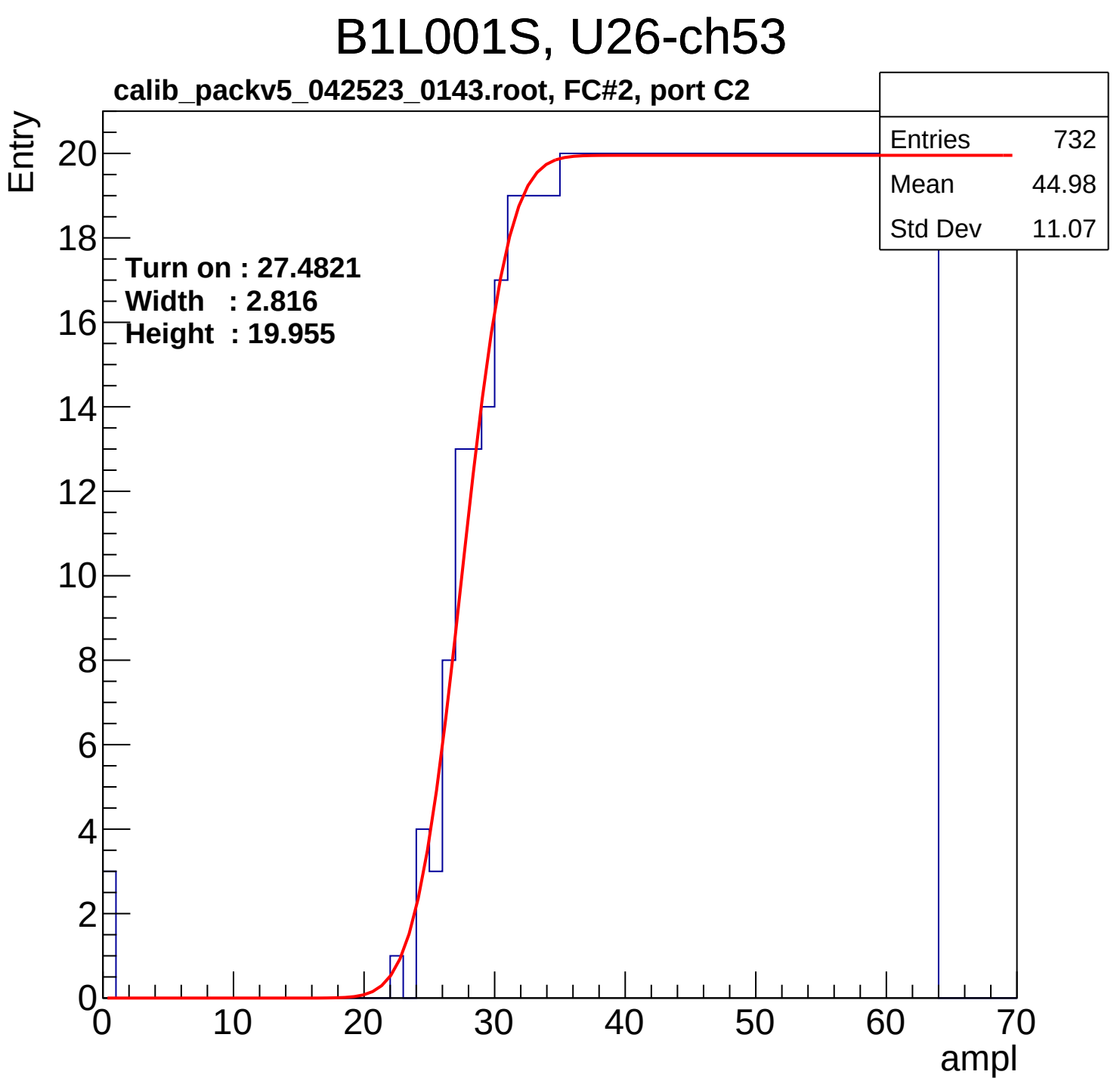

B1L001S, U26-ch48
calib_packv5_042523_0143.root, FC#2, port C2
Entries 773
Mean 44.01
Std Dev 11.5
Turn on : 25.6581
Width : 2.792
Height : 20.030
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

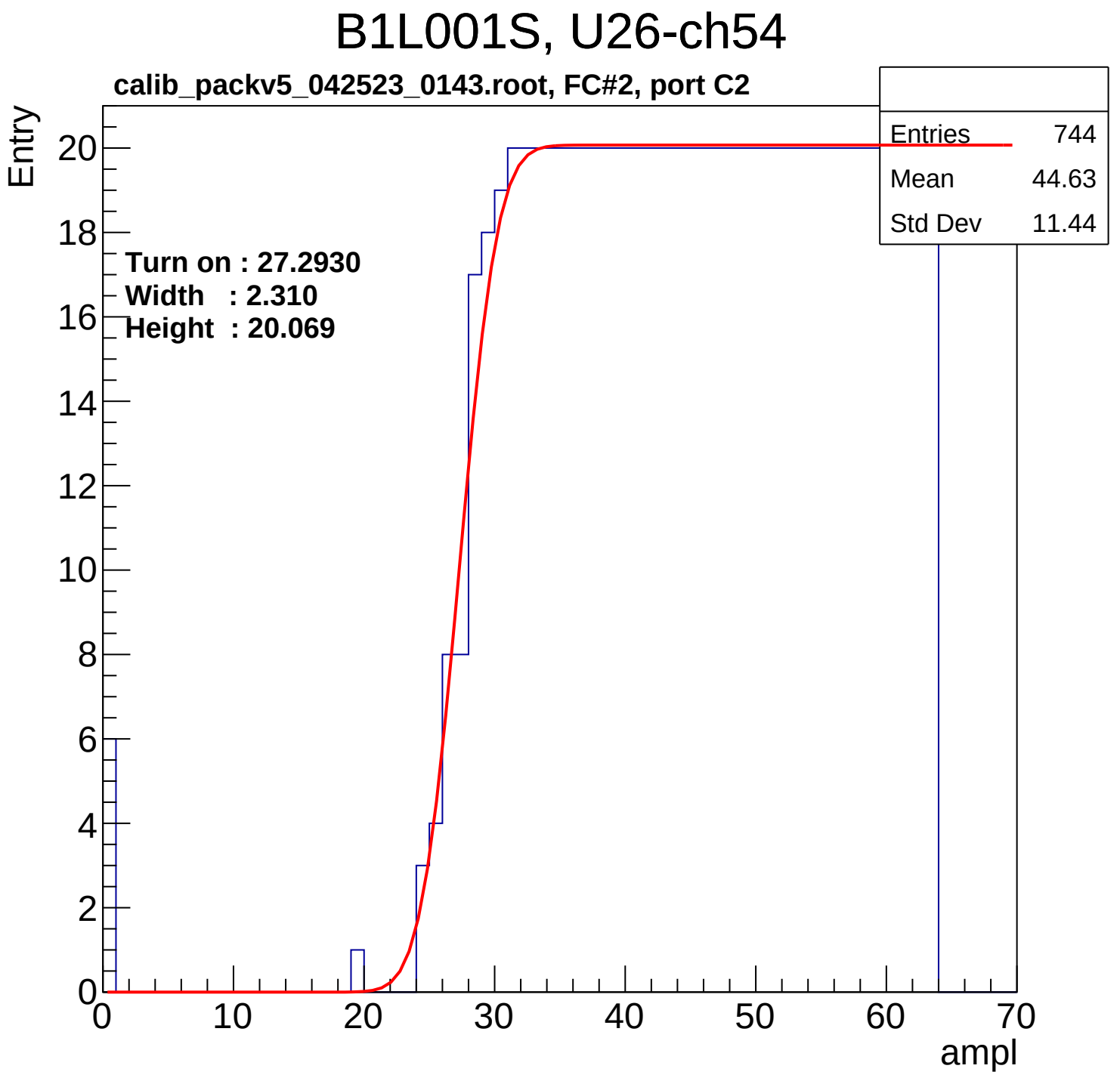

B1L001S, U26-ch49
calib_packv5_042523_0143.root, FC#2, port C2
Entries 751
Mean 44.57
Std Dev 11.18
Turn on : 26.8071
Width : 2.491
Height : 20.026
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

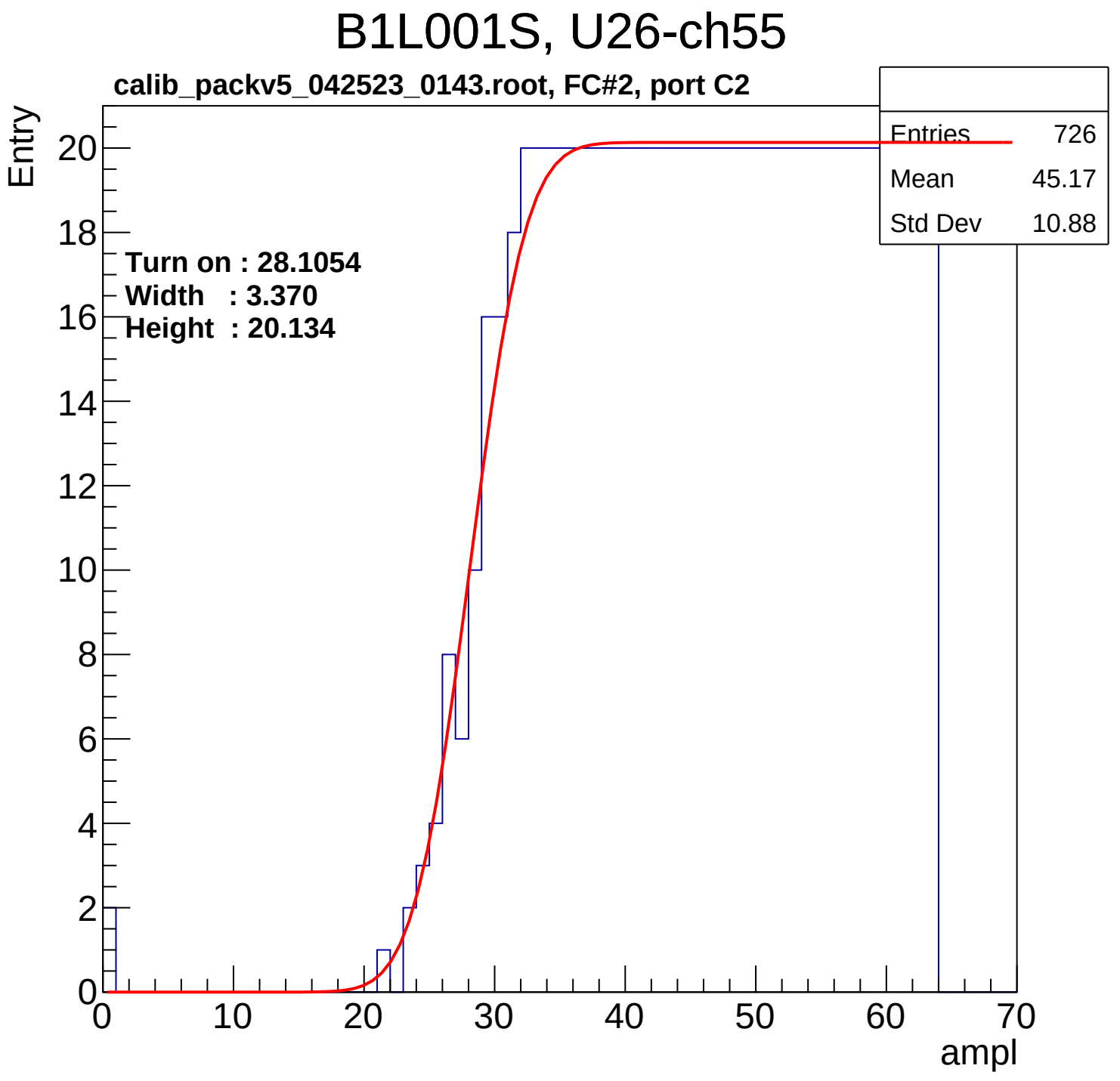

B1L001S, U26-ch50
calib_packv5_042523_0143.root, FC#2, port C2
Entries 727
Mean 45.17
Std Dev 10.85
Turn on : 27.8991
Width : 2.622
Height : 20.052
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

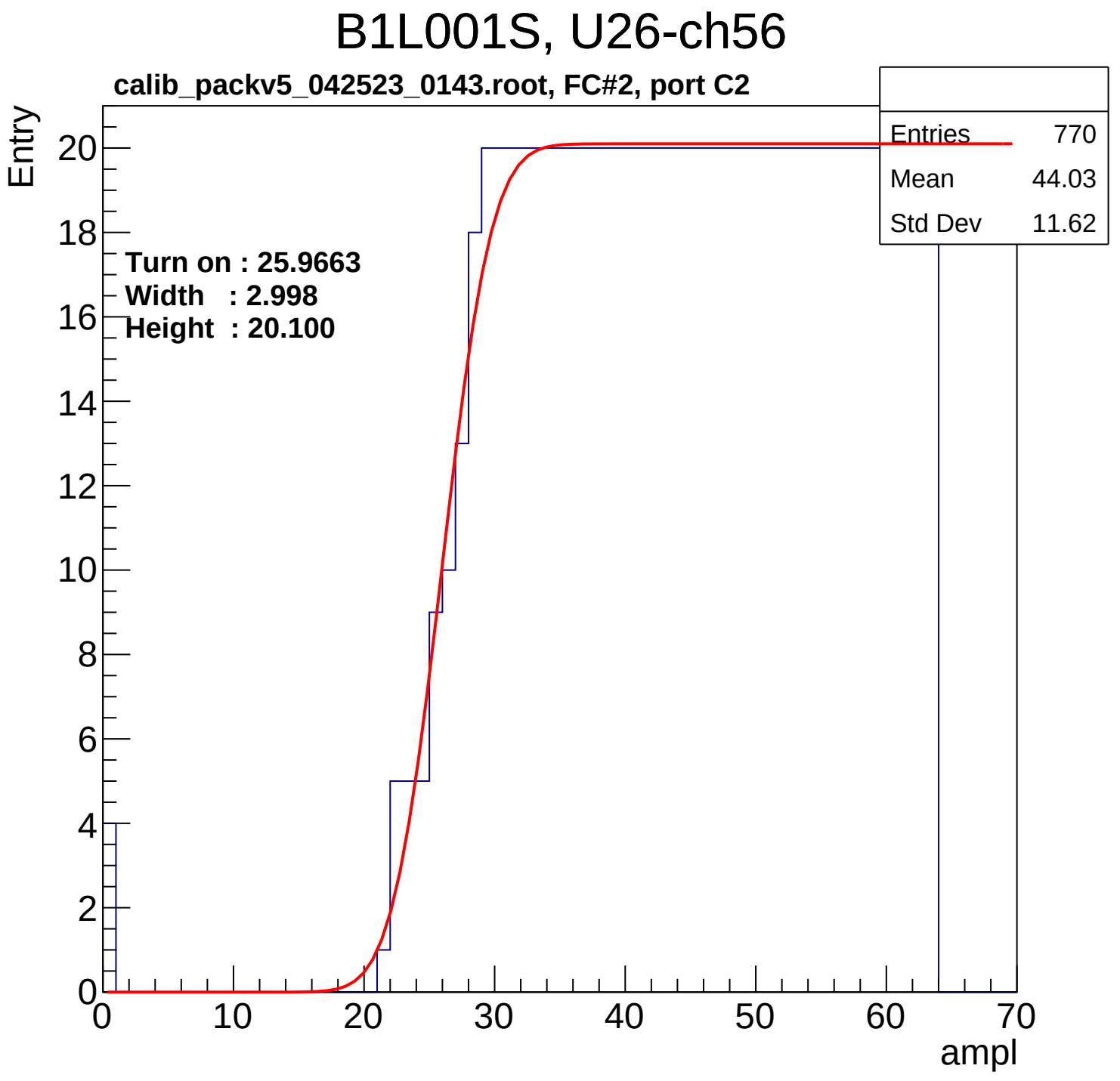

B1L001S, U26-ch51
calib_packv5_042523_0143.root, FC#2, port C2
Entries 720
Mean 45.27
Std Dev 10.92
Turn on : 28.2557
Width : 2.800
Height : 19.986
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

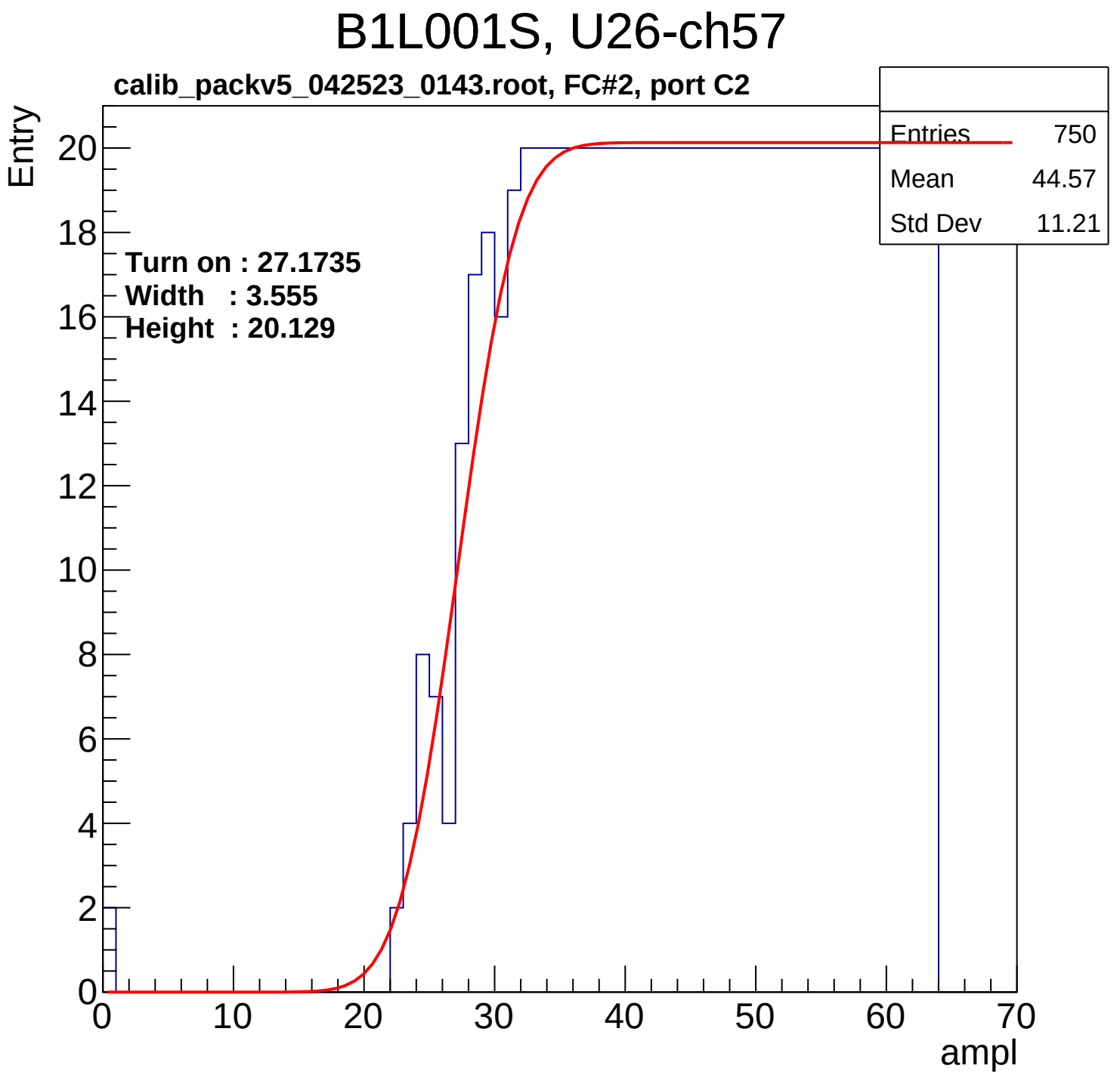

B1L001S, U26-ch52
calib_packv5_042523_0143.root, FC#2, port C2
Entries 753
Mean 44.51
Std Dev 11.22
Turn on : 26.9397
Width : 2.729
Height : 20.067
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

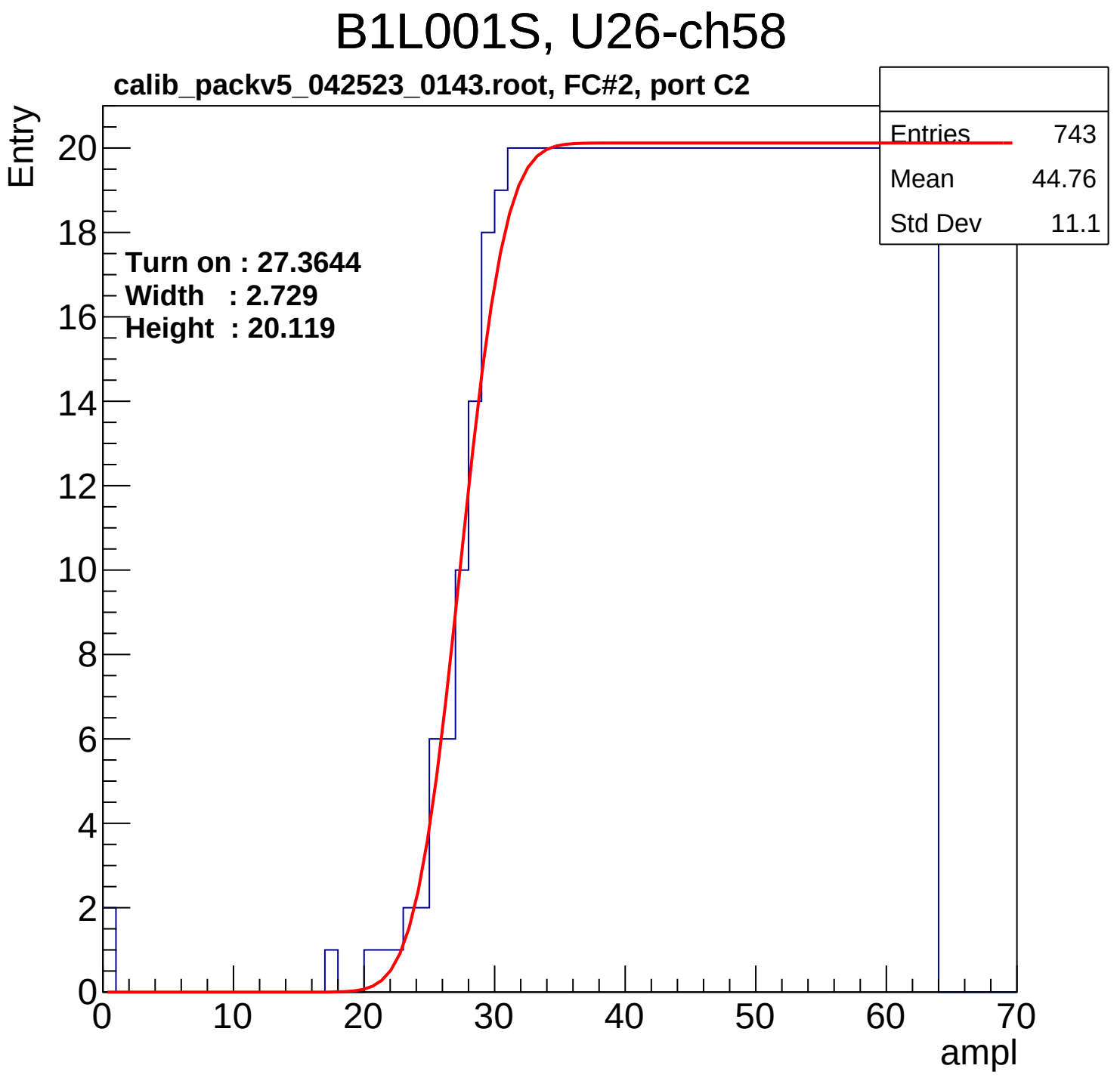

B1L001S, U26-ch53
calib_packv5_042523_0143.root, FC#2, port C2
Entries 732
Mean 44.98
Std Dev 11.07
Turn on : 27.4821
Width : 2.816
Height : 19.955
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

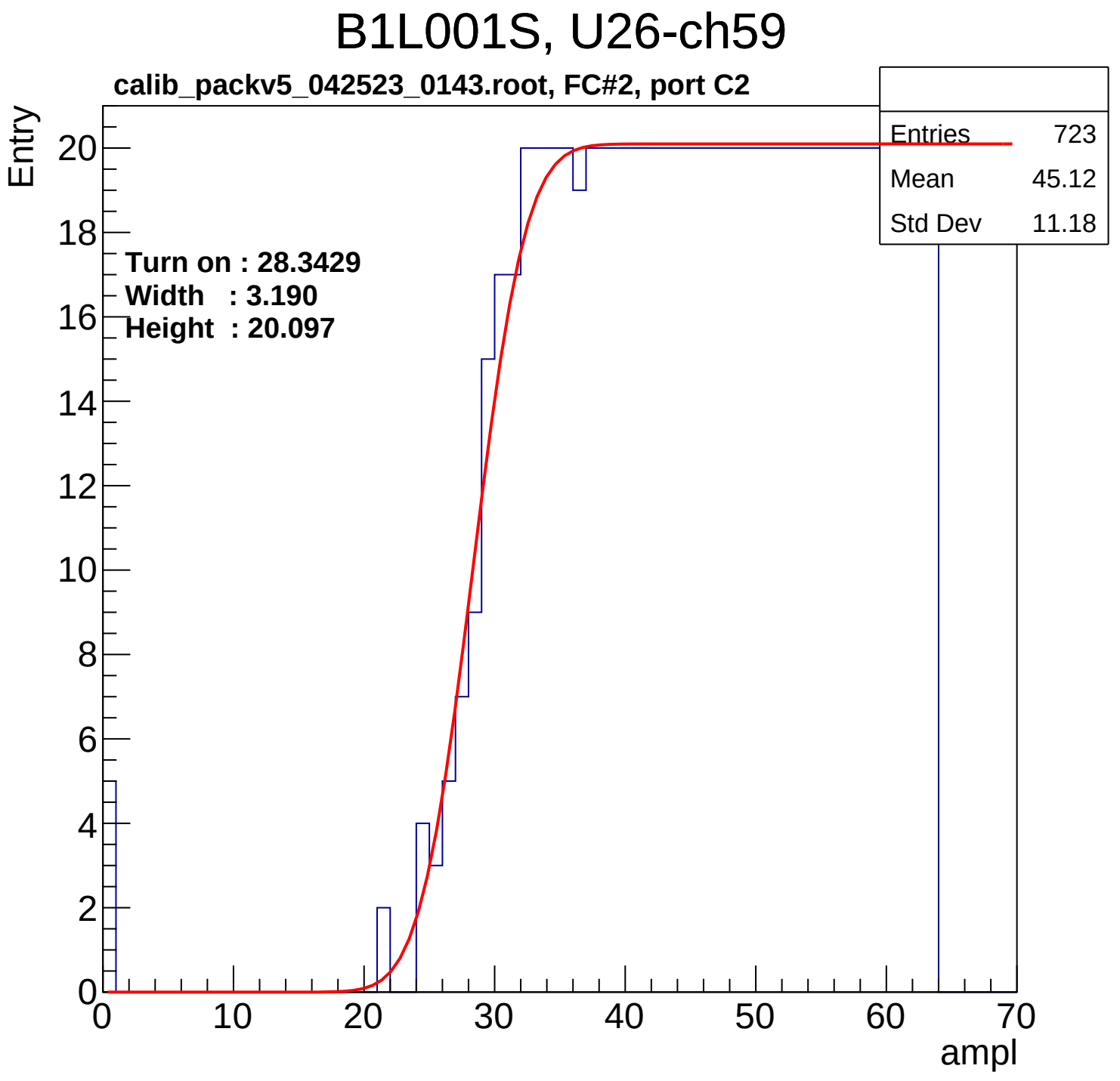

B1L001S, U26-ch54
calib_packv5_042523_0143.root, FC#2, port C2
Entries 744
Mean 44.63
Std Dev 11.44
Turn on : 27.2930
Width : 2.310
Height : 20.069
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

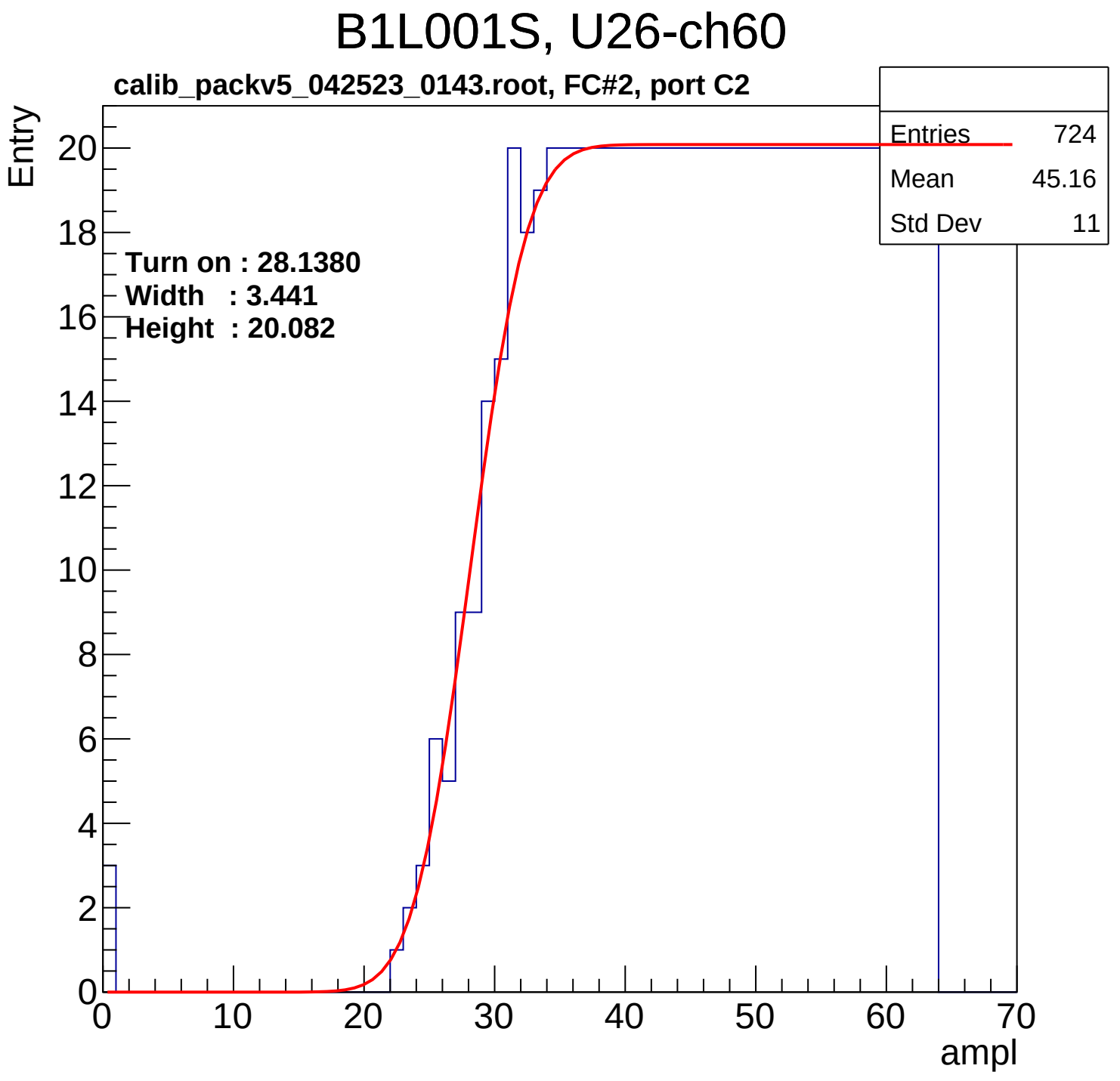

B1L001S, U26-ch55
calib_packv5_042523_0143.root, FC#2, port C2
Entries 726
Mean 45.17
Std Dev 10.88
Turn on : 28.1054
Width : 3.370
Height : 20.134
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

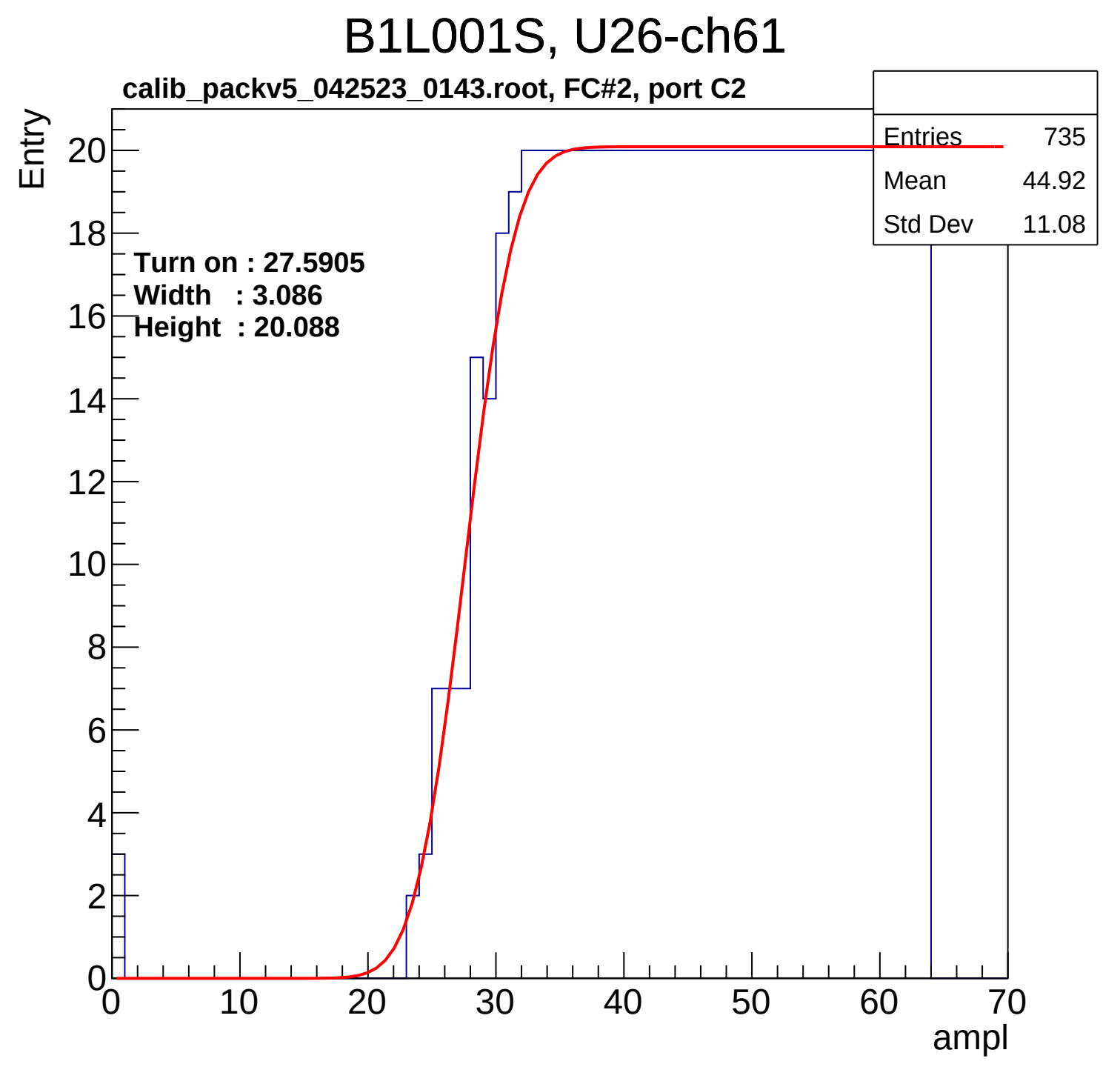

B1L001S, U26-ch56
calib_packv5_042523_0143.root, FC#2, port C2
Entries 770
Mean 44.03
Std Dev 11.62
Turn on : 25.9663
Width : 2.998
Height : 20.100
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

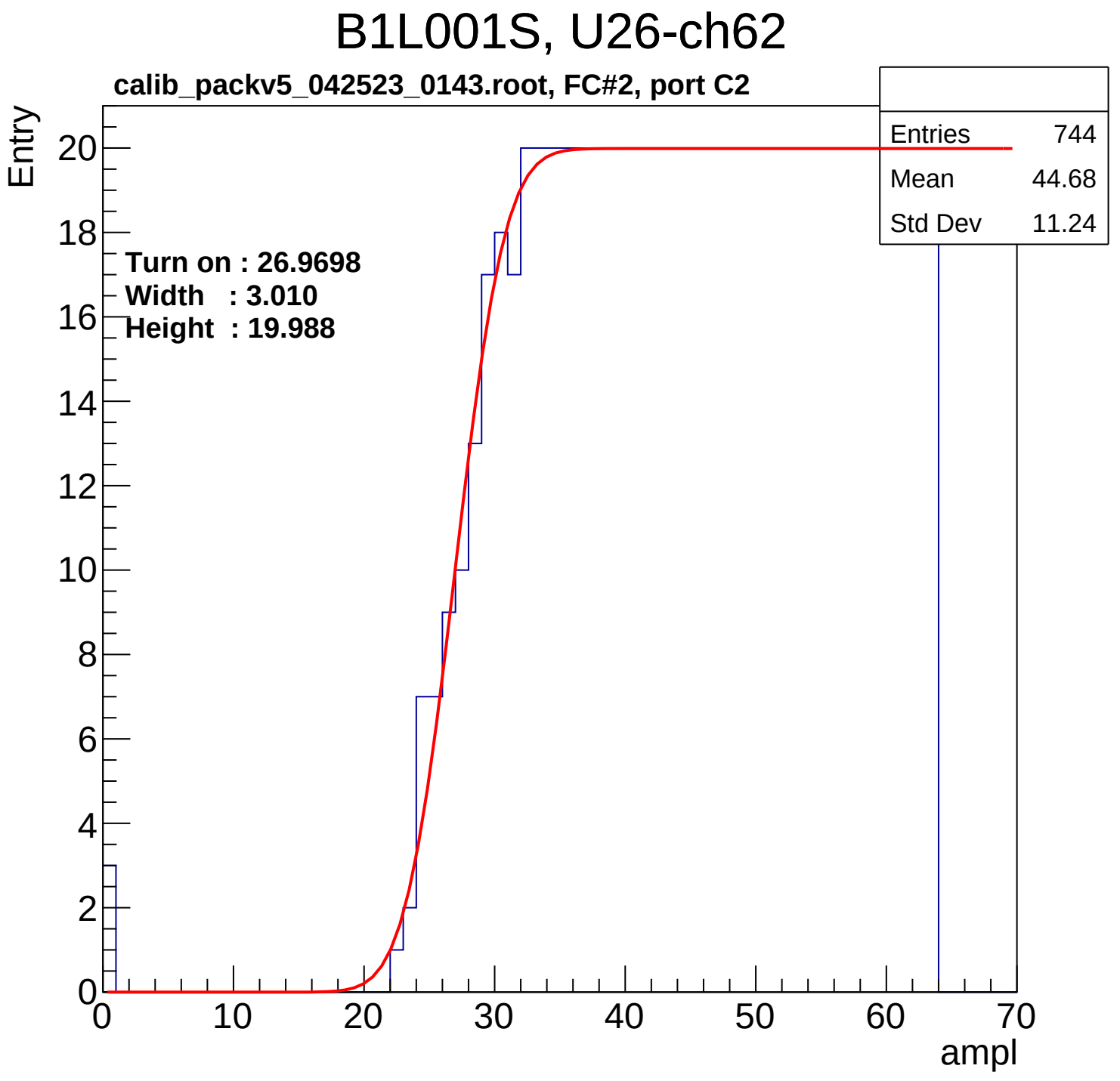

B1L001S, U26-ch57
calib_packv5_042523_0143.root, FC#2, port C2
Entries 750
Mean 44.57
Std Dev 11.21
Turn on : 27.1735
Width : 3.555
Height : 20.129
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

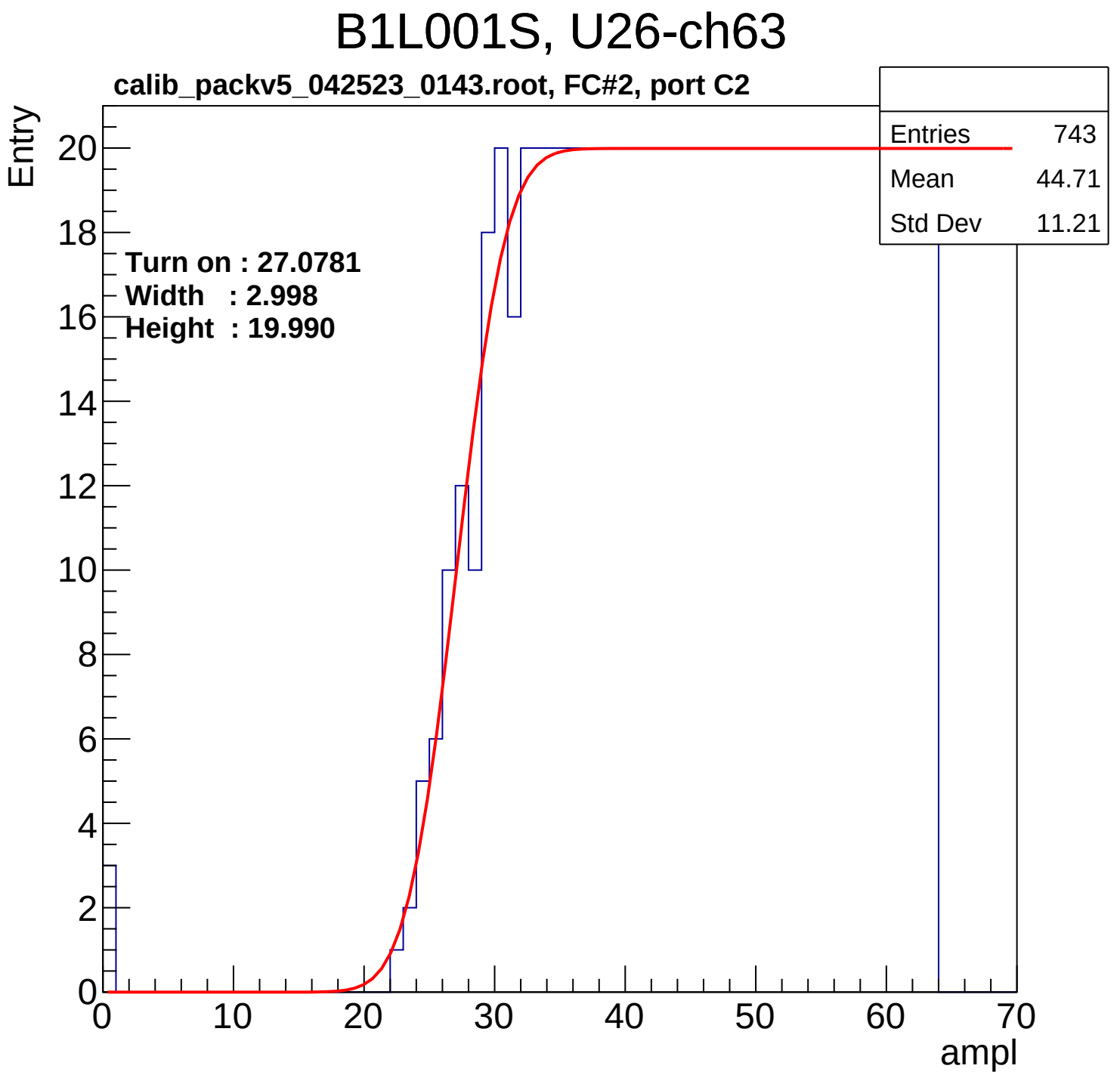

B1L001S, U26-ch58
calib_packv5_042523_0143.root, FC#2, port C2
Entries 743
Mean 44.76
Std Dev 11.1
Turn on : 27.3644
Width : 2.729
Height : 20.119
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

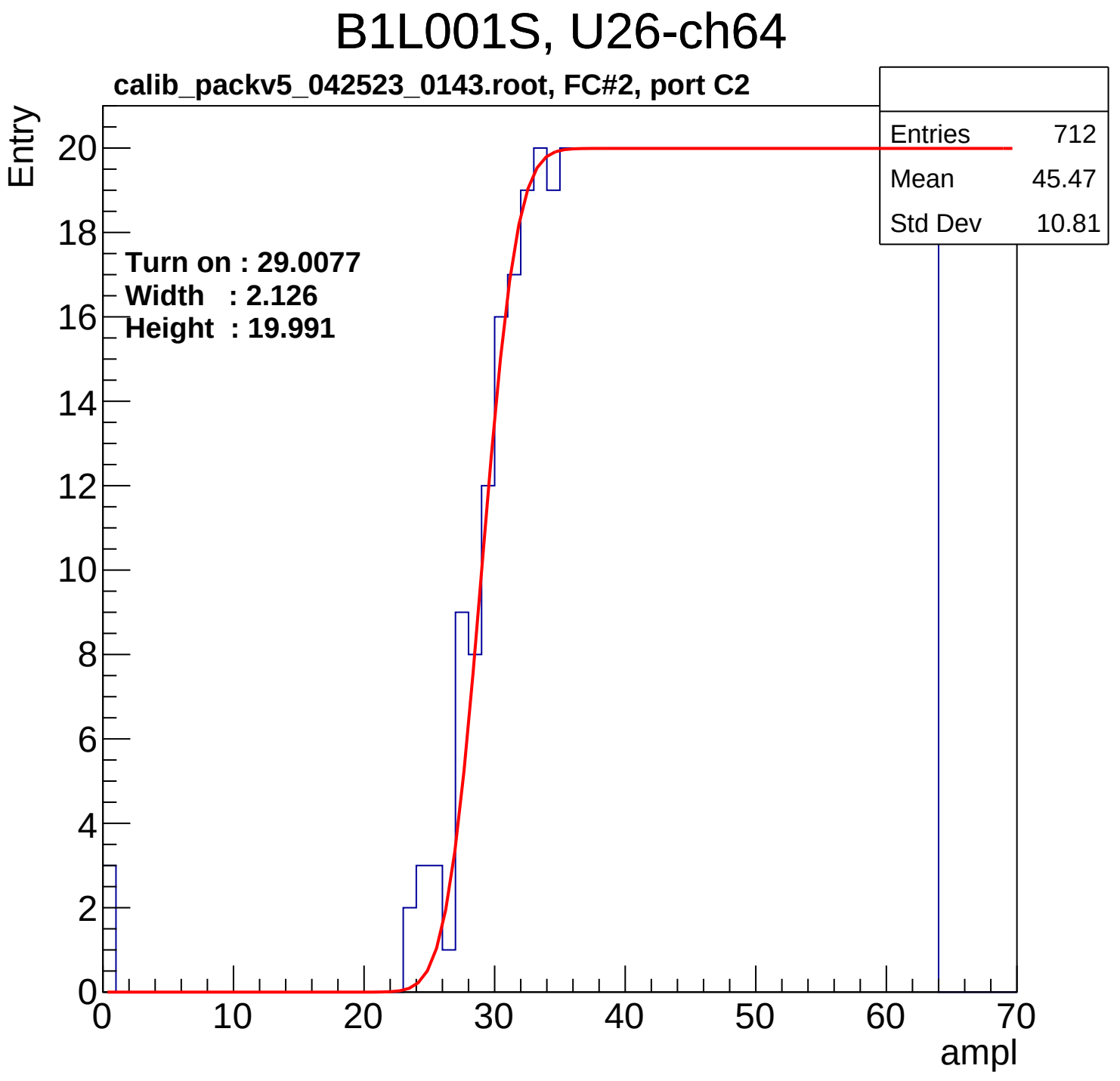

B1L001S, U26-ch59
calib_packv5_042523_0143.root, FC#2, port C2
Entries 723
Mean 45.12
Std Dev 11.18
Turn on : 28.3429
Width : 3.190
Height : 20.097
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

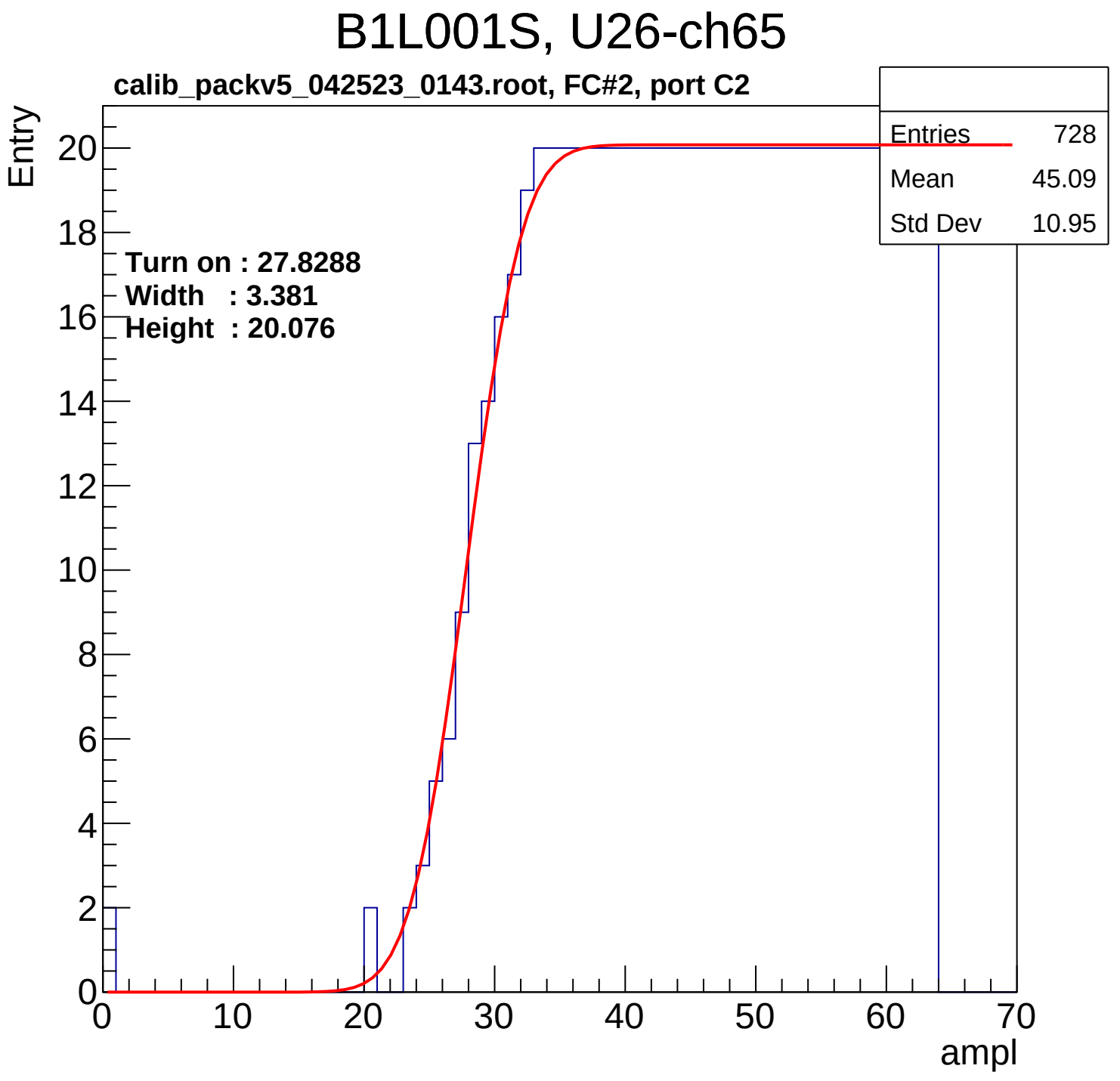

B1L001S, U26-ch60
calib_packv5_042523_0143.root, FC#2, port C2
Entries 724
Mean 45.16
Std Dev 11
Turn on : 28.1380
Width : 3.441
Height : 20.082
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

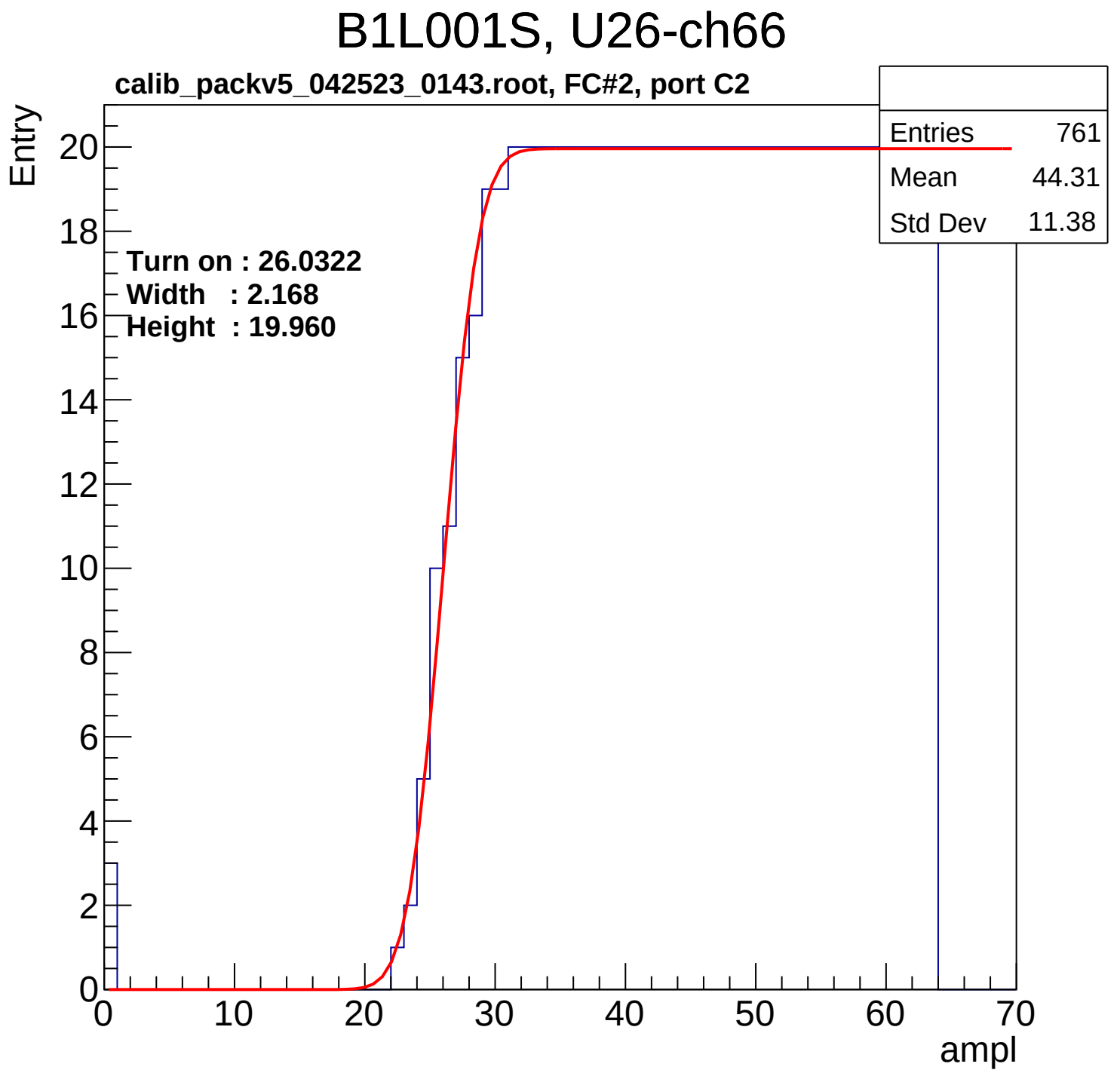

B1L001S, U26-ch61
calib_packv5_042523_0143.root, FC#2, port C2
Entries 735
Mean 44.92
Std Dev 11.08
Turn on : 27.5905
Width : 3.086
Height : 20.088
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

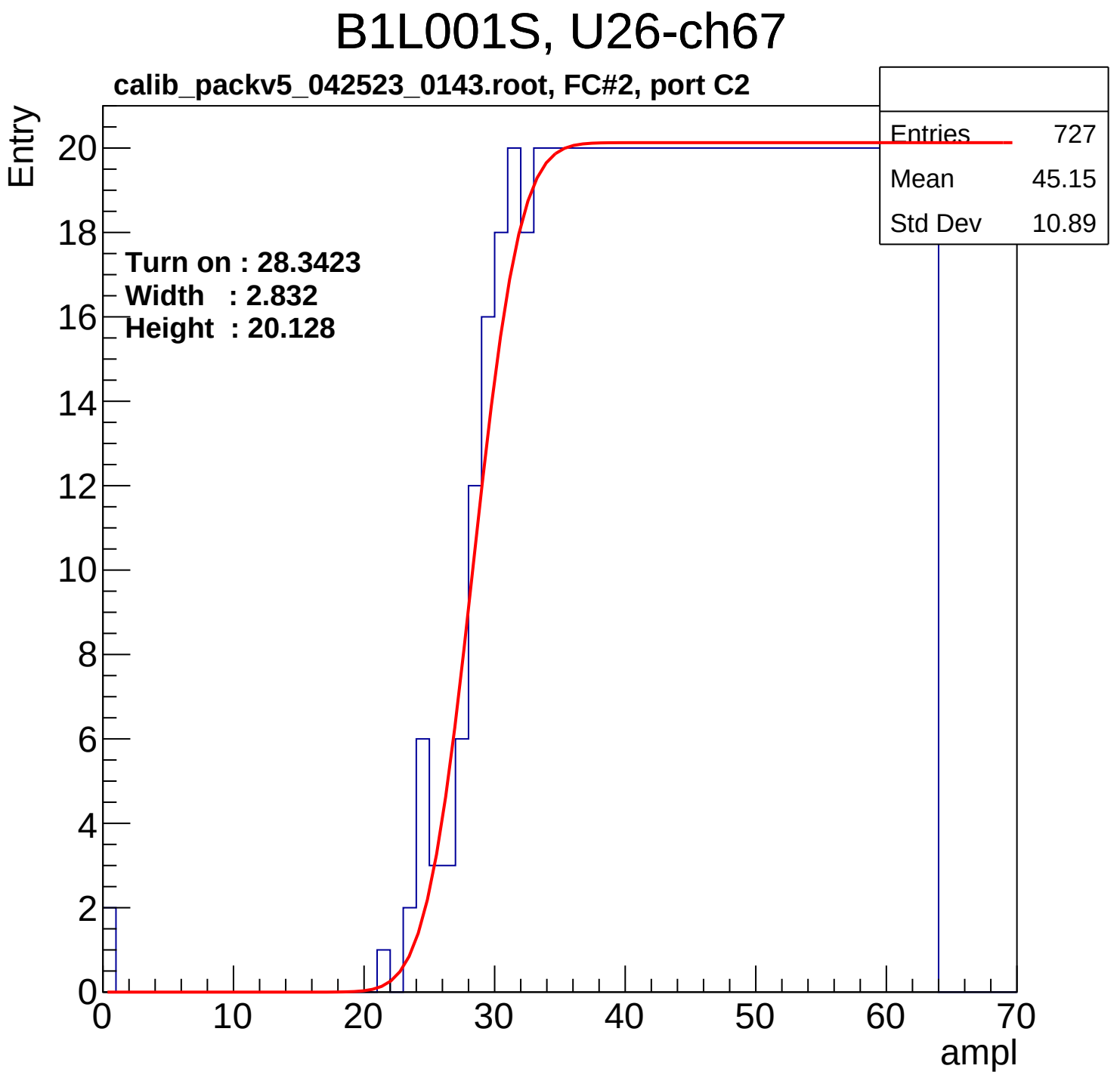

B1L001S, U26-ch62
calib_packv5_042523_0143.root, FC#2, port C2
Entries 744
Mean 44.68
Std Dev 11.24
Turn on : 26.9698
Width : 3.010
Height : 19.988
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

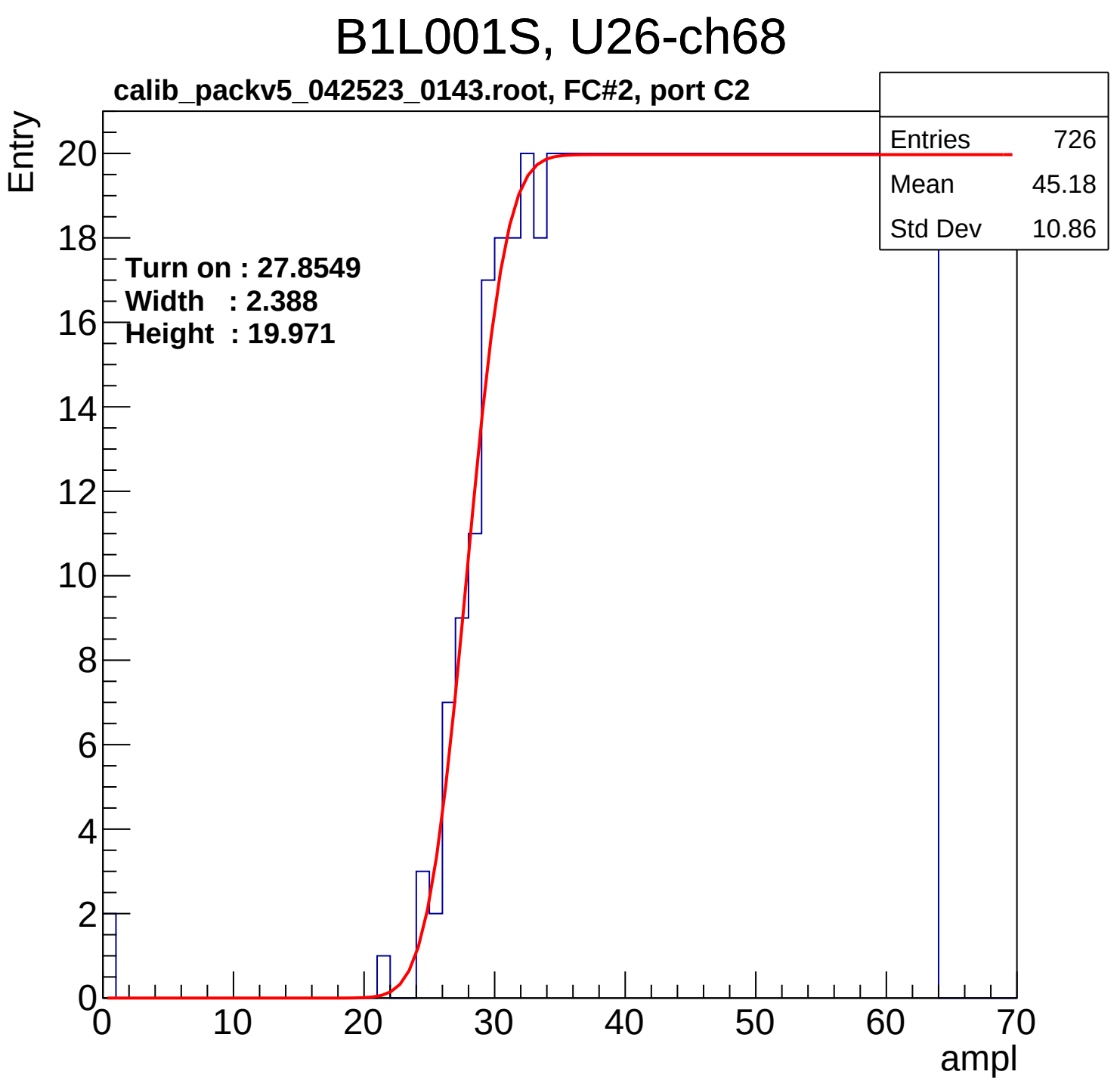

B1L001S, U26-ch63
calib_packv5_042523_0143.root, FC#2, port C2
Entries 743
Mean 44.71
Std Dev 11.21
Turn on : 27.0781
Width : 2.998
Height : 19.990
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

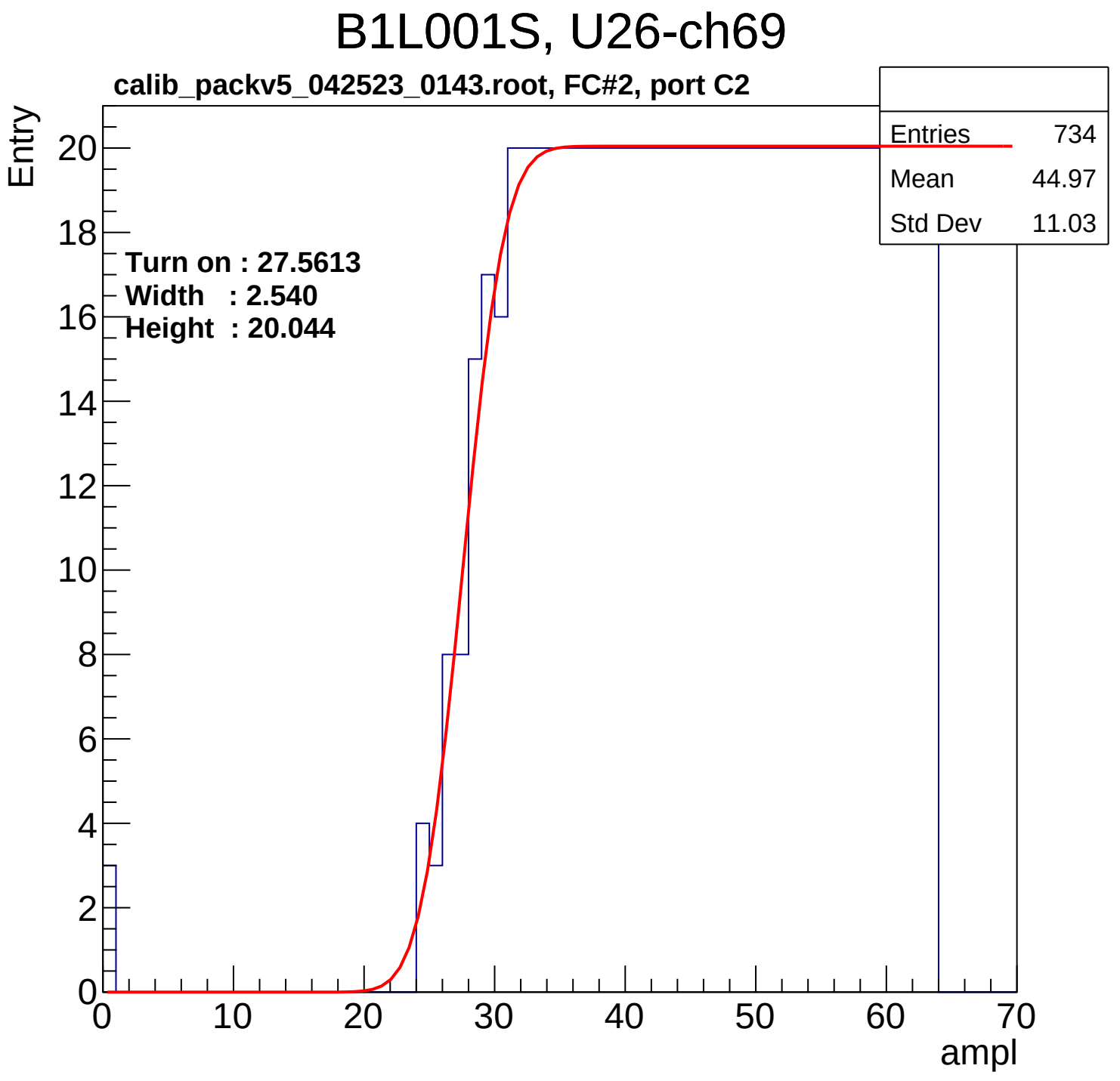

B1L001S, U26-ch64
calib_packv5_042523_0143.root, FC#2, port C2
Entries 712
Mean 45.47
Std Dev 10.81
Turn on : 29.0077
Width : 2.126
Height : 19.991
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

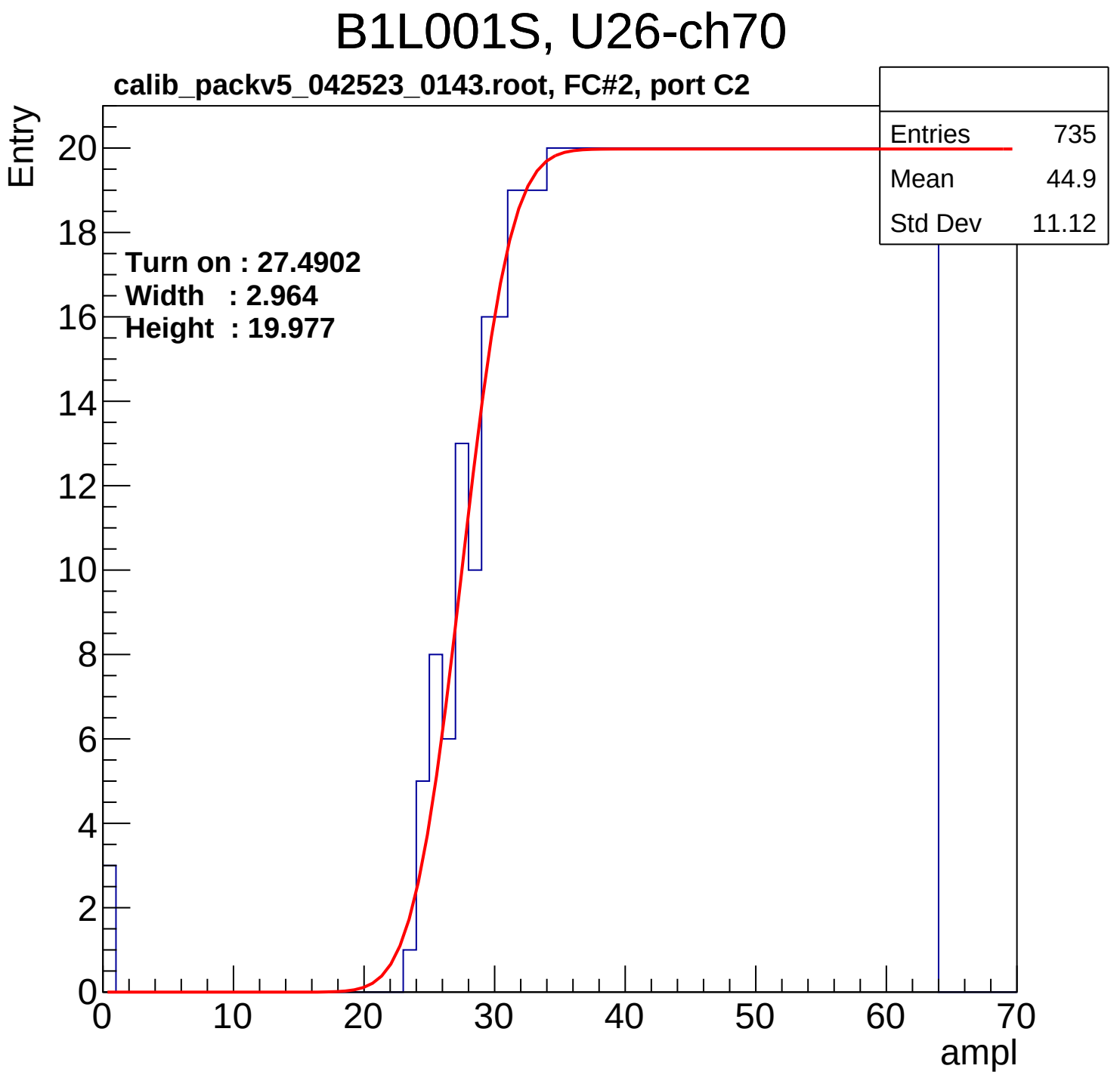

B1L001S, U26-ch65
calib_packv5_042523_0143.root, FC#2, port C2
Entries 728
Mean 45.09
Std Dev 10.95
Turn on : 27.8288
Width : 3.381
Height : 20.076
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

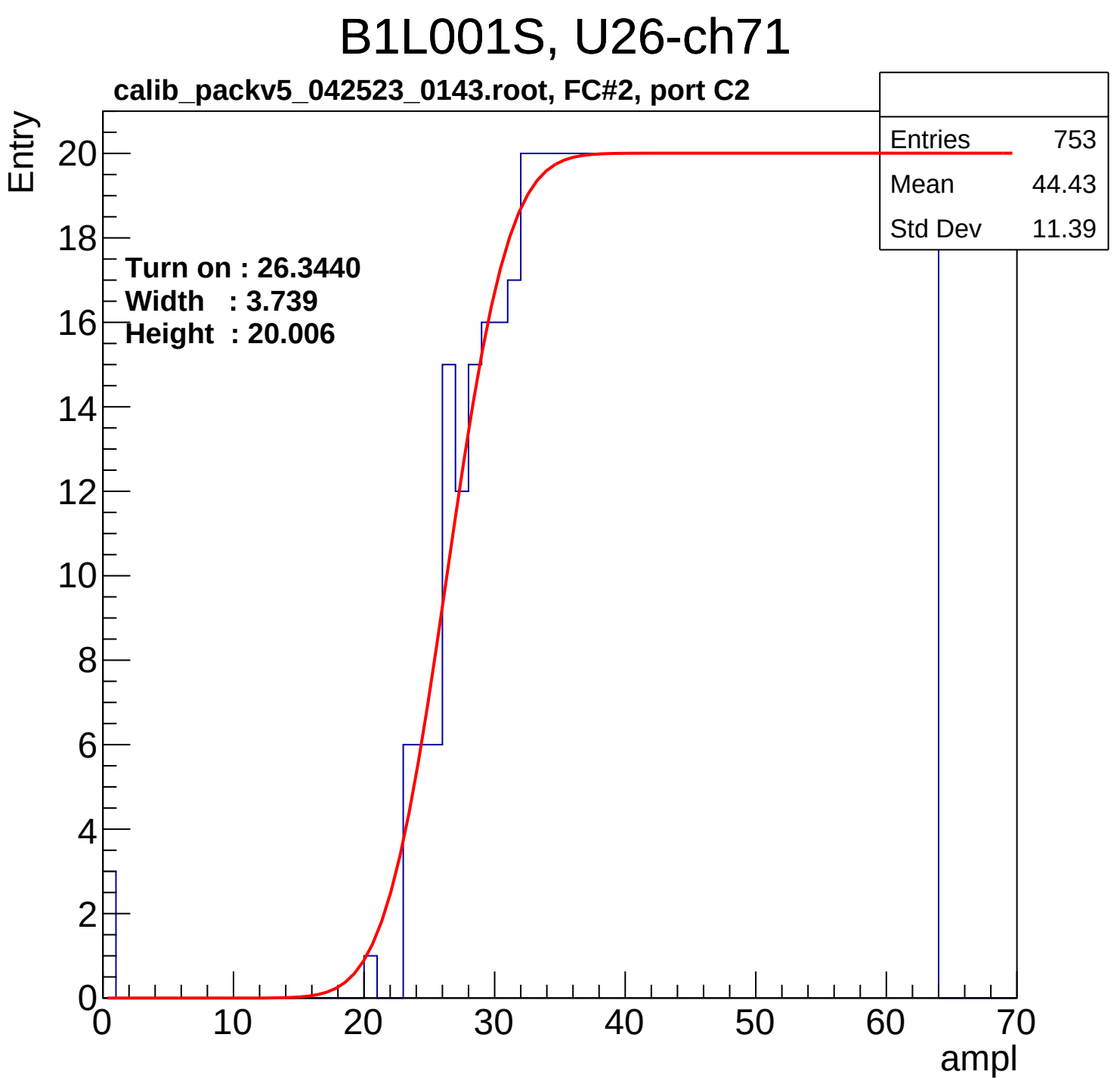

B1L001S, U26-ch66
calib_packv5_042523_0143.root, FC#2, port C2
Entries 761
Mean 44.31
Std Dev 11.38
Turn on : 26.0322
Width : 2.168
Height : 19.960
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

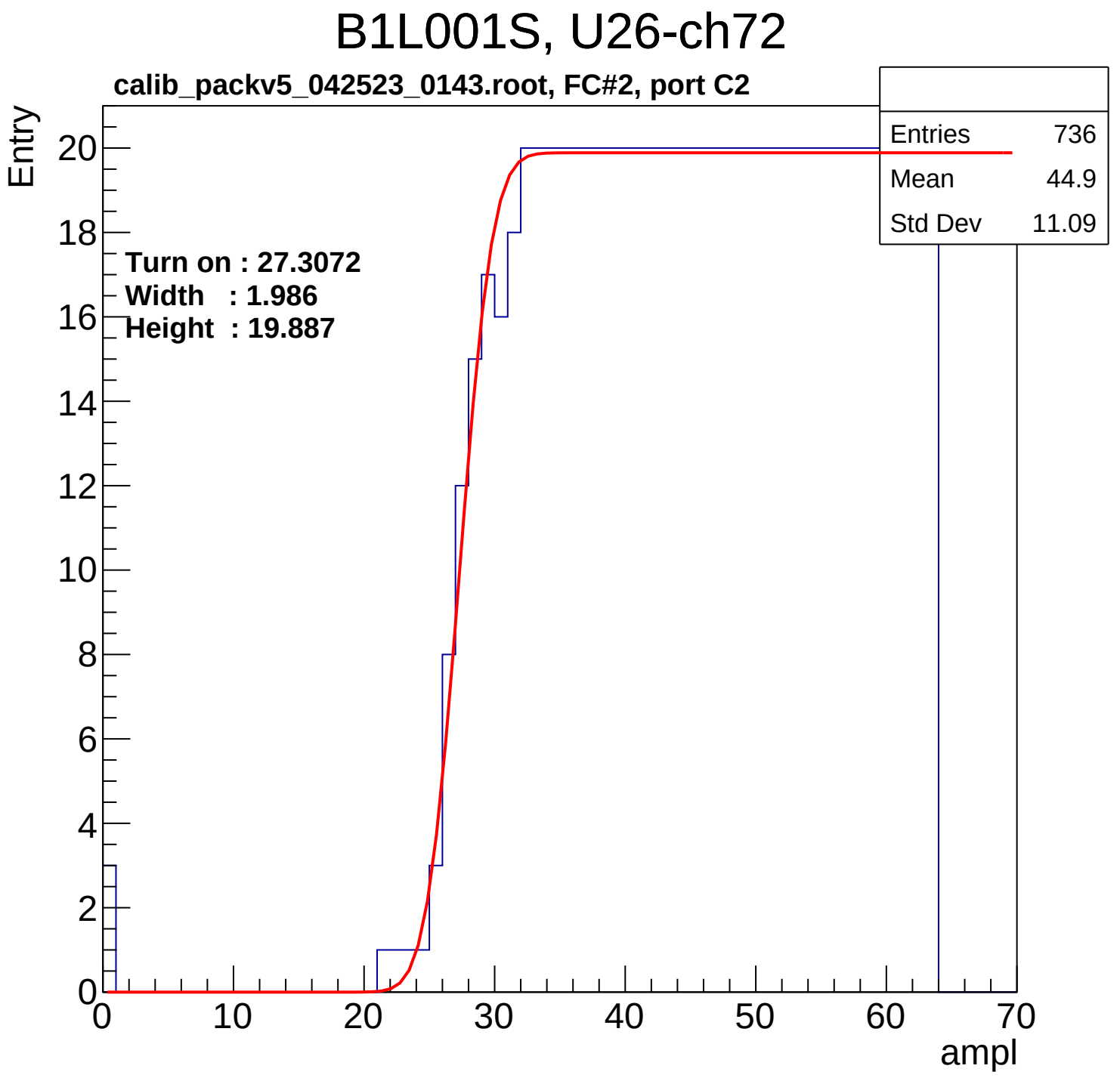

B1L001S, U26-ch67
calib_packv5_042523_0143.root, FC#2, port C2
Entries 727
Mean 45.15
Std Dev 10.89
Turn on : 28.3423
Width : 2.832
Height : 20.128
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

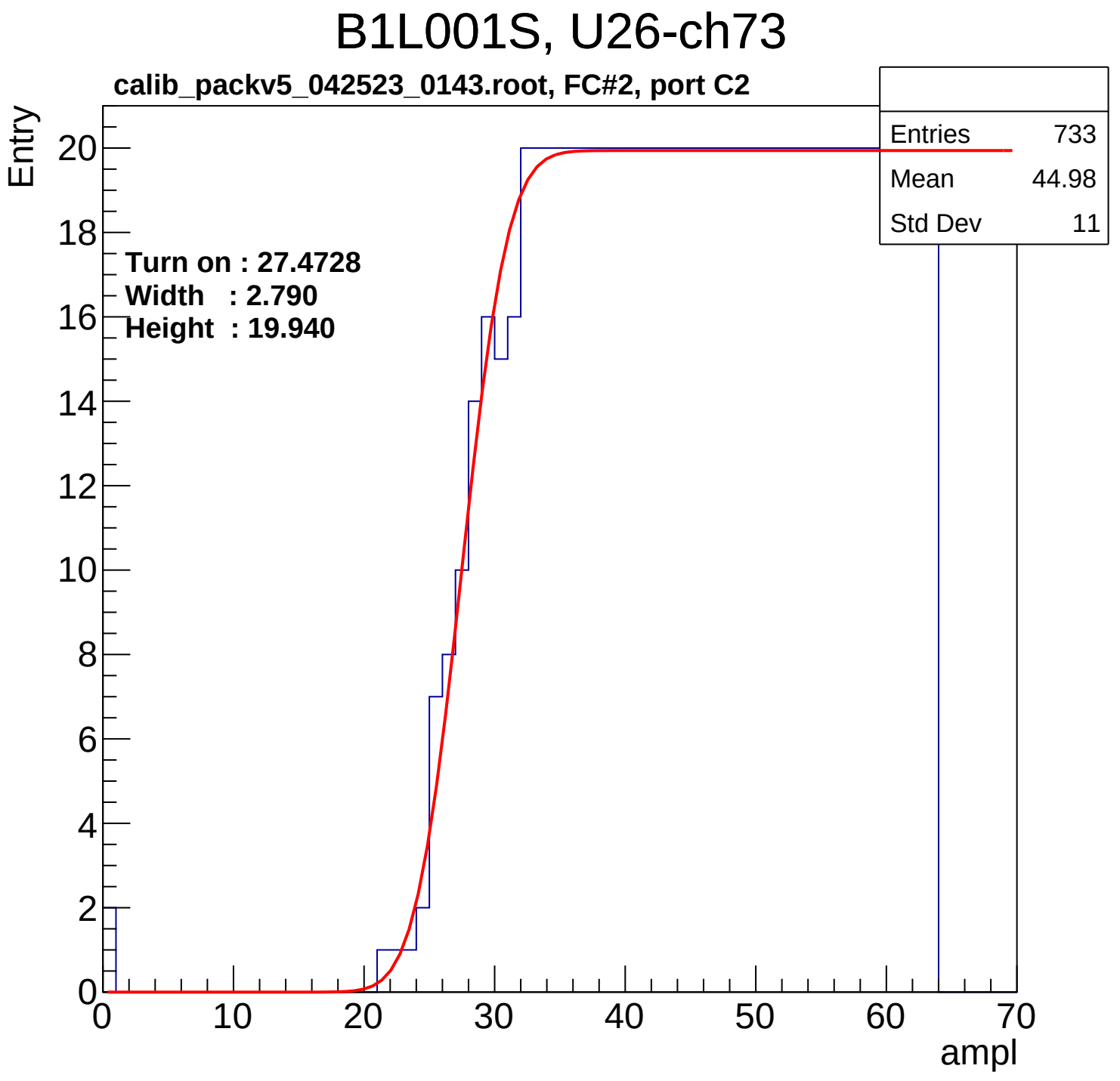

B1L001S, U26-ch68
calib_packv5_042523_0143.root, FC#2, port C2
Entries 726
Mean 45.18
Std Dev 10.86
Turn on : 27.8549
Width : 2.388
Height : 19.971
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

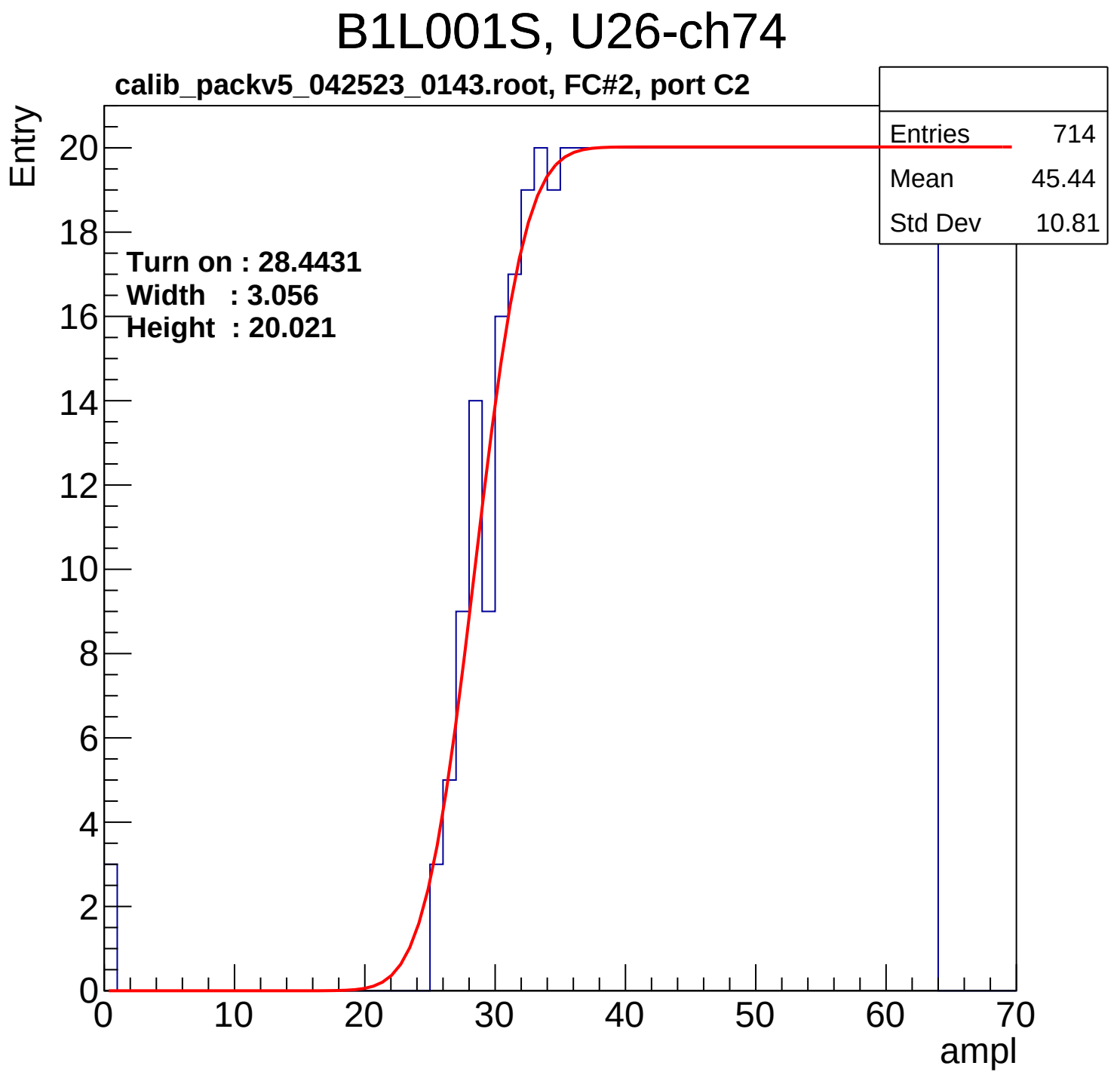

B1L001S, U26-ch69
calib_packv5_042523_0143.root, FC#2, port C2
Entries 734
Mean 44.97
Std Dev 11.03
Turn on : 27.5613
Width : 2.540
Height : 20.044
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

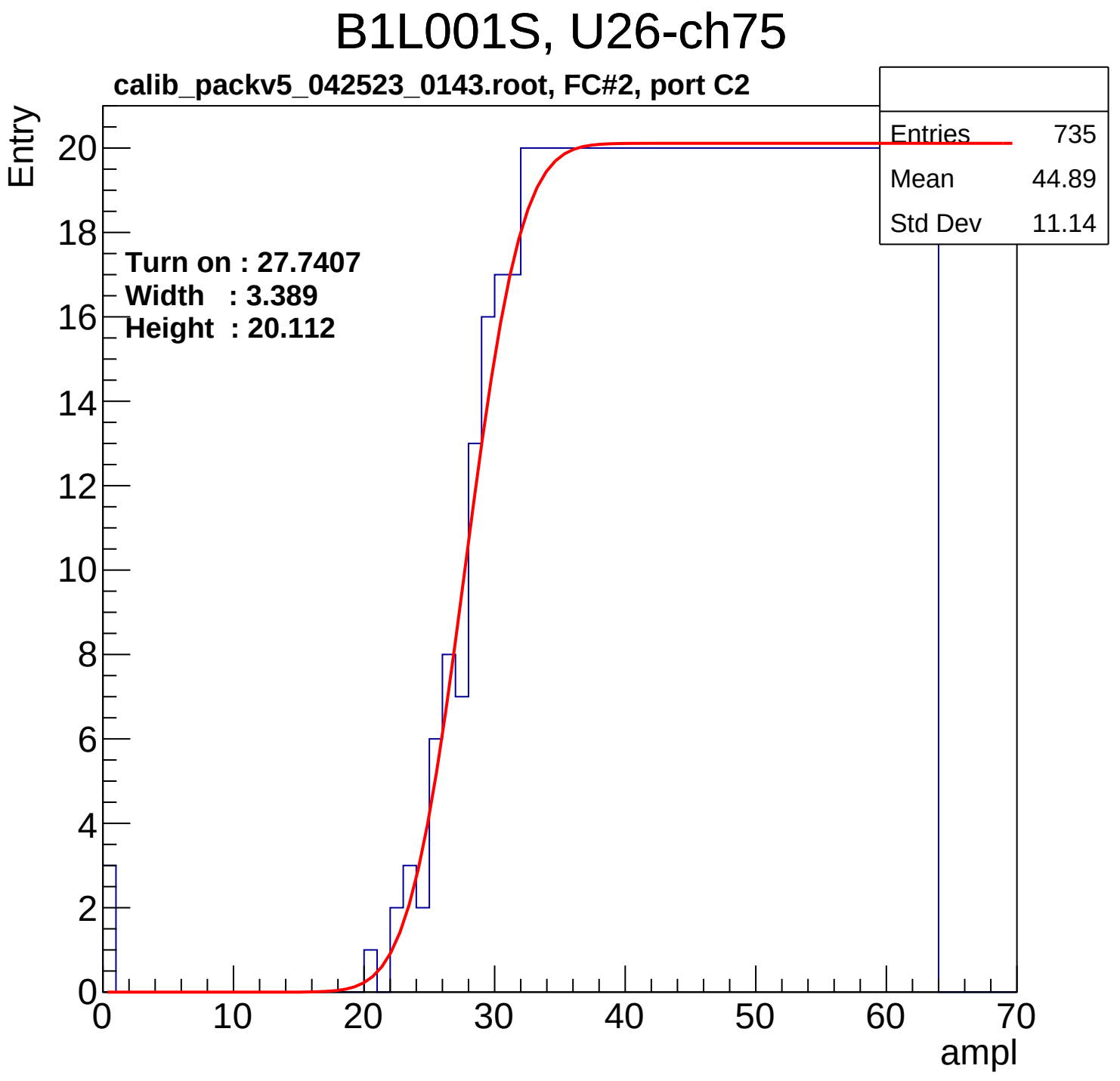

B1L001S, U26-ch70
calib_packv5_042523_0143.root, FC#2, port C2
Entries 735
Mean 44.9
Std Dev 11.12
Turn on : 27.4902
Width : 2.964
Height : 19.977
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

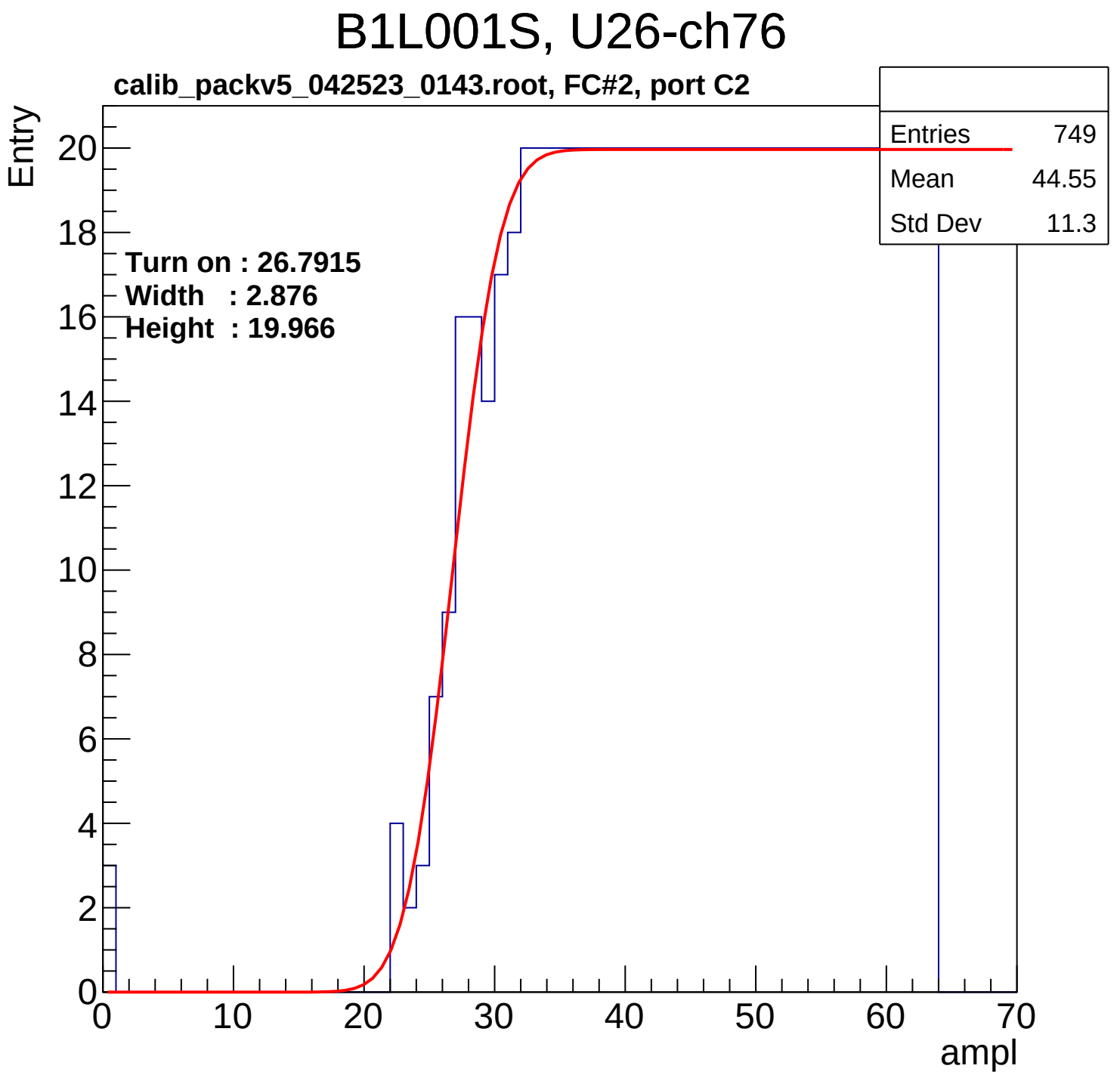

B1L001S, U26-ch71
calib_packv5_042523_0143.root, FC#2, port C2
Entries 753
Mean 44.43
Std Dev 11.39
Turn on : 26.3440
Width : 3.739
Height : 20.006
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

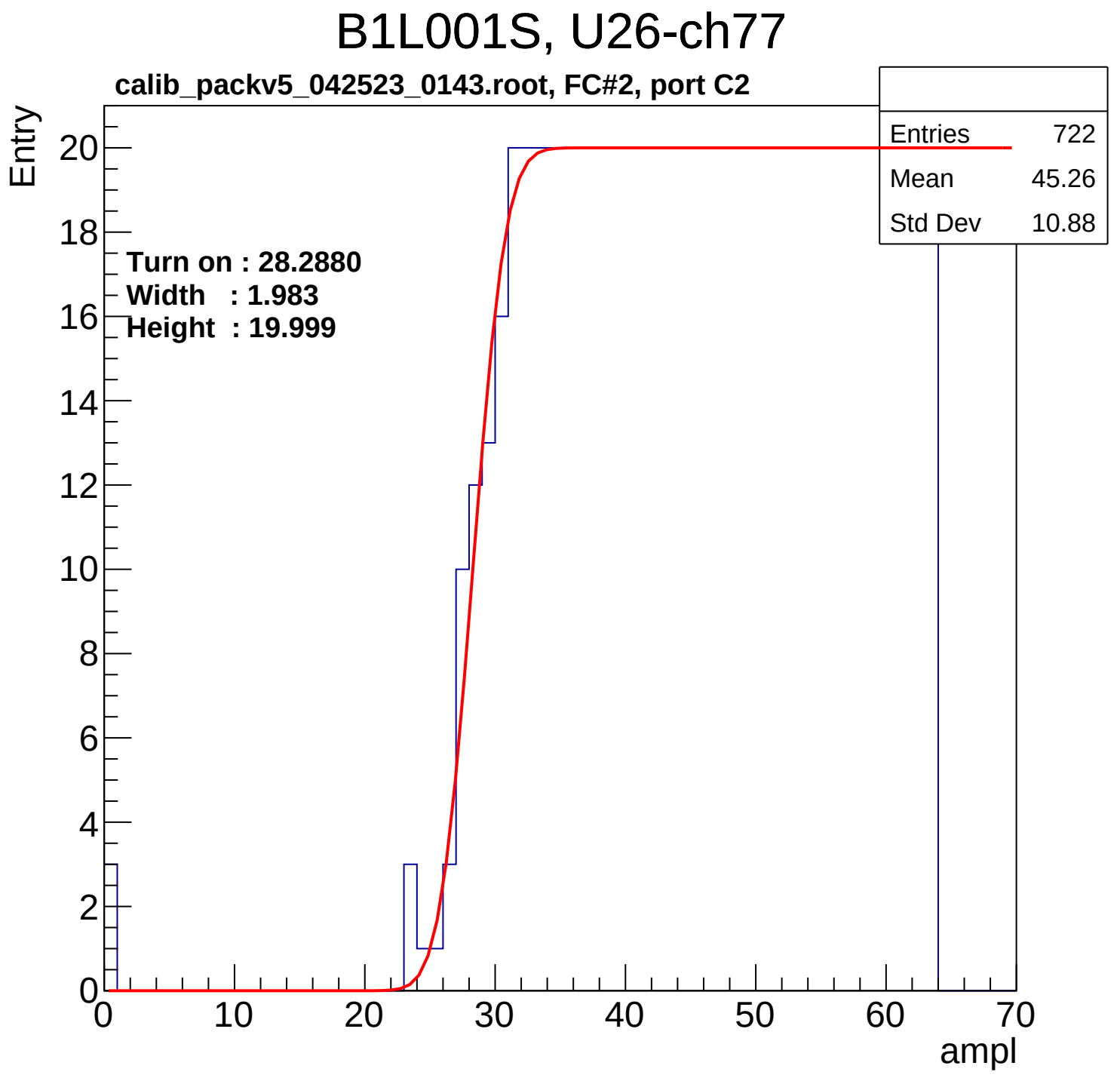

B1L001S, U26-ch72
calib_packv5_042523_0143.root, FC#2, port C2
Entries 736
Mean 44.9
Std Dev 11.09
Turn on : 27.3072
Width : 1.986
Height : 19.887
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

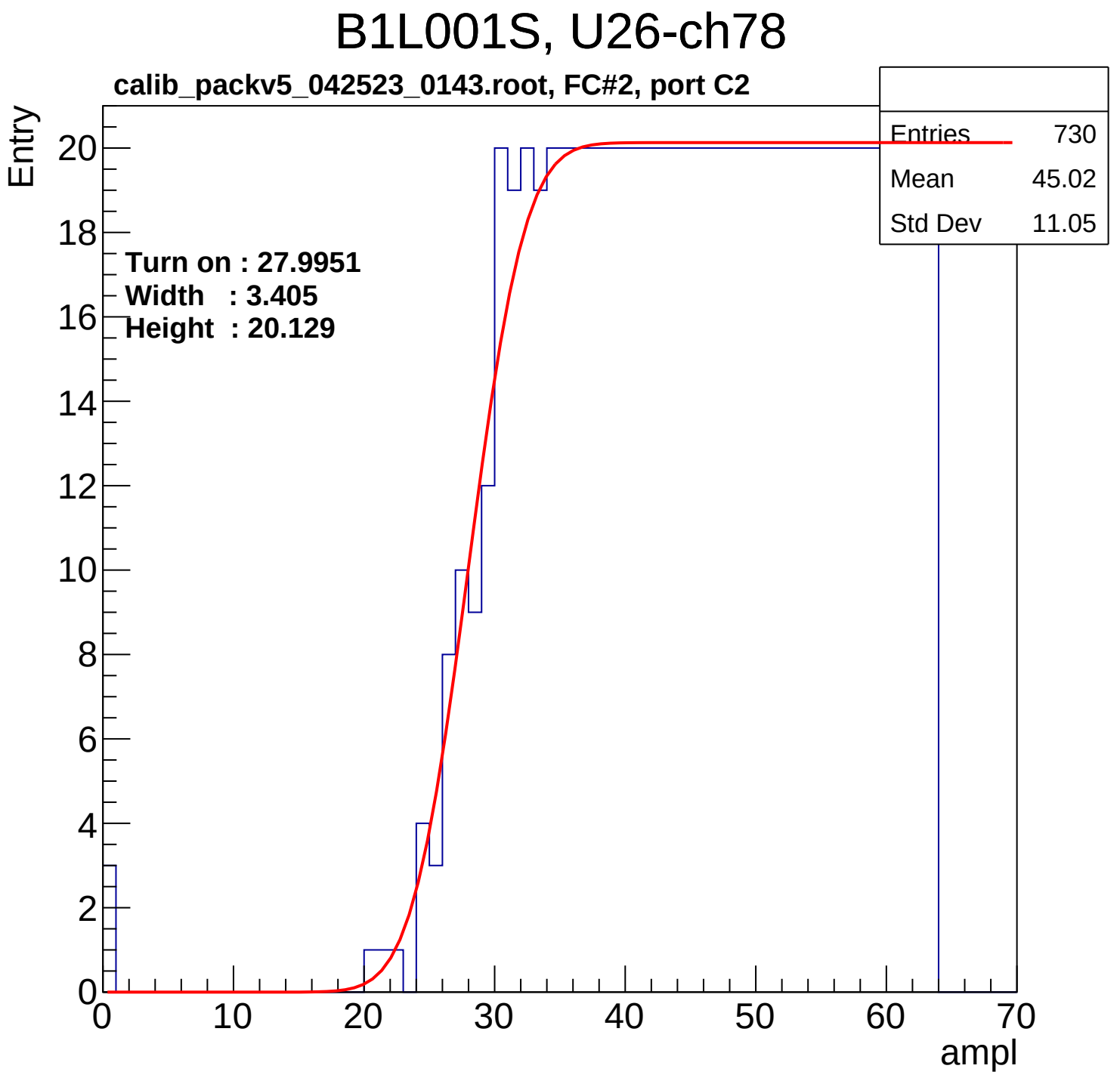

B1L001S, U26-ch73
calib_packv5_042523_0143.root, FC#2, port C2
Entries 733
Mean 44.98
Std Dev 11
Turn on : 27.4728
Width : 2.790
Height : 19.940
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

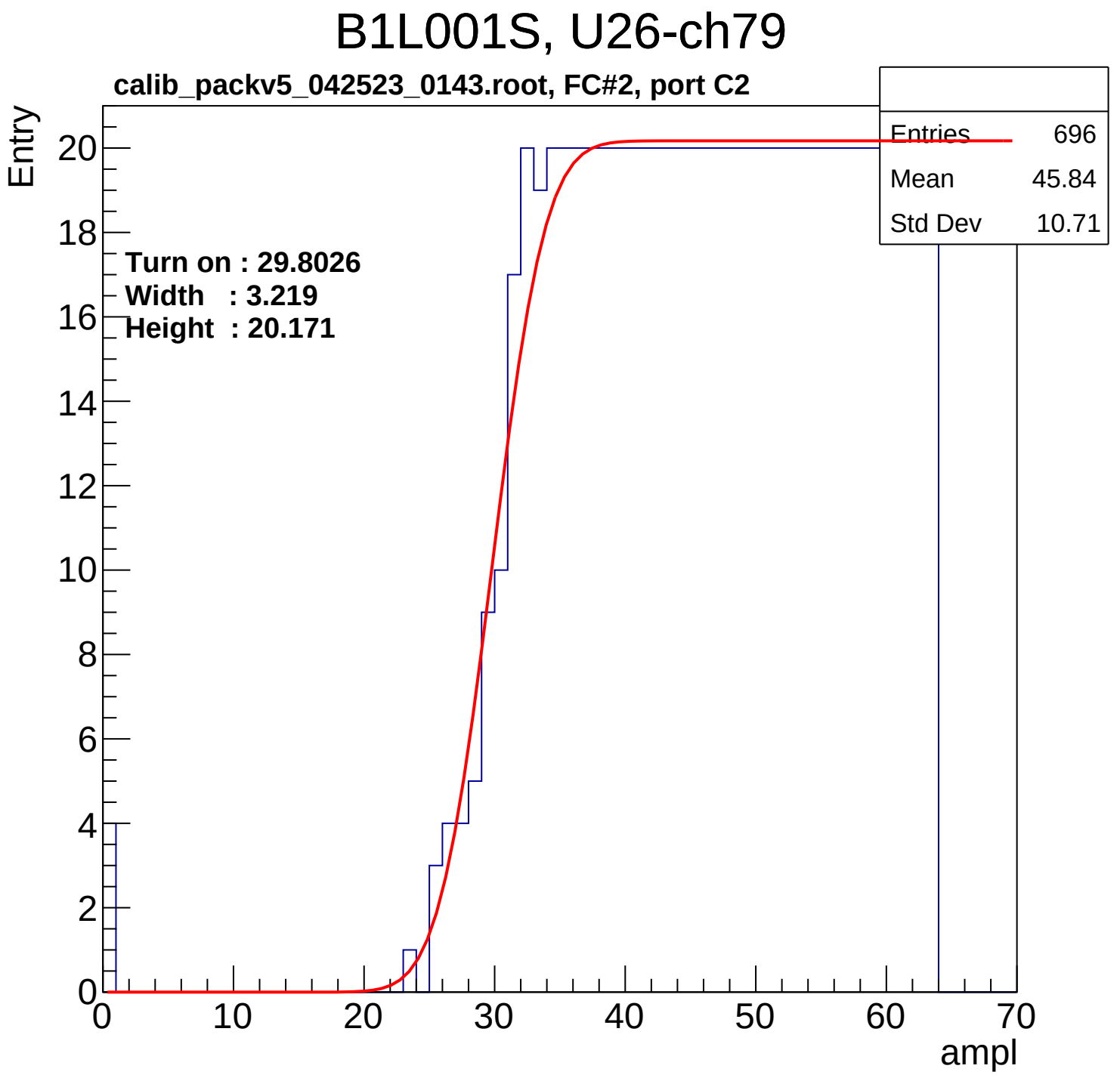

B1L001S, U26-ch74
calib_packv5_042523_0143.root, FC#2, port C2
Entries 714
Mean 45.44
Std Dev 10.81
Turn on : 28.4431
Width : 3.056
Height : 20.021
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

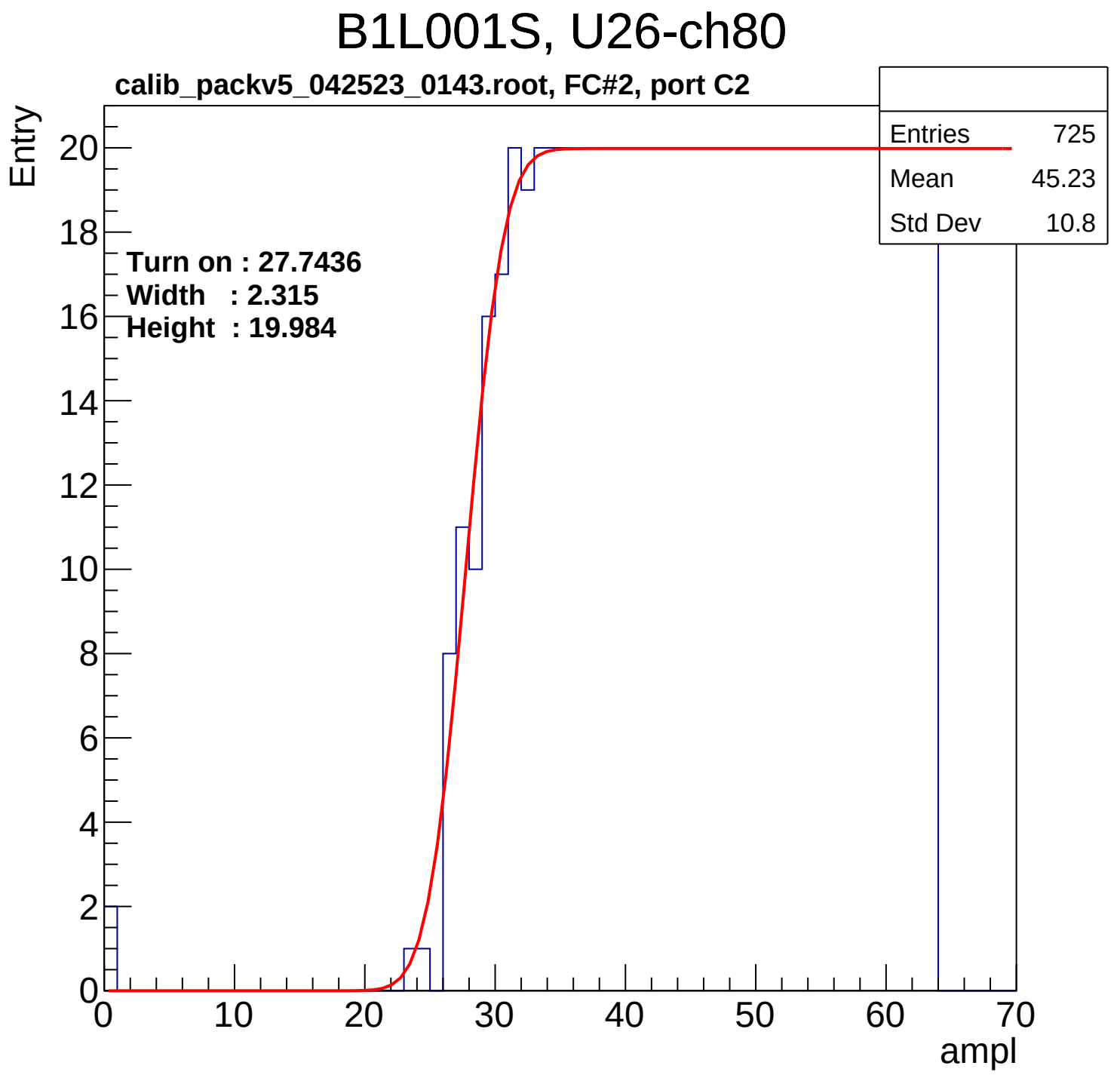

B1L001S, U26-ch75
calib_packv5_042523_0143.root, FC#2, port C2
Entries 735
Mean 44.89
Std Dev 11.14
Turn on : 27.7407
Width : 3.389
Height : 20.112
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

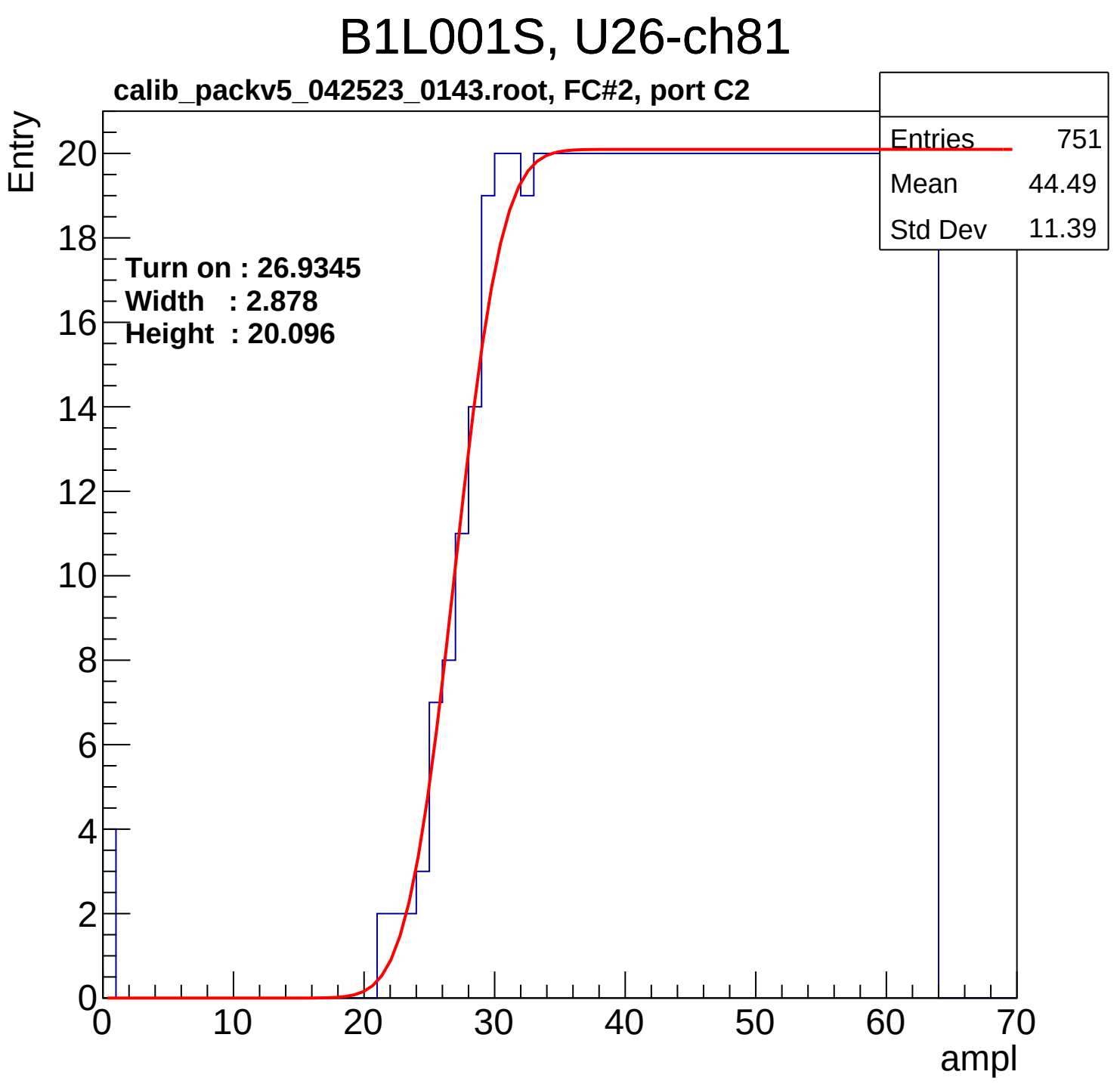

B1L001S, U26-ch76
calib_packv5_042523_0143.root, FC#2, port C2
Entries 749
Mean 44.55
Std Dev 11.3
Turn on : 26.7915
Width : 2.876
Height : 19.966
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

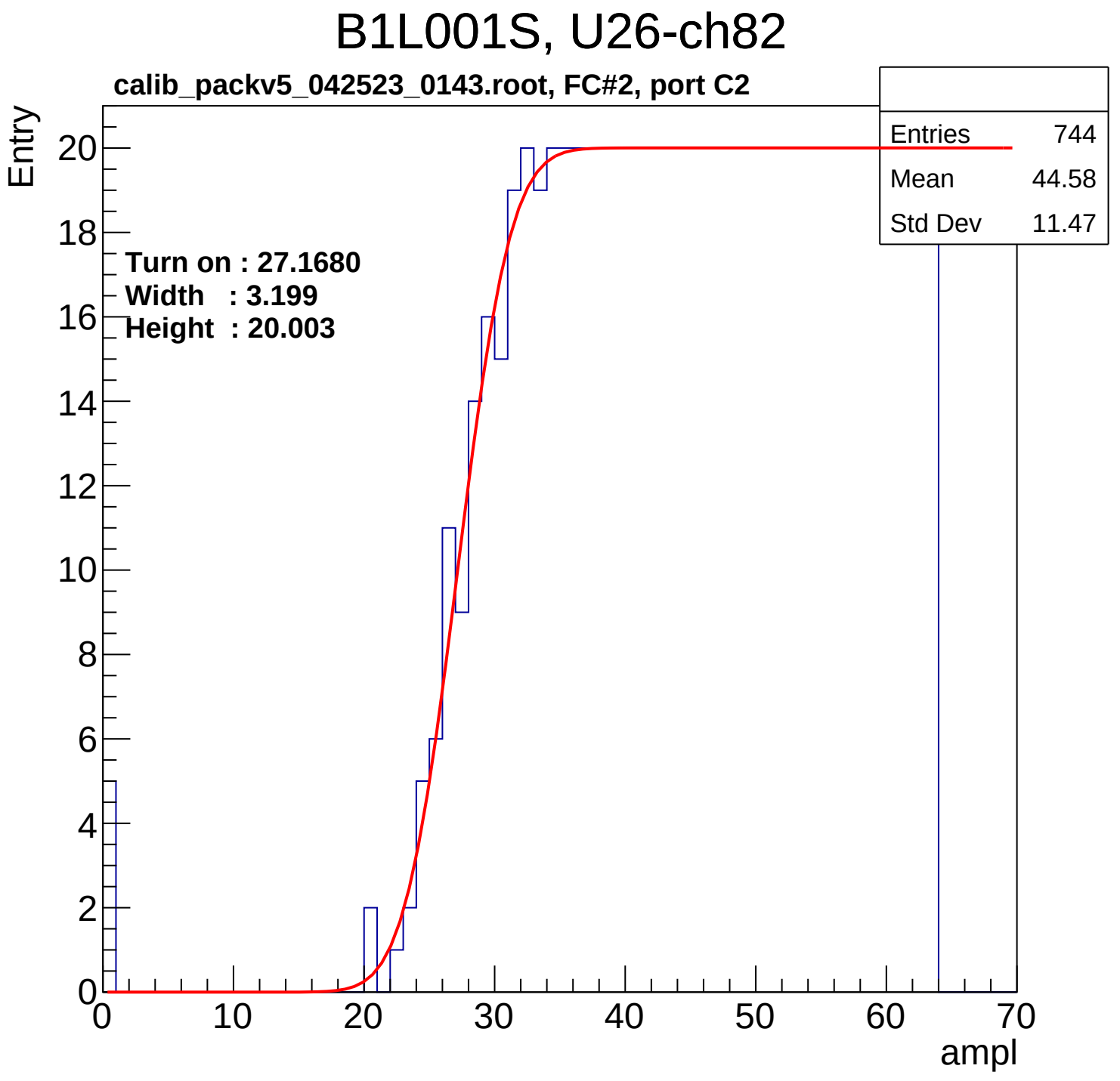

B1L001S, U26-ch77
calib_packv5_042523_0143.root, FC#2, port C2
Entries 722
Mean 45.26
Std Dev 10.88
Turn on : 28.2880
Width : 1.983
Height : 19.999
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

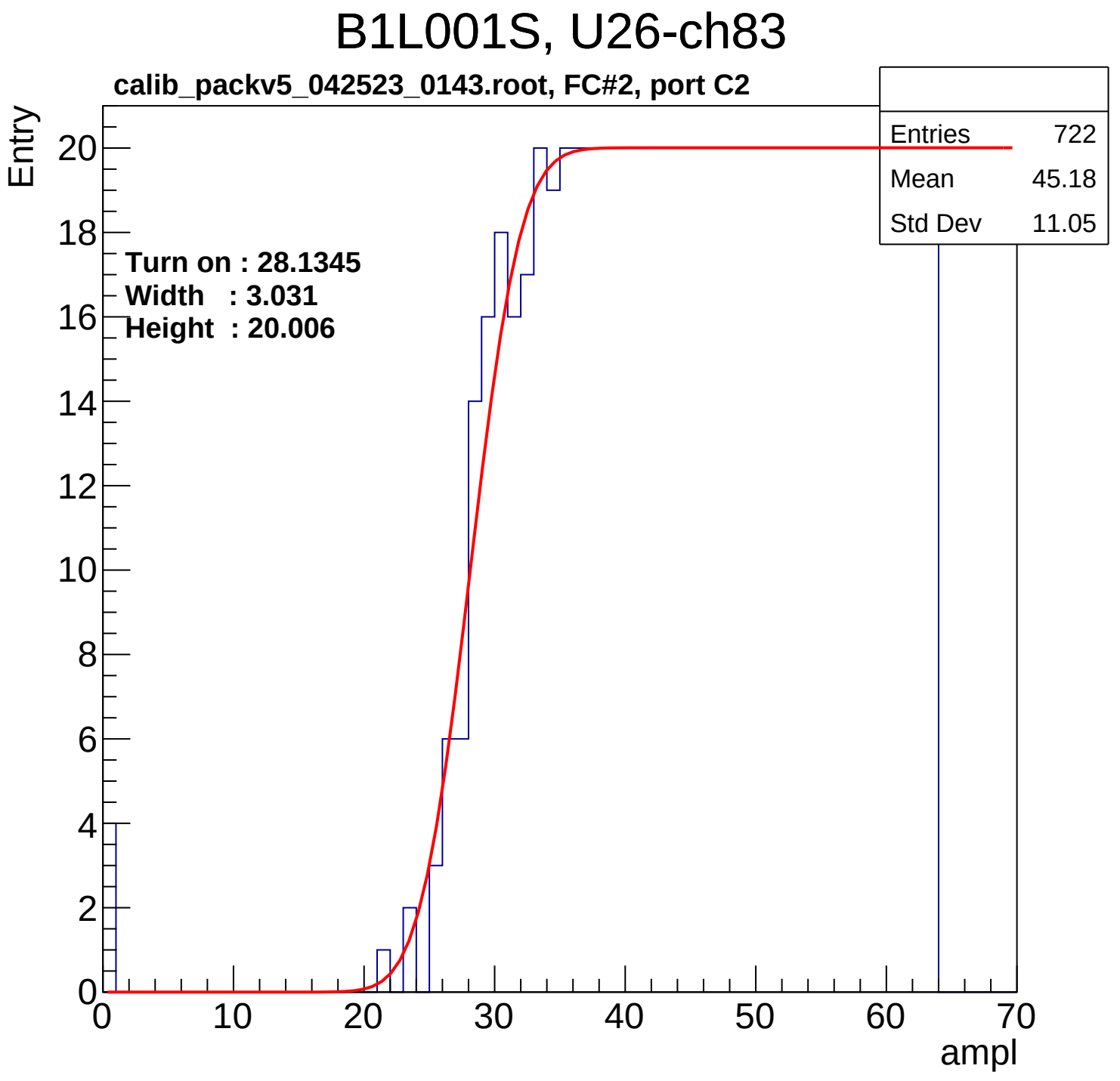

B1L001S, U26-ch78
calib_packv5_042523_0143.root, FC#2, port C2
Entries 730
Mean 45.02
Std Dev 11.05
Turn on : 27.9951
Width : 3.405
Height : 20.129
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

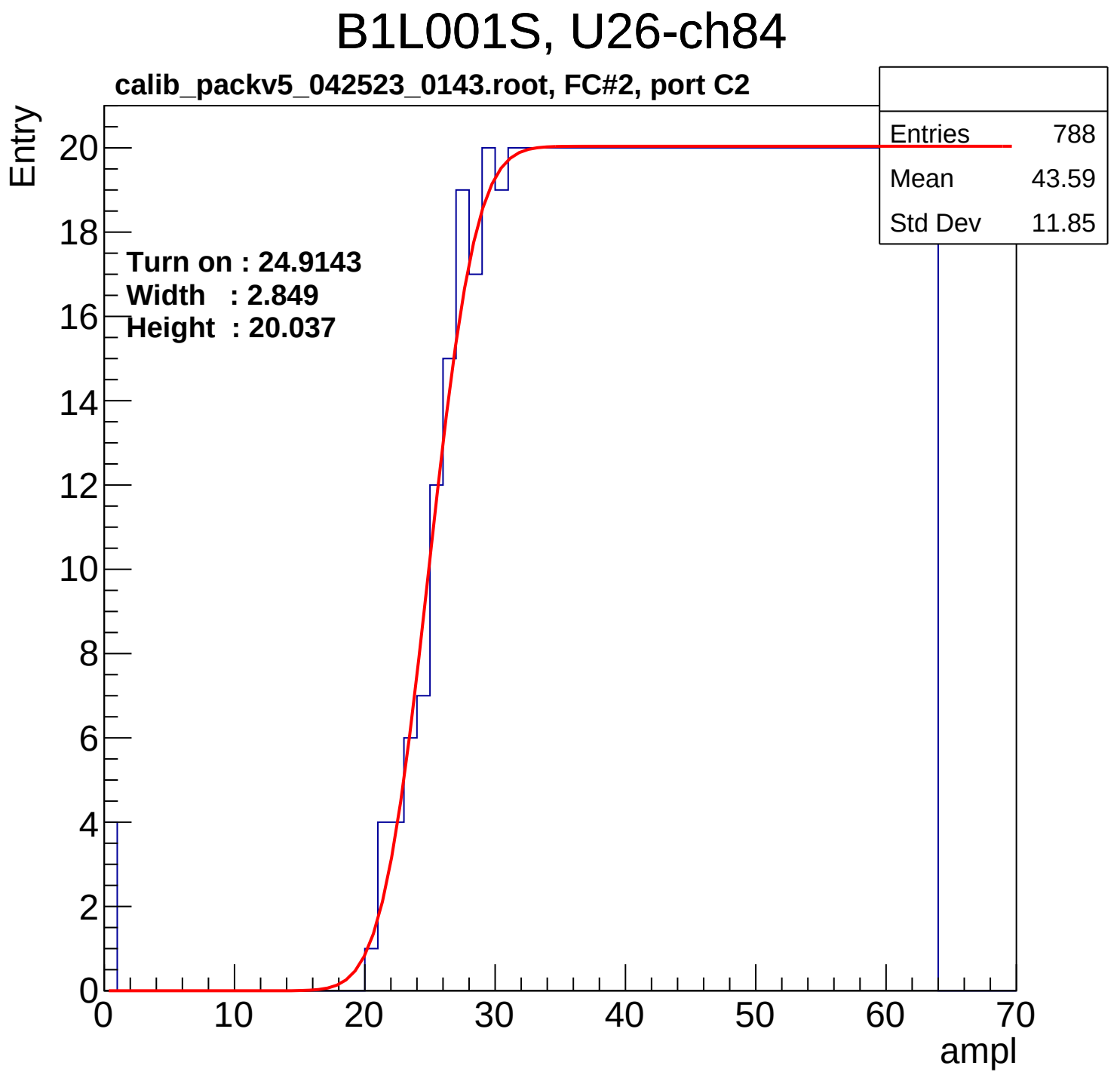

B1L001S, U26-ch79
calib_packv5_042523_0143.root, FC#2, port C2
Entries 696
Mean 45.84
Std Dev 10.71
Turn on : 29.8026
Width : 3.219
Height : 20.171
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

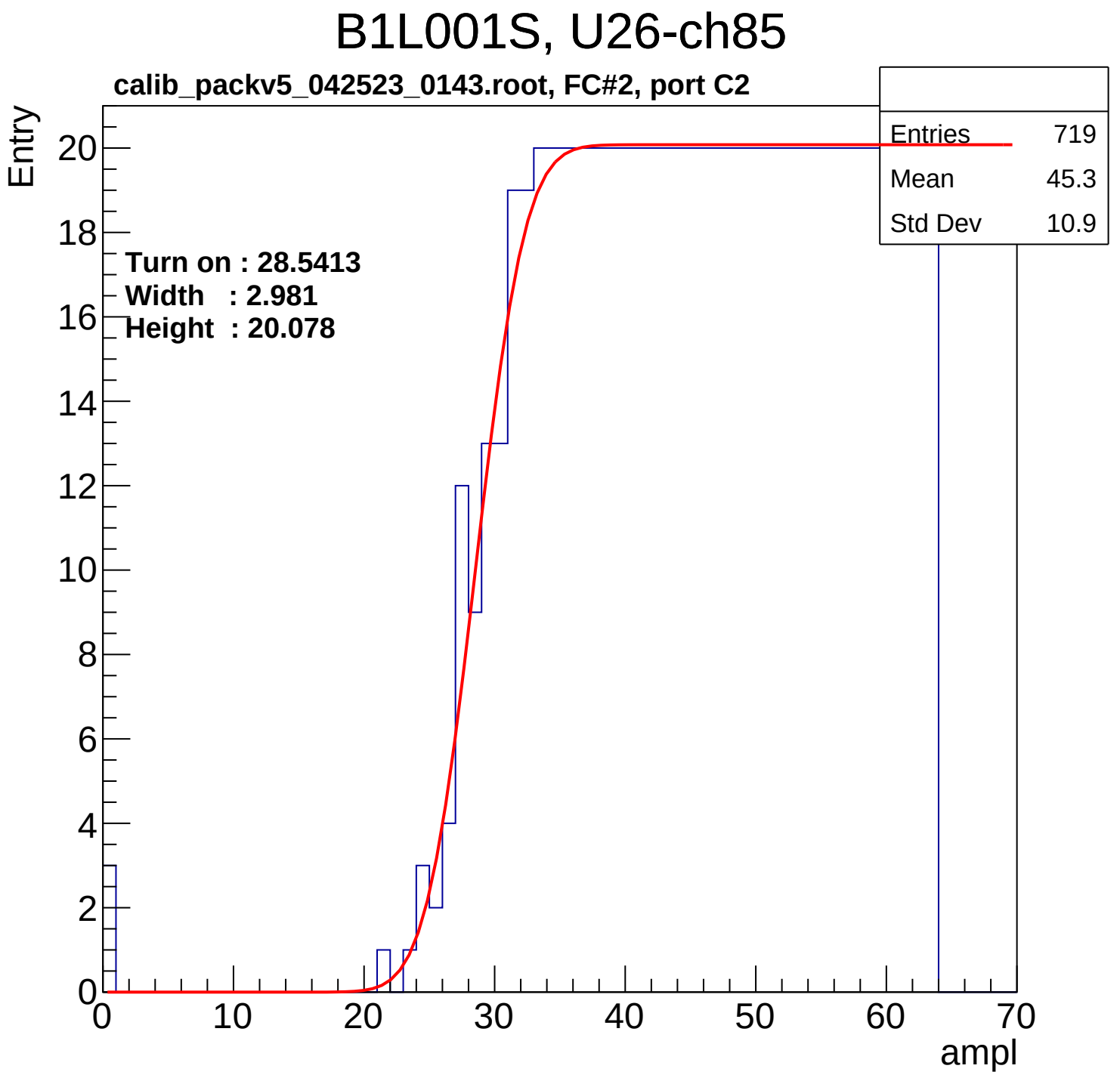

B1L001S, U26-ch80
calib_packv5_042523_0143.root, FC#2, port C2
Entries 725
Mean 45.23
Std Dev 10.8
Turn on : 27.7436
Width : 2.315
Height : 19.984
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

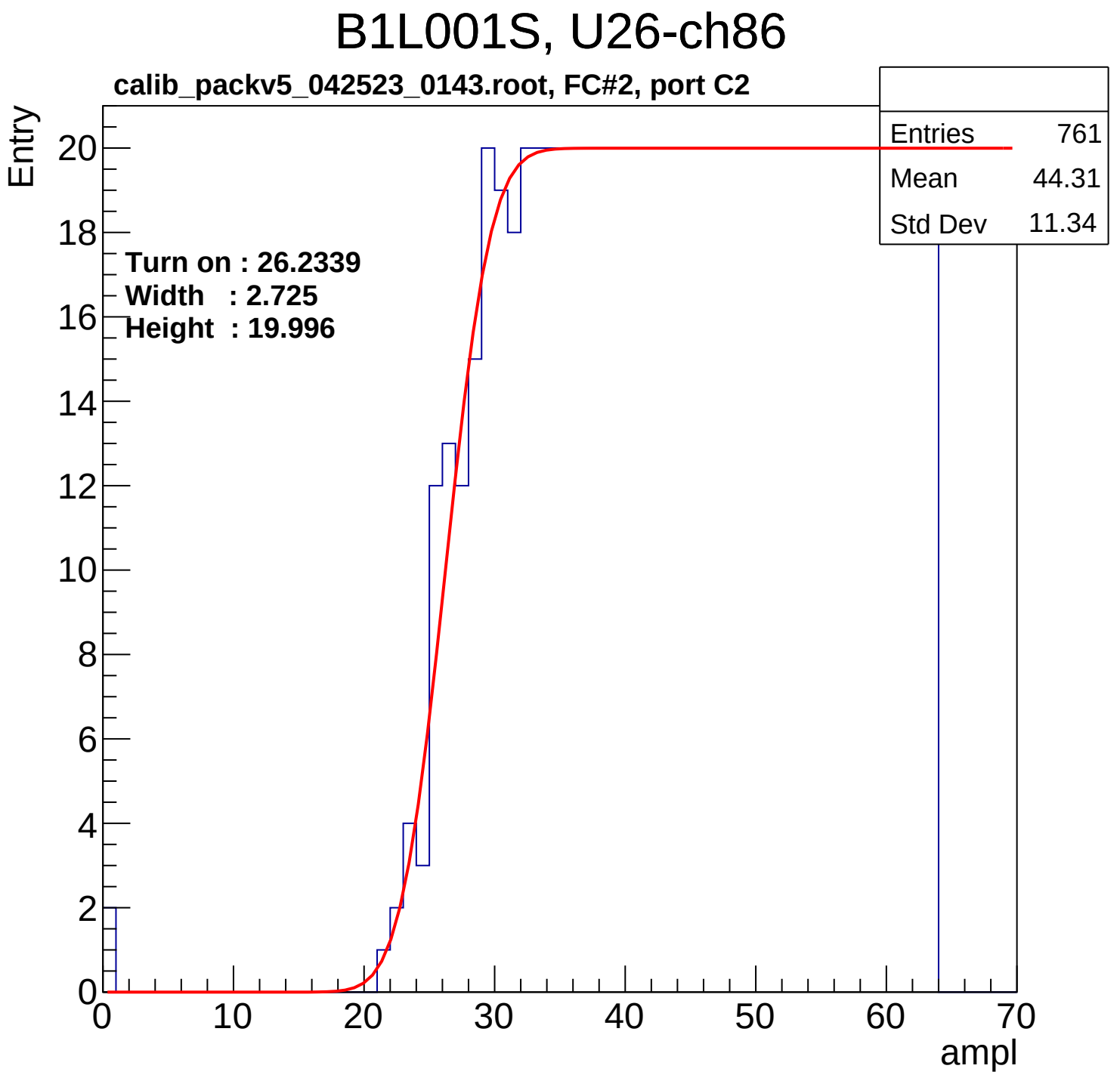

B1L001S, U26-ch81
calib_packv5_042523_0143.root, FC#2, port C2
Entries 751
Mean 44.49
Std Dev 11.39
Turn on : 26.9345
Width : 2.878
Height : 20.096
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

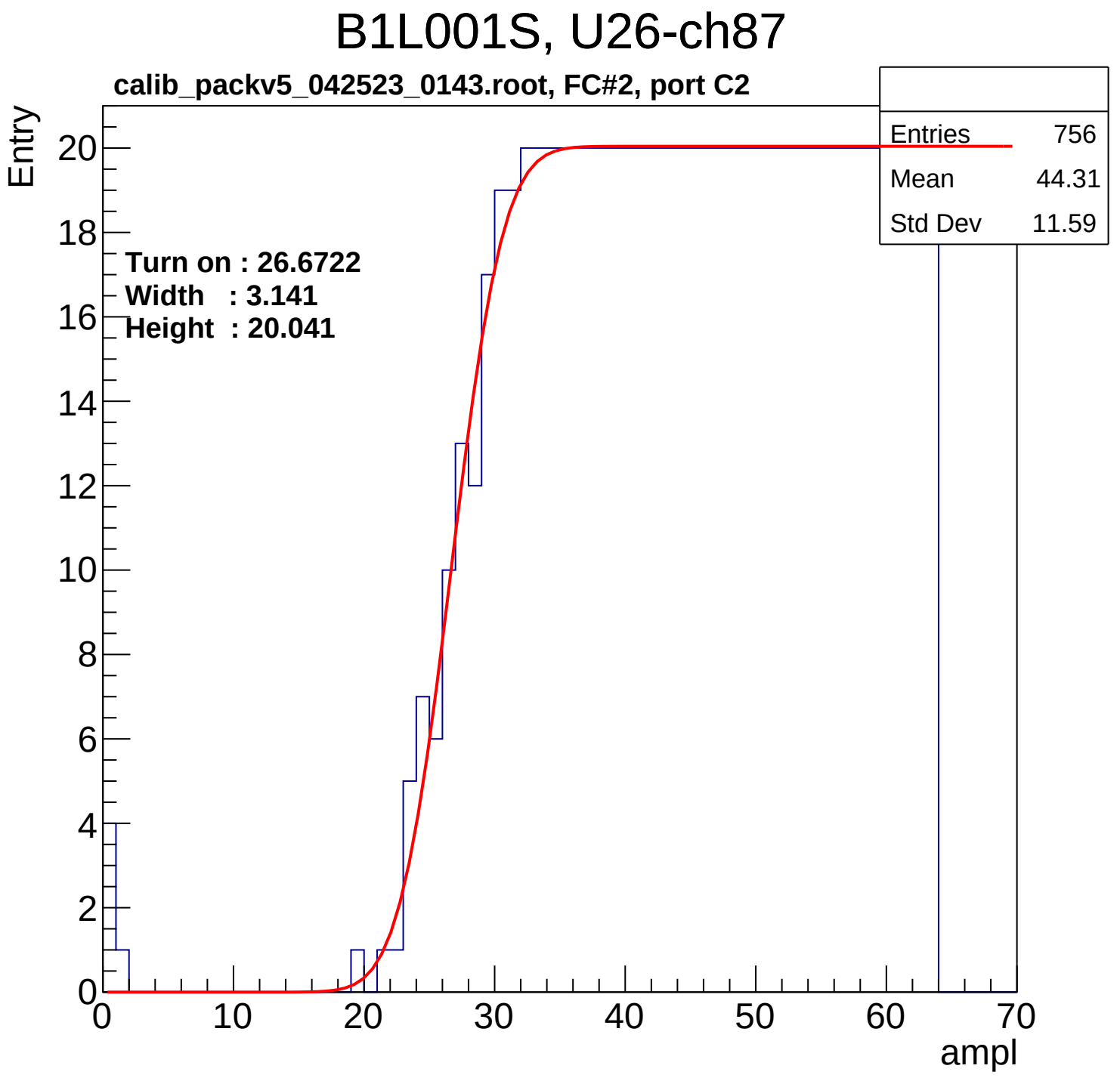

B1L001S, U26-ch82
calib_packv5_042523_0143.root, FC#2, port C2
Entries 744
Mean 44.58
Std Dev 11.47
Turn on : 27.1680
Width : 3.199
Height : 20.003
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

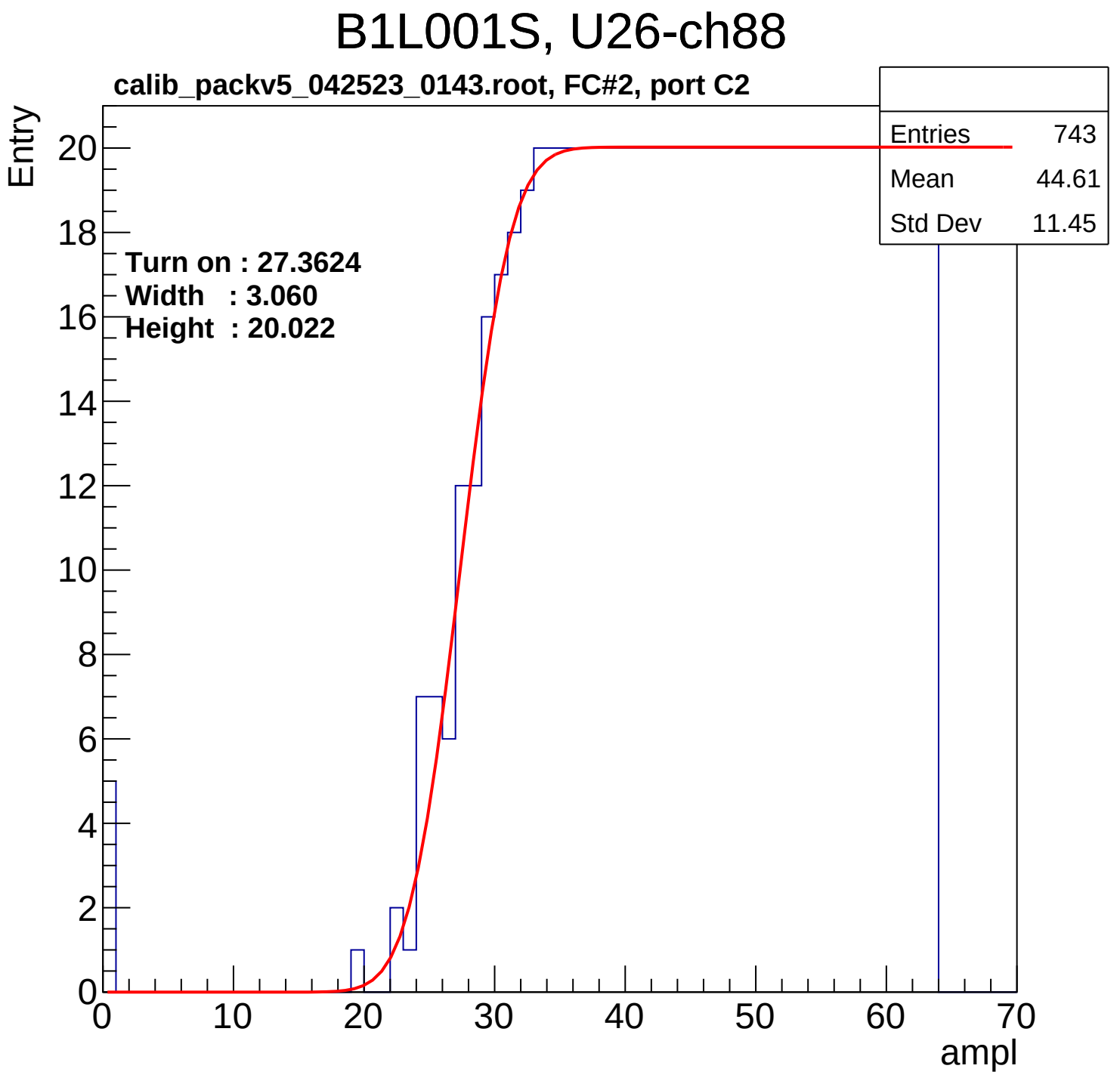

B1L001S, U26-ch83
calib_packv5_042523_0143.root, FC#2, port C2
Entries 722
Mean 45.18
Std Dev 11.05
Turn on : 28.1345
Width : 3.031
Height : 20.006
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

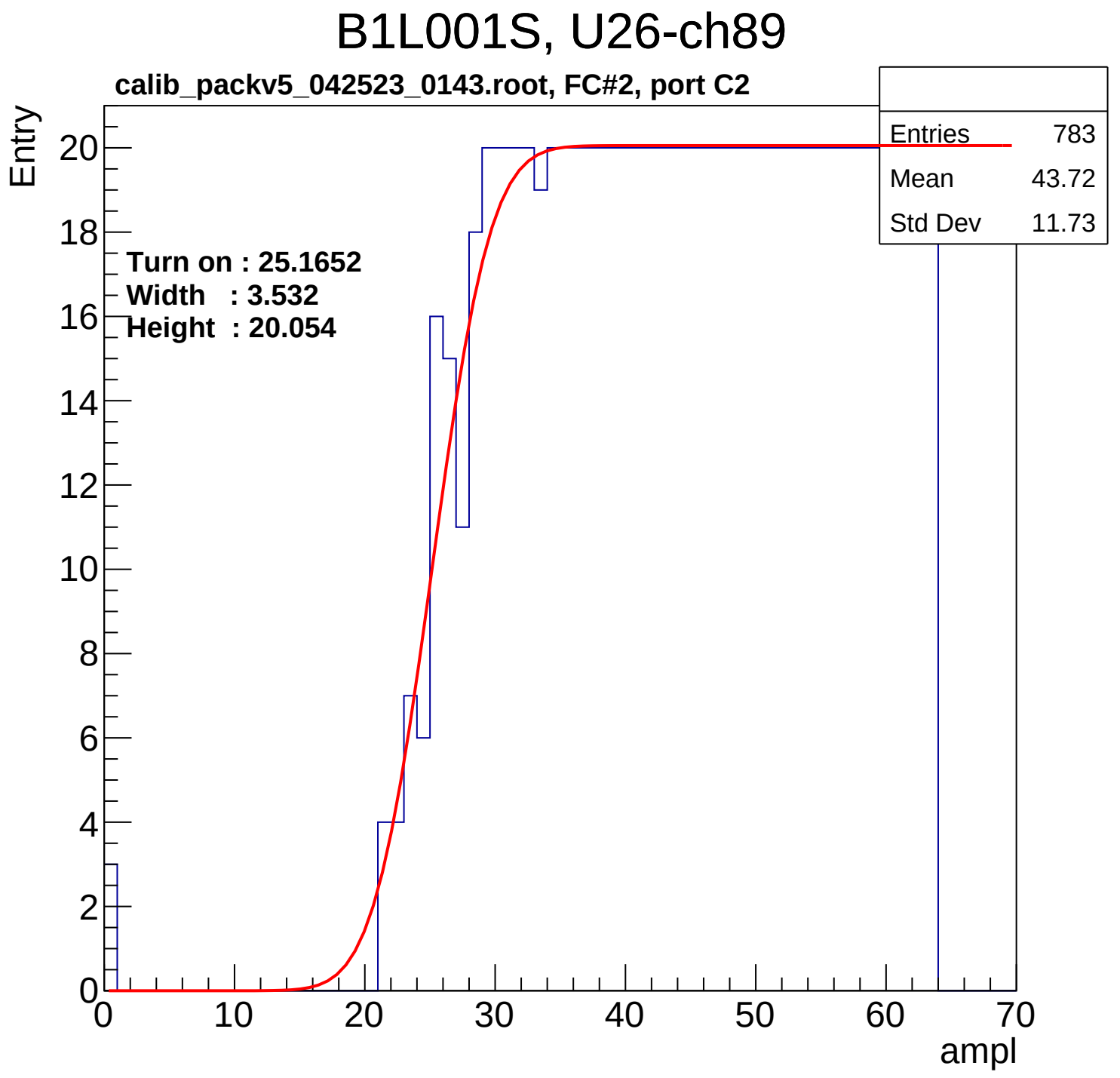

B1L001S, U26-ch84
calib_packv5_042523_0143.root, FC#2, port C2
Entries 788
Mean 43.59
Std Dev 11.85
Turn on : 24.9143
Width : 2.849
Height : 20.037
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

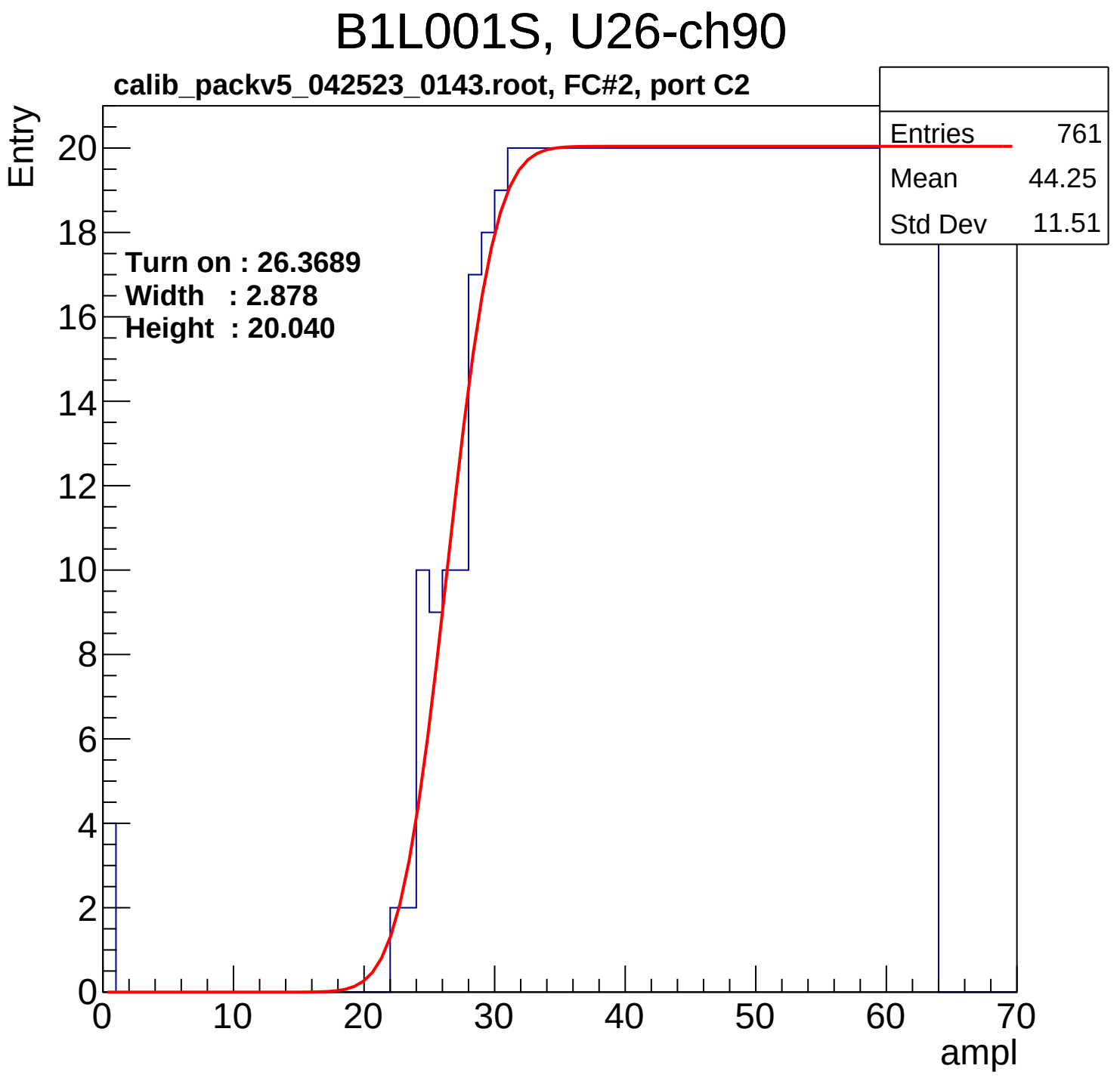

B1L001S, U26-ch85
calib_packv5_042523_0143.root, FC#2, port C2
Entries 719
Mean 45.3
Std Dev 10.9
Turn on : 28.5413
Width : 2.981
Height : 20.078
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

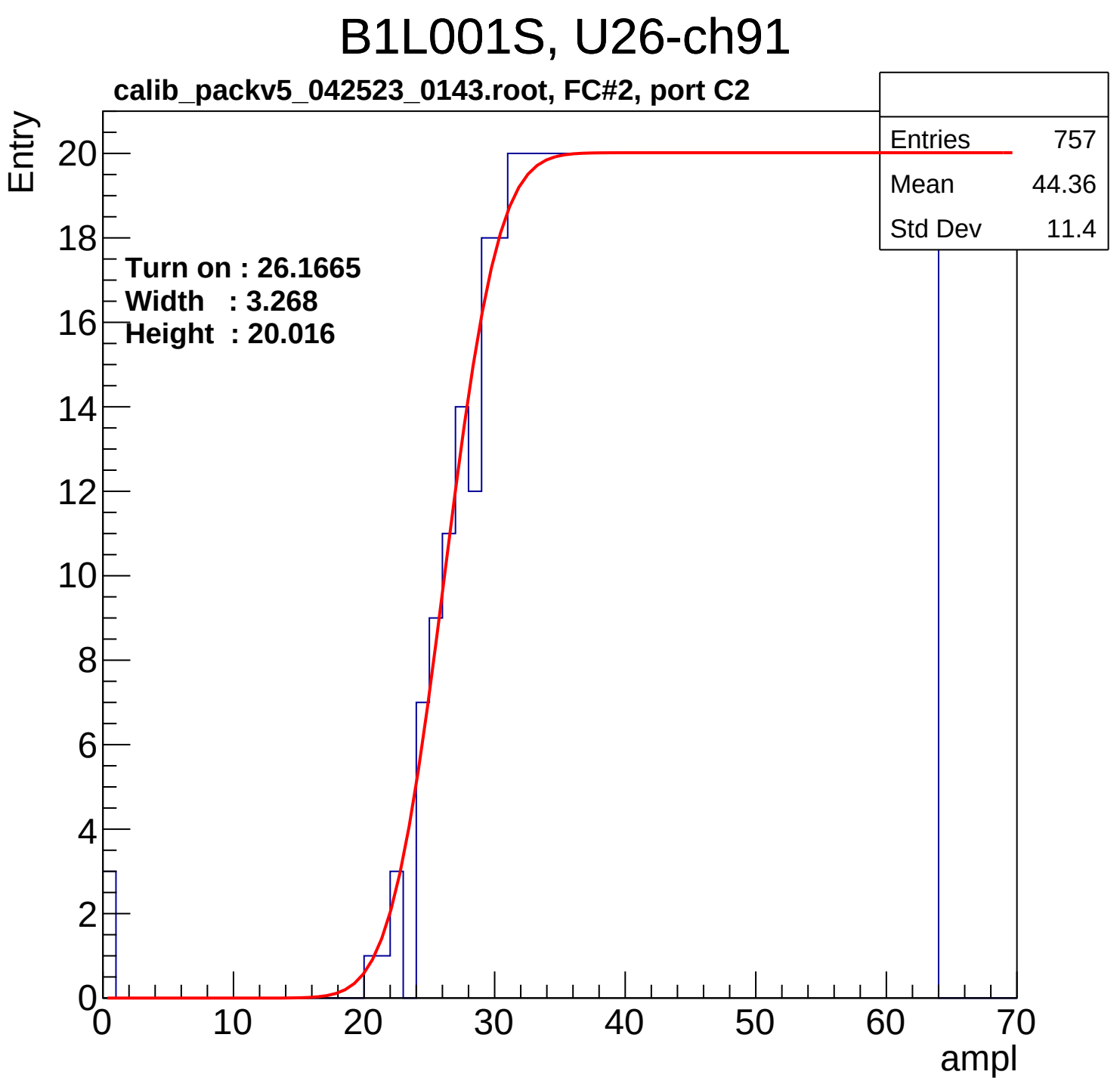

B1L001S, U26-ch86
calib_packv5_042523_0143.root, FC#2, port C2
Entries 761
Mean 44.31
Std Dev 11.34
Turn on : 26.2339
Width : 2.725
Height : 19.996
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

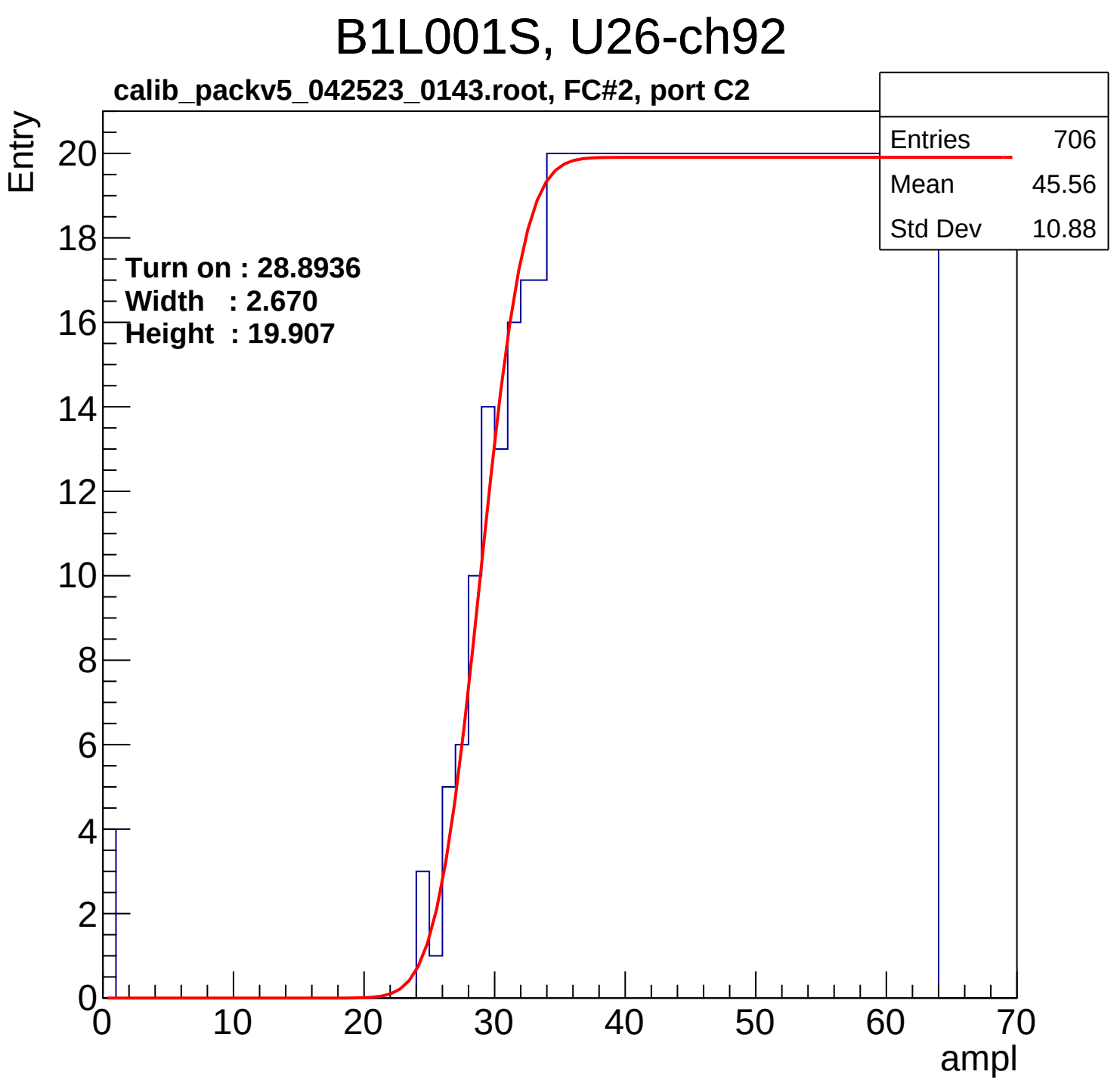

B1L001S, U26-ch87
calib_packv5_042523_0143.root, FC#2, port C2
Entries 756
Mean 44.31
Std Dev 11.59
Turn on : 26.6722
Width : 3.141
Height : 20.041
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

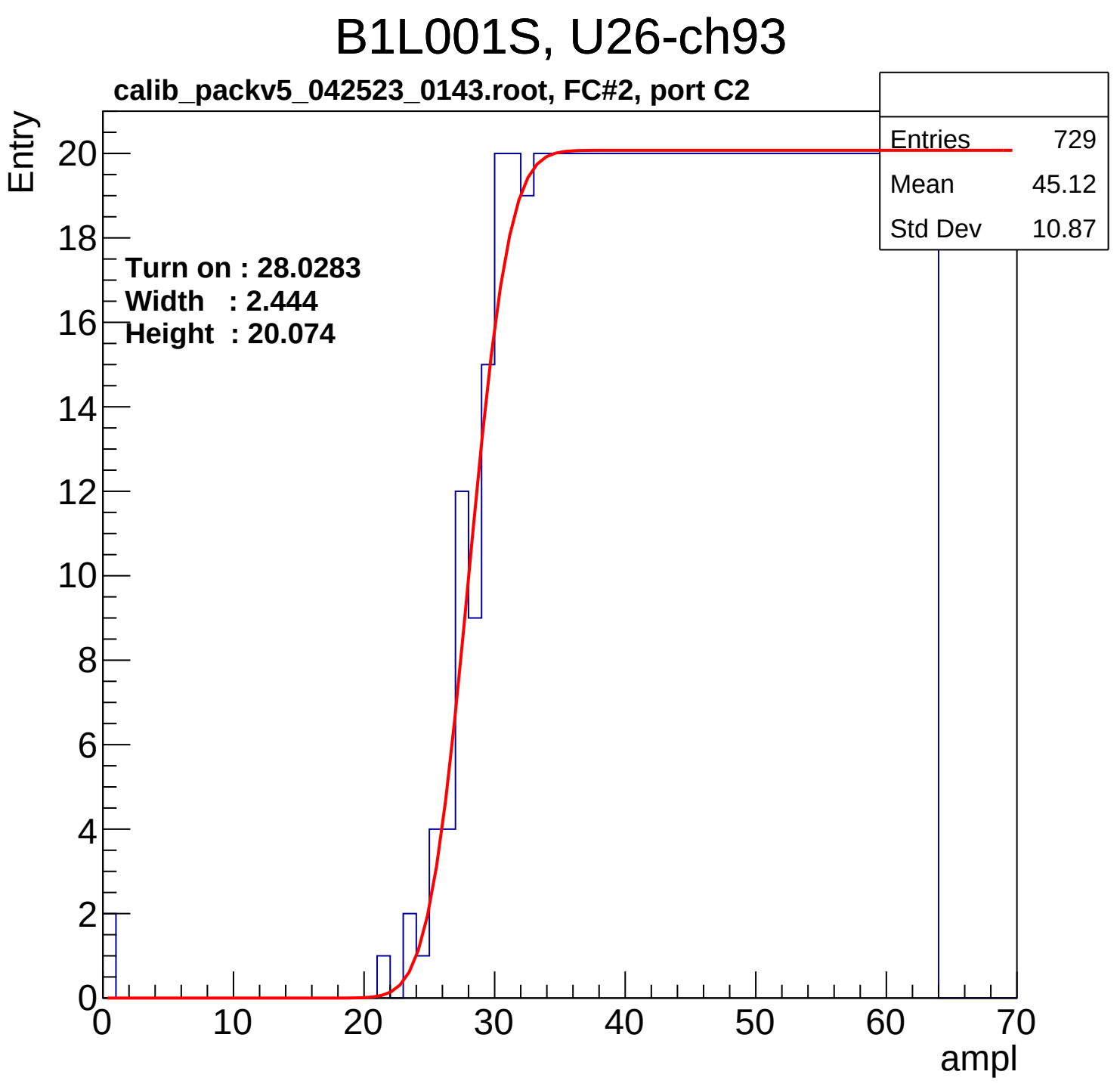

B1L001S, U26-ch88
calib_packv5_042523_0143.root, FC#2, port C2
Entries 743
Mean 44.61
Std Dev 11.45
Turn on : 27.3624
Width : 3.060
Height : 20.022
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

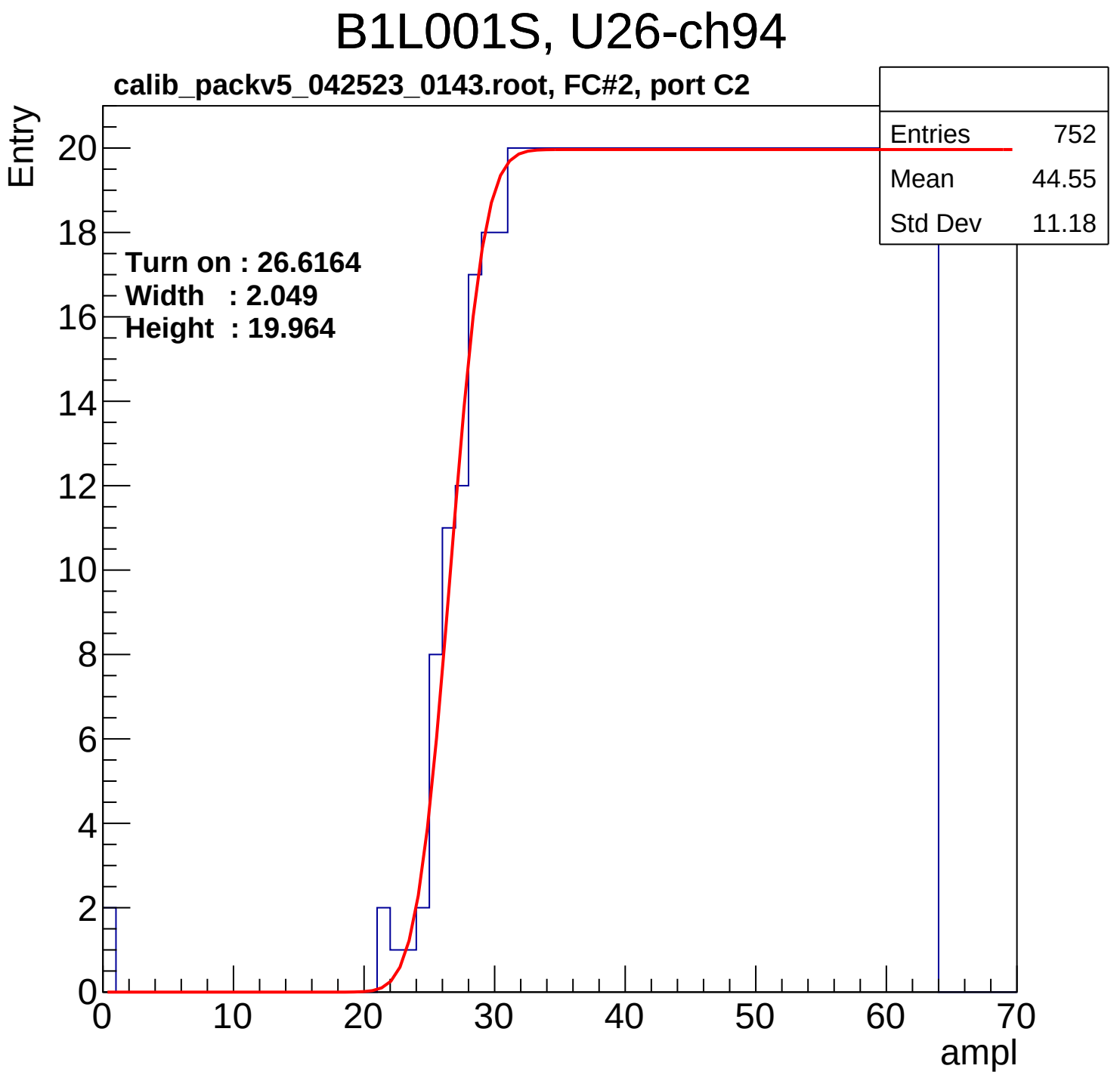

B1L001S, U26-ch89
calib_packv5_042523_0143.root, FC#2, port C2
Entries 783
Mean 43.72
Std Dev 11.73
Turn on : 25.1652
Width : 3.532
Height : 20.054
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

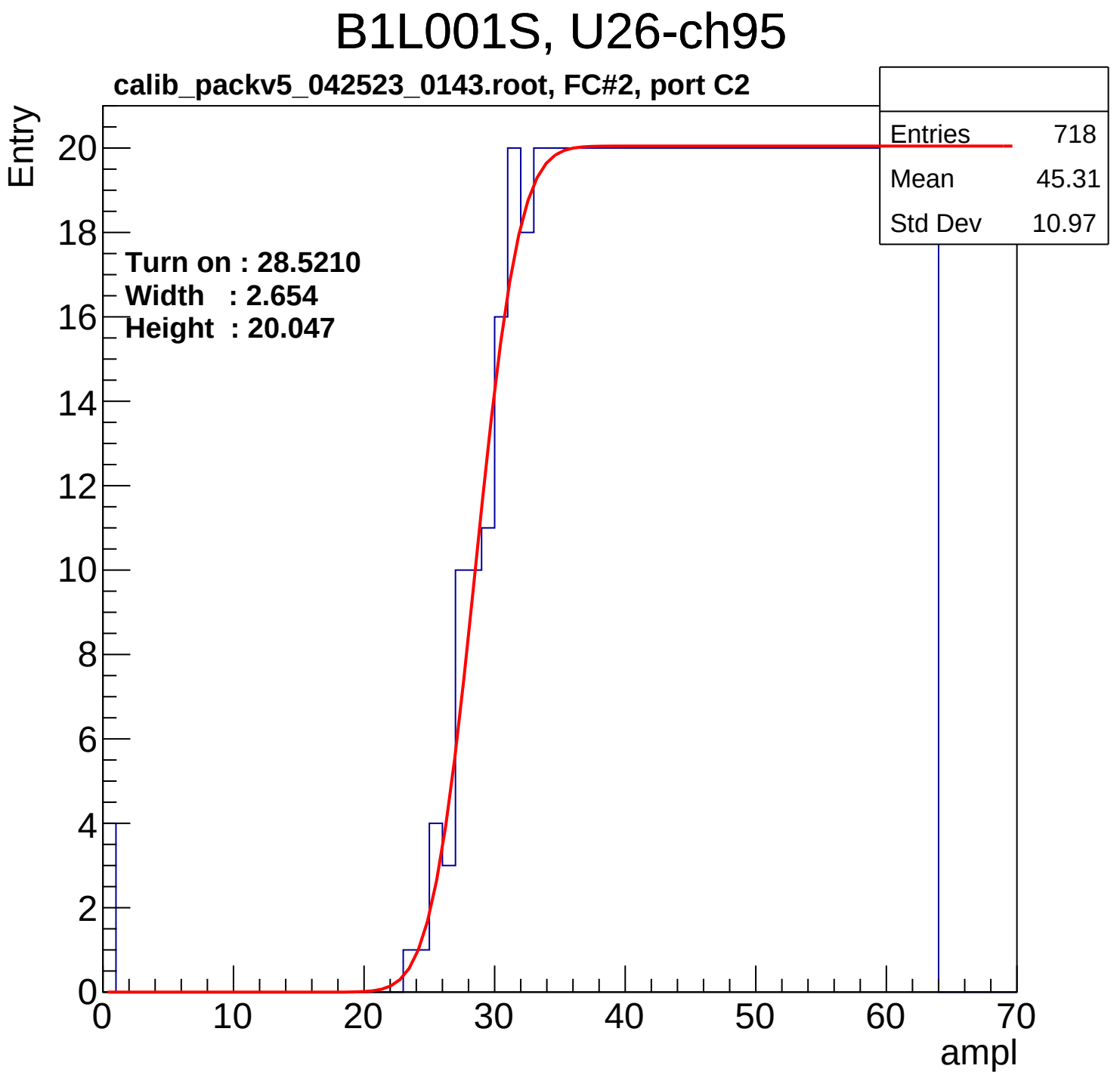

B1L001S, U26-ch90
calib_packv5_042523_0143.root, FC#2, port C2
Entries 761
Mean 44.25
Std Dev 11.51
Turn on : 26.3689
Width : 2.878
Height : 20.040
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

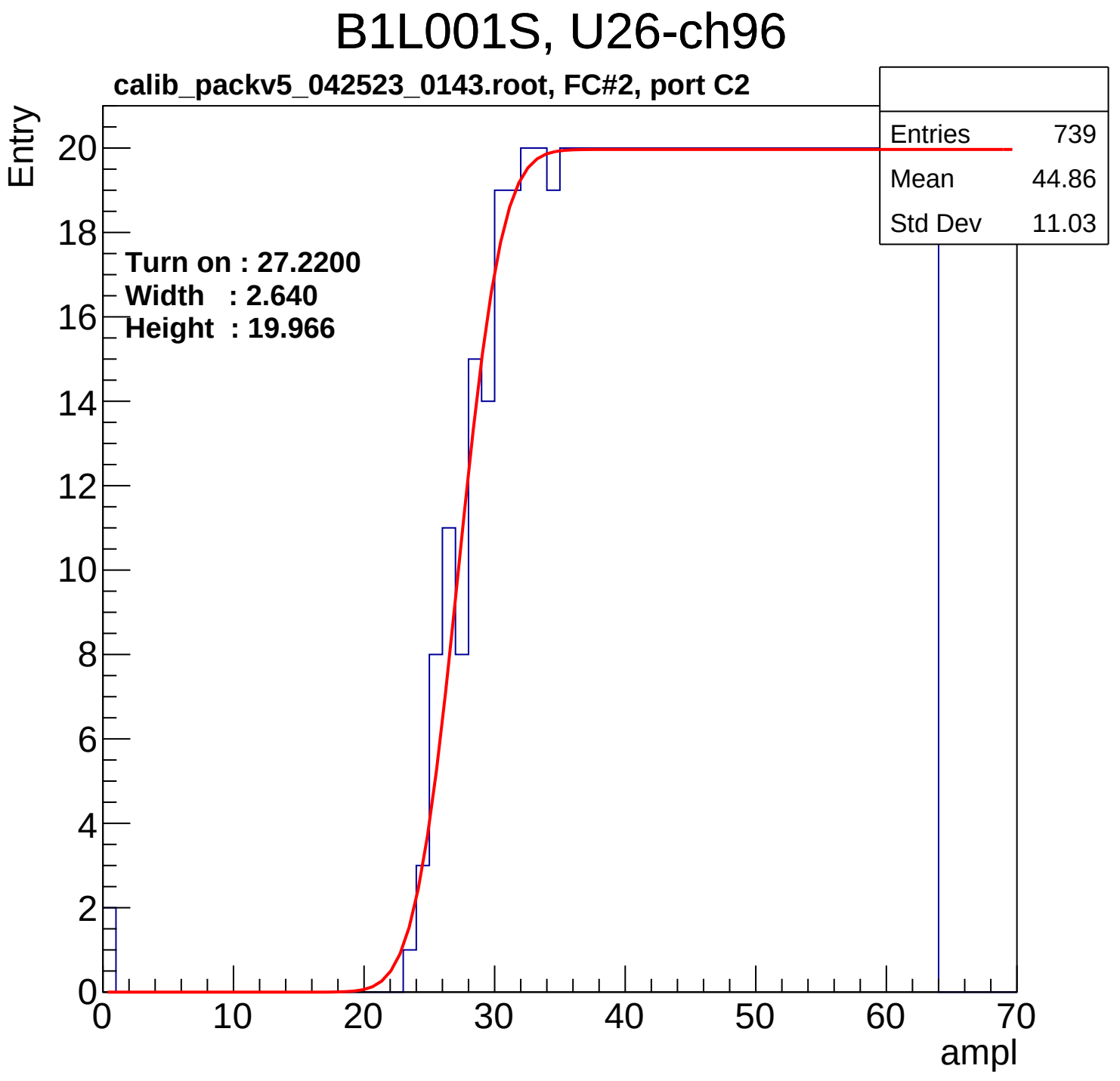

B1L001S, U26-ch91
calib_packv5_042523_0143.root, FC#2, port C2
Entries 757
Mean 44.36
Std Dev 11.4
Turn on : 26.1665
Width : 3.268
Height : 20.016
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

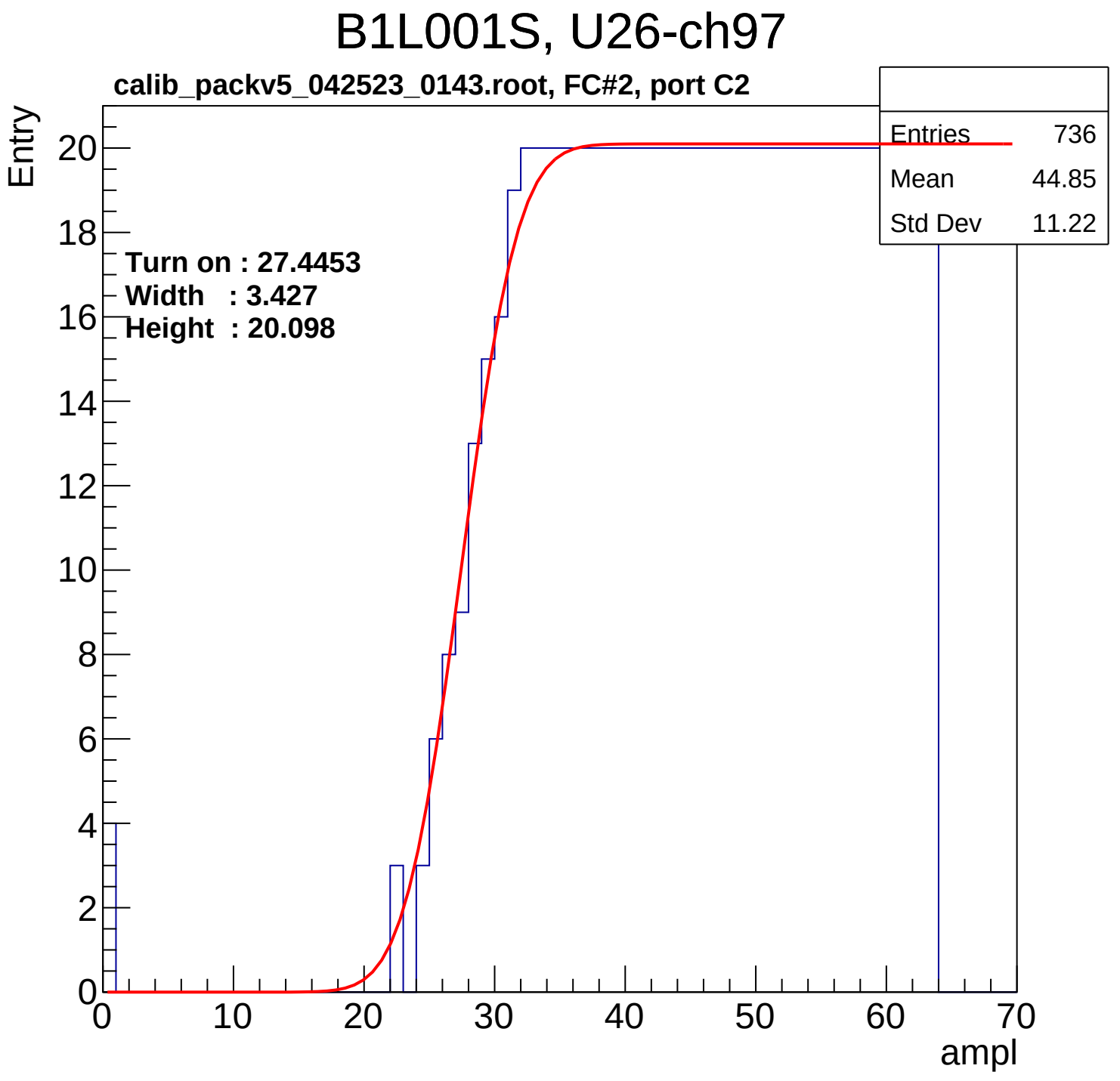

B1L001S, U26-ch92
calib_packv5_042523_0143.root, FC#2, port C2
Entries 706
Mean 45.56
Std Dev 10.88
Turn on : 28.8936
Width : 2.670
Height : 19.907
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

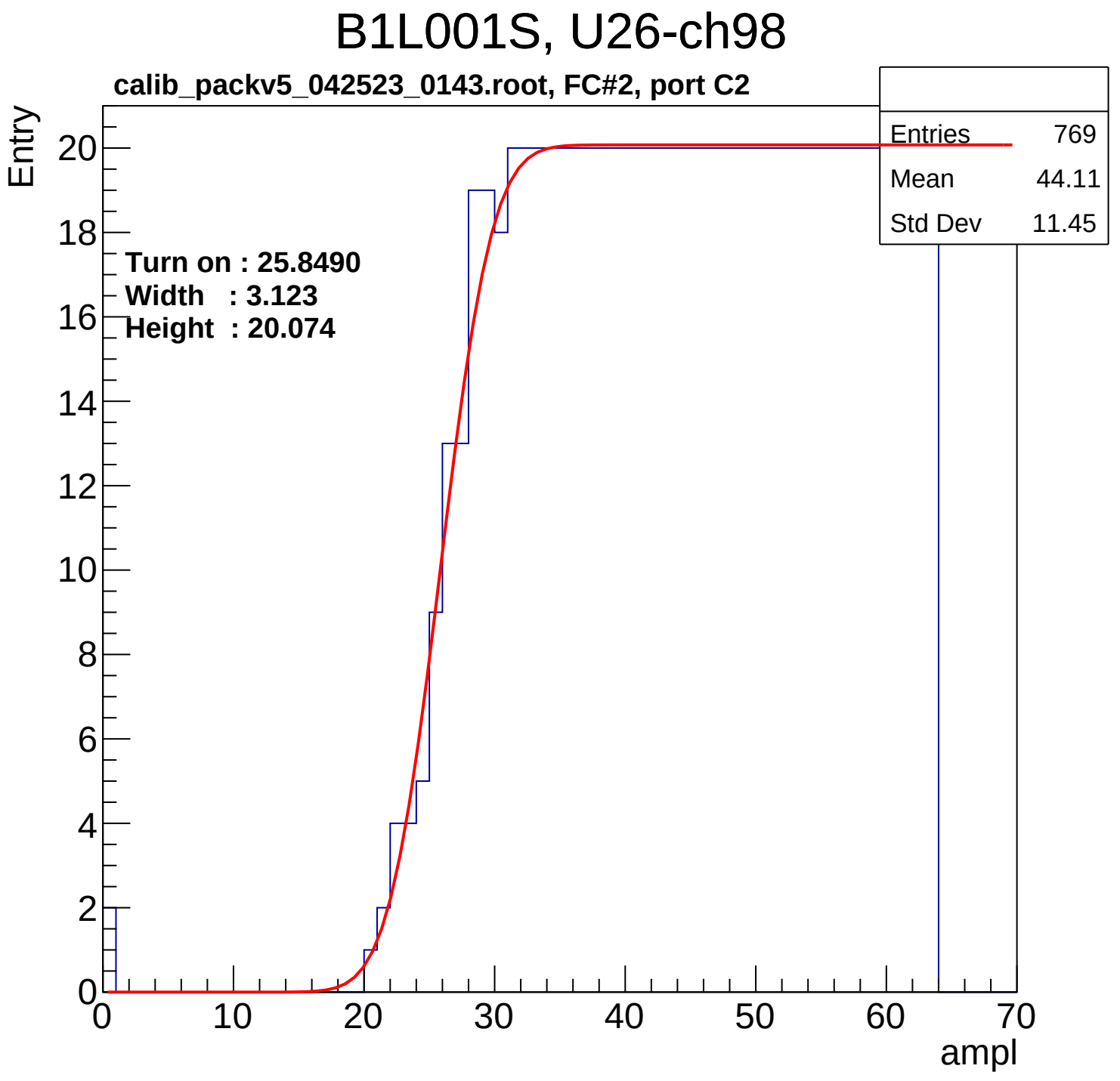

B1L001S, U26-ch93
calib_packv5_042523_0143.root, FC#2, port C2
Entries 729
Mean 45.12
Std Dev 10.87
Turn on : 28.0283
Width : 2.444
Height : 20.074
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

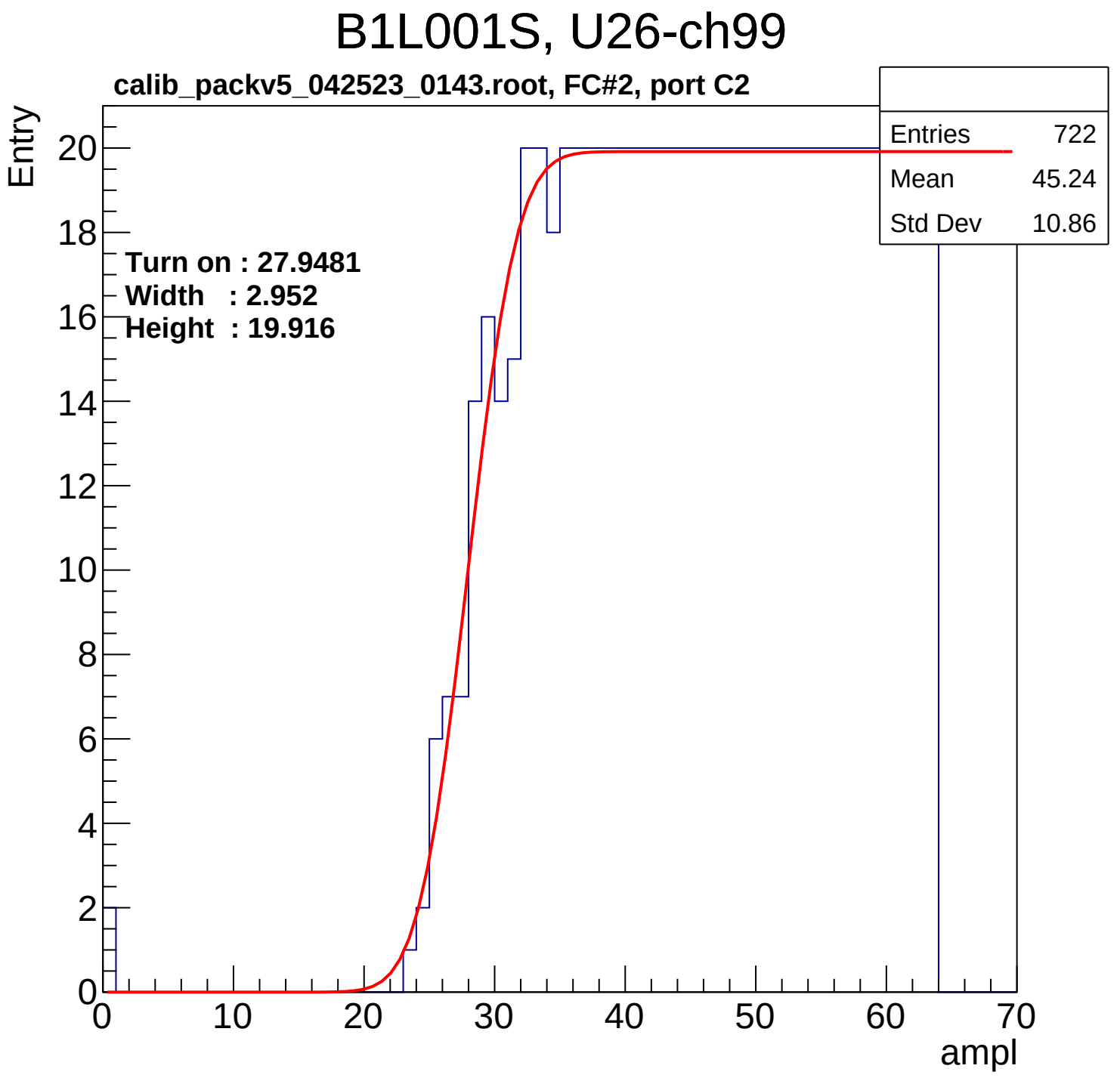

B1L001S, U26-ch94
calib_packv5_042523_0143.root, FC#2, port C2
Entries 752
Mean 44.55
Std Dev 11.18
Turn on : 26.6164
Width : 2.049
Height : 19.964
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

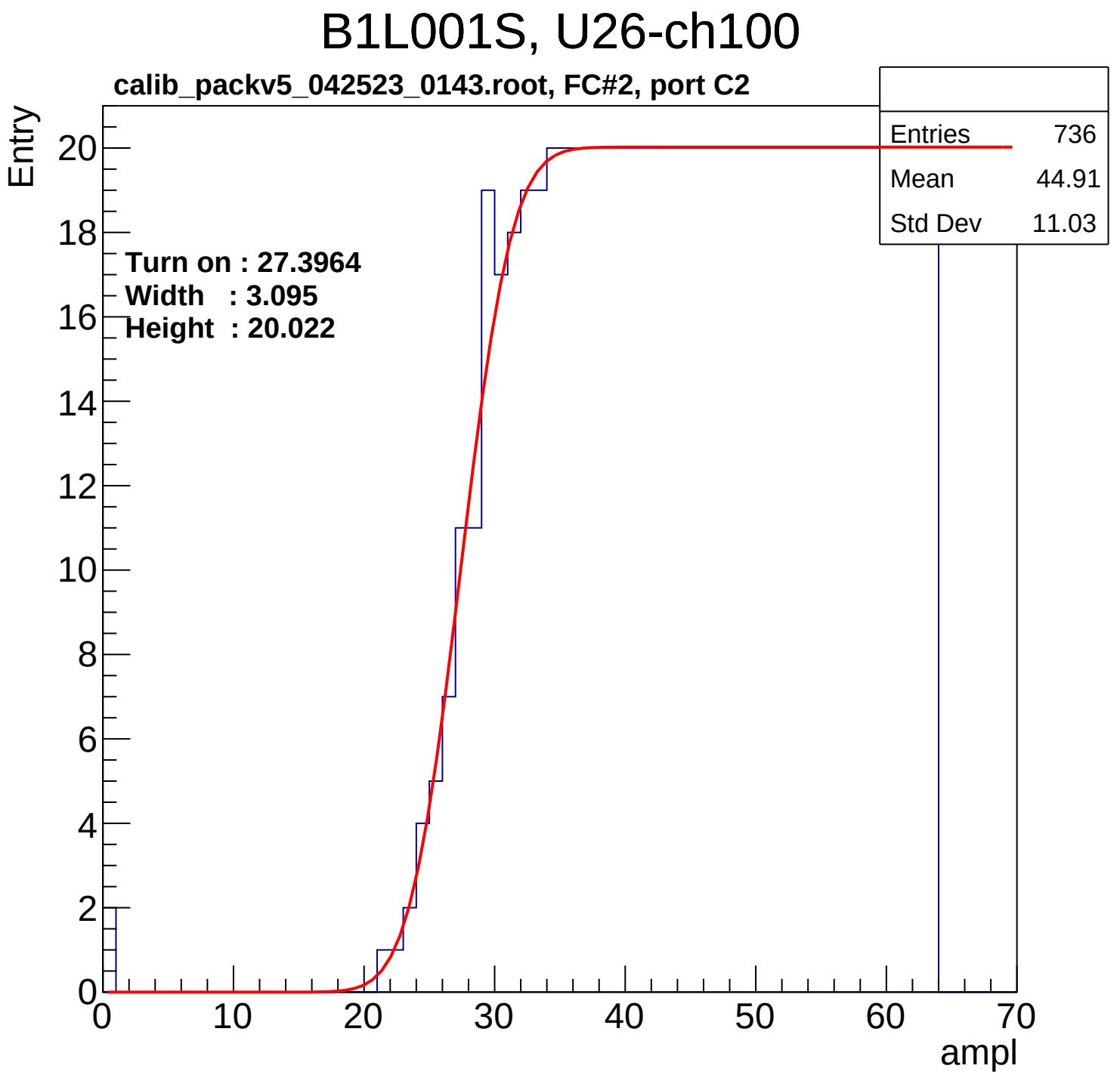

B1L001S, U26-ch95
calib_packv5_042523_0143.root, FC#2, port C2
Entries 718
Mean 45.31
Std Dev 10.97
Turn on : 28.5210
Width : 2.654
Height : 20.047
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

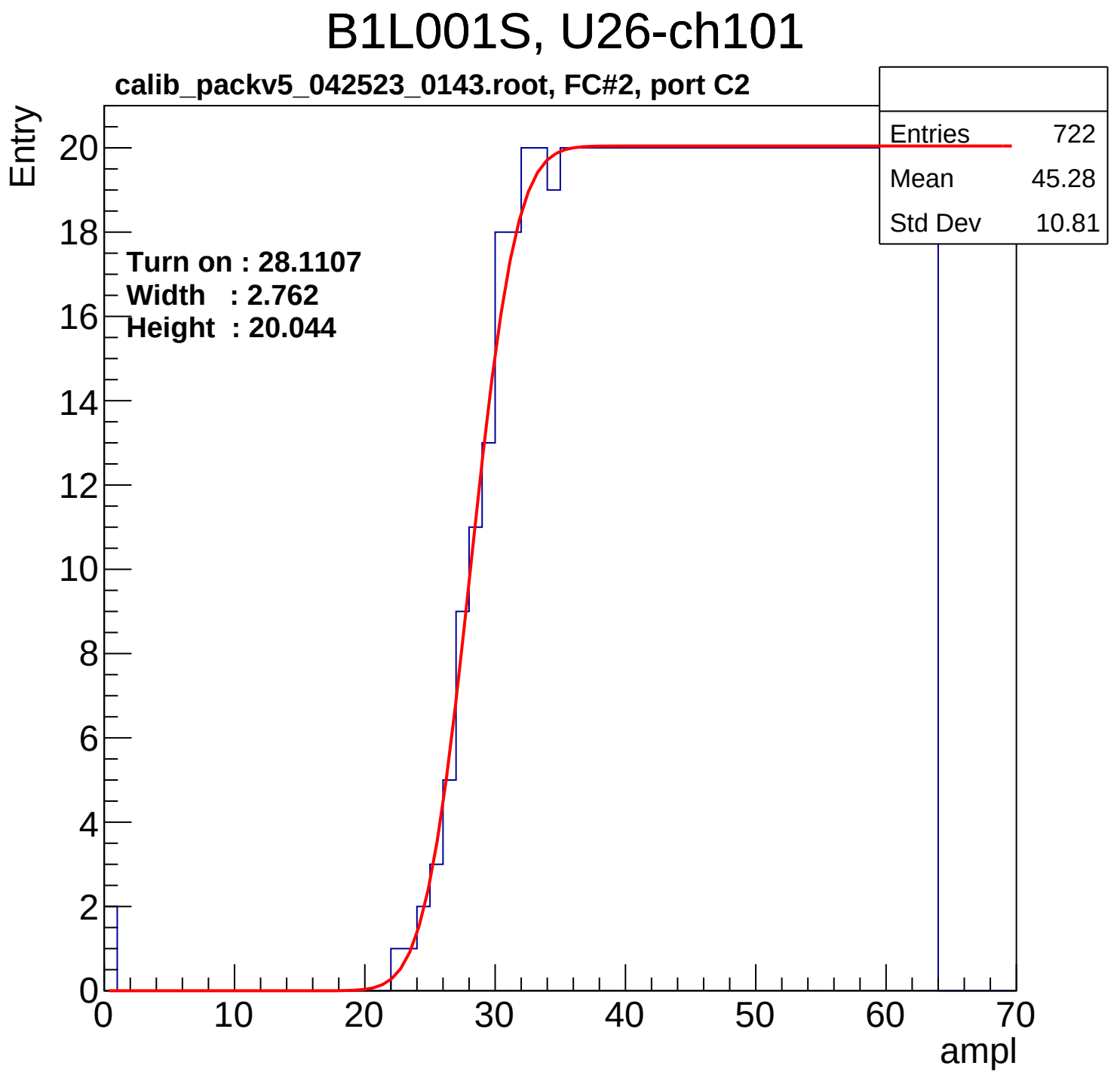

B1L001S, U26-ch96
calib_packv5_042523_0143.root, FC#2, port C2
Entries 739
Mean 44.86
Std Dev 11.03
Turn on : 27.2200
Width : 2.640
Height : 19.966
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

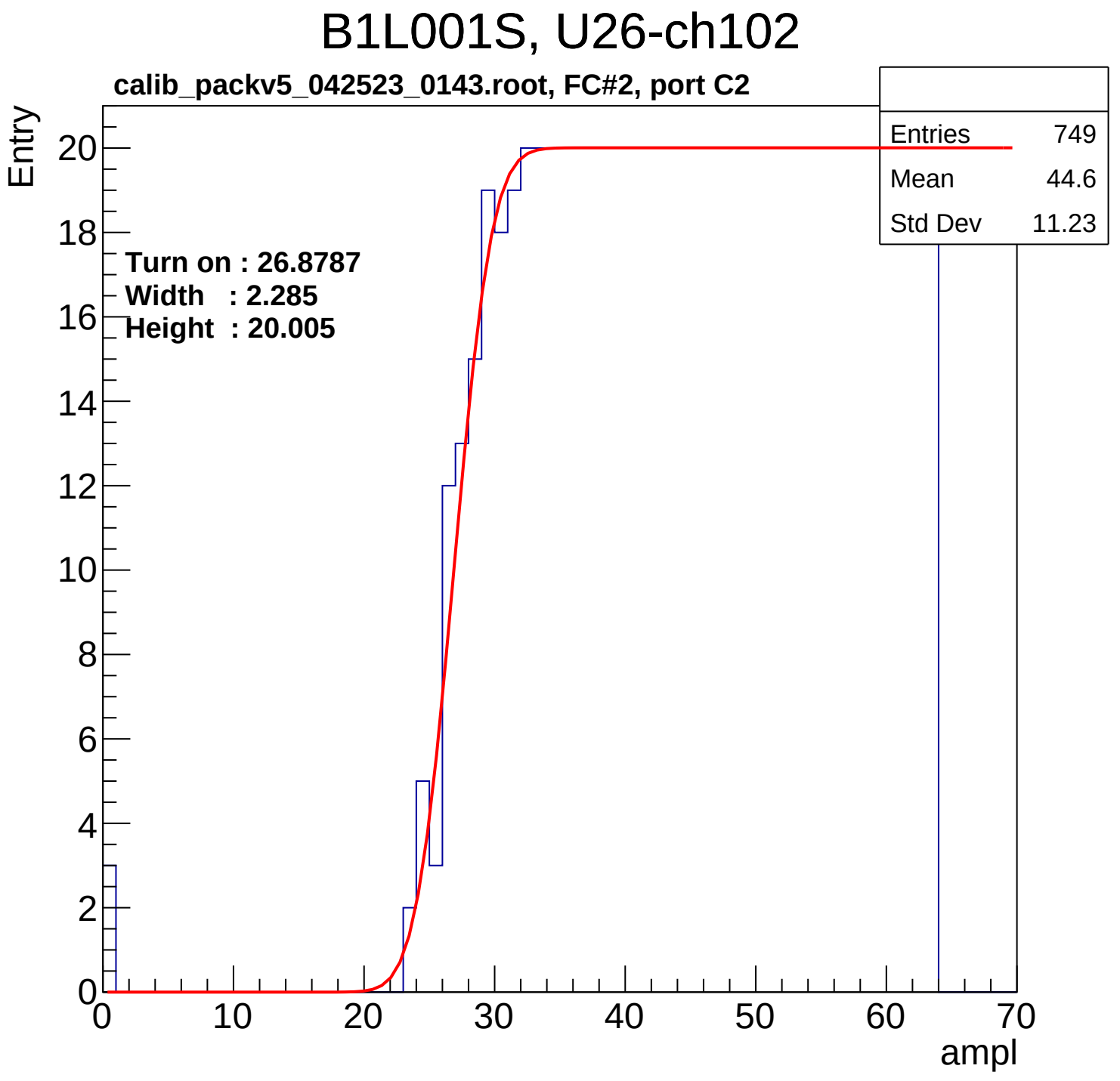

B1L001S, U26-ch97
calib_packv5_042523_0143.root, FC#2, port C2
Entries 736
Mean 44.85
Std Dev 11.22
Turn on : 27.4453
Width : 3.427
Height : 20.098
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

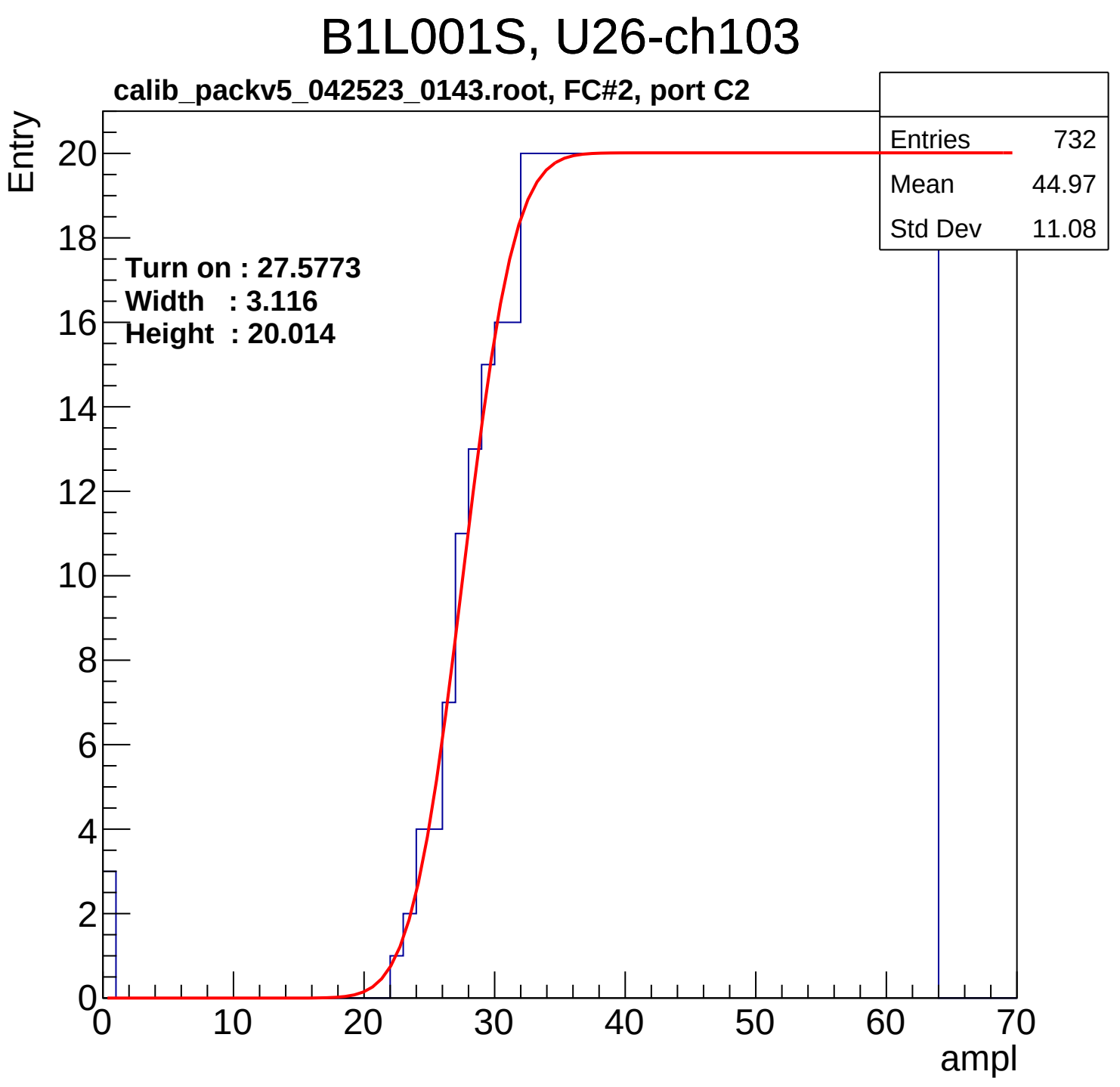

B1L001S, U26-ch98
calib_packv5_042523_0143.root, FC#2, port C2
Entries 769
Mean 44.11
Std Dev 11.45
Turn on : 25.8490
Width : 3.123
Height : 20.074
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

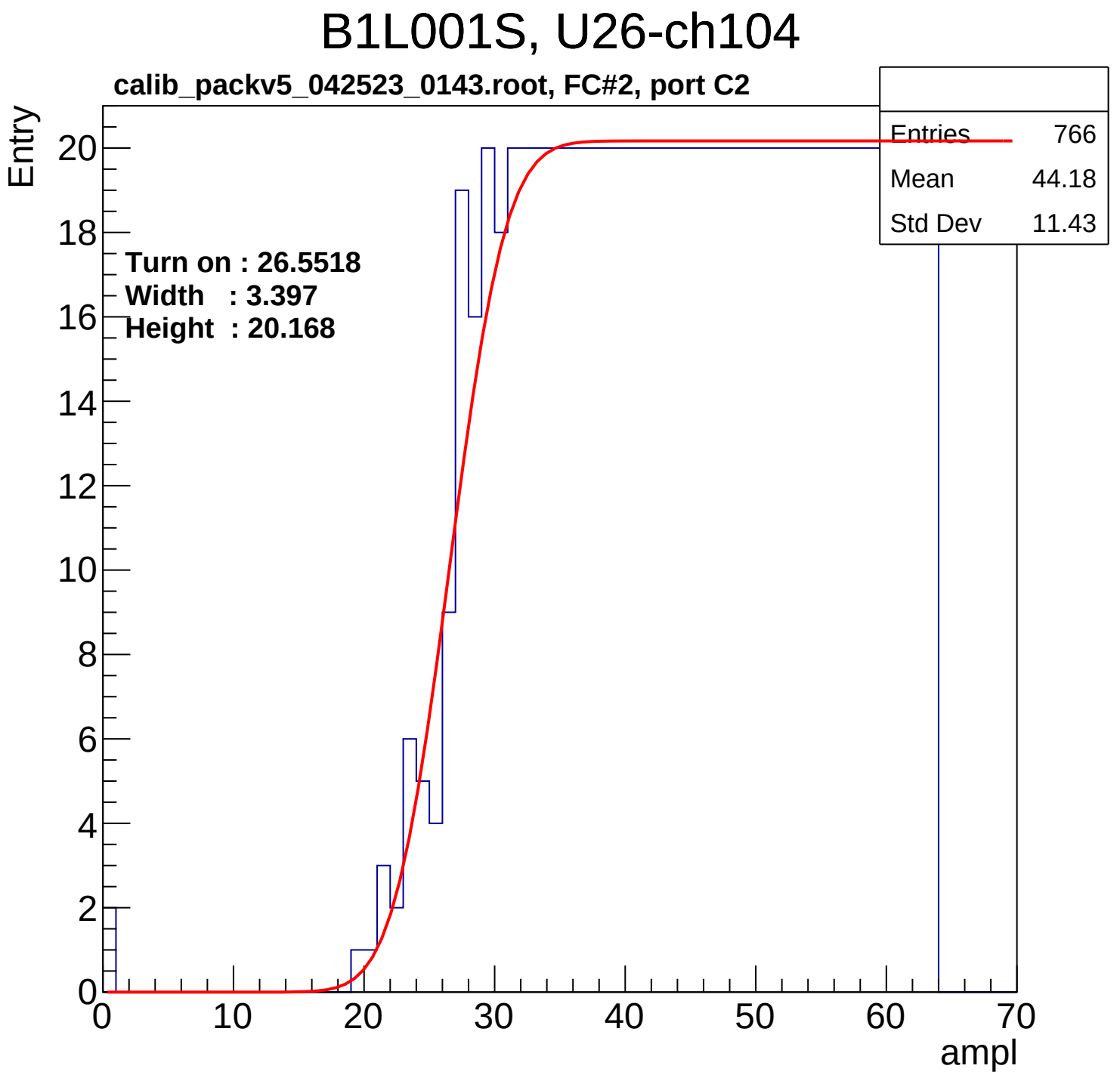

B1L001S, U26-ch99
calib_packv5_042523_0143.root, FC#2, port C2
Entries 722
Mean 45.24
Std Dev 10.86
Turn on : 27.9481
Width : 2.952
Height : 19.916
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

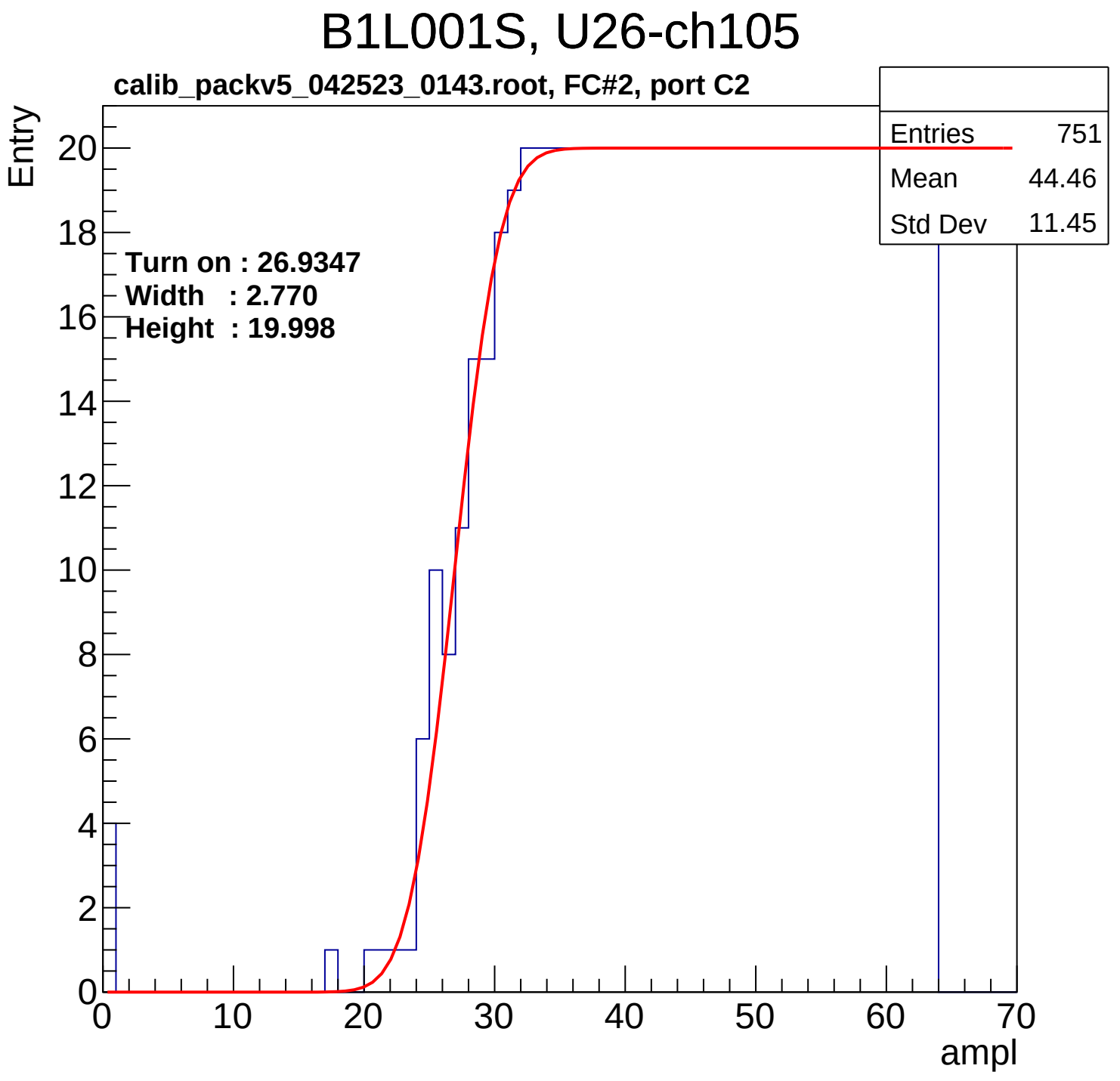

B1L001S, U26-ch100
calib_packv5_042523_0143.root, FC#2, port C2
Entries 736
Mean 44.91
Std Dev 11.03
Turn on : 27.3964
Width : 3.095
Height : 20.022
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

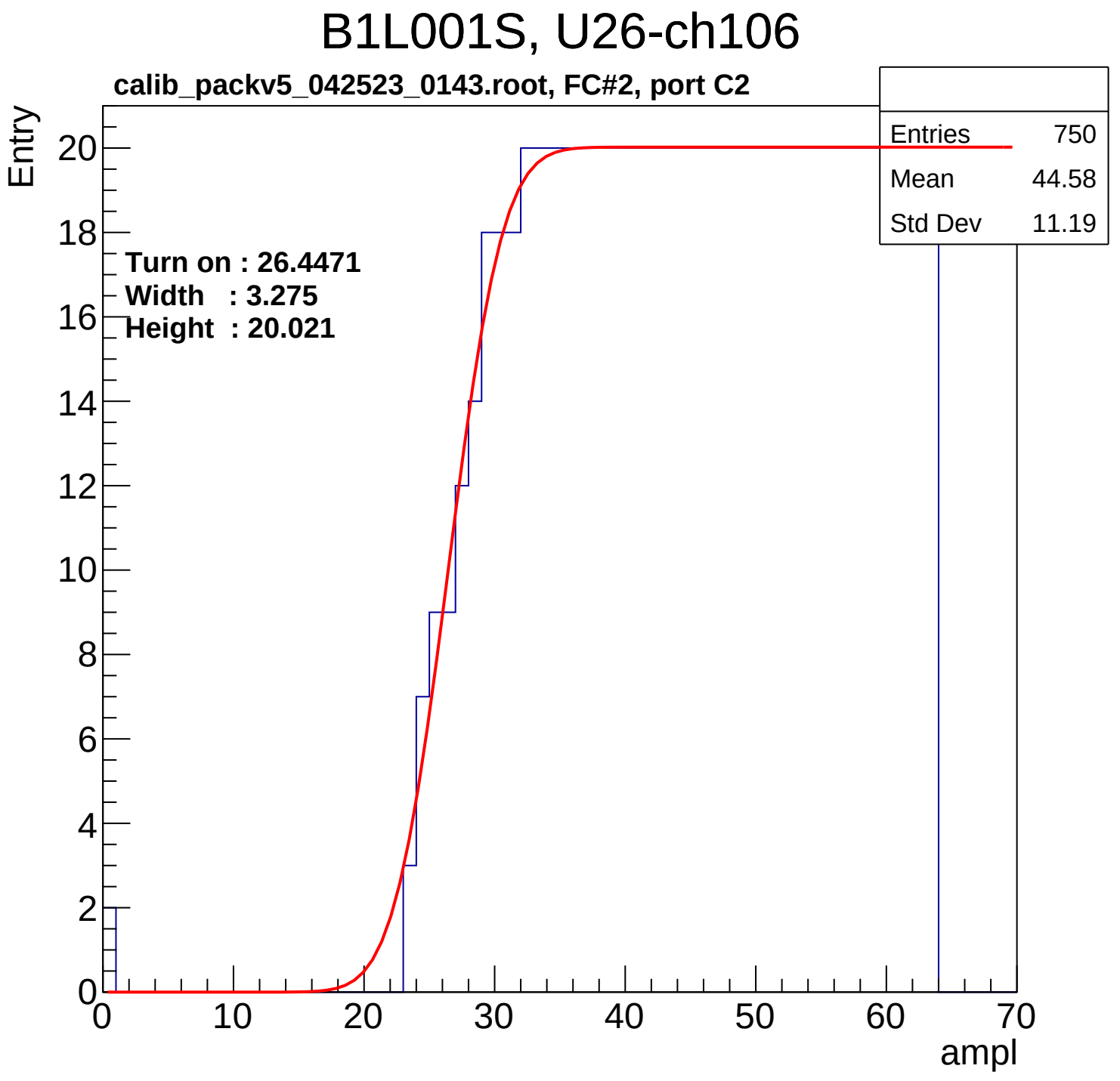

B1L001S, U26-ch101
calib_packv5_042523_0143.root, FC#2, port C2
Entries 722
Mean 45.28
Std Dev 10.81
Turn on : 28.1107
Width : 2.762
Height : 20.044
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

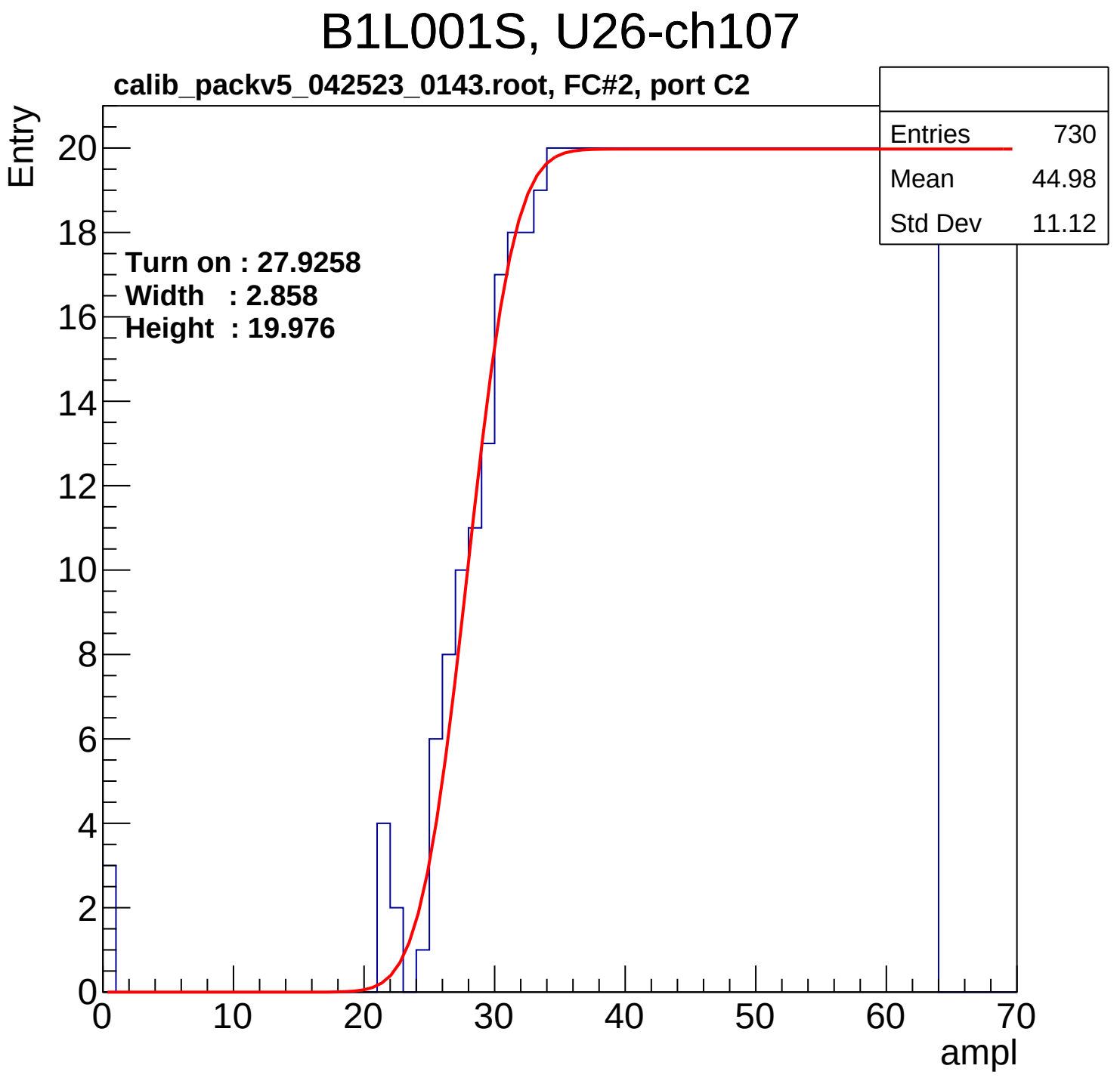

B1L001S, U26-ch102
calib_packv5_042523_0143.root, FC#2, port C2
Entries 749
Mean 44.6
Std Dev 11.23
Turn on : 26.8787
Width : 2.285
Height : 20.005
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

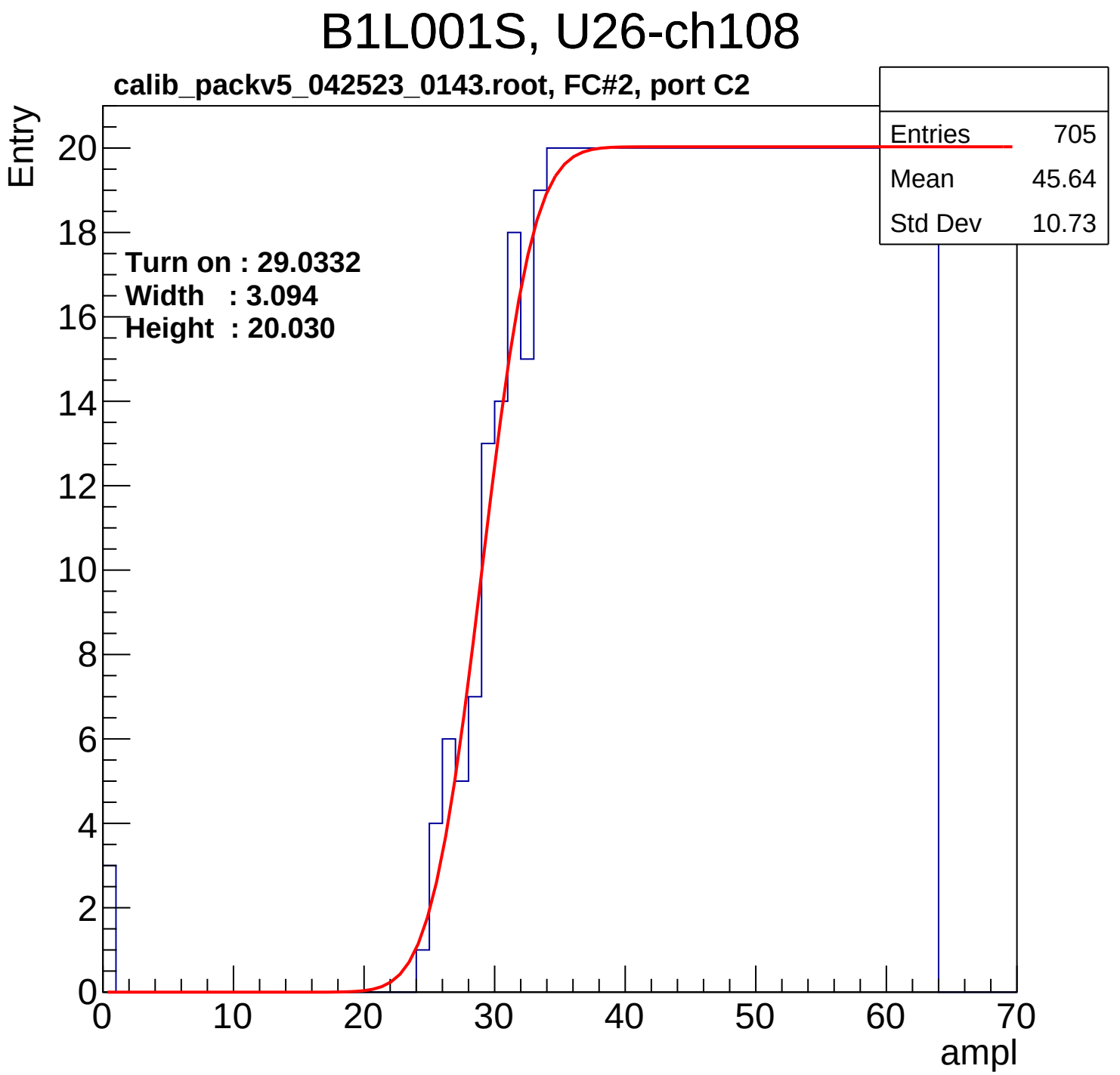

B1L001S, U26-ch103
calib_packv5_042523_0143.root, FC#2, port C2
Entries 732
Mean 44.97
Std Dev 11.08
Turn on : 27.5773
Width : 3.116
Height : 20.014
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

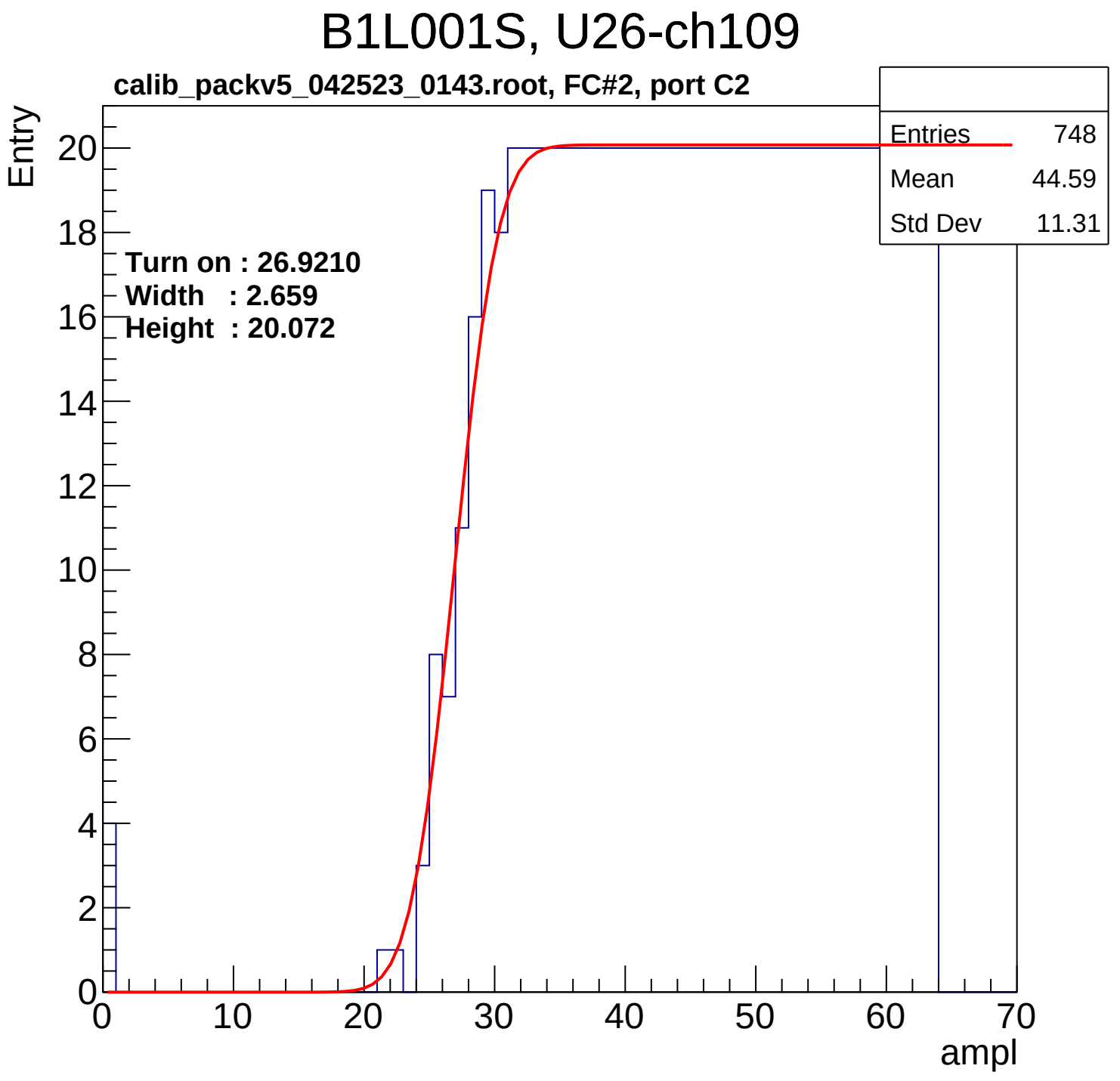

B1L001S, U26-ch104
calib_packv5_042523_0143.root, FC#2, port C2
Entries 766
Mean 44.18
Std Dev 11.43
Turn on : 26.5518
Width : 3.397
Height : 20.168
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

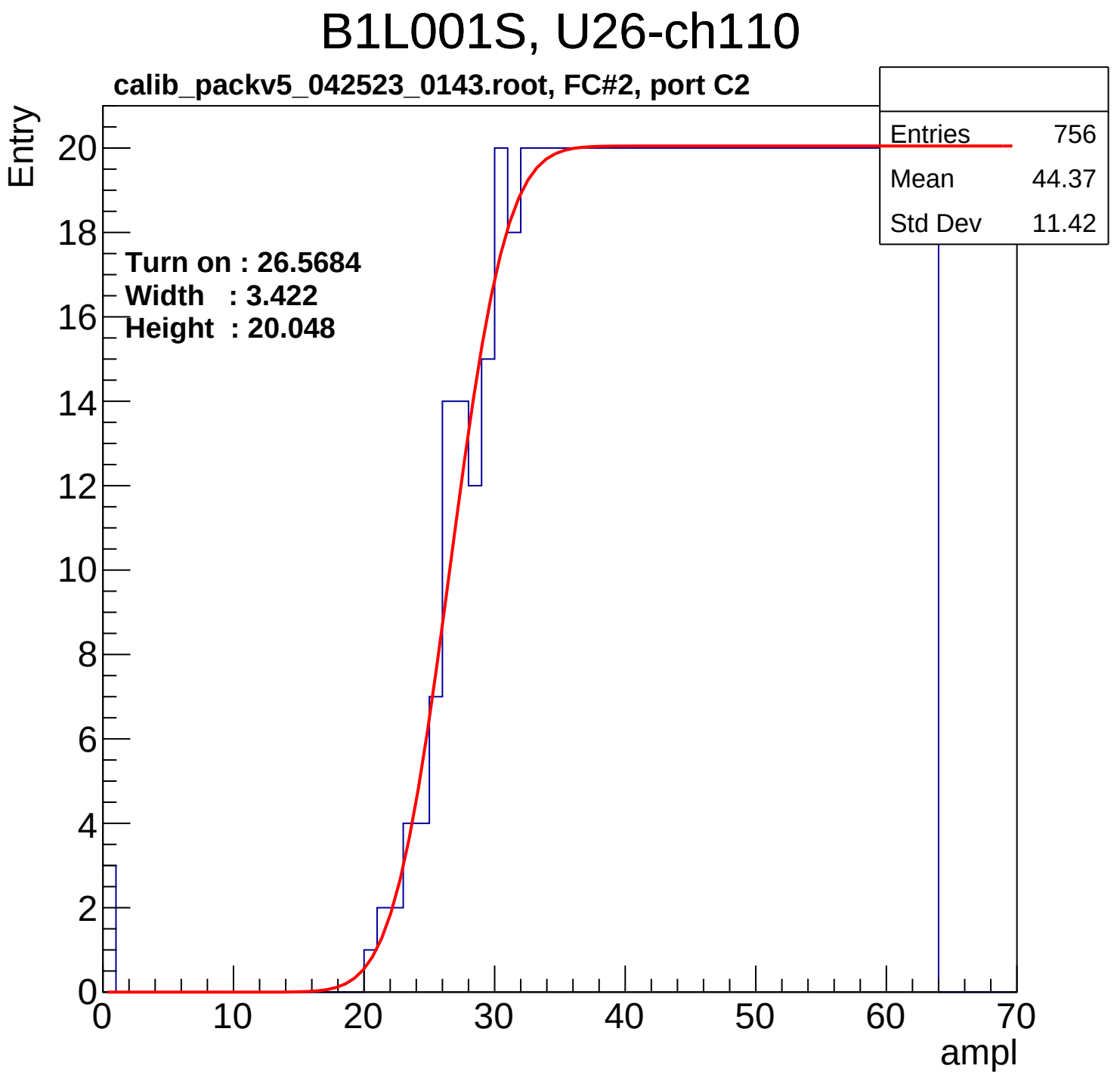

B1L001S, U26-ch105
calib_packv5_042523_0143.root, FC#2, port C2
Entries 751
Mean 44.46
Std Dev 11.45
Turn on : 26.9347
Width : 2.770
Height : 19.998
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

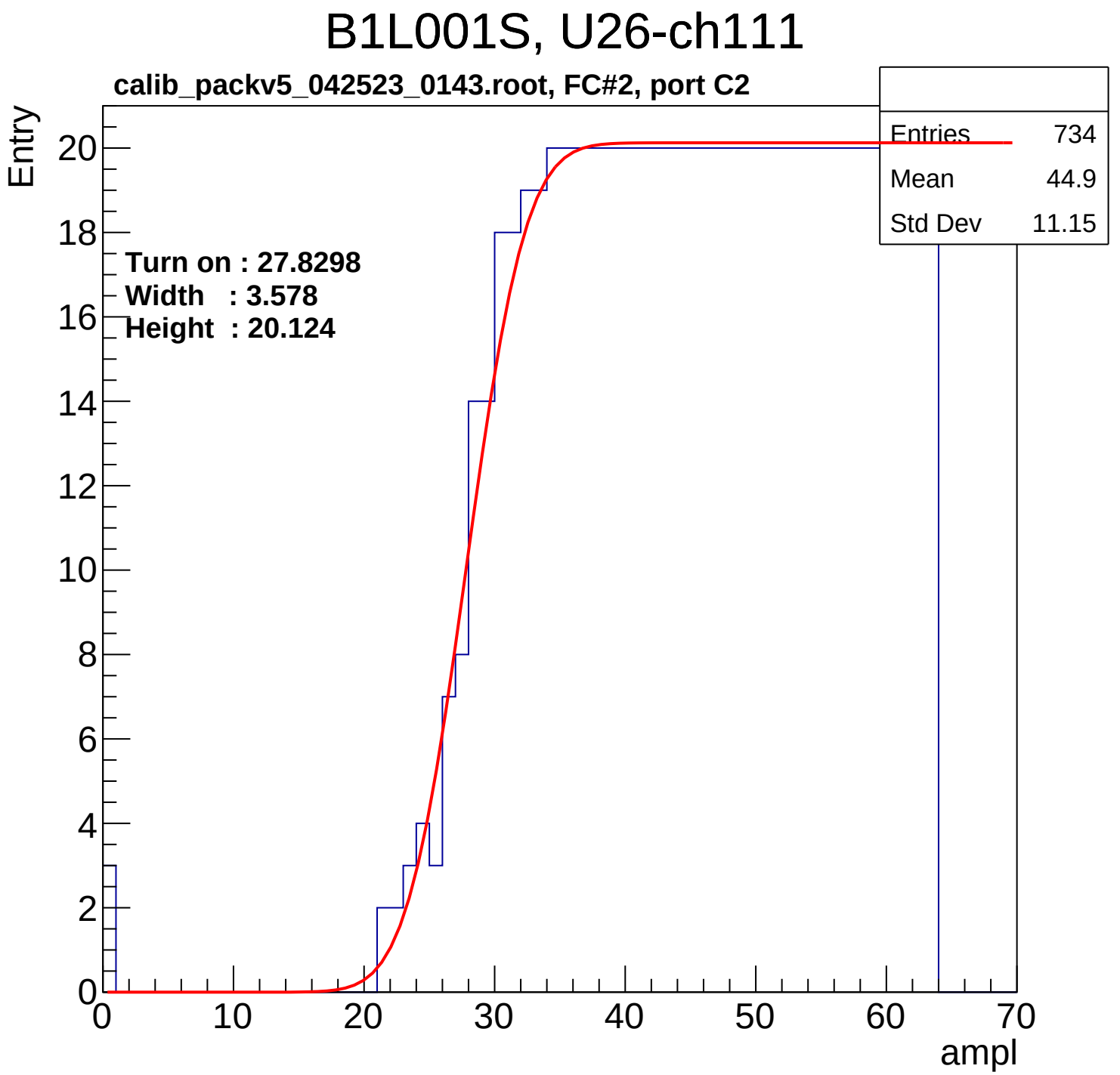

B1L001S, U26-ch106
calib_packv5_042523_0143.root, FC#2, port C2
Entries 750
Mean 44.58
Std Dev 11.19
Turn on : 26.4471
Width : 3.275
Height : 20.021
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

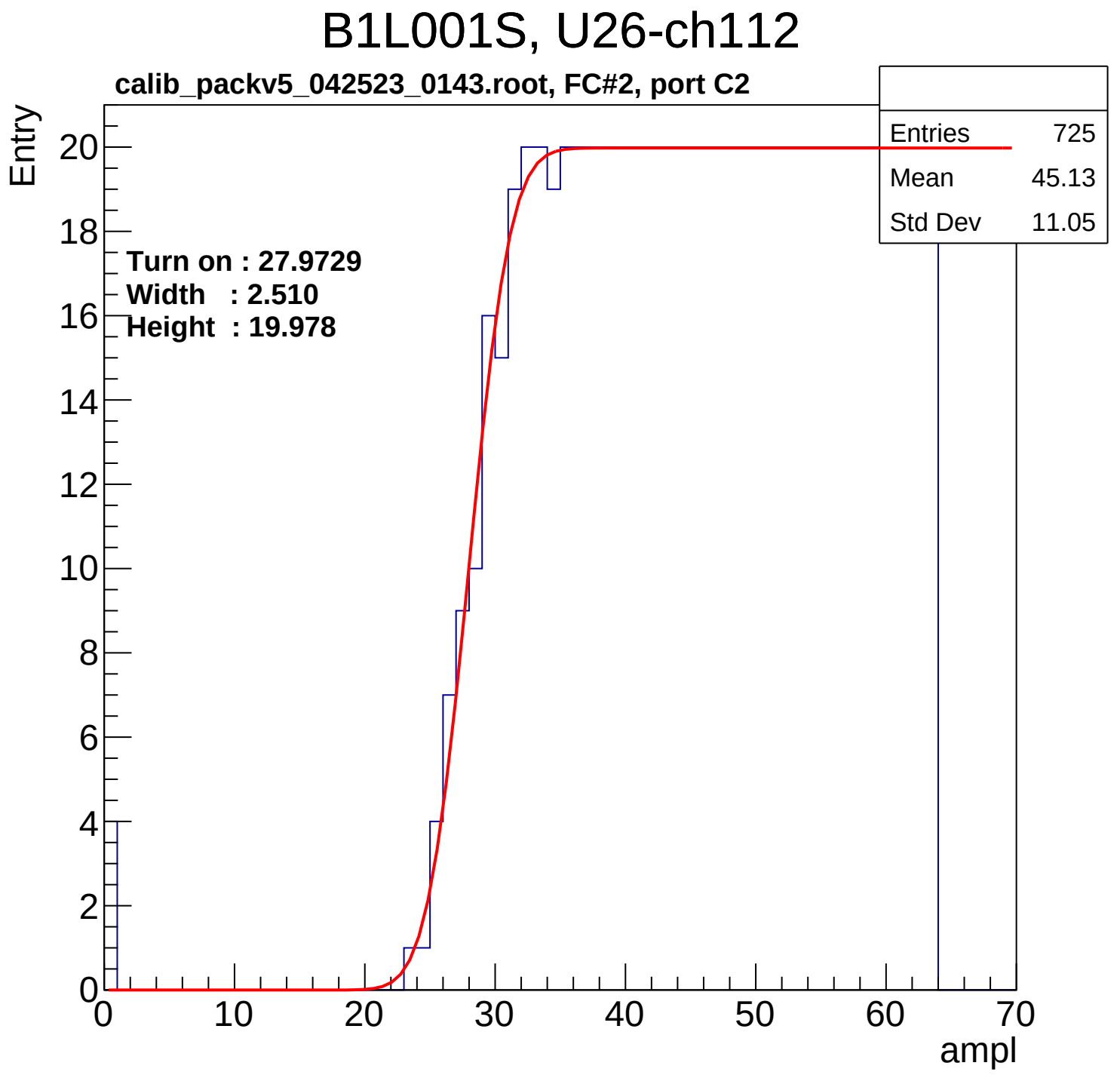

B1L001S, U26-ch107
calib_packv5_042523_0143.root, FC#2, port C2
Entries 730
Mean 44.98
Std Dev 11.12
Turn on : 27.9258
Width : 2.858
Height : 19.976
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

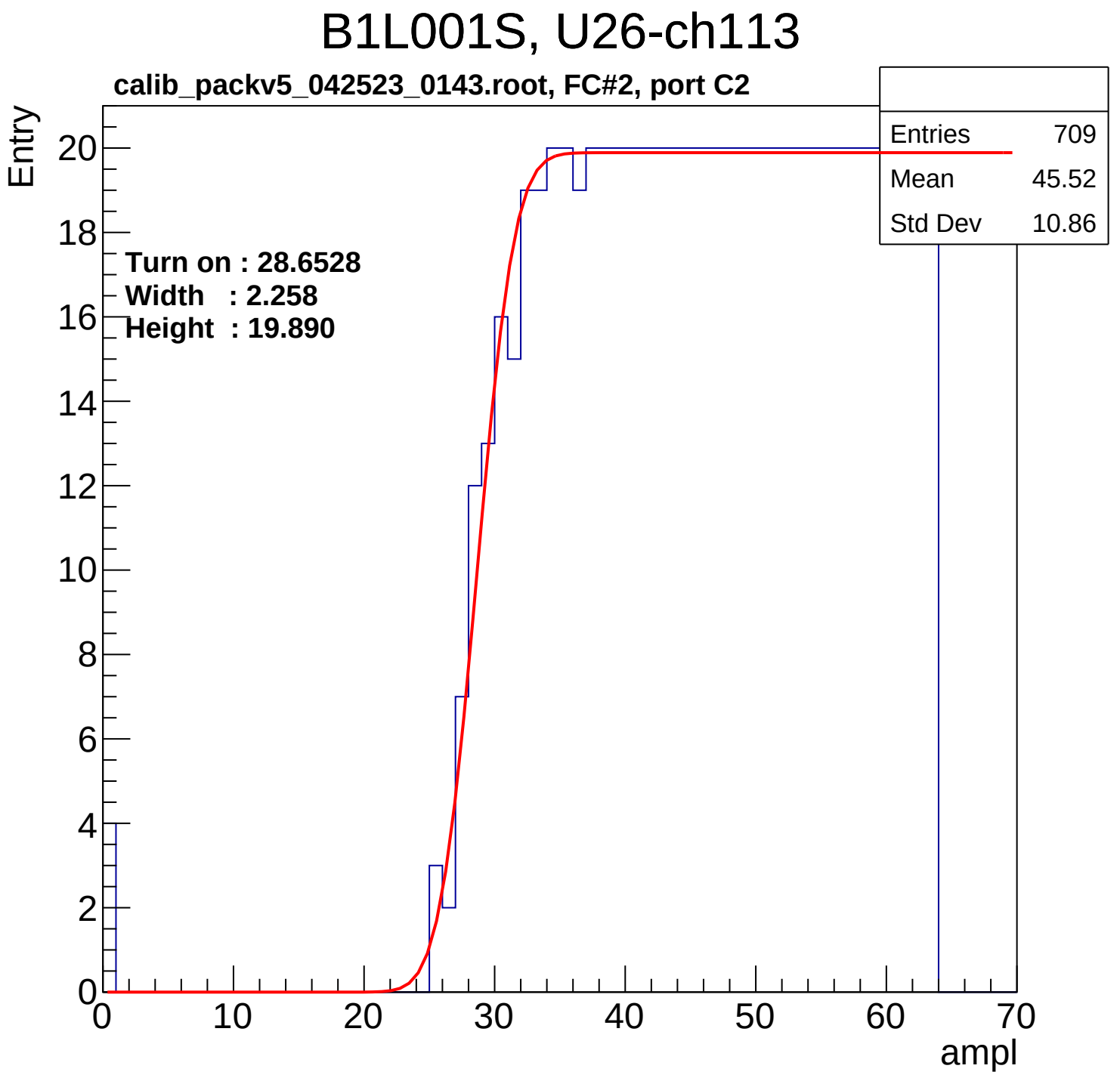

B1L001S, U26-ch108
calib_packv5_042523_0143.root, FC#2, port C2
Entries 705
Mean 45.64
Std Dev 10.73
Turn on : 29.0332
Width : 3.094
Height : 20.030
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

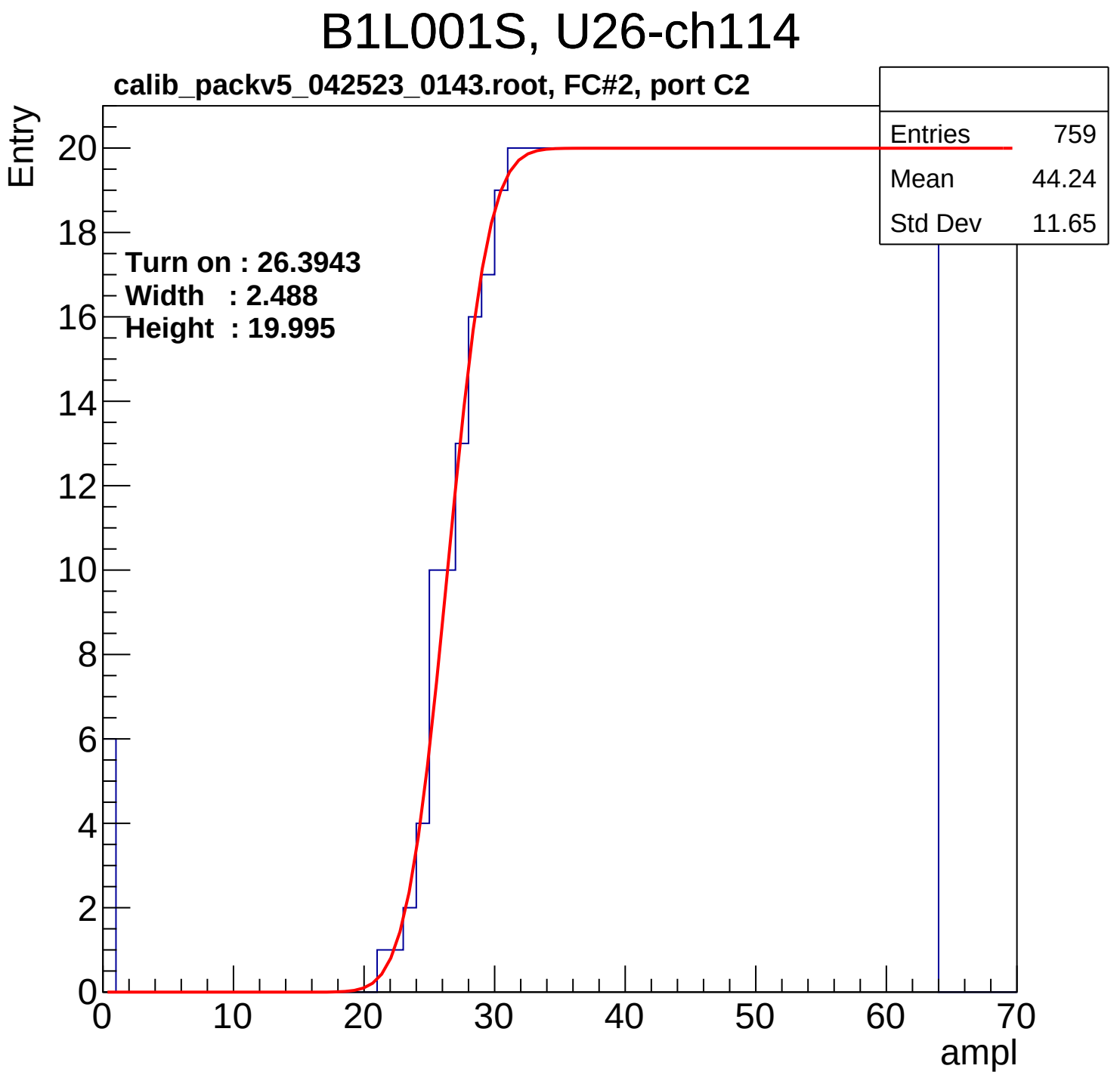

B1L001S, U26-ch109
calib_packv5_042523_0143.root, FC#2, port C2
Entries 748
Mean 44.59
Std Dev 11.31
Turn on : 26.9210
Width : 2.659
Height : 20.072
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

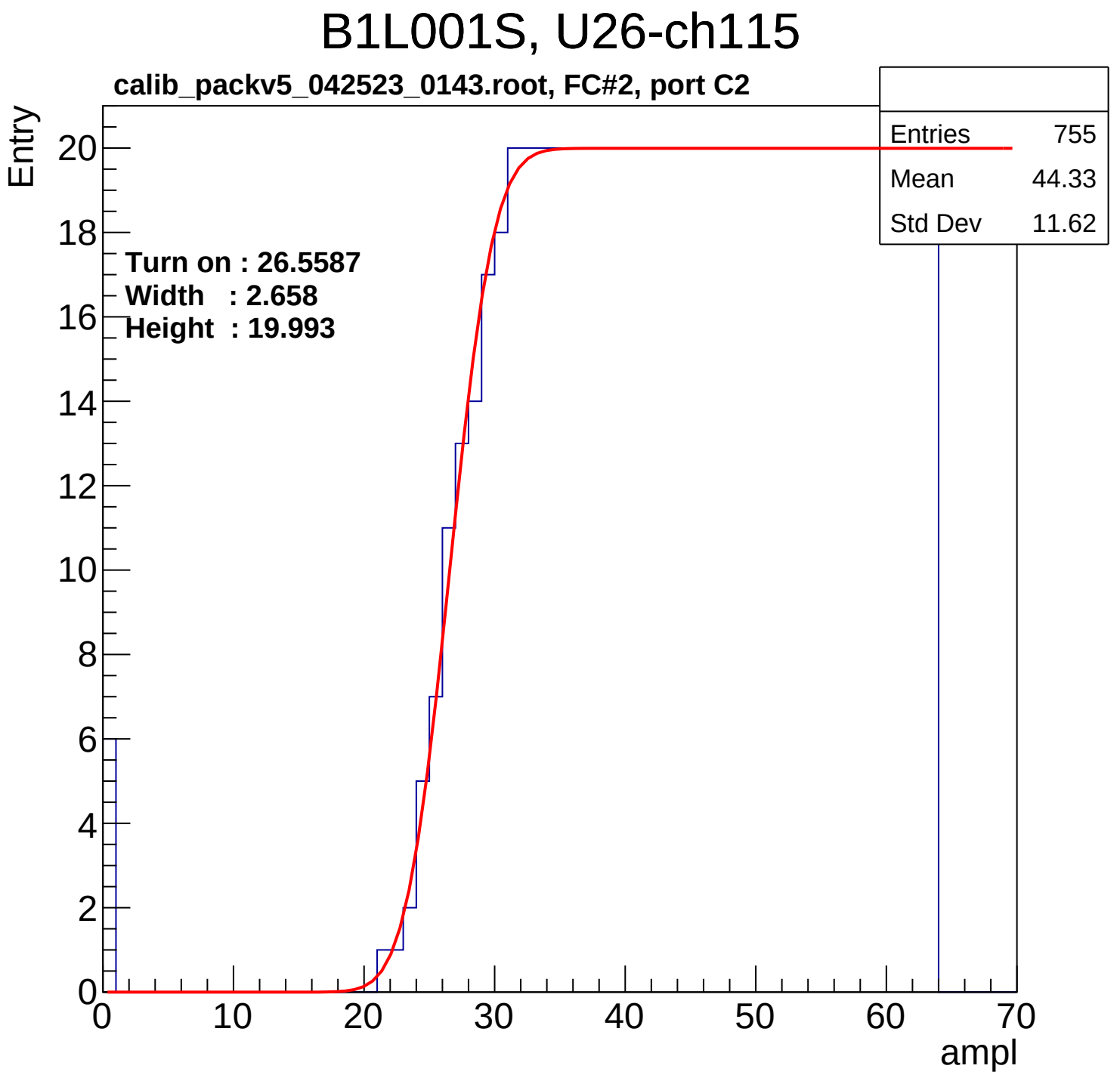

B1L001S, U26-ch110
calib_packv5_042523_0143.root, FC#2, port C2
Entries 756
Mean 44.37
Std Dev 11.42
Turn on : 26.5684
Width : 3.422
Height : 20.048
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

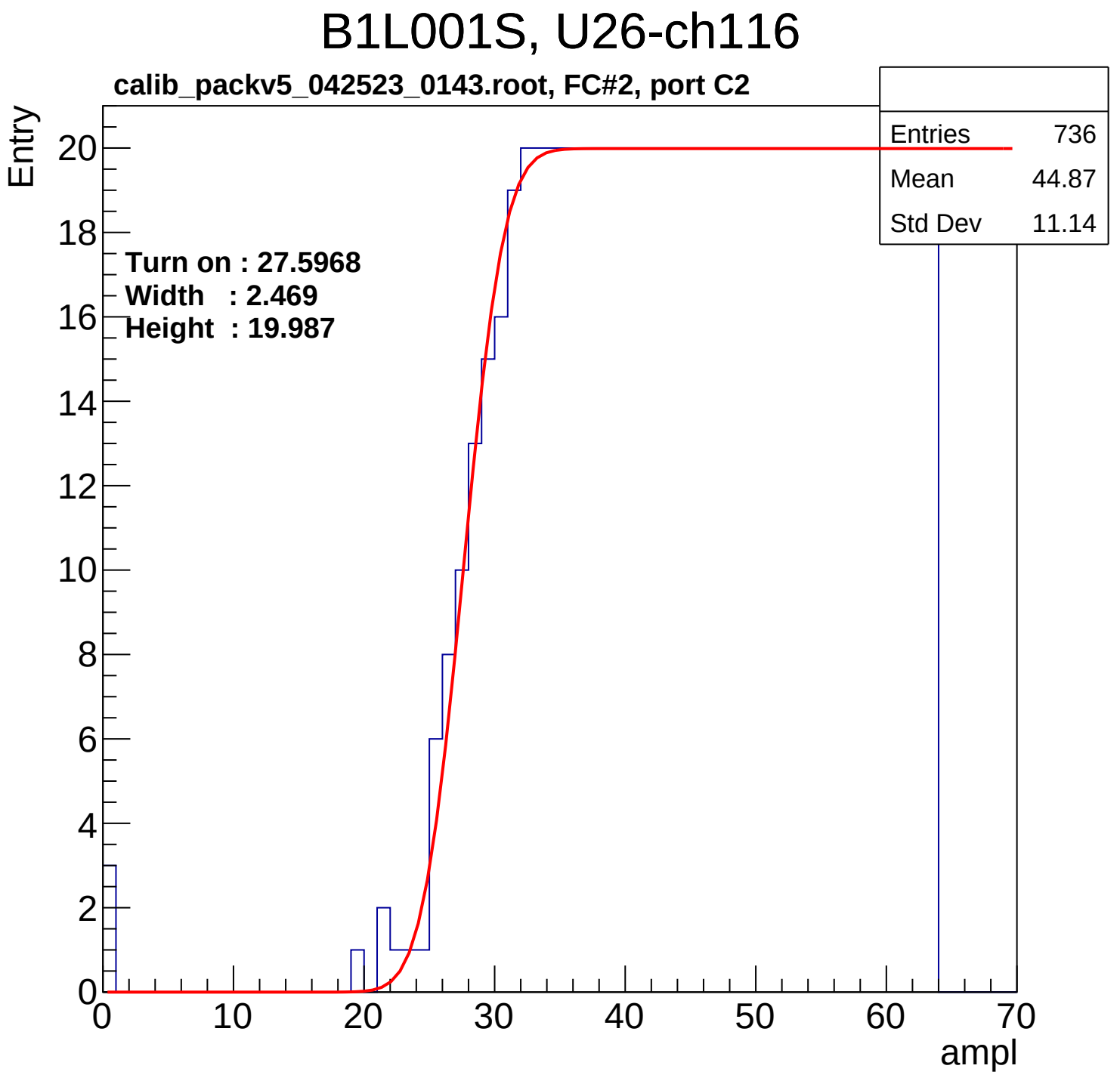

B1L001S, U26-ch111
calib_packv5_042523_0143.root, FC#2, port C2
Entries 734
Mean 44.9
Std Dev 11.15
Turn on : 27.8298
Width : 3.578
Height : 20.124
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

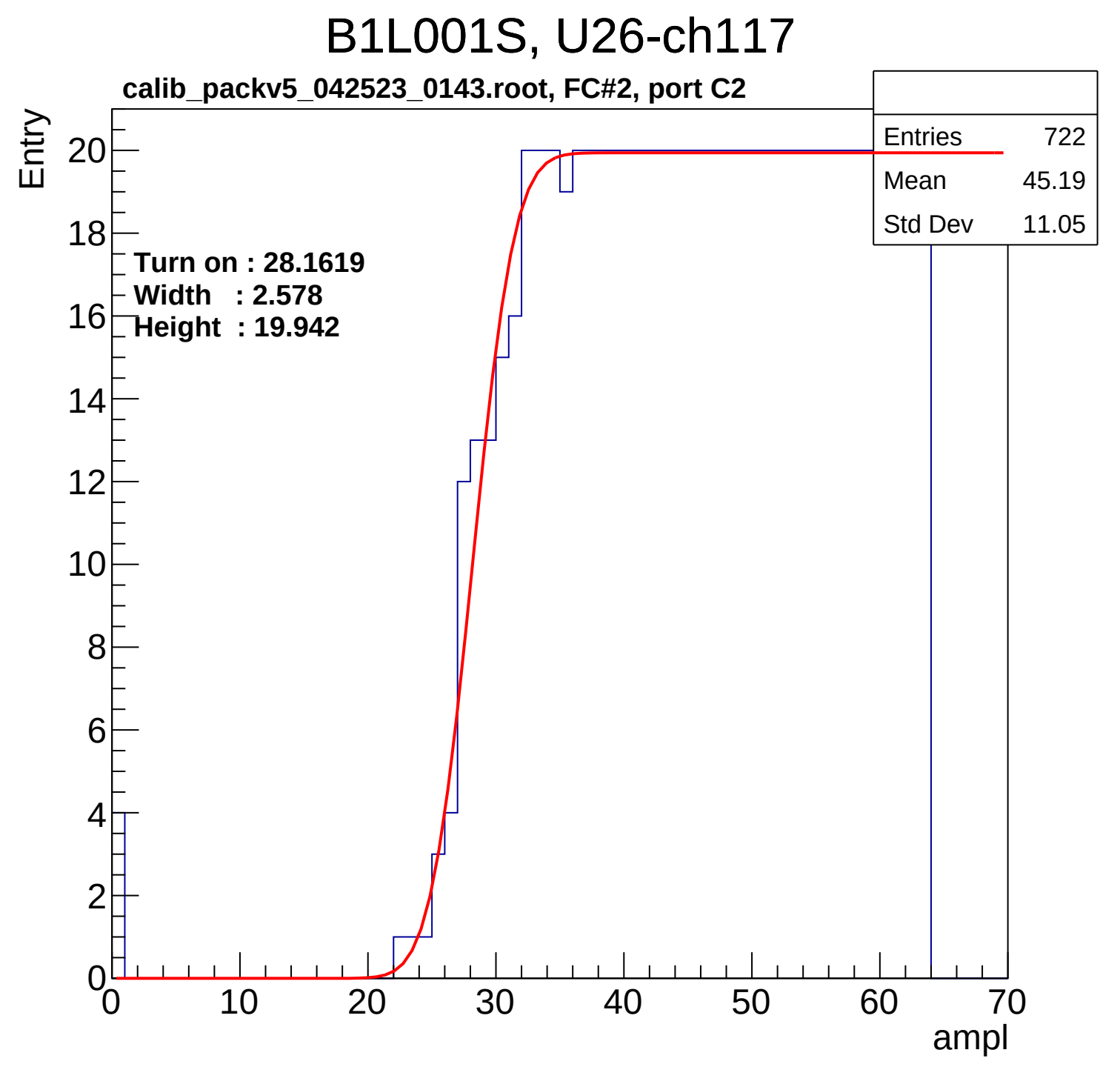

B1L001S, U26-ch112
calib_packv5_042523_0143.root, FC#2, port C2
Entries 725
Mean 45.13
Std Dev 11.05
Turn on : 27.9729
Width : 2.510
Height : 19.978
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

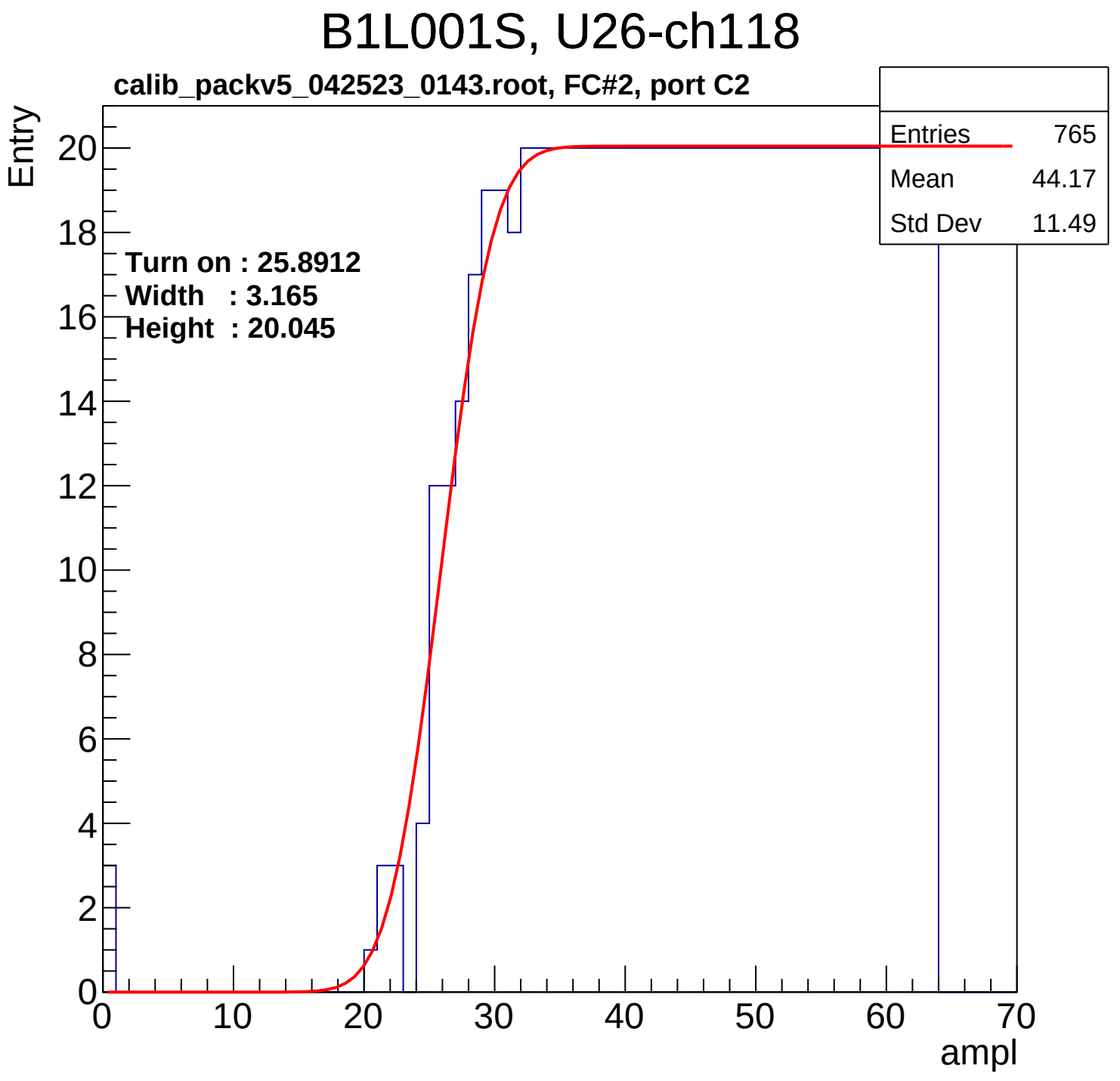

B1L001S, U26-ch113
calib_packv5_042523_0143.root, FC#2, port C2
Entries 709
Mean 45.52
Std Dev 10.86
Turn on : 28.6528
Width : 2.258
Height : 19.890
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

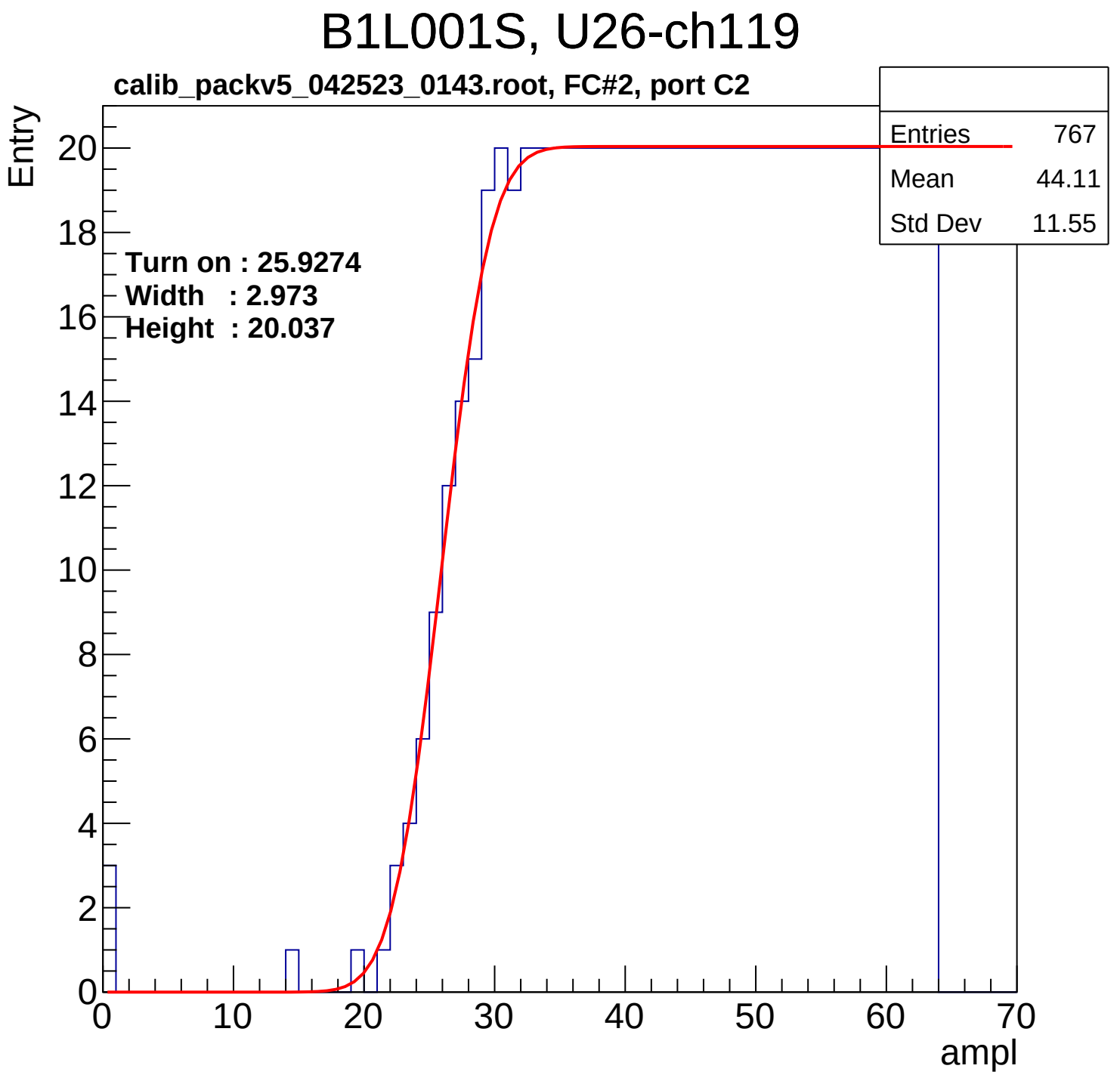

B1L001S, U26-ch114
calib_packv5_042523_0143.root, FC#2, port C2
Entries 759
Mean 44.24
Std Dev 11.65
Turn on : 26.3943
Width : 2.488
Height : 19.995
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

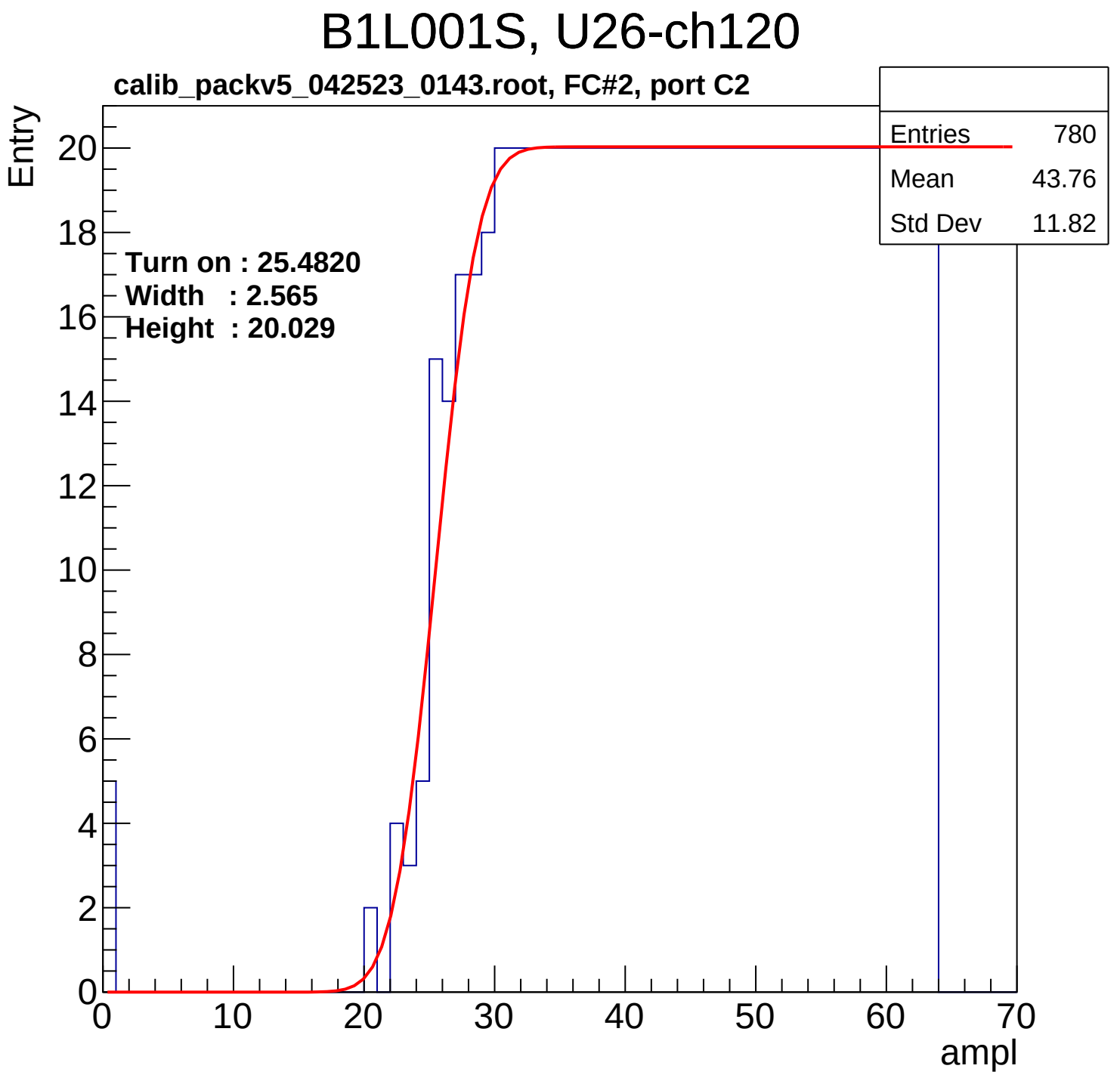

B1L001S, U26-ch115
calib_packv5_042523_0143.root, FC#2, port C2
Entries 755
Mean 44.33
Std Dev 11.62
Turn on : 26.5587
Width : 2.658
Height : 19.993
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

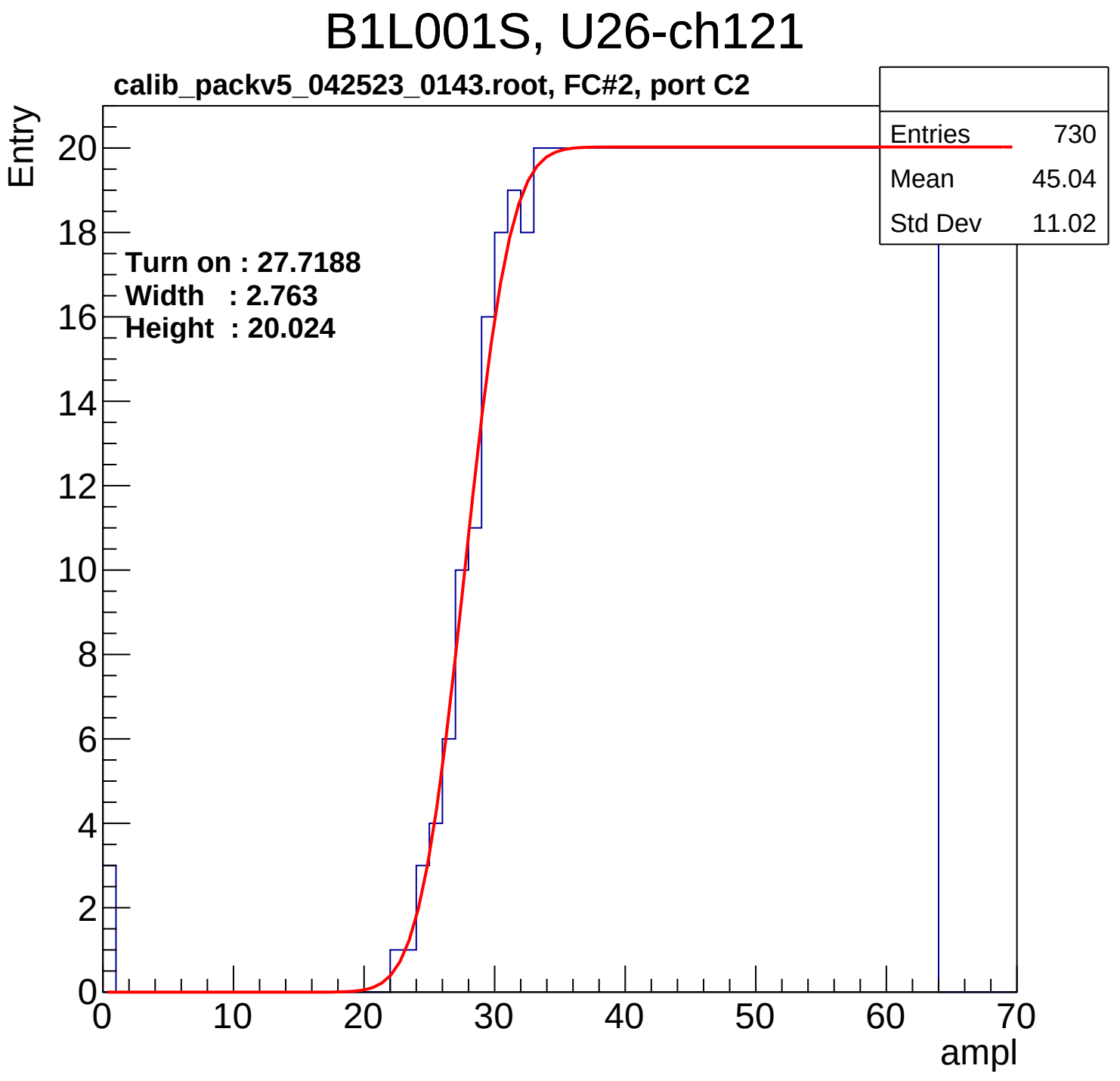

B1L001S, U26-ch116
calib_packv5_042523_0143.root, FC#2, port C2
Entries 736
Mean 44.87
Std Dev 11.14
Turn on : 27.5968
Width : 2.469
Height : 19.987
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

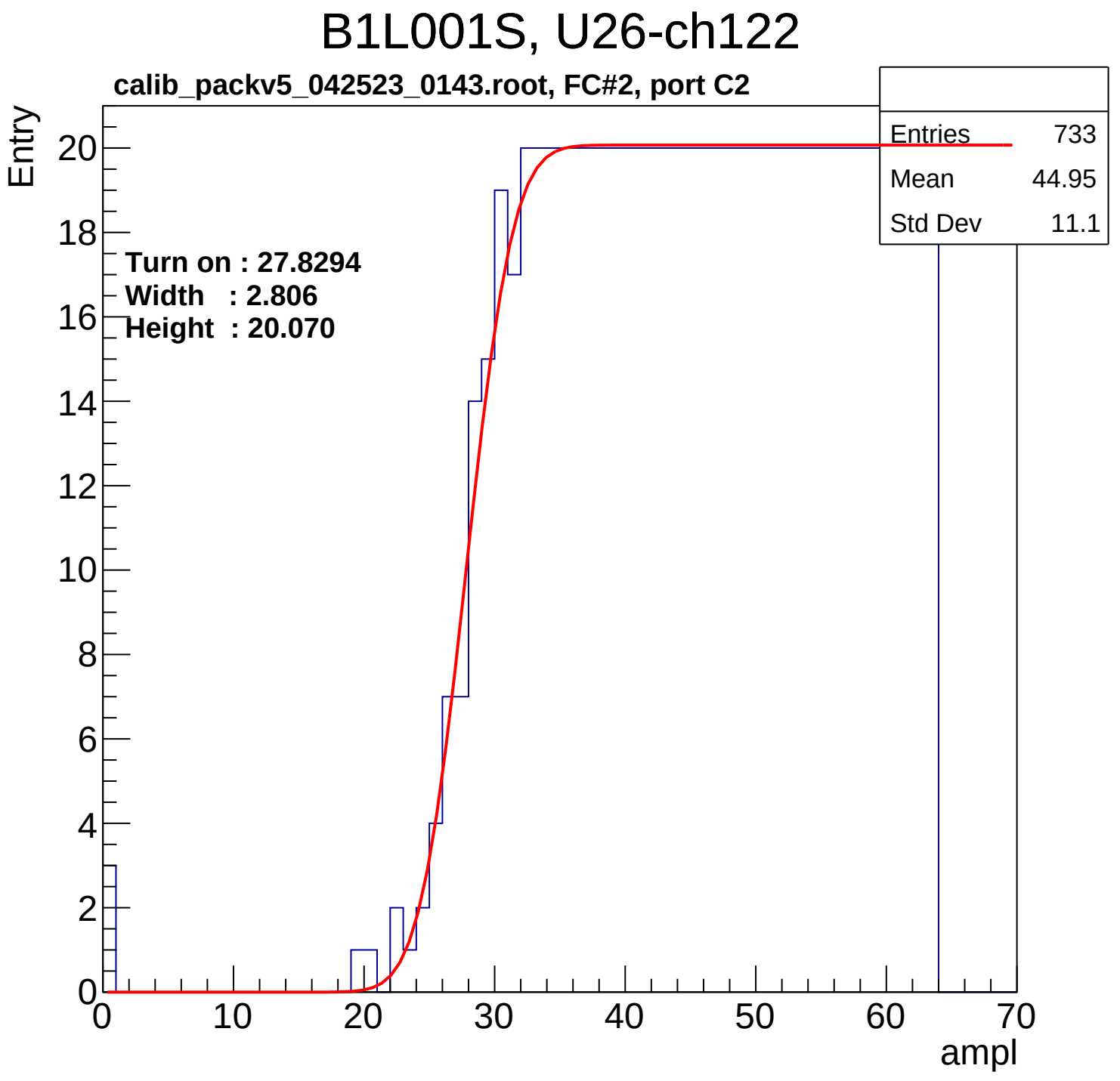

B1L001S, U26-ch117
calib_packv5_042523_0143.root, FC#2, port C2
Entries 722
Mean 45.19
Std Dev 11.05
Turn on : 28.1619
Width : 2.578
Height : 19.942
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

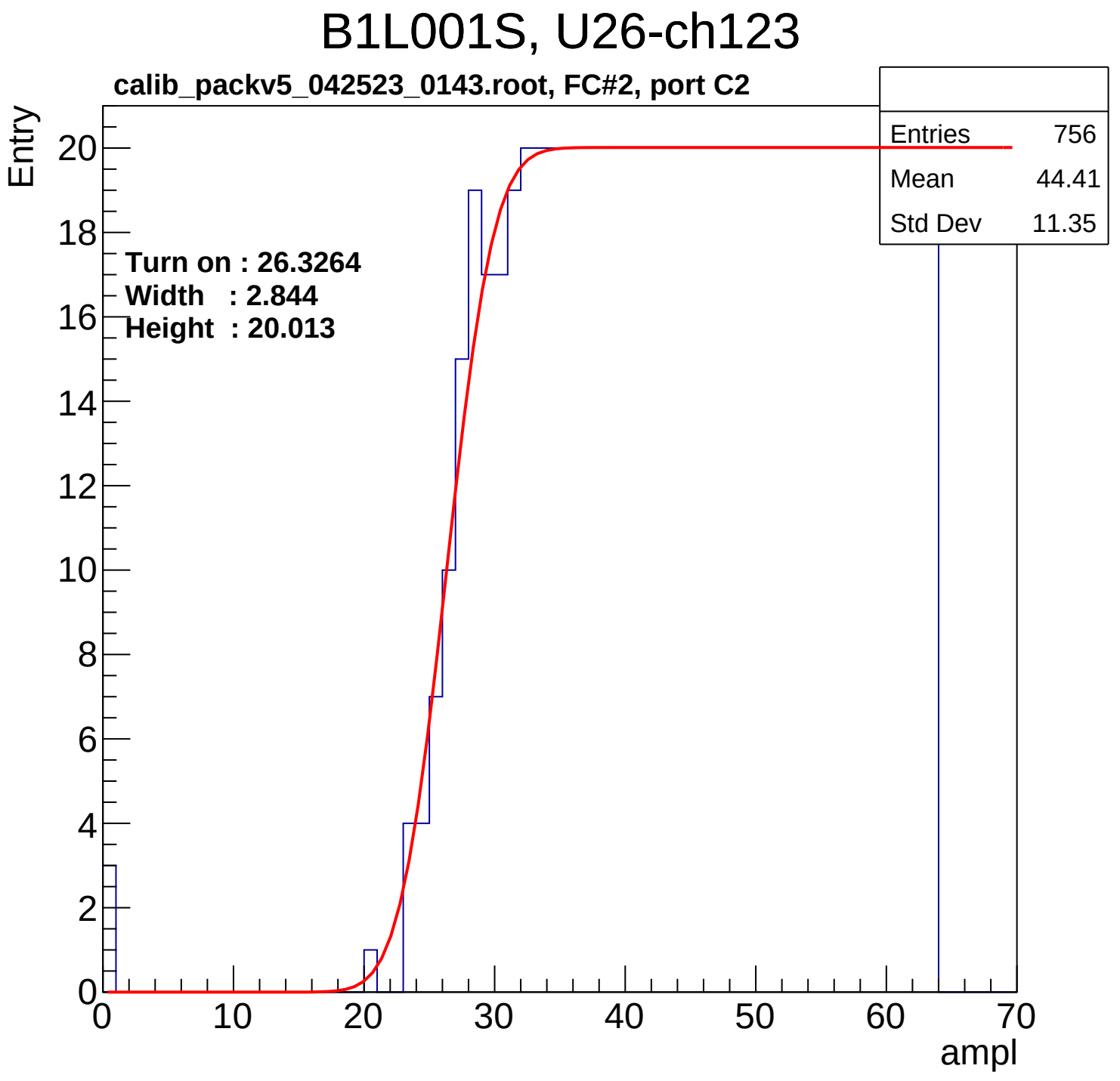

B1L001S, U26-ch118
calib_packv5_042523_0143.root, FC#2, port C2
Entries 765
Mean 44.17
Std Dev 11.49
Turn on : 25.8912
Width : 3.165
Height : 20.045
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

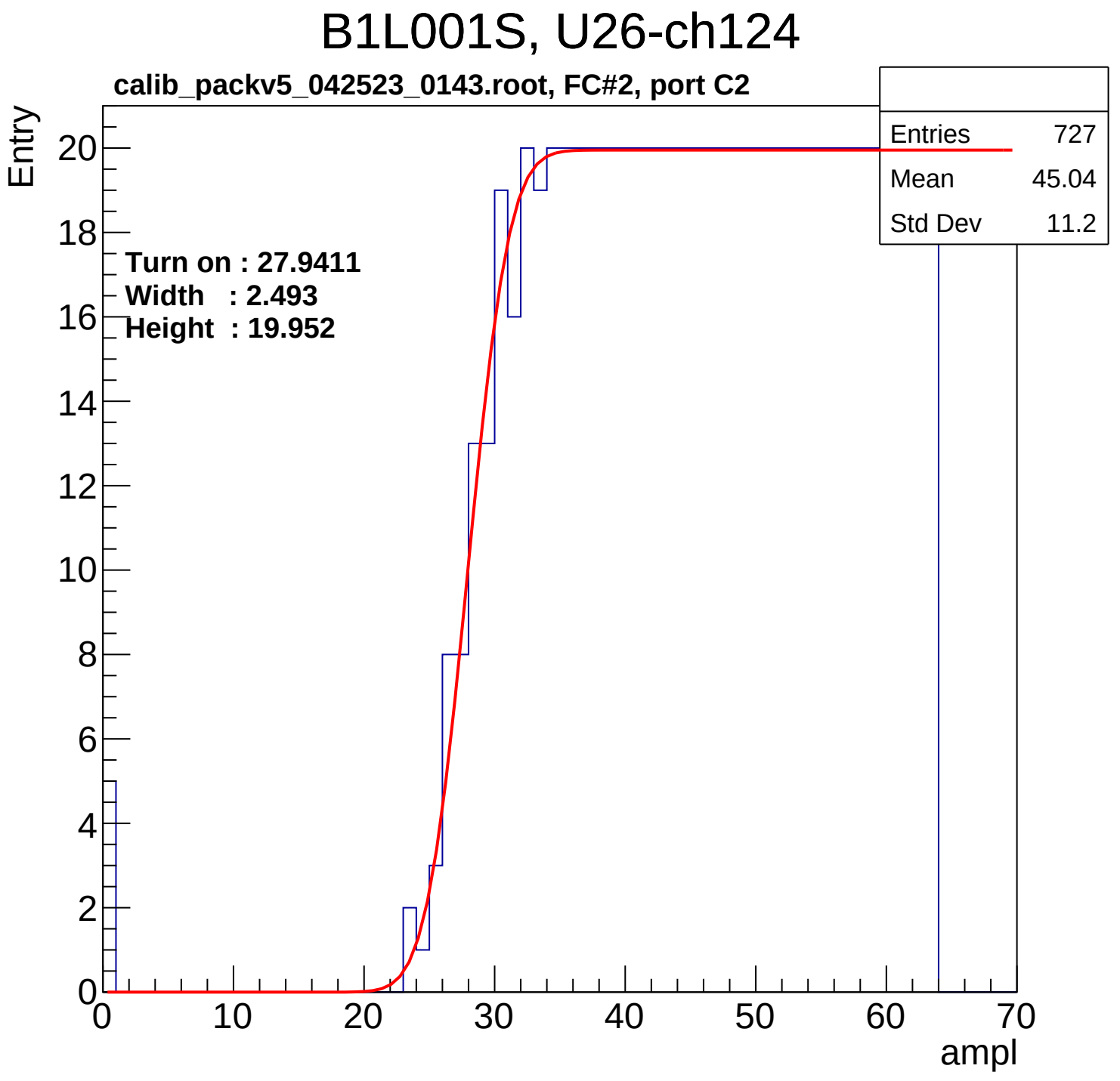

B1L001S, U26-ch119
calib_packv5_042523_0143.root, FC#2, port C2
Entries 767
Mean 44.11
Std Dev 11.55
Turn on : 25.9274
Width : 2.973
Height : 20.037
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

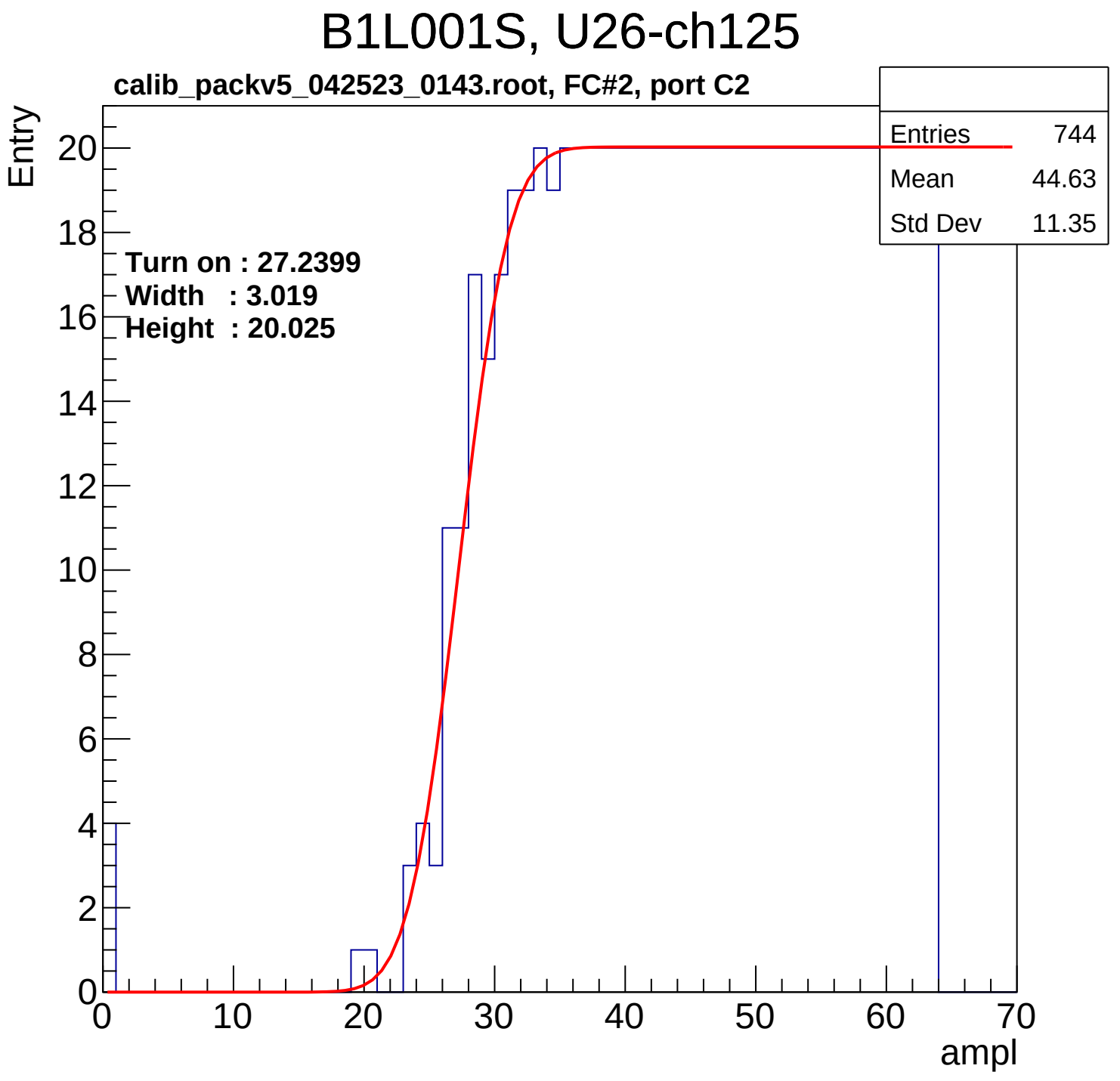

B1L001S, U26-ch120
calib_packv5_042523_0143.root, FC#2, port C2
Entries 780
Mean 43.76
Std Dev 11.82
Turn on : 25.4820
Width : 2.565
Height : 20.029
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

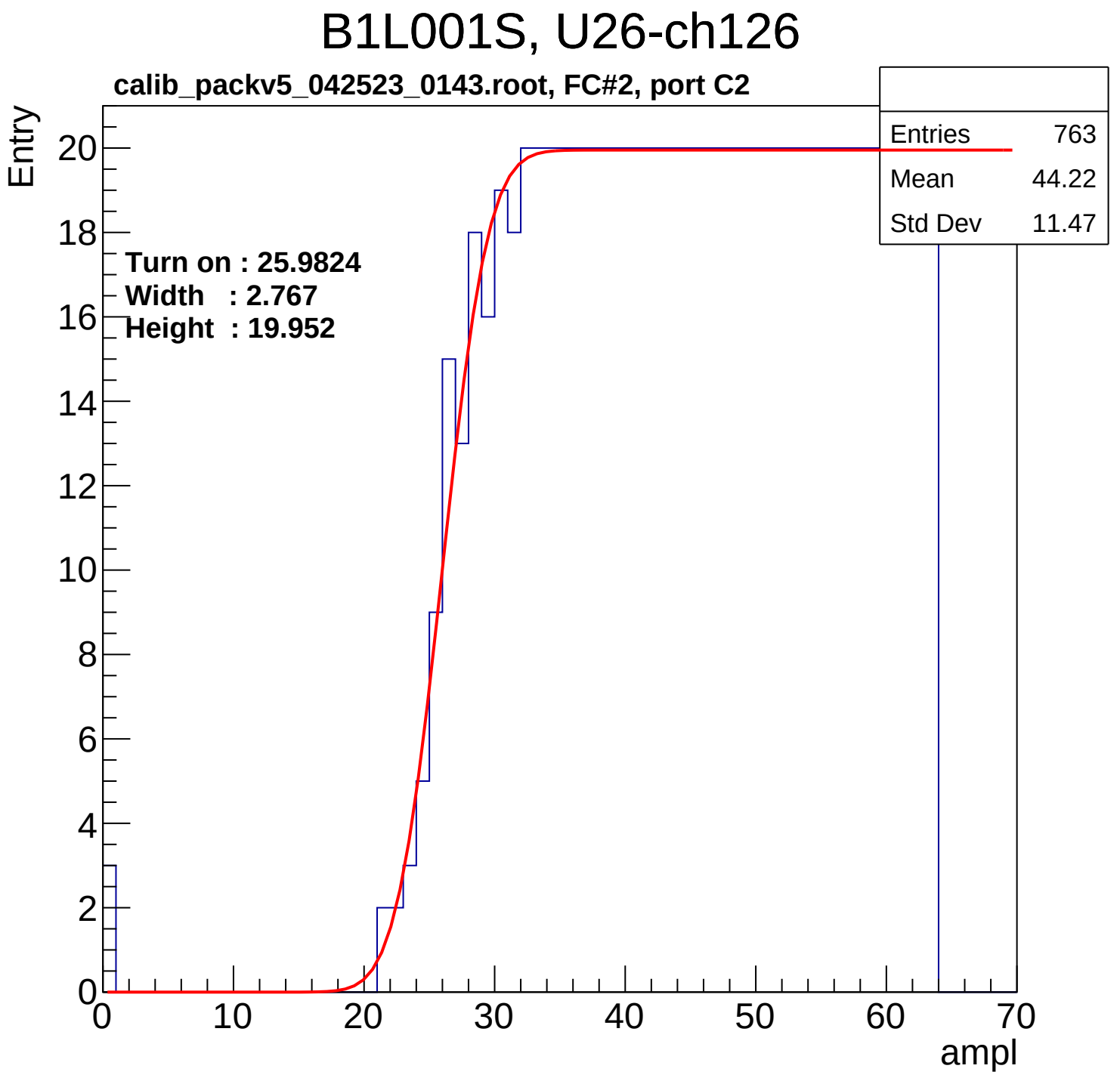

B1L001S, U26-ch121
calib_packv5_042523_0143.root, FC#2, port C2
Entries 730
Mean 45.04
Std Dev 11.02
Turn on : 27.7188
Width : 2.763
Height : 20.024
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

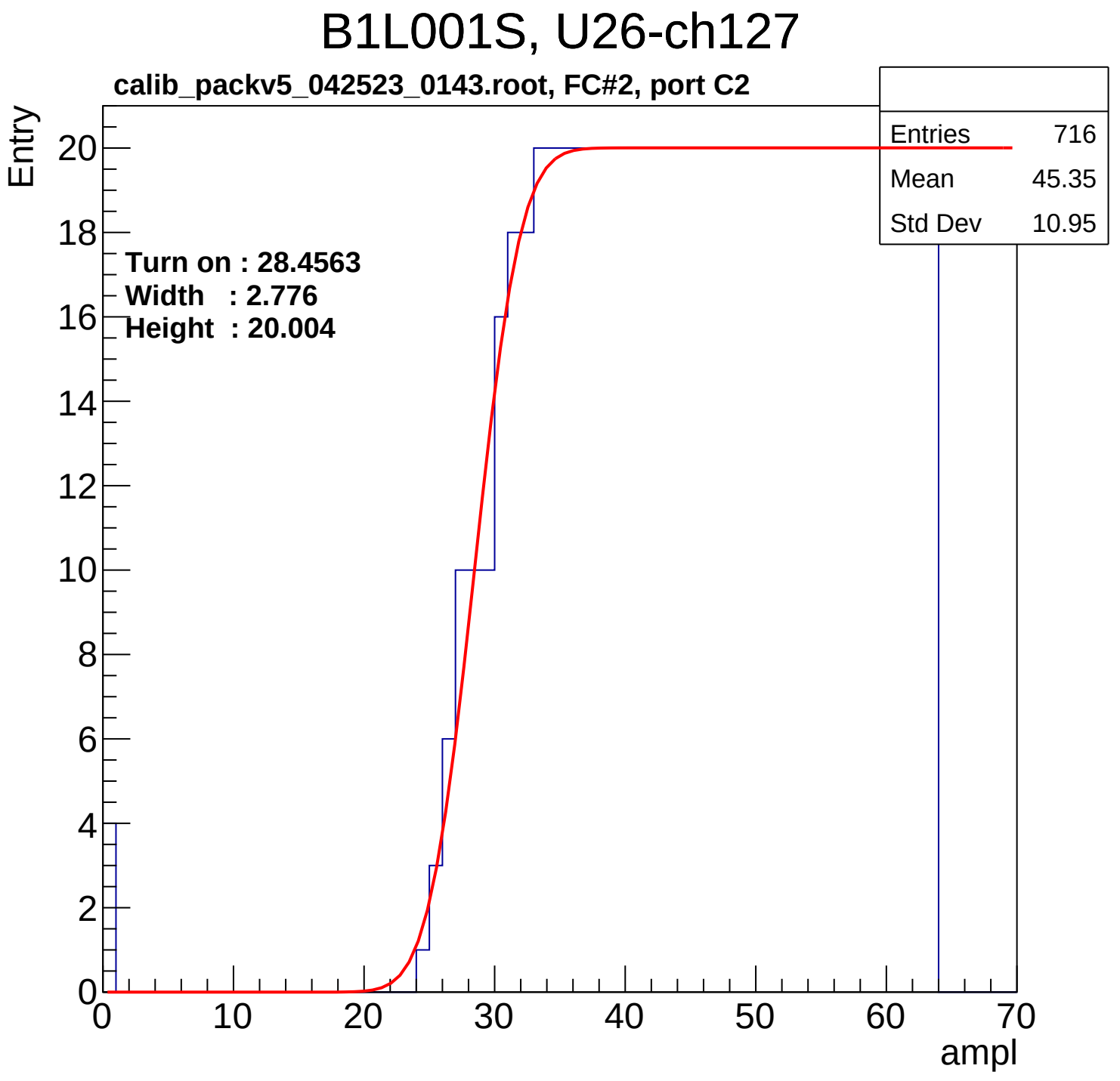

B1L001S, U26-ch122
calib_packv5_042523_0143.root, FC#2, port C2
Entries 733
Mean 44.95
Std Dev 11.1
Turn on : 27.8294
Width : 2.806
Height : 20.070
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

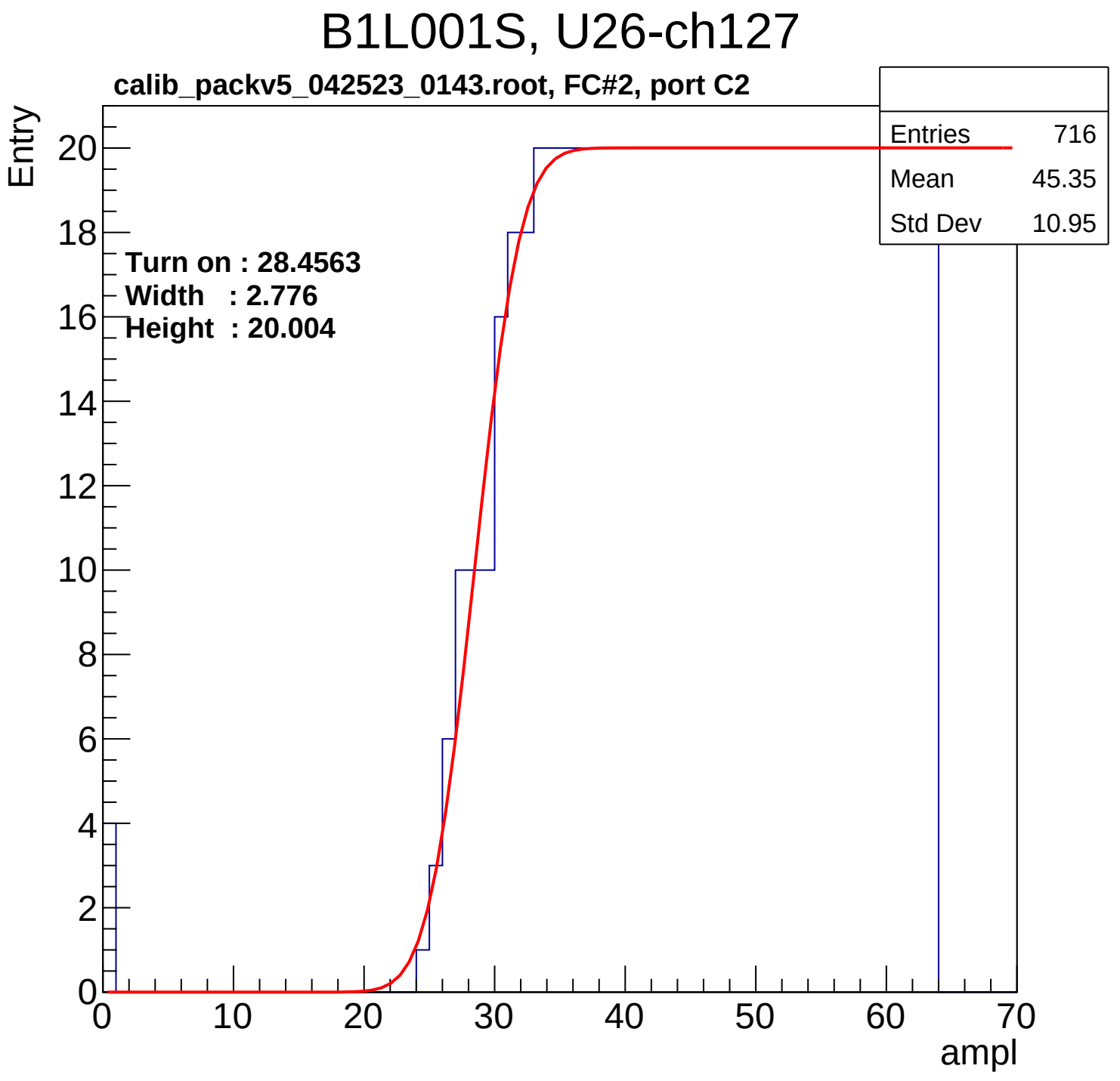

B1L001S, U26-ch123
calib_packv5_042523_0143.root, FC#2, port C2
Entries 756
Mean 44.41
Std Dev 11.35
Turn on : 26.3264
Width : 2.844
Height : 20.013
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70


B1L001S, U26-ch124
calib_packv5_042523_0143.root, FC#2, port C2
Entries 727
Mean 45.04
Std Dev 11.2
Turn on : 27.9411
Width : 2.493
Height : 19.952
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70


B1L001S, U26-ch125
calib_packv5_042523_0143.root, FC#2, port C2
Entries 744
Mean 44.63
Std Dev 11.35
Turn on : 27.2399
Width : 3.019
Height : 20.025
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70


B1L001S, U26-ch126
calib_packv5_042523_0143.root, FC#2, port C2
Entries 763
Mean 44.22
Std Dev 11.47
Turn on : 25.9824
Width : 2.767
Height : 19.952
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70


B1L001S, U26-ch127
calib_packv5_042523_0143.root, FC#2, port C2
Entries 716
Mean 45.35
Std Dev 10.95
Turn on : 28.4563
Width : 2.776
Height : 20.004
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70


B1L001S, U26-ch127
calib_packv5_042523_0143.root, FC#2, port C2
Entries 716
Mean 45.35
Std Dev 10.95
Turn on : 28.4563
Width : 2.776
Height : 20.004
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70