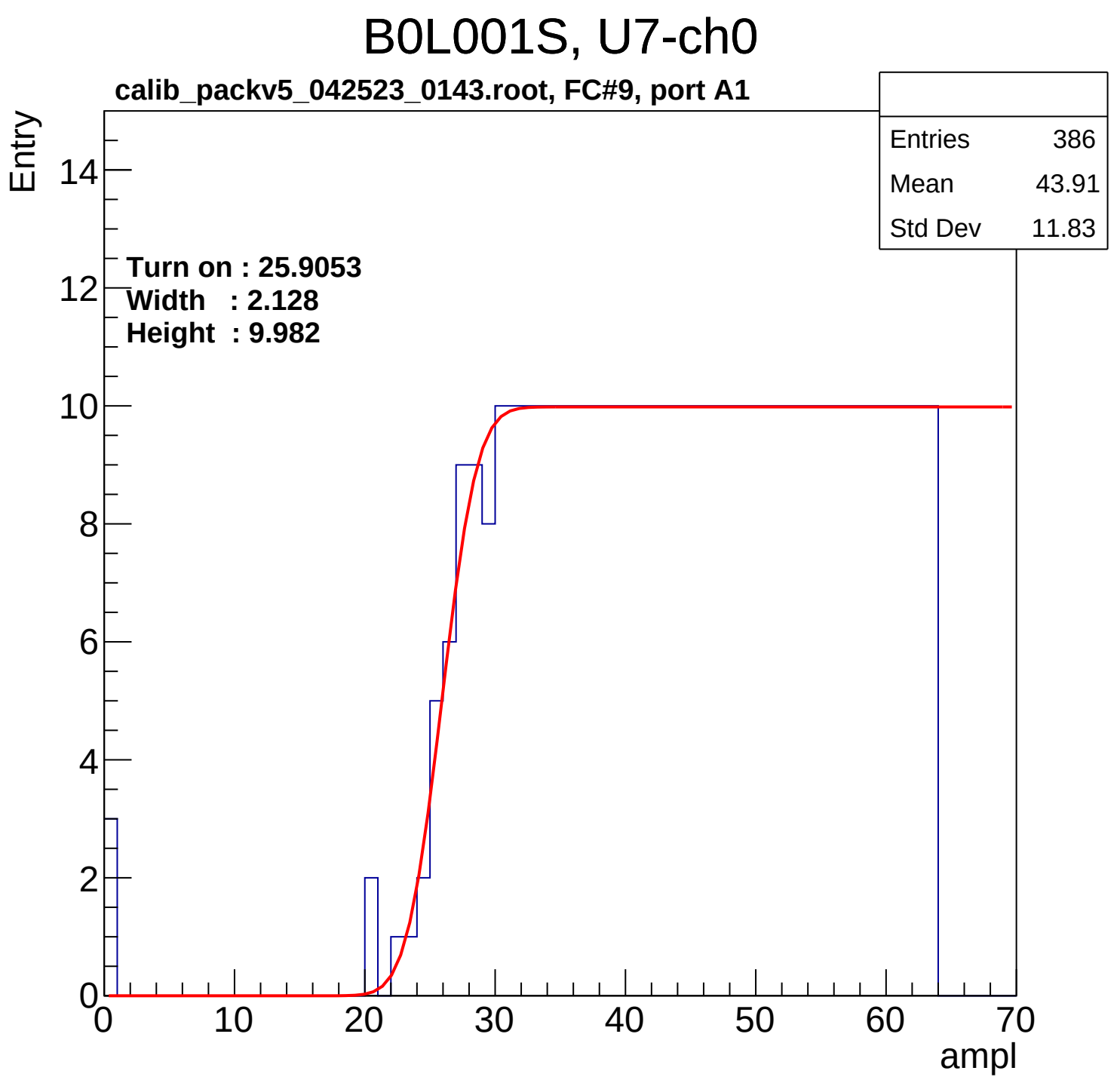
B0L001S, U7-ch0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 386
Mean 43.91
Std Dev 11.83
Turn on : 25.9053
Width : 2.128
Height : 9.982
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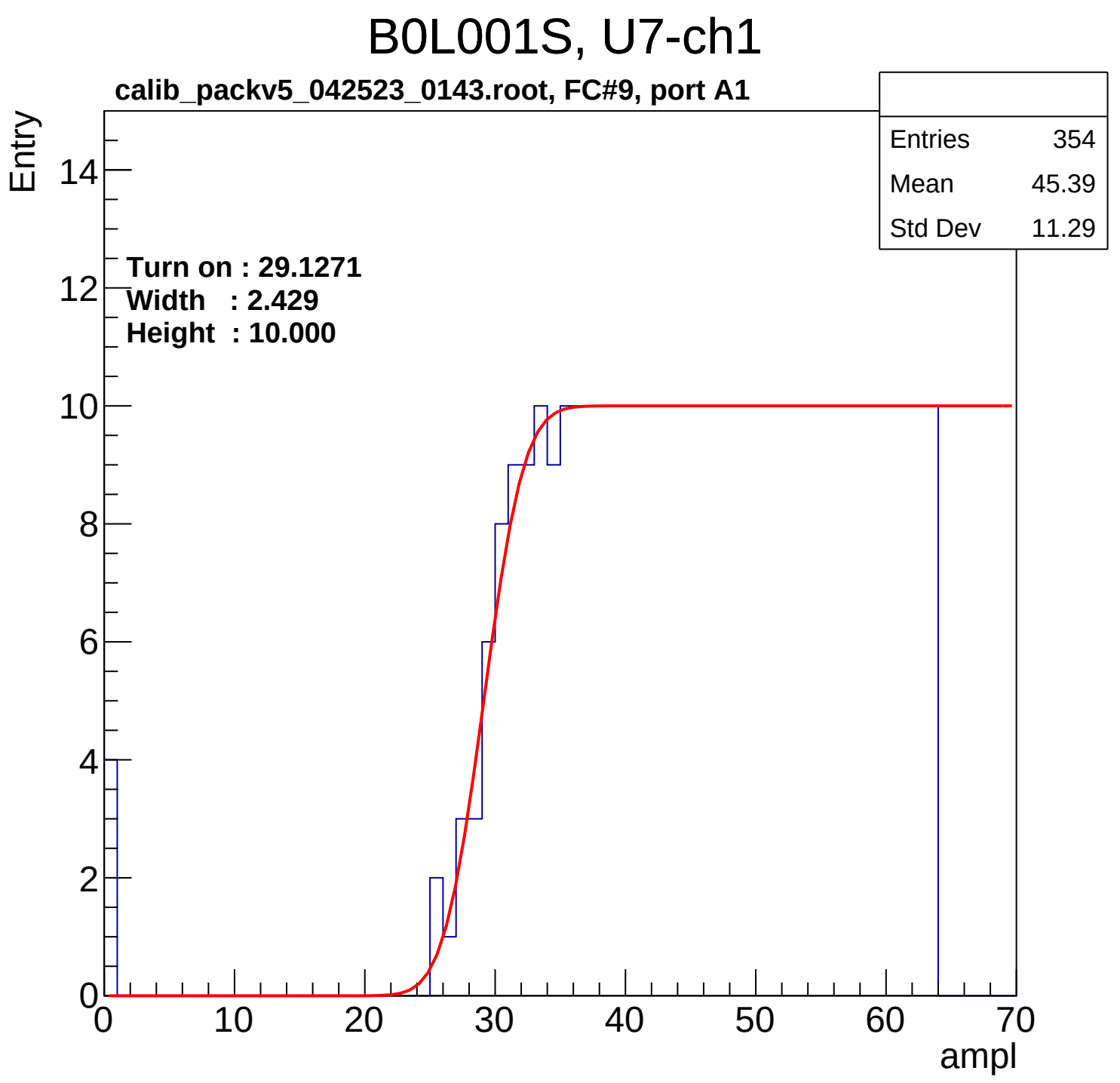
B0L001S, U7-ch1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 354
Mean 45.39
Std Dev 11.29
Turn on : 29.1271
Width : 2.429
Height : 10.000
Entry
ampl
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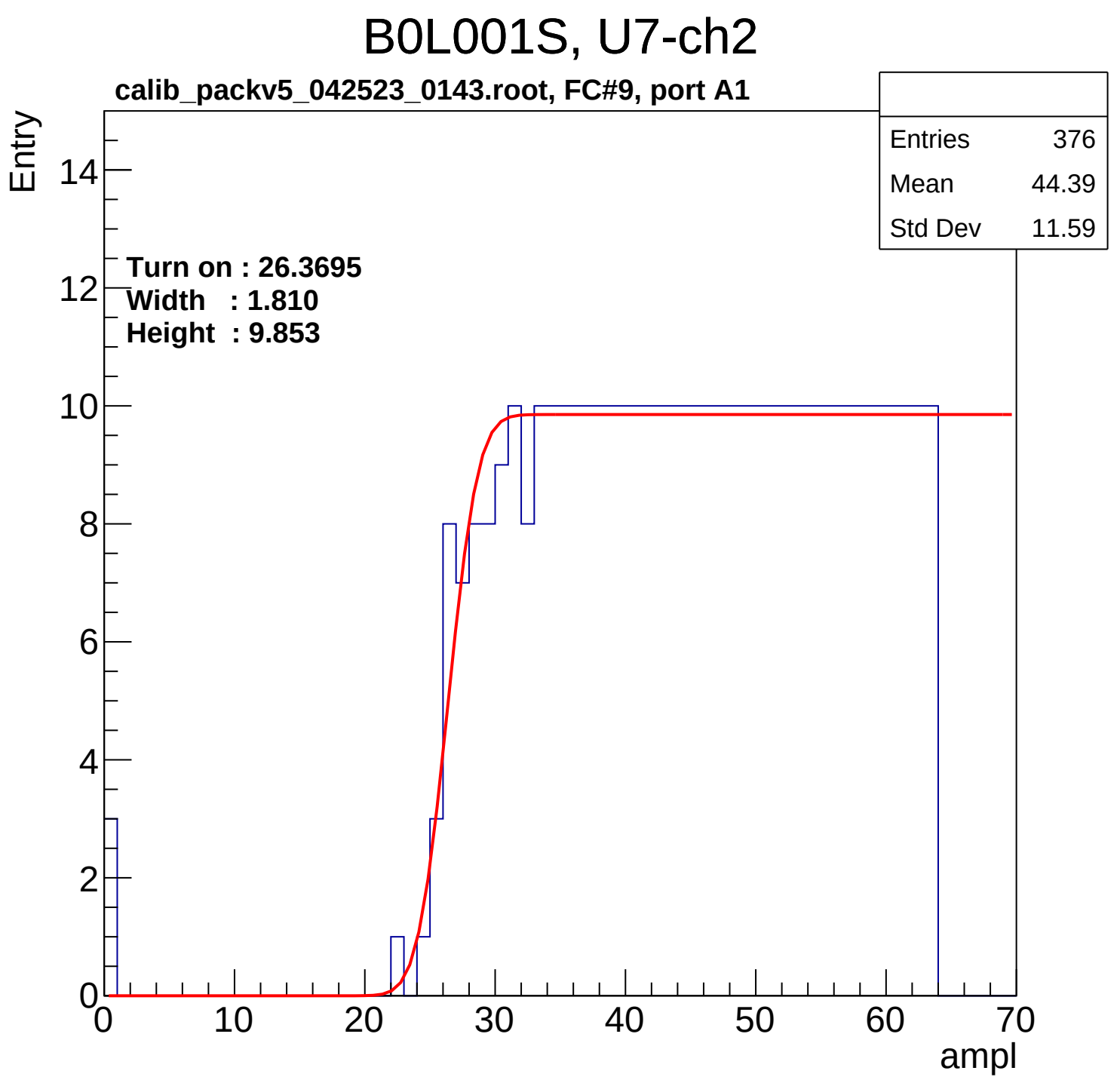
B0L001S, U7-ch2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 376
Mean 44.39
Std Dev 11.59
Turn on : 26.3695
Width : 1.810
Height : 9.853
Entry
ampl
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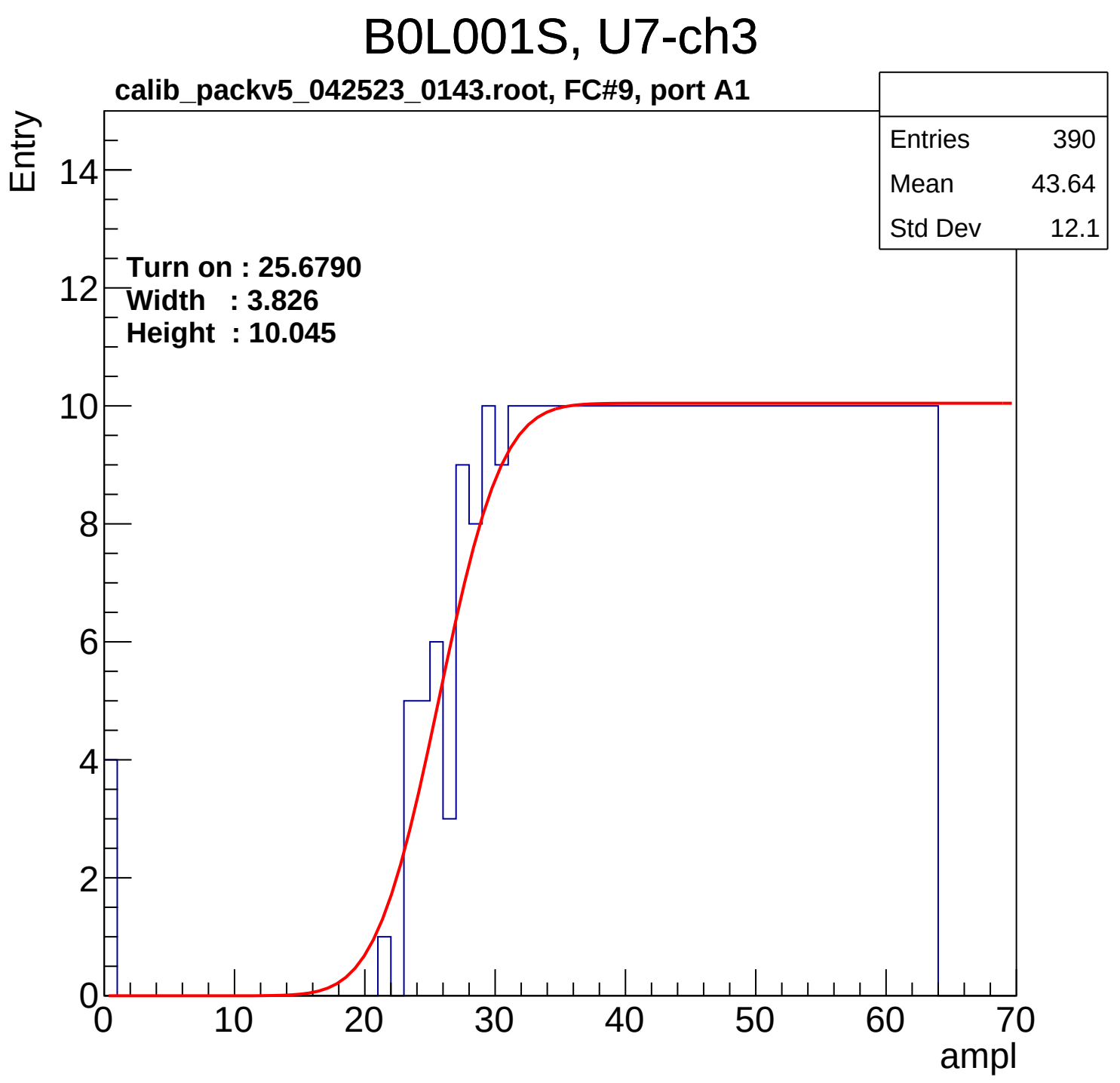
B0L001S, U7-ch3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 390
Mean 43.64
Std Dev 12.1
Turn on : 25.6790
Width : 3.826
Height : 10.045
Entry
ampl
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2
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6
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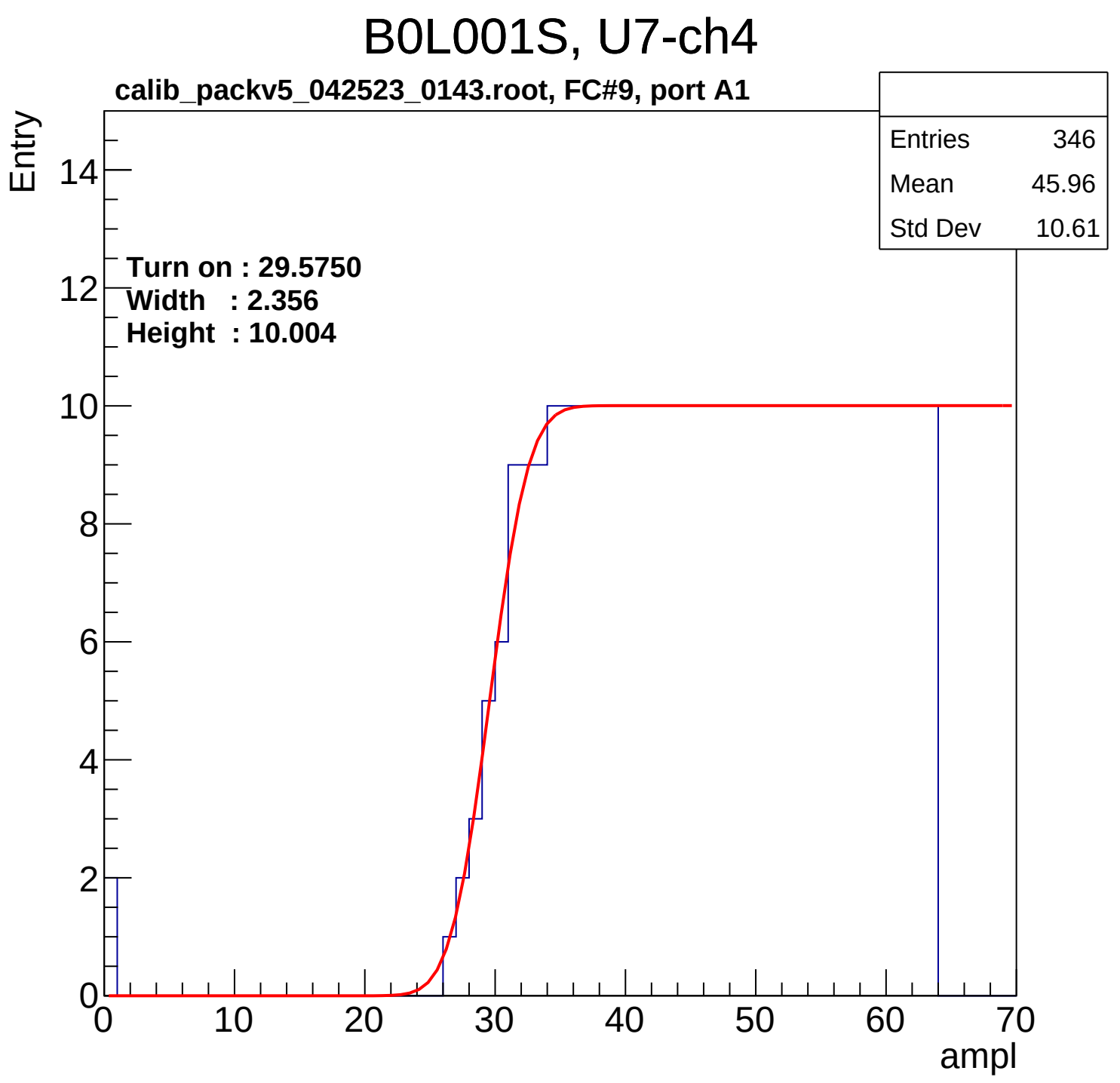
B0L001S, U7-ch4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 346
Mean 45.96
Std Dev 10.61
Turn on : 29.5750
Width : 2.356
Height : 10.004
Entry
ampl
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2
4
6
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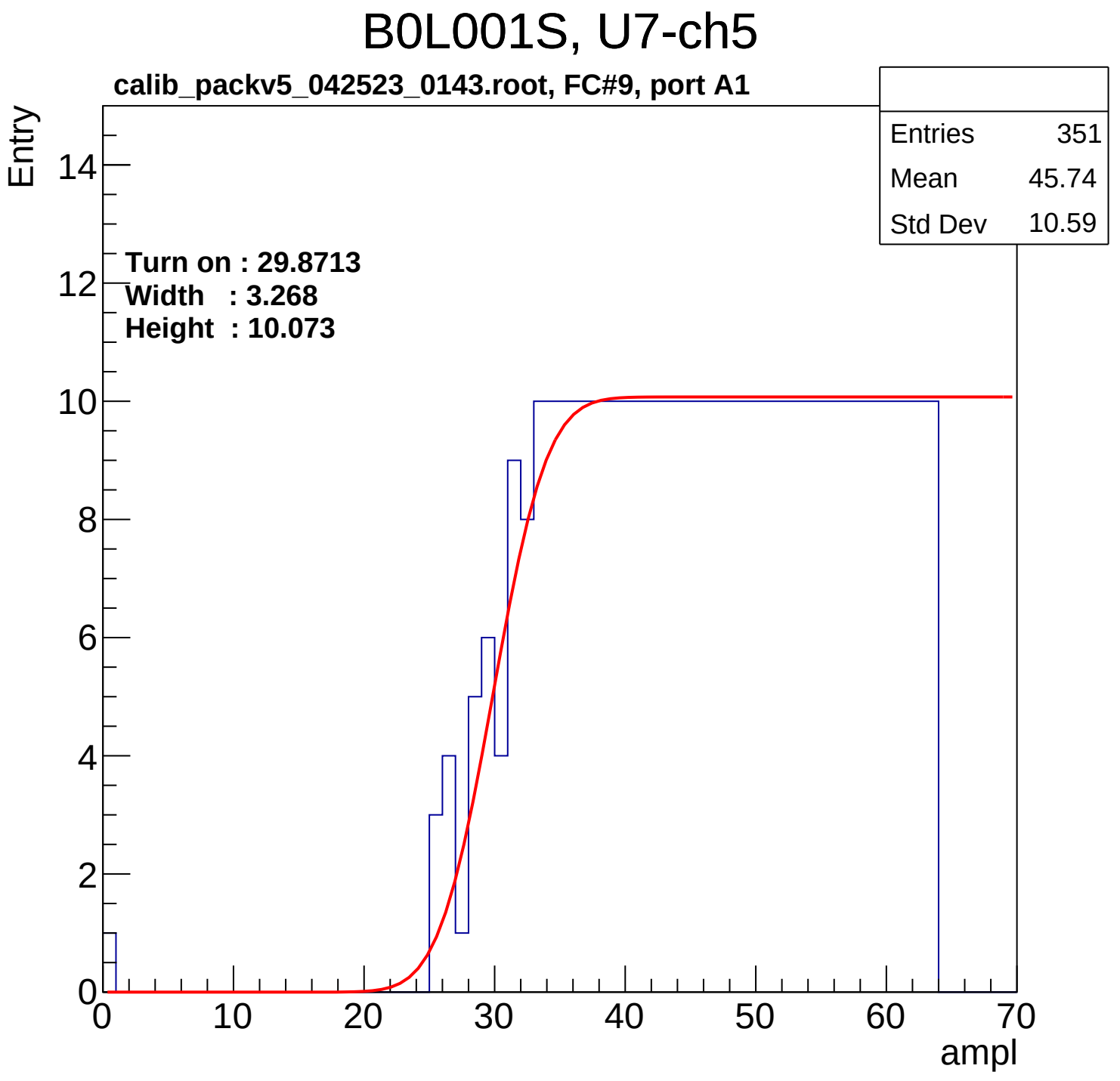
B0L001S, U7-ch5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 351
Mean 45.74
Std Dev 10.59
Turn on : 29.8713
Width : 3.268
Height : 10.073
Entry
ampl
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2
4
6
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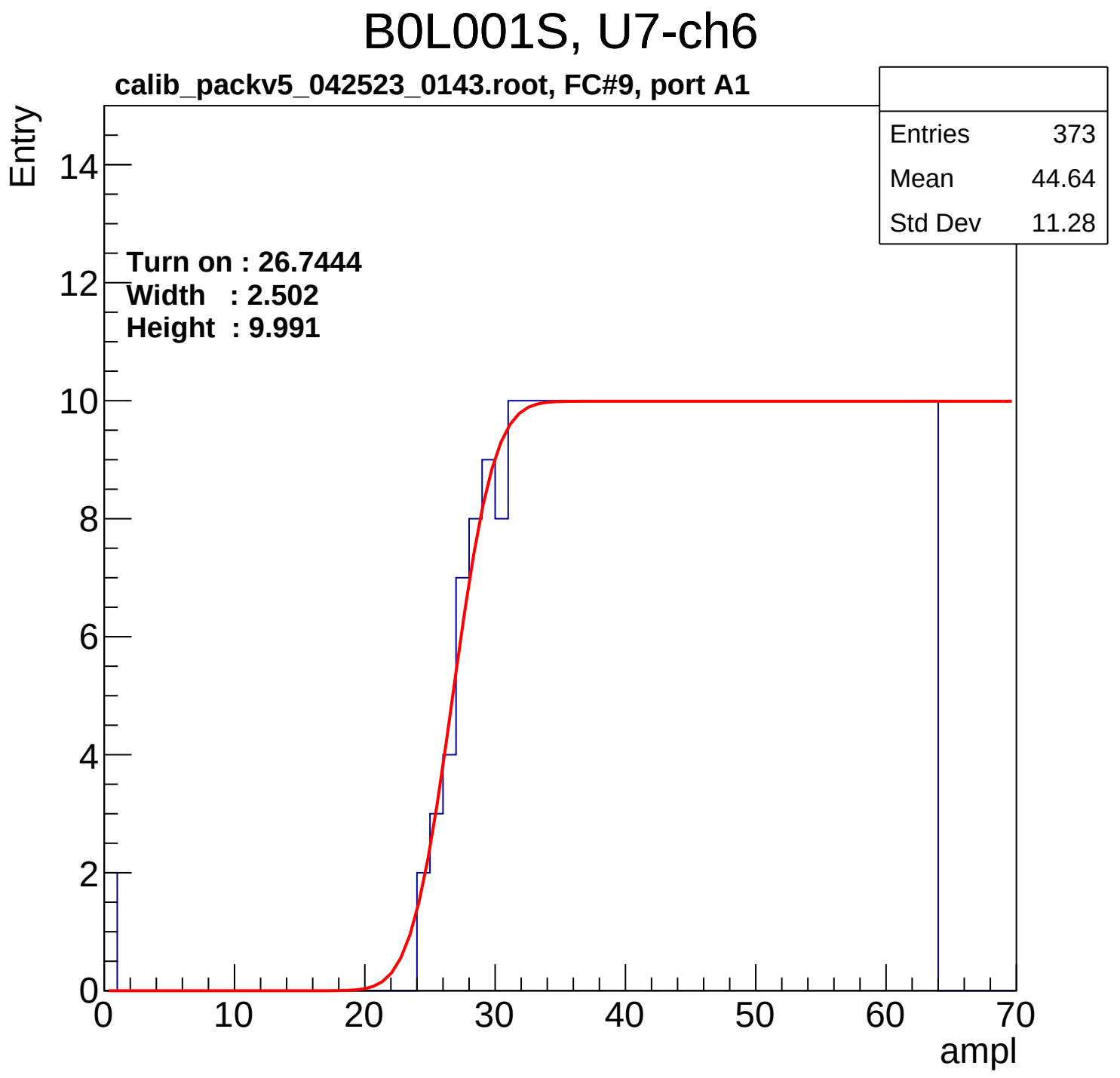
B0L001S, U7-ch6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 373
Mean 44.64
Std Dev 11.28
Turn on : 26.7444
Width : 2.502
Height : 9.991
Entry
ampl
0
2
4
6
8
10
12
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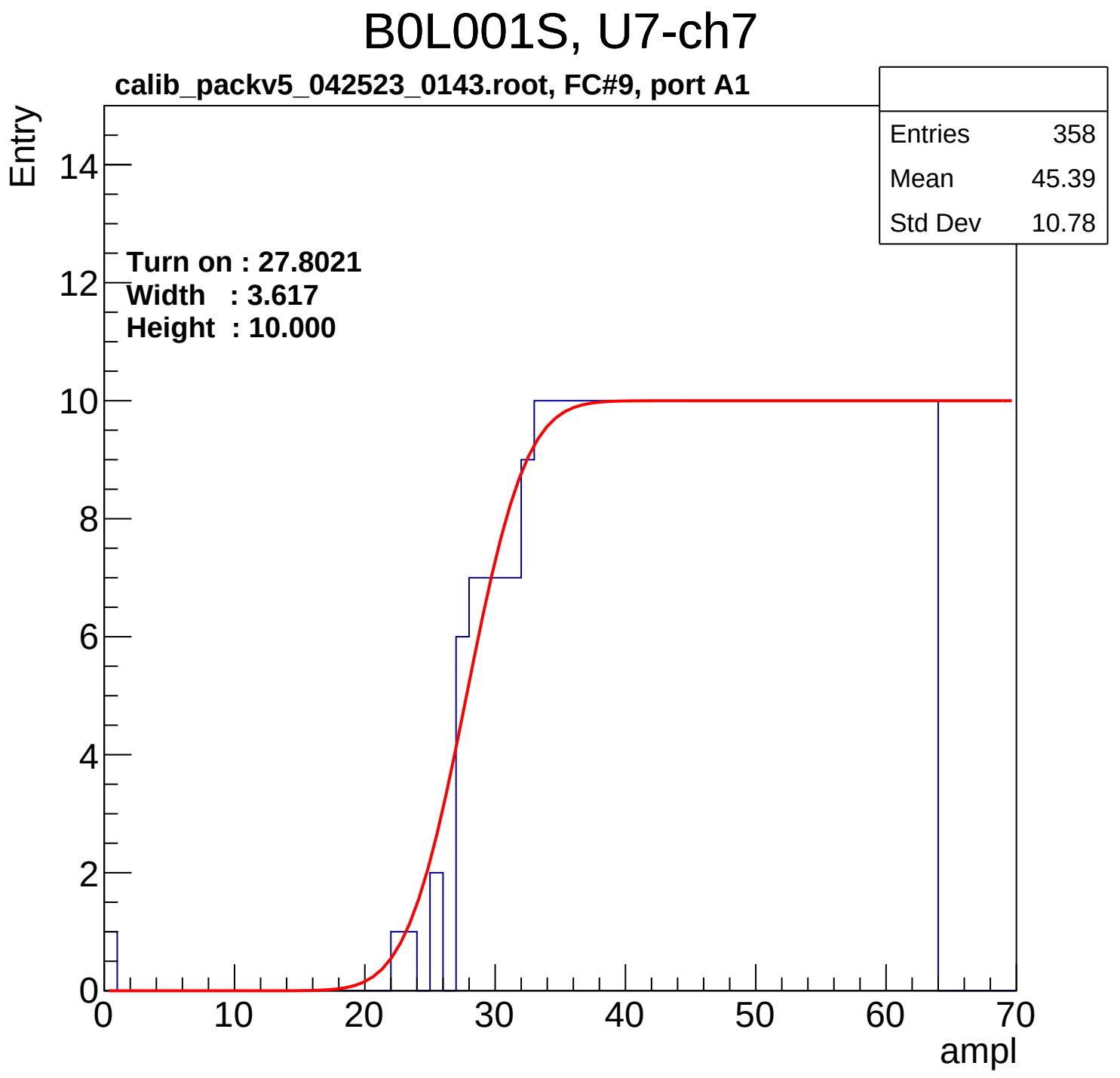
B0L001S, U7-ch7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 358
Mean 45.39
Std Dev 10.78
Turn on : 27.8021
Width : 3.617
Height : 10.000
Entry
ampl
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2
4
6
8
10
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0
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60
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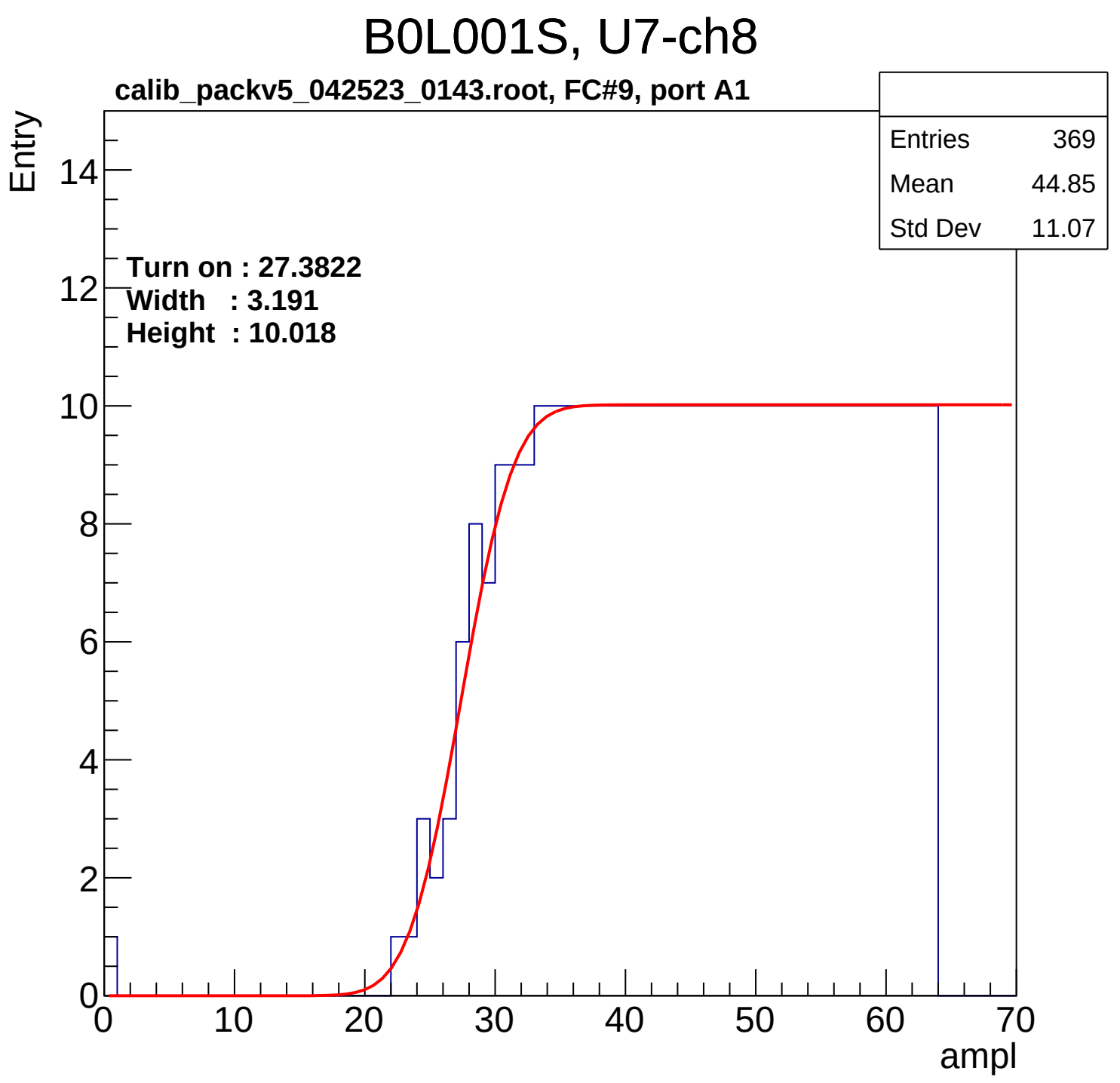
B0L001S, U7-ch8
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.85
Std Dev 11.07
Turn on : 27.3822
Width : 3.191
Height : 10.018
Entry
ampl
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6
8
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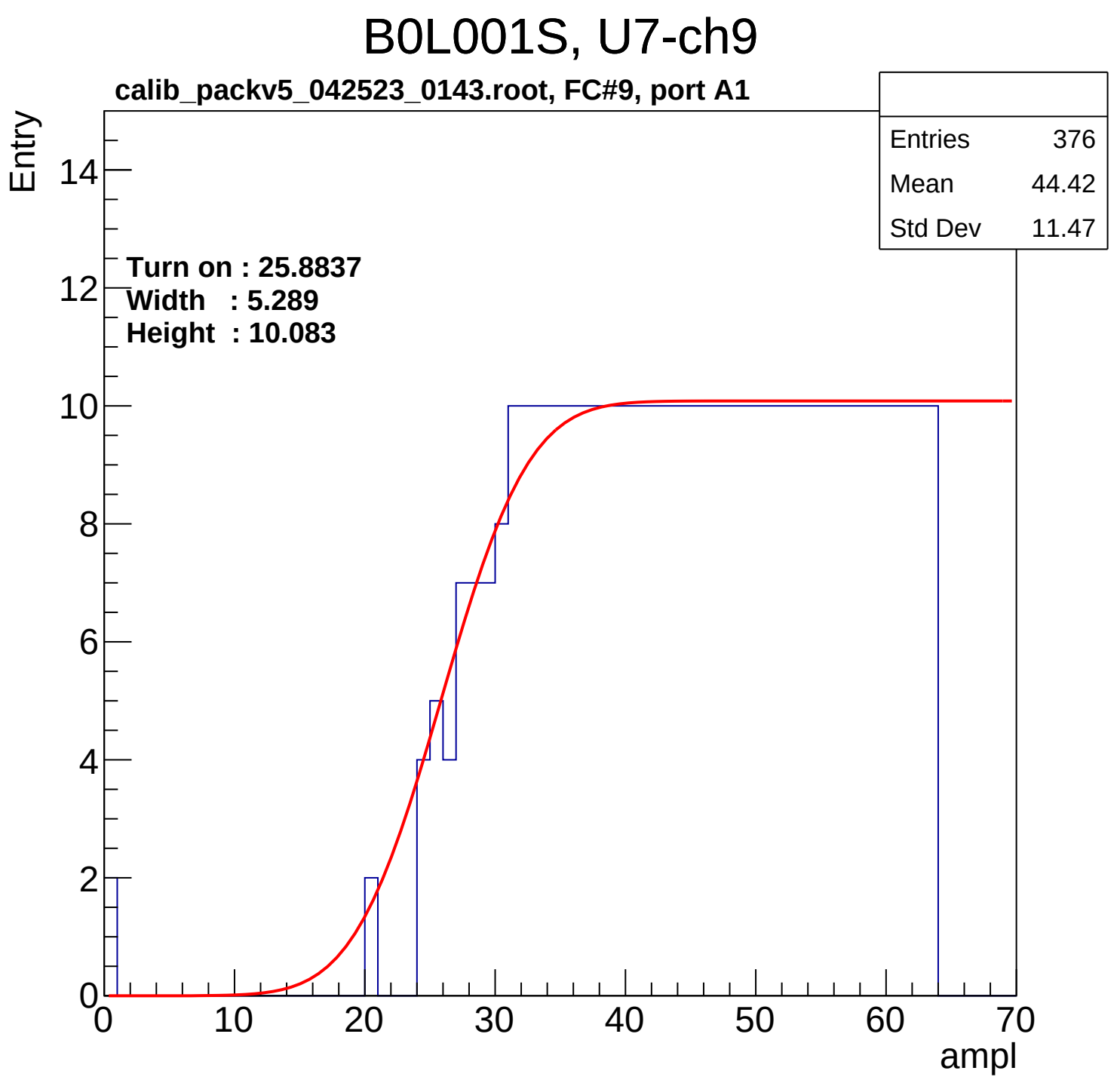
B0L001S, U7-ch9
calib_packv5_042523_0143.root, FC#9, port A1
Entries 376
Mean 44.42
Std Dev 11.47
Turn on : 25.8837
Width : 5.289
Height : 10.083
Entry
ampl
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2
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6
8
10
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0
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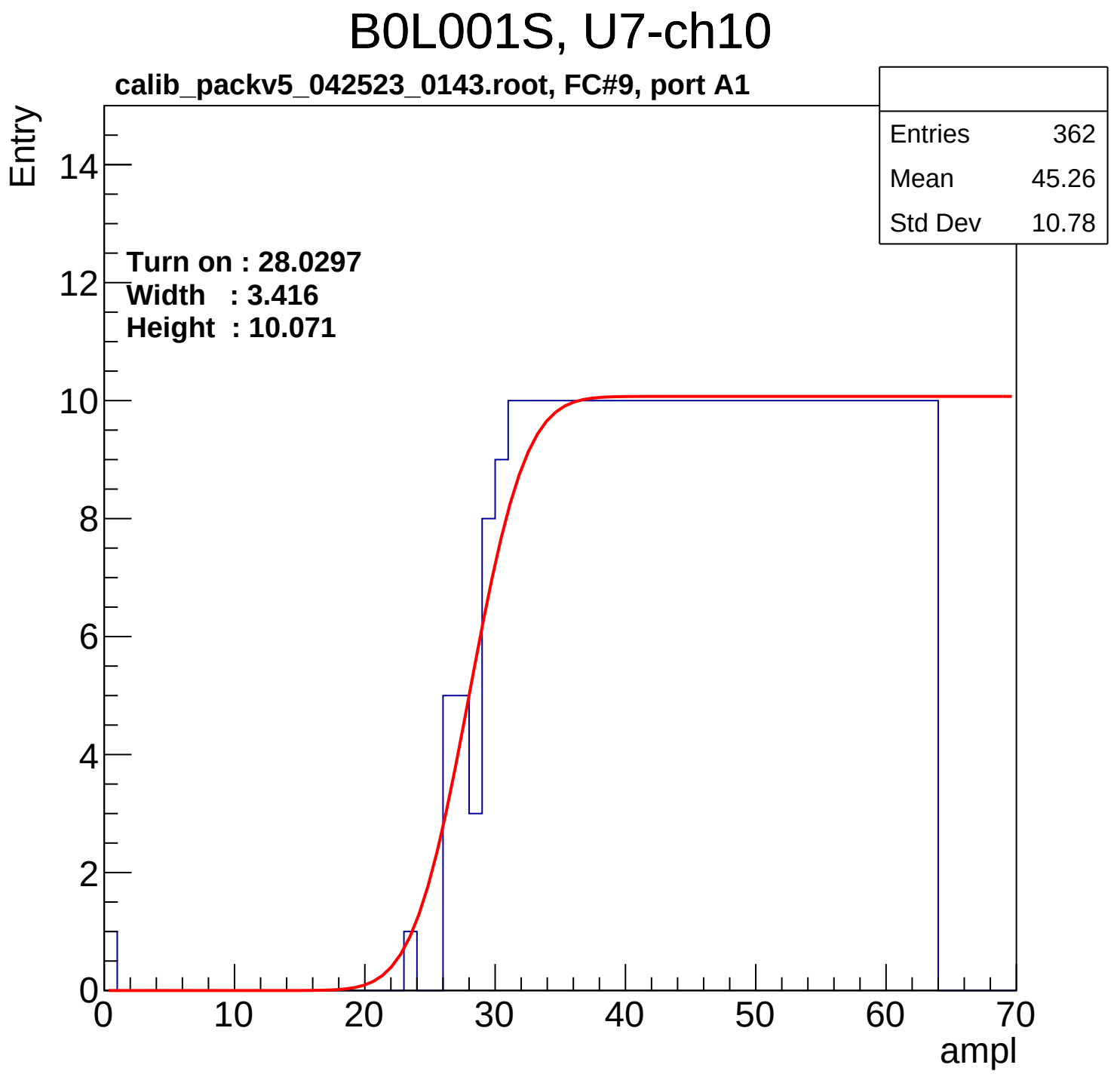
B0L001S, U7-ch10
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 45.26
Std Dev 10.78
Turn on : 28.0297
Width : 3.416
Height : 10.071
Entry
ampl
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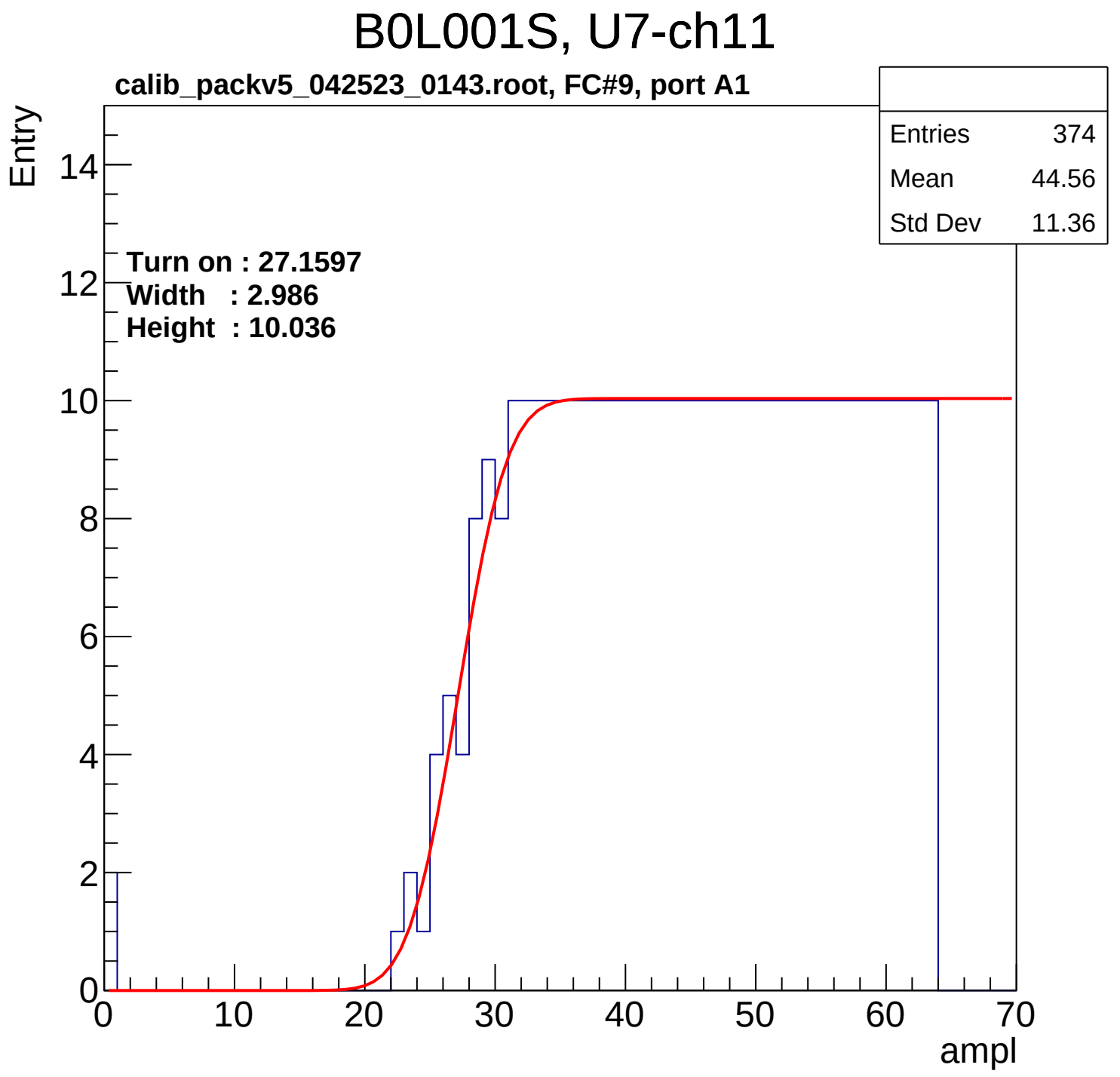
B0L001S, U7-ch11
calib_packv5_042523_0143.root, FC#9, port A1
Entries 374
Mean 44.56
Std Dev 11.36
Turn on : 27.1597
Width : 2.986
Height : 10.036
Entry
ampl
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2
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6
8
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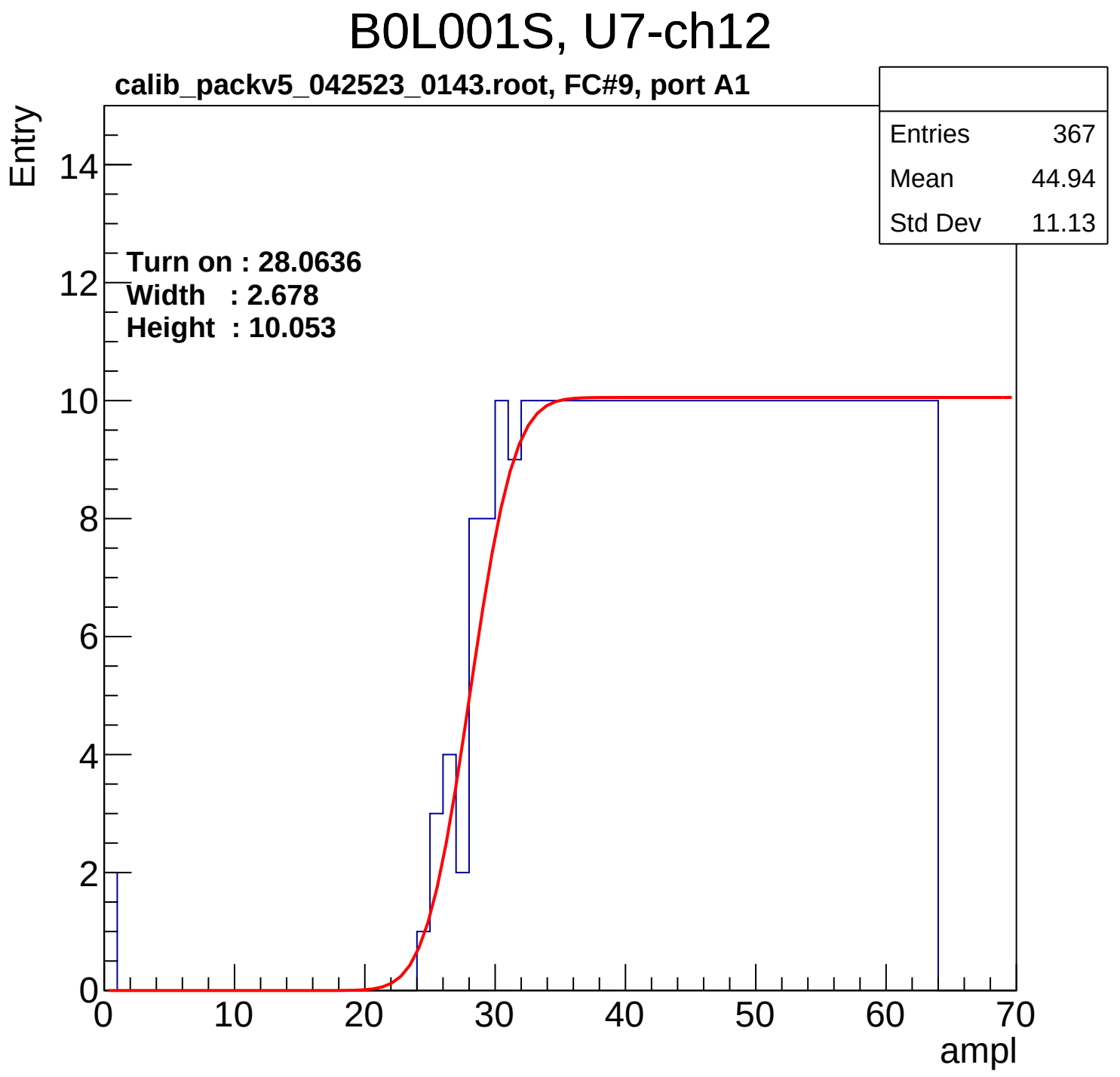
B0L001S, U7-ch12
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.94
Std Dev 11.13
Turn on : 28.0636
Width : 2.678
Height : 10.053
Entry
ampl
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6
8
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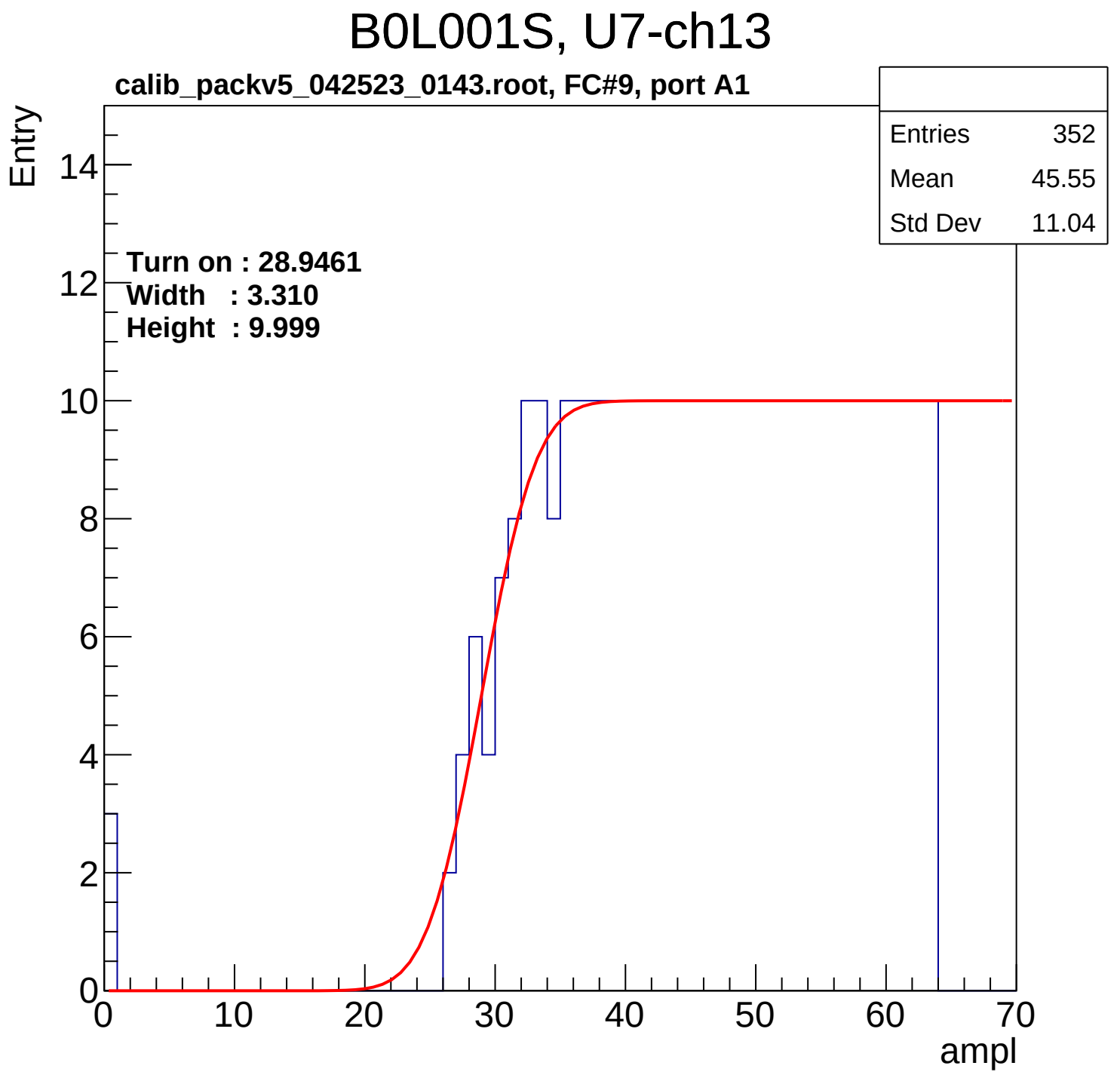
B0L001S, U7-ch13
calib_packv5_042523_0143.root, FC#9, port A1
Entries 352
Mean 45.55
Std Dev 11.04
Turn on : 28.9461
Width : 3.310
Height : 9.999
Entry
ampl
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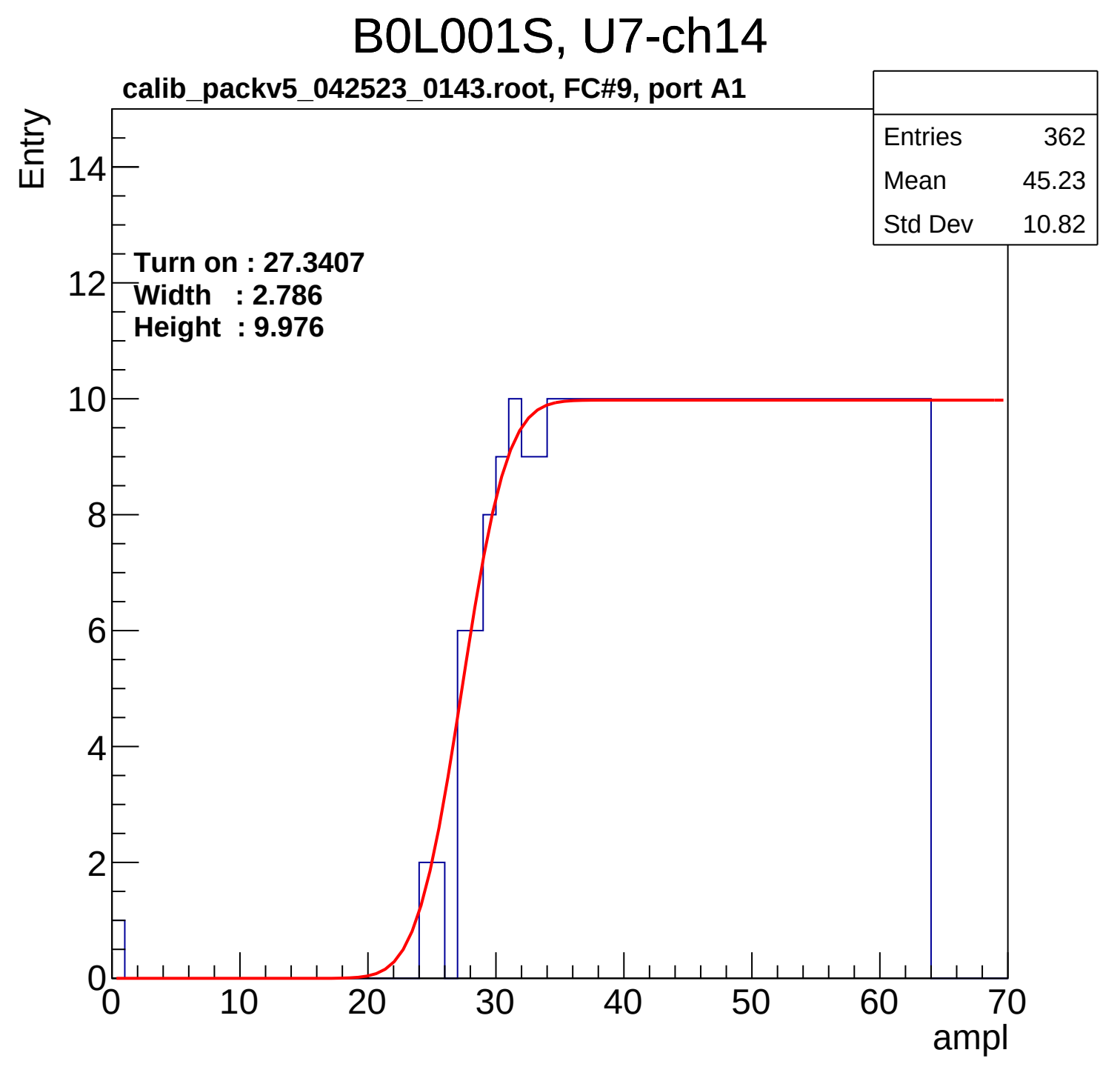
B0L001S, U7-ch14
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 45.23
Std Dev 10.82
Turn on : 27.3407
Width : 2.786
Height : 9.976
Entry
ampl
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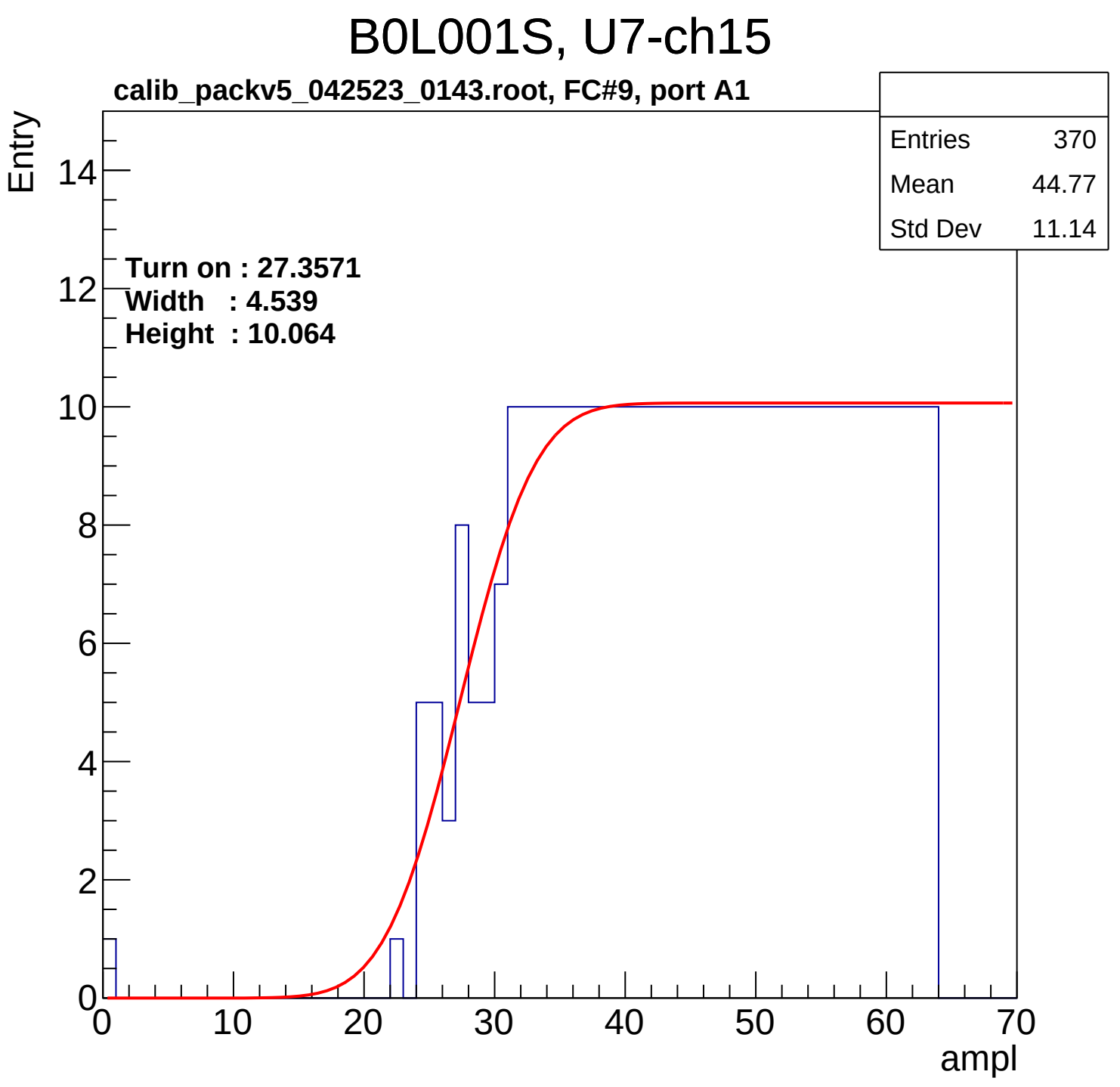
B0L001S, U7-ch15
calib_packv5_042523_0143.root, FC#9, port A1
Entries 370
Mean 44.77
Std Dev 11.14
Turn on : 27.3571
Width : 4.539
Height : 10.064
Entry
ampl
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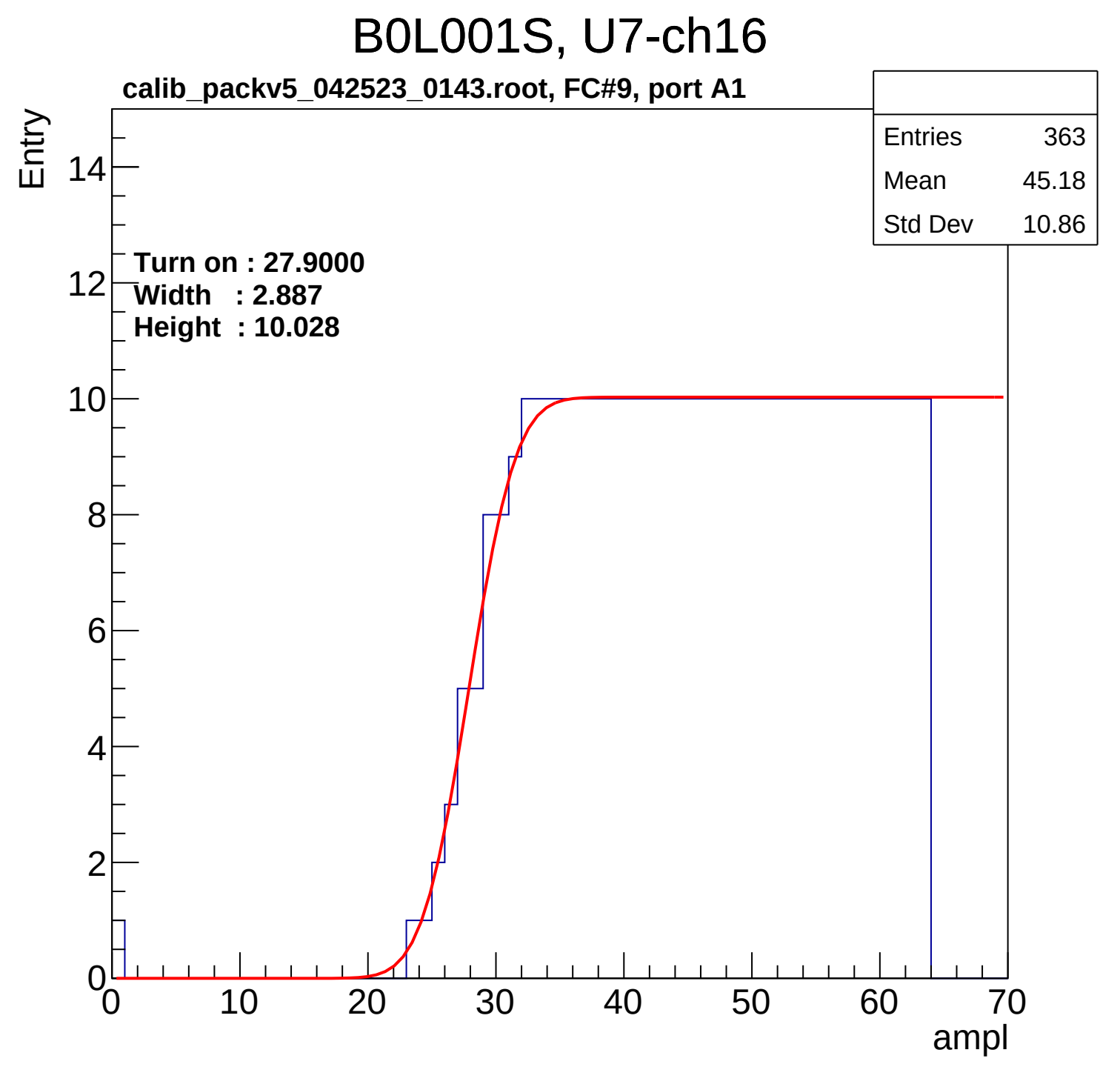
B0L001S, U7-ch16
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 45.18
Std Dev 10.86
Turn on : 27.9000
Width : 2.887
Height : 10.028
Entry
ampl
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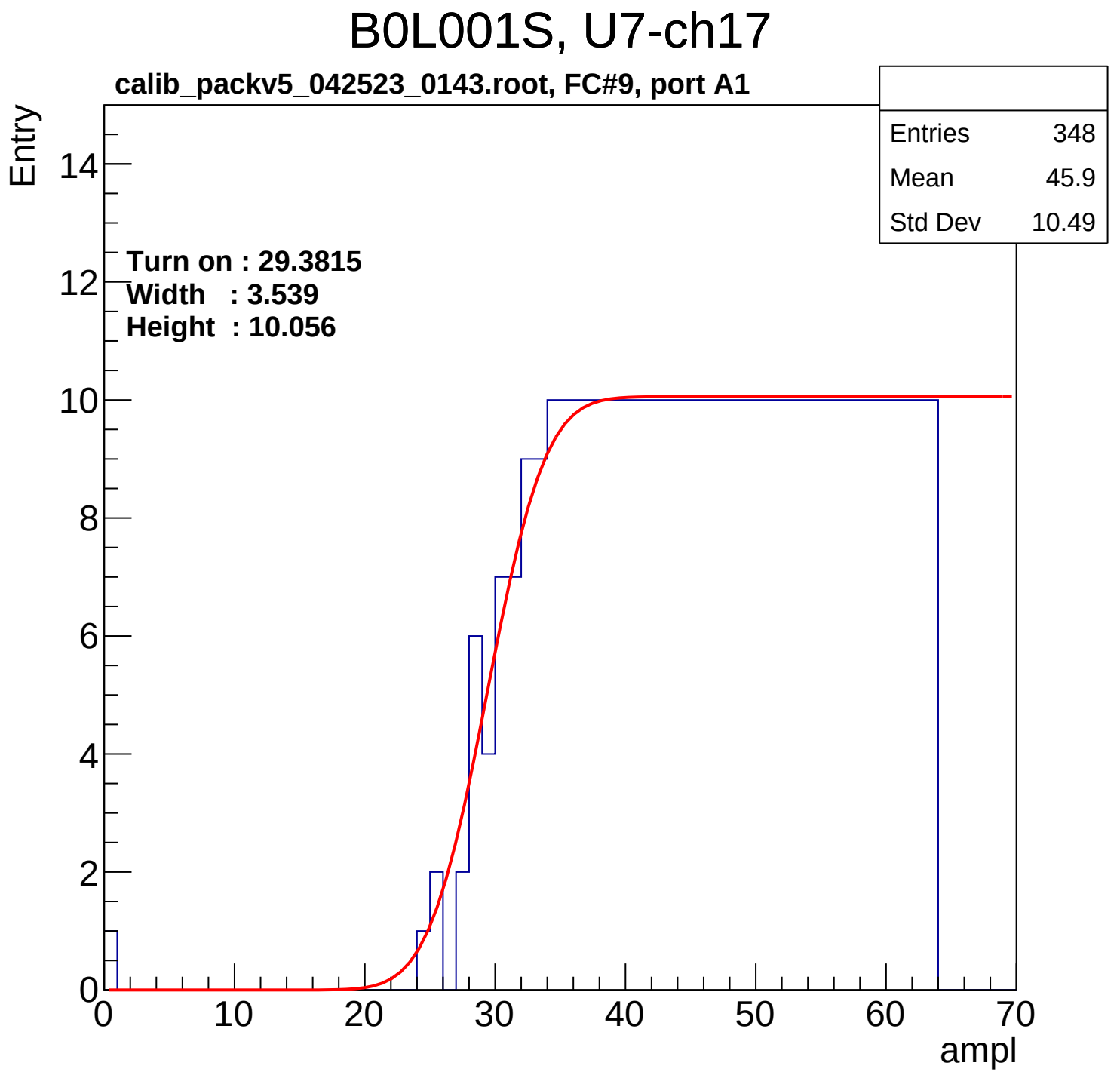
B0L001S, U7-ch17
calib_packv5_042523_0143.root, FC#9, port A1
Entries 348
Mean 45.9
Std Dev 10.49
Turn on : 29.3815
Width : 3.539
Height : 10.056
Entry
ampl
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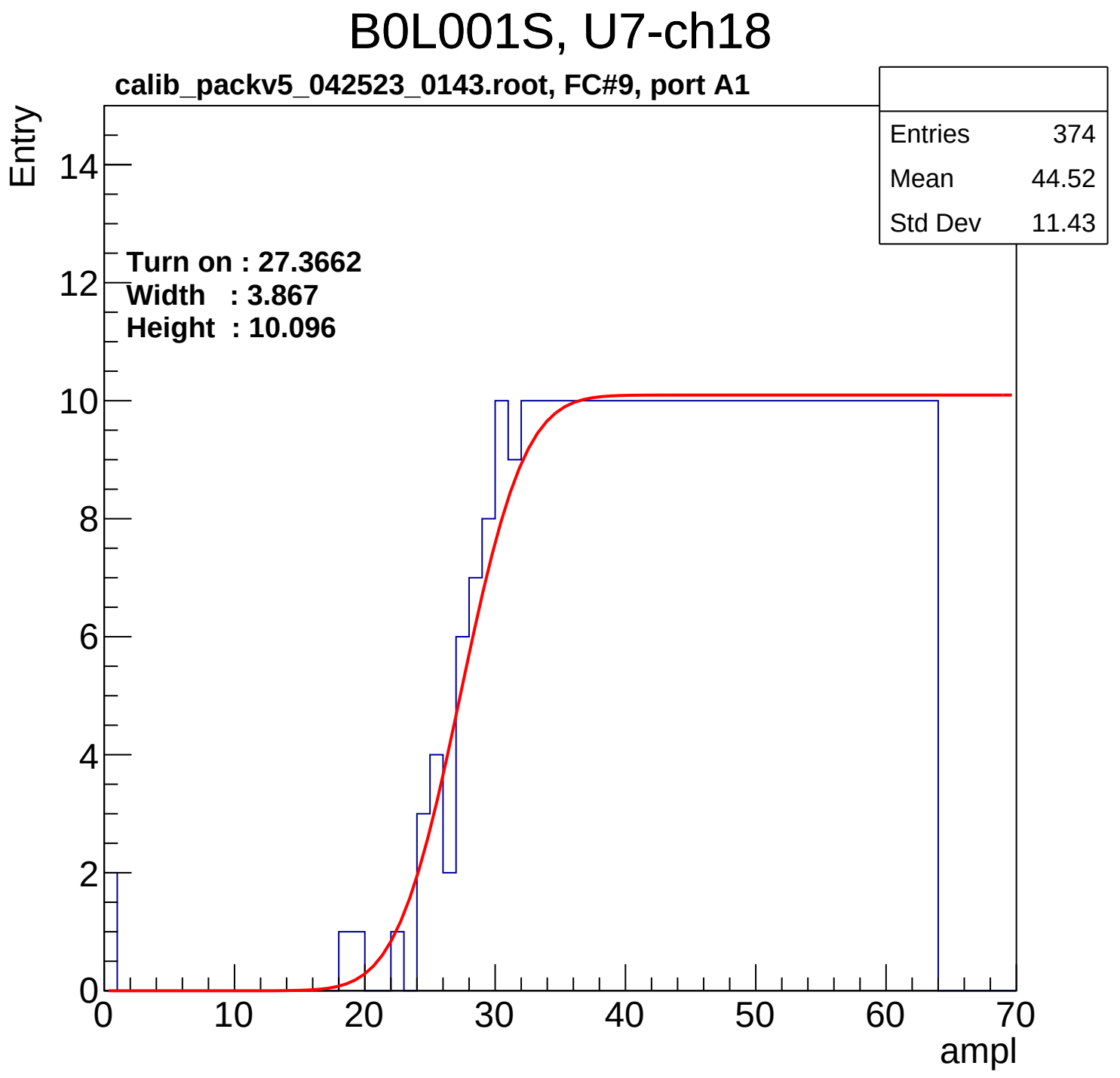
B0L001S, U7-ch18
calib_packv5_042523_0143.root, FC#9, port A1
Entries 374
Mean 44.52
Std Dev 11.43
Turn on : 27.3662
Width : 3.867
Height : 10.096
Entry
ampl
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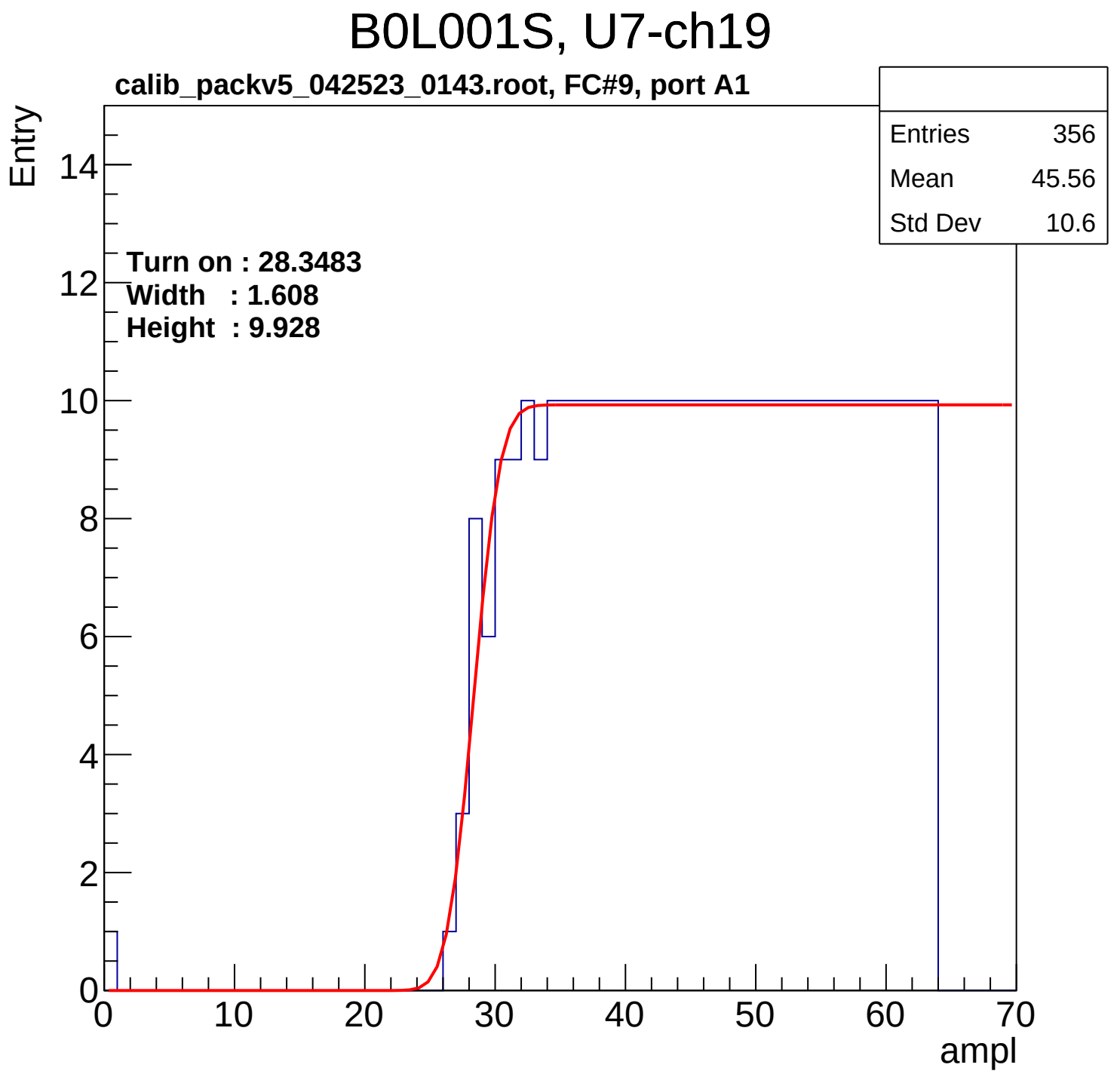
B0L001S, U7-ch19
calib_packv5_042523_0143.root, FC#9, port A1
Entries 356
Mean 45.56
Std Dev 10.6
Turn on : 28.3483
Width : 1.608
Height : 9.928
Entry
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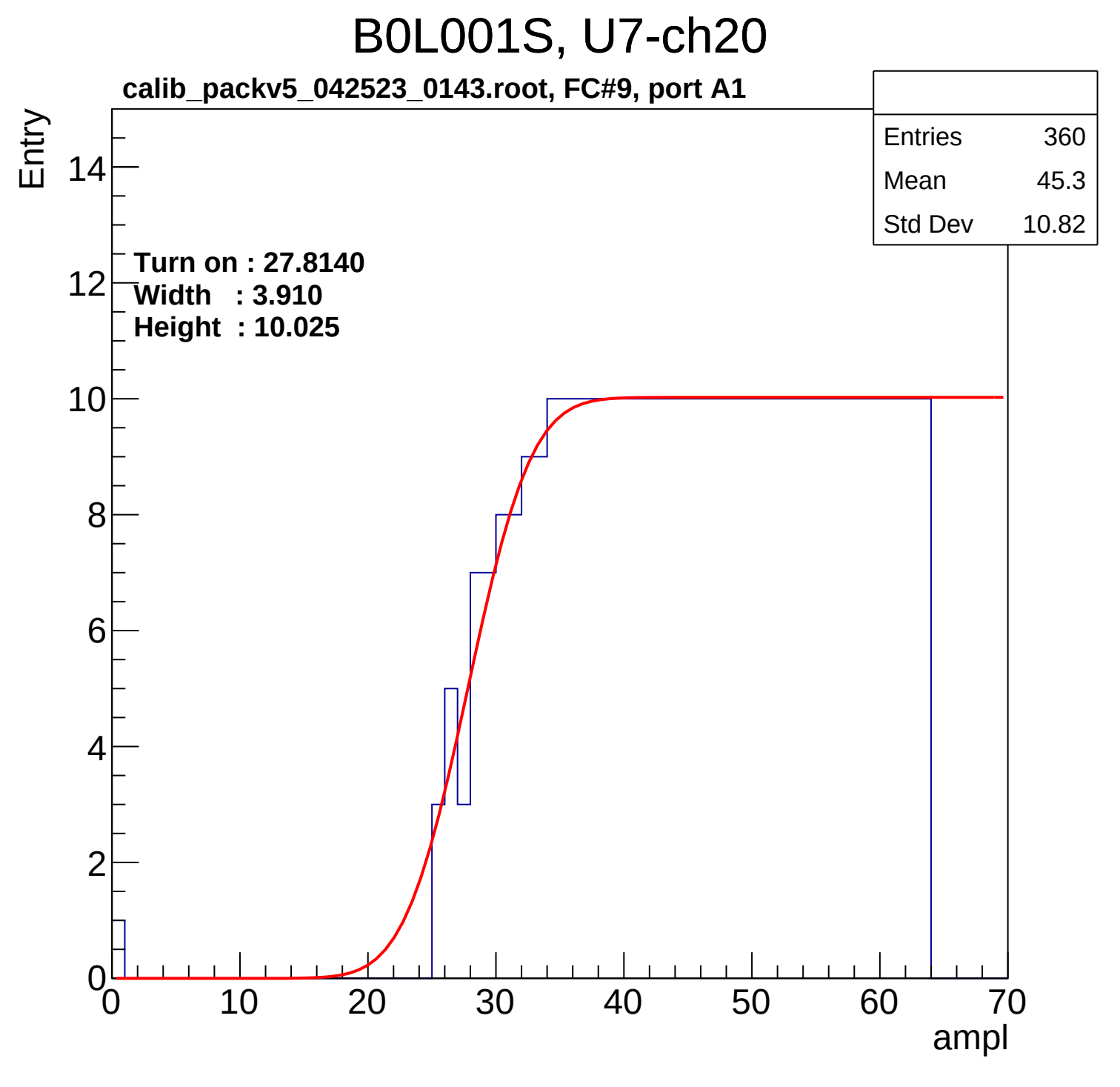
B0L001S, U7-ch20
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 45.3
Std Dev 10.82
Turn on : 27.8140
Width : 3.910
Height : 10.025
Entry
ampl
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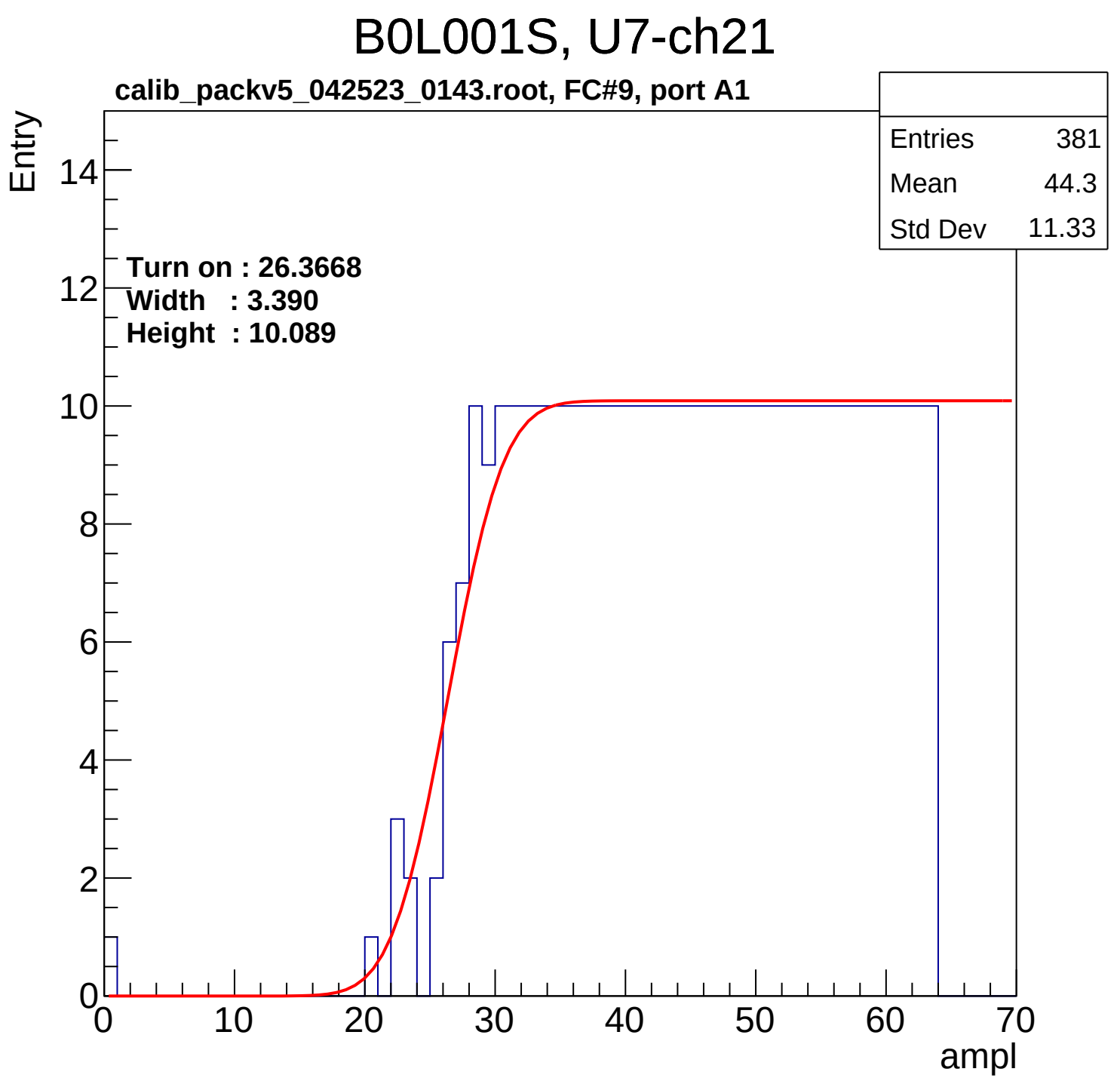
B0L001S, U7-ch21
calib_packv5_042523_0143.root, FC#9, port A1
Entries 381
Mean 44.3
Std Dev 11.33
Turn on : 26.3668
Width : 3.390
Height : 10.089
Entry
ampl
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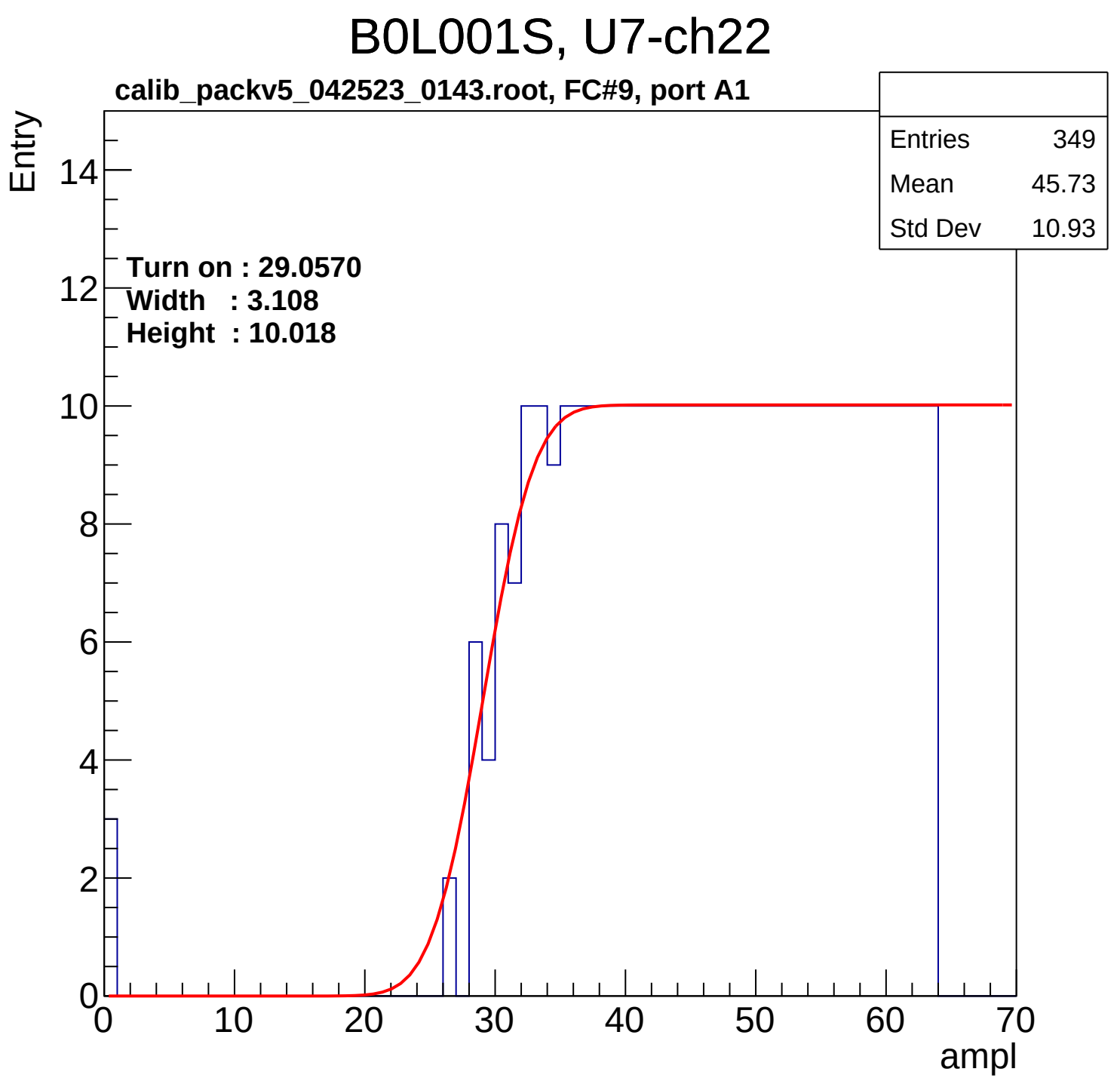
B0L001S, U7-ch22
calib_packv5_042523_0143.root, FC#9, port A1
Entries 349
Mean 45.73
Std Dev 10.93
Turn on : 29.0570
Width : 3.108
Height : 10.018
Entry
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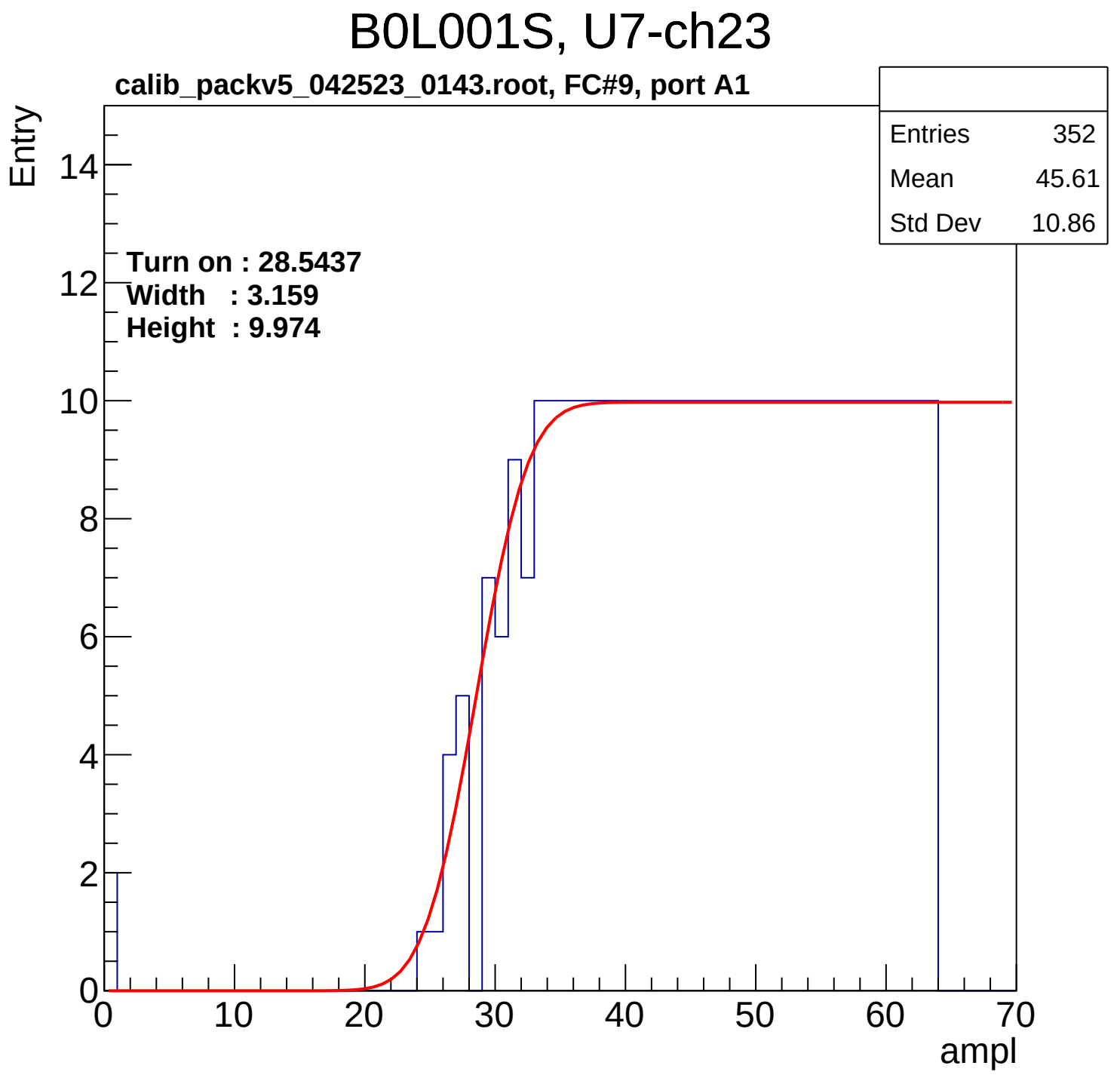
B0L001S, U7-ch23
calib_packv5_042523_0143.root, FC#9, port A1
Entries 352
Mean 45.61
Std Dev 10.86
Turn on : 28.5437
Width : 3.159
Height : 9.974
Entry
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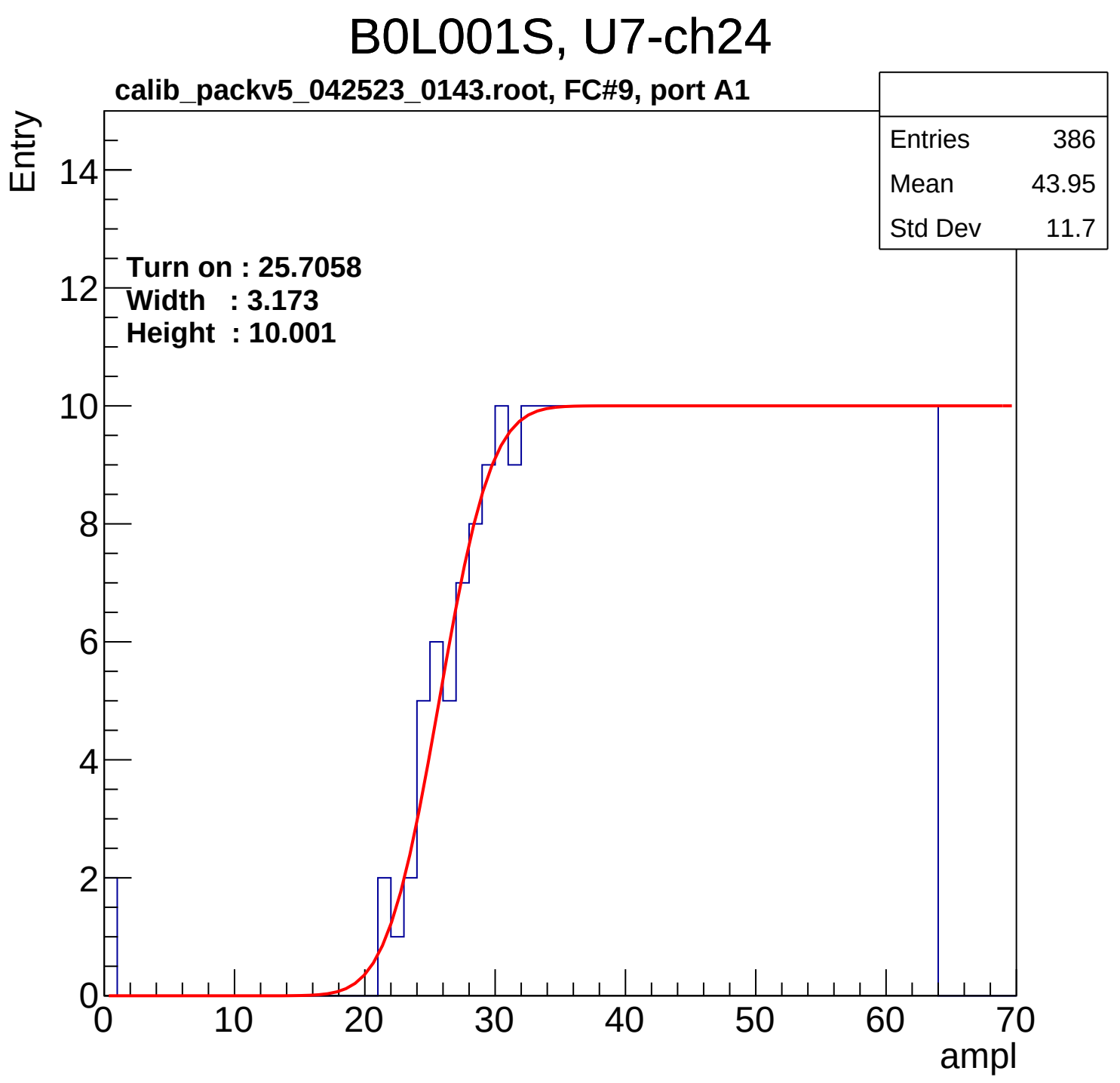
B0L001S, U7-ch24
calib_packv5_042523_0143.root, FC#9, port A1
Entries 386
Mean 43.95
Std Dev 11.7
Turn on : 25.7058
Width : 3.173
Height : 10.001
Entry
ampl
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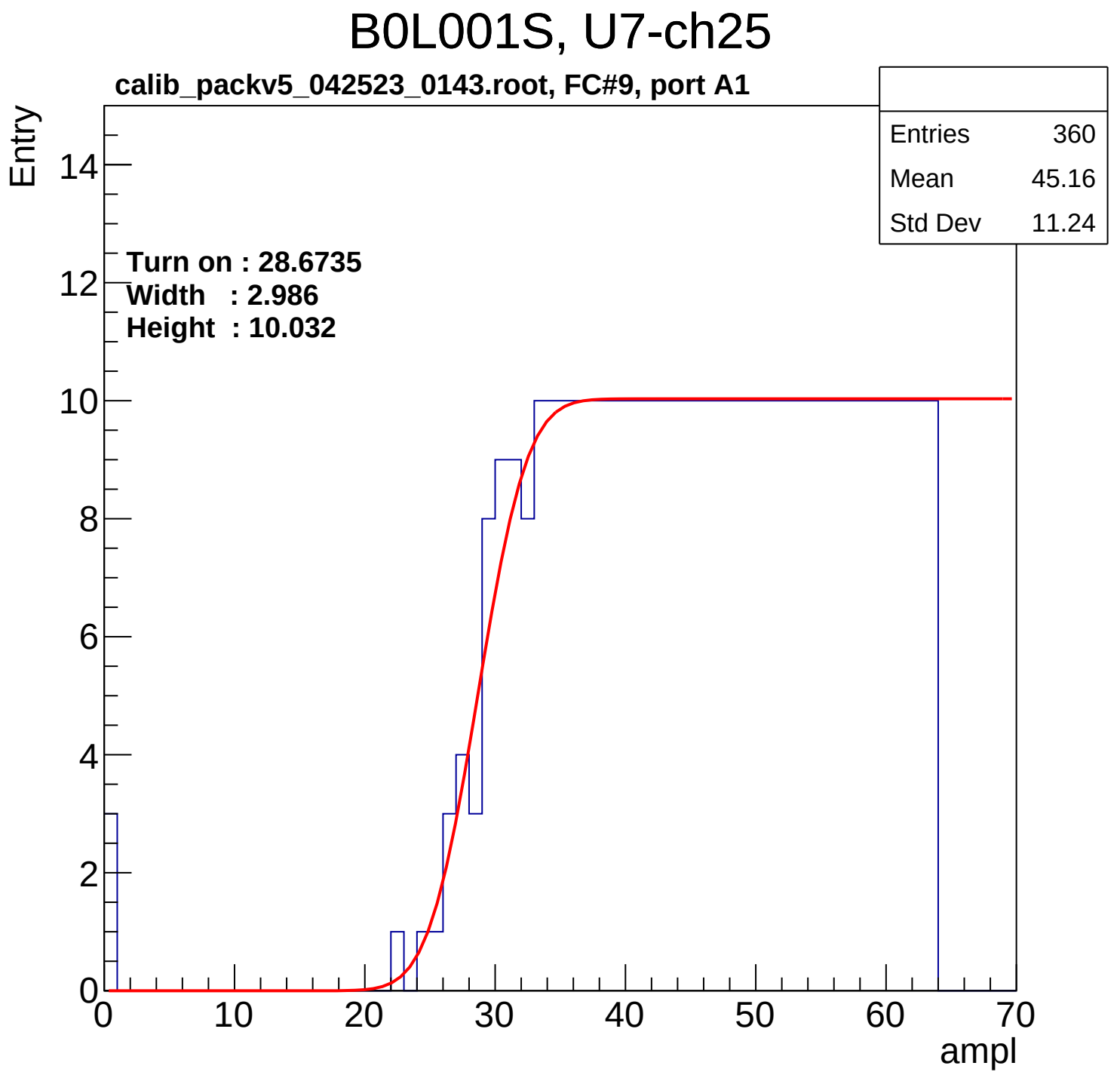
B0L001S, U7-ch25
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 45.16
Std Dev 11.24
Turn on : 28.6735
Width : 2.986
Height : 10.032
Entry
ampl
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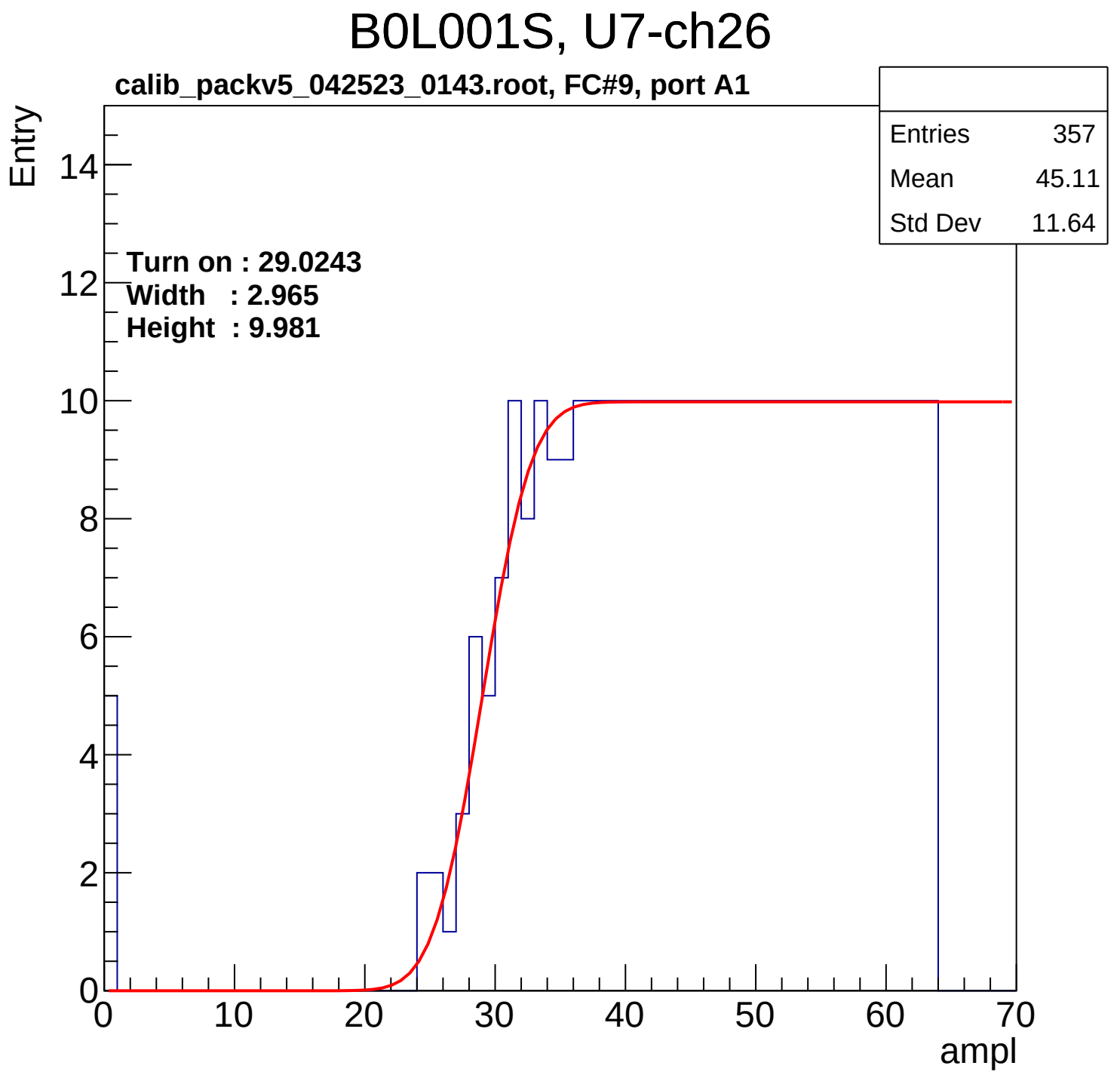
B0L001S, U7-ch26
calib_packv5_042523_0143.root, FC#9, port A1
Entries 357
Mean 45.11
Std Dev 11.64
Turn on : 29.0243
Width : 2.965
Height : 9.981
Entry
ampl
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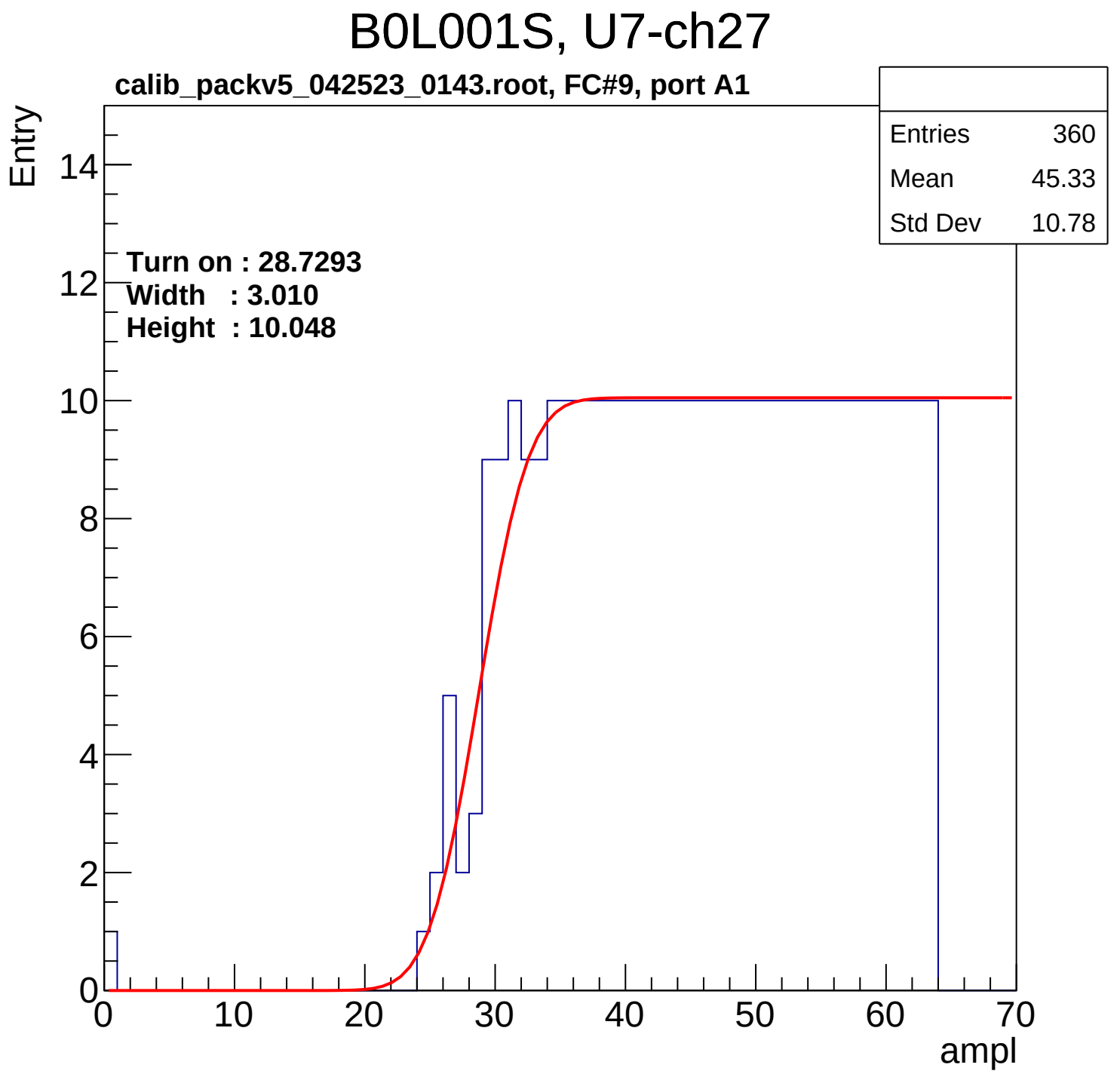
B0L001S, U7-ch27
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 45.33
Std Dev 10.78
Turn on : 28.7293
Width : 3.010
Height : 10.048
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ampl
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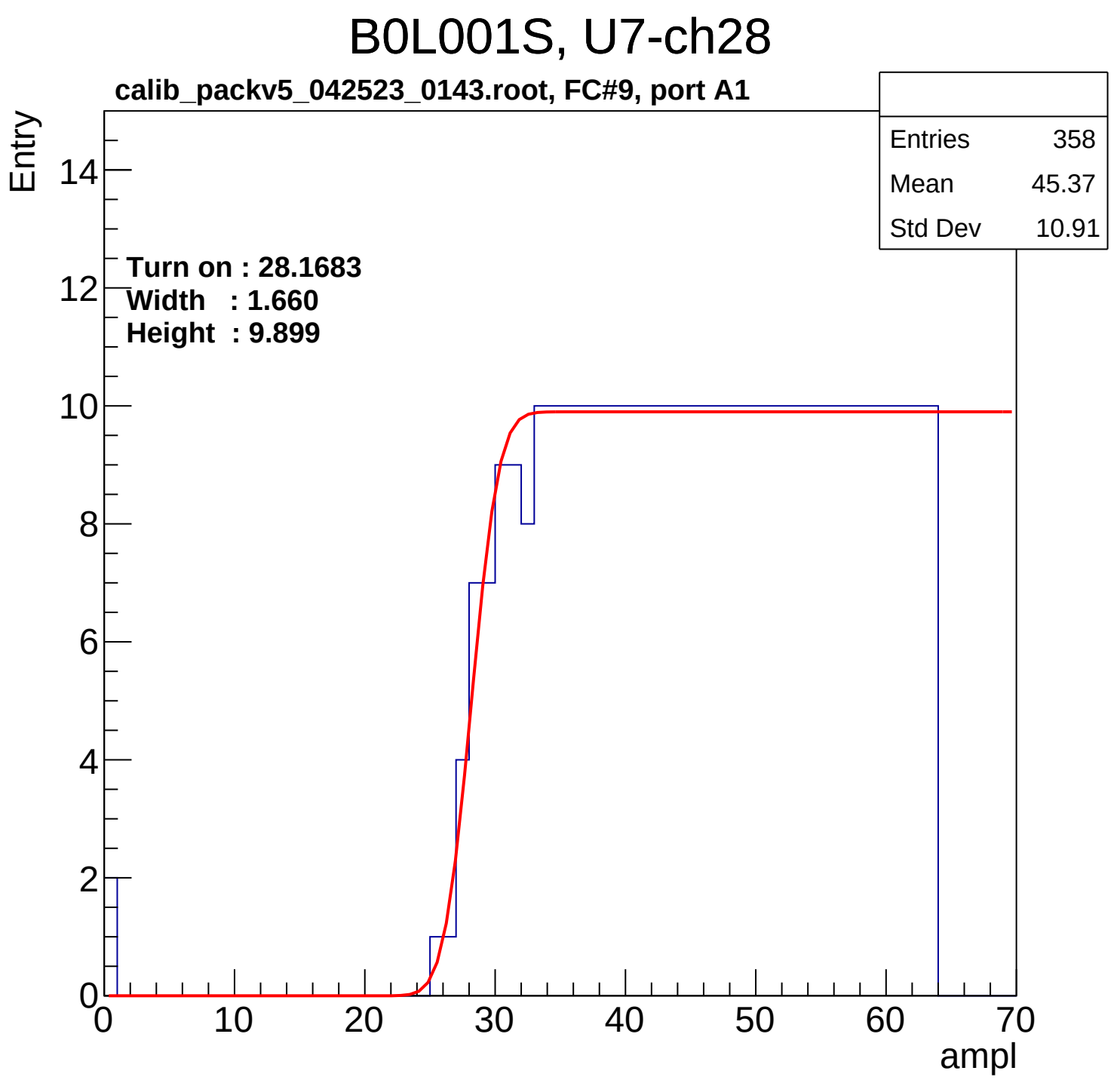
B0L001S, U7-ch28
calib_packv5_042523_0143.root, FC#9, port A1
Entries 358
Mean 45.37
Std Dev 10.91
Turn on : 28.1683
Width : 1.660
Height : 9.899
Entry
ampl
0
2
4
6
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10
12
14
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10
20
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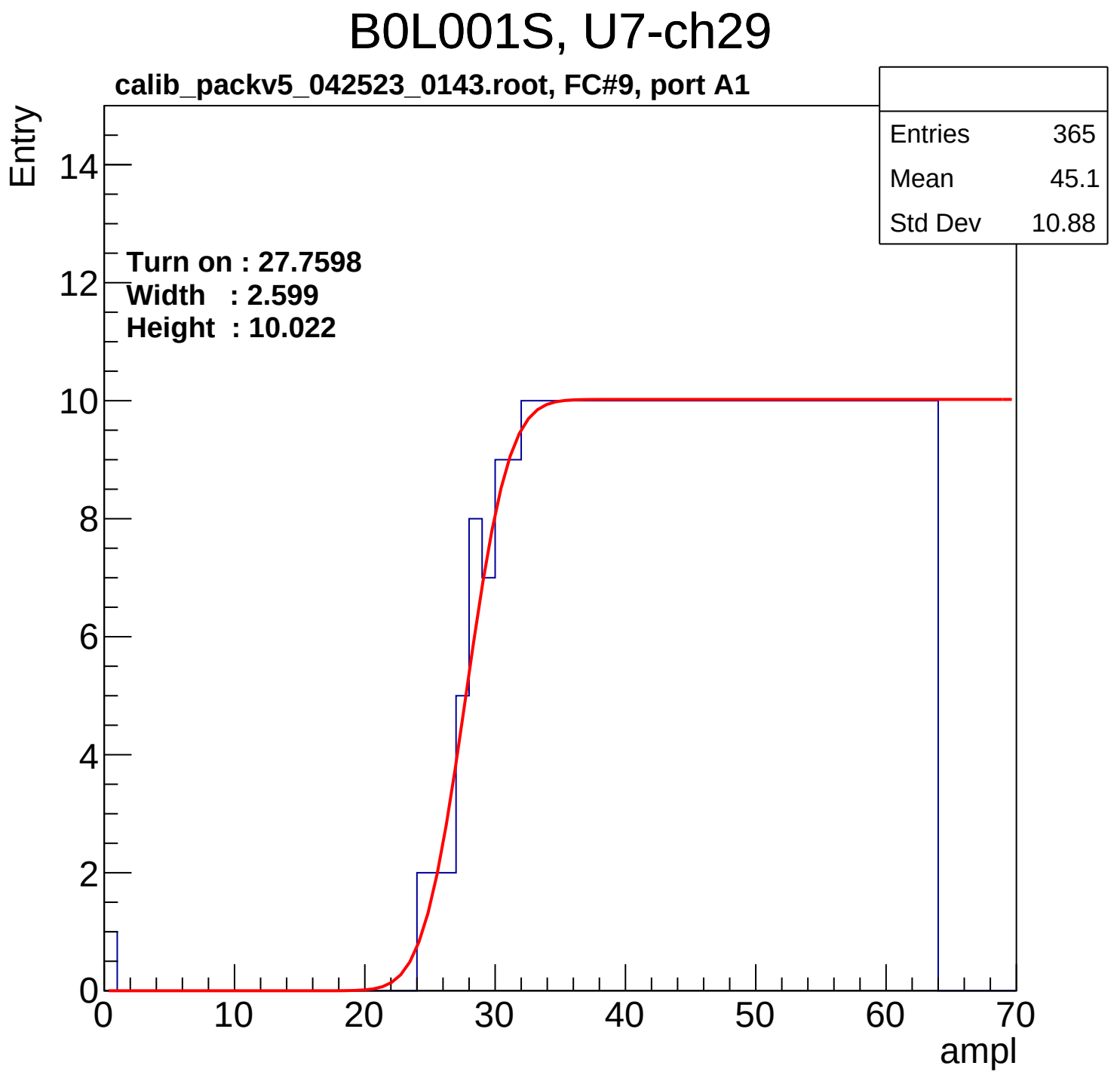
B0L001S, U7-ch29
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 45.1
Std Dev 10.88
Turn on : 27.7598
Width : 2.599
Height : 10.022
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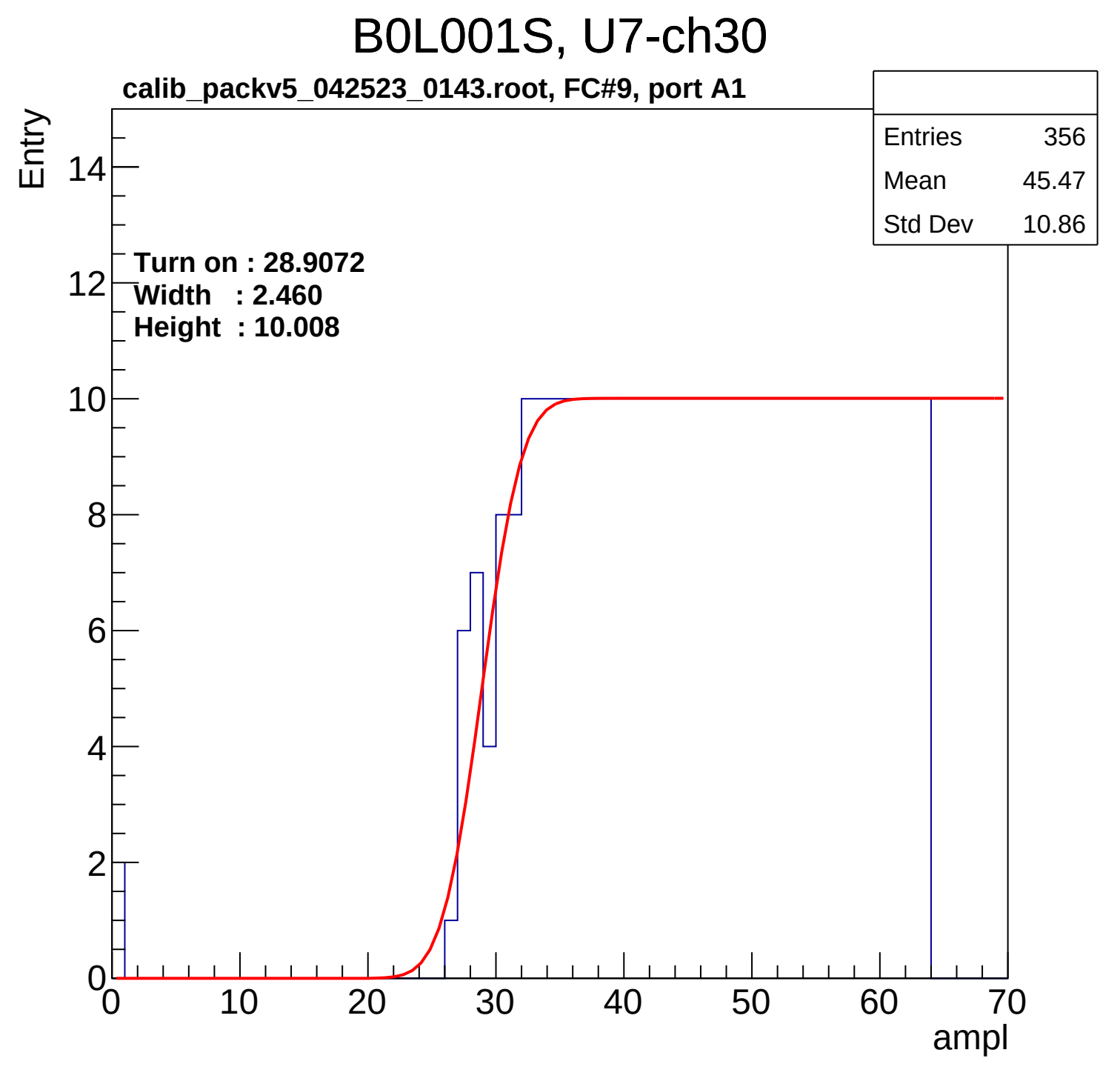
B0L001S, U7-ch30
calib_packv5_042523_0143.root, FC#9, port A1
Entries 356
Mean 45.47
Std Dev 10.86
Turn on : 28.9072
Width : 2.460
Height : 10.008
Entry
ampl
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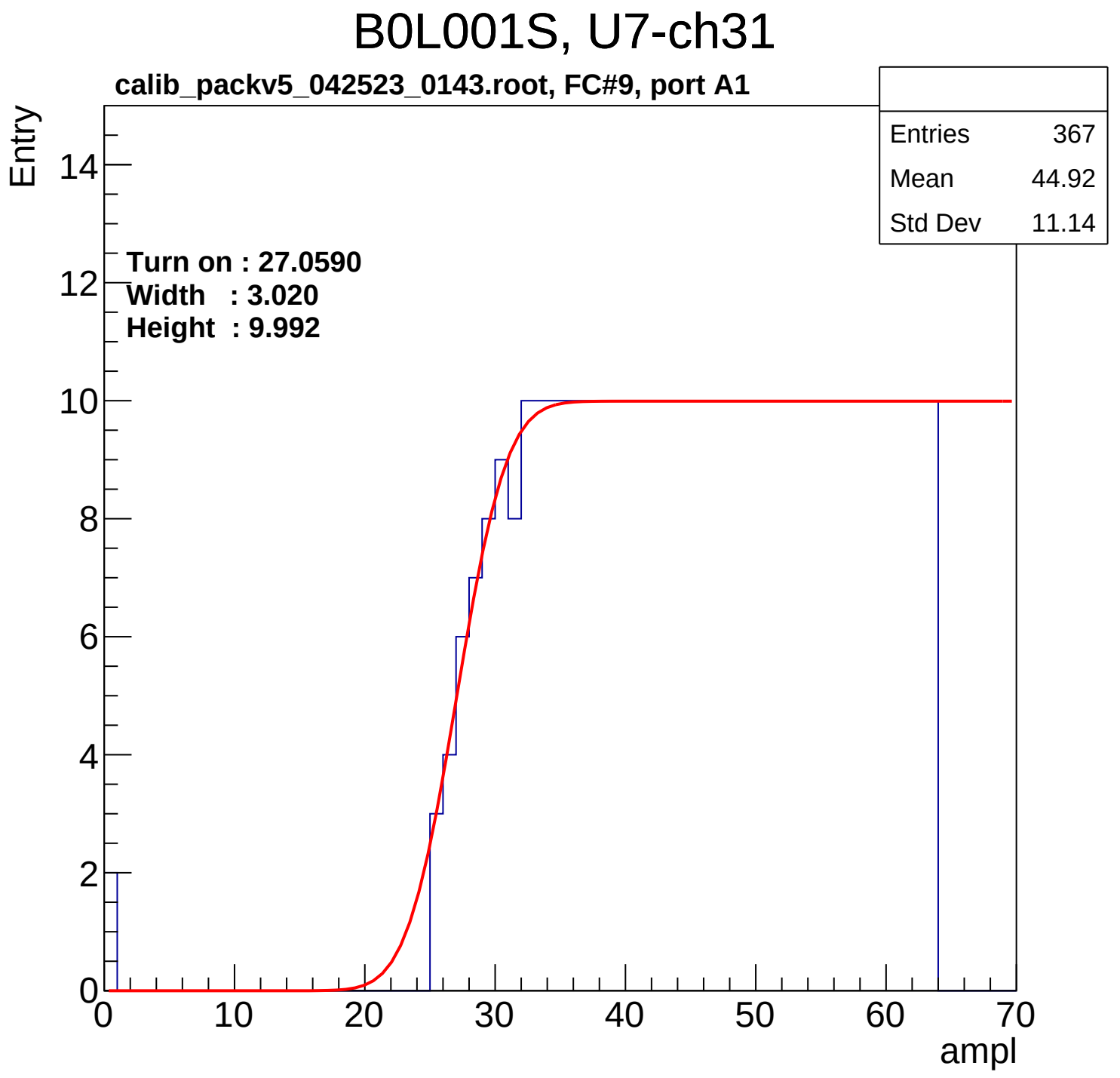
B0L001S, U7-ch31
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.92
Std Dev 11.14
Turn on : 27.0590
Width : 3.020
Height : 9.992
Entry
ampl
0
2
4
6
8
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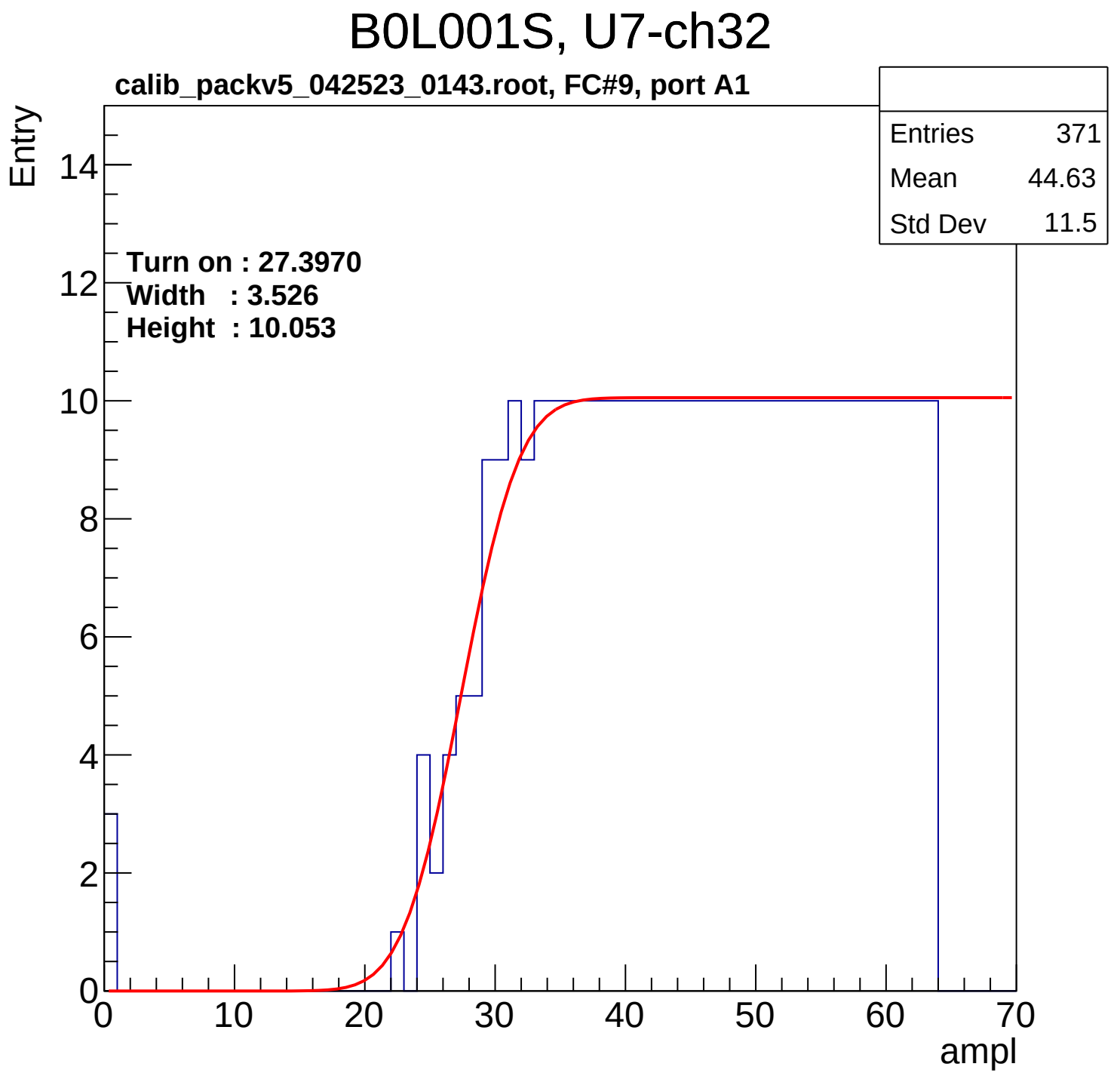
B0L001S, U7-ch32
calib_packv5_042523_0143.root, FC#9, port A1
Entries 371
Mean 44.63
Std Dev 11.5
Turn on : 27.3970
Width : 3.526
Height : 10.053
Entry
ampl
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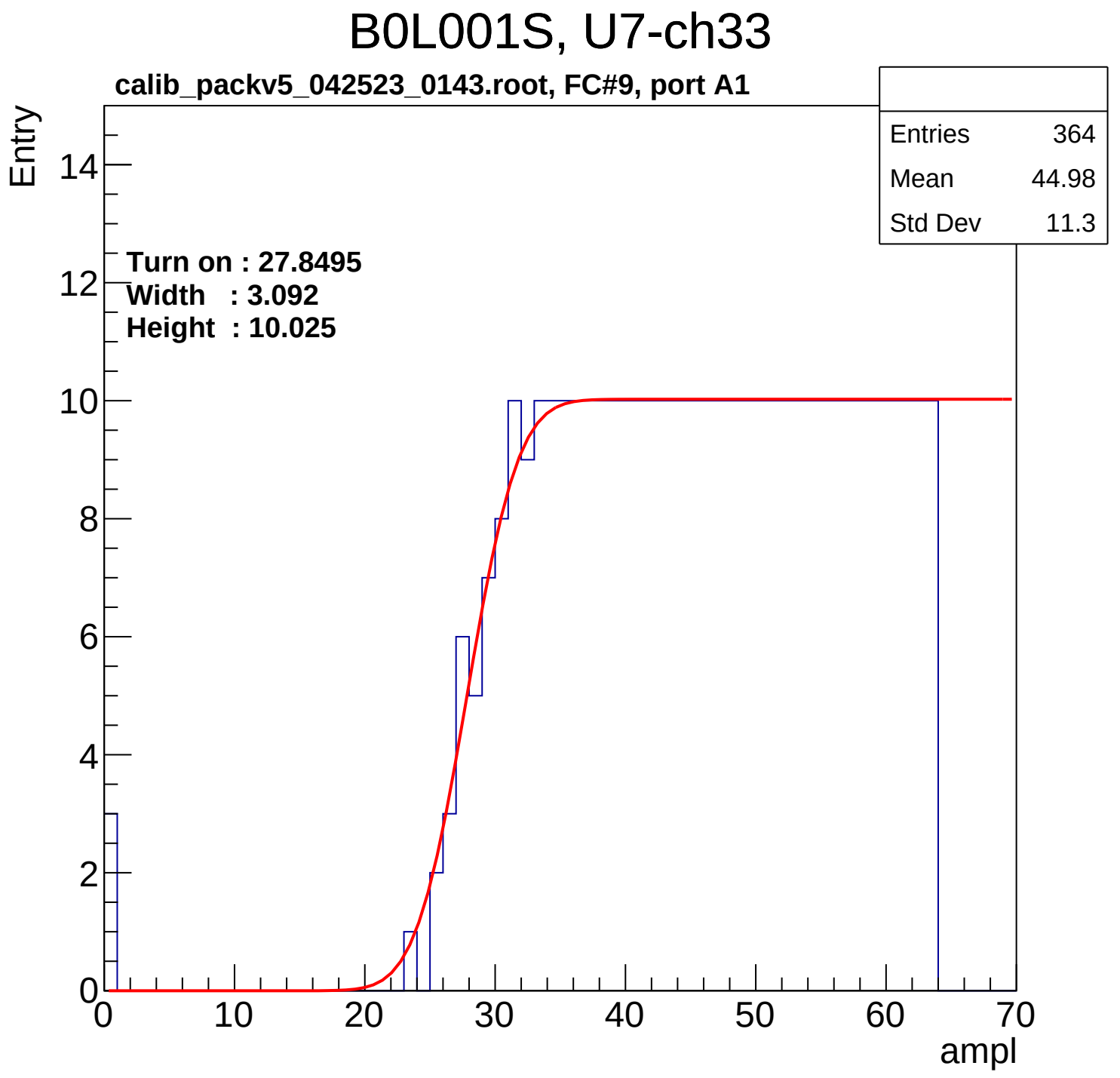
B0L001S, U7-ch33
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 44.98
Std Dev 11.3
Turn on : 27.8495
Width : 3.092
Height : 10.025
Entry
ampl
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2
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6
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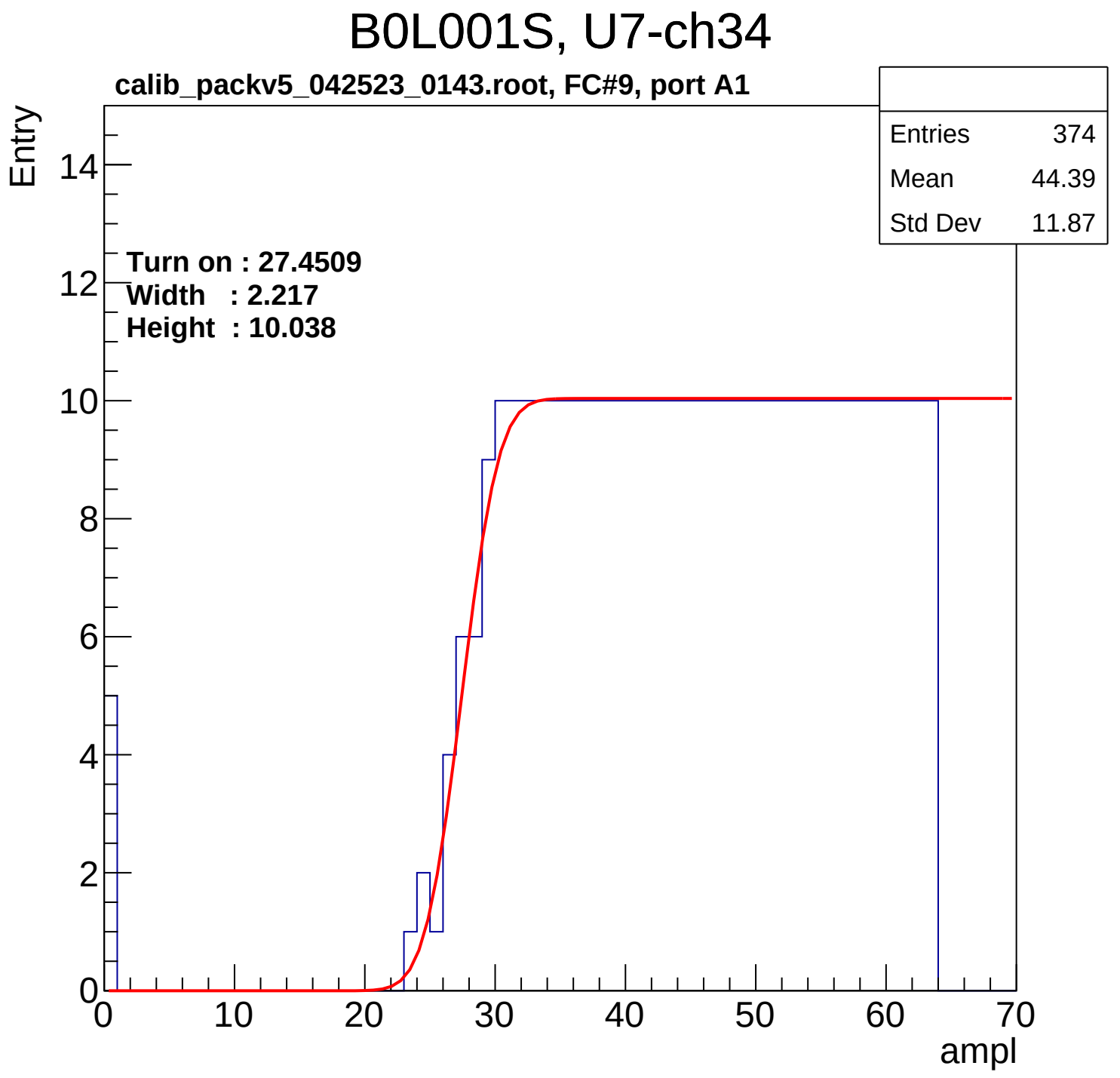
B0L001S, U7-ch34
calib_packv5_042523_0143.root, FC#9, port A1
Entries 374
Mean 44.39
Std Dev 11.87
Turn on : 27.4509
Width : 2.217
Height : 10.038
Entry
ampl
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2
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6
8
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0
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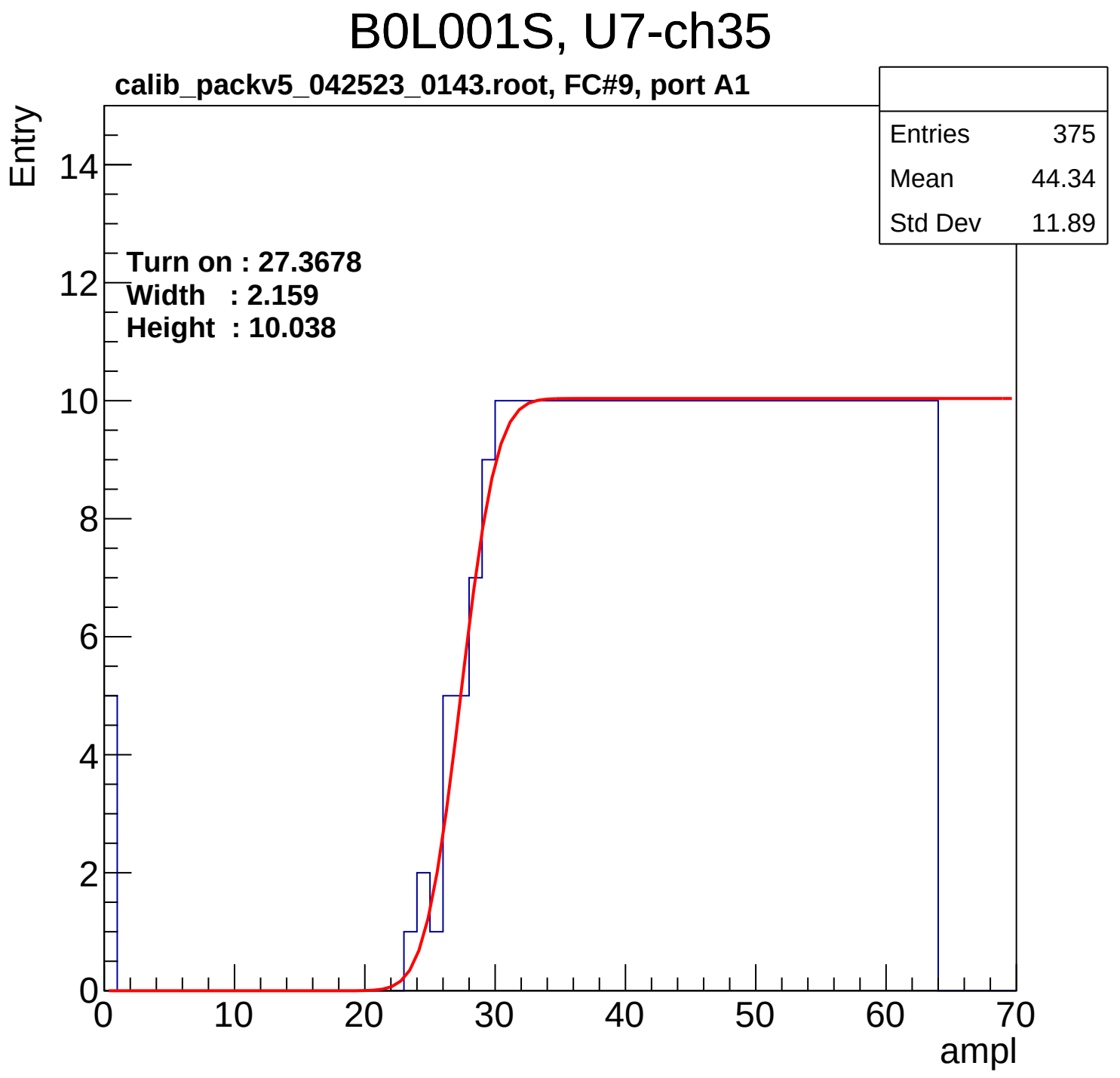
B0L001S, U7-ch35
calib_packv5_042523_0143.root, FC#9, port A1
Entries 375
Mean 44.34
Std Dev 11.89
Turn on : 27.3678
Width : 2.159
Height : 10.038
Entry
ampl
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2
4
6
8
10
12
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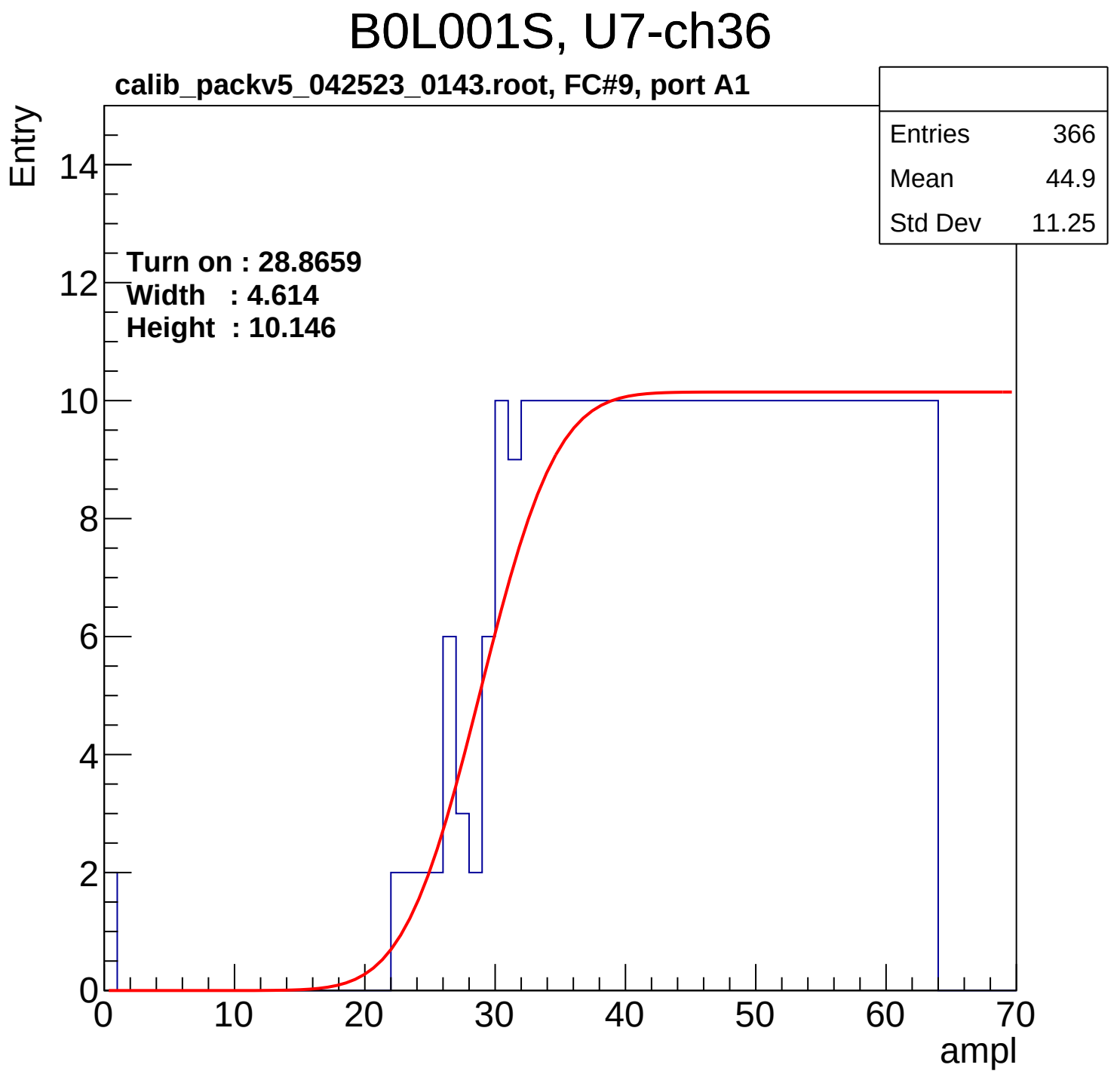
B0L001S, U7-ch36
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.9
Std Dev 11.25
Turn on : 28.8659
Width : 4.614
Height : 10.146
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
50
60
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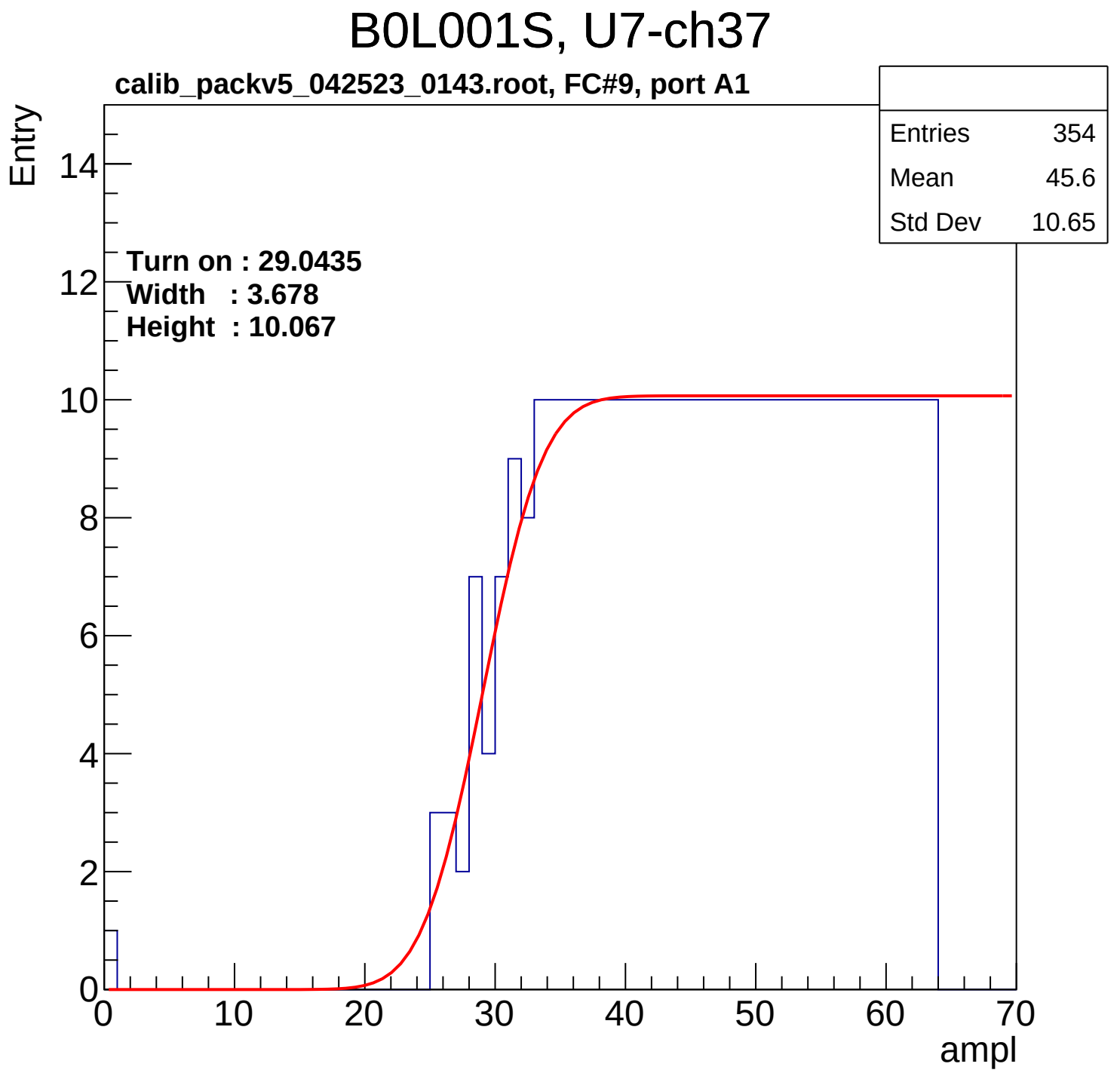
B0L001S, U7-ch37
calib_packv5_042523_0143.root, FC#9, port A1
Entries 354
Mean 45.6
Std Dev 10.65
Turn on : 29.0435
Width : 3.678
Height : 10.067
Entry
ampl
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6
8
10
12
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0
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60
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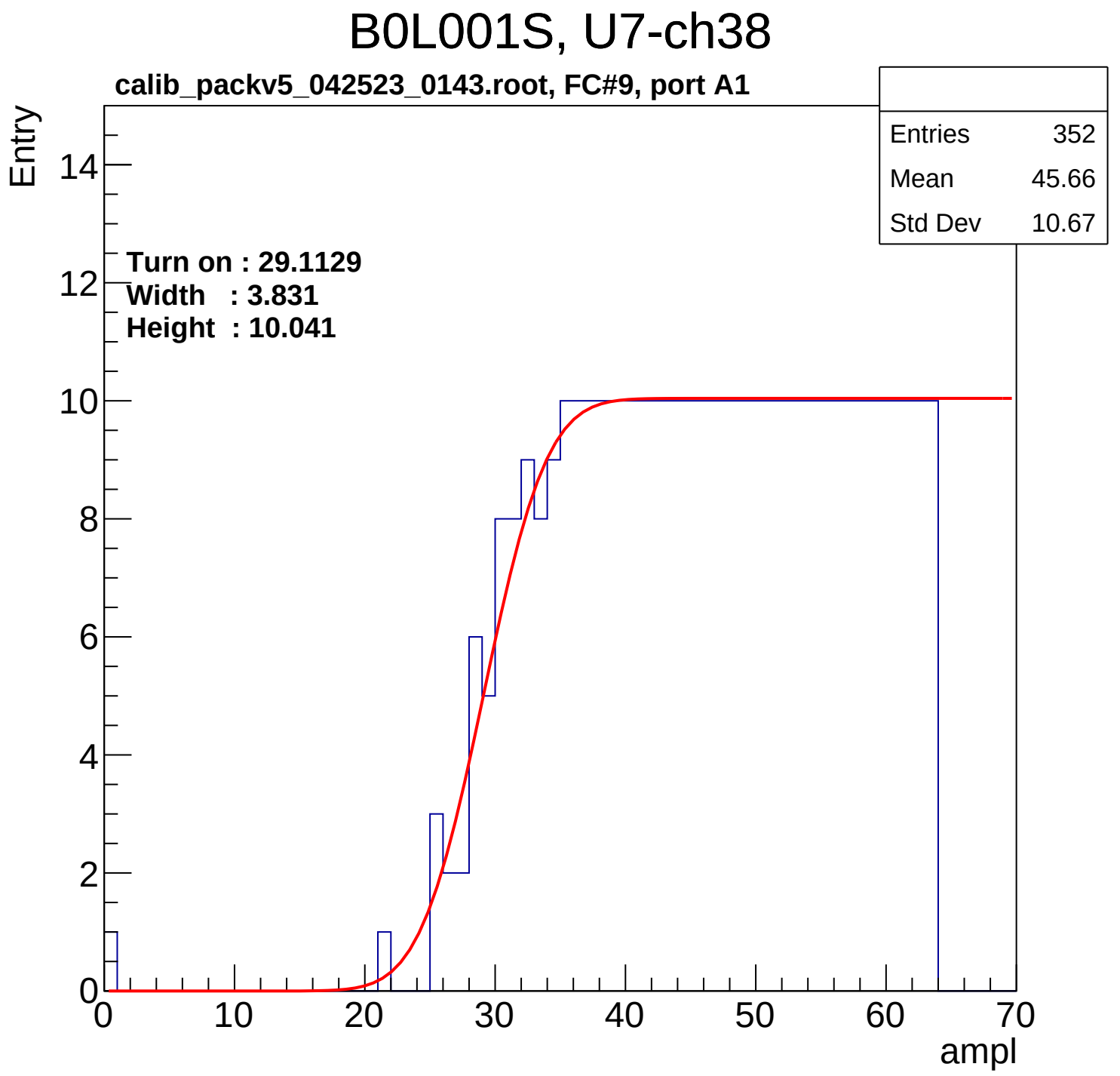
B0L001S, U7-ch38
calib_packv5_042523_0143.root, FC#9, port A1
Entries 352
Mean 45.66
Std Dev 10.67
Turn on : 29.1129
Width : 3.831
Height : 10.041
Entry
ampl
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4
6
8
10
12
14
0
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20
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40
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60
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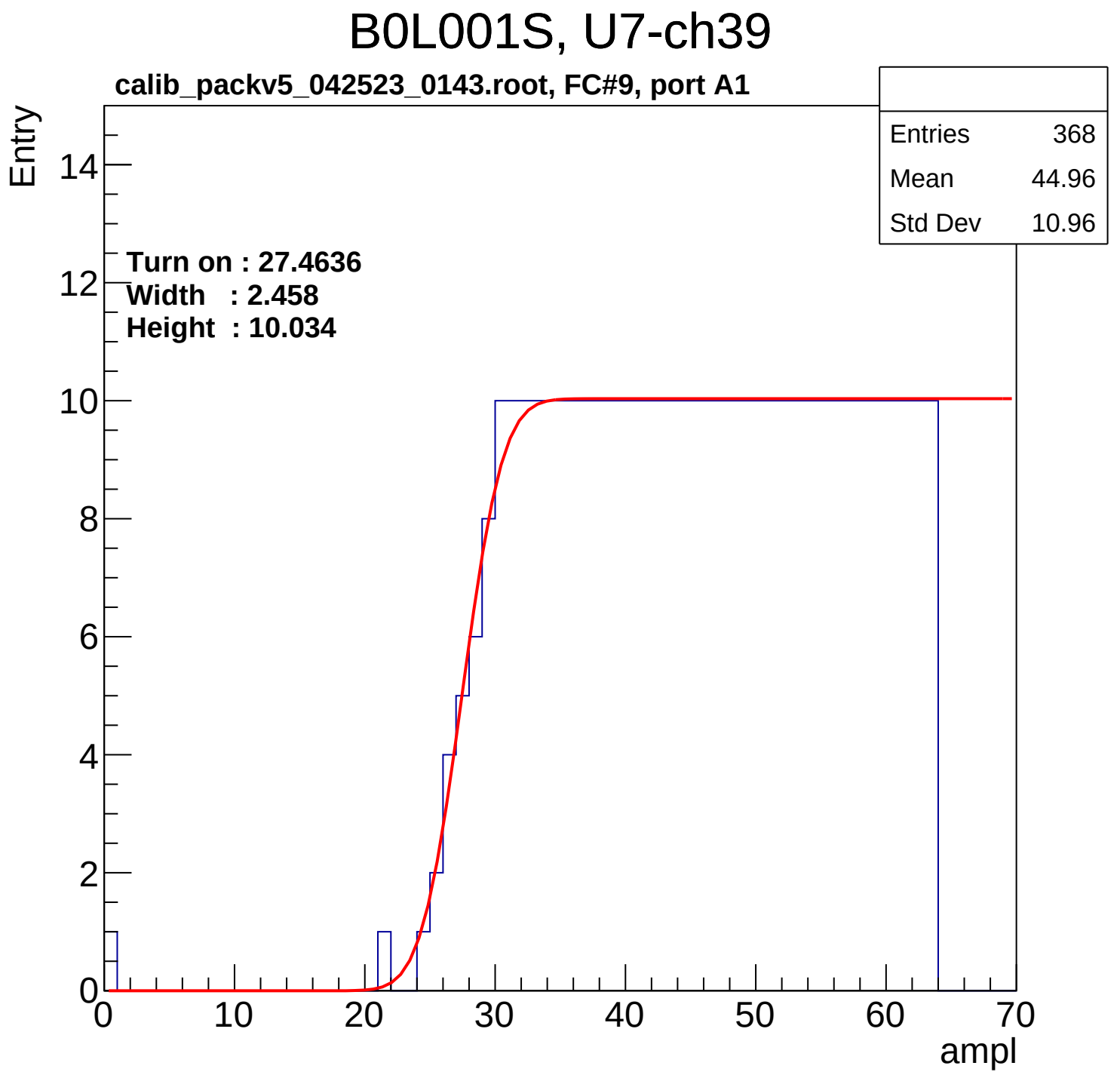
B0L001S, U7-ch39
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.96
Std Dev 10.96
Turn on : 27.4636
Width : 2.458
Height : 10.034
Entry
ampl
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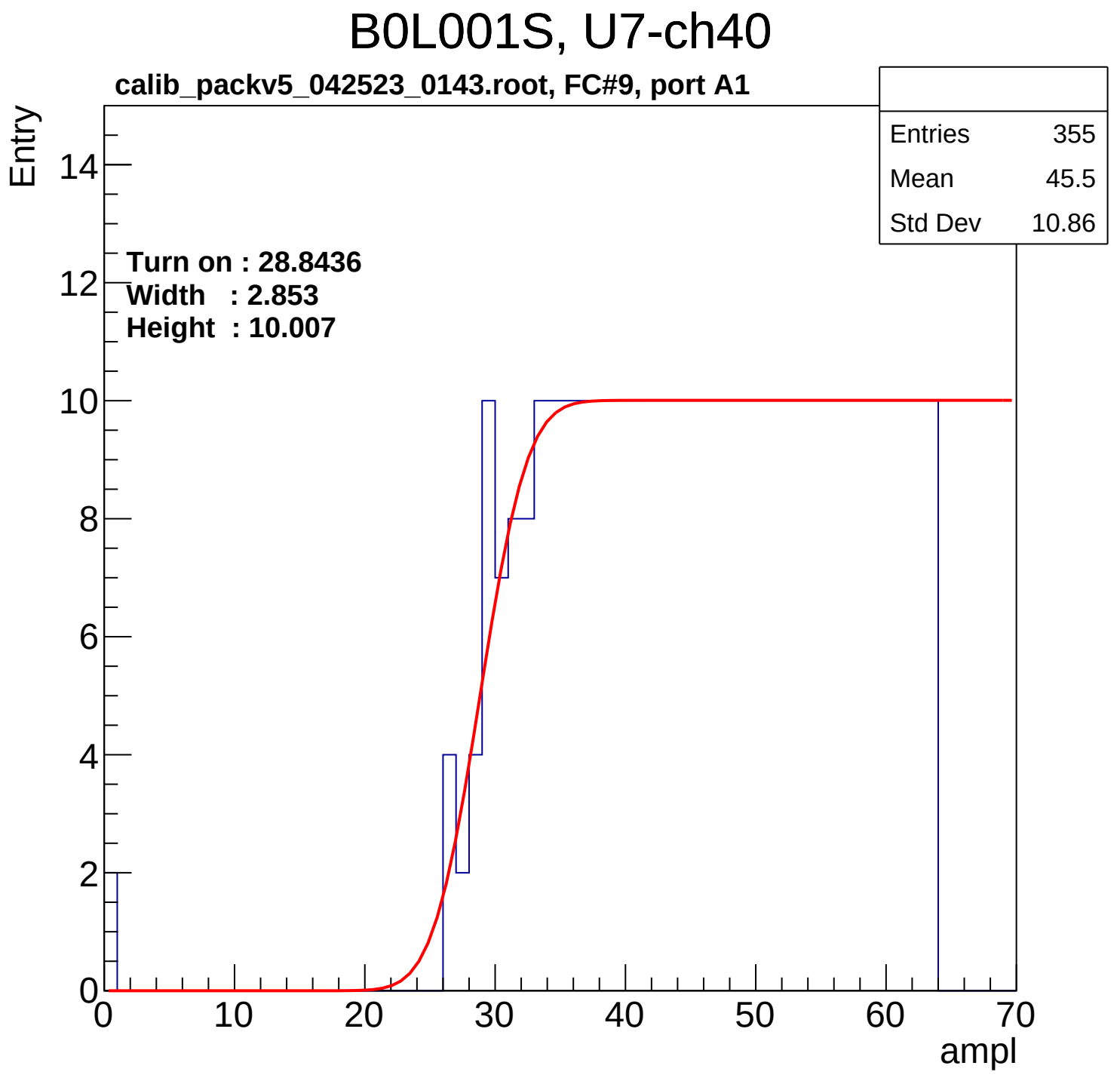
B0L001S, U7-ch40
calib_packv5_042523_0143.root, FC#9, port A1
Entries 355
Mean 45.5
Std Dev 10.86
Turn on : 28.8436
Width : 2.853
Height : 10.007
Entry
ampl
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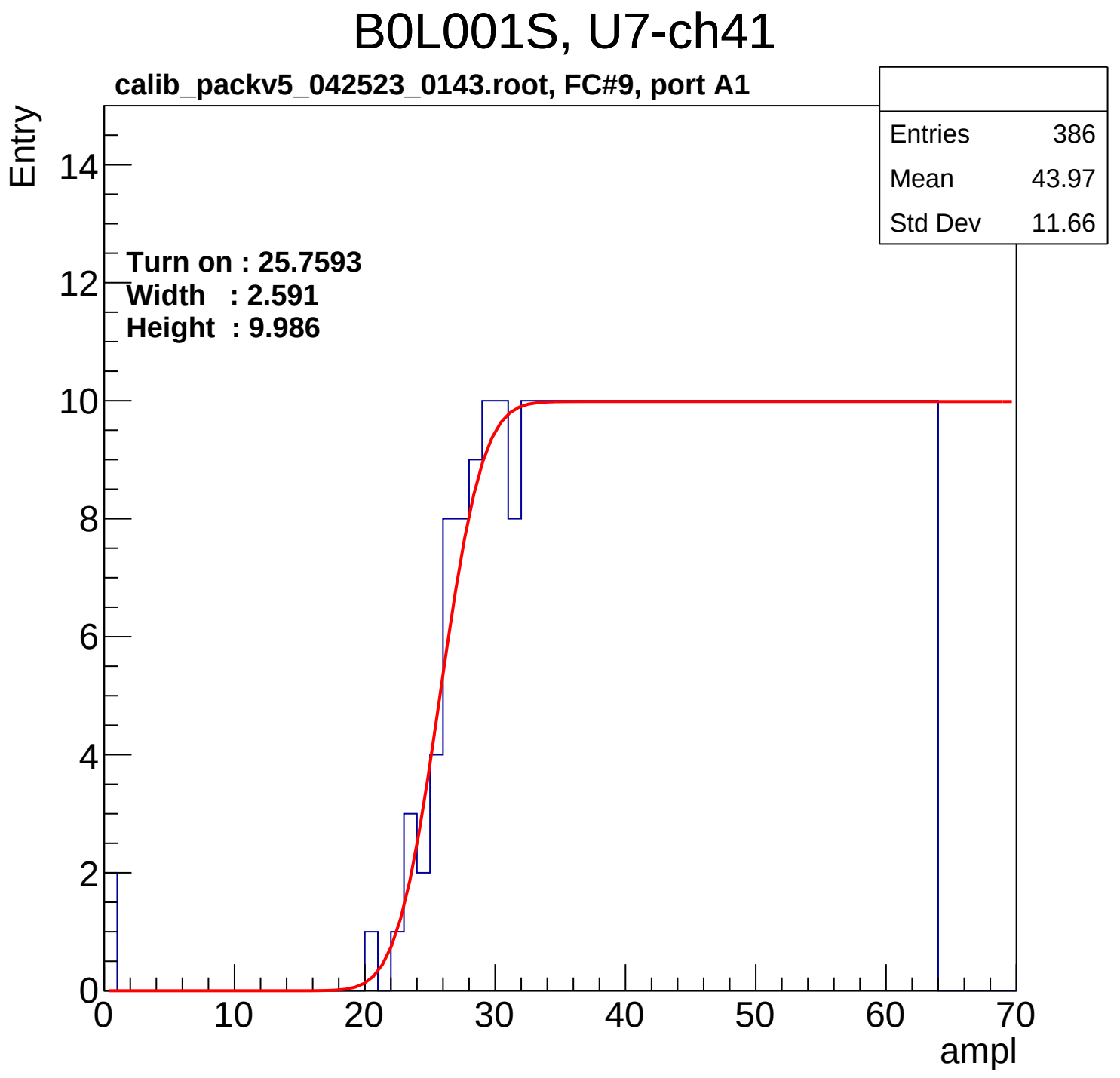
B0L001S, U7-ch41
calib_packv5_042523_0143.root, FC#9, port A1
Entries 386
Mean 43.97
Std Dev 11.66
Turn on : 25.7593
Width : 2.591
Height : 9.986
Entry
ampl
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6
8
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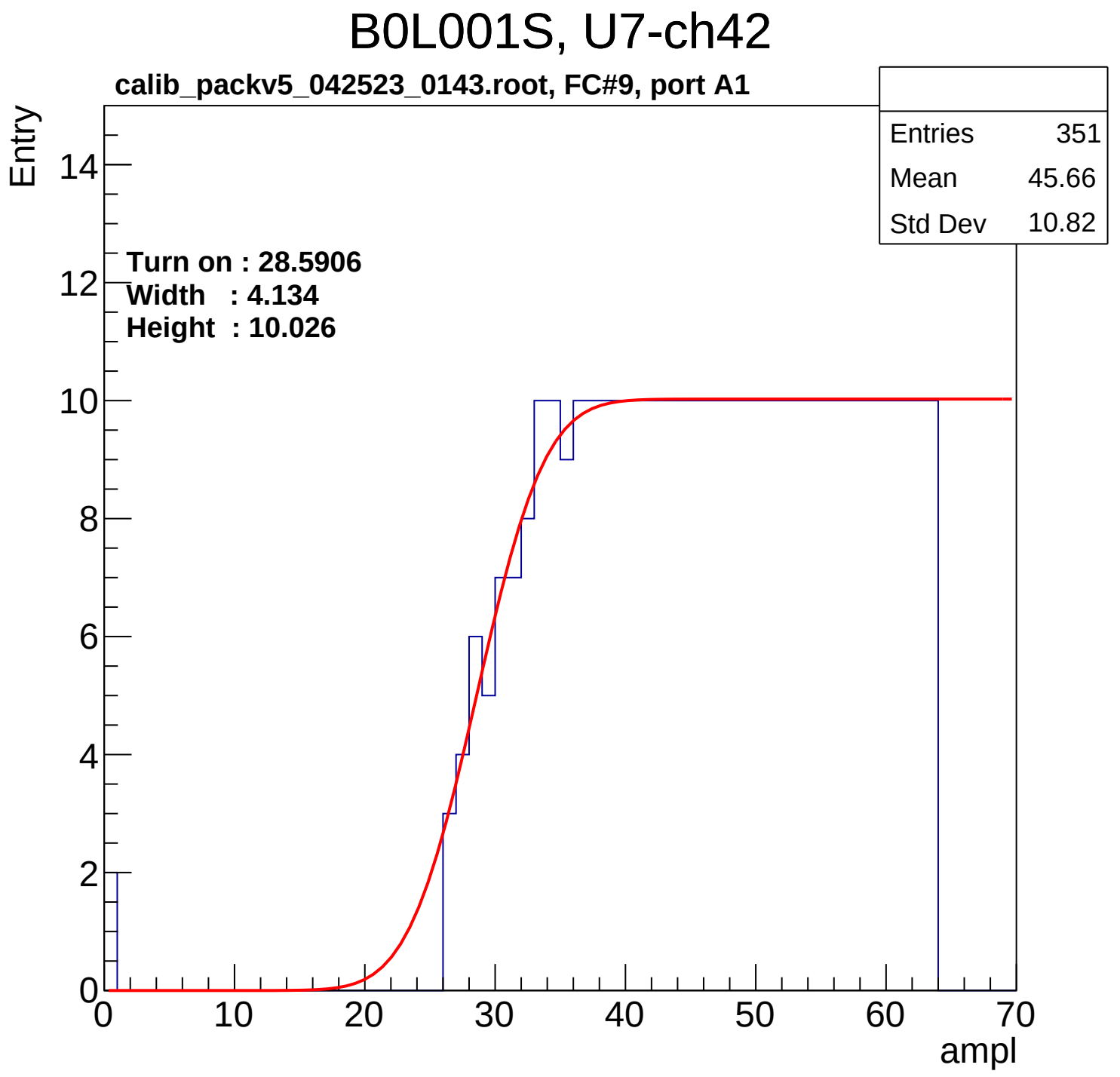
B0L001S, U7-ch42
calib_packv5_042523_0143.root, FC#9, port A1
Entries 351
Mean 45.66
Std Dev 10.82
Turn on : 28.5906
Width : 4.134
Height : 10.026
Entry
ampl
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6
8
10
12
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0
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20
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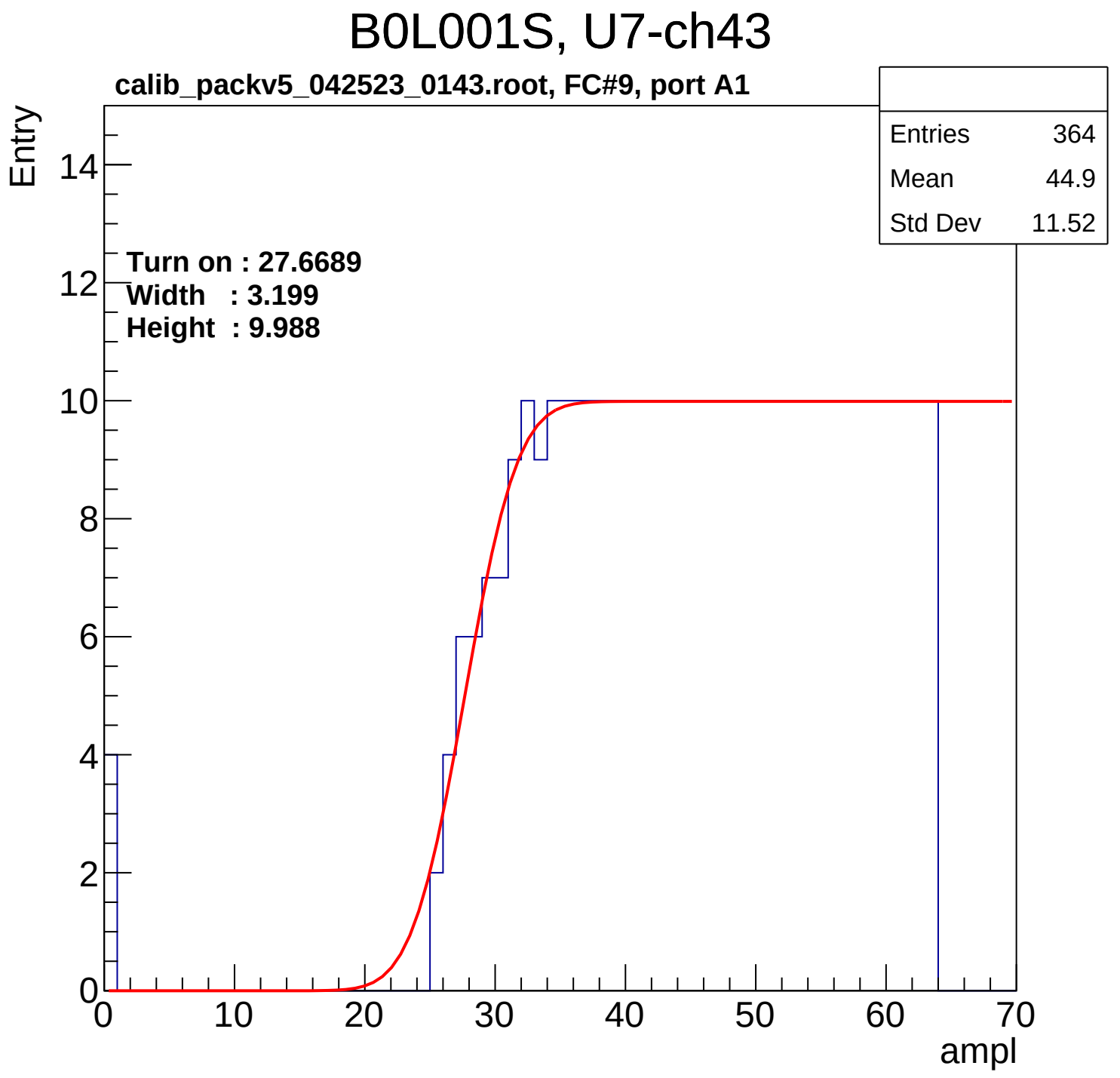
B0L001S, U7-ch43
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 44.9
Std Dev 11.52
Turn on : 27.6689
Width : 3.199
Height : 9.988
Entry
ampl
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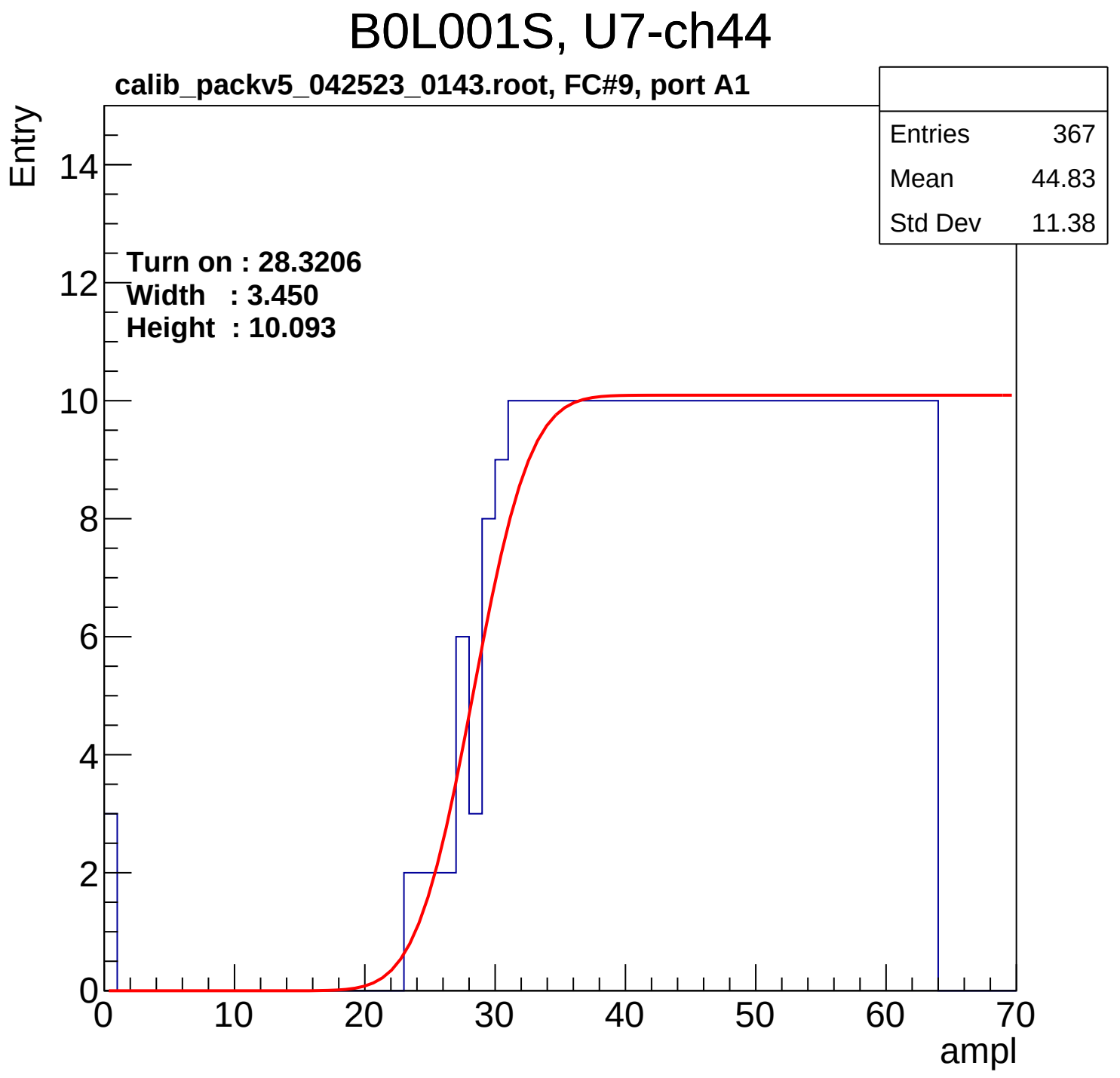
B0L001S, U7-ch44
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.83
Std Dev 11.38
Turn on : 28.3206
Width : 3.450
Height : 10.093
Entry
ampl
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2
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6
8
10
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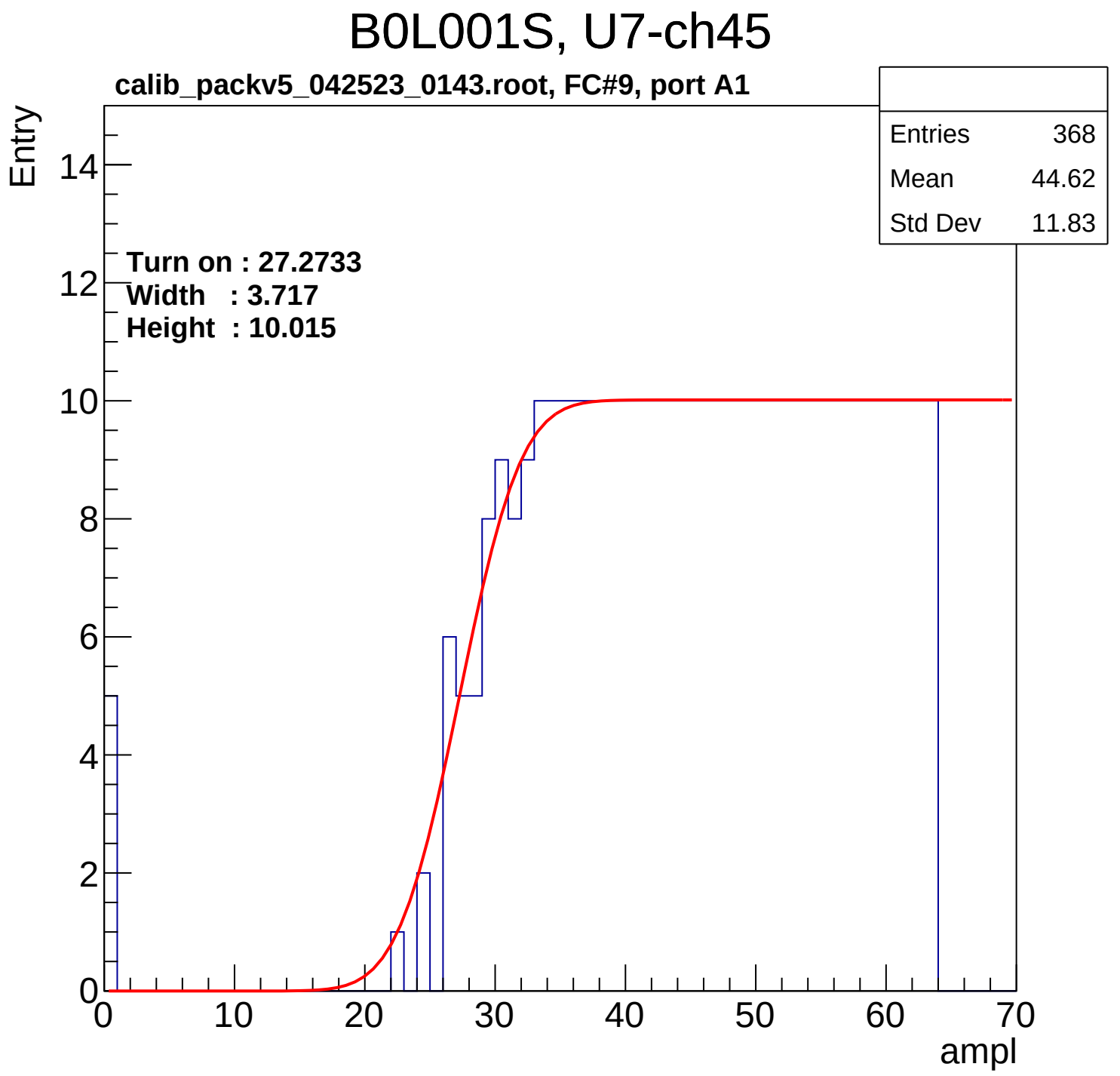
B0L001S, U7-ch45
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.62
Std Dev 11.83
Turn on : 27.2733
Width : 3.717
Height : 10.015
Entry
ampl
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8
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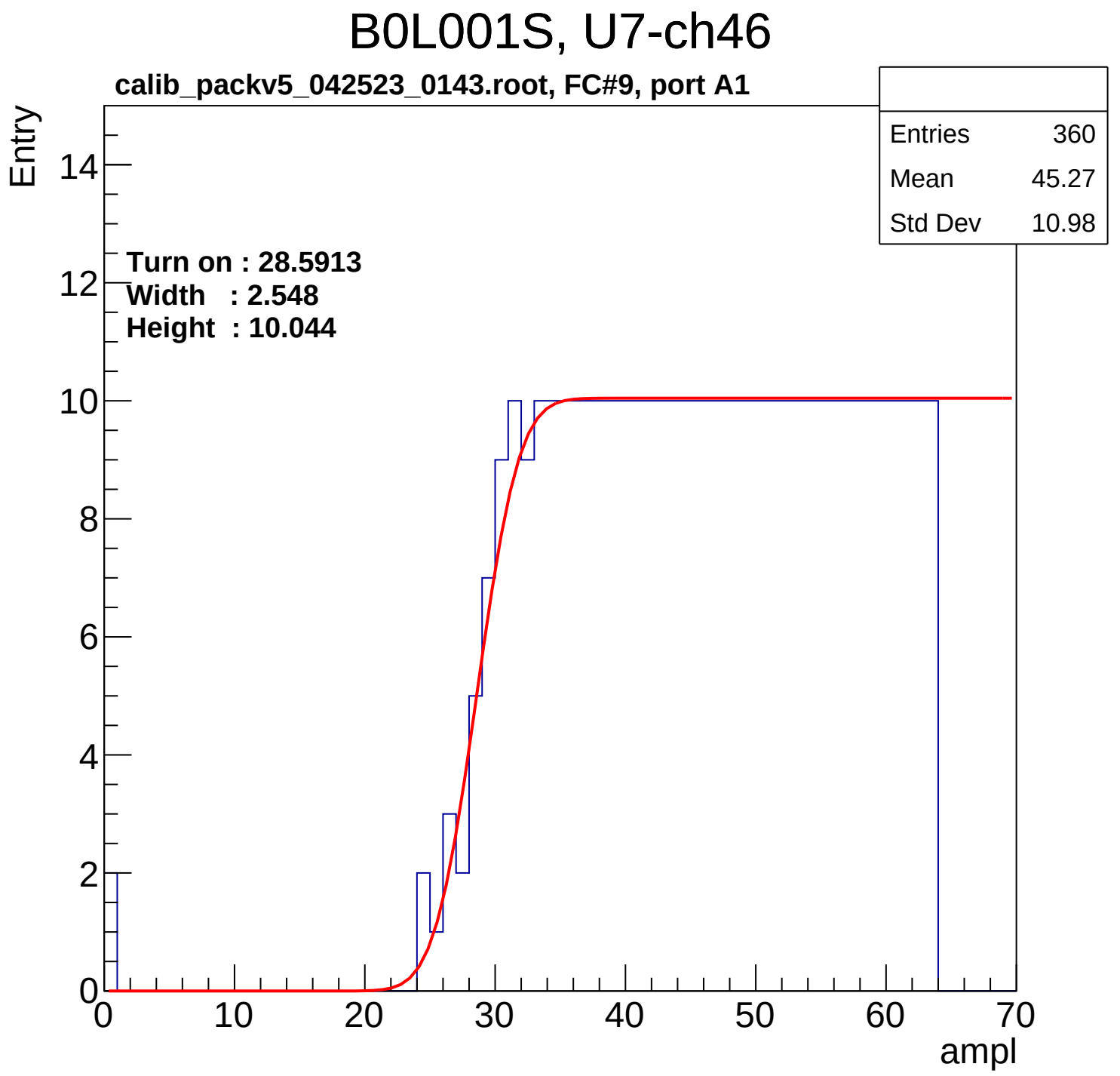
B0L001S, U7-ch46
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 45.27
Std Dev 10.98
Turn on : 28.5913
Width : 2.548
Height : 10.044
Entry
ampl
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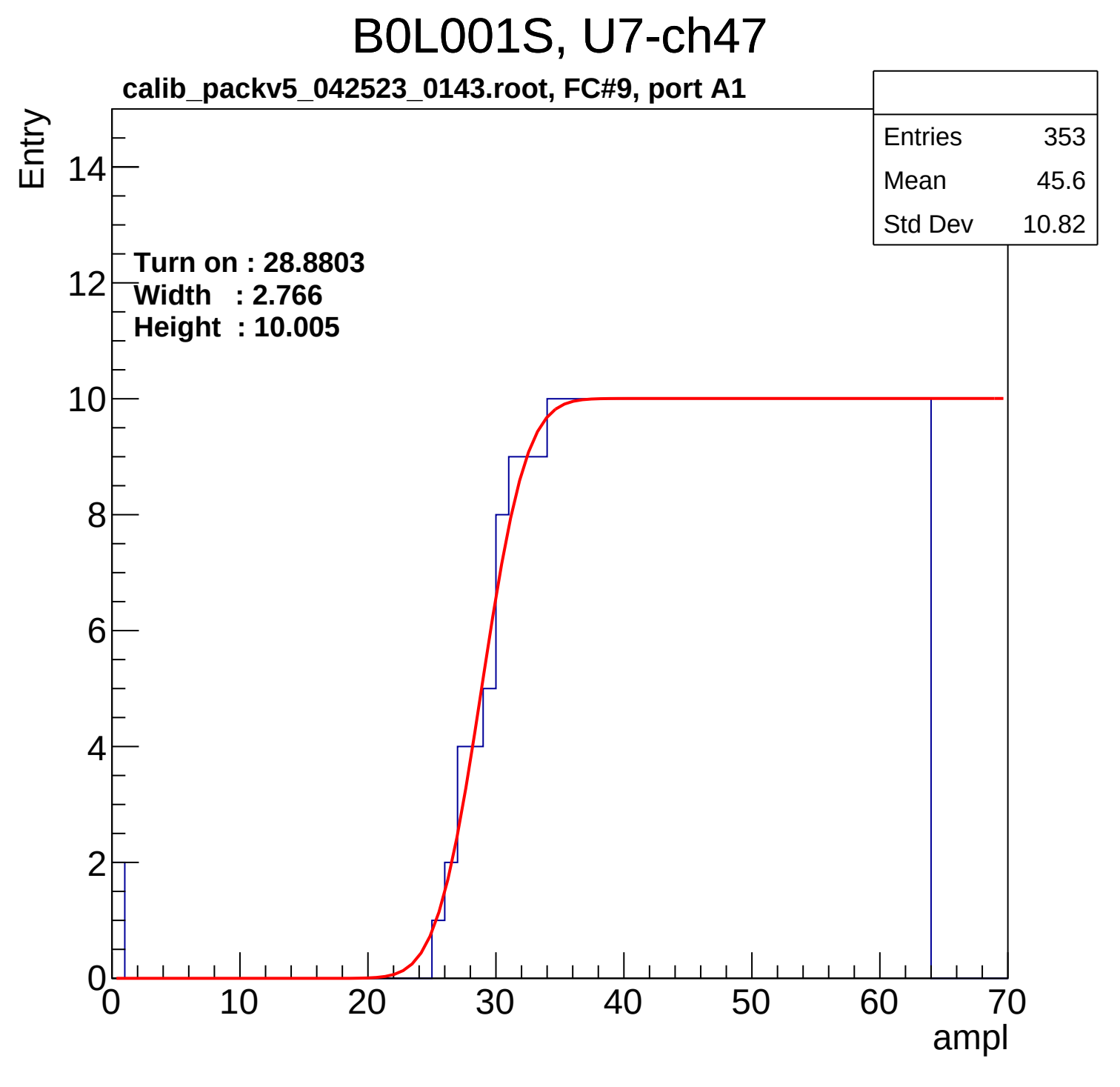
B0L001S, U7-ch47
calib_packv5_042523_0143.root, FC#9, port A1
Entries 353
Mean 45.6
Std Dev 10.82
Turn on : 28.8803
Width : 2.766
Height : 10.005
Entry
ampl
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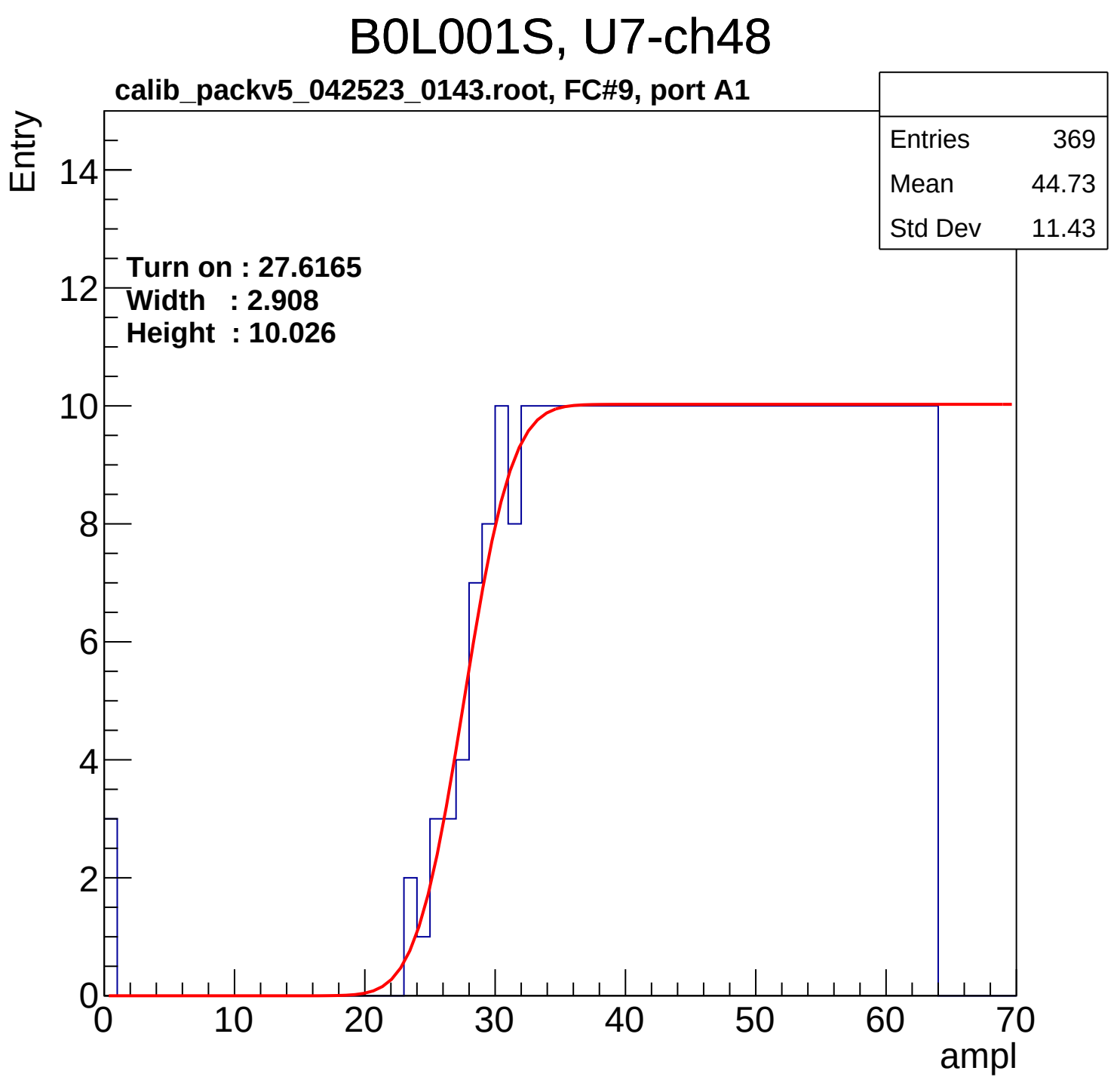
B0L001S, U7-ch48
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.73
Std Dev 11.43
Turn on : 27.6165
Width : 2.908
Height : 10.026
Entry
ampl
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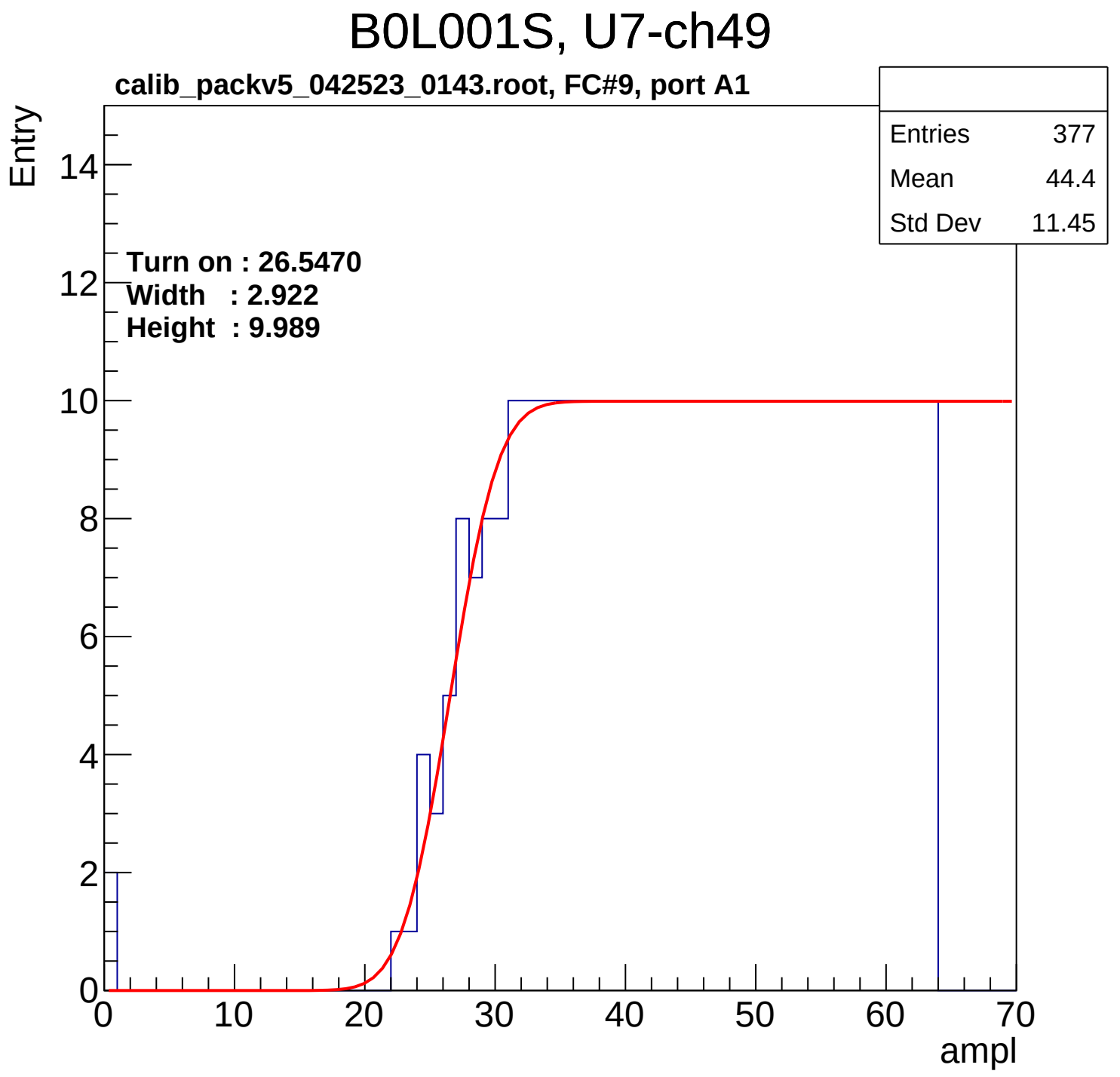
B0L001S, U7-ch49
calib_packv5_042523_0143.root, FC#9, port A1
Entries 377
Mean 44.4
Std Dev 11.45
Turn on : 26.5470
Width : 2.922
Height : 9.989
Entry
ampl
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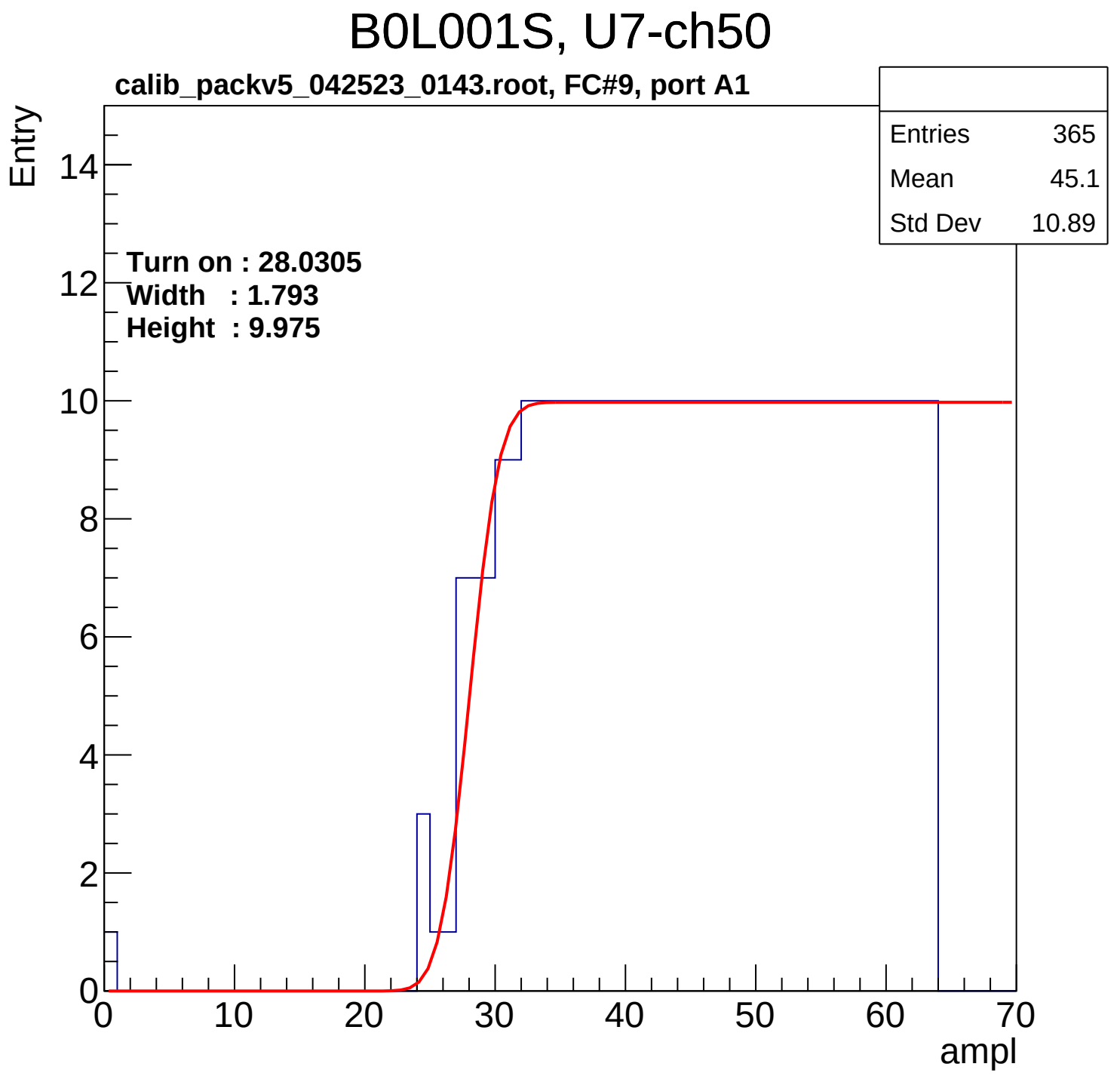
B0L001S, U7-ch50
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 45.1
Std Dev 10.89
Turn on : 28.0305
Width : 1.793
Height : 9.975
Entry
ampl
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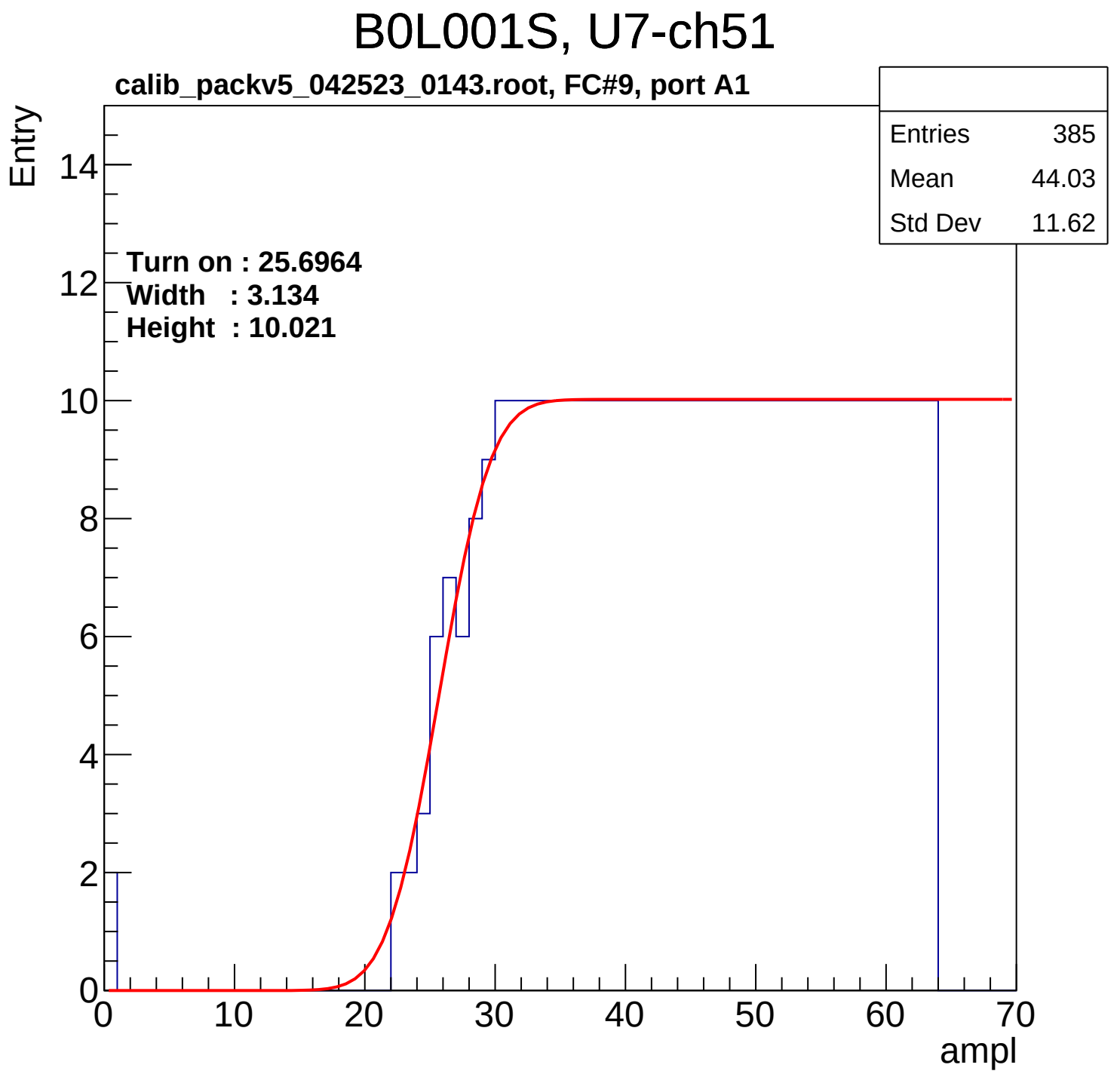
B0L001S, U7-ch51
calib_packv5_042523_0143.root, FC#9, port A1
Entries 385
Mean 44.03
Std Dev 11.62
Turn on : 25.6964
Width : 3.134
Height : 10.021
Entry
ampl
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8
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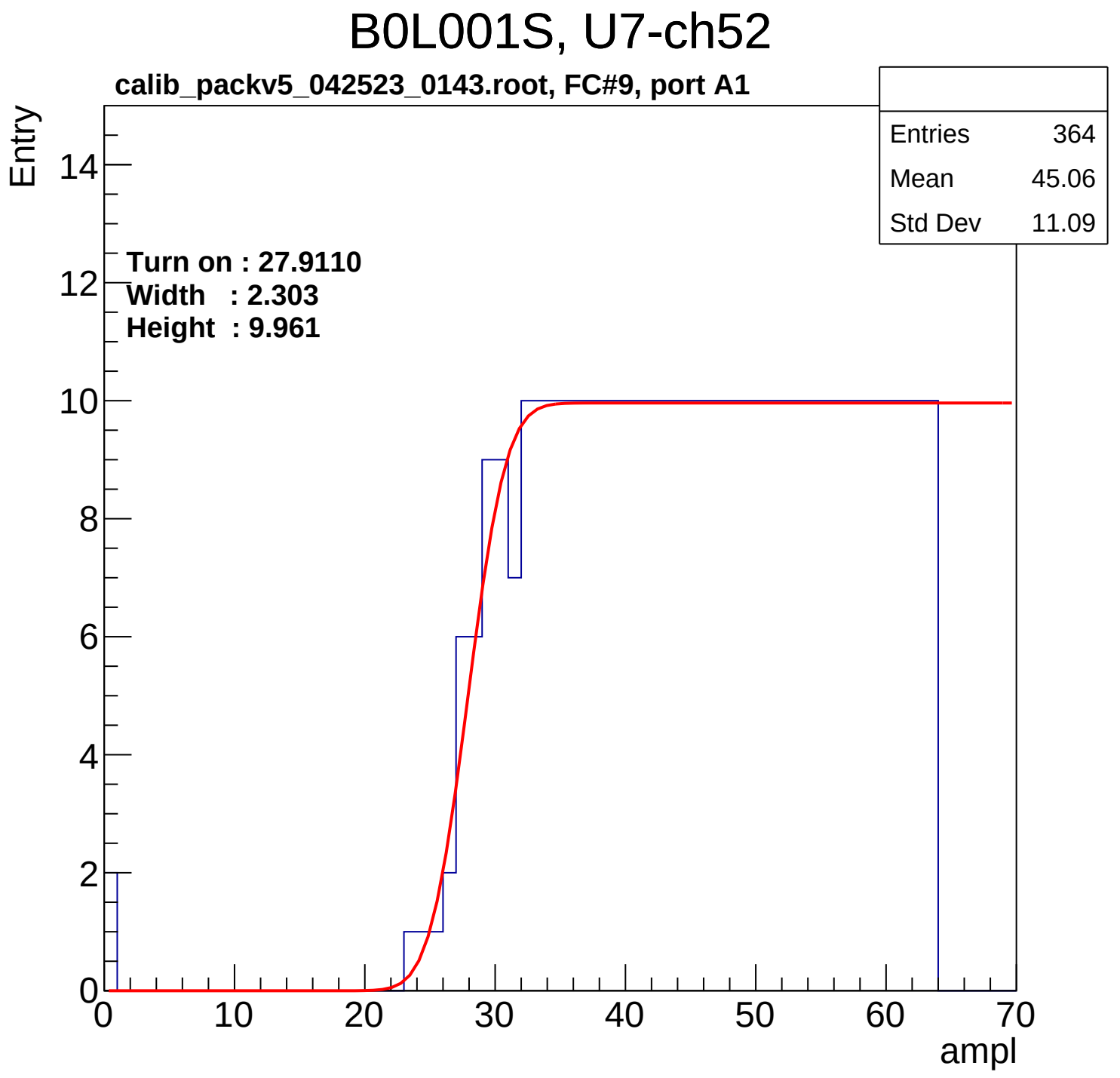
B0L001S, U7-ch52
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 45.06
Std Dev 11.09
Turn on : 27.9110
Width : 2.303
Height : 9.961
Entry
ampl
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6
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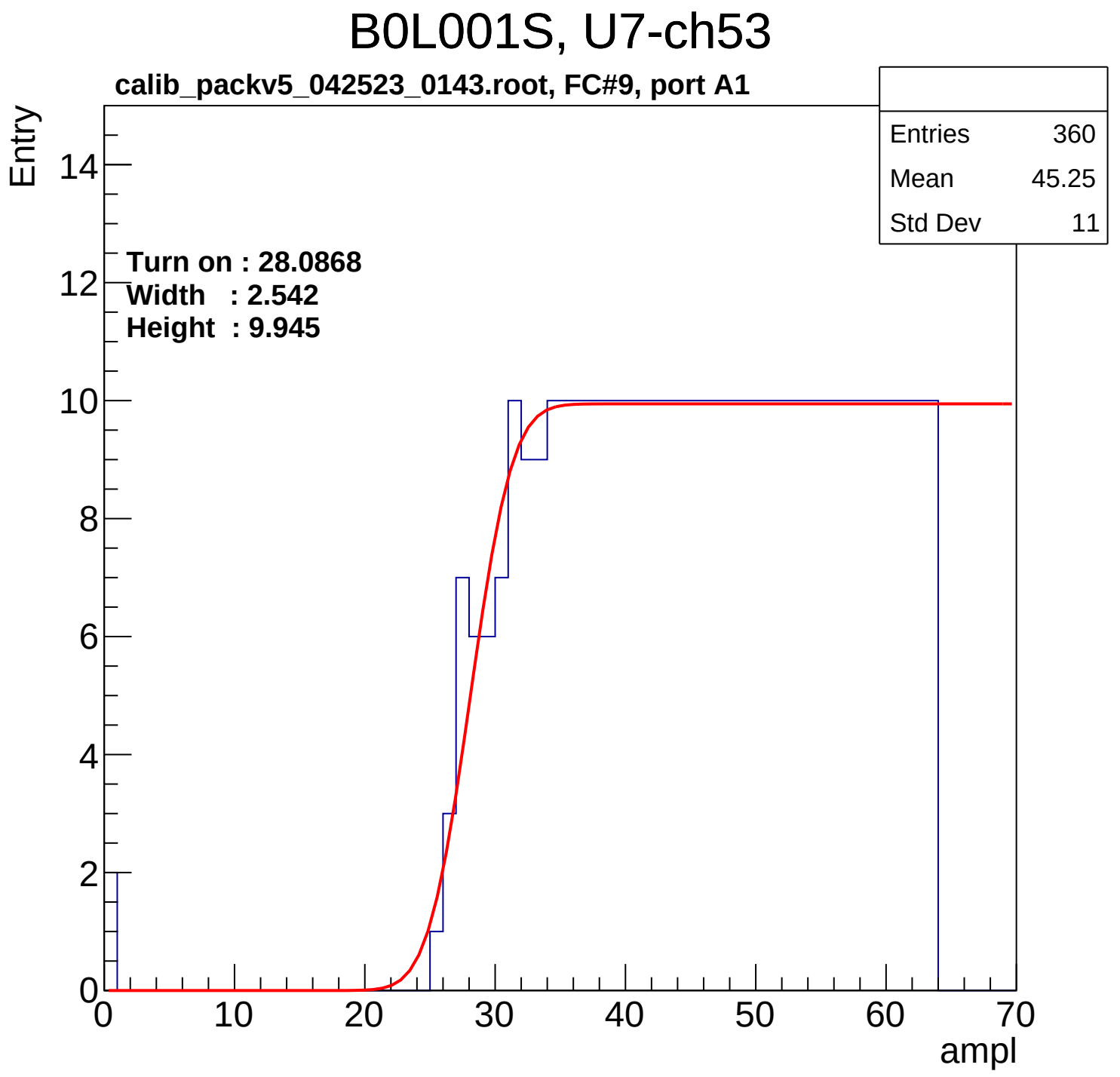
B0L001S, U7-ch53
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 45.25
Std Dev 11
Turn on : 28.0868
Width : 2.542
Height : 9.945
Entry
ampl
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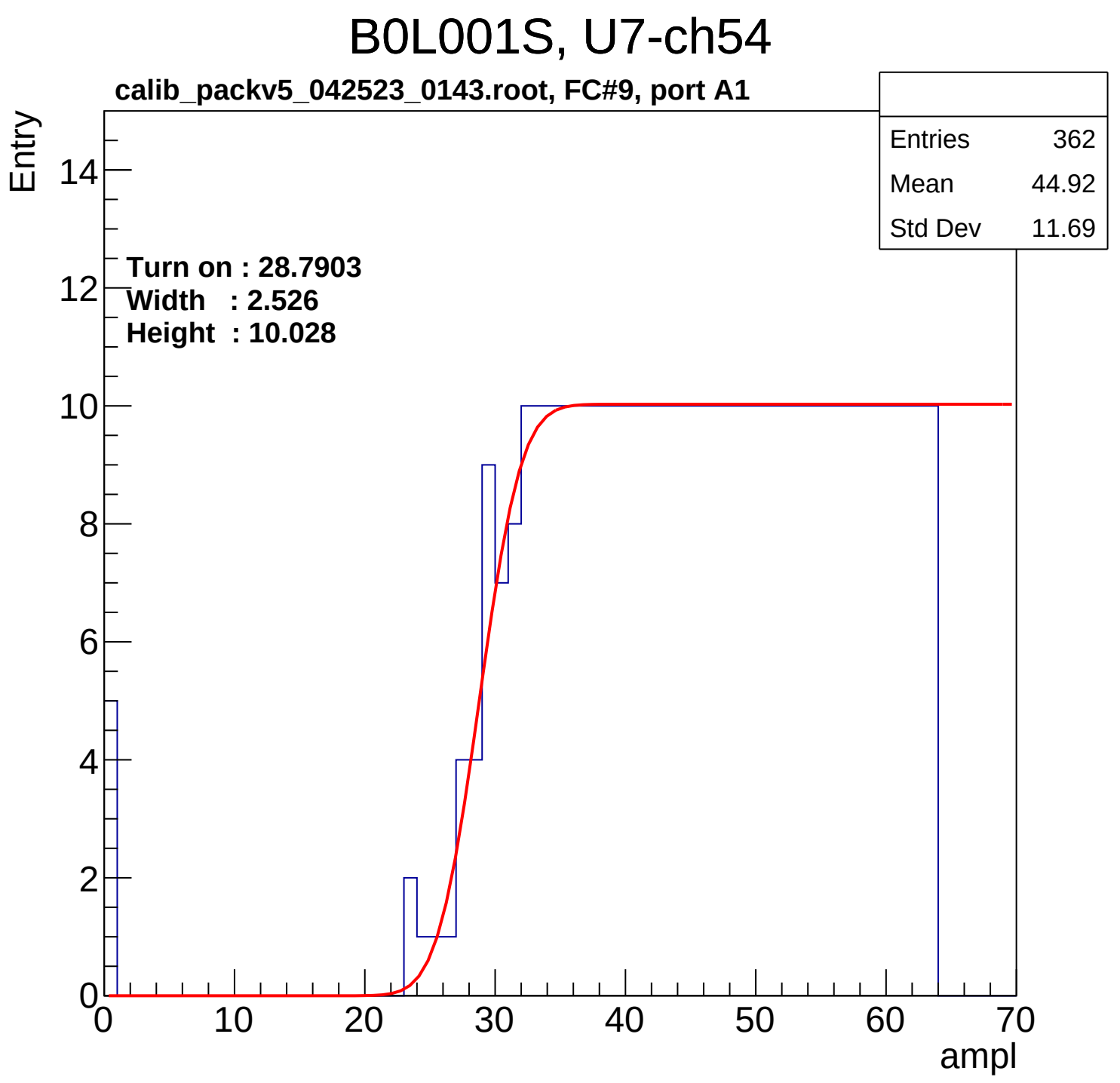
B0L001S, U7-ch54
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 44.92
Std Dev 11.69
Turn on : 28.7903
Width : 2.526
Height : 10.028
Entry
ampl
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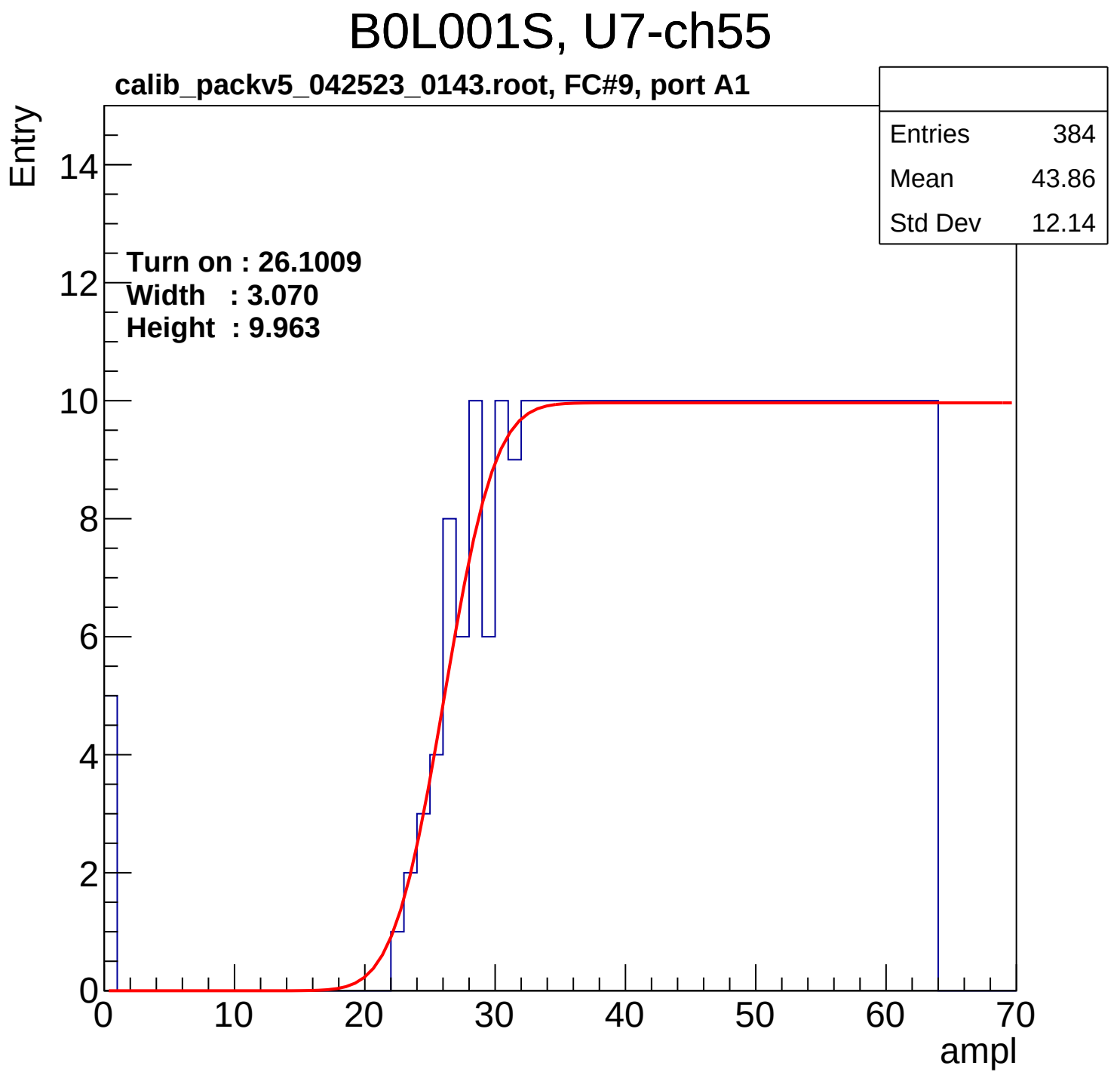
B0L001S, U7-ch55
calib_packv5_042523_0143.root, FC#9, port A1
Entries 384
Mean 43.86
Std Dev 12.14
Turn on : 26.1009
Width : 3.070
Height : 9.963
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ampl
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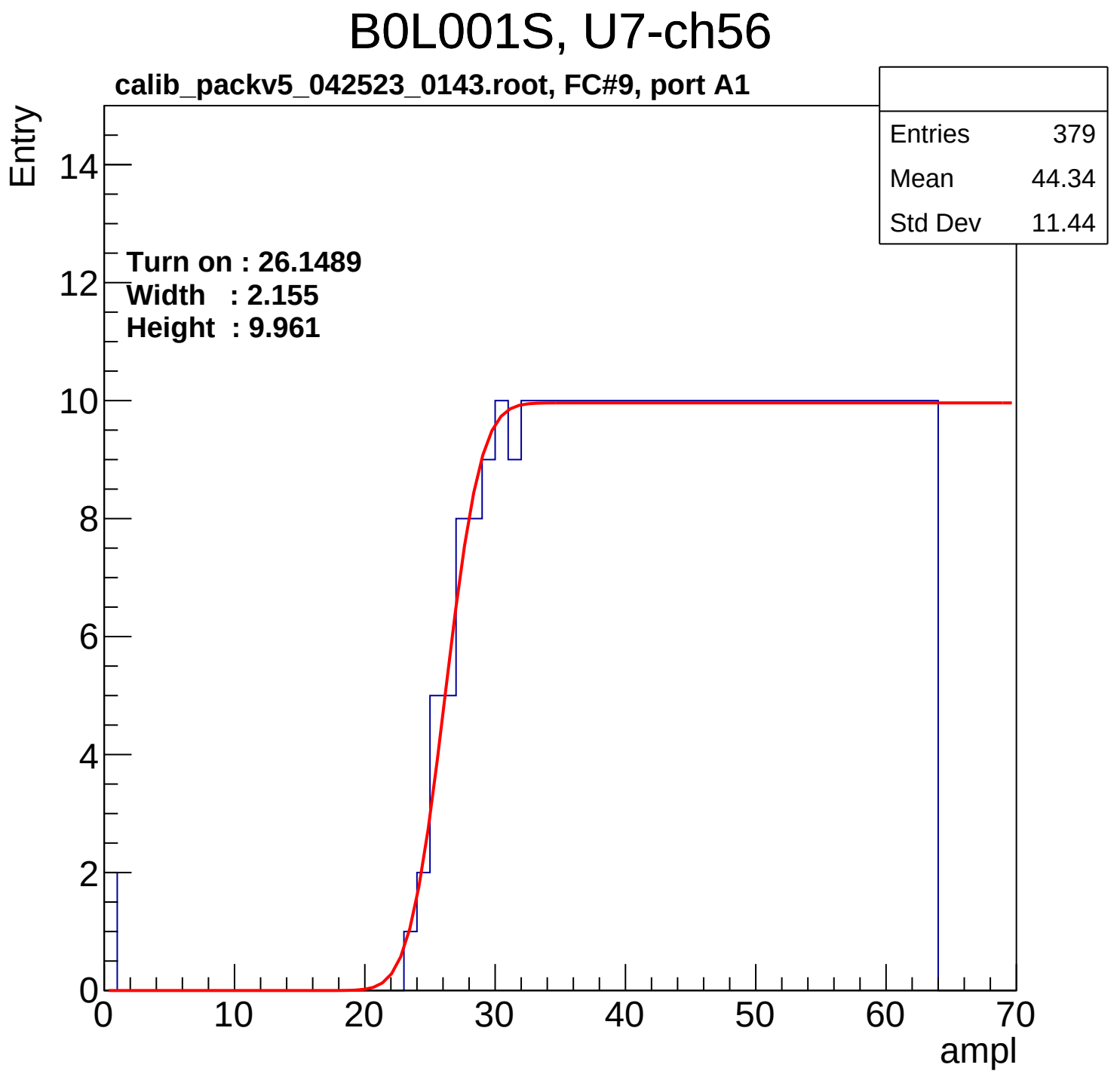
B0L001S, U7-ch56
calib_packv5_042523_0143.root, FC#9, port A1
Entries 379
Mean 44.34
Std Dev 11.44
Turn on : 26.1489
Width : 2.155
Height : 9.961
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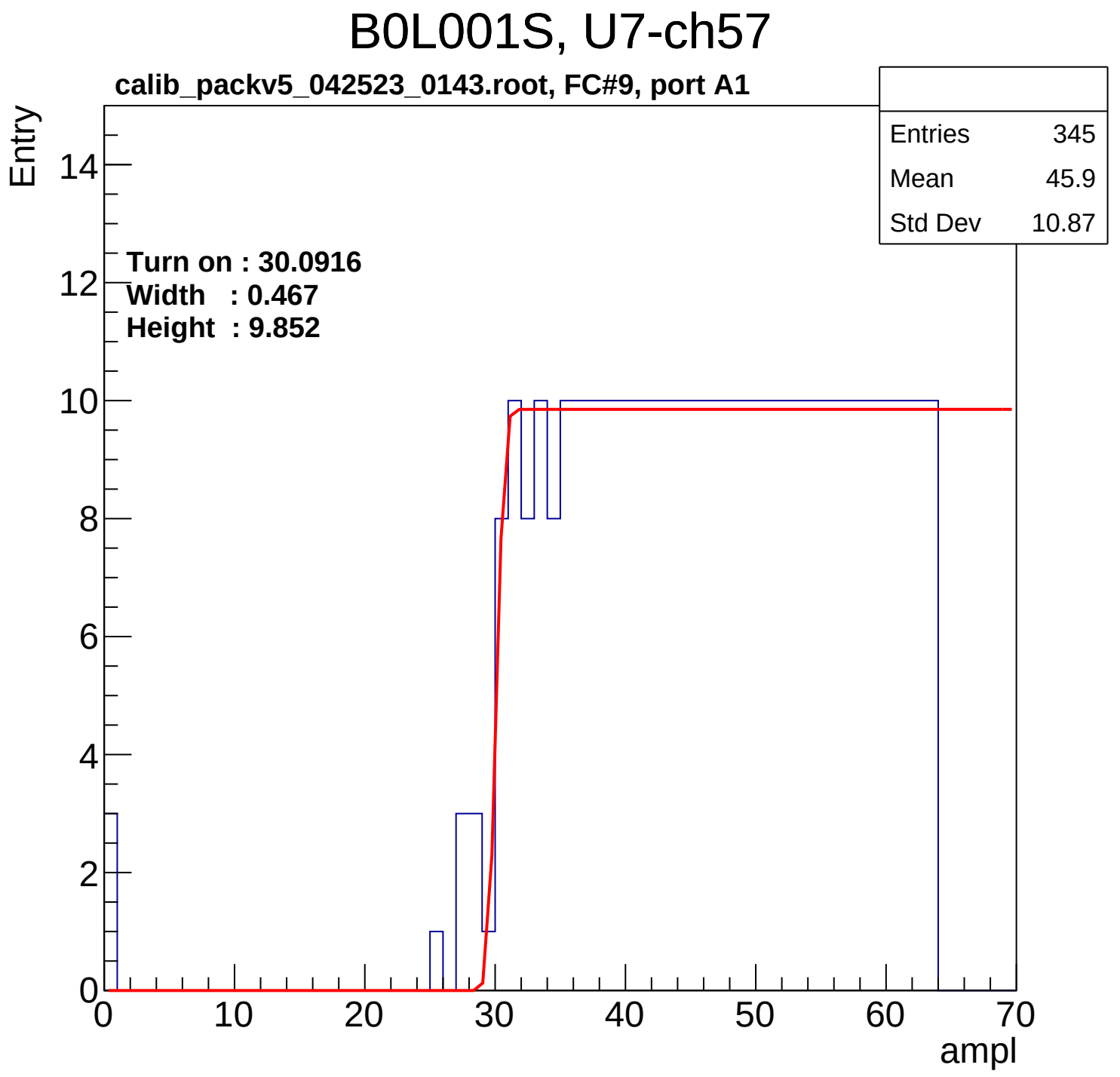
B0L001S, U7-ch57
calib_packv5_042523_0143.root, FC#9, port A1
Entries 345
Mean 45.9
Std Dev 10.87
Turn on : 30.0916
Width : 0.467
Height : 9.852
Entry
ampl
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20
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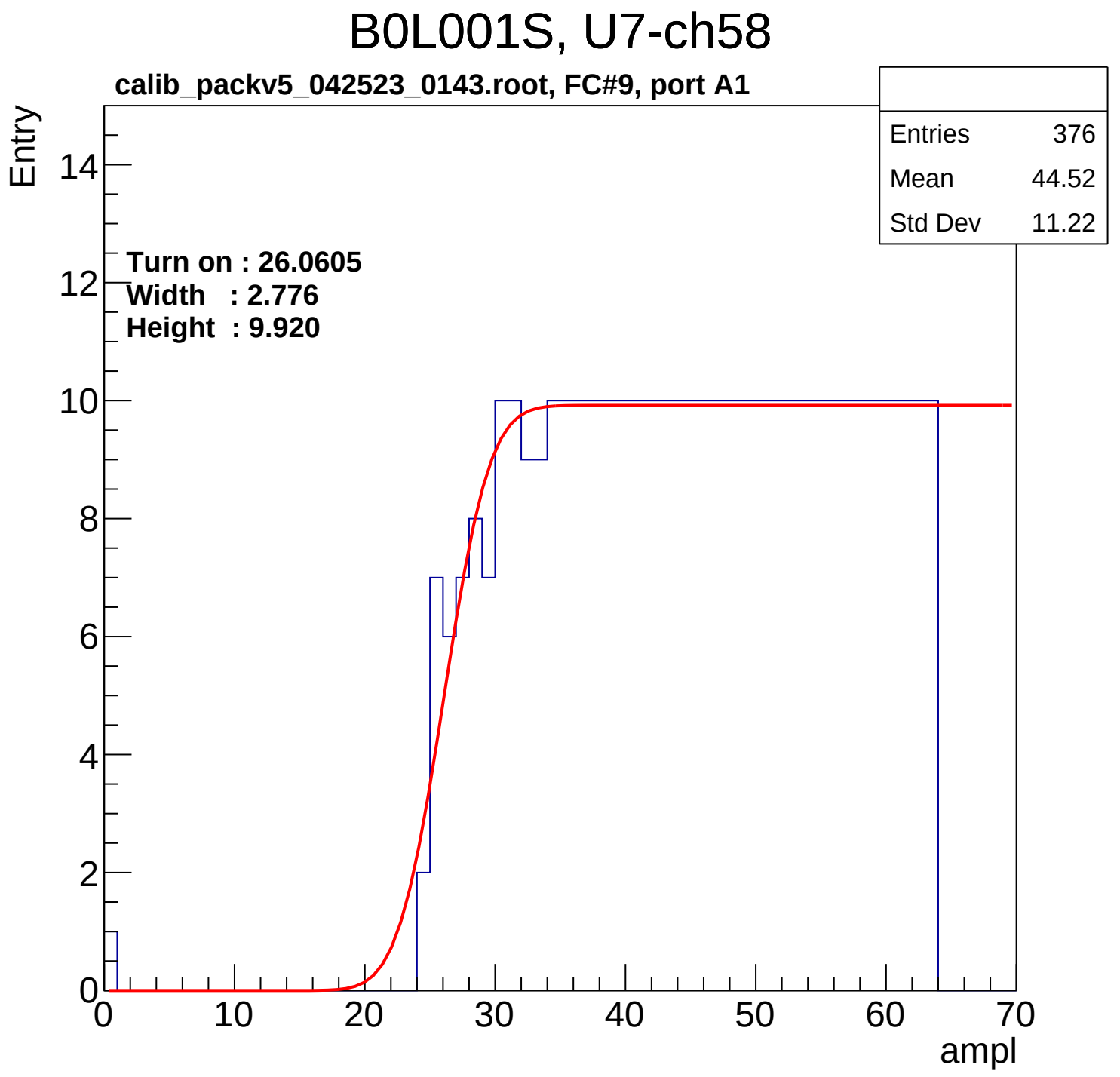
B0L001S, U7-ch58
calib_packv5_042523_0143.root, FC#9, port A1
Entries 376
Mean 44.52
Std Dev 11.22
Turn on : 26.0605
Width : 2.776
Height : 9.920
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ampl
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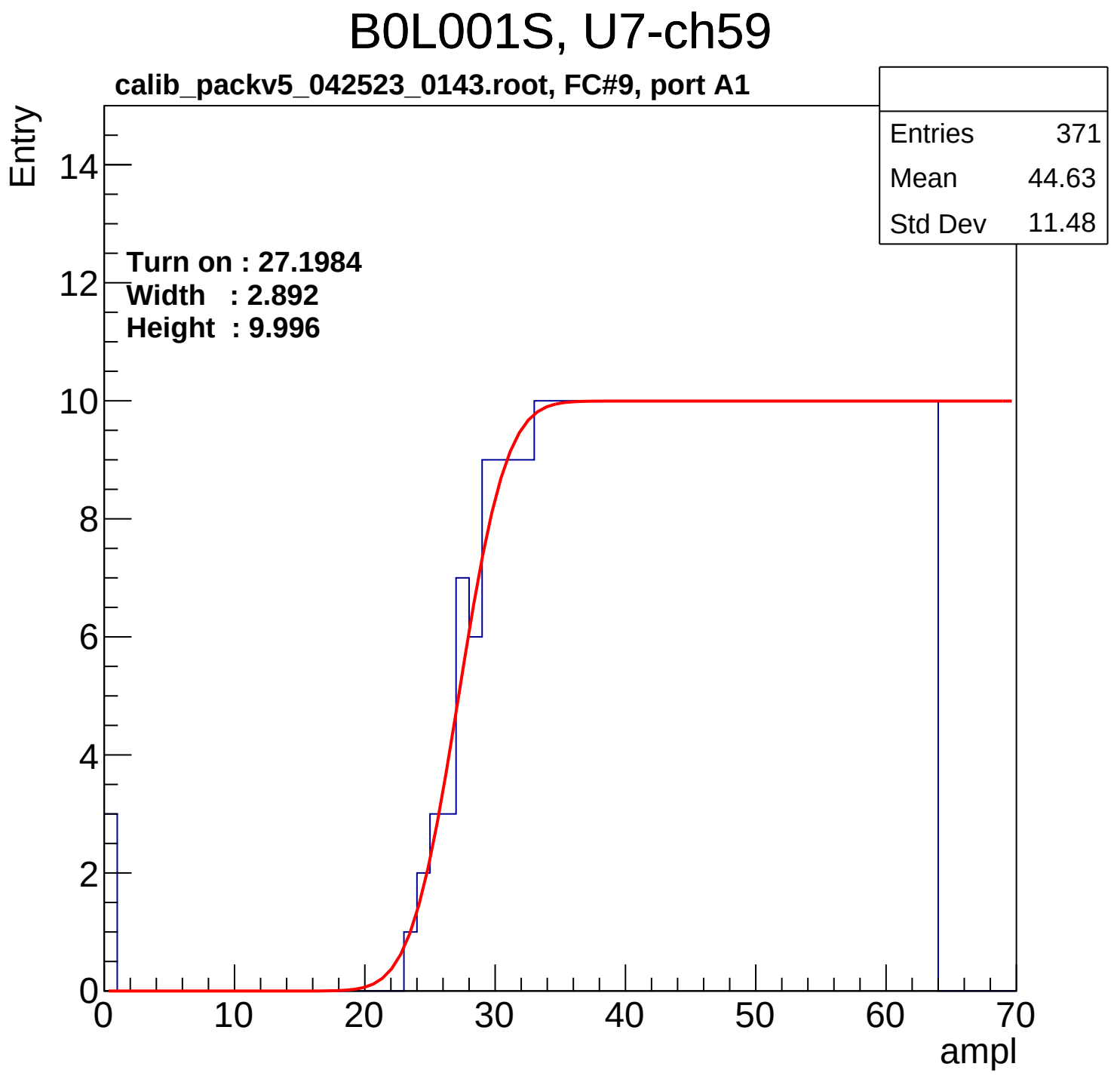
B0L001S, U7-ch59
calib_packv5_042523_0143.root, FC#9, port A1
Entries 371
Mean 44.63
Std Dev 11.48
Turn on : 27.1984
Width : 2.892
Height : 9.996
Entry
ampl
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6
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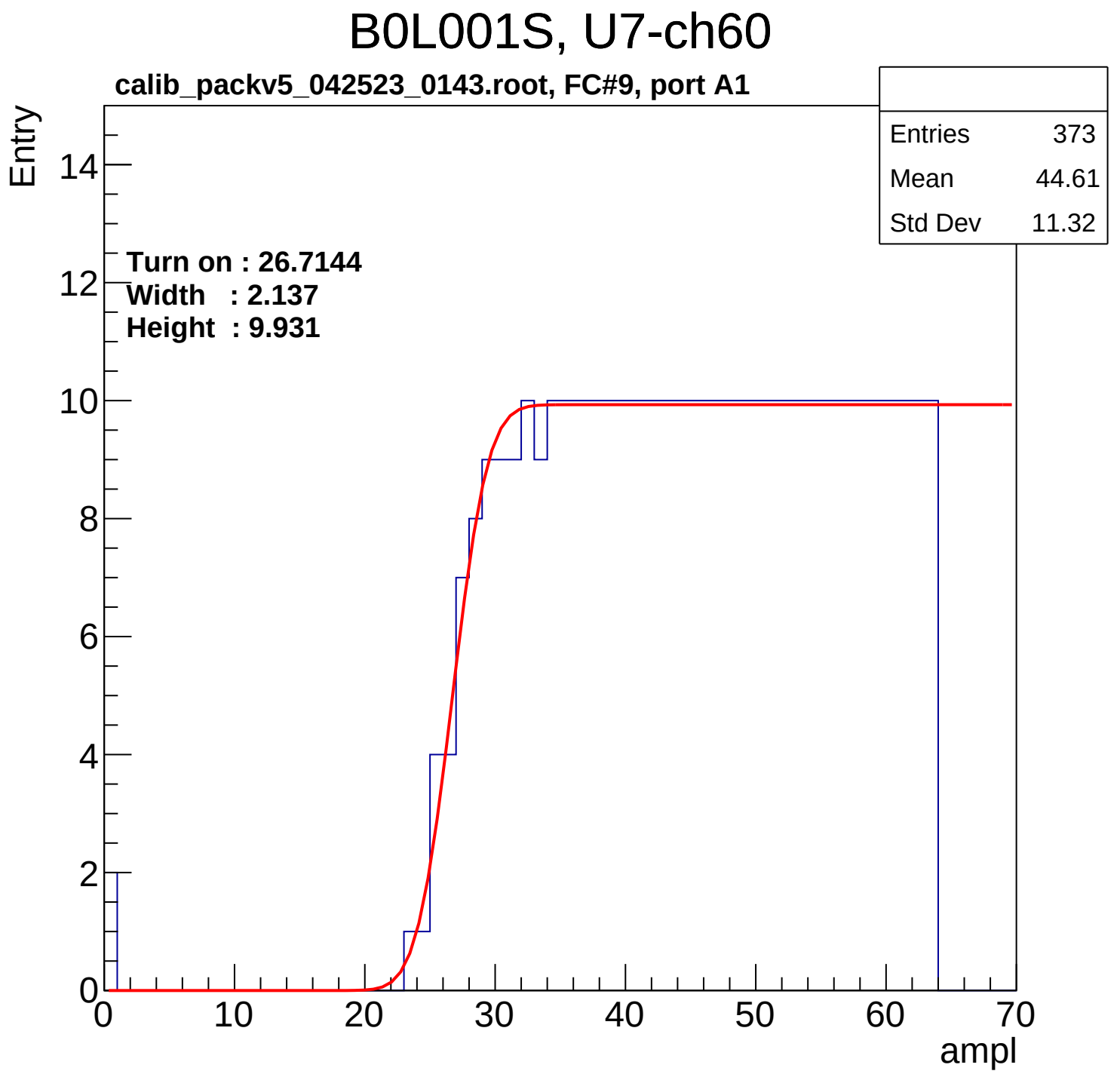
B0L001S, U7-ch60
calib_packv5_042523_0143.root, FC#9, port A1
Entries 373
Mean 44.61
Std Dev 11.32
Turn on : 26.7144
Width : 2.137
Height : 9.931
Entry
ampl
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2
4
6
8
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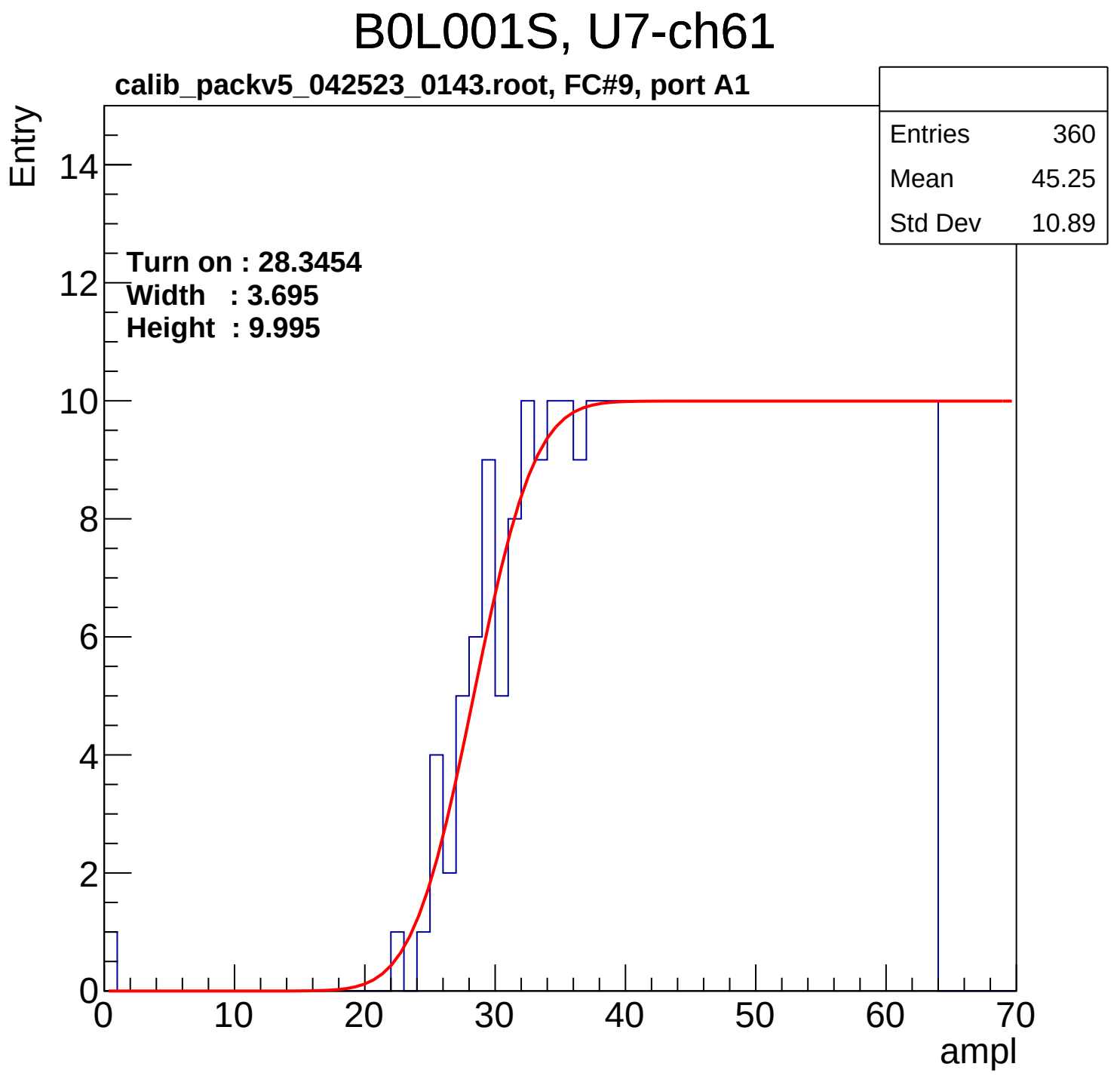
B0L001S, U7-ch61
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 45.25
Std Dev 10.89
Turn on : 28.3454
Width : 3.695
Height : 9.995
Entry
ampl
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2
4
6
8
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0
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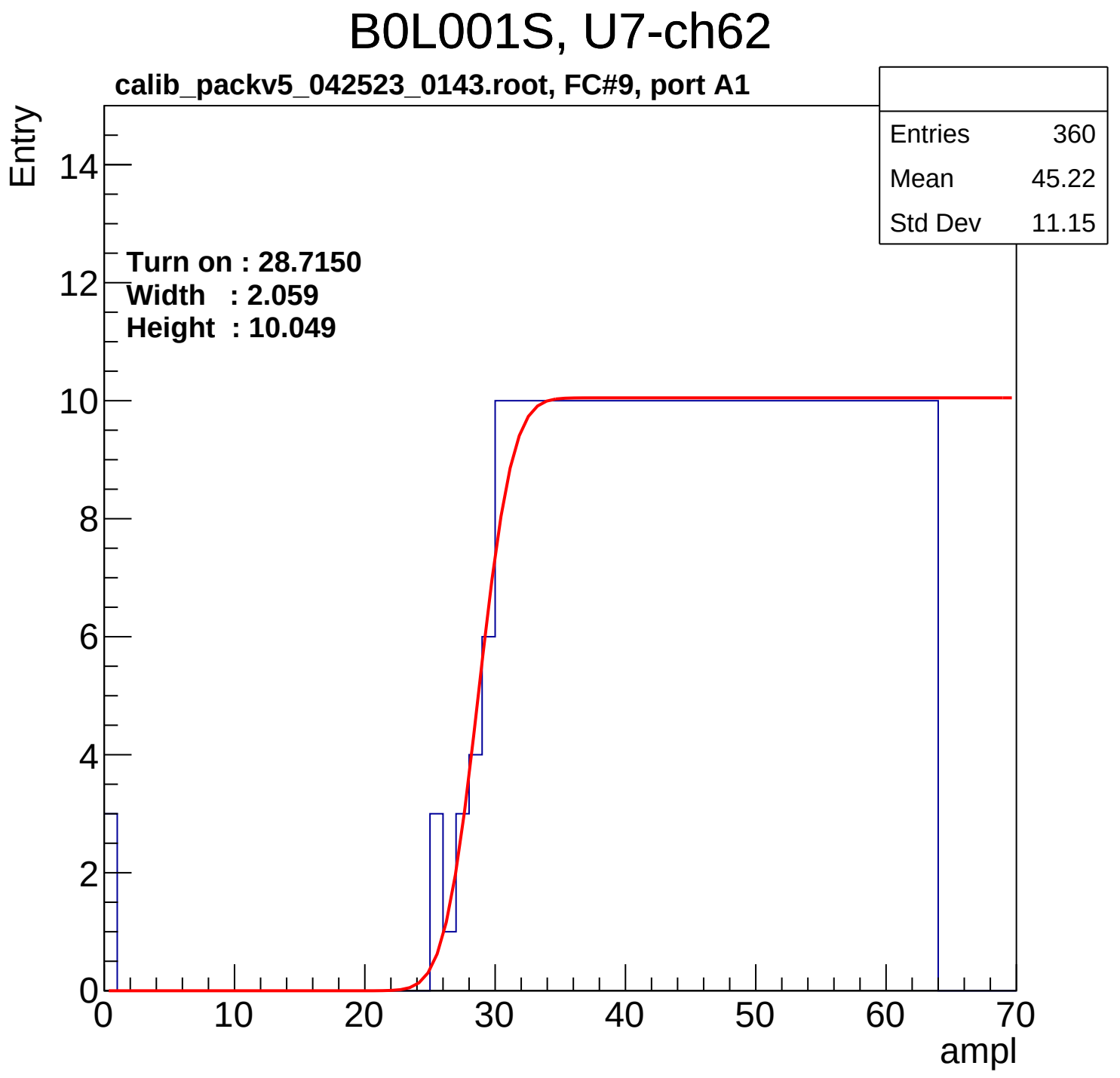
B0L001S, U7-ch62
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 45.22
Std Dev 11.15
Turn on : 28.7150
Width : 2.059
Height : 10.049
Entry
ampl
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2
4
6
8
10
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0
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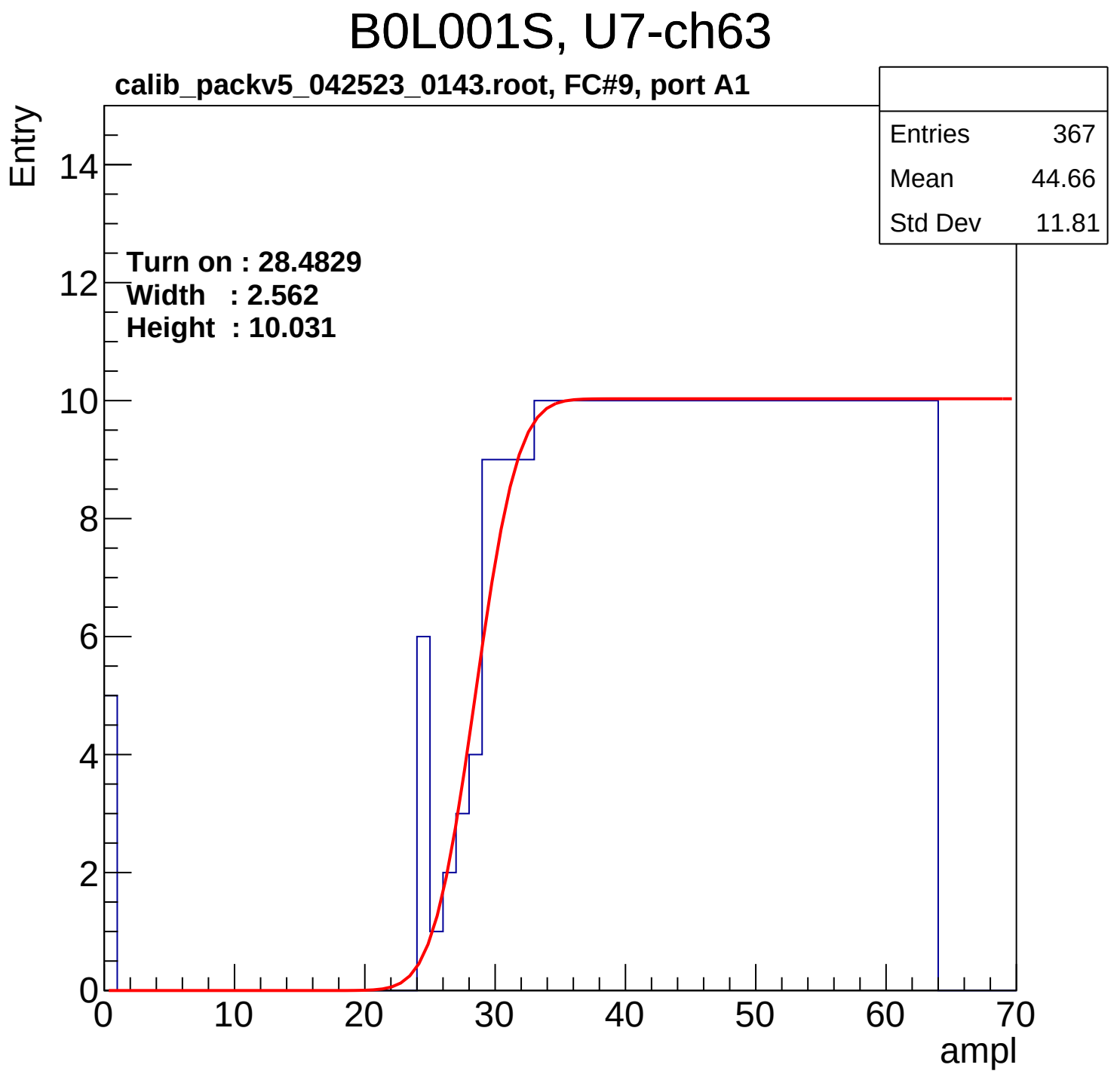
B0L001S, U7-ch63
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.66
Std Dev 11.81
Turn on : 28.4829
Width : 2.562
Height : 10.031
Entry
ampl
0
2
4
6
8
10
12
14
0
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40
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60
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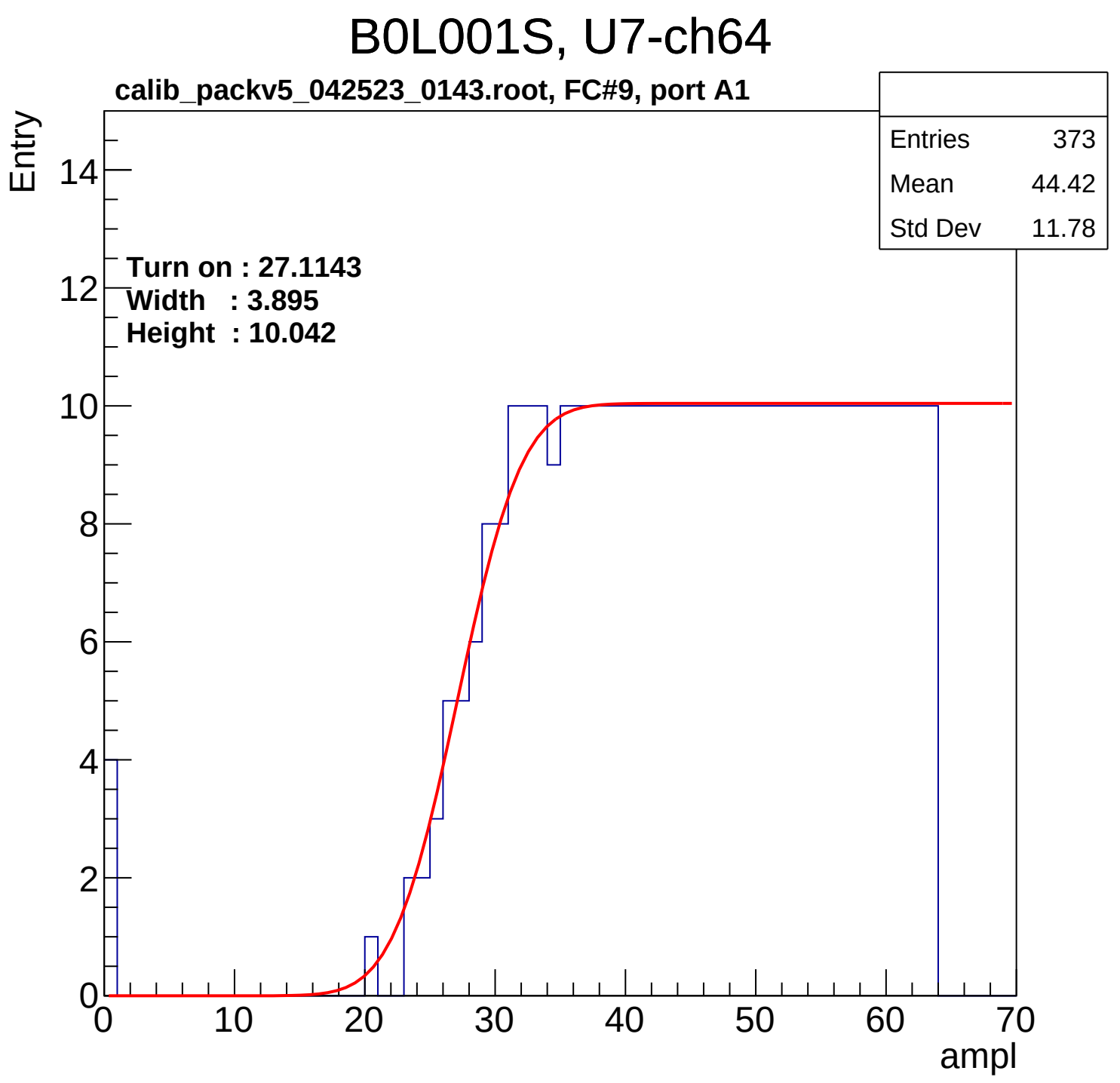
B0L001S, U7-ch64
calib_packv5_042523_0143.root, FC#9, port A1
Entries 373
Mean 44.42
Std Dev 11.78
Turn on : 27.1143
Width : 3.895
Height : 10.042
Entry
ampl
0
2
4
6
8
10
12
14
0
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60
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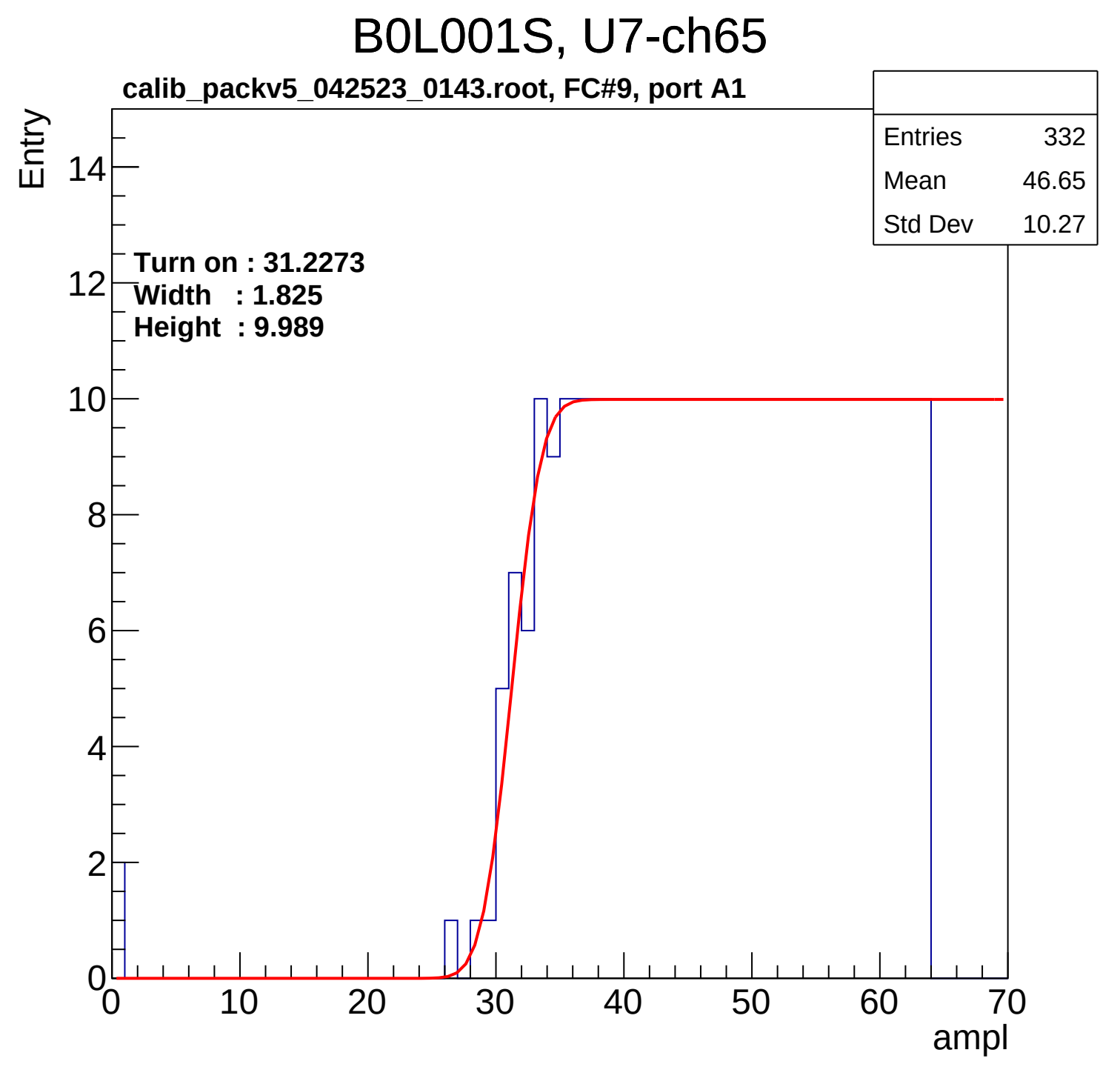
B0L001S, U7-ch65
calib_packv5_042523_0143.root, FC#9, port A1
Entries 332
Mean 46.65
Std Dev 10.27
Turn on : 31.2273
Width : 1.825
Height : 9.989
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
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60
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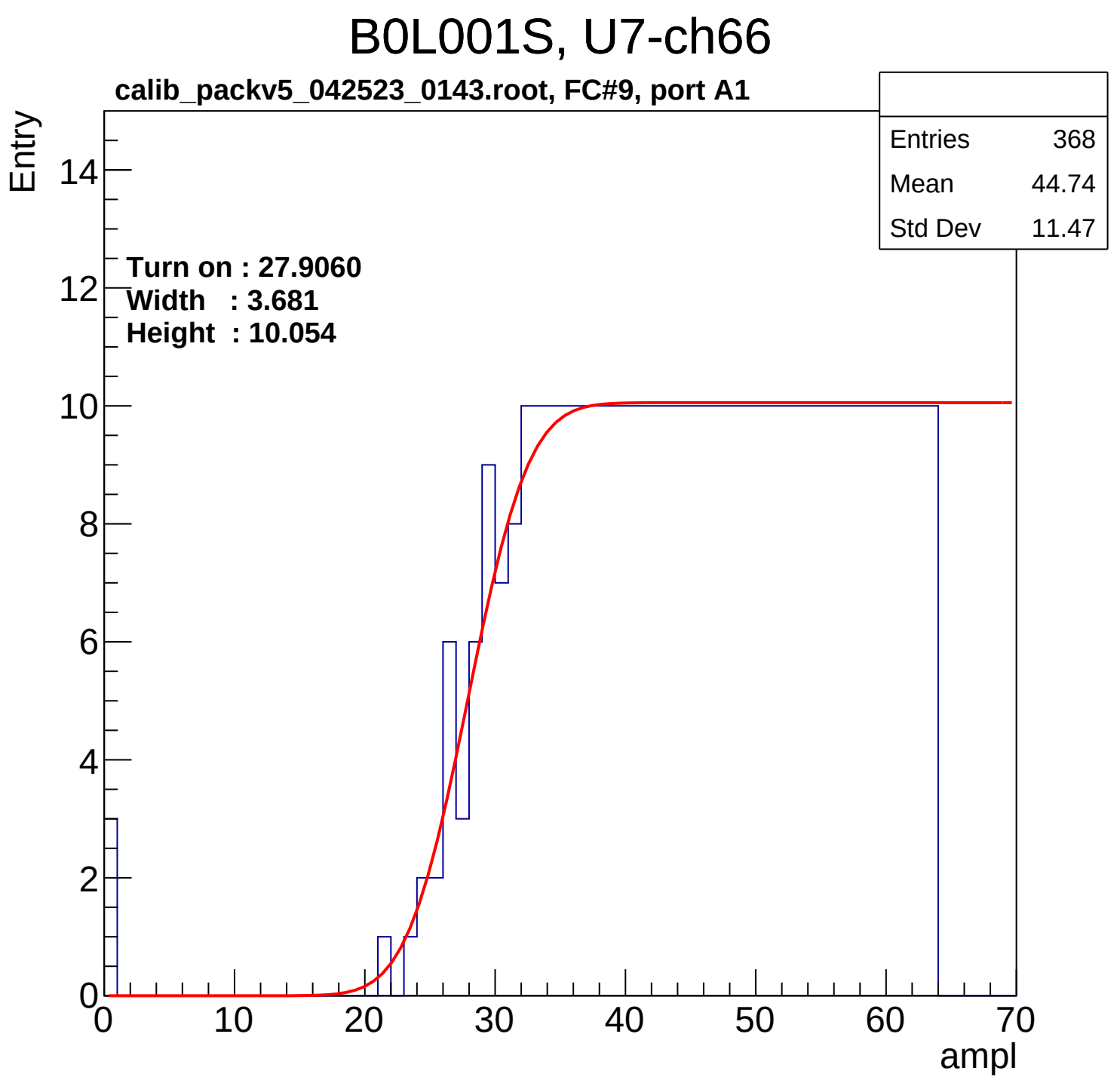
B0L001S, U7-ch66
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.74
Std Dev 11.47
Turn on : 27.9060
Width : 3.681
Height : 10.054
Entry
ampl
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4
6
8
10
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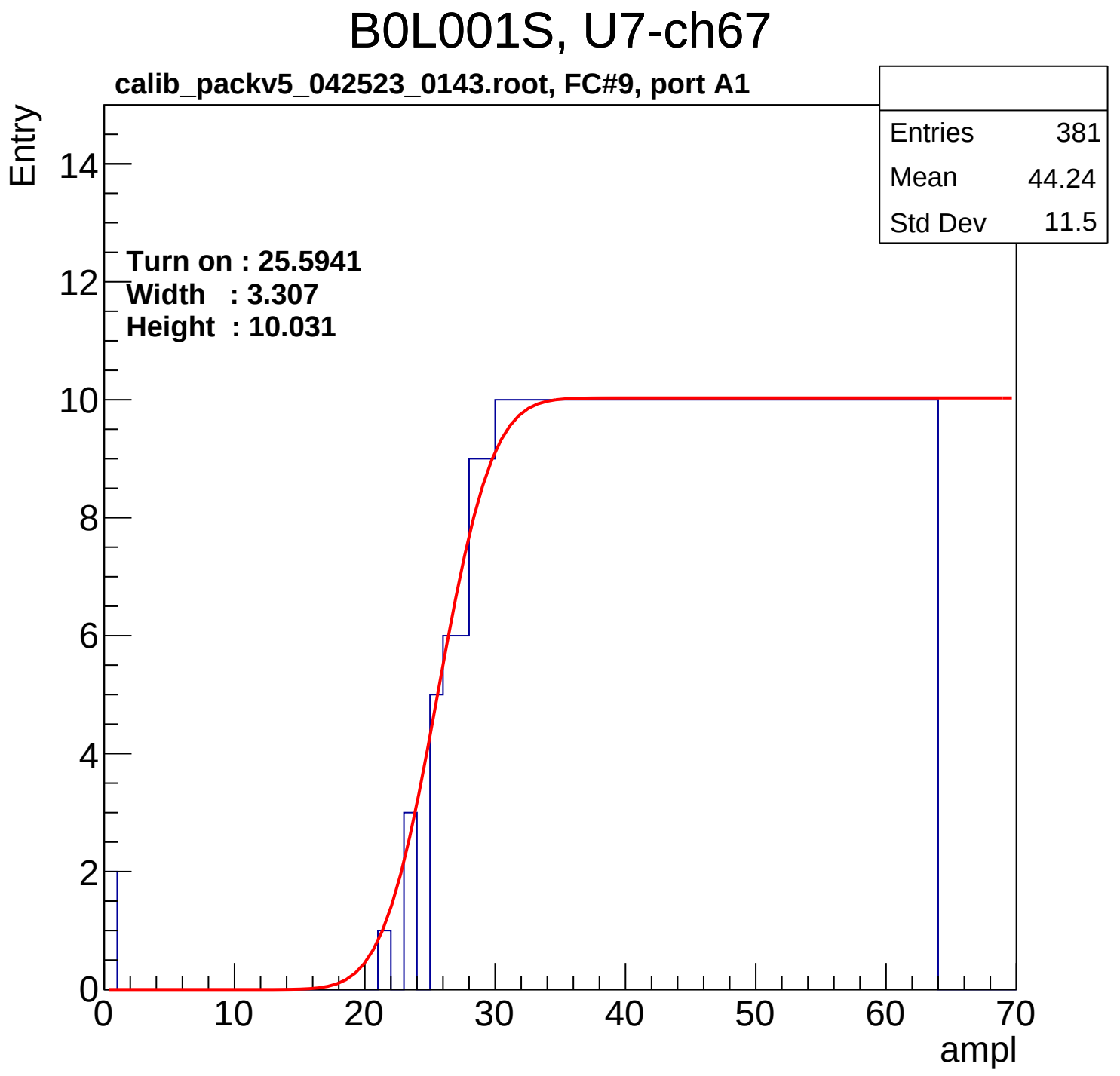
B0L001S, U7-ch67
calib_packv5_042523_0143.root, FC#9, port A1
Entries 381
Mean 44.24
Std Dev 11.5
Turn on : 25.5941
Width : 3.307
Height : 10.031
Entry
ampl
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2
4
6
8
10
12
14
0
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60
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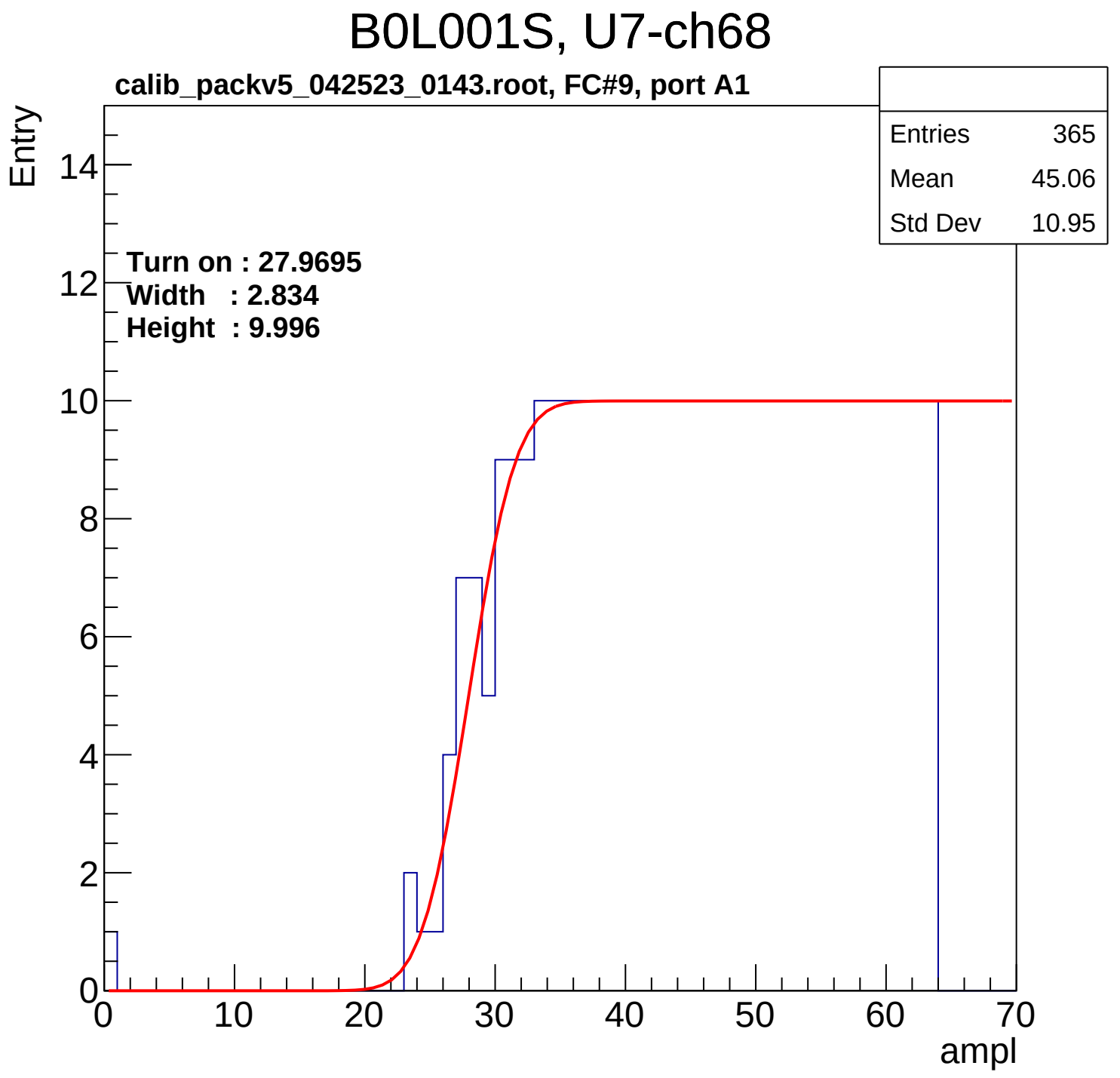
B0L001S, U7-ch68
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 45.06
Std Dev 10.95
Turn on : 27.9695
Width : 2.834
Height : 9.996
Entry
ampl
0
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4
6
8
10
12
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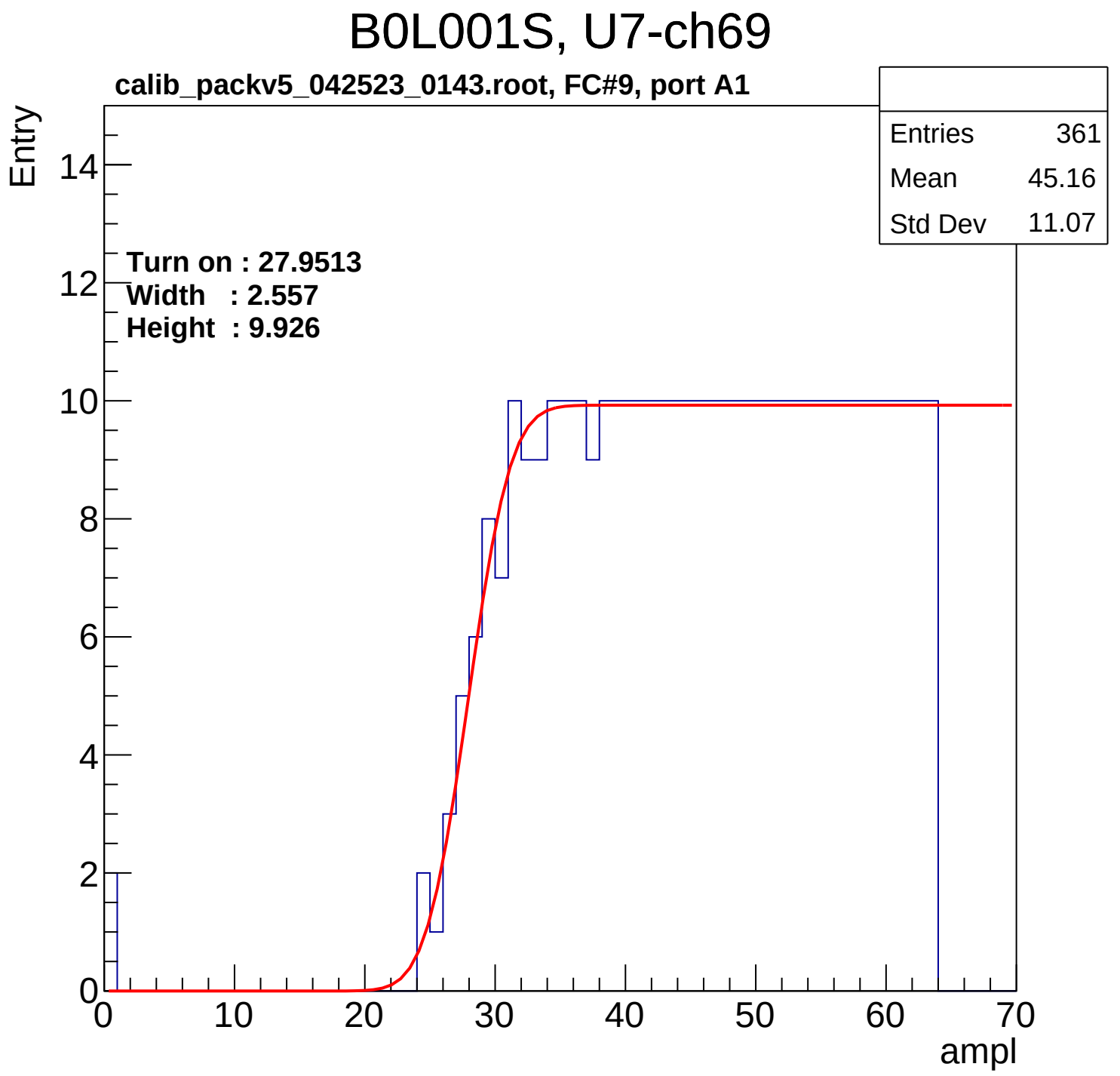
B0L001S, U7-ch69
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 45.16
Std Dev 11.07
Turn on : 27.9513
Width : 2.557
Height : 9.926
Entry
ampl
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6
8
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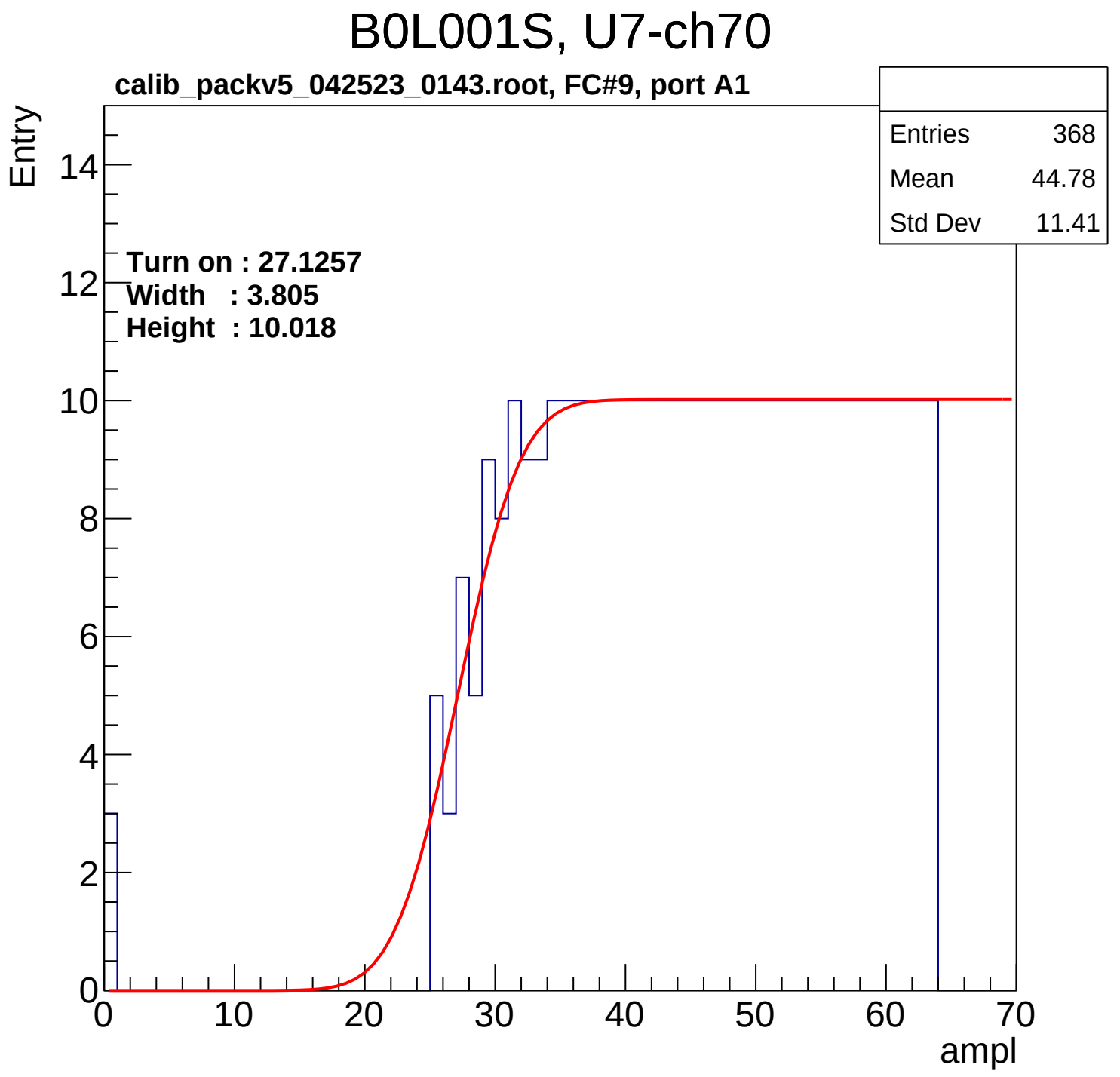
B0L001S, U7-ch70
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.78
Std Dev 11.41
Turn on : 27.1257
Width : 3.805
Height : 10.018
Entry
ampl
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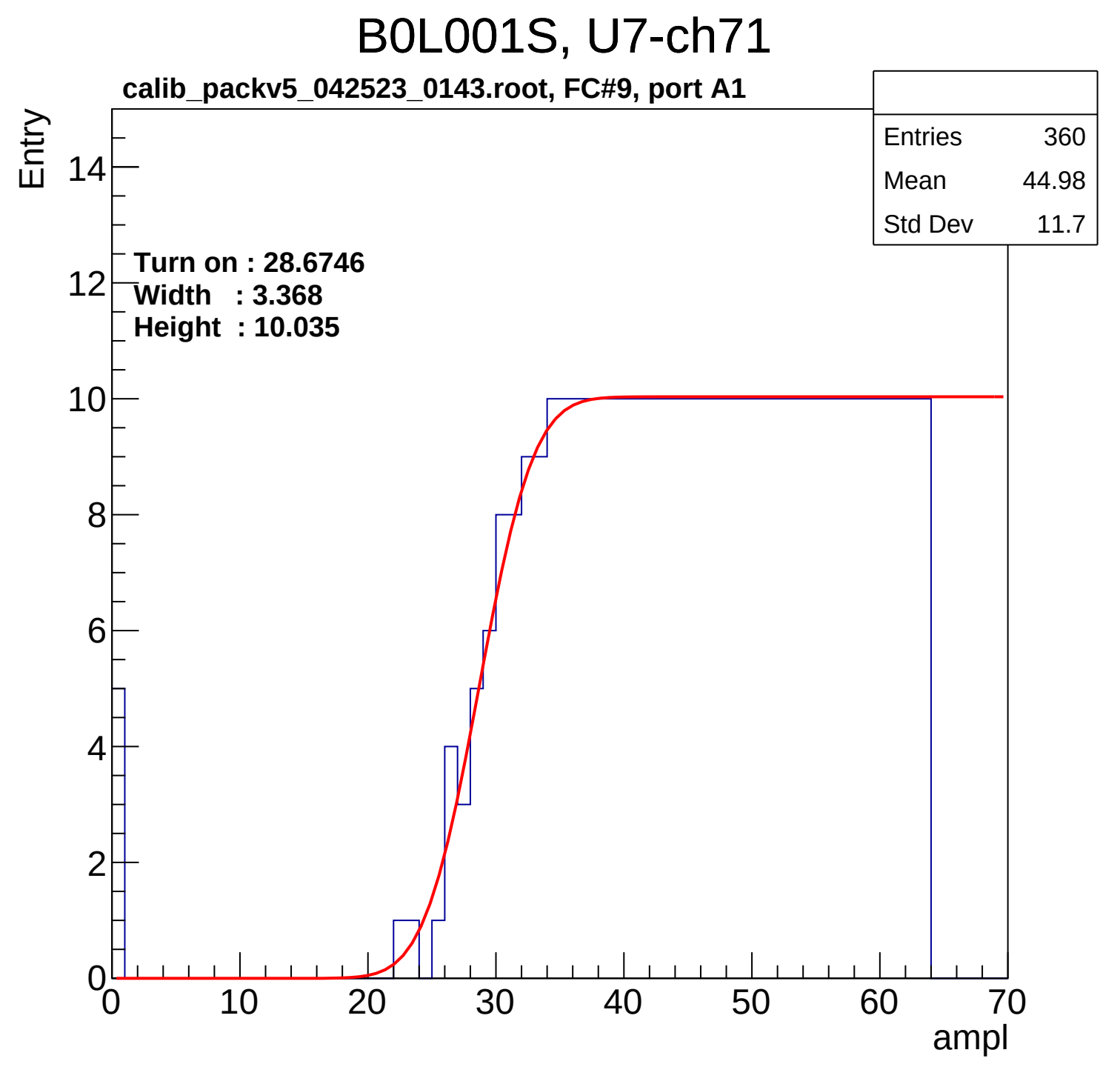
B0L001S, U7-ch71
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 44.98
Std Dev 11.7
Turn on : 28.6746
Width : 3.368
Height : 10.035
Entry
ampl
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6
8
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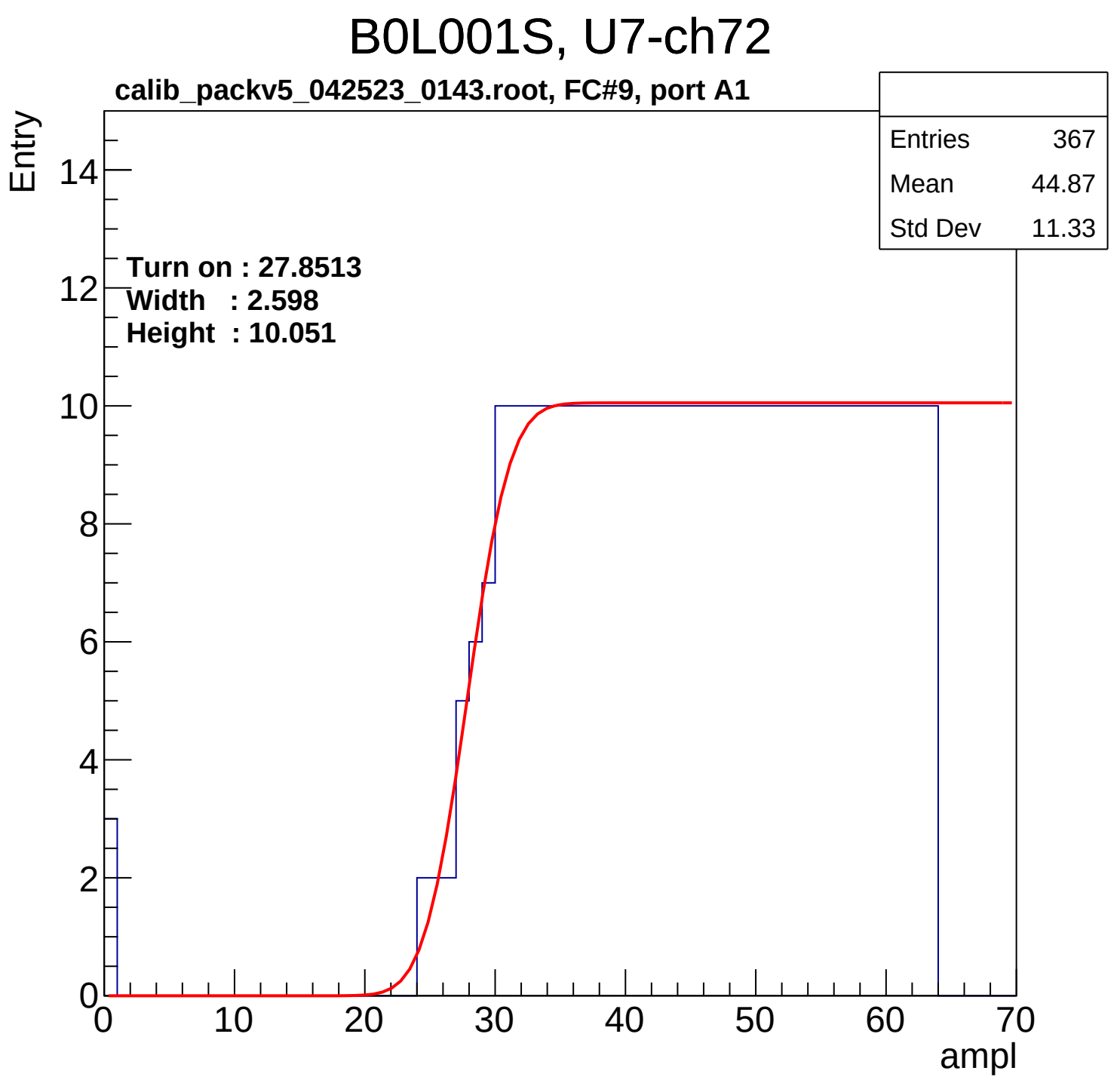
B0L001S, U7-ch72
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.87
Std Dev 11.33
Turn on : 27.8513
Width : 2.598
Height : 10.051
Entry
ampl
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4
6
8
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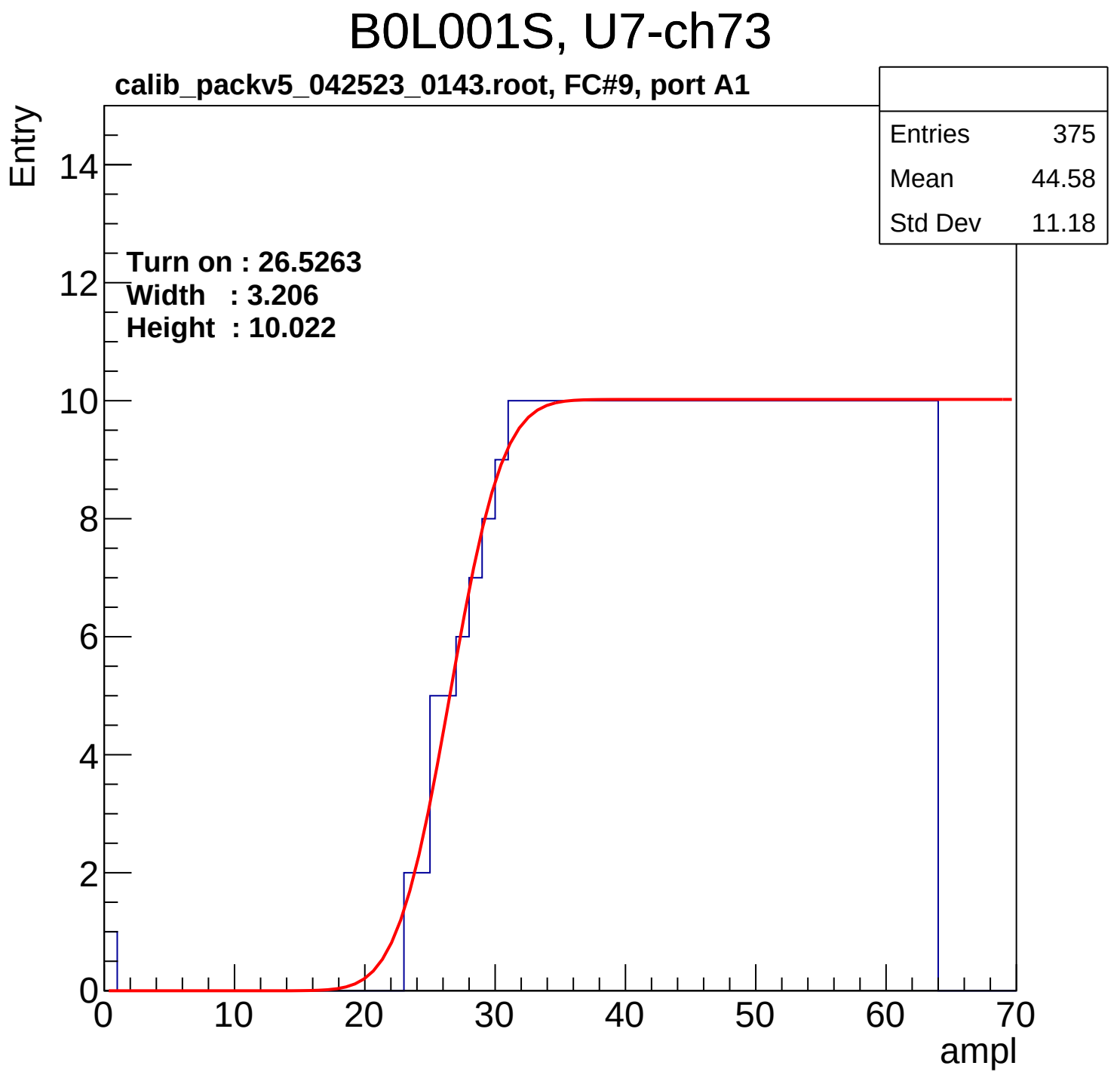
B0L001S, U7-ch73
calib_packv5_042523_0143.root, FC#9, port A1
Entries 375
Mean 44.58
Std Dev 11.18
Turn on : 26.5263
Width : 3.206
Height : 10.022
Entry
ampl
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10
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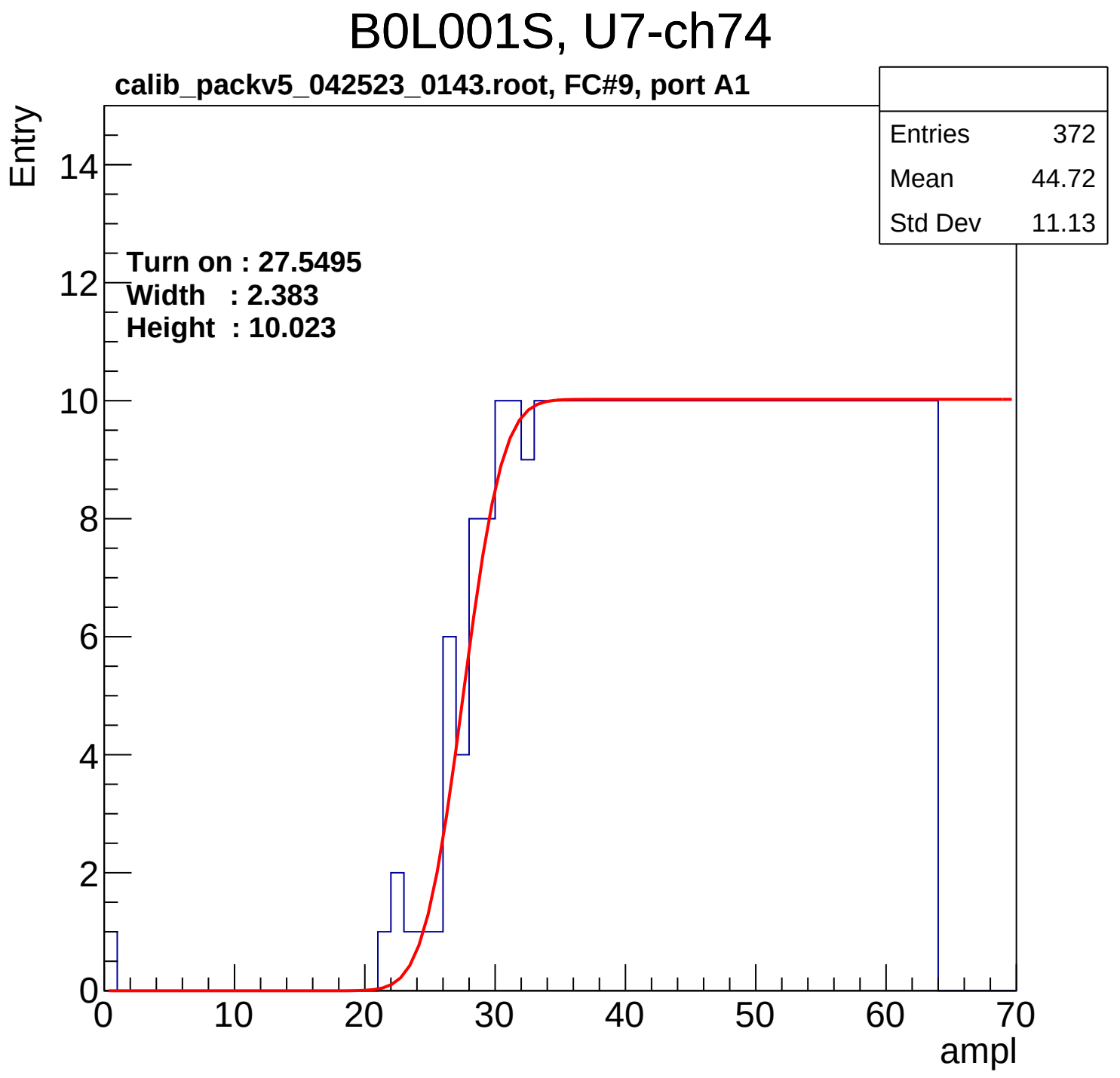
B0L001S, U7-ch74
calib_packv5_042523_0143.root, FC#9, port A1
Entries 372
Mean 44.72
Std Dev 11.13
Turn on : 27.5495
Width : 2.383
Height : 10.023
Entry
ampl
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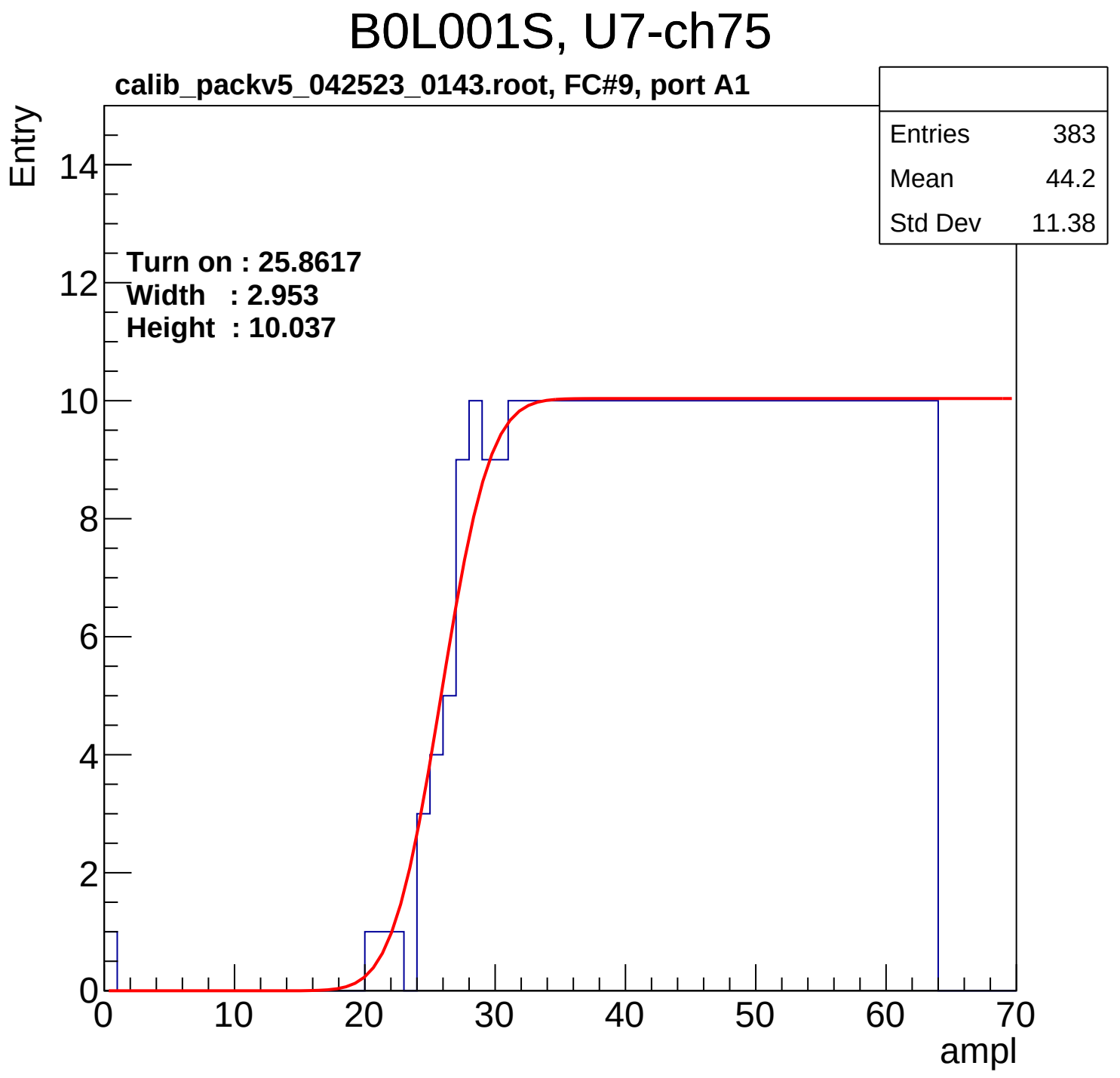
B0L001S, U7-ch75
calib_packv5_042523_0143.root, FC#9, port A1
Entries 383
Mean 44.2
Std Dev 11.38
Turn on : 25.8617
Width : 2.953
Height : 10.037
Entry
ampl
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8
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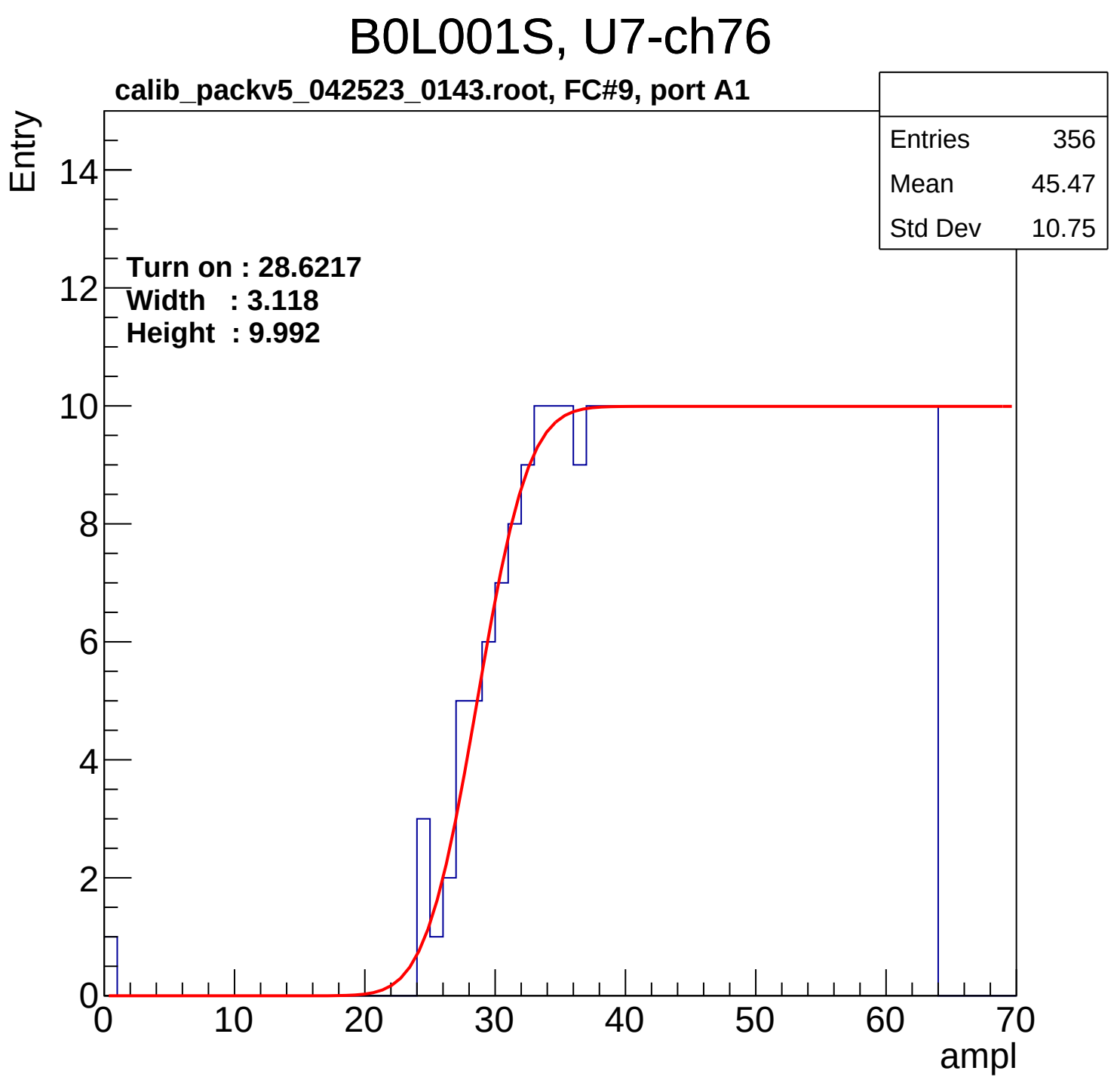
B0L001S, U7-ch76
calib_packv5_042523_0143.root, FC#9, port A1
Entries 356
Mean 45.47
Std Dev 10.75
Turn on : 28.6217
Width : 3.118
Height : 9.992
Entry
ampl
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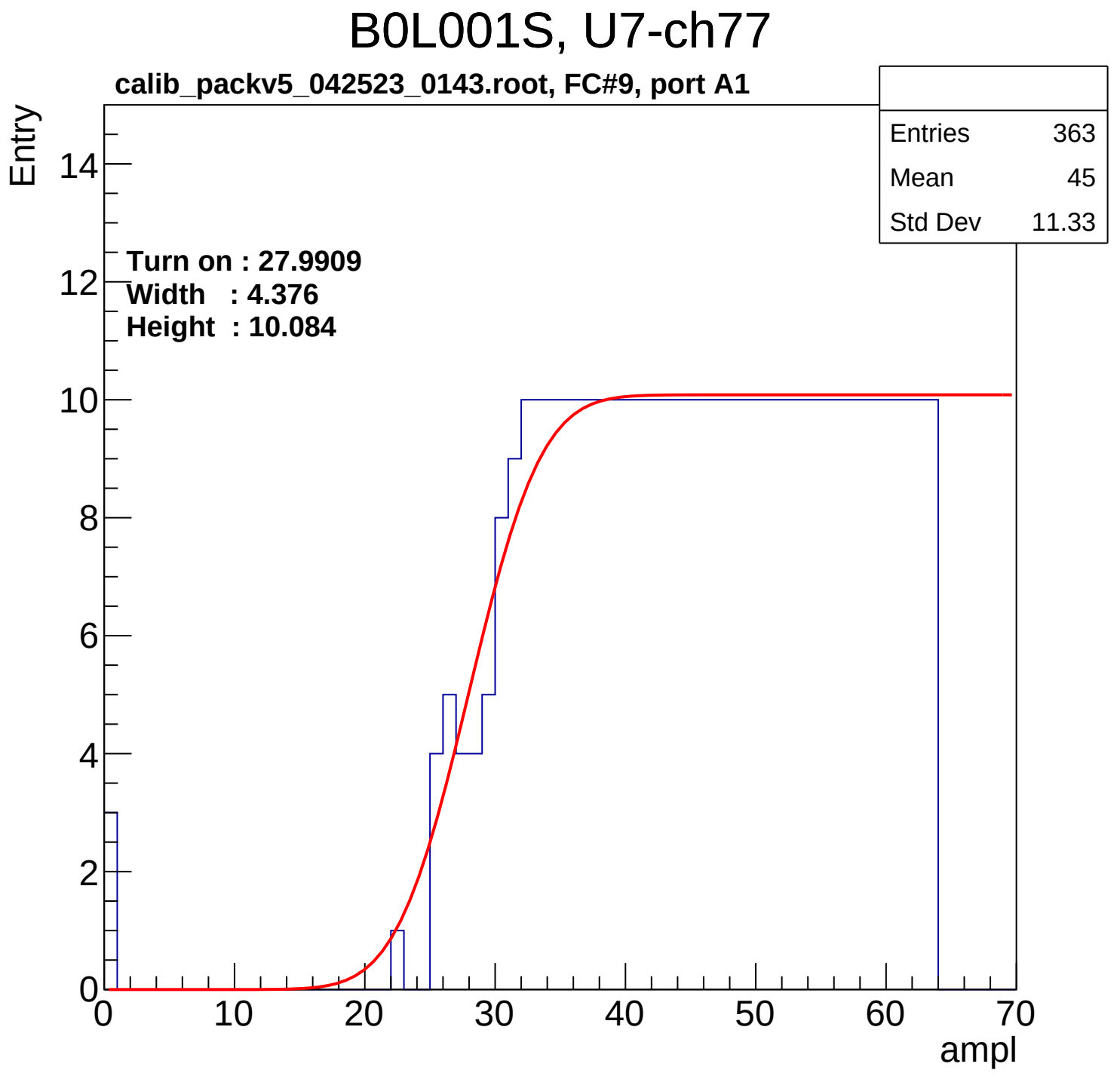
B0L001S, U7-ch77
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 45
Std Dev 11.33
Turn on : 27.9909
Width : 4.376
Height : 10.084
Entry
ampl
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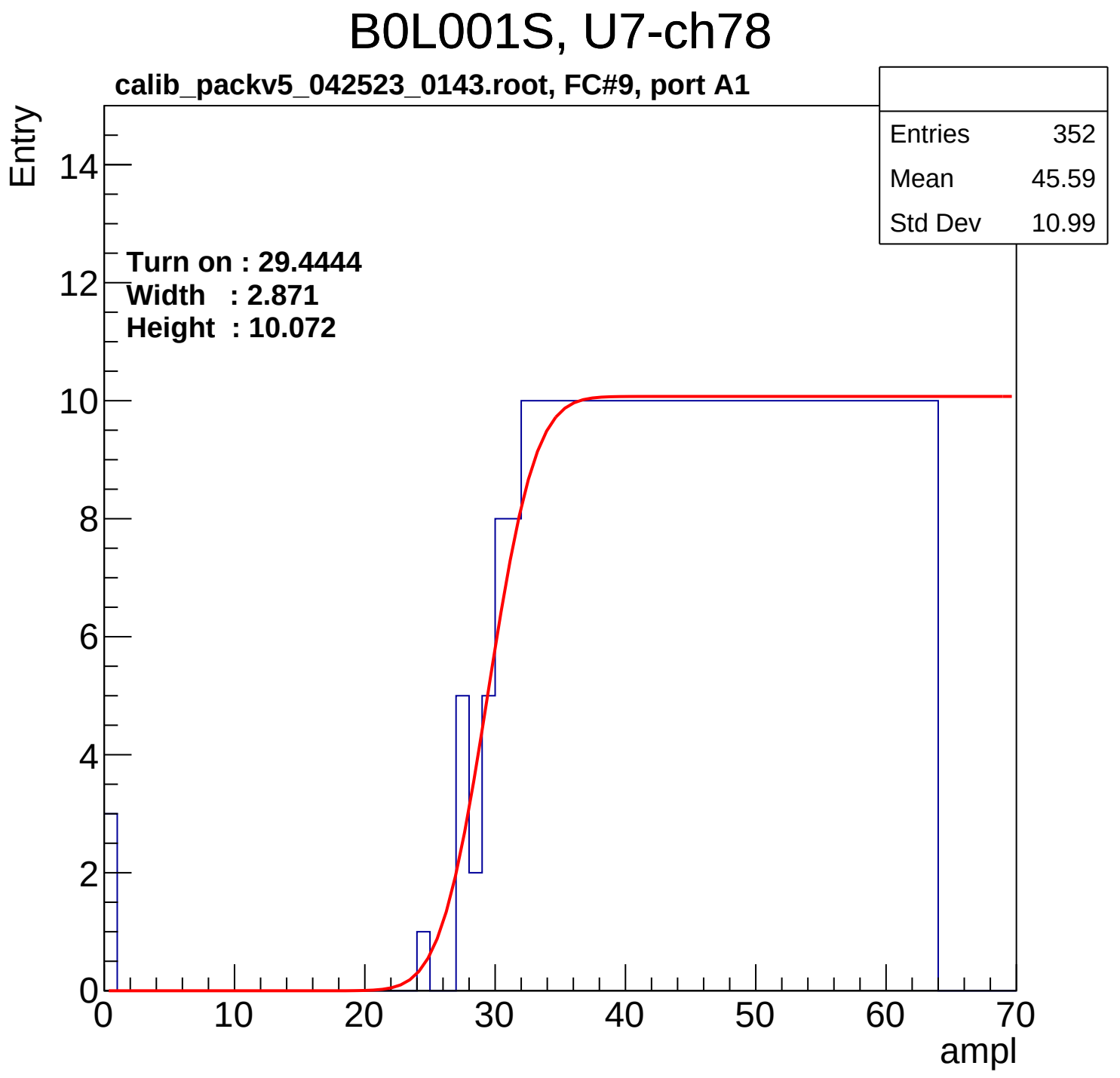
B0L001S, U7-ch78
calib_packv5_042523_0143.root, FC#9, port A1
Entries 352
Mean 45.59
Std Dev 10.99
Turn on : 29.4444
Width : 2.871
Height : 10.072
Entry
ampl
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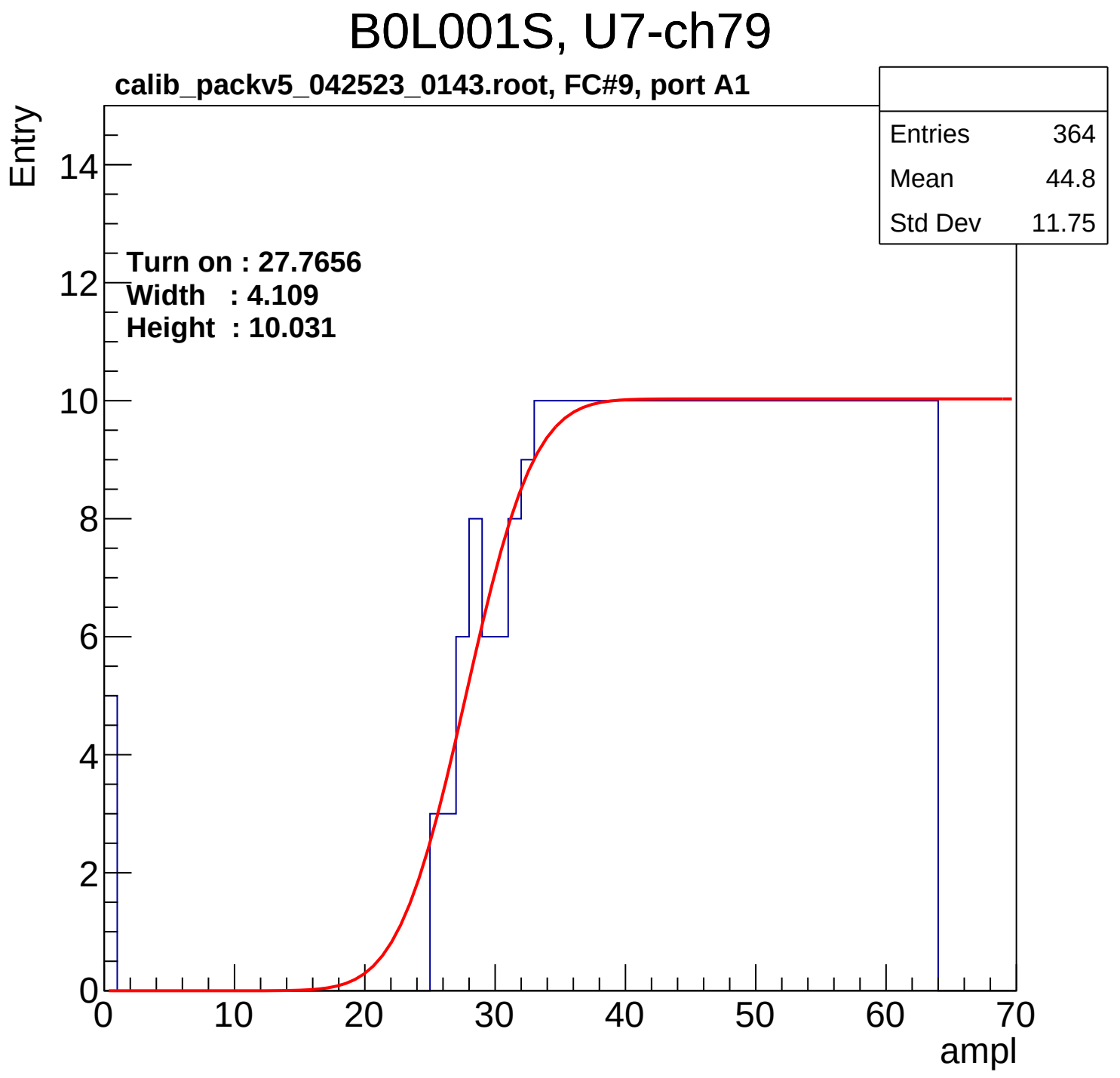
B0L001S, U7-ch79
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 44.8
Std Dev 11.75
Turn on : 27.7656
Width : 4.109
Height : 10.031
Entry
ampl
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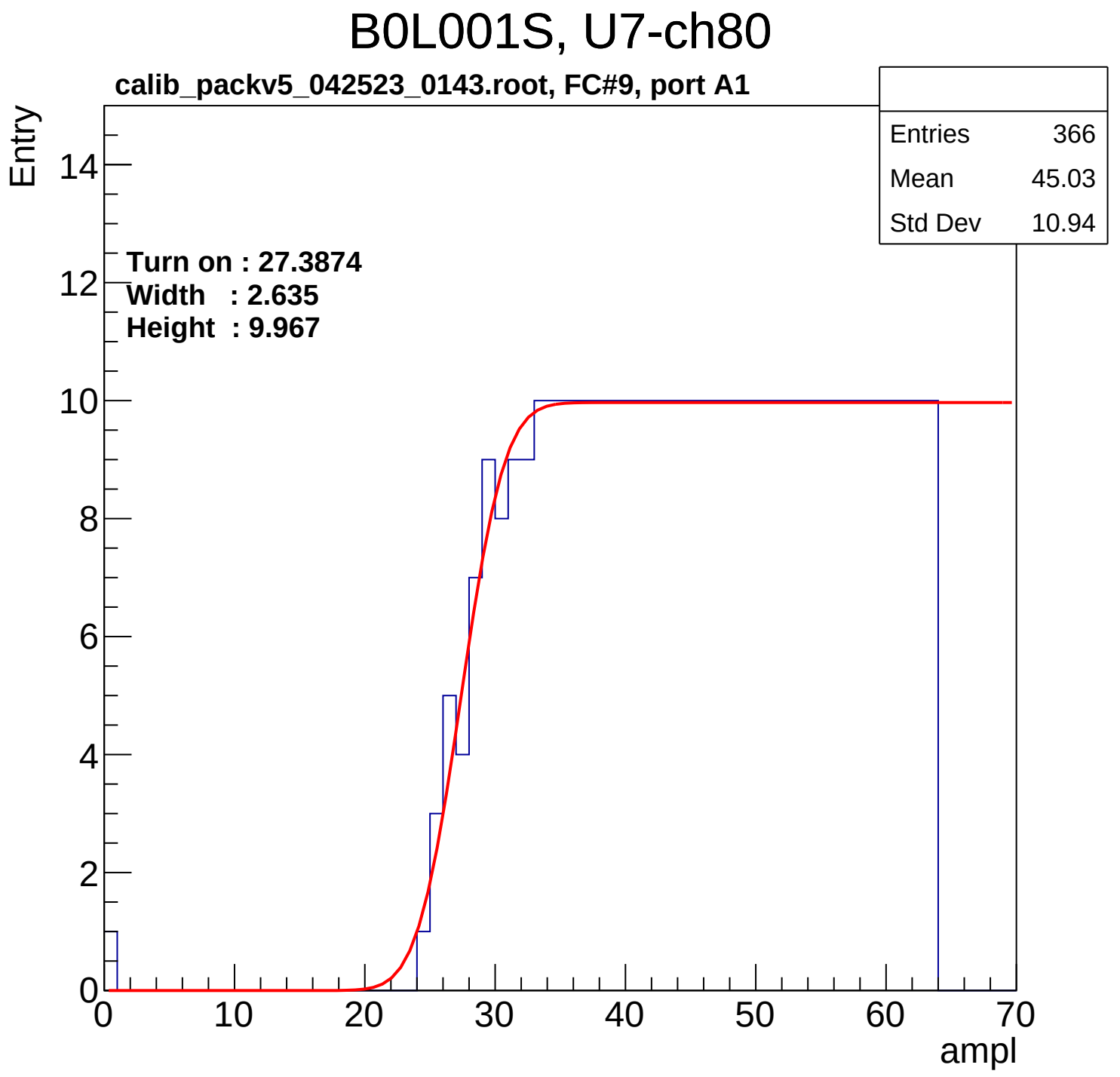
B0L001S, U7-ch80
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 45.03
Std Dev 10.94
Turn on : 27.3874
Width : 2.635
Height : 9.967
Entry
ampl
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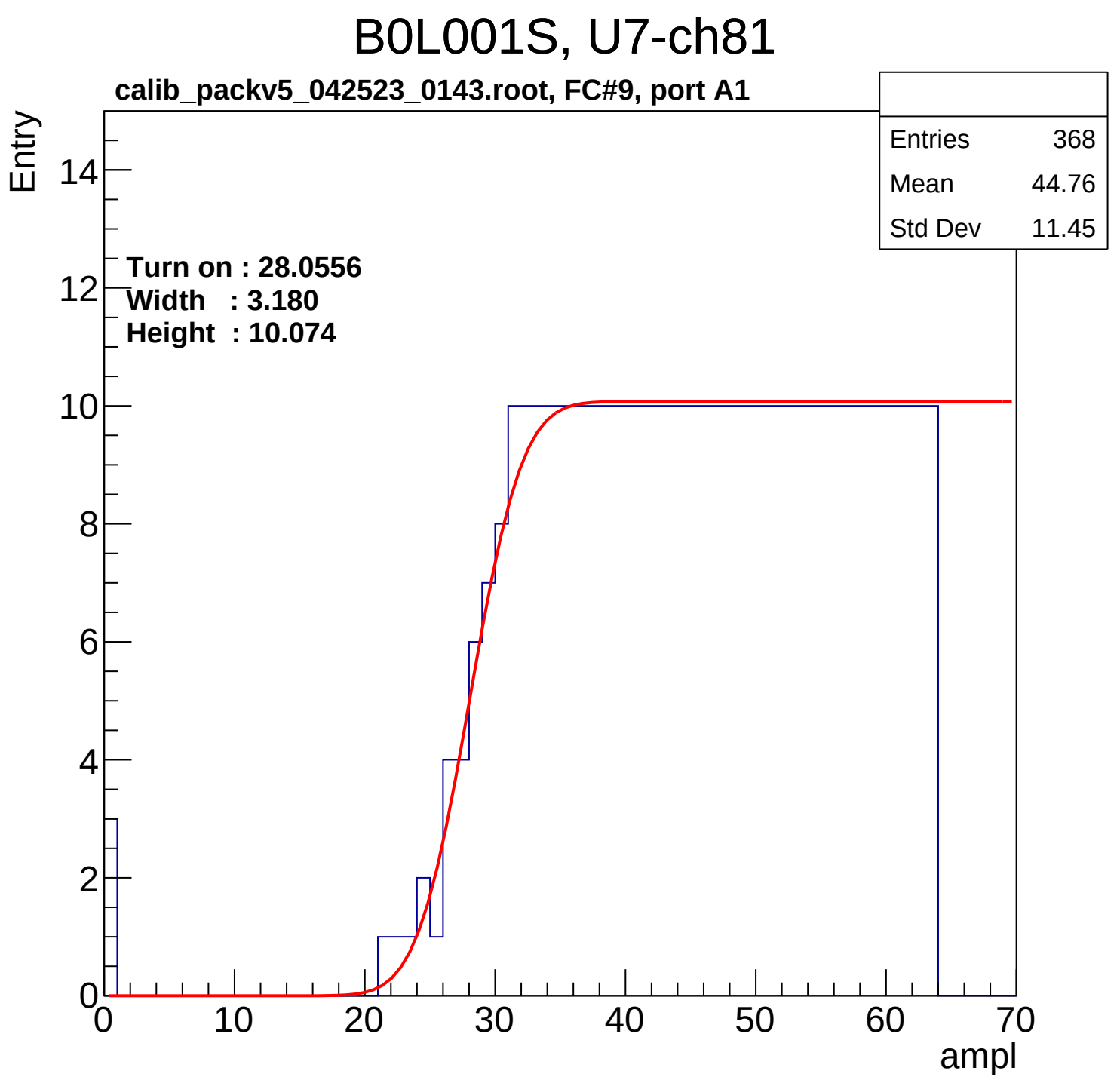
B0L001S, U7-ch81
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.76
Std Dev 11.45
Turn on : 28.0556
Width : 3.180
Height : 10.074
Entry
ampl
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4
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8
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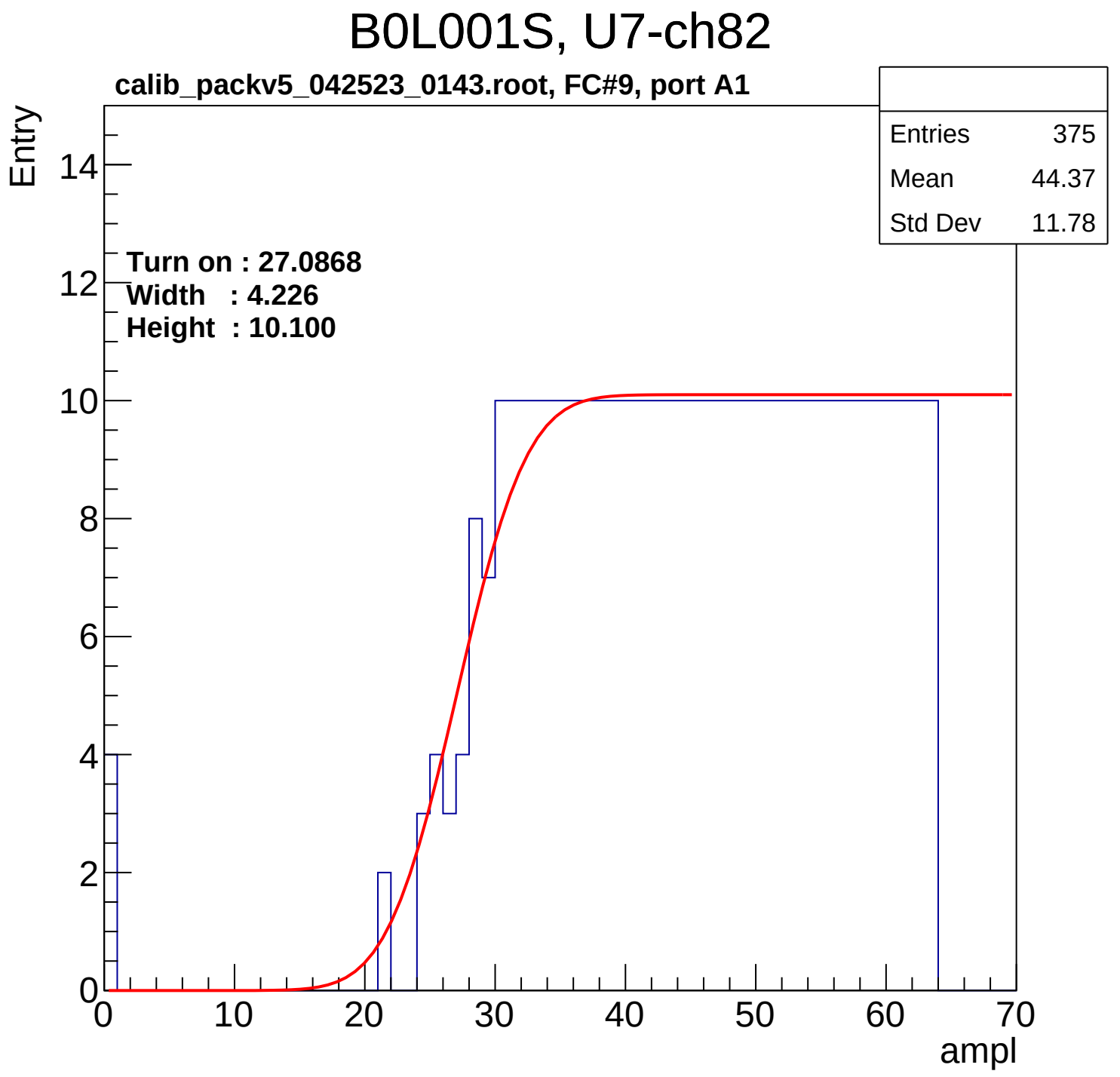
B0L001S, U7-ch82
calib_packv5_042523_0143.root, FC#9, port A1
Entries 375
Mean 44.37
Std Dev 11.78
Turn on : 27.0868
Width : 4.226
Height : 10.100
Entry
ampl
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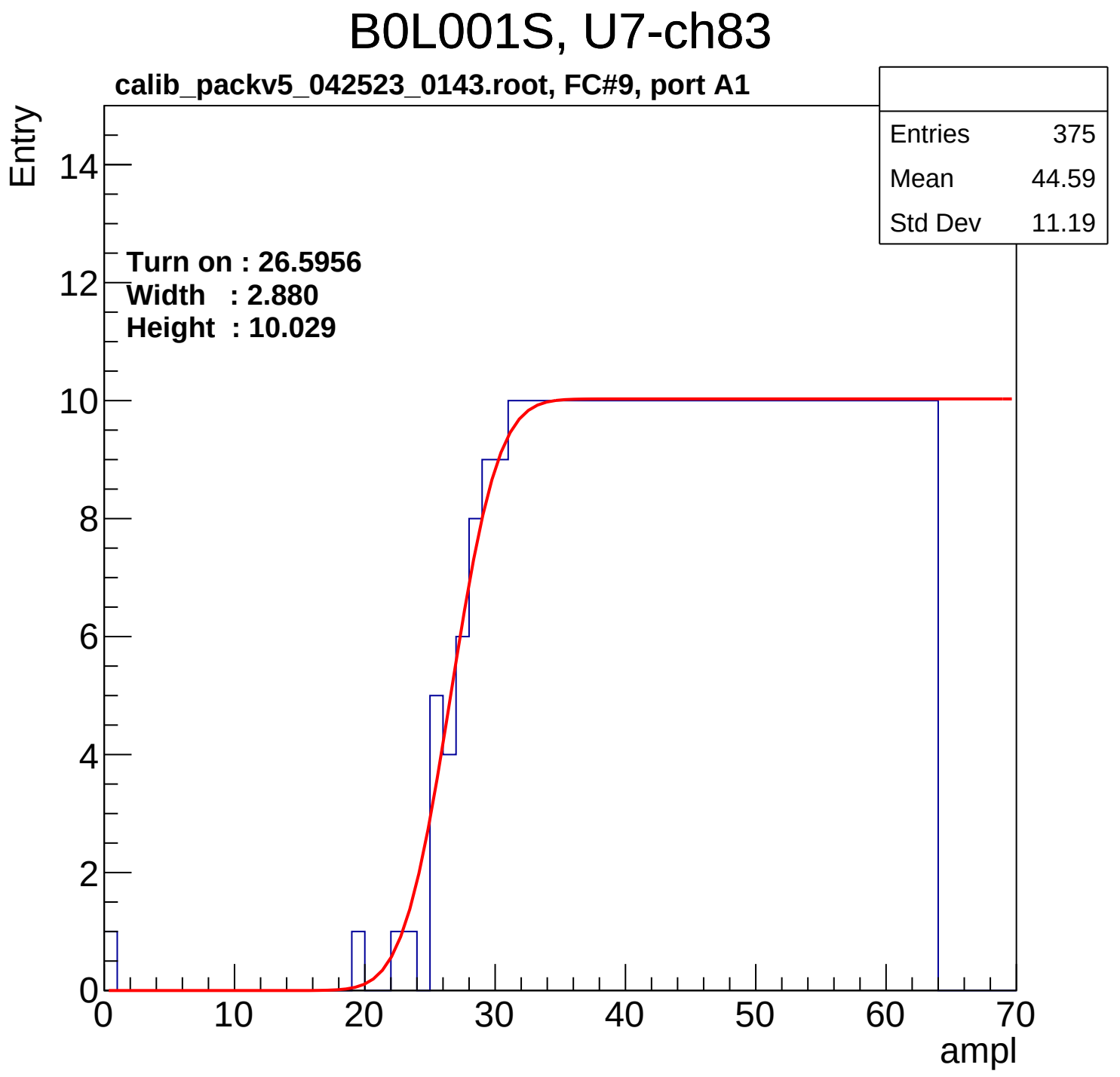
B0L001S, U7-ch83
calib_packv5_042523_0143.root, FC#9, port A1
Entries 375
Mean 44.59
Std Dev 11.19
Turn on : 26.5956
Width : 2.880
Height : 10.029
Entry
ampl
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4
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8
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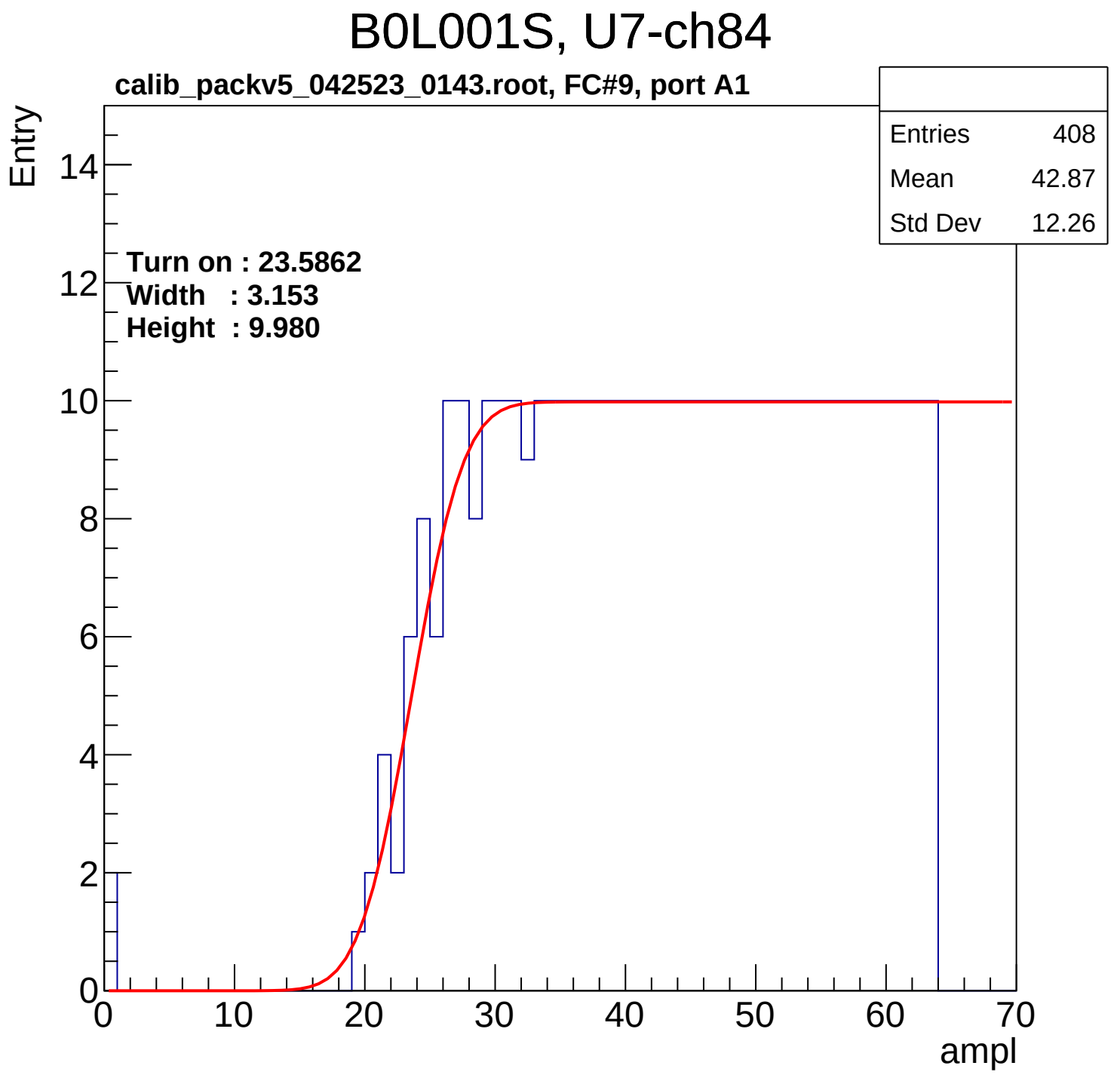
B0L001S, U7-ch84
calib_packv5_042523_0143.root, FC#9, port A1
Entries 408
Mean 42.87
Std Dev 12.26
Turn on : 23.5862
Width : 3.153
Height : 9.980
Entry
ampl
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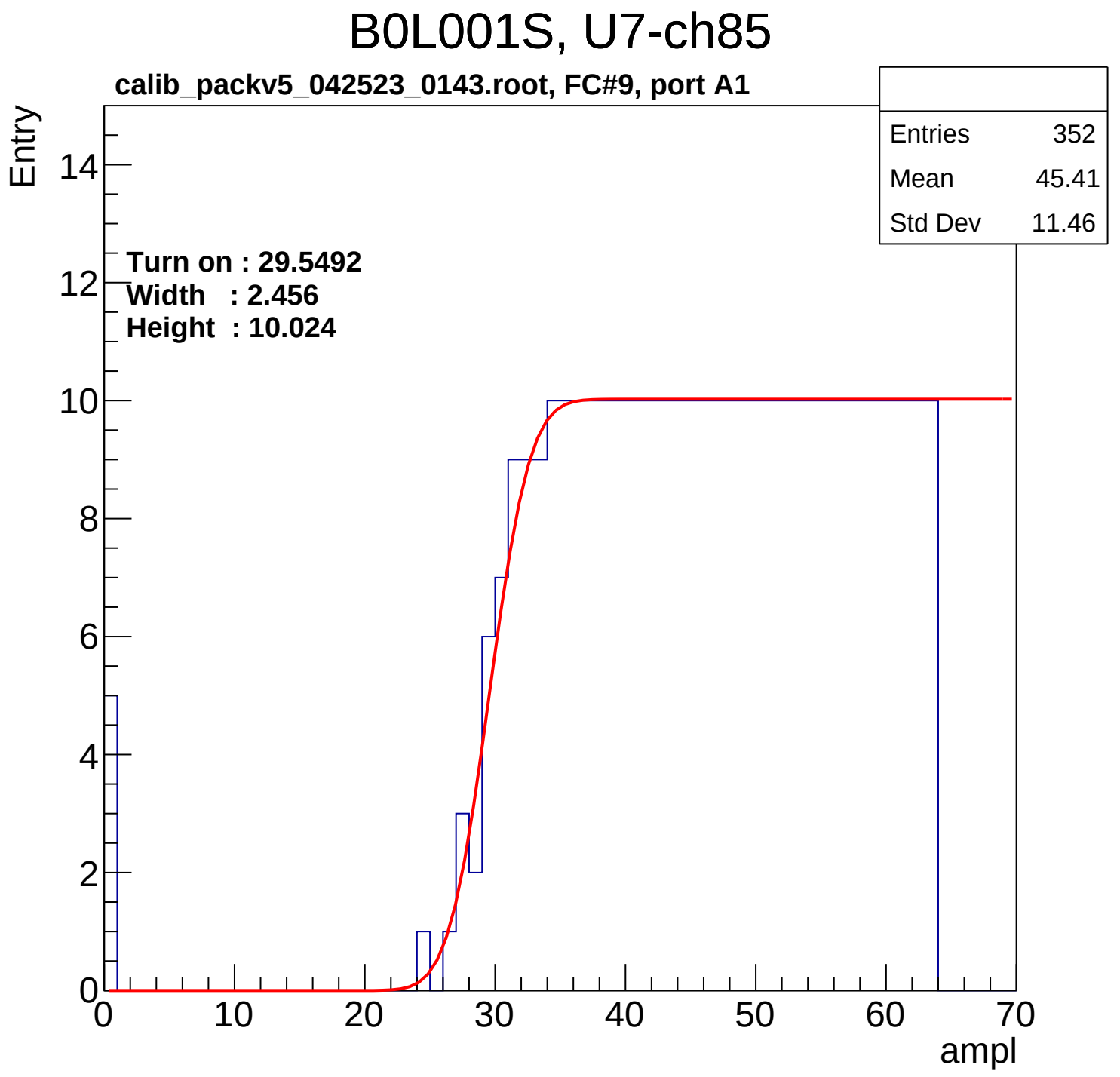
B0L001S, U7-ch85
calib_packv5_042523_0143.root, FC#9, port A1
Entries 352
Mean 45.41
Std Dev 11.46
Turn on : 29.5492
Width : 2.456
Height : 10.024
Entry
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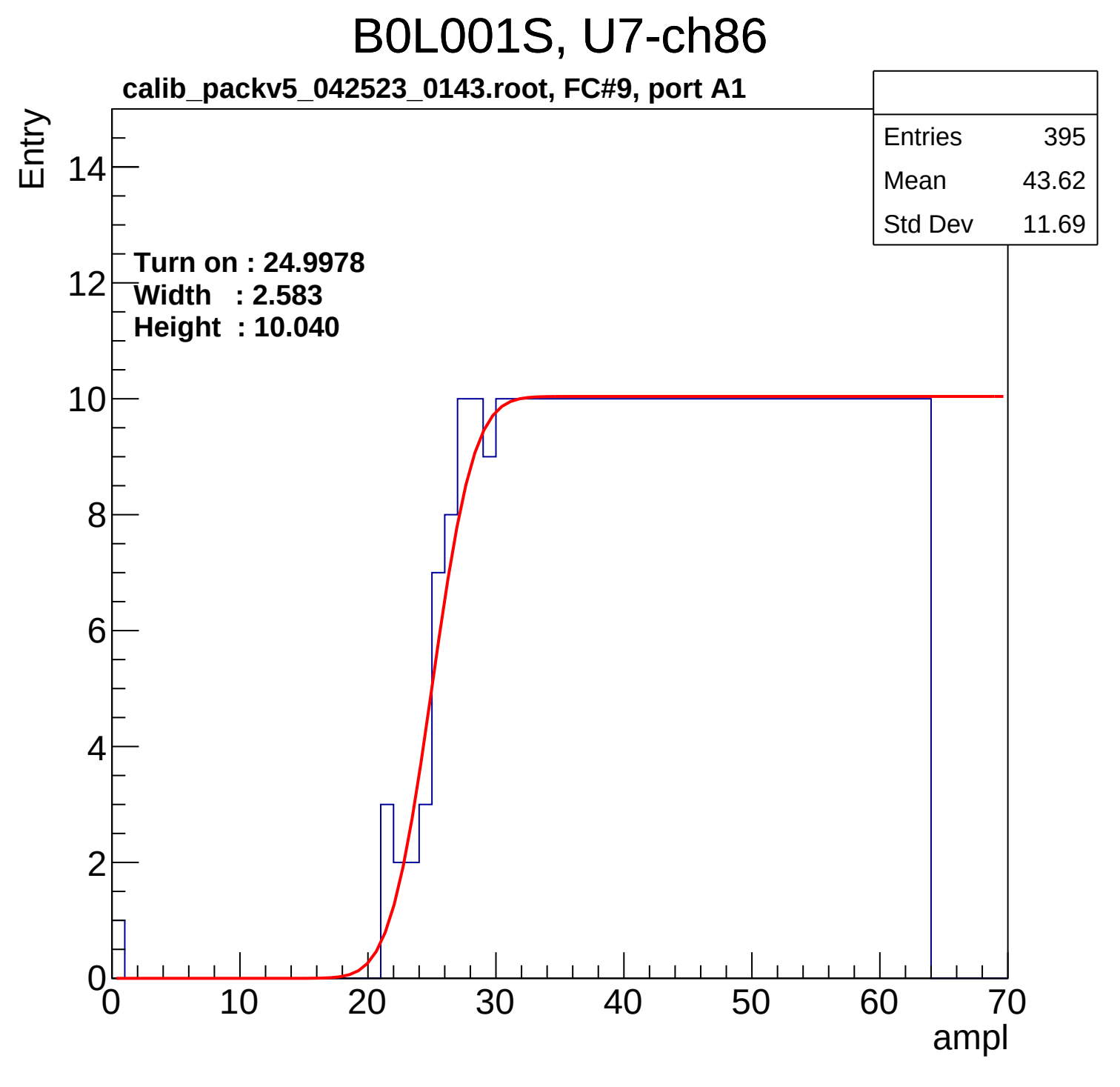
B0L001S, U7-ch86
calib_packv5_042523_0143.root, FC#9, port A1
Entries 395
Mean 43.62
Std Dev 11.69
Turn on : 24.9978
Width : 2.583
Height : 10.040
Entry
ampl
0
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4
6
8
10
12
14
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10
20
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40
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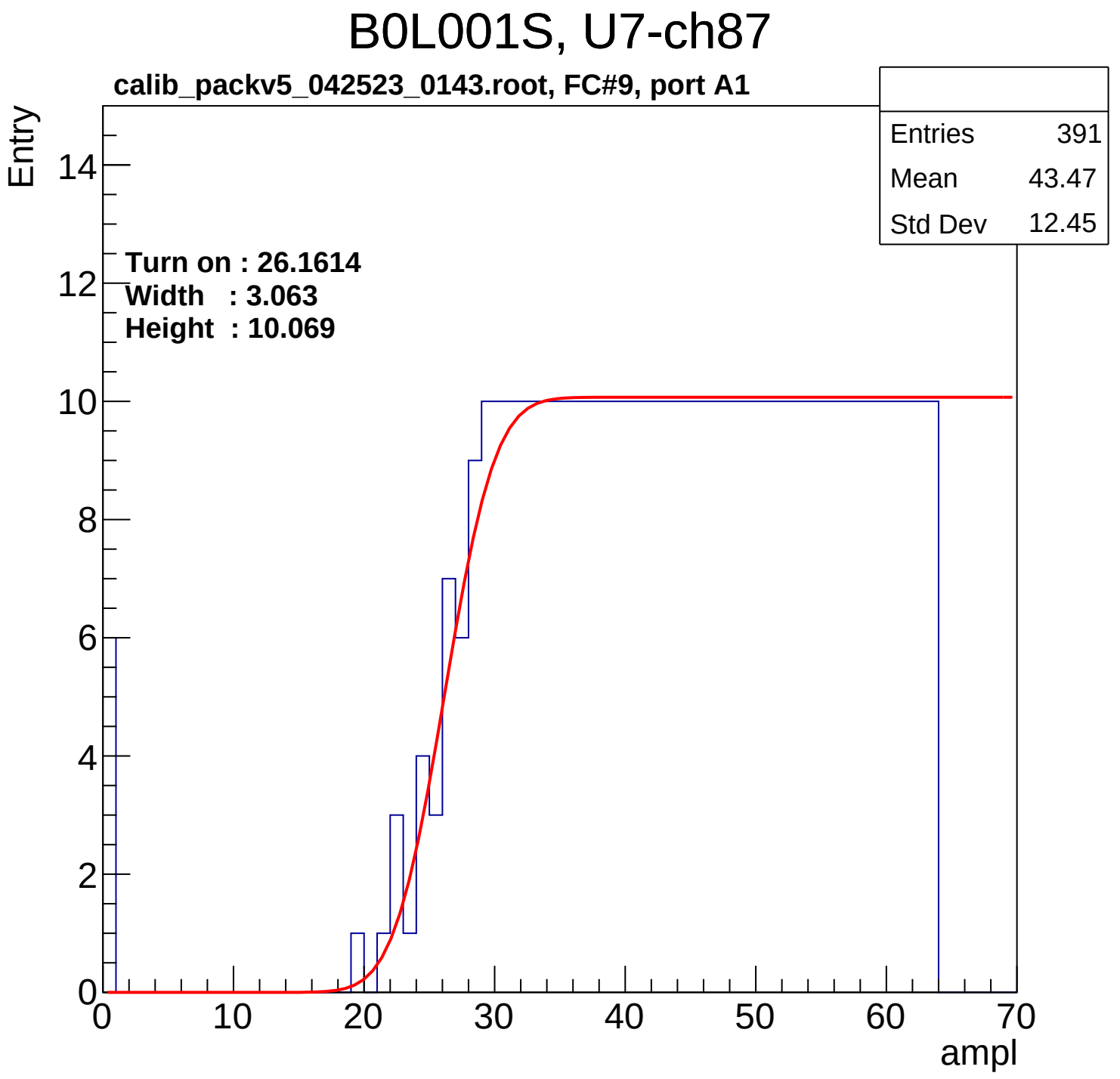
B0L001S, U7-ch87
calib_packv5_042523_0143.root, FC#9, port A1
Entries 391
Mean 43.47
Std Dev 12.45
Turn on : 26.1614
Width : 3.063
Height : 10.069
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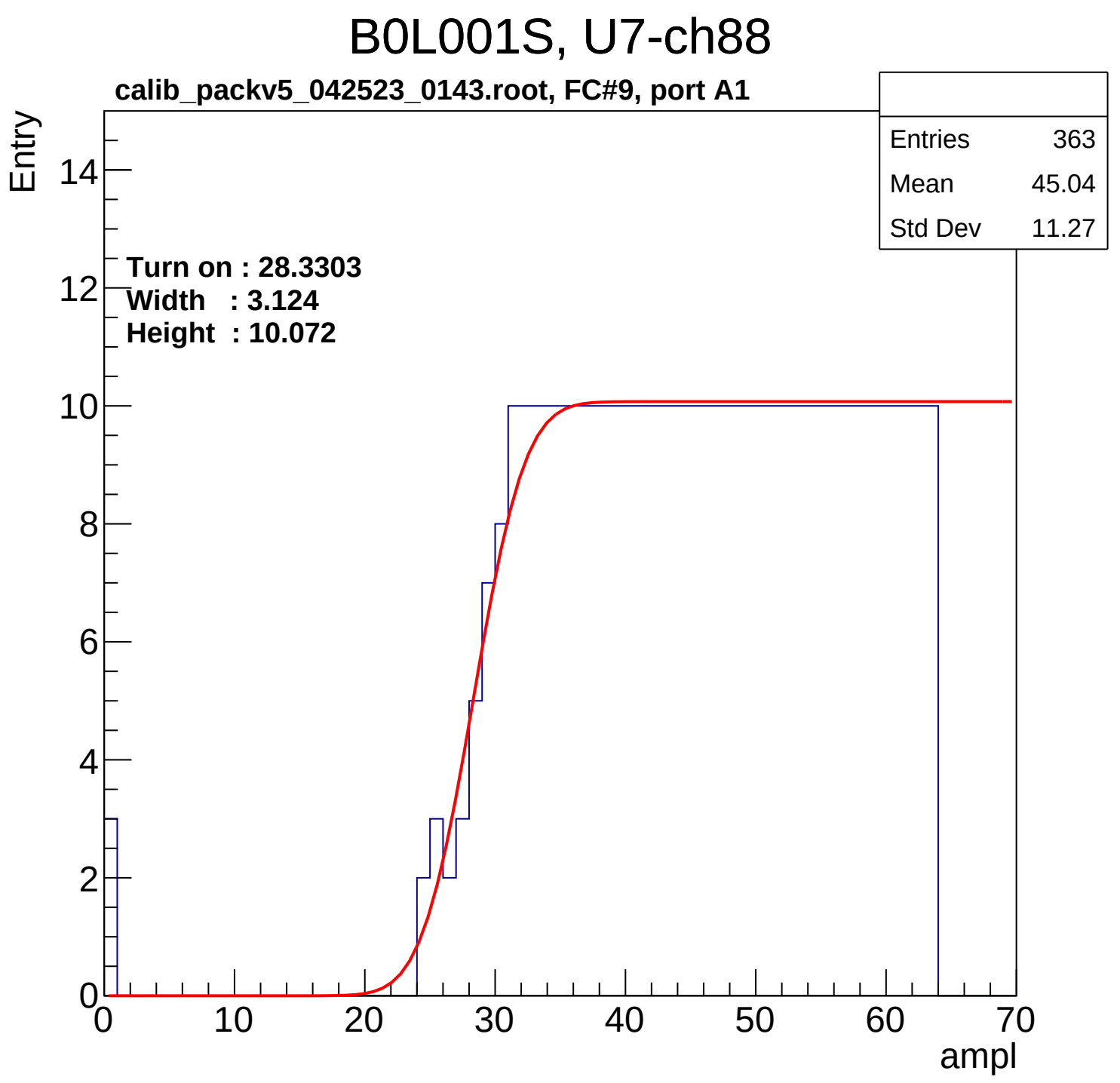
B0L001S, U7-ch88
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 45.04
Std Dev 11.27
Turn on : 28.3303
Width : 3.124
Height : 10.072
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ampl
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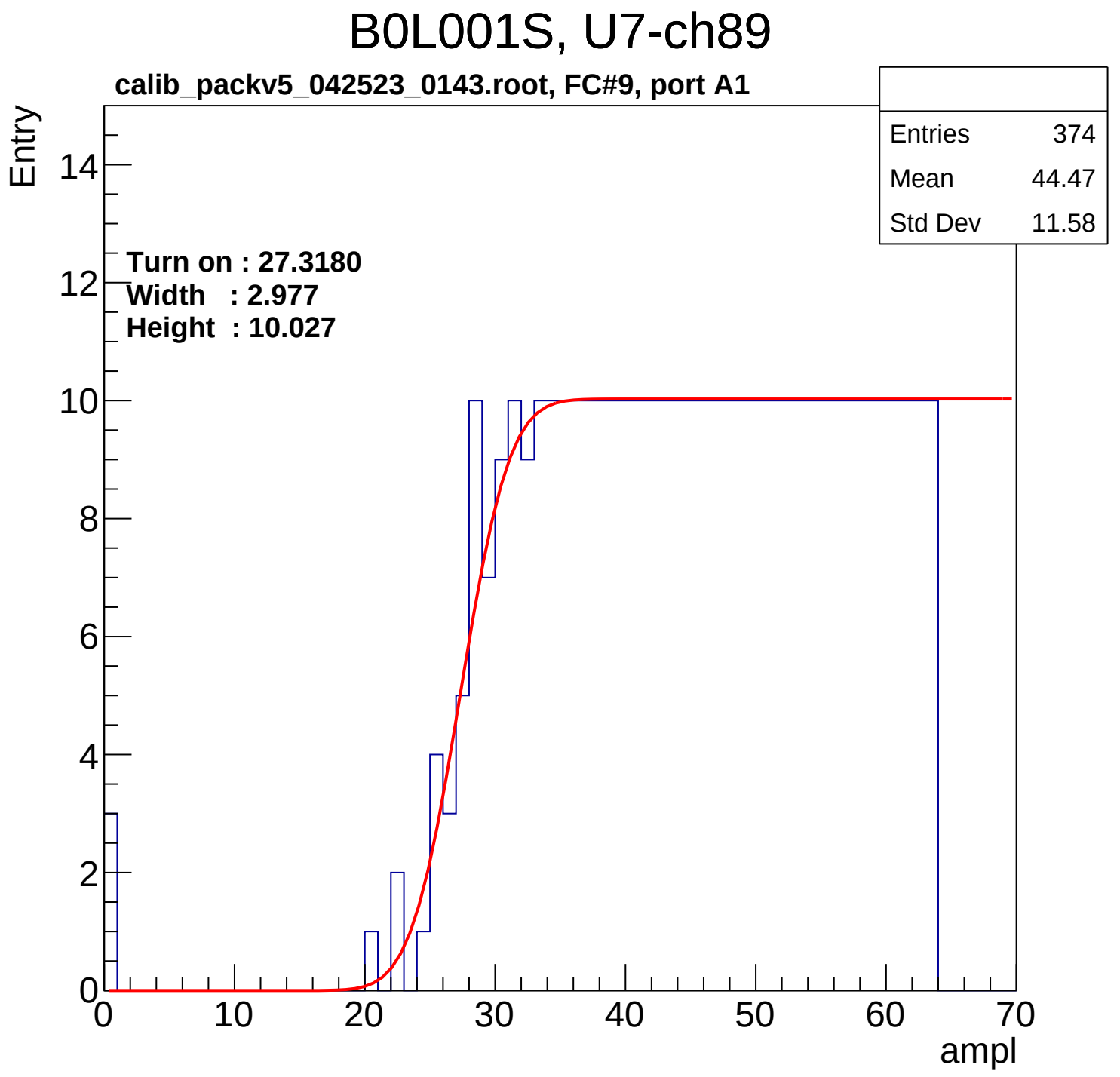
B0L001S, U7-ch89
calib_packv5_042523_0143.root, FC#9, port A1
Entries 374
Mean 44.47
Std Dev 11.58
Turn on : 27.3180
Width : 2.977
Height : 10.027
Entry
ampl
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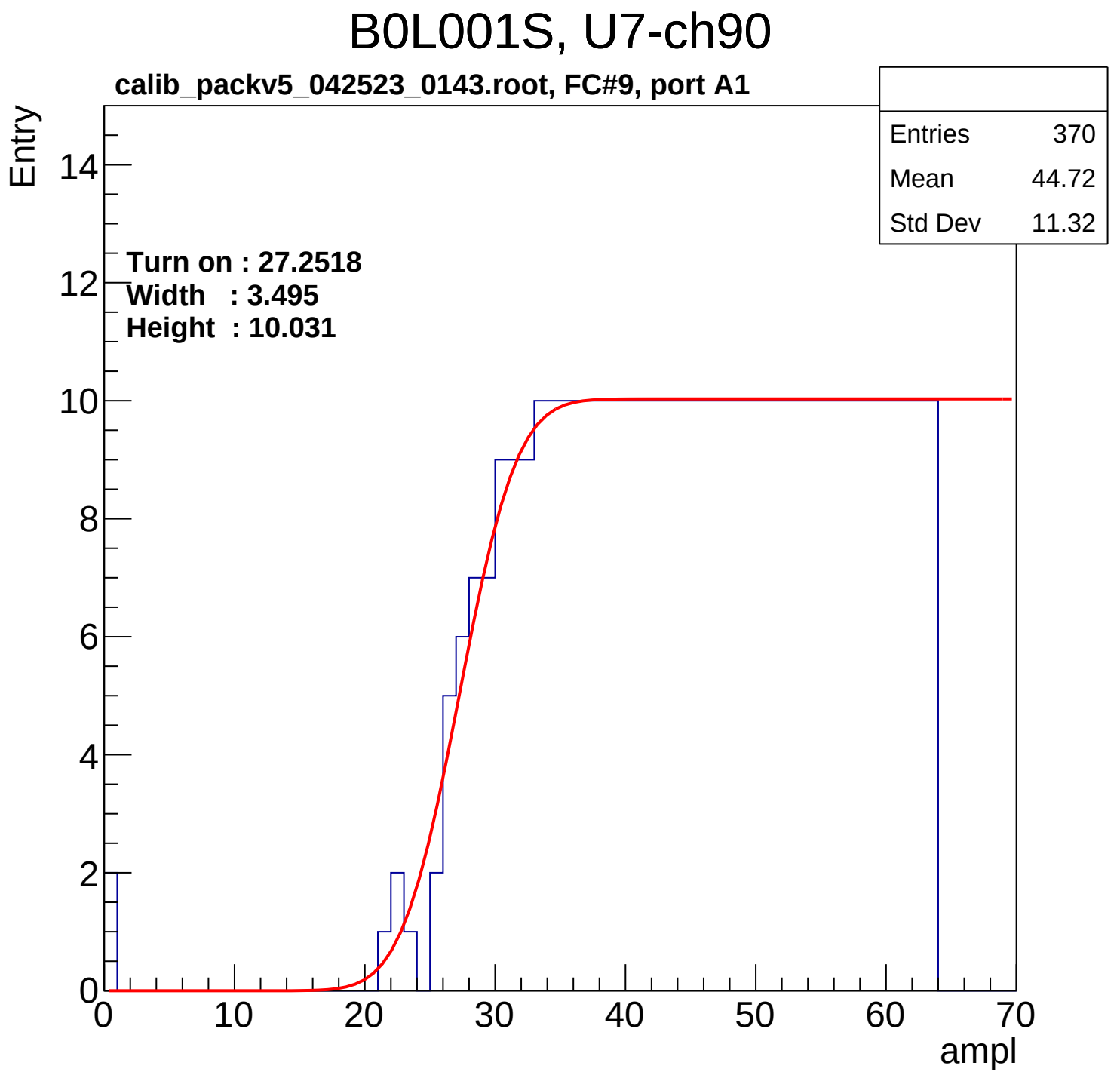
B0L001S, U7-ch90
calib_packv5_042523_0143.root, FC#9, port A1
Entries 370
Mean 44.72
Std Dev 11.32
Turn on : 27.2518
Width : 3.495
Height : 10.031
Entry
ampl
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2
4
6
8
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12
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0
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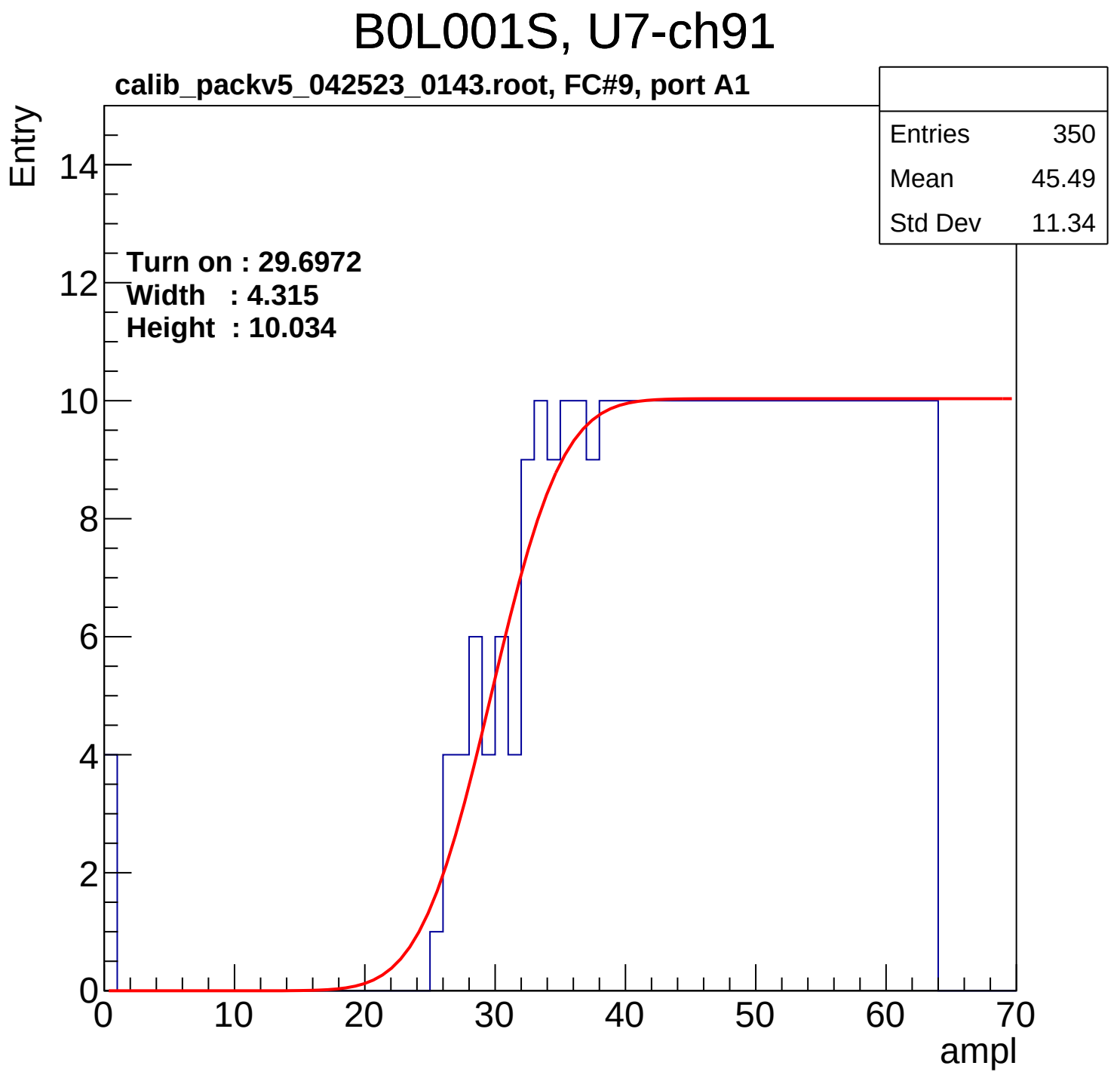
B0L001S, U7-ch91
calib_packv5_042523_0143.root, FC#9, port A1
Entries 350
Mean 45.49
Std Dev 11.34
Turn on : 29.6972
Width : 4.315
Height : 10.034
Entry
ampl
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2
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8
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0
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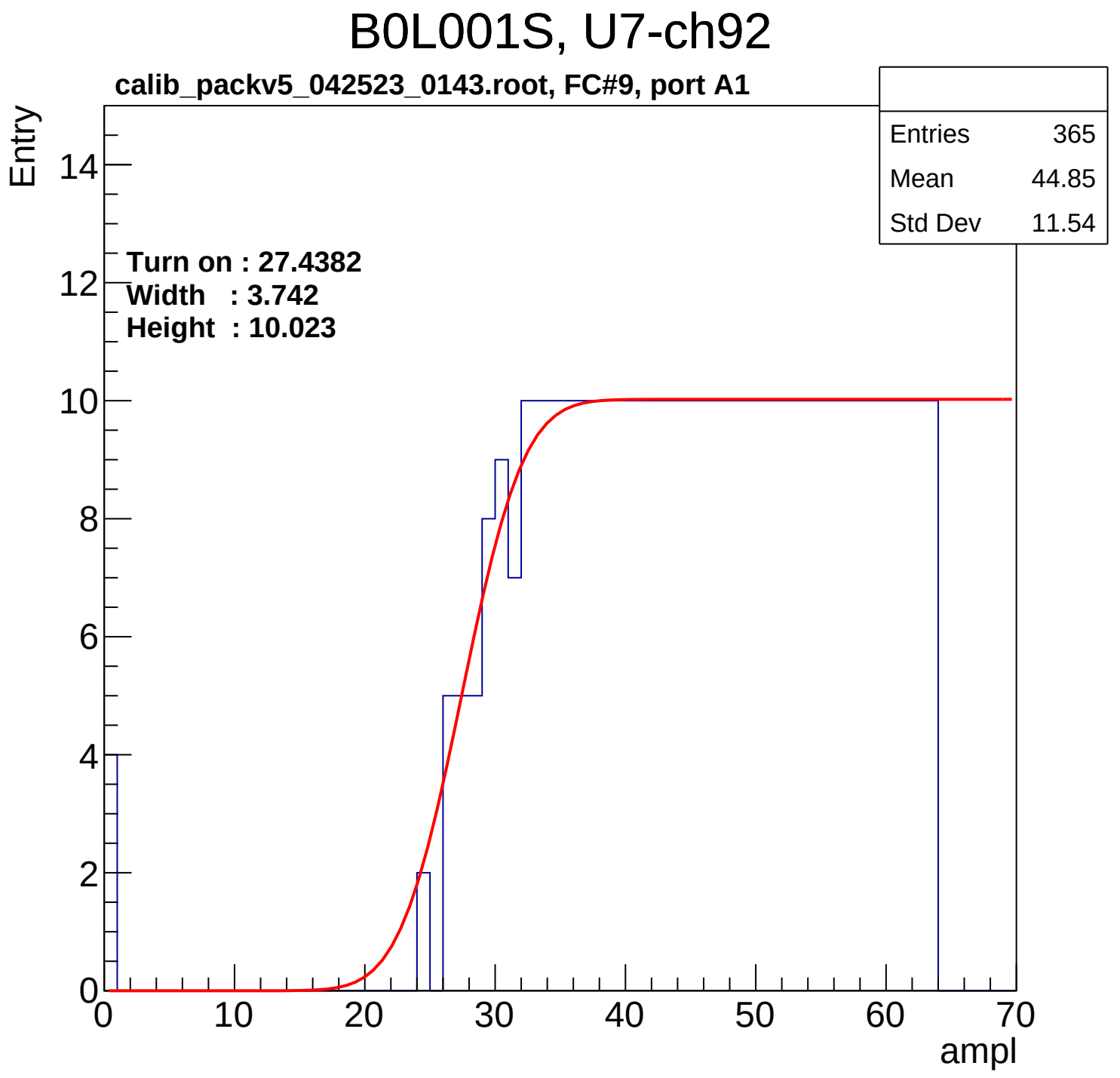
B0L001S, U7-ch92
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 44.85
Std Dev 11.54
Turn on : 27.4382
Width : 3.742
Height : 10.023
Entry
ampl
0
2
4
6
8
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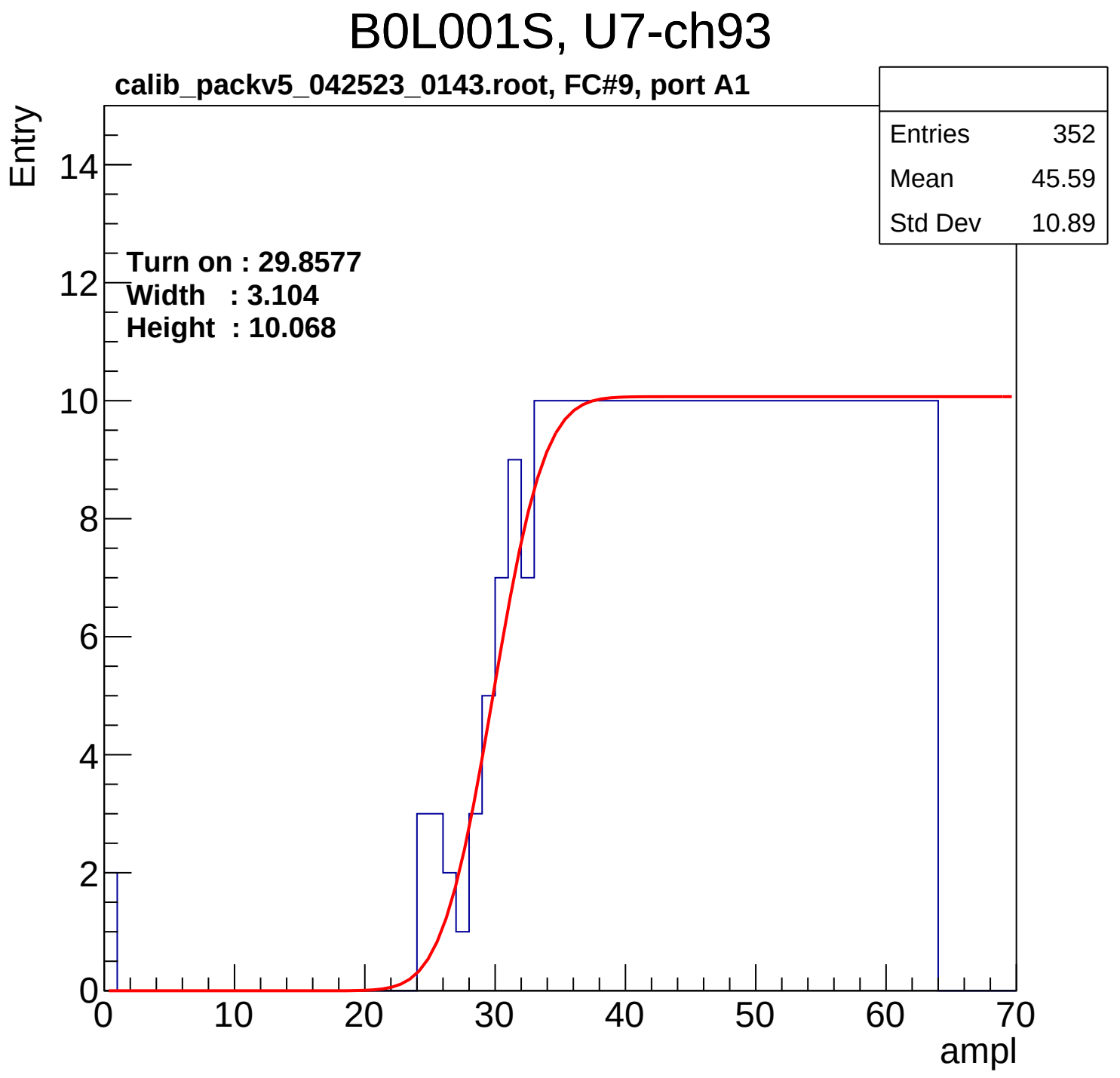
B0L001S, U7-ch93
calib_packv5_042523_0143.root, FC#9, port A1
Entries 352
Mean 45.59
Std Dev 10.89
Turn on : 29.8577
Width : 3.104
Height : 10.068
Entry
ampl
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6
8
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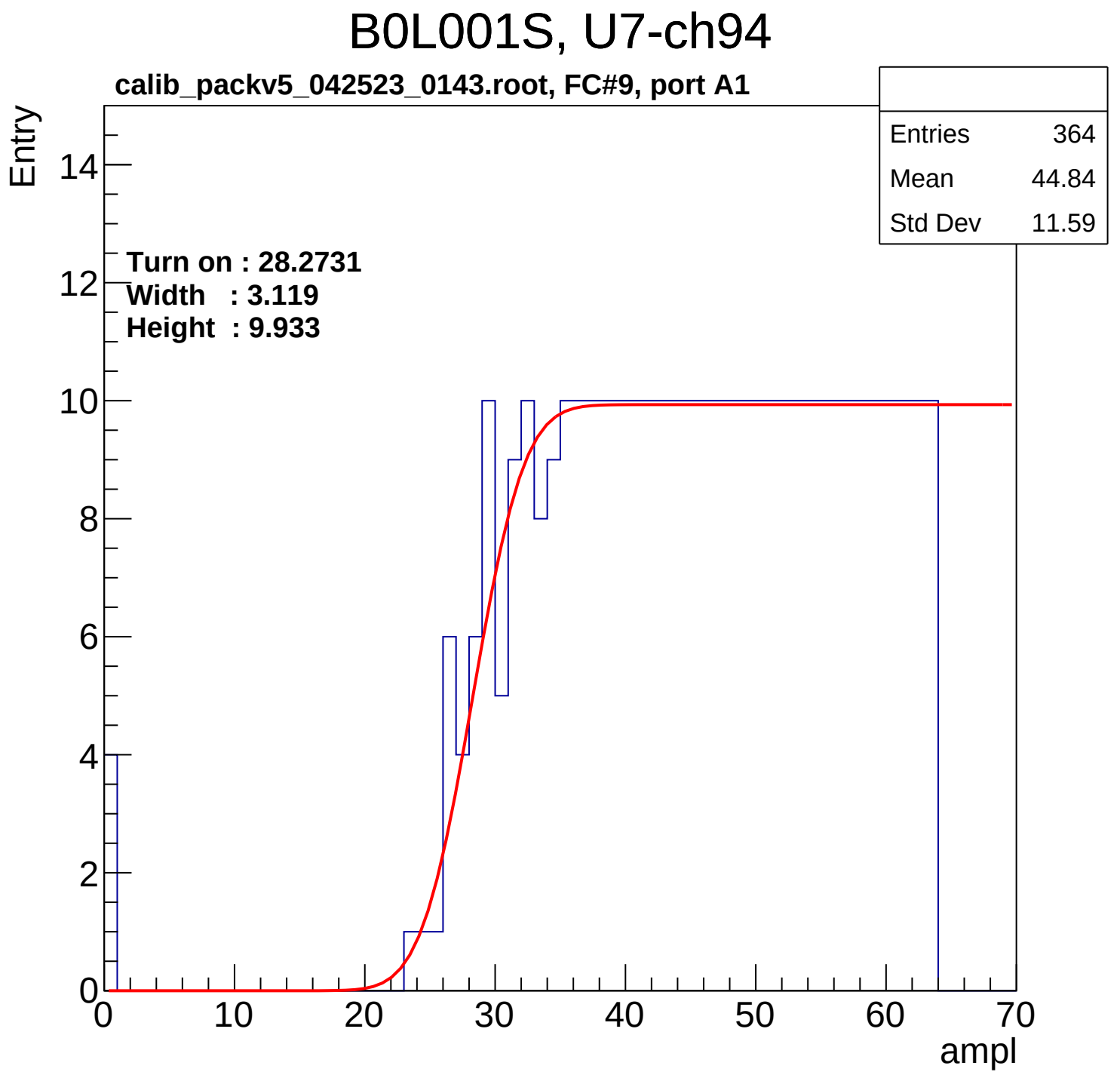
B0L001S, U7-ch94
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 44.84
Std Dev 11.59
Turn on : 28.2731
Width : 3.119
Height : 9.933
Entry
ampl
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2
4
6
8
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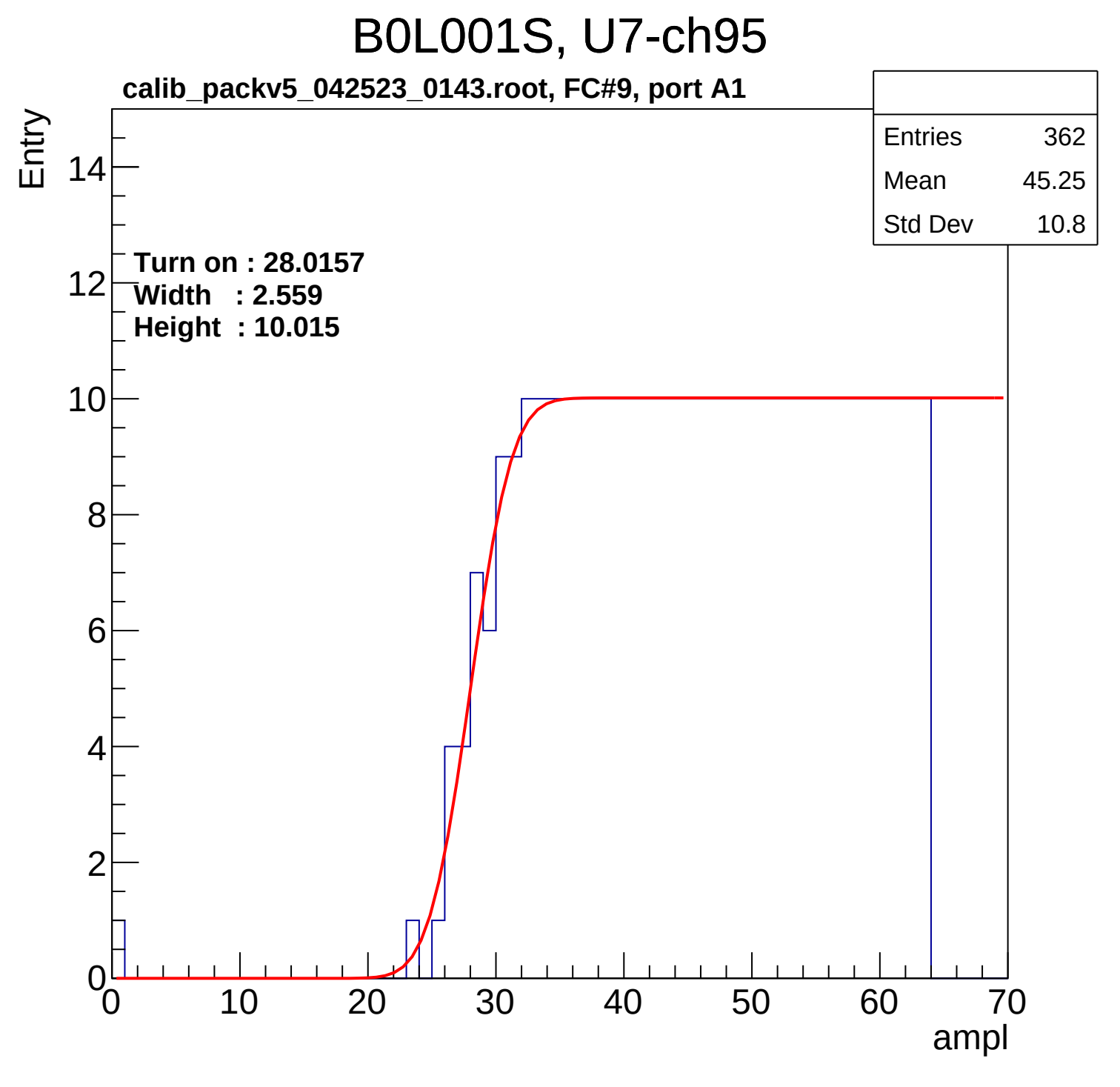
B0L001S, U7-ch95
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 45.25
Std Dev 10.8
Turn on : 28.0157
Width : 2.559
Height : 10.015
Entry
ampl
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6
8
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0
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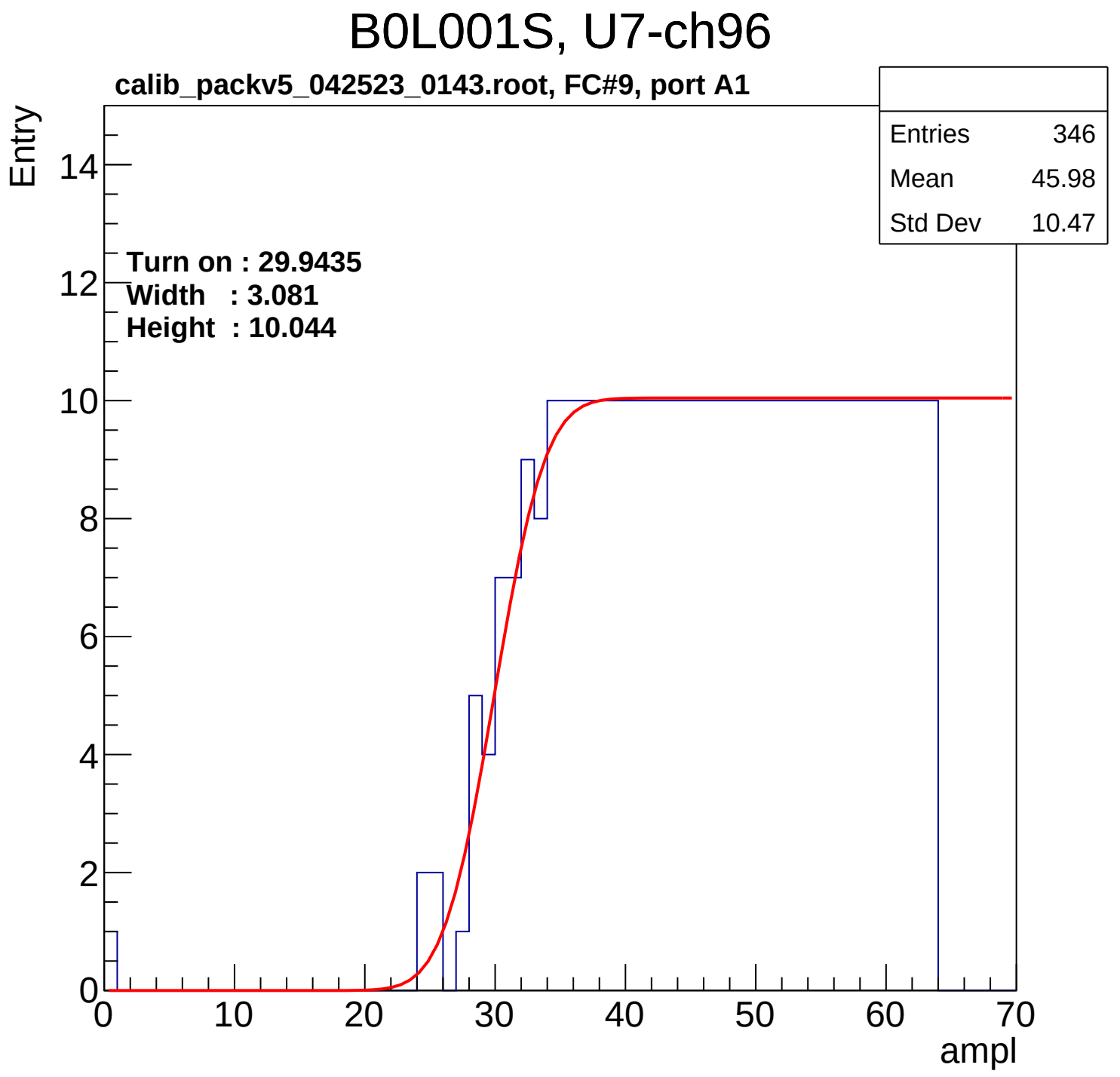
B0L001S, U7-ch96
calib_packv5_042523_0143.root, FC#9, port A1
Entries 346
Mean 45.98
Std Dev 10.47
Turn on : 29.9435
Width : 3.081
Height : 10.044
Entry
ampl
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6
8
10
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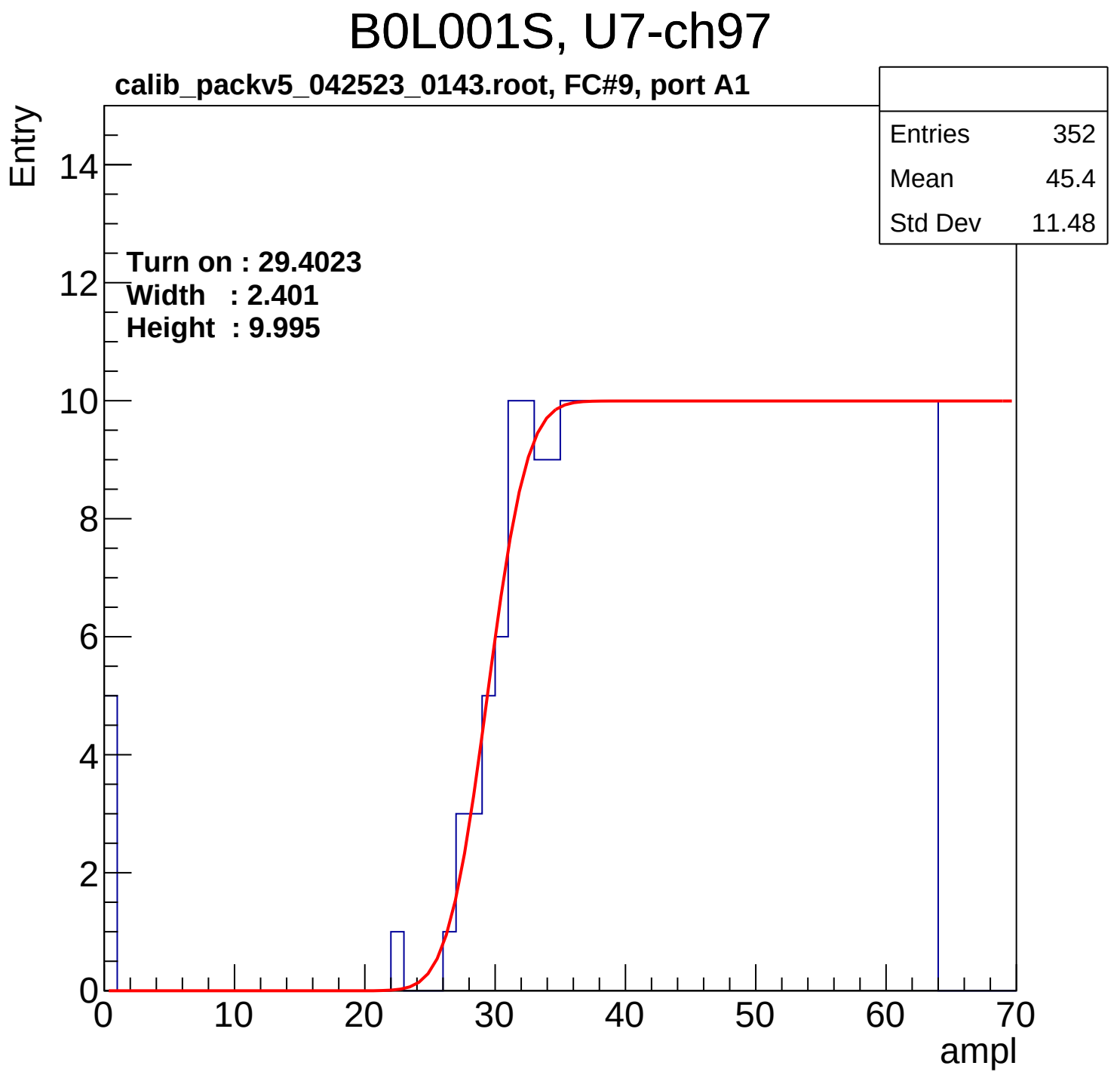
B0L001S, U7-ch97
calib_packv5_042523_0143.root, FC#9, port A1
Entries 352
Mean 45.4
Std Dev 11.48
Turn on : 29.4023
Width : 2.401
Height : 9.995
Entry
ampl
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4
6
8
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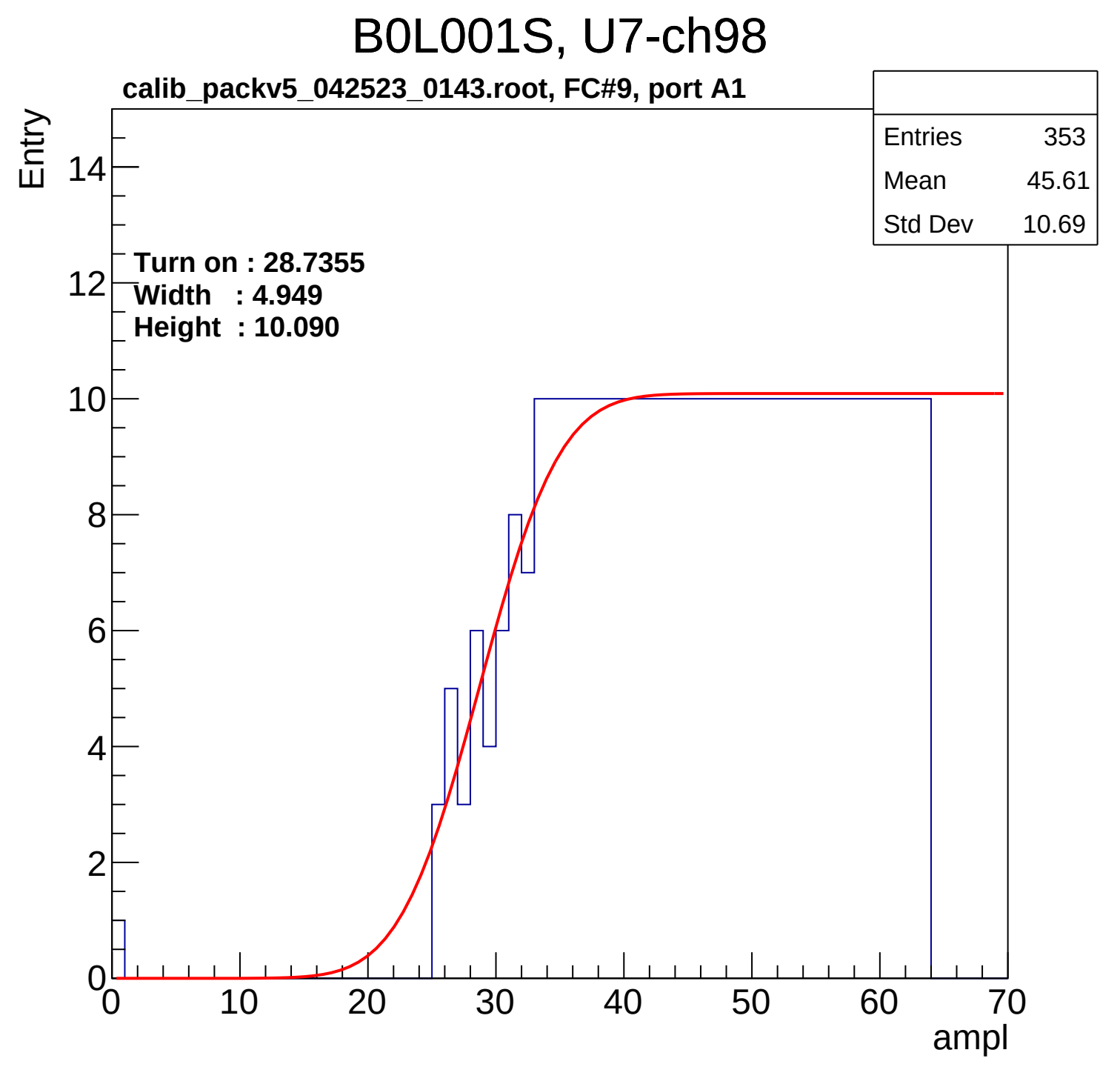
B0L001S, U7-ch98
calib_packv5_042523_0143.root, FC#9, port A1
Entries 353
Mean 45.61
Std Dev 10.69
Turn on : 28.7355
Width : 4.949
Height : 10.090
Entry
ampl
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6
8
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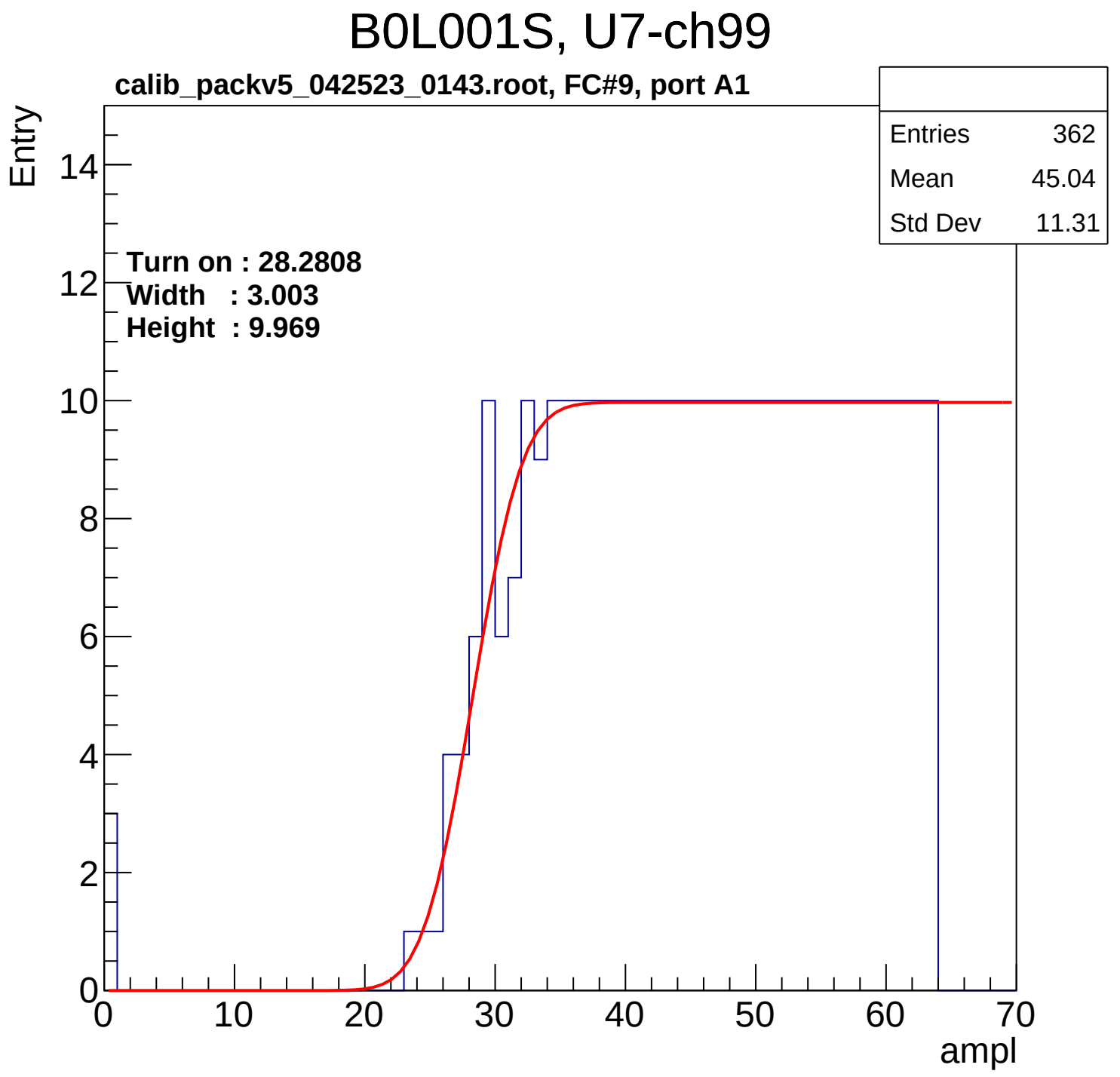
B0L001S, U7-ch99
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 45.04
Std Dev 11.31
Turn on : 28.2808
Width : 3.003
Height : 9.969
Entry
ampl
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6
8
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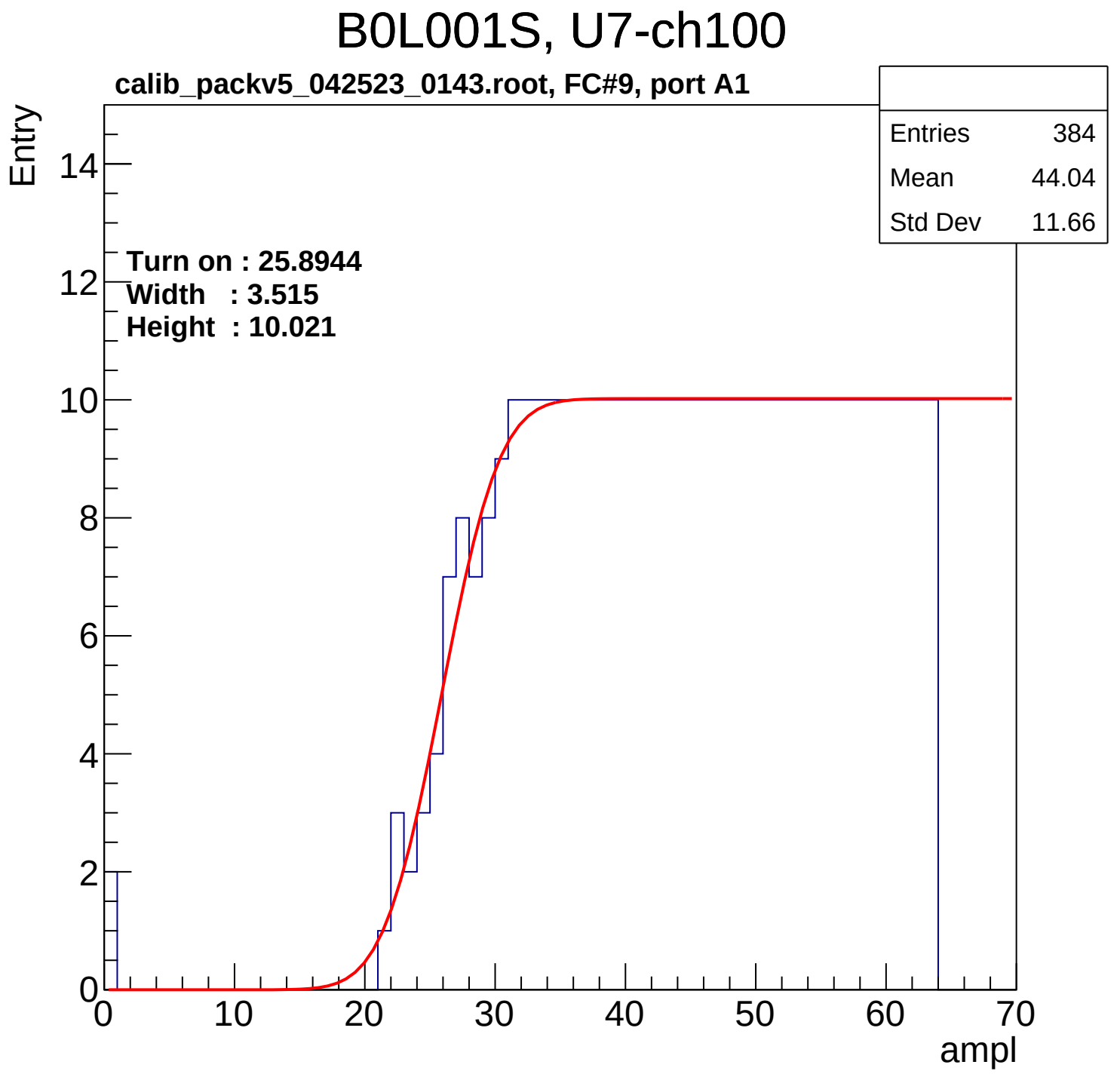
B0L001S, U7-ch100
calib_packv5_042523_0143.root, FC#9, port A1
Entries 384
Mean 44.04
Std Dev 11.66
Turn on : 25.8944
Width : 3.515
Height : 10.021
Entry
ampl
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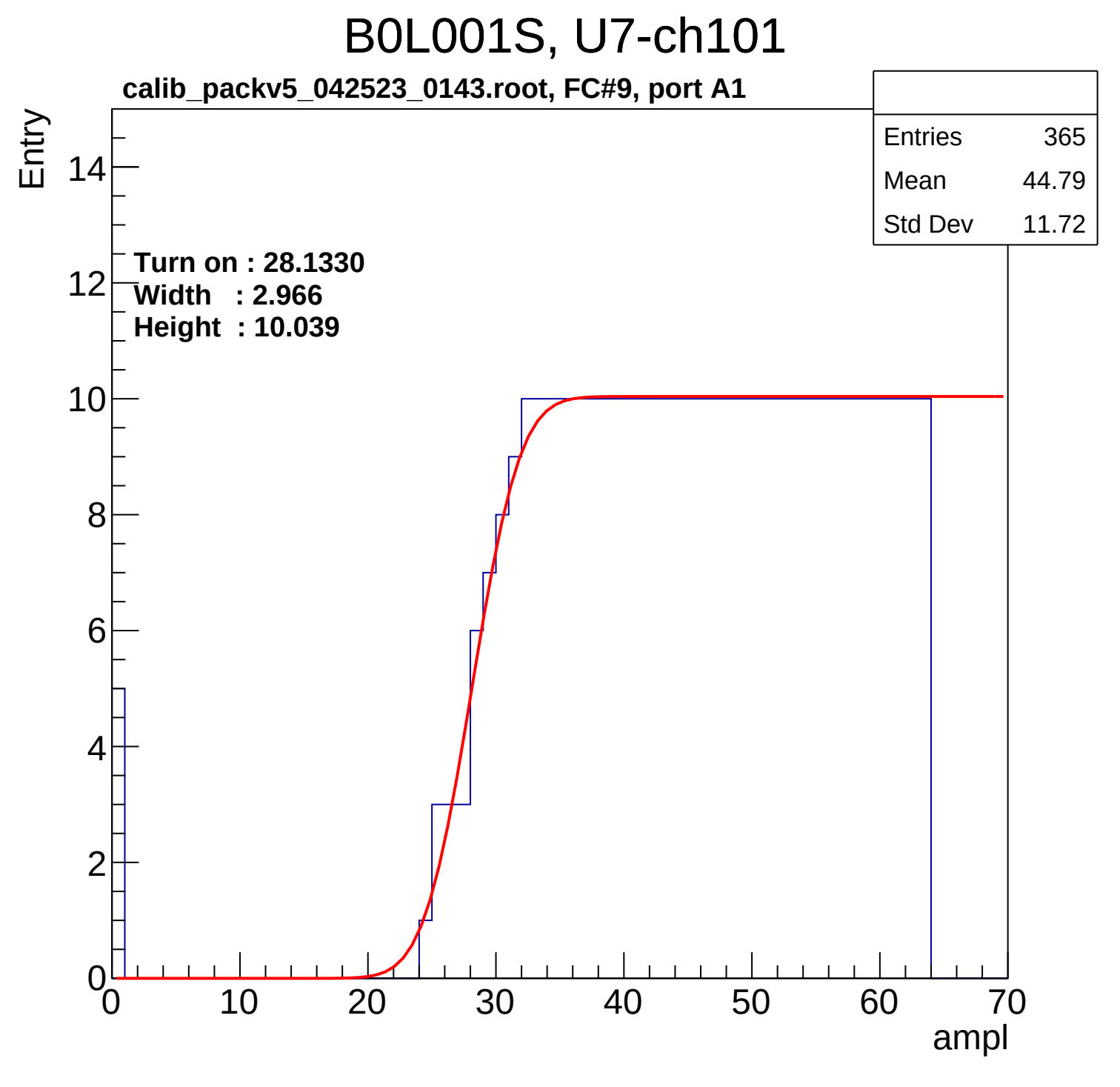
B0L001S, U7-ch101
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 44.79
Std Dev 11.72
Turn on : 28.1330
Width : 2.966
Height : 10.039
Entry
ampl
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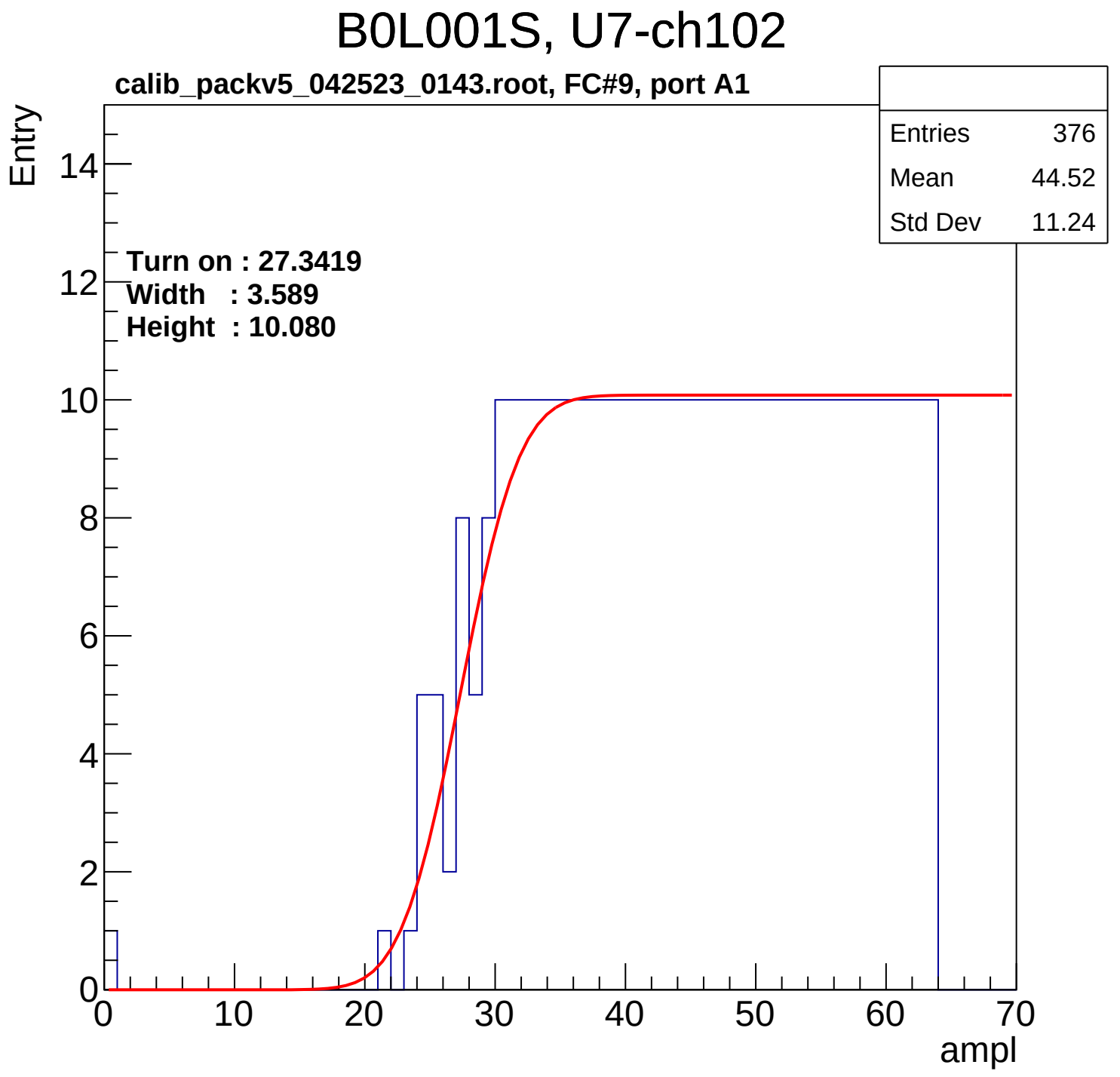
B0L001S, U7-ch102
calib_packv5_042523_0143.root, FC#9, port A1
Entries 376
Mean 44.52
Std Dev 11.24
Turn on : 27.3419
Width : 3.589
Height : 10.080
Entry
ampl
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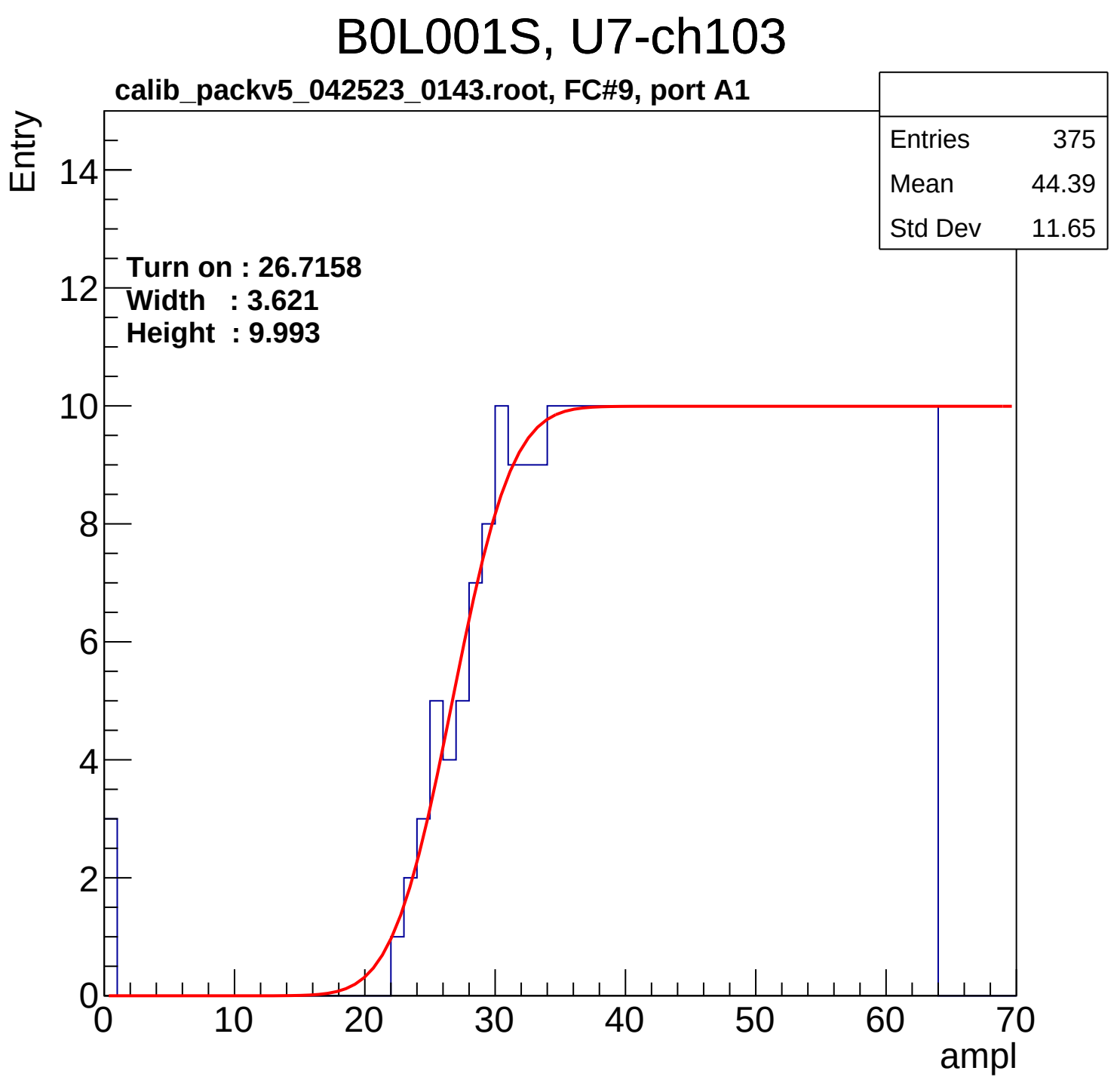
B0L001S, U7-ch103
calib_packv5_042523_0143.root, FC#9, port A1
Entries 375
Mean 44.39
Std Dev 11.65
Turn on : 26.7158
Width : 3.621
Height : 9.993
Entry
ampl
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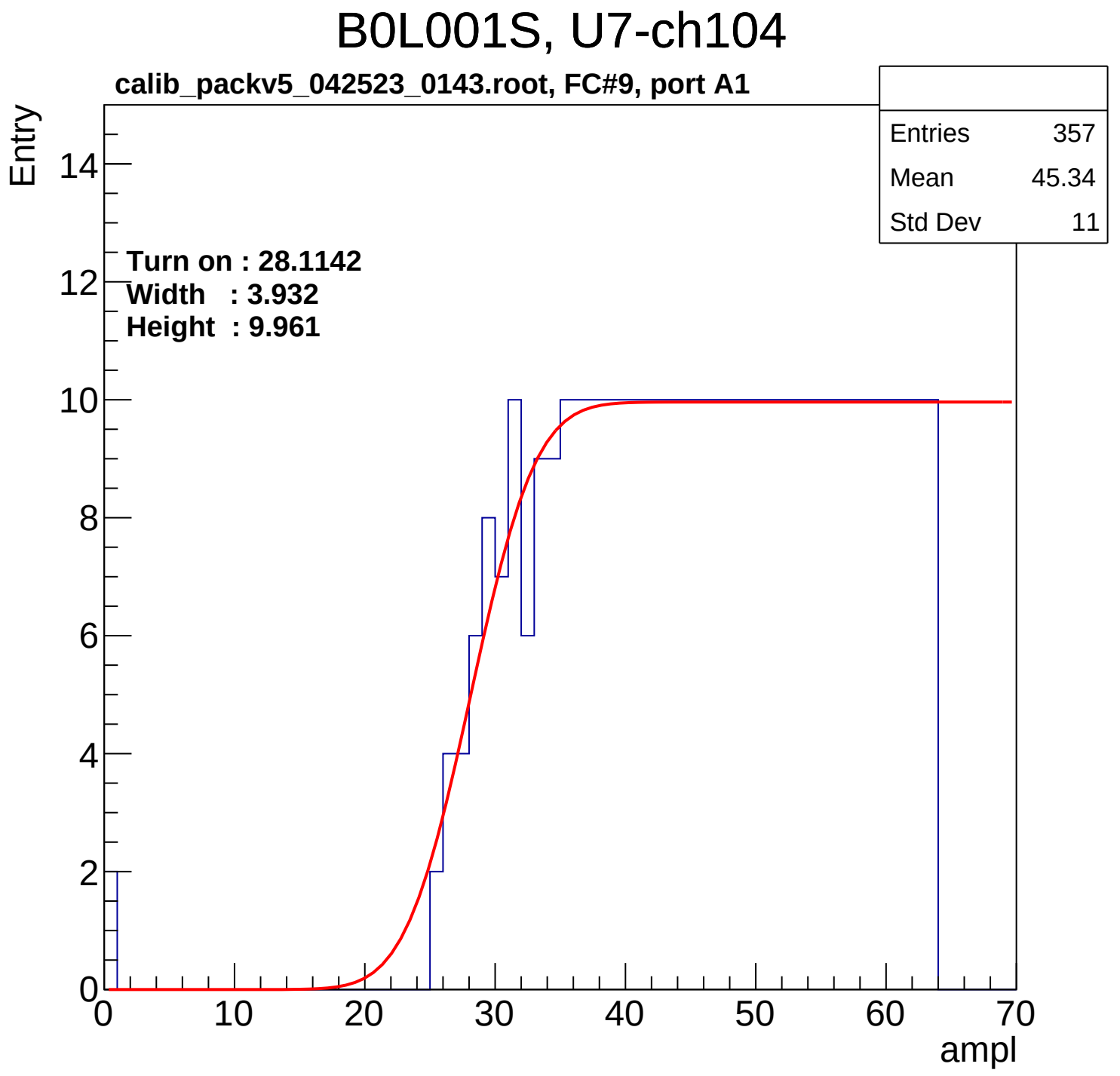
B0L001S, U7-ch104
calib_packv5_042523_0143.root, FC#9, port A1
Entries 357
Mean 45.34
Std Dev 11
Turn on : 28.1142
Width : 3.932
Height : 9.961
Entry
ampl
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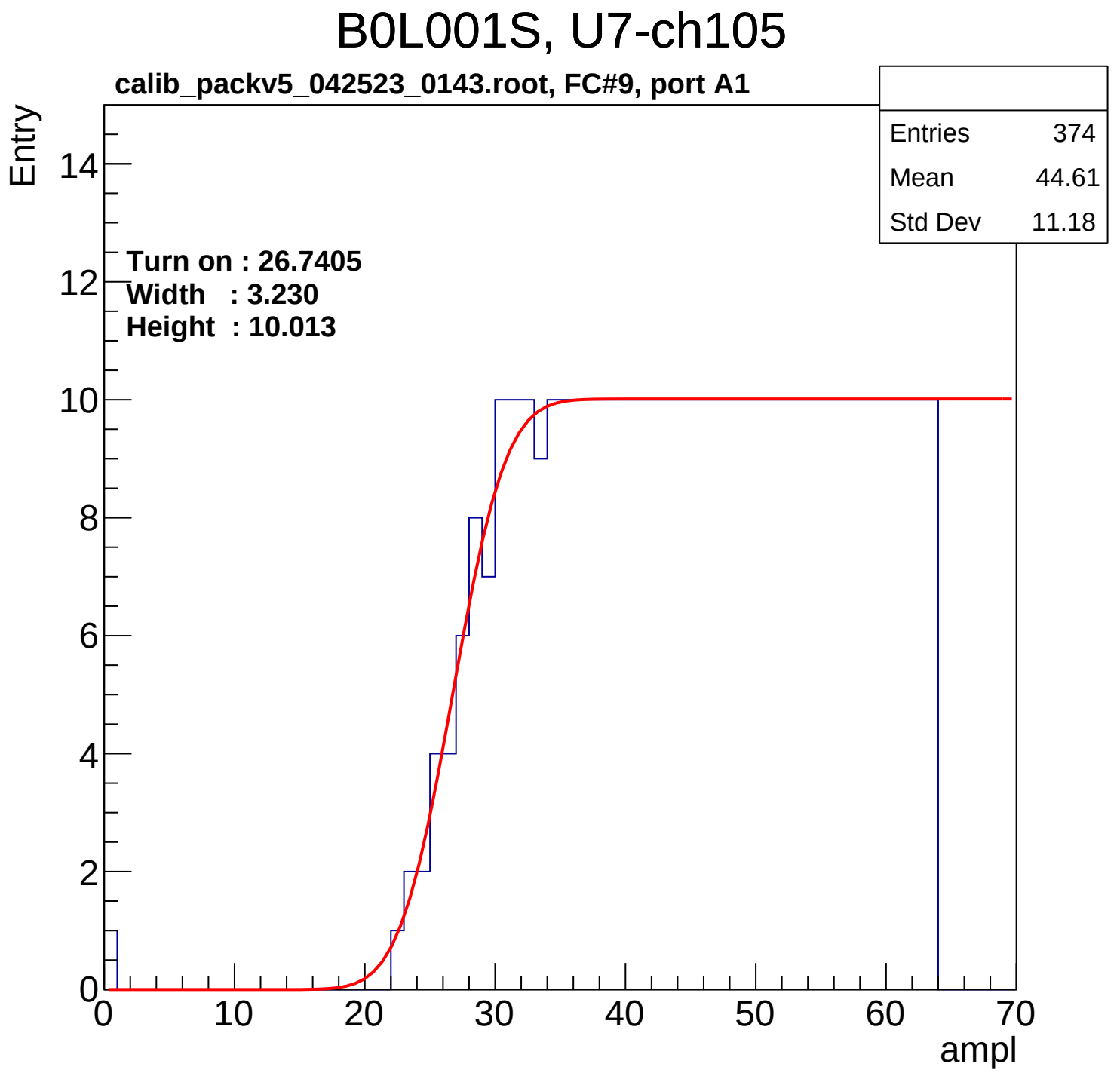
B0L001S, U7-ch105
calib_packv5_042523_0143.root, FC#9, port A1
Entries 374
Mean 44.61
Std Dev 11.18
Turn on : 26.7405
Width : 3.230
Height : 10.013
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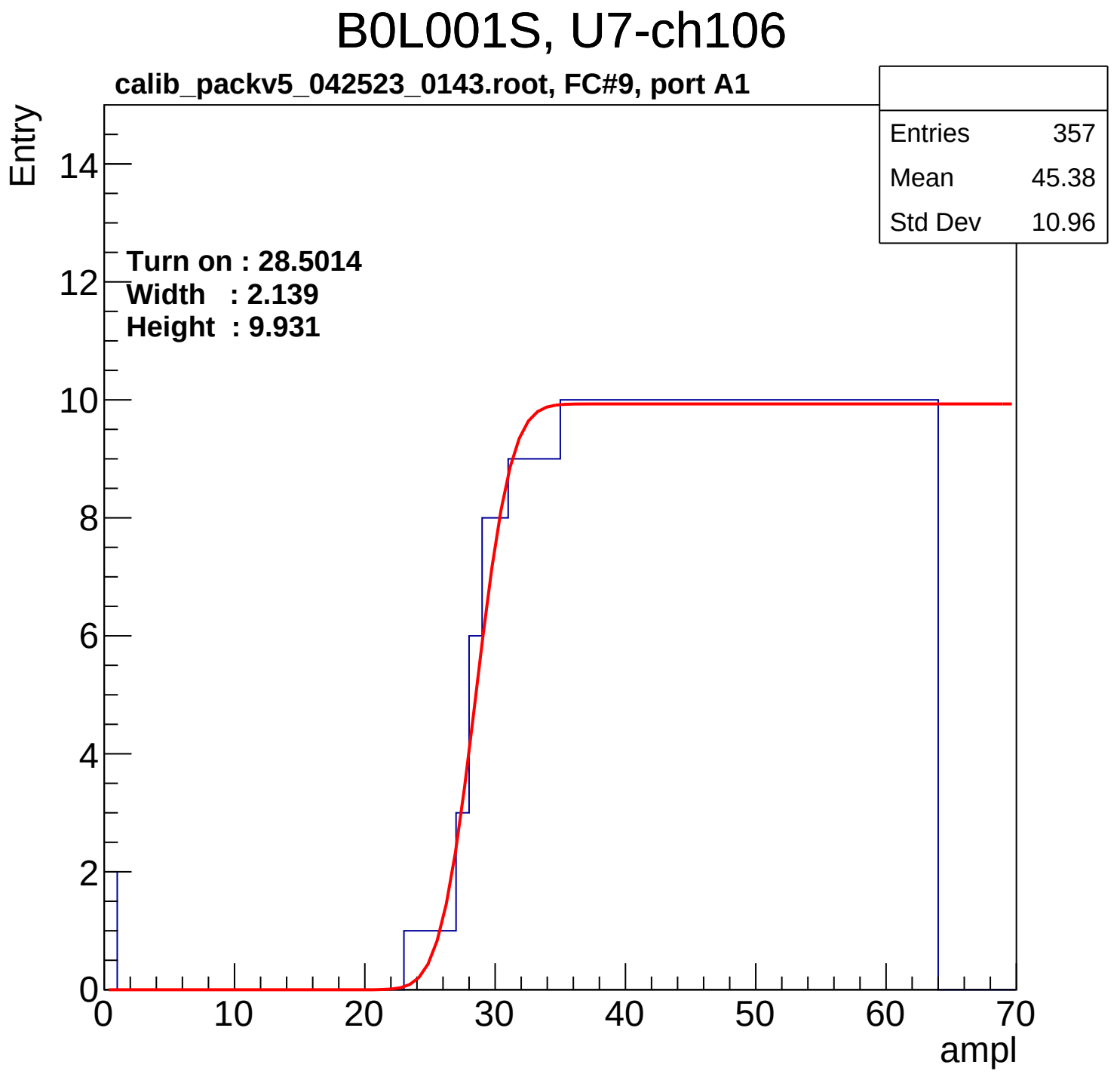
B0L001S, U7-ch106
calib_packv5_042523_0143.root, FC#9, port A1
Entries 357
Mean 45.38
Std Dev 10.96
Turn on : 28.5014
Width : 2.139
Height : 9.931
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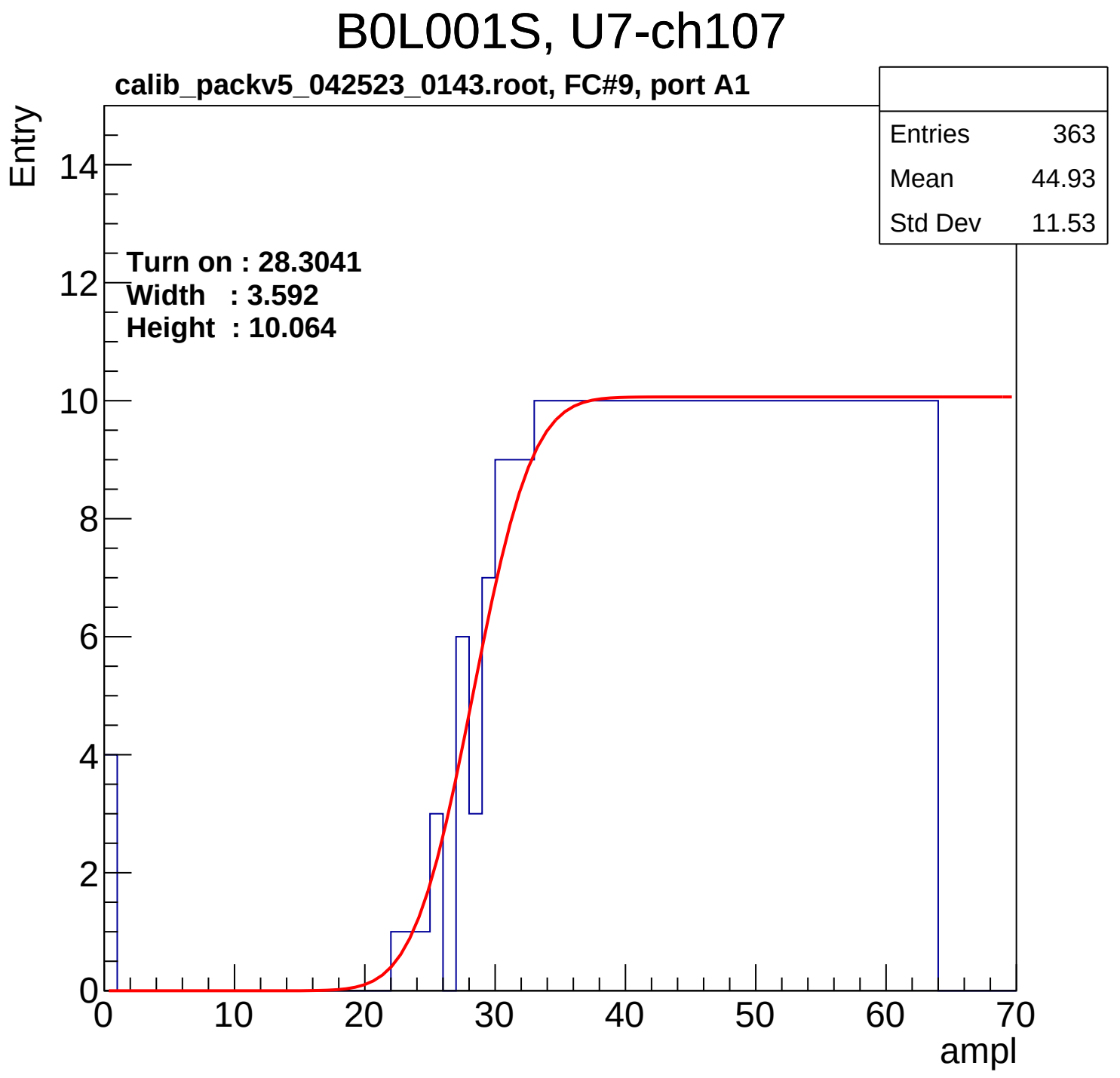
B0L001S, U7-ch107
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 44.93
Std Dev 11.53
Turn on : 28.3041
Width : 3.592
Height : 10.064
Entry
ampl
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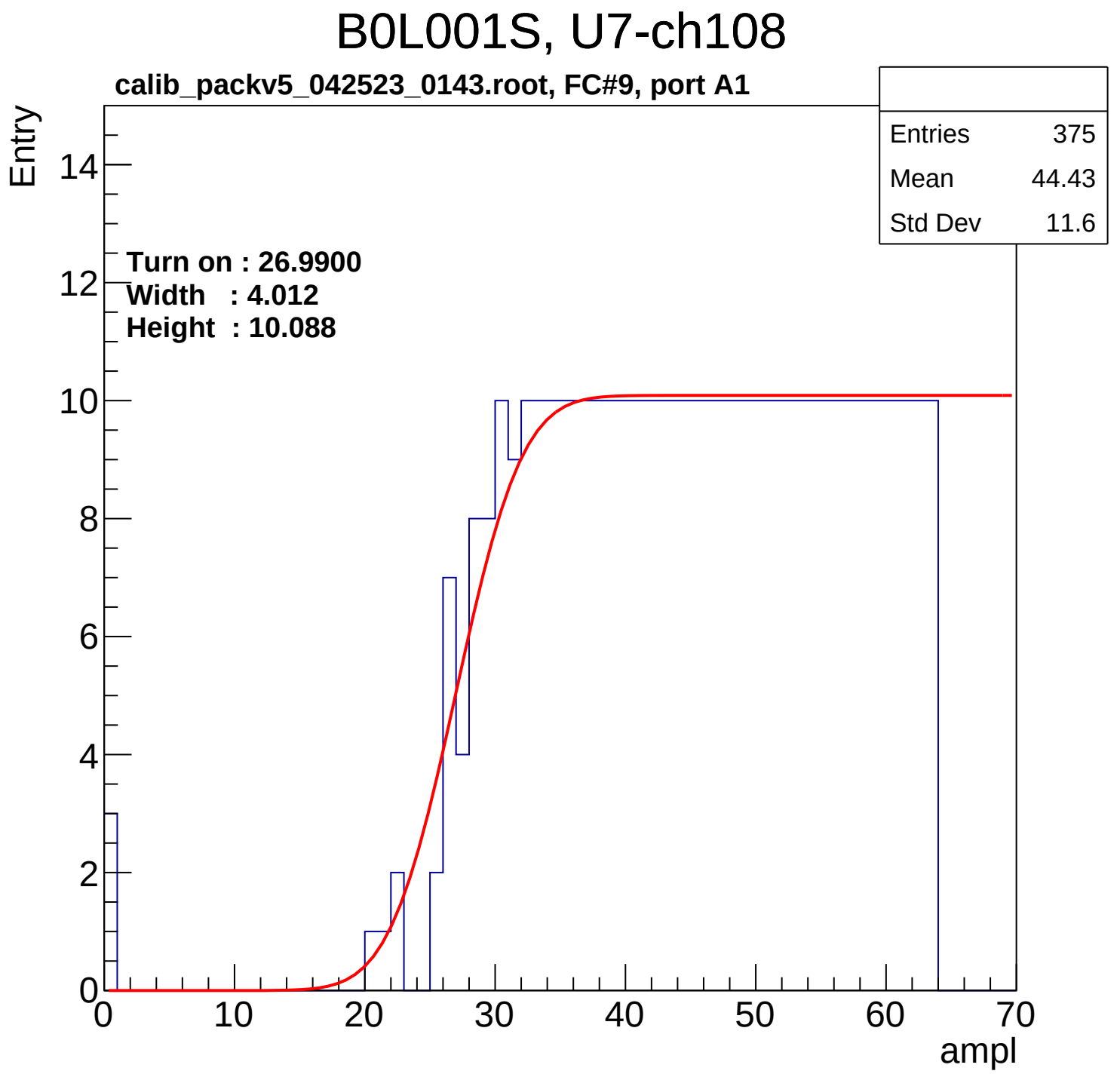
B0L001S, U7-ch108
calib_packv5_042523_0143.root, FC#9, port A1
Entries 375
Mean 44.43
Std Dev 11.6
Turn on : 26.9900
Width : 4.012
Height : 10.088
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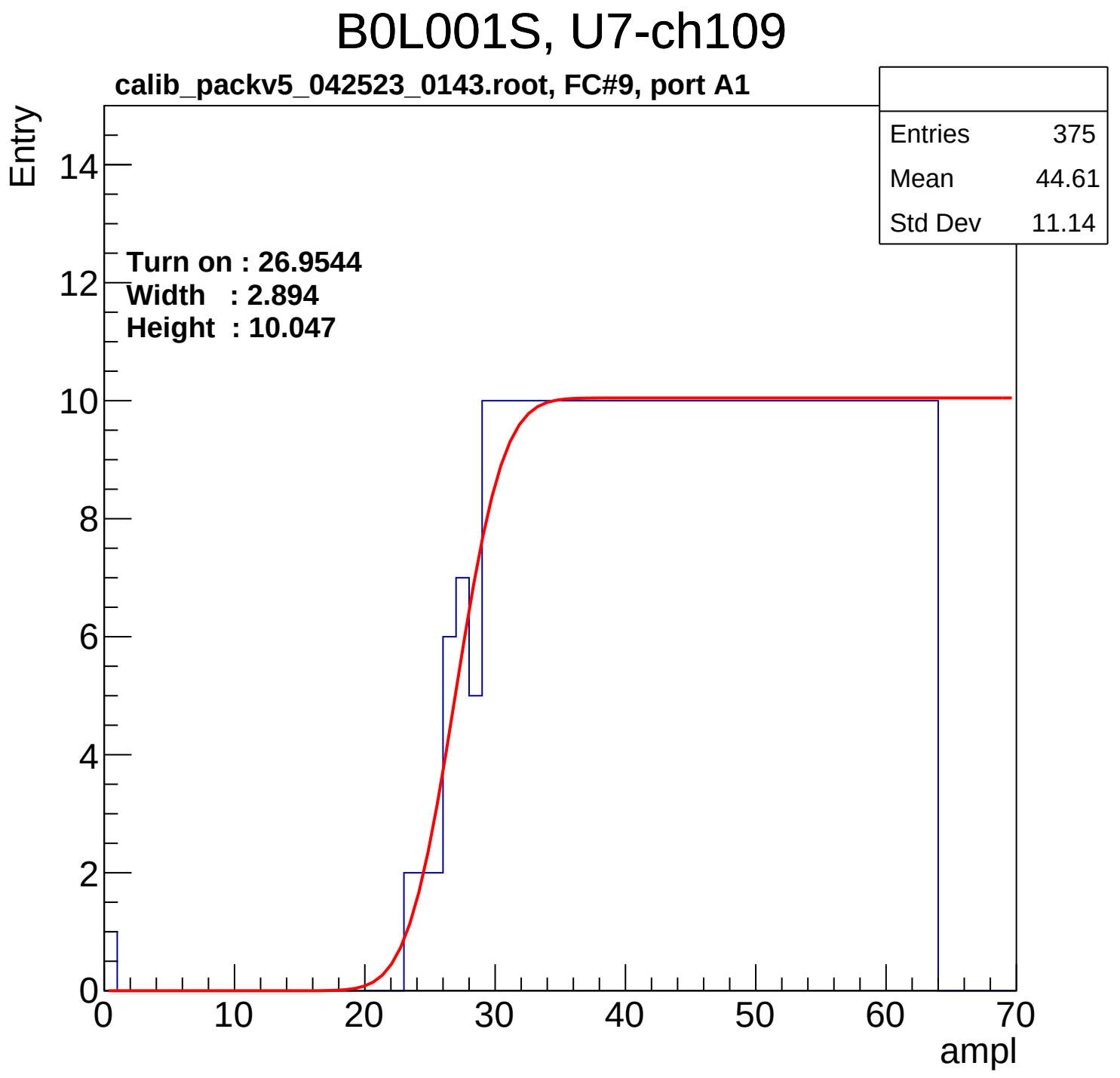
B0L001S, U7-ch109
calib_packv5_042523_0143.root, FC#9, port A1
Entries 375
Mean 44.61
Std Dev 11.14
Turn on : 26.9544
Width : 2.894
Height : 10.047
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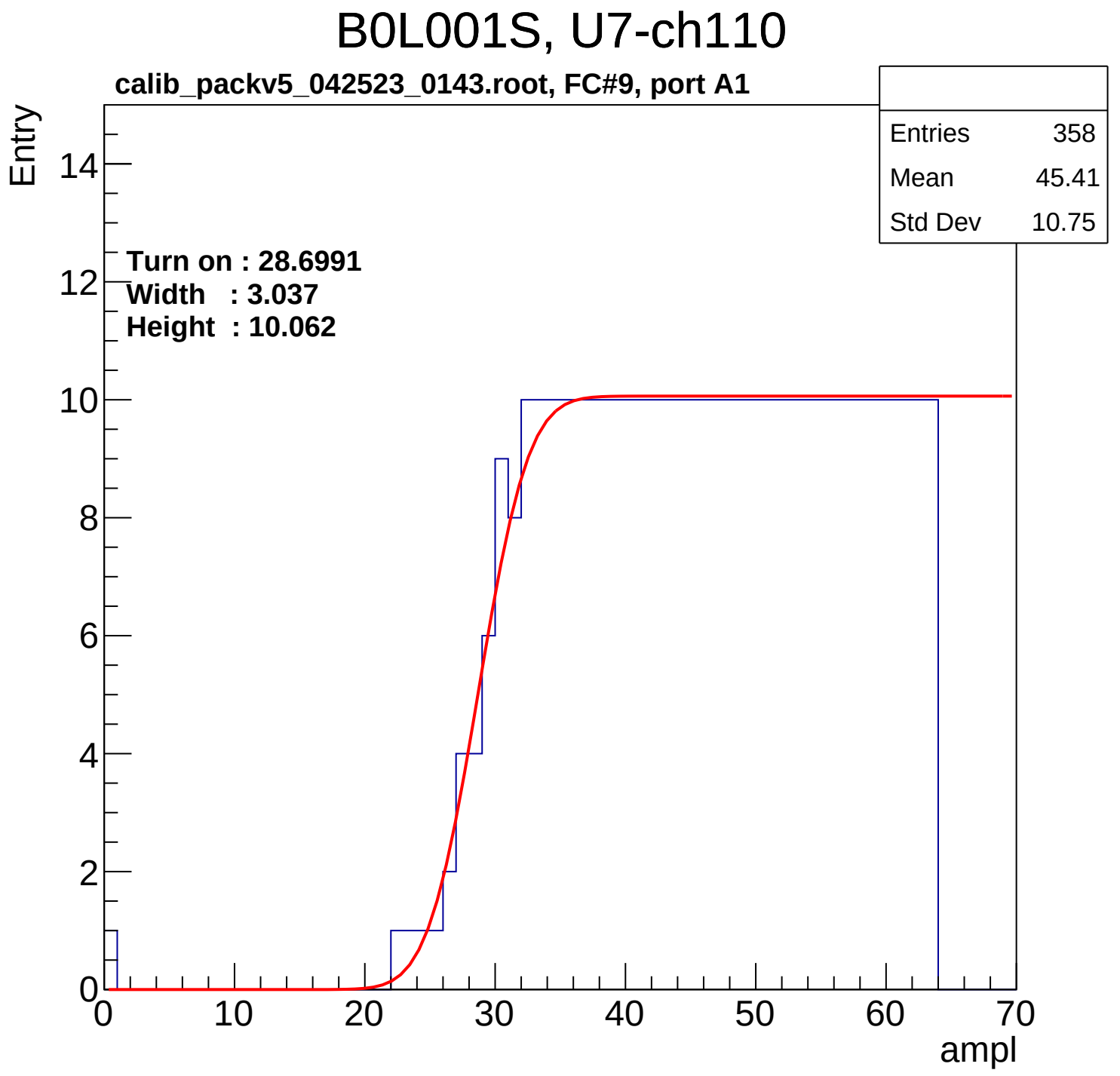
B0L001S, U7-ch110
calib_packv5_042523_0143.root, FC#9, port A1
Entries 358
Mean 45.41
Std Dev 10.75
Turn on : 28.6991
Width : 3.037
Height : 10.062
Entry
ampl
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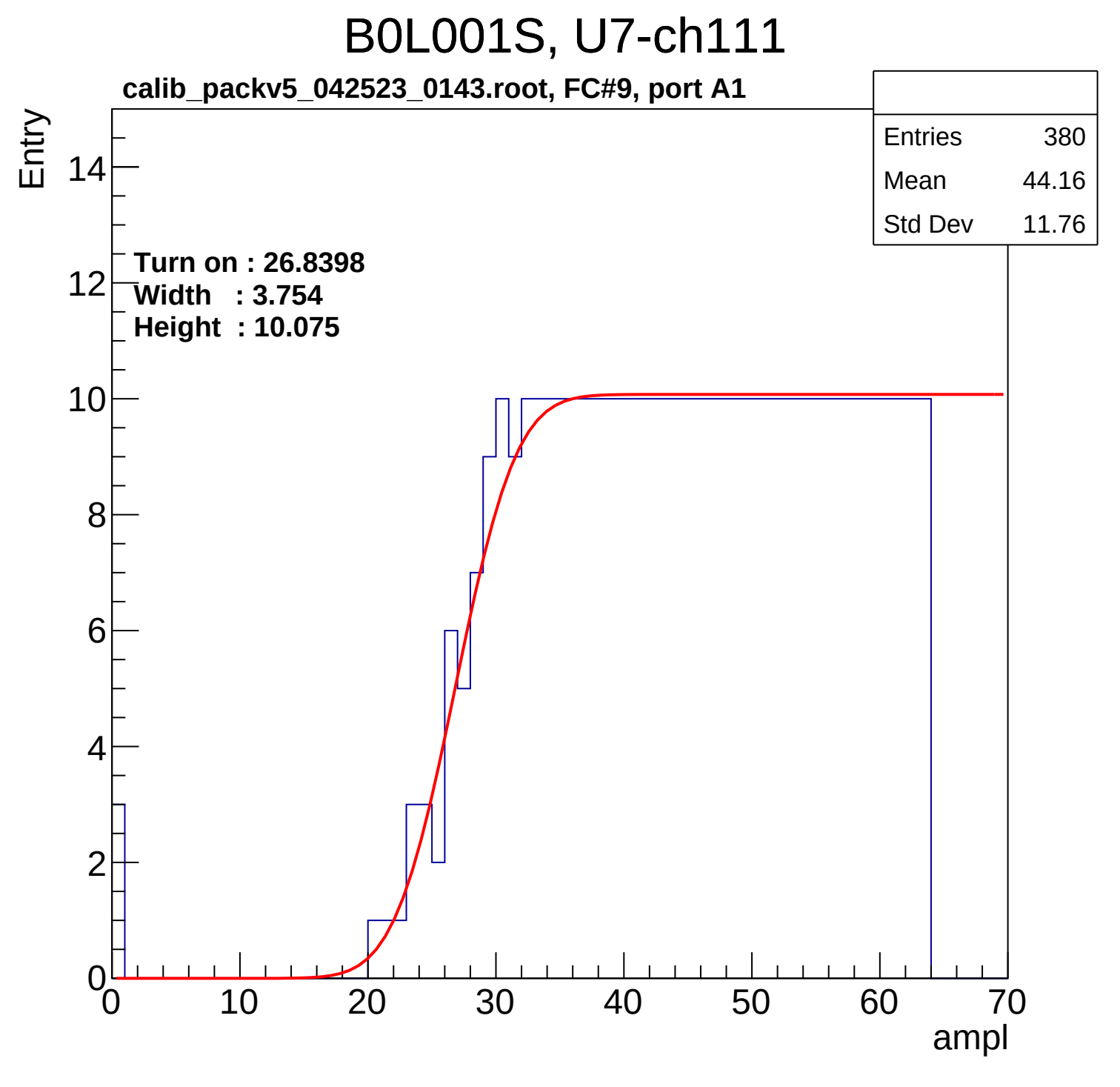
B0L001S, U7-ch111
calib_packv5_042523_0143.root, FC#9, port A1
Entries 380
Mean 44.16
Std Dev 11.76
Turn on : 26.8398
Width : 3.754
Height : 10.075
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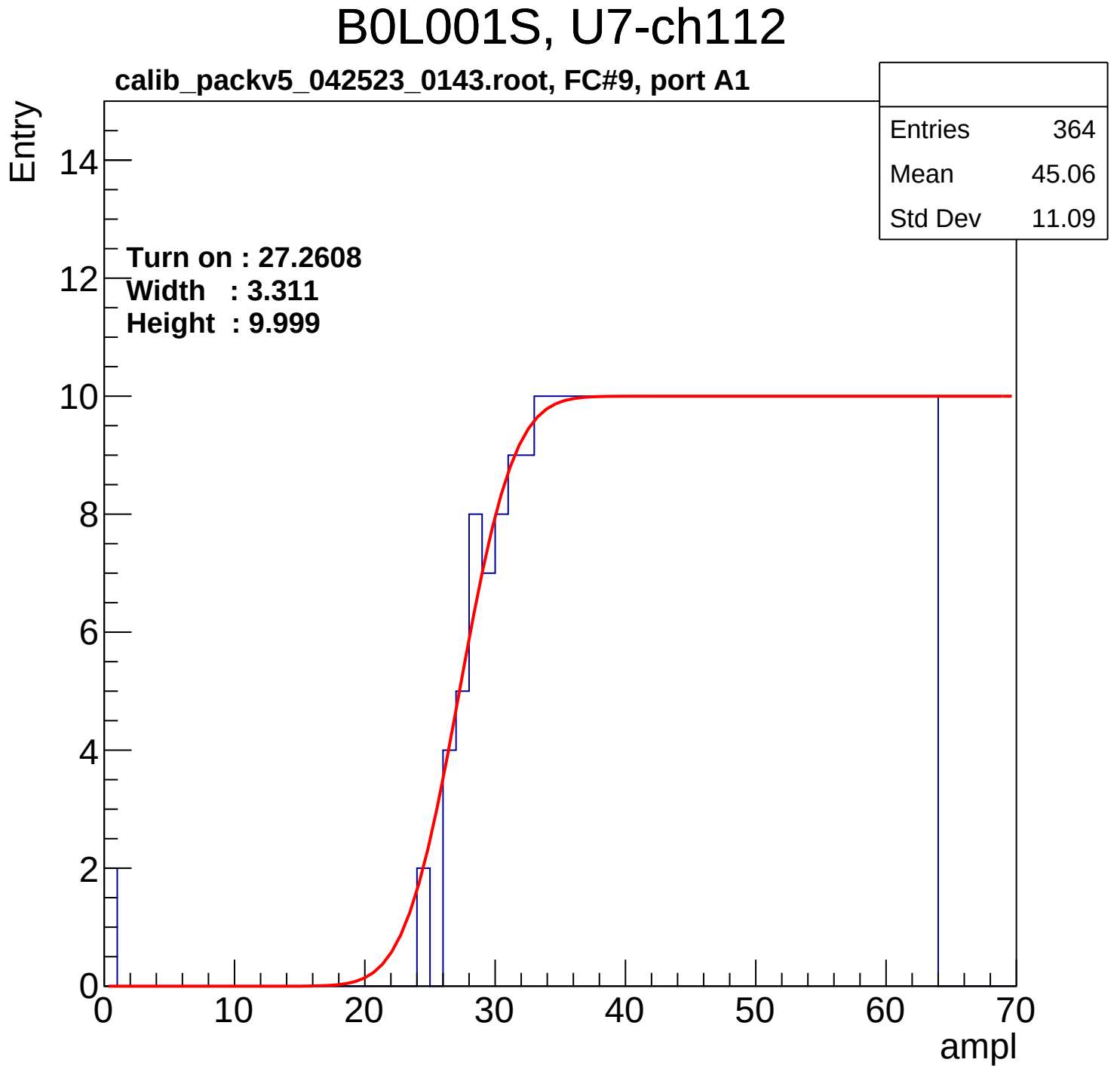
B0L001S, U7-ch112
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 45.06
Std Dev 11.09
Turn on : 27.2608
Width : 3.311
Height : 9.999
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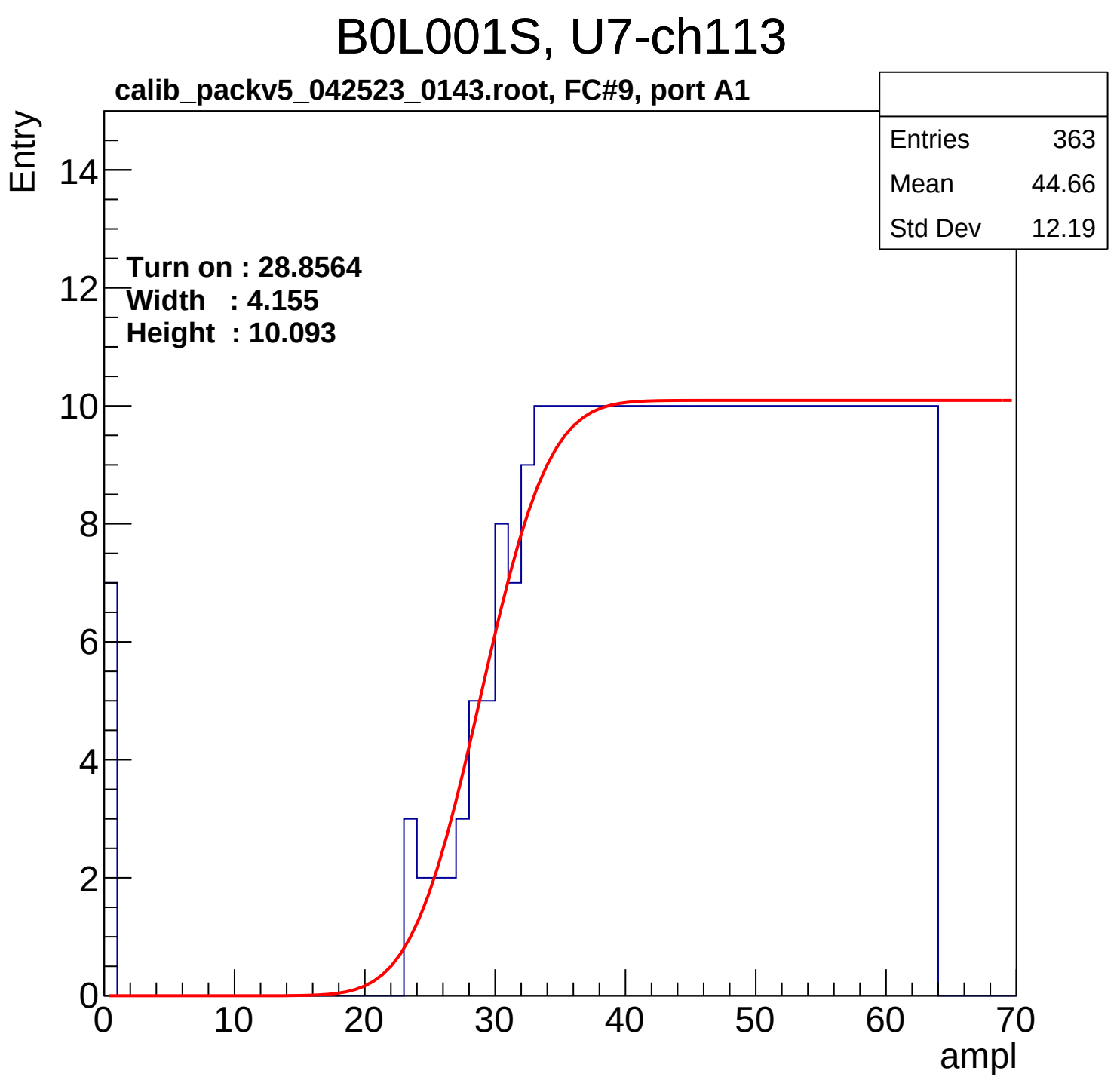
B0L001S, U7-ch113
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 44.66
Std Dev 12.19
Turn on : 28.8564
Width : 4.155
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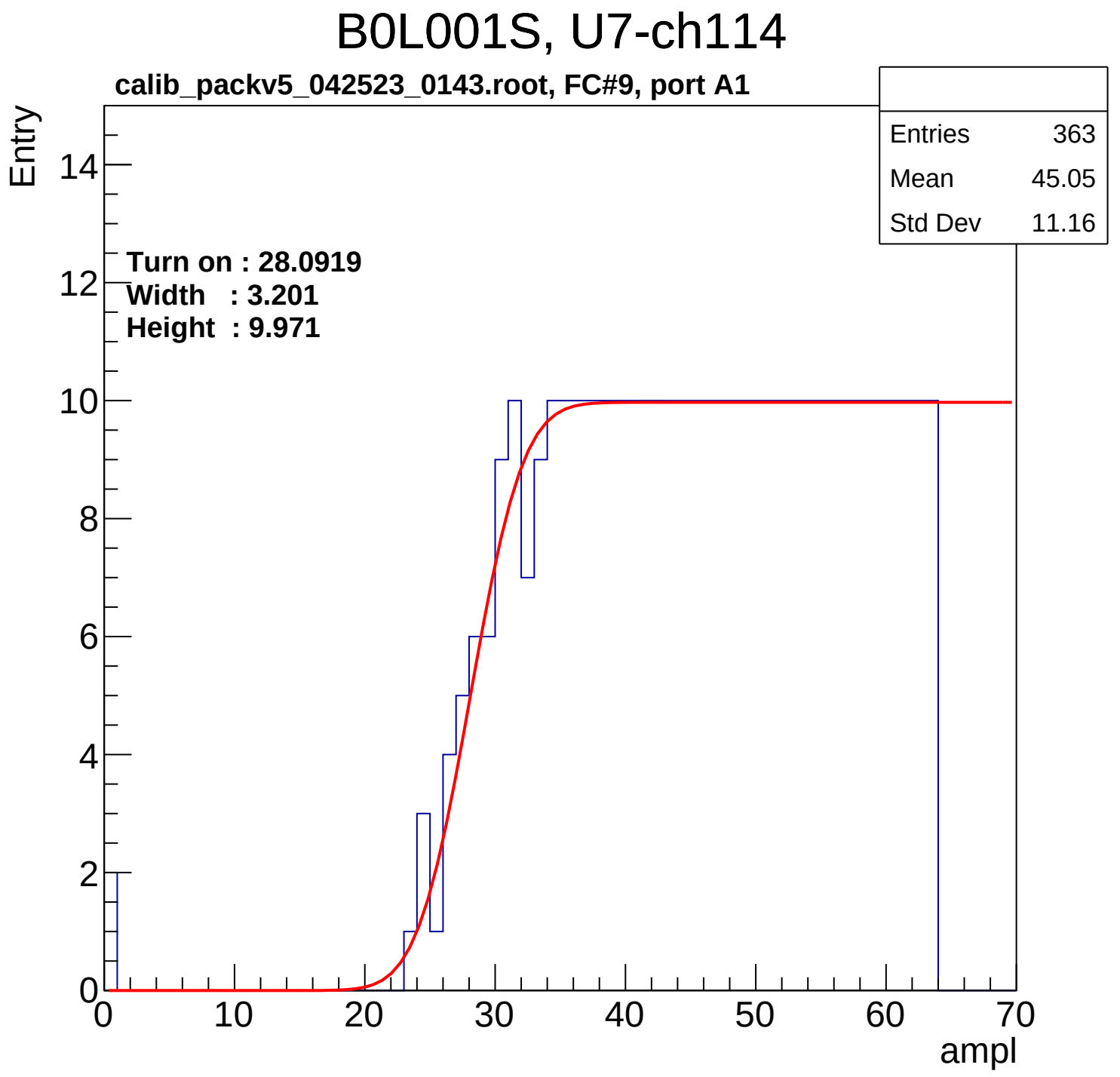
B0L001S, U7-ch114
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 45.05
Std Dev 11.16
Turn on : 28.0919
Width : 3.201
Height : 9.971
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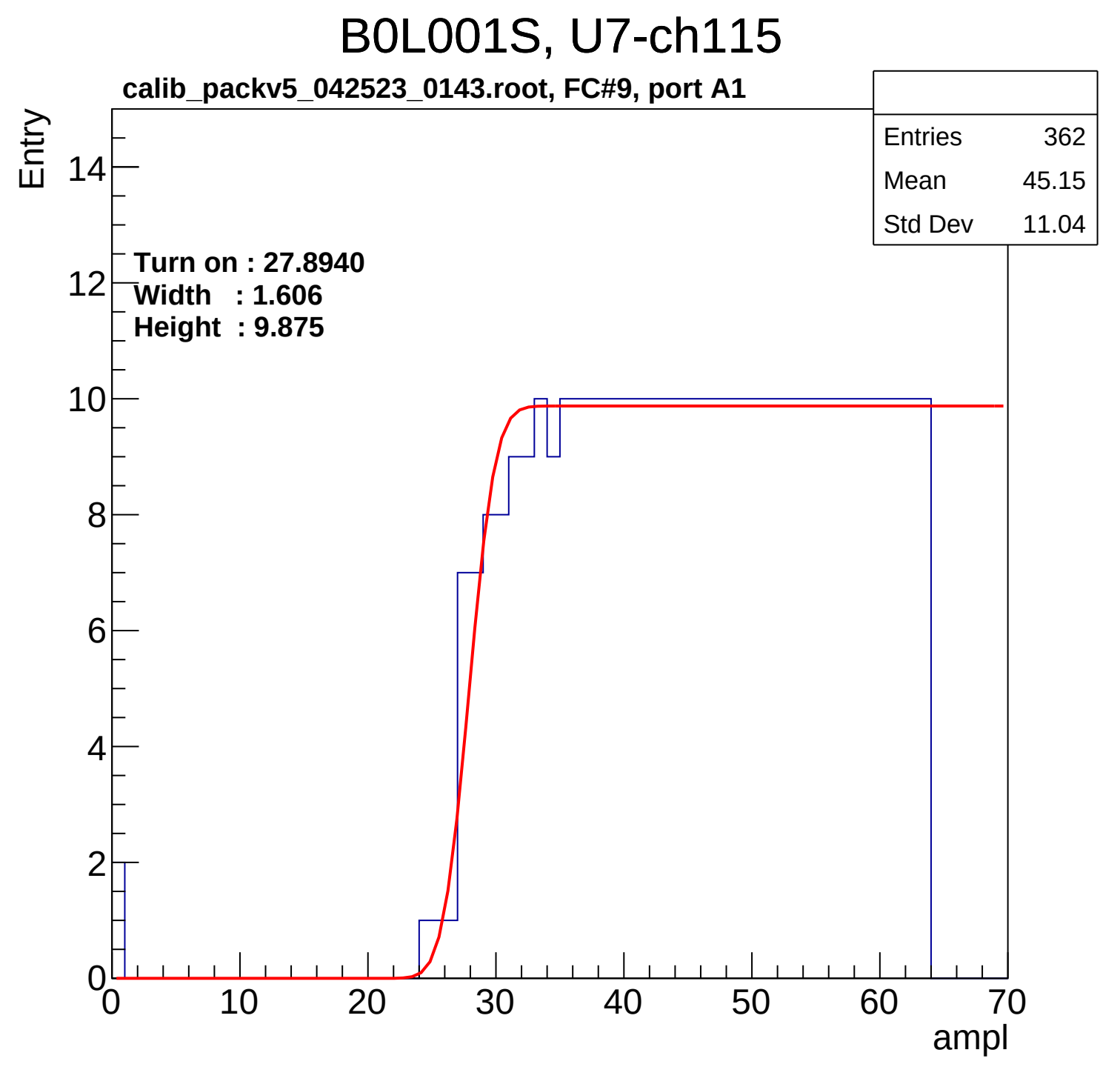
B0L001S, U7-ch115
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 45.15
Std Dev 11.04
Turn on : 27.8940
Width : 1.606
Height : 9.875
Entry
ampl
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6
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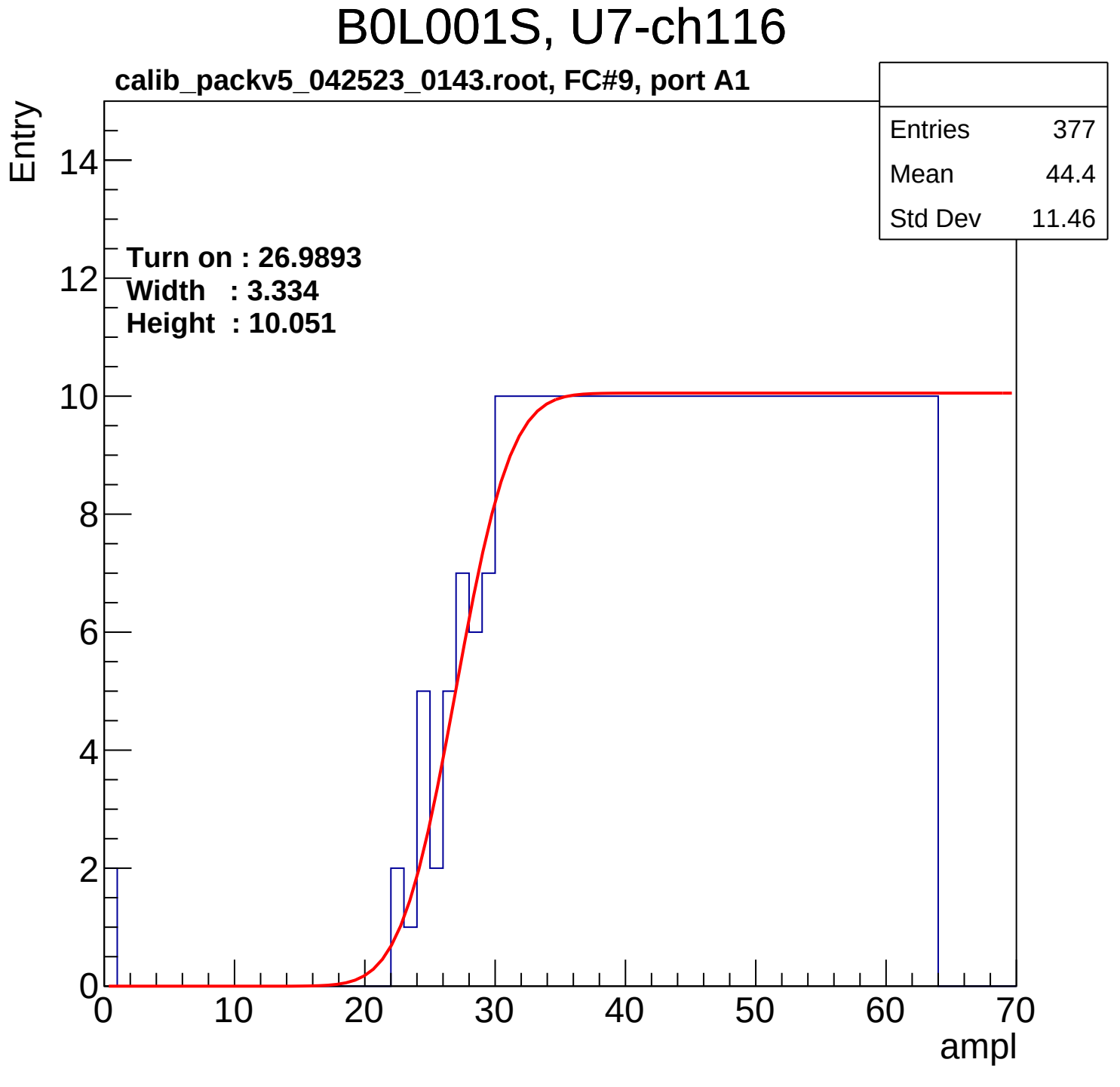
B0L001S, U7-ch116
calib_packv5_042523_0143.root, FC#9, port A1
Entries 377
Mean 44.4
Std Dev 11.46
Turn on : 26.9893
Width : 3.334
Height : 10.051
Entry
ampl
0
2
4
6
8
10
12
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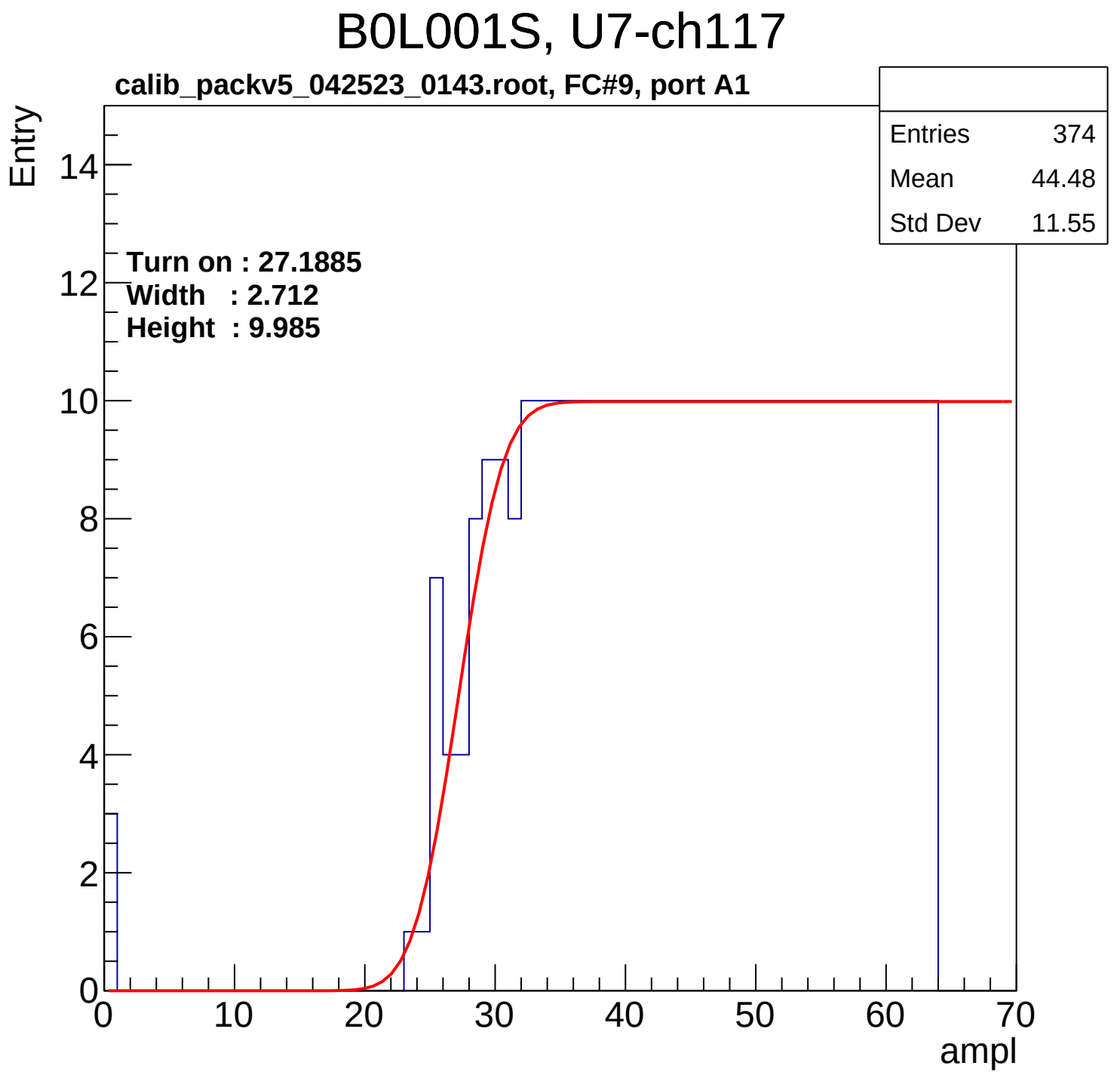
B0L001S, U7-ch117
calib_packv5_042523_0143.root, FC#9, port A1
Entries 374
Mean 44.48
Std Dev 11.55
Turn on : 27.1885
Width : 2.712
Height : 9.985
Entry
ampl
0
2
4
6
8
10
12
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10
20
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40
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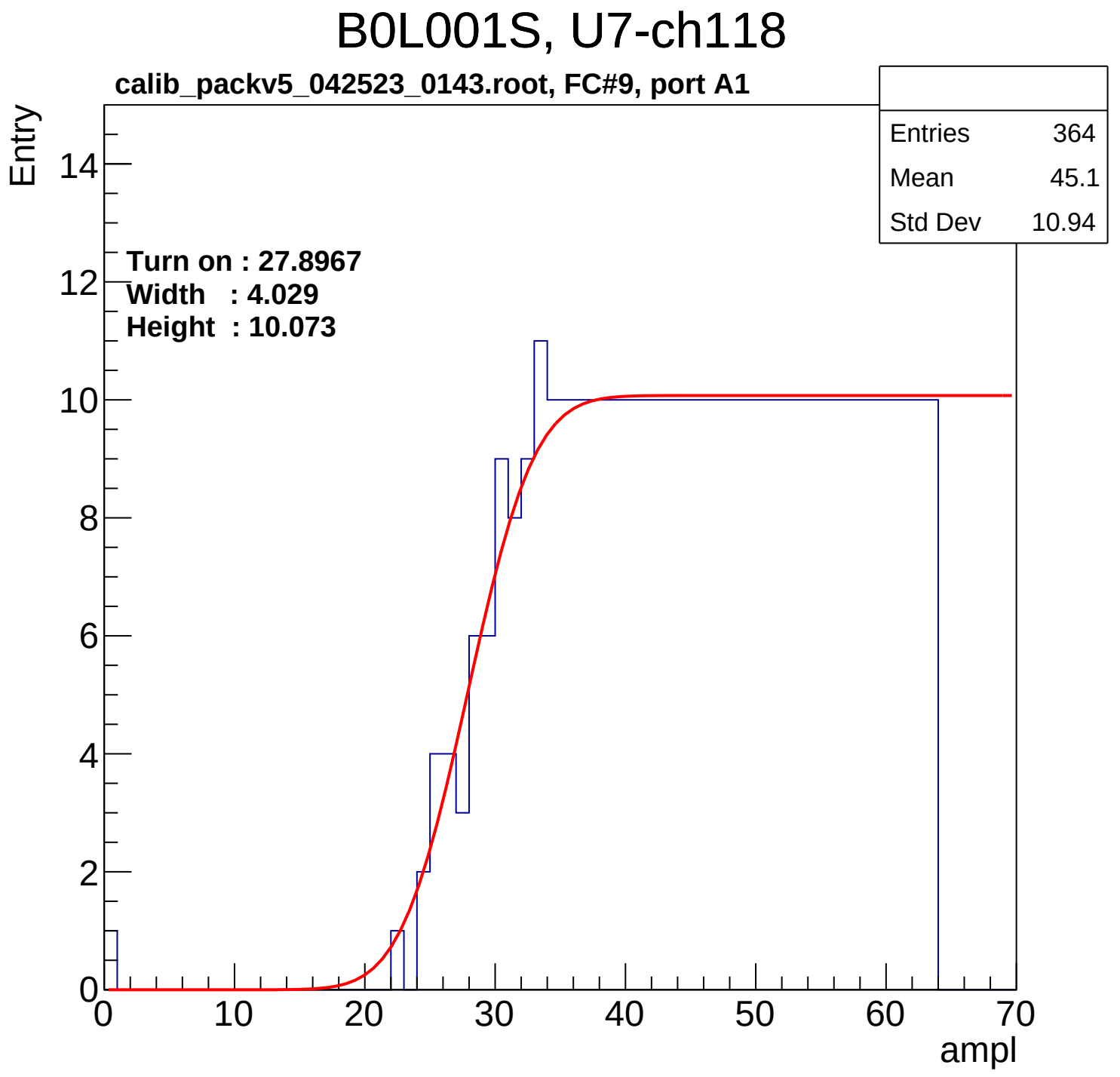
B0L001S, U7-ch118
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 45.1
Std Dev 10.94
Turn on : 27.8967
Width : 4.029
Height : 10.073
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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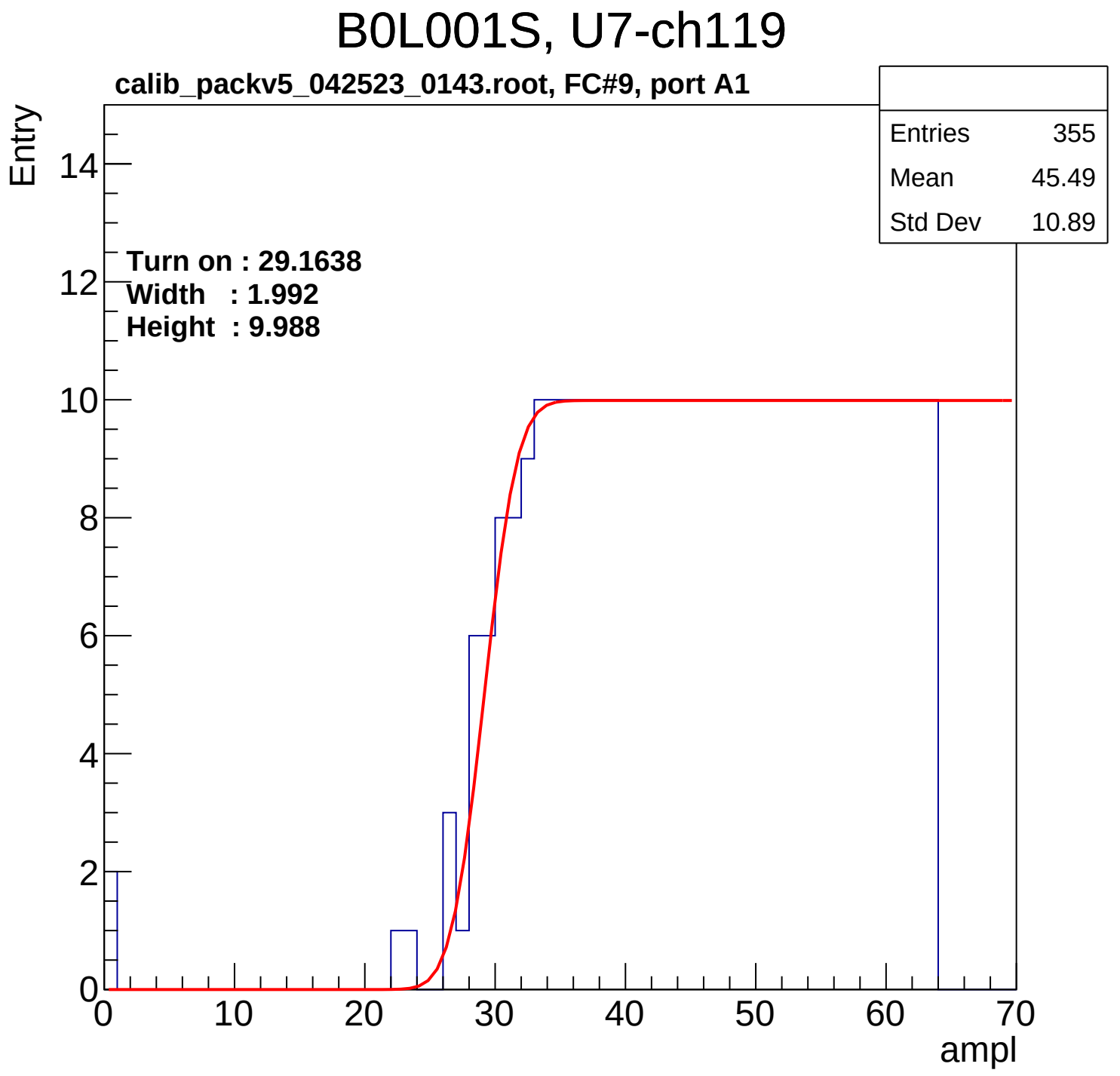
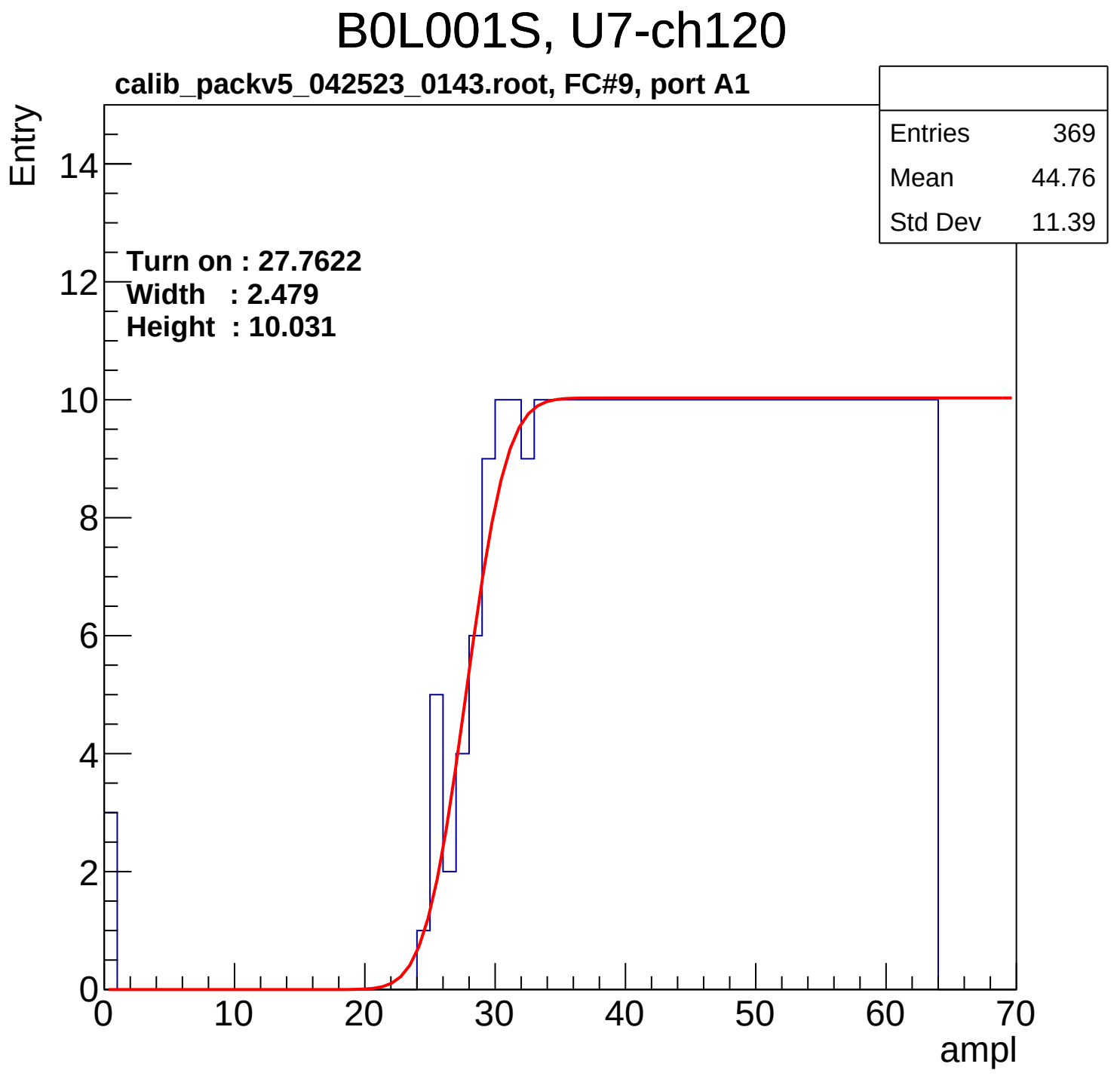

B0L001S, U7-ch119
calib_packv5_042523_0143.root, FC#9, port A1
Entries 355
Mean 45.49
Std Dev 10.89
Turn on : 29.1638
Width : 1.992
Height : 9.988
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U7-ch120
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.76
Std Dev 11.39
Turn on : 27.7622
Width : 2.479
Height : 10.031
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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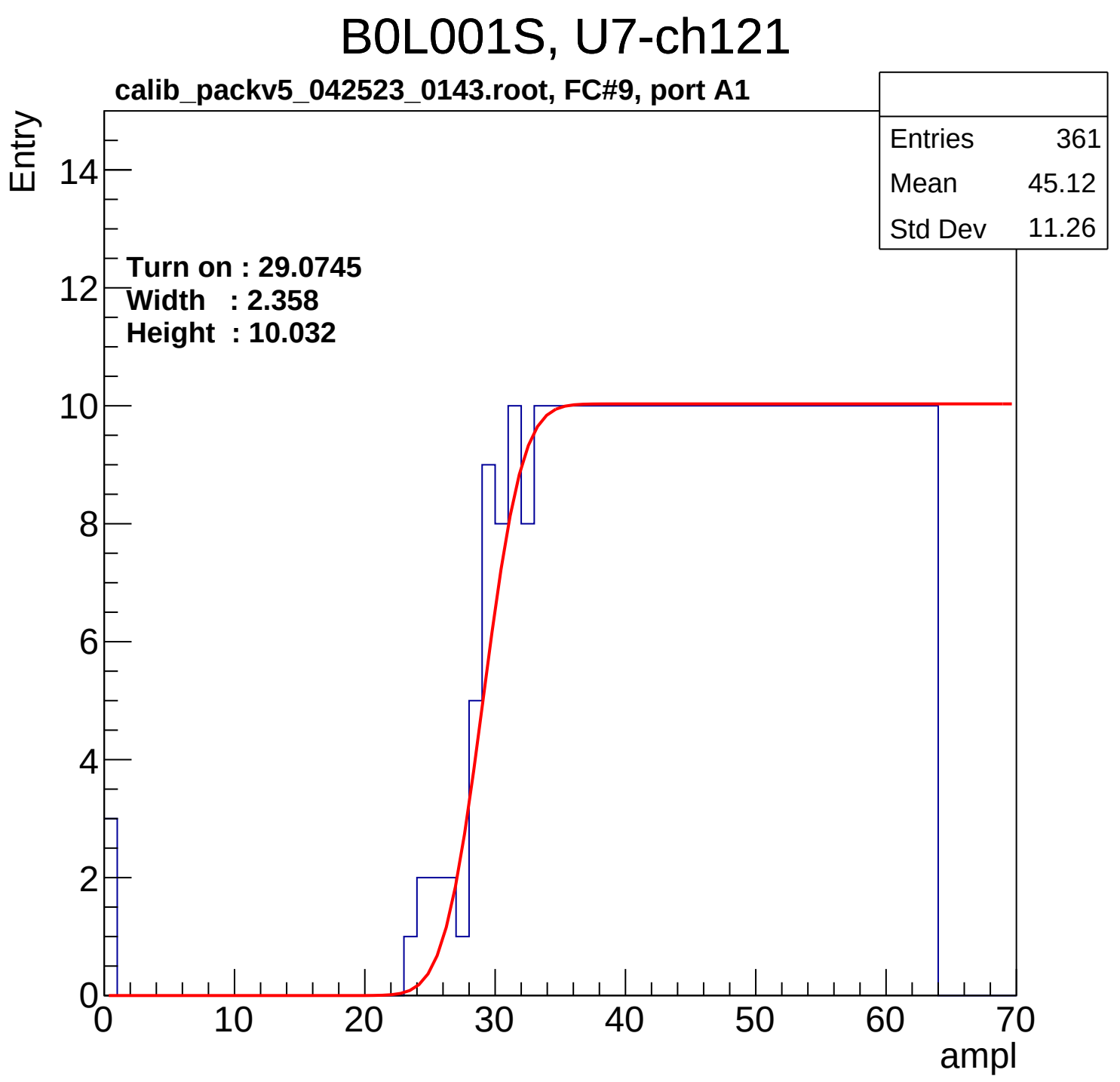
B0L001S, U7-ch121
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 45.12
Std Dev 11.26
Turn on : 29.0745
Width : 2.358
Height : 10.032
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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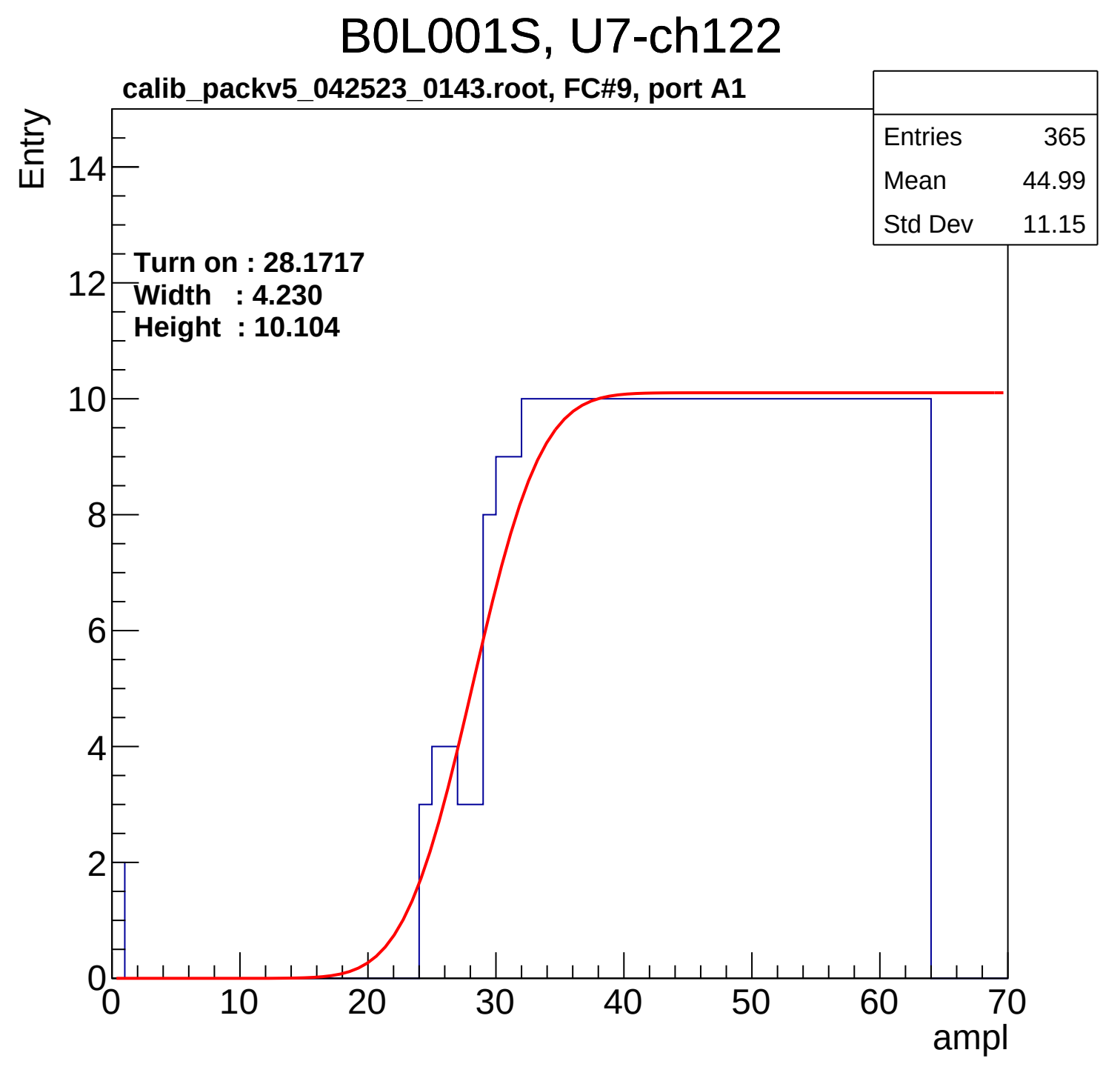
B0L001S, U7-ch122
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 44.99
Std Dev 11.15
Turn on : 28.1717
Width : 4.230
Height : 10.104
Entry
ampl
0
2
4
6
8
10
12
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0
10
20
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40
50
60
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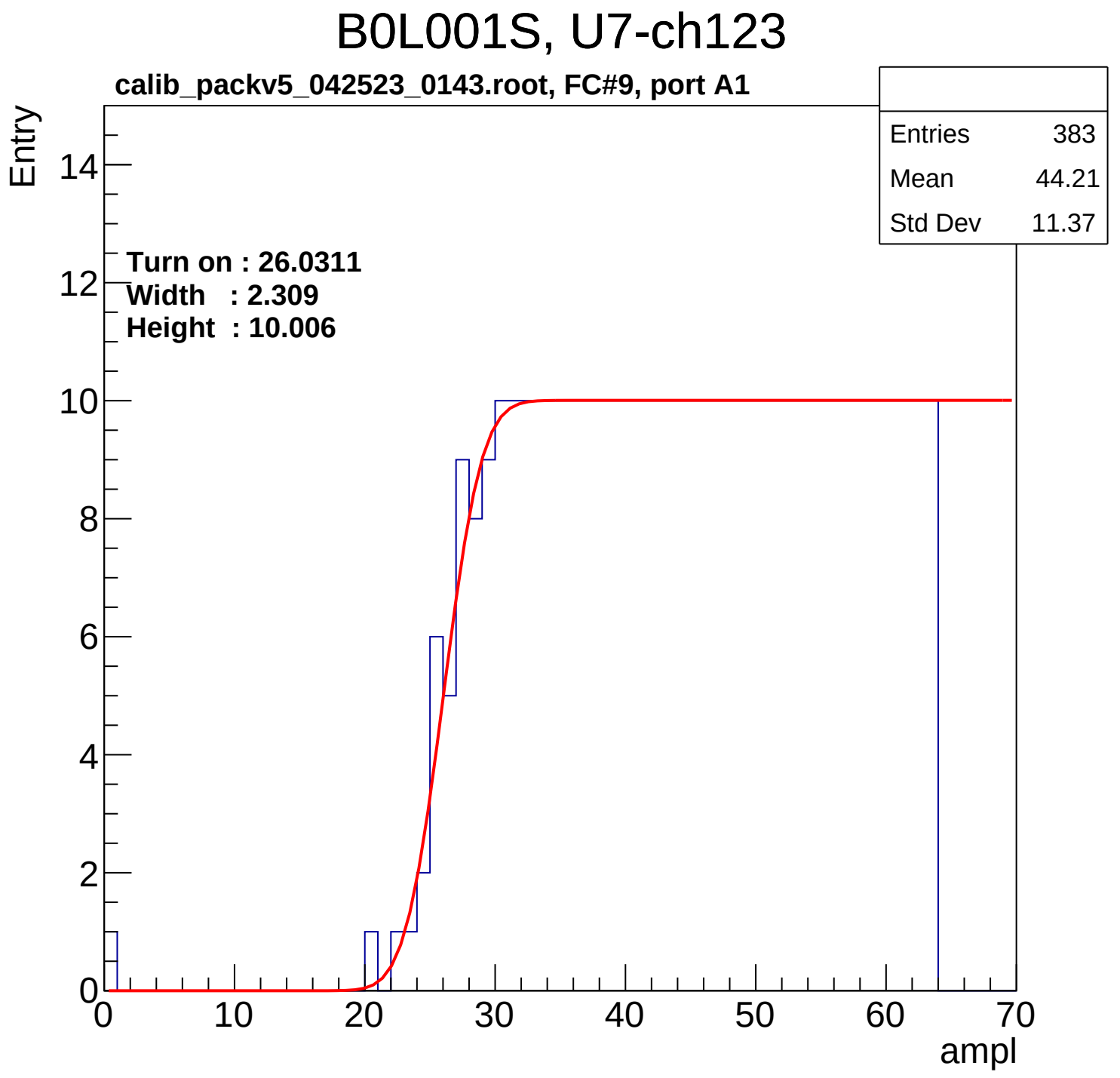
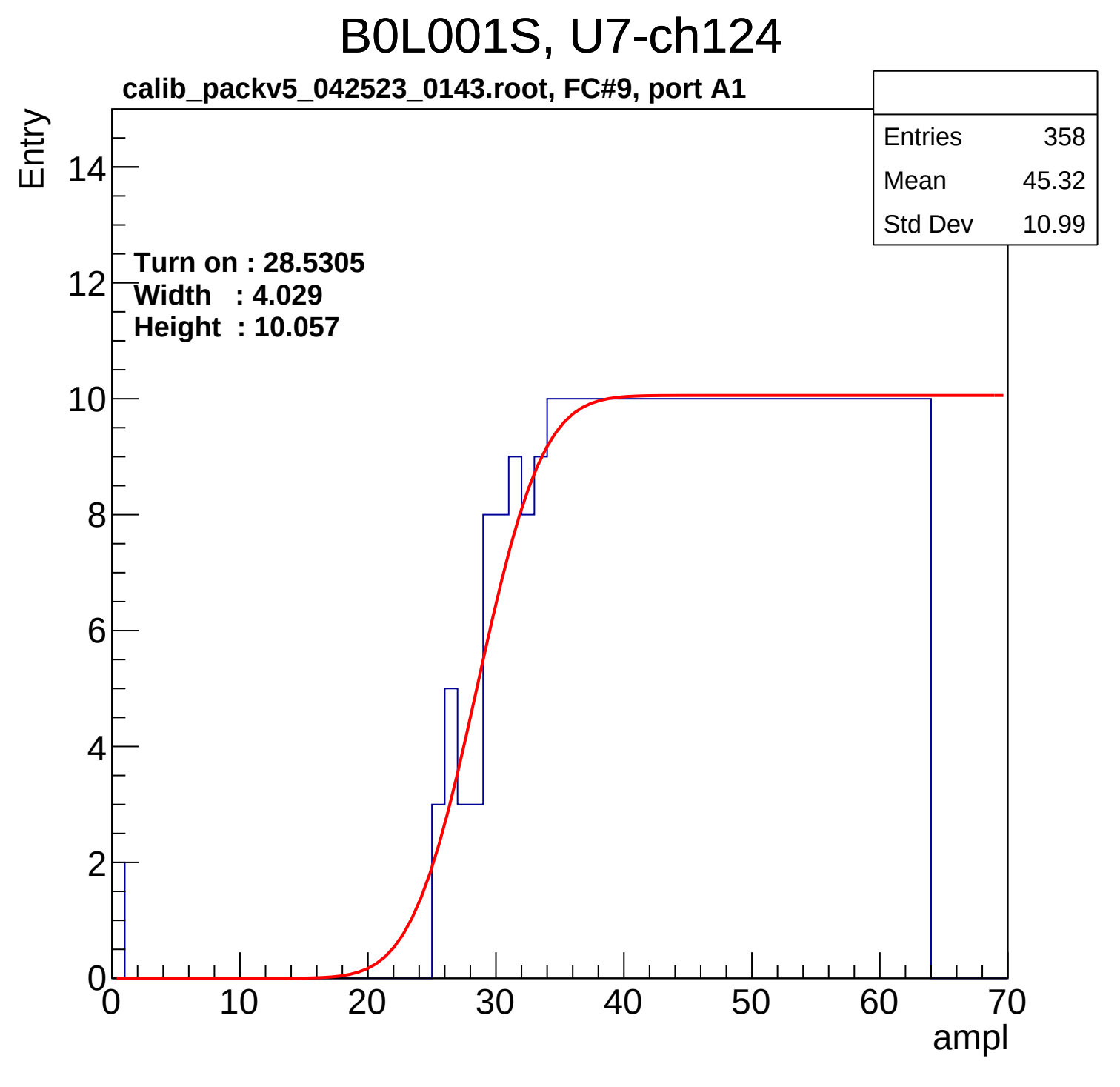

B0L001S, U7-ch123
calib_packv5_042523_0143.root, FC#9, port A1
Entries 383
Mean 44.21
Std Dev 11.37
Turn on : 26.0311
Width : 2.309
Height : 10.006
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U7-ch124
calib_packv5_042523_0143.root, FC#9, port A1
Entries 358
Mean 45.32
Std Dev 10.99
Turn on : 28.5305
Width : 4.029
Height : 10.057
Entry
ampl
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2
4
6
8
10
12
14
0
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20
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40
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60
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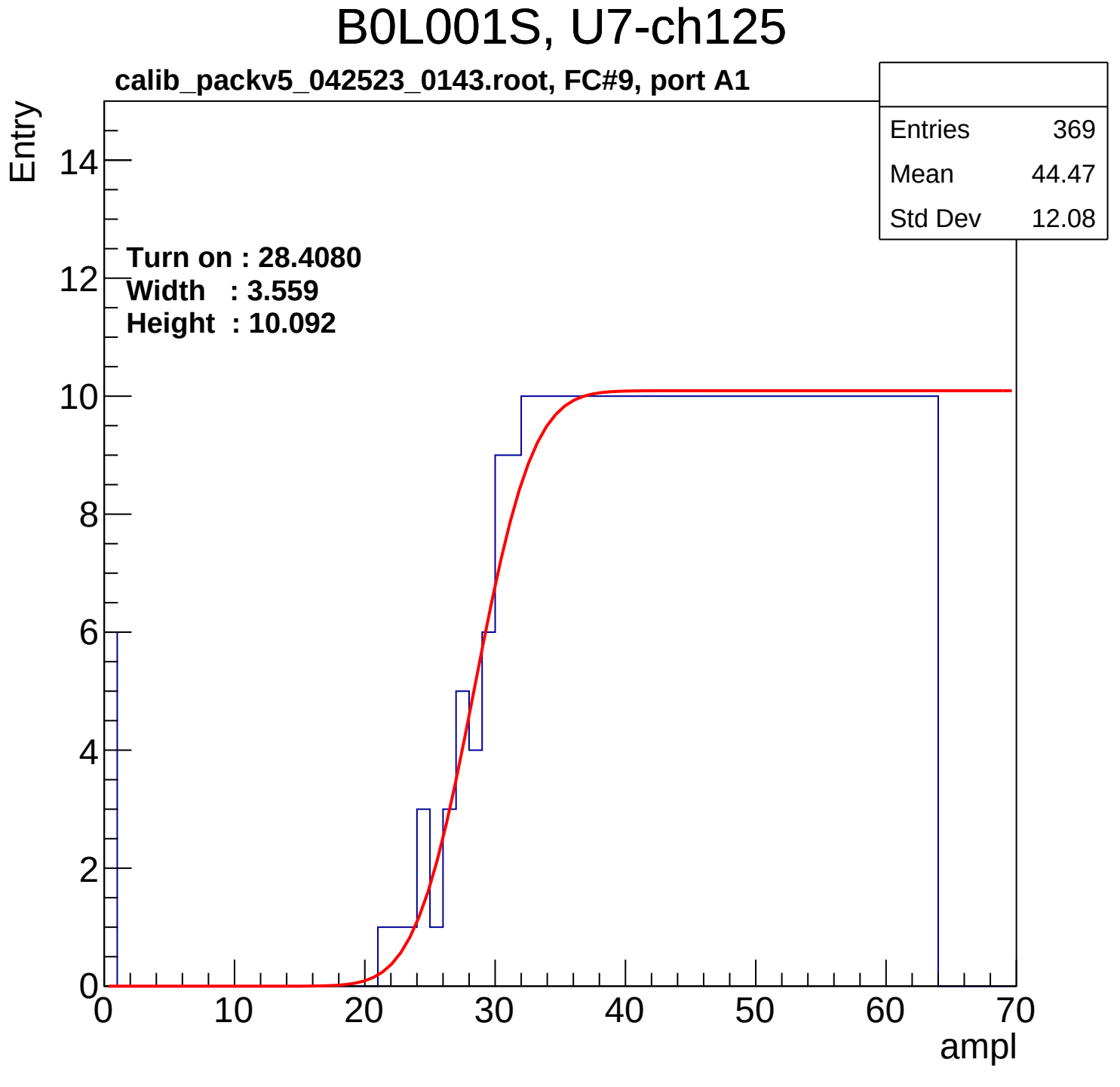
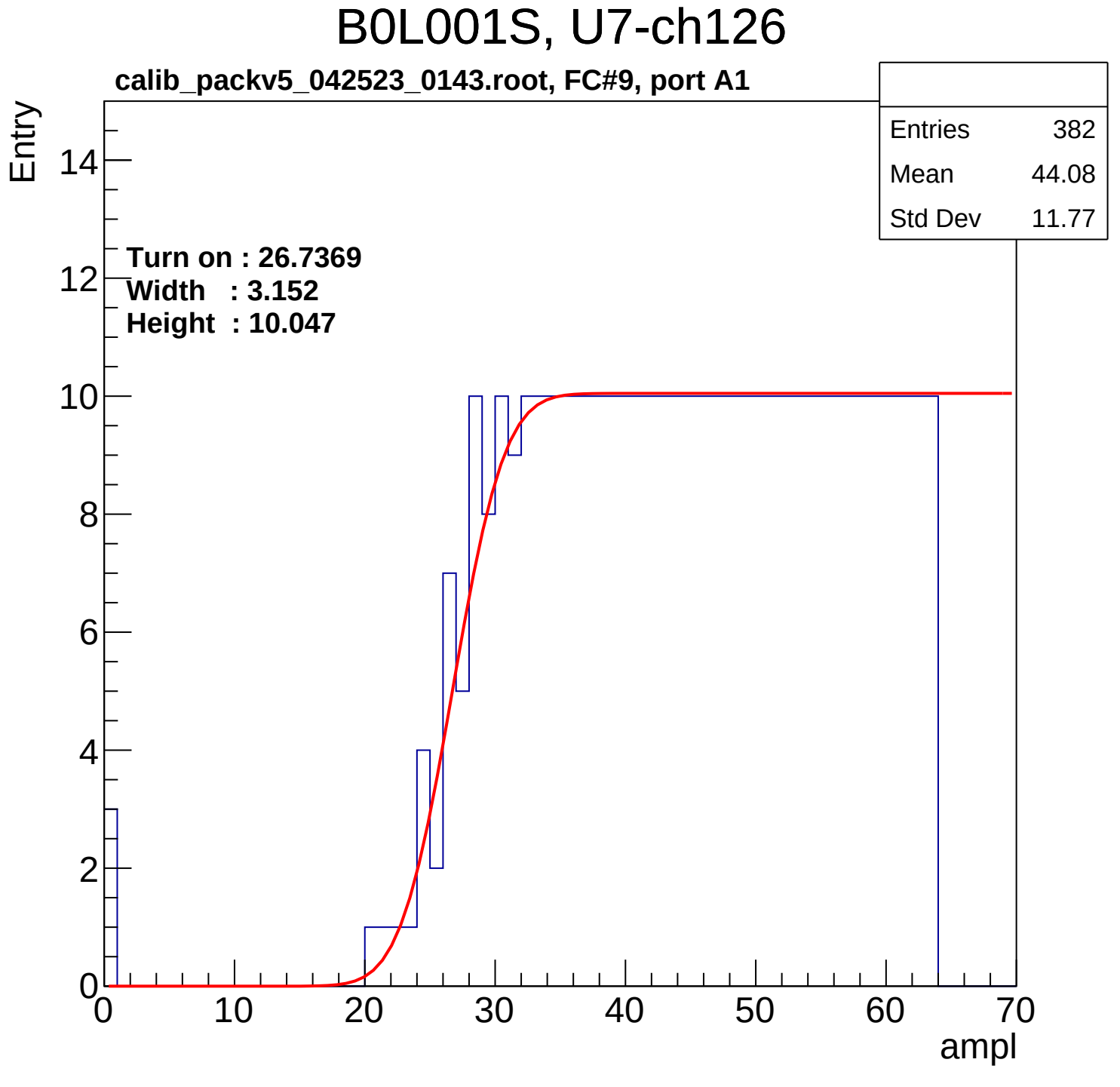

B0L001S, U7-ch125
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.47
Std Dev 12.08
Turn on : 28.4080
Width : 3.559
Height : 10.092
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U7-ch126
calib_packv5_042523_0143.root, FC#9, port A1
Entries 382
Mean 44.08
Std Dev 11.77
Turn on : 26.7369
Width : 3.152
Height : 10.047
Entry
ampl
0
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4
6
8
10
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0
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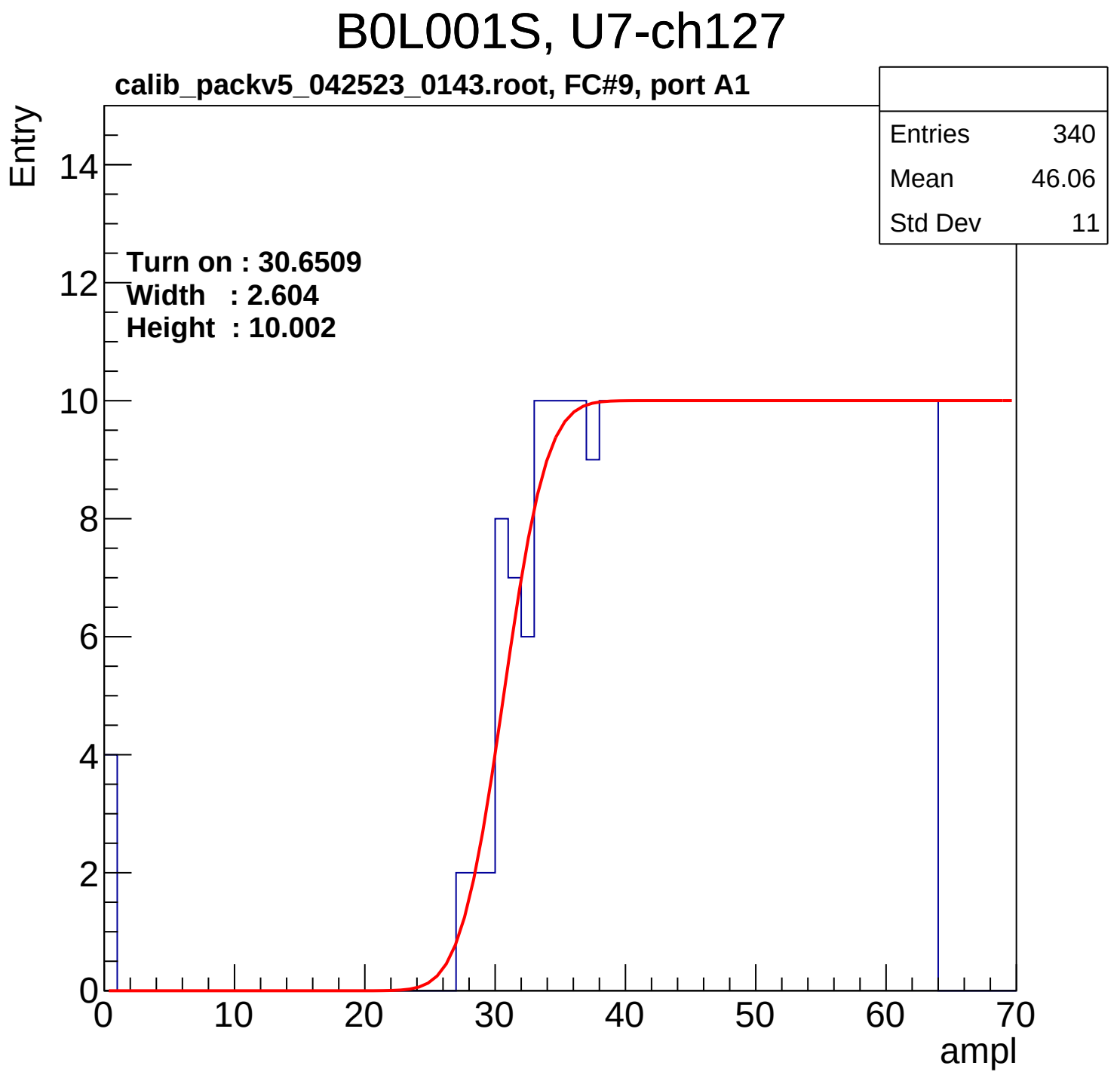
B0L001S, U7-ch127
calib_packv5_042523_0143.root, FC#9, port A1
Entries 340
Mean 46.06
Std Dev 11
Turn on : 30.6509
Width : 2.604
Height : 10.002
Entry
ampl
0
2
4
6
8
10
12
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0
10
20
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40
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60
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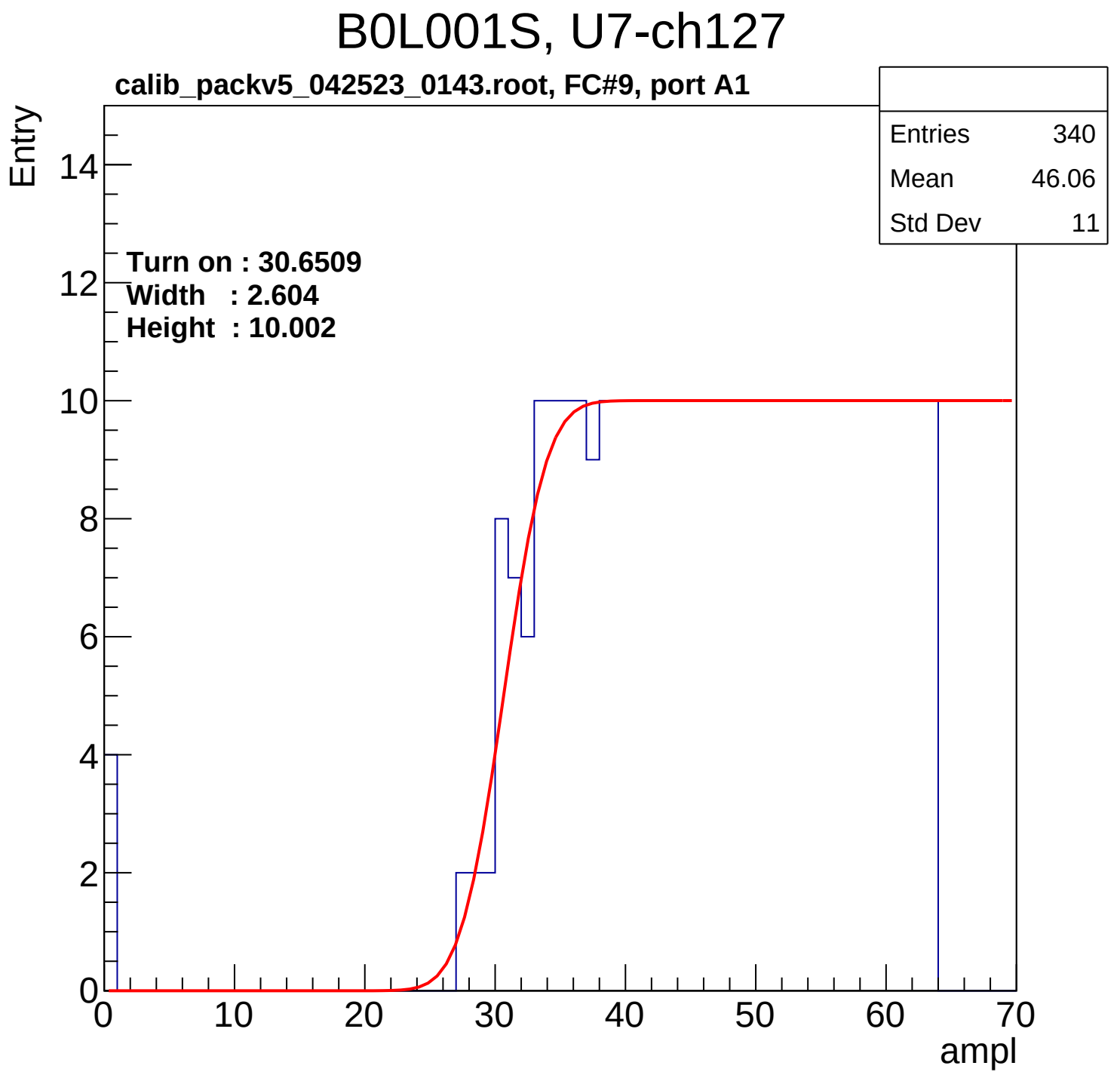
B0L001S, U7-ch127
calib_packv5_042523_0143.root, FC#9, port A1
Entries 340
Mean 46.06
Std Dev 11
Turn on : 30.6509
Width : 2.604
Height : 10.002
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70