B0L101S, U7-ch0

calib_packv5_042523_0143.root, FC#1, port C1
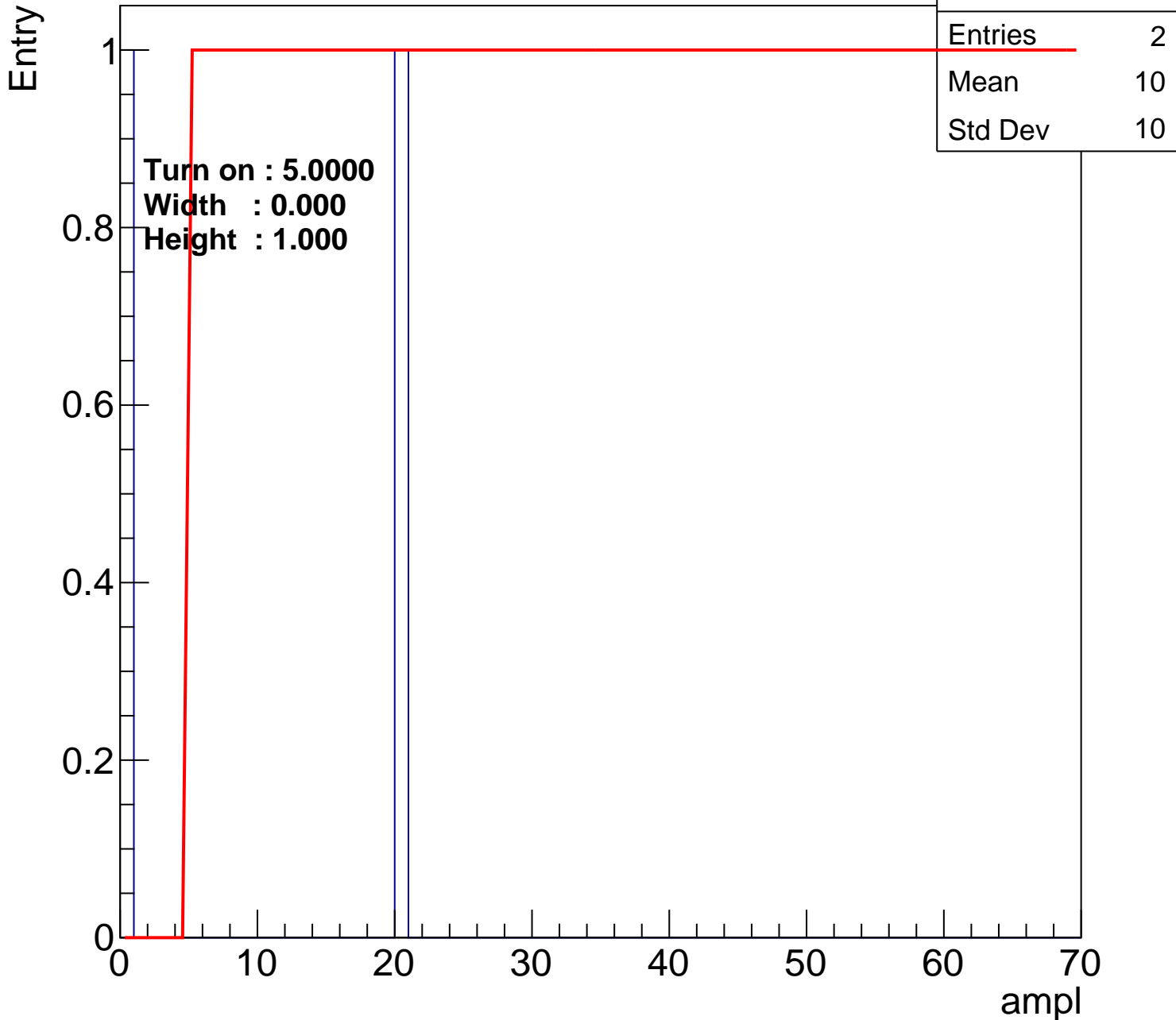
Entries	2
Mean	10
Std Dev	10

Turn on : 5.0000
Width   : 0.000
Height : 1.000

B0L101S, U7-ch1

Entry

Entries	3
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

ampl
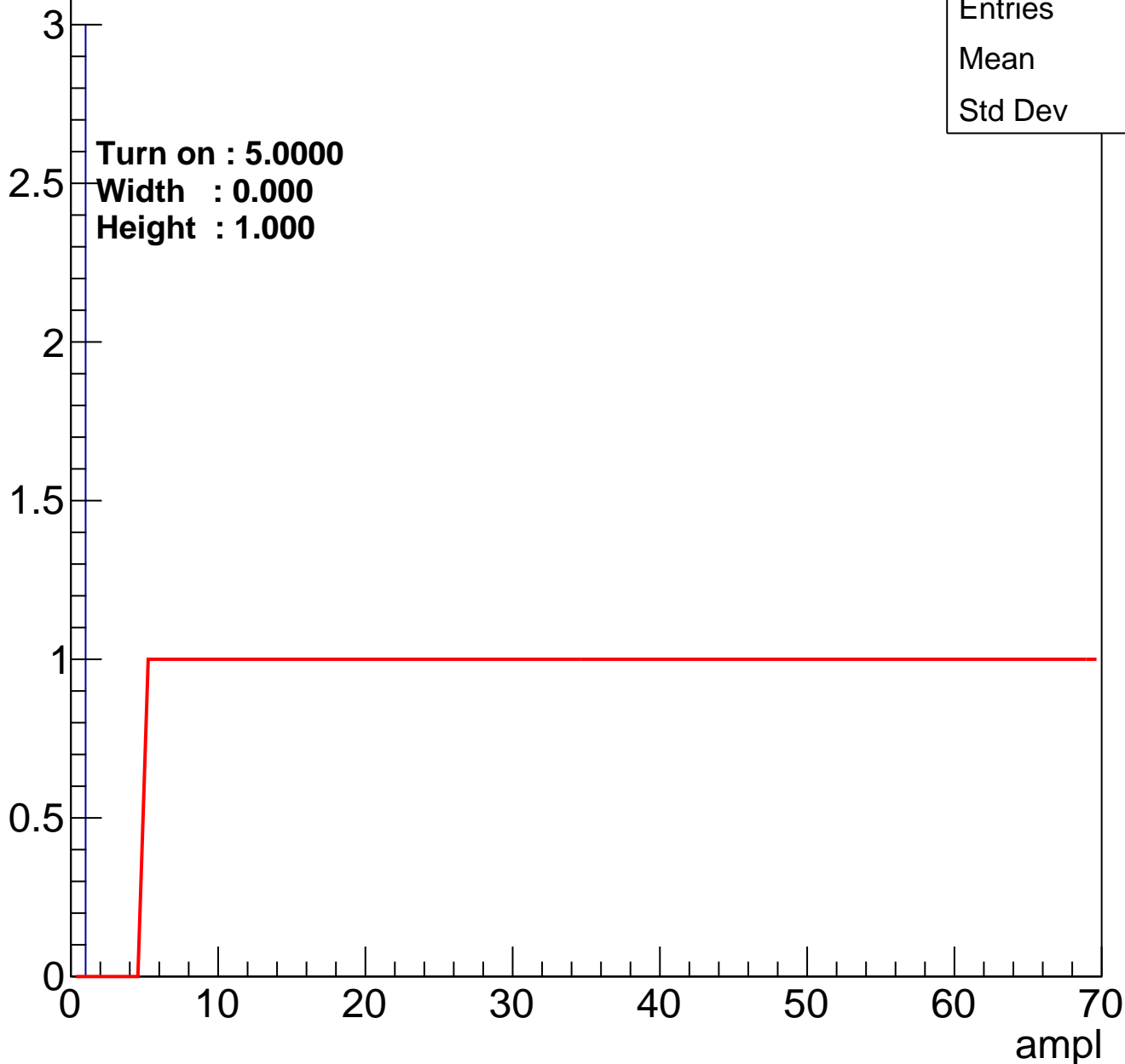
B0L101S, U7-ch2

calib_packv5_042523_0143.root, FC#1, port C1

Entries	1
Mean	0
Std Dev	0

Entry

Turn on : 5.0000
Width   : 0.000
Height : 1.000

ampl

B0L101S, U7-ch3

Entry

Entries	3
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

ampl
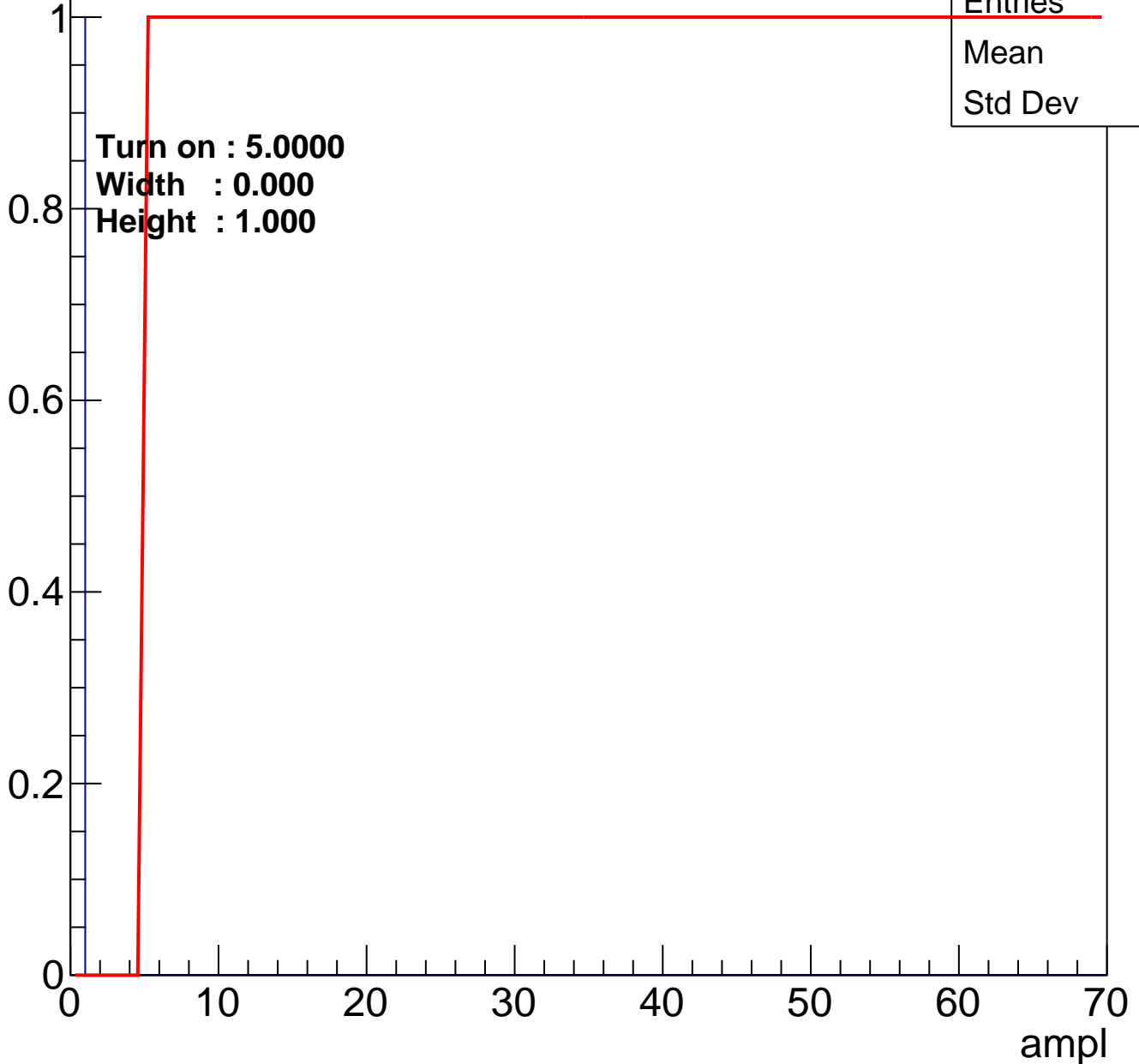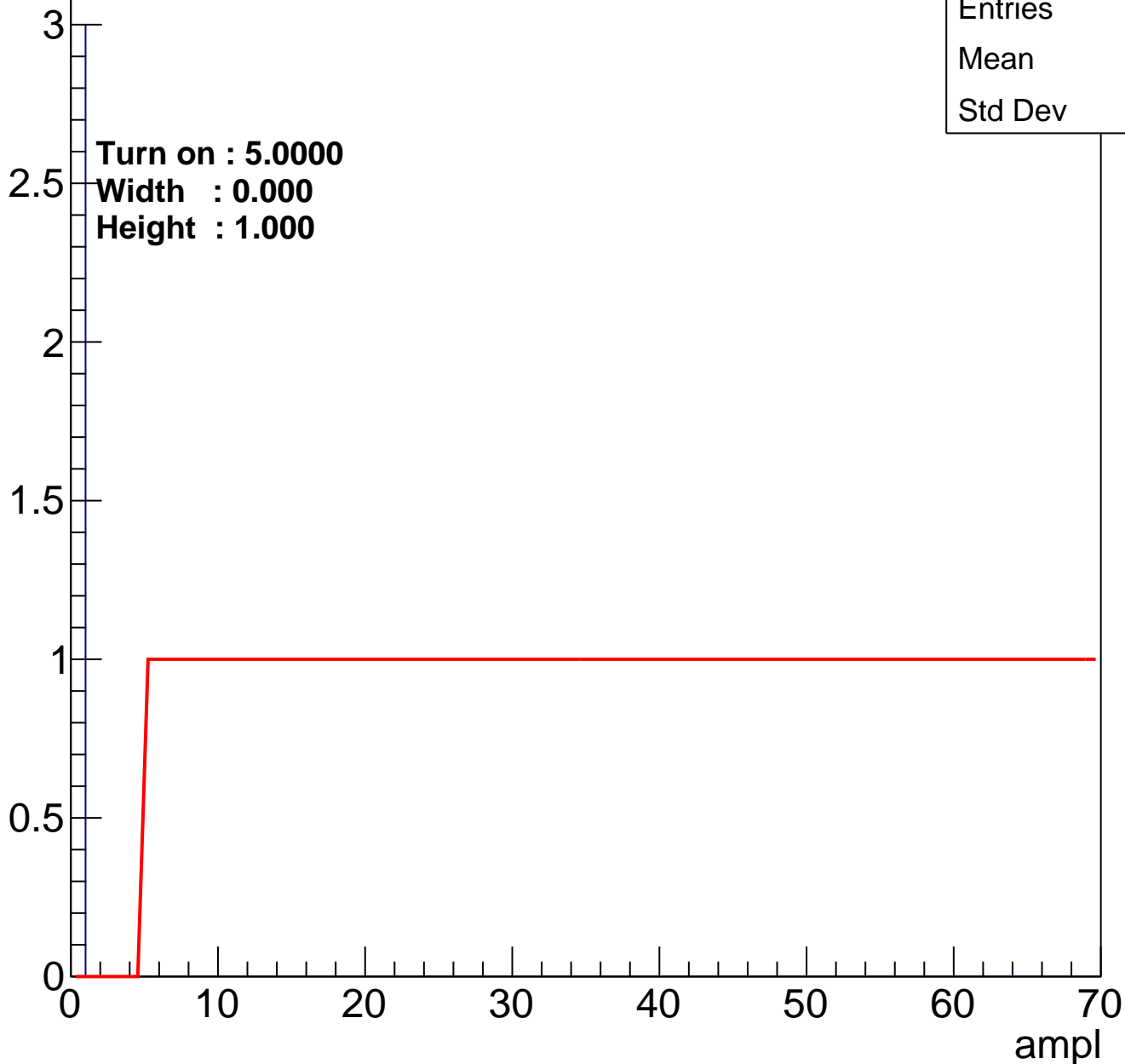
B0L101S, U7-ch4

calib_packv5_042523_0143.root, FC#1, port C1

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entries	2
Mean	0
Std Dev	0

Entry

ampl

B0L101S, U7-ch5

Entries	5
Mean	0
Std Dev	0

Turn on : 5.0000
Width : 0.000
Height : 1.000

Entry

ampl
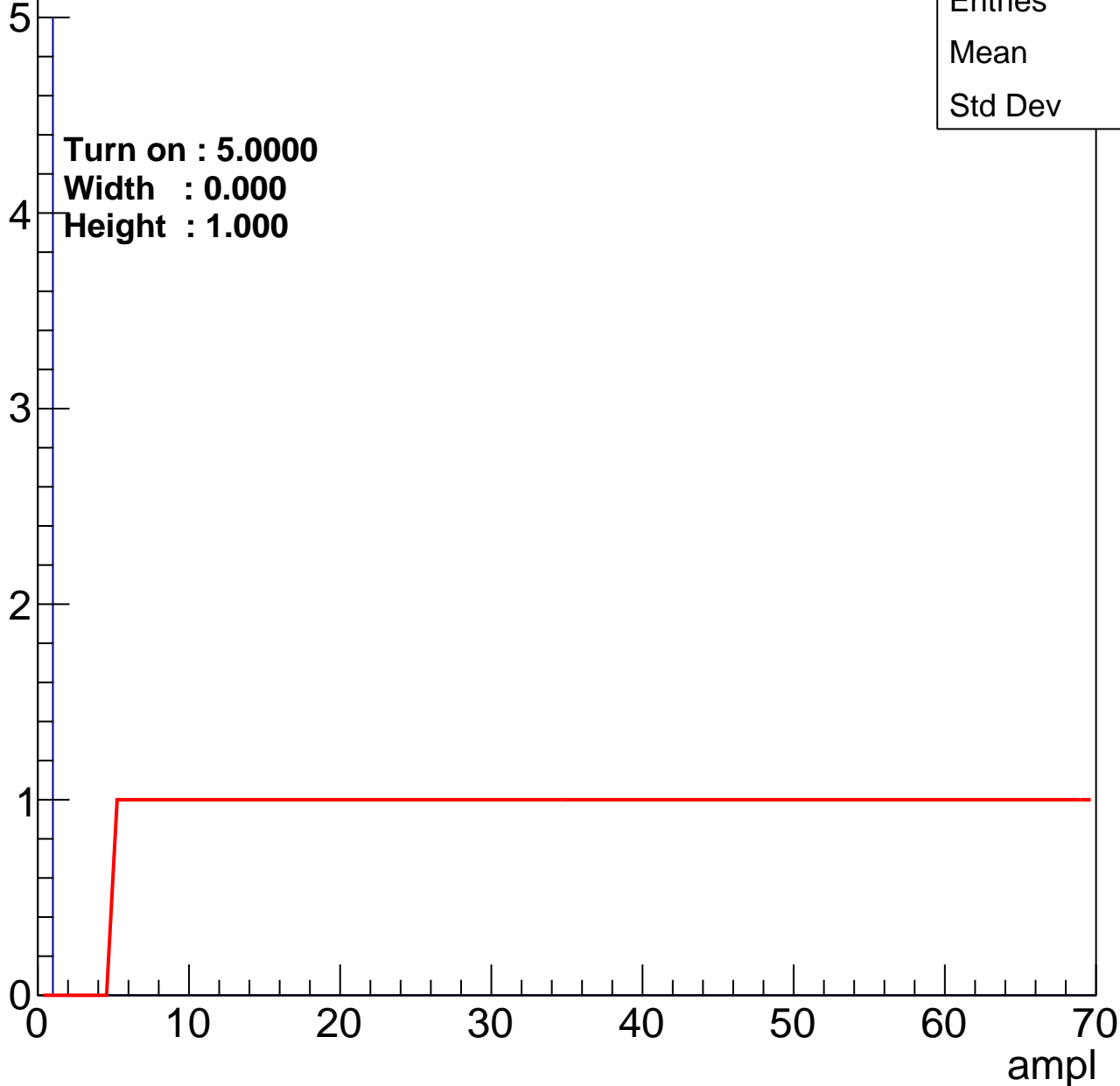
B0L101S, U7-ch6

calib_packv5_042523_0143.root, FC#1, port C1

Entries	2
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U7-ch7

calib_packv5_042523_0143.root, FC#1, port C1

Entries	7
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

ampl

Entry

B0L101S, U7-ch8

Turn on : 5.0000
Width   : 0.000
Height : 1.000

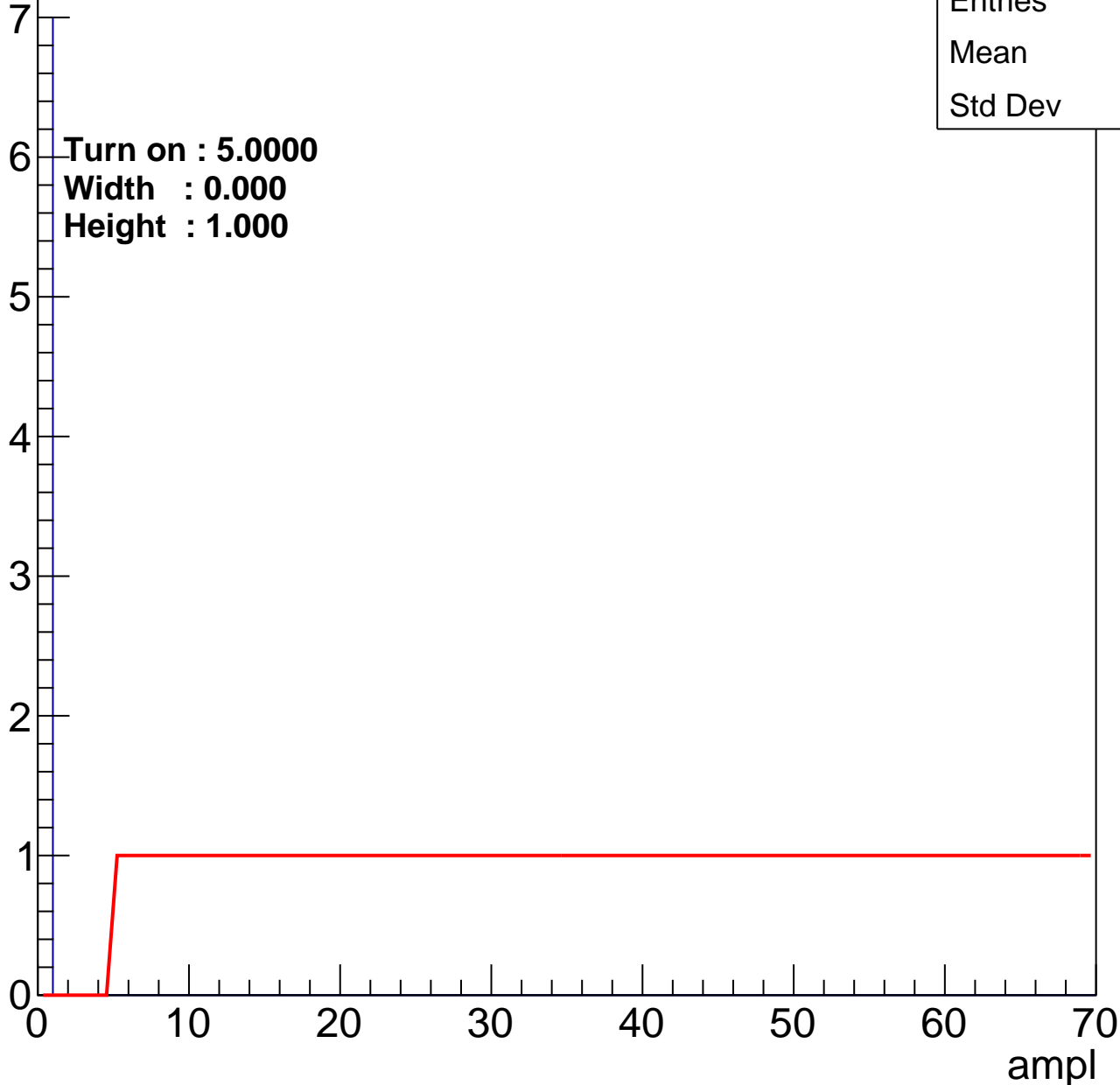|	
Entries	1
Mean	0
Std Dev	0

Entry

ampl
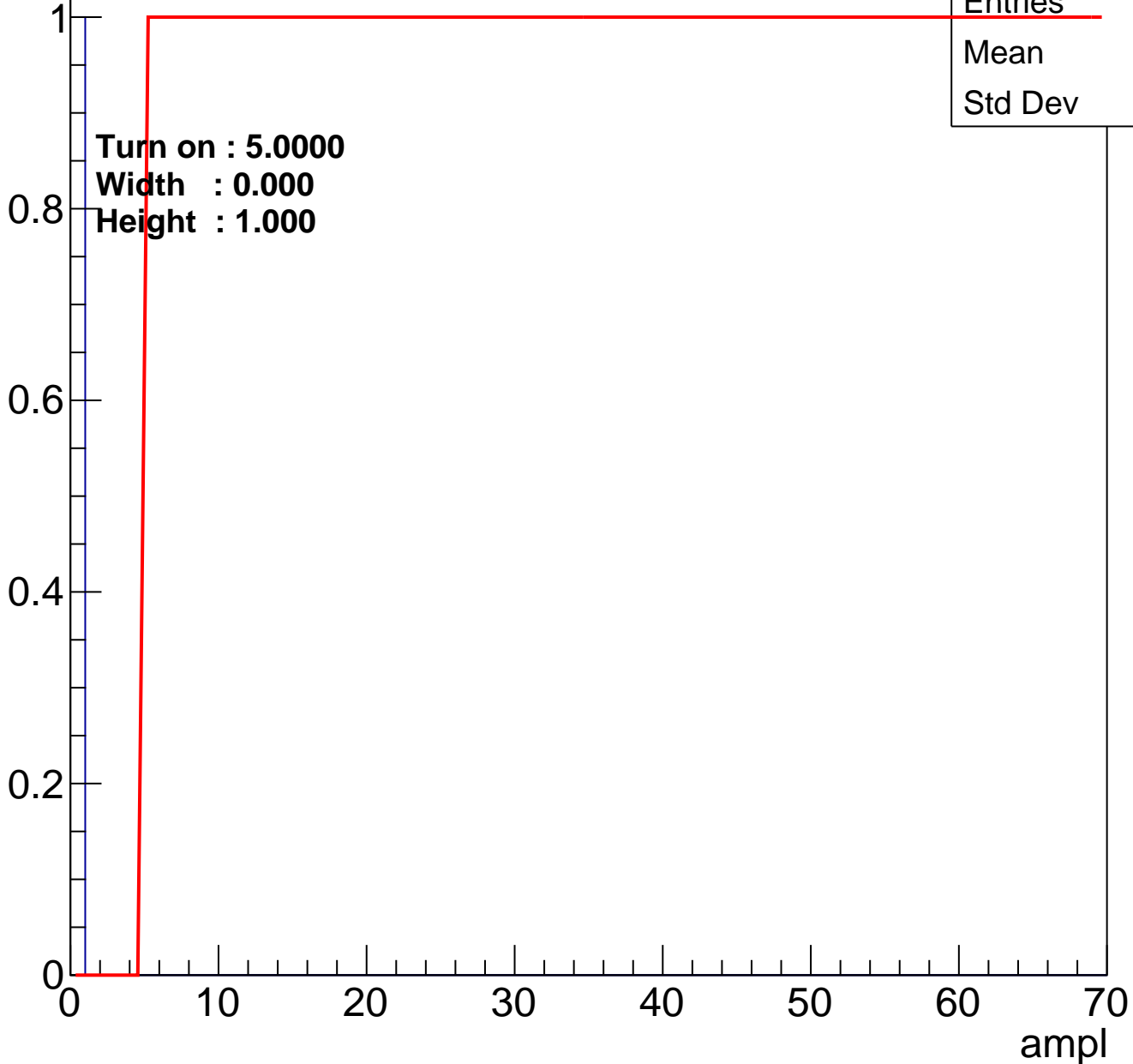
B0L101S, U7-ch9

calib_packv5_042523_0143.root, FC#1, port C1
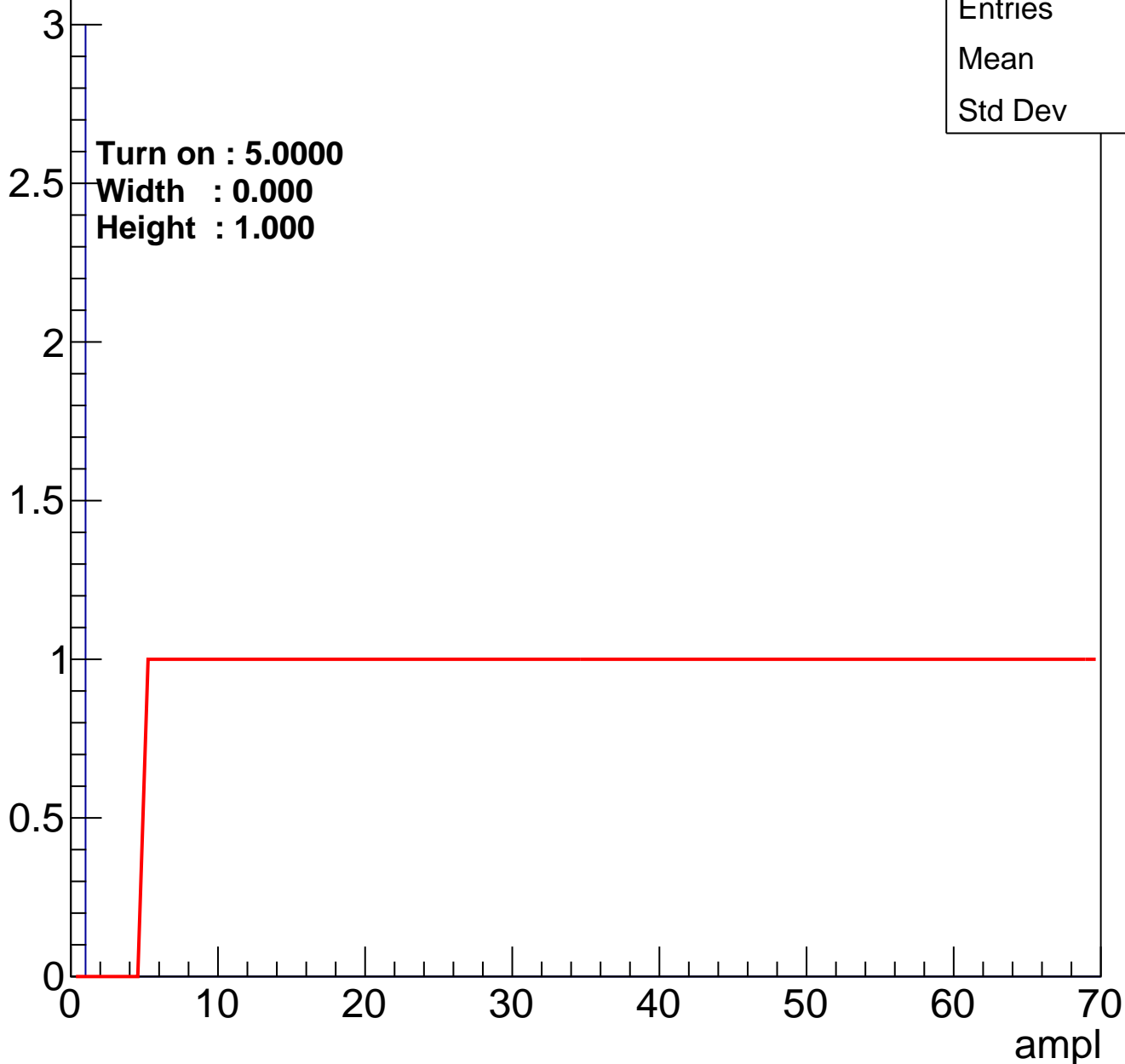
Entries	3
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

B0L101S, U7-ch10

Entry

Entries	1
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

ampl

B0L101S, U7-ch11

calib_packv5_042523_0143.root, FC#1, port C1

Entry

Entries	1
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

ampl

B0L101S, U7-ch12

Entry

Entries		0
Mean		0
Std Dev		0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

ampl

B0L101S, U7-ch13

calib_packv5_042523_0143.root, FC#1, port C1

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B0L101S, U7-ch14

calib_packv5_042523_0143.root, FC#1, port C1

Entry

Entries	3
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

ampl
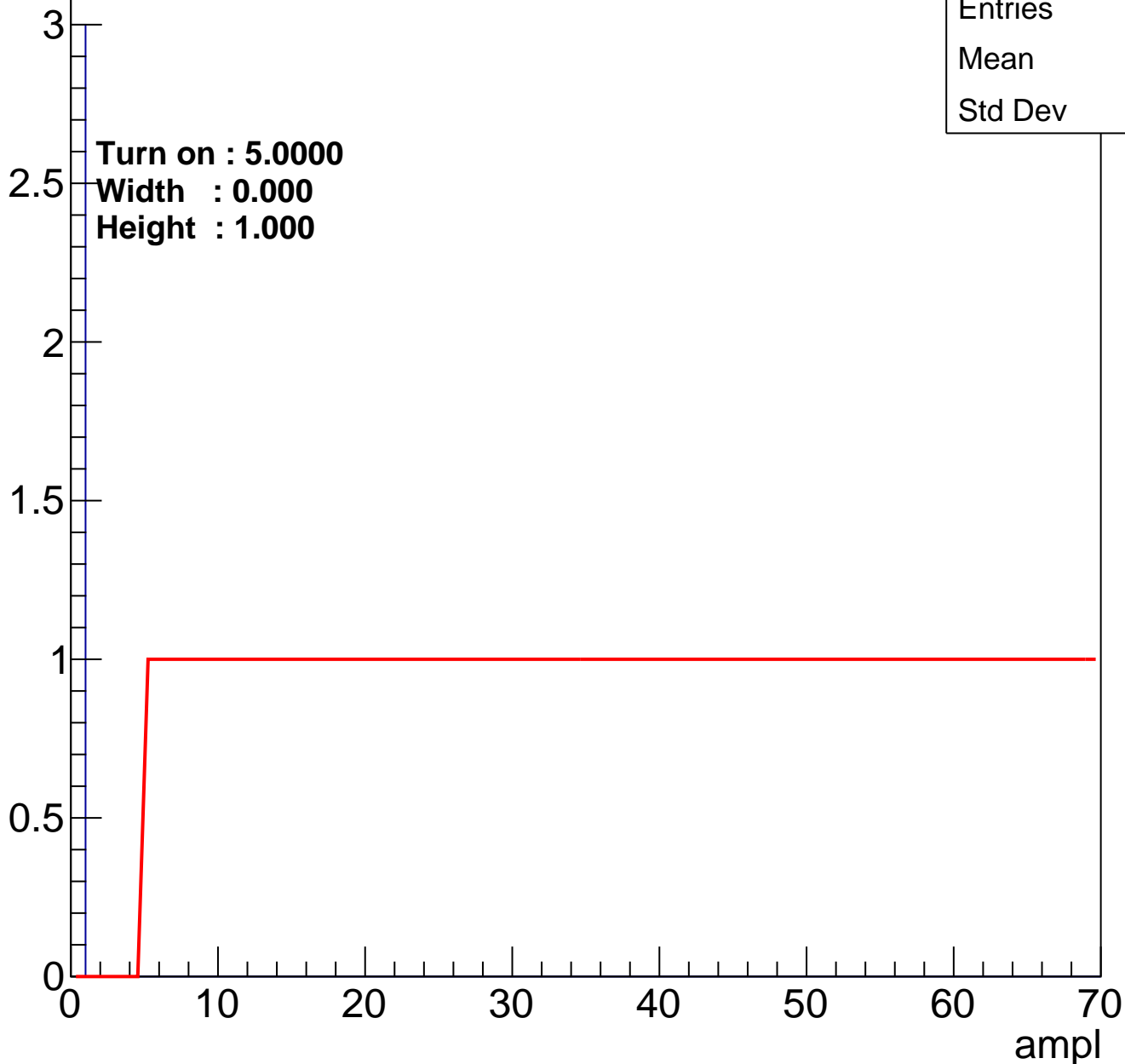
B0L101S, U7-ch15

calib_packv5_042523_0143.root, FC#1, port C1

Entries	1
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U7-ch16

calib_packv5_042523_0143.root, FC#1, port C1

Entries	2
Mean	0
Std Dev	0

Turn on : 5.0000
Width : 0.000
Height : 1.000

Entry

ampl

B0L101S, U7-ch17

calib_packv5_042523_0143.root, FC#1, port C1

Entries	1
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U7-ch18

calib_packv5_042523_0143.root, FC#1, port C1

Entries	0
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U7-ch19

calib_packv5_042523_0143.root, FC#1, port C1

Turn on : 5.0000
Width   : 0.000
Height : 1.000
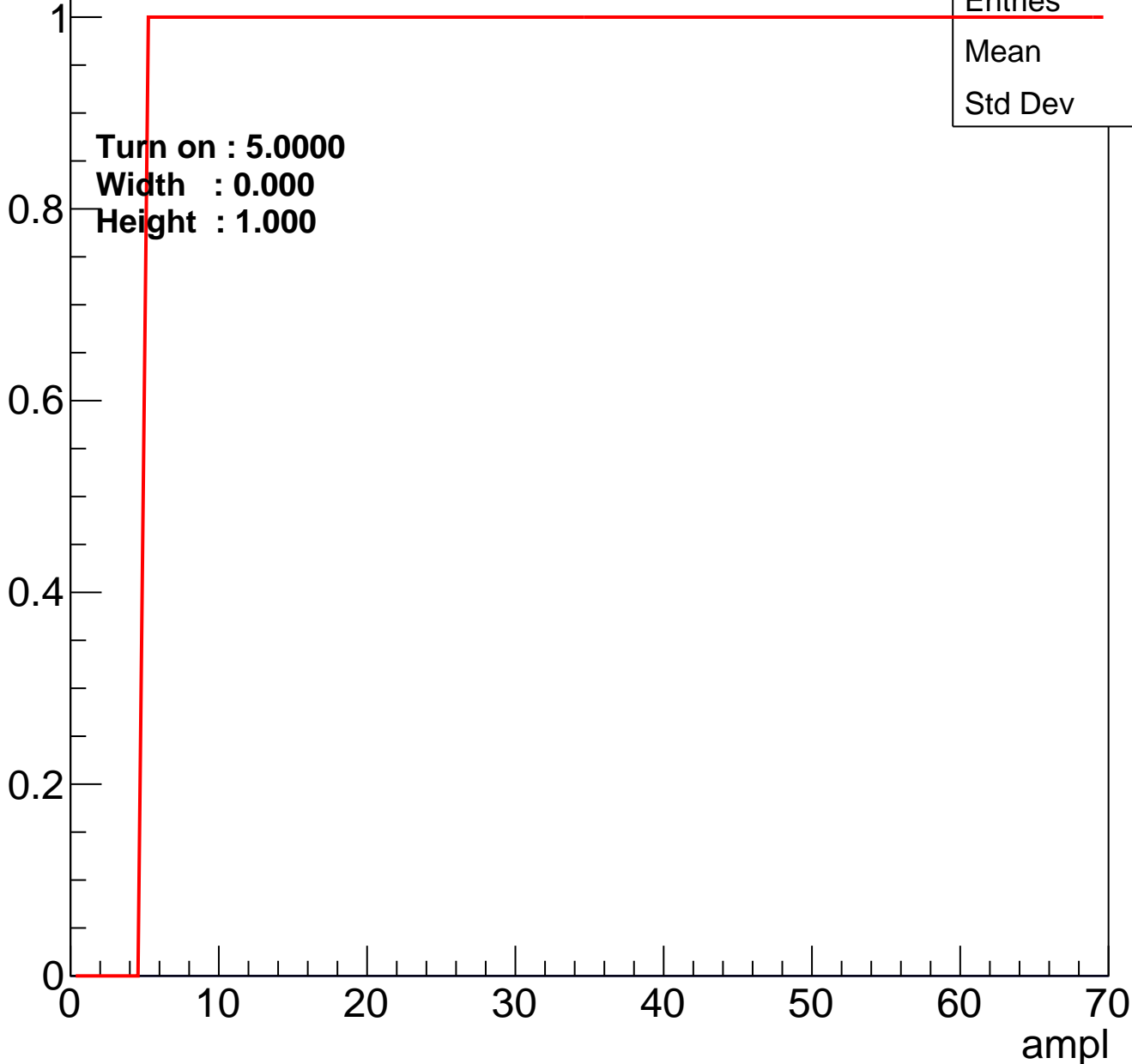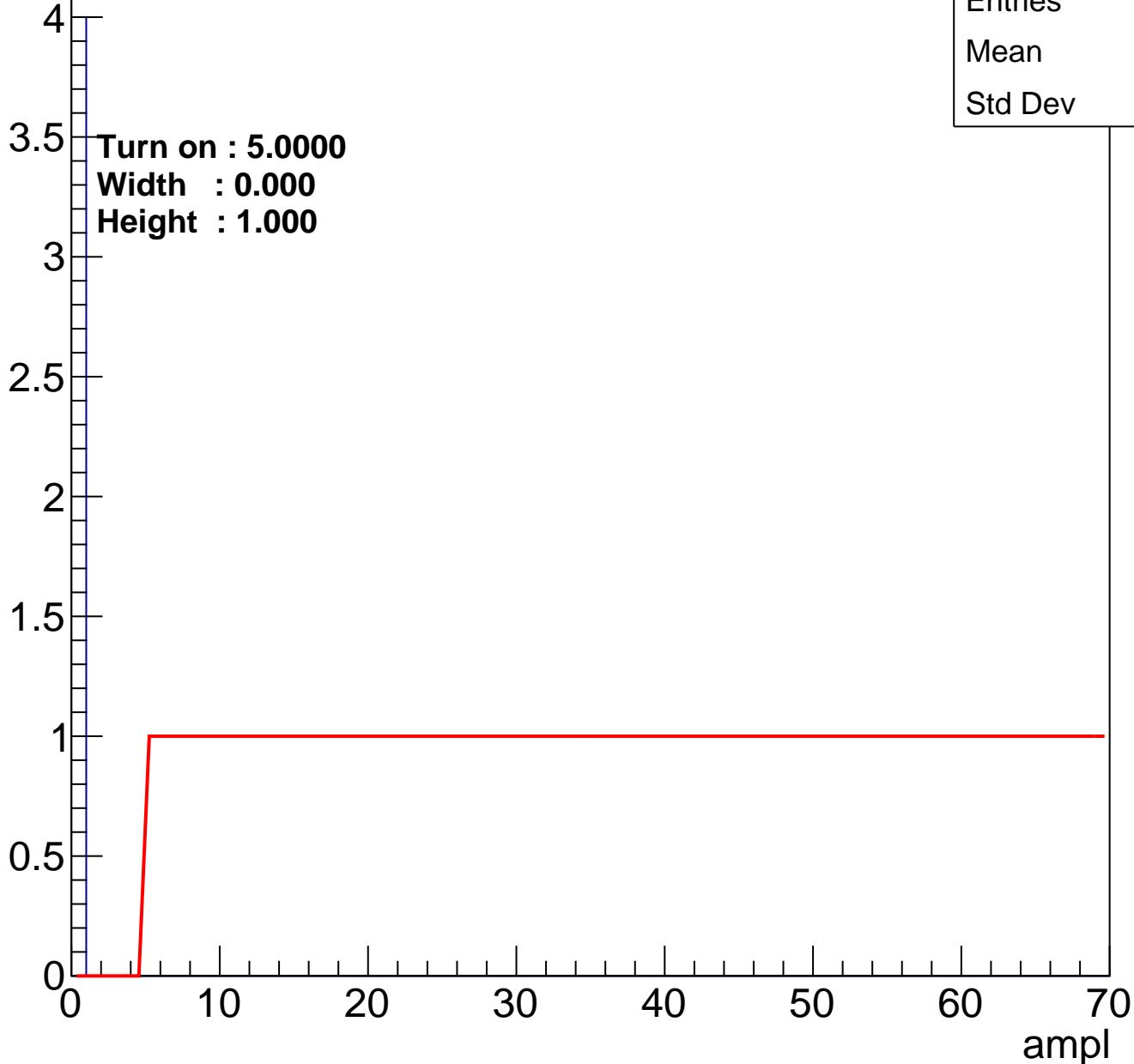
Entries	0
Mean	0
Std Dev	0

B0L101S, U7-ch20

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entries	4
Mean	0
Std Dev	0

B0L101S, U7-ch21

calib_packv5_042523_0143.root, FC#1, port C1

Entries	0
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U7-ch22

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B0L101S, U7-ch23

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entries	1
Mean	0
Std Dev	0

B0L101S, U7-ch24

calib_packv5_042523_0143.root, FC#1, port C1

Entry

Entries	1
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

ampl

B0L101S, U7-ch25

calib_packv5_042523_0143.root, FC#1, port C1

Entries	2
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl
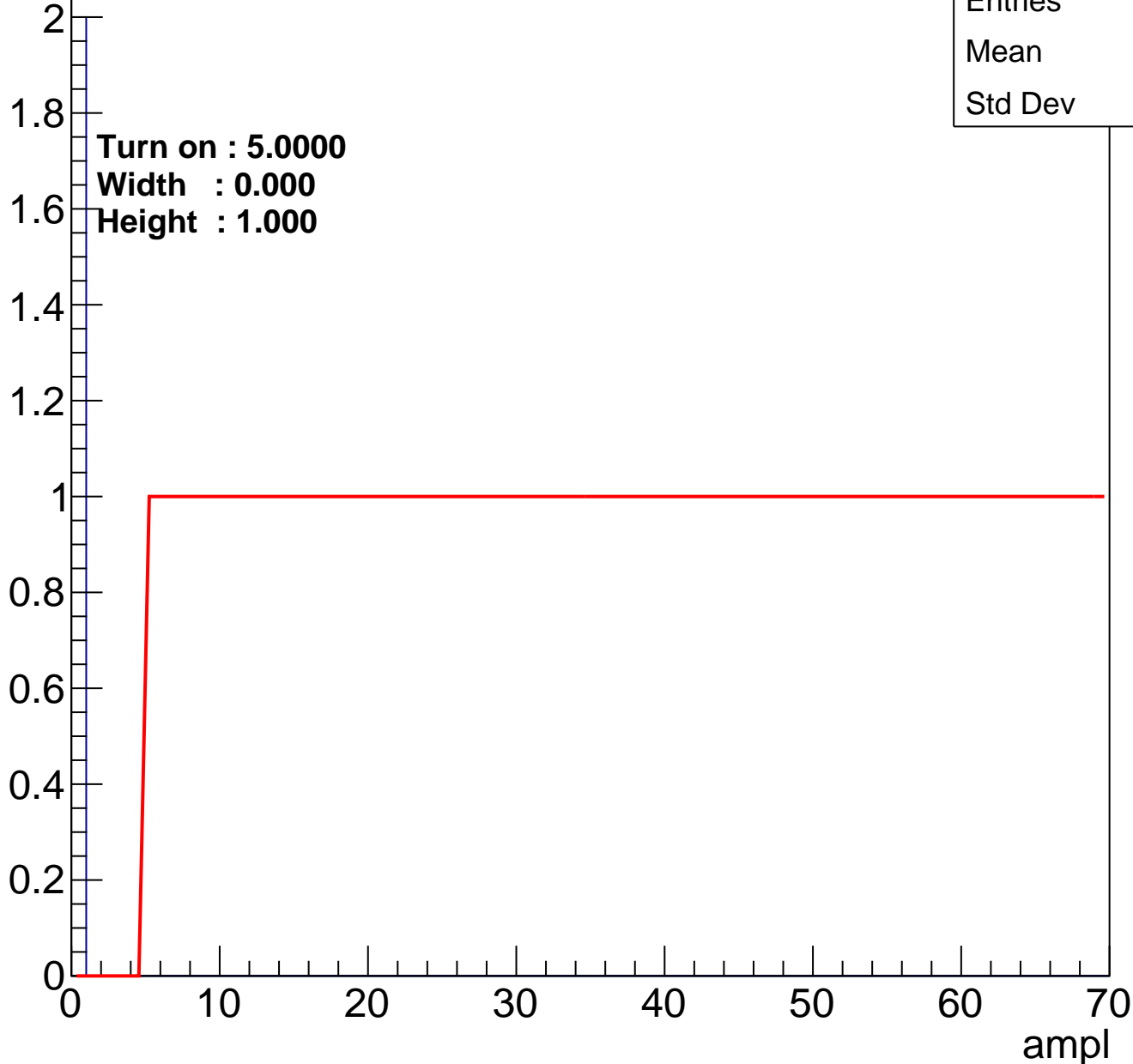
B0L101S, U7-ch26

calib_packv5_042523_0143.root, FC#1, port C1

Entries	0
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl
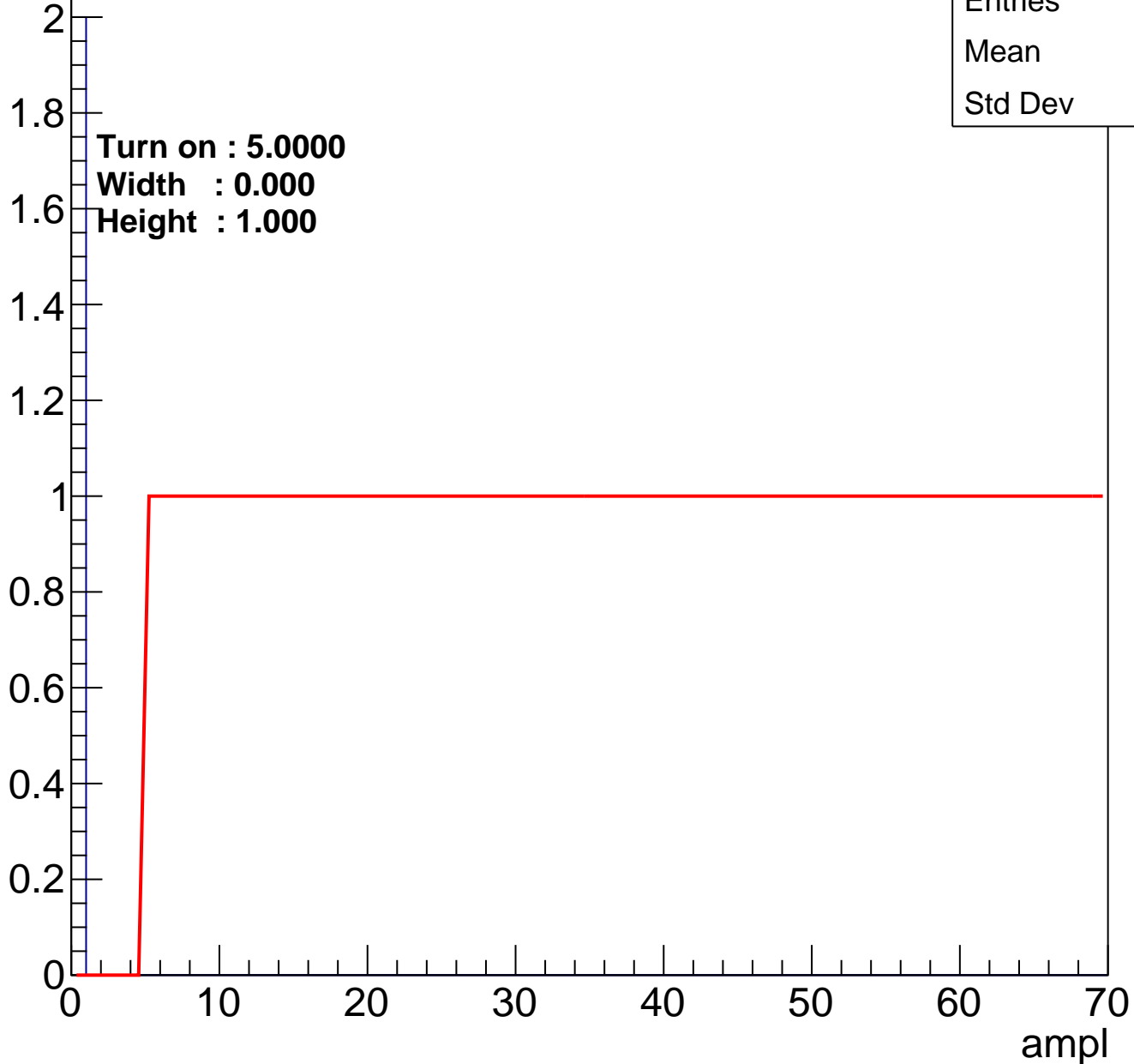
B0L101S, U7-ch27

calib_packv5_042523_0143.root, FC#1, port C1

Entries	2
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U7-ch28

calib_packv5_042523_0143.root, FC#1, port C1

Entries	1
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

B0L101S, U7-ch29

calib_packv5_042523_0143.root, FC#1, port C1

Entry

Entries	0
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

ampl
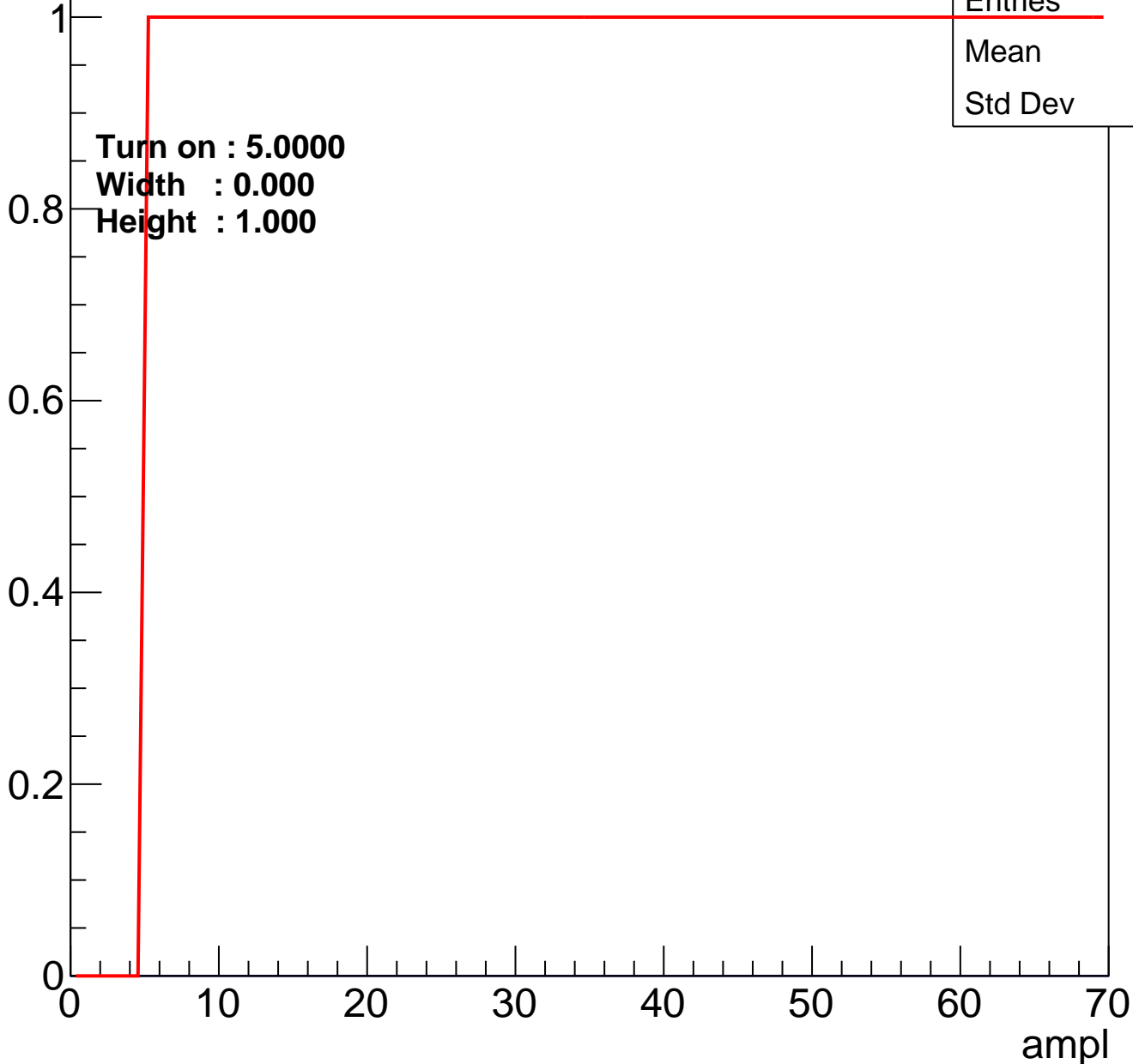
B0L101S, U7-ch30

calib_packv5_042523_0143.root, FC#1, port C1

Entries	4
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000
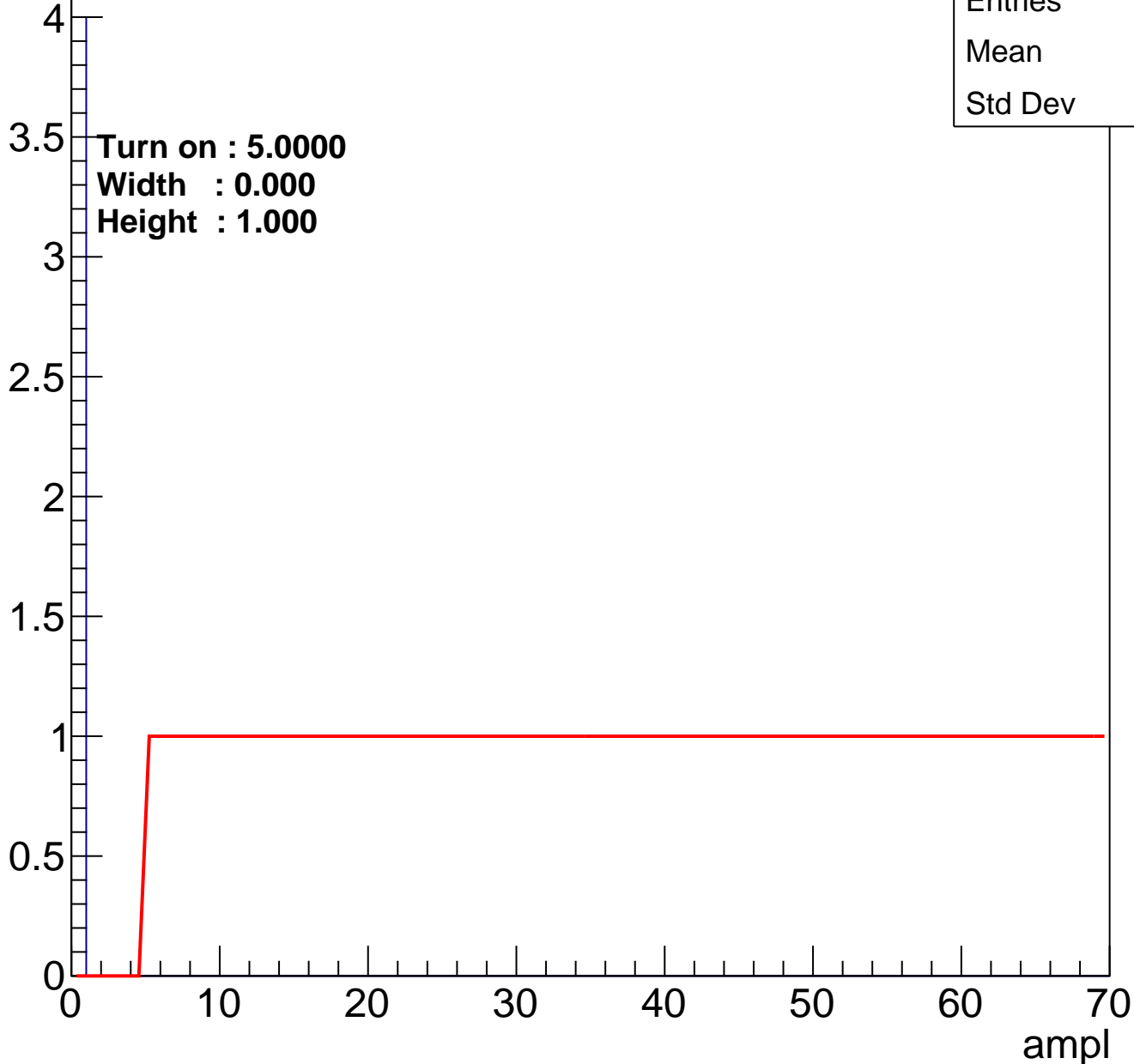
B0L101S, U7-ch31

calib_packv5_042523_0143.root, FC#1, port C1

Entries	1
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

B0L101S, U7-ch32

calib_packv5_042523_0143.root, FC#1, port C1

Entries	0
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U7-ch33

calib_packv5_042523_0143.root, FC#1, port C1

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

	Entries	0
	Mean	0
	Std Dev	0

B0L101S, U7-ch34

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entries	1
Mean	0
Std Dev	0

Entry

ampl

B0L101S, U7-ch35

calib_packv5_042523_0143.root, FC#1, port C1

Entries	0
Mean	0
Std Dev	0
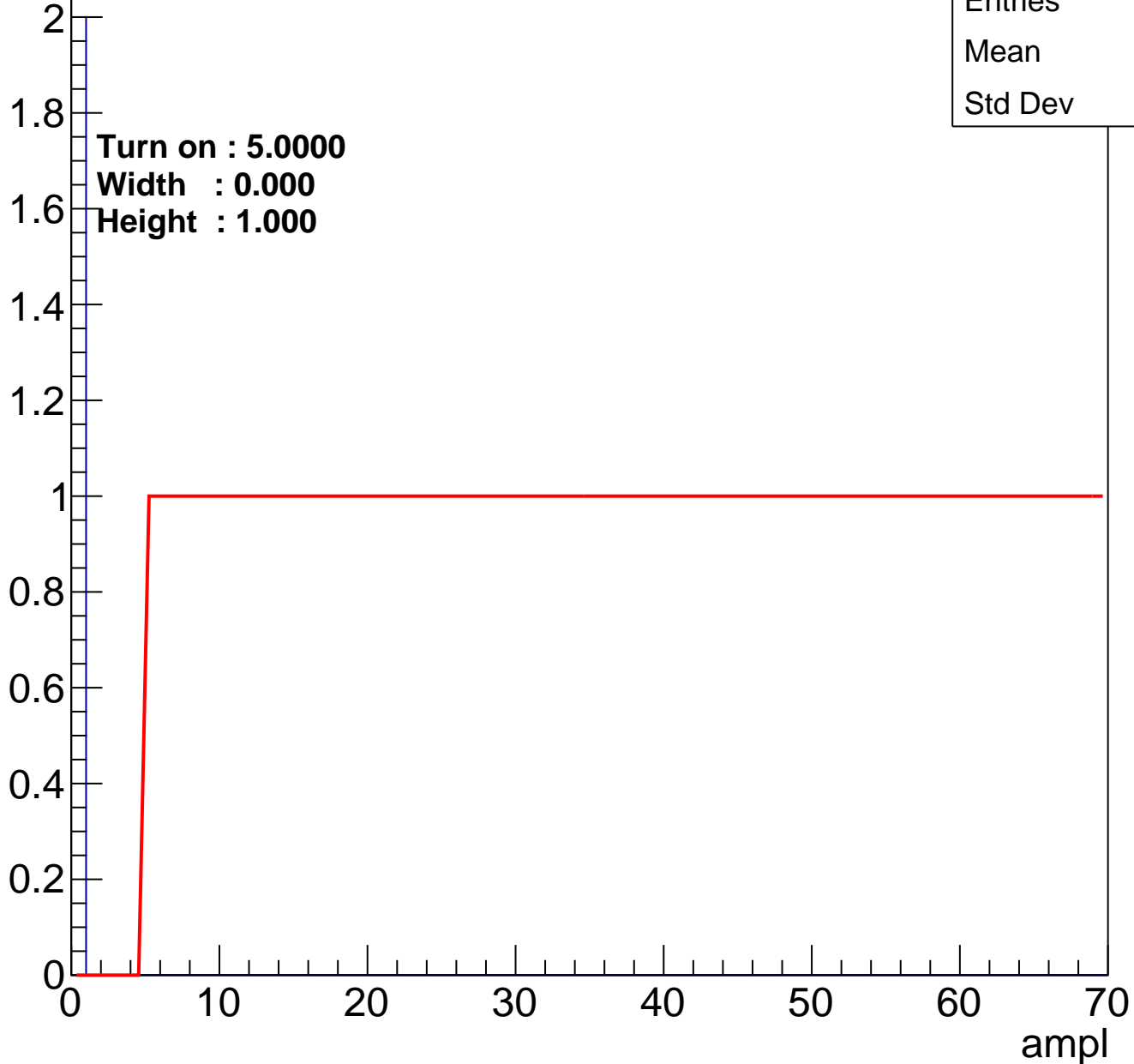
Turn on : 5.0000
Width   : 0.000
Height : 1.000

B0L101S, U7-ch36

calib_packv5_042523_0143.root, FC#1, port C1

Entries	2
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U7-ch37

calib_packv5_042523_0143.root, FC#1, port C1

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entries	2
Mean	0
Std Dev	0

Entry

ampl

B0L101S, U7-ch38

calib_packv5_042523_0143.root, FC#1, port C1

Entries	2
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U7-ch39

calib_packv5_042523_0143.root, FC#1, port C1

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B0L101S, U7-ch40

calib_packv5_042523_0143.root, FC#1, port C1

Entry

Entries	0
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

ampl
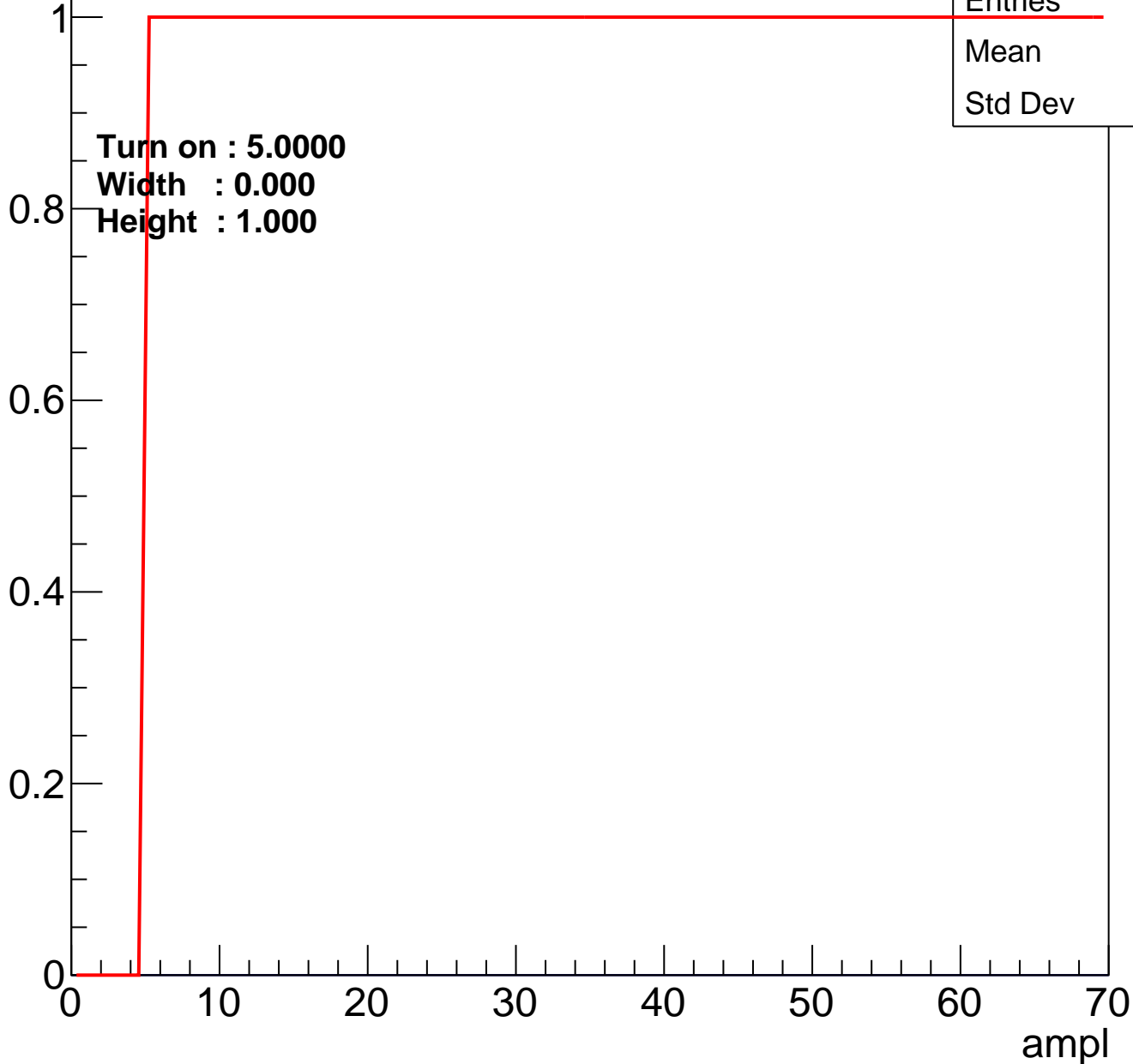
B0L101S, U7-ch41

calib_packv5_042523_0143.root, FC#1, port C1

Entries		0
Mean		0
Std Dev		0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U7-ch42

calib_packv5_042523_0143.root, FC#1, port C1

Entry

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entries	2
Mean	0
Std Dev	0

ampl
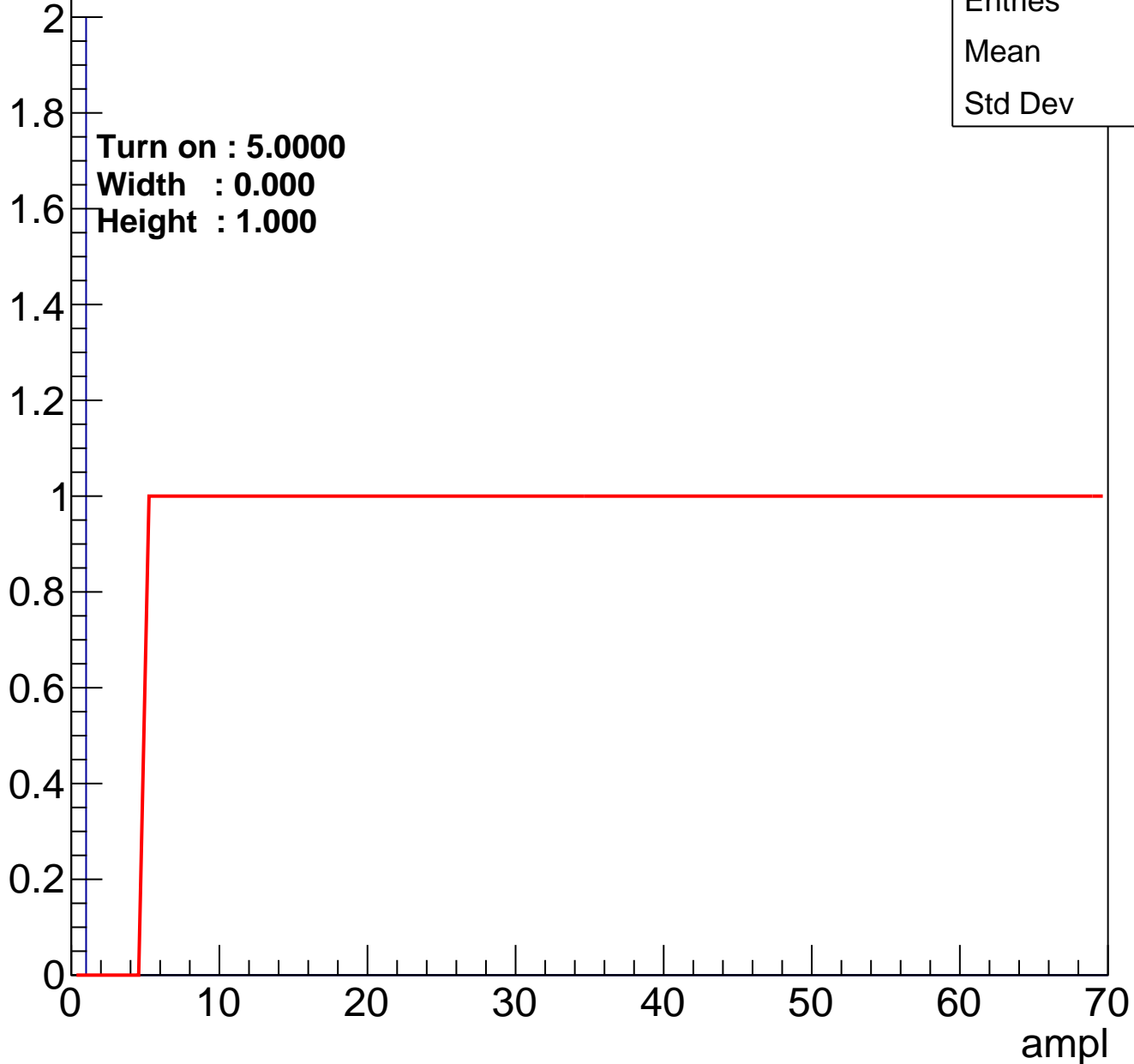
B0L101S, U7-ch43

calib_packv5_042523_0143.root, FC#1, port C1

Entries	2
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl
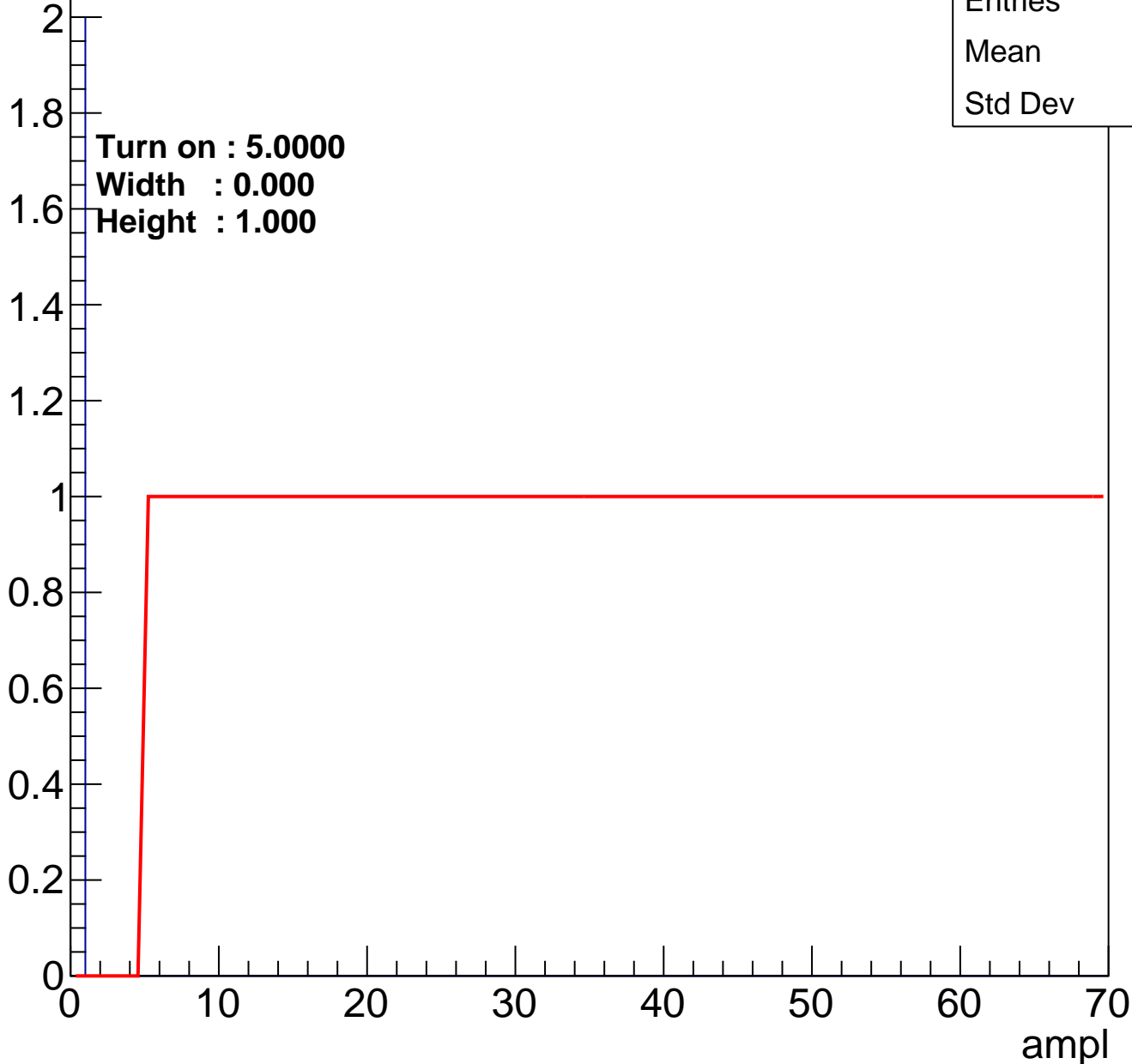
B0L101S, U7-ch44

calib_packv5_042523_0143.root, FC#1, port C1

Entries	0
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U7-ch45

Entries	1
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U7-ch46

calib_packv5_042523_0143.root, FC#1, port C1

Entry

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entries	2
Mean	0
Std Dev	0

ampl
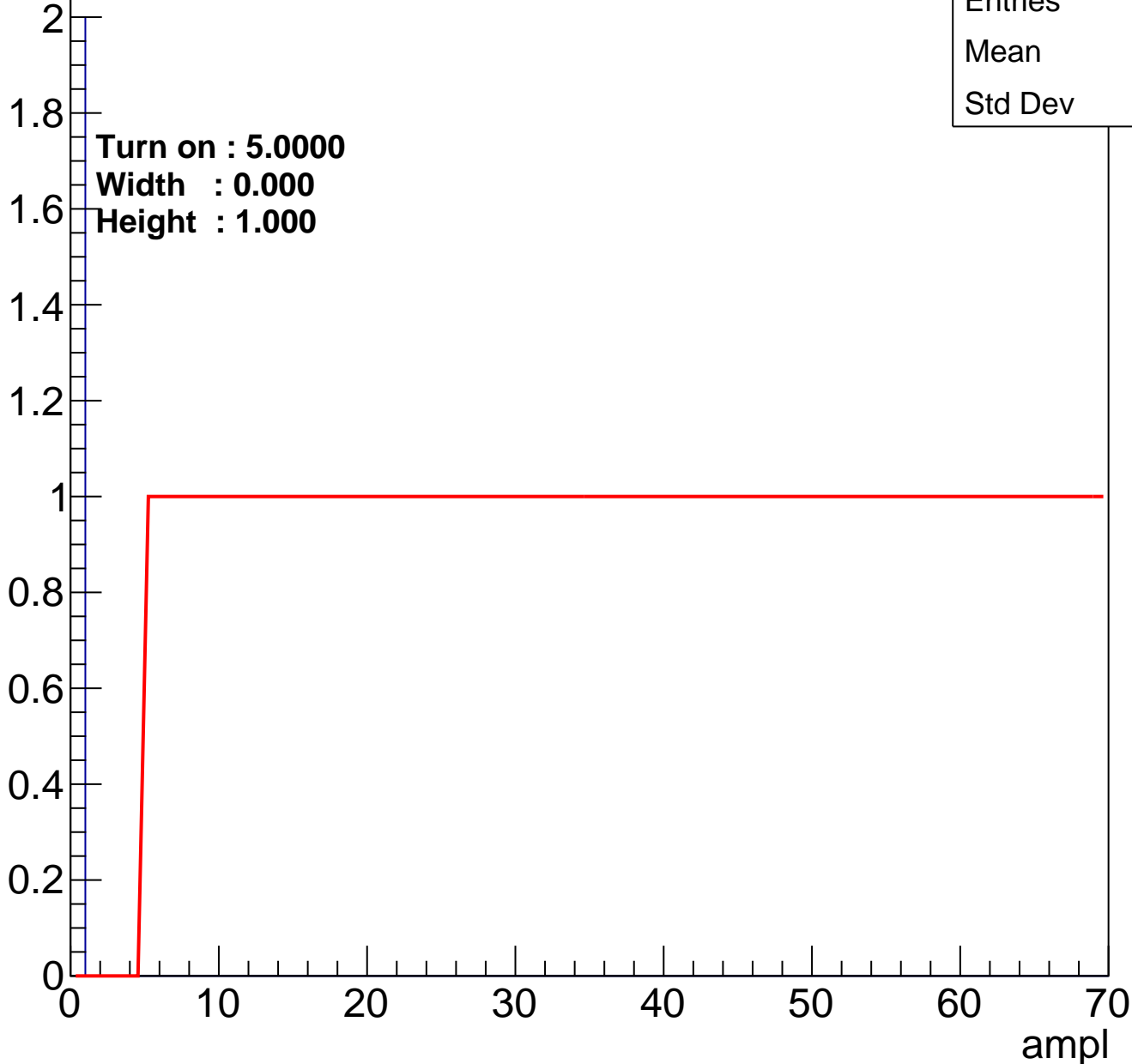
B0L101S, U7-ch47

calib_packv5_042523_0143.root, FC#1, port C1

Entries	1
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

B0L101S, U7-ch48

Entry

Entries	0
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

ampl

B0L101S, U7-ch49

calib_packv5_042523_0143.root, FC#1, port C1

Entries	2
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl
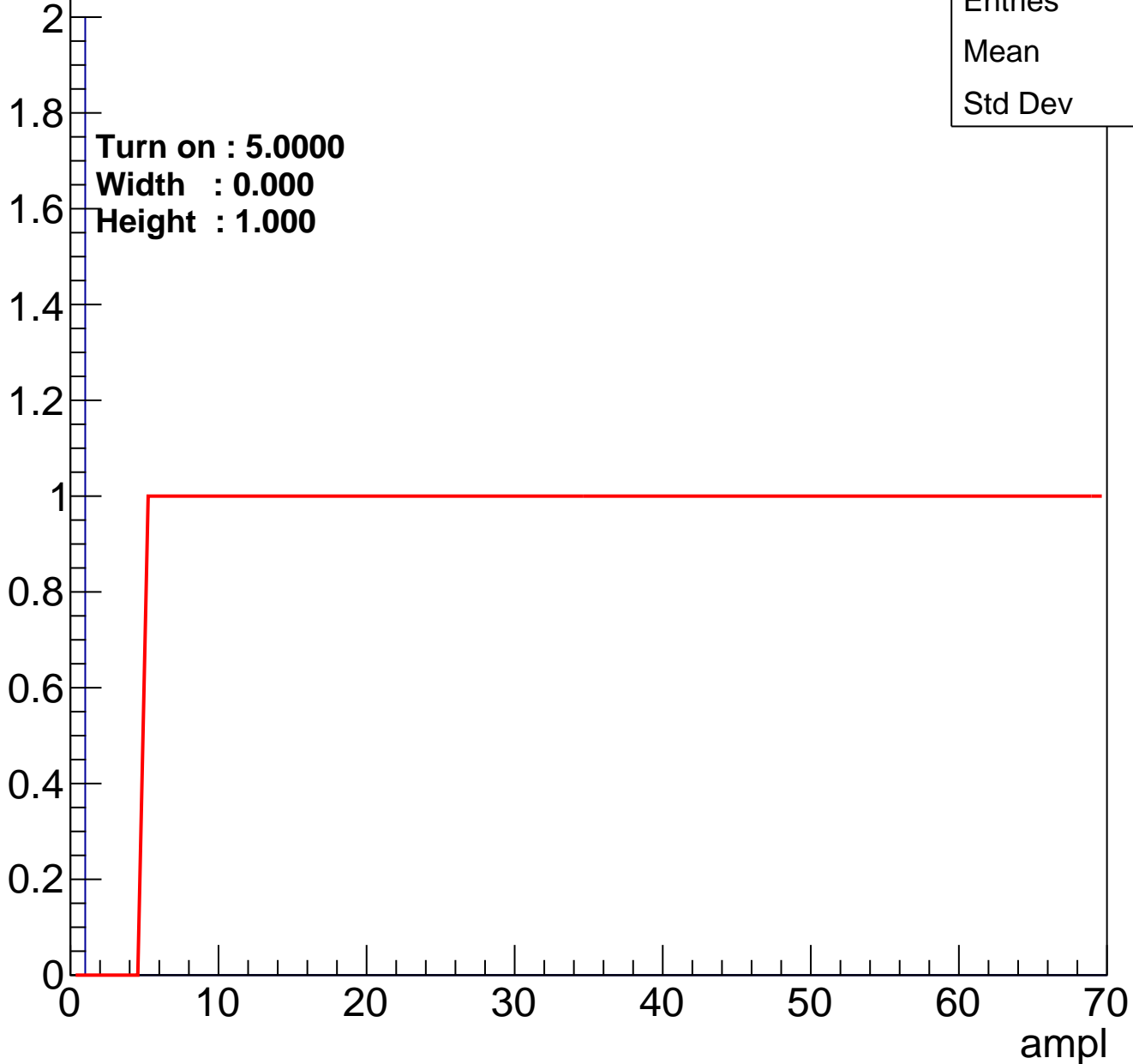
B0L101S, U7-ch50

calib_packv5_042523_0143.root, FC#1, port C1

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B0L101S, U7-ch51

calib_packv5_042523_0143.root, FC#1, port C1

Entry

Entries	0
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

ampl

B0L101S, U7-ch52

Entry

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entries	0
Mean	0
Std Dev	0

ampl

B0L101S, U7-ch54

calib_packv5_042523_0143.root, FC#1, port C1

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entries	2
Mean	0
Std Dev	0

Entry

ampl
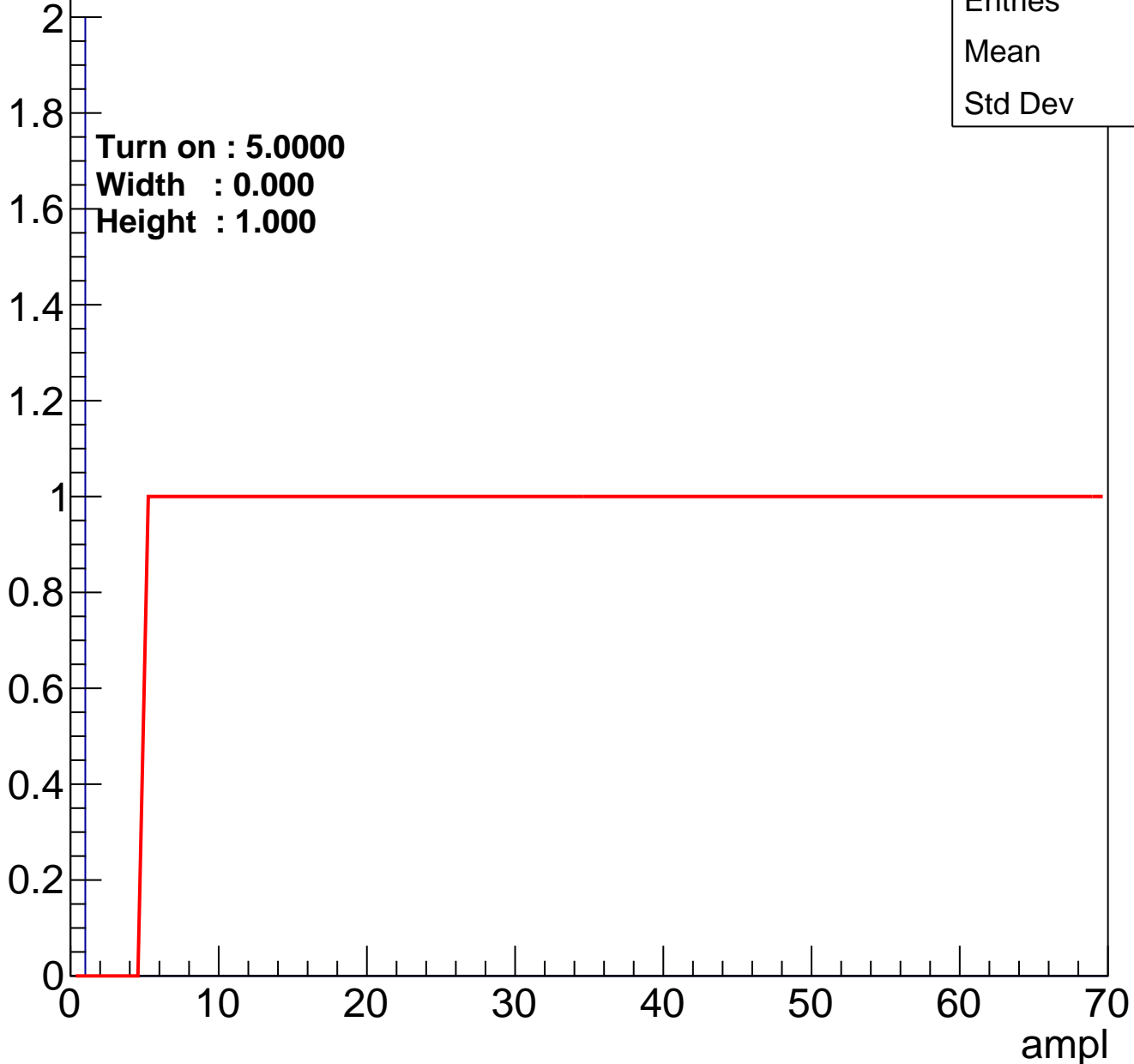
B0L101S, U7-ch55

calib_packv5_042523_0143.root, FC#1, port C1
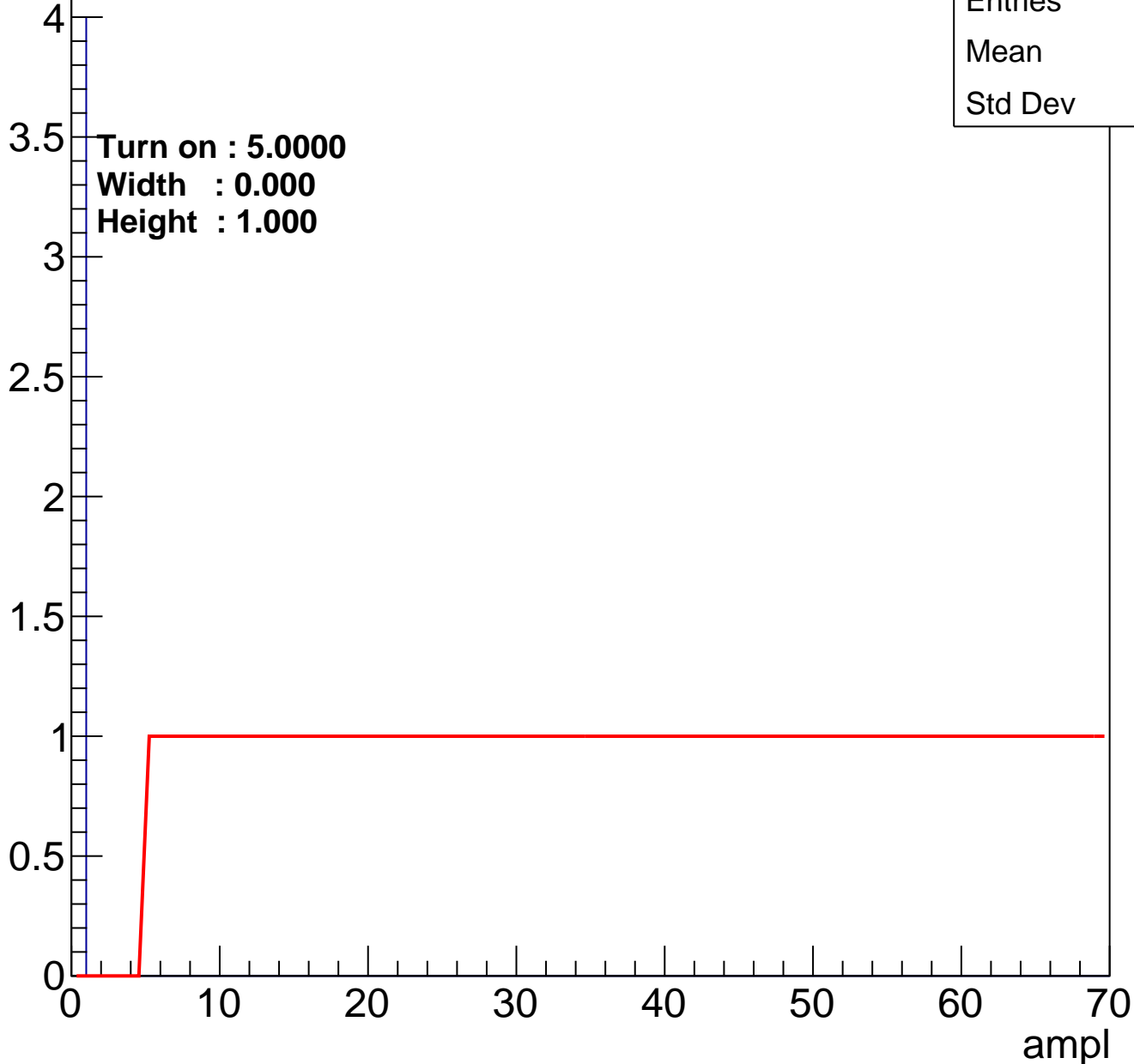
Entries	4
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U7-ch56

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entries	10
Mean	15.3
Std Dev	5.1

Entry

ampl
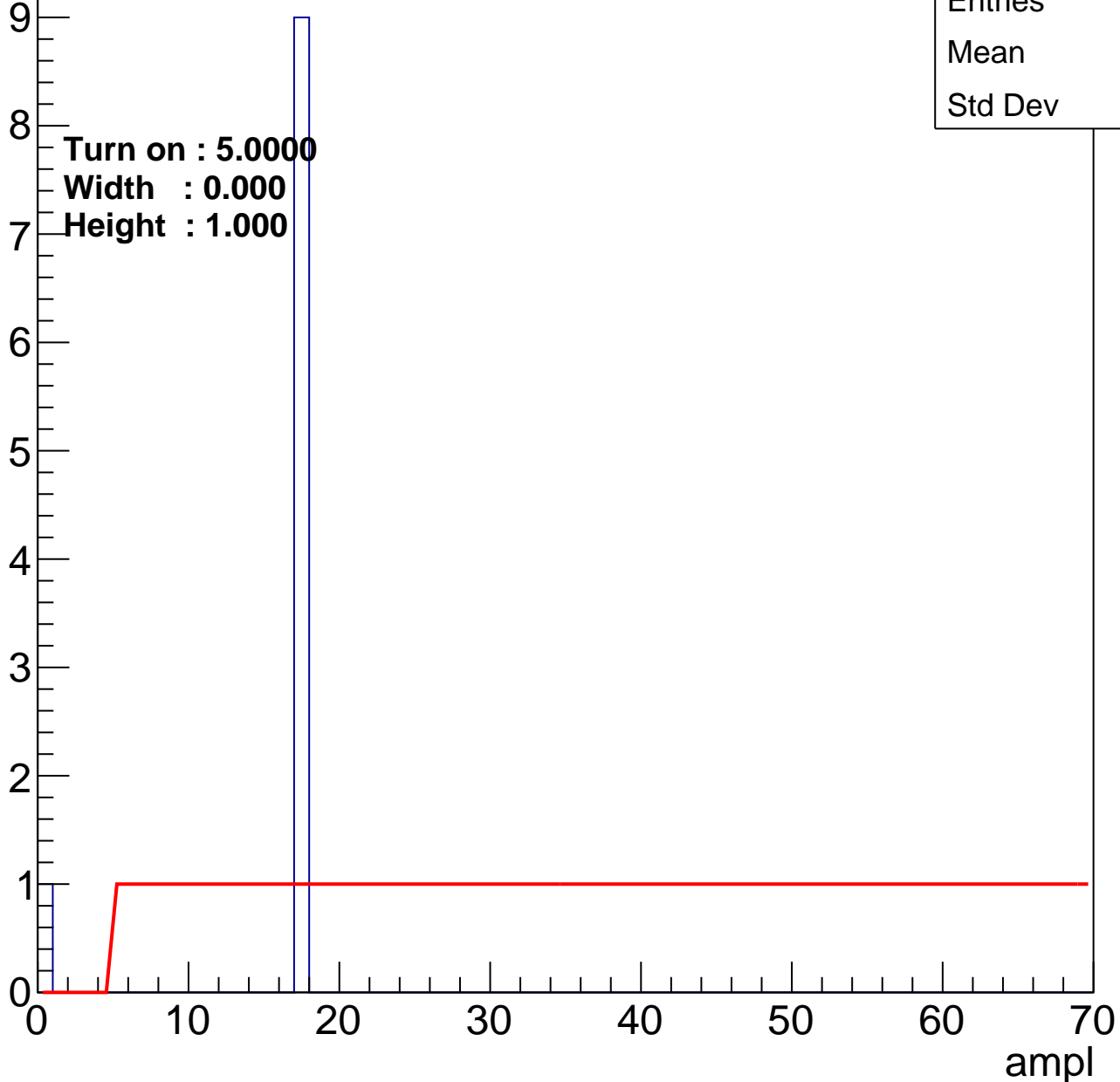
B0L101S, U7-ch57

calib_packv5_042523_0143.root, FC#1, port C1

Entry

Entries	1
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

ampl

B0L101S, U7-ch58

Entries	1
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl
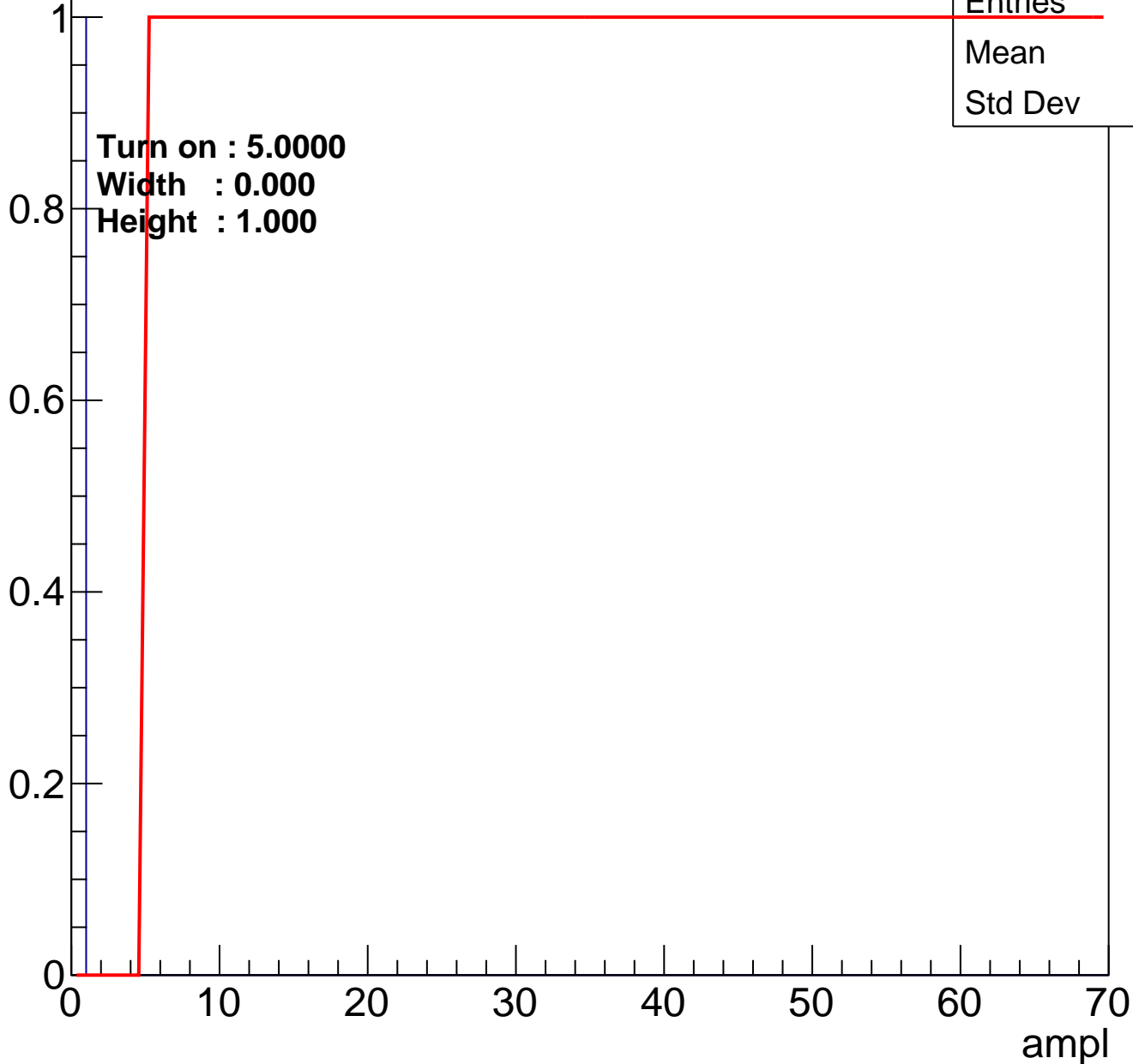
B0L101S, U7-ch59

calib_packv5_042523_0143.root, FC#1, port C1
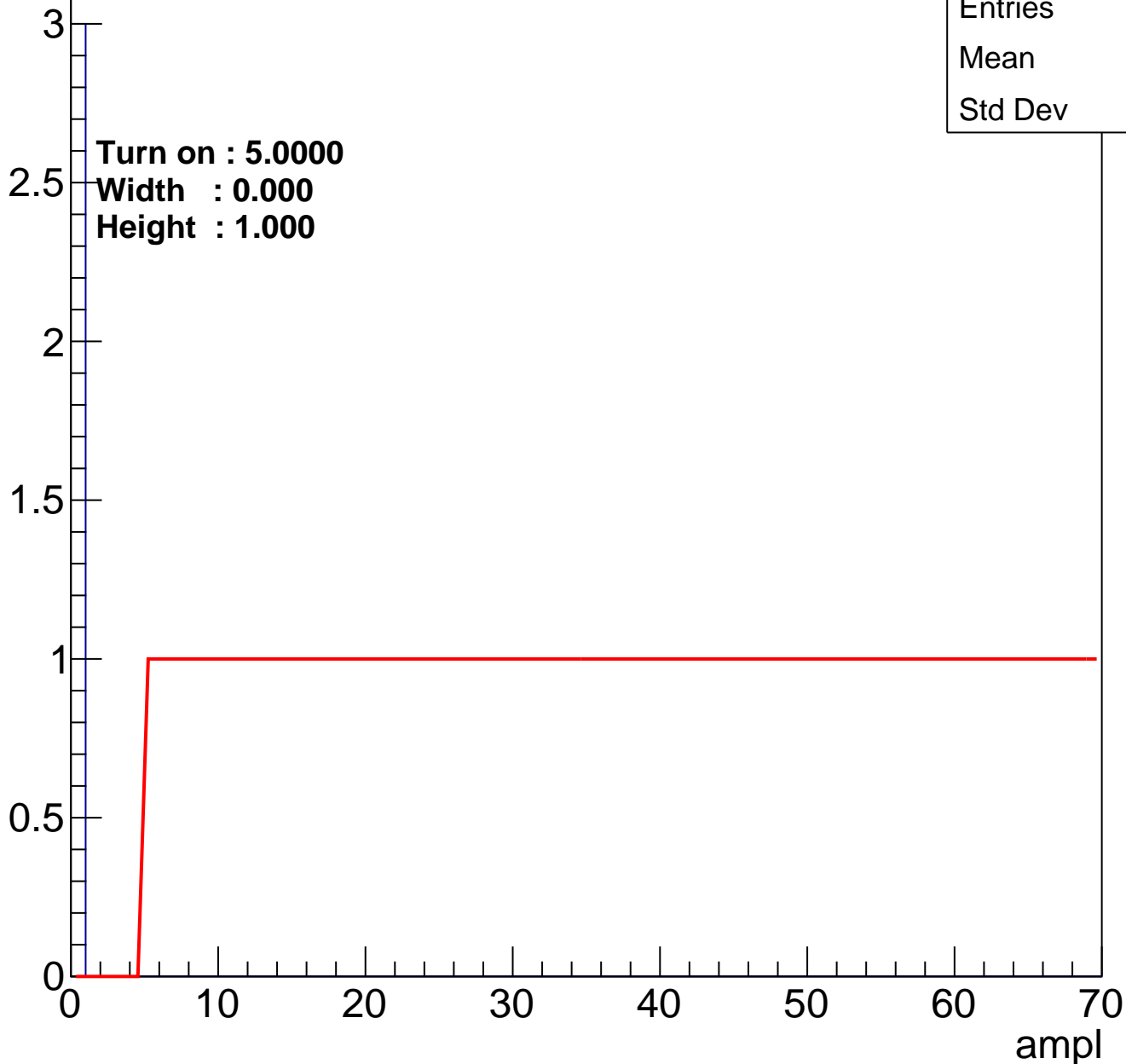
Entry

Entries	3
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

ampl

B0L101S, U7-ch60

Entry

Entries	1
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

ampl

B0L101S, U7-ch61

calib_packv5_042523_0143.root, FC#1, port C1

Entries	2
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U7-ch62
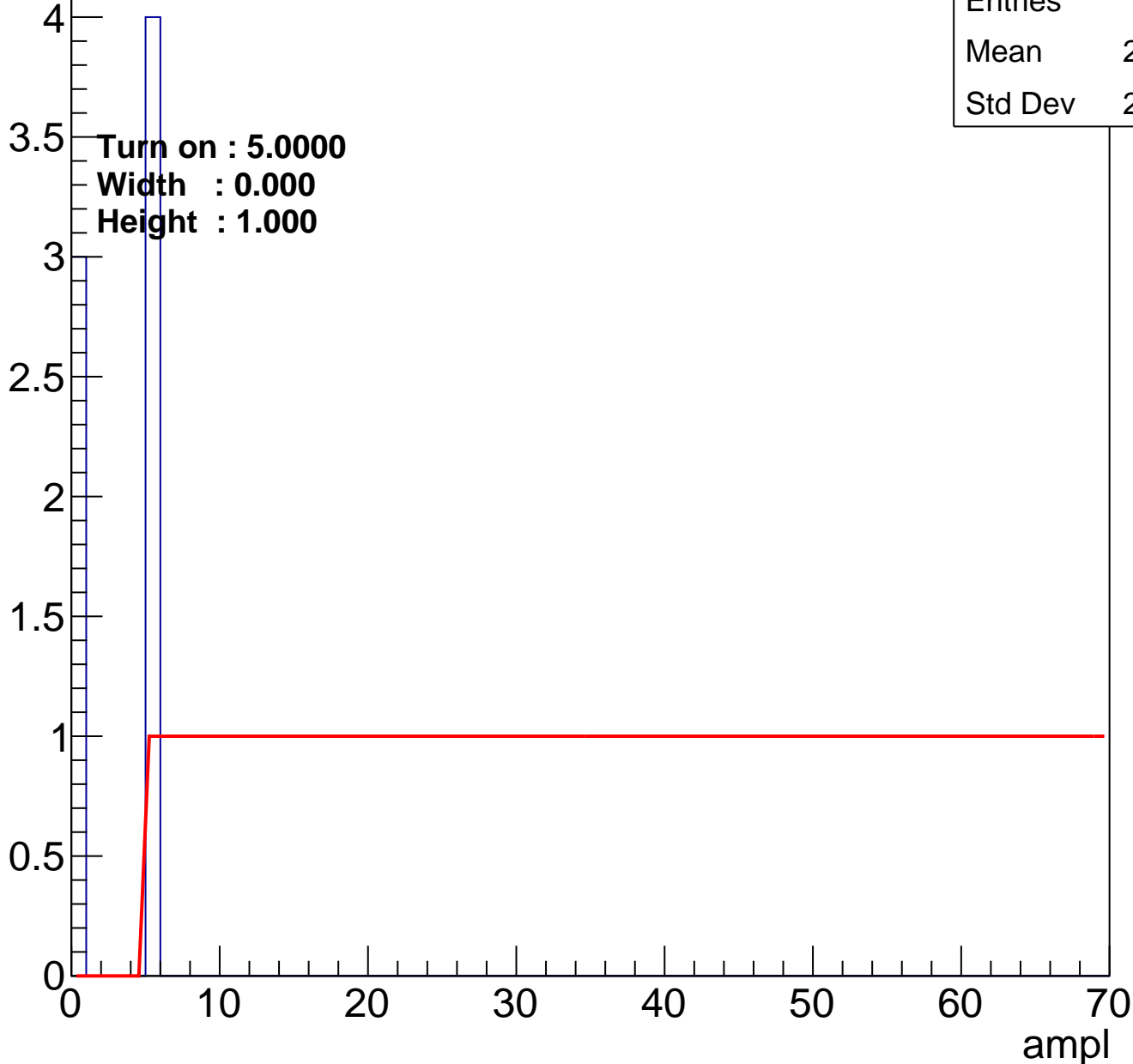
Entry

Entries	7
Mean	2.857
Std Dev	2.474

Turn on : 5.0000
Width   : 0.000
Height : 1.000

ampl

B0L101S, U7-ch63

calib_packv5_042523_0143.root, FC#1, port C1

Entry

Entries	0
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

ampl
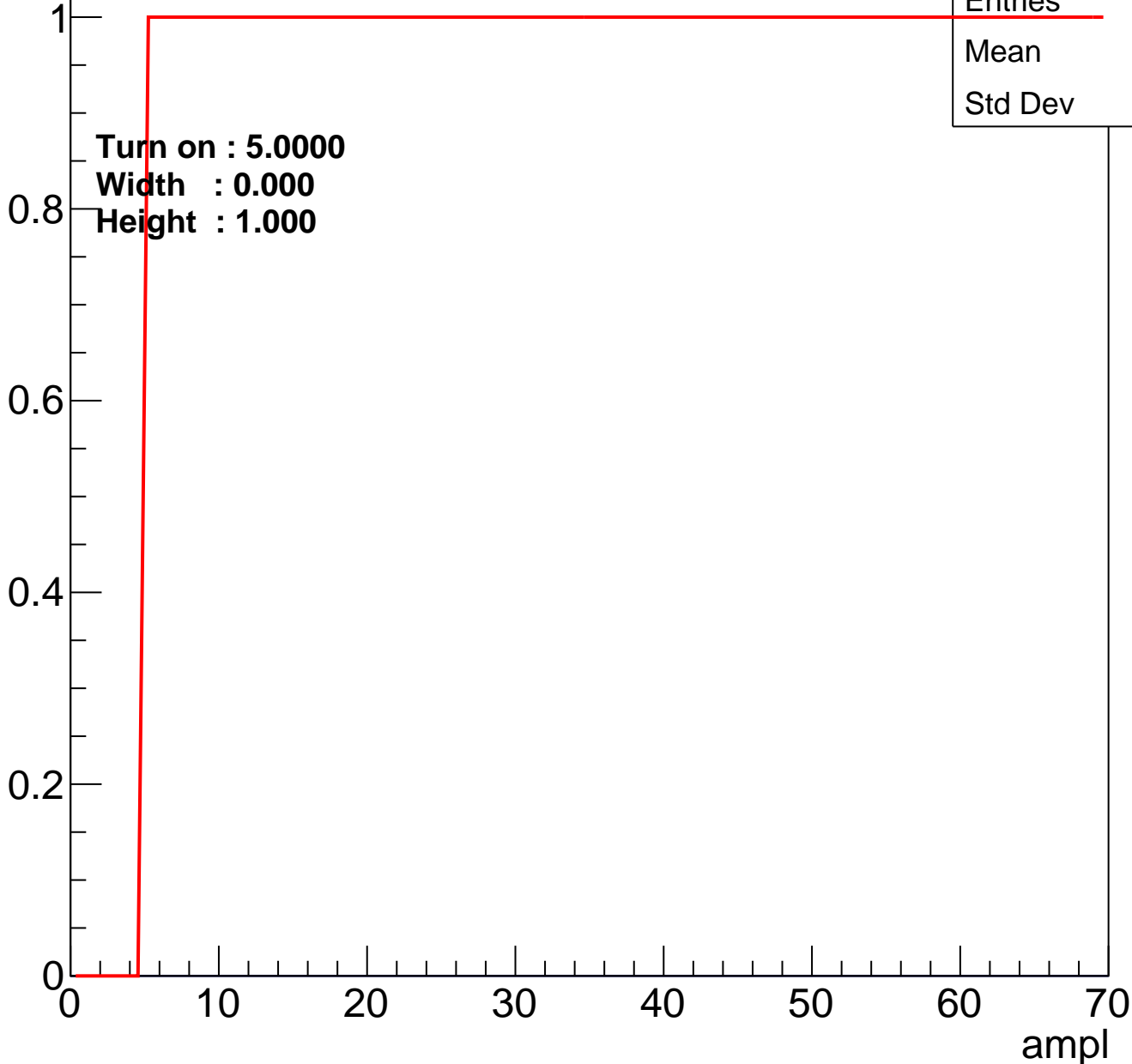
B0L101S, U7-ch64

calib_packv5_042523_0143.root, FC#1, port C1

Entries	0
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U7-ch65

calib_packv5_042523_0143.root, FC#1, port C1

Turn on : 5.0000
Width   : 0.000
Height : 1.000
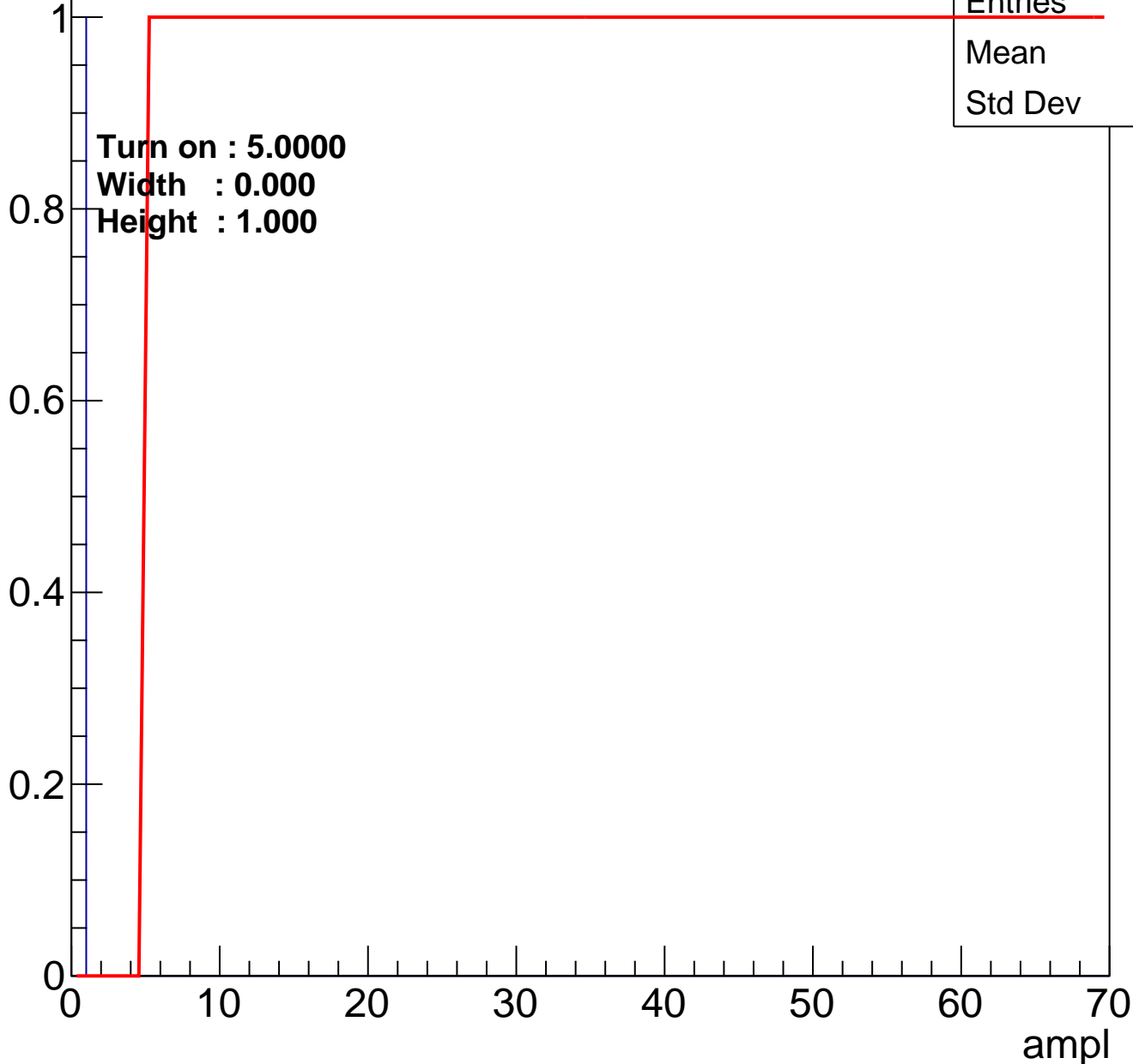
	Entries	1
	Mean	0
	Std Dev	0

B0L101S, U7-ch66

calib_packv5_042523_0143.root, FC#1, port C1

Entries	3
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl
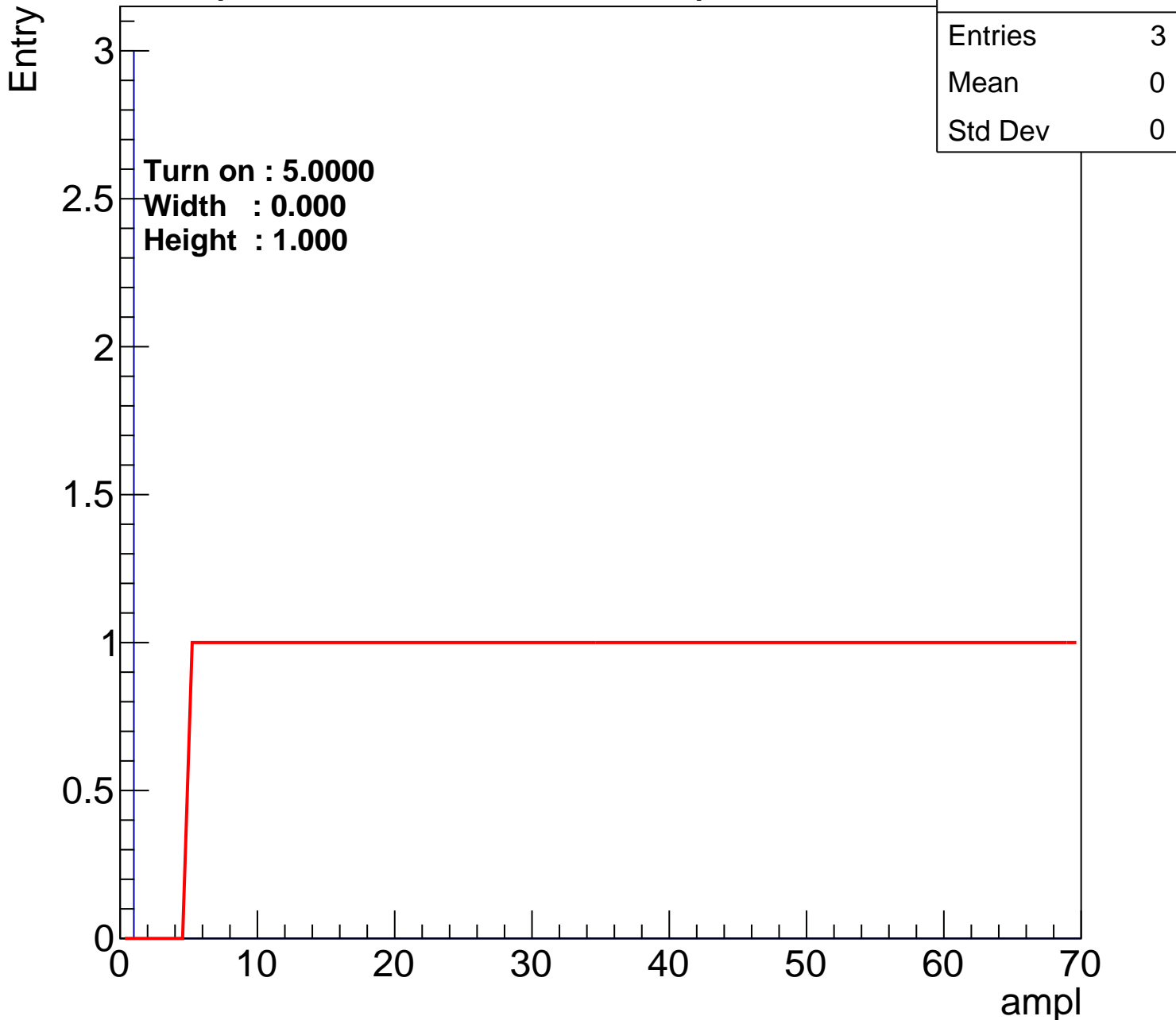
B0L101S, U7-ch67

calib_packv5_042523_0143.root, FC#1, port C1

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entries	2
Mean	0
Std Dev	0

Entry

ampl

B0L101S, U7-ch68

calib_packv5_042523_0143.root, FC#1, port C1

Entries	4
Mean	0
Std Dev	0
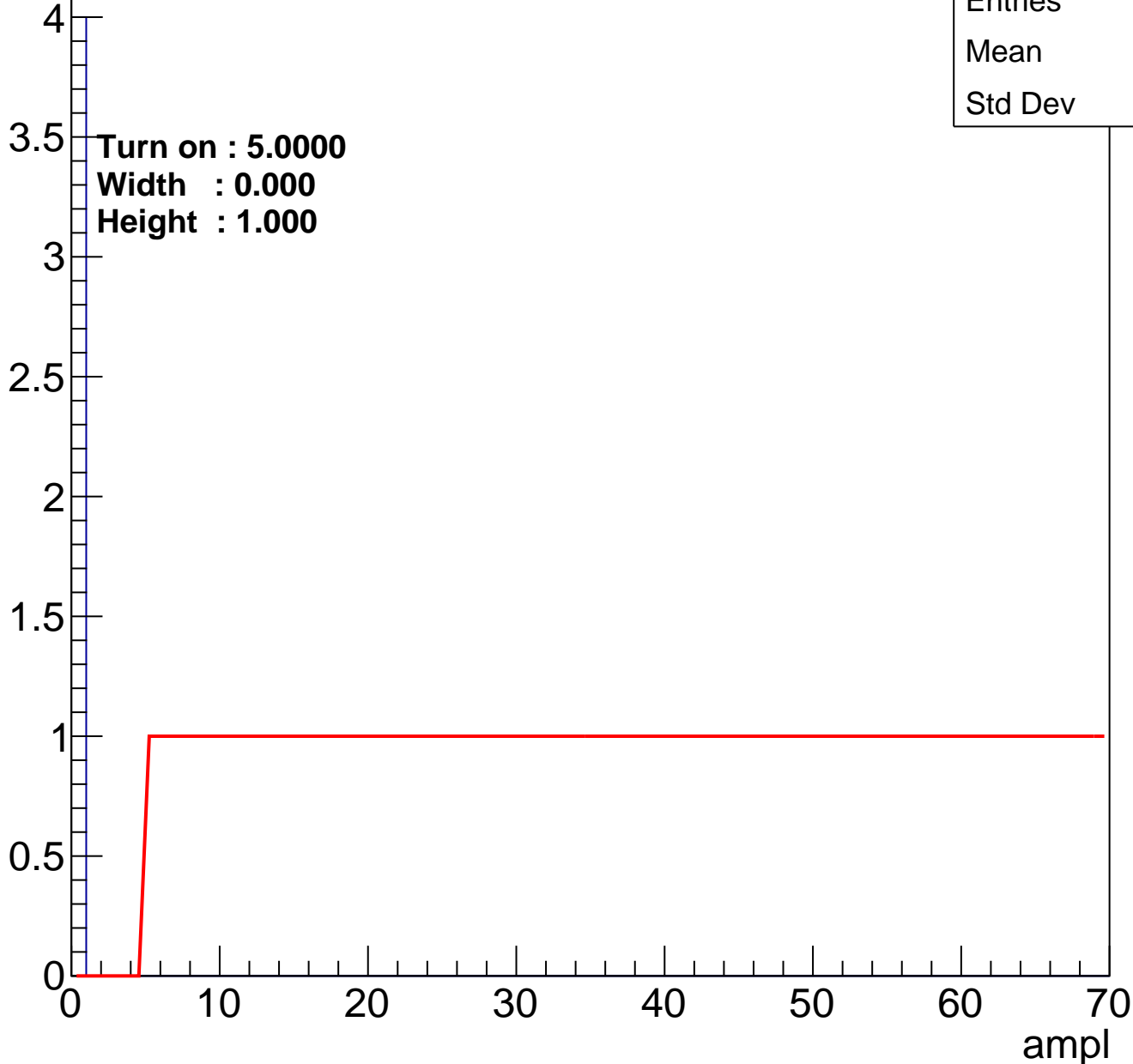
Turn on : 5.0000
Width   : 0.000
Height : 1.000

B0L101S, U7-ch69

calib_packv5_042523_0143.root, FC#1, port C1

Entries	2
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U7-ch70

calib_packv5_042523_0143.root, FC#1, port C1

Entry

Entries	2
Mean	10.5
Std Dev	10.5

Turn on : 5.0000
Width   : 0.000
Height : 1.000

ampl
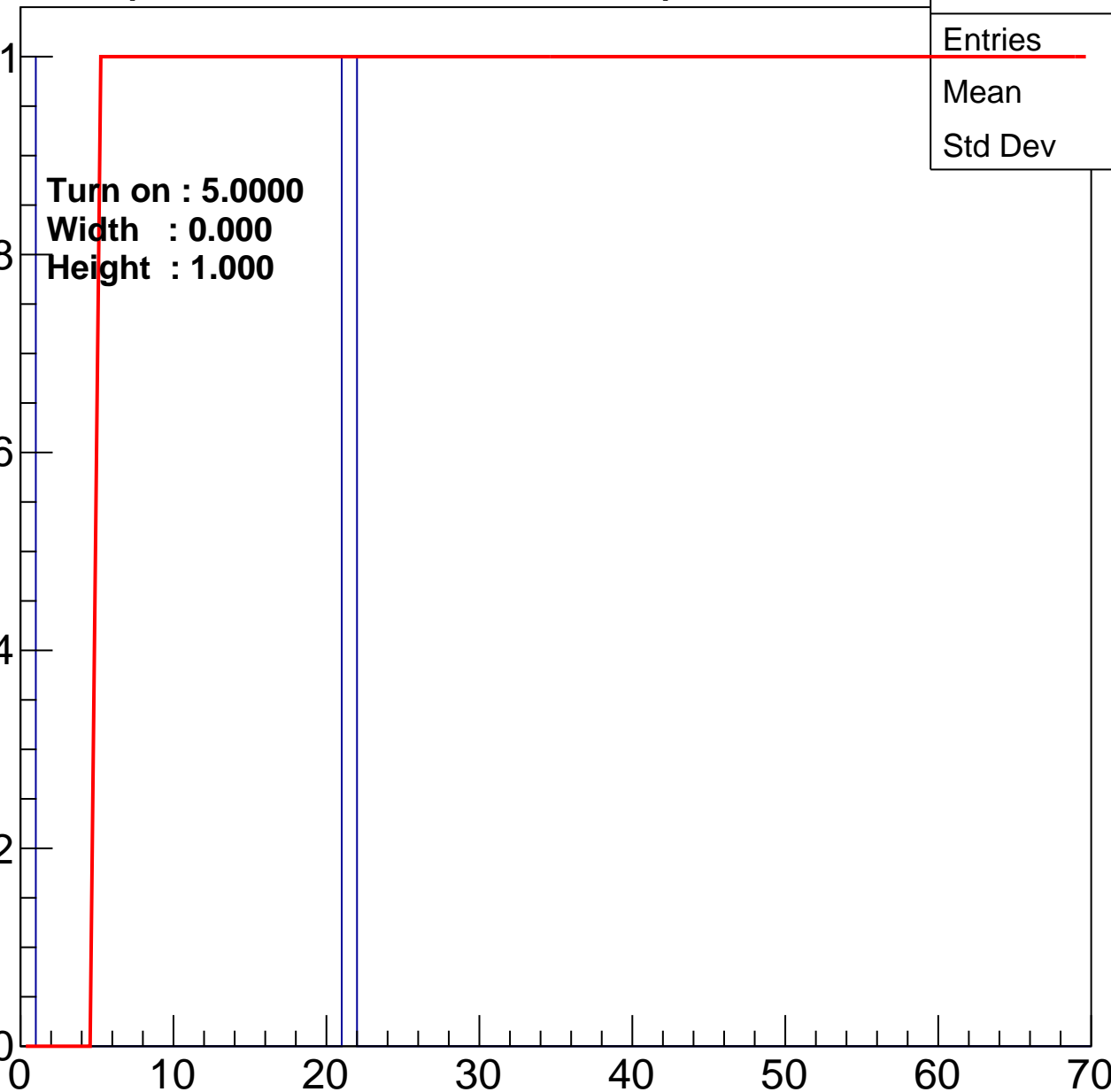
B0L101S, U7-ch71

calib_packv5_042523_0143.root, FC#1, port C1

Entries	2
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U7-ch72

calib_packv5_042523_0143.root, FC#1, port C1

Entry

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entries	2
Mean	0
Std Dev	0

ampl

B0L101S, U7-ch73

calib_packv5_042523_0143.root, FC#1, port C1

Entries	2
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U7-ch74

Entries	3
Mean	0
Std Dev	0

Entry

Turn on : 5.0000
Width   : 0.000
Height : 1.000

ampl

B0L101S, U7-ch75

Entry

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entries	1
Mean	0
Std Dev	0

ampl
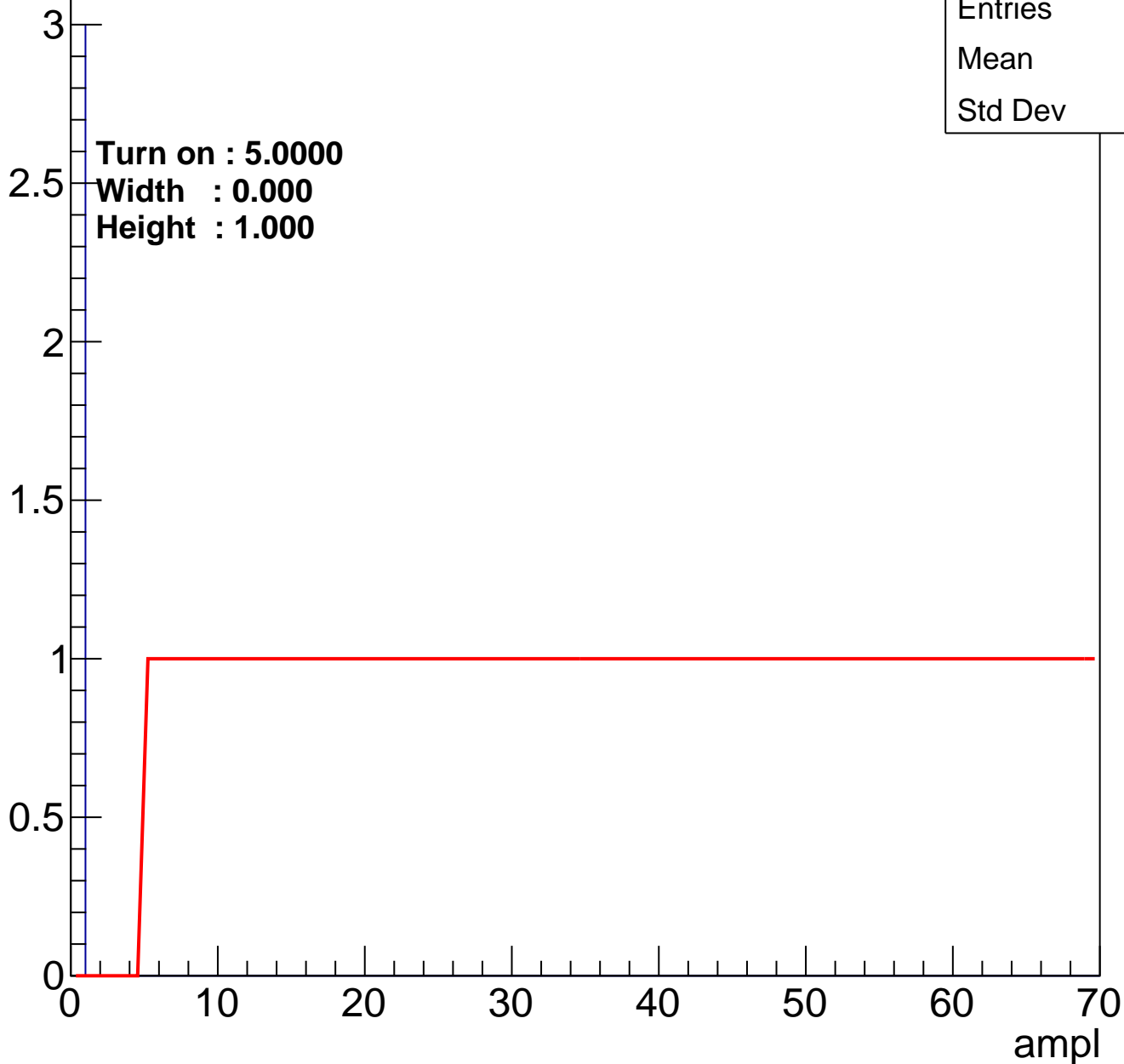
B0L101S, U7-ch76

calib_packv5_042523_0143.root, FC#1, port C1

Entries	0
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U7-ch77

calib_packv5_042523_0143.root, FC#1, port C1

Entry

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entries	4
Mean	7
Std Dev	12.12

ampl
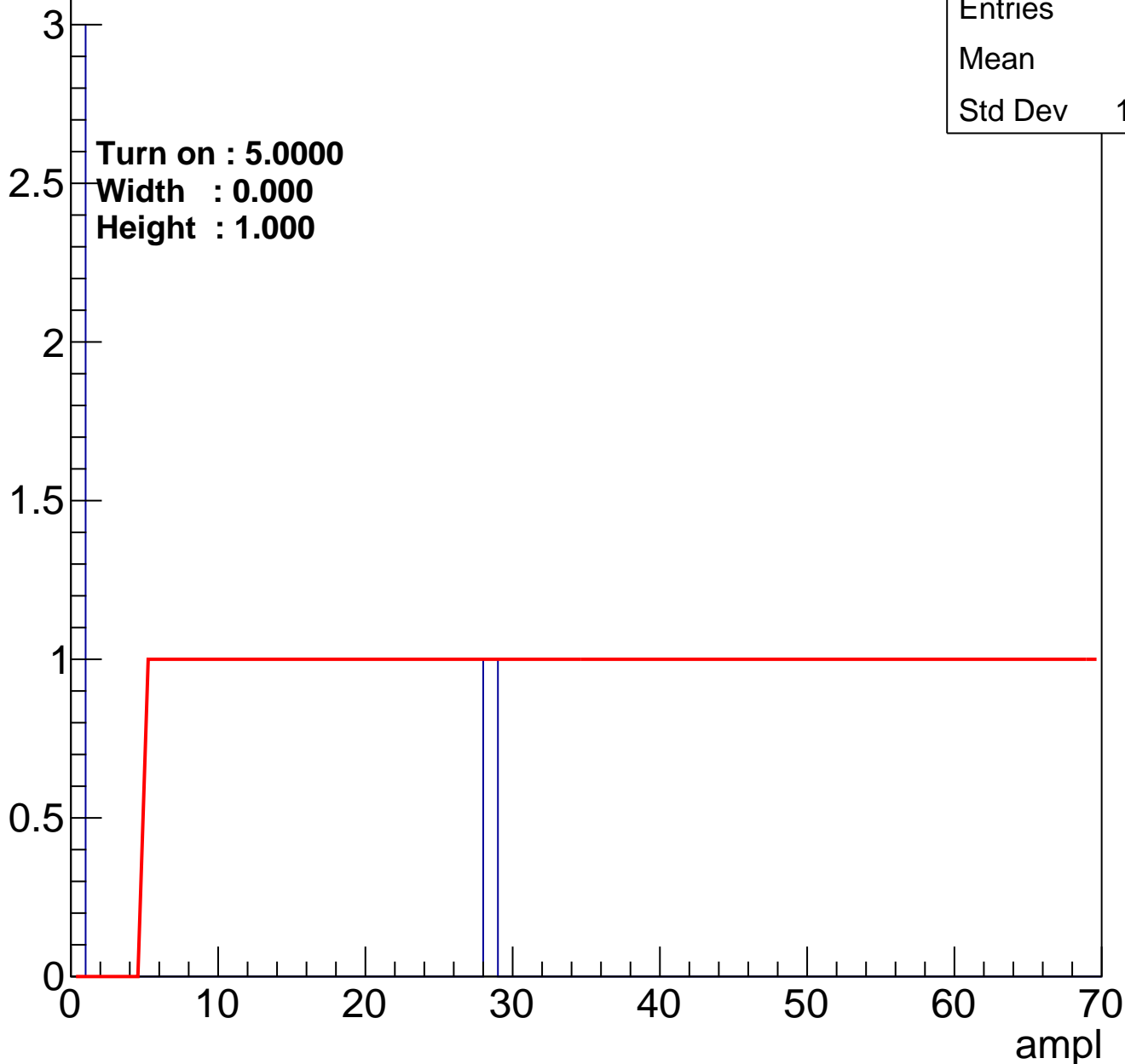
B0L101S, U7-ch78

calib_packv5_042523_0143.root, FC#1, port C1

Entries	2
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl
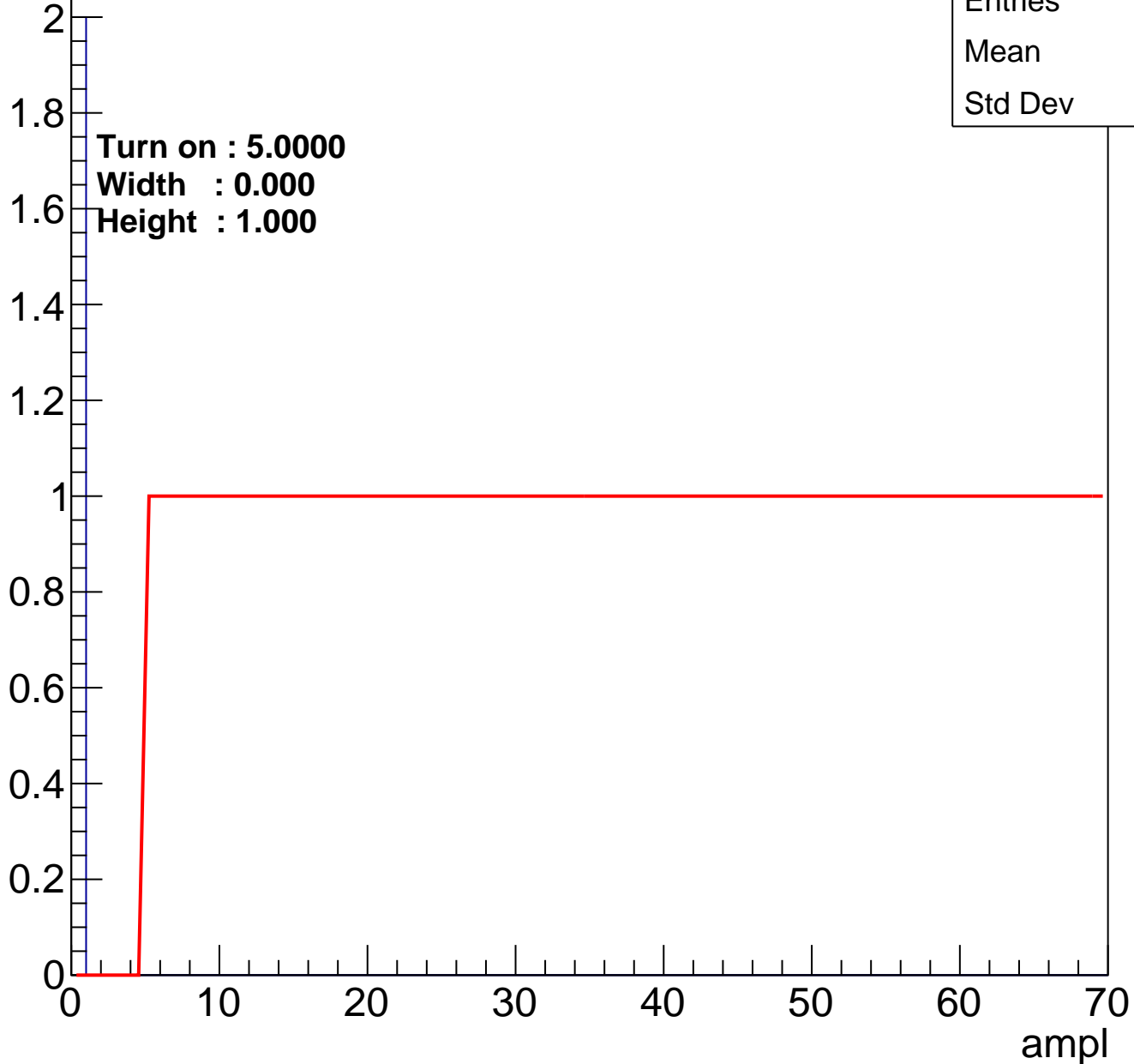
B0L101S, U7-ch79

calib_packv5_042523_0143.root, FC#1, port C1

Entry

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entries	3
Mean	0
Std Dev	0

ampl
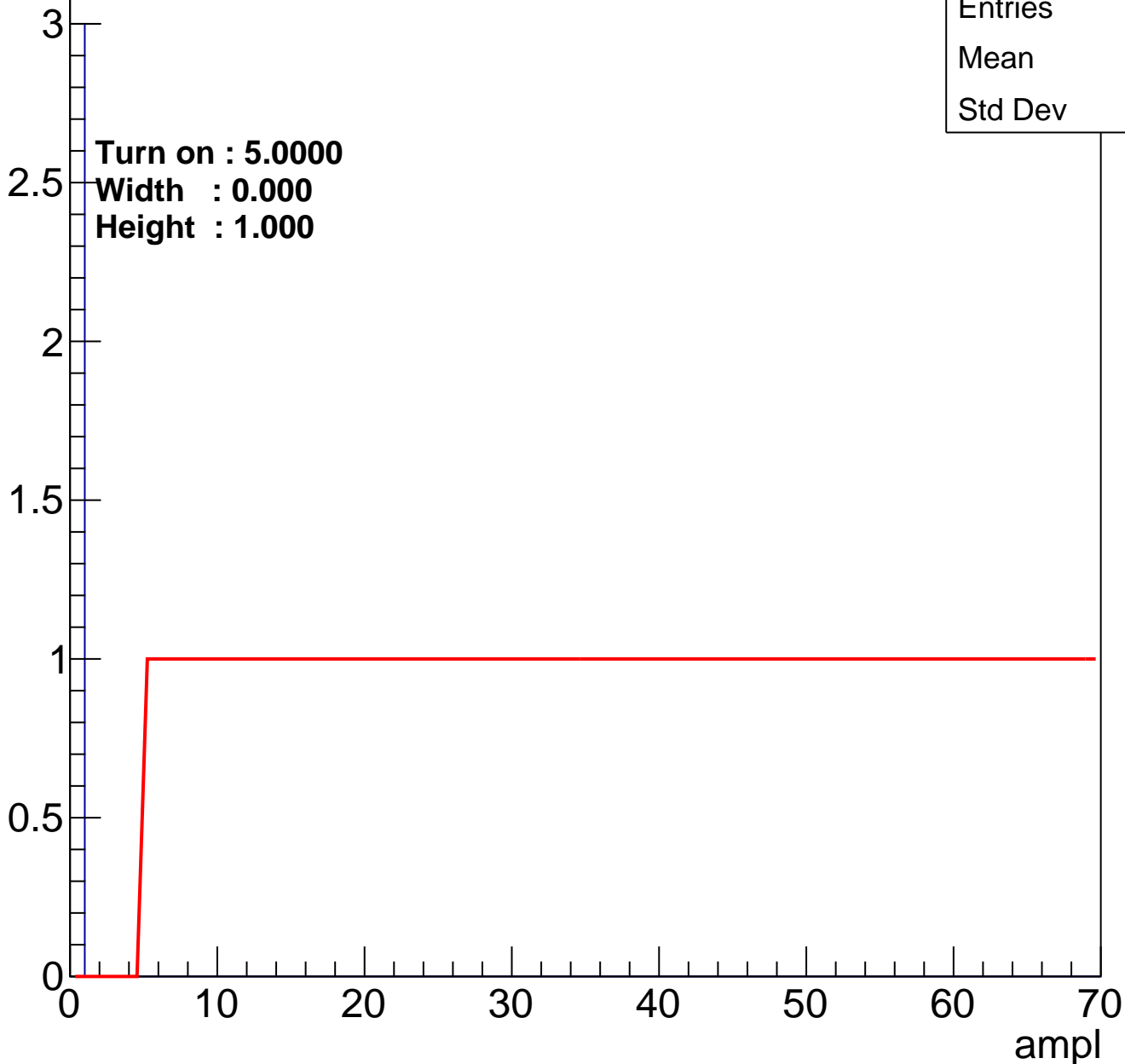
B0L101S, U7-ch80

calib_packv5_042523_0143.root, FC#1, port C1

Entry

Entries	2
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

ampl
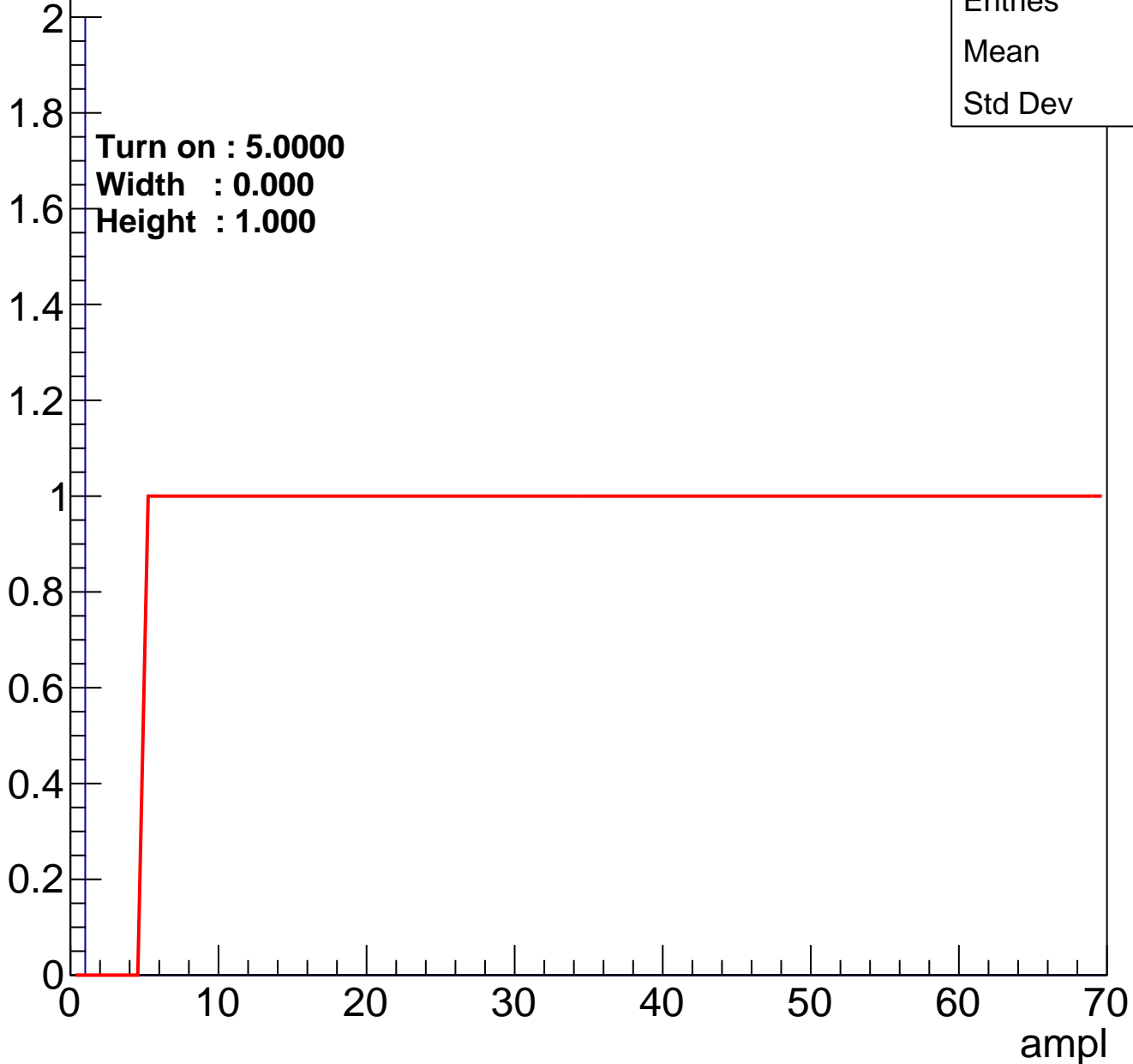
B0L101S, U7-ch81

calib_packv5_042523_0143.root, FC#1, port C1

Entries	0
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U7-ch82

calib_packv5_042523_0143.root, FC#1, port C1

Turn on : 5.0000
Width   : 0.000
Height : 1.000
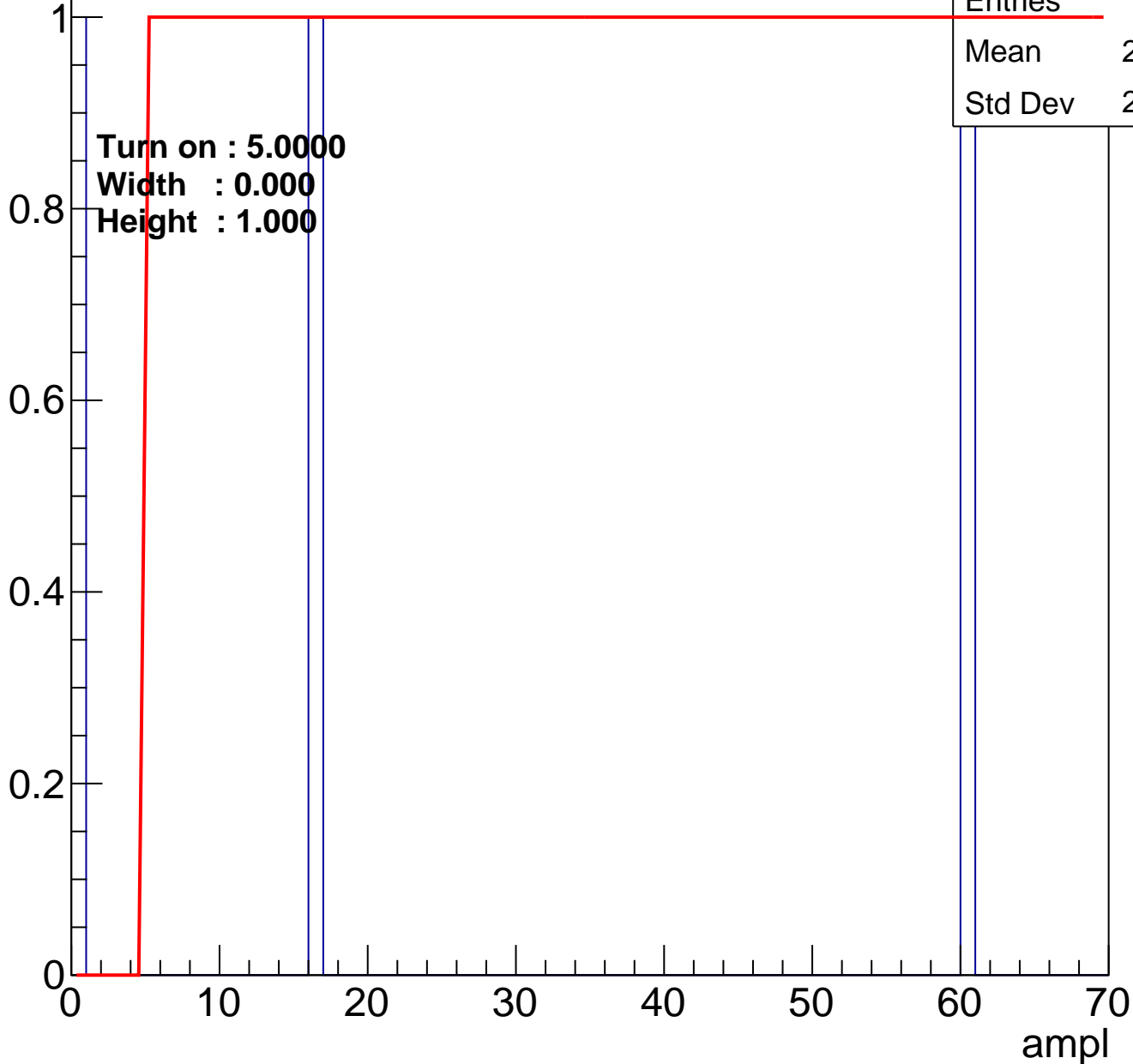
Entries	3
Mean	25.33
Std Dev	25.37

Entry

ampl

B0L101S, U7-ch83

calib_packv5_042523_0143.root, FC#1, port C1

Entries	3
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl
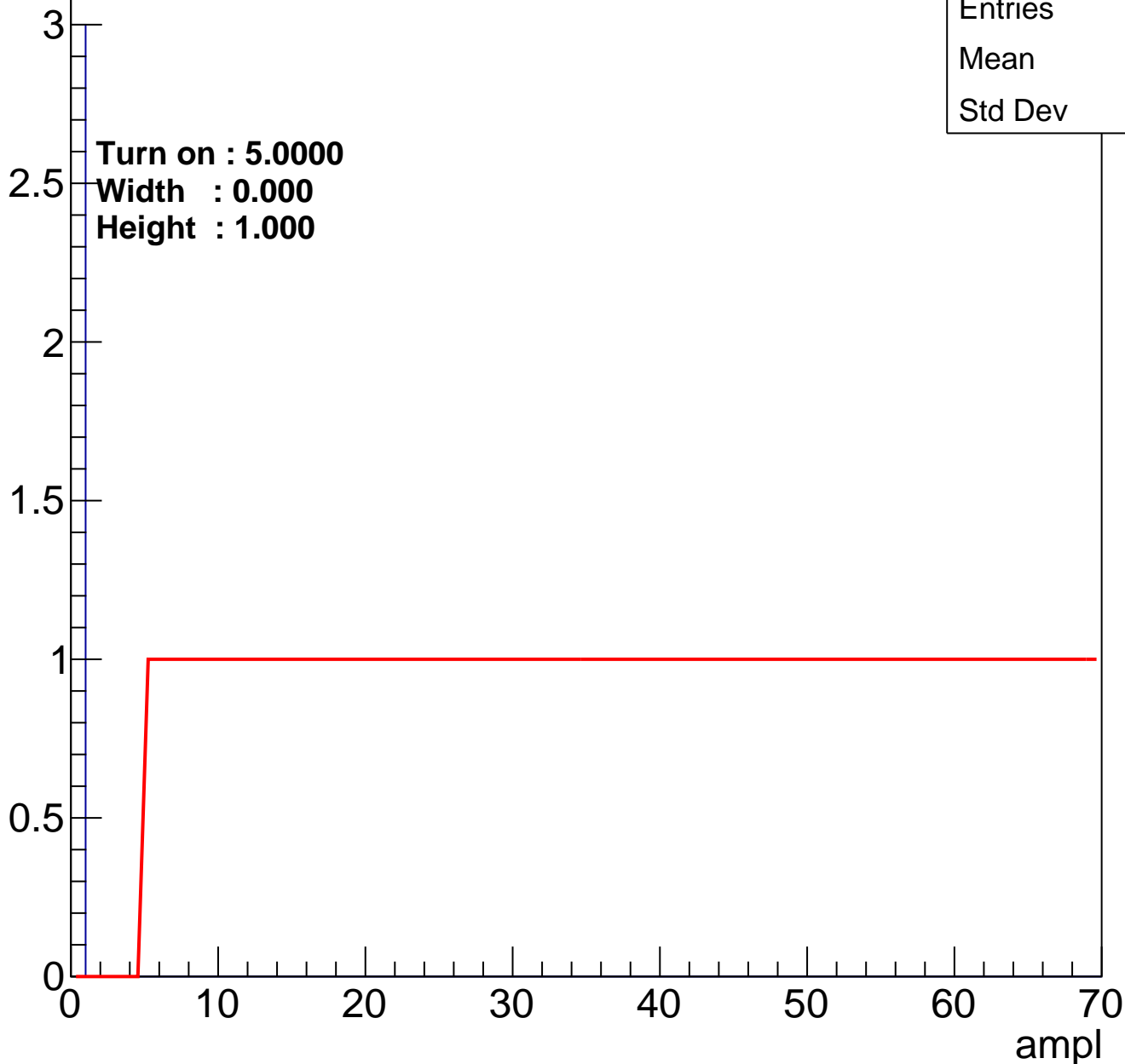
B0L101S, U7-ch84

calib_packv5_042523_0143.root, FC#1, port C1

Entries	2
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U7-ch85

calib_packv5_042523_0143.root, FC#1, port C1

Entries	2
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl
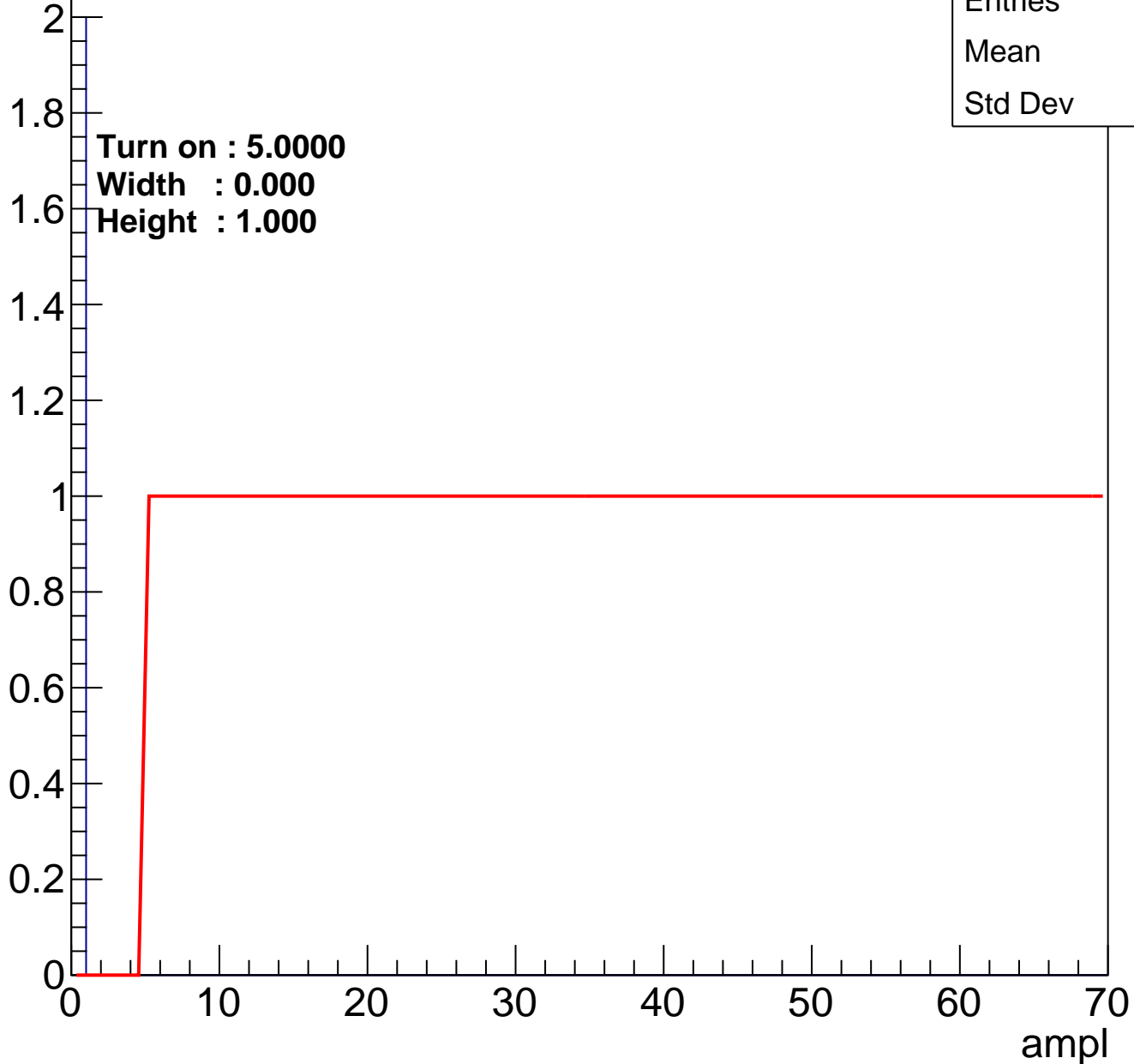
B0L101S, U7-ch86

calib_packv5_042523_0143.root, FC#1, port C1

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entries	2
Mean	0
Std Dev	0
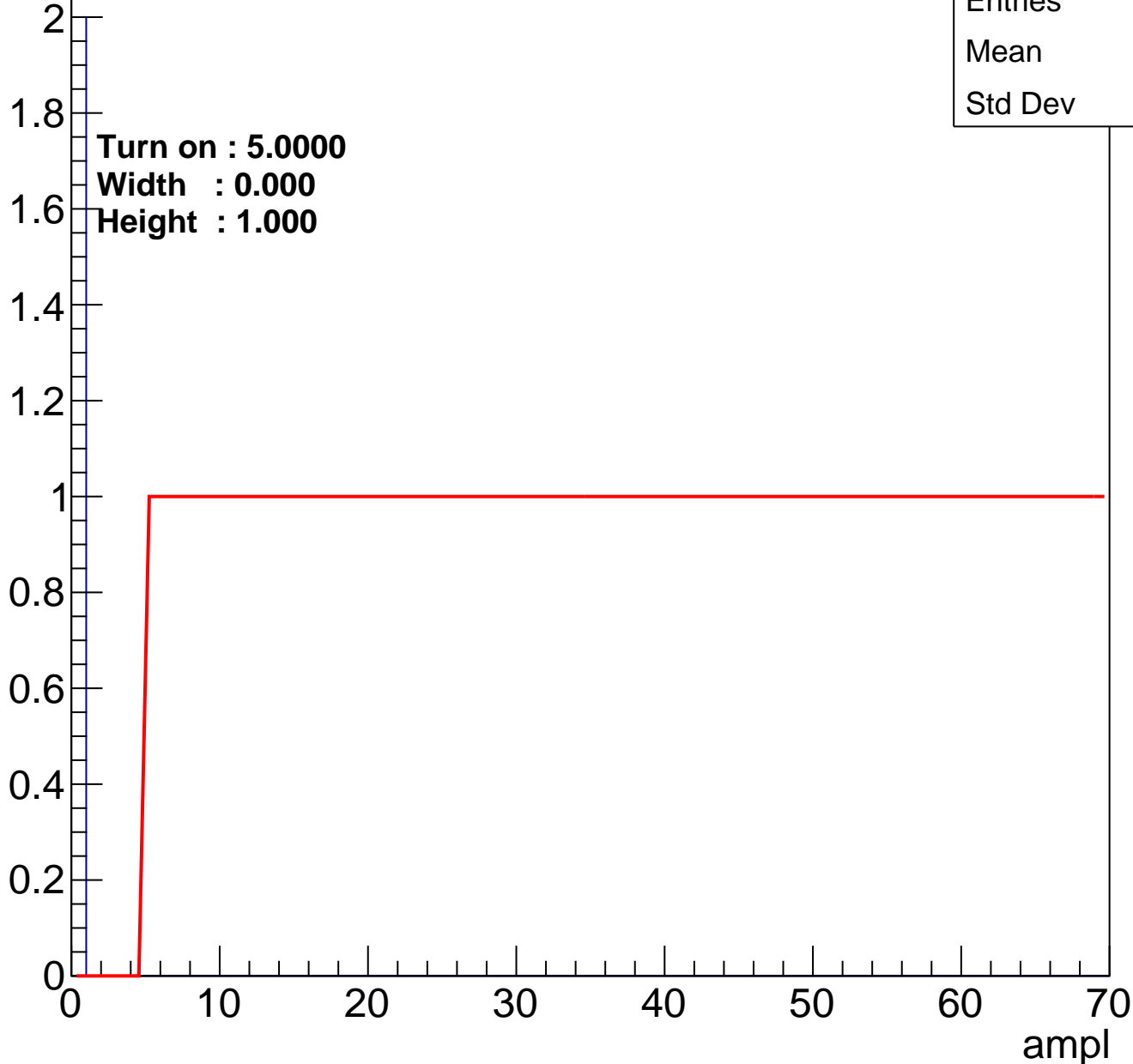
B0L101S, U7-ch87

calib_packv5_042523_0143.root, FC#1, port C1

Entries	2
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl
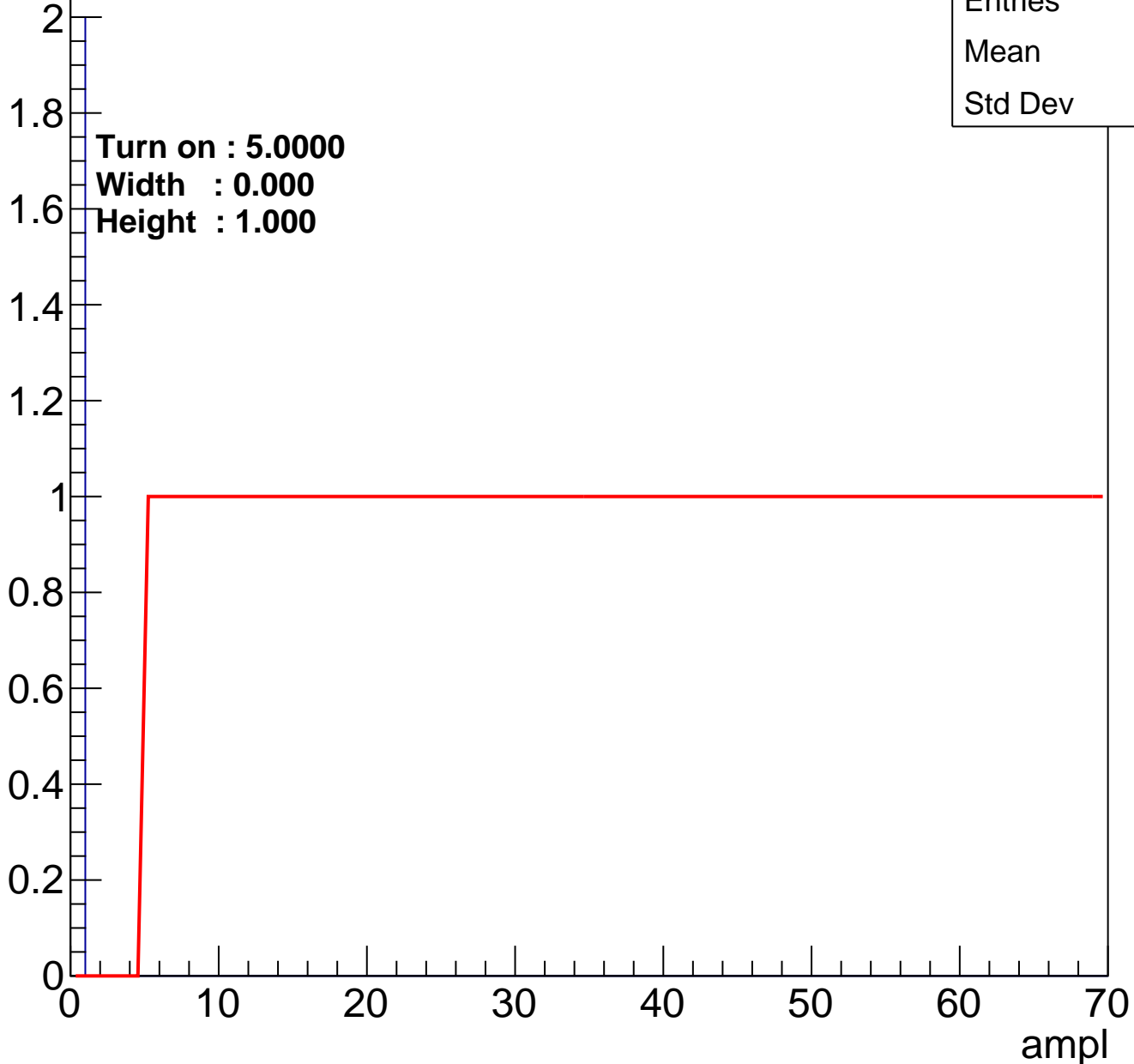
B0L101S, U7-ch88

calib_packv5_042523_0143.root, FC#1, port C1
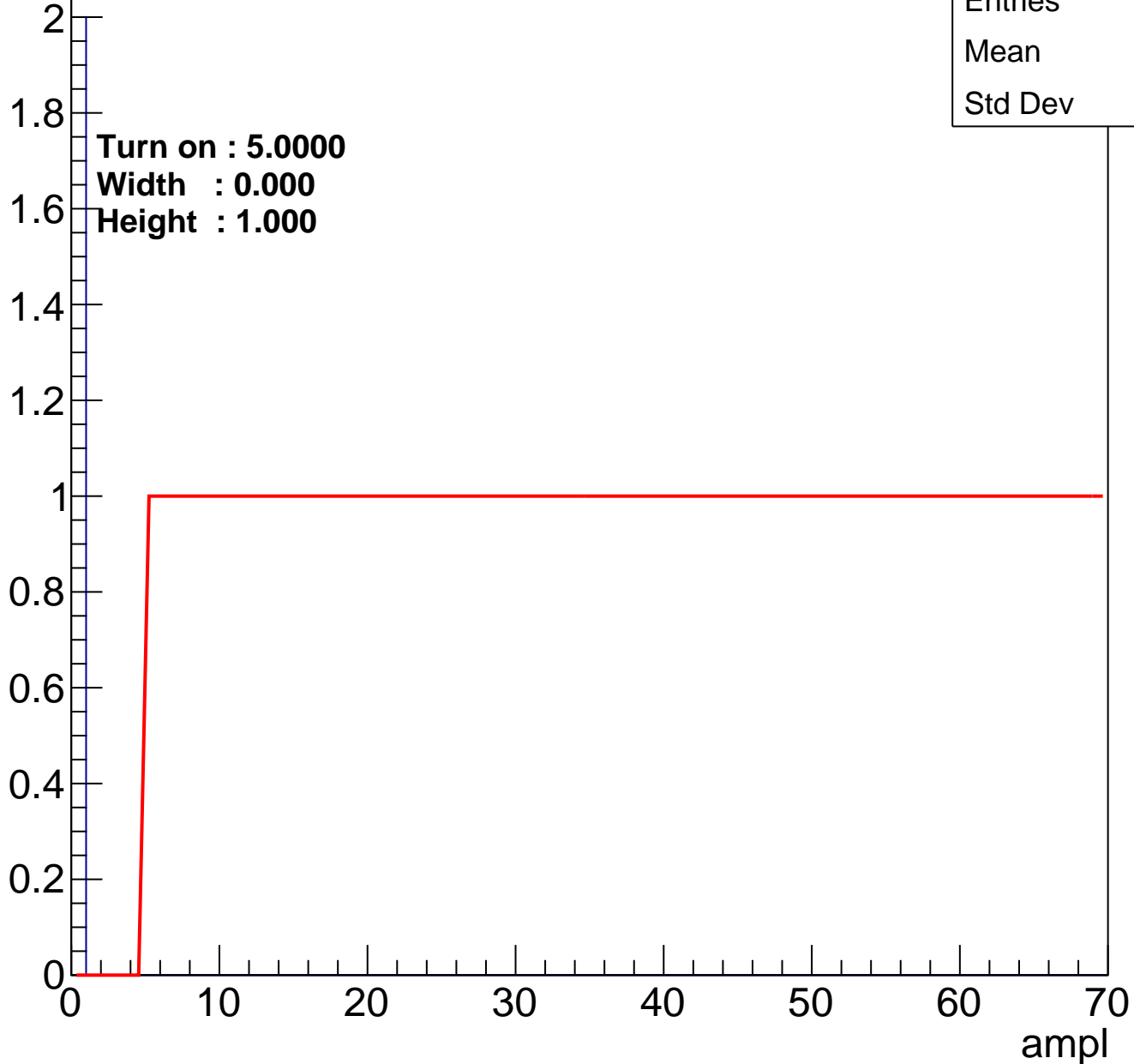
Entries	2
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U7-ch90

calib_packv5_042523_0143.root, FC#1, port C1

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entries	2
Mean	0
Std Dev	0

Entry

ampl

B0L101S, U7-ch91

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entries	1
Mean	0
Std Dev	0

Entry

ampl

B0L101S, U7-ch92

Entry

Entries	4
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

ampl

B0L101S, U7-ch93

calib_packv5_042523_0143.root, FC#1, port C1

Entry

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entries	2
Mean	0
Std Dev	0

ampl

B0L101S, U7-ch94

calib_packv5_042523_0143.root, FC#1, port C1

Entries	3
Mean	19
Std Dev	26.87

Turn on : 5.0000
Width   : 0.000
Height : 1.000
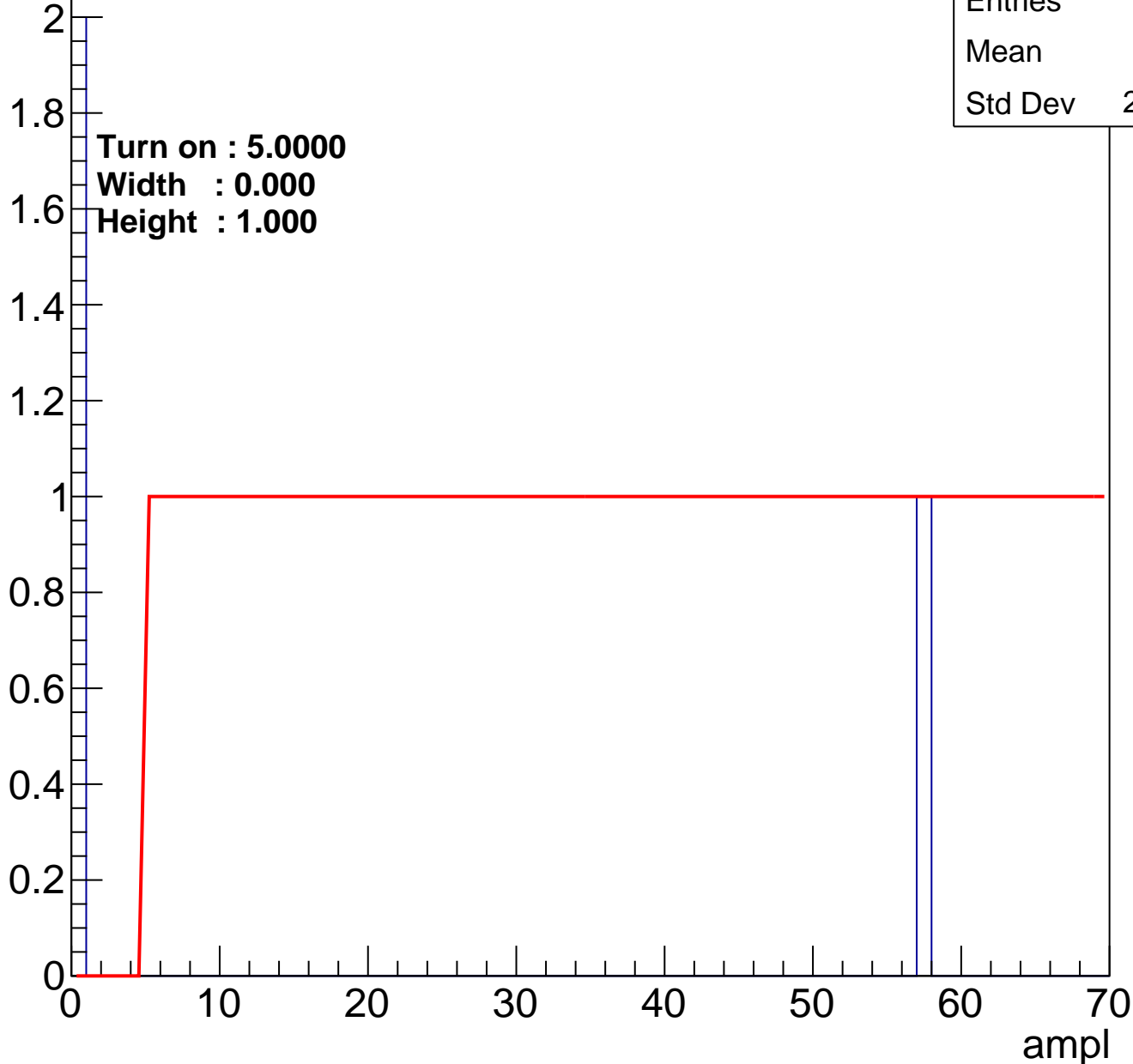
B0L101S, U7-ch95

calib_packv5_042523_0143.root, FC#1, port C1

Entry

Entries	1
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

ampl

B0L101S, U7-ch96

calib_packv5_042523_0143.root, FC#1, port C1

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entries	2
Mean	9.5
Std Dev	9.5

Entry

ampl
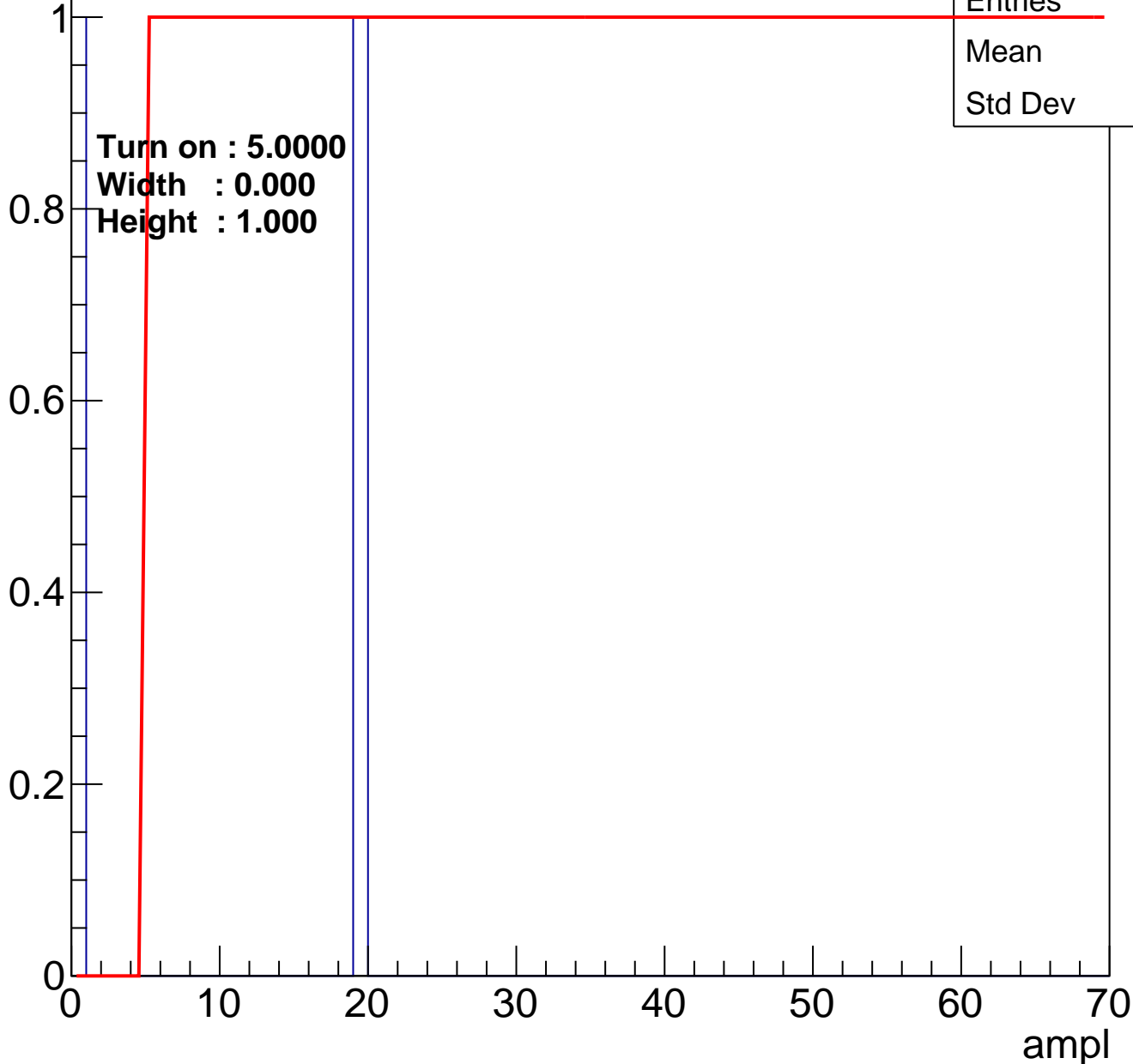
B0L101S, U7-ch97

calib_packv5_042523_0143.root, FC#1, port C1

Entries	1
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U7-ch98

calib_packv5_042523_0143.root, FC#1, port C1

Entries	1
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl
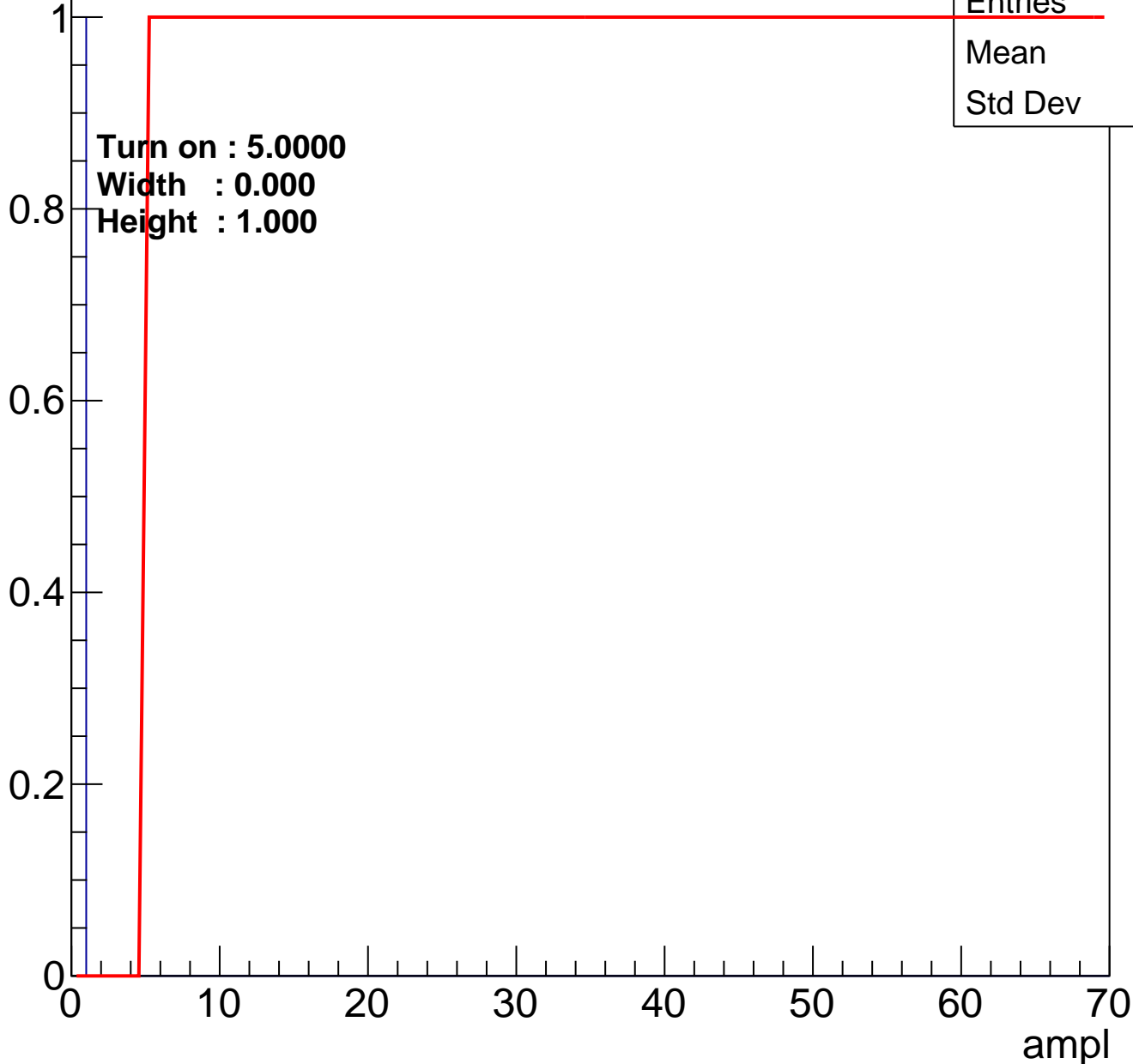
B0L101S, U7-ch99

calib_packv5_042523_0143.root, FC#1, port C1

Entries	1
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl
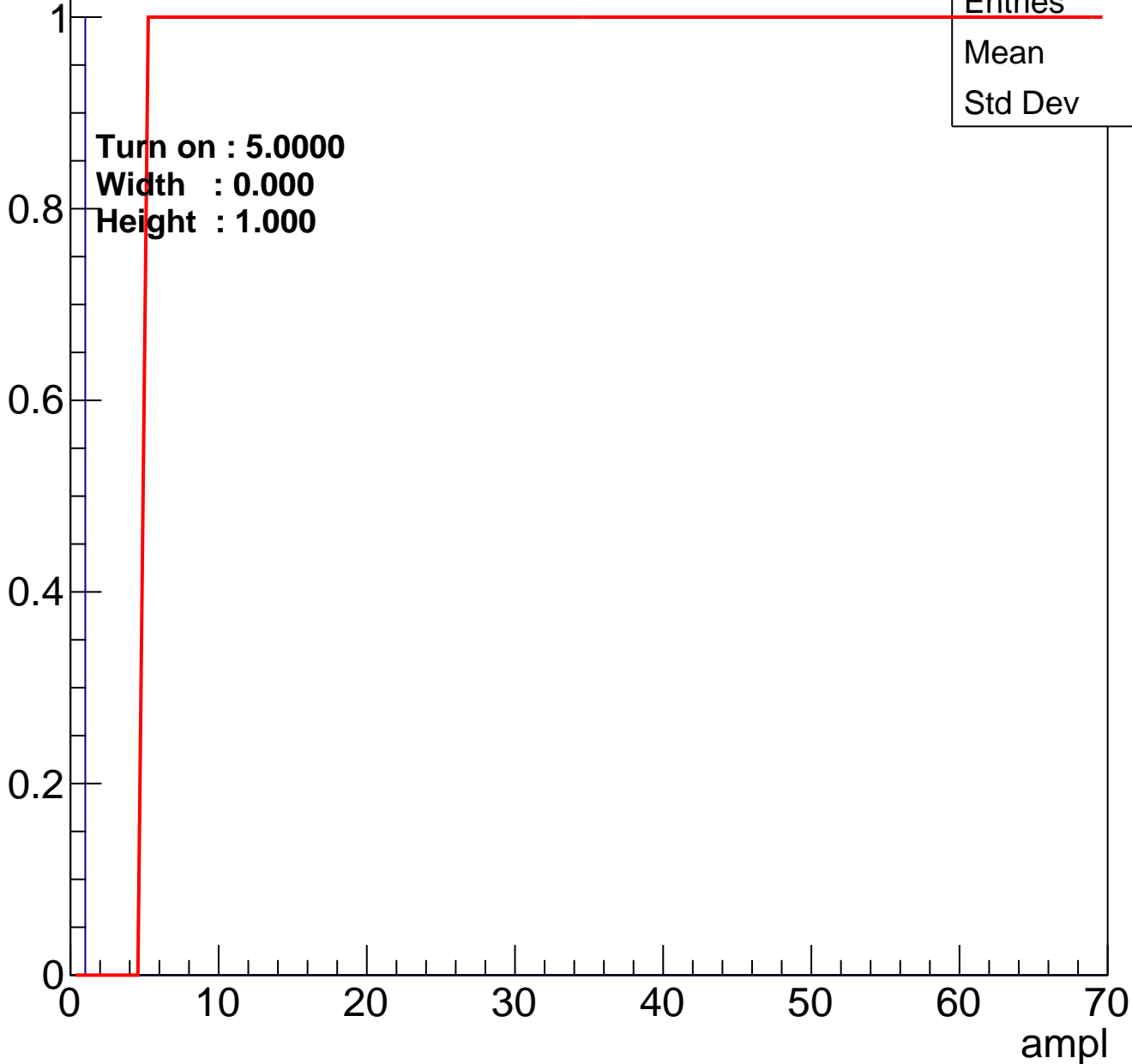
B0L101S, U7-ch100

calib_packv5_042523_0143.root, FC#1, port C1

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entries	1
Mean	0
Std Dev	0

B0L101S, U7-ch101

Entries	0
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U7-ch102

calib_packv5_042523_0143.root, FC#1, port C1
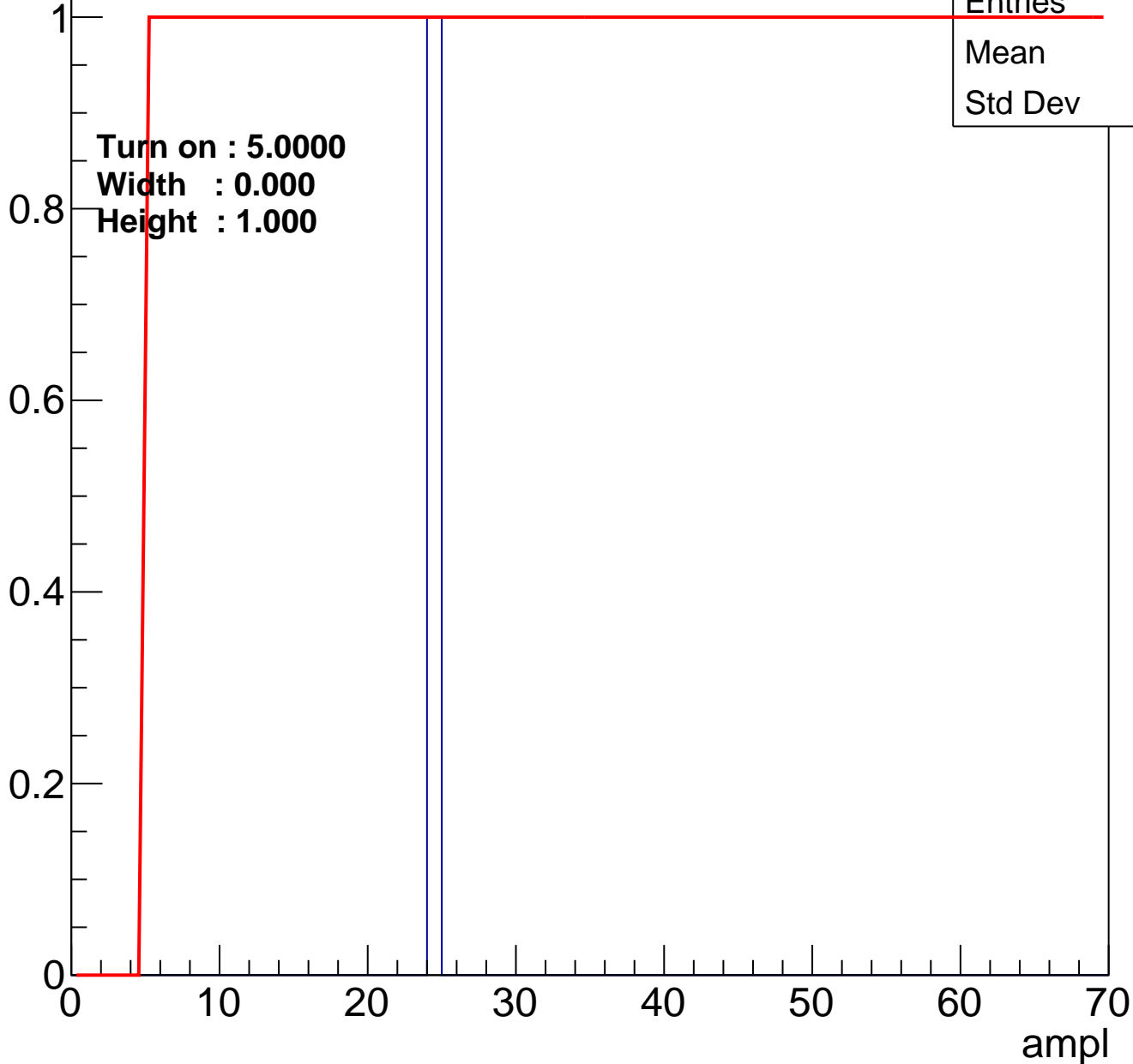
Entries	1
Mean	24
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U7-ch103

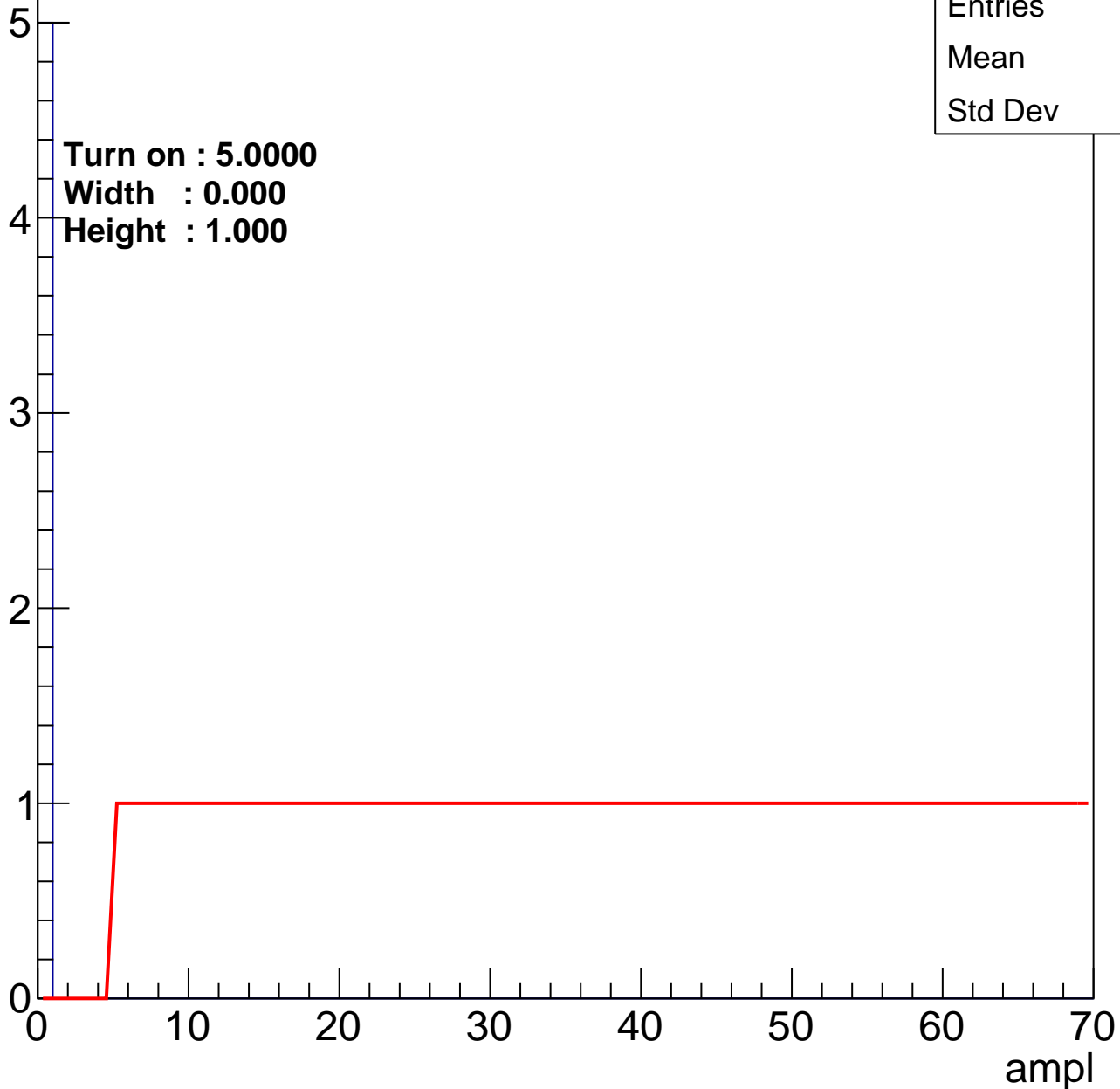**calib_packv5_042523_0143.root, FC#1, port C1**

Entries	5
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

B0L101S, U7-ch104

calib_packv5_042523_0143.root, FC#1, port C1

Entries	2
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

B0L101S, U7-ch105

calib_packv5_042523_0143.root, FC#1, port C1

Entries	3
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U7-ch106

calib_packv5_042523_0143.root, FC#1, port C1

Entries		2
Mean		0
Std Dev		0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U7-ch107

calib_packv5_042523_0143.root, FC#1, port C1

Entries	2
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl
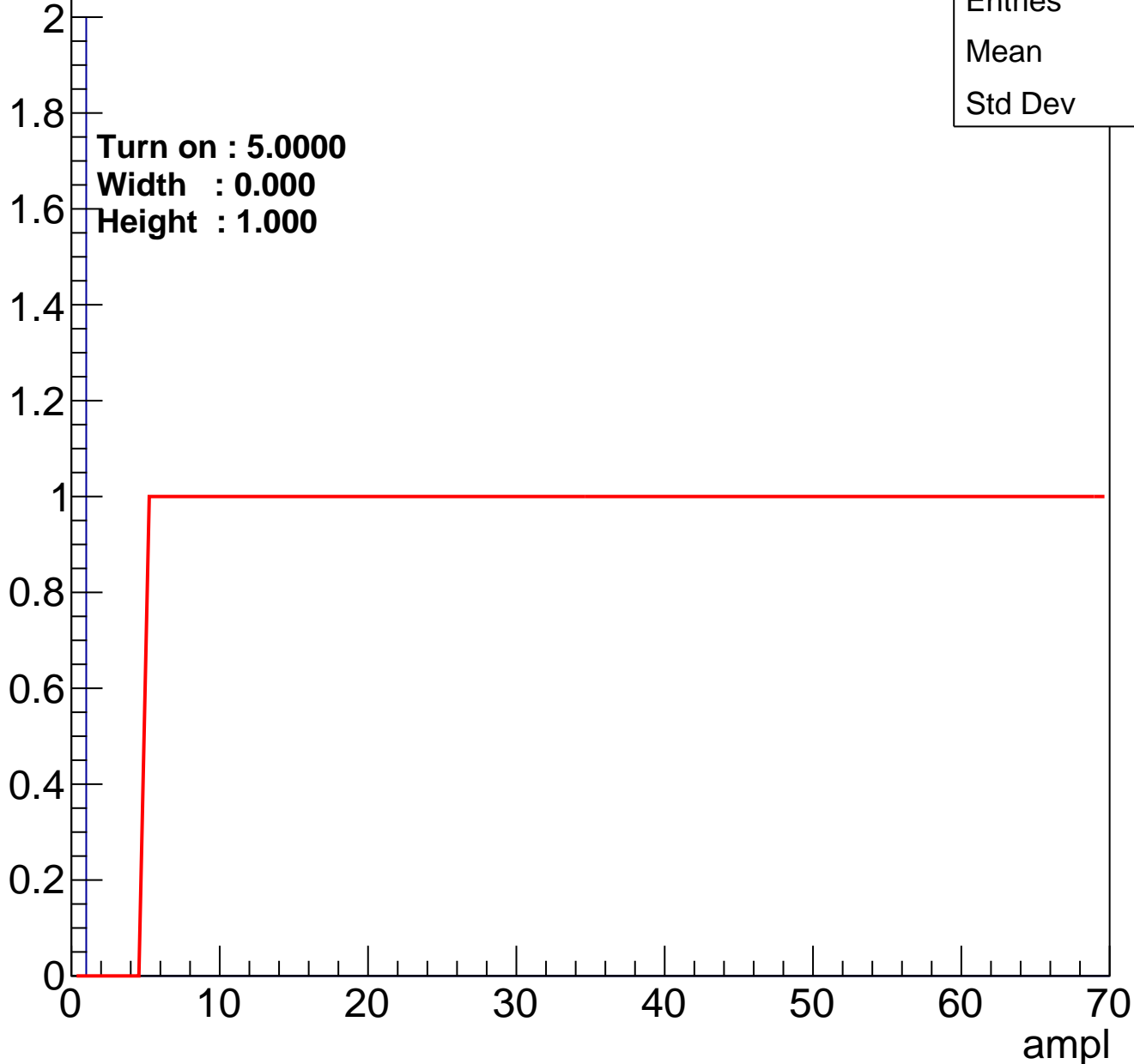
B0L101S, U7-ch108

calib_packv5_042523_0143.root, FC#1, port C1

Entries	3
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl
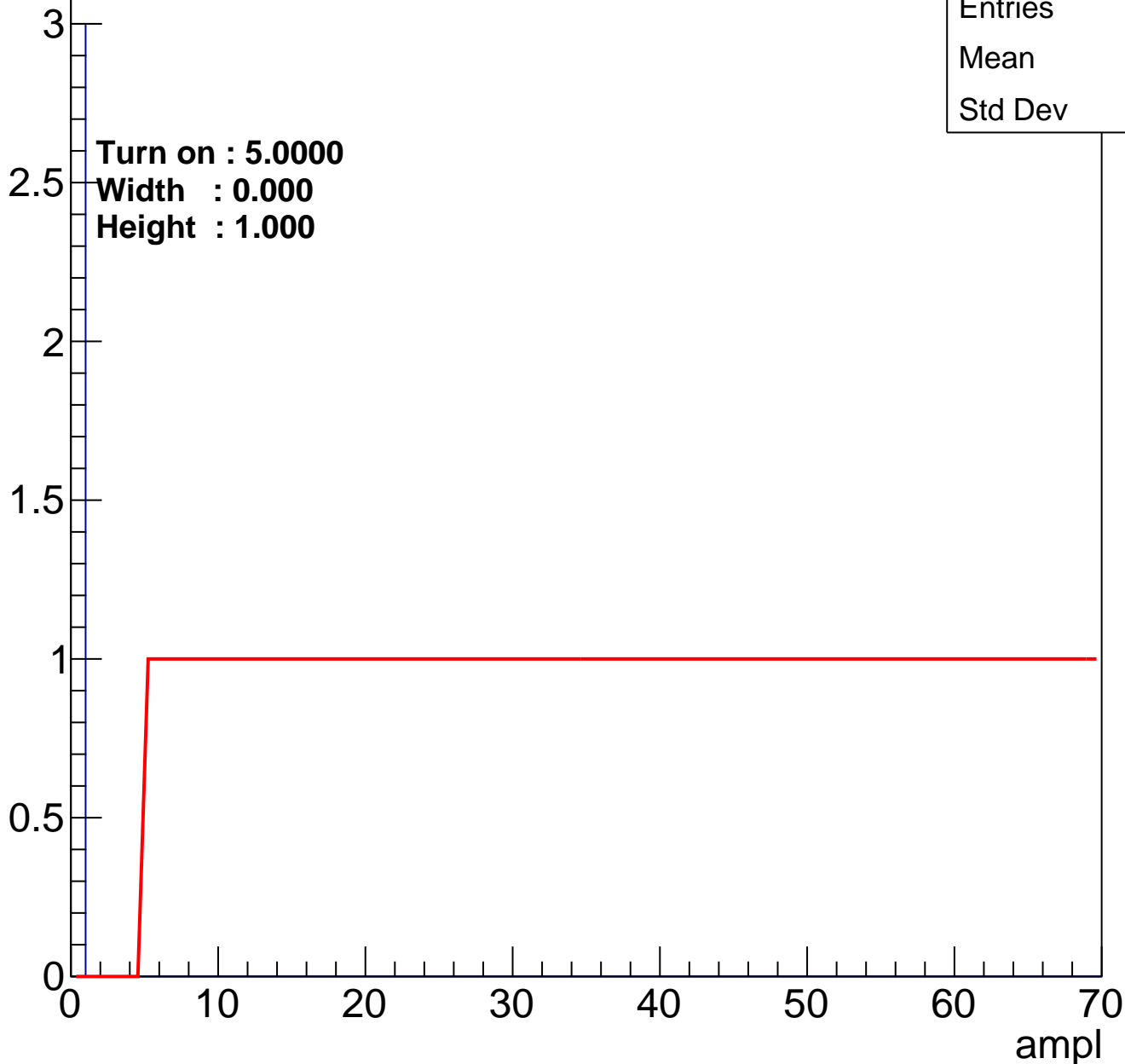
B0L101S, U7-ch109

calib_packv5_042523_0143.root, FC#1, port C1

Entries	3
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl
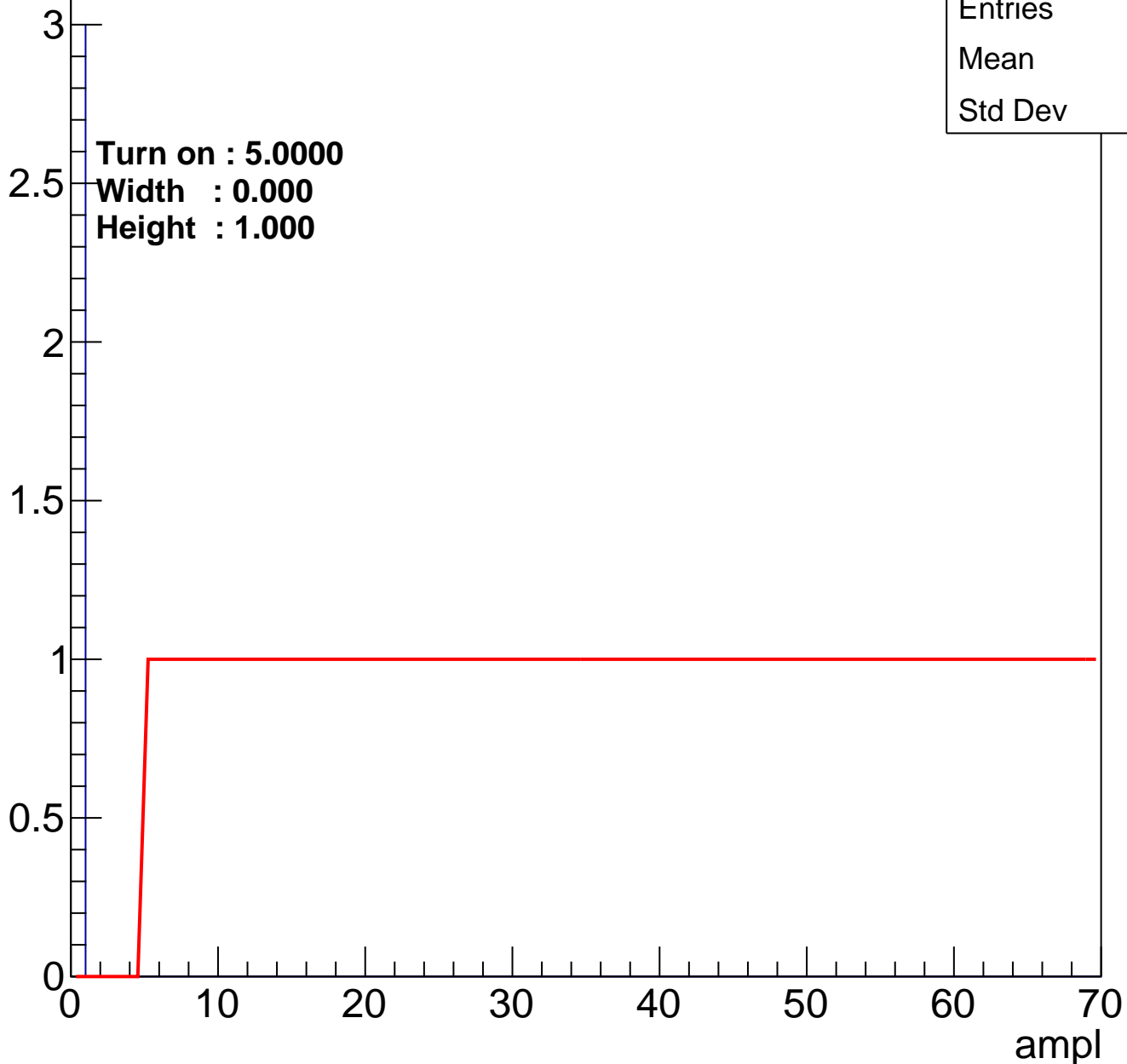
B0L101S, U7-ch110

calib_packv5_042523_0143.root, FC#1, port C1

Entries	3
Mean	20.33
Std Dev	28.76

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl
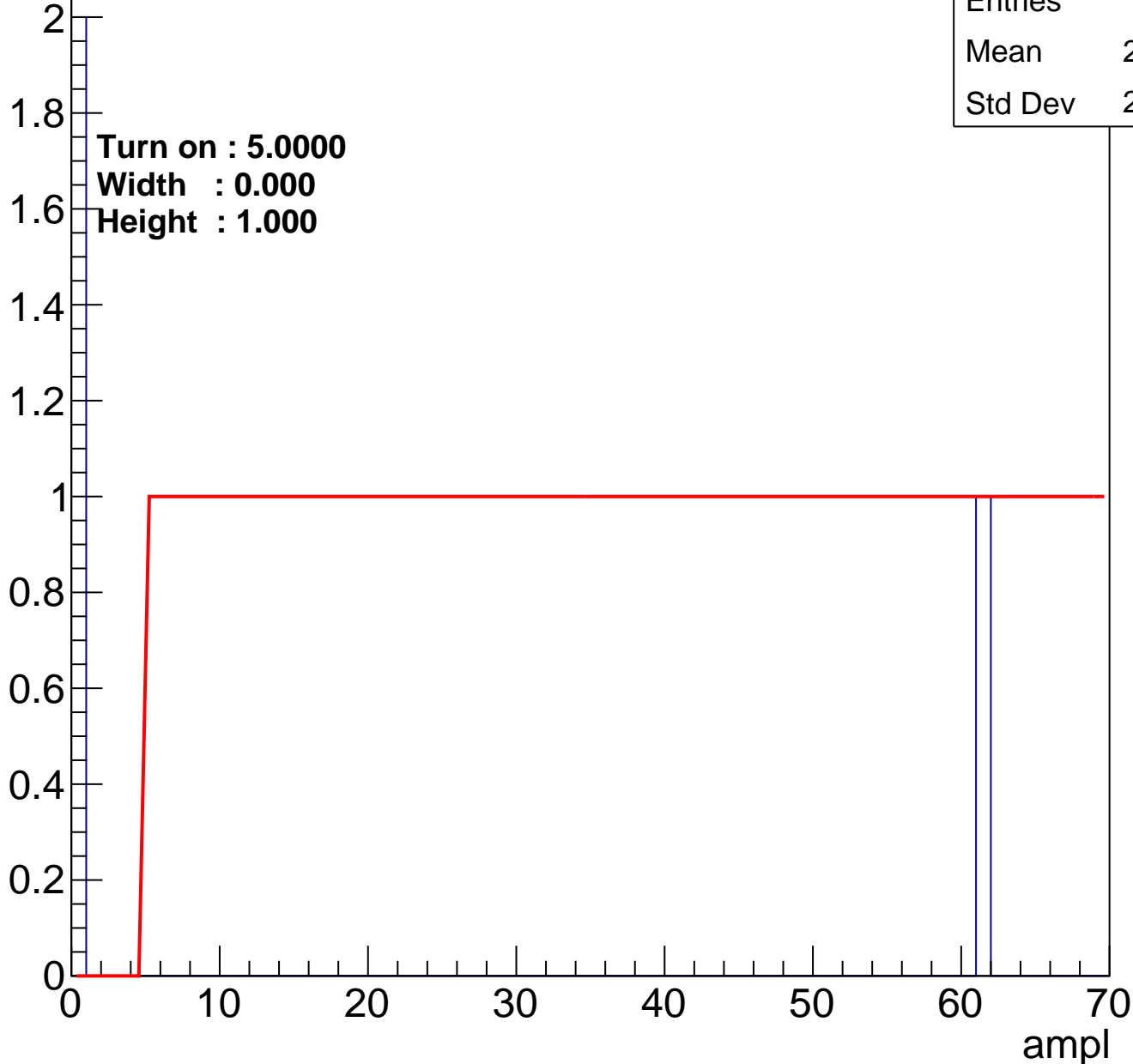
B0L101S, U7-ch111

calib_packv5_042523_0143.root, FC#1, port C1

Entries	1
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U7-ch112

calib_packv5_042523_0143.root, FC#1, port C1

Turn on : 5.0000
Width   : 0.000
Height : 1.000
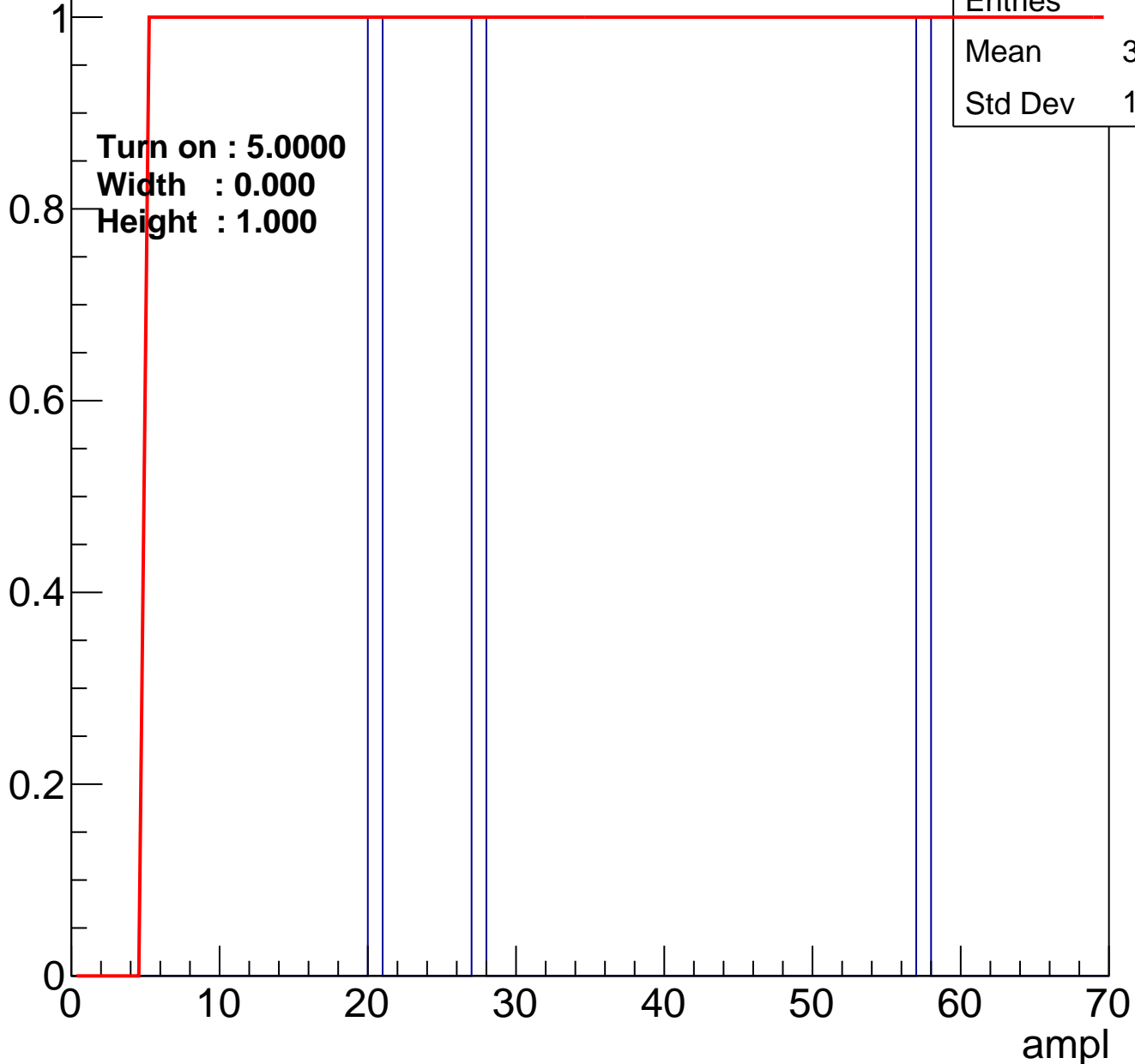
Entries	3
Mean	34.67
Std Dev	16.05

ampl

B0L101S, U7-ch113

calib_packv5_042523_0143.root, FC#1, port C1

Entries	2
Mean	0
Std Dev	0

Turn on : 5.0000
Width : 0.000
Height : 1.000

Entry

ampl

B0L101S, U7-ch114

calib_packv5_042523_0143.root, FC#1, port C1

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entries	5
Mean	12.2
Std Dev	18.98

ampl
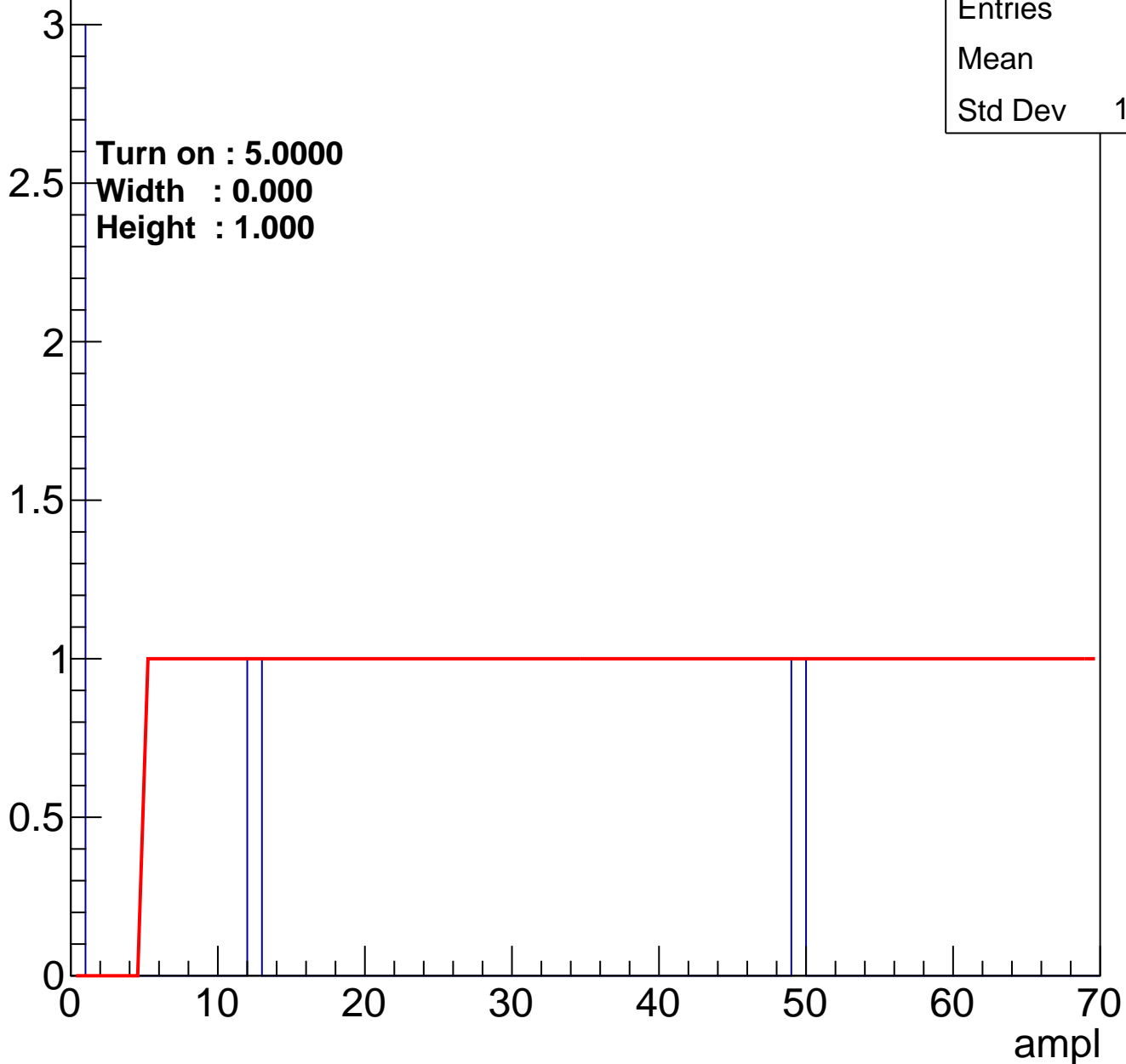
B0L101S, U7-ch115

calib_packv5_042523_0143.root, FC#1, port C1

Entries	0
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U7-ch116

calib_packv5_042523_0143.root, FC#1, port C1
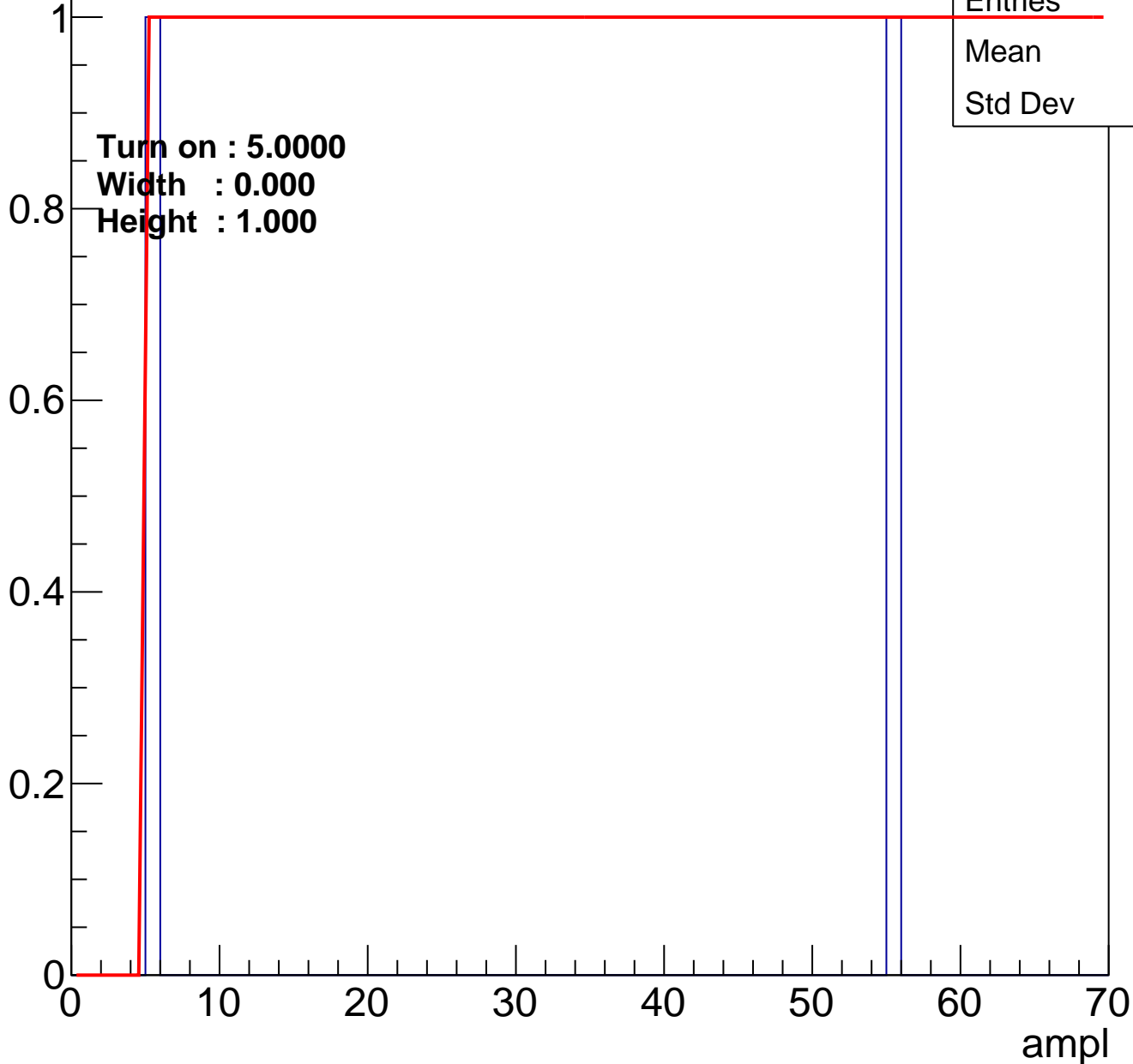
Entries	2
Mean	30
Std Dev	25

Turn on : 5.0000
Width   : 0.000
Height : 1.000

B0L101S, U7-ch117

calib_packv5_042523_0143.root, FC#1, port C1

Entries	2
Mean	0
Std Dev	0

Turn on : 5.0000
Width : 0.000
Height : 1.000

Entry

ampl

B0L101S, U7-ch118

calib_packv5_042523_0143.root, FC#1, port C1

Entries	6
Mean	17.67
Std Dev	19.75

Turn on : 5.0000
Width   : 0.000
Height : 1.000
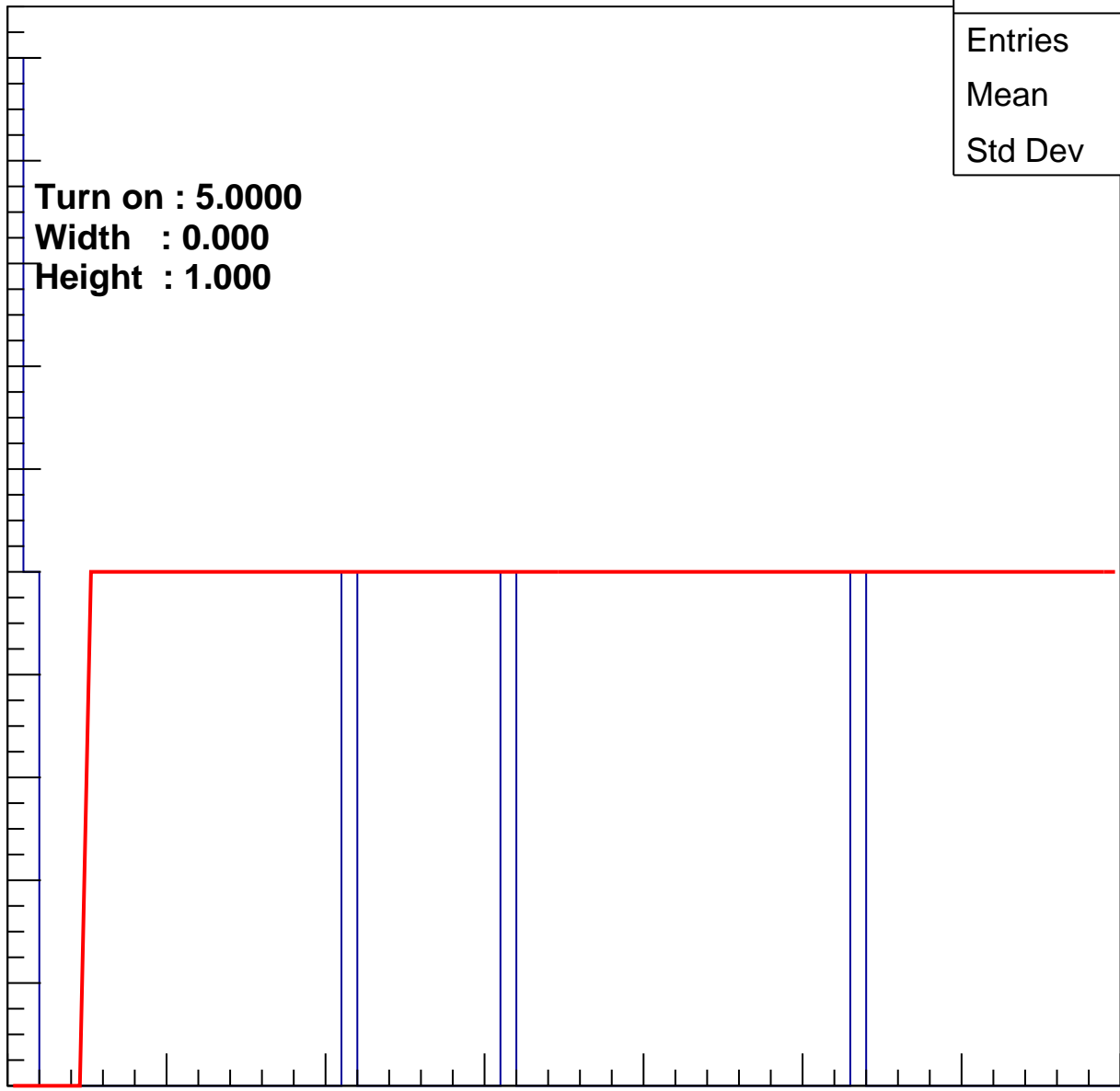
B0L101S, U7-ch119

calib_packv5_042523_0143.root, FC#1, port C1

Entries	2
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U7-ch120

calib_packv5_042523_0143.root, FC#1, port C1
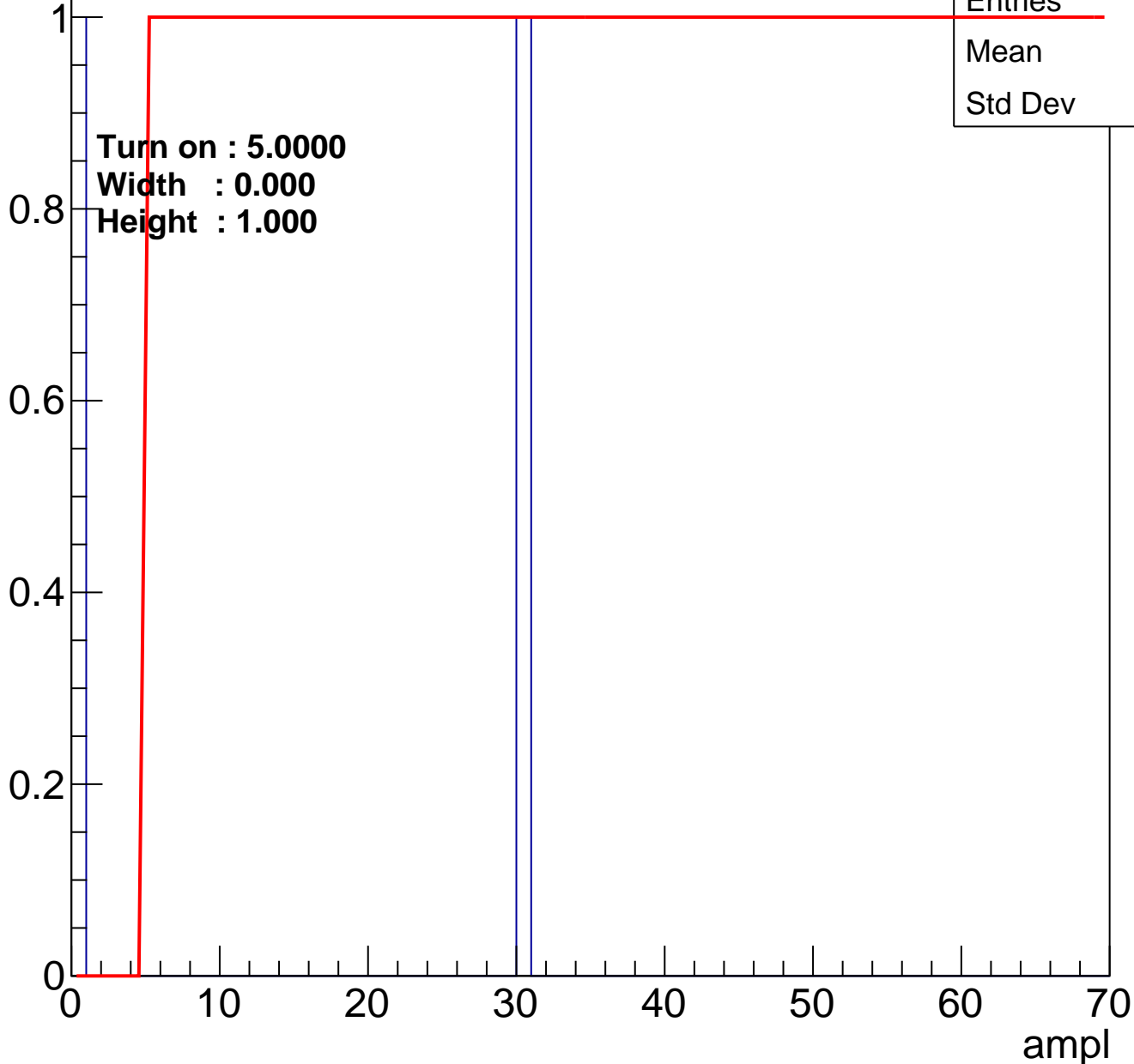
Entries	2
Mean	15
Std Dev	15

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U7-ch121

Entries	4
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

ampl
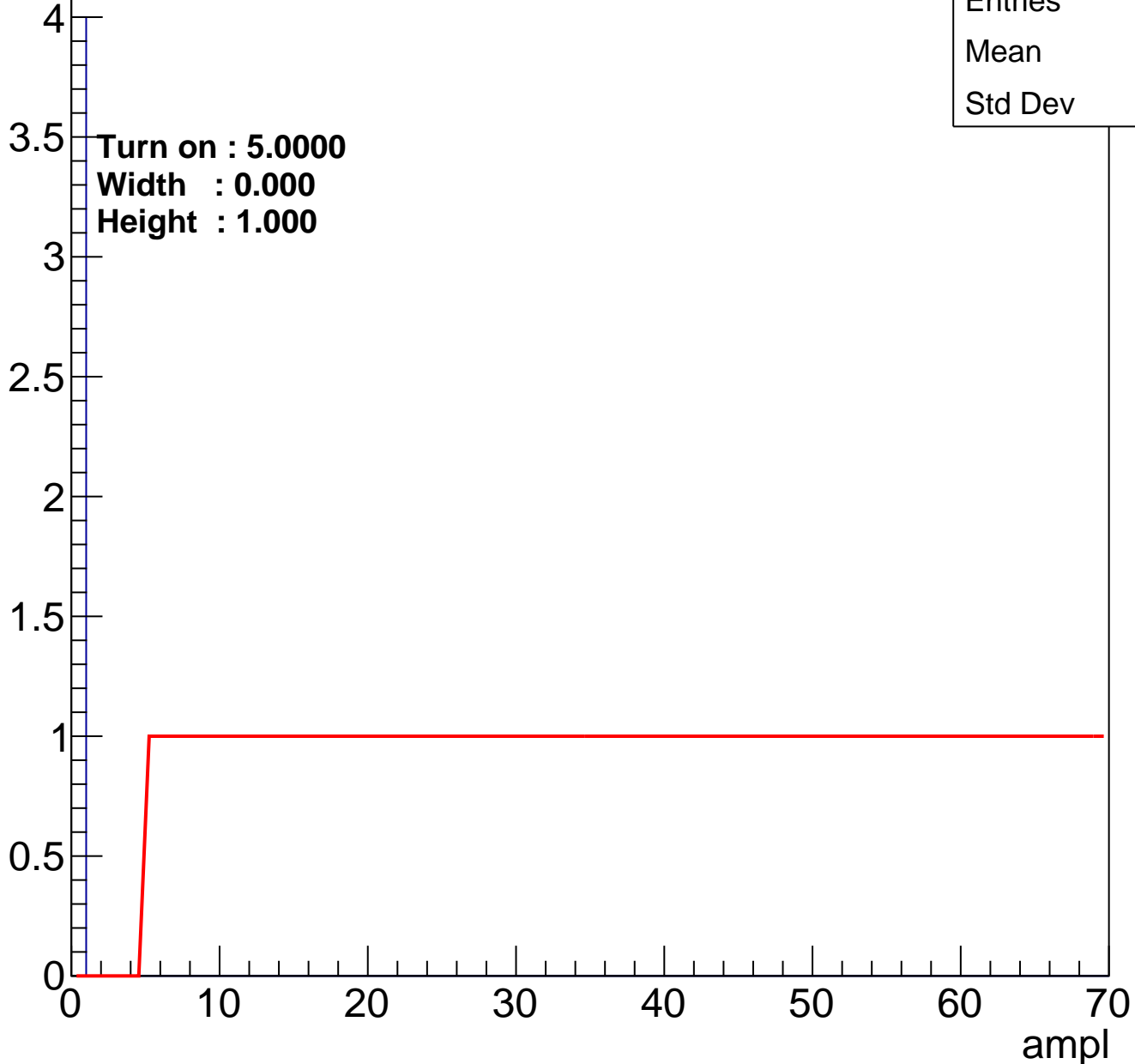
Entry

B0L101S, U7-ch122

calib_packv5_042523_0143.root, FC#1, port C1
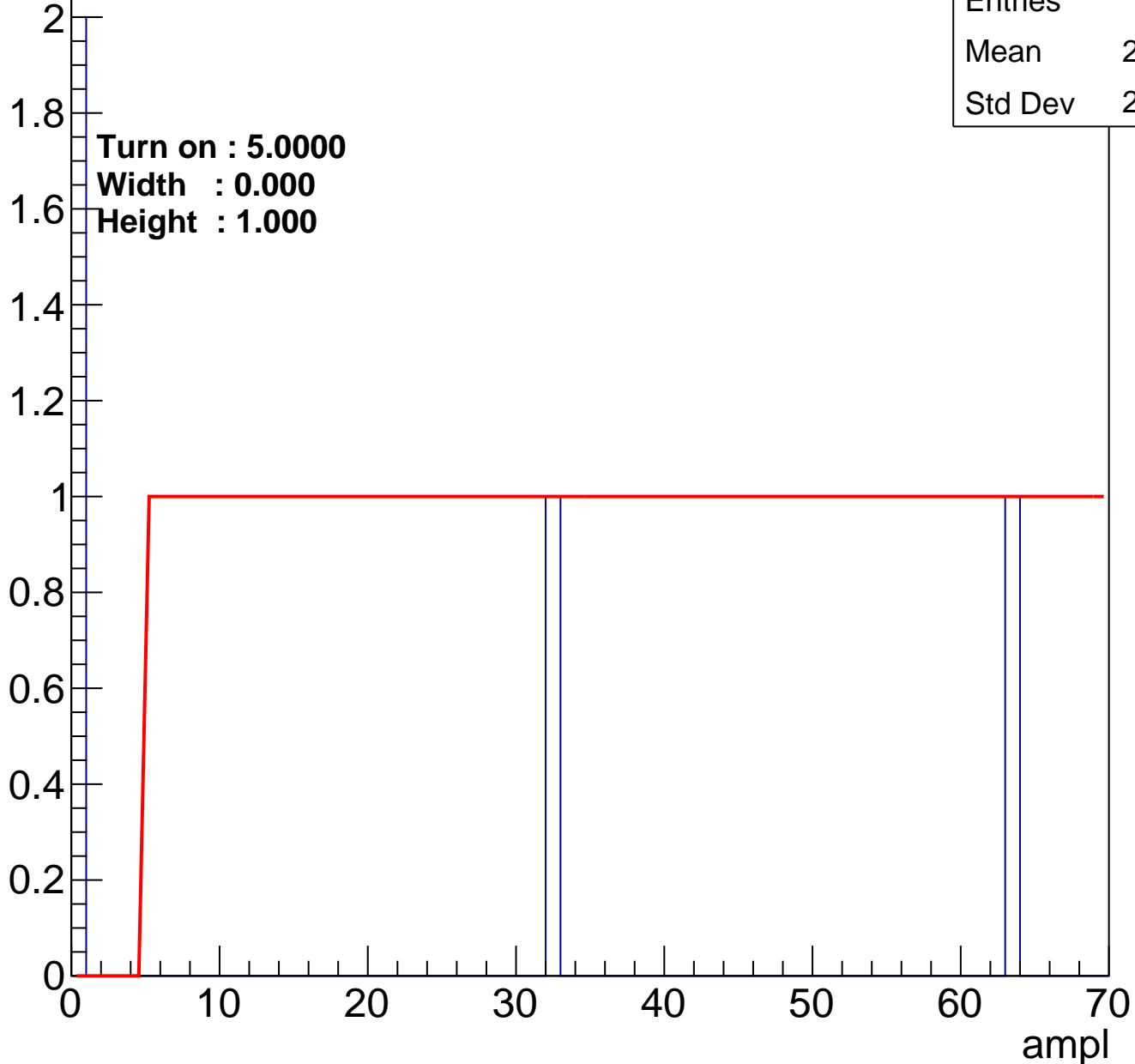
Entries	4
Mean	23.75
Std Dev	26.16

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U7-ch123

calib_packv5_042523_0143.root, FC#1, port C1

Entries	1
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

B0L101S, U7-ch124

calib_packv5_042523_0143.root, FC#1, port C1

Entries	4
Mean	25.5
Std Dev	20.16

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl
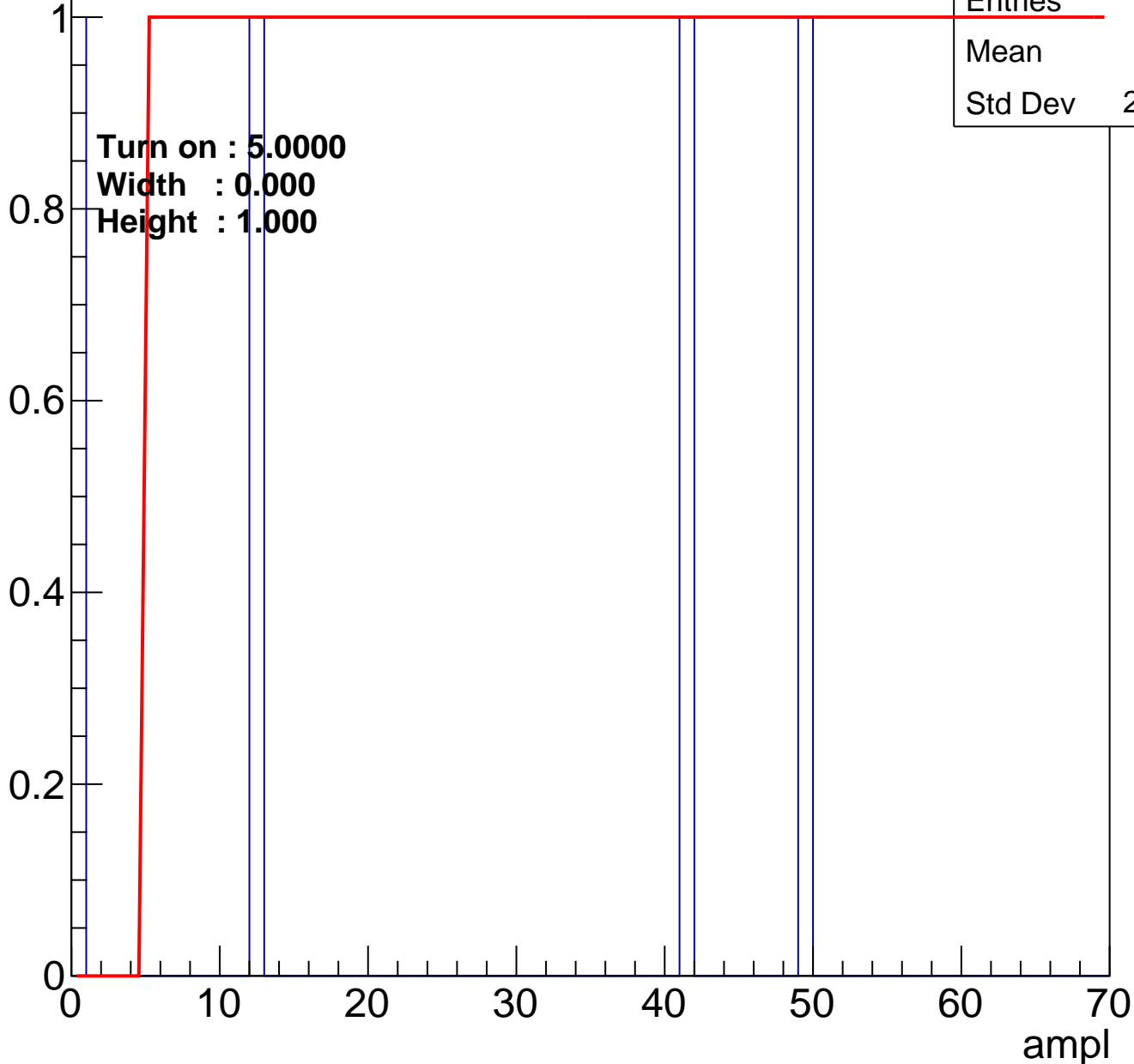
B0L101S, U7-ch125

calib_packv5_042523_0143.root, FC#1, port C1

Entry

	Entries	1
	Mean	0
	Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

ampl

B0L101S, U7-ch126

calib_packv5_042523_0143.root, FC#1, port C1

Entries	17
Mean	29.24
Std Dev	22.35

Turn on : 17.4629
Width   : 3.820
Height : 1.059

B0L101S, U7-ch127

calib_packv5_042523_0143.root, FC#1, port C1

Entries	5
Mean	17.4
Std Dev	21.33

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl
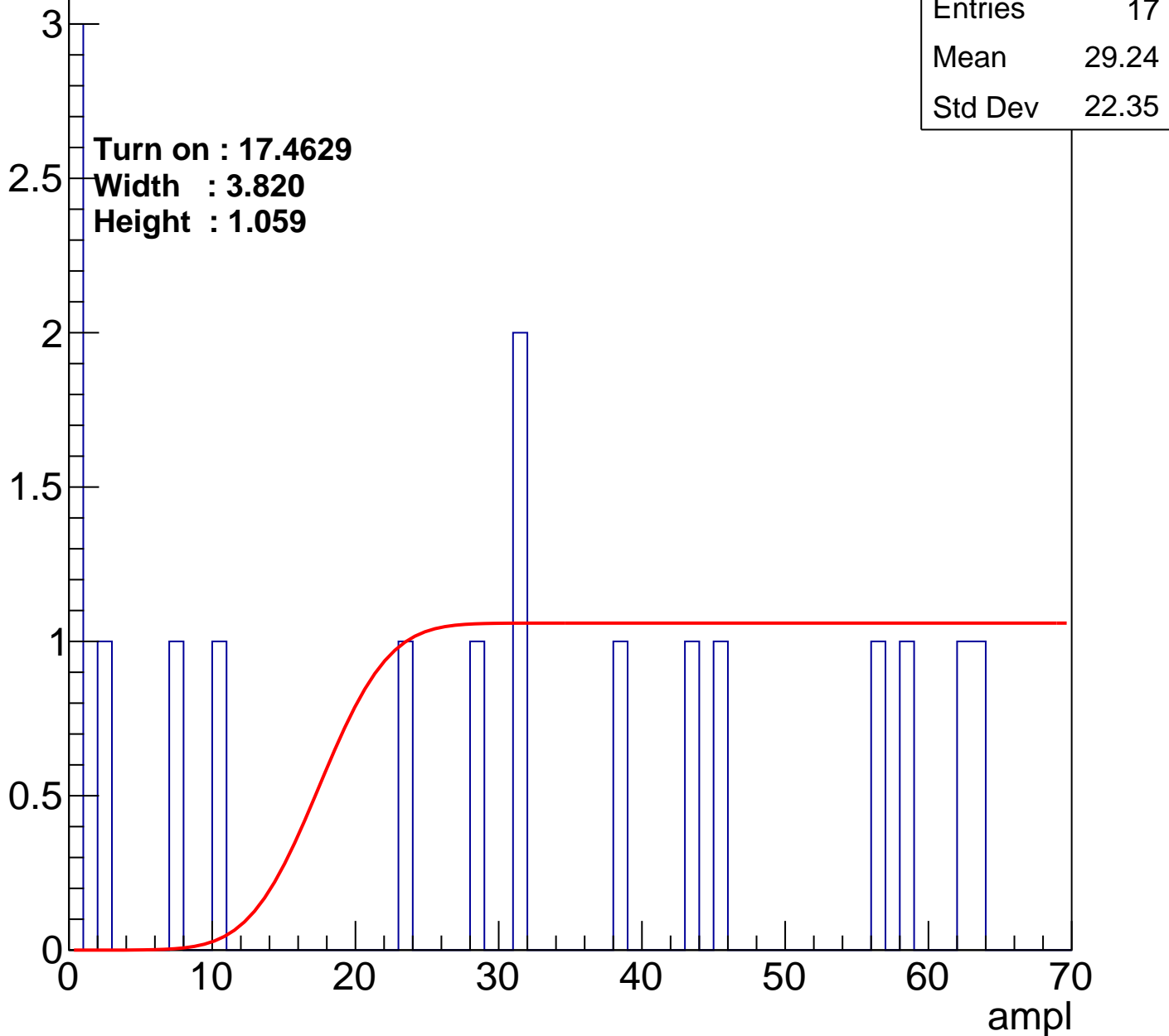
B0L101S, U7-ch127

calib_packv5_042523_0143.root, FC#1, port C1

Entry

Entries	5
Mean	17.4
Std Dev	21.33

Turn on : 5.0000
Width   : 0.000
Height : 1.000

ampl