

B1L103S, U9-ch0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	460
Mean	37.98
Std Dev	17.86

Turn on : 24.2646

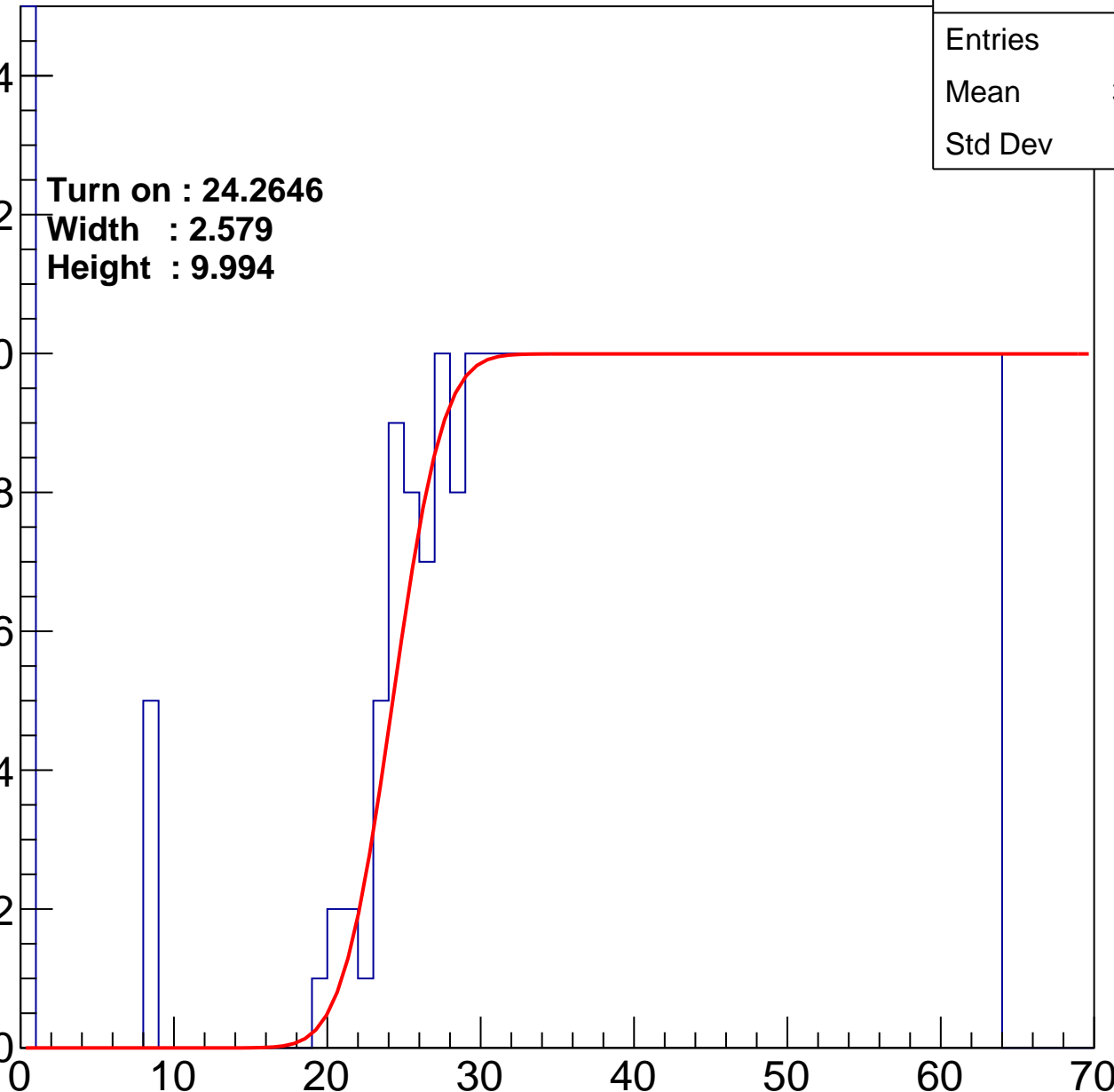
Width : 2.579

Height : 9.994

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	420
Mean	39.86
Std Dev	17.29

Turn on : 26.5768

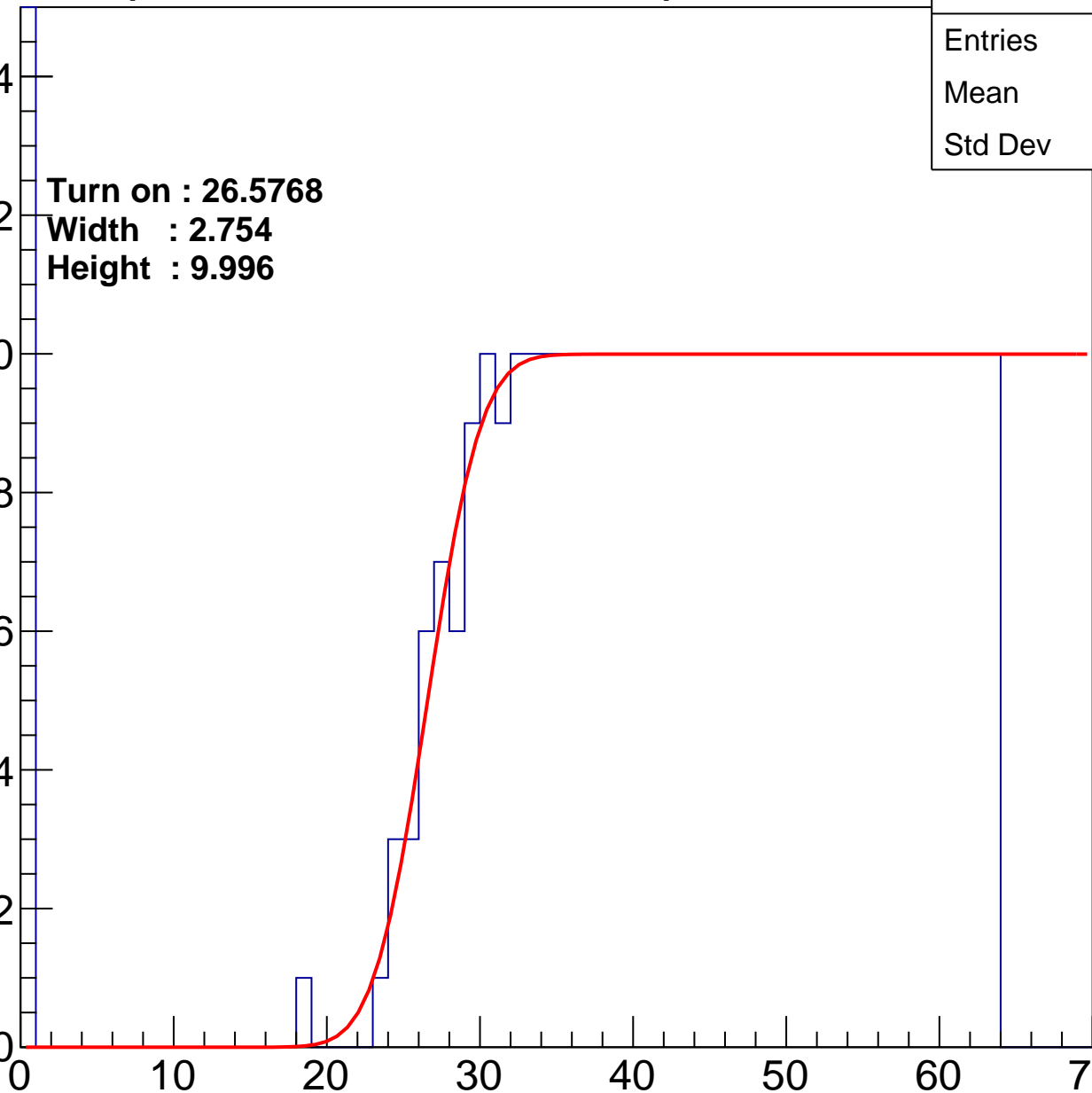
Width : 2.754

Height : 9.996

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	440
Mean	39.3
Std Dev	17

Turn on : 24.4384

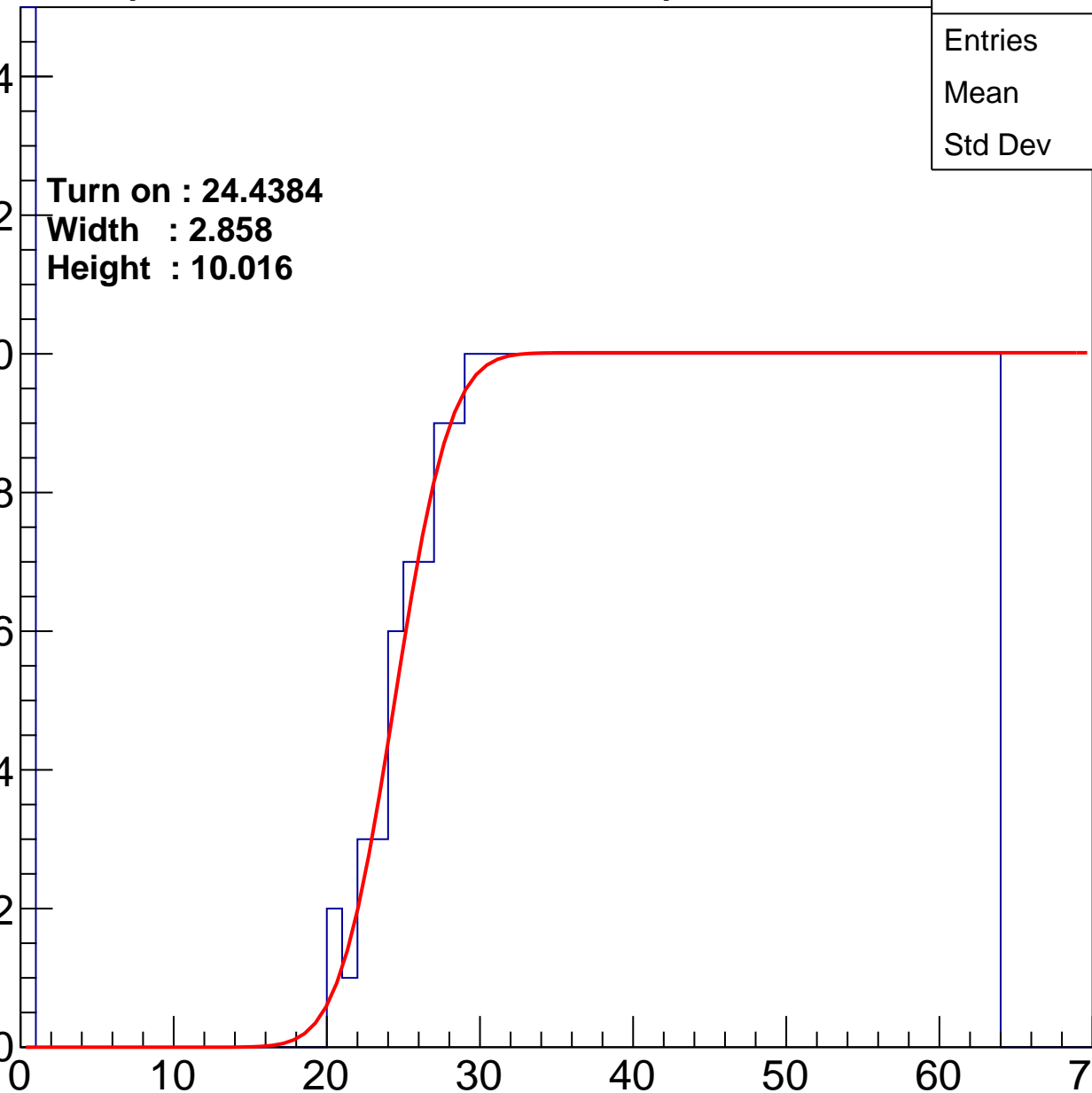
Width : 2.858

Height : 10.016

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch3

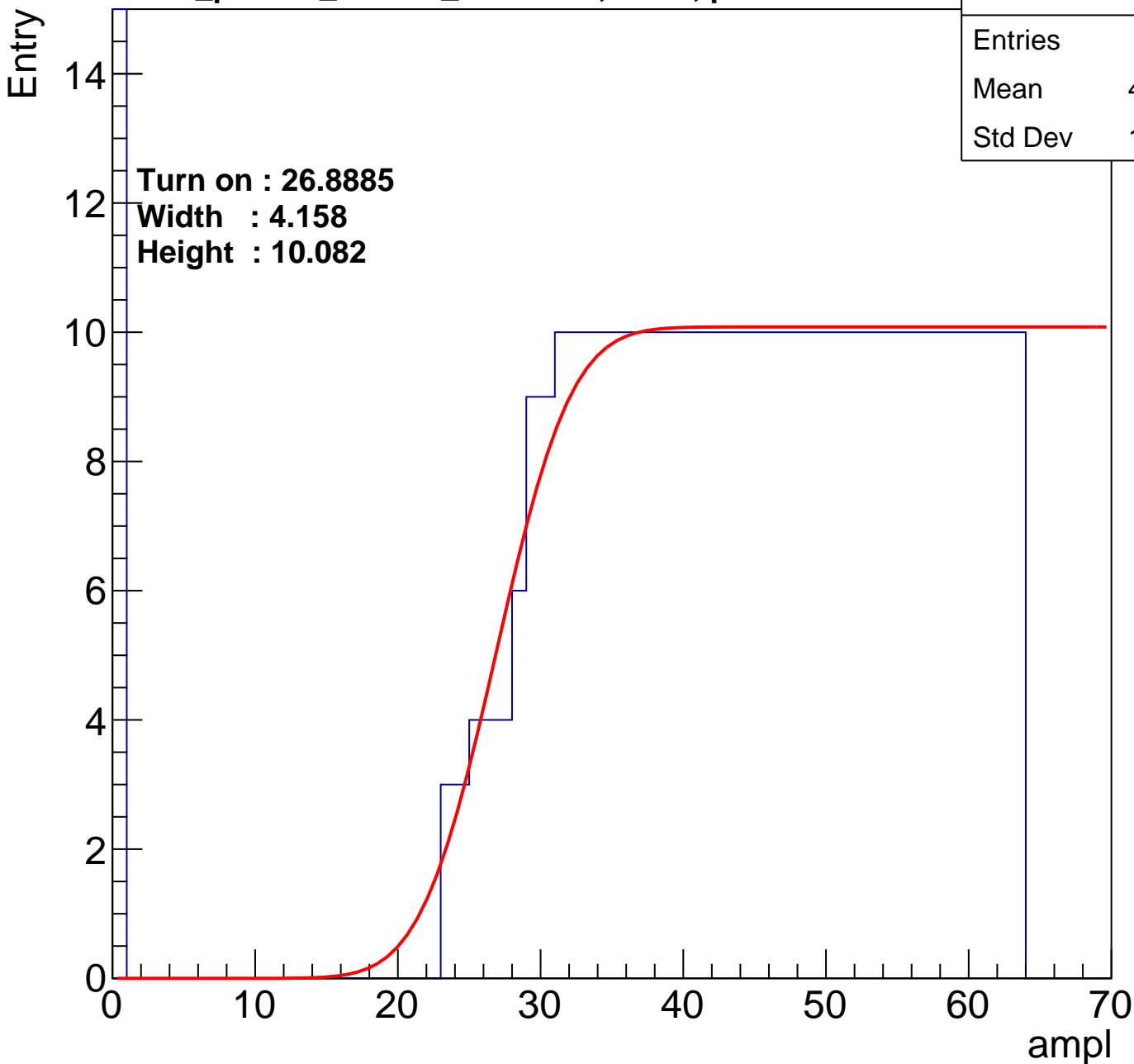
calib_packv5_041523_1651.root, FC#0, port C2

Entries	412
Mean	40.44
Std Dev	16.84

Turn on : 26.8885

Width : 4.158

Height : 10.082



B1L103S, U9-ch4

calib_packv5_041523_1651.root, FC#0, port C2

Entries	411
Mean	40.47
Std Dev	16.85

Turn on : 27.0082

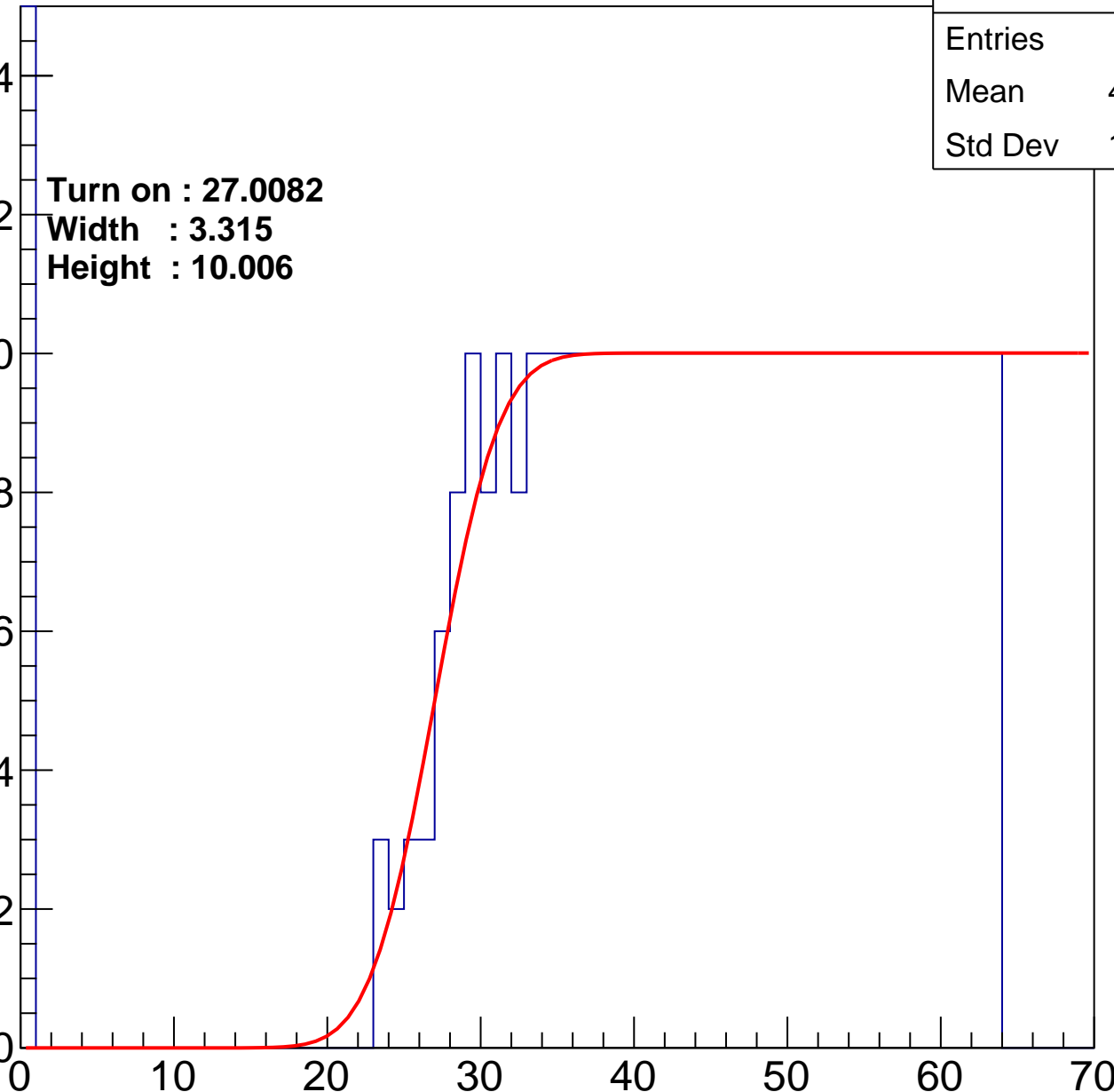
Width : 3.315

Height : 10.006

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch5

calib_packv5_041523_1651.root, FC#0, port C2

Entries	411
Mean	40.81
Std Dev	16.3

Turn on : 26.4325

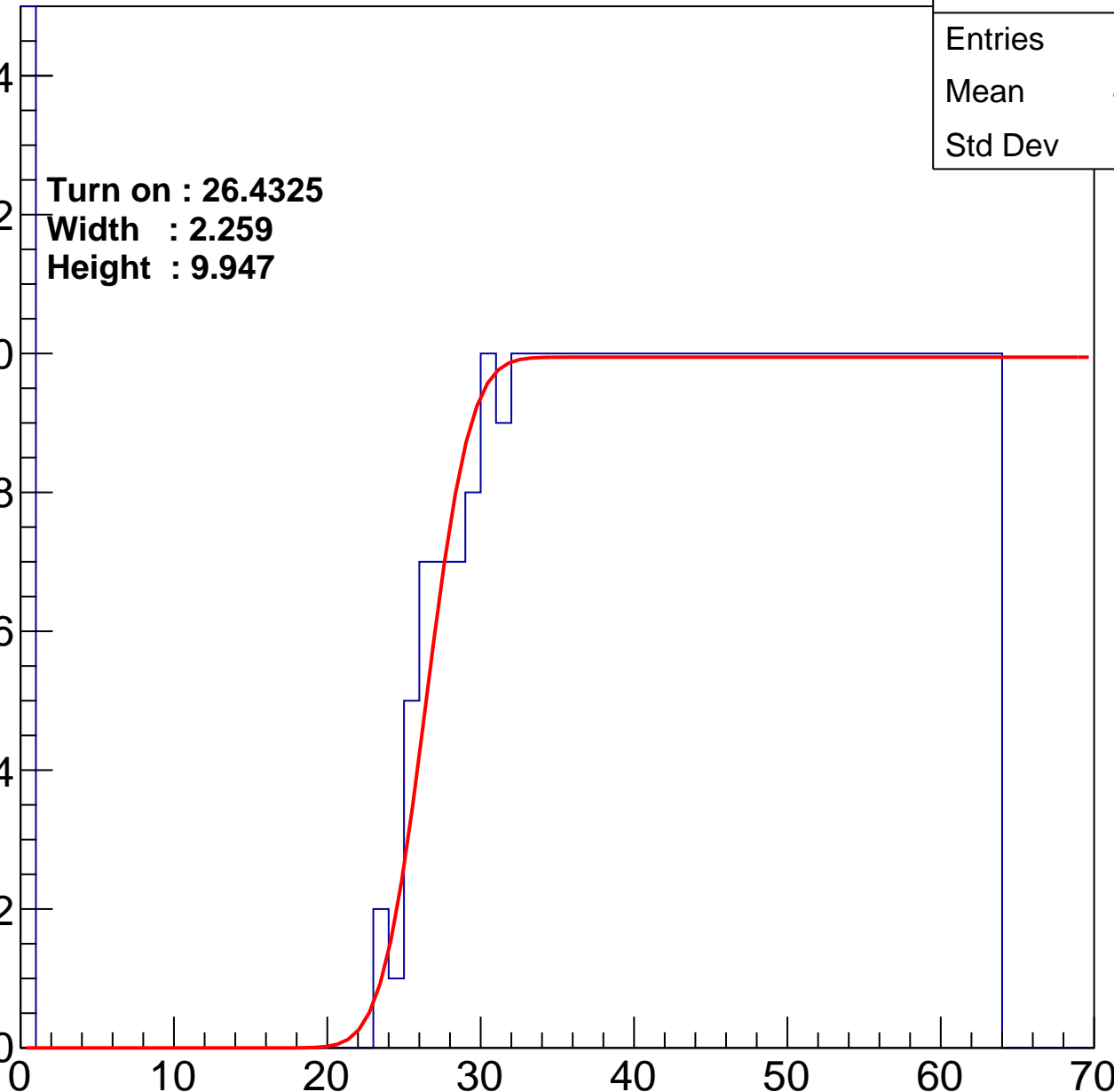
Width : 2.259

Height : 9.947

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch6

calib_packv5_041523_1651.root, FC#0, port C2

Entries	432
Mean	39.37
Std Dev	17.37

Turn on : 25.5833

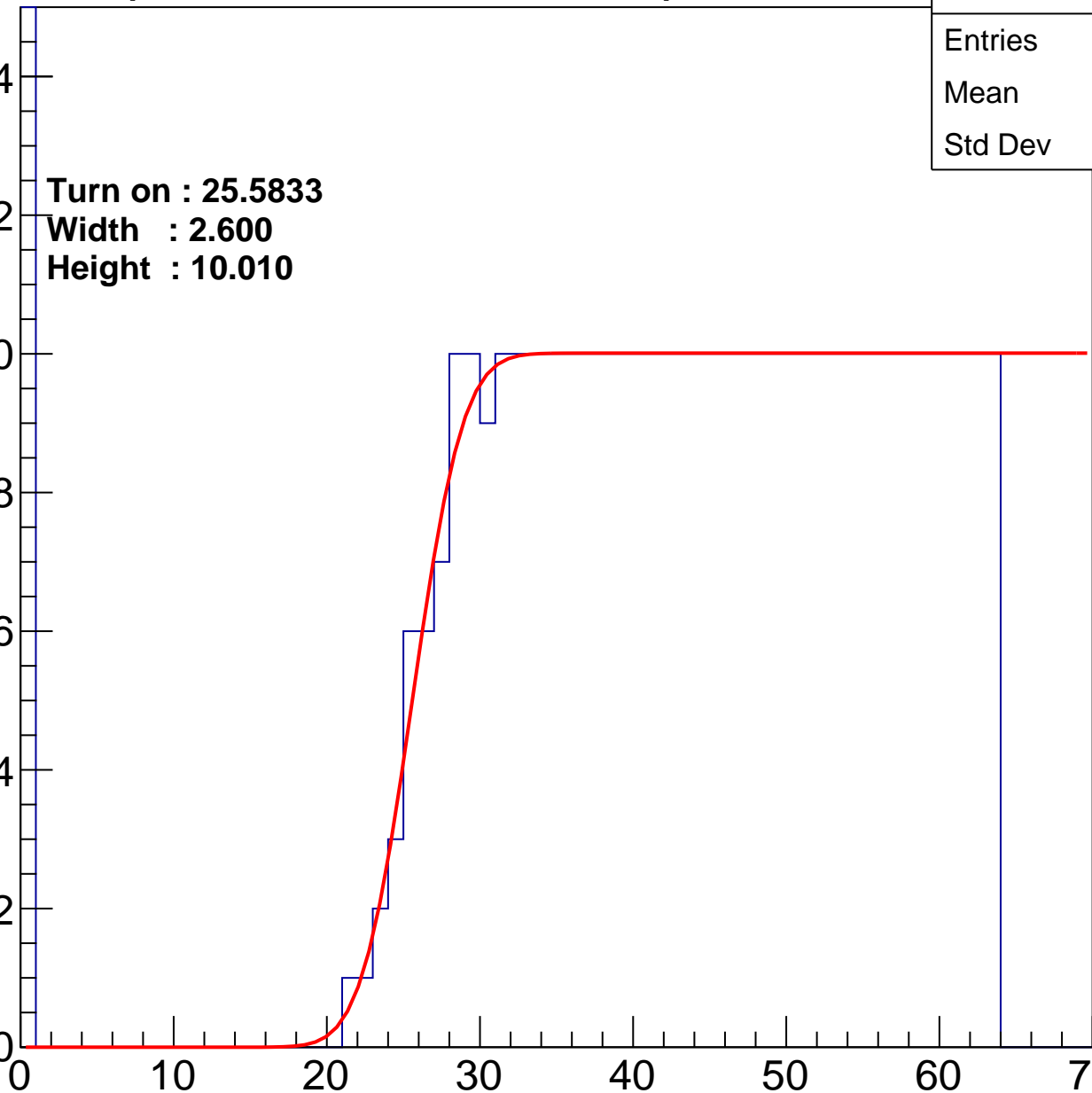
Width : 2.600

Height : 10.010

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	396
Mean	40.95
Std Dev	17.03

Turn on : 28.7957

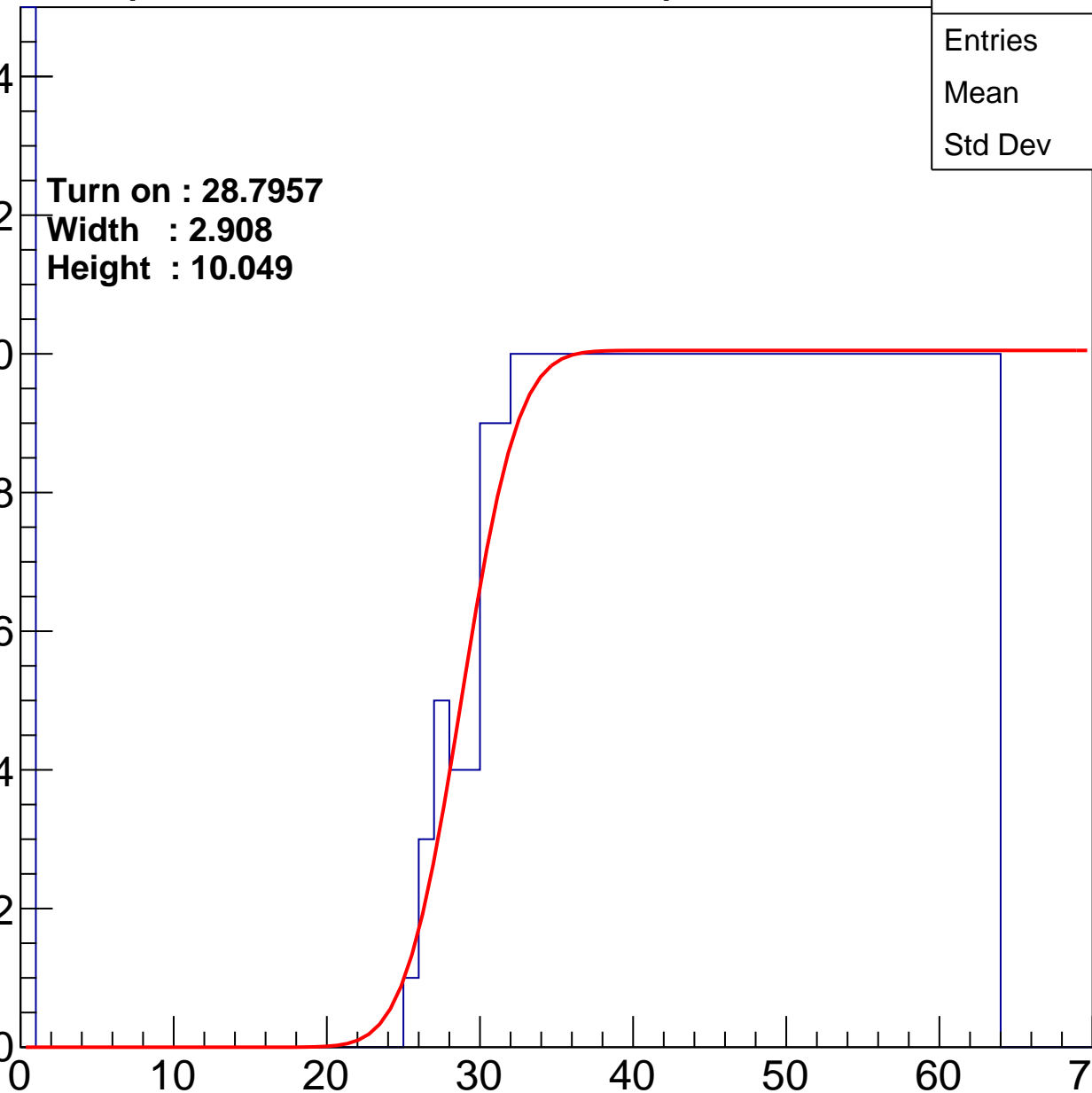
Width : 2.908

Height : 10.049

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch8

calib_packv5_041523_1651.root, FC#0, port C2

Entries	412
Mean	41.15
Std Dev	15.65

Turn on : 25.6293

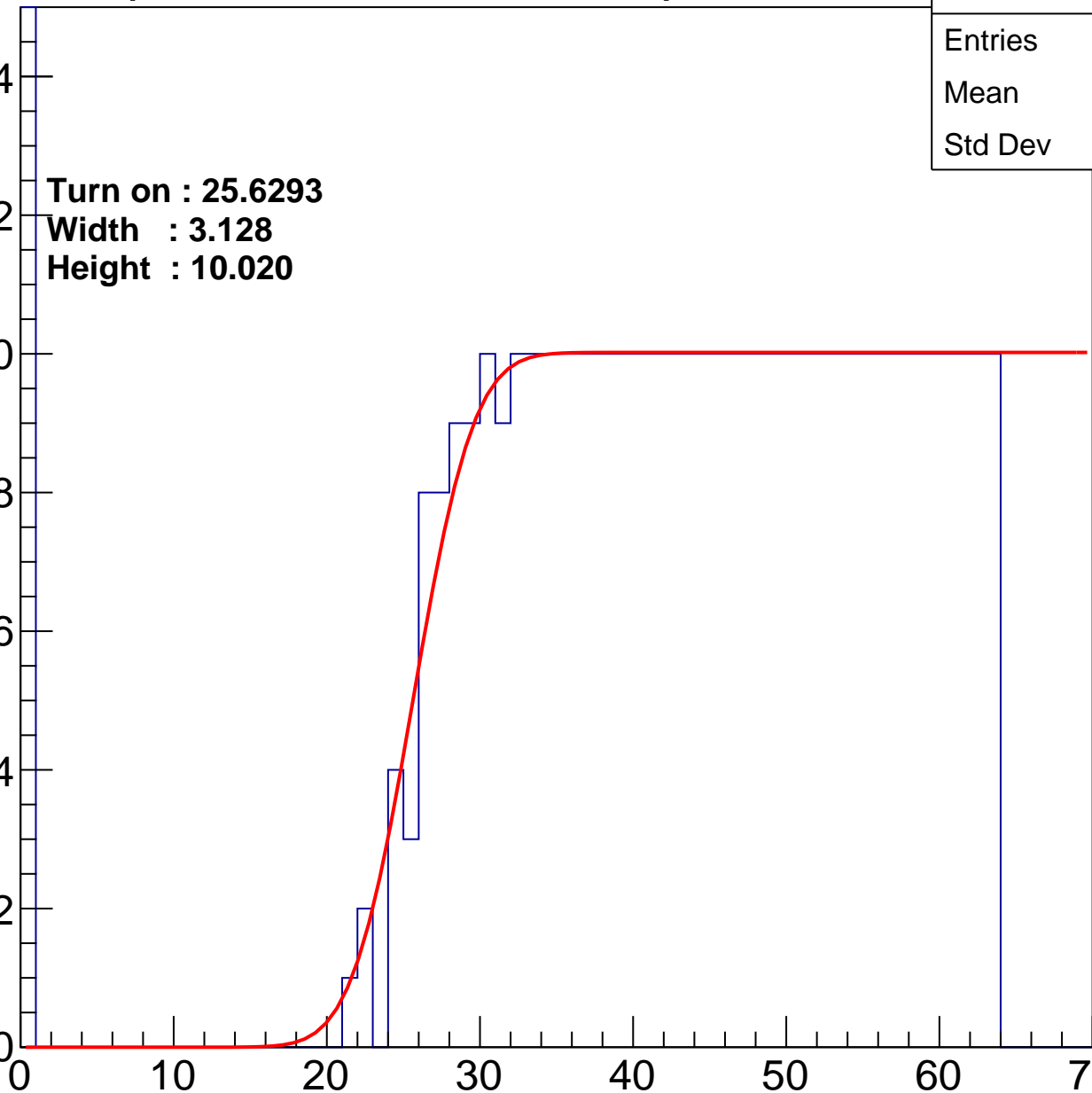
Width : 3.128

Height : 10.020

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch9

calib_packv5_041523_1651.root, FC#0, port C2

Entries	435
Mean	39.6
Std Dev	16.79

Turn on : 25.1308

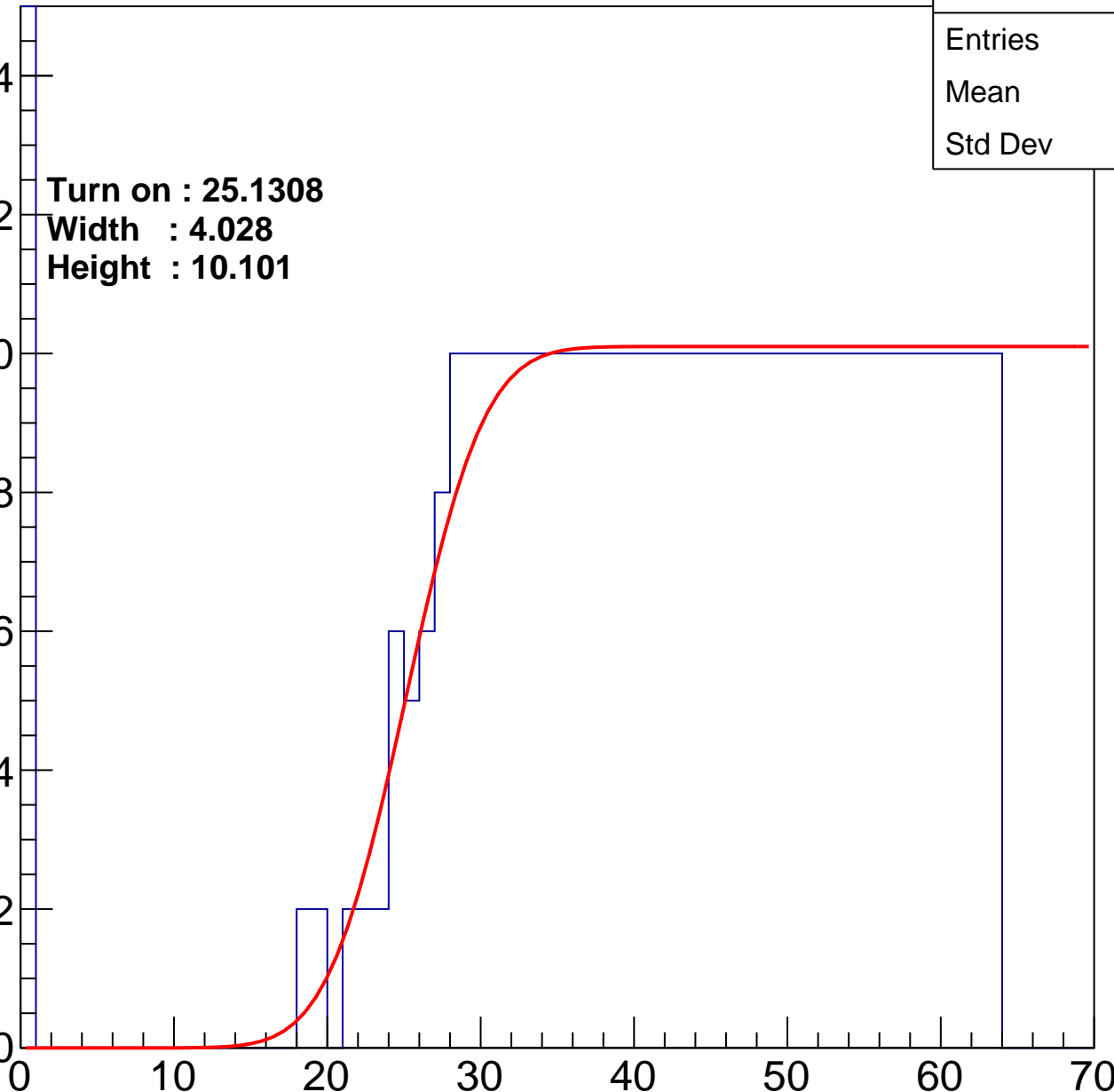
Width : 4.028

Height : 10.101

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch10

calib_packv5_041523_1651.root, FC#0, port C2

Entries	448
Mean	39.07
Std Dev	16.9

Turn on : 23.4247

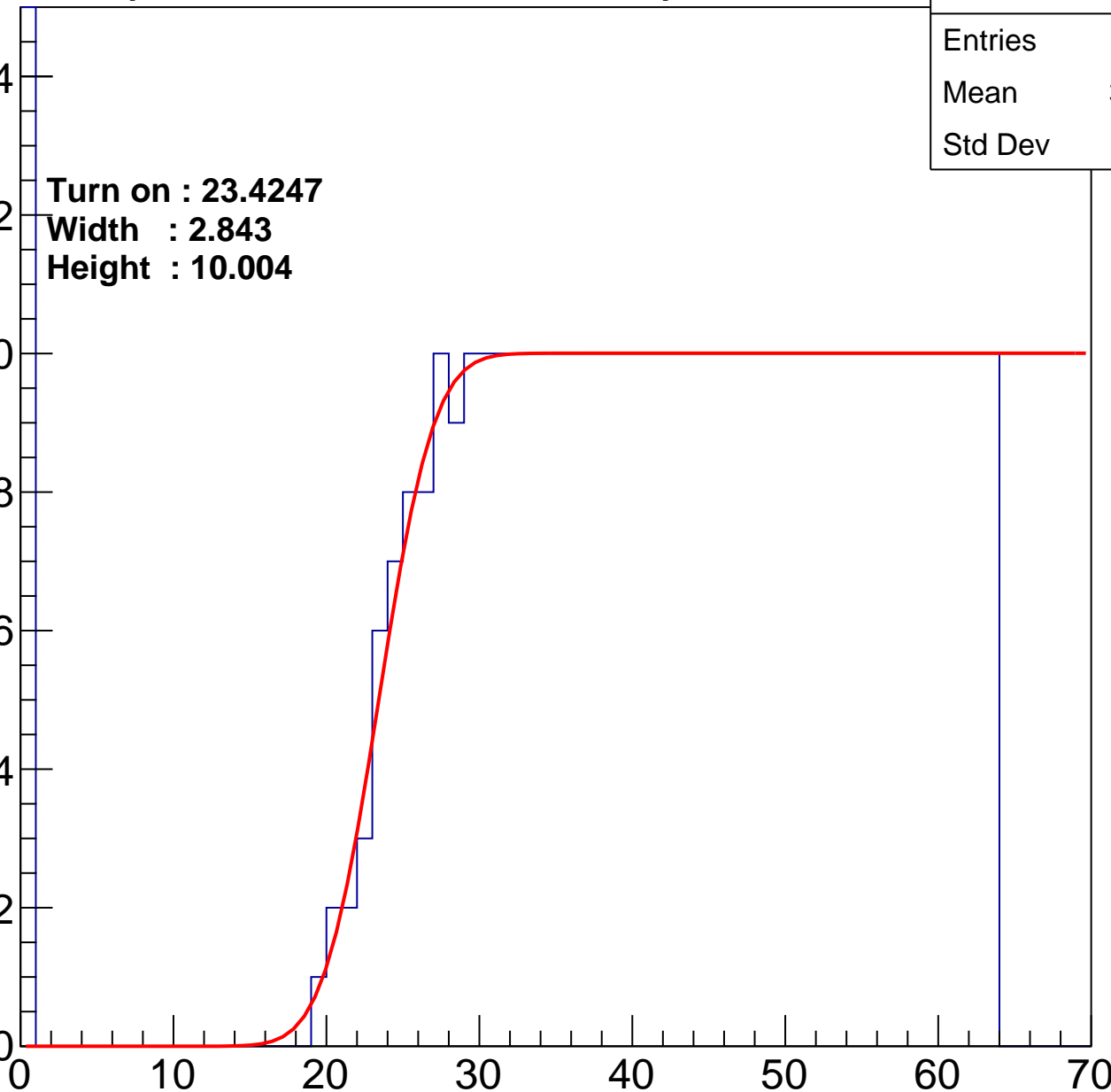
Width : 2.843

Height : 10.004

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch11

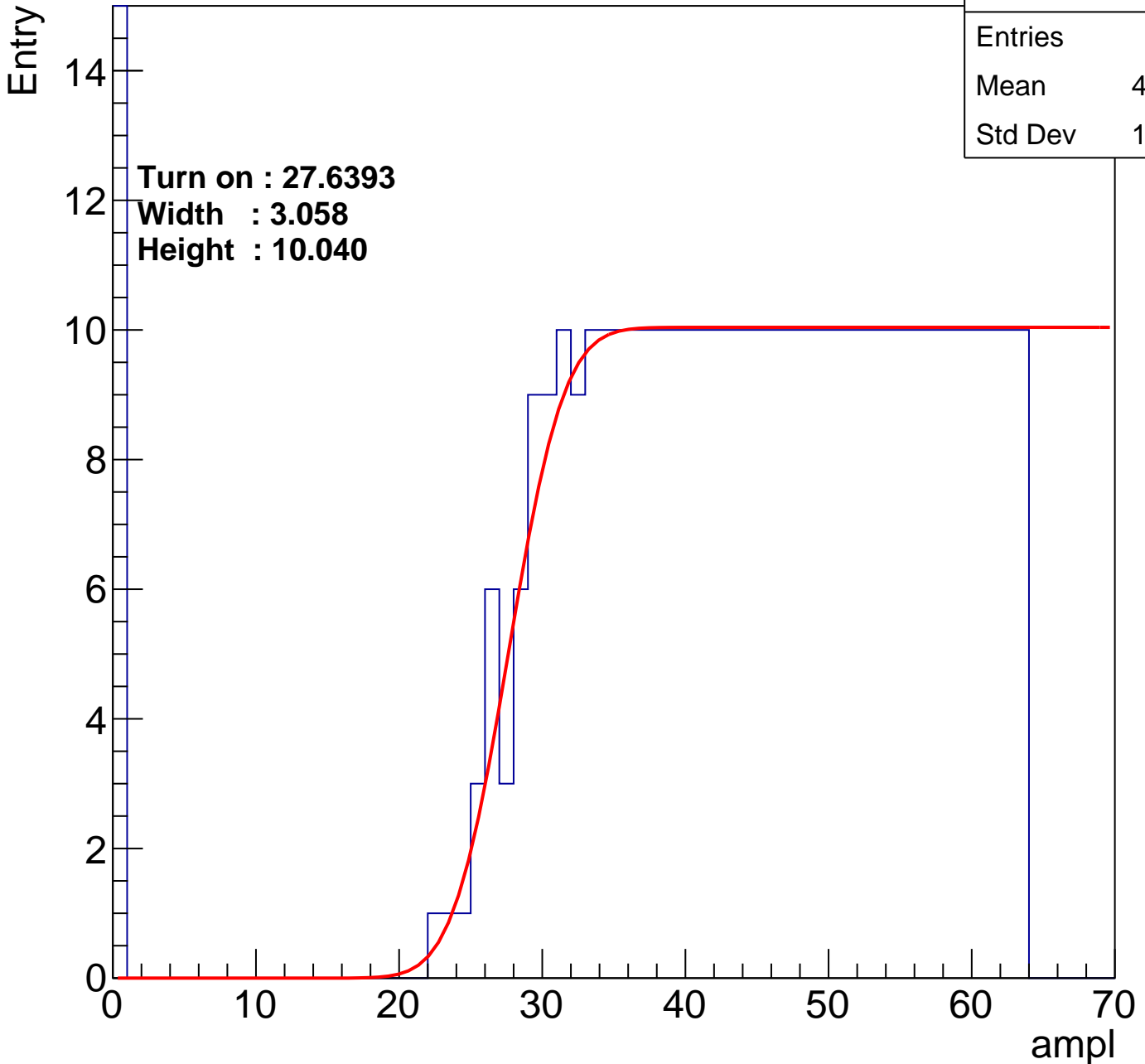
calib_packv5_041523_1651.root, FC#0, port C2

Entries	407
Mean	40.68
Std Dev	16.76

Turn on : 27.6393

Width : 3.058

Height : 10.040



B1L103S, U9-ch12

calib_packv5_041523_1651.root, FC#0, port C2

Entries	422
Mean	39.67
Std Dev	17.46

Turn on : 26.9734

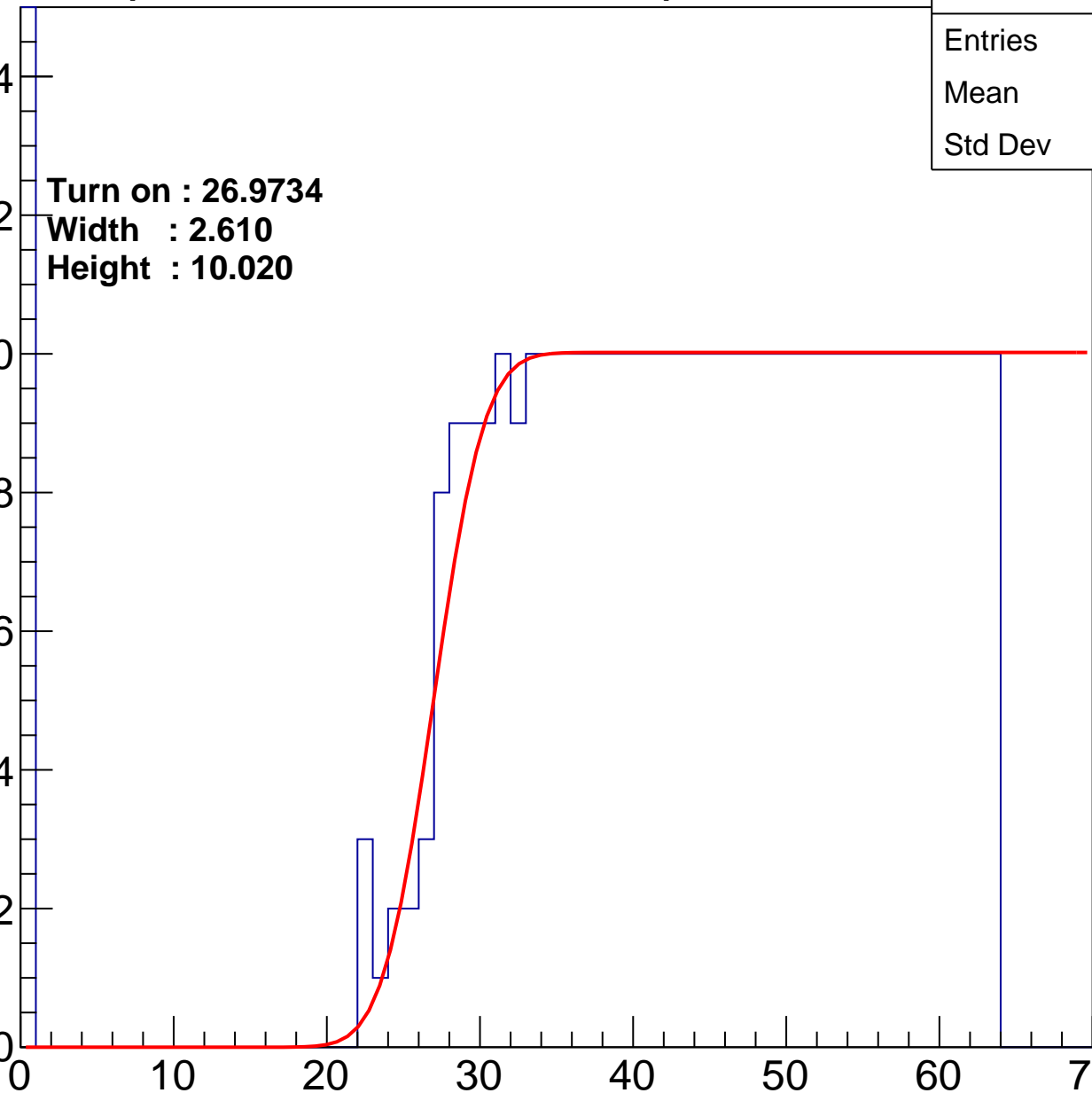
Width : 2.610

Height : 10.020

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch13

calib_packv5_041523_1651.root, FC#0, port C2

Entries	413
Mean	40.41
Std Dev	16.83

Turn on : 26.8720

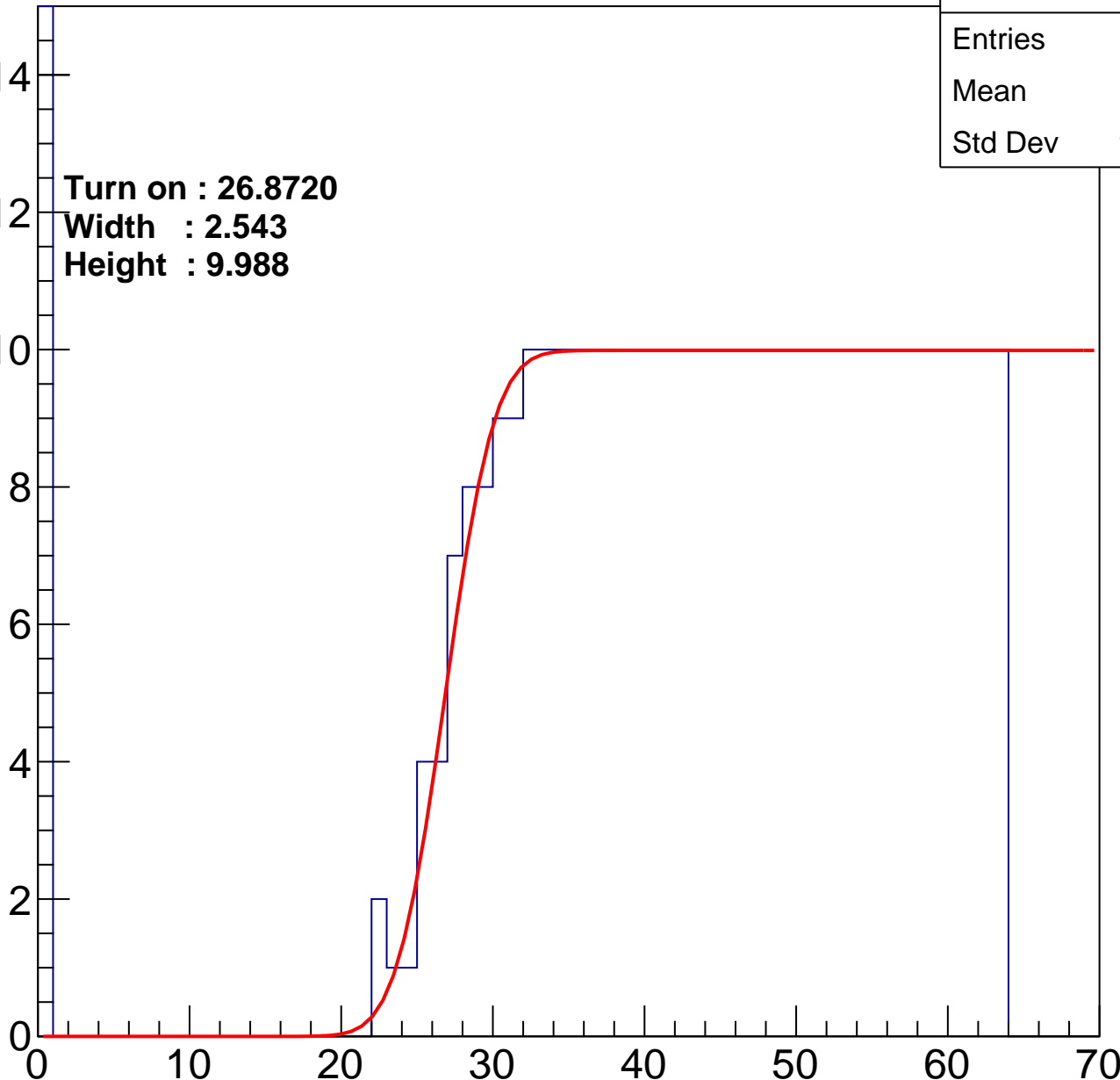
Width : 2.543

Height : 9.988

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch14

calib_packv5_041523_1651.root, FC#0, port C2

Entries	416
Mean	40.49
Std Dev	16.52

Turn on : 26.6591

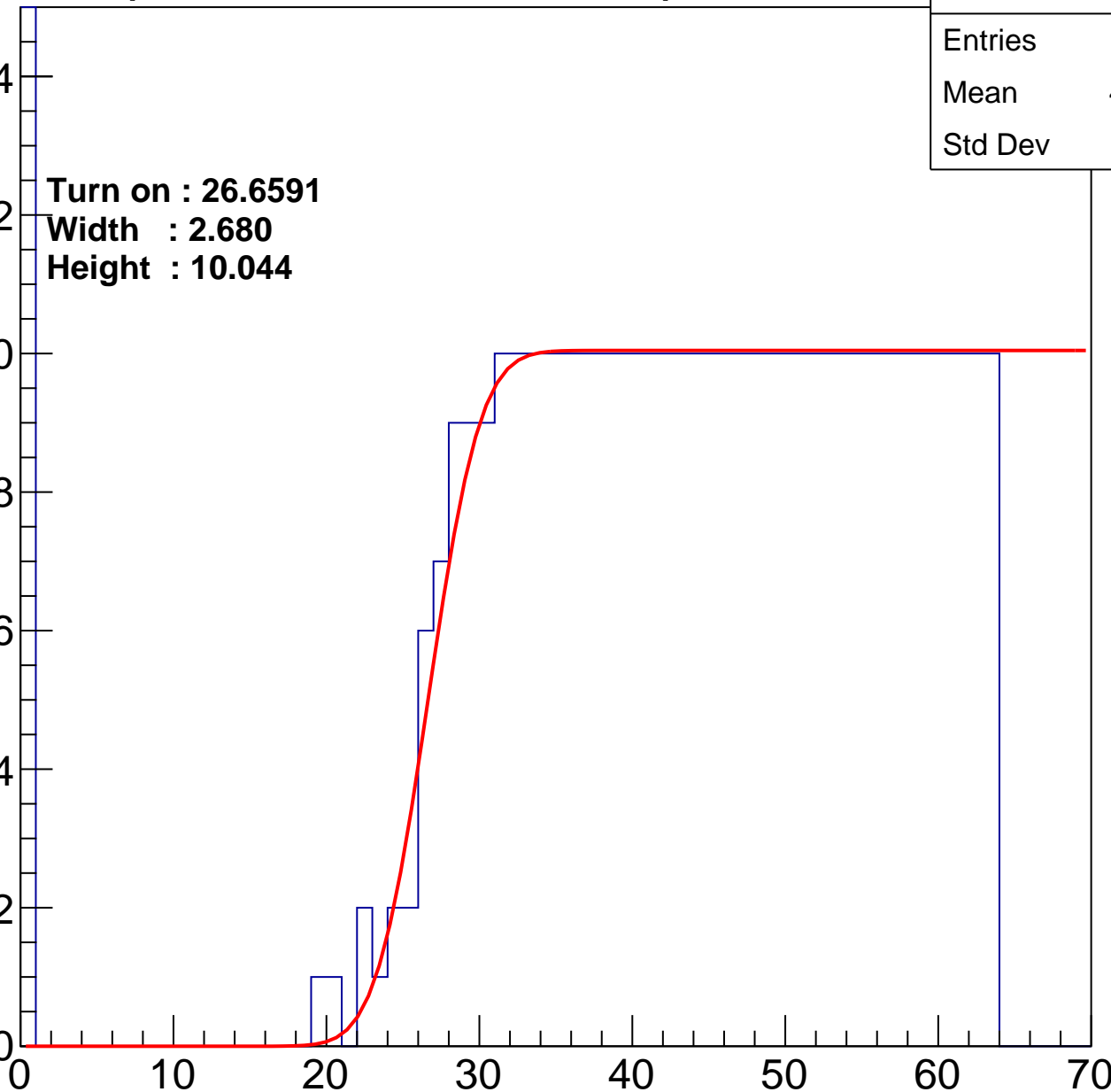
Width : 2.680

Height : 10.044

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch15

calib_packv5_041523_1651.root, FC#0, port C2

Entries	407
Mean	41.04
Std Dev	16.14

Turn on : 27.1011

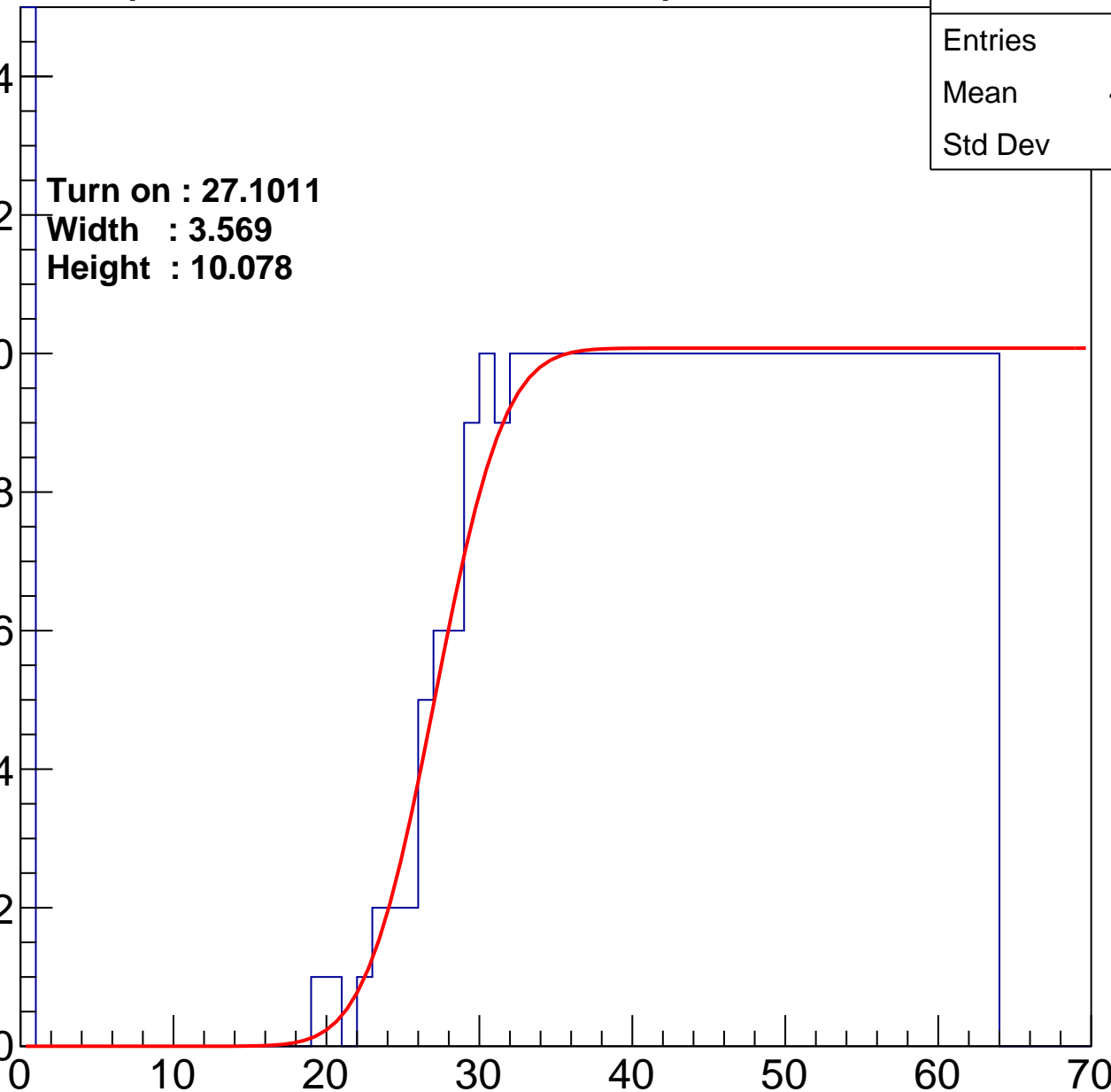
Width : 3.569

Height : 10.078

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch16

calib_packv5_041523_1651.root, FC#0, port C2

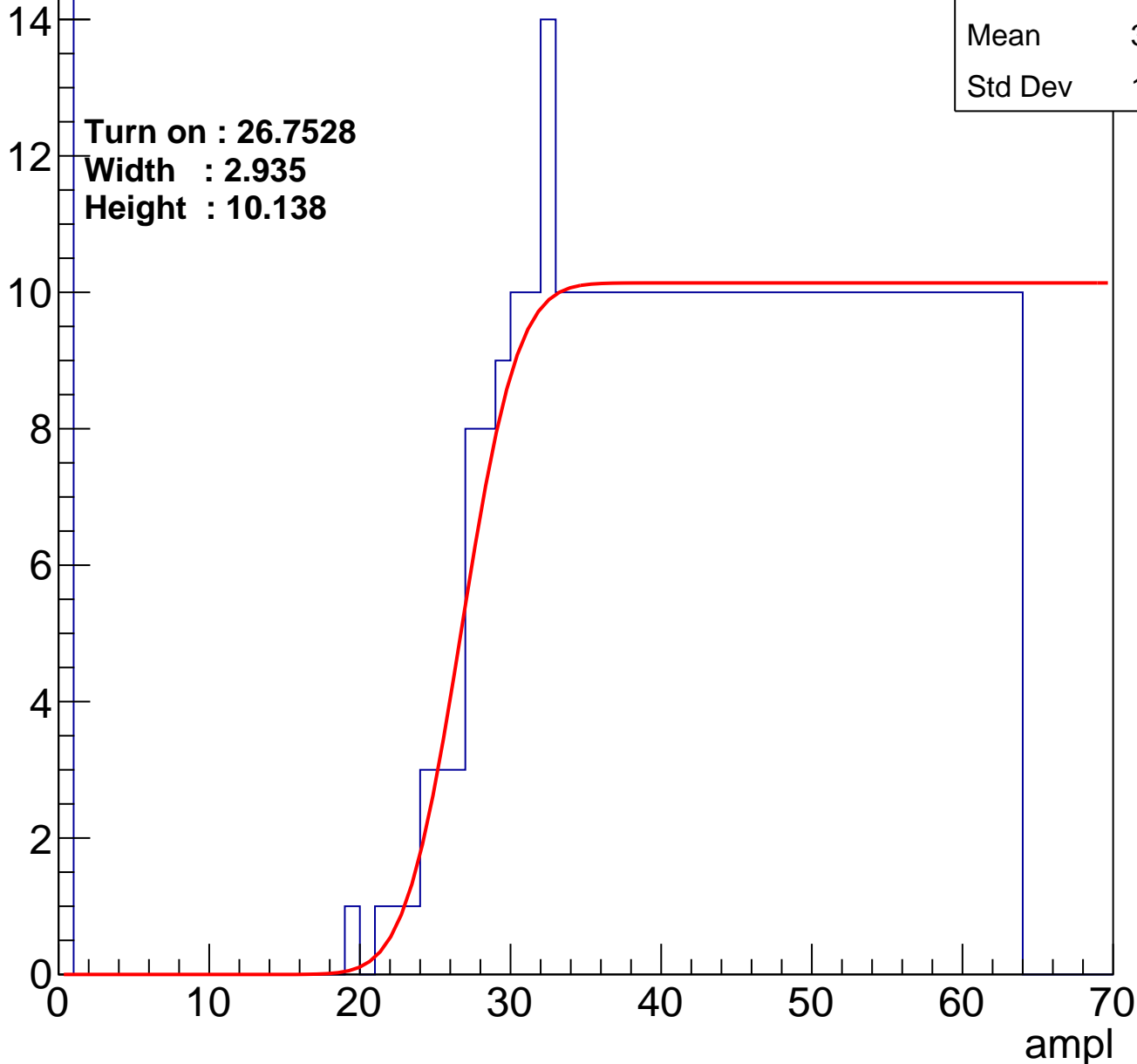
Entries	424
Mean	39.97
Std Dev	16.93

Turn on : 26.7528

Width : 2.935

Height : 10.138

Entry



B1L103S, U9-ch17

calib_packv5_041523_1651.root, FC#0, port C2

Entries	437
Mean	38.98
Std Dev	17.69

Turn on : 25.4655

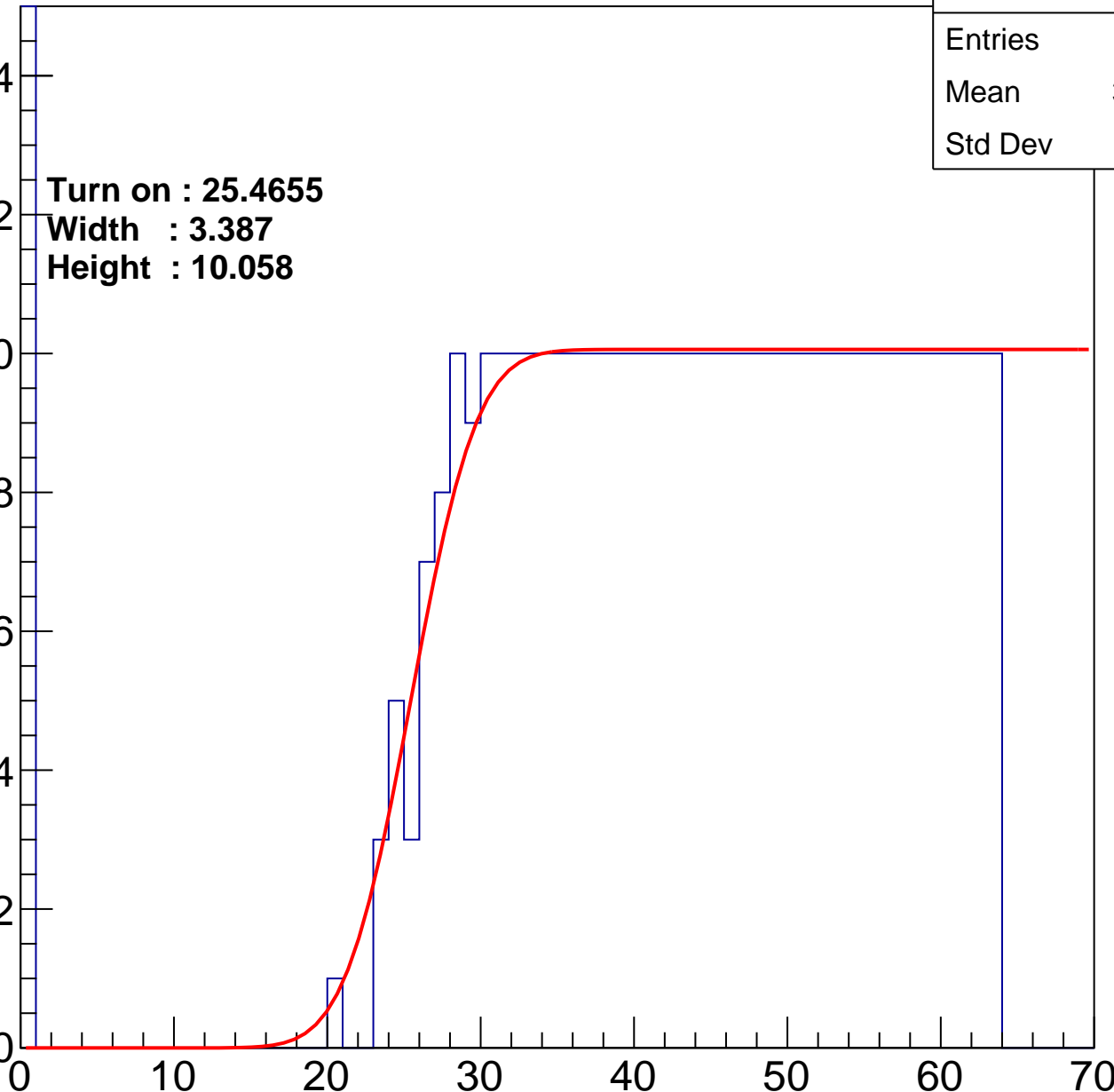
Width : 3.387

Height : 10.058

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch18

calib_packv5_041523_1651.root, FC#0, port C2

Entries	407
Mean	40.45
Std Dev	17.15

Turn on : 27.6510

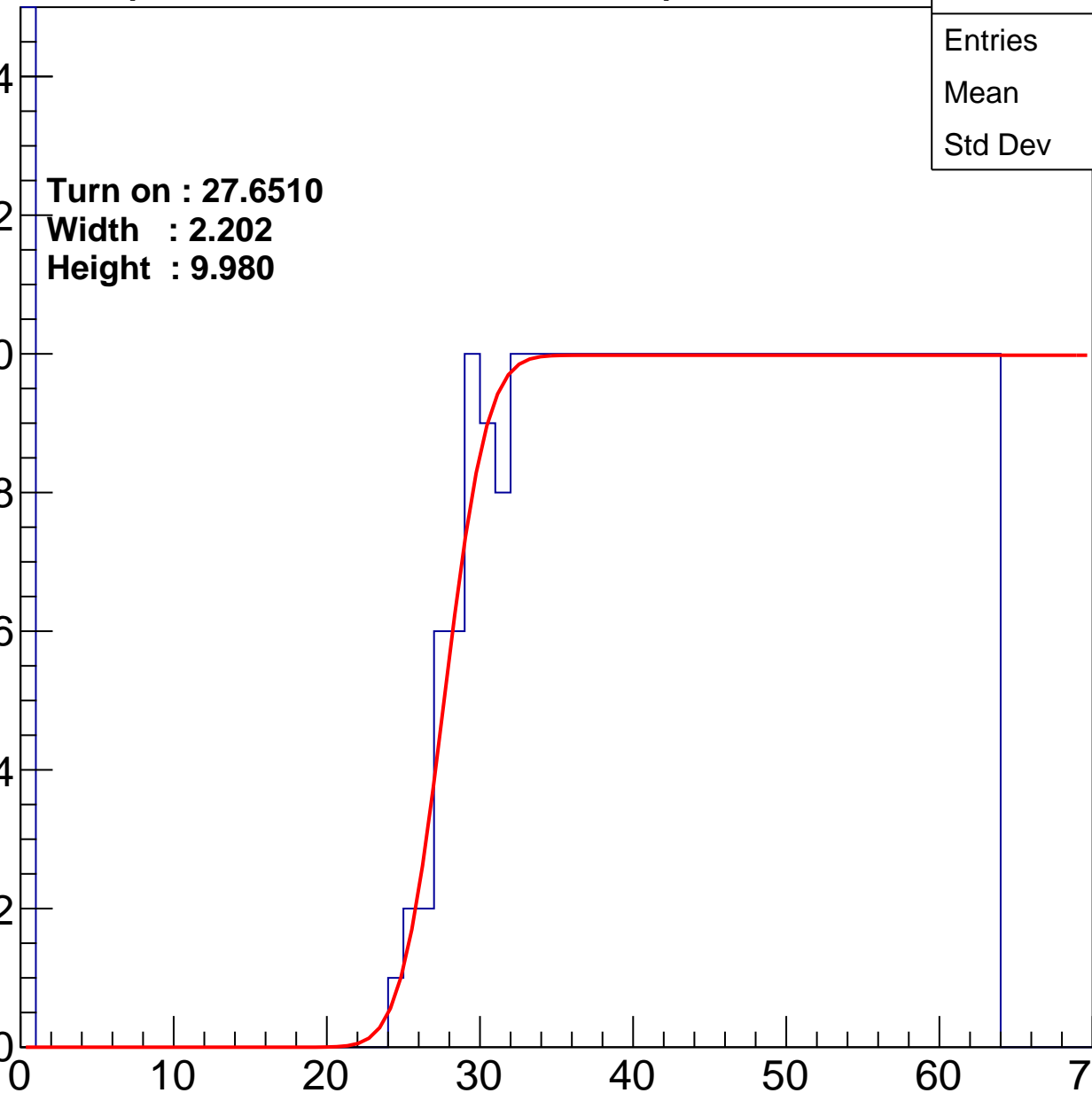
Width : 2.202

Height : 9.980

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch19

calib_packv5_041523_1651.root, FC#0, port C2

Entries	396
Mean	41.28
Std Dev	16.48

Turn on : 27.9509

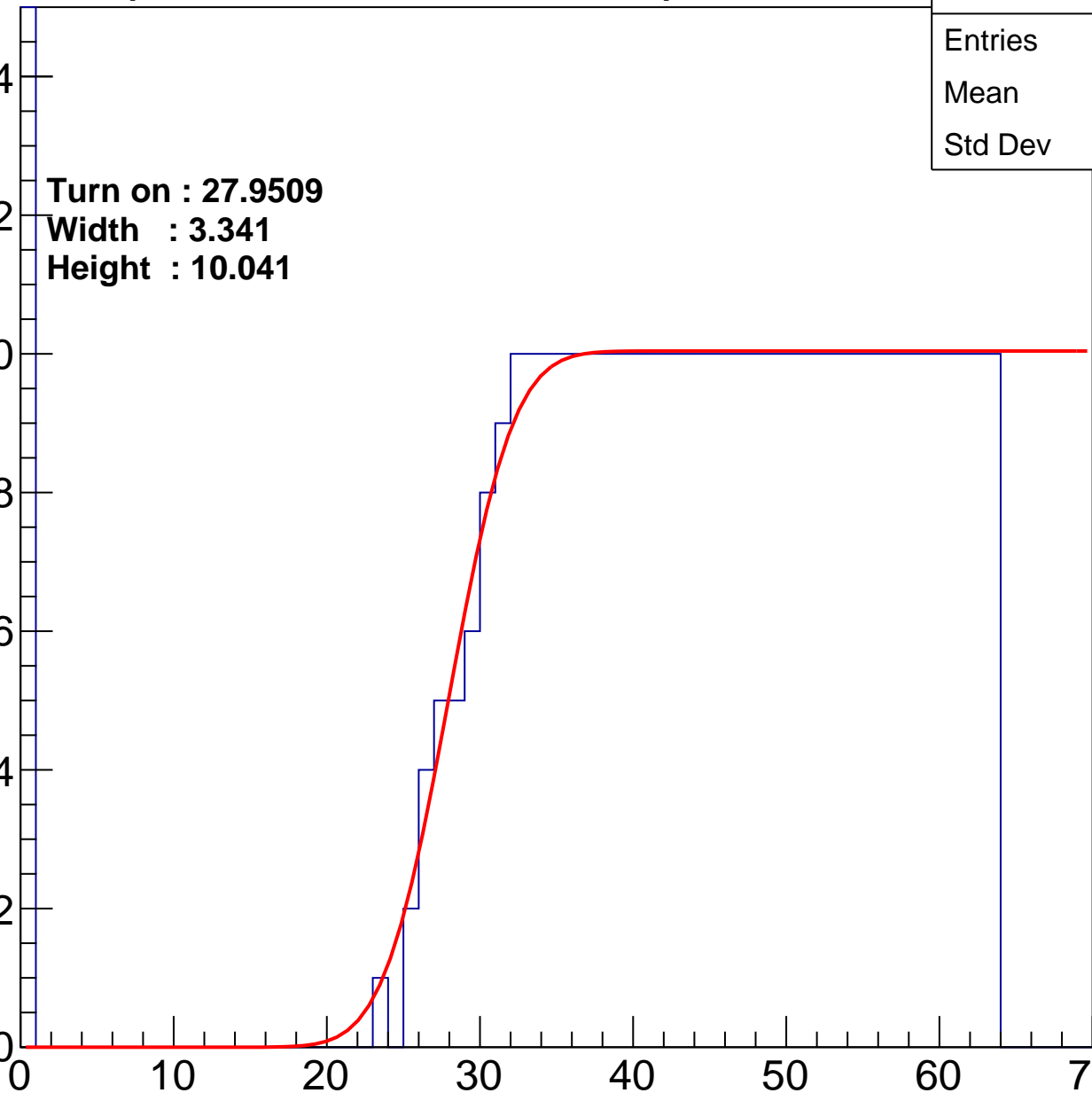
Width : 3.341

Height : 10.041

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch20

calib_packv5_041523_1651.root, FC#0, port C2

Entries	413
Mean	40.38
Std Dev	16.9

Turn on : 26.8857

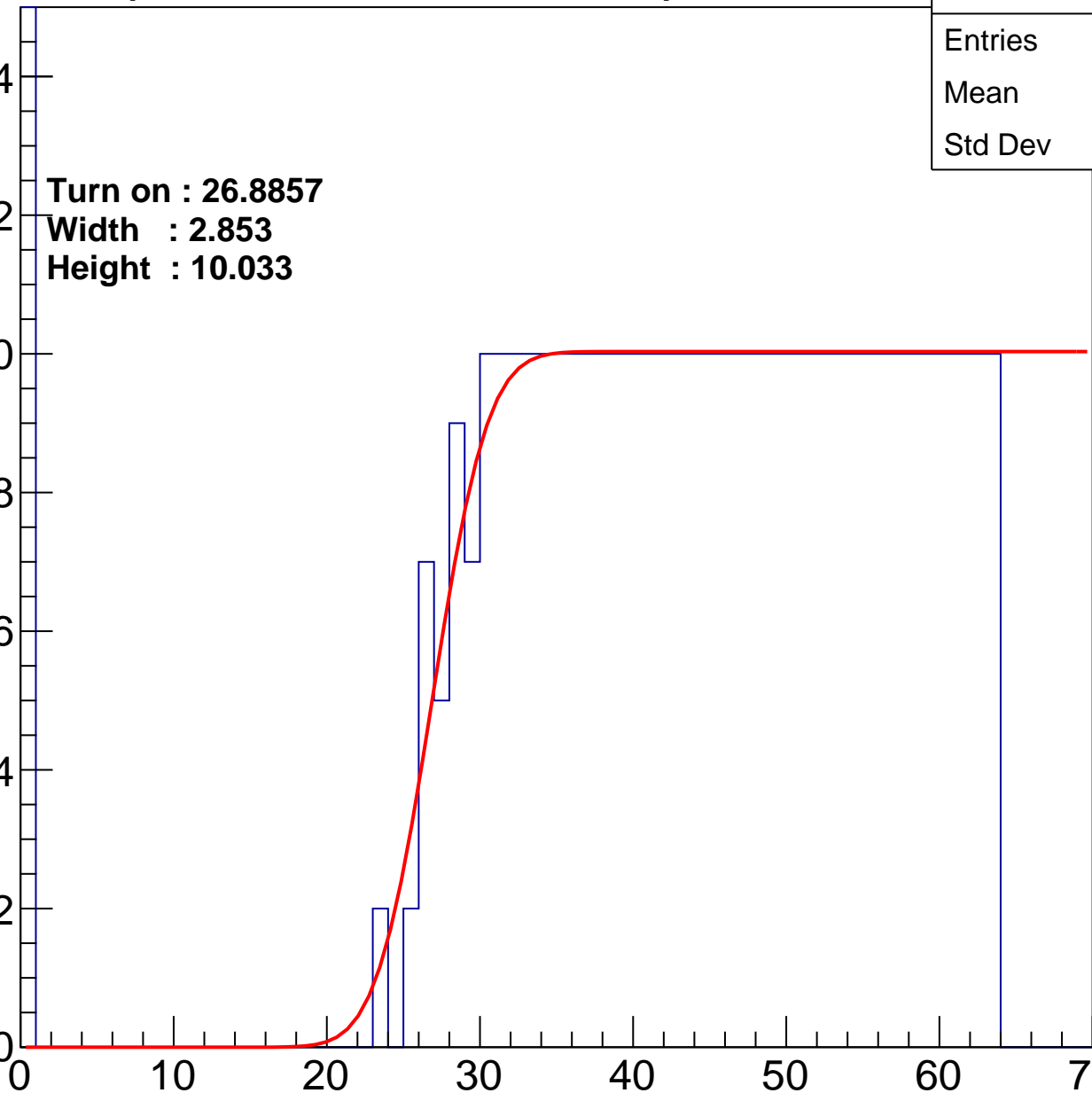
Width : 2.853

Height : 10.033

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch21

calib_packv5_041523_1651.root, FC#0, port C2

Entries	402
Mean	41.09
Std Dev	16.43

Turn on : 27.4648

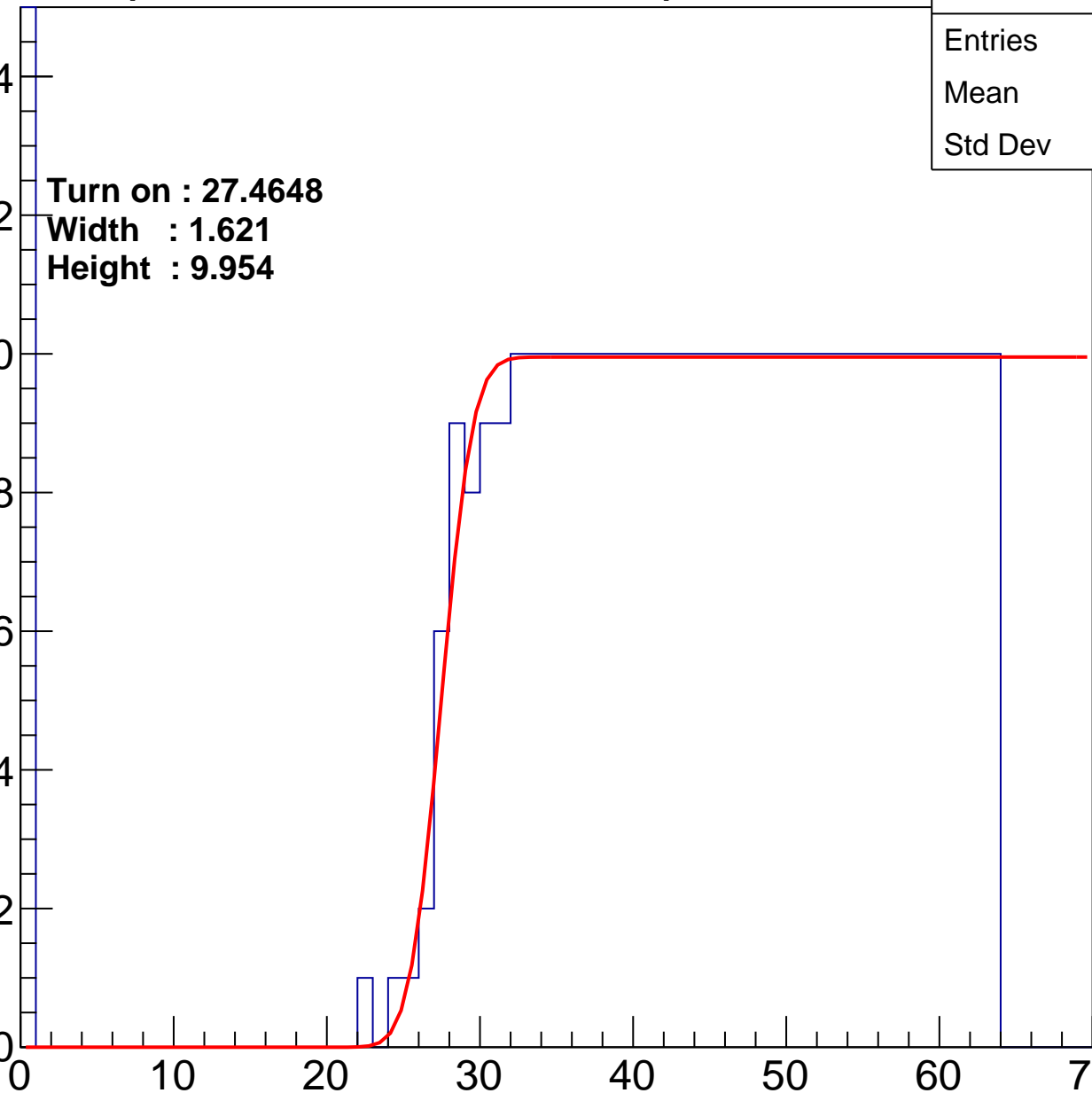
Width : 1.621

Height : 9.954

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch22

calib_packv5_041523_1651.root, FC#0, port C2

Entries	429
Mean	39.69
Std Dev	17.04

Turn on : 25.1637

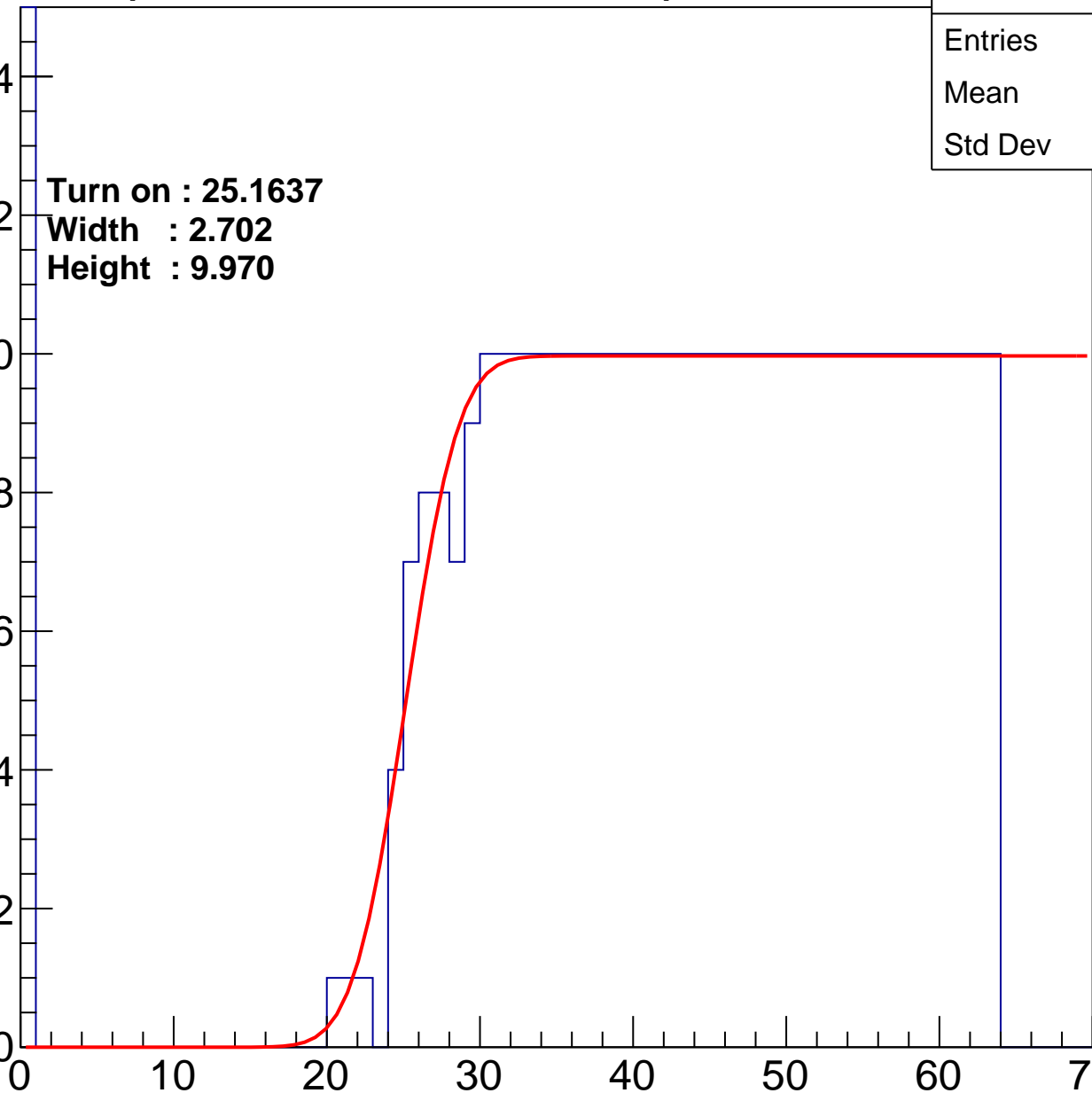
Width : 2.702

Height : 9.970

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch23

calib_packv5_041523_1651.root, FC#0, port C2

Entries	410
Mean	40.69
Std Dev	16.55

Turn on : 27.3569

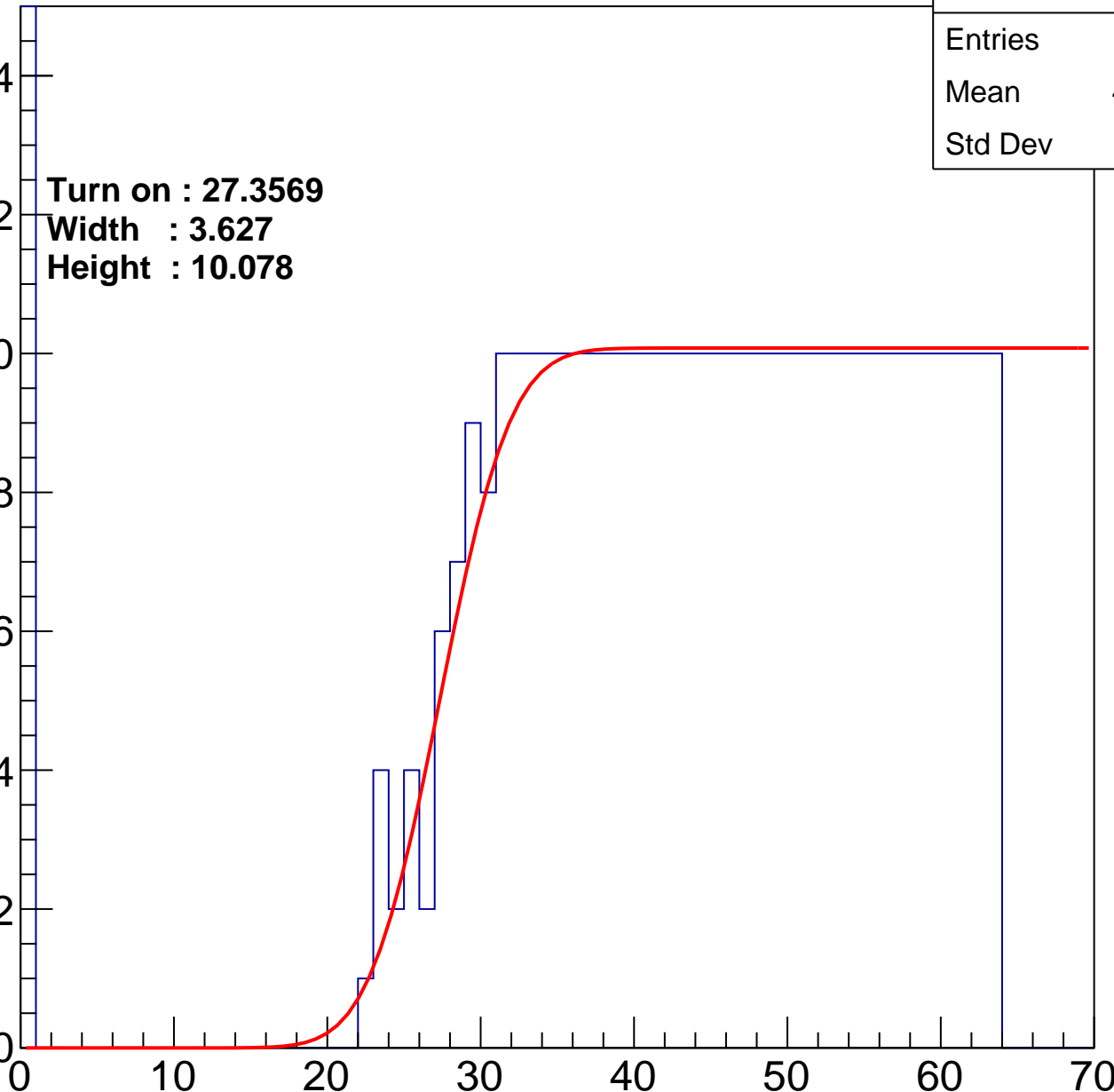
Width : 3.627

Height : 10.078

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch24

calib_packv5_041523_1651.root, FC#0, port C2

Entries	420
Mean	40.46
Std Dev	16.35

Turn on : 25.4014

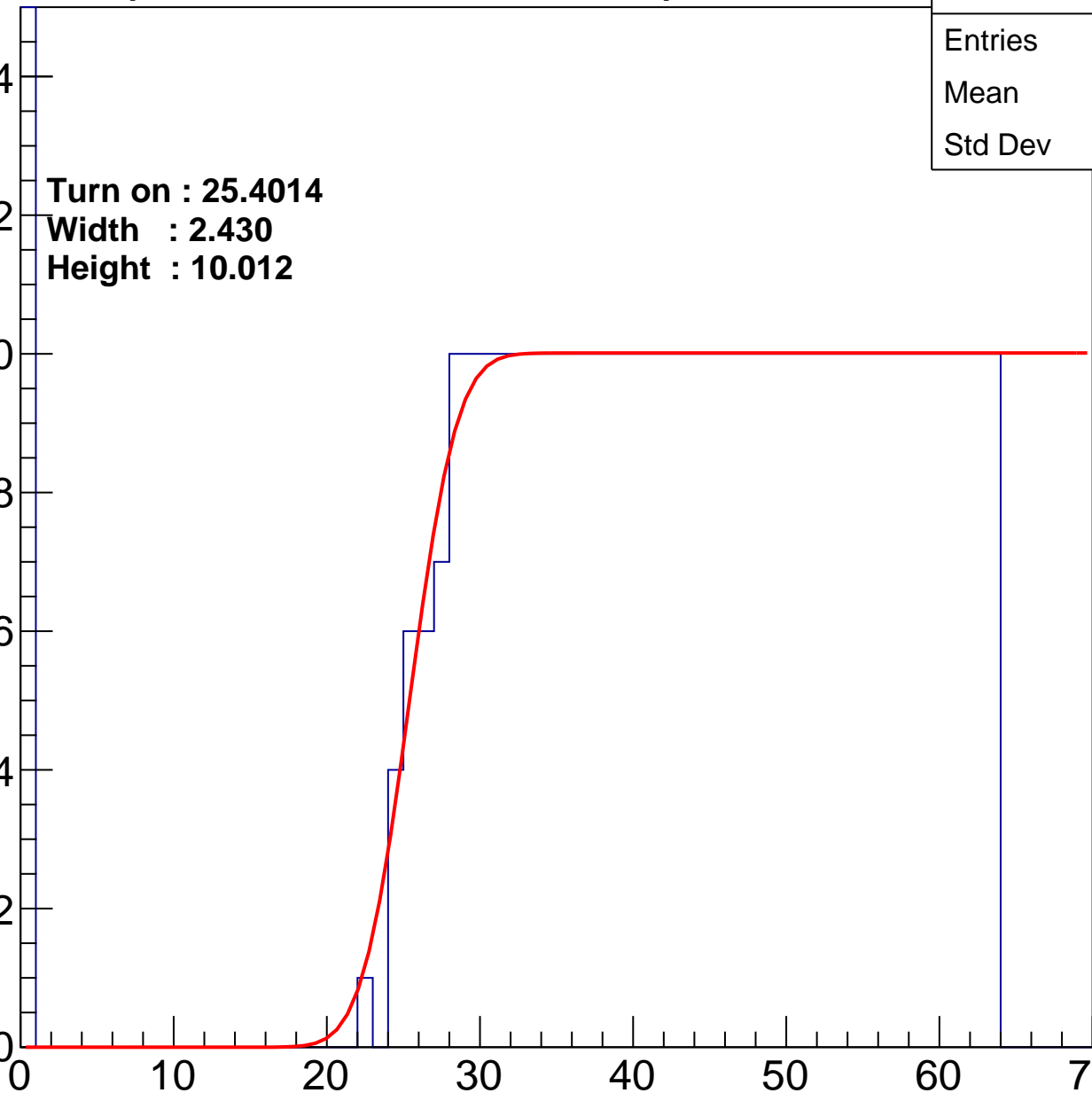
Width : 2.430

Height : 10.012

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch25

calib_packv5_041523_1651.root, FC#0, port C2

Entries	417
Mean	39.92
Std Dev	17.38

Turn on : 26.8910

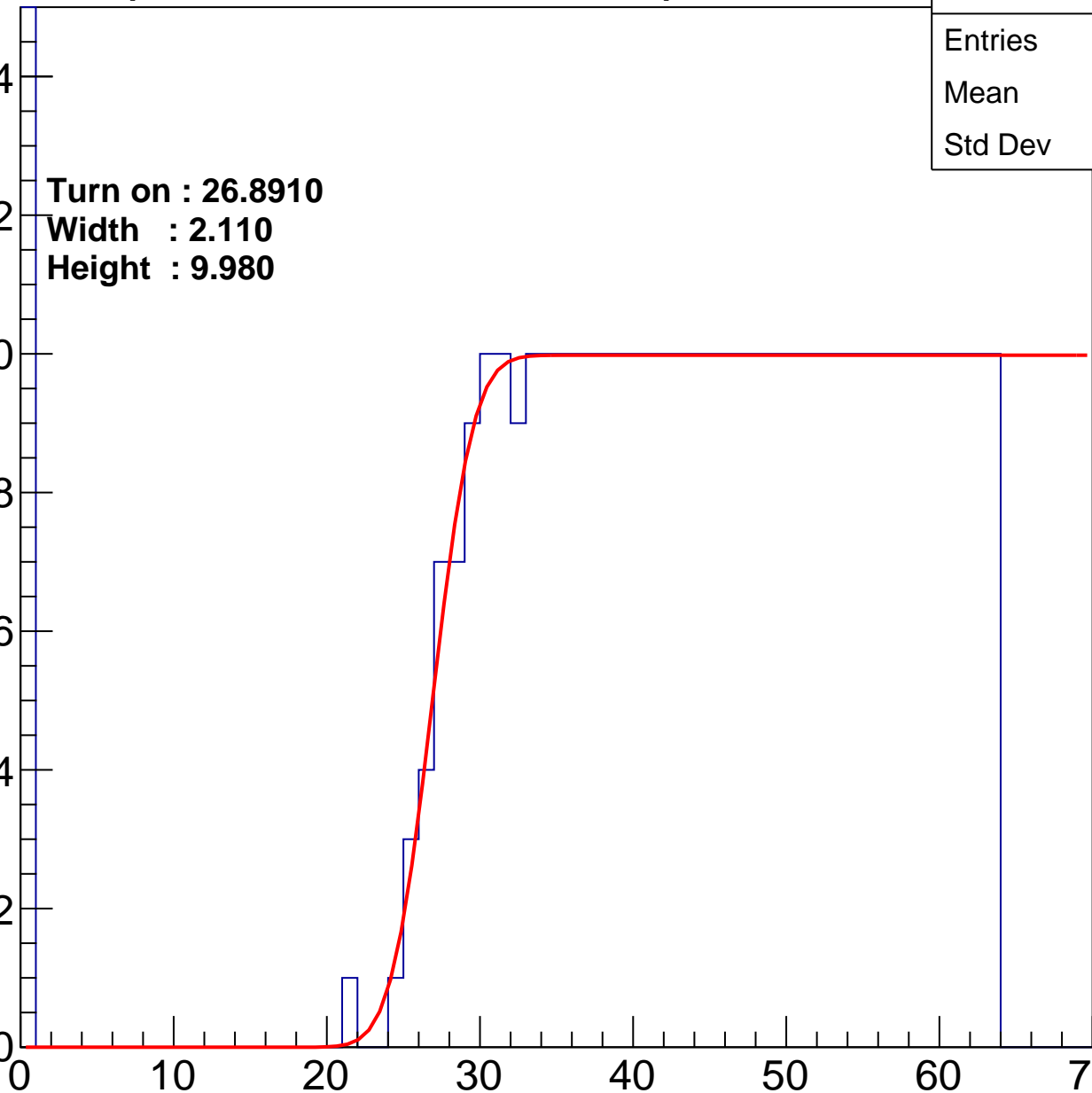
Width : 2.110

Height : 9.980

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch26

calib_packv5_041523_1651.root, FC#0, port C2

Entries	435
Mean	39.47
Std Dev	17.02

Turn on : 25.1756

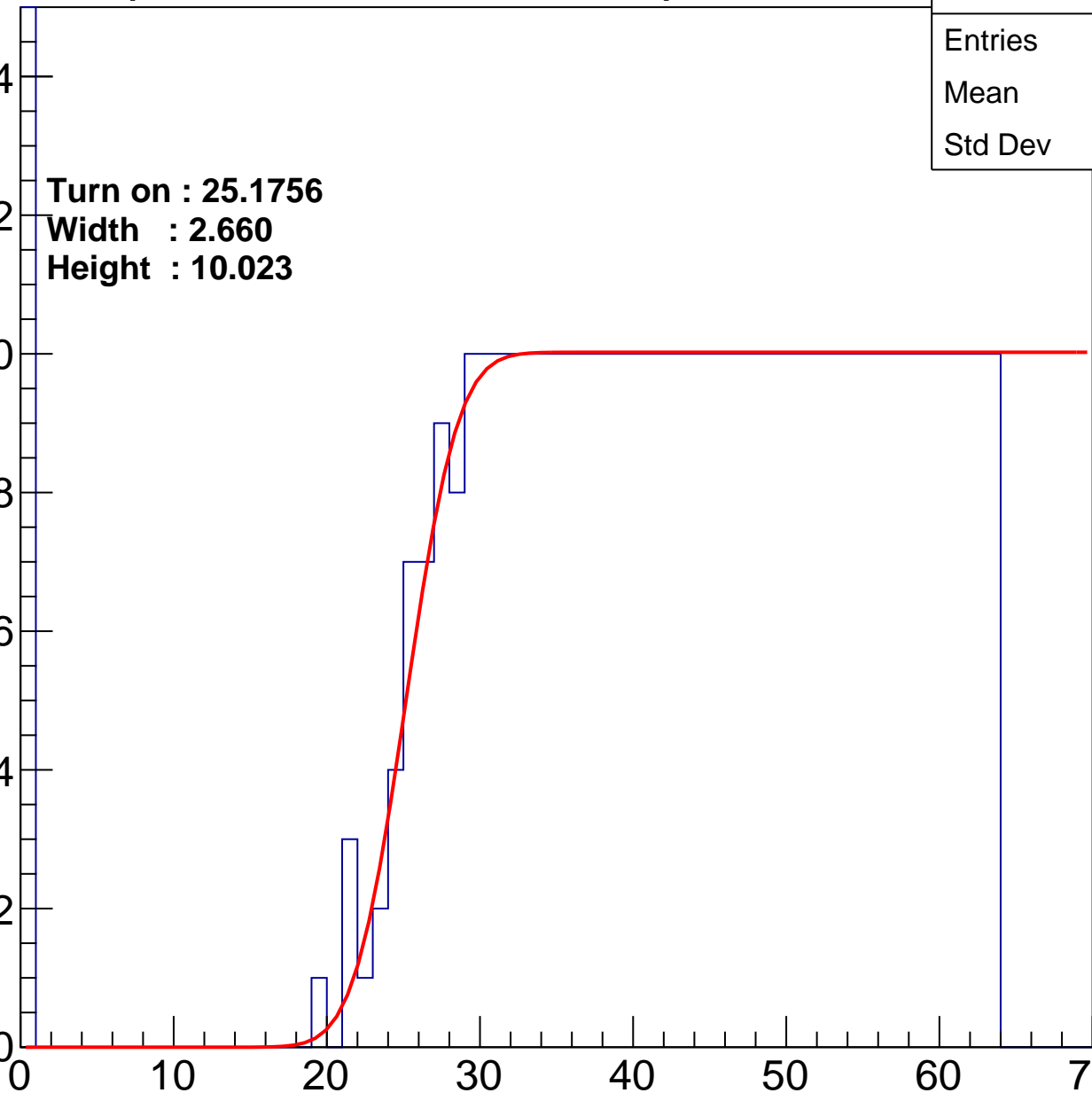
Width : 2.660

Height : 10.023

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch27

calib_packv5_041523_1651.root, FC#0, port C2

Entries	412
Mean	40.27
Std Dev	17.13

Turn on : 26.9079

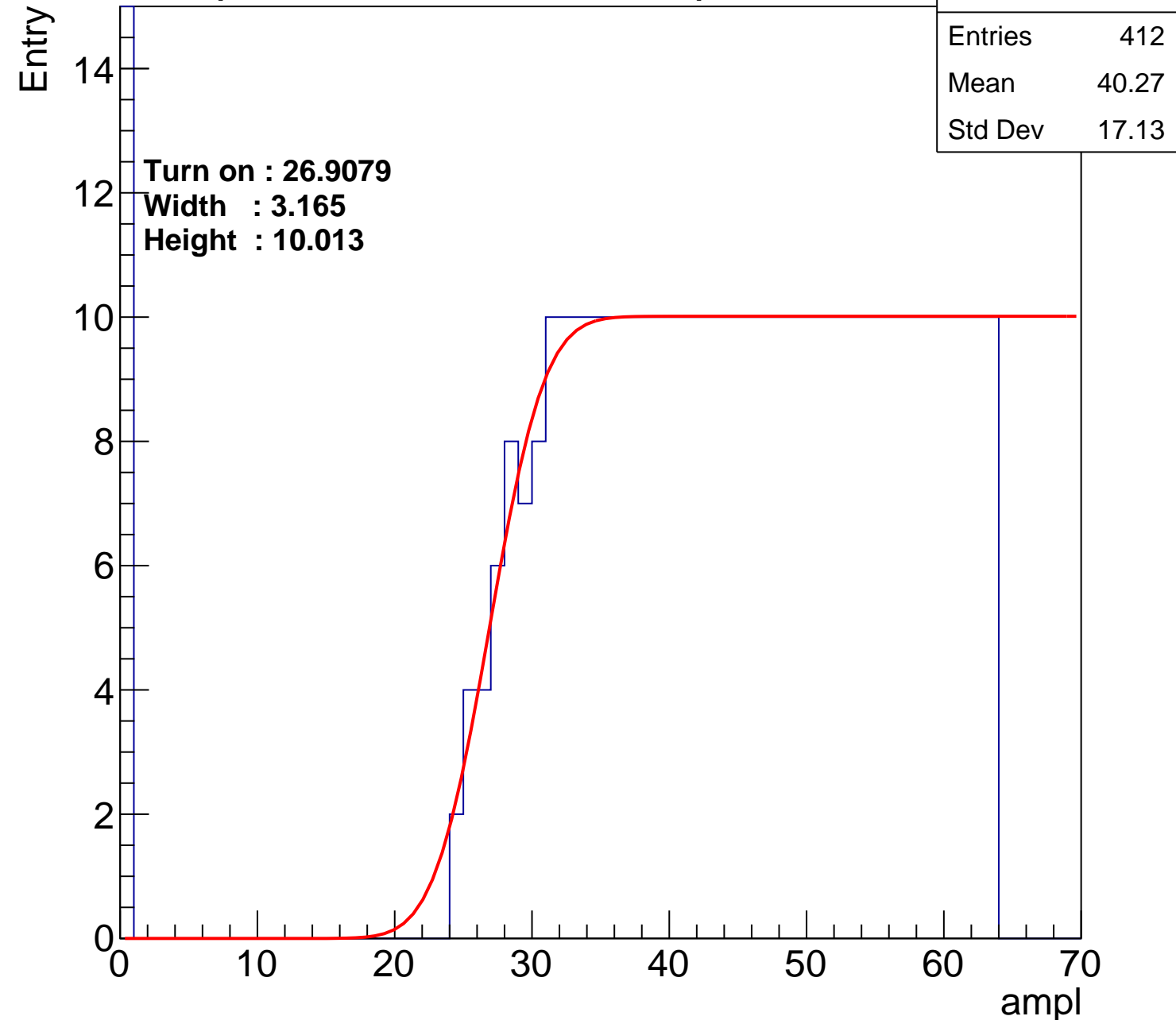
Width : 3.165

Height : 10.013

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch28

calib_packv5_041523_1651.root, FC#0, port C2

Entries	430
Mean	39.67
Std Dev	16.99

Turn on : 25.8456

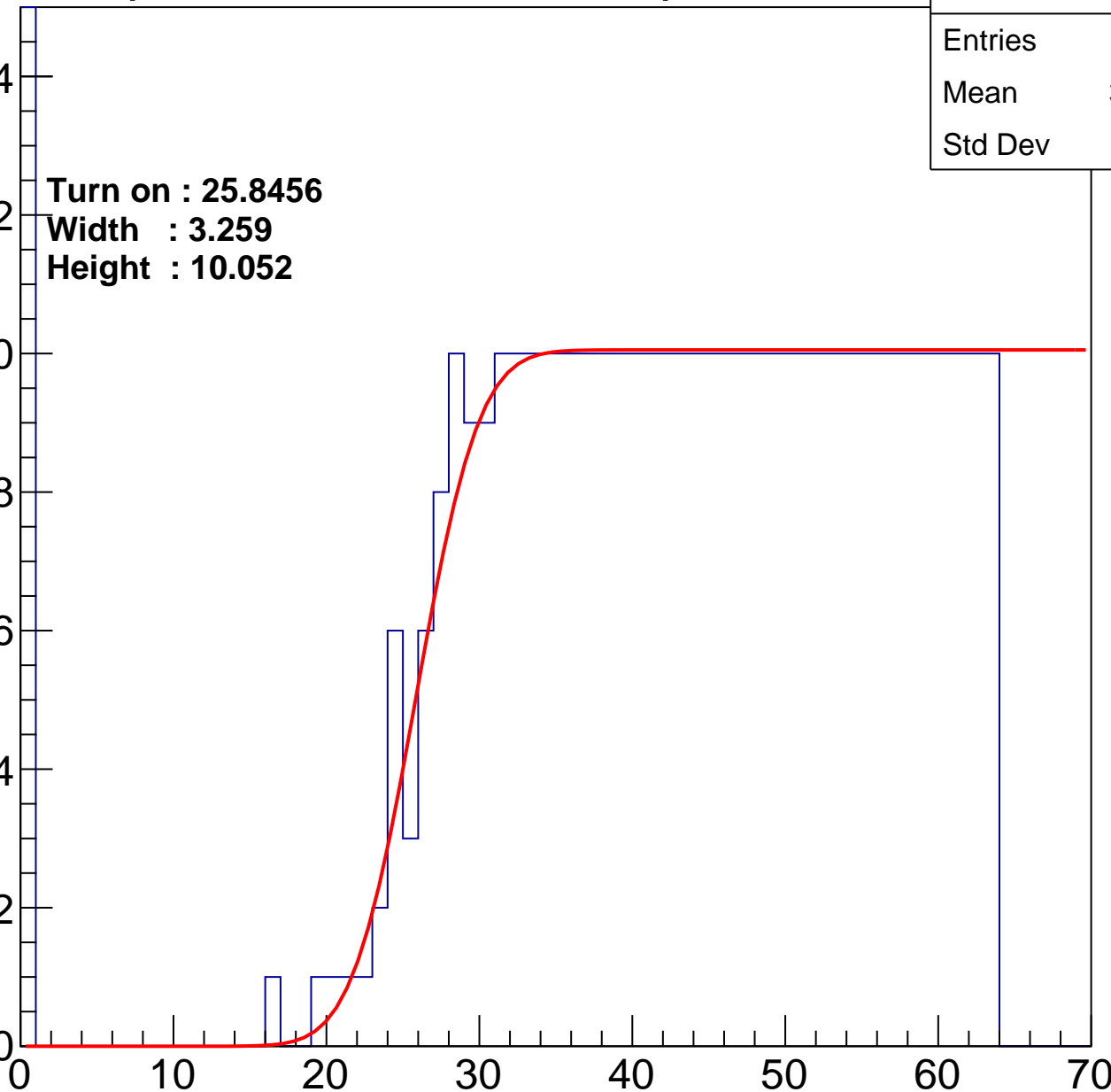
Width : 3.259

Height : 10.052

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch29

calib_packv5_041523_1651.root, FC#0, port C2

Entries	417
Mean	39.83
Std Dev	17.5

Turn on : 27.8266

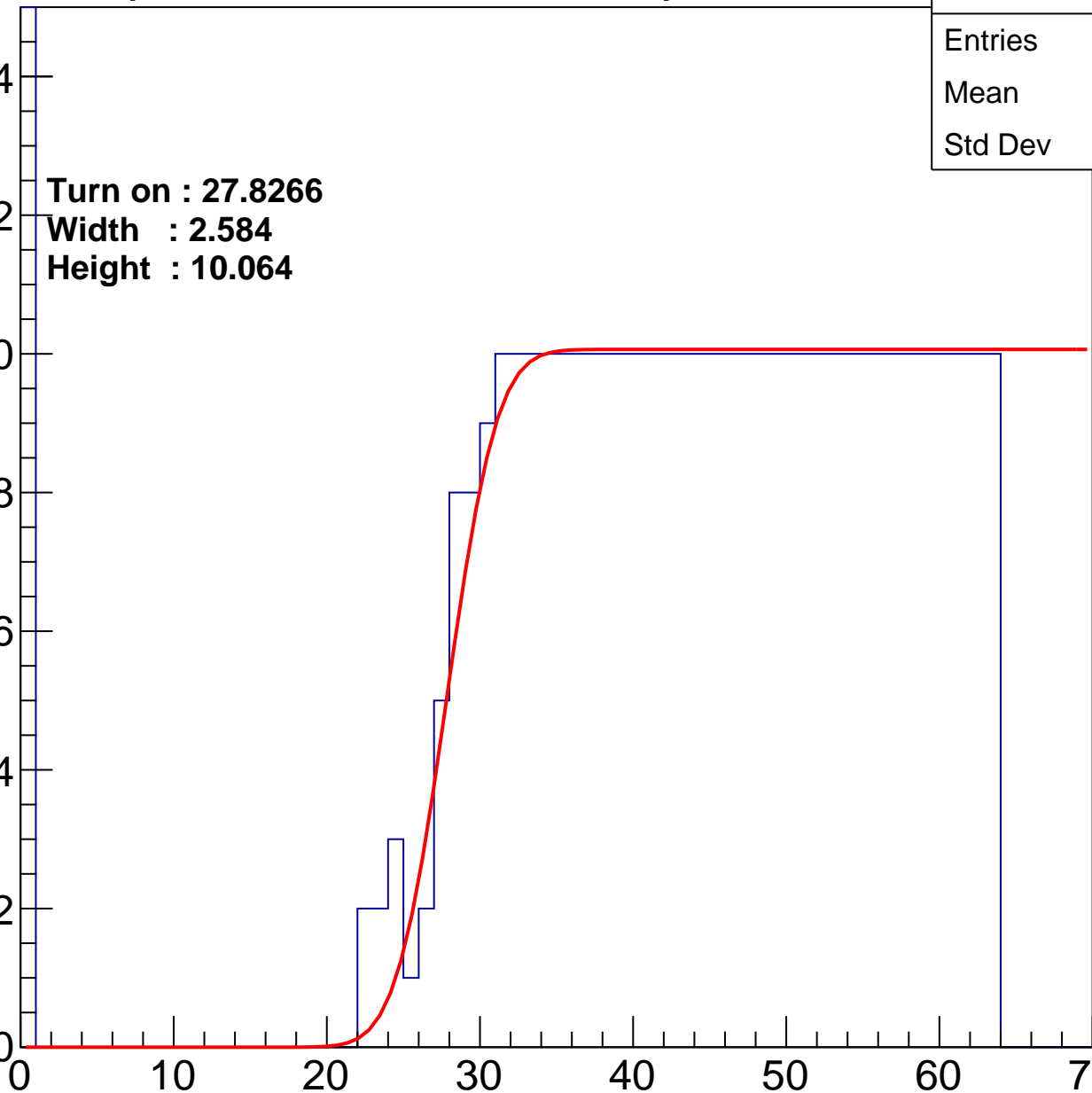
Width : 2.584

Height : 10.064

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch30

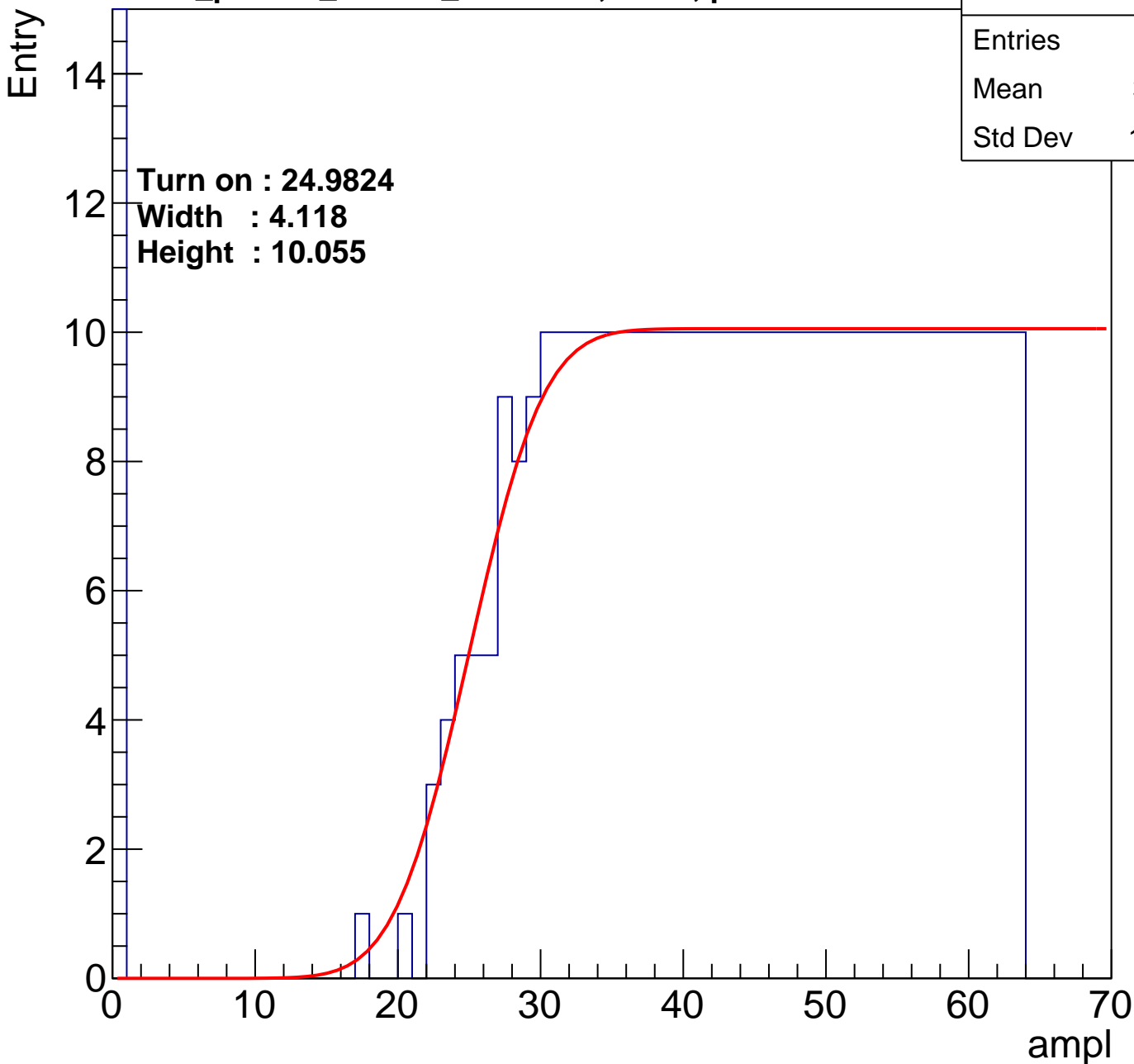
calib_packv5_041523_1651.root, FC#0, port C2

Entries	442
Mean	38.71
Std Dev	17.78

Turn on : 24.9824

Width : 4.118

Height : 10.055



B1L103S, U9-ch31

calib_packv5_041523_1651.root, FC#0, port C2

Entries	415
Mean	40.01
Std Dev	17.33

Turn on : 26.9495

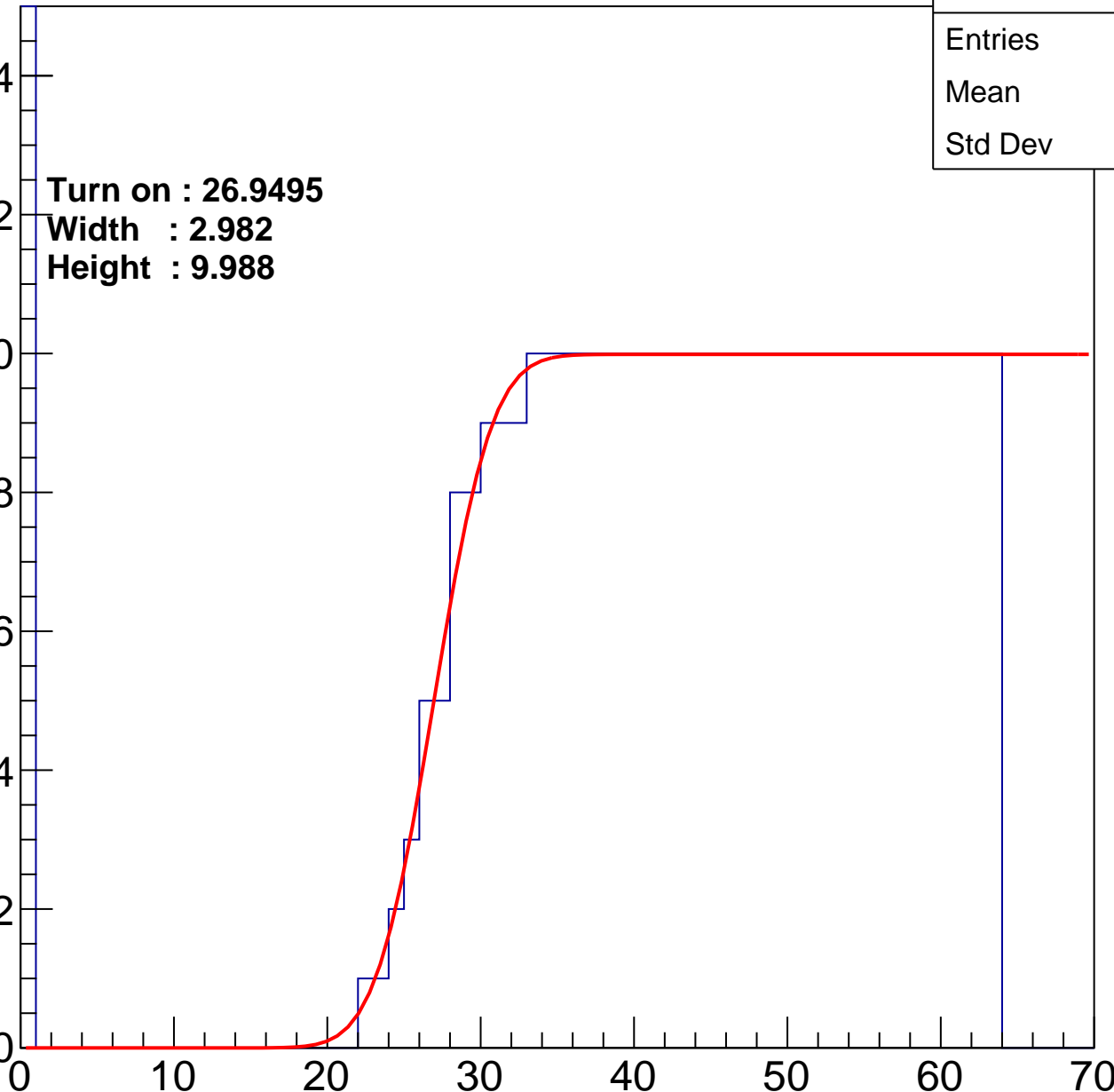
Width : 2.982

Height : 9.988

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch32

calib_packv5_041523_1651.root, FC#0, port C2

Entries	426
Mean	40.02
Std Dev	16.68

Turn on : 25.4356

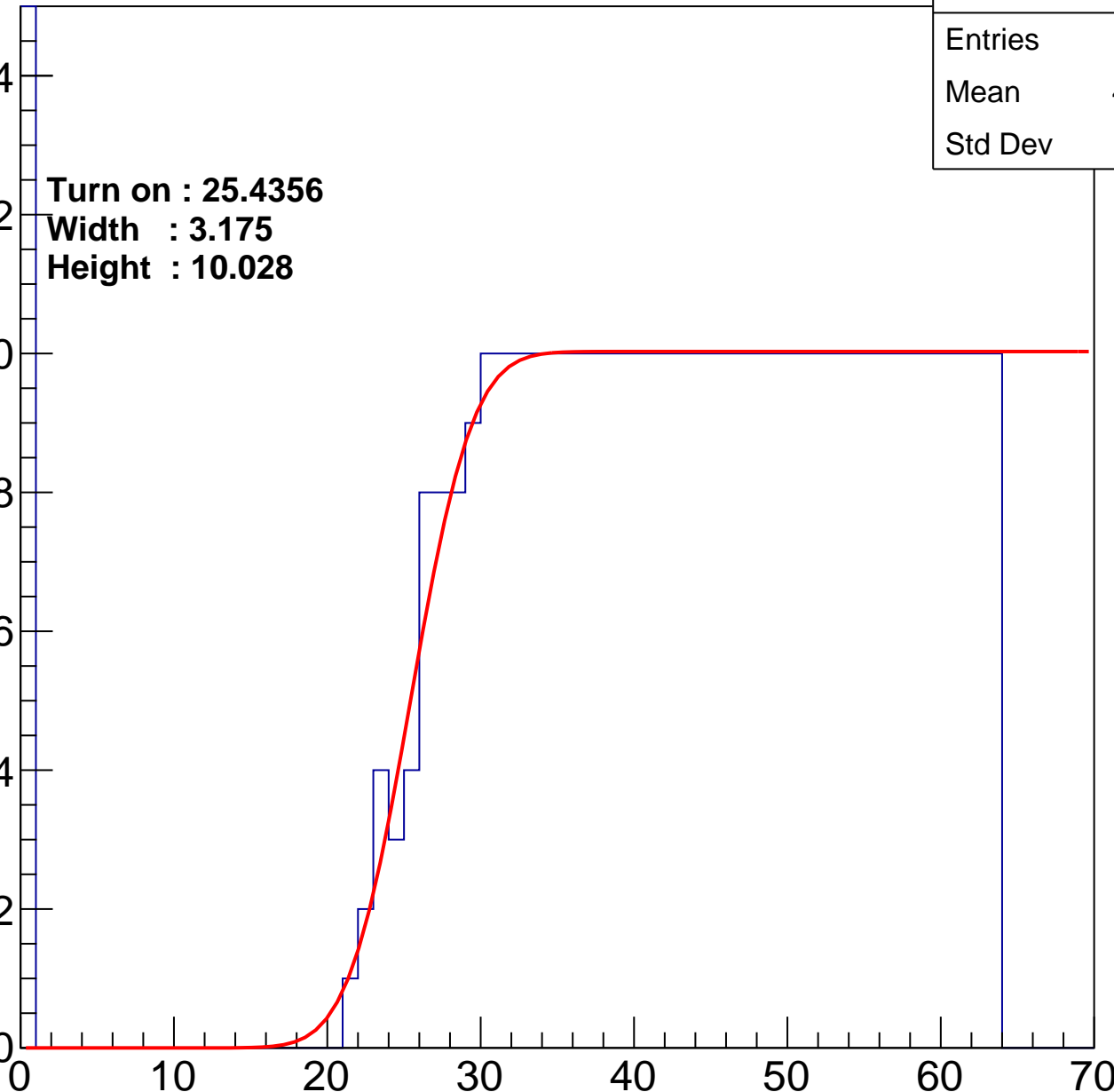
Width : 3.175

Height : 10.028

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch33

calib_packv5_041523_1651.root, FC#0, port C2

Entries	416
Mean	40.72
Std Dev	16.16

Turn on : 25.8890

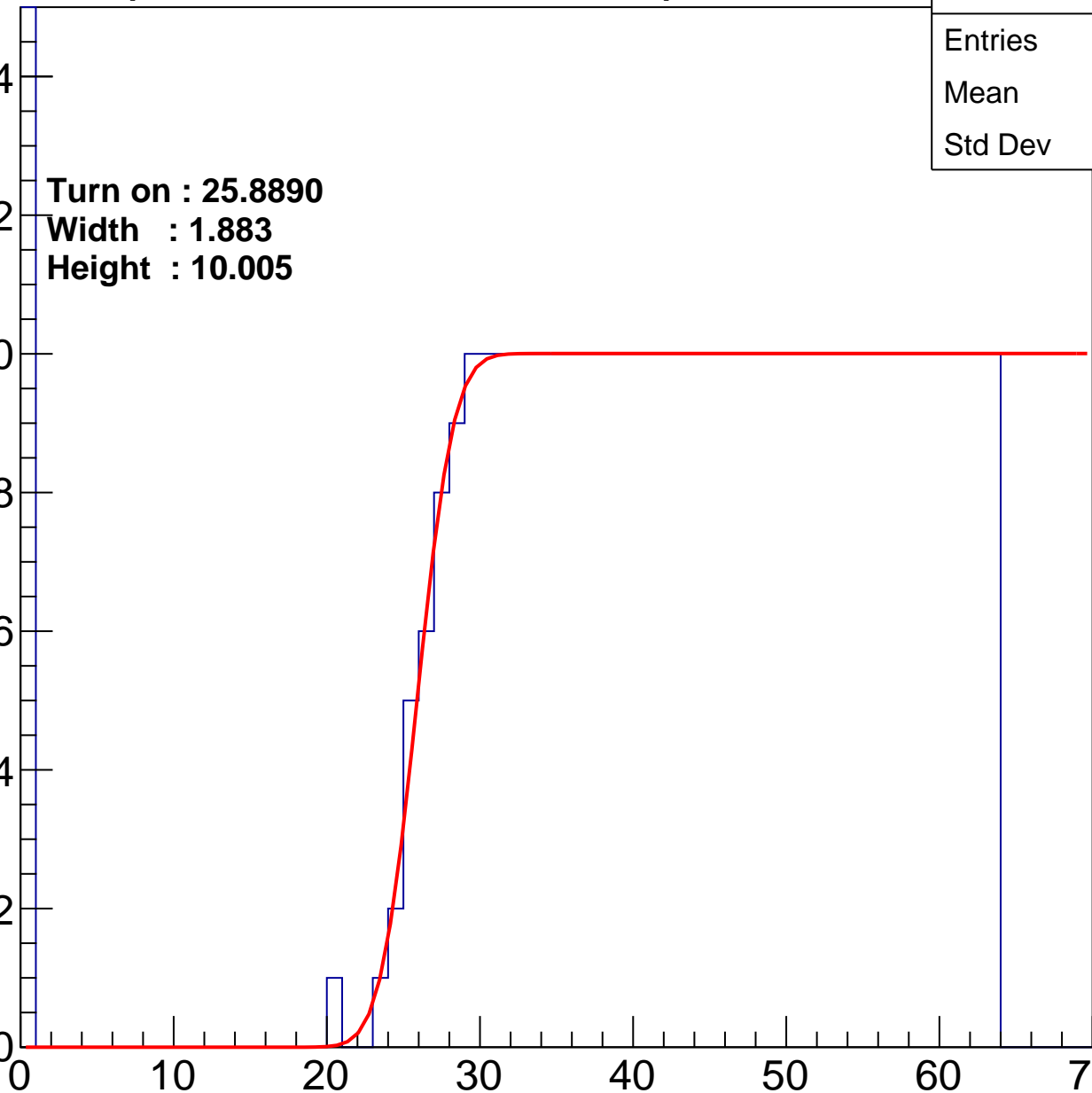
Width : 1.883

Height : 10.005

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch34

calib_packv5_041523_1651.root, FC#0, port C2

Entries	428
Mean	39.74
Std Dev	17.03

Turn on : 25.4229

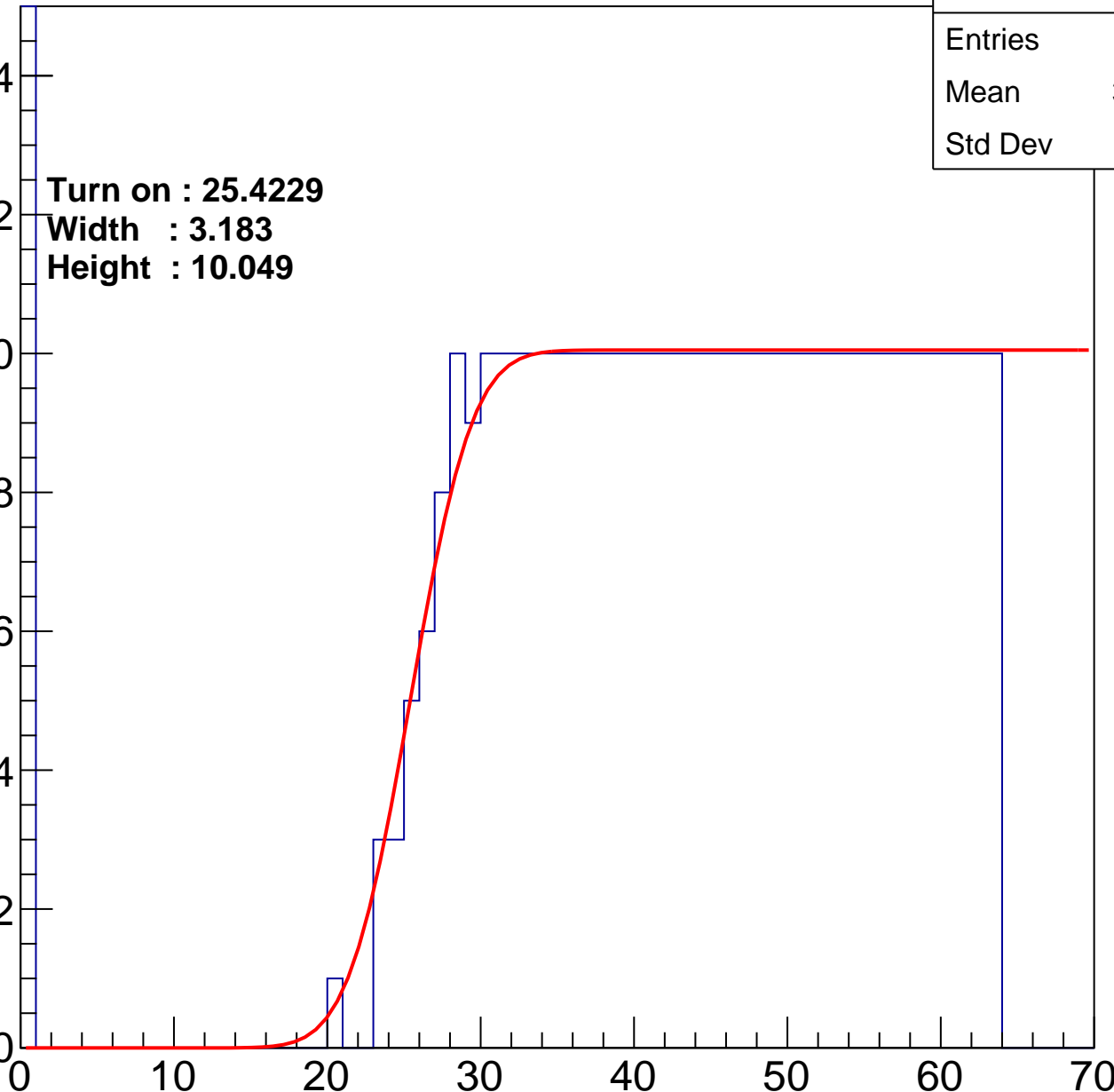
Width : 3.183

Height : 10.049

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch35

calib_packv5_041523_1651.root, FC#0, port C2

Entries	425
Mean	39.77
Std Dev	17.15

Turn on : 26.1904

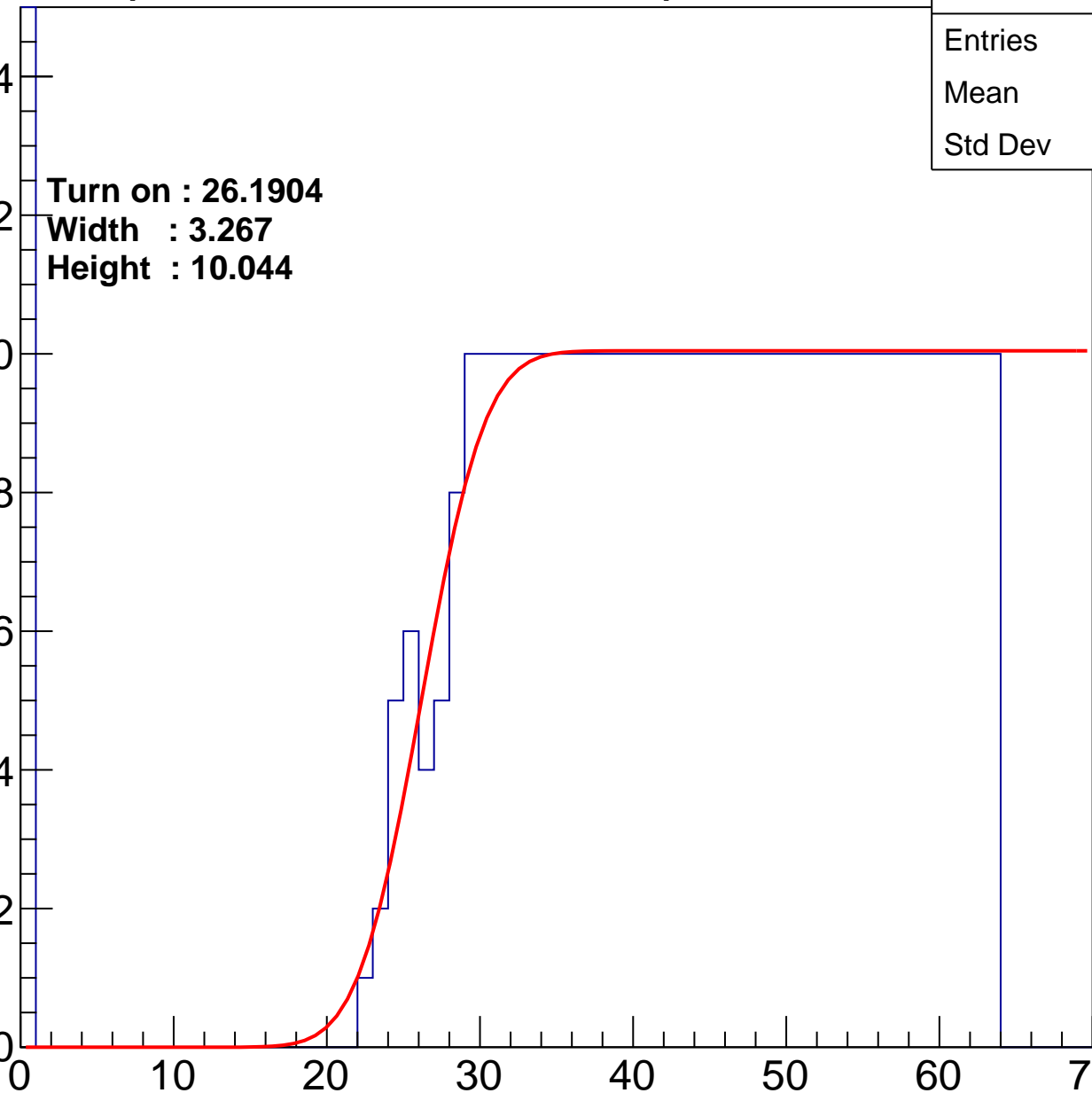
Width : 3.267

Height : 10.044

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch36

calib_packv5_041523_1651.root, FC#0, port C2

Entries	437
Mean	38.79
Std Dev	17.95

Turn on : 25.8169

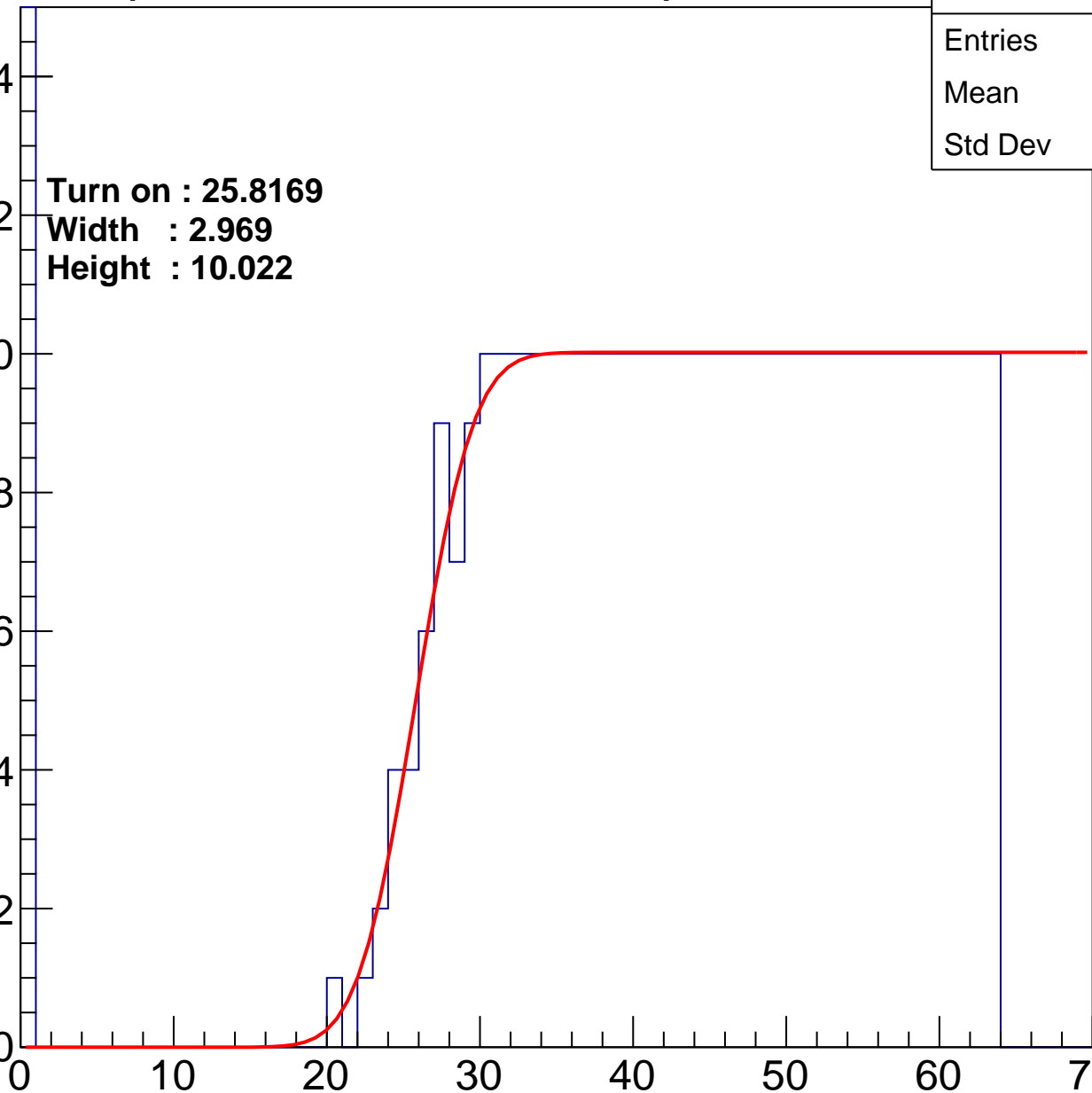
Width : 2.969

Height : 10.022

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch37

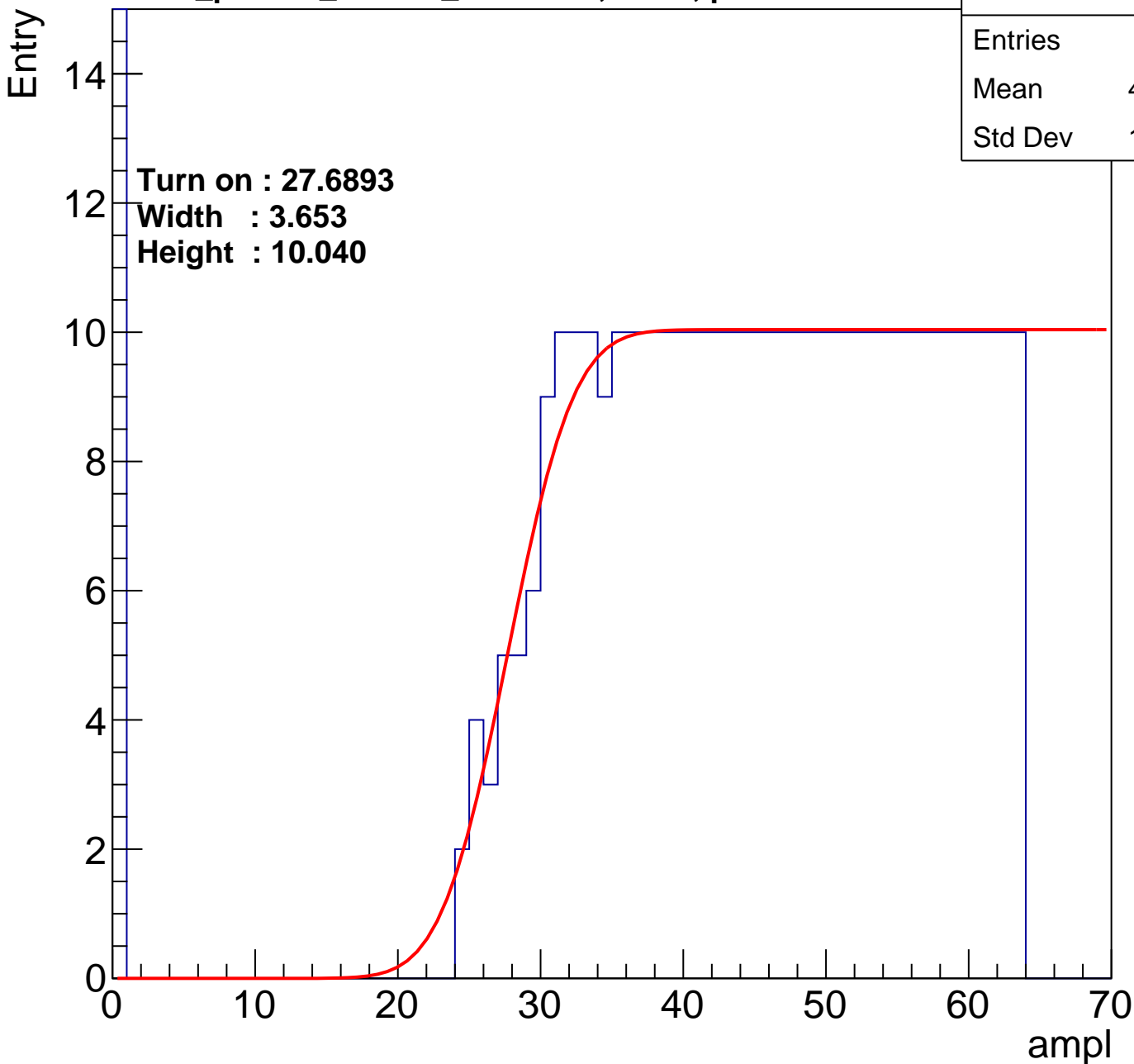
calib_packv5_041523_1651.root, FC#0, port C2

Entries	399
Mean	41.16
Std Dev	16.48

Turn on : 27.6893

Width : 3.653

Height : 10.040



B1L103S, U9-ch38

calib_packv5_041523_1651.root, FC#0, port C2

Entries	433
Mean	38.96
Std Dev	17.91

Turn on : 25.5879

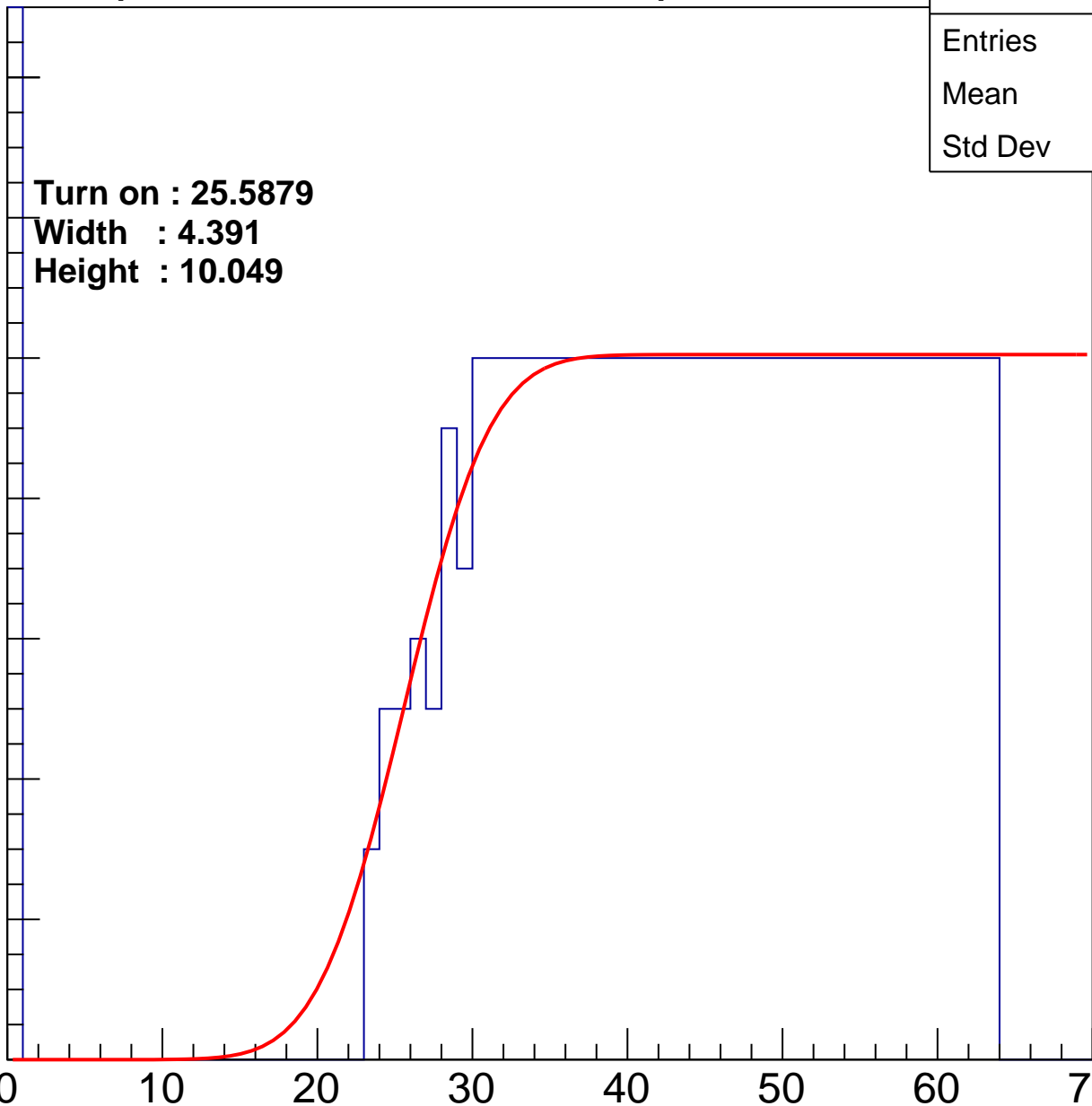
Width : 4.391

Height : 10.049

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch39

calib_packv5_041523_1651.root, FC#0, port C2

Entries	407
Mean	40.38
Std Dev	17.2

Turn on : 27.2648

Width : 3.917

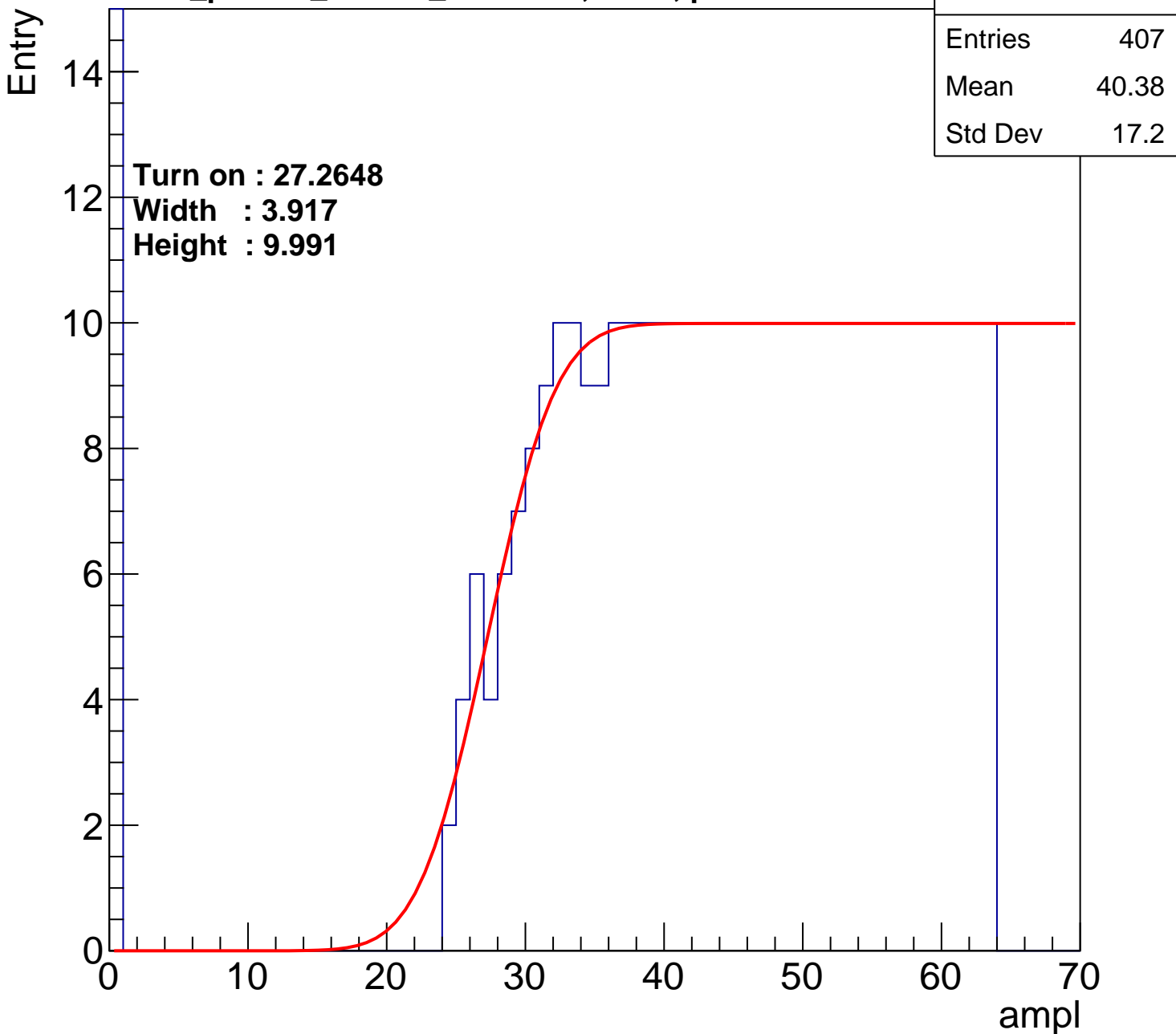
Height : 9.991

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L103S, U9-ch40

calib_packv5_041523_1651.root, FC#0, port C2

Entries	431
Mean	39.61
Std Dev	17.27

Turn on : 25.6521

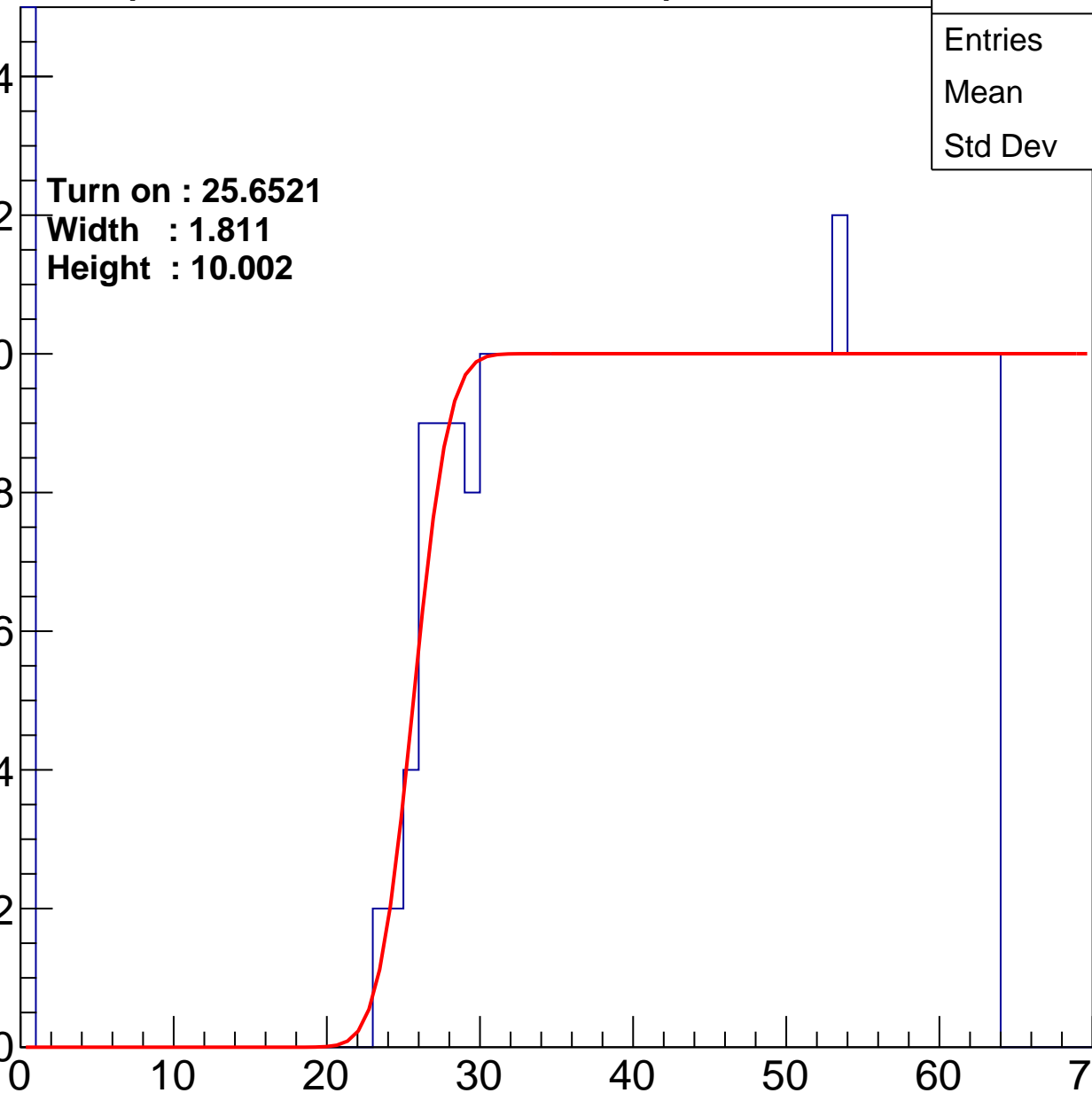
Width : 1.811

Height : 10.002

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch41

calib_packv5_041523_1651.root, FC#0, port C2

Entries	414
Mean	39.83
Std Dev	17.65

Turn on : 28.0229

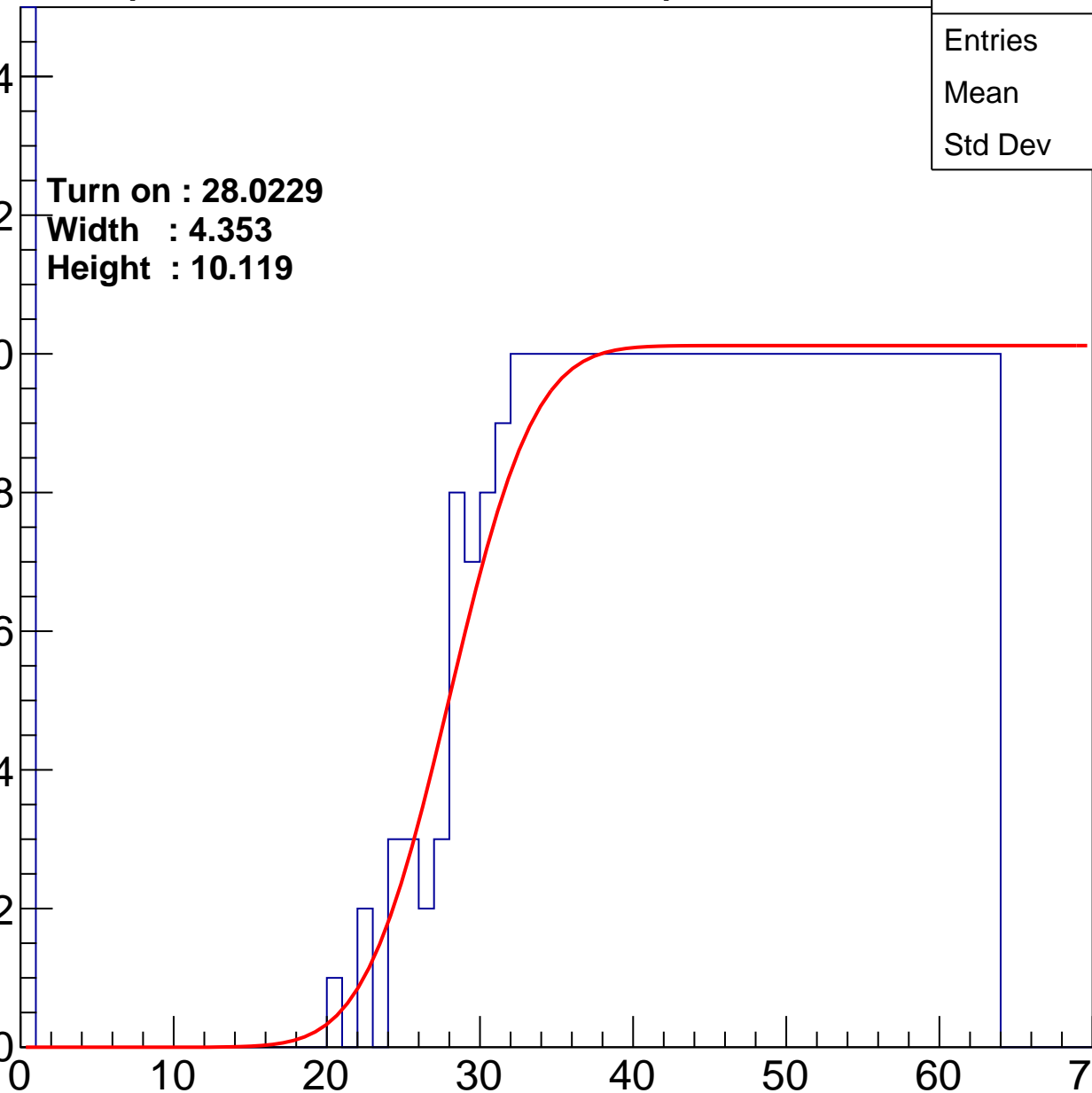
Width : 4.353

Height : 10.119

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch42

calib_packv5_041523_1651.root, FC#0, port C2

Entries	437
Mean	38.88
Std Dev	17.84

Turn on : 26.0545

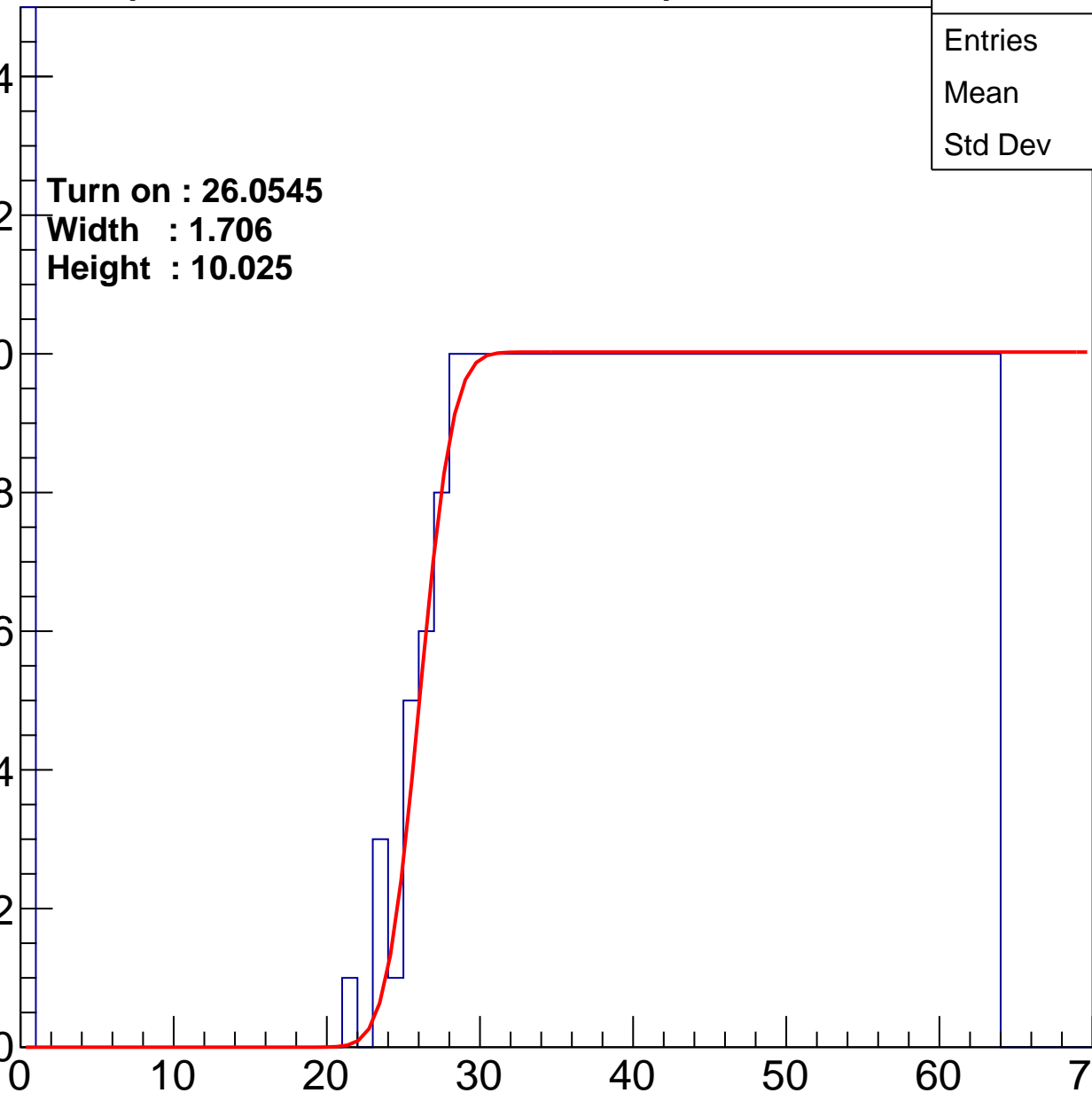
Width : 1.706

Height : 10.025

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch43

calib_packv5_041523_1651.root, FC#0, port C2

Entries	404
Mean	41.2
Std Dev	16.1

Turn on : 27.4334

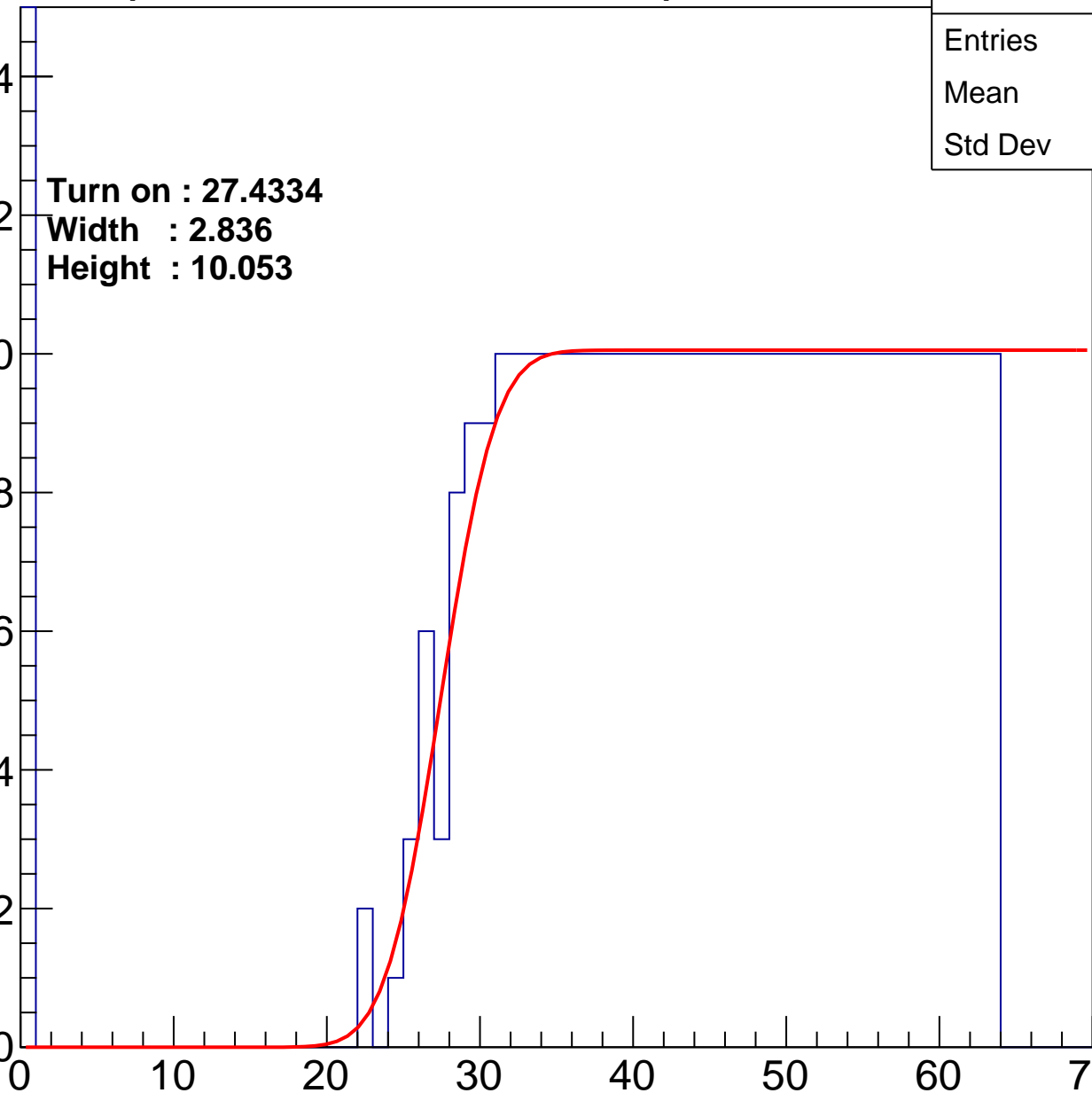
Width : 2.836

Height : 10.053

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch44

calib_packv5_041523_1651.root, FC#0, port C2

Entries	387
Mean	41.95
Std Dev	15.92

Turn on : 28.5675

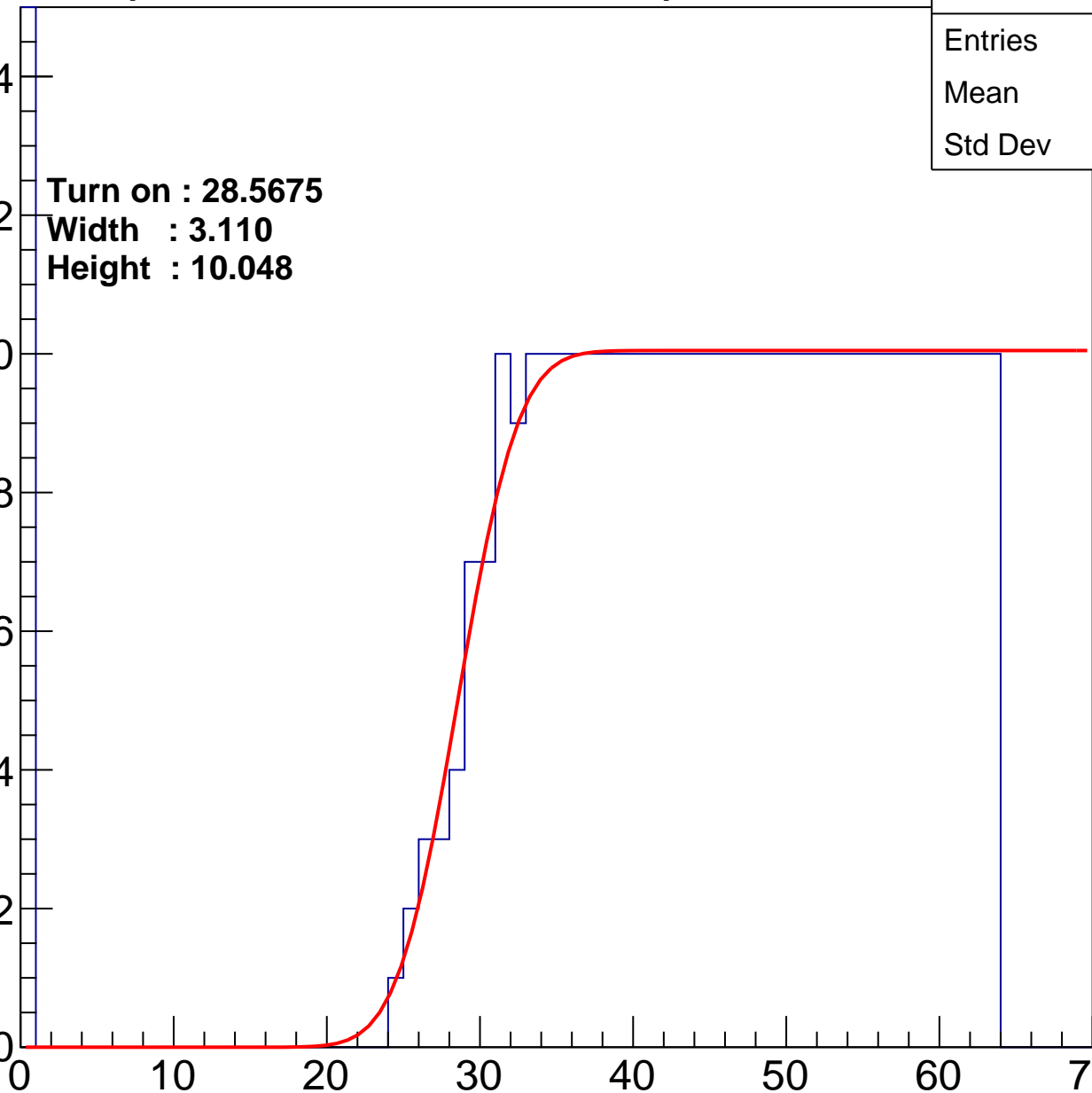
Width : 3.110

Height : 10.048

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch45

calib_packv5_041523_1651.root, FC#0, port C2

Entries	412
Mean	40.03
Std Dev	17.47

Turn on : 27.7105

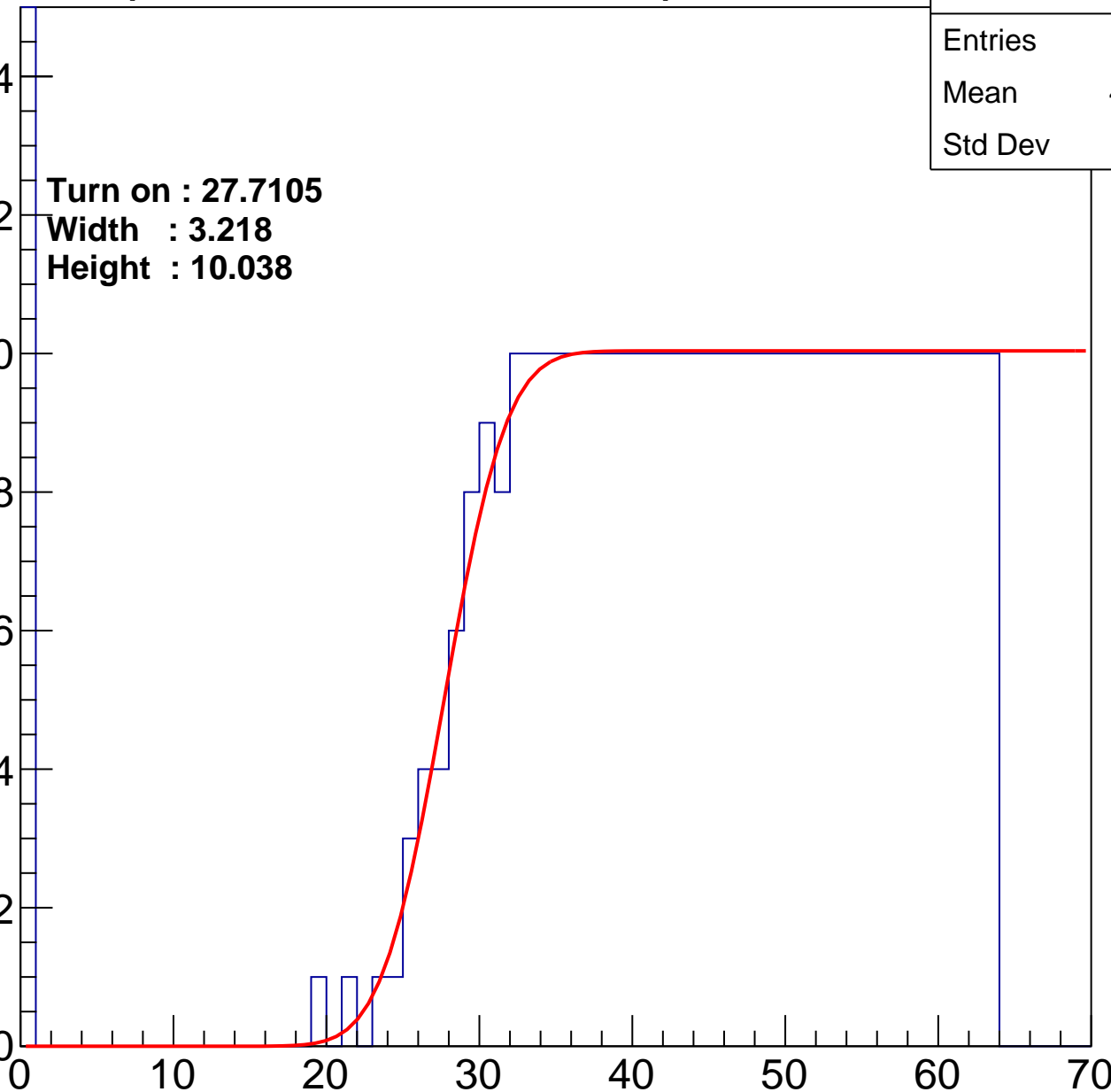
Width : 3.218

Height : 10.038

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch46

calib_packv5_041523_1651.root, FC#0, port C2

Entries	429
Mean	40
Std Dev	16.5

Turn on : 25.1024

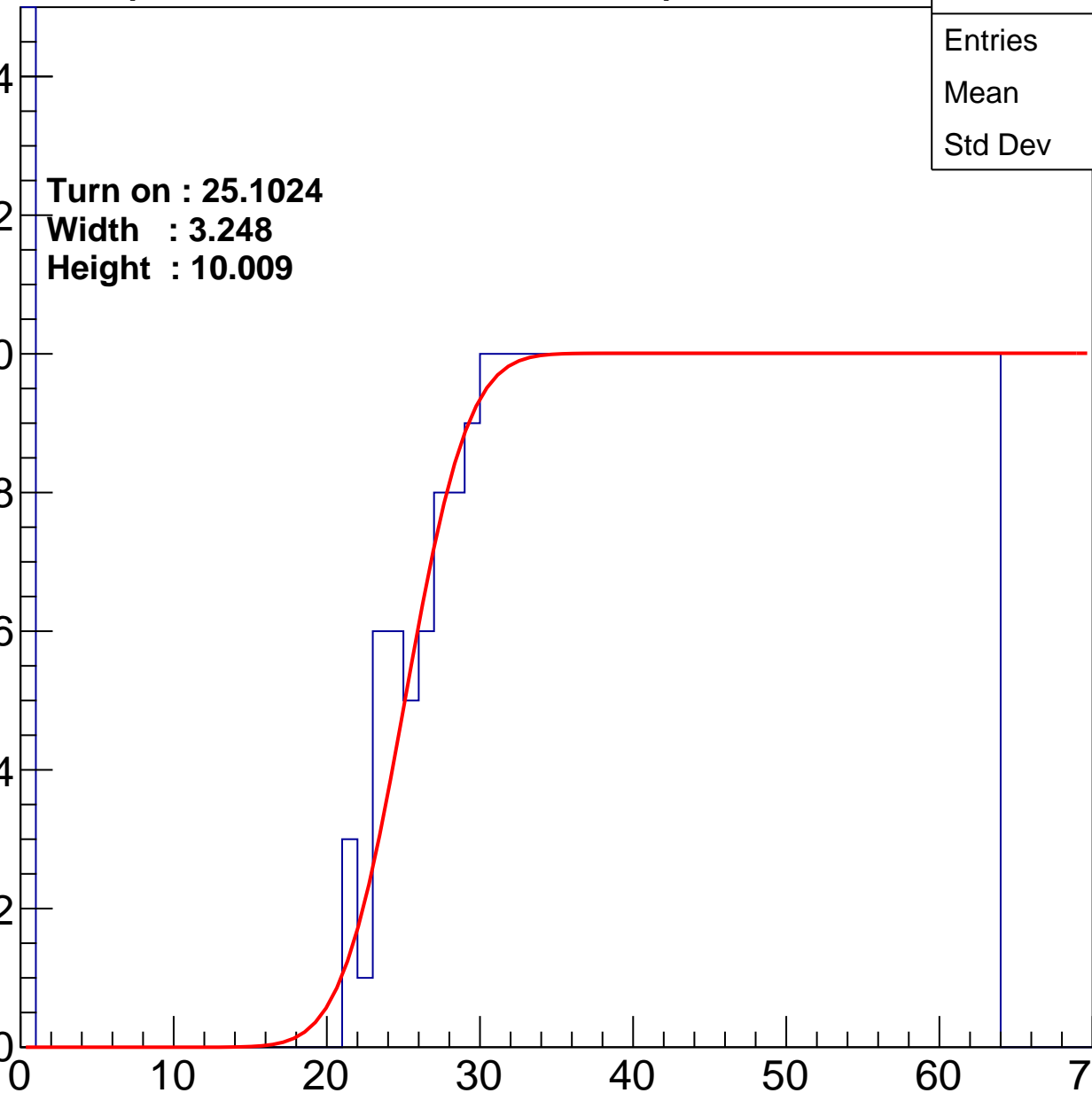
Width : 3.248

Height : 10.009

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch47

calib_packv5_041523_1651.root, FC#0, port C2

Entries	419
Mean	40.14
Std Dev	16.91

Turn on : 26.2932

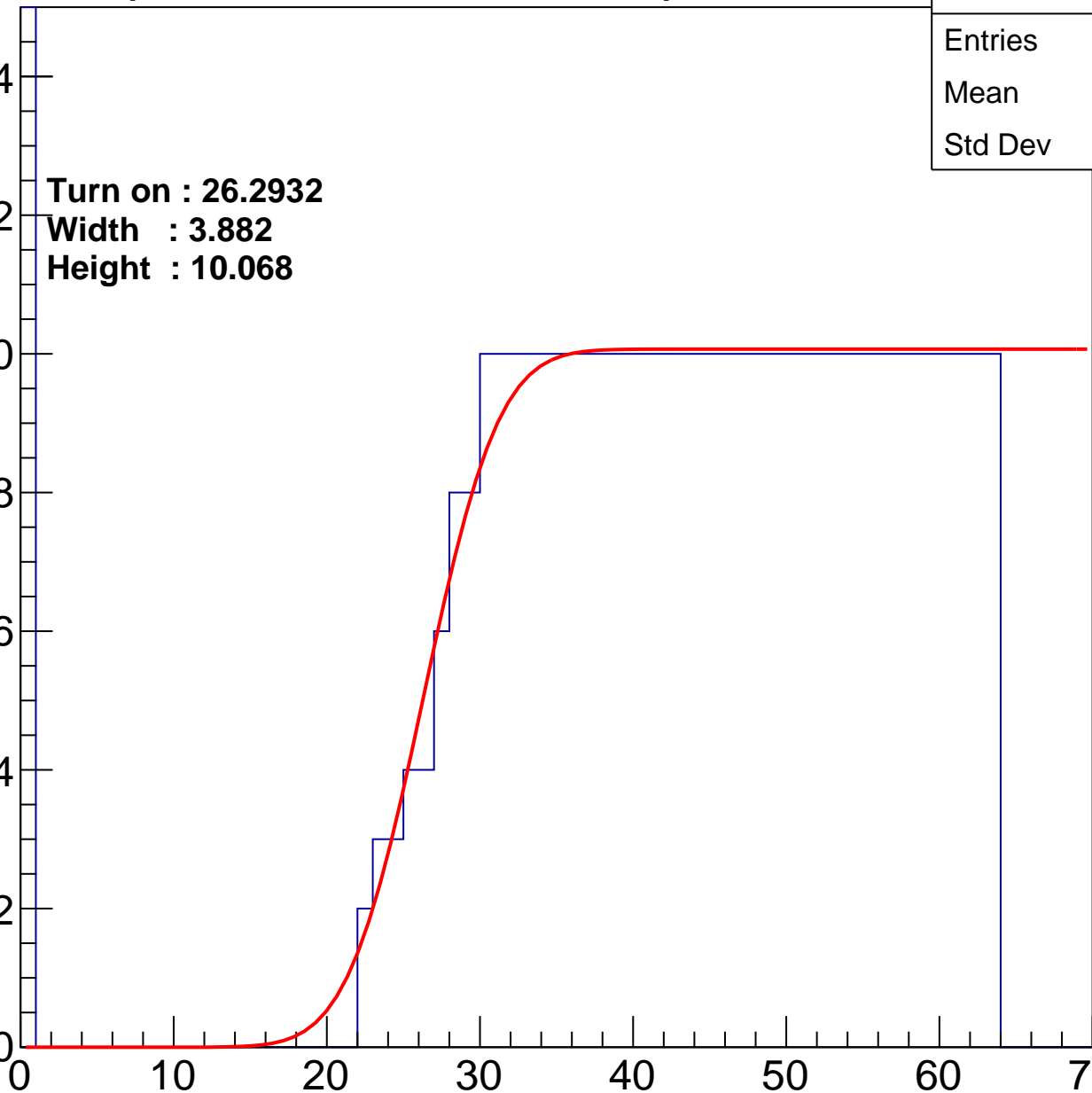
Width : 3.882

Height : 10.068

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch48

calib_packv5_041523_1651.root, FC#0, port C2

Entries	432
Mean	39.64
Std Dev	16.93

Turn on : 25.1431

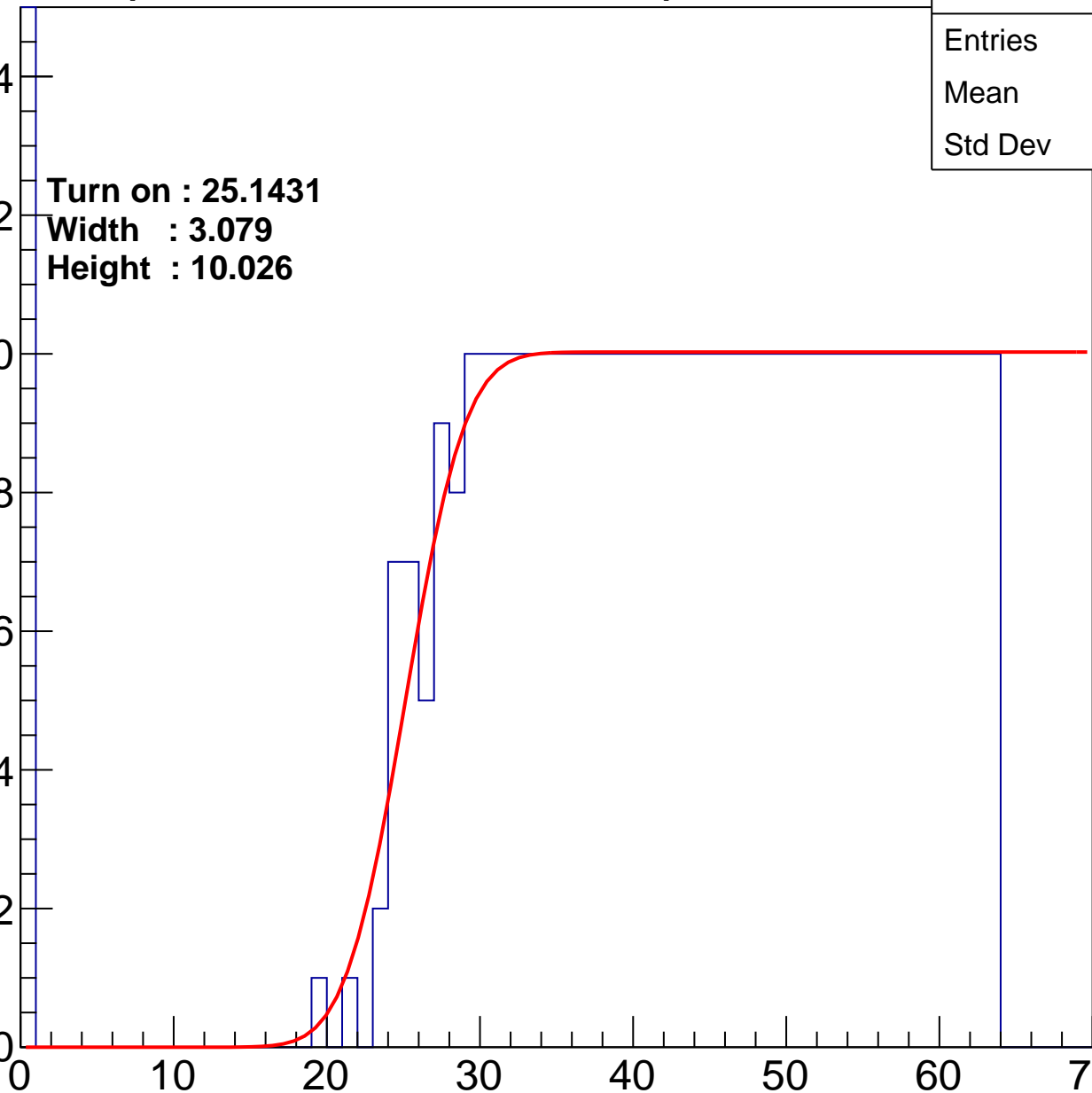
Width : 3.079

Height : 10.026

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch49

calib_packv5_041523_1651.root, FC#0, port C2

Entries	405
Mean	40.98
Std Dev	16.42

Turn on : 27.6490

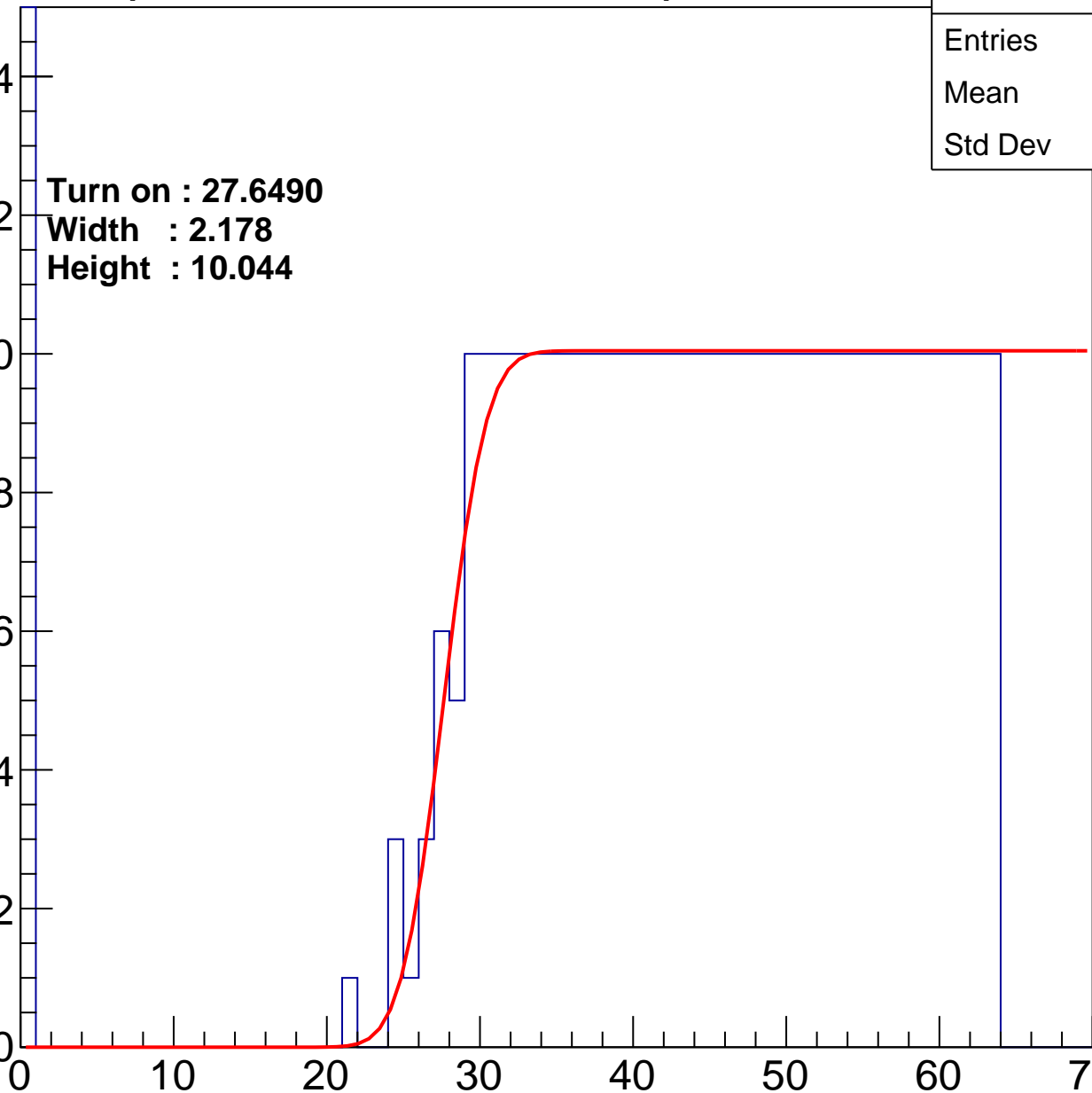
Width : 2.178

Height : 10.044

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch50

calib_packv5_041523_1651.root, FC#0, port C2

Entries	422
Mean	40.4
Std Dev	16.29

Turn on : 25.3357

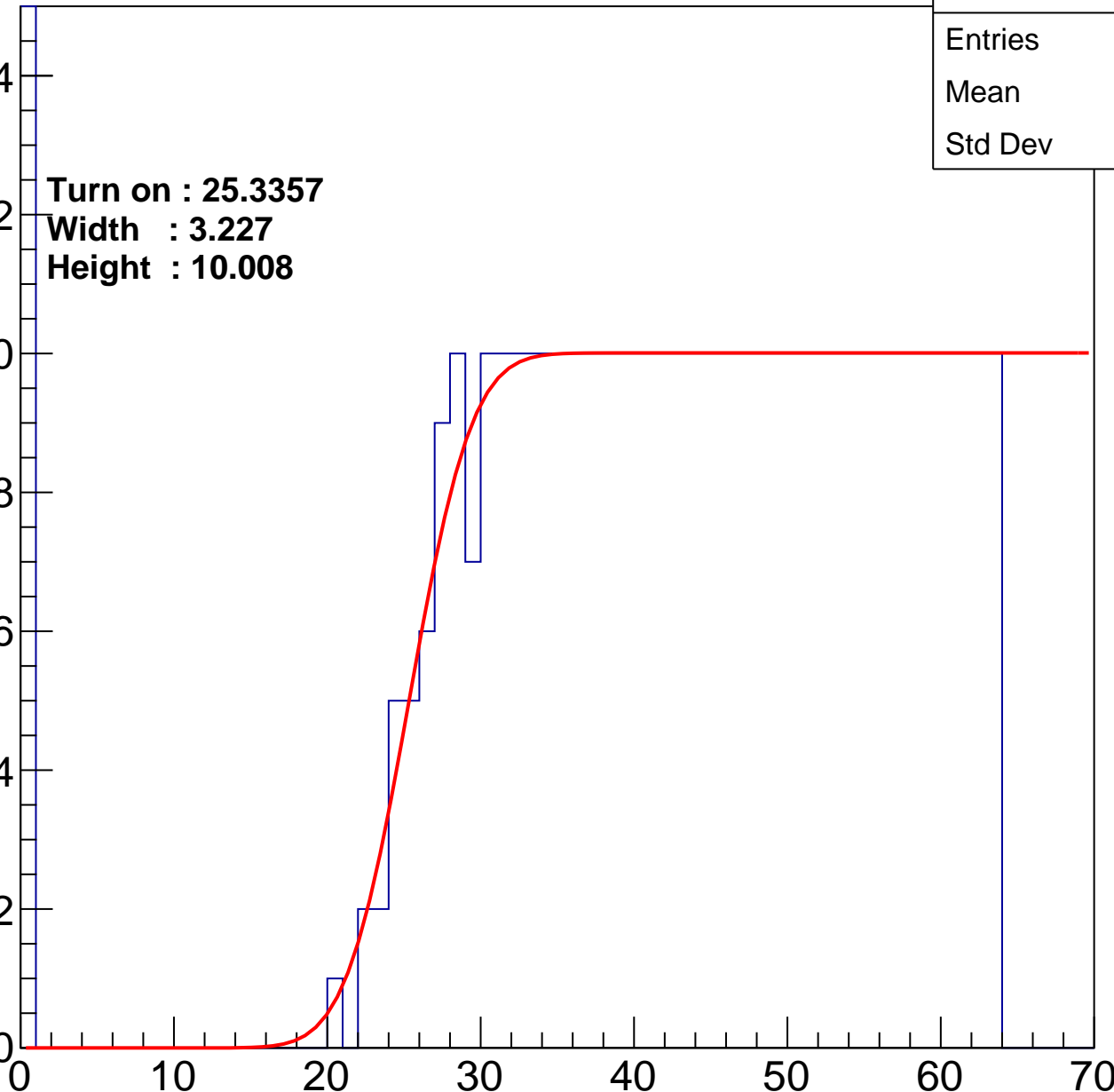
Width : 3.227

Height : 10.008

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch51

calib_packv5_041523_1651.root, FC#0, port C2

Entries	420
Mean	39.62
Std Dev	17.61

Turn on : 27.0744

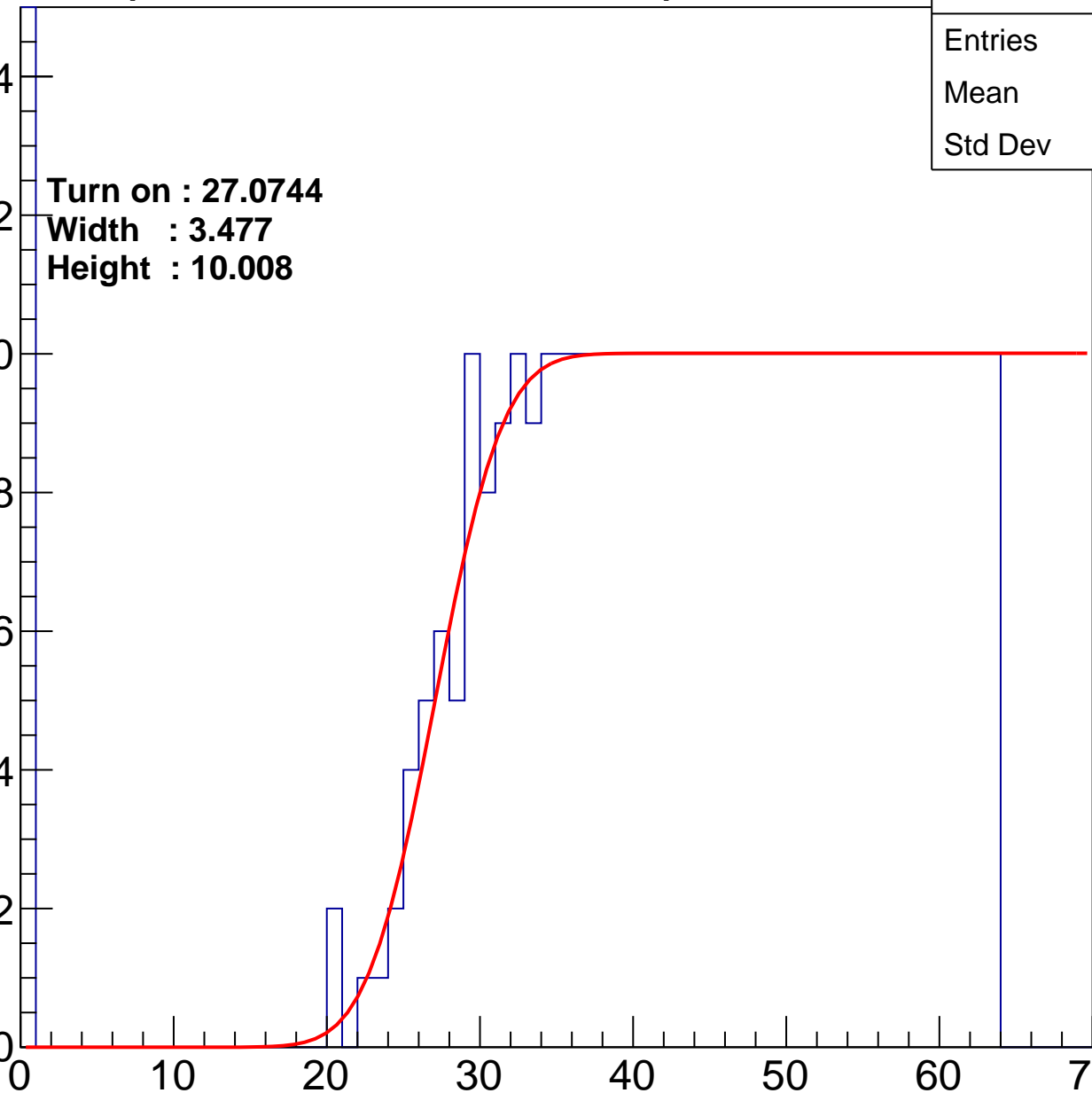
Width : 3.477

Height : 10.008

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch52

calib_packv5_041523_1651.root, FC#0, port C2

Entries	405
Mean	40.67
Std Dev	16.89

Turn on : 27.7726

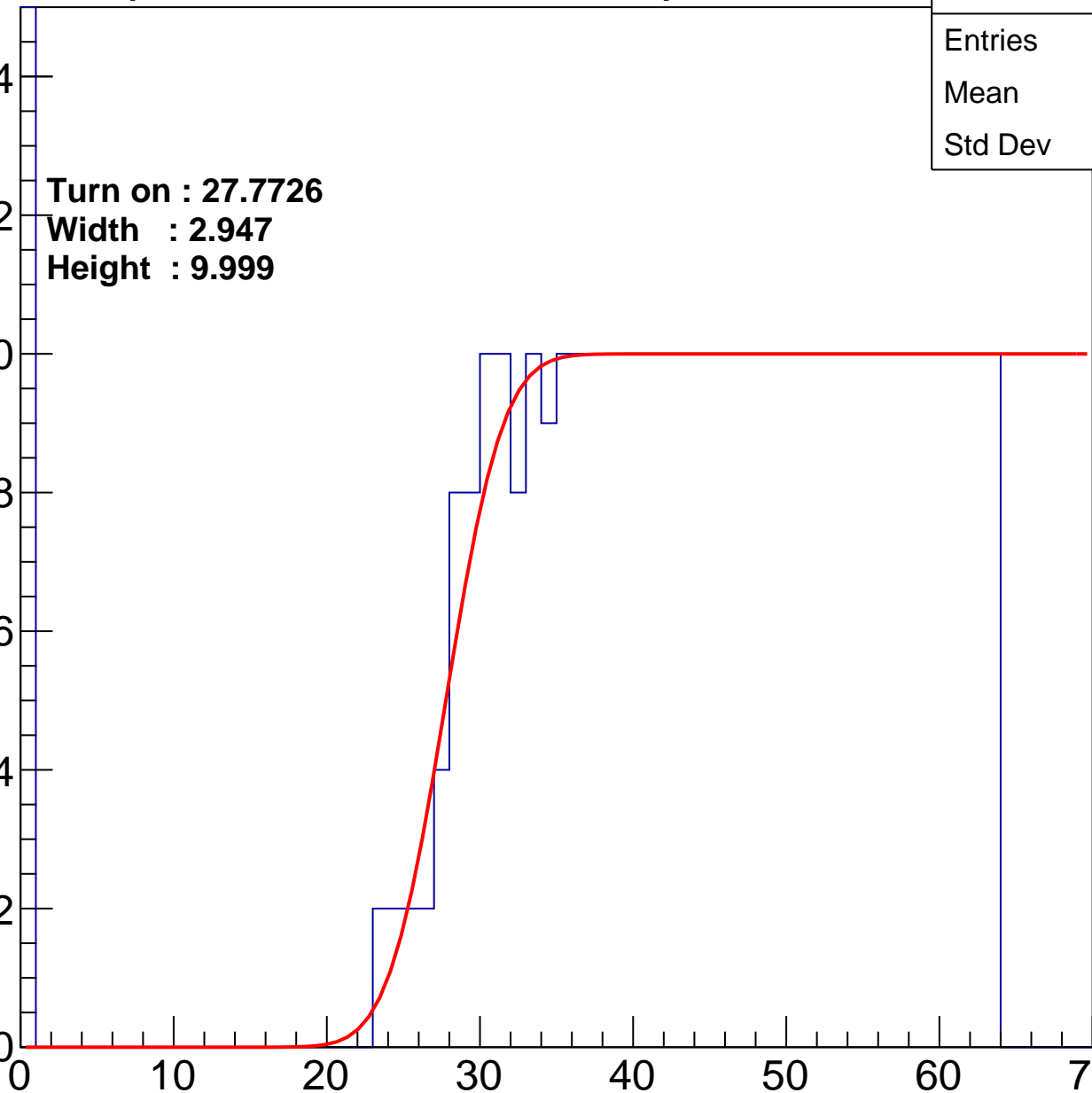
Width : 2.947

Height : 9.999

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch53

calib_packv5_041523_1651.root, FC#0, port C2

Entries	395
Mean	40.85
Std Dev	17.19

Turn on : 29.0158

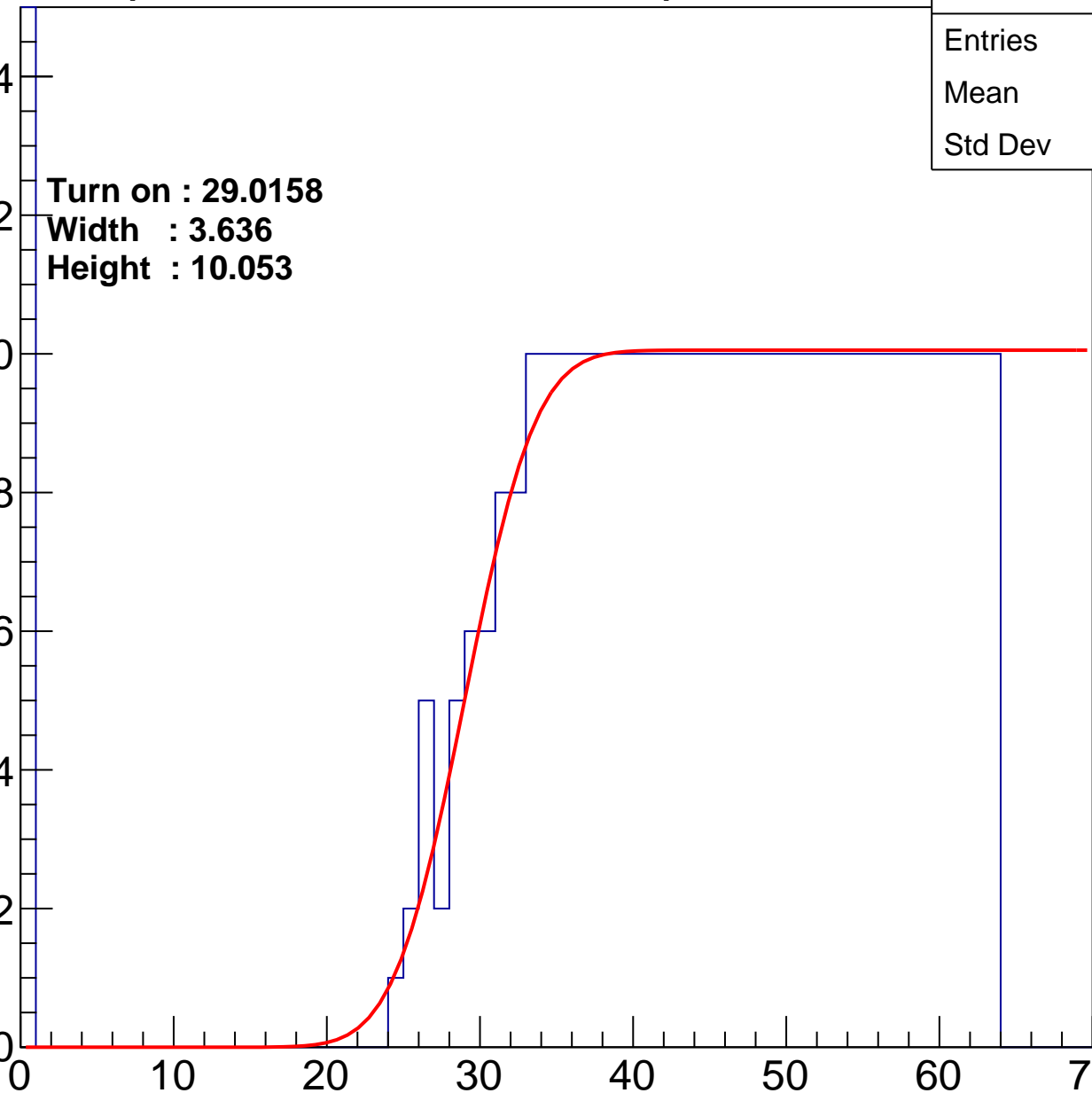
Width : 3.636

Height : 10.053

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch54

calib_packv5_041523_1651.root, FC#0, port C2

Entries	436
Mean	39.69
Std Dev	16.59

Turn on : 24.1392

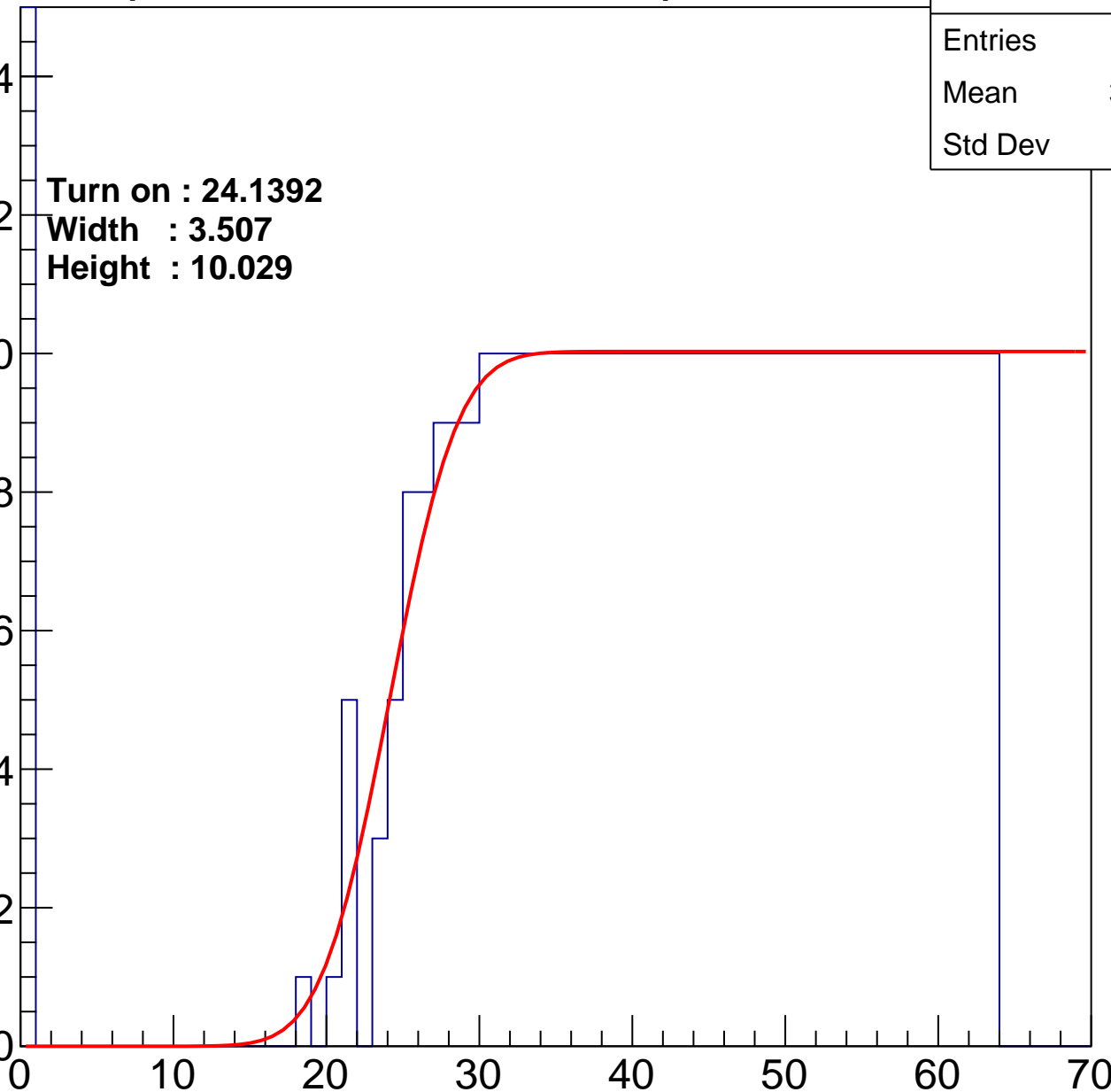
Width : 3.507

Height : 10.029

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch55

calib_packv5_041523_1651.root, FC#0, port C2

Entries	411
Mean	41.12
Std Dev	15.76

Turn on : 26.1064

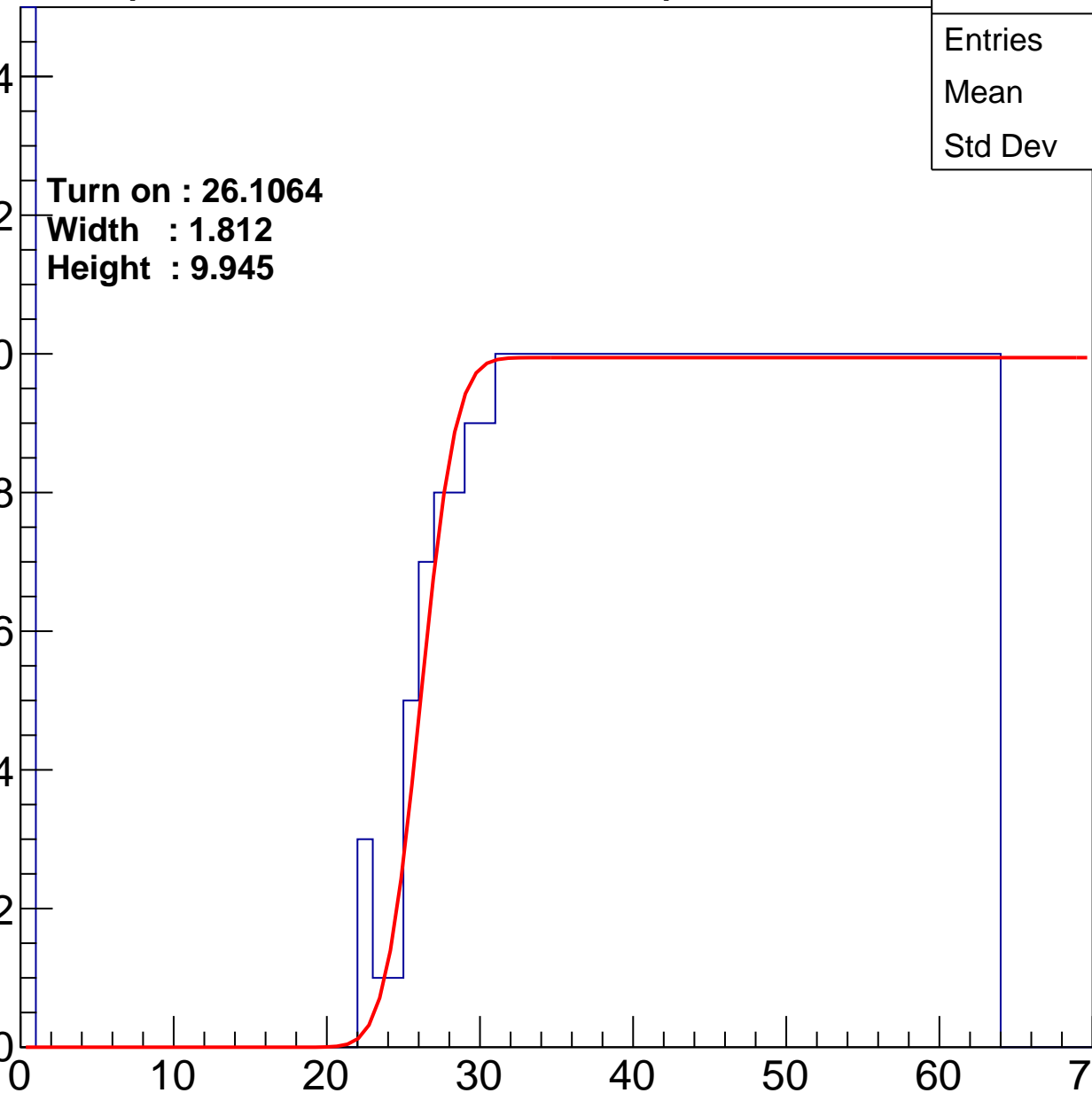
Width : 1.812

Height : 9.945

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch56

calib_packv5_041523_1651.root, FC#0, port C2

Entries	429
Mean	39.61
Std Dev	17.15

Turn on : 25.8298

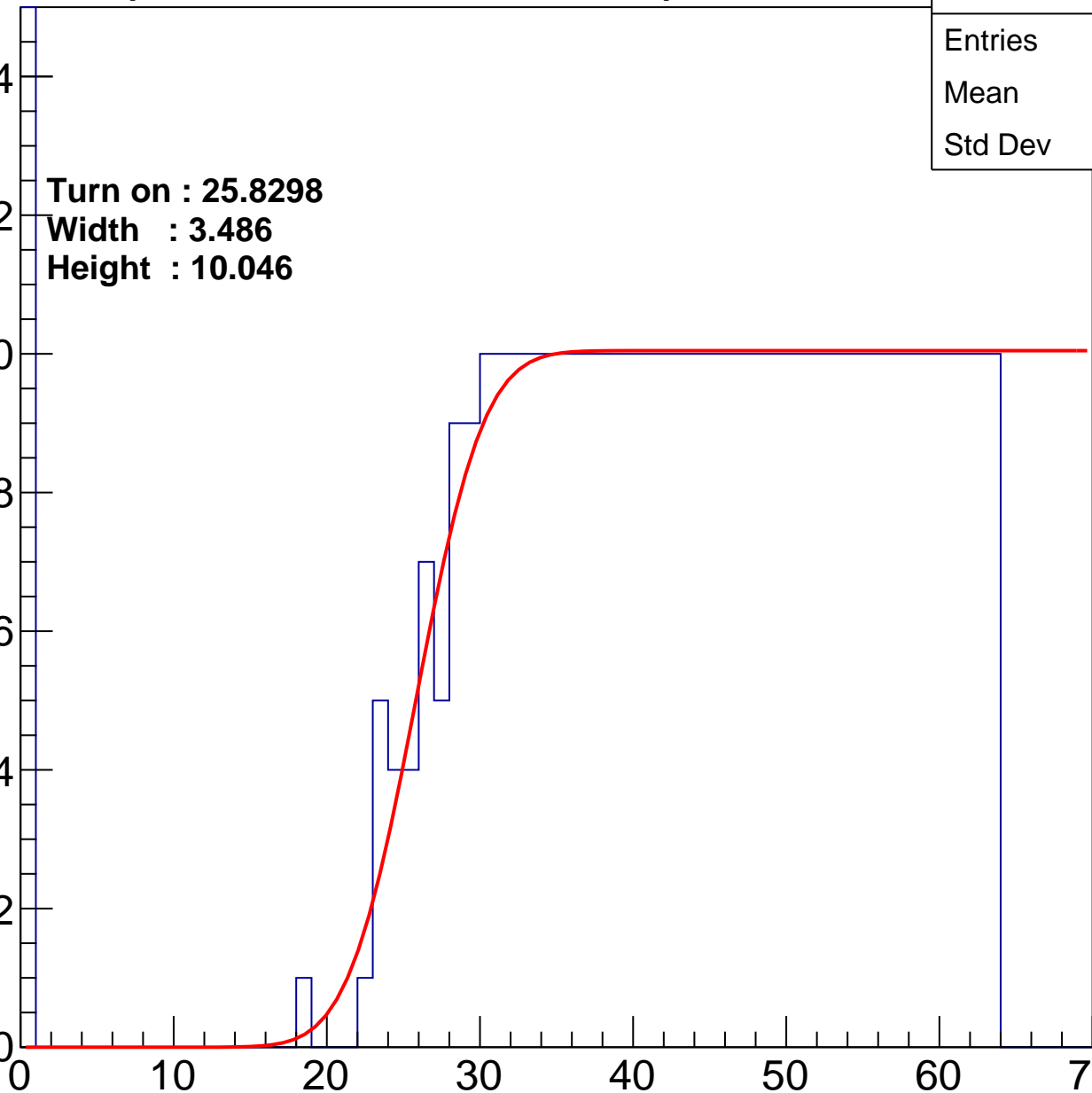
Width : 3.486

Height : 10.046

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch57

calib_packv5_041523_1651.root, FC#0, port C2

Entries	419
Mean	39.75
Std Dev	17.5

Turn on : 27.1455

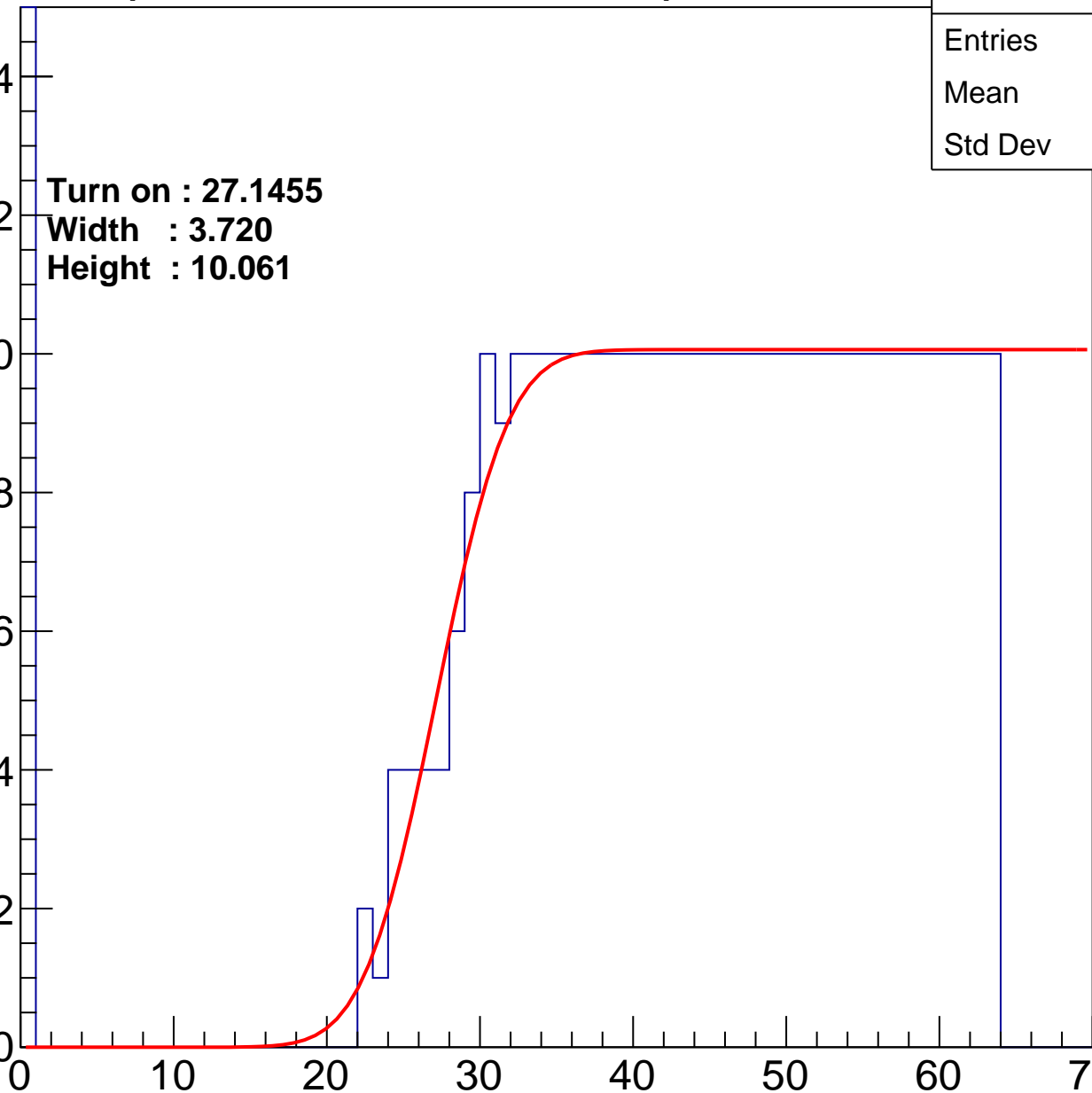
Width : 3.720

Height : 10.061

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch58

calib_packv5_041523_1651.root, FC#0, port C2

Entries	433
Mean	39.09
Std Dev	17.73

Turn on : 26.0558

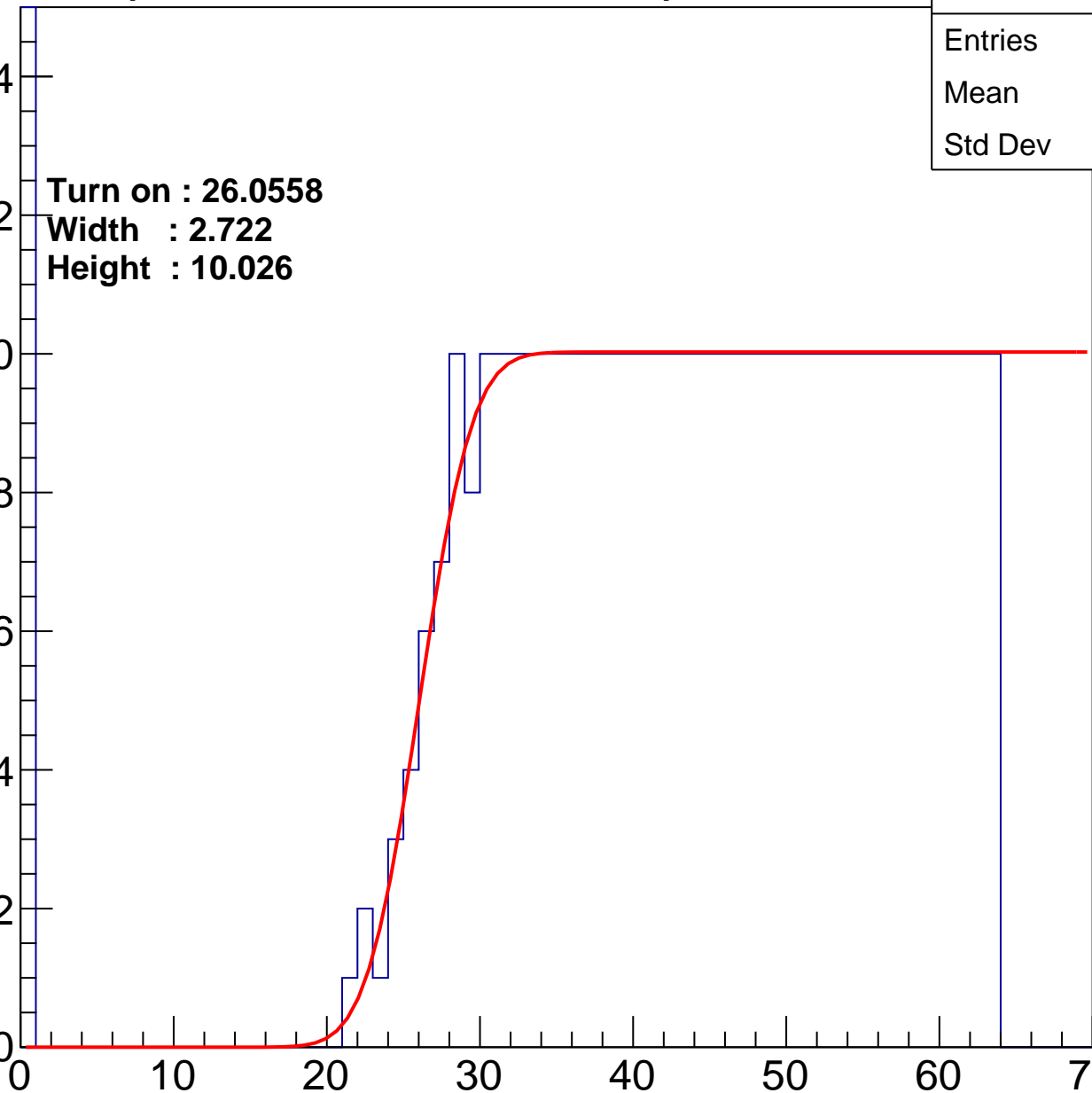
Width : 2.722

Height : 10.026

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch59

calib_packv5_041523_1651.root, FC#0, port C2

Entries	423
Mean	40.43
Std Dev	16.18

Turn on : 25.1704

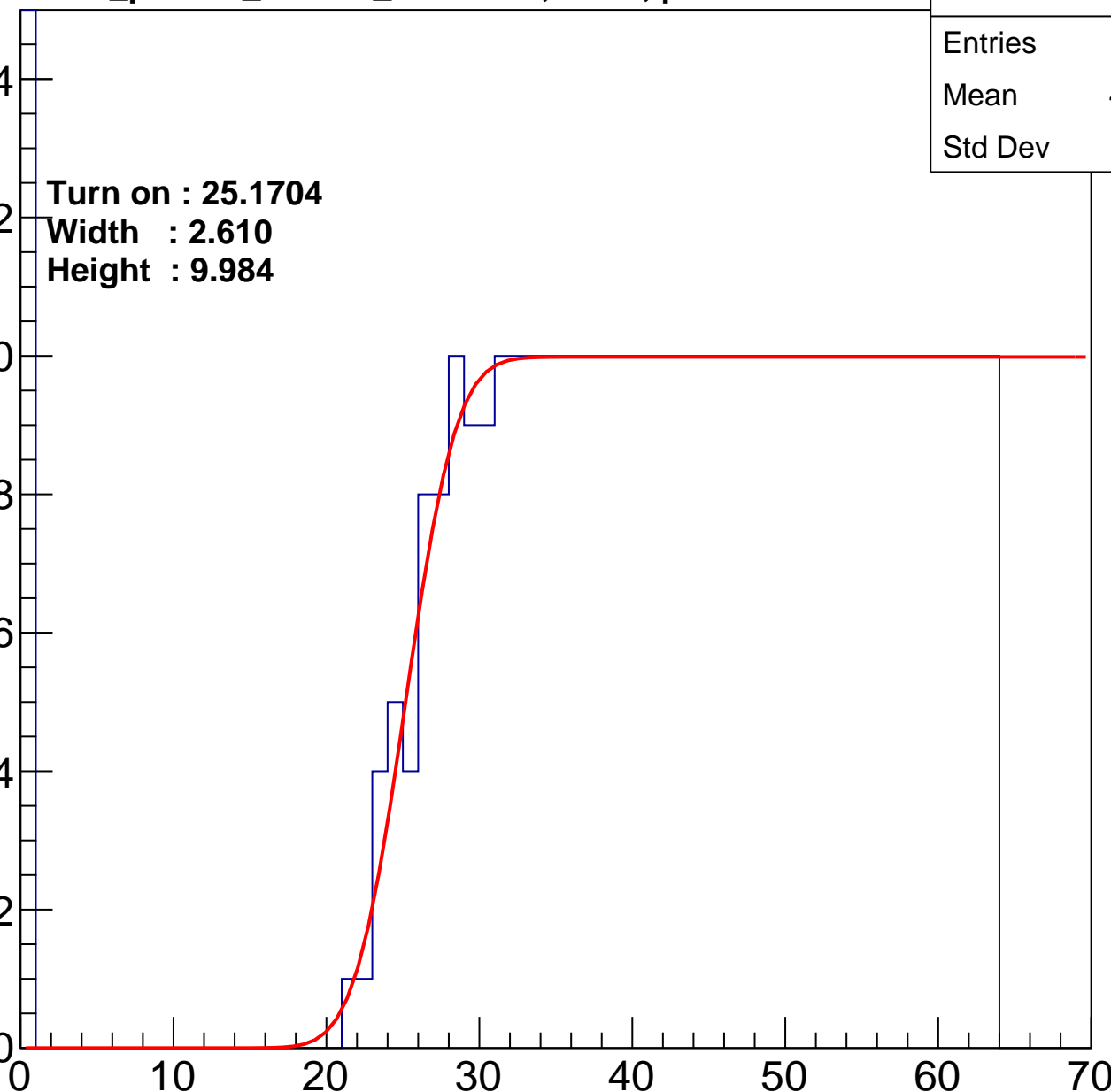
Width : 2.610

Height : 9.984

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch60

calib_packv5_041523_1651.root, FC#0, port C2

Entries	433
Mean	39.75
Std Dev	16.69

Turn on : 24.6908

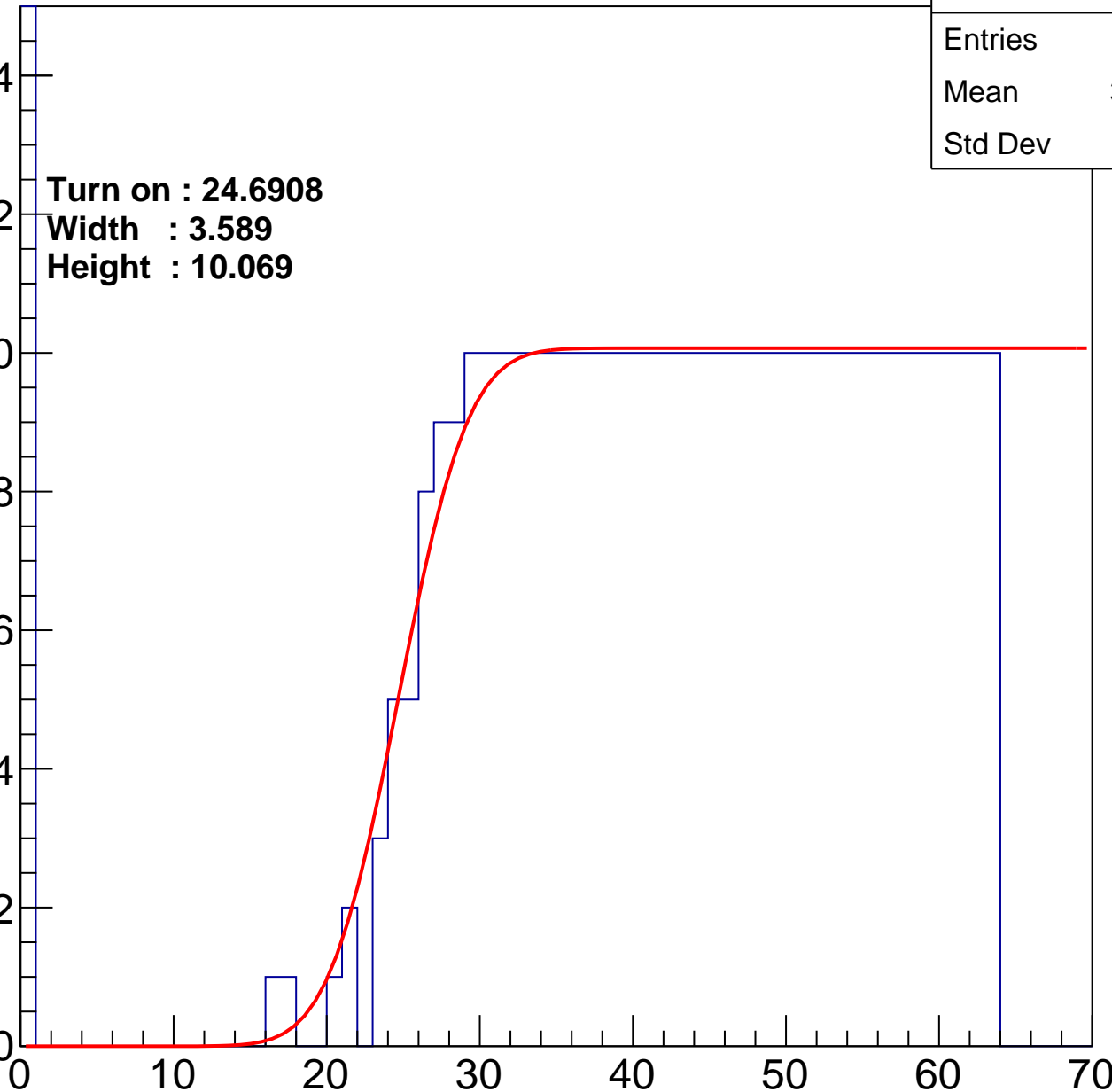
Width : 3.589

Height : 10.069

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch61

calib_packv5_041523_1651.root, FC#0, port C2

Entries	413
Mean	40.55
Std Dev	16.61

Turn on : 26.6039

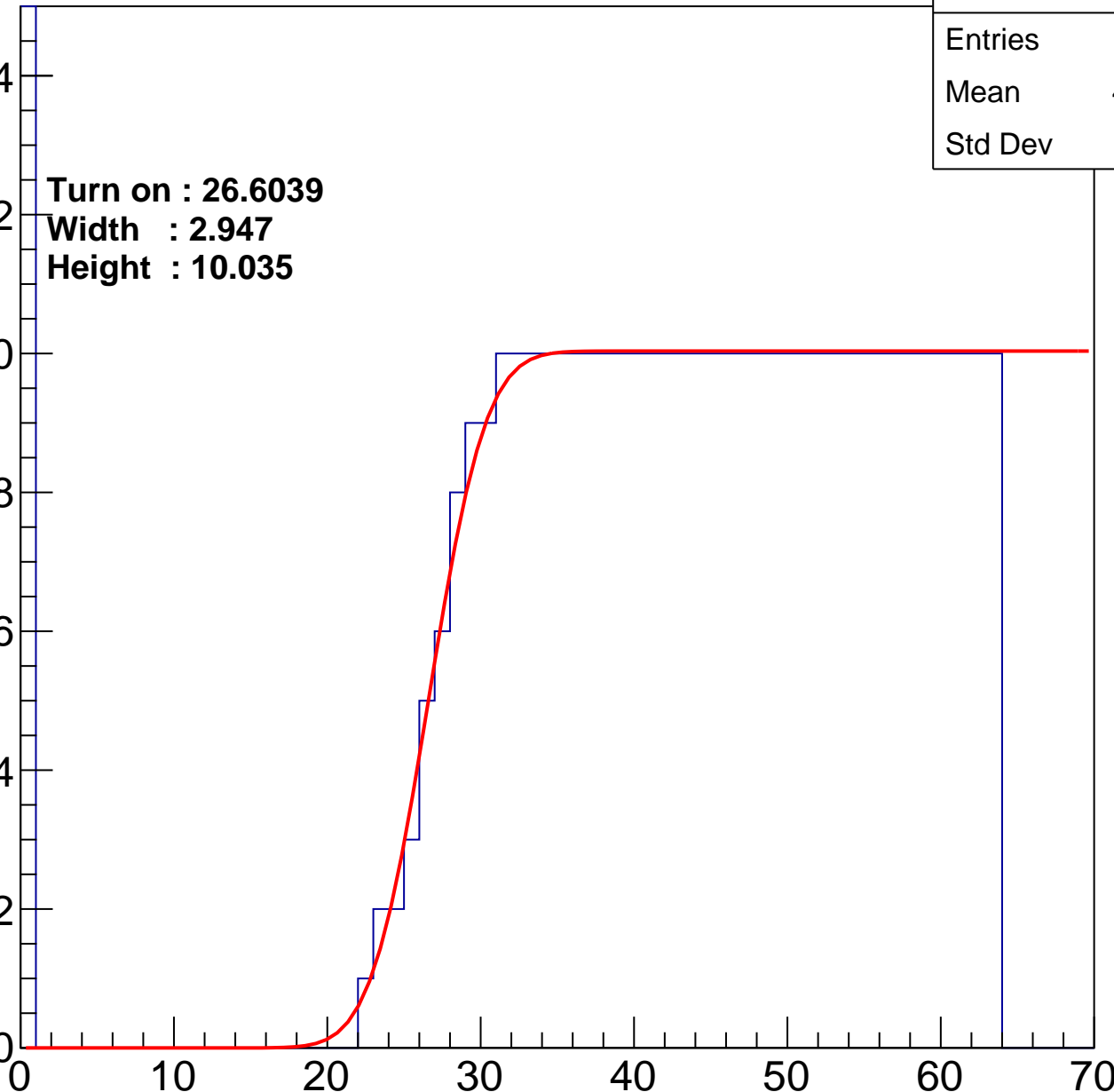
Width : 2.947

Height : 10.035

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch62

calib_packv5_041523_1651.root, FC#0, port C2

Entries	427
Mean	39.47
Std Dev	17.45

Turn on : 26.1178

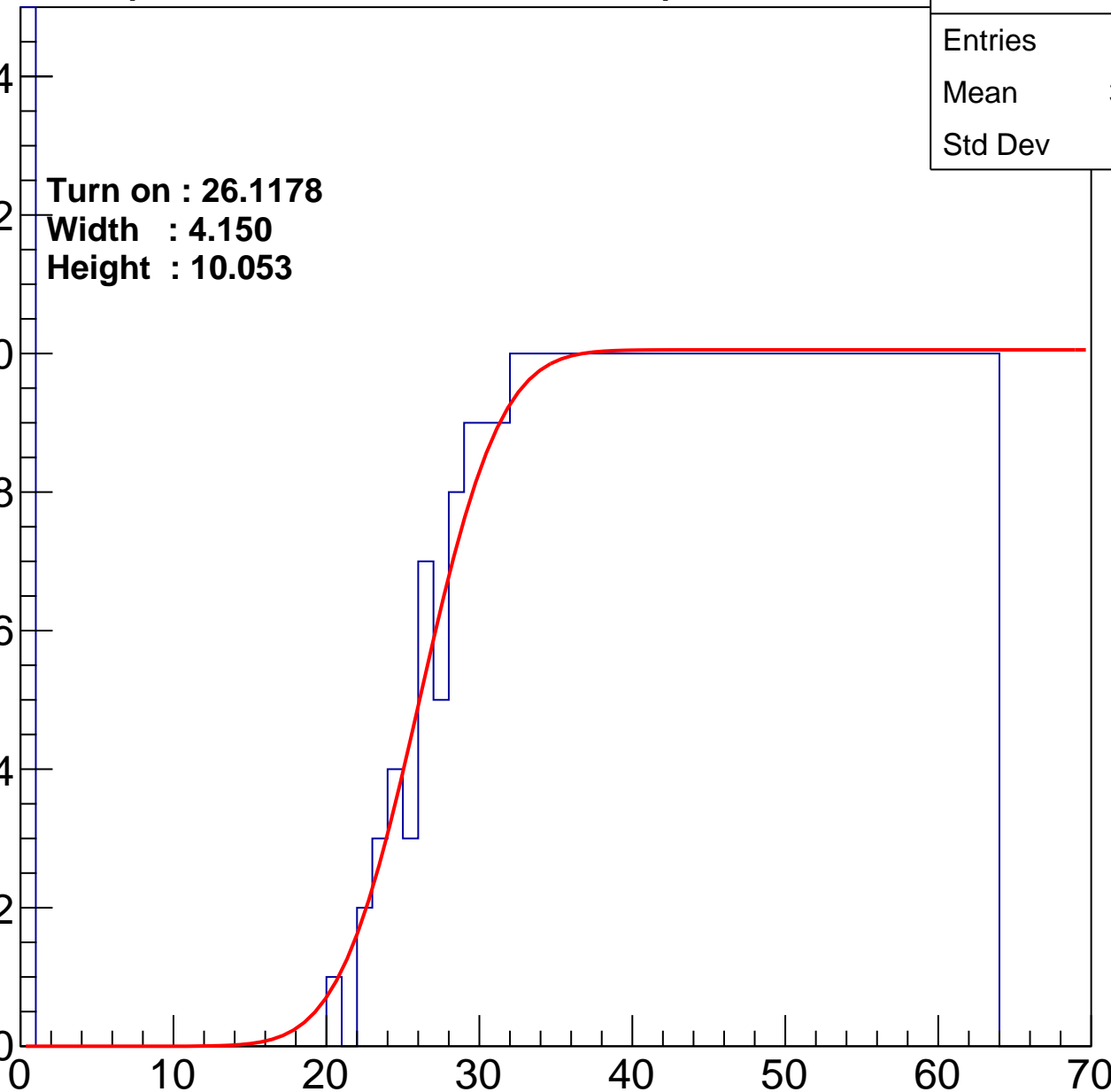
Width : 4.150

Height : 10.053

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch63

calib_packv5_041523_1651.root, FC#0, port C2

Entries	405
Mean	40.25
Std Dev	17.58

Turn on : 28.4008

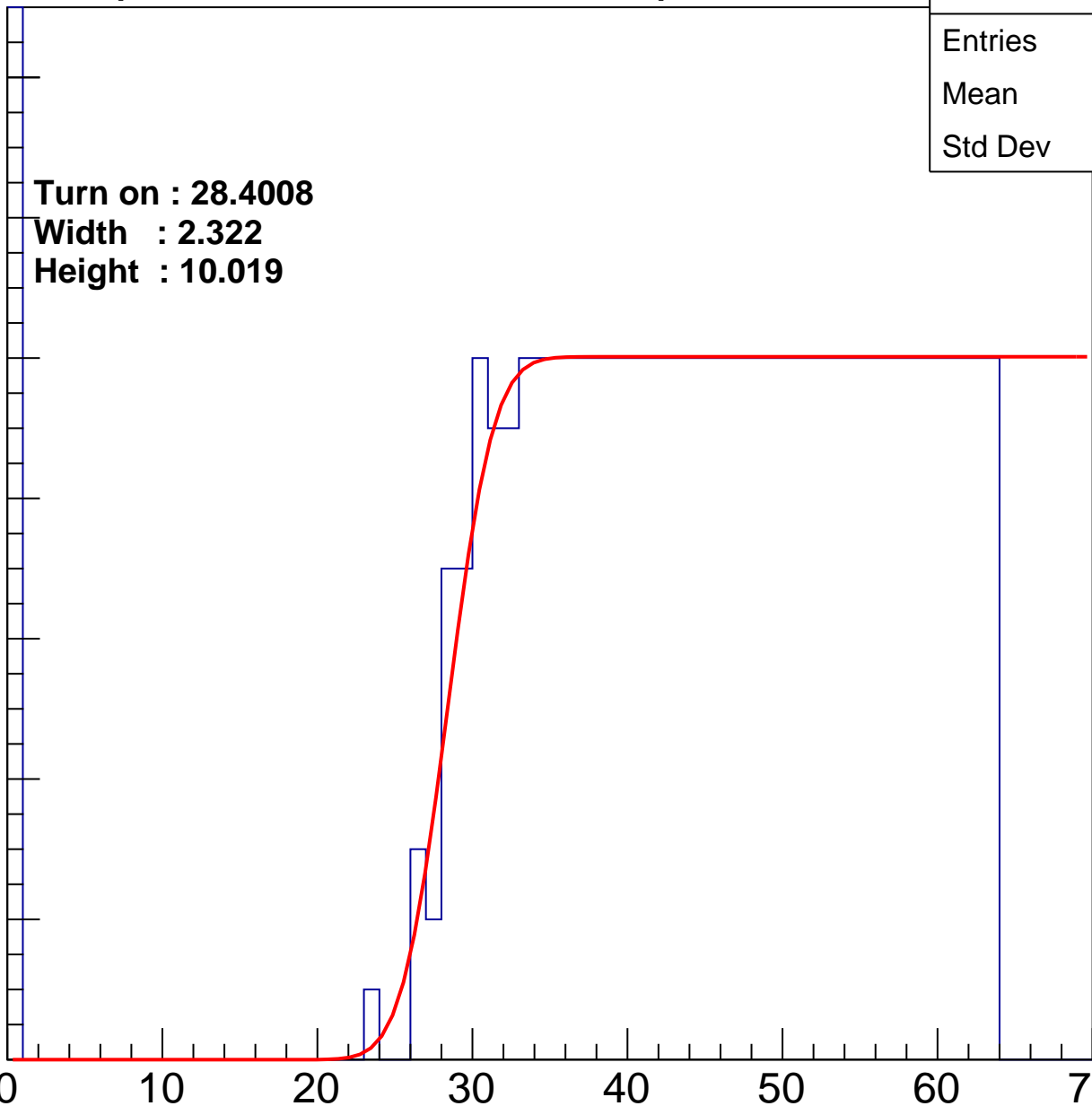
Width : 2.322

Height : 10.019

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch64

calib_packv5_041523_1651.root, FC#0, port C2

Entries	443
Mean	38.75
Std Dev	17.64

Turn on : 25.9290

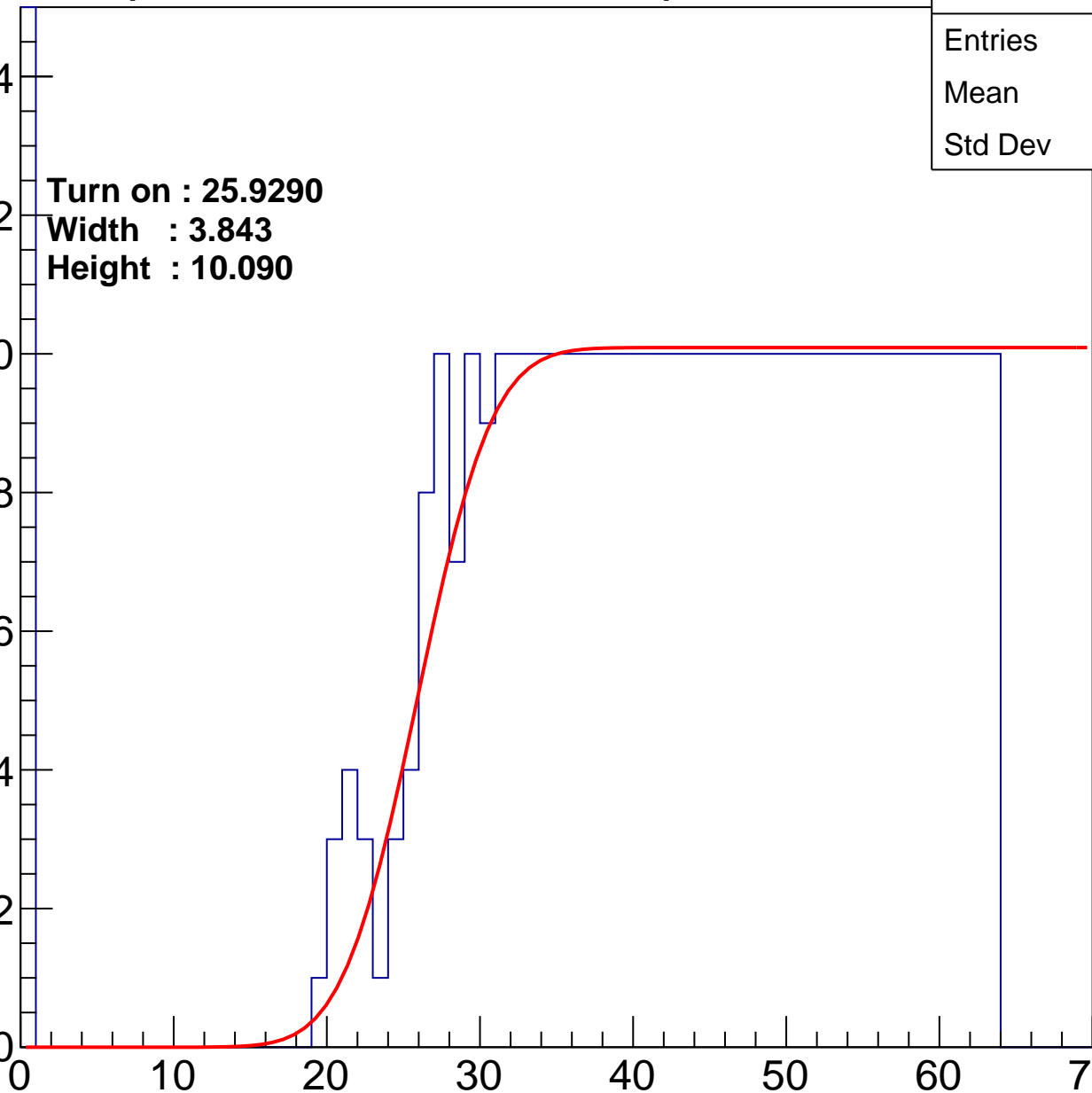
Width : 3.843

Height : 10.090

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch65

calib_packv5_041523_1651.root, FC#0, port C2

Entries	415
Mean	40.31
Std Dev	16.9

Turn on : 26.7569

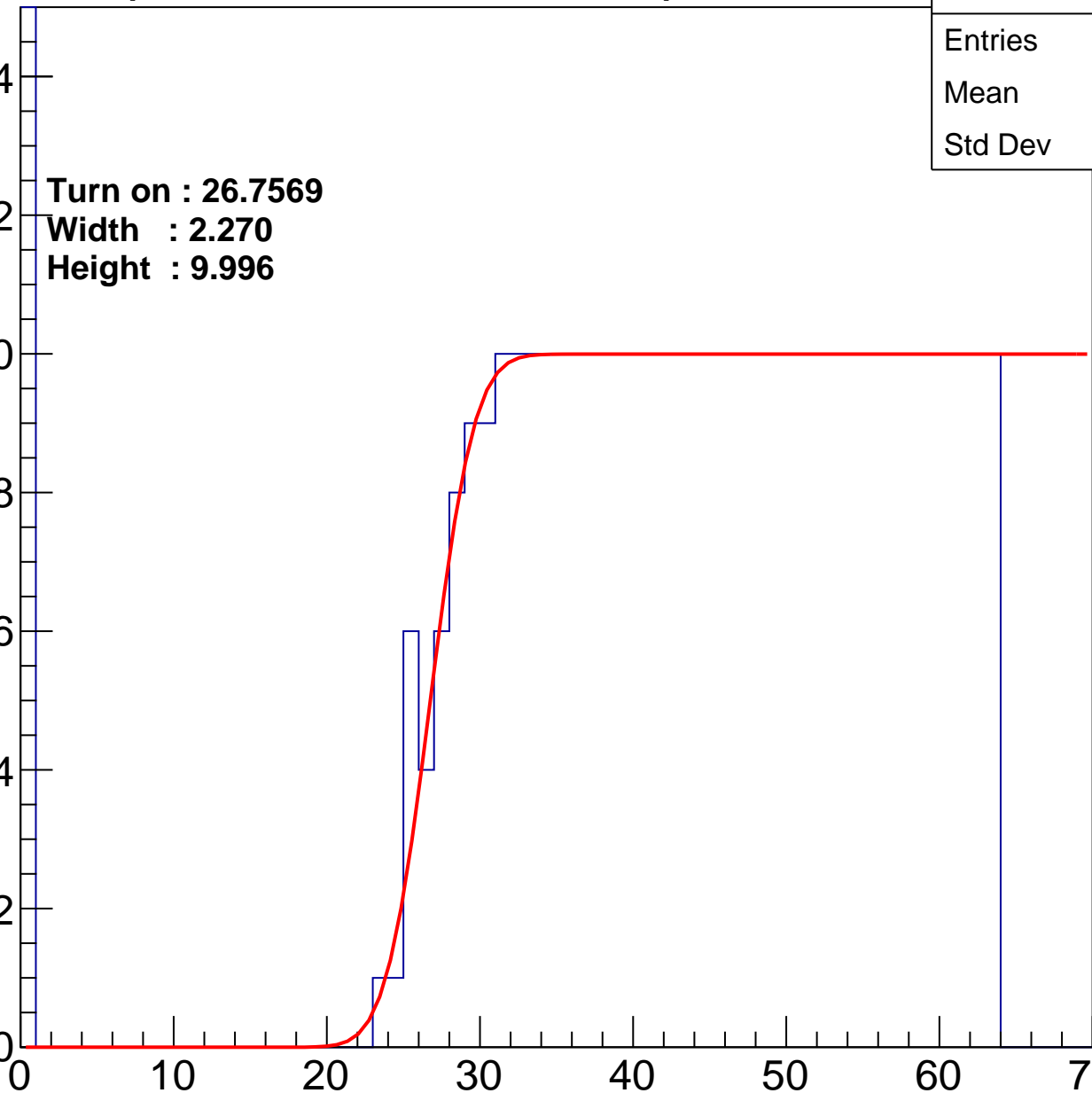
Width : 2.270

Height : 9.996

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch66

calib_packv5_041523_1651.root, FC#0, port C2

Entries	436
Mean	39.5
Std Dev	16.89

Turn on : 25.1760

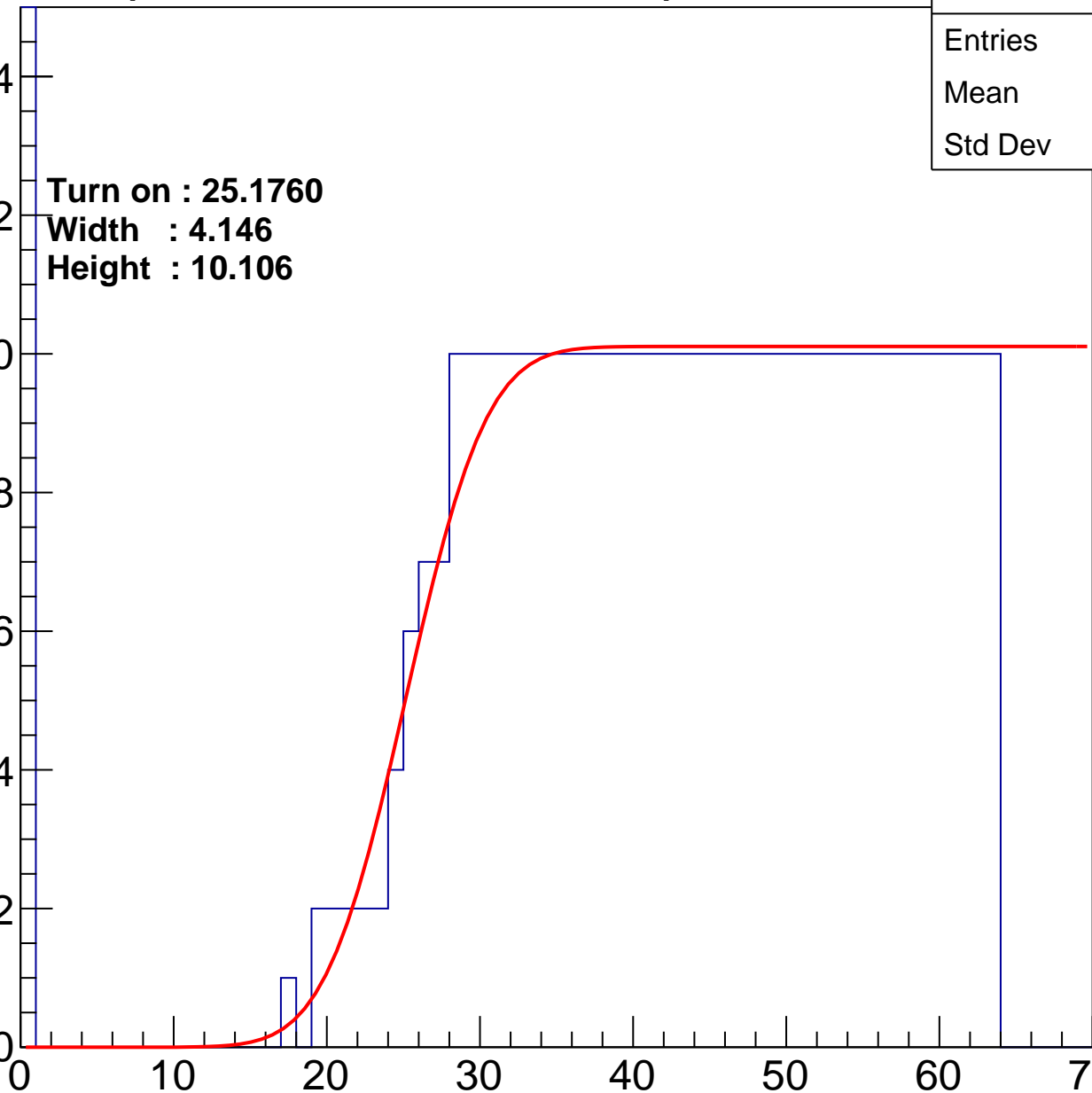
Width : 4.146

Height : 10.106

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch67

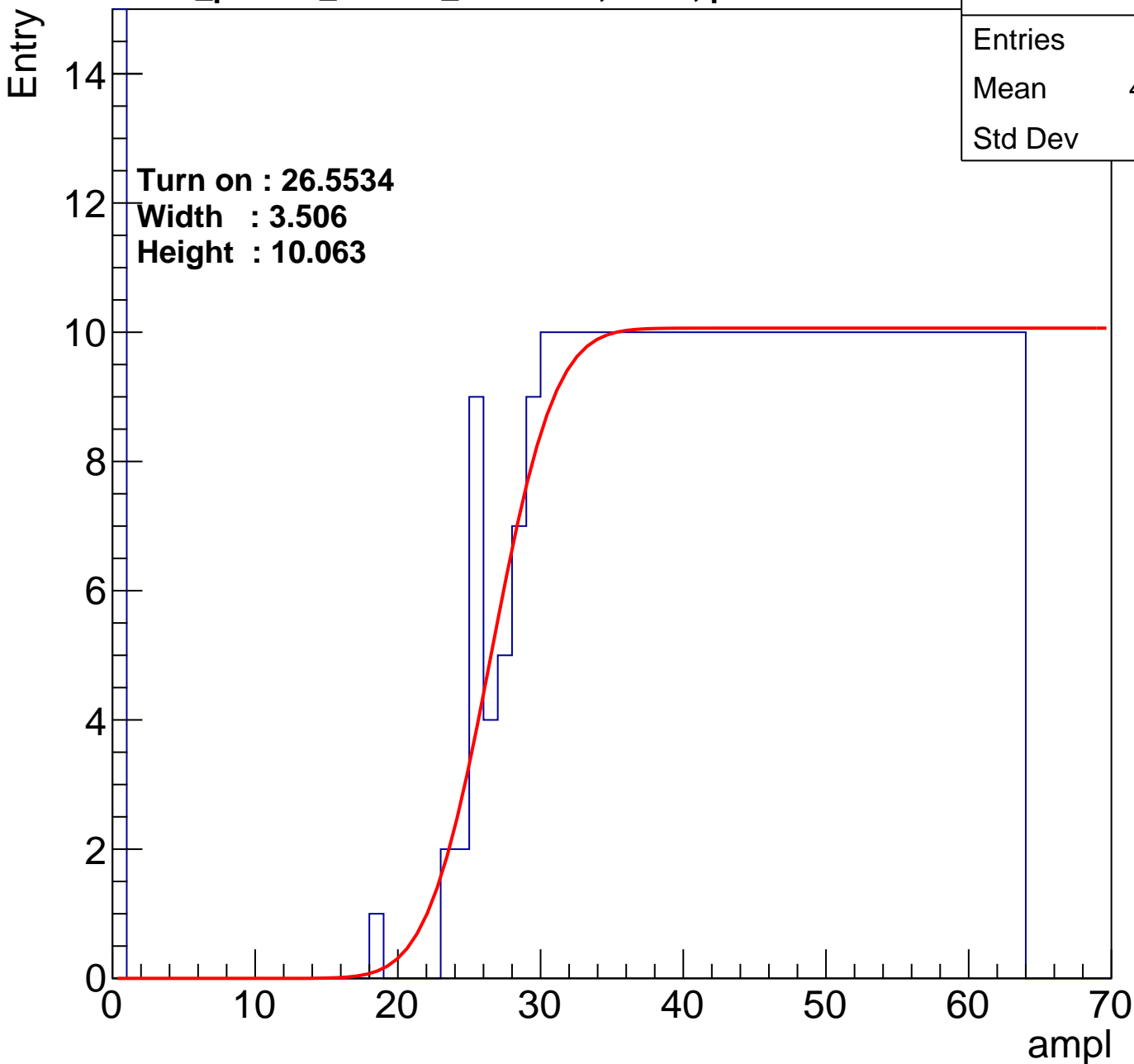
calib_packv5_041523_1651.root, FC#0, port C2

Entries	421
Mean	40.01
Std Dev	17

Turn on : 26.5534

Width : 3.506

Height : 10.063



B1L103S, U9-ch68

calib_packv5_041523_1651.root, FC#0, port C2

Entries	411
Mean	40.92
Std Dev	16.09

Turn on : 25.4750

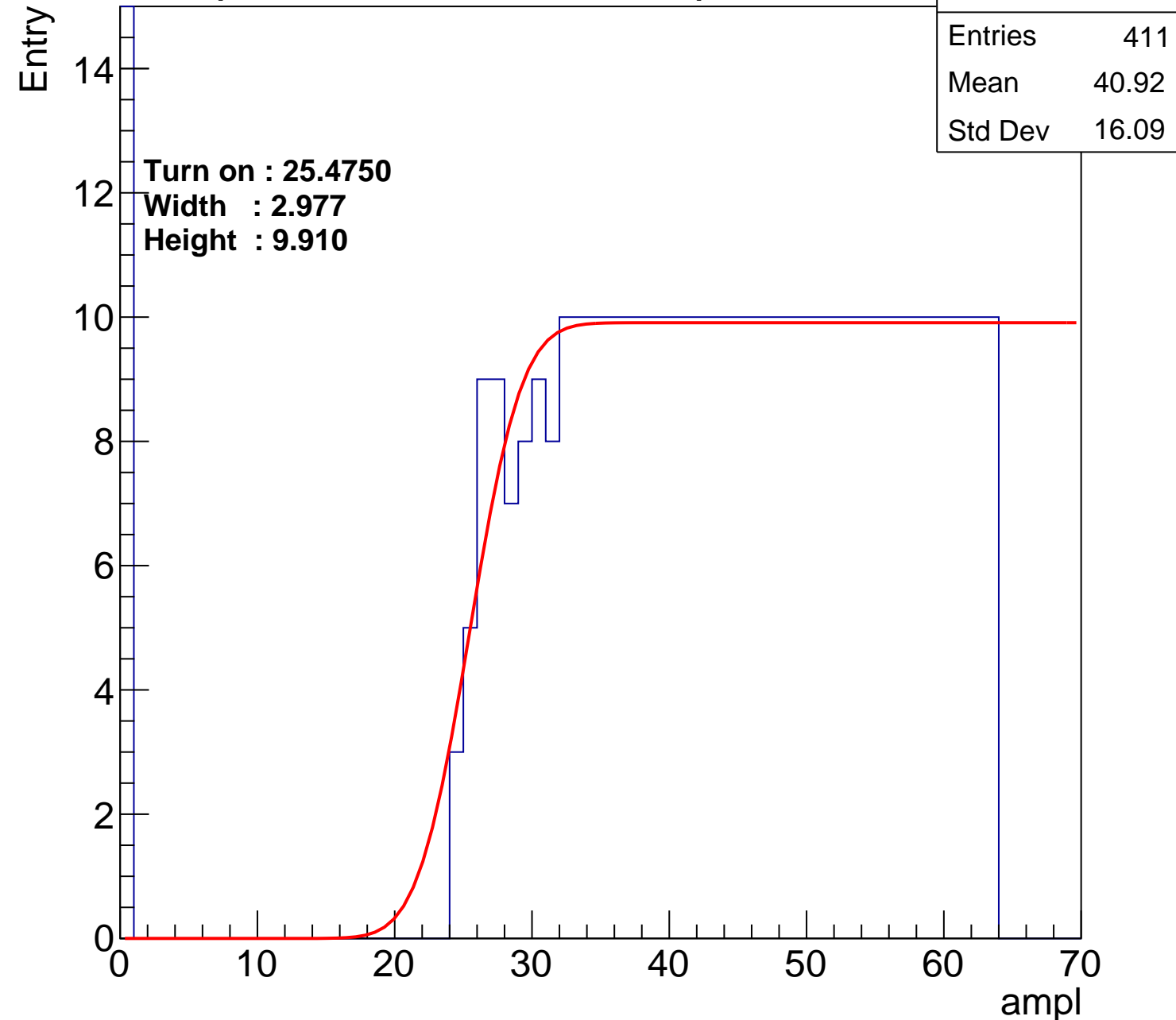
Width : 2.977

Height : 9.910

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch69

calib_packv5_041523_1651.root, FC#0, port C2

Entries	408
Mean	40.82
Std Dev	16.45

Turn on : 27.3232

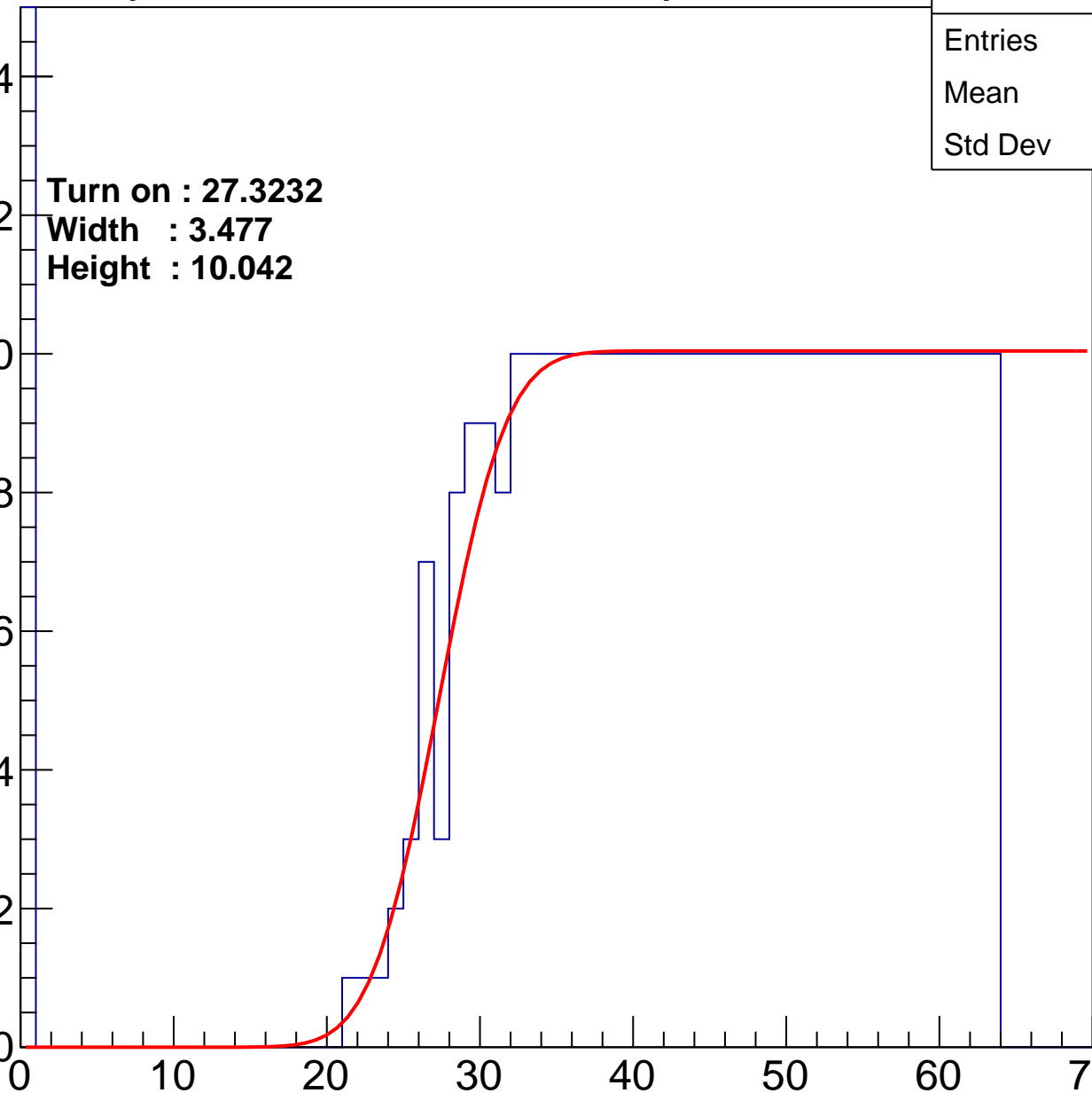
Width : 3.477

Height : 10.042

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch70

calib_packv5_041523_1651.root, FC#0, port C2

Entries	404
Mean	40.85
Std Dev	16.66

Turn on : 27.4422

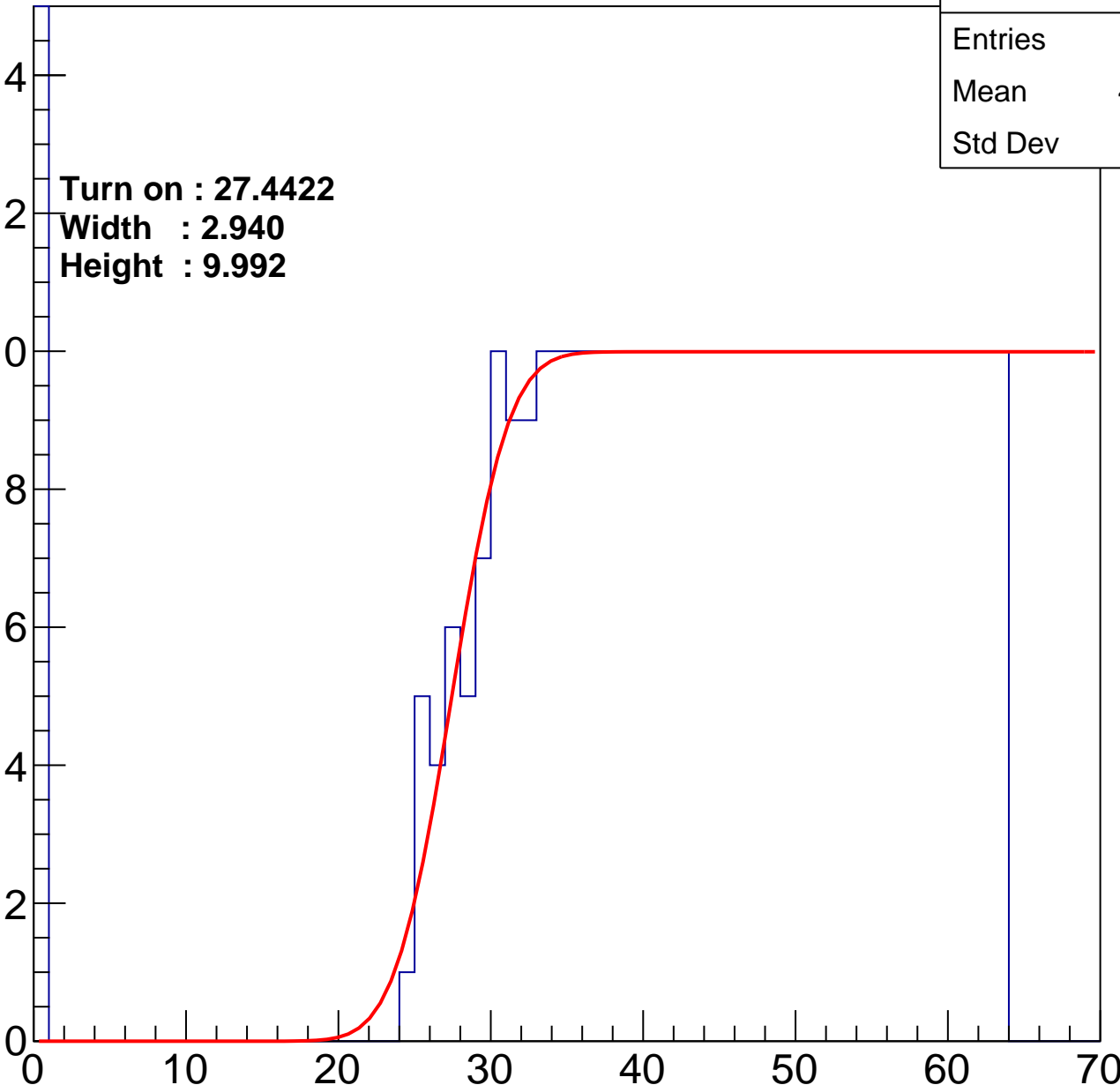
Width : 2.940

Height : 9.992

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch71

calib_packv5_041523_1651.root, FC#0, port C2

Entries	435
Mean	39.31
Std Dev	17.28

Turn on : 24.7971

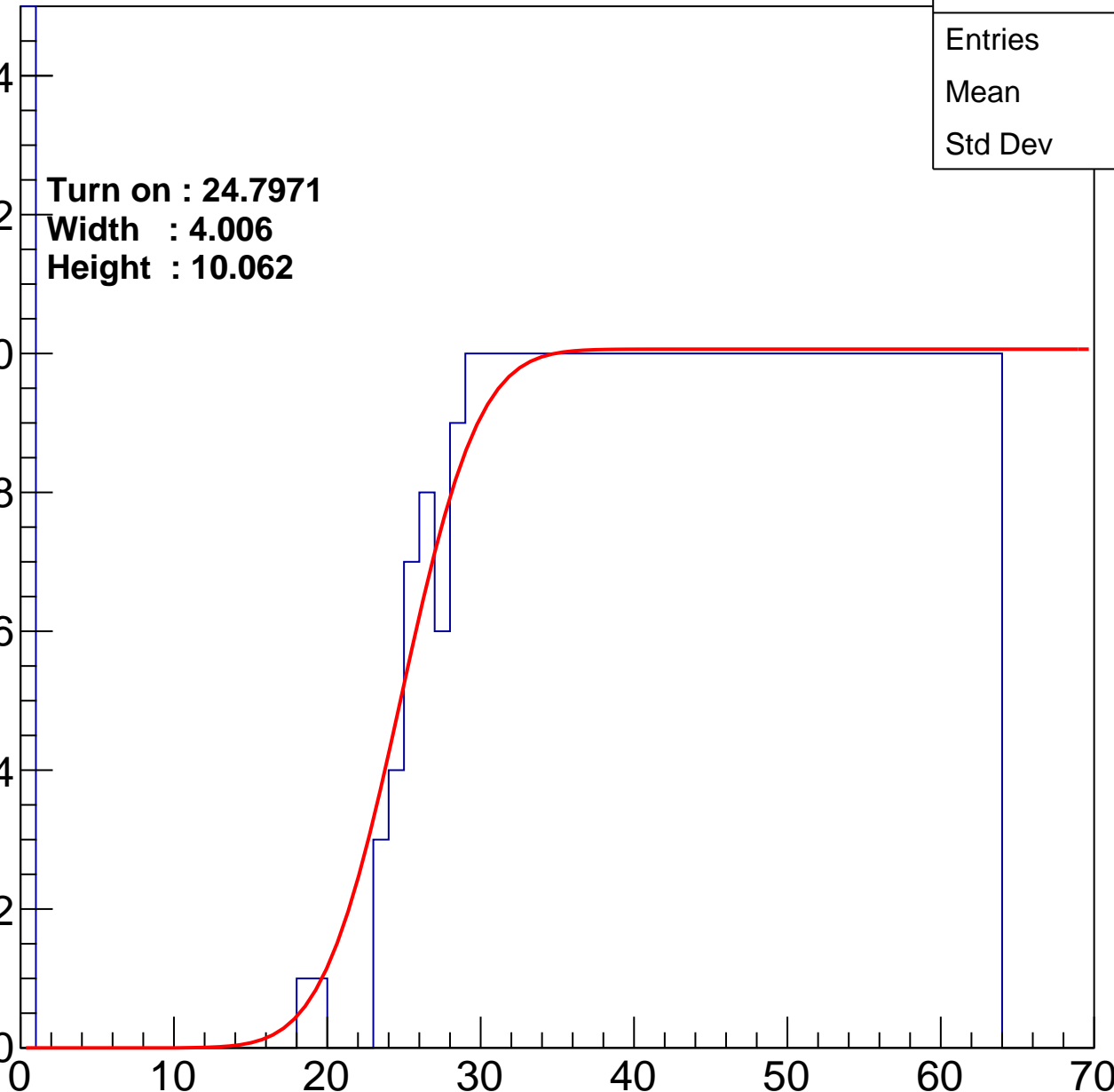
Width : 4.006

Height : 10.062

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch72

calib_packv5_041523_1651.root, FC#0, port C2

Entries	423
Mean	40.51
Std Dev	16.02

Turn on : 25.2689

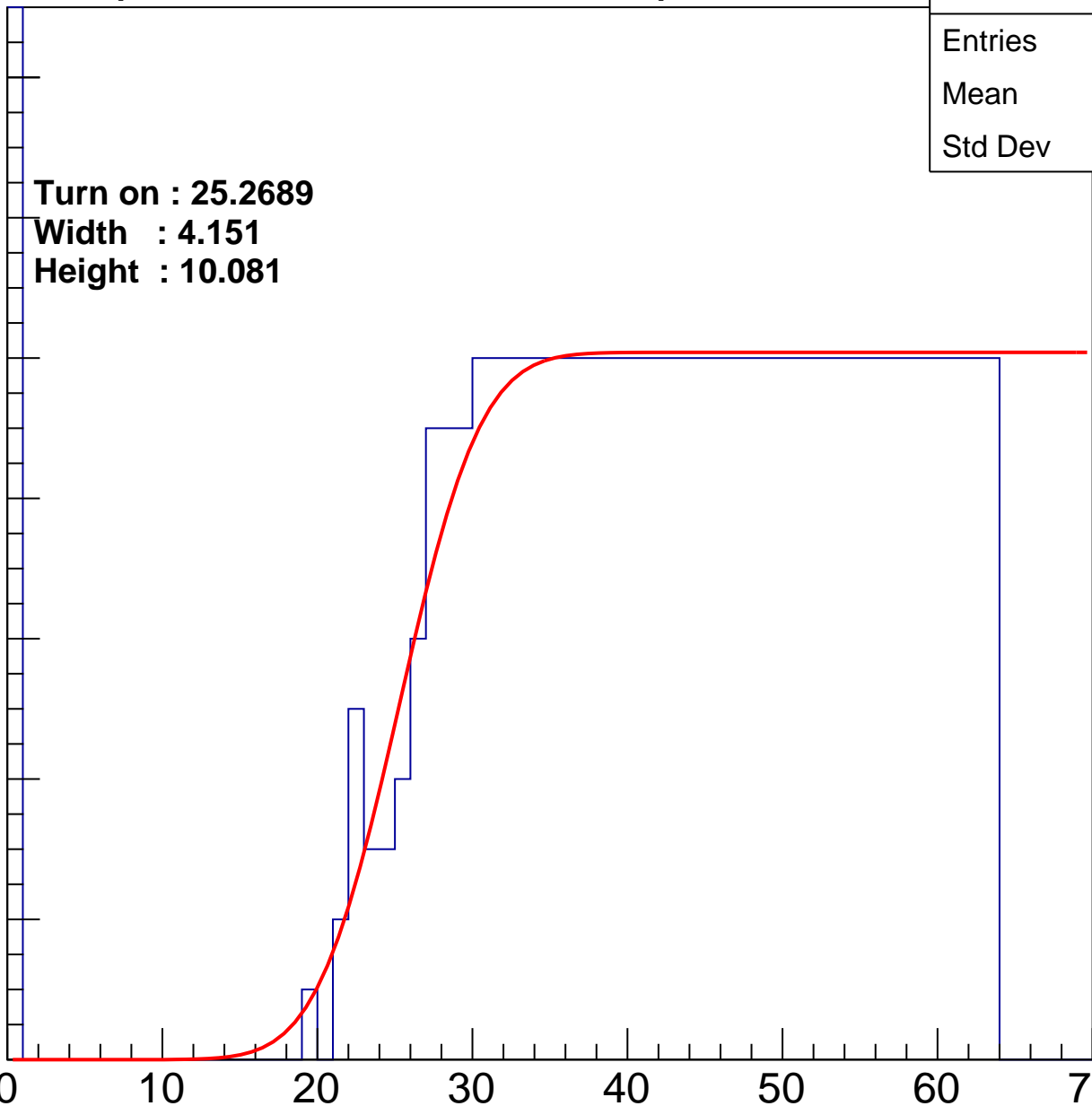
Width : 4.151

Height : 10.081

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch73

calib_packv5_041523_1651.root, FC#0, port C2

Entries	419
Mean	39.9
Std Dev	17.28

Turn on : 26.6756

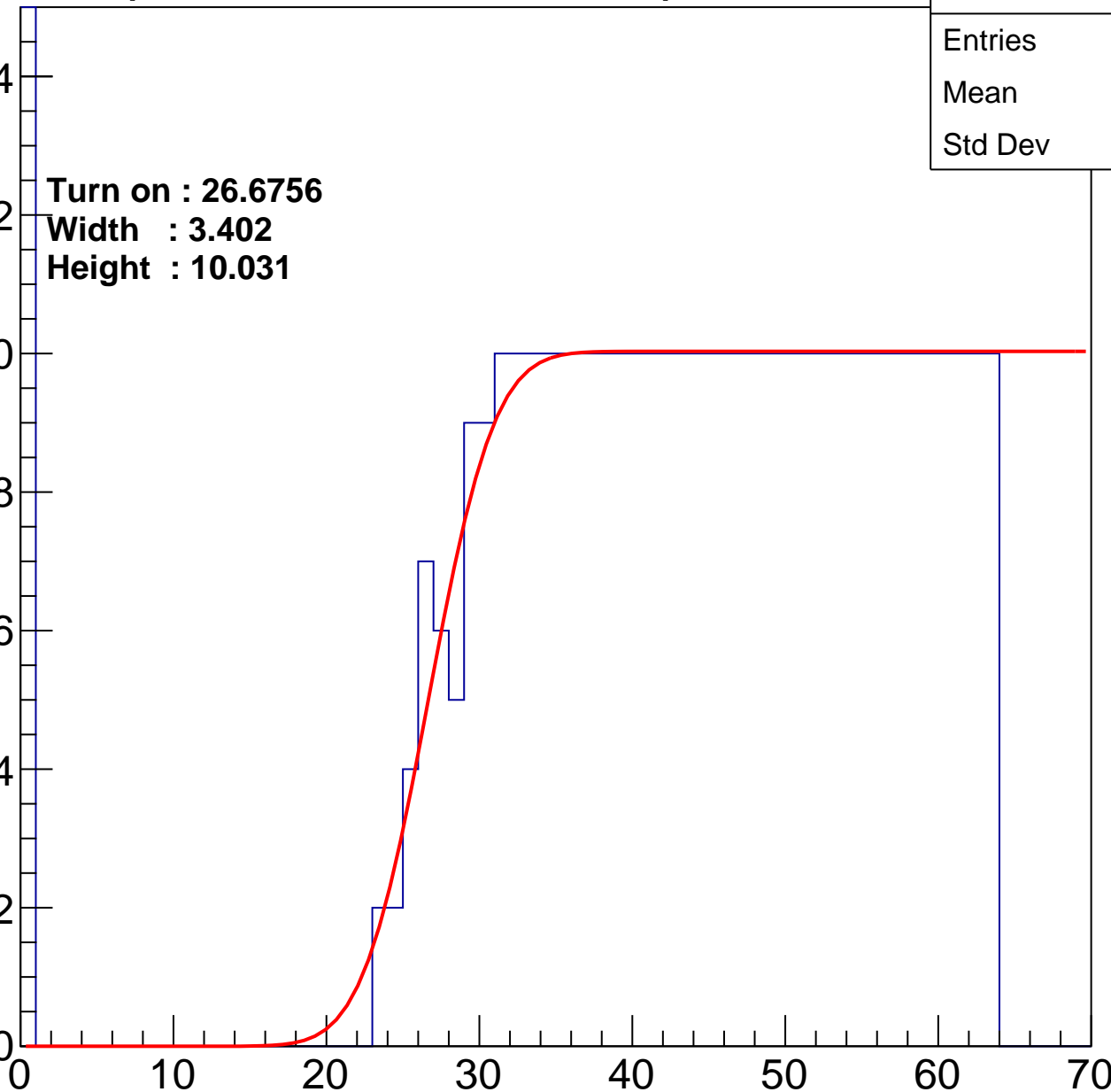
Width : 3.402

Height : 10.031

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch74

calib_packv5_041523_1651.root, FC#0, port C2

Entries	436
Mean	39.67
Std Dev	16.65

Turn on : 24.3435

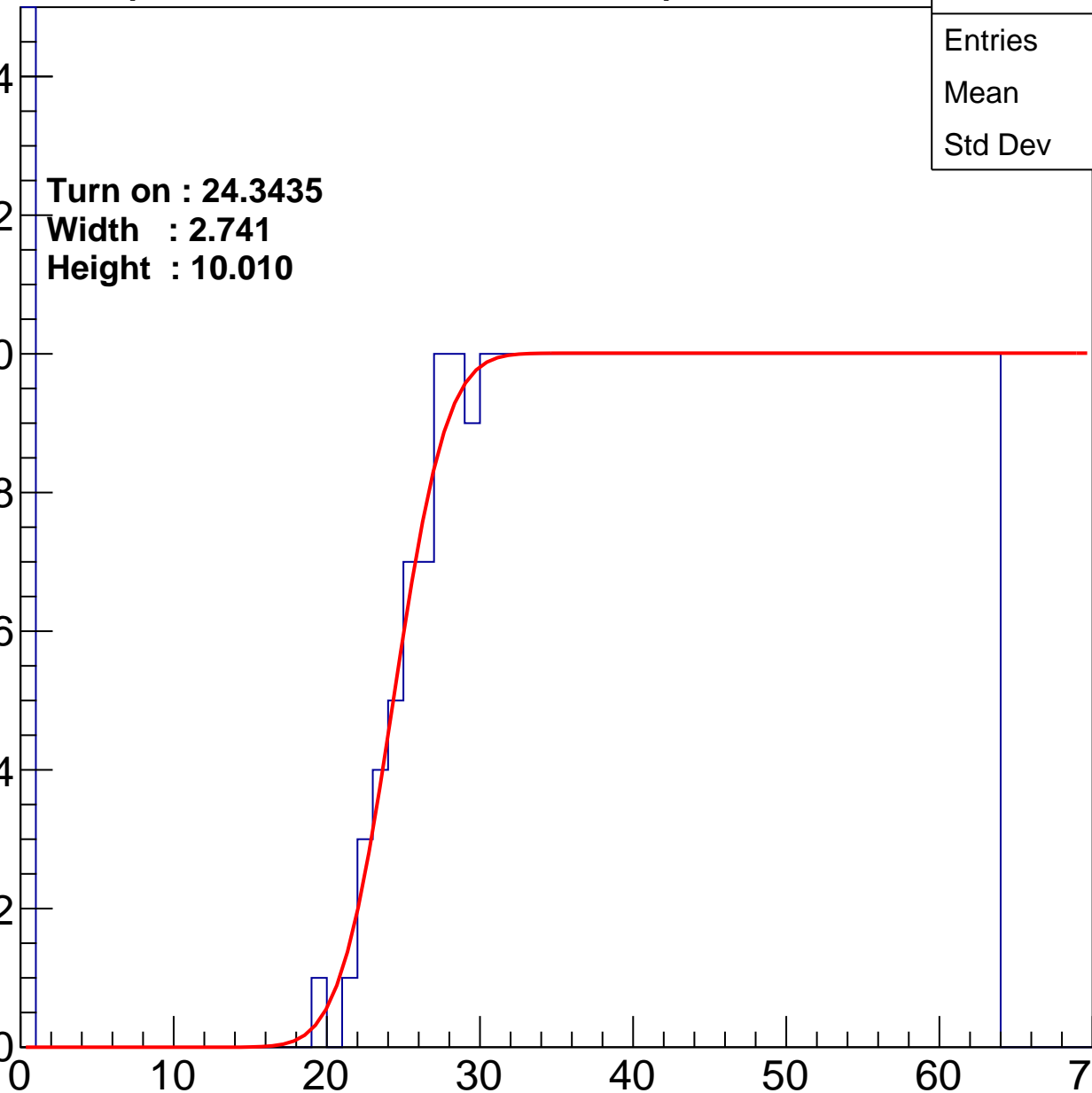
Width : 2.741

Height : 10.010

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch75

calib_packv5_041523_1651.root, FC#0, port C2

Entries	439
Mean	39.16
Std Dev	17.28

Turn on : 25.6652

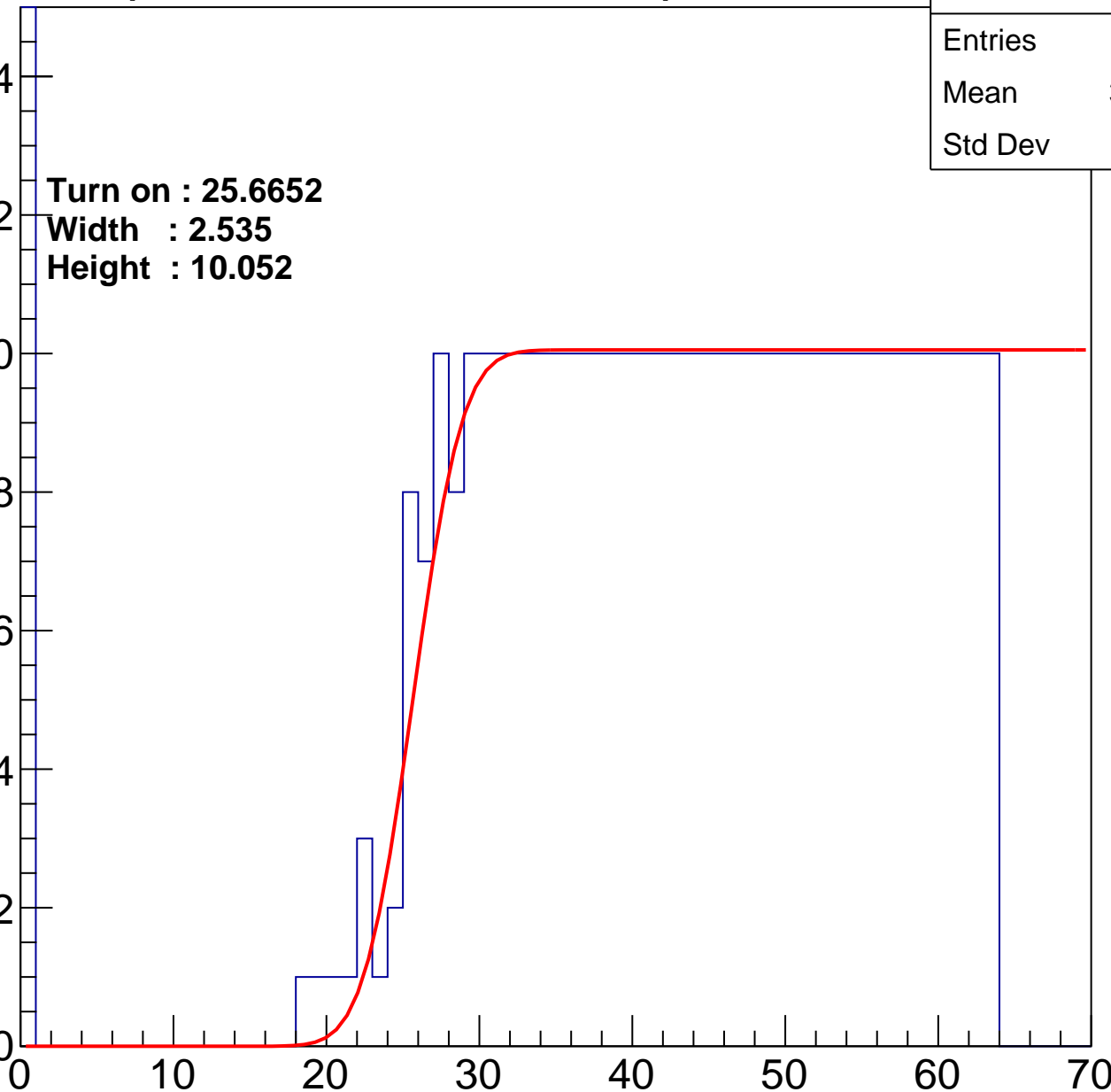
Width : 2.535

Height : 10.052

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch76

calib_packv5_041523_1651.root, FC#0, port C2

Entries	444
Mean	38.45
Std Dev	18.06

Turn on : 24.9808

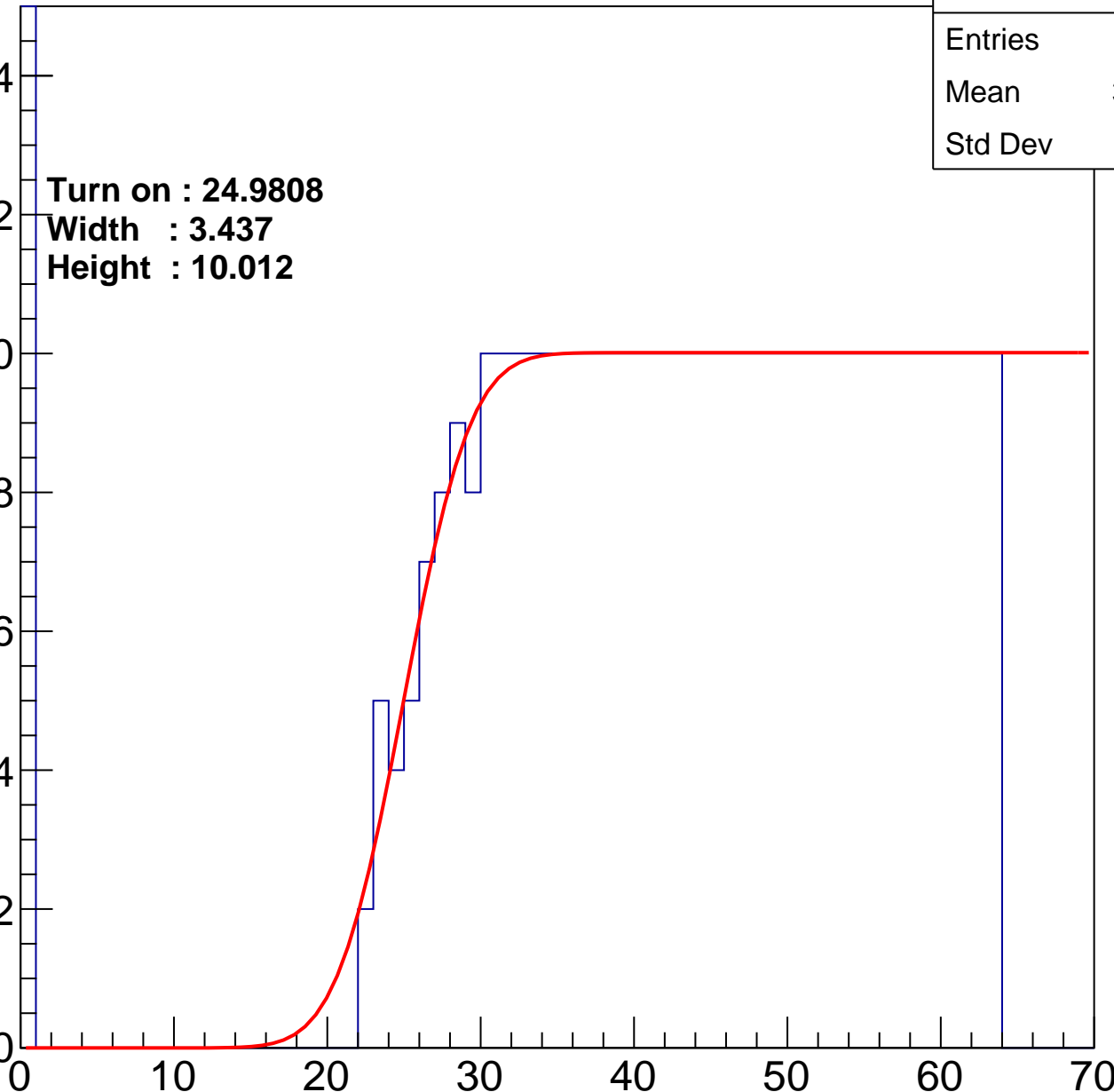
Width : 3.437

Height : 10.012

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch77

calib_packv5_041523_1651.root, FC#0, port C2

Entries	416
Mean	39.75
Std Dev	17.69

Turn on : 27.1993

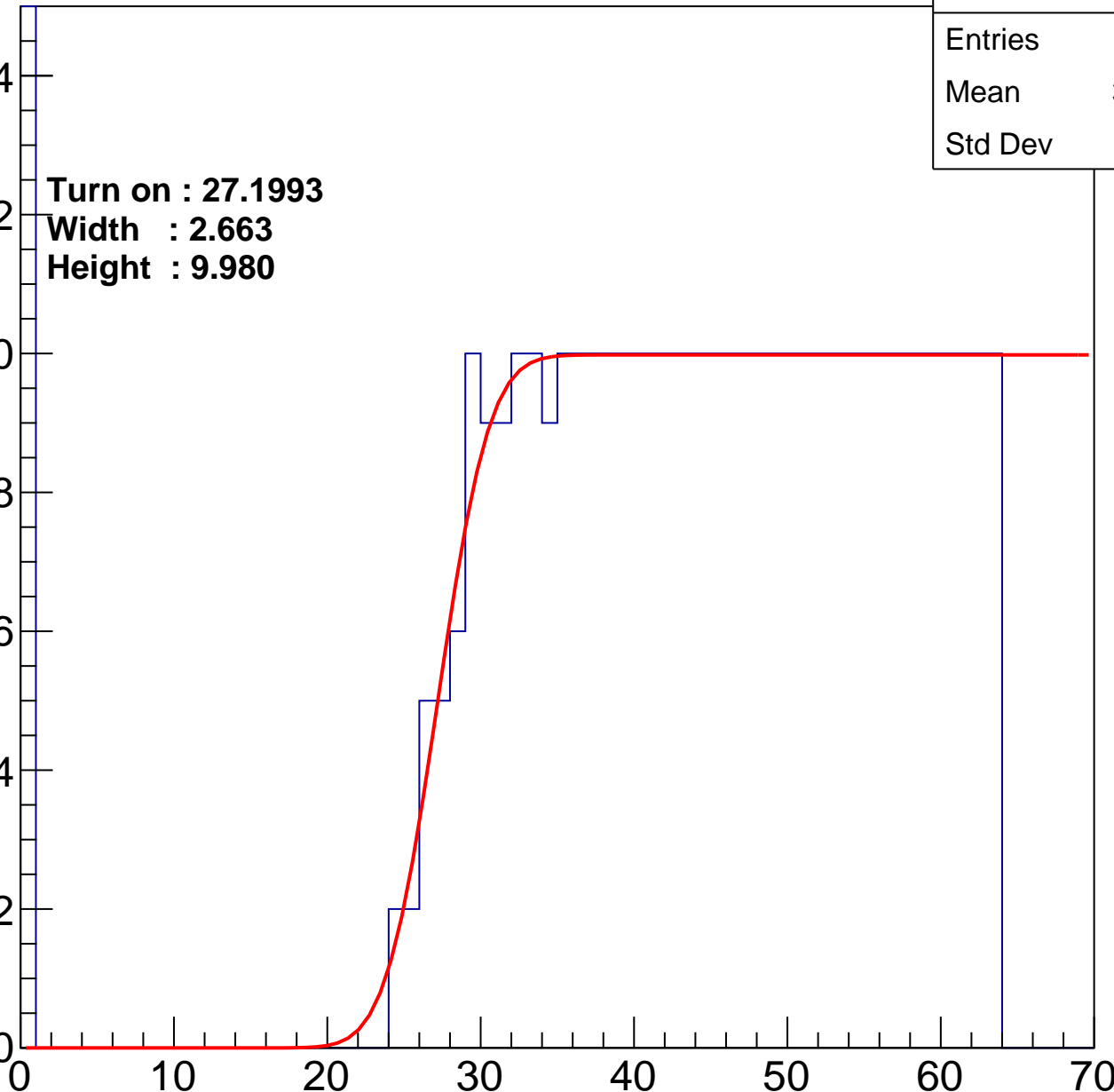
Width : 2.663

Height : 9.980

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch78

calib_packv5_041523_1651.root, FC#0, port C2

Entries	447
Mean	38.35
Std Dev	18.04

Turn on : 25.0761

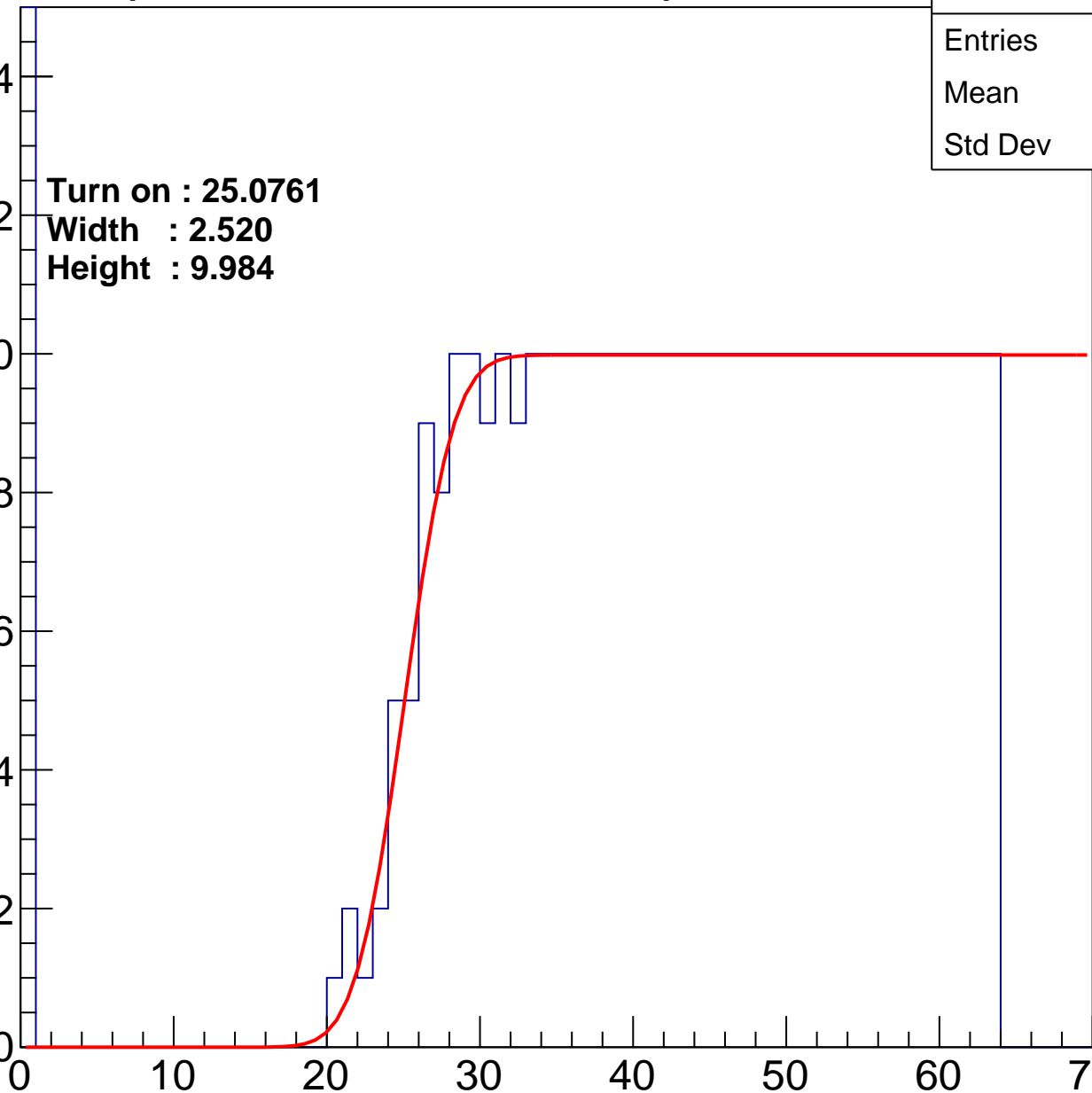
Width : 2.520

Height : 9.984

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch79

calib_packv5_041523_1651.root, FC#0, port C2

Entries	425
Mean	39.9
Std Dev	16.9

Turn on : 26.0832

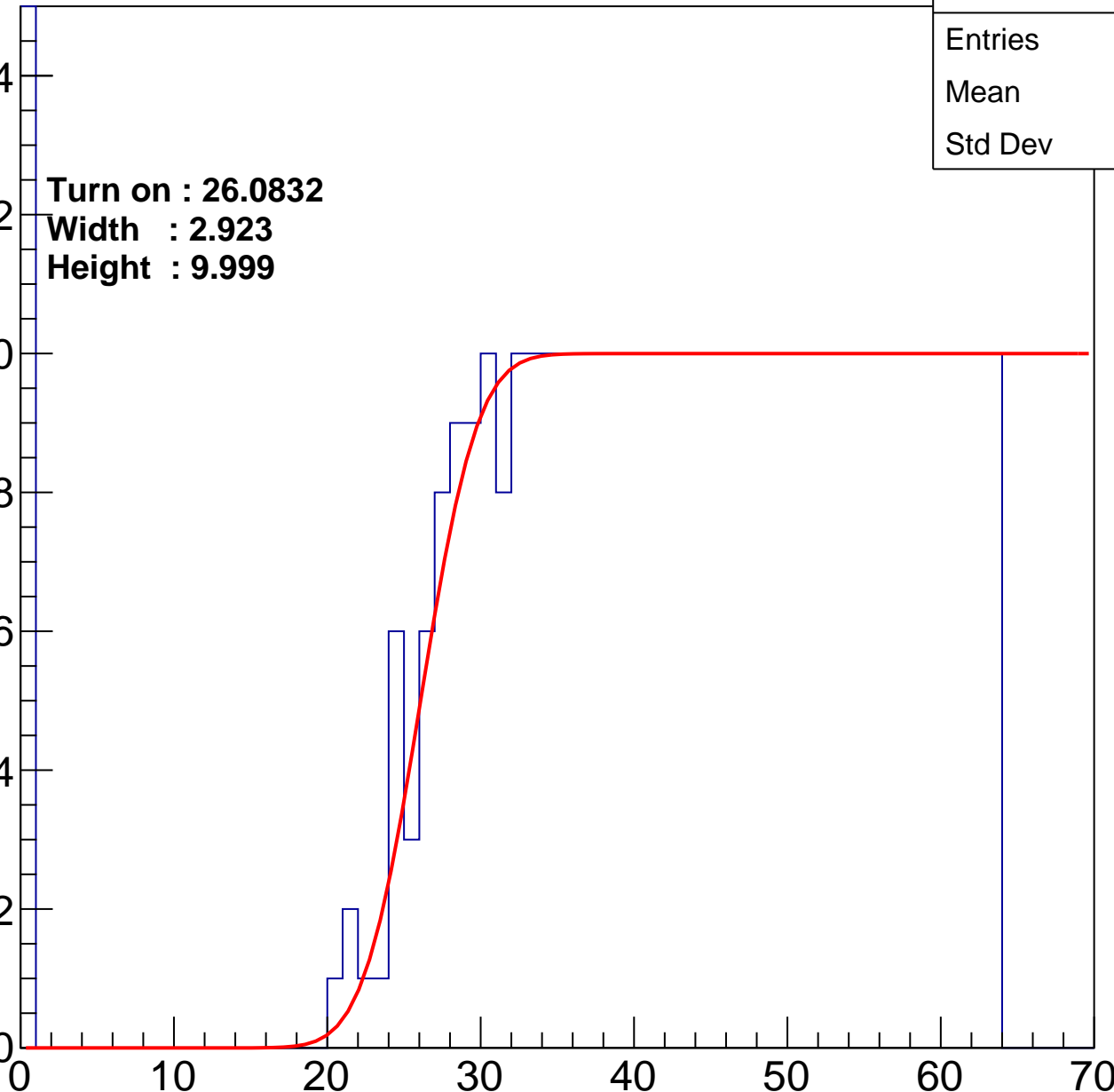
Width : 2.923

Height : 9.999

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch80

calib_packv5_041523_1651.root, FC#0, port C2

Entries	443
Mean	38.59
Std Dev	17.91

Turn on : 25.2080

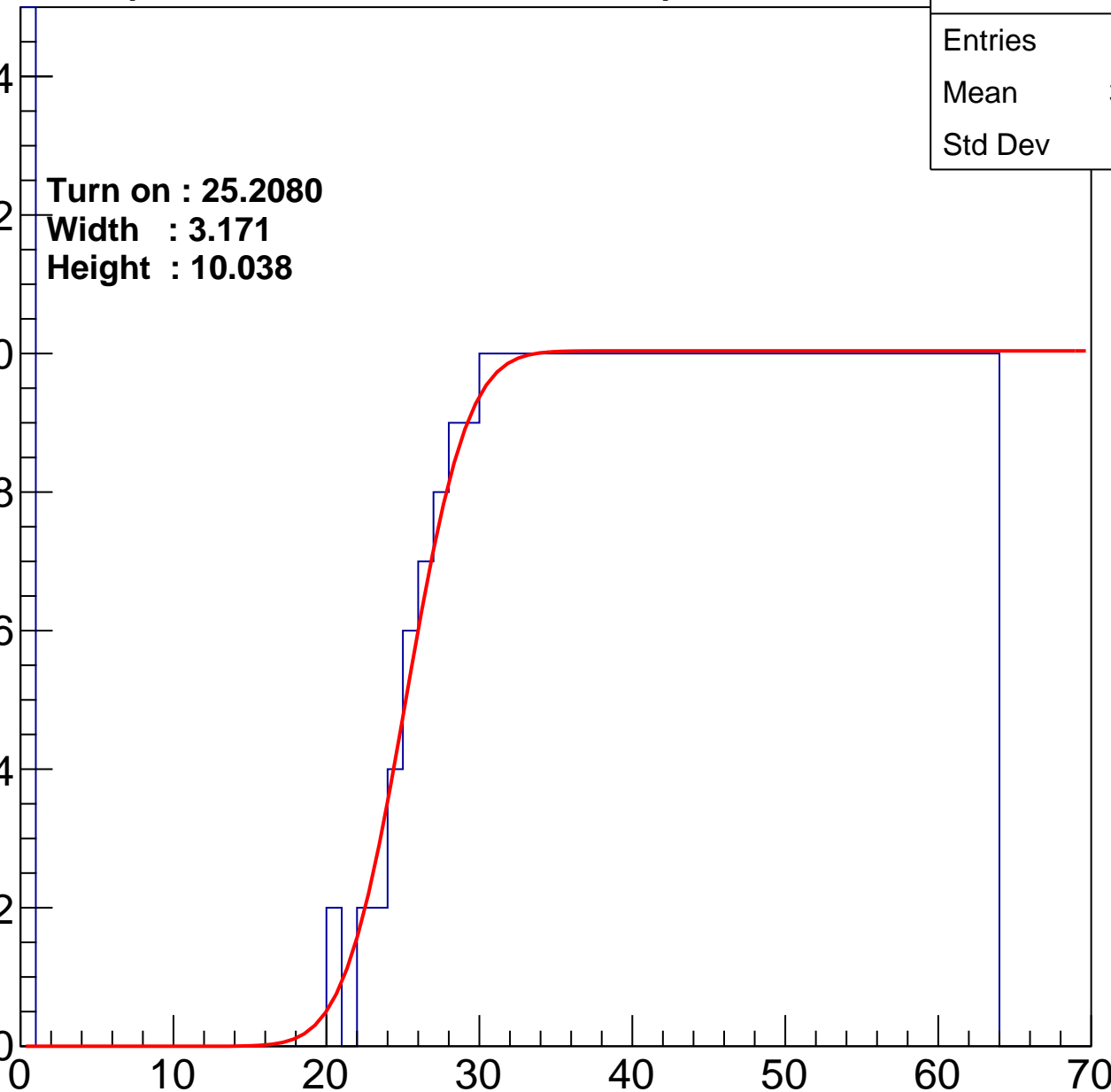
Width : 3.171

Height : 10.038

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch81

calib_packv5_041523_1651.root, FC#0, port C2

Entries	424
Mean	40.09
Std Dev	16.68

Turn on : 25.7840

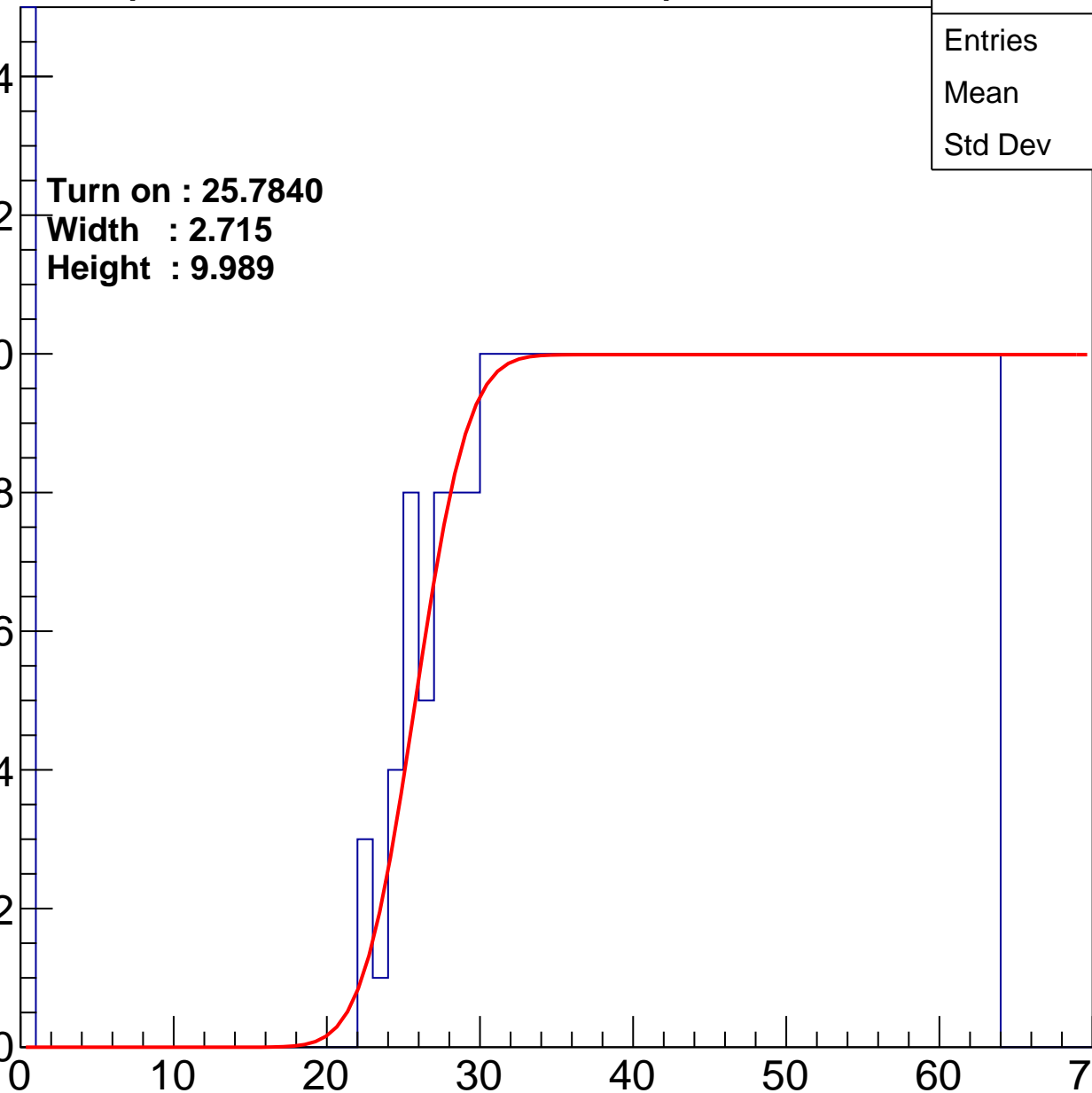
Width : 2.715

Height : 9.989

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch82

calib_packv5_041523_1651.root, FC#0, port C2

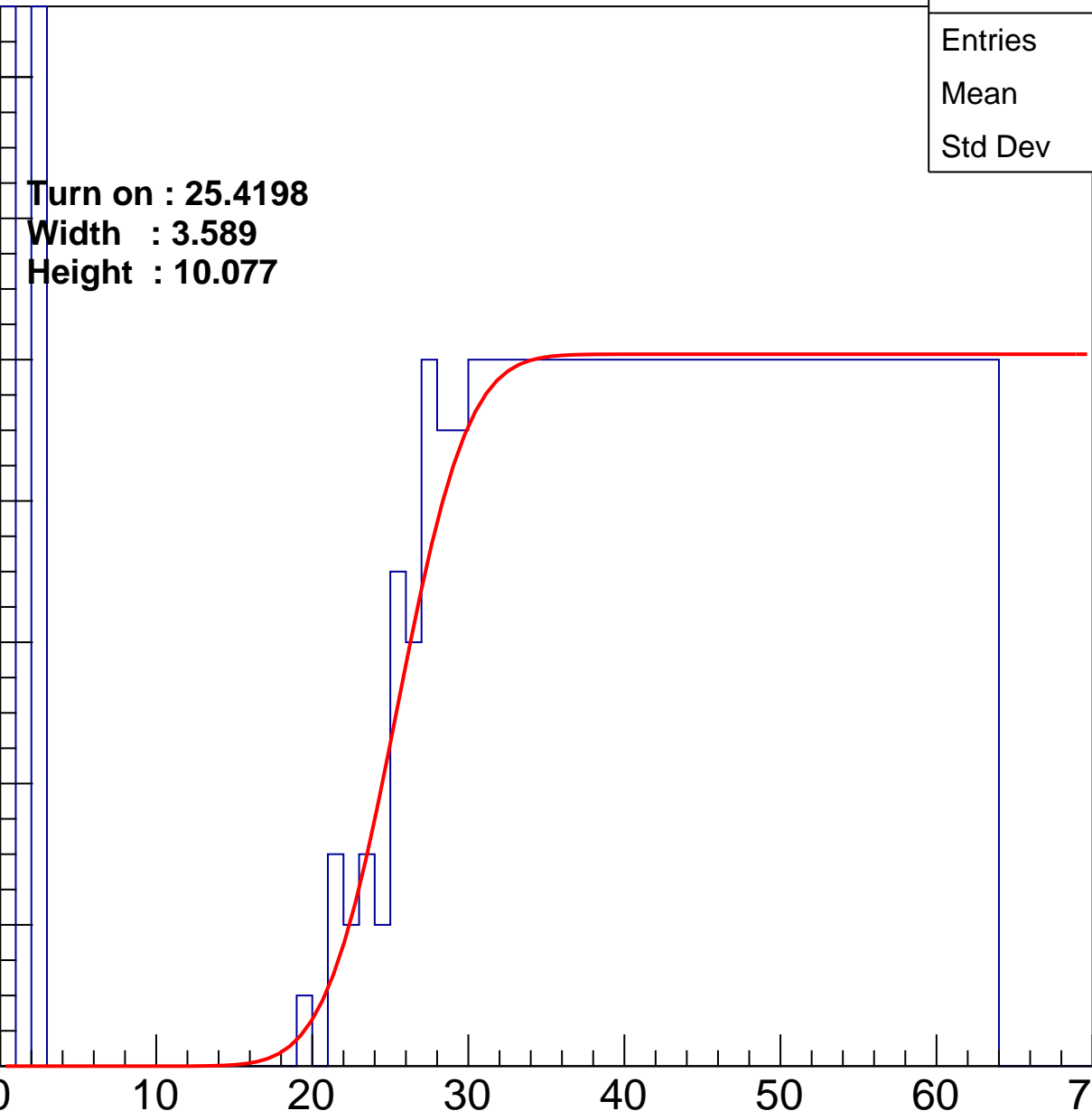
Entry

14
12
10
8
6
4
2
0

Turn on : 25.4198
Width : 3.589
Height : 10.077

Entries	502
Mean	34.44
Std Dev	20.37

ampl



B1L103S, U9-ch83

calib_packv5_041523_1651.root, FC#0, port C2

Entries	431
Mean	38.17
Std Dev	19.1

Turn on : 27.7201

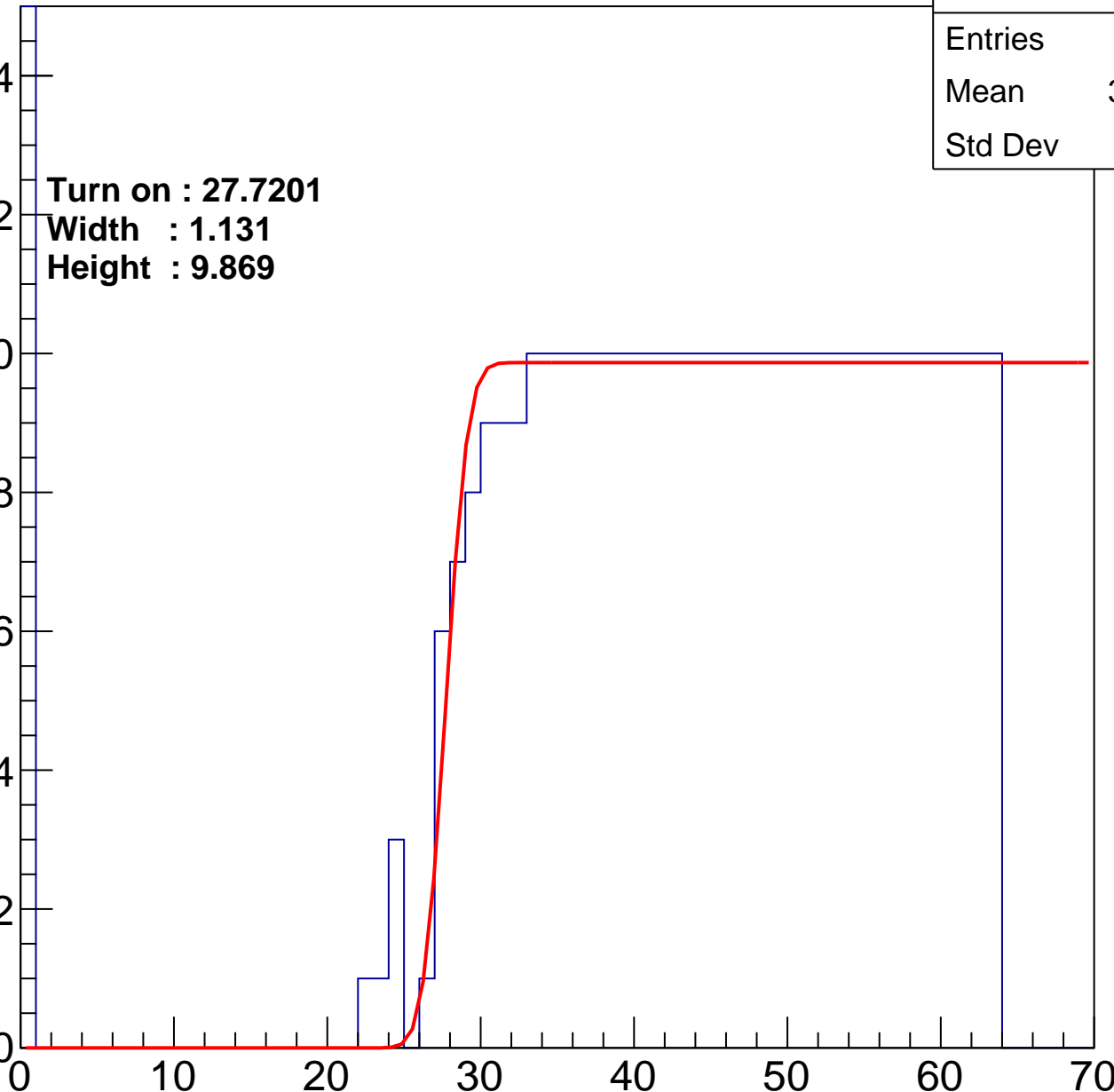
Width : 1.131

Height : 9.869

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch84

calib_packv5_041523_1651.root, FC#0, port C2

Entries	448
Mean	38.73
Std Dev	17.41

Turn on : 24.0325

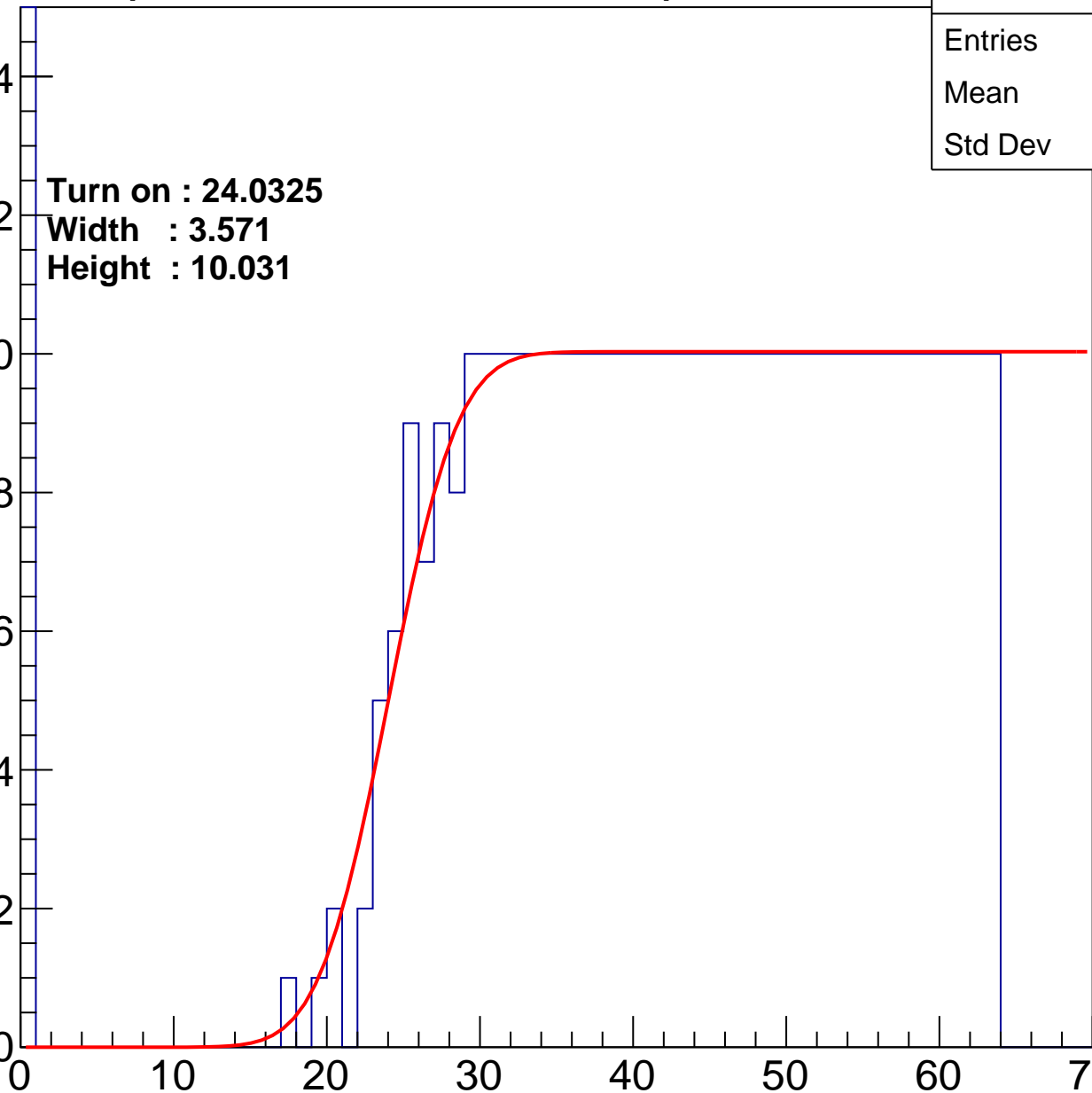
Width : 3.571

Height : 10.031

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch85

calib_packv5_041523_1651.root, FC#0, port C2

Entries	426
Mean	39.83
Std Dev	17.02

Turn on : 26.2924

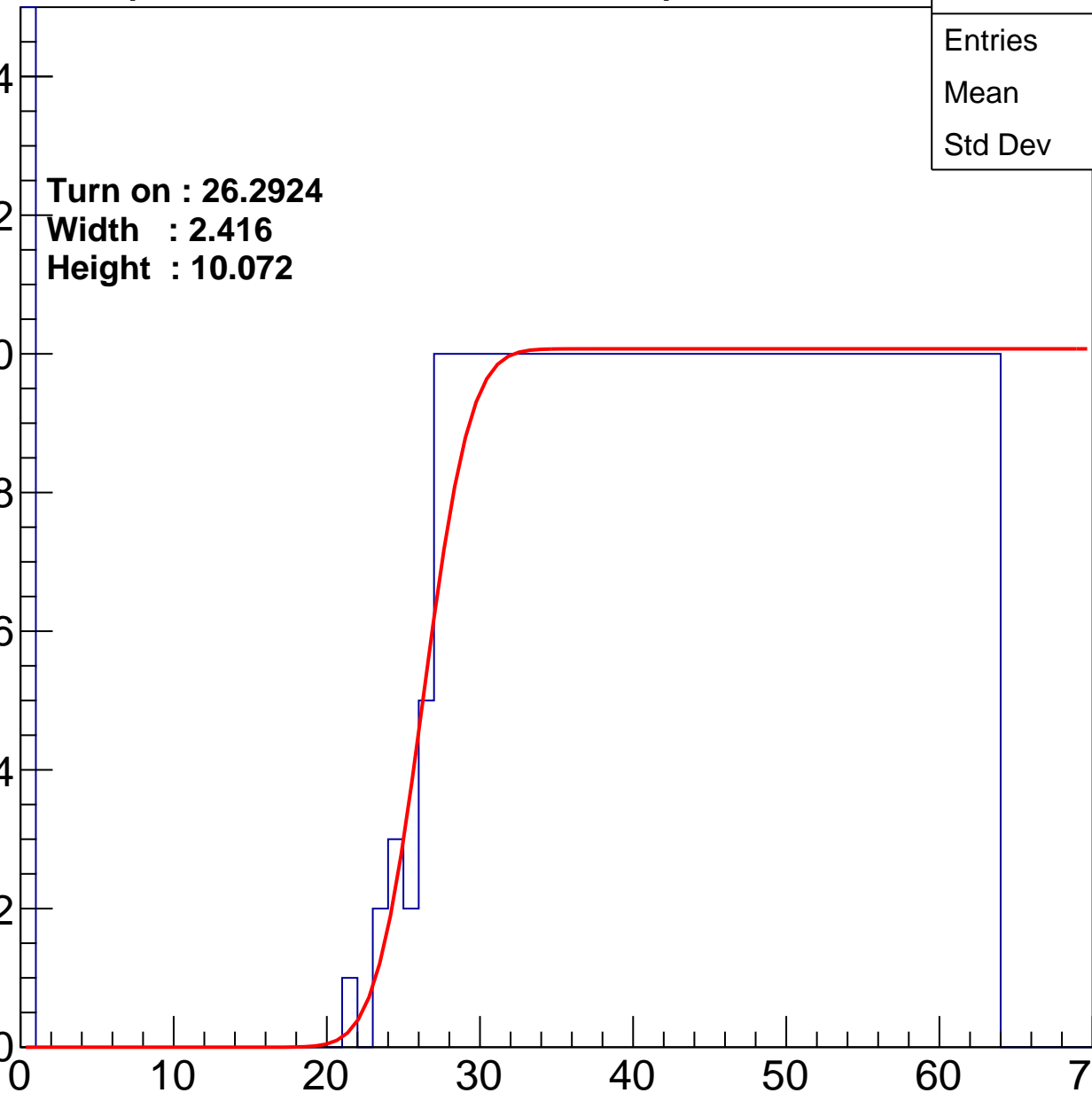
Width : 2.416

Height : 10.072

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch86

calib_packv5_041523_1651.root, FC#0, port C2

Entries	410
Mean	41.15
Std Dev	15.77

Turn on : 25.9042

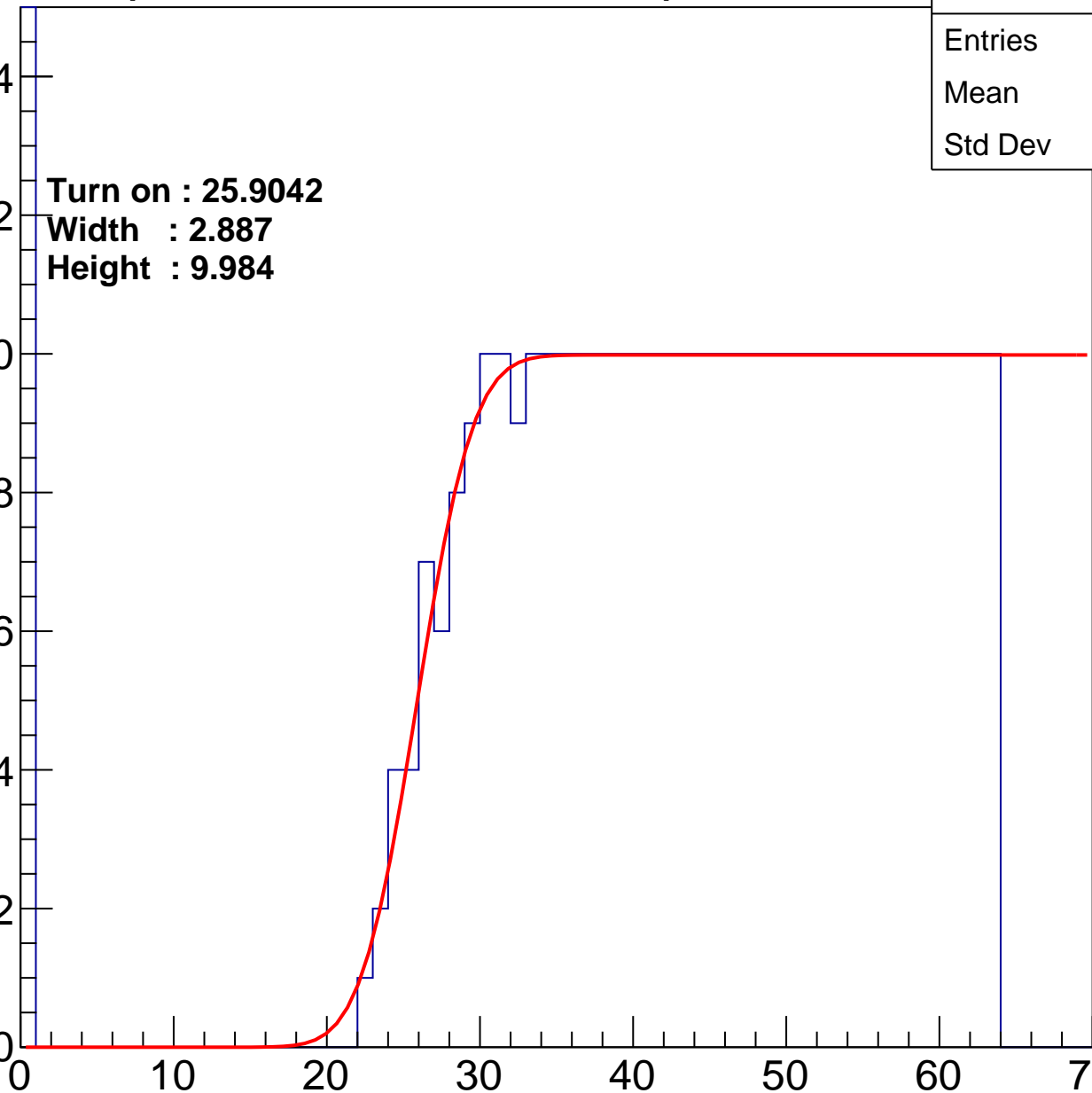
Width : 2.887

Height : 9.984

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch87

calib_packv5_041523_1651.root, FC#0, port C2

Entries	416
Mean	40.11
Std Dev	17.13

Turn on : 26.4169

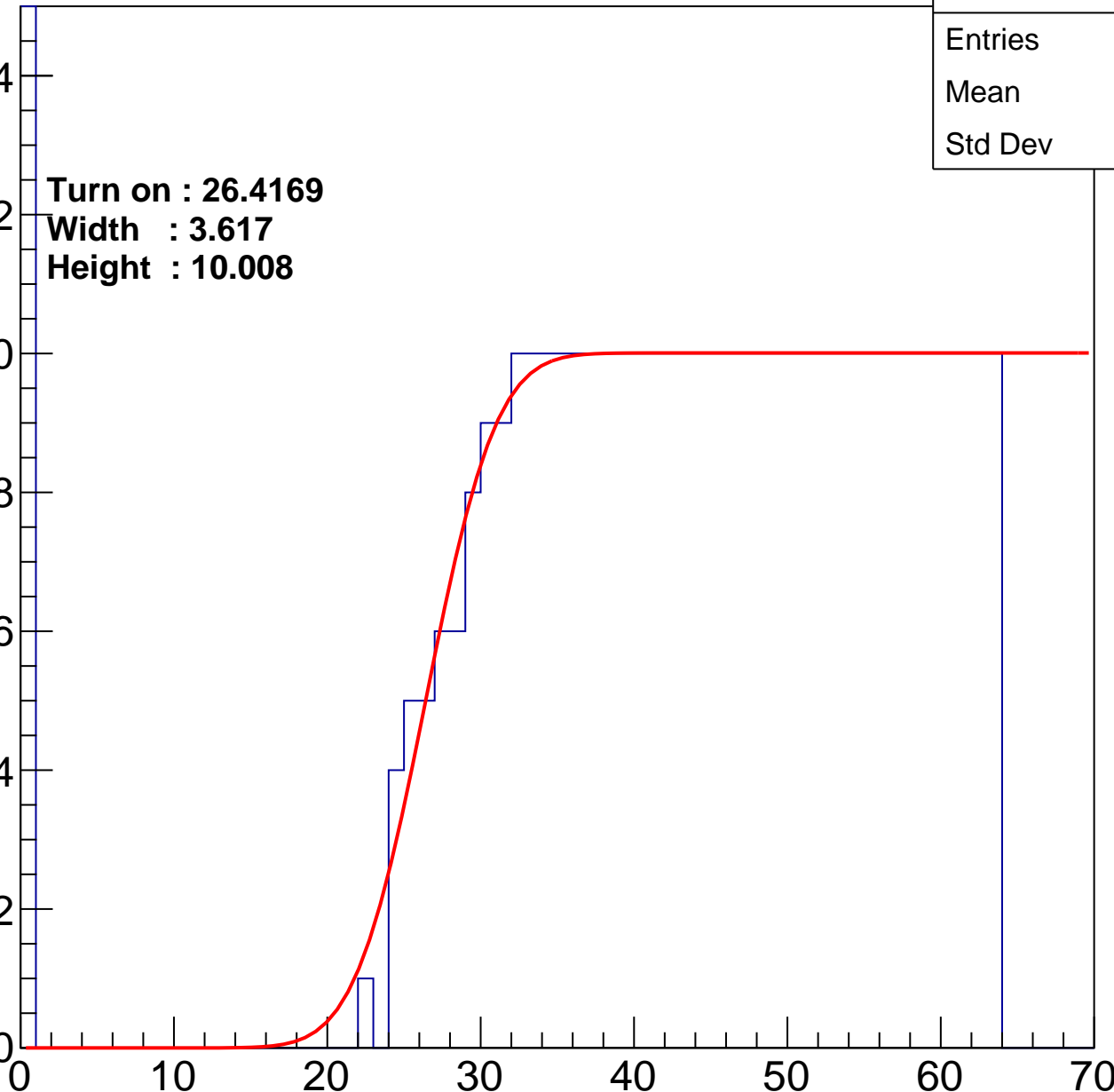
Width : 3.617

Height : 10.008

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch88

calib_packv5_041523_1651.root, FC#0, port C2

Entries	414
Mean	40.49
Std Dev	16.63

Turn on : 26.0626

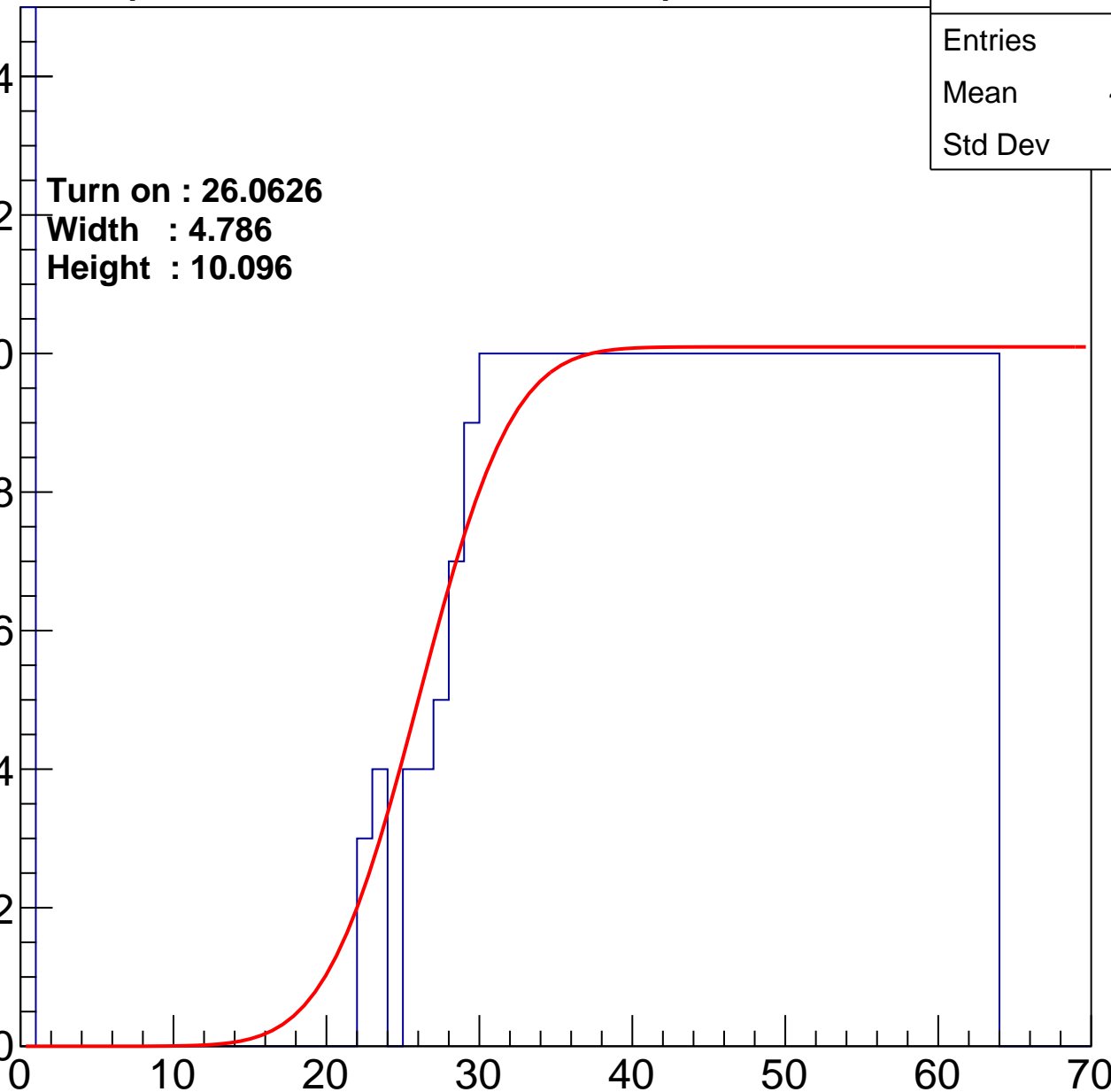
Width : 4.786

Height : 10.096

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch89

calib_packv5_041523_1651.root, FC#0, port C2

Entries	431
Mean	40.4
Std Dev	15.69

Turn on : 23.0264

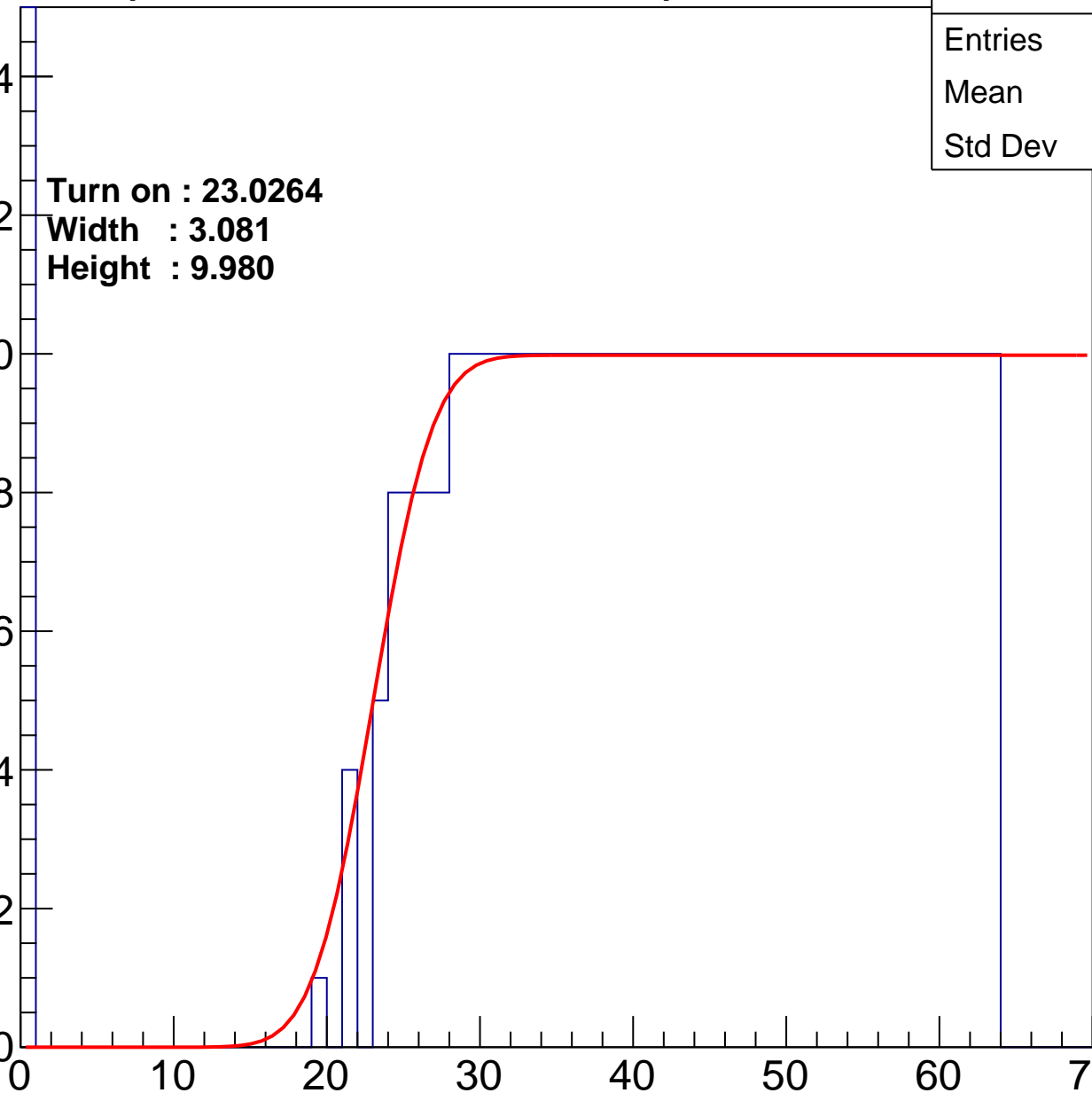
Width : 3.081

Height : 9.980

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch90

calib_packv5_041523_1651.root, FC#0, port C2

Entries	422
Mean	39.77
Std Dev	17.3

Turn on : 26.9623

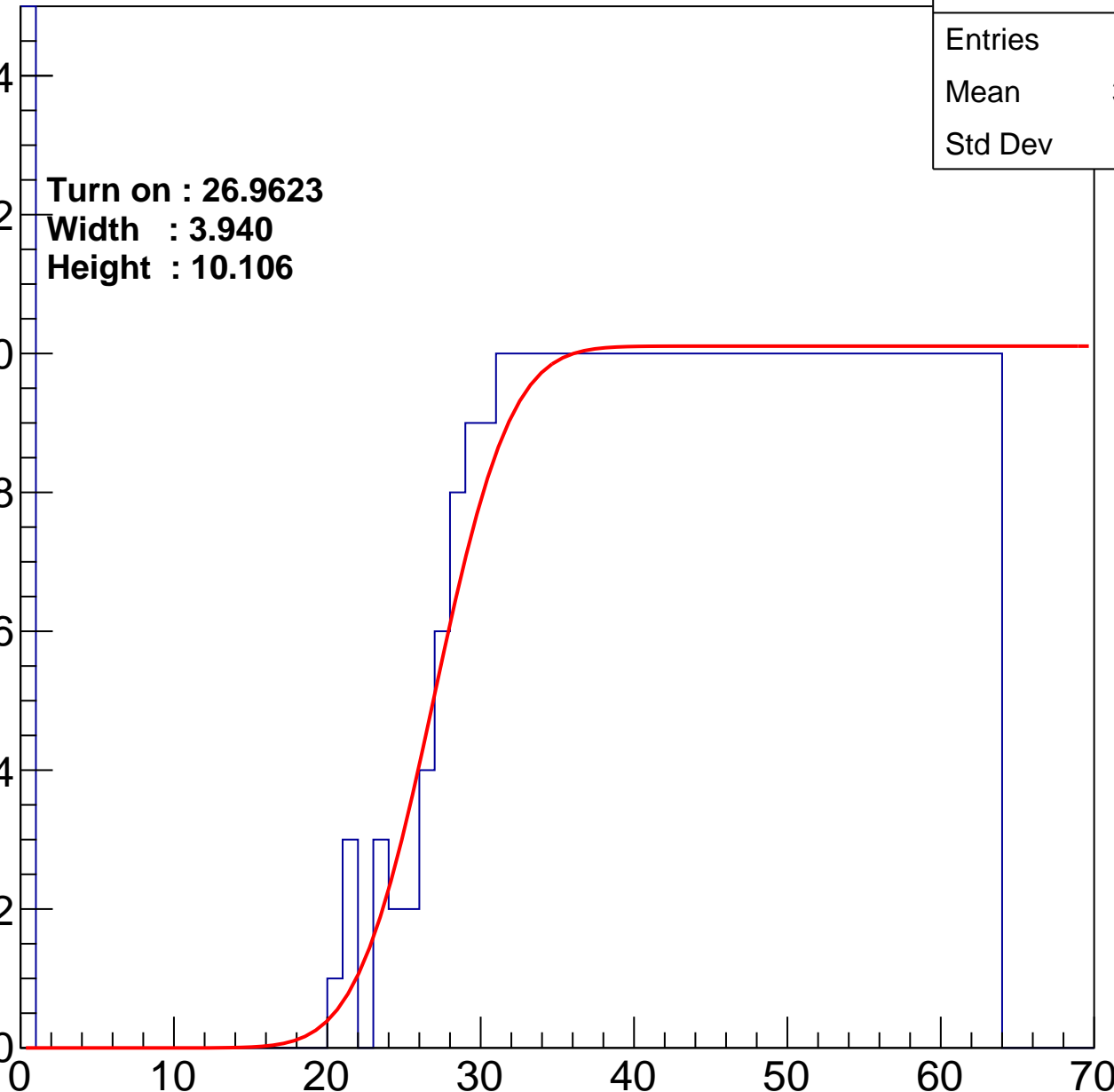
Width : 3.940

Height : 10.106

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch91

calib_packv5_041523_1651.root, FC#0, port C2

Entries	429
Mean	39.17
Std Dev	17.83

Turn on : 25.0675

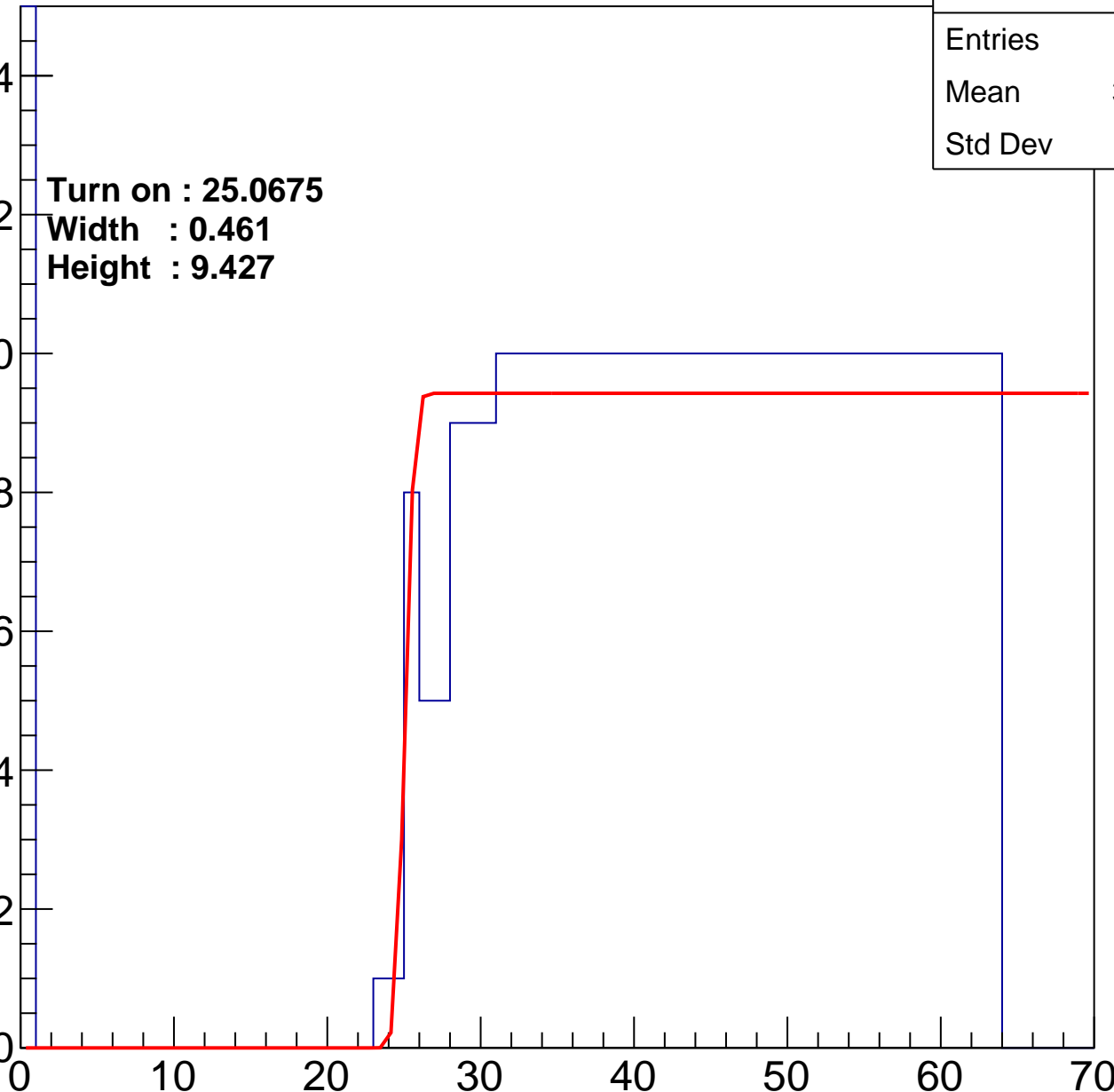
Width : 0.461

Height : 9.427

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch92

calib_packv5_041523_1651.root, FC#0, port C2

Entries	459
Mean	37.77
Std Dev	18.22

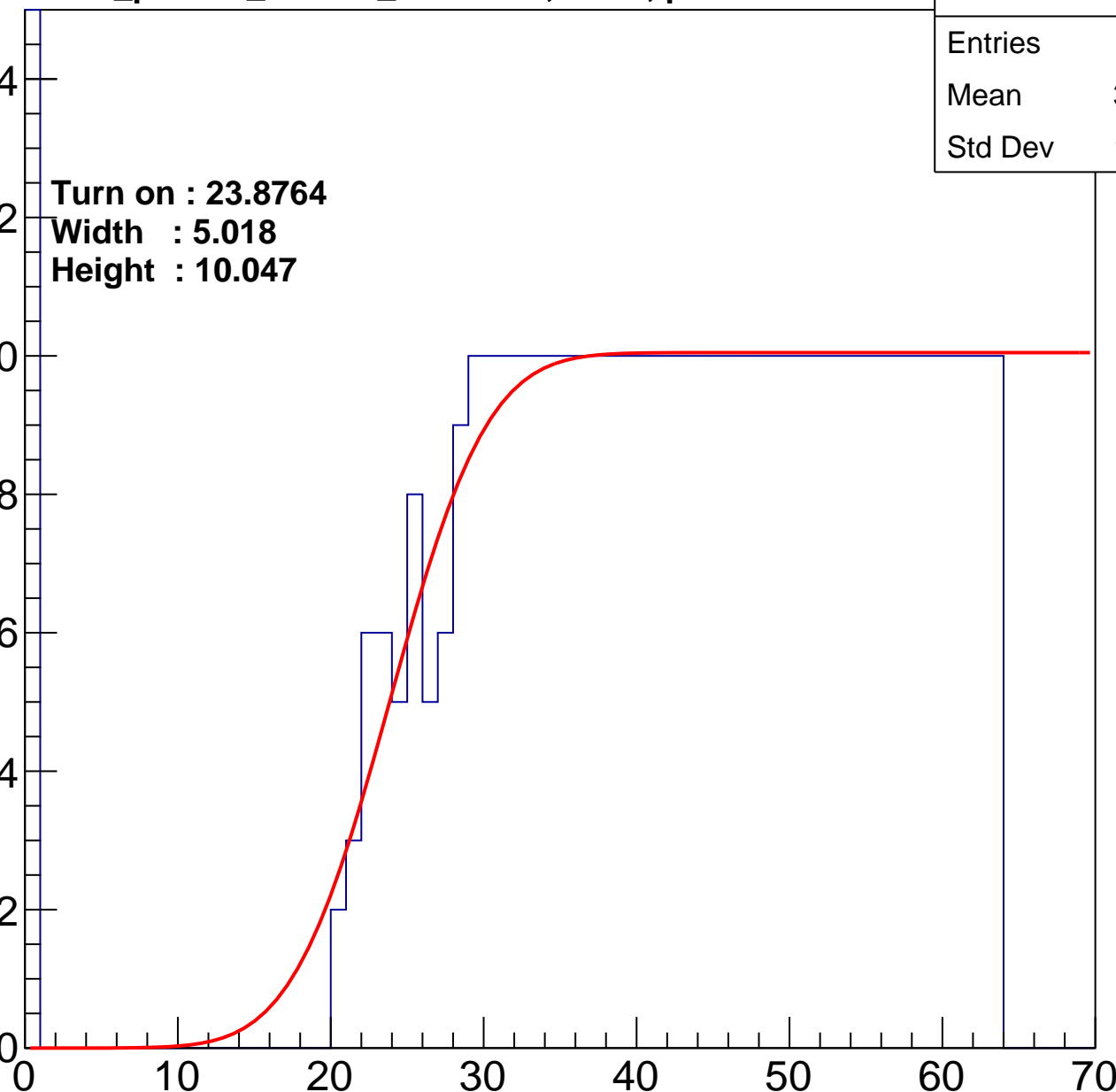
Turn on : 23.8764

Width : 5.018

Height : 10.047

Entry

14
12
10
8
6
4
2
0



ampl

B1L103S, U9-ch93

calib_packv5_041523_1651.root, FC#0, port C2

Entries	427
Mean	39.8
Std Dev	16.97

Turn on : 25.8466

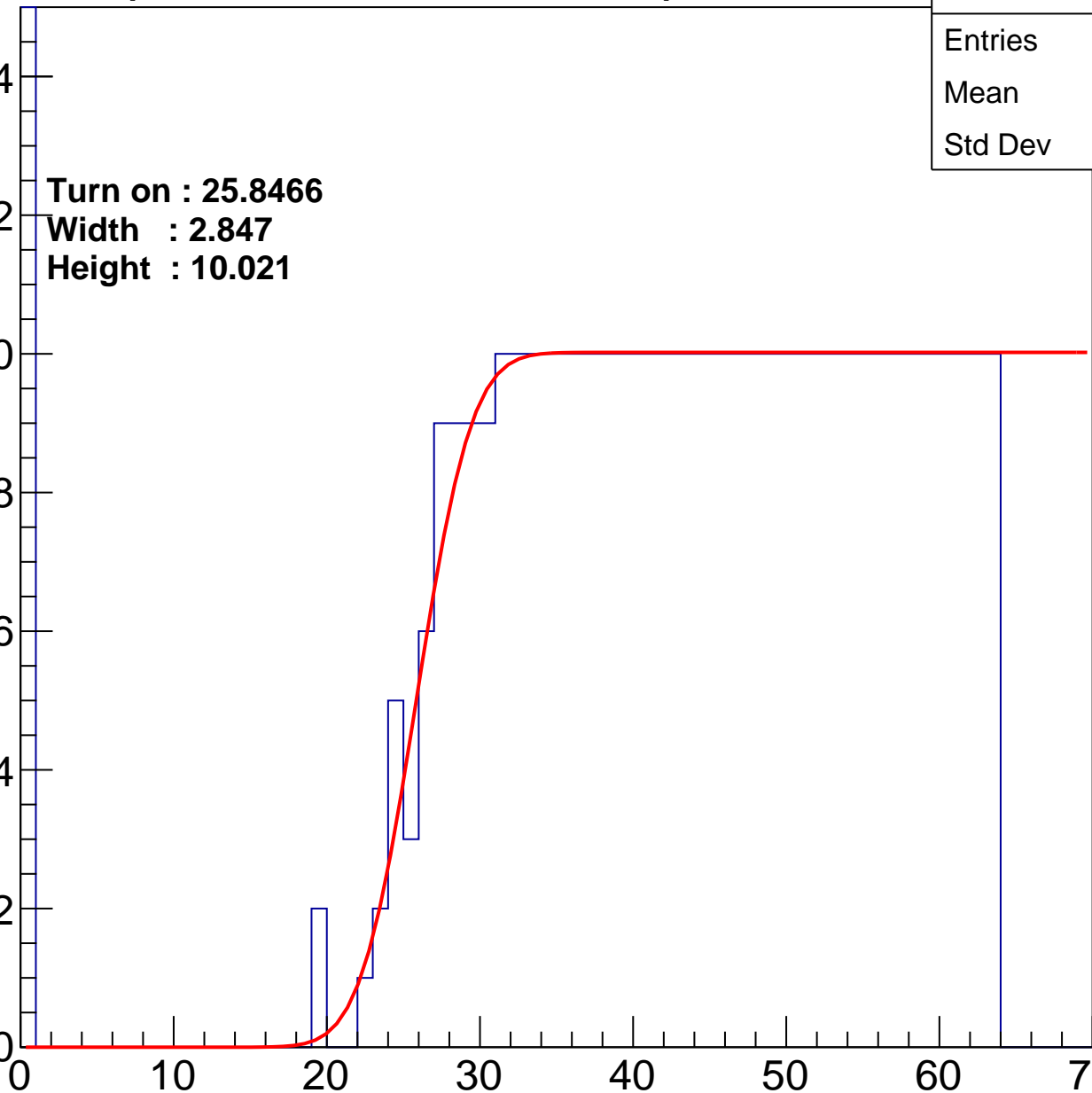
Width : 2.847

Height : 10.021

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch94

calib_packv5_041523_1651.root, FC#0, port C2

Entries	451
Mean	37.9
Std Dev	18.48

Turn on : 25.2338

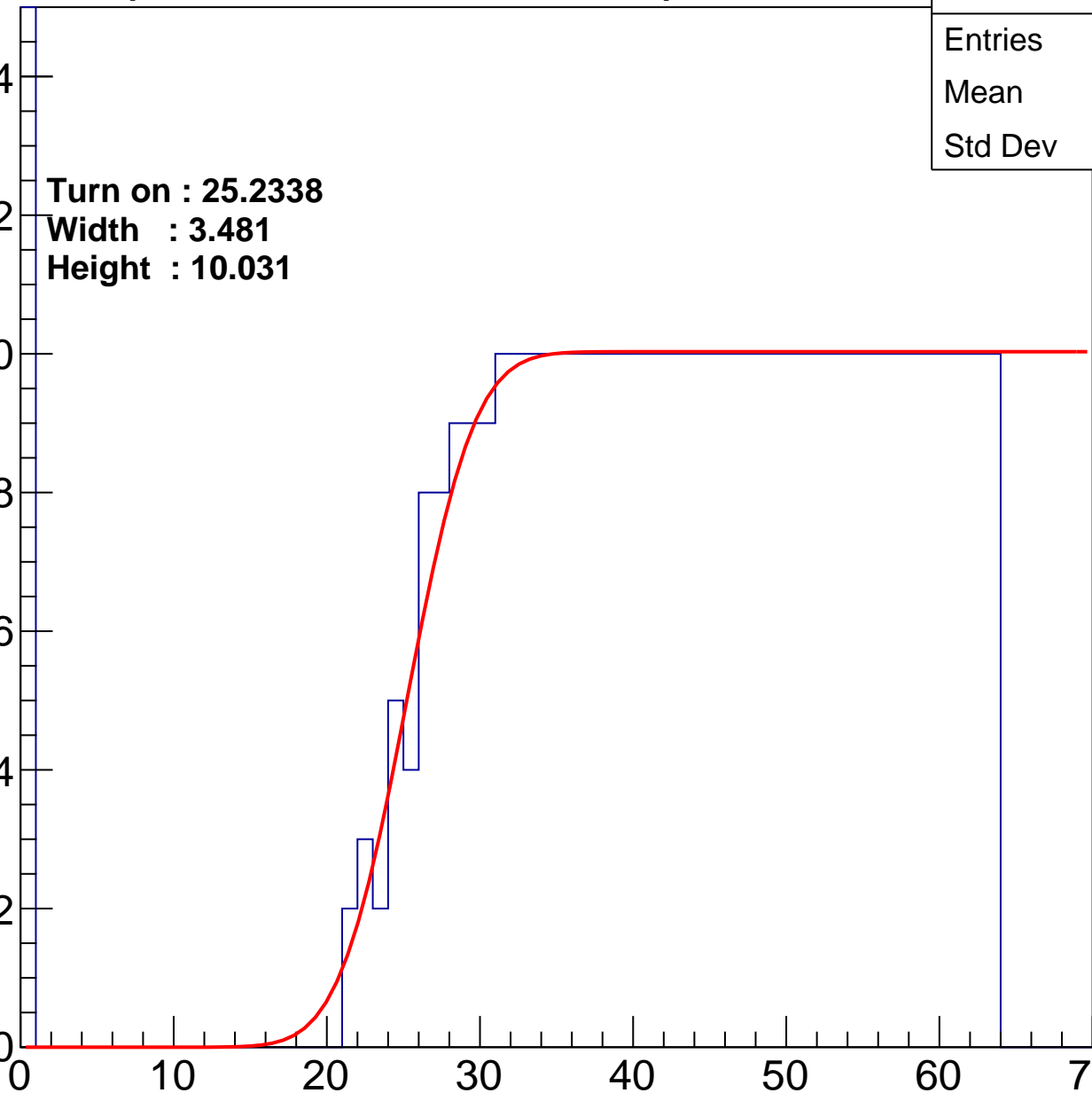
Width : 3.481

Height : 10.031

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch95

calib_packv5_041523_1651.root, FC#0, port C2

Entries	409
Mean	40.83
Std Dev	16.41

Turn on : 26.9493

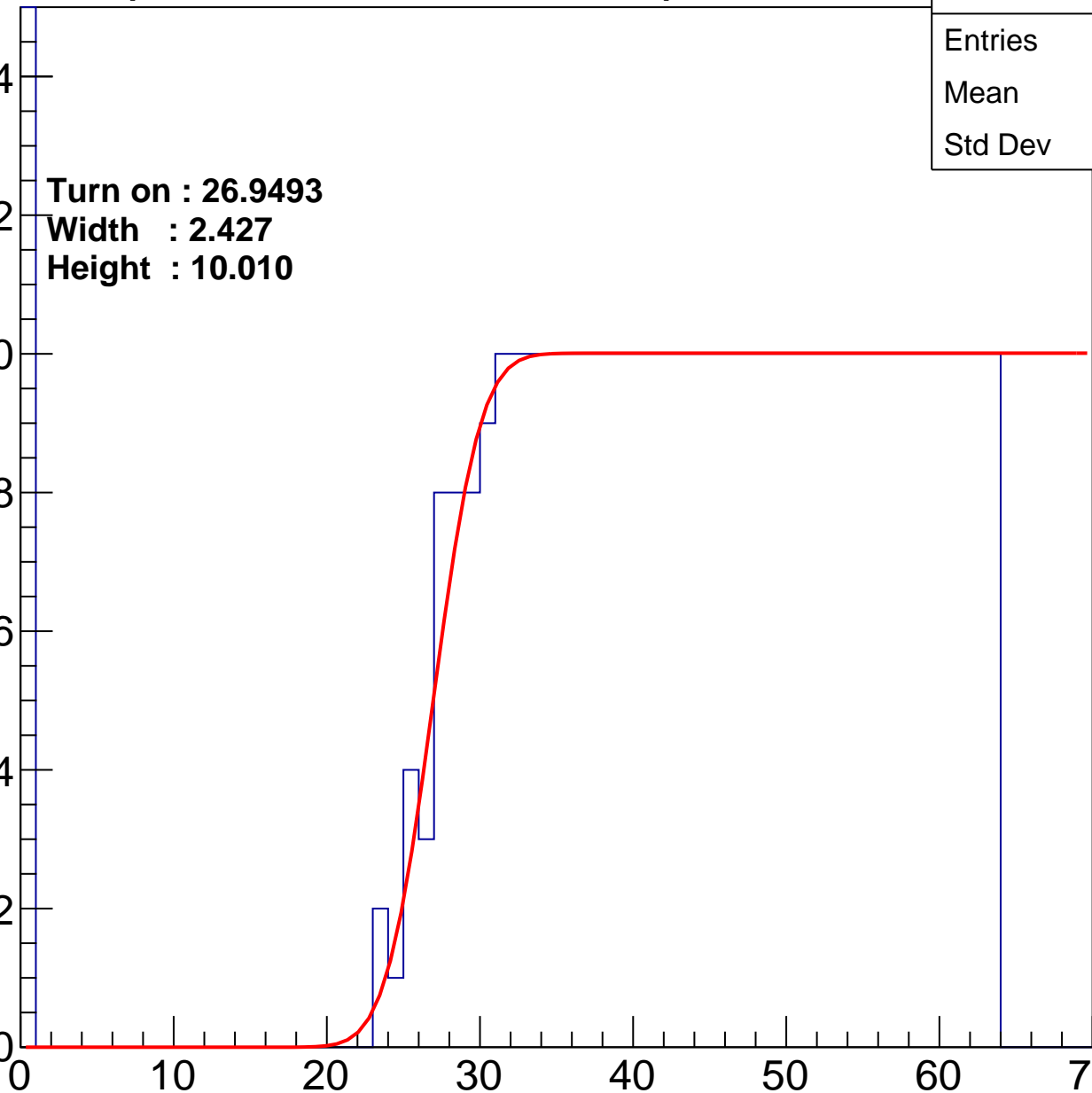
Width : 2.427

Height : 10.010

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch96

calib_packv5_041523_1651.root, FC#0, port C2

Entries	433
Mean	39.1
Std Dev	17.68

Turn on : 26.3003

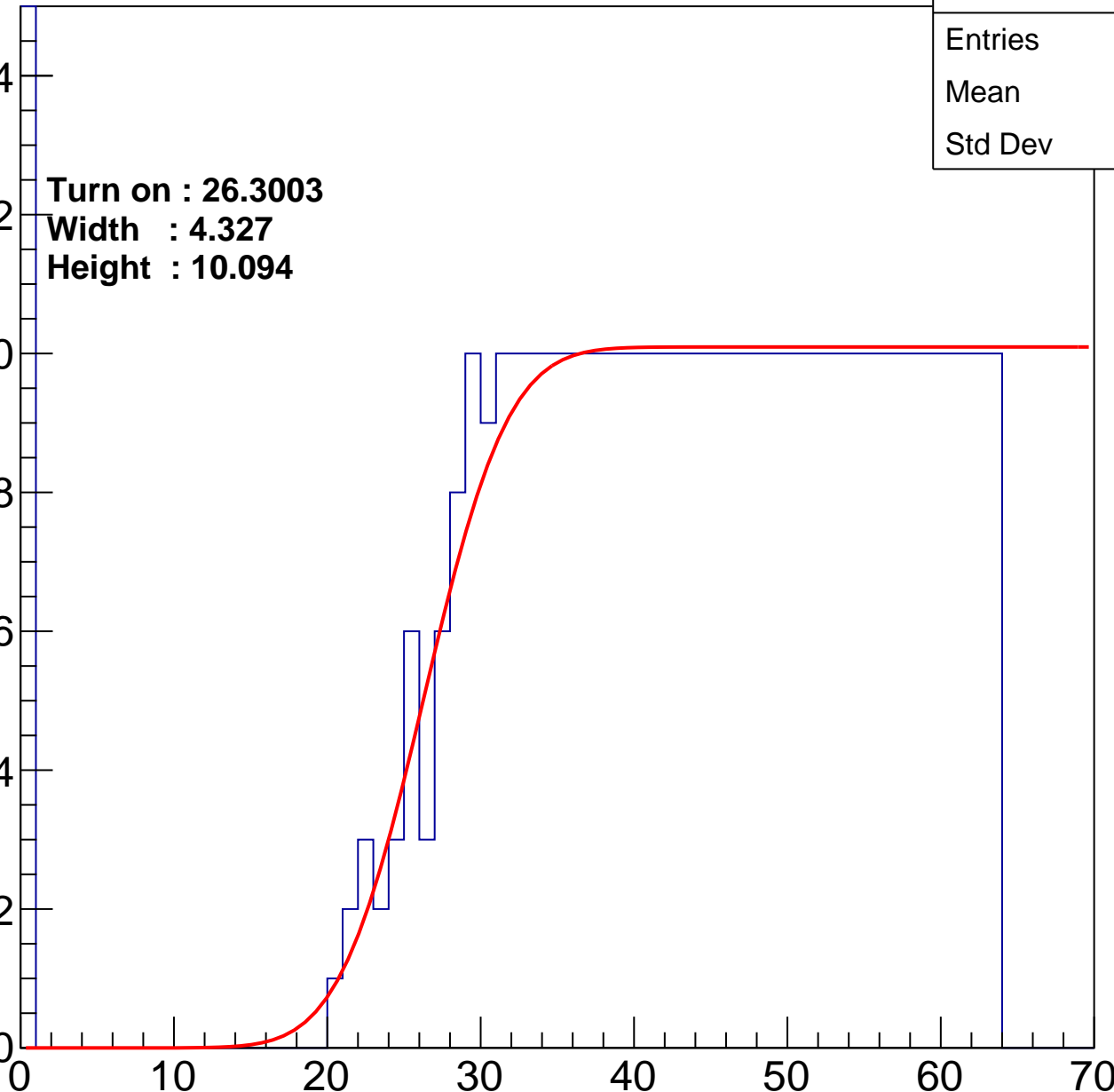
Width : 4.327

Height : 10.094

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch97

calib_packv5_041523_1651.root, FC#0, port C2

Entries	431
Mean	39.88
Std Dev	16.59

Turn on : 25.1379

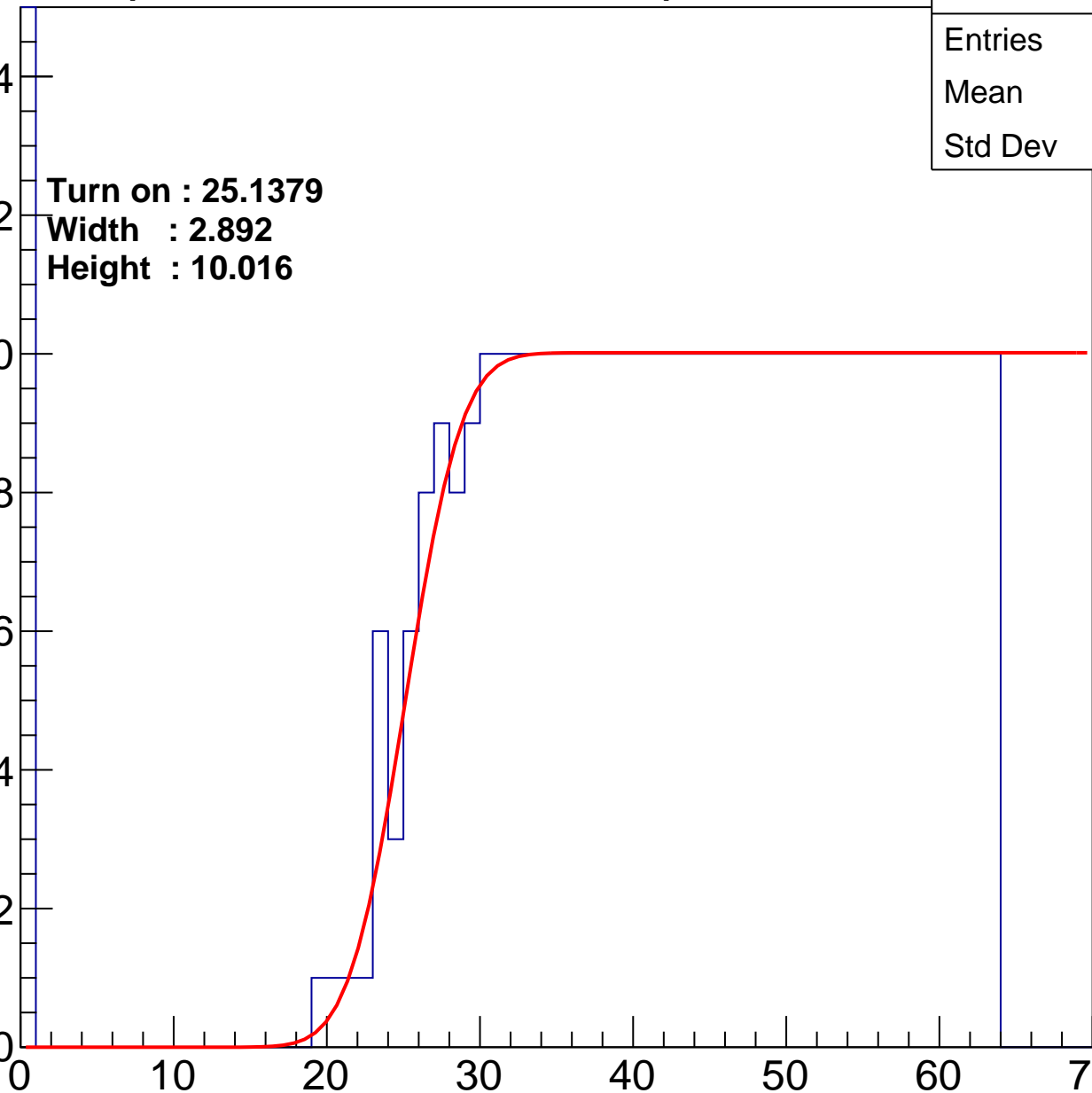
Width : 2.892

Height : 10.016

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch98

calib_packv5_041523_1651.root, FC#0, port C2

Entries	432
Mean	40.22
Std Dev	15.97

Turn on : 24.6214

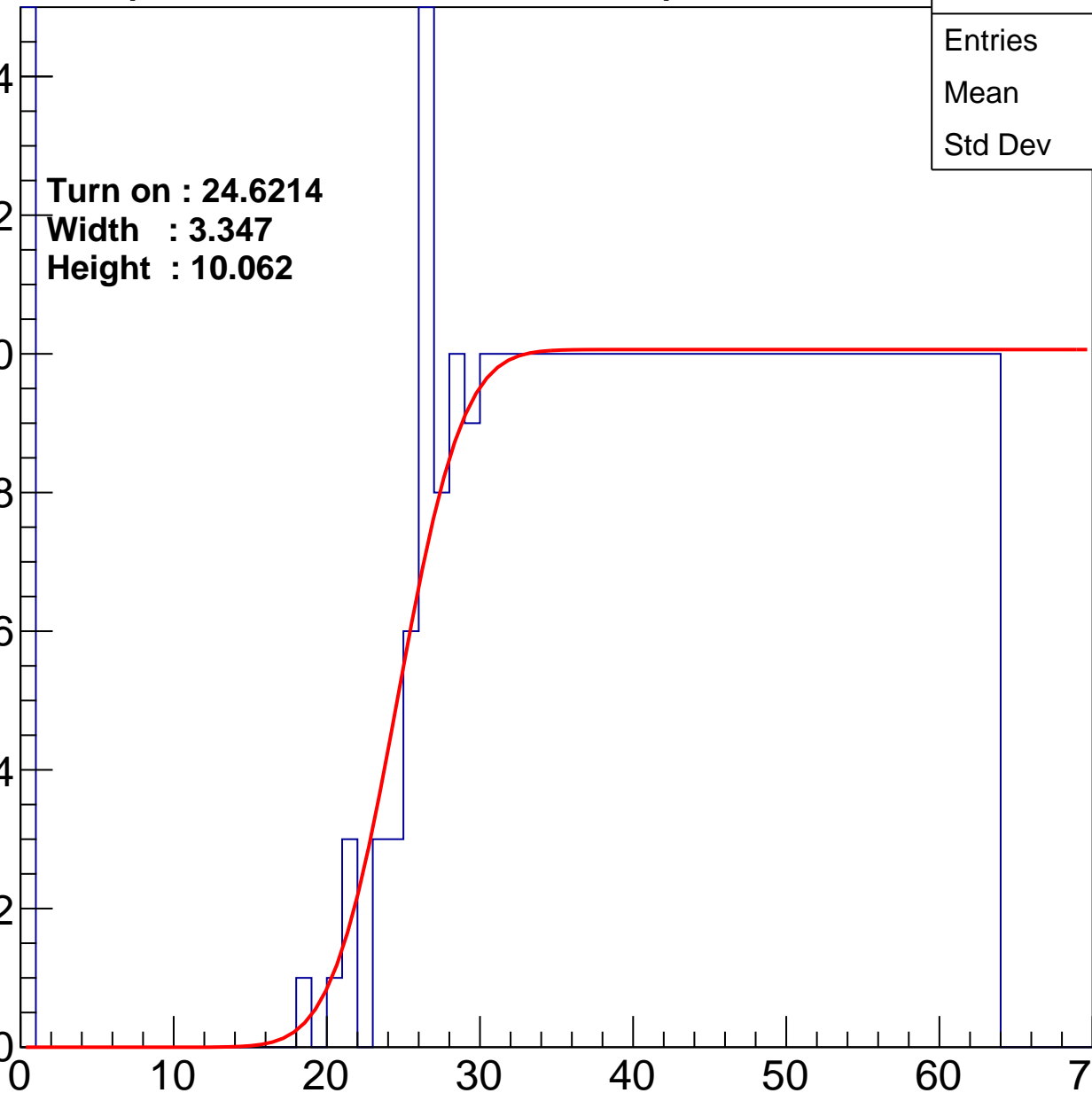
Width : 3.347

Height : 10.062

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch99

calib_packv5_041523_1651.root, FC#0, port C2

Entries	441
Mean	38.8
Std Dev	17.7

Turn on : 25.2130

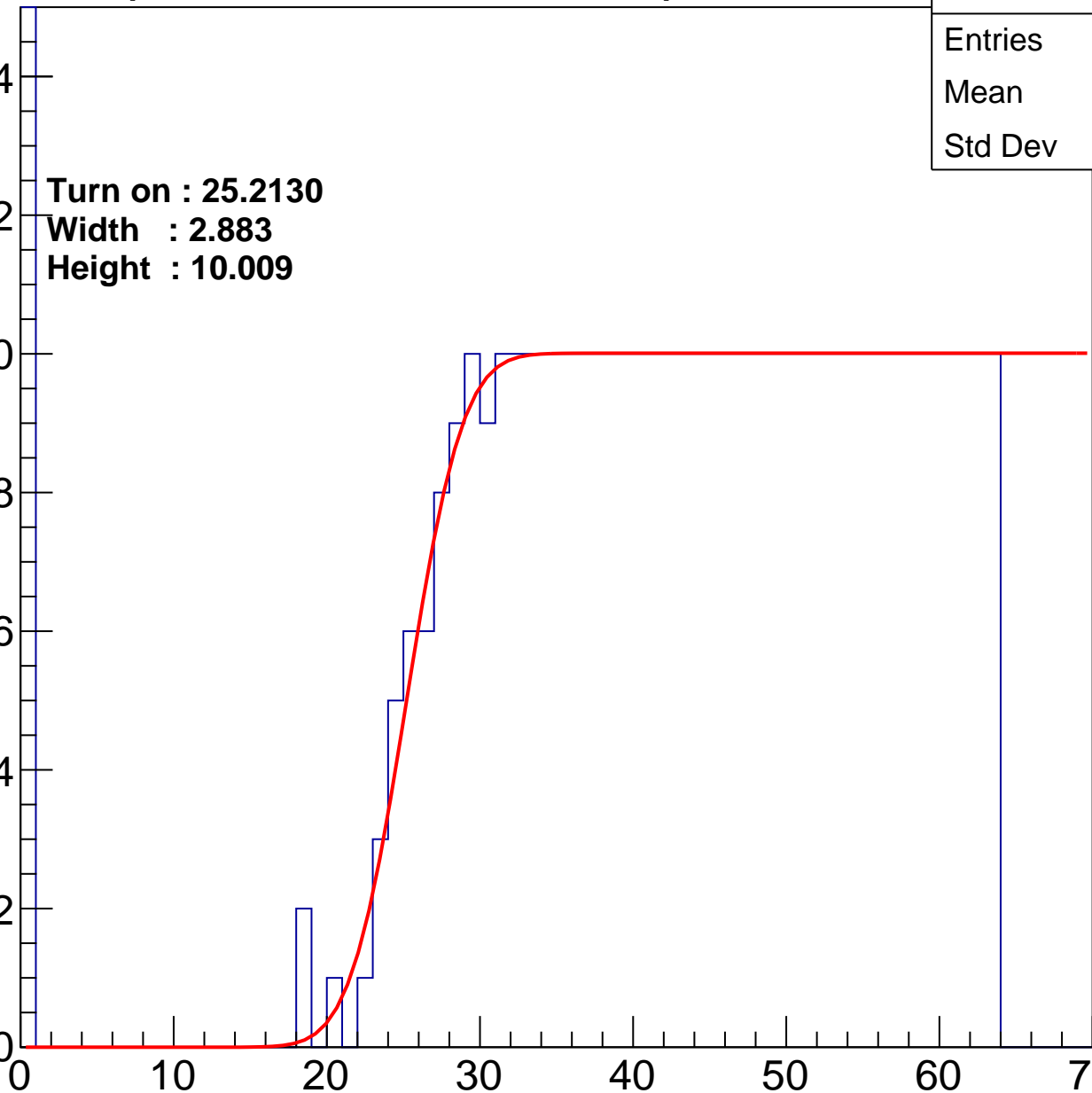
Width : 2.883

Height : 10.009

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch100

calib_packv5_041523_1651.root, FC#0, port C2

Entries	452
Mean	38.23
Std Dev	17.95

Turn on : 24.6398

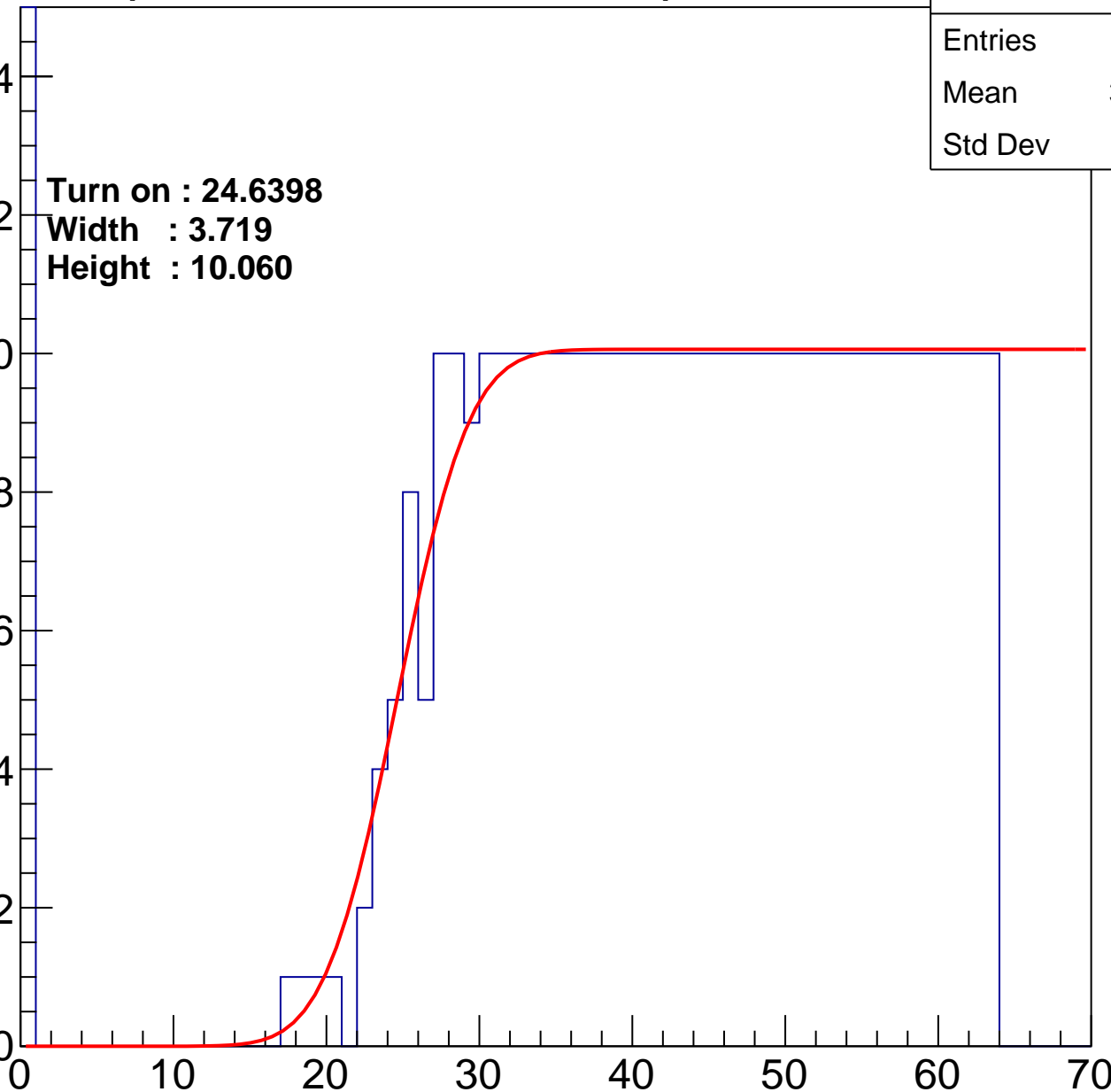
Width : 3.719

Height : 10.060

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch101

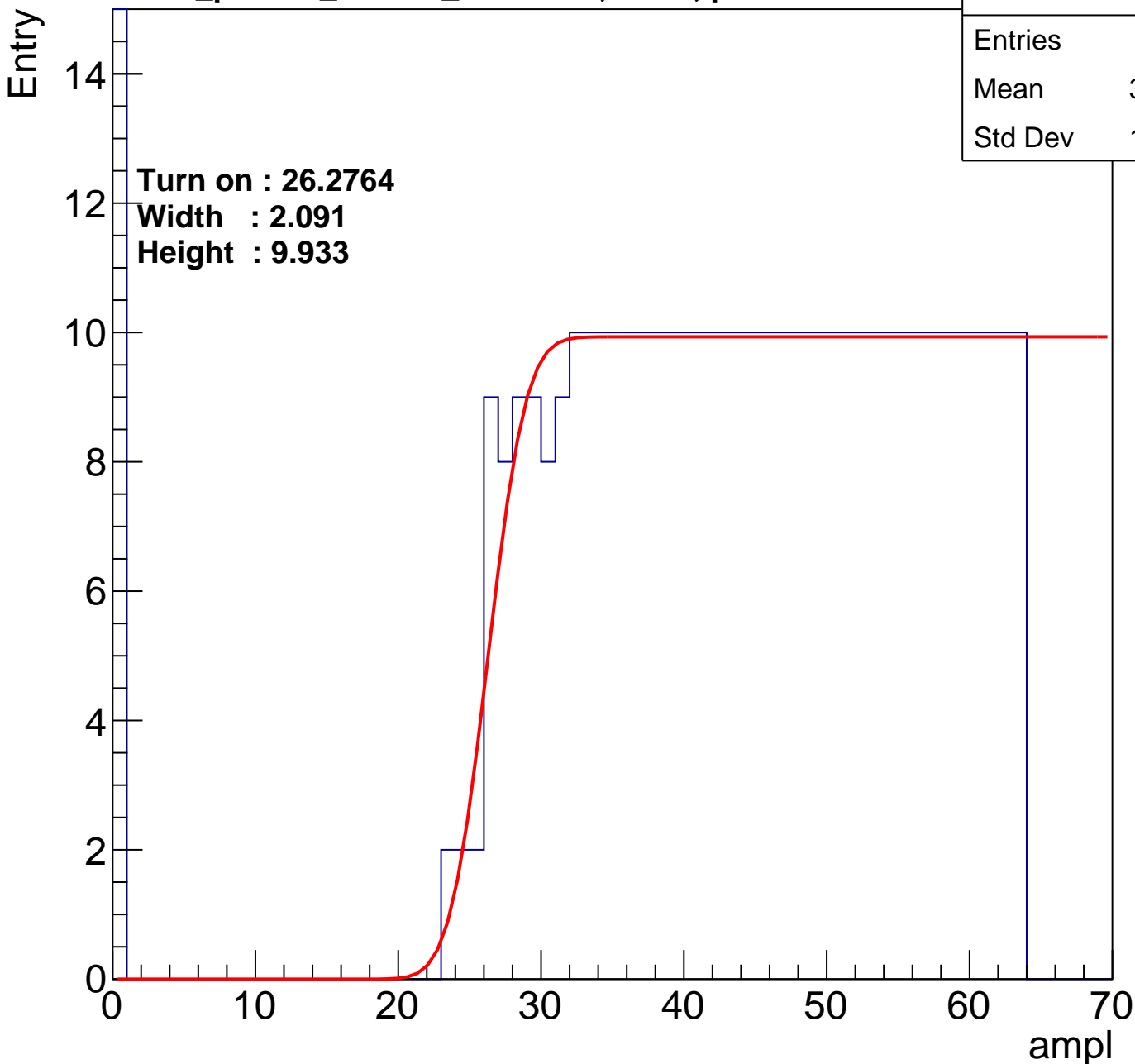
calib_packv5_041523_1651.root, FC#0, port C2

Entries	430
Mean	39.13
Std Dev	17.83

Turn on : 26.2764

Width : 2.091

Height : 9.933



B1L103S, U9-ch102

calib_packv5_041523_1651.root, FC#0, port C2

Entries	433
Mean	39.79
Std Dev	16.65

Turn on : 24.8012

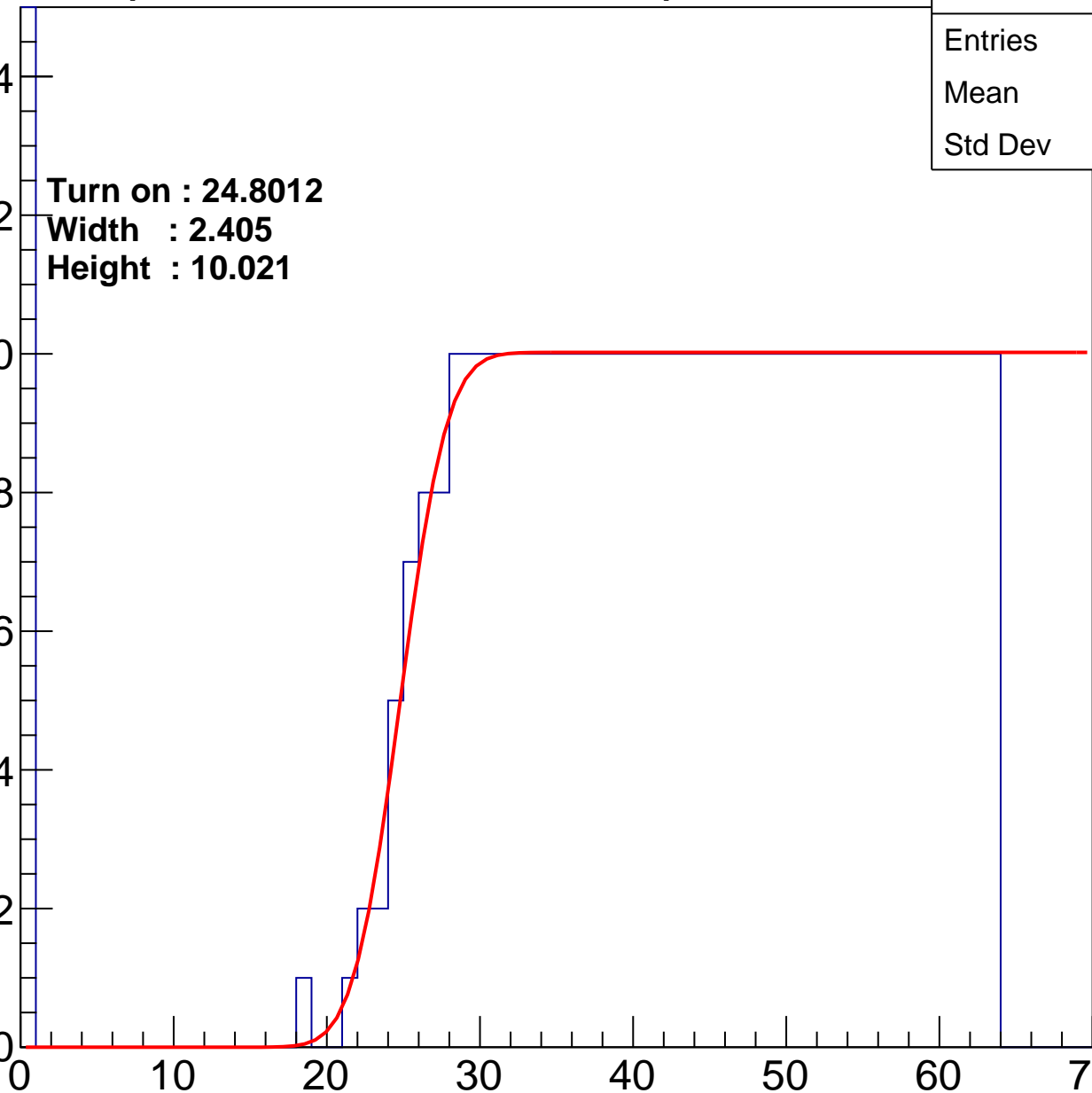
Width : 2.405

Height : 10.021

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch103

calib_packv5_041523_1651.root, FC#0, port C2

Entries	421
Mean	39.42
Std Dev	17.87

Turn on : 27.4716

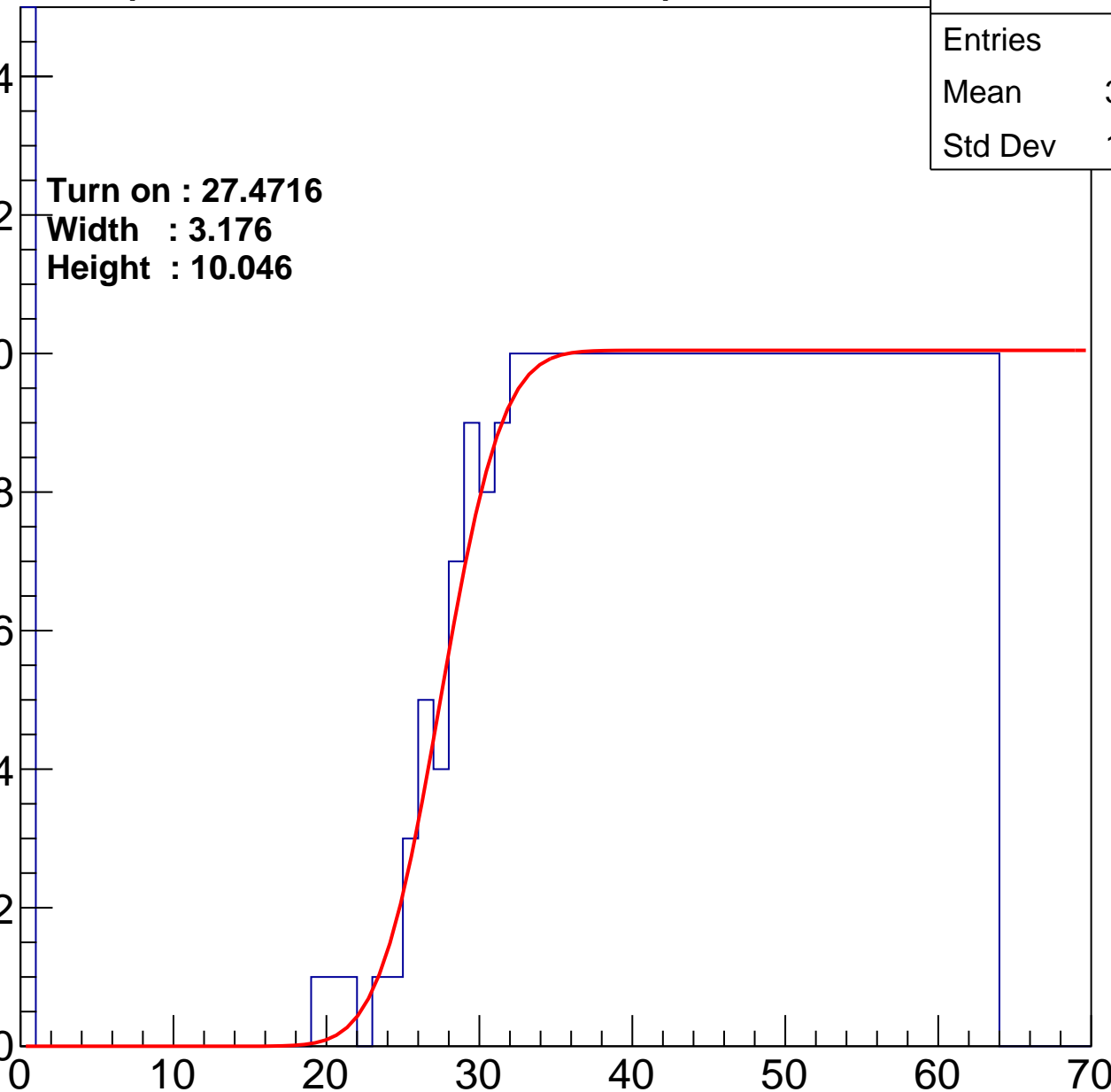
Width : 3.176

Height : 10.046

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch104

calib_packv5_041523_1651.root, FC#0, port C2

Entries	443
Mean	39.05
Std Dev	17.2

Turn on : 24.3186

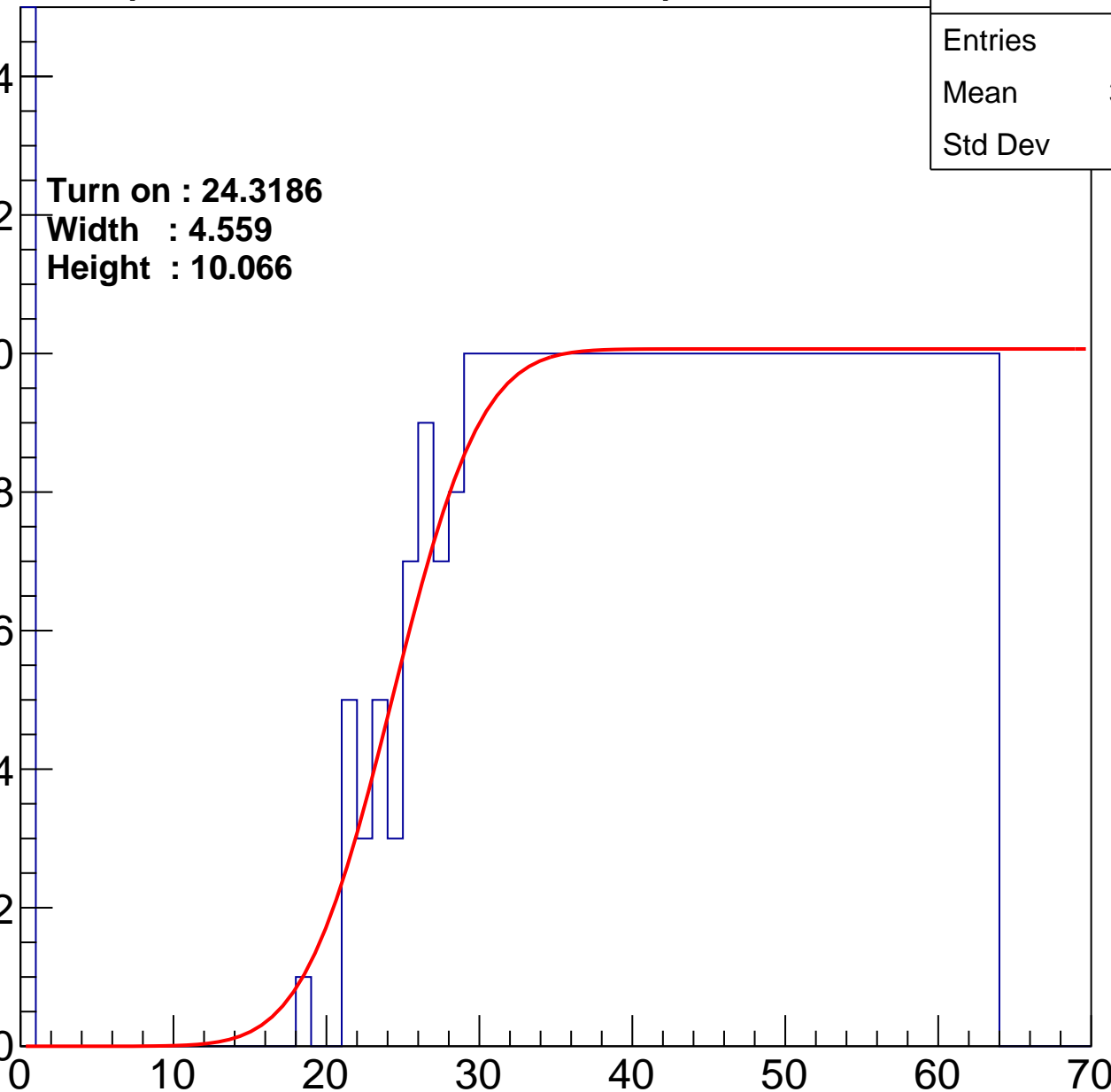
Width : 4.559

Height : 10.066

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch105

calib_packv5_041523_1651.root, FC#0, port C2

Entries	417
Mean	40.42
Std Dev	16.59

Turn on : 26.5061

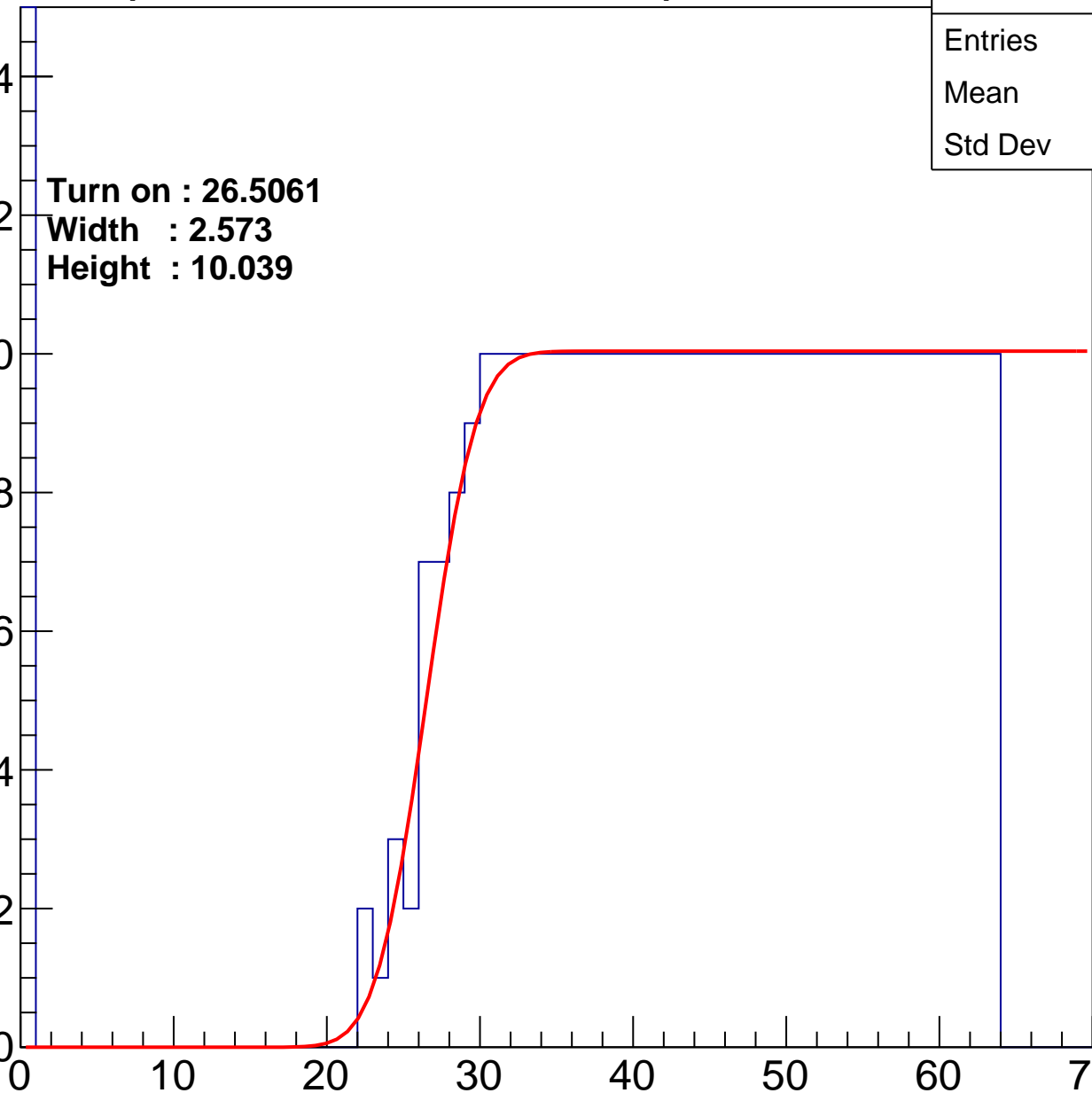
Width : 2.573

Height : 10.039

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch106

calib_packv5_041523_1651.root, FC#0, port C2

Entries	454
Mean	38.01
Std Dev	18.12

Turn on : 24.2417

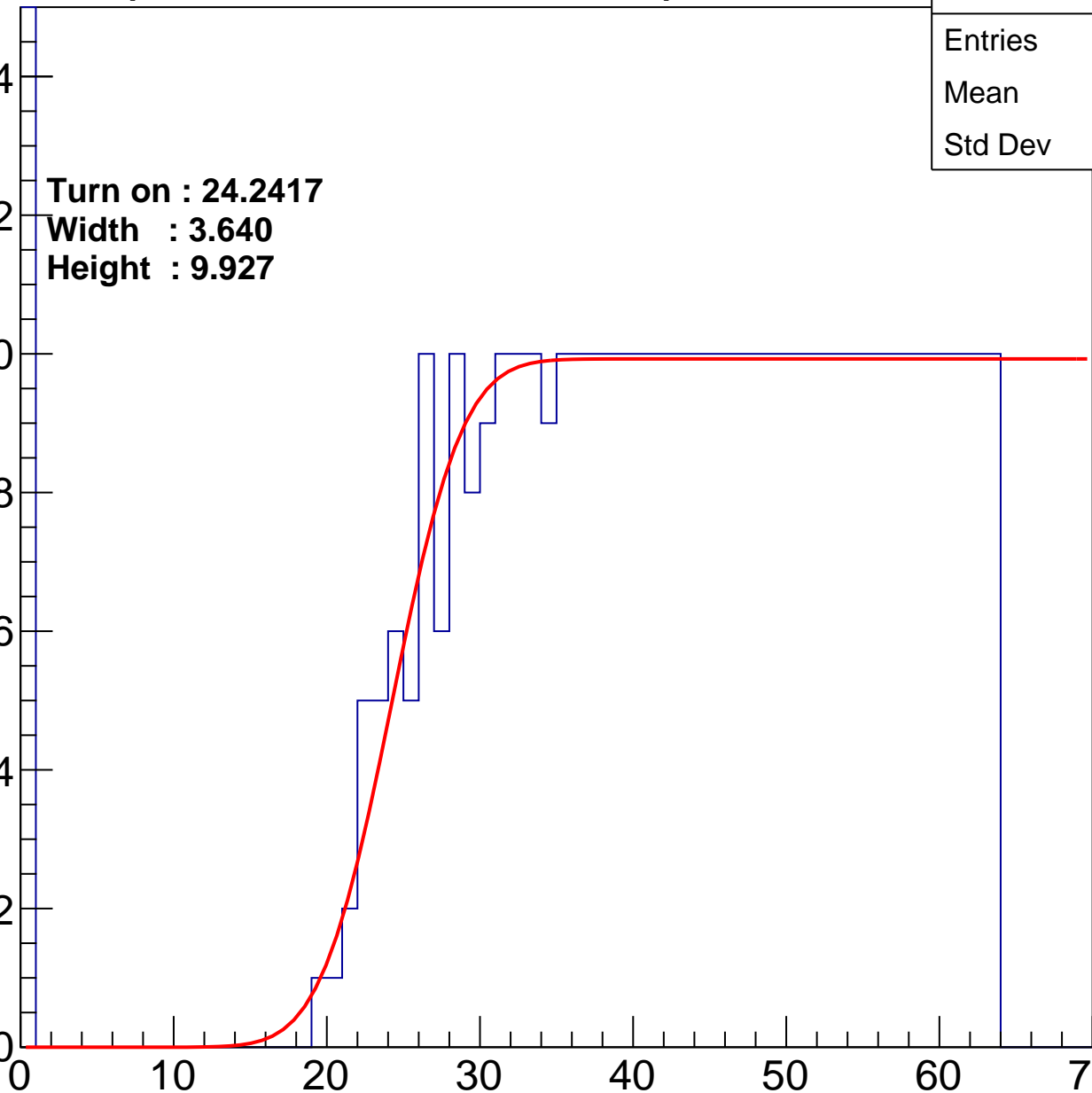
Width : 3.640

Height : 9.927

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch107

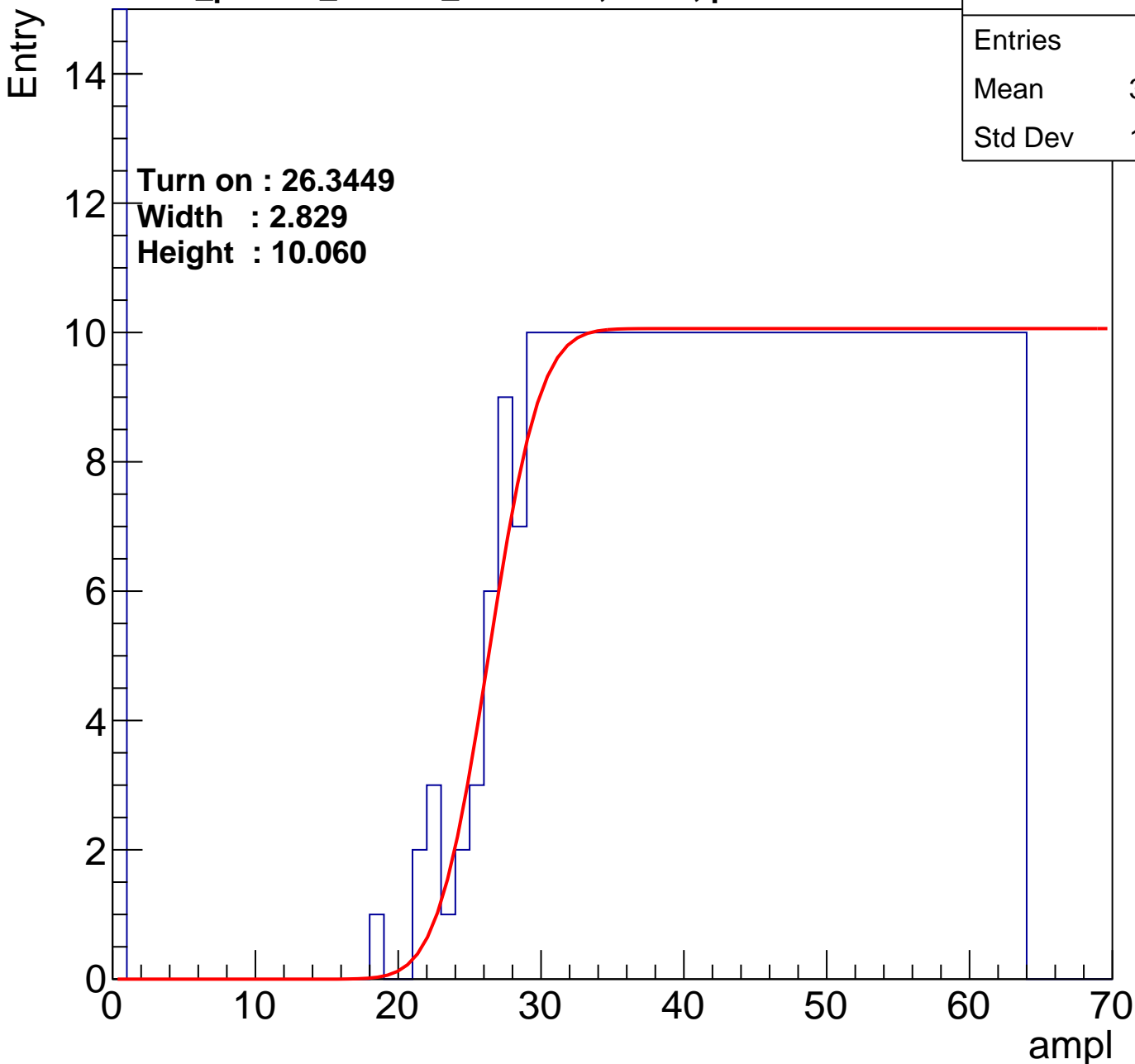
calib_packv5_041523_1651.root, FC#0, port C2

Entries	448
Mean	37.87
Std Dev	18.66

Turn on : 26.3449

Width : 2.829

Height : 10.060



B1L103S, U9-ch108

calib_packv5_041523_1651.root, FC#0, port C2

Entries	418
Mean	39.94
Std Dev	17.24

Turn on : 26.5914

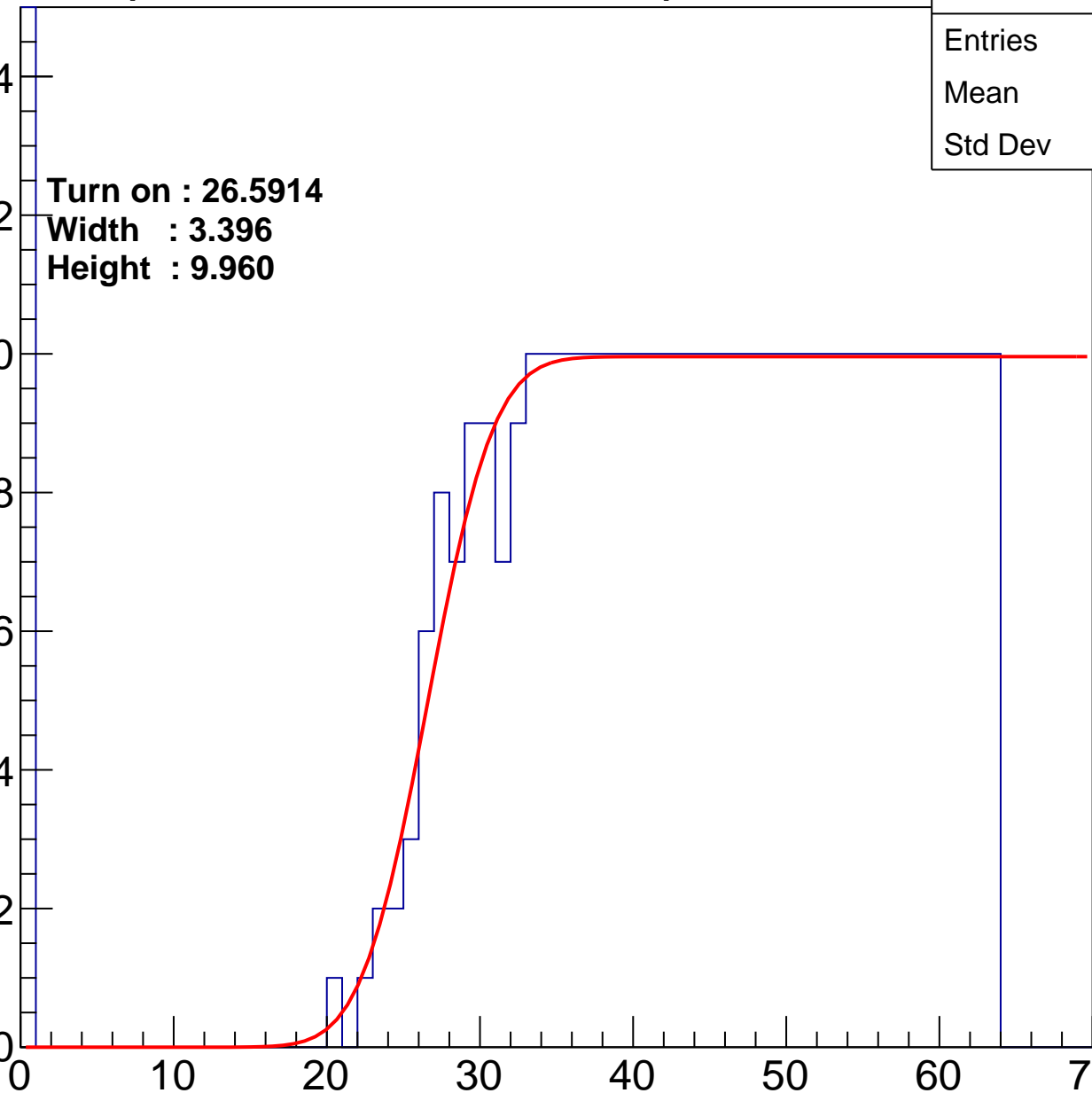
Width : 3.396

Height : 9.960

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch109

calib_packv5_041523_1651.root, FC#0, port C2

Entries	449
Mean	37.92
Std Dev	18.52

Turn on : 26.0522

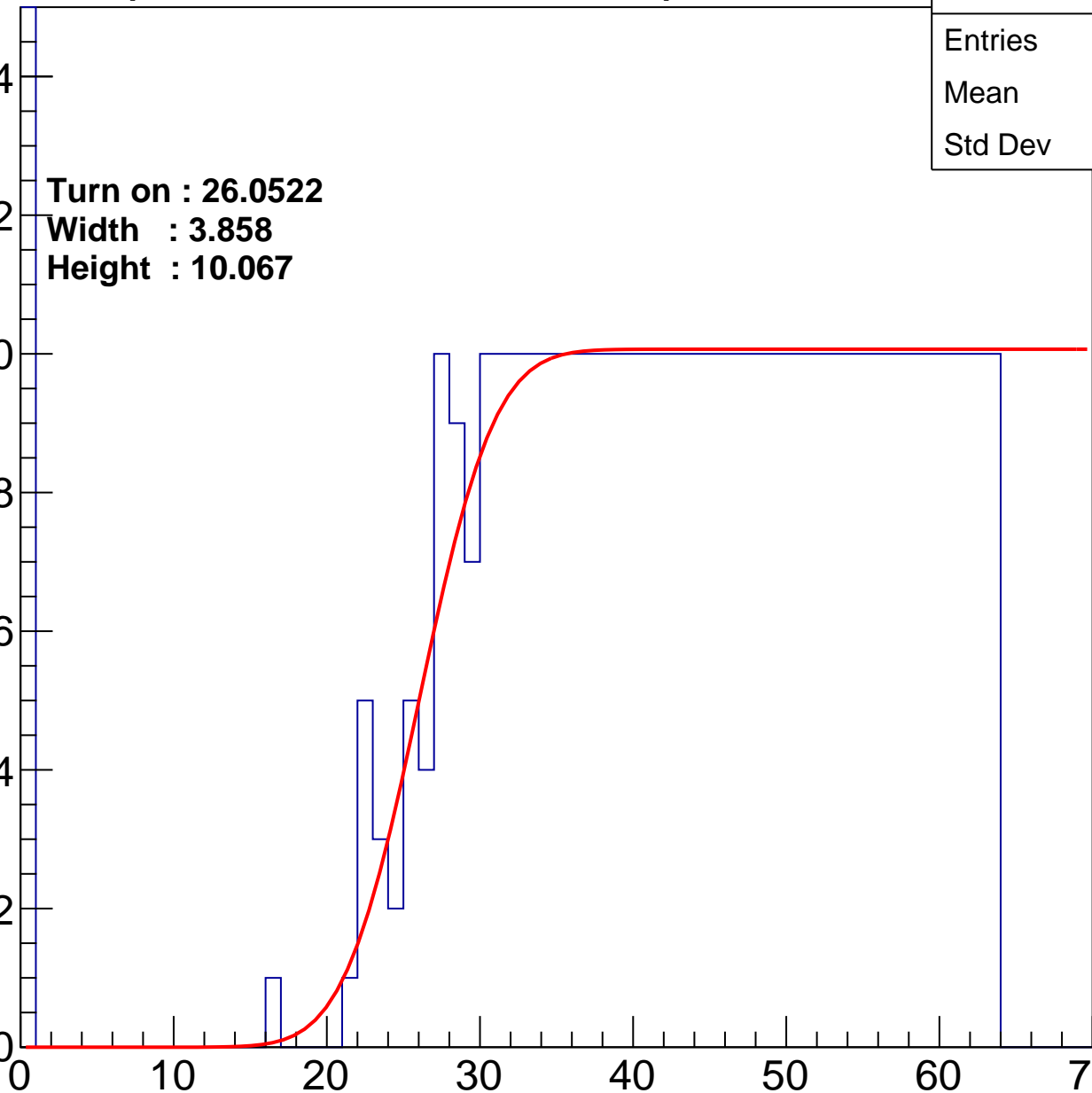
Width : 3.858

Height : 10.067

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch110

calib_packv5_041523_1651.root, FC#0, port C2

Entries	429
Mean	39.53
Std Dev	17.26

Turn on : 26.0820

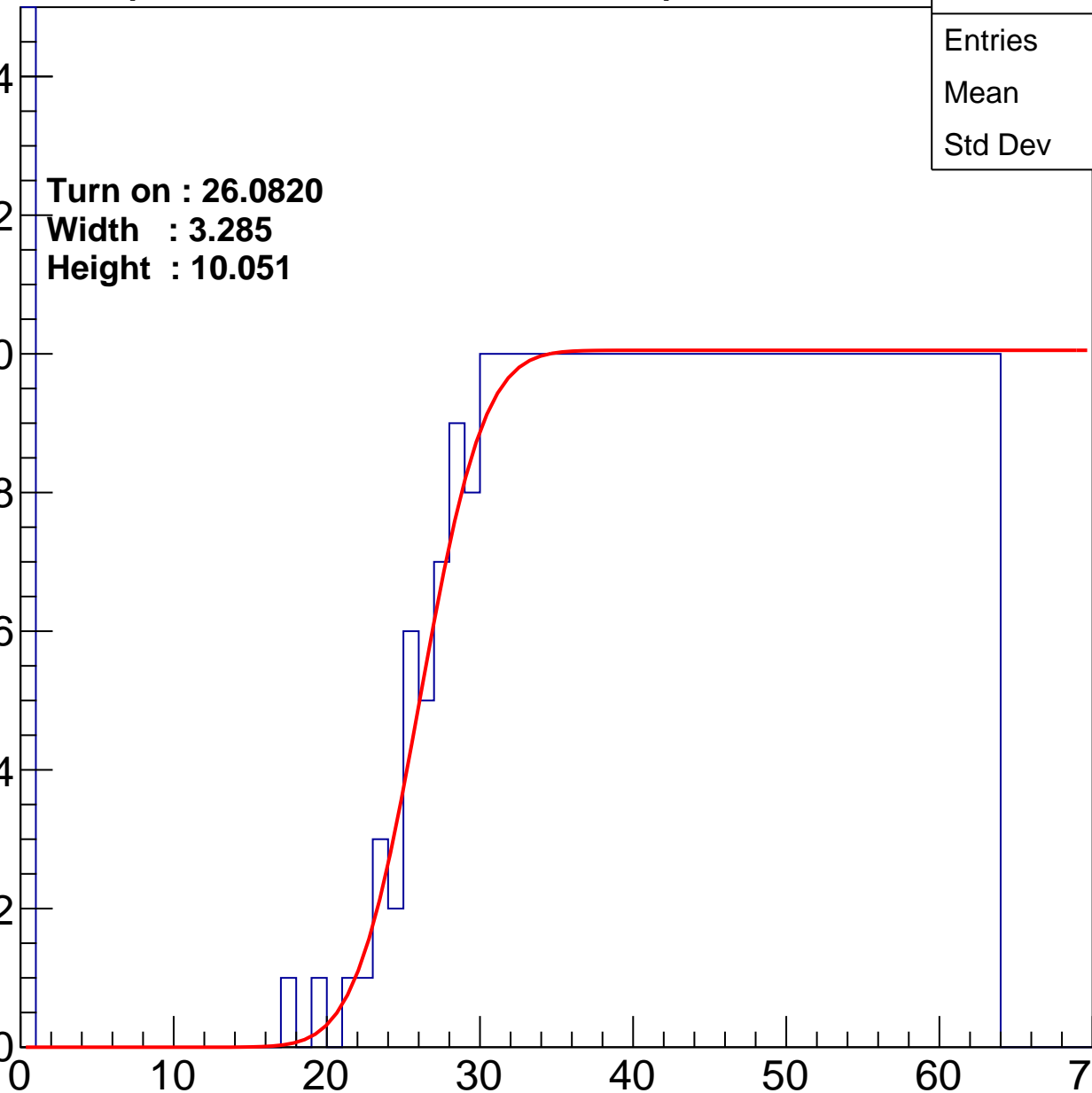
Width : 3.285

Height : 10.051

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch111

calib_packv5_041523_1651.root, FC#0, port C2

Entries	433
Mean	38.55
Std Dev	18.5

Turn on : 27.5186

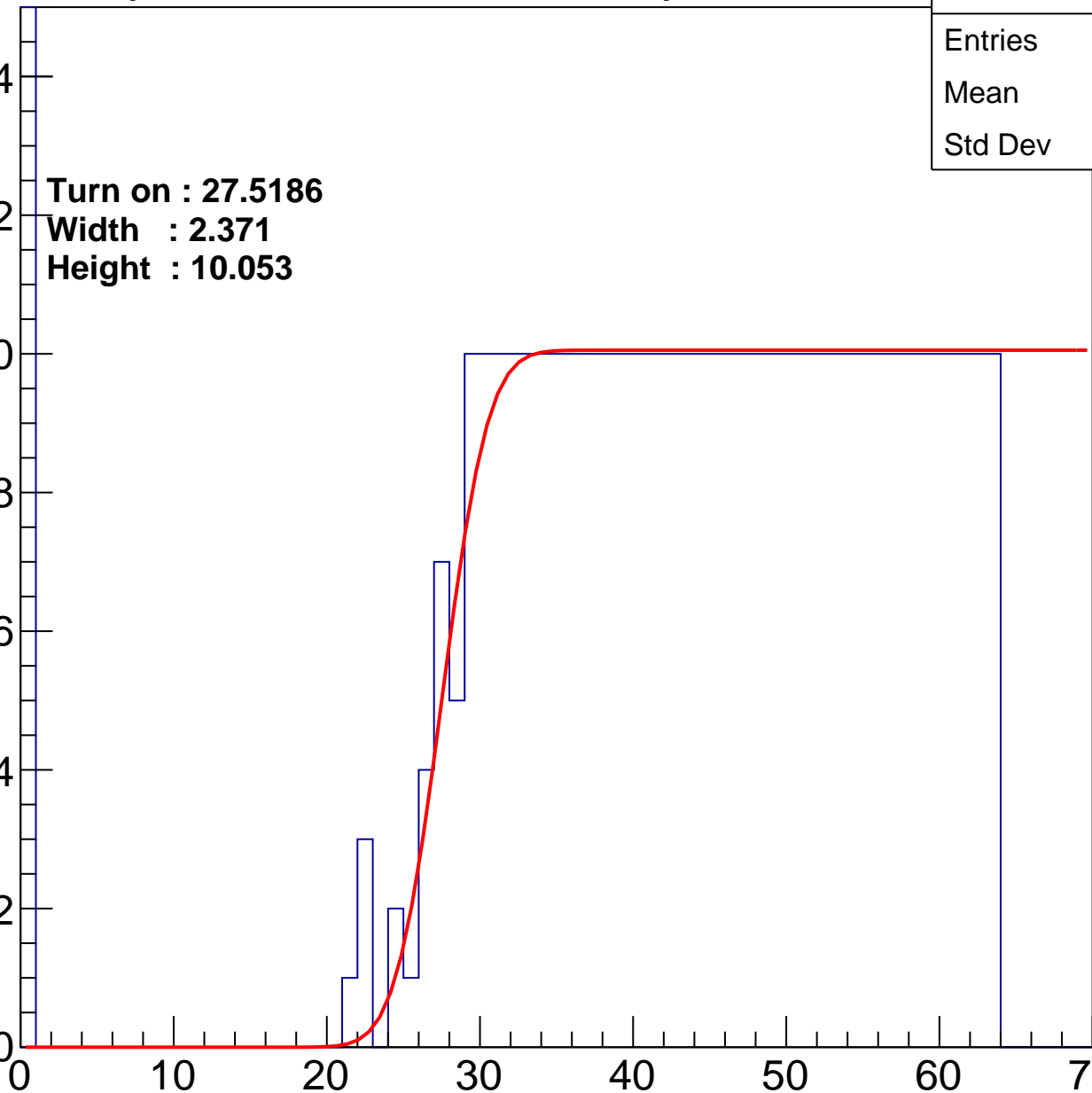
Width : 2.371

Height : 10.053

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch112

calib_packv5_041523_1651.root, FC#0, port C2

Entries	449
Mean	38.17
Std Dev	18.2

Turn on : 25.1012

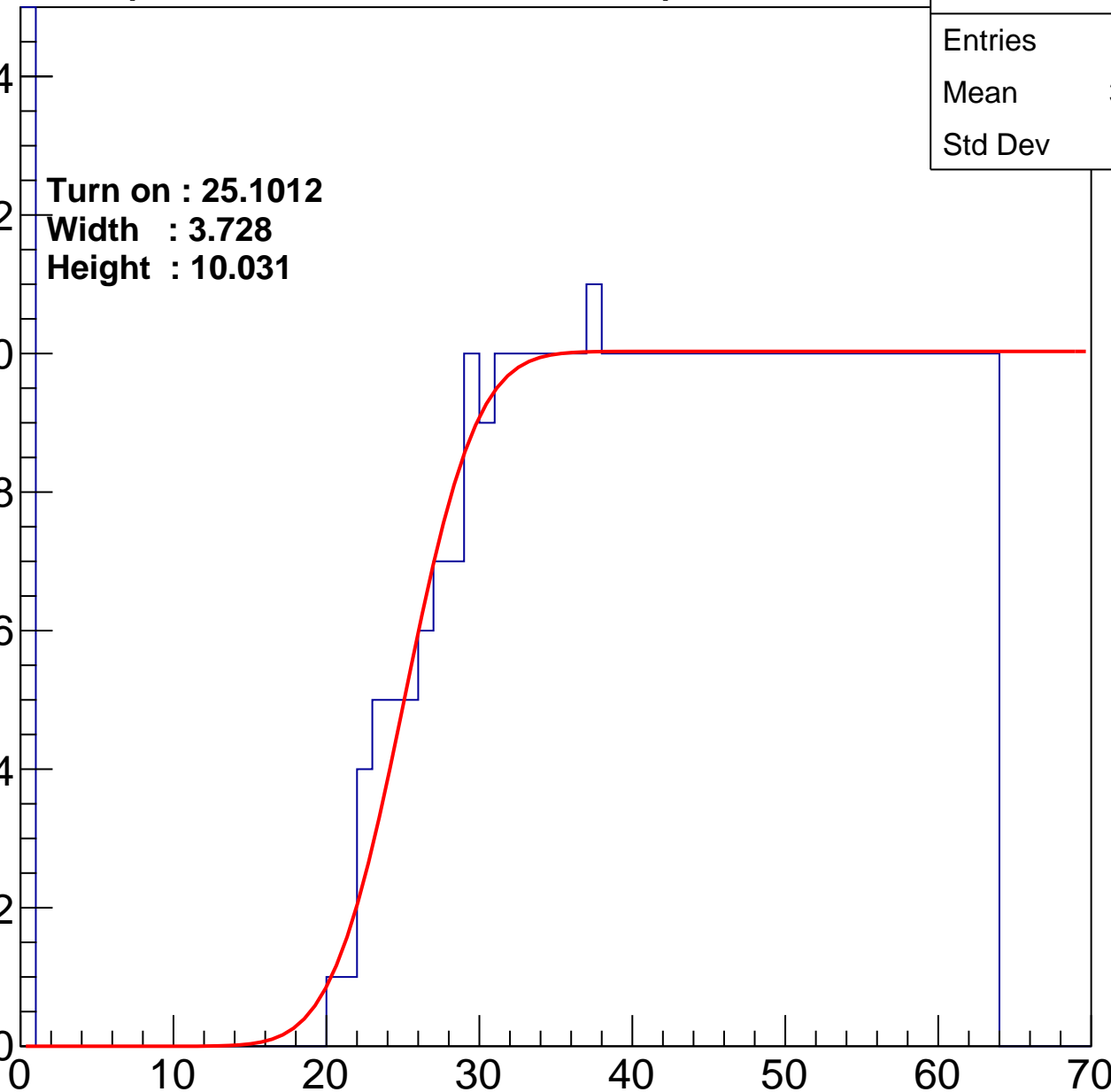
Width : 3.728

Height : 10.031

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch113

calib_packv5_041523_1651.root, FC#0, port C2

Entries	435
Mean	39.04
Std Dev	17.67

Turn on : 25.8641

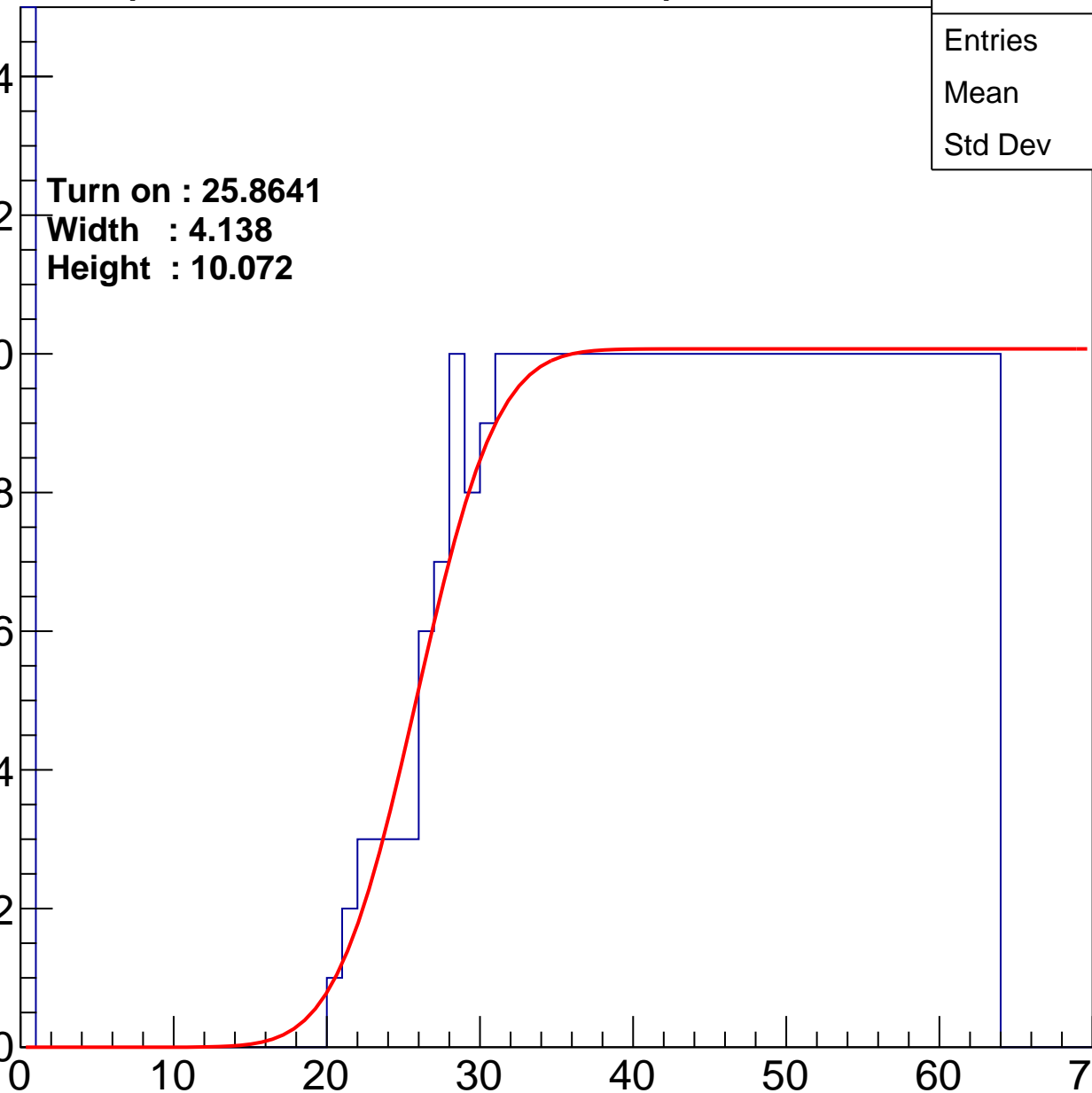
Width : 4.138

Height : 10.072

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch114

calib_packv5_041523_1651.root, FC#0, port C2

Entries	434
Mean	39.05
Std Dev	17.7

Turn on : 26.0670

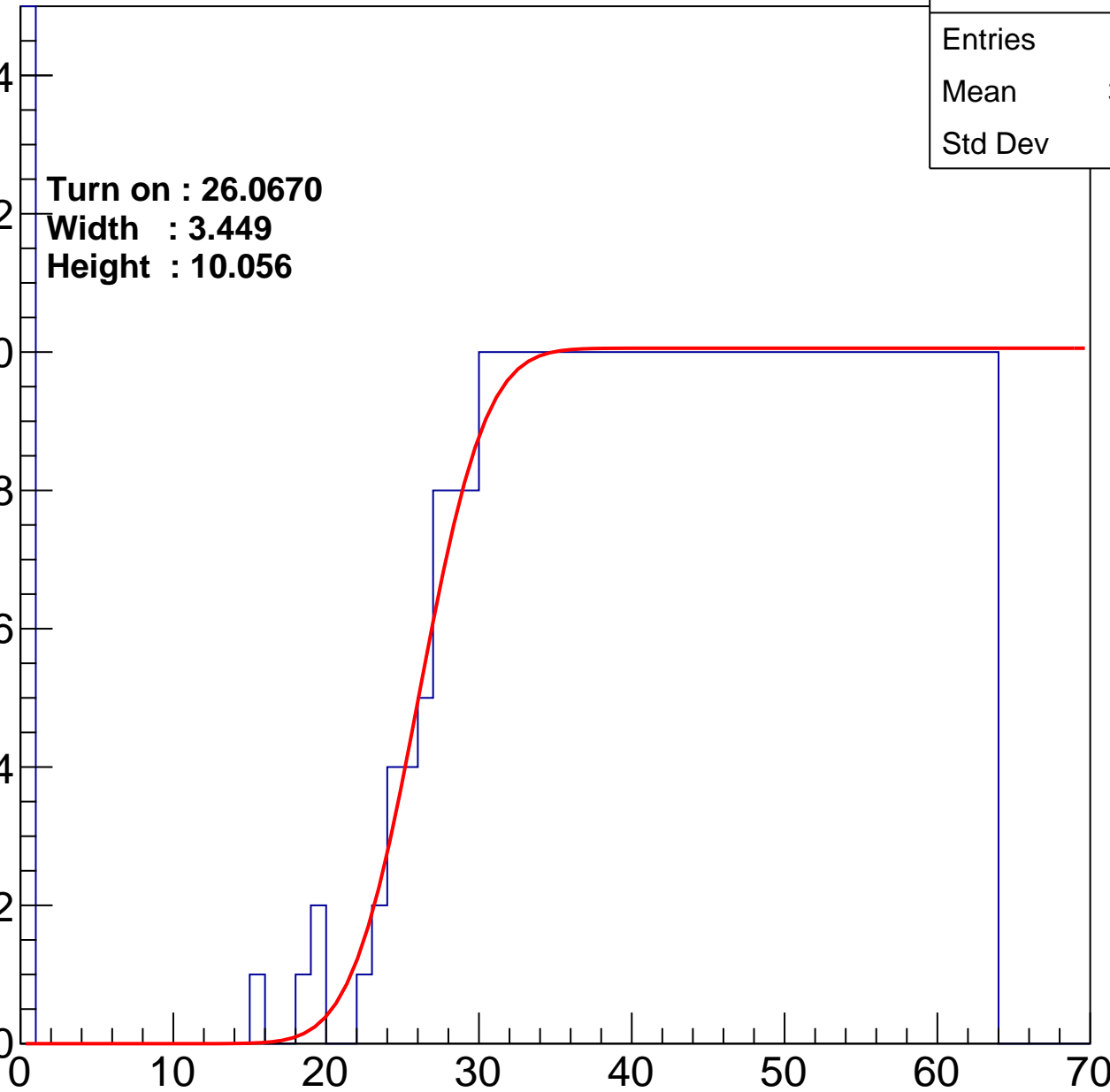
Width : 3.449

Height : 10.056

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch115

calib_packv5_041523_1651.root, FC#0, port C2

Entries	431
Mean	39.44
Std Dev	17.3

Turn on : 25.7587

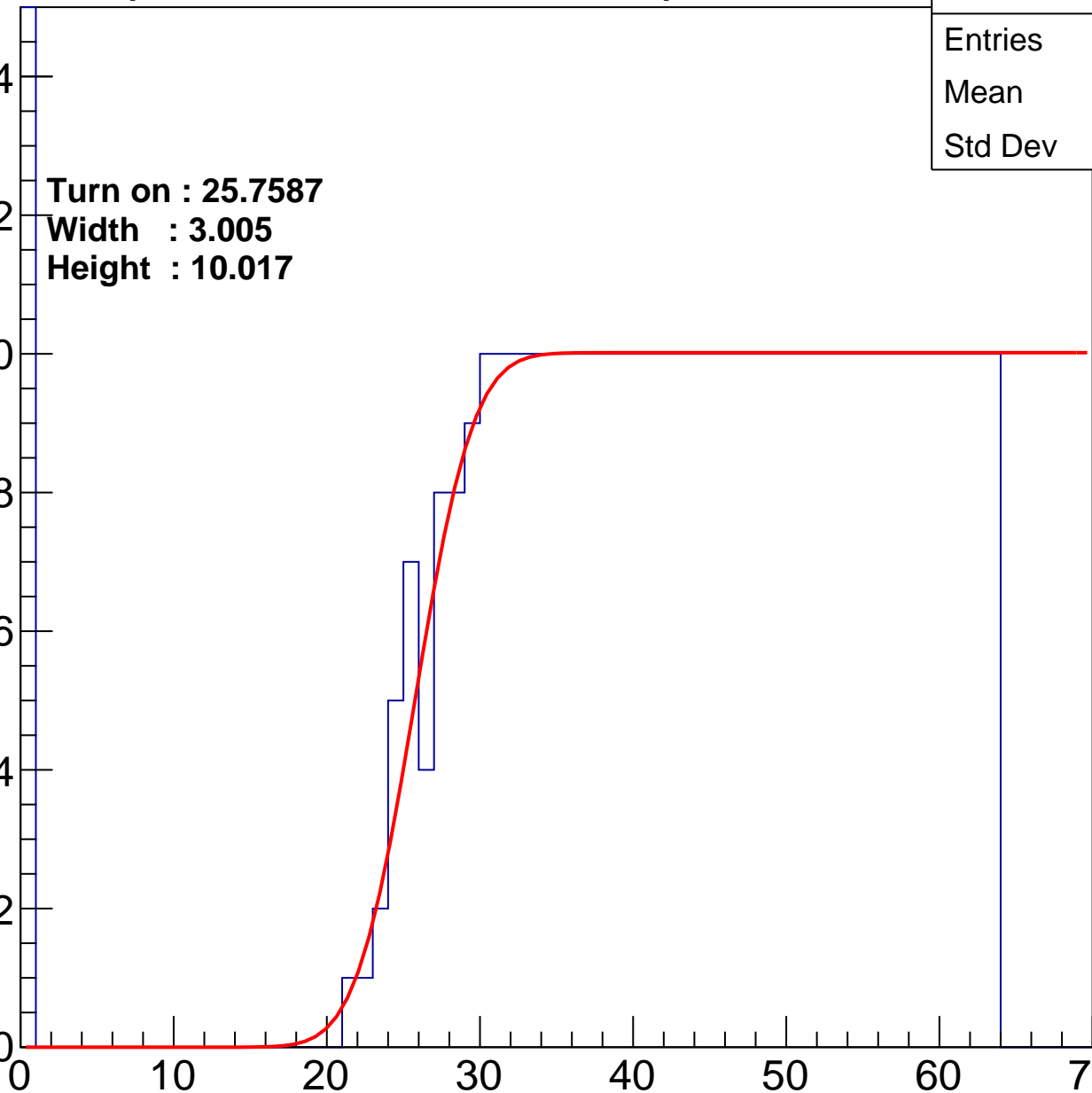
Width : 3.005

Height : 10.017

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch116

calib_packv5_041523_1651.root, FC#0, port C2

Entries	425
Mean	40.03
Std Dev	16.67

Turn on : 26.3173

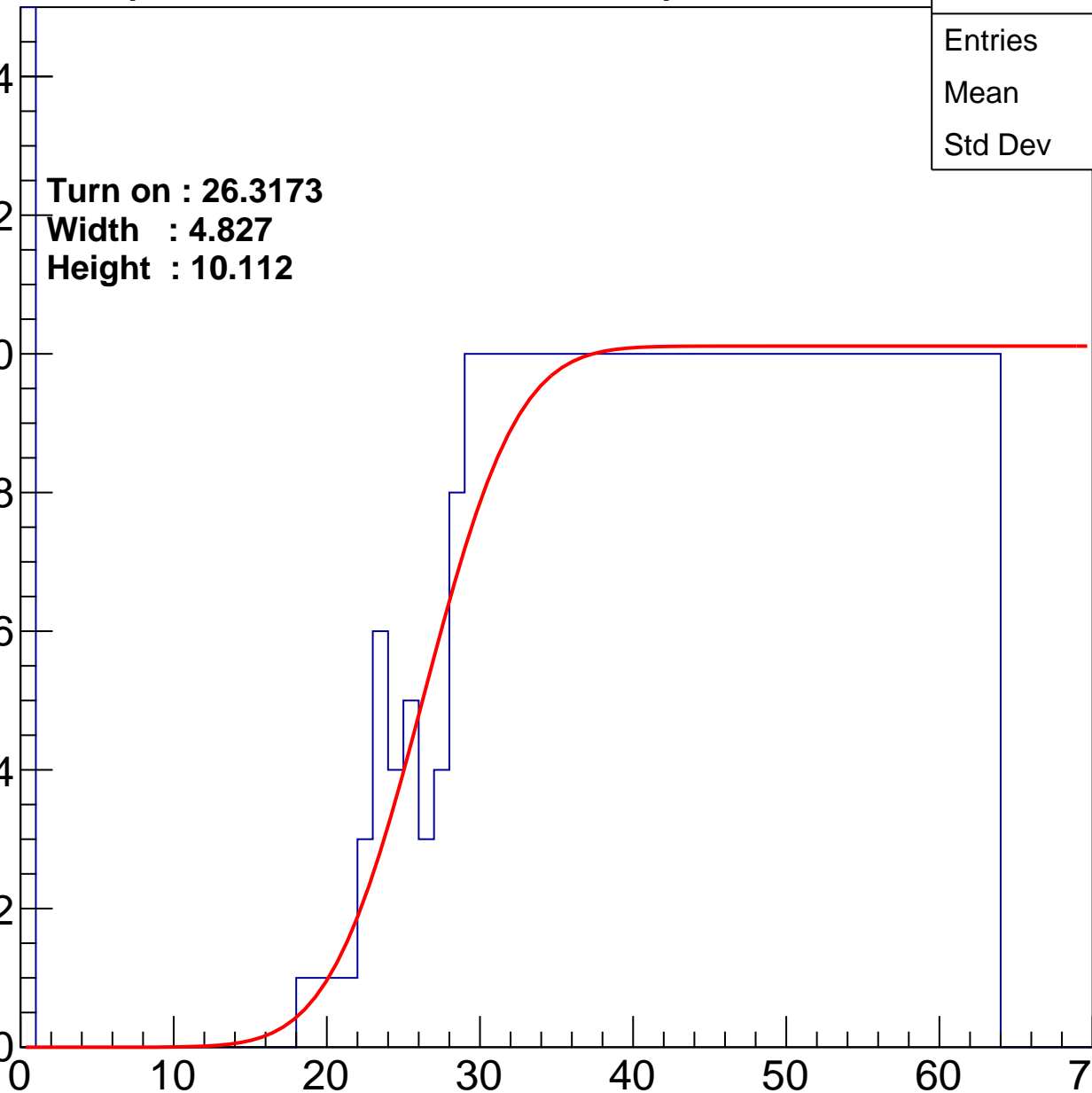
Width : 4.827

Height : 10.112

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch117

calib_packv5_041523_1651.root, FC#0, port C2

Entries	436
Mean	39.03
Std Dev	17.68

Turn on : 25.6121

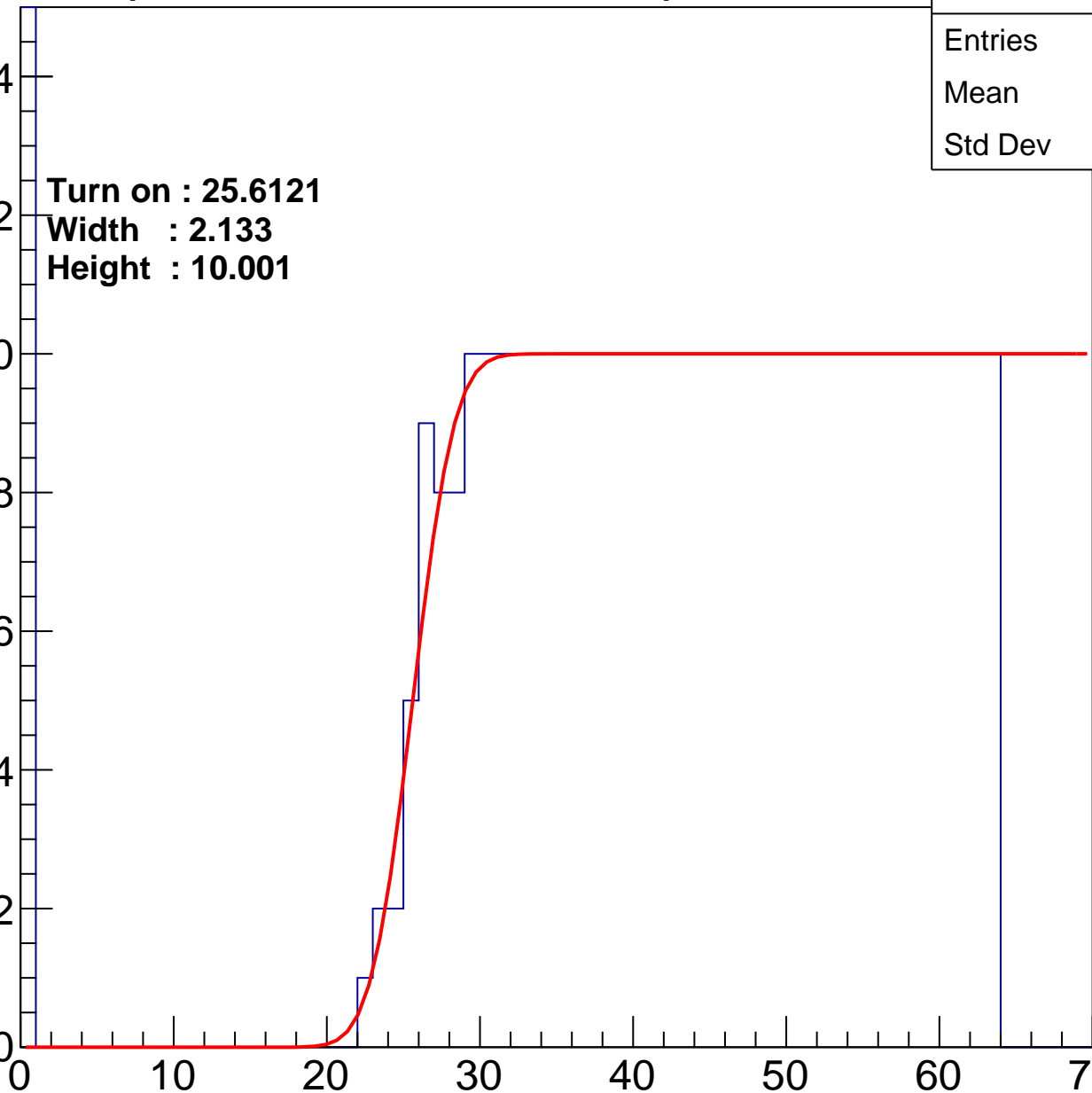
Width : 2.133

Height : 10.001

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch118

calib_packv5_041523_1651.root, FC#0, port C2

Entries	455
Mean	37.41
Std Dev	18.94

Turn on : 25.7852

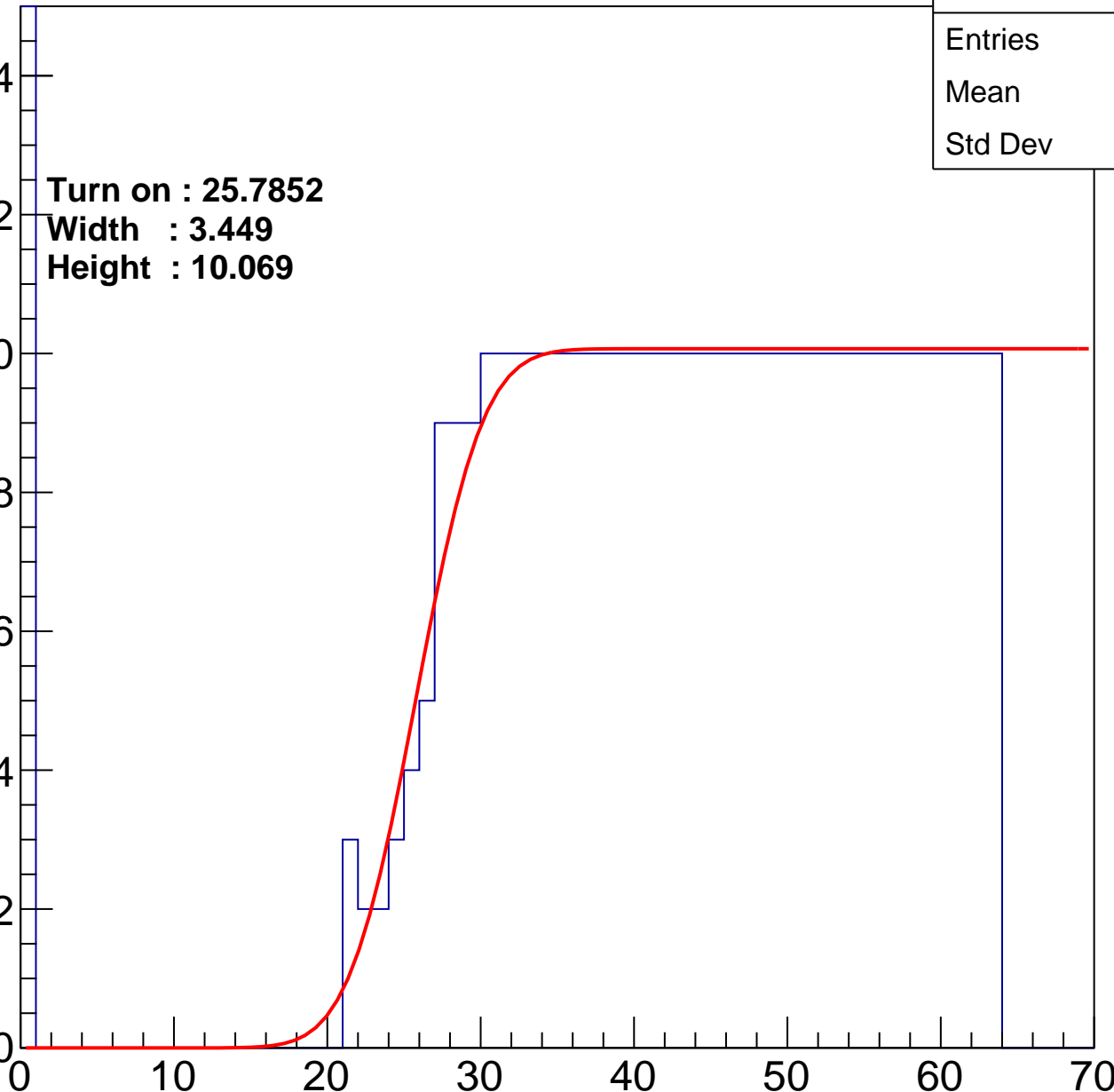
Width : 3.449

Height : 10.069

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch119

calib_packv5_041523_1651.root, FC#0, port C2

Entries	438
Mean	39.07
Std Dev	17.5

Turn on : 25.4800

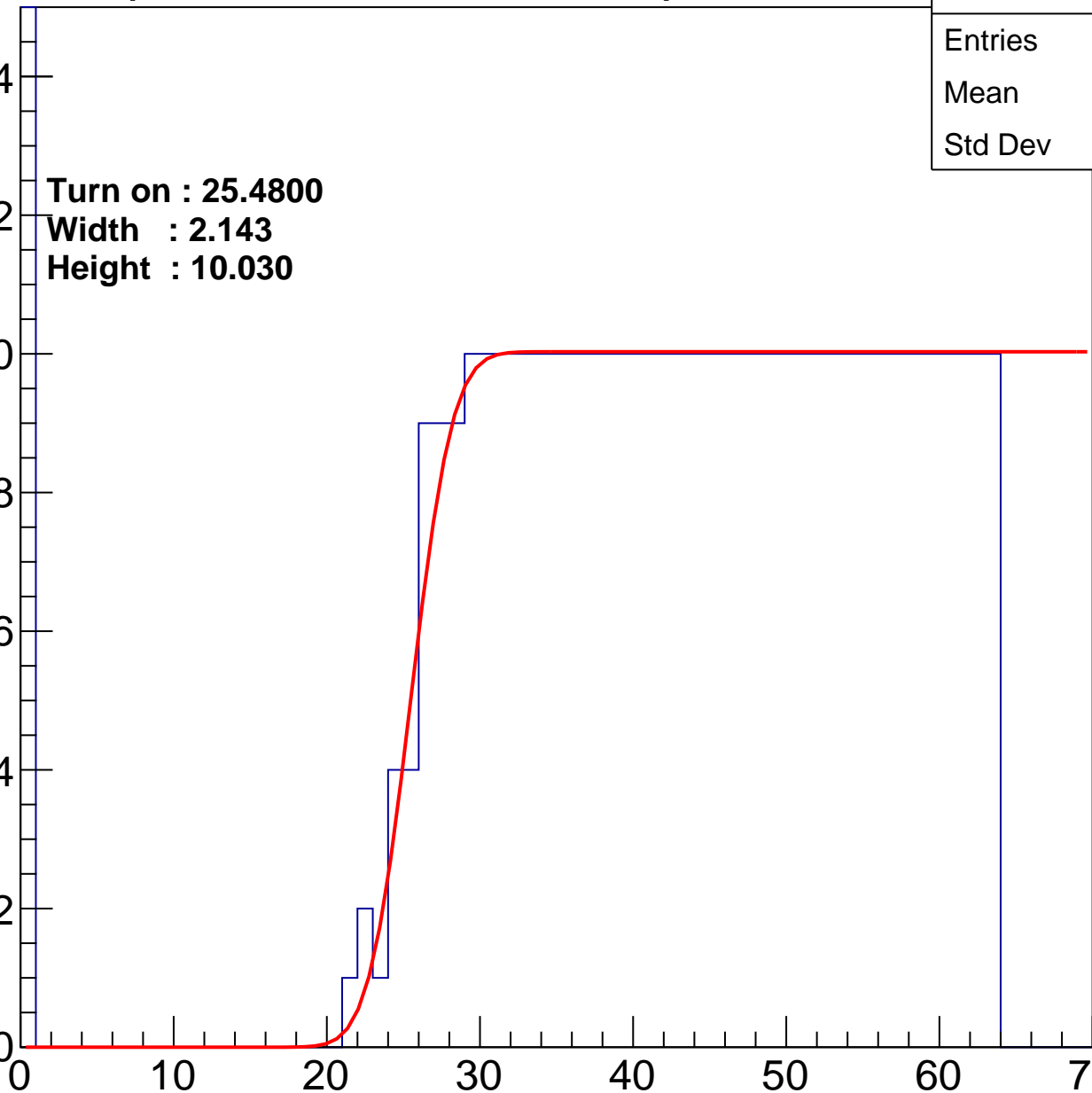
Width : 2.143

Height : 10.030

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch120

calib_packv5_041523_1651.root, FC#0, port C2

Entries	476
Mean	37.15
Std Dev	18.27

Turn on : 22.5892

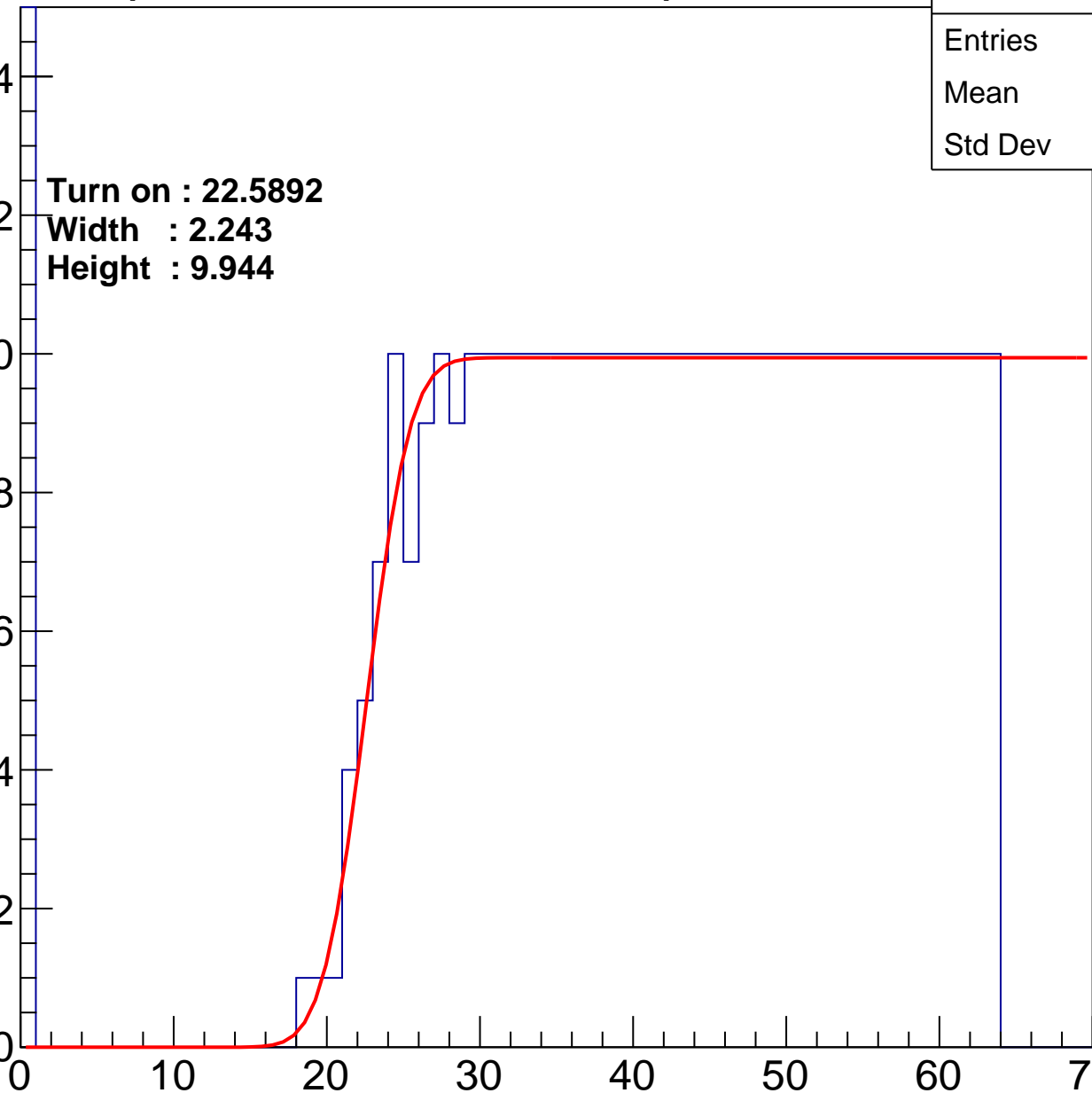
Width : 2.243

Height : 9.944

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch121

calib_packv5_041523_1651.root, FC#0, port C2

Entries	424
Mean	39.95
Std Dev	16.94

Turn on : 25.7808

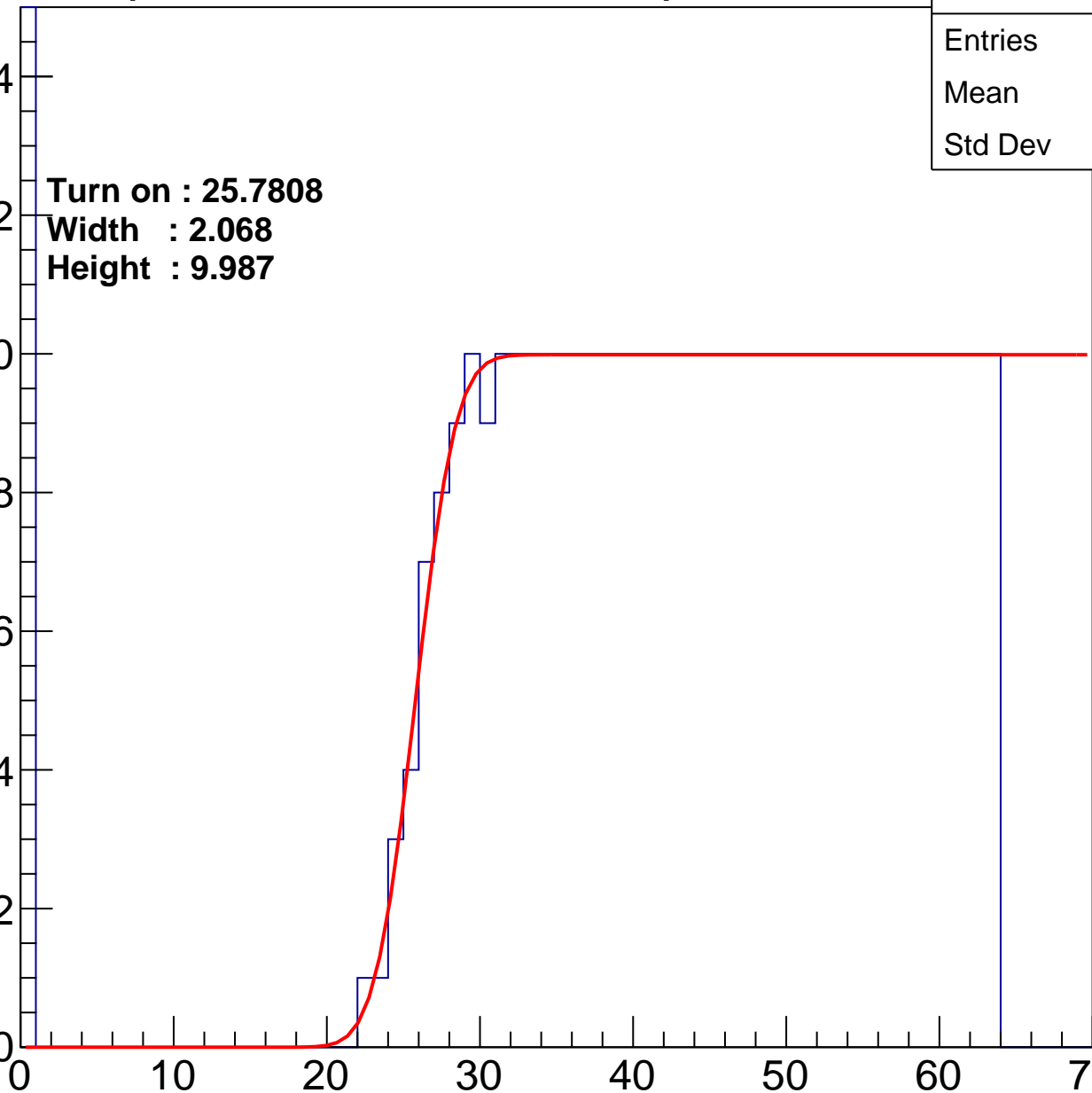
Width : 2.068

Height : 9.987

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch122

calib_packv5_041523_1651.root, FC#0, port C2

Entries	429
Mean	40.01
Std Dev	16.52

Turn on : 24.8462

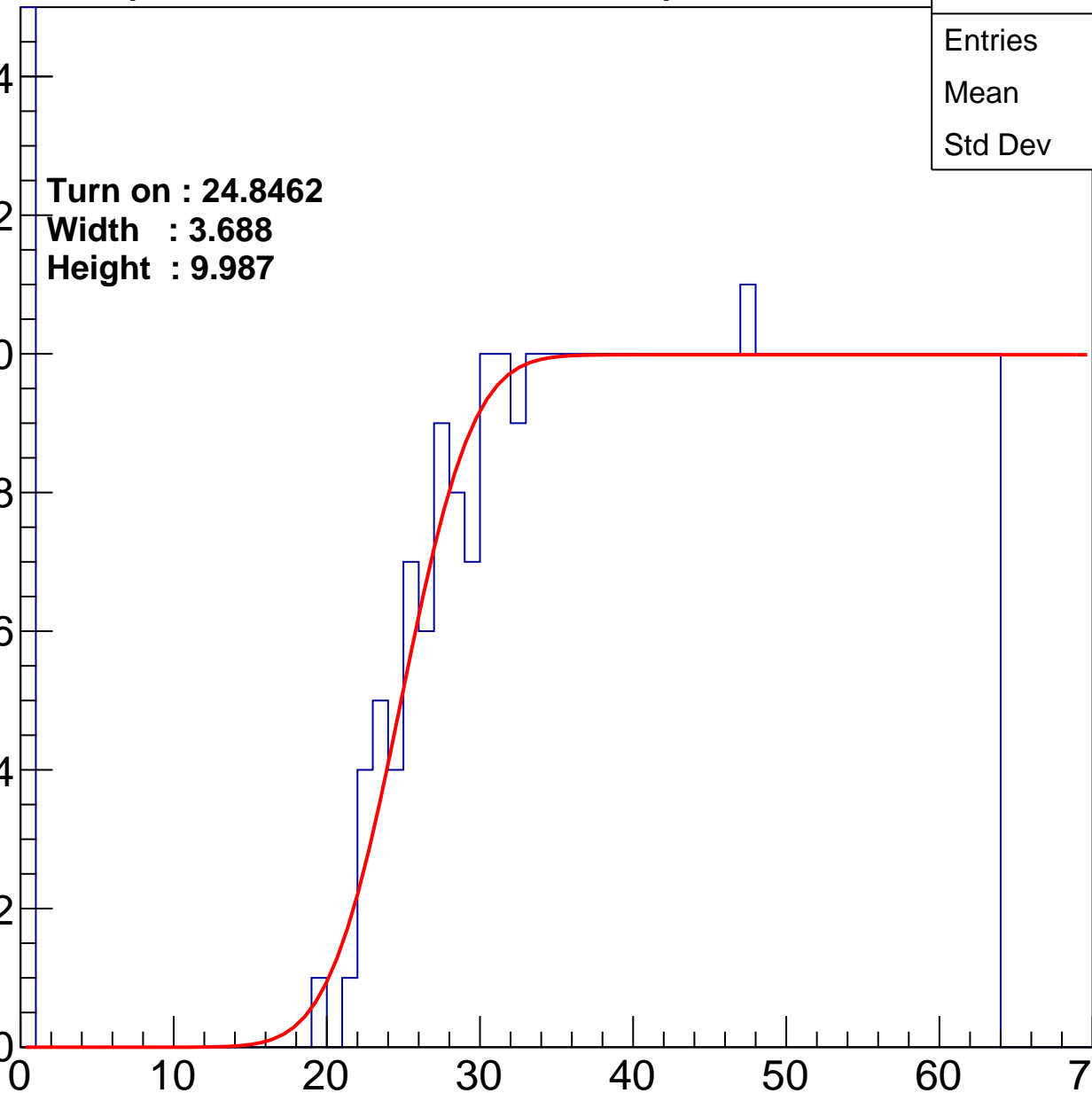
Width : 3.688

Height : 9.987

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch123

calib_packv5_041523_1651.root, FC#0, port C2

Entries	410
Mean	40.47
Std Dev	16.89

Turn on : 27.6466

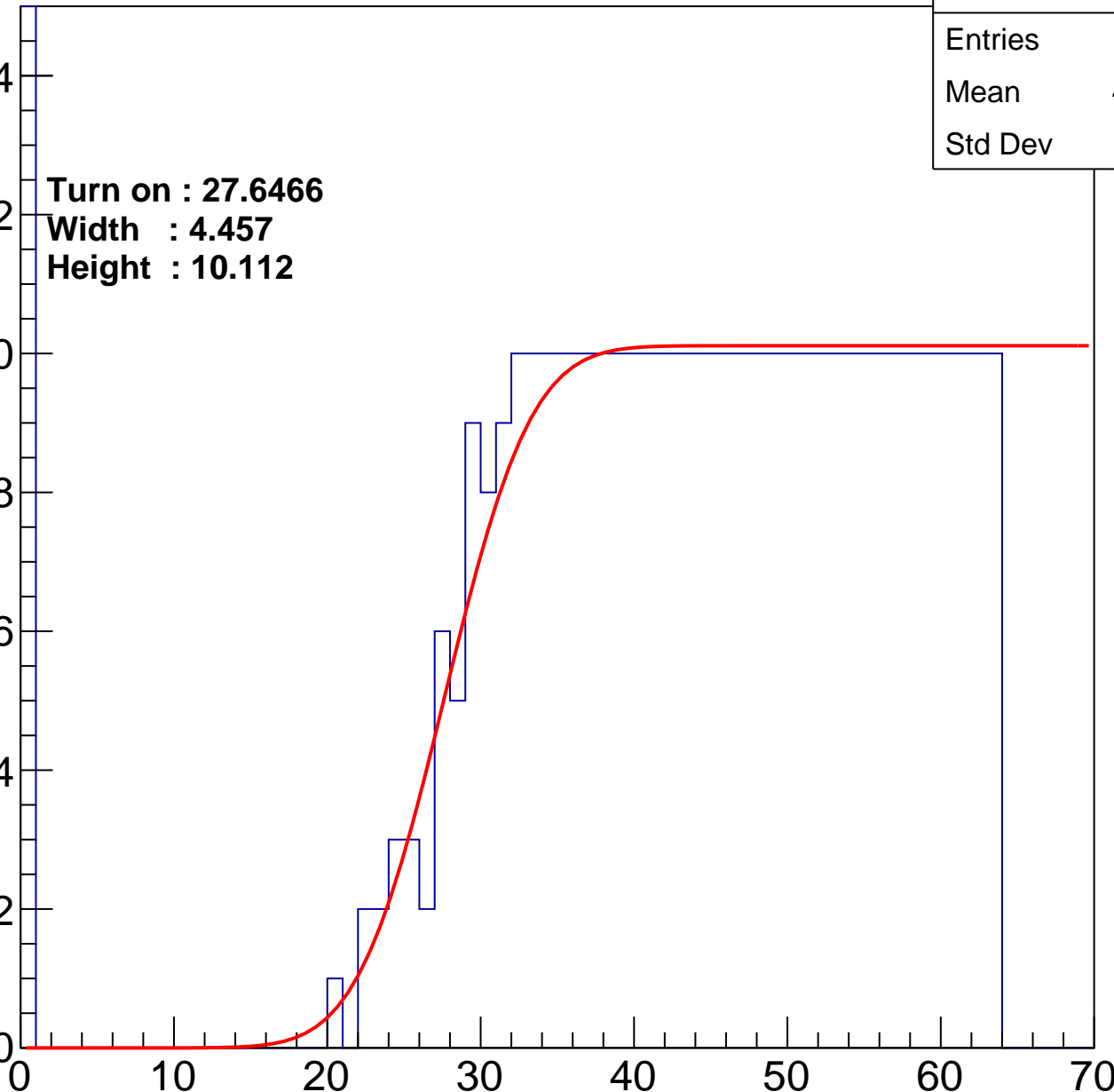
Width : 4.457

Height : 10.112

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch124

calib_packv5_041523_1651.root, FC#0, port C2

Entries	445
Mean	38.9
Std Dev	17.3

Turn on : 24.4466

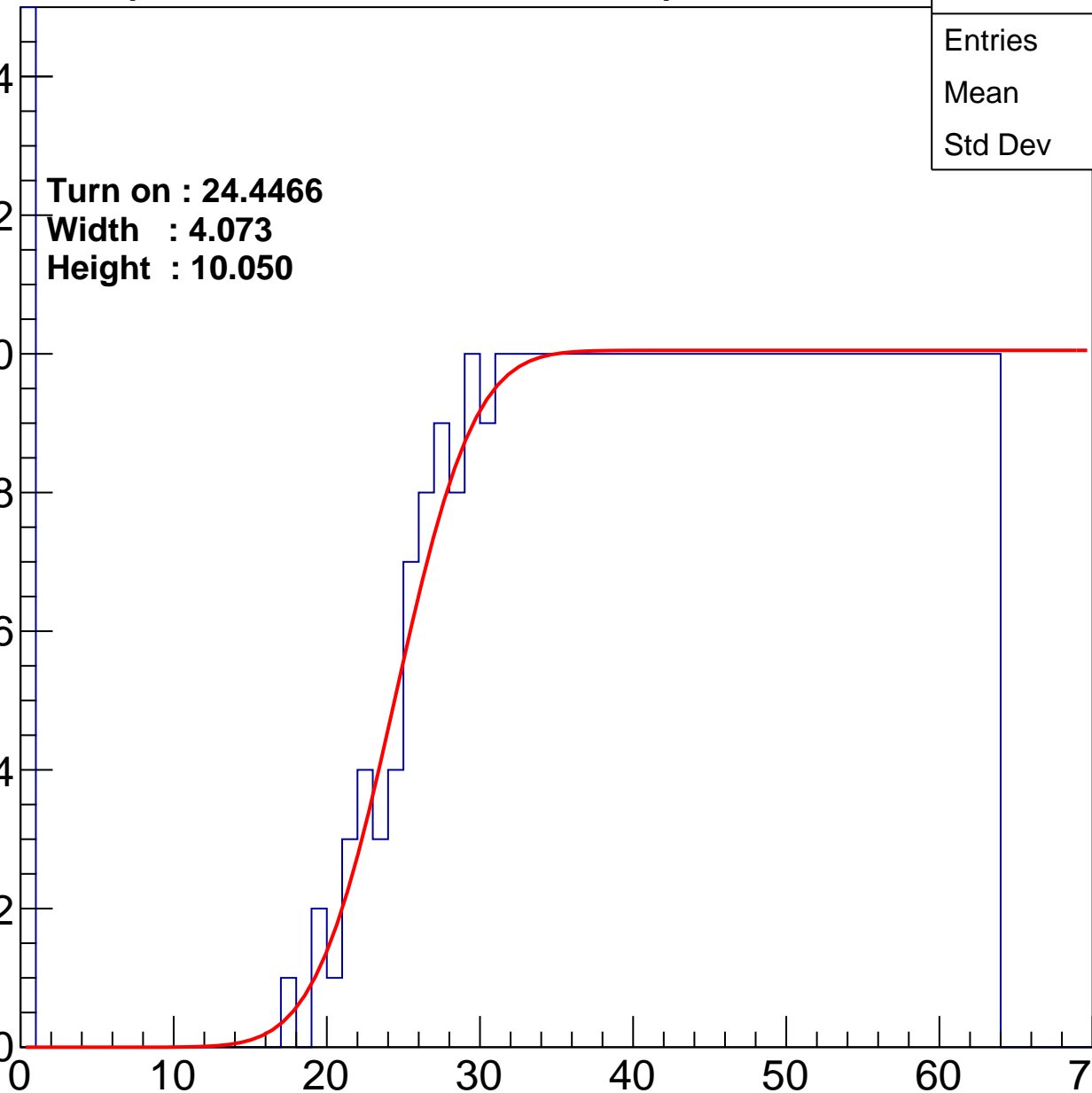
Width : 4.073

Height : 10.050

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch125

calib_packv5_041523_1651.root, FC#0, port C2

Entries	429
Mean	39.36
Std Dev	17.52

Turn on : 26.2532

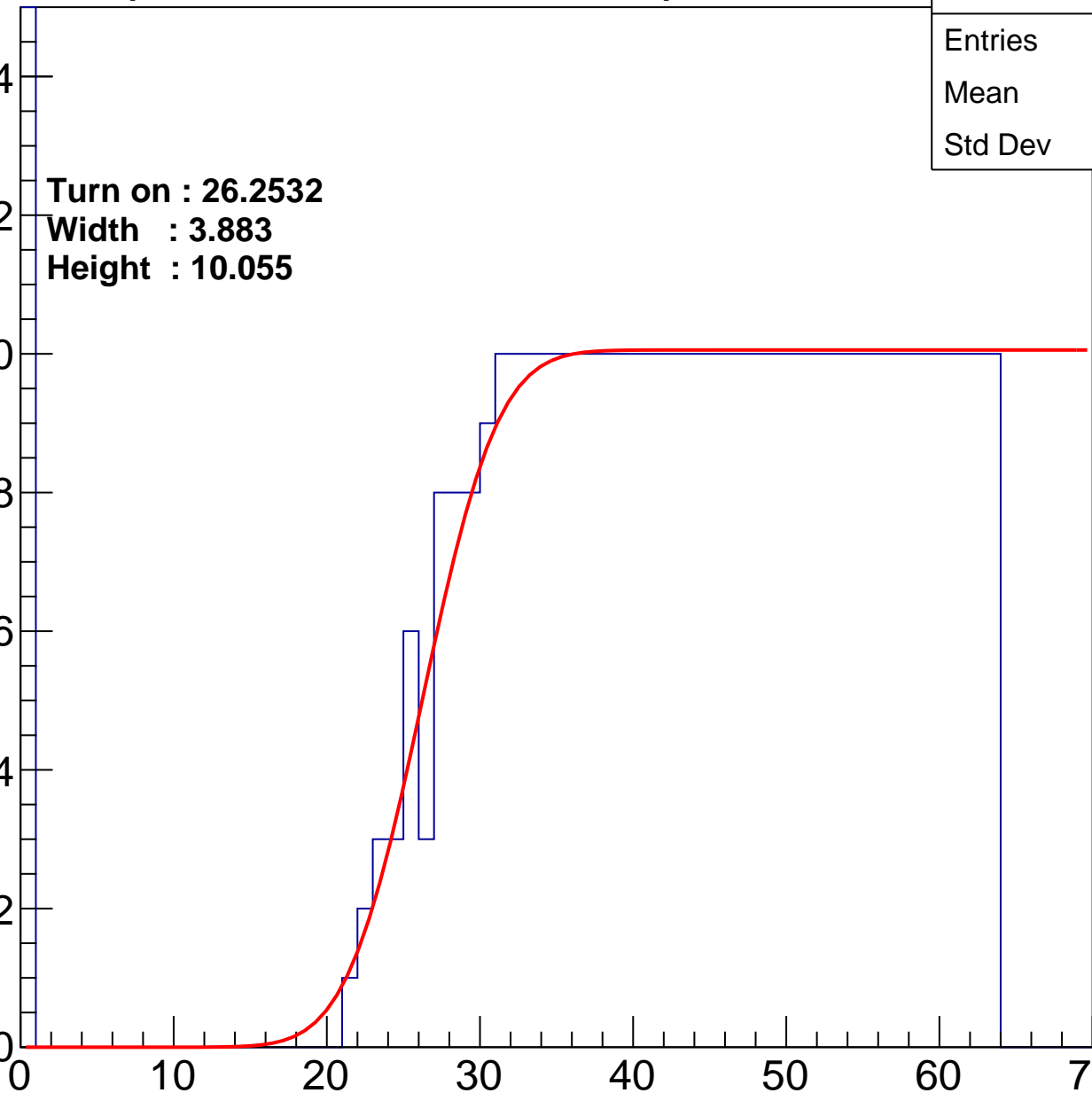
Width : 3.883

Height : 10.055

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch126

calib_packv5_041523_1651.root, FC#0, port C2

Entries	458
Mean	38.08
Std Dev	17.85

Turn on : 23.9810

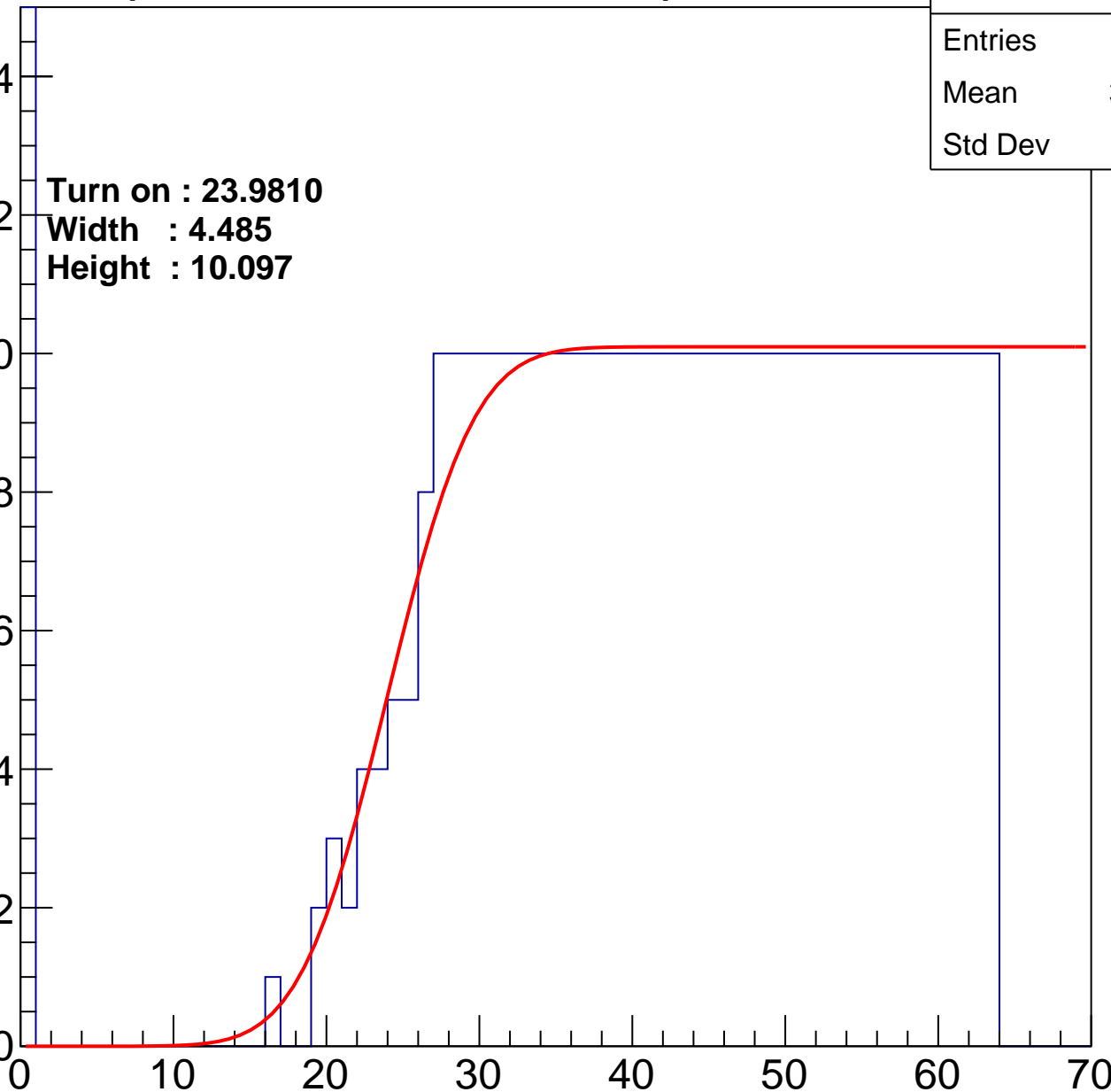
Width : 4.485

Height : 10.097

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch127

calib_packv5_041523_1651.root, FC#0, port C2

Entries	457
Mean	37.62
Std Dev	18.5

Turn on : 24.7720

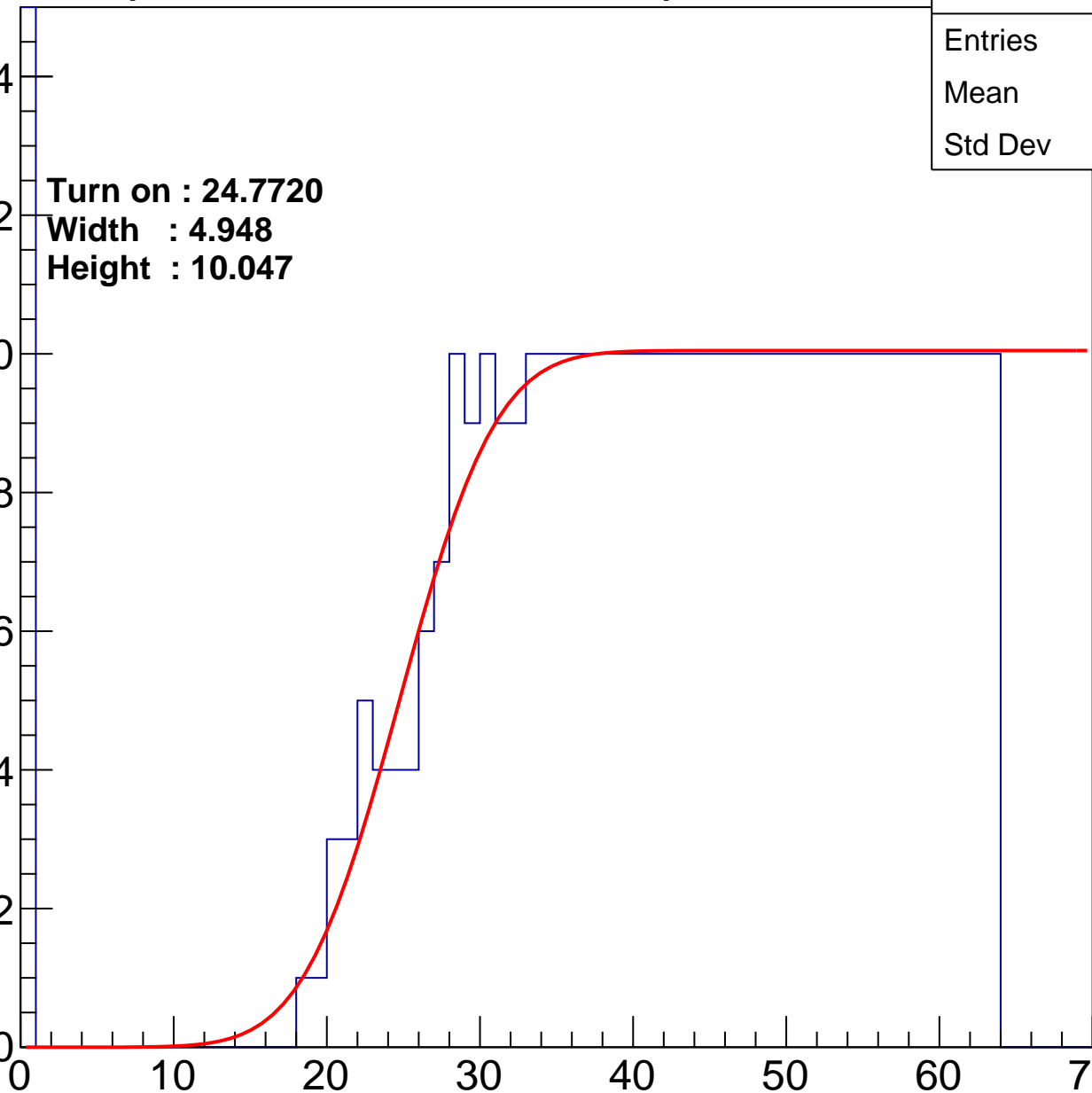
Width : 4.948

Height : 10.047

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U9-ch127

calib_packv5_041523_1651.root, FC#0, port C2

Entries	457
Mean	37.62
Std Dev	18.5

Turn on : 24.7720

Width : 4.948

Height : 10.047

Entry

14
12
10
8
6
4
2
0

ampl

