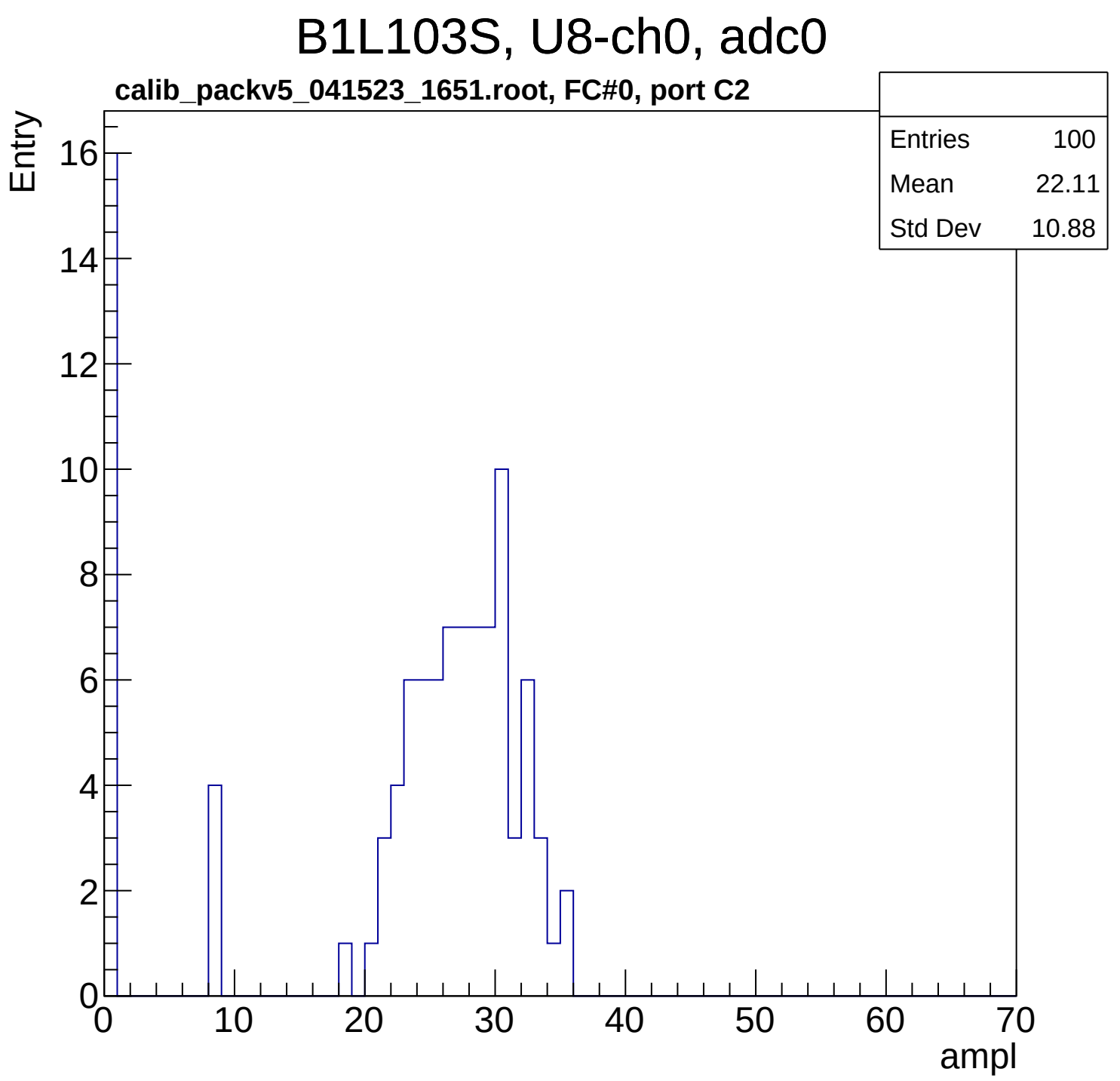
B1L103S, U8-ch0, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 100
Mean 22.11
Std Dev 10.88
Entry
0
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4
6
8
10
12
14
16
0
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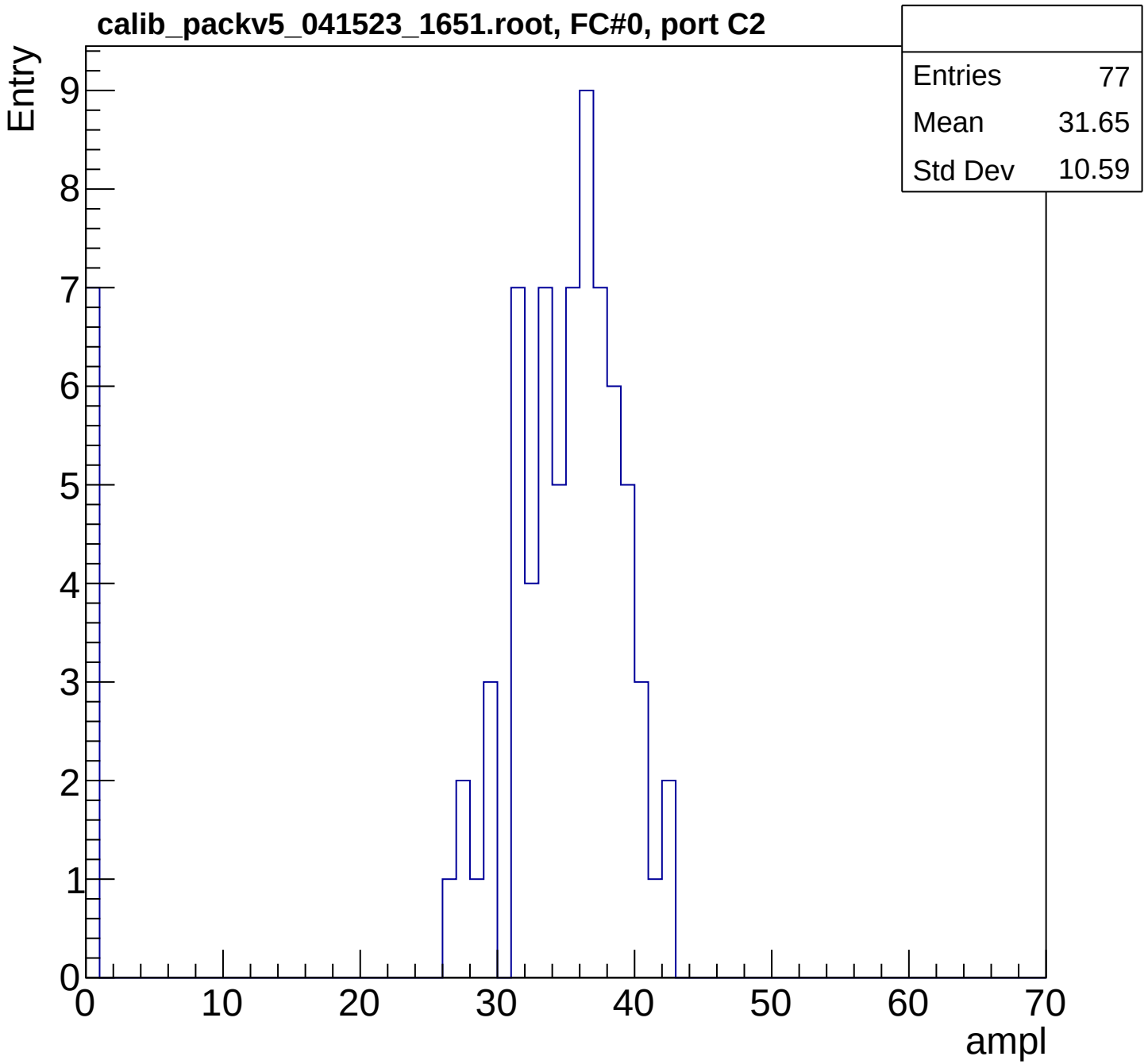
70
ampl


B1L103S, U8-ch0, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 31.65
Std Dev 10.59
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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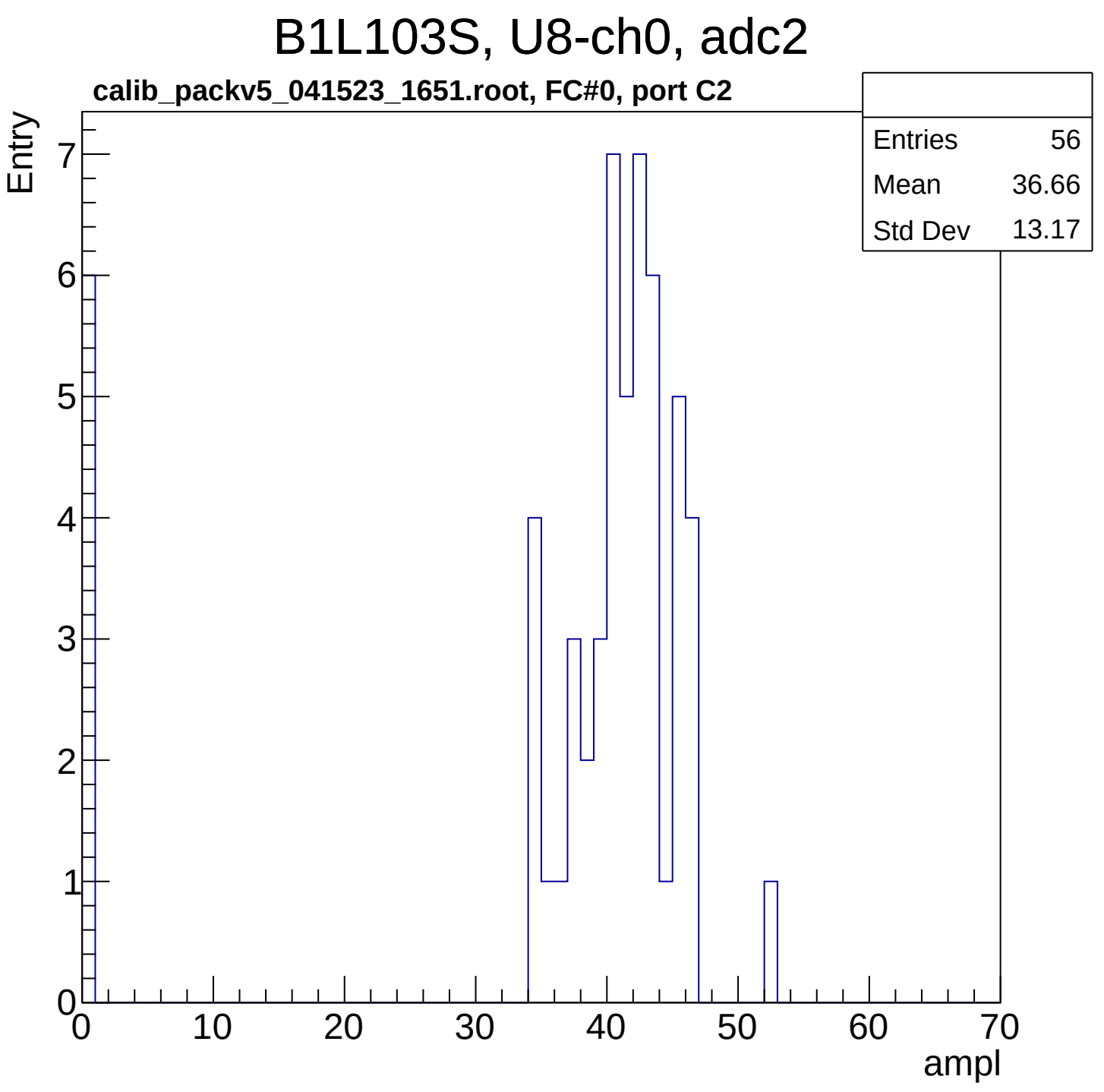
B1L103S, U8-ch0, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 36.66
Std Dev 13.17
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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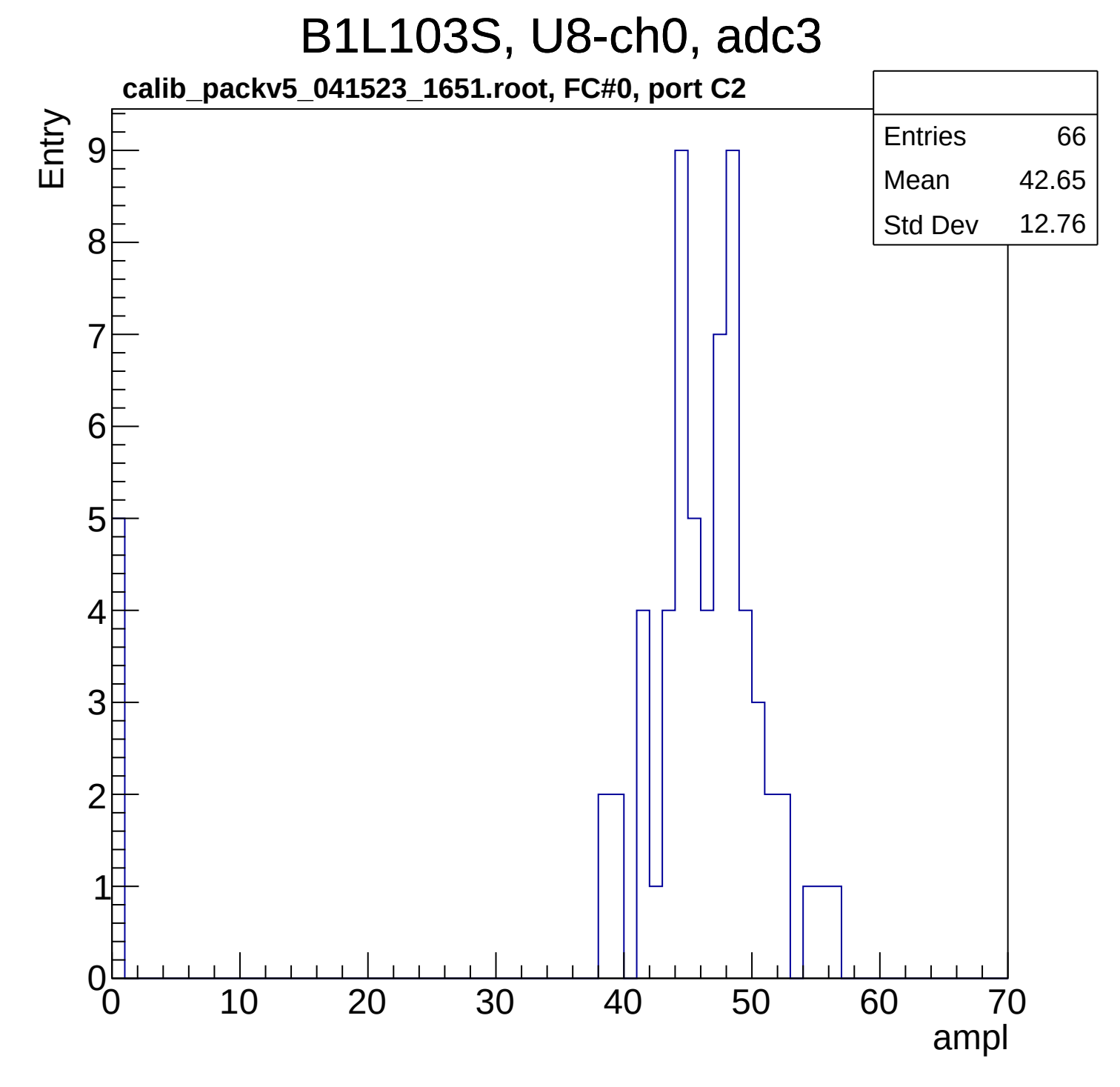
B1L103S, U8-ch0, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 42.65
Std Dev 12.76
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
30
40
50
60
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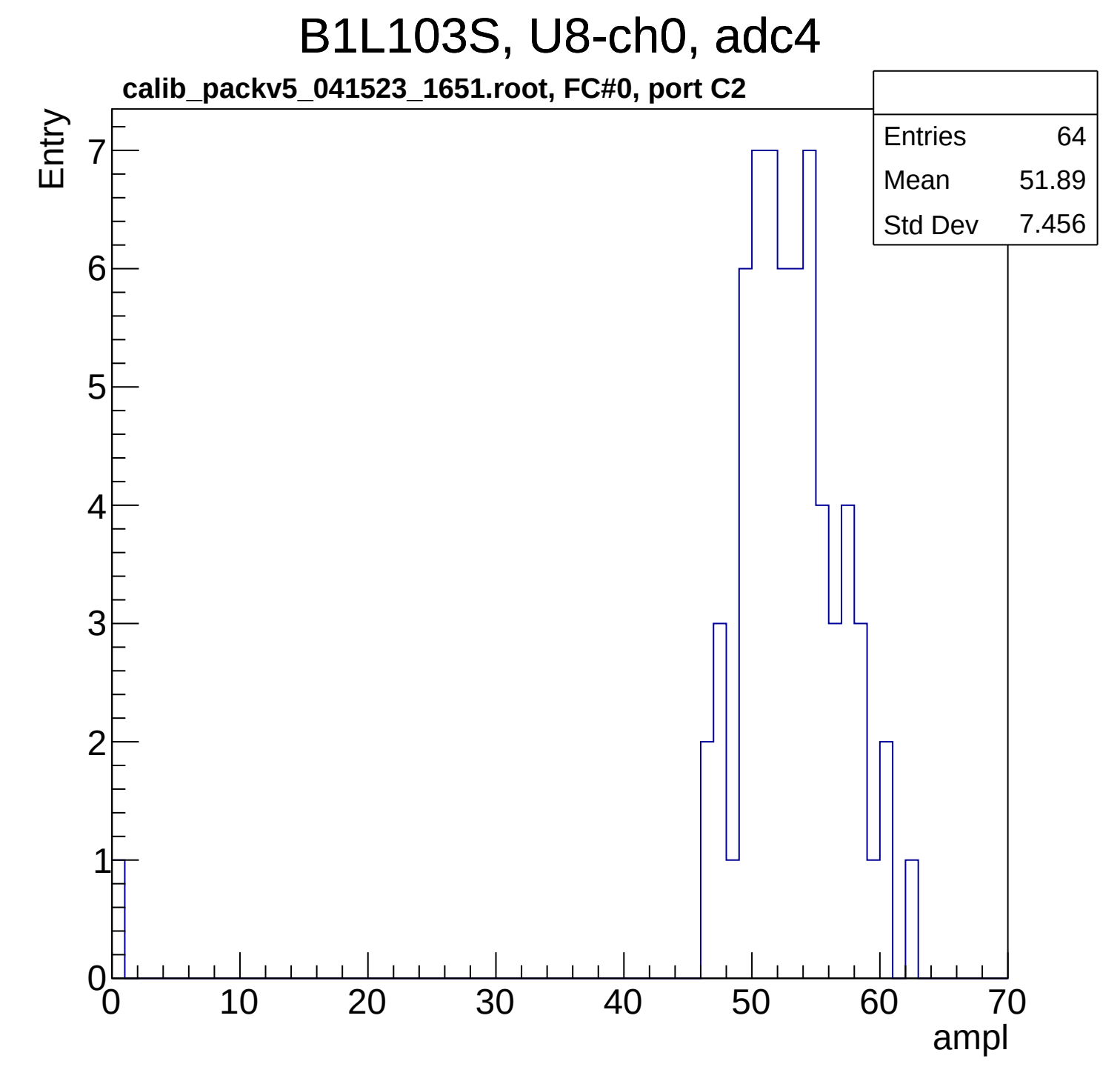
B1L103S, U8-ch0, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 51.89
Std Dev 7.456
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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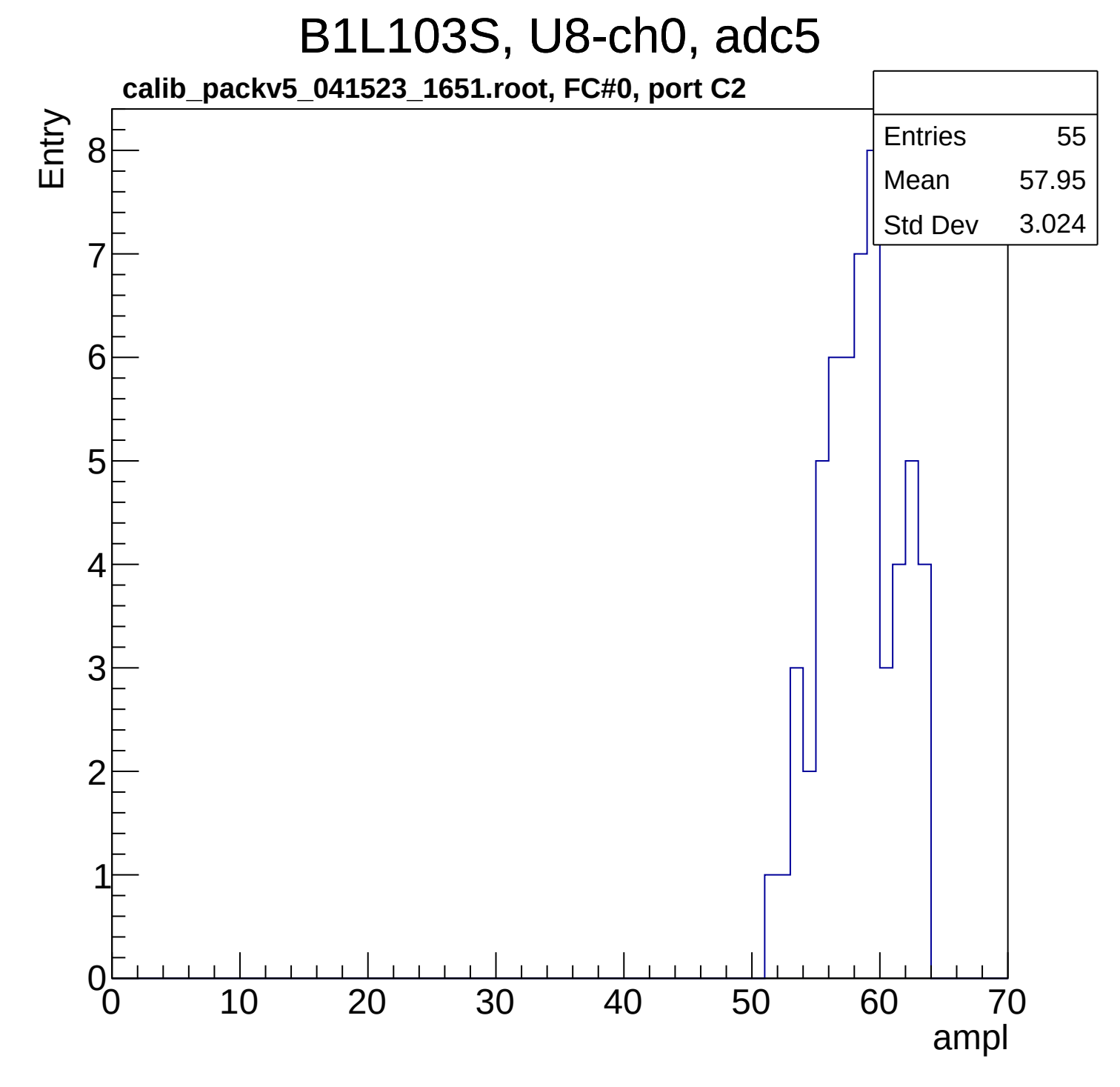
B1L103S, U8-ch0, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 57.95
Std Dev 3.024
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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40
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60
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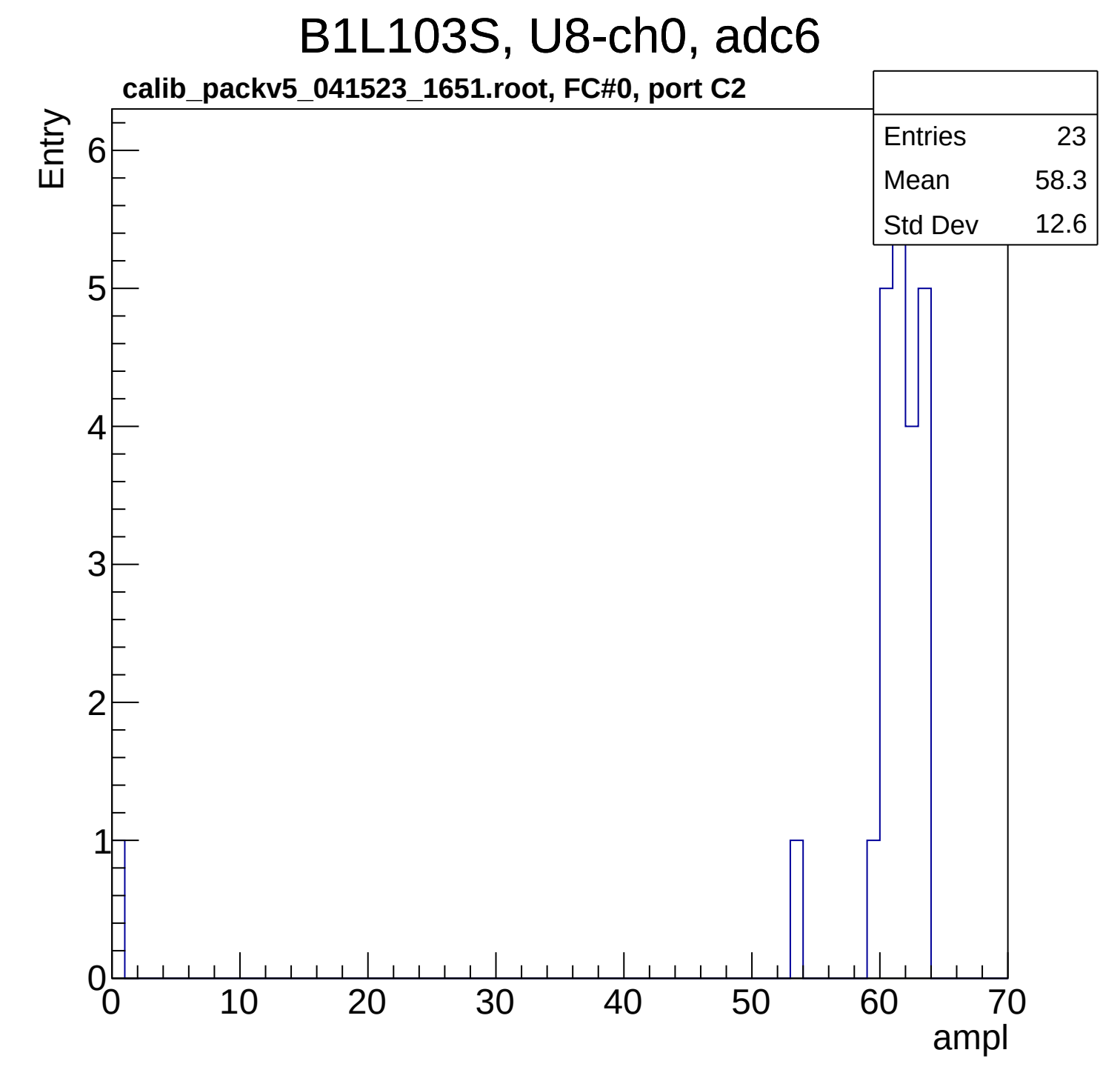
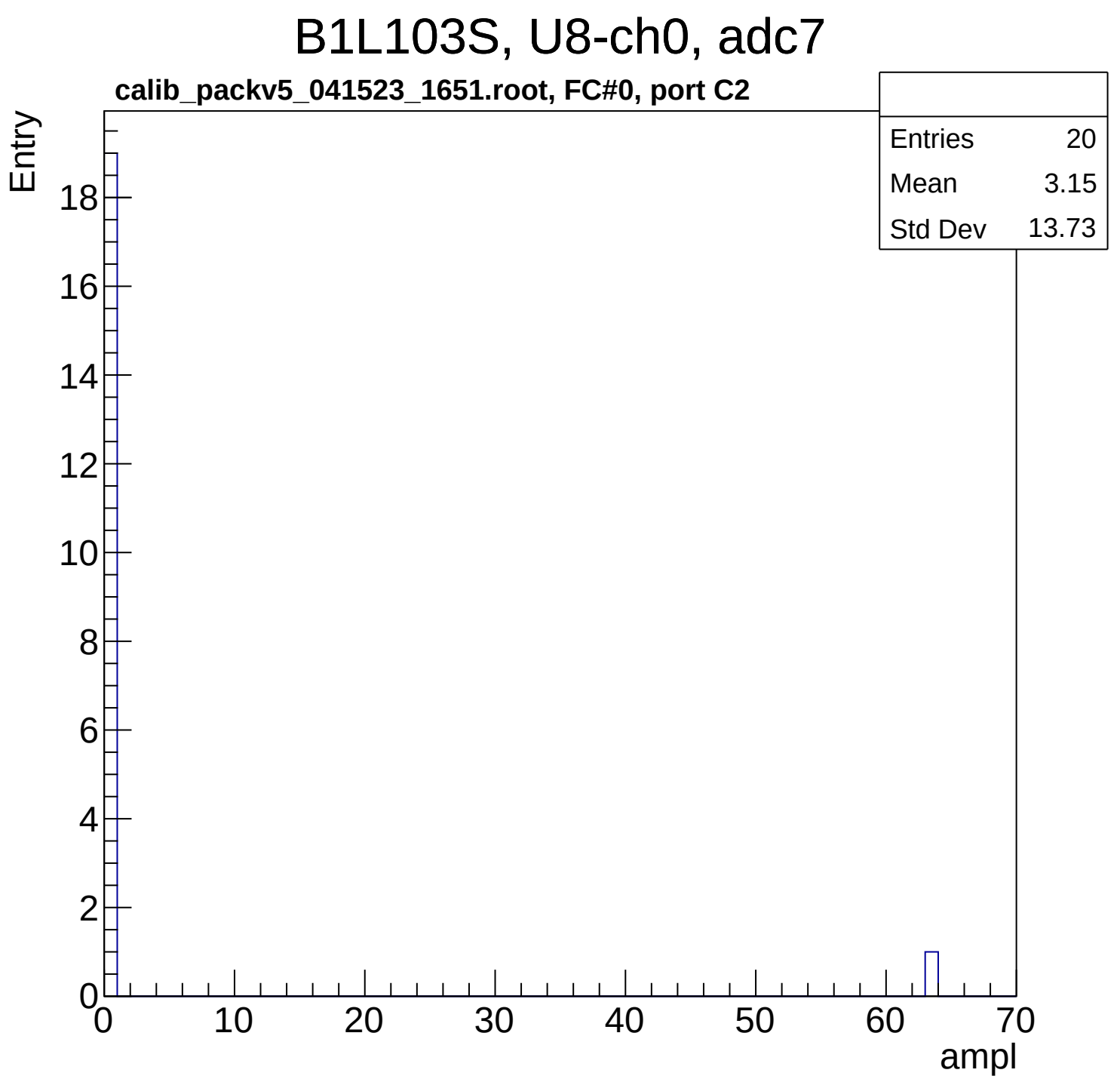

B1L103S, U8-ch0, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 58.3
Std Dev 12.6
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U8-ch0, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
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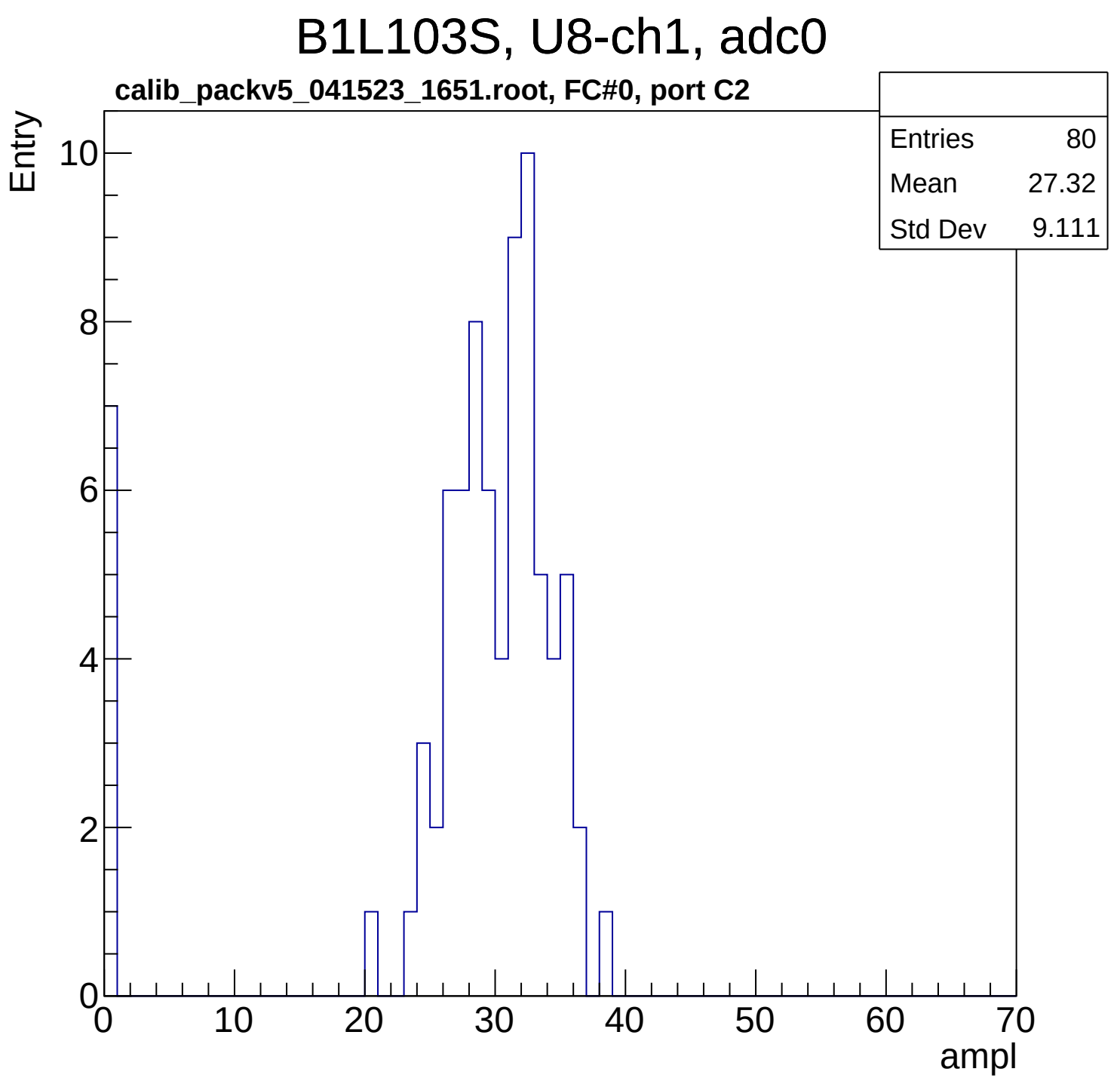
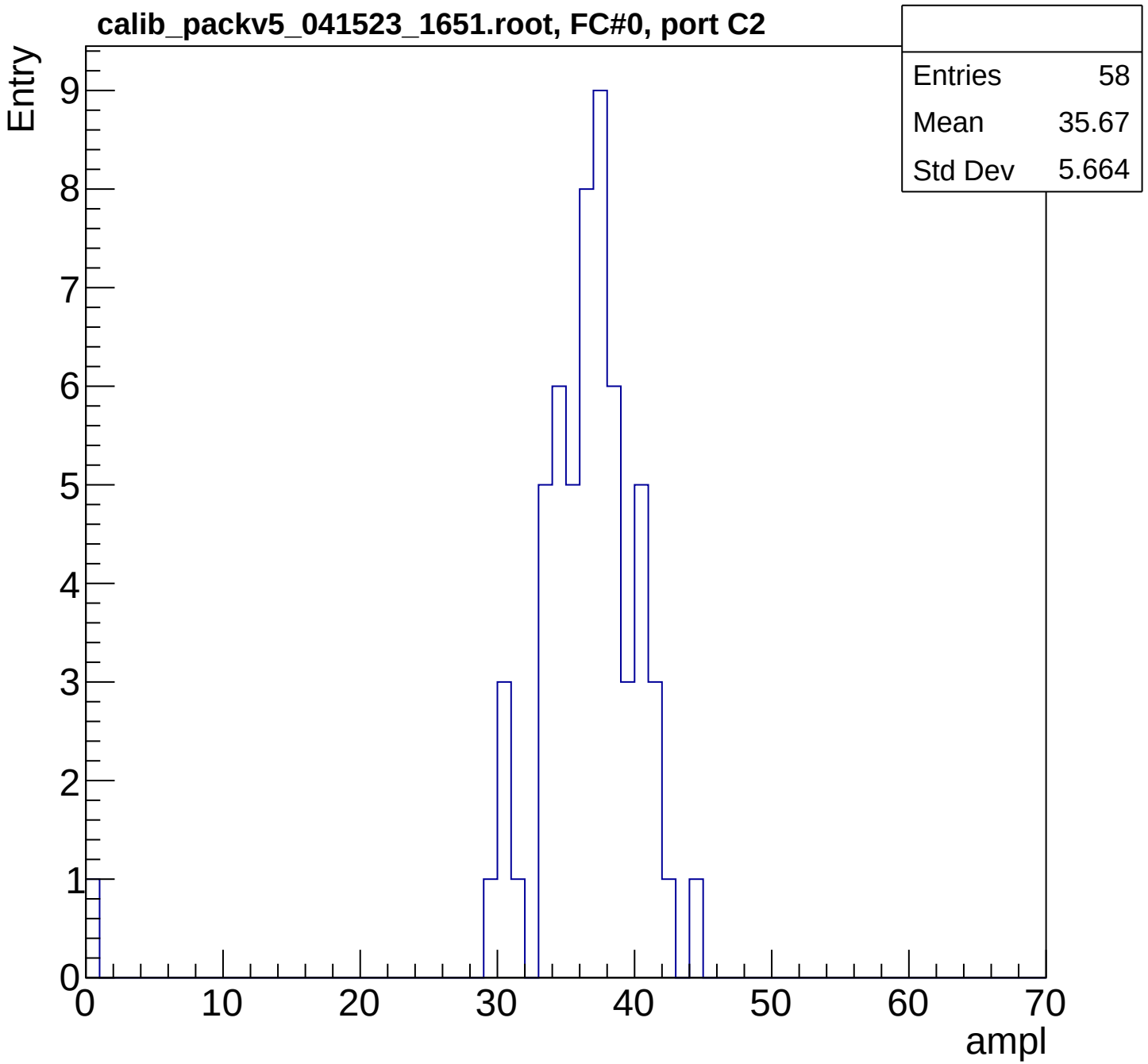
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch1, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 27.32
Std Dev 9.111
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U8-ch1, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 35.67
Std Dev 5.664
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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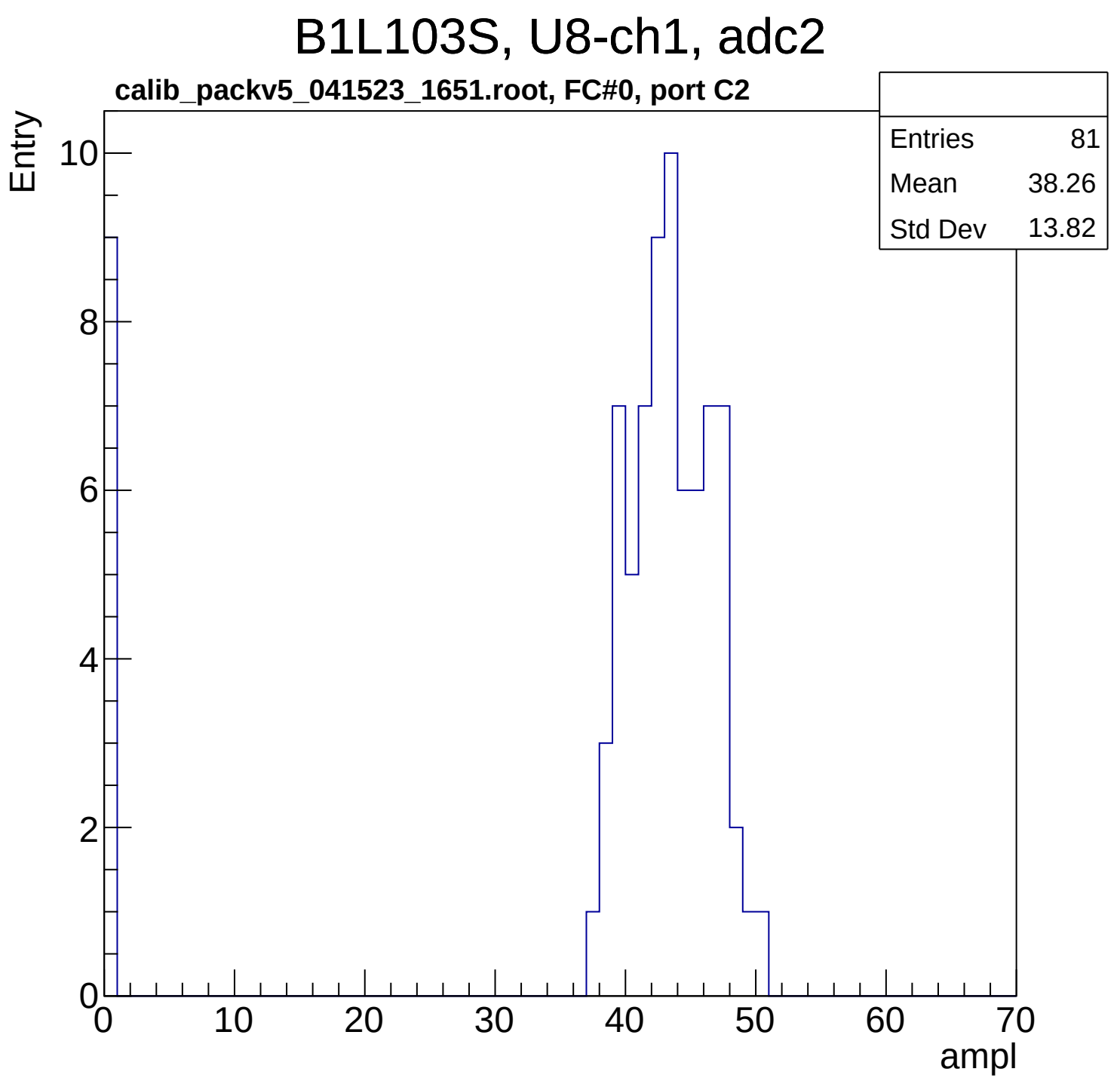
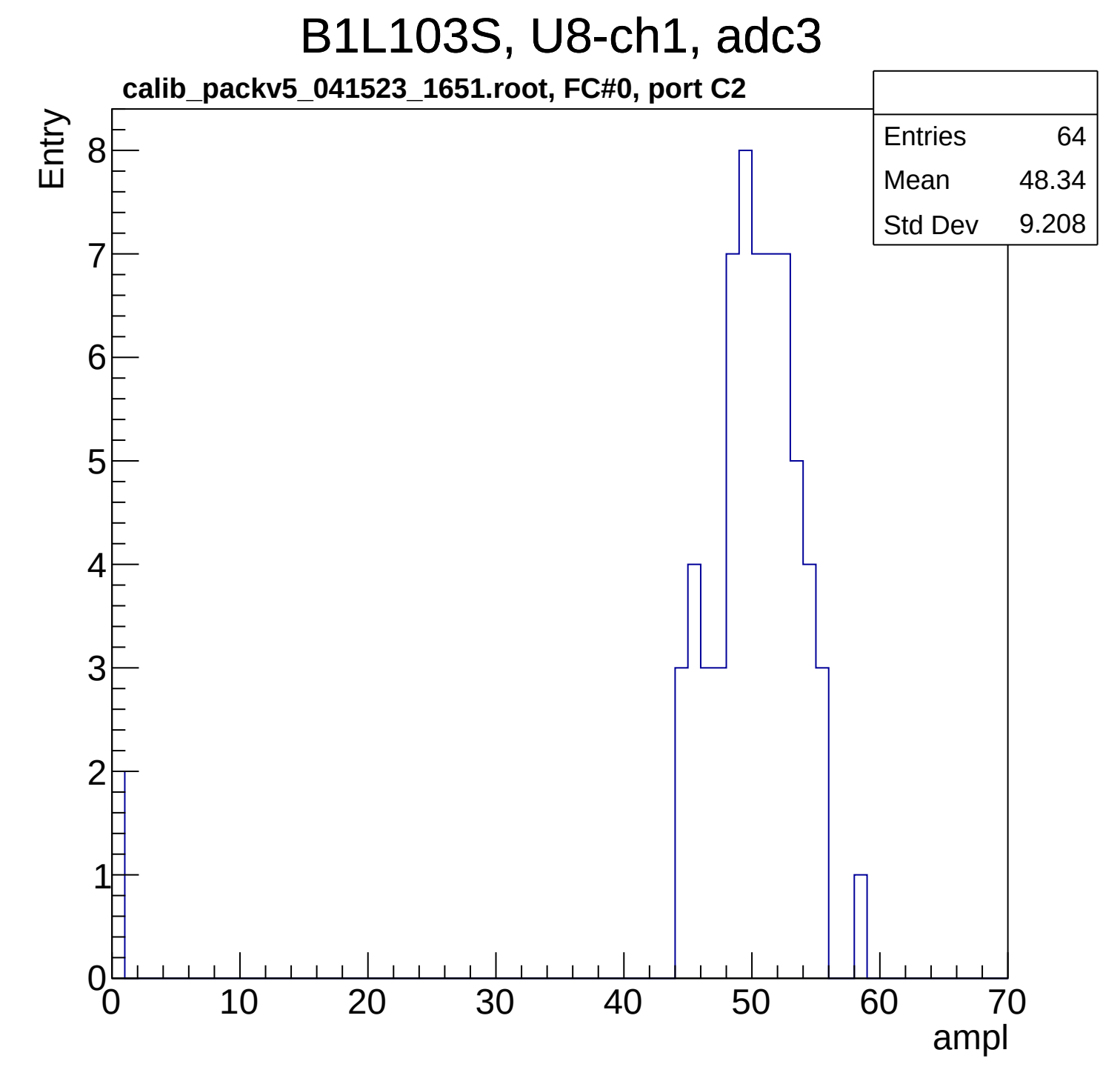

B1L103S, U8-ch1, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 38.26
Std Dev 13.82
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U8-ch1, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 48.34
Std Dev 9.208
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
50
60
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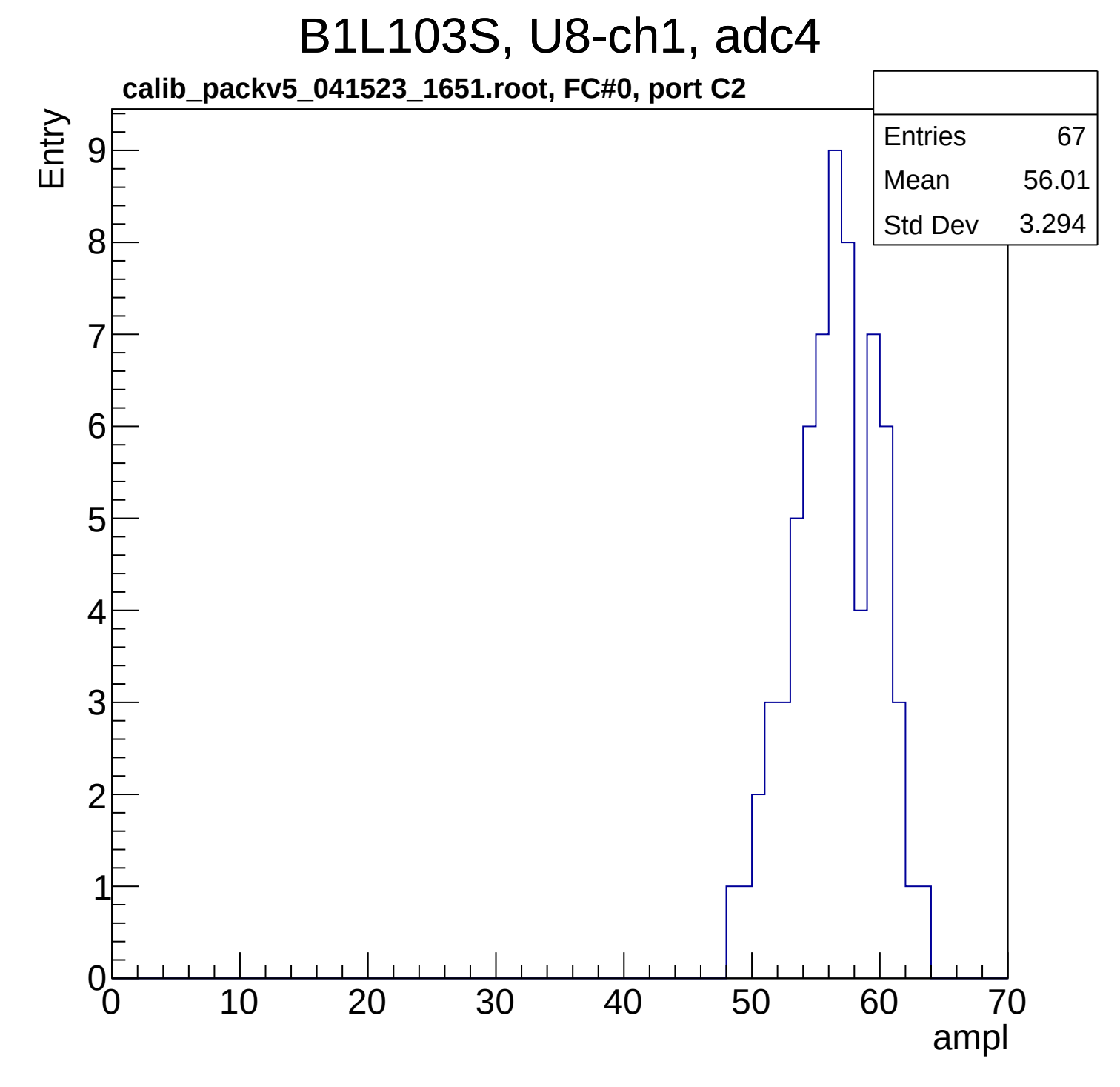
B1L103S, U8-ch1, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 56.01
Std Dev 3.294
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
30
40
50
60
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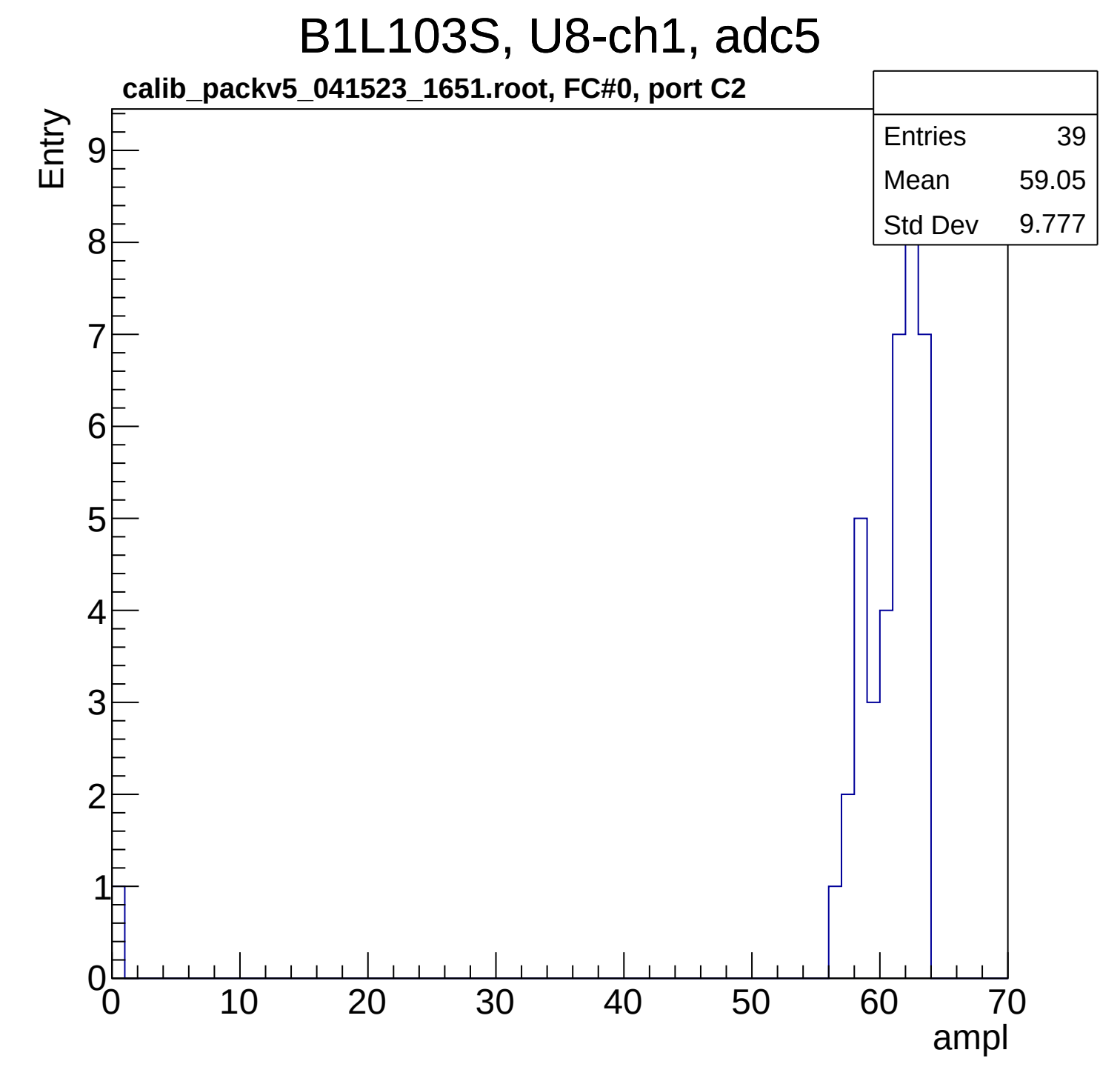
B1L103S, U8-ch1, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 59.05
Std Dev 9.777
Entry
ampl
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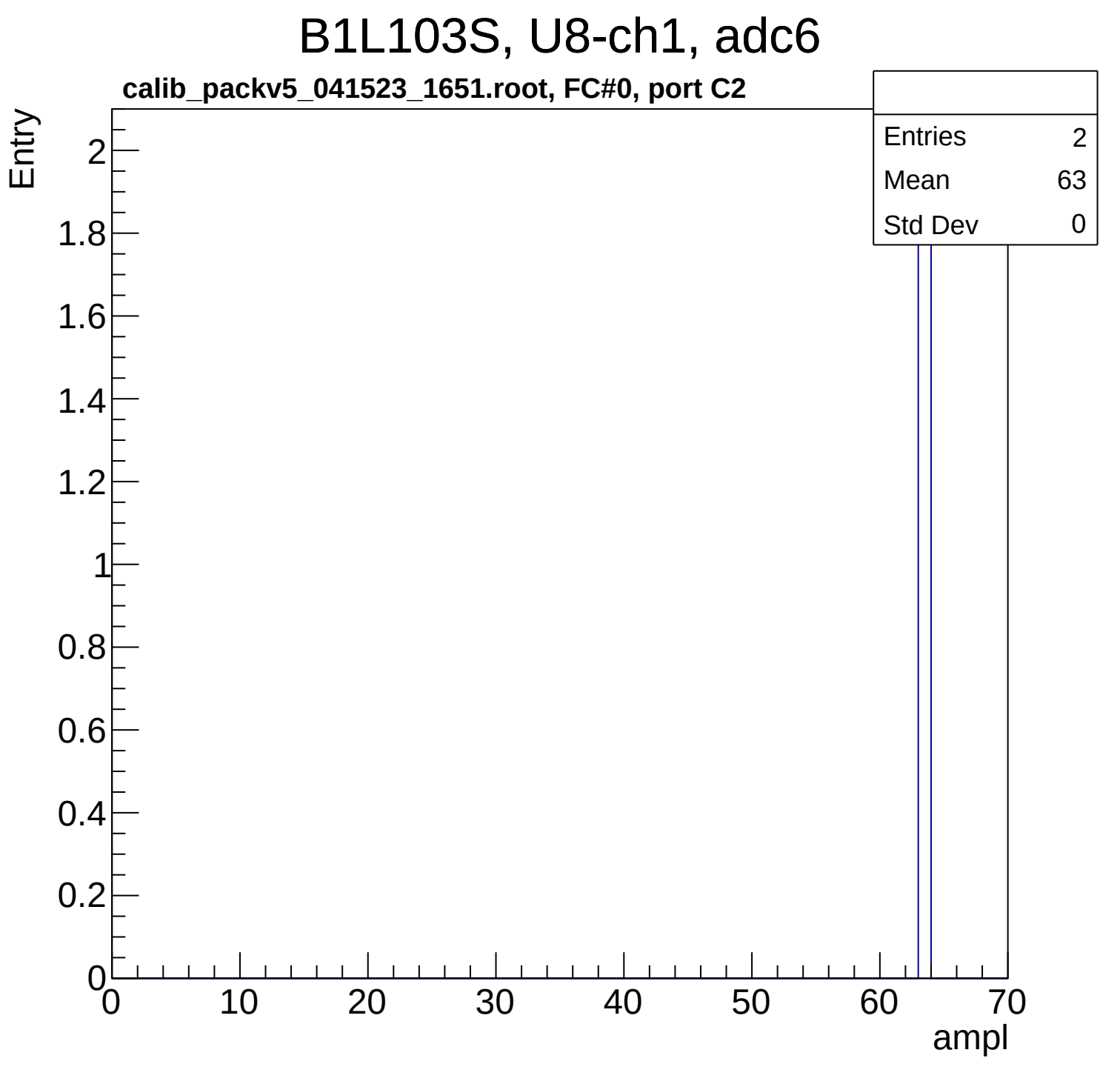
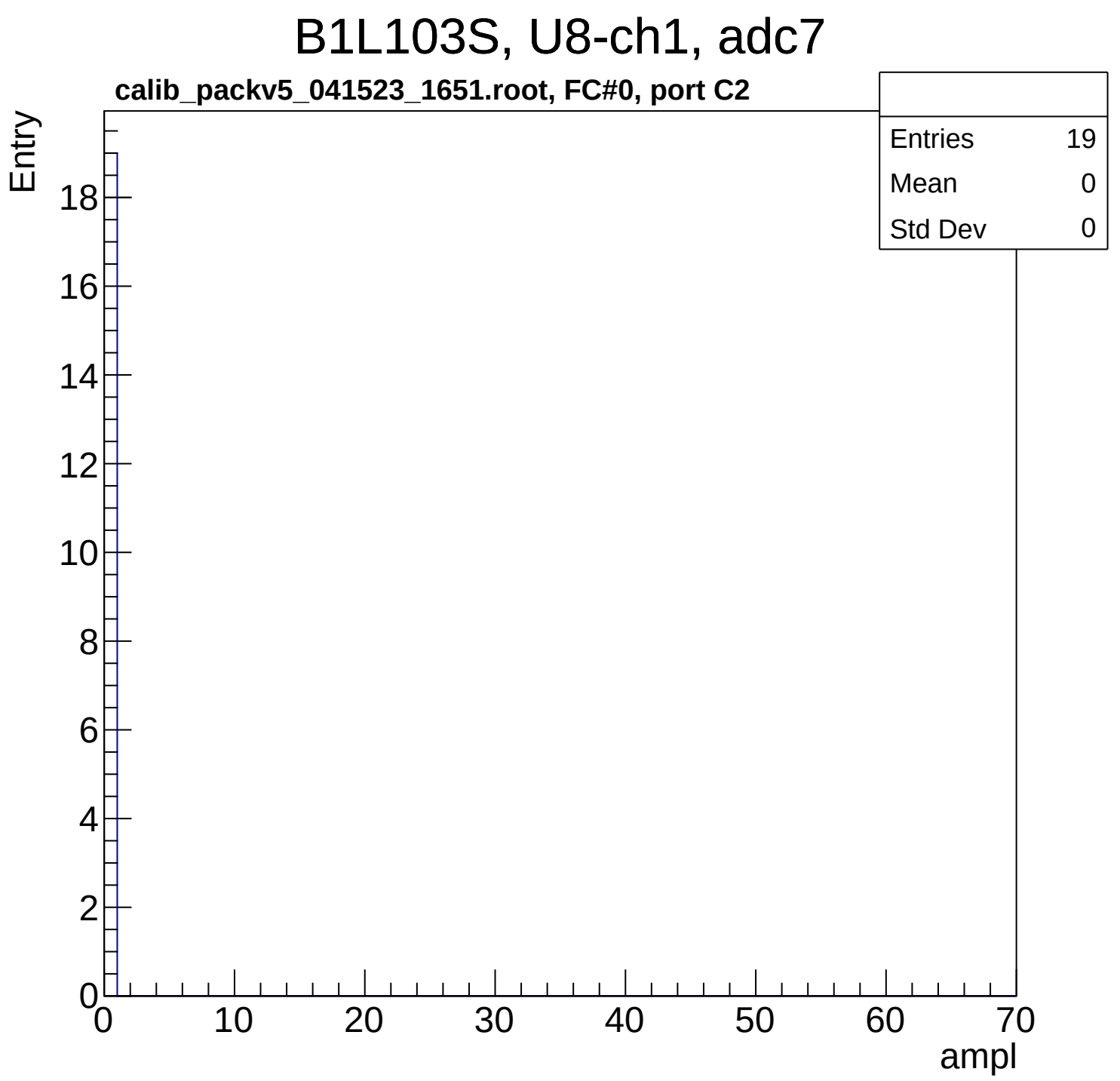
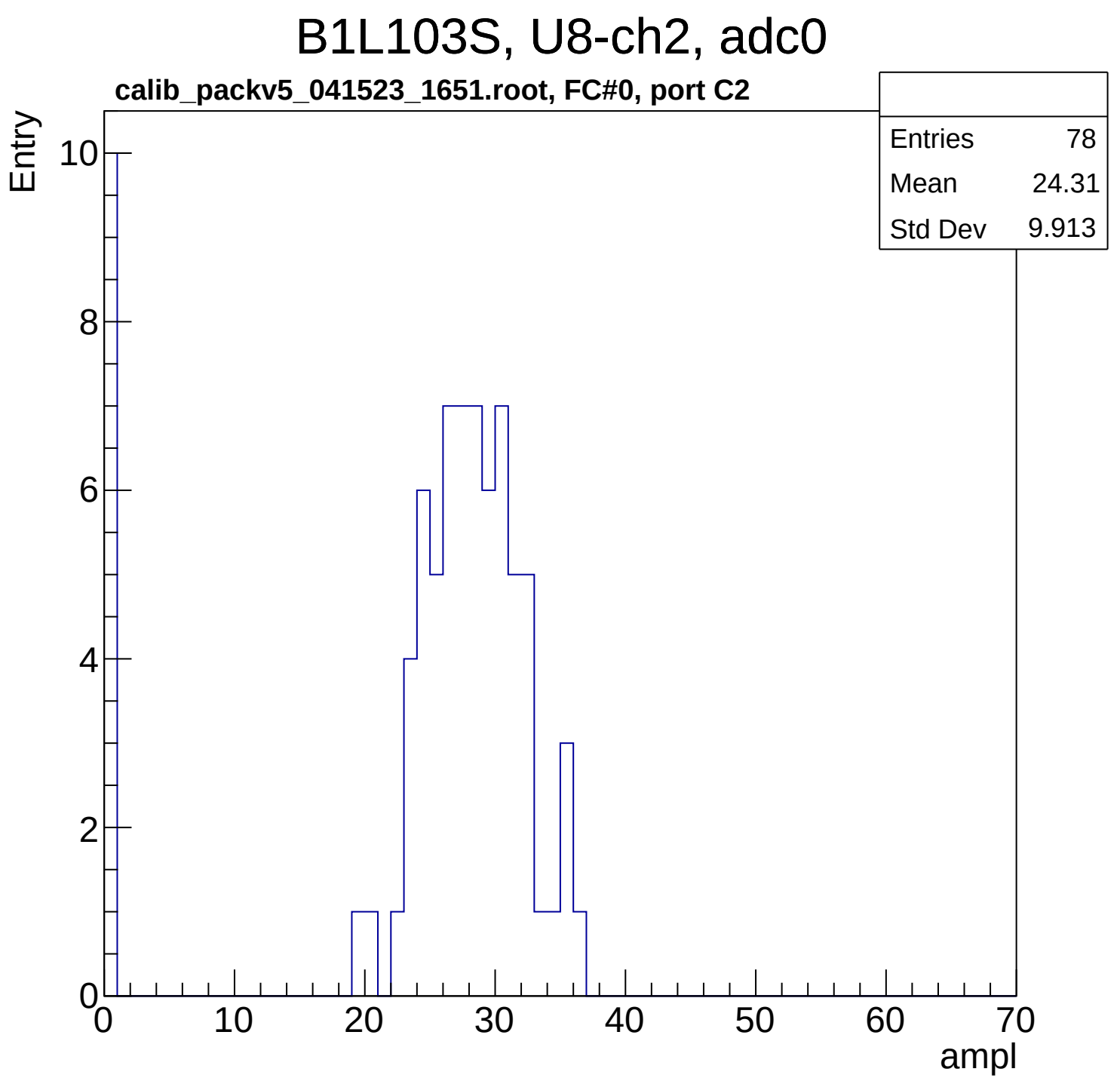
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U8-ch1, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 63
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U8-ch1, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch2, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 24.31
Std Dev 9.913
Entry
ampl
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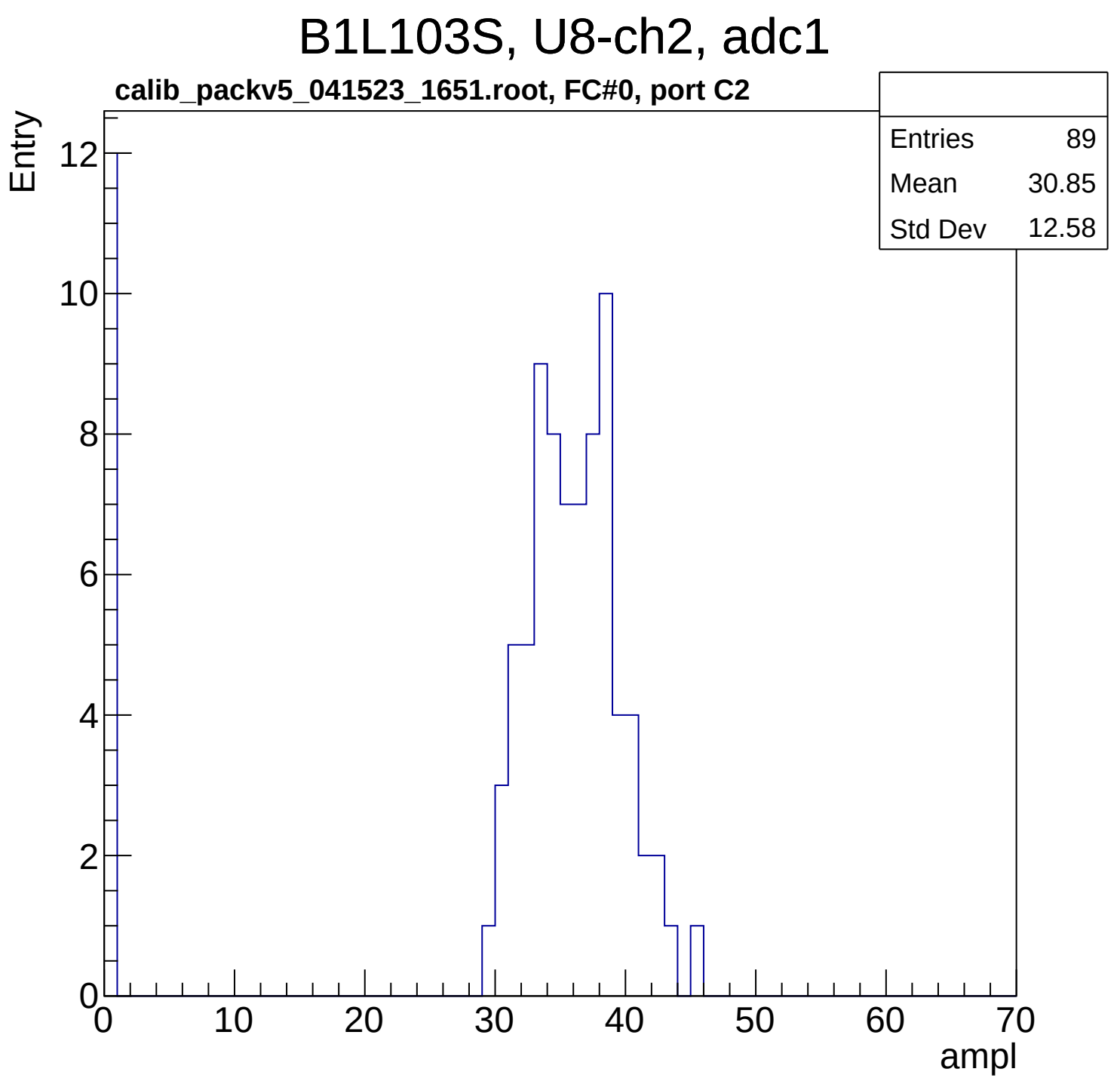
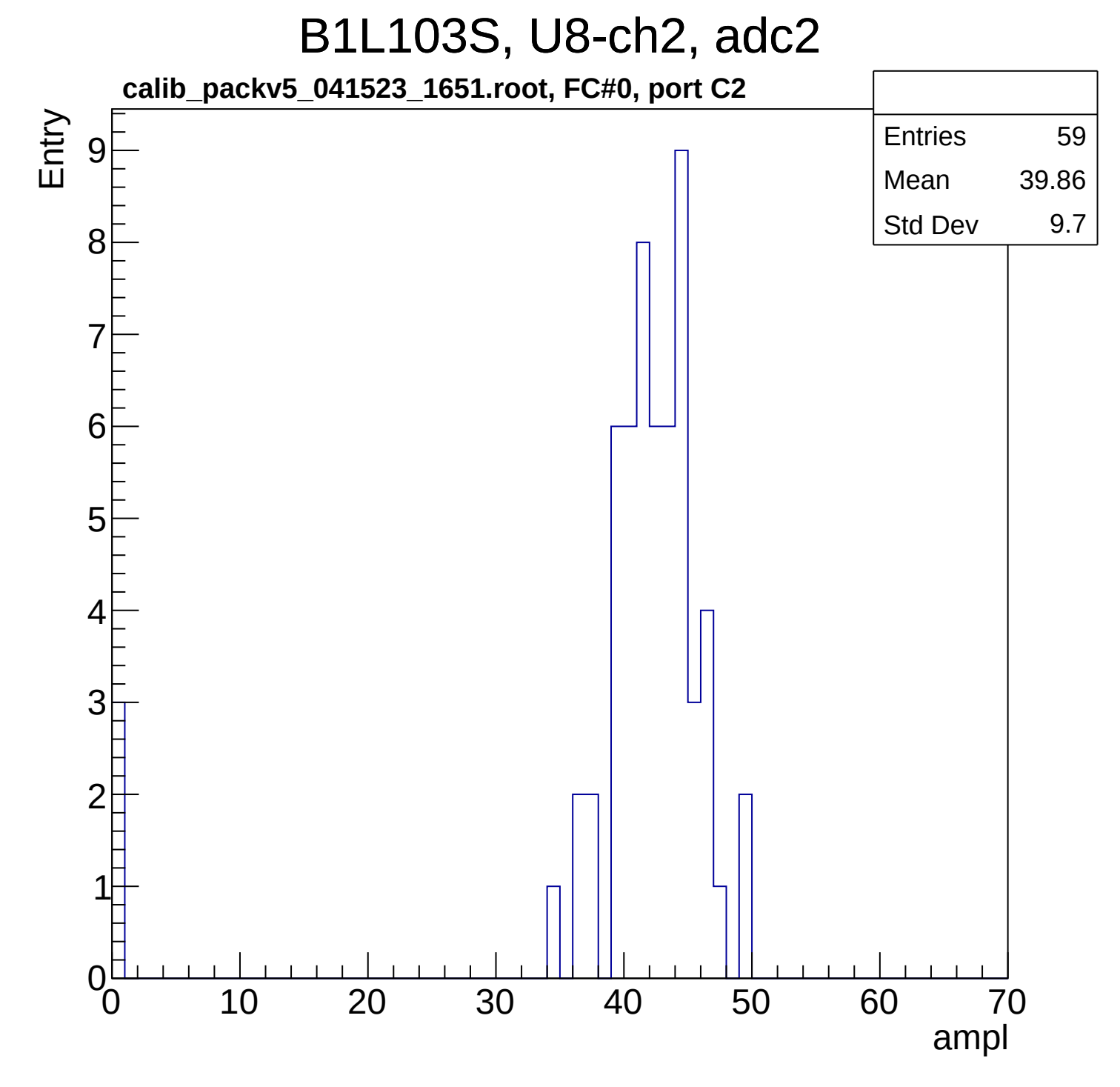
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U8-ch2, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 30.85
Std Dev 12.58
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch2, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 39.86
Std Dev 9.7
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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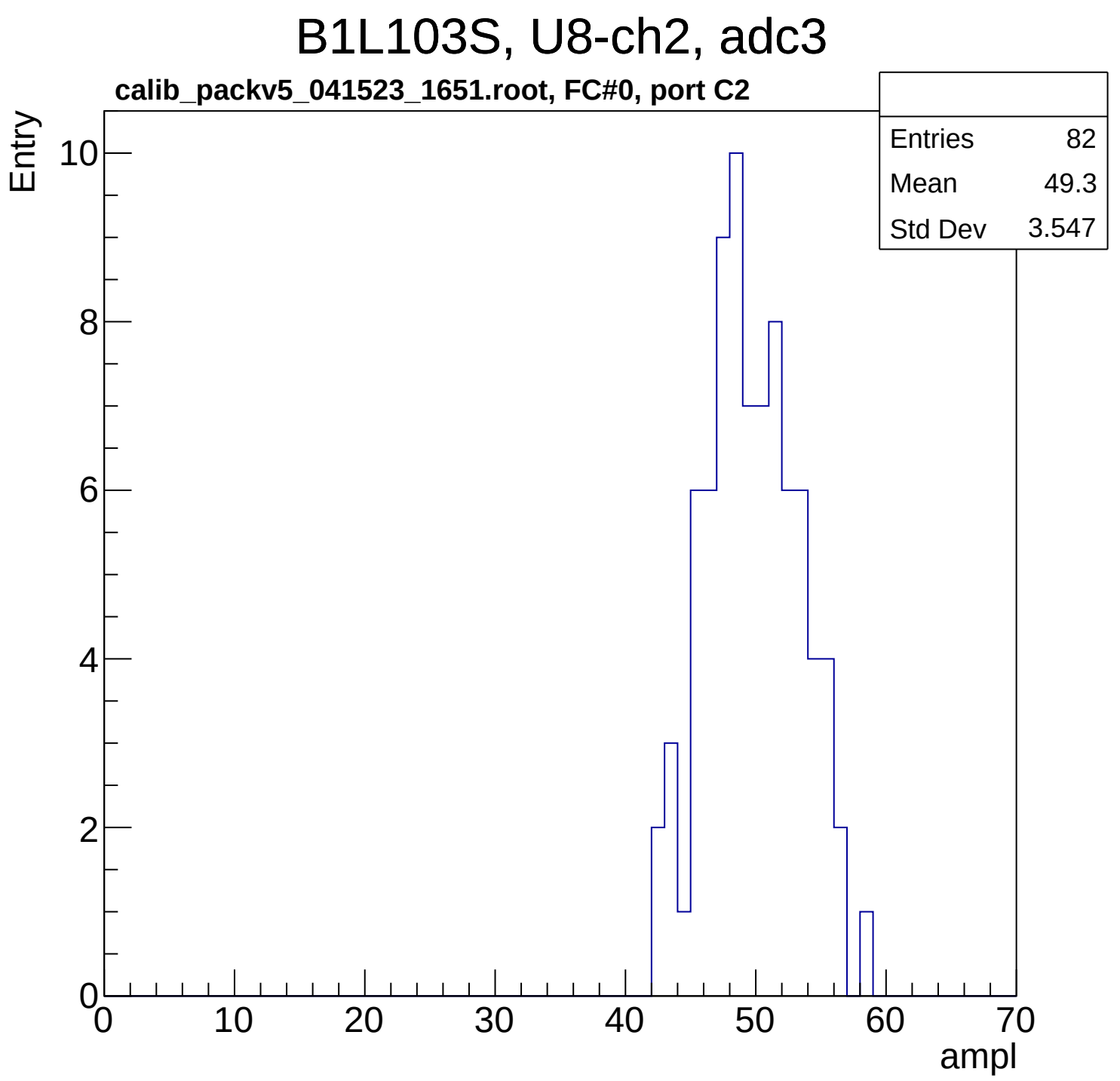
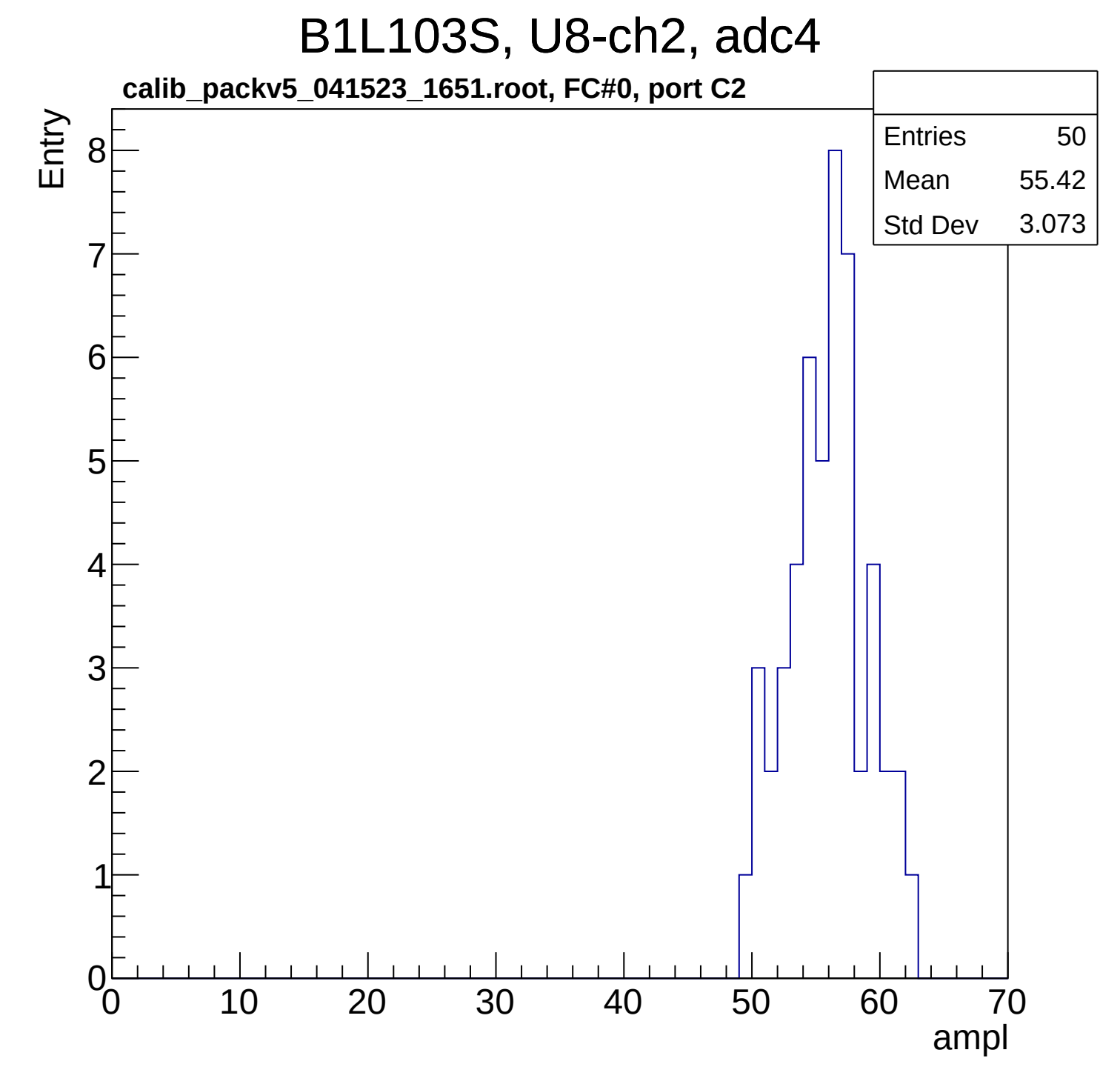
20
30
40
50
60
70


B1L103S, U8-ch2, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 49.3
Std Dev 3.547
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch2, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 55.42
Std Dev 3.073
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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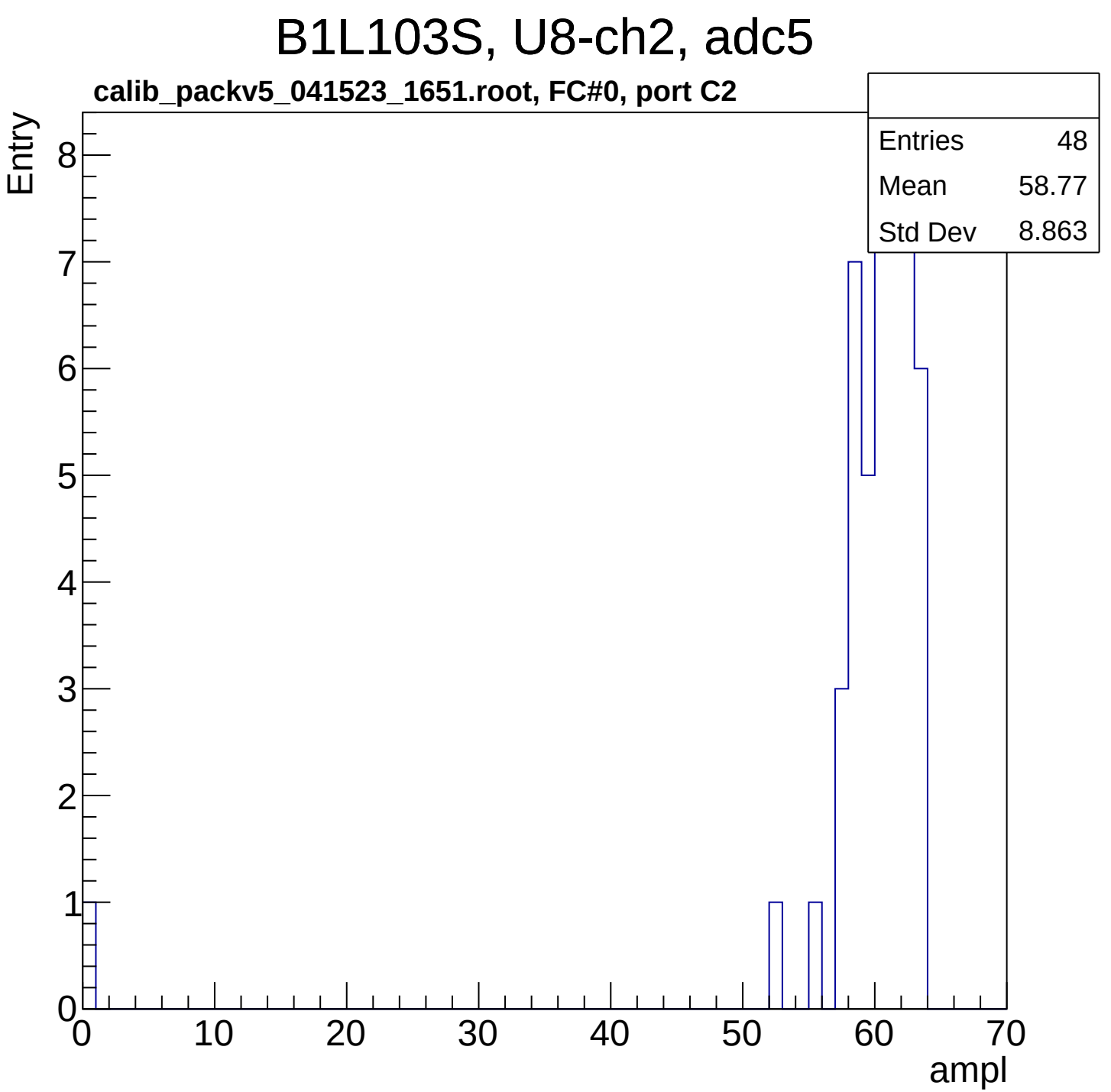
40
50
60
70


B1L103S, U8-ch2, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 58.77
Std Dev 8.863
Entry
ampl
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1
2
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4
5
6
7
8
0
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60
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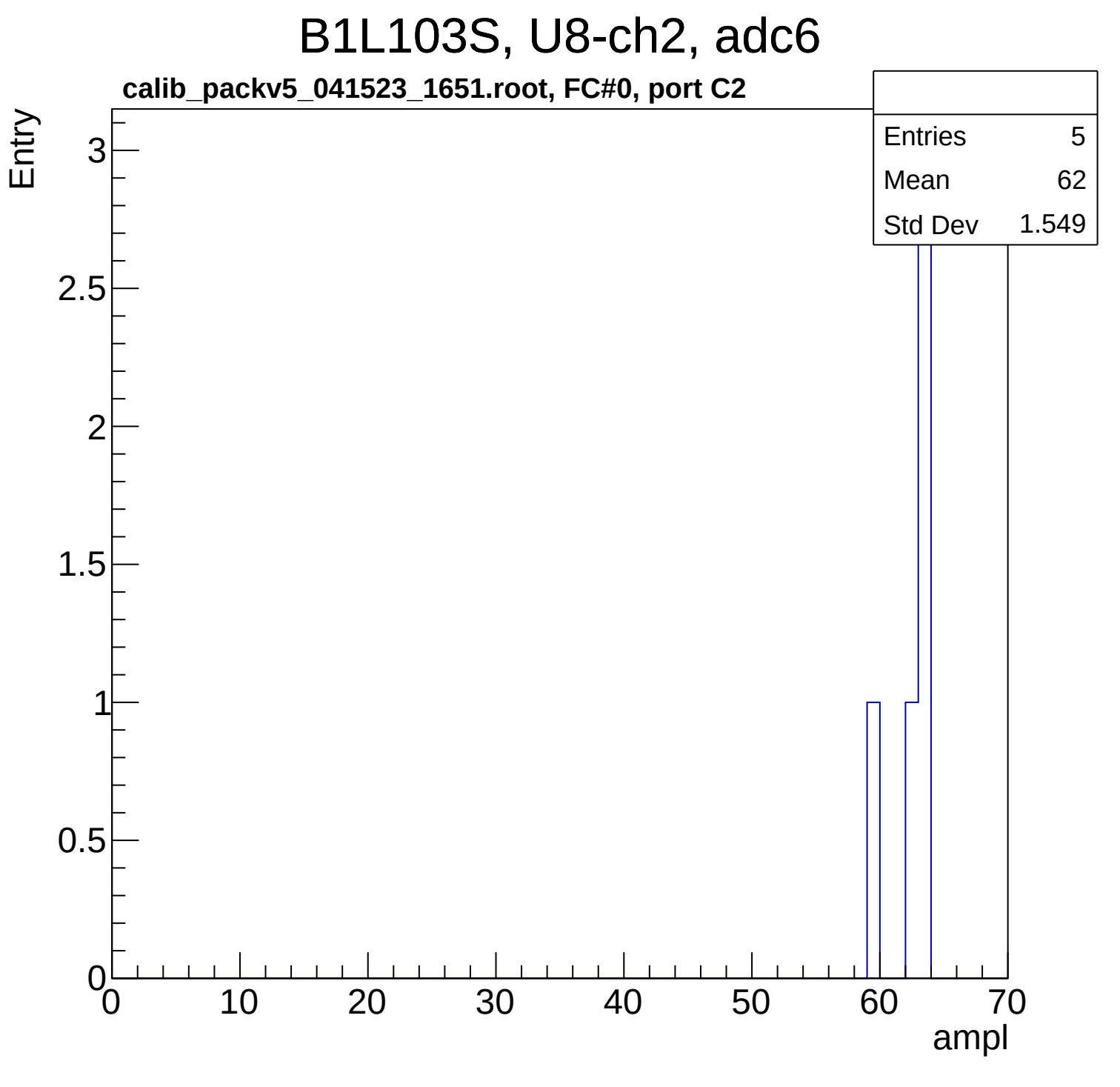
B1L103S, U8-ch2, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 62
Std Dev 1.549
Entry
ampl
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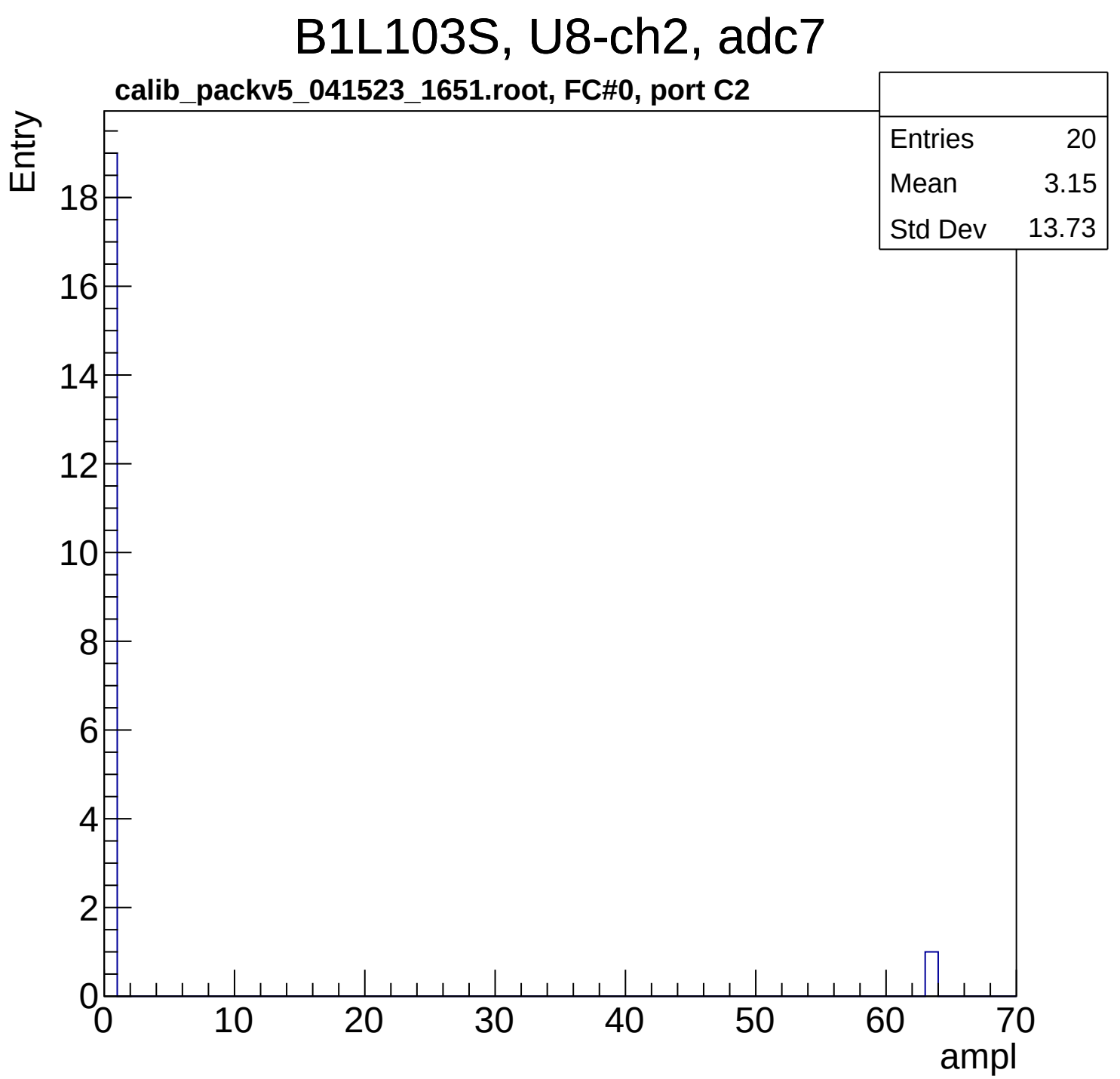
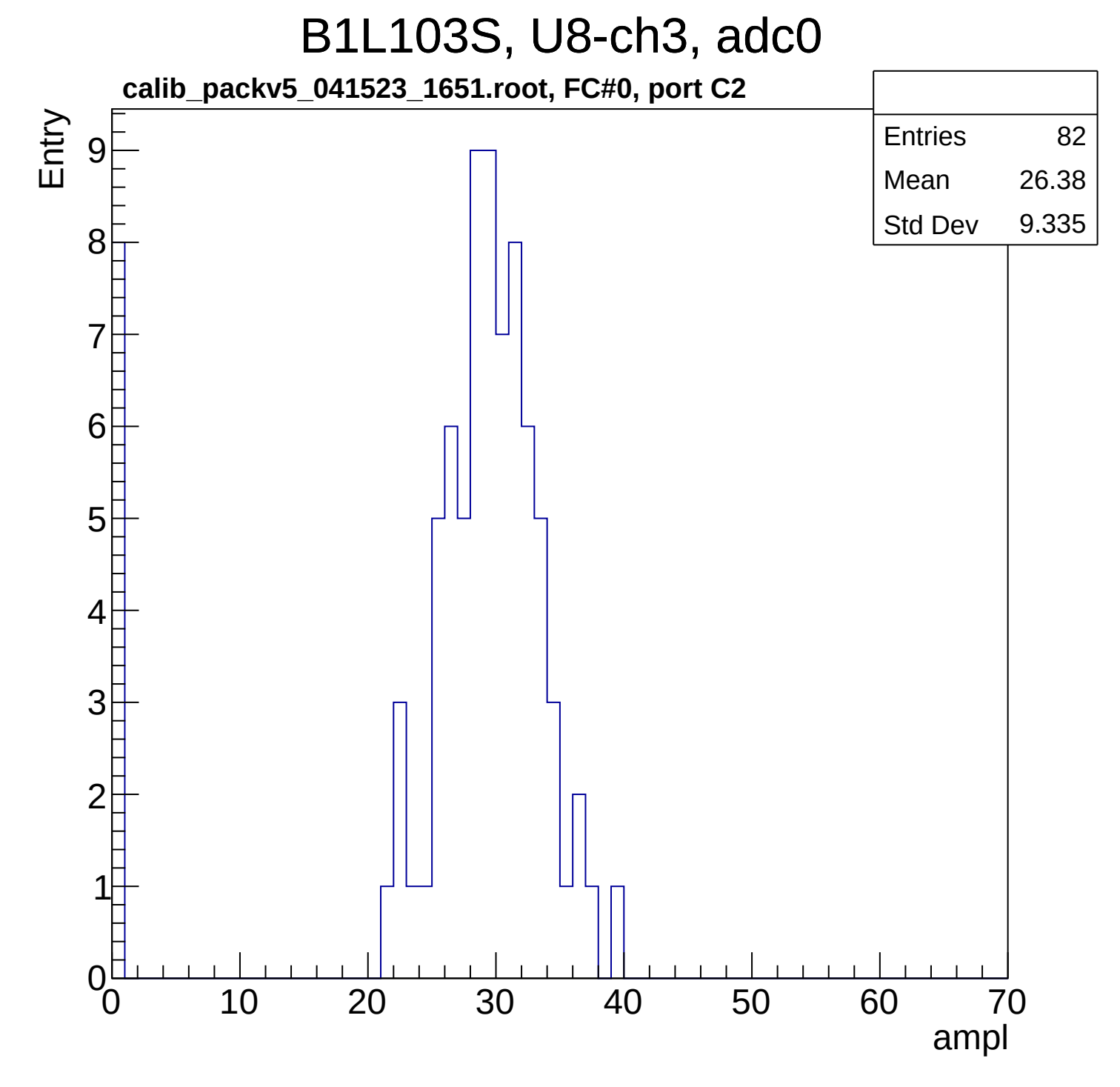
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U8-ch2, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch3, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 26.38
Std Dev 9.335
Entry
ampl
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3
4
5
6
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8
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0
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60
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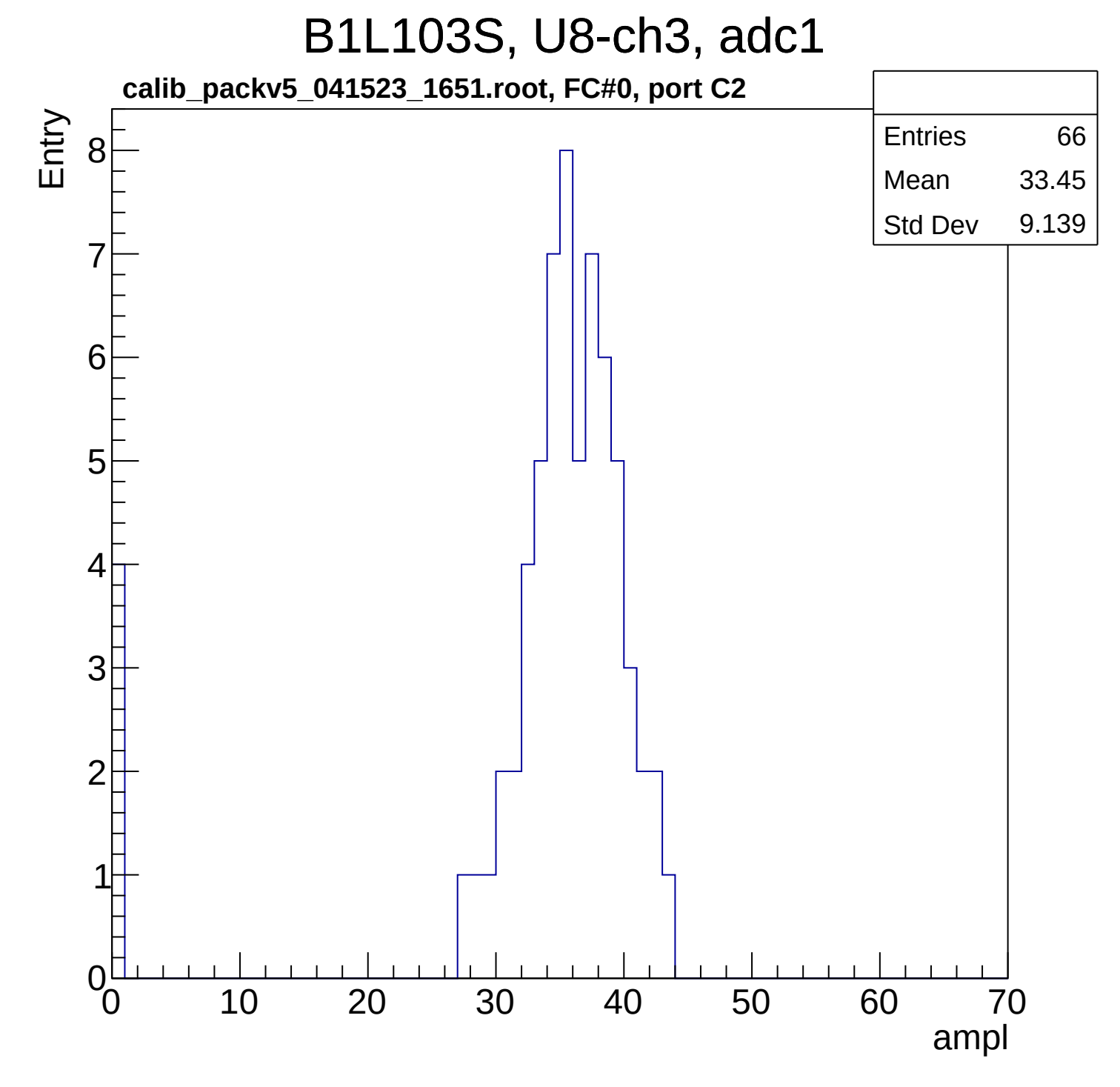
B1L103S, U8-ch3, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 33.45
Std Dev 9.139
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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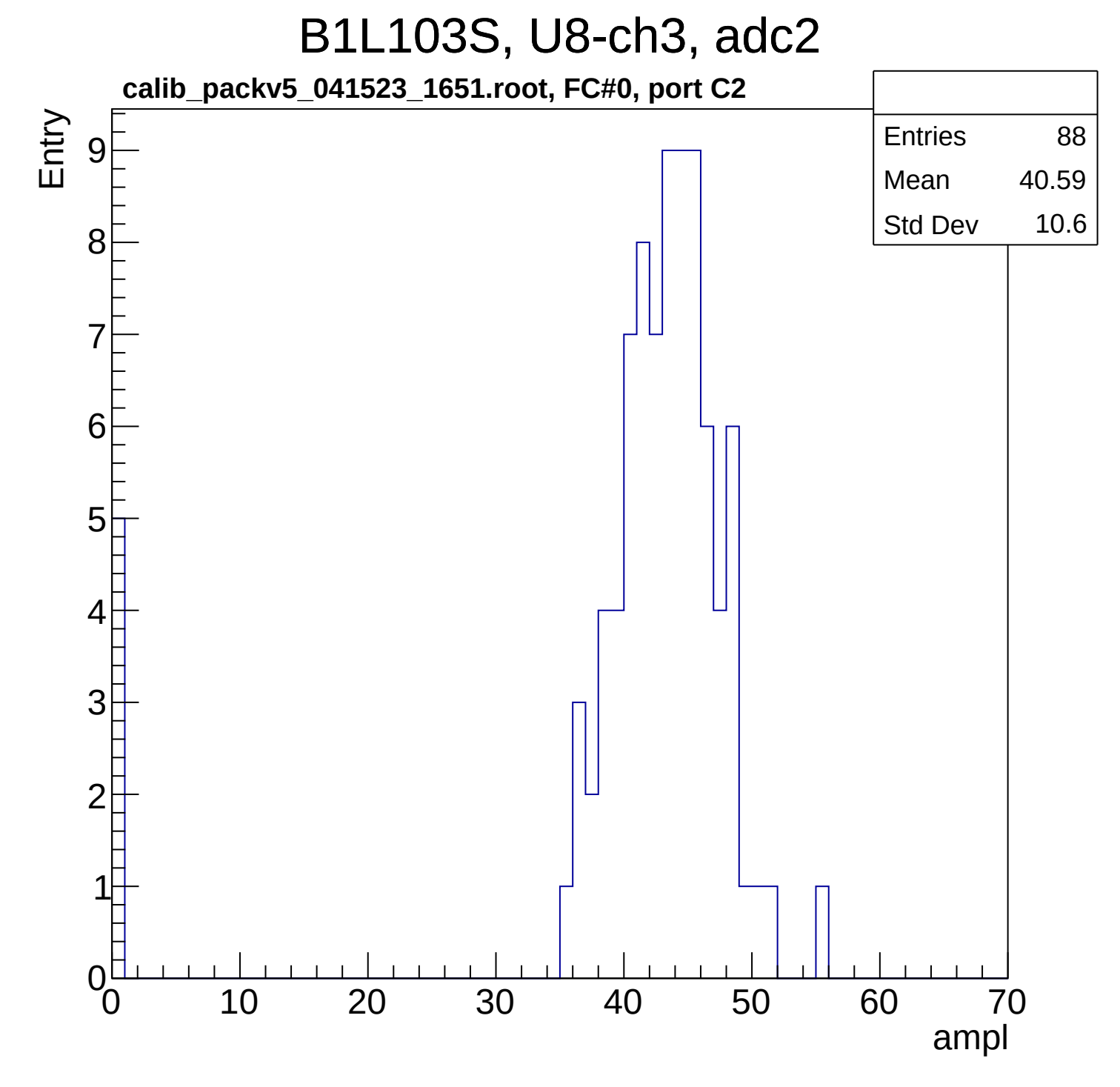
B1L103S, U8-ch3, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 40.59
Std Dev 10.6
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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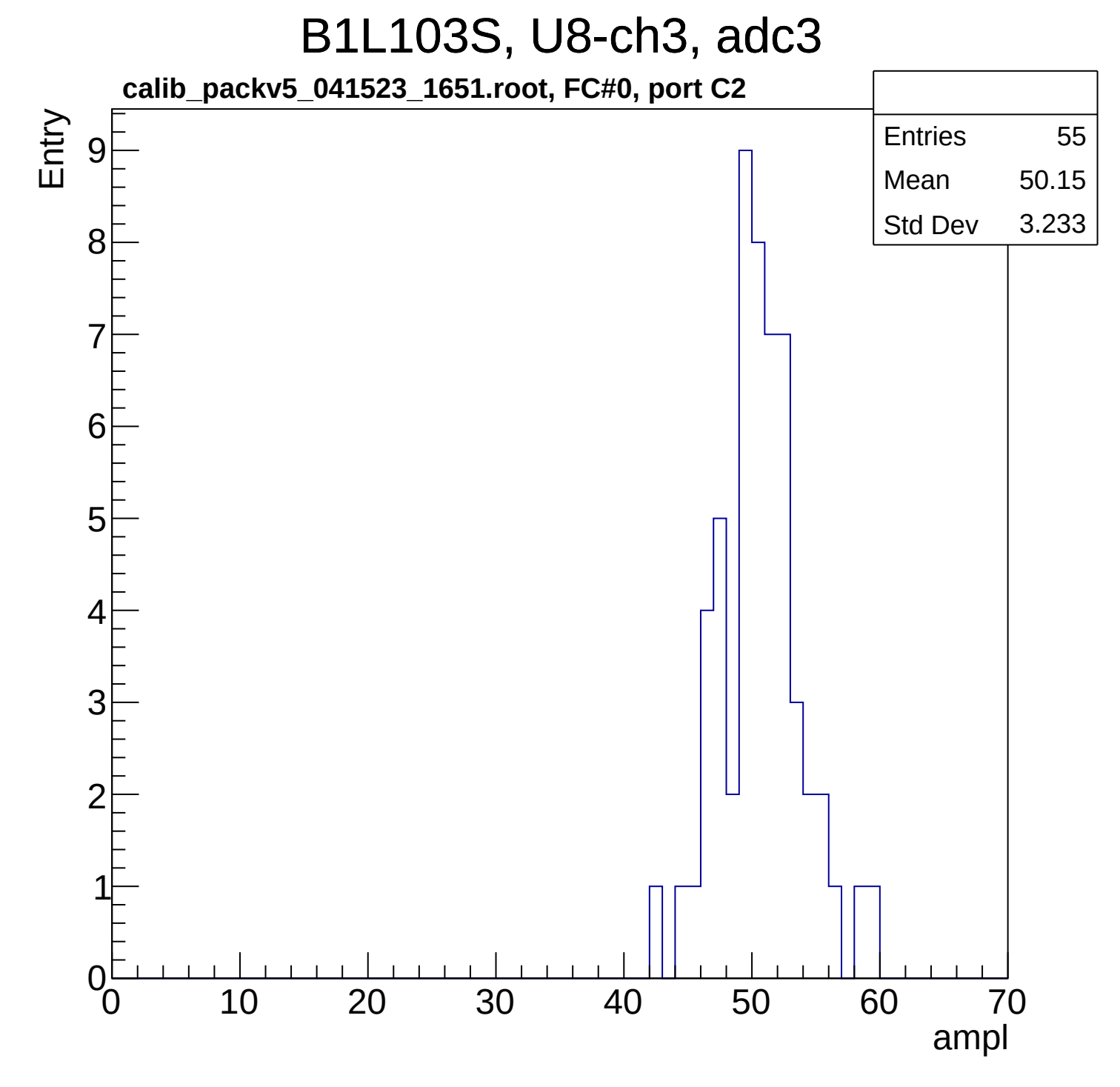
40
50
60
70


B1L103S, U8-ch3, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 50.15
Std Dev 3.233
Entry
ampl
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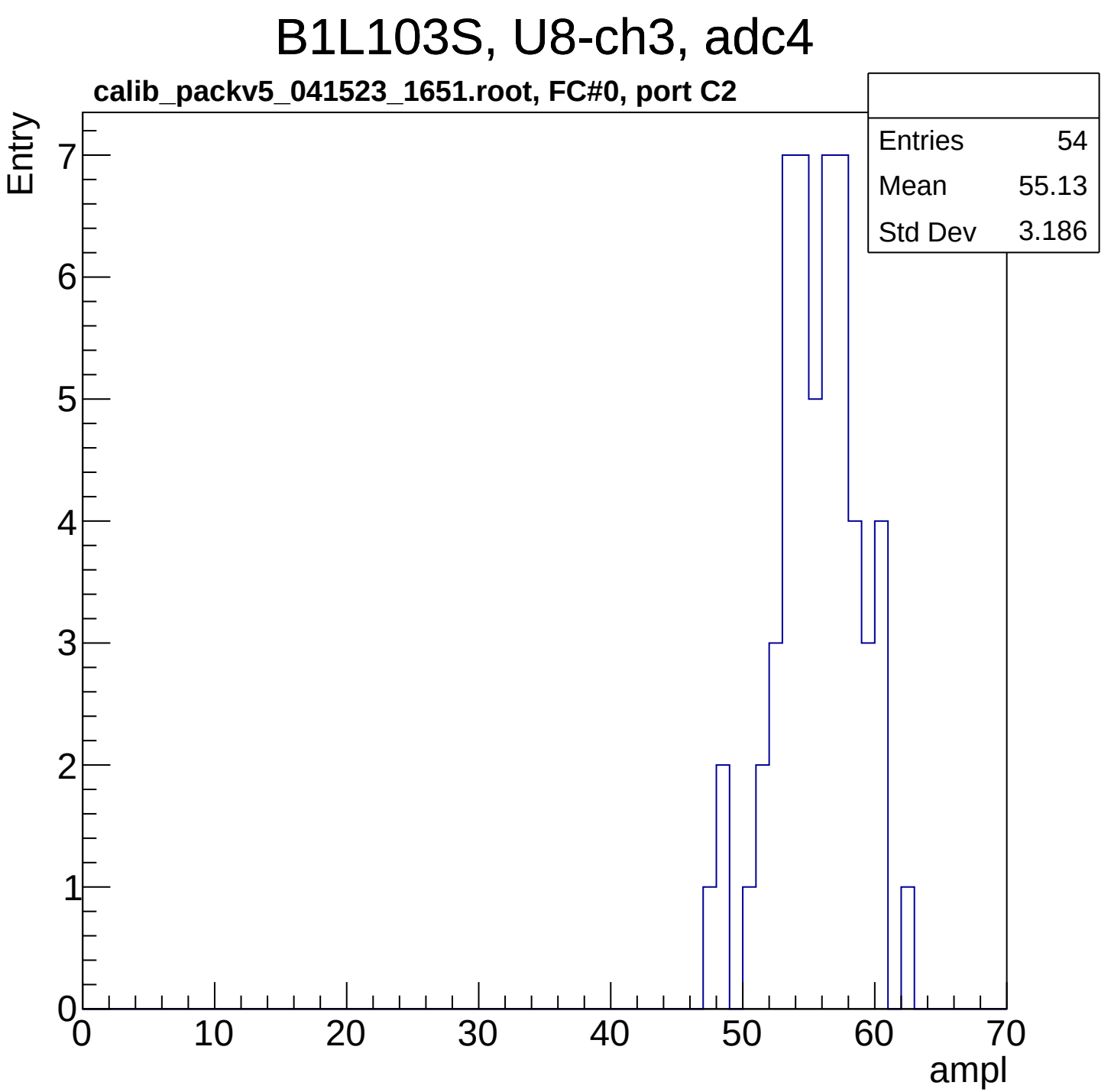
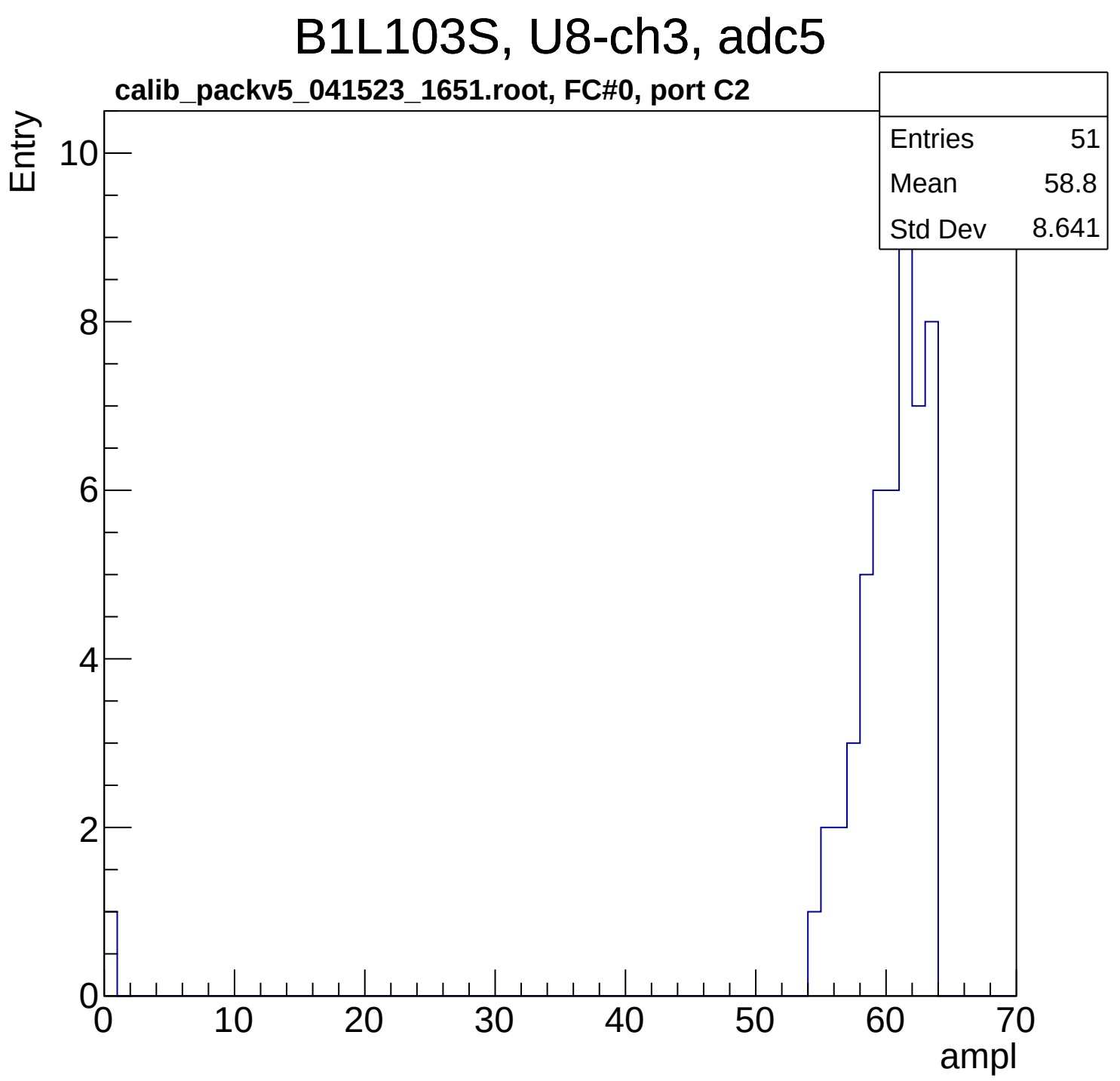
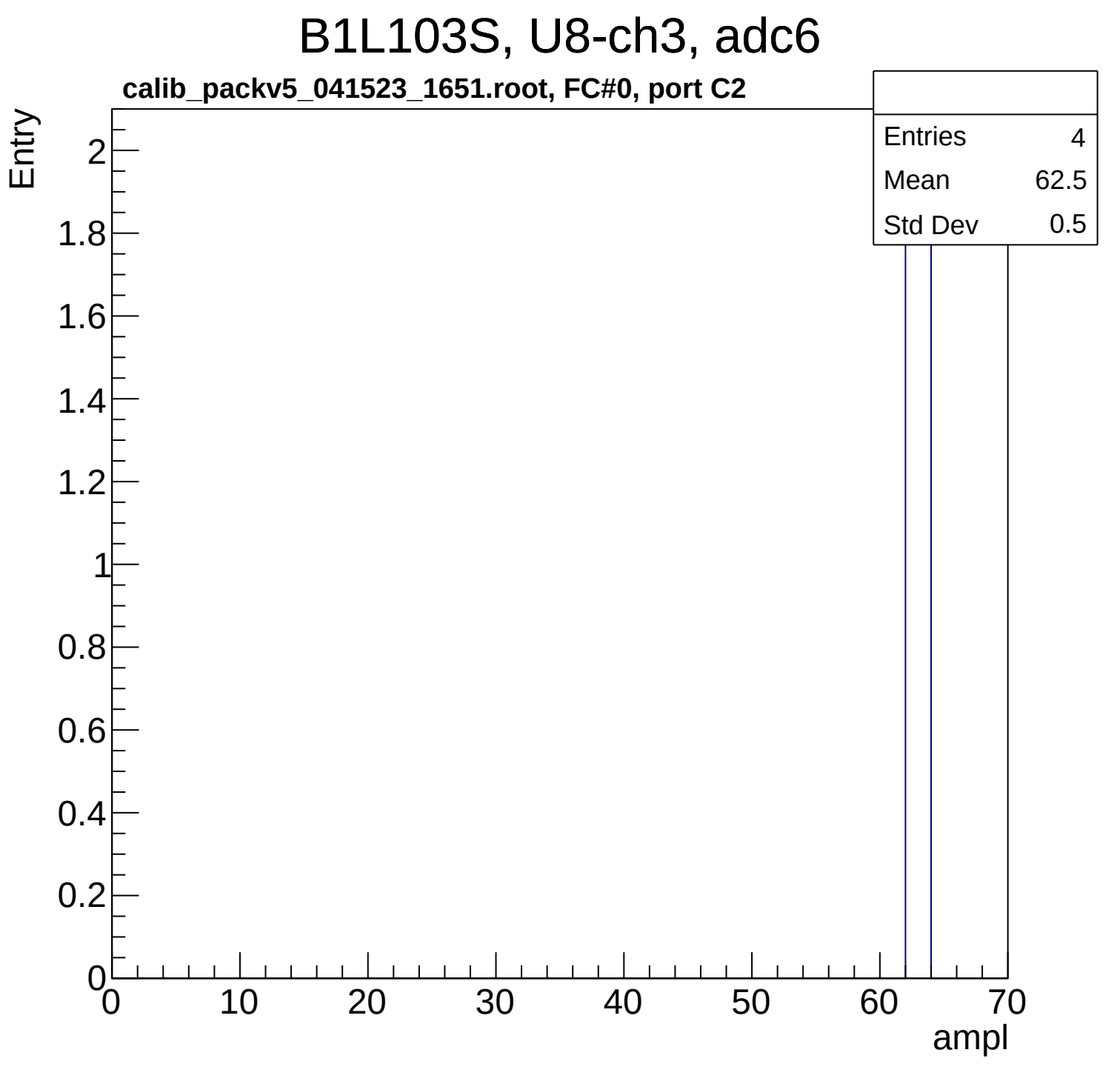
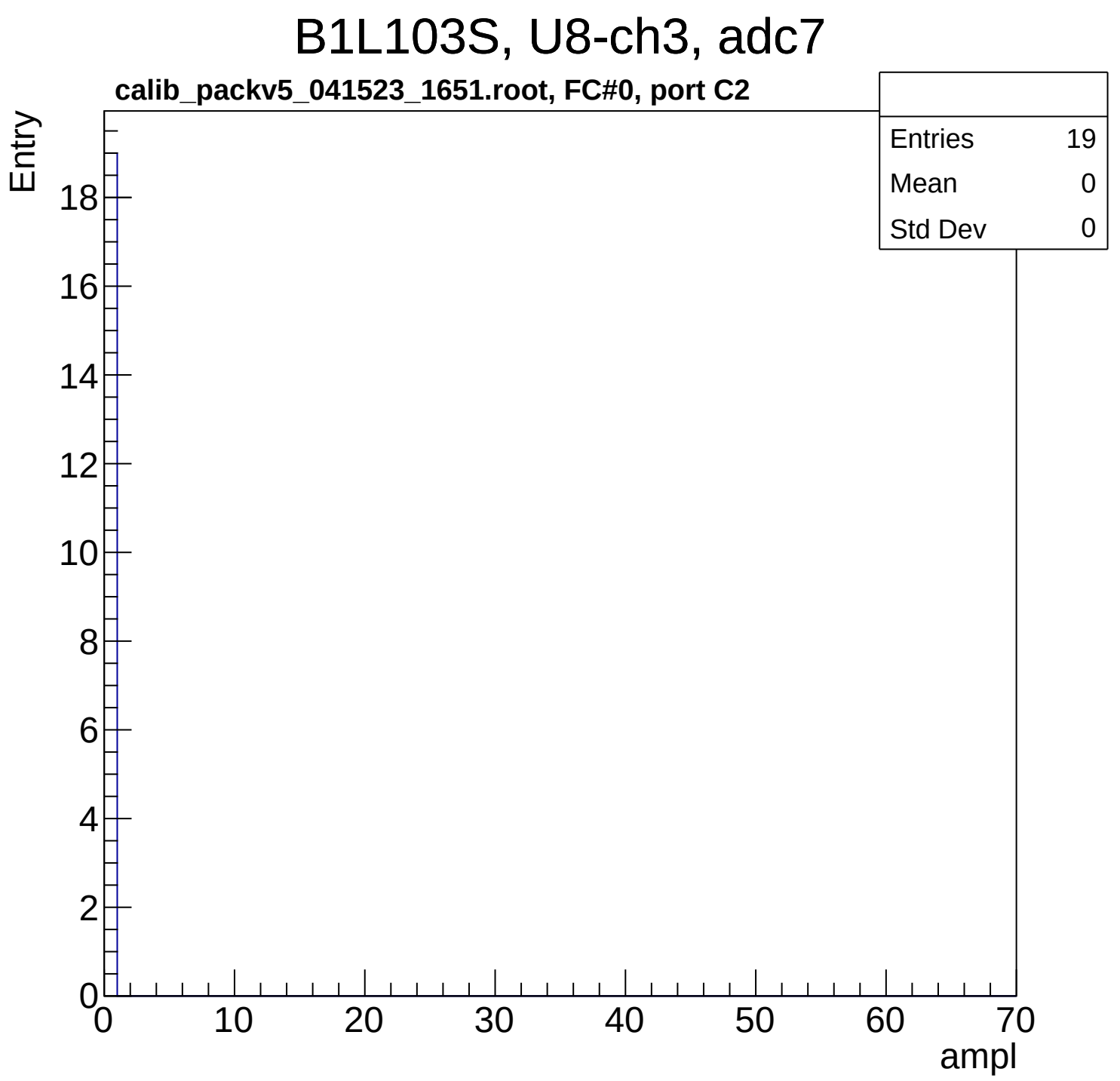
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U8-ch3, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 55.13
Std Dev 3.186
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U8-ch3, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 58.8
Std Dev 8.641
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch3, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 62.5
Std Dev 0.5
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U8-ch3, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
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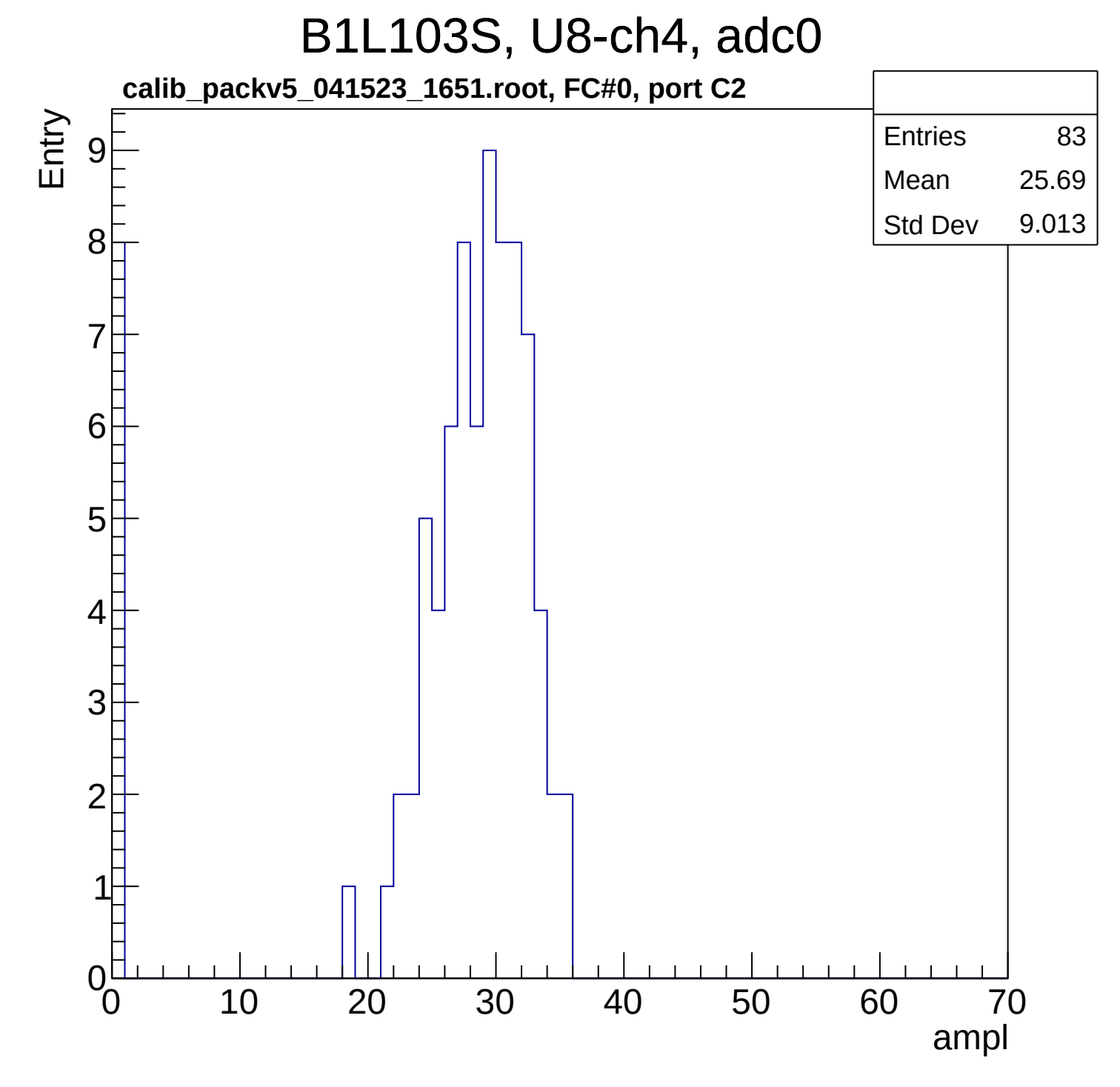
40
50
60
70
ampl


B1L103S, U8-ch4, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 25.69
Std Dev 9.013
Entry
ampl
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2
3
4
5
6
7
8
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0
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60
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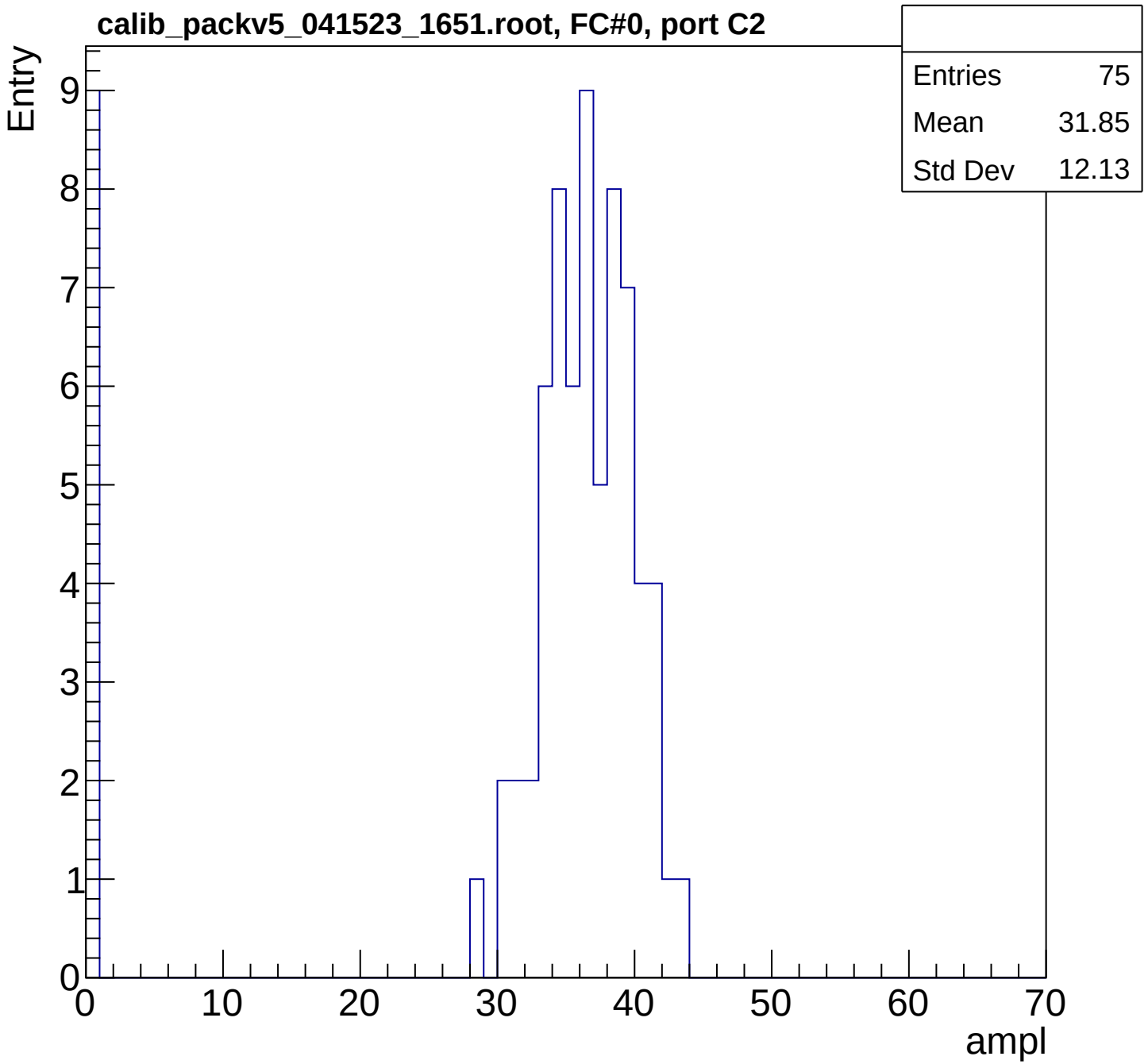
B1L103S, U8-ch4, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 31.85
Std Dev 12.13
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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20
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40
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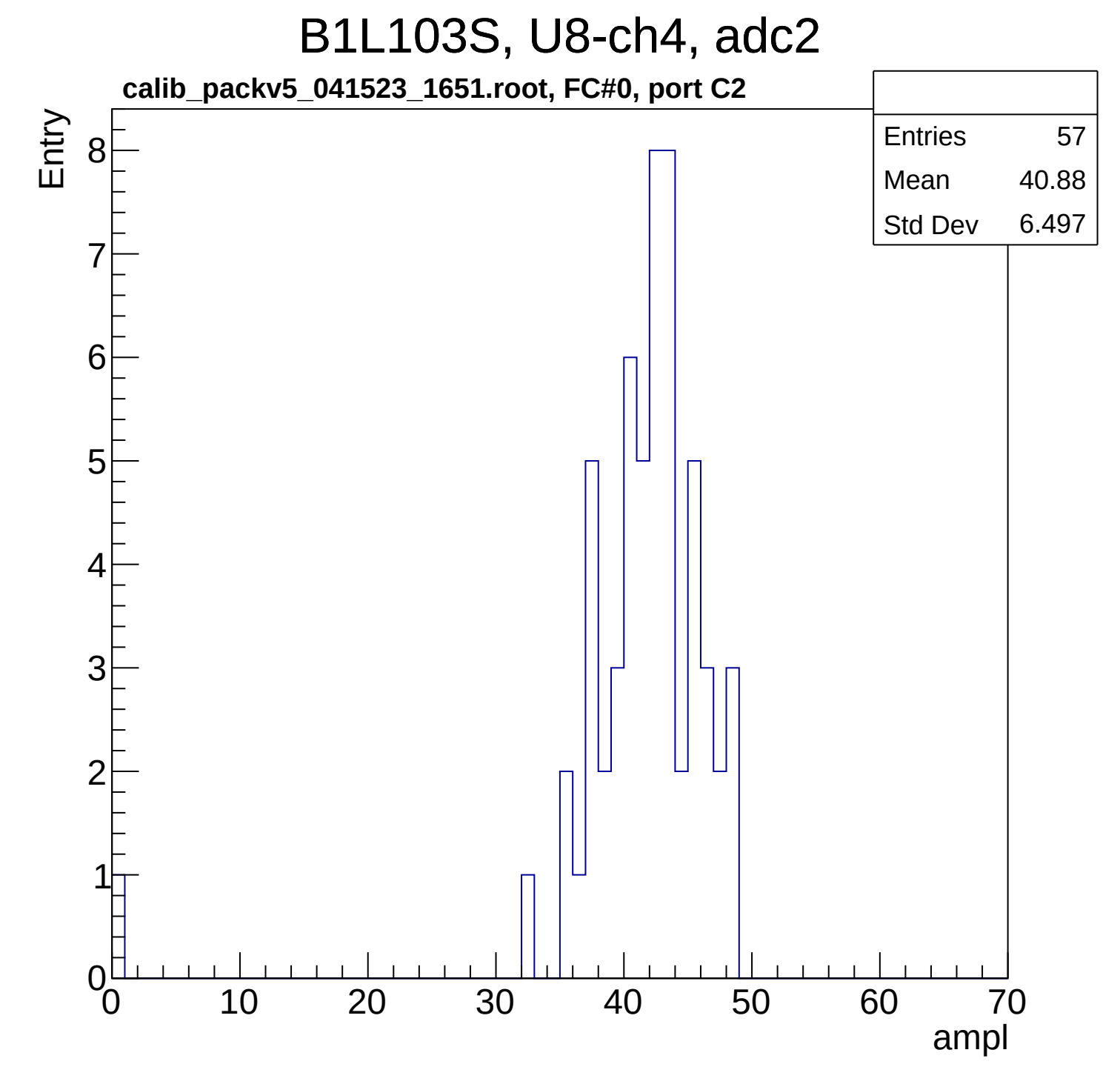
60
70


B1L103S, U8-ch4, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 40.88
Std Dev 6.497
Entry
ampl
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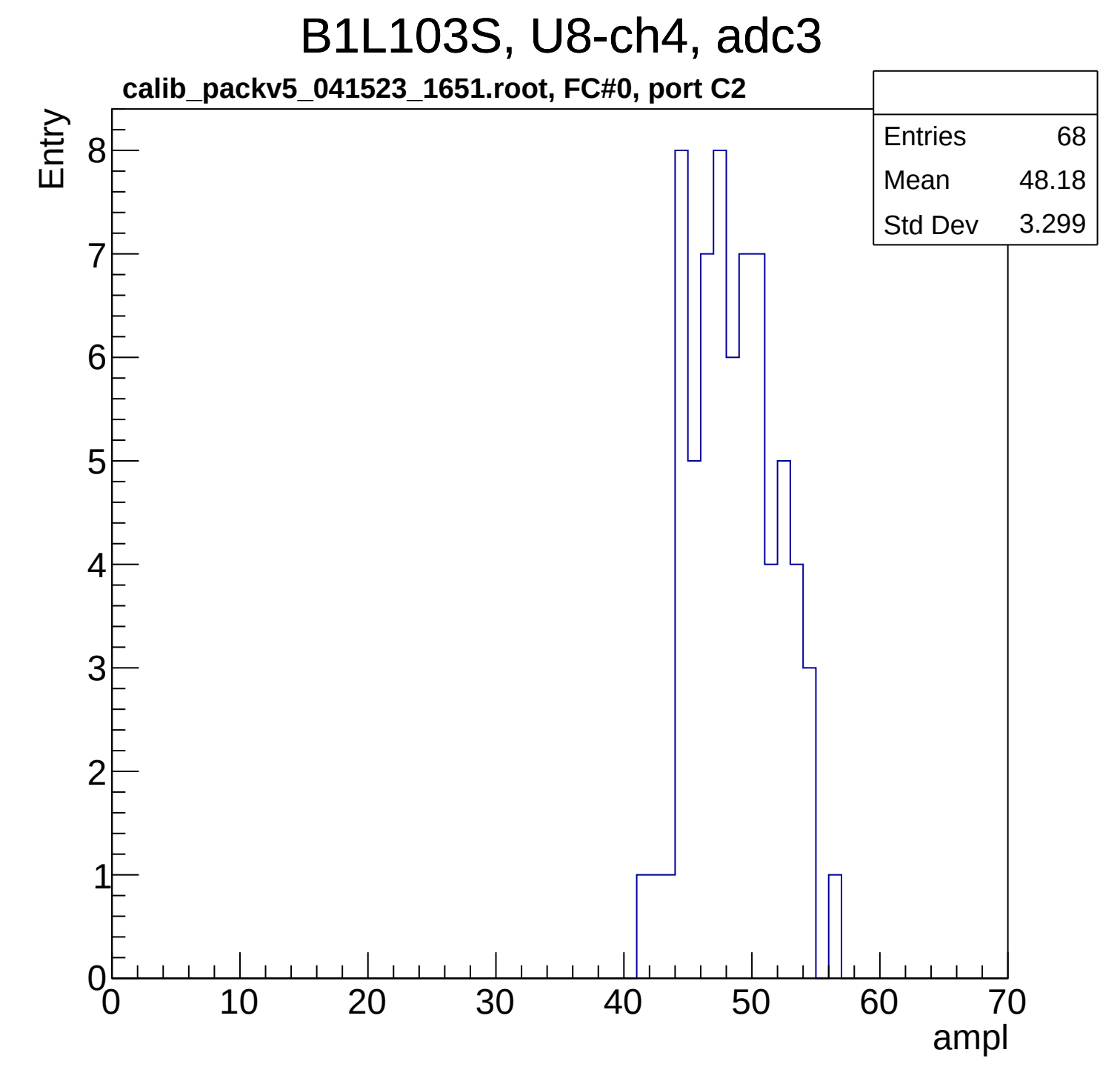
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch4, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 48.18
Std Dev 3.299
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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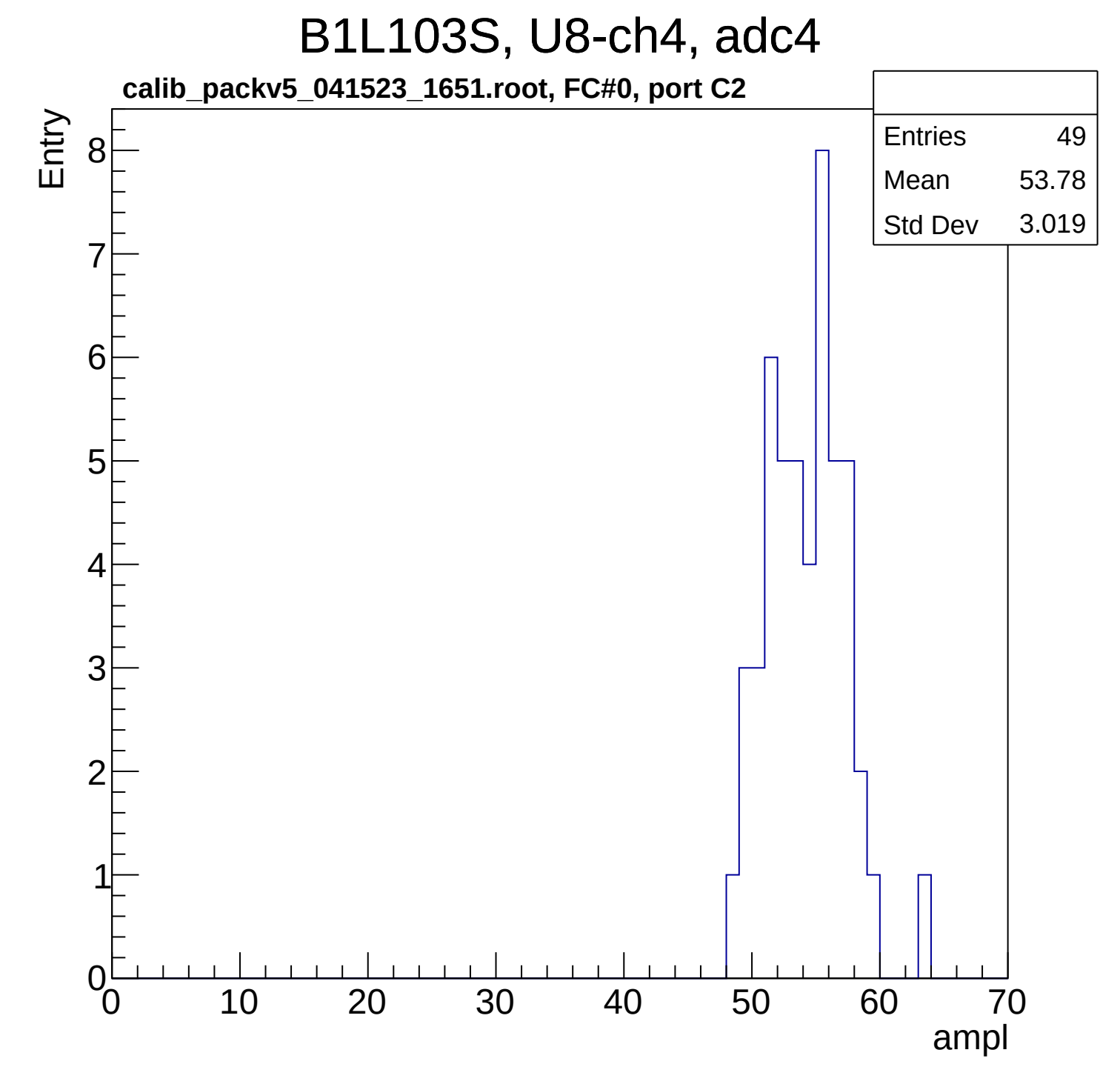
40
50
60
70


B1L103S, U8-ch4, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 53.78
Std Dev 3.019
Entry
ampl
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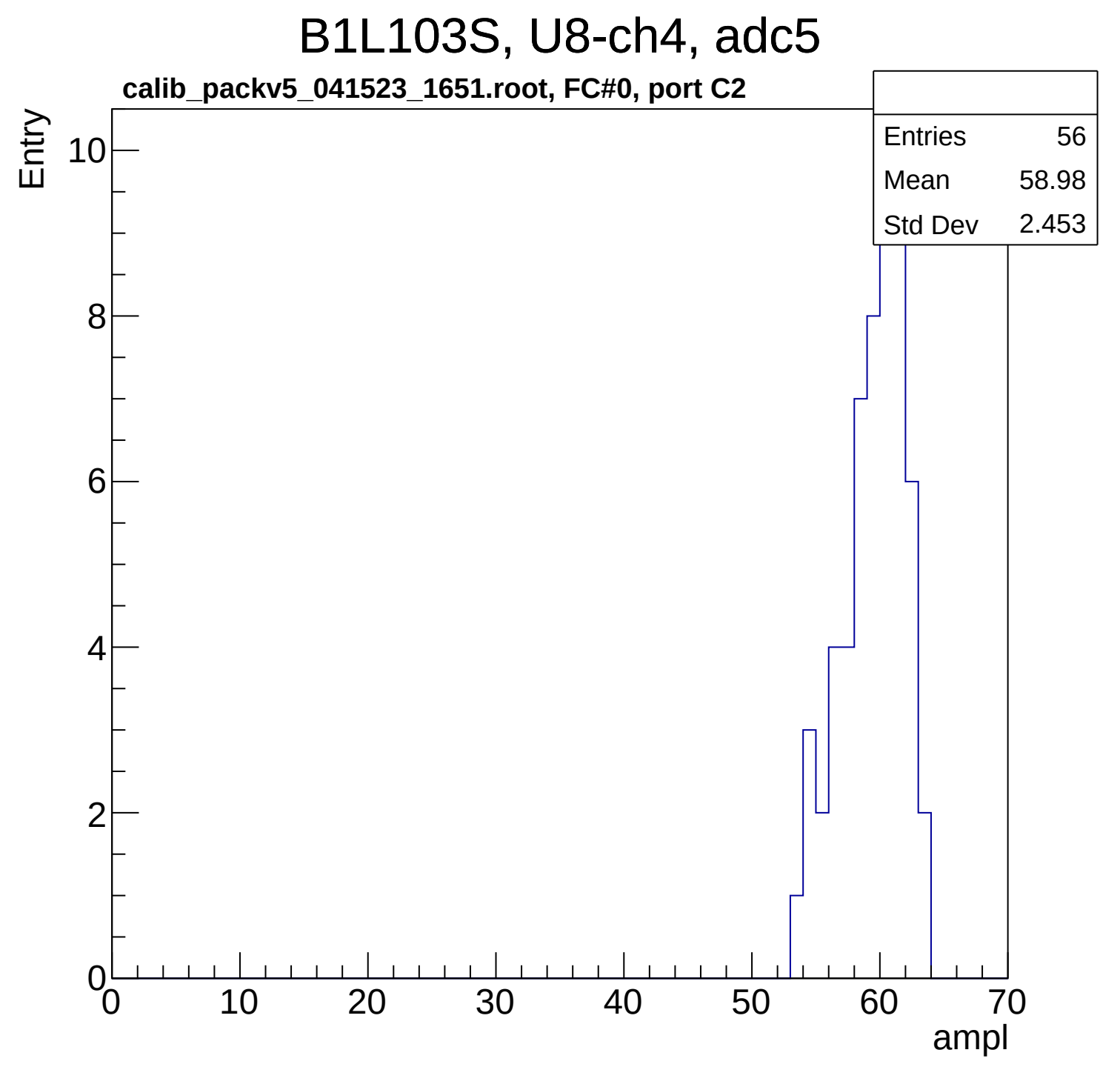
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch4, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 58.98
Std Dev 2.453
Entry
ampl
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2
4
6
8
10
0
10
20
30
40
50
60
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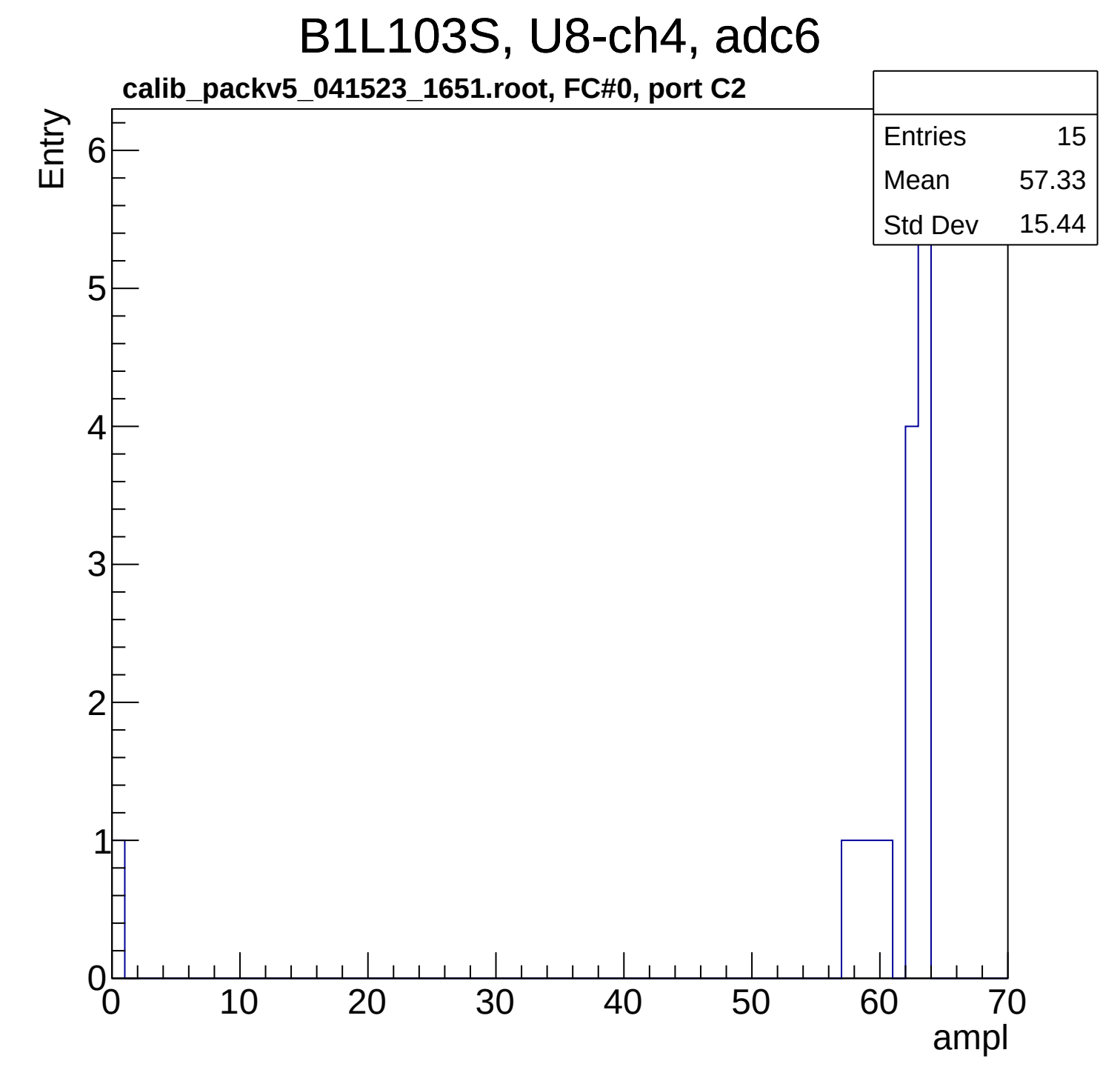
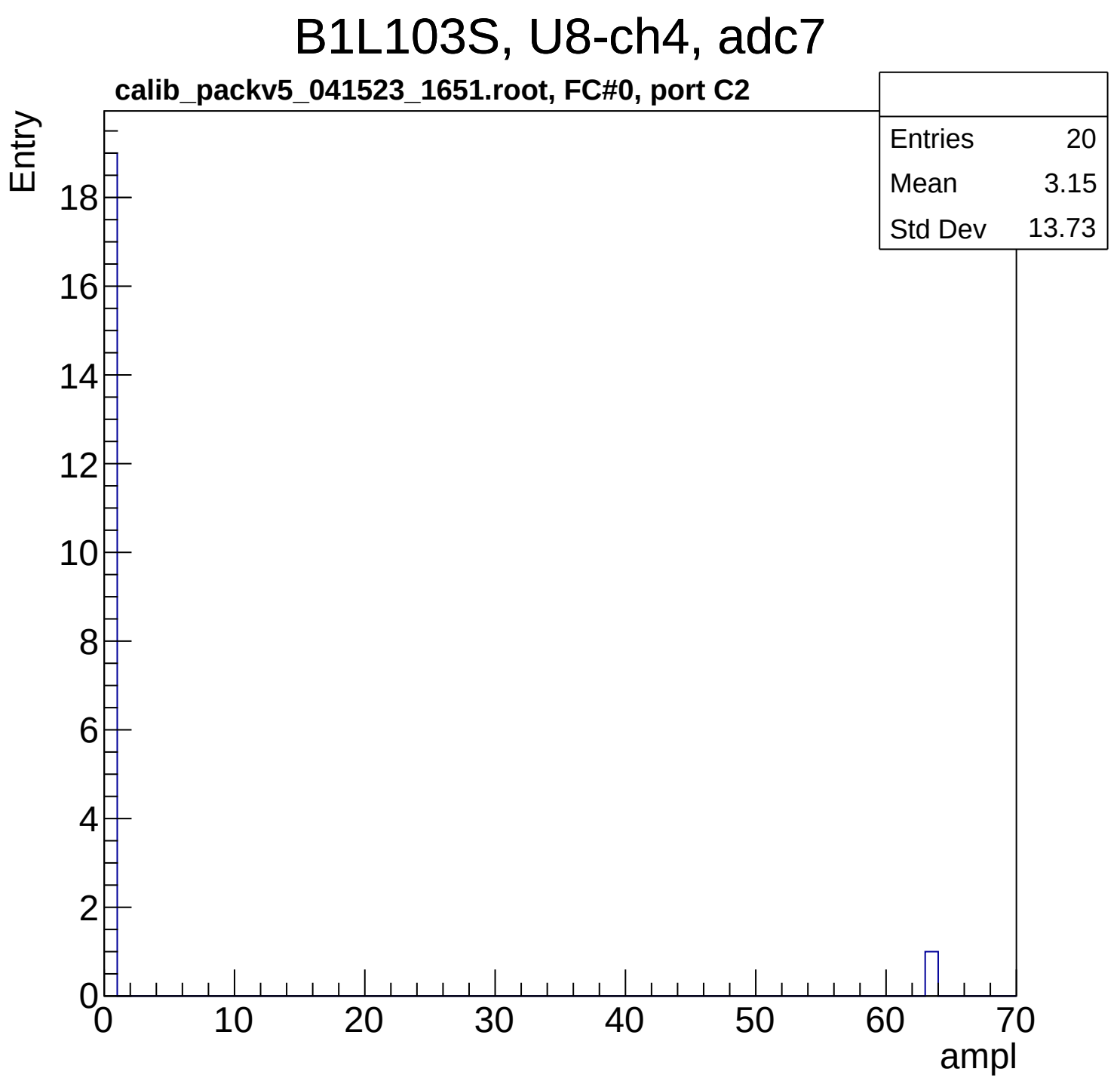
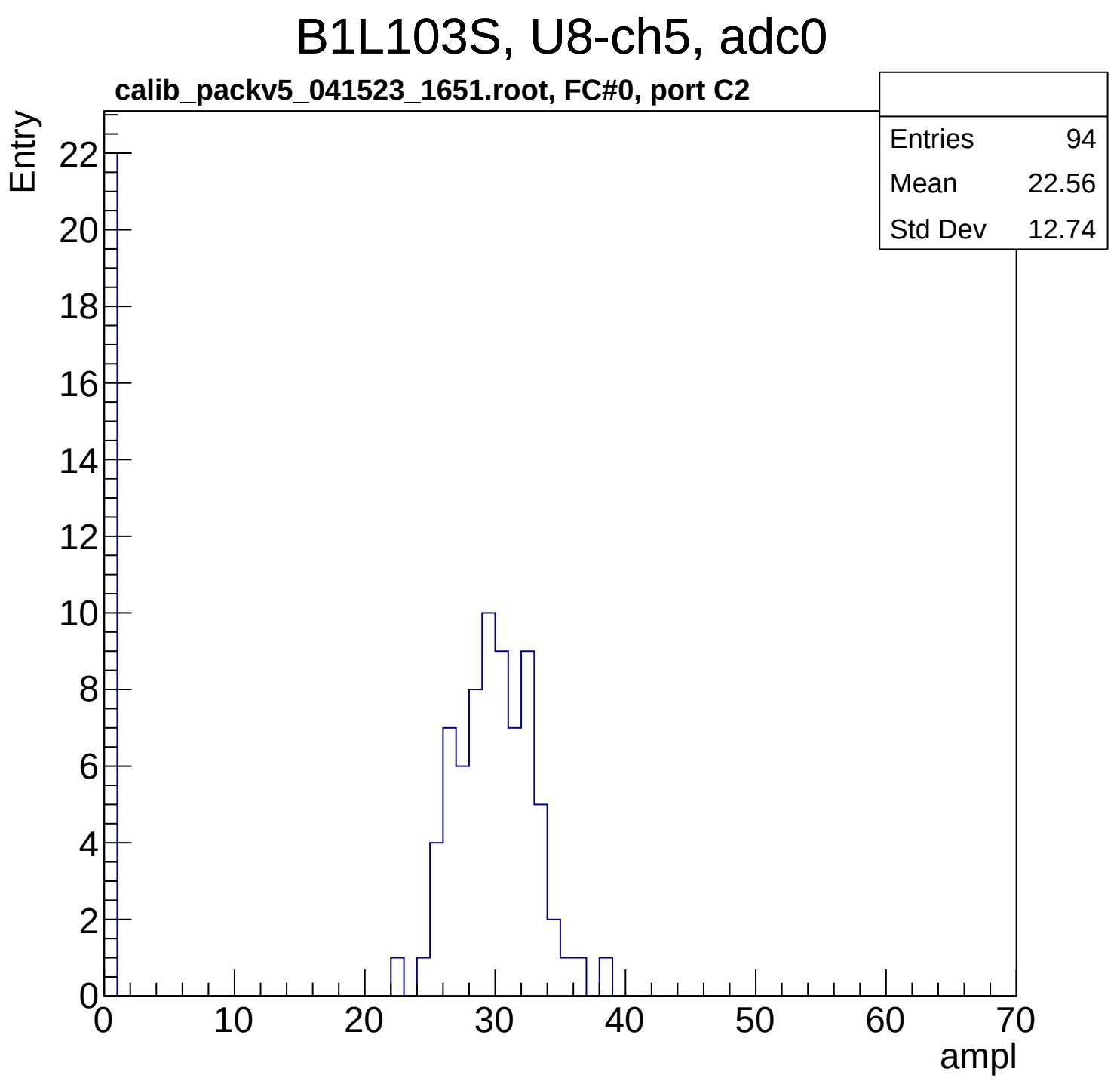
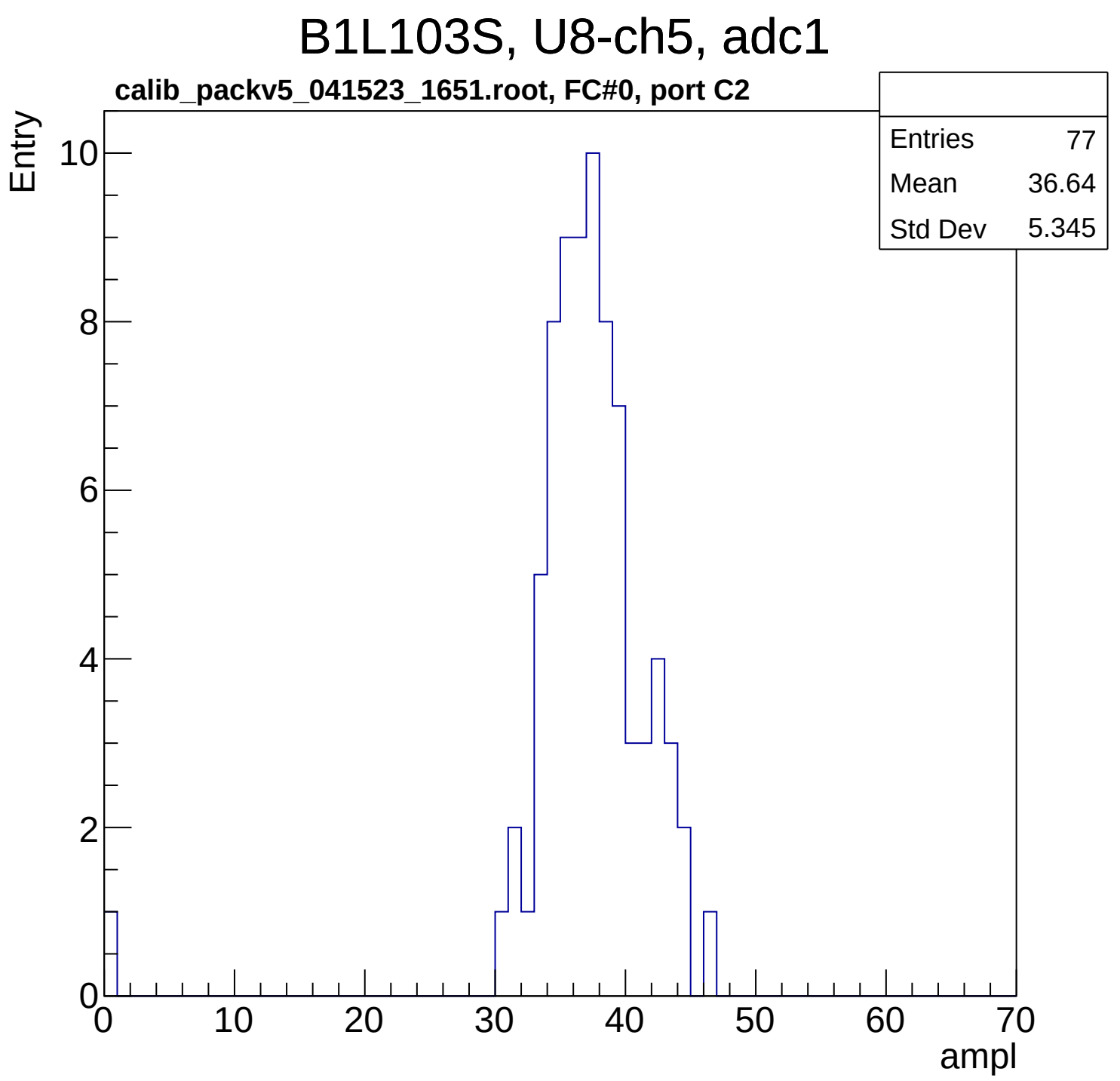
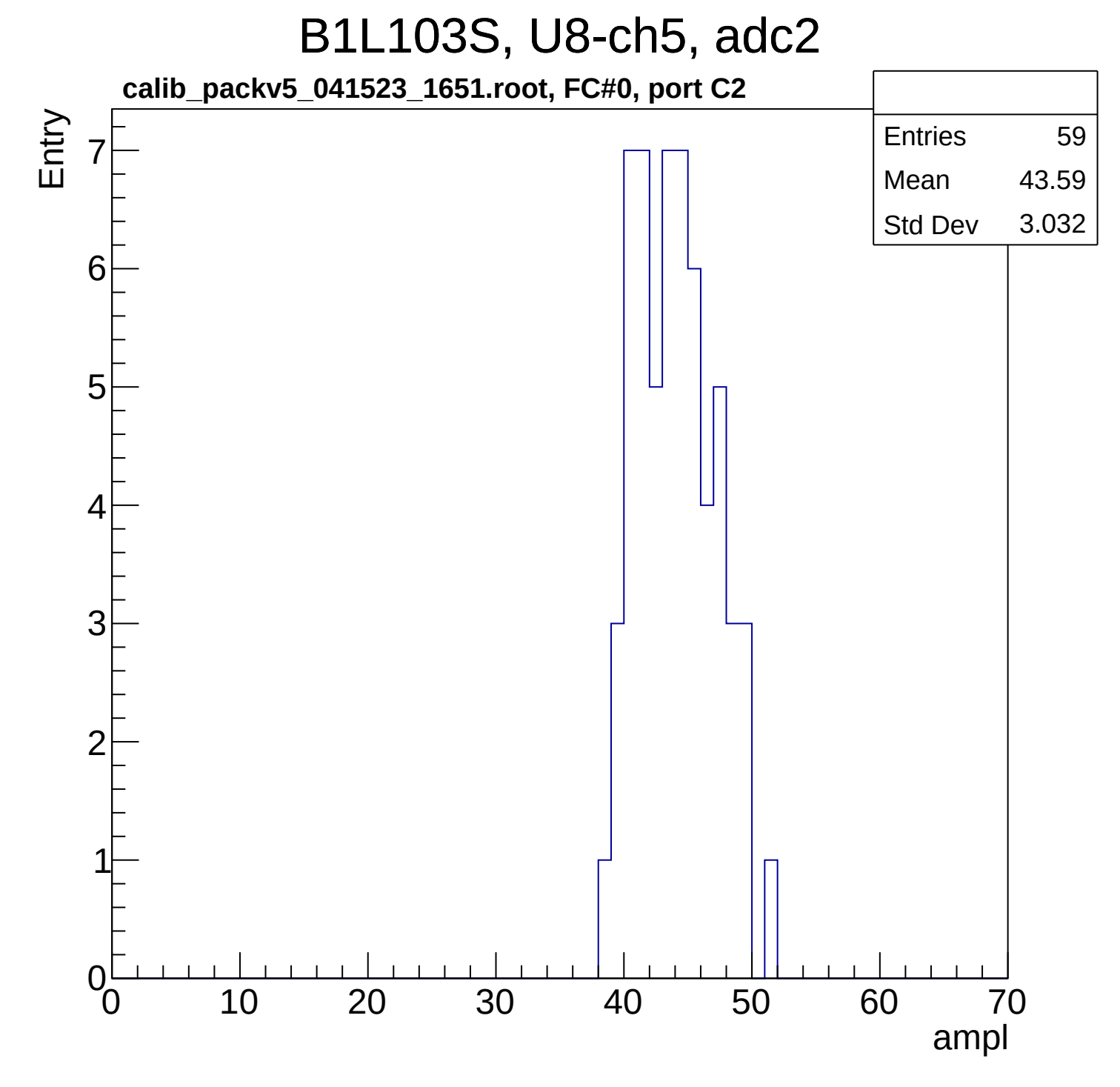
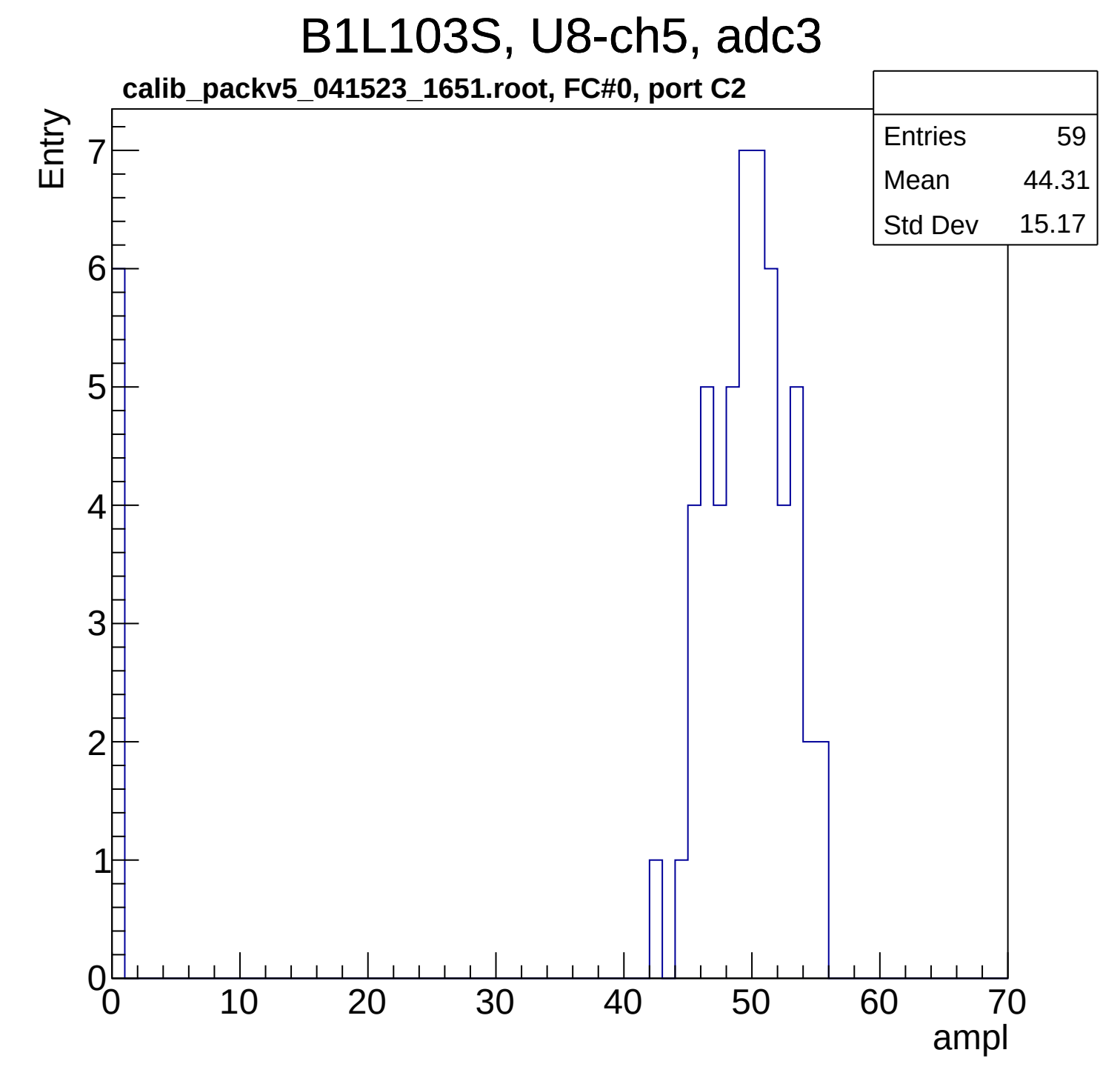

B1L103S, U8-ch4, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 57.33
Std Dev 15.44
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

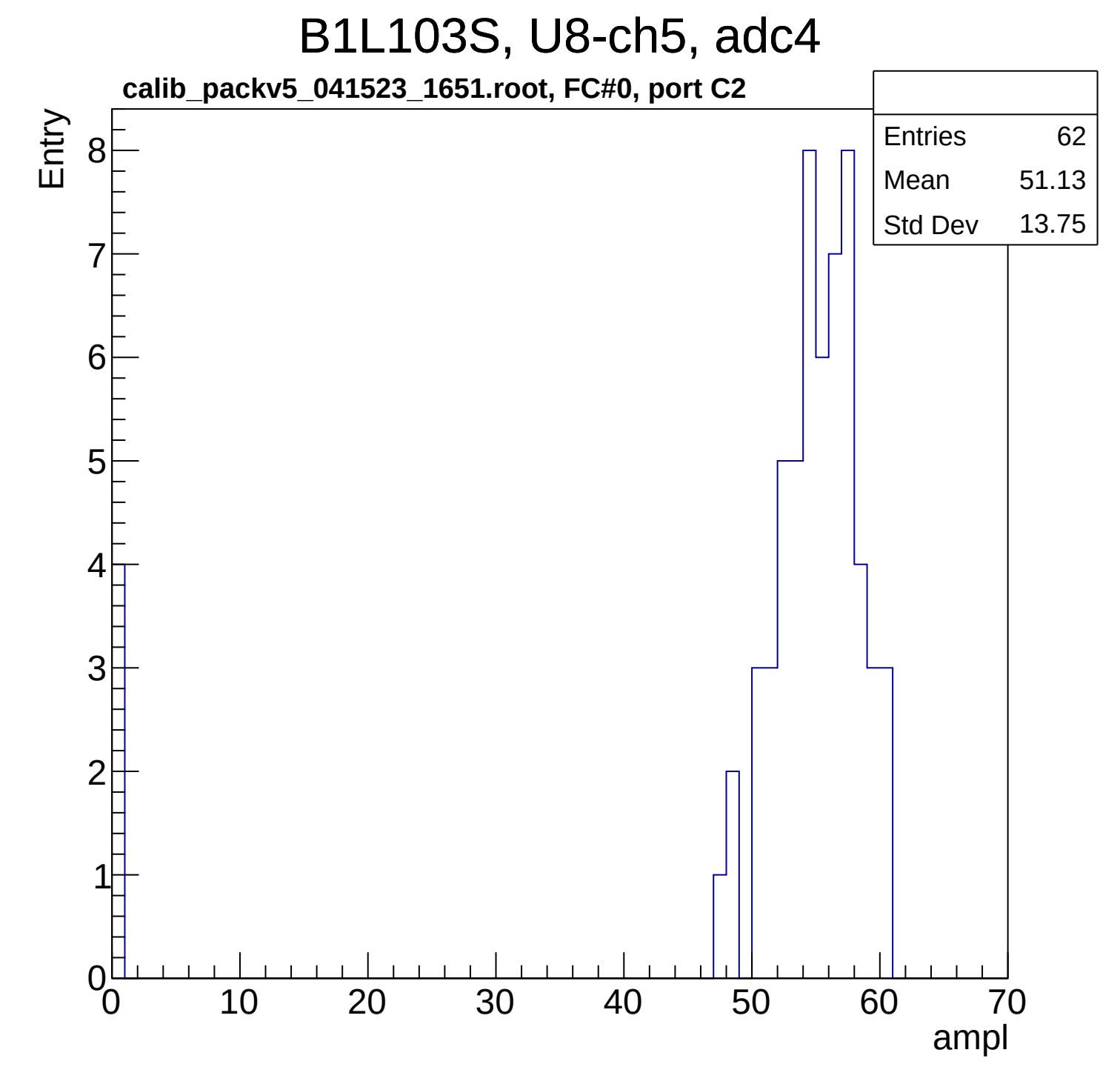

B1L103S, U8-ch4, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

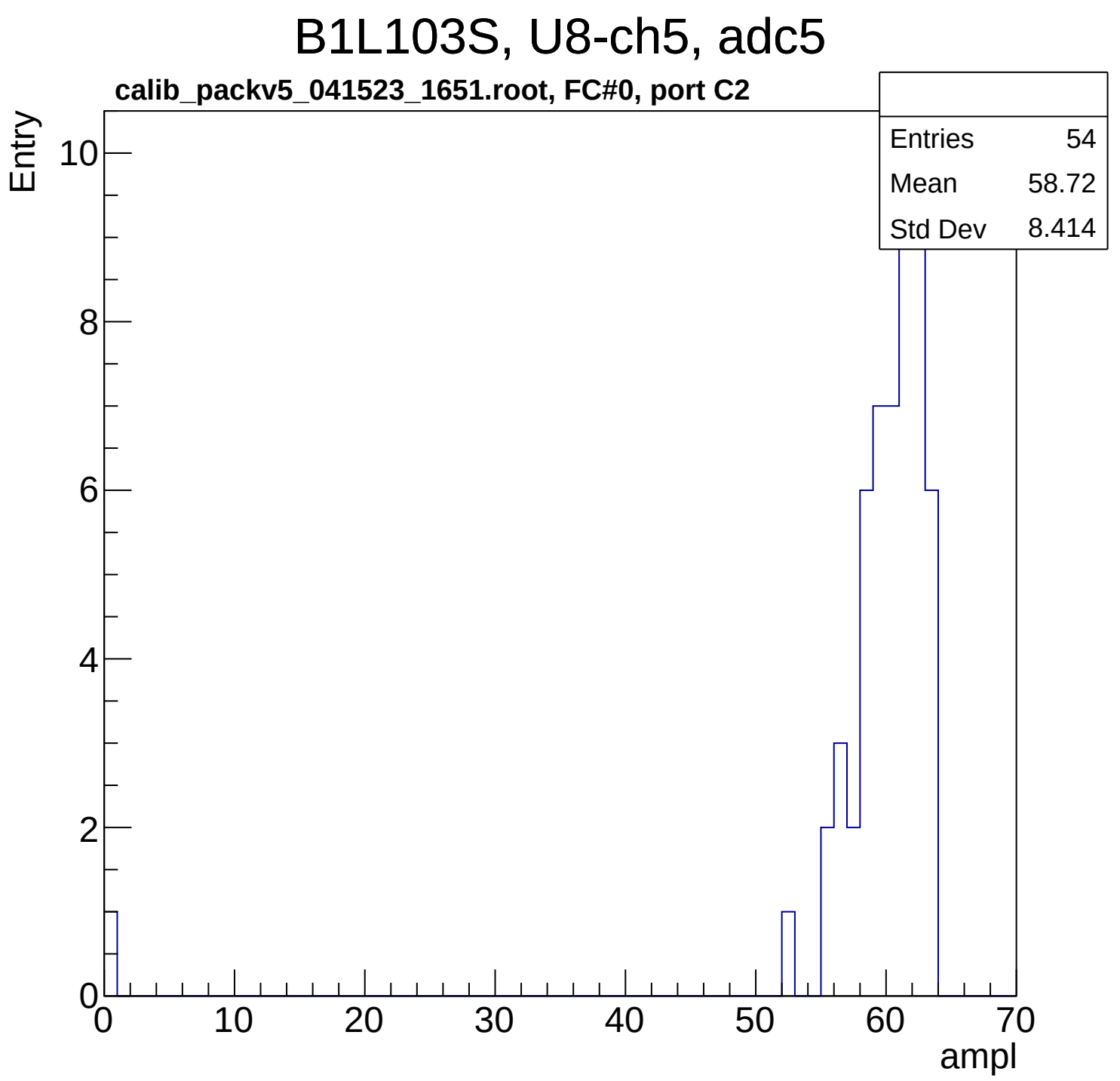

B1L103S, U8-ch5, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 22.56
Std Dev 12.74
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70

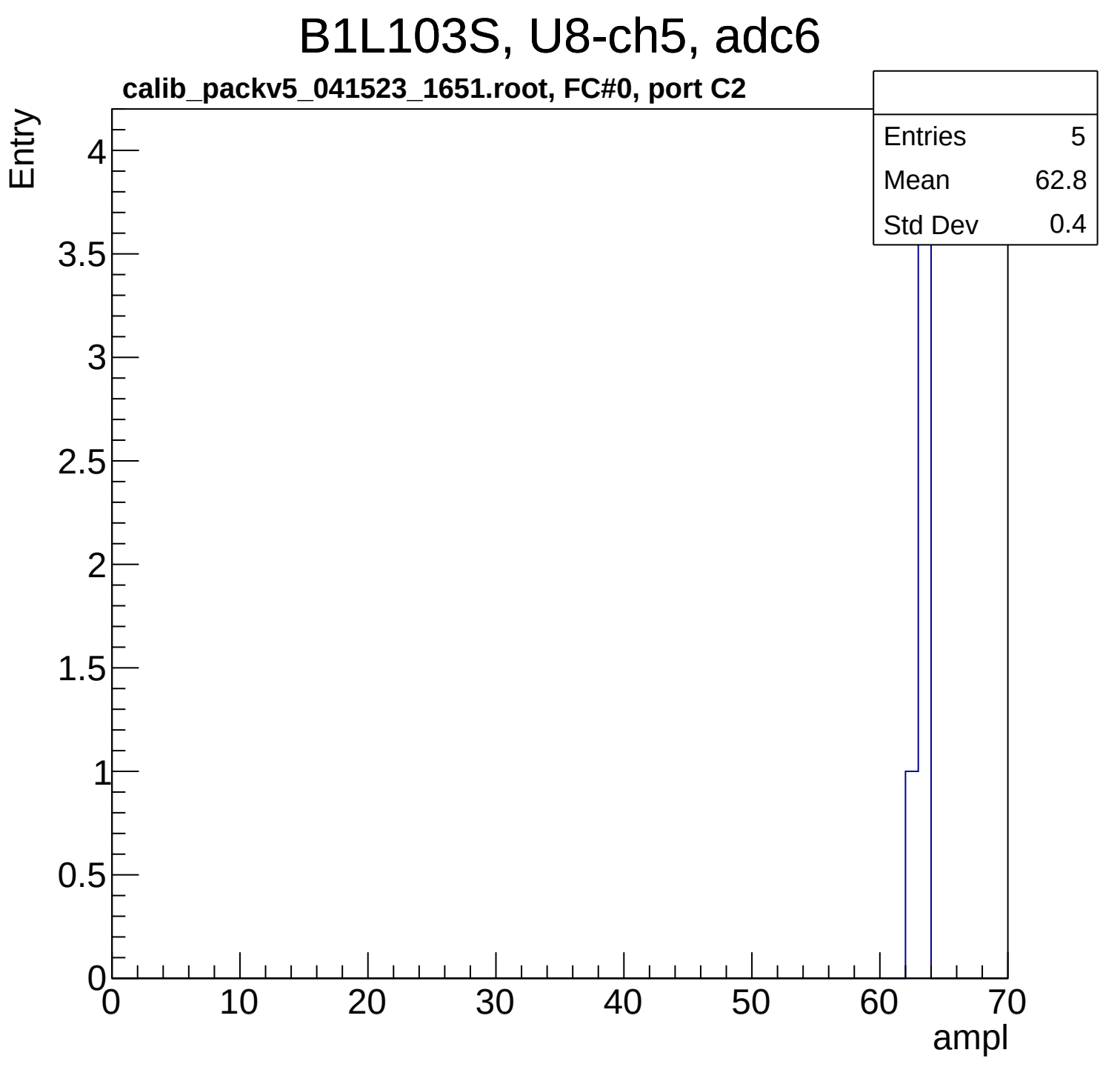

B1L103S, U8-ch5, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 36.64
Std Dev 5.345
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U8-ch5, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 43.59
Std Dev 3.032
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U8-ch5, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 44.31
Std Dev 15.17
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U8-ch5, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 51.13
Std Dev 13.75
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch5, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 58.72
Std Dev 8.414
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch5, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 62.8
Std Dev 0.4
Entry
ampl
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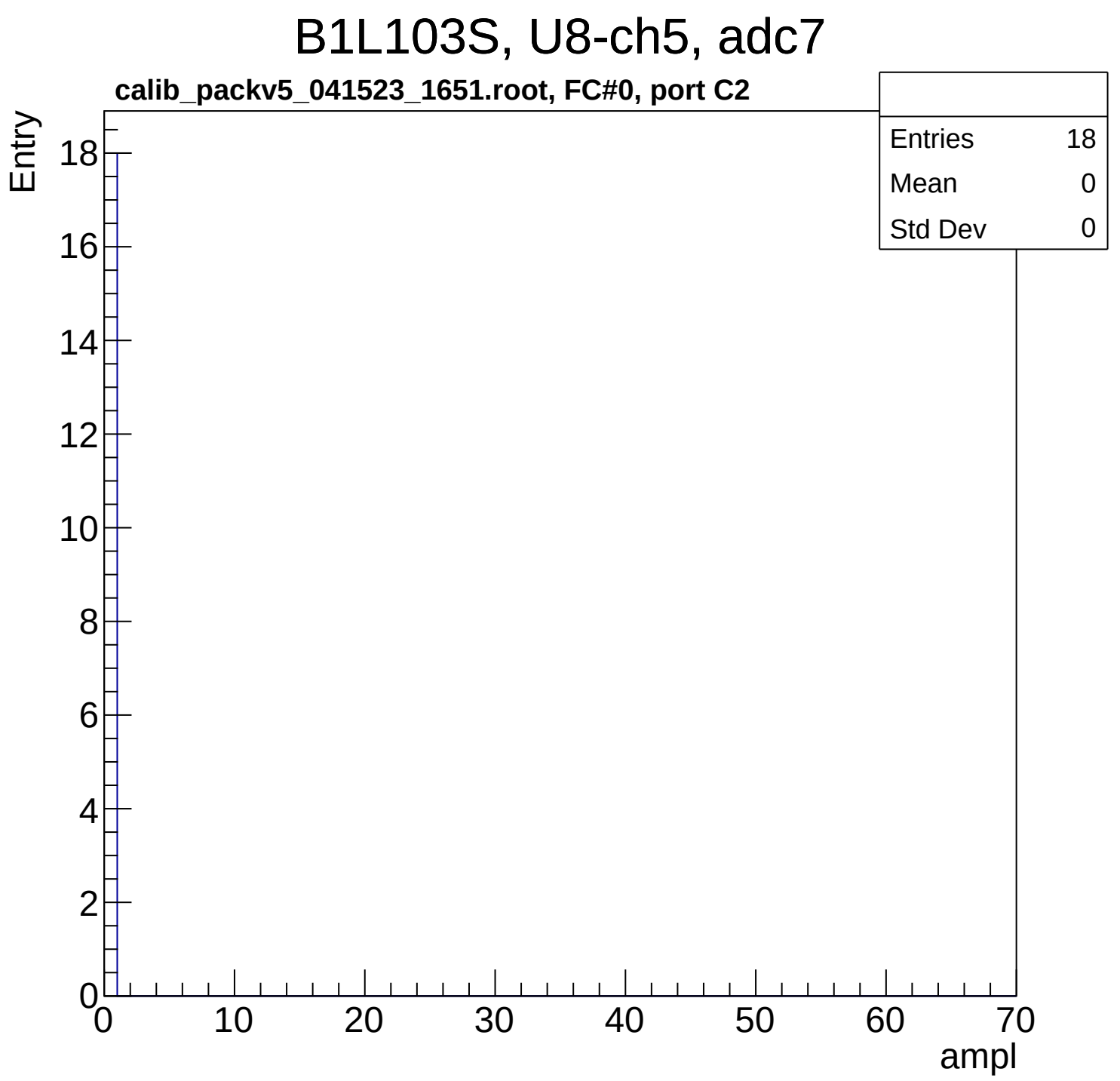
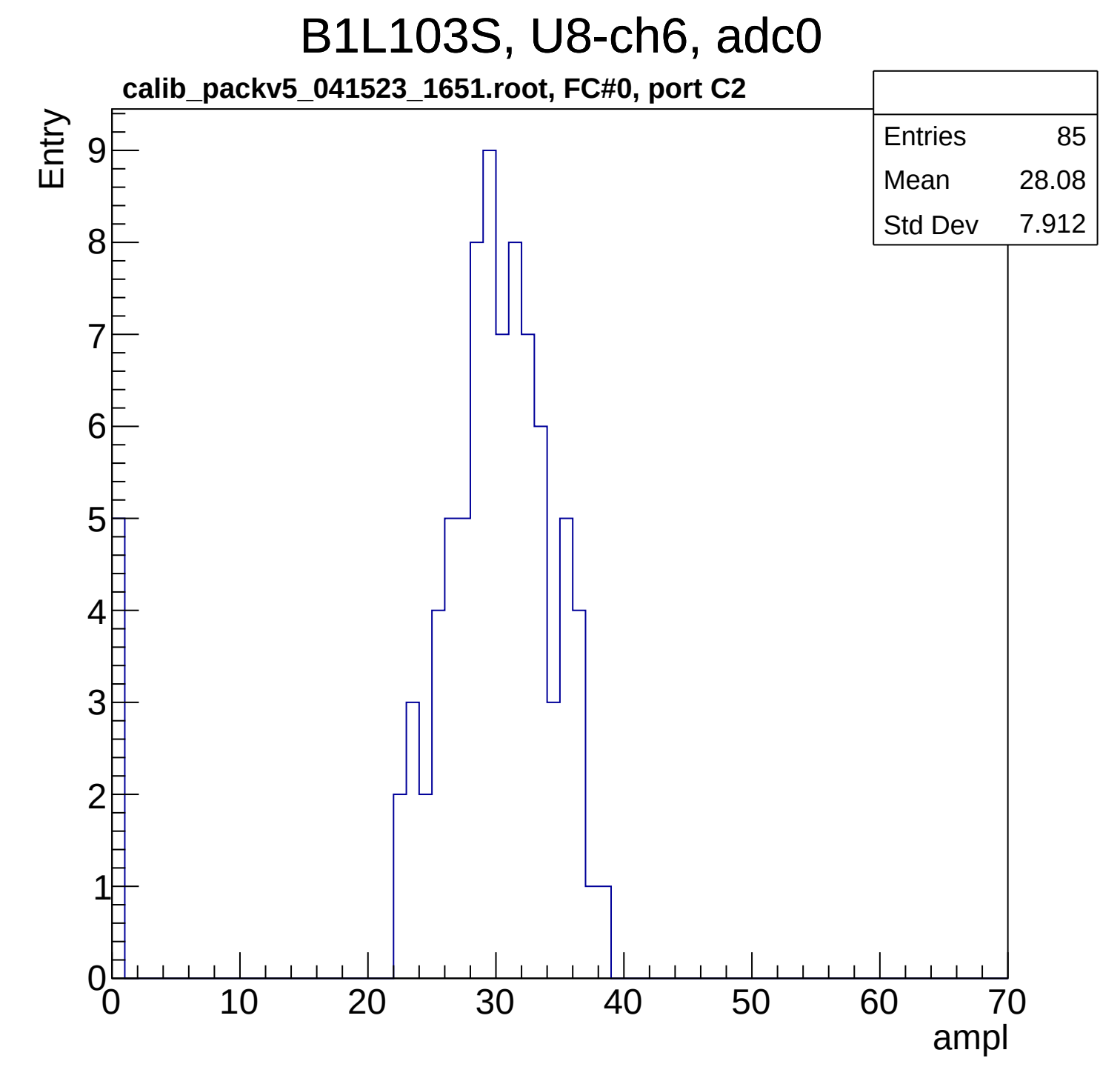
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U8-ch5, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch6, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 28.08
Std Dev 7.912
Entry
ampl
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2
3
4
5
6
7
8
9
0
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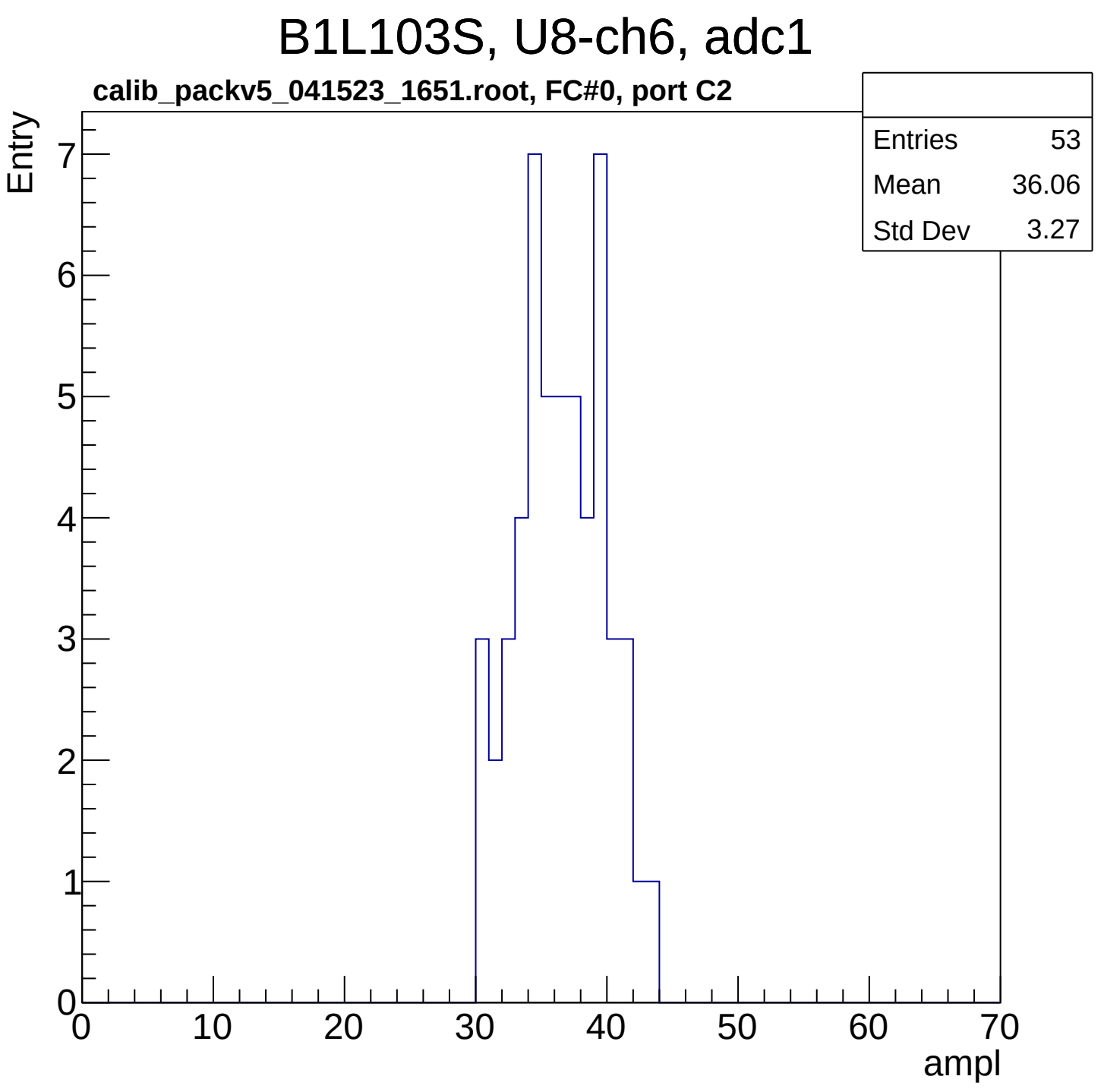
30
40
50
60
70


B1L103S, U8-ch6, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 36.06
Std Dev 3.27
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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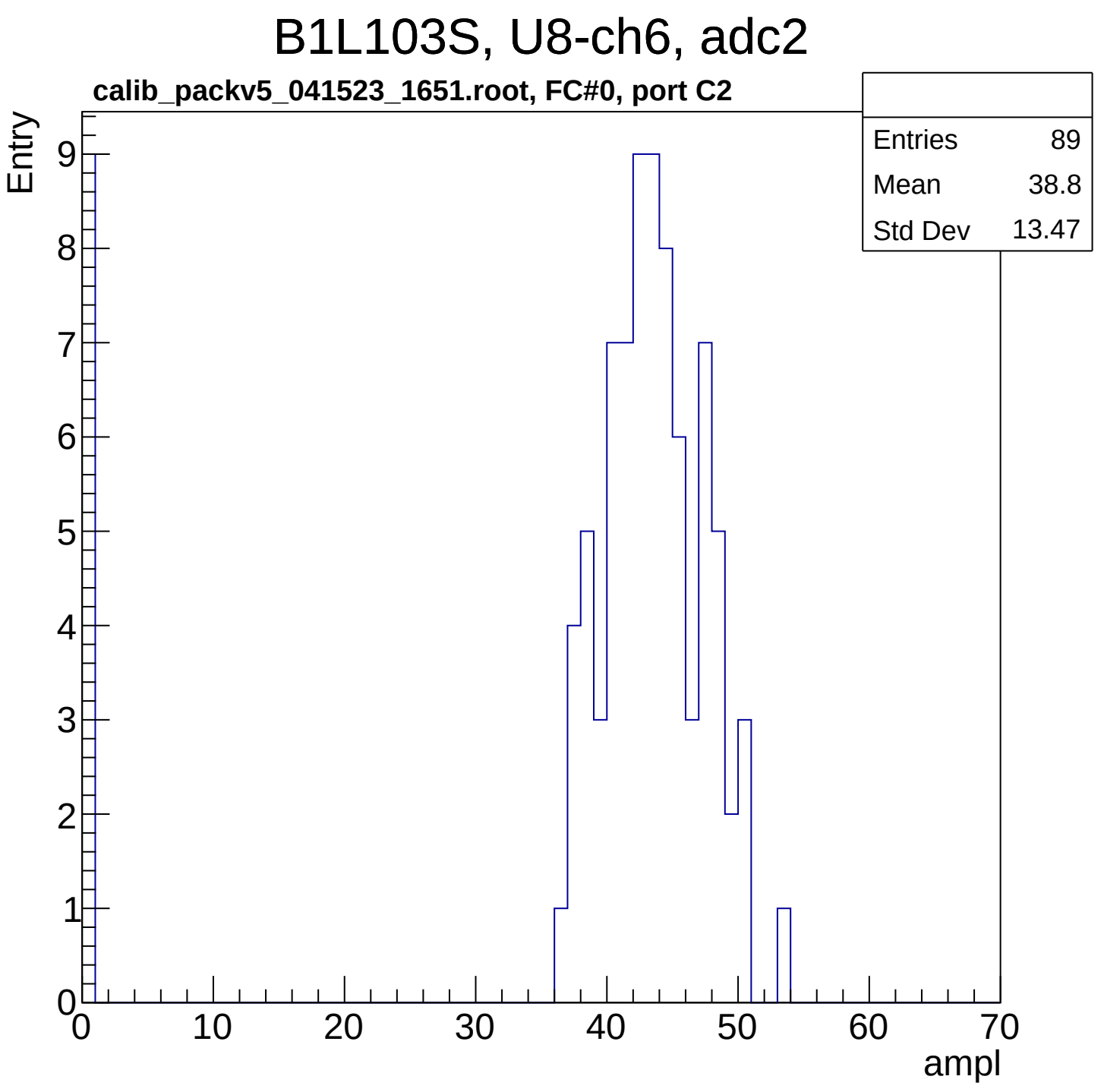
40
50
60
70


B1L103S, U8-ch6, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 38.8
Std Dev 13.47
Entry
ampl
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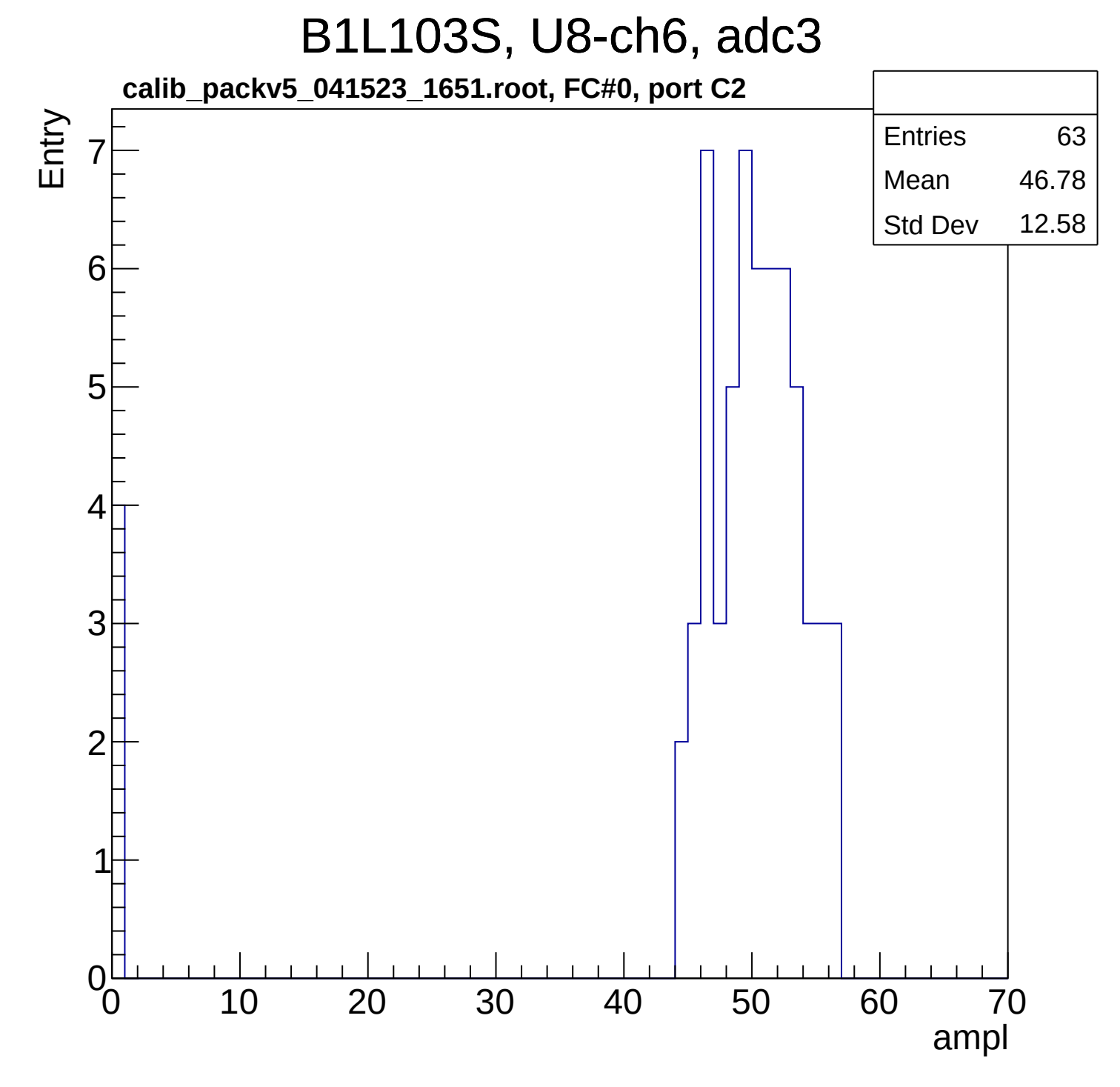
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U8-ch6, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 46.78
Std Dev 12.58
Entry
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1
2
3
4
5
6
7
0
10
20
30
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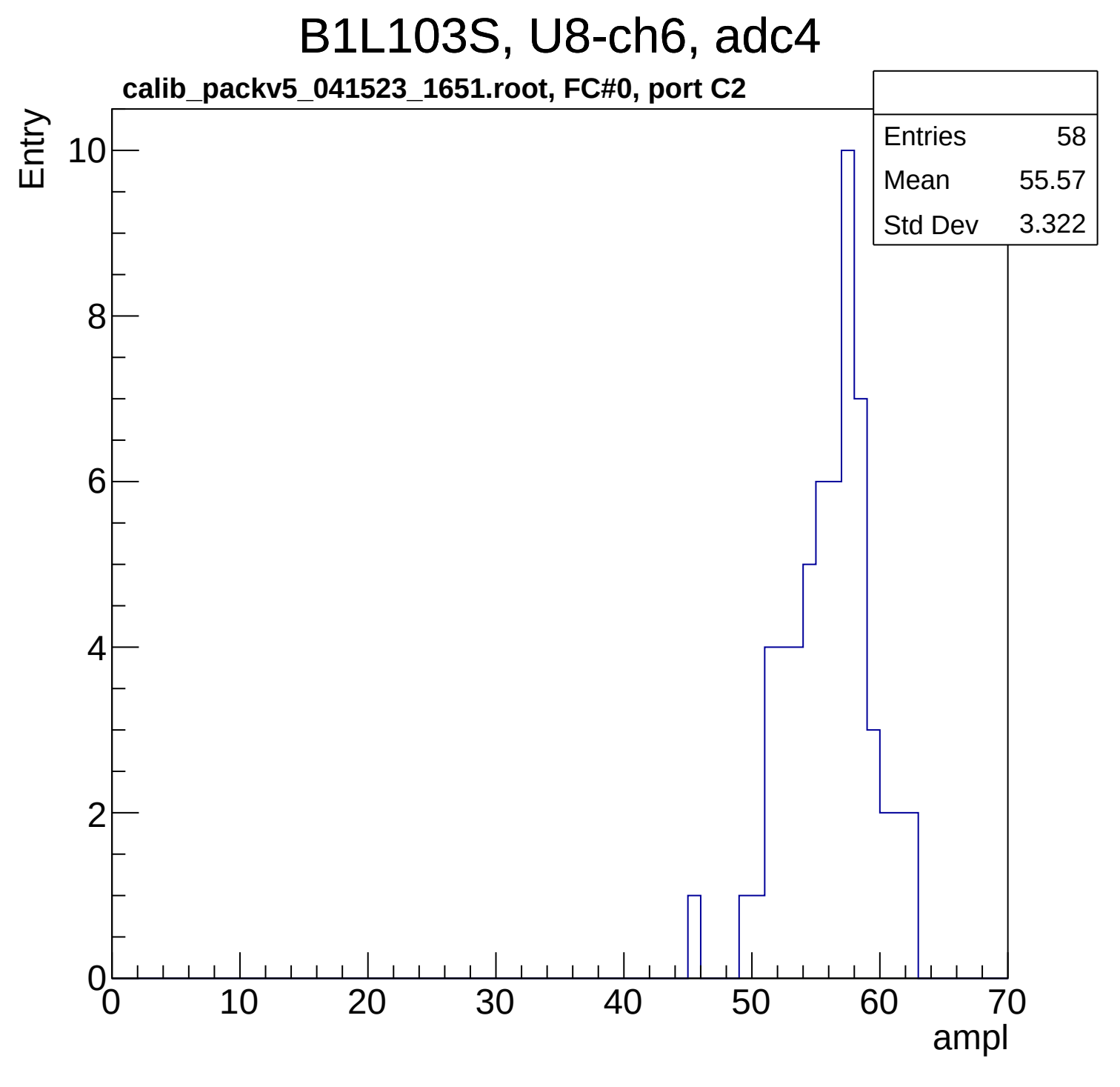
50
60
70
ampl


B1L103S, U8-ch6, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 55.57
Std Dev 3.322
Entry
ampl
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2
4
6
8
10
0
10
20
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40
50
60
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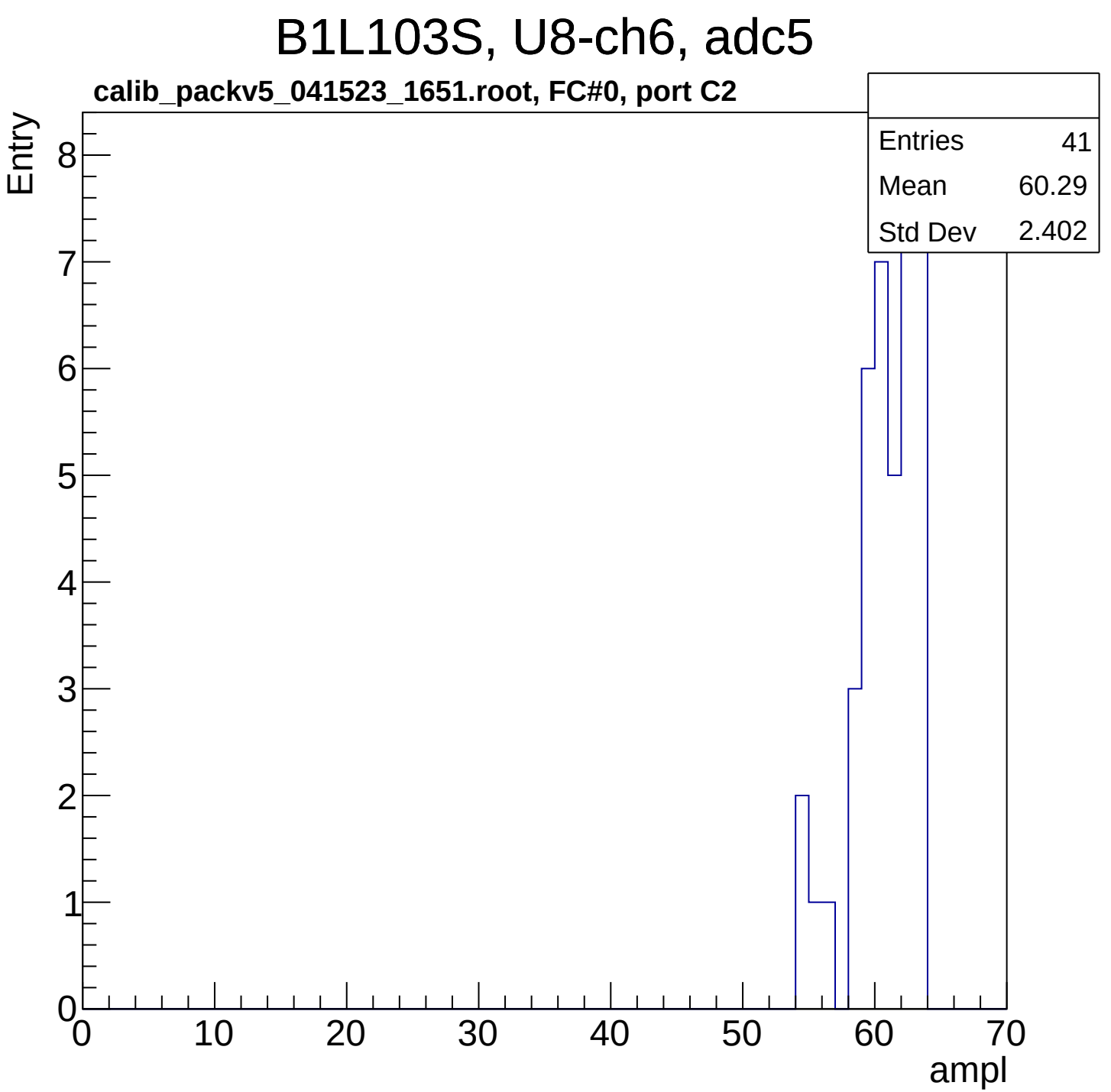
B1L103S, U8-ch6, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 60.29
Std Dev 2.402
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
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40
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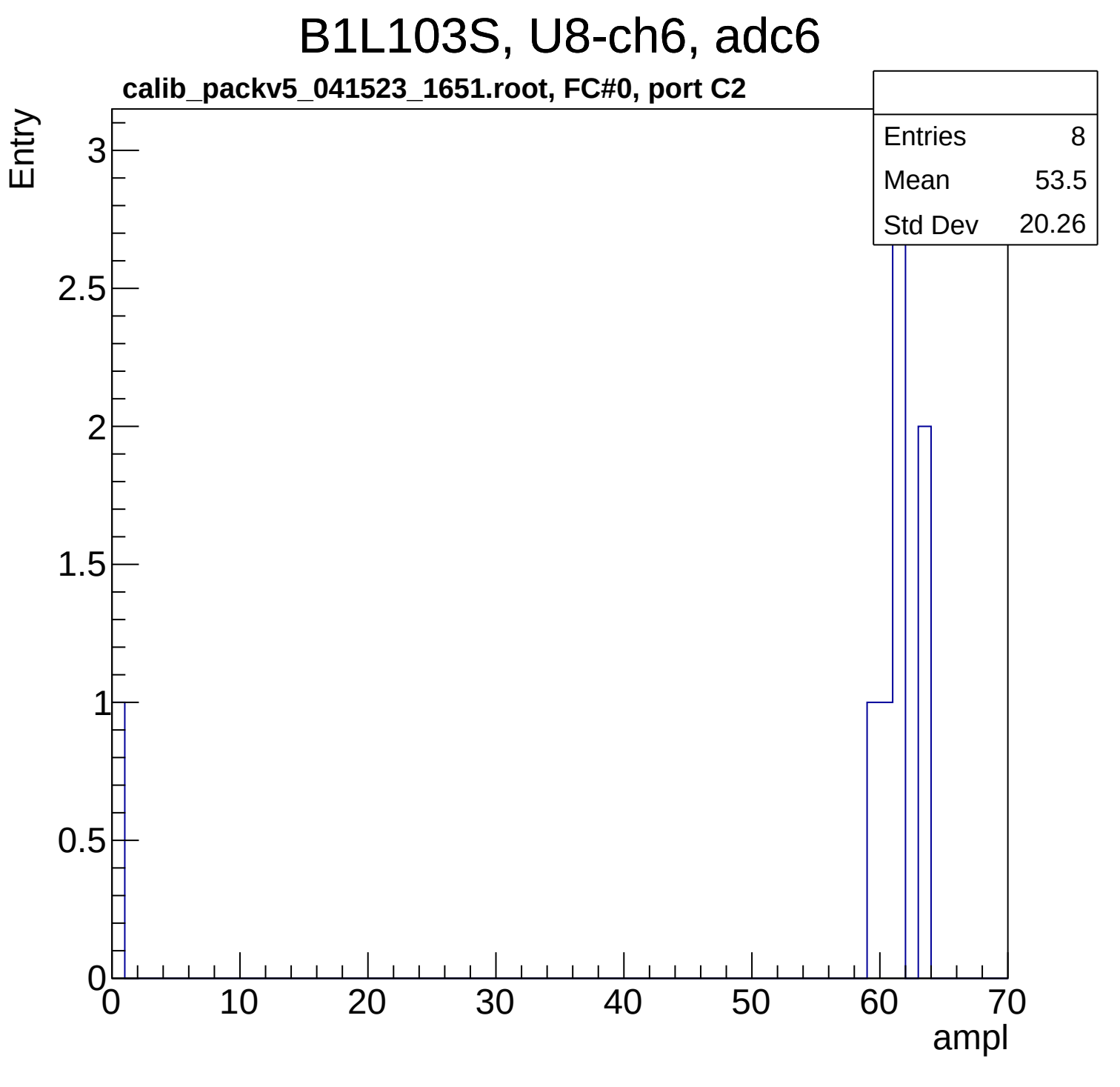
60
70


B1L103S, U8-ch6, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 53.5
Std Dev 20.26
Entry
ampl
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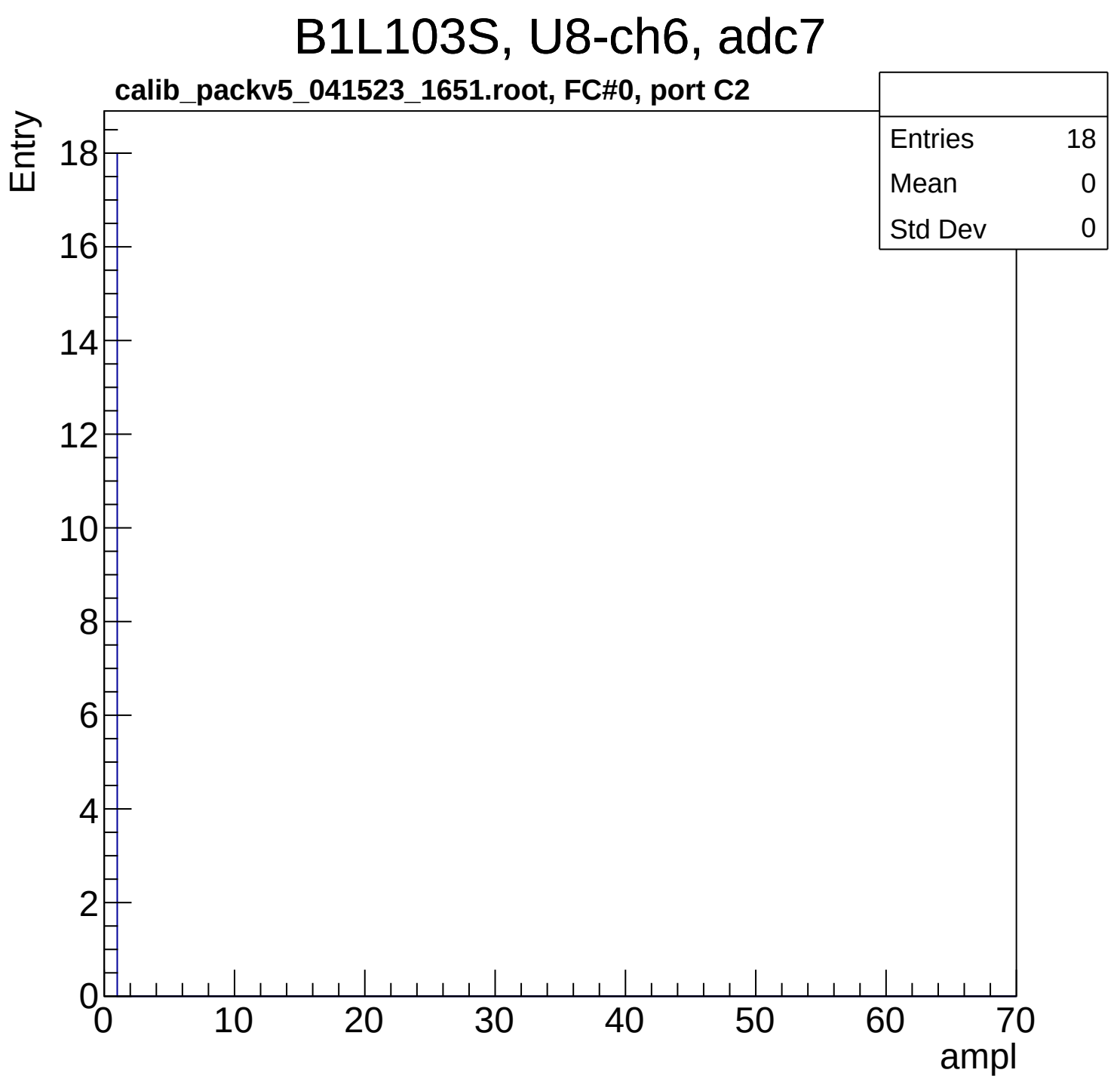
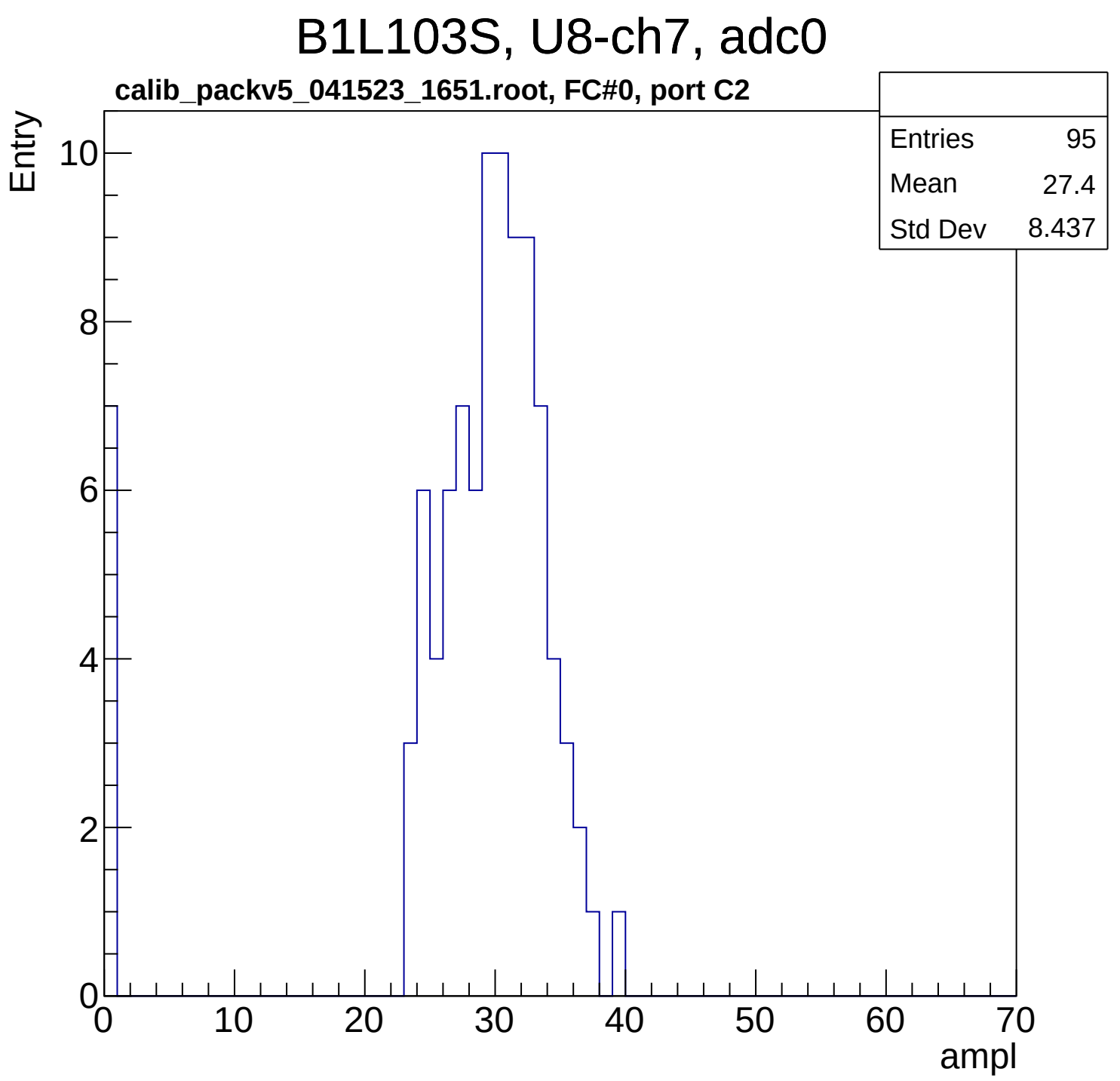
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U8-ch6, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch7, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 27.4
Std Dev 8.437
Entry
ampl
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2
4
6
8
10
0
10
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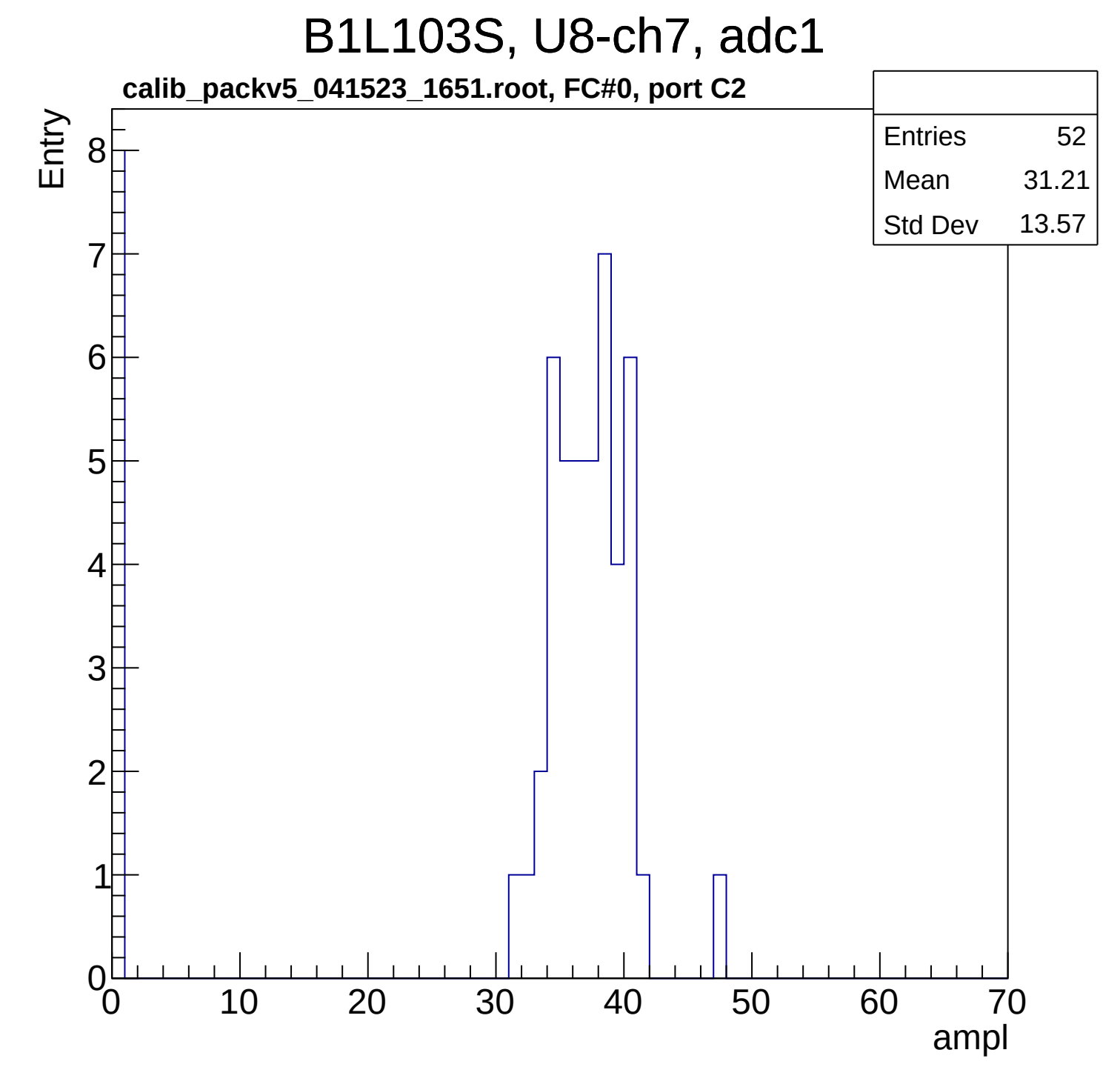
40
50
60
70


B1L103S, U8-ch7, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 31.21
Std Dev 13.57
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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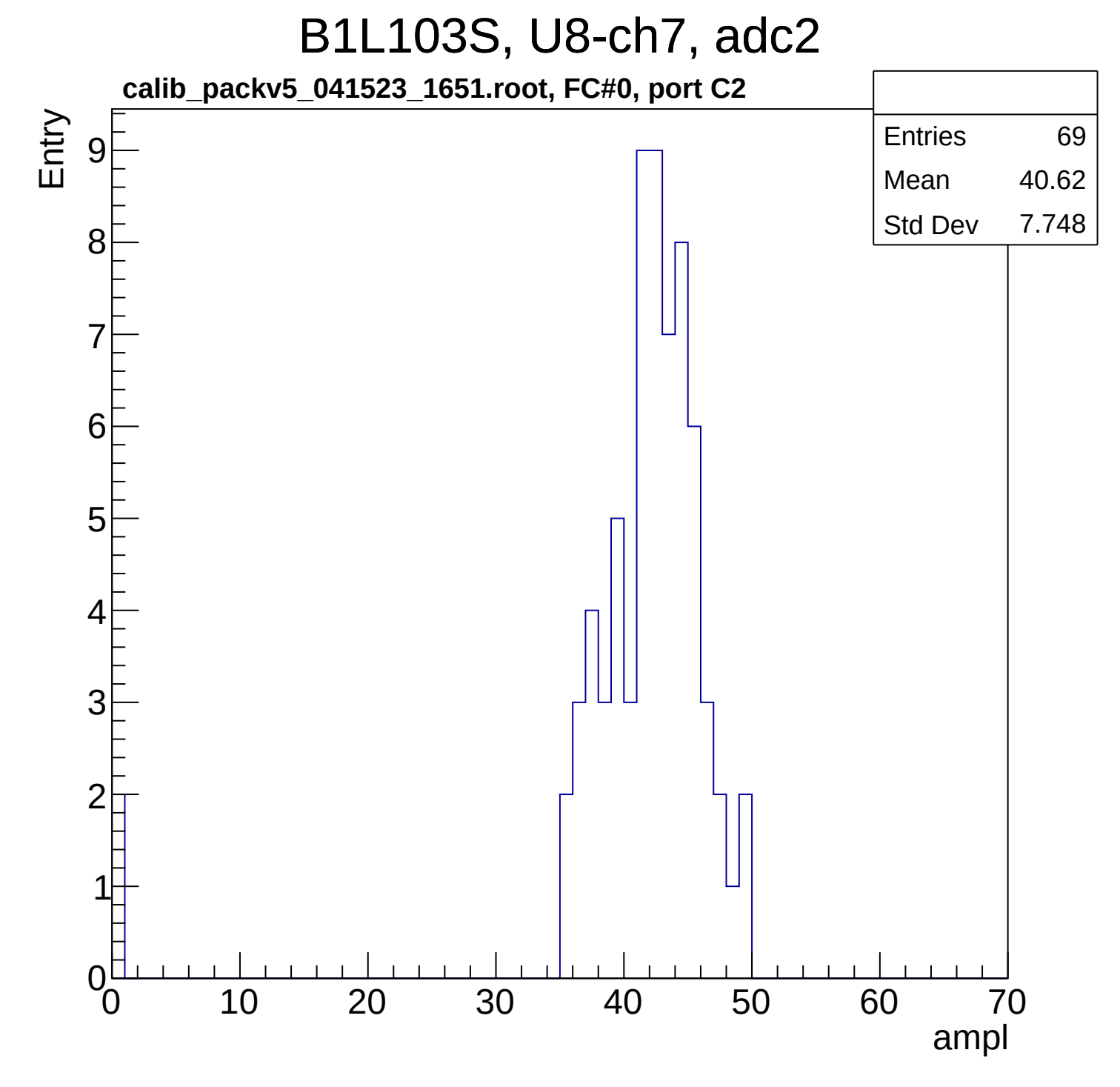
40
50
60
70


B1L103S, U8-ch7, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 40.62
Std Dev 7.748
Entry
ampl
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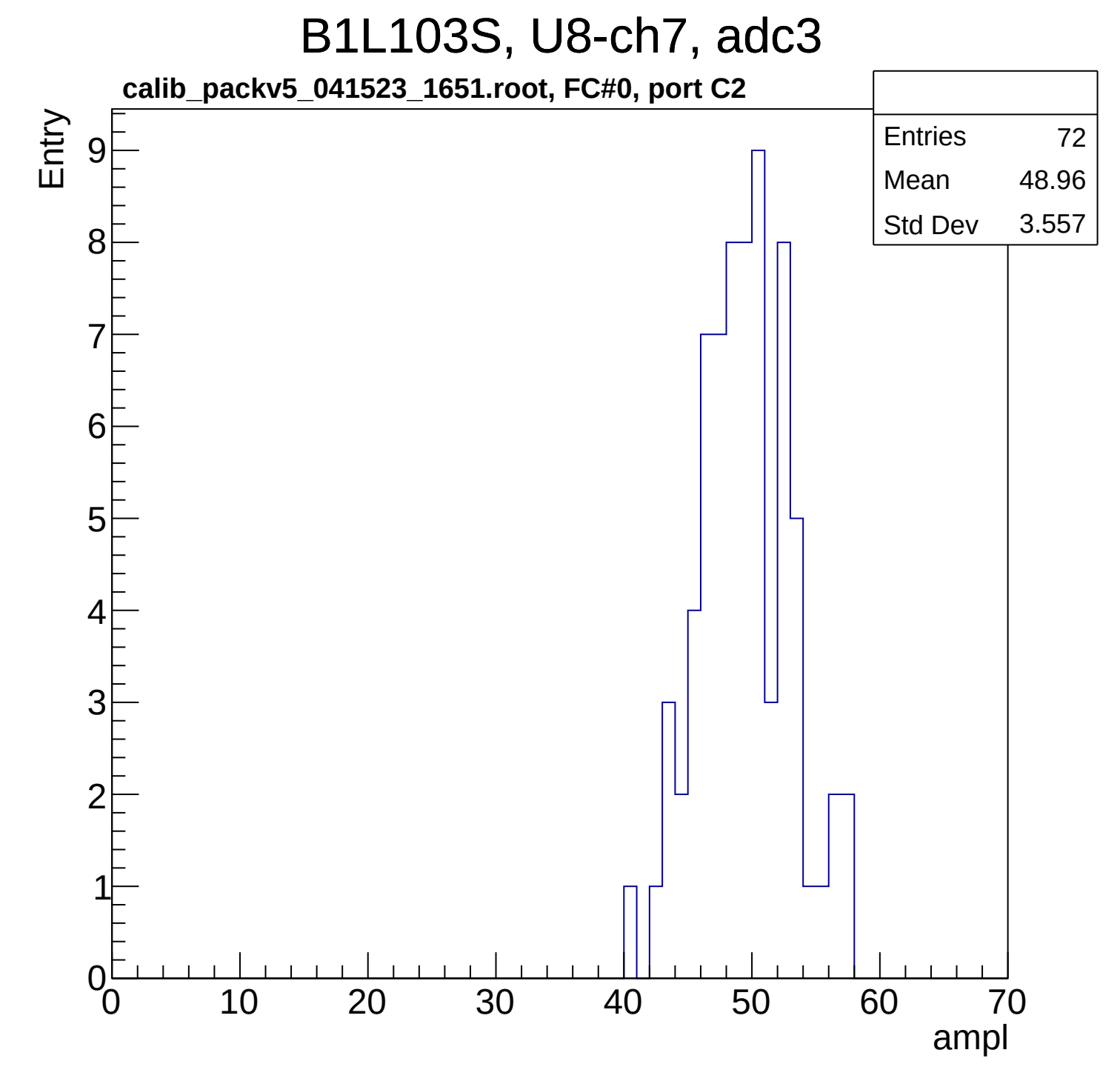
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U8-ch7, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 48.96
Std Dev 3.557
Entry
ampl
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2
3
4
5
6
7
8
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0
10
20
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60
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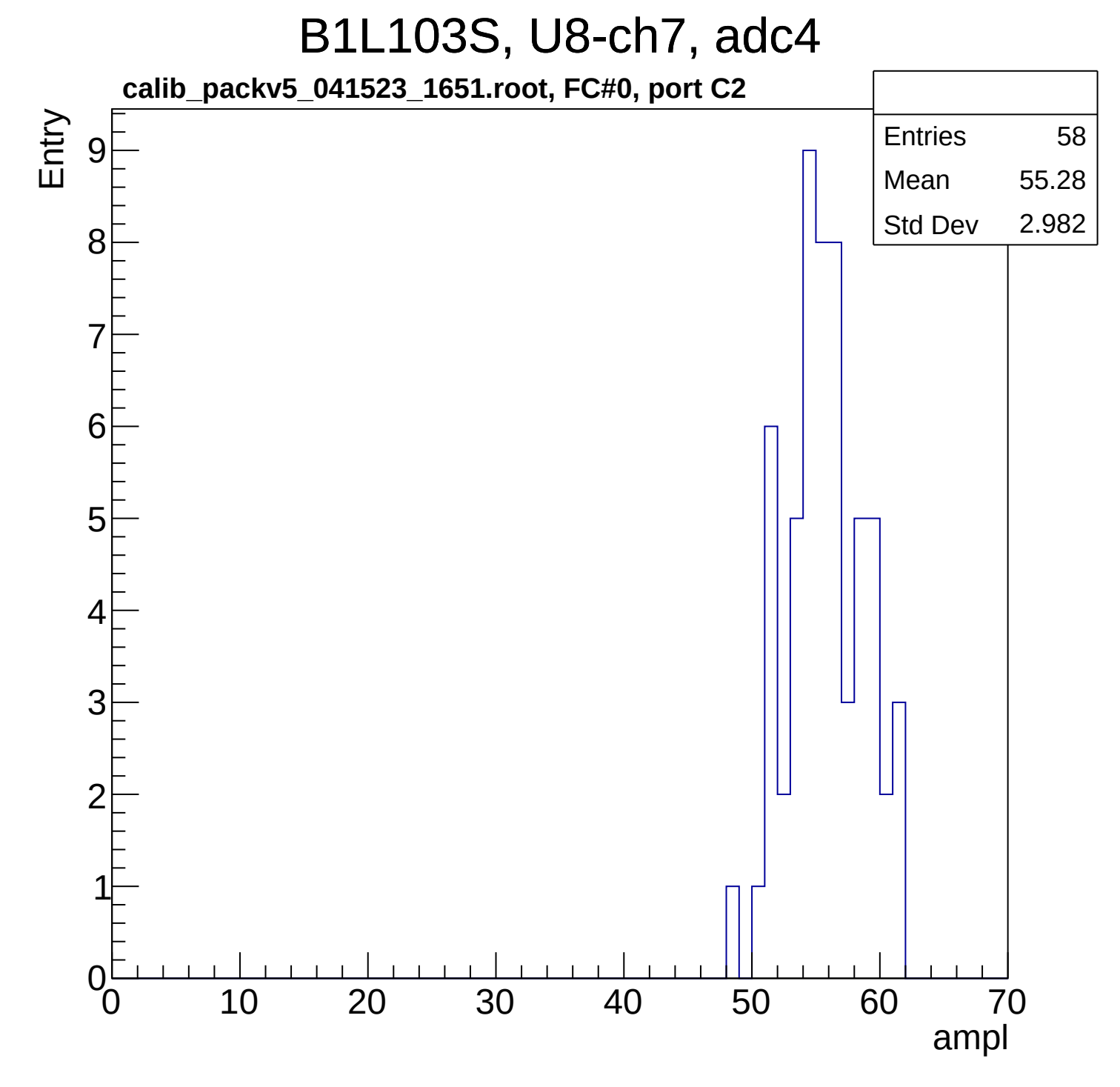
B1L103S, U8-ch7, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 55.28
Std Dev 2.982
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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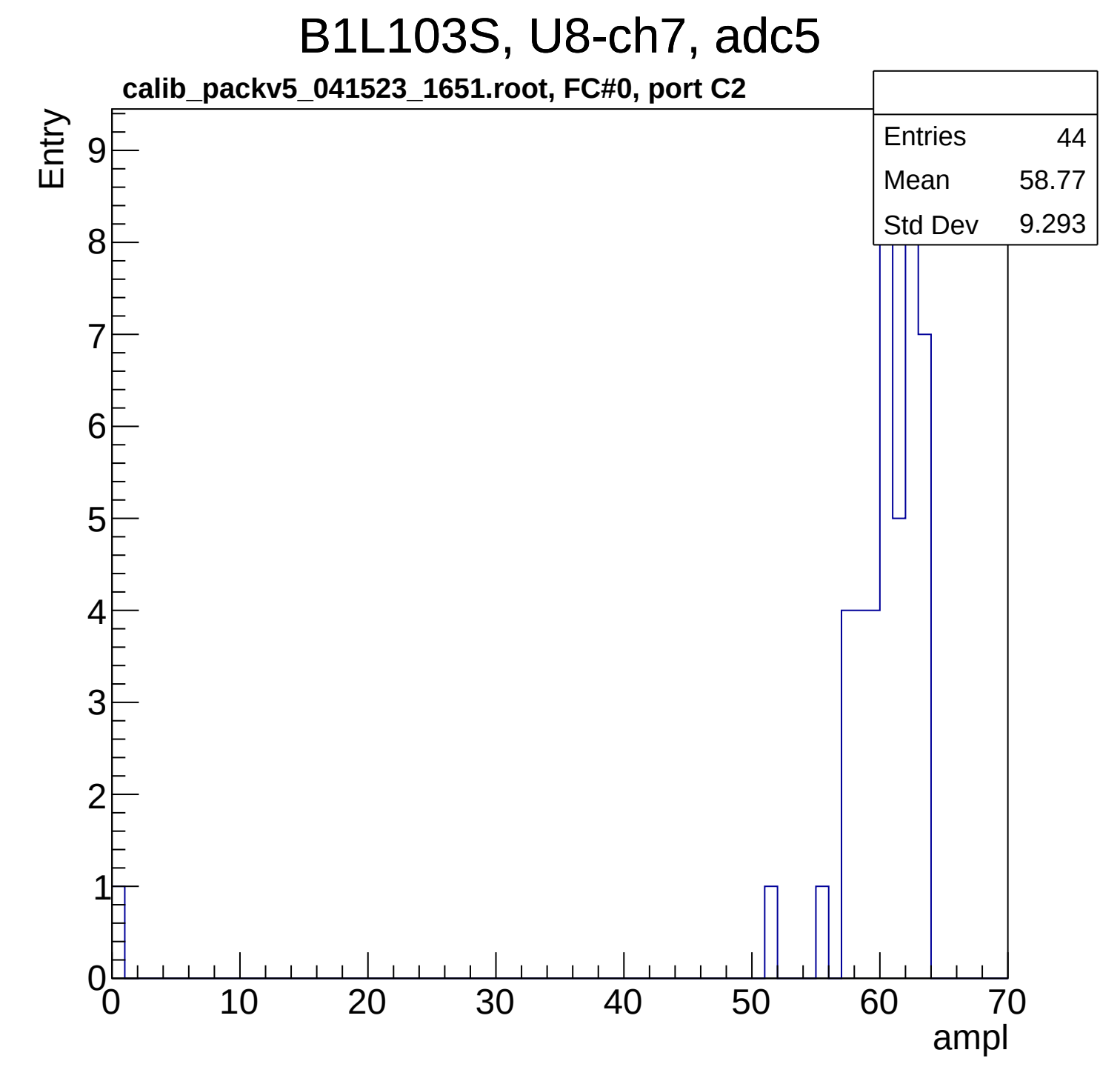
B1L103S, U8-ch7, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 58.77
Std Dev 9.293
Entry
ampl
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3
4
5
6
7
8
9
0
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20
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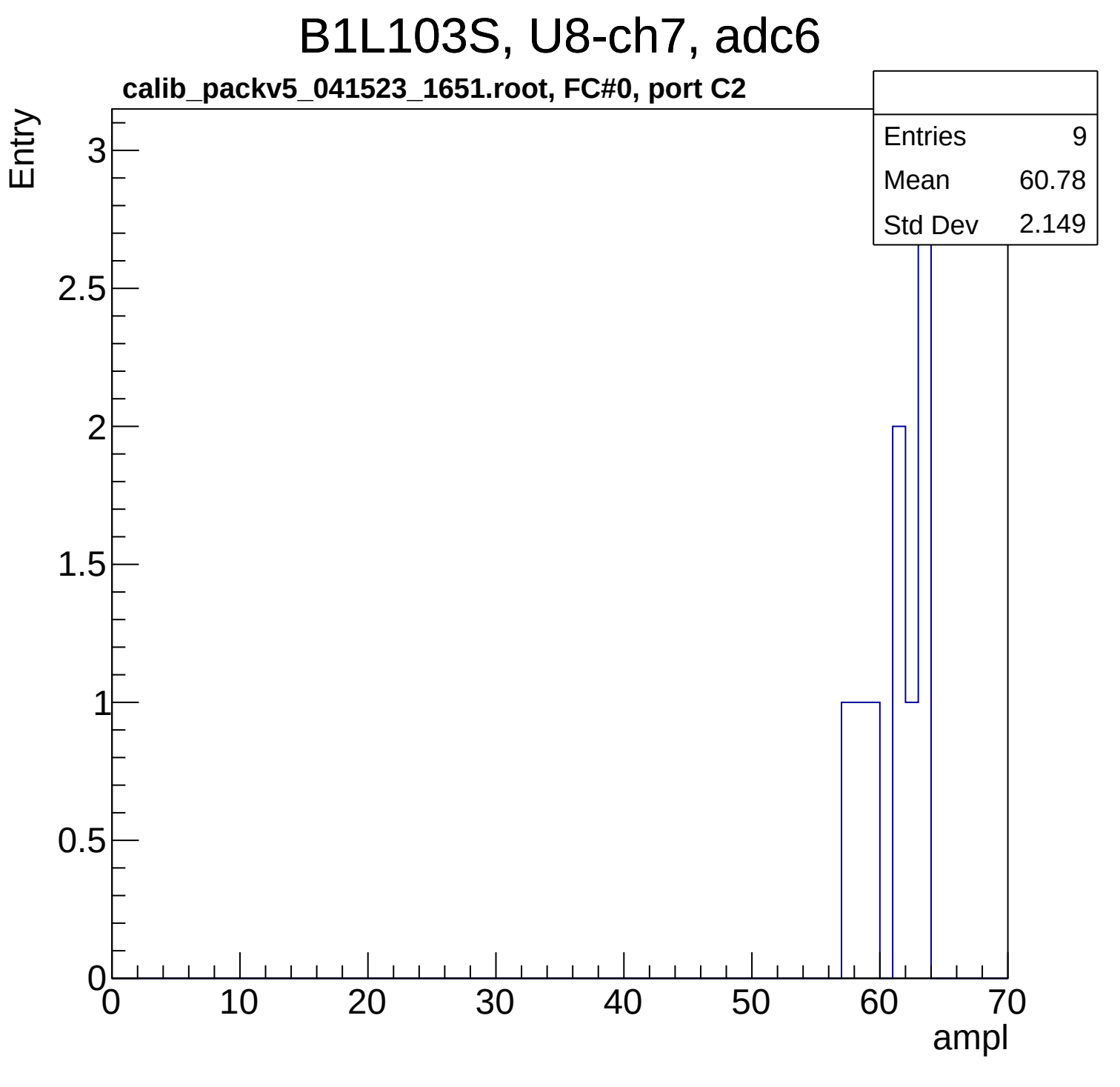
40
50
60
70


B1L103S, U8-ch7, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 60.78
Std Dev 2.149
Entry
ampl
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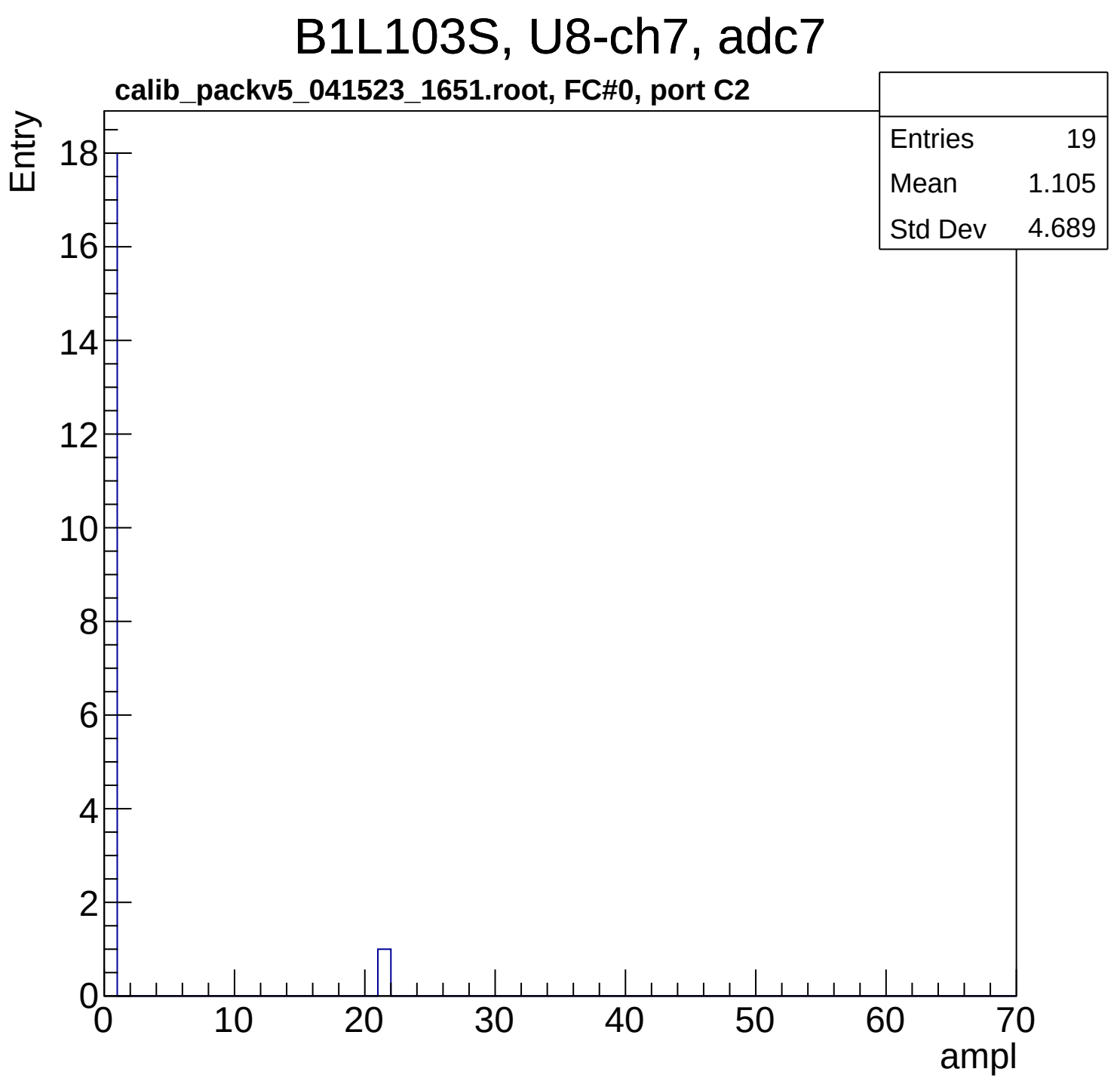
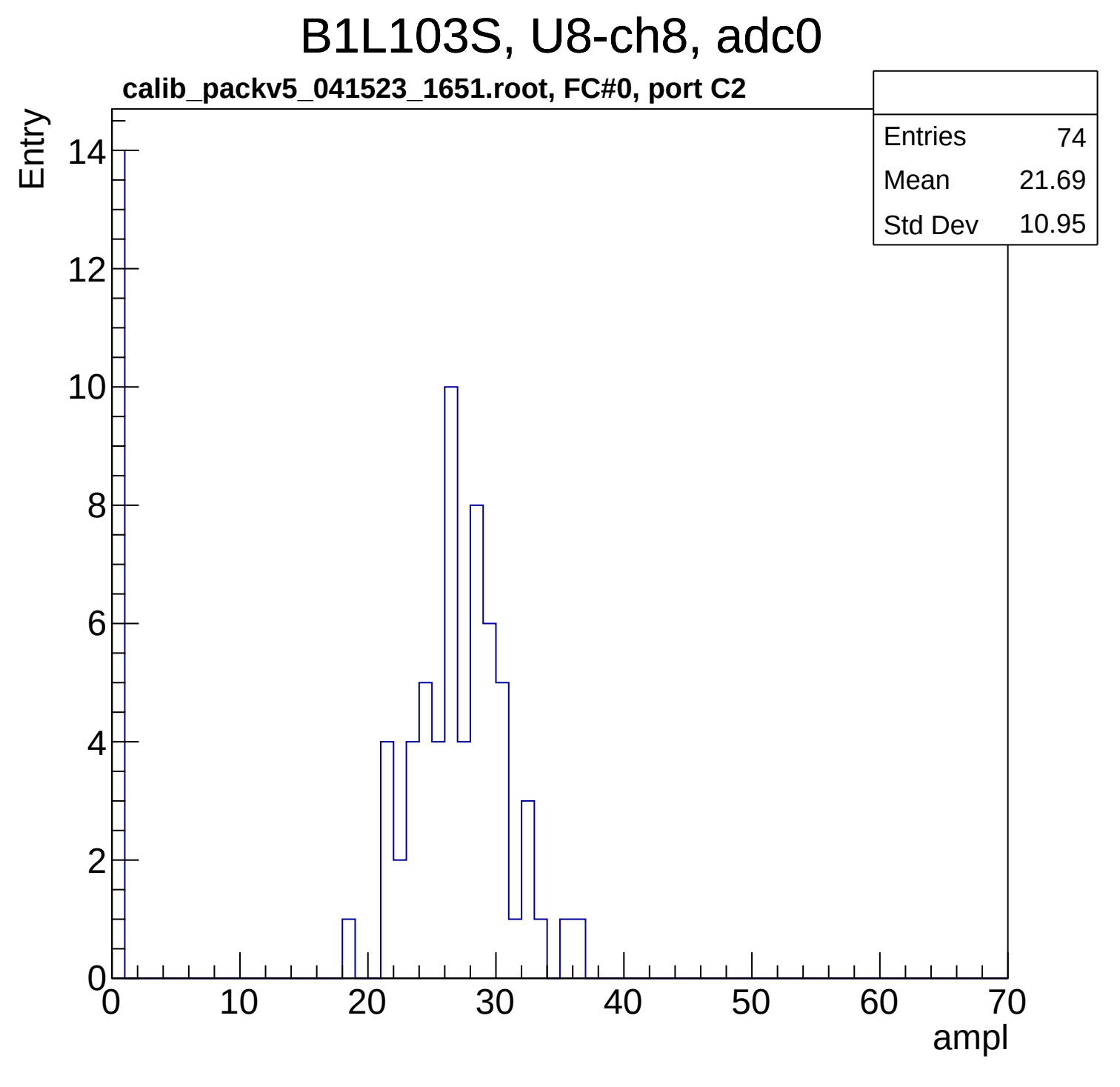
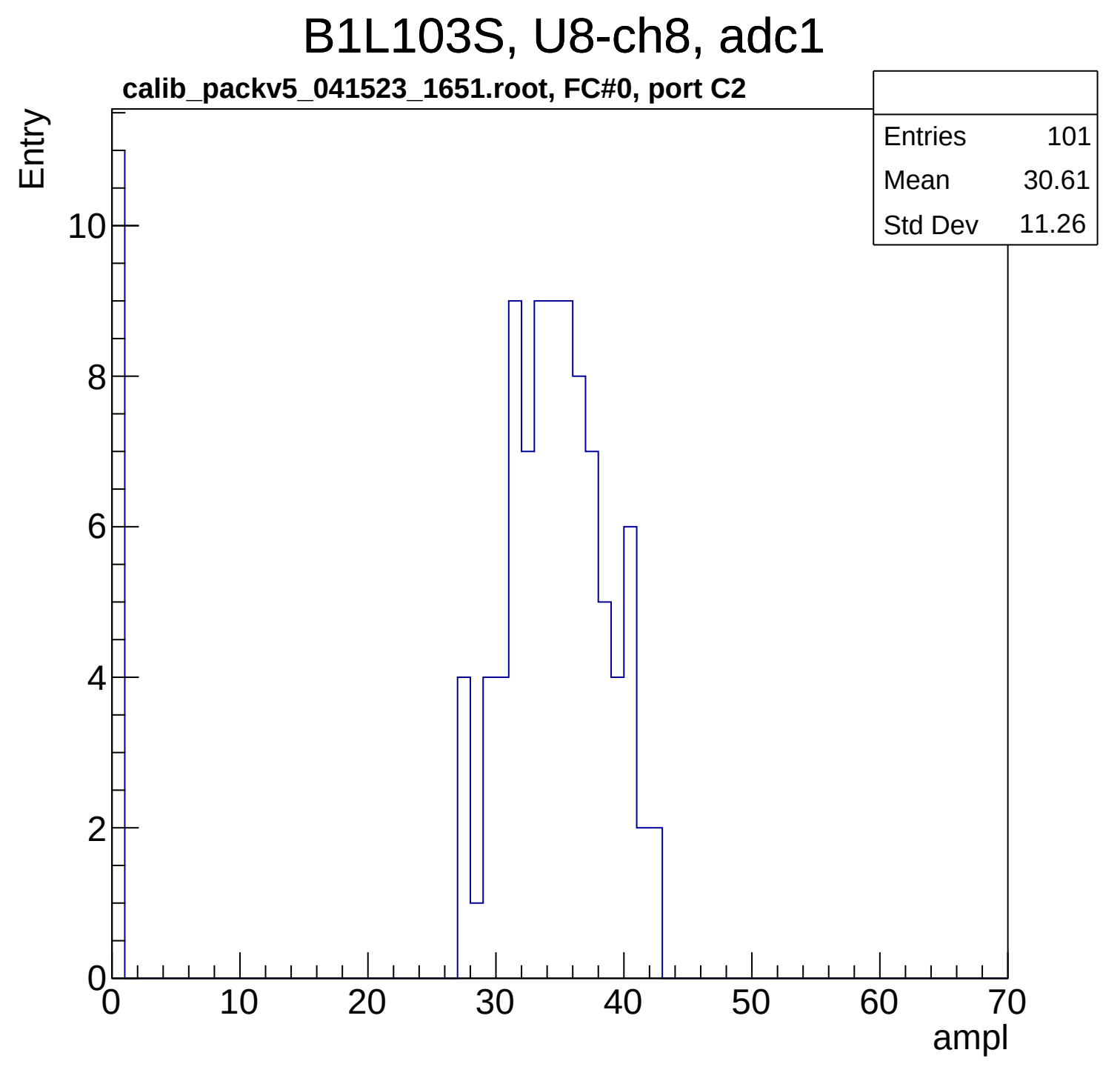
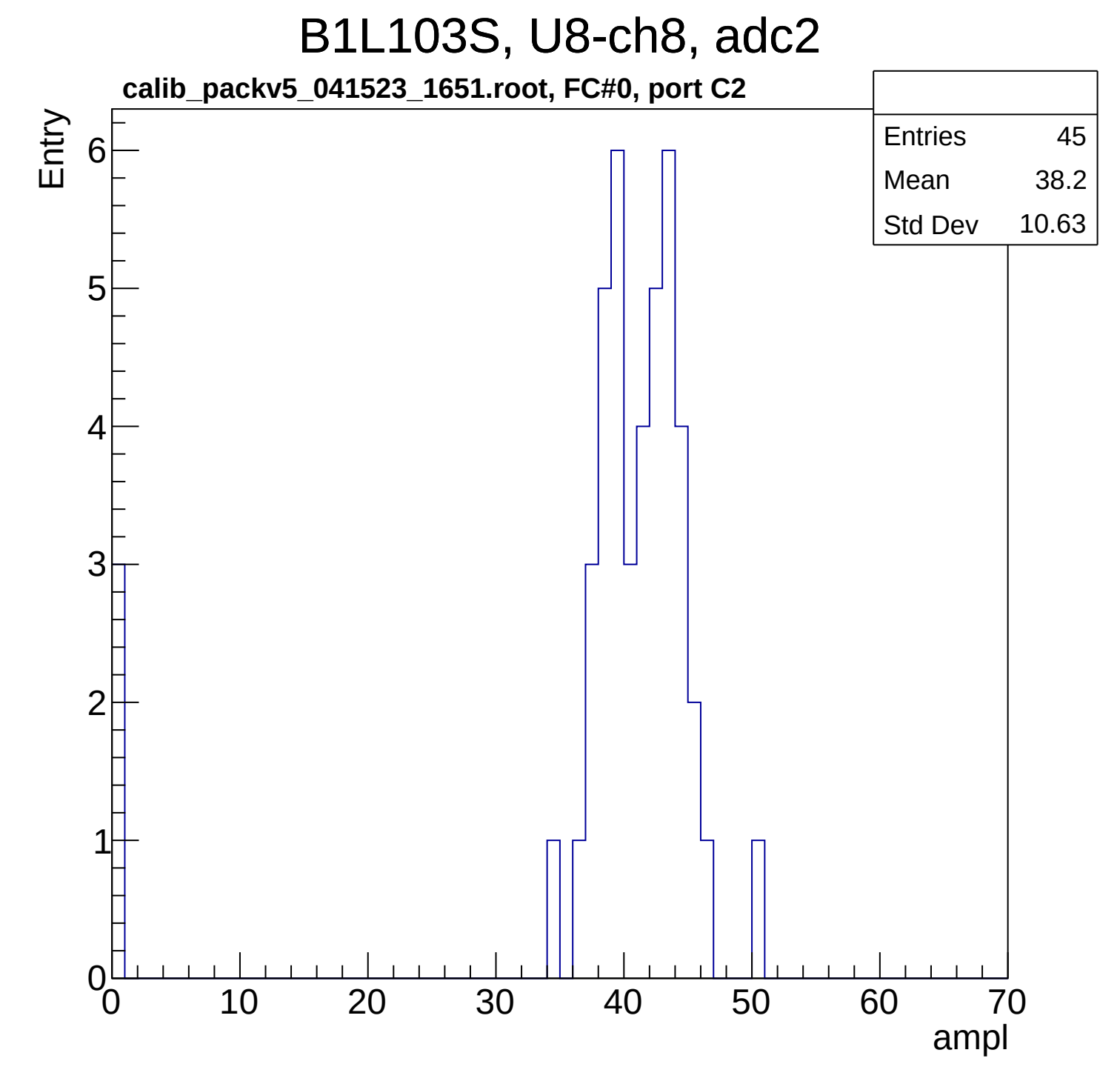
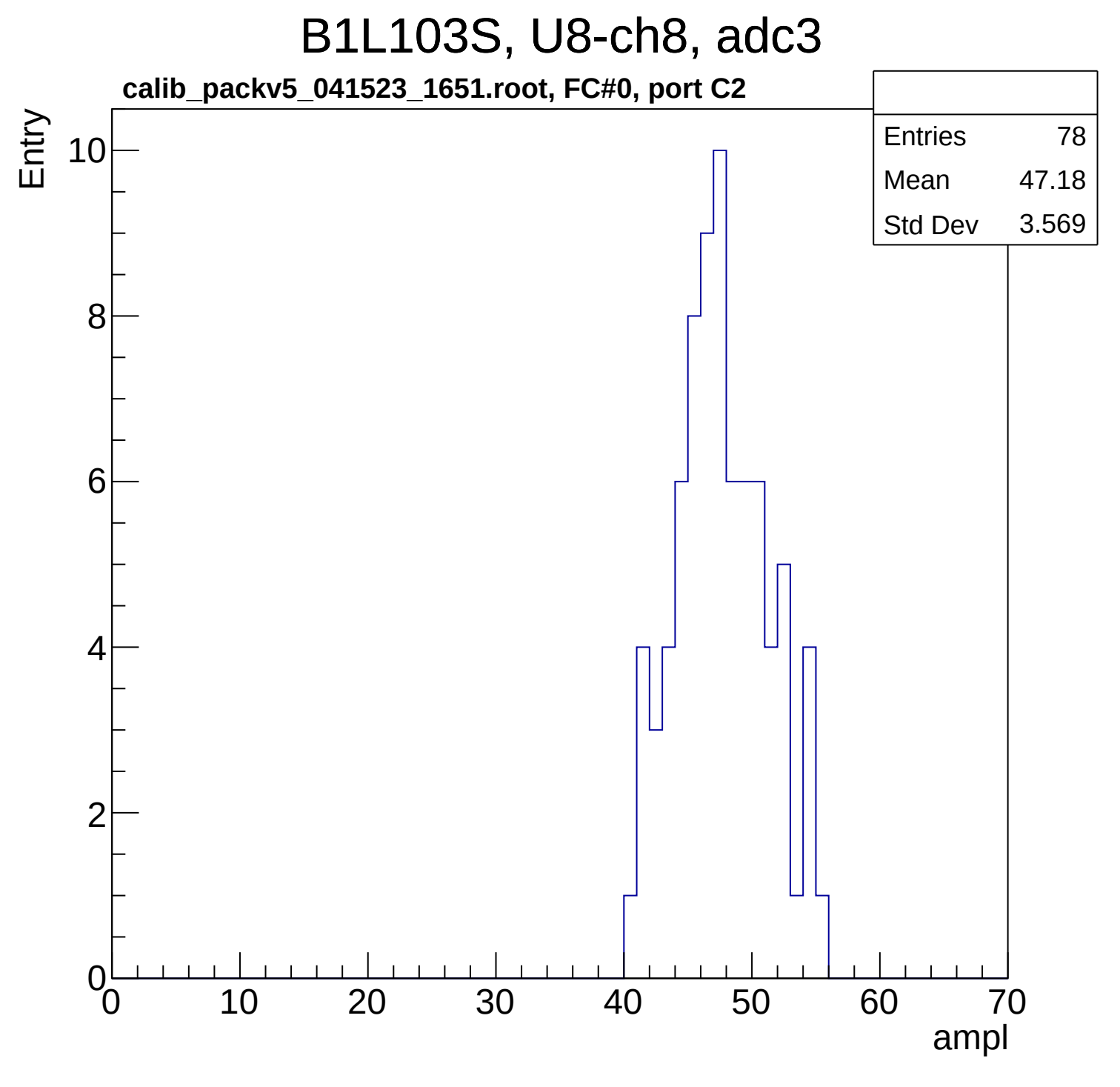
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

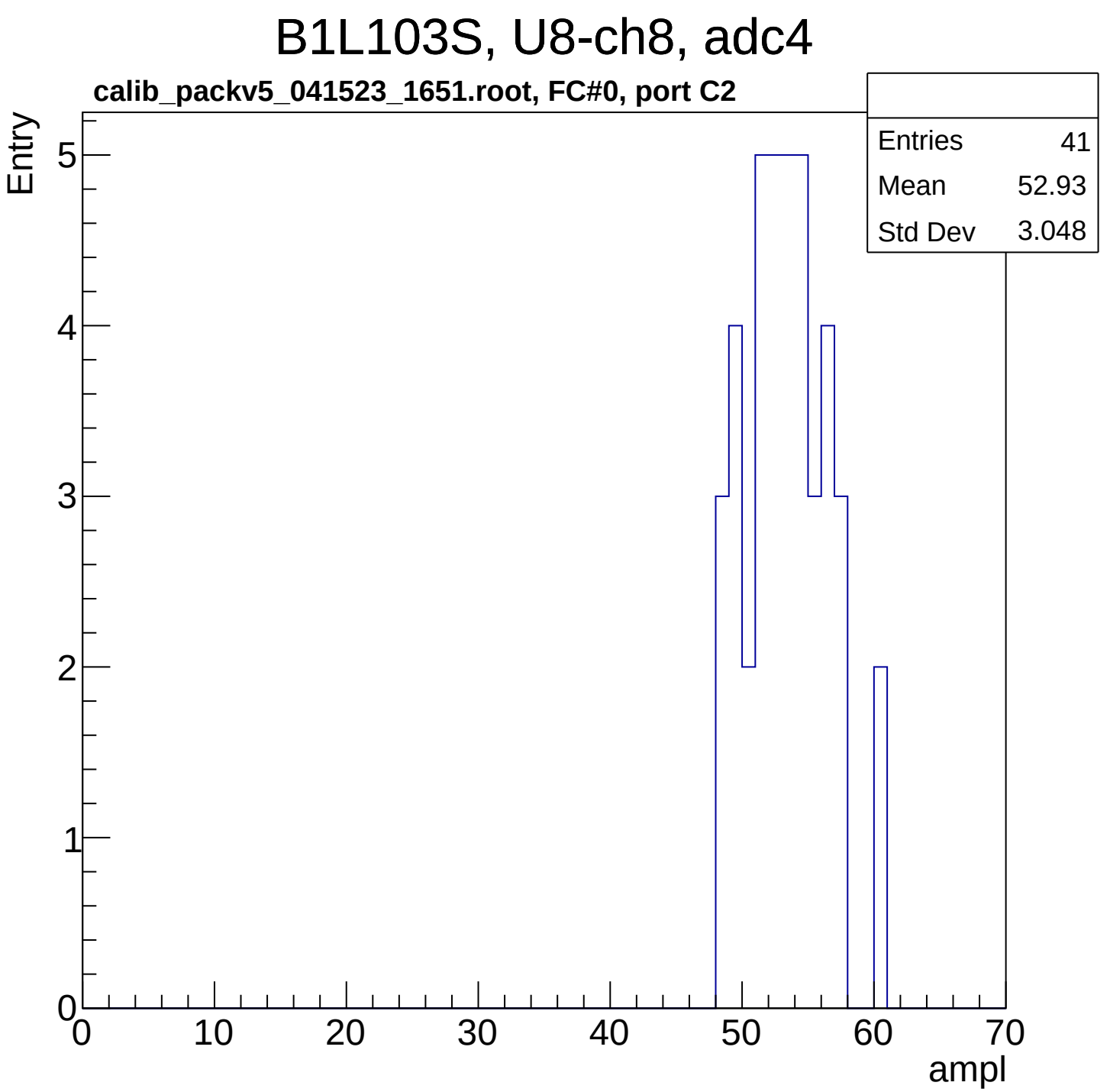

B1L103S, U8-ch7, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.105
Std Dev 4.689
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

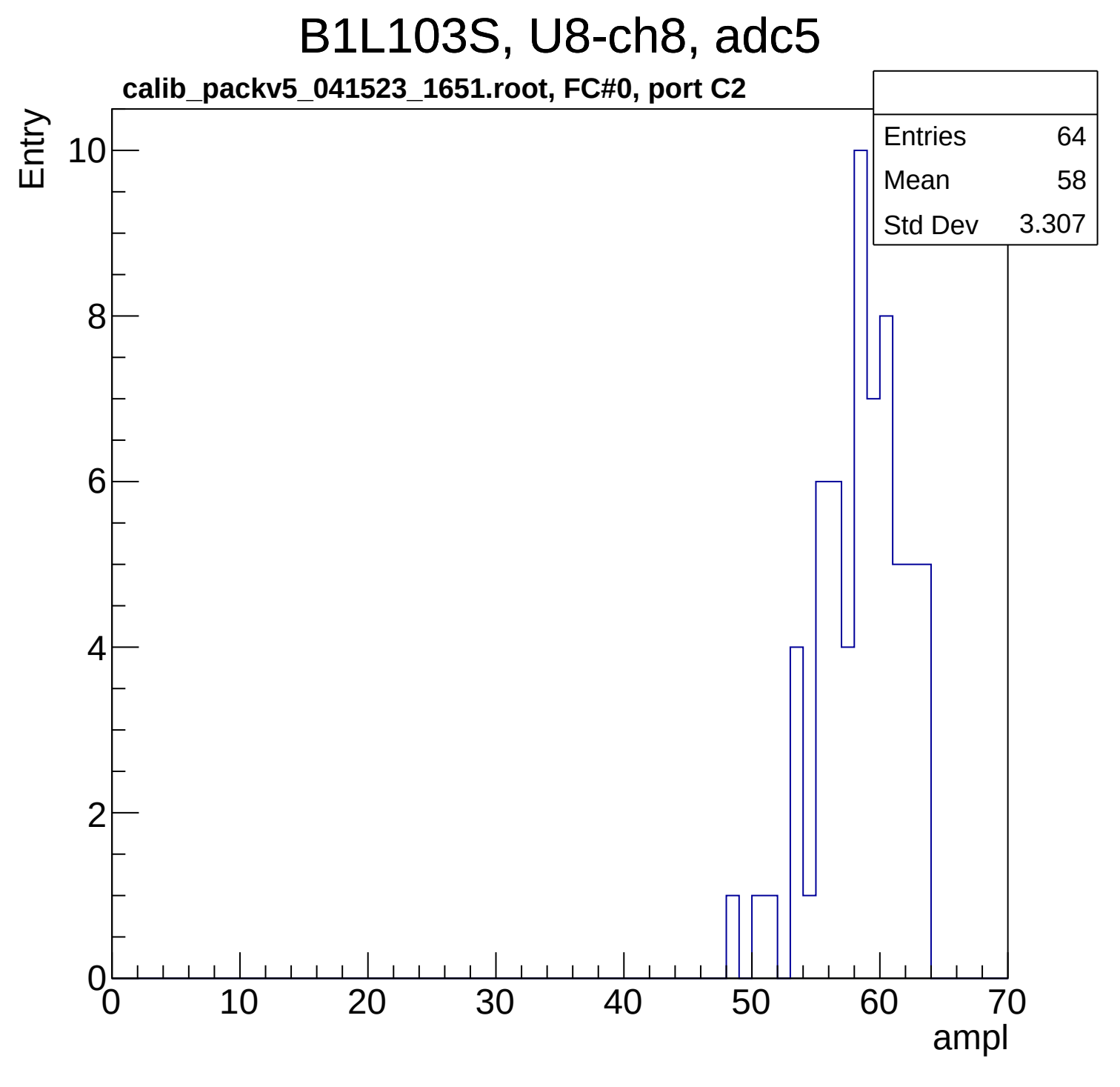

B1L103S, U8-ch8, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 21.69
Std Dev 10.95
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

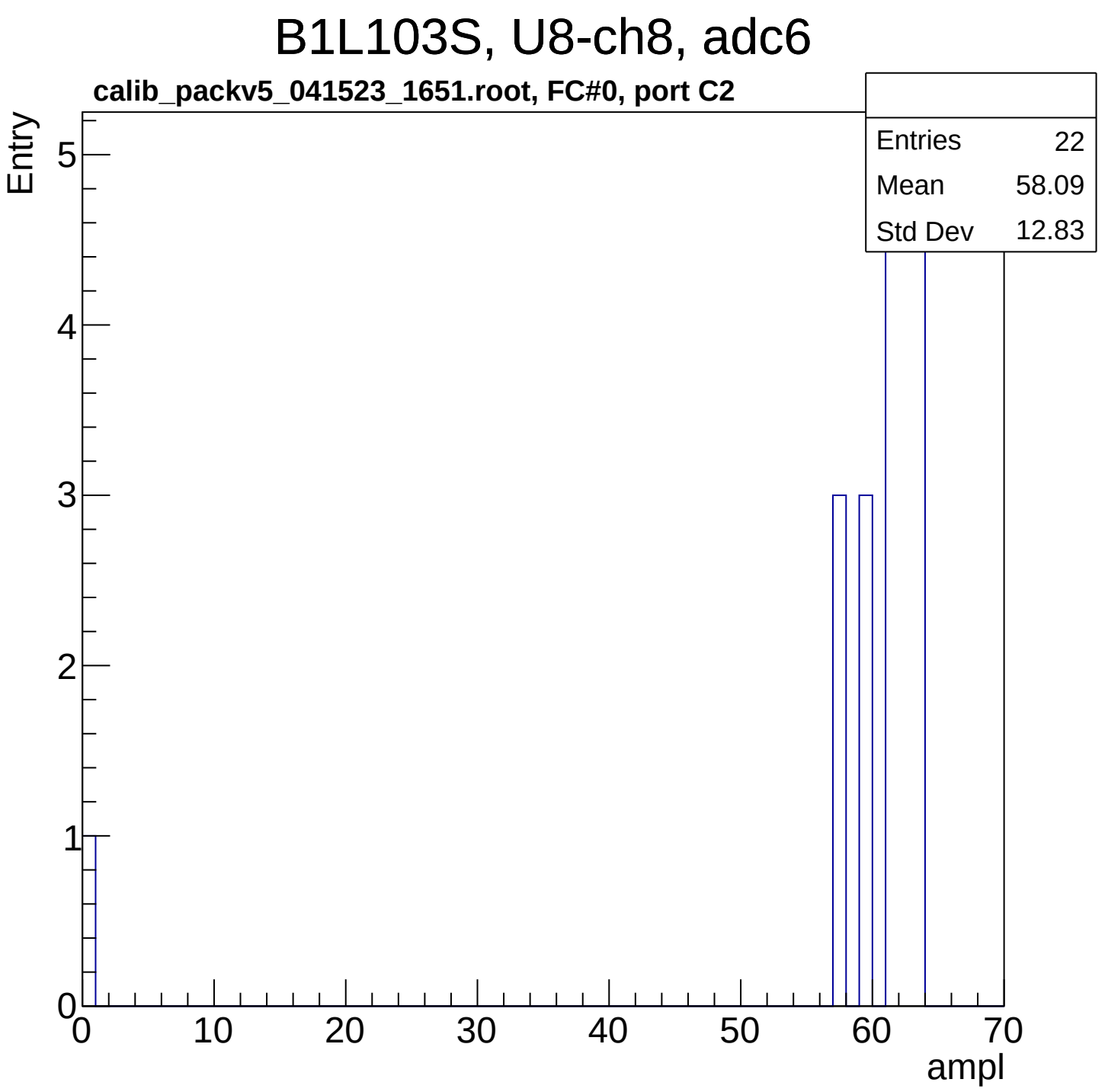

B1L103S, U8-ch8, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 101
Mean 30.61
Std Dev 11.26
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

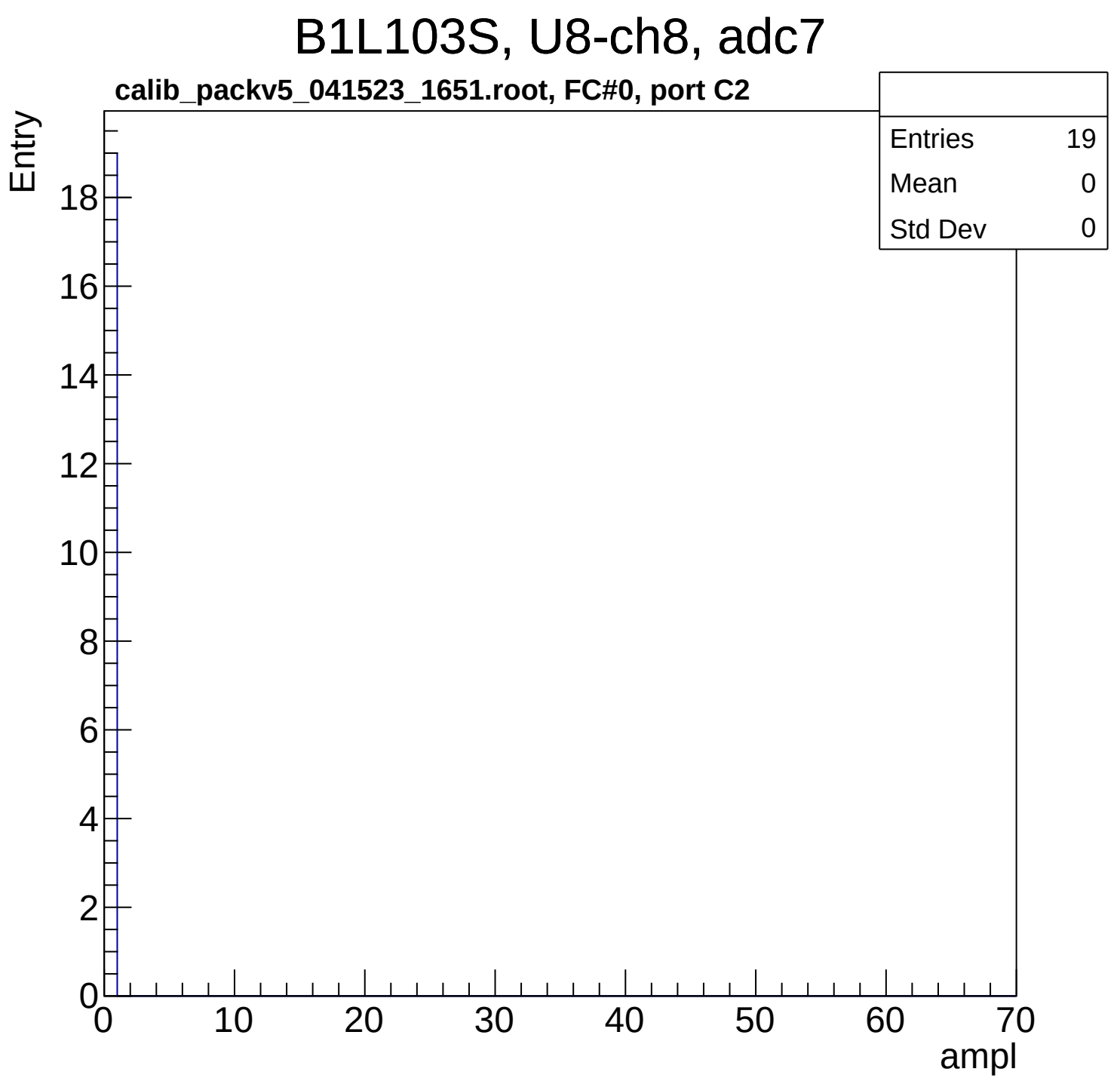

B1L103S, U8-ch8, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 38.2
Std Dev 10.63
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

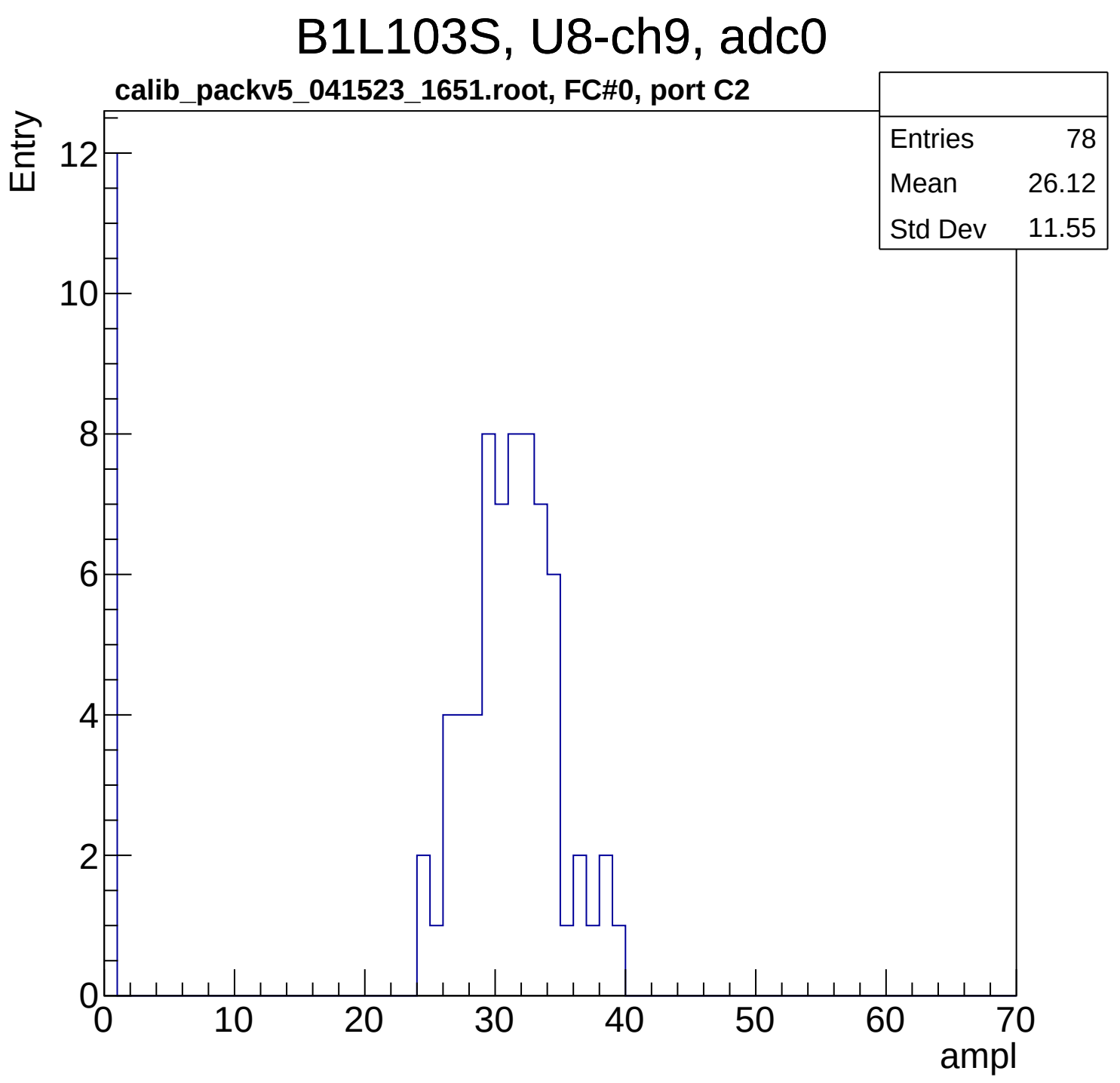

B1L103S, U8-ch8, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 47.18
Std Dev 3.569
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

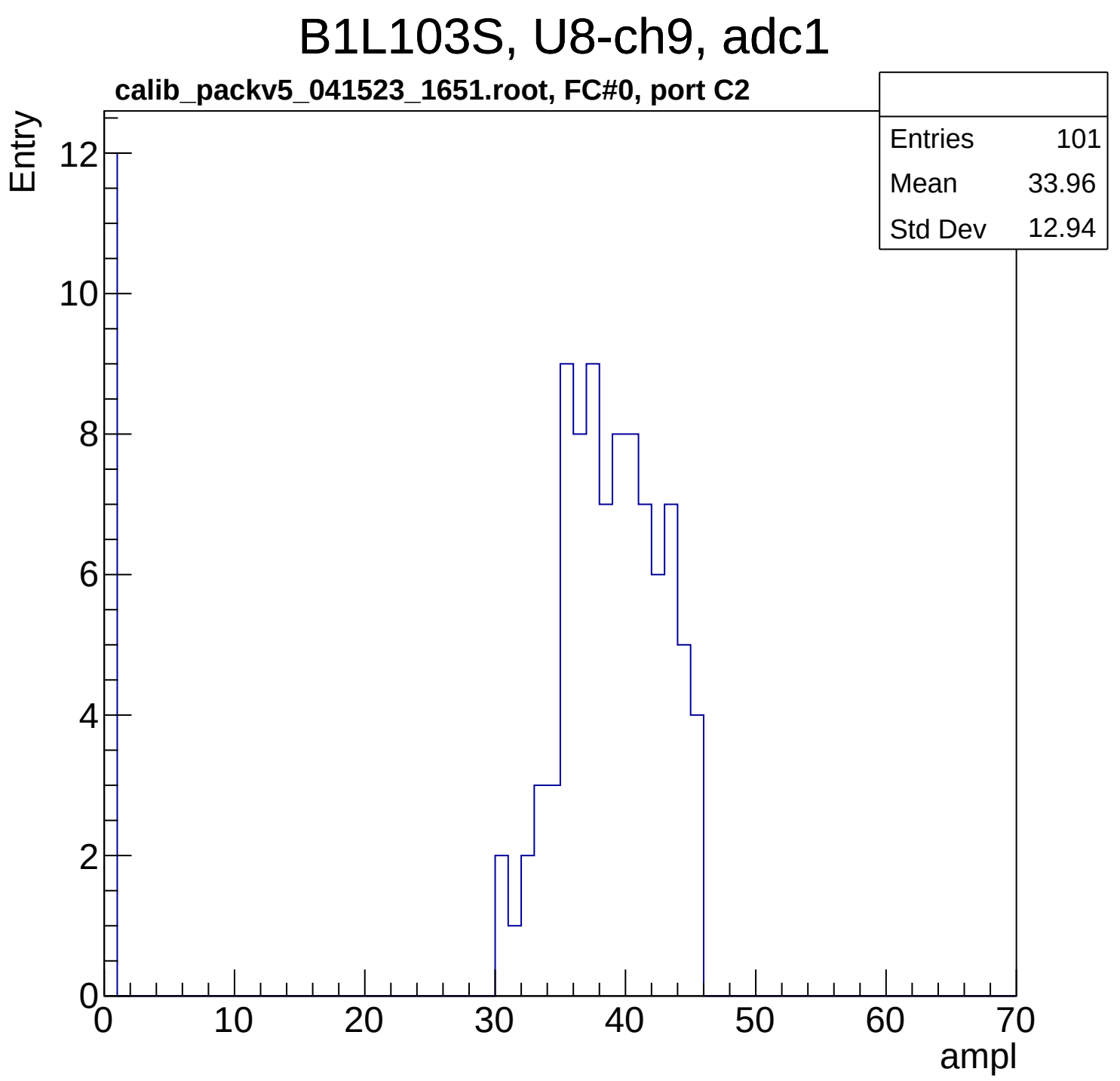

B1L103S, U8-ch8, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 52.93
Std Dev 3.048
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

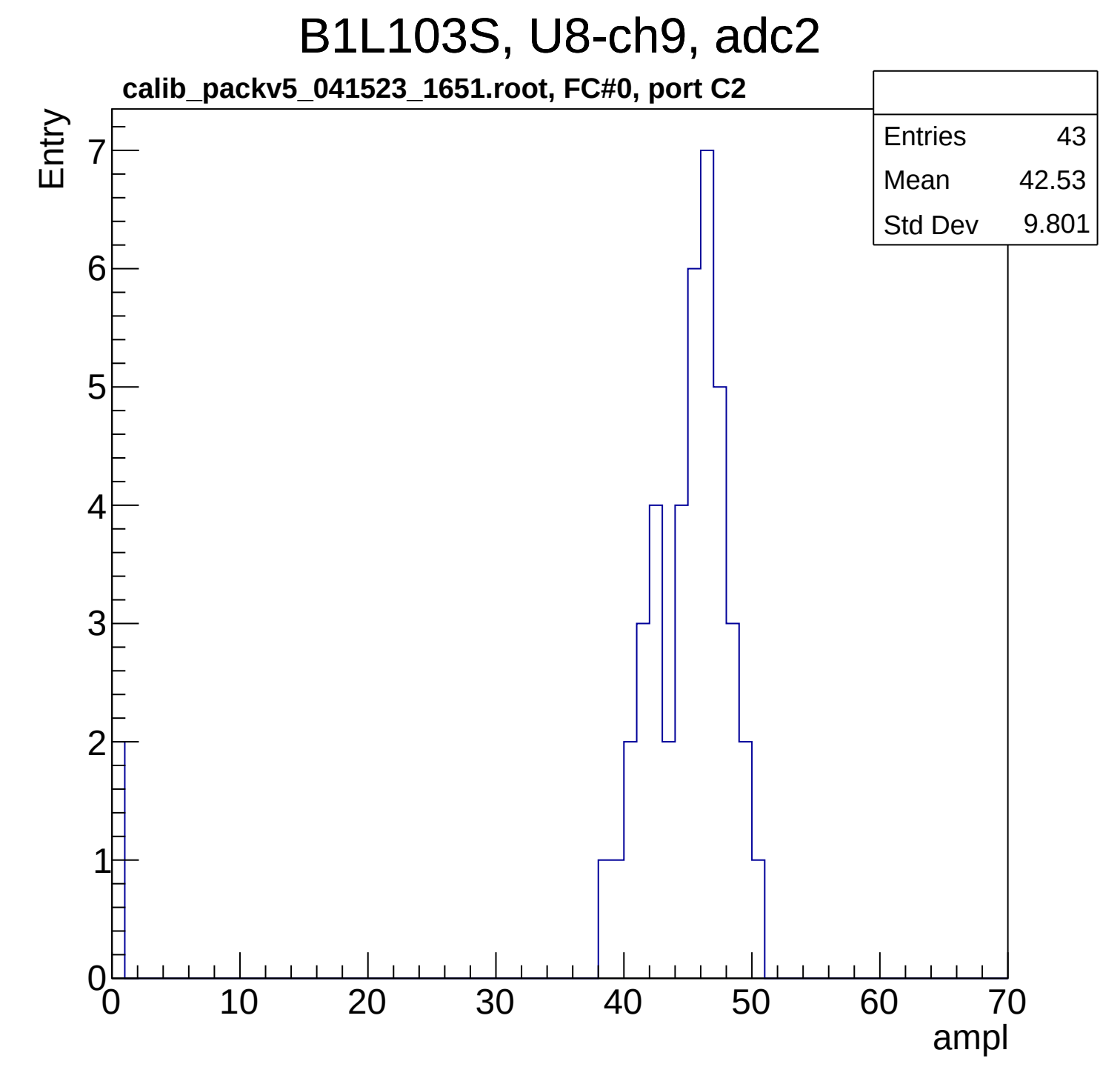

B1L103S, U8-ch8, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 58
Std Dev 3.307
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

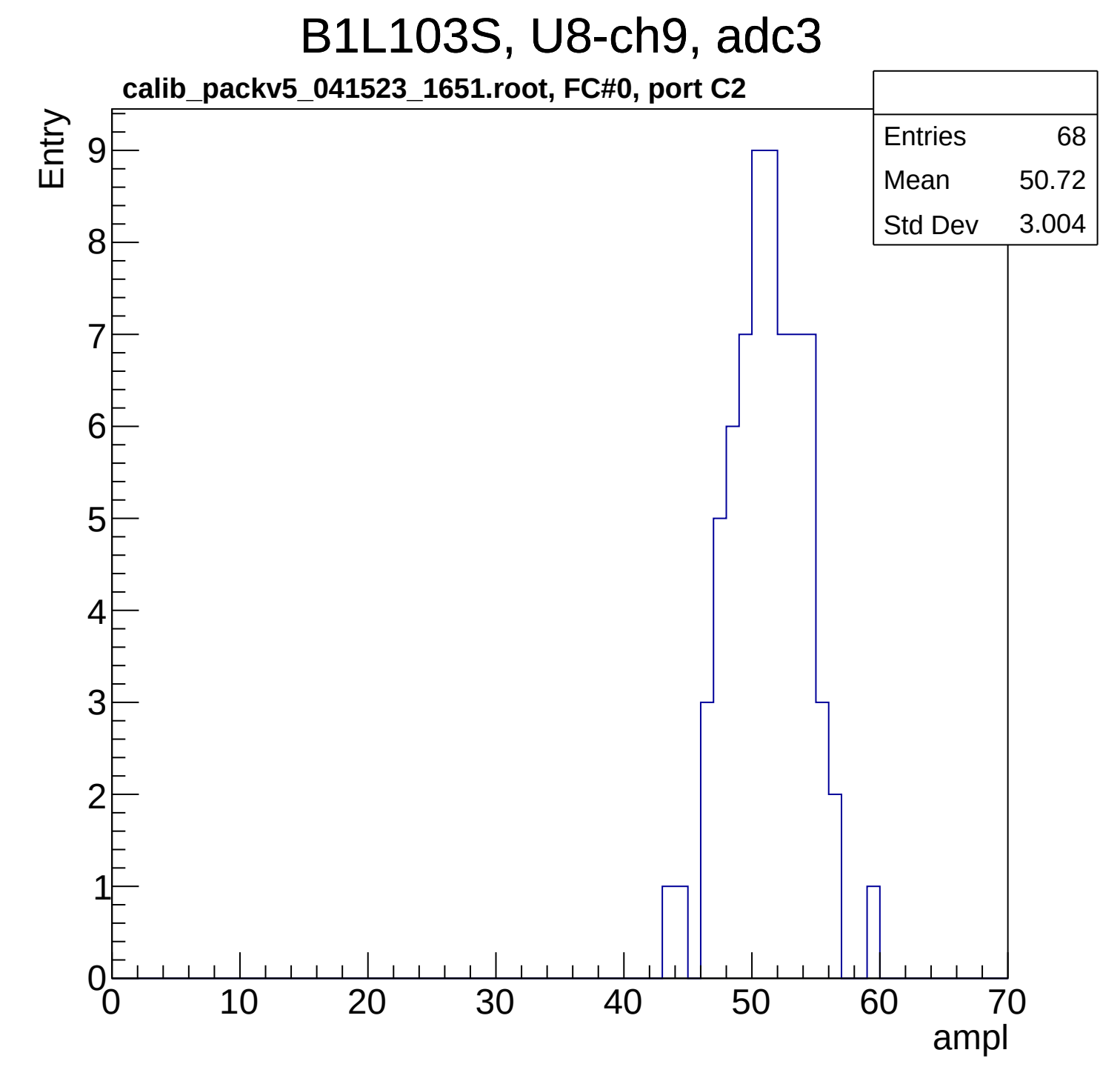

B1L103S, U8-ch8, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 58.09
Std Dev 12.83
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

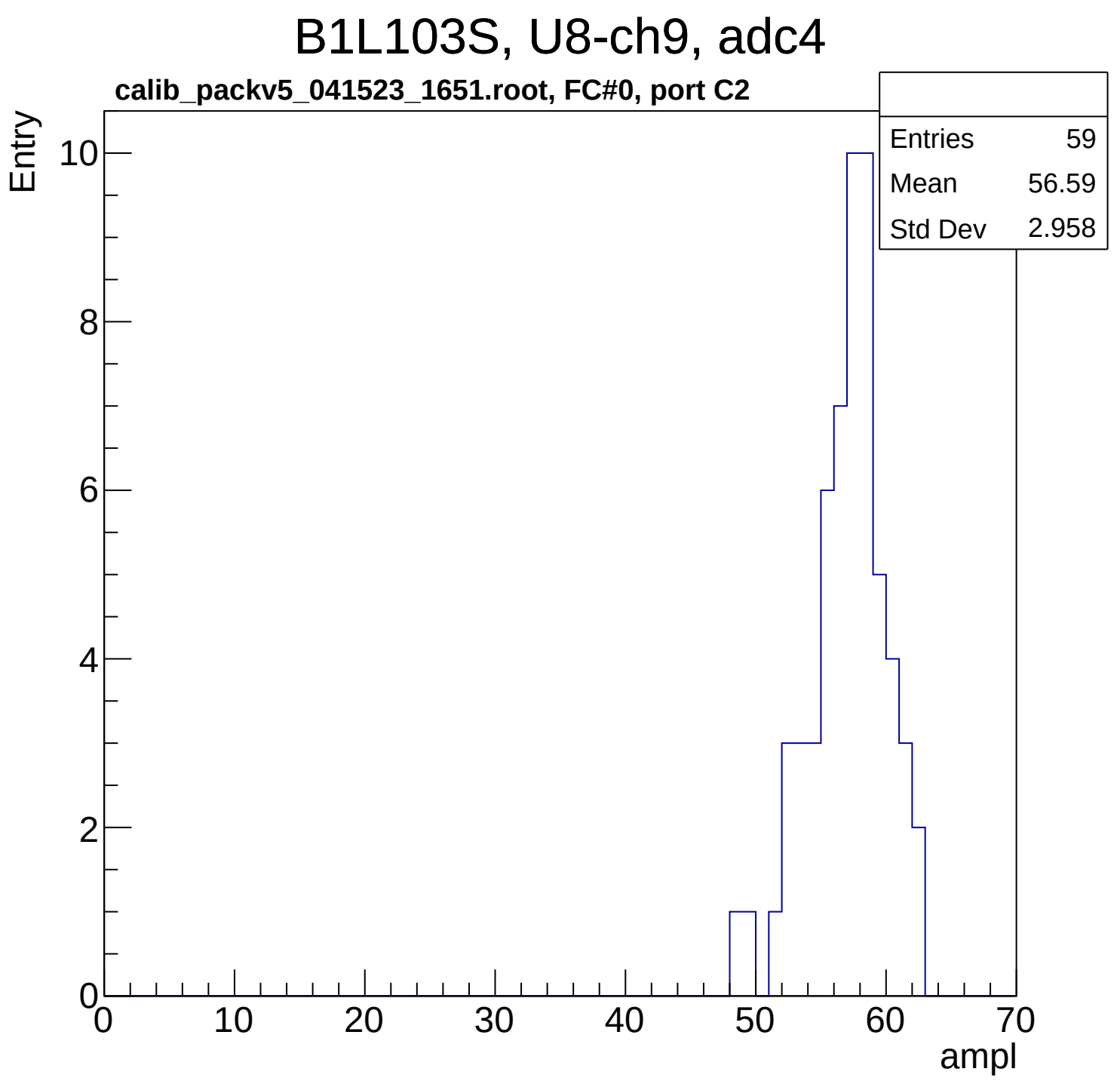

B1L103S, U8-ch8, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

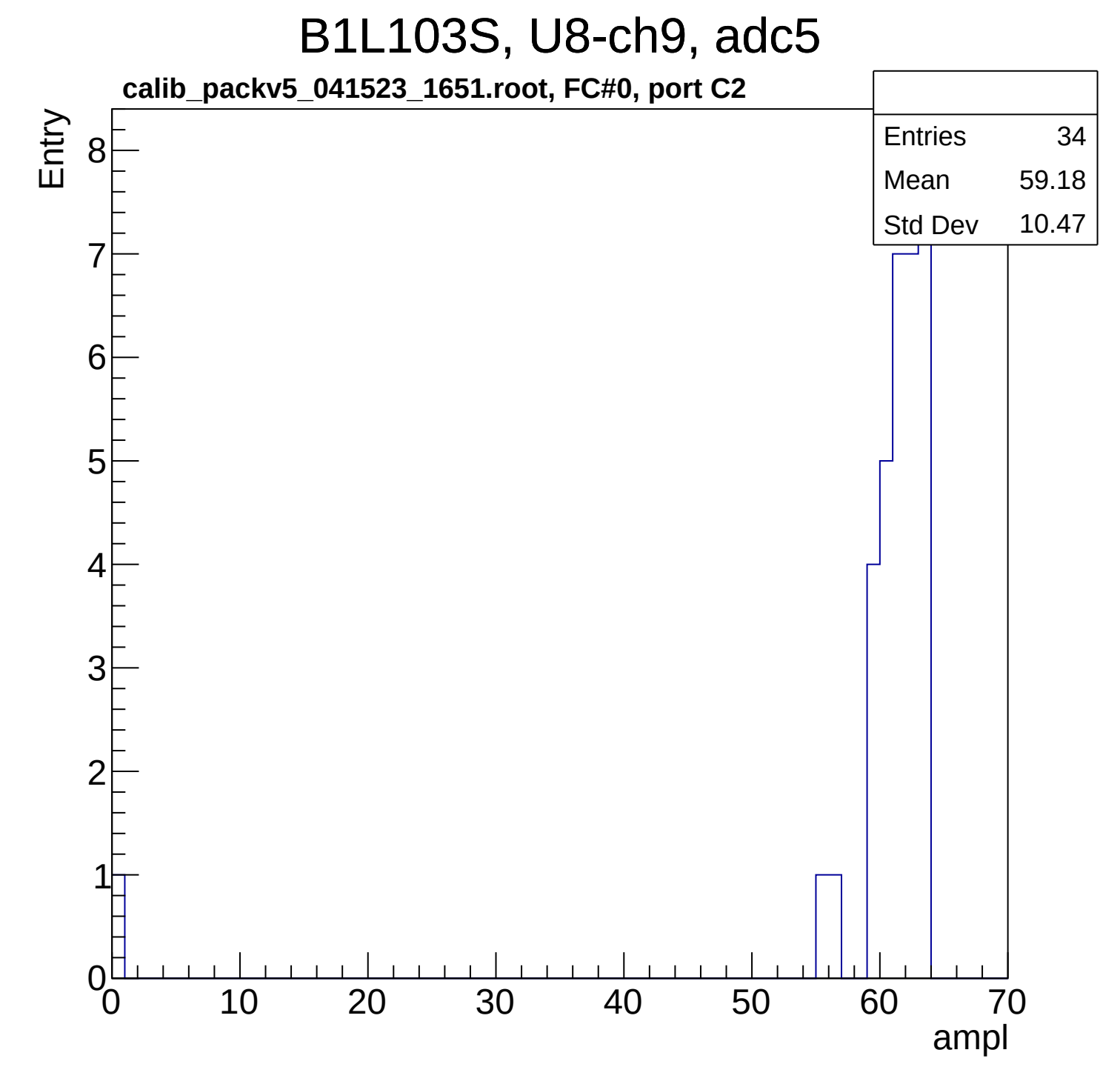

B1L103S, U8-ch9, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 26.12
Std Dev 11.55
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch9, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 101
Mean 33.96
Std Dev 12.94
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U8-ch9, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 42.53
Std Dev 9.801
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U8-ch9, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 50.72
Std Dev 3.004
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U8-ch9, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 56.59
Std Dev 2.958
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch9, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 59.18
Std Dev 10.47
Entry
ampl
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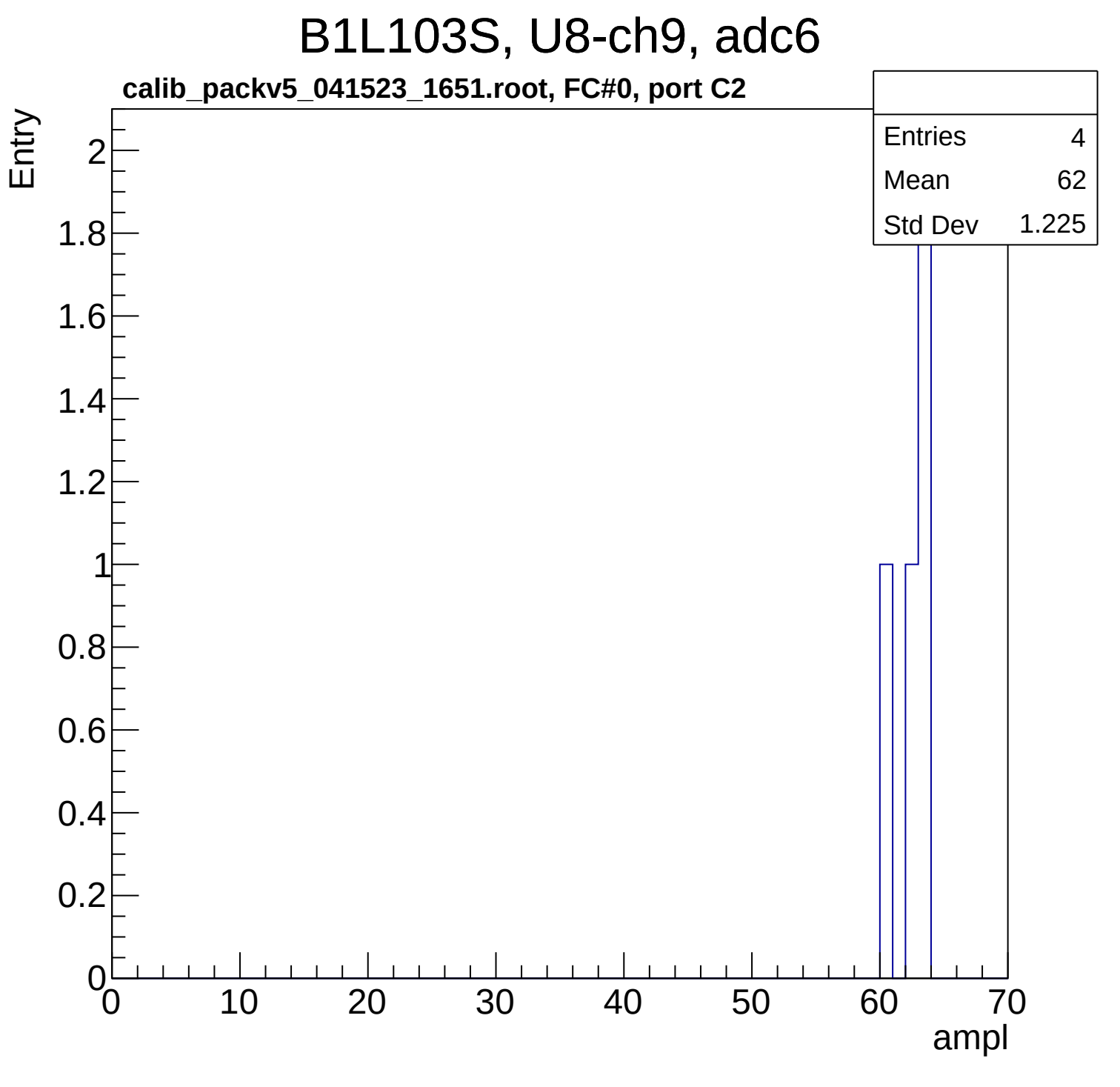
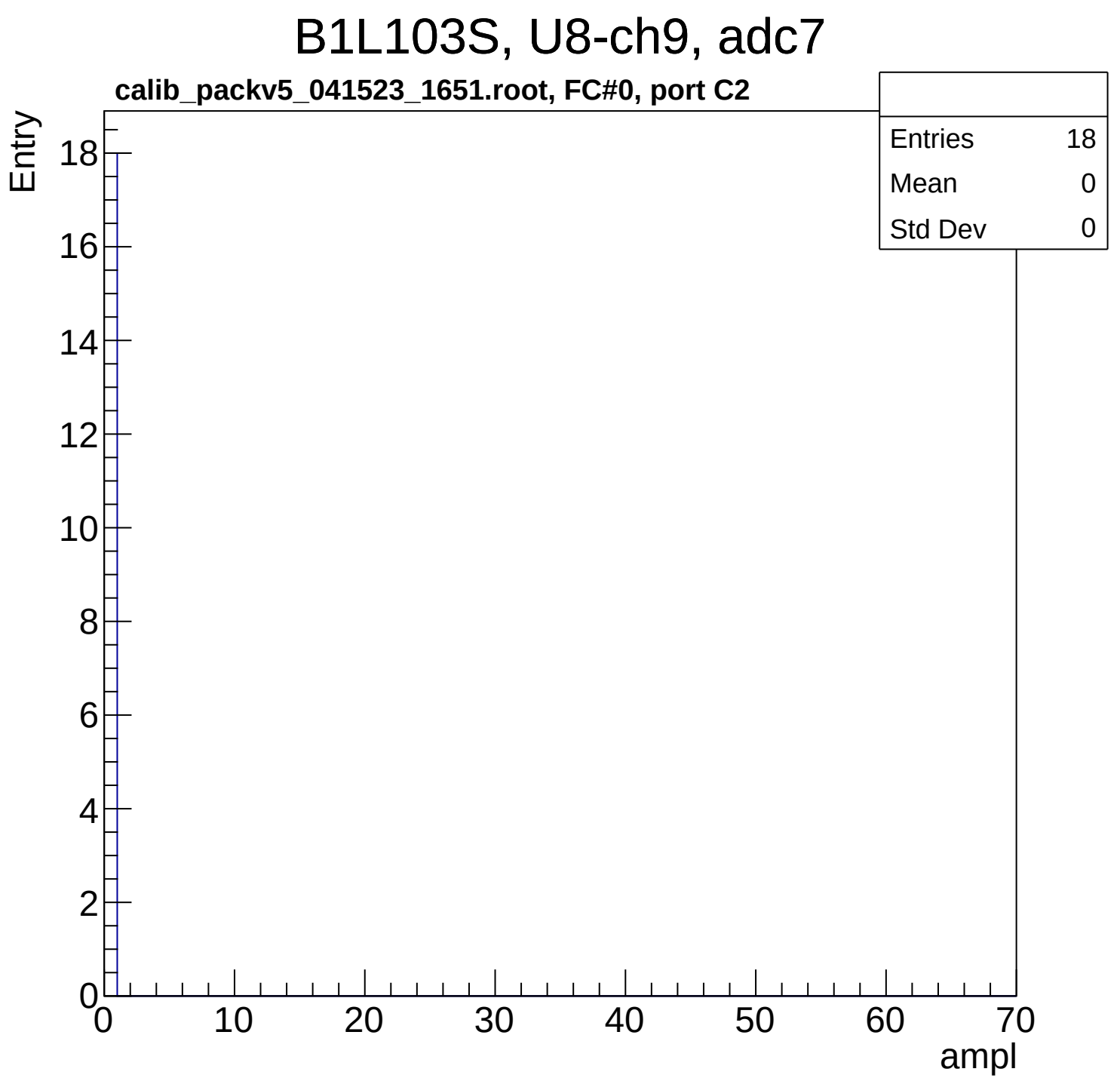
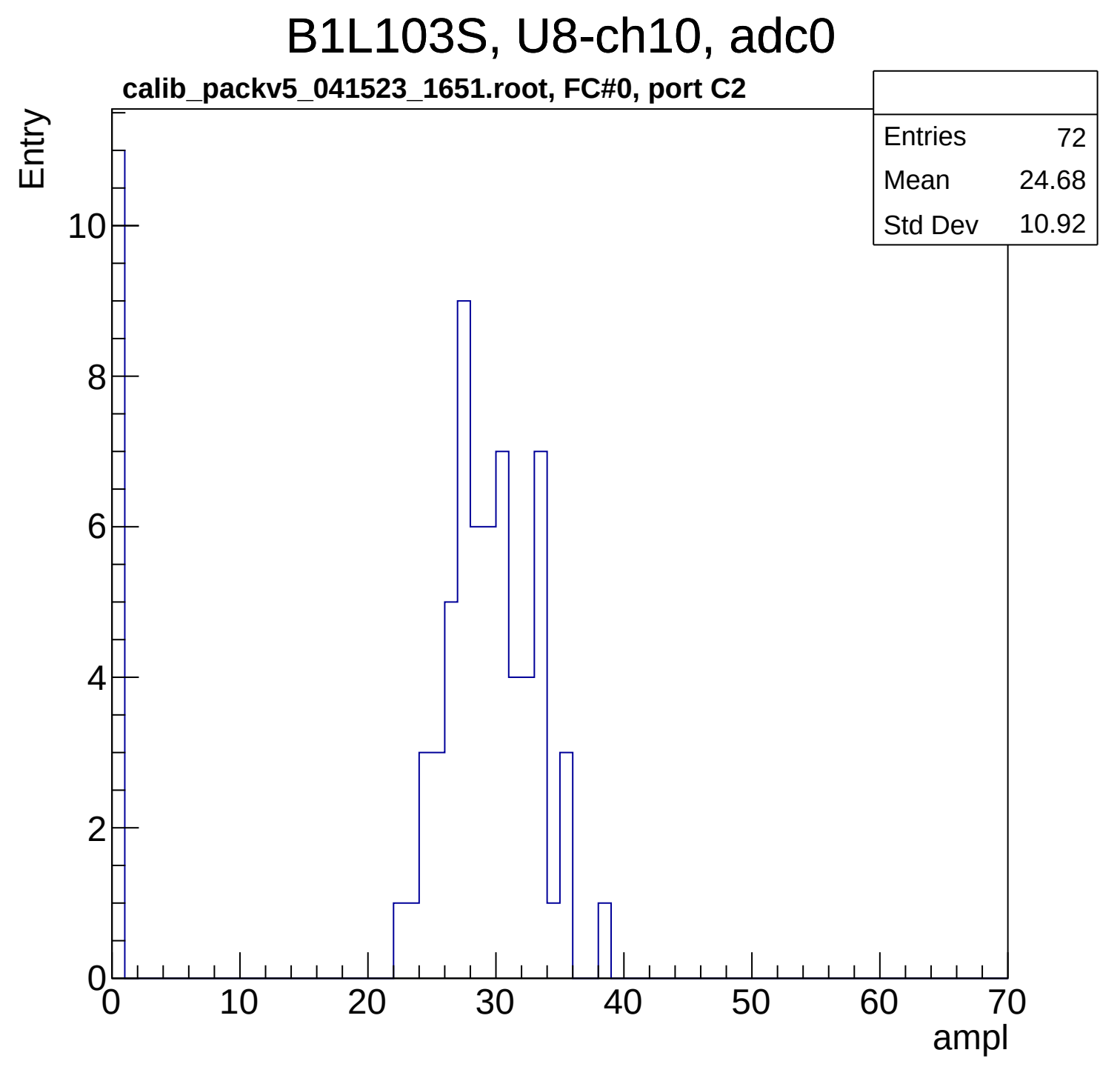
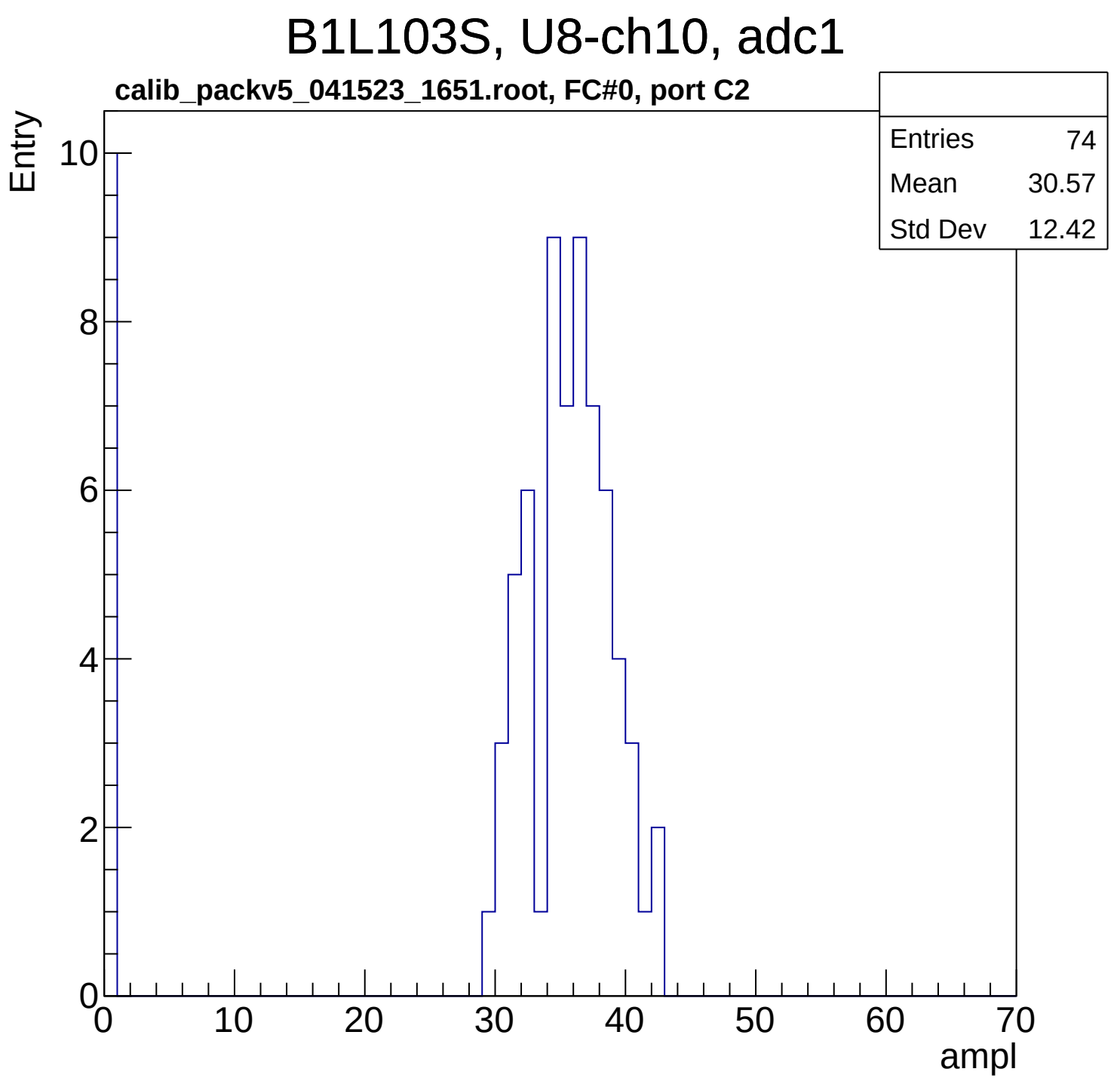
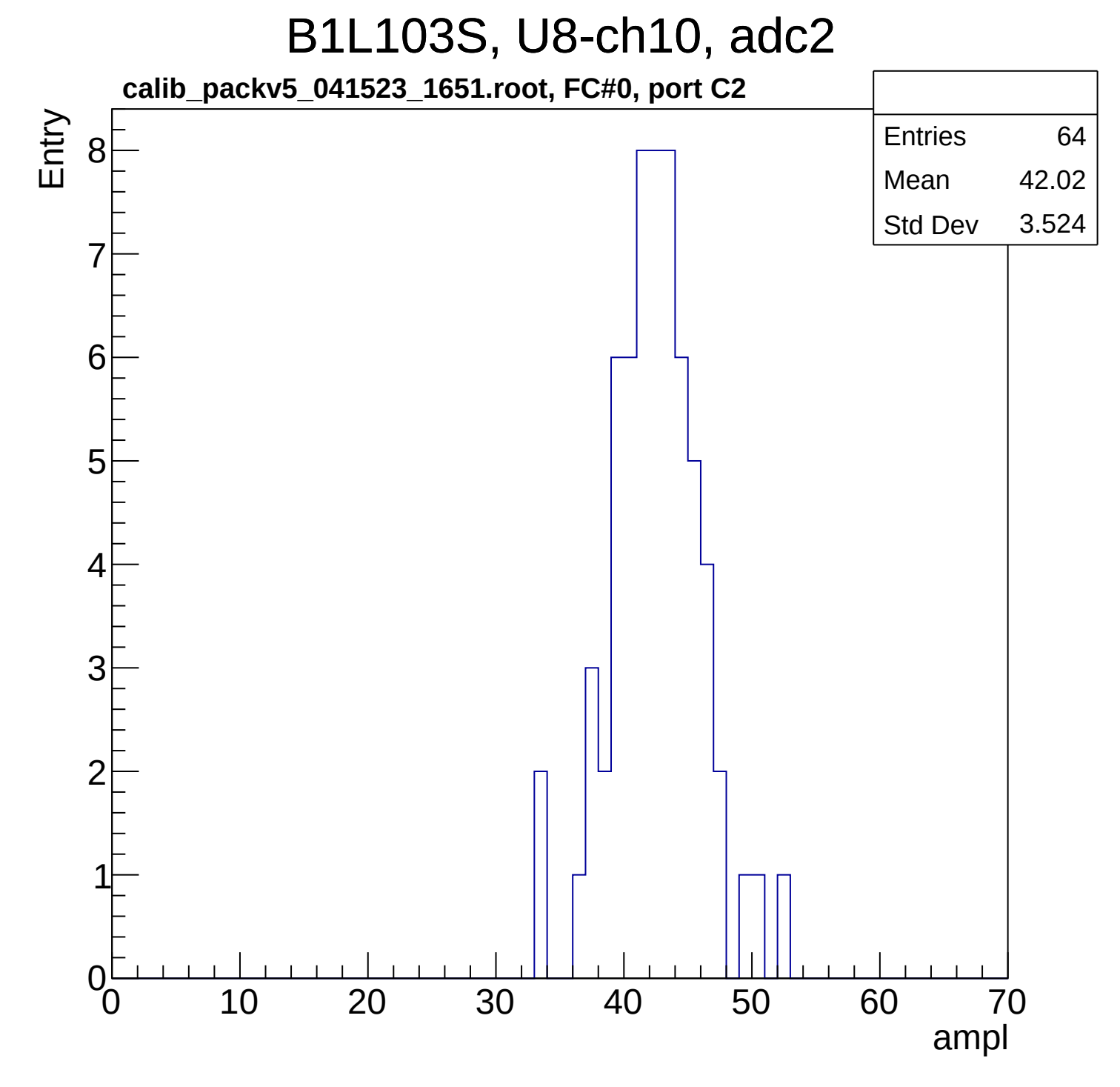
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch9, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 62
Std Dev 1.225
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U8-ch9, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch10, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 24.68
Std Dev 10.92
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch10, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 30.57
Std Dev 12.42
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U8-ch10, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 42.02
Std Dev 3.524
Entry
ampl
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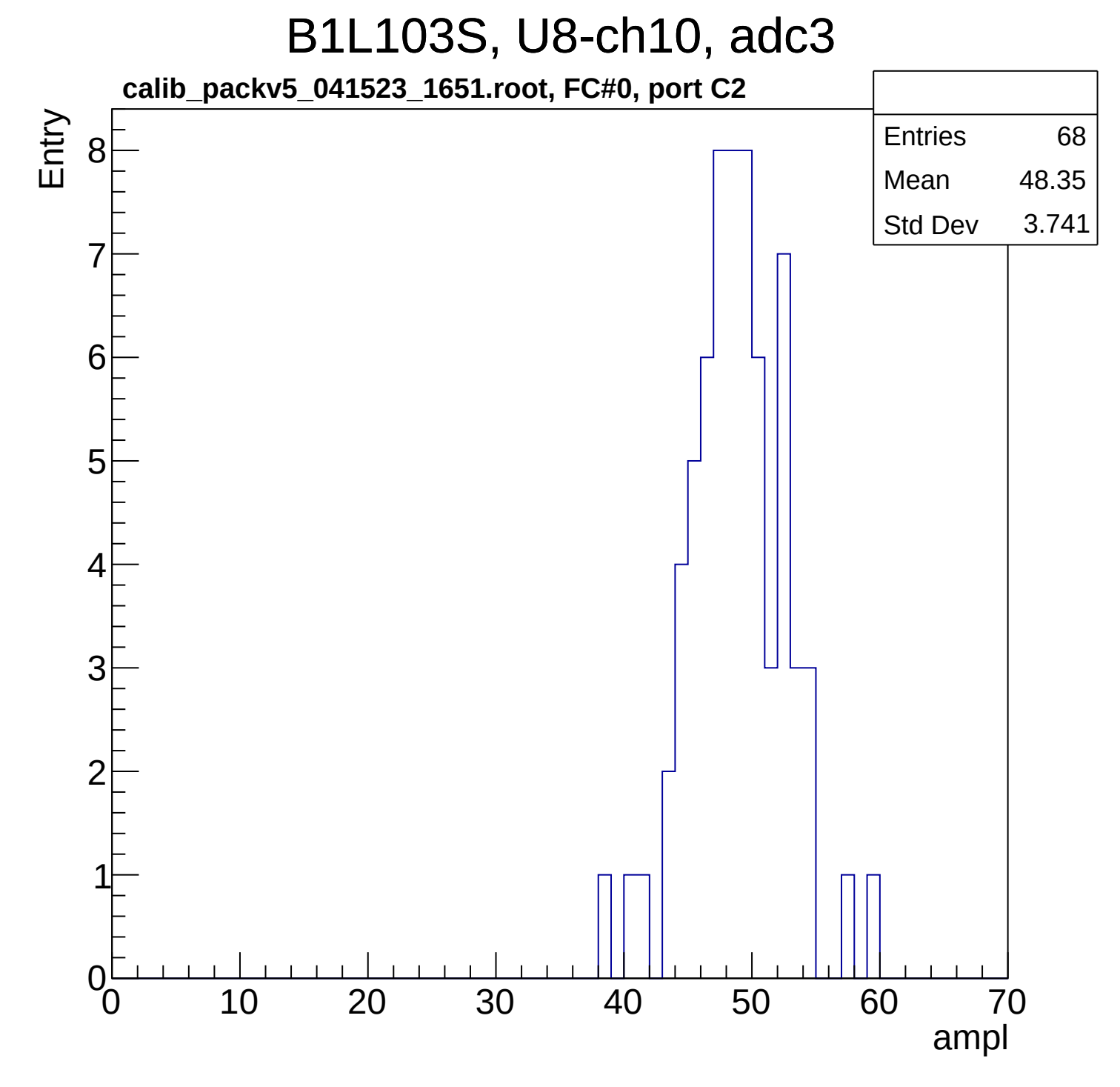
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch10, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 48.35
Std Dev 3.741
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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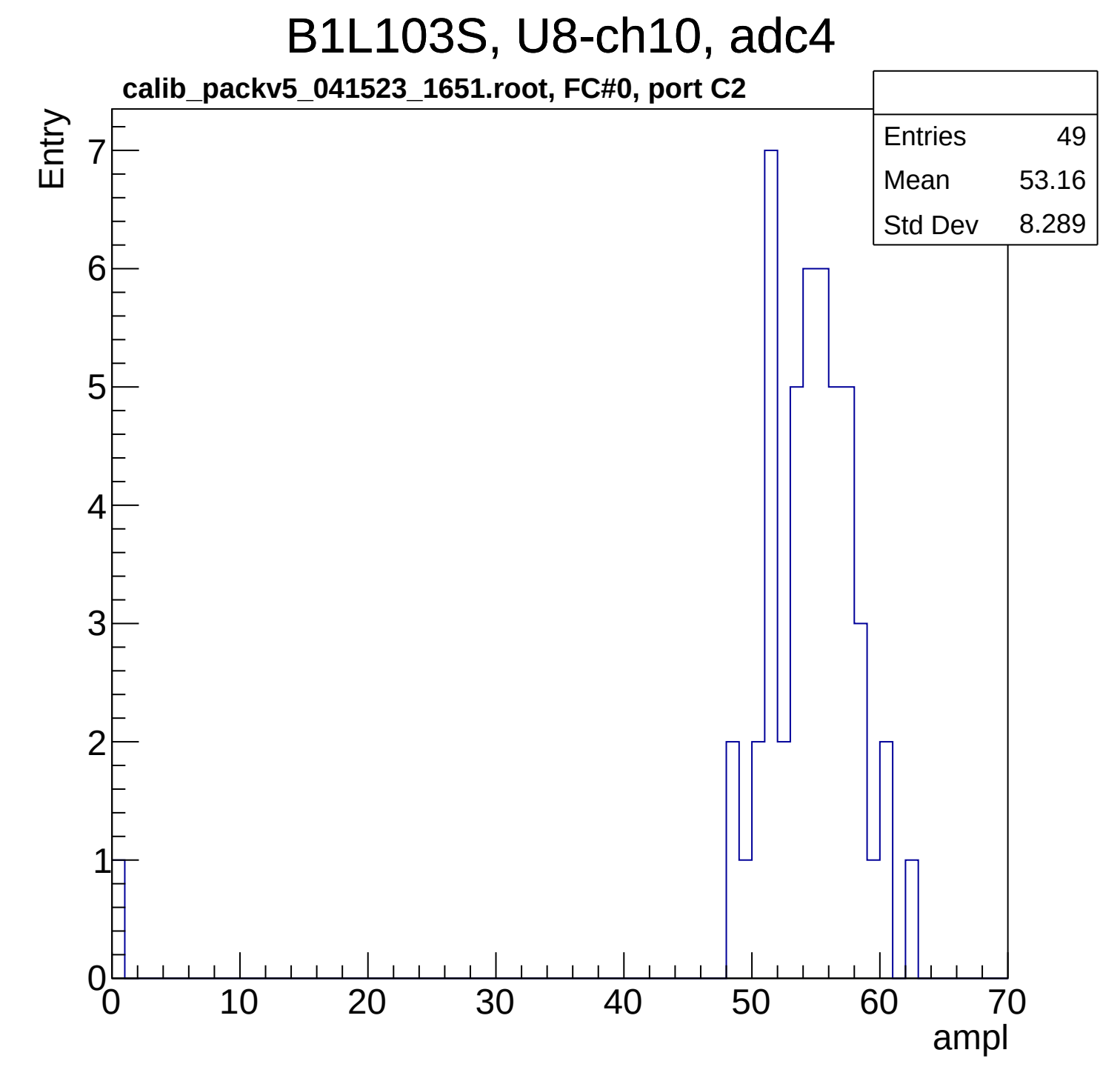
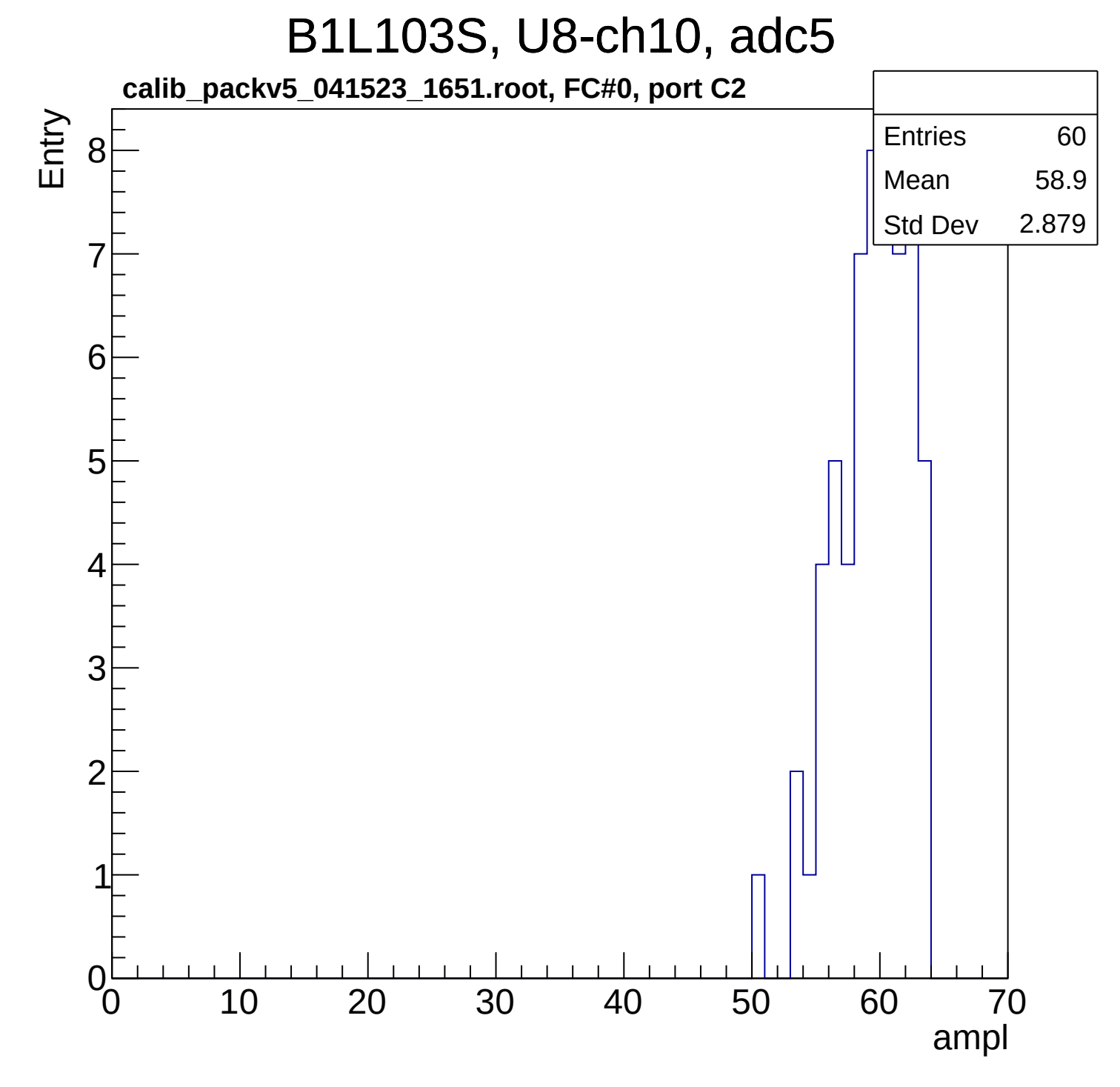
40
50
60
70


B1L103S, U8-ch10, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 53.16
Std Dev 8.289
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U8-ch10, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 58.9
Std Dev 2.879
Entry
ampl
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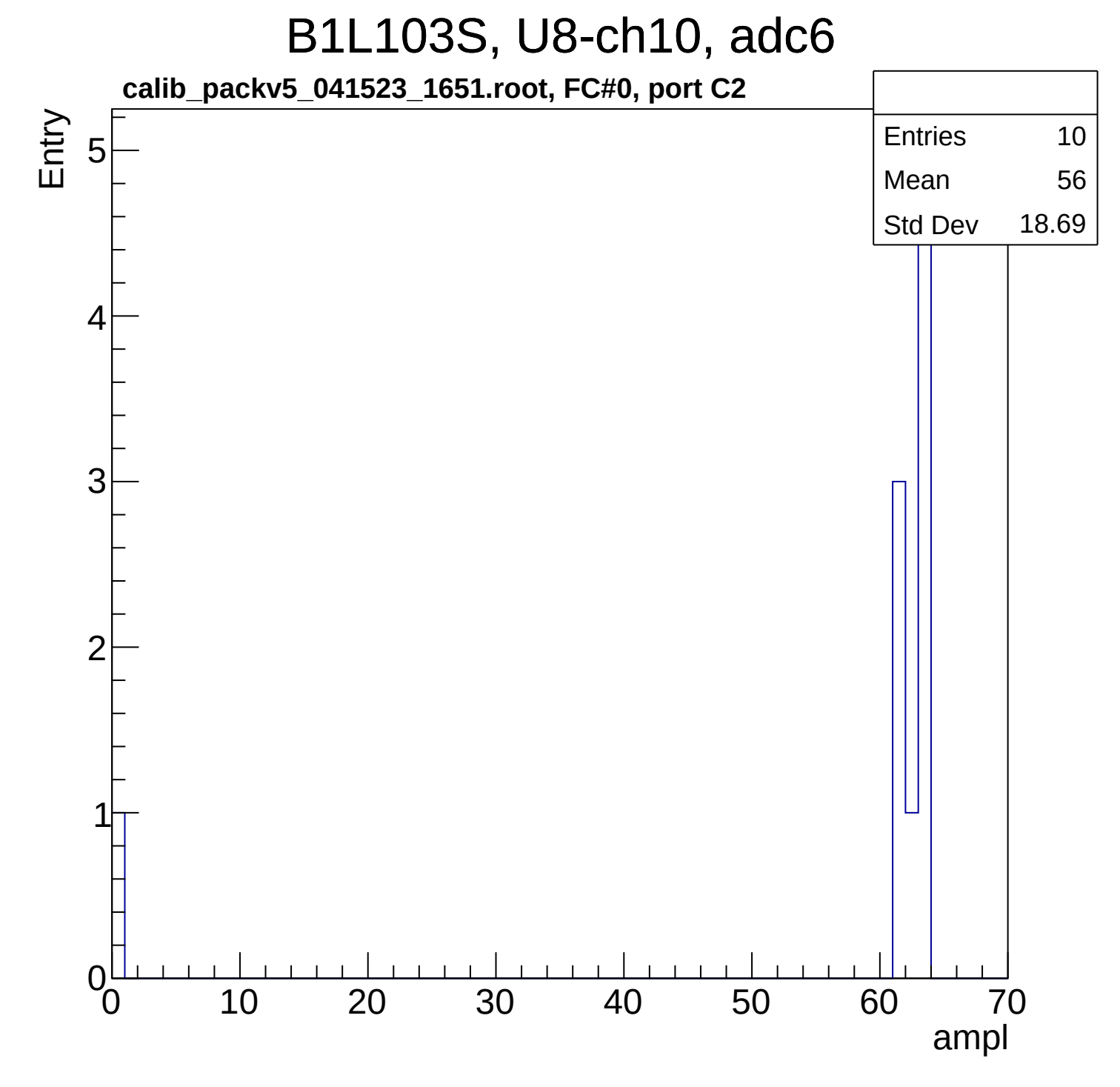
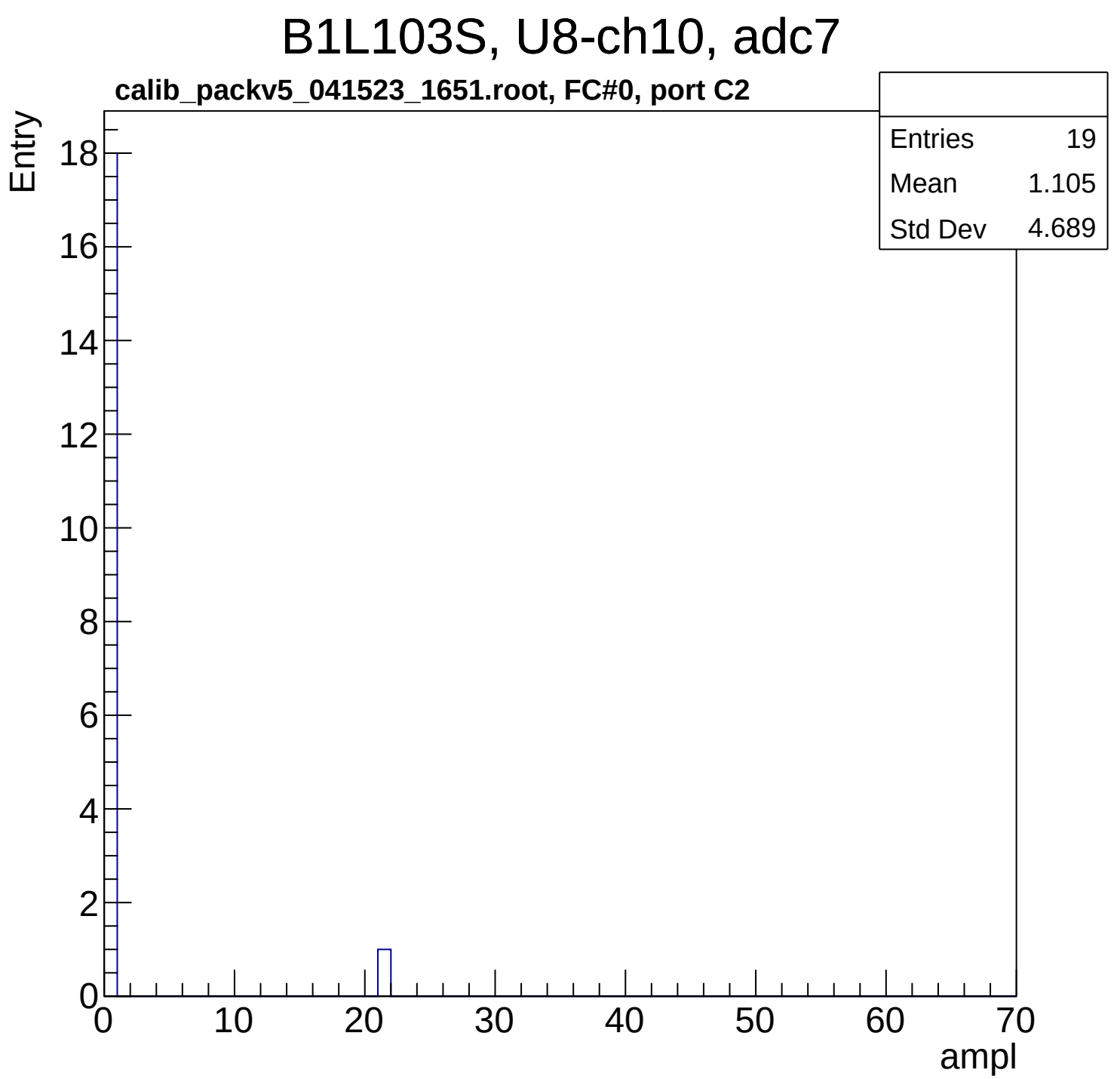
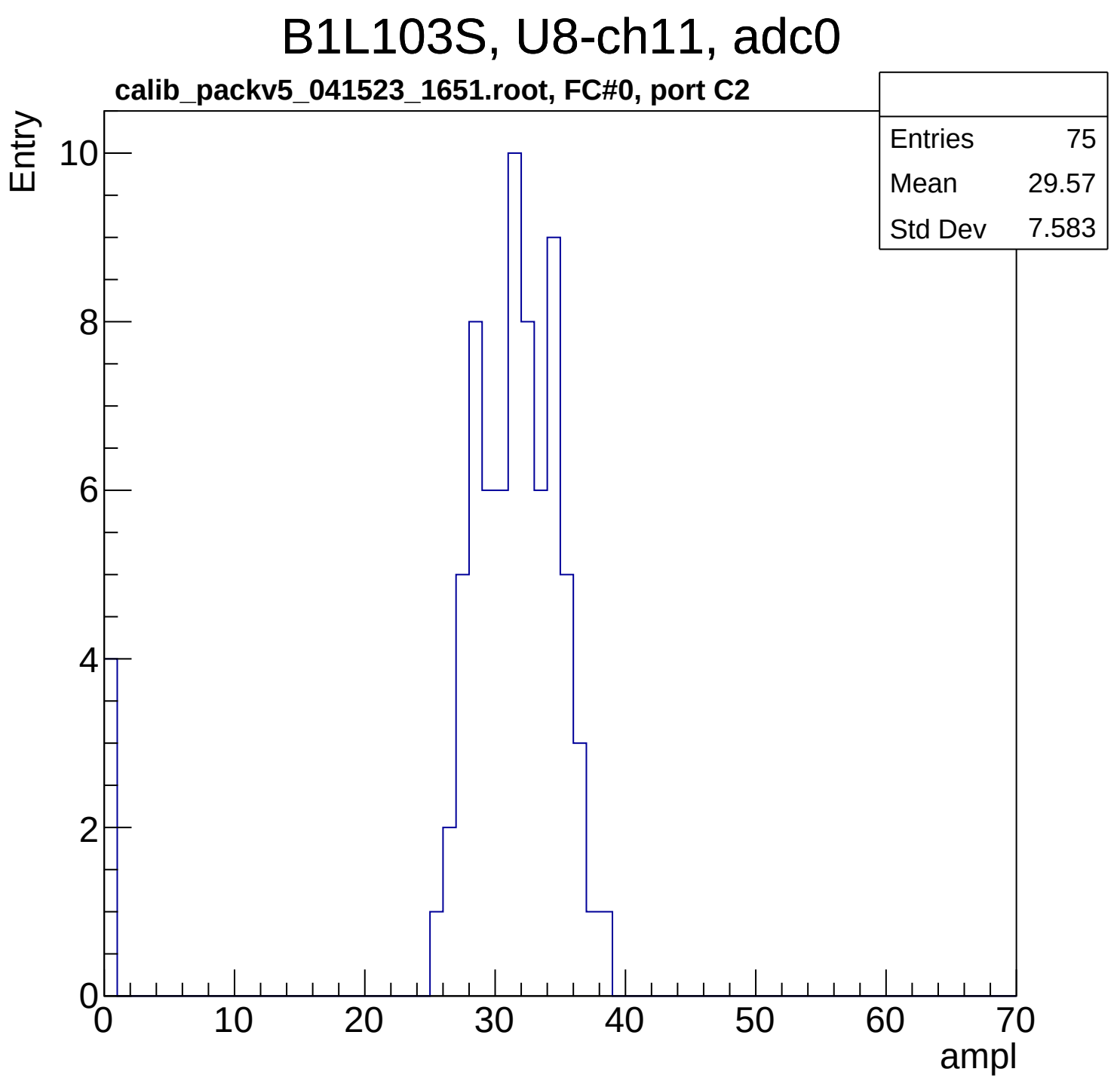
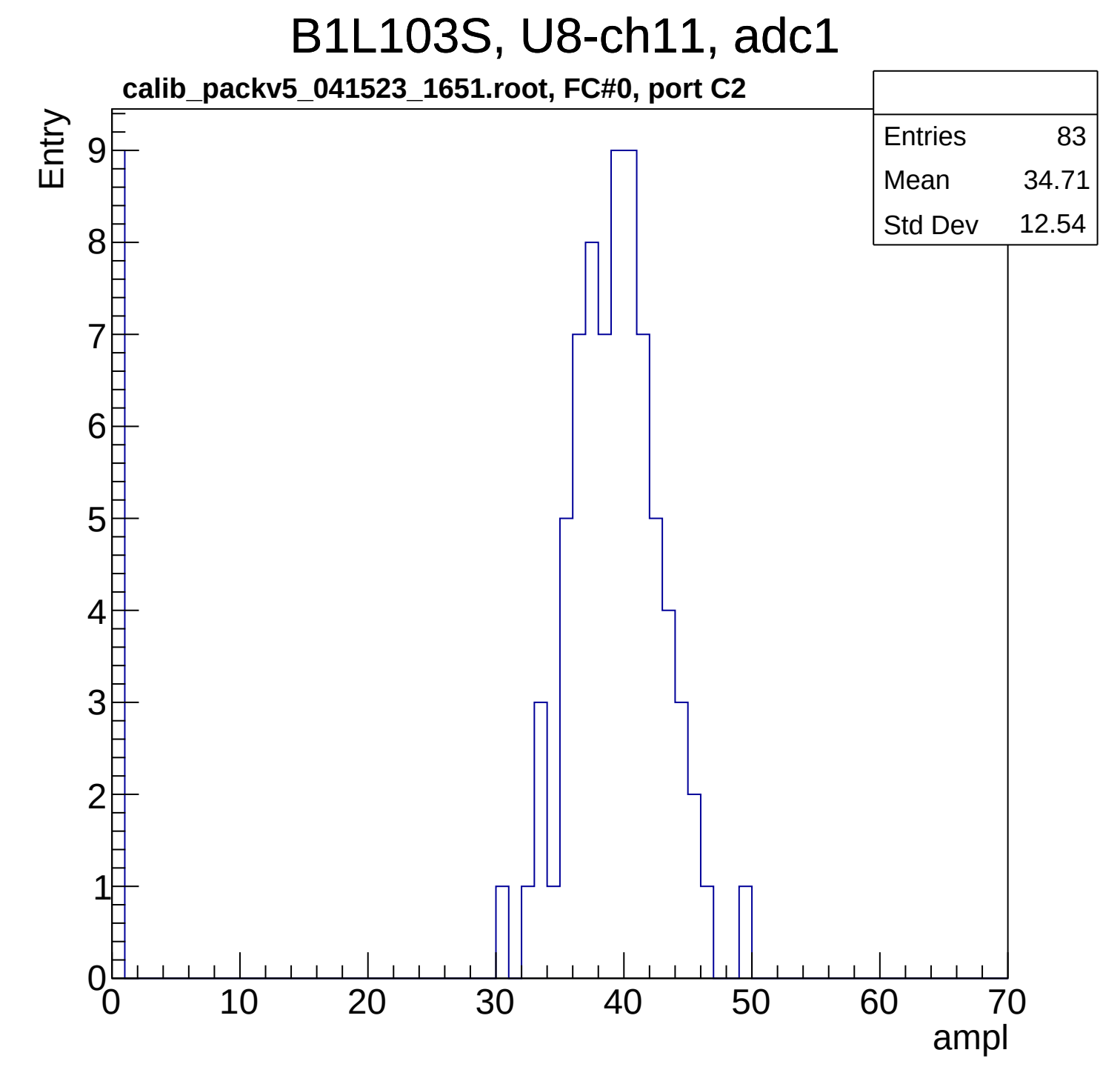
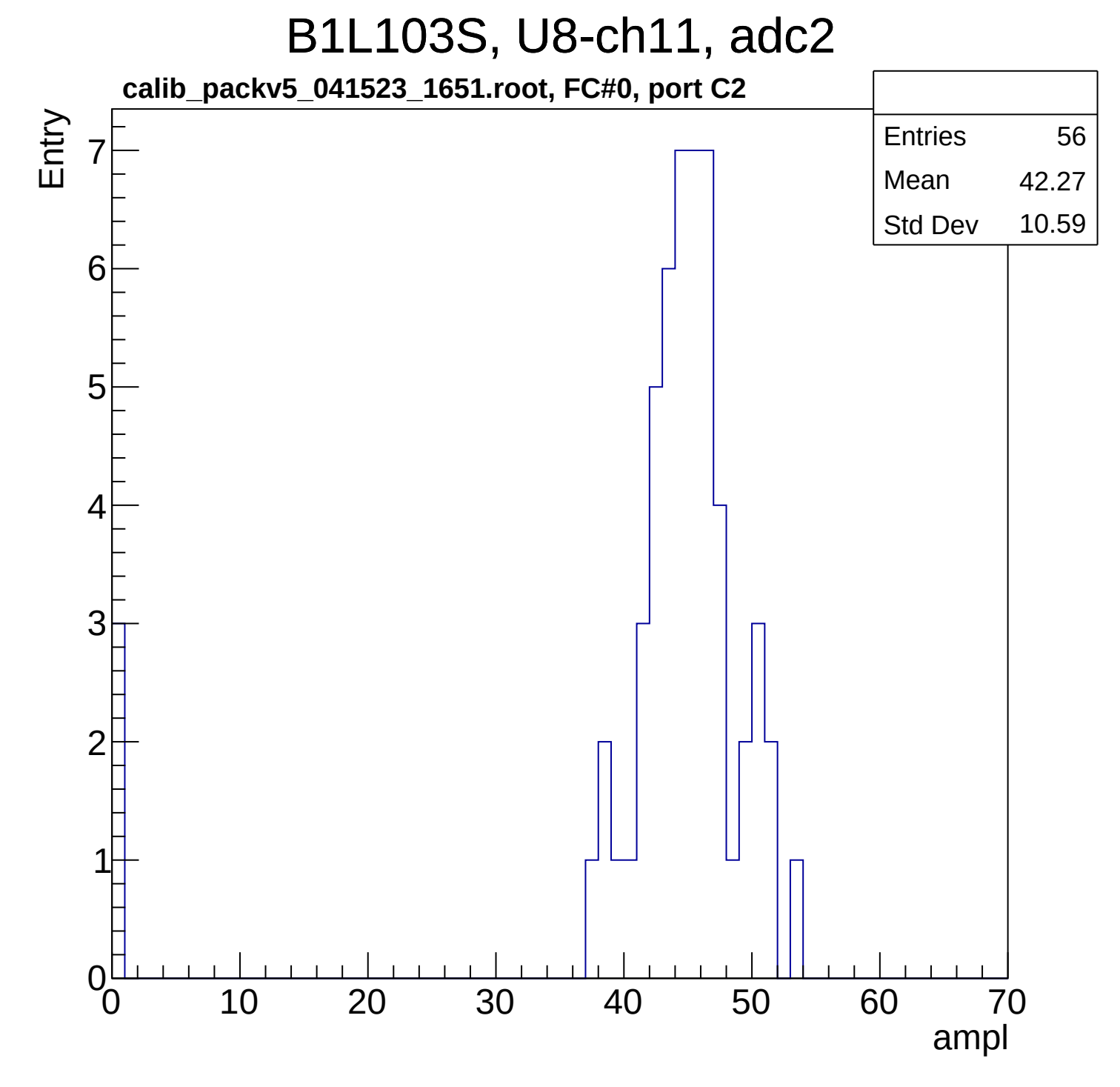
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

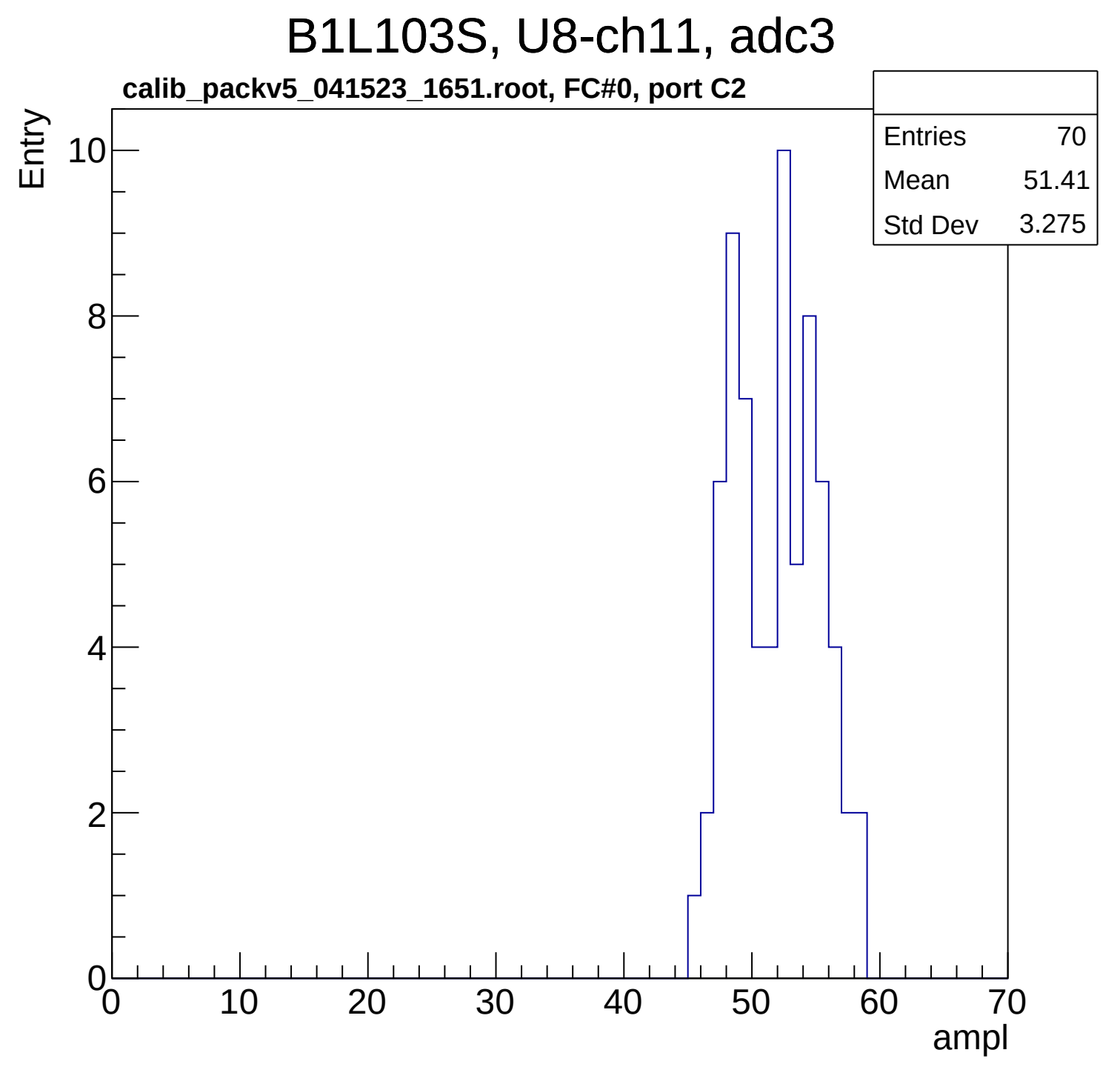

B1L103S, U8-ch10, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 56
Std Dev 18.69
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

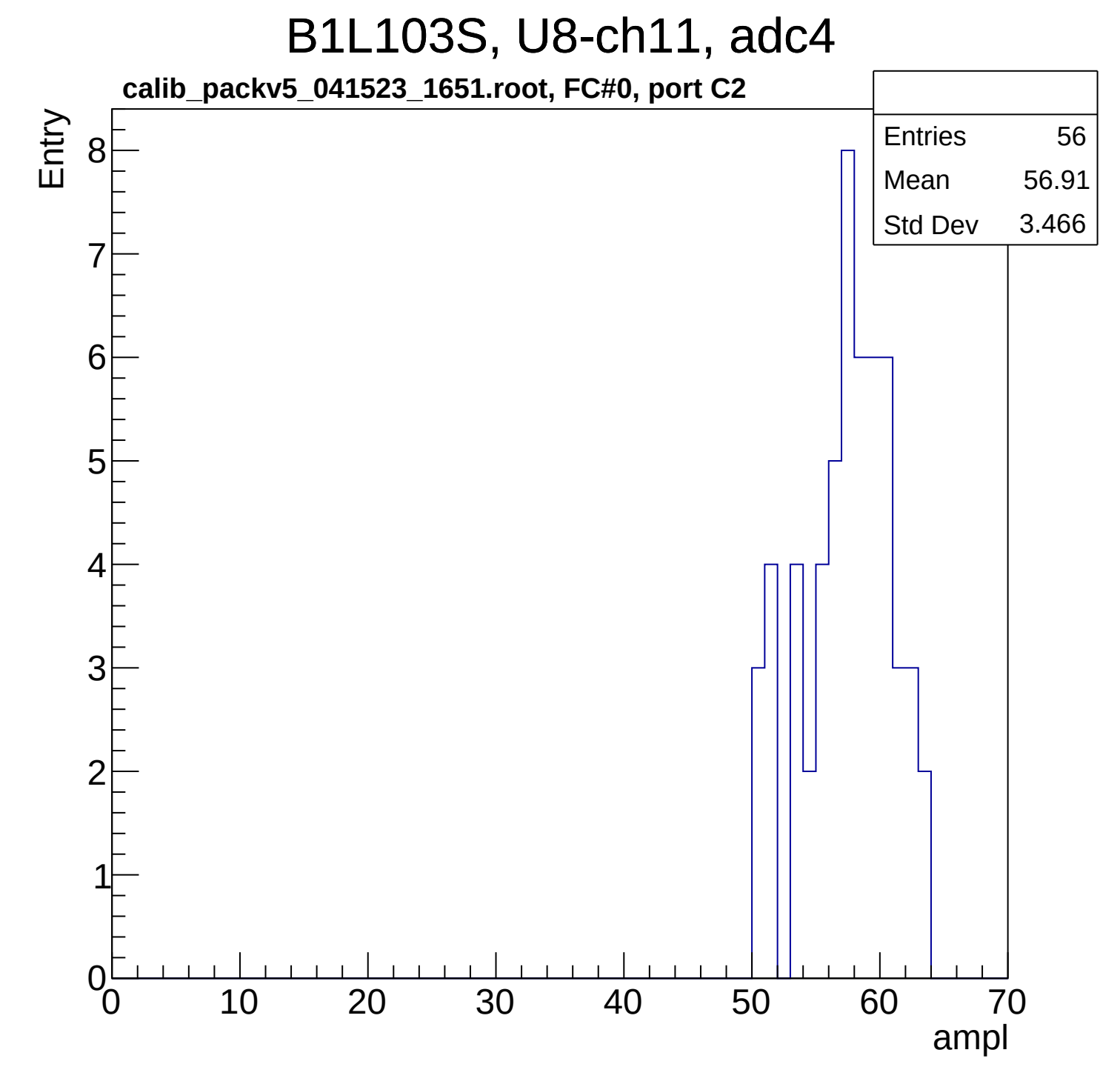

B1L103S, U8-ch10, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.105
Std Dev 4.689
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

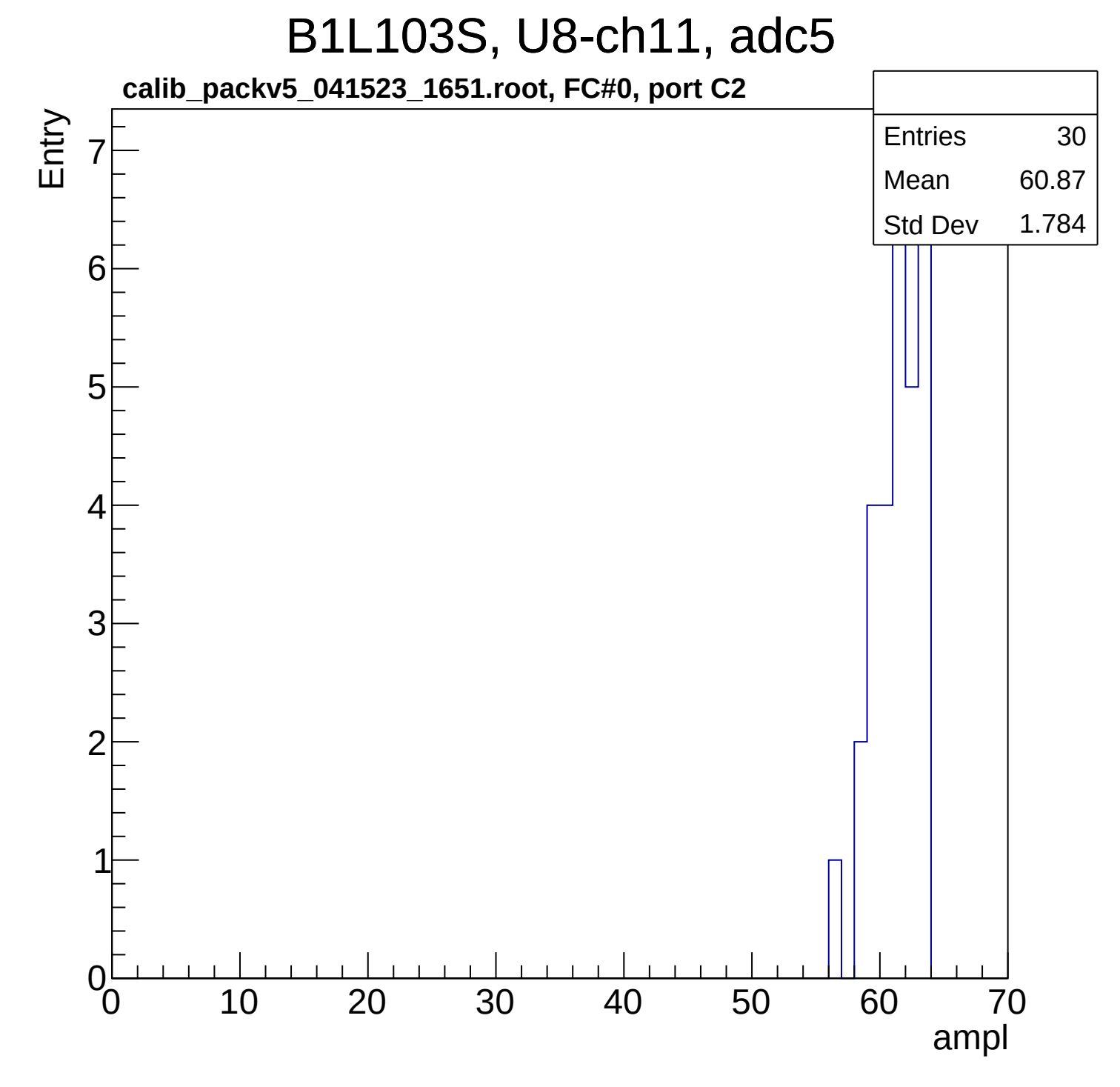

B1L103S, U8-ch11, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 29.57
Std Dev 7.583
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

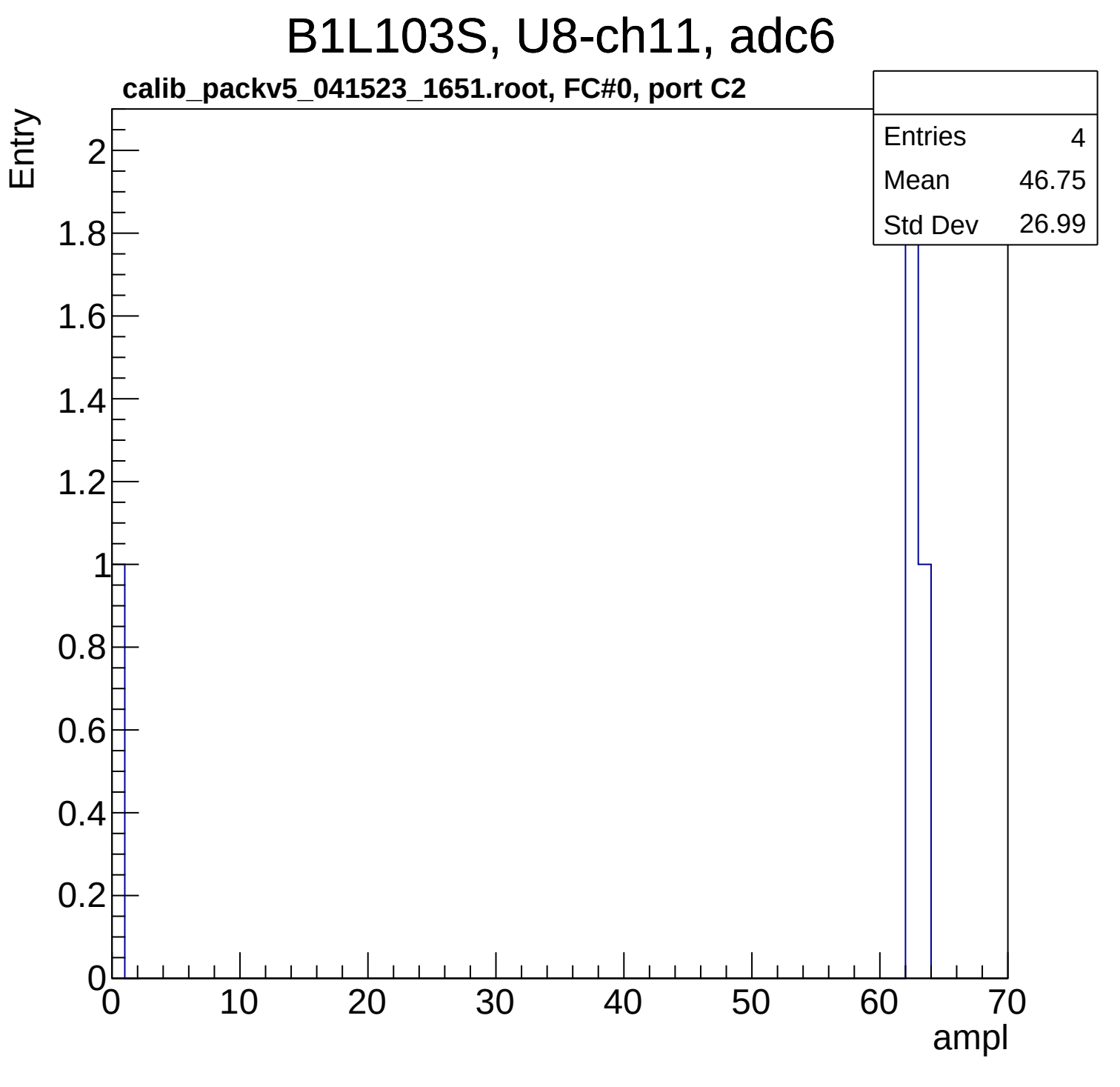

B1L103S, U8-ch11, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 34.71
Std Dev 12.54
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

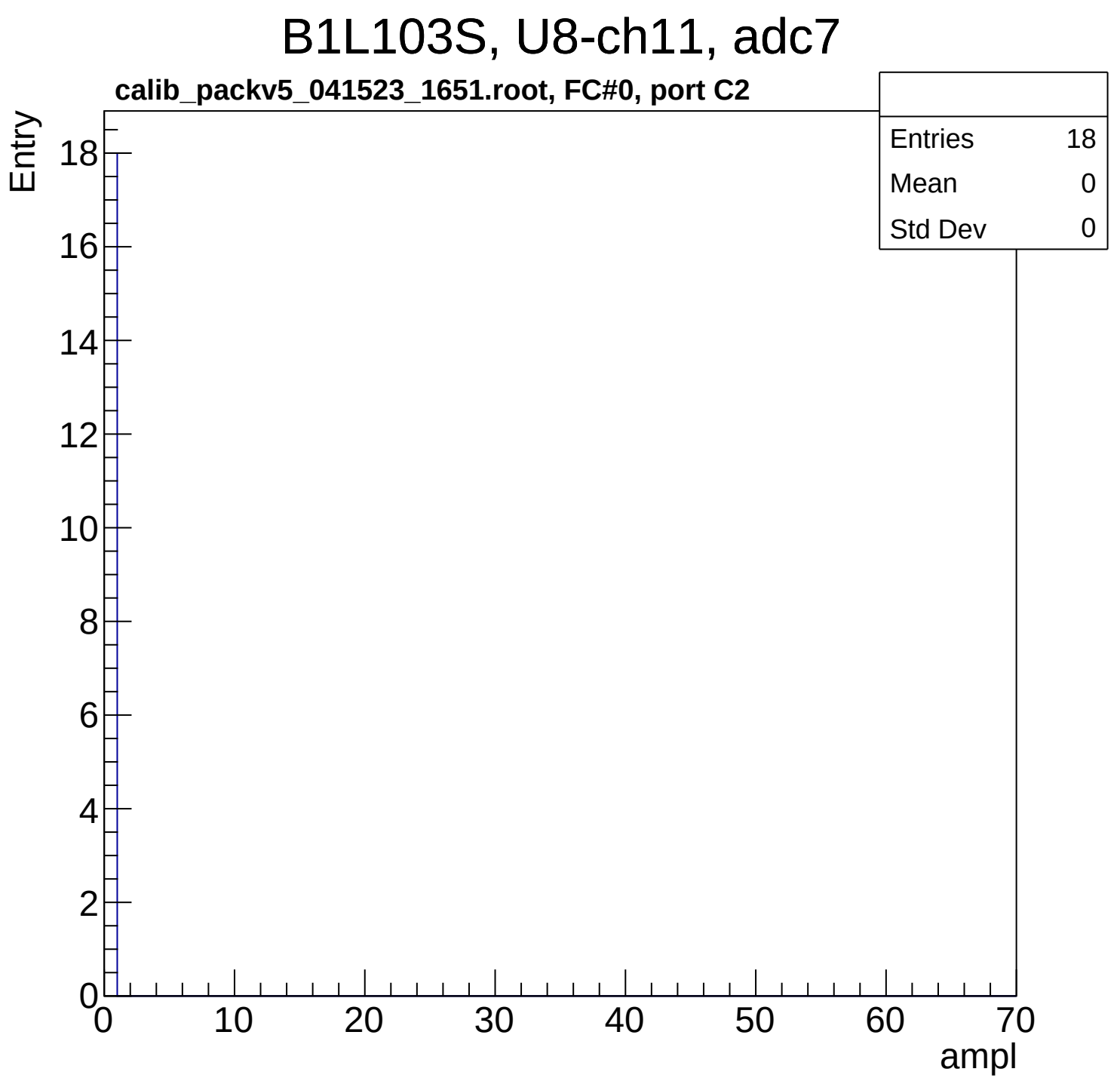

B1L103S, U8-ch11, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 42.27
Std Dev 10.59
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

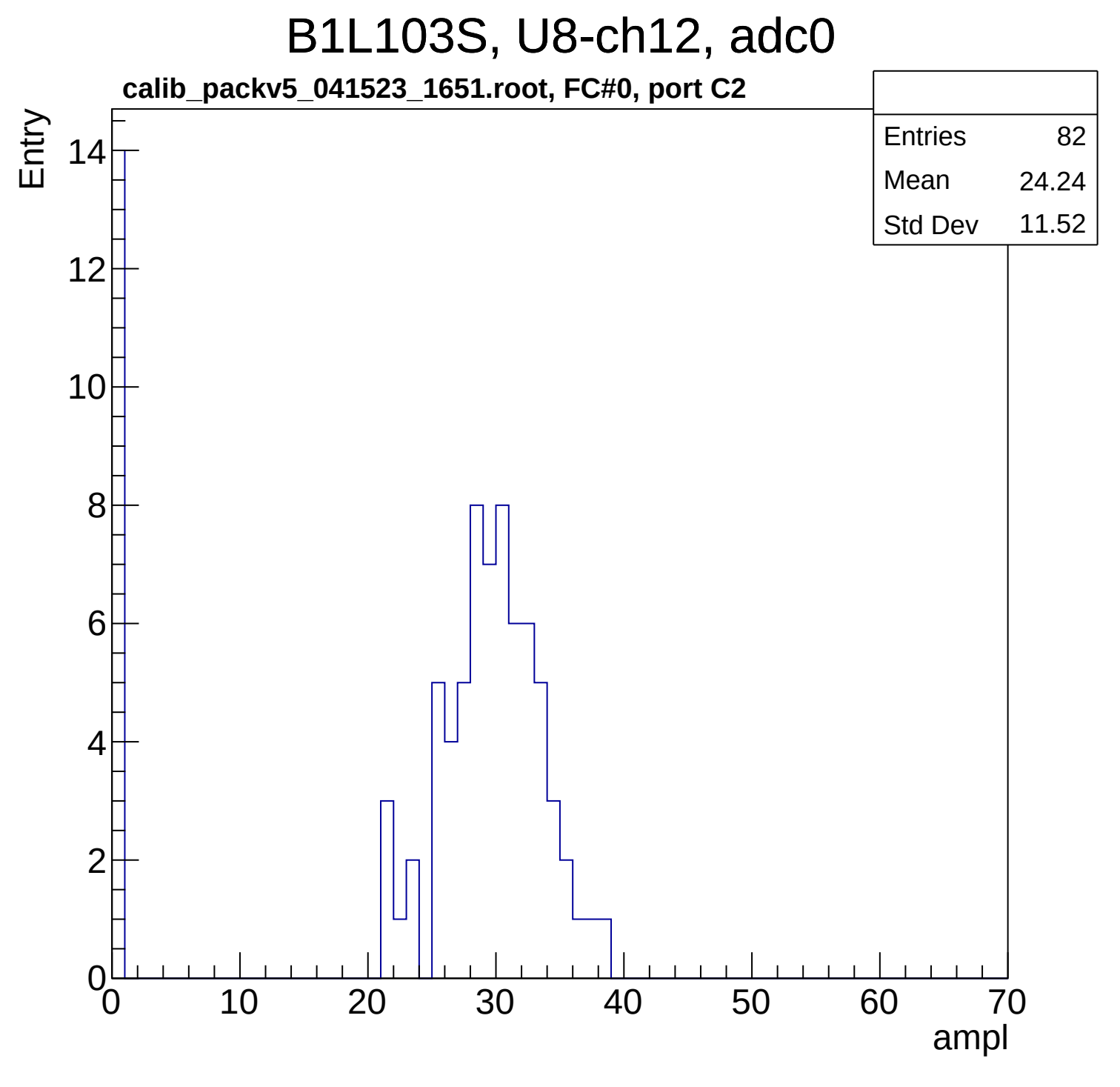

B1L103S, U8-ch11, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 51.41
Std Dev 3.275
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U8-ch11, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 56.91
Std Dev 3.466
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch11, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 60.87
Std Dev 1.784
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U8-ch11, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 46.75
Std Dev 26.99
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U8-ch11, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch12, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 24.24
Std Dev 11.52
Entry
0
2
4
6
8
10
12
14
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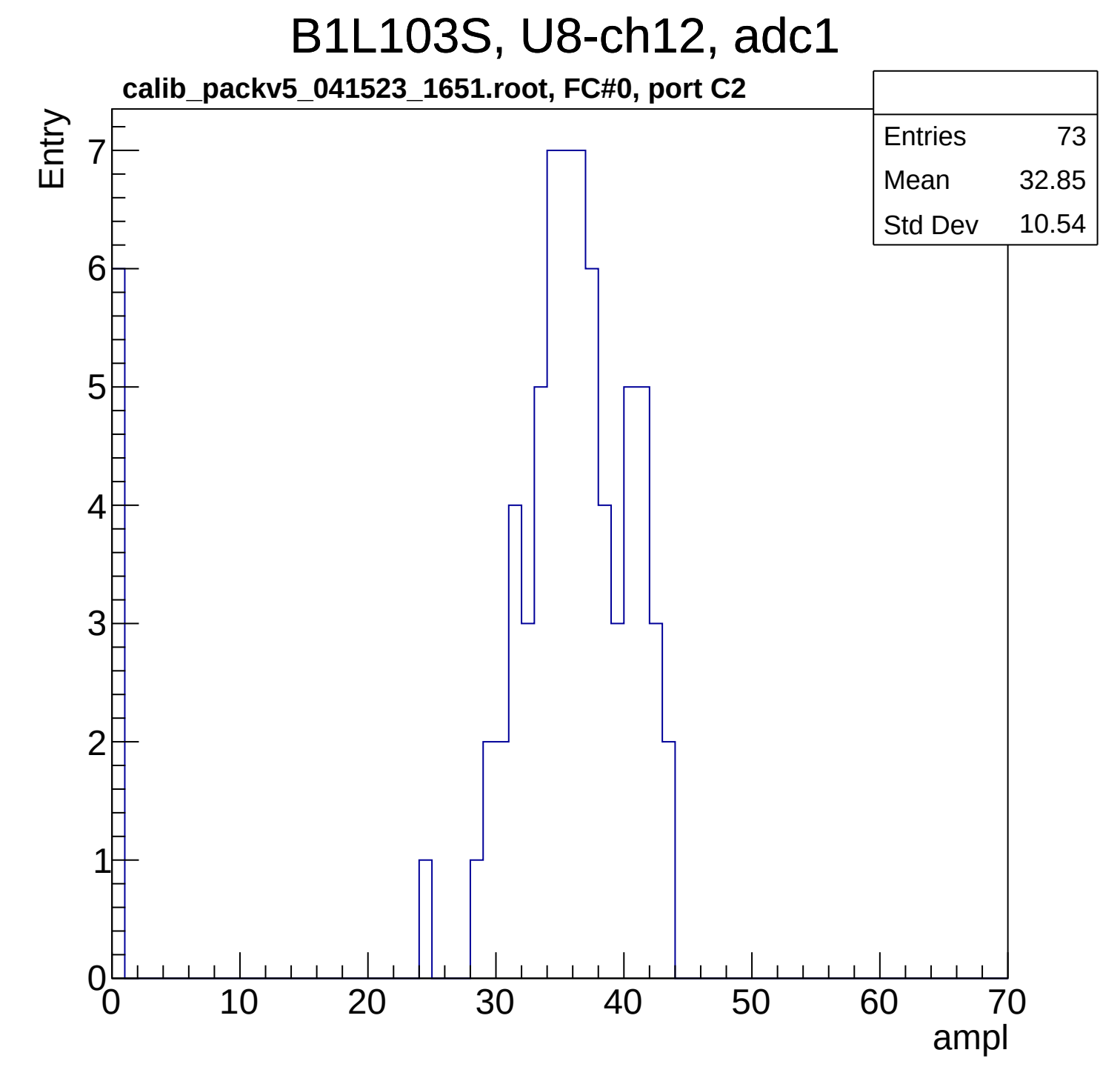
70
ampl


B1L103S, U8-ch12, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 32.85
Std Dev 10.54
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
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60
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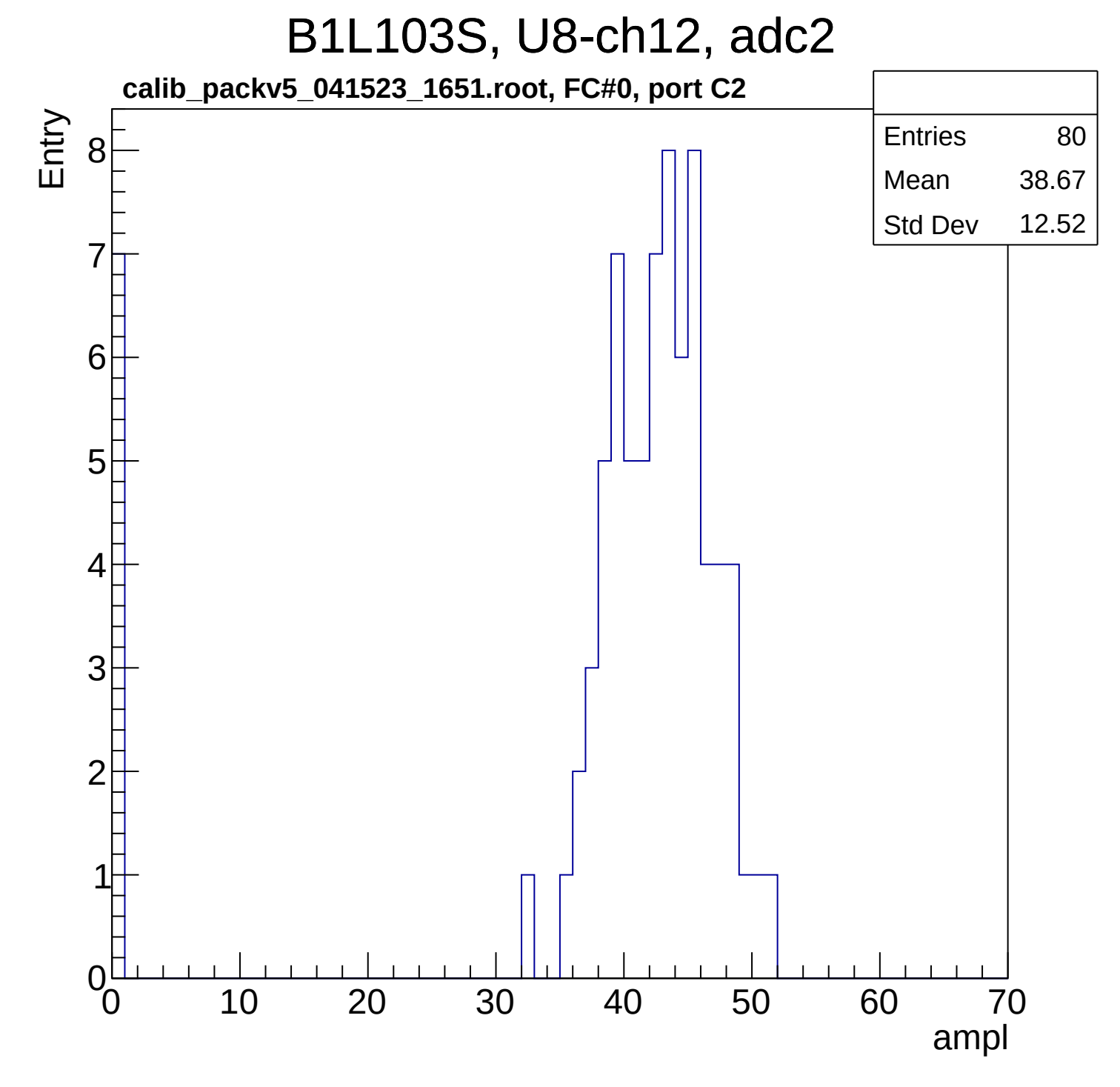
B1L103S, U8-ch12, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 38.67
Std Dev 12.52
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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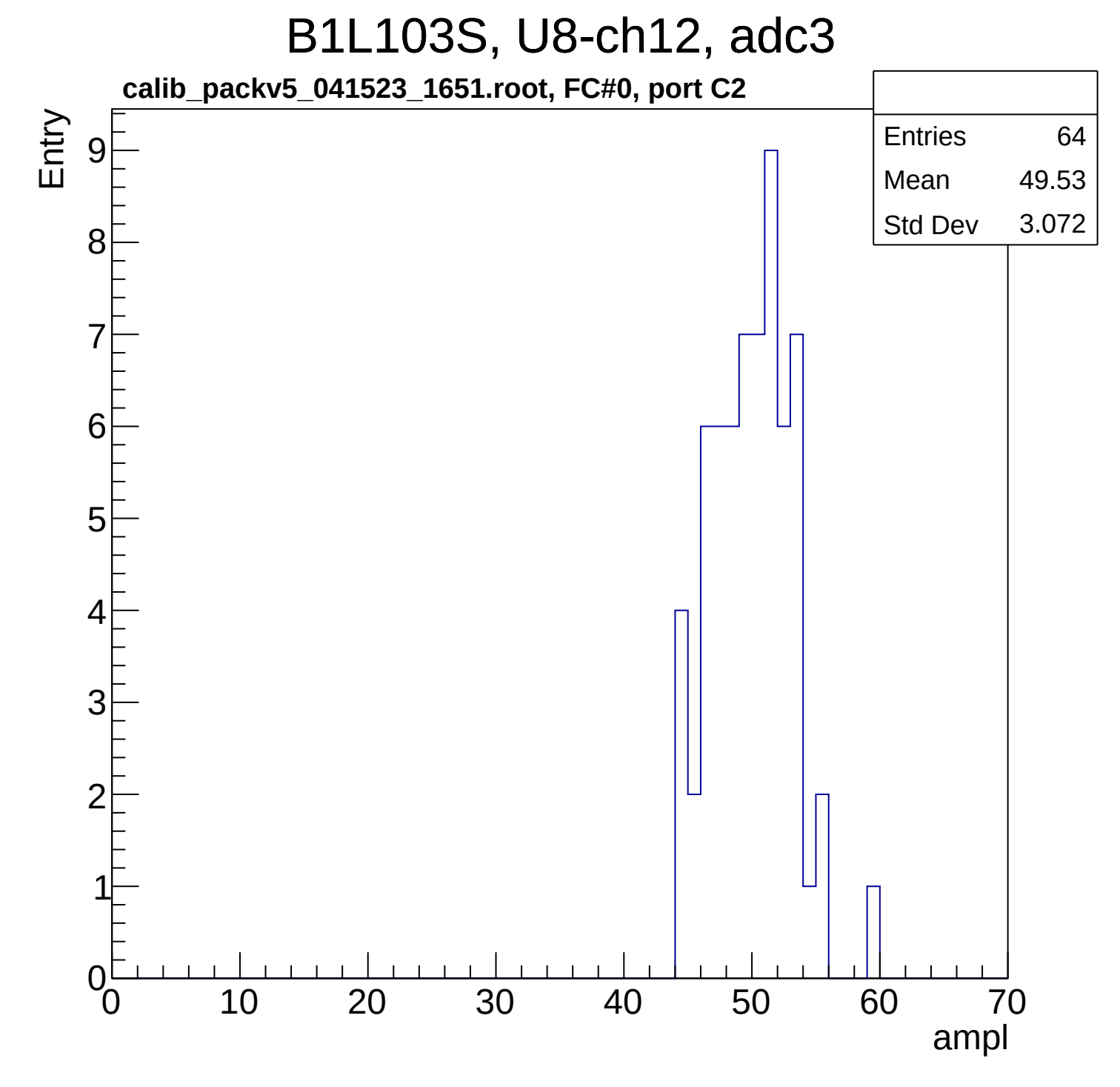
B1L103S, U8-ch12, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 49.53
Std Dev 3.072
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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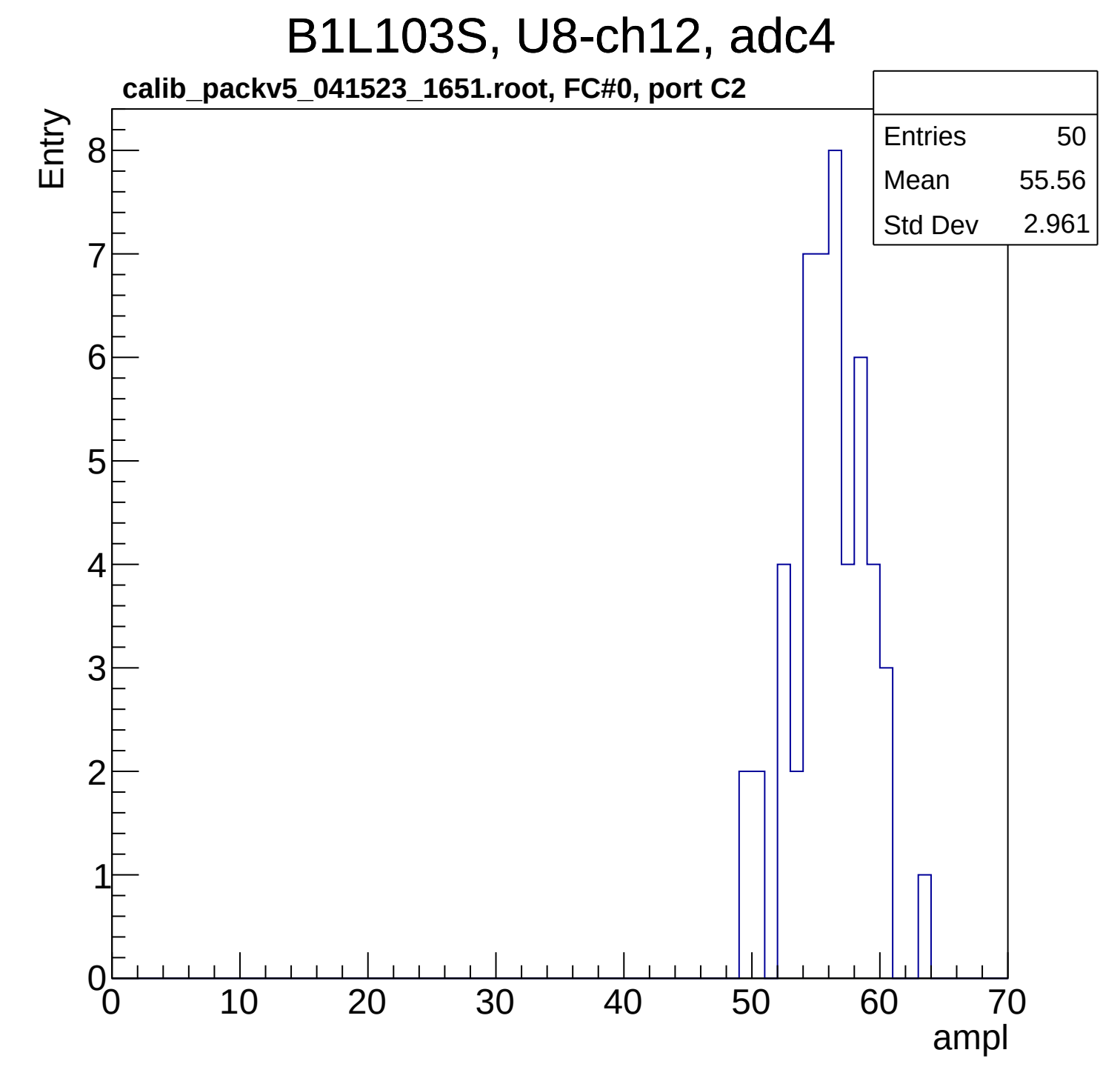
B1L103S, U8-ch12, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 55.56
Std Dev 2.961
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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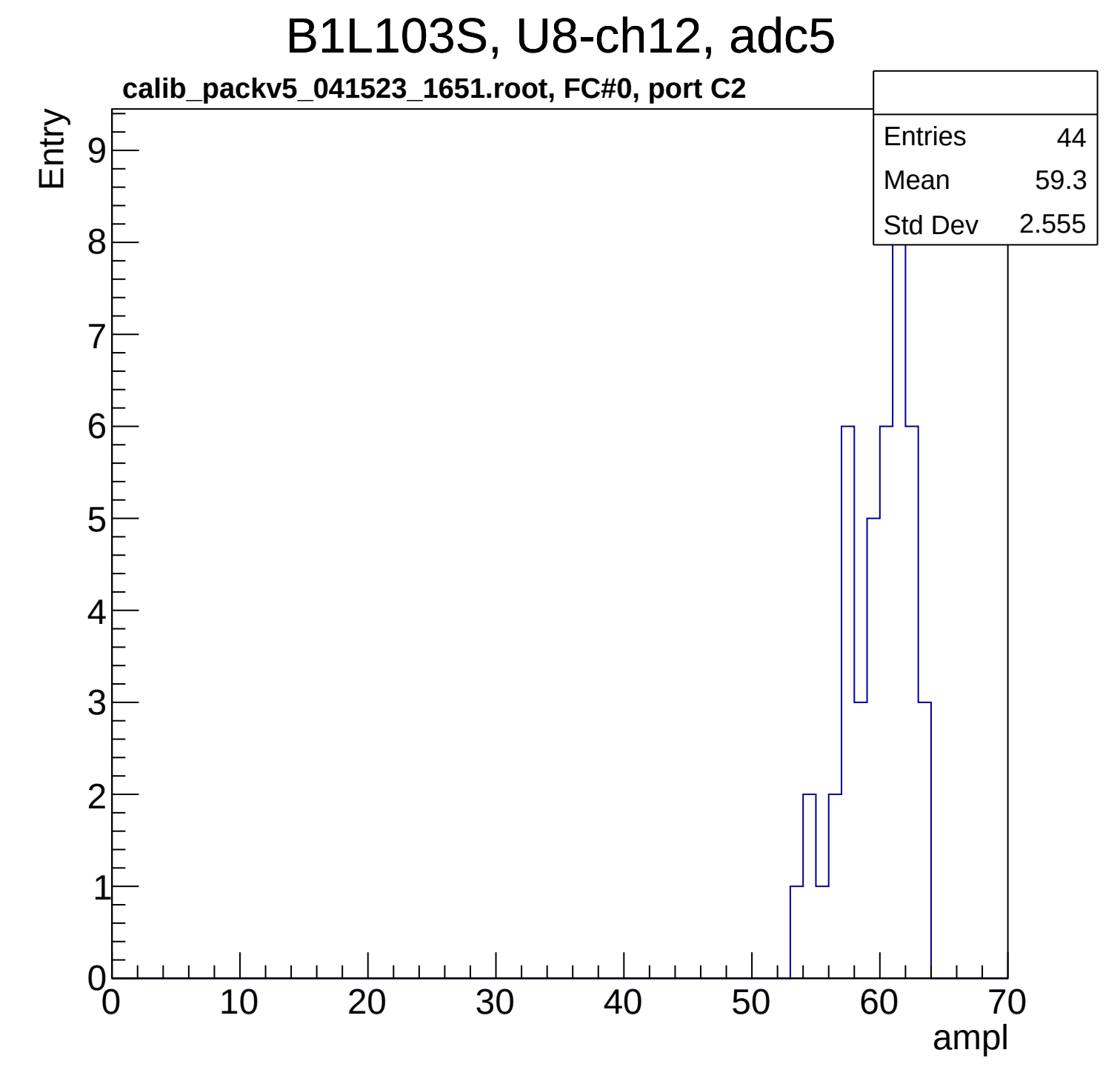
B1L103S, U8-ch12, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 59.3
Std Dev 2.555
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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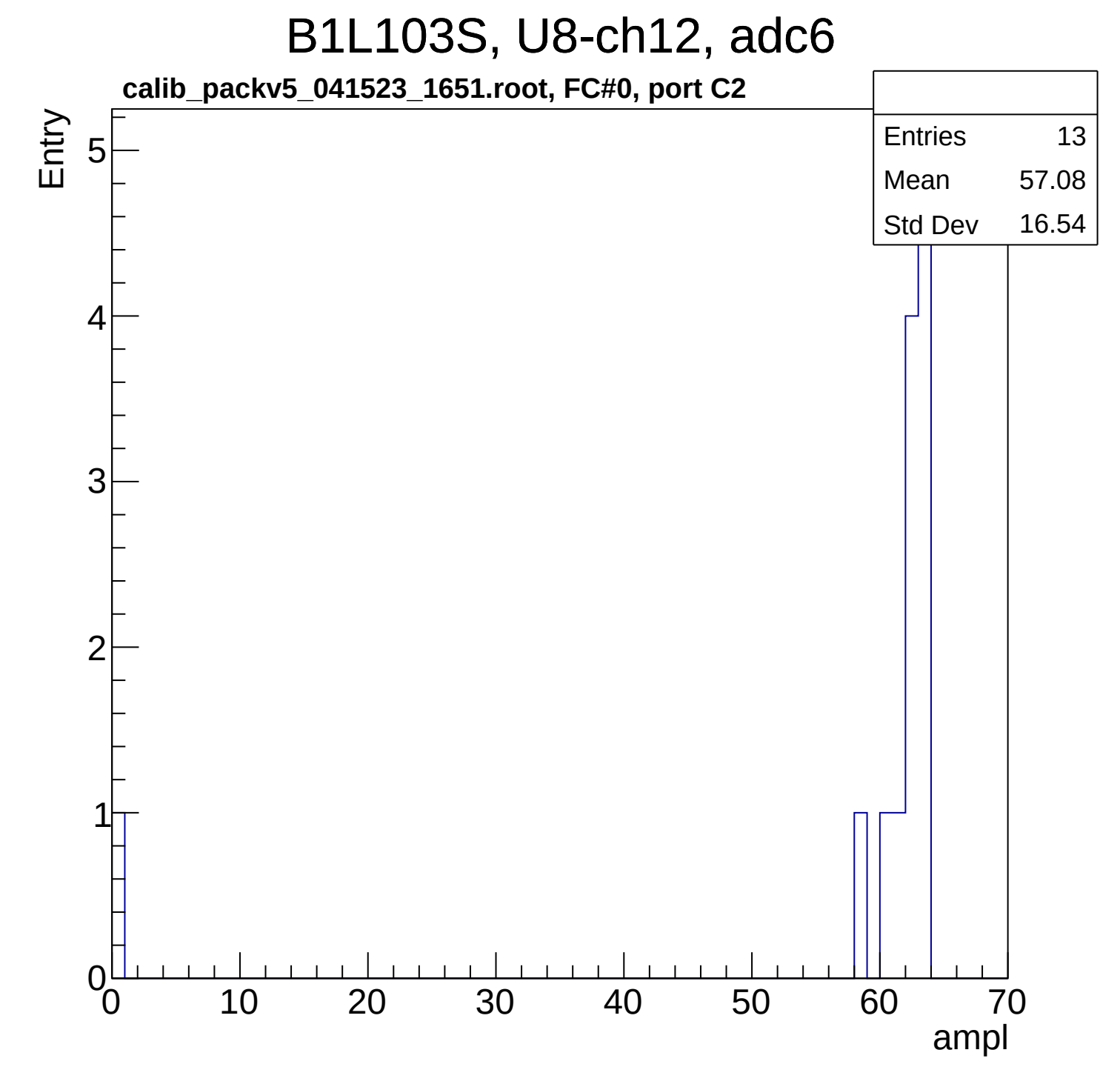
B1L103S, U8-ch12, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 57.08
Std Dev 16.54
Entry
ampl
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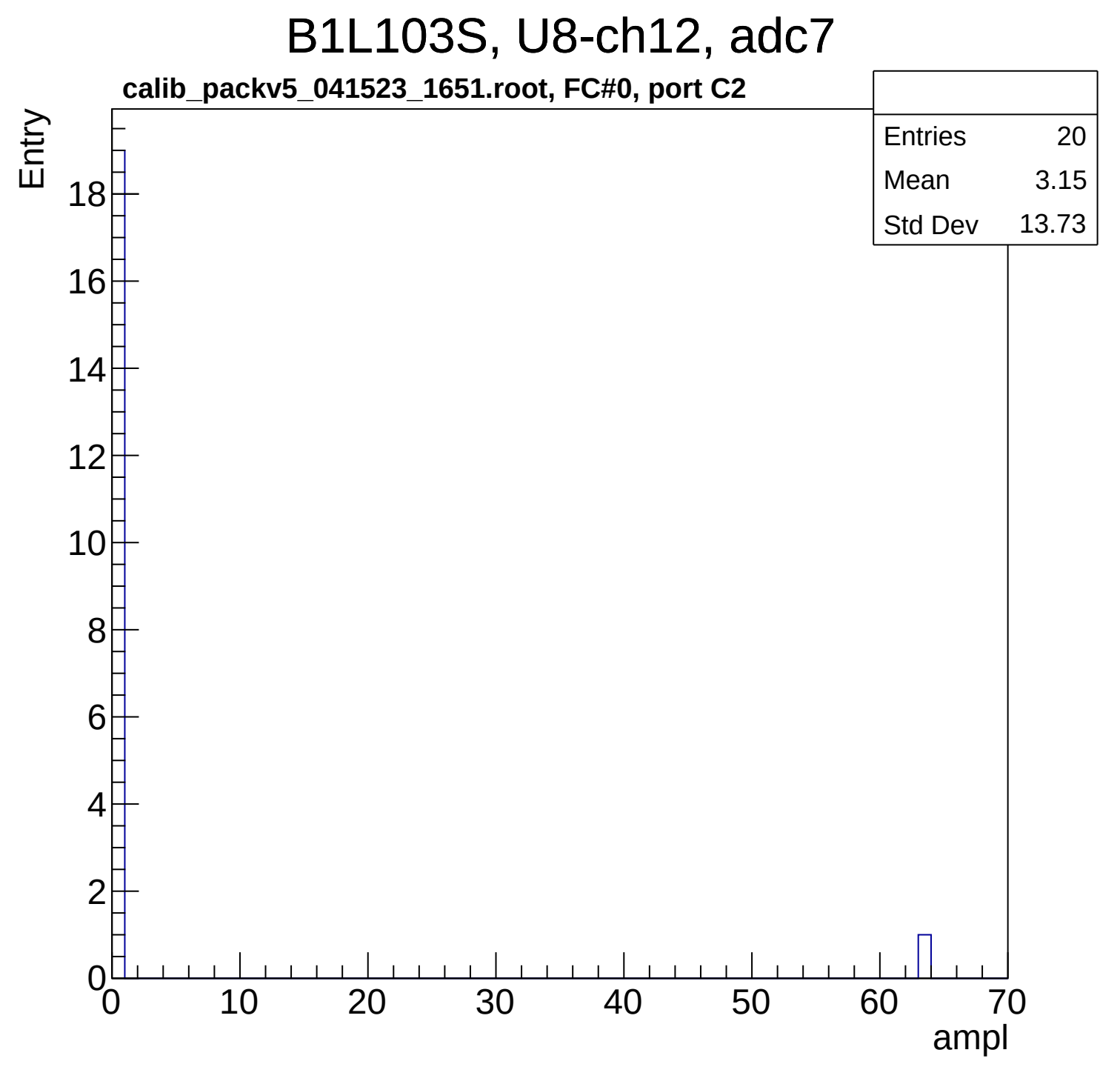
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U8-ch12, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
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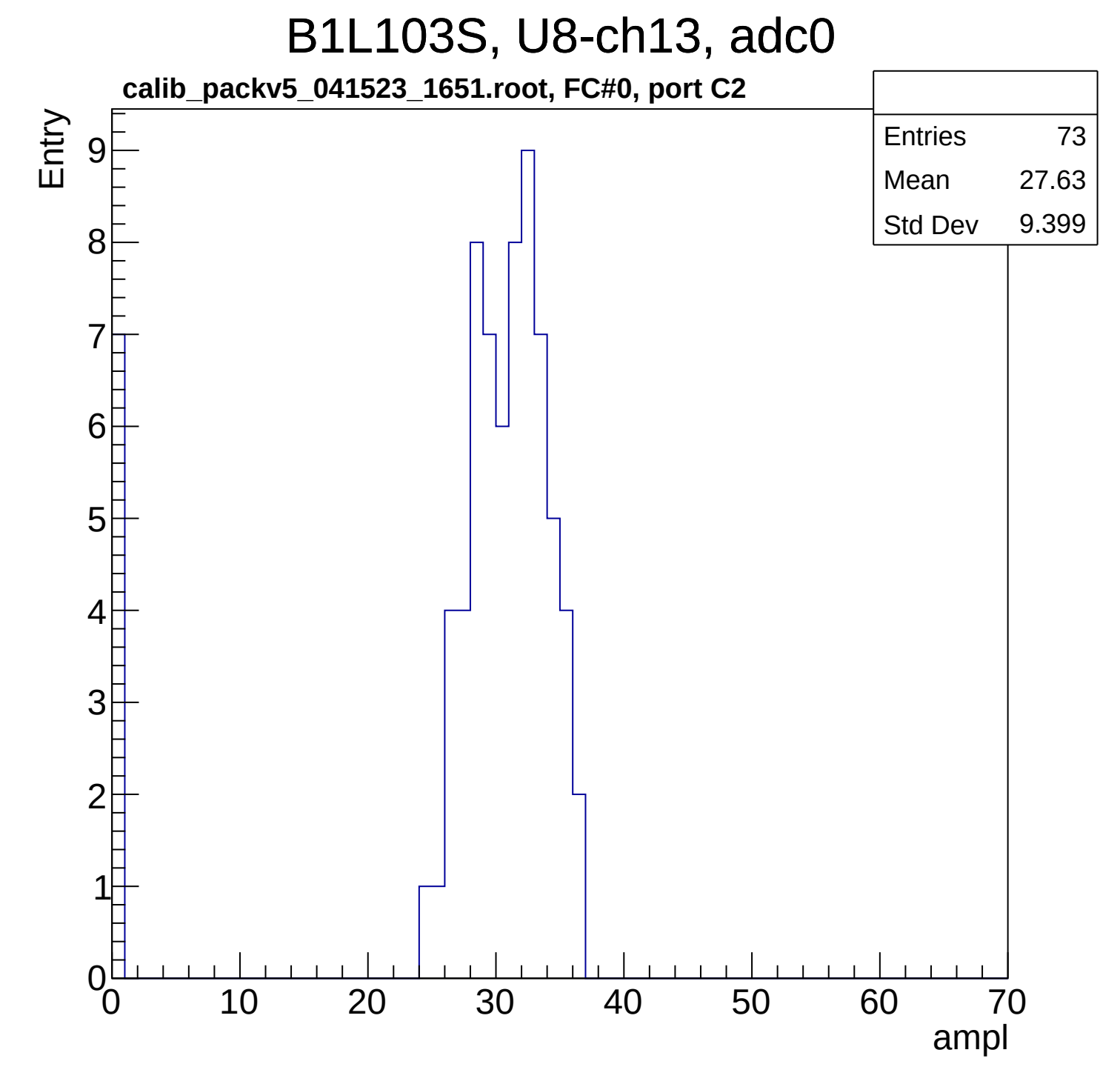
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch13, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 27.63
Std Dev 9.399
Entry
ampl
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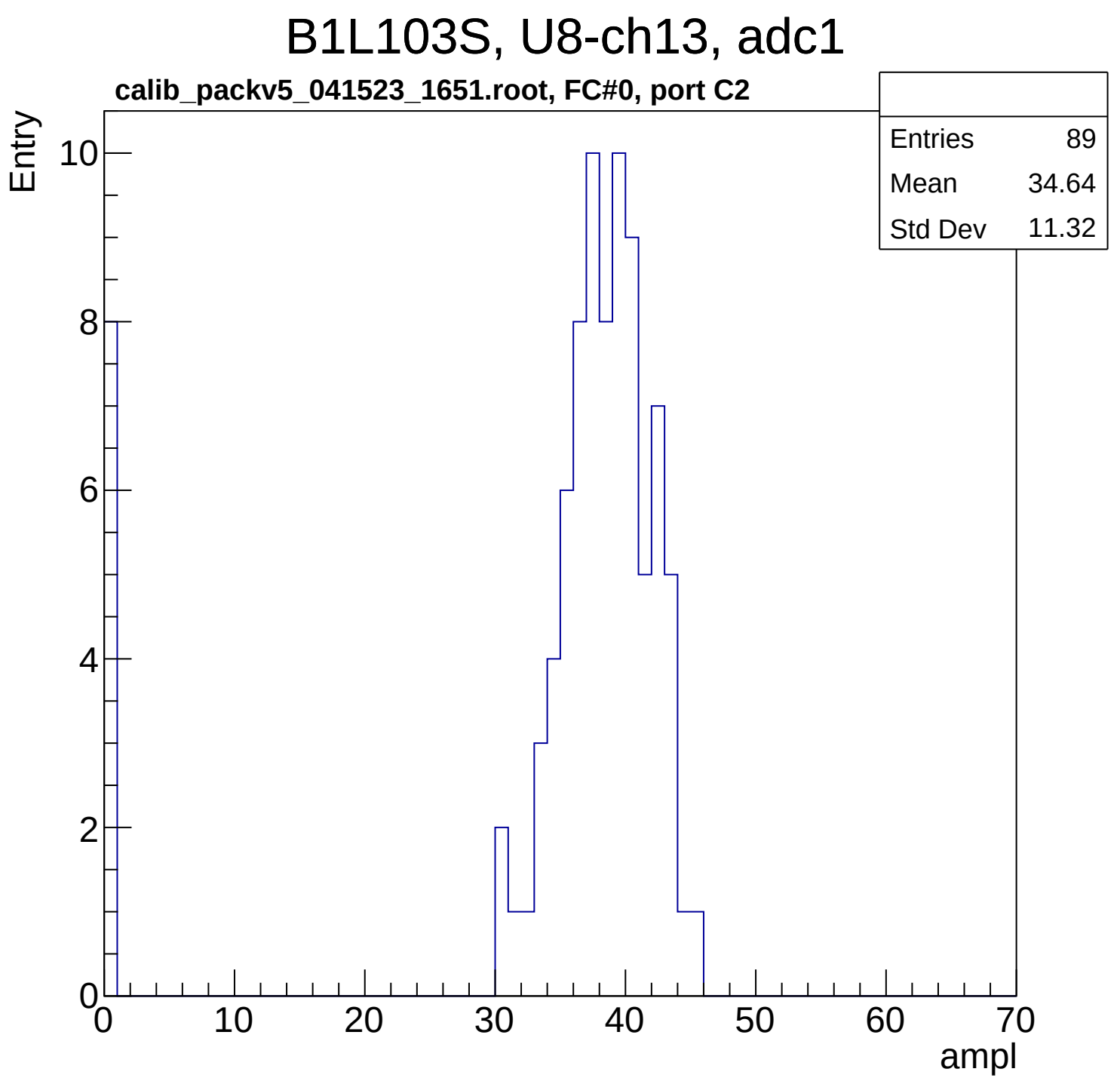
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U8-ch13, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 34.64
Std Dev 11.32
Entry
ampl
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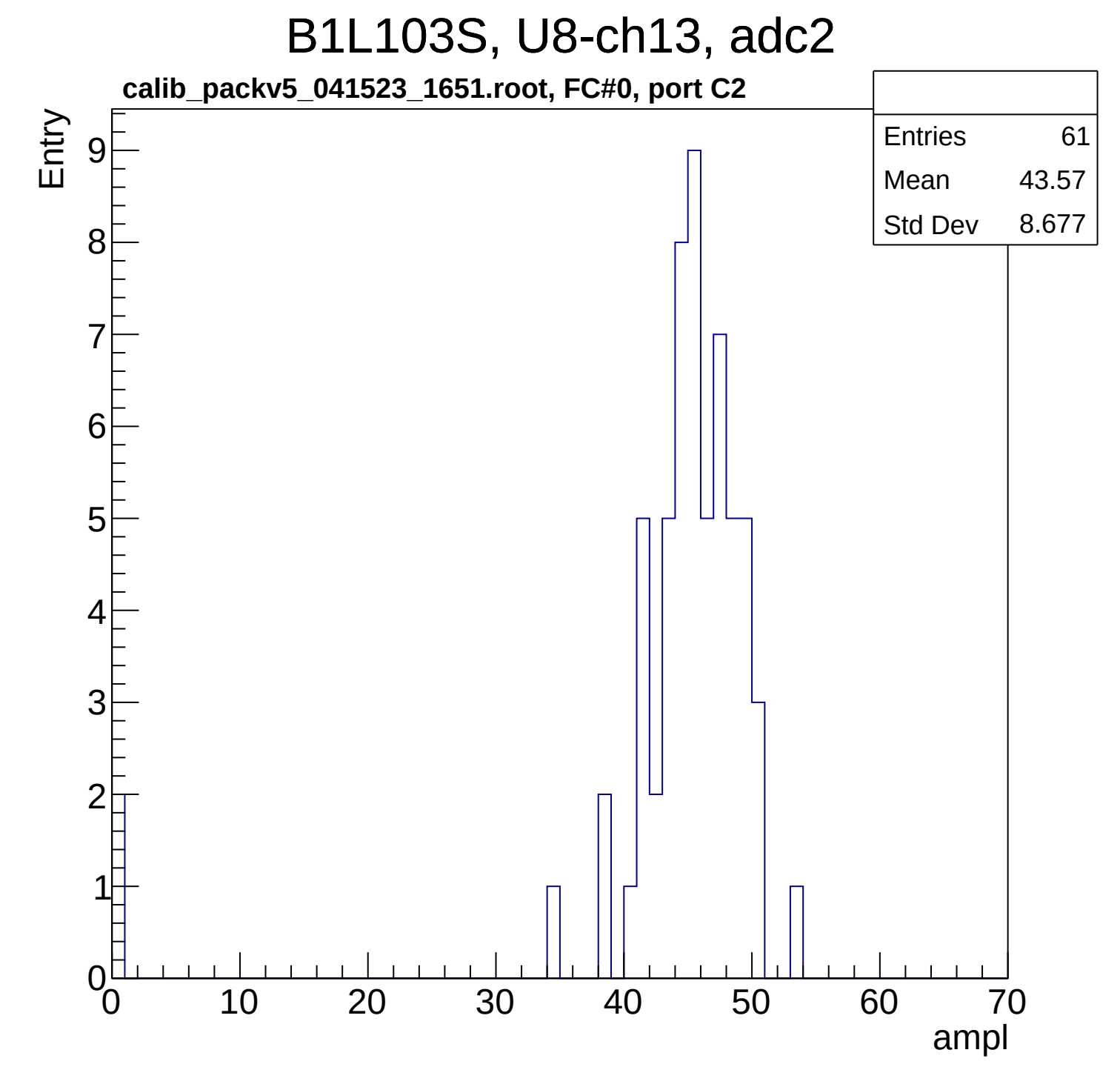
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U8-ch13, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 43.57
Std Dev 8.677
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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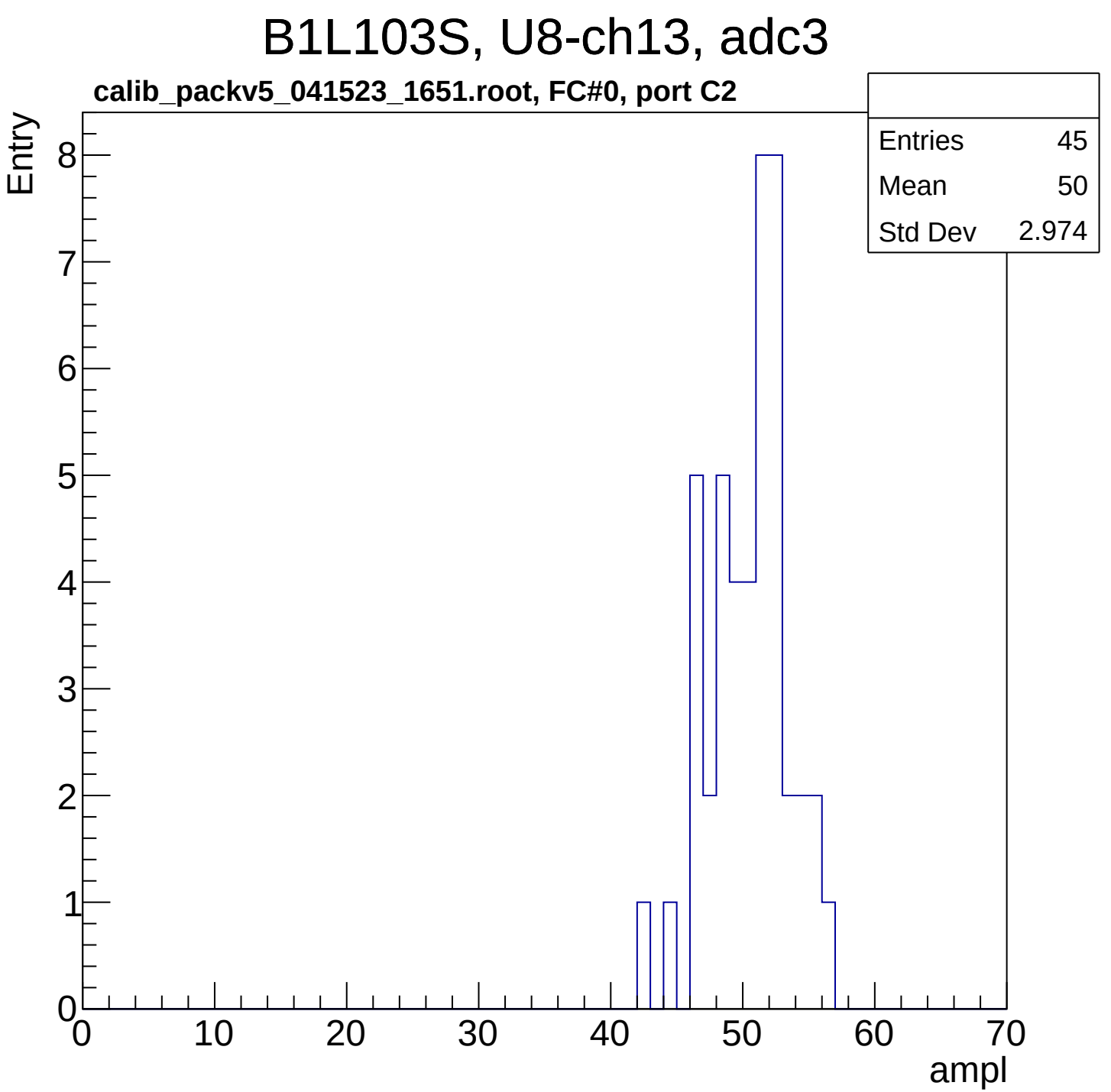
B1L103S, U8-ch13, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 50
Std Dev 2.974
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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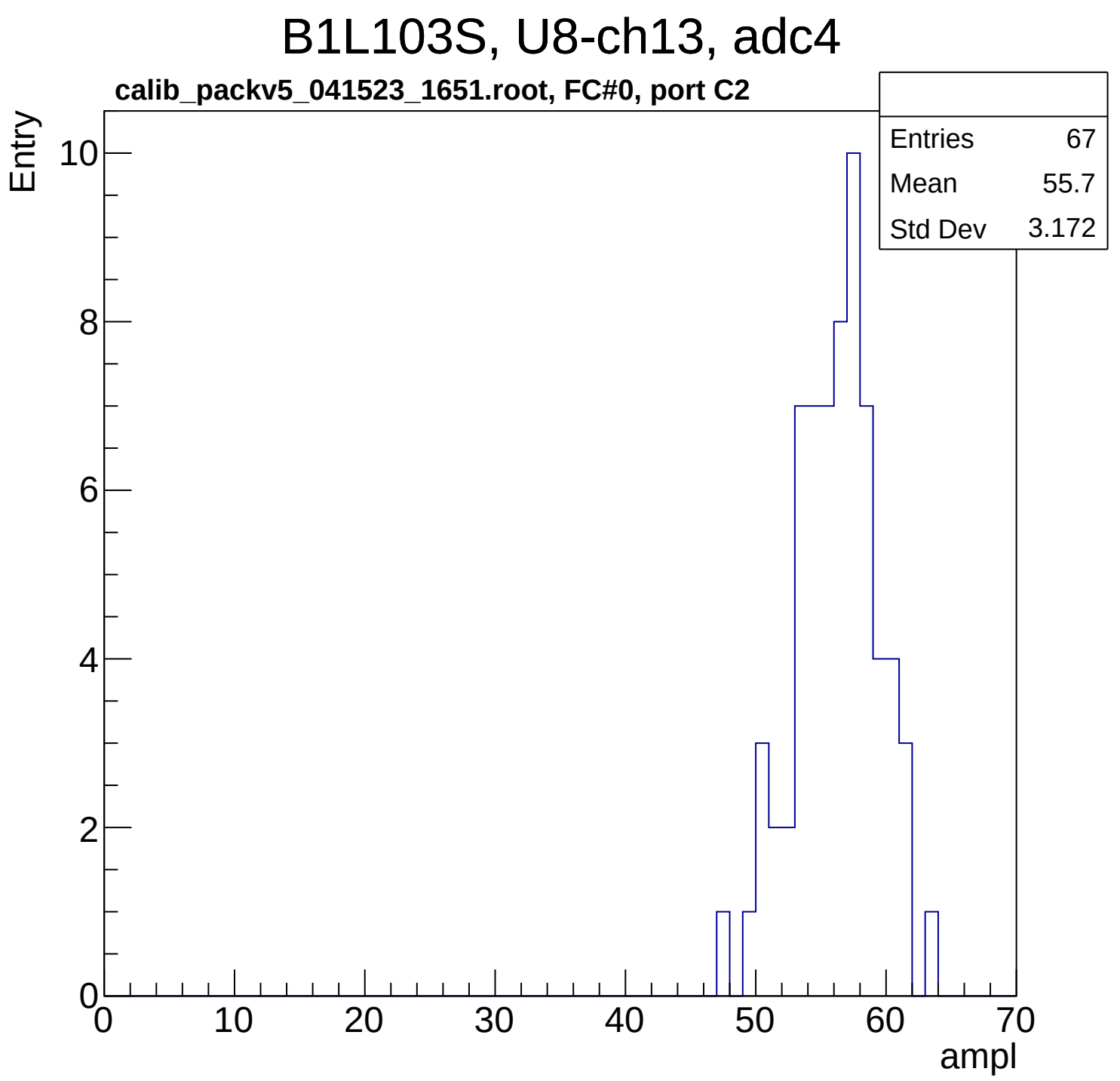
B1L103S, U8-ch13, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 55.7
Std Dev 3.172
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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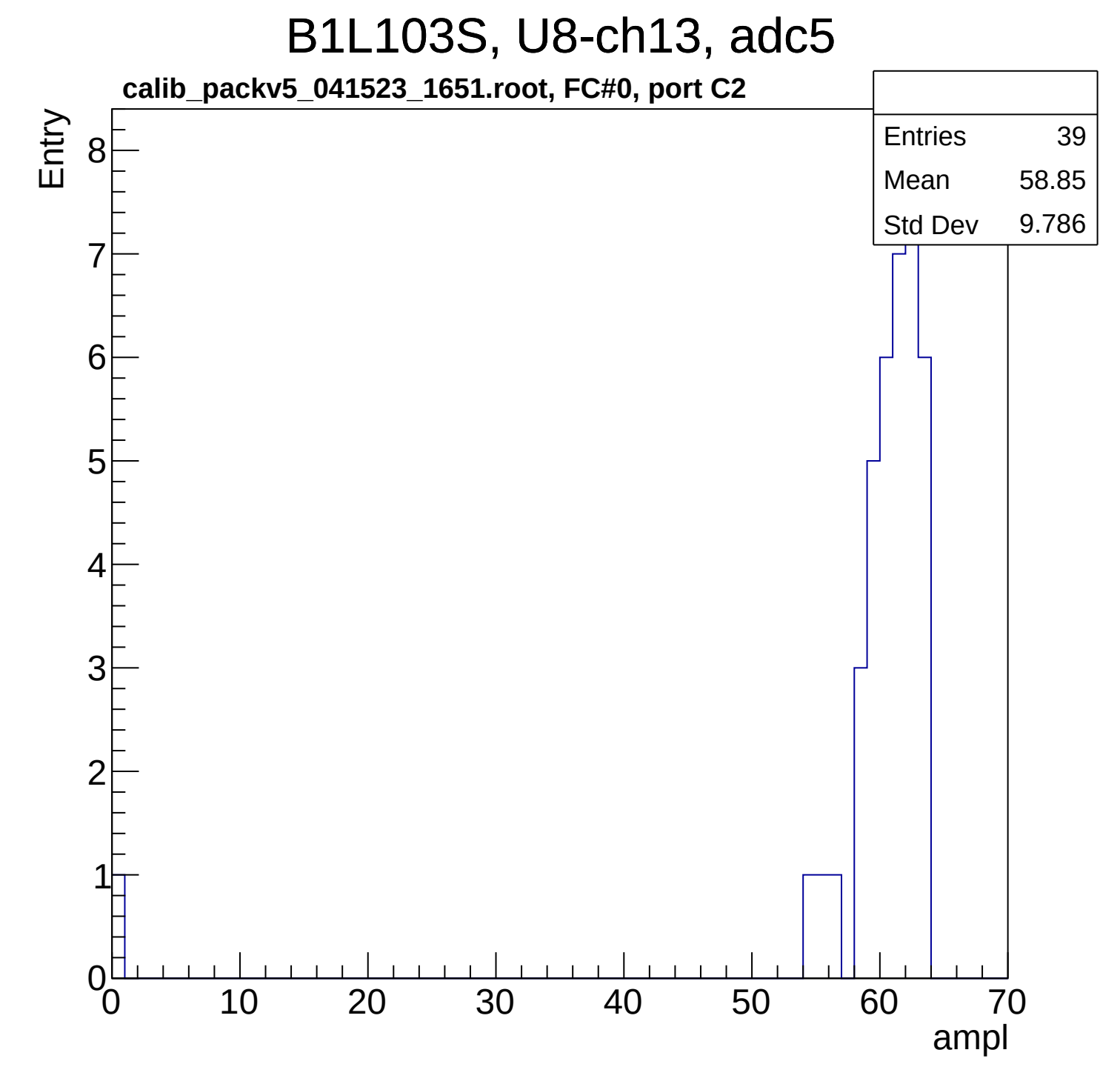
B1L103S, U8-ch13, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 58.85
Std Dev 9.786
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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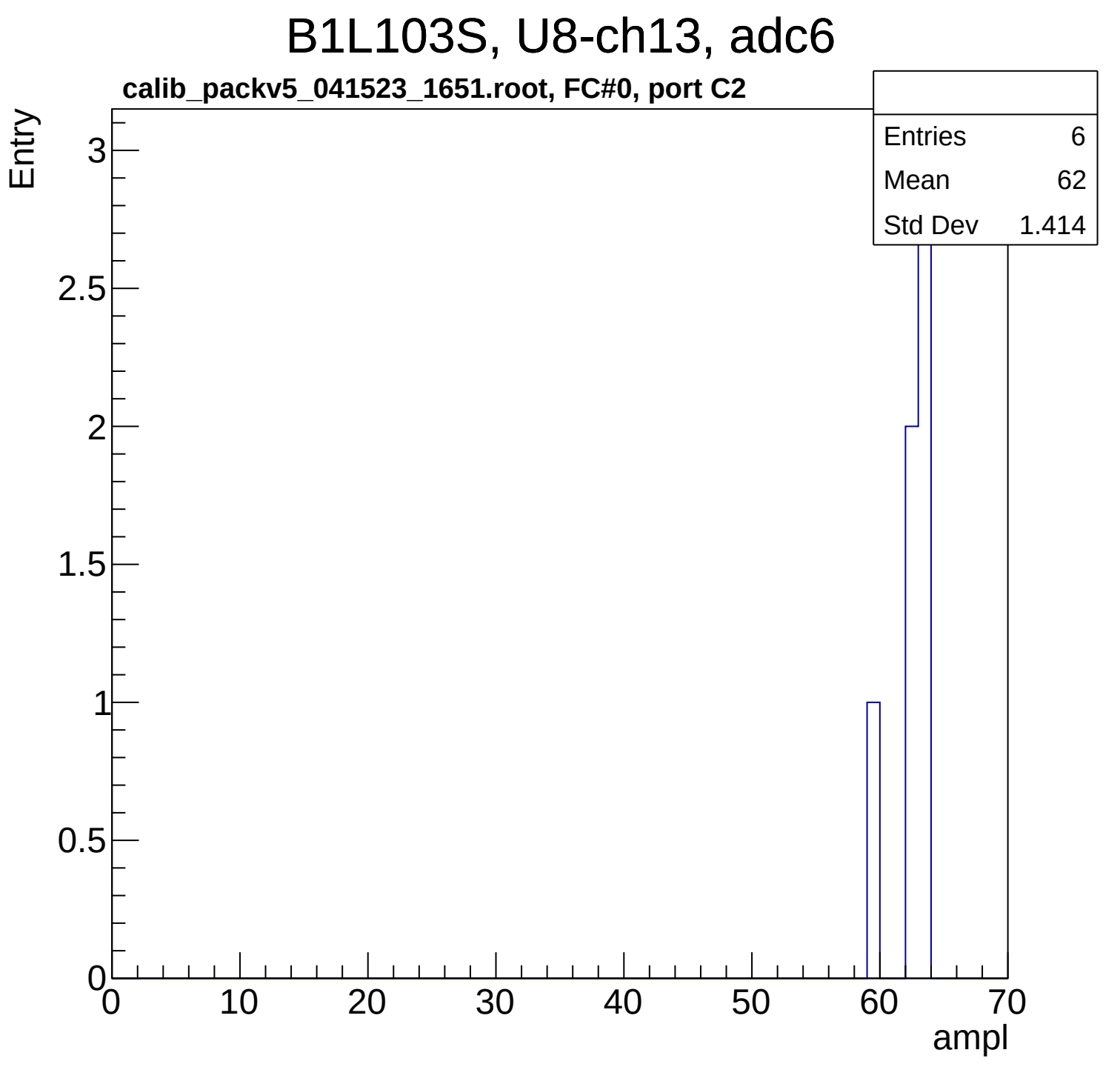
B1L103S, U8-ch13, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 62
Std Dev 1.414
Entry
ampl
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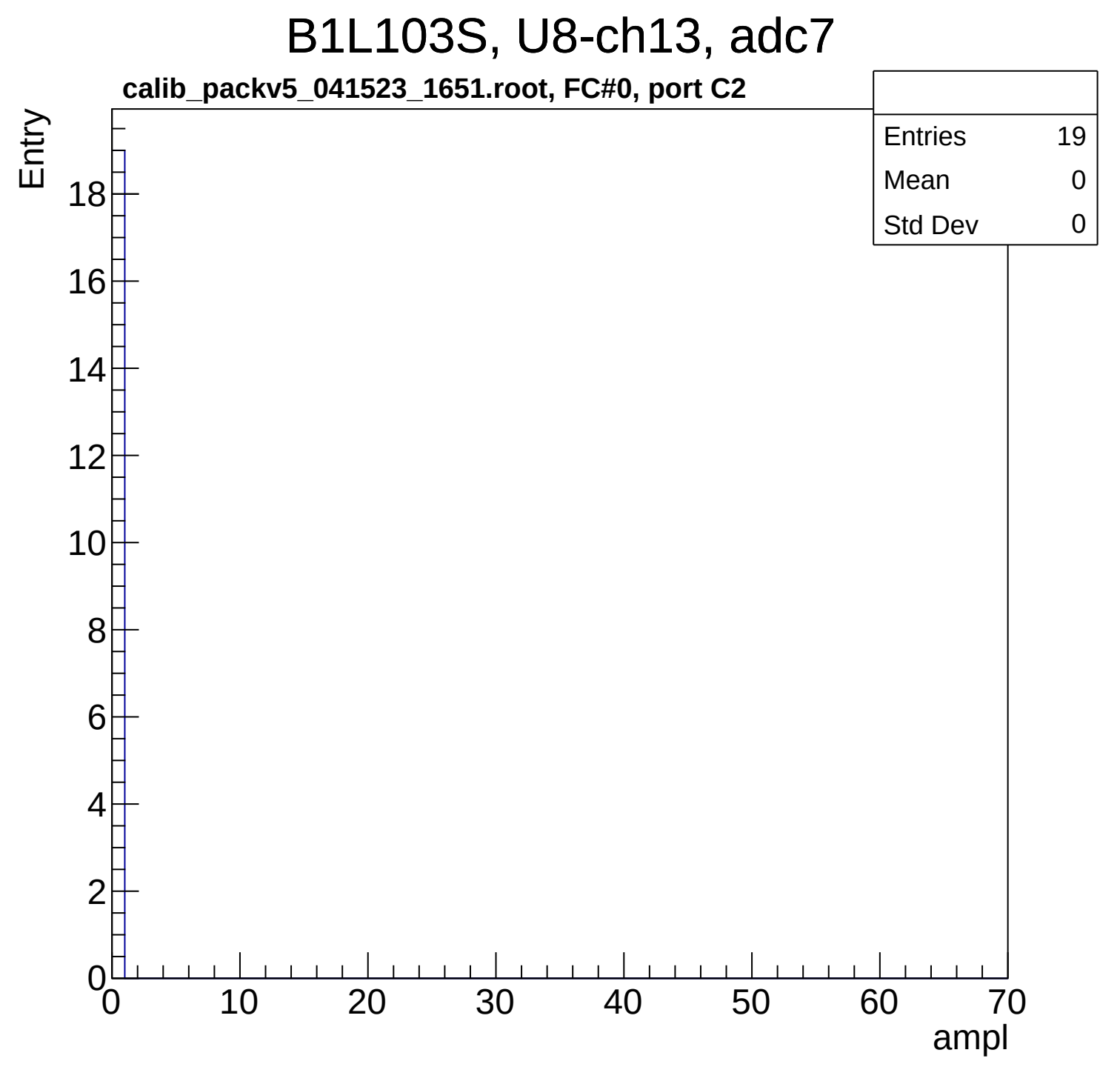
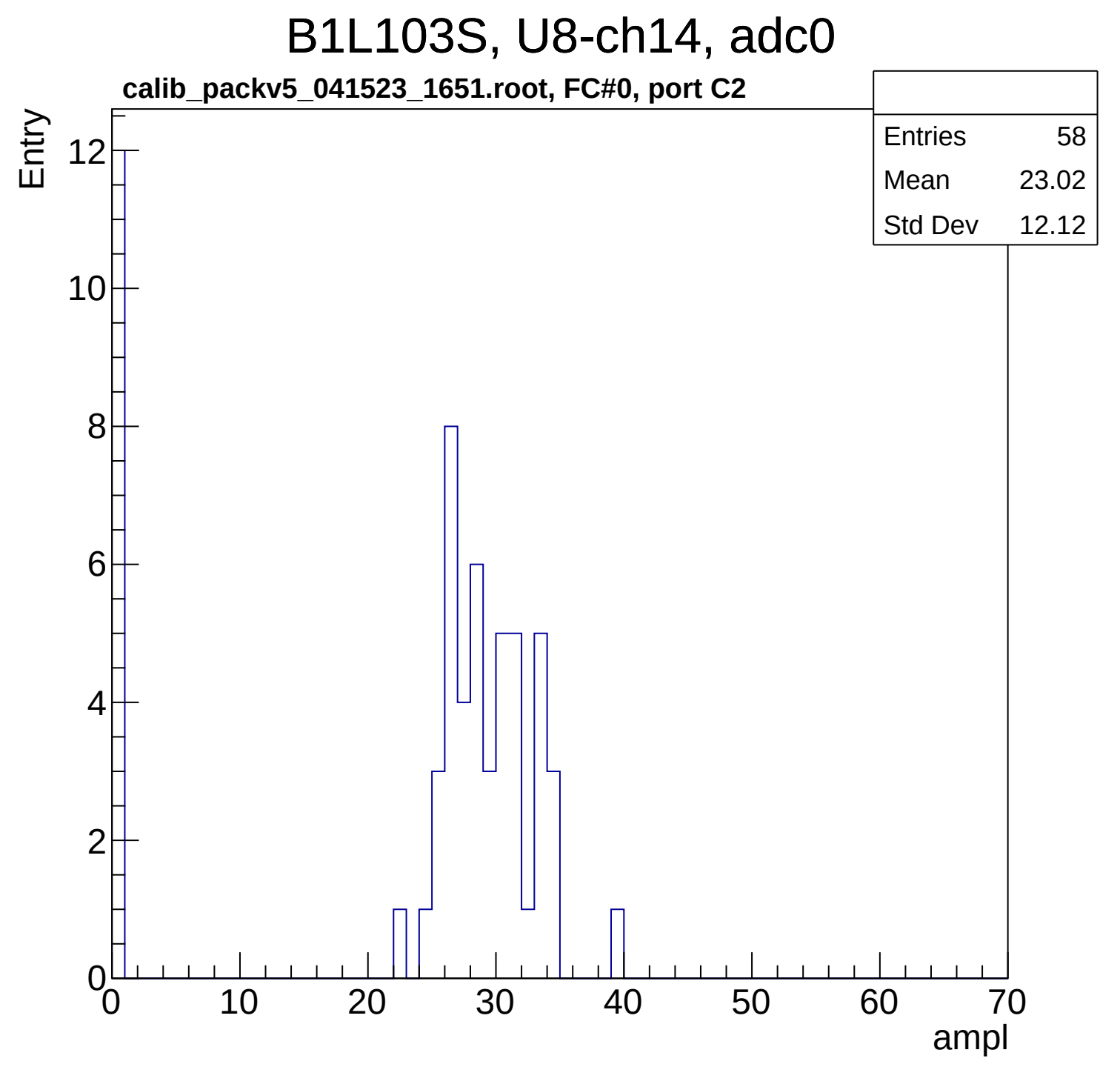
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U8-ch13, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch14, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 23.02
Std Dev 12.12
Entry
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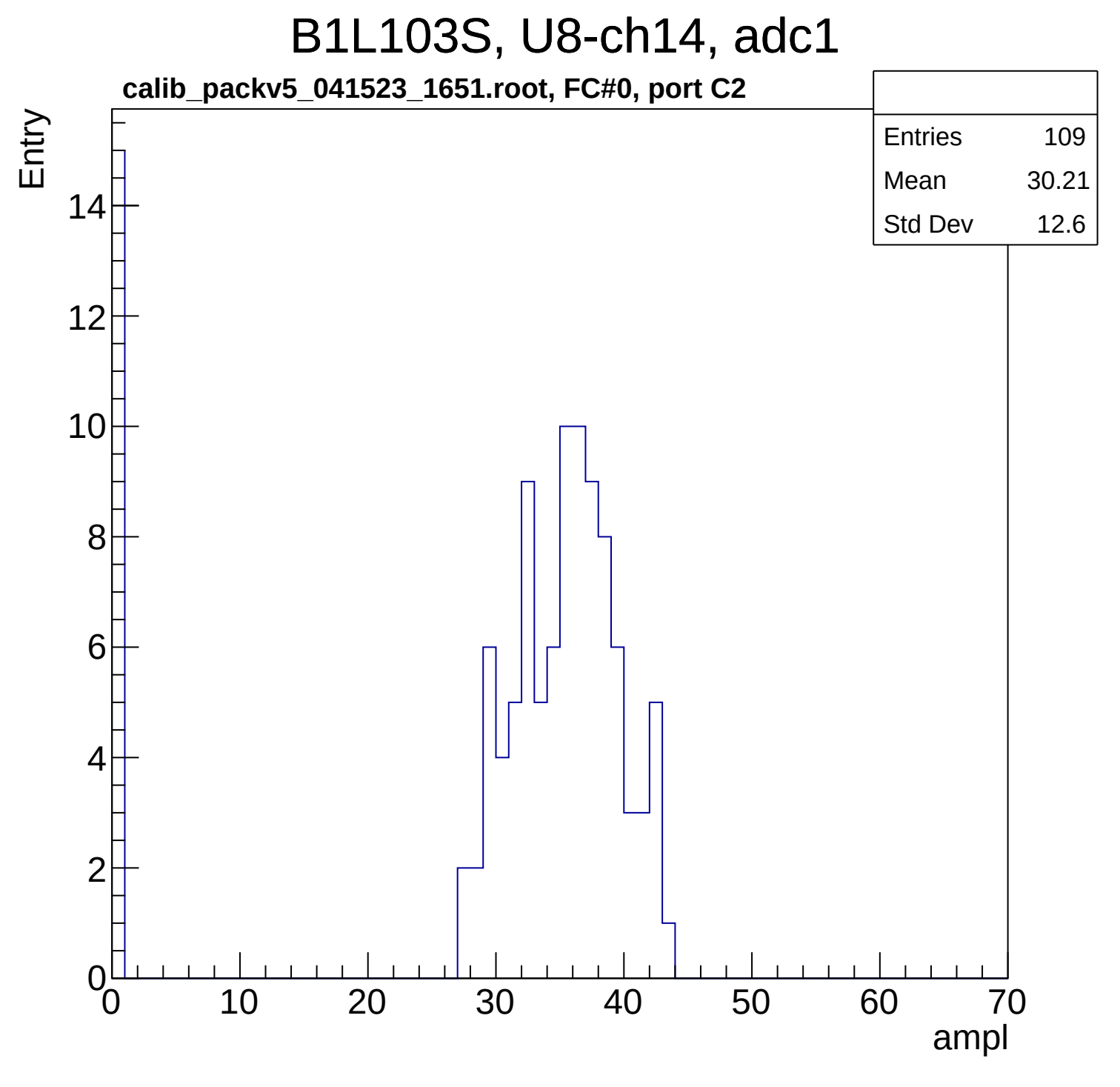
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch14, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 109
Mean 30.21
Std Dev 12.6
Entry
ampl
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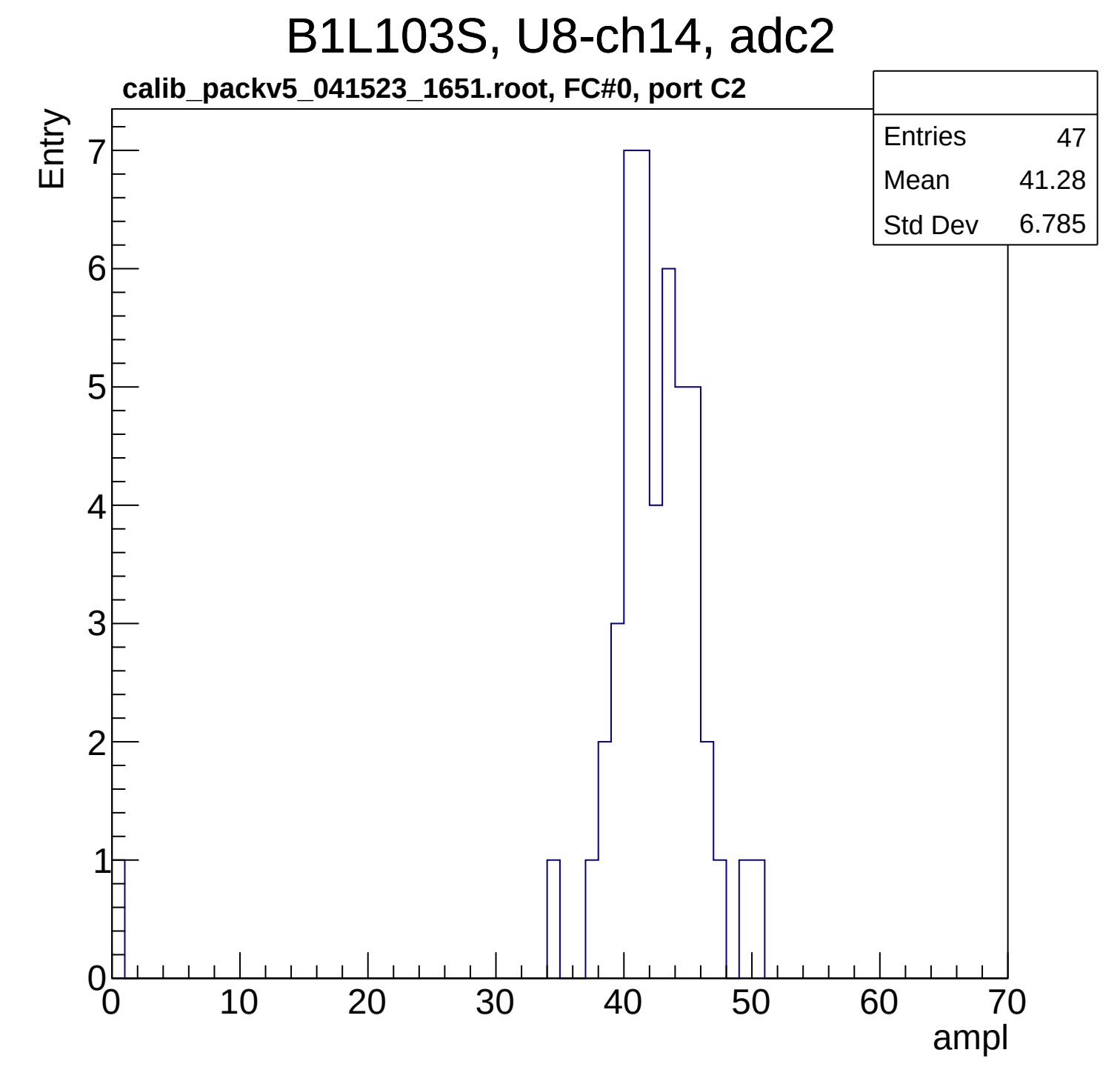
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U8-ch14, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 41.28
Std Dev 6.785
Entry
ampl
0
1
2
3
4
5
6
7
0
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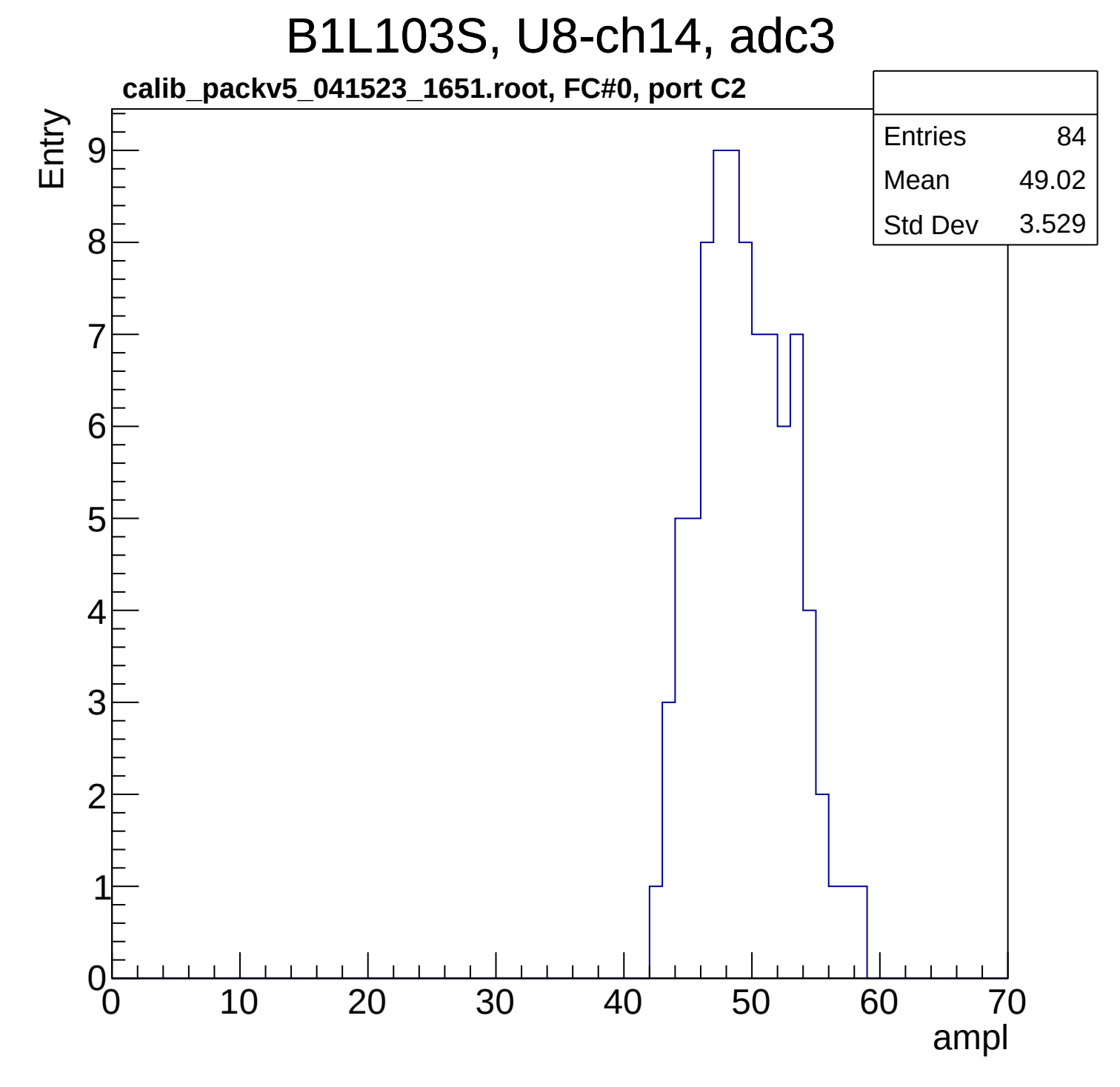
20
30
40
50
60
70


B1L103S, U8-ch14, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 49.02
Std Dev 3.529
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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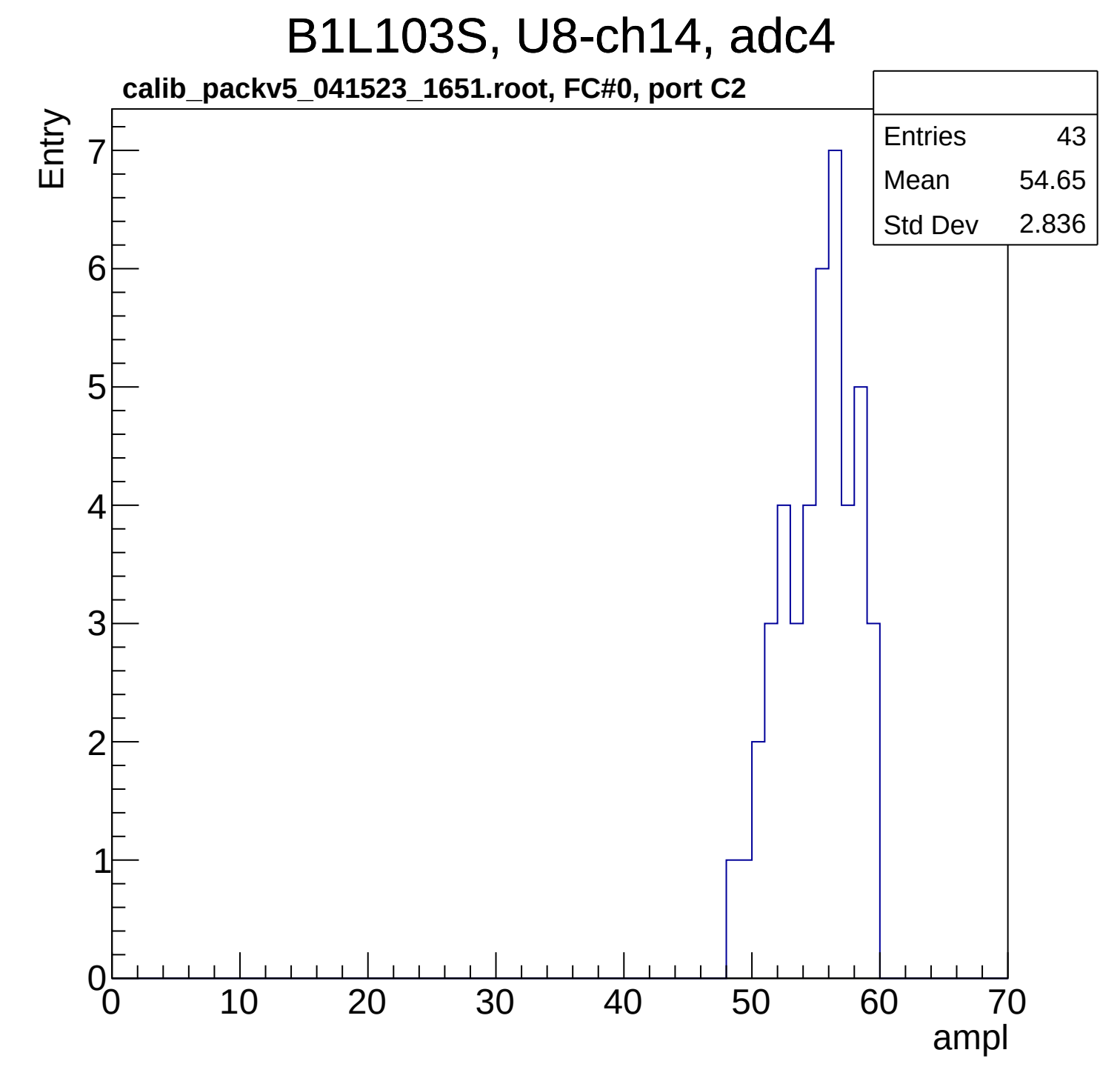
60
70


B1L103S, U8-ch14, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 54.65
Std Dev 2.836
Entry
ampl
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1
2
3
4
5
6
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0
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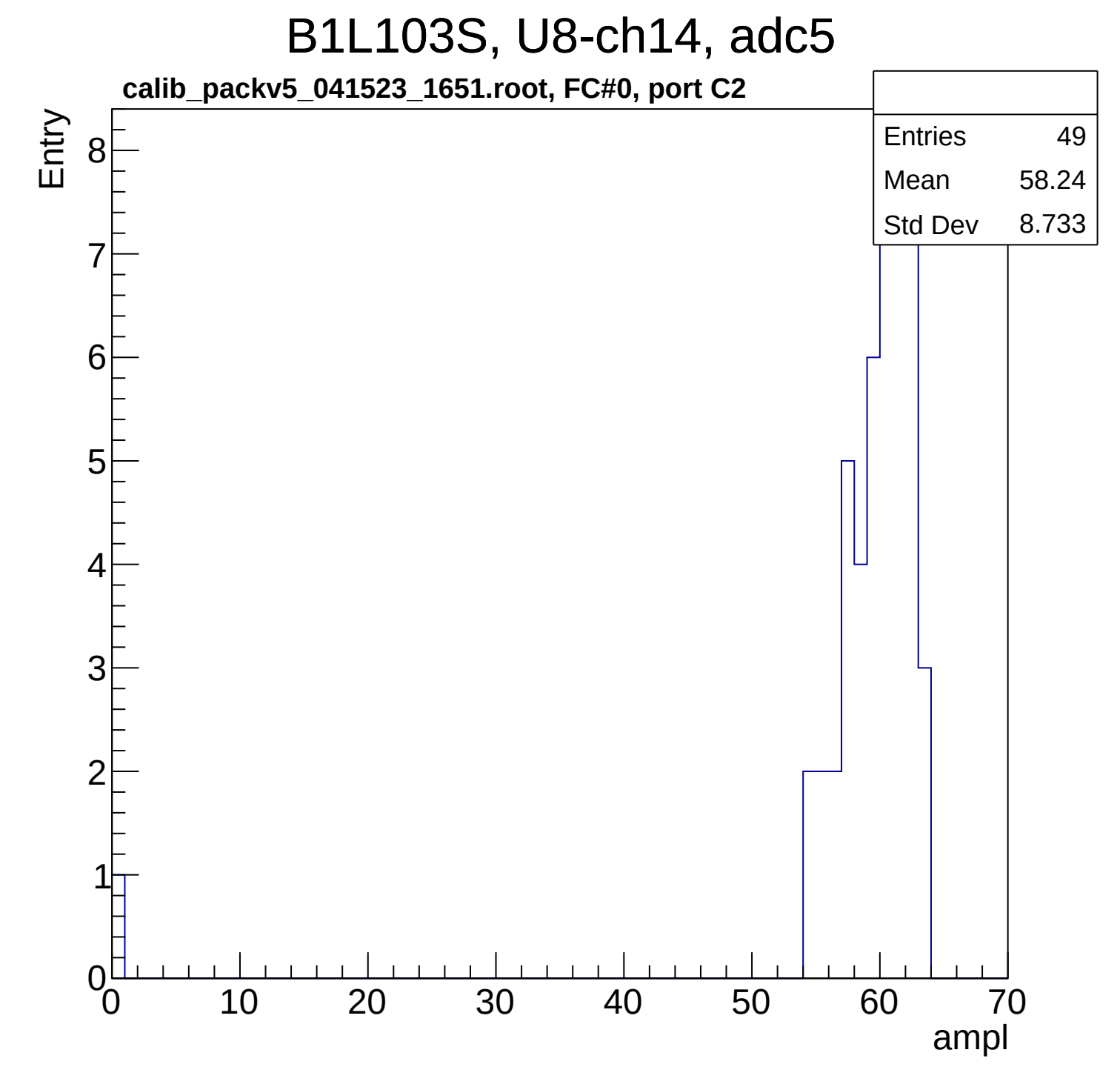
B1L103S, U8-ch14, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 58.24
Std Dev 8.733
Entry
ampl
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1
2
3
4
5
6
7
8
0
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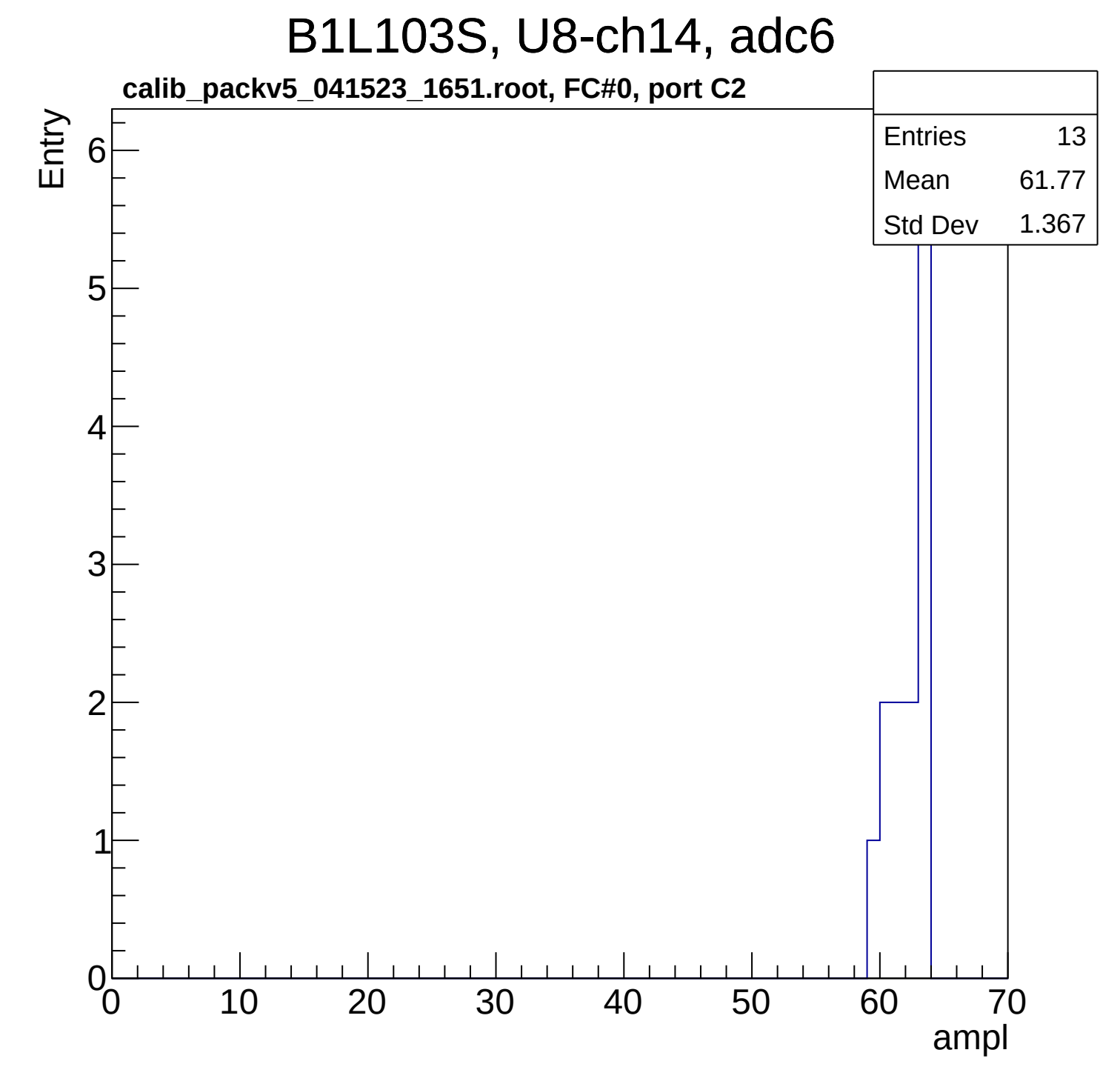
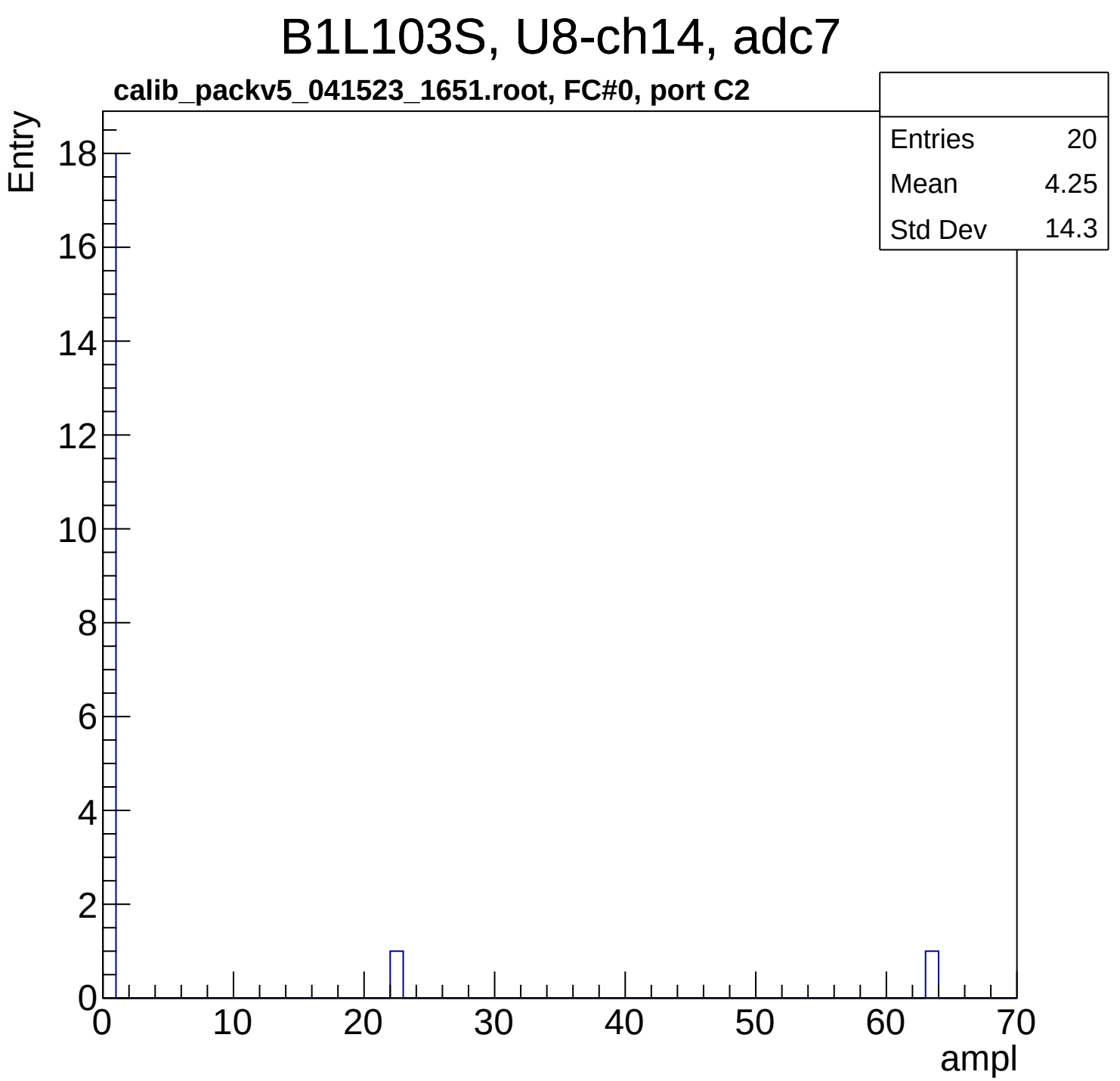
20
30
40
50
60
70


B1L103S, U8-ch14, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 61.77
Std Dev 1.367
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch14, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4.25
Std Dev 14.3
Entry
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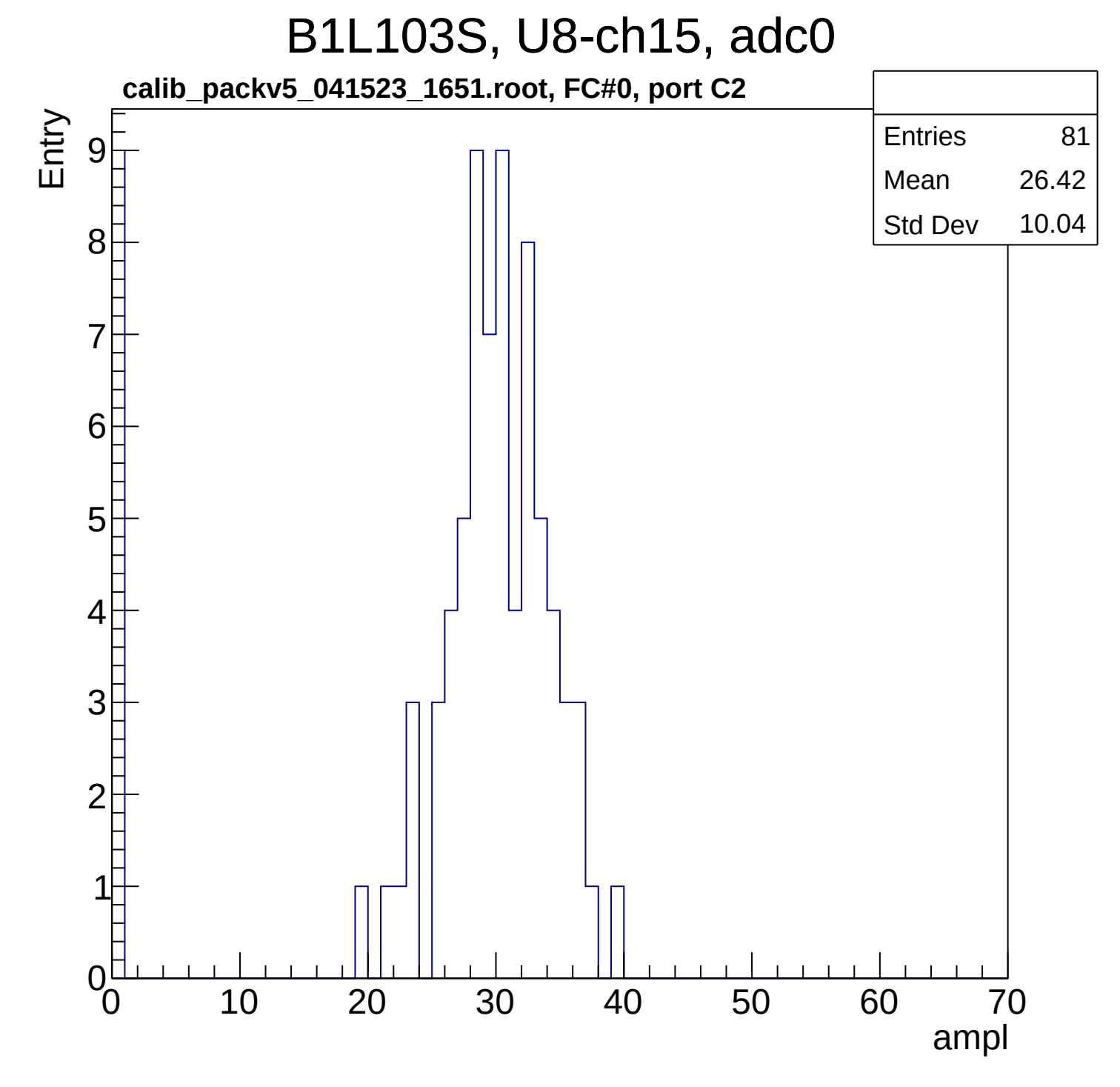
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch15, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 26.42
Std Dev 10.04
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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60
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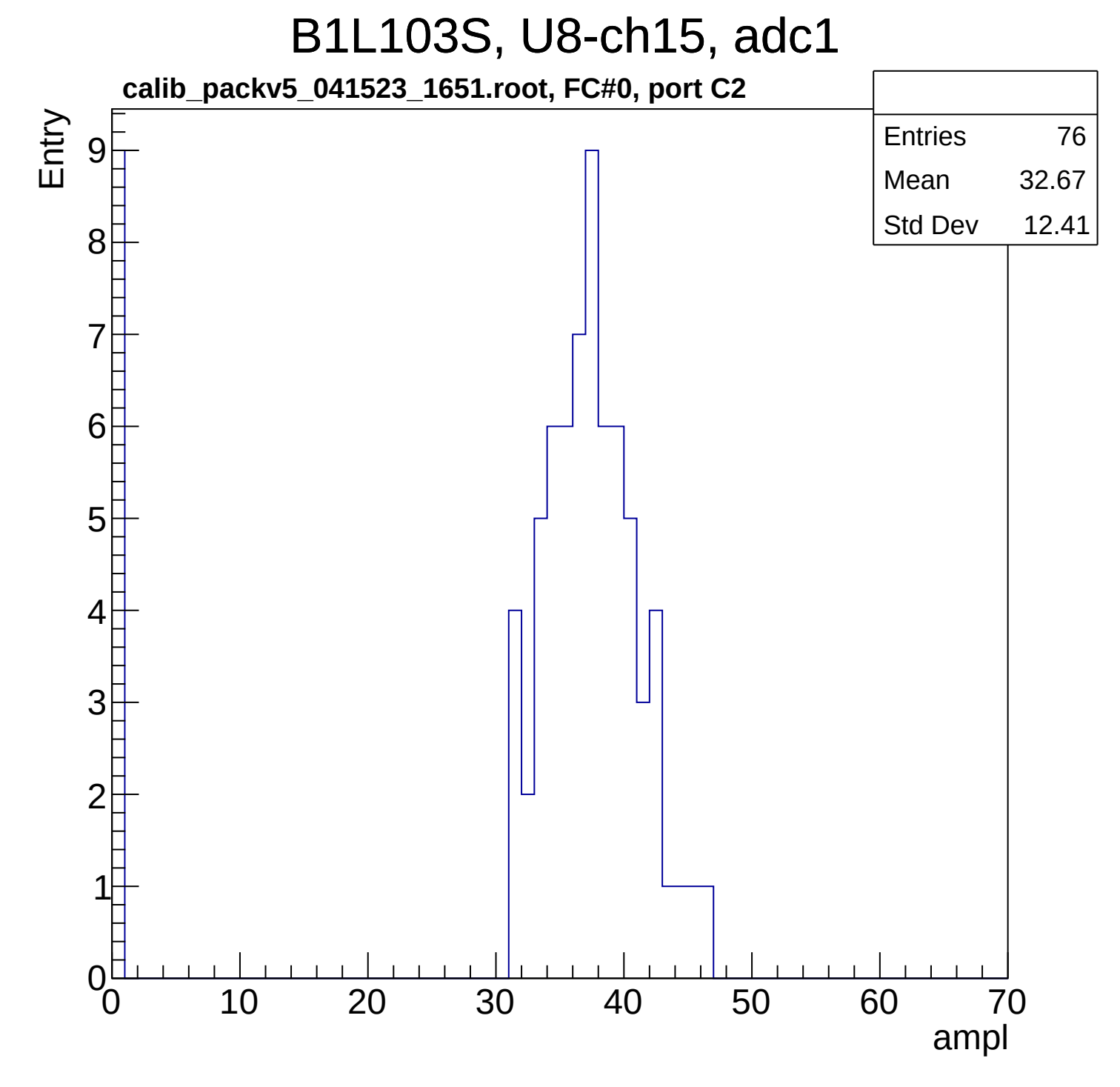
B1L103S, U8-ch15, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 32.67
Std Dev 12.41
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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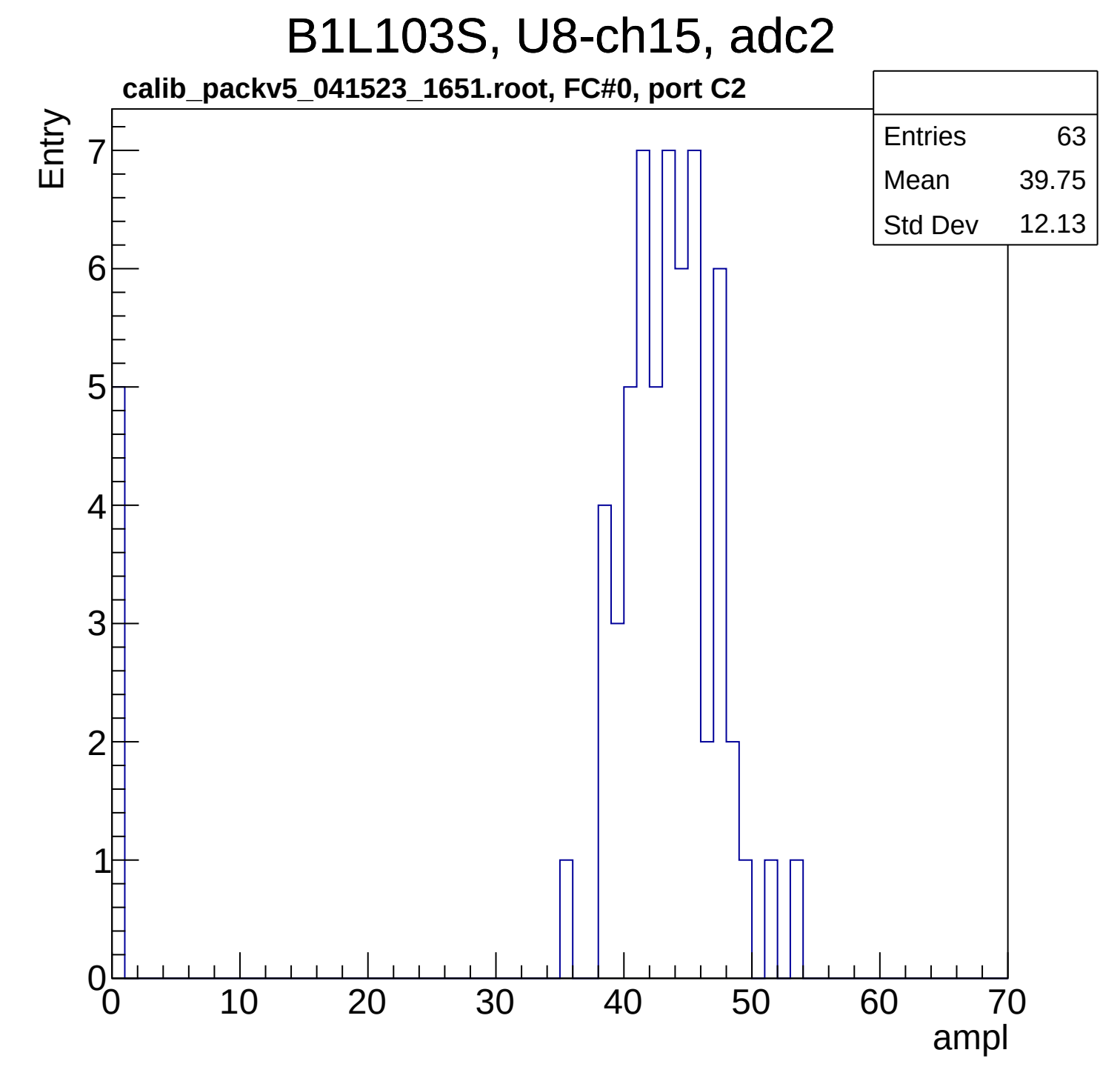
B1L103S, U8-ch15, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 39.75
Std Dev 12.13
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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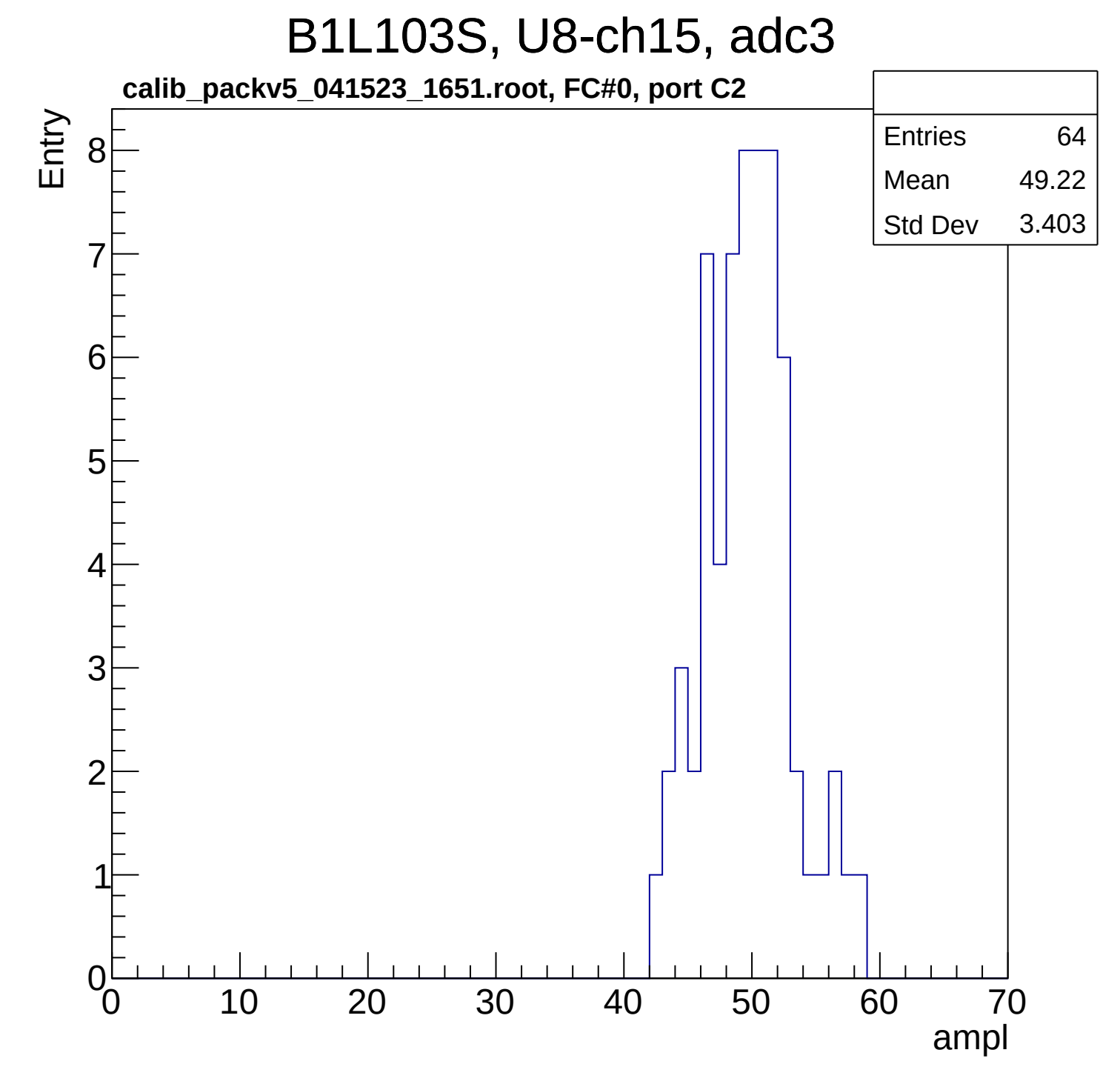
40
50
60
70


B1L103S, U8-ch15, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 49.22
Std Dev 3.403
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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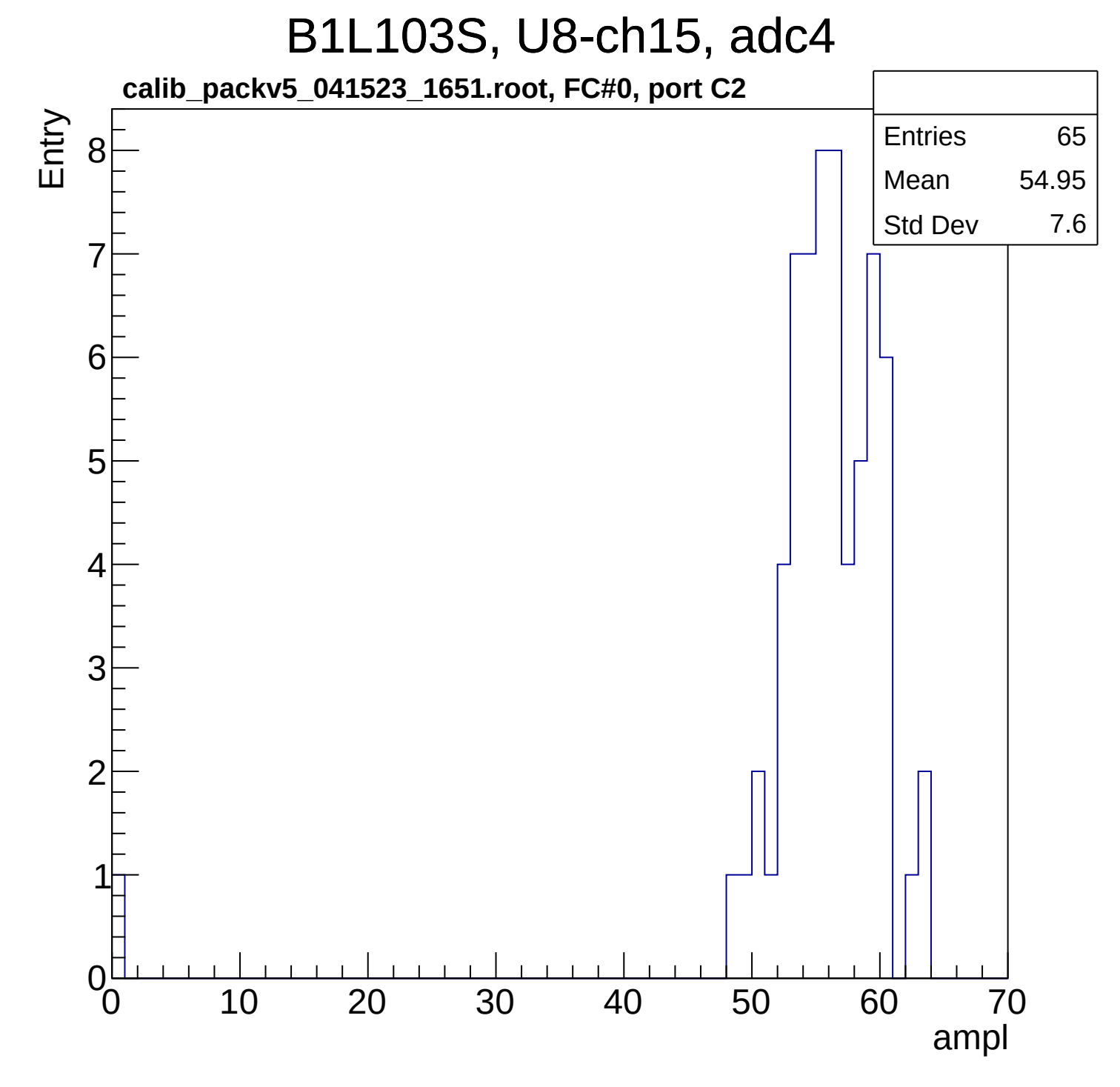
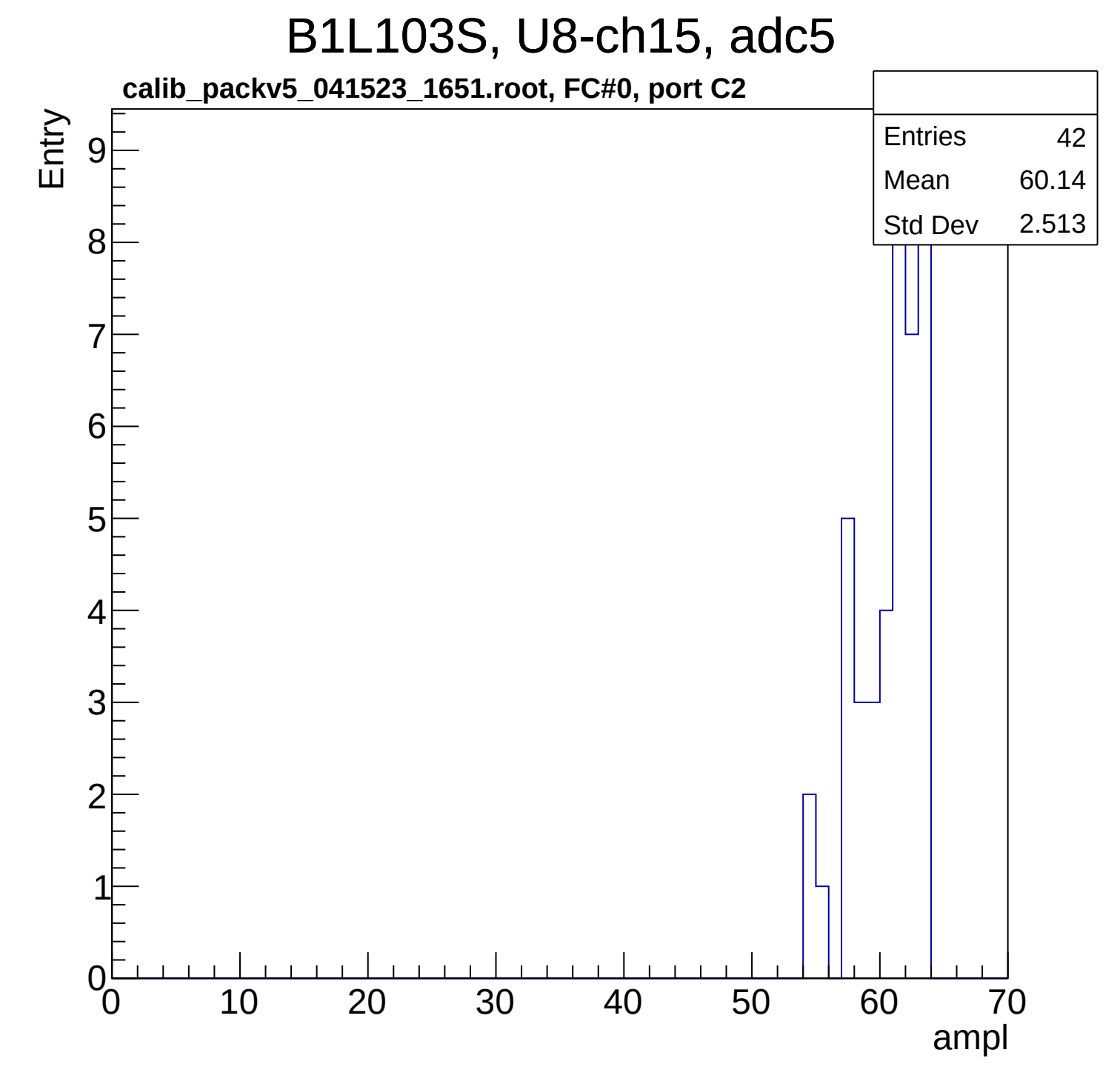

B1L103S, U8-ch15, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 54.95
Std Dev 7.6
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch15, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 60.14
Std Dev 2.513
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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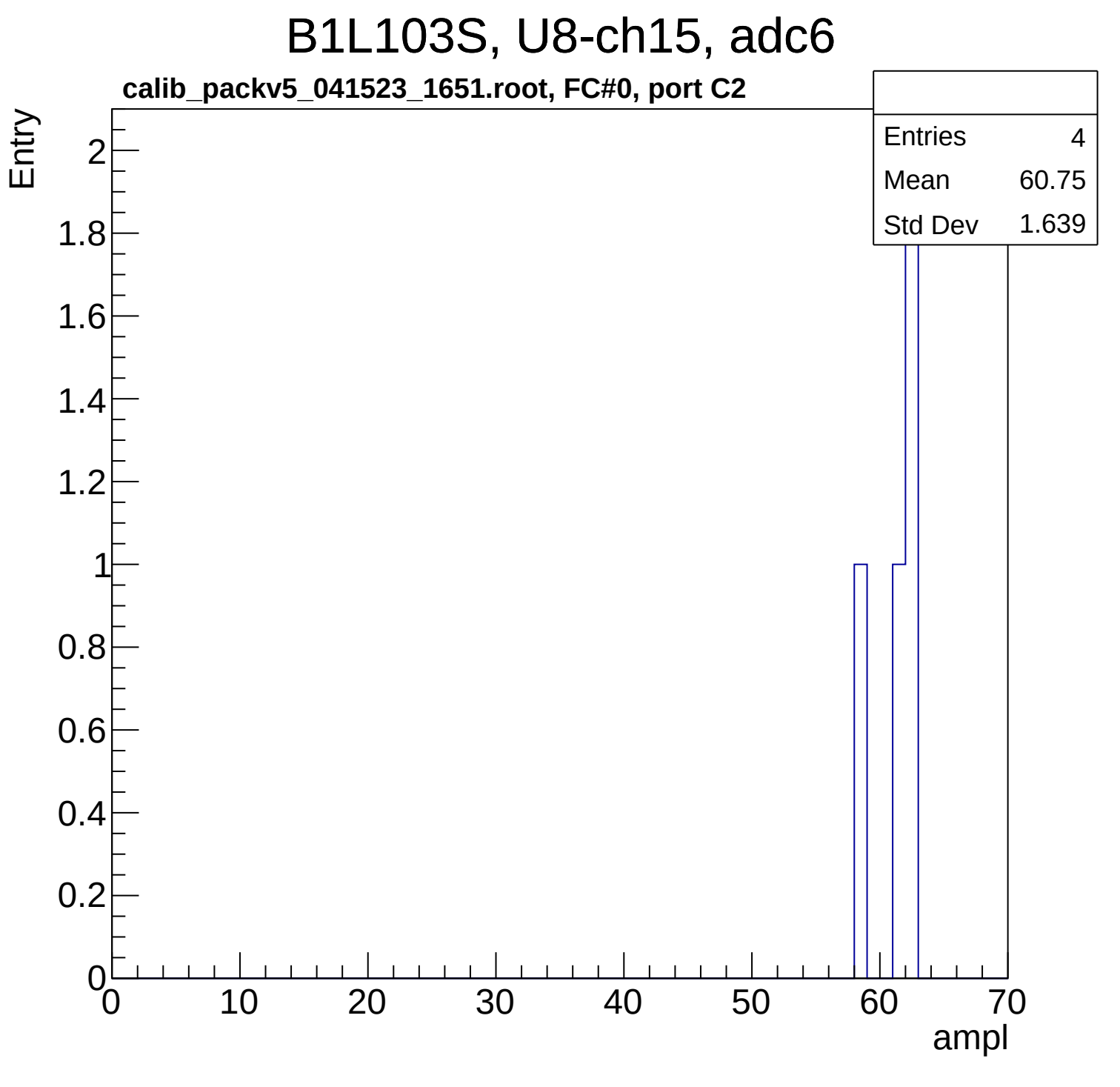
B1L103S, U8-ch15, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 60.75
Std Dev 1.639
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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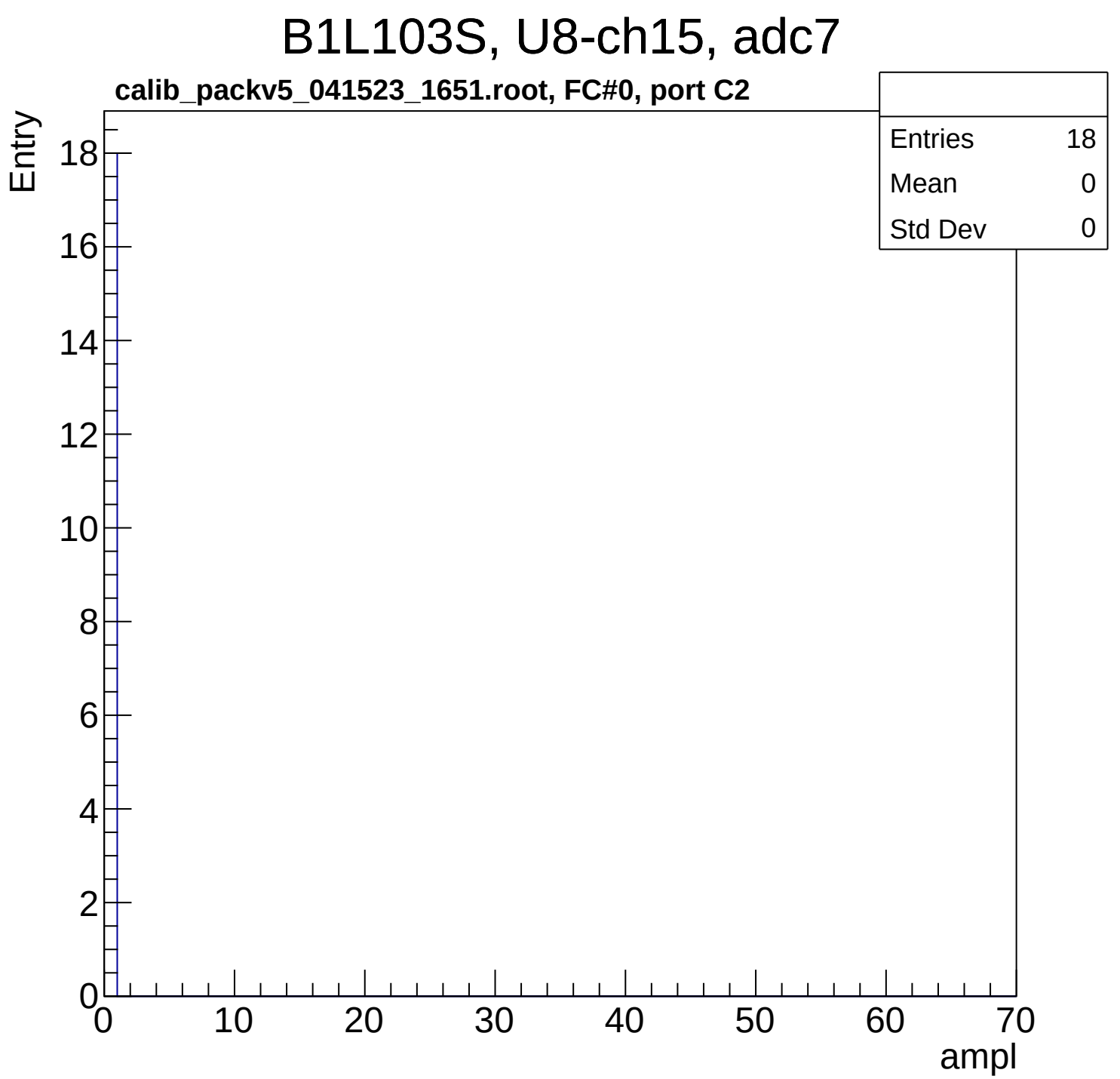
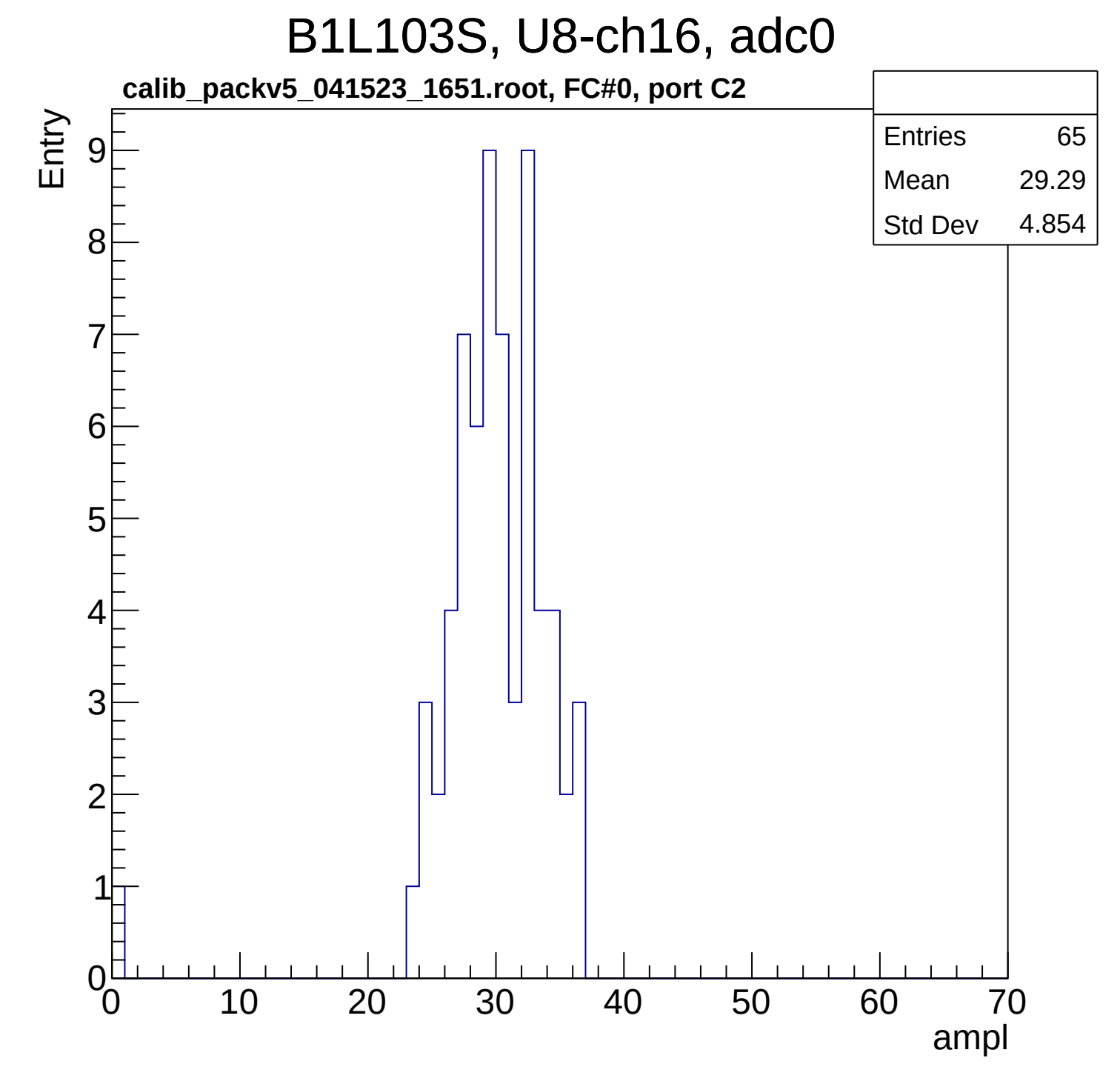
40
50
60
70


B1L103S, U8-ch15, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch16, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 29.29
Std Dev 4.854
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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20
30
40
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60
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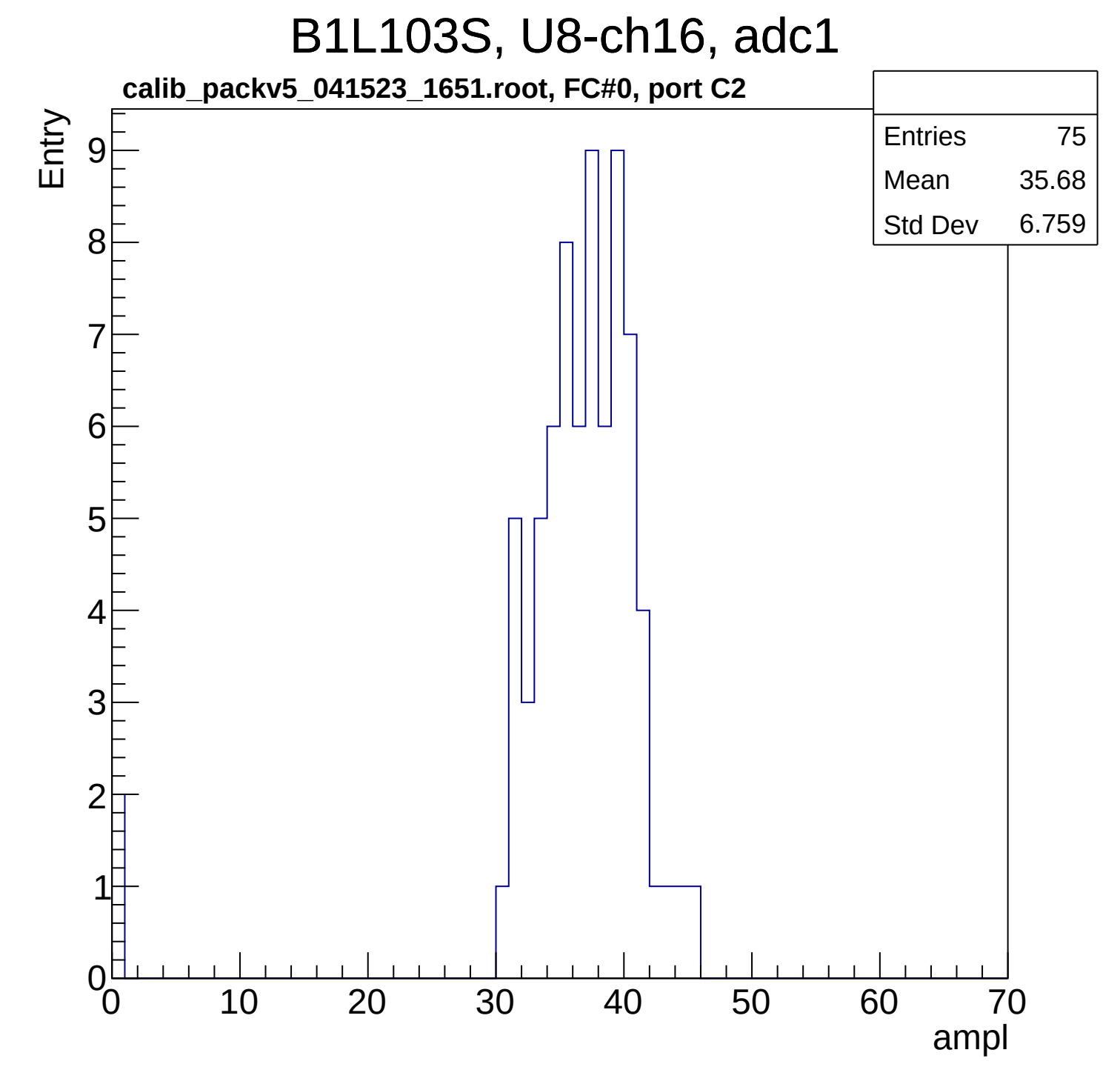
B1L103S, U8-ch16, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 35.68
Std Dev 6.759
Entry
ampl
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3
4
5
6
7
8
9
0
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40
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60
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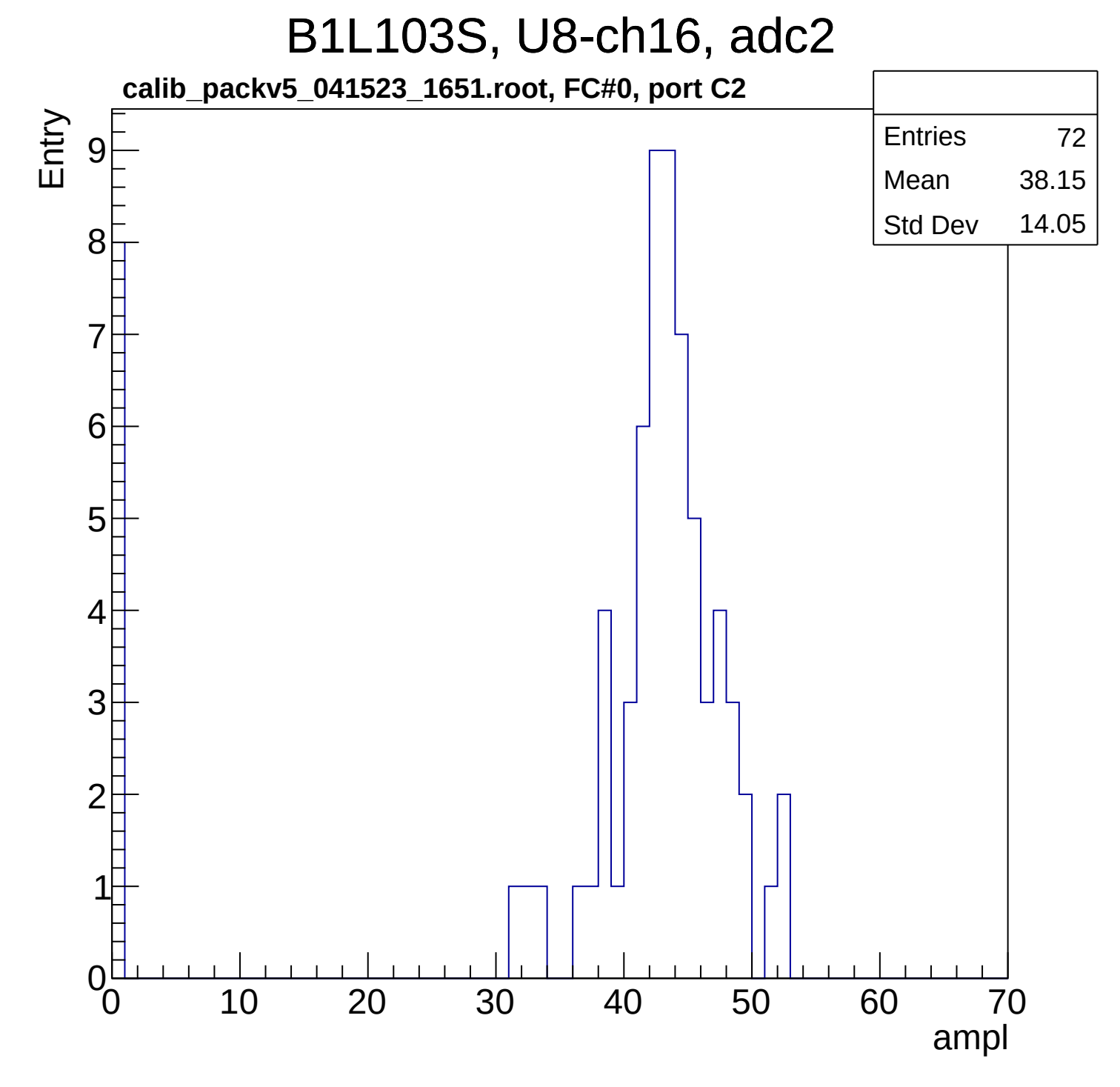
B1L103S, U8-ch16, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 38.15
Std Dev 14.05
Entry
ampl
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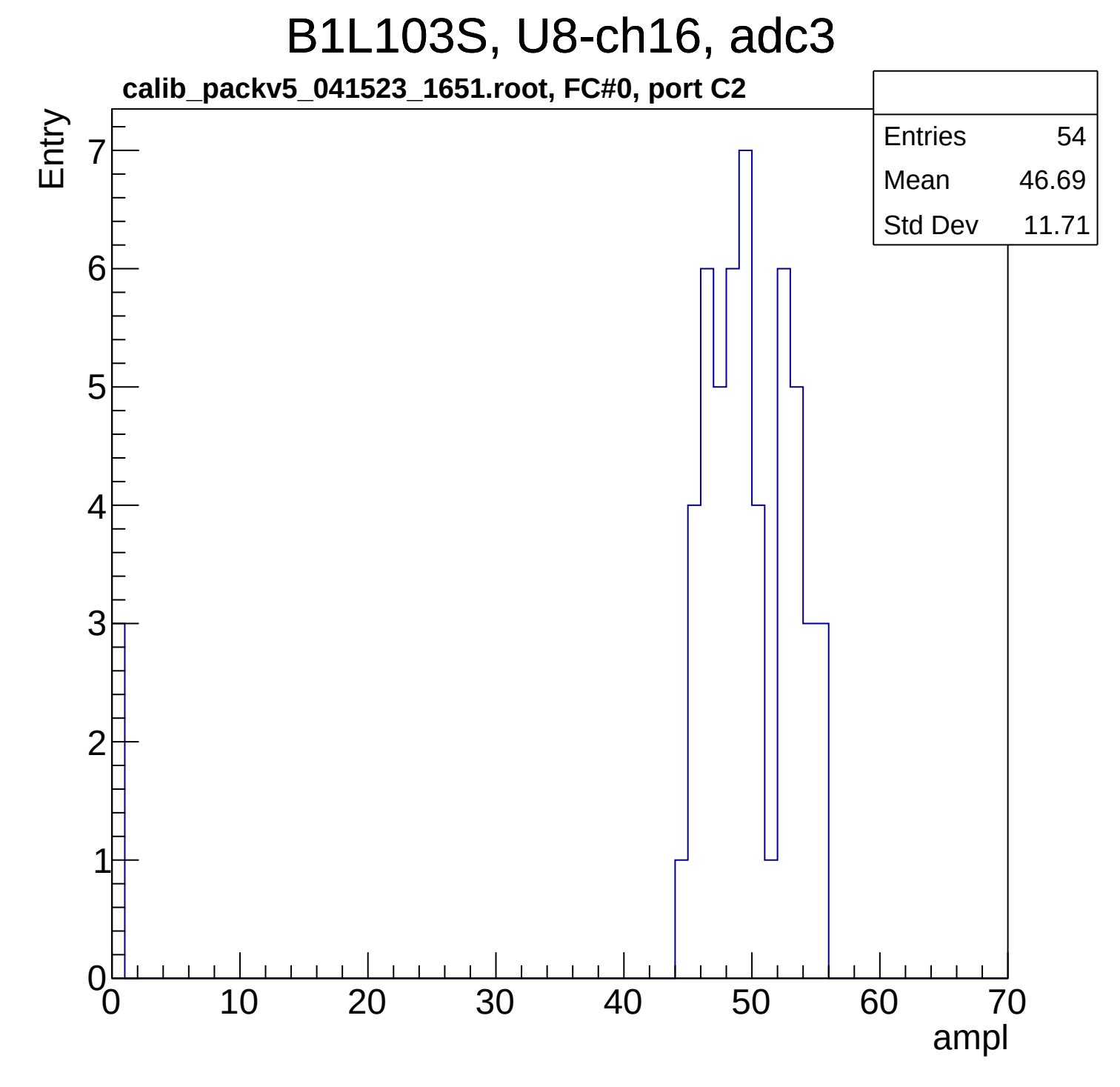
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U8-ch16, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 46.69
Std Dev 11.71
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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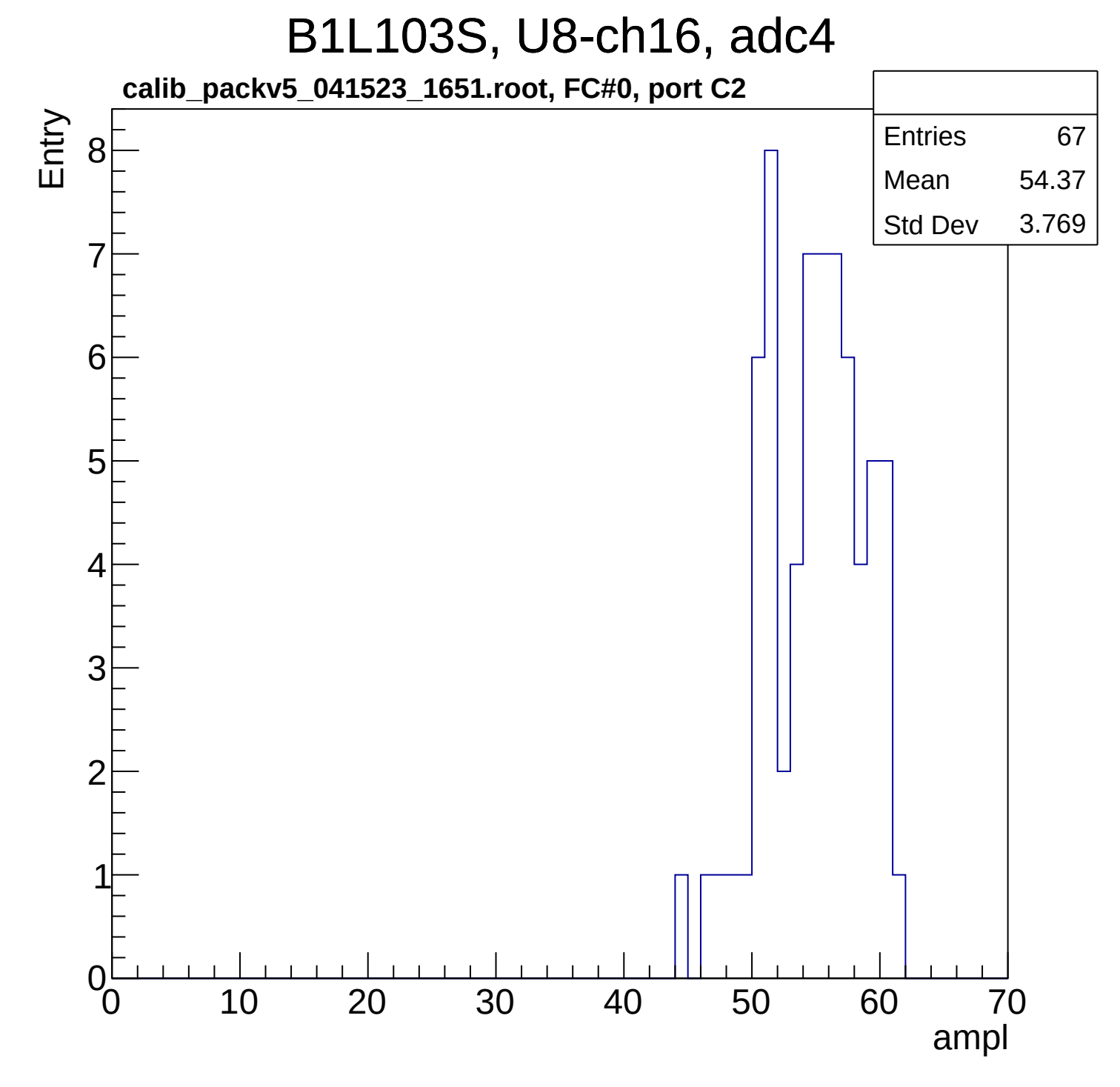
B1L103S, U8-ch16, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 54.37
Std Dev 3.769
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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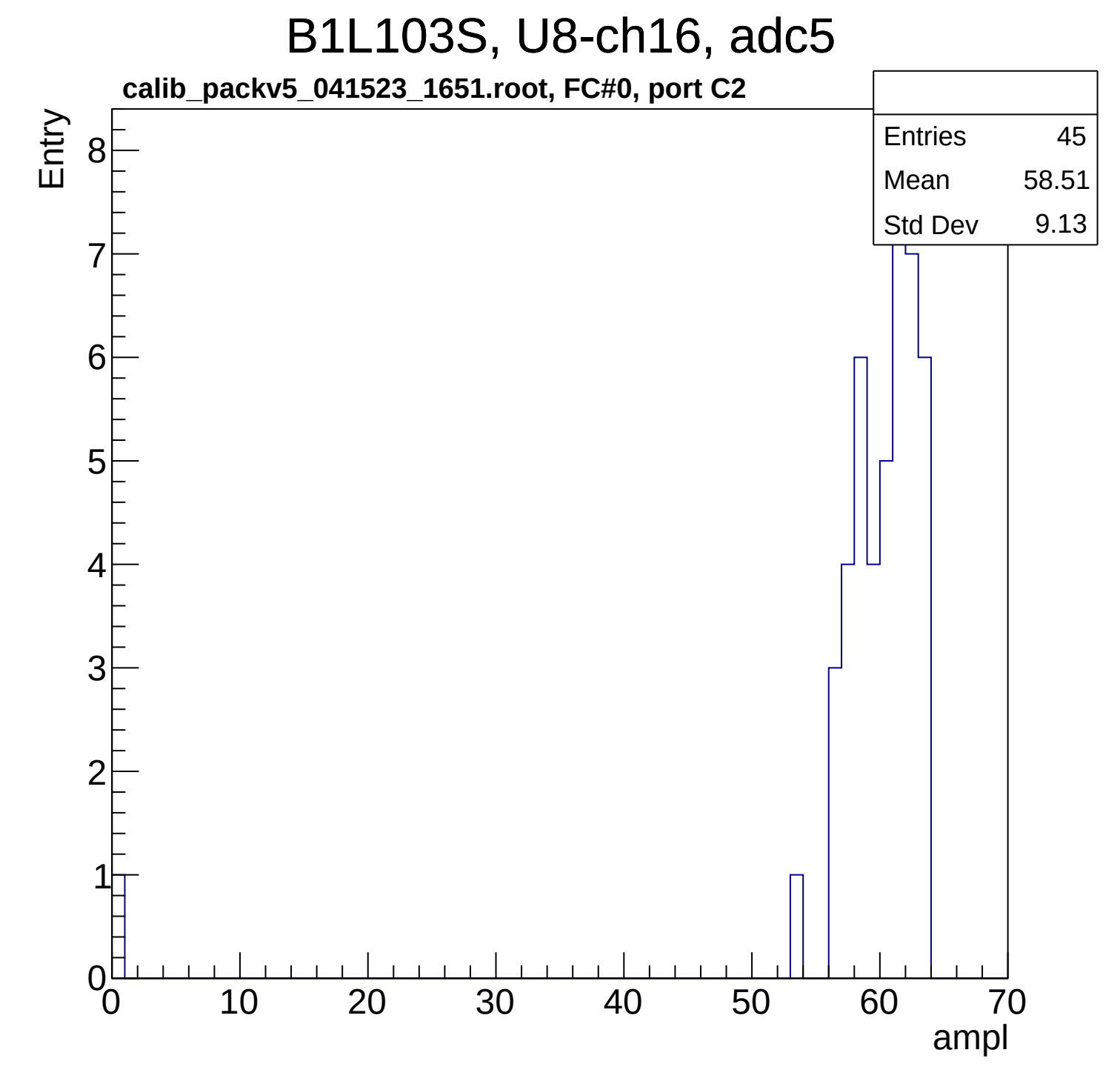
B1L103S, U8-ch16, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 58.51
Std Dev 9.13
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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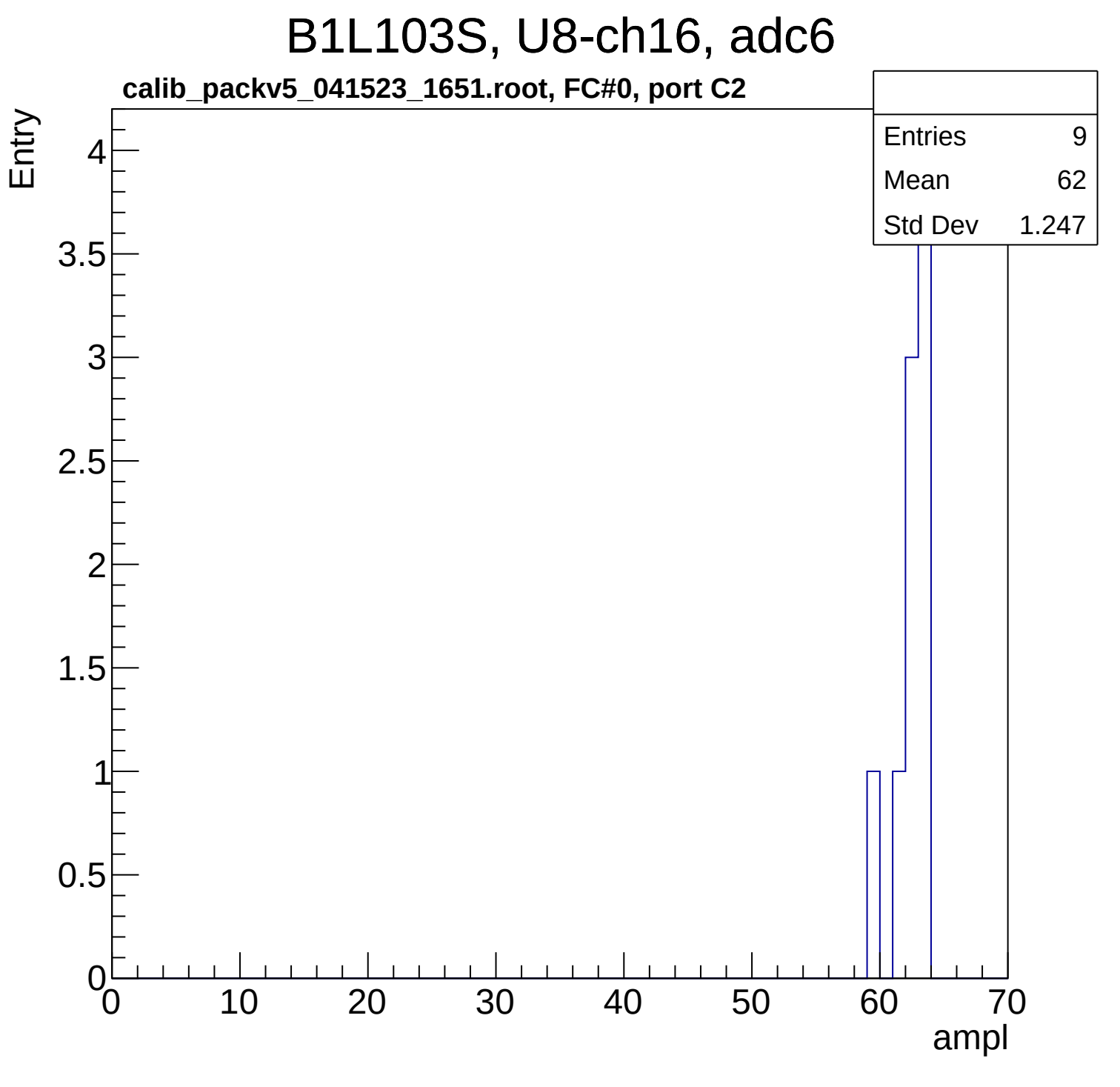
B1L103S, U8-ch16, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 62
Std Dev 1.247
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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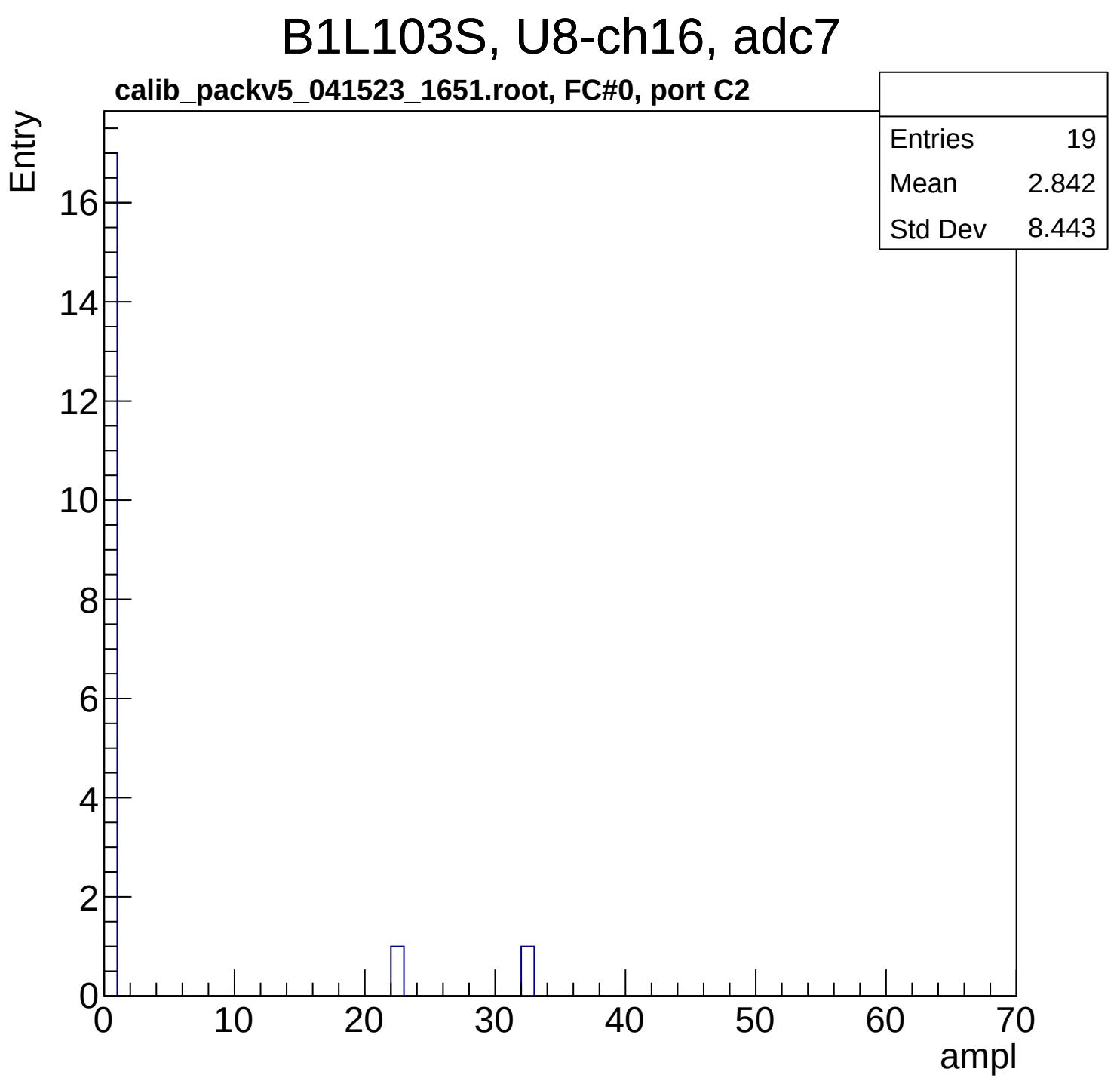
B1L103S, U8-ch16, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 2.842
Std Dev 8.443
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
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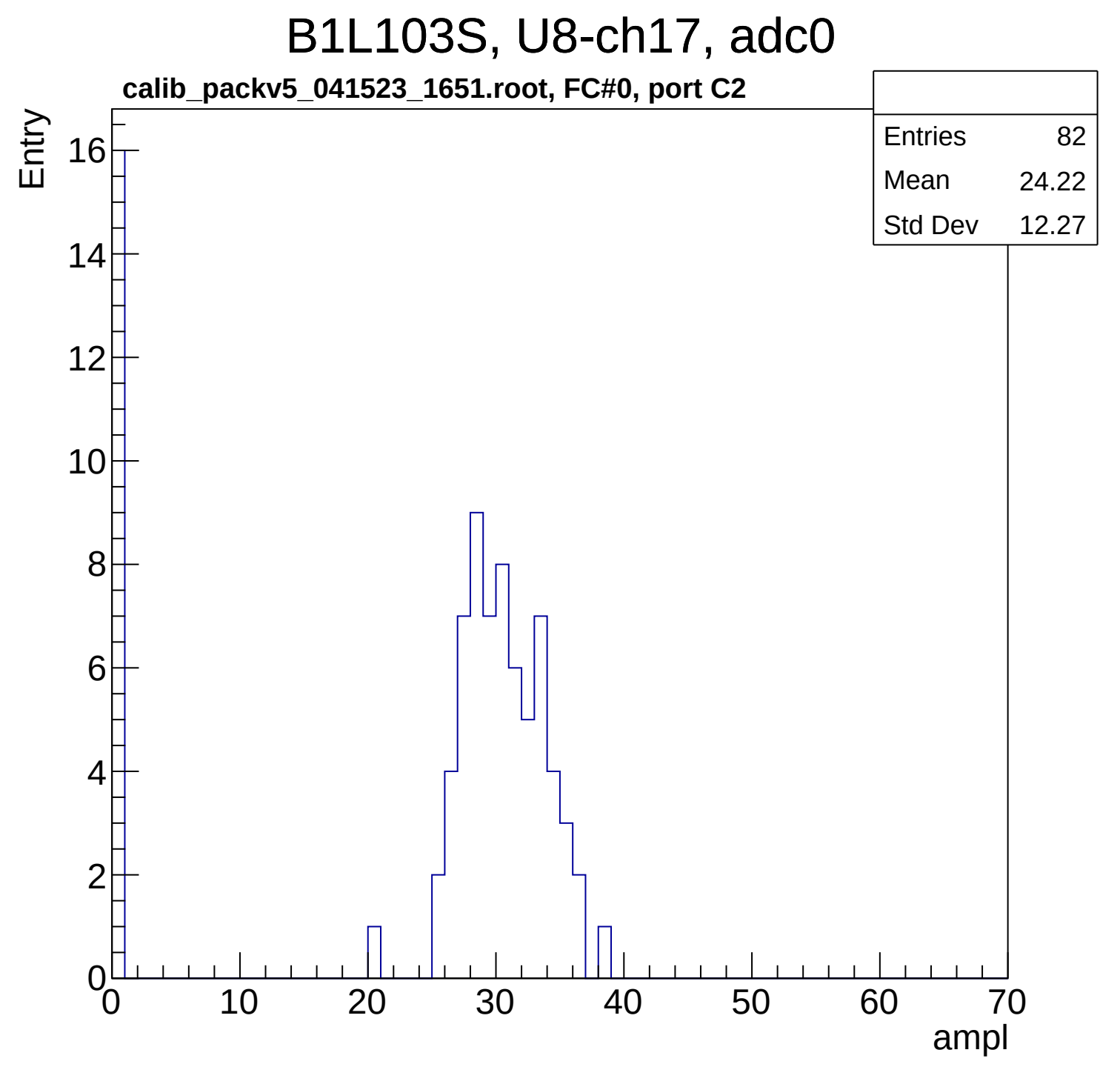
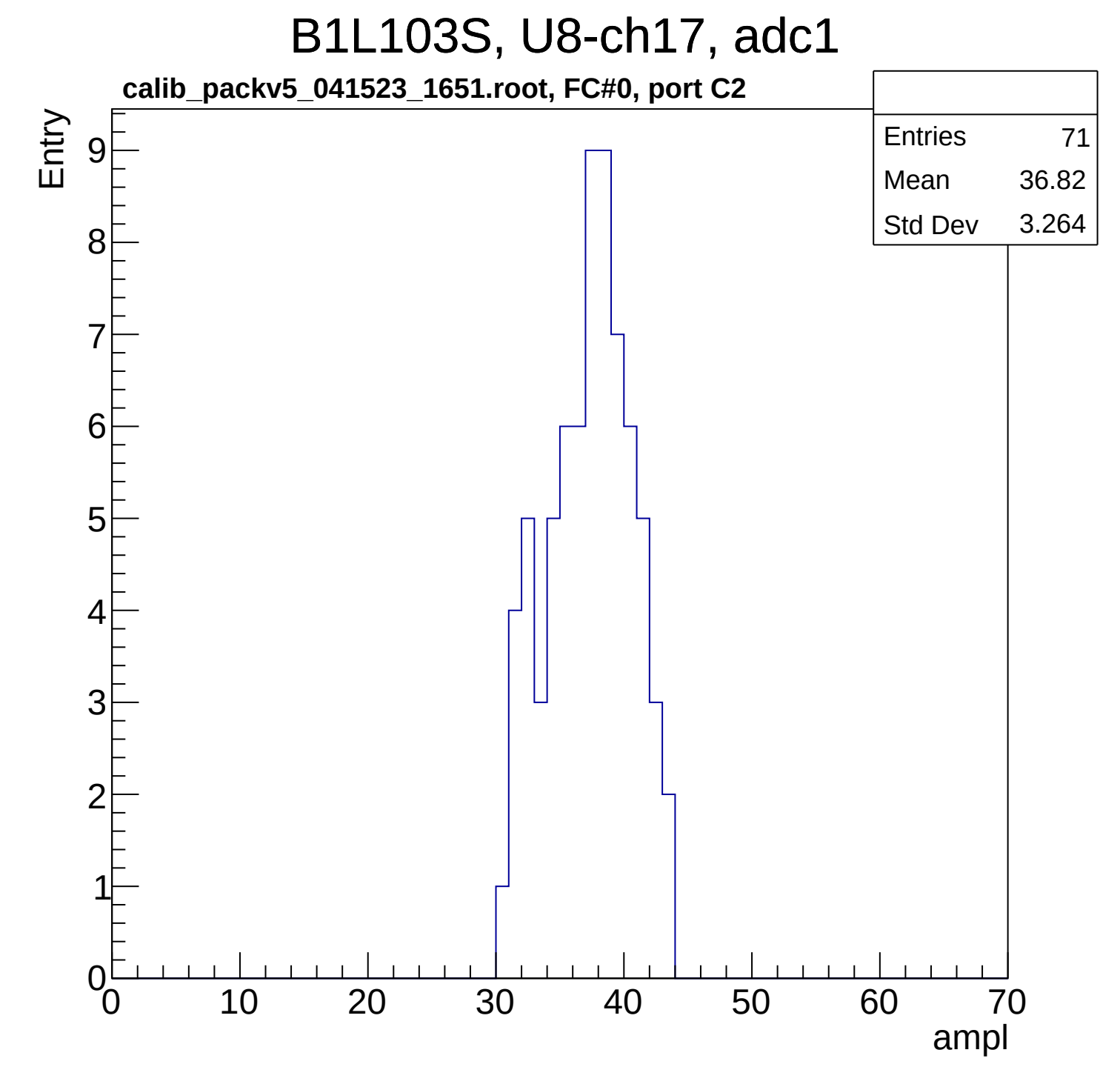
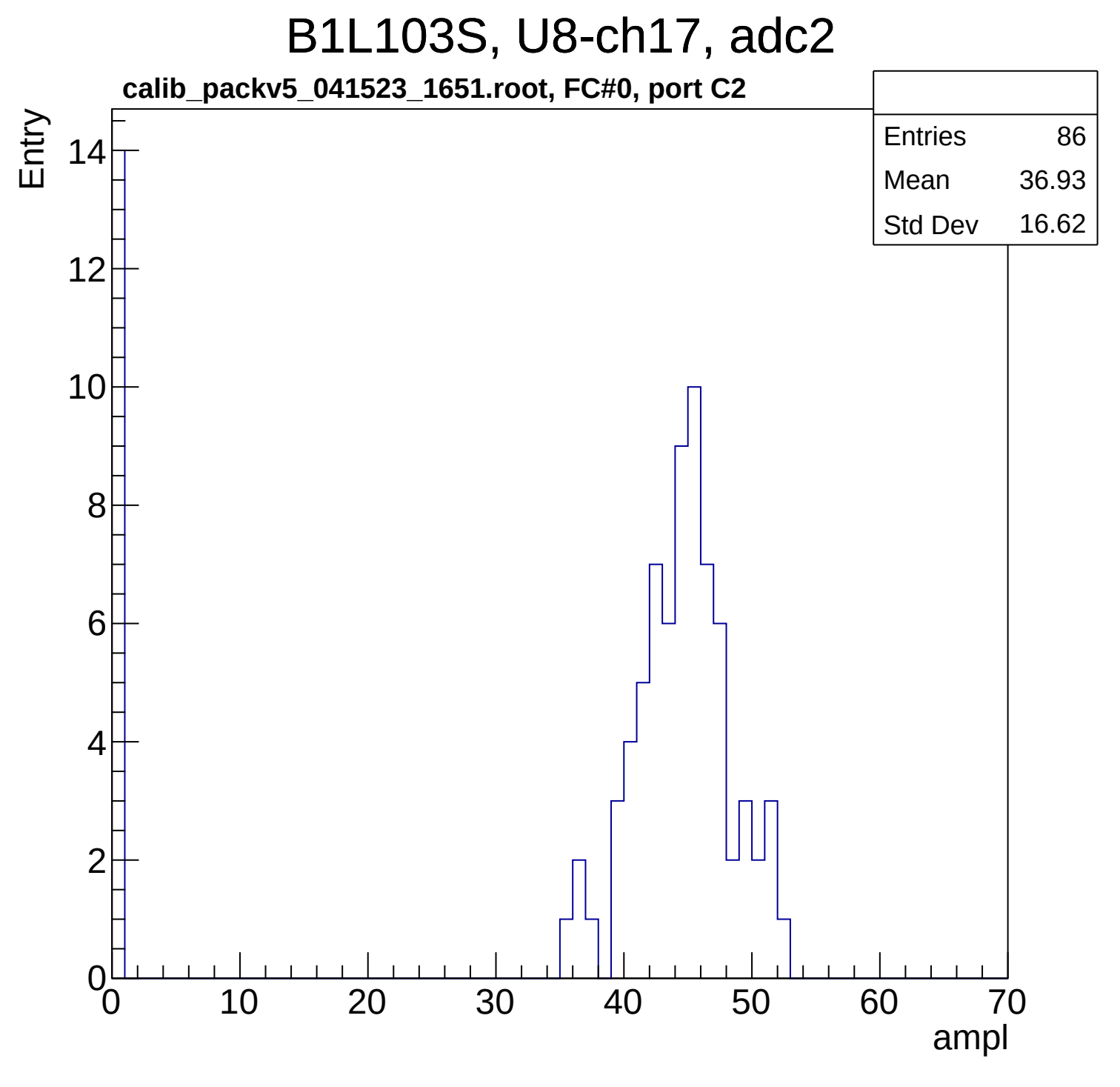
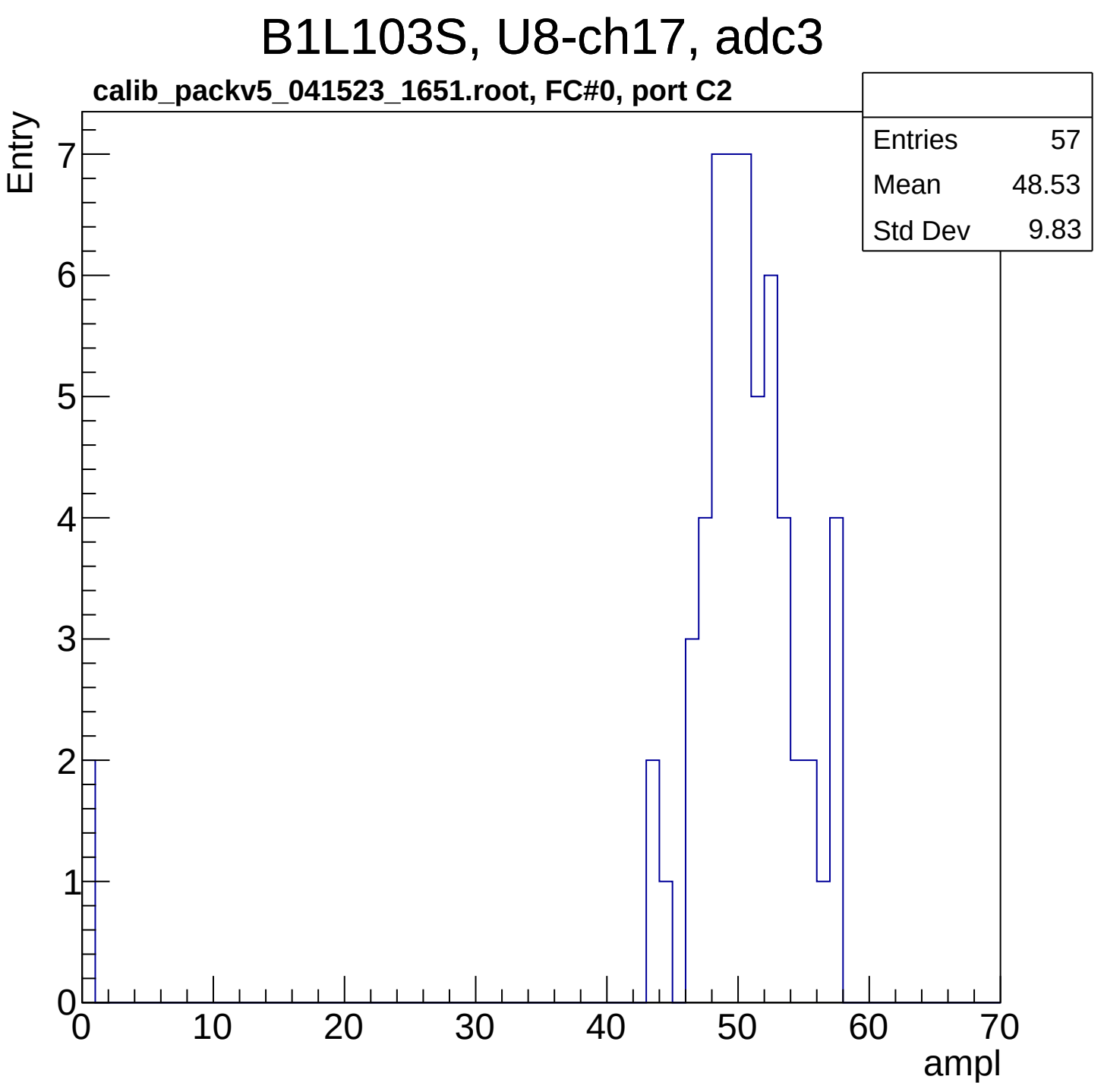
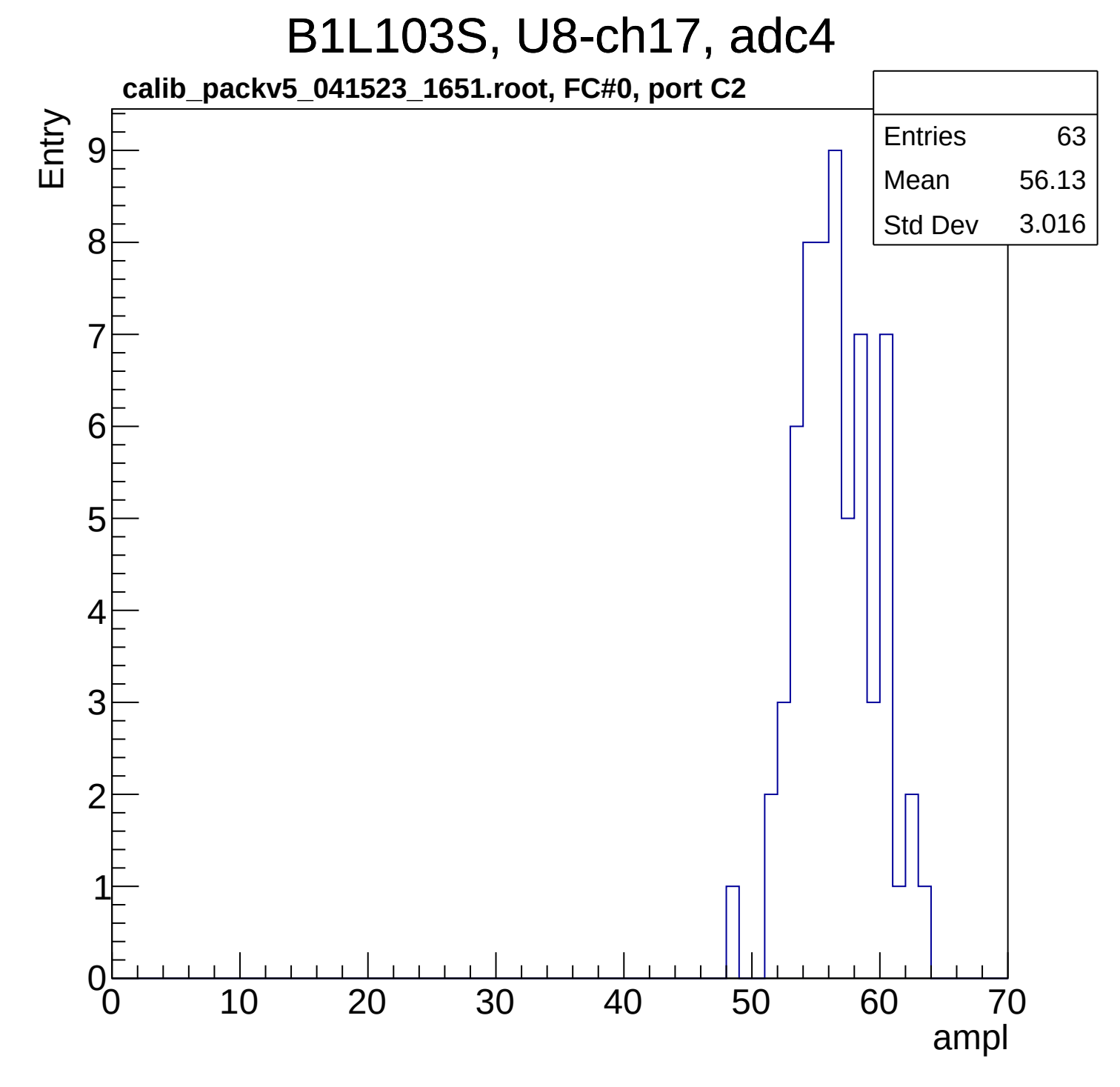
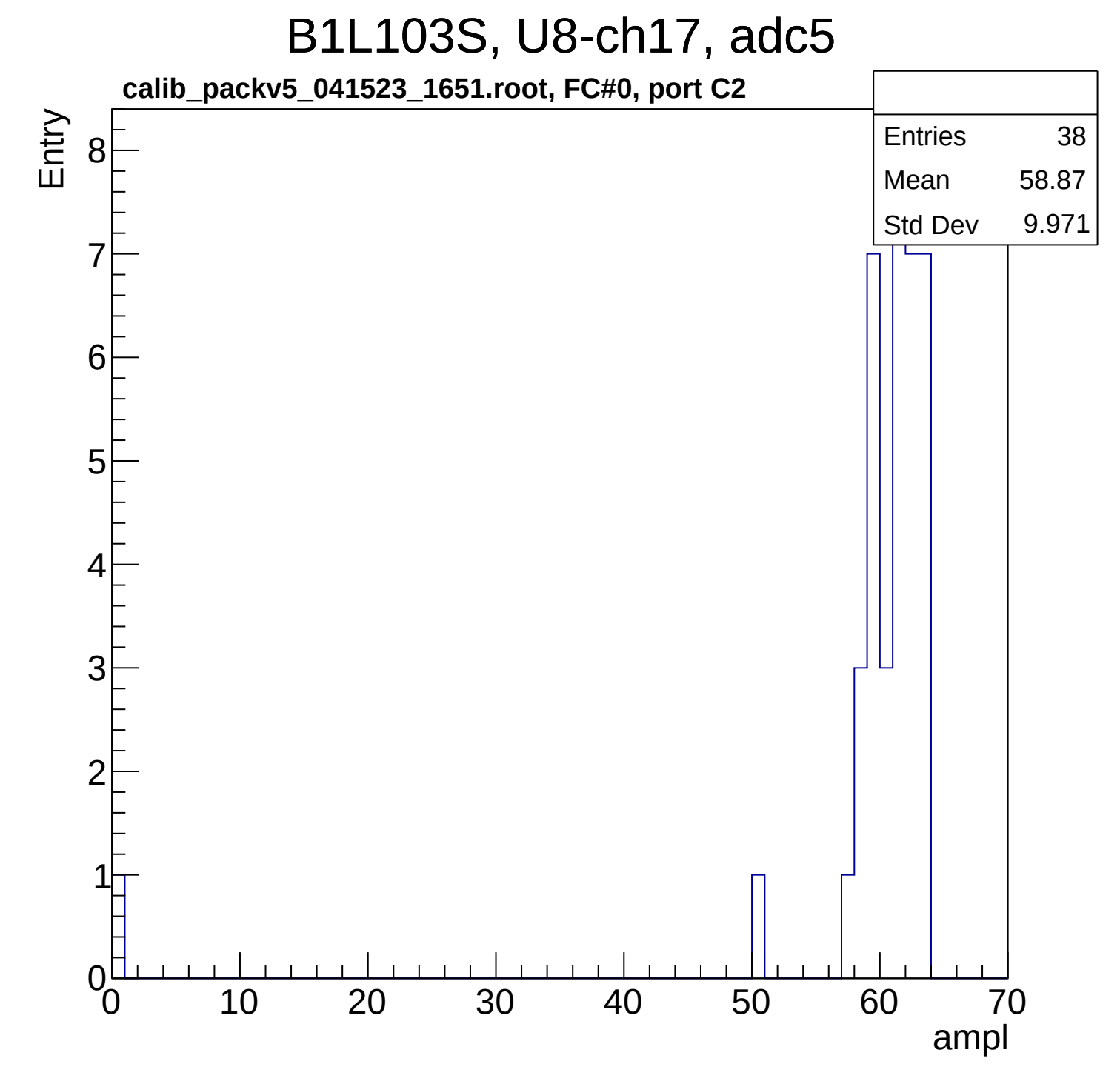

B1L103S, U8-ch17, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 24.22
Std Dev 12.27
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L103S, U8-ch17, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 36.82
Std Dev 3.264
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U8-ch17, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 36.93
Std Dev 16.62
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U8-ch17, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 48.53
Std Dev 9.83
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U8-ch17, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 56.13
Std Dev 3.016
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U8-ch17, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 58.87
Std Dev 9.971
Entry
ampl
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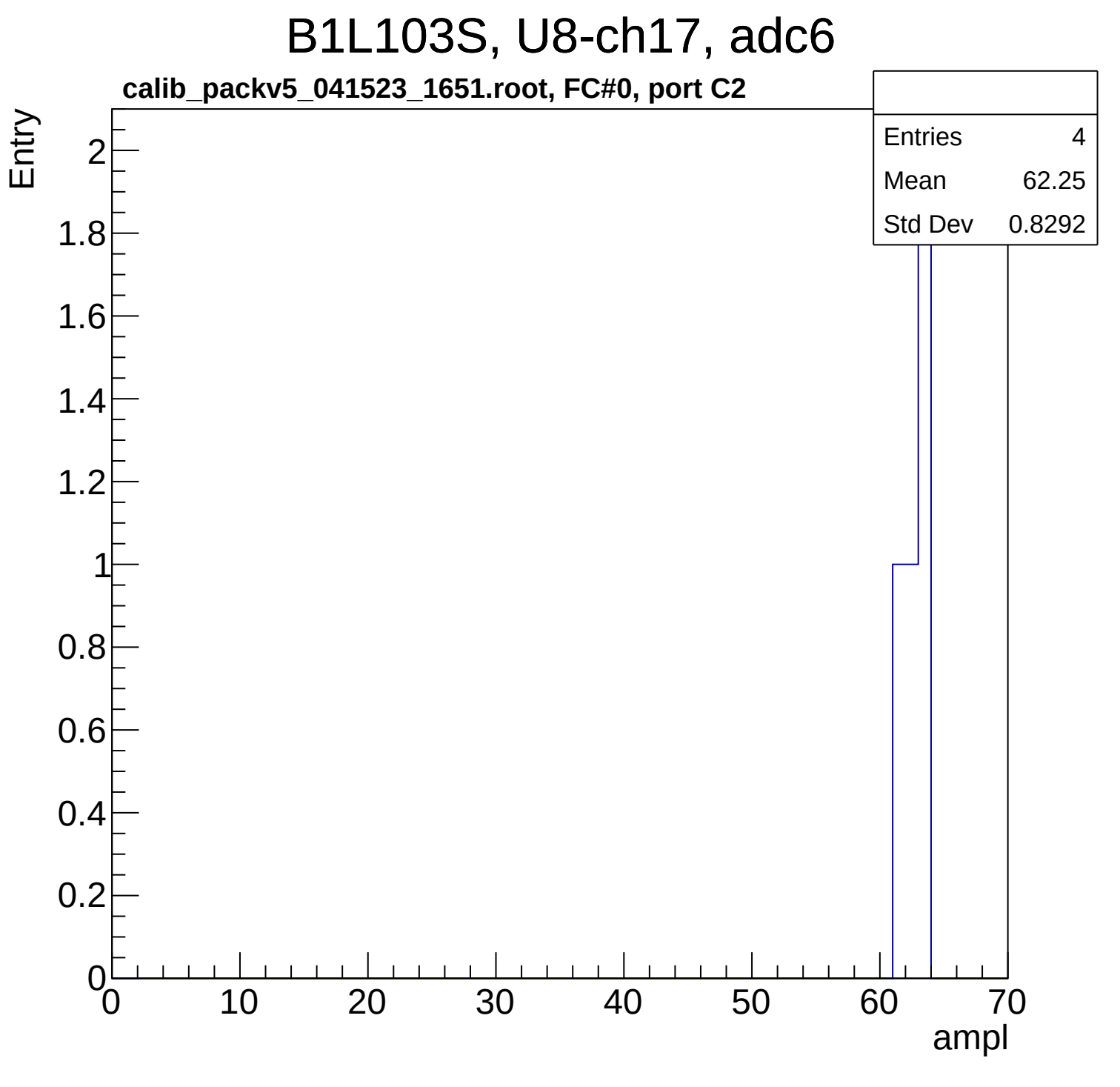
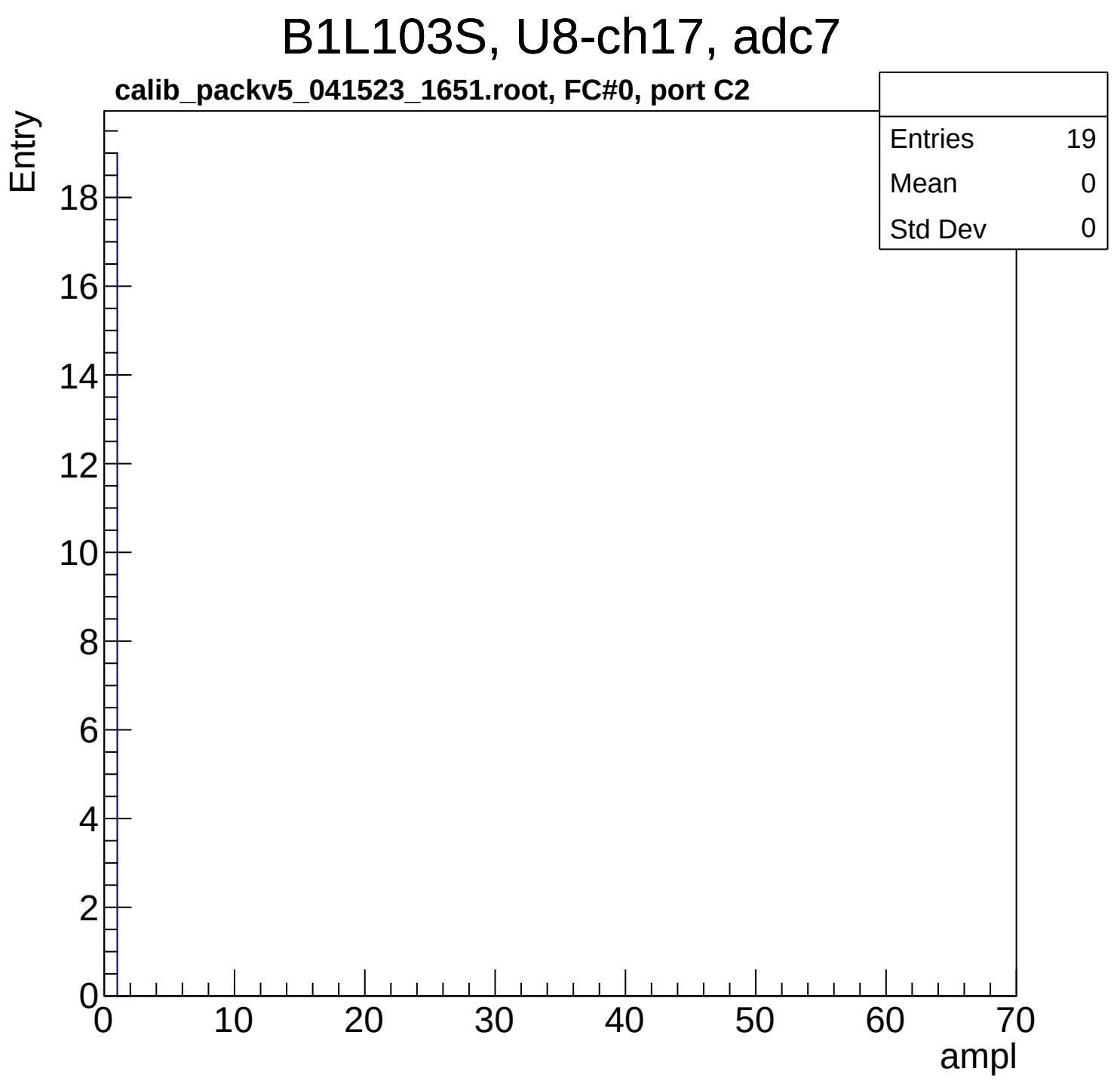
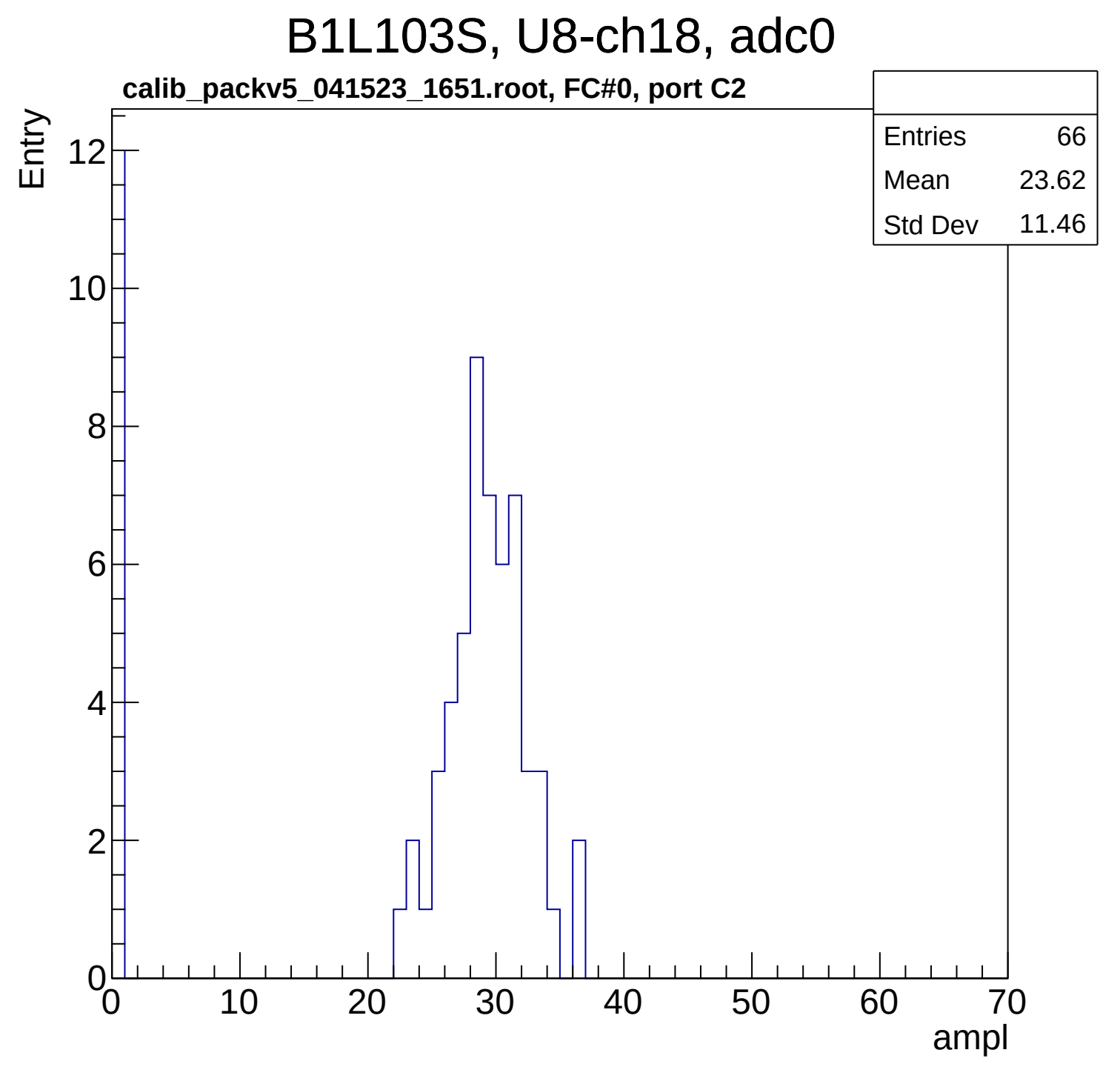
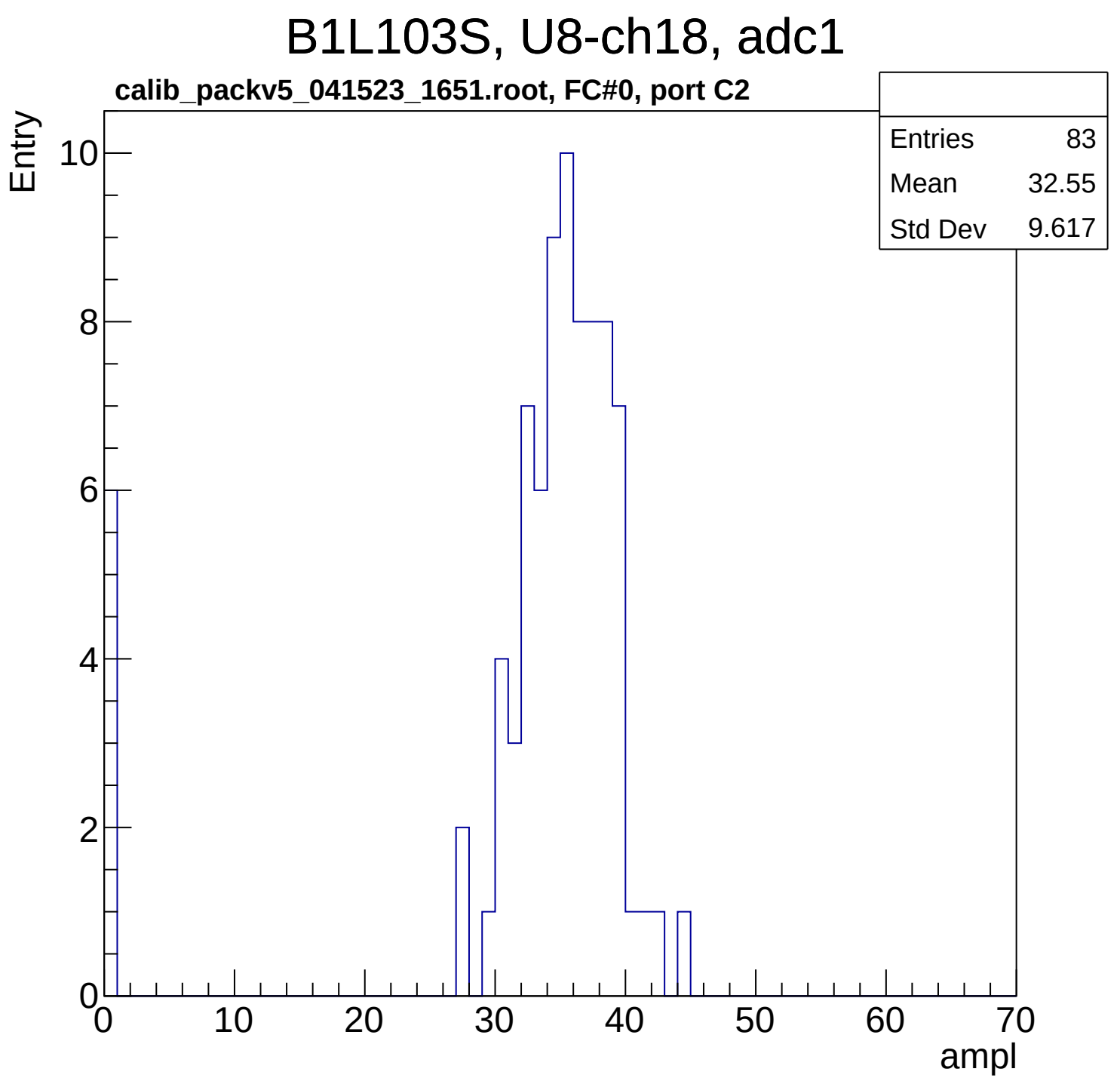
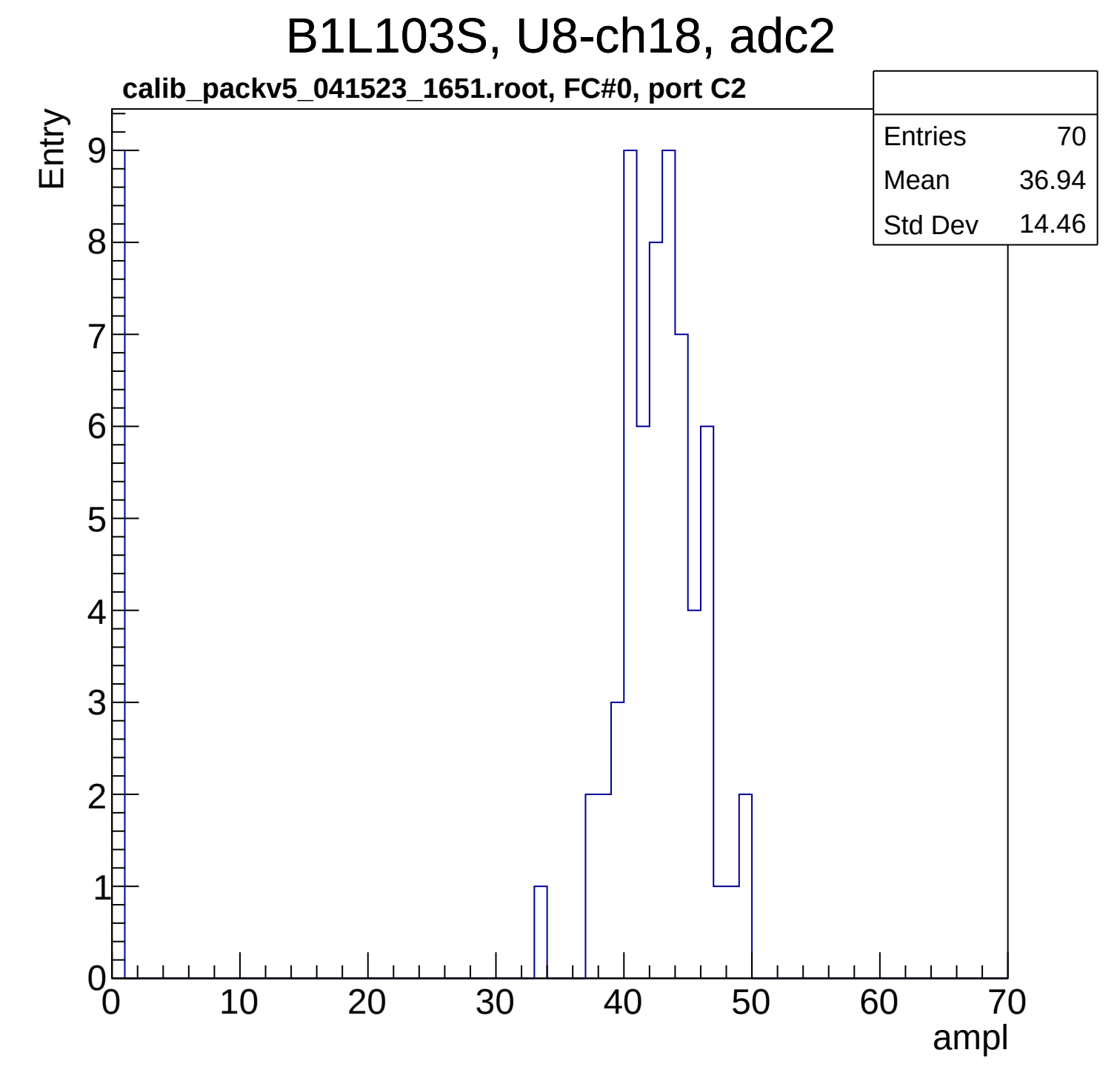
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

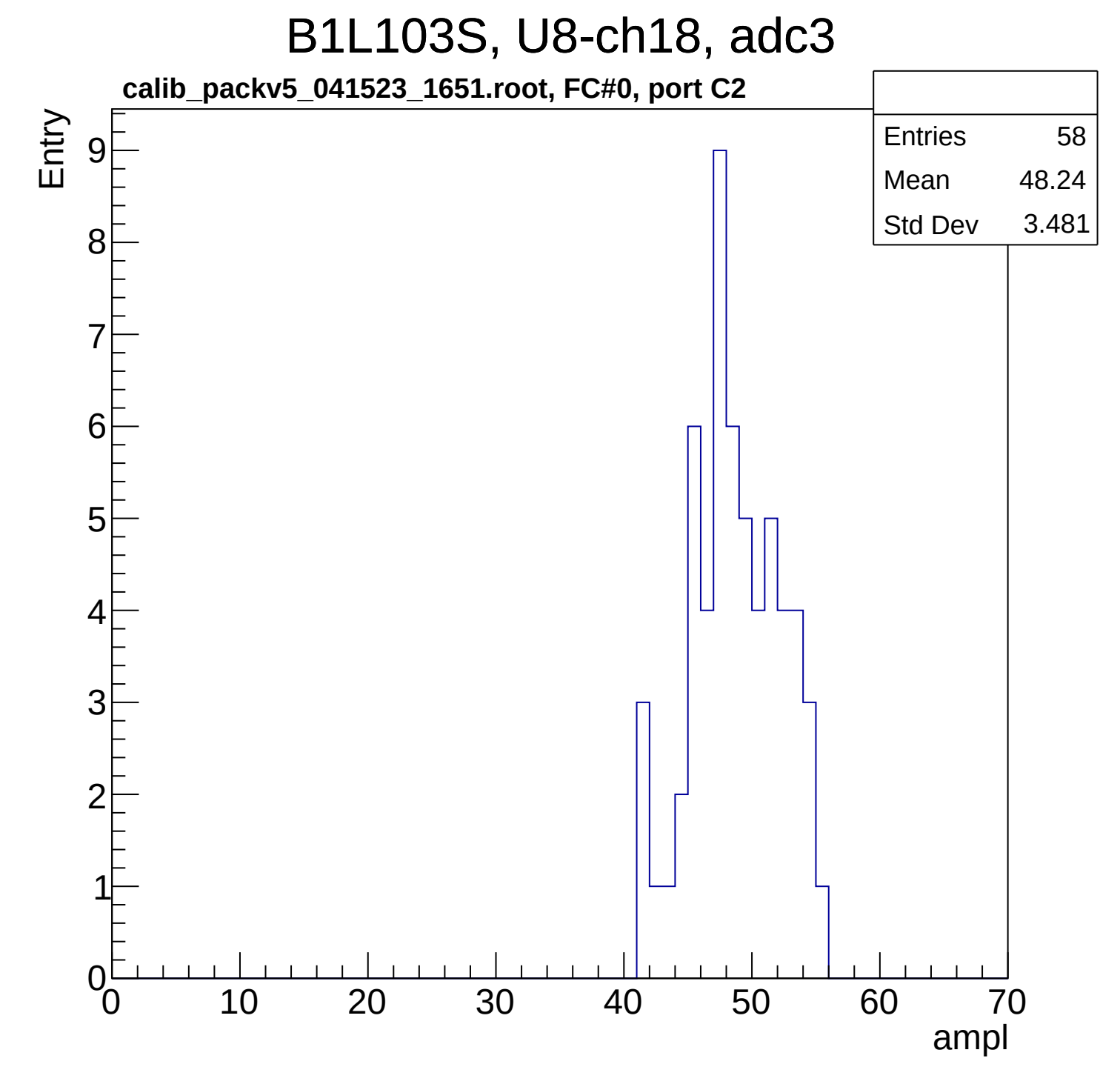

B1L103S, U8-ch17, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 62.25
Std Dev 0.8292
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U8-ch17, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch18, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 23.62
Std Dev 11.46
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U8-ch18, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 32.55
Std Dev 9.617
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch18, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 36.94
Std Dev 14.46
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U8-ch18, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 48.24
Std Dev 3.481
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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60
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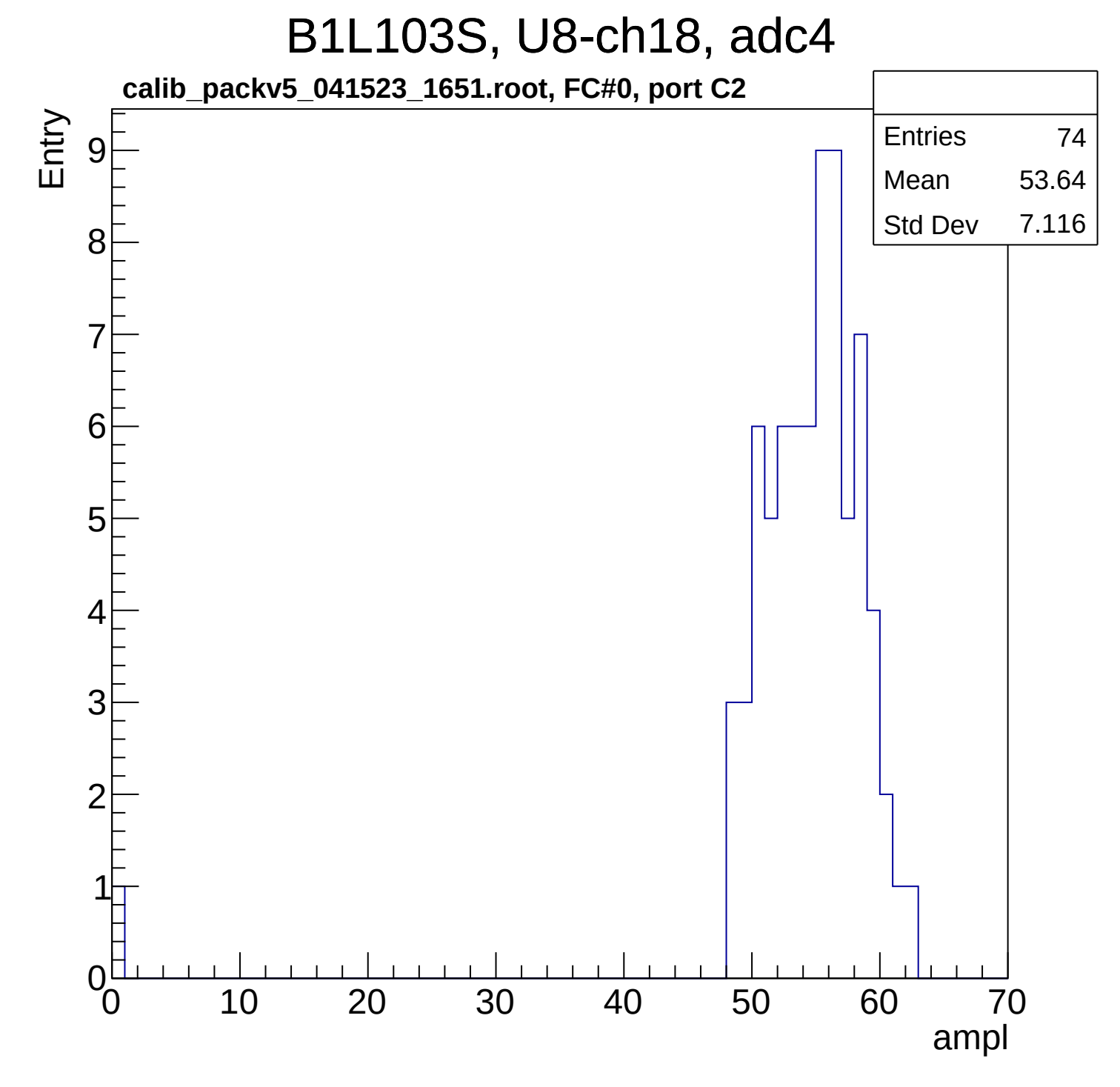
B1L103S, U8-ch18, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 53.64
Std Dev 7.116
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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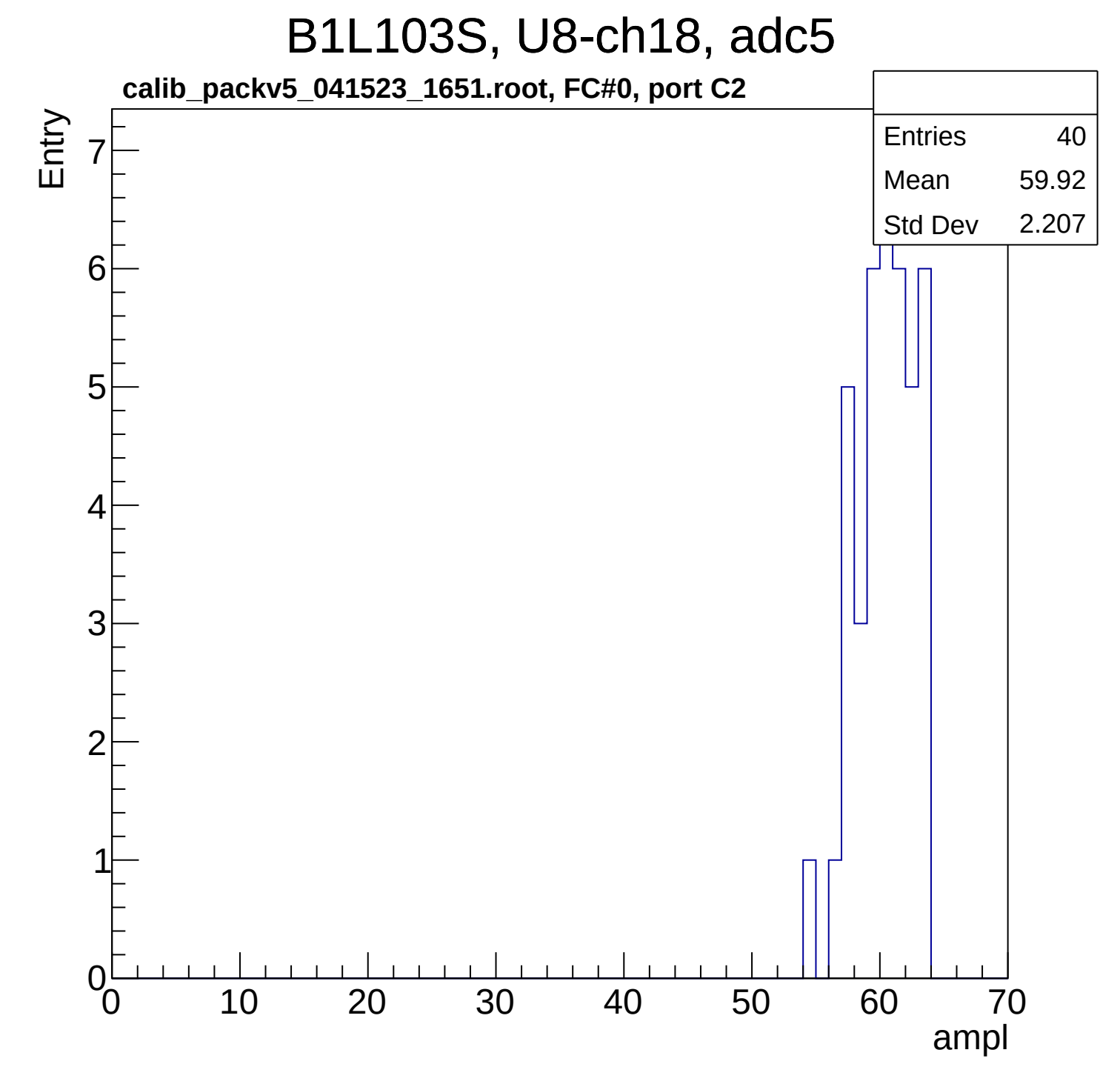
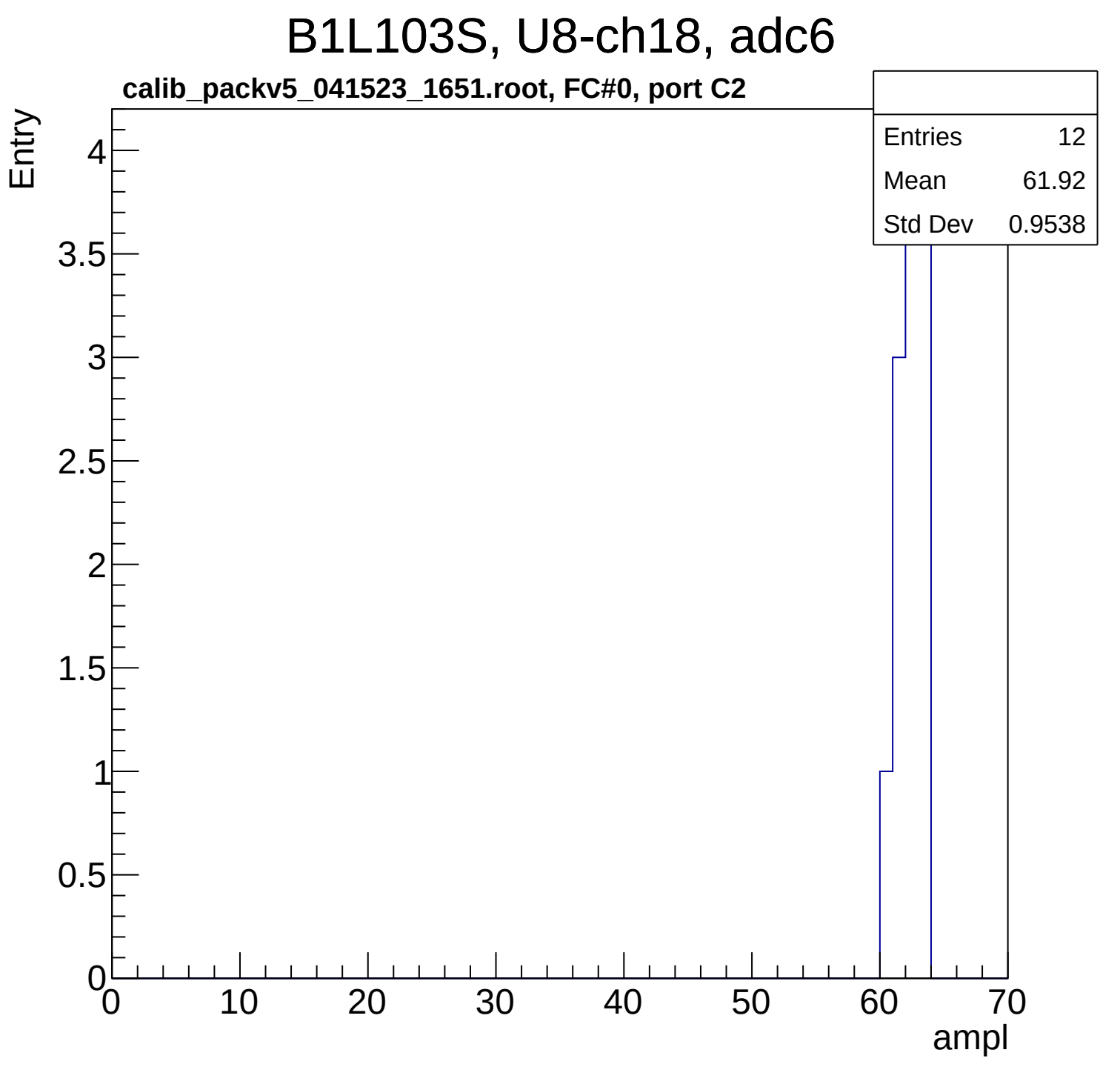

B1L103S, U8-ch18, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 59.92
Std Dev 2.207
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U8-ch18, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.92
Std Dev 0.9538
Entry
ampl
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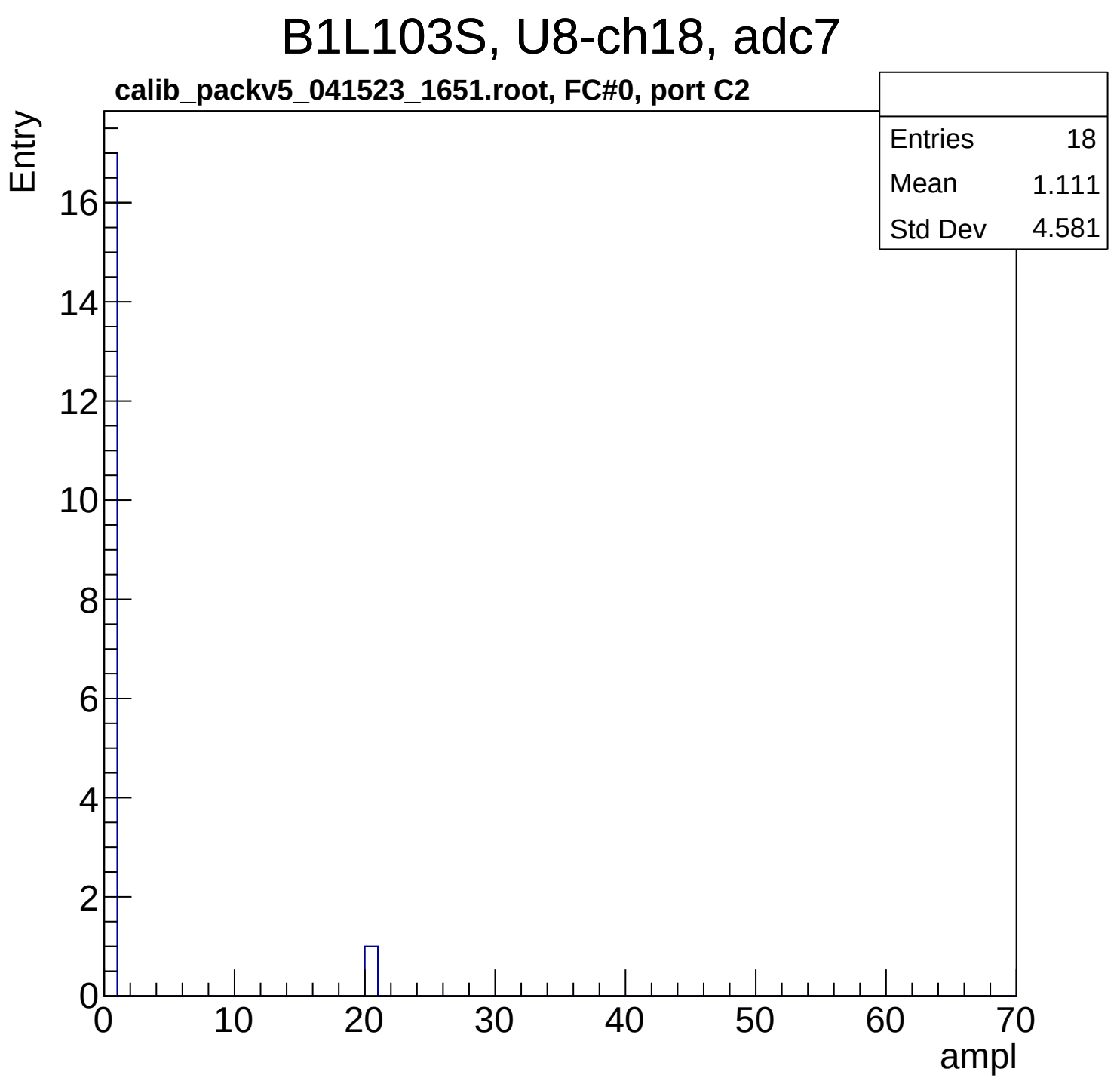
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U8-ch18, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.111
Std Dev 4.581
Entry
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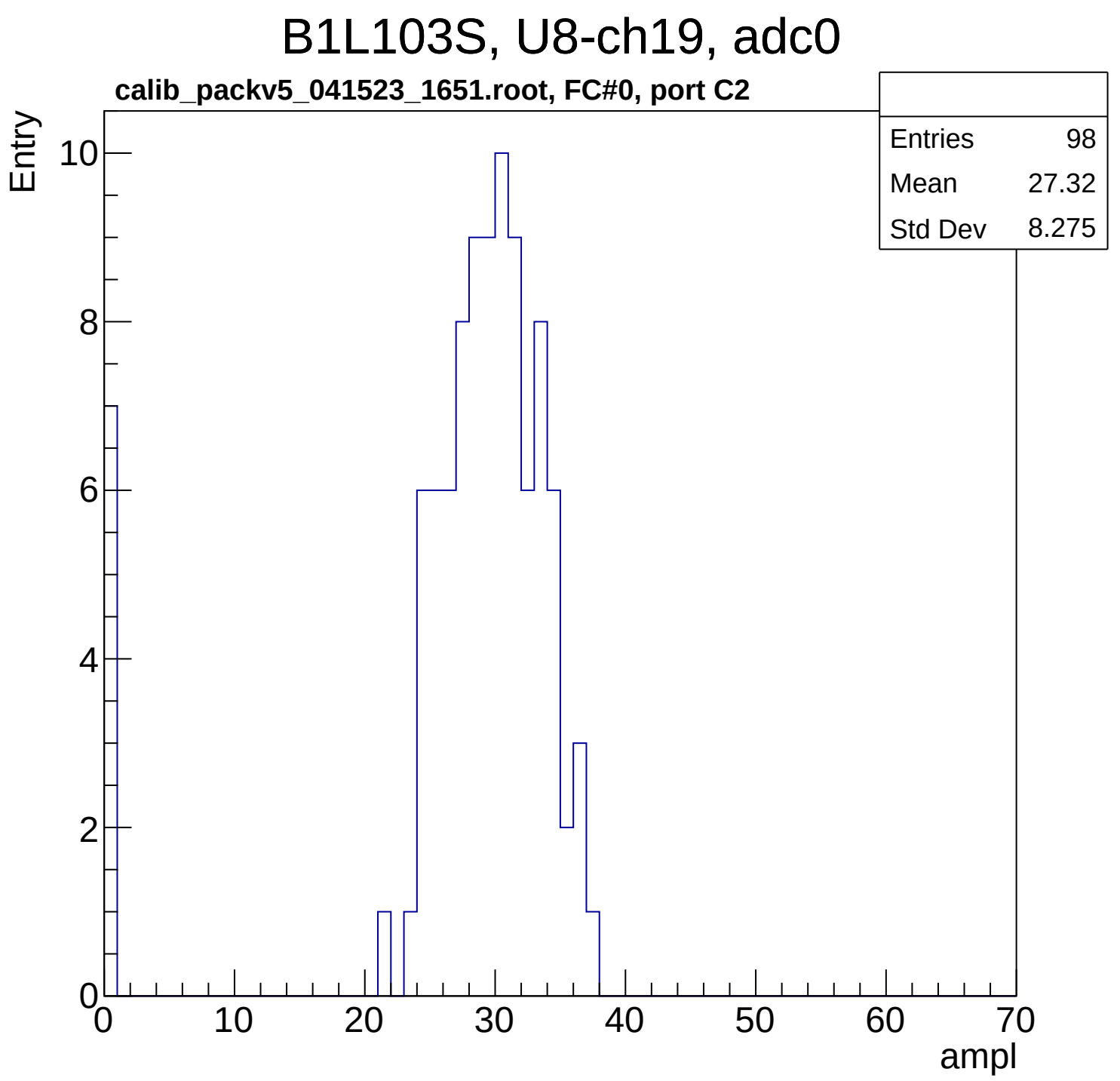
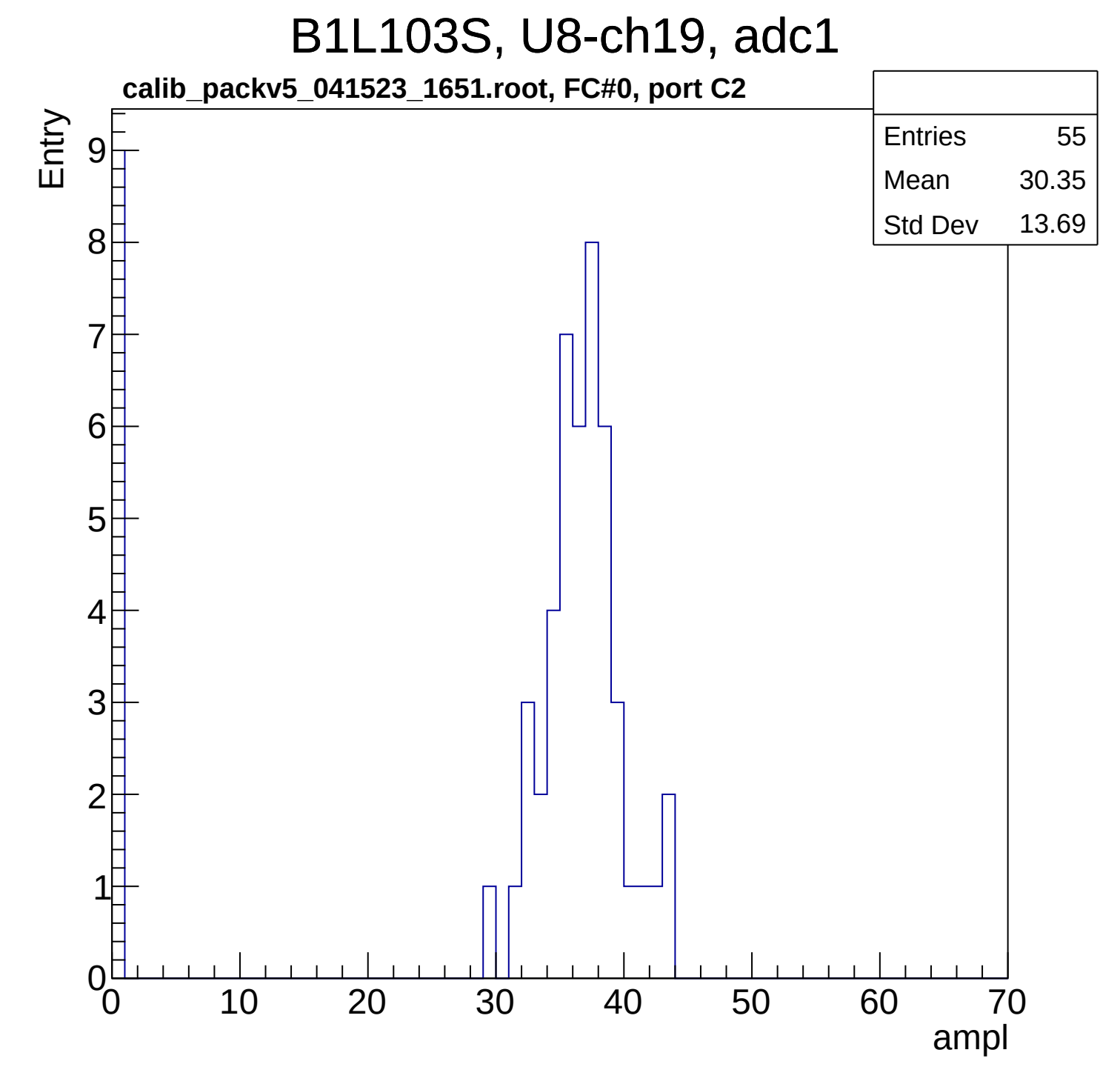
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch19, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 98
Mean 27.32
Std Dev 8.275
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U8-ch19, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 30.35
Std Dev 13.69
Entry
ampl
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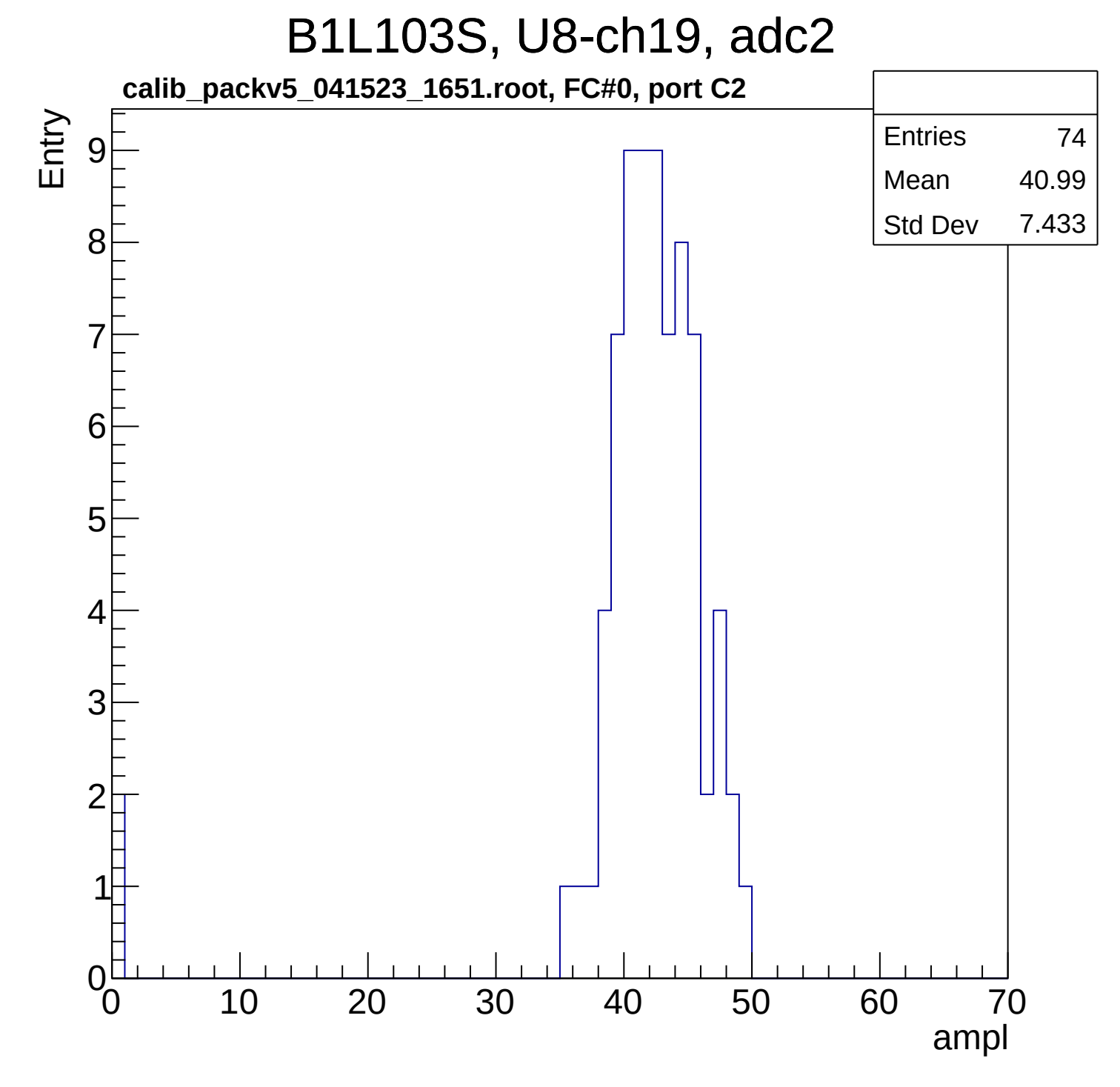
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U8-ch19, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 40.99
Std Dev 7.433
Entry
ampl
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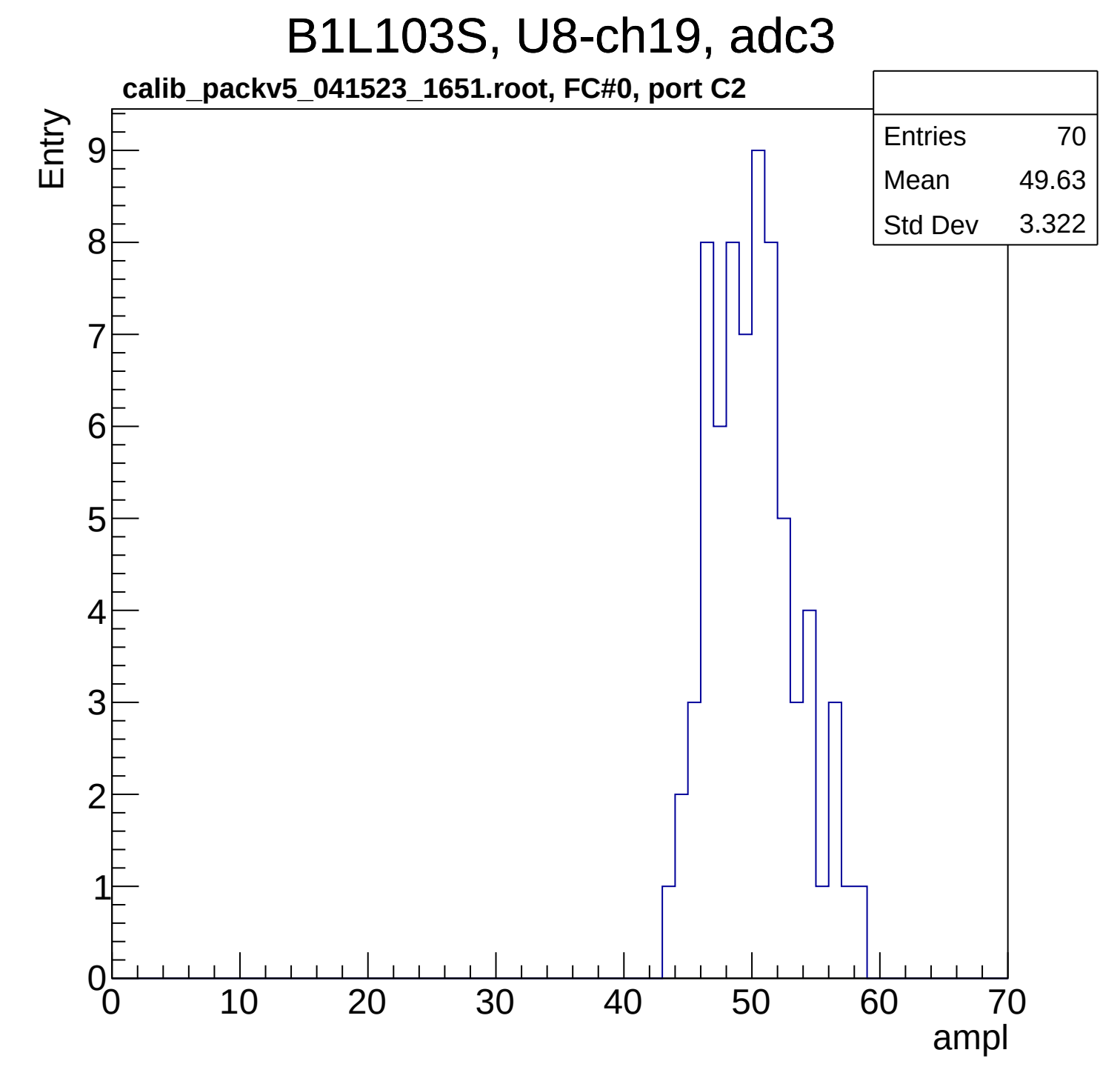
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U8-ch19, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 49.63
Std Dev 3.322
Entry
ampl
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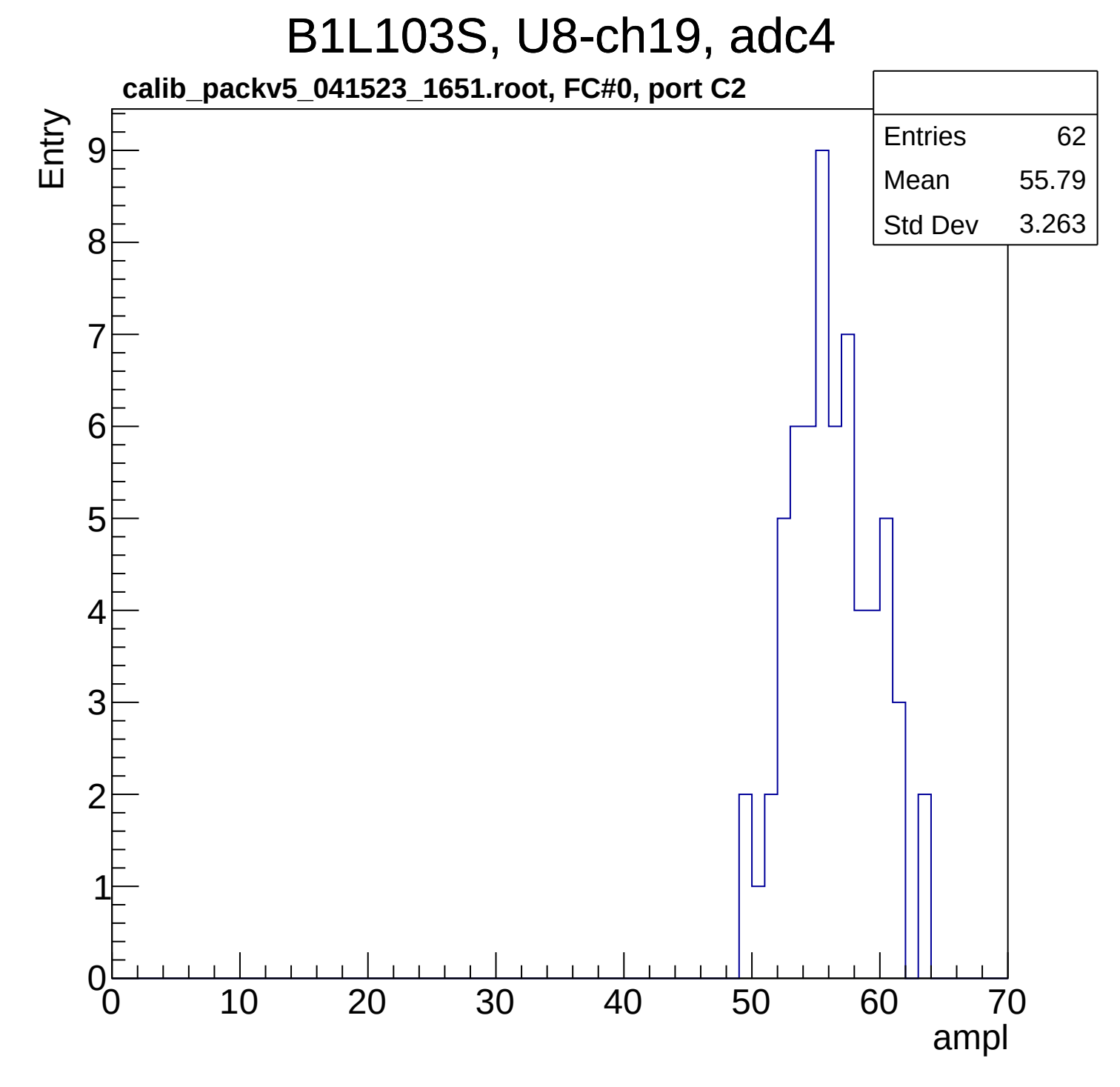
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U8-ch19, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 55.79
Std Dev 3.263
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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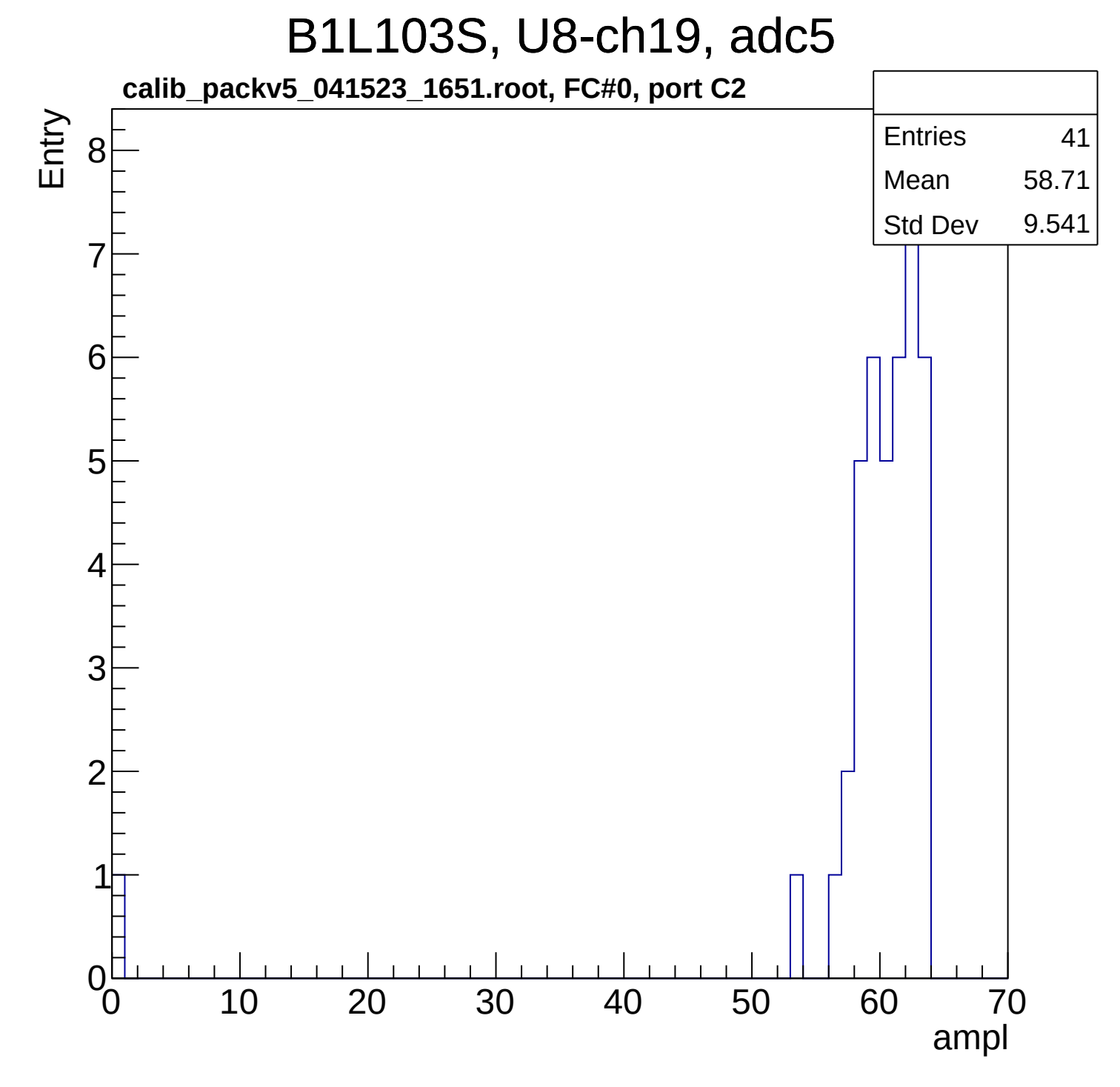
B1L103S, U8-ch19, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 58.71
Std Dev 9.541
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
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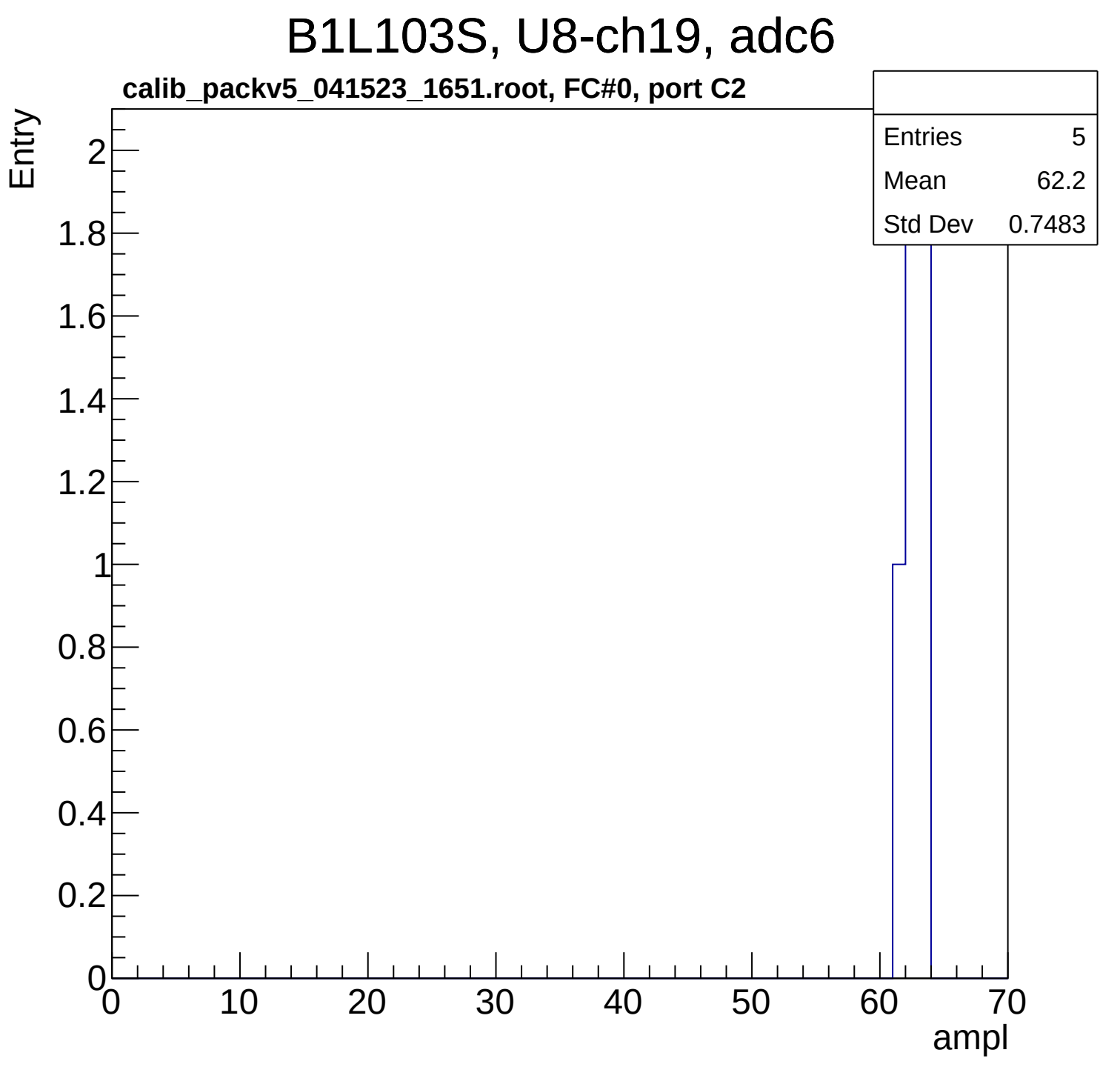
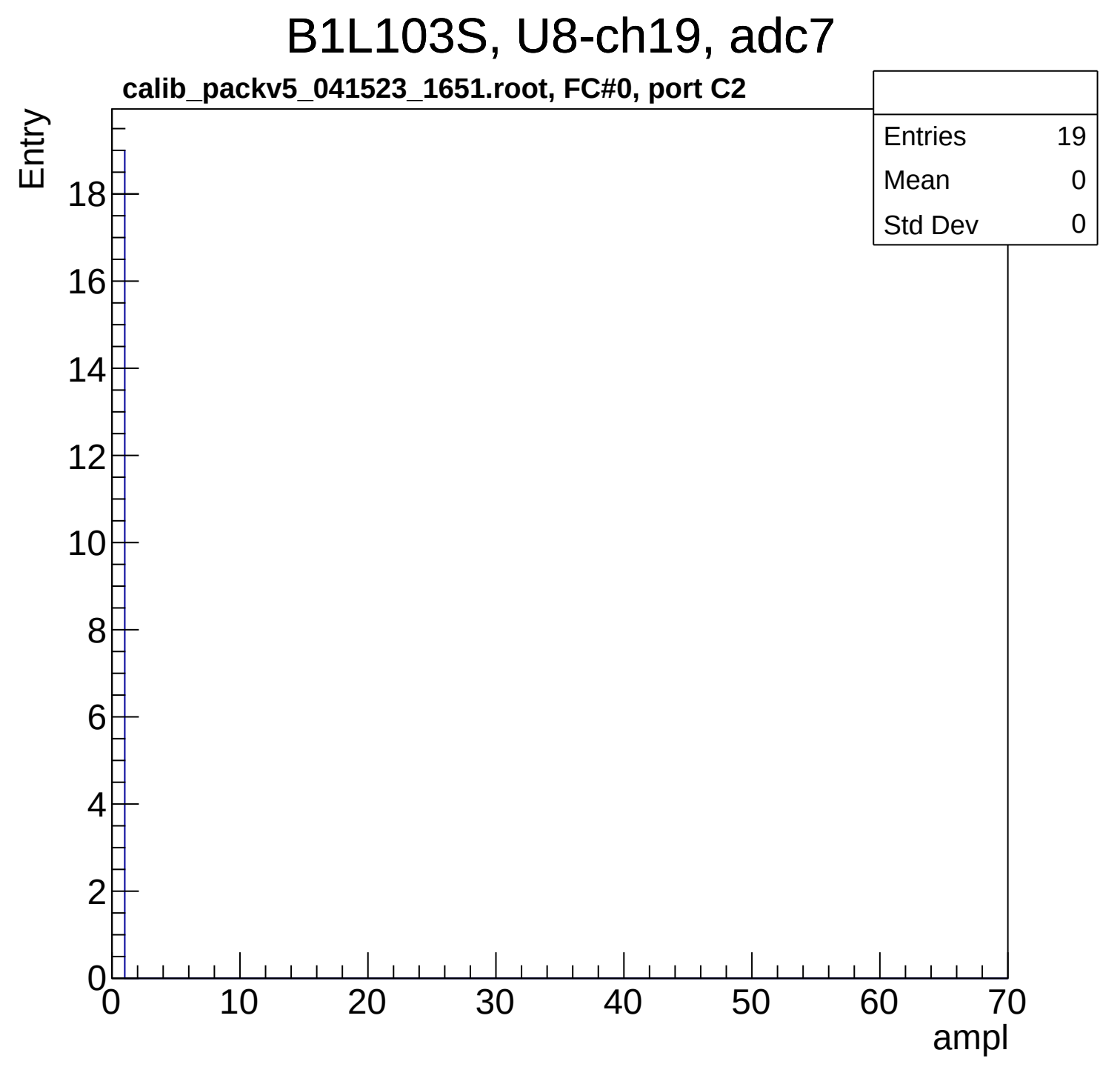
30
40
50
60
70


B1L103S, U8-ch19, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 62.2
Std Dev 0.7483
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U8-ch19, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
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18
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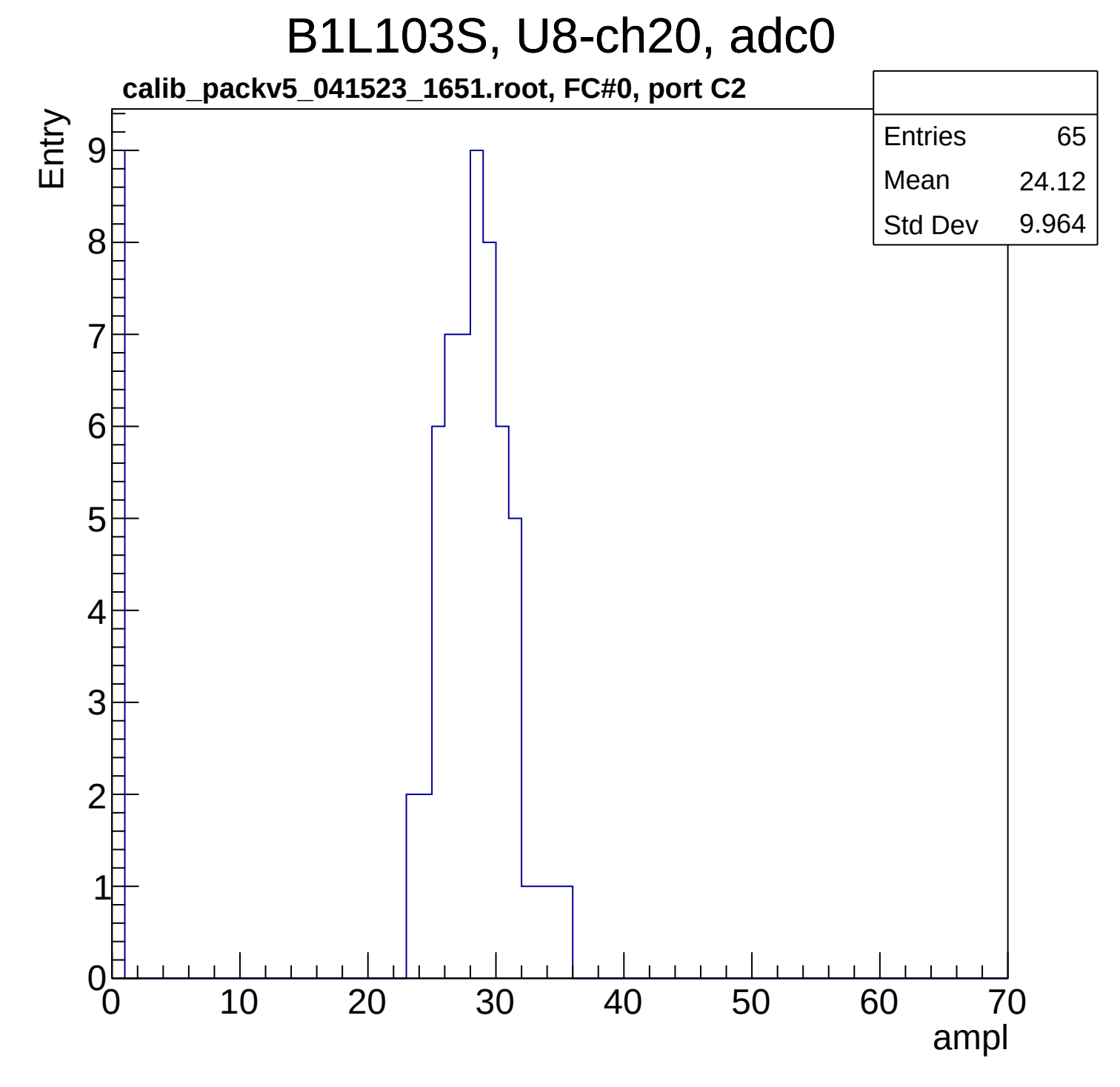
ampl


B1L103S, U8-ch20, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 24.12
Std Dev 9.964
Entry
ampl
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3
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0
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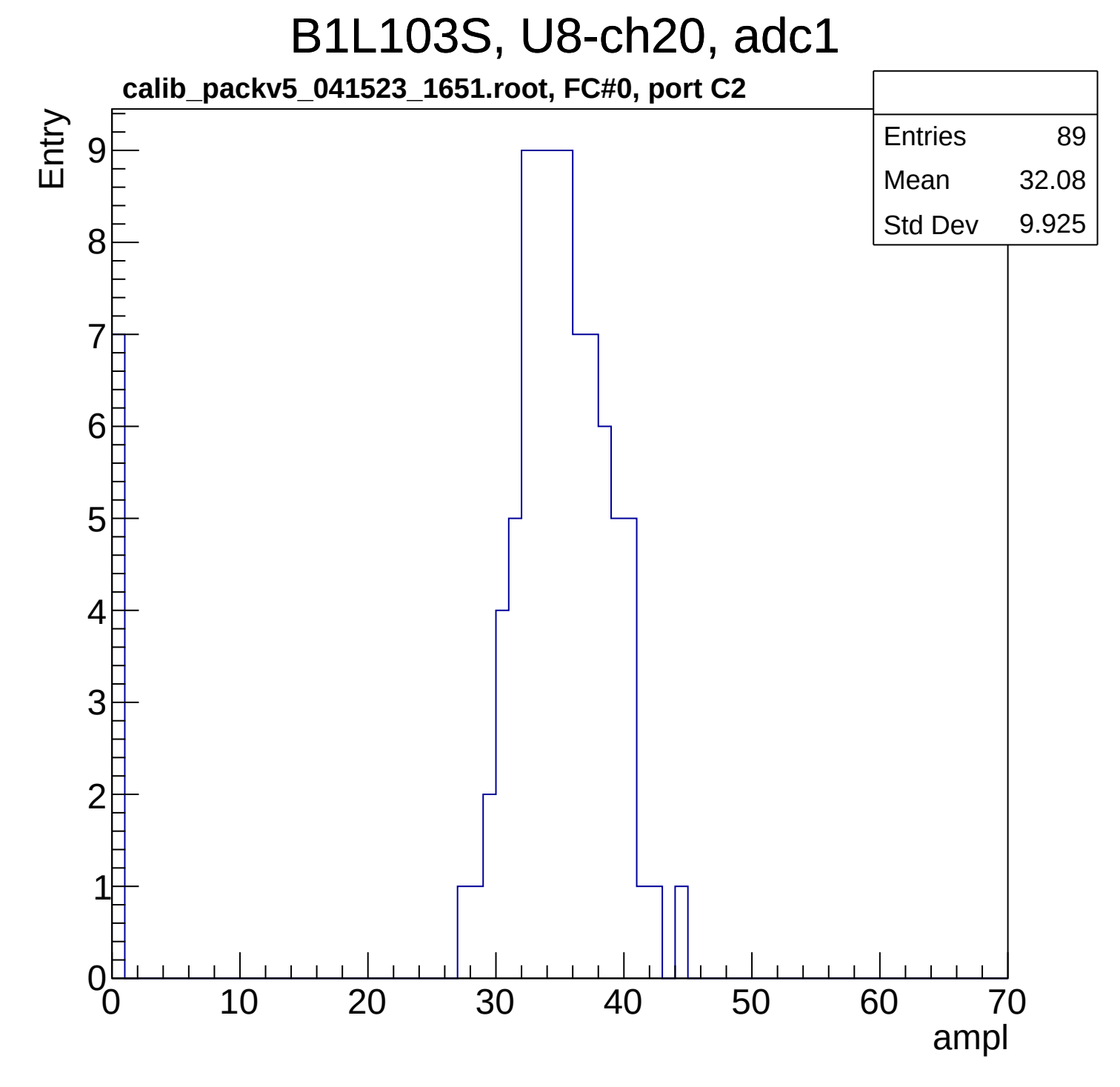
B1L103S, U8-ch20, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 32.08
Std Dev 9.925
Entry
ampl
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3
4
5
6
7
8
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0
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20
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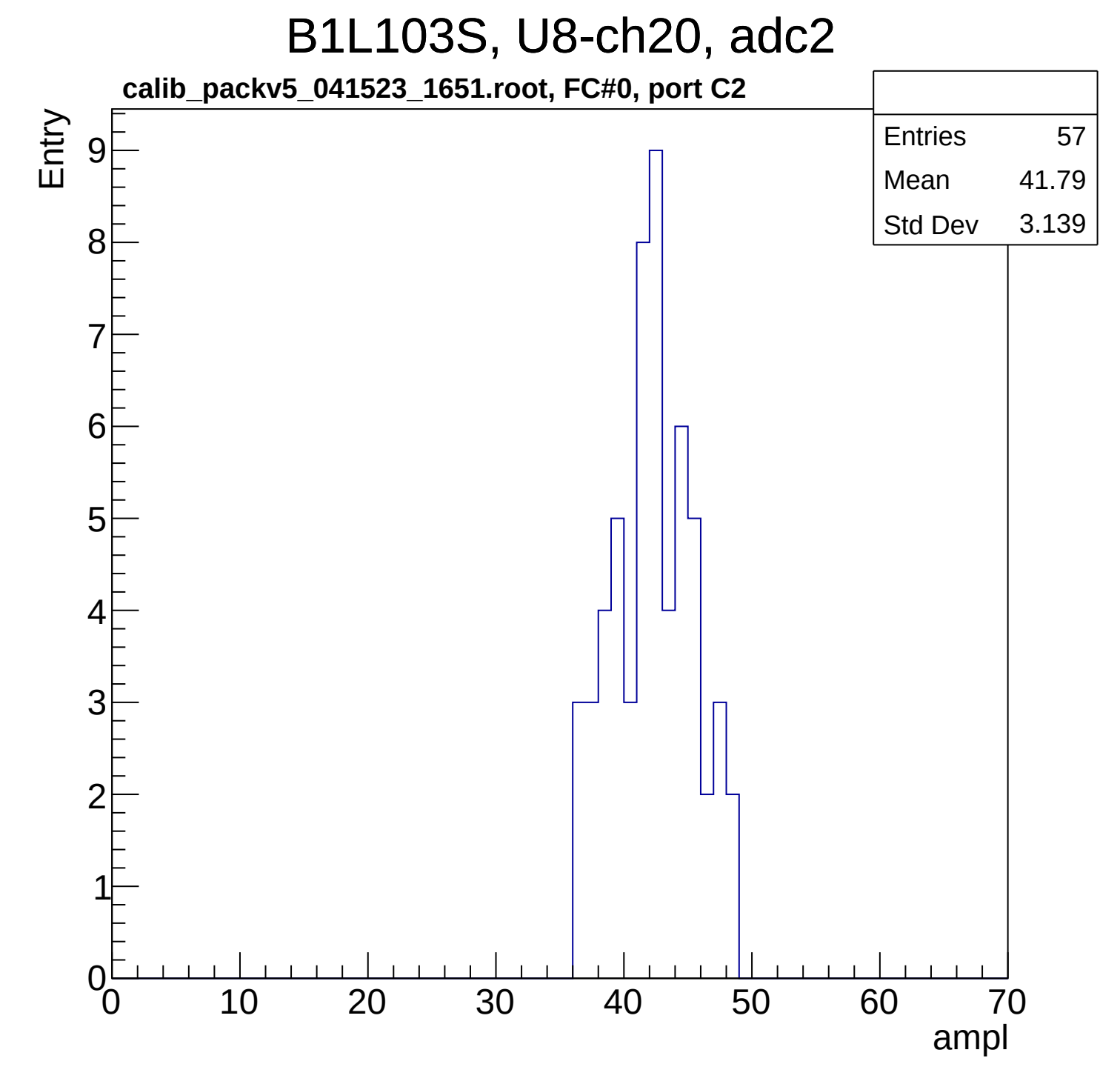
B1L103S, U8-ch20, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 41.79
Std Dev 3.139
Entry
ampl
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2
3
4
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6
7
8
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0
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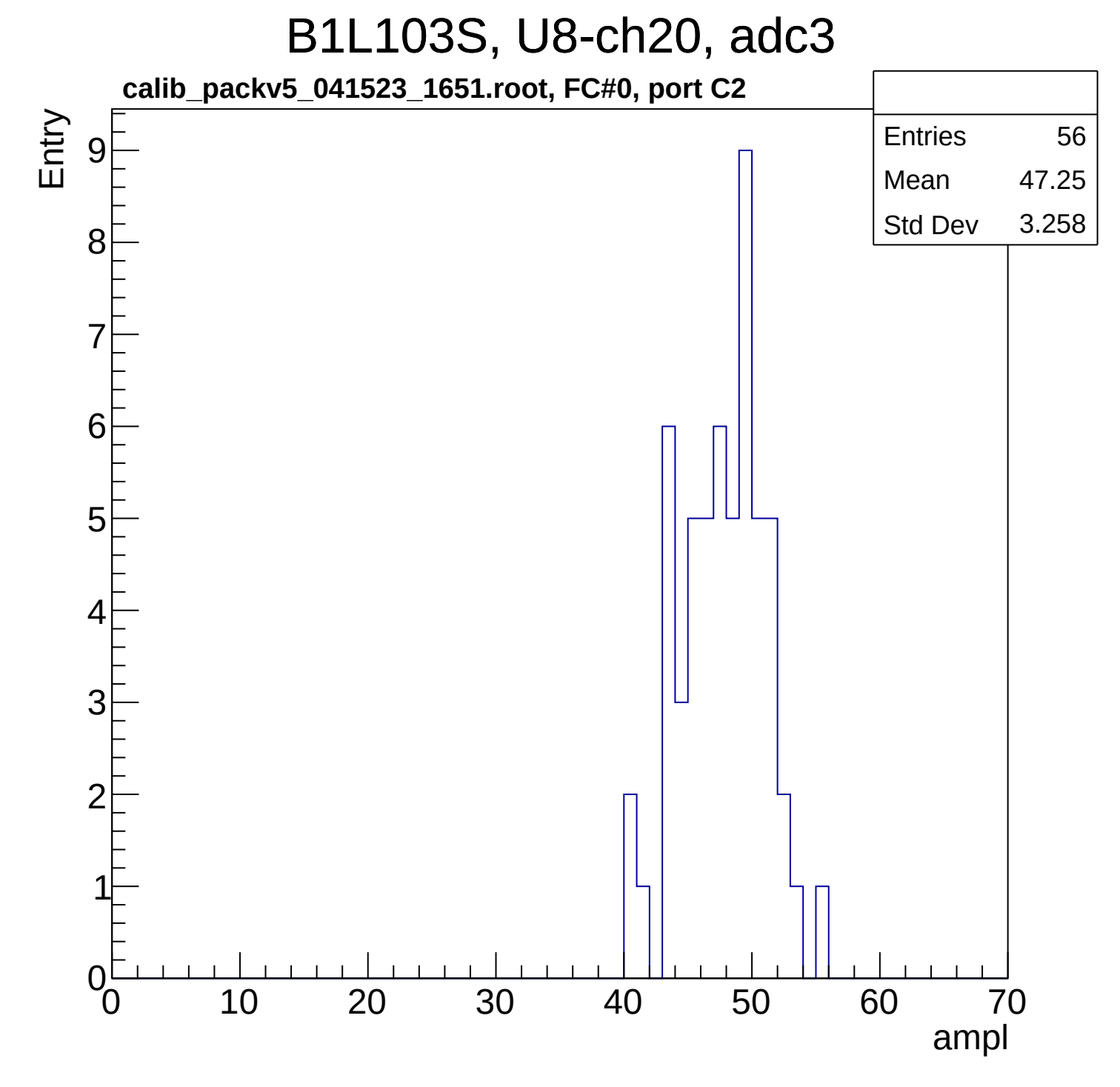
B1L103S, U8-ch20, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 47.25
Std Dev 3.258
Entry
ampl
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3
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6
7
8
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0
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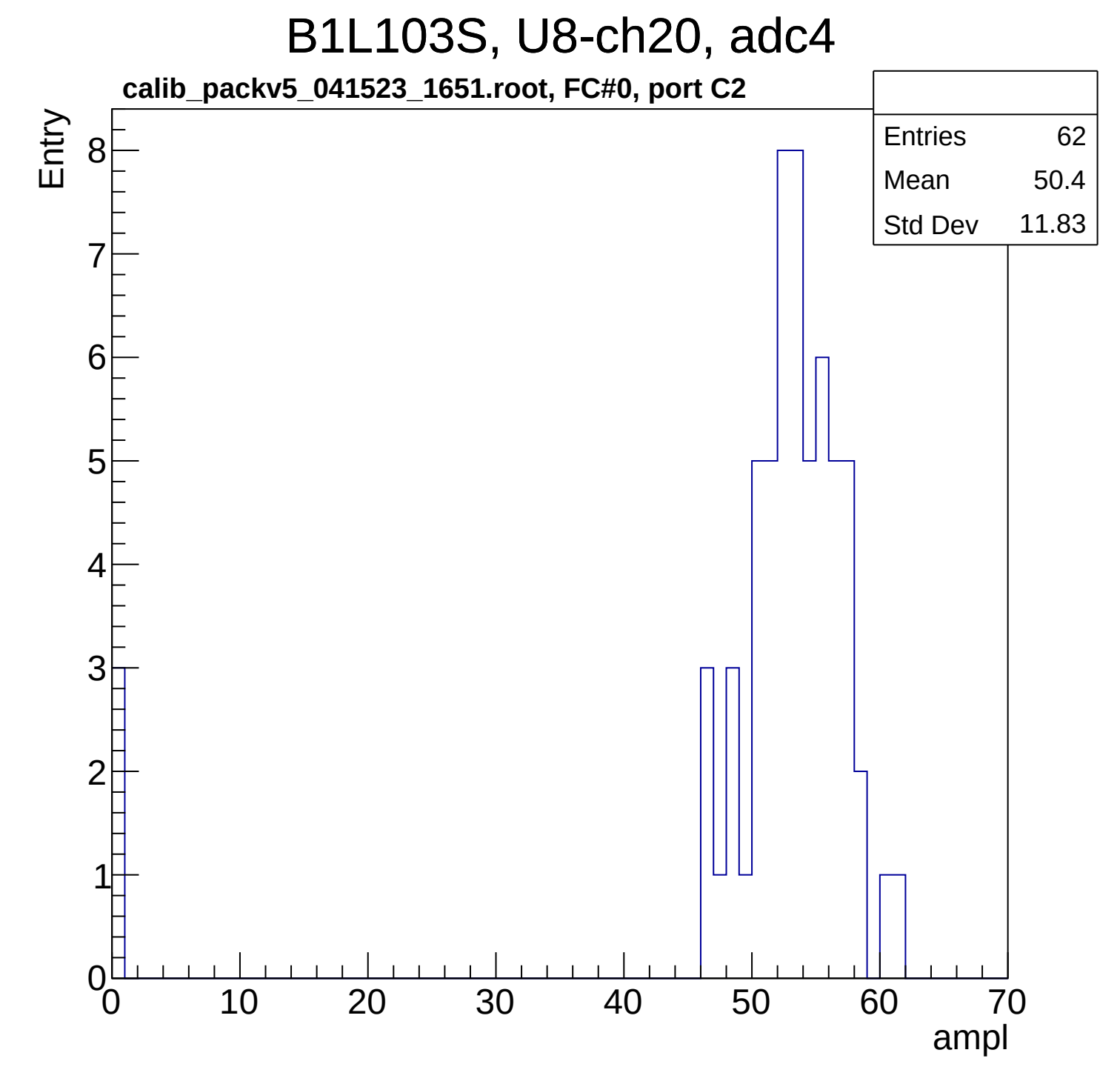
B1L103S, U8-ch20, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 50.4
Std Dev 11.83
Entry
ampl
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2
3
4
5
6
7
8
0
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20
30
40
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60
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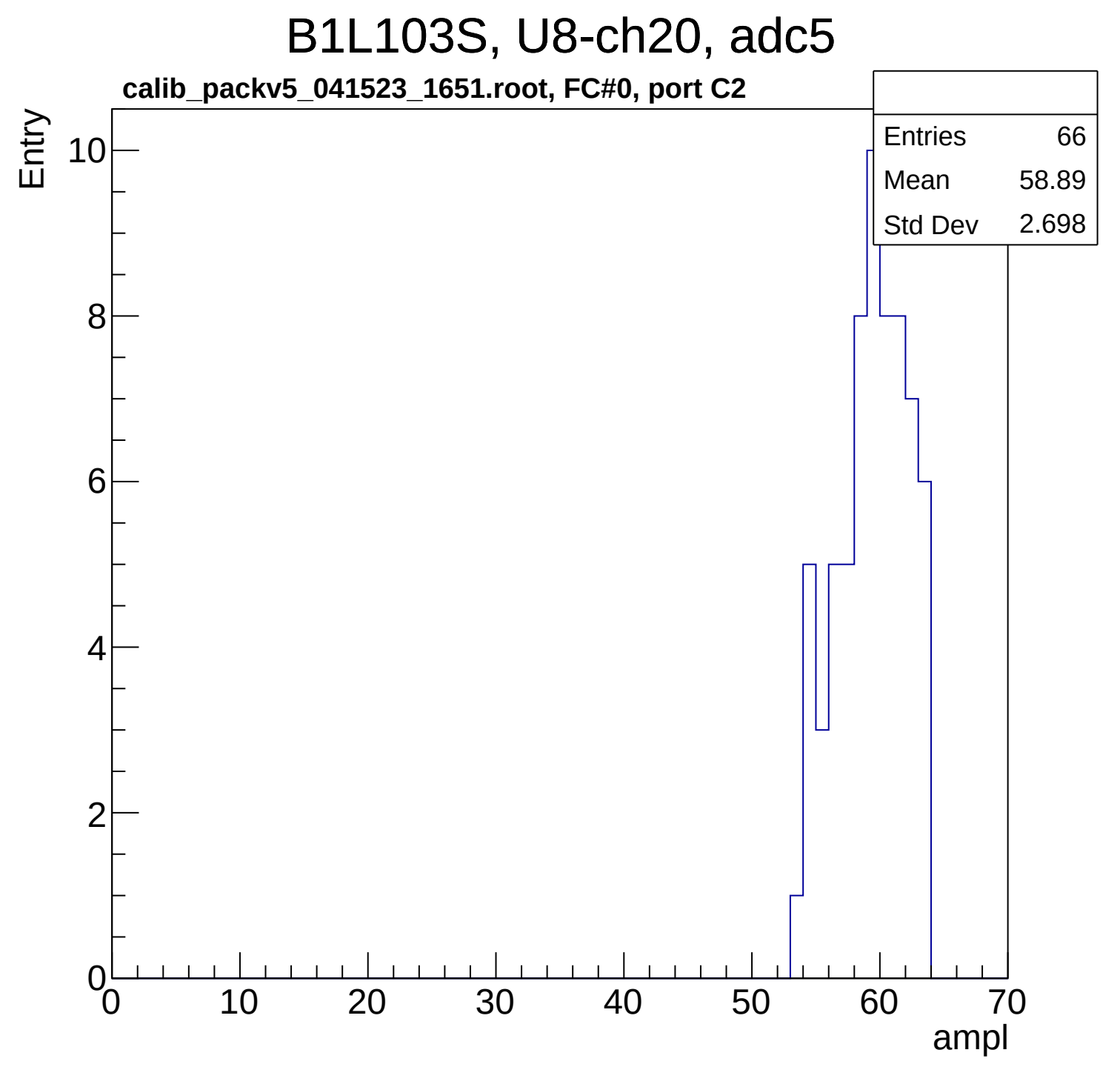
B1L103S, U8-ch20, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 58.89
Std Dev 2.698
Entry
ampl
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2
4
6
8
10
0
10
20
30
40
50
60
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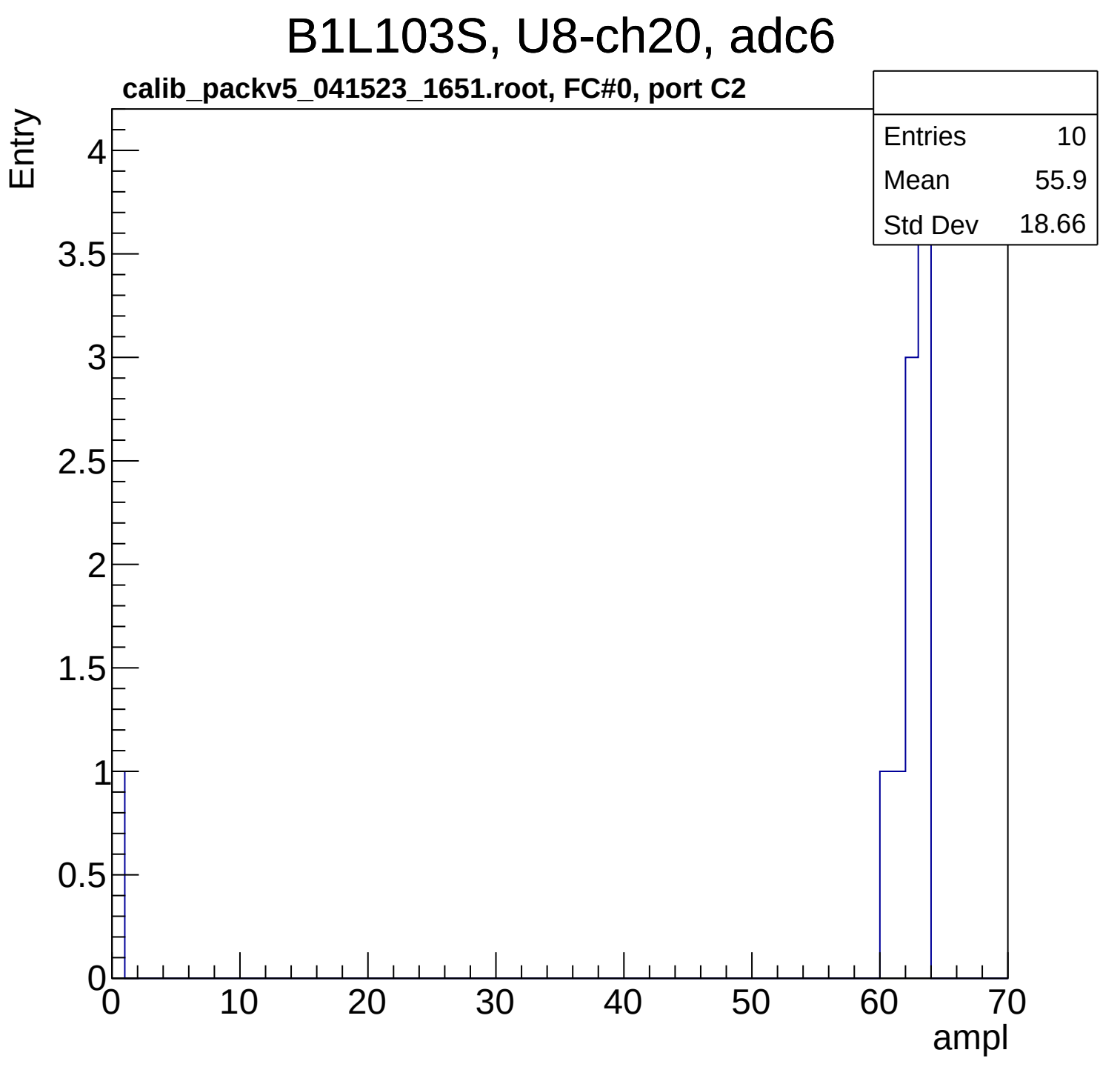
B1L103S, U8-ch20, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 55.9
Std Dev 18.66
Entry
ampl
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1
1.5
2
2.5
3
3.5
4
0
10
20
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40
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60
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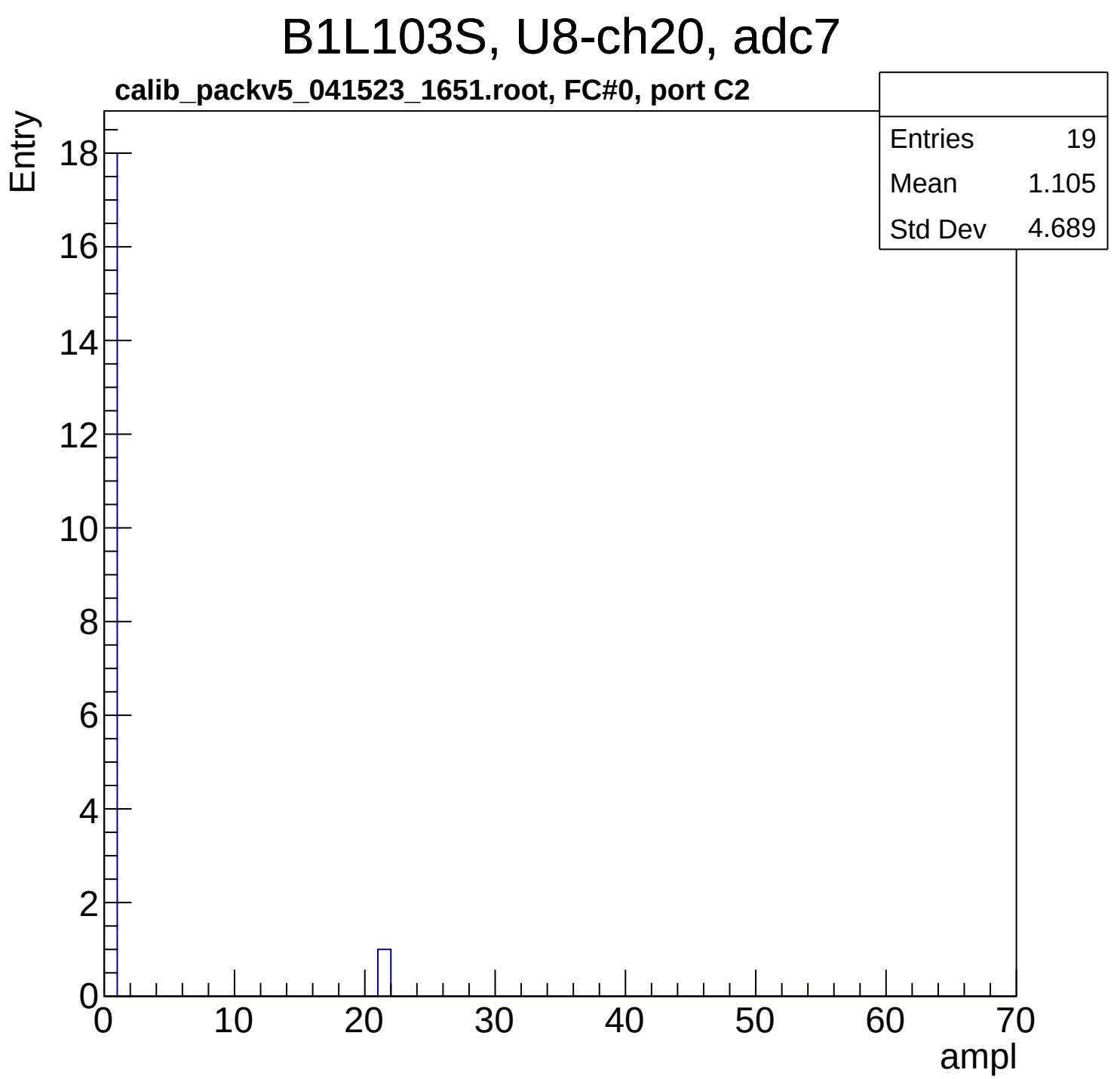
B1L103S, U8-ch20, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.105
Std Dev 4.689
Entry
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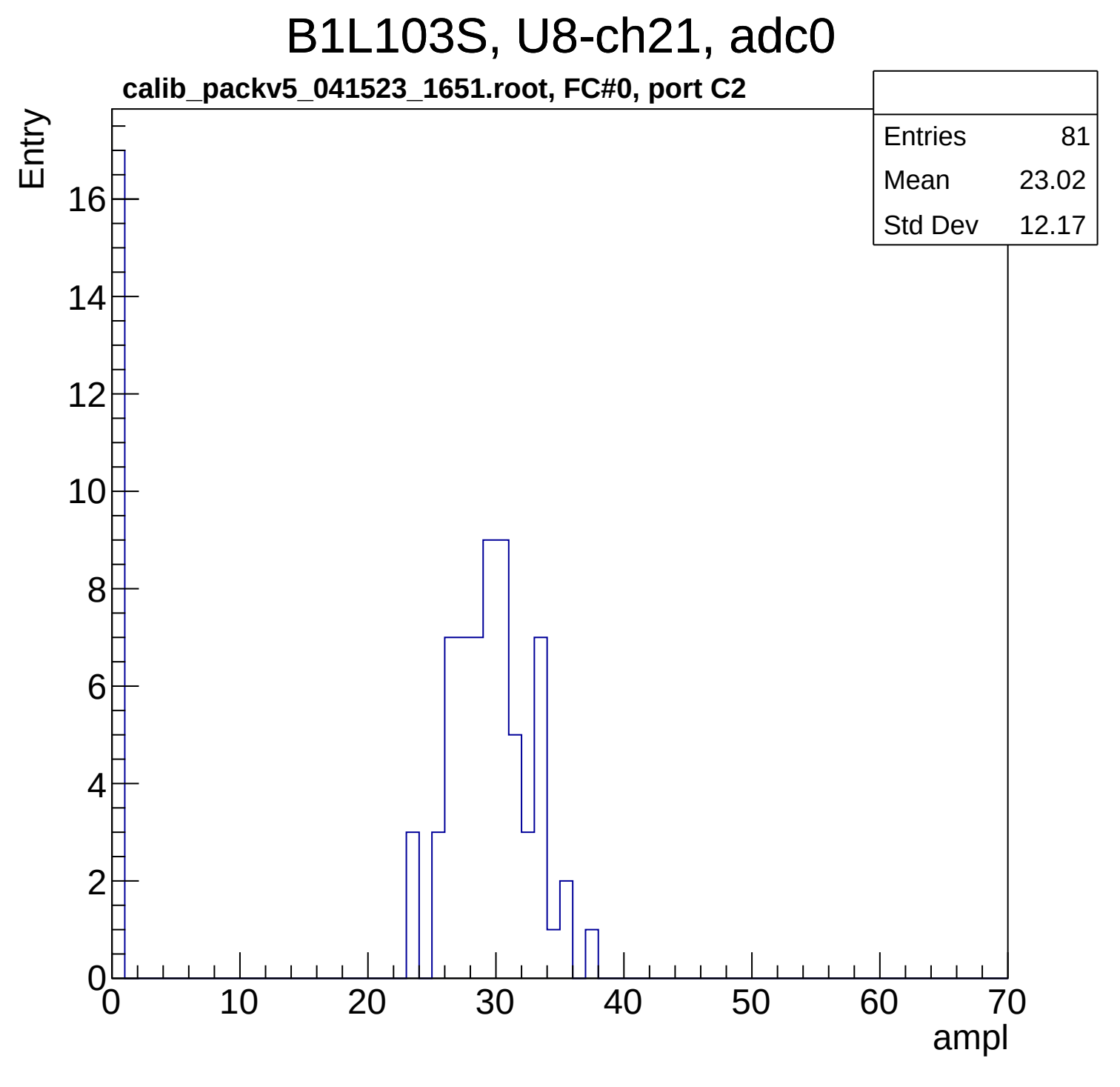
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch21, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 23.02
Std Dev 12.17
Entry
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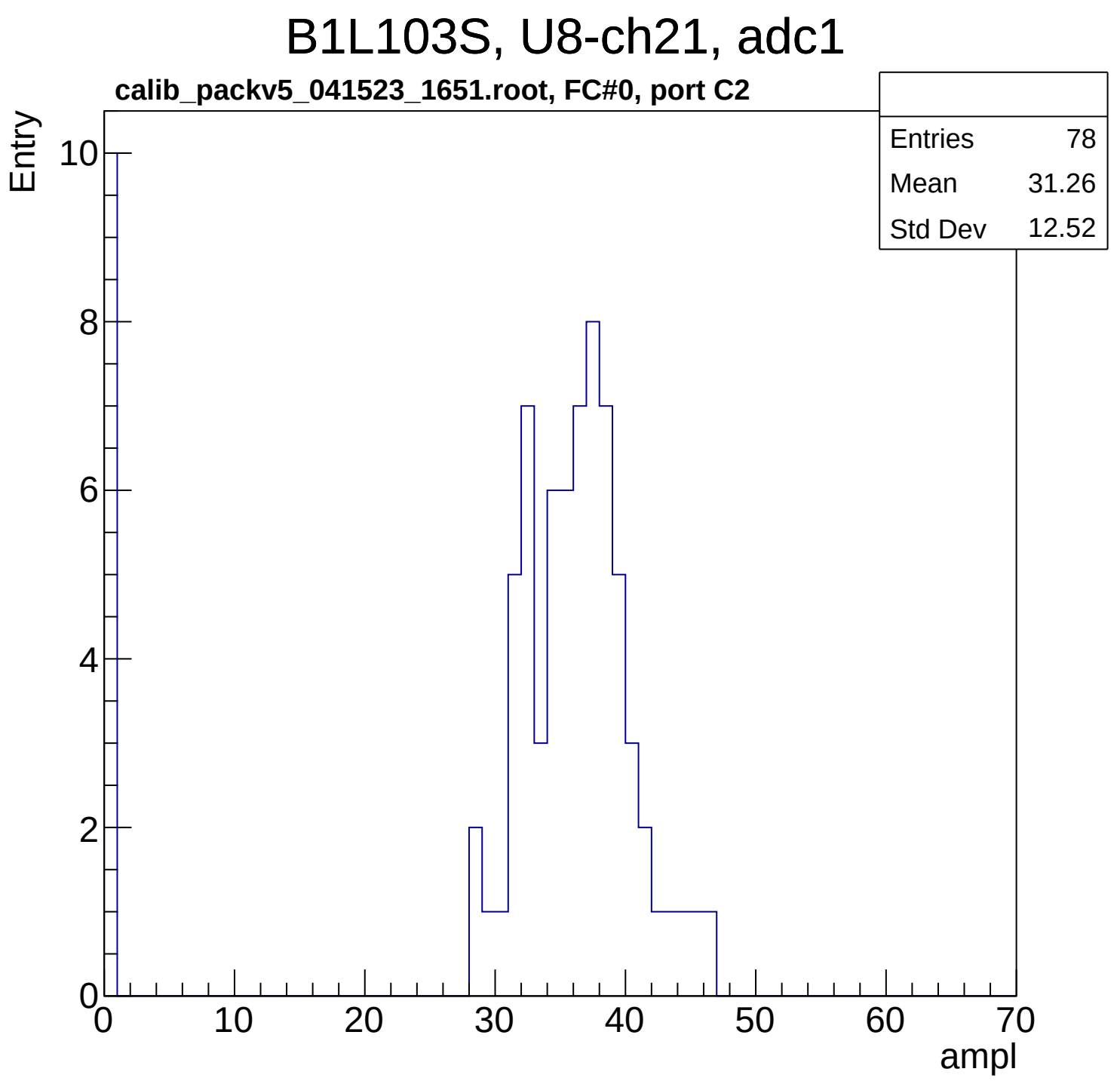
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch21, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 31.26
Std Dev 12.52
Entry
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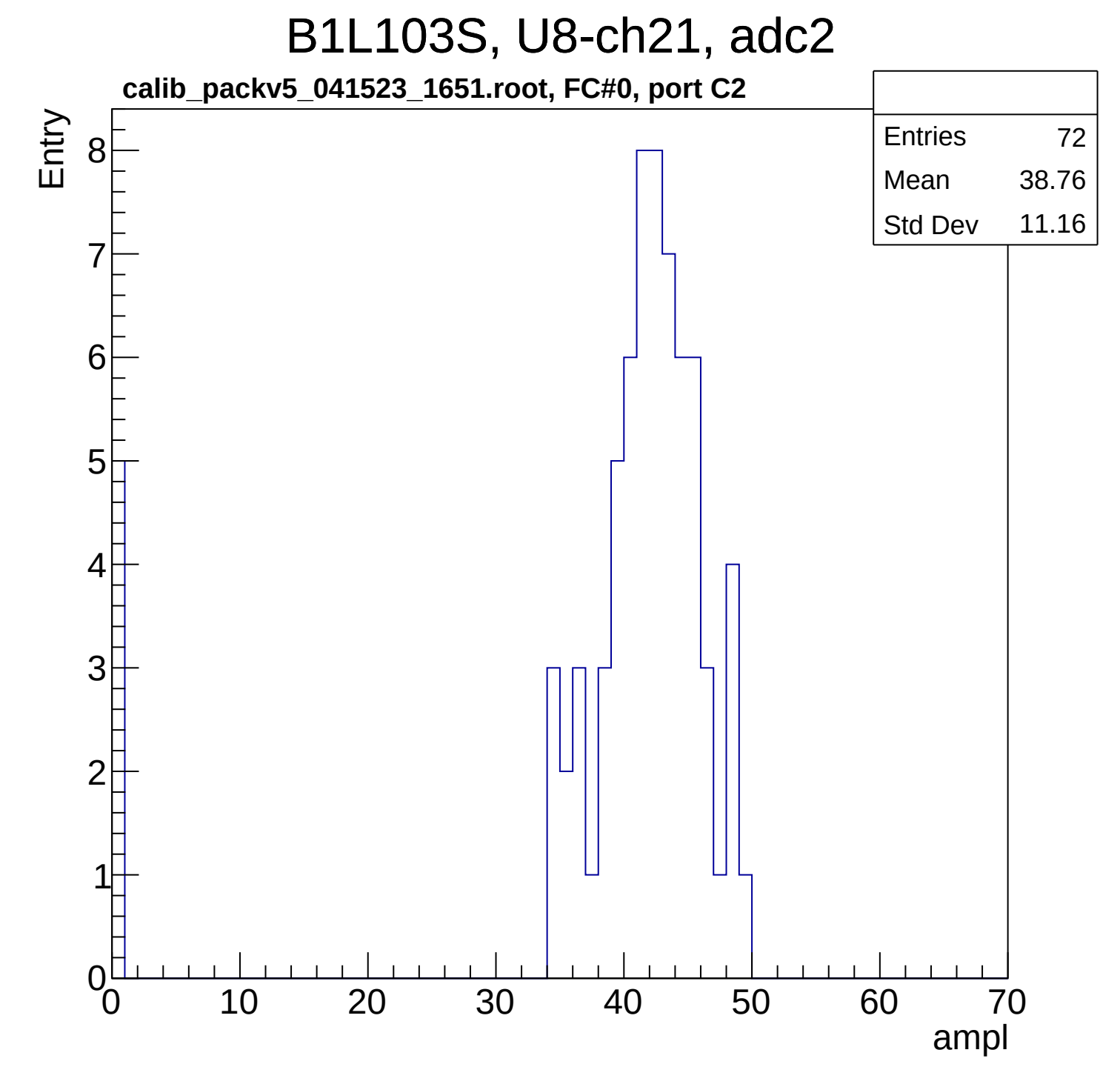
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch21, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 38.76
Std Dev 11.16
Entry
ampl
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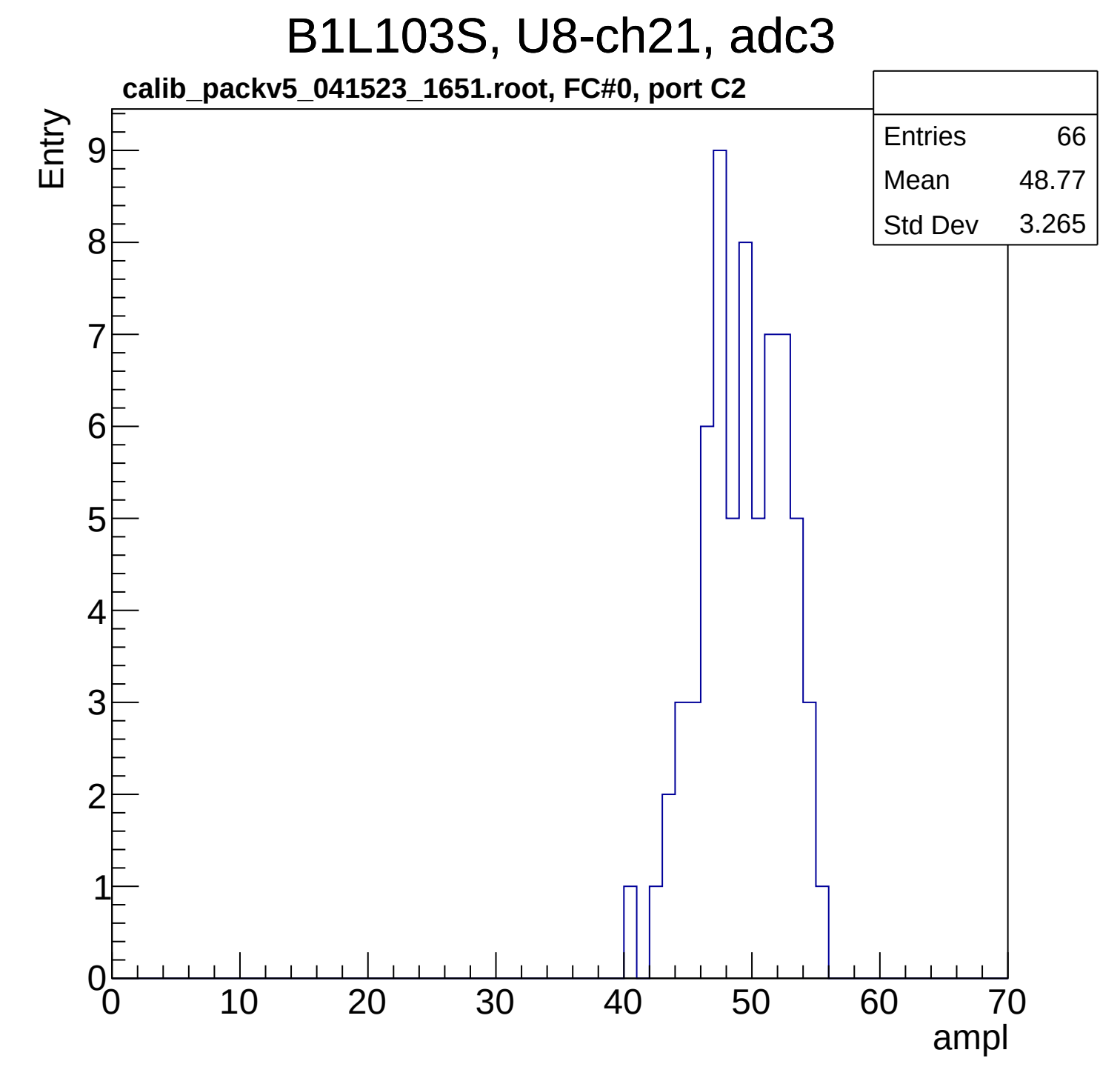
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch21, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 48.77
Std Dev 3.265
Entry
ampl
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3
4
5
6
7
8
9
0
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40
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60
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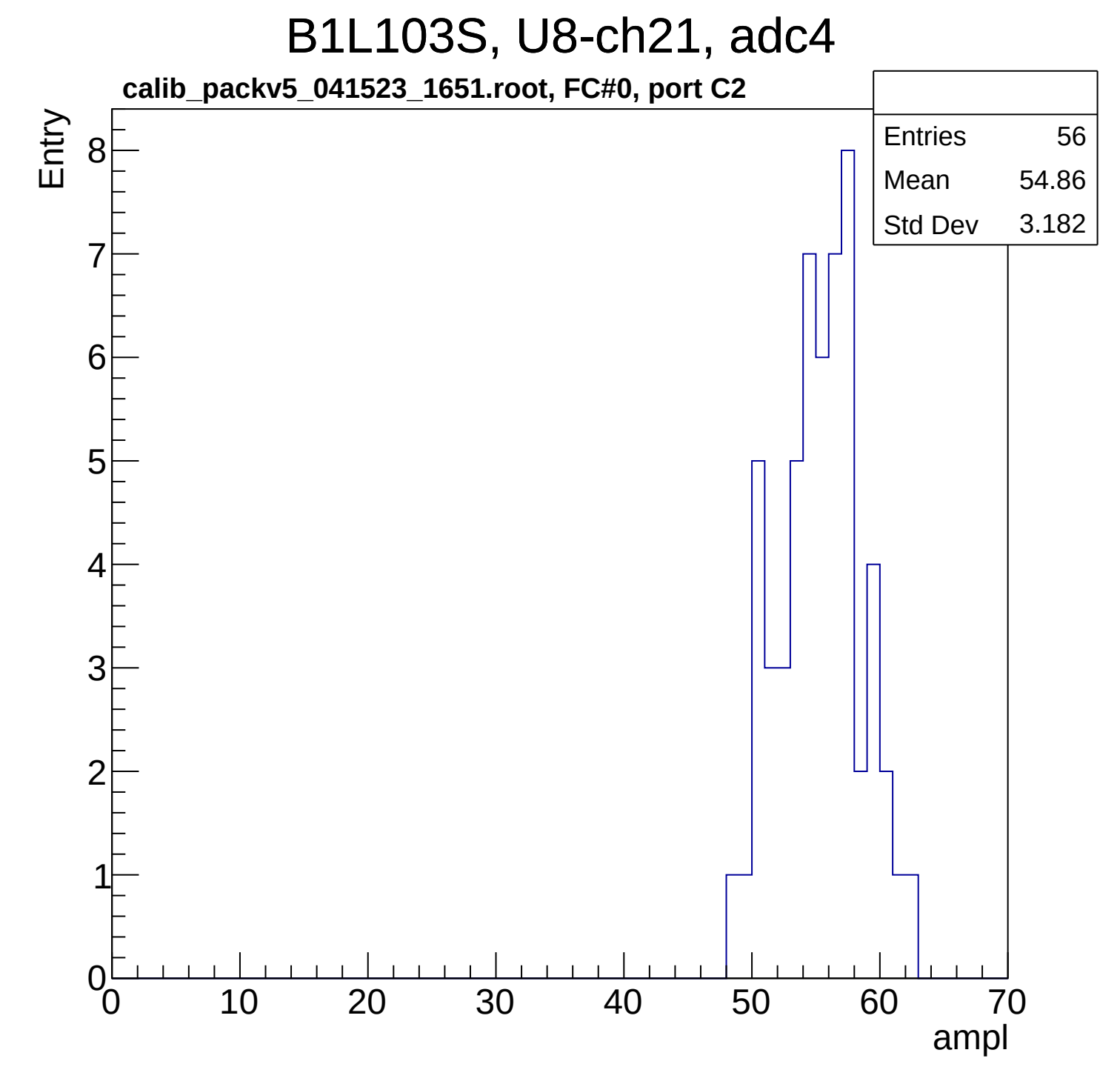
B1L103S, U8-ch21, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 54.86
Std Dev 3.182
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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40
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60
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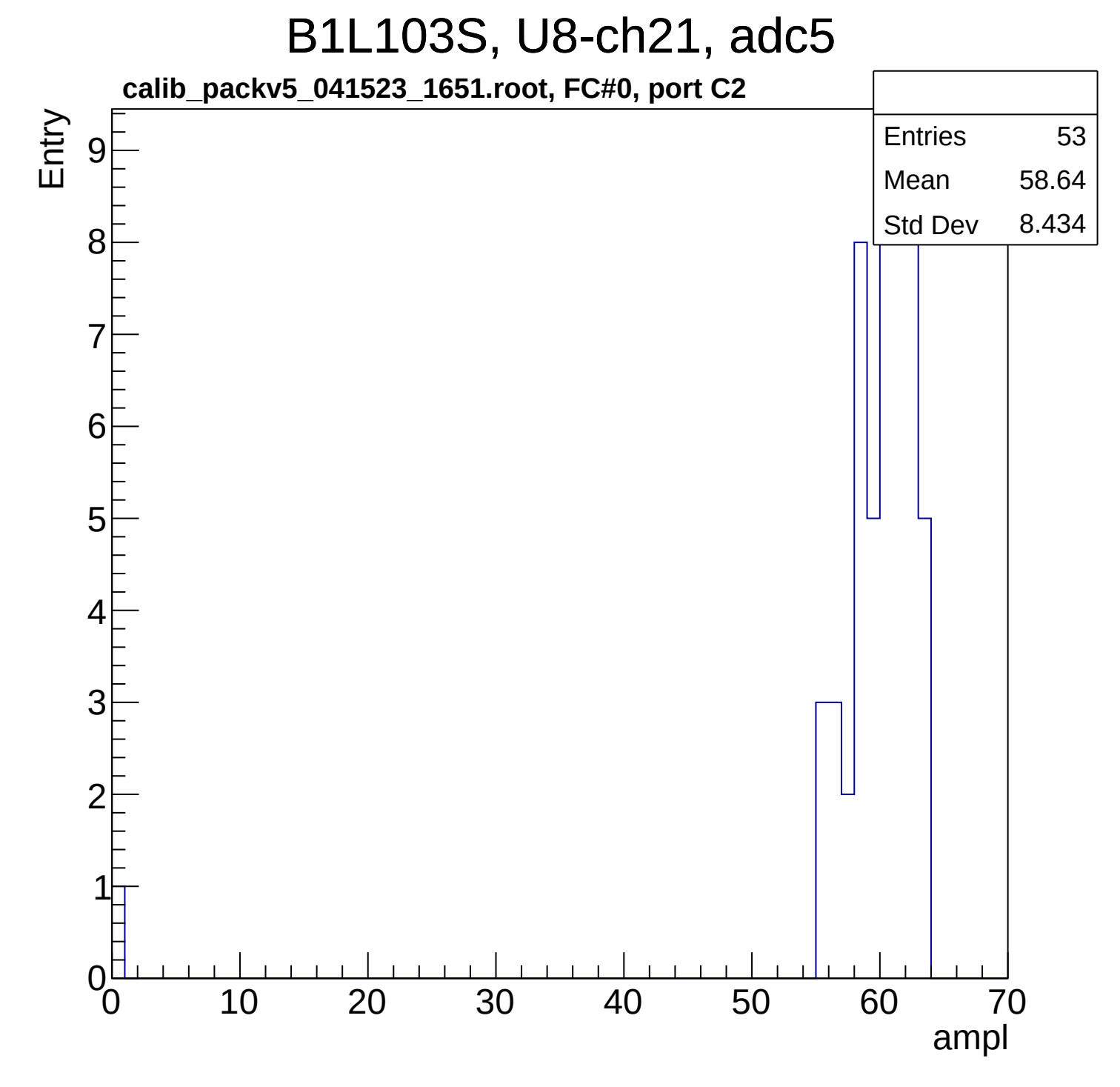
B1L103S, U8-ch21, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 58.64
Std Dev 8.434
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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60
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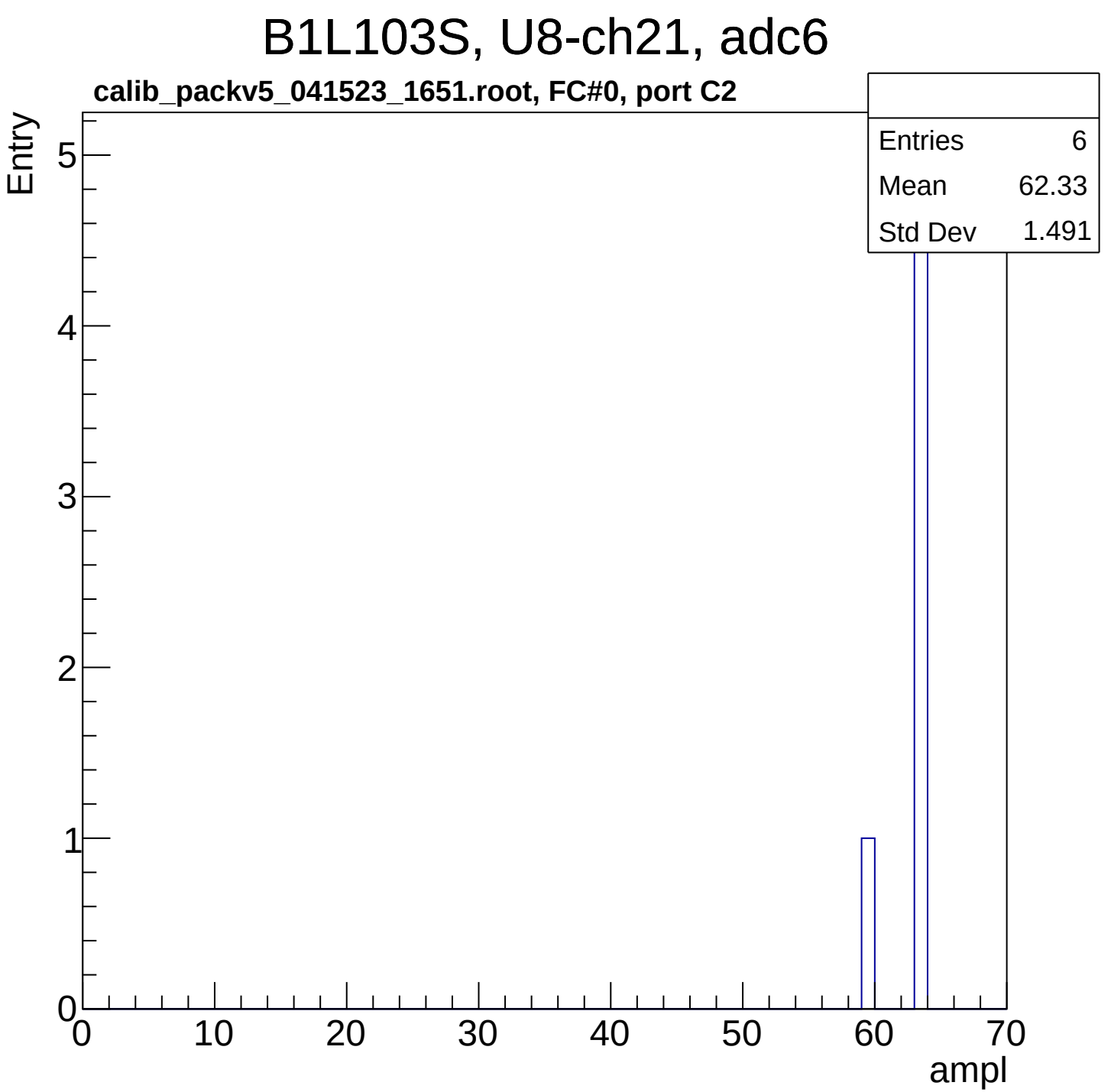
B1L103S, U8-ch21, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 62.33
Std Dev 1.491
Entry
ampl
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1
2
3
4
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0
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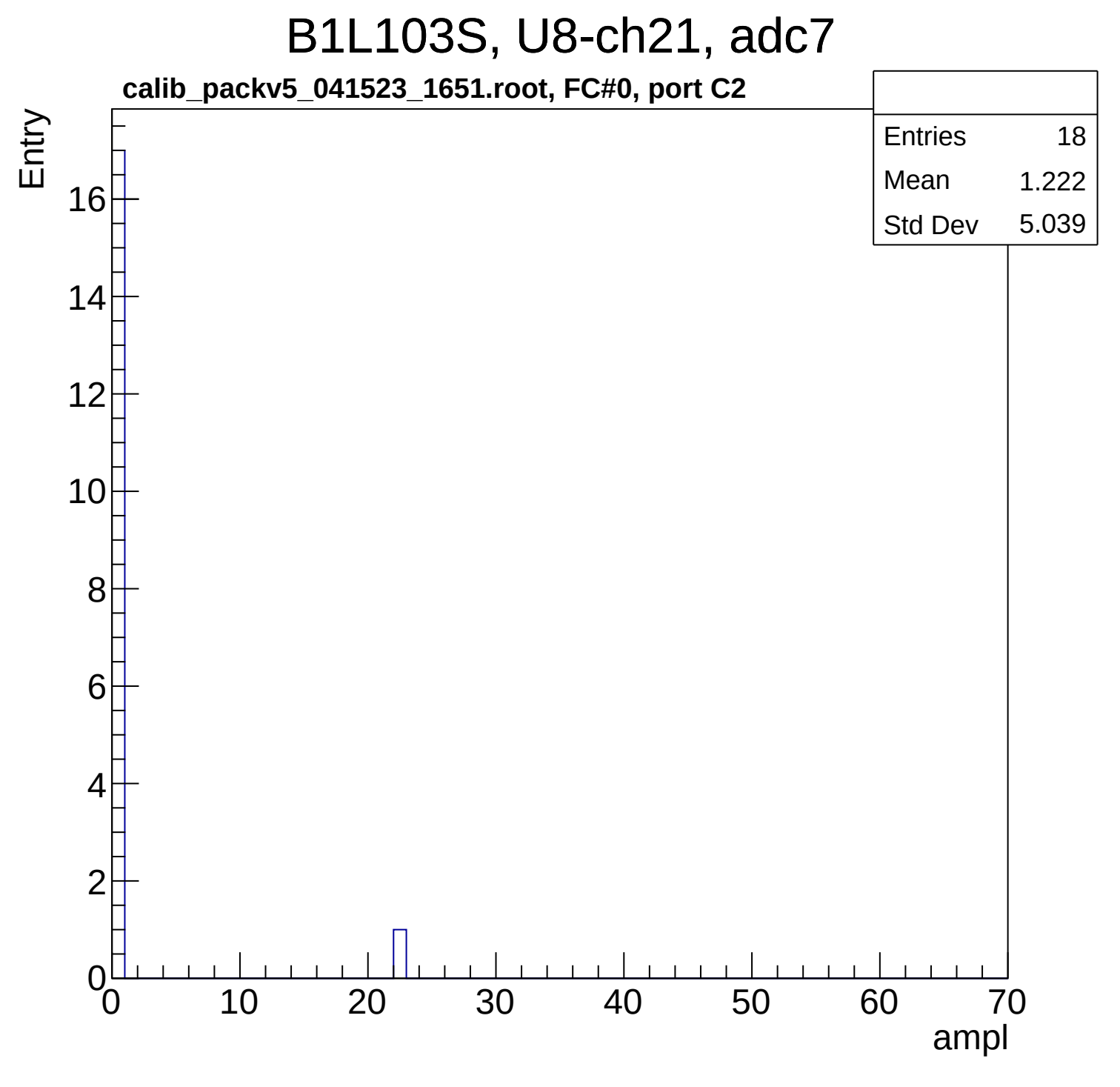
20
30
40
50
60
70


B1L103S, U8-ch21, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.222
Std Dev 5.039
Entry
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4
6
8
10
12
14
16
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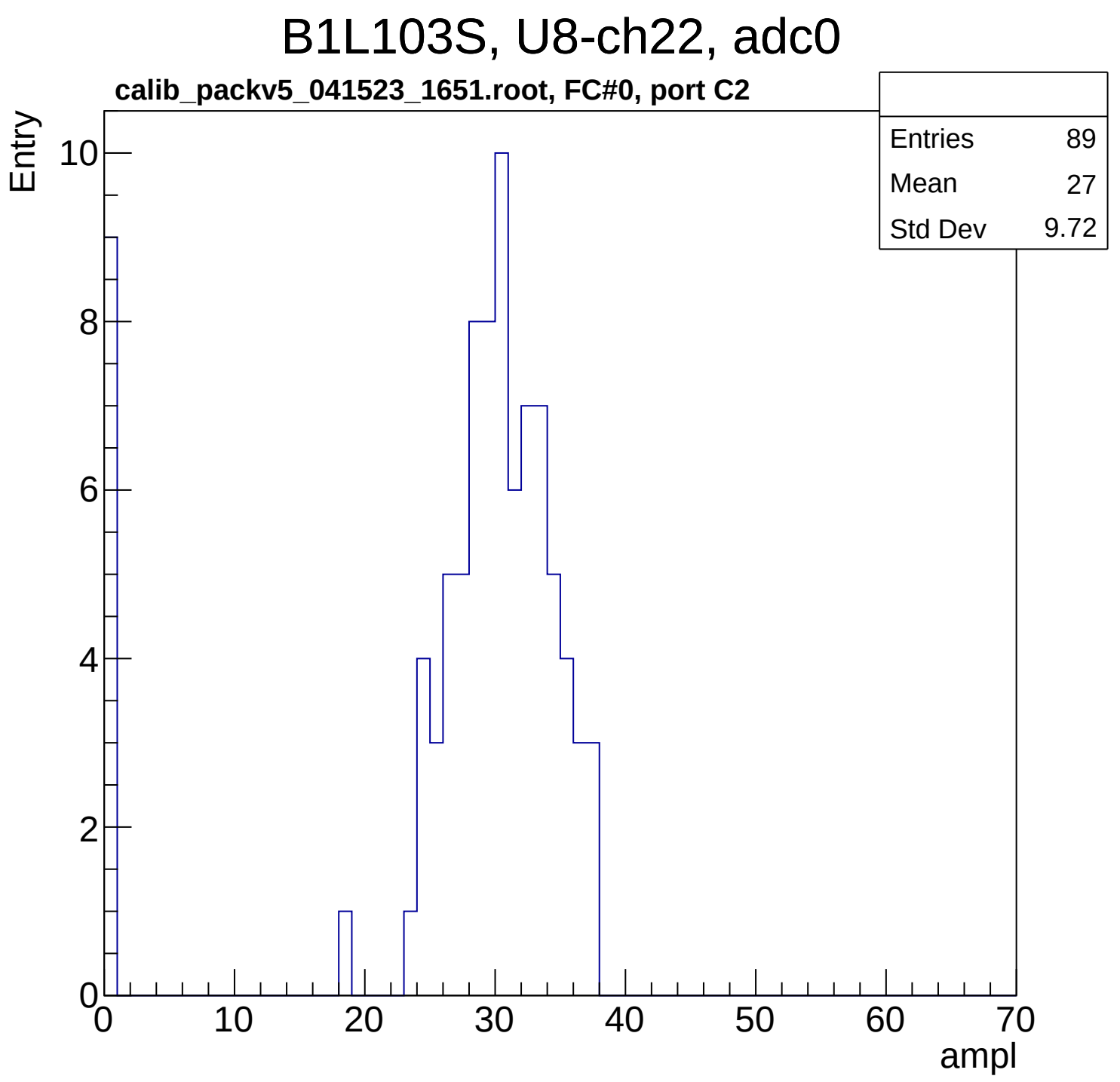
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch22, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 27
Std Dev 9.72
Entry
ampl
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6
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0
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20
30
40
50
60
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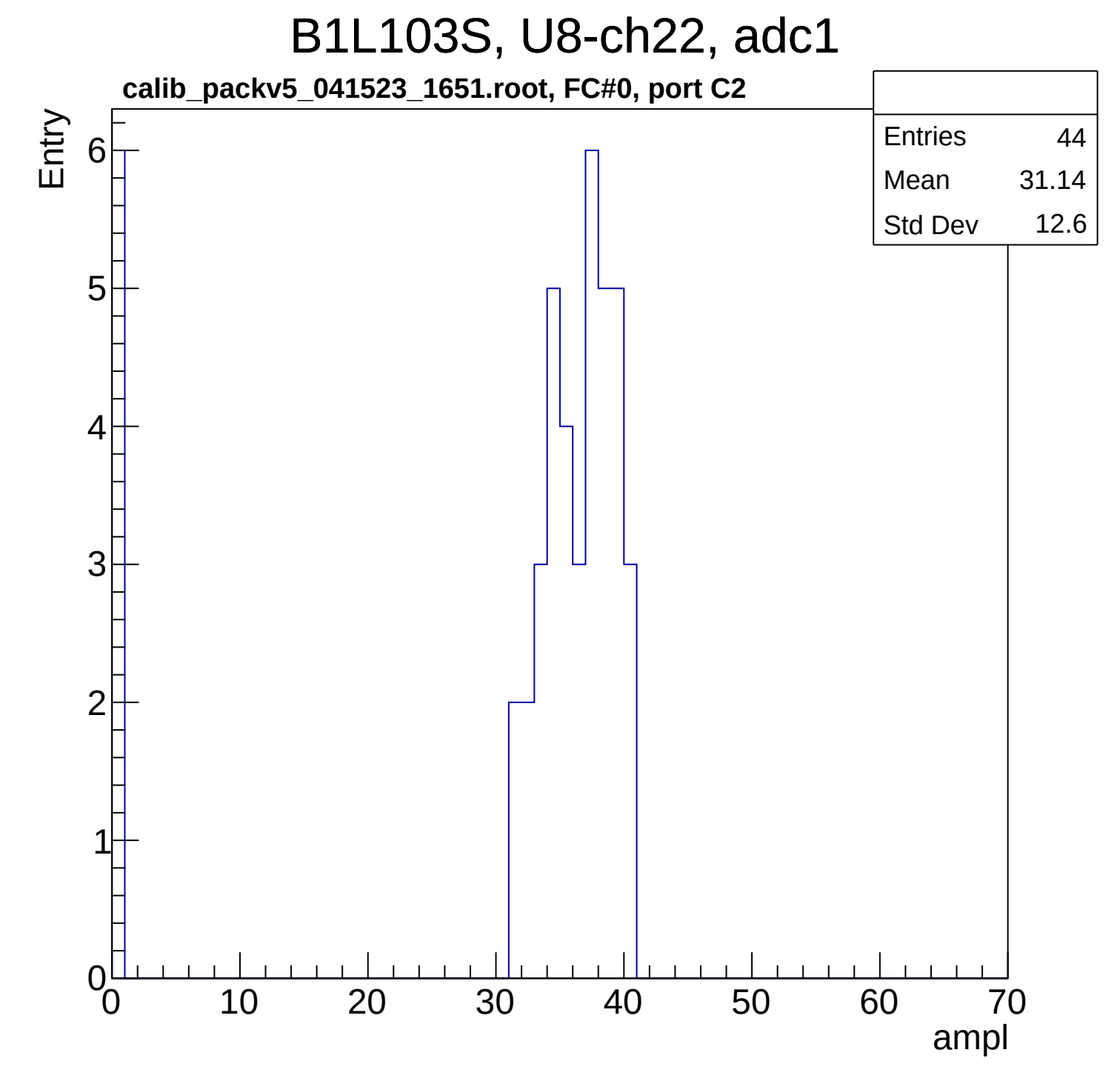
B1L103S, U8-ch22, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 31.14
Std Dev 12.6
Entry
ampl
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1
2
3
4
5
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0
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20
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40
50
60
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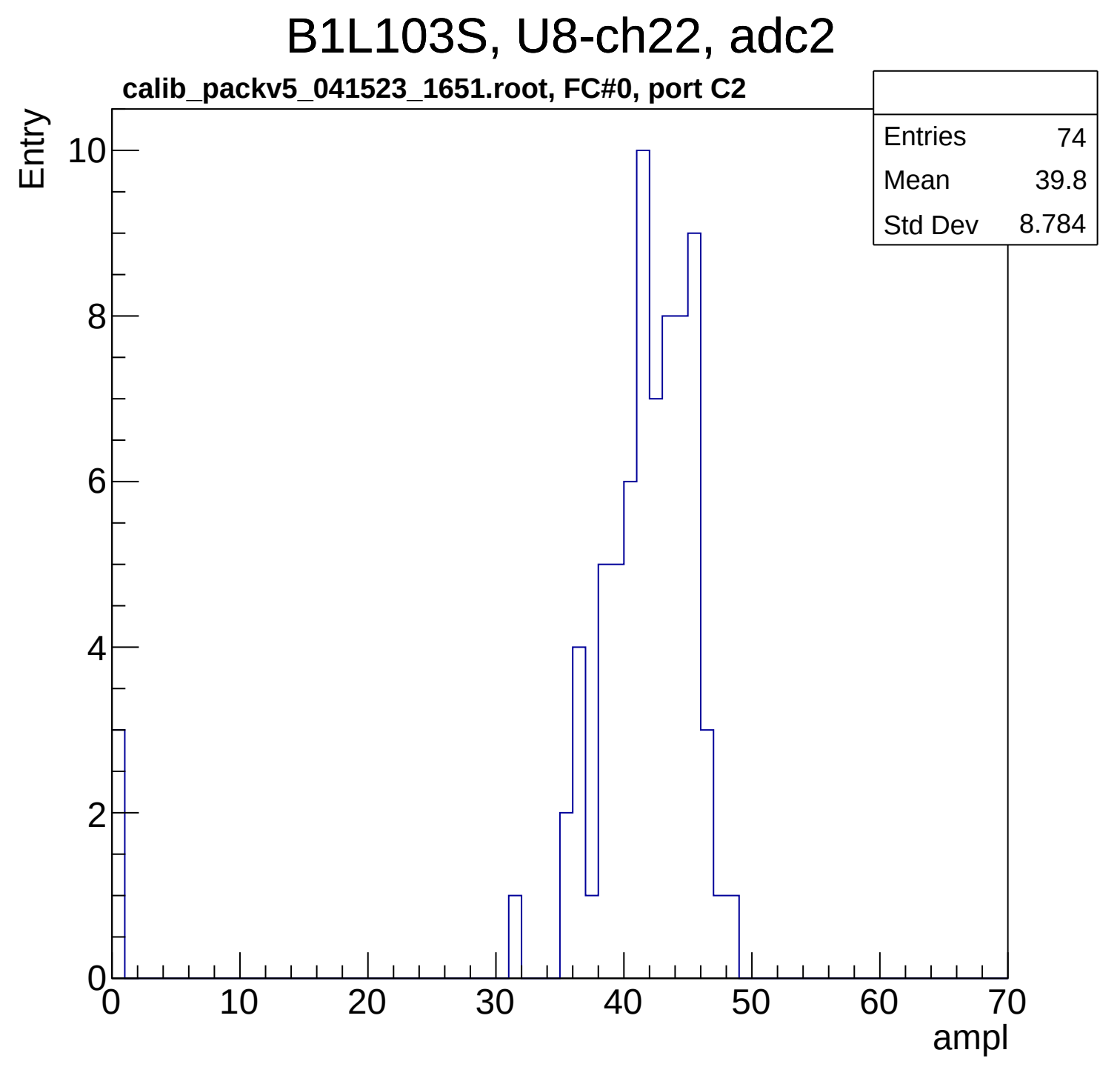
B1L103S, U8-ch22, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 39.8
Std Dev 8.784
Entry
ampl
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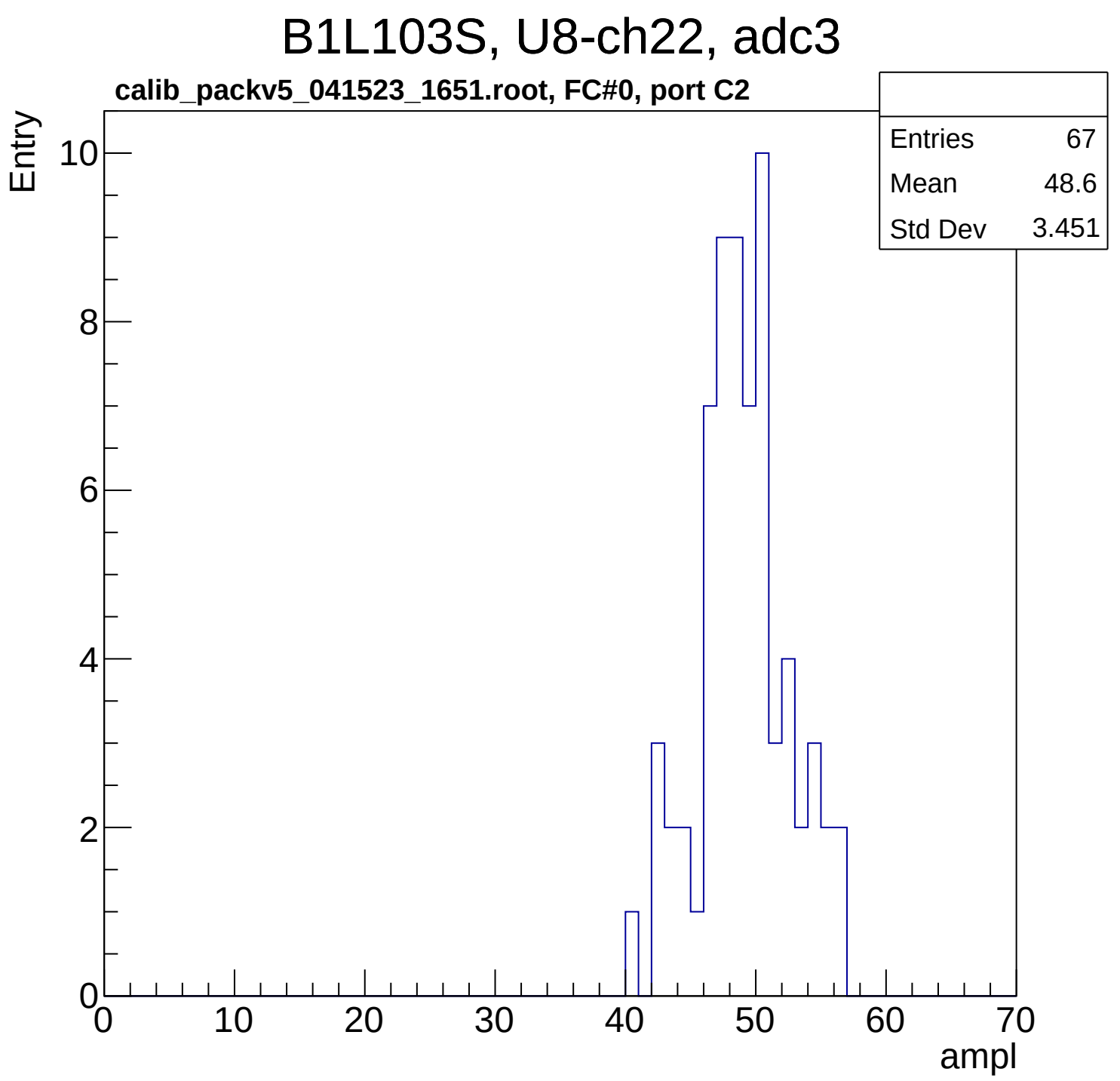
B1L103S, U8-ch22, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 48.6
Std Dev 3.451
Entry
ampl
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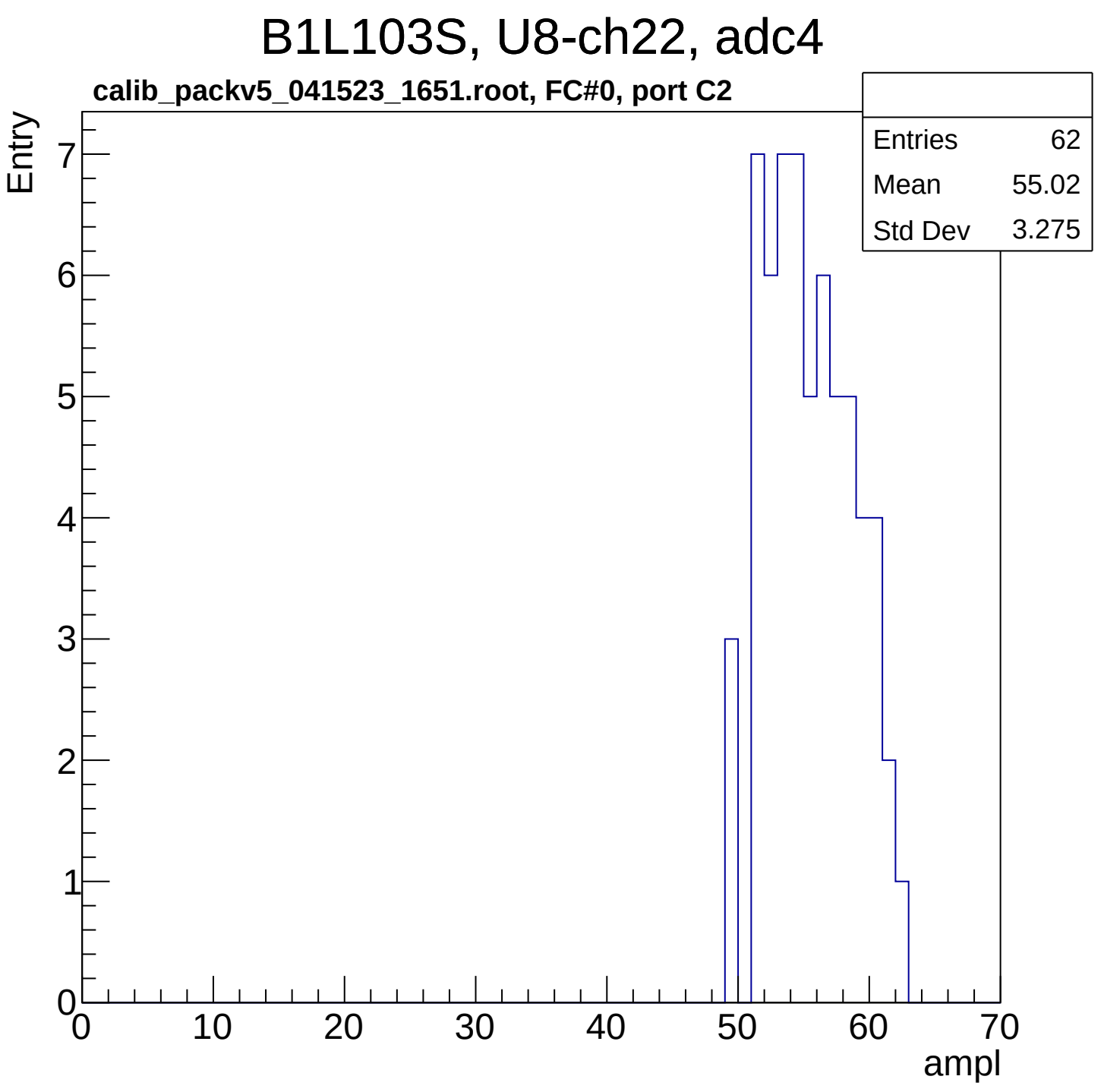
B1L103S, U8-ch22, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 55.02
Std Dev 3.275
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
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60
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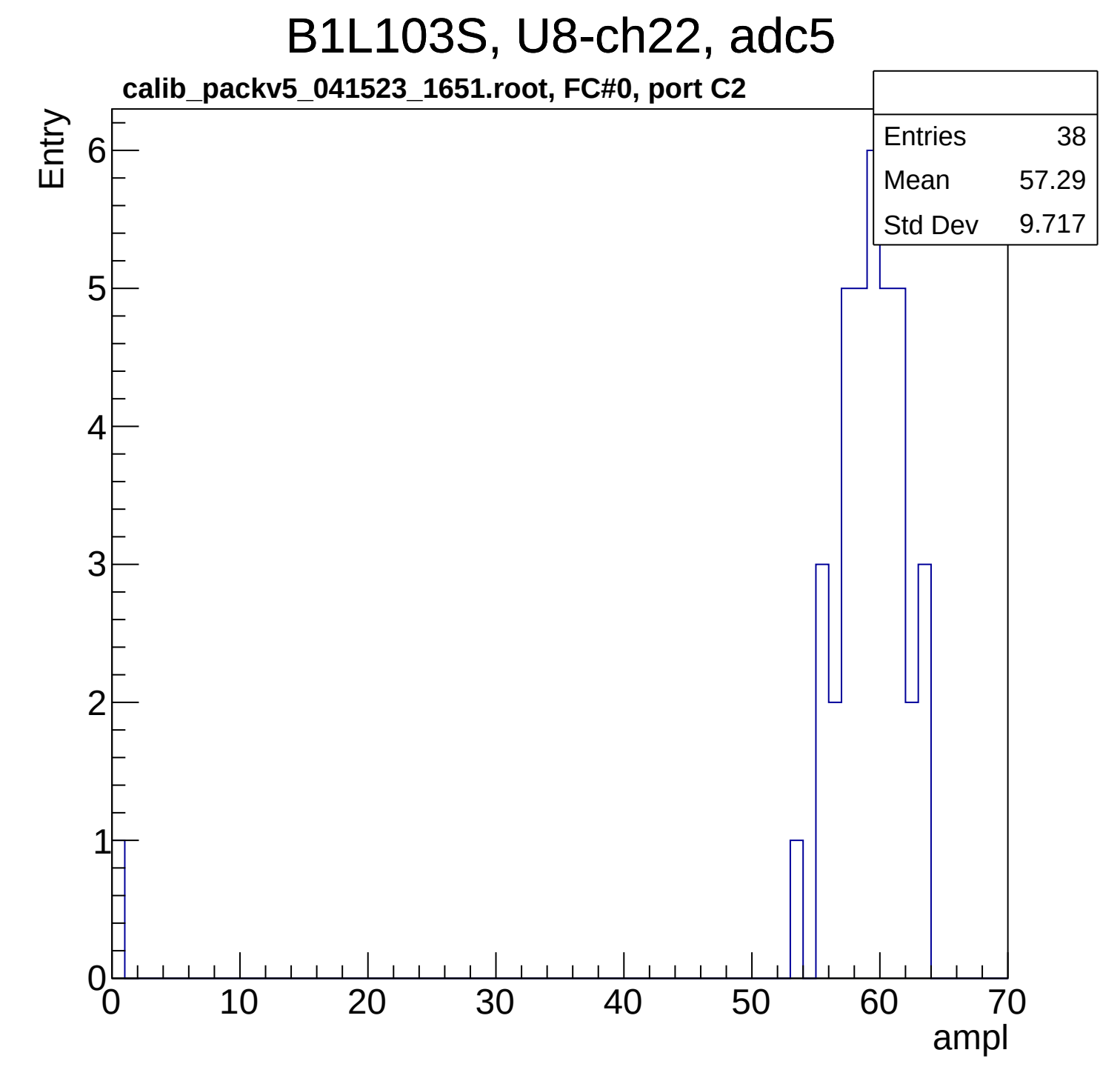
B1L103S, U8-ch22, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 57.29
Std Dev 9.717
Entry
ampl
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0
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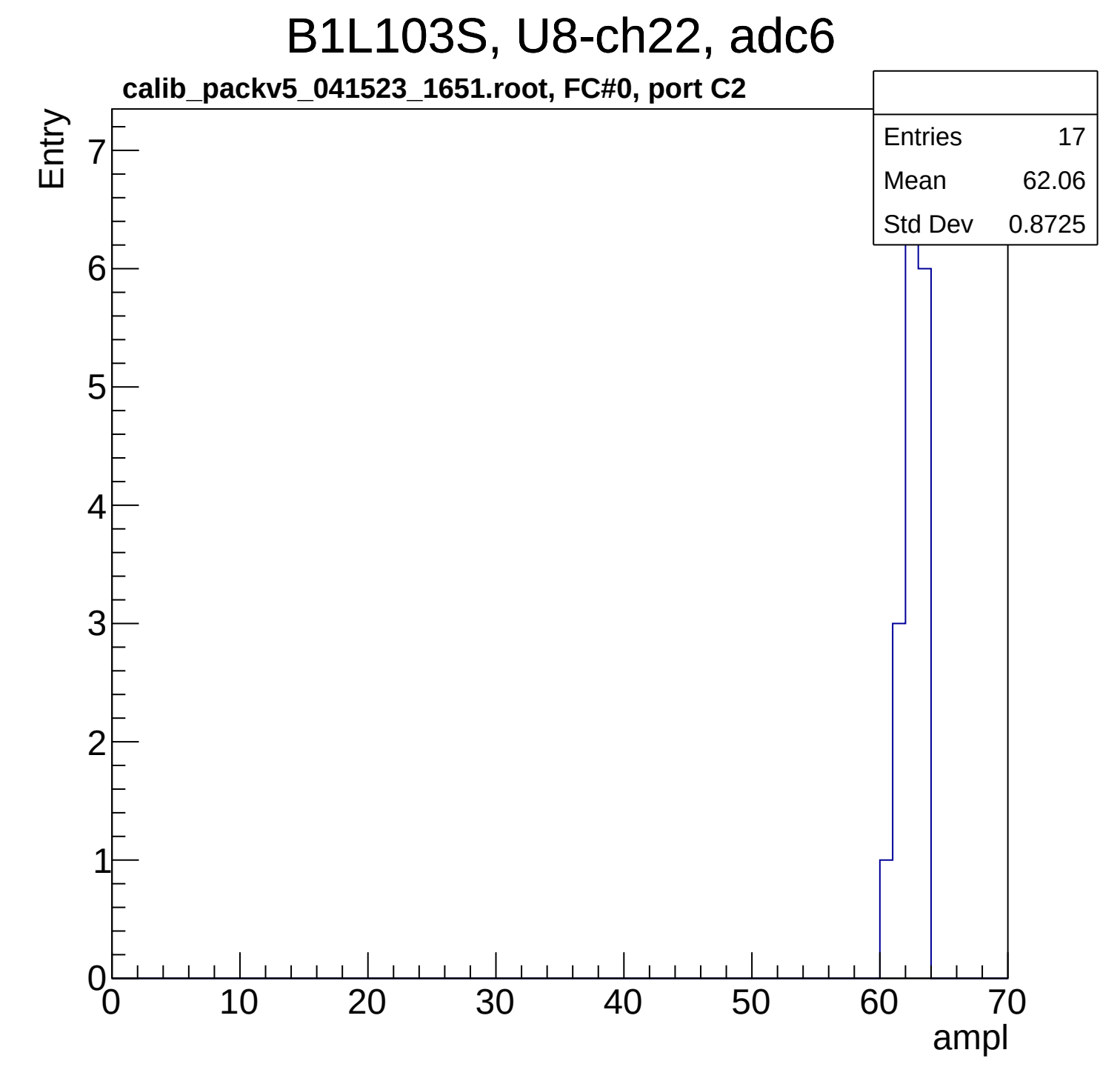
B1L103S, U8-ch22, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 62.06
Std Dev 0.8725
Entry
ampl
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1
2
3
4
5
6
7
0
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20
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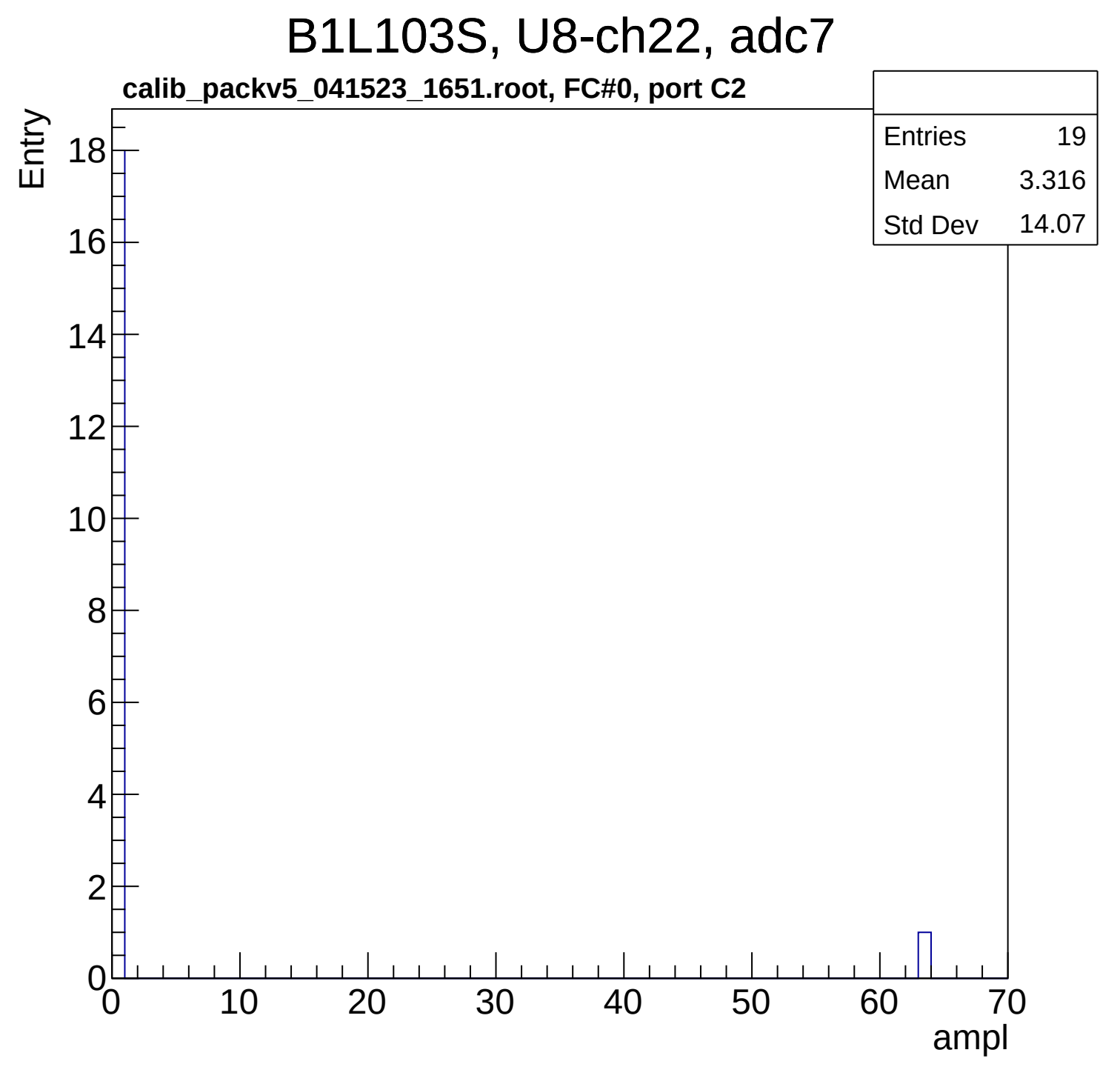
B1L103S, U8-ch22, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.316
Std Dev 14.07
Entry
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6
8
10
12
14
16
18
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10
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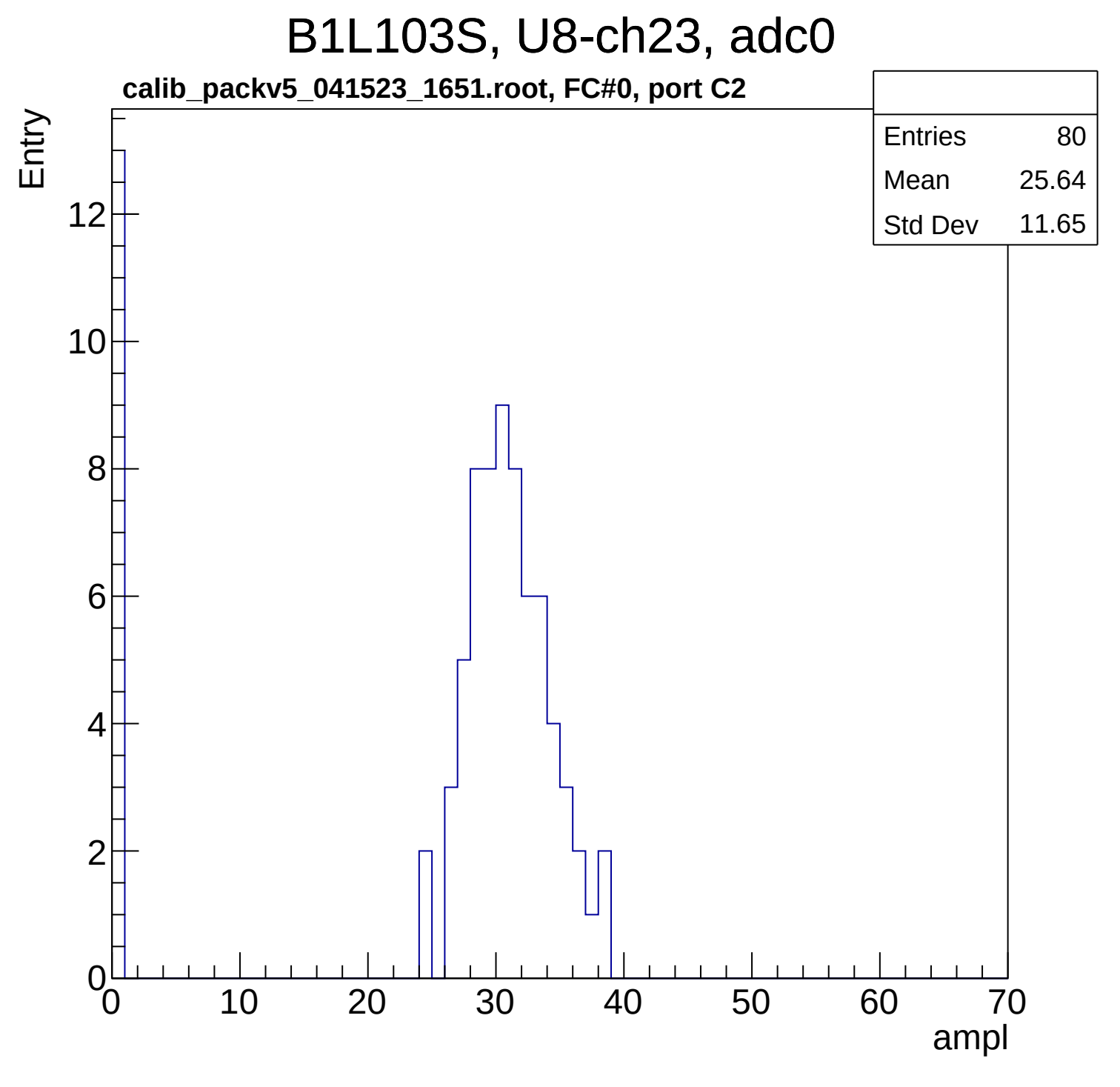
70
ampl


B1L103S, U8-ch23, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 25.64
Std Dev 11.65
Entry
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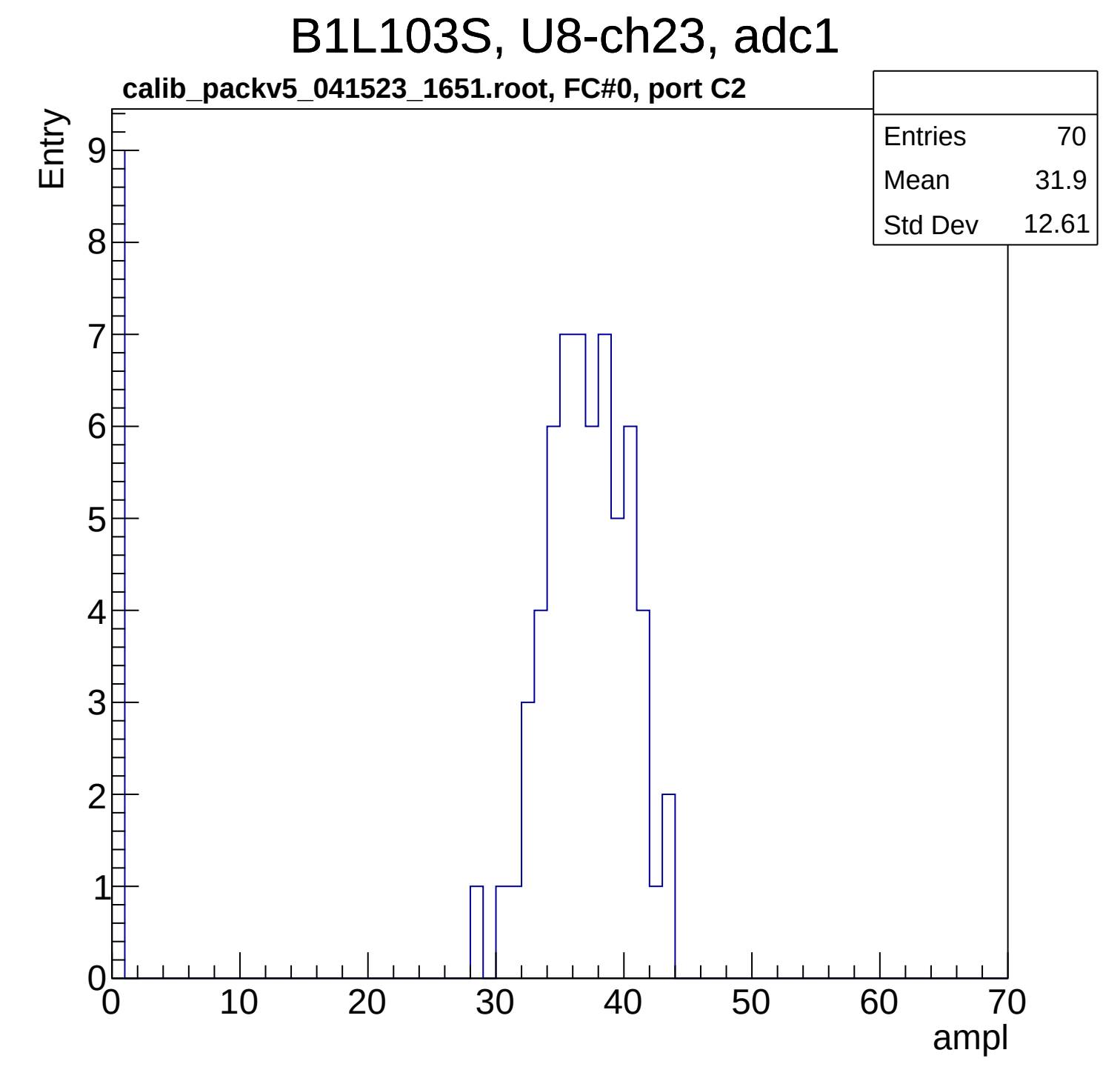
70
ampl


B1L103S, U8-ch23, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 31.9
Std Dev 12.61
Entry
ampl
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3
4
5
6
7
8
9
0
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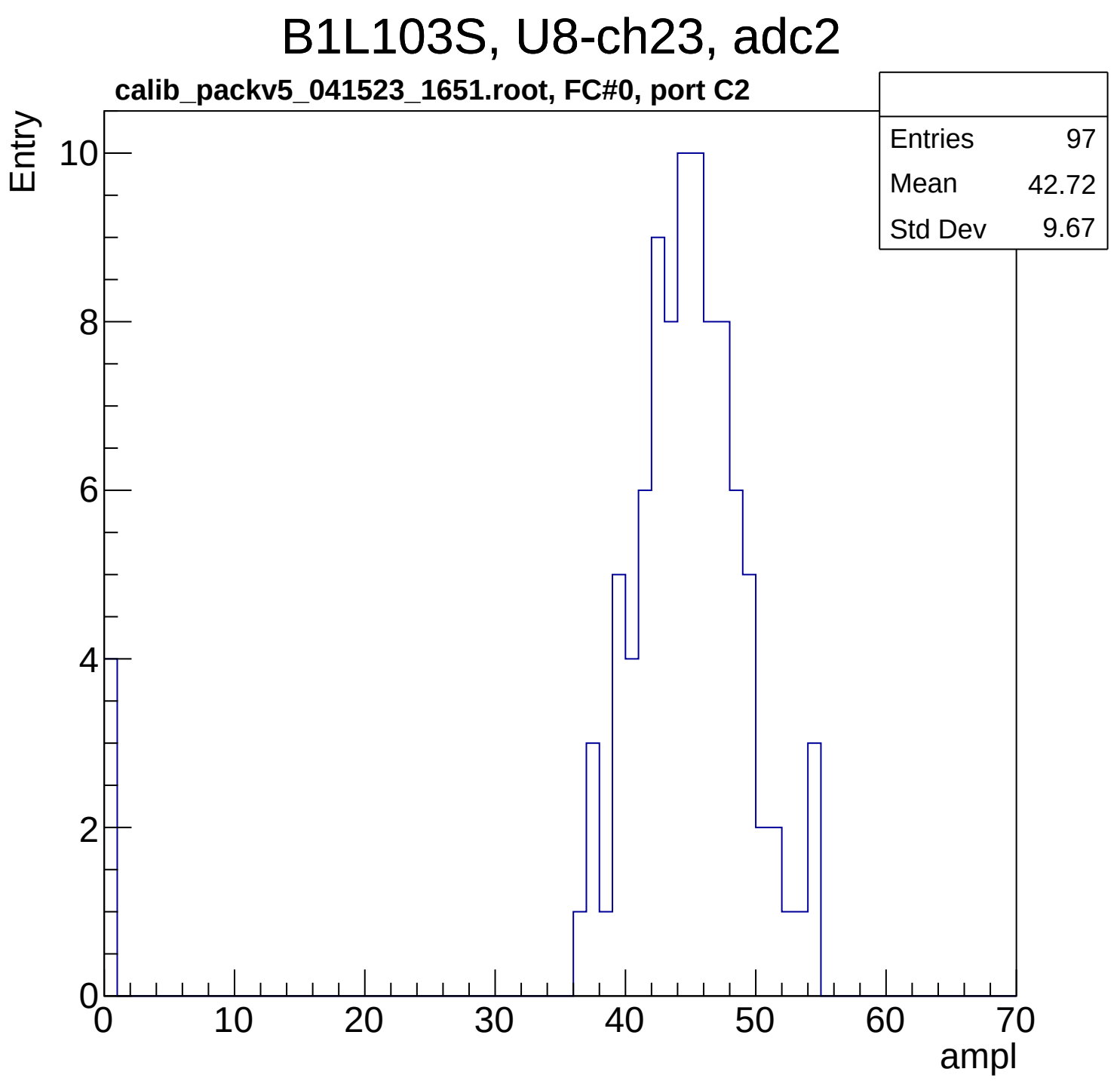
B1L103S, U8-ch23, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 42.72
Std Dev 9.67
Entry
ampl
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2
4
6
8
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0
10
20
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60
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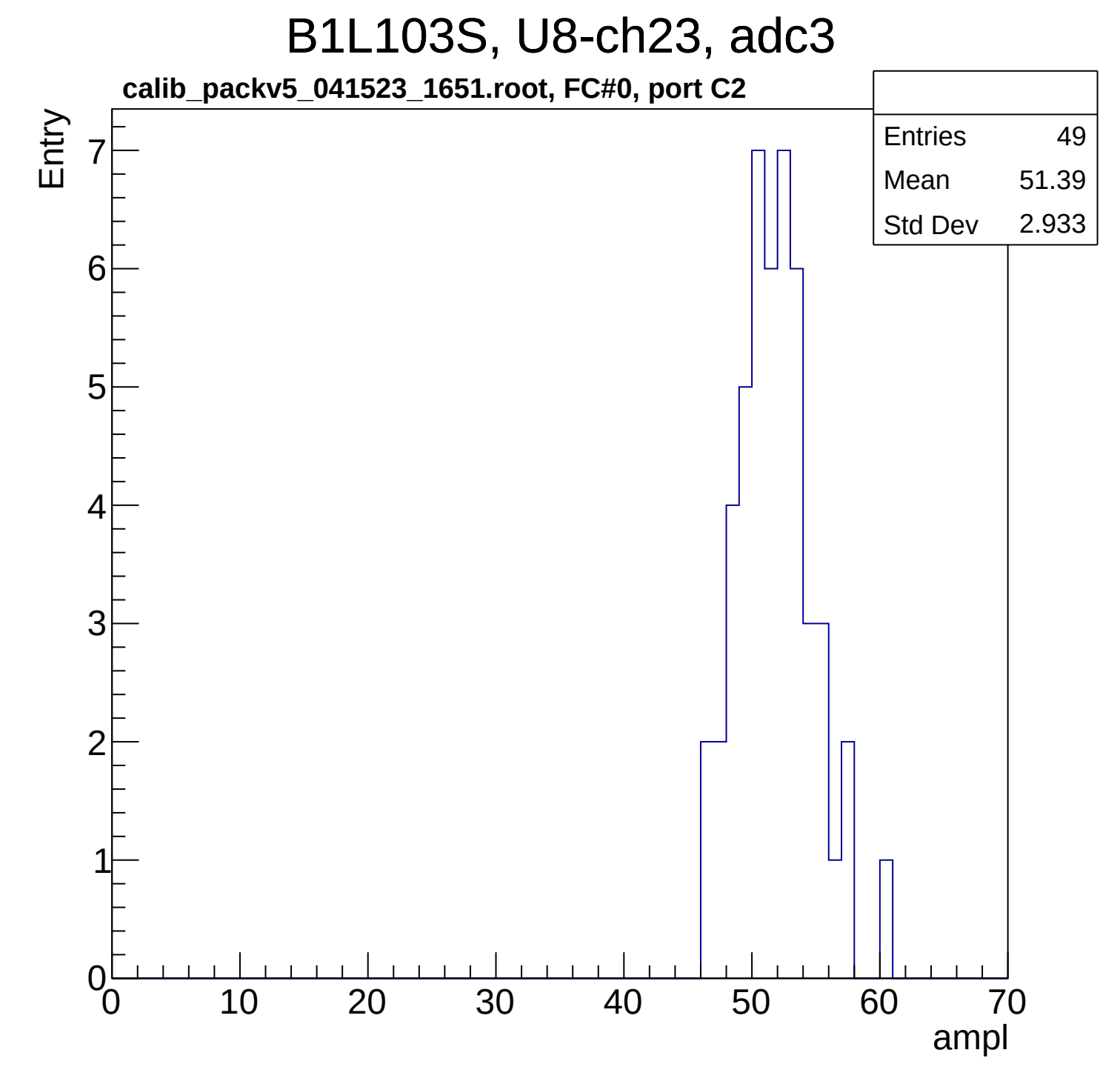
B1L103S, U8-ch23, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 51.39
Std Dev 2.933
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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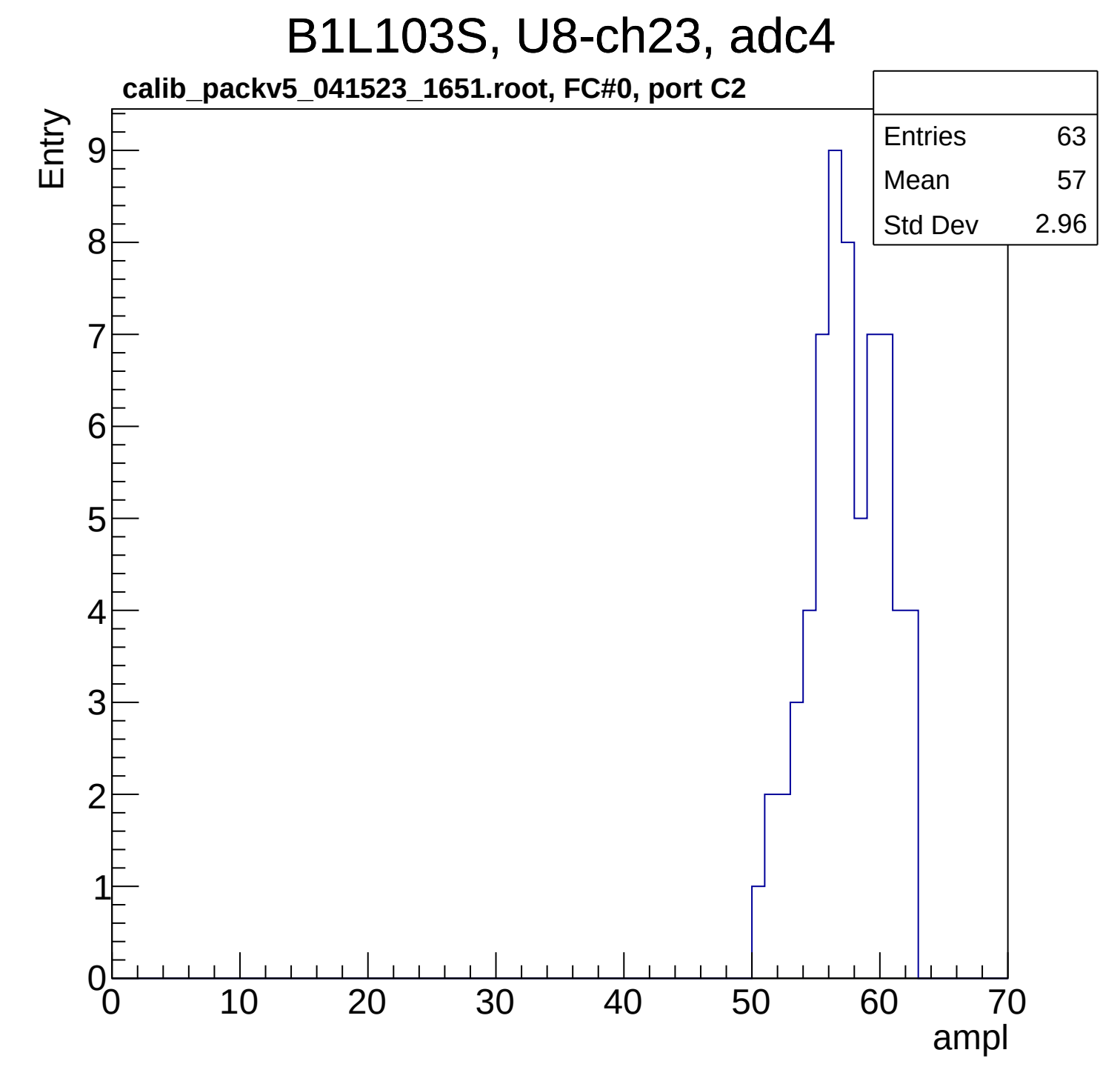
B1L103S, U8-ch23, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 57
Std Dev 2.96
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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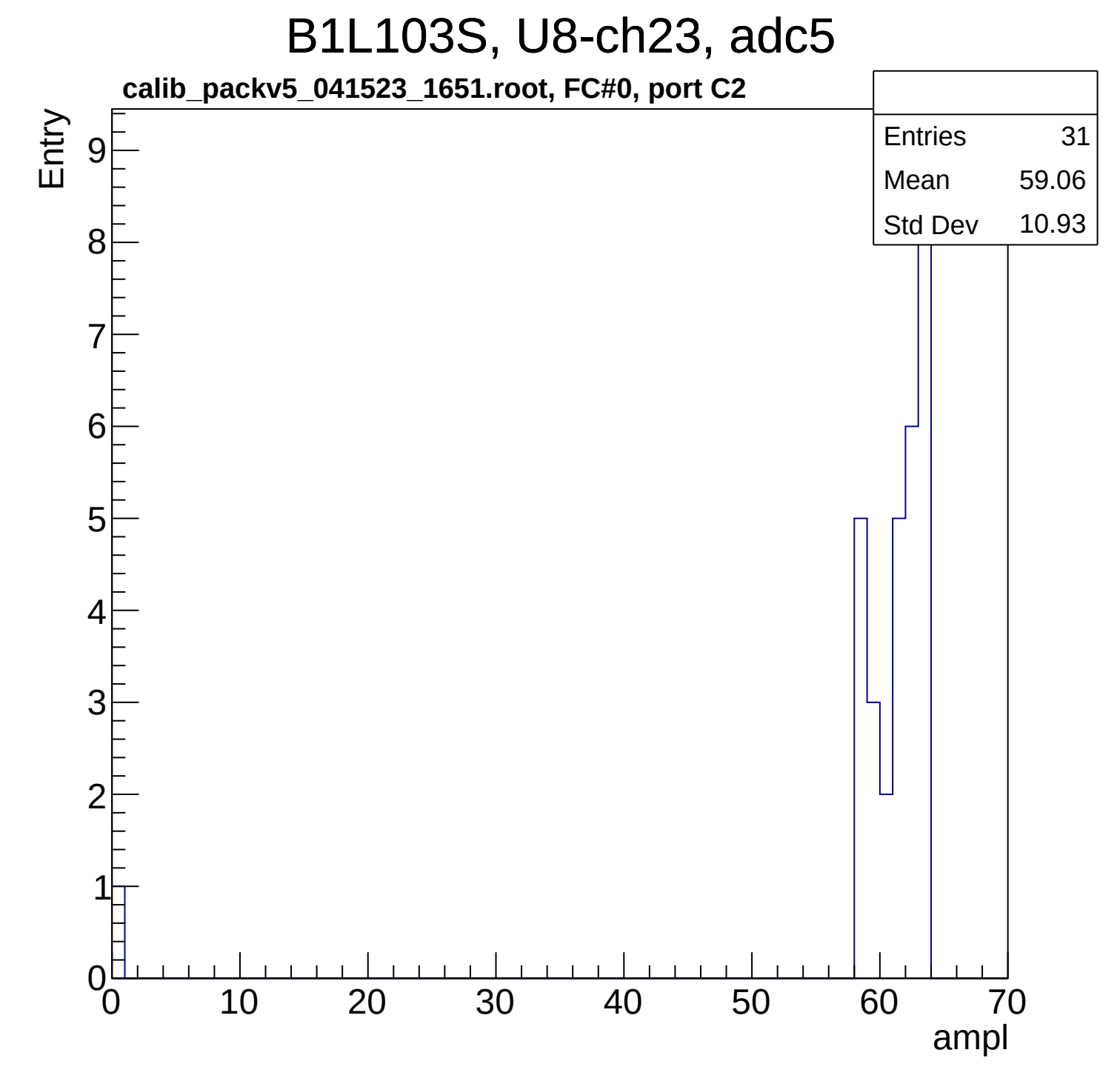
B1L103S, U8-ch23, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 59.06
Std Dev 10.93
Entry
ampl
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3
4
5
6
7
8
9
0
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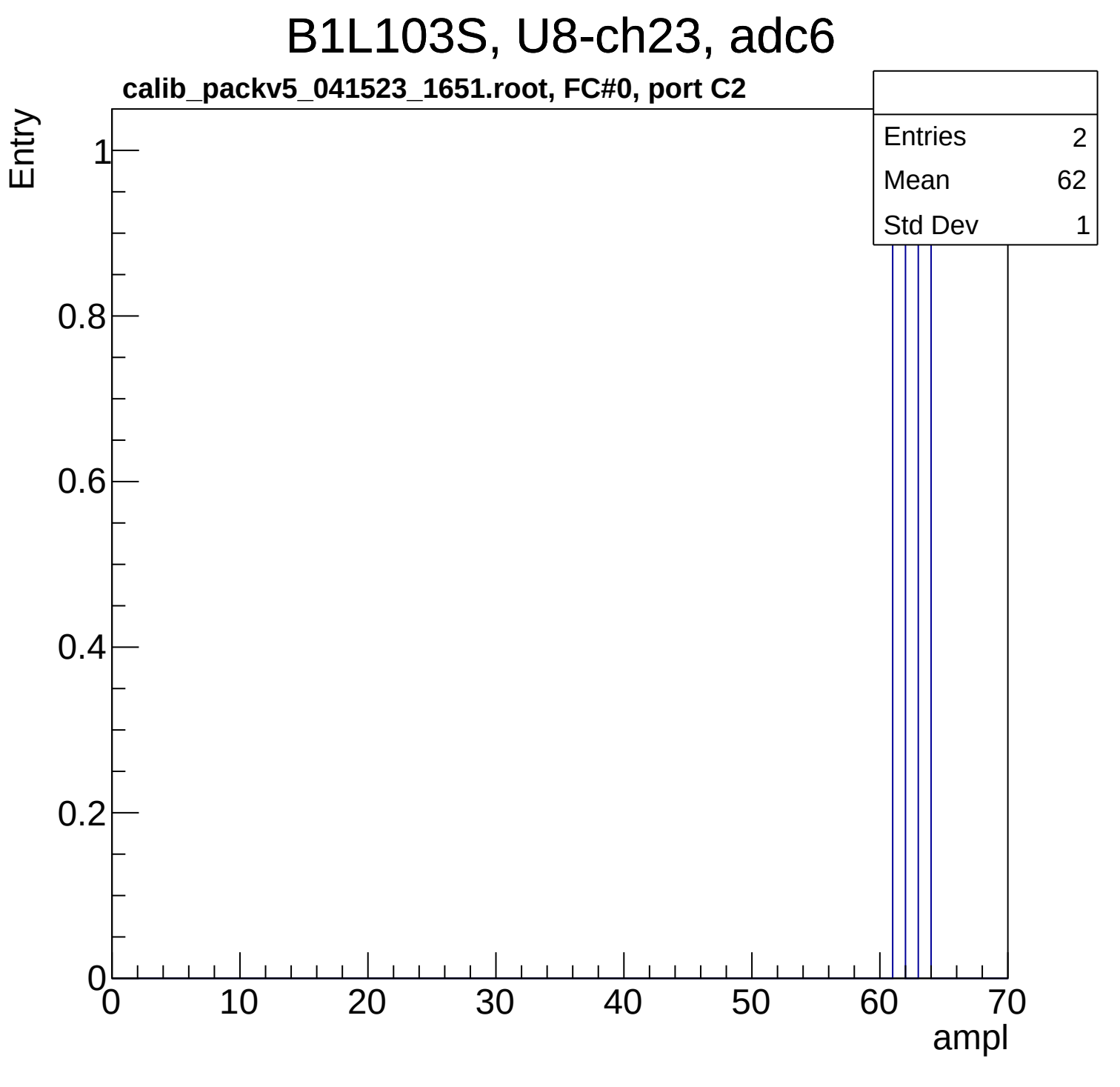
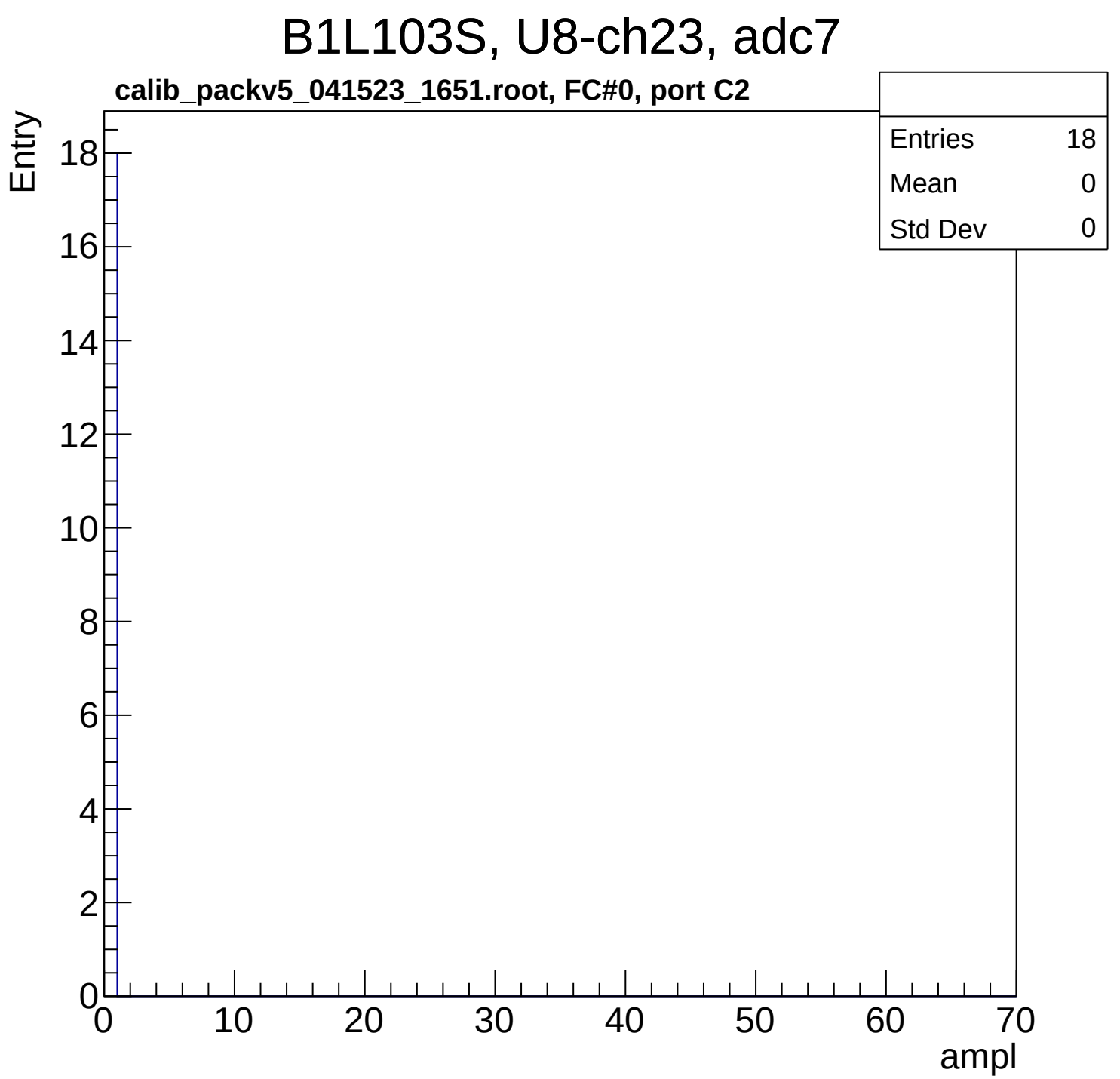

B1L103S, U8-ch23, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 62
Std Dev 1
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B1L103S, U8-ch23, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
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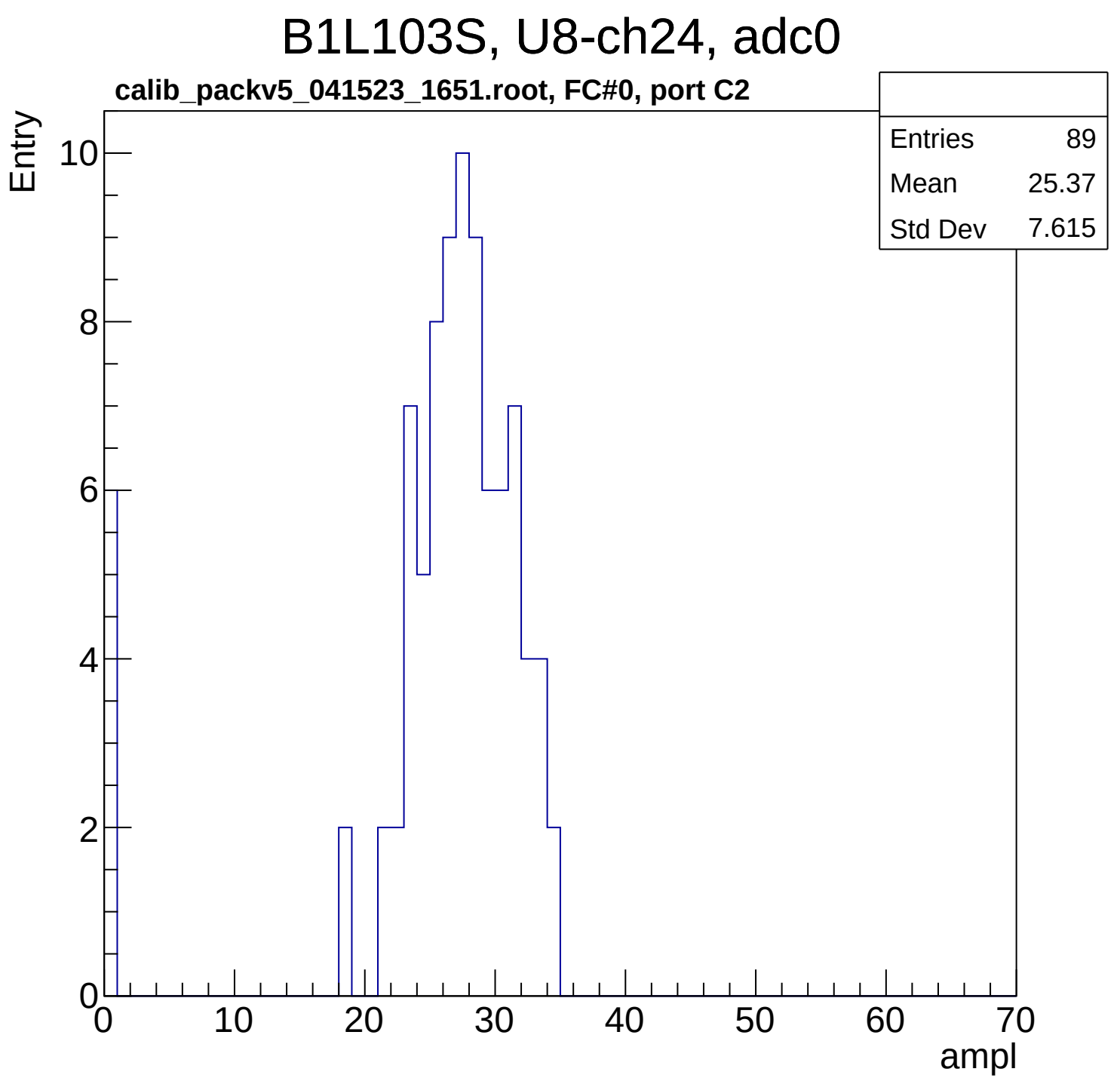
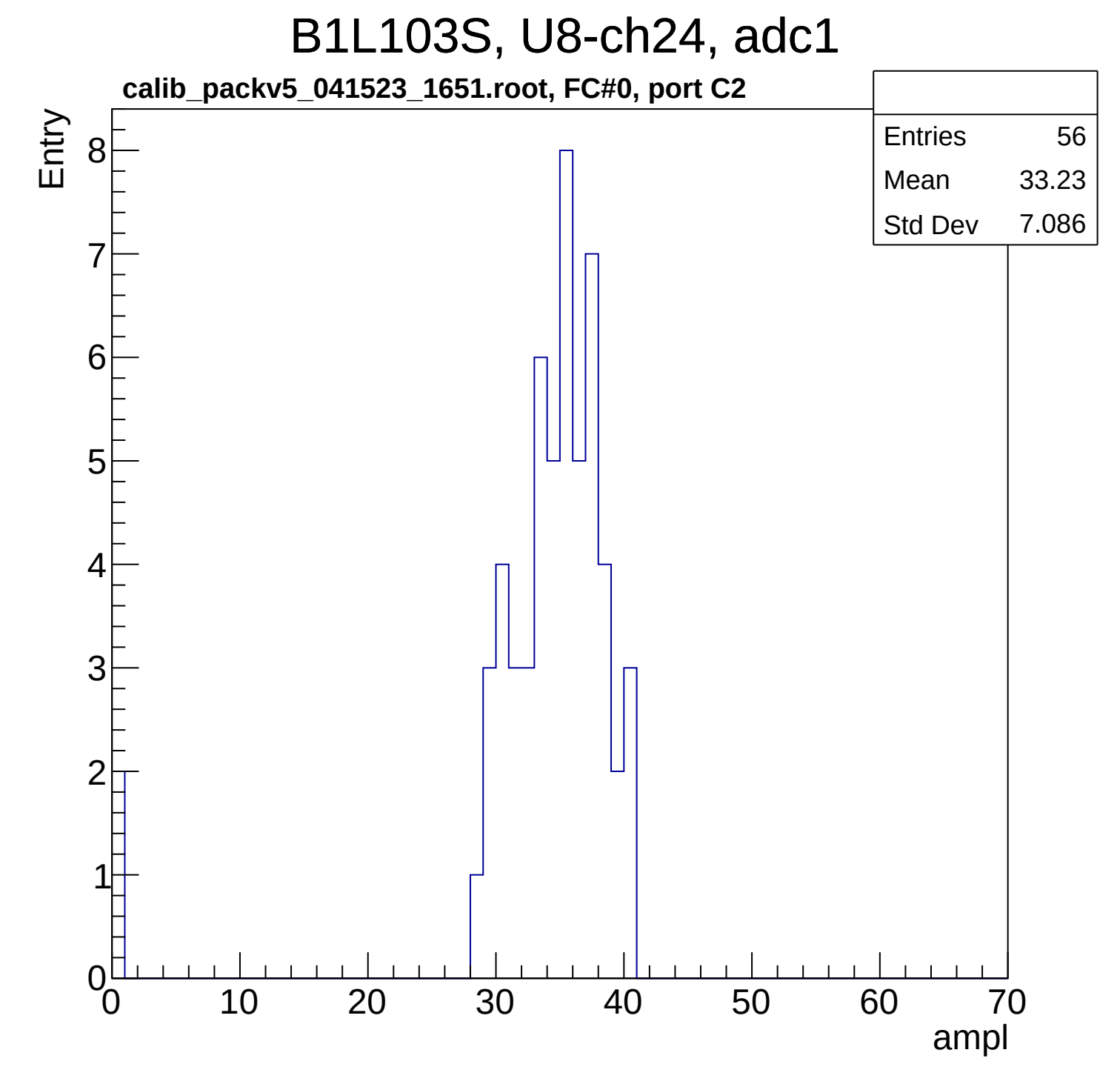
50
60
70
ampl


B1L103S, U8-ch24, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 25.37
Std Dev 7.615
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U8-ch24, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 33.23
Std Dev 7.086
Entry
ampl
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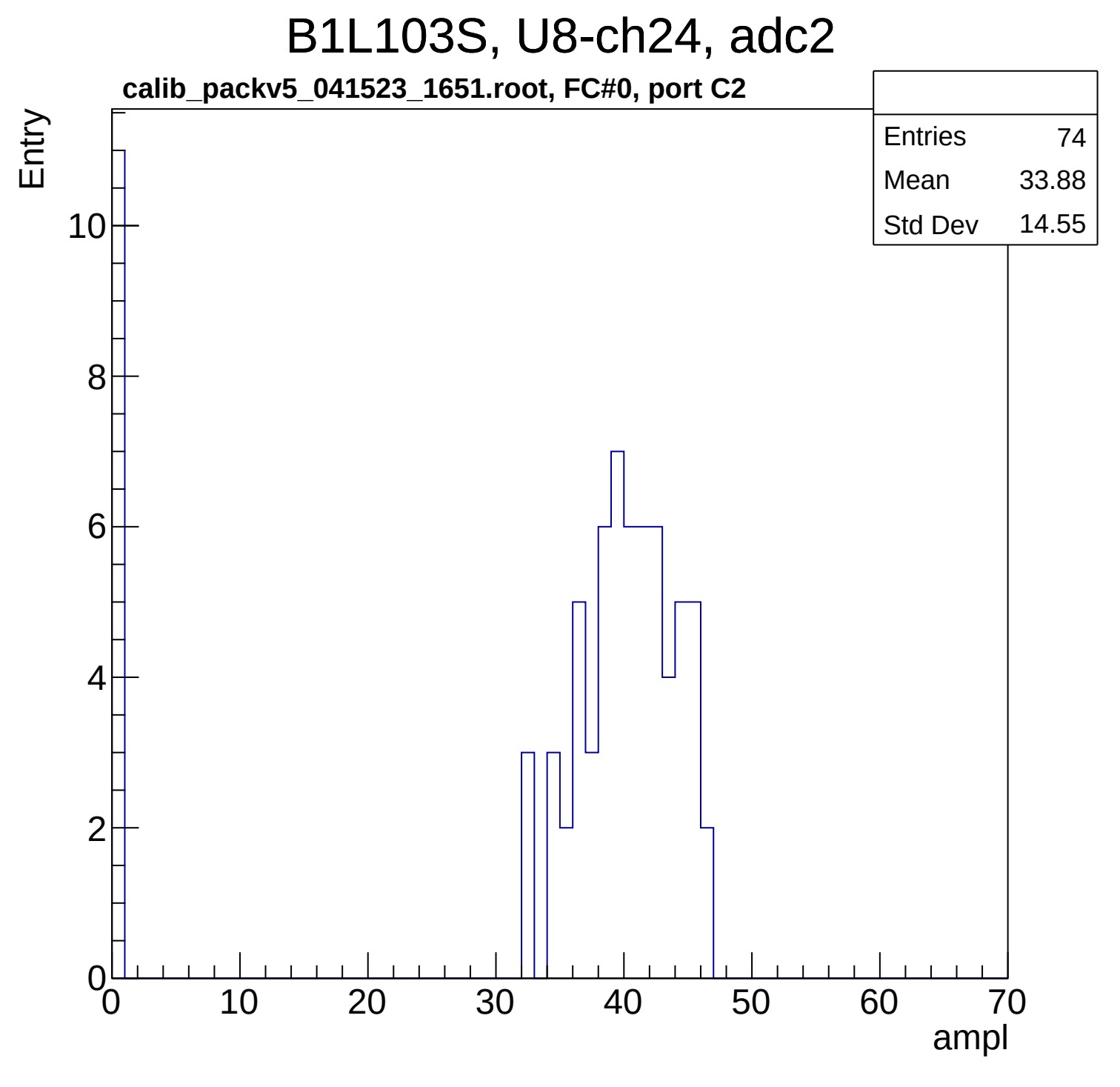
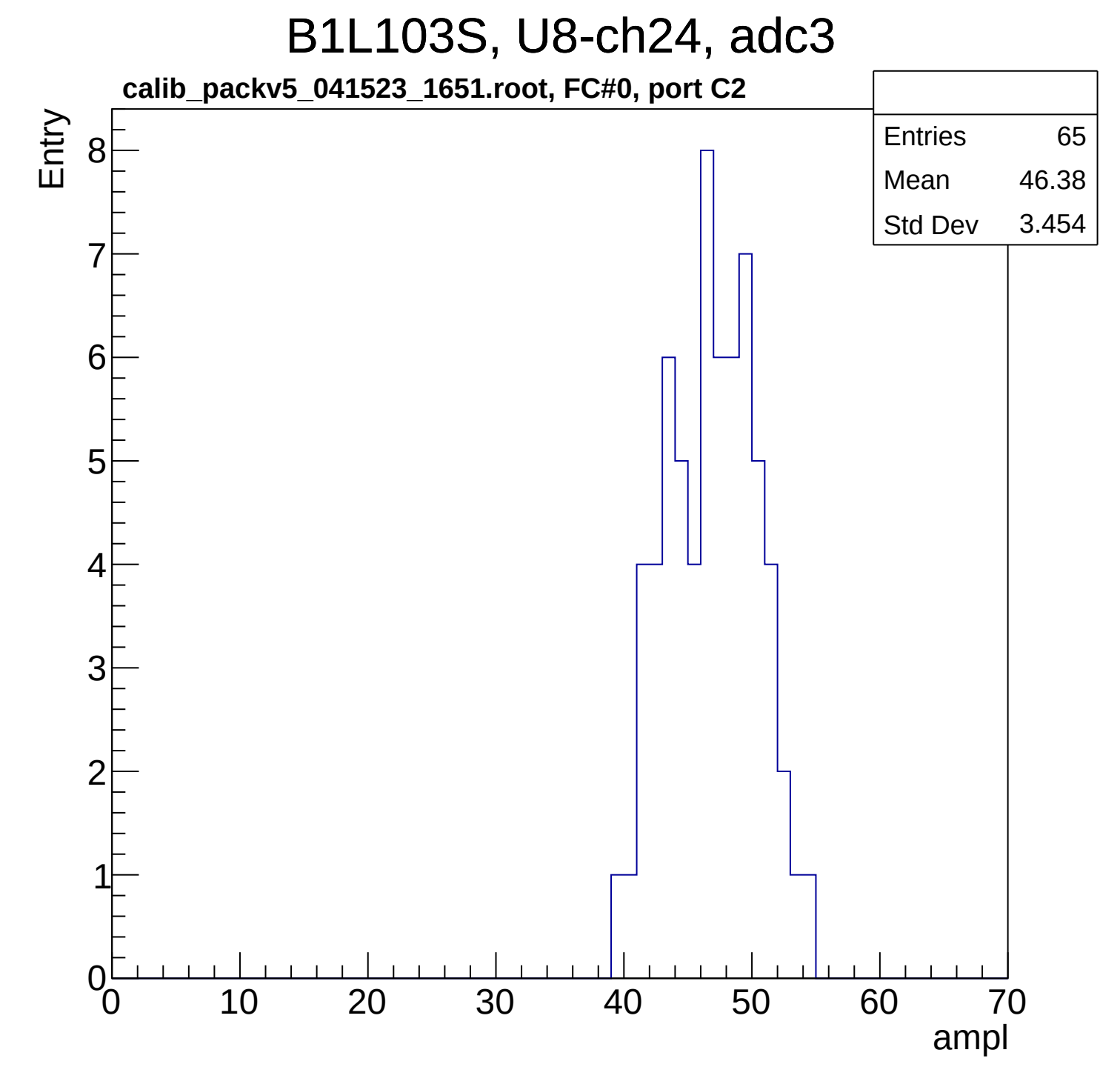
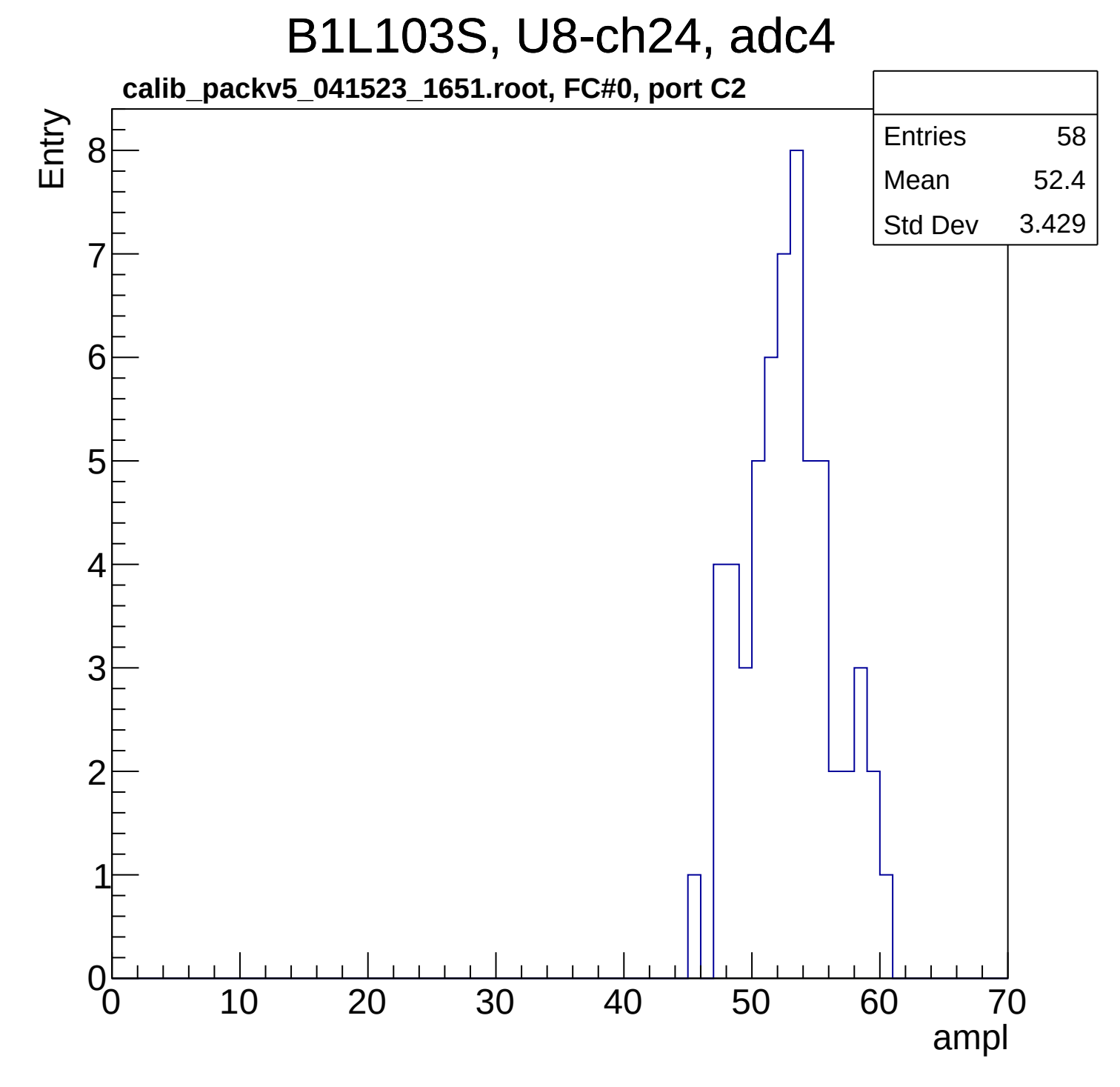
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch24, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 33.88
Std Dev 14.55
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch24, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 46.38
Std Dev 3.454
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch24, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 52.4
Std Dev 3.429
Entry
ampl
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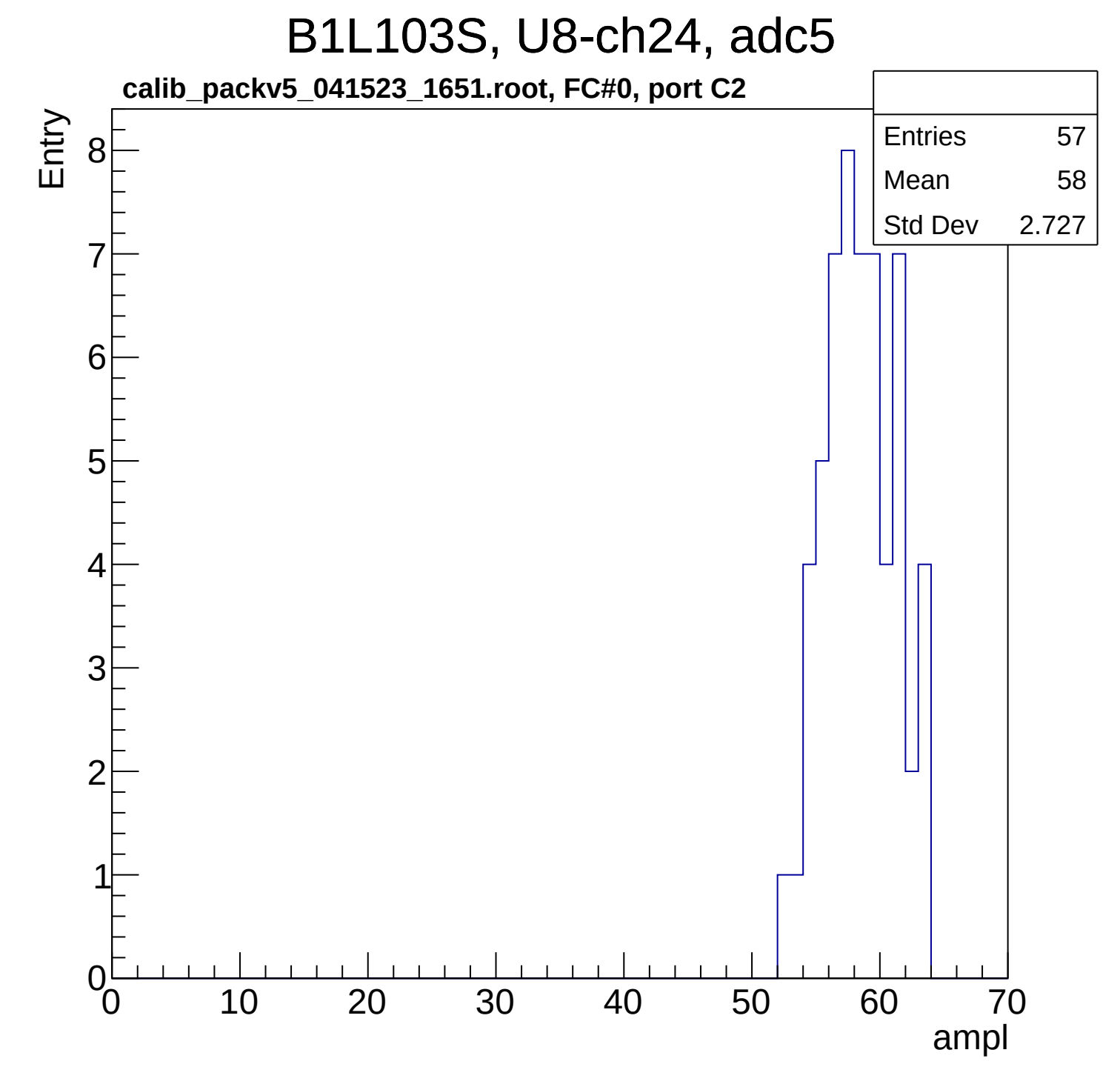
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch24, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 58
Std Dev 2.727
Entry
ampl
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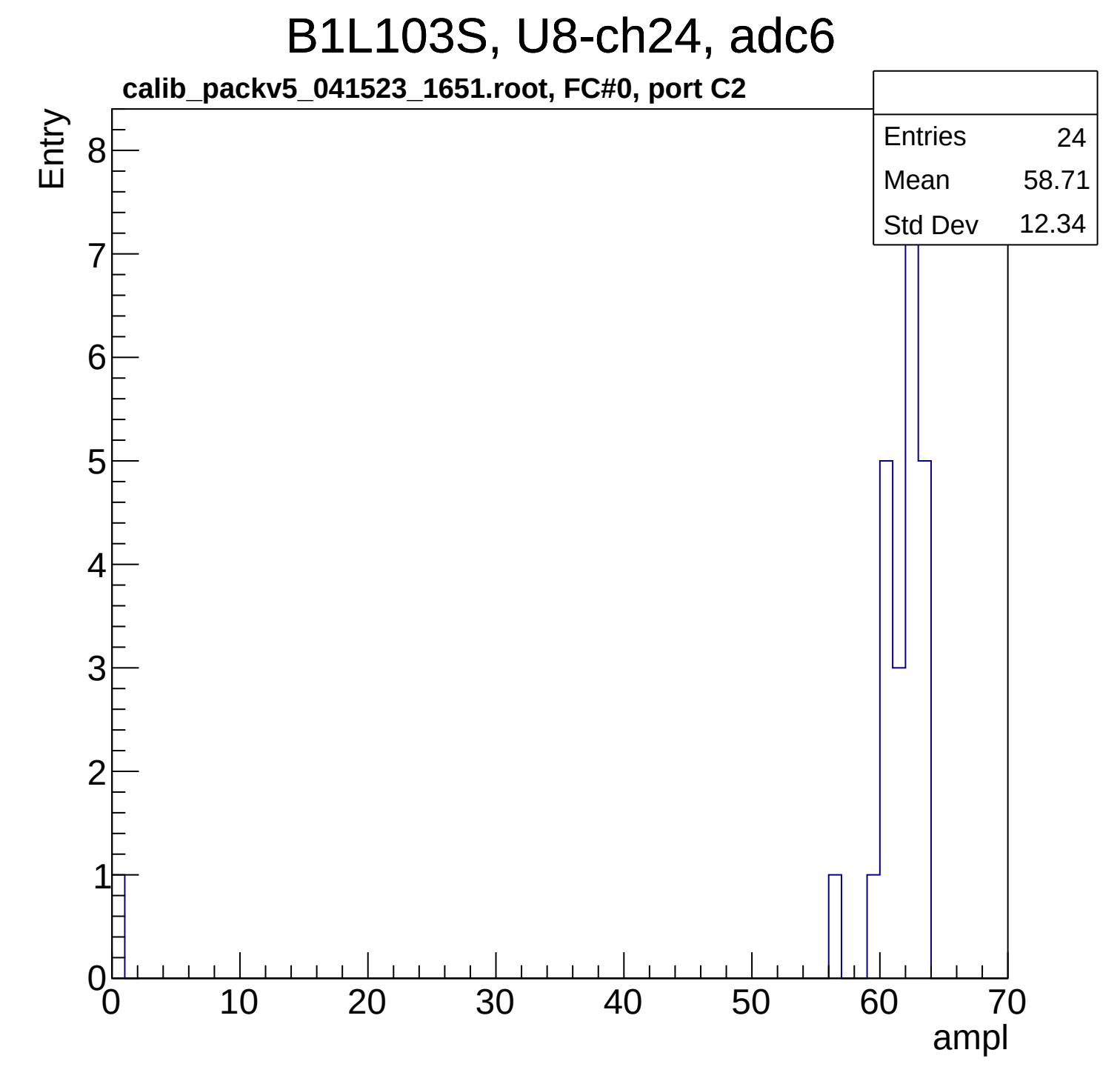
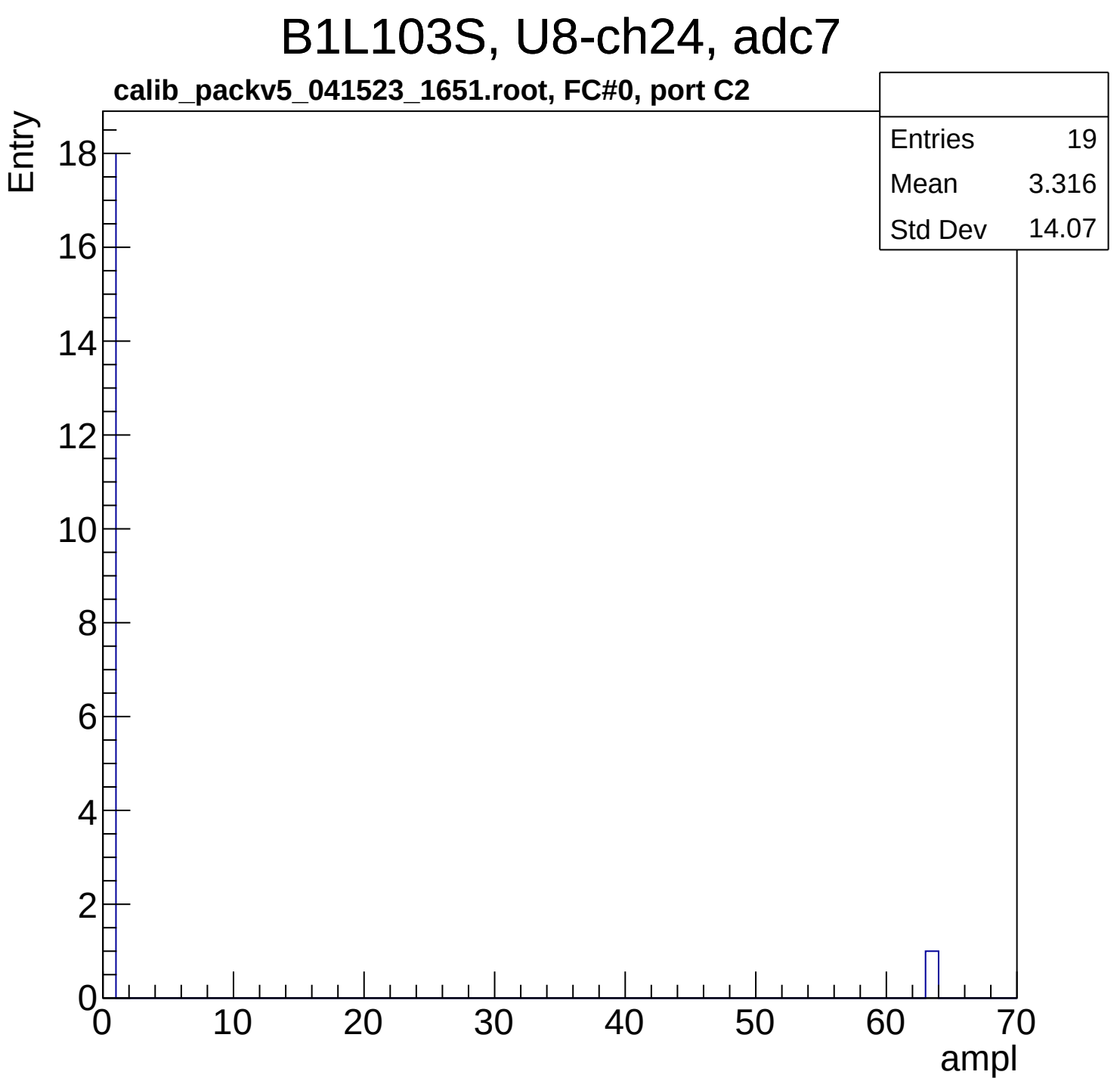
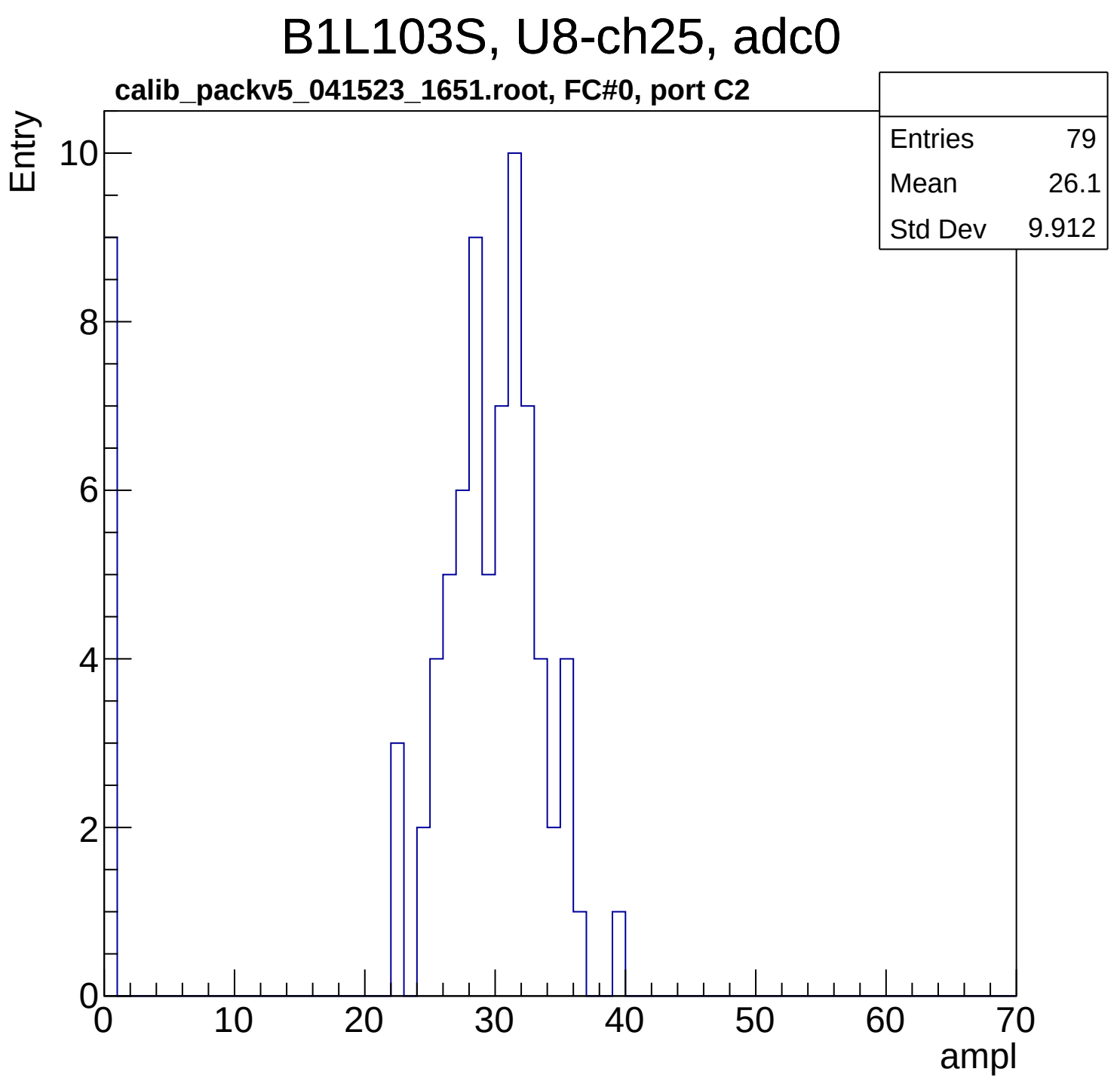
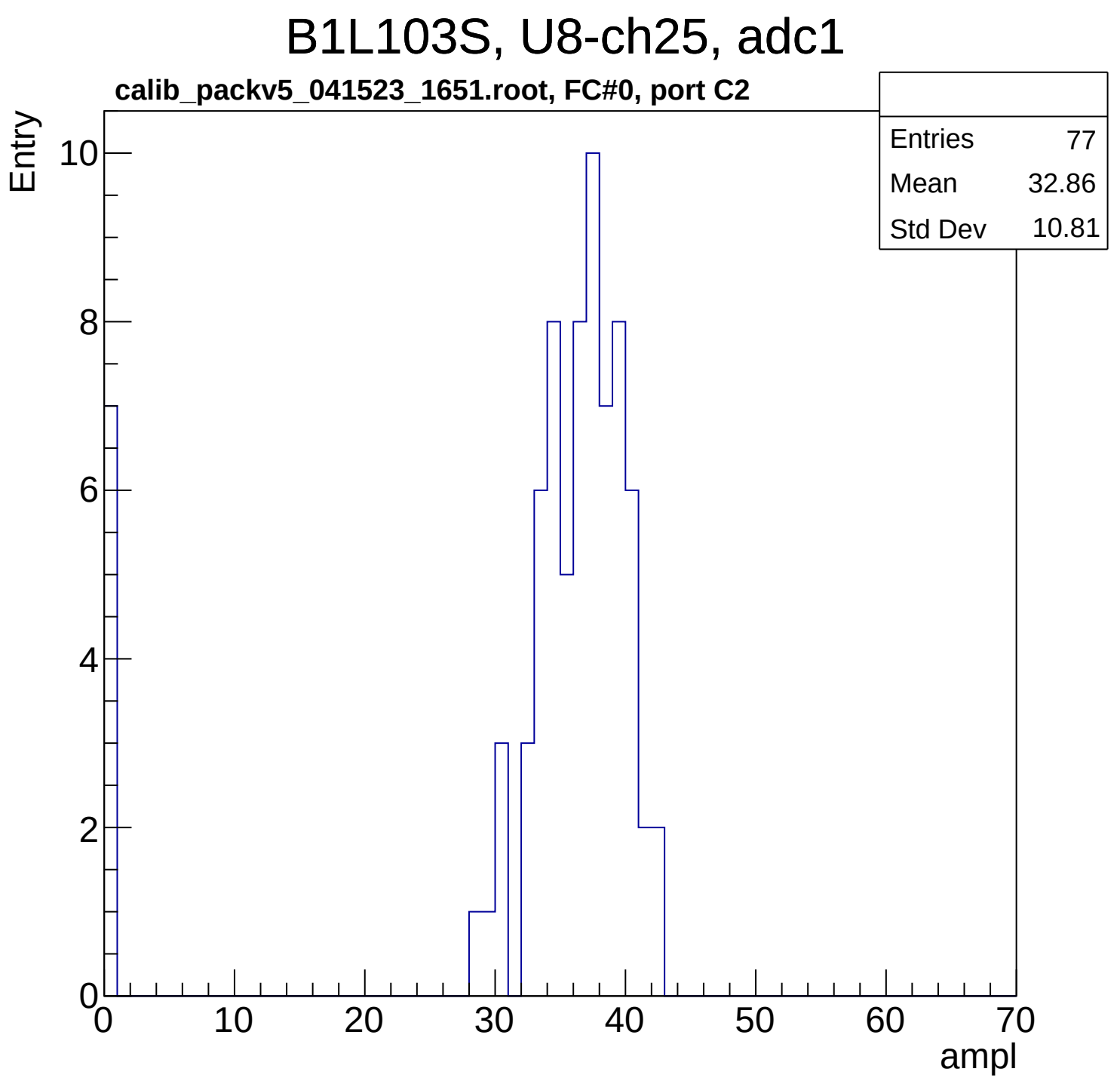
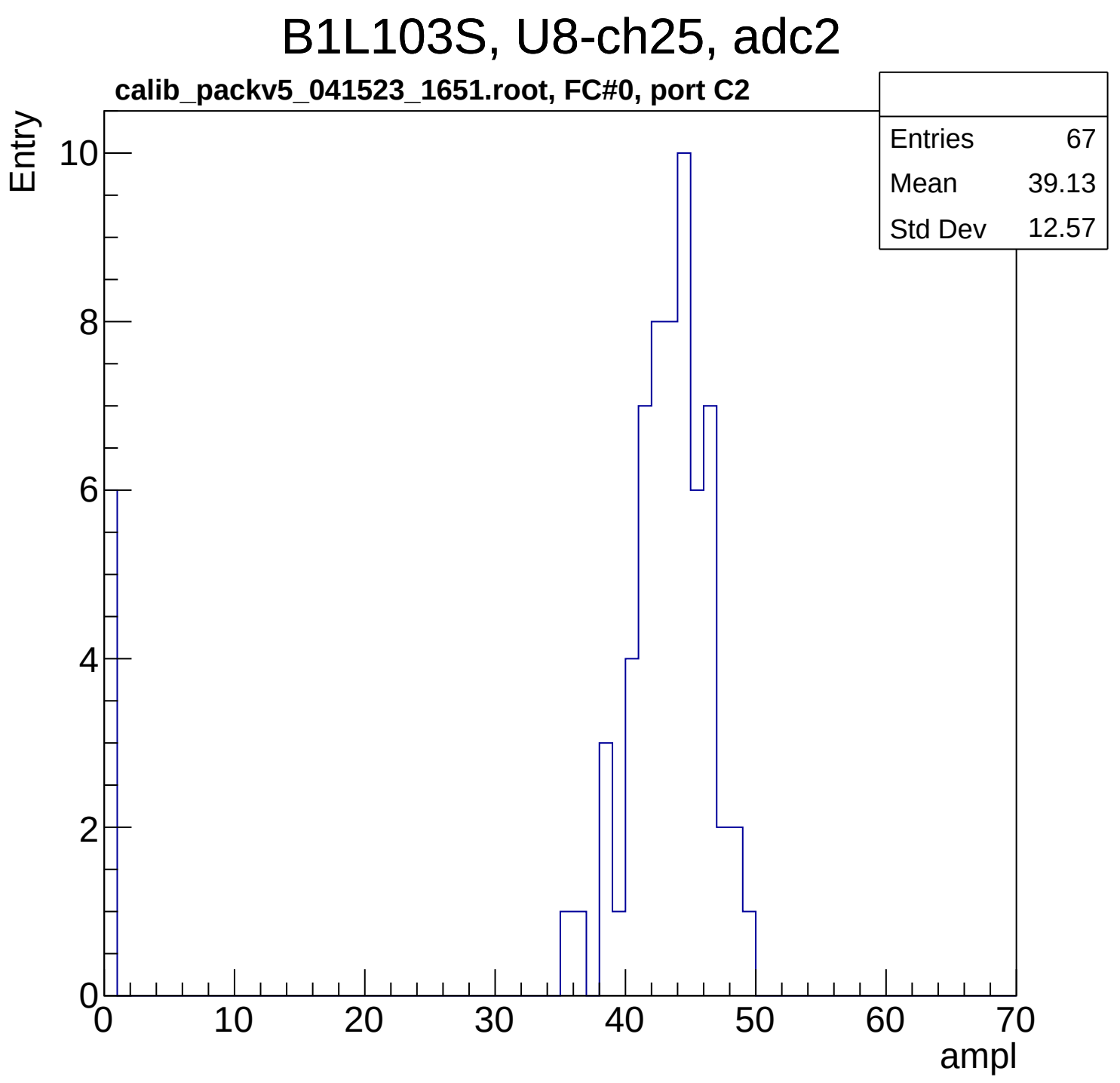
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

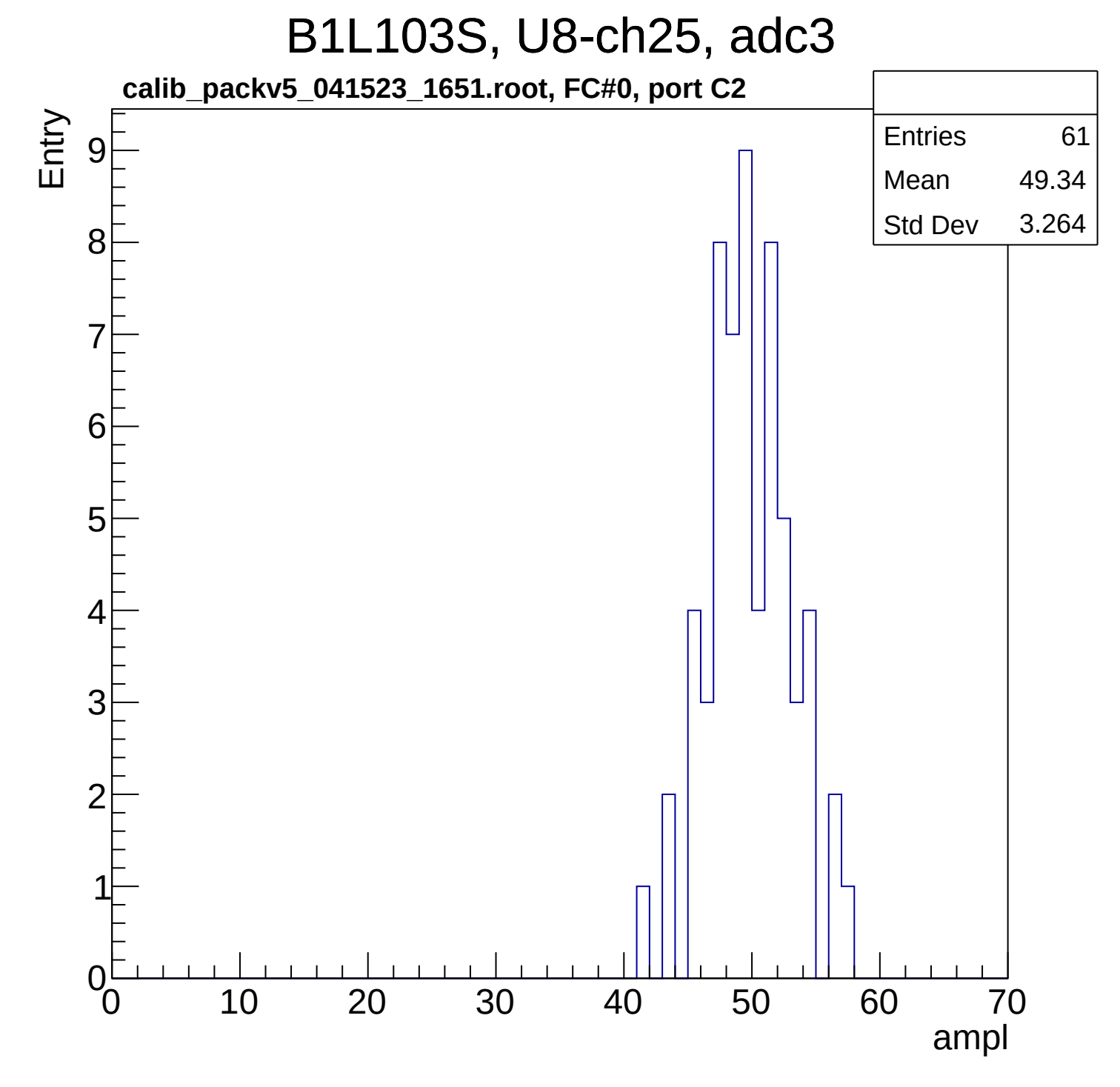

B1L103S, U8-ch24, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 58.71
Std Dev 12.34
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

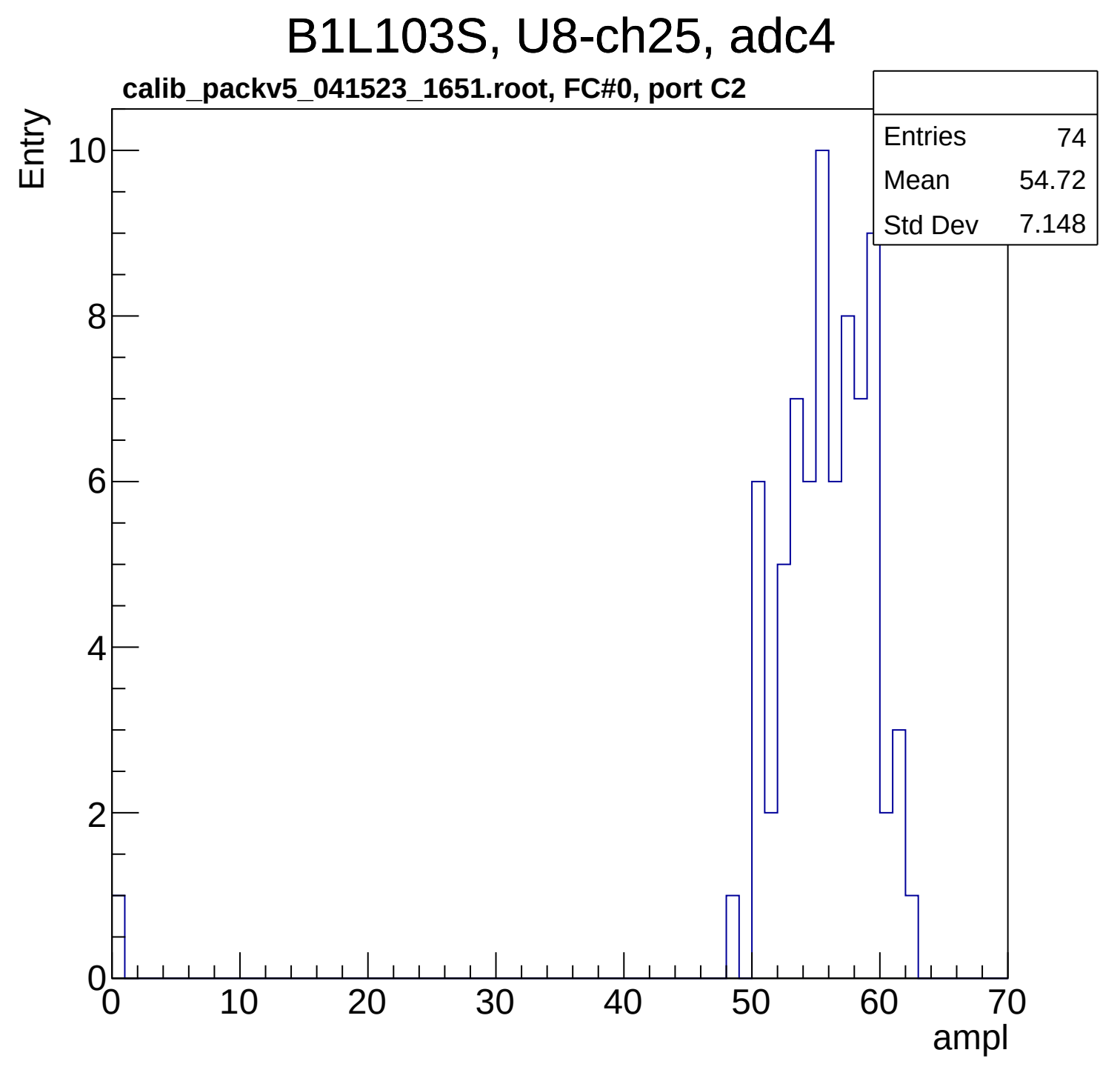

B1L103S, U8-ch24, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.316
Std Dev 14.07
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

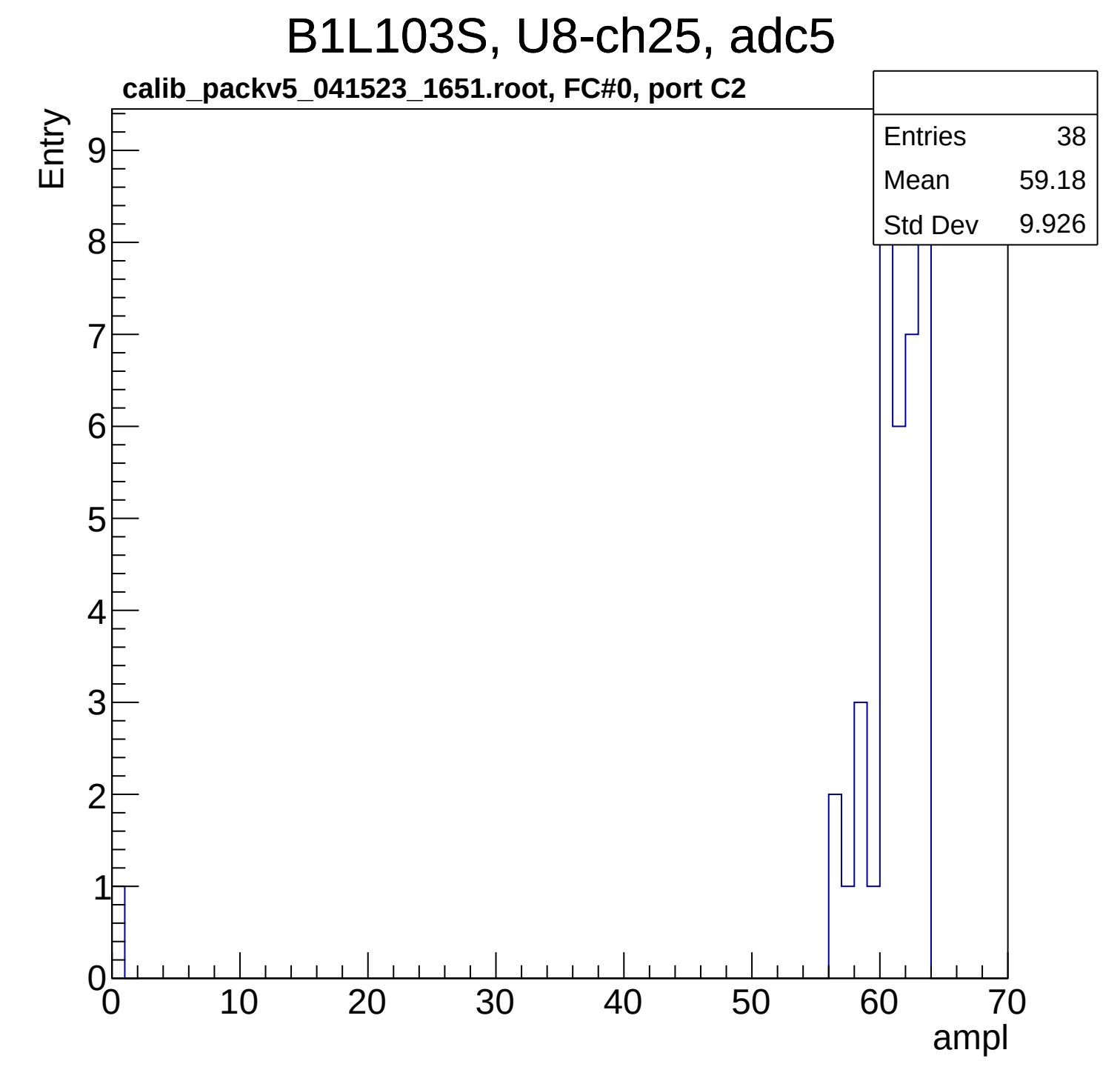

B1L103S, U8-ch25, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 26.1
Std Dev 9.912
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U8-ch25, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 32.86
Std Dev 10.81
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch25, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 39.13
Std Dev 12.57
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U8-ch25, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 49.34
Std Dev 3.264
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U8-ch25, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 54.72
Std Dev 7.148
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U8-ch25, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 59.18
Std Dev 9.926
Entry
ampl
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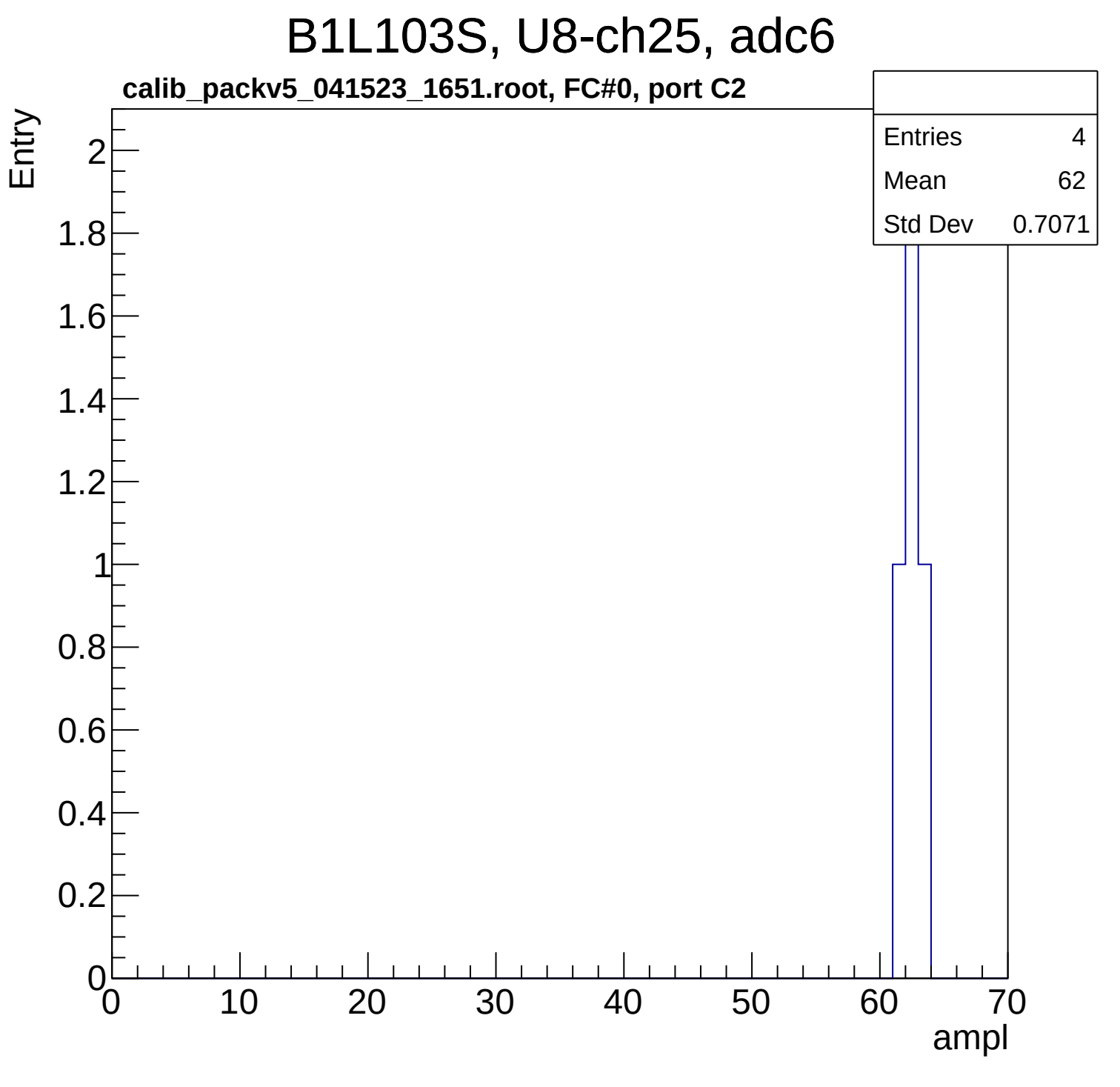
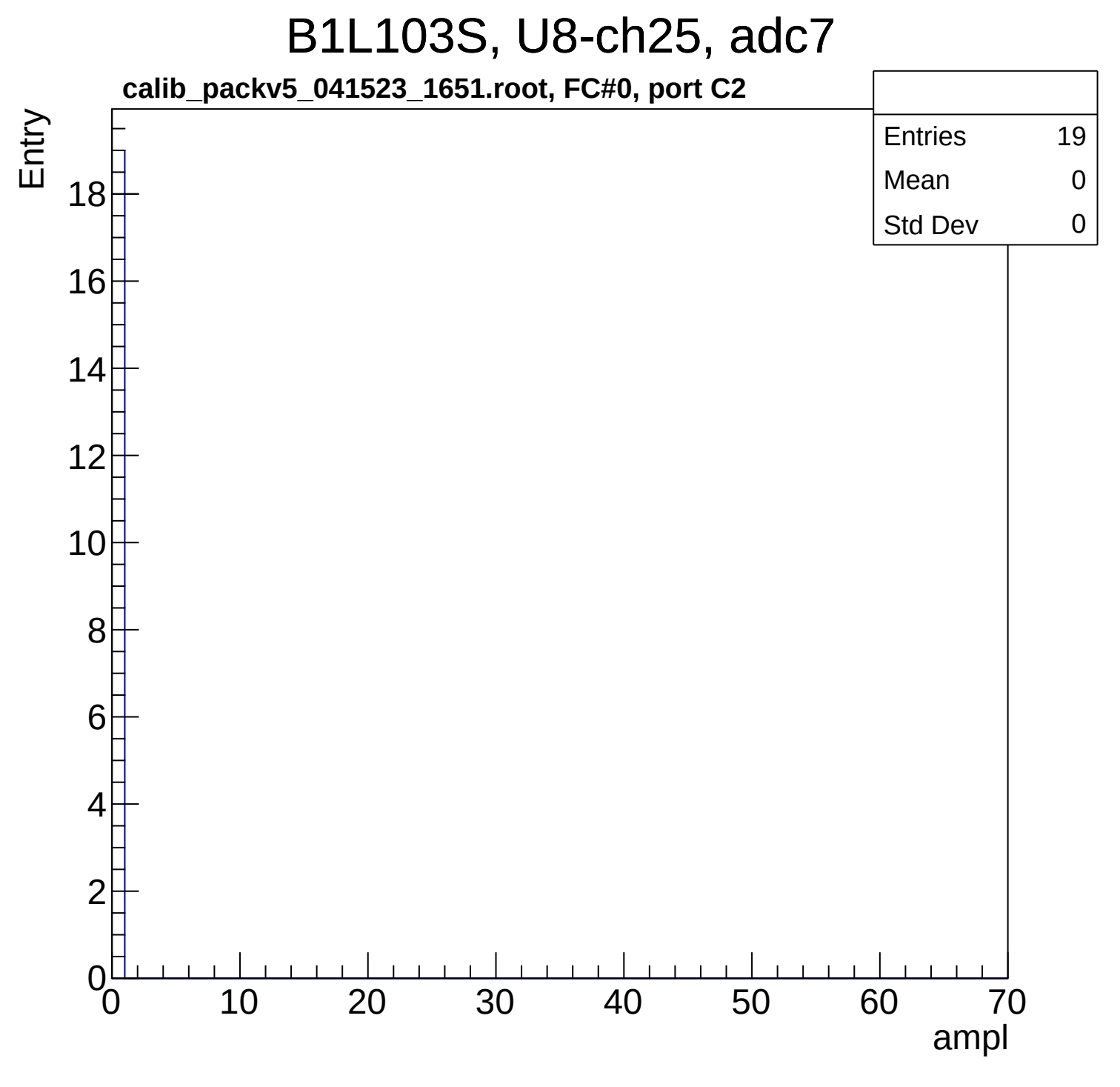
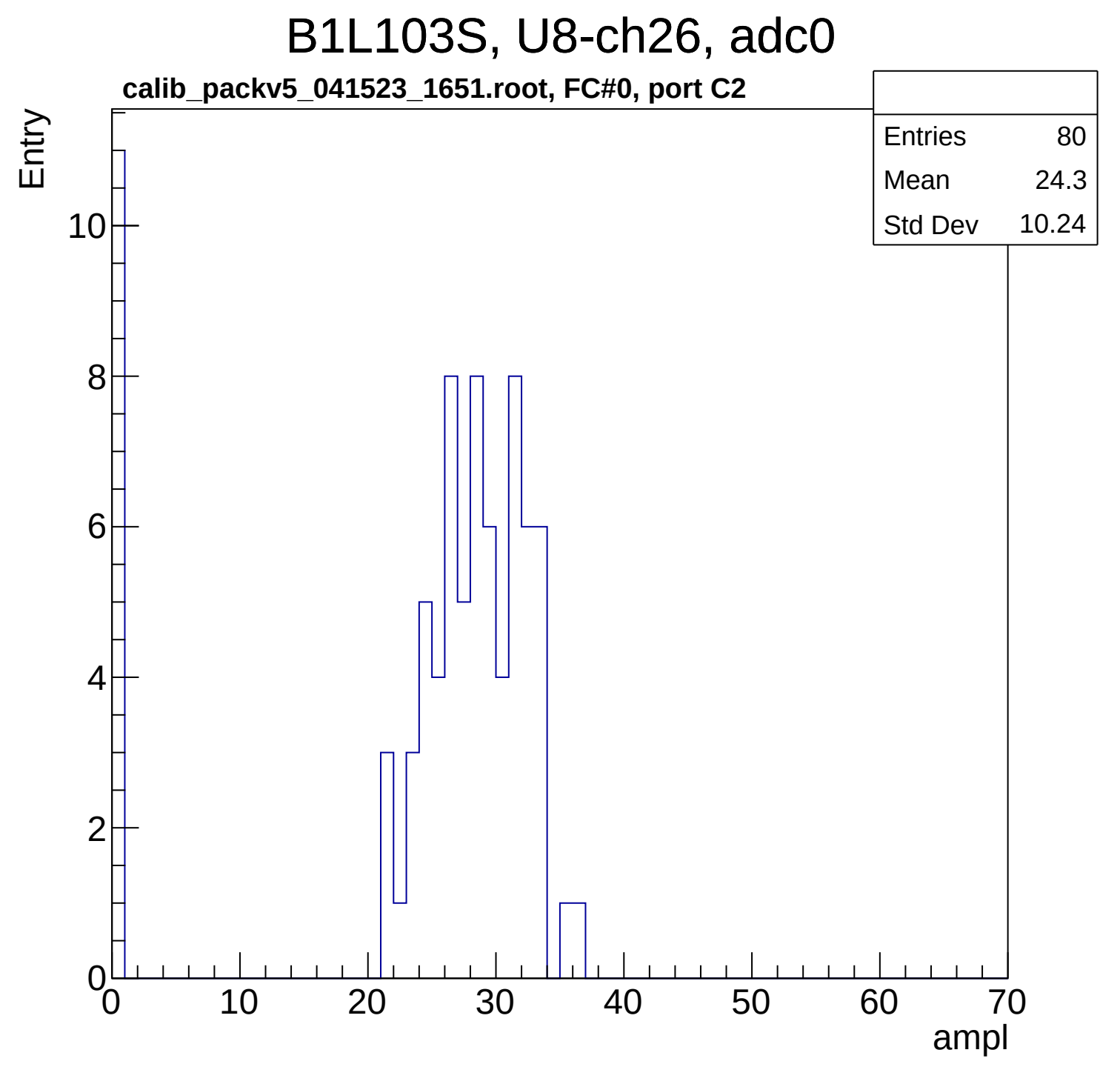
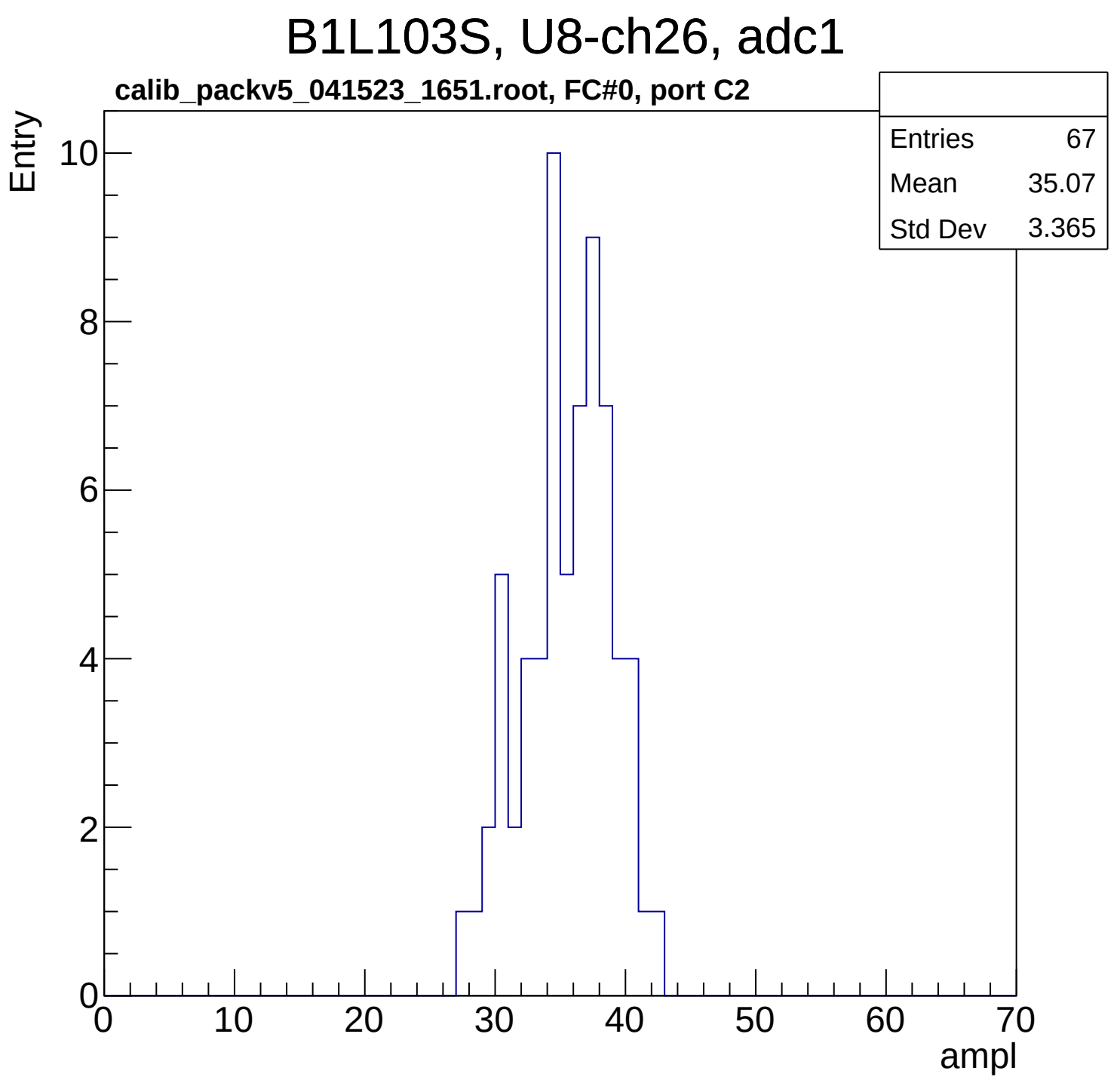
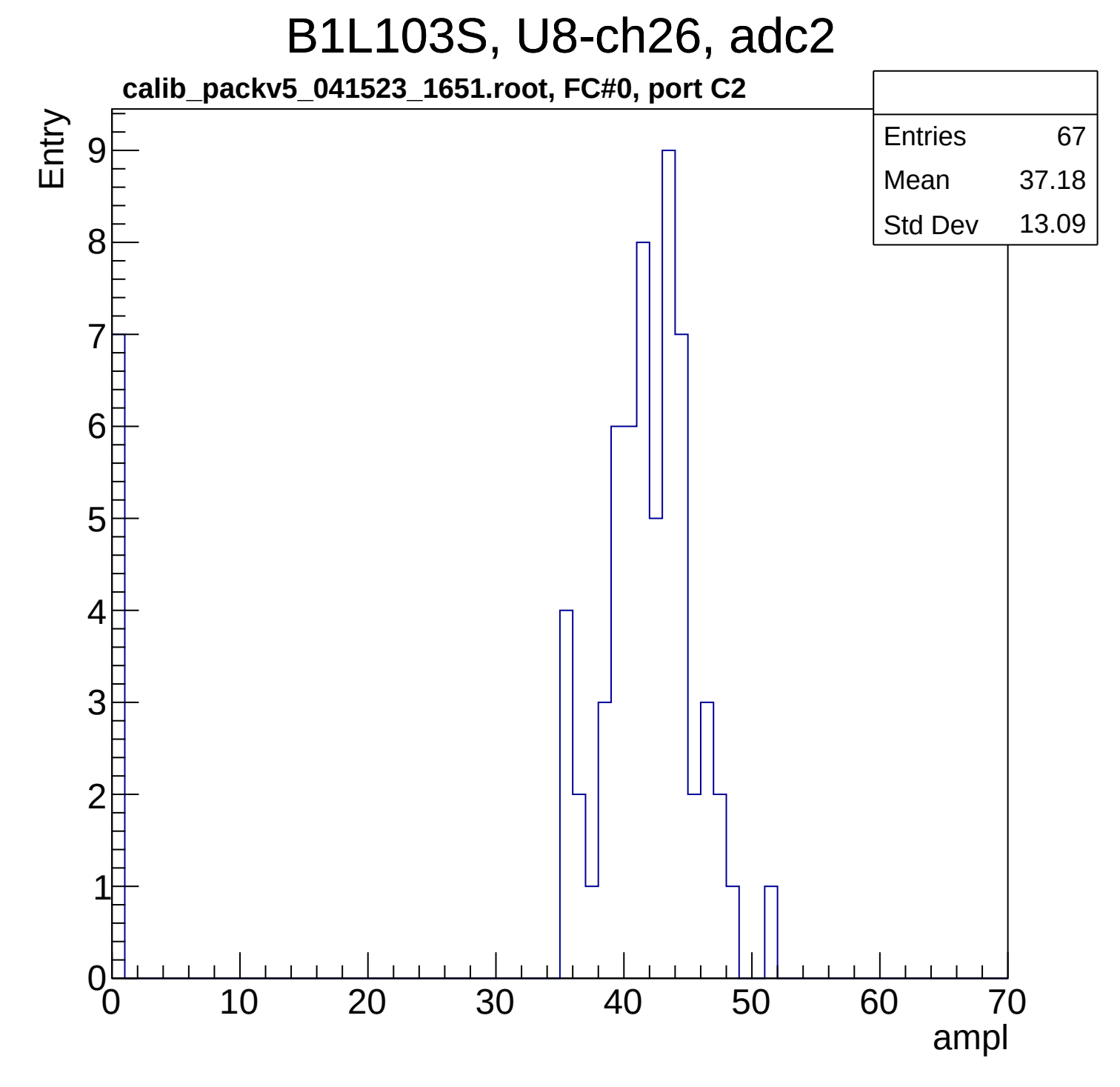
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

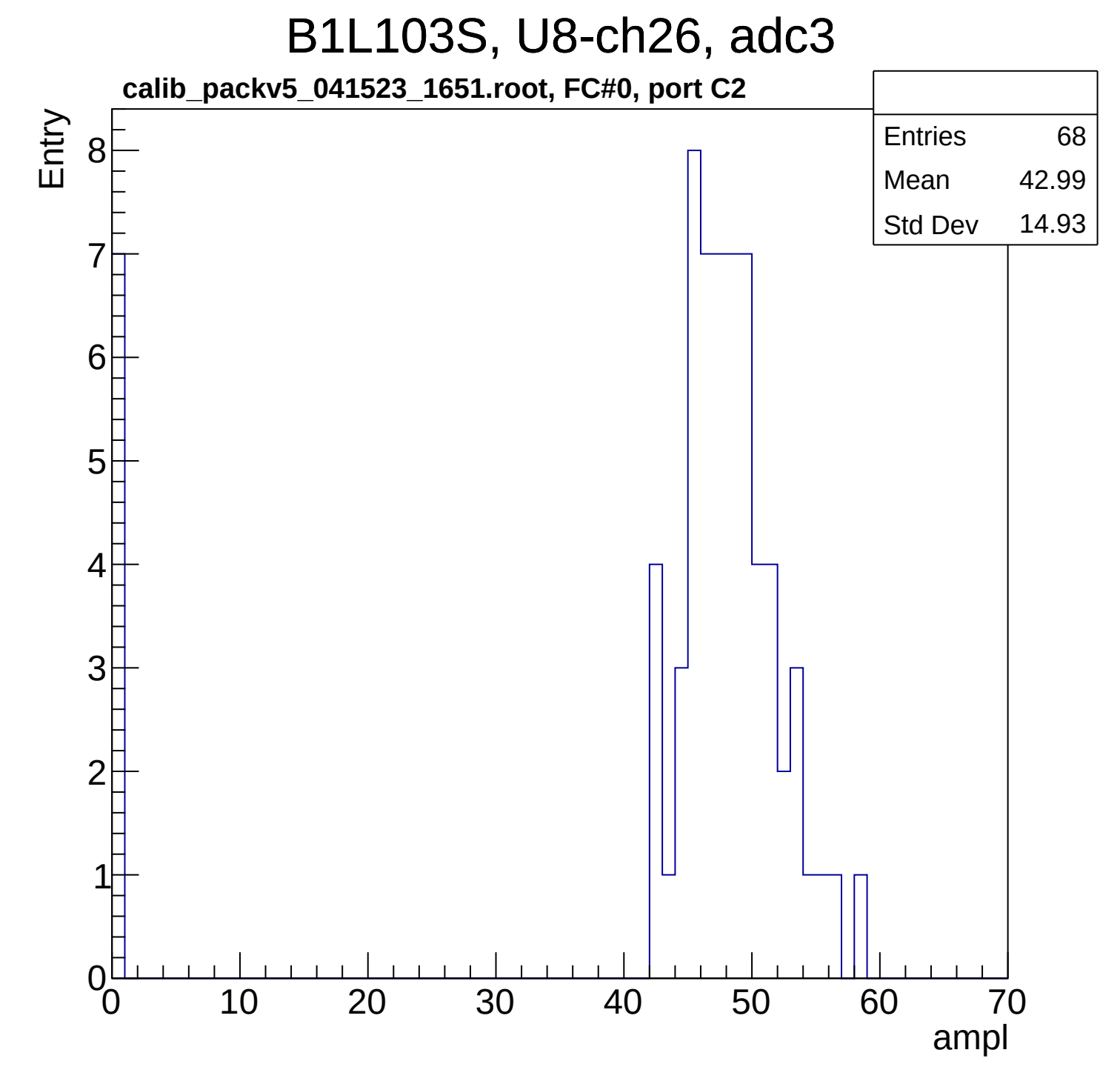

B1L103S, U8-ch25, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 62
Std Dev 0.7071
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U8-ch25, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch26, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 24.3
Std Dev 10.24
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch26, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 35.07
Std Dev 3.365
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U8-ch26, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 37.18
Std Dev 13.09
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U8-ch26, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 42.99
Std Dev 14.93
Entry
ampl
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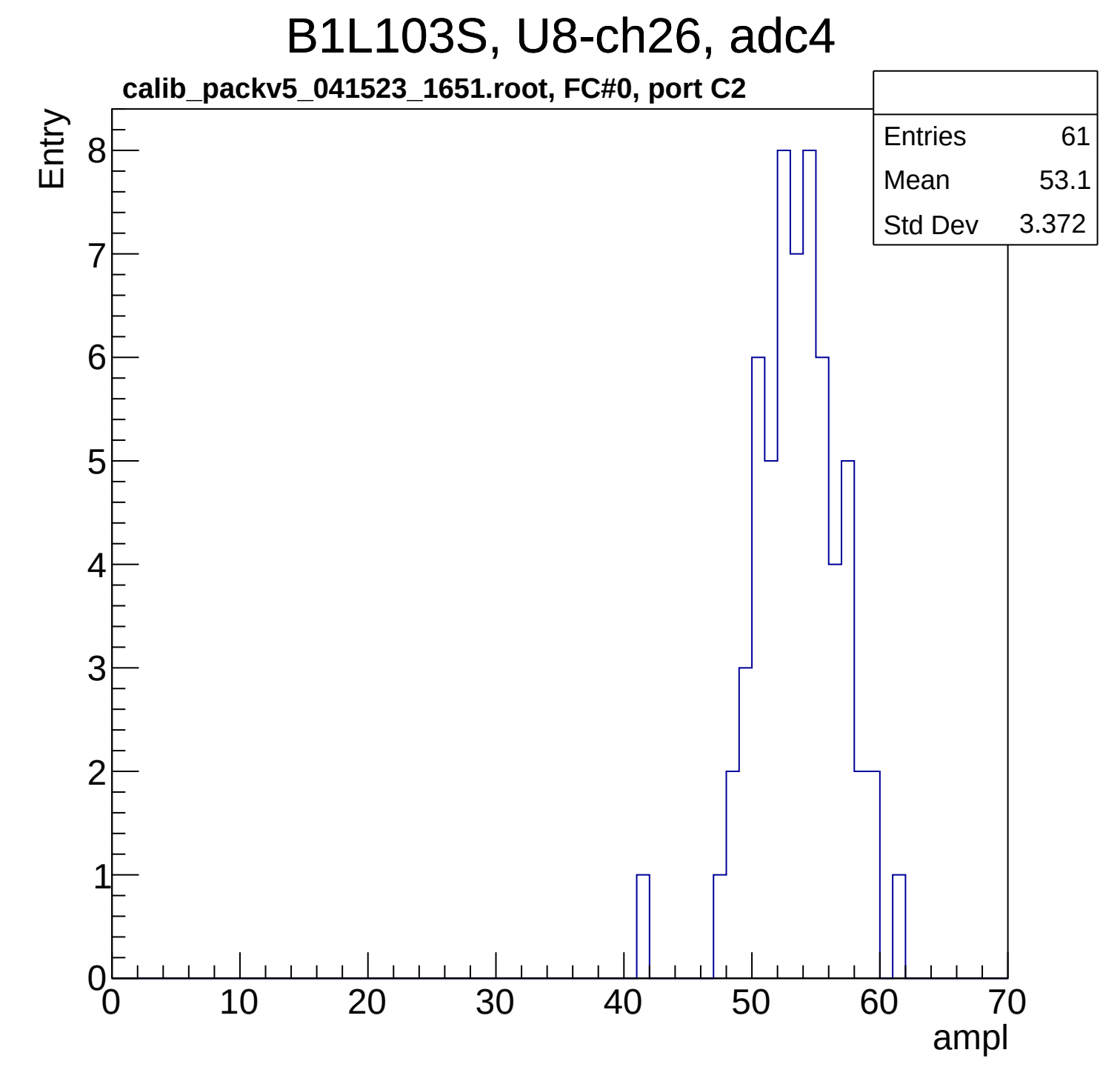
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch26, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 53.1
Std Dev 3.372
Entry
ampl
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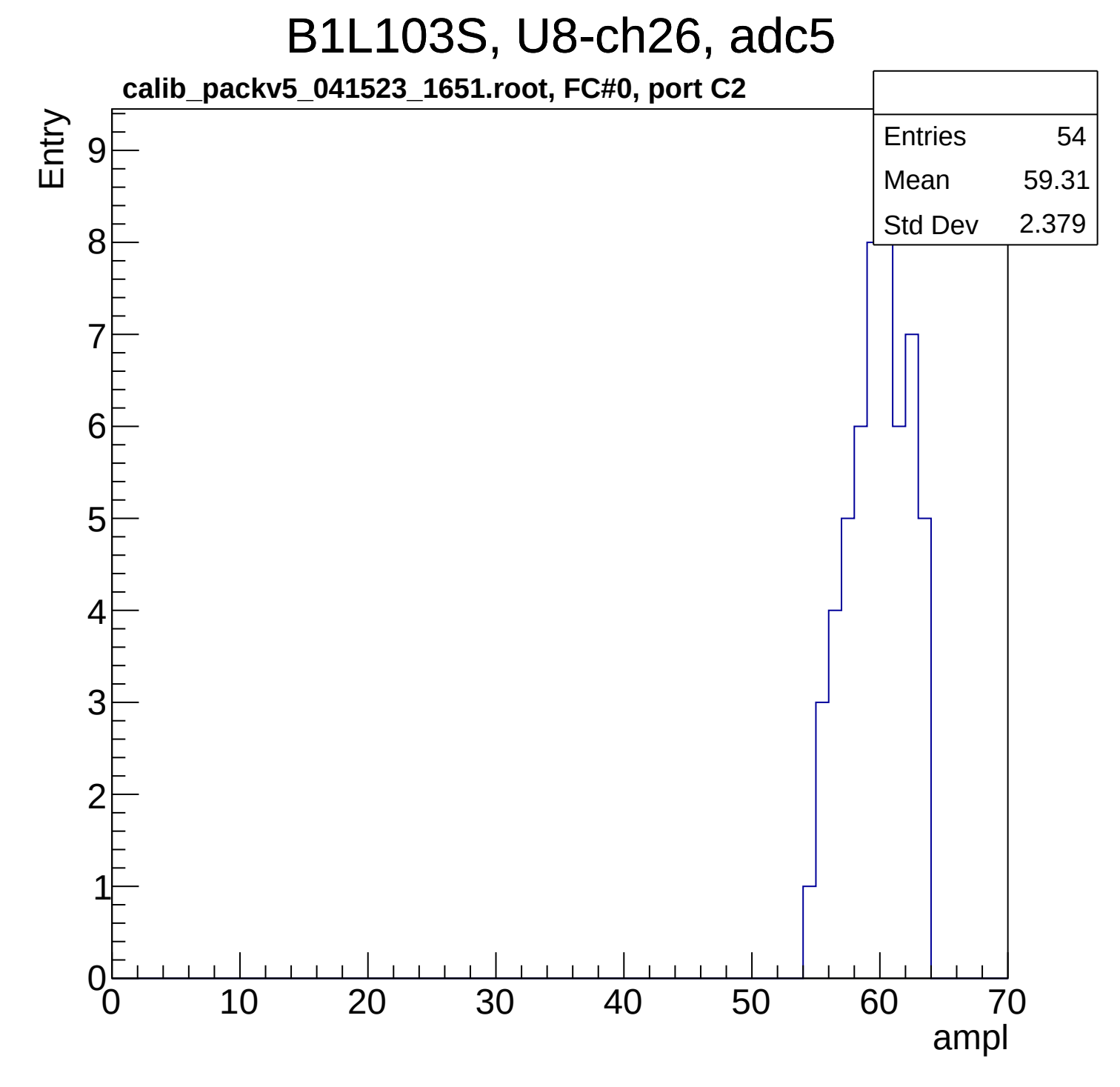
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch26, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 59.31
Std Dev 2.379
Entry
ampl
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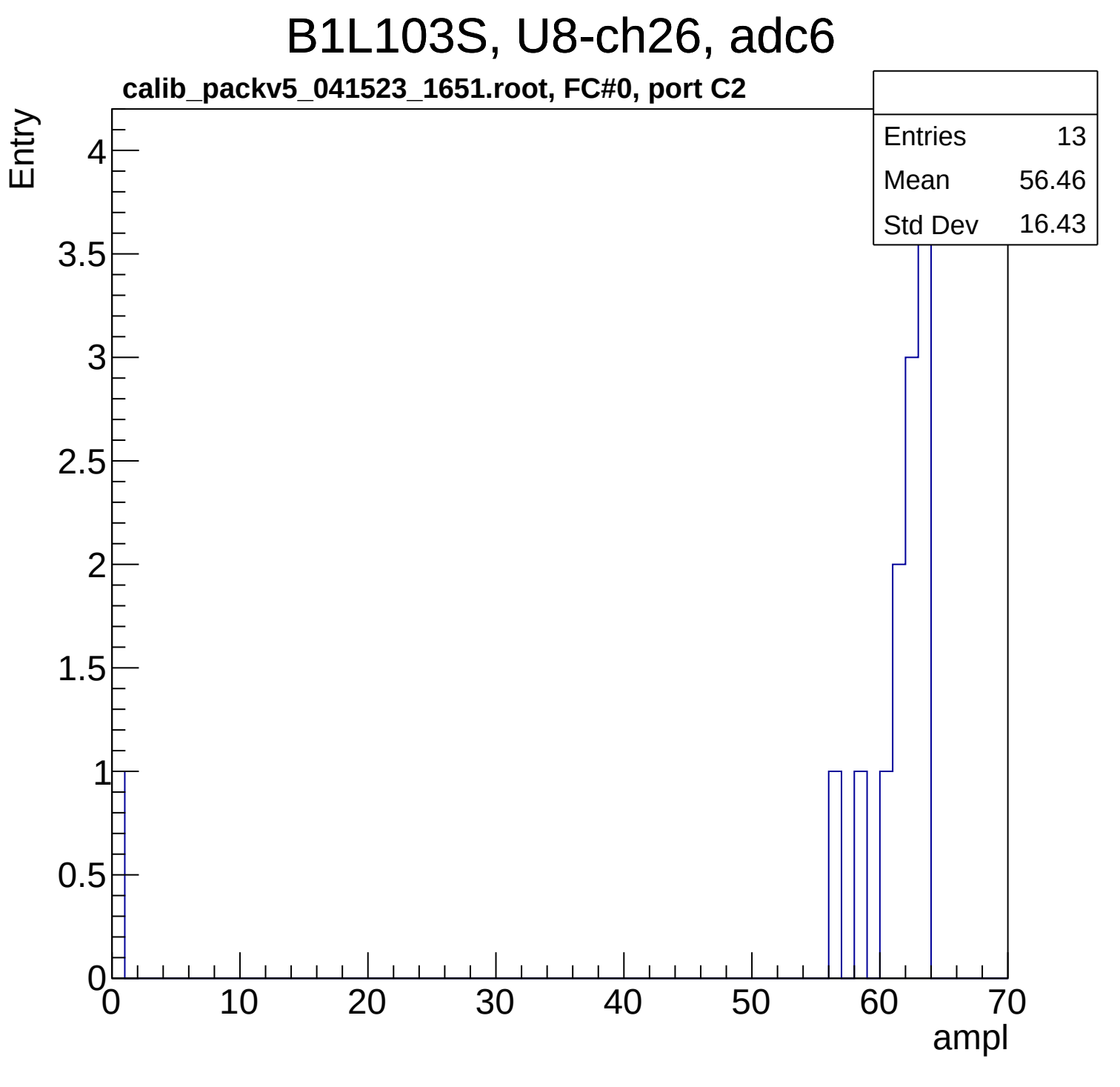
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U8-ch26, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 56.46
Std Dev 16.43
Entry
ampl
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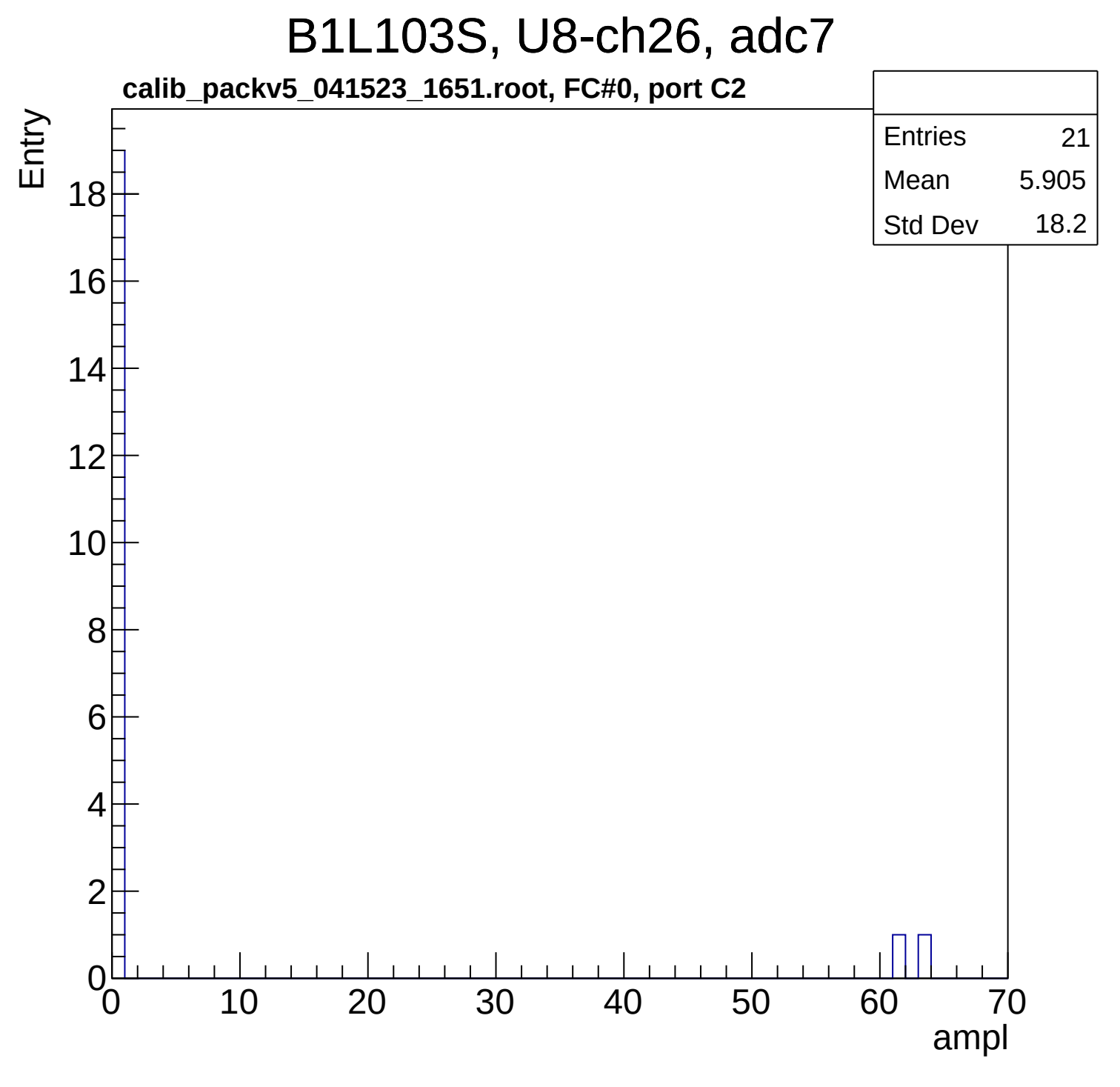
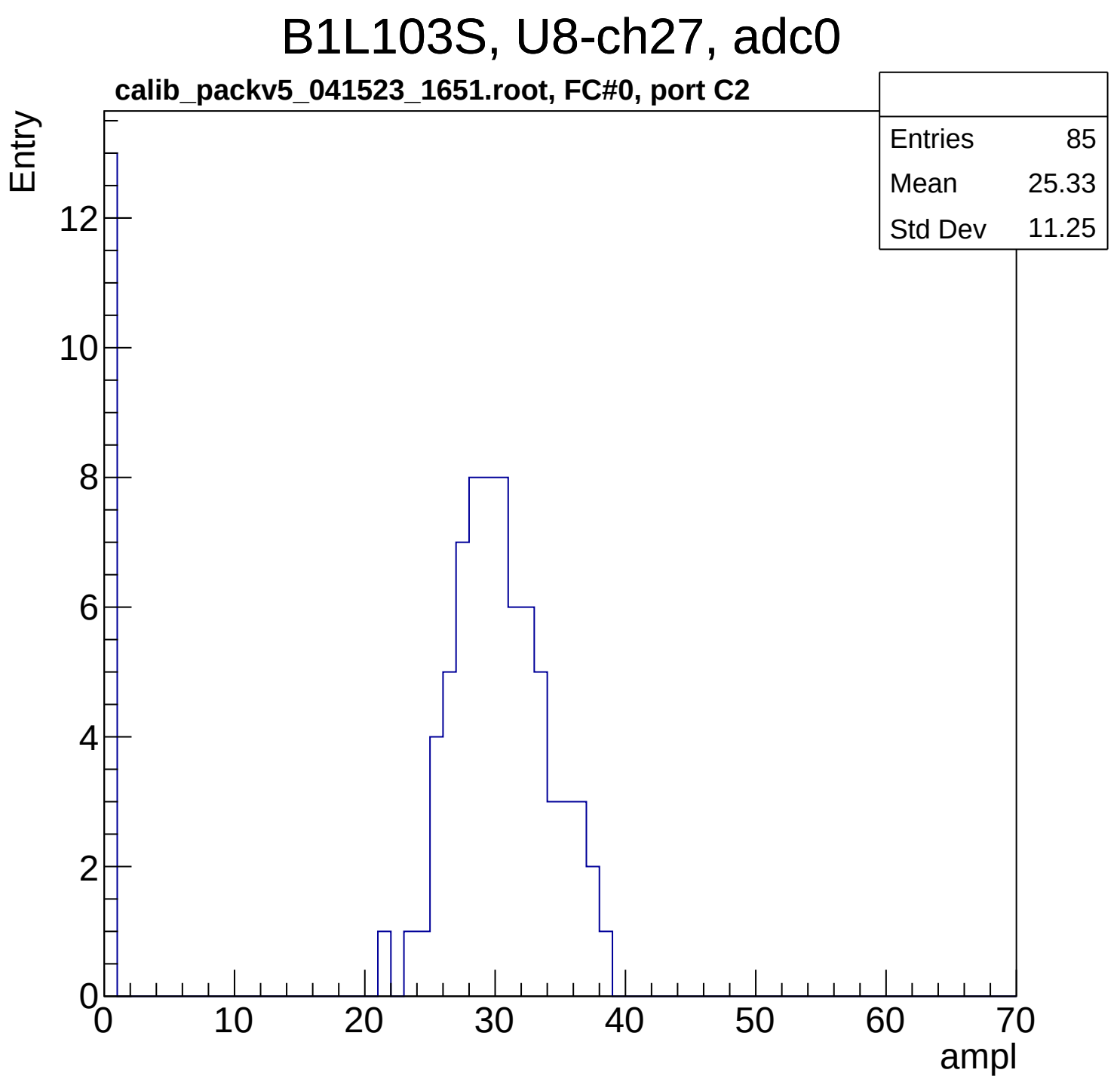
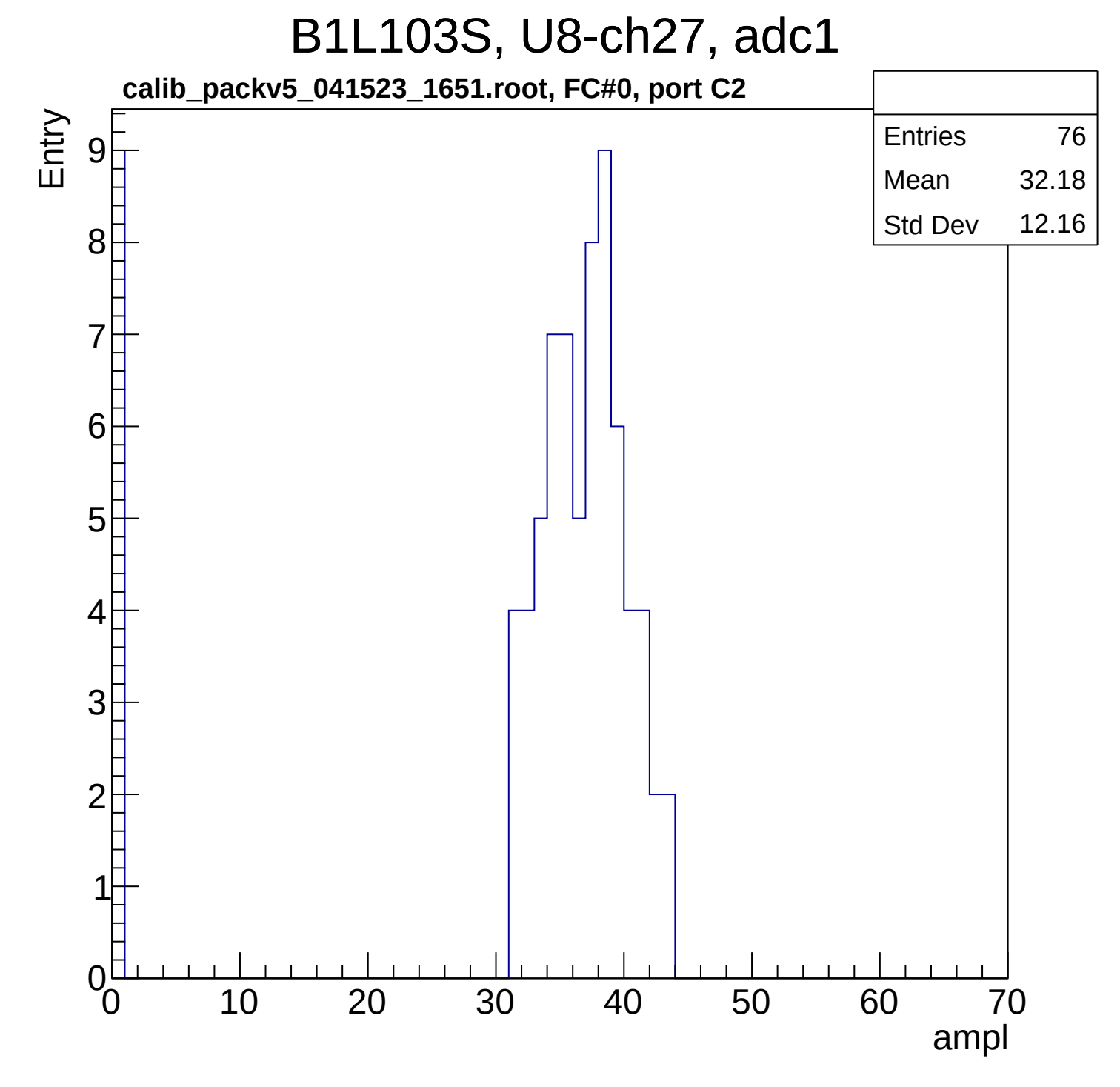
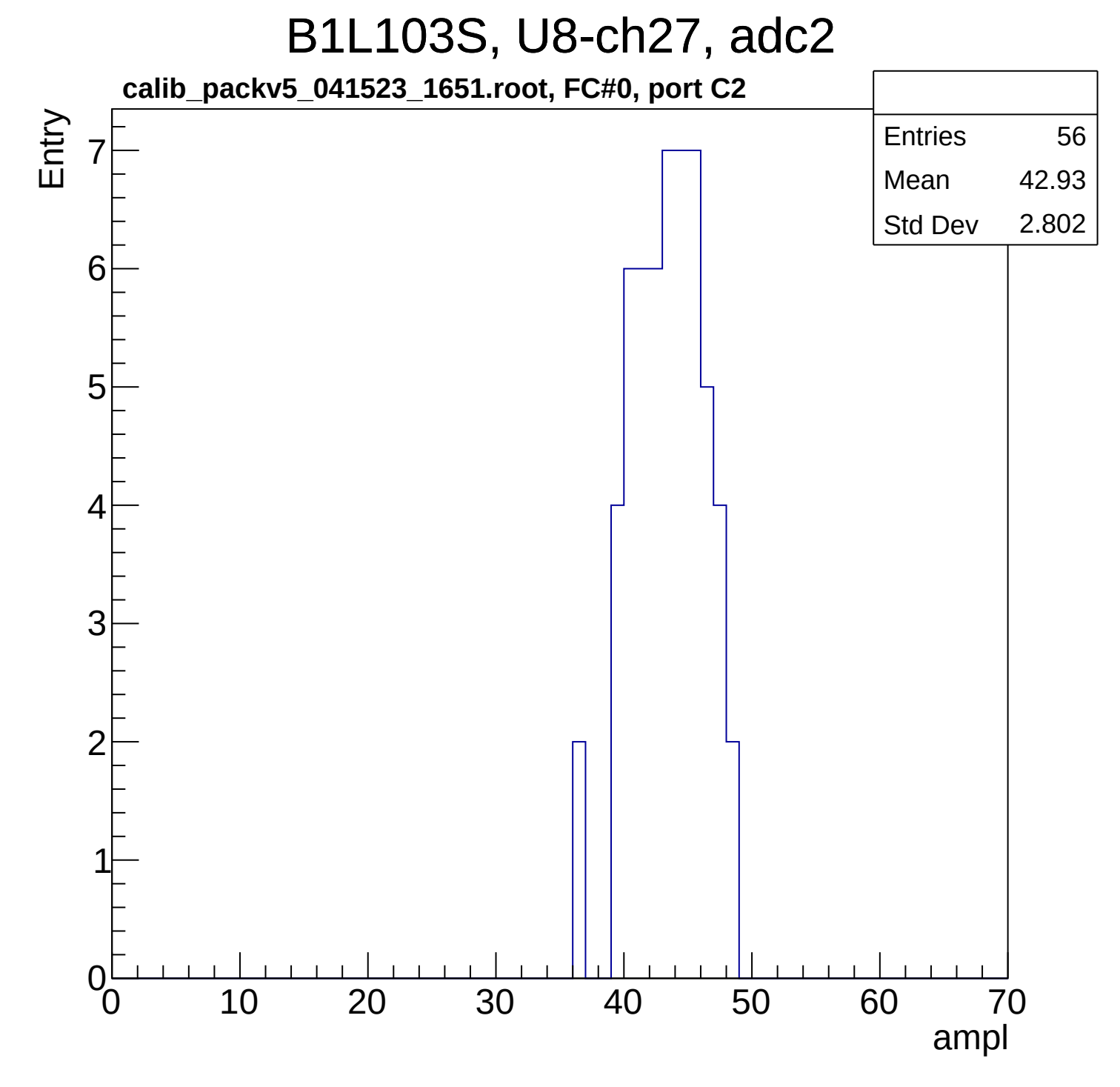
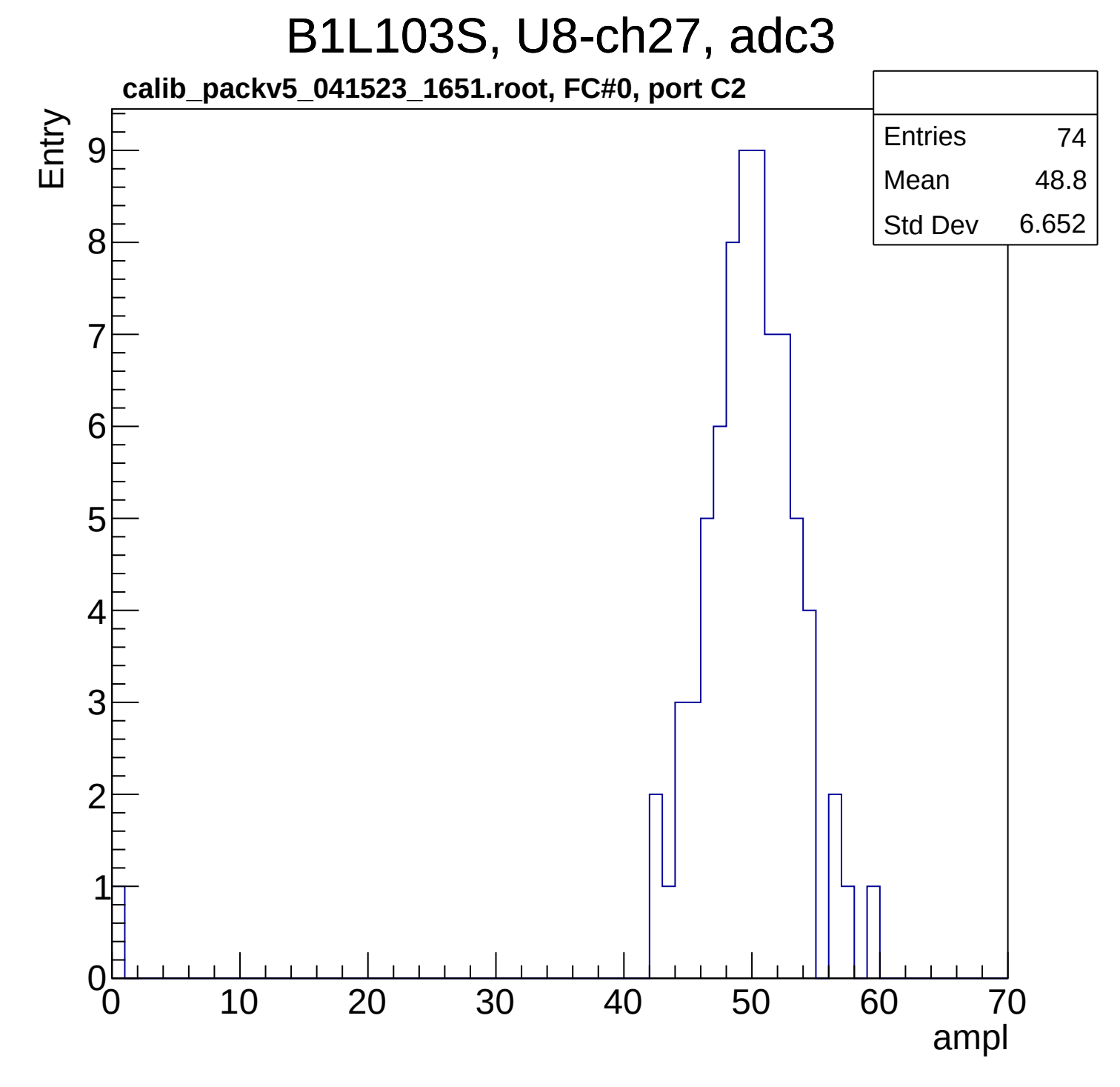
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

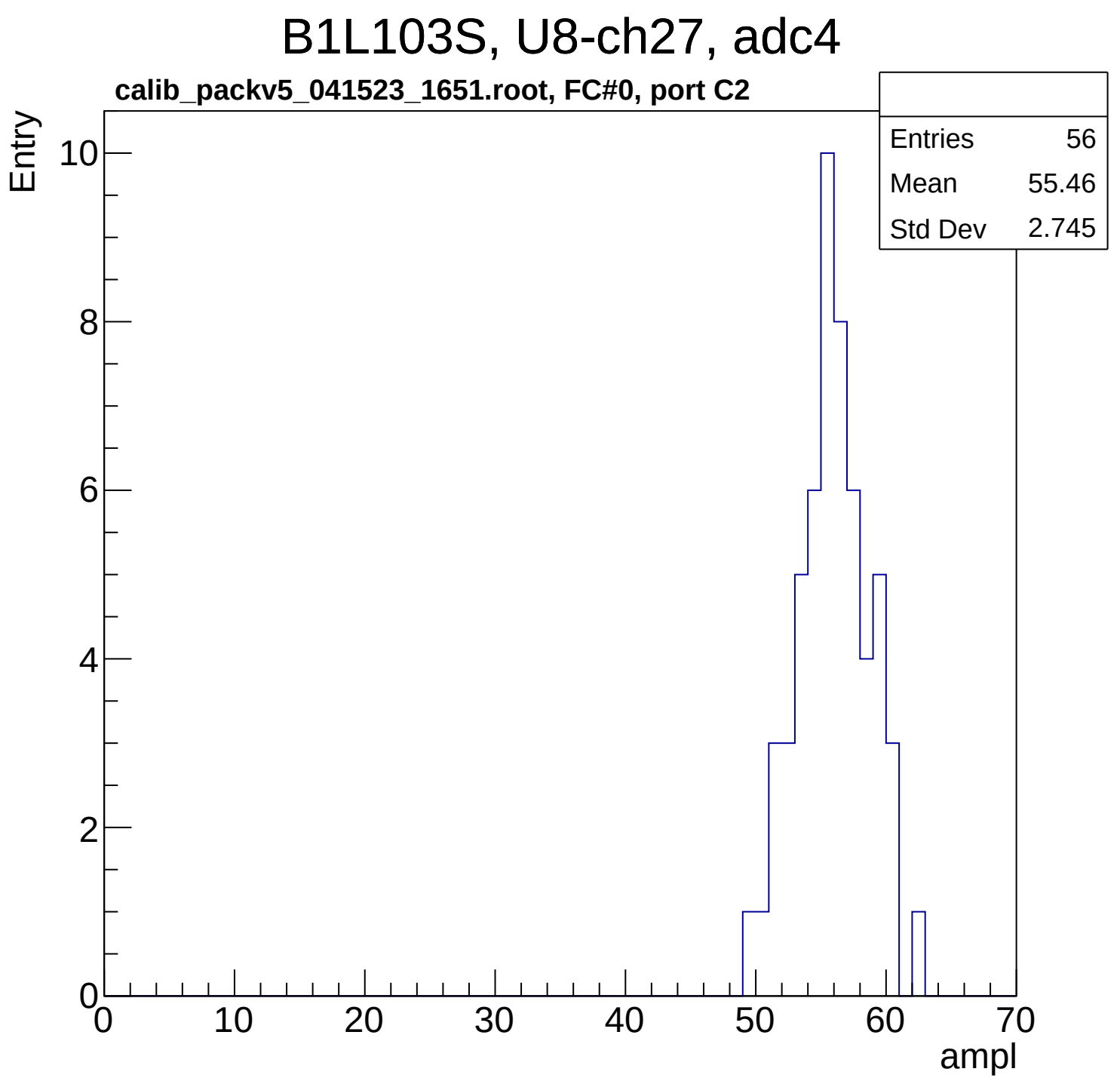

B1L103S, U8-ch26, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.905
Std Dev 18.2
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

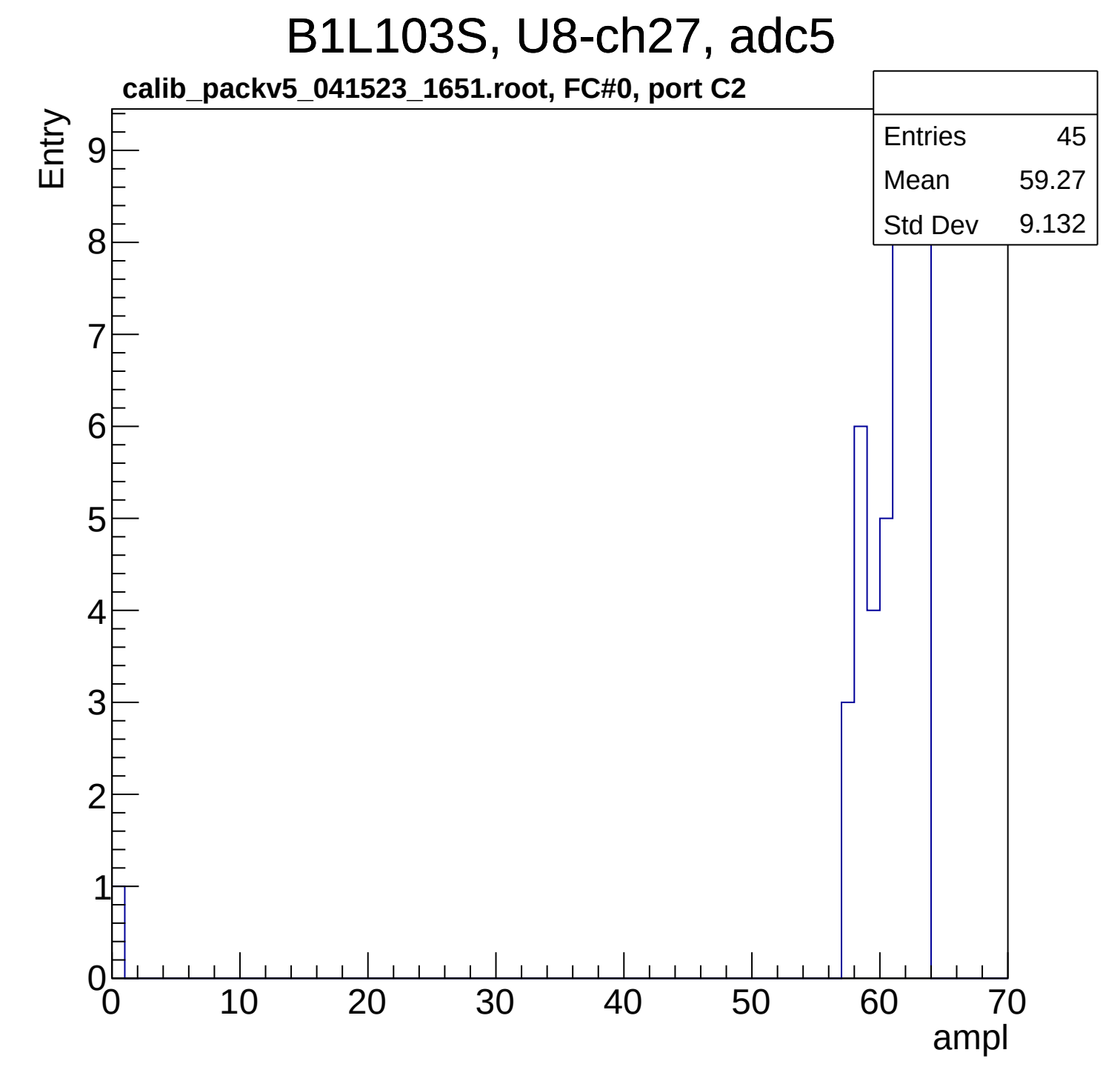

B1L103S, U8-ch27, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 25.33
Std Dev 11.25
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

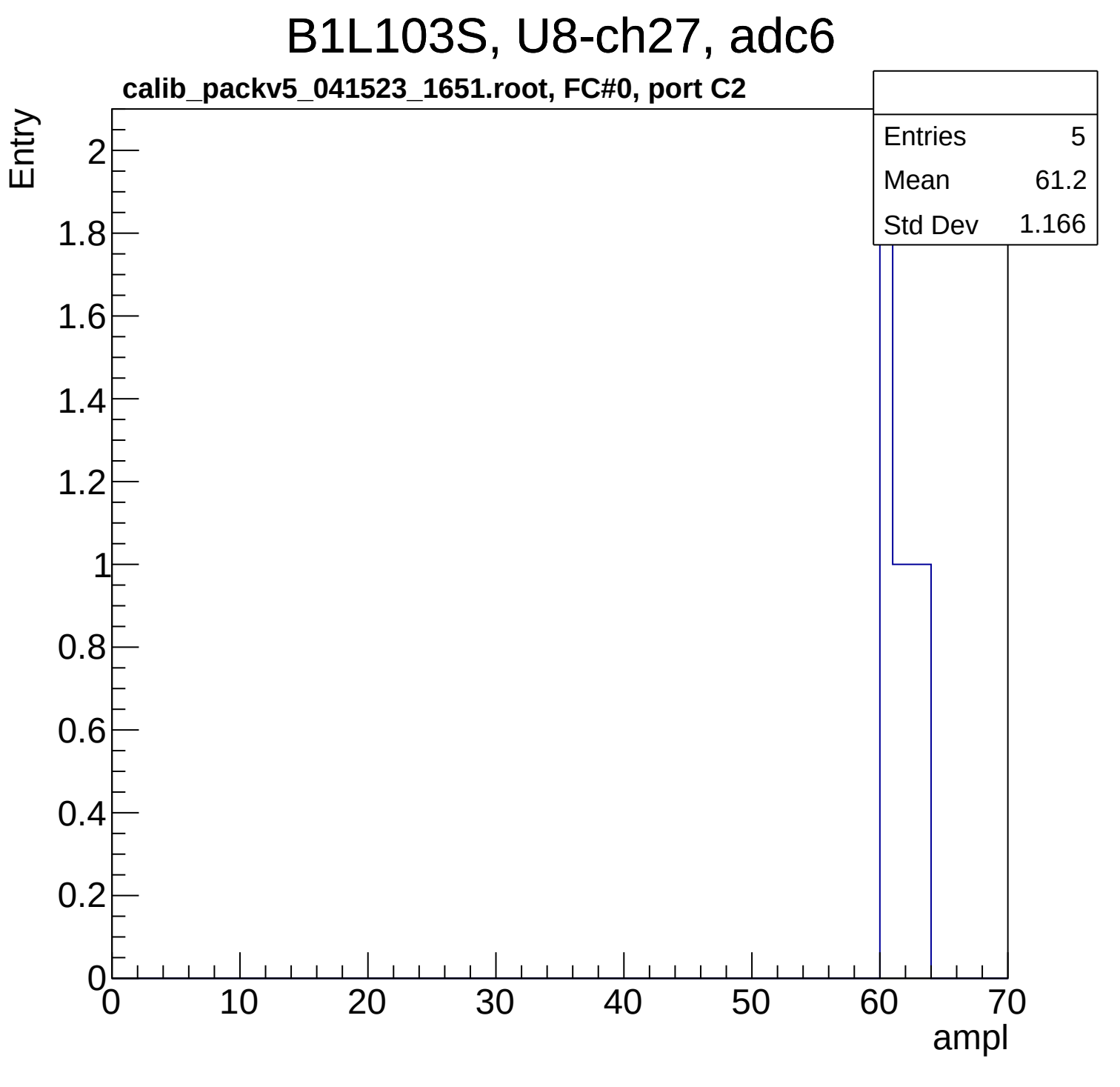

B1L103S, U8-ch27, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 32.18
Std Dev 12.16
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U8-ch27, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 42.93
Std Dev 2.802
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U8-ch27, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 48.8
Std Dev 6.652
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U8-ch27, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 55.46
Std Dev 2.745
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U8-ch27, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 59.27
Std Dev 9.132
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U8-ch27, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 61.2
Std Dev 1.166
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
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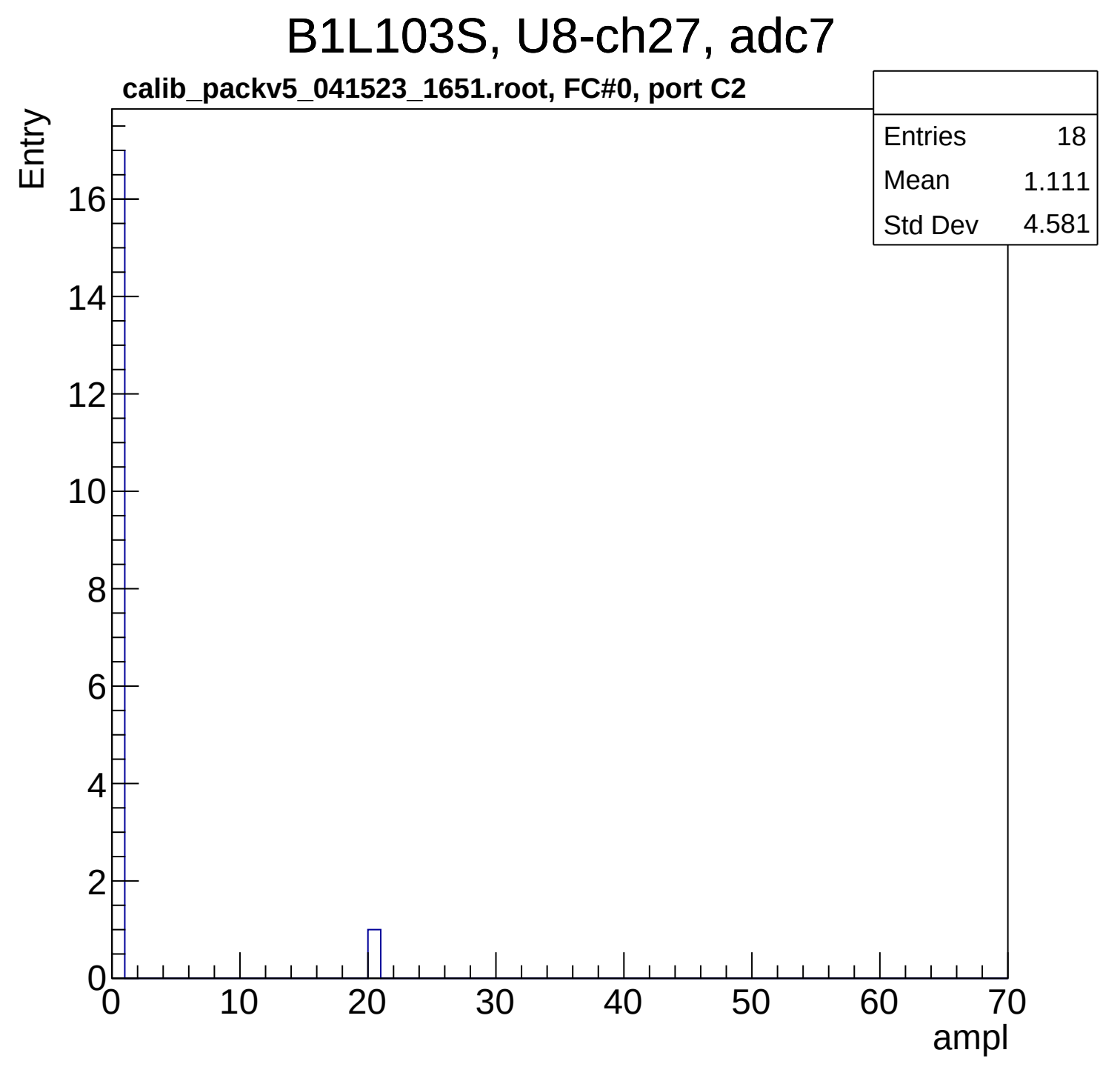
B1L103S, U8-ch27, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.111
Std Dev 4.581
Entry
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4
6
8
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12
14
16
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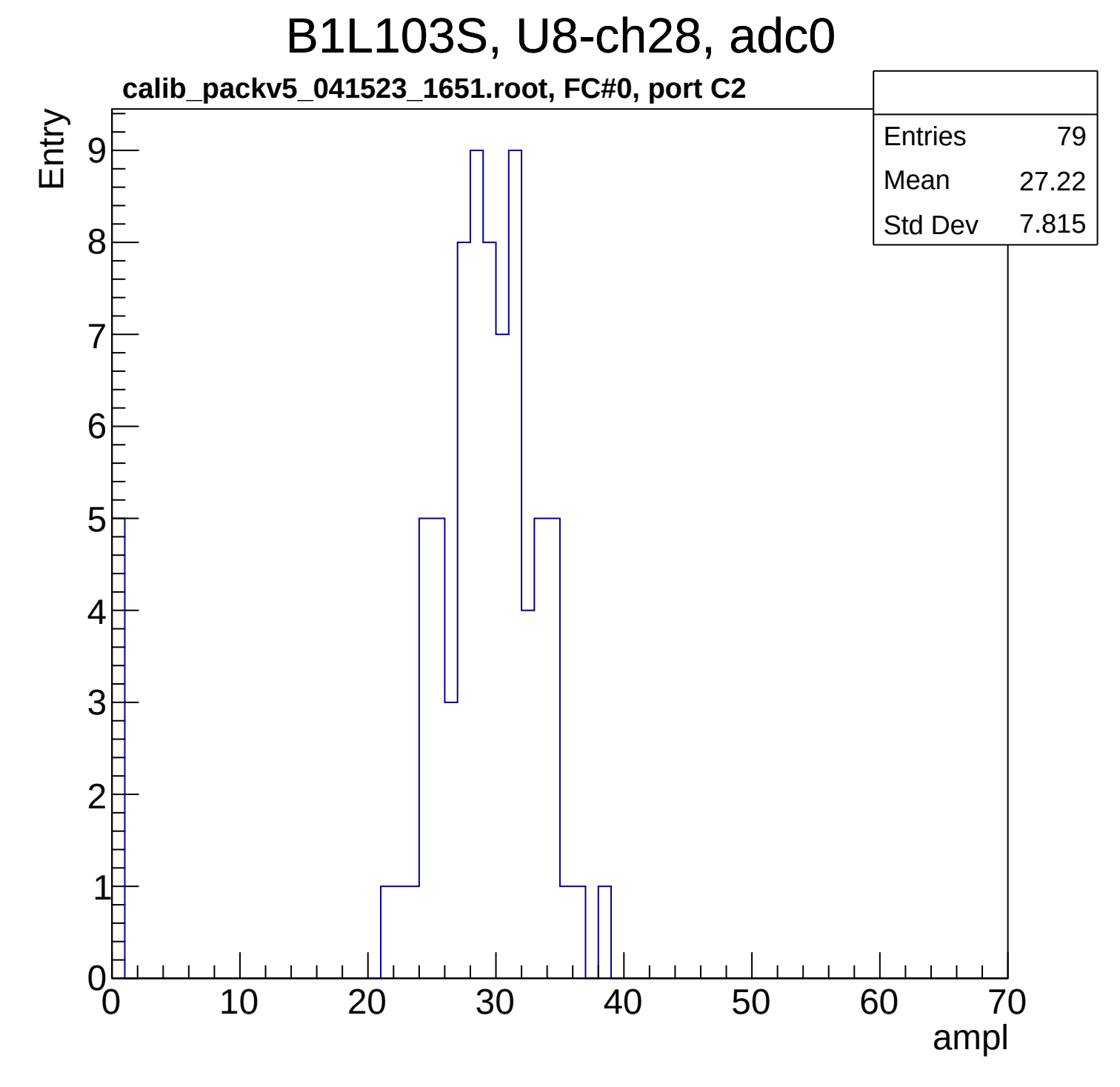
70
ampl


B1L103S, U8-ch28, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 27.22
Std Dev 7.815
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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60
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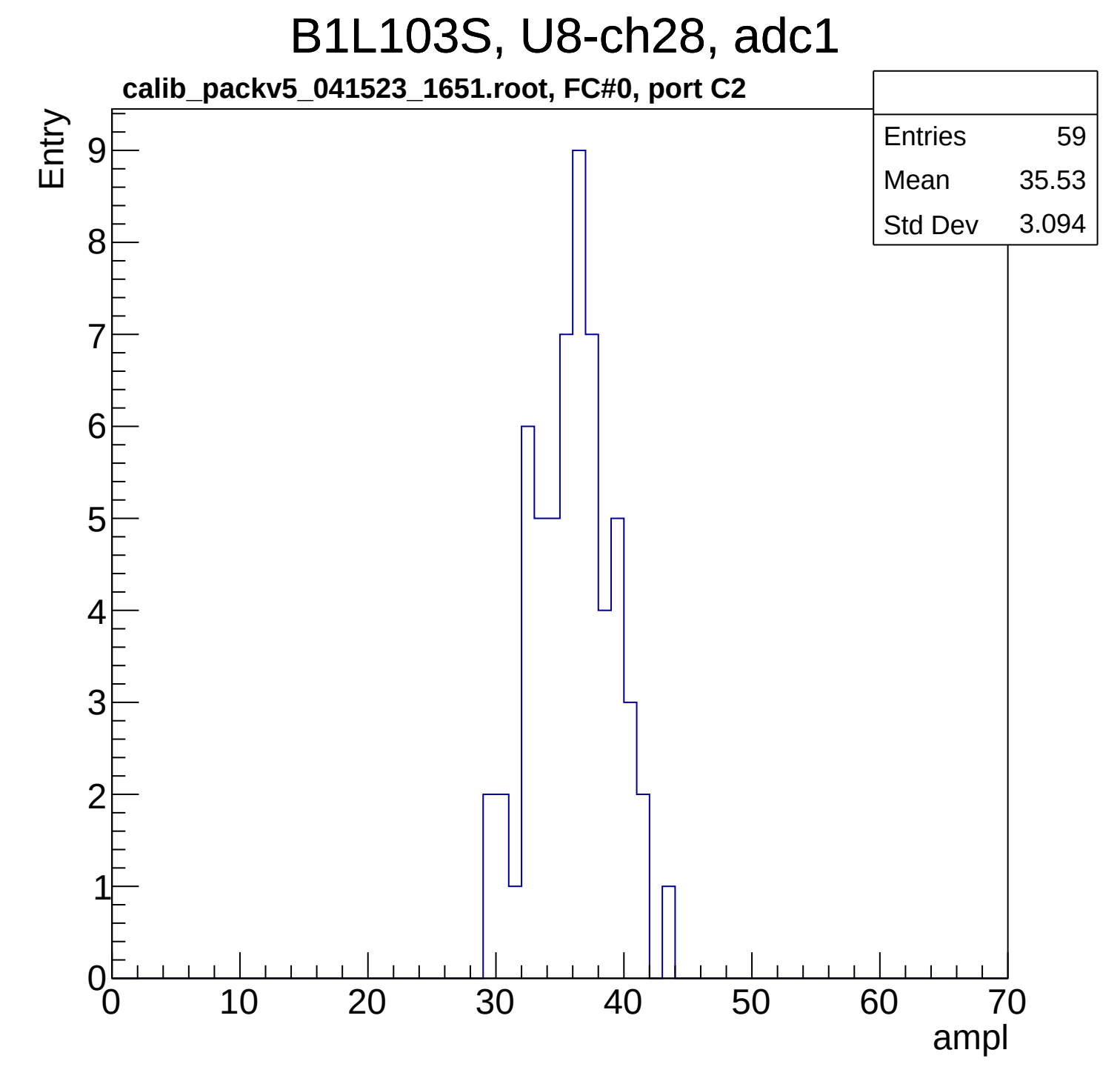
B1L103S, U8-ch28, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 35.53
Std Dev 3.094
Entry
ampl
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2
3
4
5
6
7
8
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0
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60
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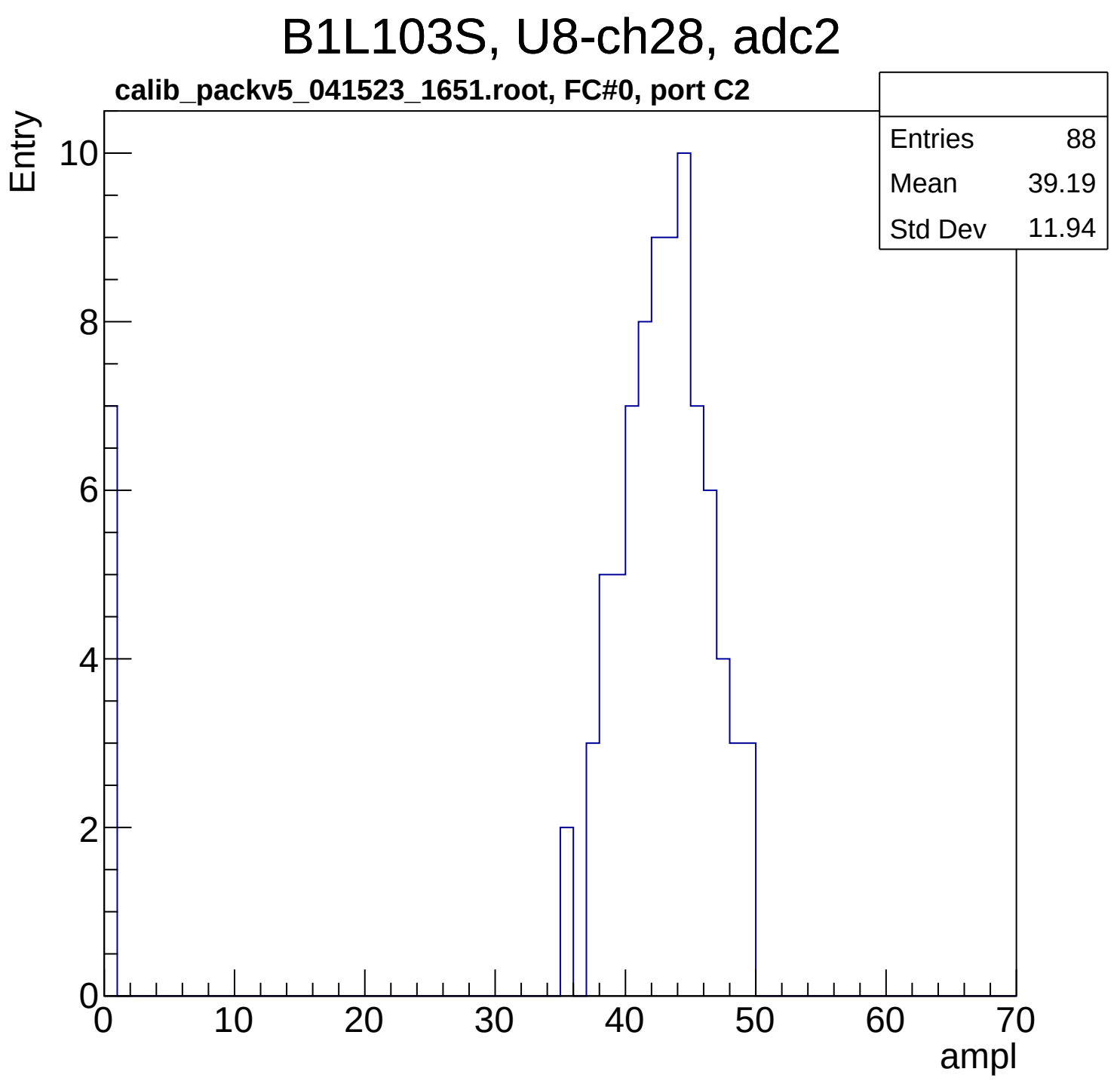
B1L103S, U8-ch28, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 39.19
Std Dev 11.94
Entry
ampl
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2
4
6
8
10
0
10
20
30
40
50
60
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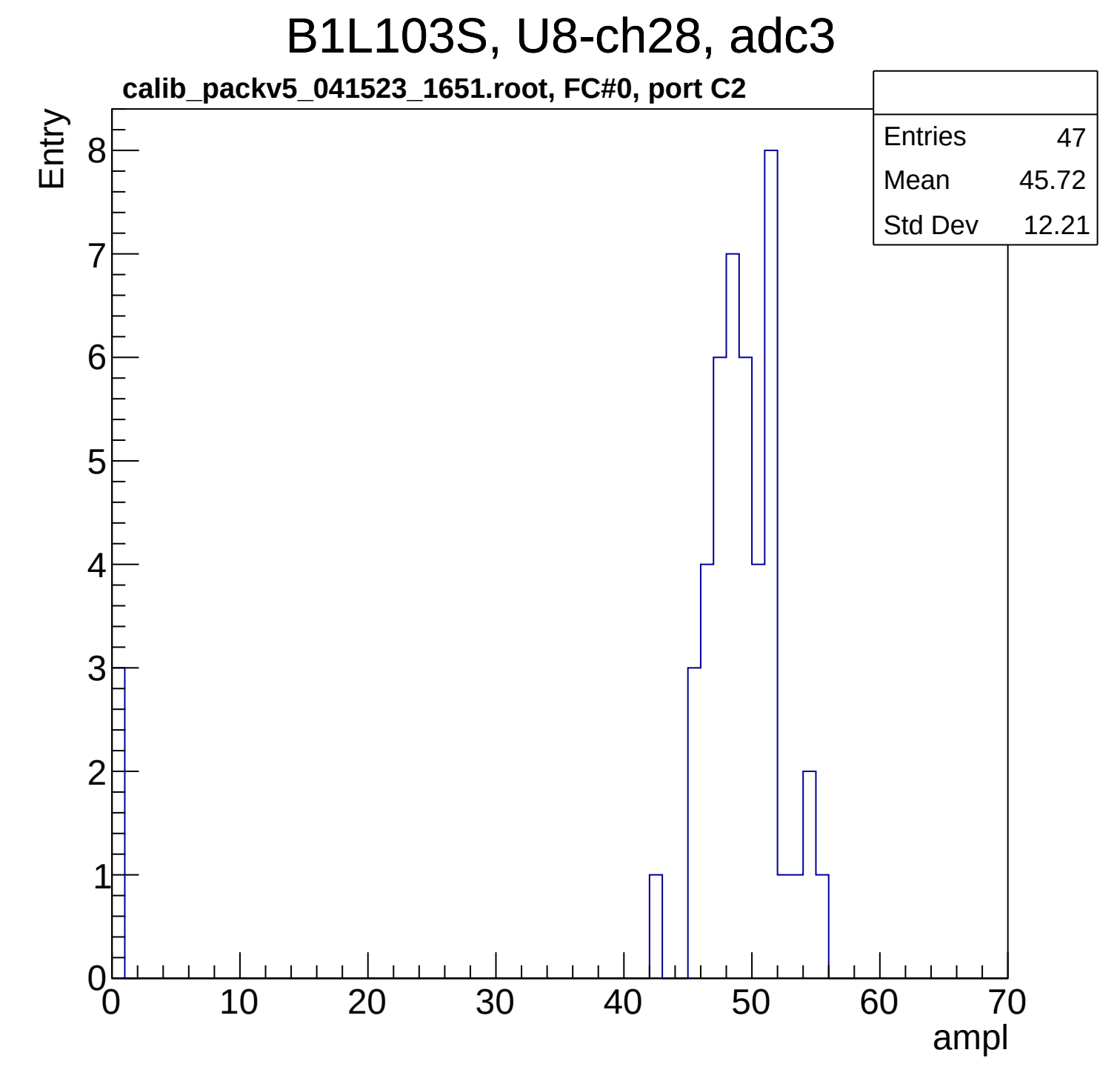
B1L103S, U8-ch28, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 45.72
Std Dev 12.21
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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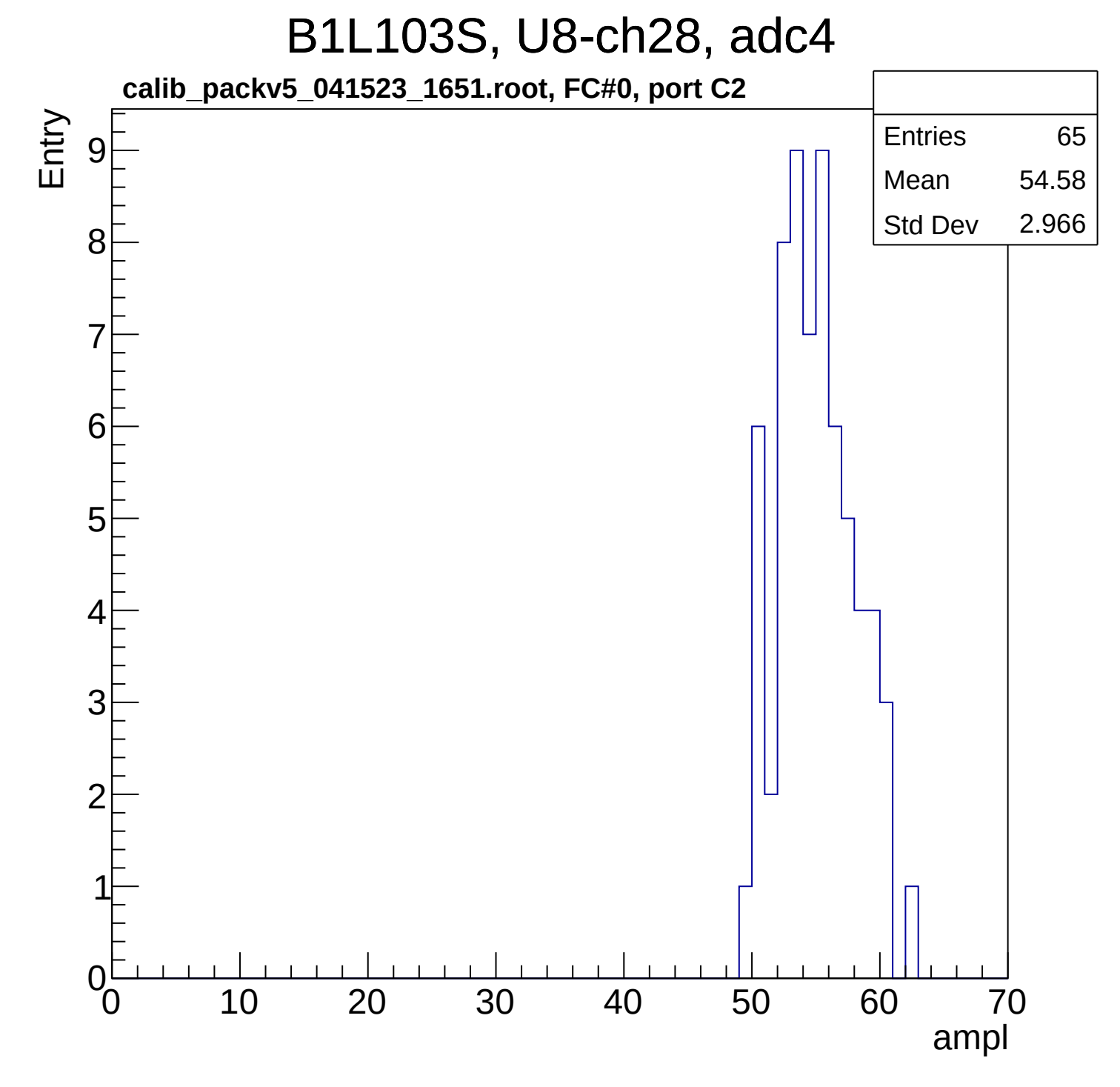
B1L103S, U8-ch28, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 54.58
Std Dev 2.966
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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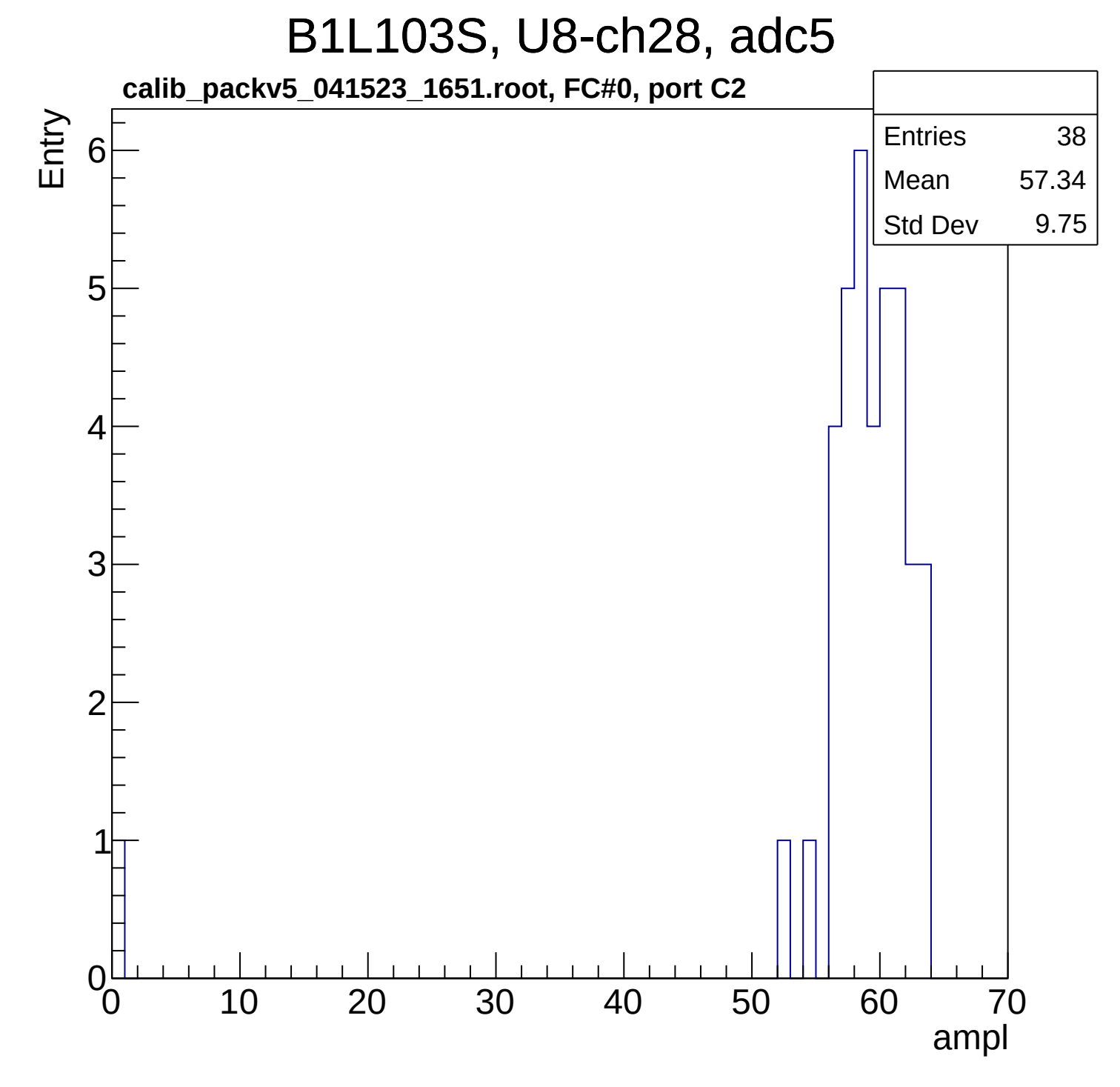
B1L103S, U8-ch28, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 57.34
Std Dev 9.75
Entry
ampl
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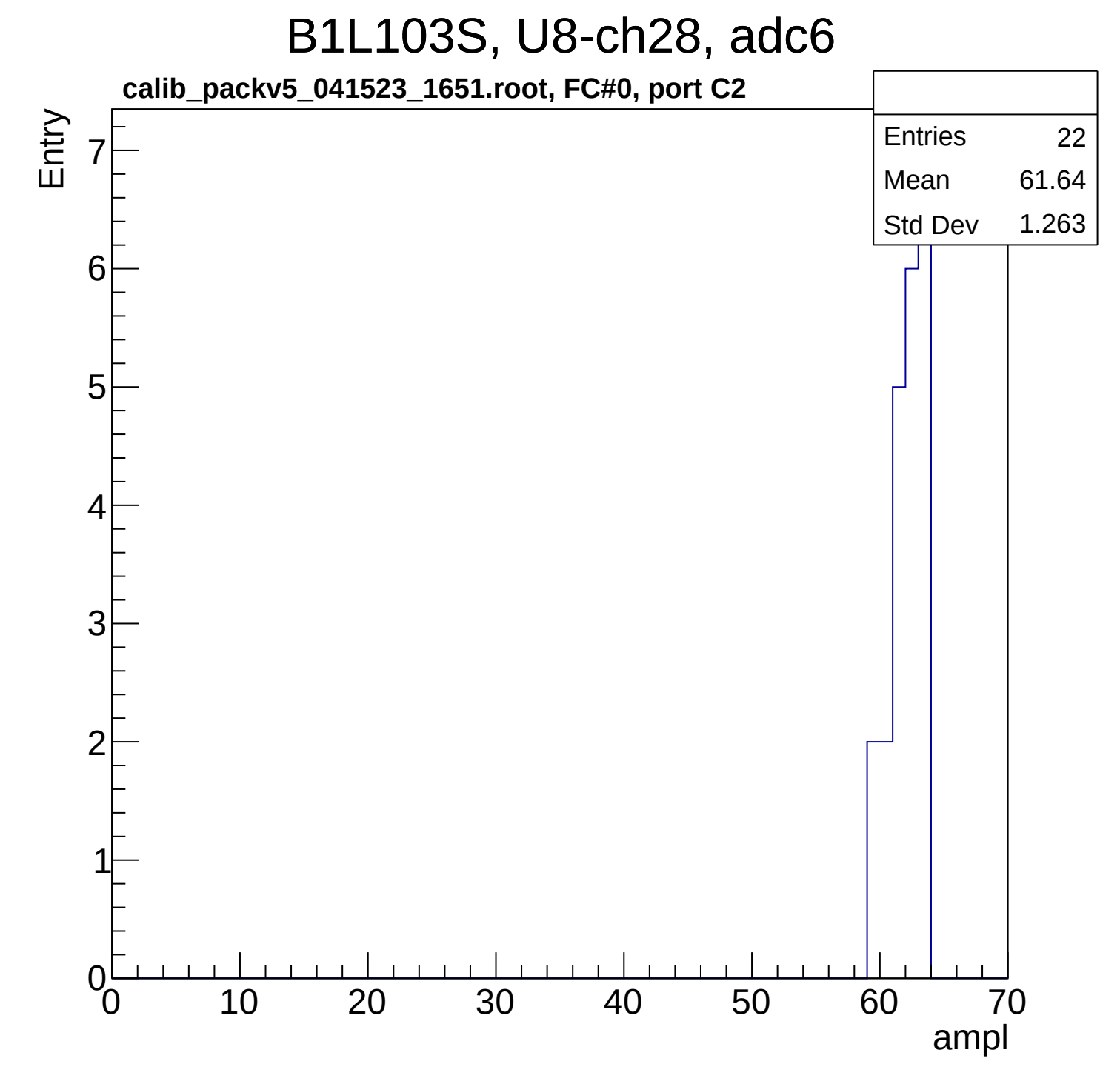
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U8-ch28, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 61.64
Std Dev 1.263
Entry
ampl
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2
3
4
5
6
7
0
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20
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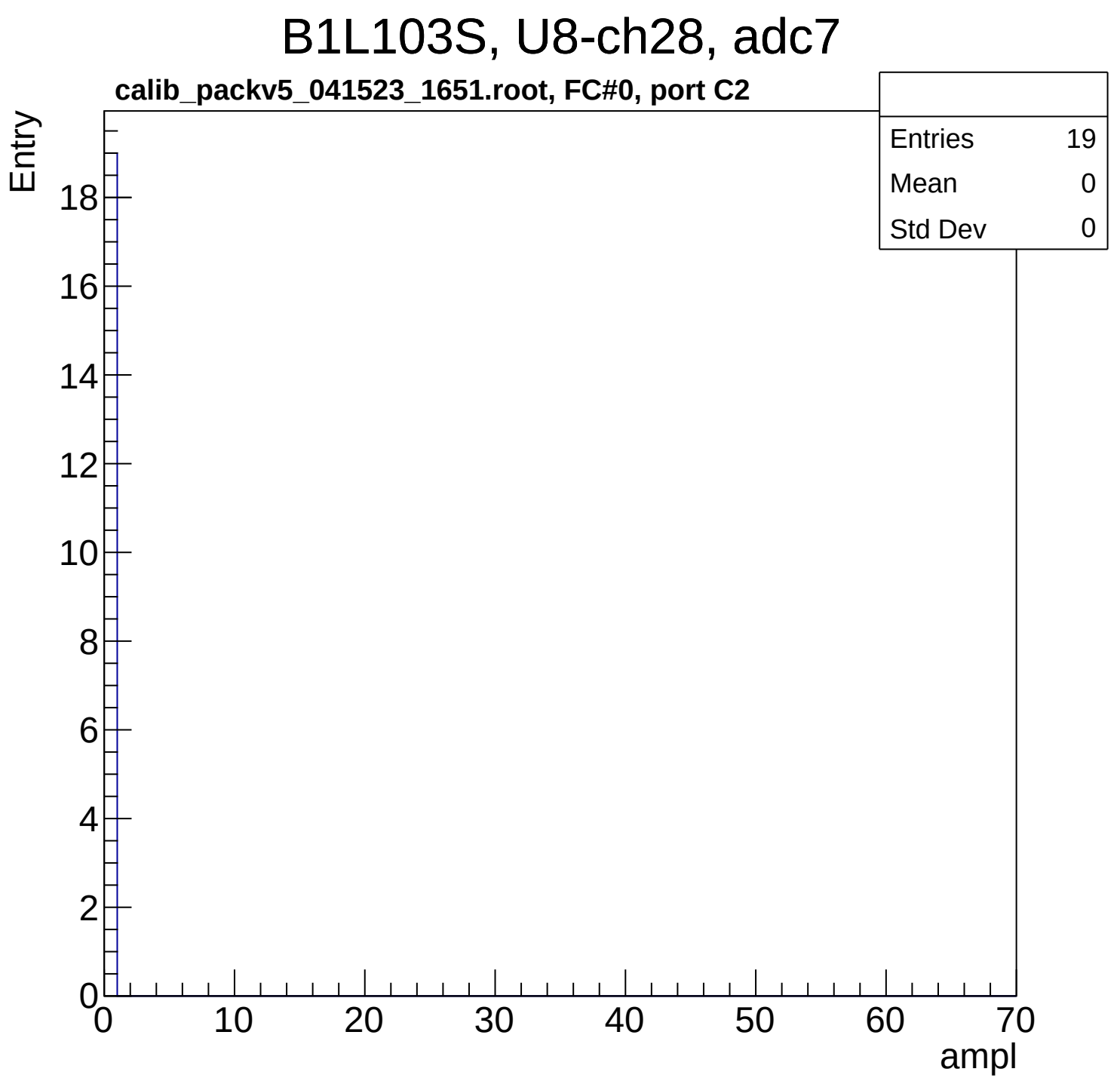
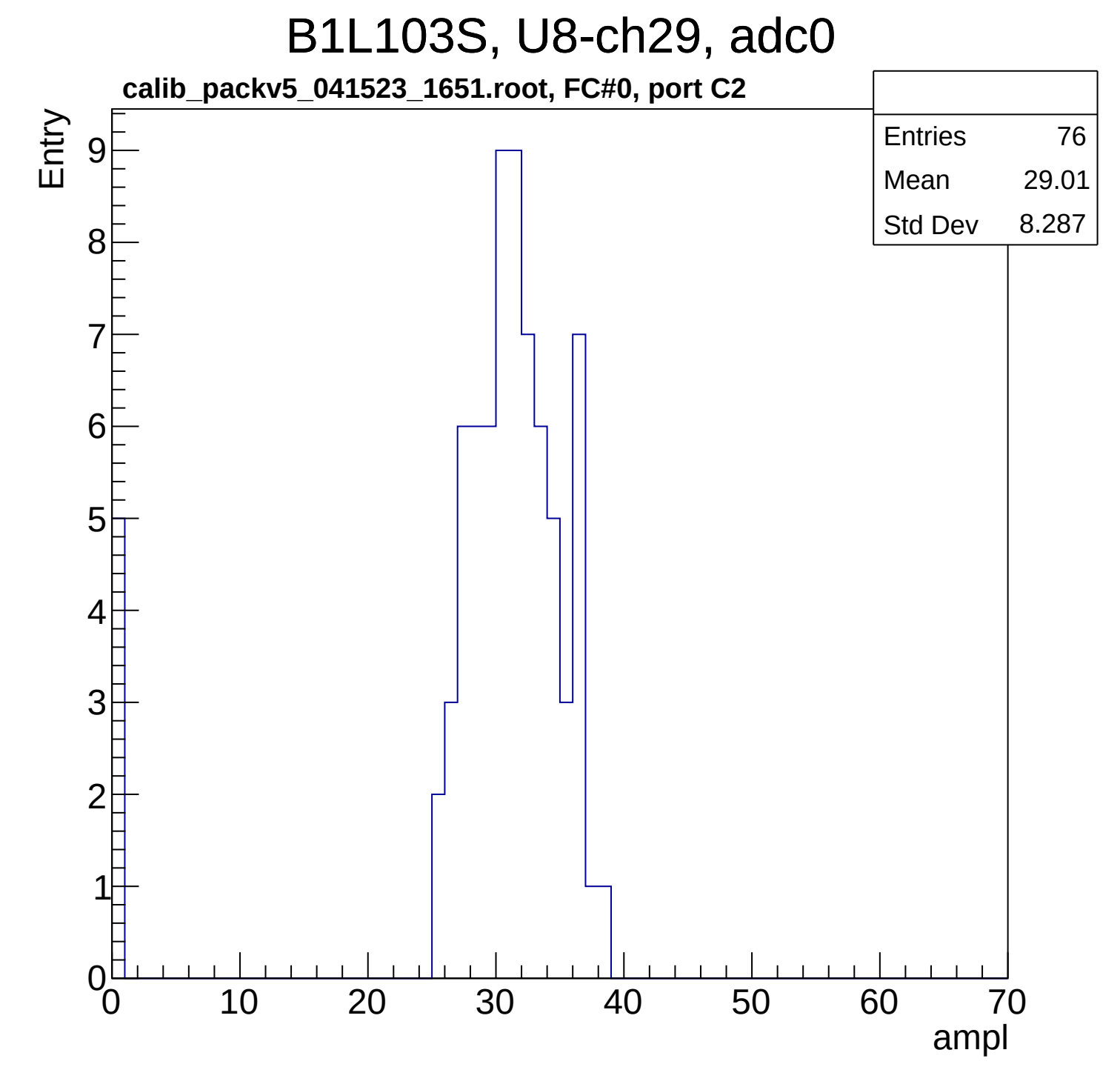
40
50
60
70


B1L103S, U8-ch28, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch29, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 29.01
Std Dev 8.287
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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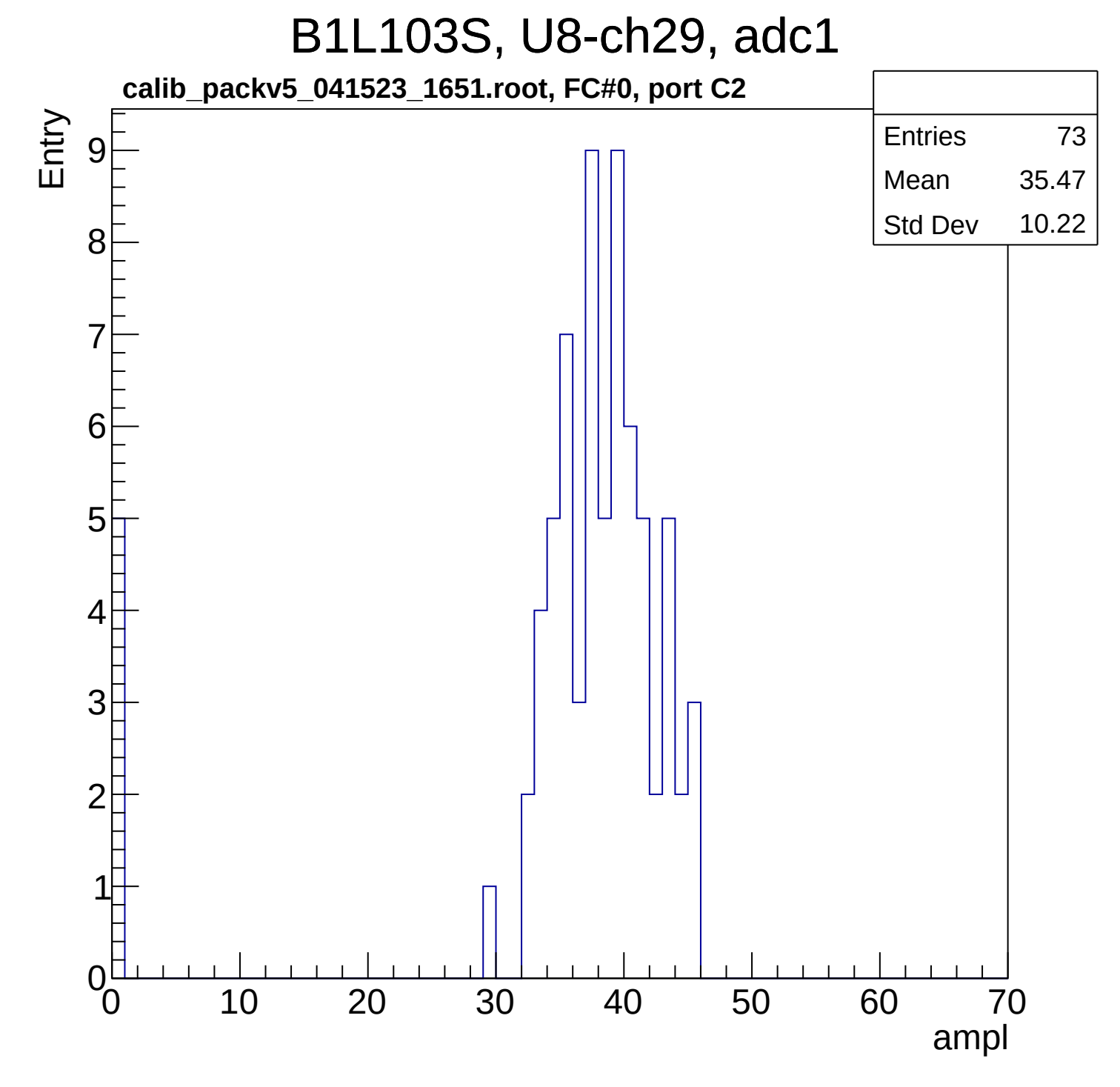
B1L103S, U8-ch29, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 35.47
Std Dev 10.22
Entry
ampl
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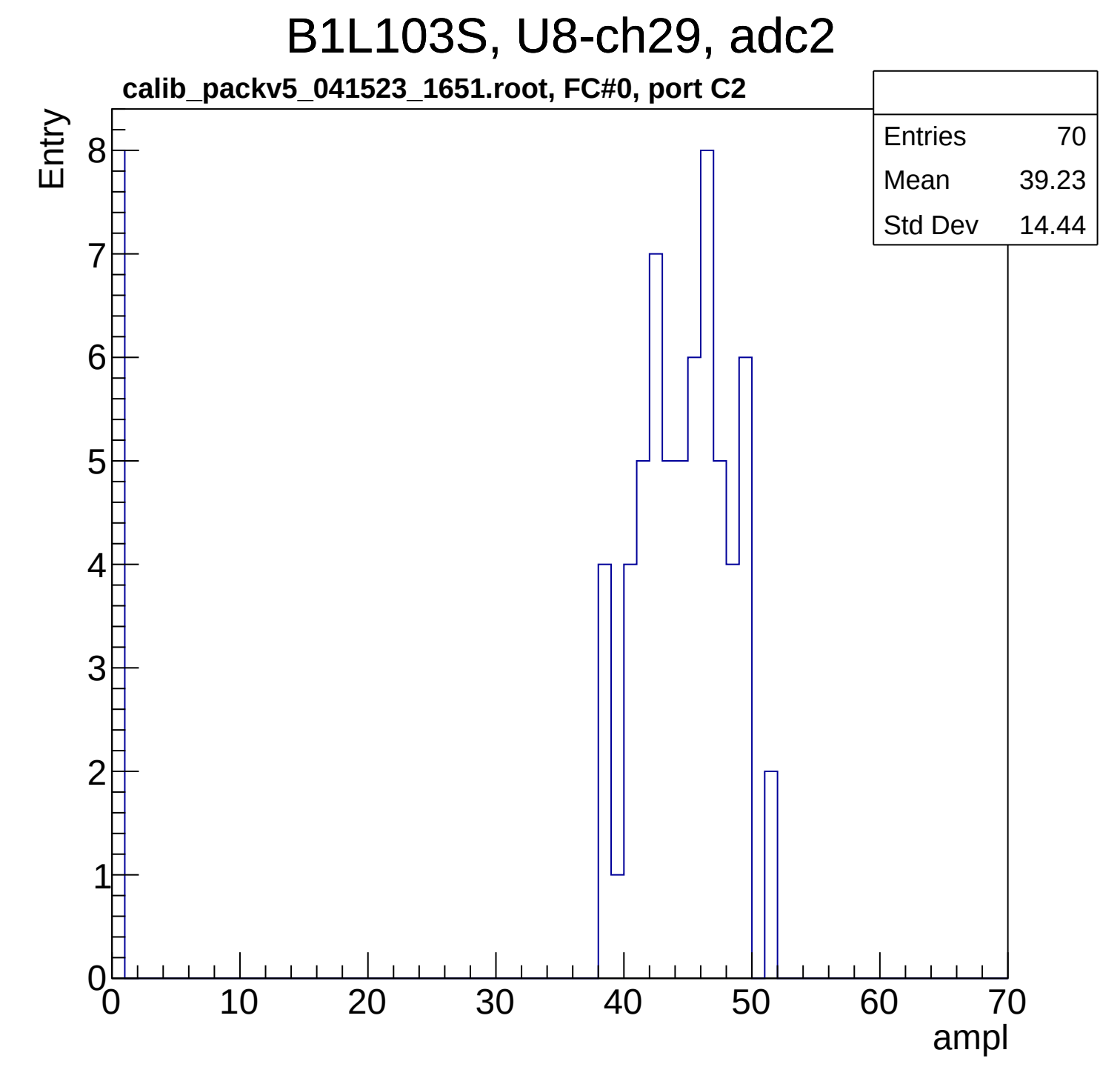
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U8-ch29, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 39.23
Std Dev 14.44
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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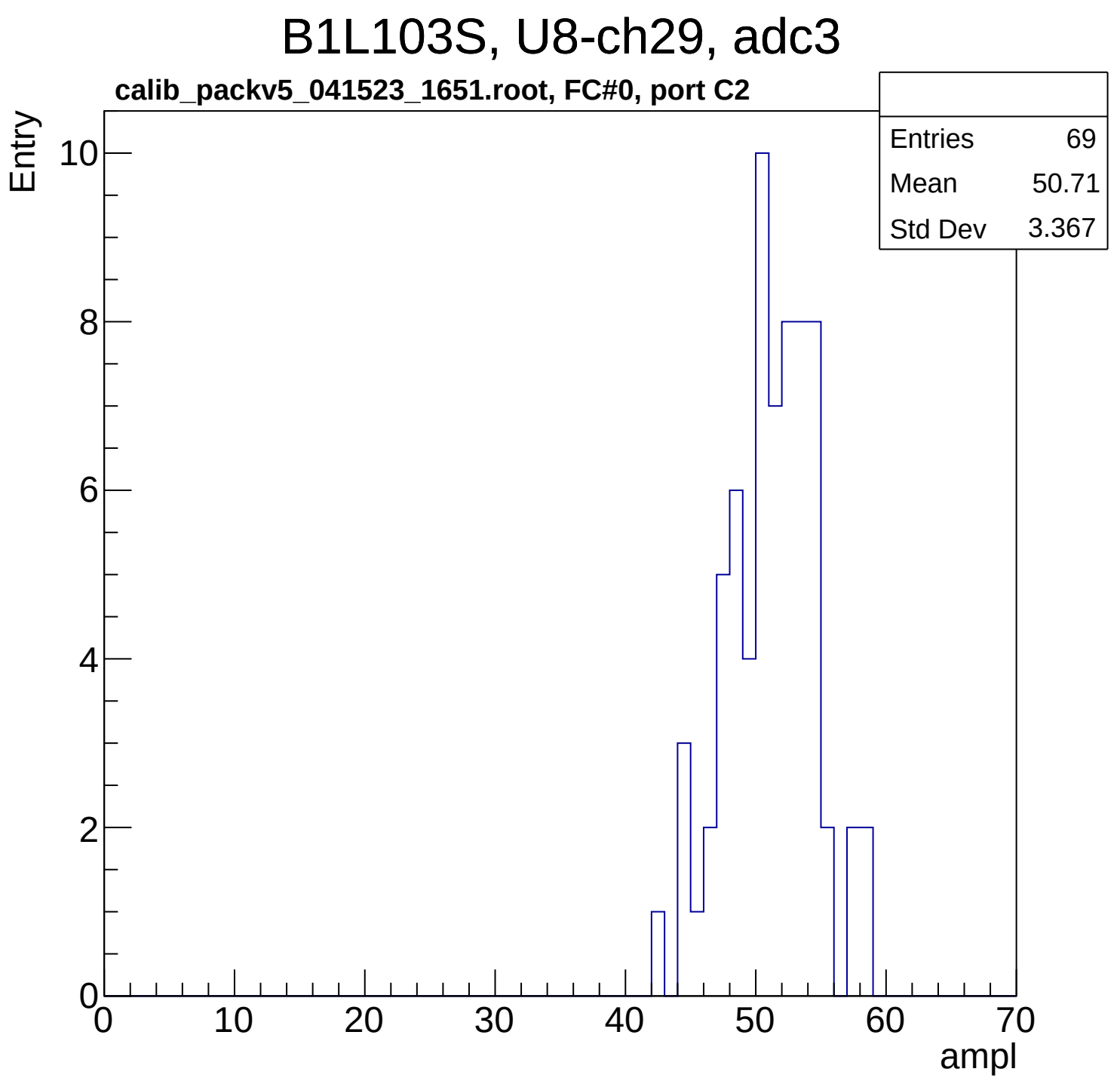
B1L103S, U8-ch29, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 50.71
Std Dev 3.367
Entry
ampl
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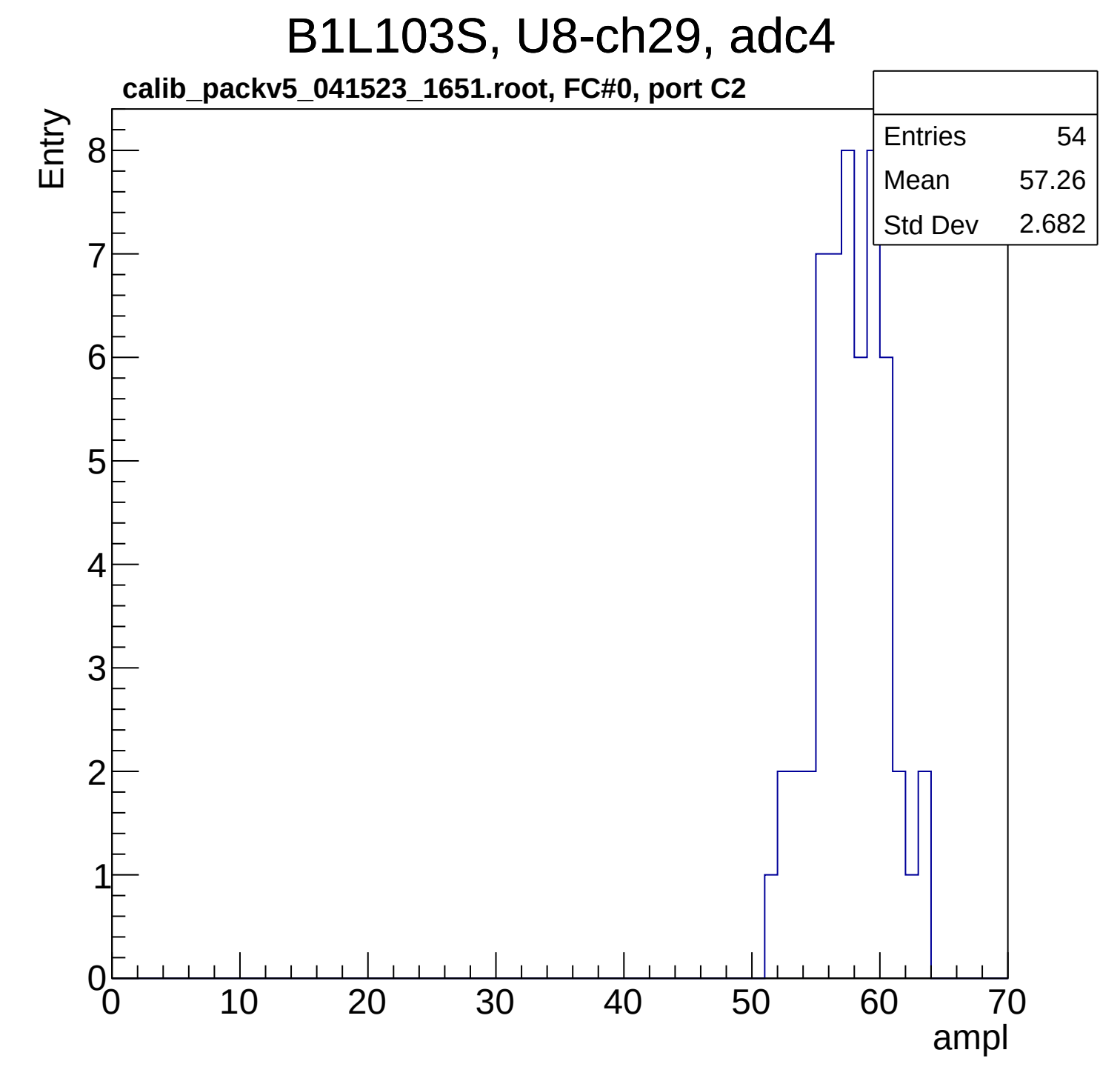
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U8-ch29, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 57.26
Std Dev 2.682
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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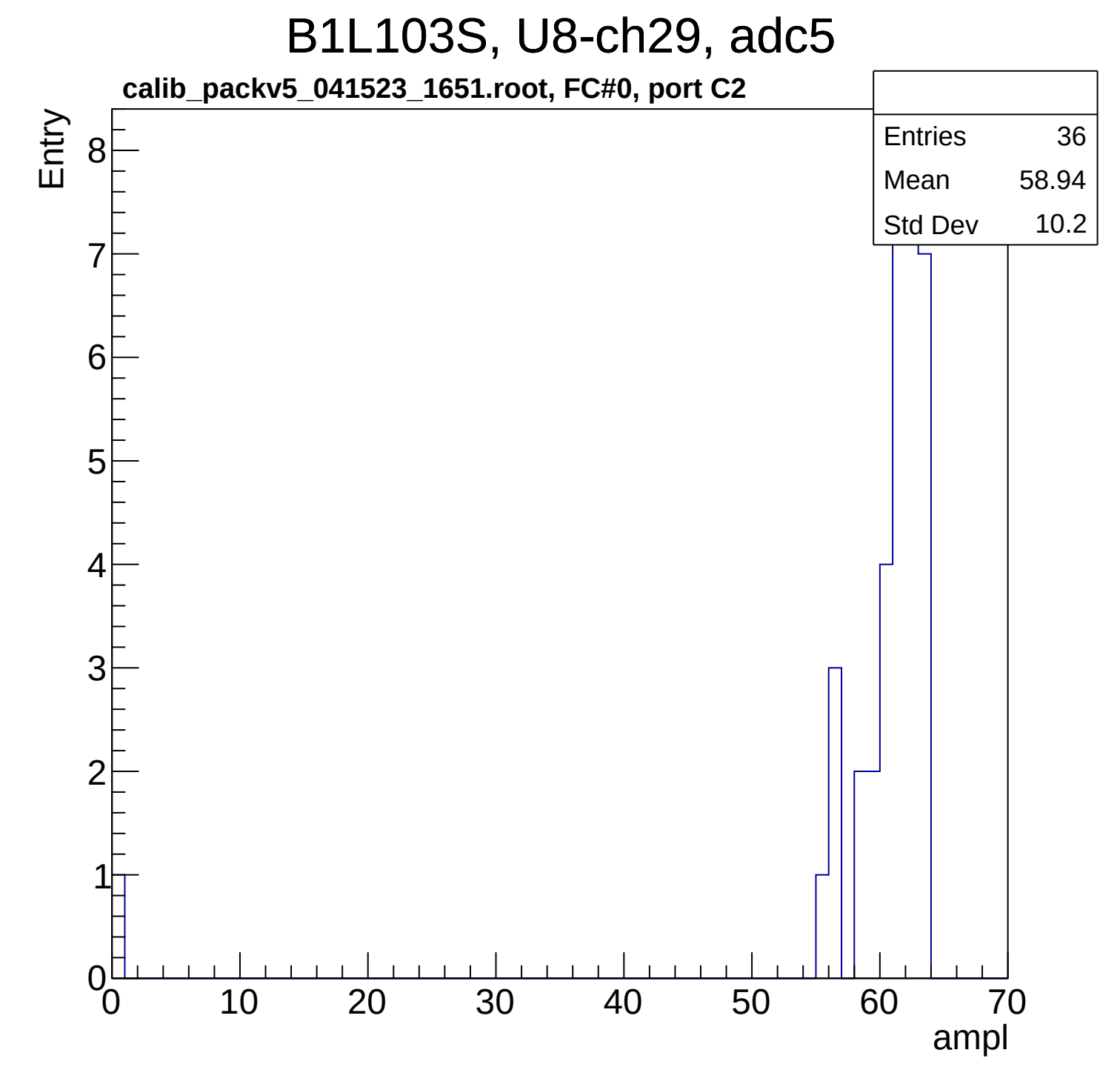
B1L103S, U8-ch29, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 58.94
Std Dev 10.2
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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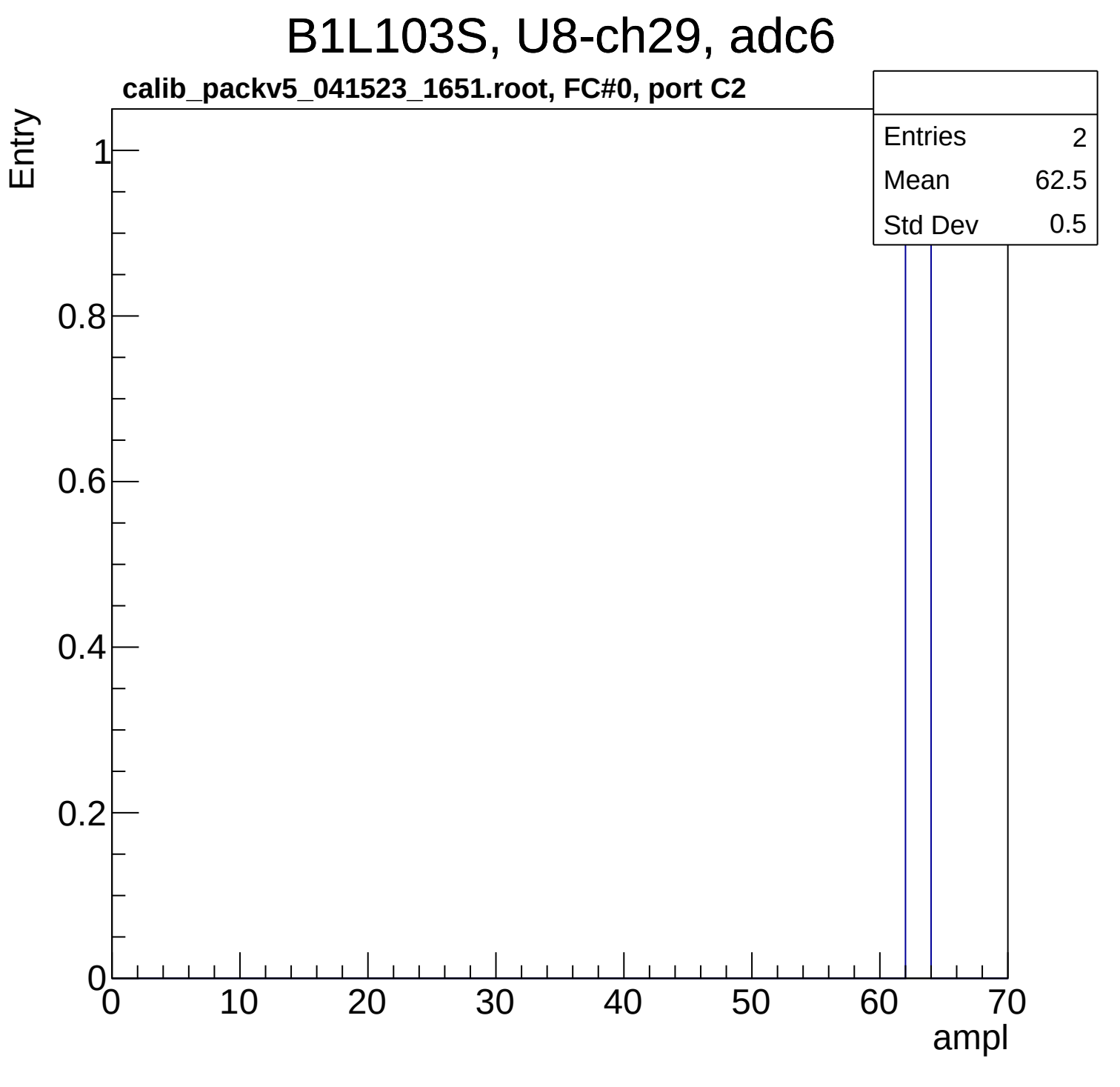
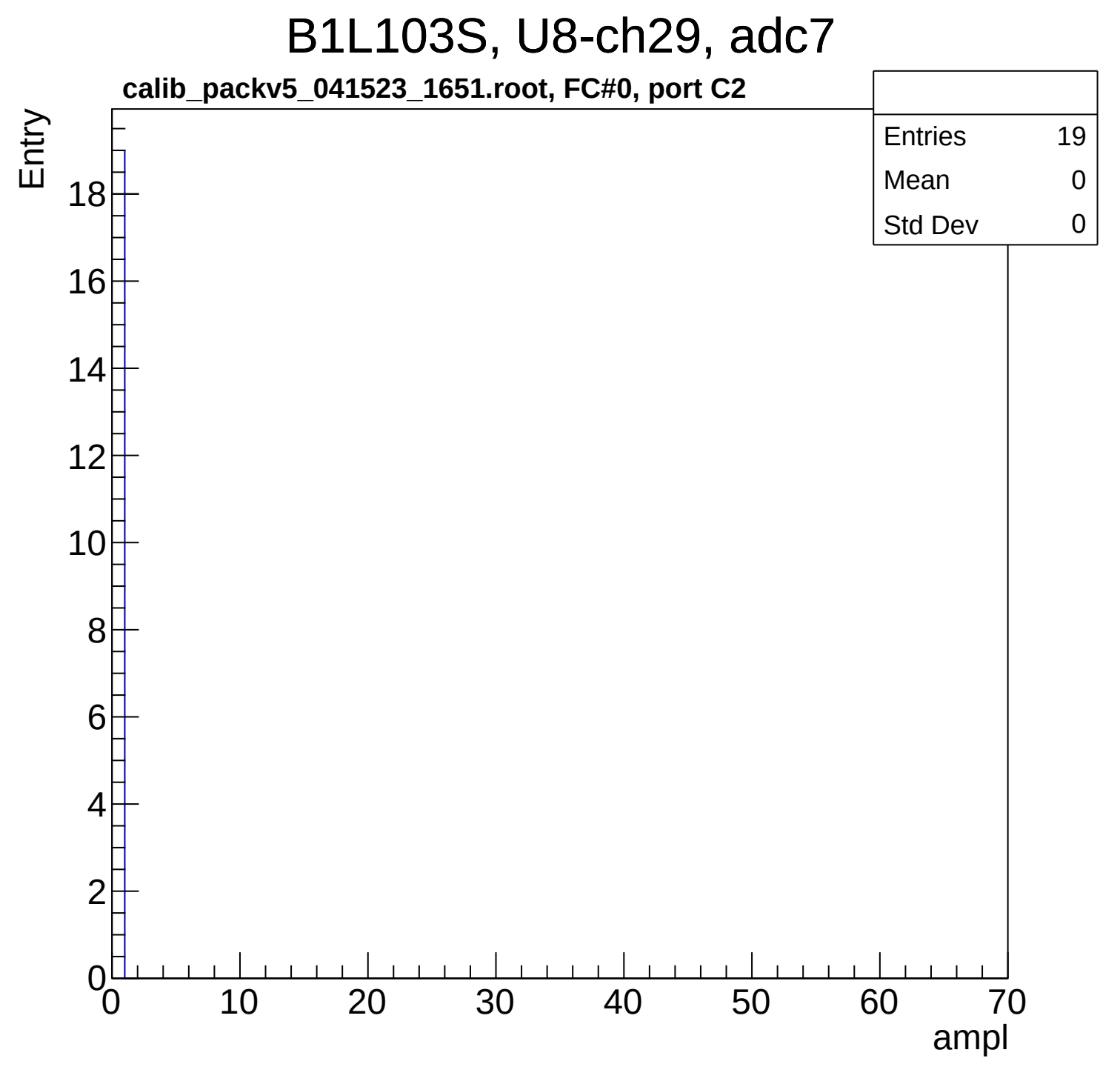
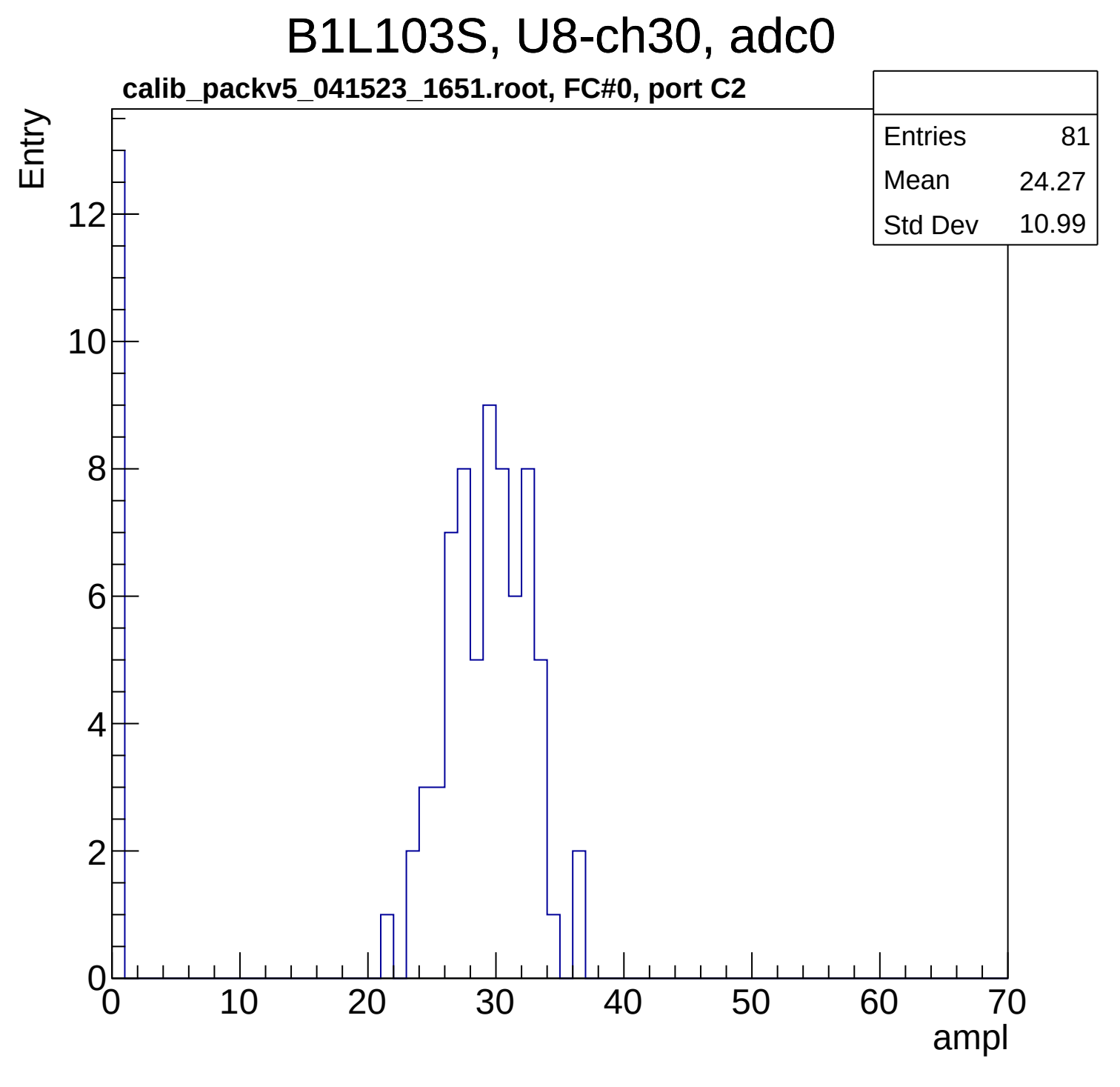

B1L103S, U8-ch29, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch29, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch30, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 24.27
Std Dev 10.99
Entry
0
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4
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8
10
12
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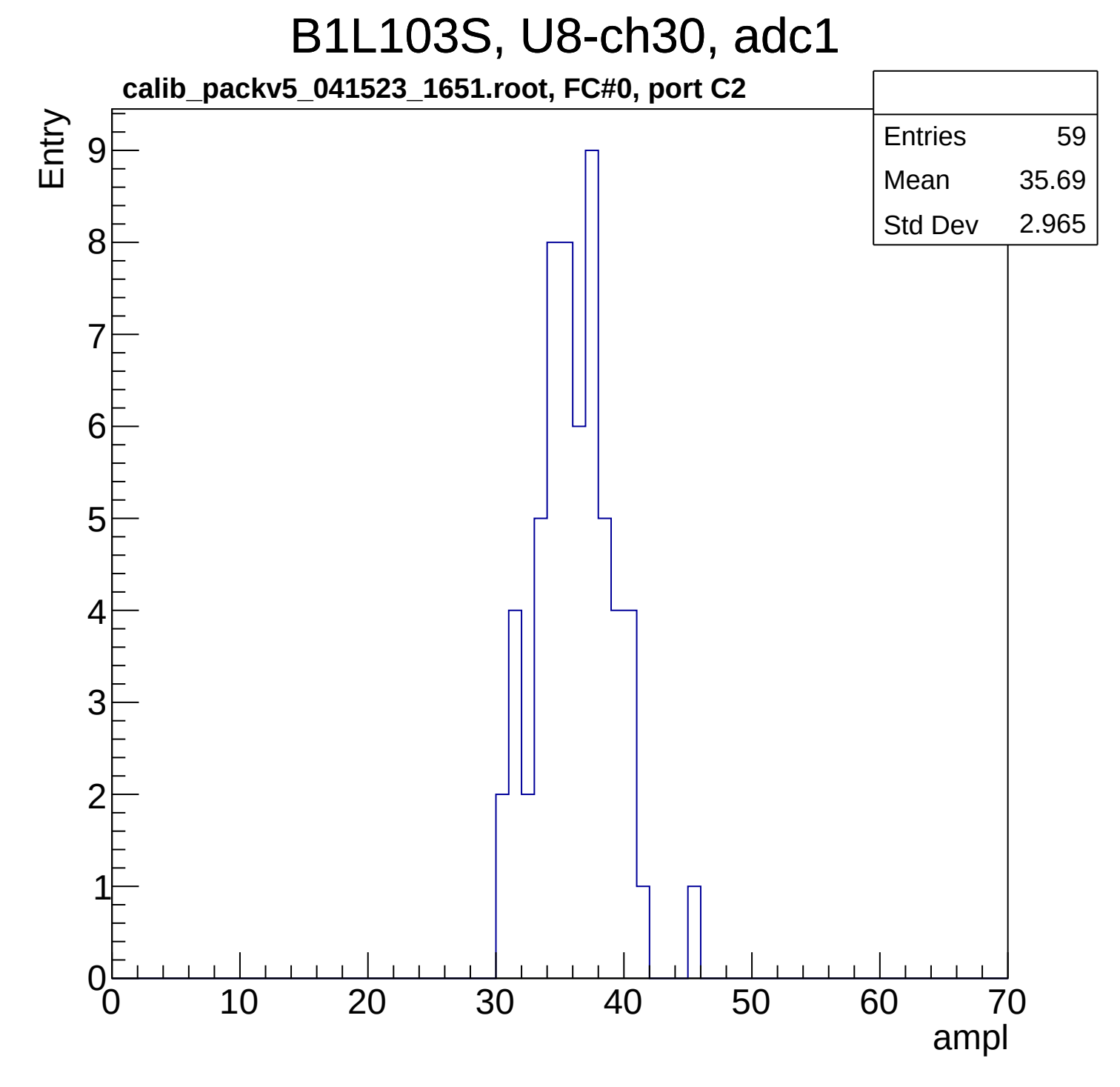
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch30, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 35.69
Std Dev 2.965
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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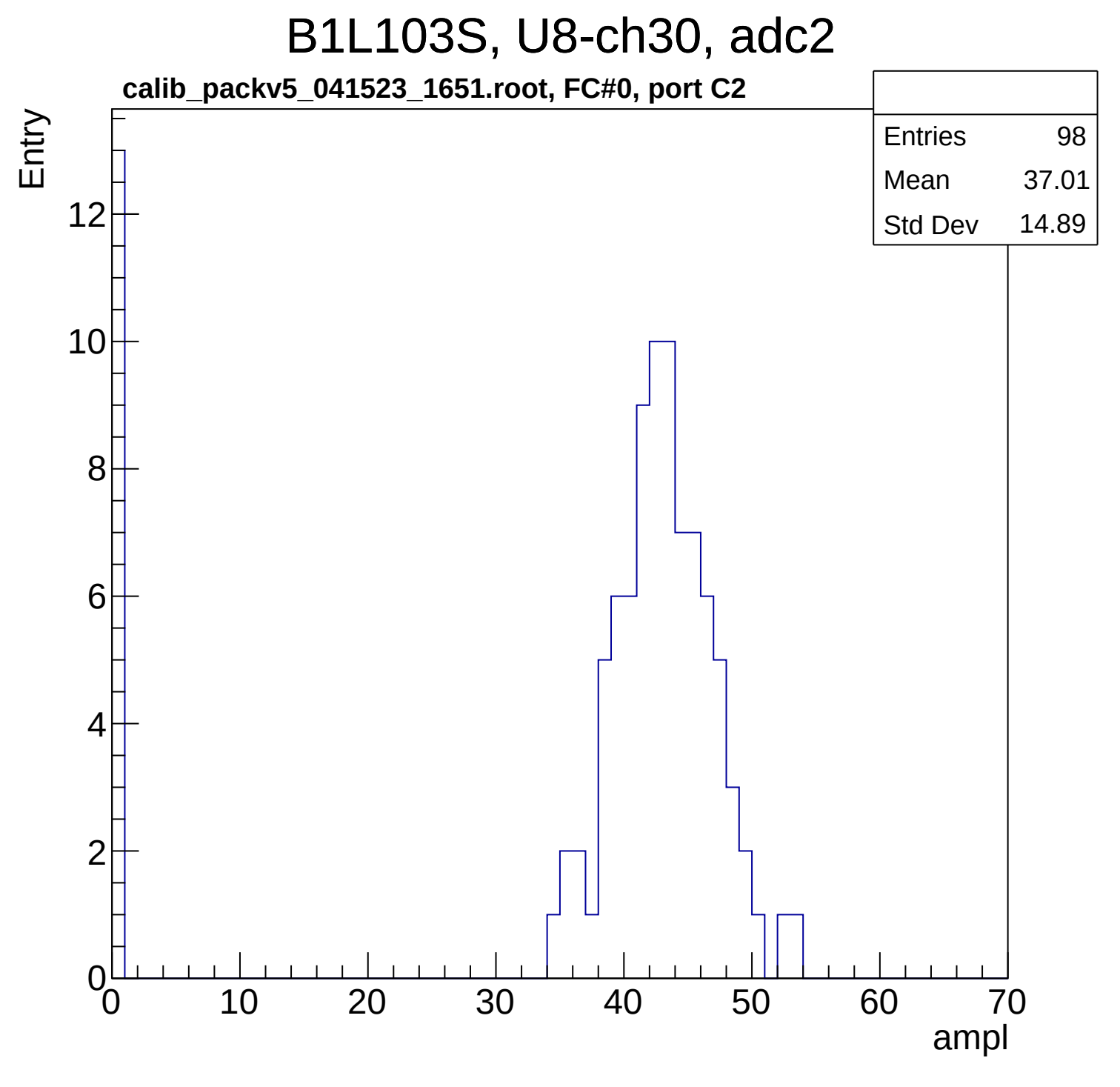
B1L103S, U8-ch30, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 98
Mean 37.01
Std Dev 14.89
Entry
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2
4
6
8
10
12
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10
20
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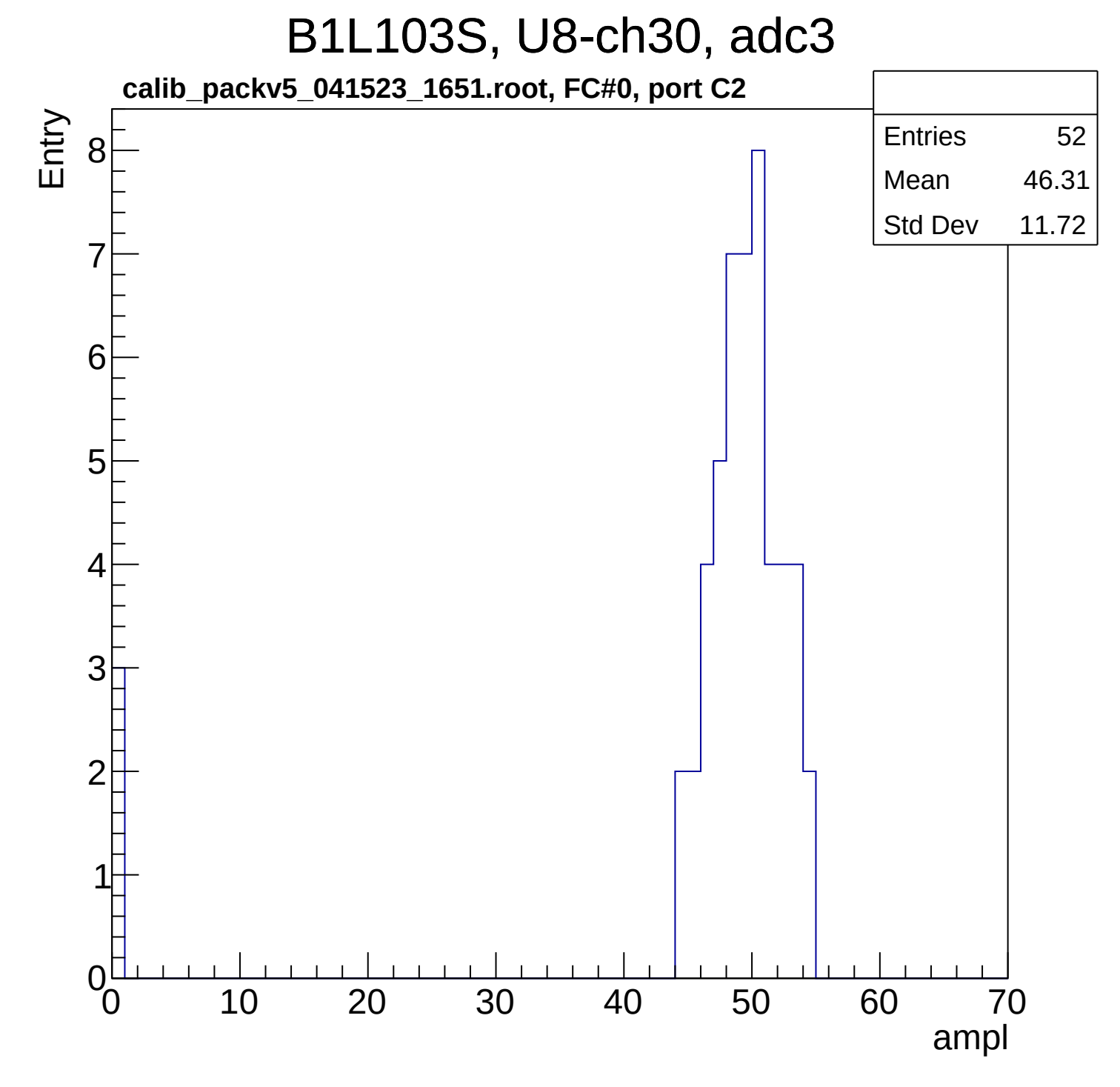
50
60
70
ampl


B1L103S, U8-ch30, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 46.31
Std Dev 11.72
Entry
ampl
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2
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4
5
6
7
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20
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40
50
60
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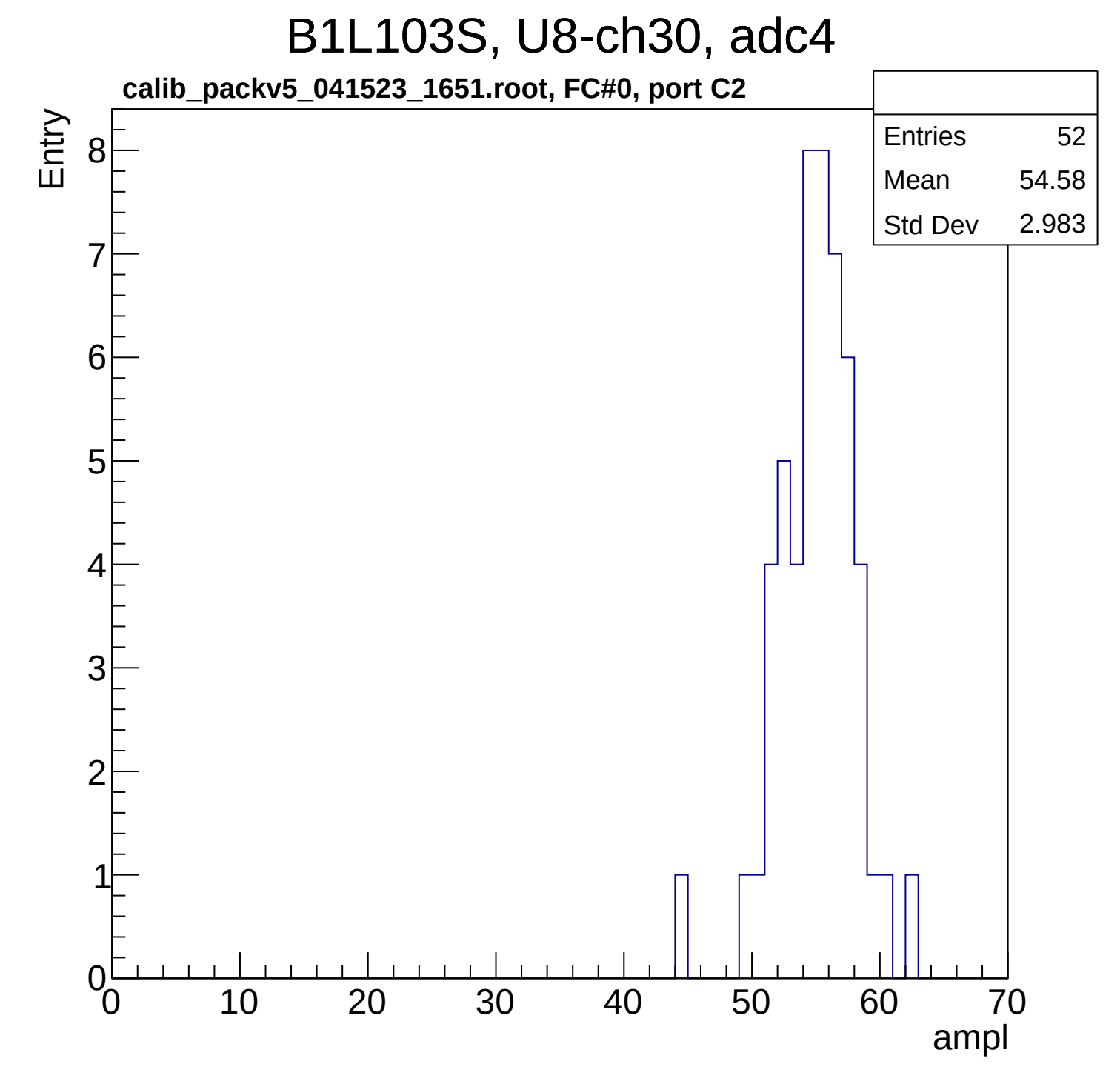
B1L103S, U8-ch30, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 54.58
Std Dev 2.983
Entry
ampl
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1
2
3
4
5
6
7
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0
10
20
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40
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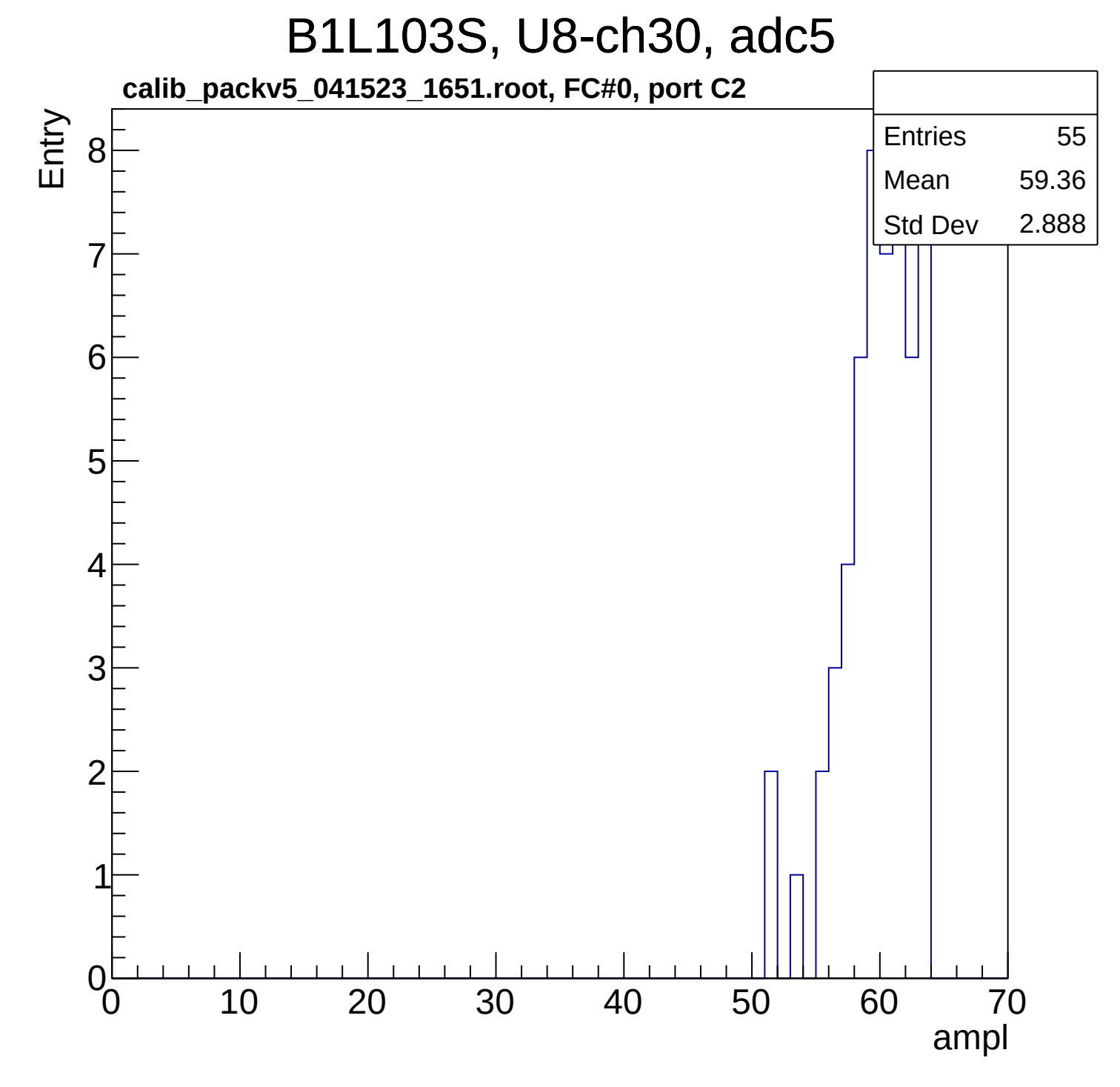
60
70


B1L103S, U8-ch30, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 59.36
Std Dev 2.888
Entry
ampl
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2
3
4
5
6
7
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0
10
20
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40
50
60
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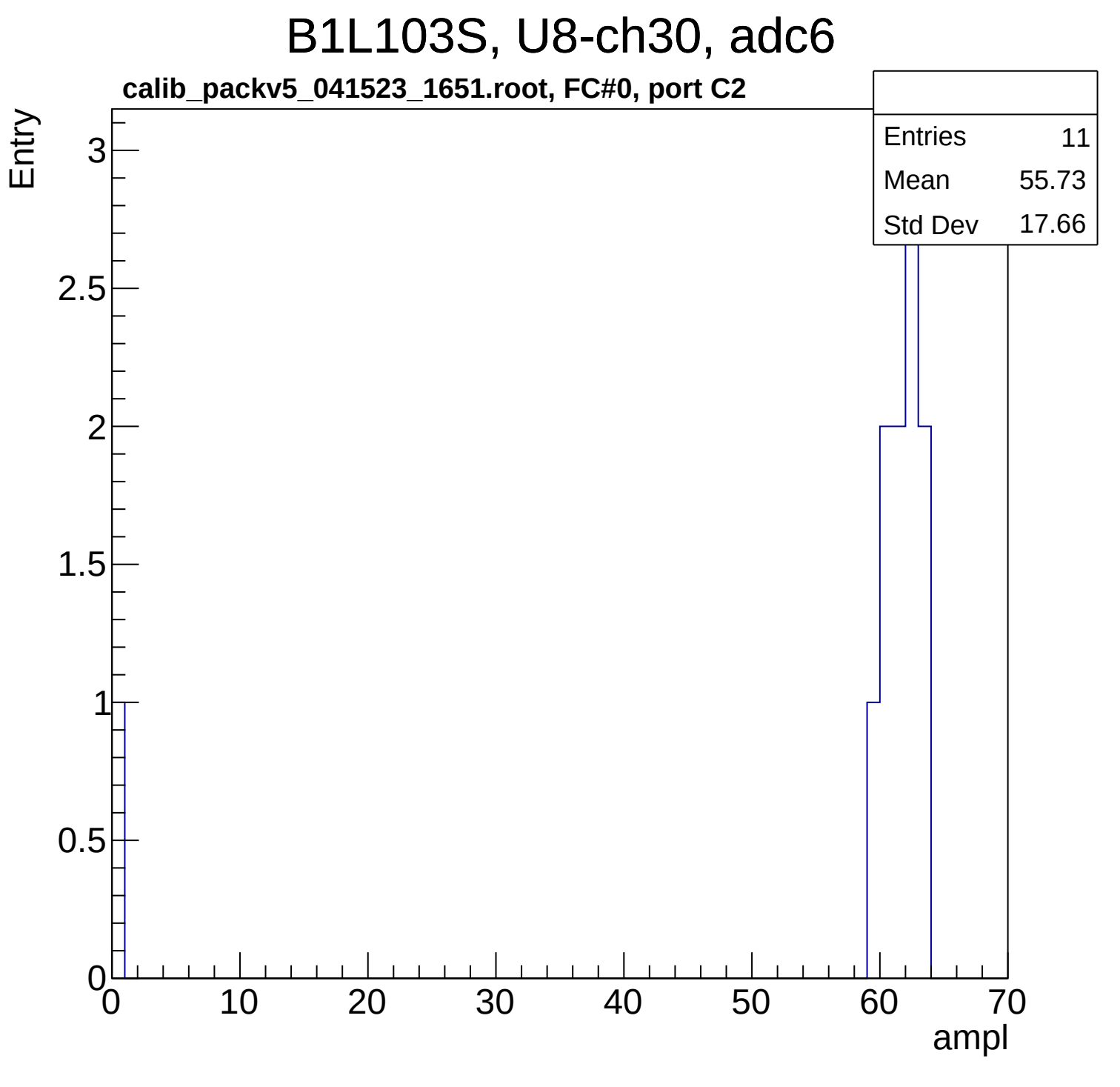
B1L103S, U8-ch30, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 55.73
Std Dev 17.66
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
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40
50
60
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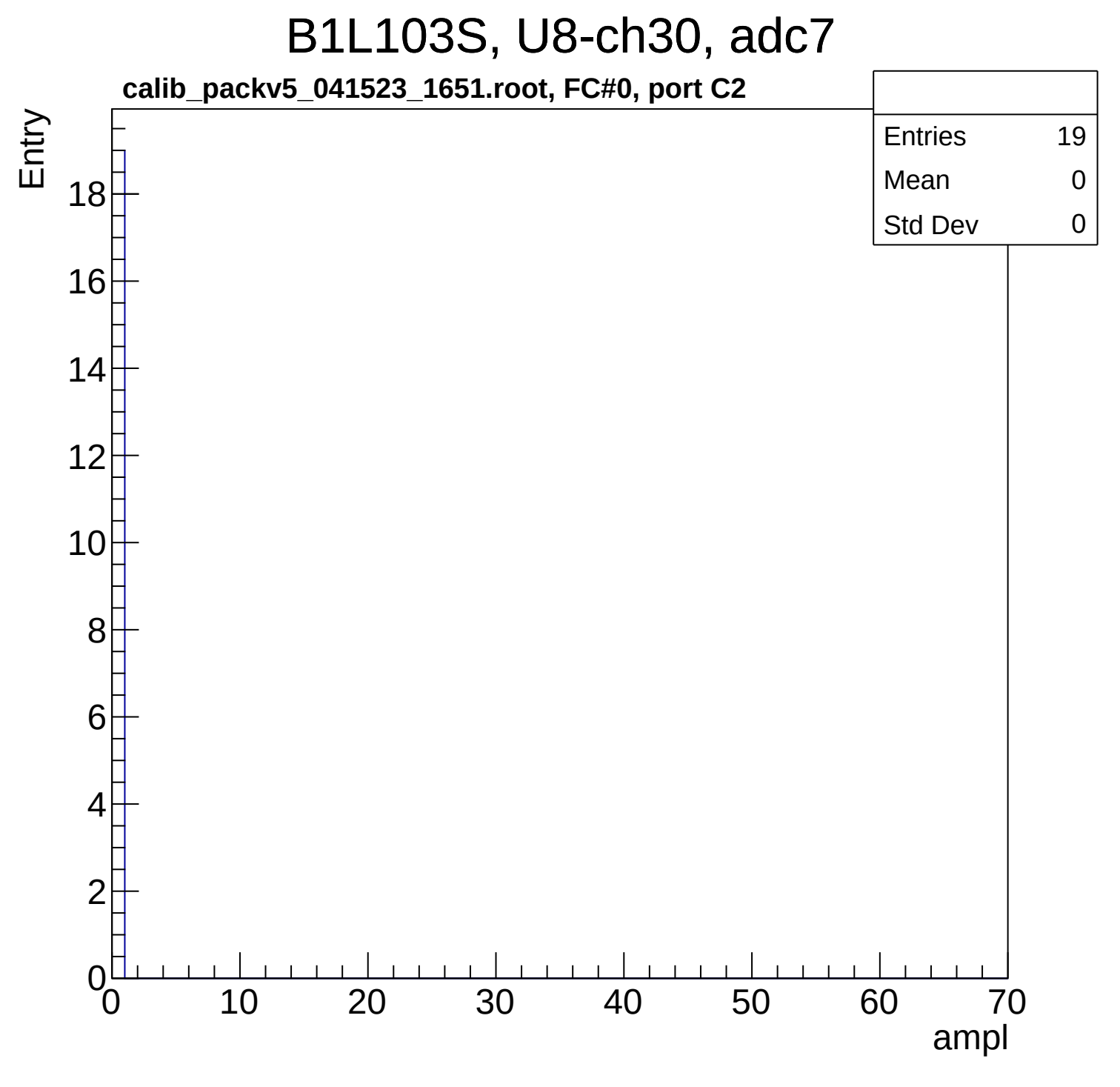
B1L103S, U8-ch30, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
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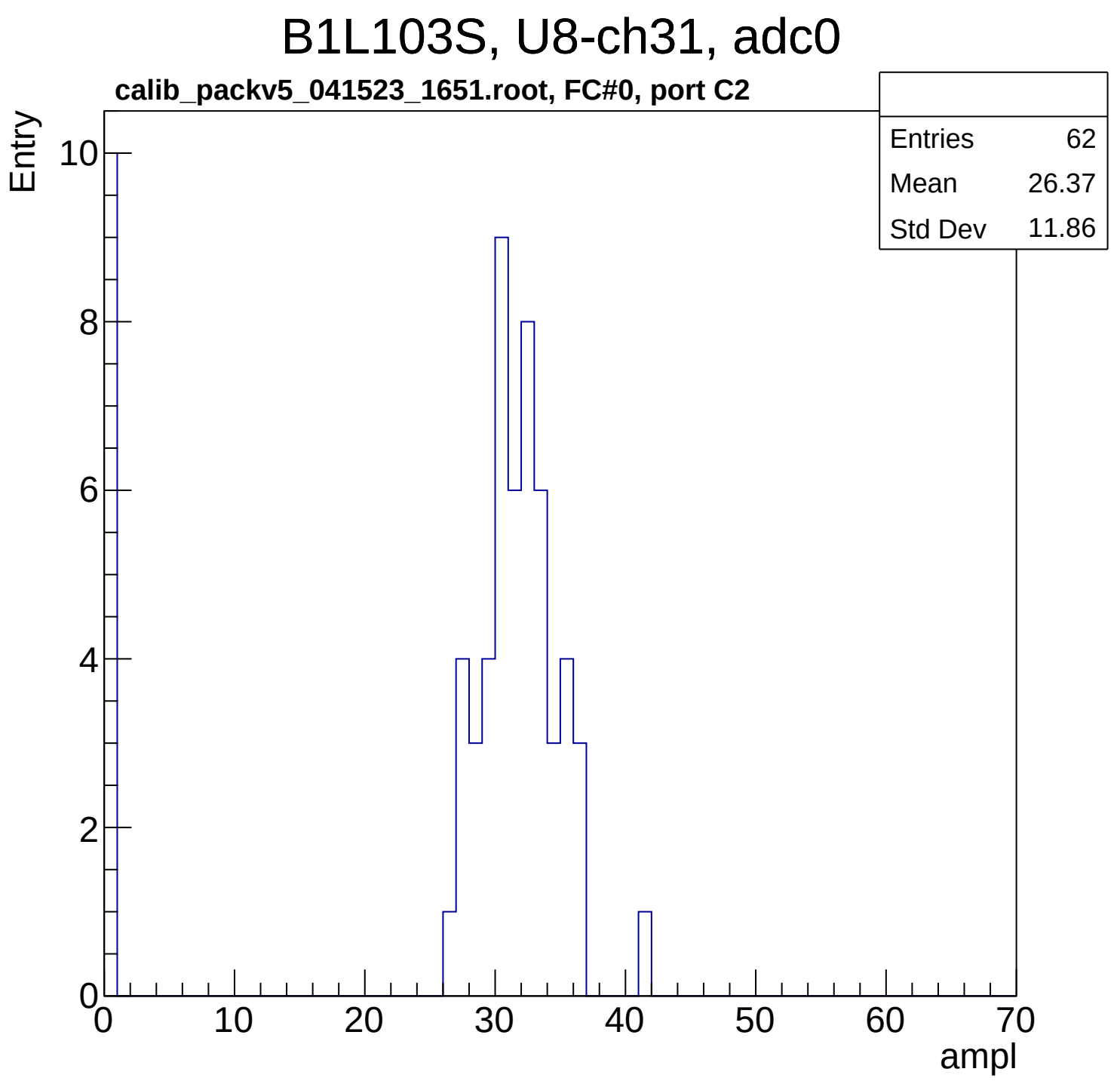
50
60
70
ampl


B1L103S, U8-ch31, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 26.37
Std Dev 11.86
Entry
ampl
0
2
4
6
8
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0
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20
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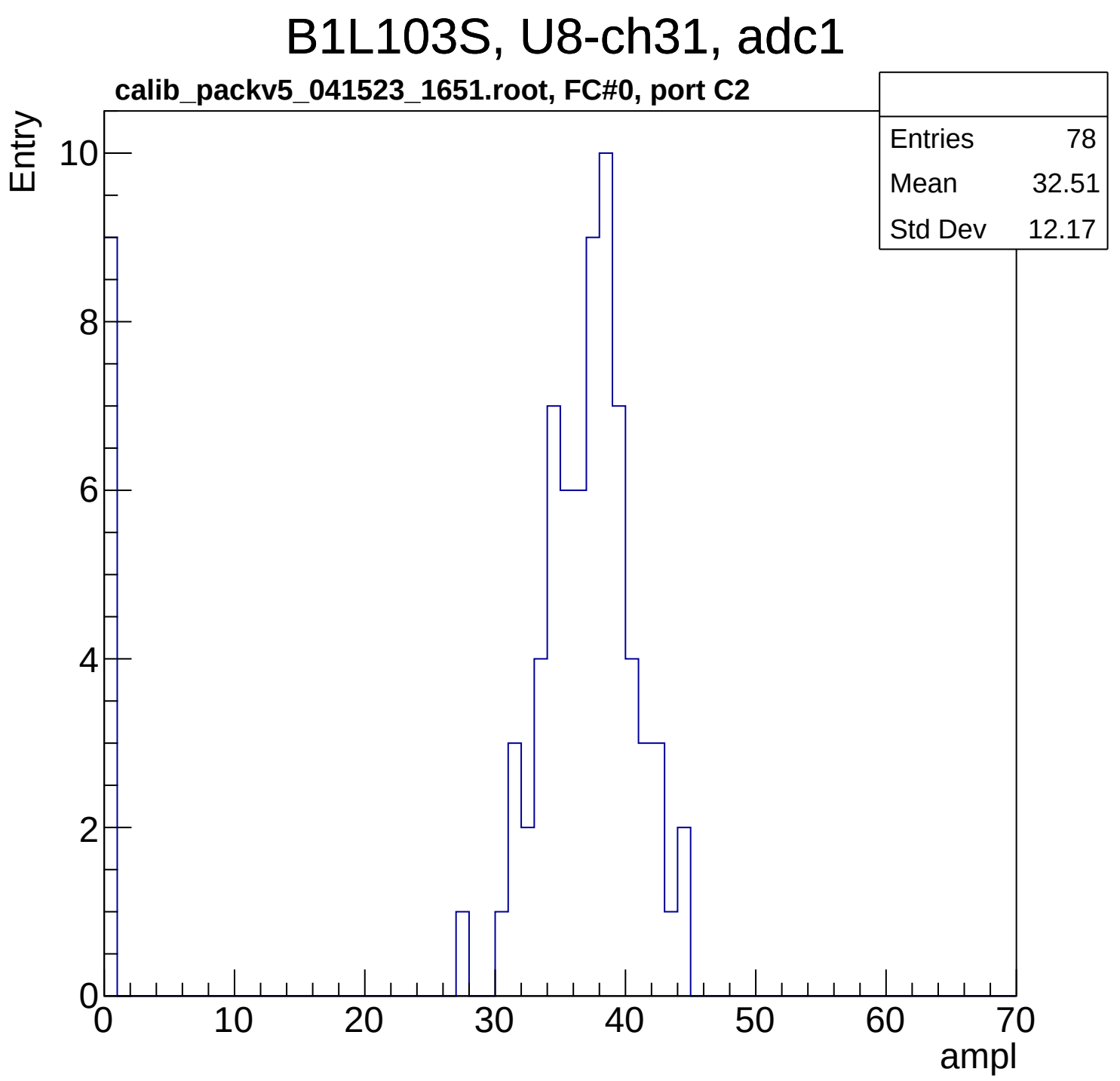
60
70


B1L103S, U8-ch31, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 32.51
Std Dev 12.17
Entry
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4
6
8
10
0
10
20
30
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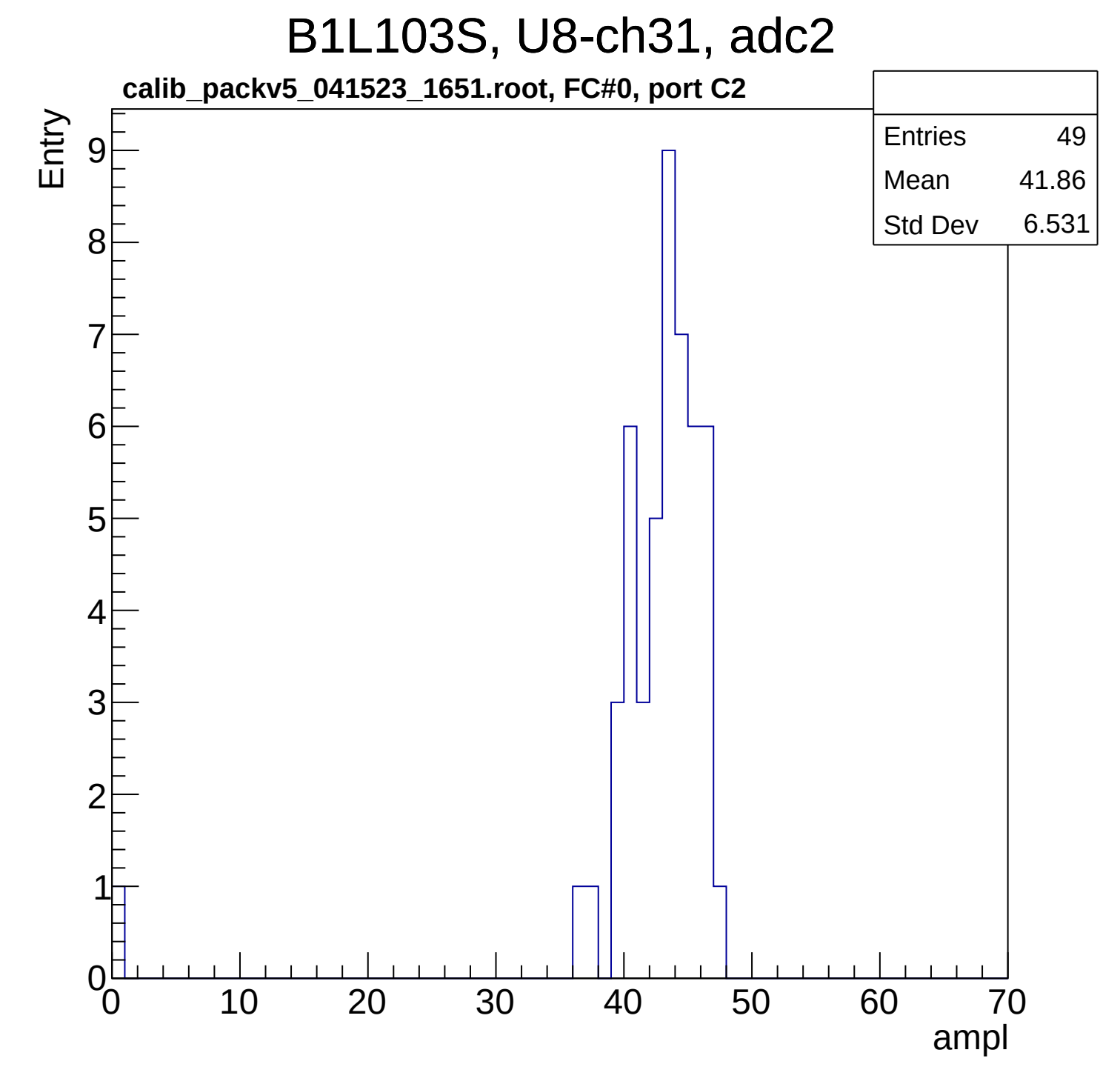
50
60
70
ampl


B1L103S, U8-ch31, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 41.86
Std Dev 6.531
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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60
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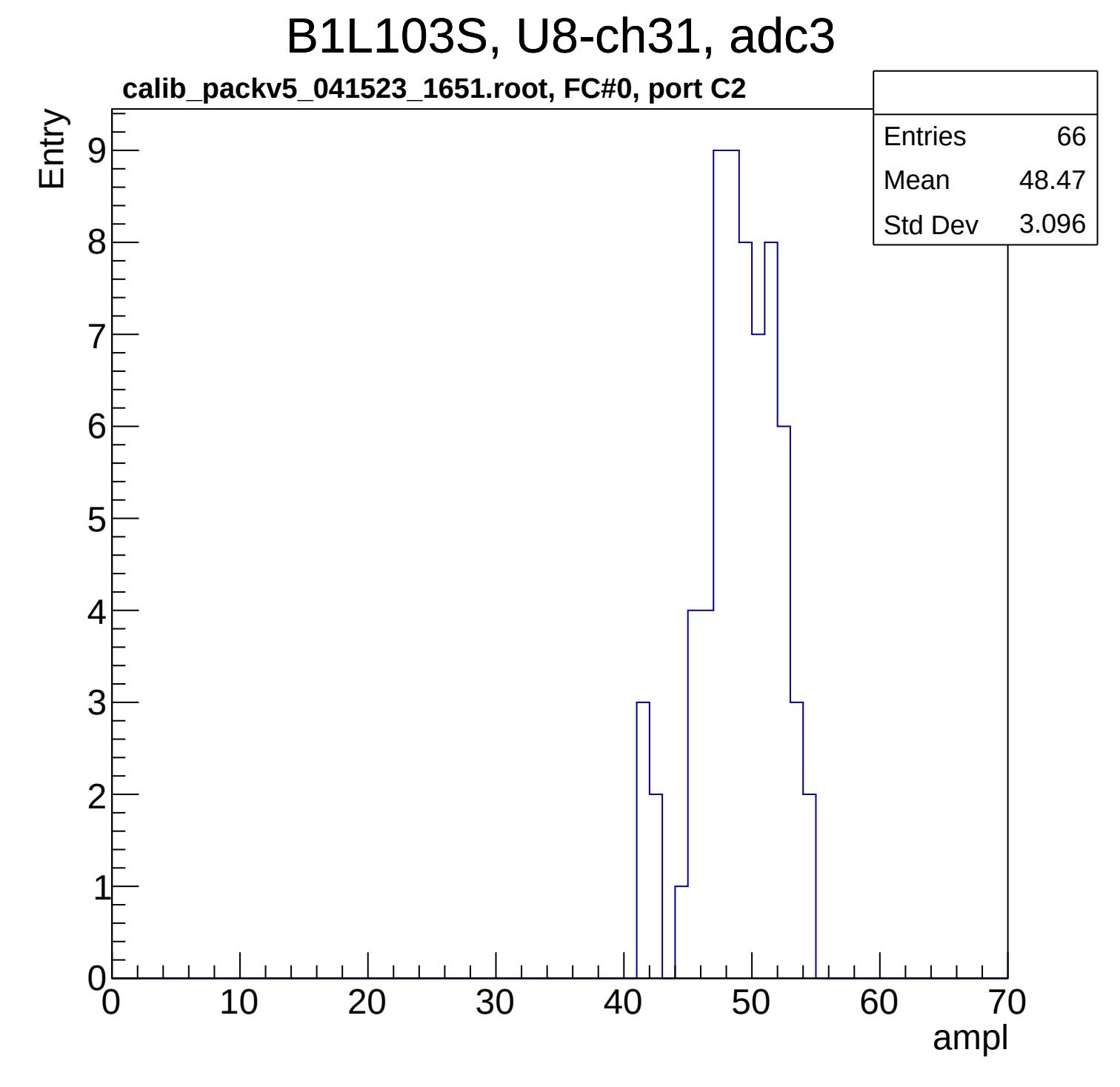
B1L103S, U8-ch31, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 48.47
Std Dev 3.096
Entry
ampl
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2
3
4
5
6
7
8
9
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60
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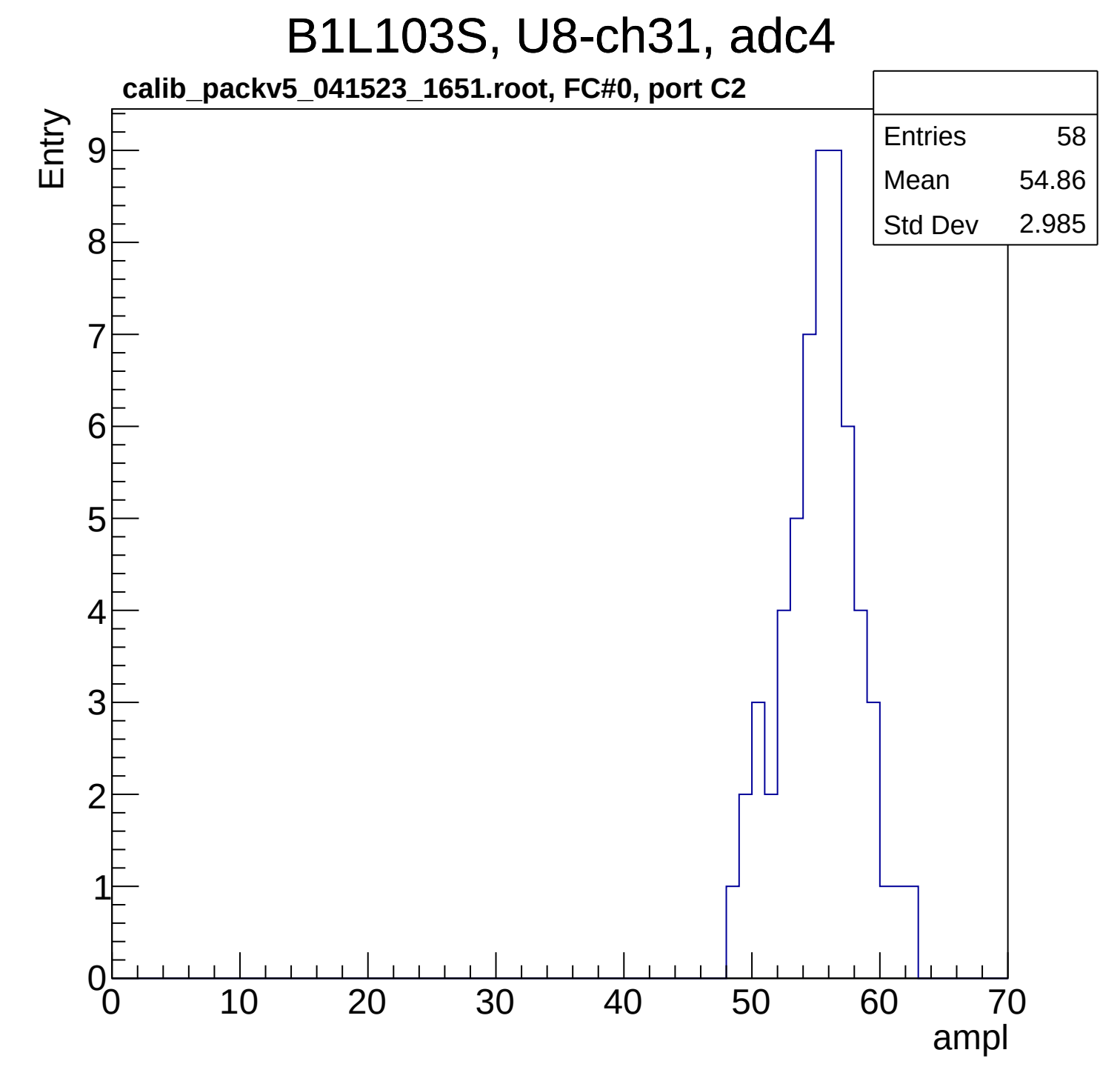
B1L103S, U8-ch31, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 54.86
Std Dev 2.985
Entry
ampl
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2
3
4
5
6
7
8
9
0
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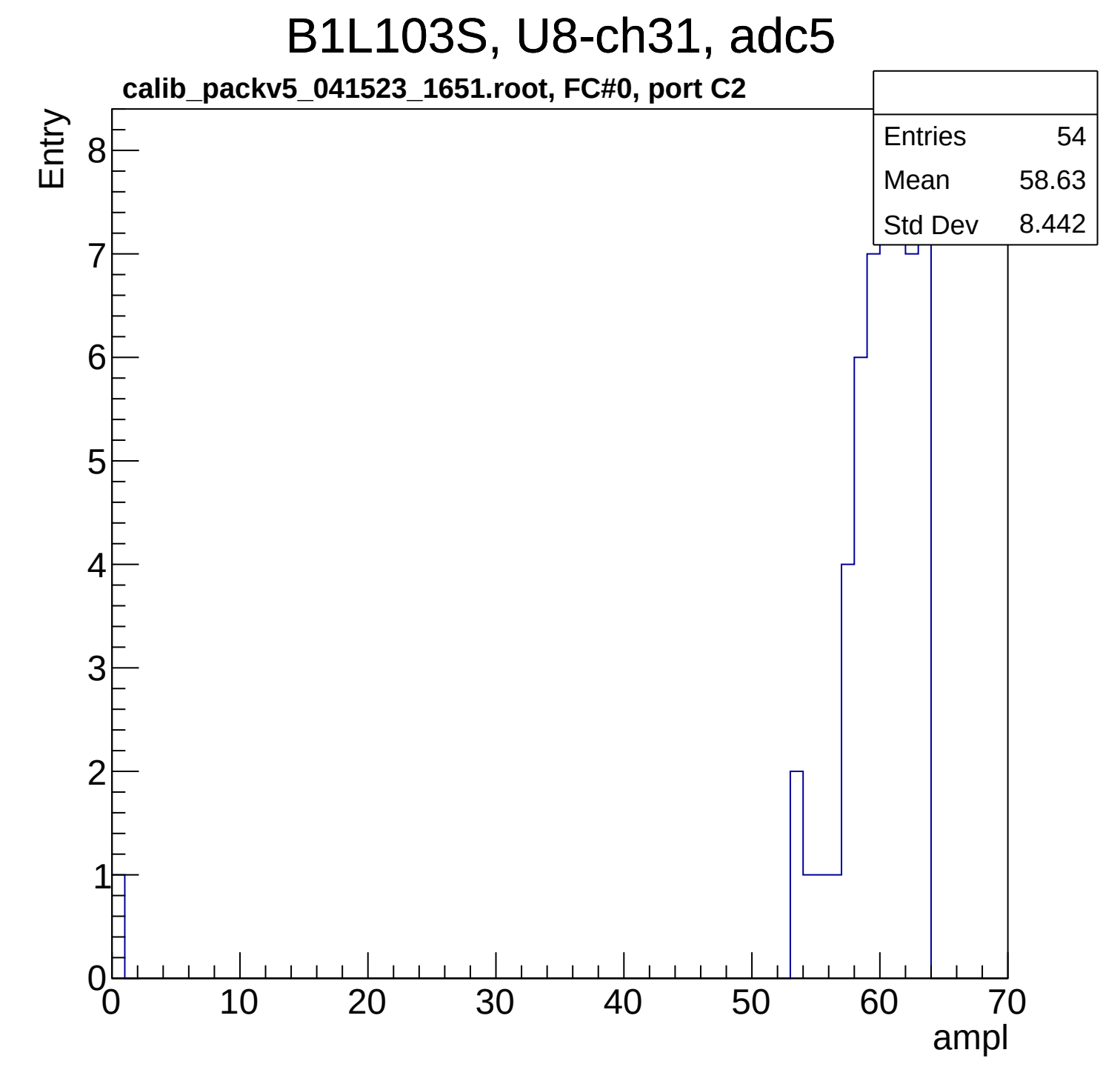
B1L103S, U8-ch31, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 58.63
Std Dev 8.442
Entry
ampl
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1
2
3
4
5
6
7
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60
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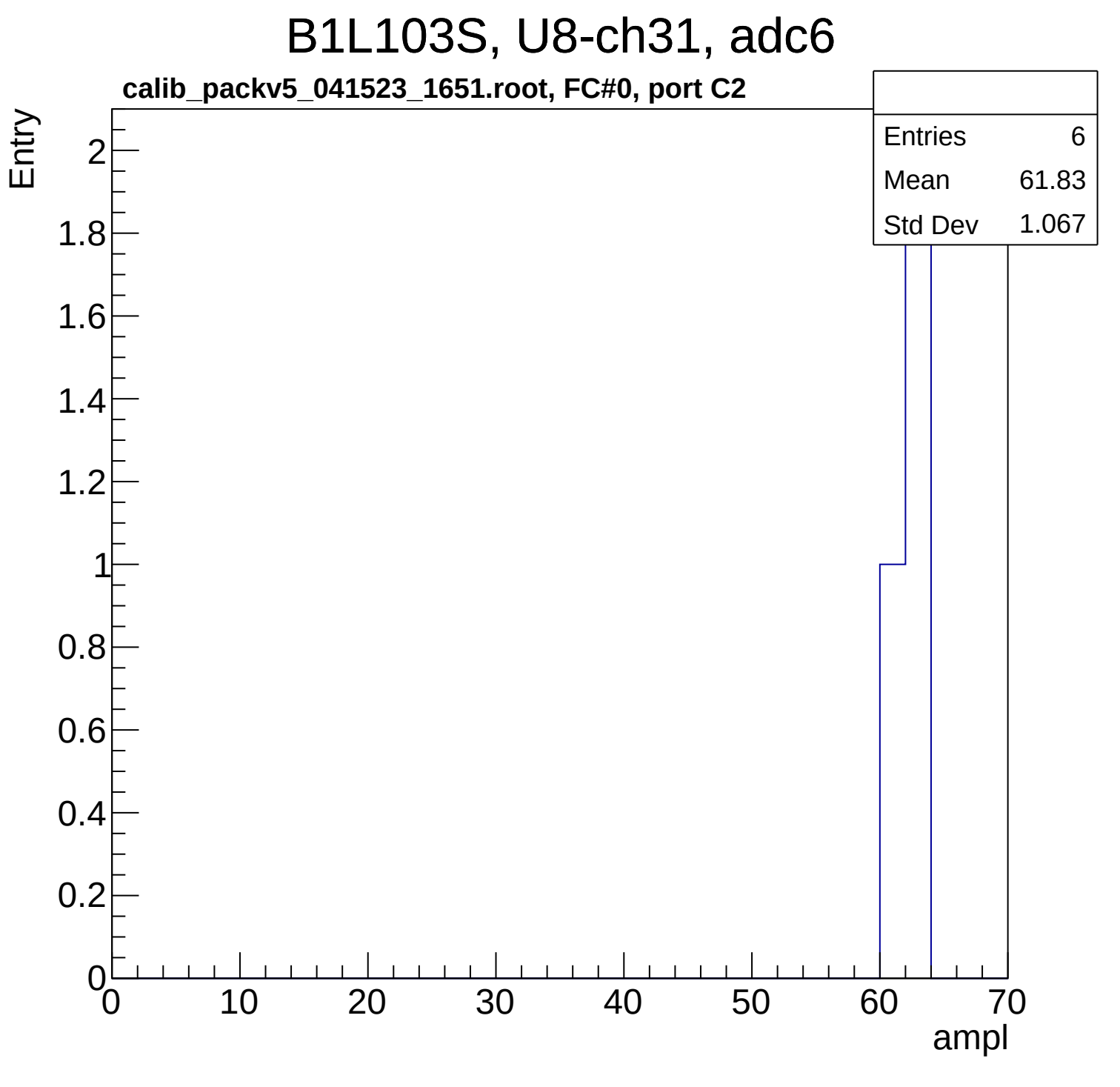
B1L103S, U8-ch31, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 61.83
Std Dev 1.067
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
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0
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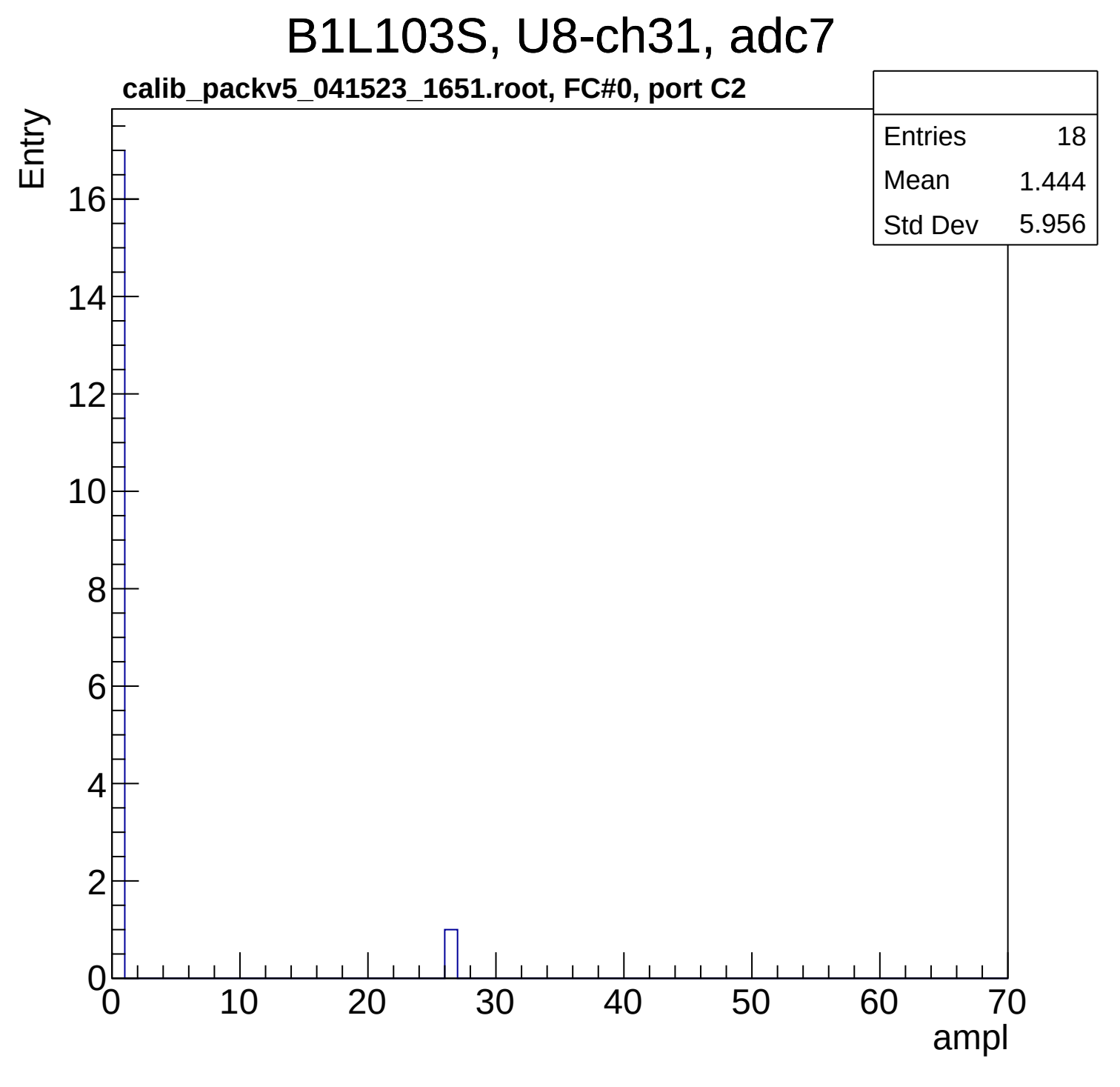
40
50
60
70


B1L103S, U8-ch31, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.444
Std Dev 5.956
Entry
0
2
4
6
8
10
12
14
16
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10
20
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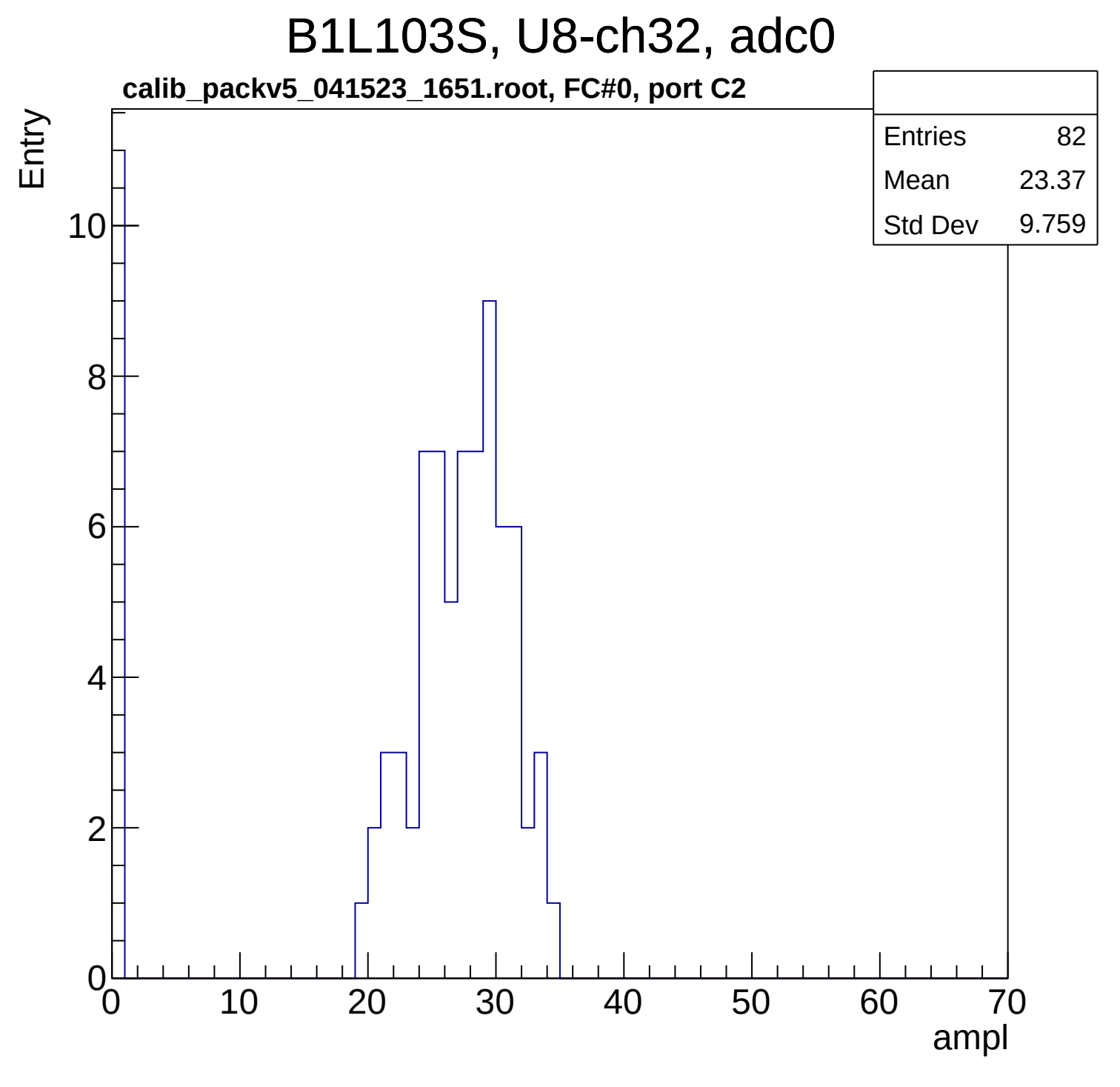
50
60
70
ampl


B1L103S, U8-ch32, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 23.37
Std Dev 9.759
Entry
0
2
4
6
8
10
0
10
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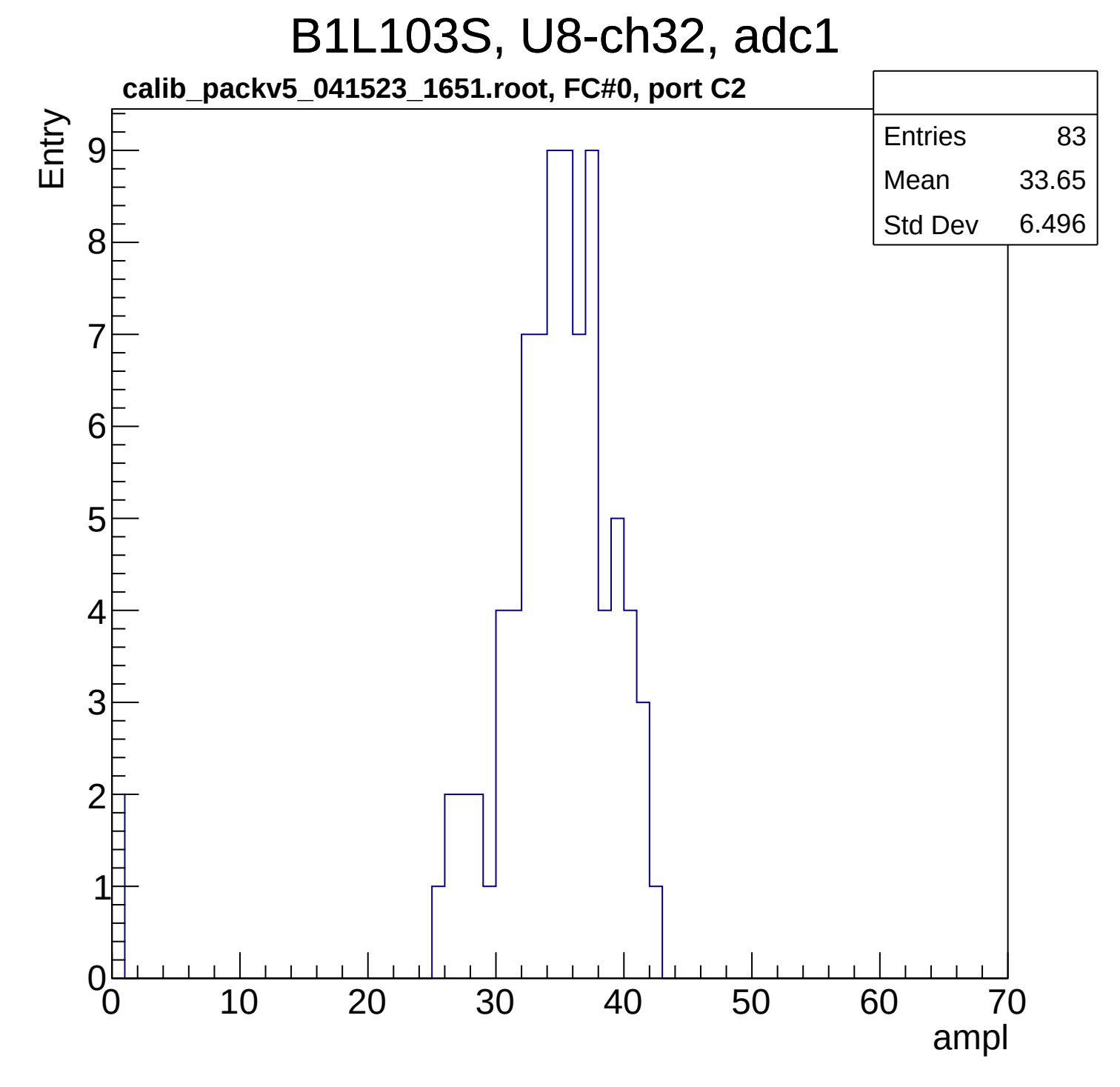
50
60
70
ampl


B1L103S, U8-ch32, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 33.65
Std Dev 6.496
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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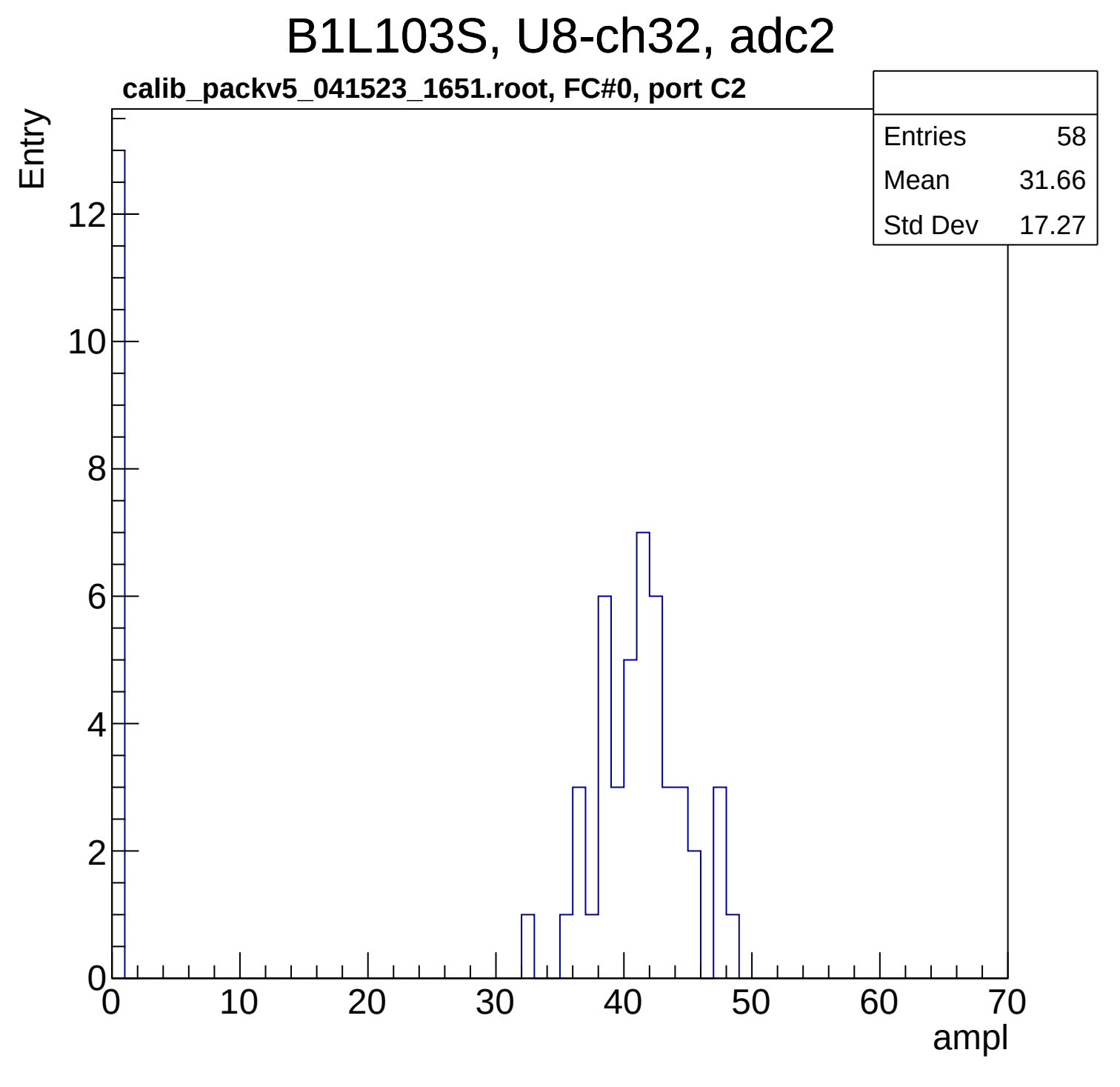
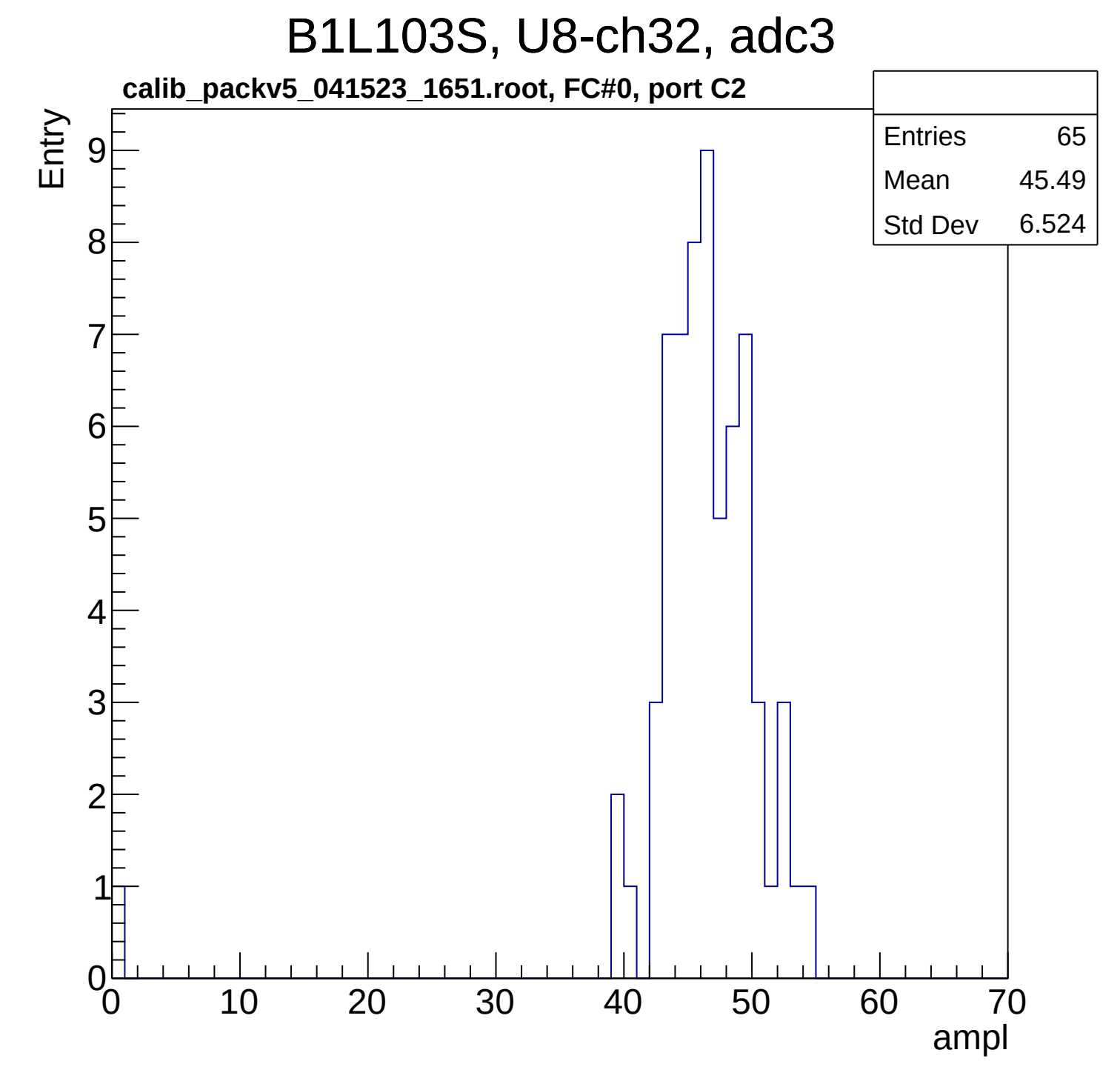
30
40
50
60
70


B1L103S, U8-ch32, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 31.66
Std Dev 17.27
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch32, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 45.49
Std Dev 6.524
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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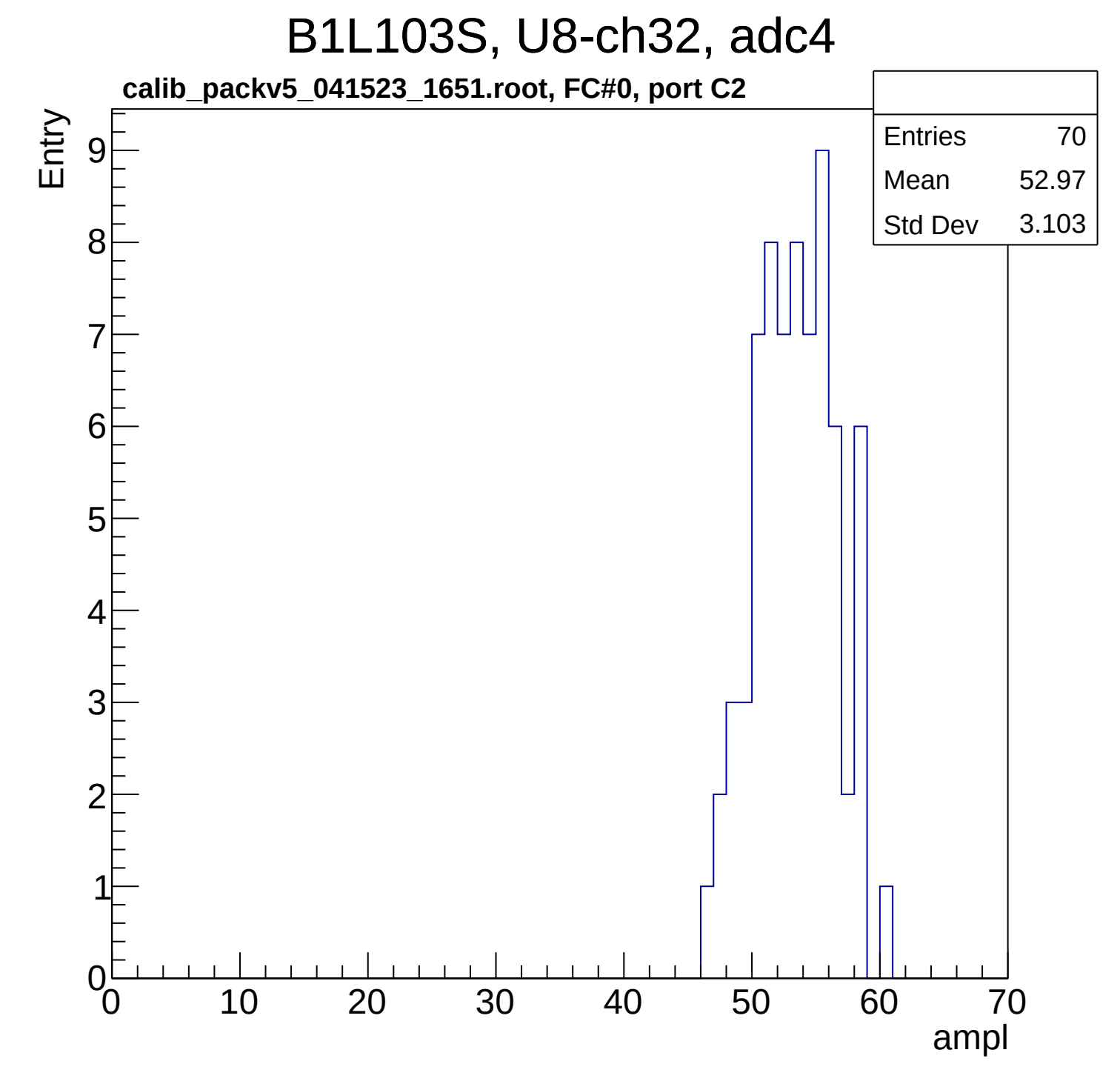
40
50
60
70


B1L103S, U8-ch32, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 52.97
Std Dev 3.103
Entry
ampl
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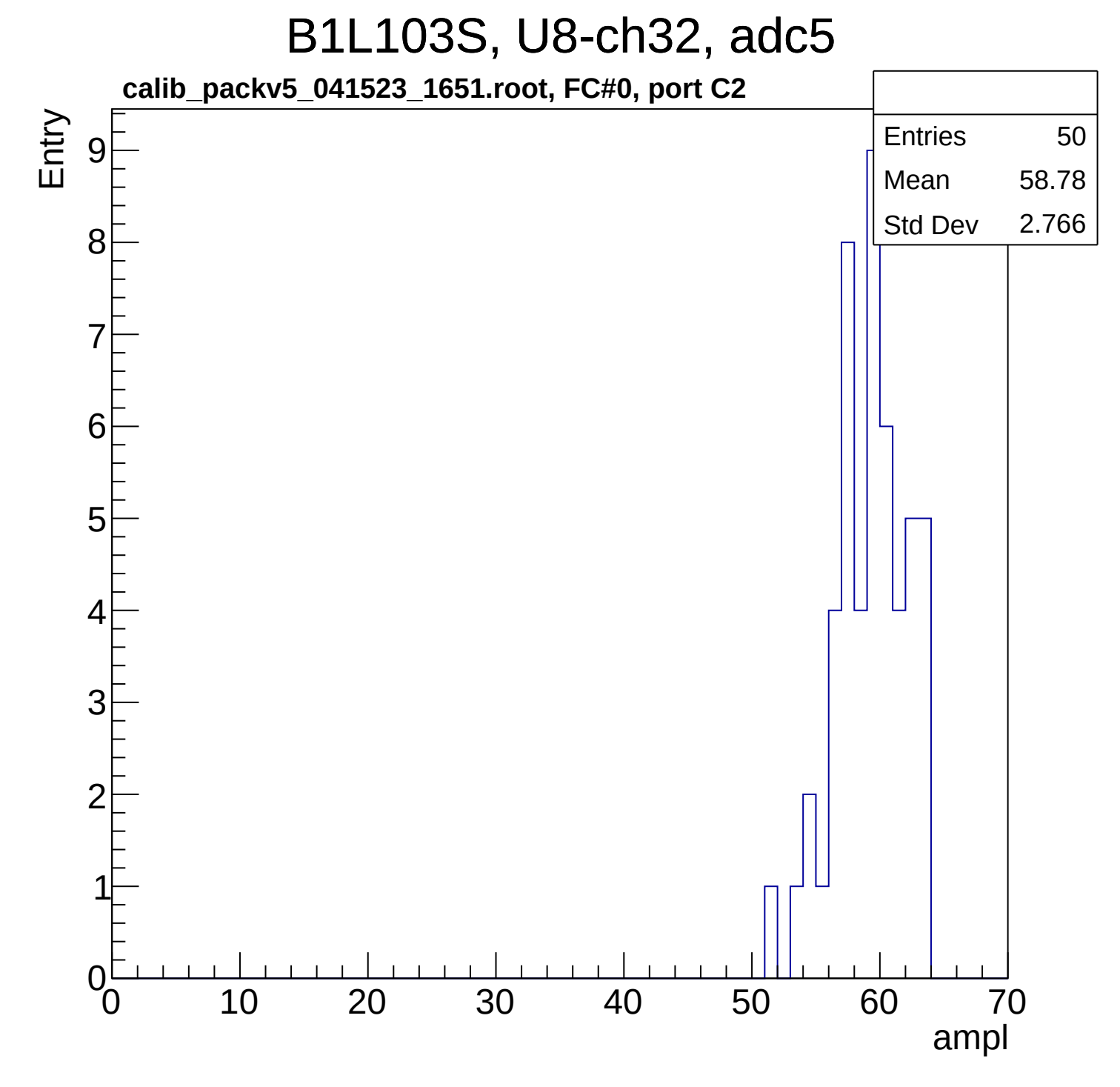
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U8-ch32, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 58.78
Std Dev 2.766
Entry
ampl
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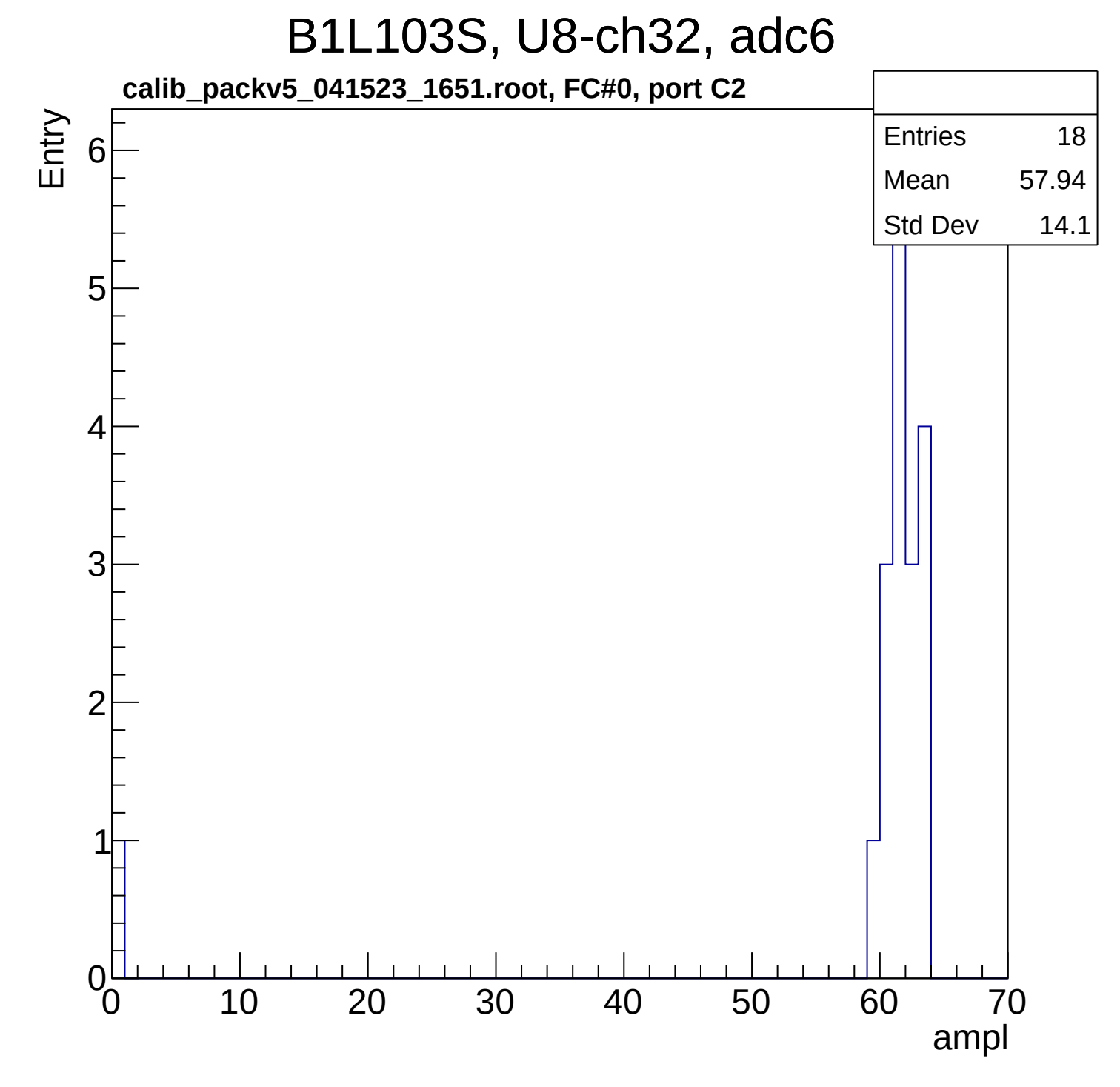
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U8-ch32, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 57.94
Std Dev 14.1
Entry
ampl
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2
3
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0
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20
30
40
50
60
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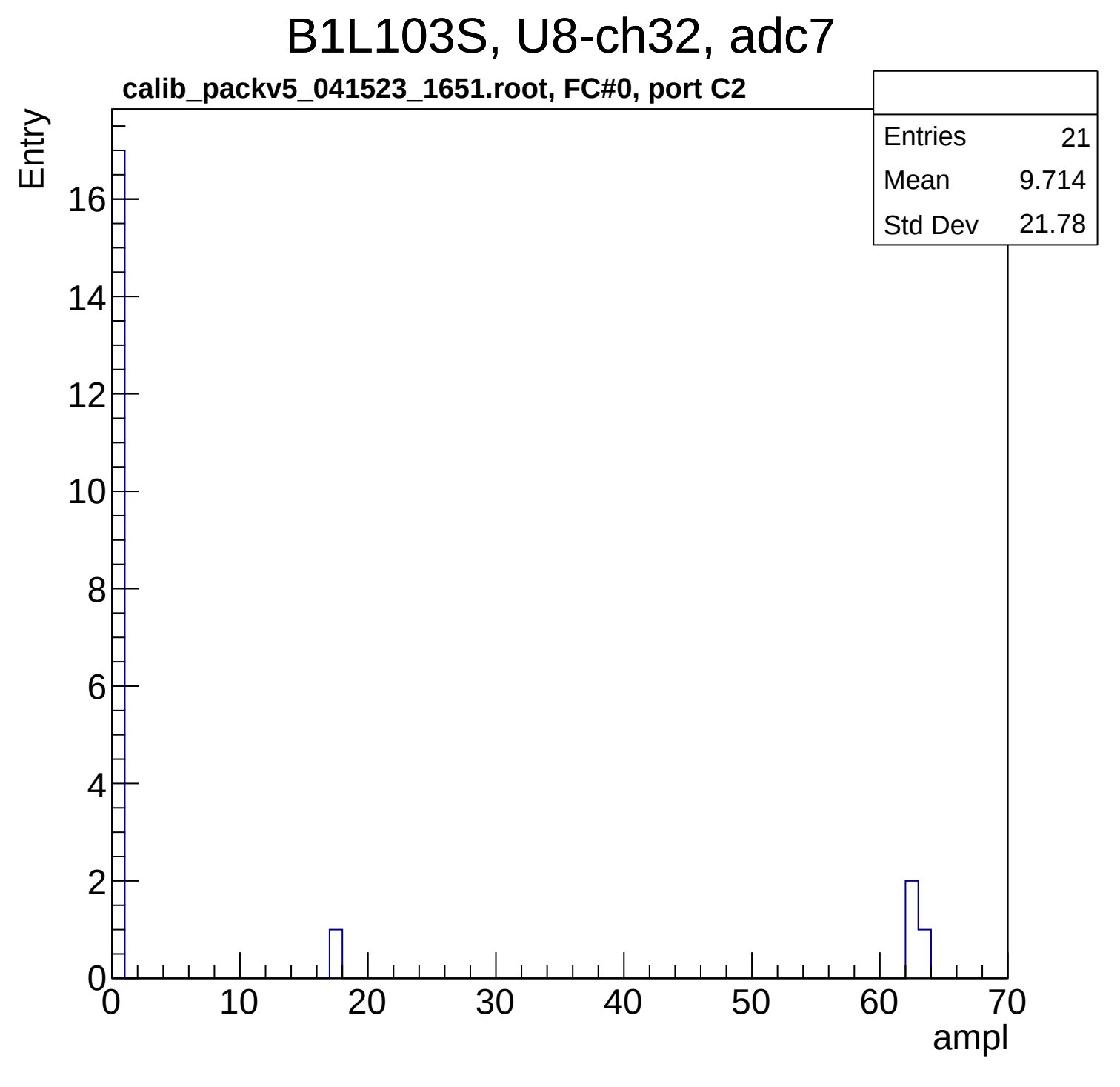
B1L103S, U8-ch32, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 9.714
Std Dev 21.78
Entry
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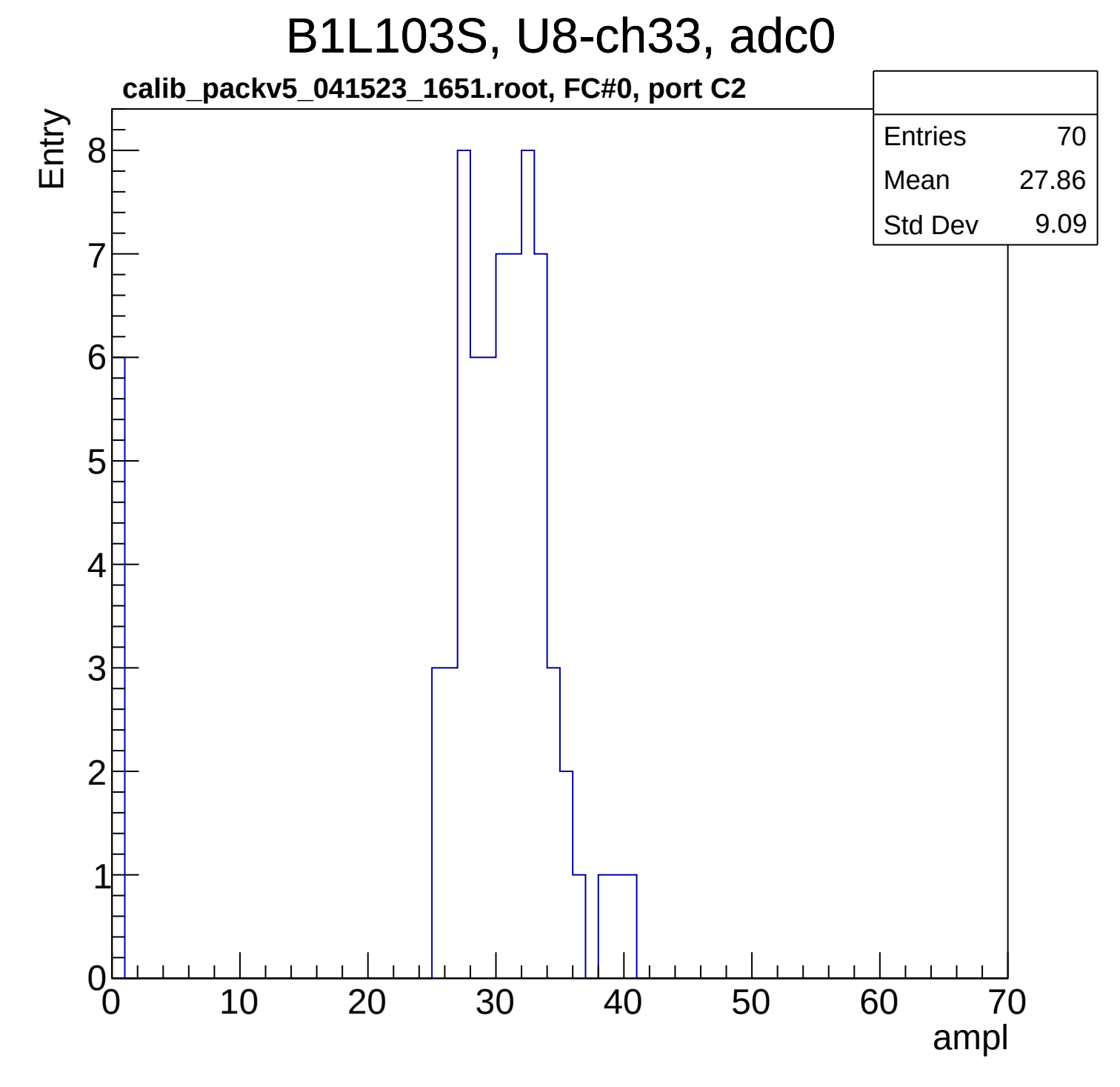
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch33, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 27.86
Std Dev 9.09
Entry
ampl
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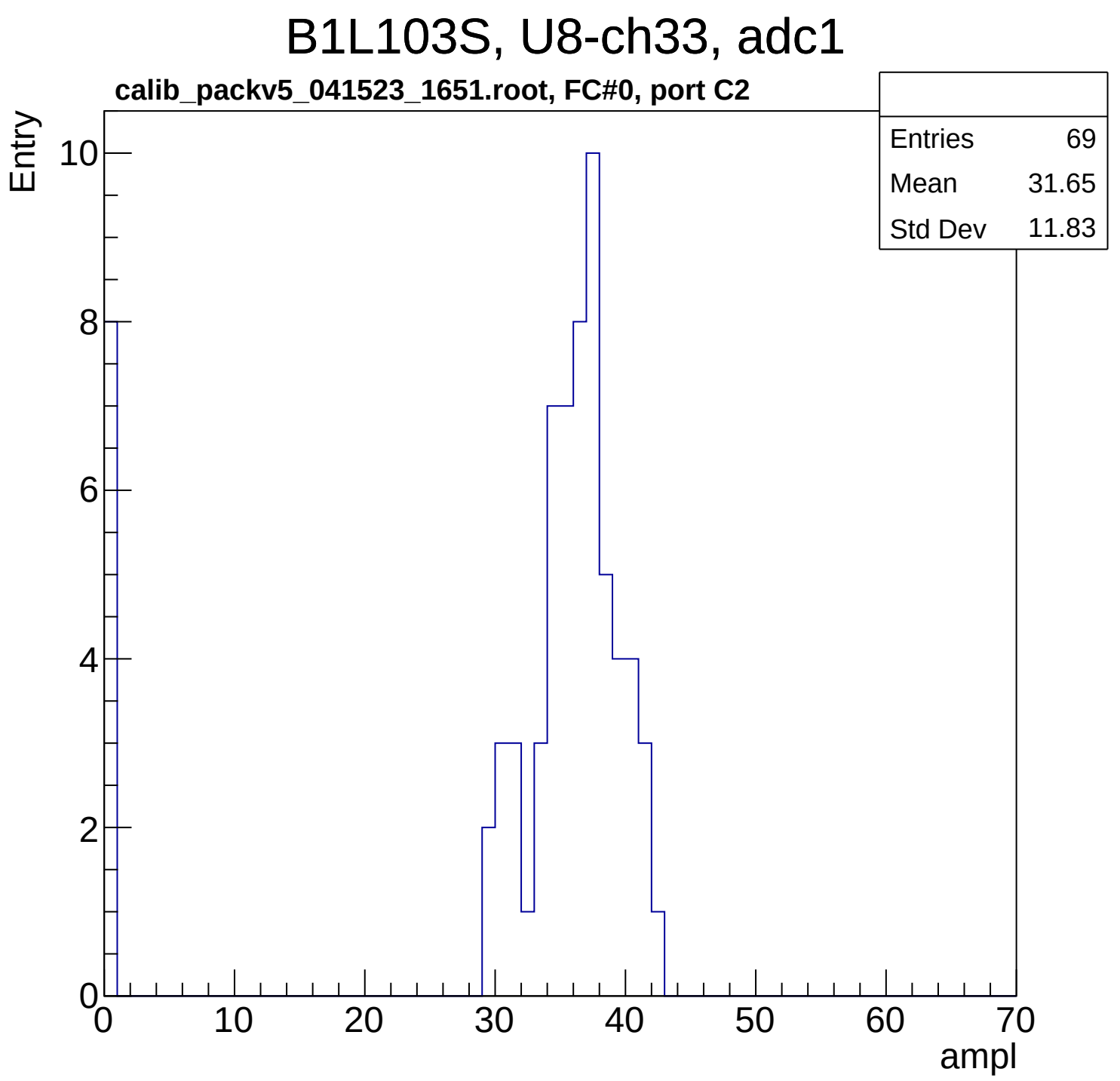
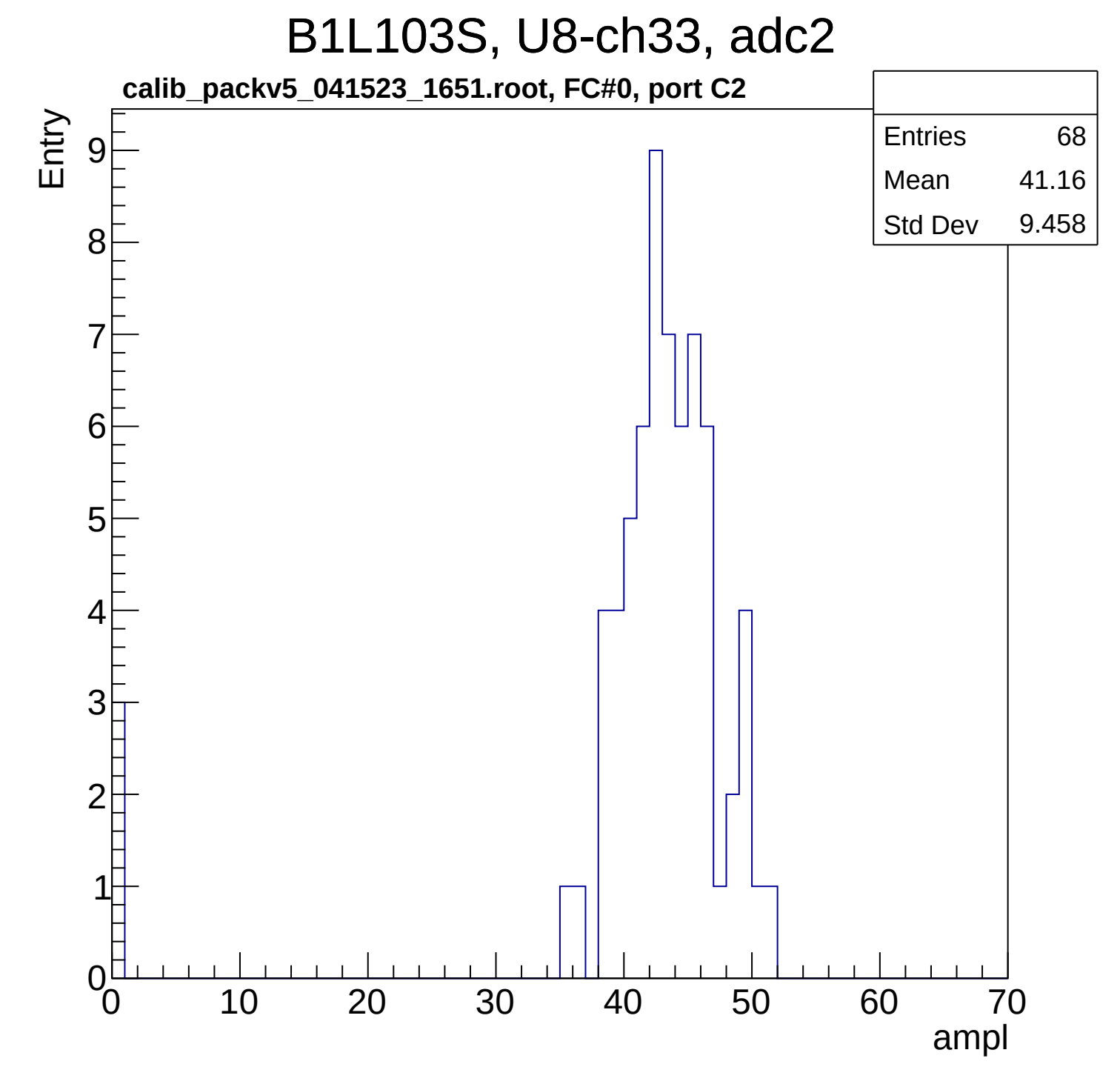
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch33, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 31.65
Std Dev 11.83
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch33, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 41.16
Std Dev 9.458
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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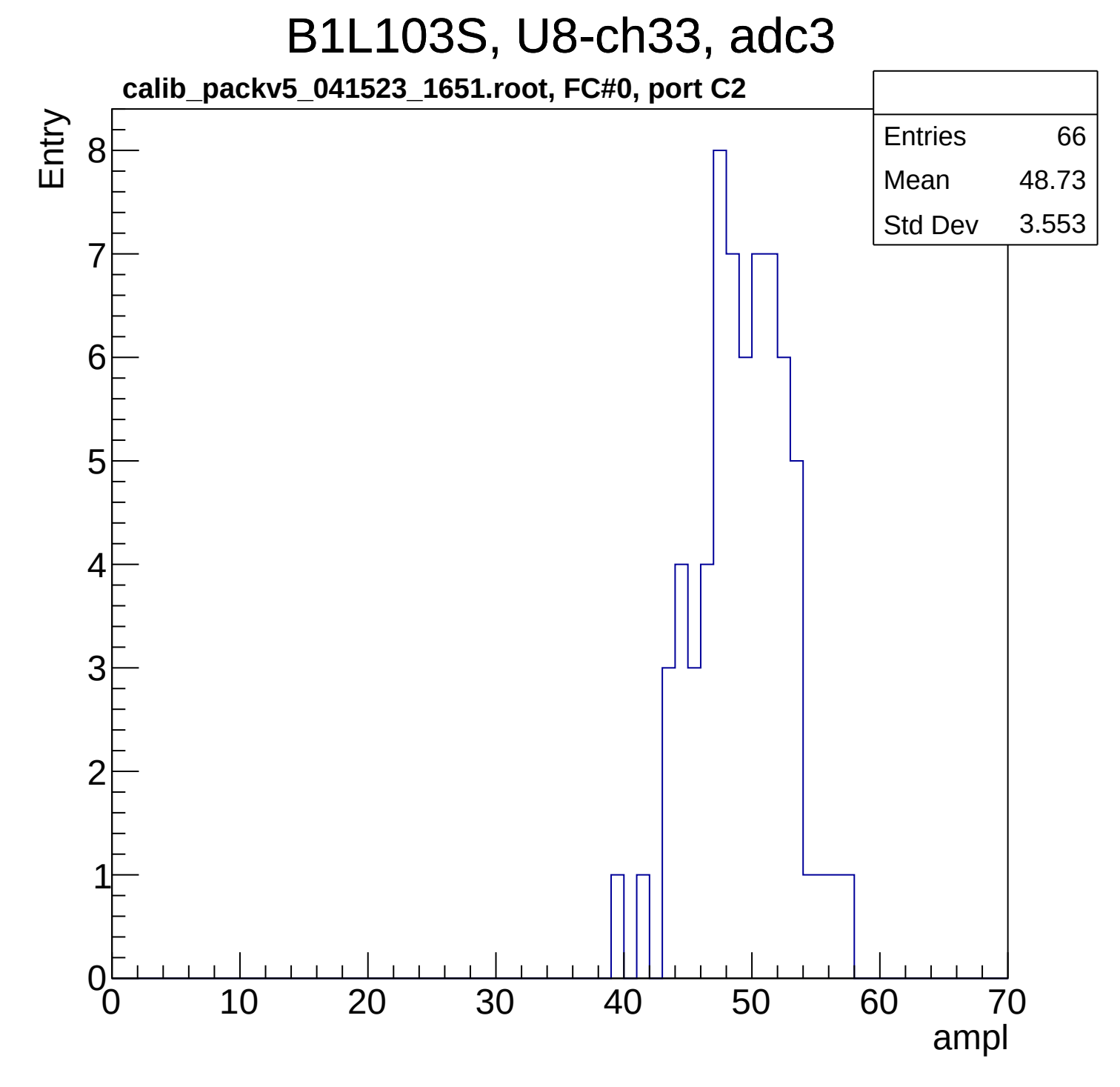
B1L103S, U8-ch33, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 48.73
Std Dev 3.553
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
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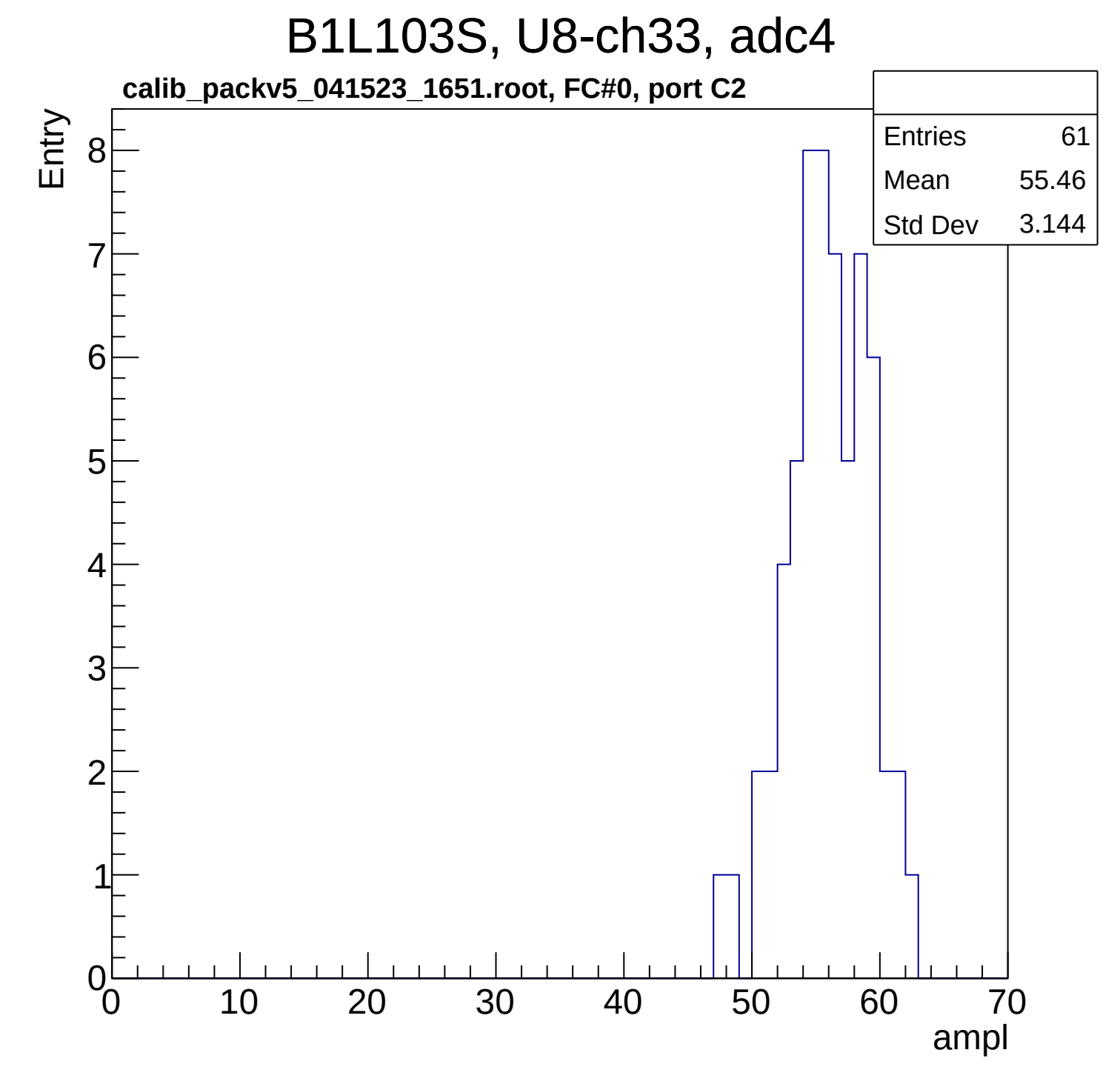
40
50
60
70


B1L103S, U8-ch33, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 55.46
Std Dev 3.144
Entry
ampl
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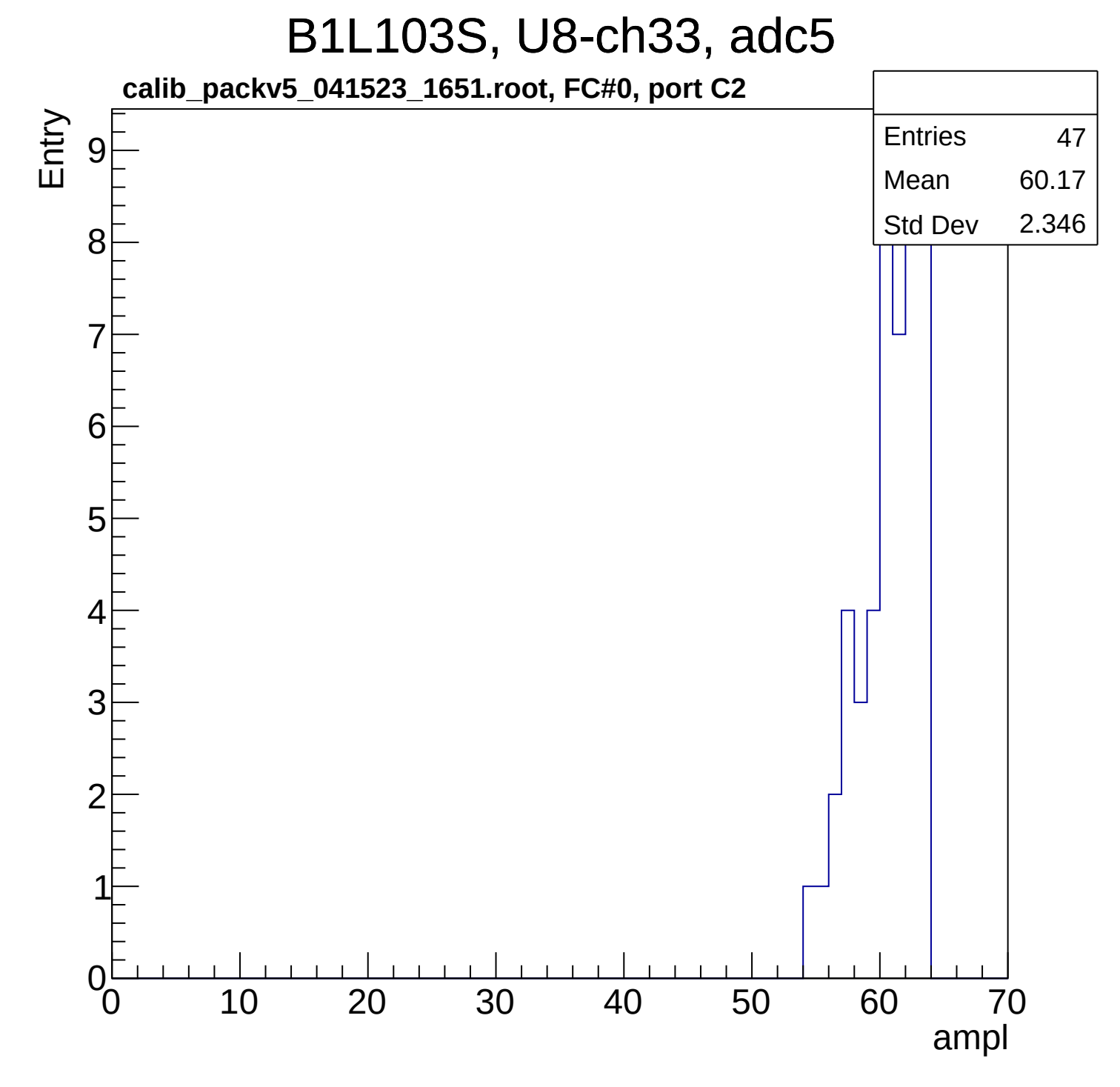
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch33, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 60.17
Std Dev 2.346
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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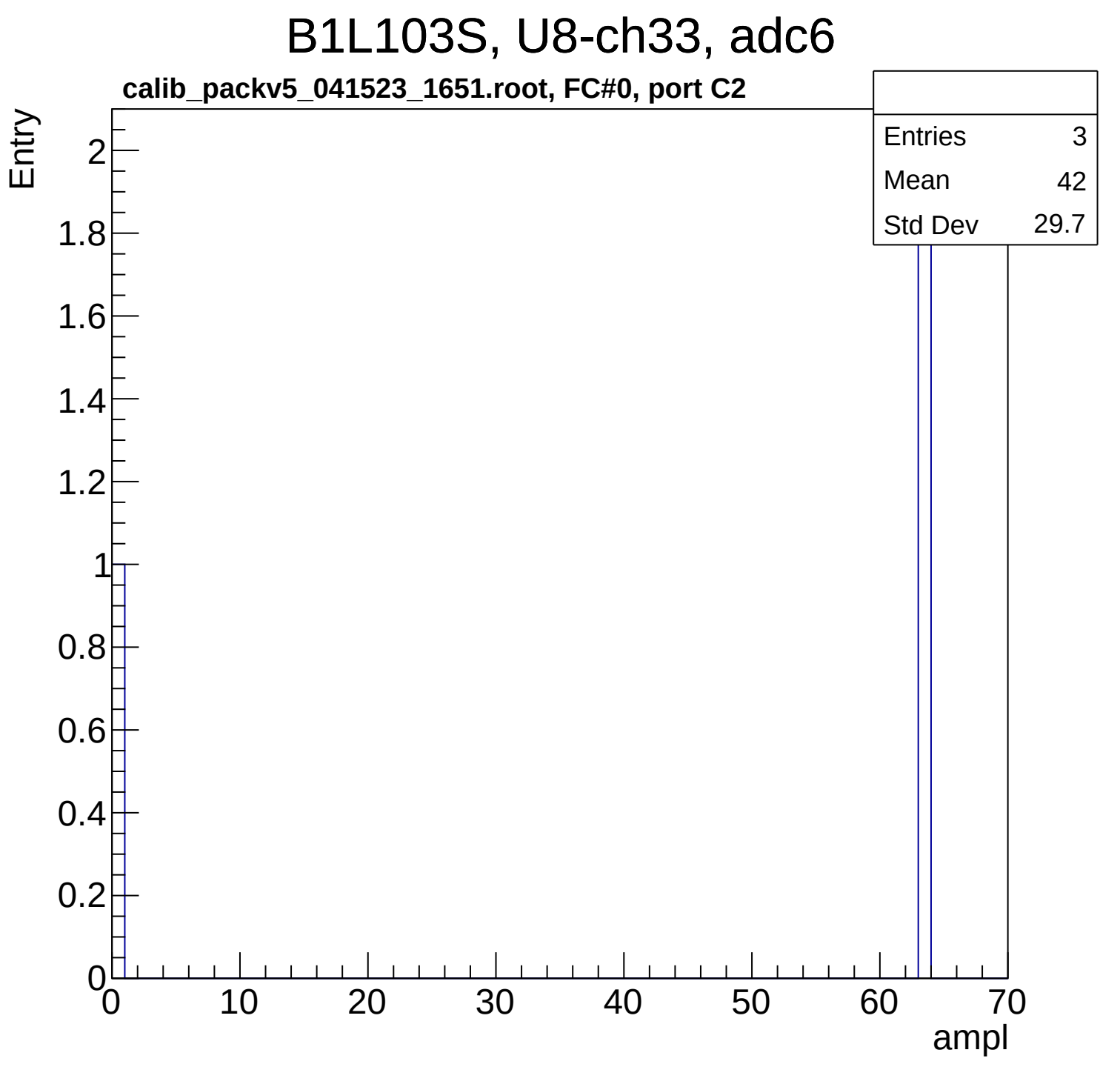
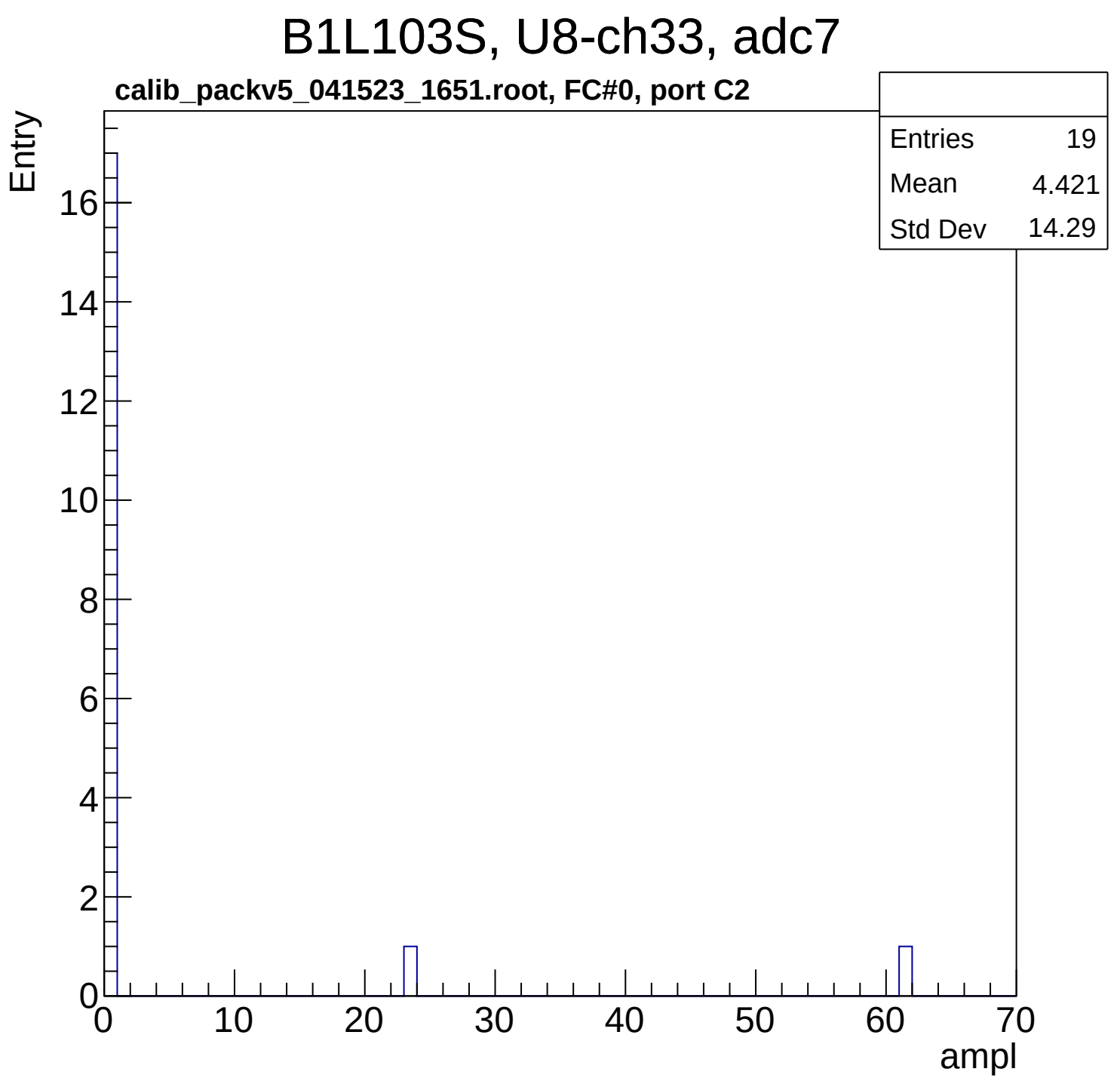
40
50
60
70


B1L103S, U8-ch33, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 42
Std Dev 29.7
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U8-ch33, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 4.421
Std Dev 14.29
Entry
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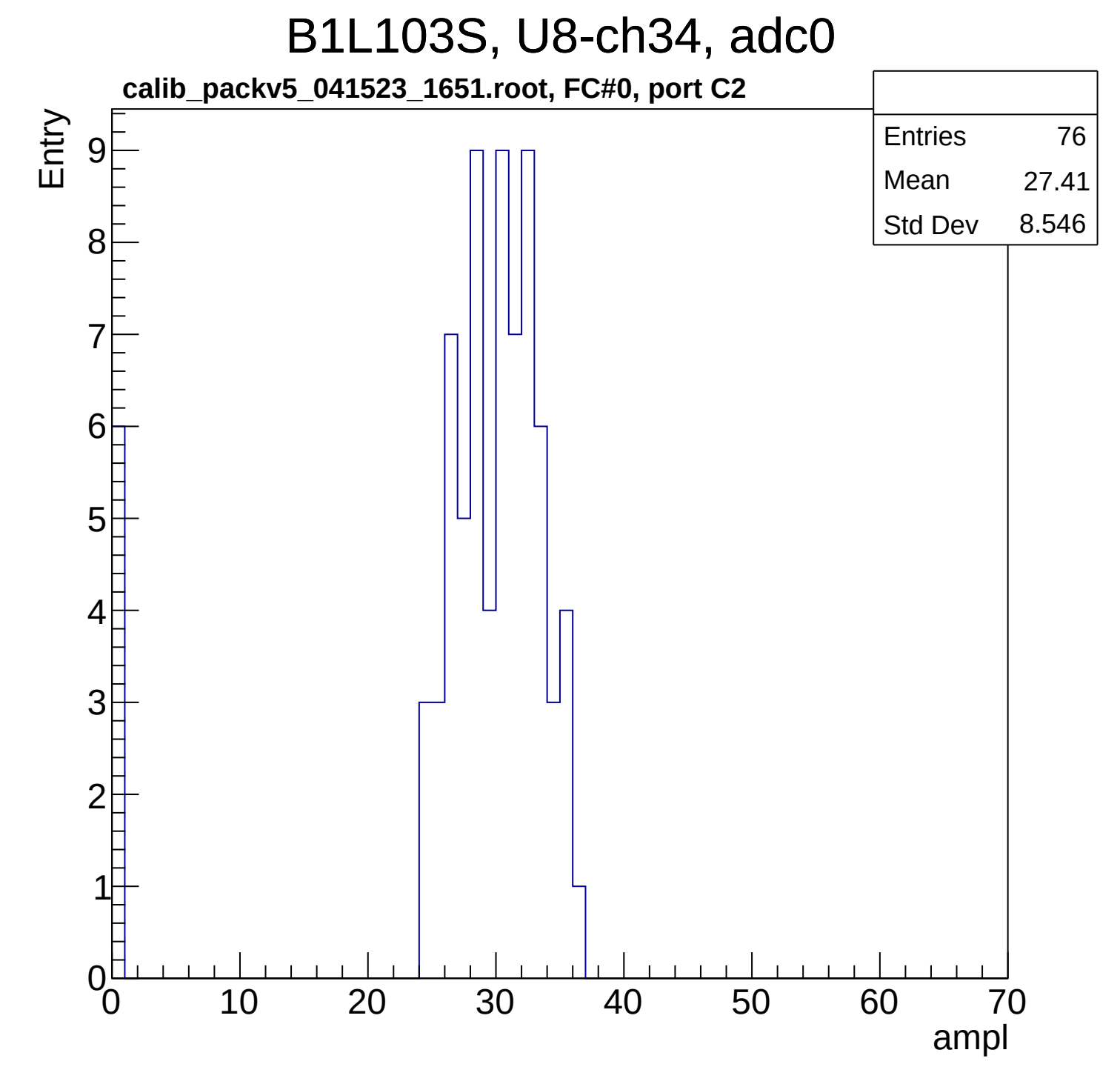
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch34, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 27.41
Std Dev 8.546
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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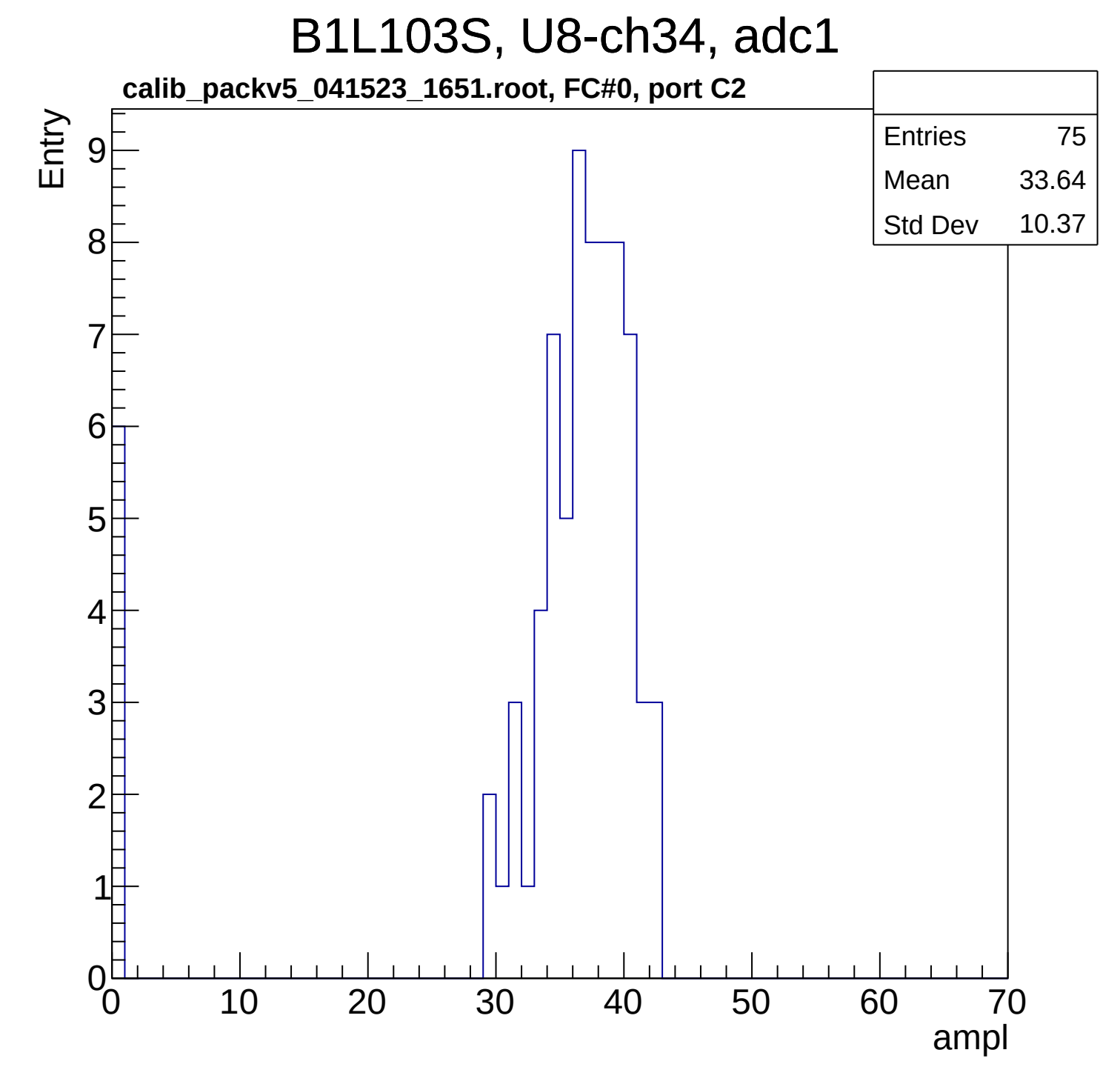
40
50
60
70


B1L103S, U8-ch34, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 33.64
Std Dev 10.37
Entry
ampl
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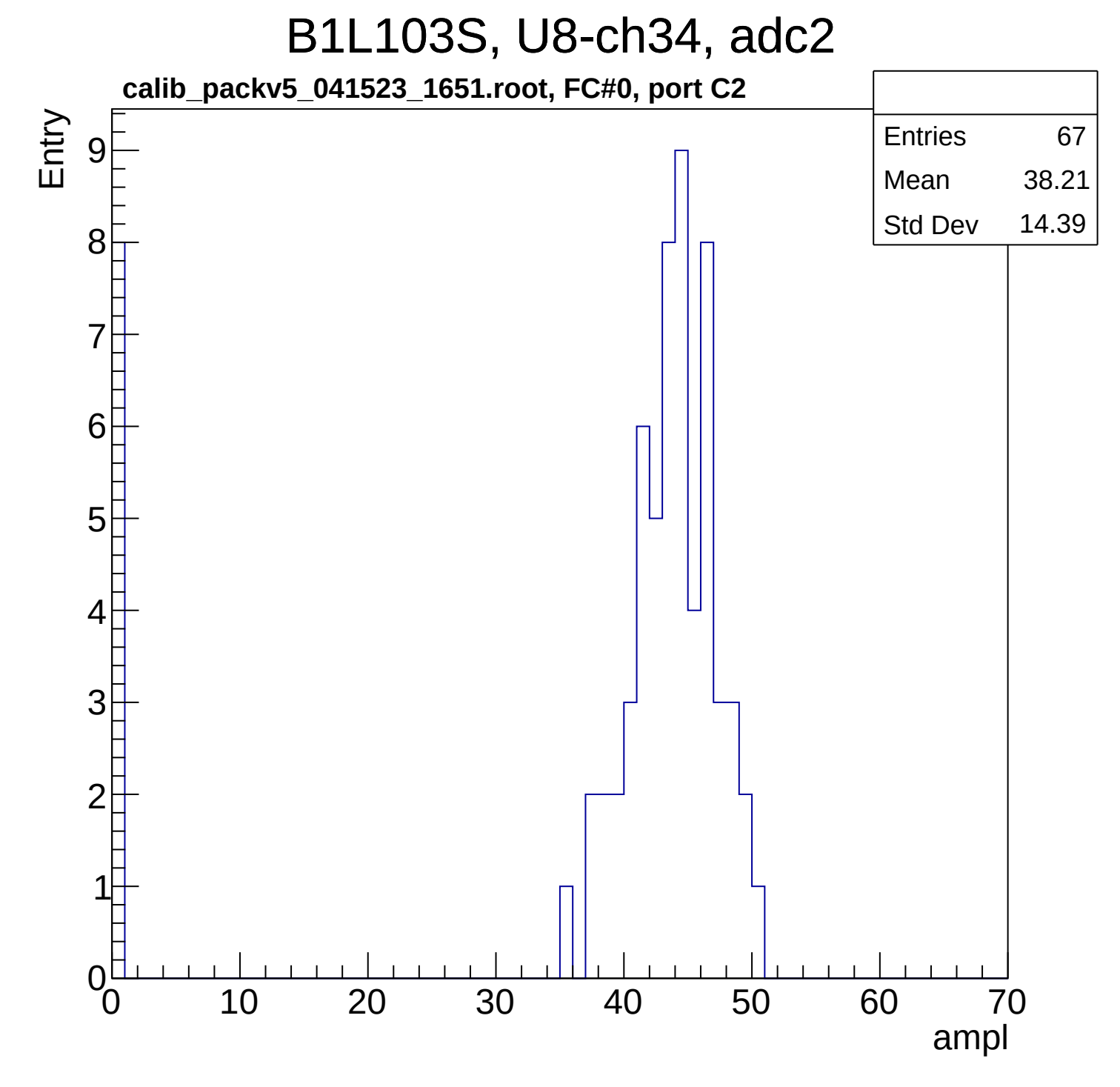
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U8-ch34, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 38.21
Std Dev 14.39
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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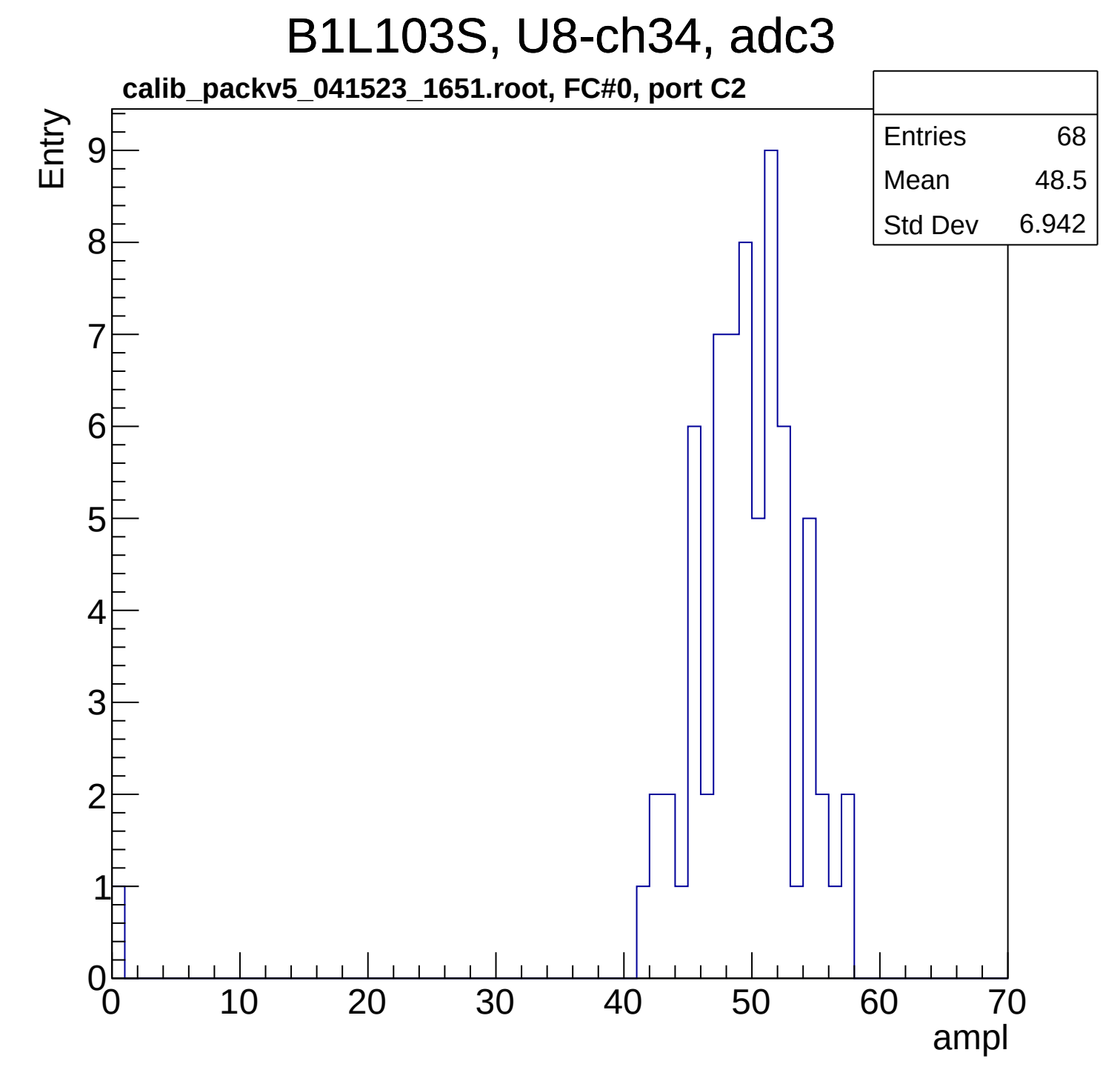
B1L103S, U8-ch34, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 48.5
Std Dev 6.942
Entry
ampl
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2
3
4
5
6
7
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0
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60
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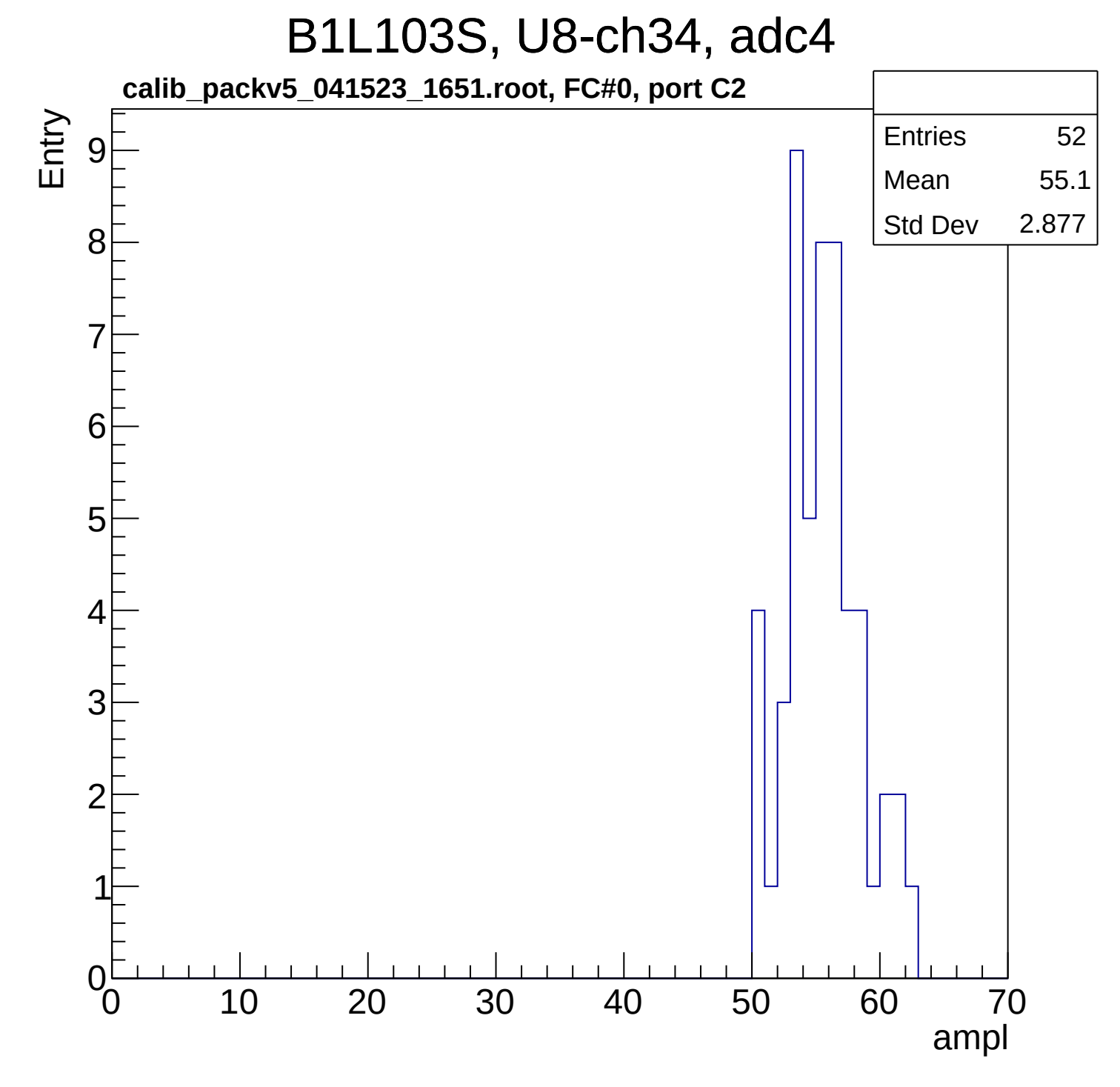
B1L103S, U8-ch34, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 55.1
Std Dev 2.877
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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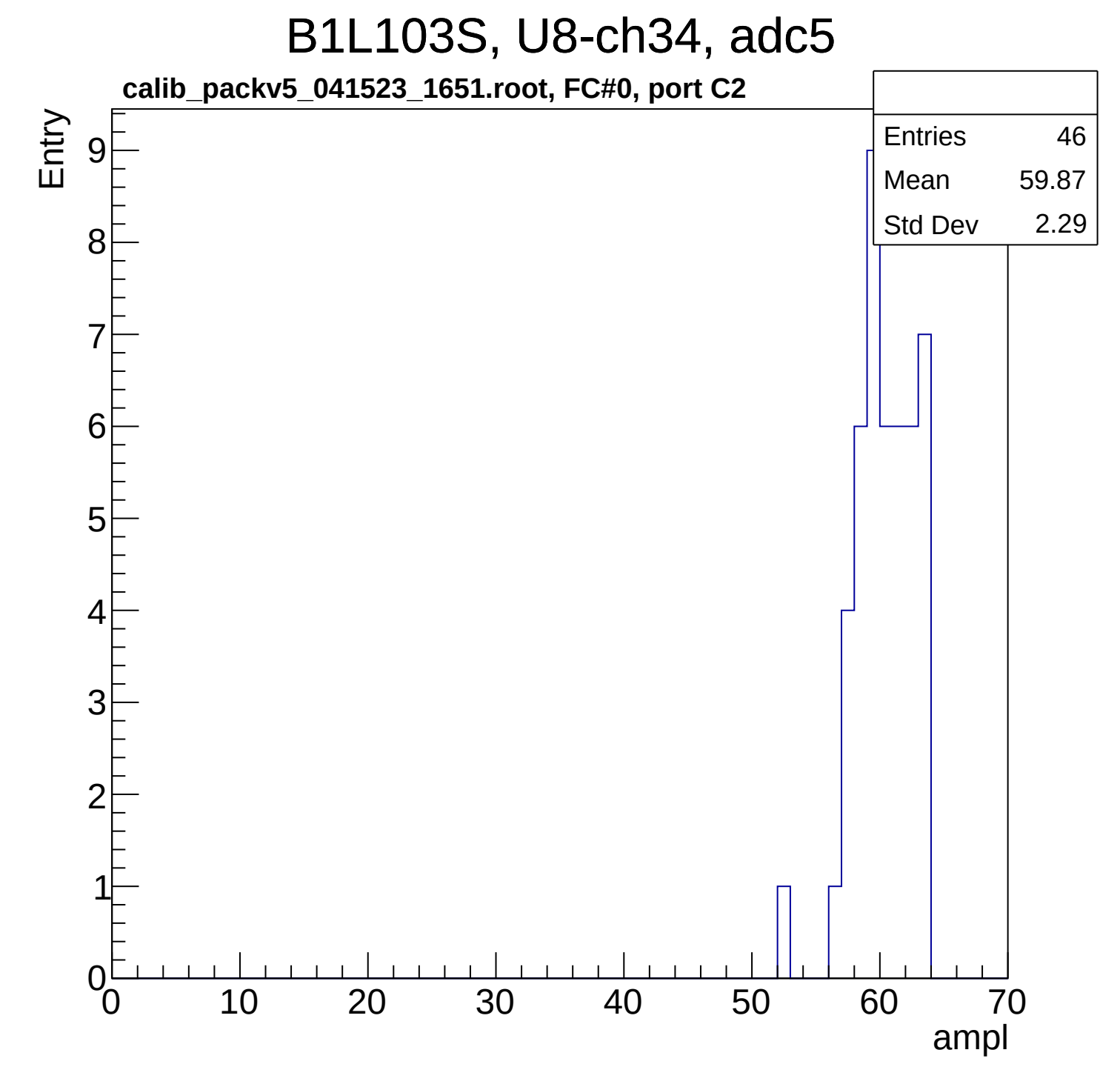
B1L103S, U8-ch34, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 59.87
Std Dev 2.29
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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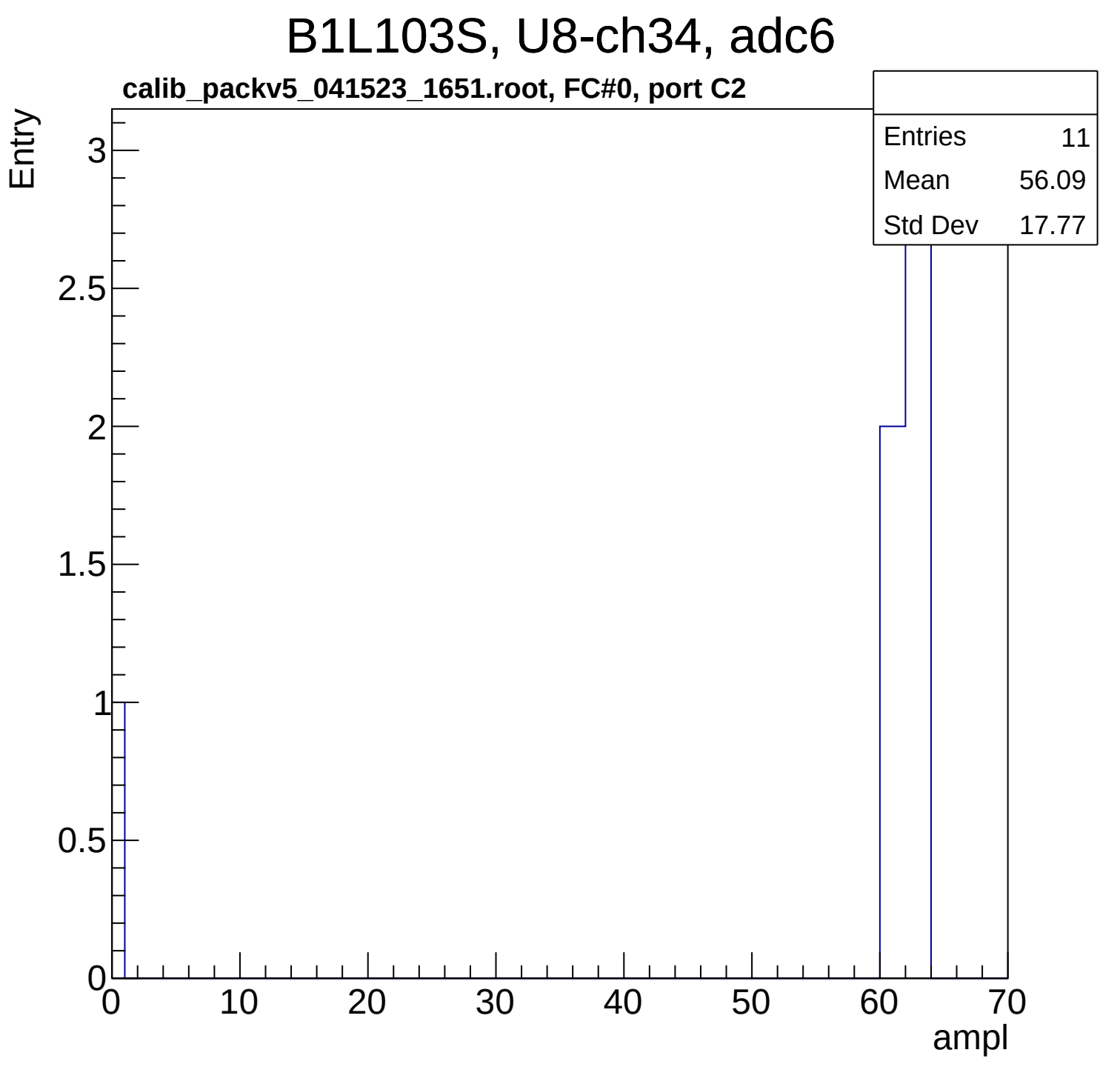
B1L103S, U8-ch34, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 56.09
Std Dev 17.77
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
30
40
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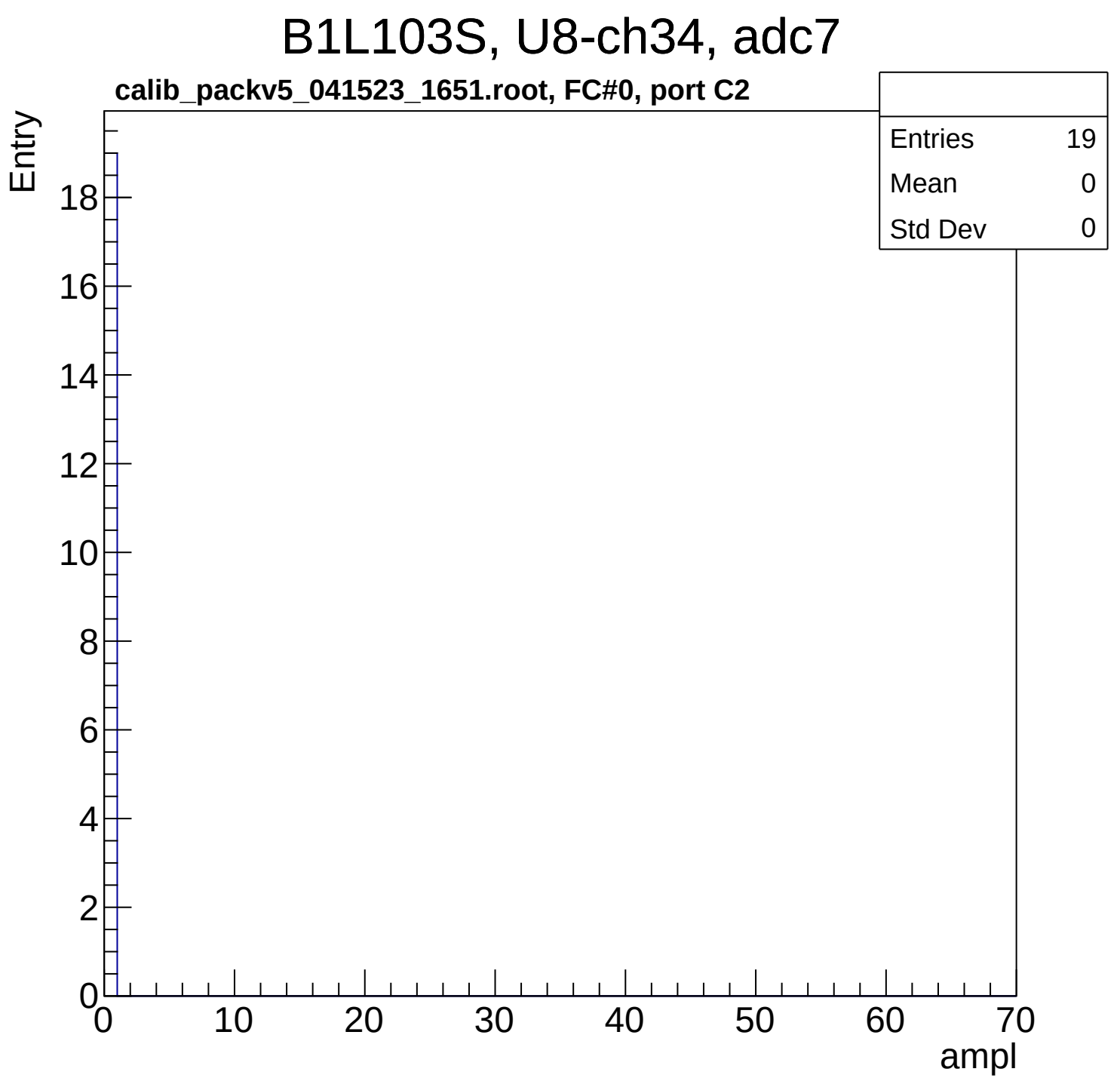
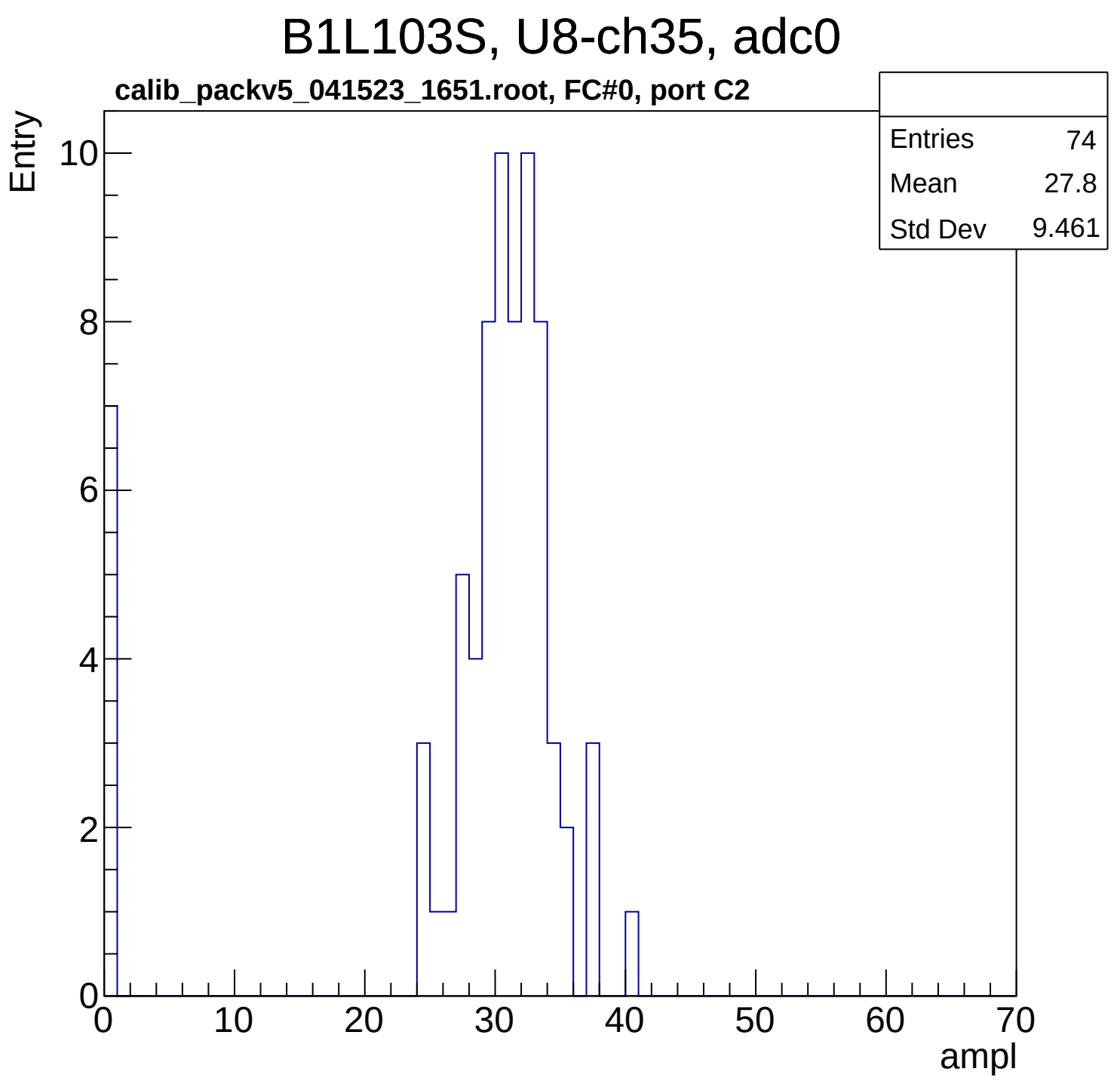
60
70


B1L103S, U8-ch34, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch35, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 27.8
Std Dev 9.461
Entry
ampl
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6
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0
10
20
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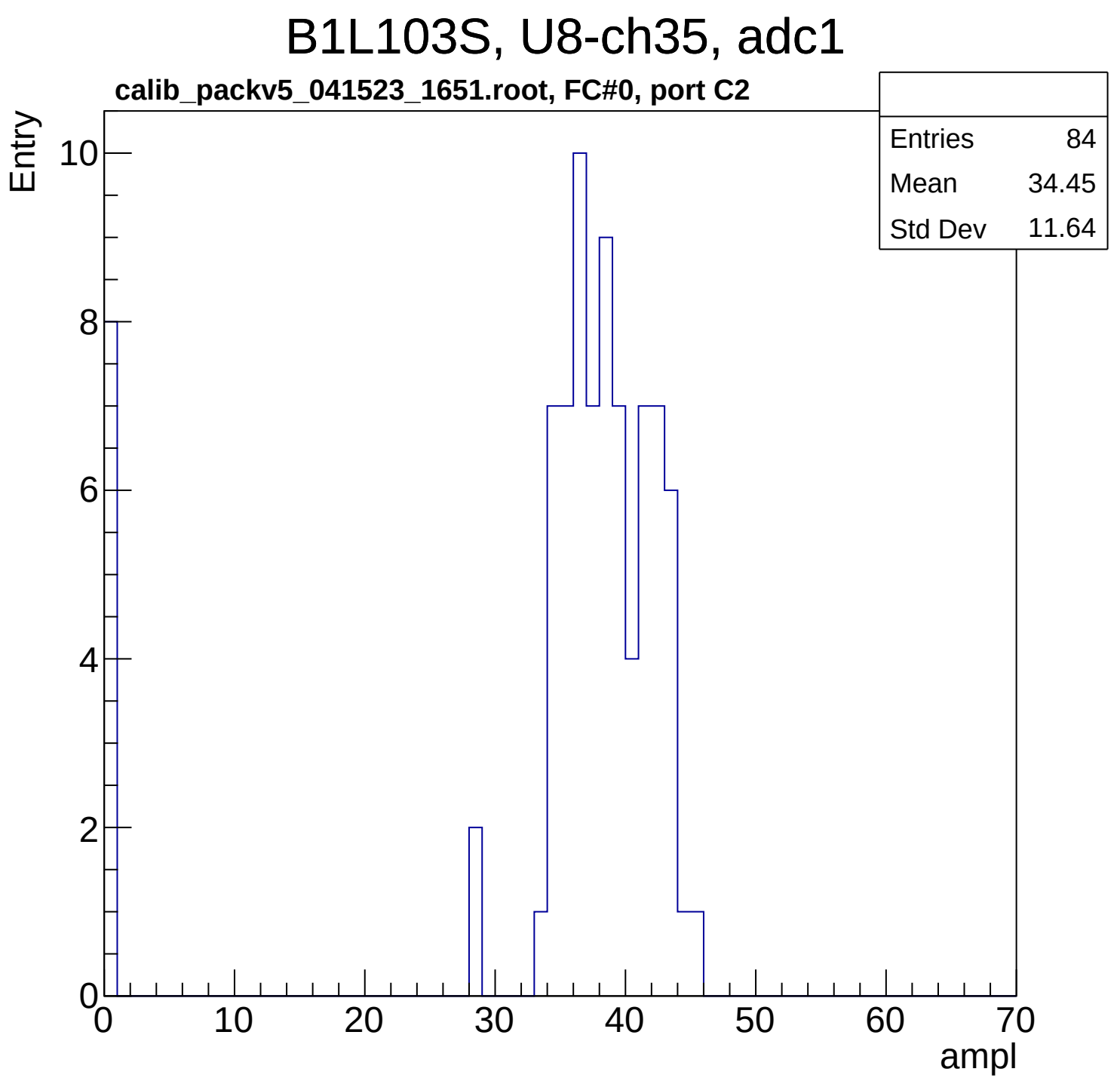
40
50
60
70


B1L103S, U8-ch35, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 34.45
Std Dev 11.64
Entry
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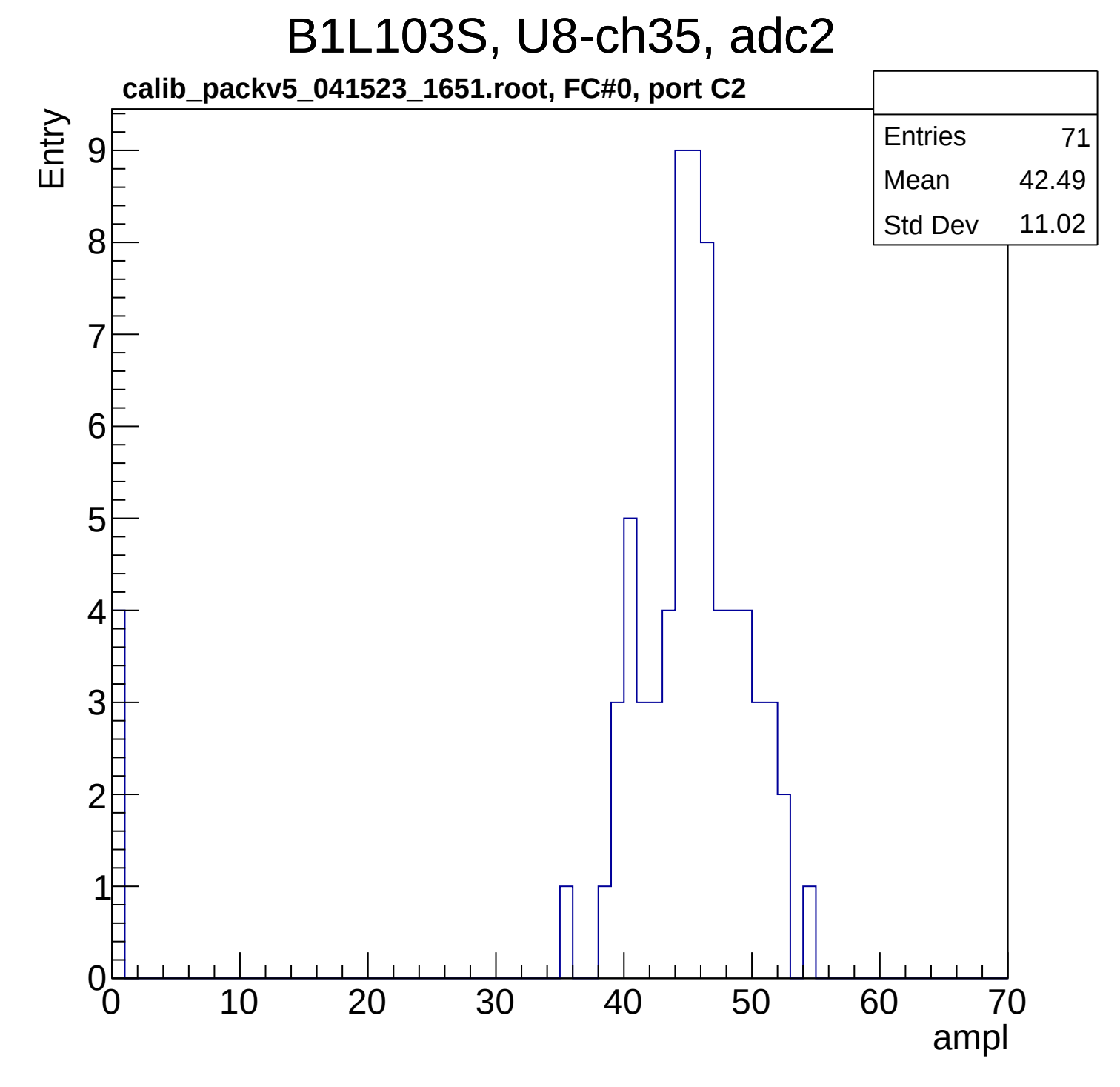
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch35, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 42.49
Std Dev 11.02
Entry
ampl
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3
4
5
6
7
8
9
0
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20
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40
50
60
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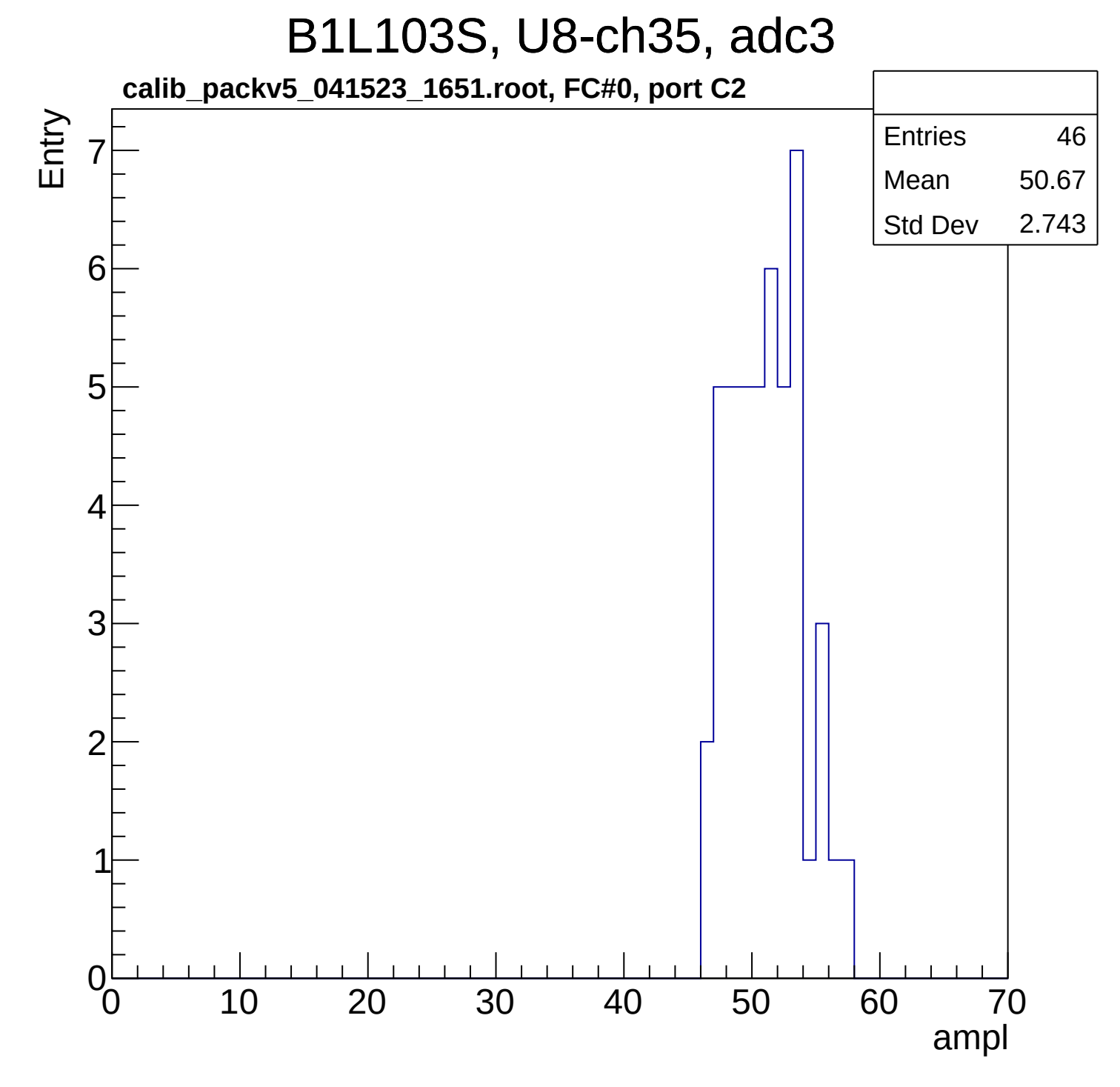
B1L103S, U8-ch35, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 50.67
Std Dev 2.743
Entry
ampl
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6
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0
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60
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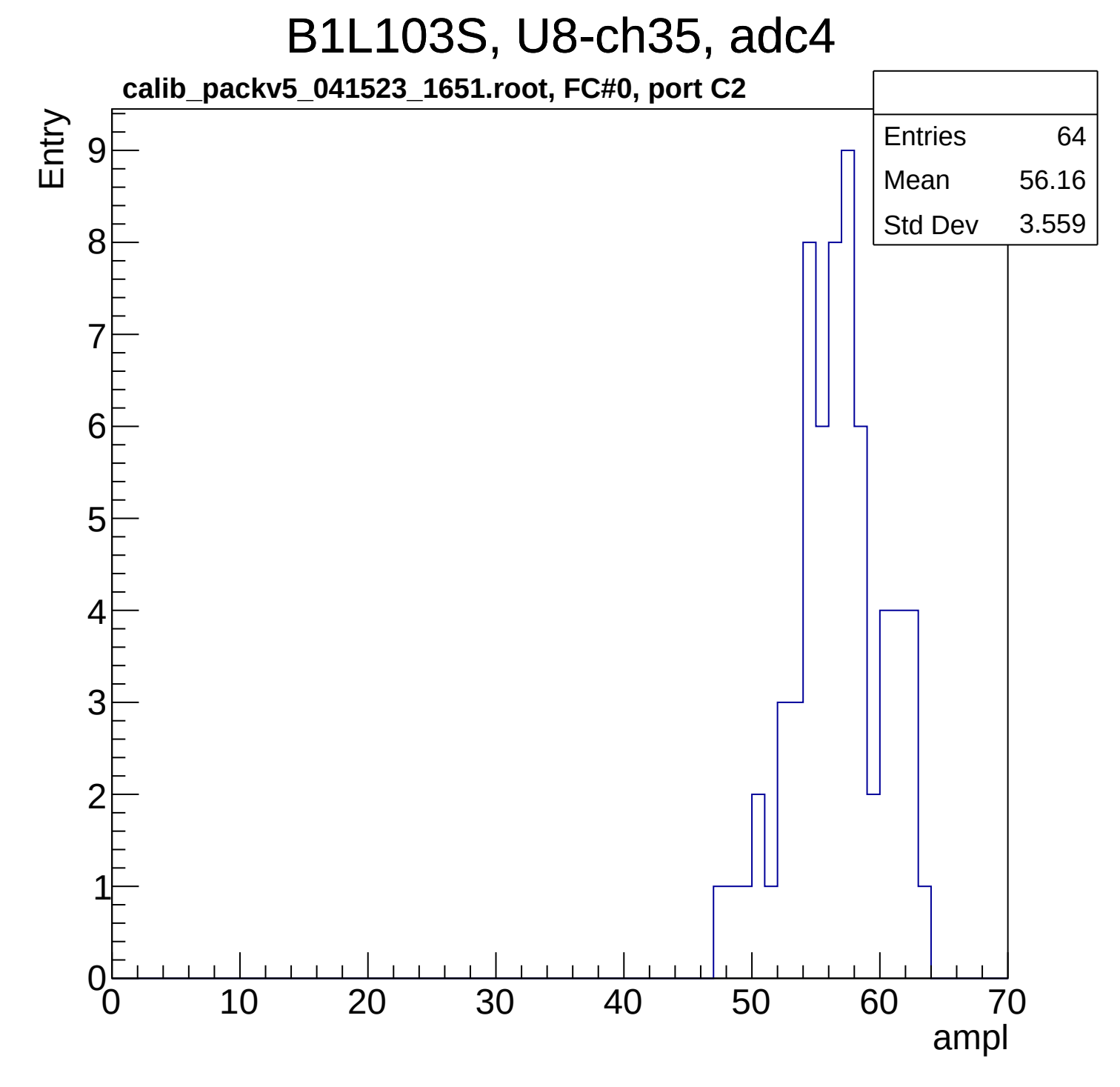
B1L103S, U8-ch35, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 56.16
Std Dev 3.559
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
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60
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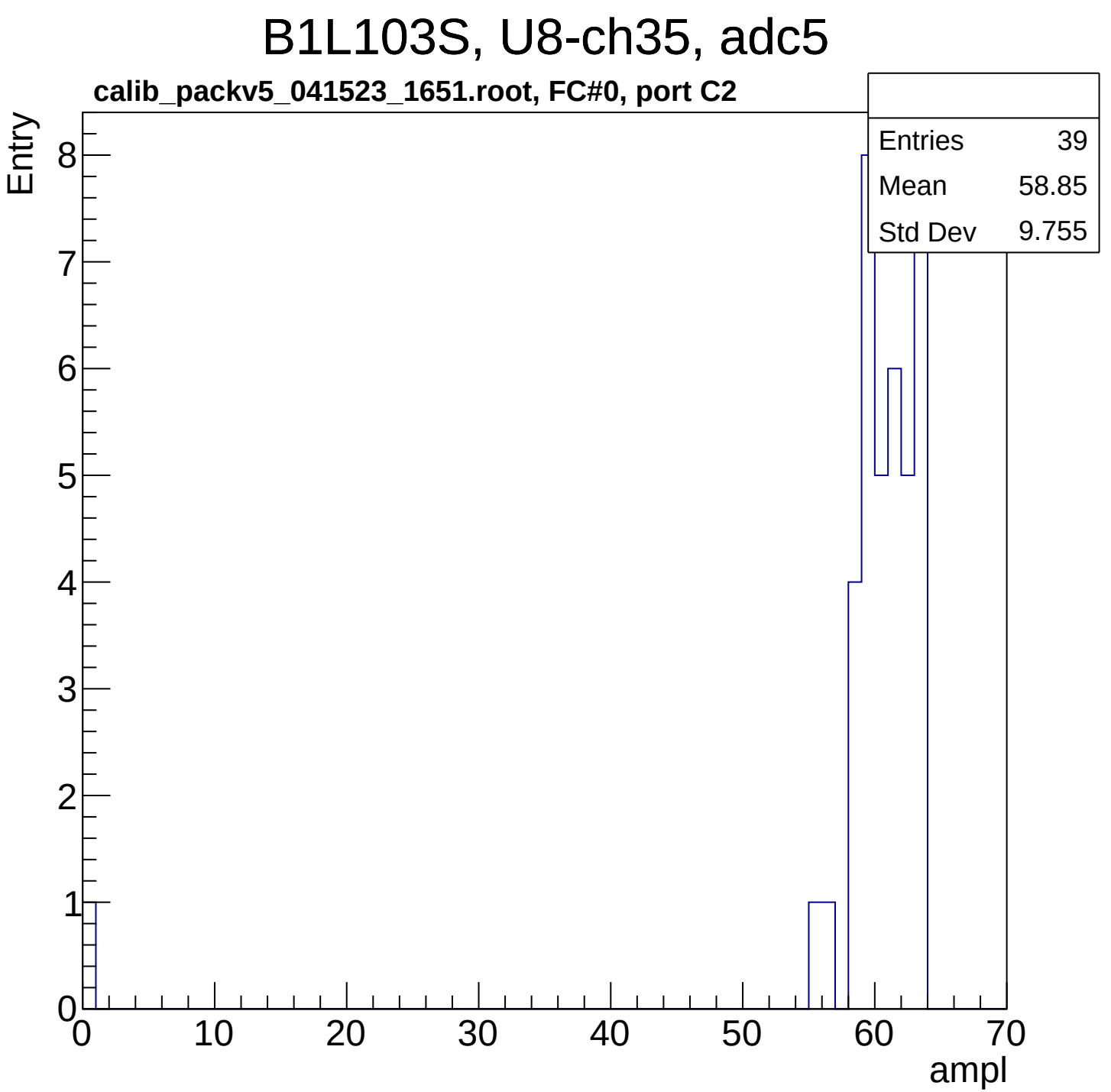
B1L103S, U8-ch35, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 58.85
Std Dev 9.755
Entry
ampl
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3
4
5
6
7
8
0
10
20
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40
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60
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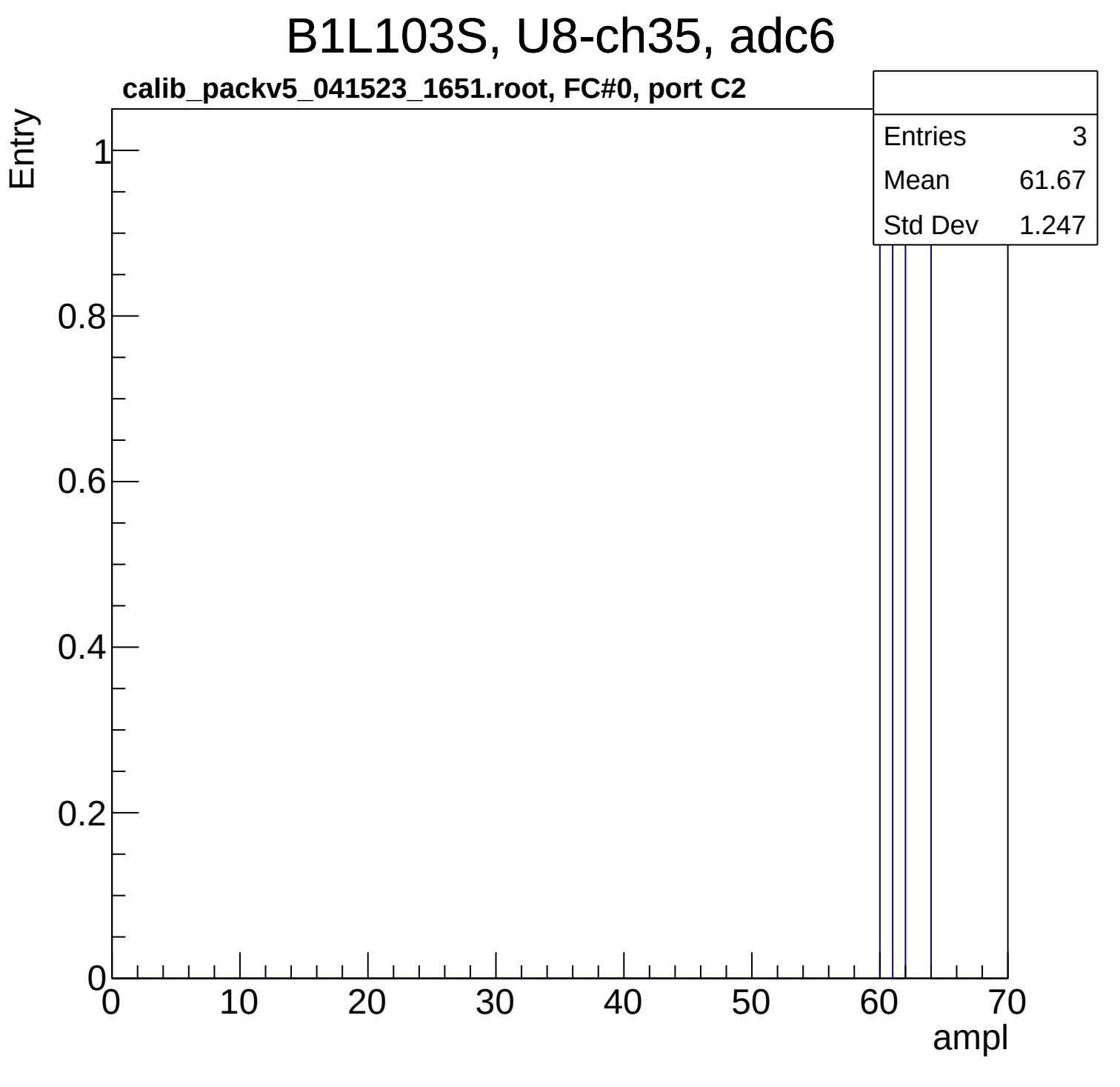
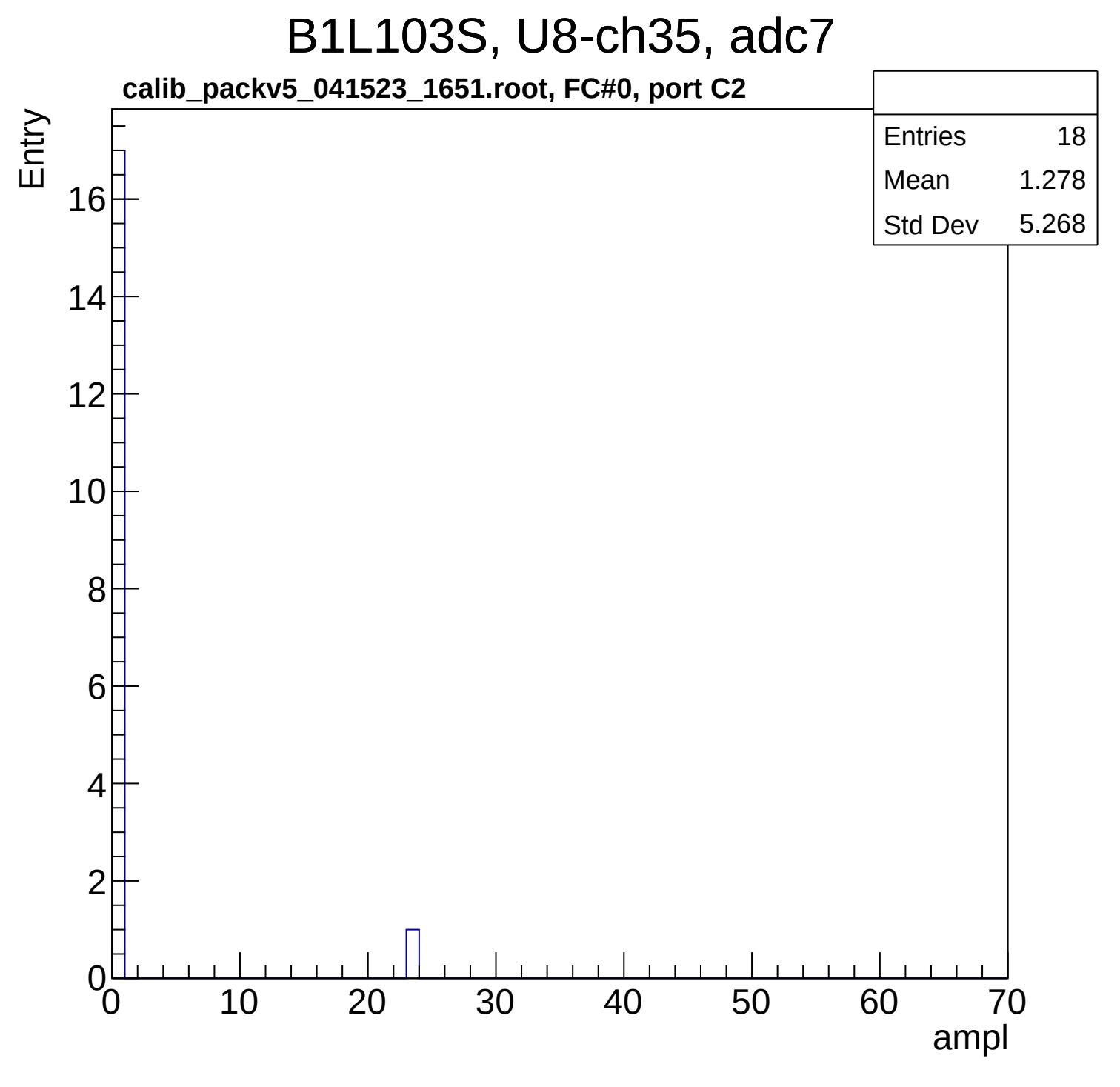
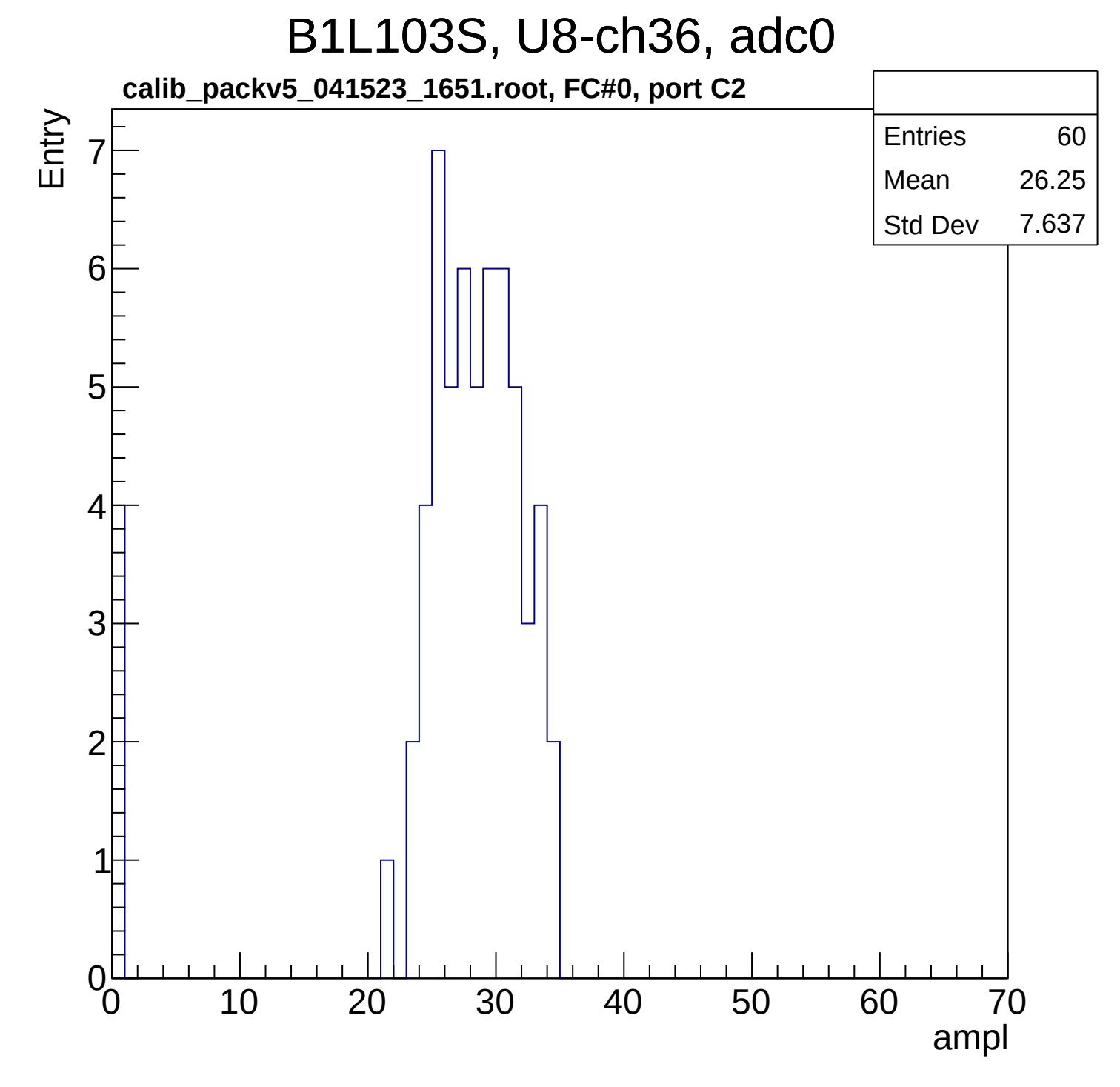
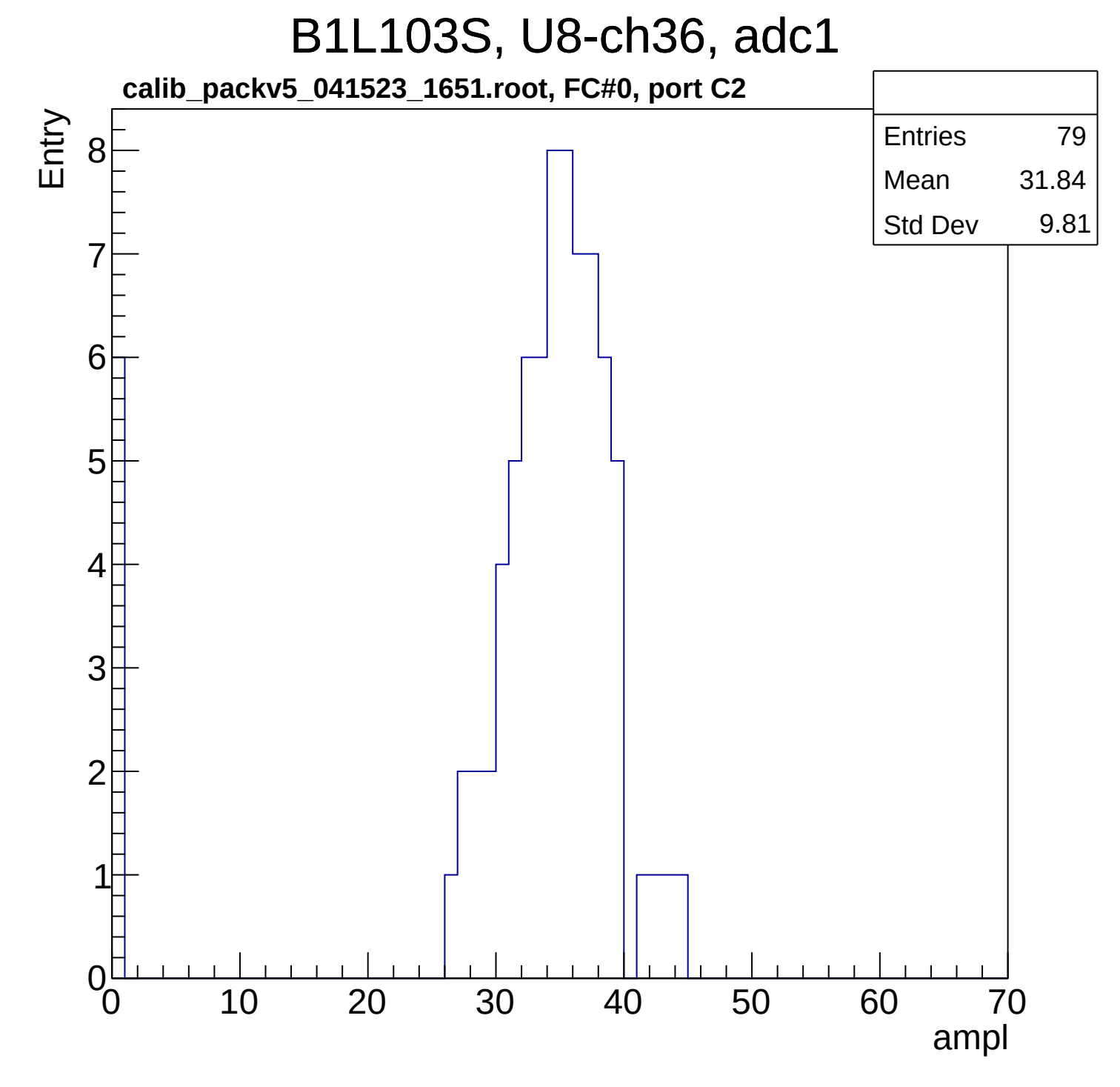

B1L103S, U8-ch35, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 61.67
Std Dev 1.247
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B1L103S, U8-ch35, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.278
Std Dev 5.268
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch36, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 26.25
Std Dev 7.637
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U8-ch36, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 31.84
Std Dev 9.81
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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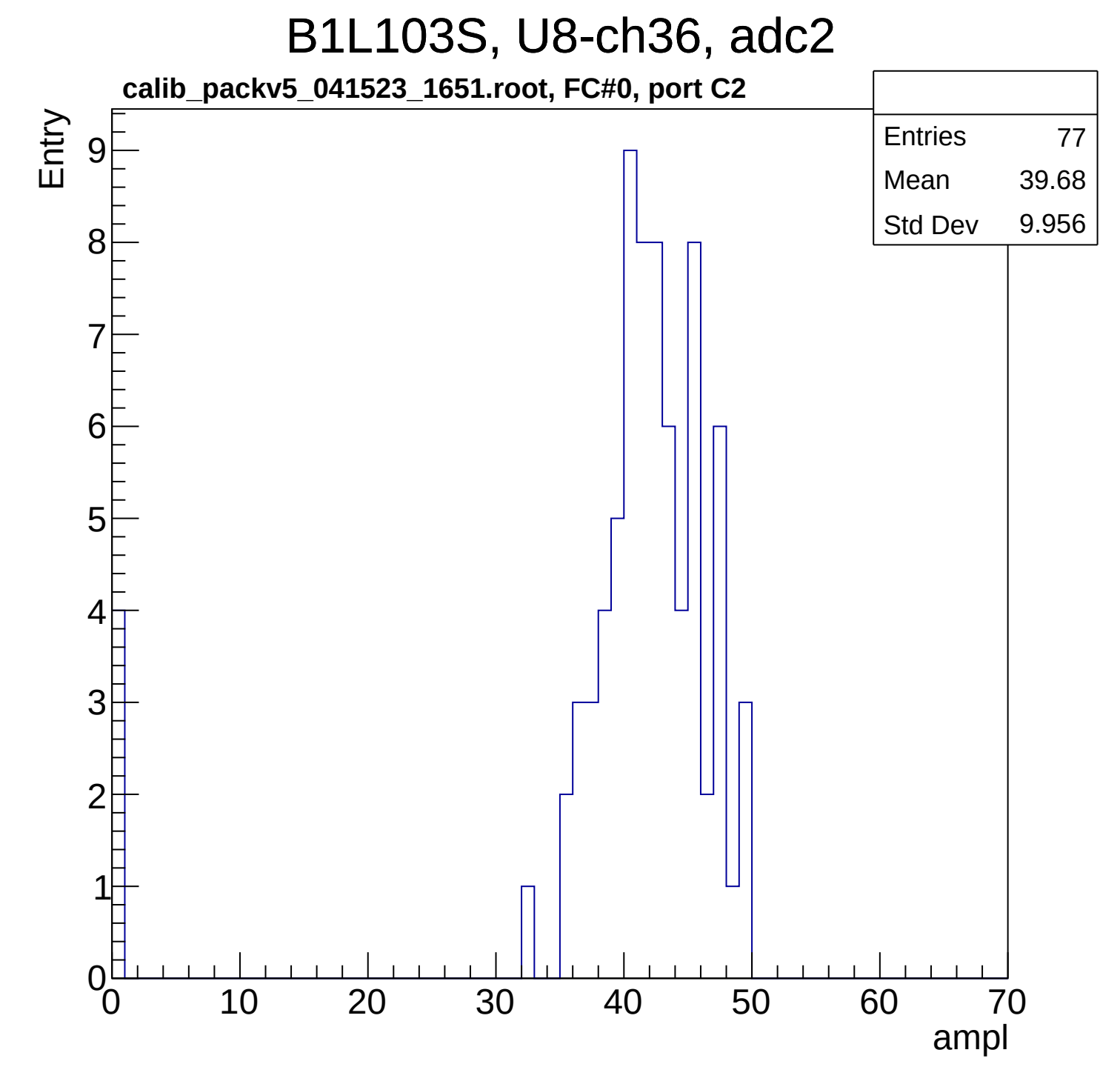
B1L103S, U8-ch36, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 39.68
Std Dev 9.956
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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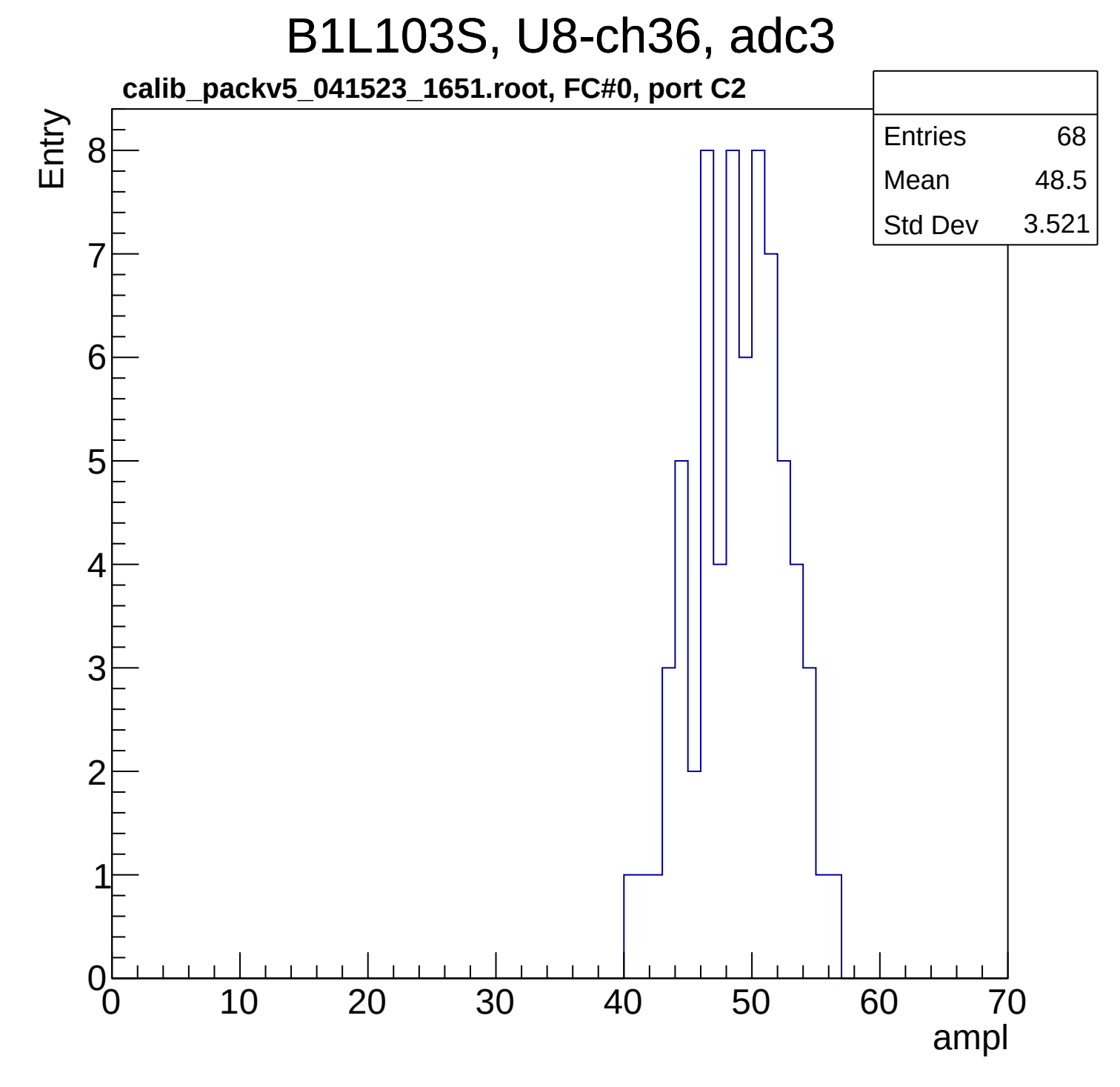
B1L103S, U8-ch36, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 48.5
Std Dev 3.521
Entry
ampl
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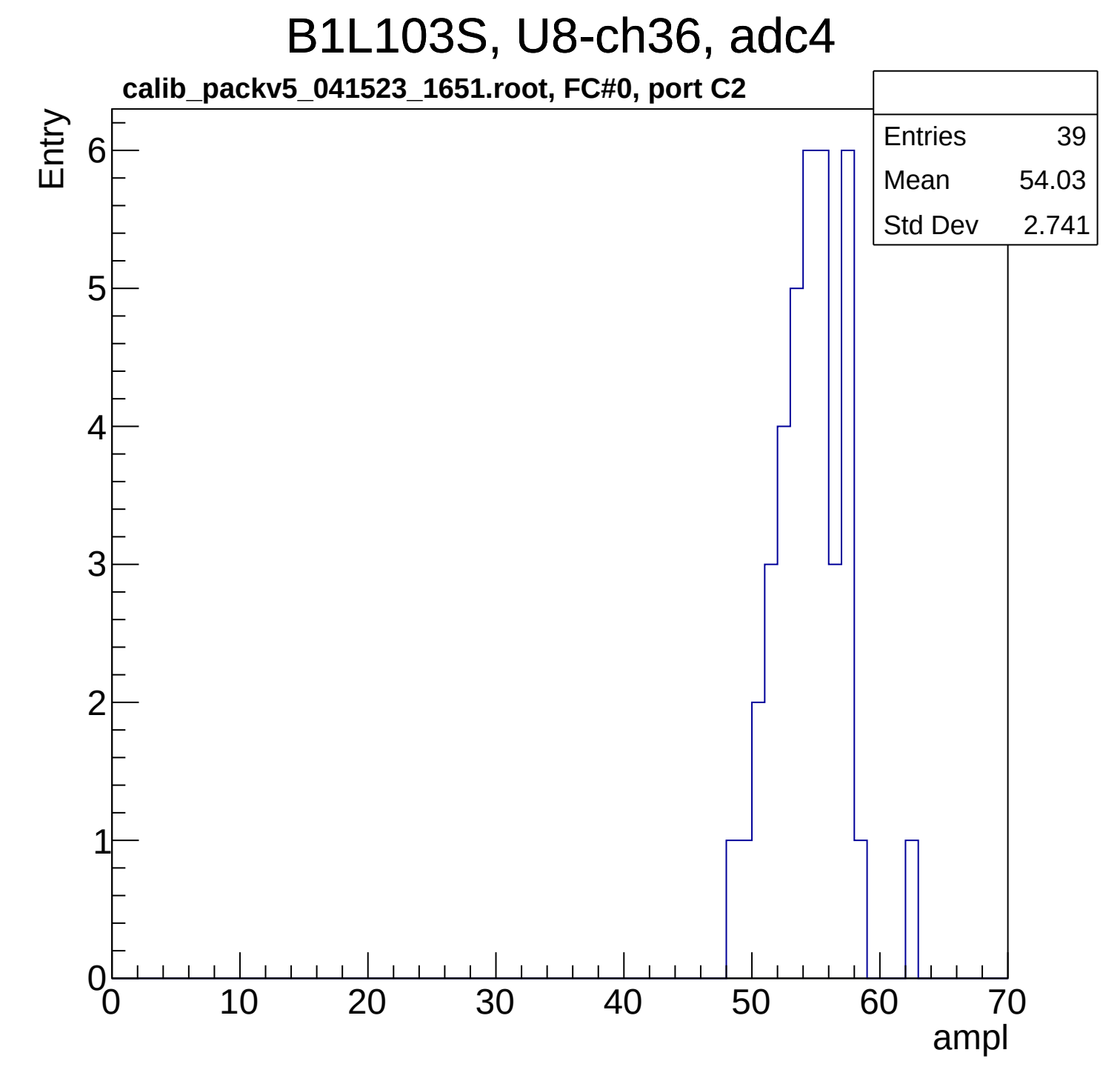
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch36, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 54.03
Std Dev 2.741
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
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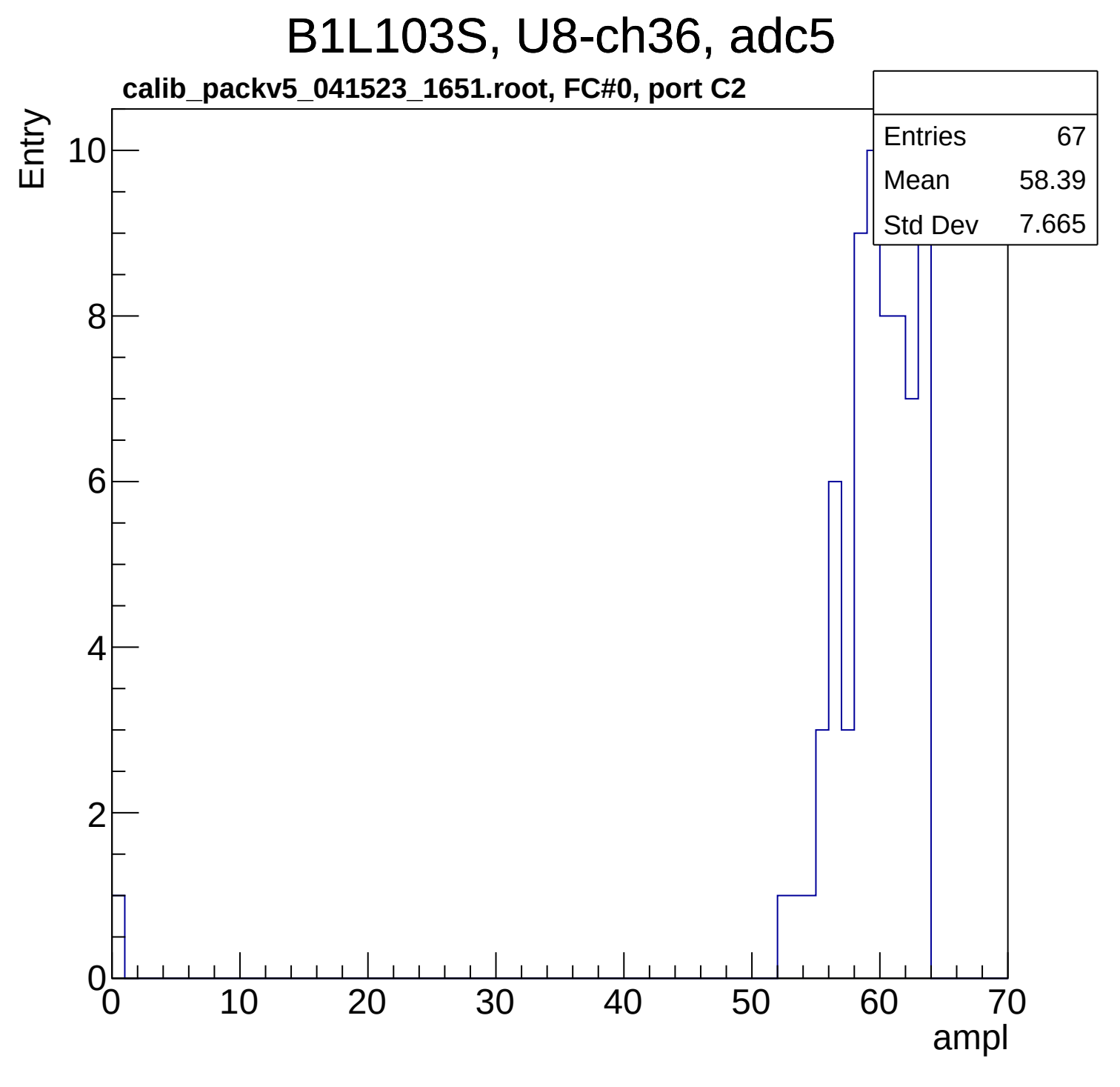
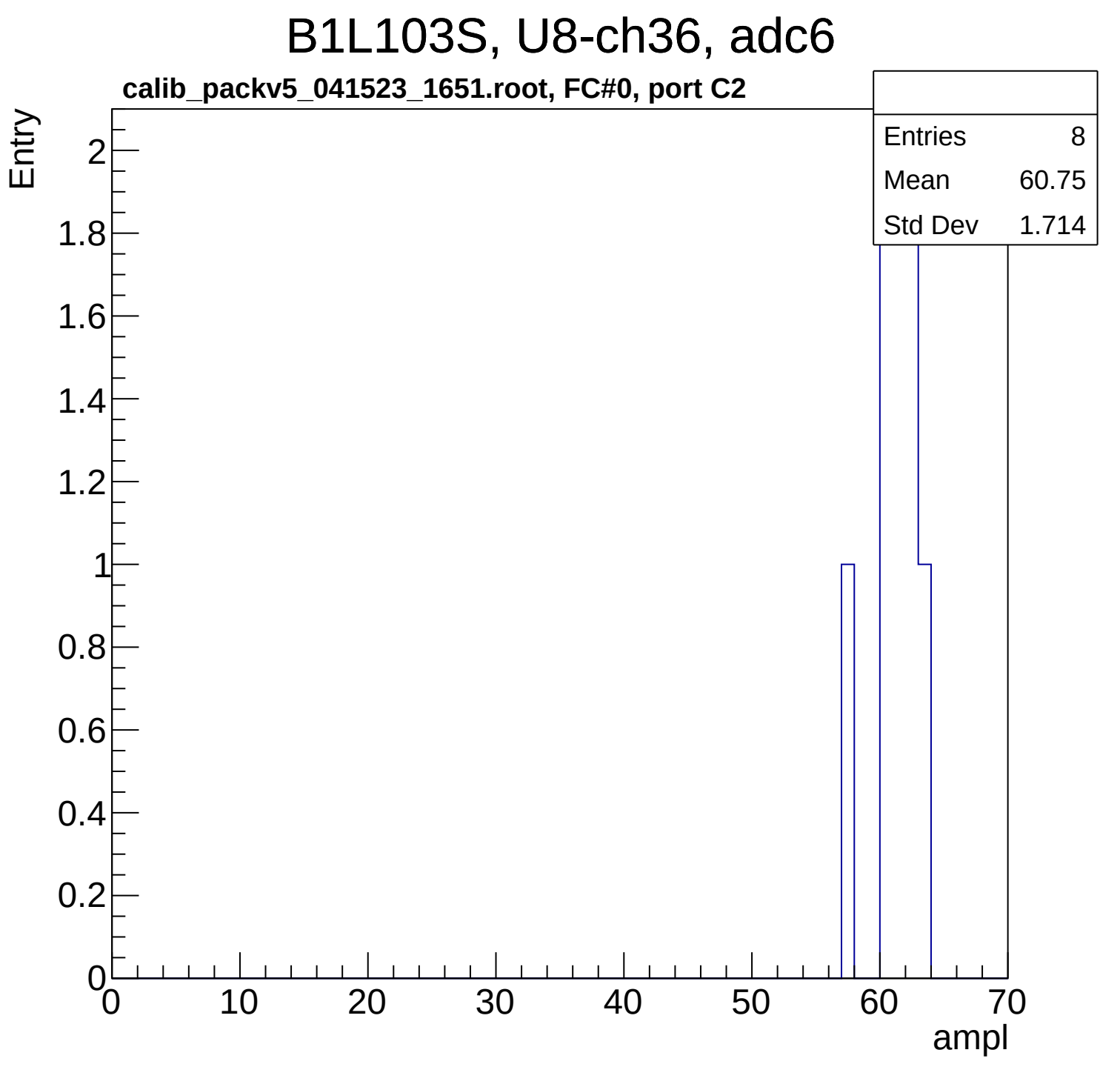

B1L103S, U8-ch36, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 58.39
Std Dev 7.665
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch36, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 60.75
Std Dev 1.714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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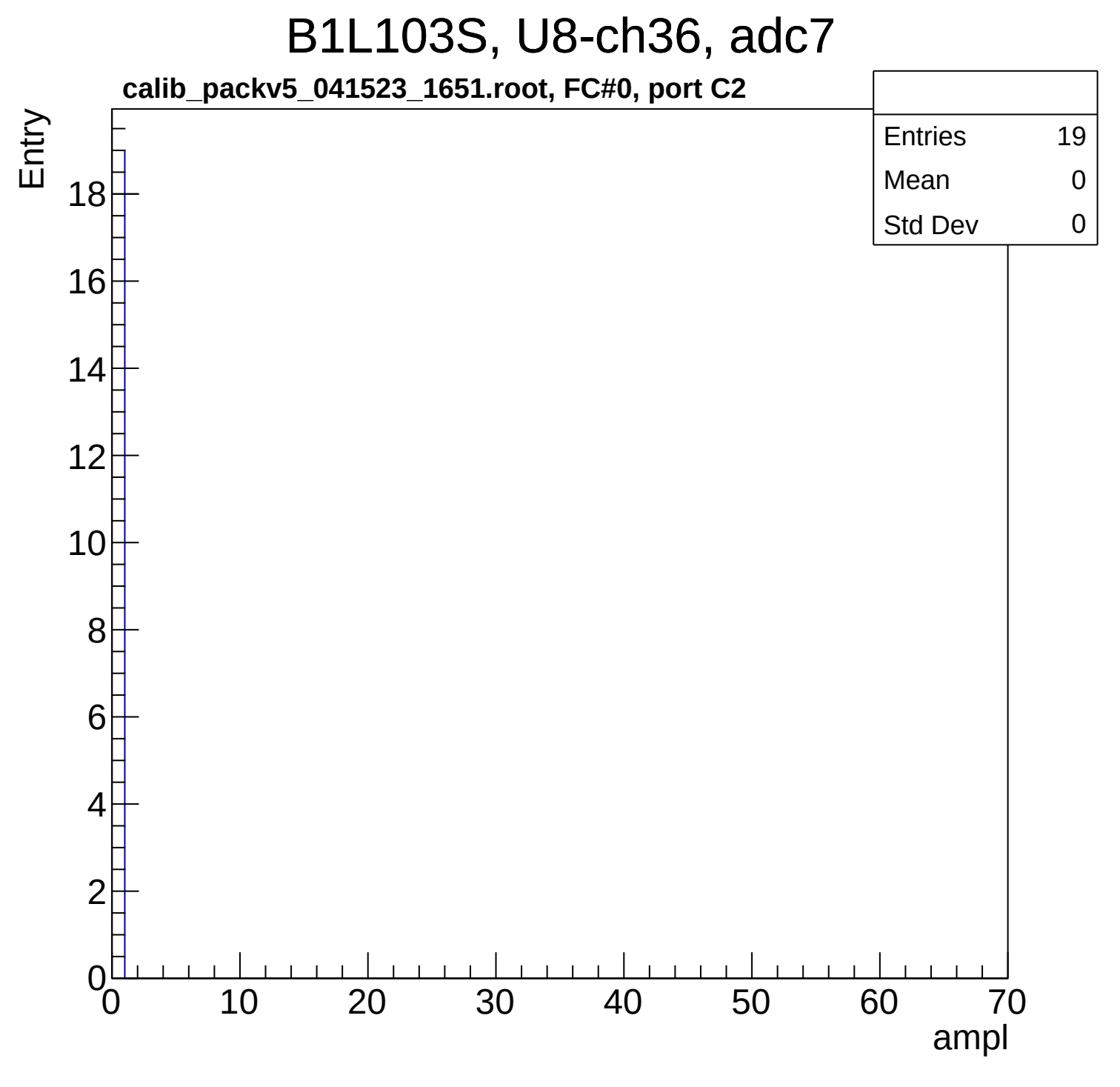
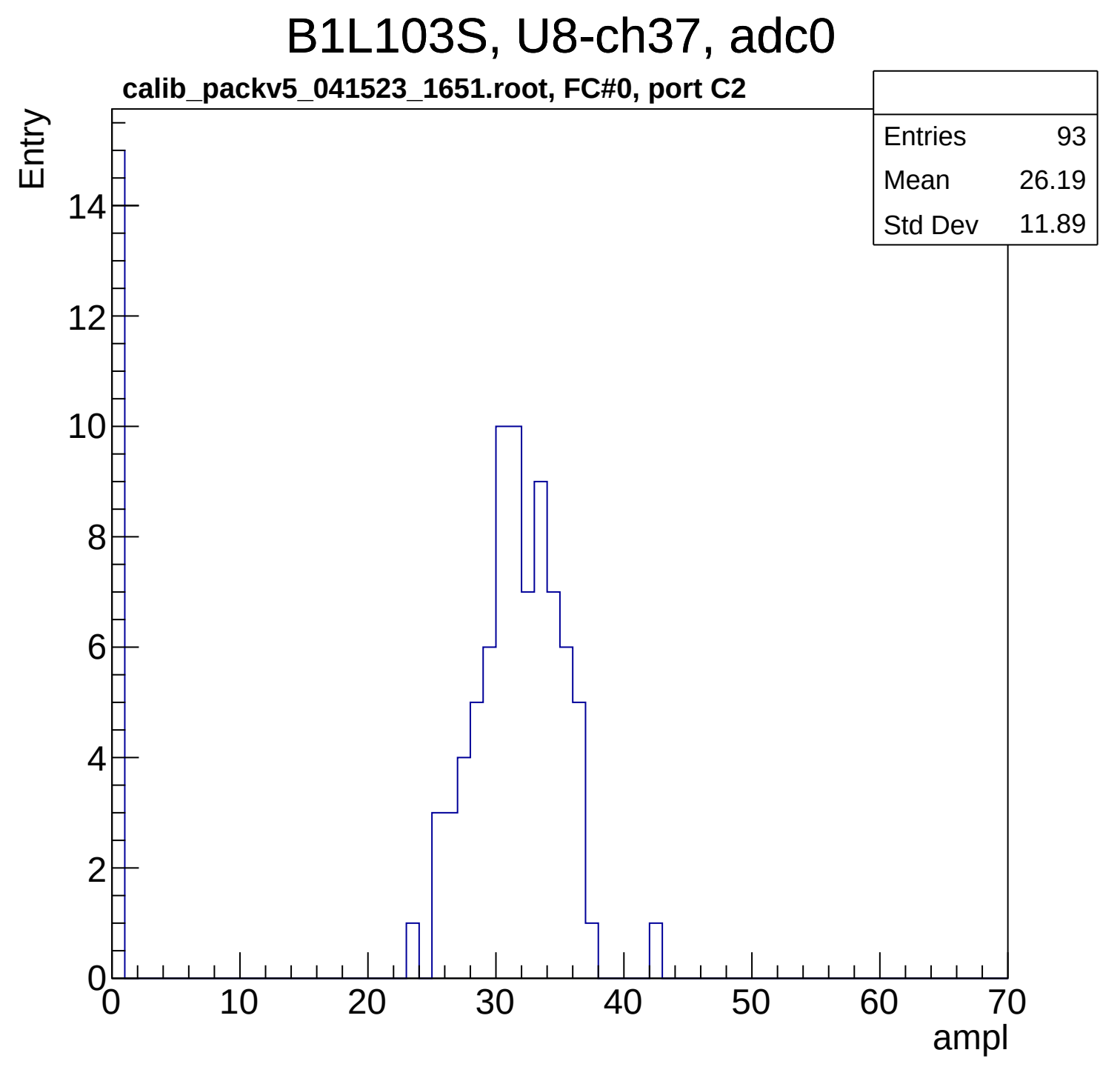
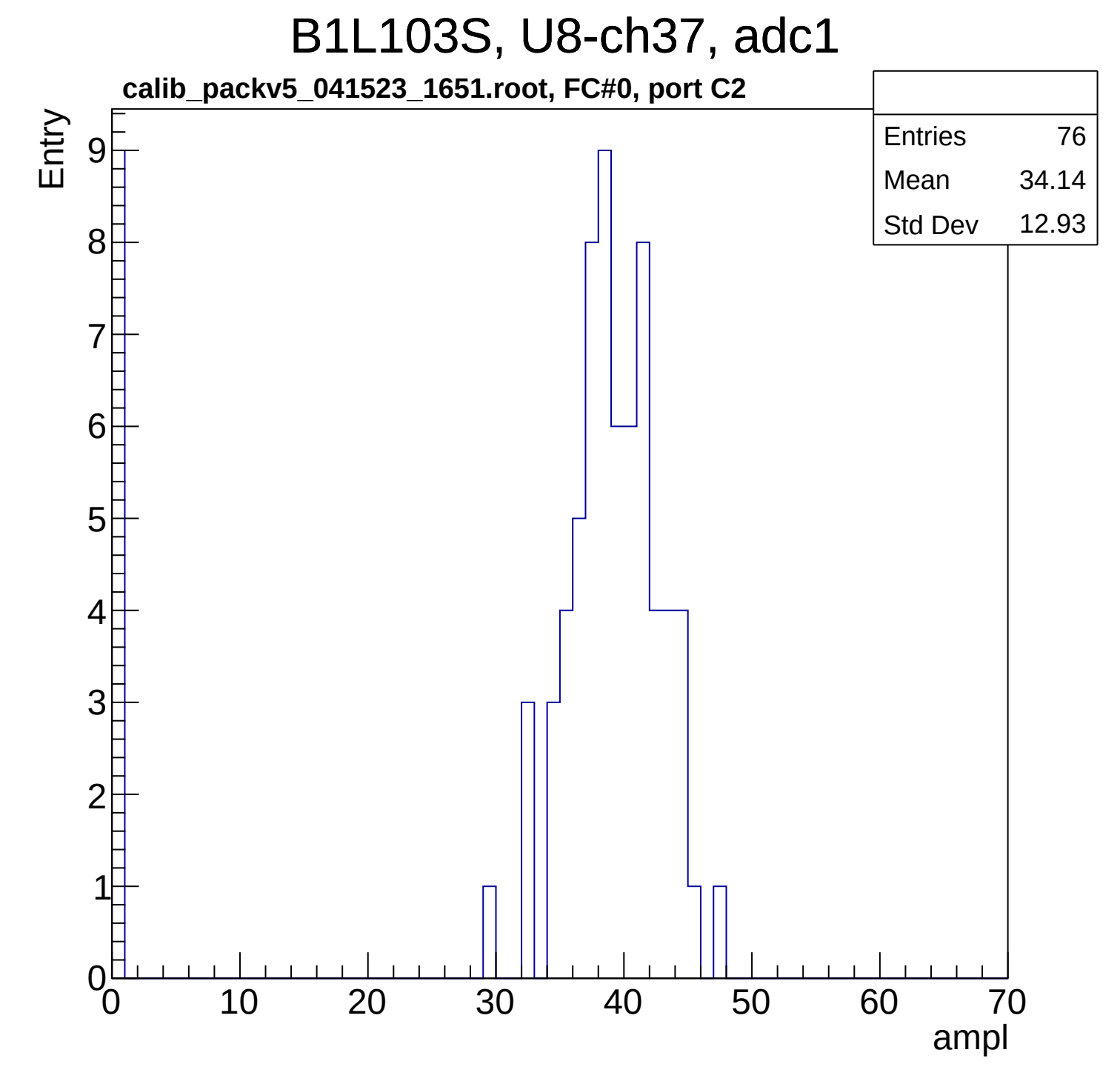

B1L103S, U8-ch36, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch37, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 26.19
Std Dev 11.89
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch37, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 34.14
Std Dev 12.93
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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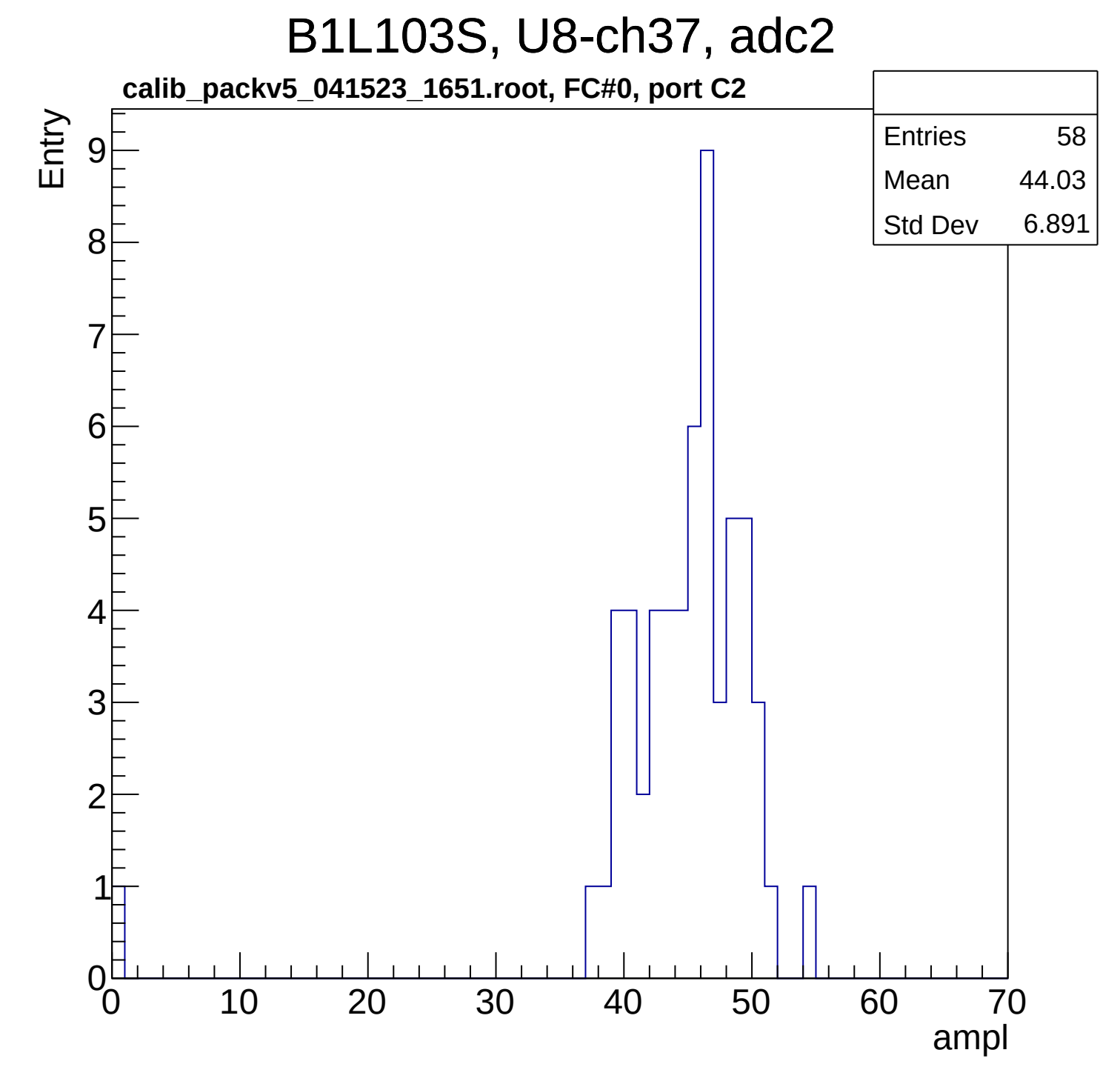
B1L103S, U8-ch37, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 44.03
Std Dev 6.891
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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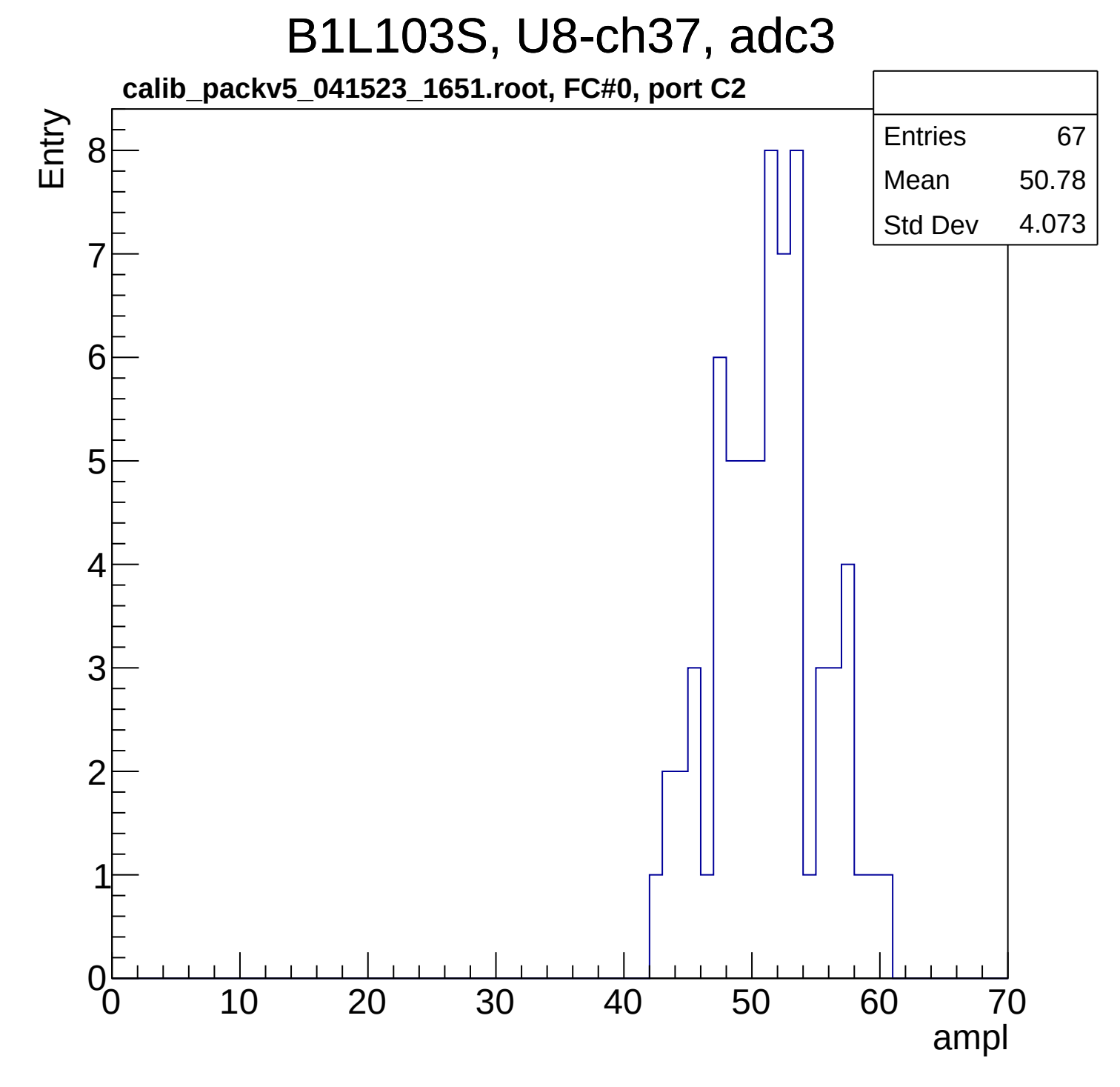
B1L103S, U8-ch37, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 50.78
Std Dev 4.073
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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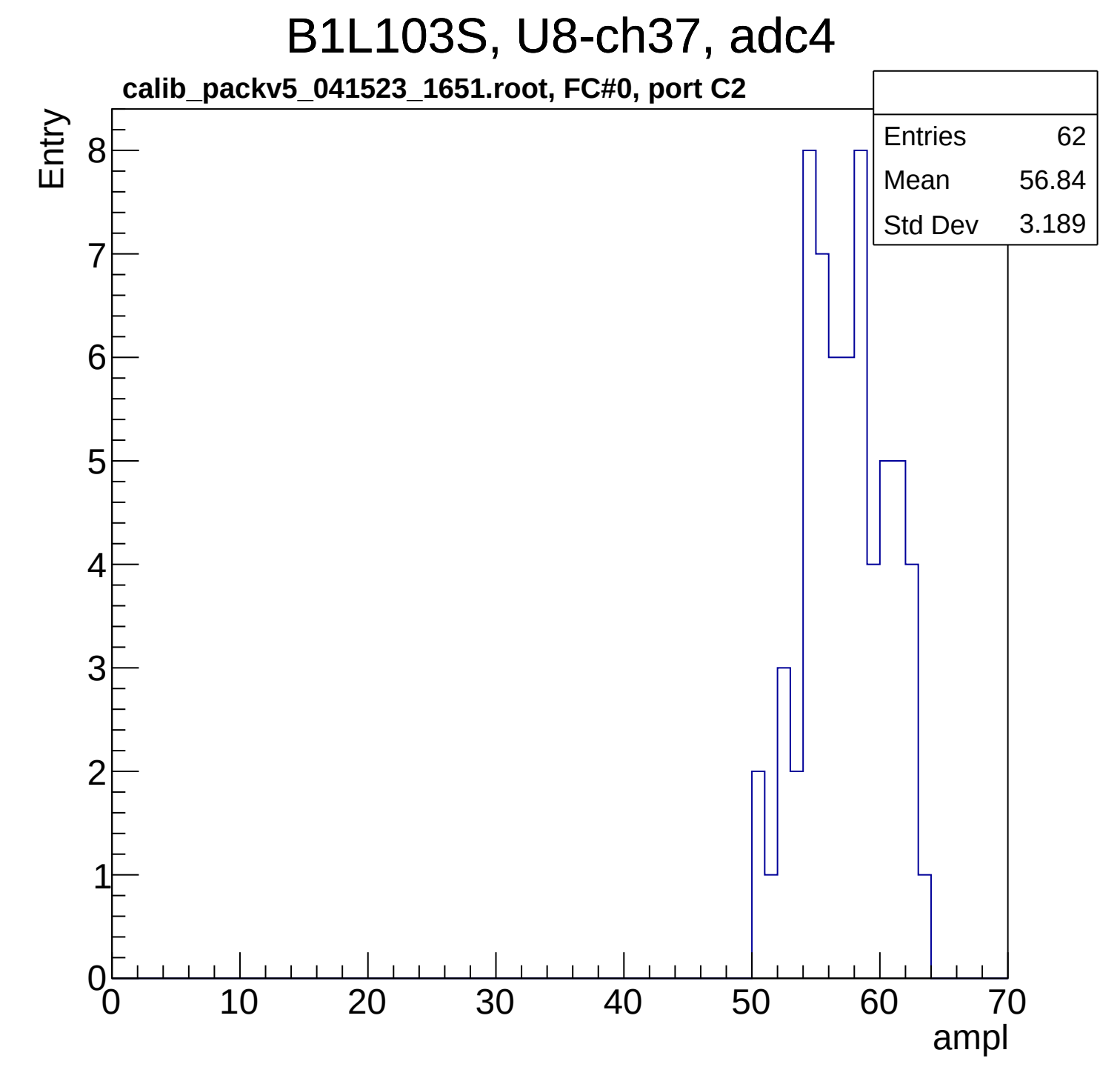
B1L103S, U8-ch37, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 56.84
Std Dev 3.189
Entry
ampl
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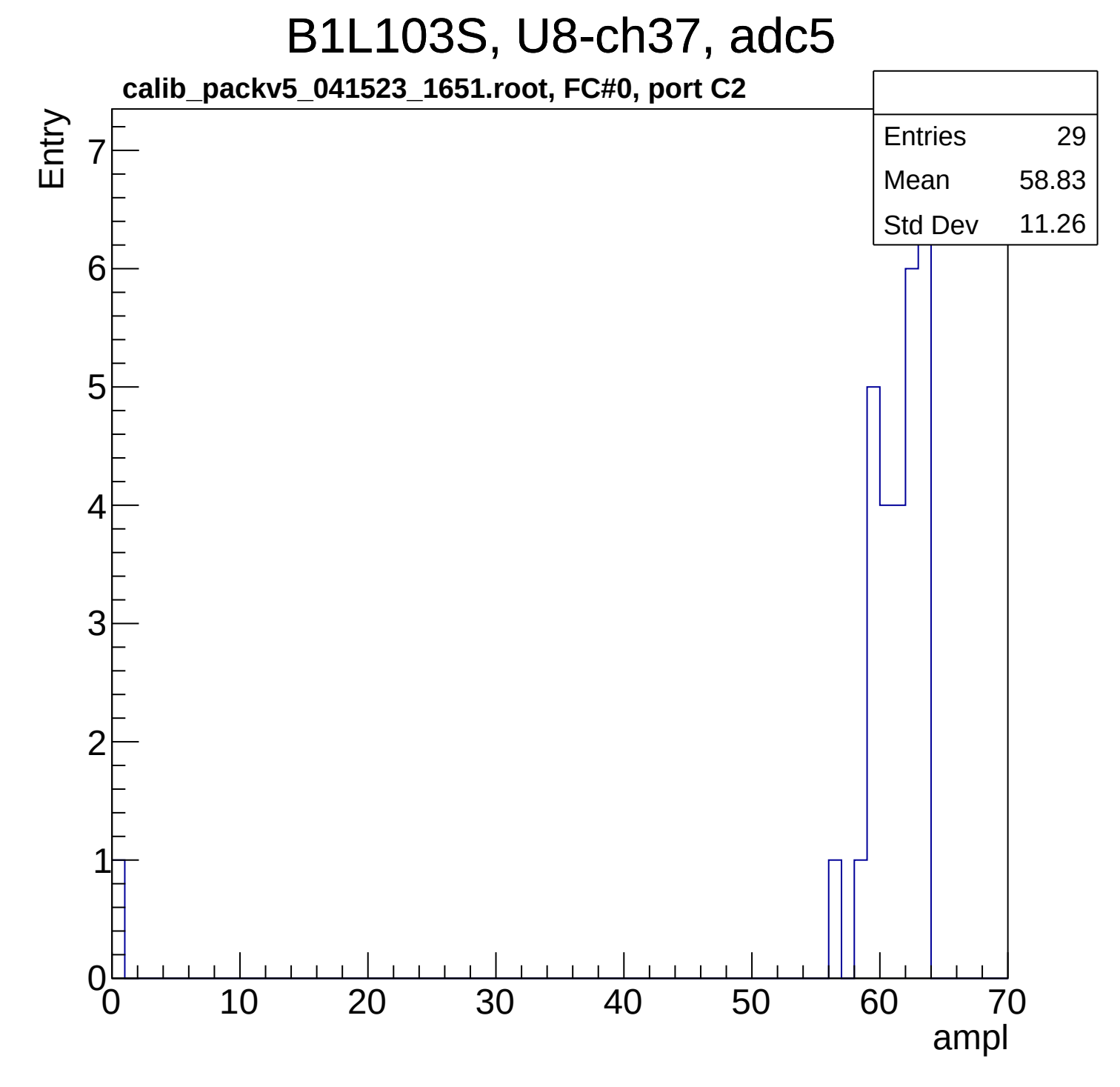
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch37, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 58.83
Std Dev 11.26
Entry
ampl
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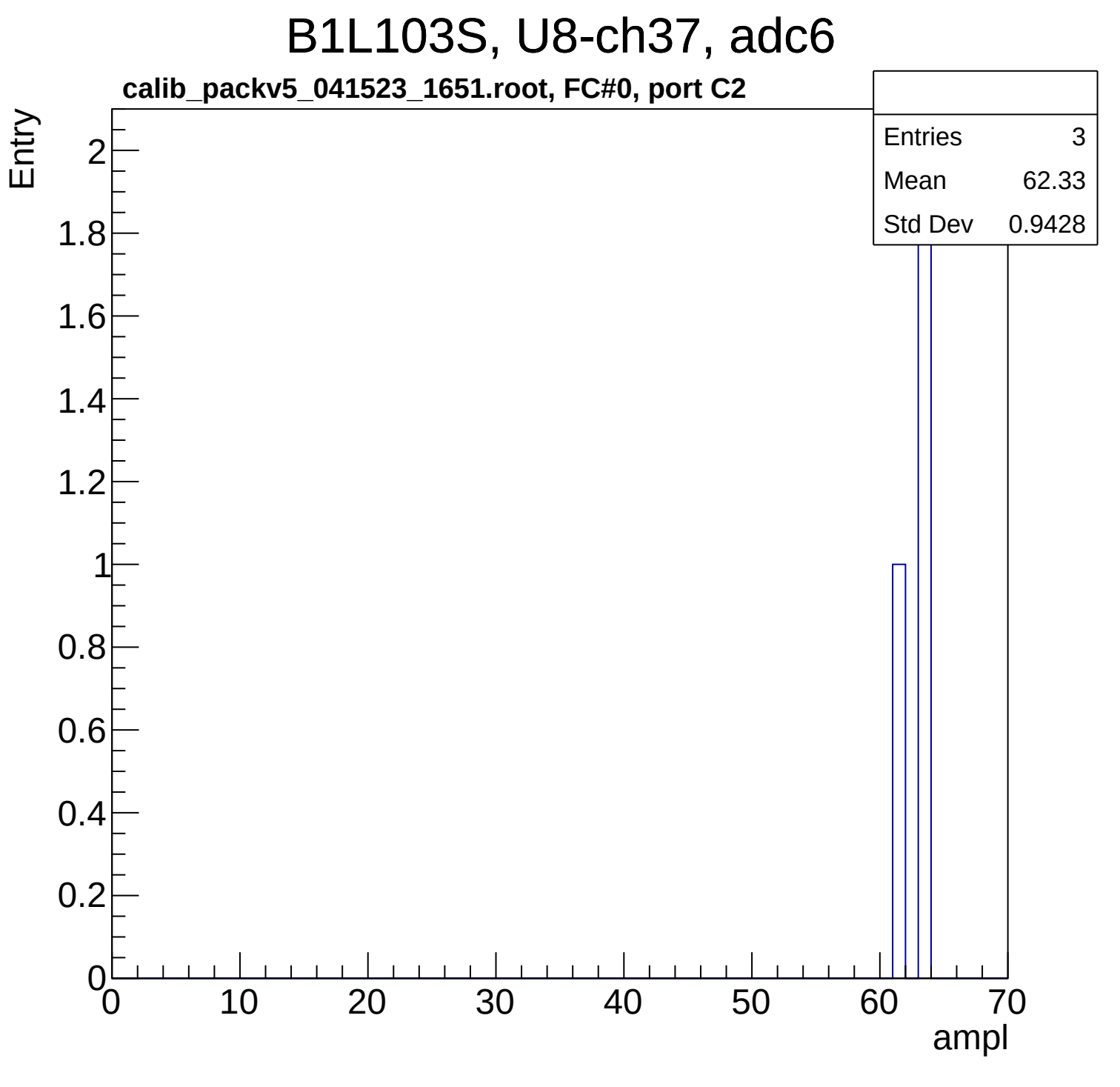
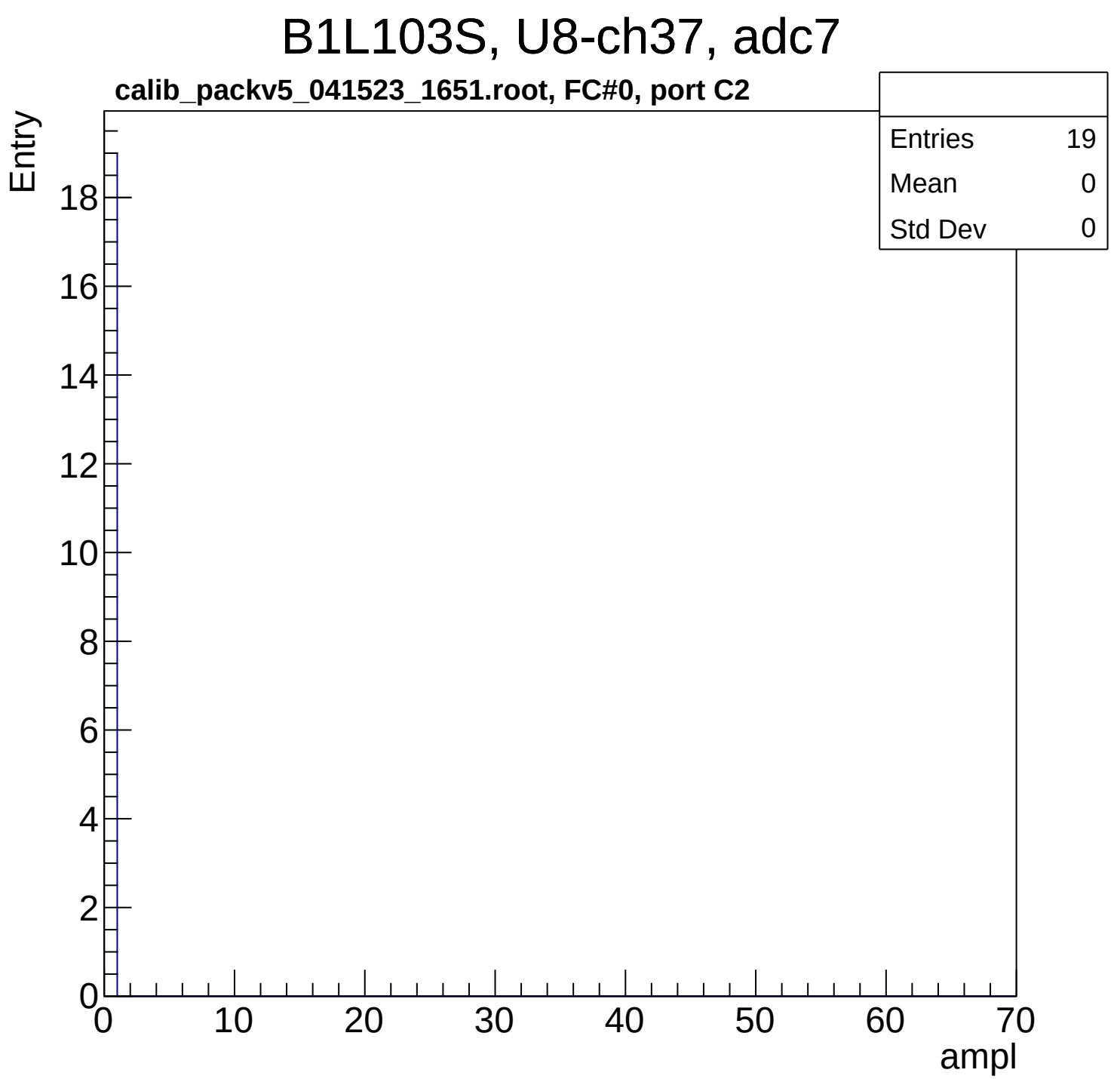
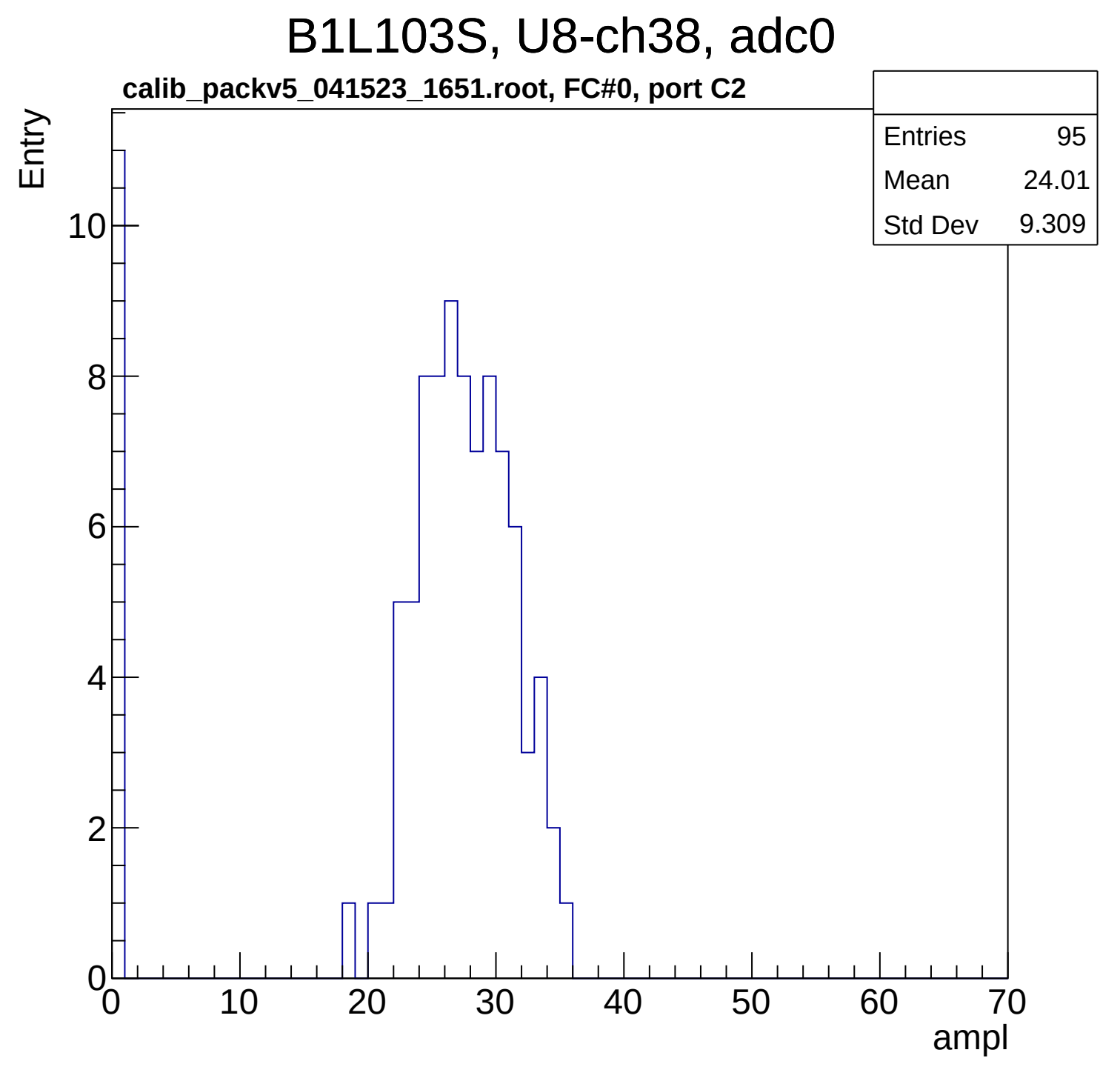
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U8-ch37, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 62.33
Std Dev 0.9428
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U8-ch37, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch38, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 24.01
Std Dev 9.309
Entry
ampl
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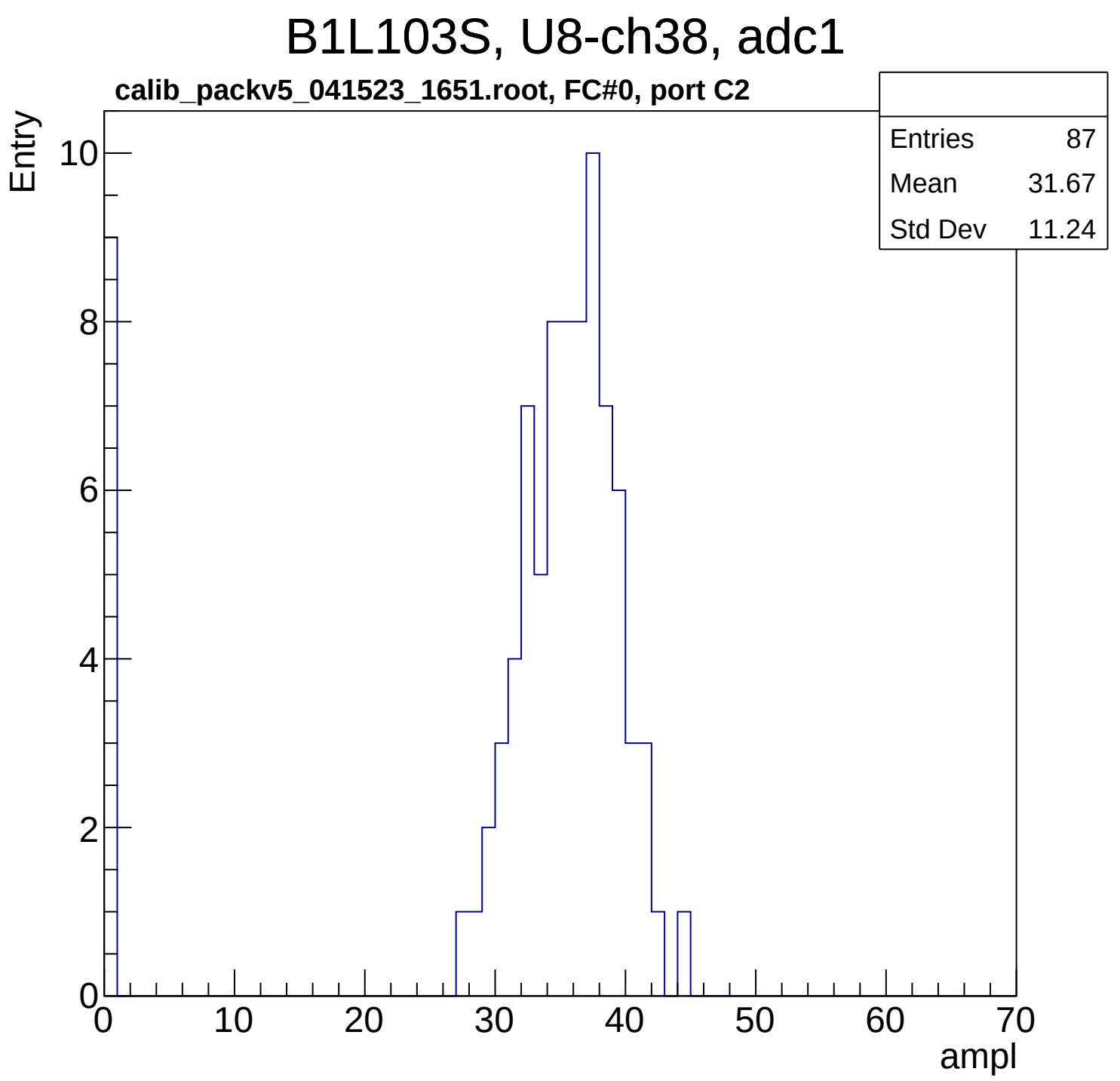
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U8-ch38, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 31.67
Std Dev 11.24
Entry
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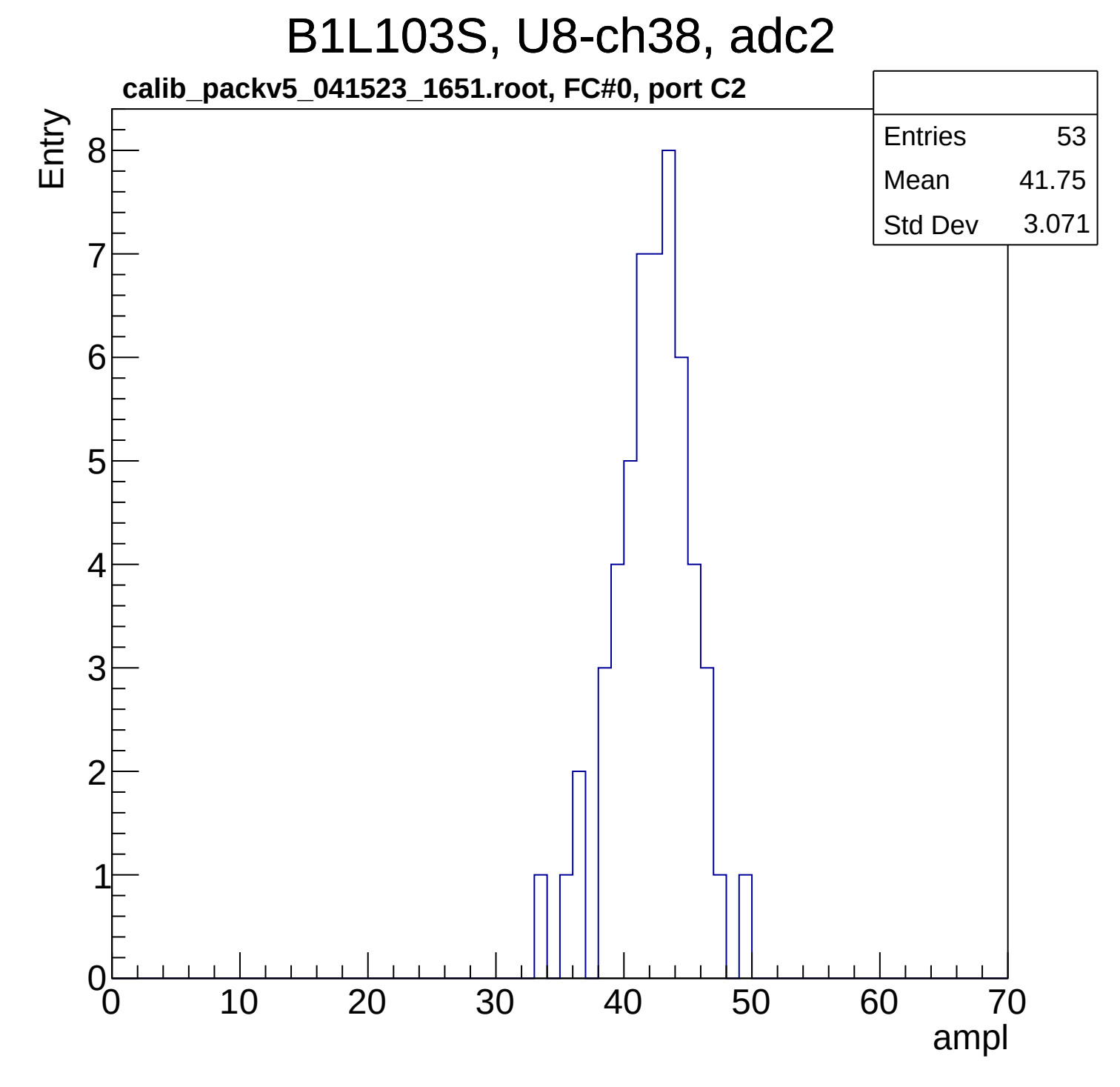
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch38, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 41.75
Std Dev 3.071
Entry
ampl
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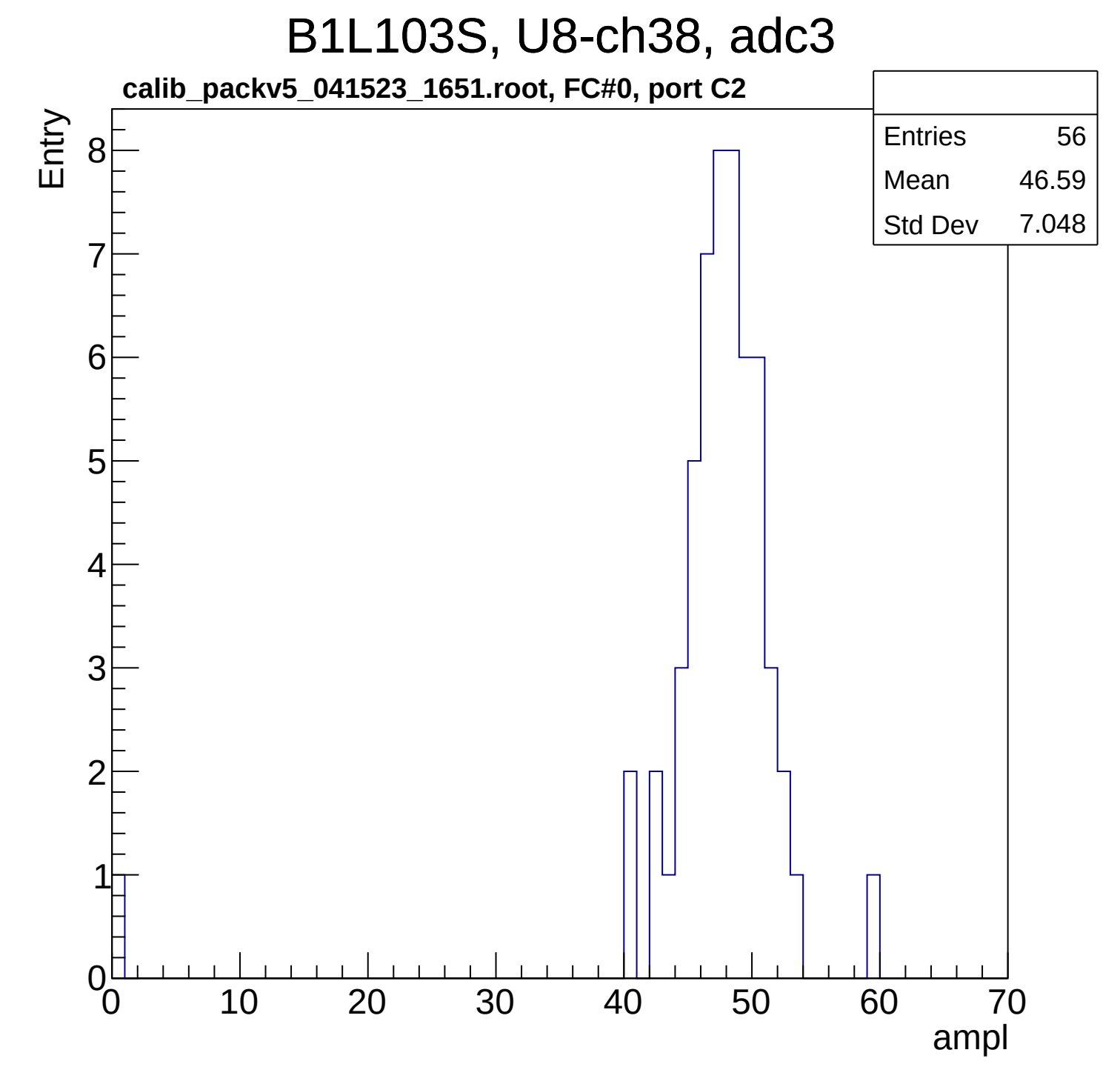
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch38, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 46.59
Std Dev 7.048
Entry
ampl
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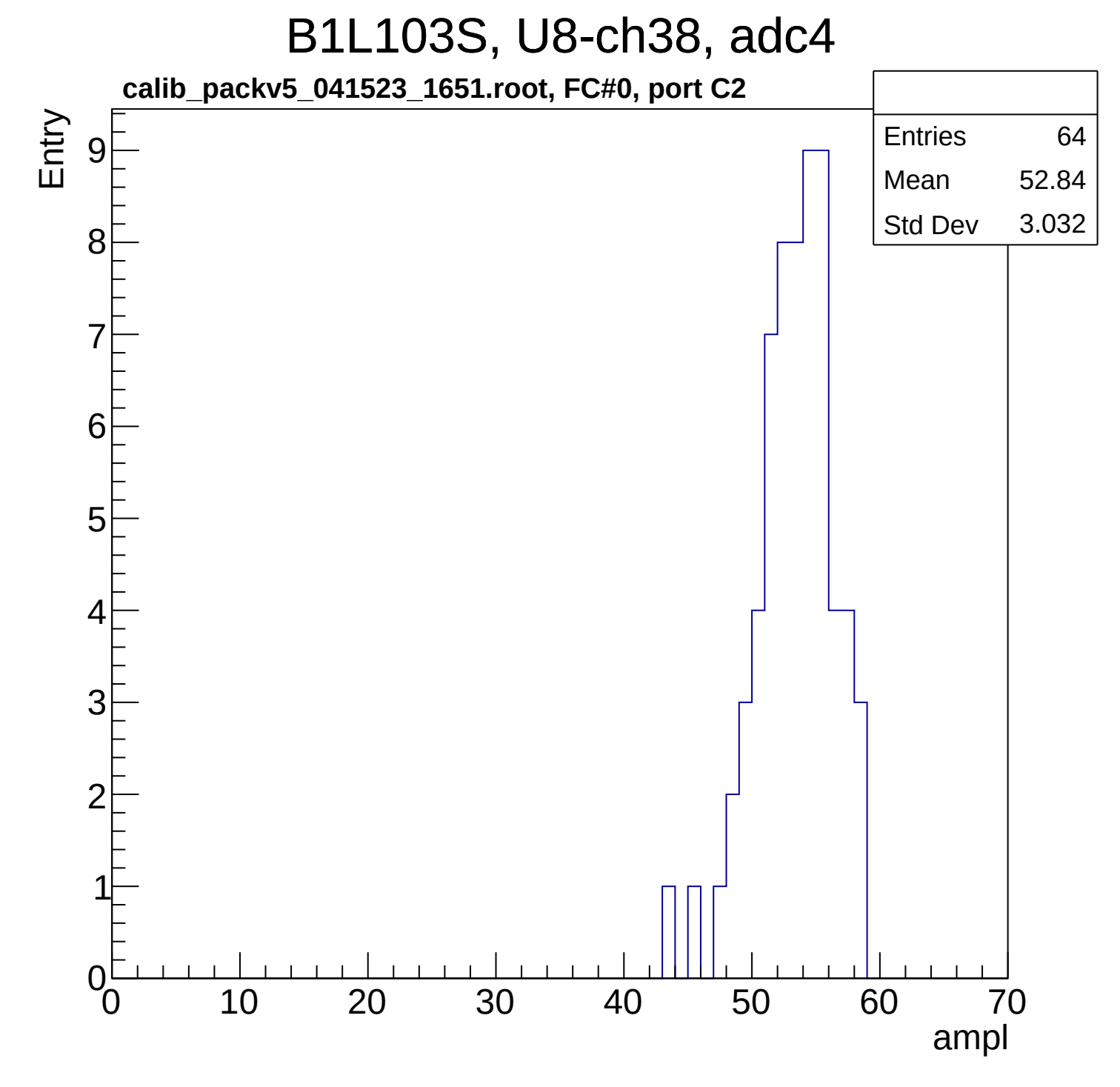
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch38, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 52.84
Std Dev 3.032
Entry
ampl
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3
4
5
6
7
8
9
0
10
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40
50
60
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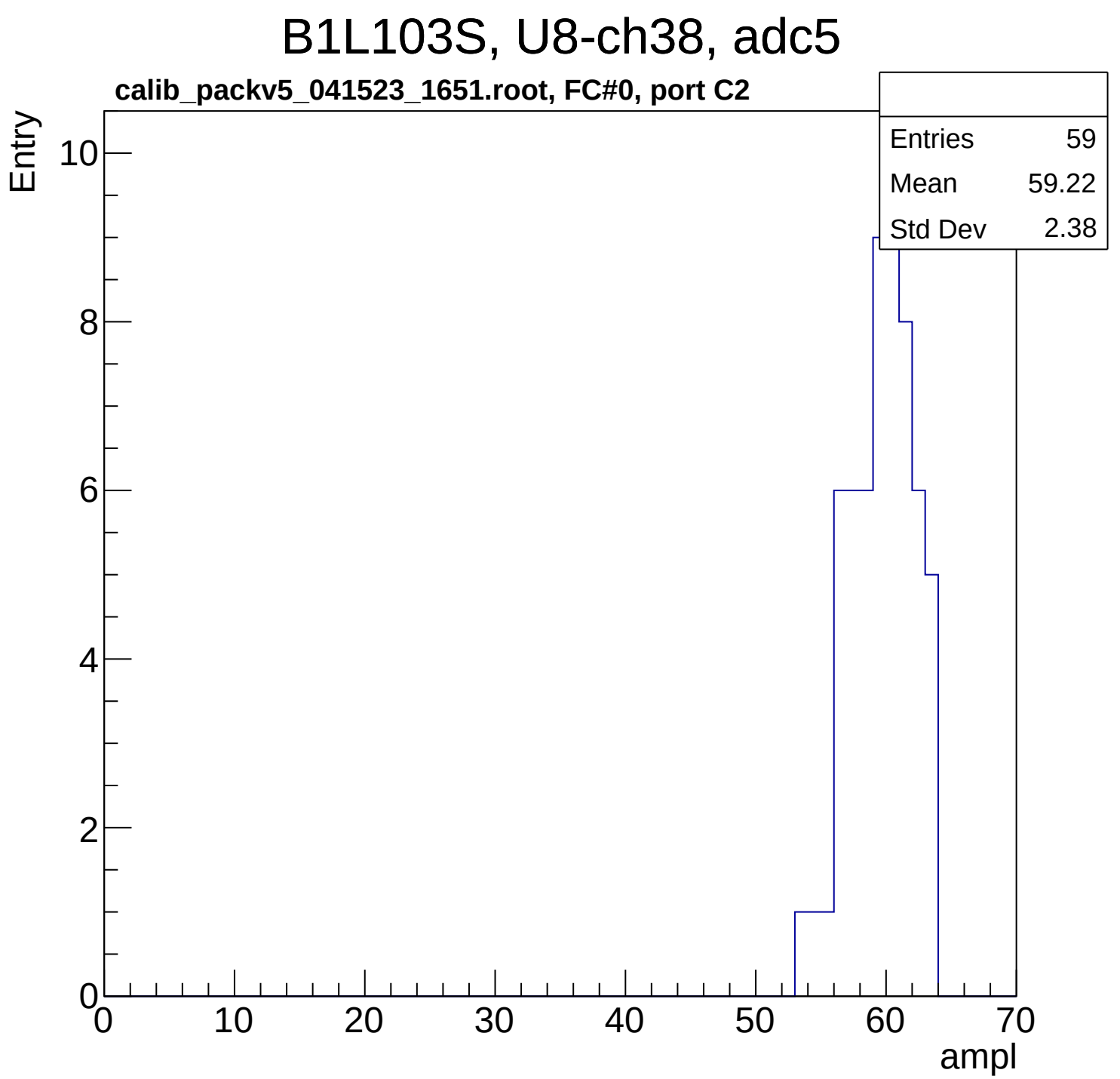
B1L103S, U8-ch38, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 59.22
Std Dev 2.38
Entry
0
2
4
6
8
10
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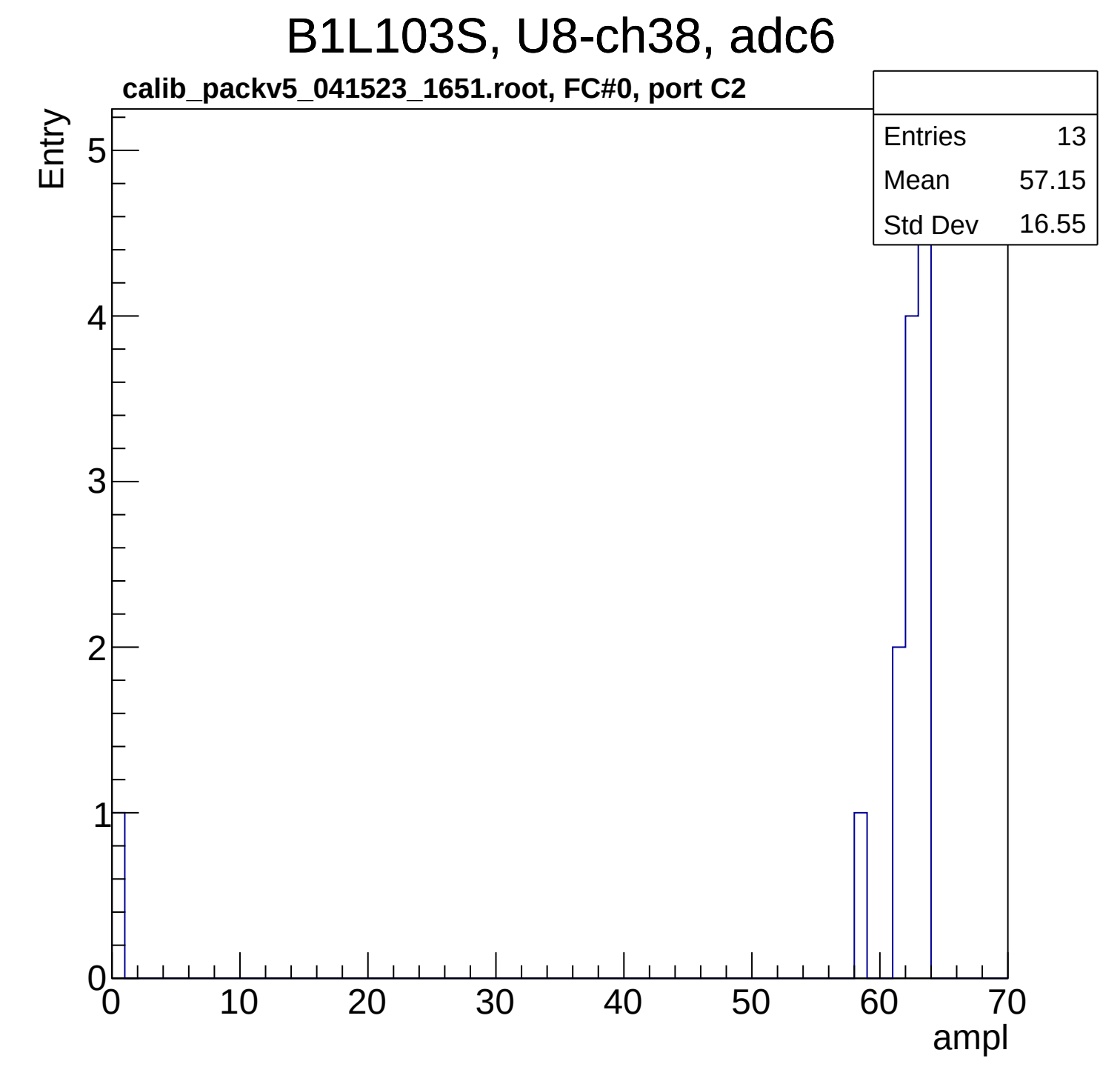
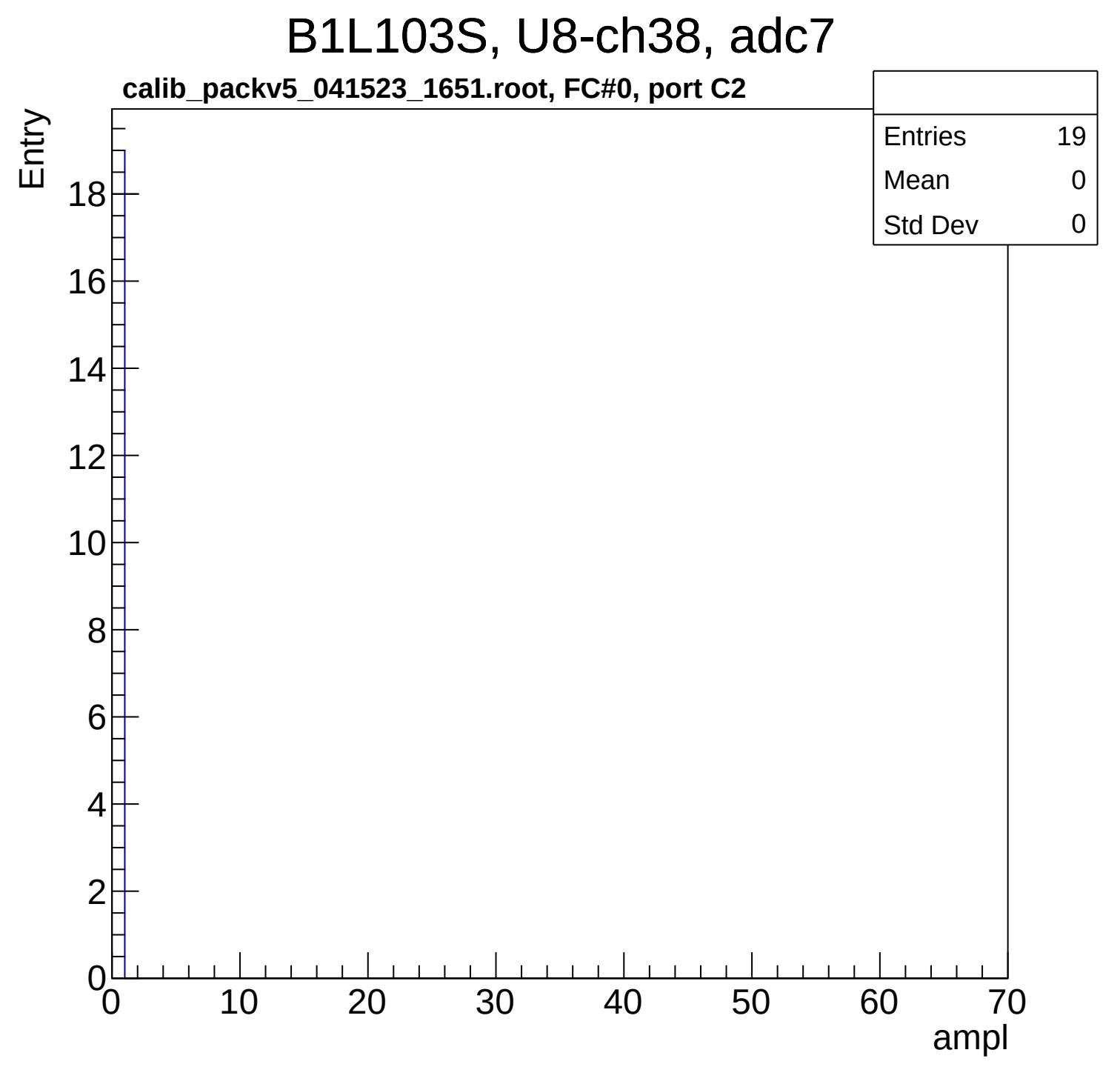
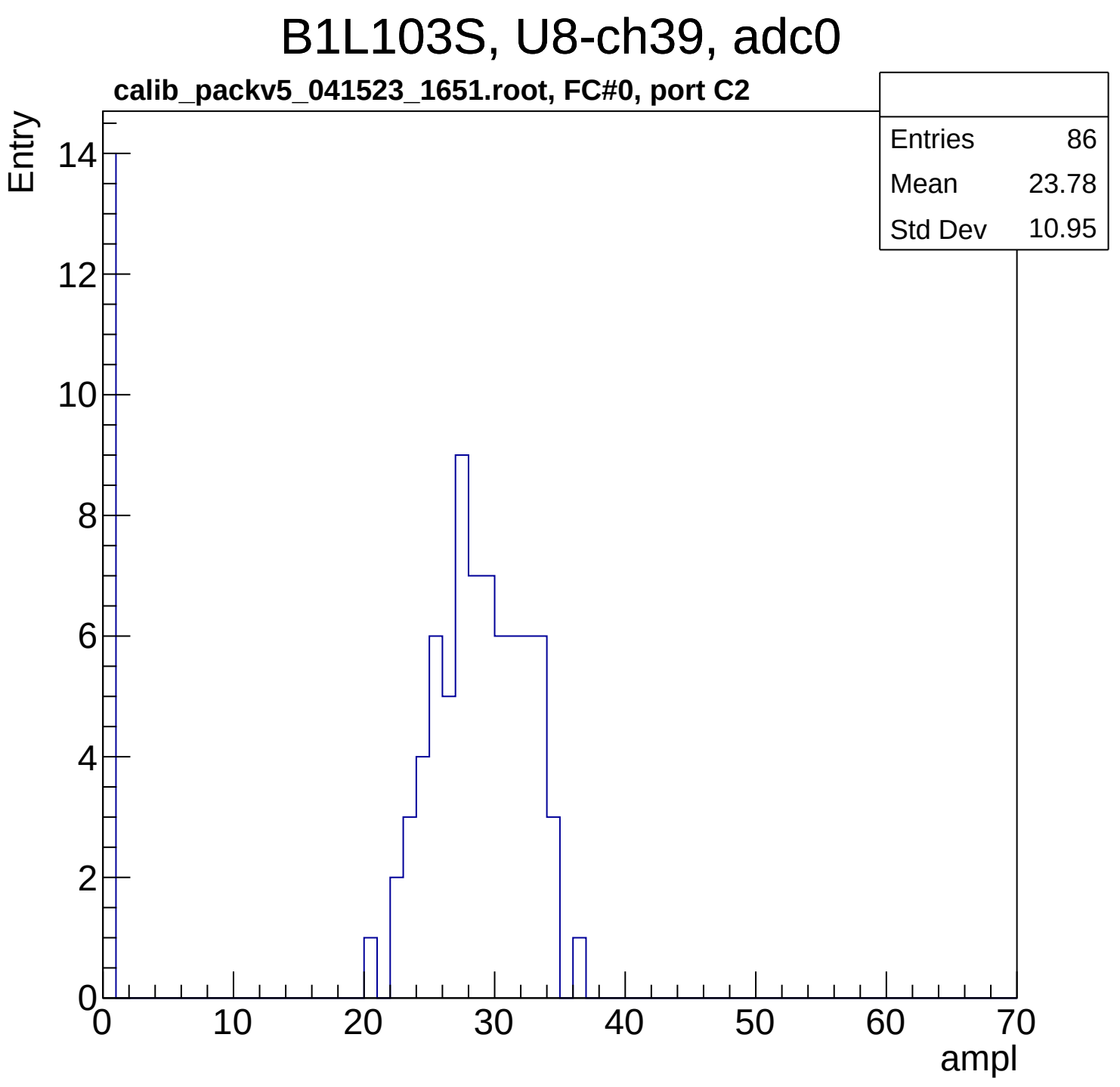
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch38, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 57.15
Std Dev 16.55
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U8-ch38, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch39, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 23.78
Std Dev 10.95
Entry
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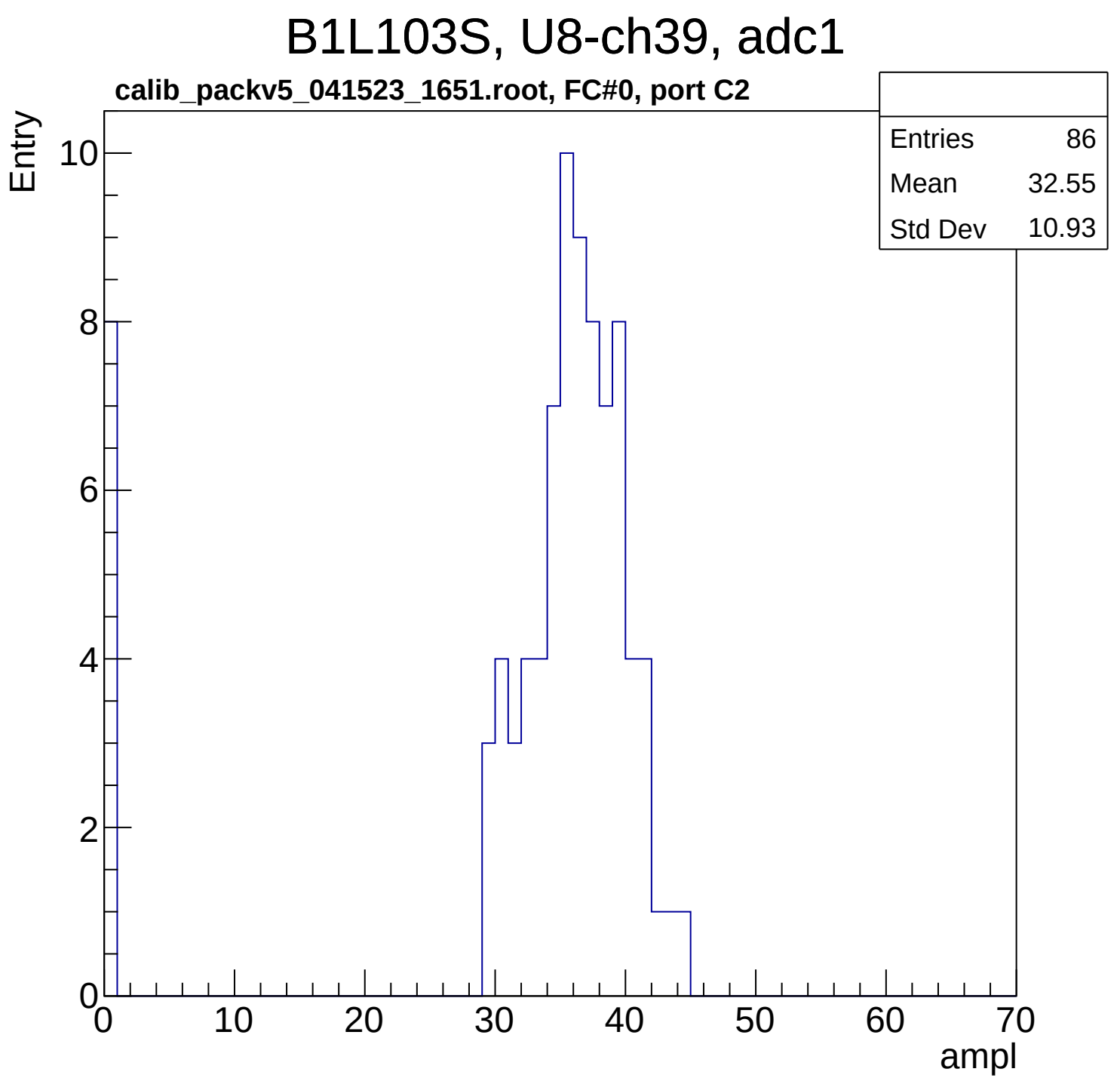
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch39, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 32.55
Std Dev 10.93
Entry
ampl
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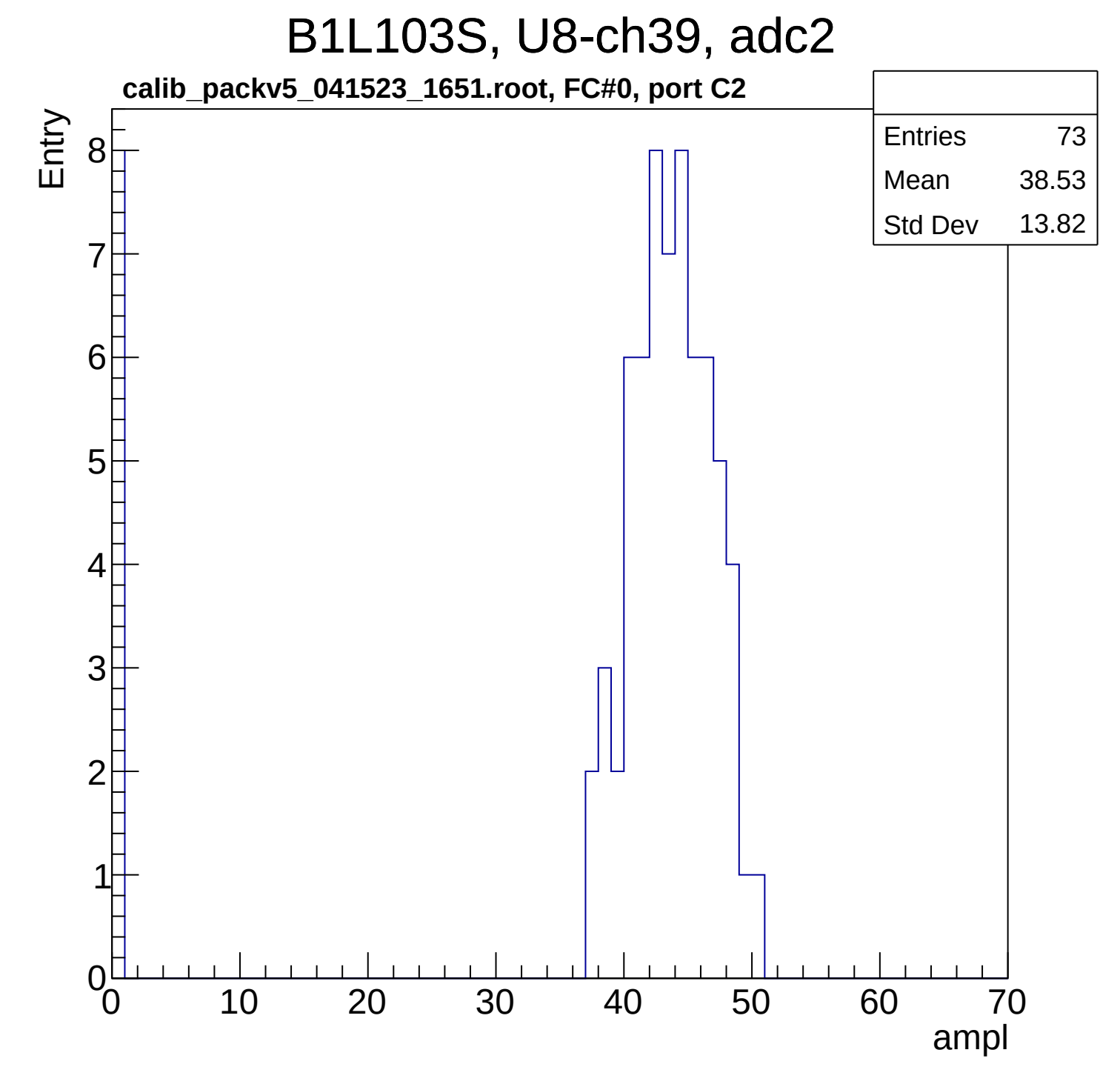
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U8-ch39, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 38.53
Std Dev 13.82
Entry
ampl
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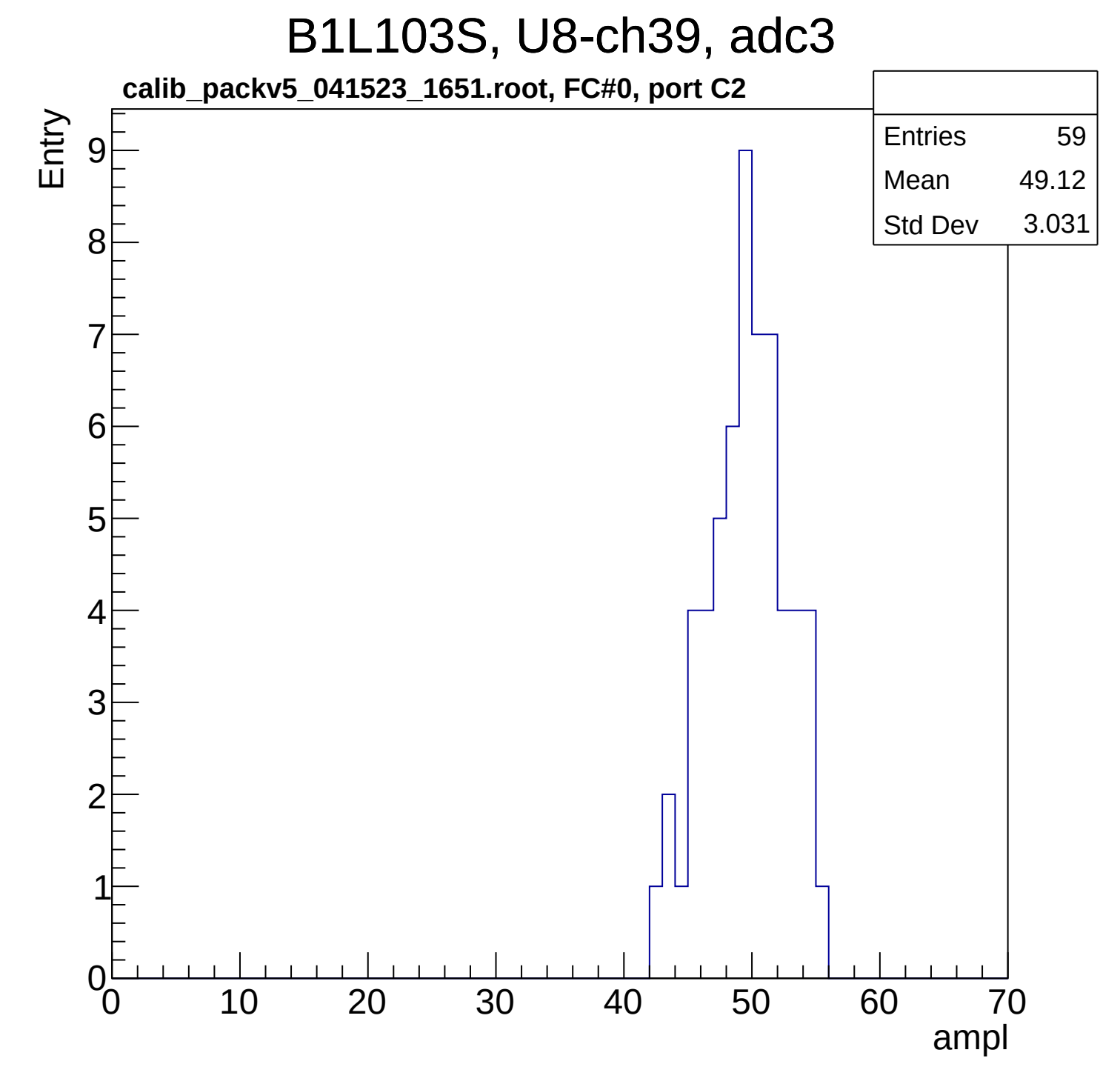
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch39, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 49.12
Std Dev 3.031
Entry
ampl
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2
3
4
5
6
7
8
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0
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60
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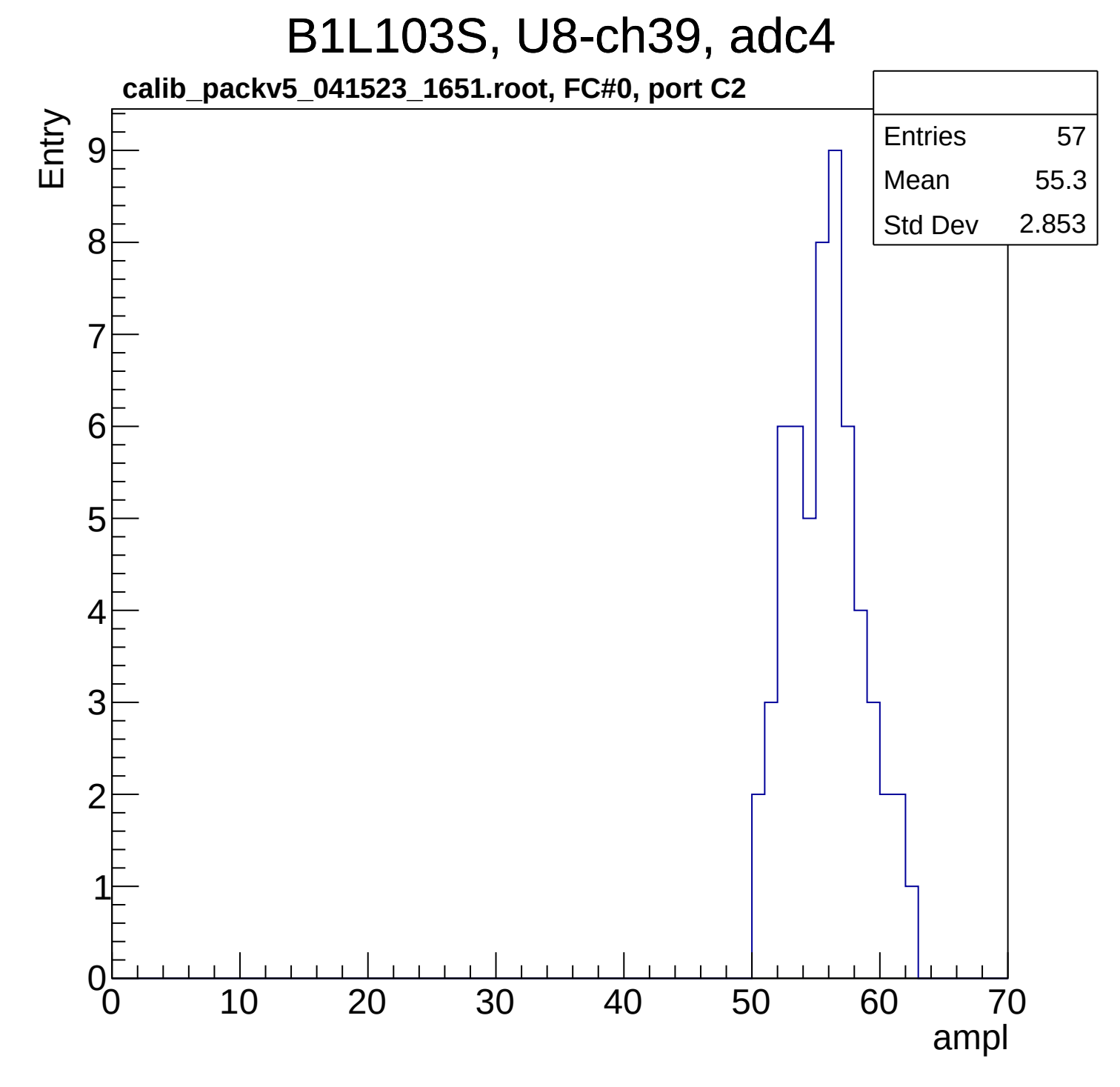
B1L103S, U8-ch39, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 55.3
Std Dev 2.853
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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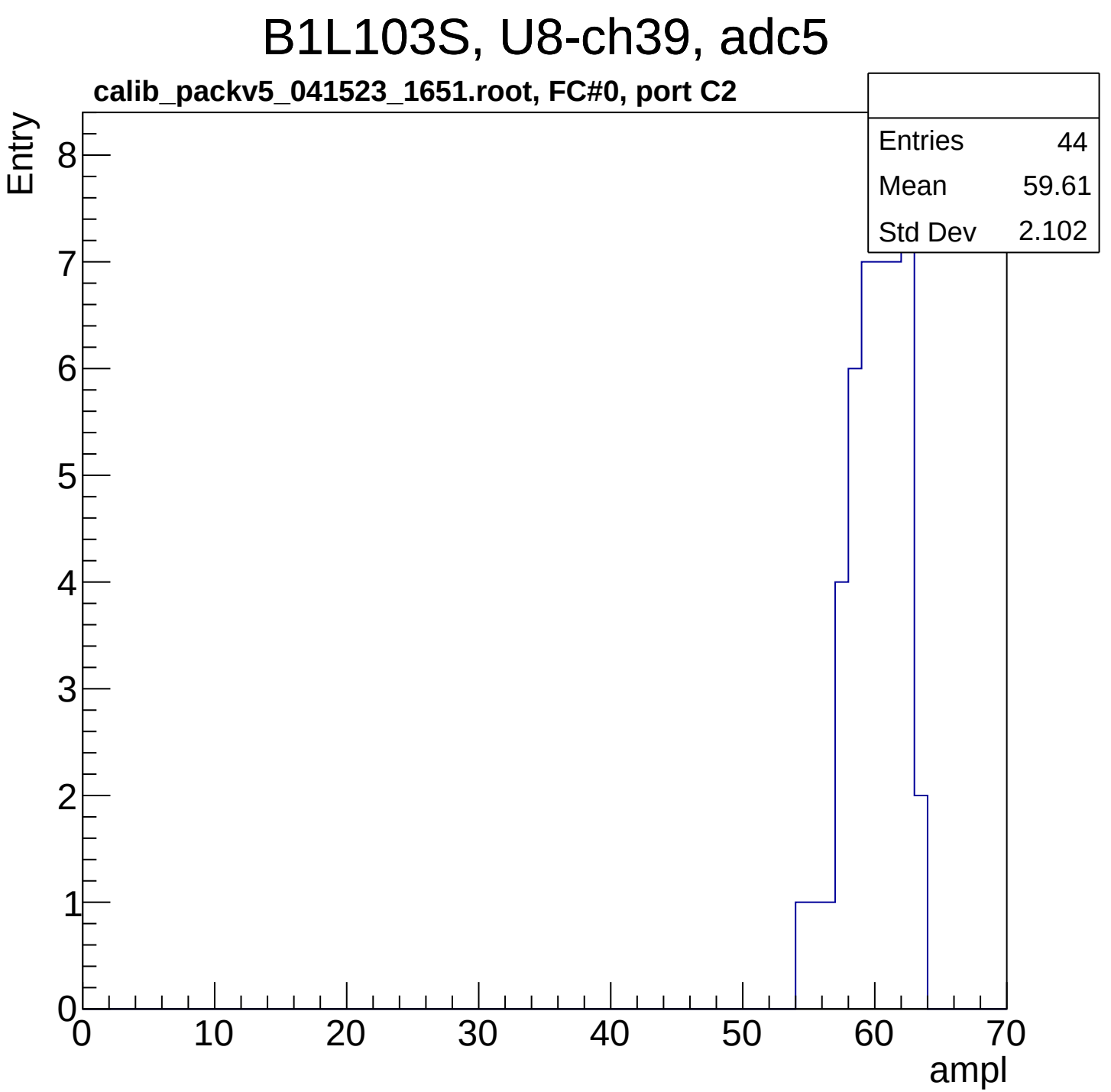
60
70


B1L103S, U8-ch39, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 59.61
Std Dev 2.102
Entry
ampl
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1
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5
6
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0
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20
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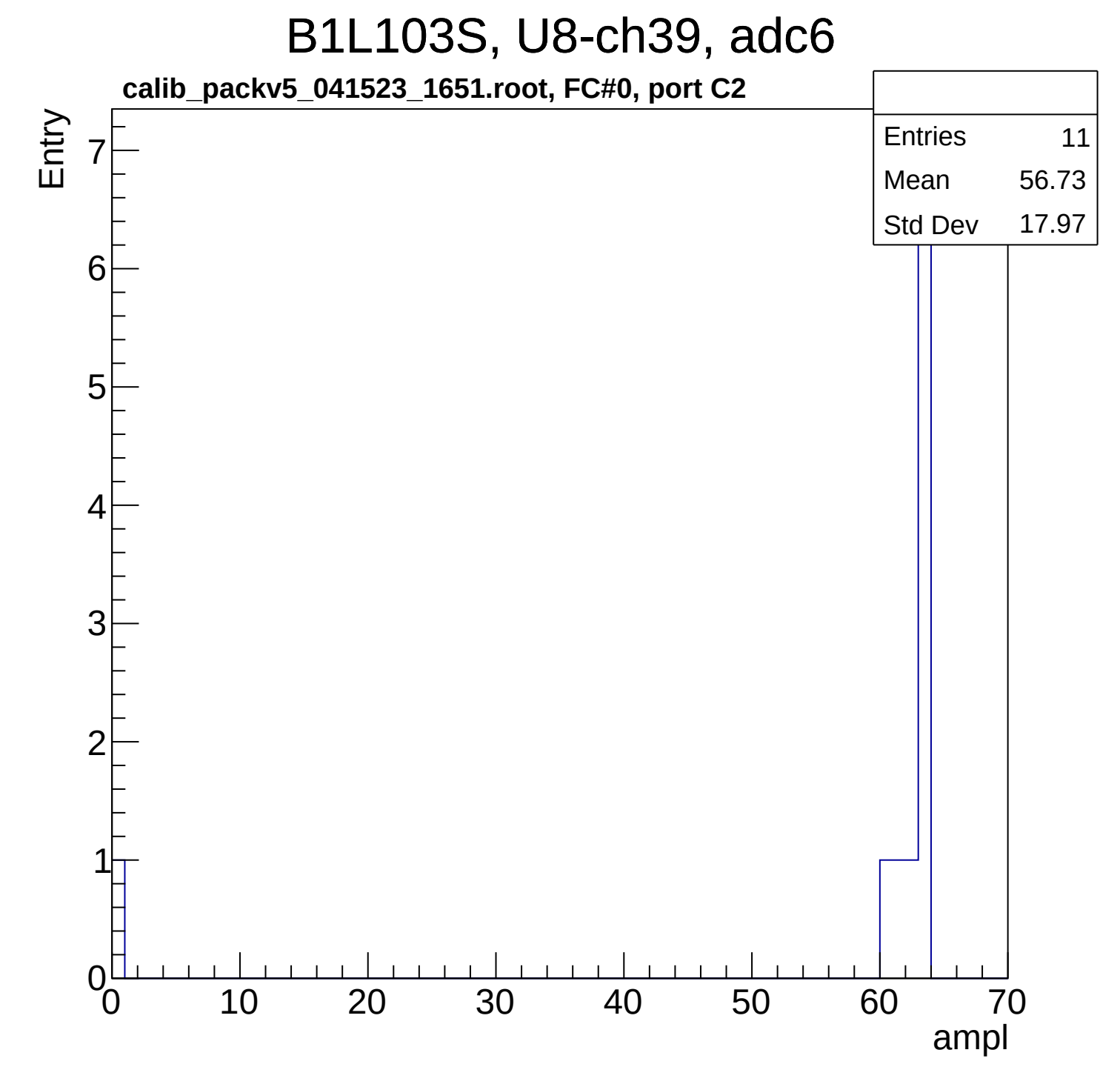
50
60
70


B1L103S, U8-ch39, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 56.73
Std Dev 17.97
Entry
ampl
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2
3
4
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6
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0
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60
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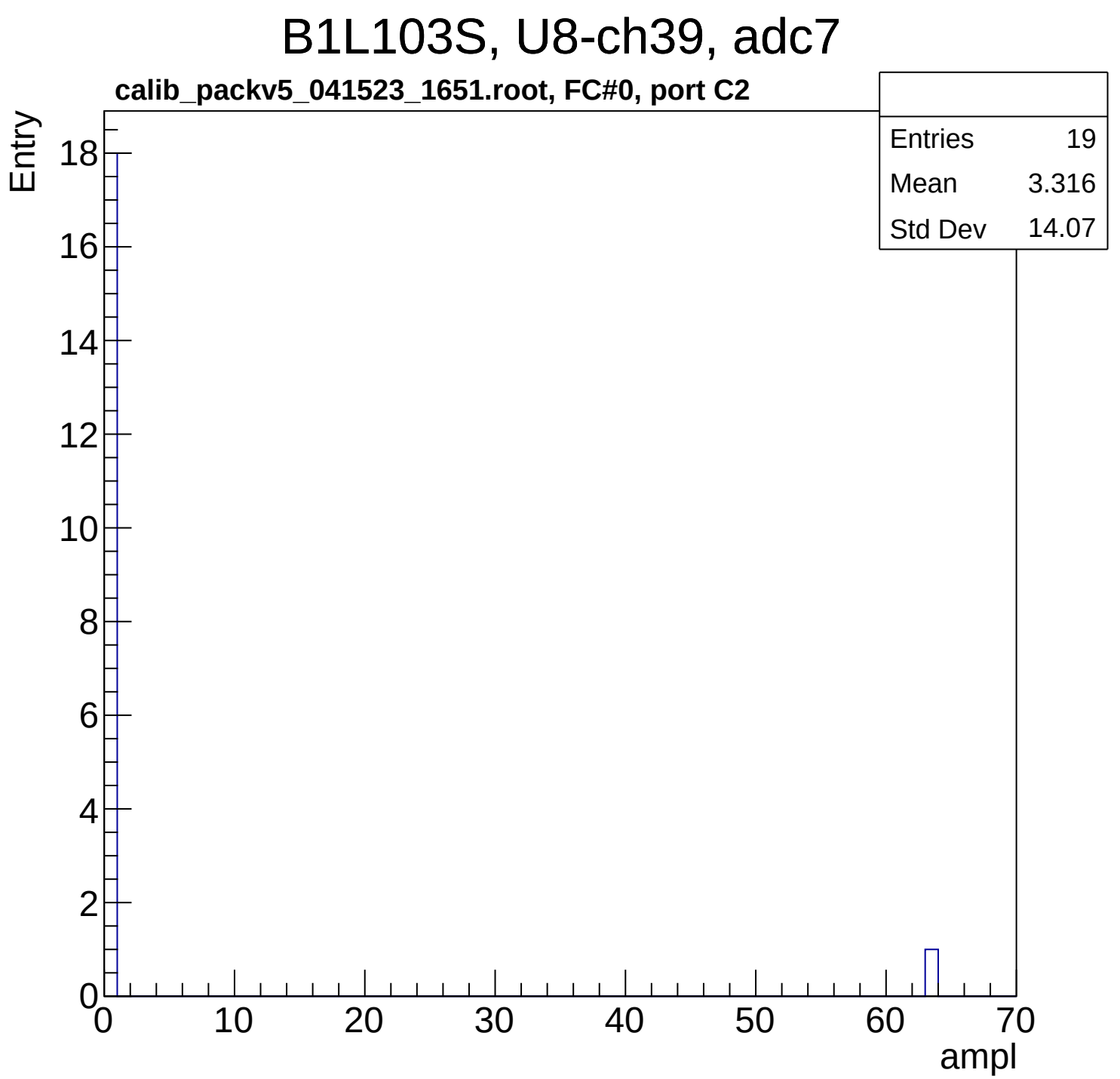
B1L103S, U8-ch39, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.316
Std Dev 14.07
Entry
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6
8
10
12
14
16
18
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10
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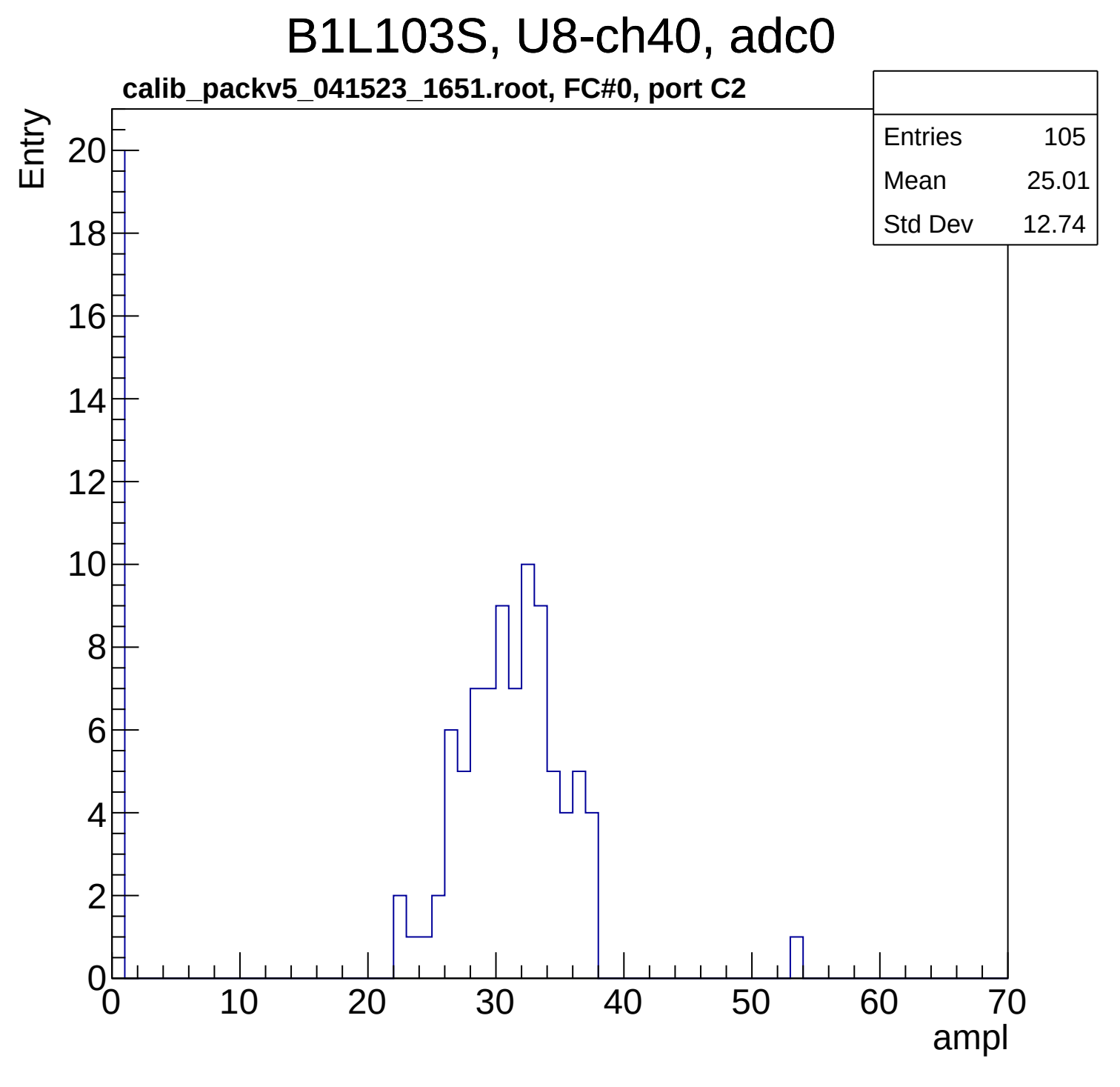
50
60
70
ampl


B1L103S, U8-ch40, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 105
Mean 25.01
Std Dev 12.74
Entry
ampl
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6
8
10
12
14
16
18
20
0
10
20
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40
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60
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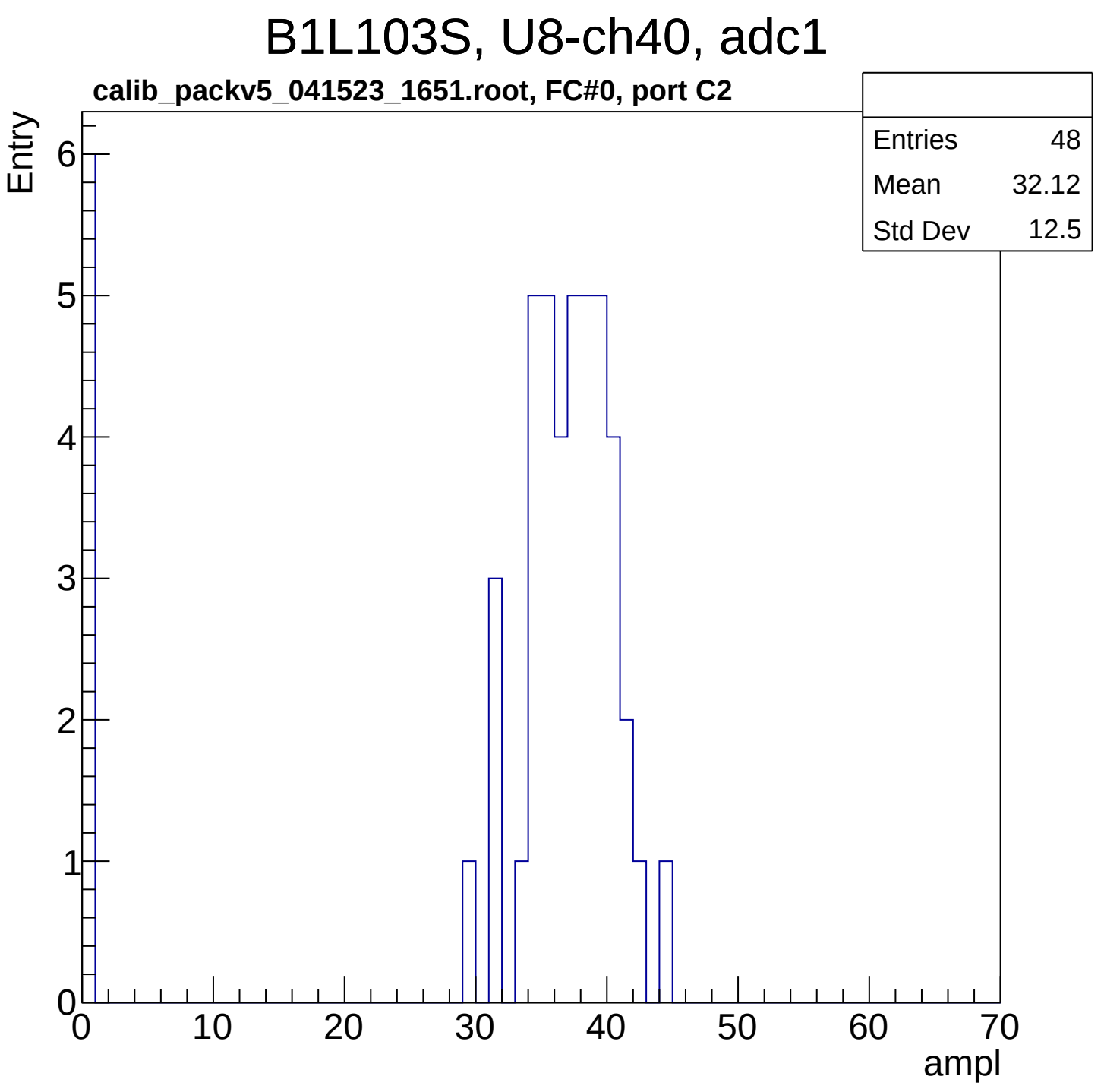
B1L103S, U8-ch40, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 32.12
Std Dev 12.5
Entry
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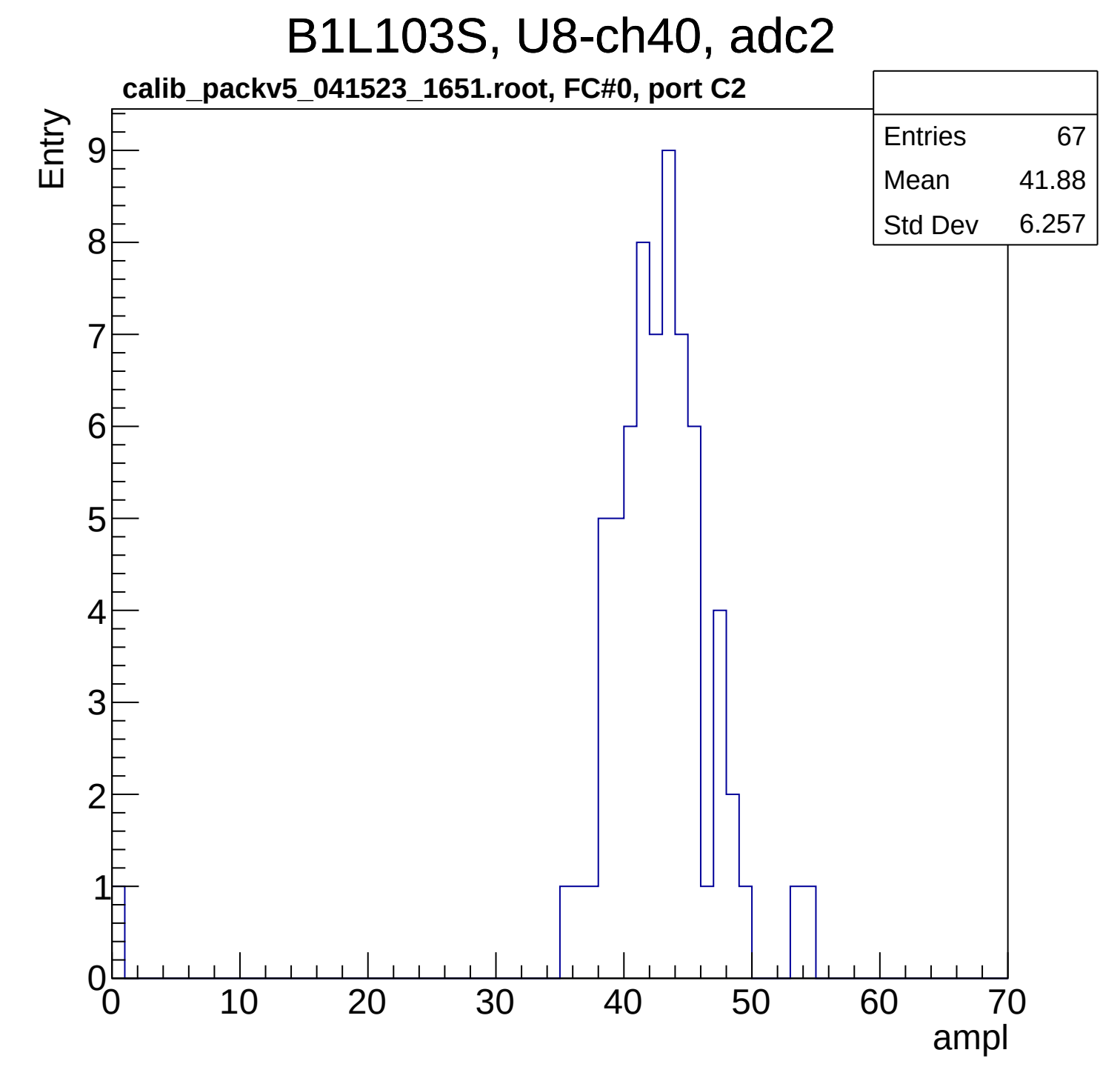
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch40, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 41.88
Std Dev 6.257
Entry
ampl
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3
4
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6
7
8
9
0
10
20
30
40
50
60
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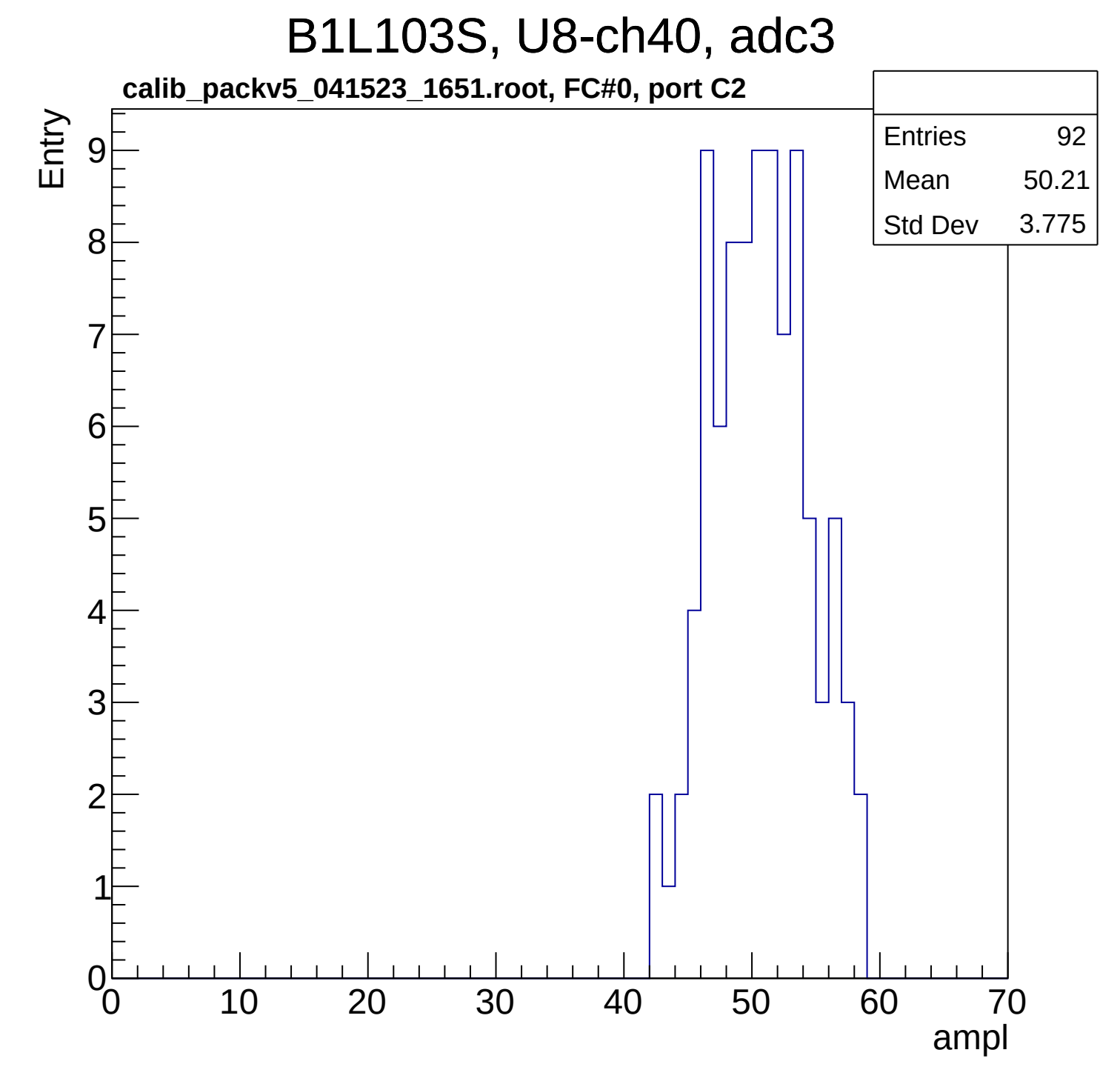
B1L103S, U8-ch40, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 50.21
Std Dev 3.775
Entry
ampl
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3
4
5
6
7
8
9
0
10
20
30
40
50
60
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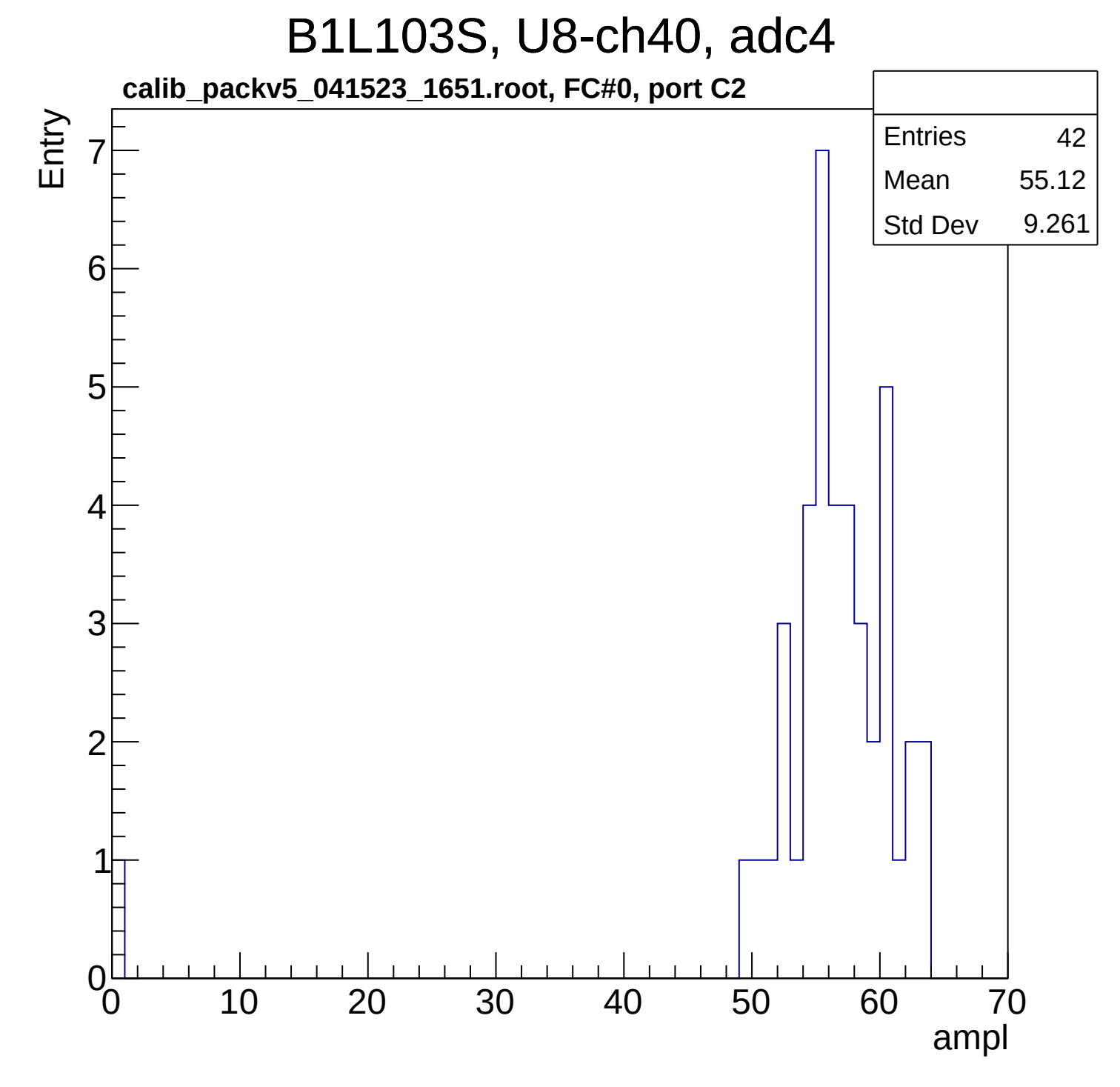
B1L103S, U8-ch40, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 55.12
Std Dev 9.261
Entry
ampl
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2
3
4
5
6
7
0
10
20
30
40
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60
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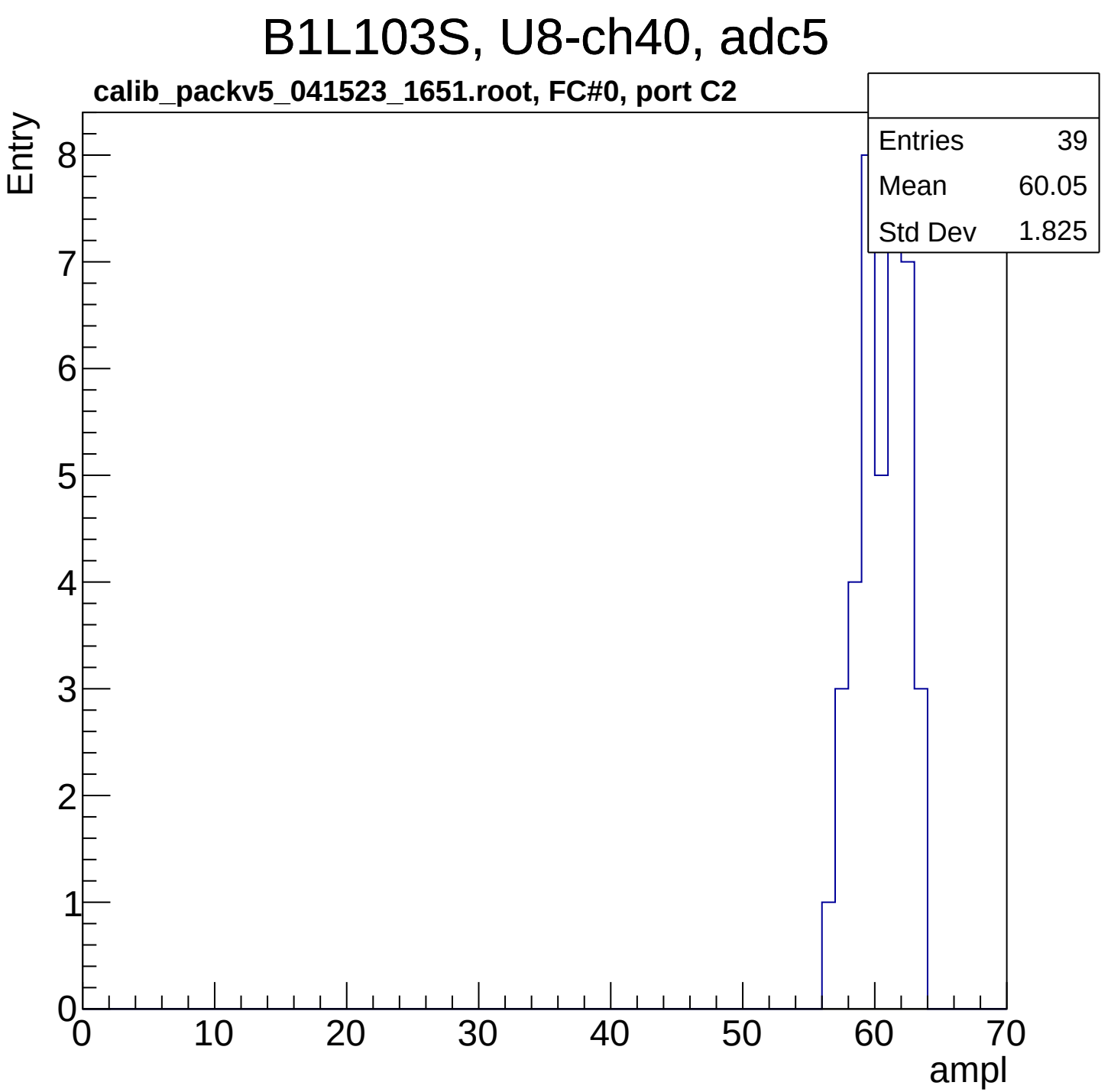
B1L103S, U8-ch40, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 60.05
Std Dev 1.825
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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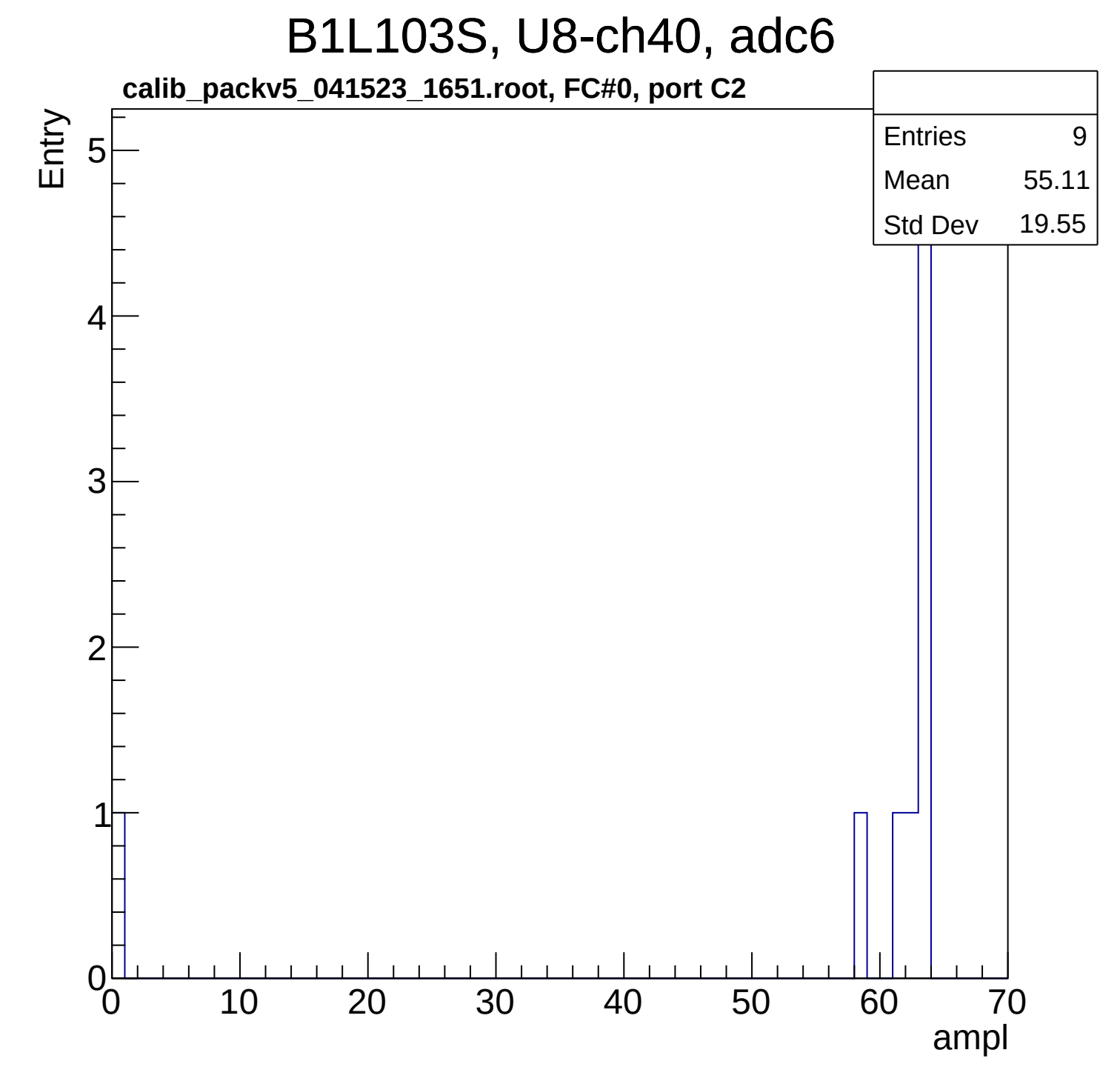
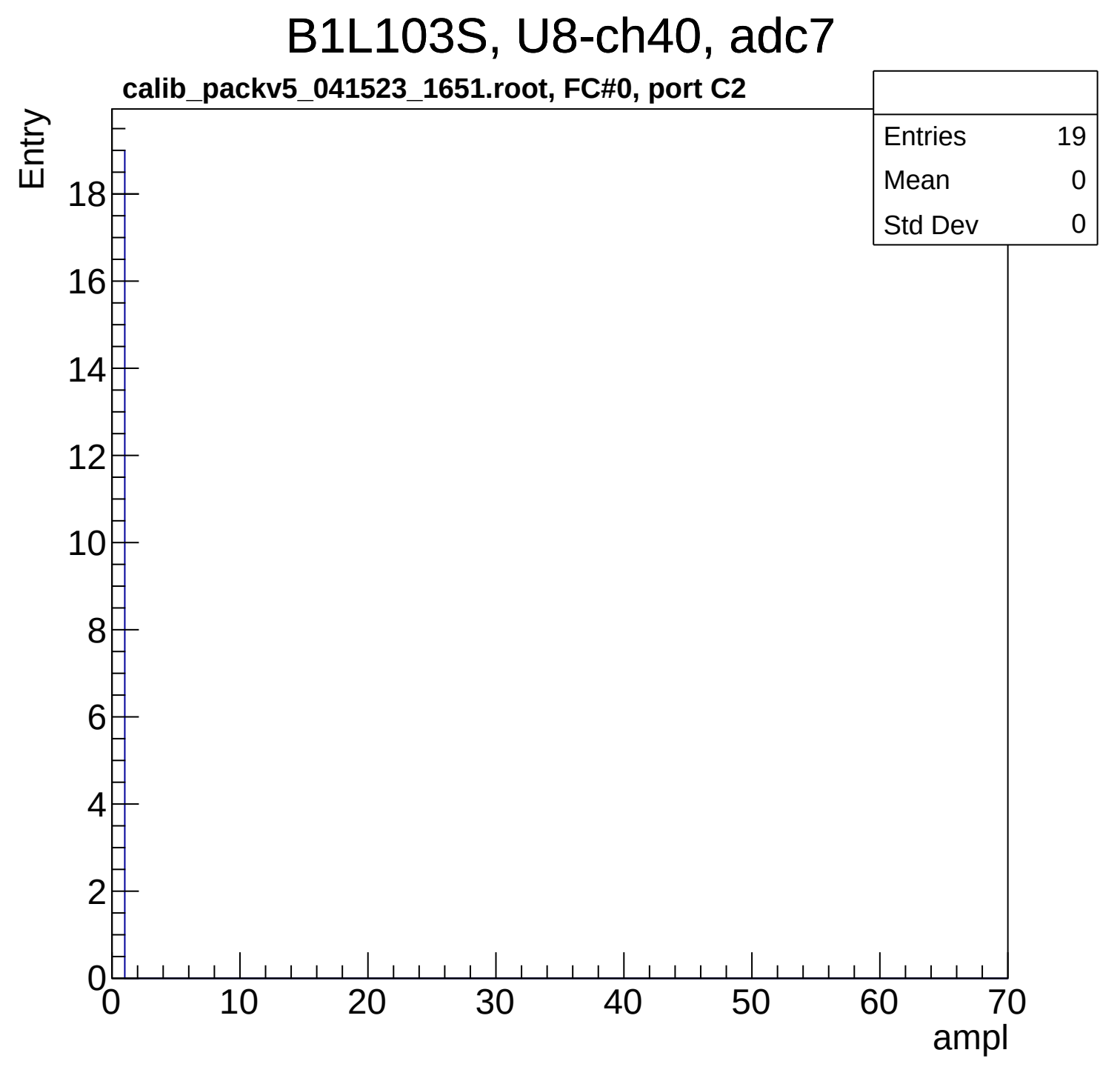
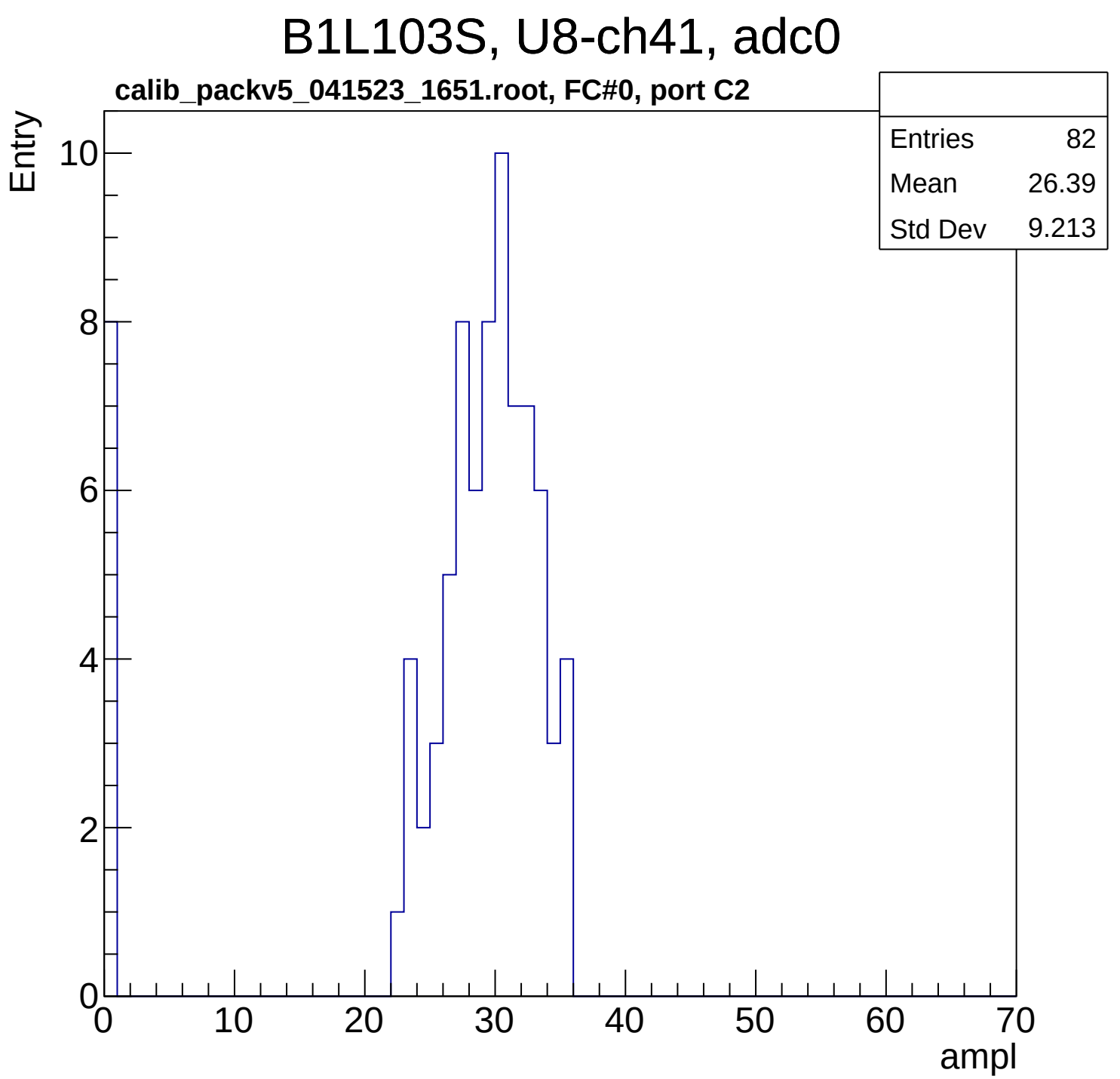

B1L103S, U8-ch40, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 55.11
Std Dev 19.55
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U8-ch40, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch41, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 26.39
Std Dev 9.213
Entry
ampl
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4
6
8
10
0
10
20
30
40
50
60
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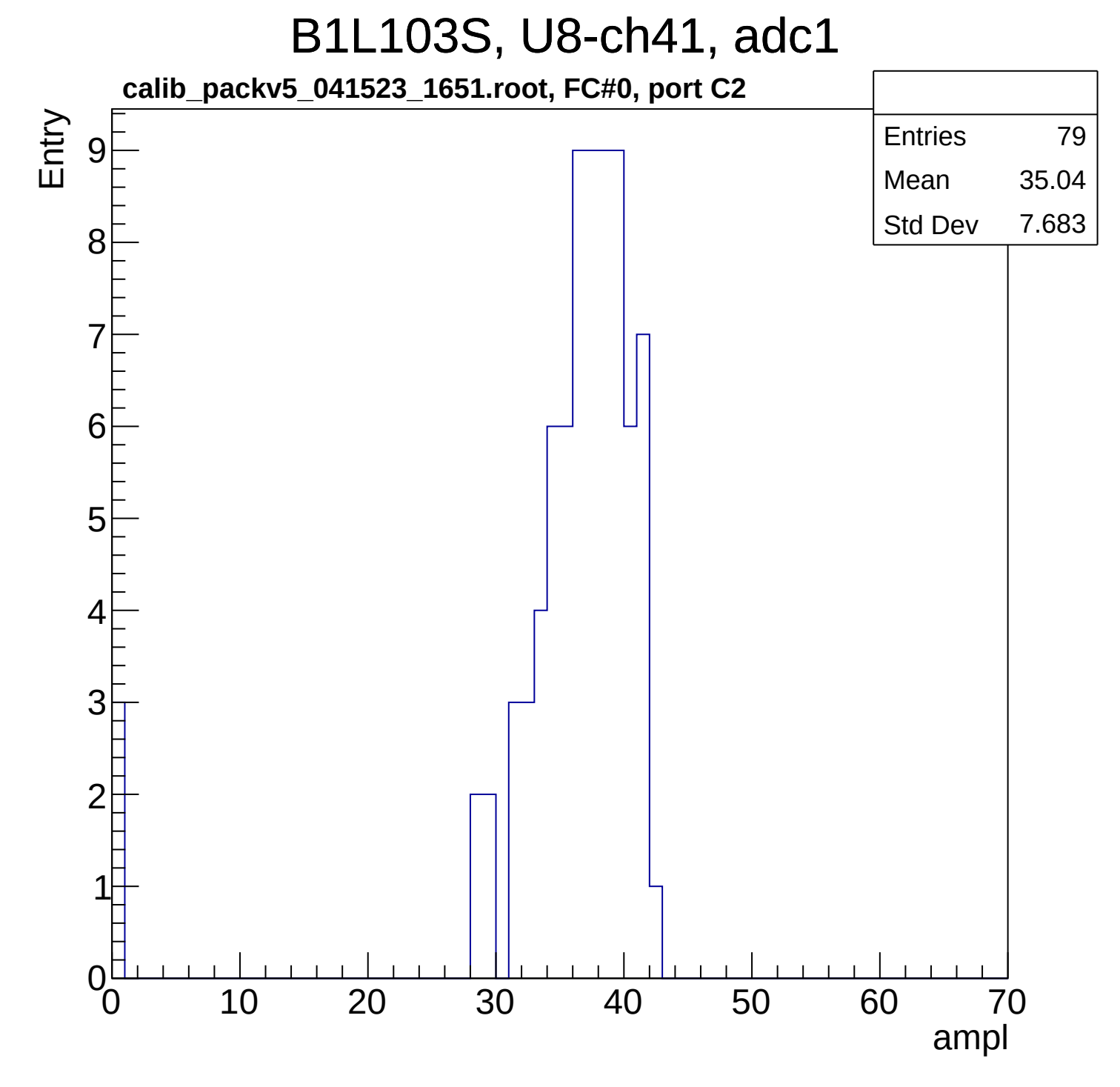
B1L103S, U8-ch41, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 35.04
Std Dev 7.683
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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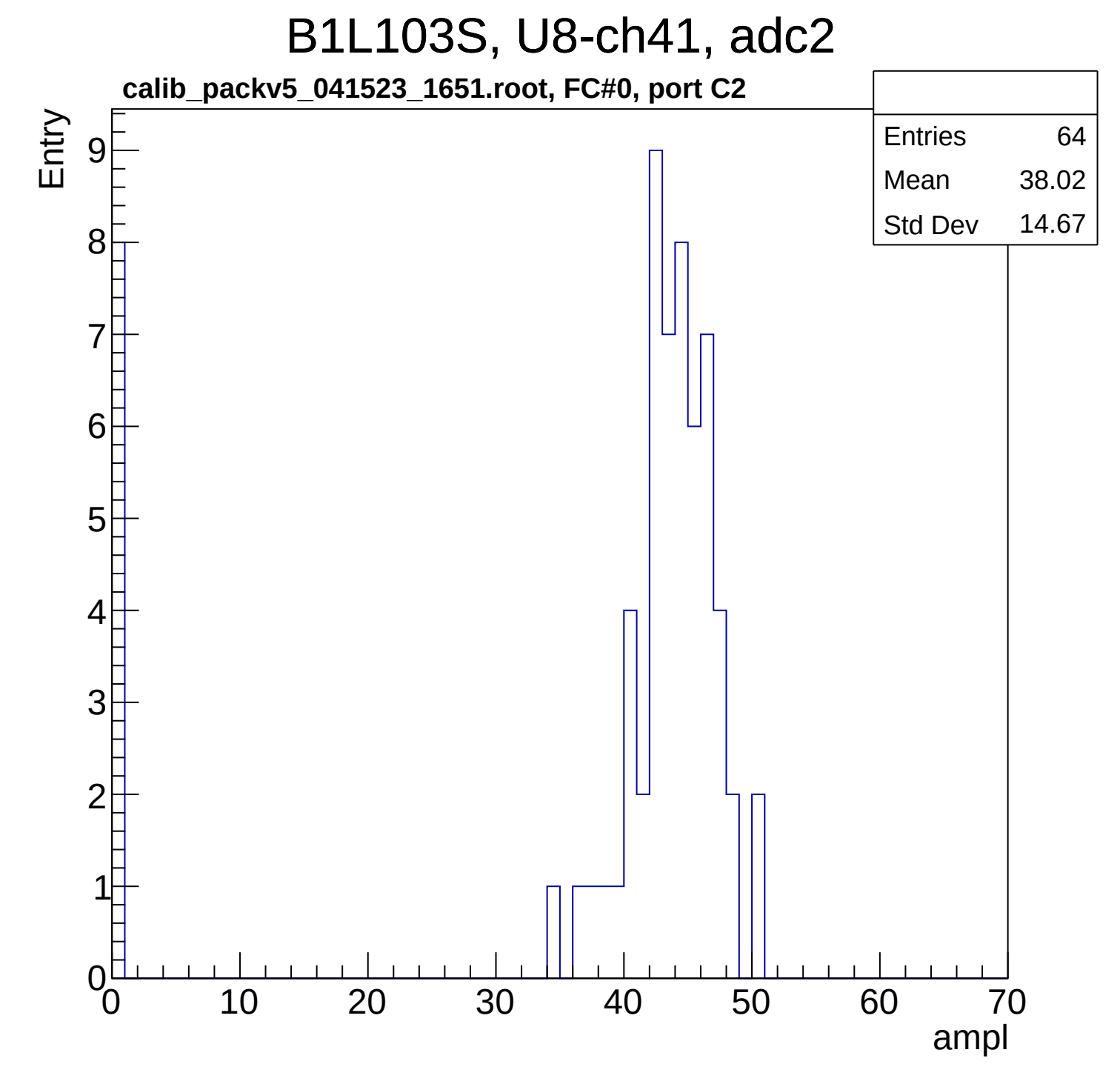
B1L103S, U8-ch41, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 38.02
Std Dev 14.67
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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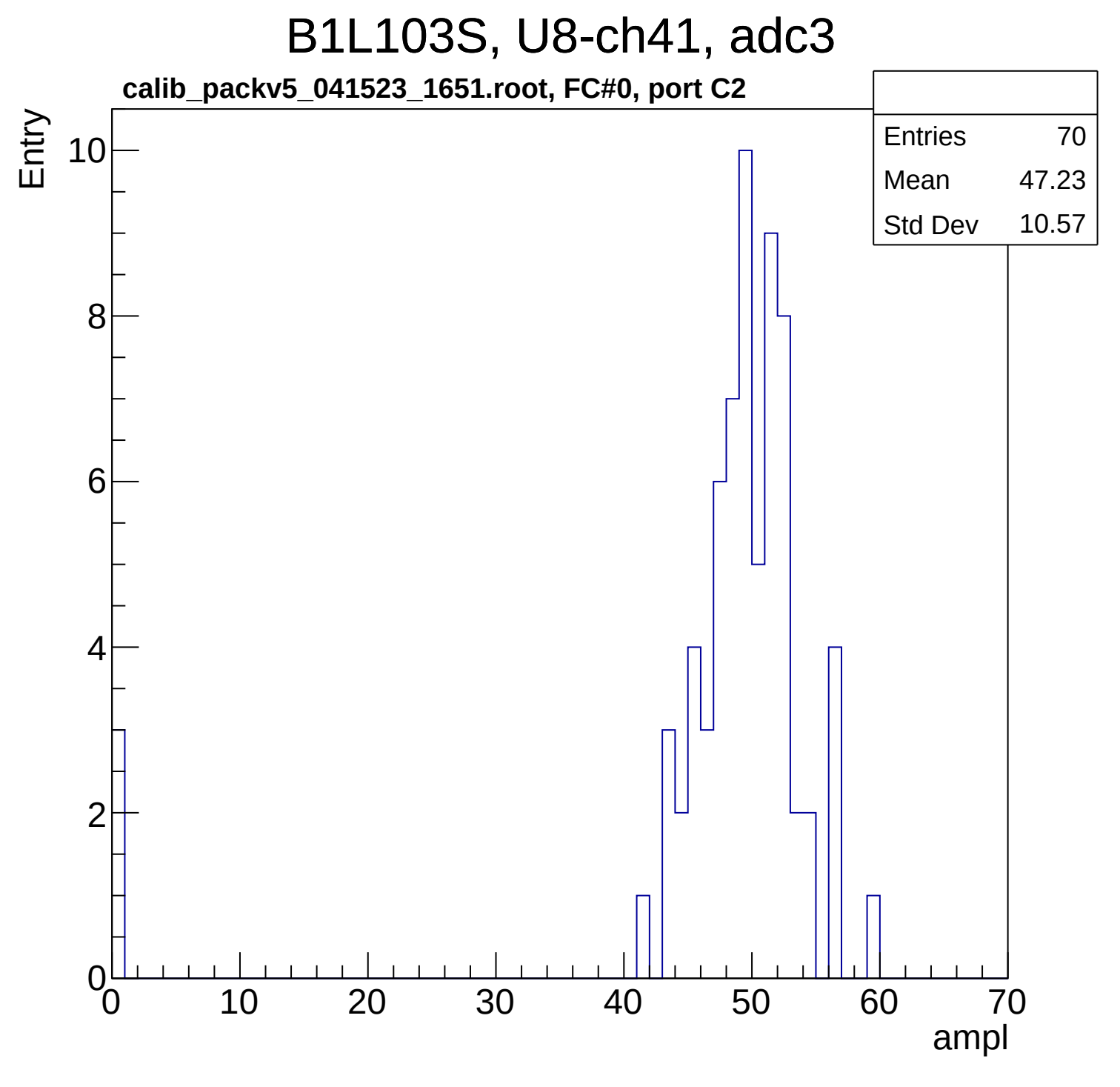
B1L103S, U8-ch41, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 47.23
Std Dev 10.57
Entry
ampl
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4
6
8
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0
10
20
30
40
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60
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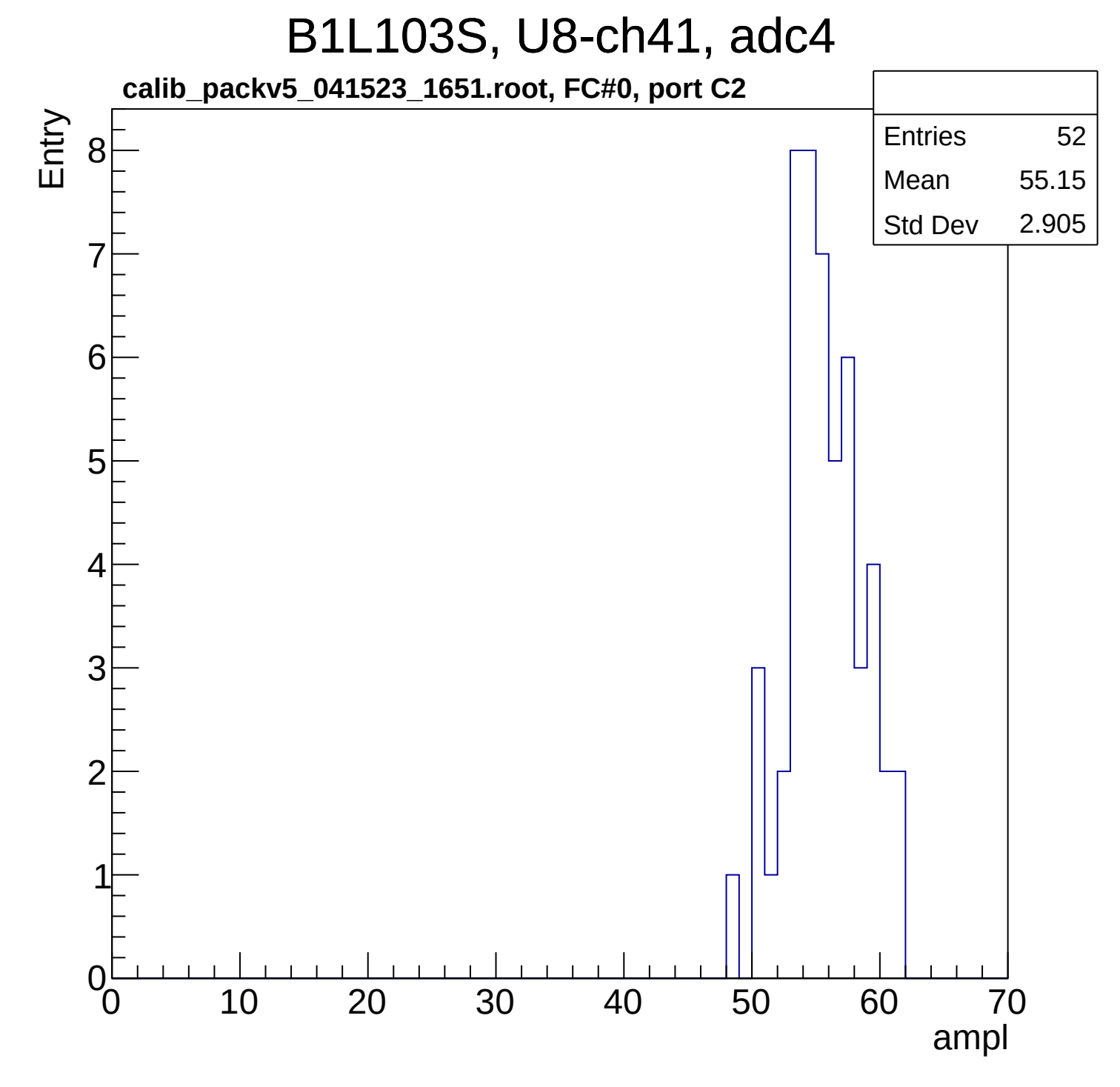
B1L103S, U8-ch41, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 55.15
Std Dev 2.905
Entry
ampl
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2
3
4
5
6
7
8
0
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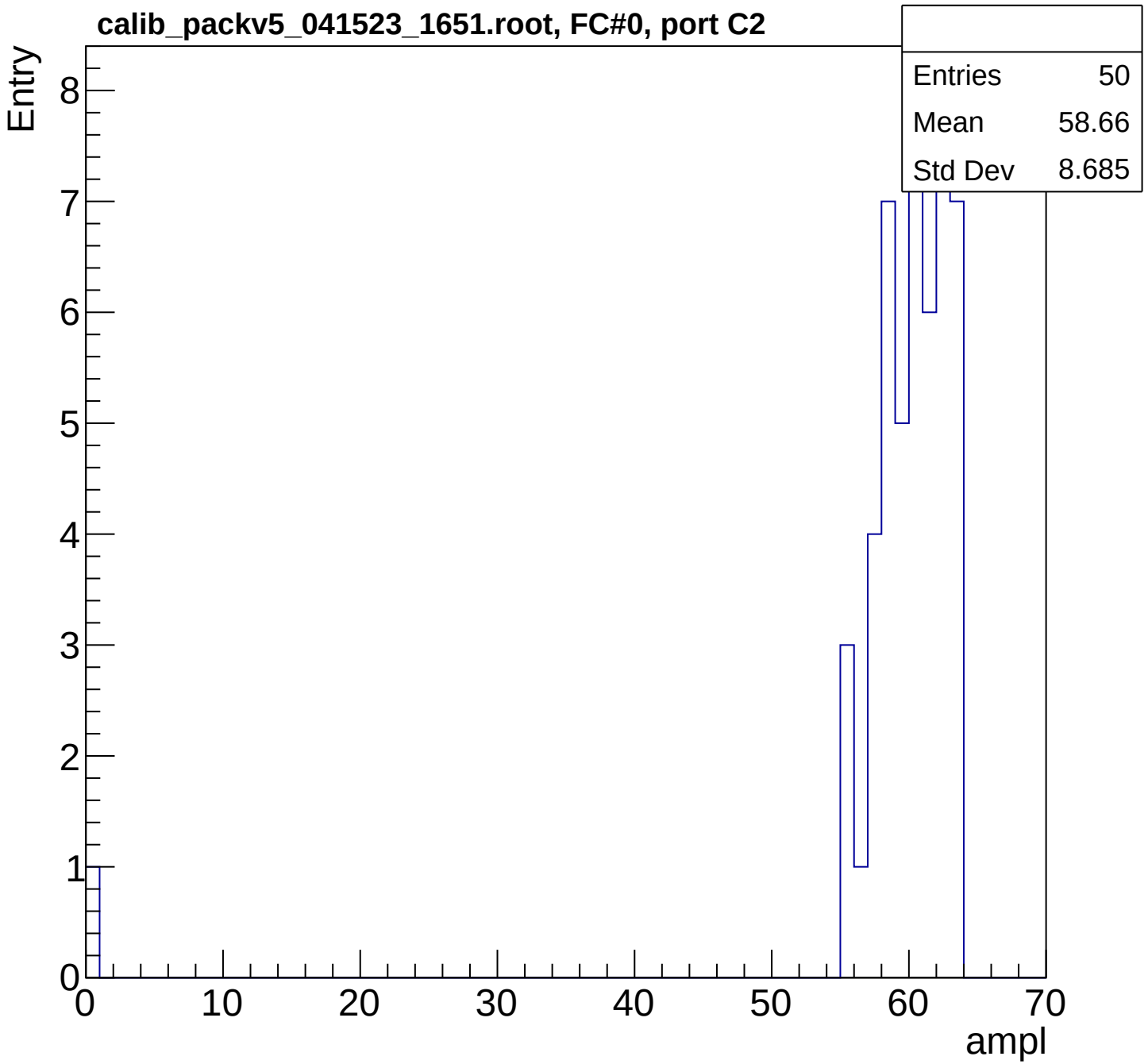
B1L103S, U8-ch41, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 58.66
Std Dev 8.685
Entry
ampl
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0
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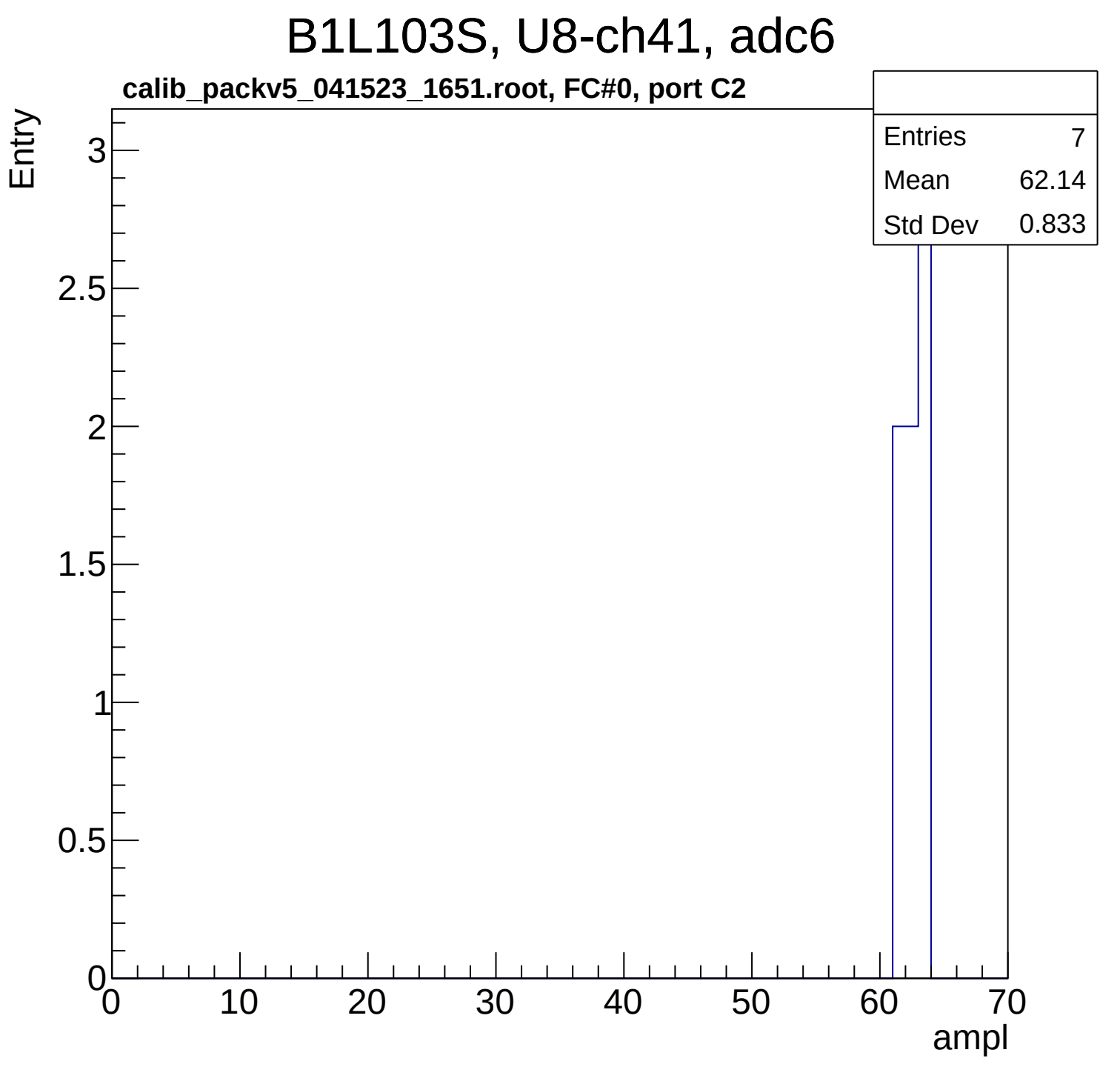
B1L103S, U8-ch41, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 62.14
Std Dev 0.833
Entry
ampl
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0.5
1
1.5
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2.5
3
0
10
20
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40
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60
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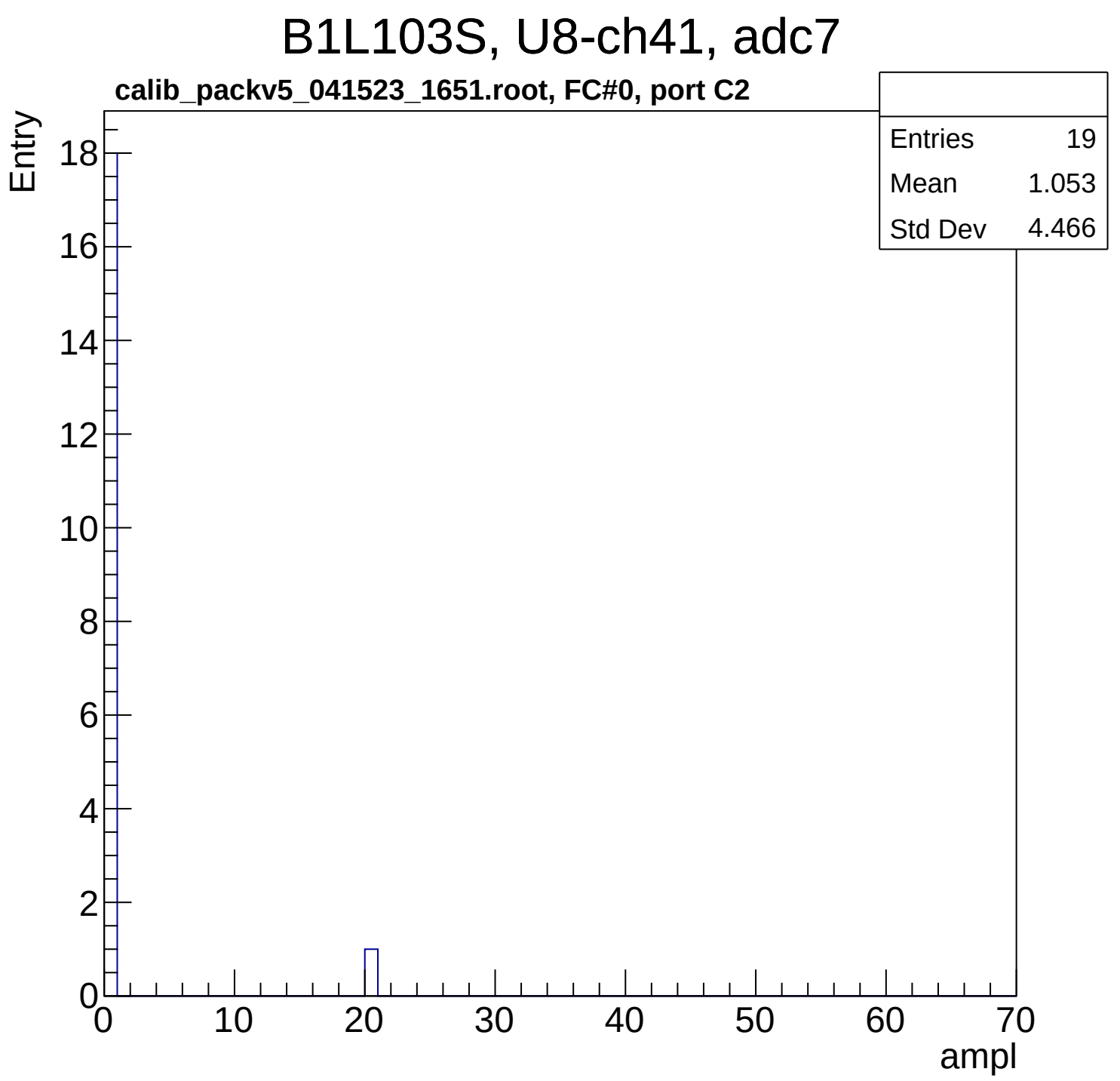
B1L103S, U8-ch41, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.053
Std Dev 4.466
Entry
ampl
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8
10
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0
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60
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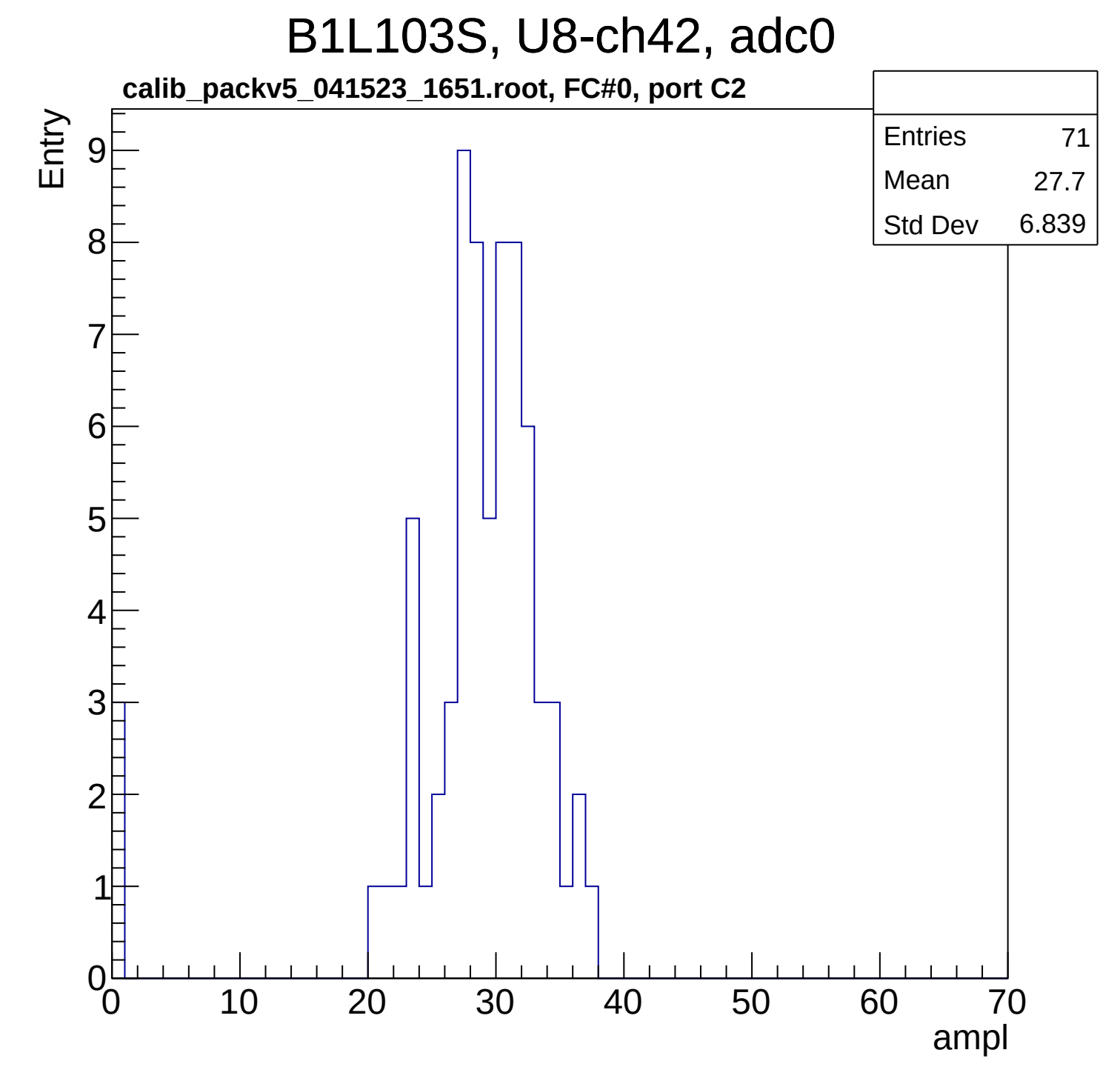
B1L103S, U8-ch42, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 27.7
Std Dev 6.839
Entry
ampl
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6
7
8
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0
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60
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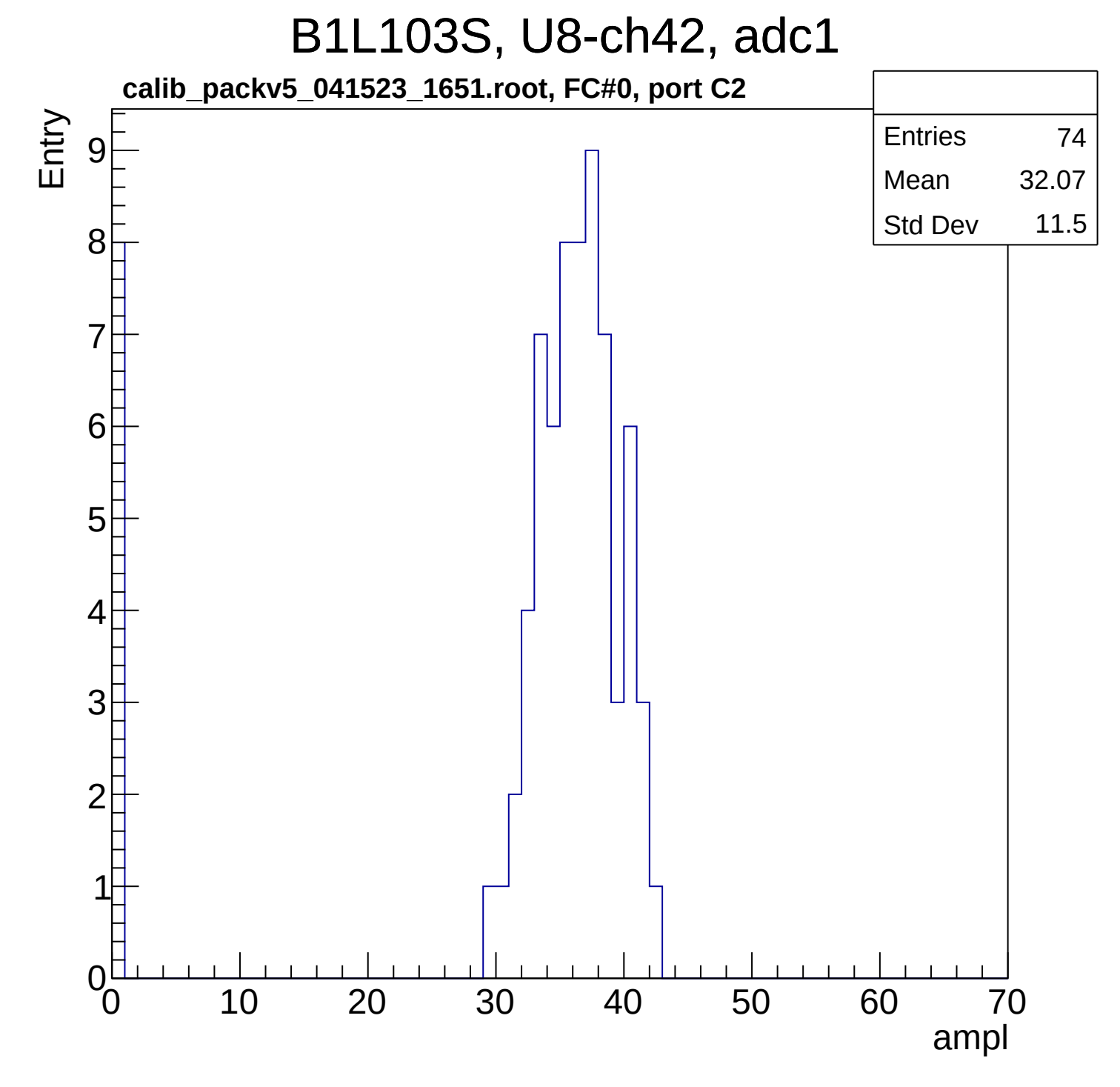
B1L103S, U8-ch42, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 32.07
Std Dev 11.5
Entry
ampl
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5
6
7
8
9
0
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20
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60
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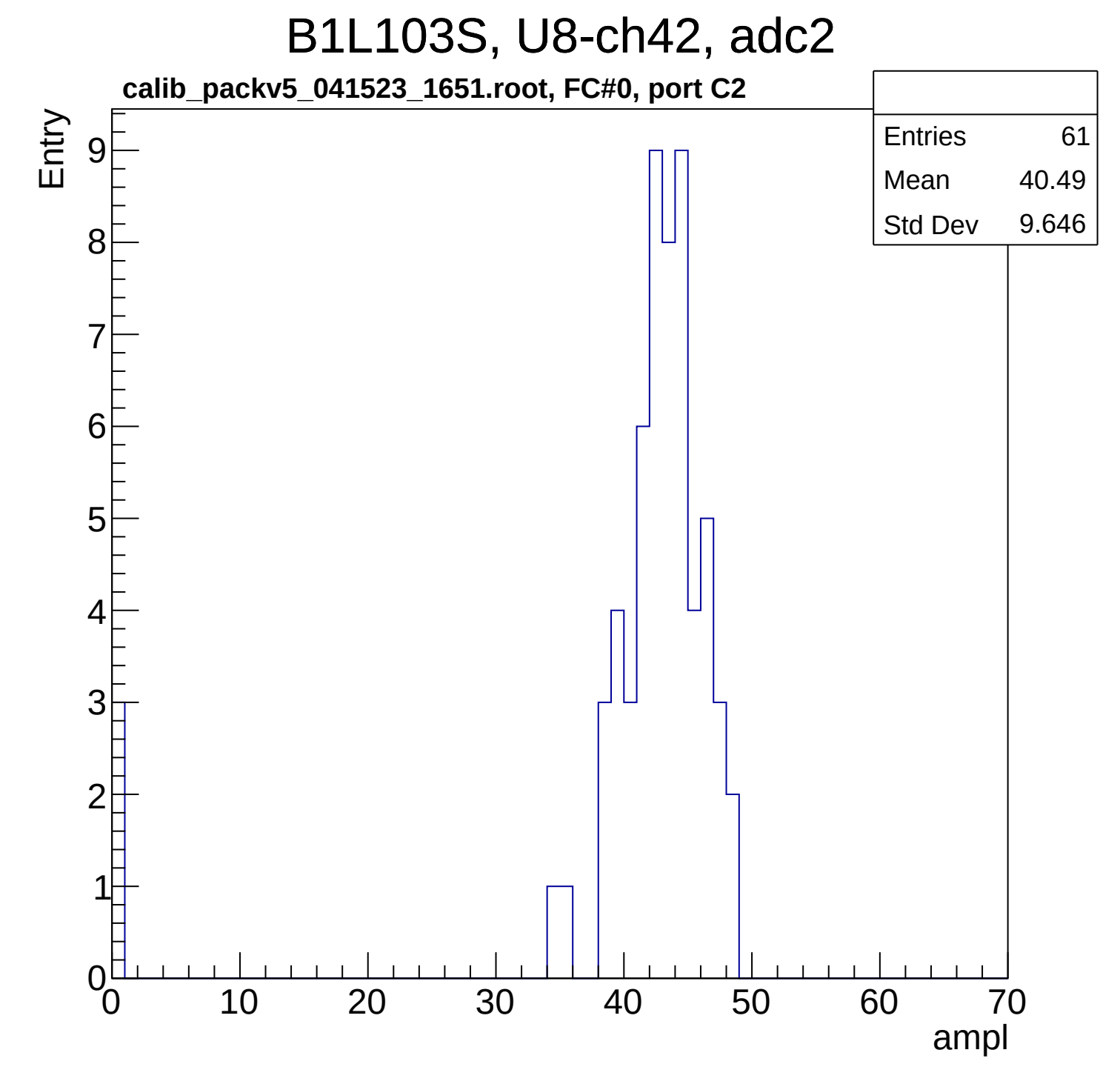
B1L103S, U8-ch42, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 40.49
Std Dev 9.646
Entry
ampl
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3
4
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6
7
8
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0
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60
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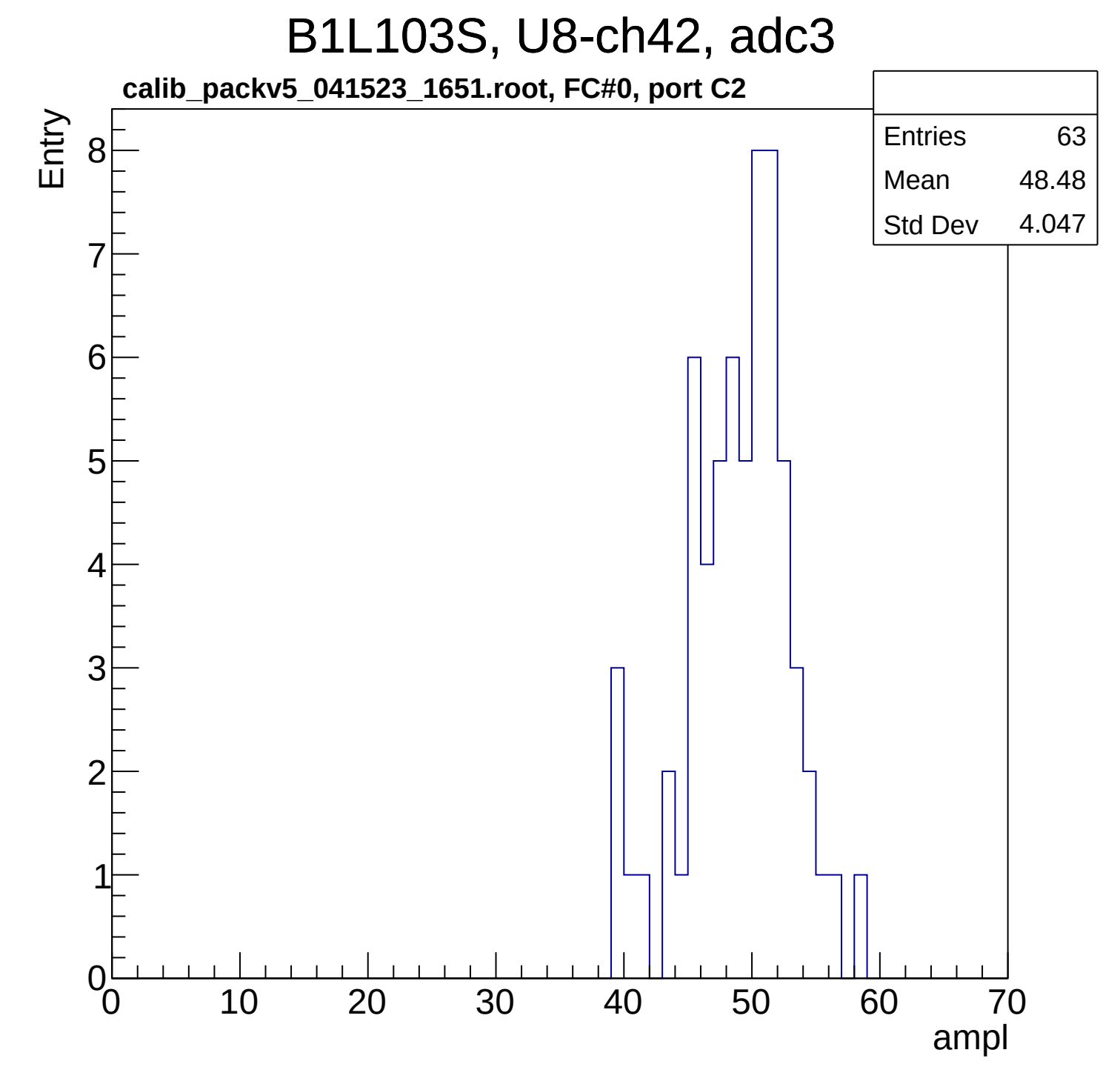
B1L103S, U8-ch42, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 48.48
Std Dev 4.047
Entry
ampl
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5
6
7
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60
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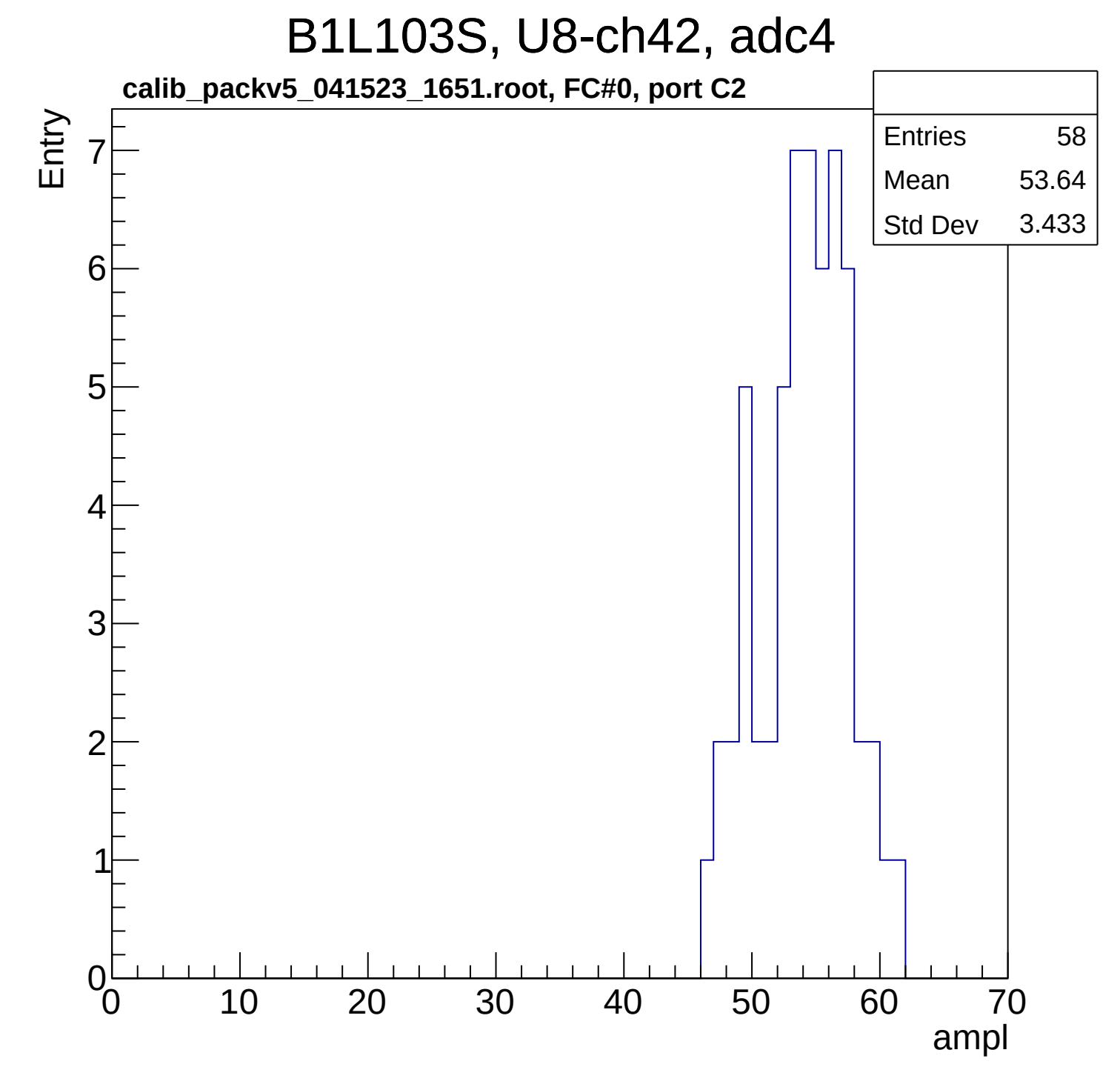
B1L103S, U8-ch42, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 53.64
Std Dev 3.433
Entry
ampl
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0
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20
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60
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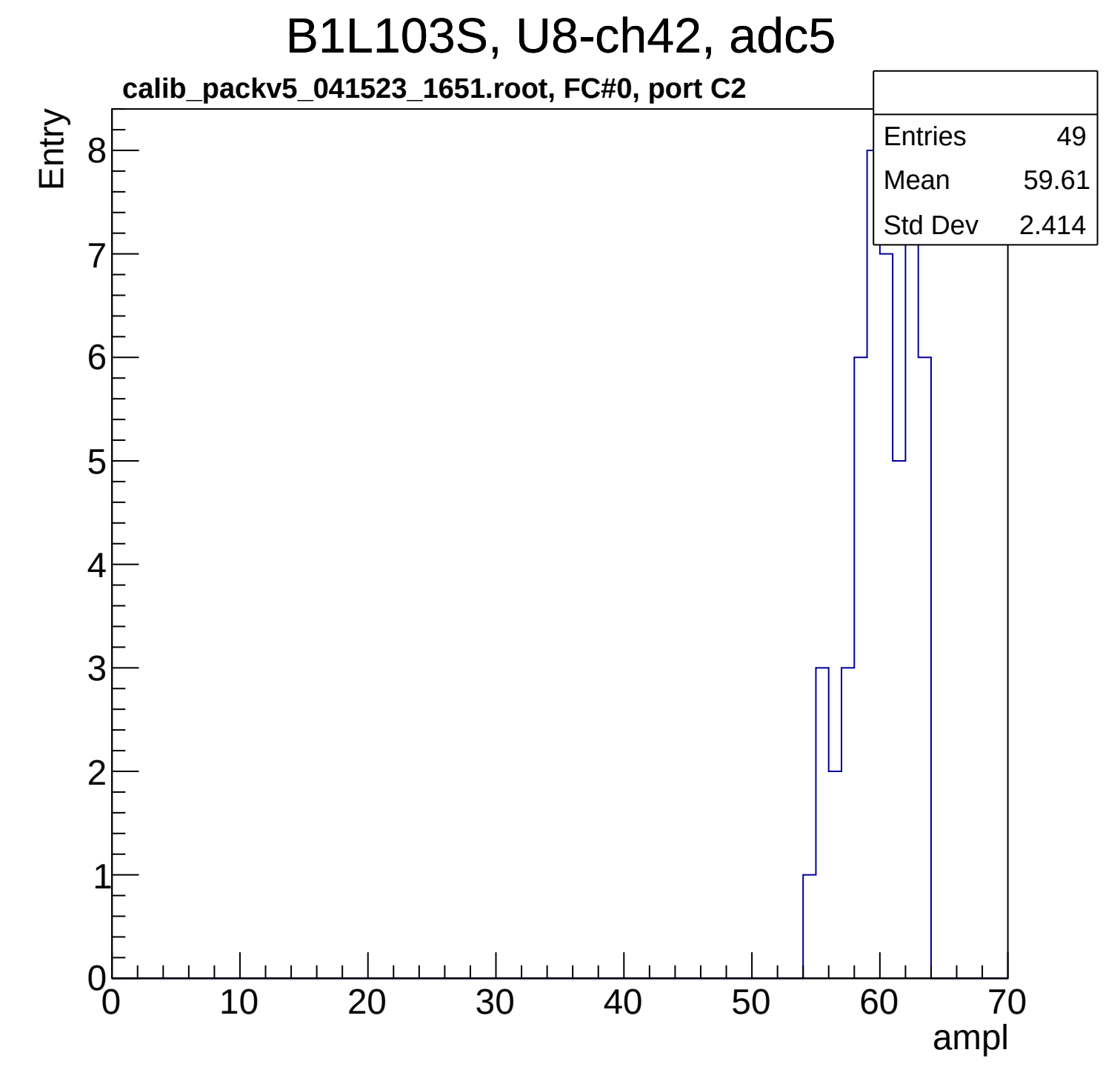
B1L103S, U8-ch42, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 59.61
Std Dev 2.414
Entry
ampl
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6
7
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0
10
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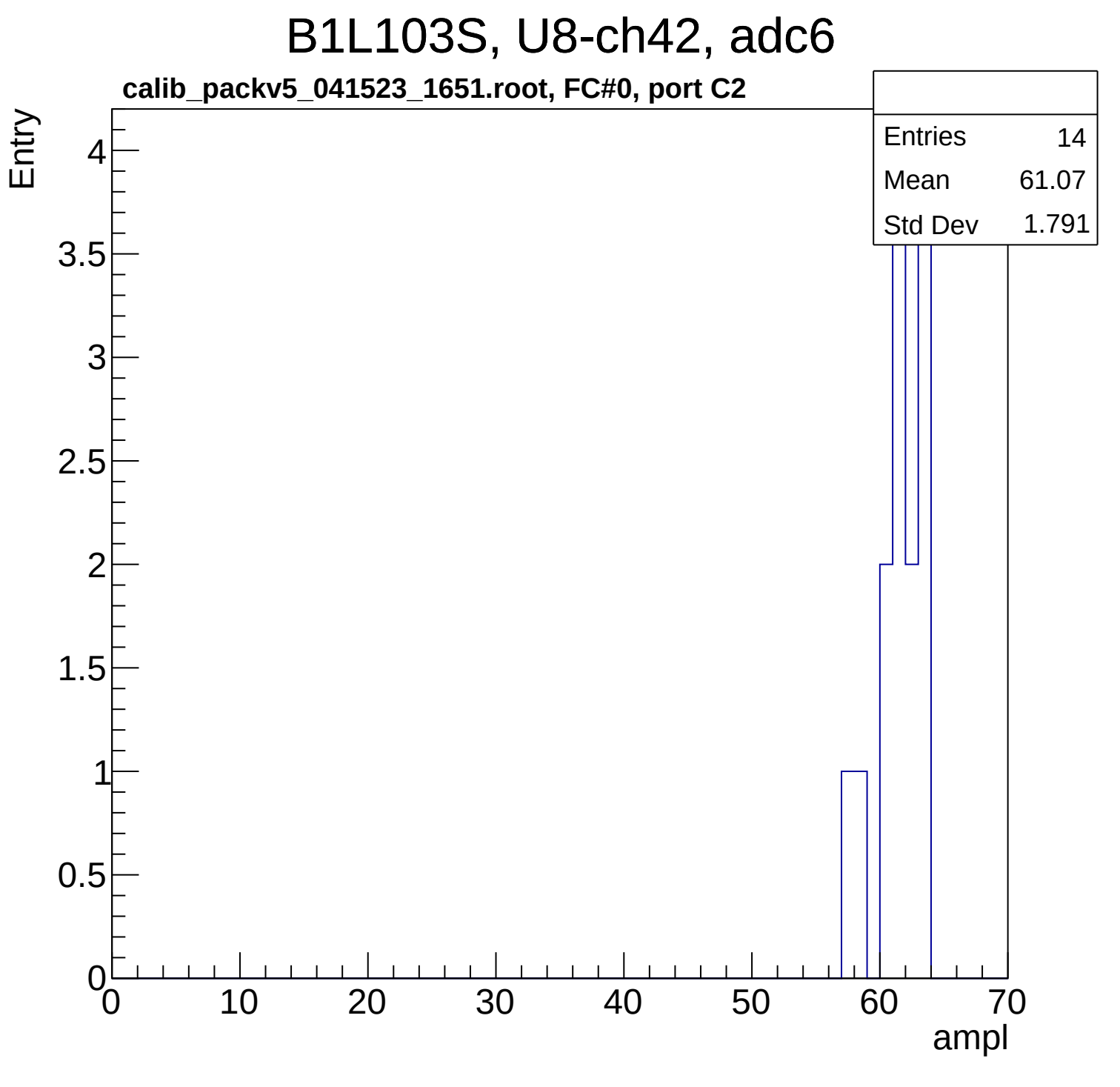
60
70


B1L103S, U8-ch42, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 61.07
Std Dev 1.791
Entry
ampl
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1.5
2
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3
3.5
4
0
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40
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60
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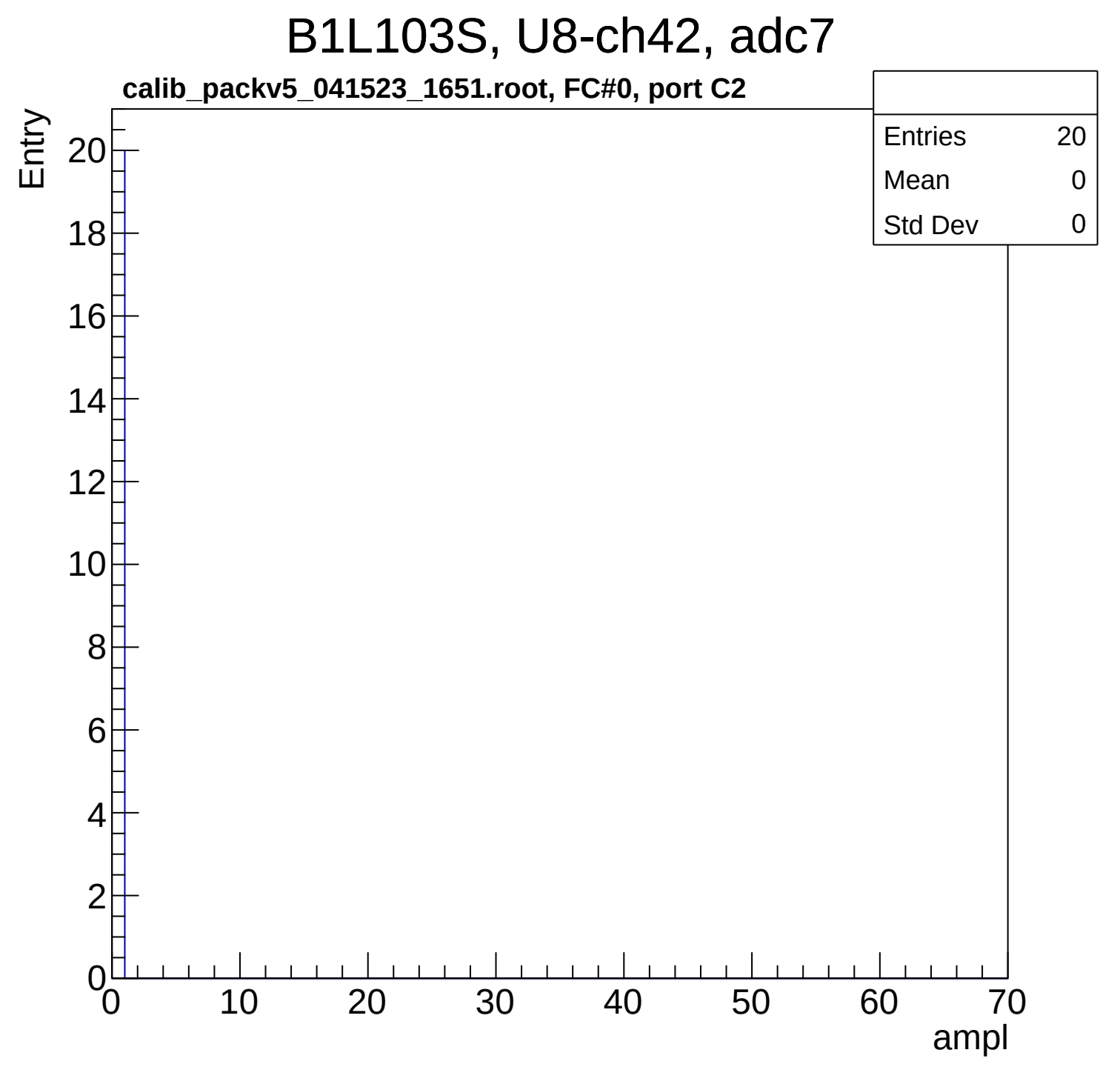
B1L103S, U8-ch42, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 0
Std Dev 0
Entry
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8
10
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18
20
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10
20
30
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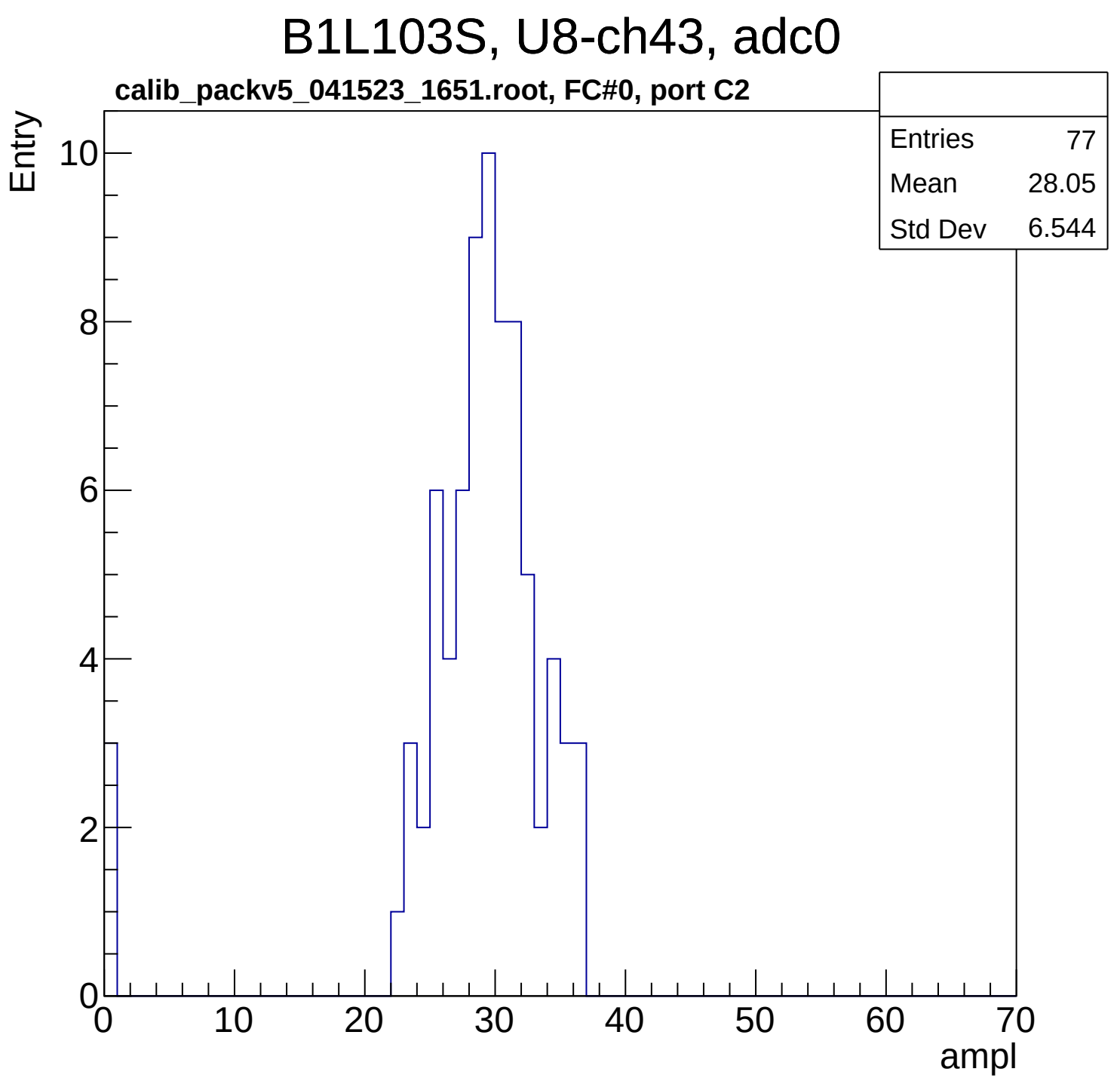
50
60
70
ampl


B1L103S, U8-ch43, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 28.05
Std Dev 6.544
Entry
ampl
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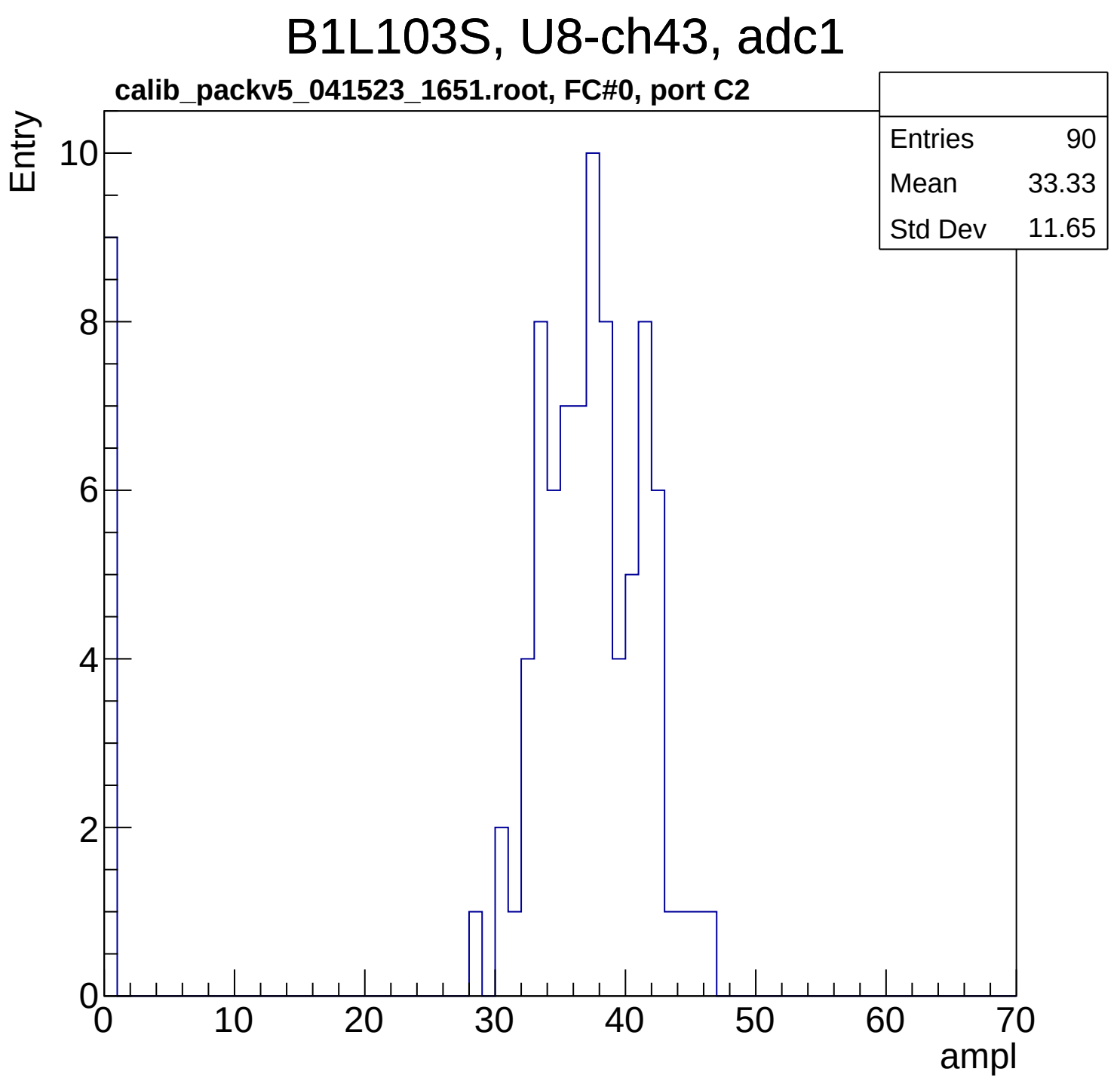
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U8-ch43, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 33.33
Std Dev 11.65
Entry
ampl
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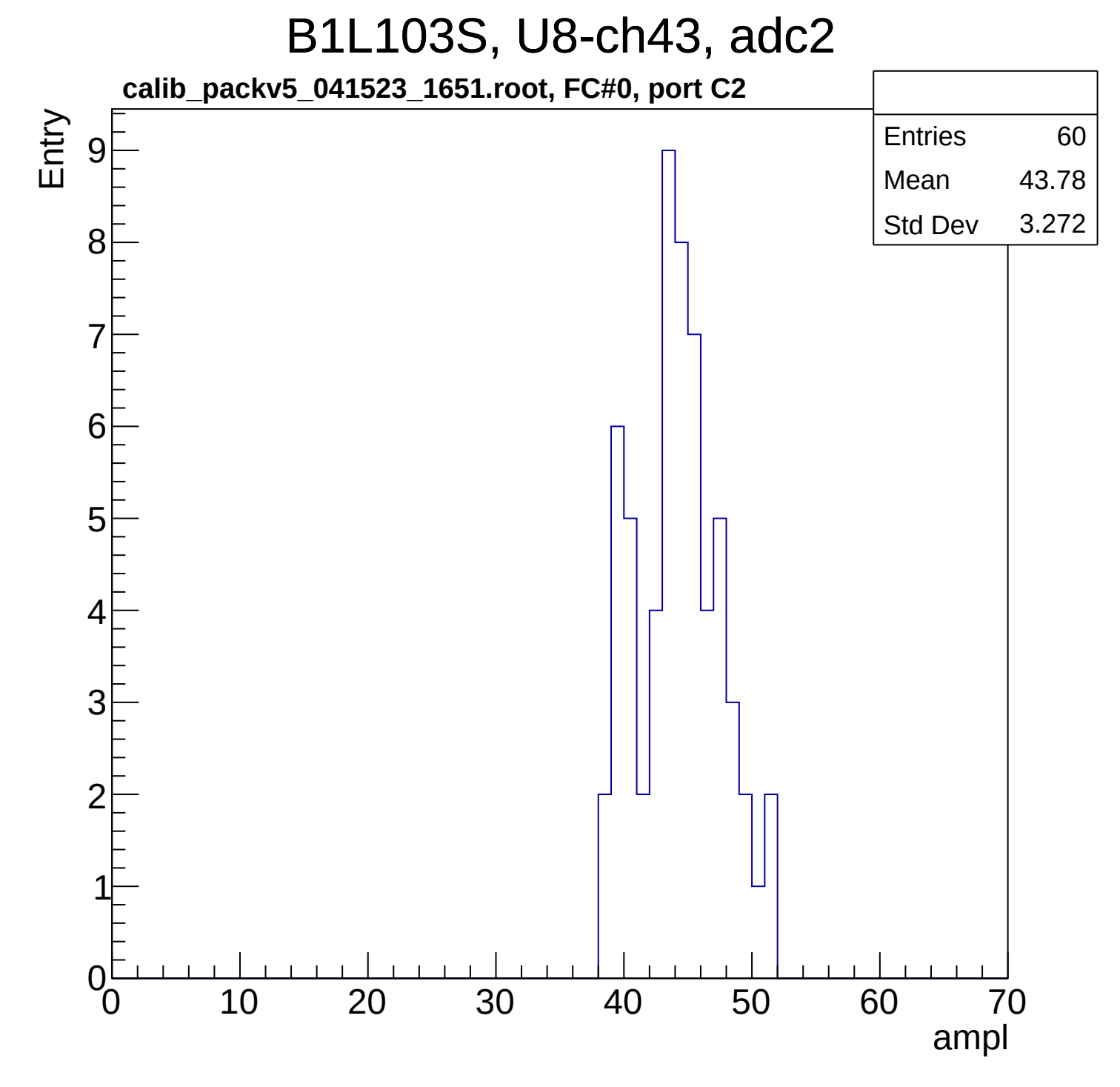
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U8-ch43, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 43.78
Std Dev 3.272
Entry
ampl
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6
7
8
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50
60
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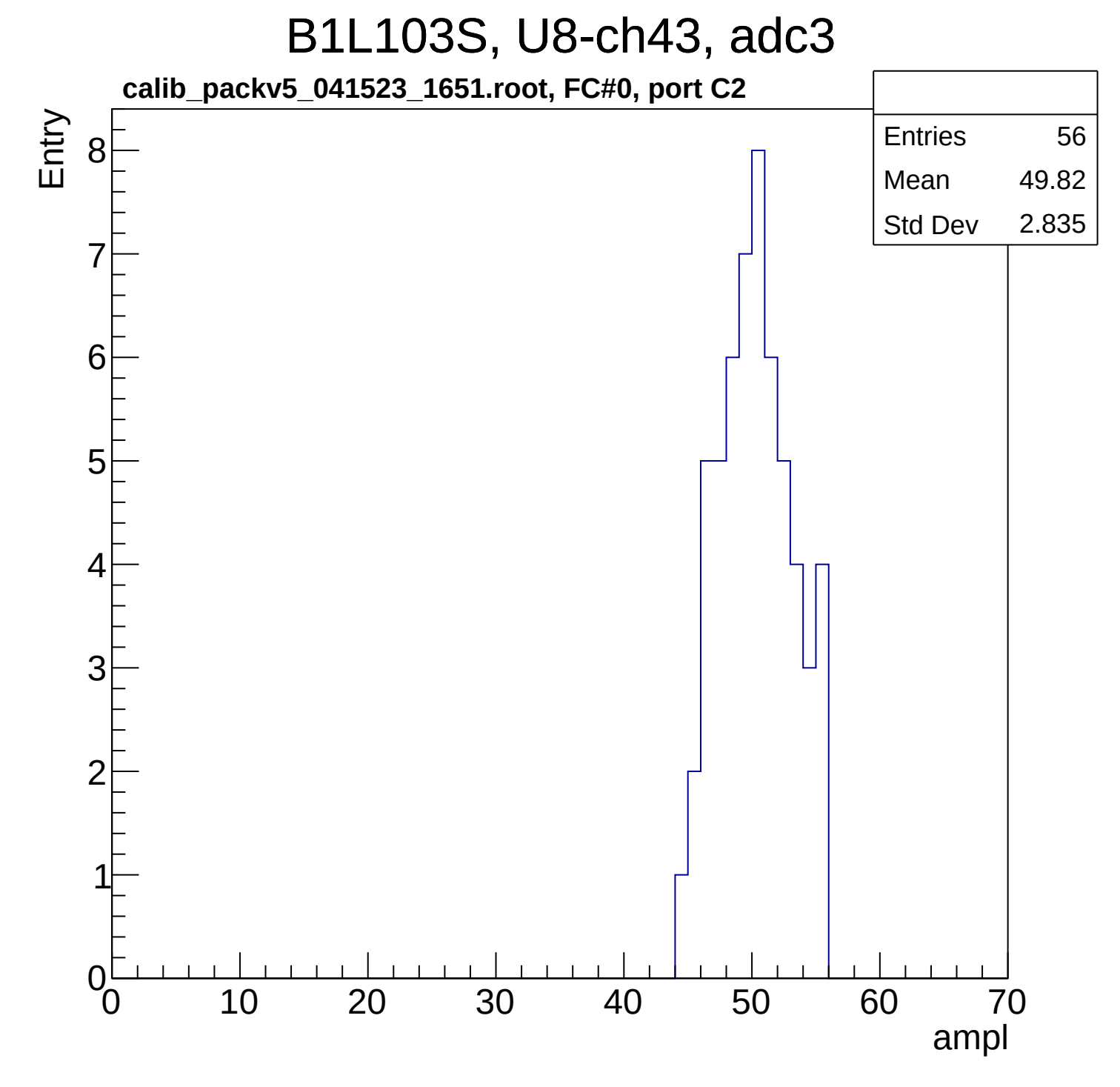
B1L103S, U8-ch43, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 49.82
Std Dev 2.835
Entry
ampl
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5
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7
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0
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40
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60
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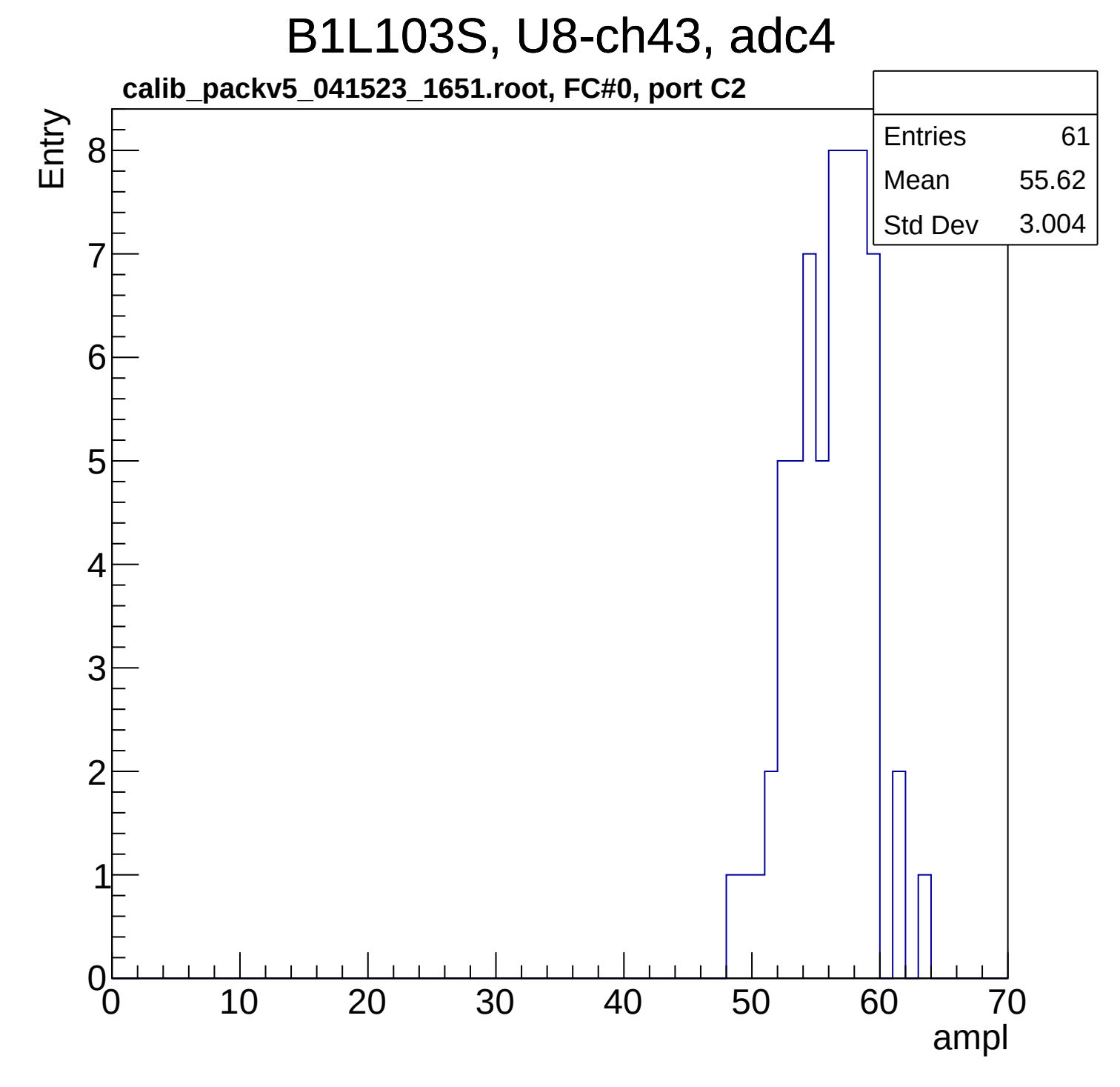
B1L103S, U8-ch43, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 55.62
Std Dev 3.004
Entry
ampl
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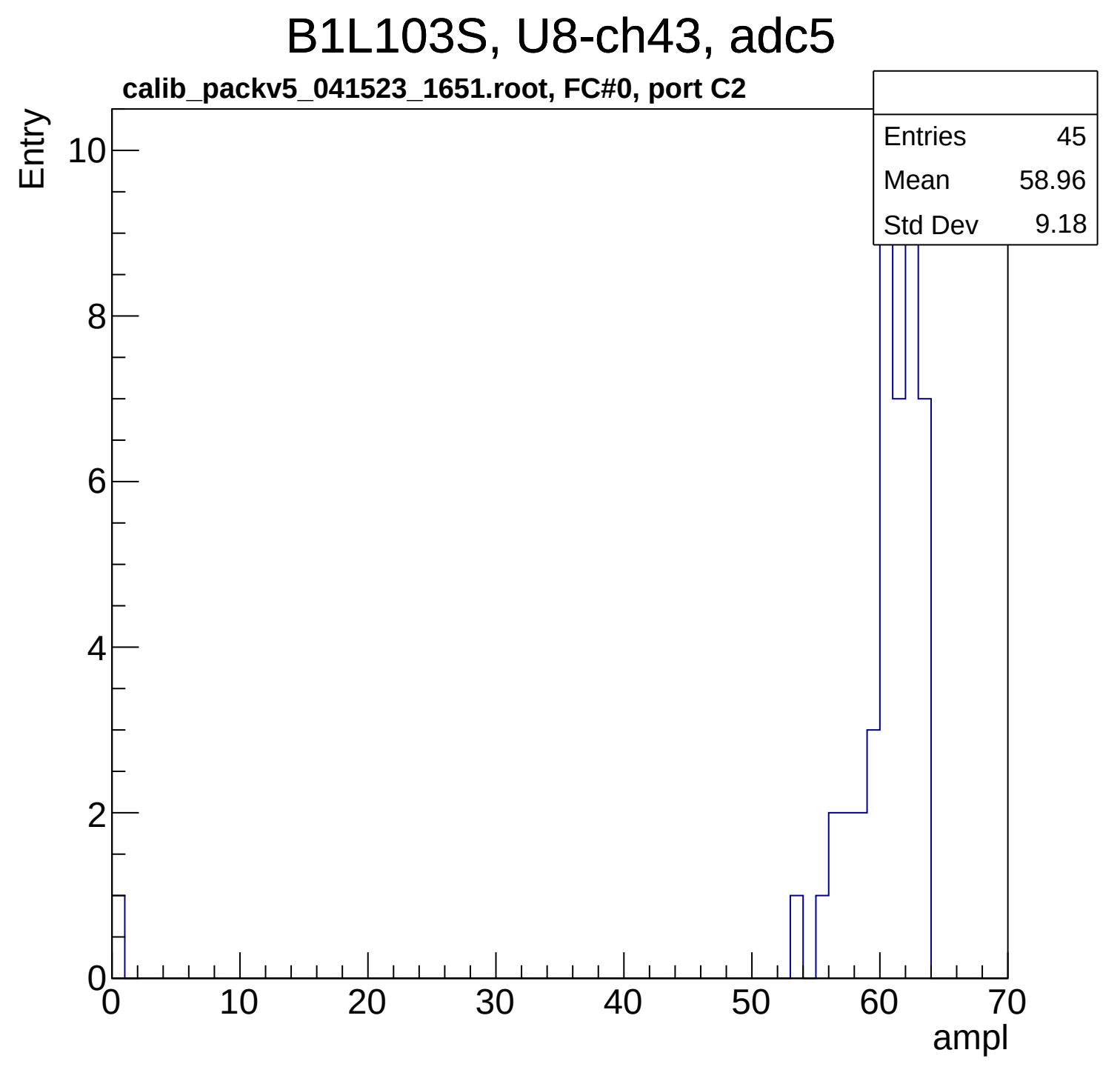
B1L103S, U8-ch43, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 58.96
Std Dev 9.18
Entry
ampl
0
2
4
6
8
10
0
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20
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40
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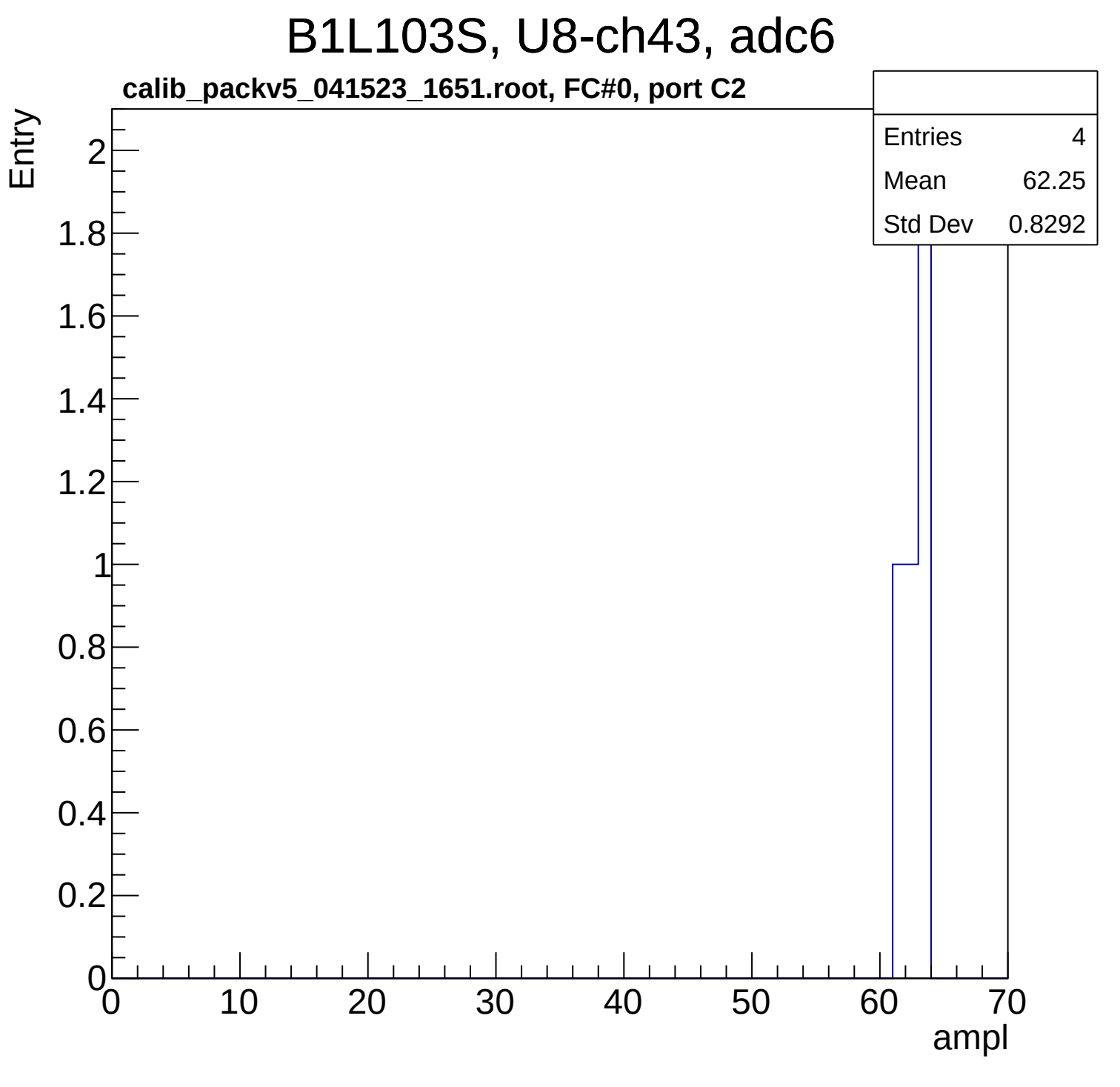
60
70


B1L103S, U8-ch43, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 62.25
Std Dev 0.8292
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
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40
50
60
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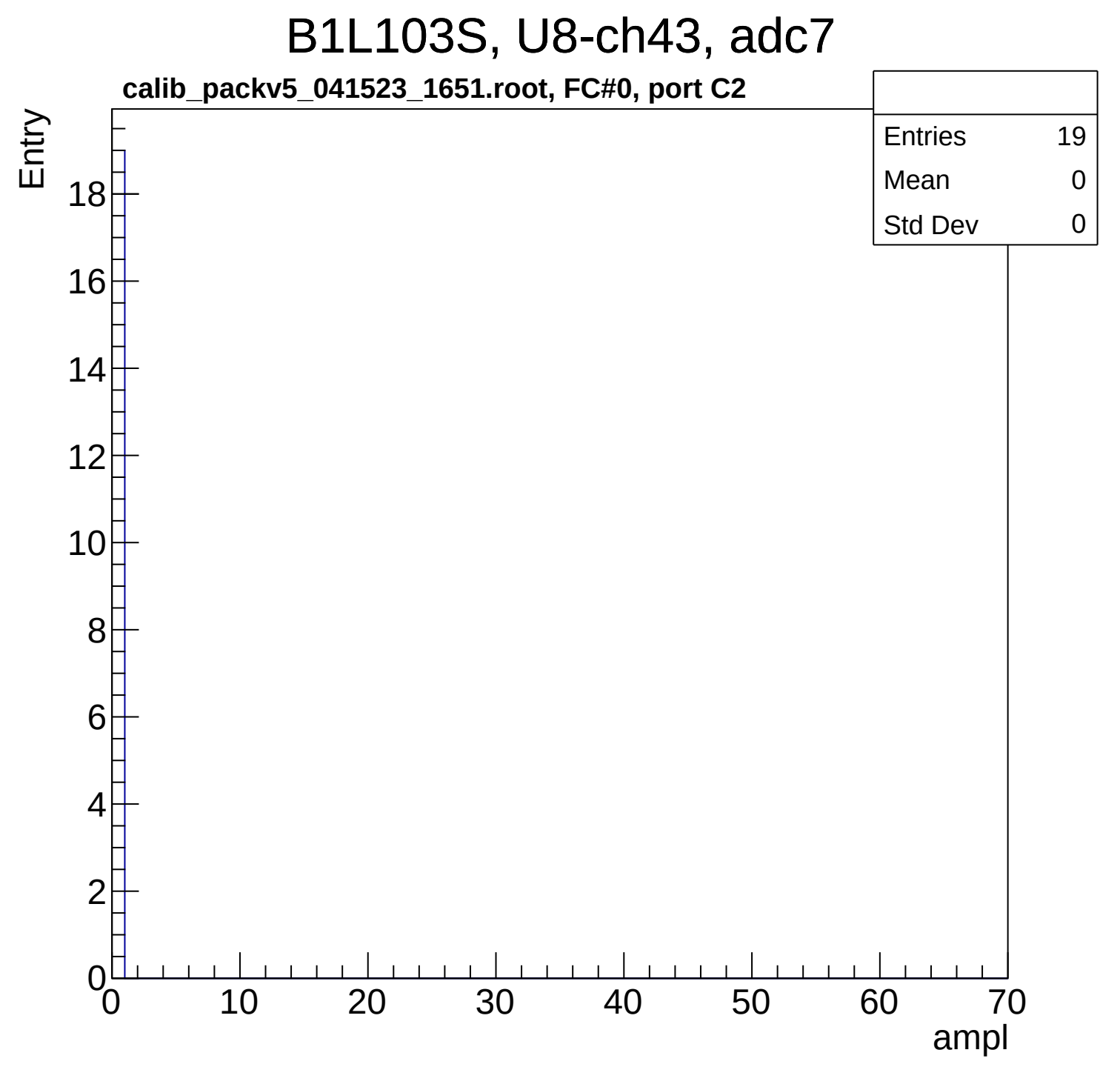
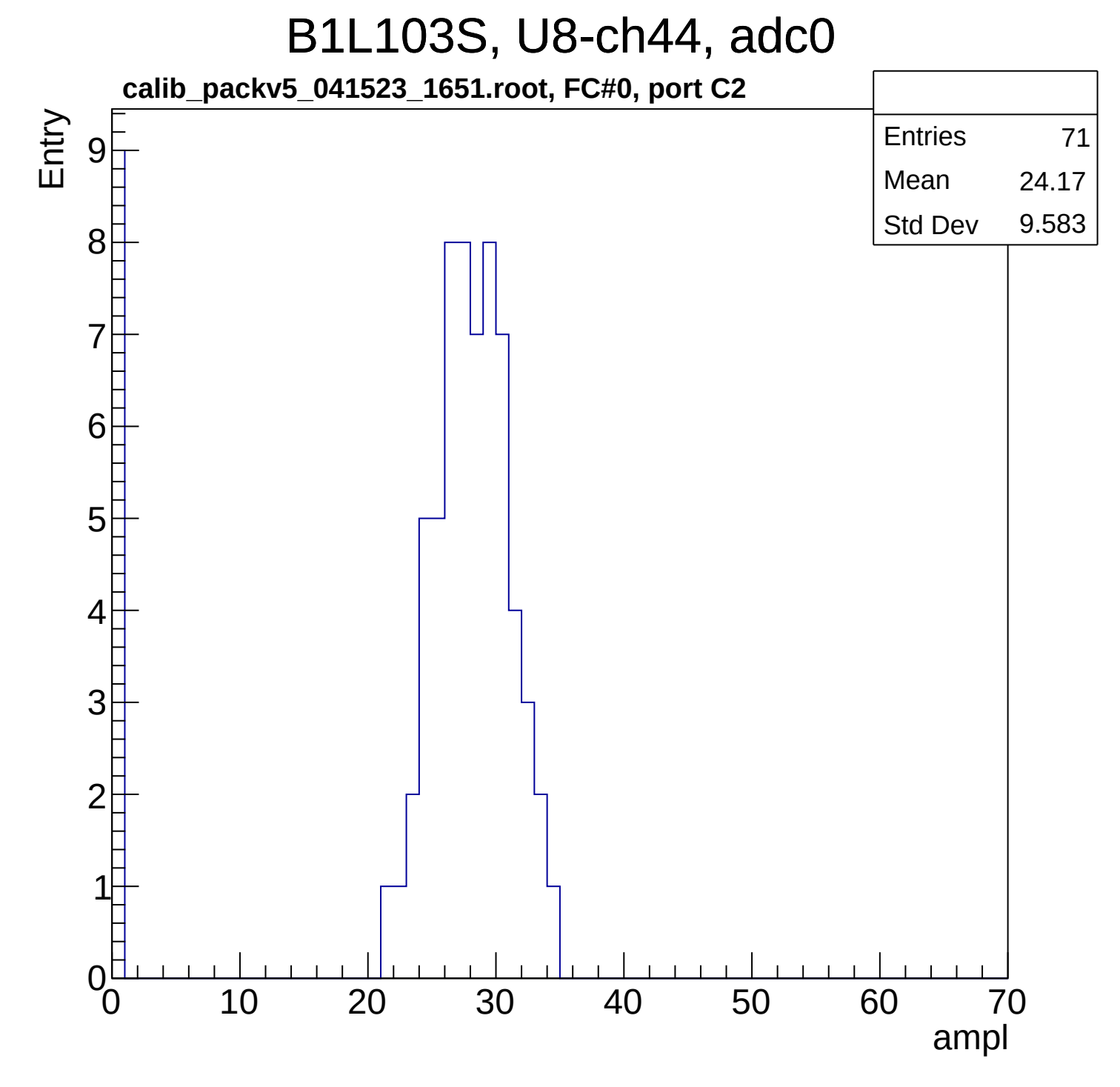

B1L103S, U8-ch43, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch44, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 24.17
Std Dev 9.583
Entry
ampl
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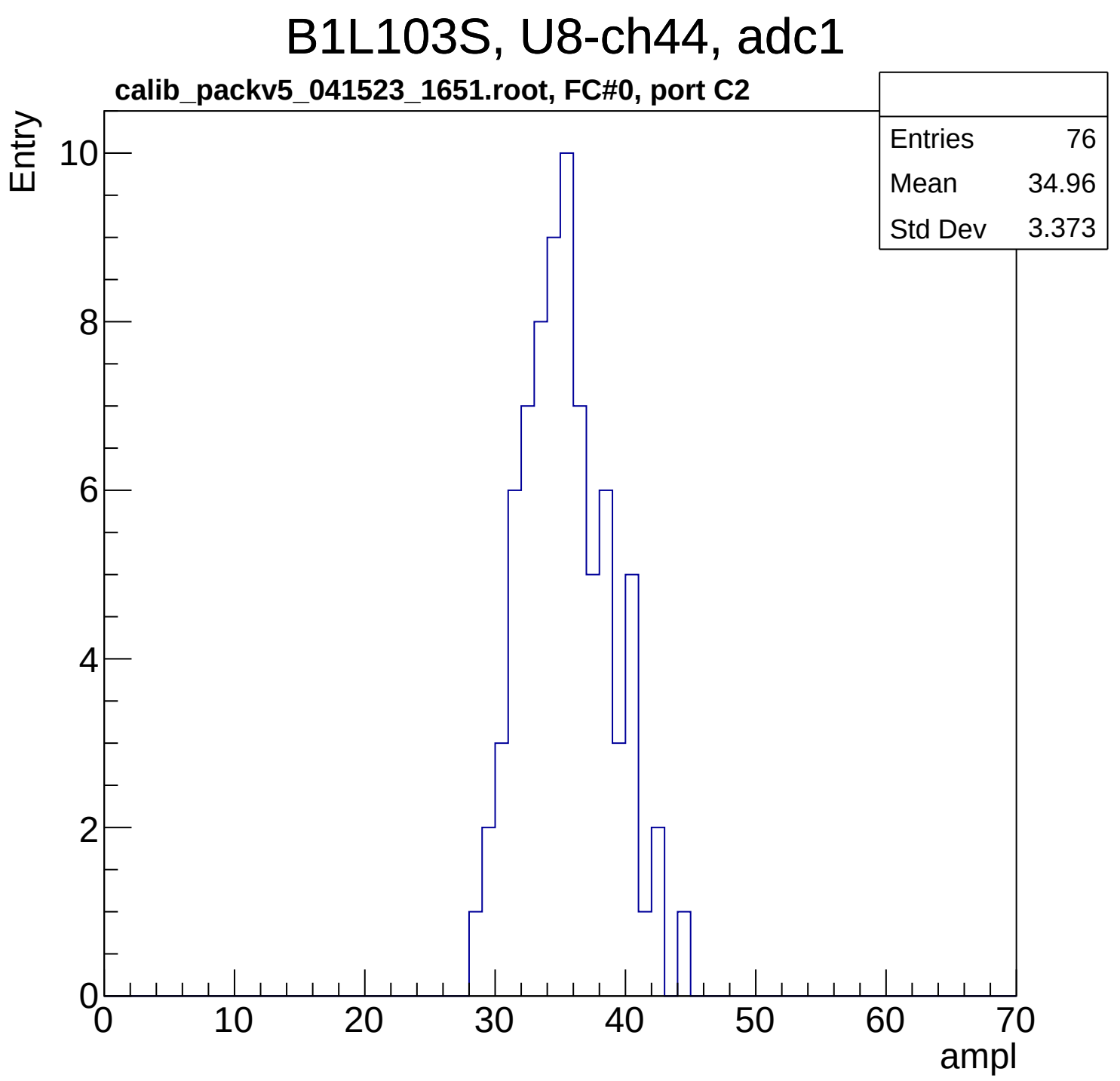
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U8-ch44, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 34.96
Std Dev 3.373
Entry
ampl
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2
4
6
8
10
0
10
20
30
40
50
60
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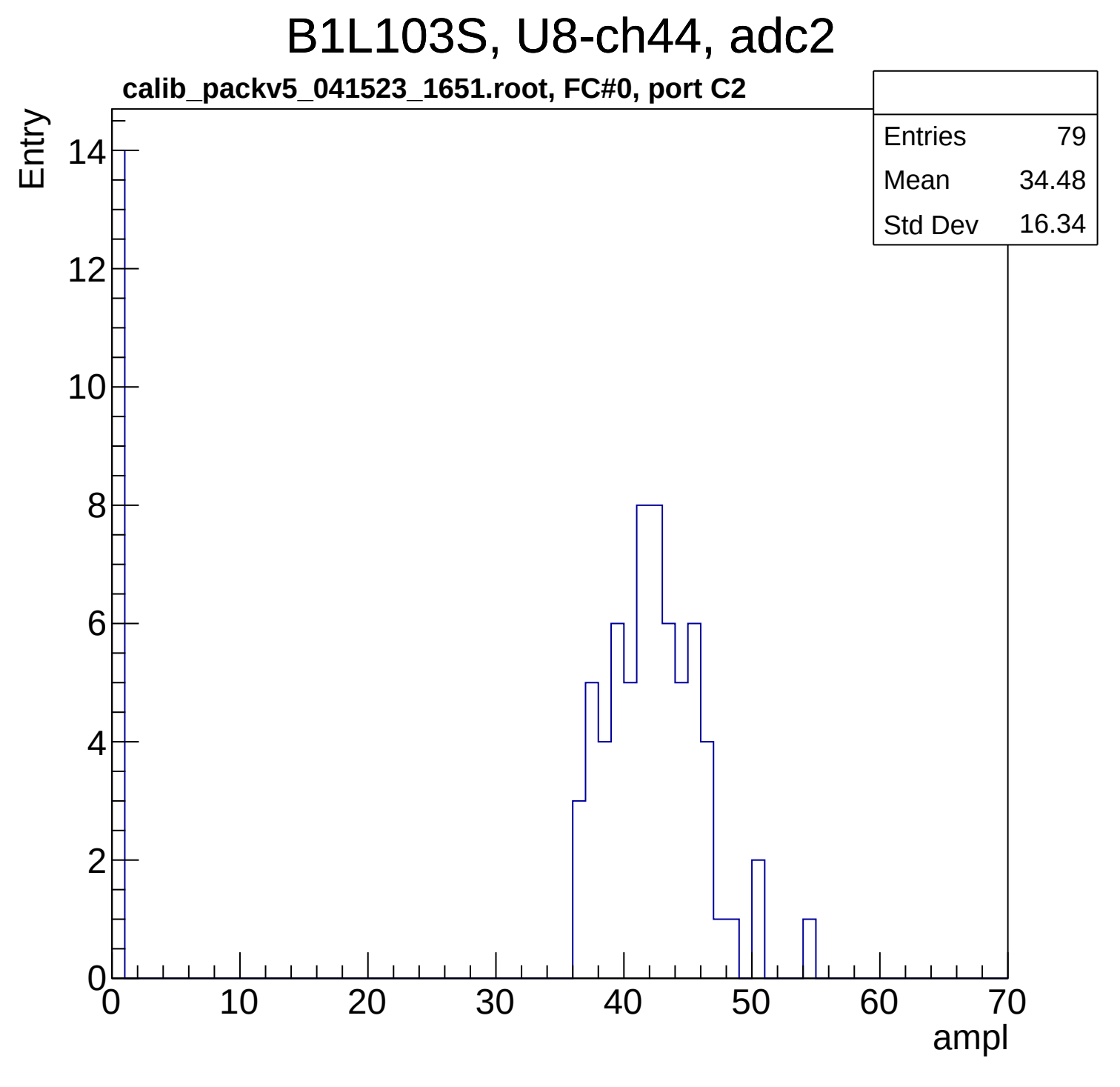
B1L103S, U8-ch44, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 34.48
Std Dev 16.34
Entry
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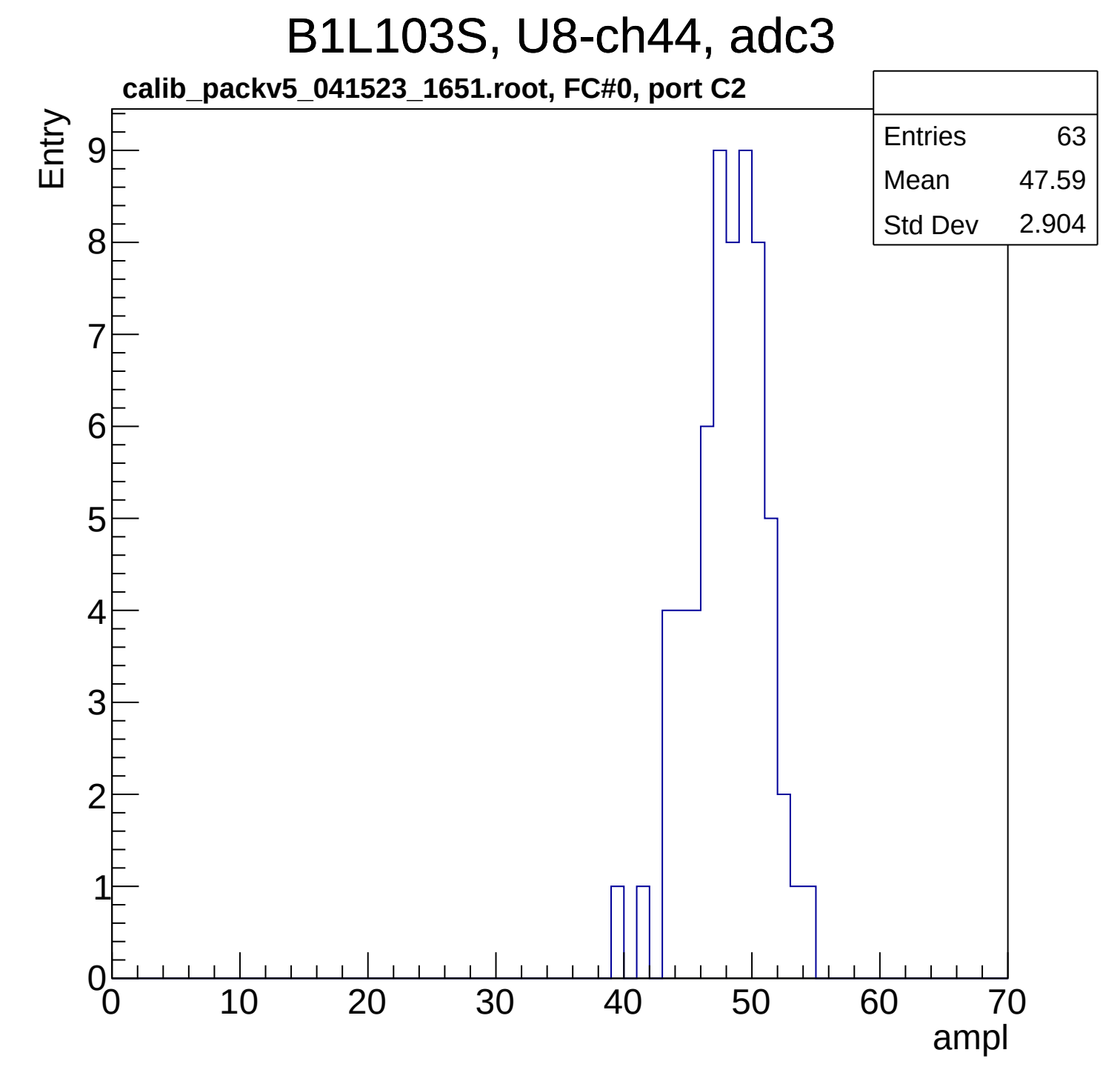
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch44, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 47.59
Std Dev 2.904
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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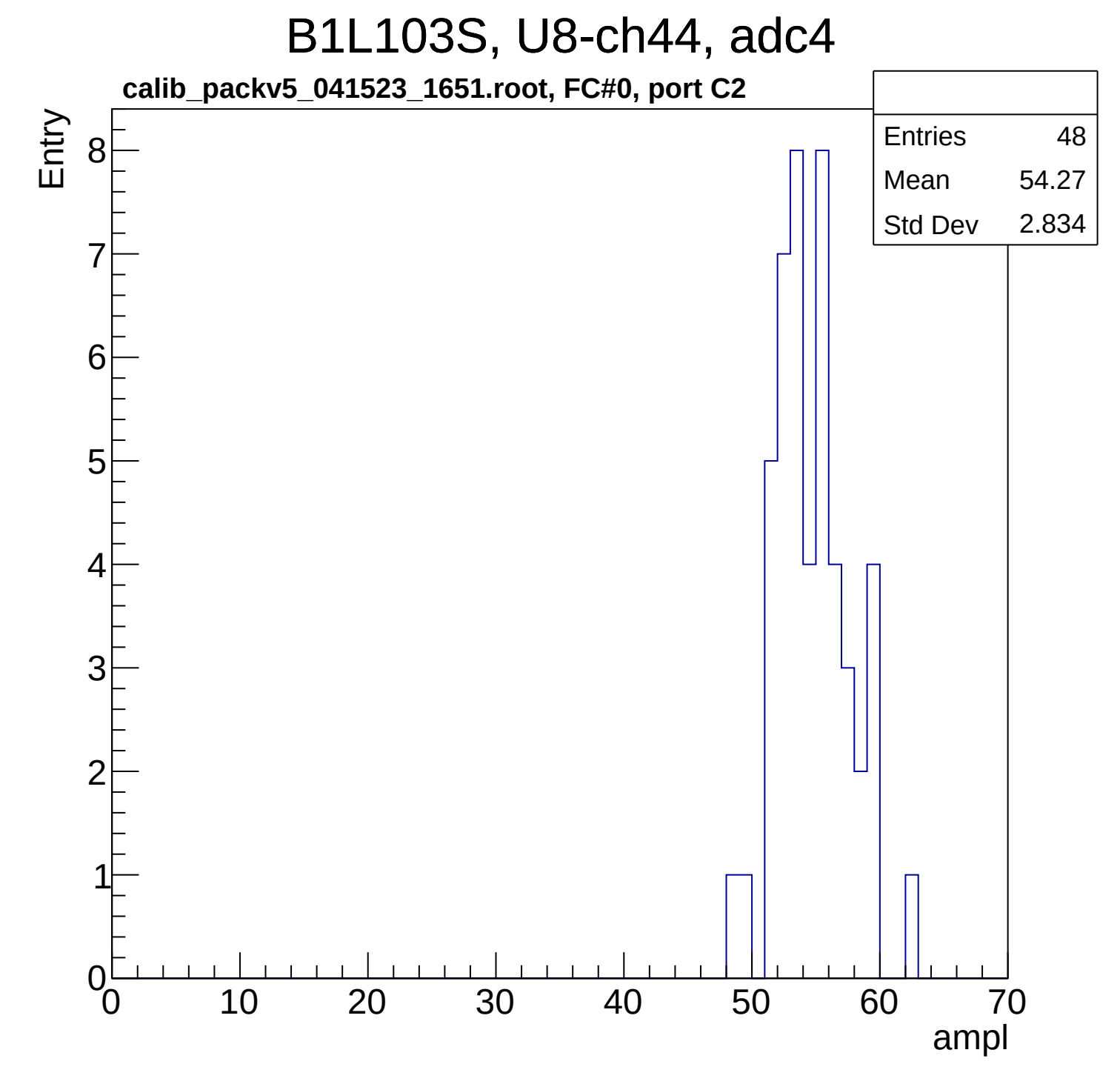
B1L103S, U8-ch44, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 54.27
Std Dev 2.834
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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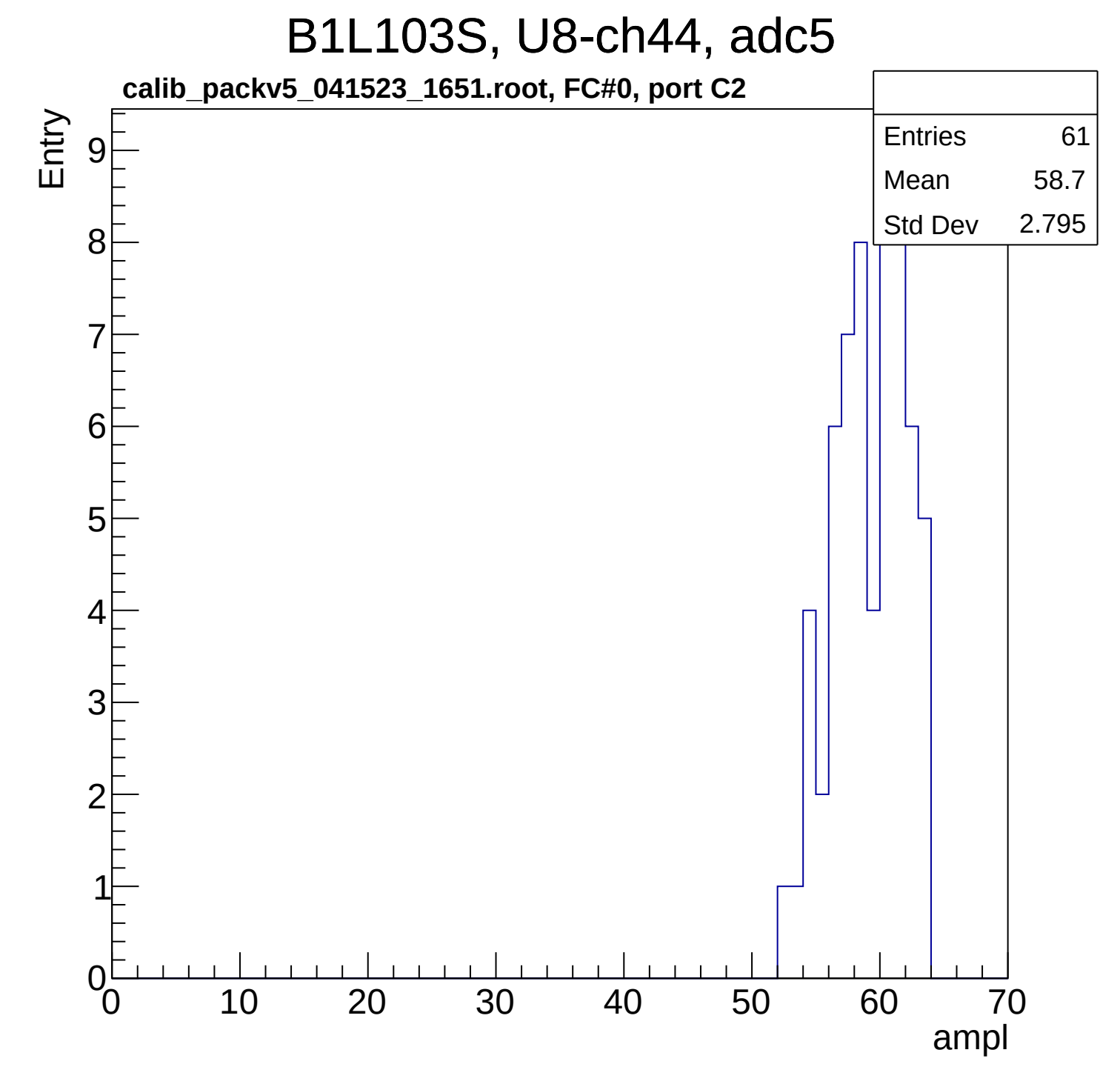
B1L103S, U8-ch44, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 58.7
Std Dev 2.795
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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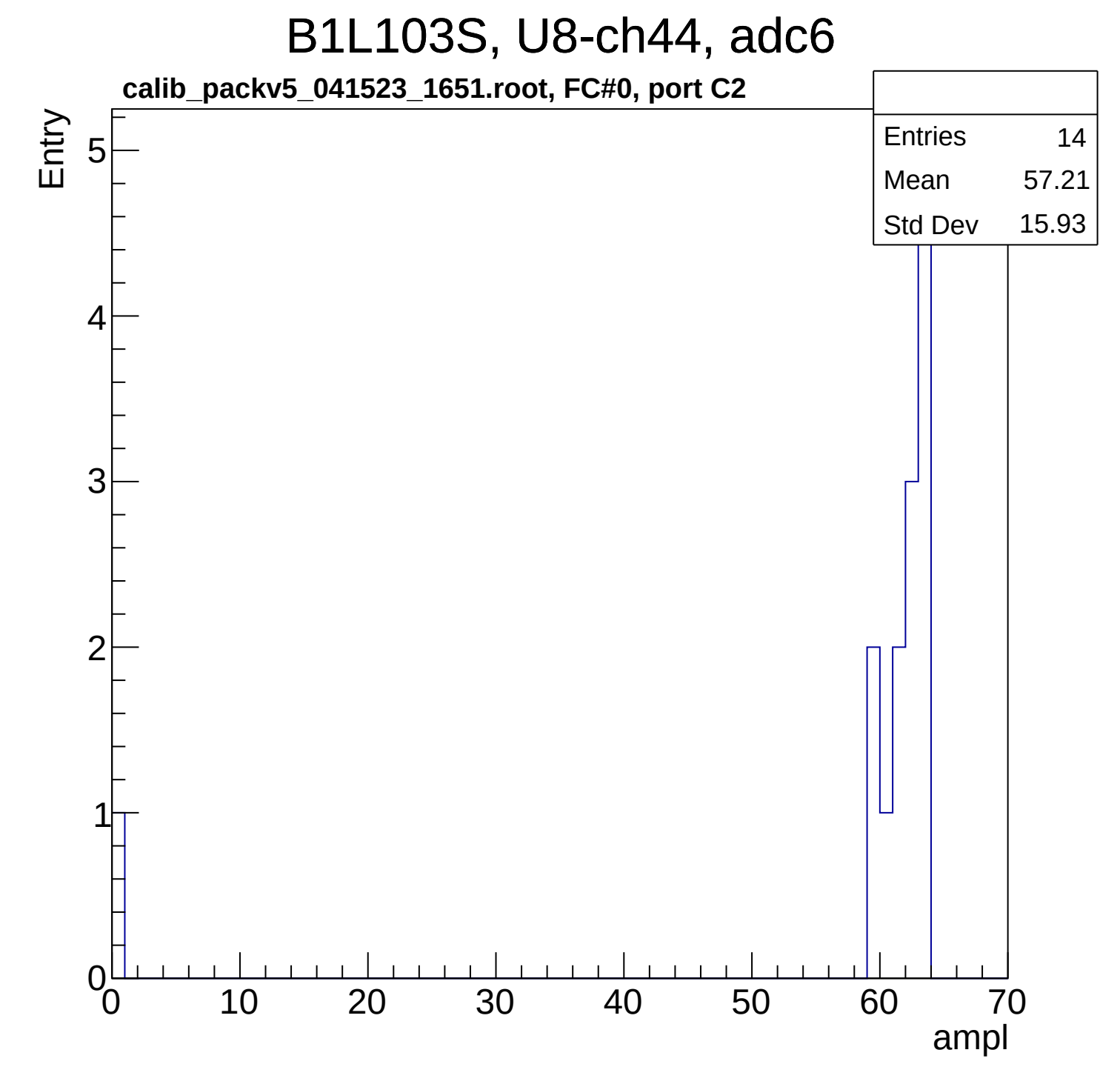
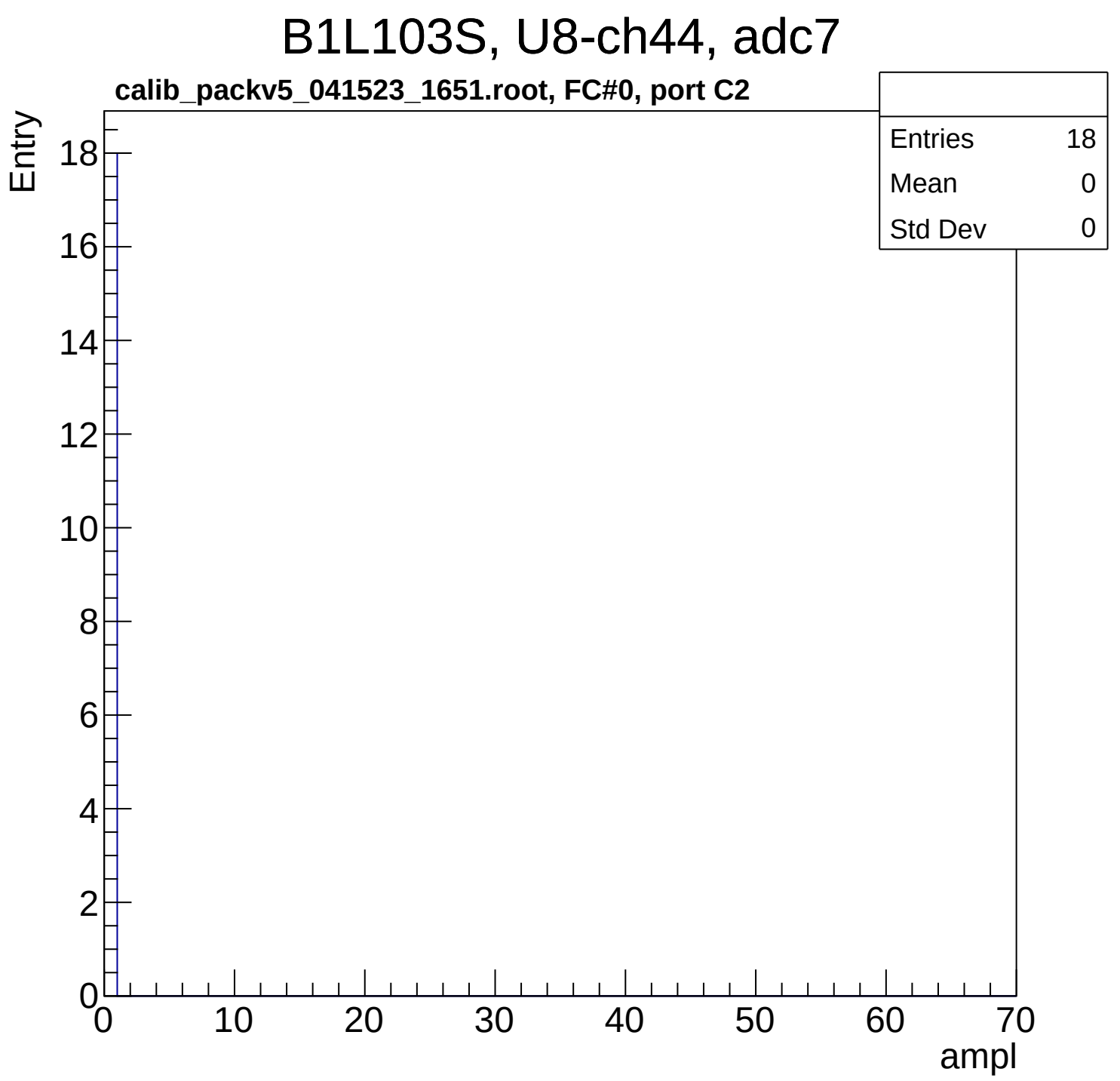
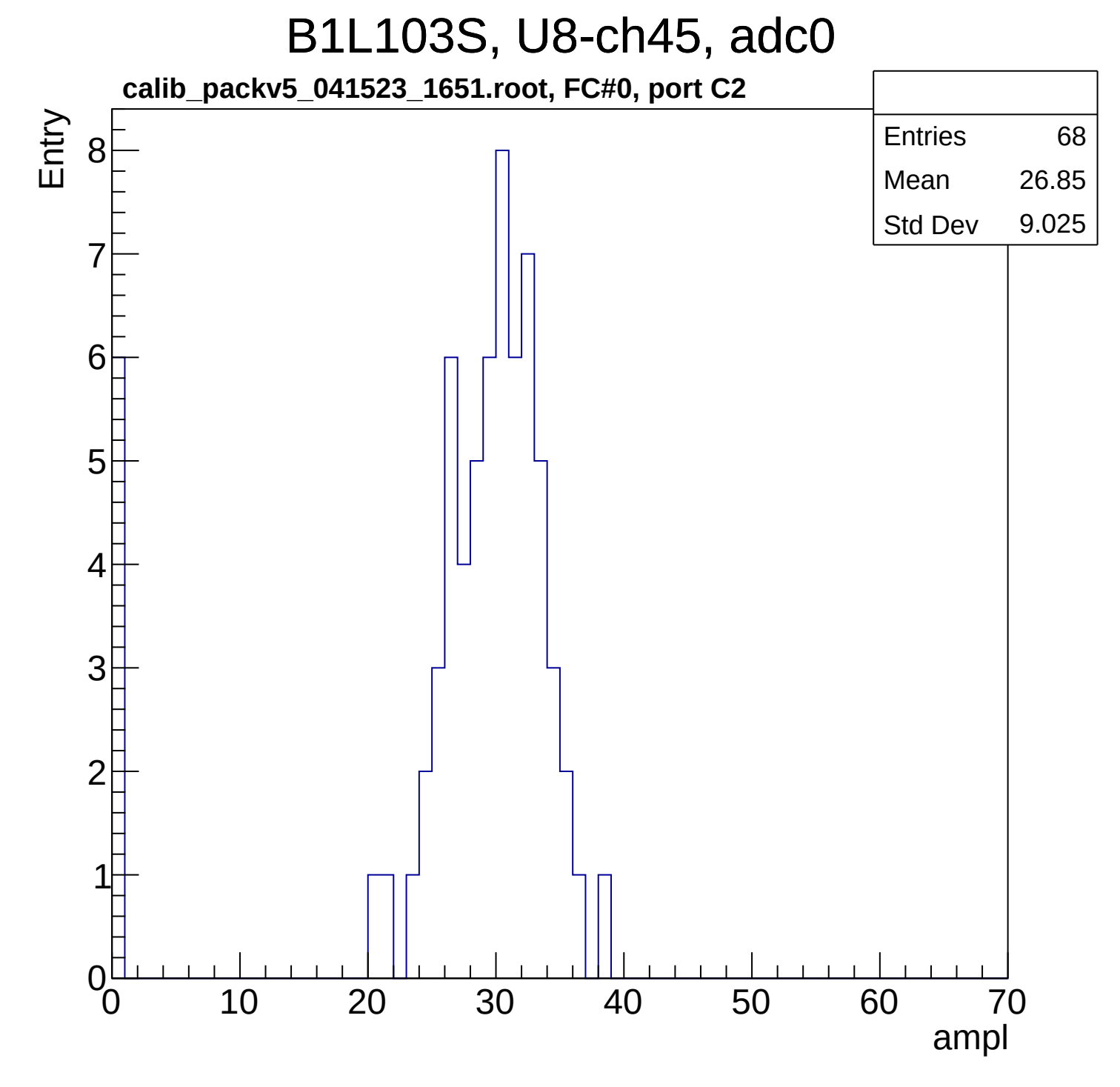
20
30
40
50
60
70


B1L103S, U8-ch44, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 57.21
Std Dev 15.93
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U8-ch44, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch45, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 26.85
Std Dev 9.025
Entry
ampl
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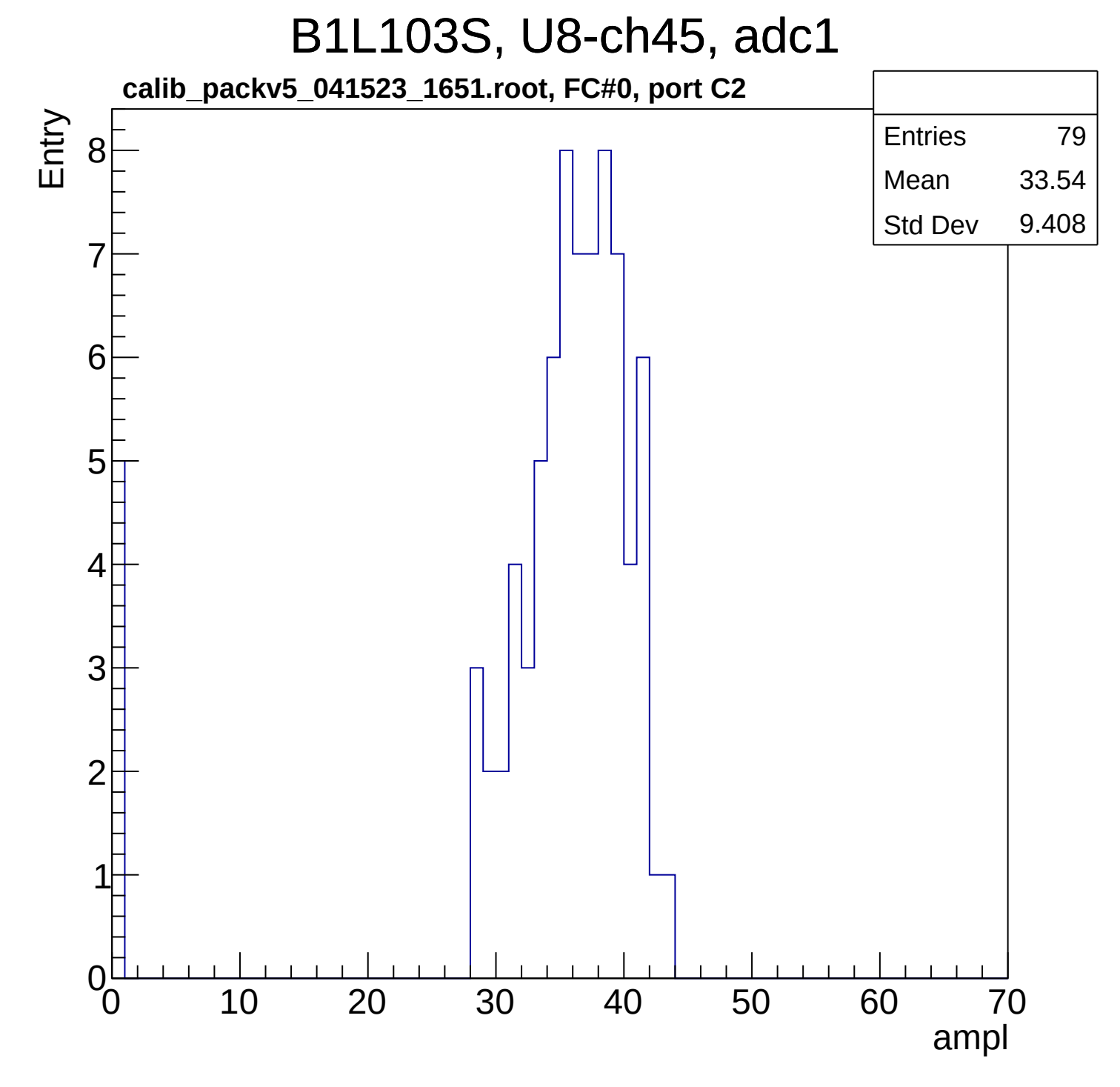
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch45, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 33.54
Std Dev 9.408
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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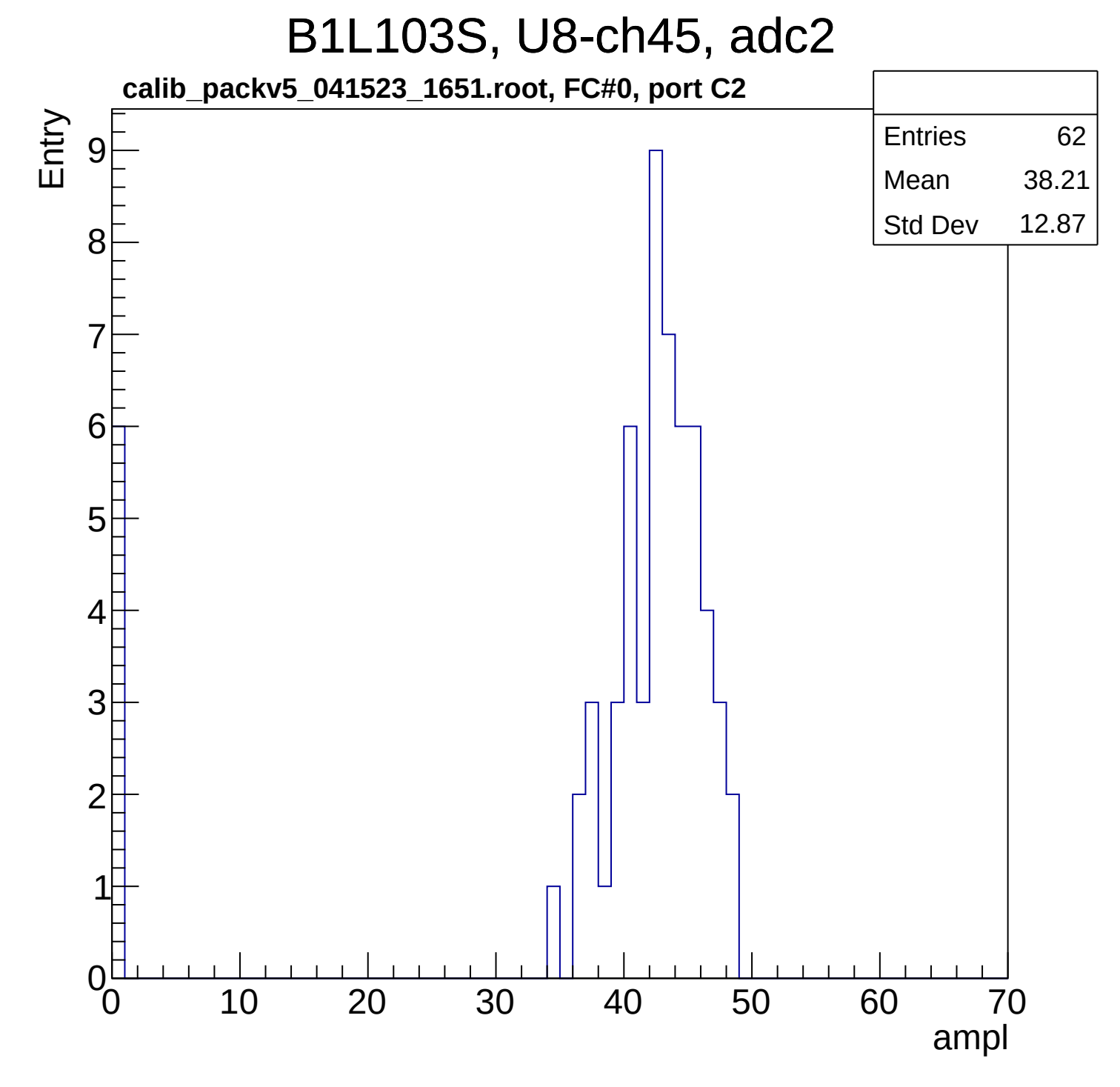
B1L103S, U8-ch45, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 38.21
Std Dev 12.87
Entry
ampl
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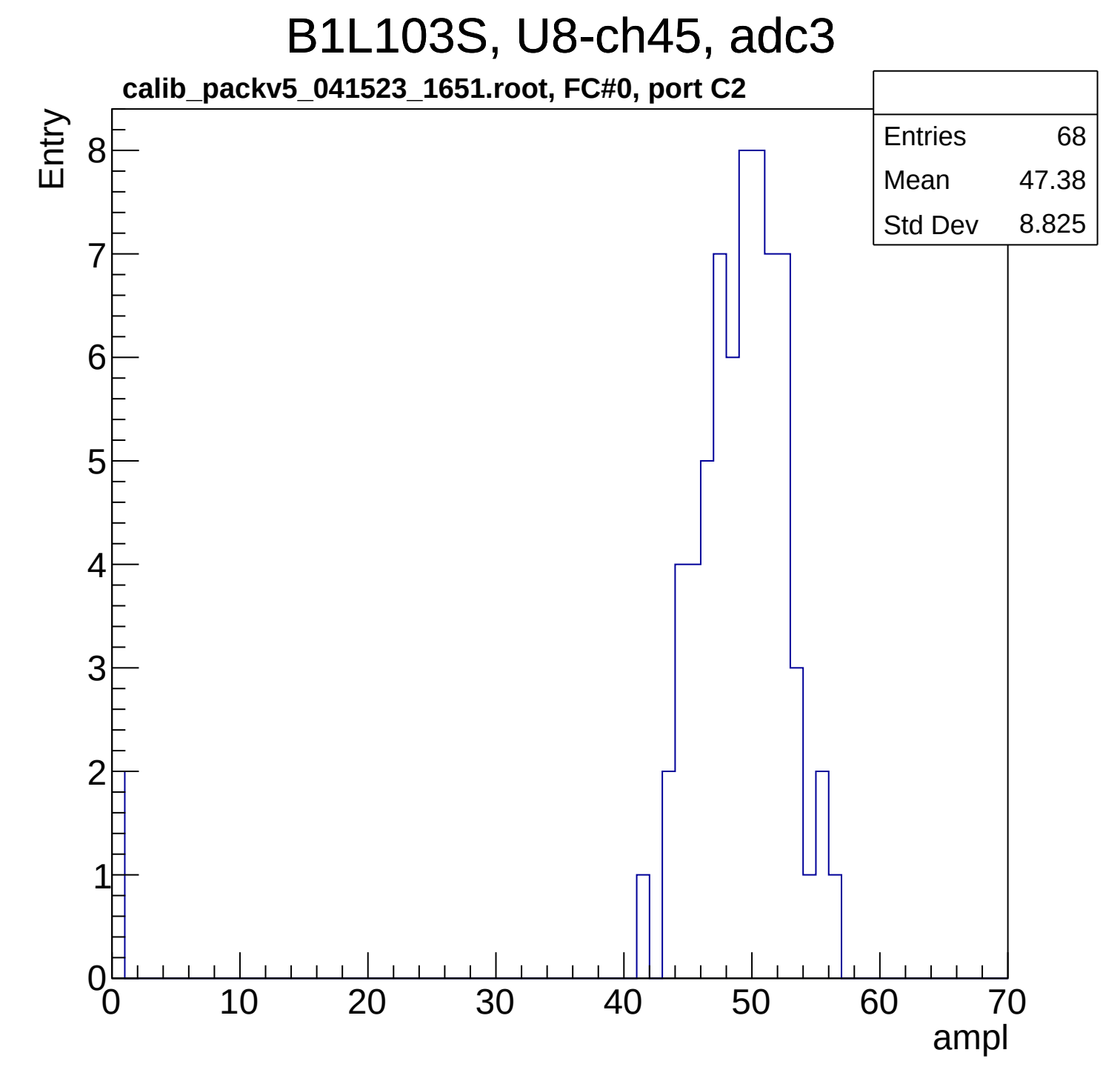
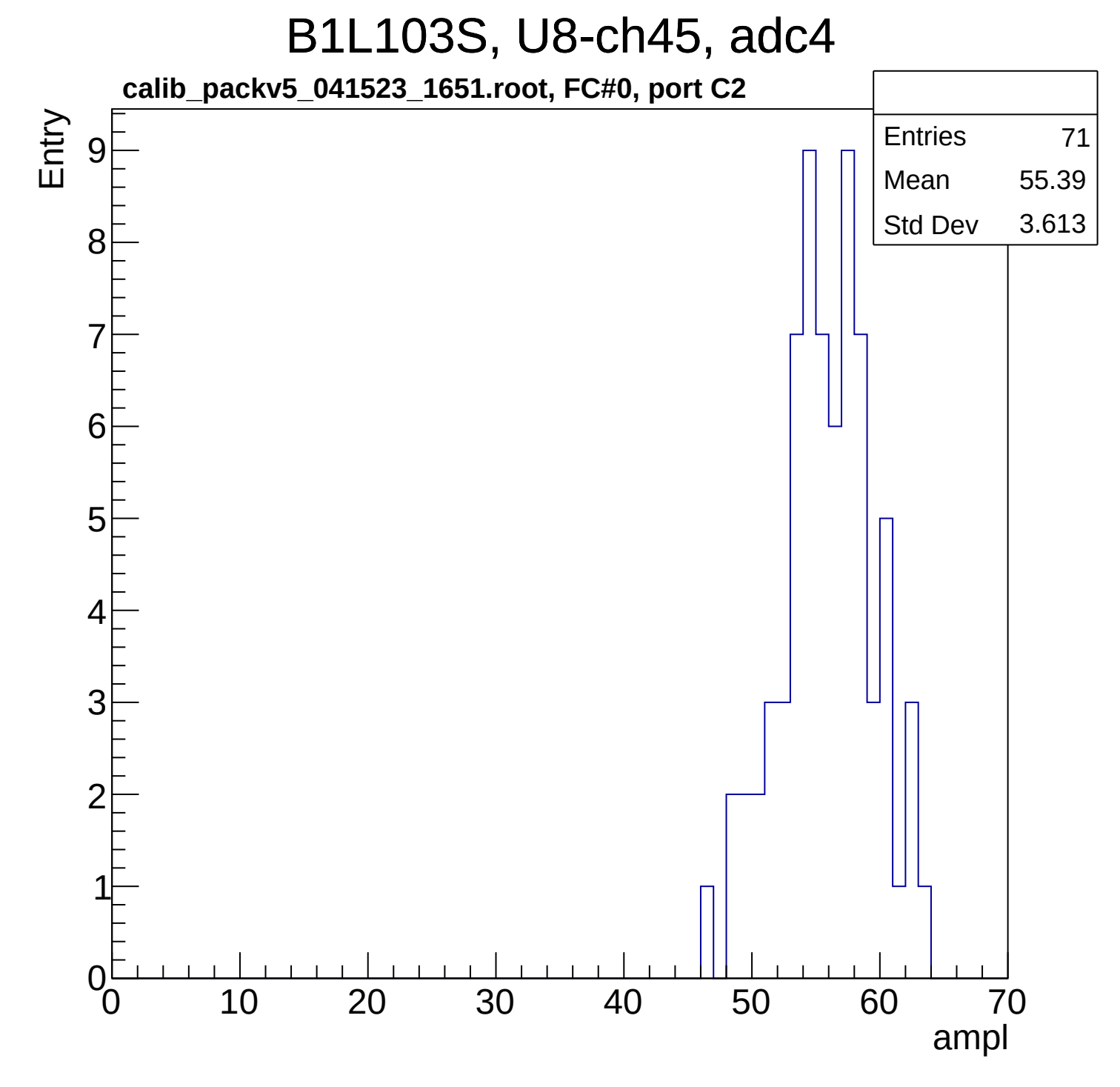
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U8-ch45, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 47.38
Std Dev 8.825
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch45, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 55.39
Std Dev 3.613
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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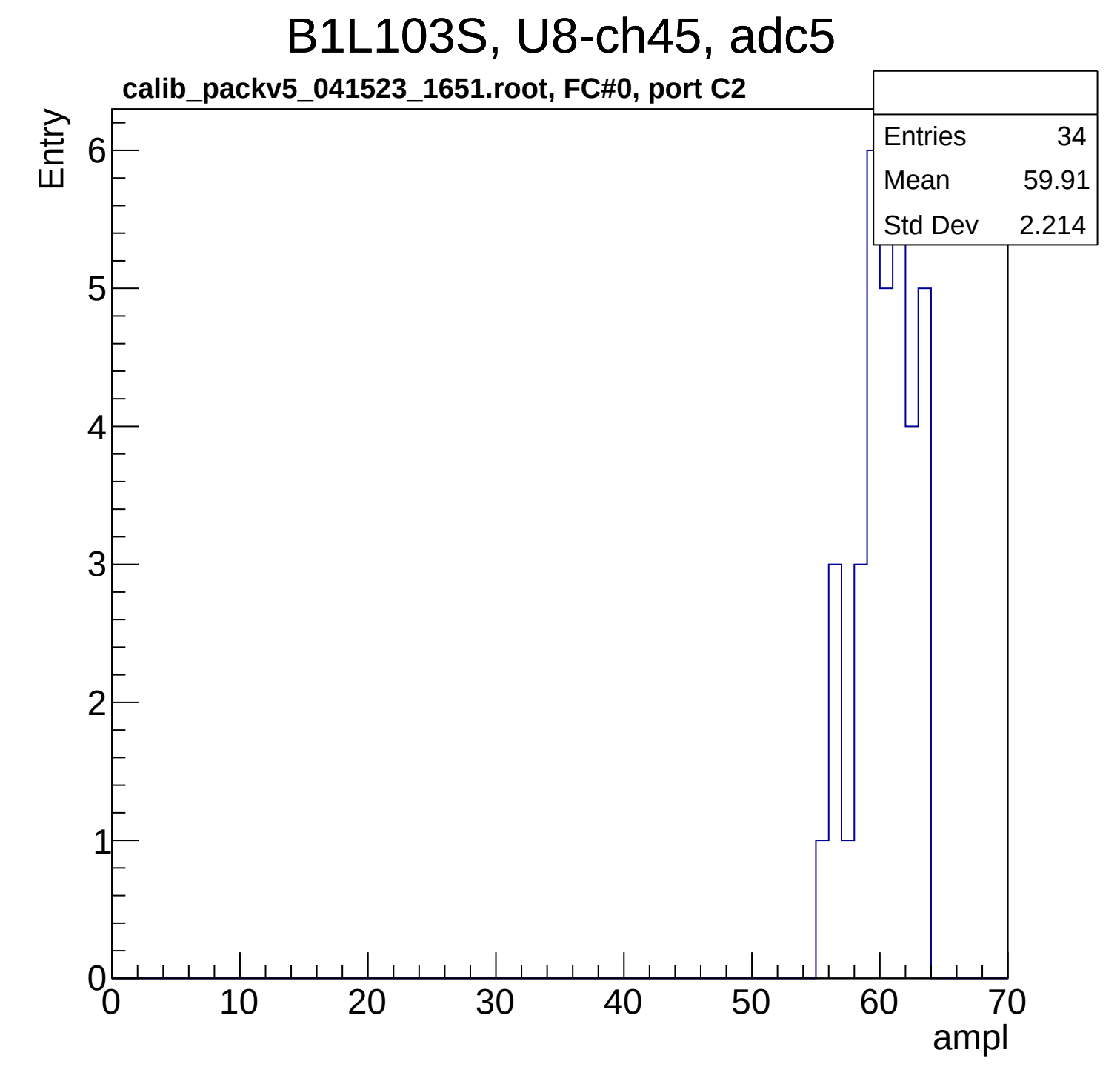
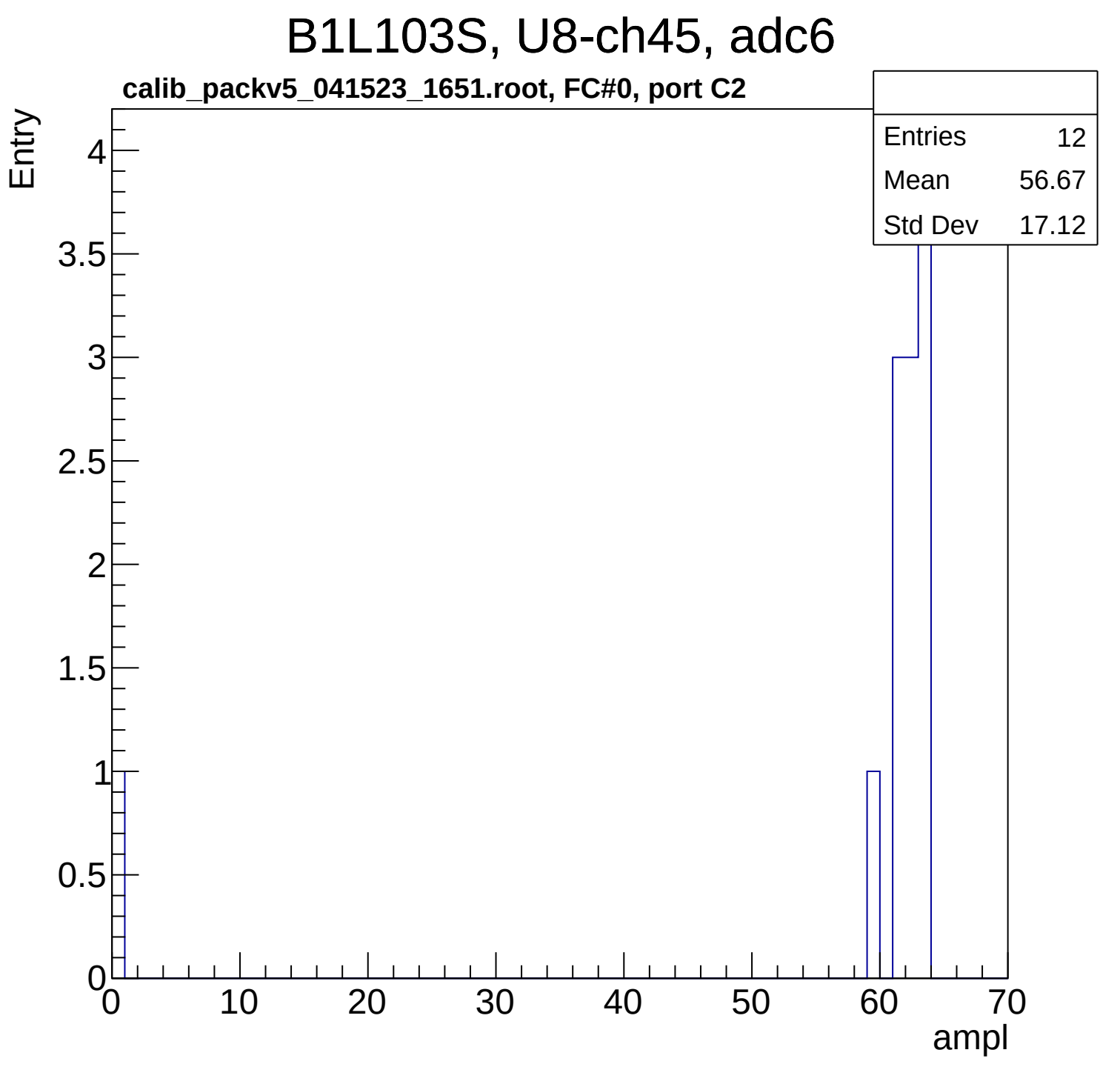
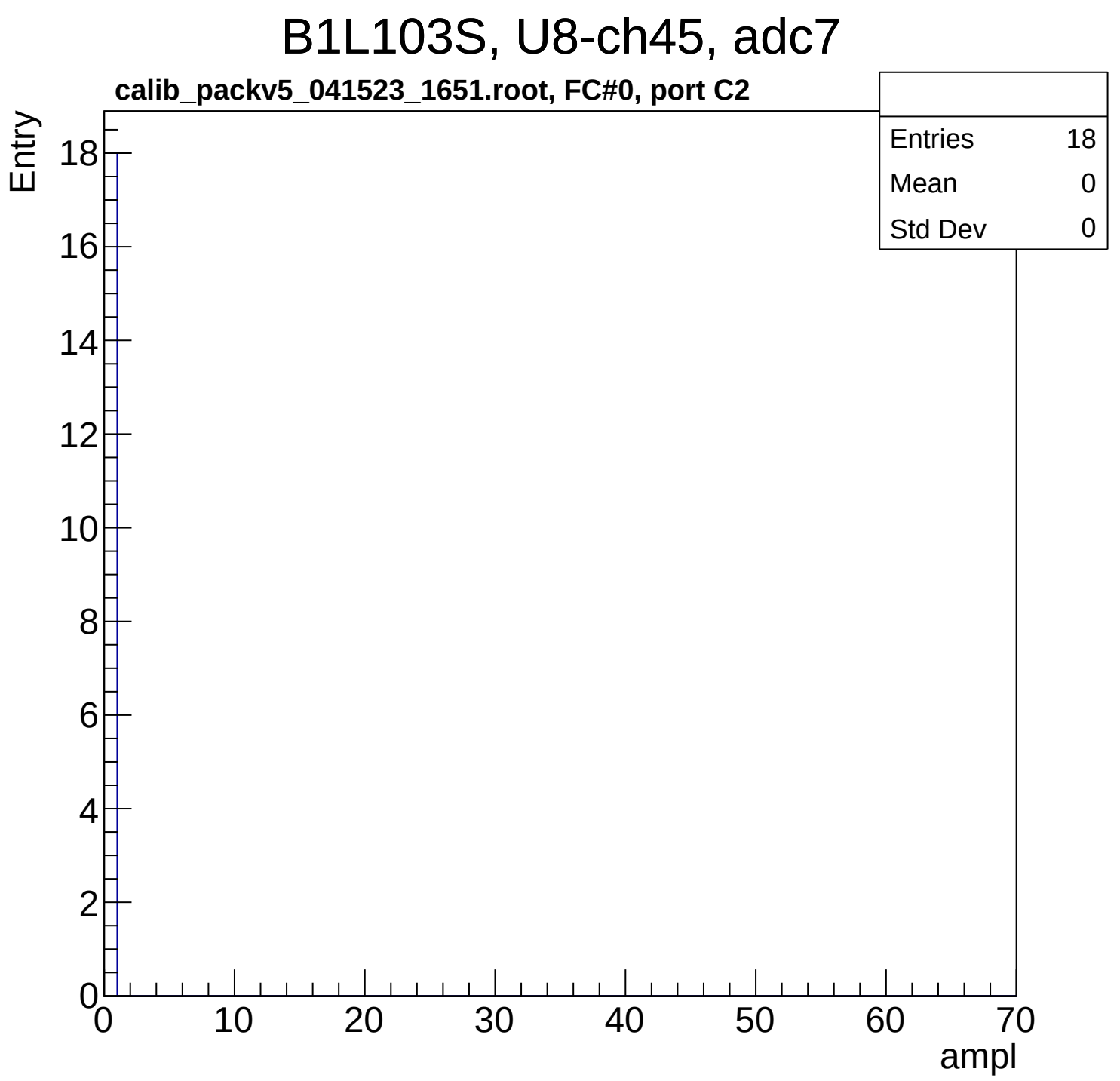
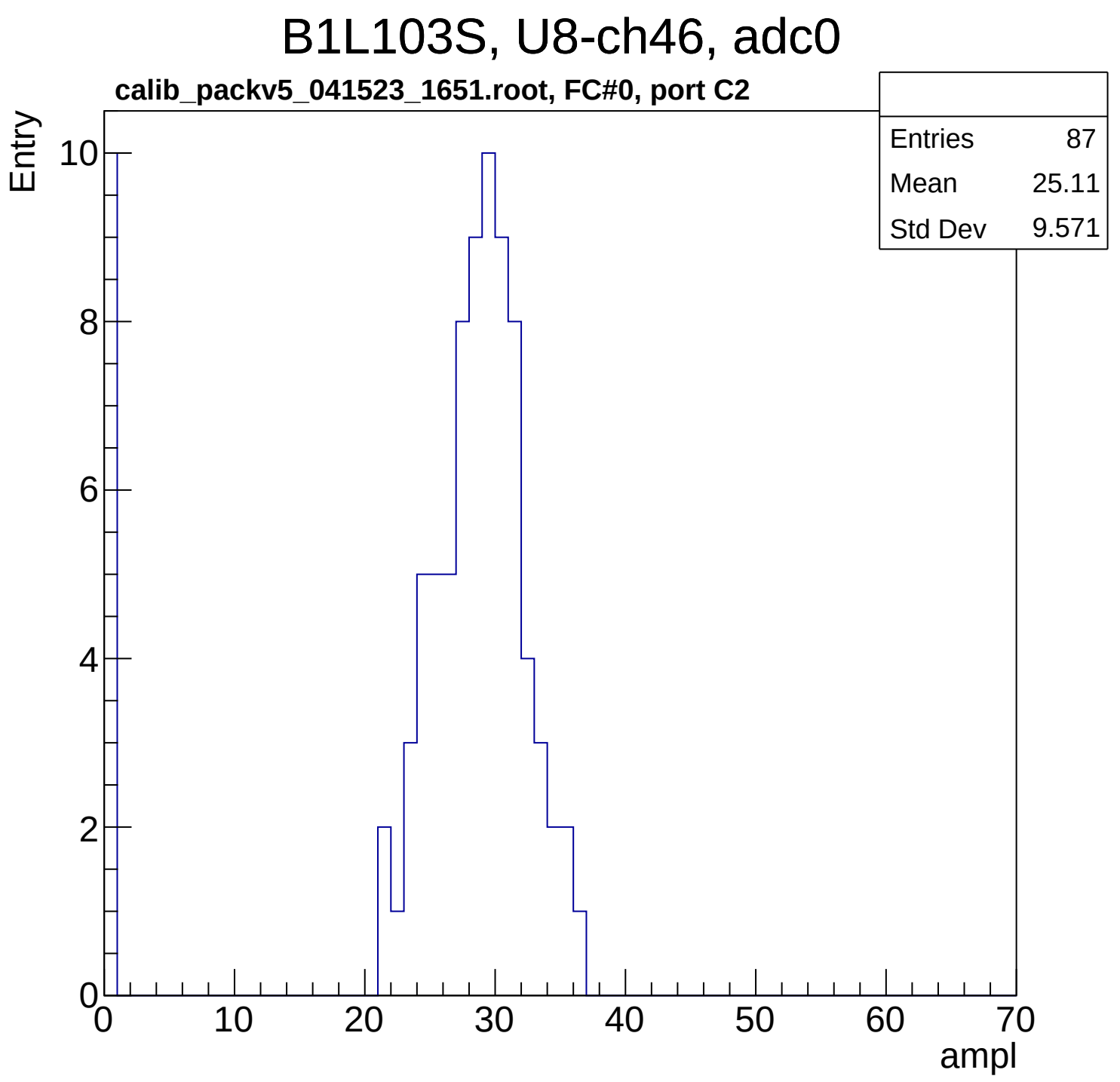
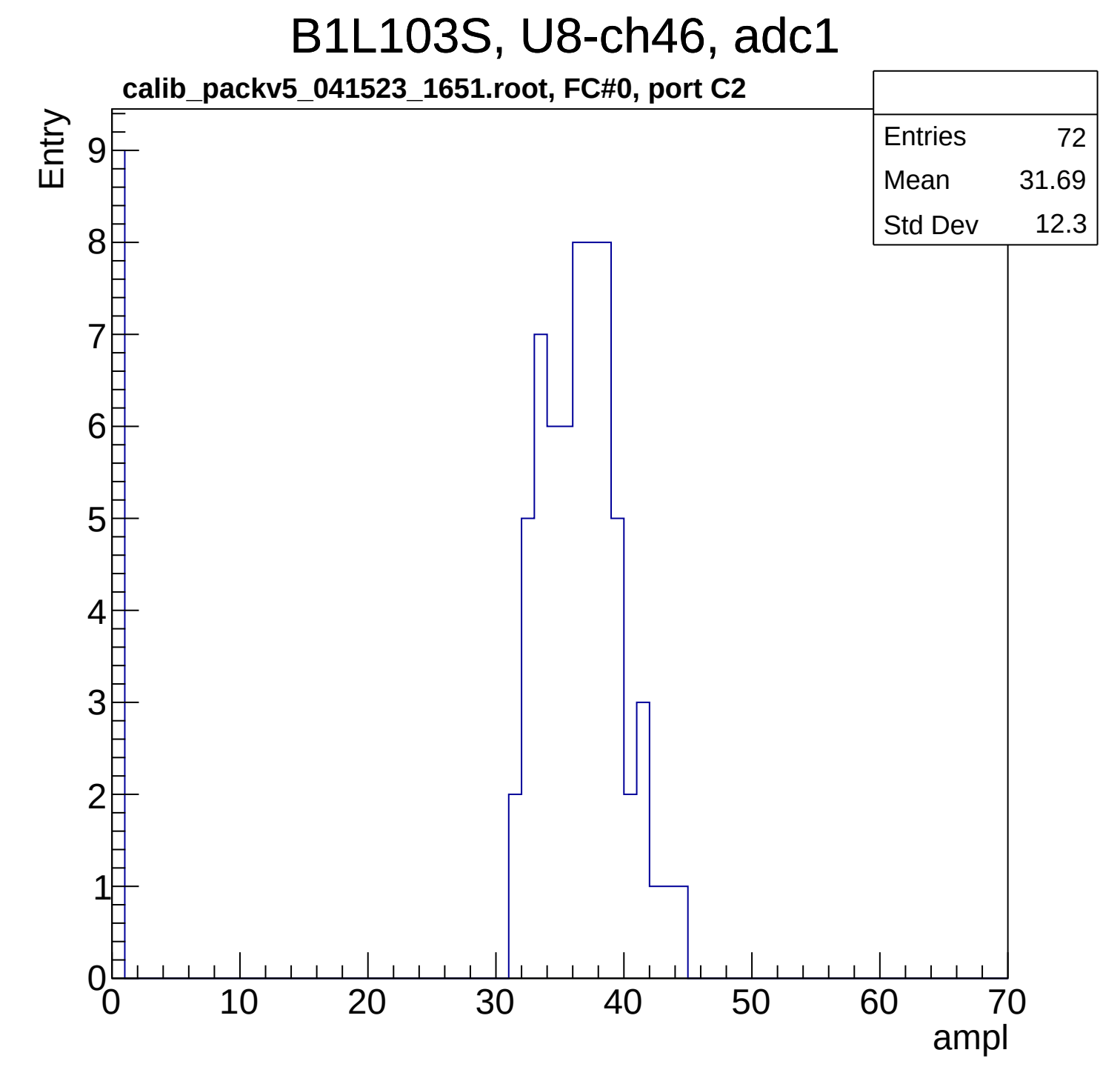

B1L103S, U8-ch45, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 59.91
Std Dev 2.214
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U8-ch45, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 56.67
Std Dev 17.12
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U8-ch45, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch46, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 25.11
Std Dev 9.571
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U8-ch46, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 31.69
Std Dev 12.3
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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60
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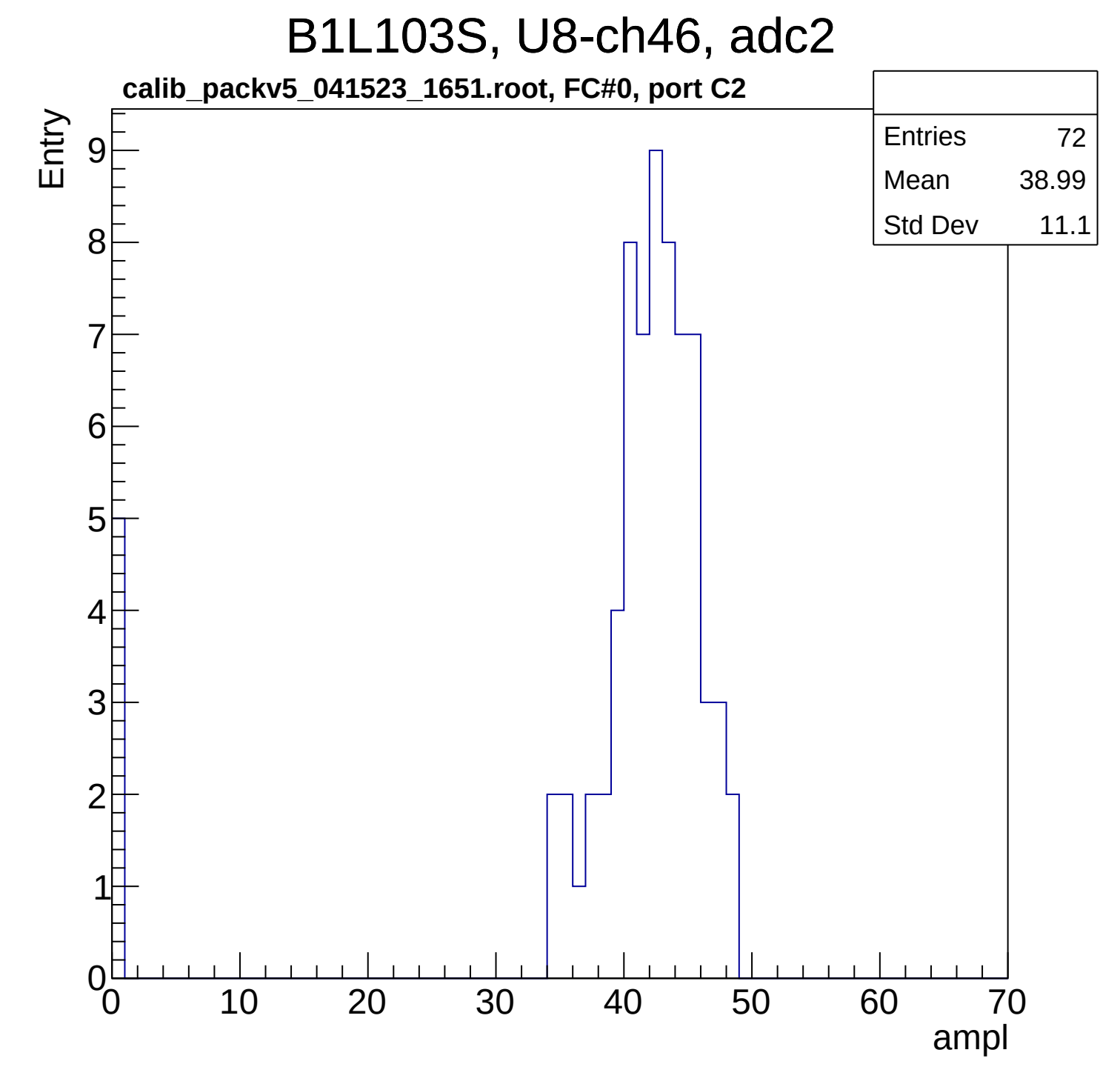
B1L103S, U8-ch46, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 38.99
Std Dev 11.1
Entry
ampl
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1
2
3
4
5
6
7
8
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0
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20
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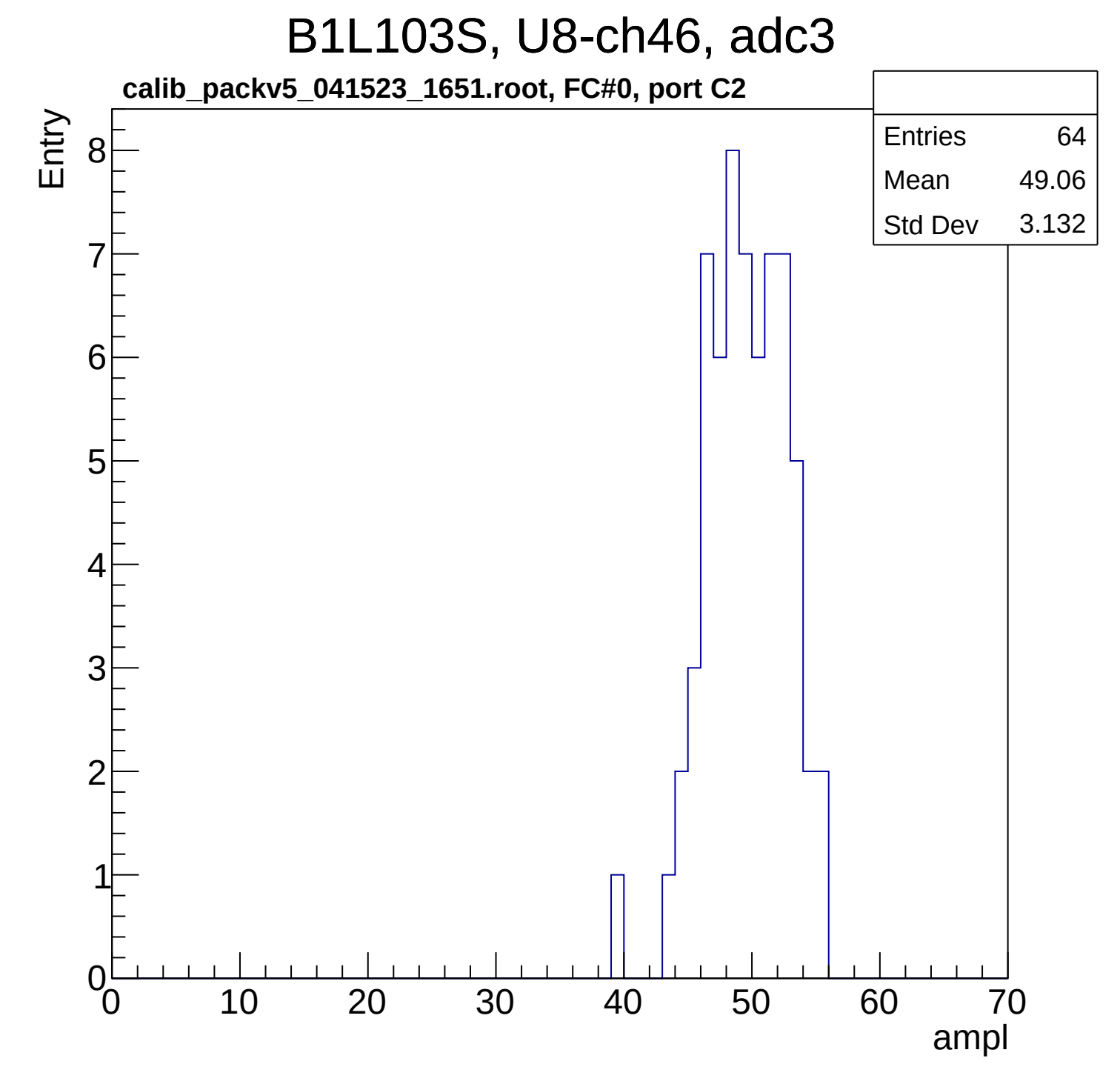
60
70


B1L103S, U8-ch46, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 49.06
Std Dev 3.132
Entry
ampl
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4
5
6
7
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40
50
60
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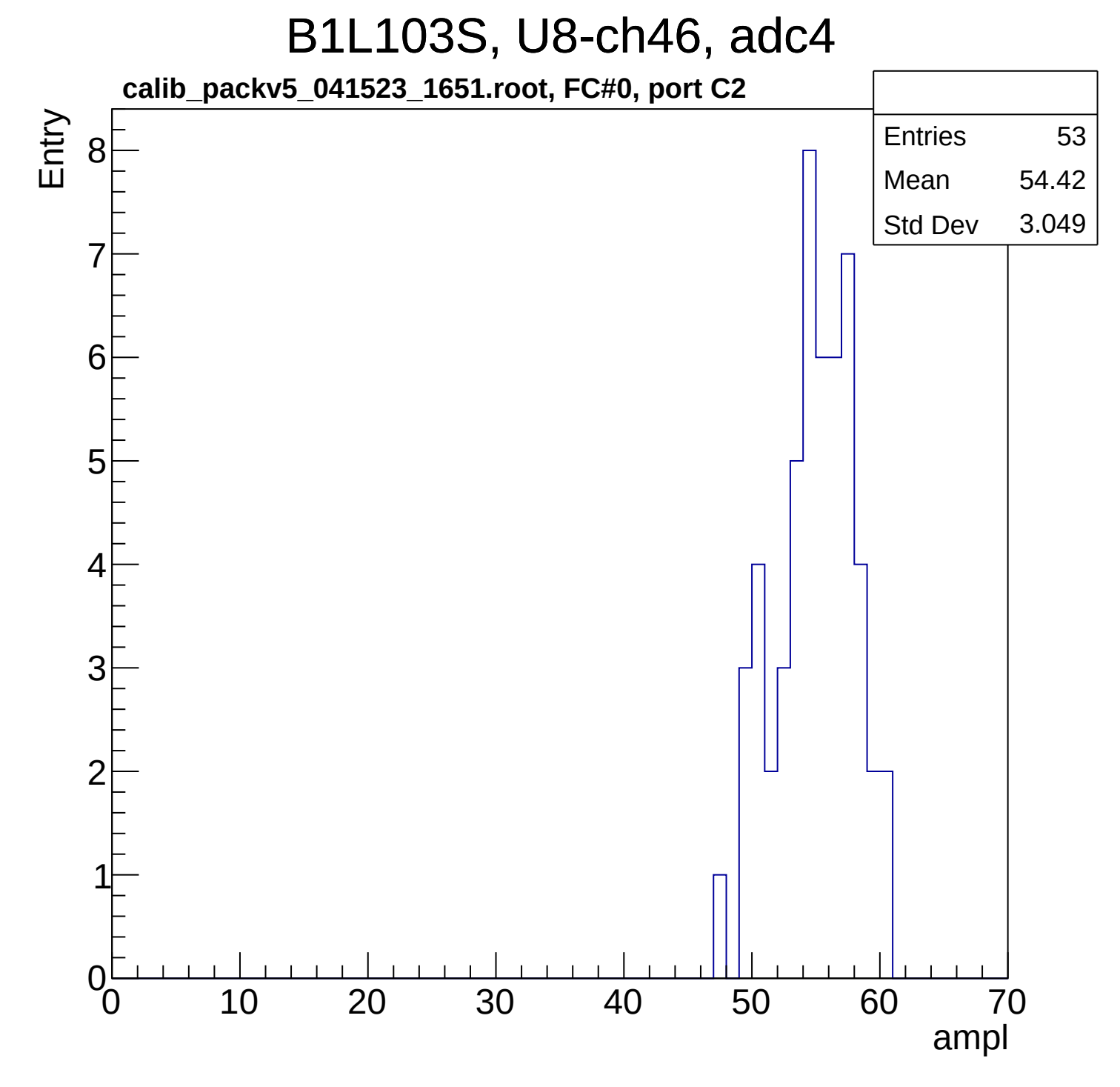
B1L103S, U8-ch46, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 54.42
Std Dev 3.049
Entry
ampl
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2
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4
5
6
7
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0
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40
50
60
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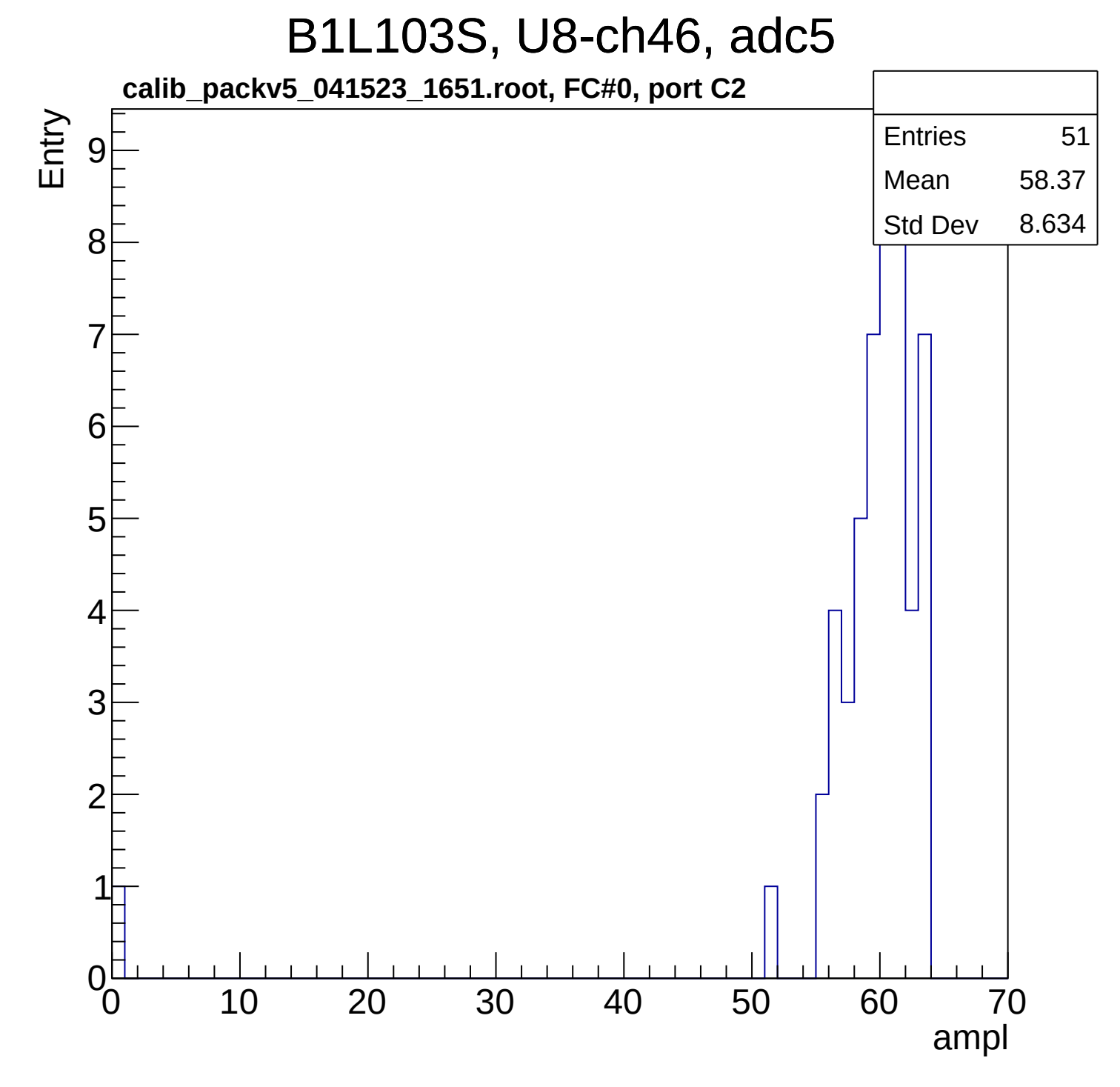
B1L103S, U8-ch46, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 58.37
Std Dev 8.634
Entry
ampl
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2
3
4
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6
7
8
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0
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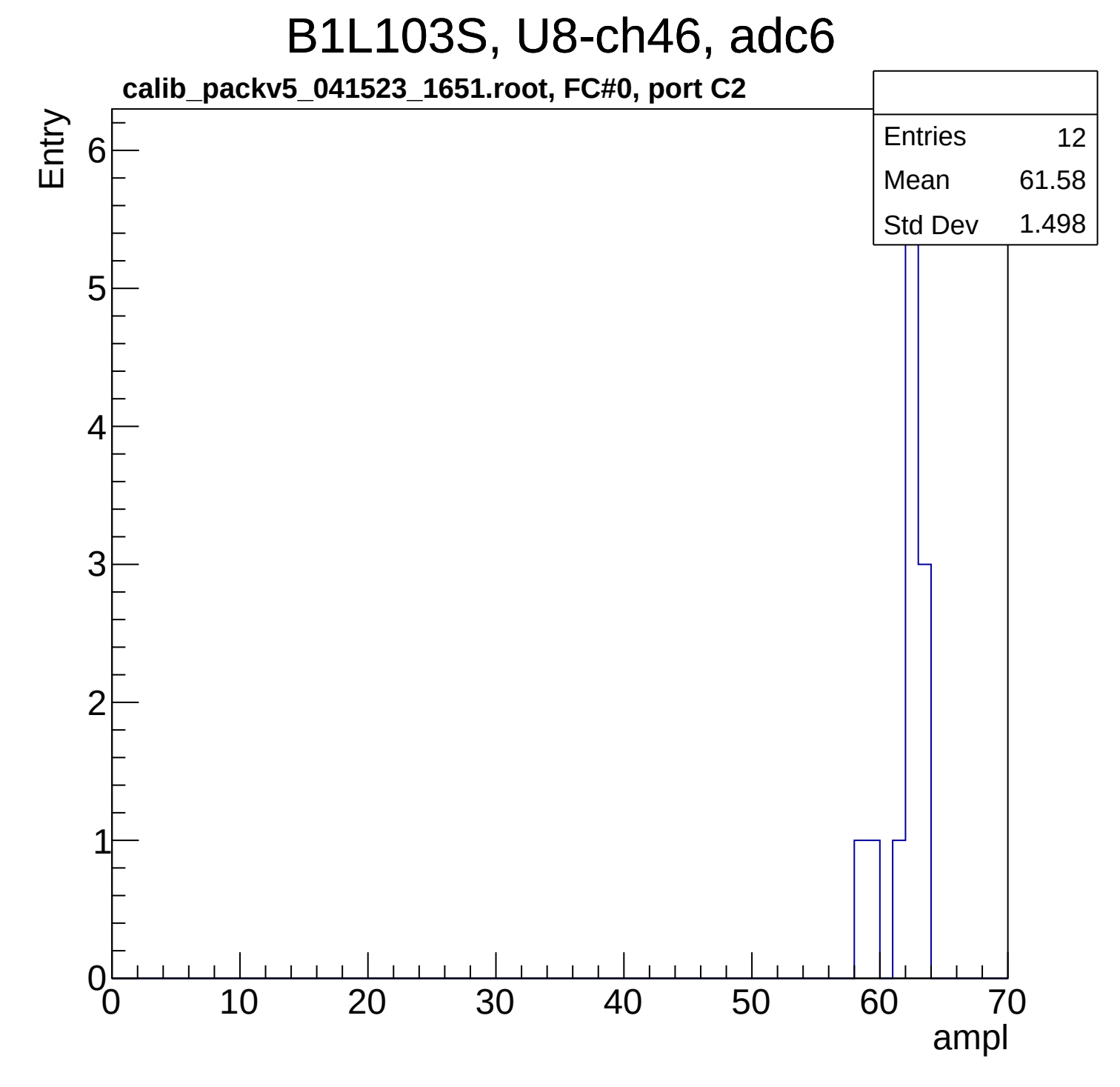
60
70


B1L103S, U8-ch46, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.58
Std Dev 1.498
Entry
ampl
0
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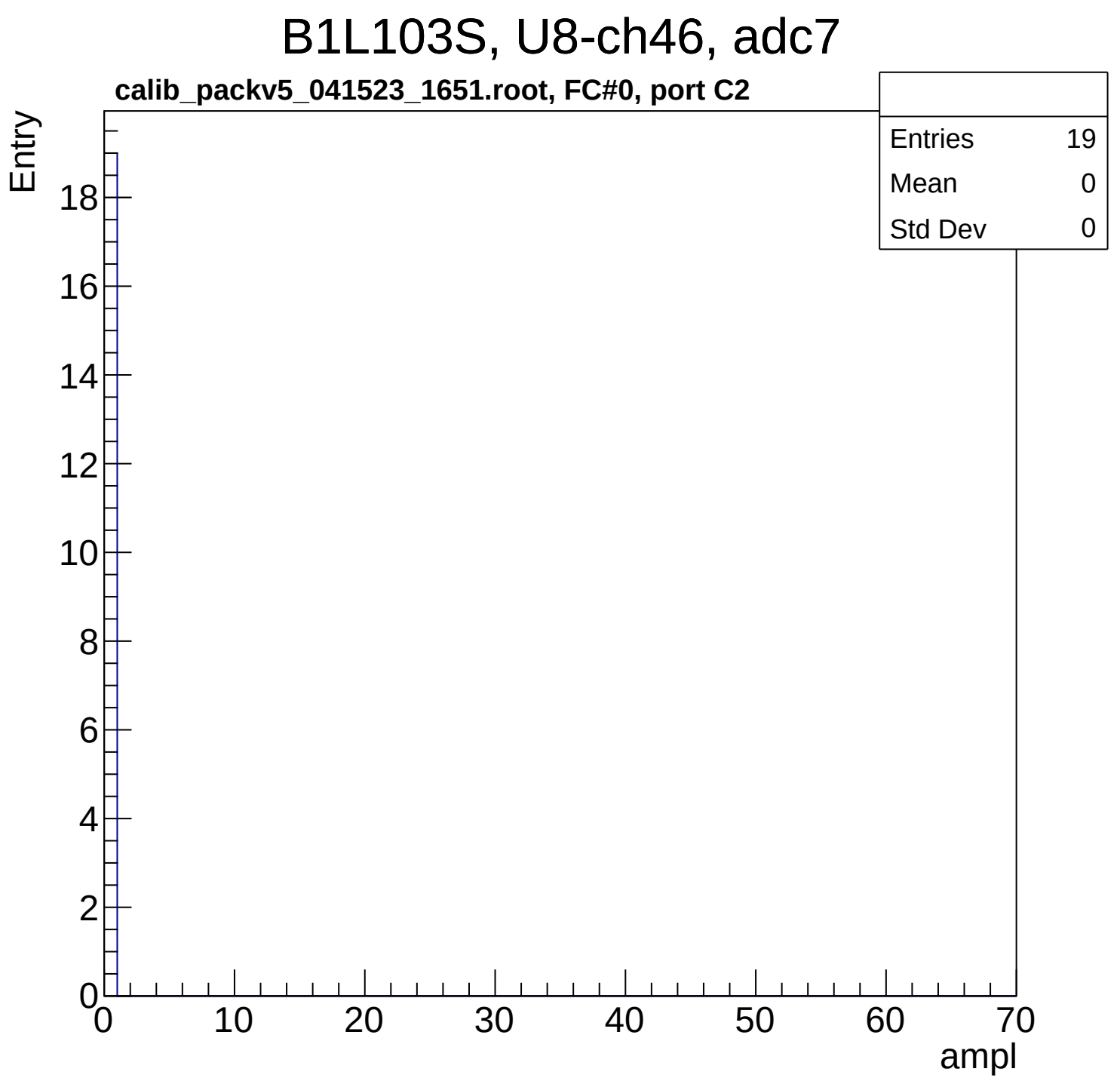
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U8-ch46, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
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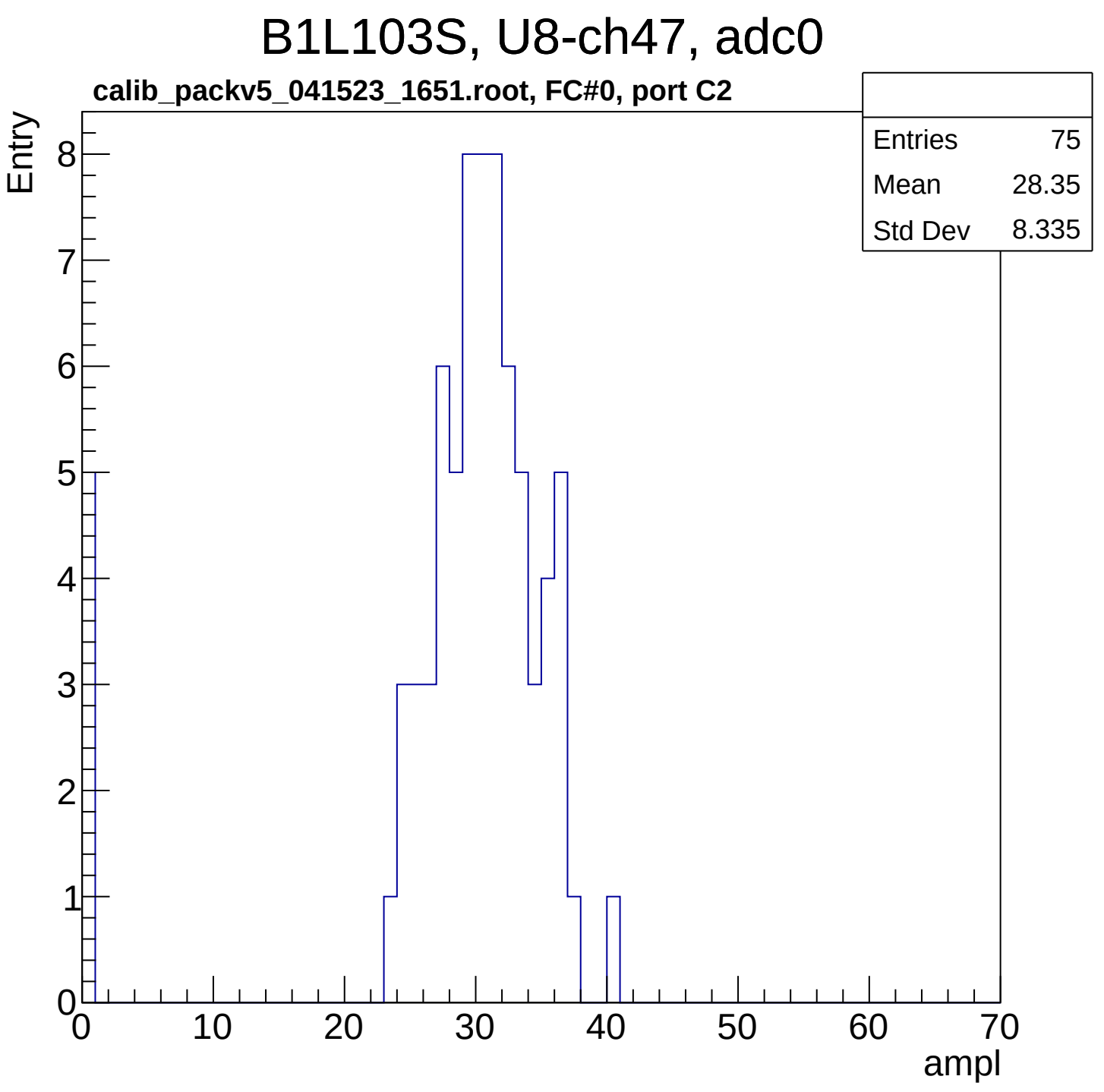
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch47, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 28.35
Std Dev 8.335
Entry
ampl
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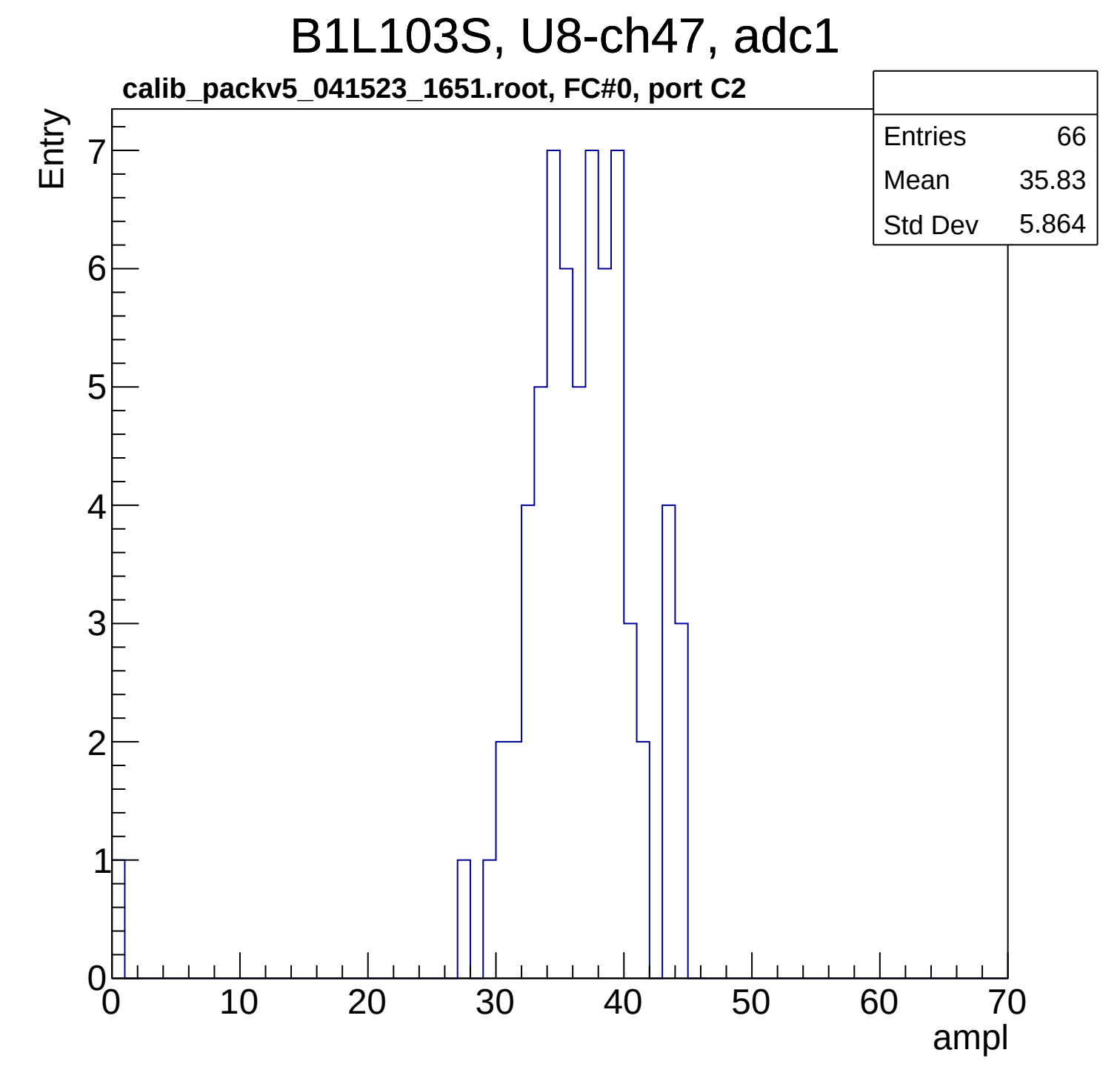
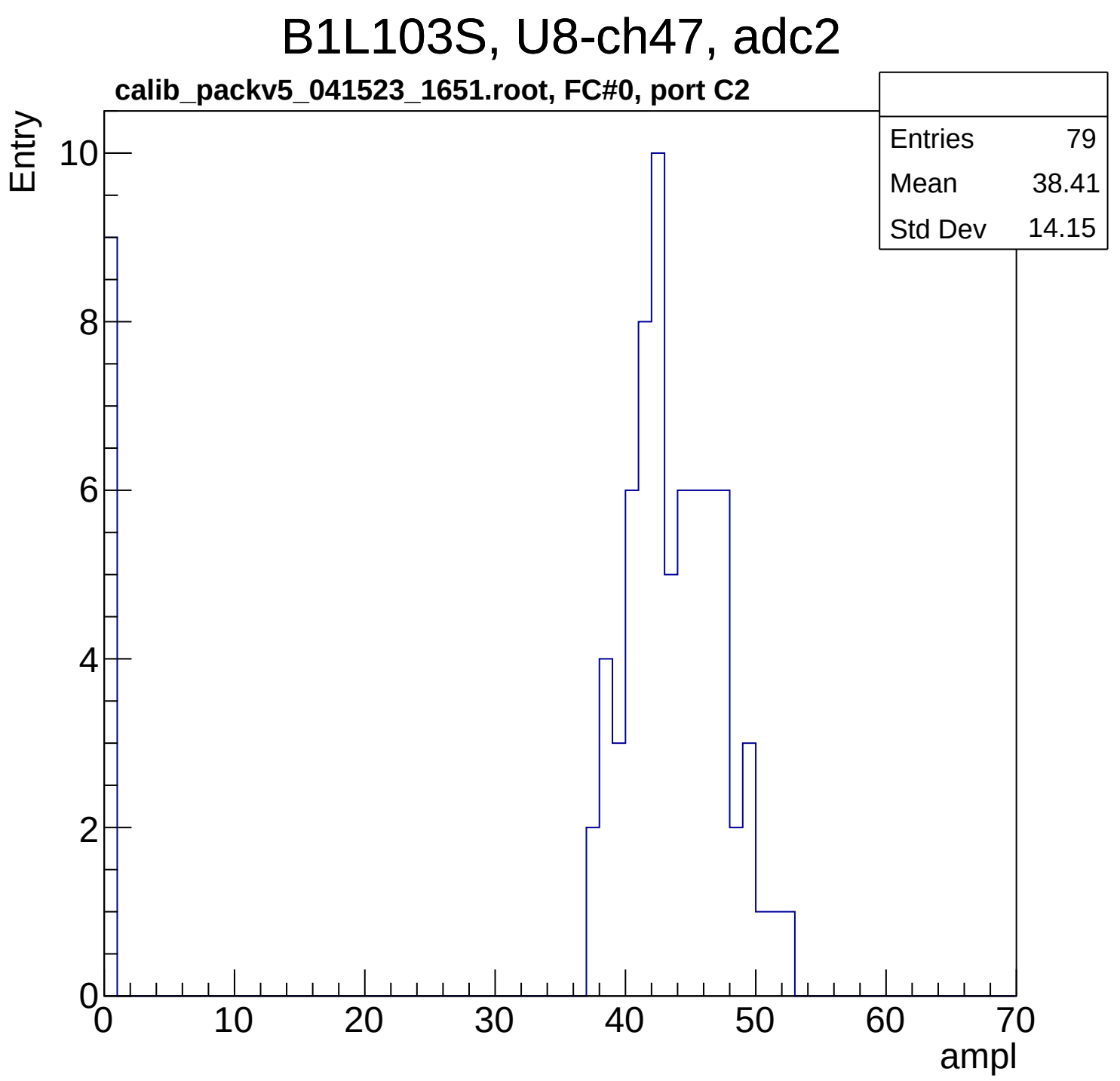
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch47, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 35.83
Std Dev 5.864
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U8-ch47, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 38.41
Std Dev 14.15
Entry
ampl
0
2
4
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0
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20
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40
50
60
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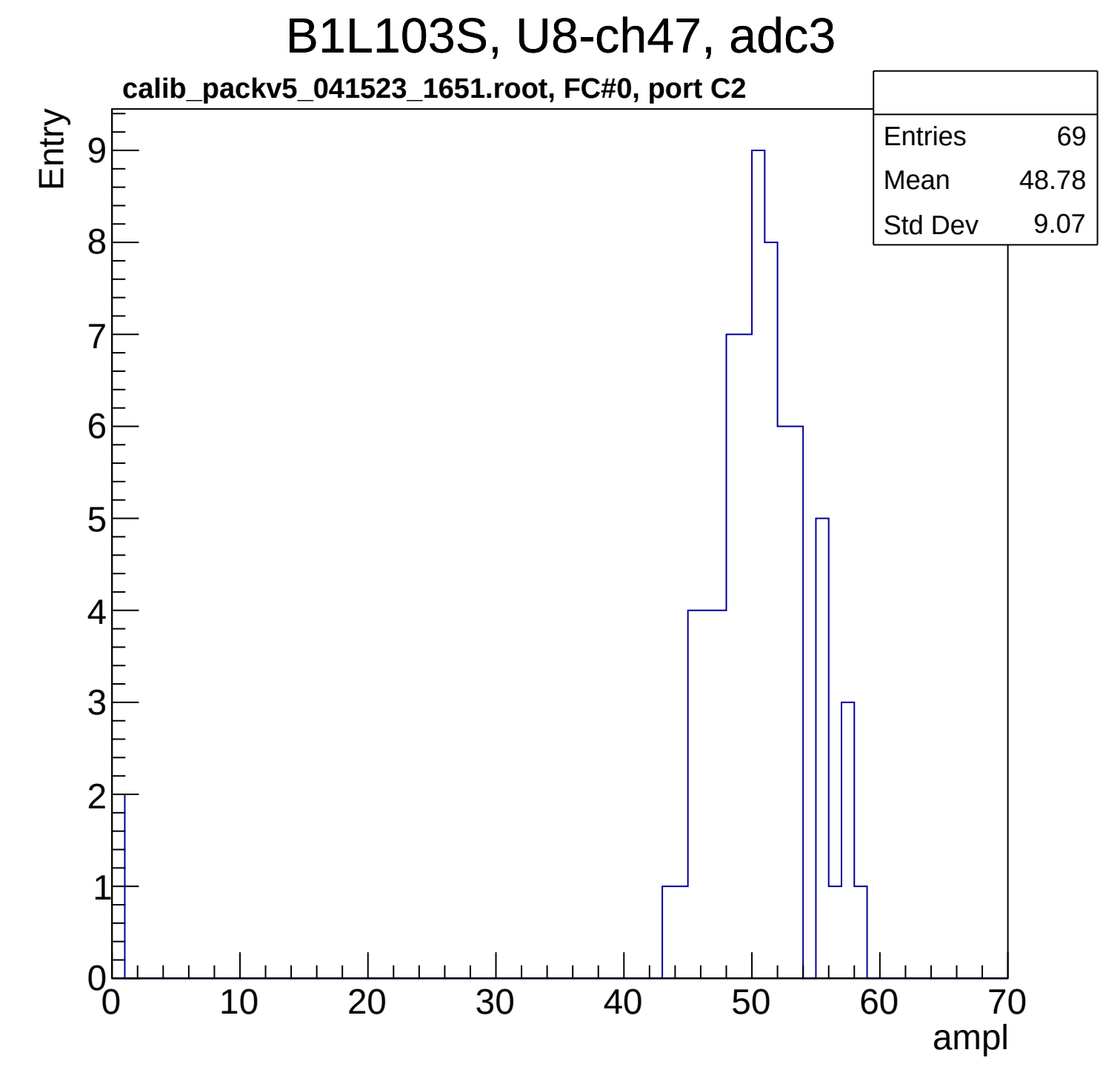
B1L103S, U8-ch47, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 48.78
Std Dev 9.07
Entry
ampl
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3
4
5
6
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8
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0
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40
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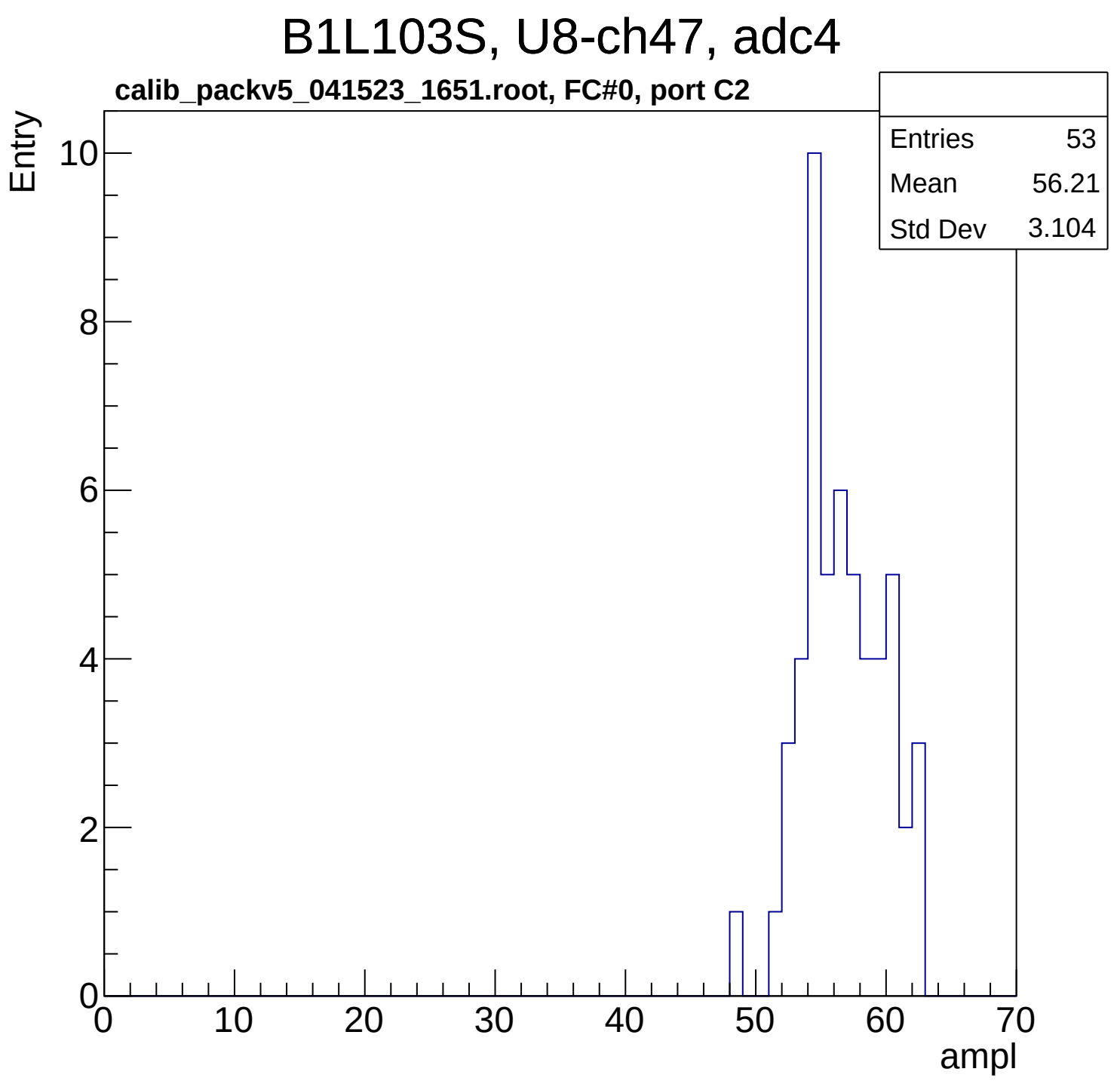
B1L103S, U8-ch47, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 56.21
Std Dev 3.104
Entry
ampl
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4
6
8
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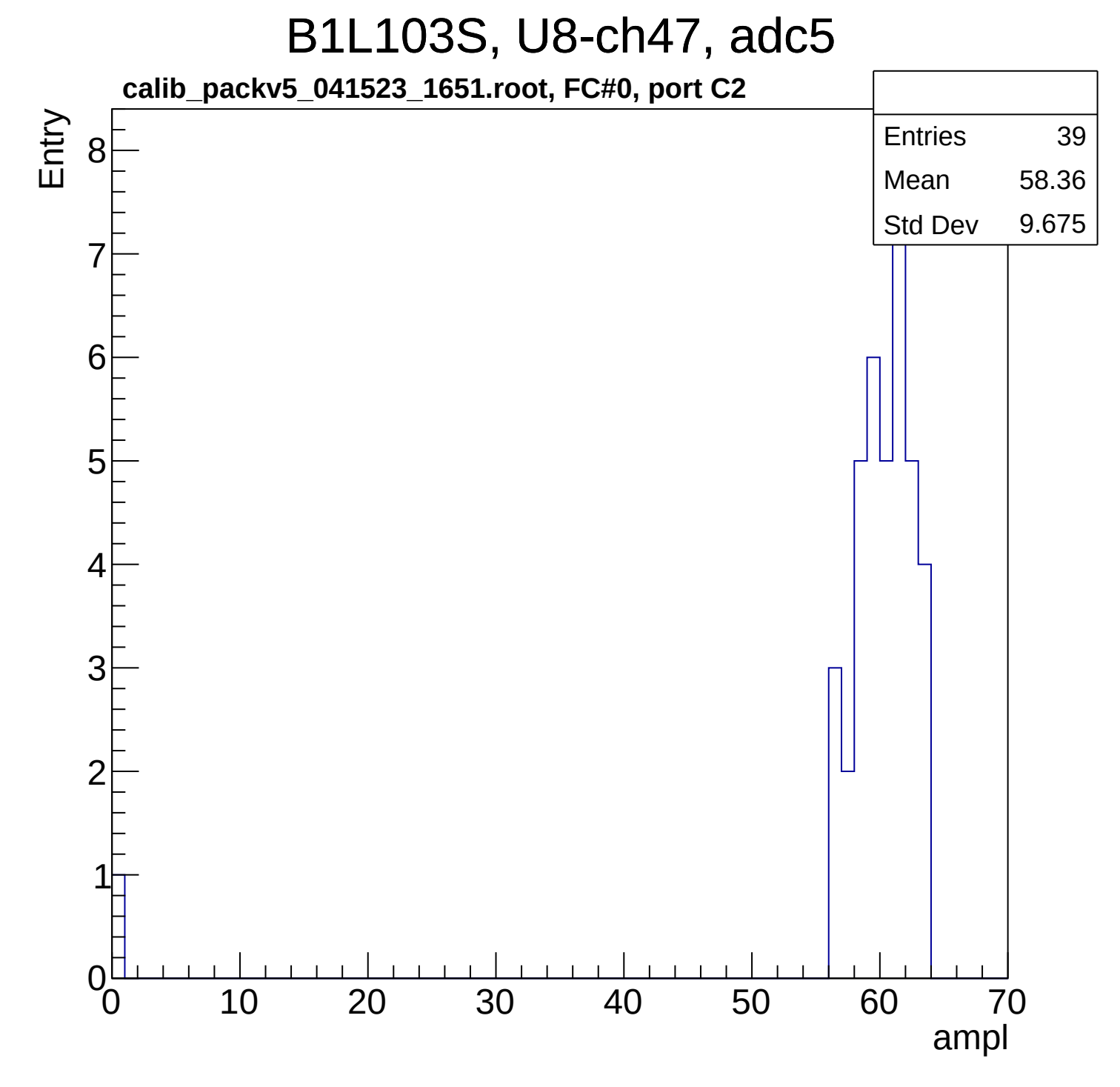
60
70


B1L103S, U8-ch47, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 58.36
Std Dev 9.675
Entry
ampl
0
1
2
3
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5
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60
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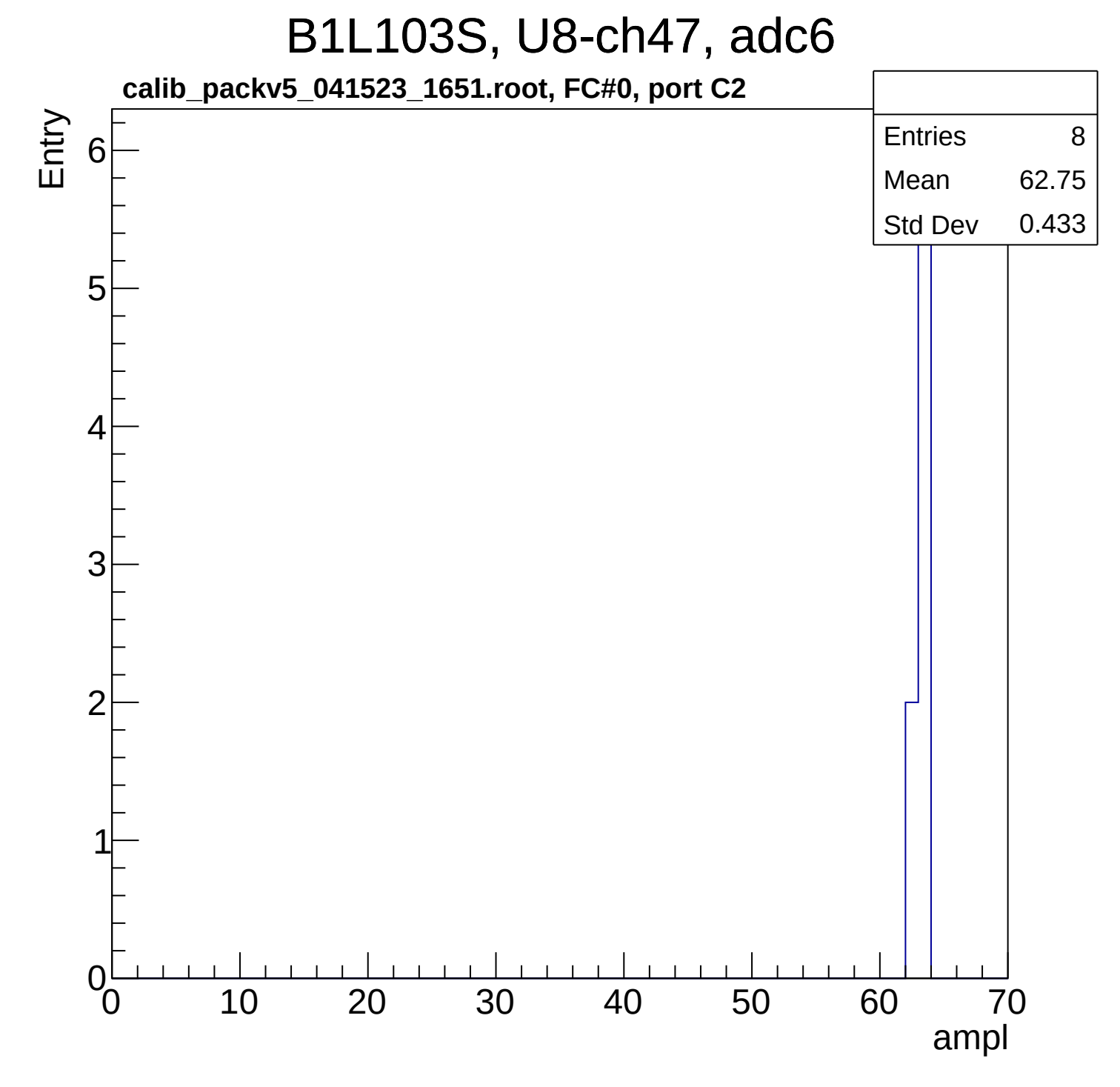
B1L103S, U8-ch47, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 62.75
Std Dev 0.433
Entry
ampl
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1
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3
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0
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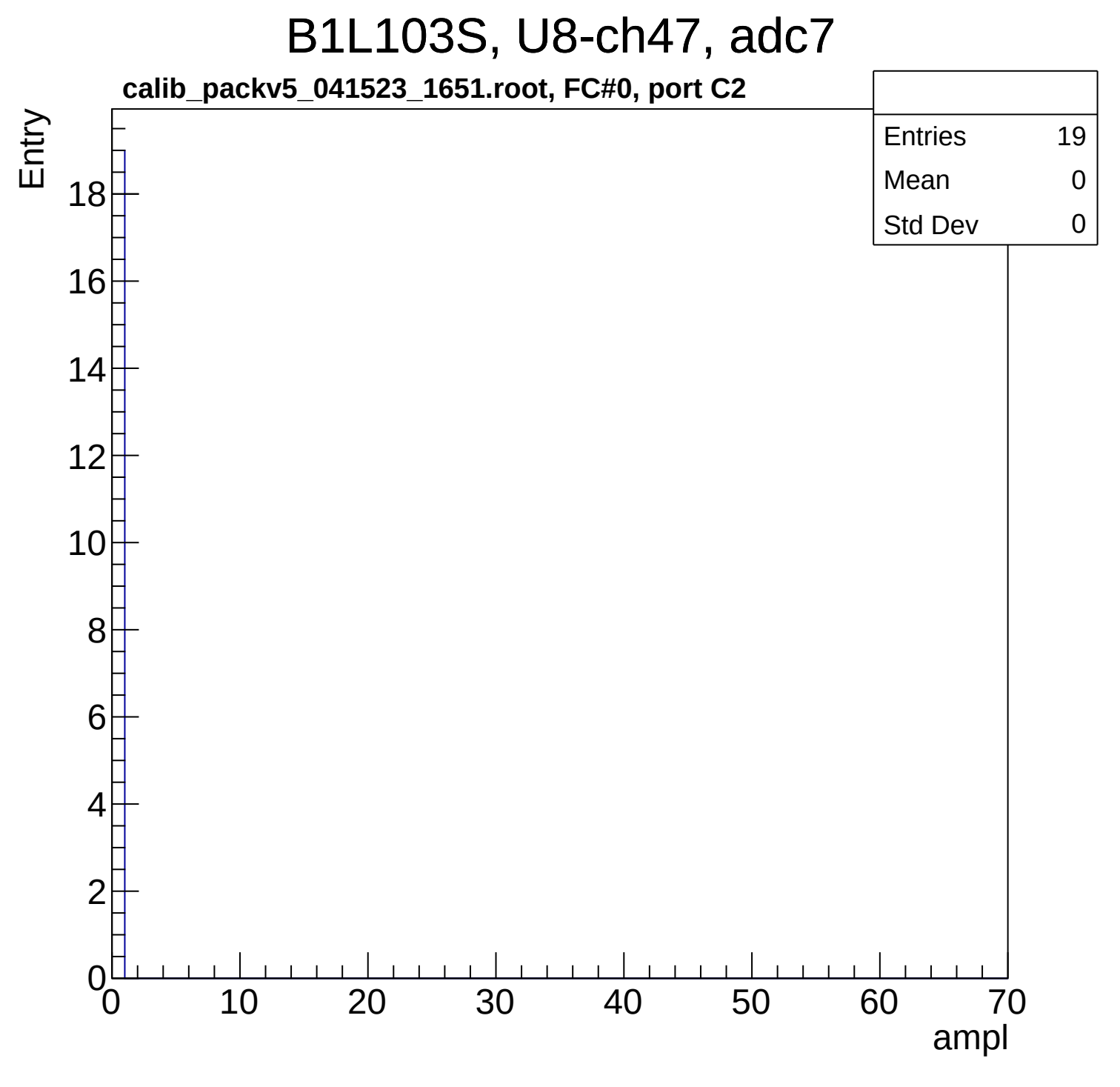
B1L103S, U8-ch47, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
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6
8
10
12
14
16
18
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10
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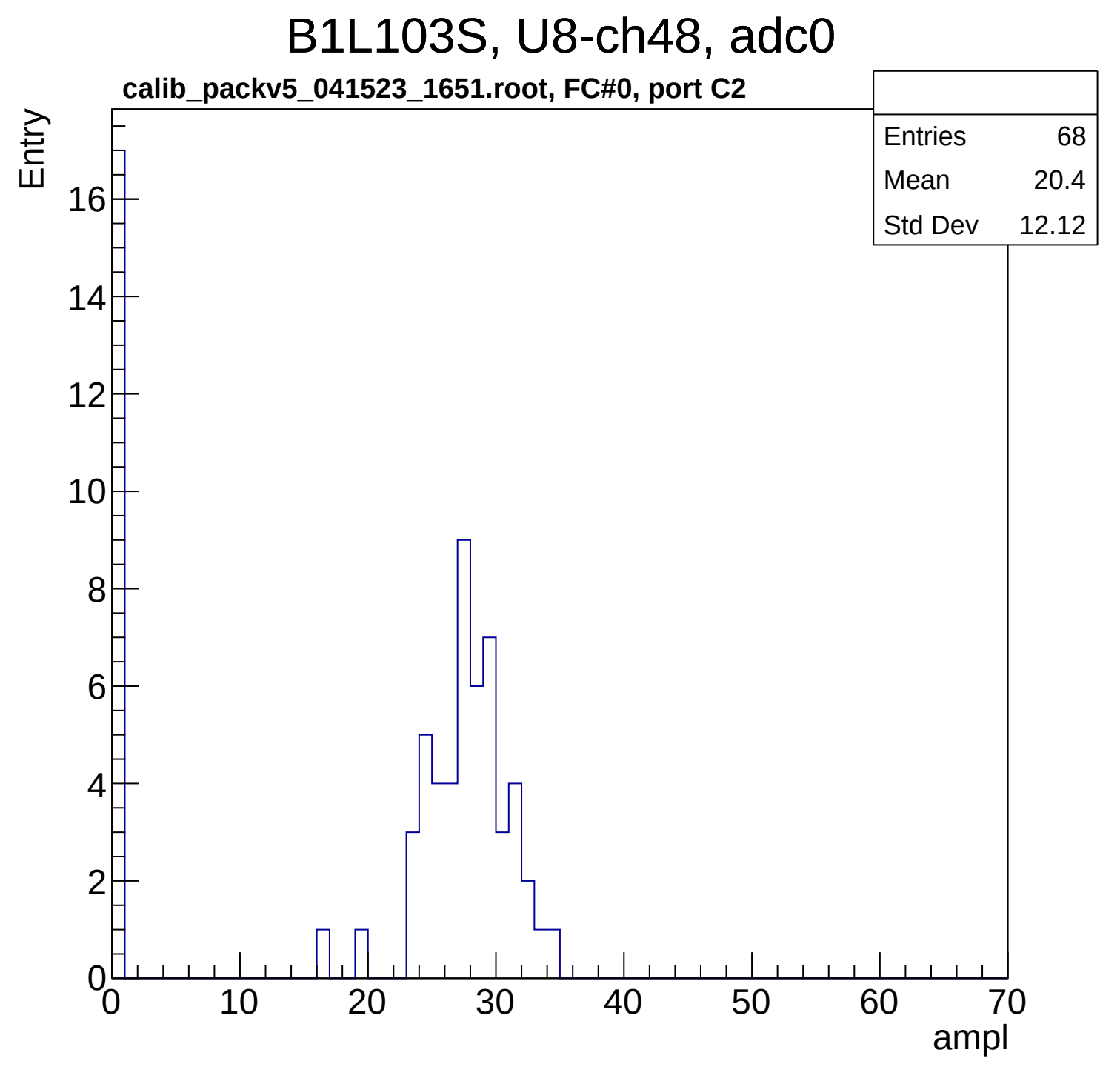
50
60
70
ampl


B1L103S, U8-ch48, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 20.4
Std Dev 12.12
Entry
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4
6
8
10
12
14
16
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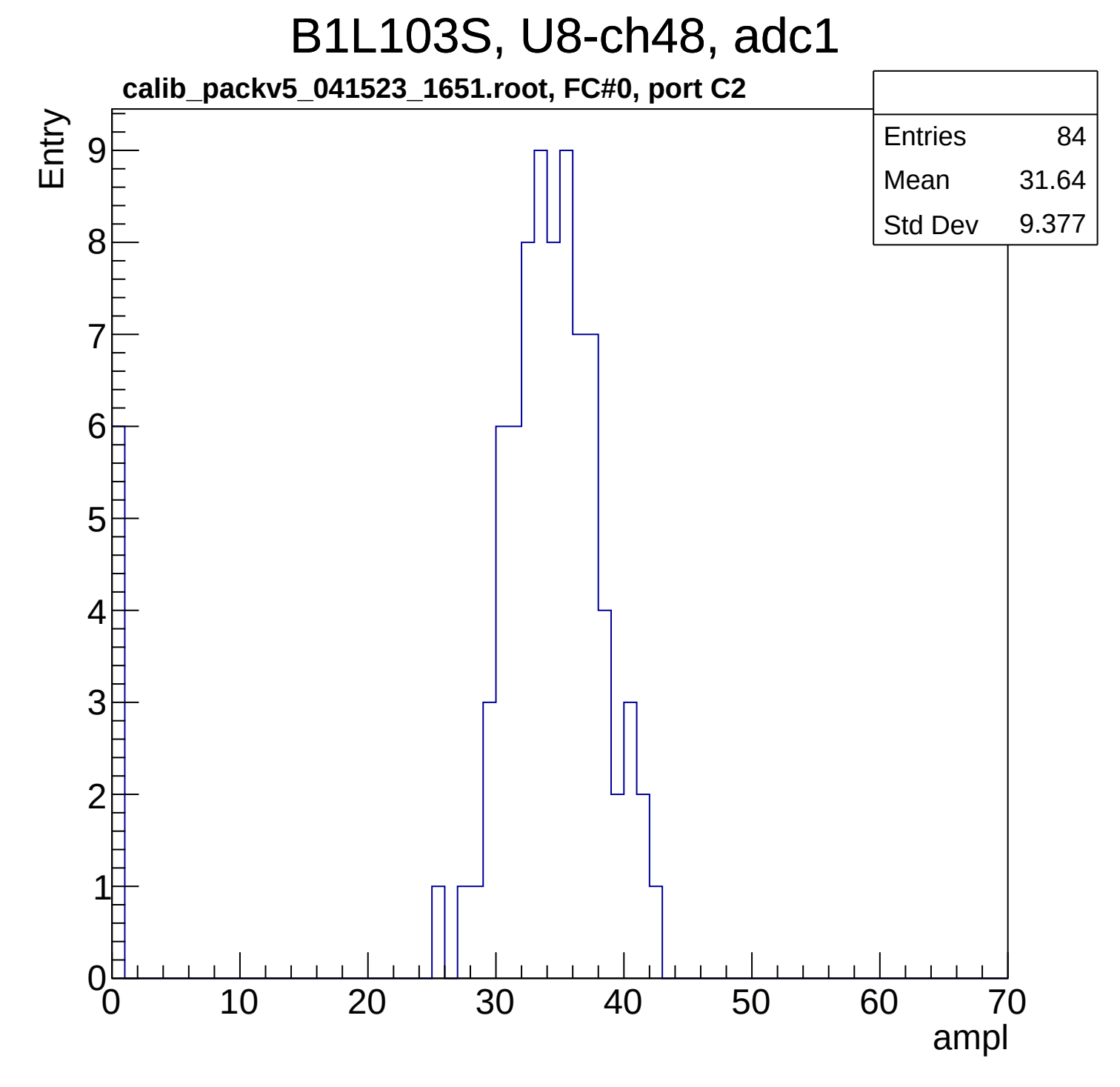
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch48, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 31.64
Std Dev 9.377
Entry
ampl
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6
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0
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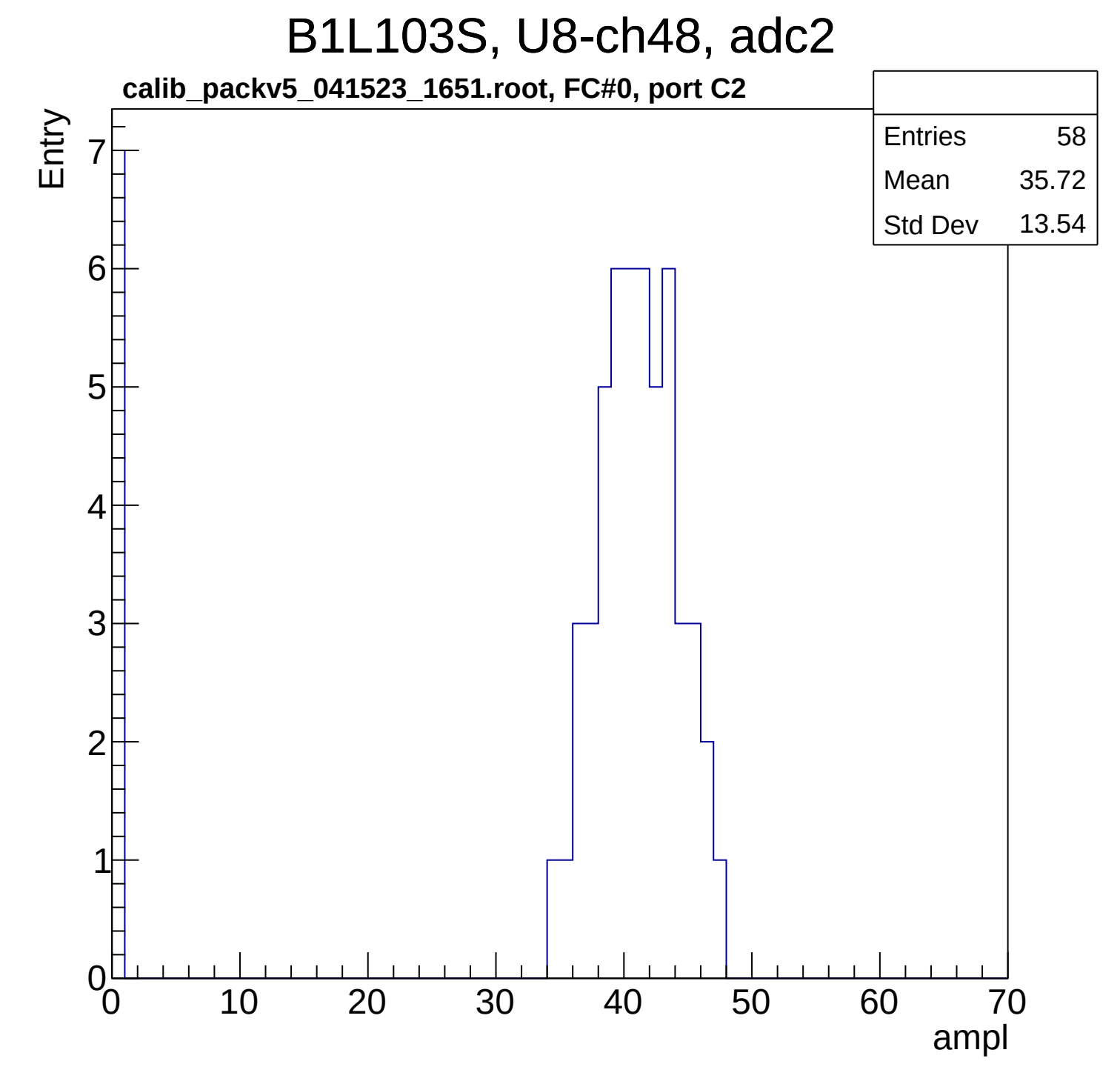
B1L103S, U8-ch48, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 35.72
Std Dev 13.54
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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40
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60
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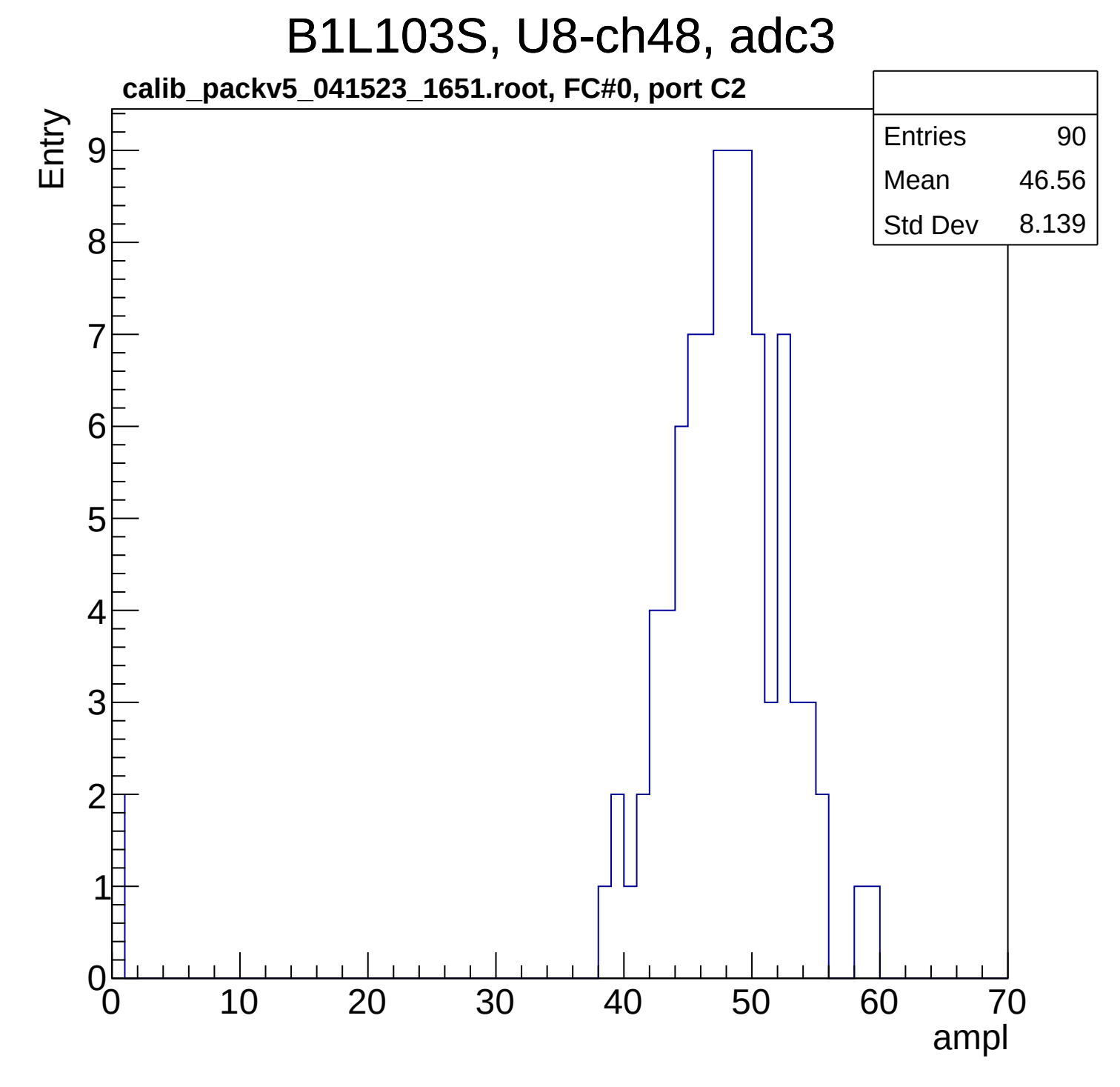
B1L103S, U8-ch48, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 46.56
Std Dev 8.139
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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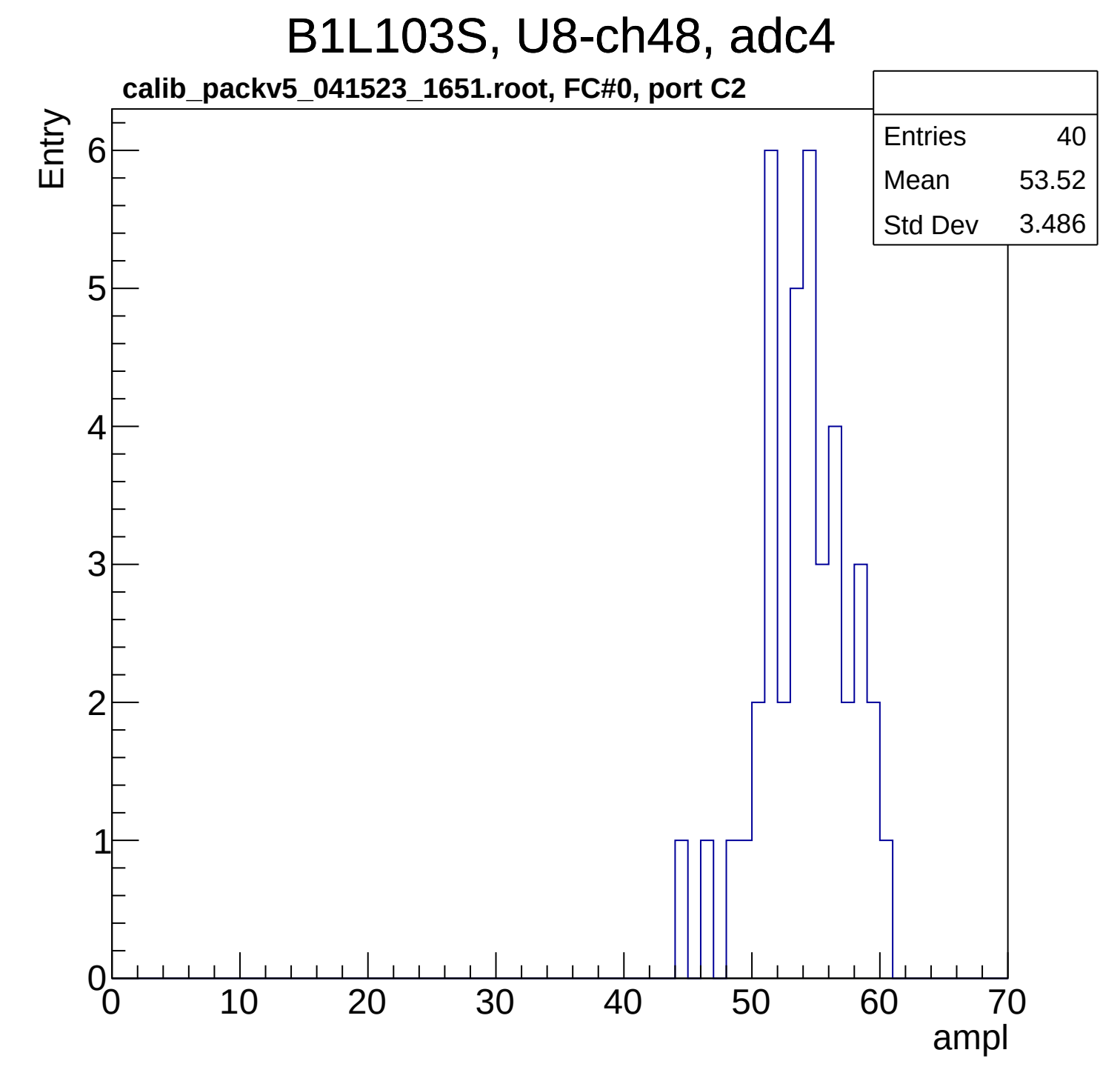
B1L103S, U8-ch48, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 53.52
Std Dev 3.486
Entry
ampl
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2
3
4
5
6
0
10
20
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40
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60
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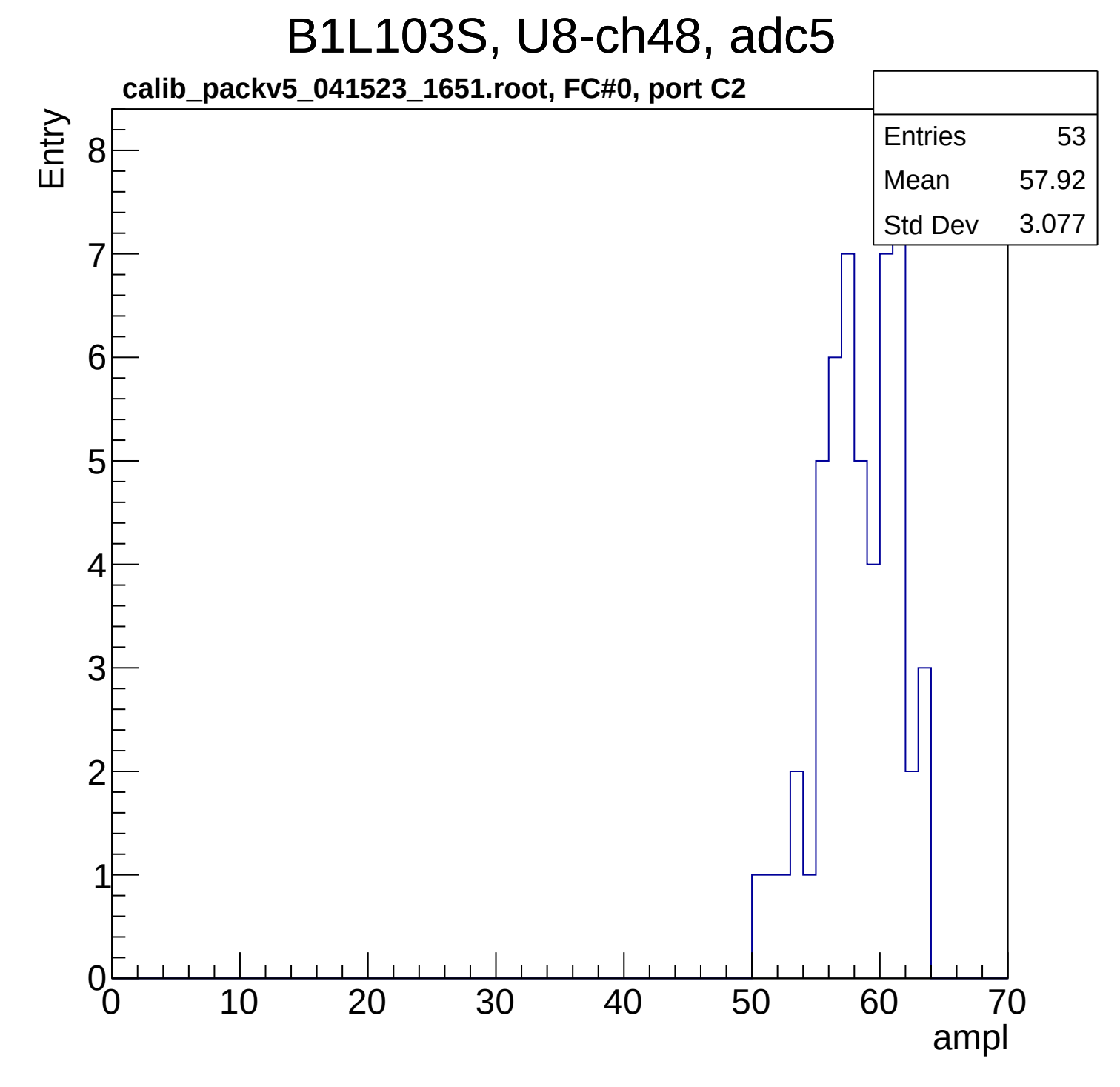
B1L103S, U8-ch48, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 57.92
Std Dev 3.077
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
50
60
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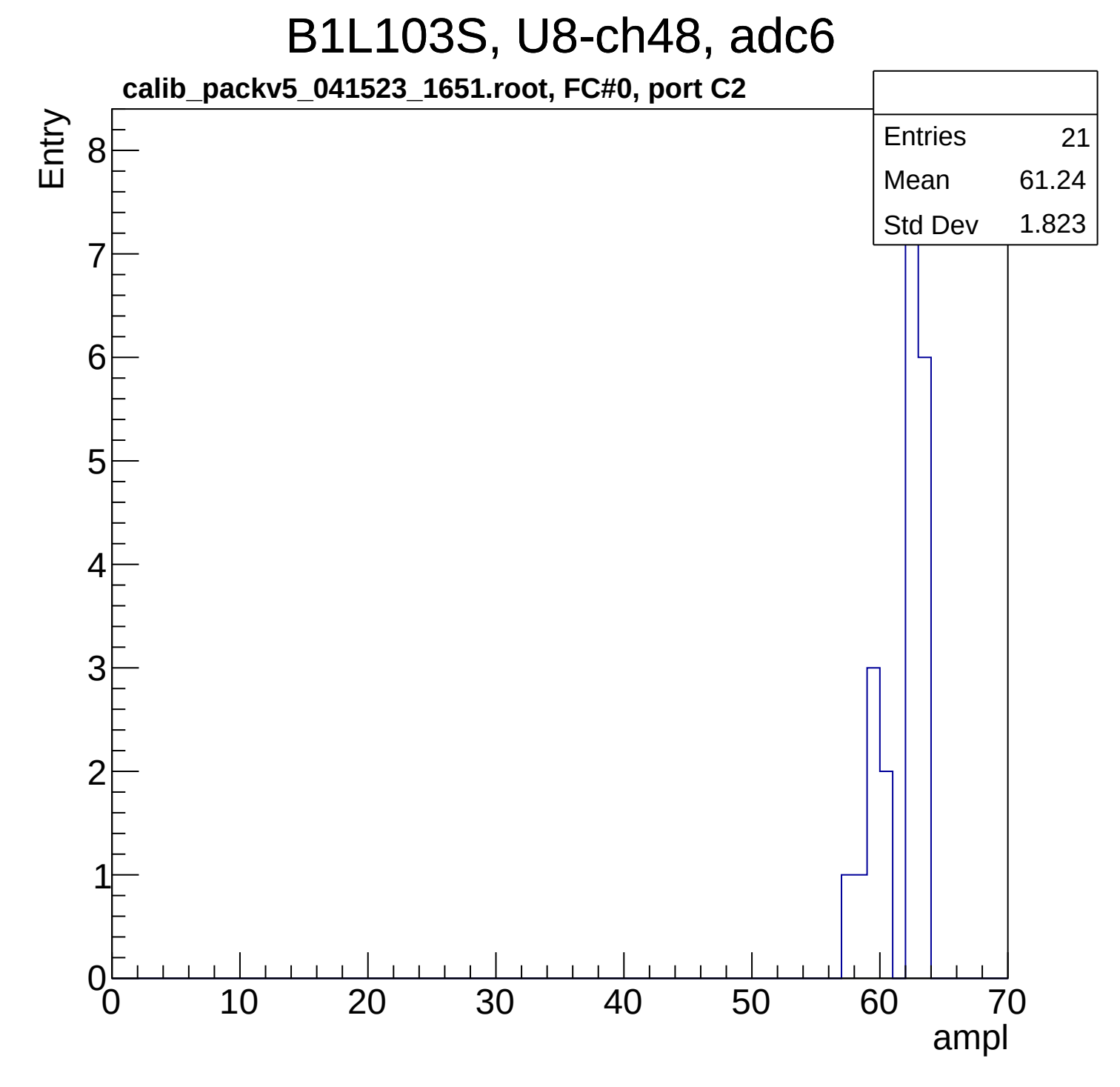
B1L103S, U8-ch48, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 61.24
Std Dev 1.823
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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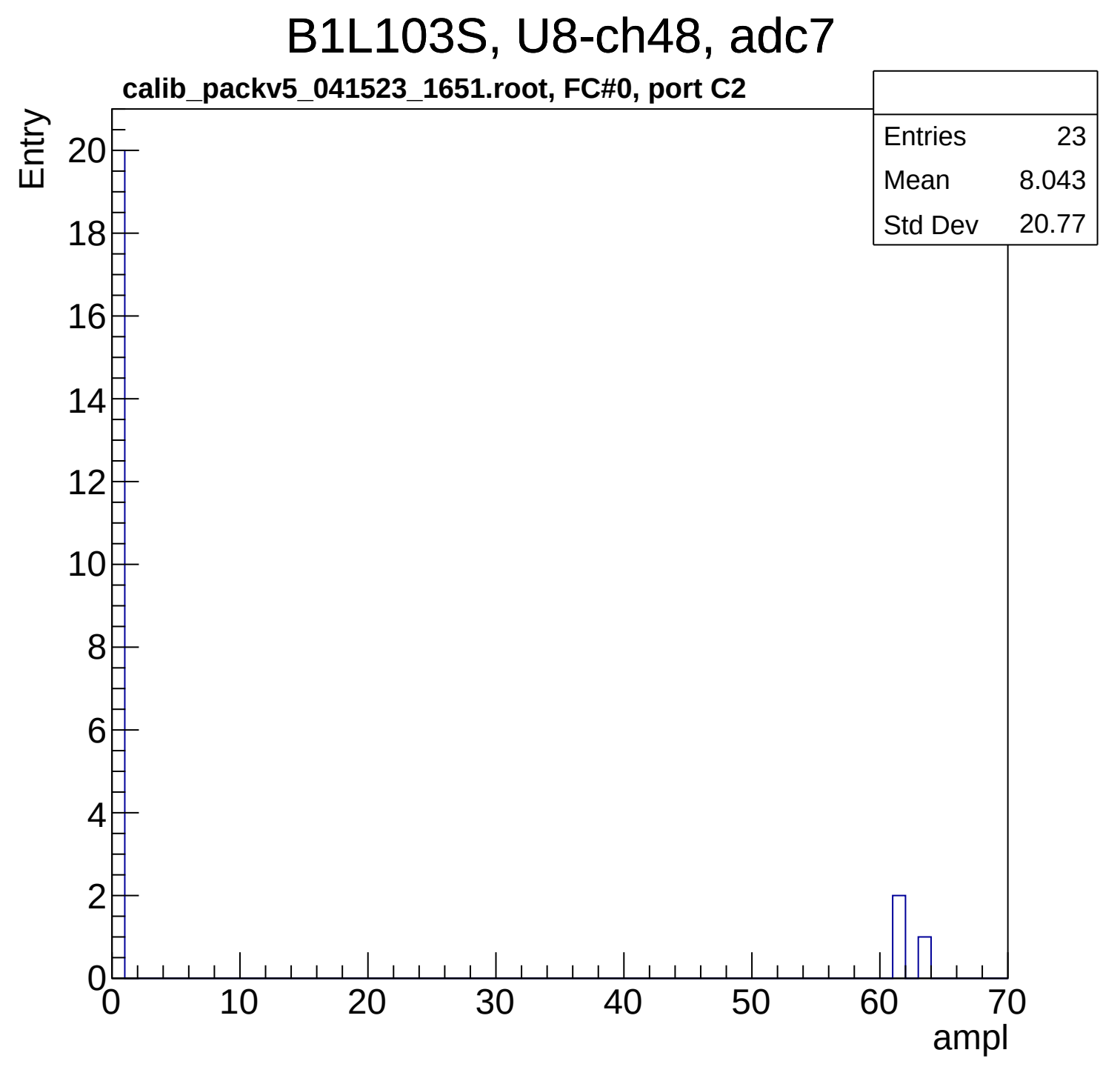
B1L103S, U8-ch48, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 8.043
Std Dev 20.77
Entry
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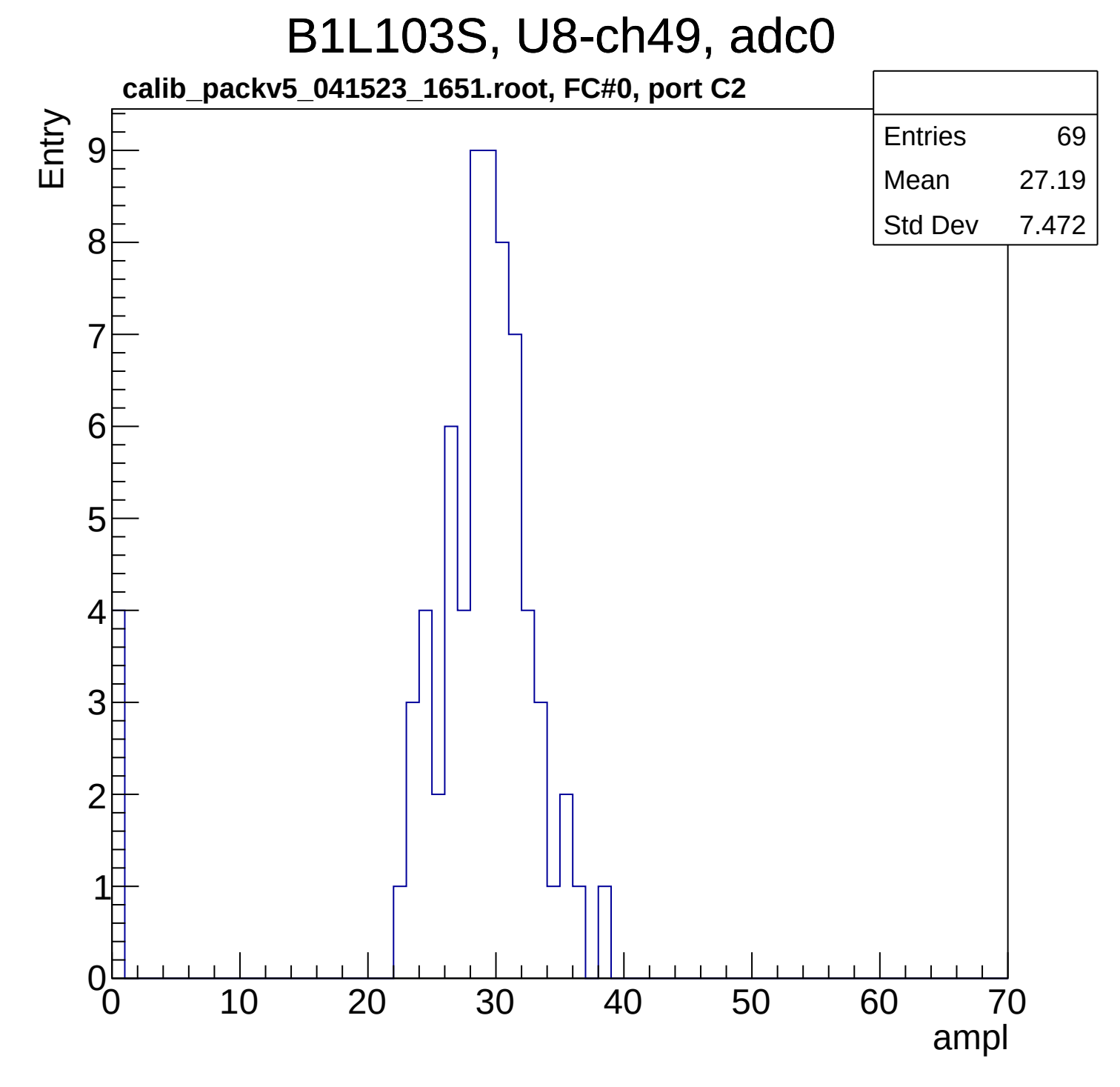
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch49, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 27.19
Std Dev 7.472
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
50
60
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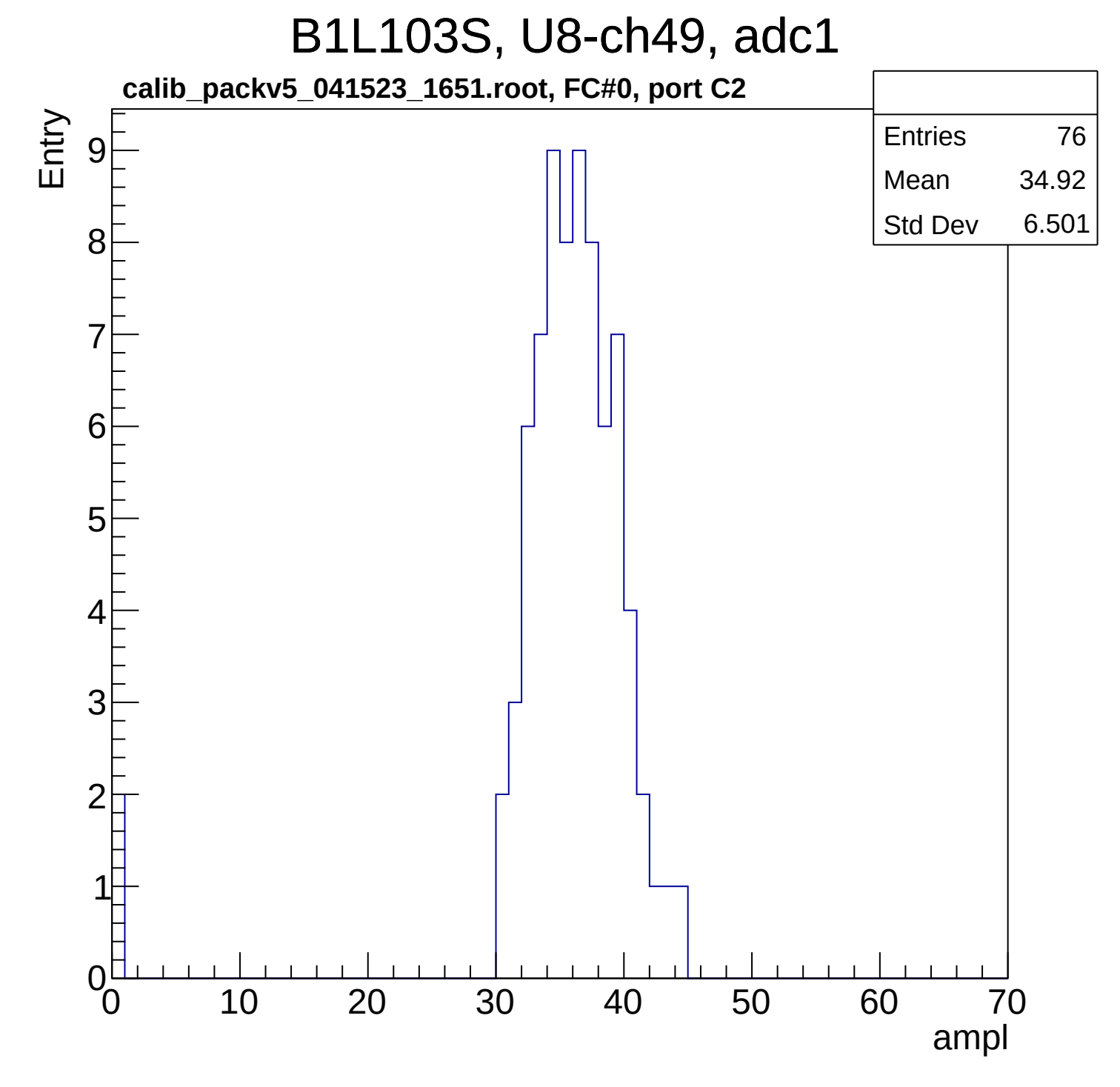
B1L103S, U8-ch49, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 34.92
Std Dev 6.501
Entry
ampl
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4
5
6
7
8
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0
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60
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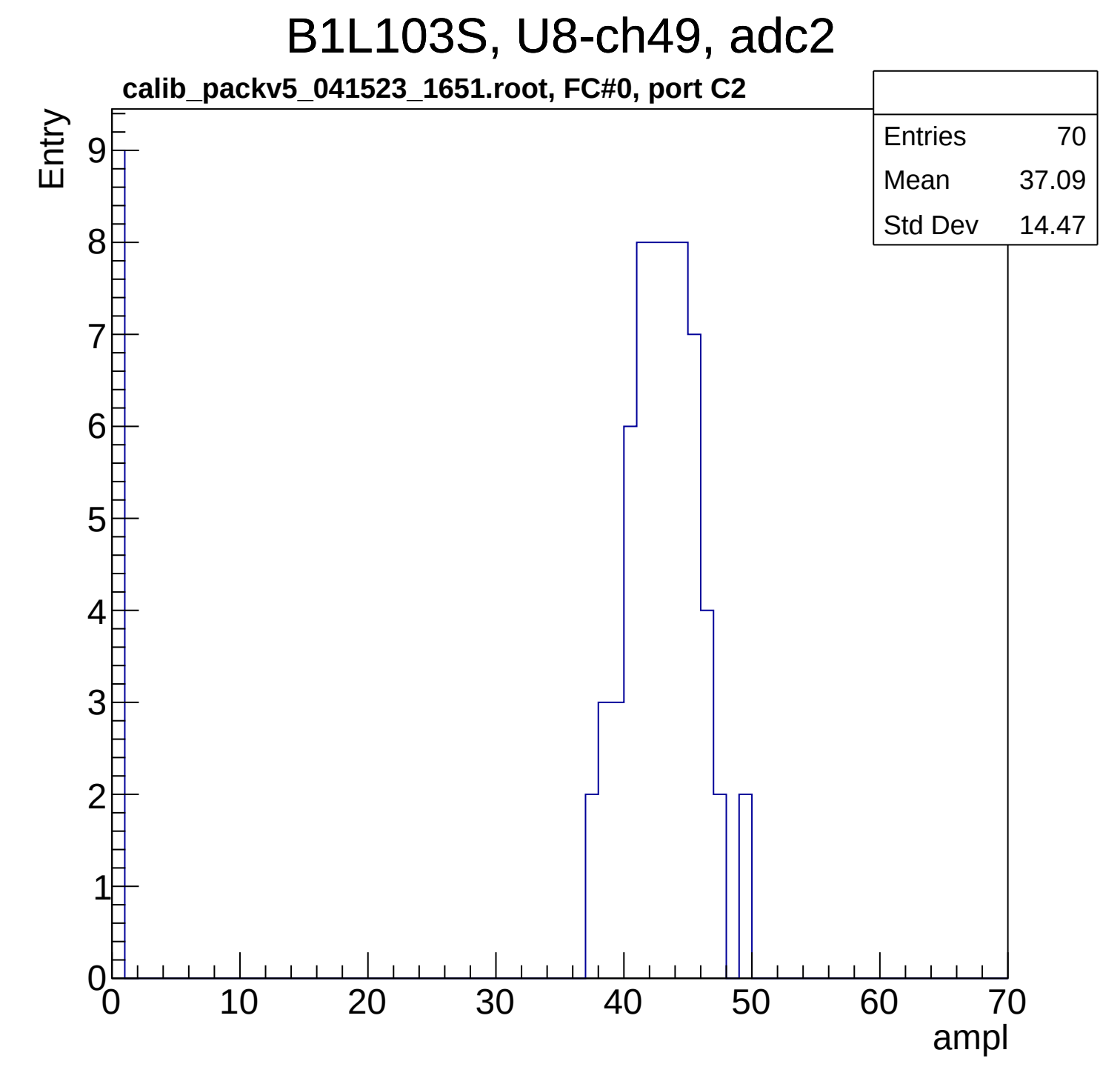
B1L103S, U8-ch49, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 37.09
Std Dev 14.47
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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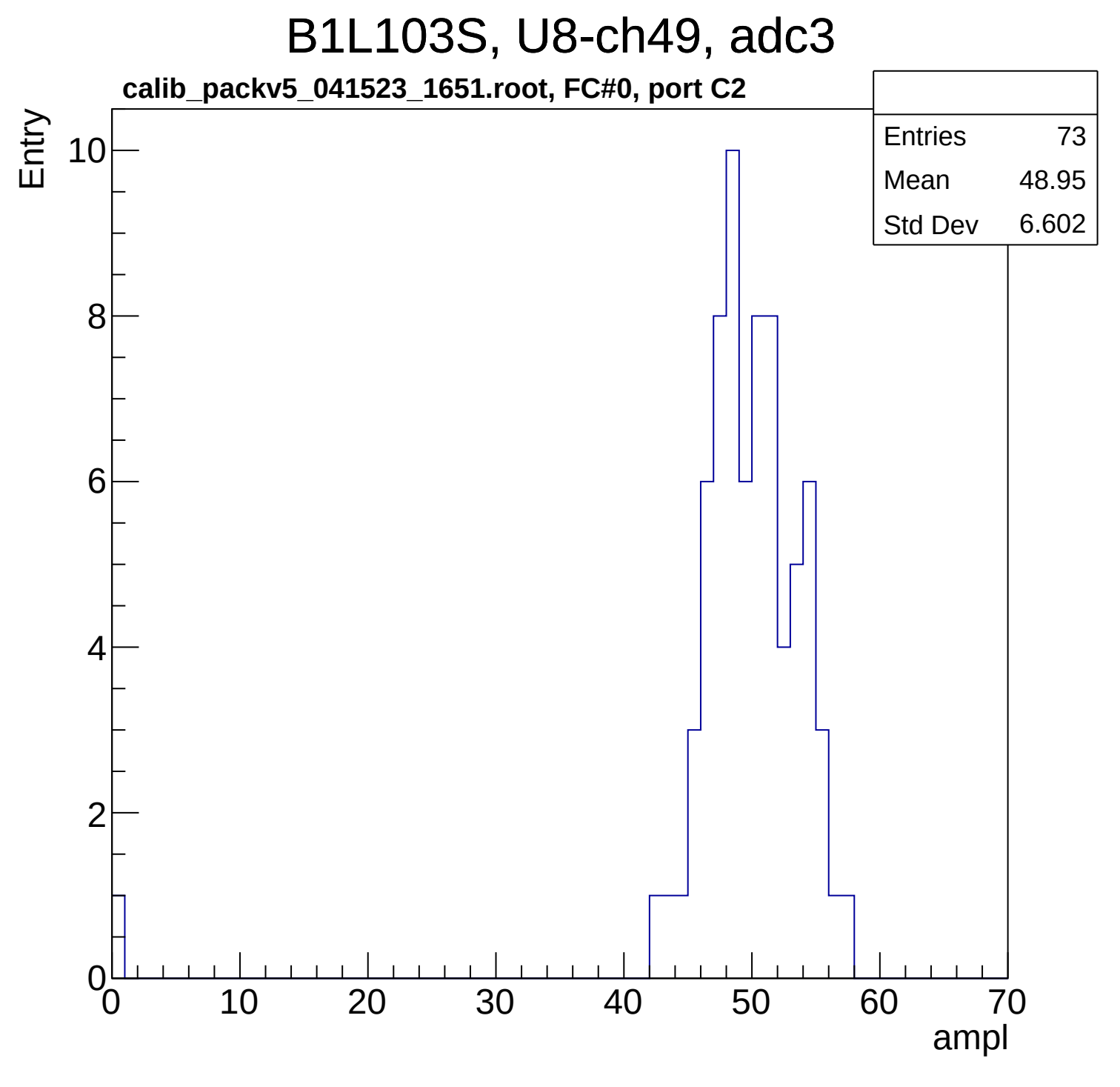
B1L103S, U8-ch49, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 48.95
Std Dev 6.602
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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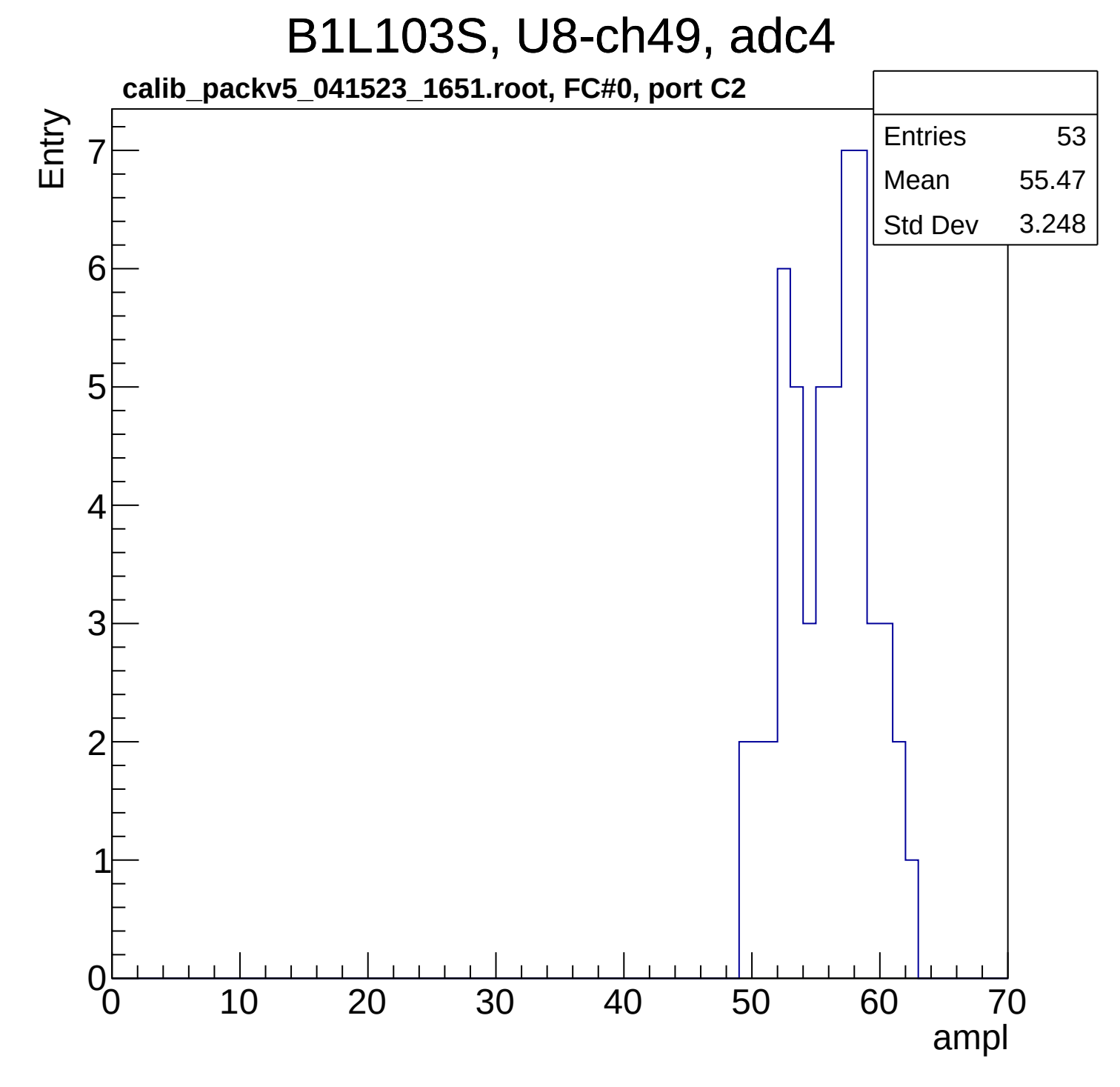
B1L103S, U8-ch49, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 55.47
Std Dev 3.248
Entry
ampl
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1
2
3
4
5
6
7
0
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20
30
40
50
60
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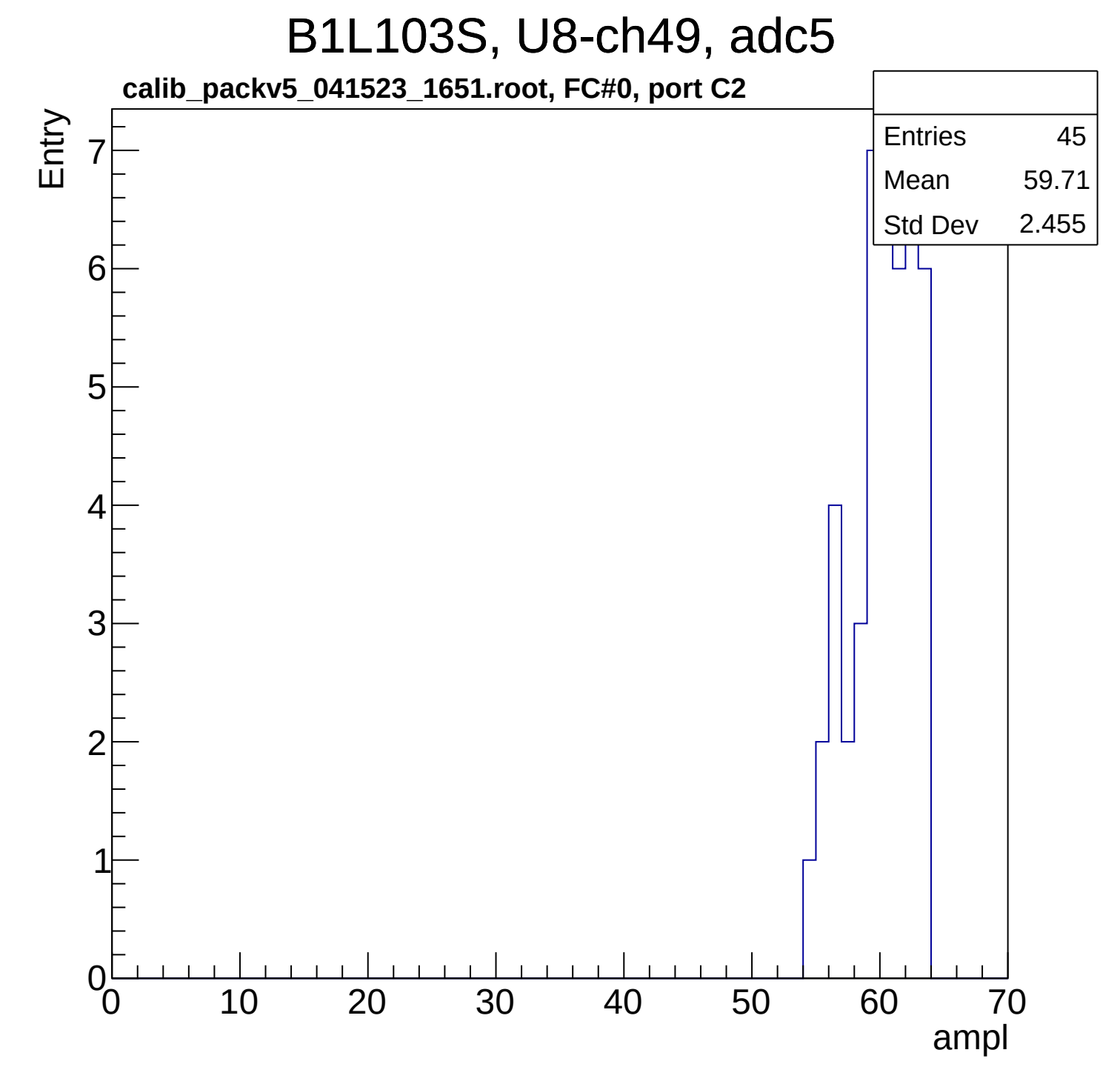
B1L103S, U8-ch49, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 59.71
Std Dev 2.455
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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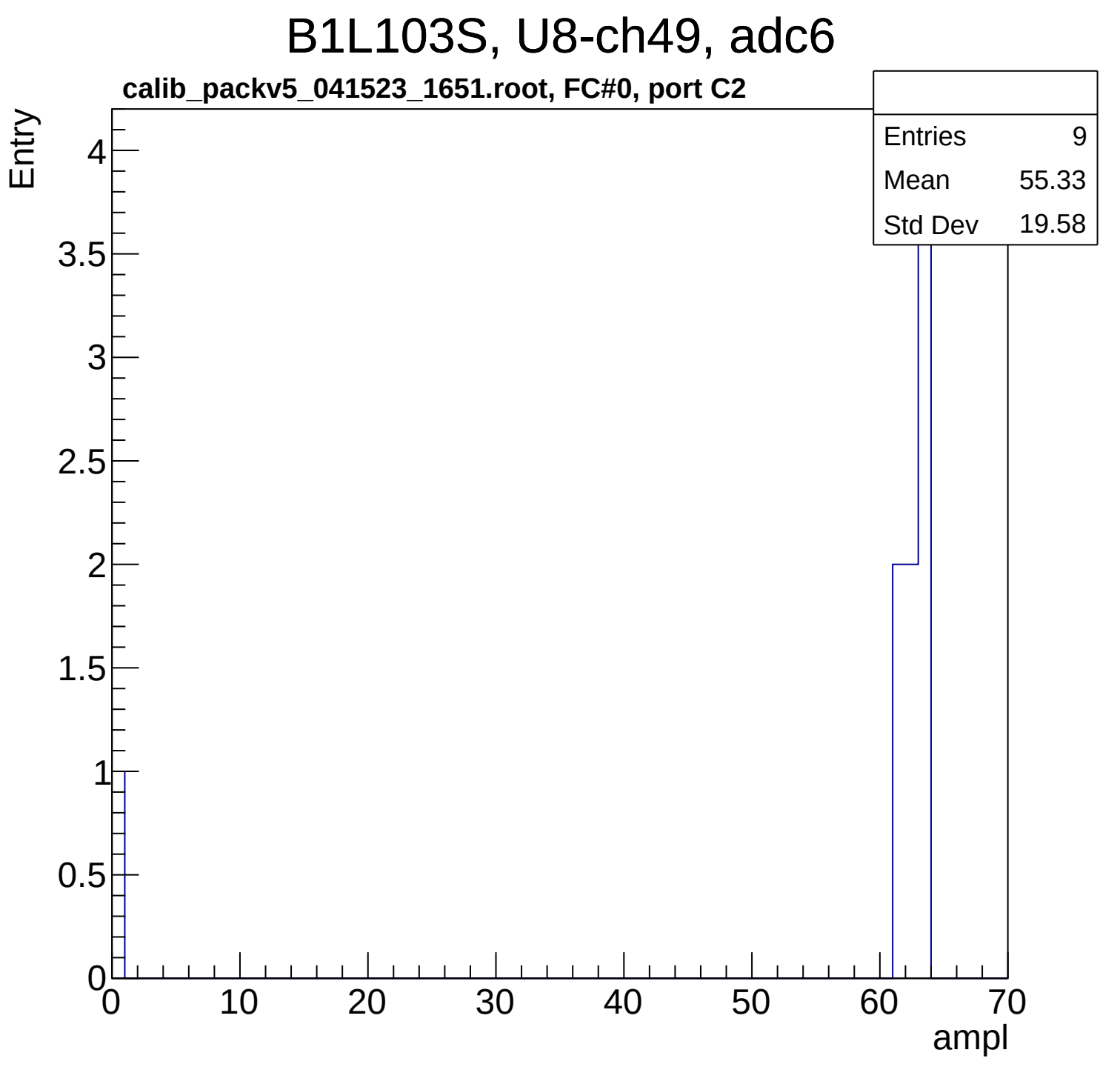
B1L103S, U8-ch49, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 55.33
Std Dev 19.58
Entry
ampl
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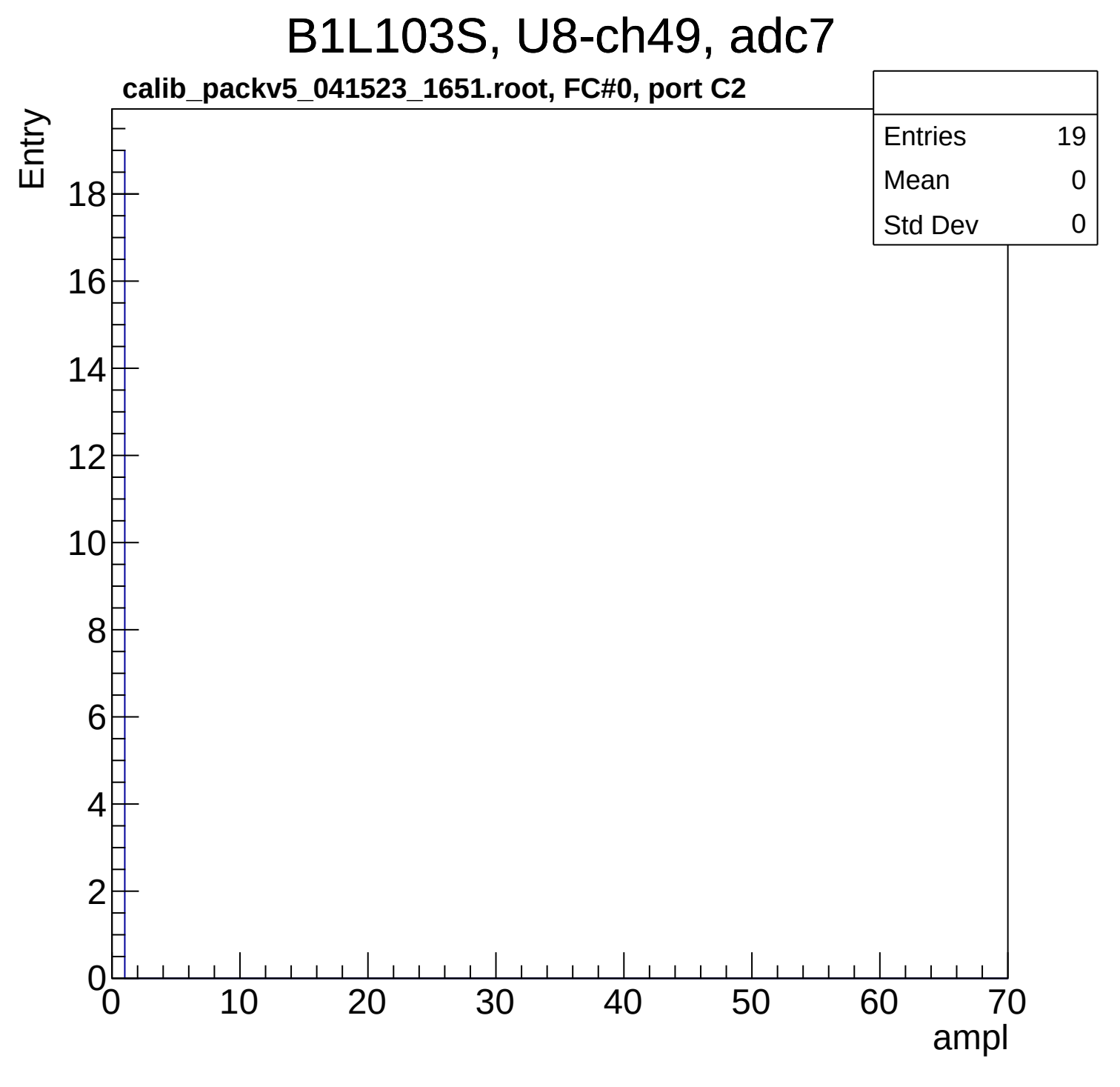
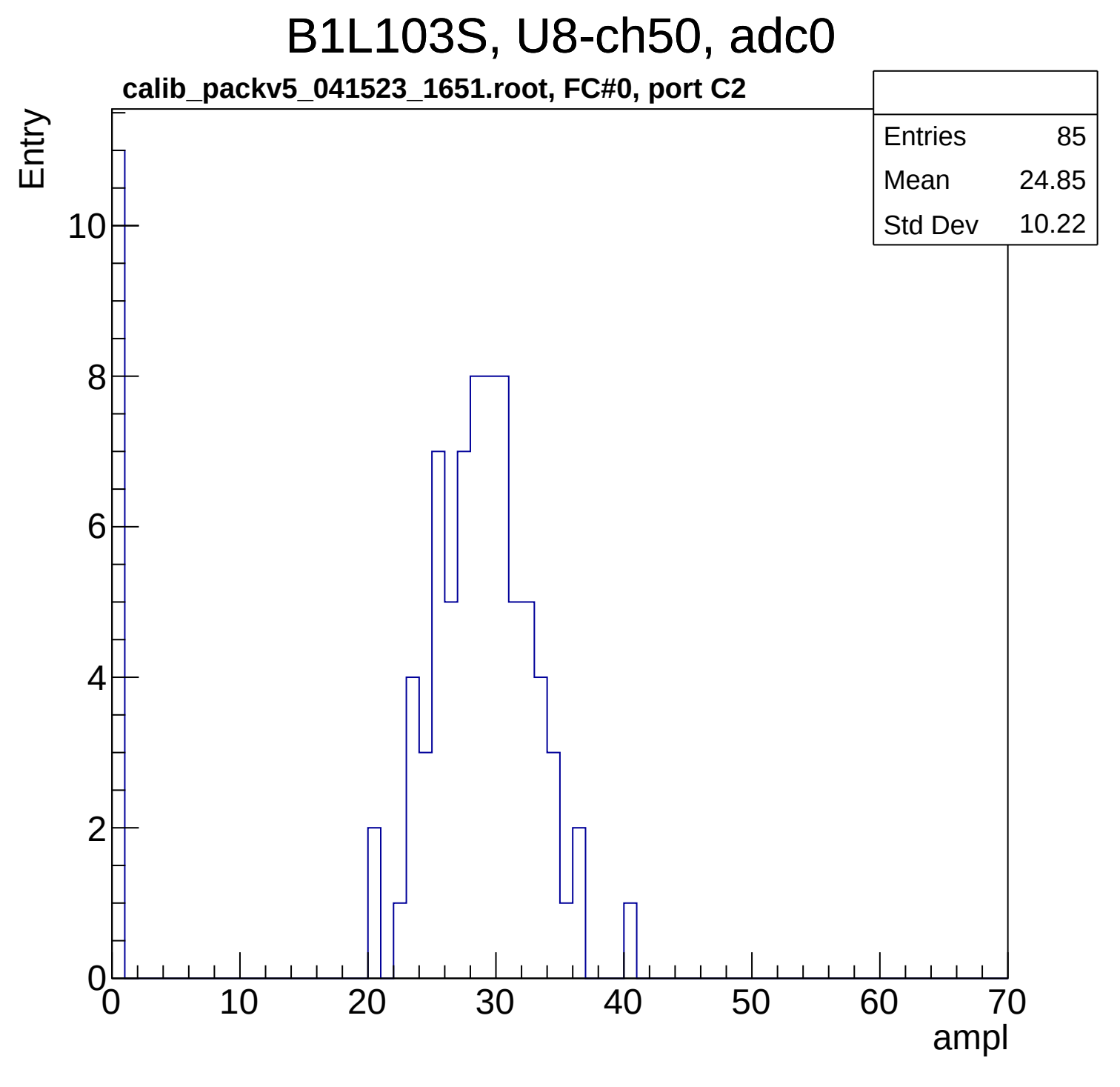
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U8-ch49, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch50, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 24.85
Std Dev 10.22
Entry
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8
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10
20
30
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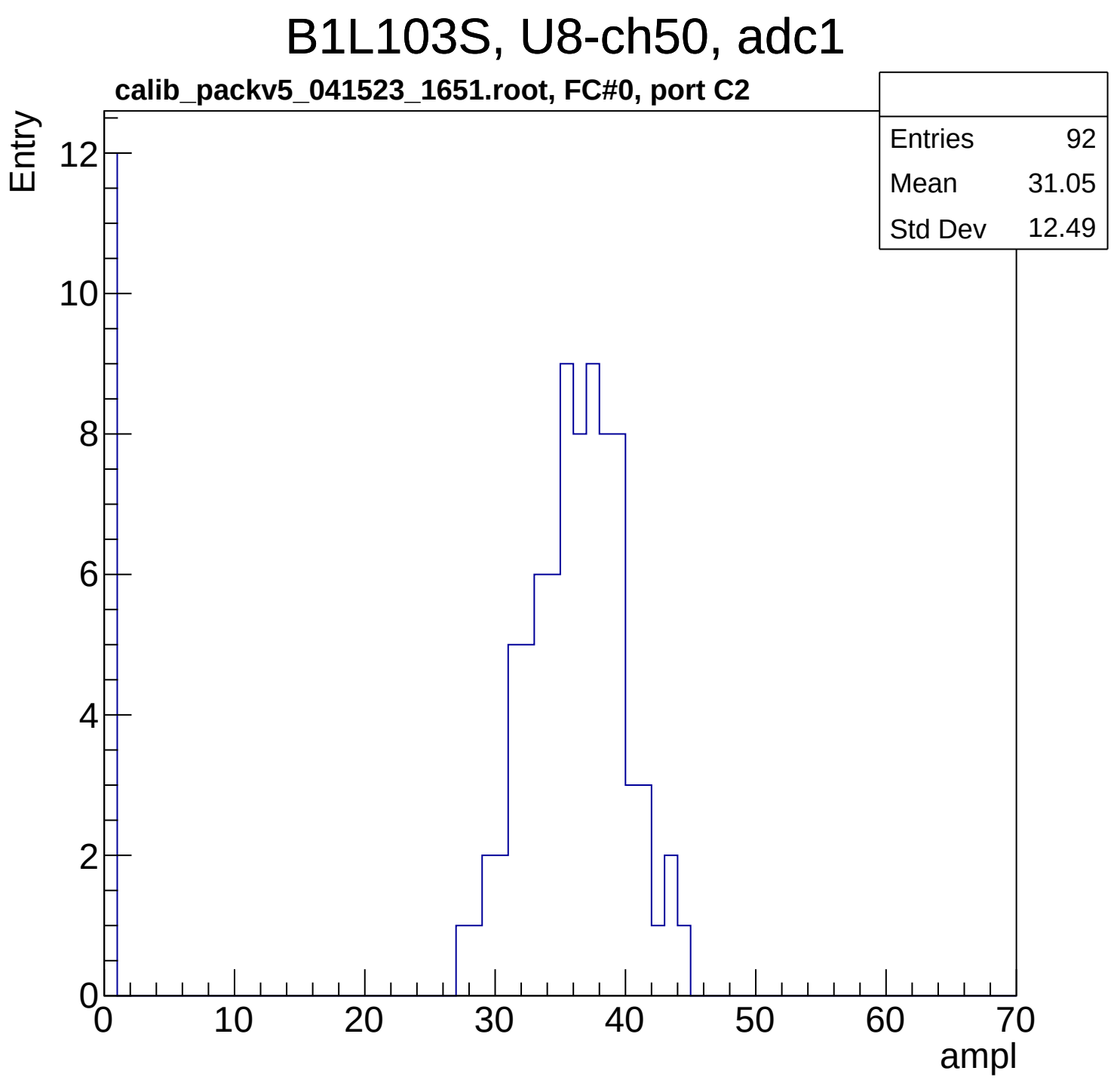
50
60
70
ampl


B1L103S, U8-ch50, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 31.05
Std Dev 12.49
Entry
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4
6
8
10
12
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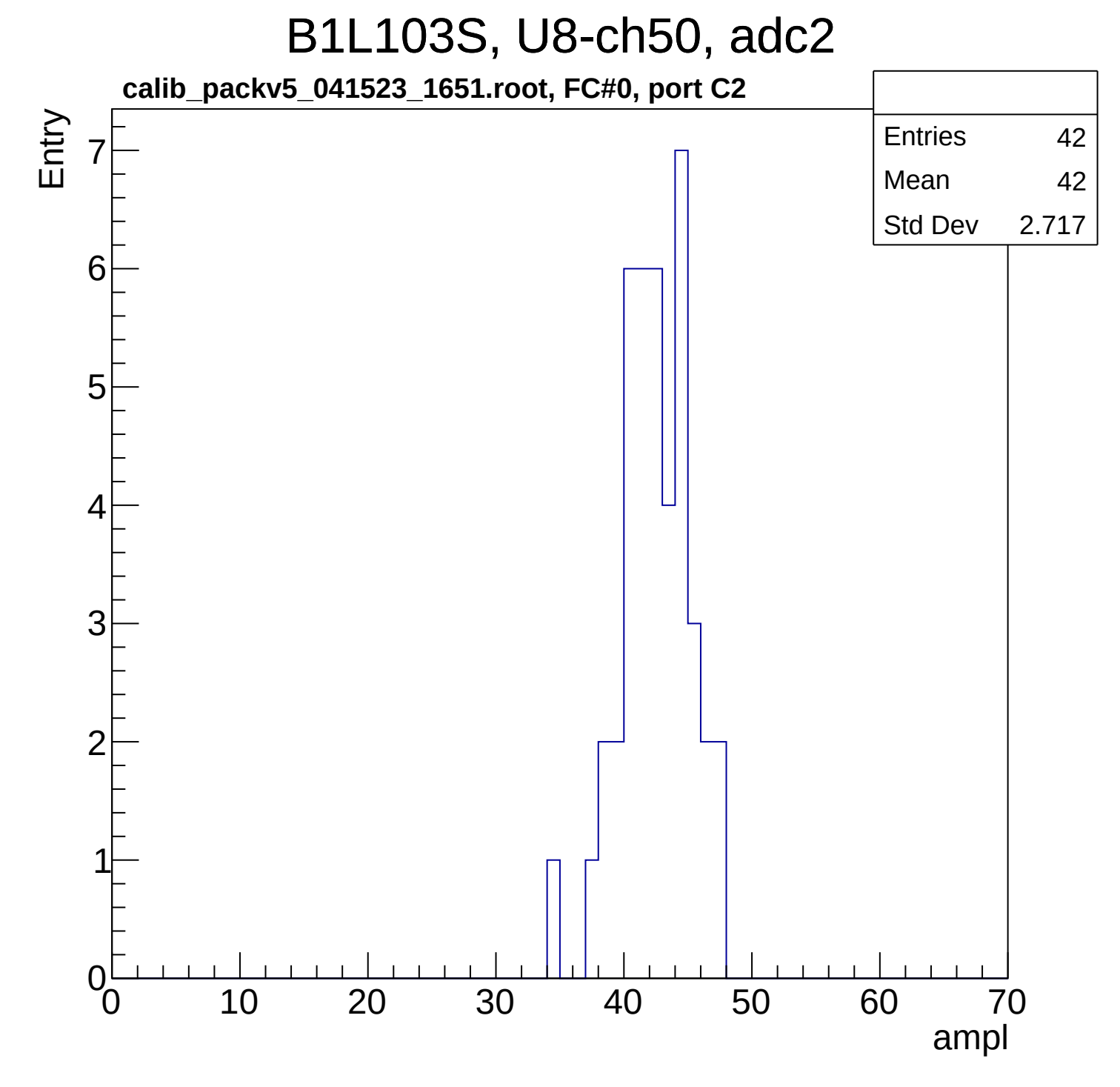
60
70
ampl


B1L103S, U8-ch50, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 42
Std Dev 2.717
Entry
ampl
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2
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4
5
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0
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60
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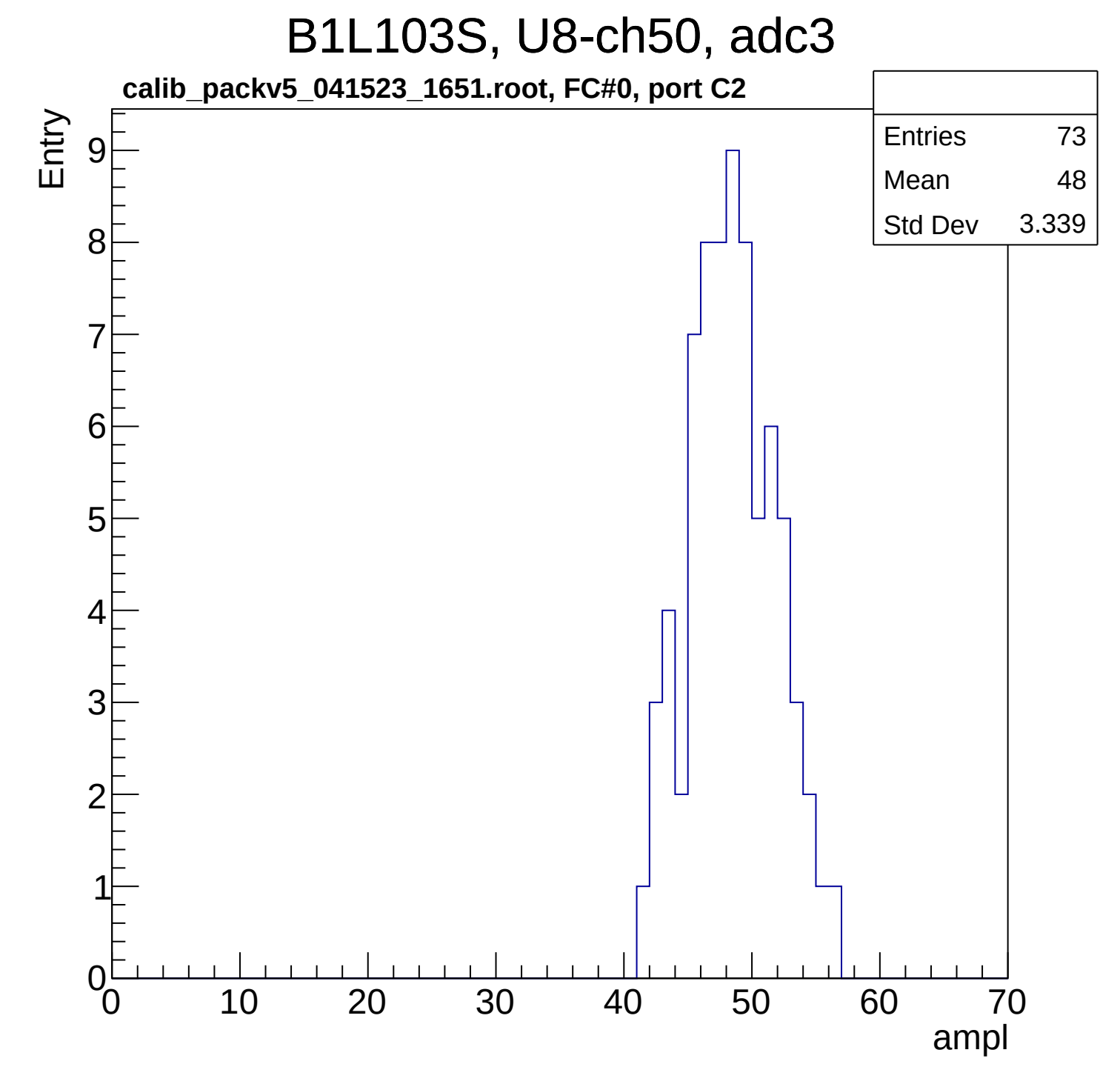
B1L103S, U8-ch50, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 48
Std Dev 3.339
Entry
ampl
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4
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7
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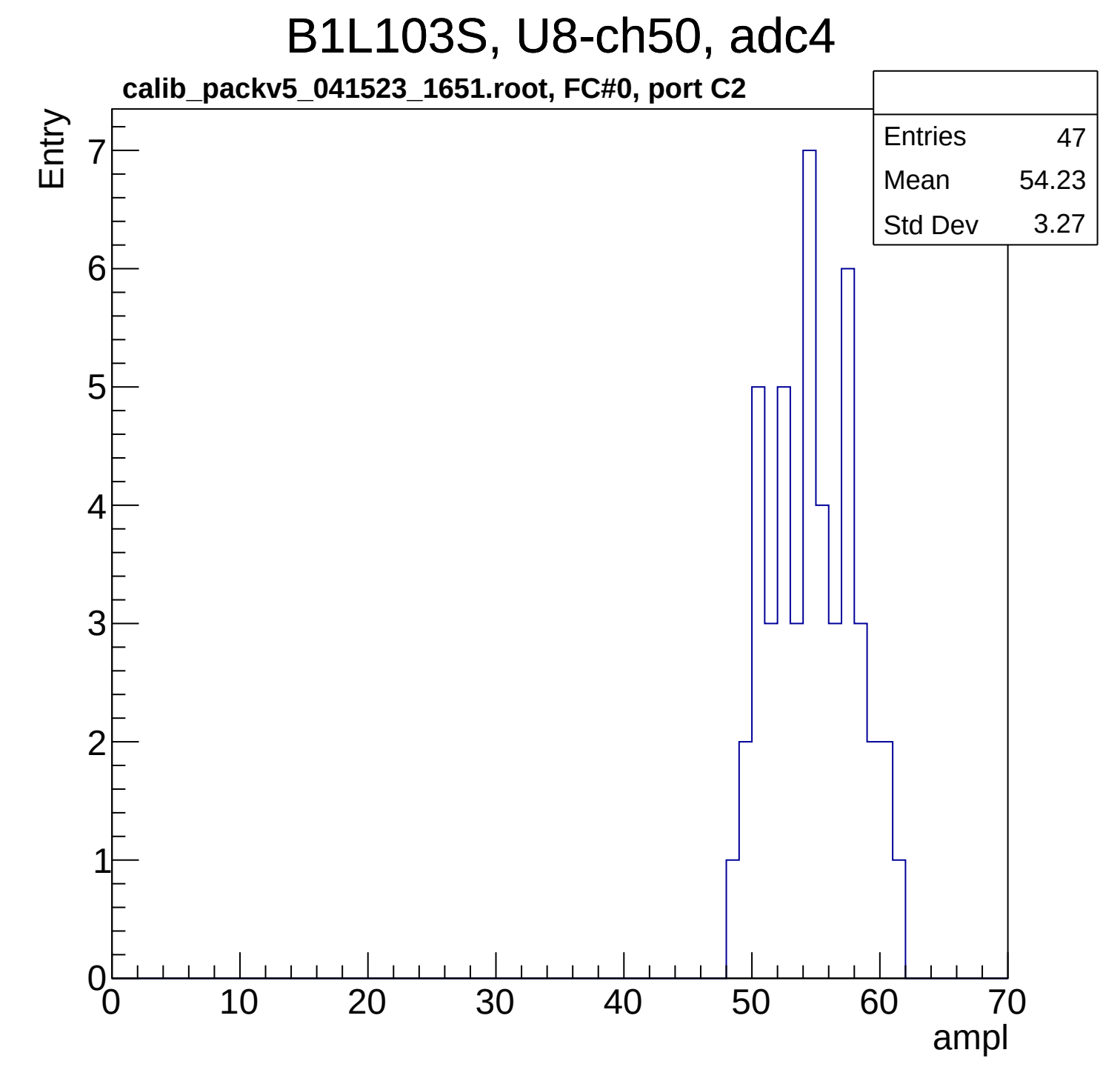
B1L103S, U8-ch50, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 54.23
Std Dev 3.27
Entry
ampl
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3
4
5
6
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0
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40
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60
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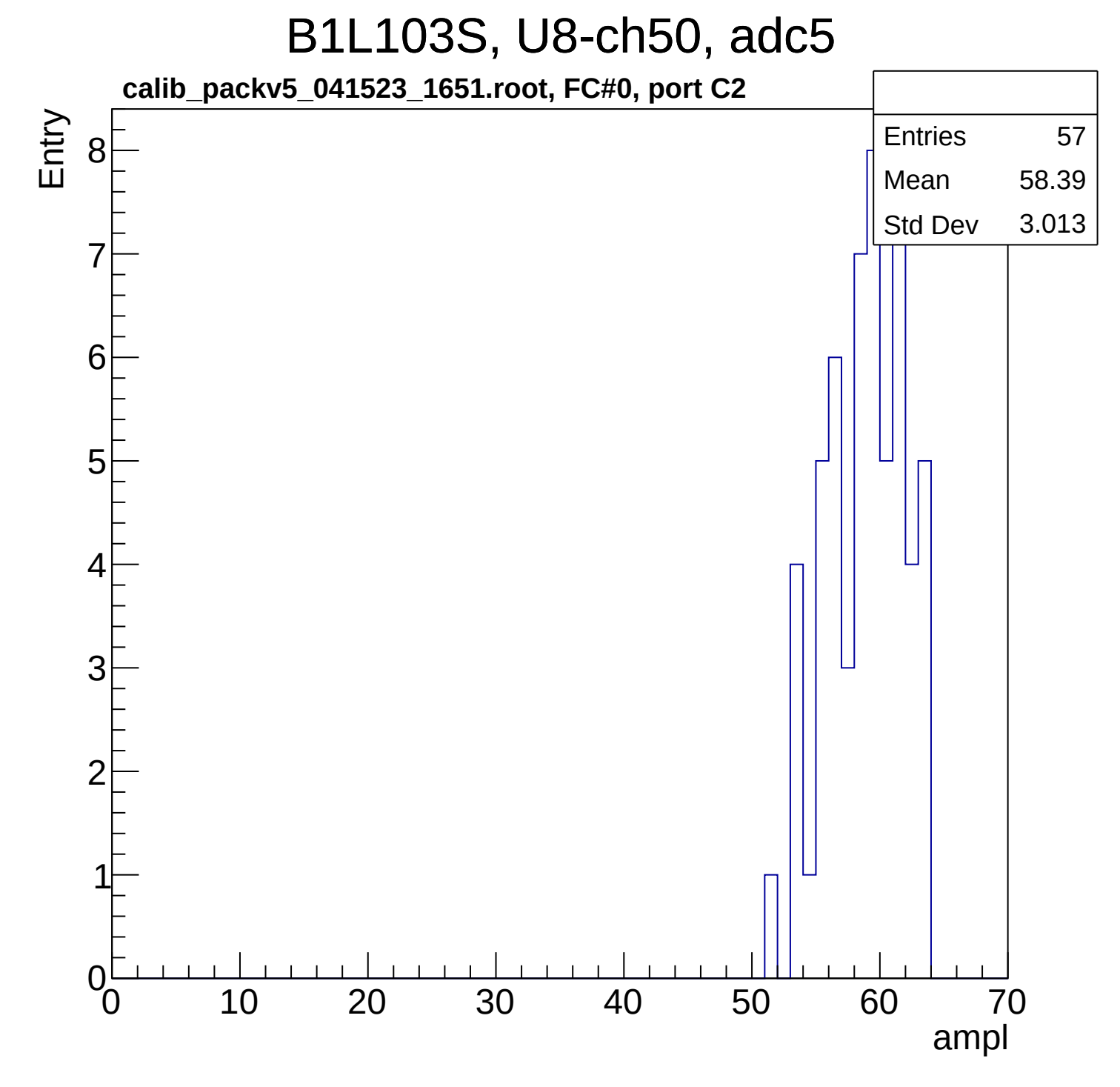
B1L103S, U8-ch50, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 58.39
Std Dev 3.013
Entry
ampl
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2
3
4
5
6
7
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0
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60
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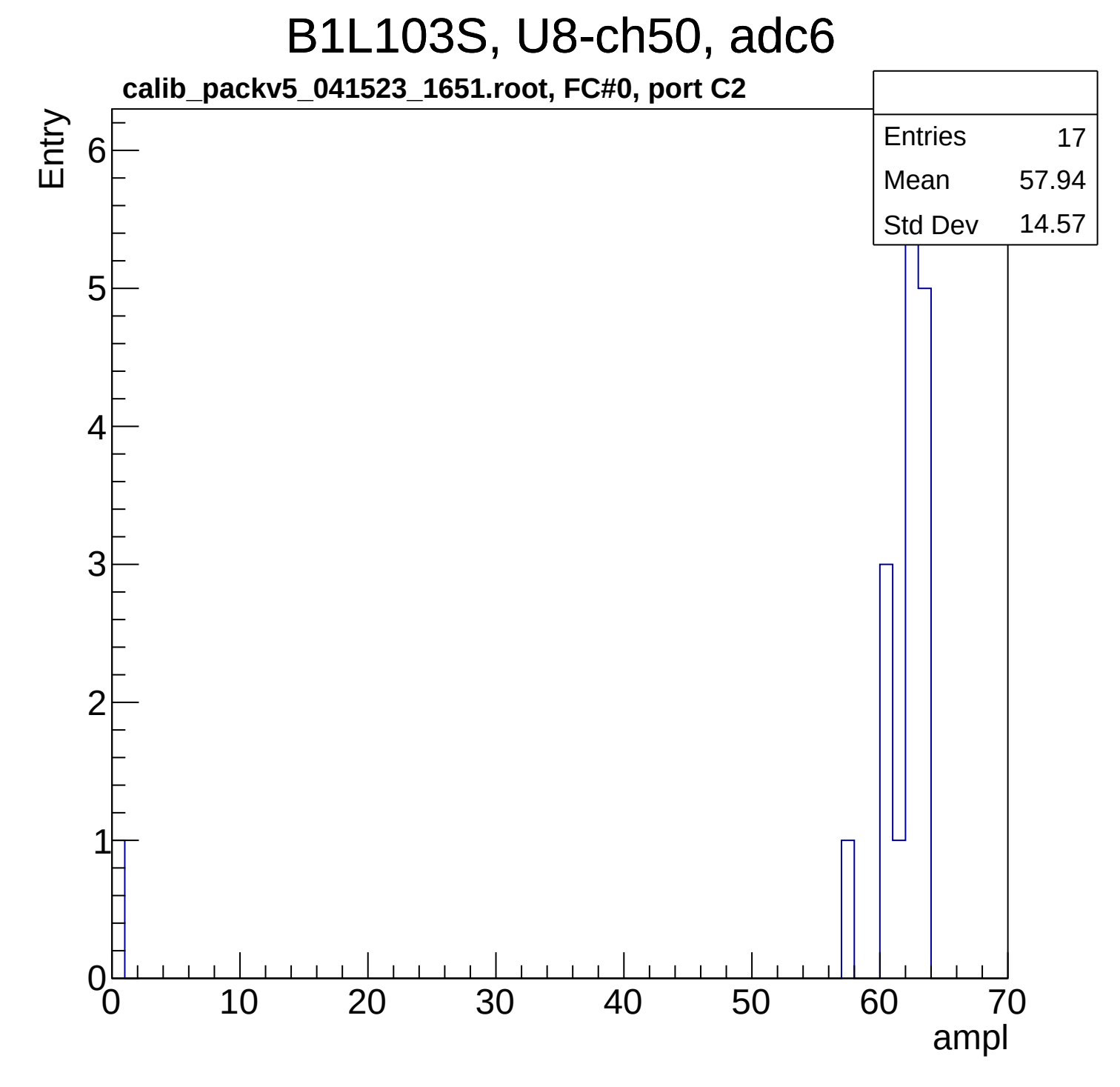
B1L103S, U8-ch50, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 57.94
Std Dev 14.57
Entry
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2
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4
5
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0
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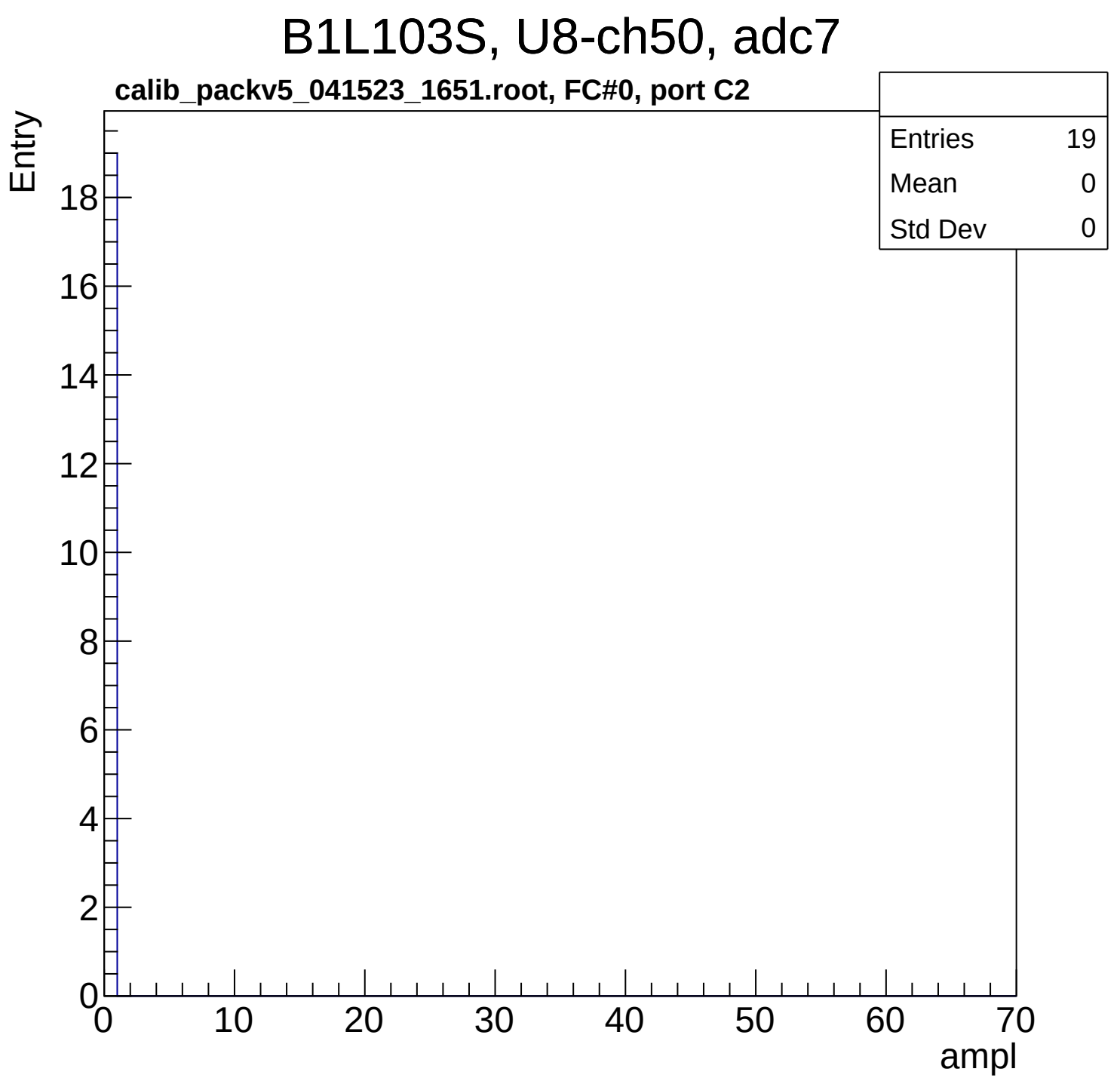
60
70
ampl


B1L103S, U8-ch50, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
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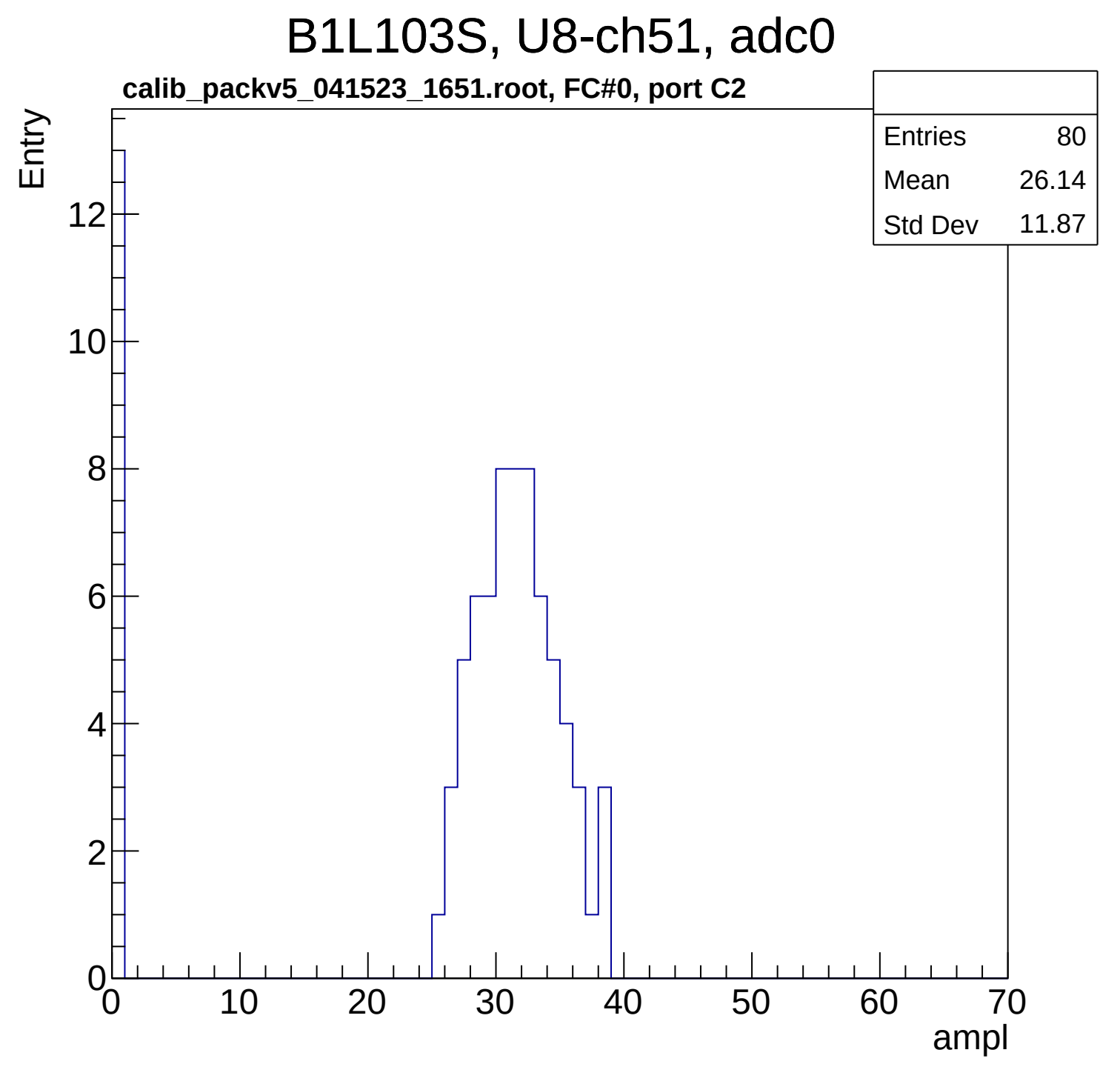
50
60
70
ampl


B1L103S, U8-ch51, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 26.14
Std Dev 11.87
Entry
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10
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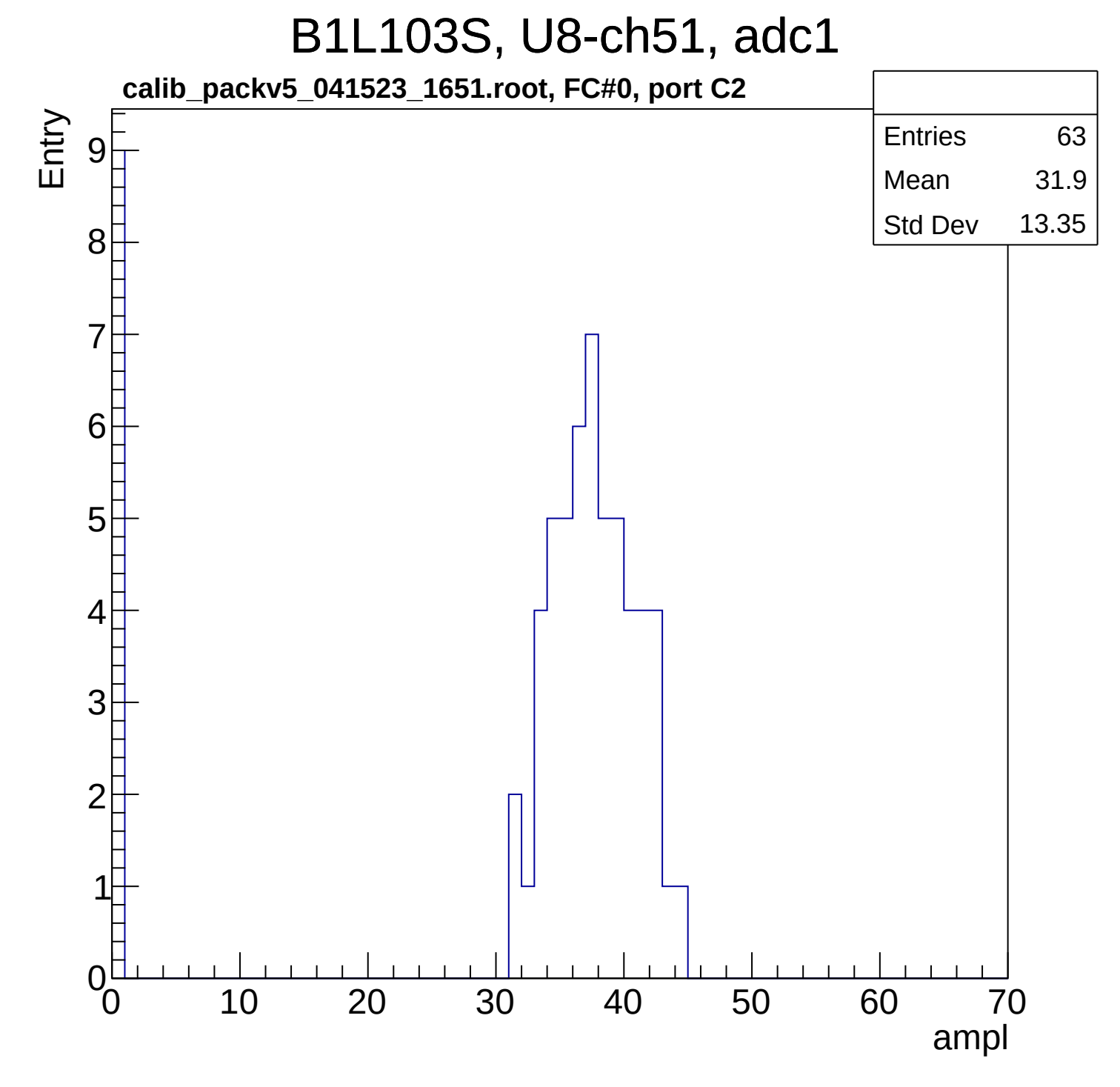
70
ampl


B1L103S, U8-ch51, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 31.9
Std Dev 13.35
Entry
ampl
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3
4
5
6
7
8
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0
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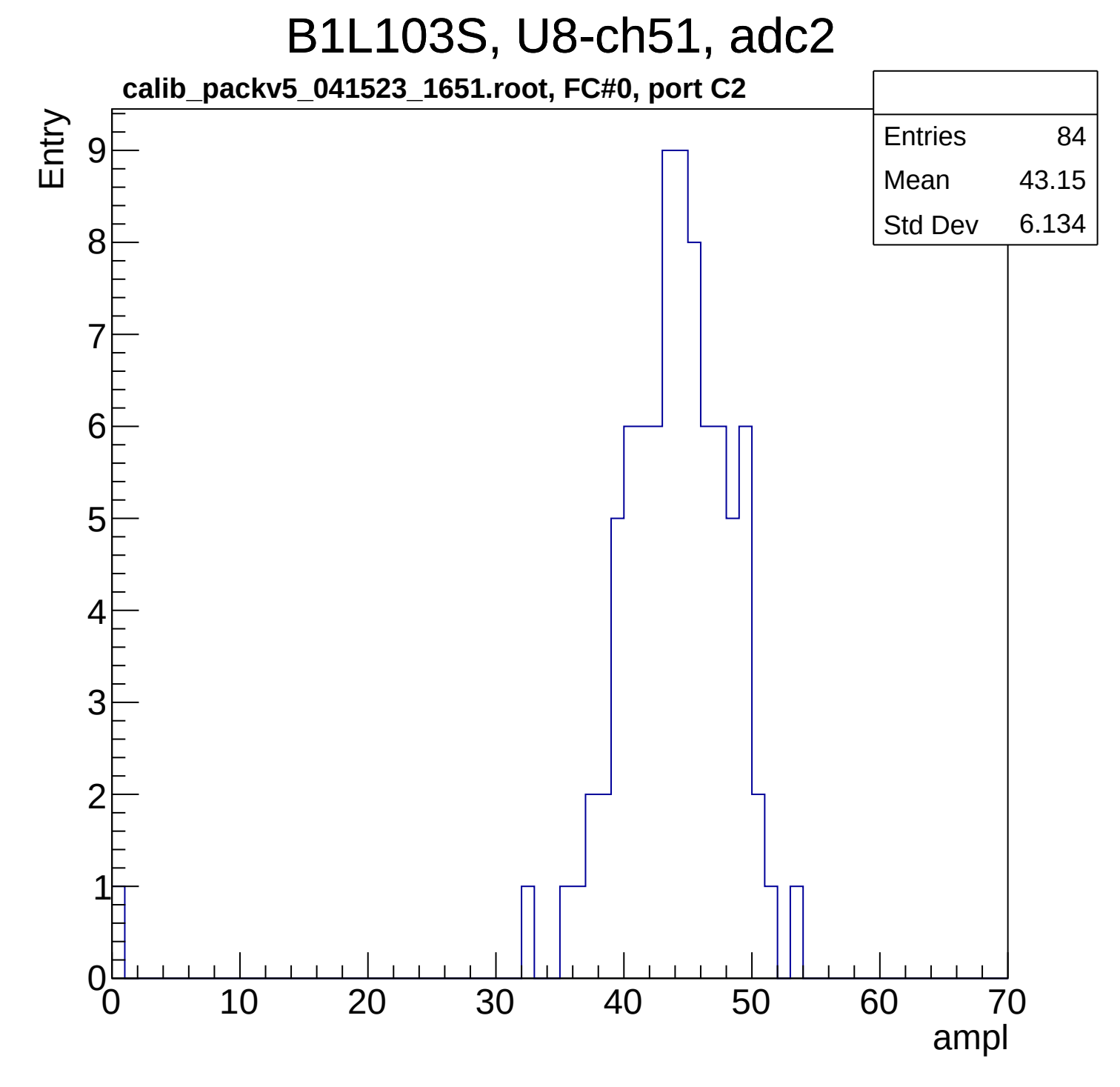
B1L103S, U8-ch51, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 43.15
Std Dev 6.134
Entry
ampl
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4
5
6
7
8
9
0
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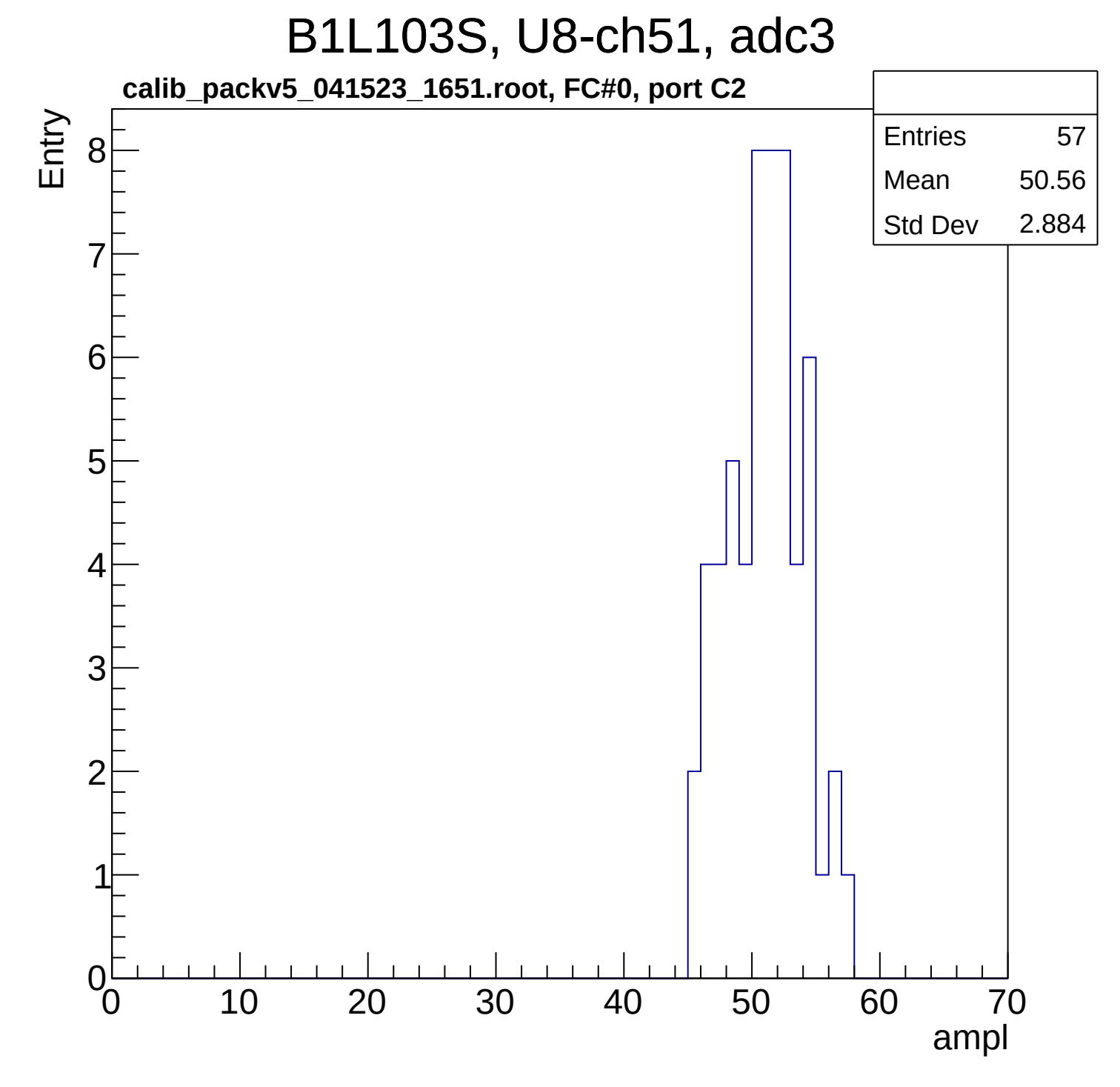
B1L103S, U8-ch51, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 50.56
Std Dev 2.884
Entry
ampl
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4
5
6
7
8
0
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20
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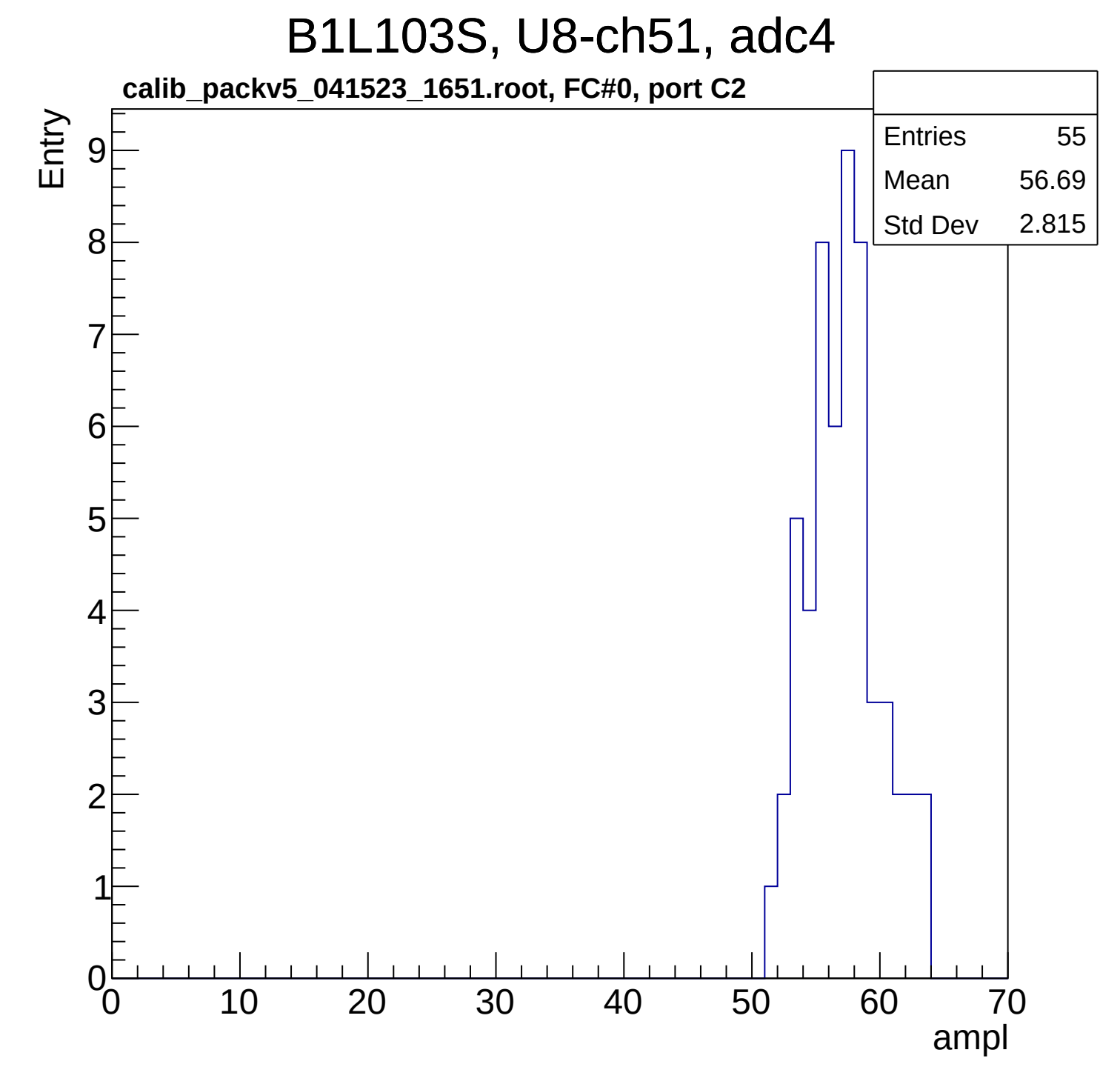
B1L103S, U8-ch51, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 56.69
Std Dev 2.815
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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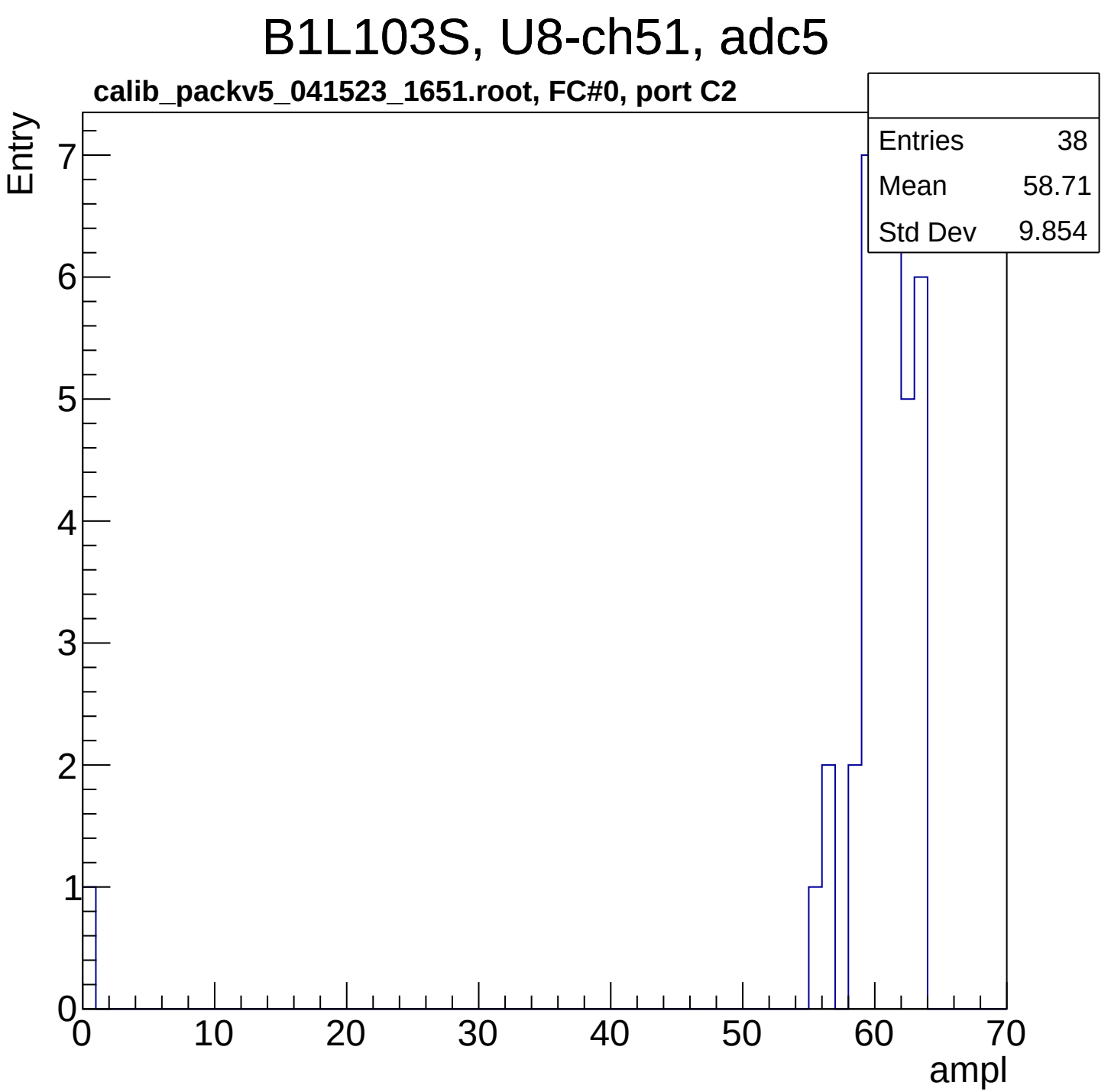
B1L103S, U8-ch51, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 58.71
Std Dev 9.854
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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60
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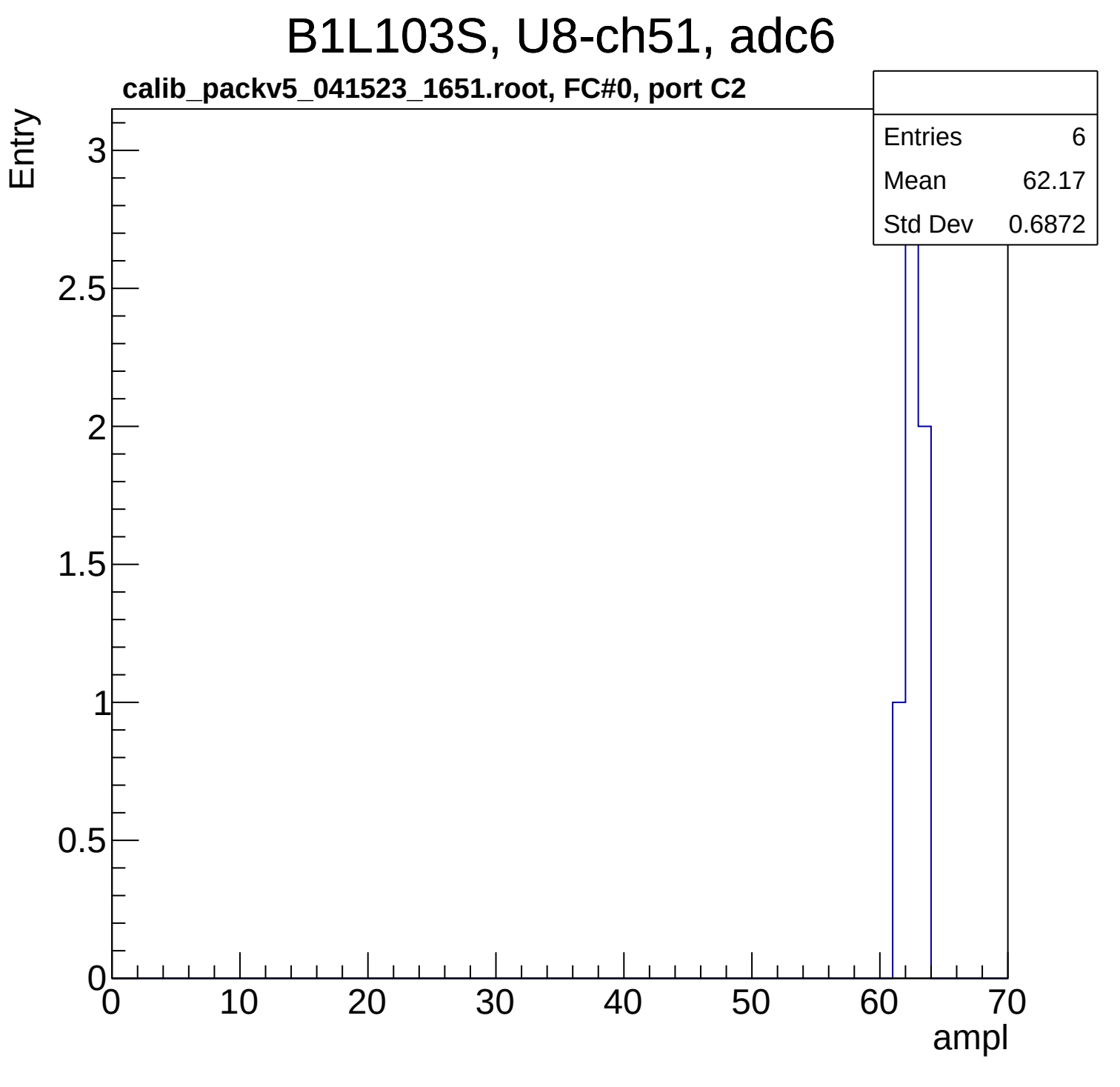
B1L103S, U8-ch51, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 62.17
Std Dev 0.6872
Entry
ampl
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0.5
1
1.5
2
2.5
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0
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60
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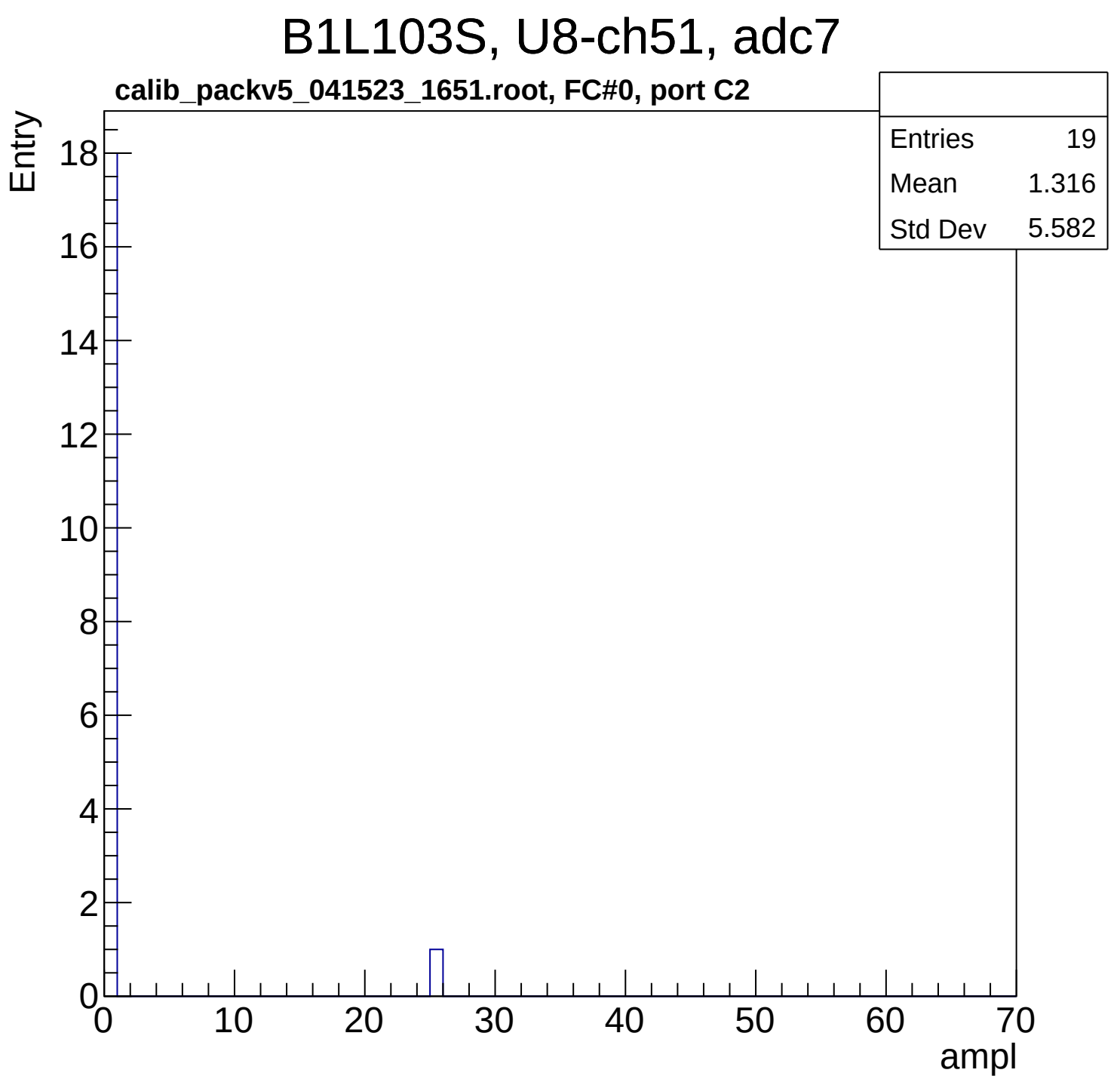
B1L103S, U8-ch51, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.316
Std Dev 5.582
Entry
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10
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14
16
18
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10
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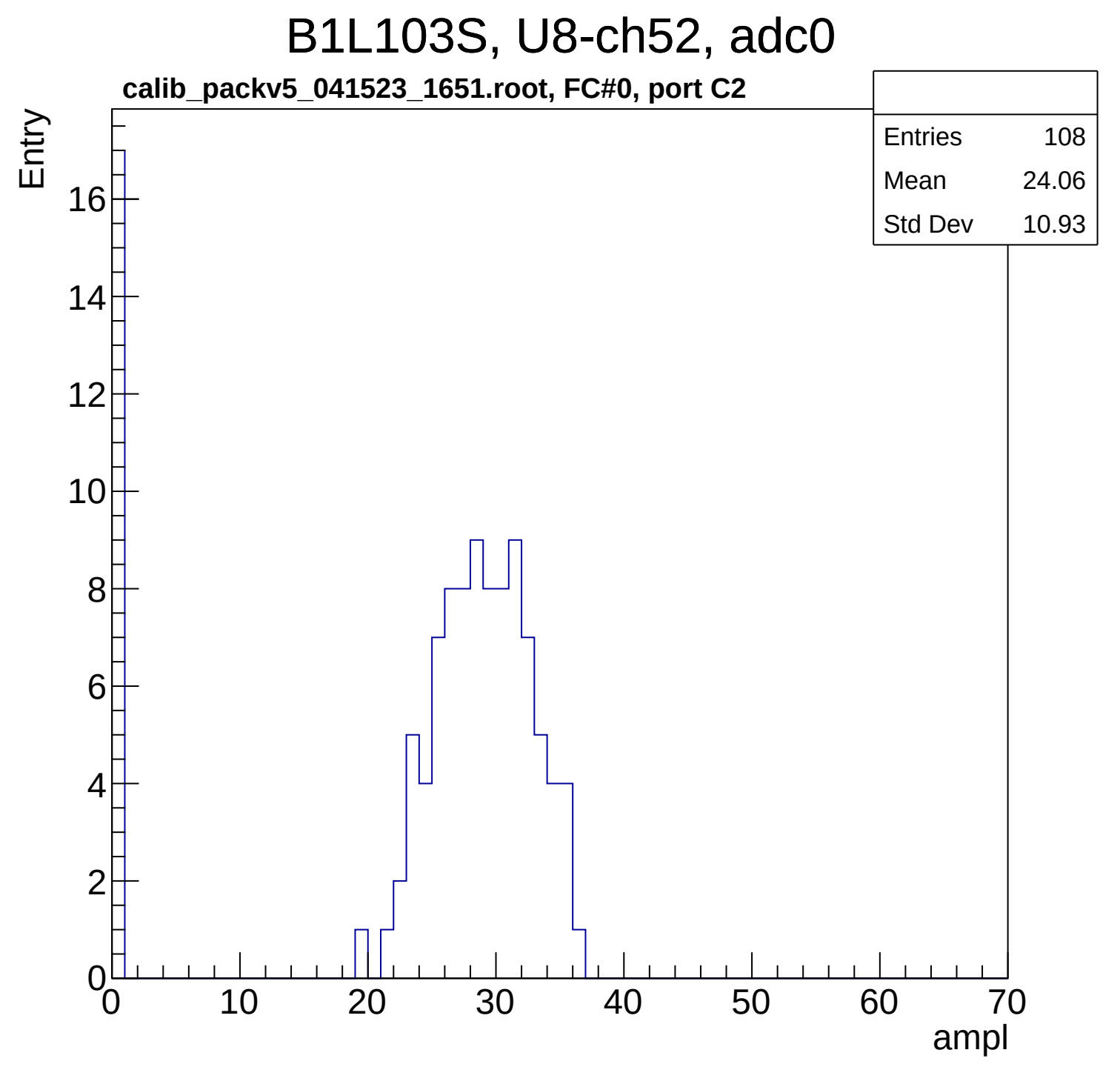
50
60
70
ampl


B1L103S, U8-ch52, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 108
Mean 24.06
Std Dev 10.93
Entry
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6
8
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12
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16
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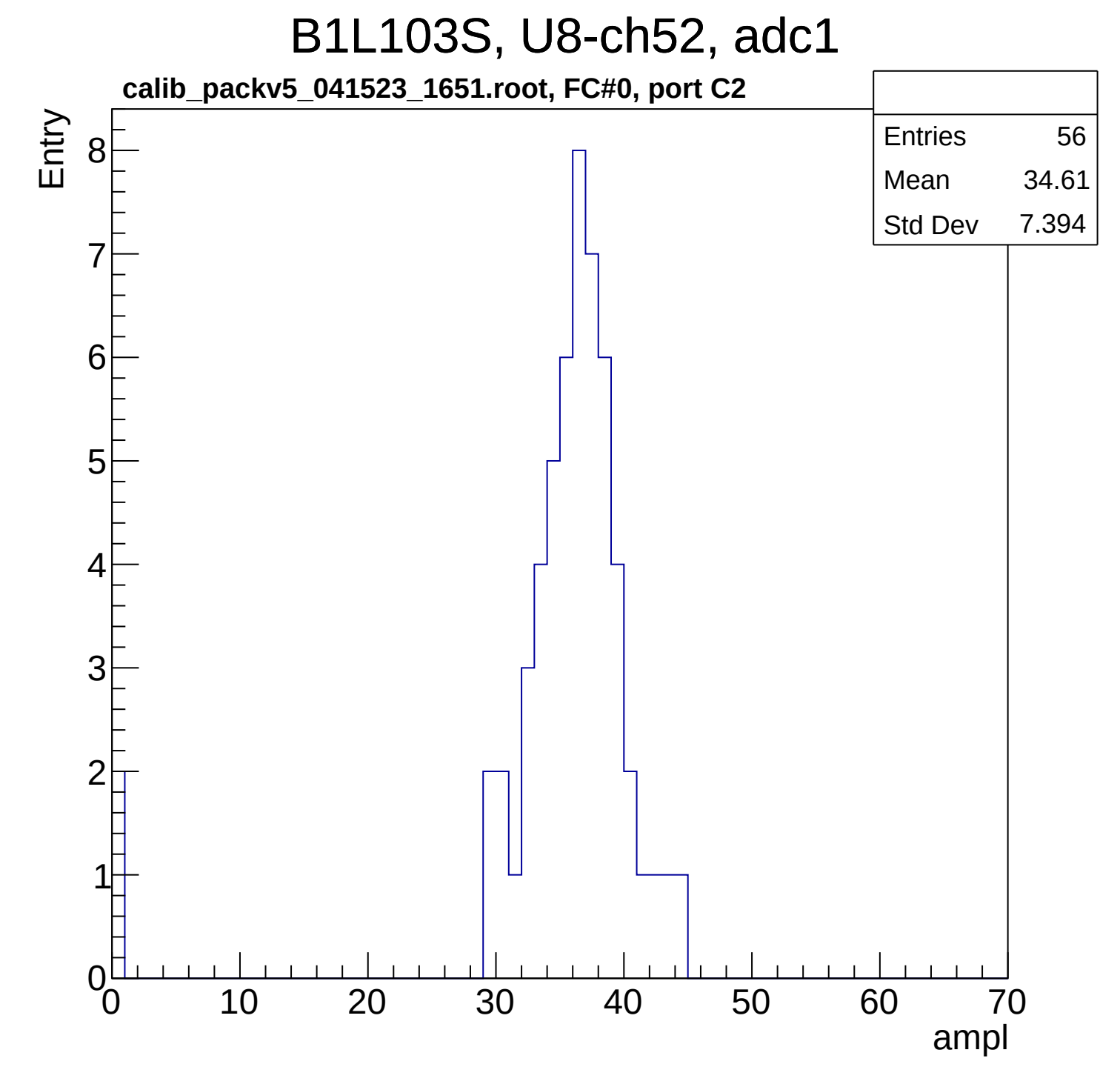
70
ampl


B1L103S, U8-ch52, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 34.61
Std Dev 7.394
Entry
ampl
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0
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60
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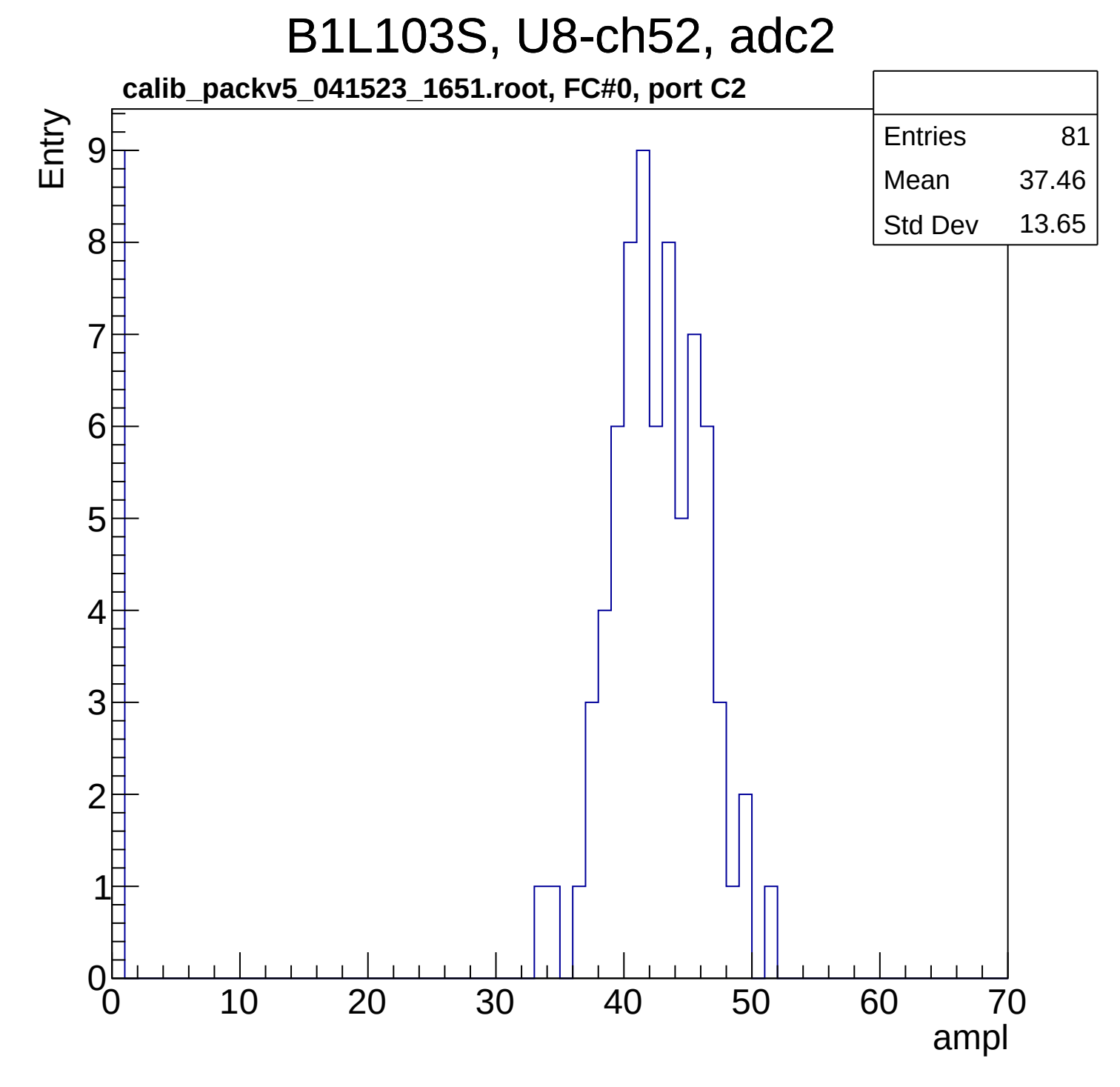
B1L103S, U8-ch52, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 37.46
Std Dev 13.65
Entry
ampl
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3
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5
6
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0
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60
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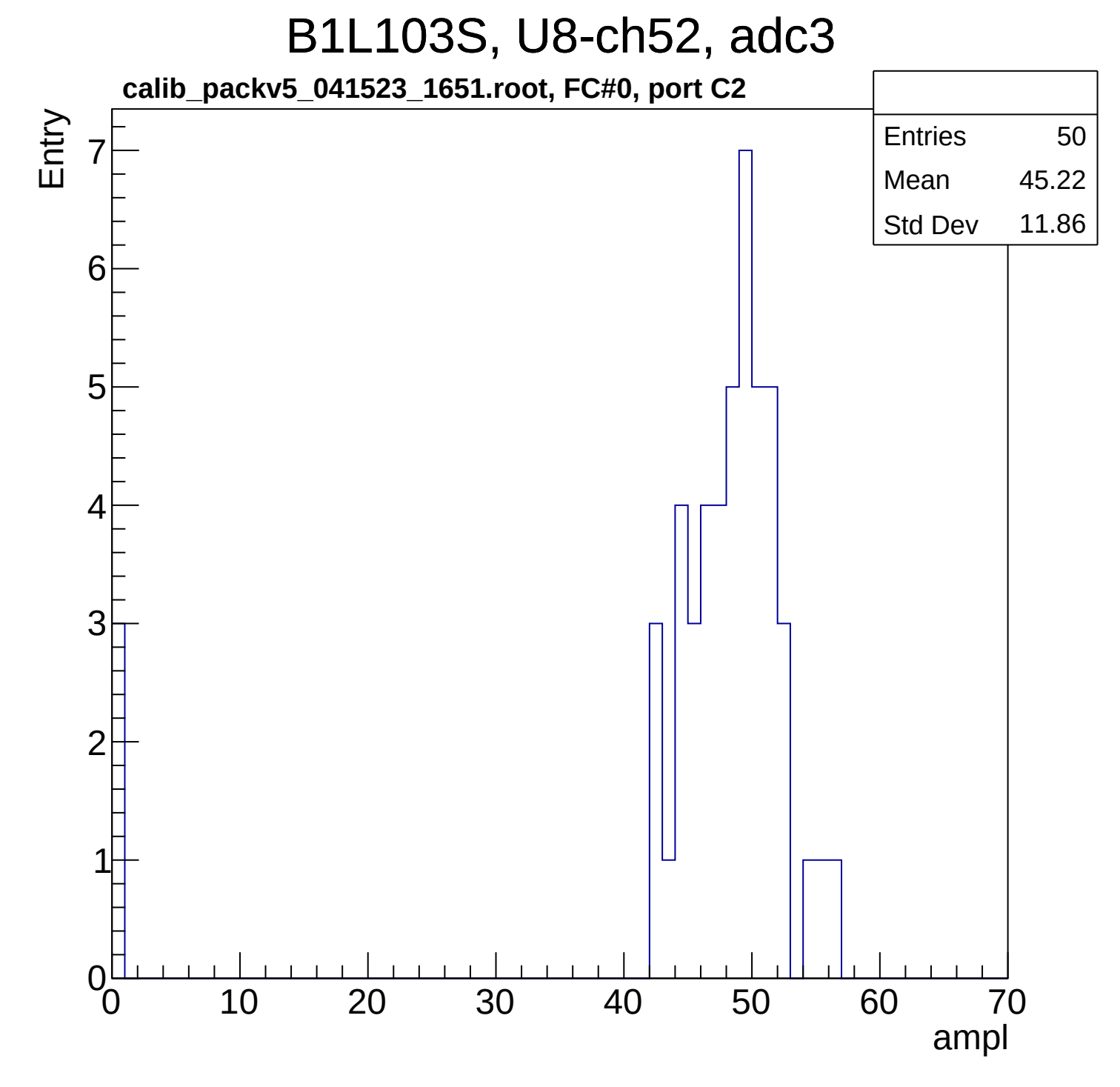
B1L103S, U8-ch52, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 45.22
Std Dev 11.86
Entry
ampl
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1
2
3
4
5
6
7
0
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20
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40
50
60
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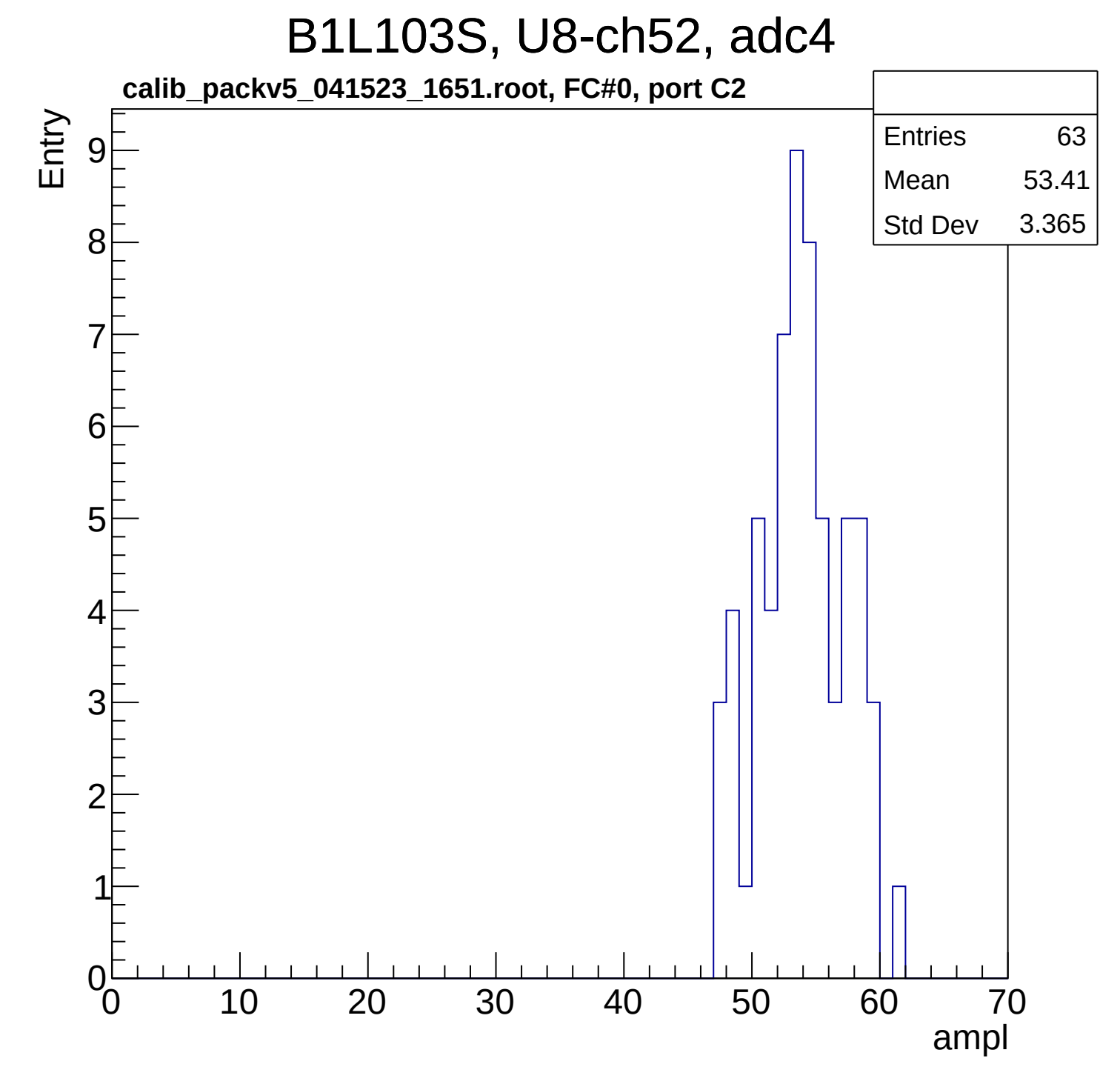
B1L103S, U8-ch52, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 53.41
Std Dev 3.365
Entry
ampl
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5
6
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9
0
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40
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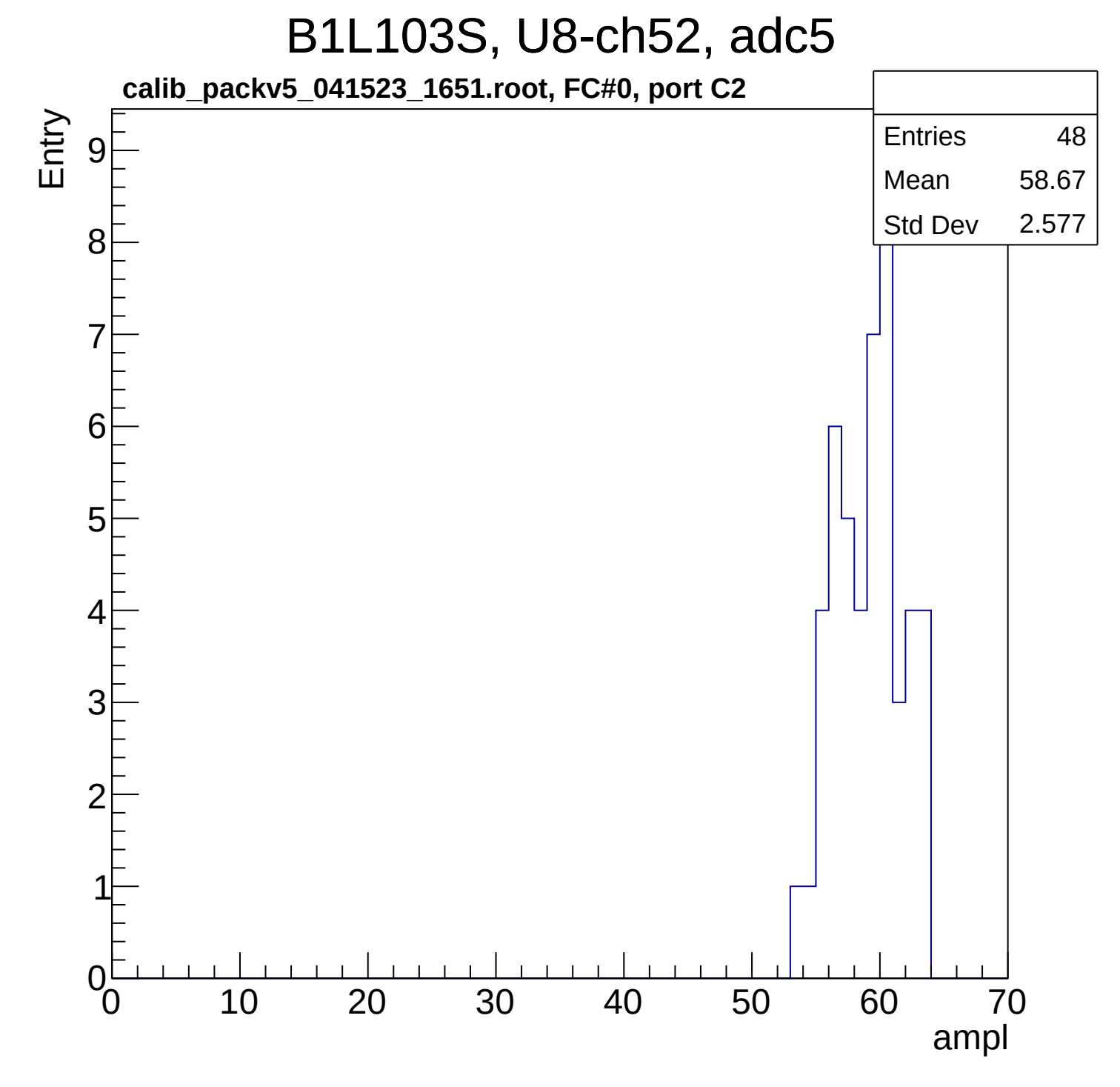
B1L103S, U8-ch52, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 58.67
Std Dev 2.577
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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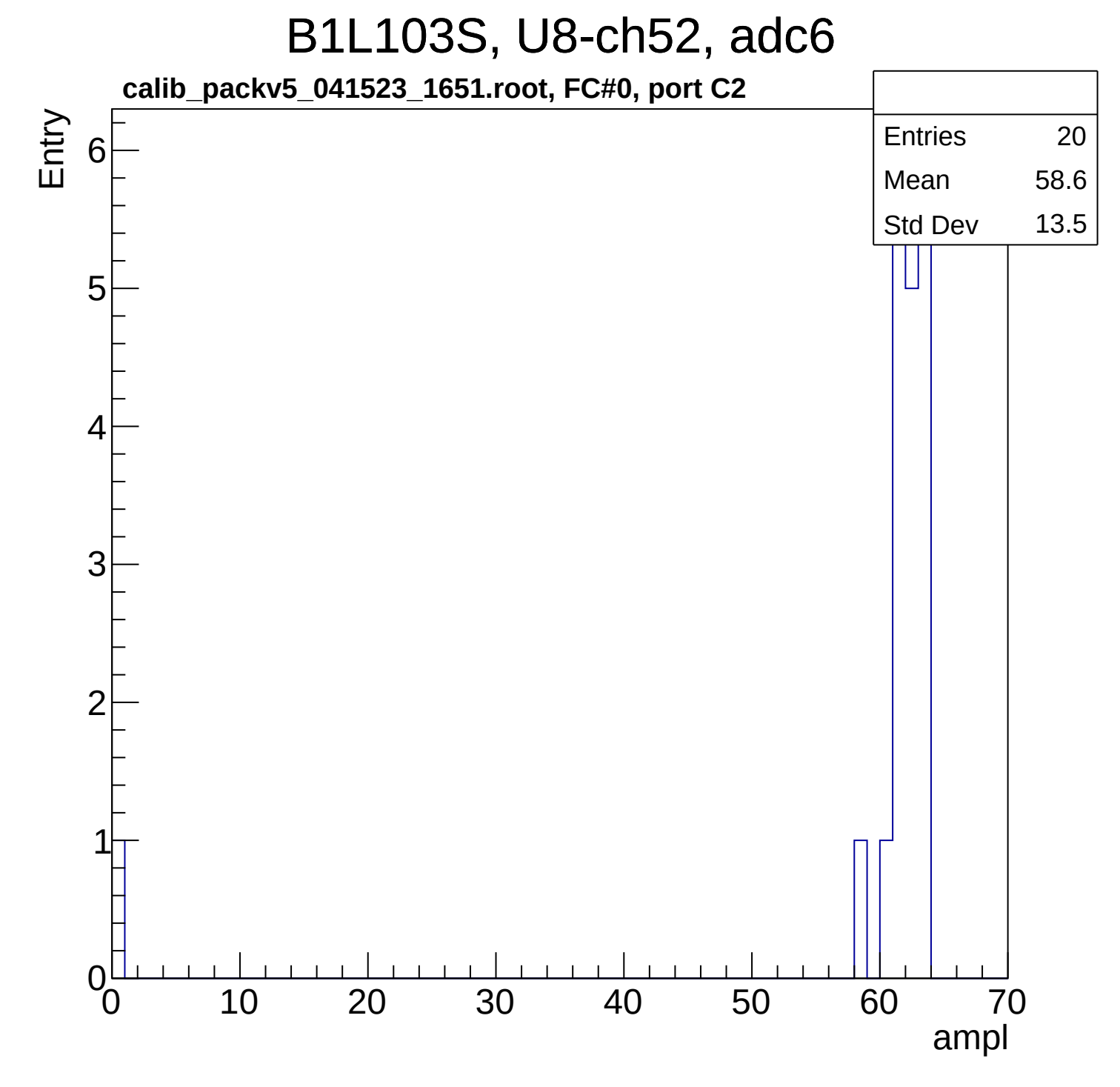
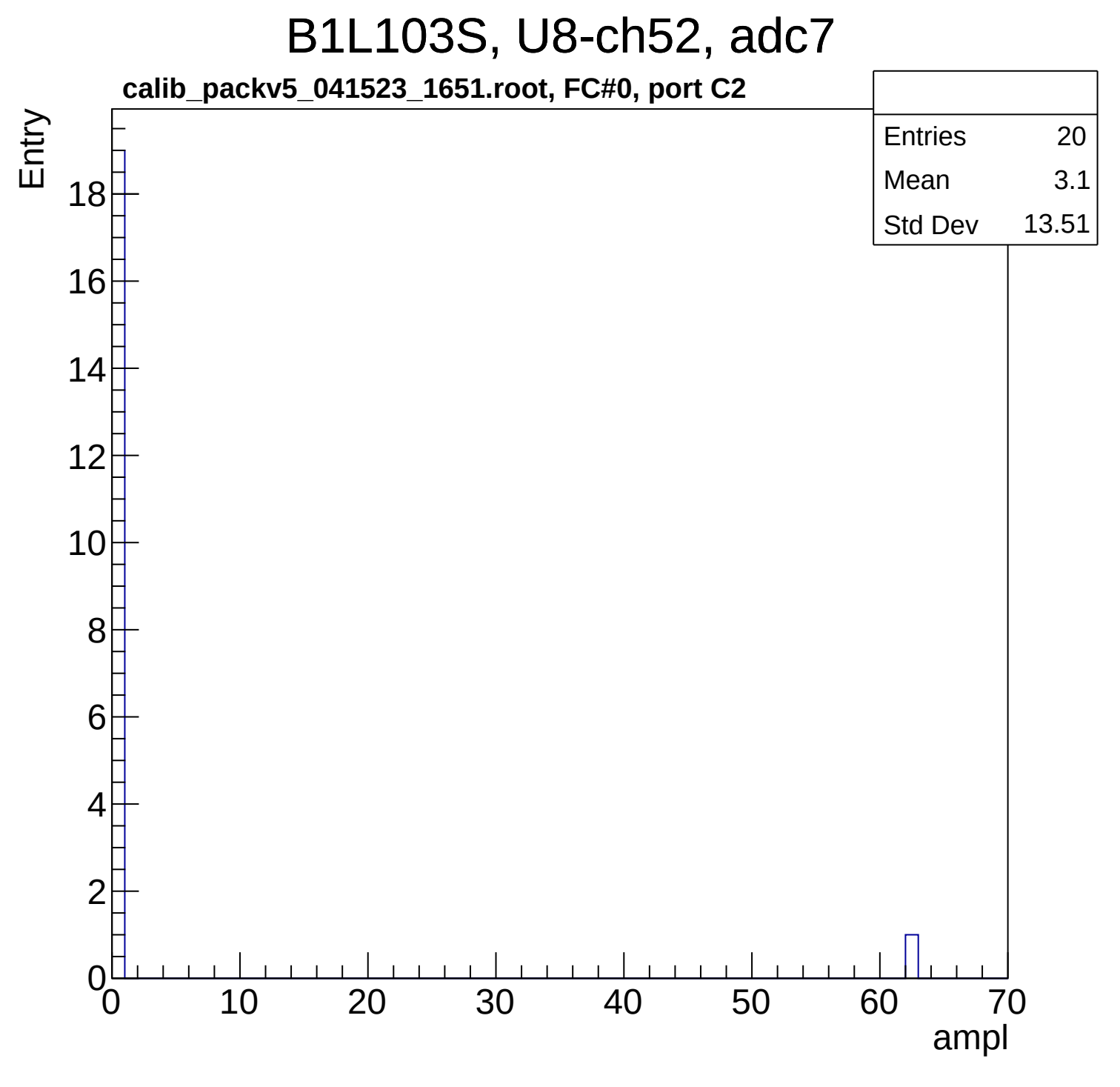
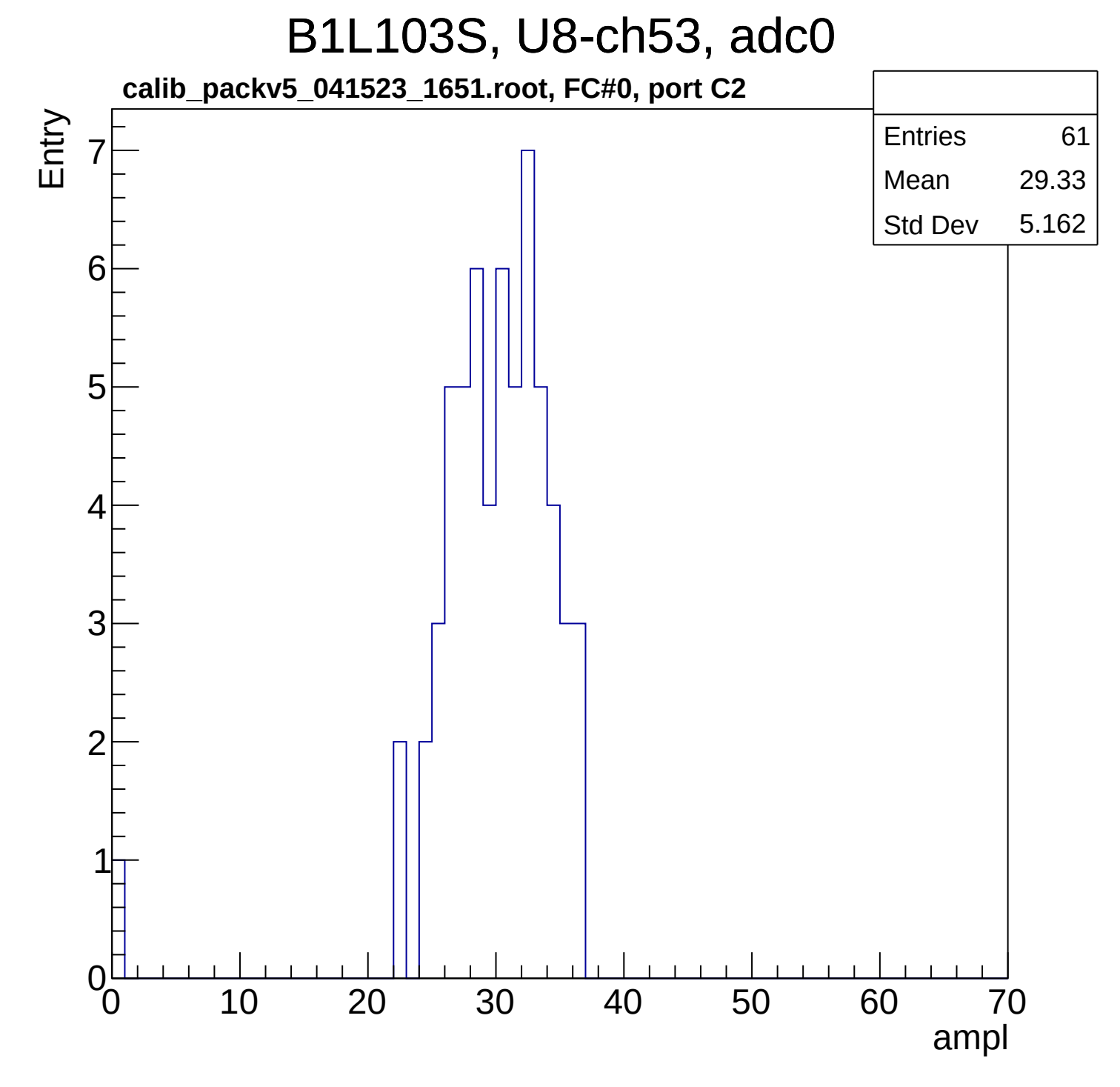

B1L103S, U8-ch52, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 58.6
Std Dev 13.5
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch52, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch53, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 29.33
Std Dev 5.162
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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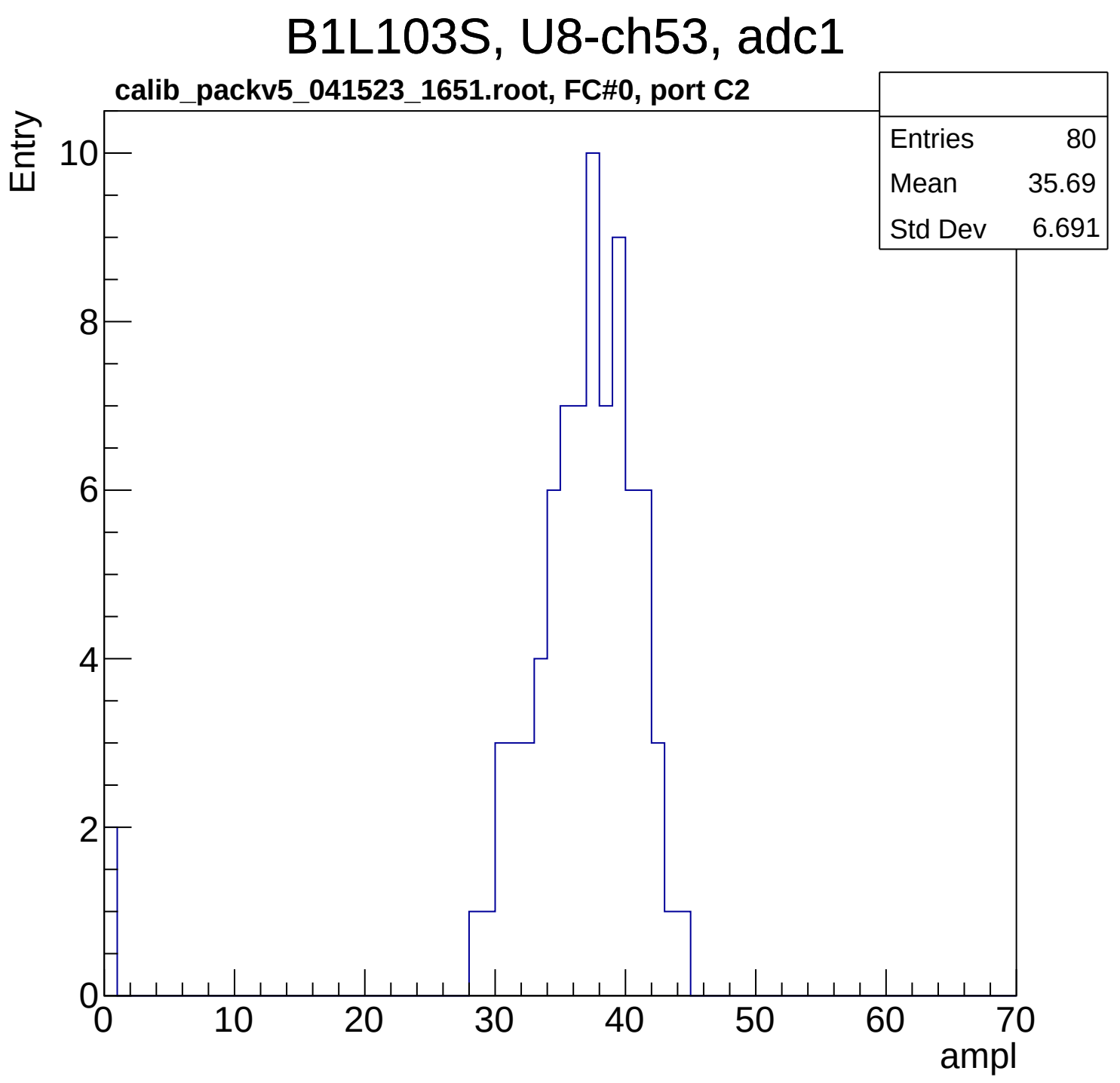
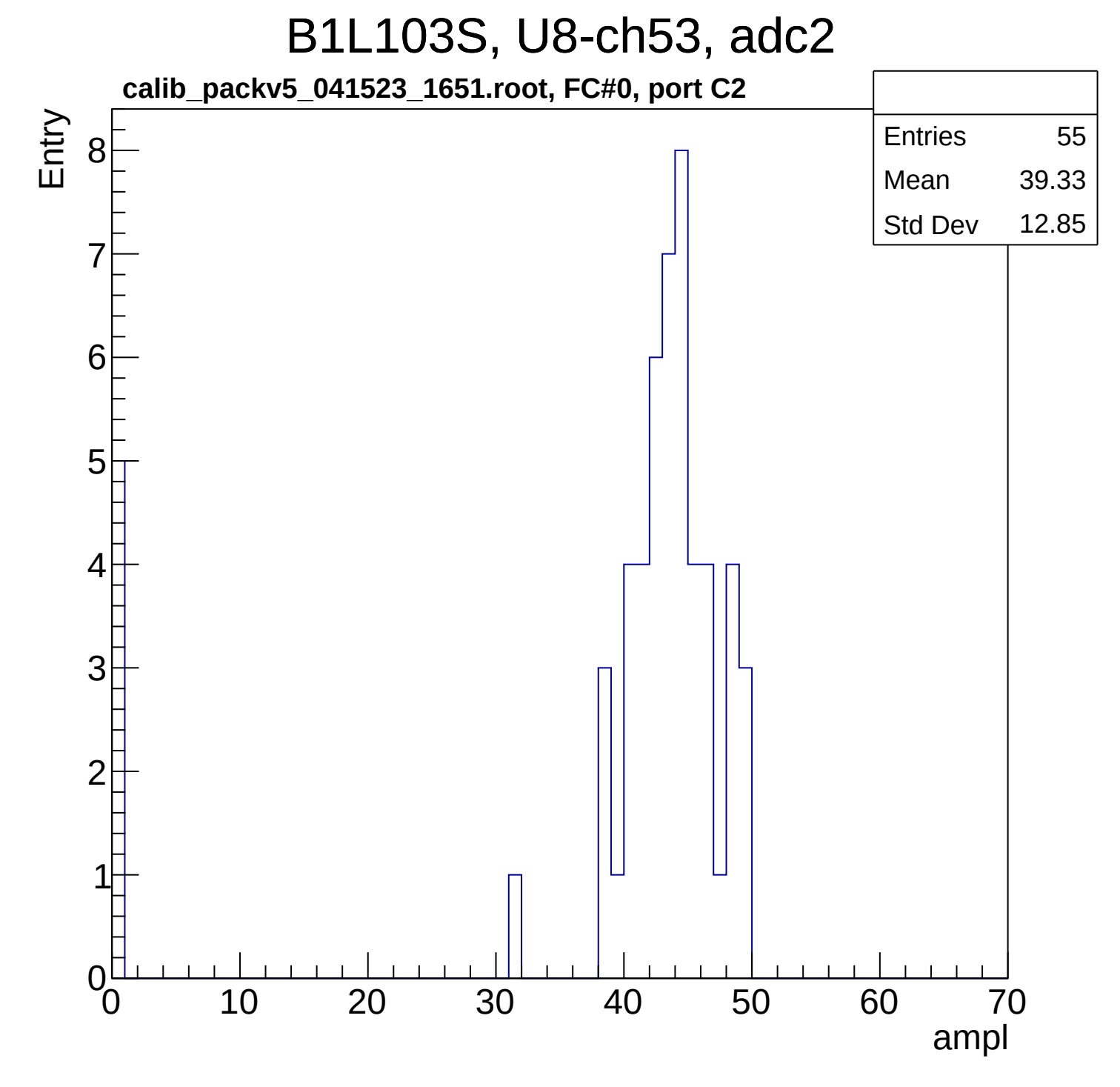

B1L103S, U8-ch53, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 35.69
Std Dev 6.691
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U8-ch53, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 39.33
Std Dev 12.85
Entry
ampl
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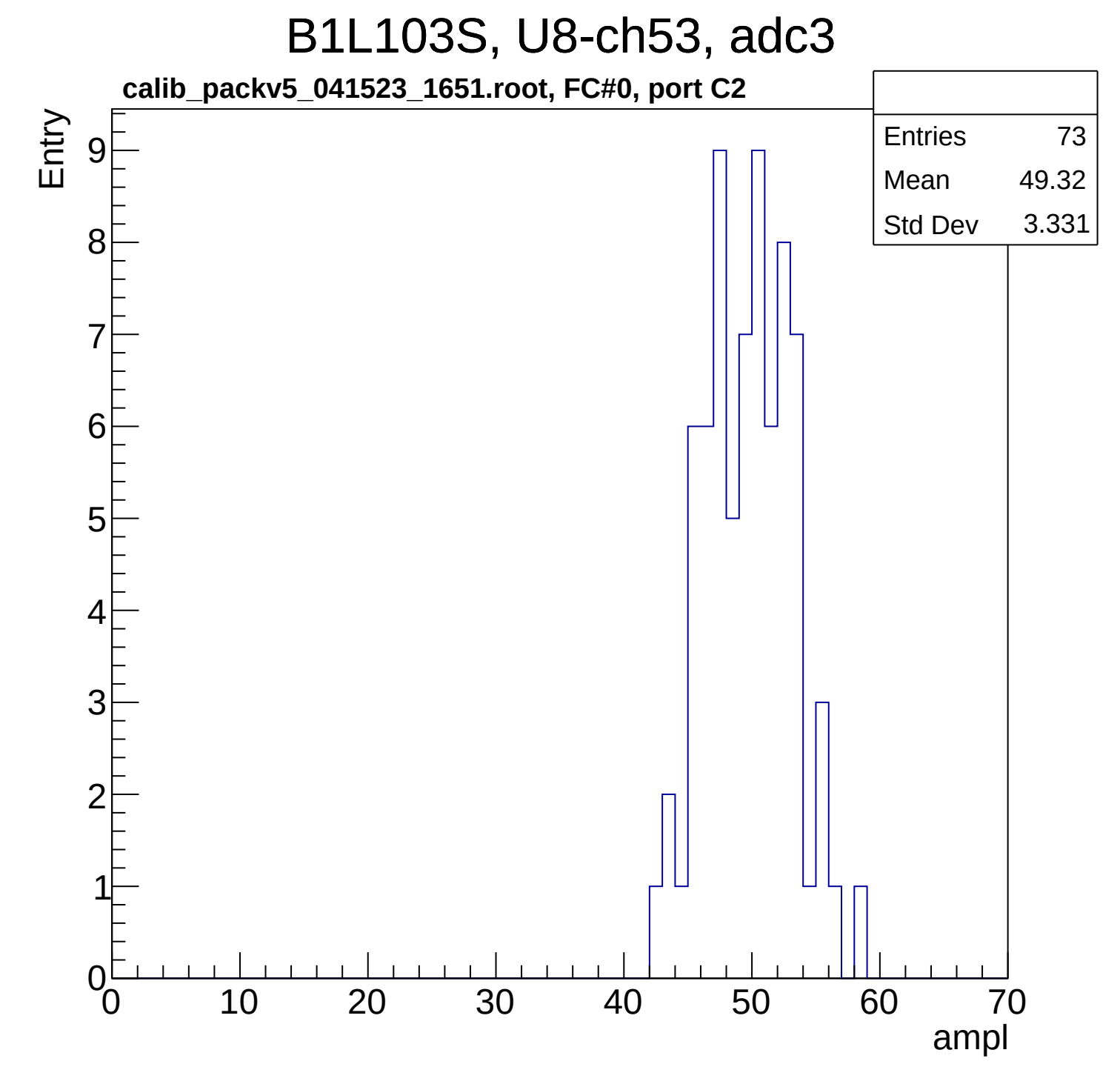
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch53, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 49.32
Std Dev 3.331
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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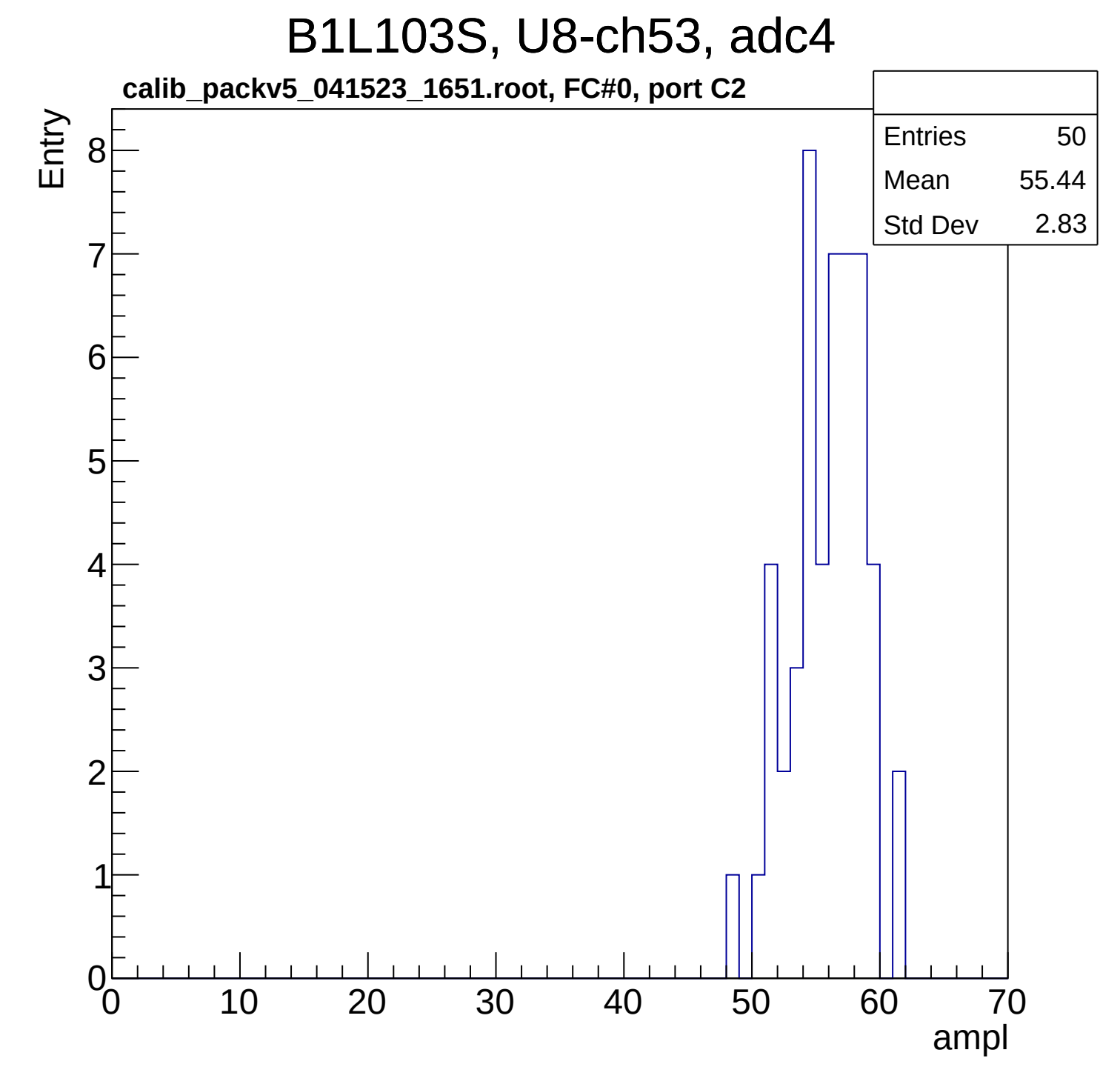
B1L103S, U8-ch53, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 55.44
Std Dev 2.83
Entry
ampl
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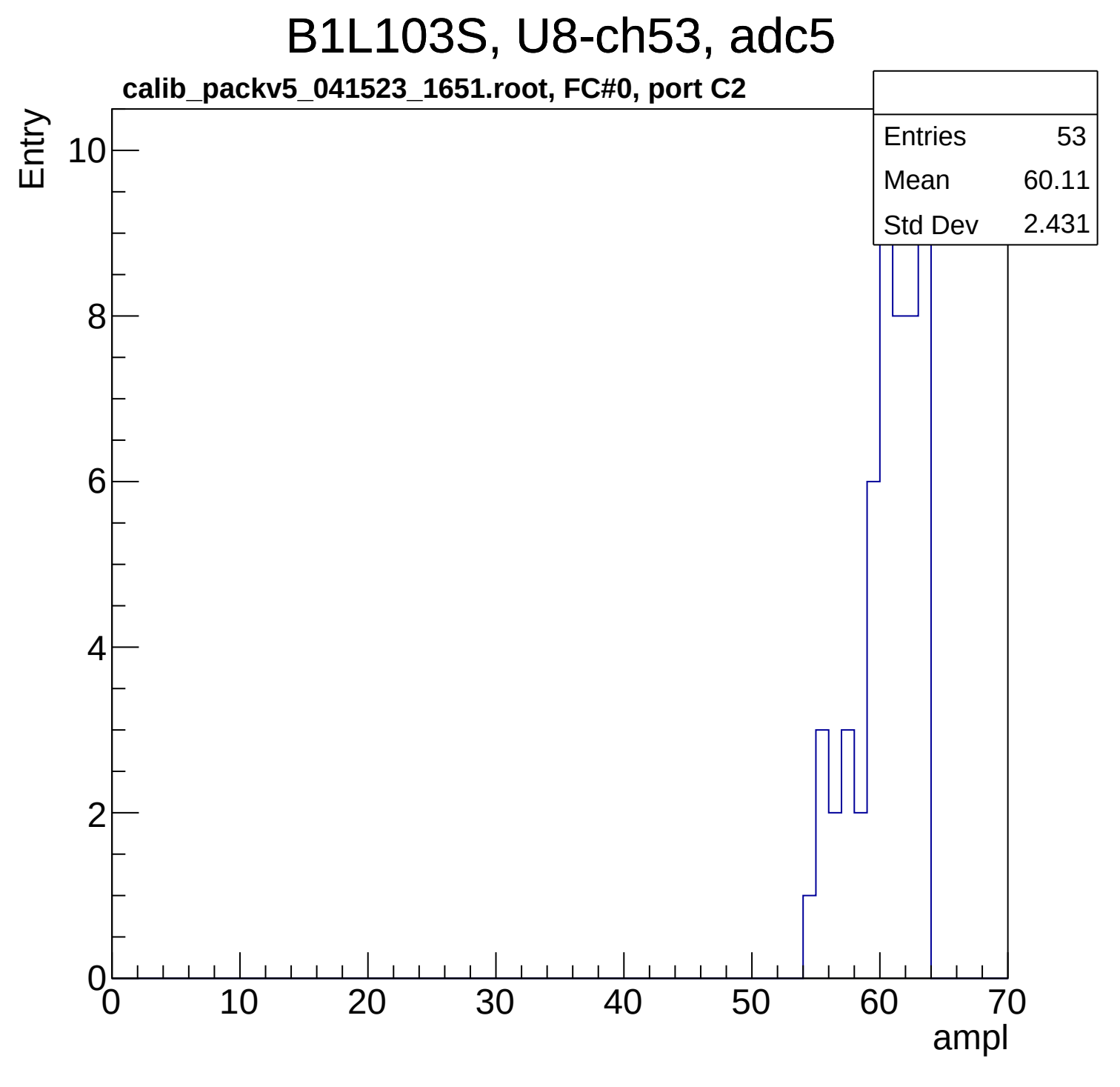
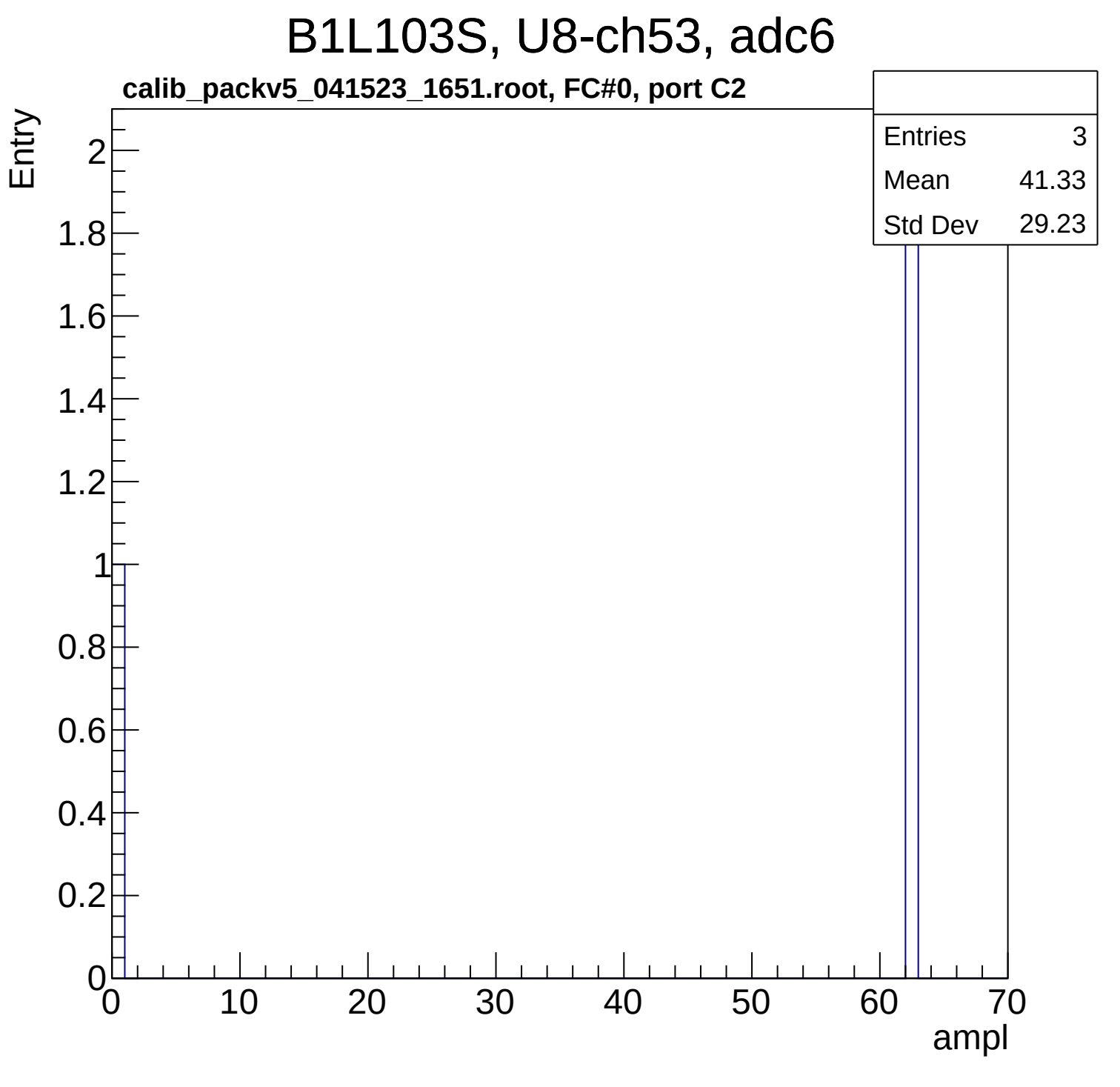
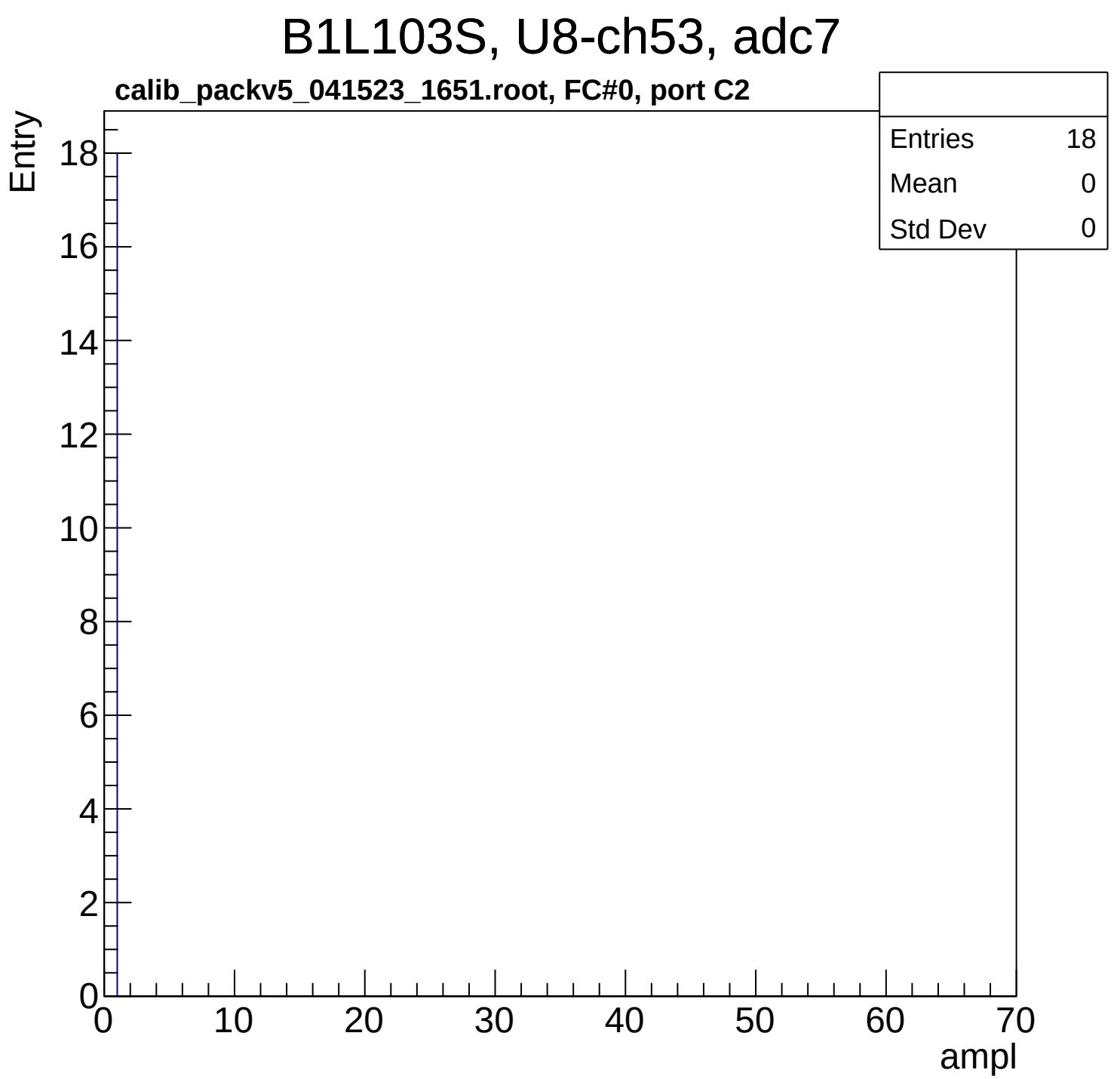
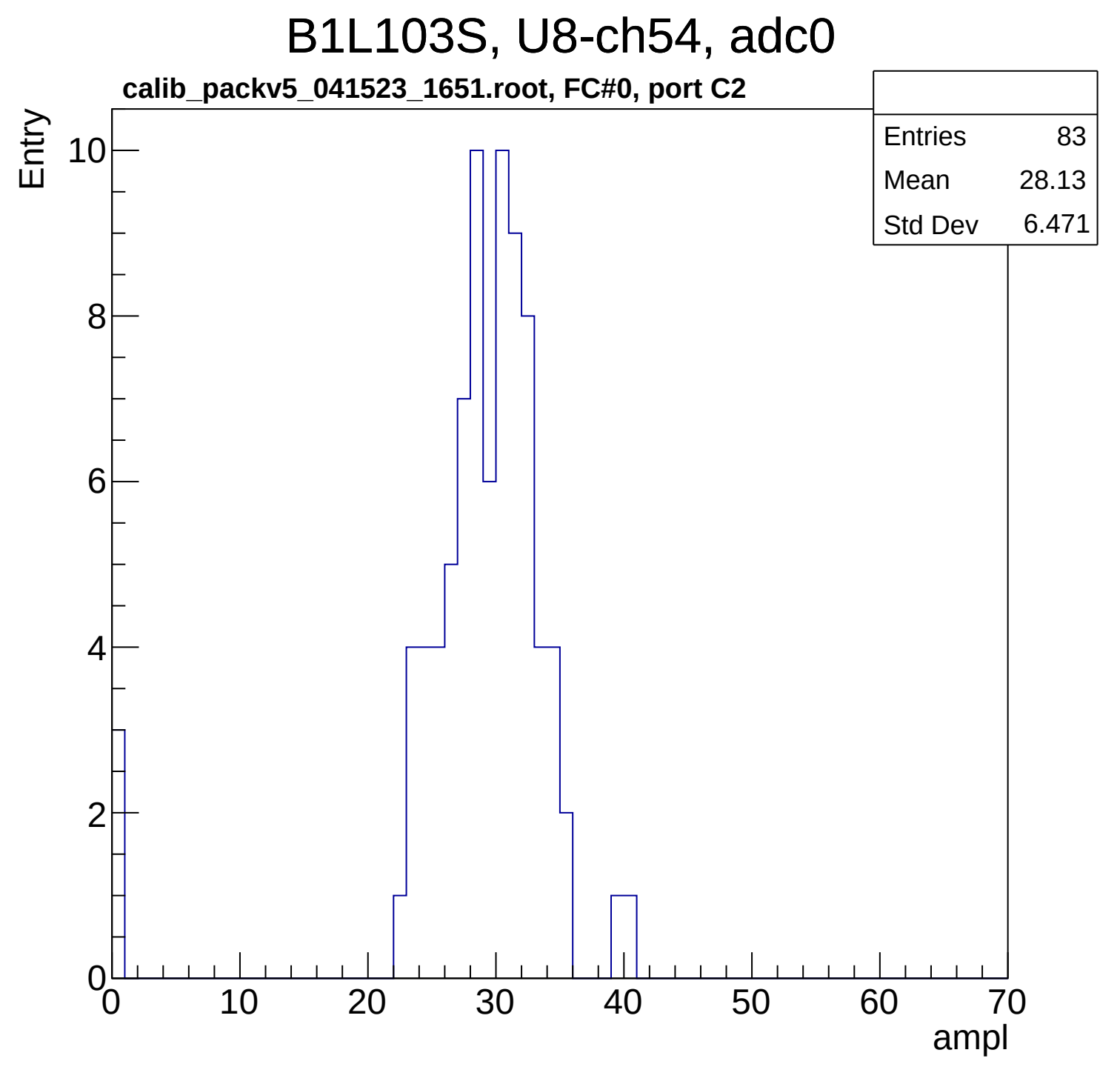
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch53, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 60.11
Std Dev 2.431
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U8-ch53, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 41.33
Std Dev 29.23
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U8-ch53, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch54, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 28.13
Std Dev 6.471
Entry
ampl
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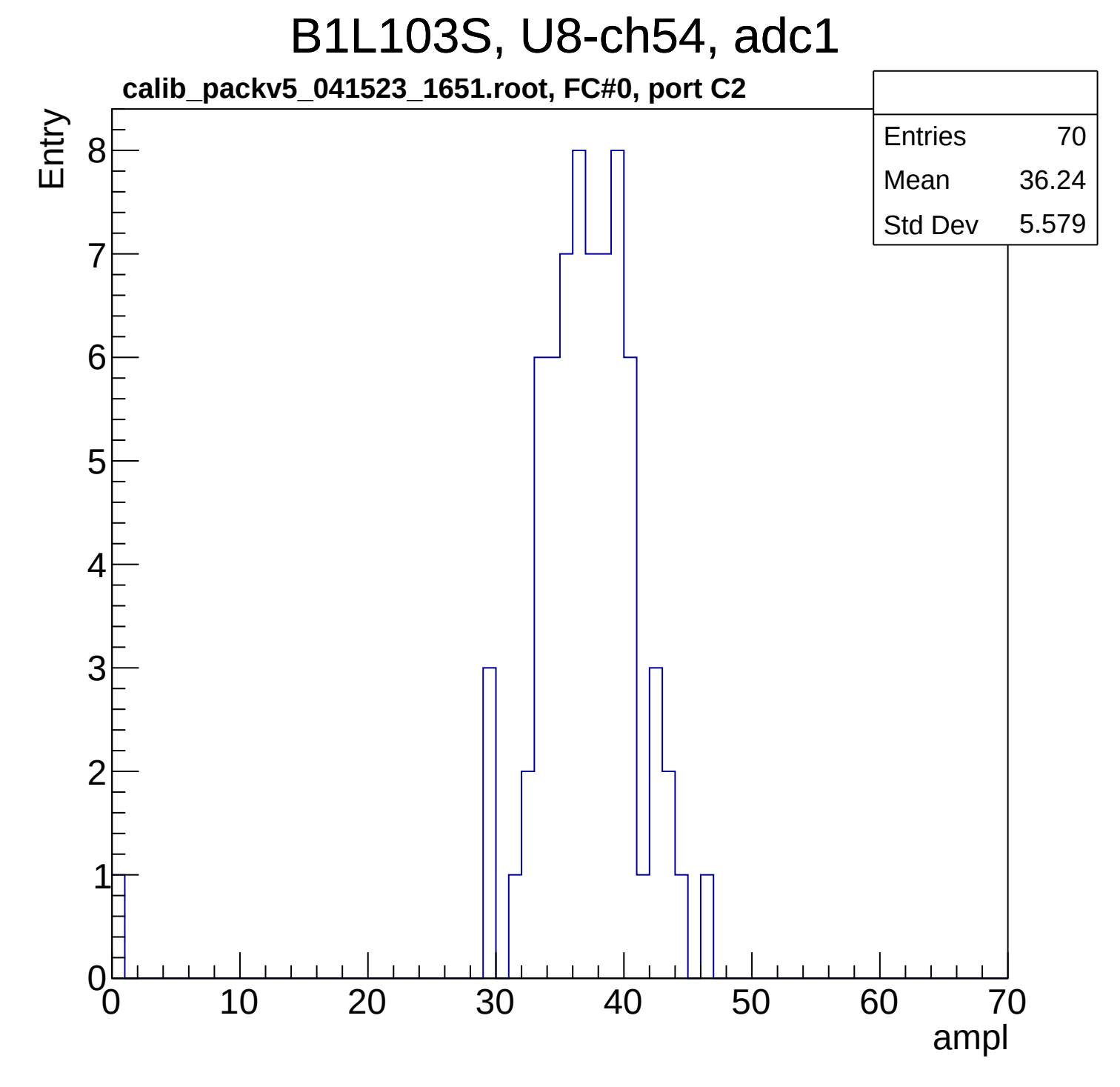
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U8-ch54, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 36.24
Std Dev 5.579
Entry
ampl
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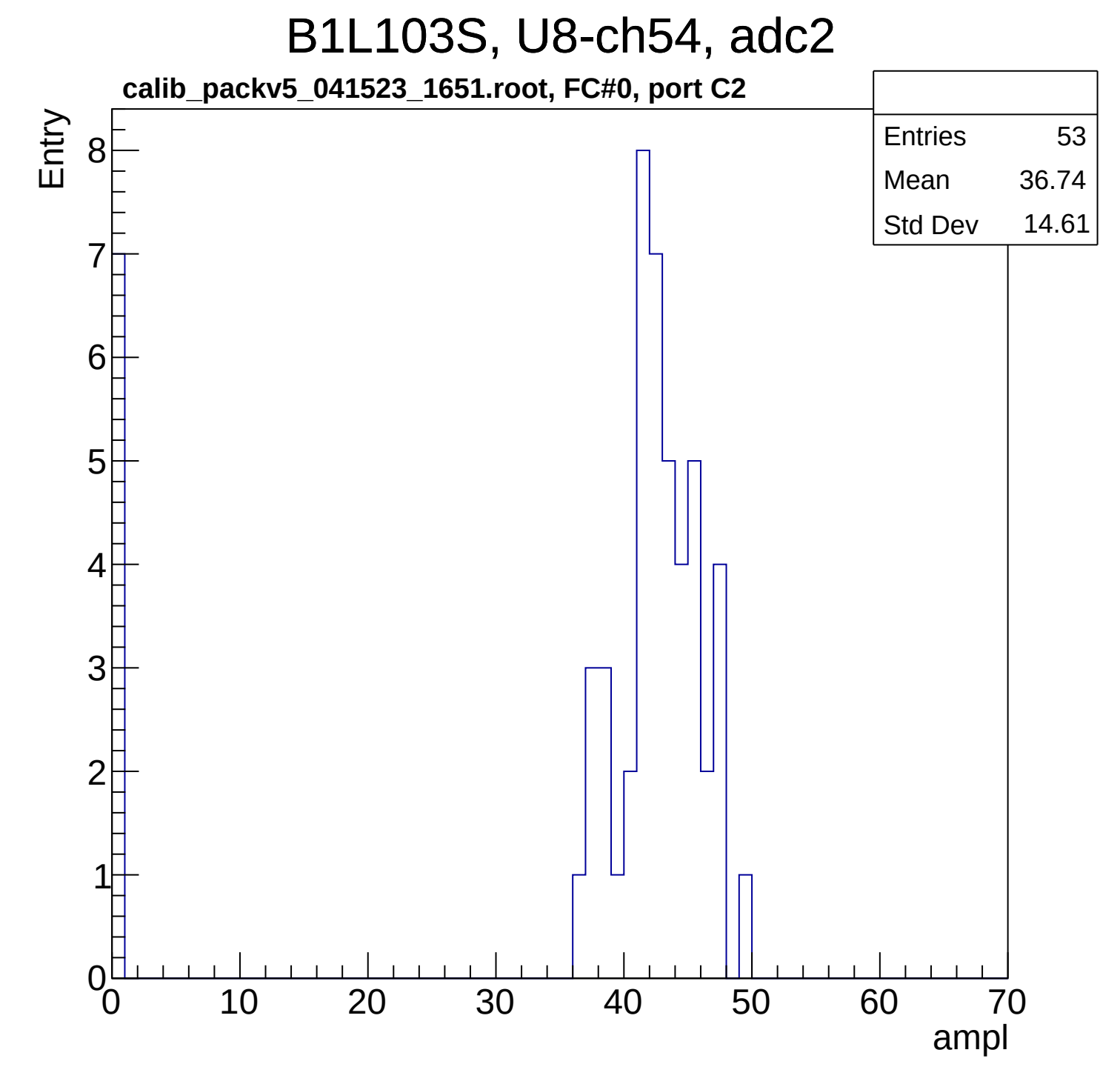
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch54, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 36.74
Std Dev 14.61
Entry
ampl
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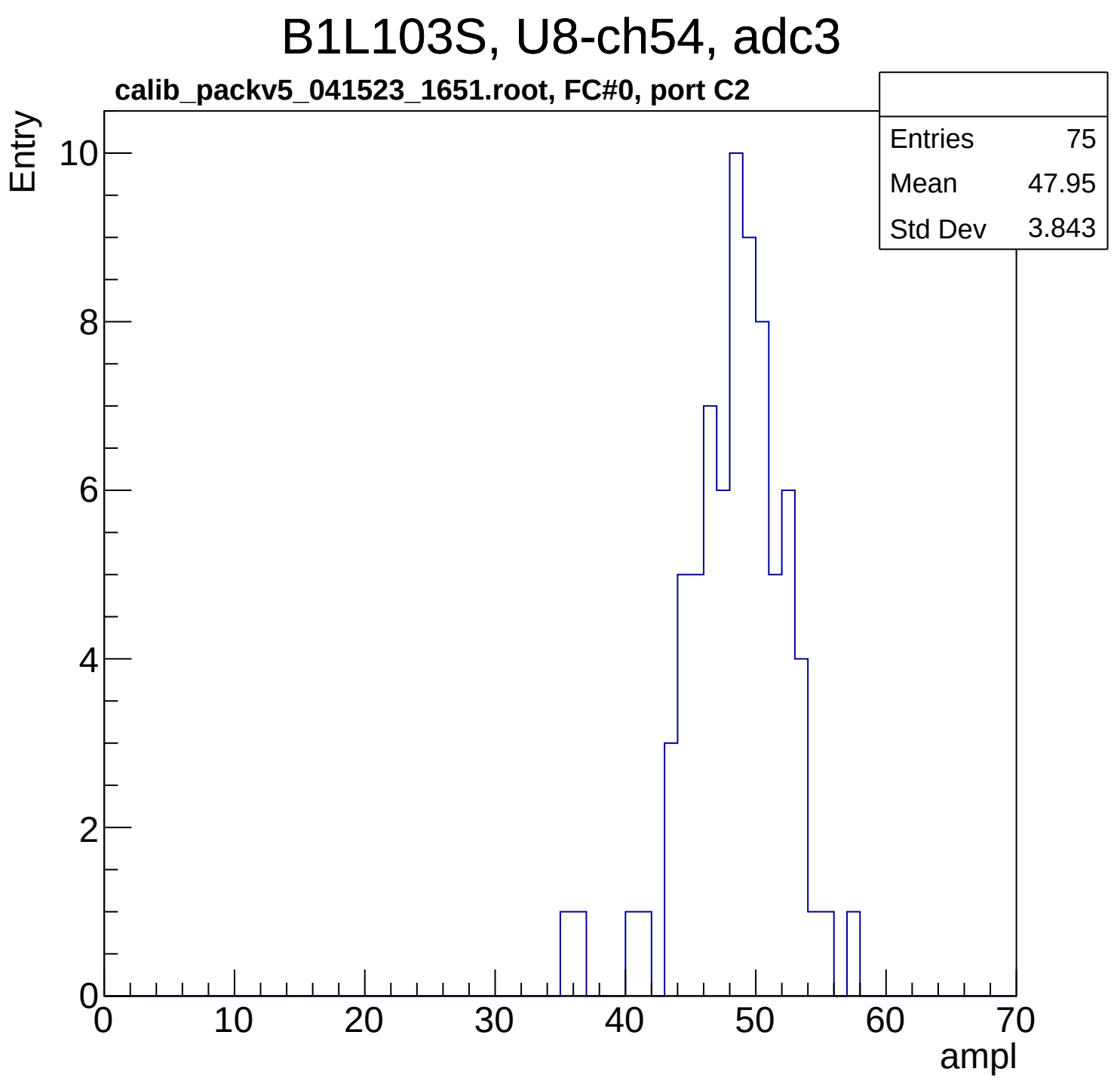
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch54, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 47.95
Std Dev 3.843
Entry
ampl
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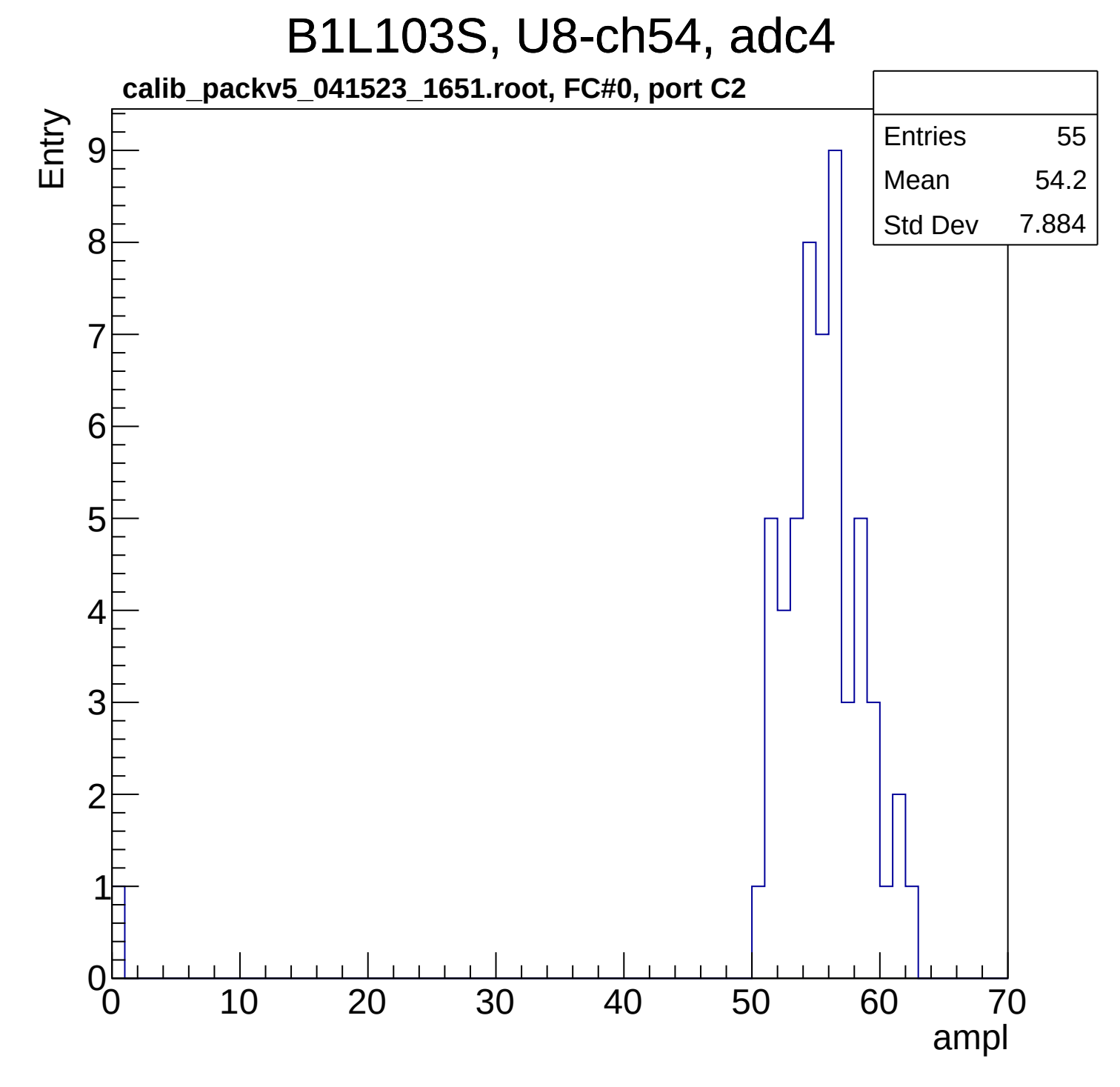
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U8-ch54, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 54.2
Std Dev 7.884
Entry
ampl
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2
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4
5
6
7
8
9
0
10
20
30
40
50
60
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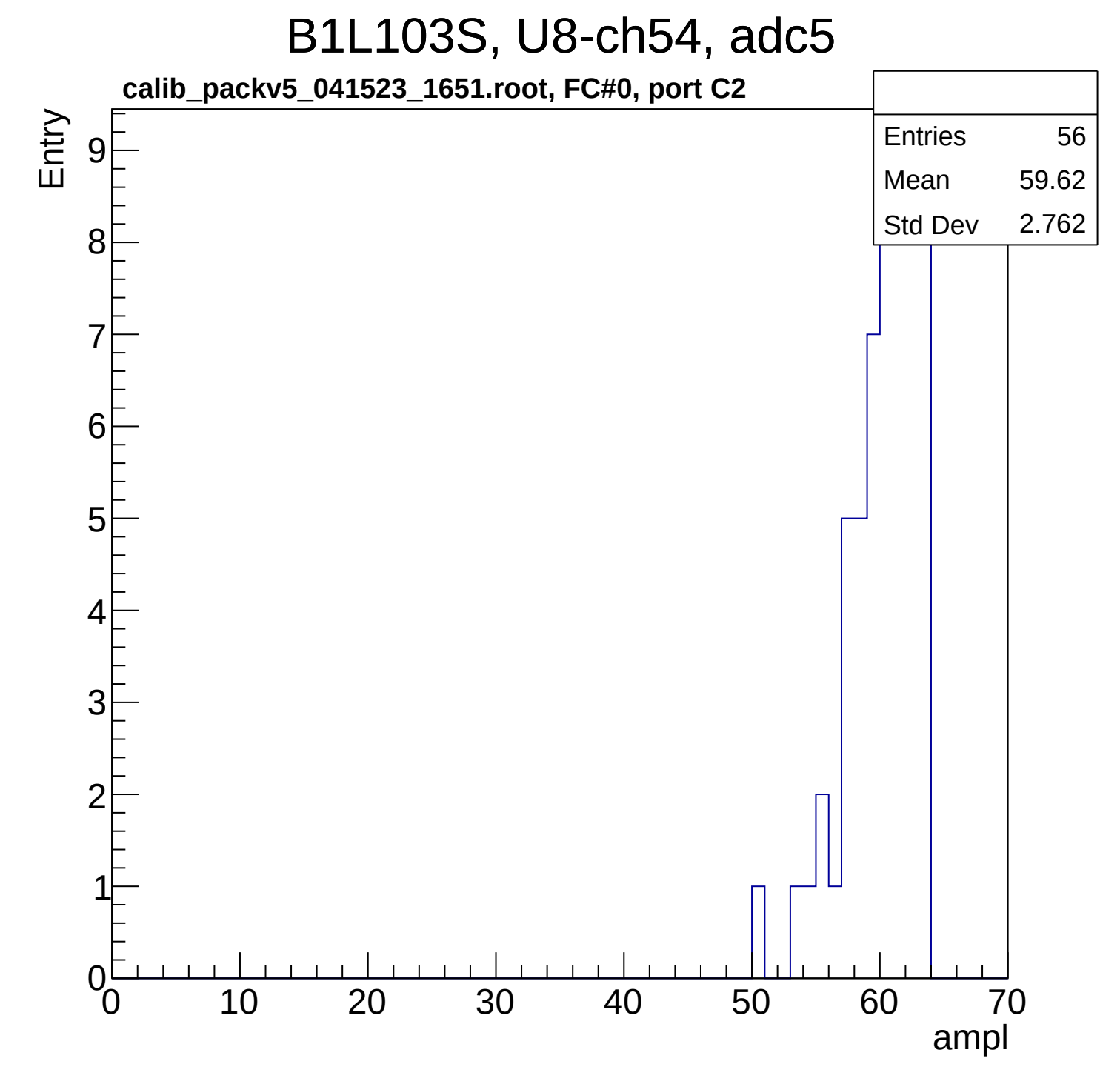
B1L103S, U8-ch54, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 59.62
Std Dev 2.762
Entry
ampl
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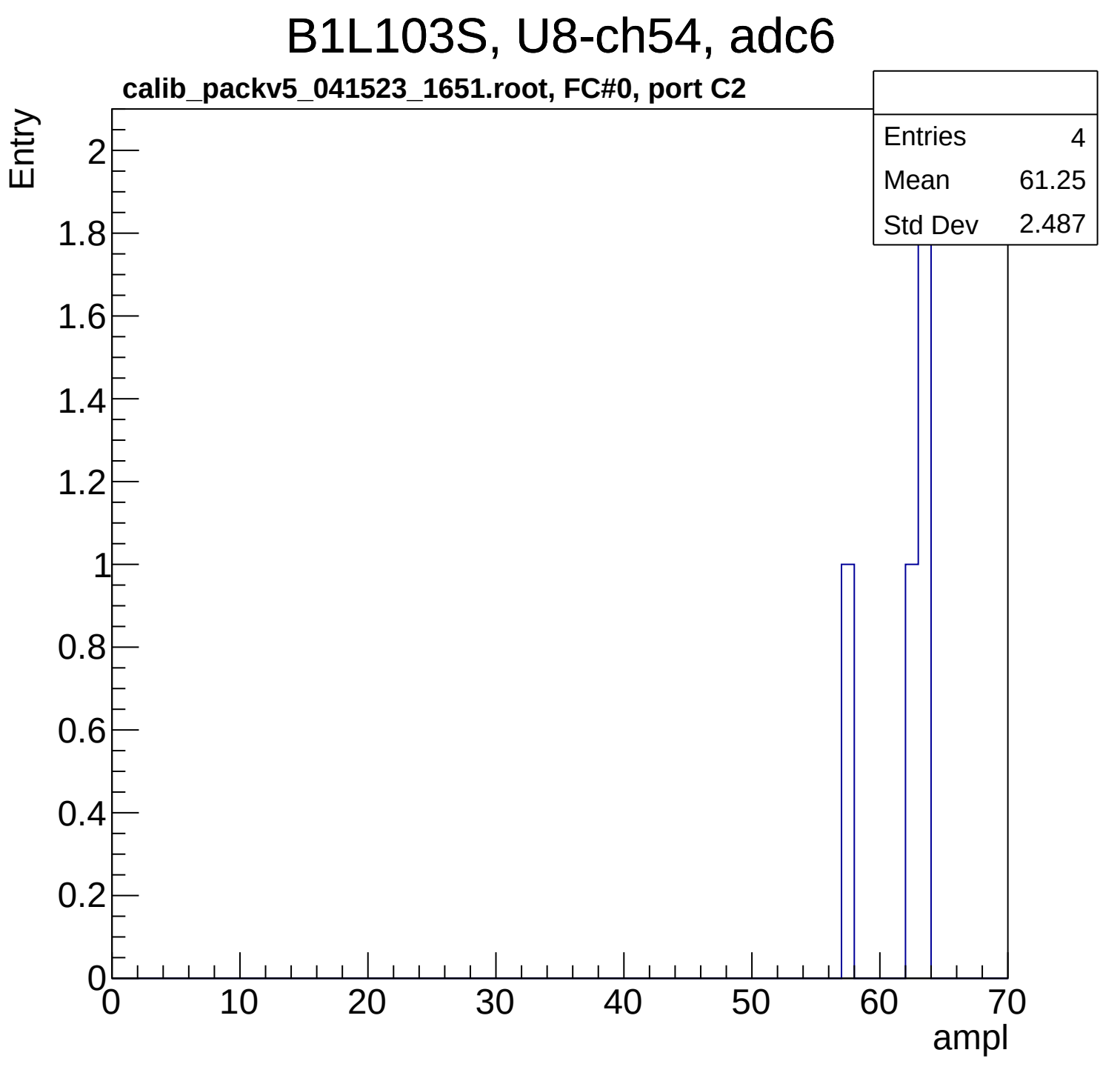
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U8-ch54, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 61.25
Std Dev 2.487
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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40
50
60
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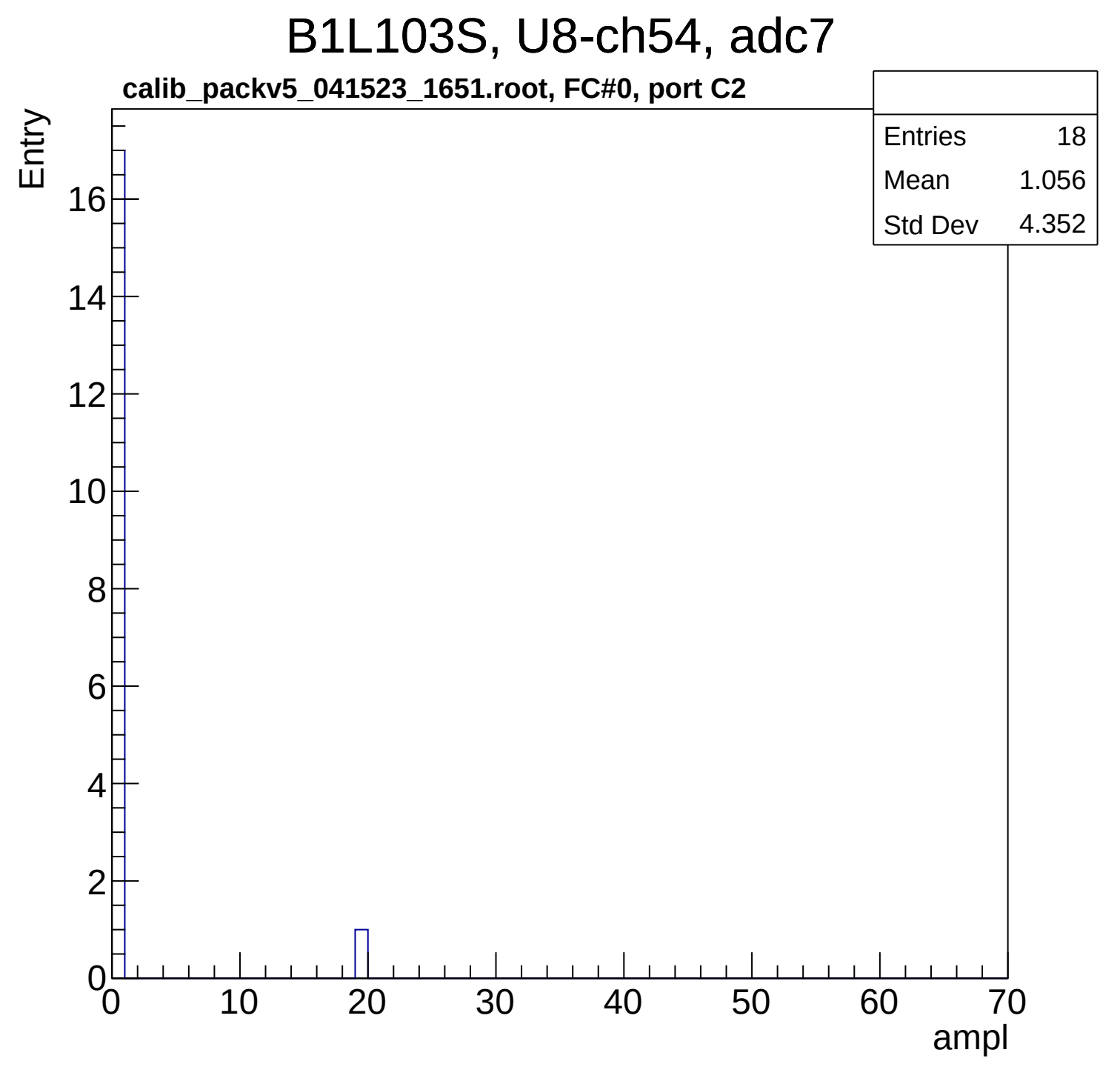
B1L103S, U8-ch54, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.056
Std Dev 4.352
Entry
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4
6
8
10
12
14
16
0
10
20
30
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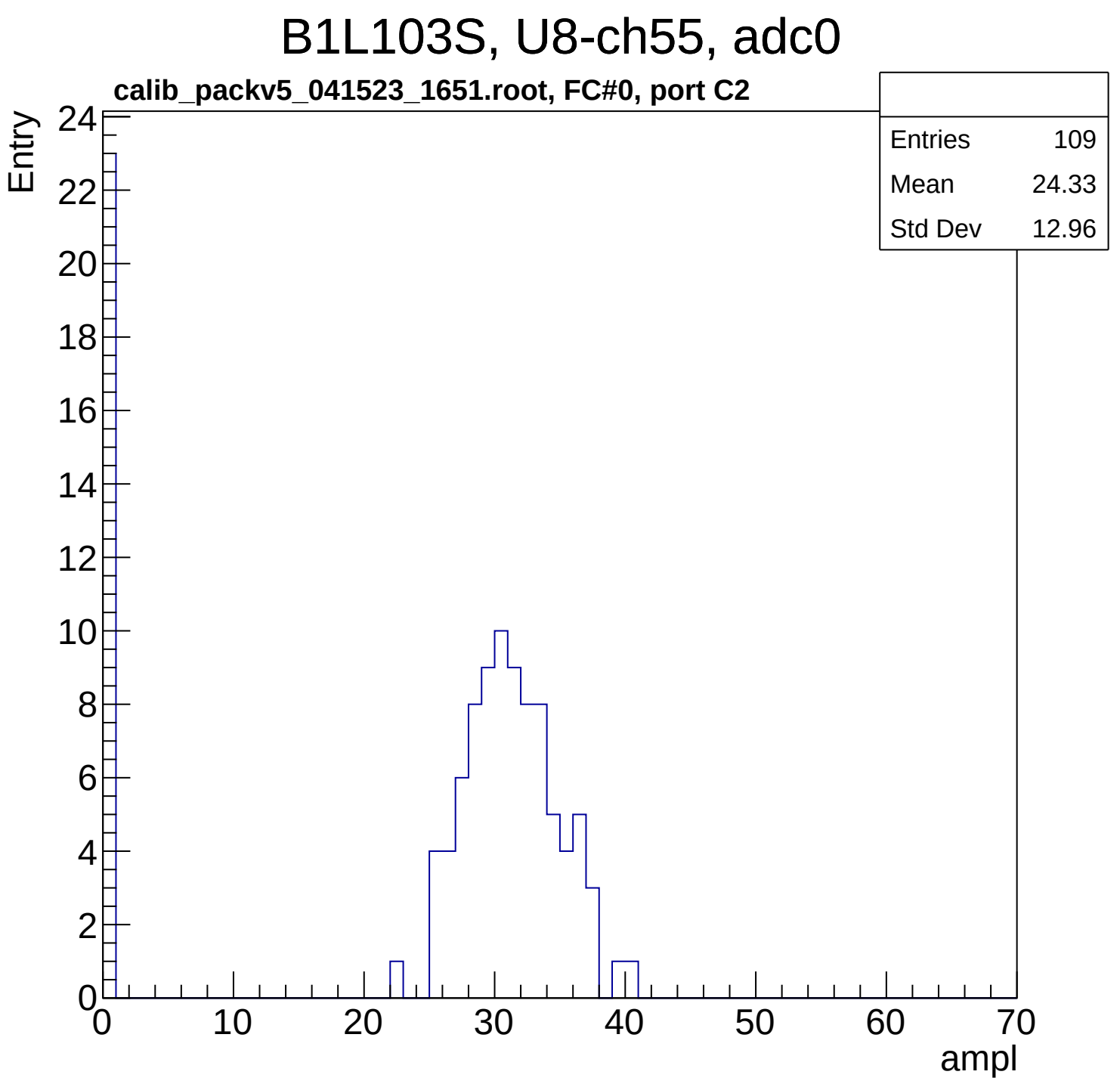
50
60
70
ampl


B1L103S, U8-ch55, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 109
Mean 24.33
Std Dev 12.96
Entry
ampl
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10
12
14
16
18
20
22
24
0
10
20
30
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60
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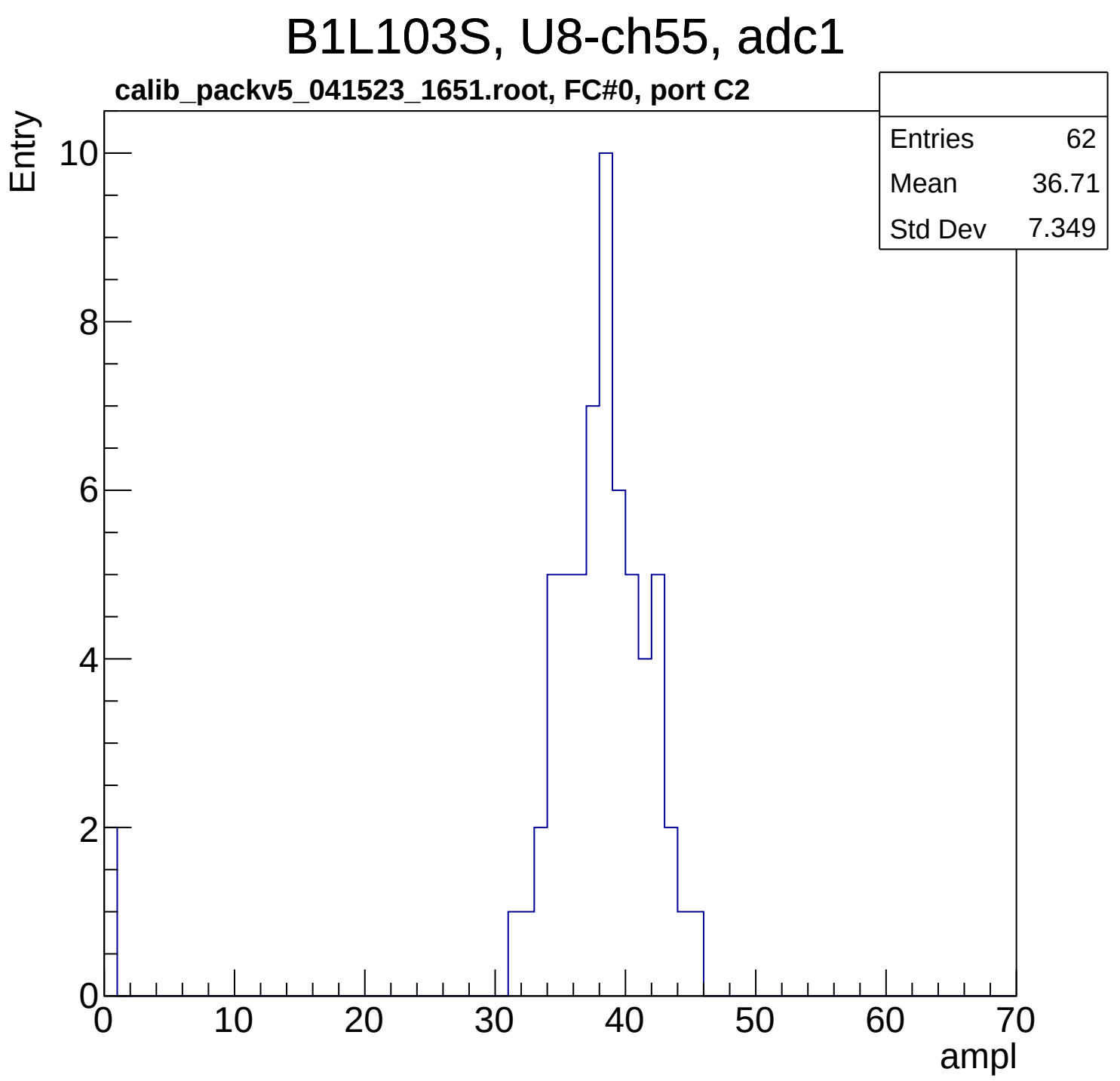
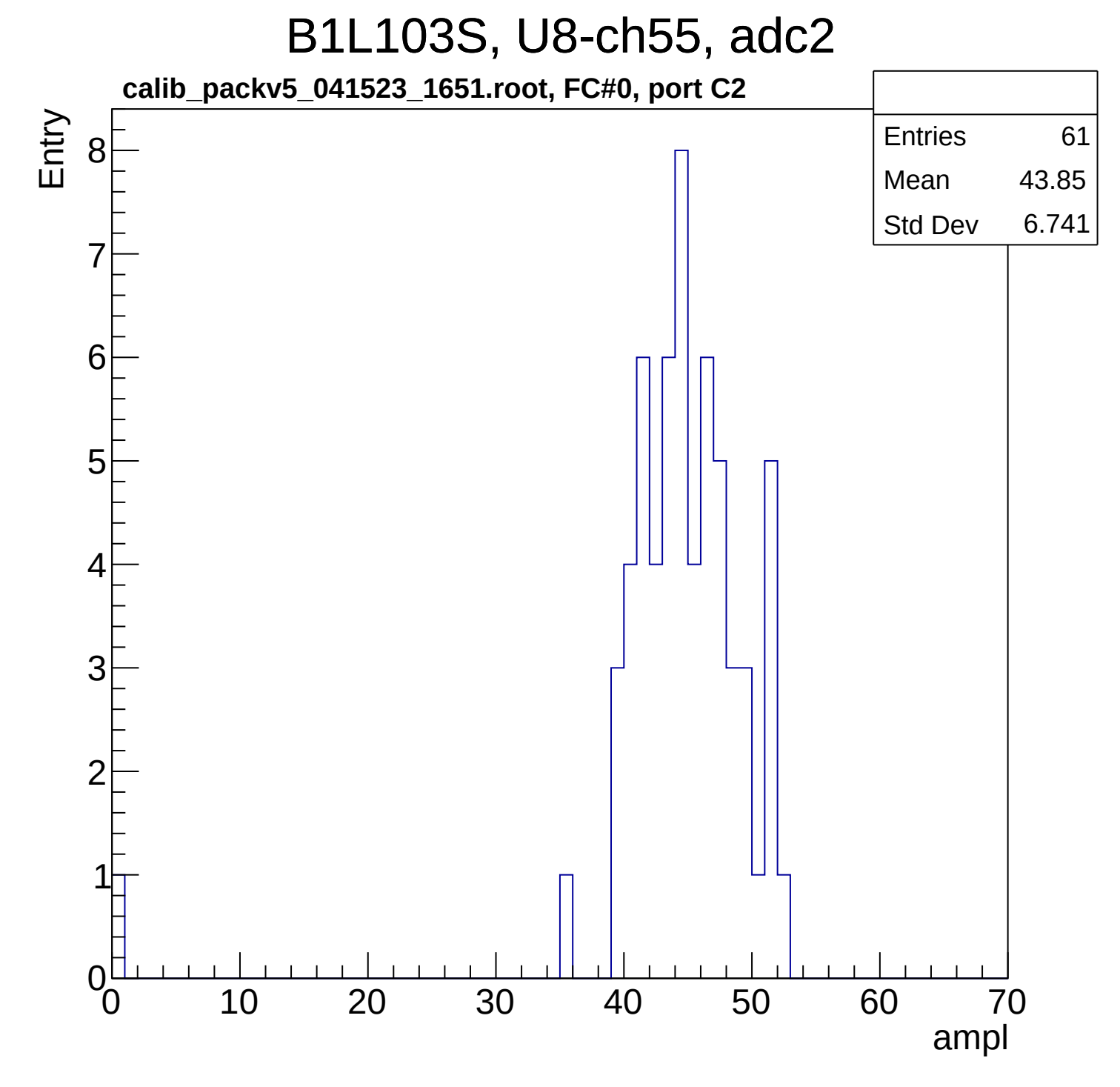

B1L103S, U8-ch55, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 36.71
Std Dev 7.349
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U8-ch55, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 43.85
Std Dev 6.741
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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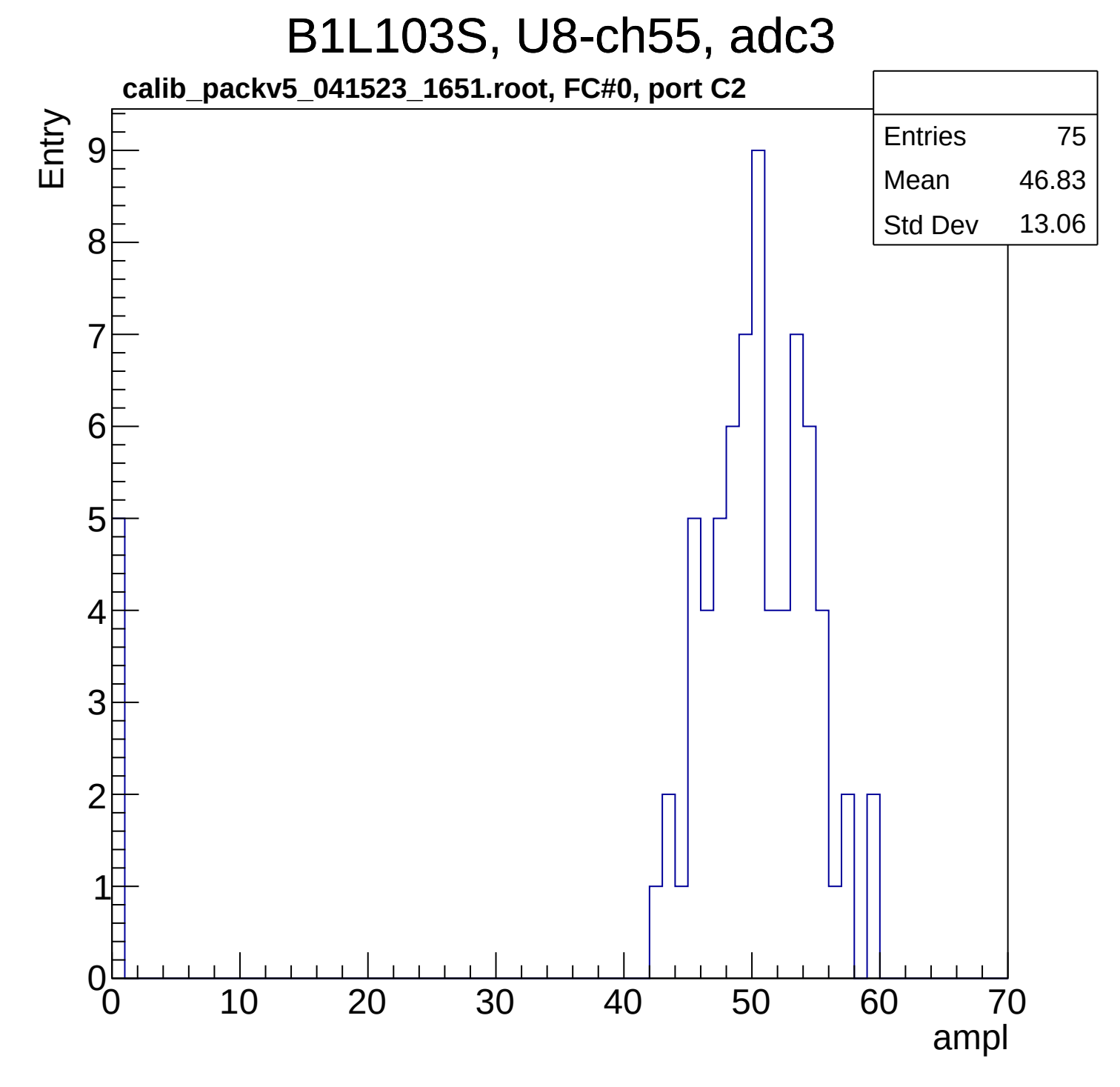
B1L103S, U8-ch55, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 46.83
Std Dev 13.06
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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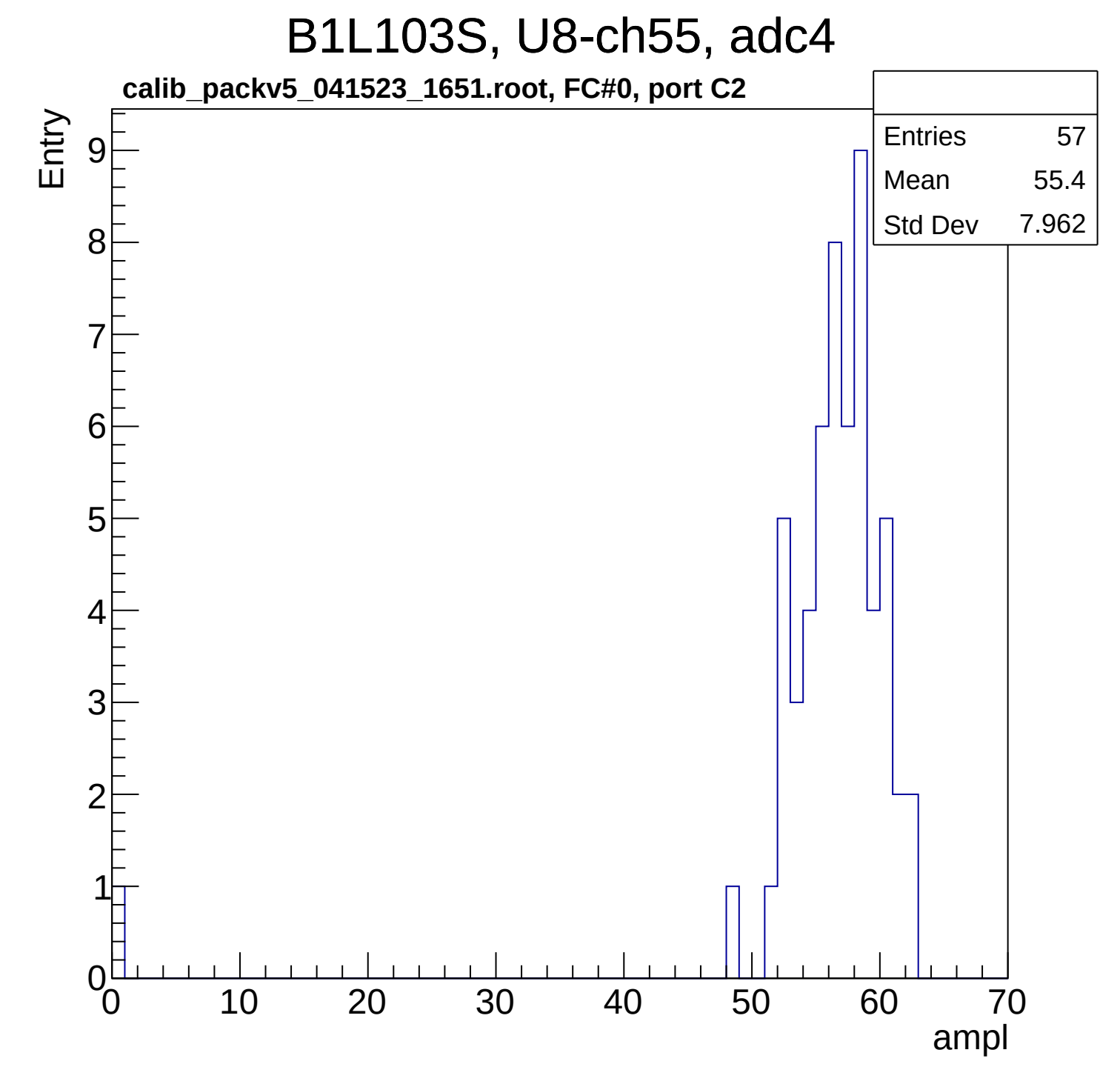
40
50
60
70


B1L103S, U8-ch55, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 55.4
Std Dev 7.962
Entry
ampl
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3
4
5
6
7
8
9
0
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20
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40
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60
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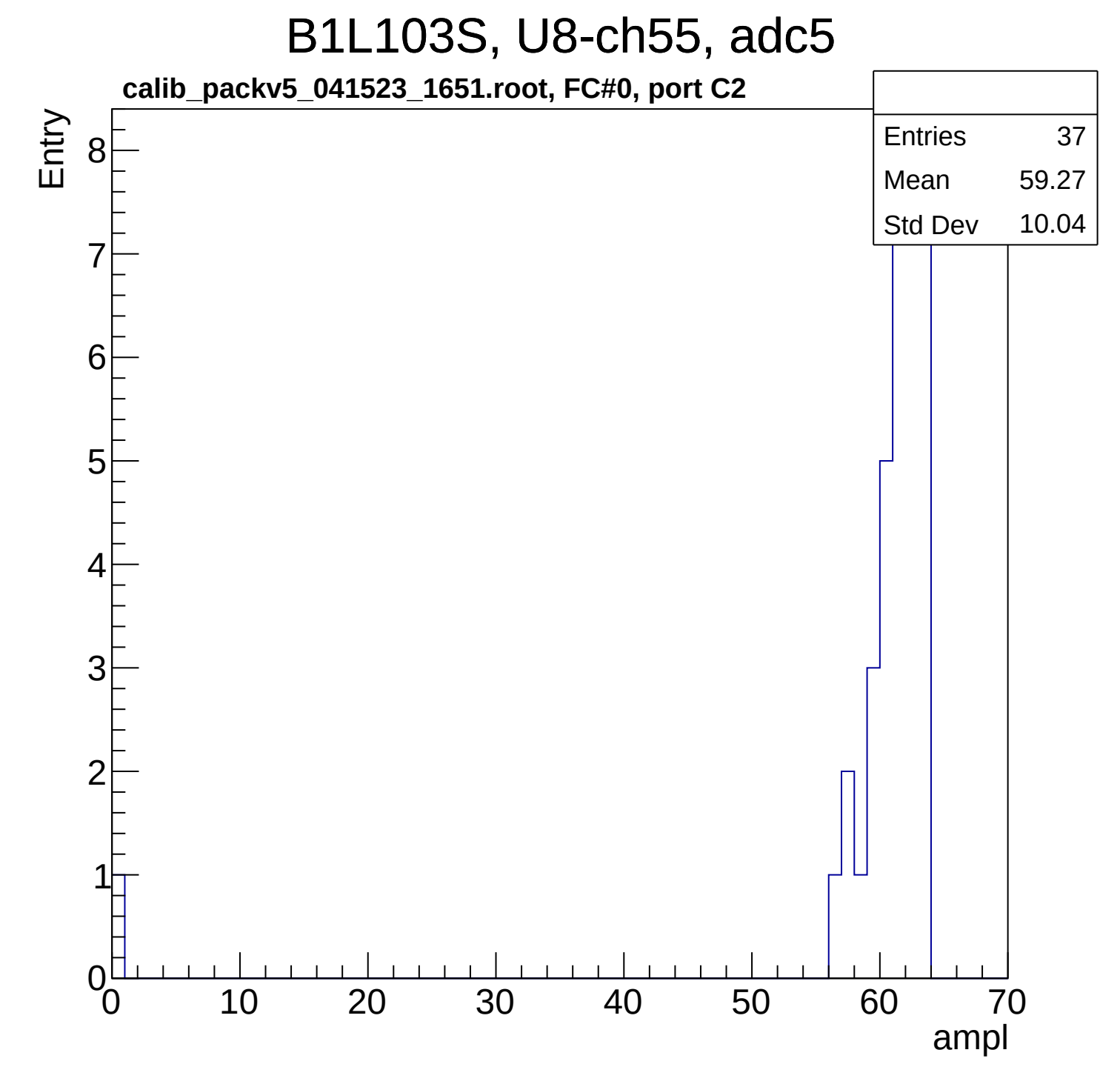
B1L103S, U8-ch55, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 59.27
Std Dev 10.04
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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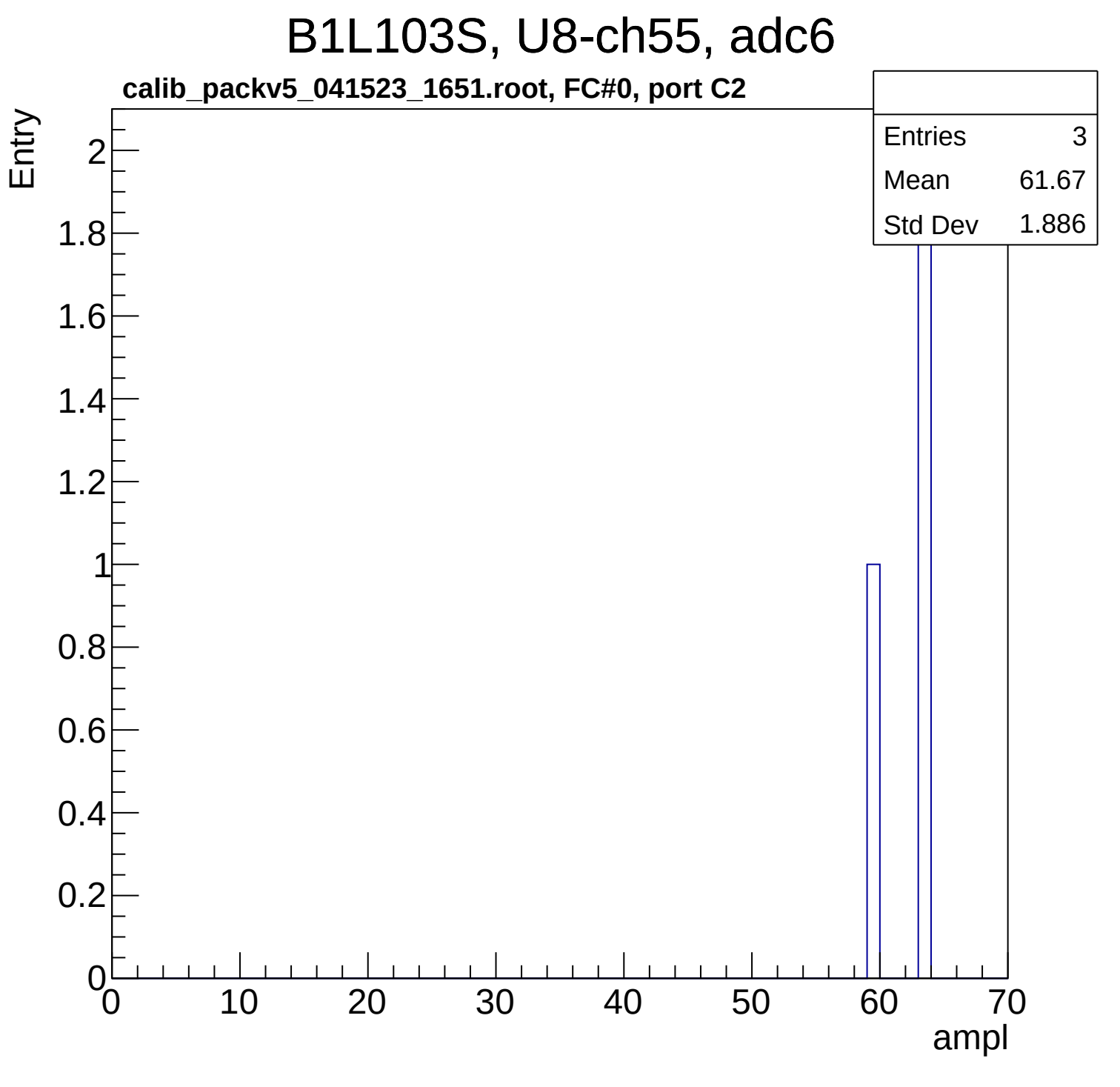
60
70


B1L103S, U8-ch55, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 61.67
Std Dev 1.886
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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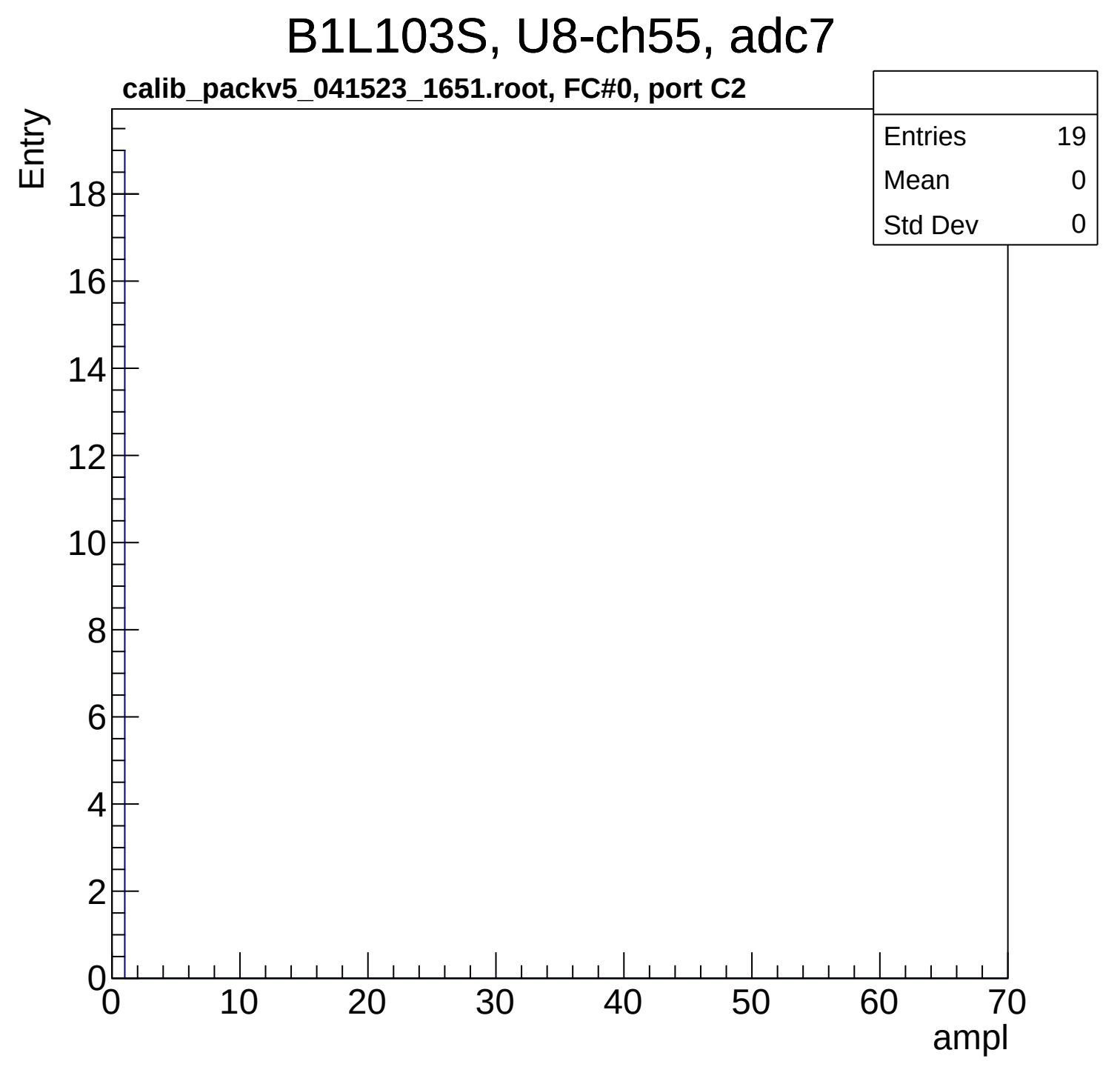
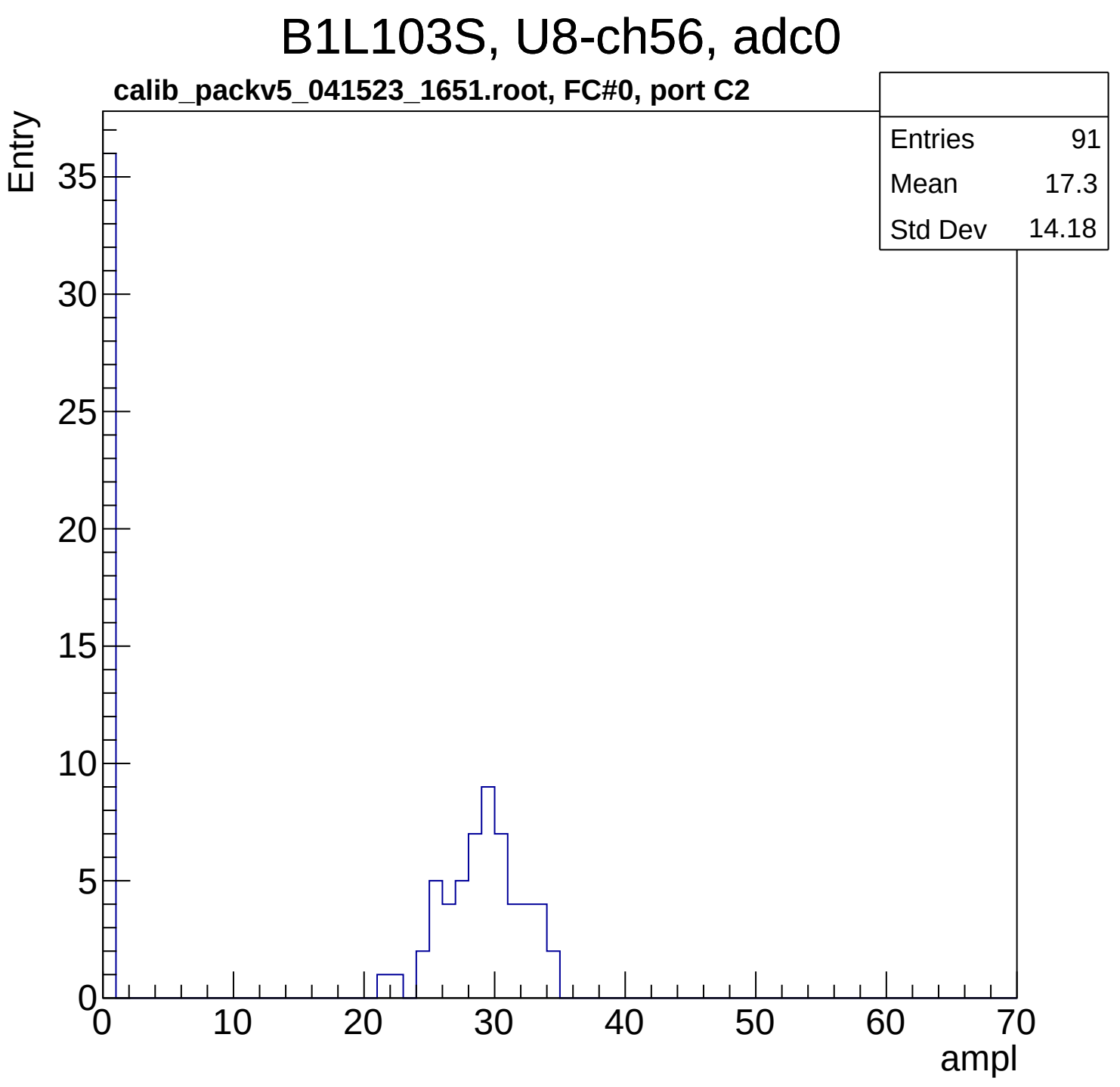
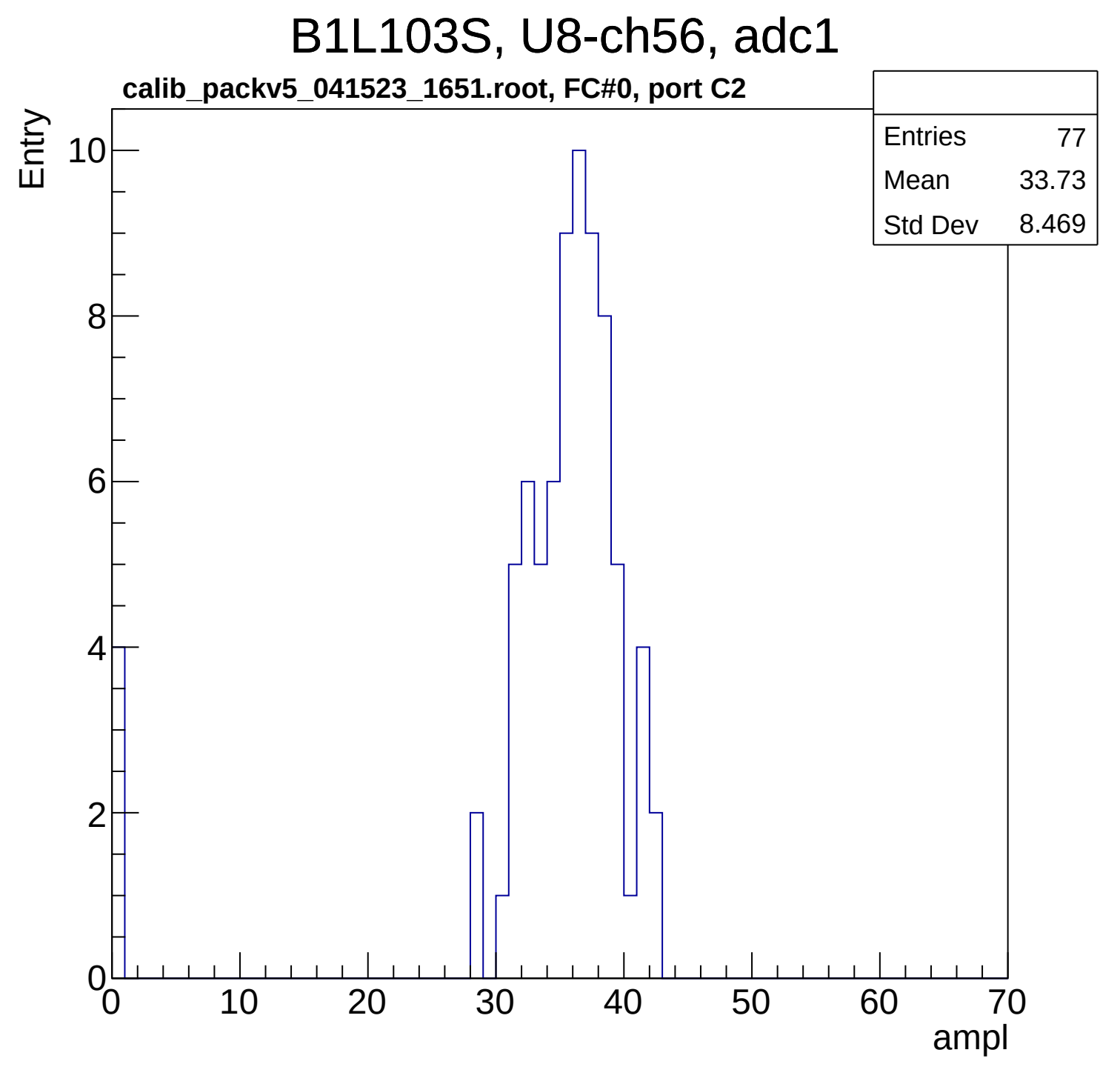

B1L103S, U8-ch55, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch56, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 17.3
Std Dev 14.18
Entry
0
5
10
15
20
25
30
35
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch56, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 33.73
Std Dev 8.469
Entry
ampl
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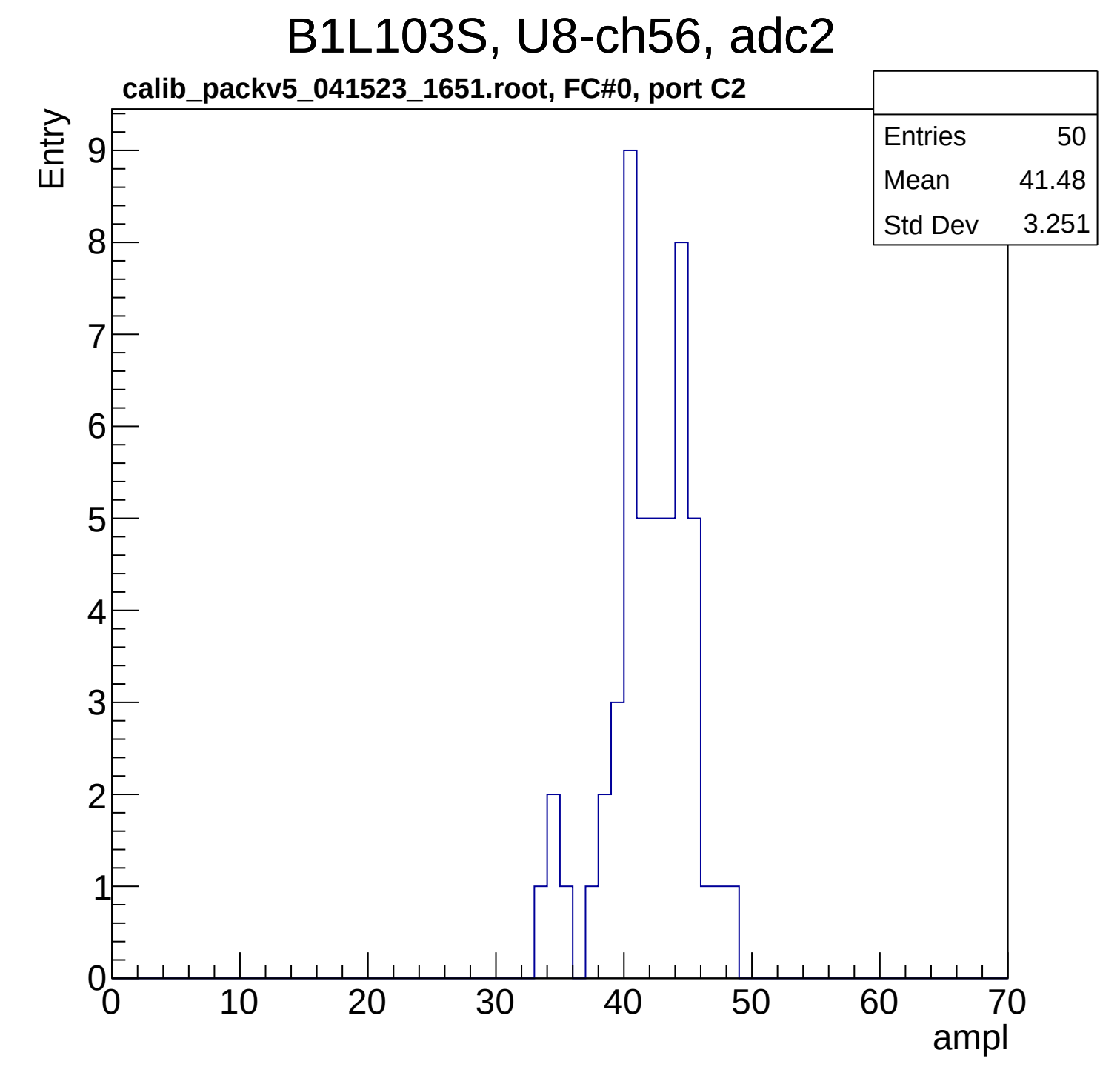
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U8-ch56, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 41.48
Std Dev 3.251
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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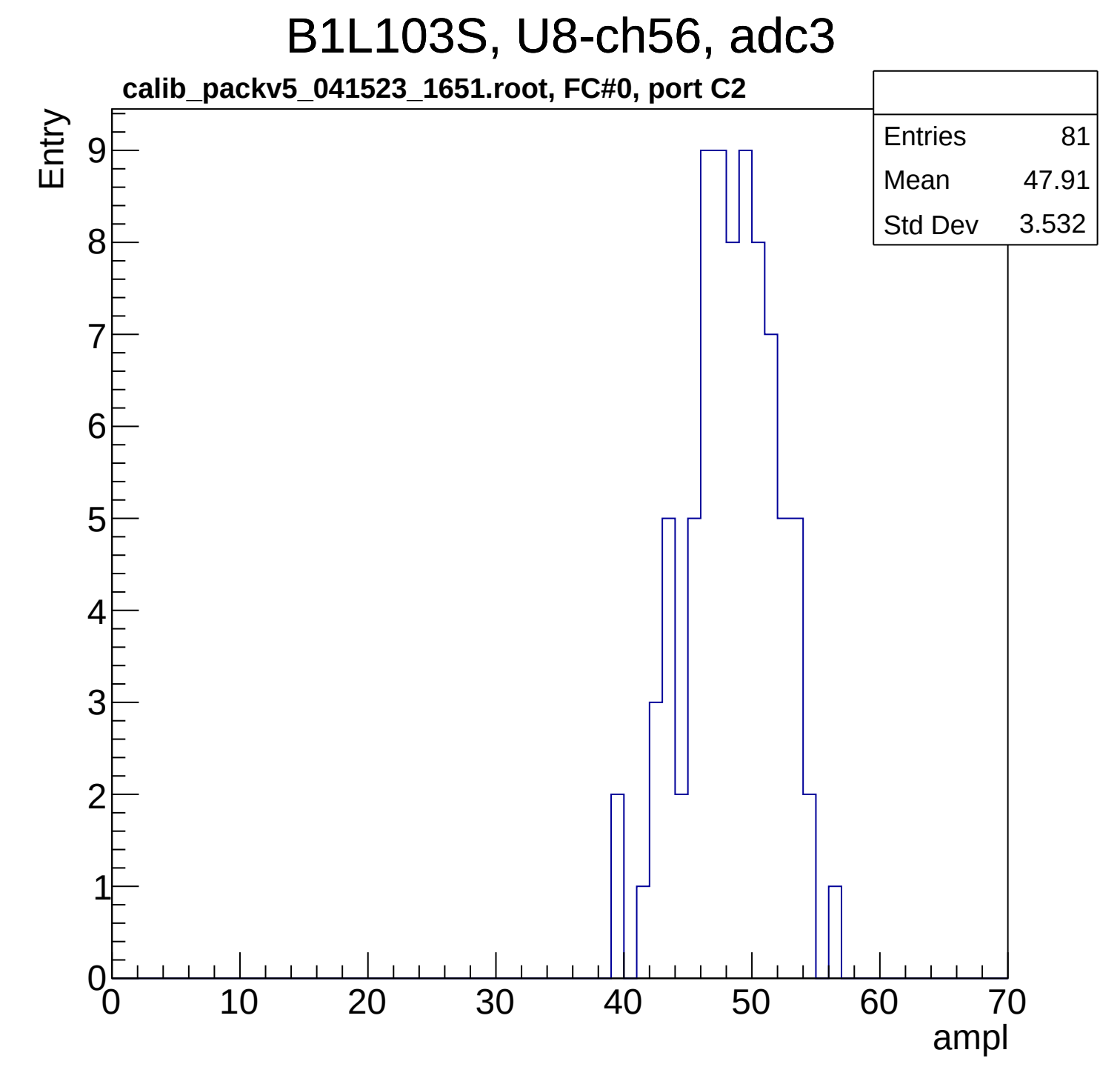
B1L103S, U8-ch56, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 47.91
Std Dev 3.532
Entry
ampl
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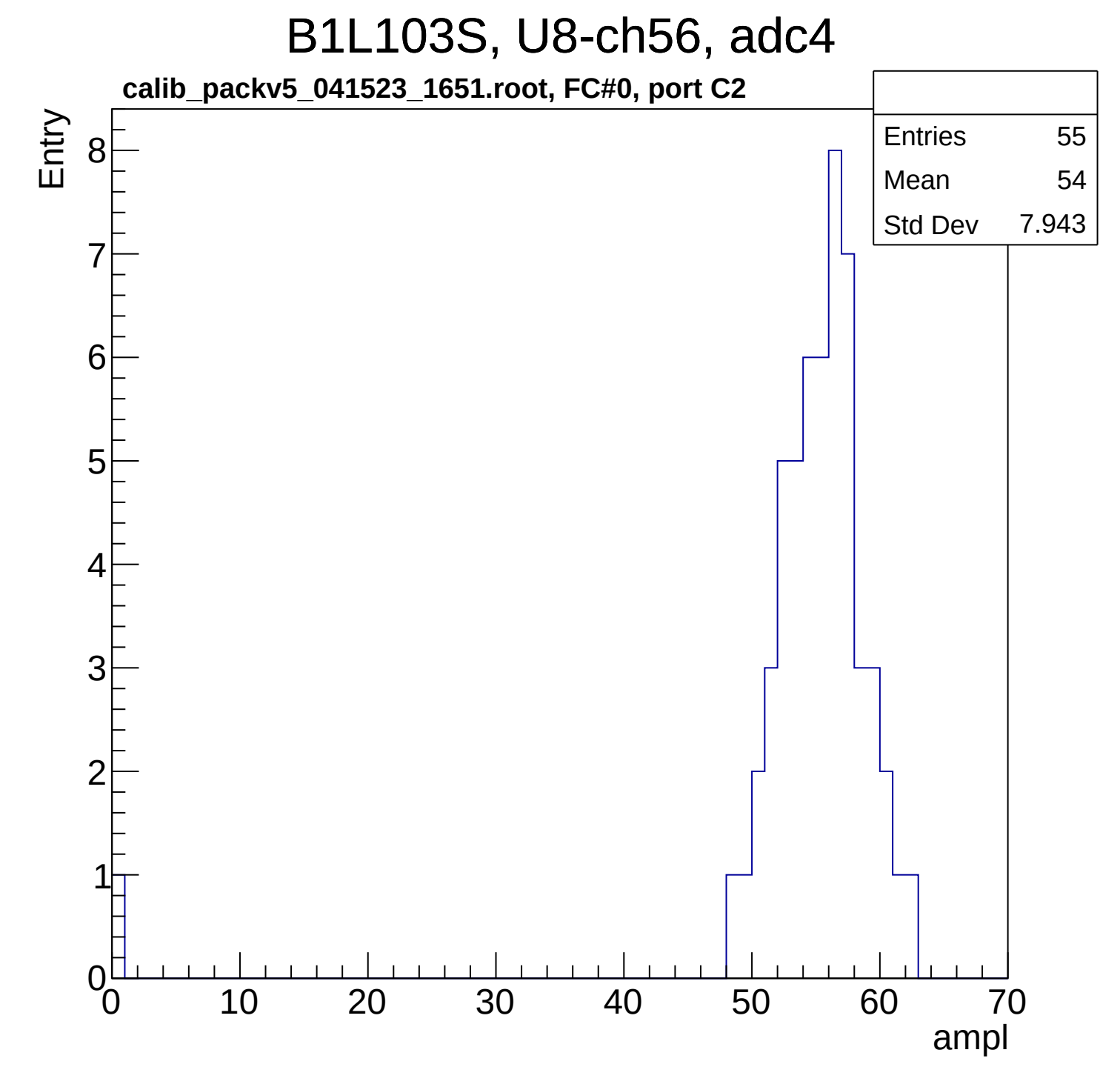
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U8-ch56, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 54
Std Dev 7.943
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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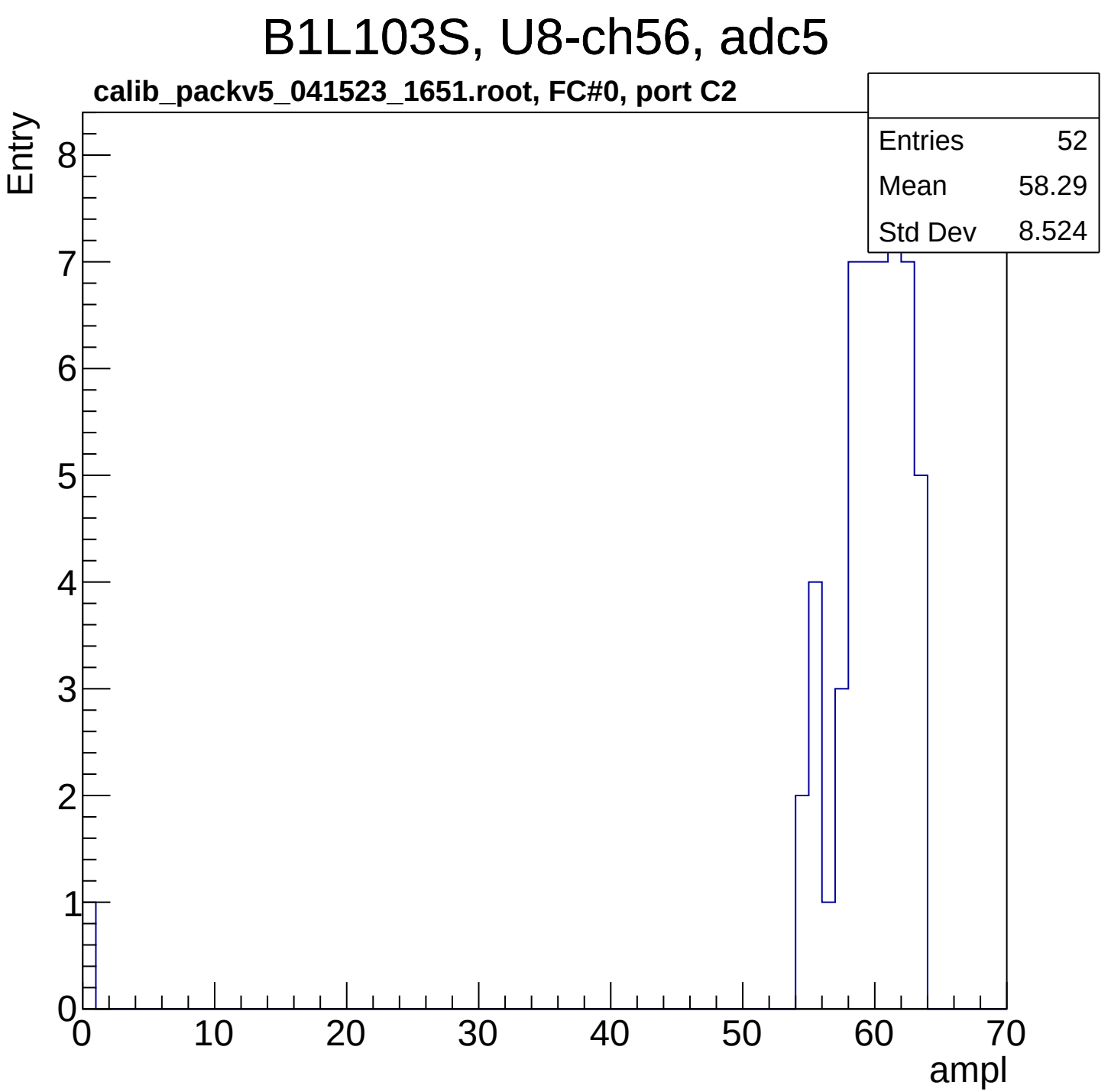
B1L103S, U8-ch56, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 58.29
Std Dev 8.524
Entry
ampl
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2
3
4
5
6
7
8
0
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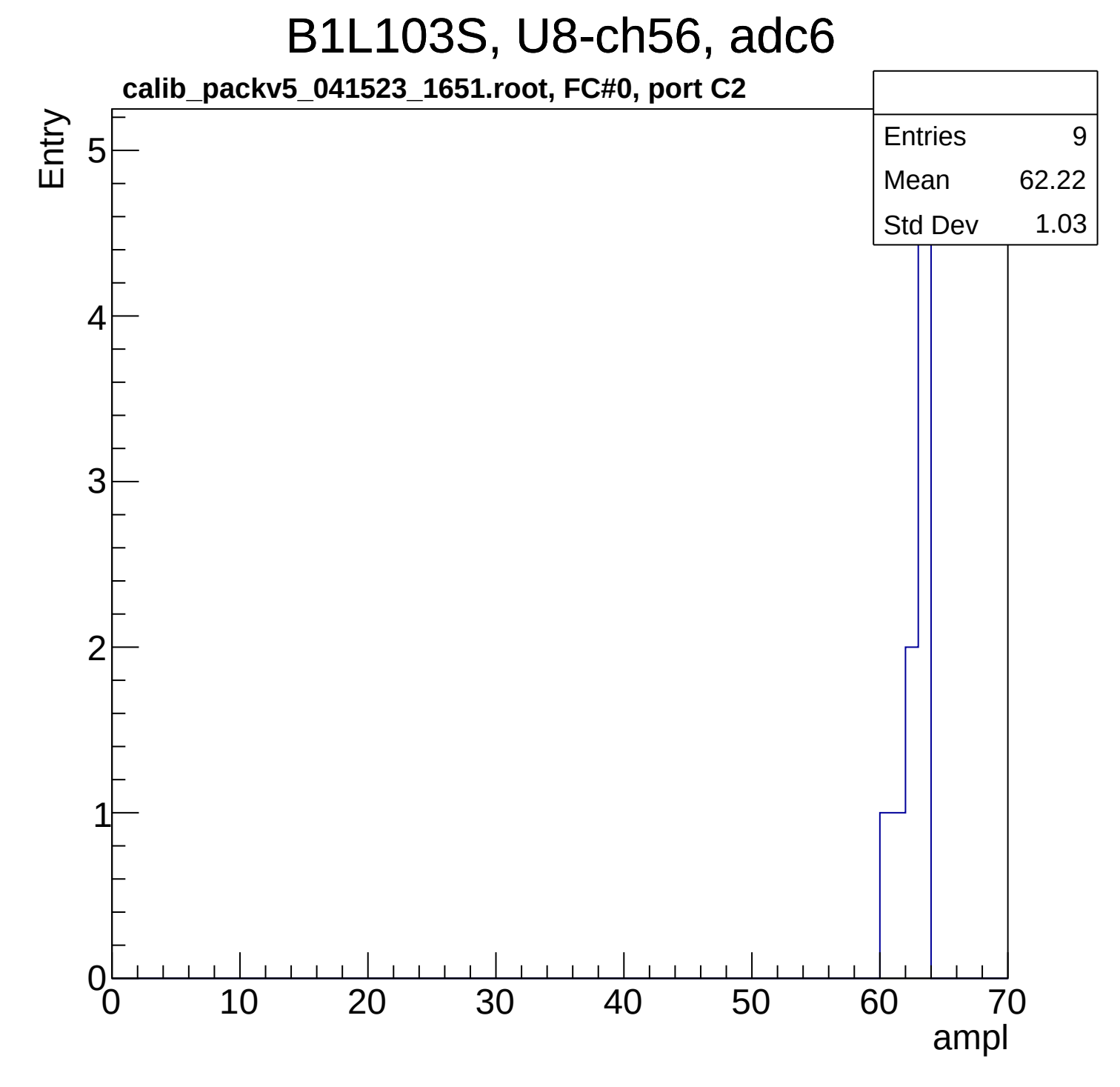
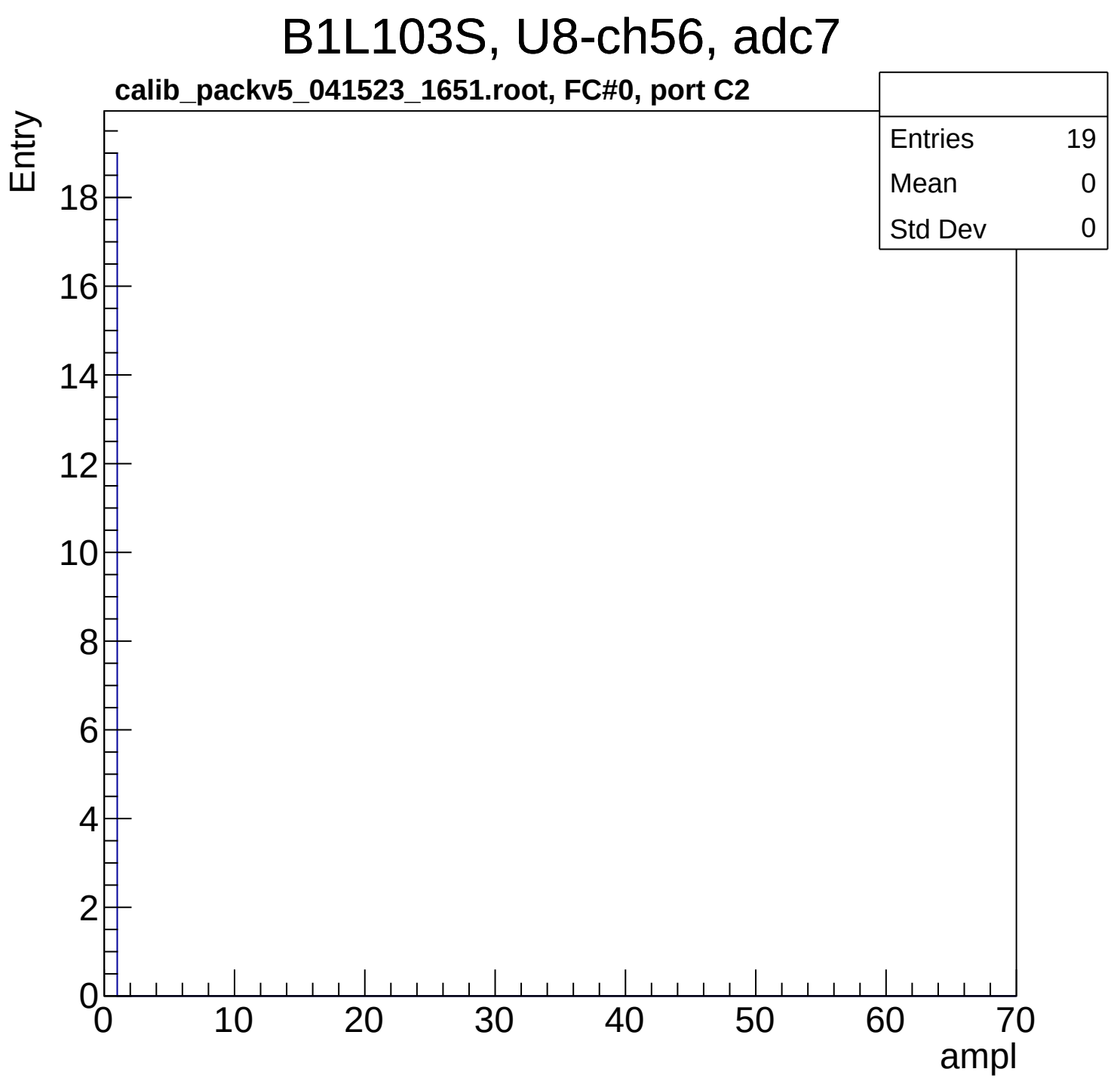
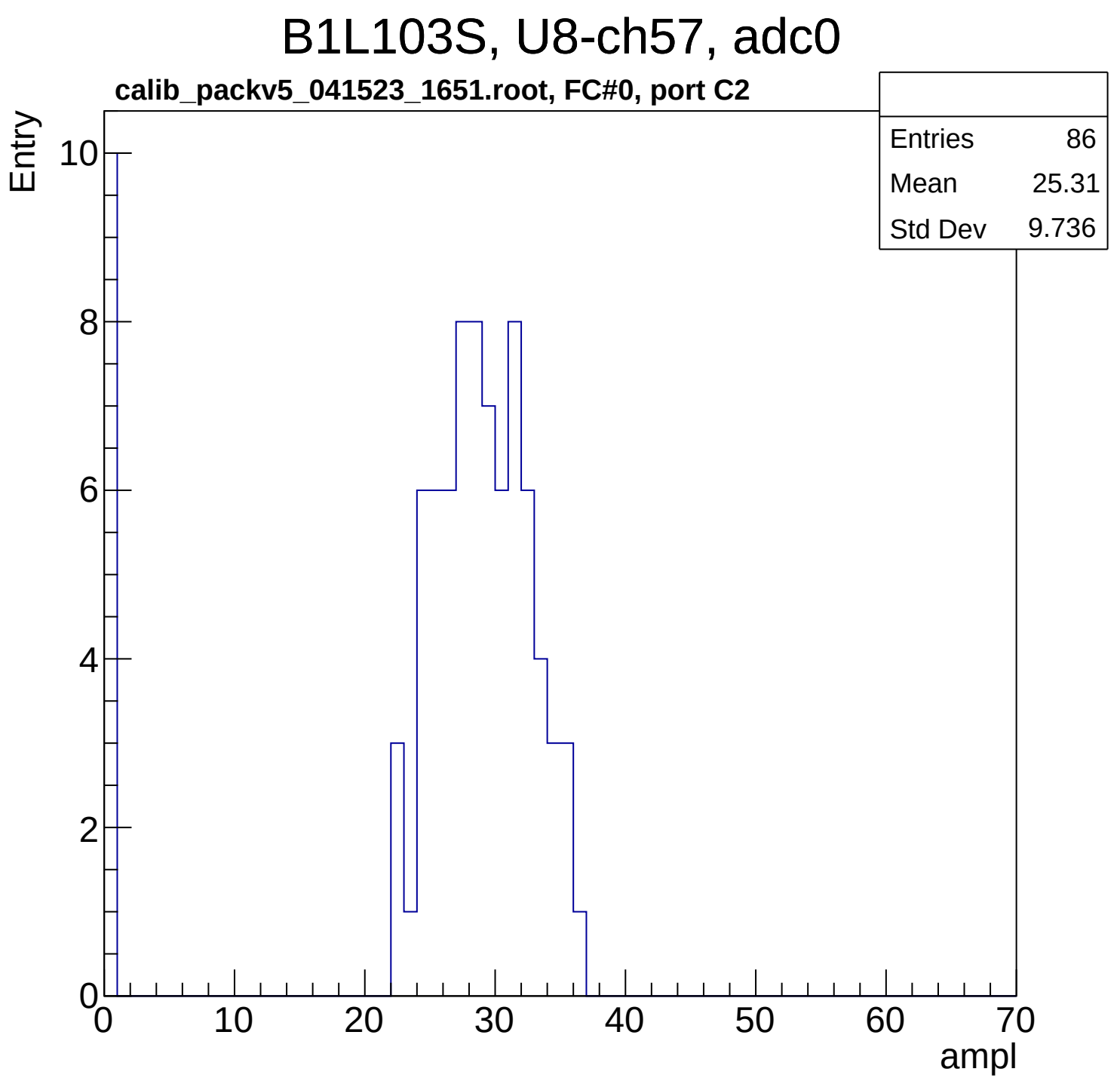
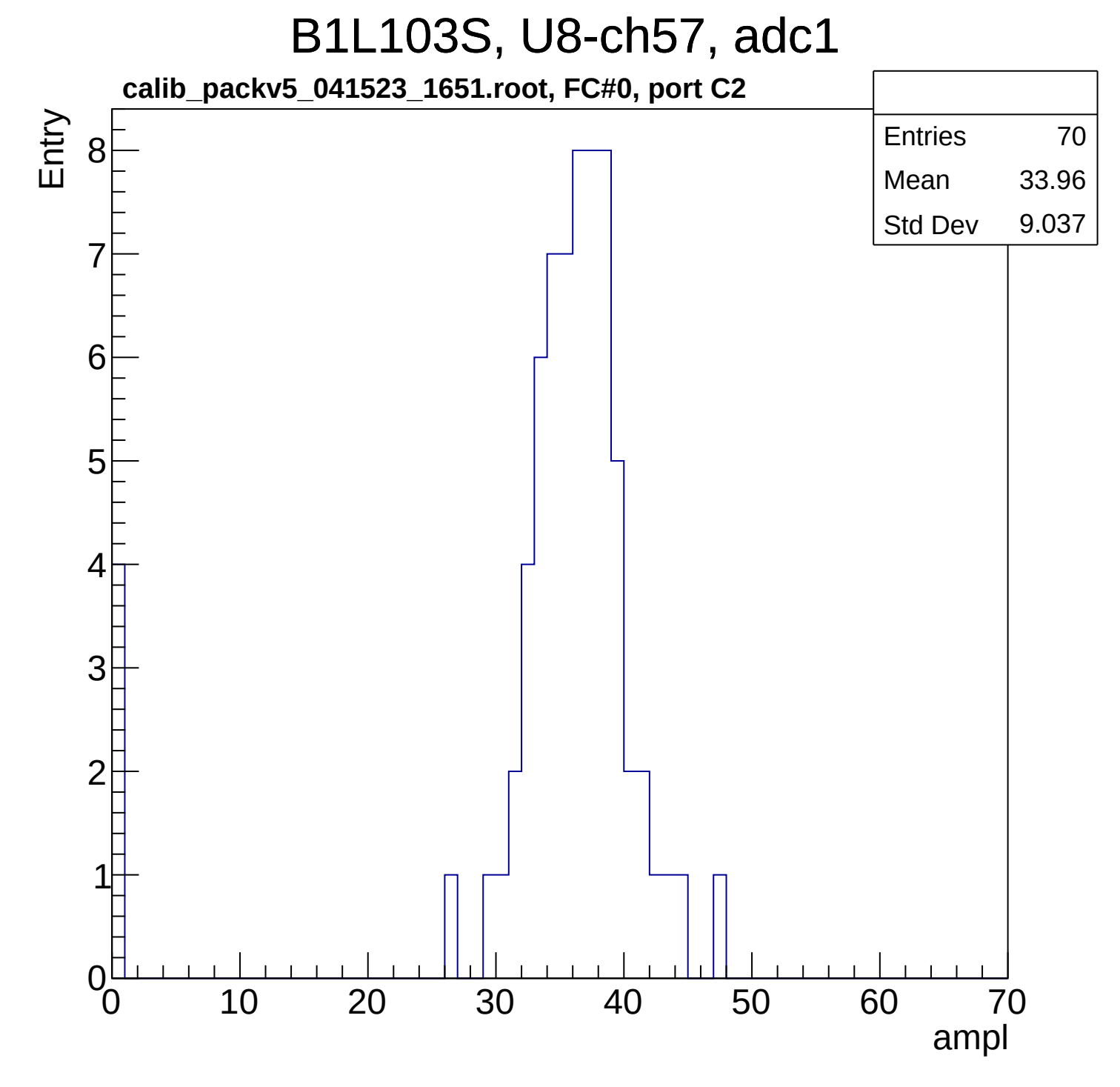
20
30
40
50
60
70


B1L103S, U8-ch56, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 62.22
Std Dev 1.03
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U8-ch56, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch57, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 25.31
Std Dev 9.736
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U8-ch57, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 33.96
Std Dev 9.037
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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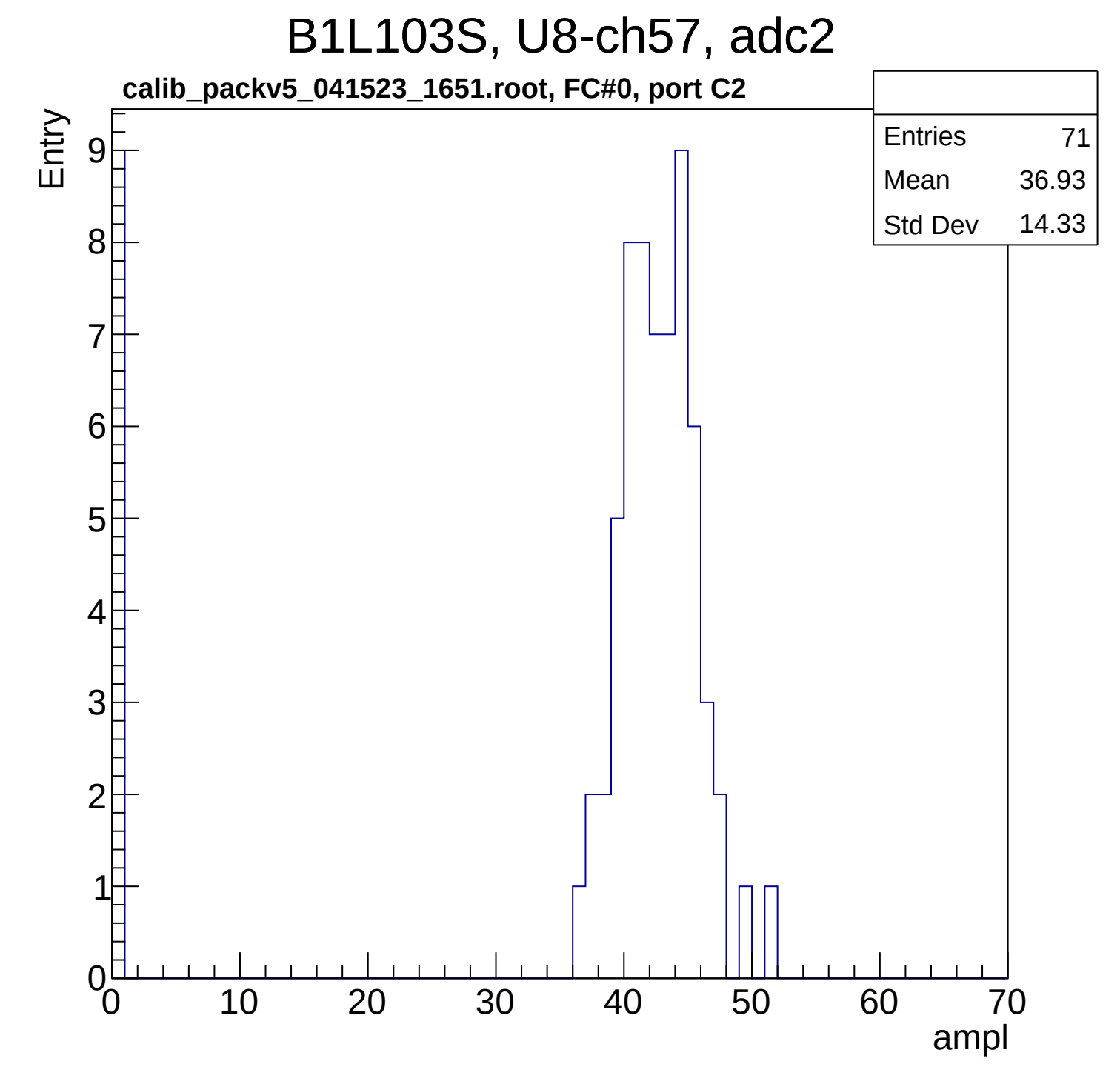
B1L103S, U8-ch57, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 36.93
Std Dev 14.33
Entry
ampl
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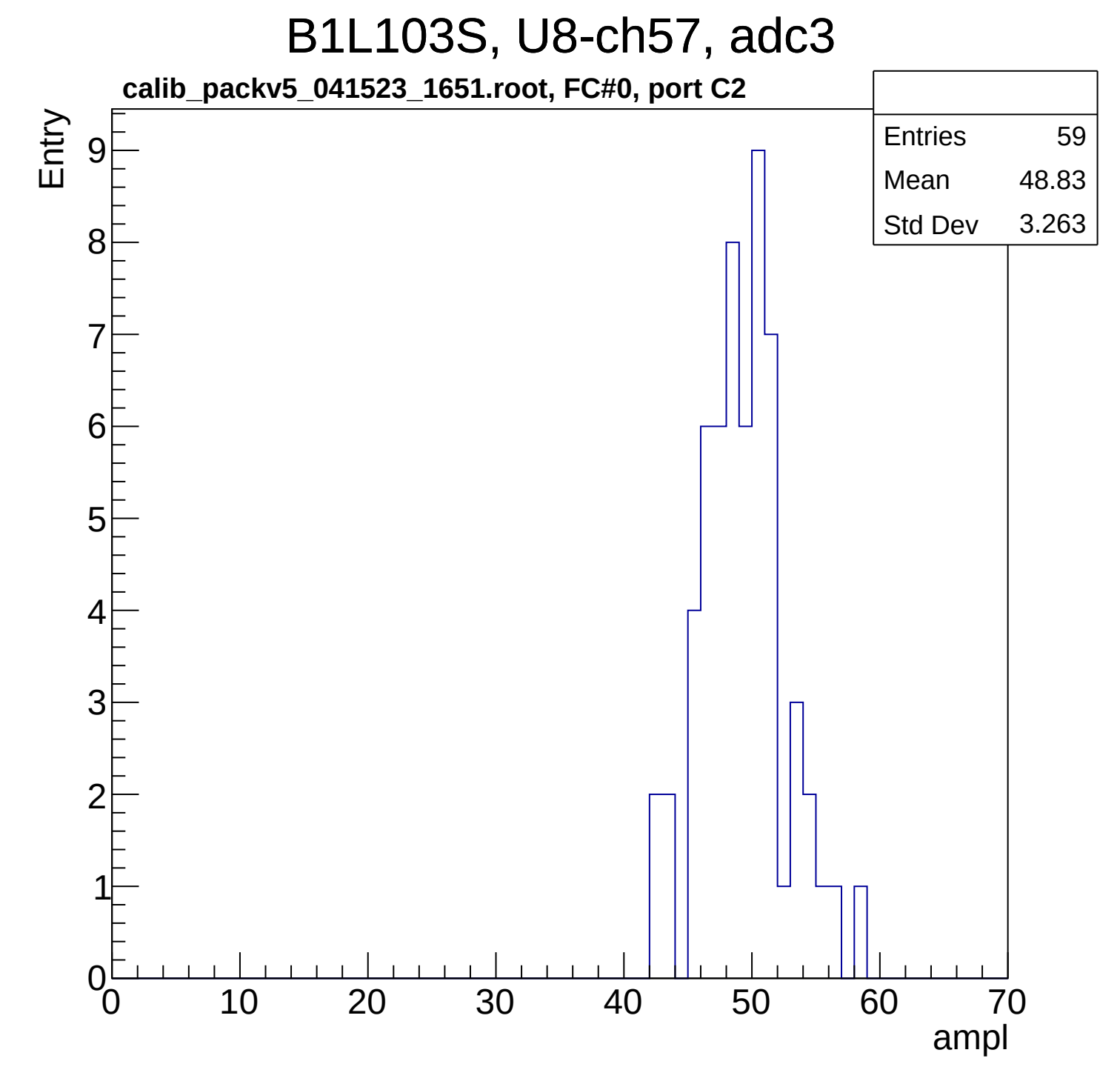
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U8-ch57, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 48.83
Std Dev 3.263
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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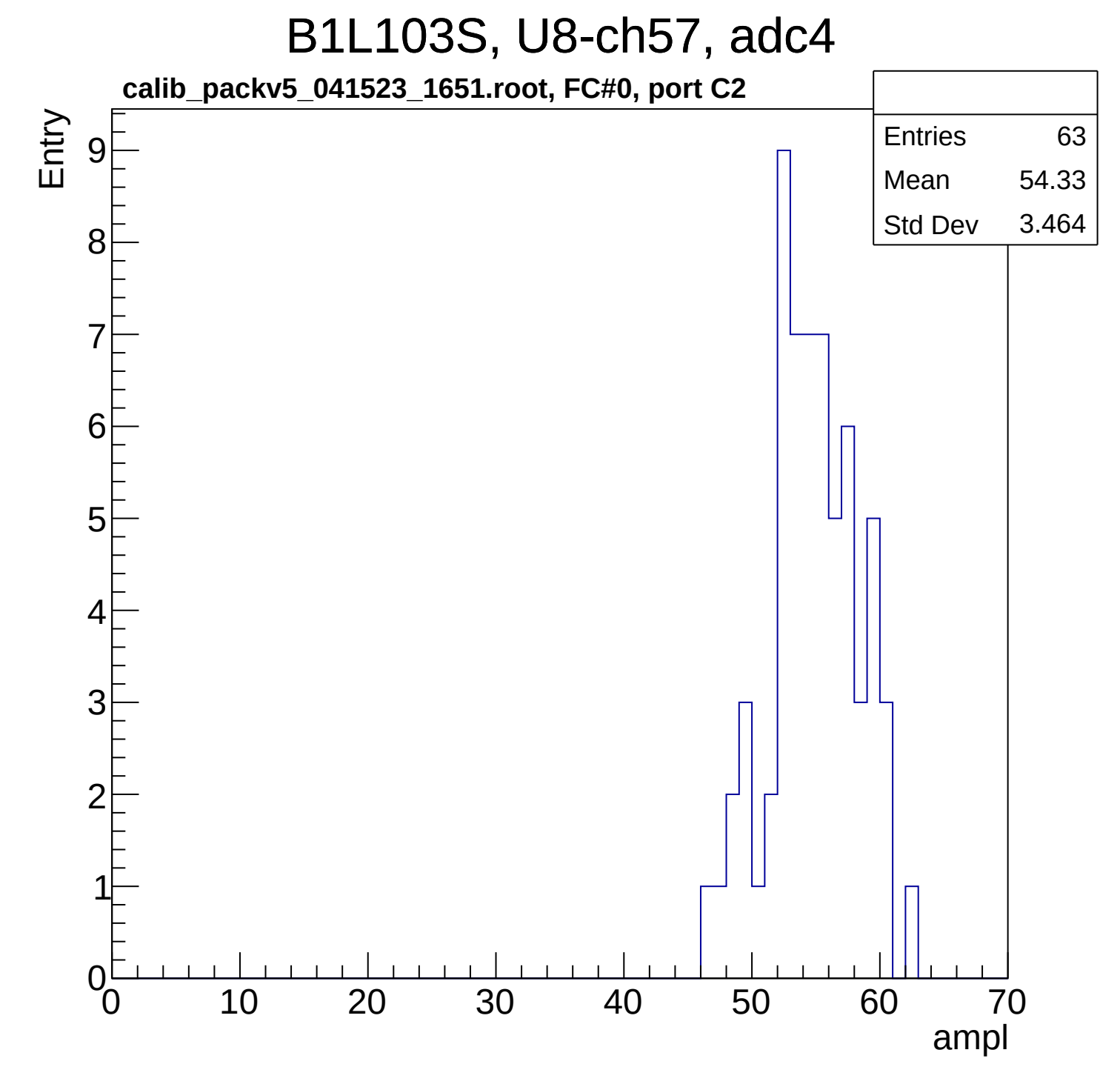
B1L103S, U8-ch57, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 54.33
Std Dev 3.464
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
30
40
50
60
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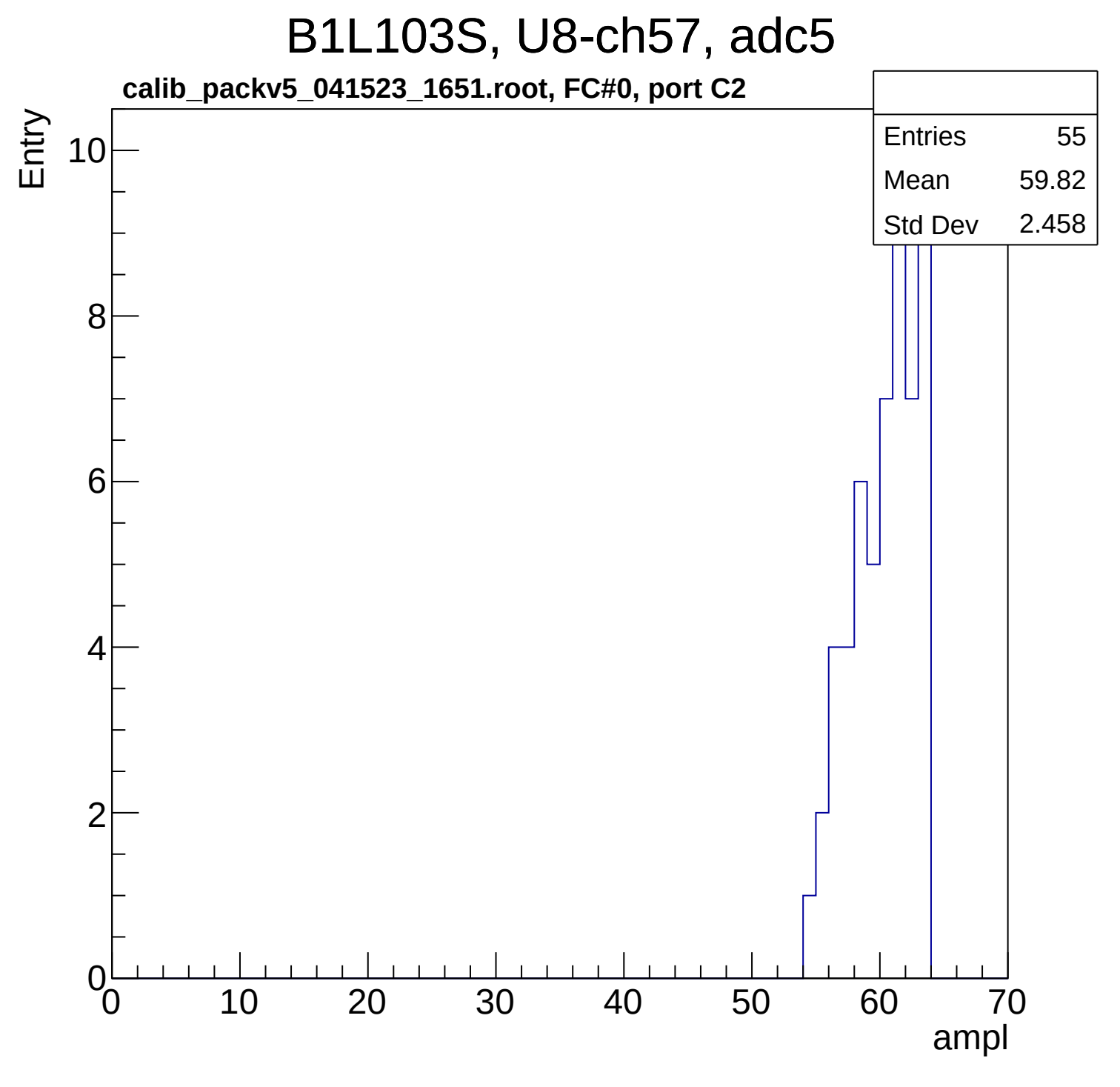
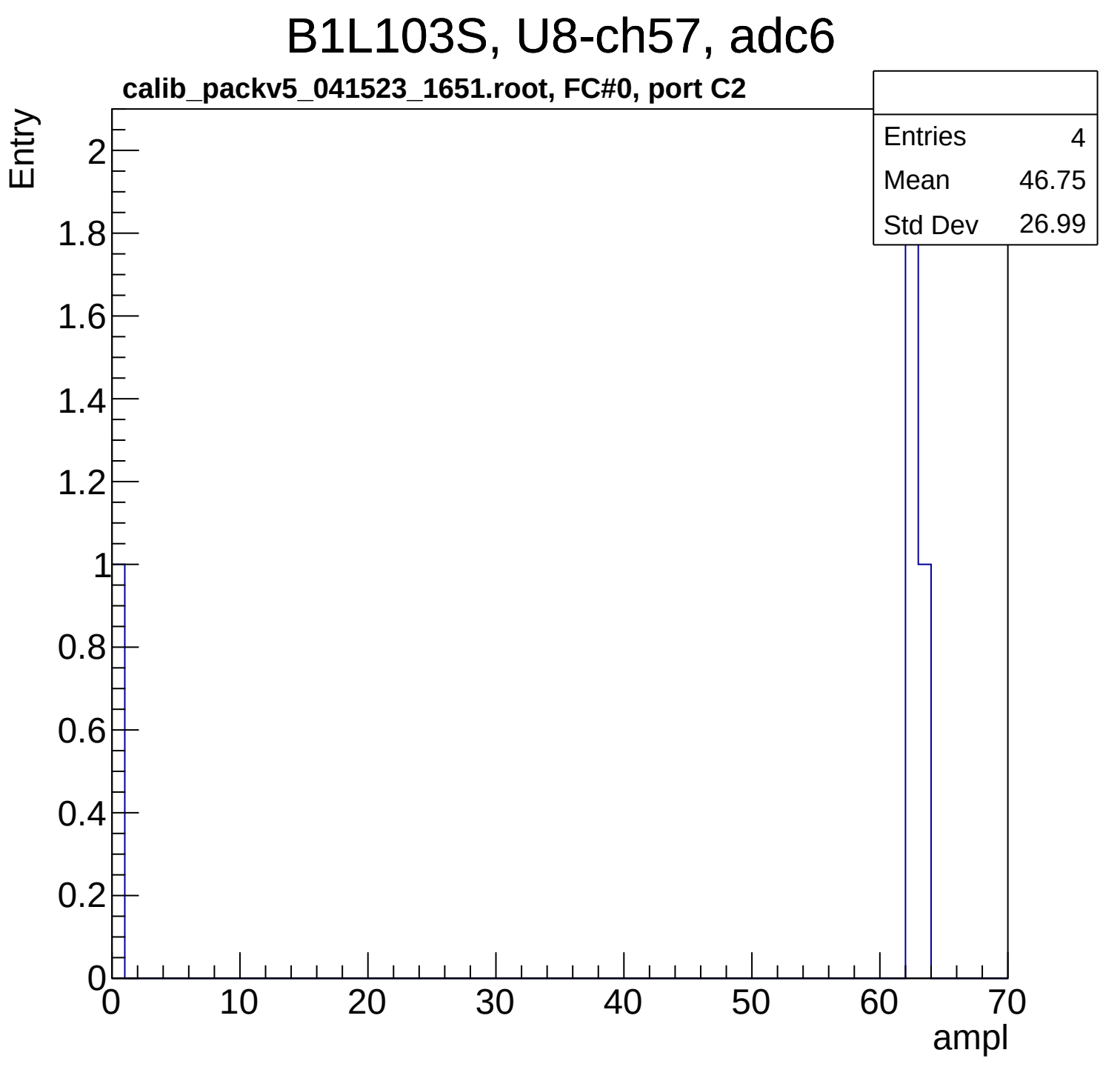
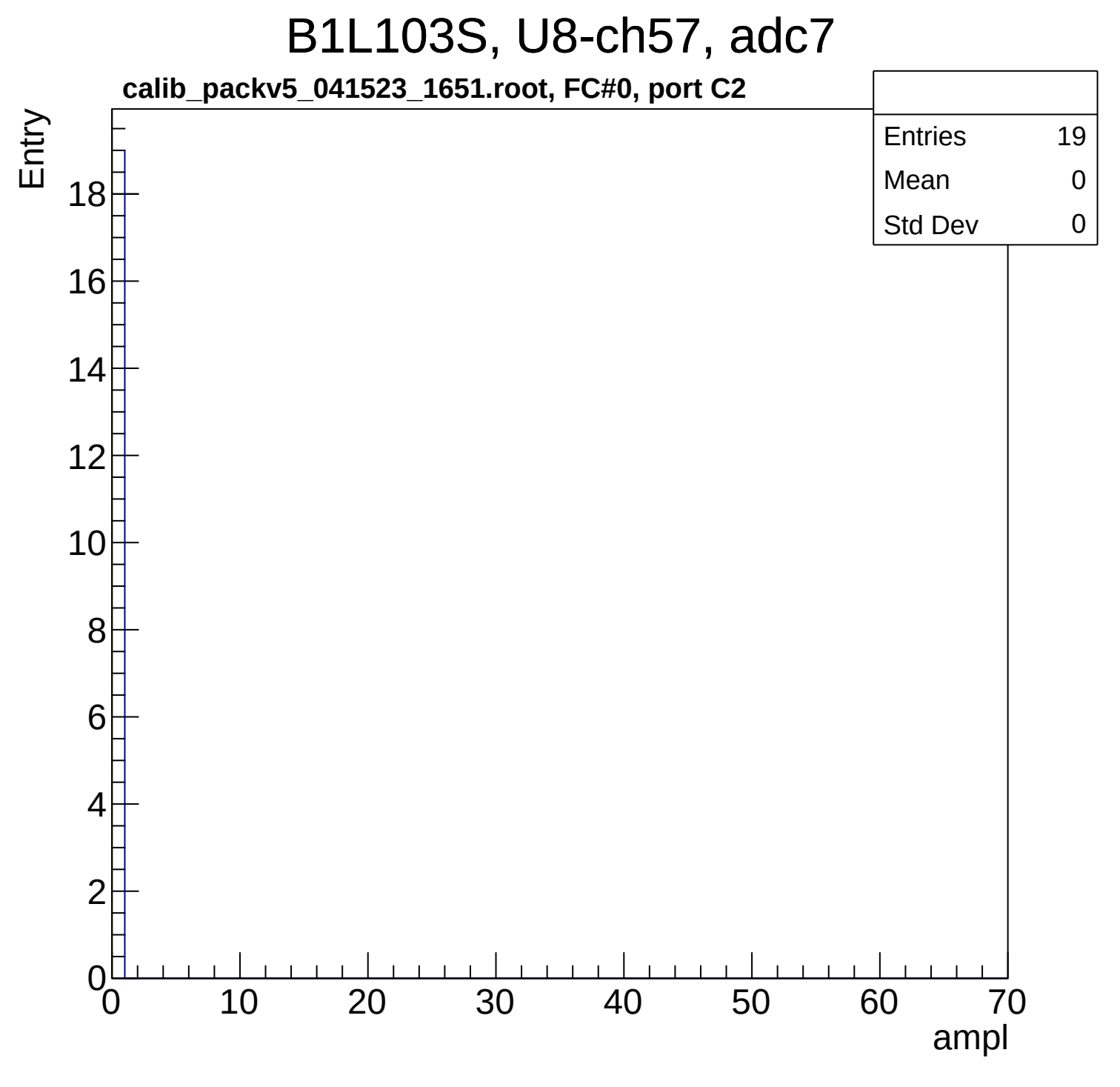
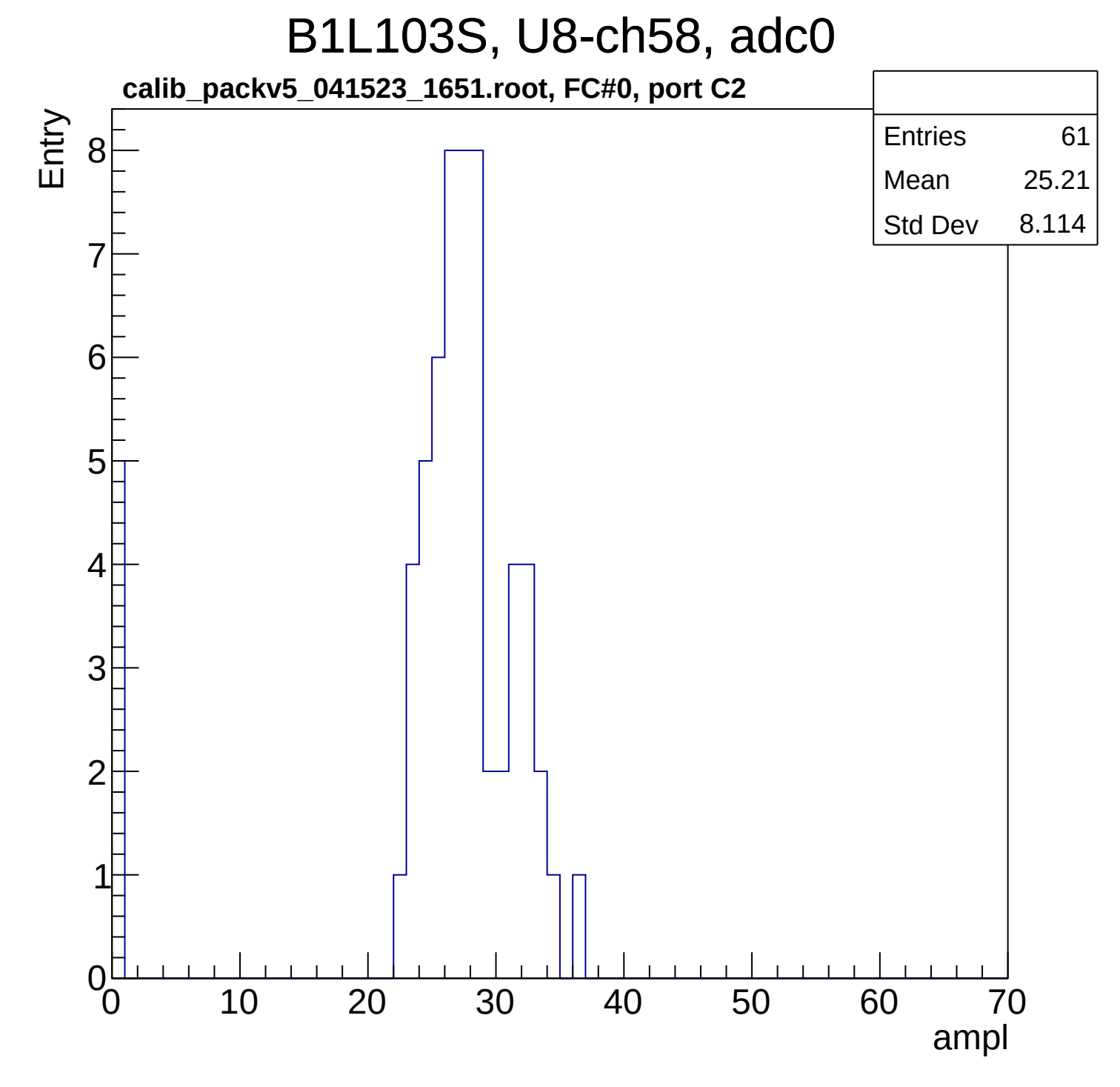

B1L103S, U8-ch57, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 59.82
Std Dev 2.458
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U8-ch57, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 46.75
Std Dev 26.99
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U8-ch57, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch58, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 25.21
Std Dev 8.114
Entry
ampl
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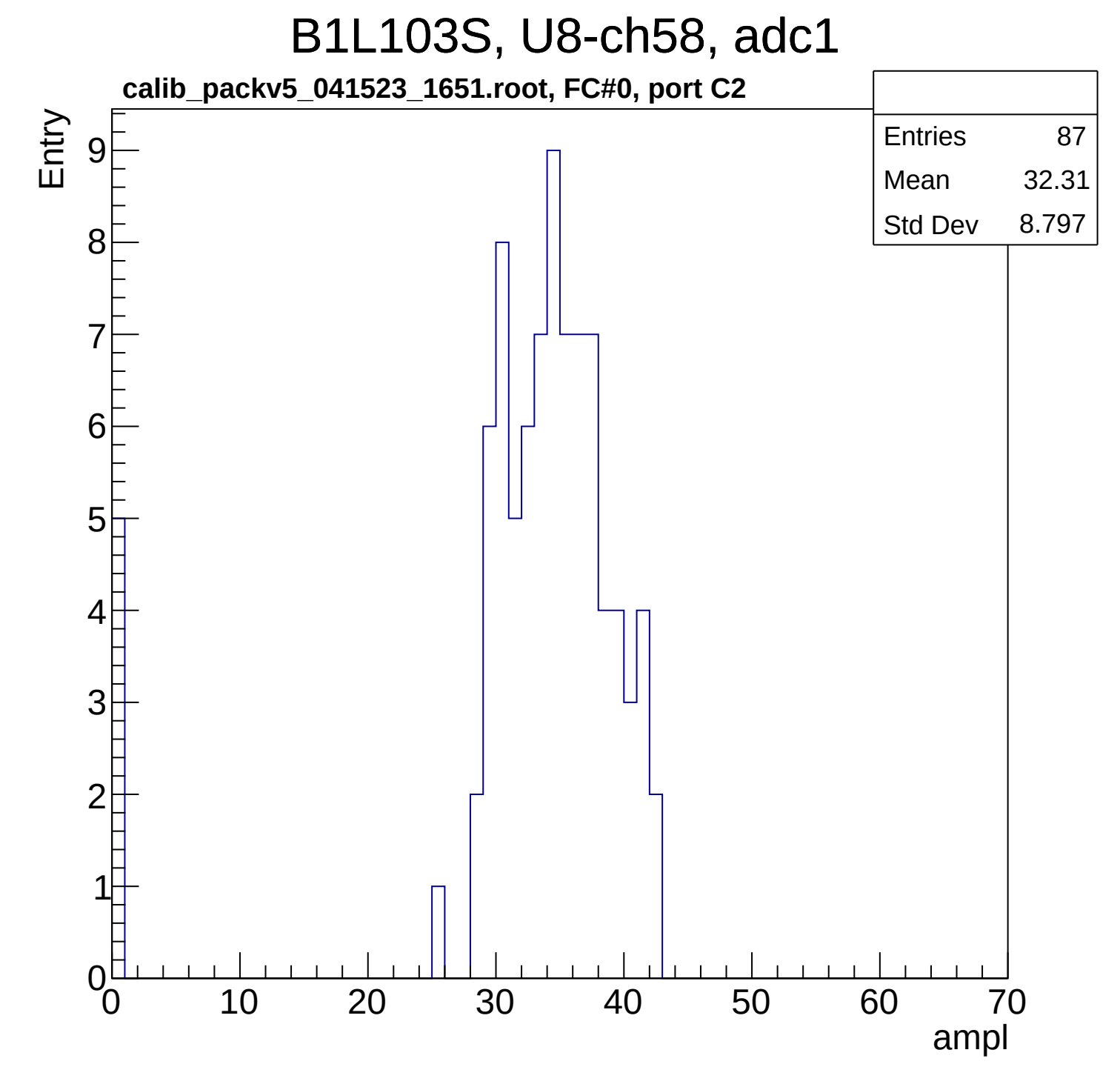
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch58, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 32.31
Std Dev 8.797
Entry
ampl
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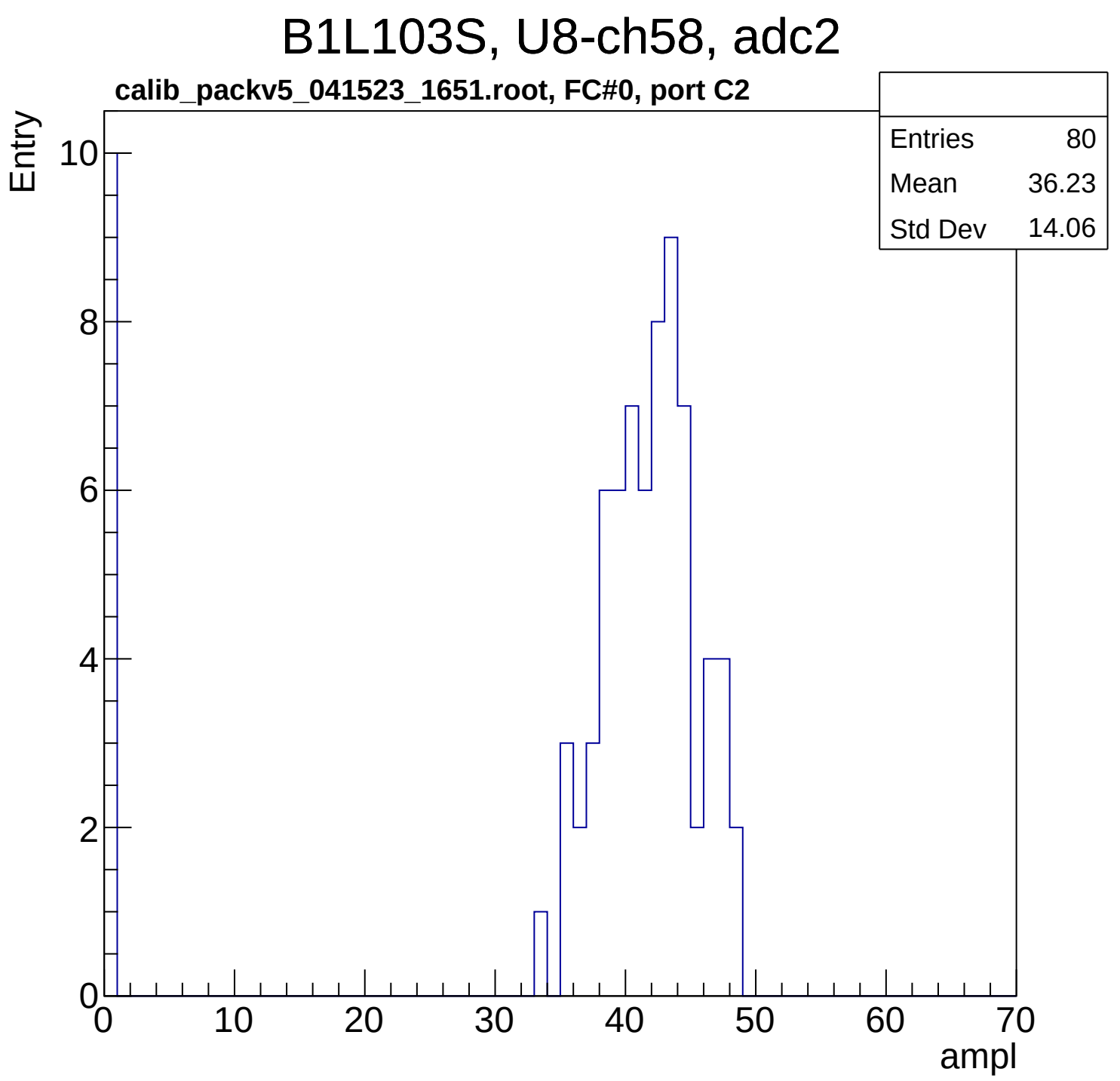
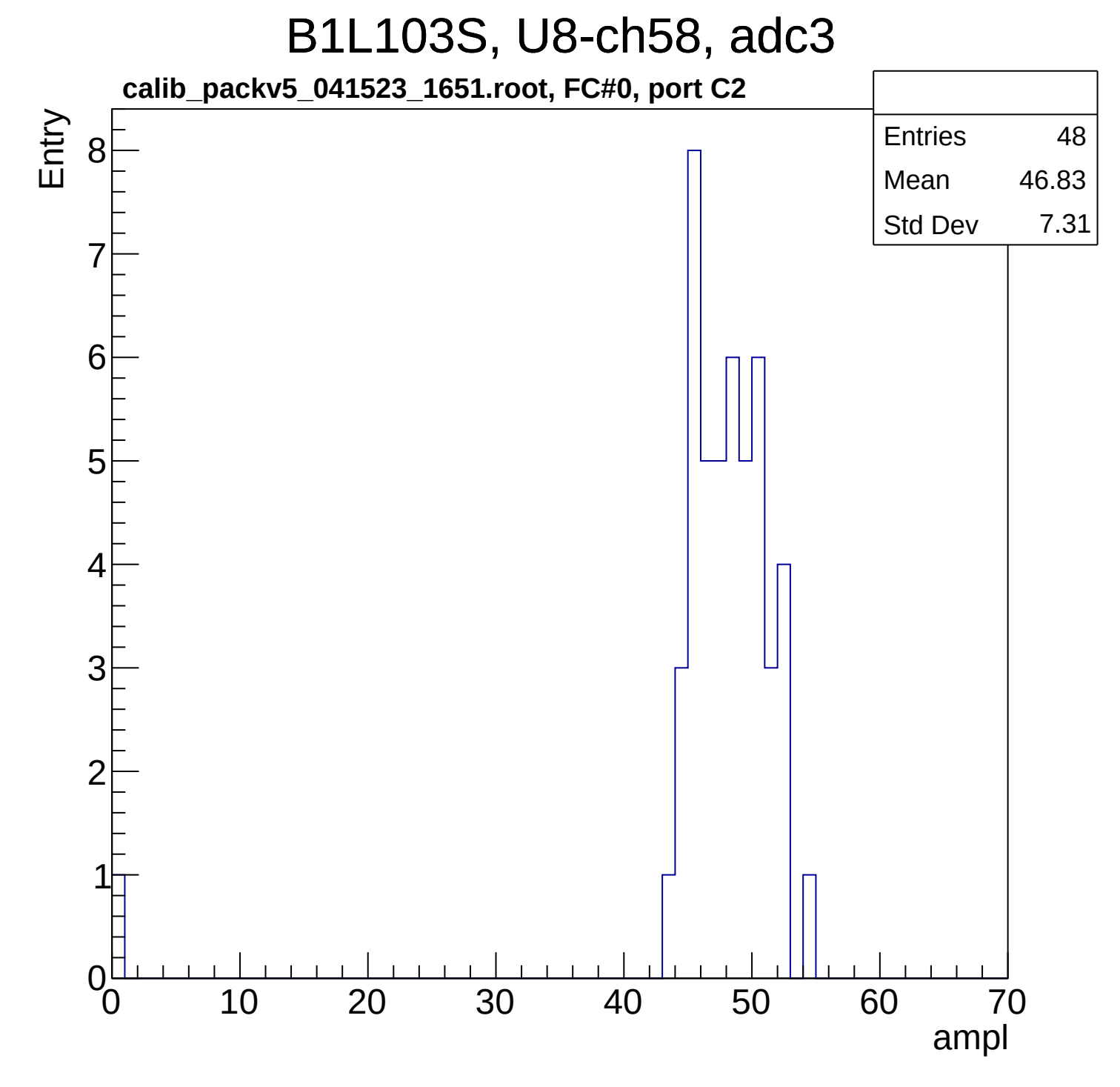
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U8-ch58, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 36.23
Std Dev 14.06
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U8-ch58, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 46.83
Std Dev 7.31
Entry
ampl
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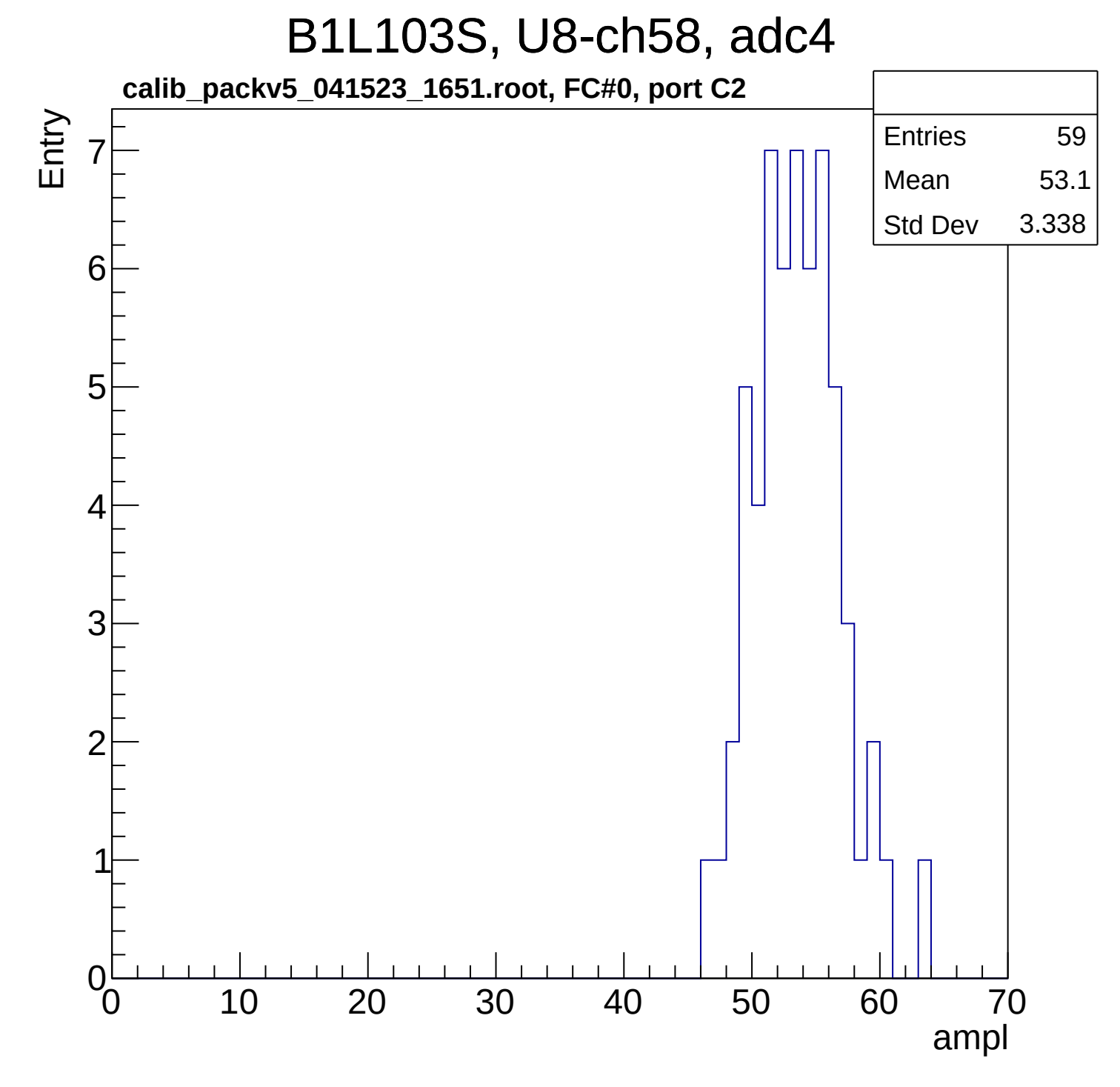
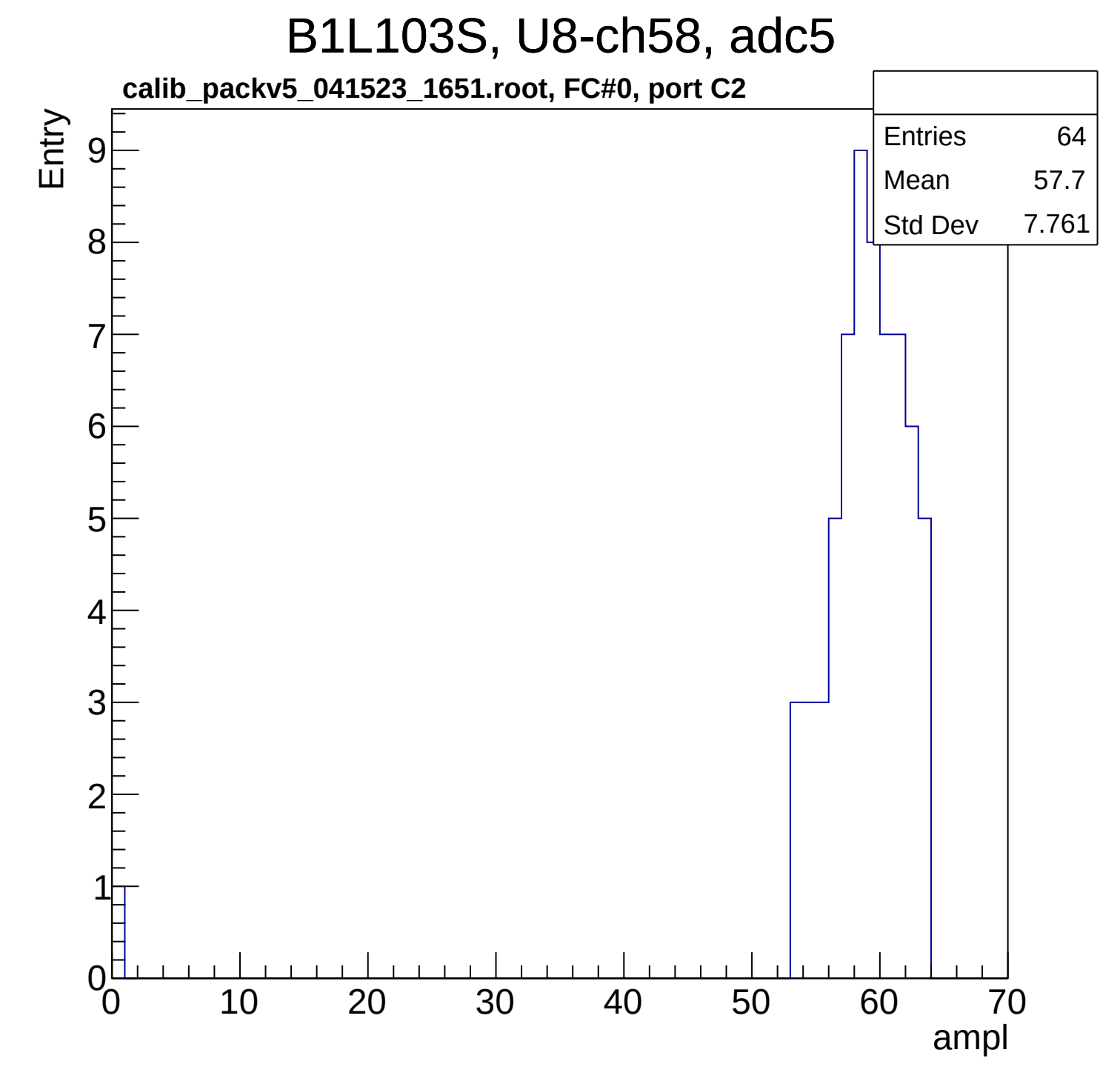
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch58, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 53.1
Std Dev 3.338
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U8-ch58, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 57.7
Std Dev 7.761
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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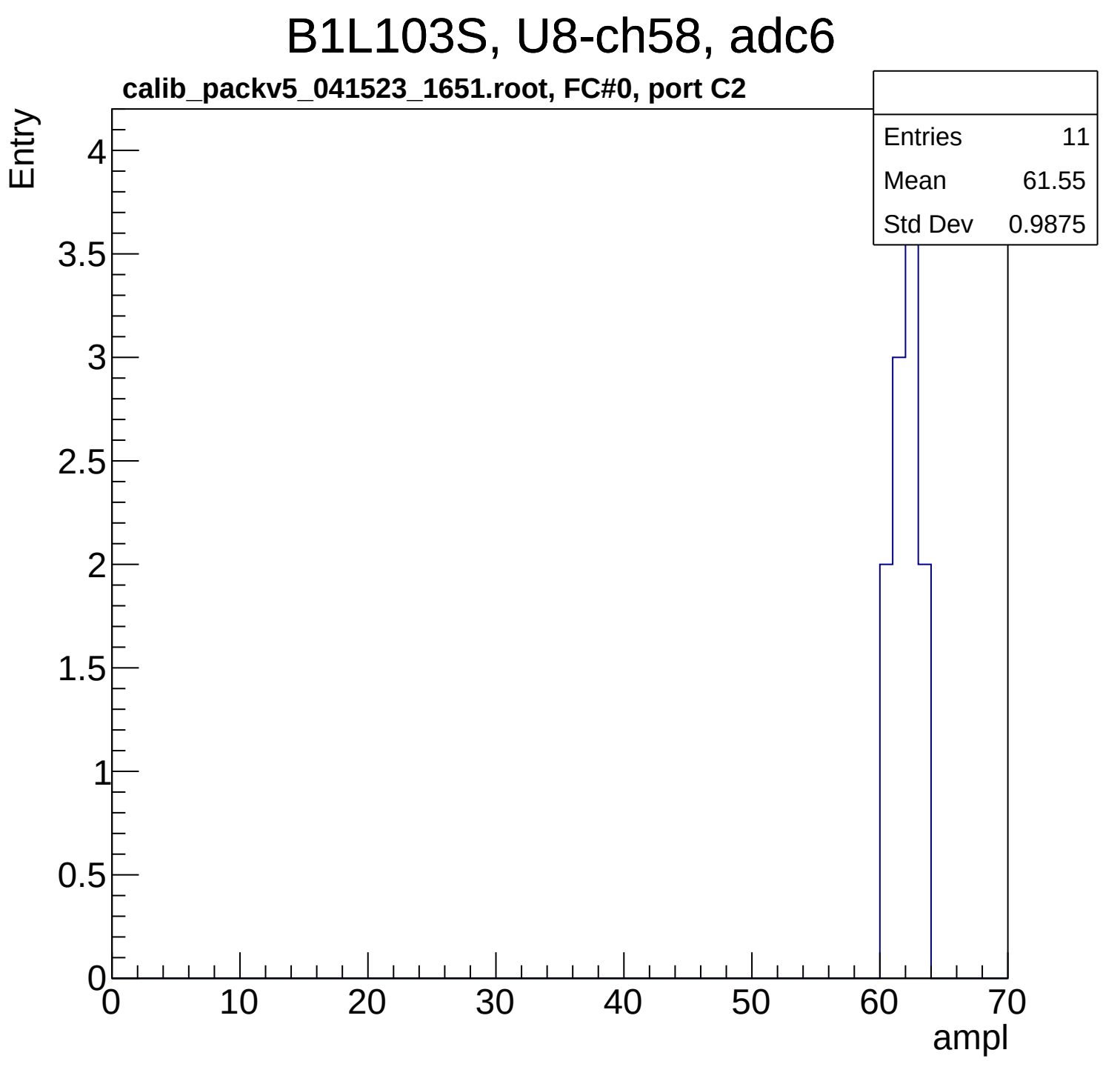
60
70


B1L103S, U8-ch58, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 61.55
Std Dev 0.9875
Entry
ampl
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0.5
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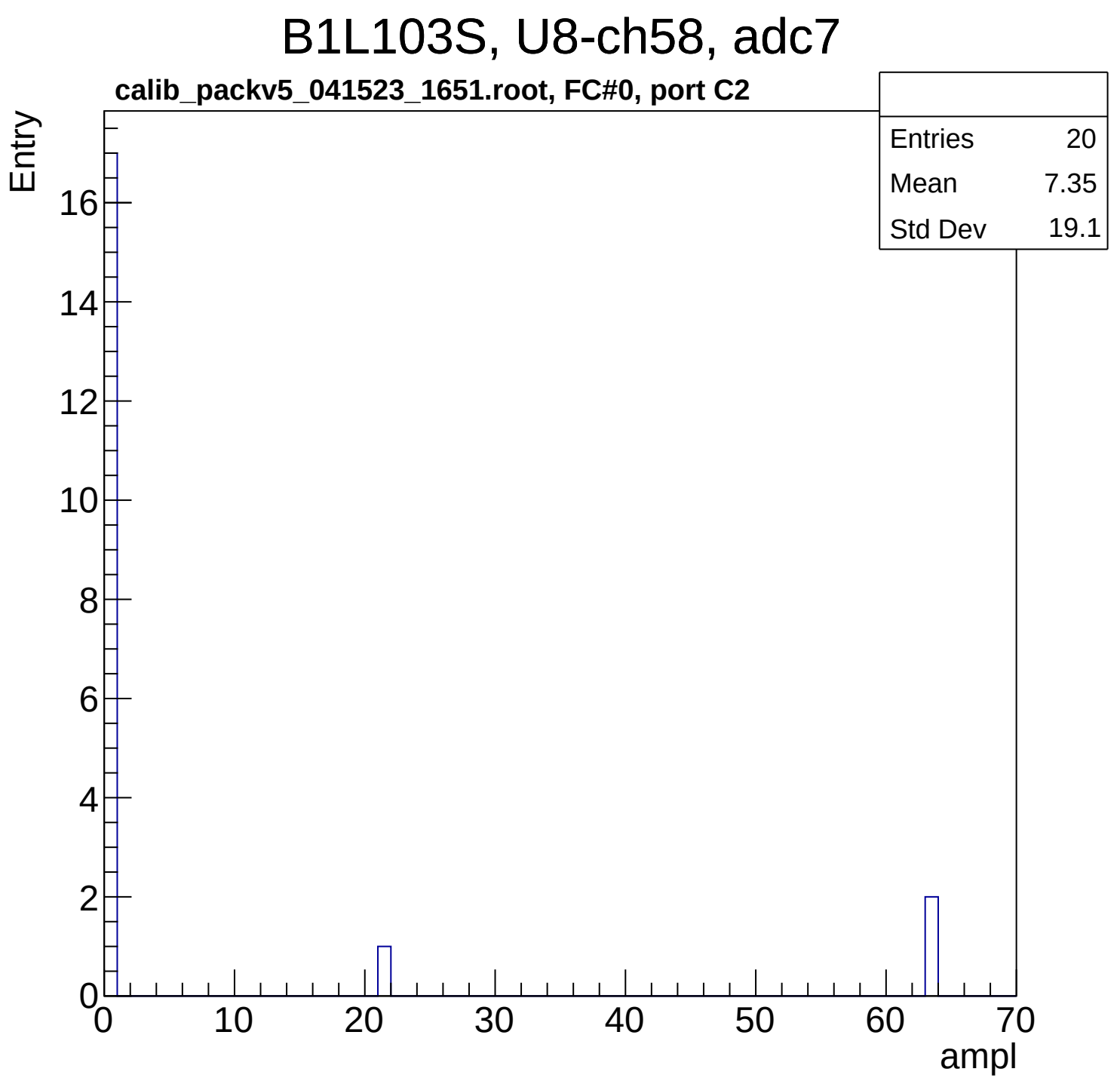
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U8-ch58, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 7.35
Std Dev 19.1
Entry
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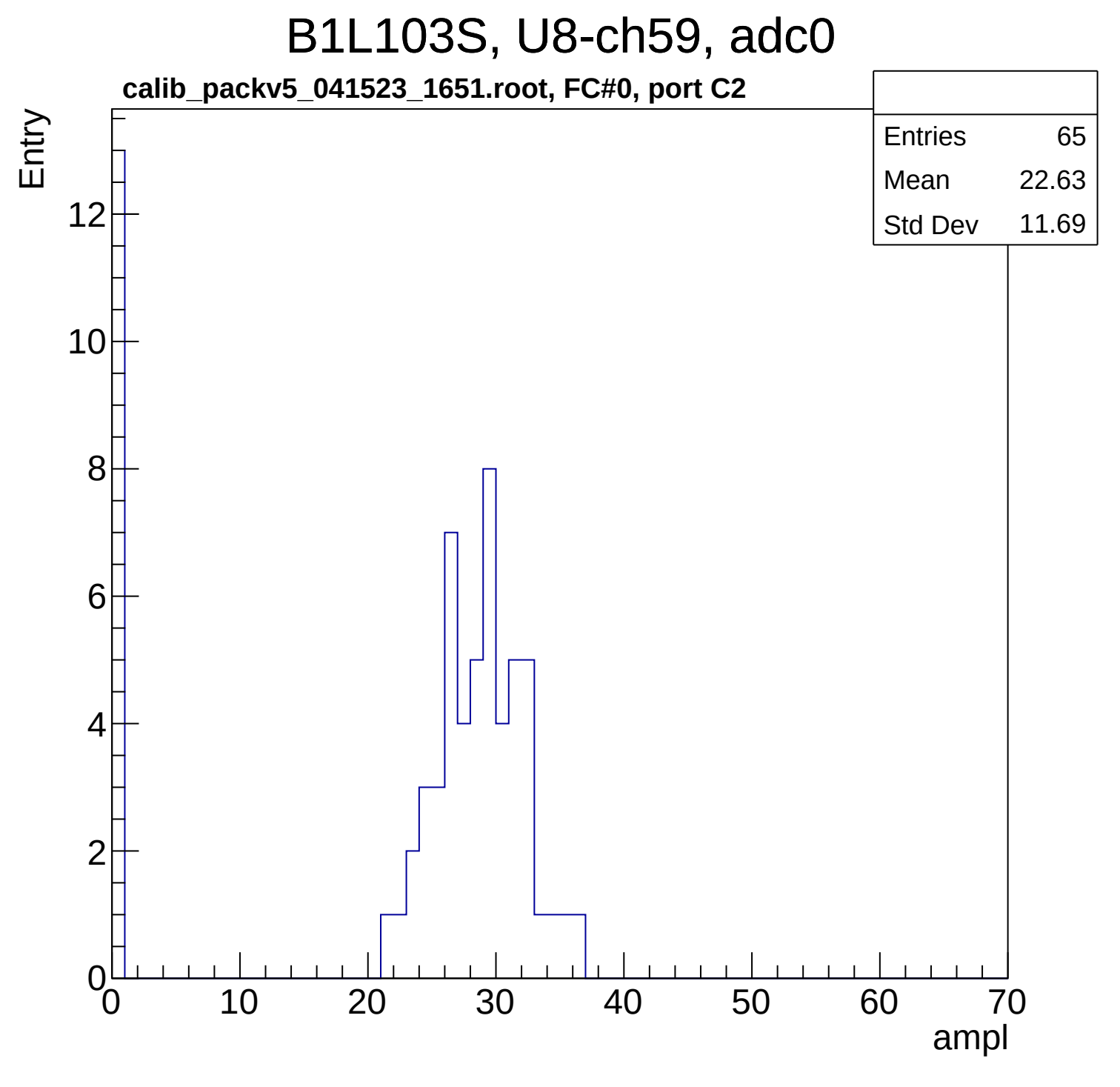
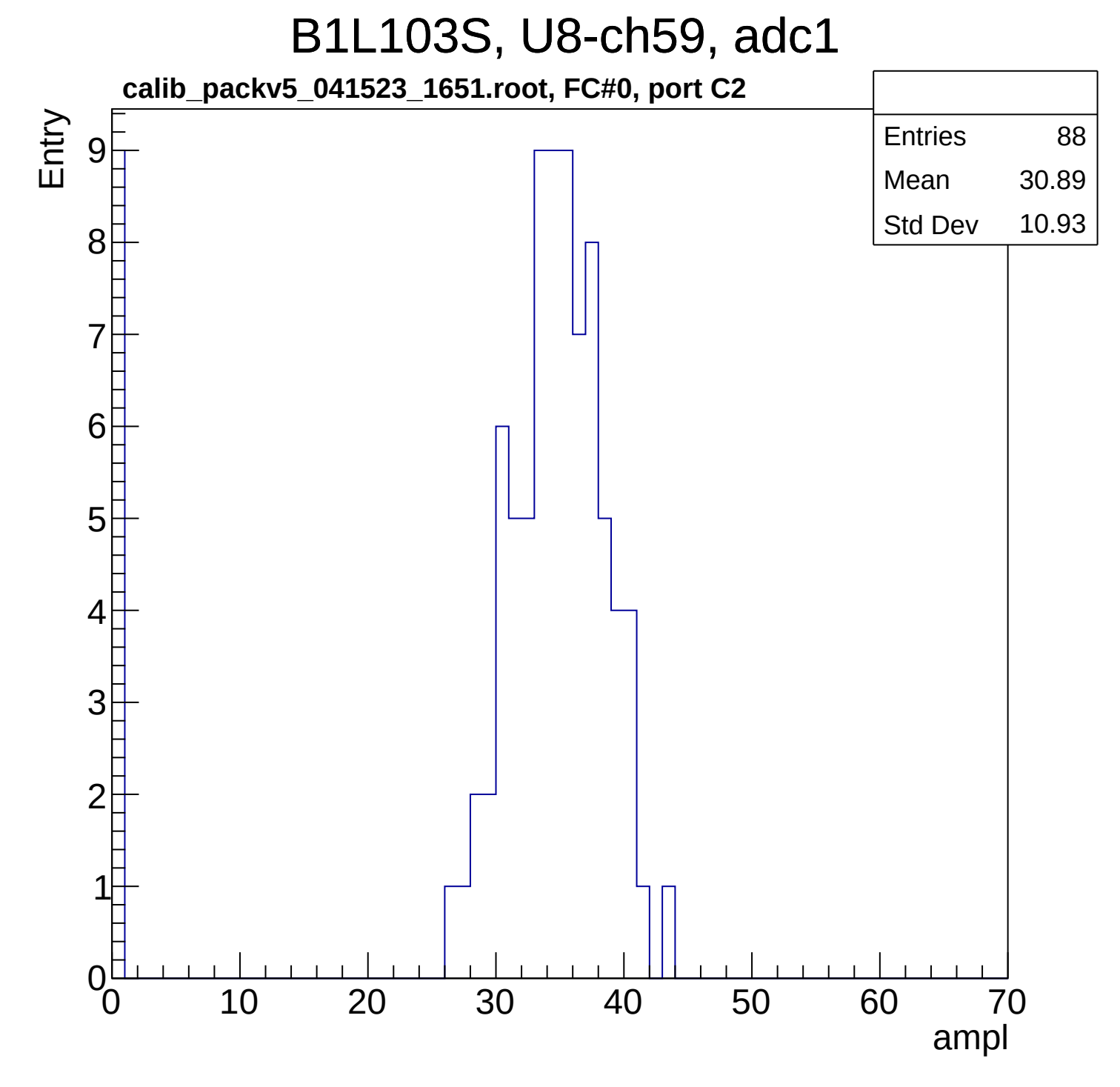
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch59, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 22.63
Std Dev 11.69
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U8-ch59, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 30.89
Std Dev 10.93
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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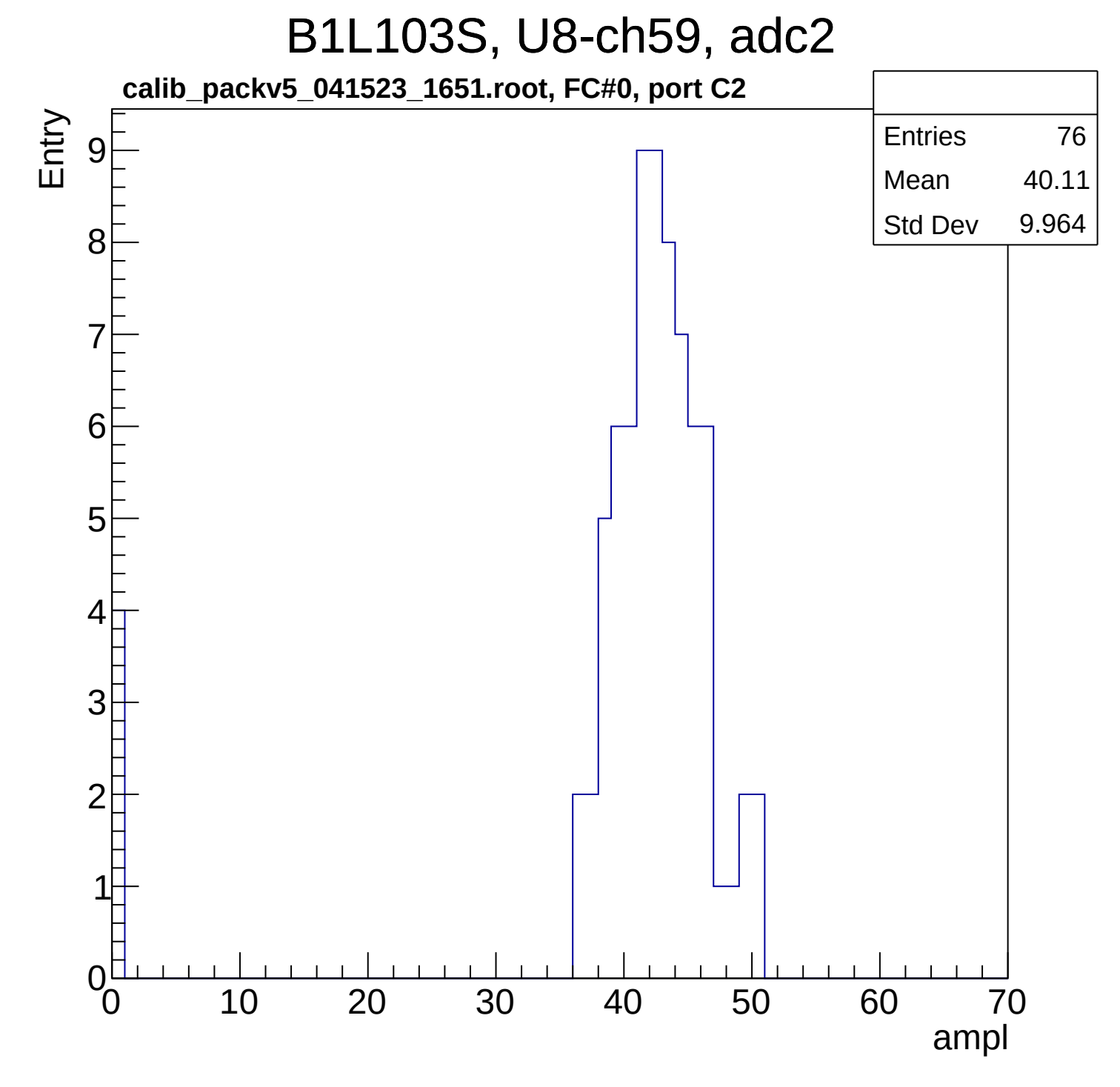
B1L103S, U8-ch59, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 40.11
Std Dev 9.964
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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60
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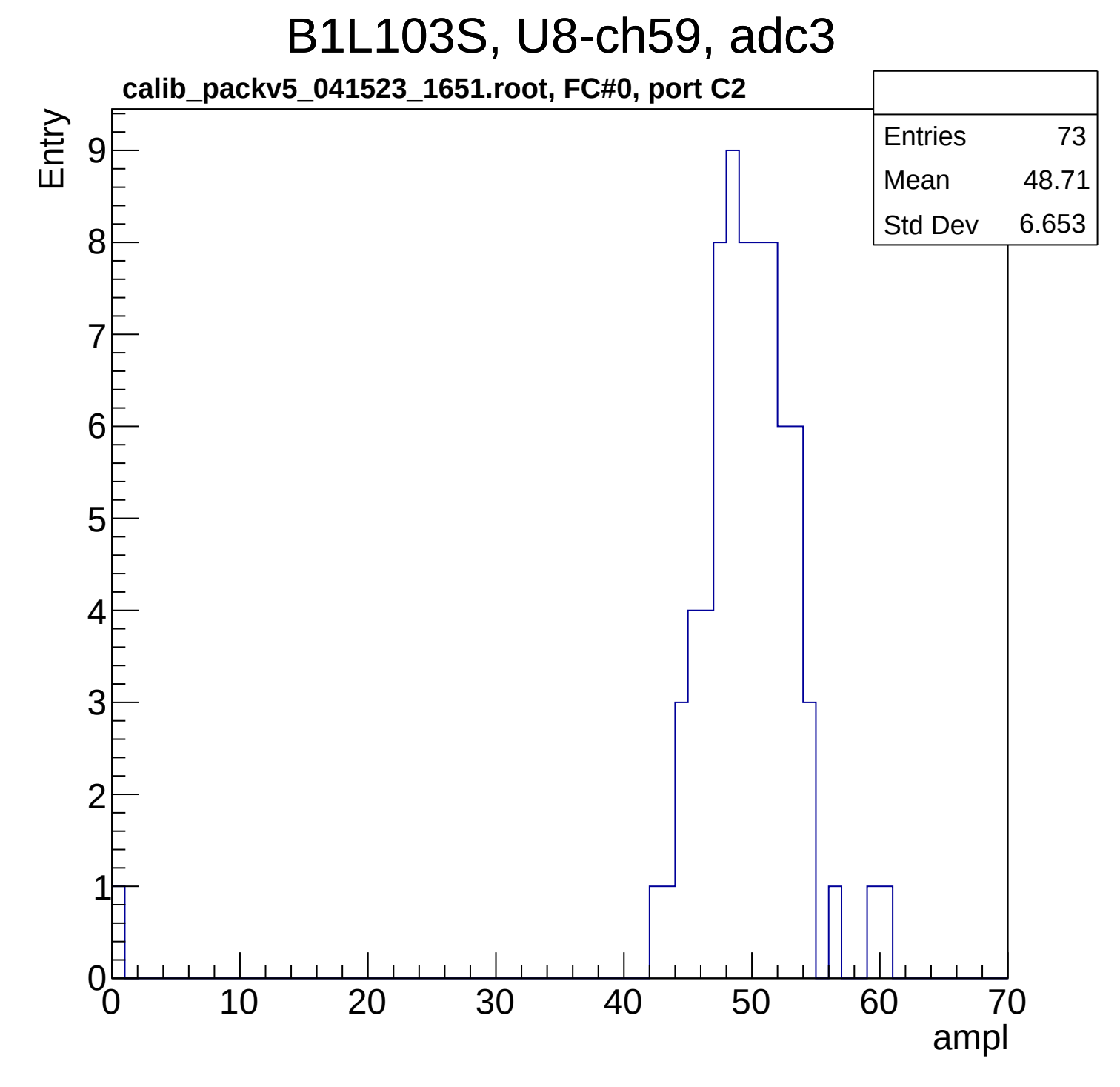
B1L103S, U8-ch59, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 48.71
Std Dev 6.653
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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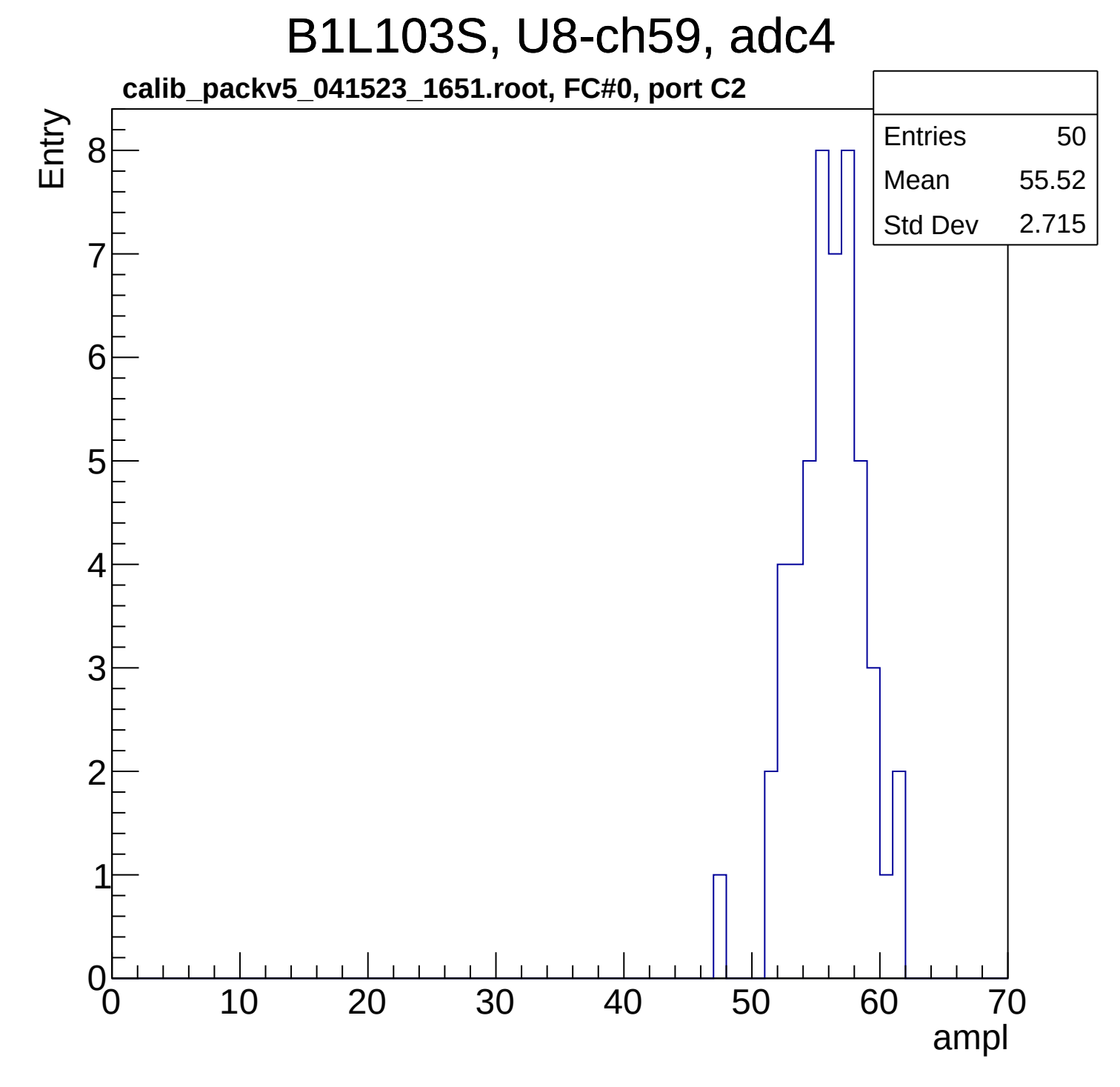
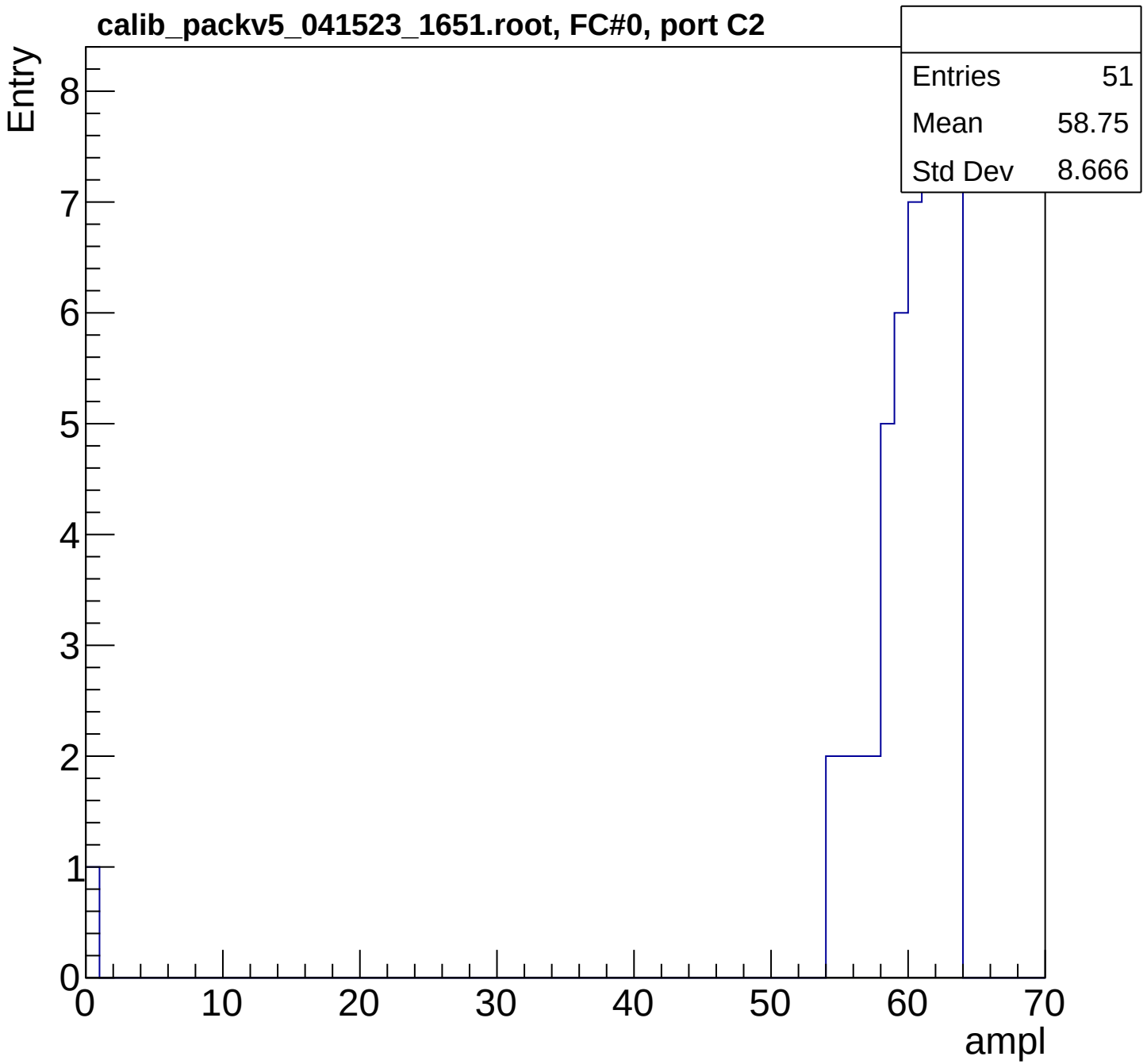
60
70


B1L103S, U8-ch59, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 55.52
Std Dev 2.715
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch59, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 58.75
Std Dev 8.666
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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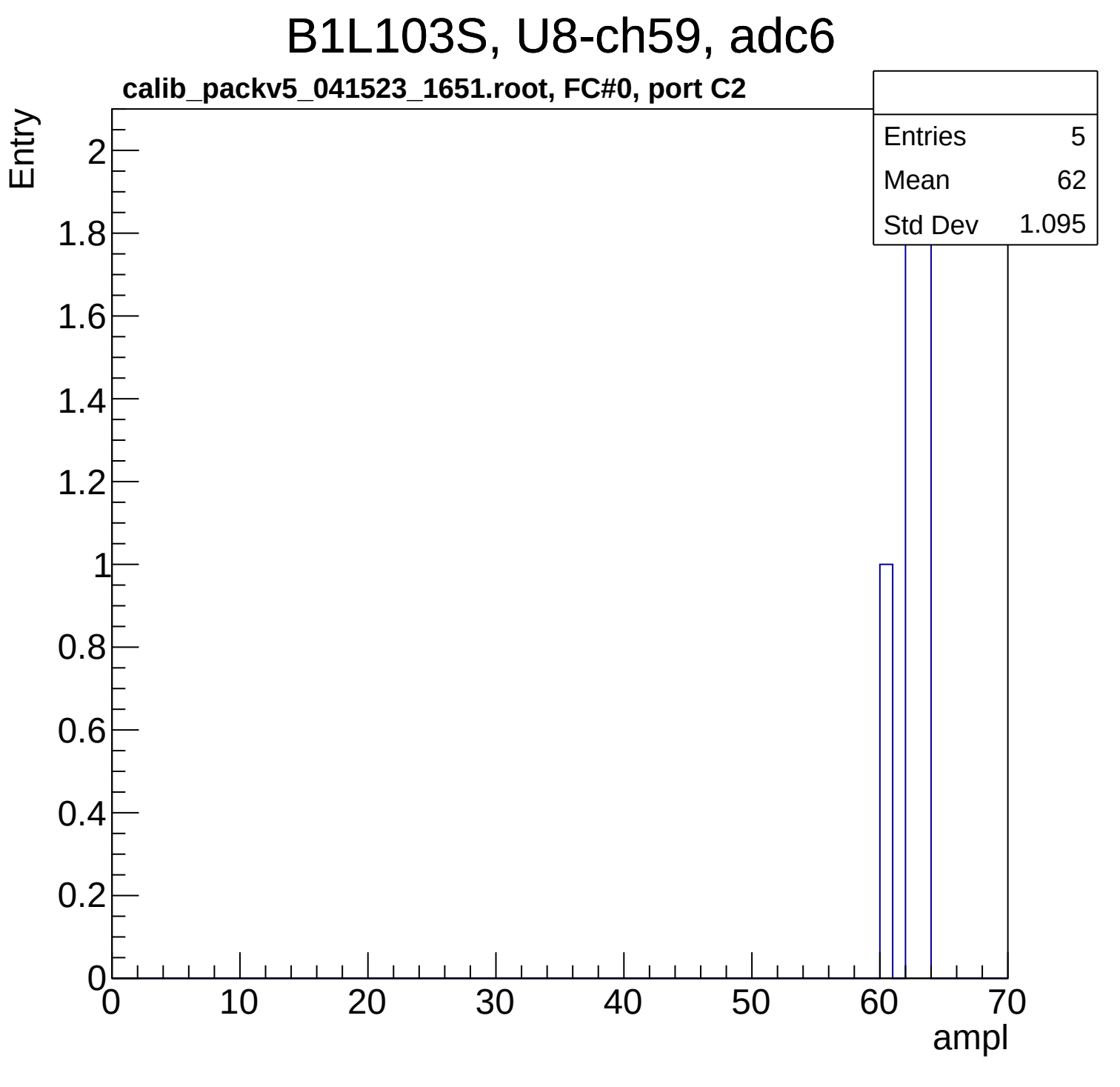
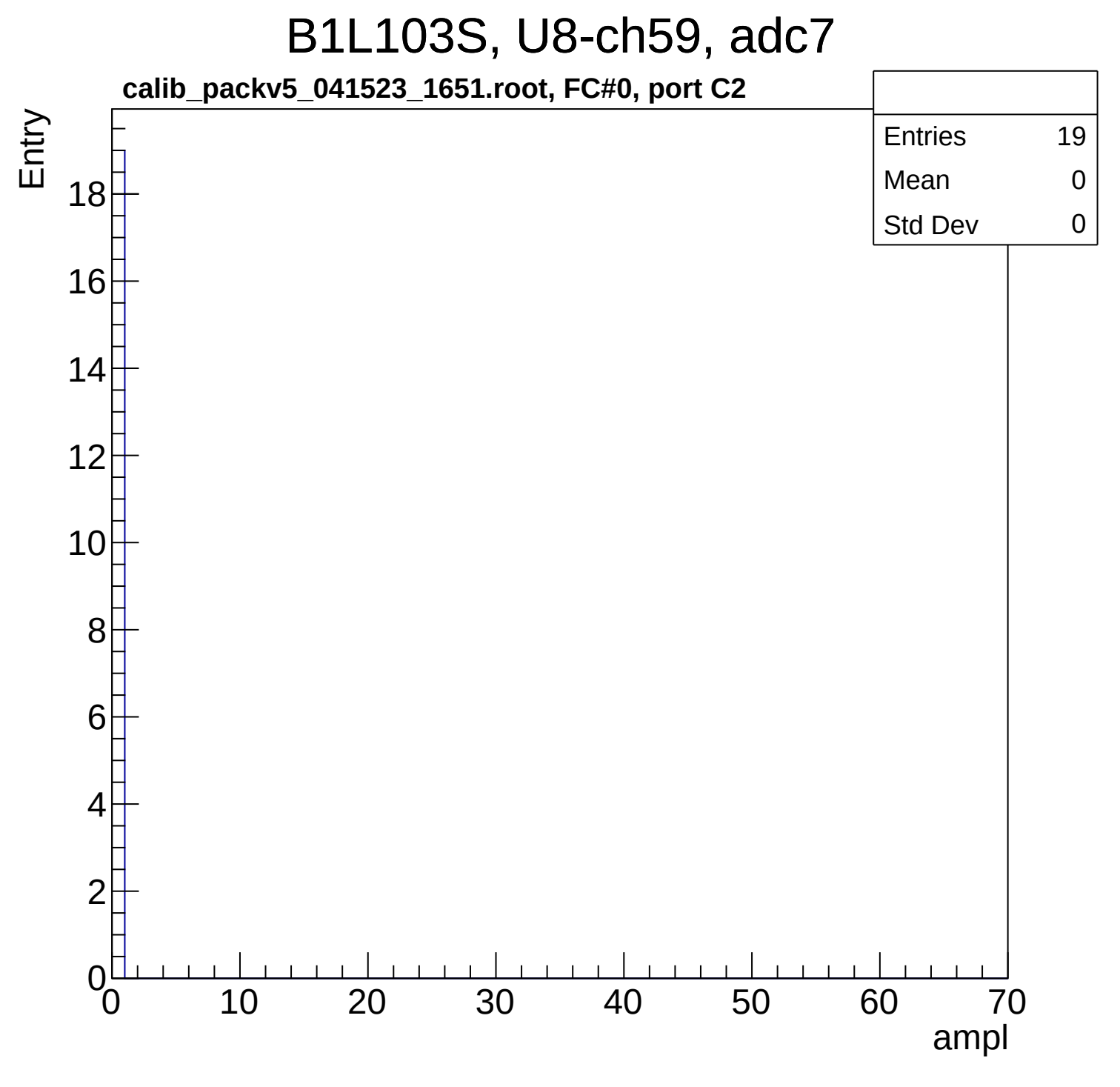
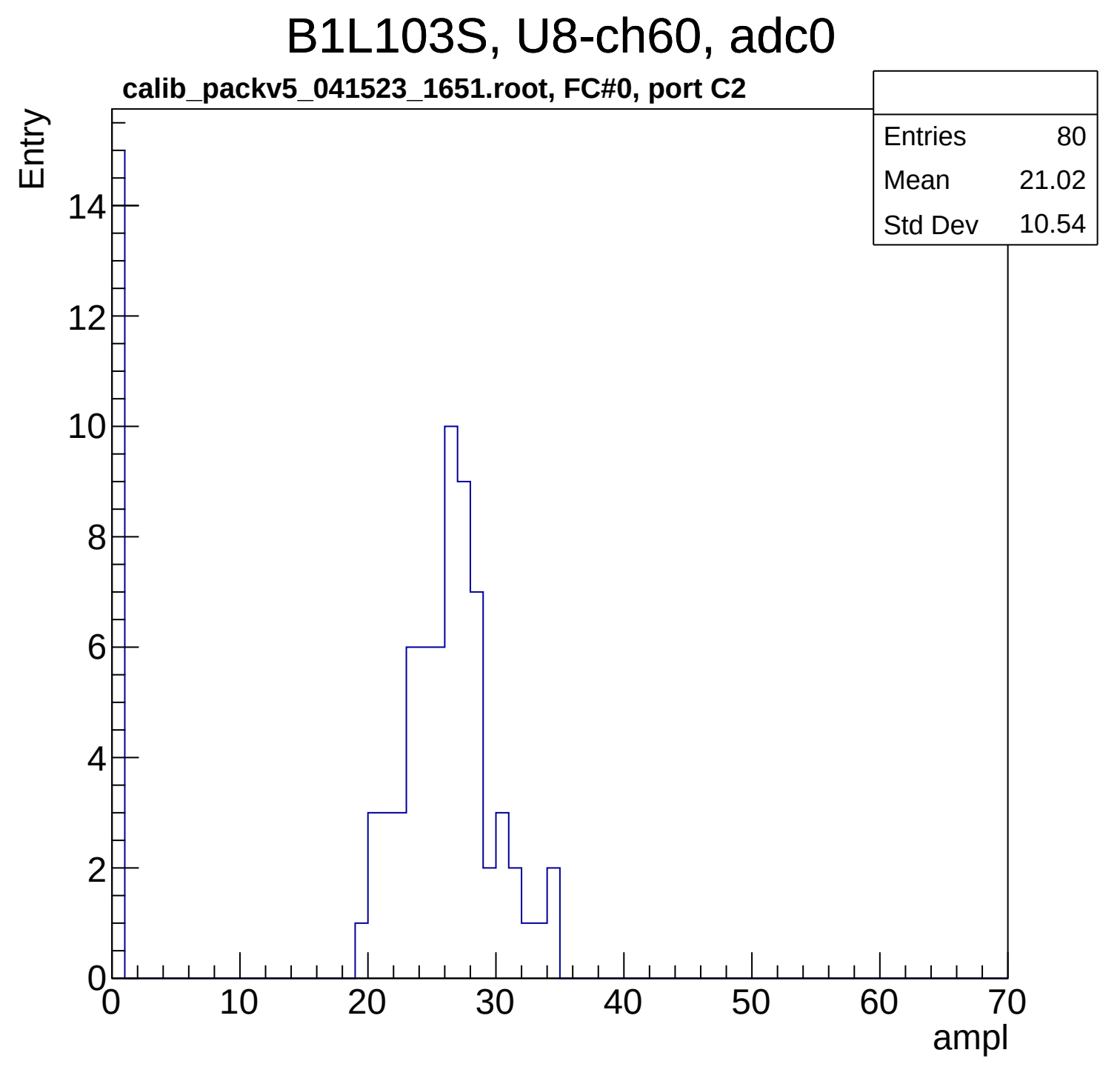

B1L103S, U8-ch59, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 62
Std Dev 1.095
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U8-ch59, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch60, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 21.02
Std Dev 10.54
Entry
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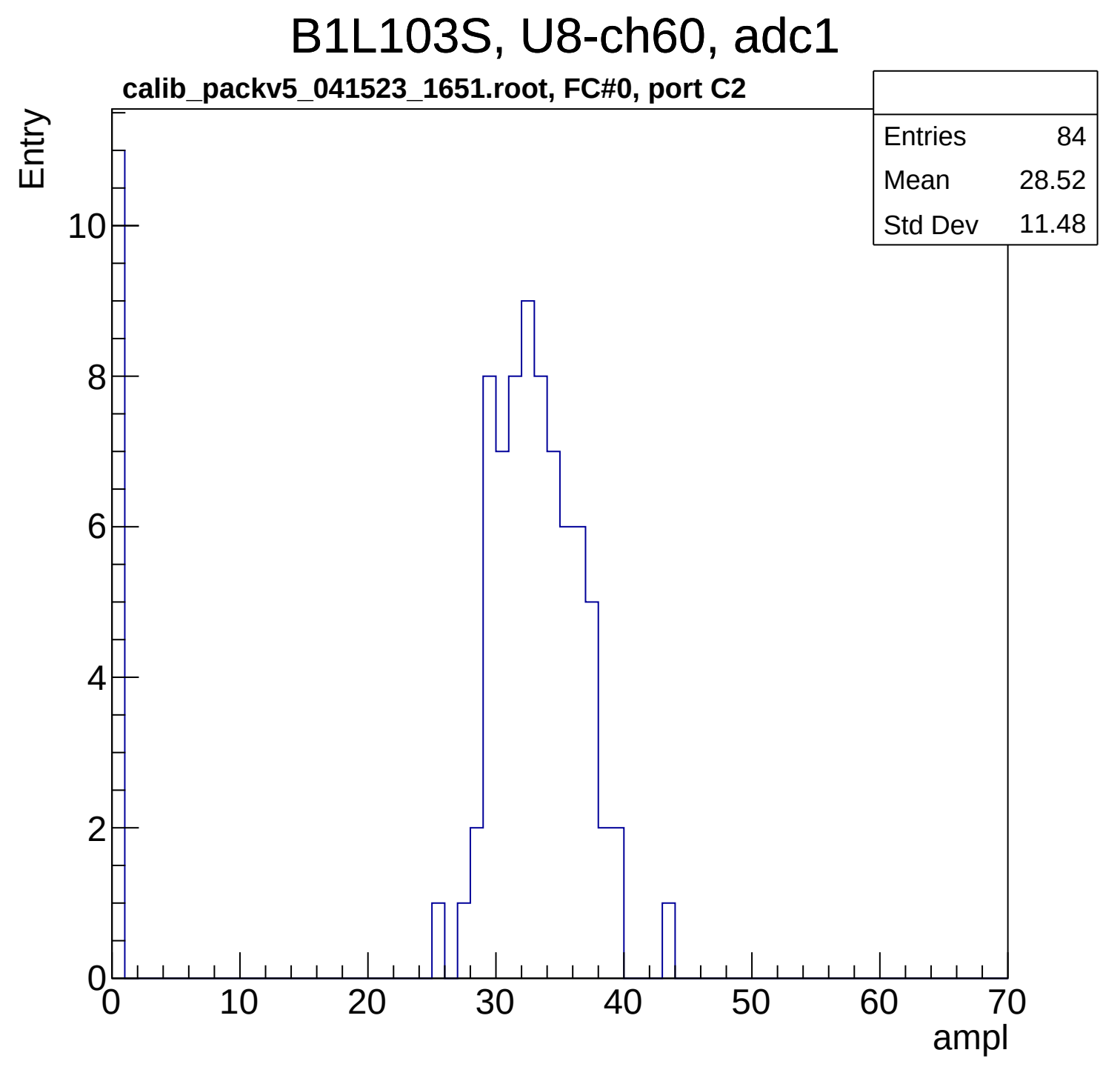
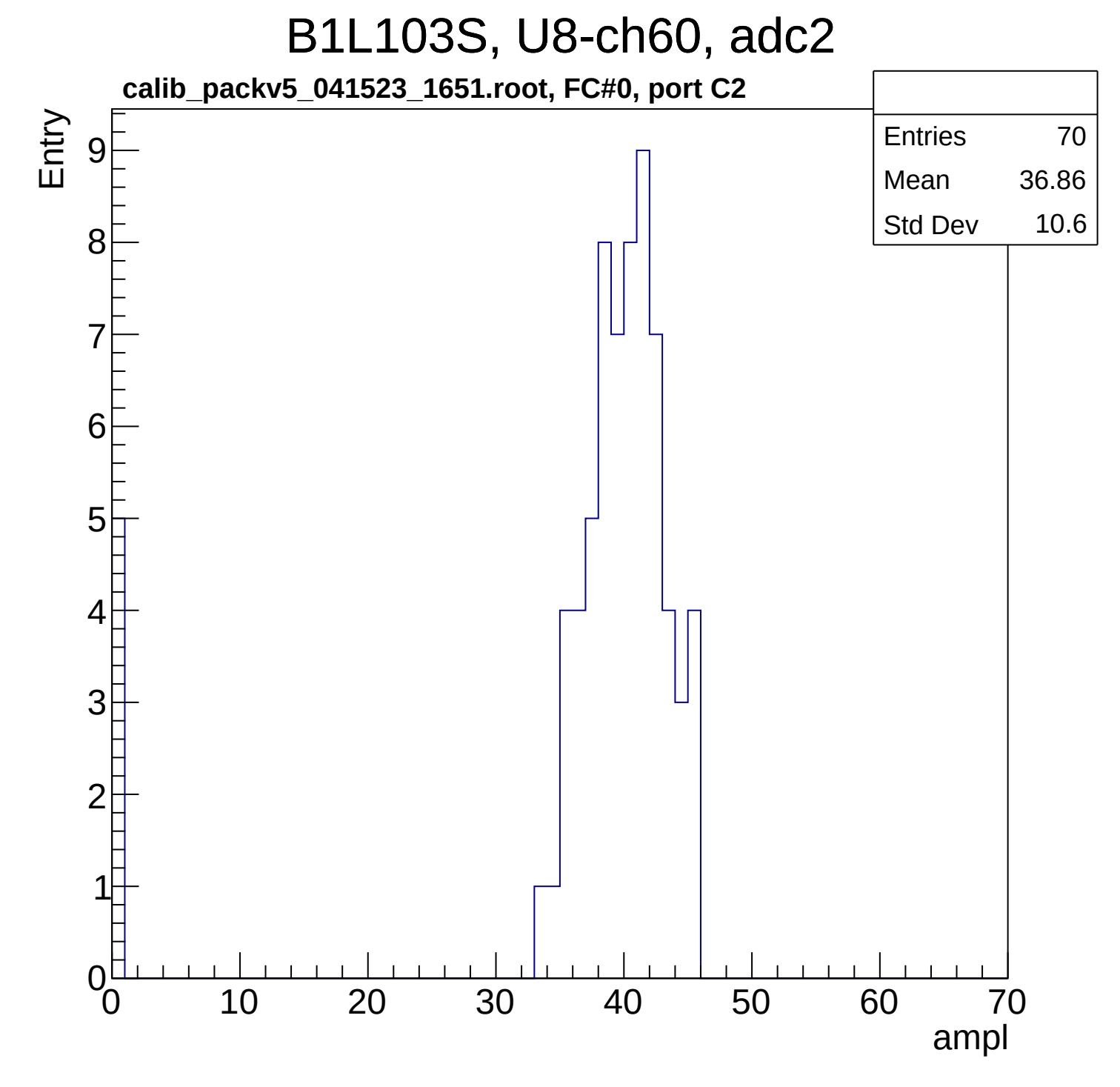
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch60, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 28.52
Std Dev 11.48
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch60, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 36.86
Std Dev 10.6
Entry
ampl
0
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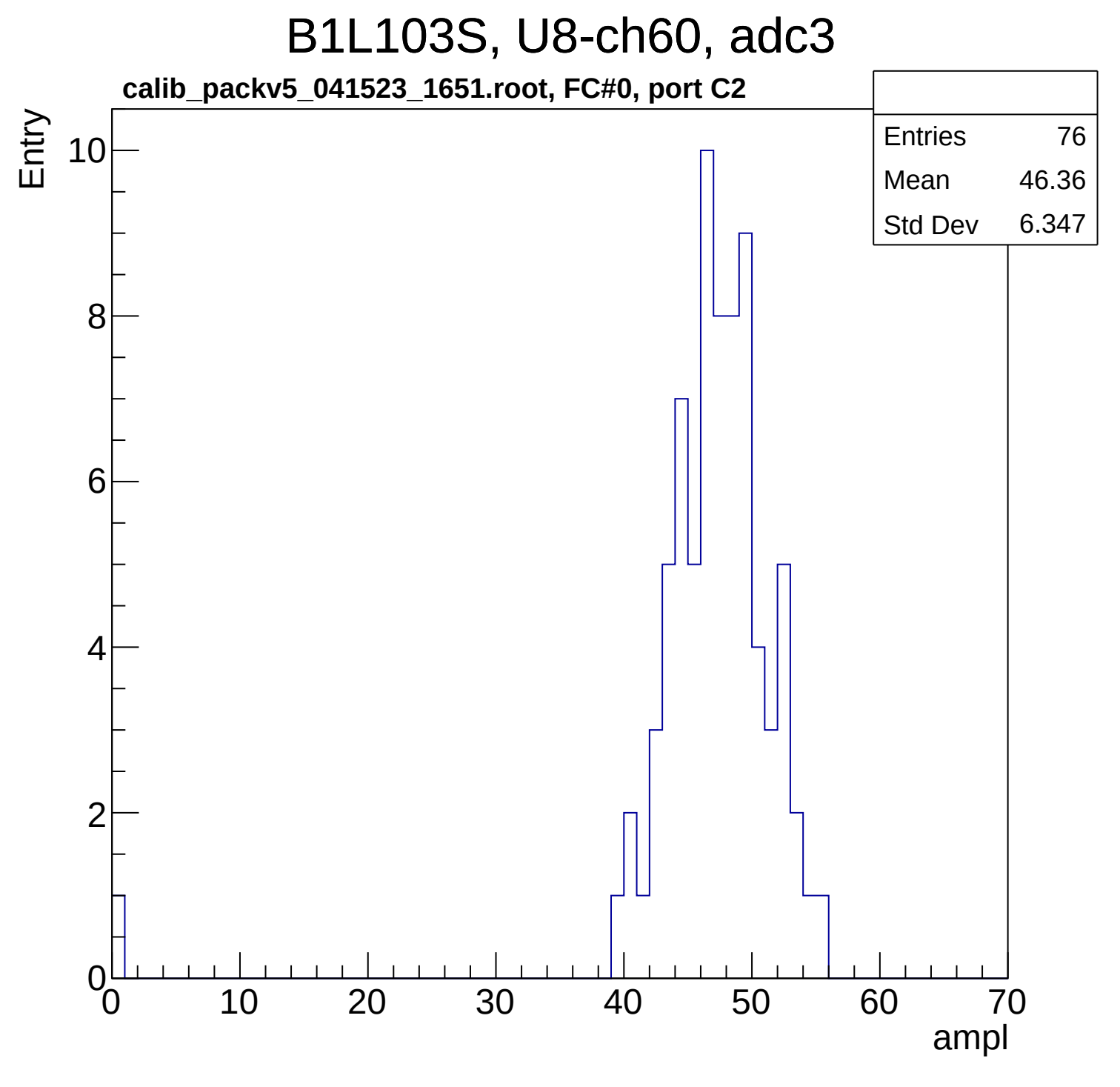
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U8-ch60, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 46.36
Std Dev 6.347
Entry
ampl
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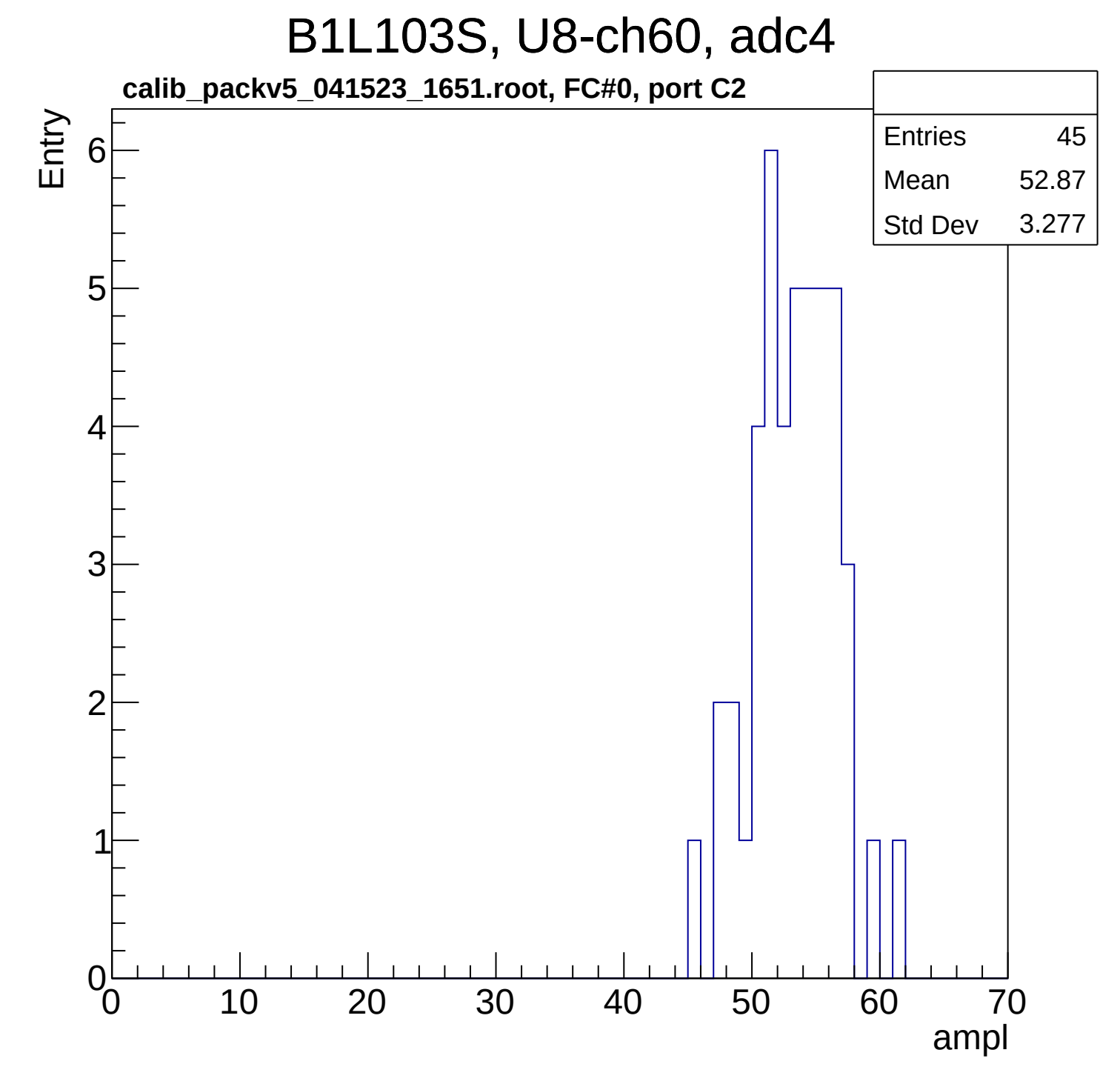
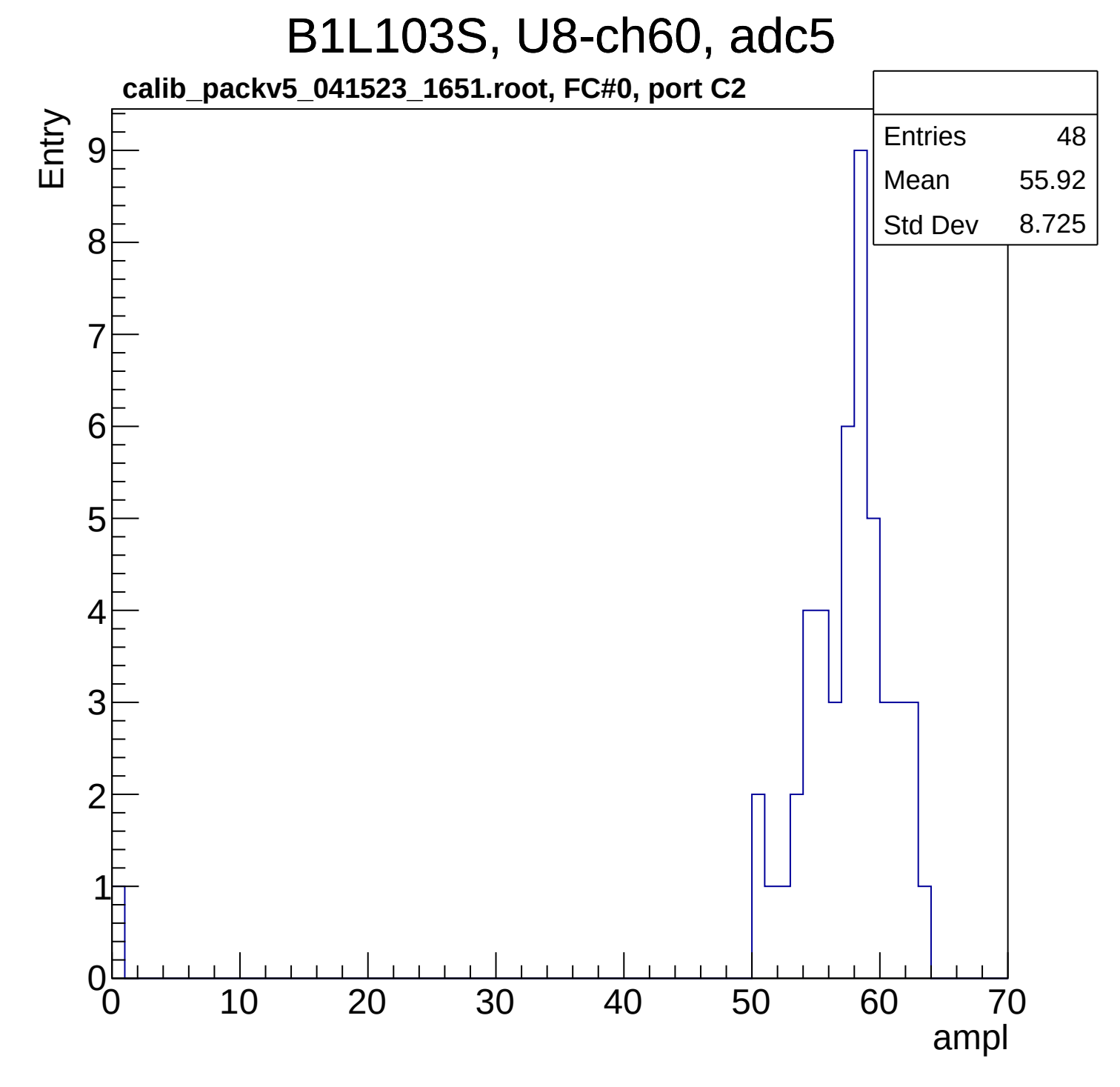
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U8-ch60, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 52.87
Std Dev 3.277
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U8-ch60, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 55.92
Std Dev 8.725
Entry
ampl
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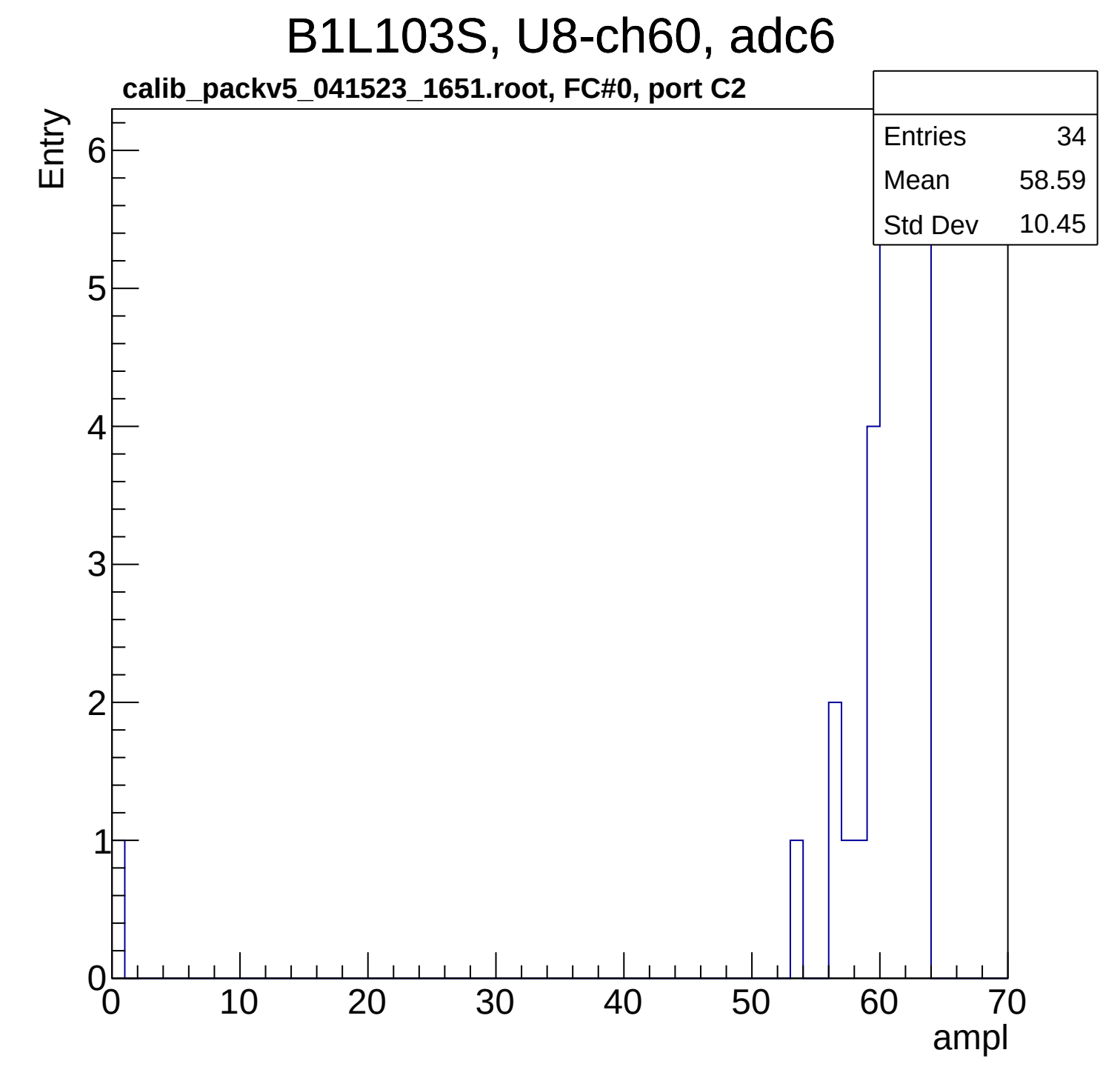
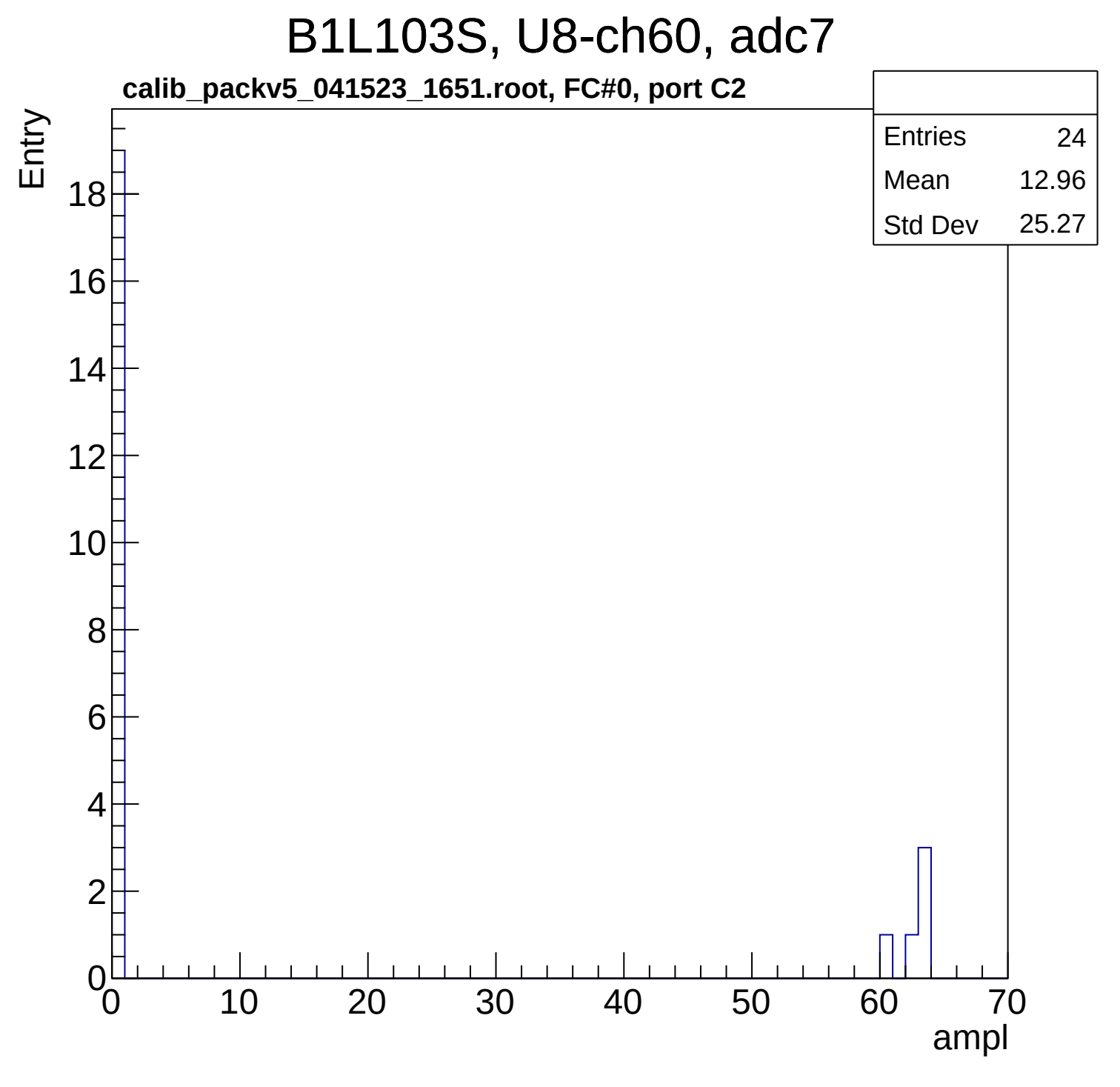
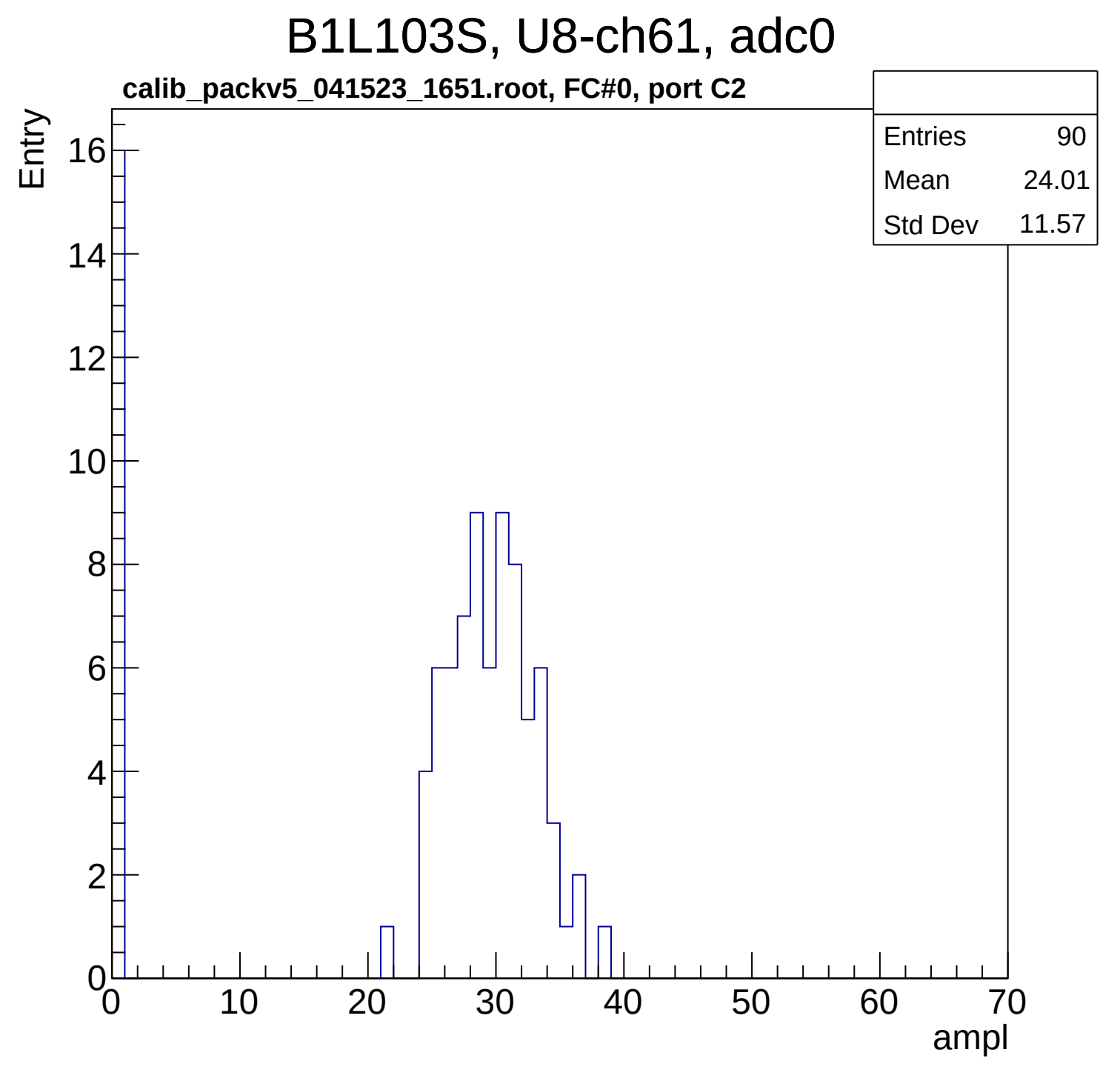
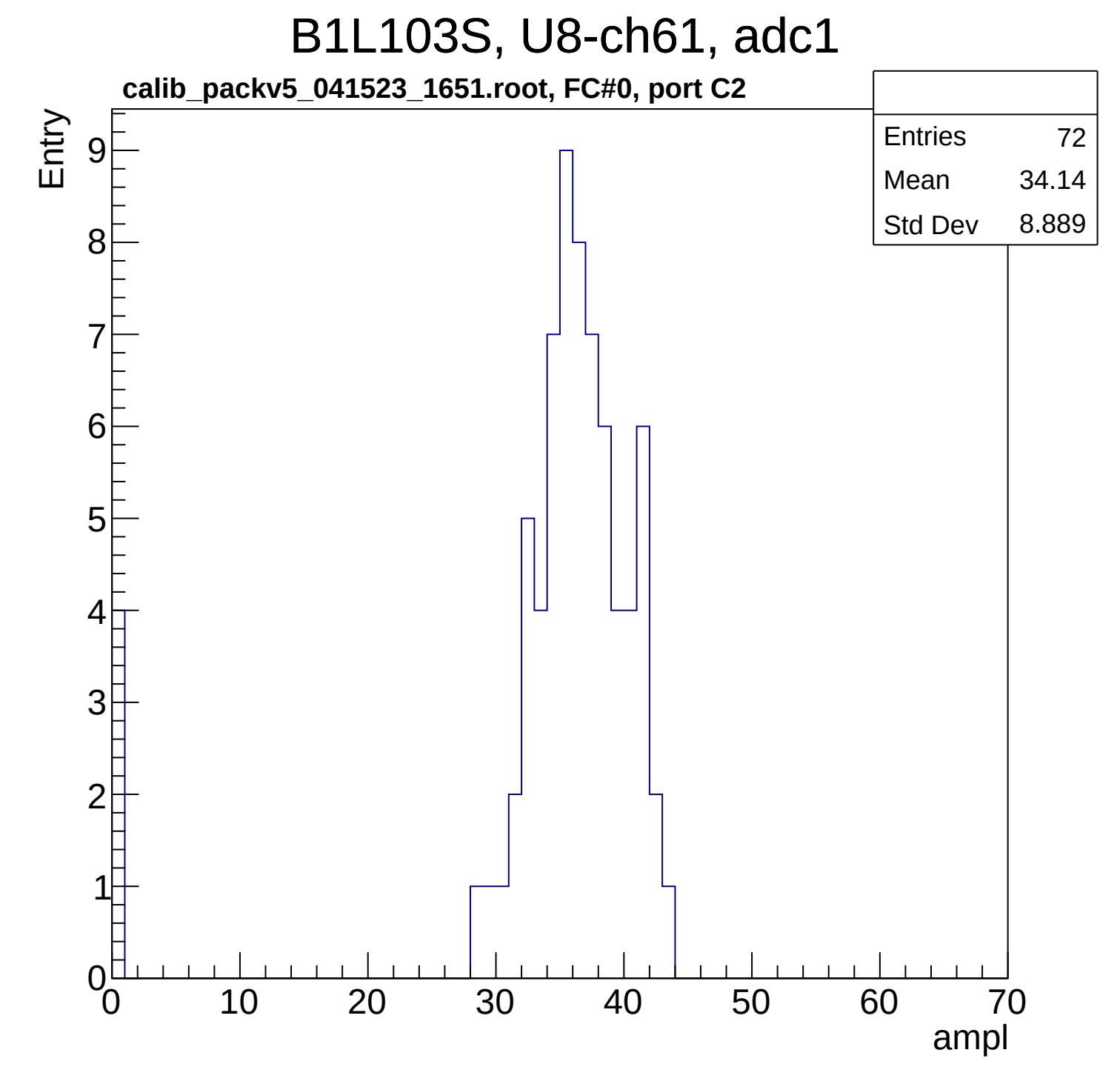
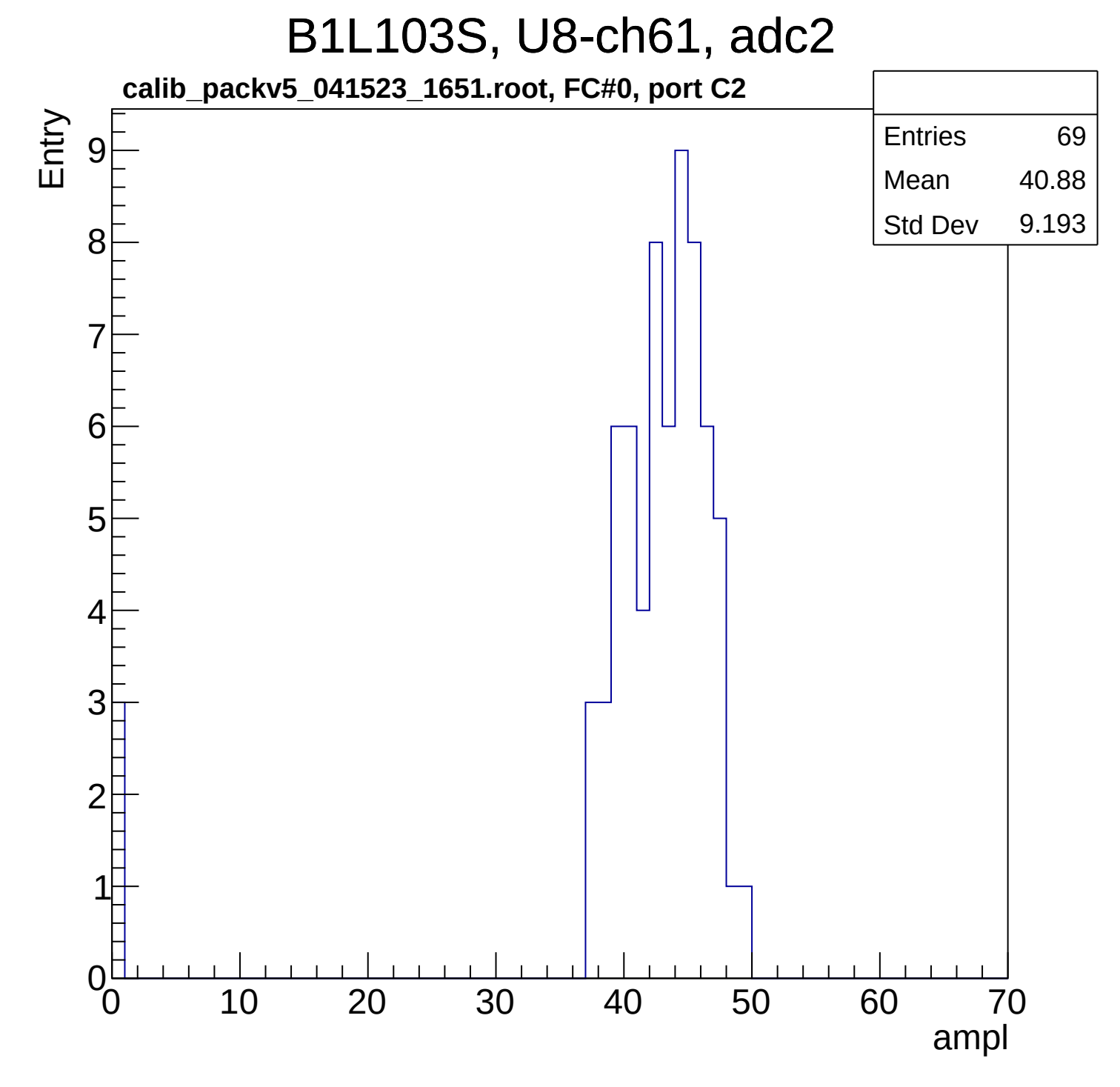
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U8-ch60, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 58.59
Std Dev 10.45
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U8-ch60, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 12.96
Std Dev 25.27
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch61, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 24.01
Std Dev 11.57
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L103S, U8-ch61, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 34.14
Std Dev 8.889
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U8-ch61, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 40.88
Std Dev 9.193
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
30
40
50
60
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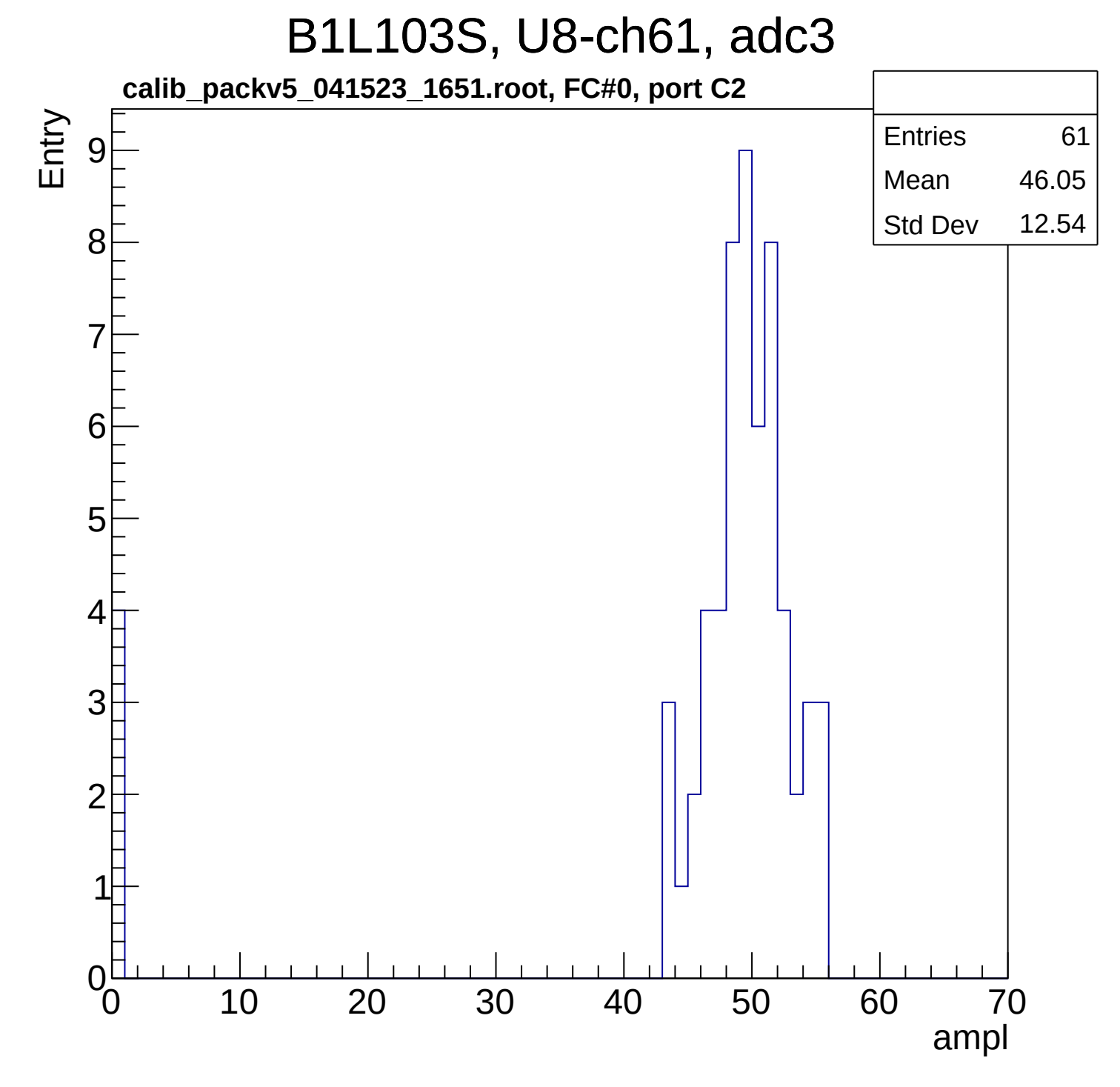
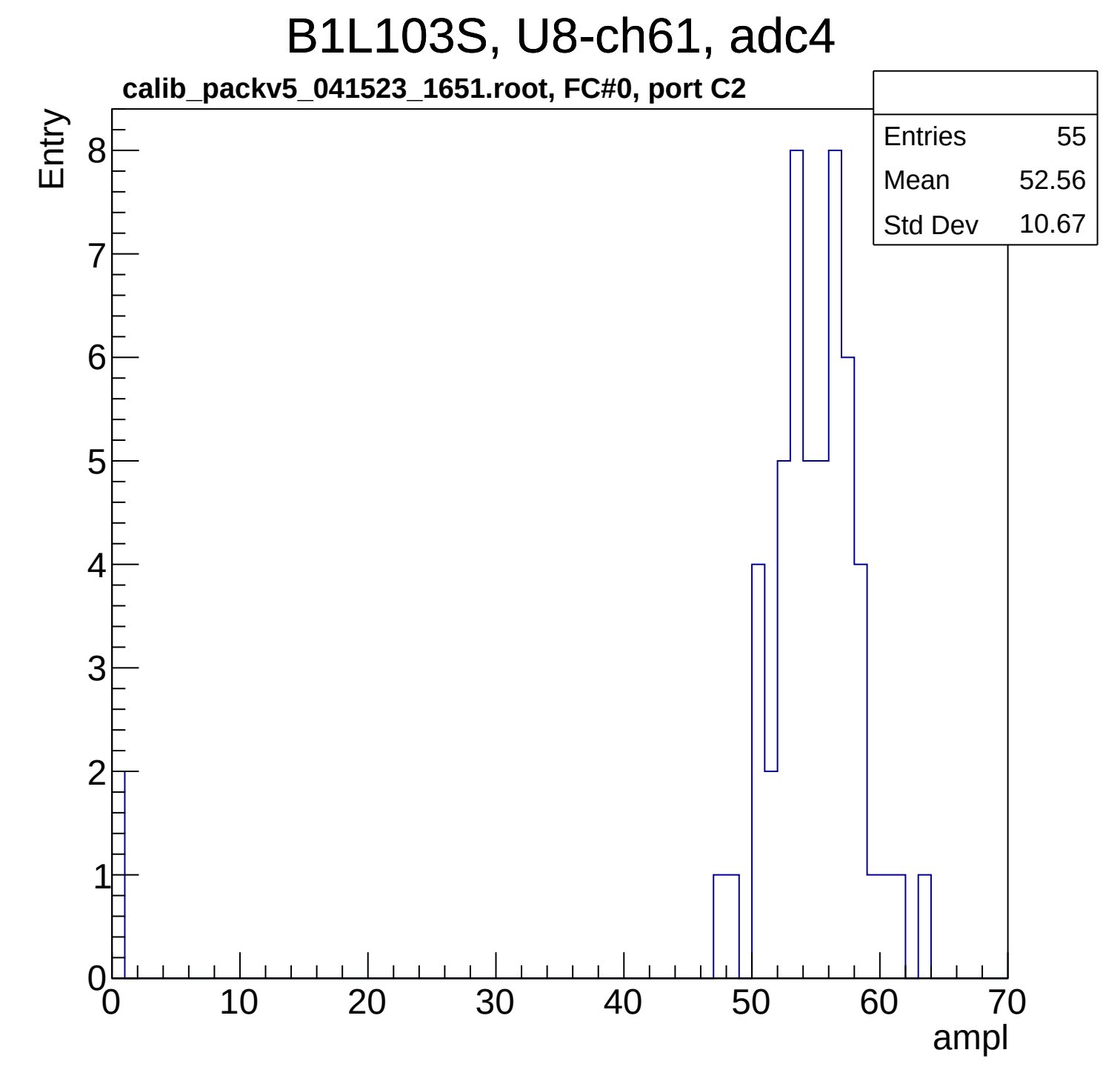

B1L103S, U8-ch61, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 46.05
Std Dev 12.54
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U8-ch61, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 52.56
Std Dev 10.67
Entry
ampl
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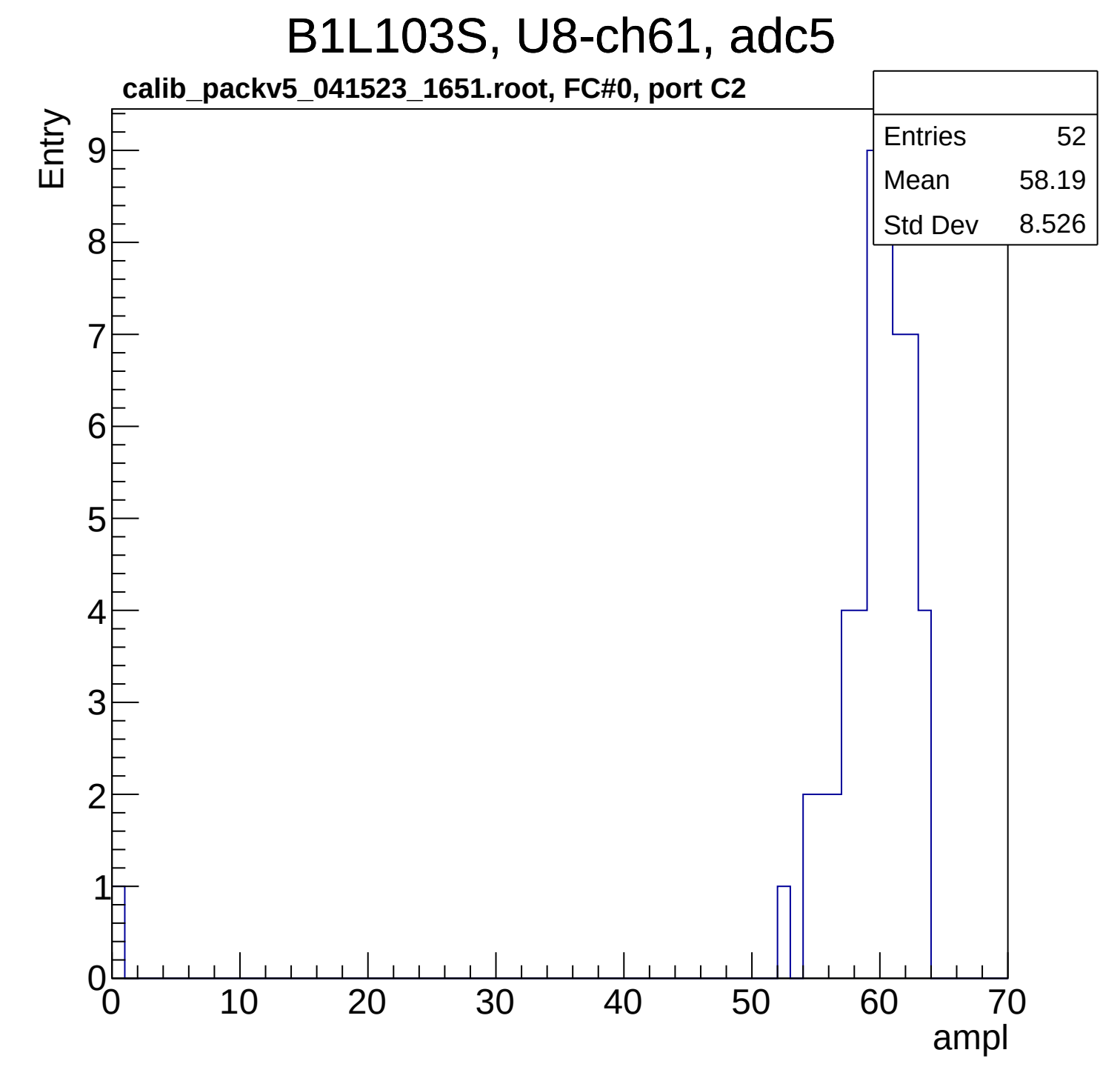
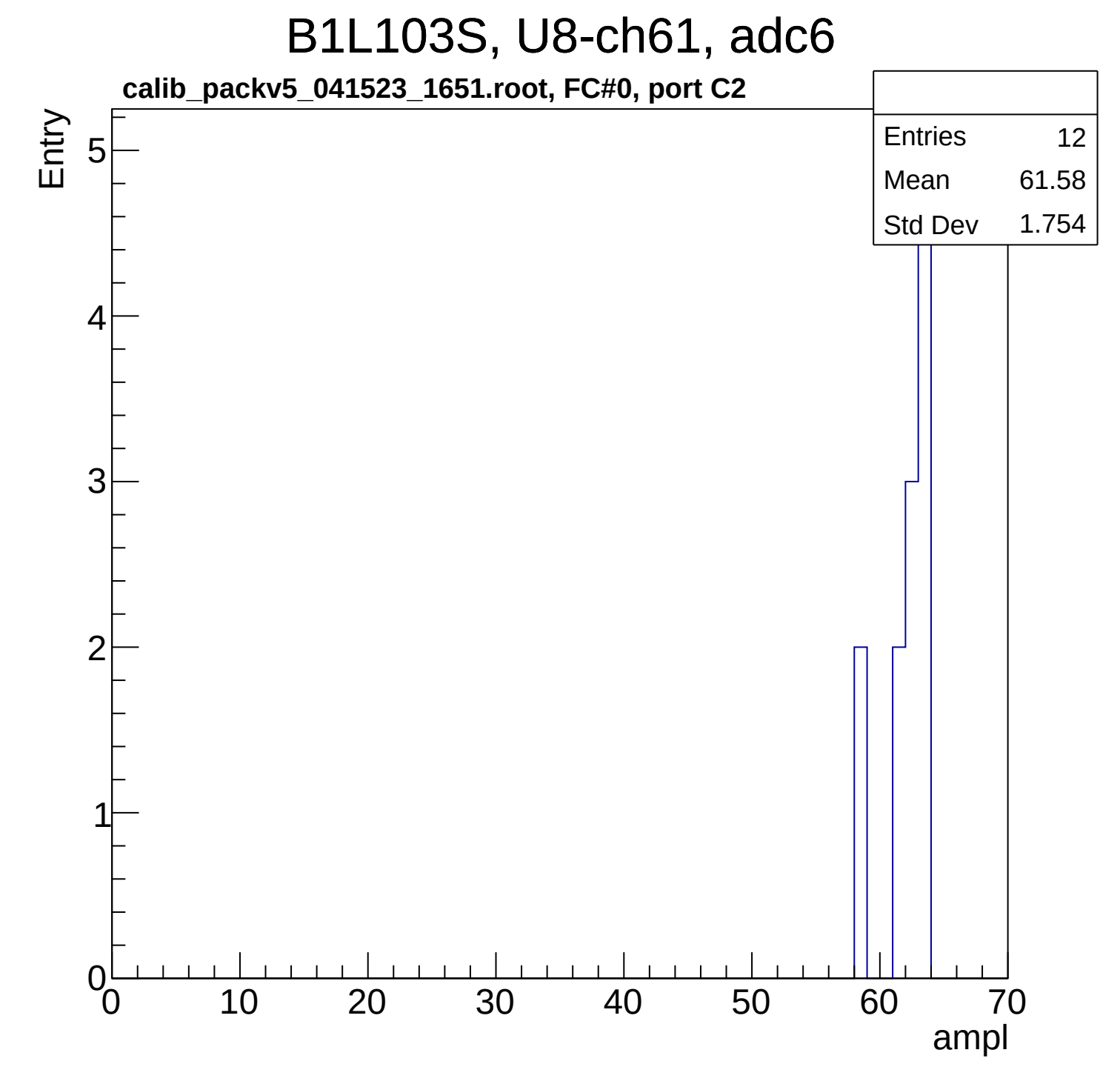
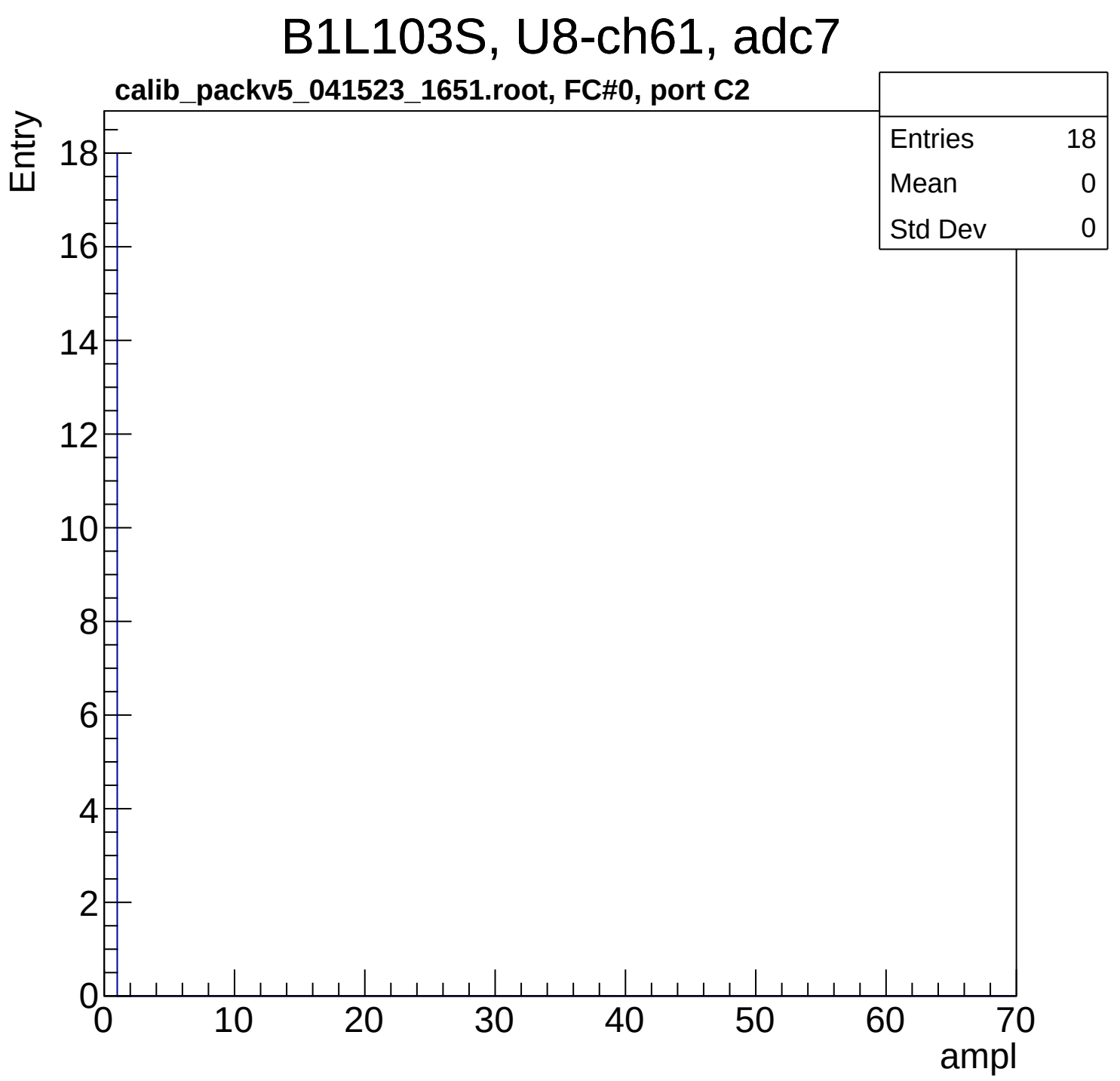
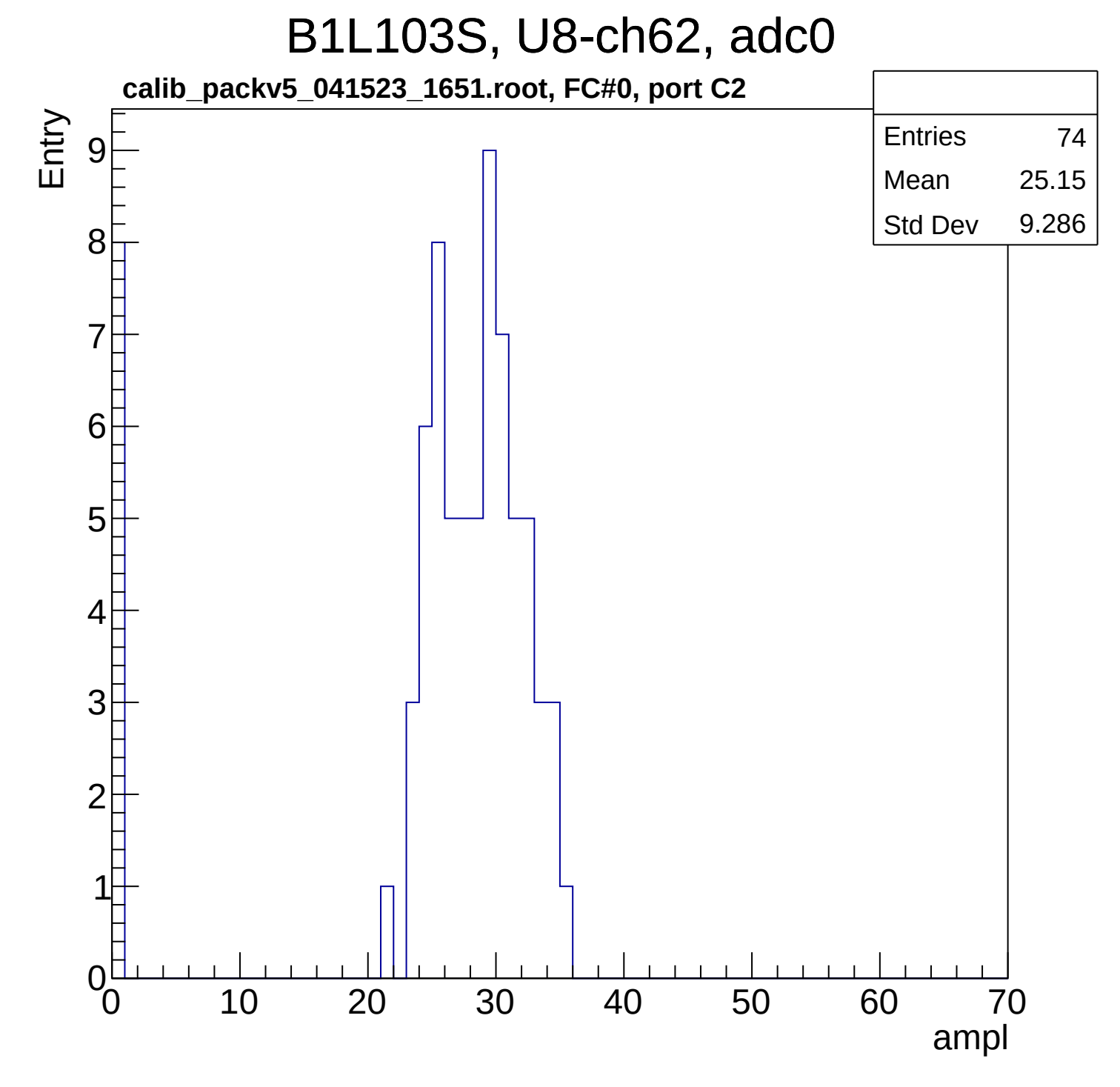
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch61, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 58.19
Std Dev 8.526
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U8-ch61, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.58
Std Dev 1.754
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U8-ch61, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch62, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 25.15
Std Dev 9.286
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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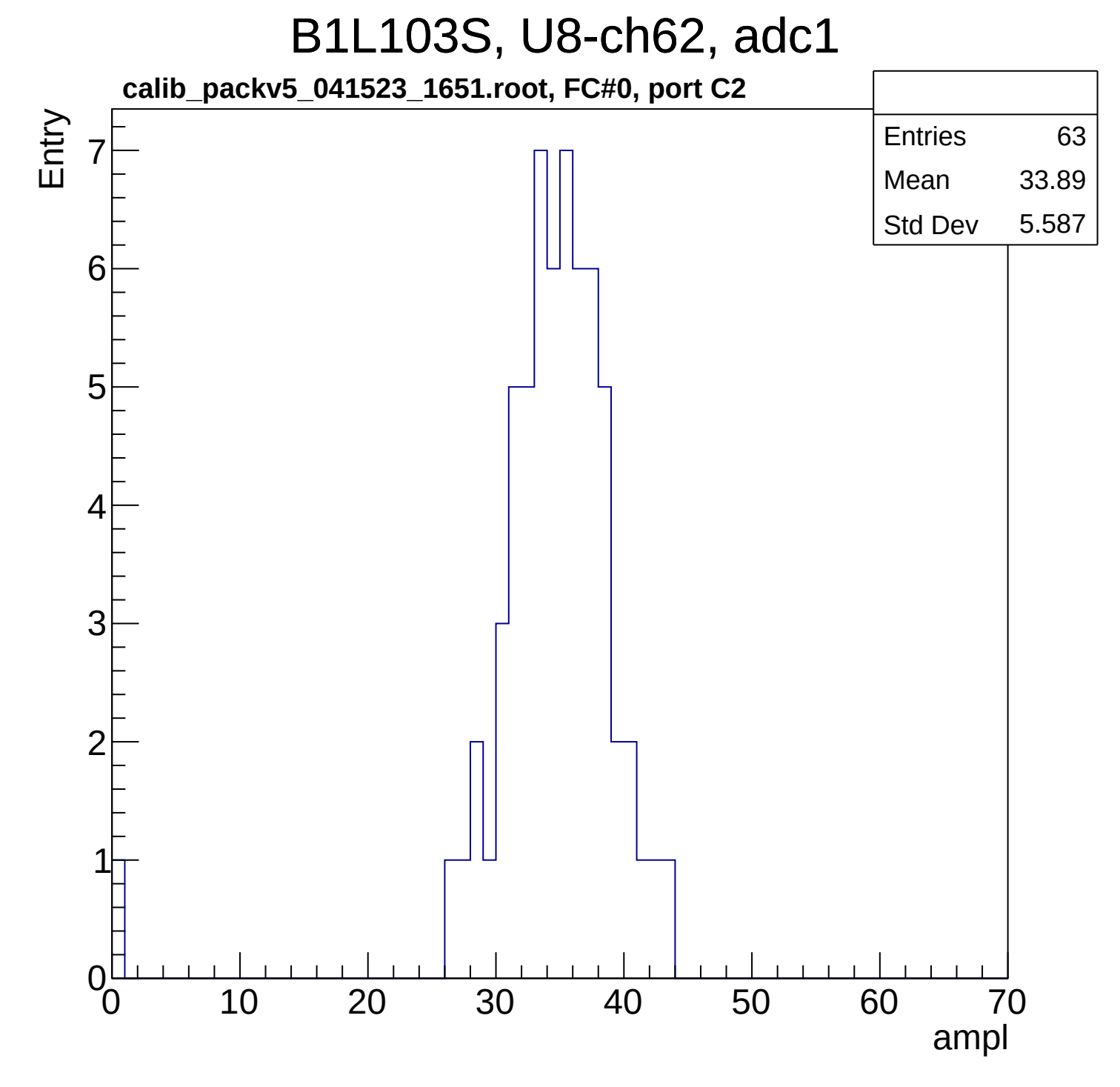
40
50
60
70


B1L103S, U8-ch62, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 33.89
Std Dev 5.587
Entry
ampl
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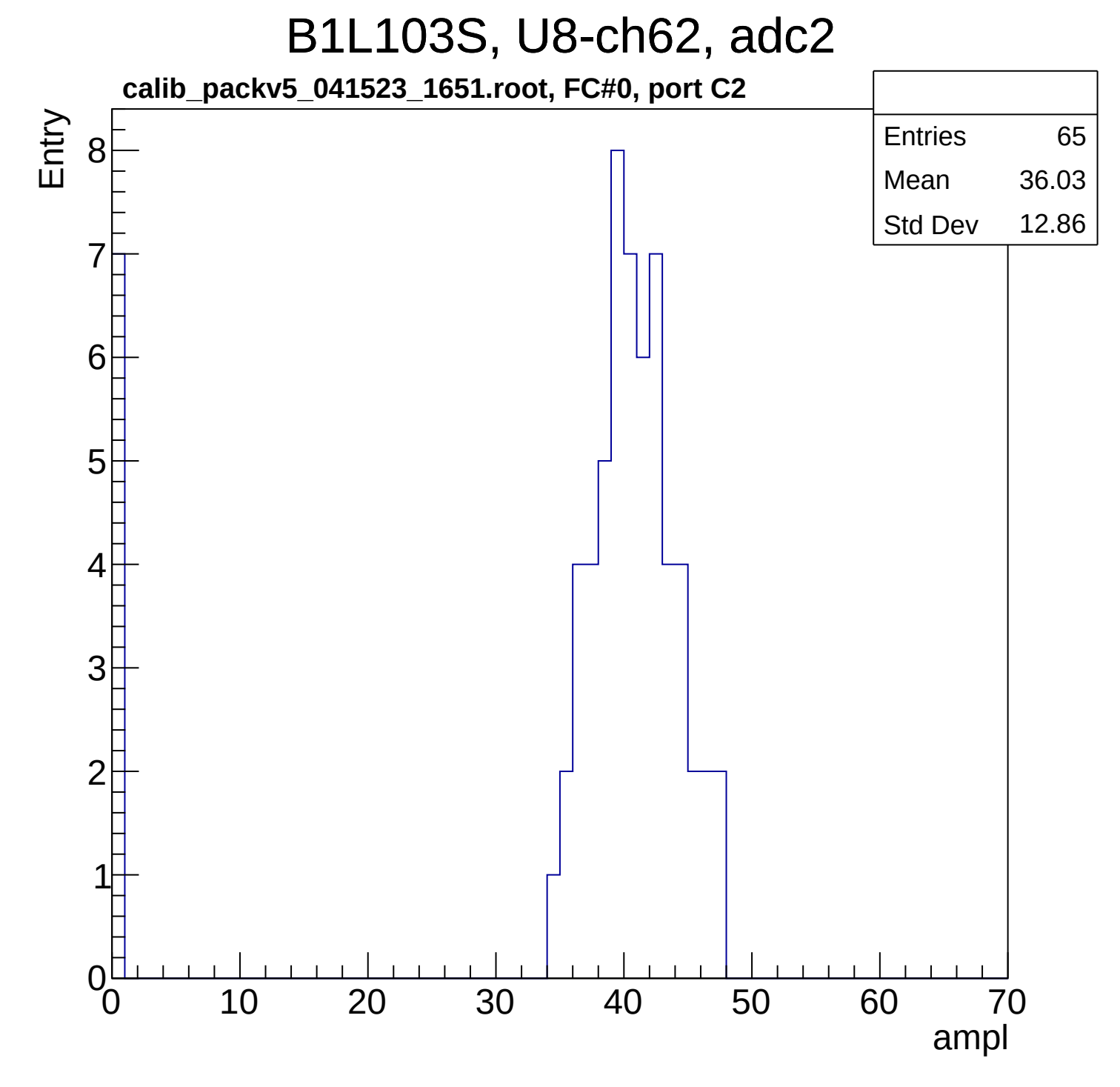
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U8-ch62, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 36.03
Std Dev 12.86
Entry
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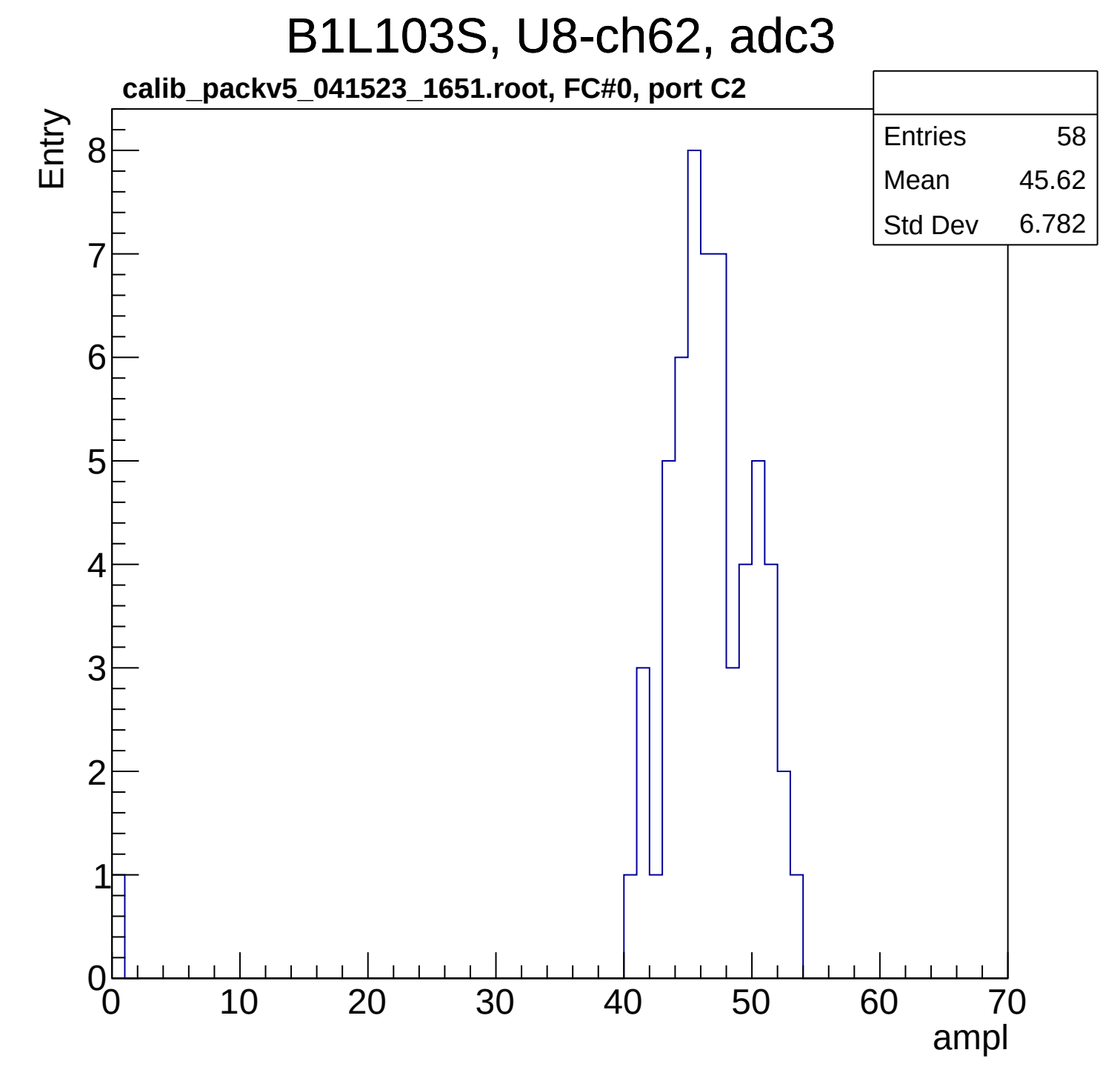
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch62, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 45.62
Std Dev 6.782
Entry
ampl
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1
2
3
4
5
6
7
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0
10
20
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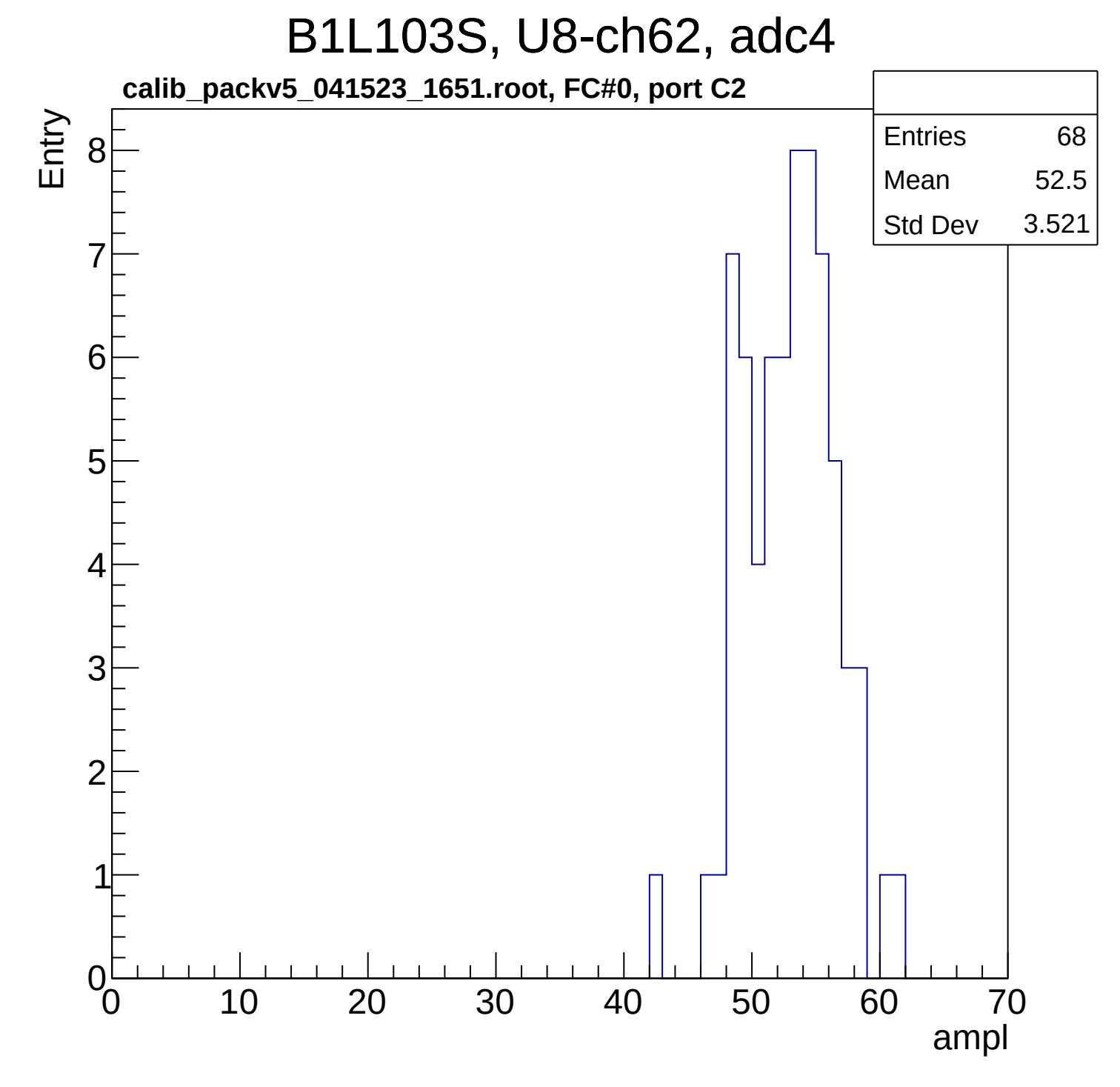
40
50
60
70


B1L103S, U8-ch62, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 52.5
Std Dev 3.521
Entry
ampl
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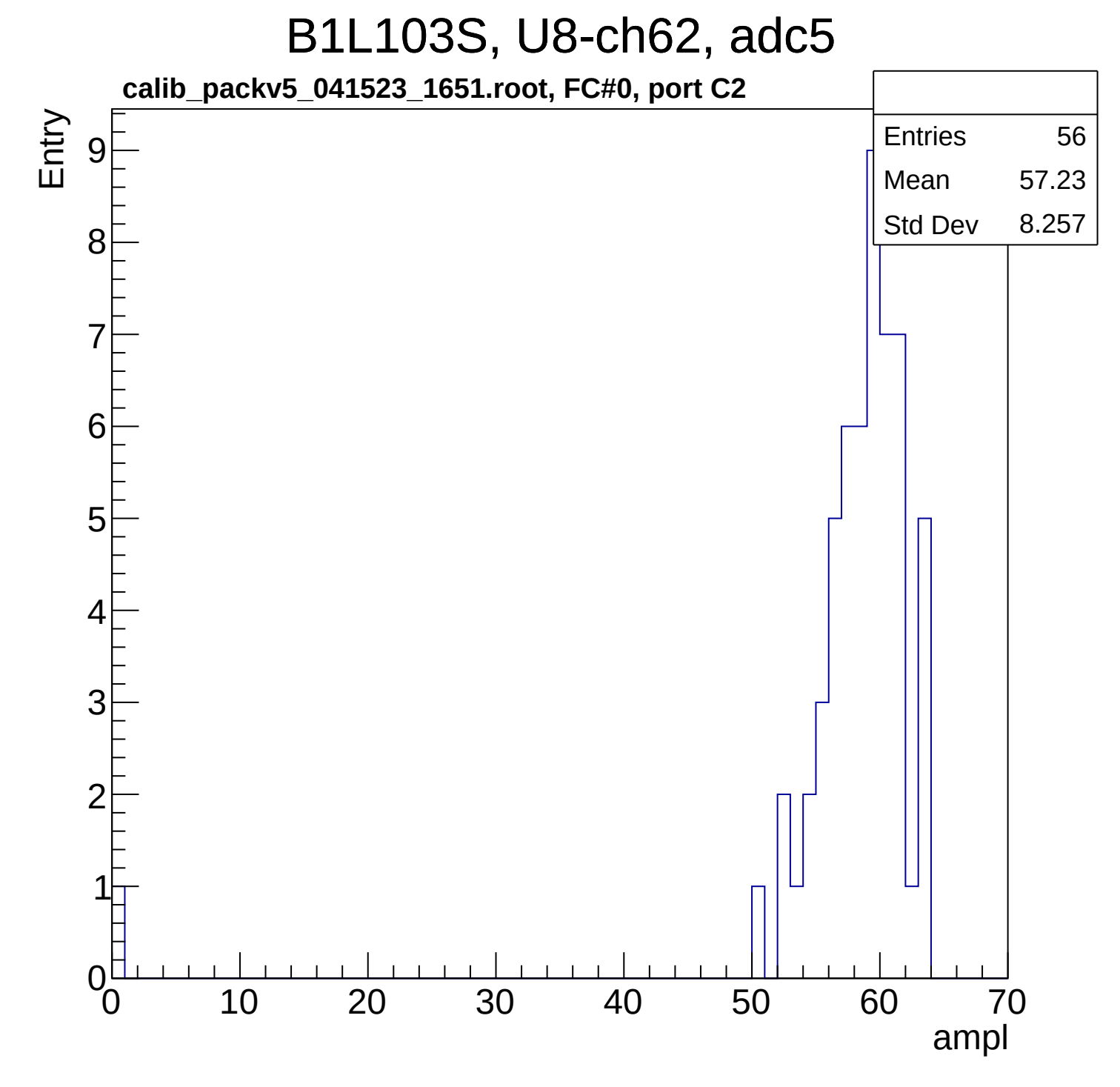
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch62, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 57.23
Std Dev 8.257
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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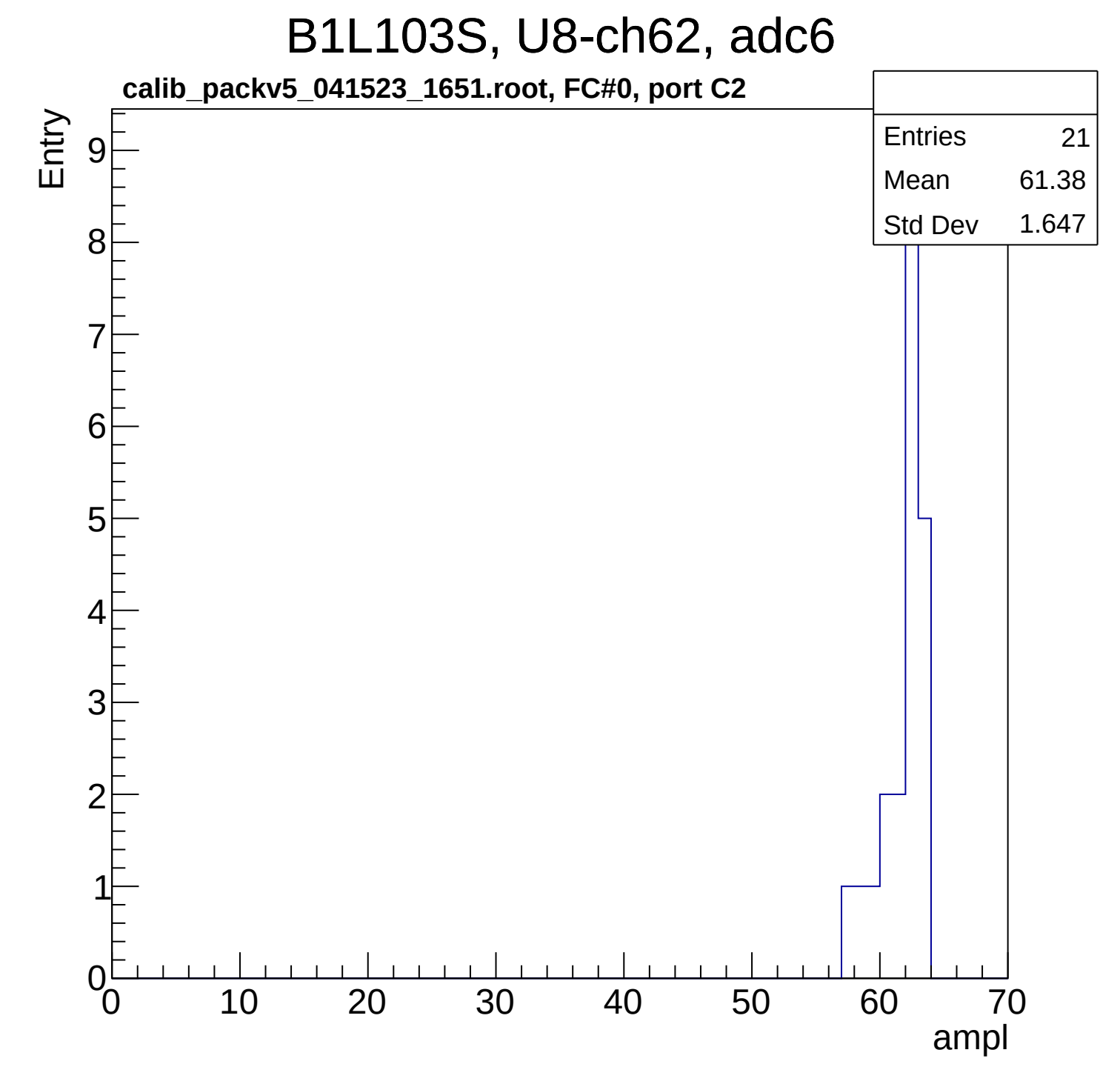
60
70


B1L103S, U8-ch62, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 61.38
Std Dev 1.647
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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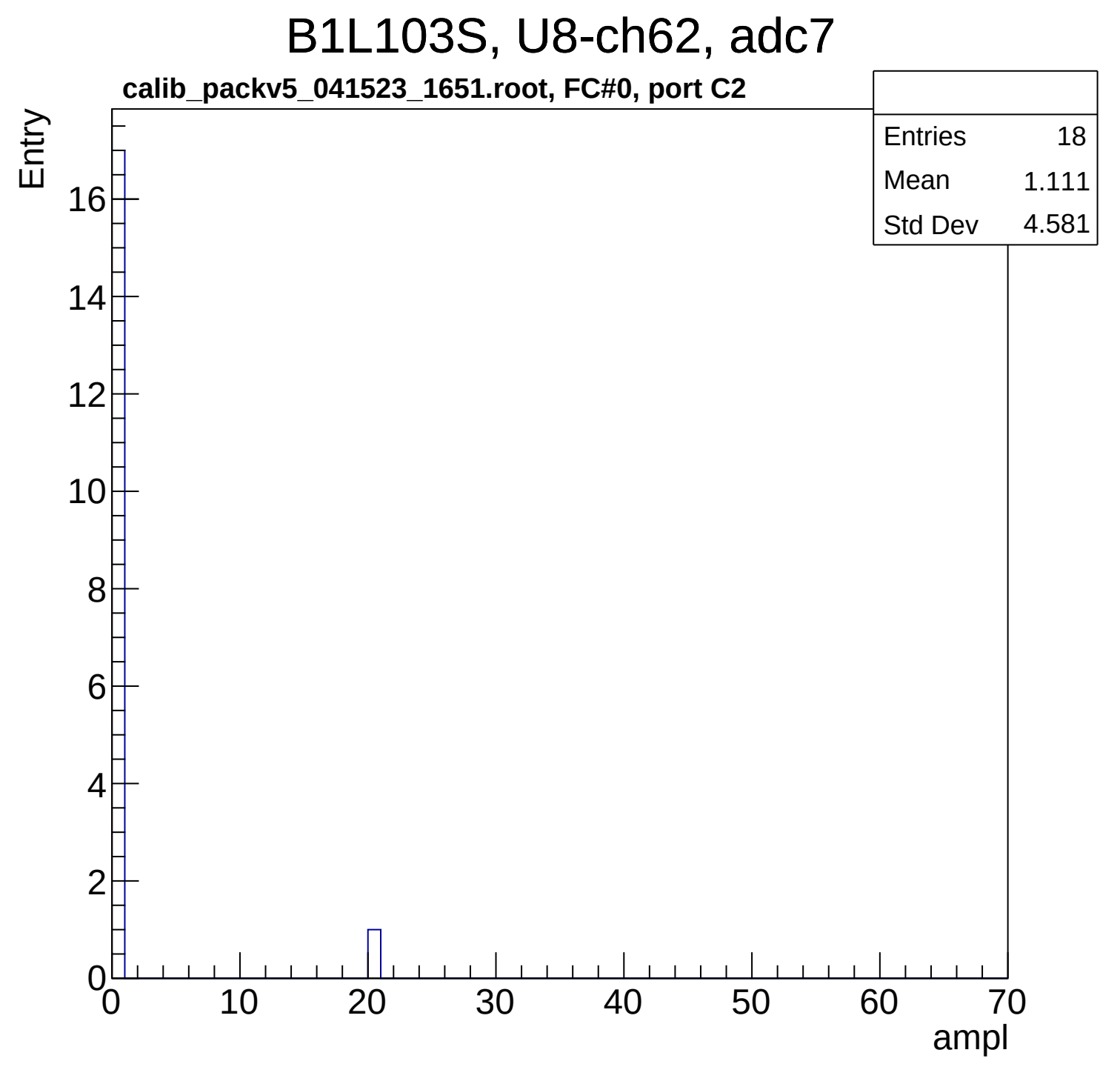
40
50
60
70


B1L103S, U8-ch62, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.111
Std Dev 4.581
Entry
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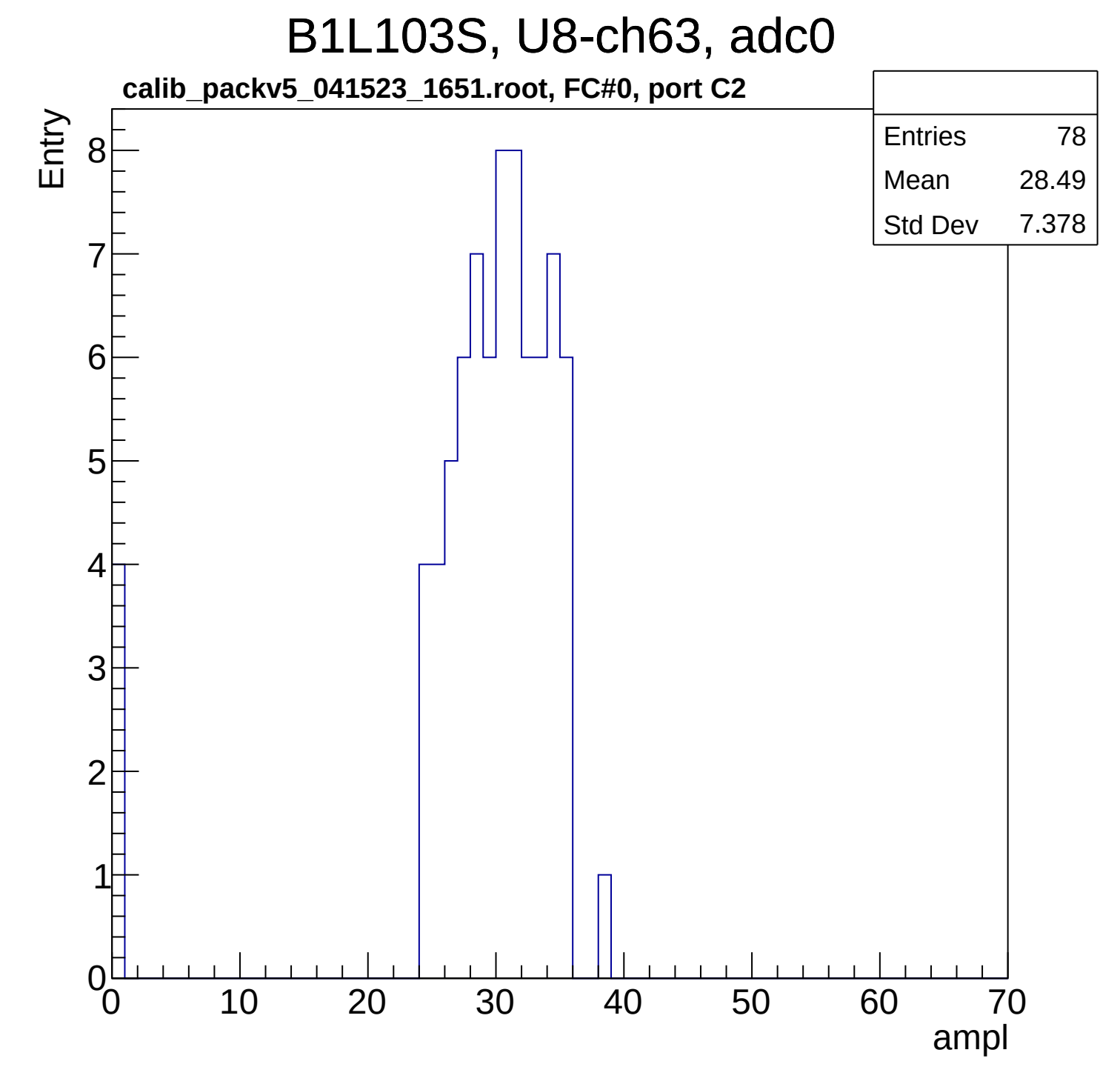
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch63, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 28.49
Std Dev 7.378
Entry
ampl
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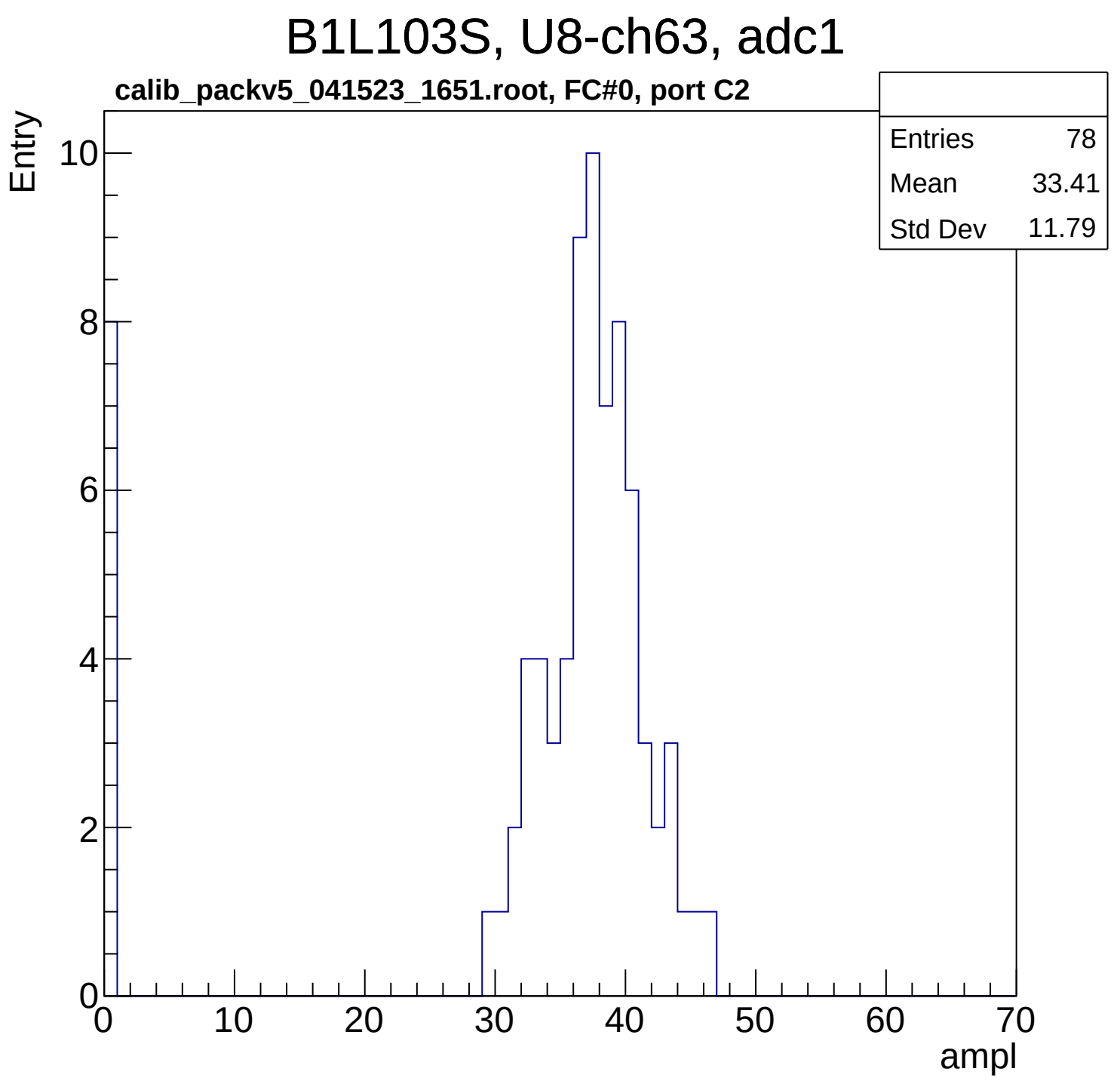
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch63, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 33.41
Std Dev 11.79
Entry
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6
8
10
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10
20
30
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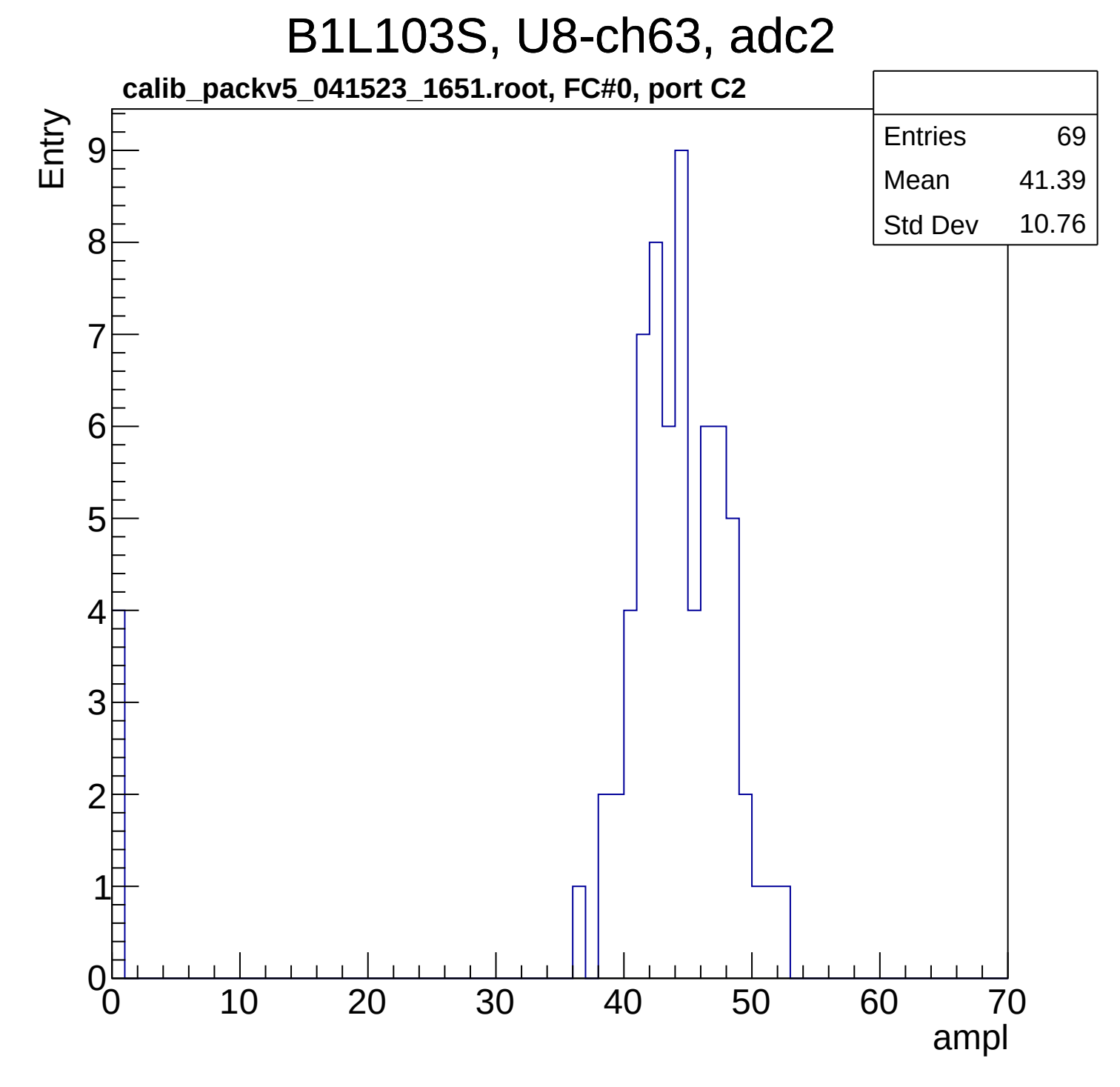
50
60
70
ampl


B1L103S, U8-ch63, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 41.39
Std Dev 10.76
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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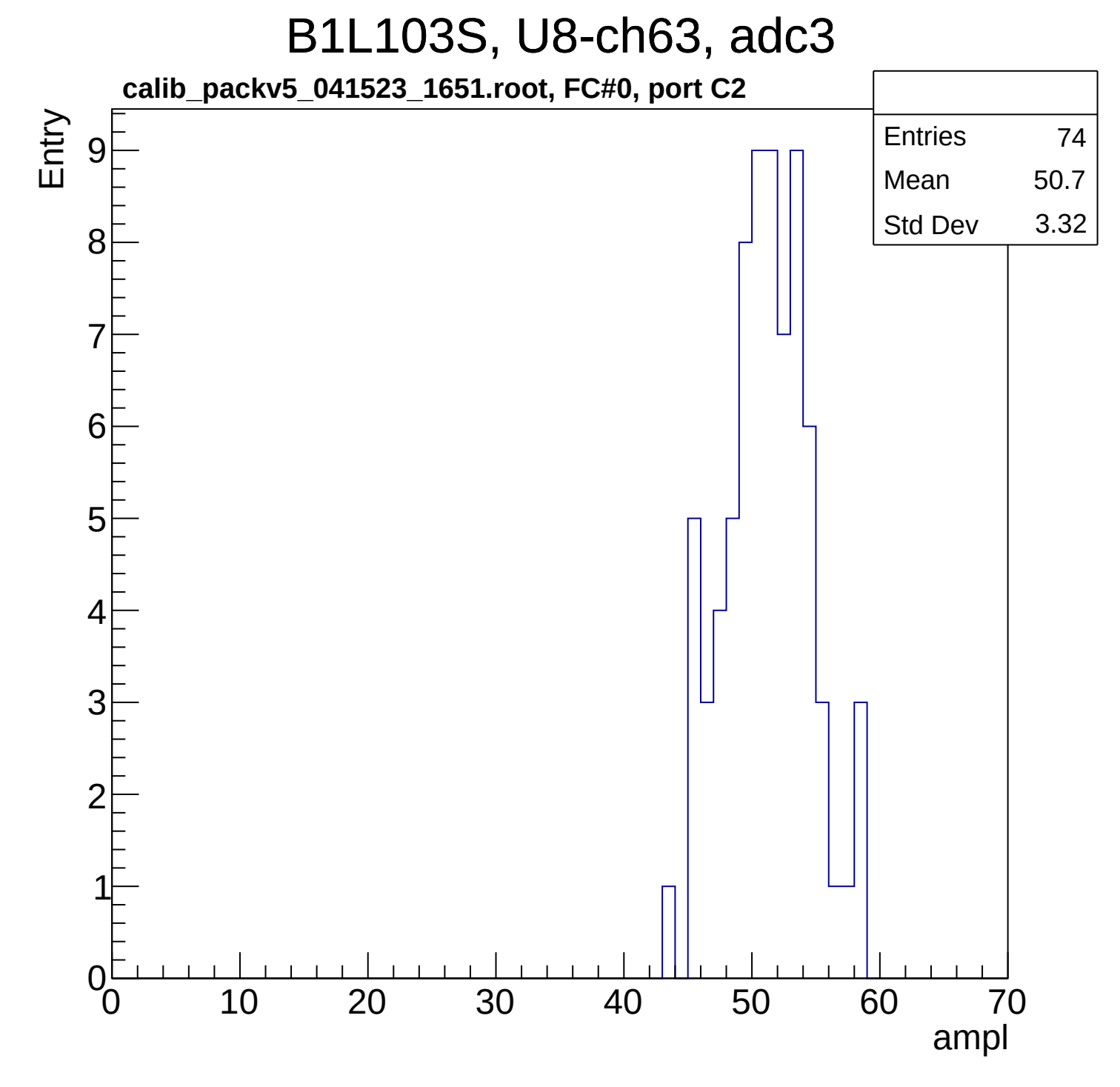
60
70


B1L103S, U8-ch63, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 50.7
Std Dev 3.32
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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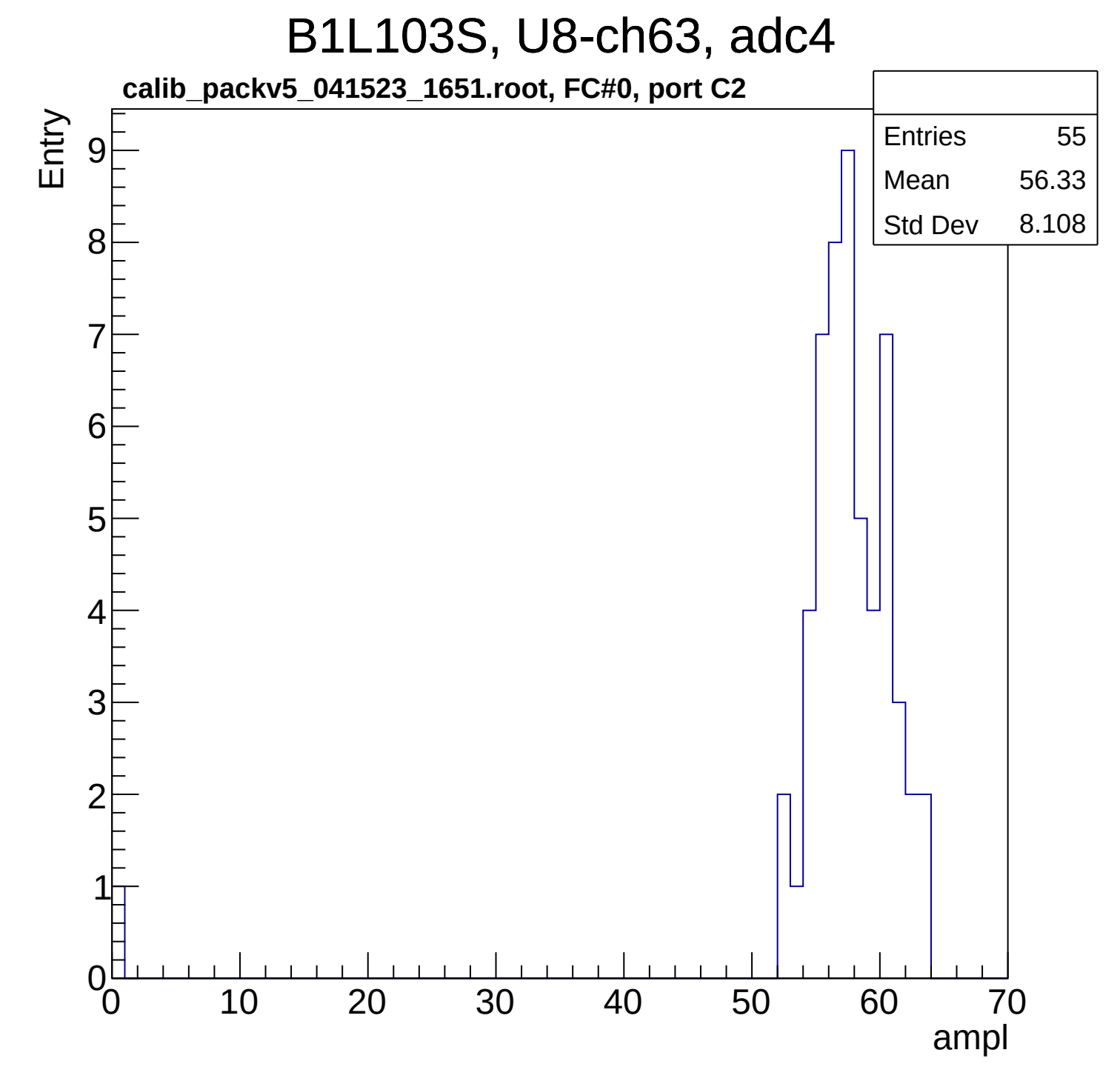
B1L103S, U8-ch63, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 56.33
Std Dev 8.108
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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20
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40
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60
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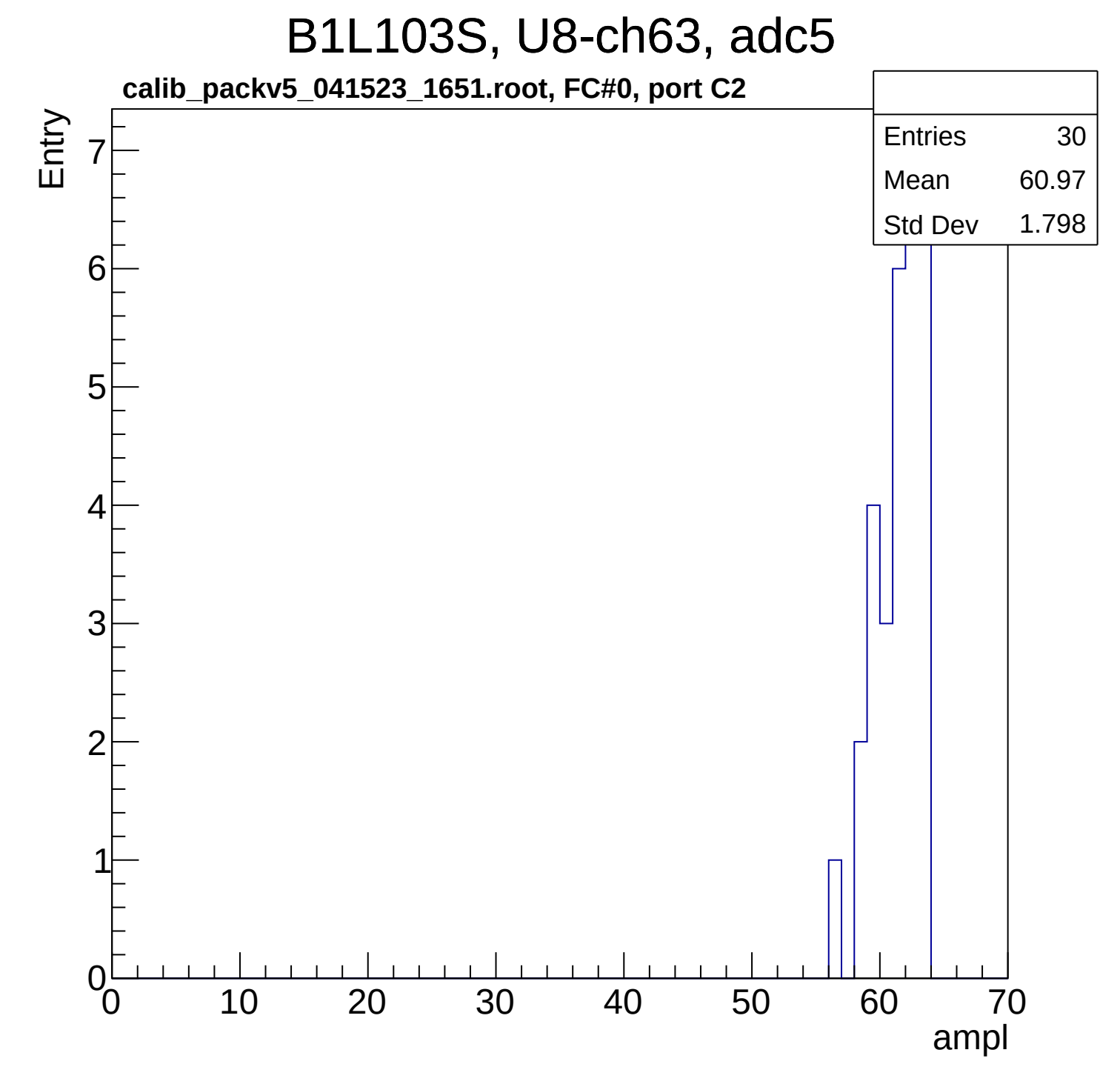
B1L103S, U8-ch63, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 60.97
Std Dev 1.798
Entry
ampl
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2
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4
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6
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0
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20
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60
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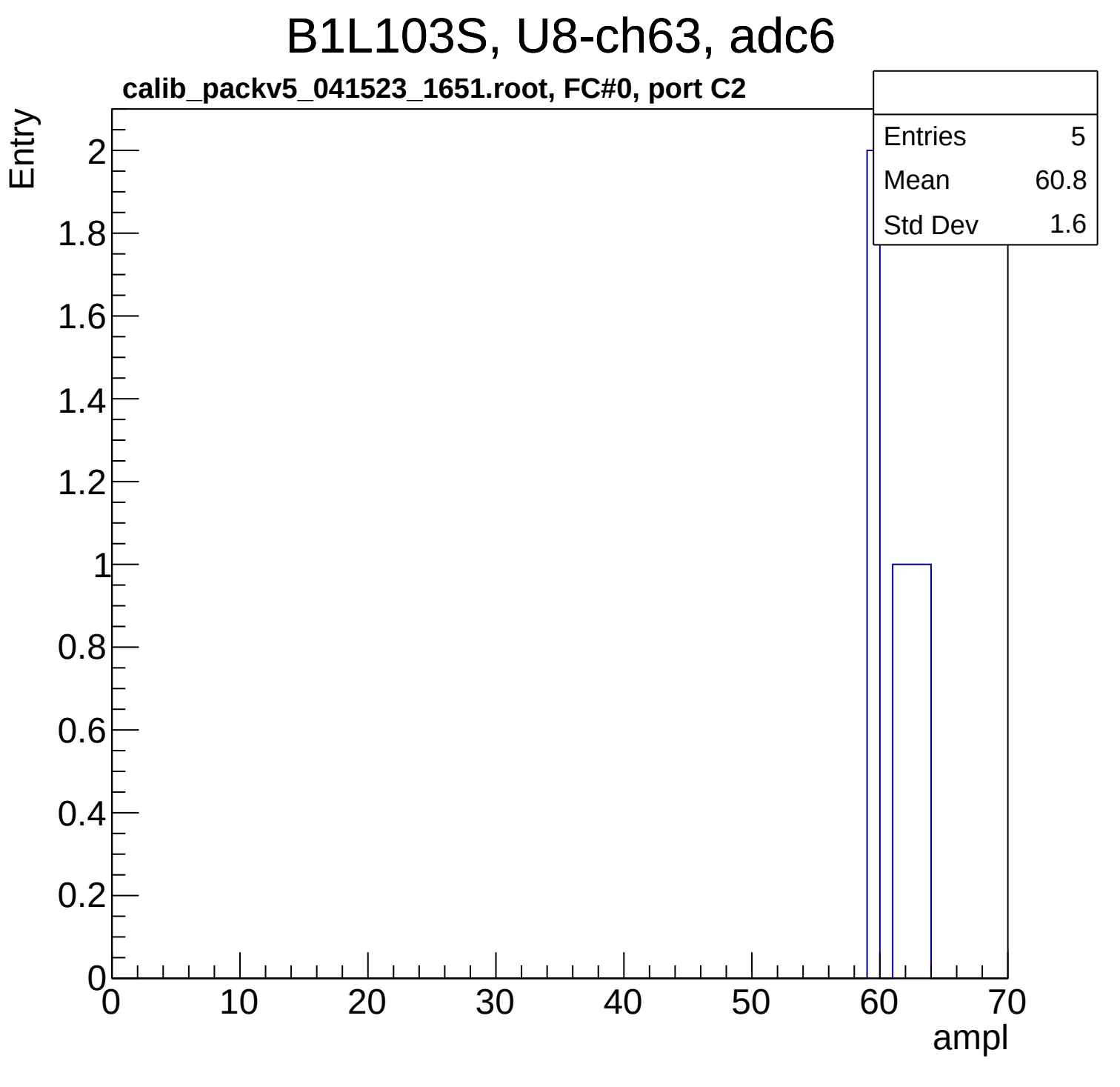
B1L103S, U8-ch63, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 60.8
Std Dev 1.6
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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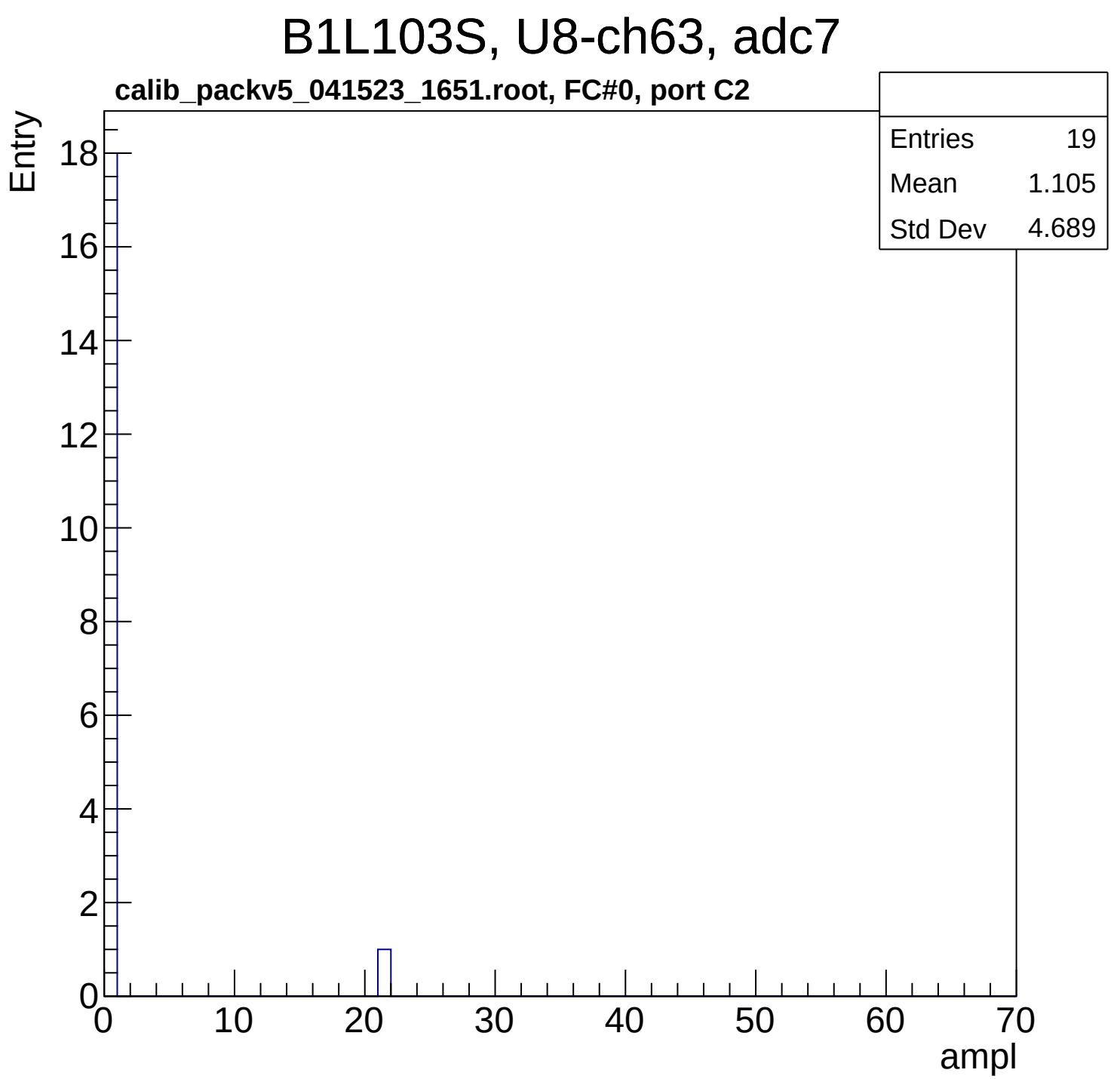
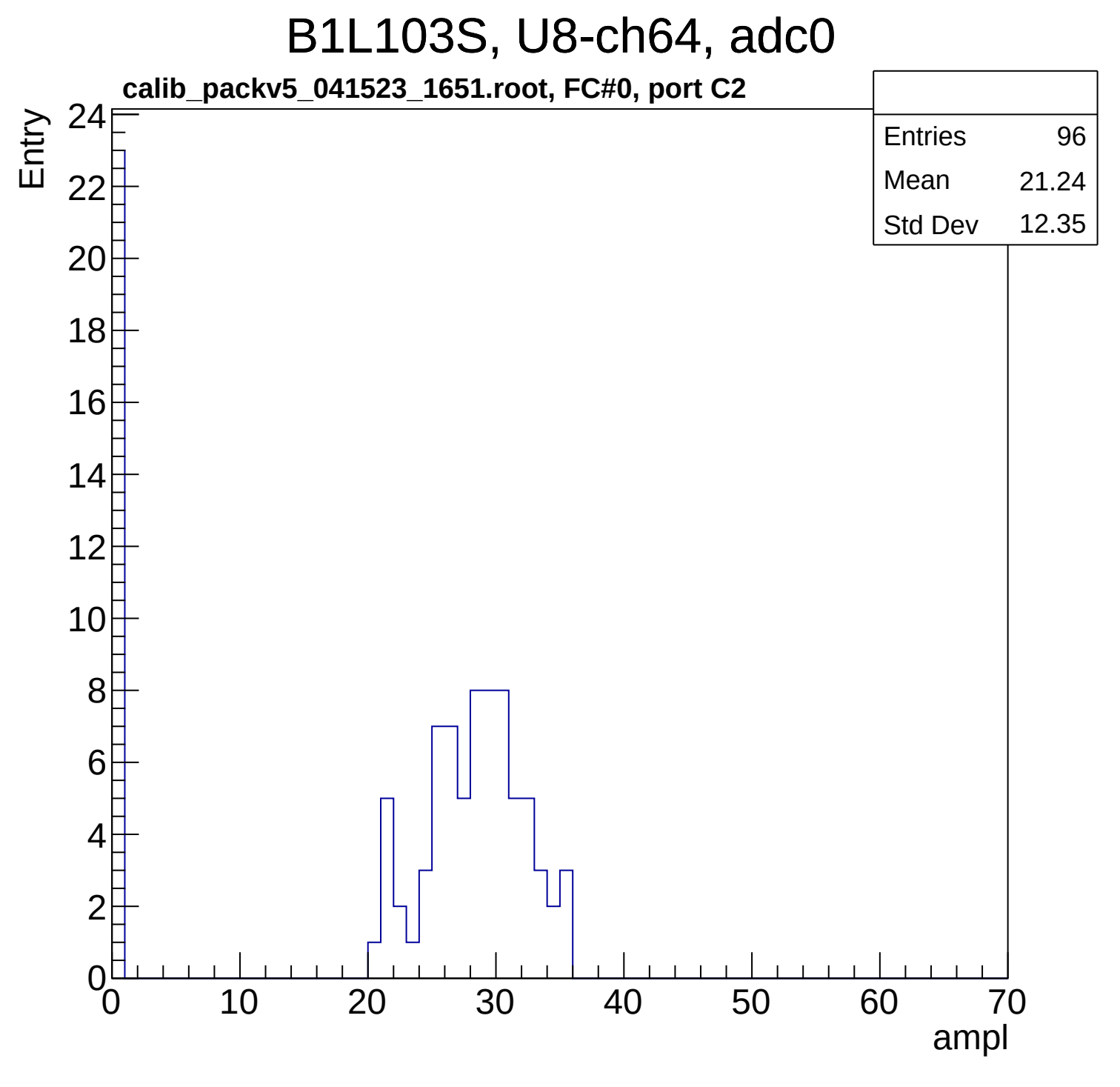

B1L103S, U8-ch63, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.105
Std Dev 4.689
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch64, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 96
Mean 21.24
Std Dev 12.35
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
24
0
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40
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60
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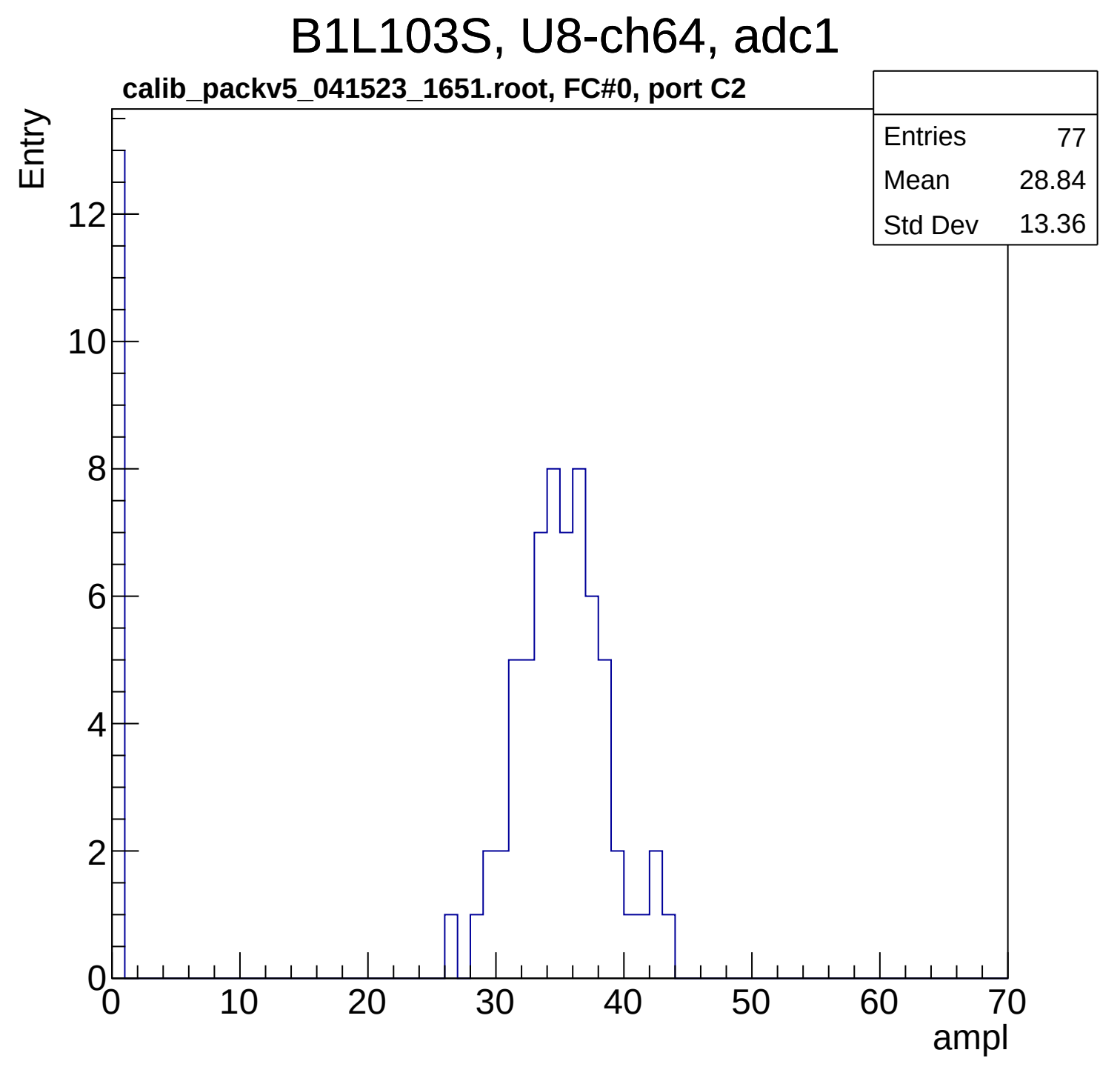
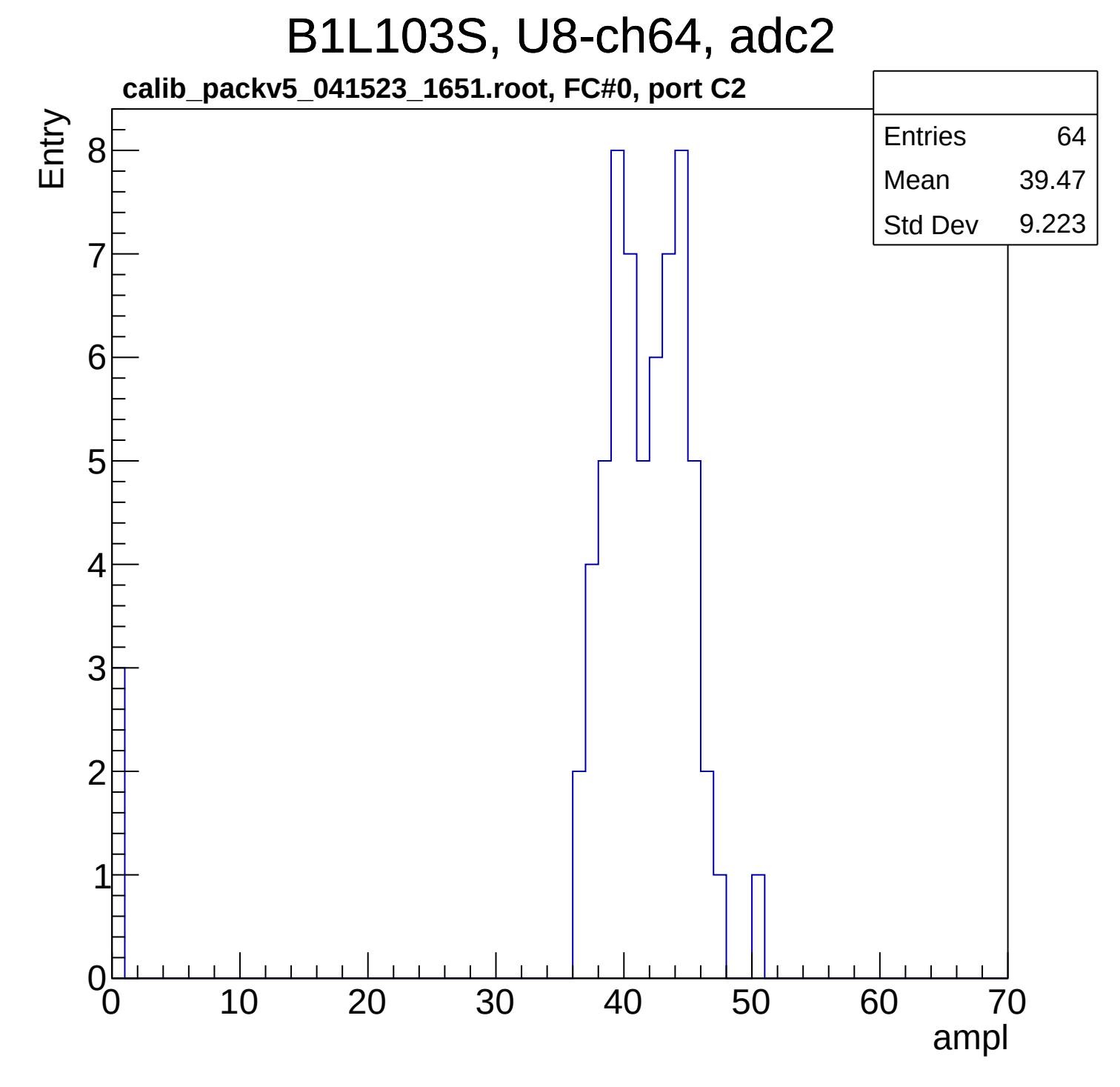

B1L103S, U8-ch64, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 28.84
Std Dev 13.36
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch64, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 39.47
Std Dev 9.223
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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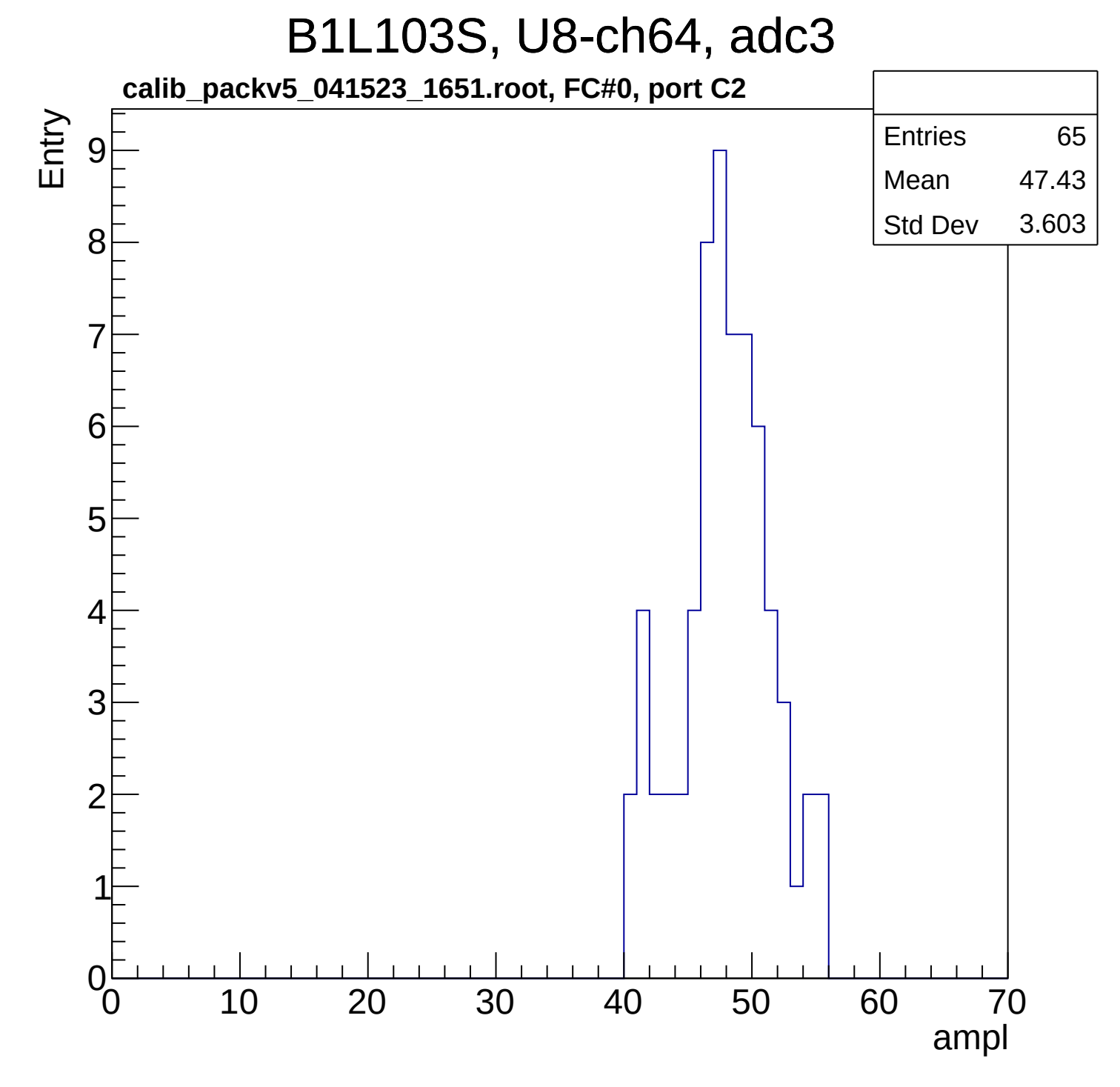
B1L103S, U8-ch64, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 47.43
Std Dev 3.603
Entry
ampl
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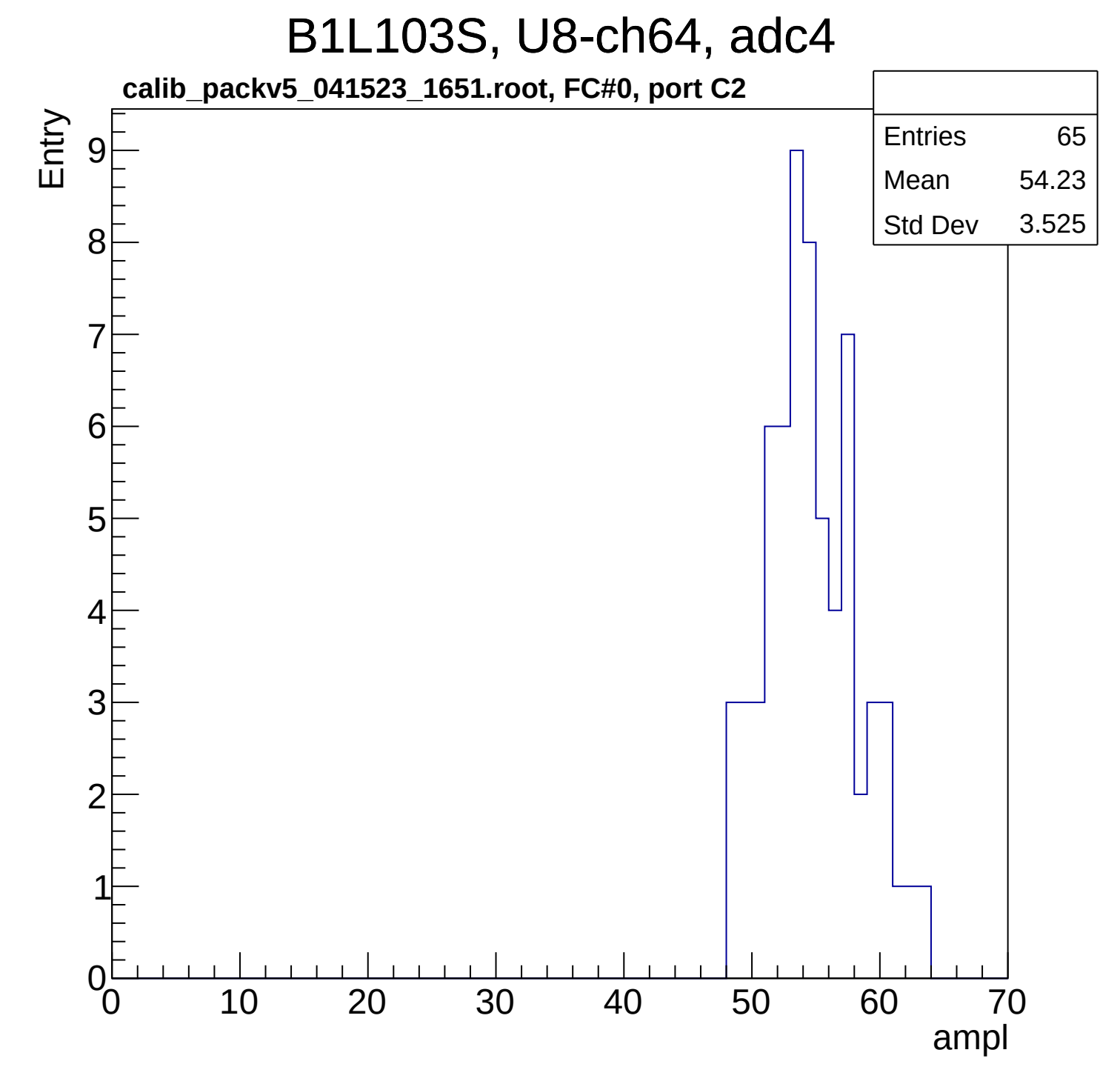
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U8-ch64, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 54.23
Std Dev 3.525
Entry
ampl
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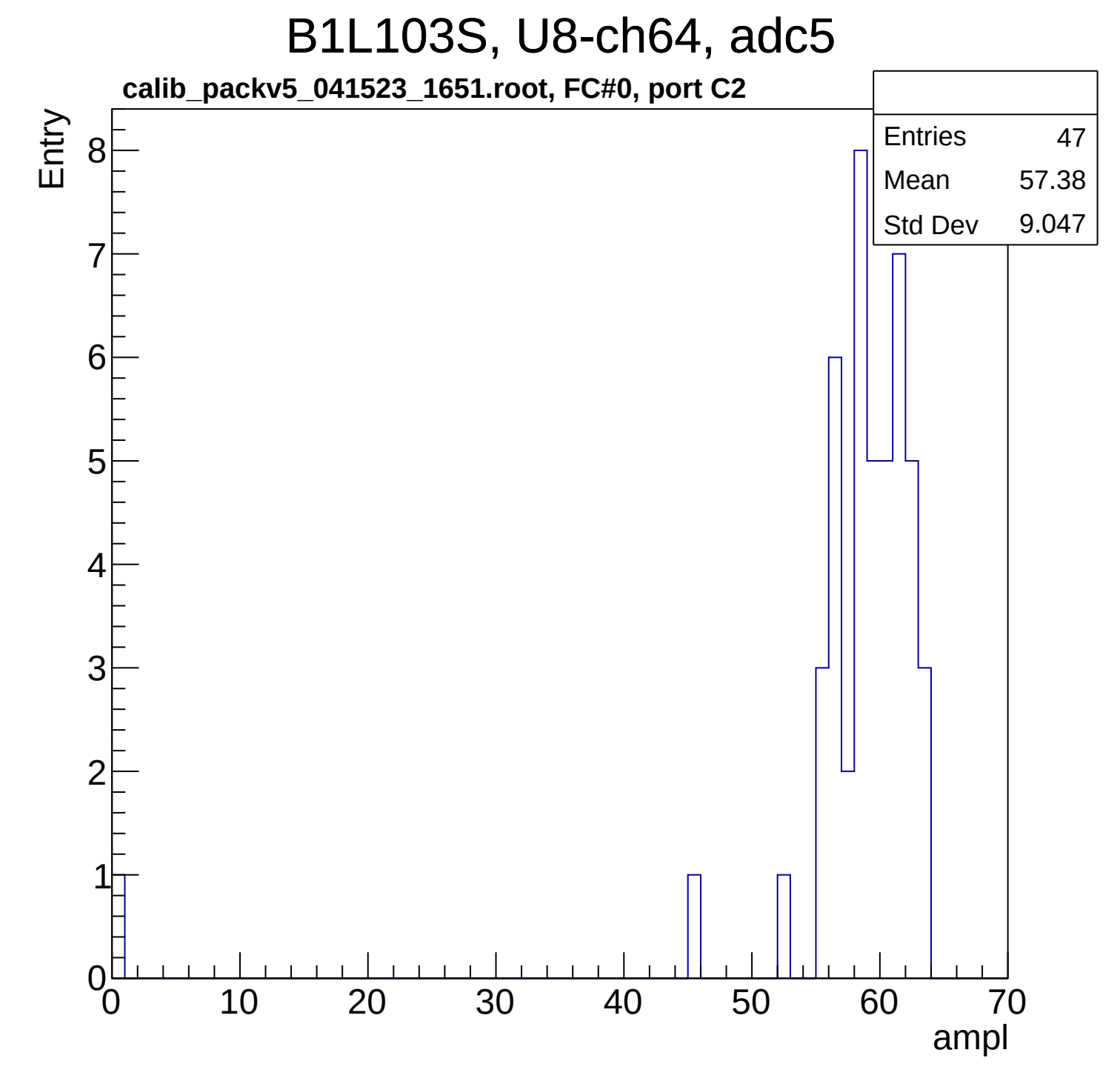
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U8-ch64, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 57.38
Std Dev 9.047
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
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60
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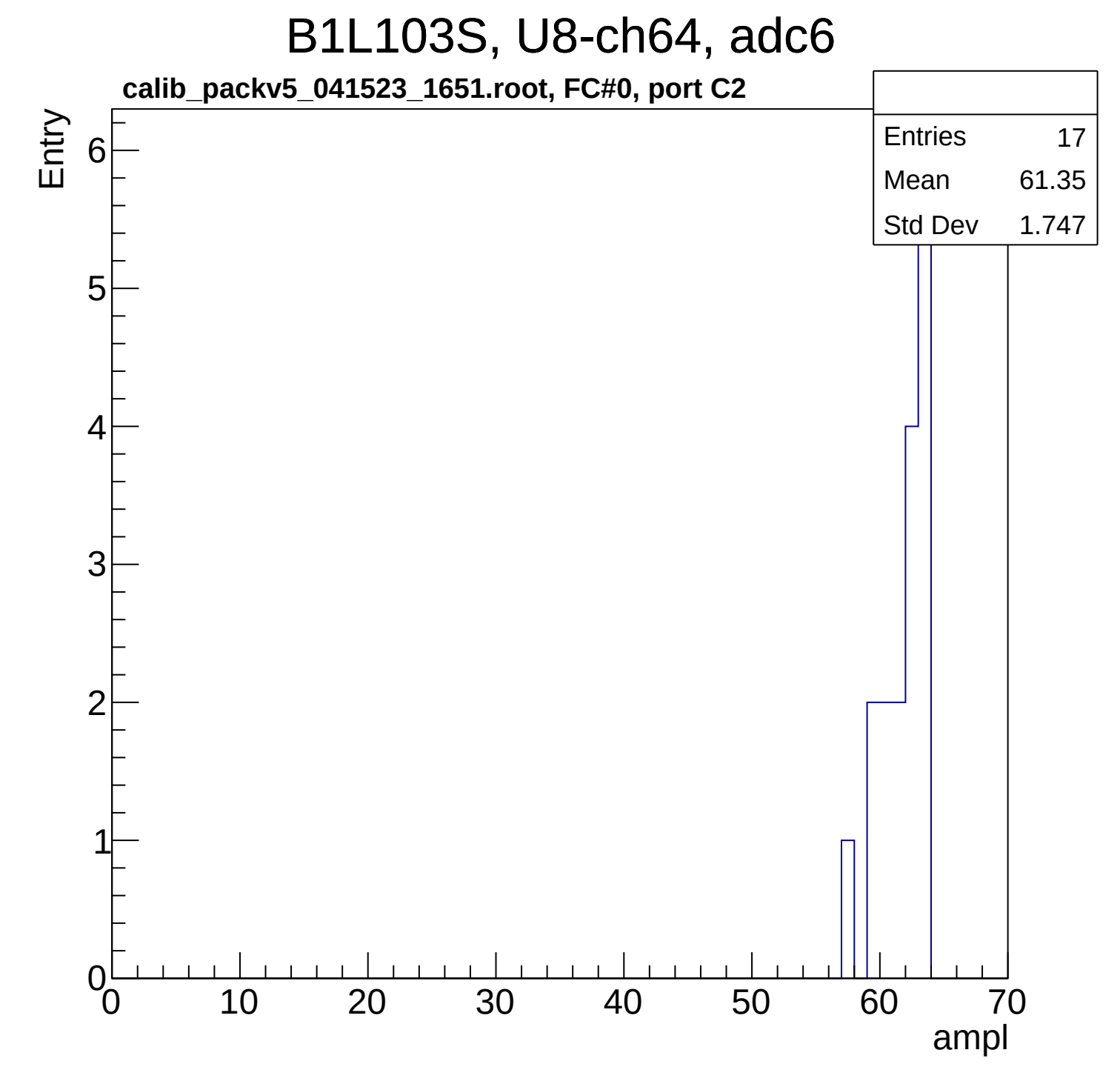
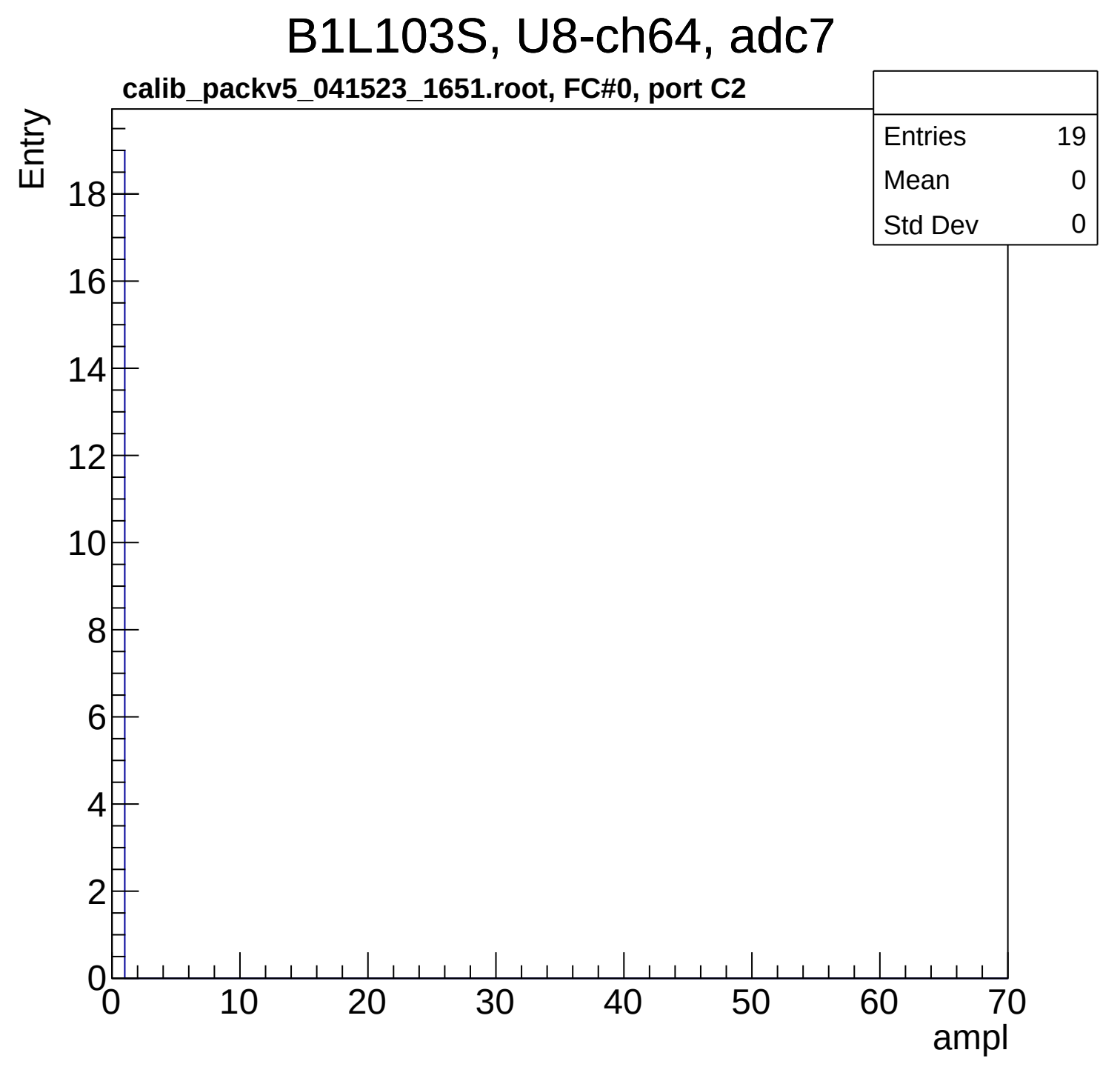
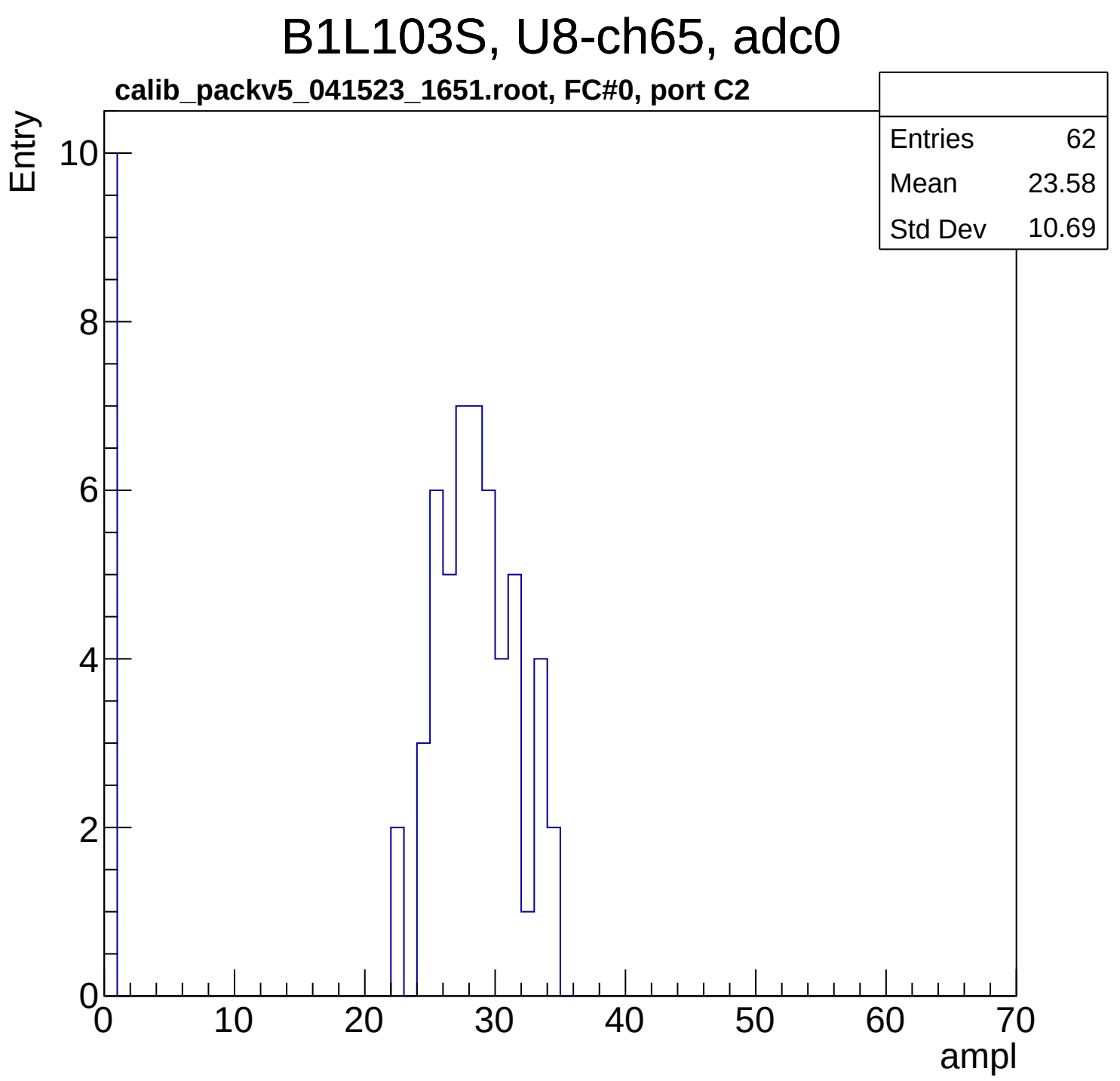
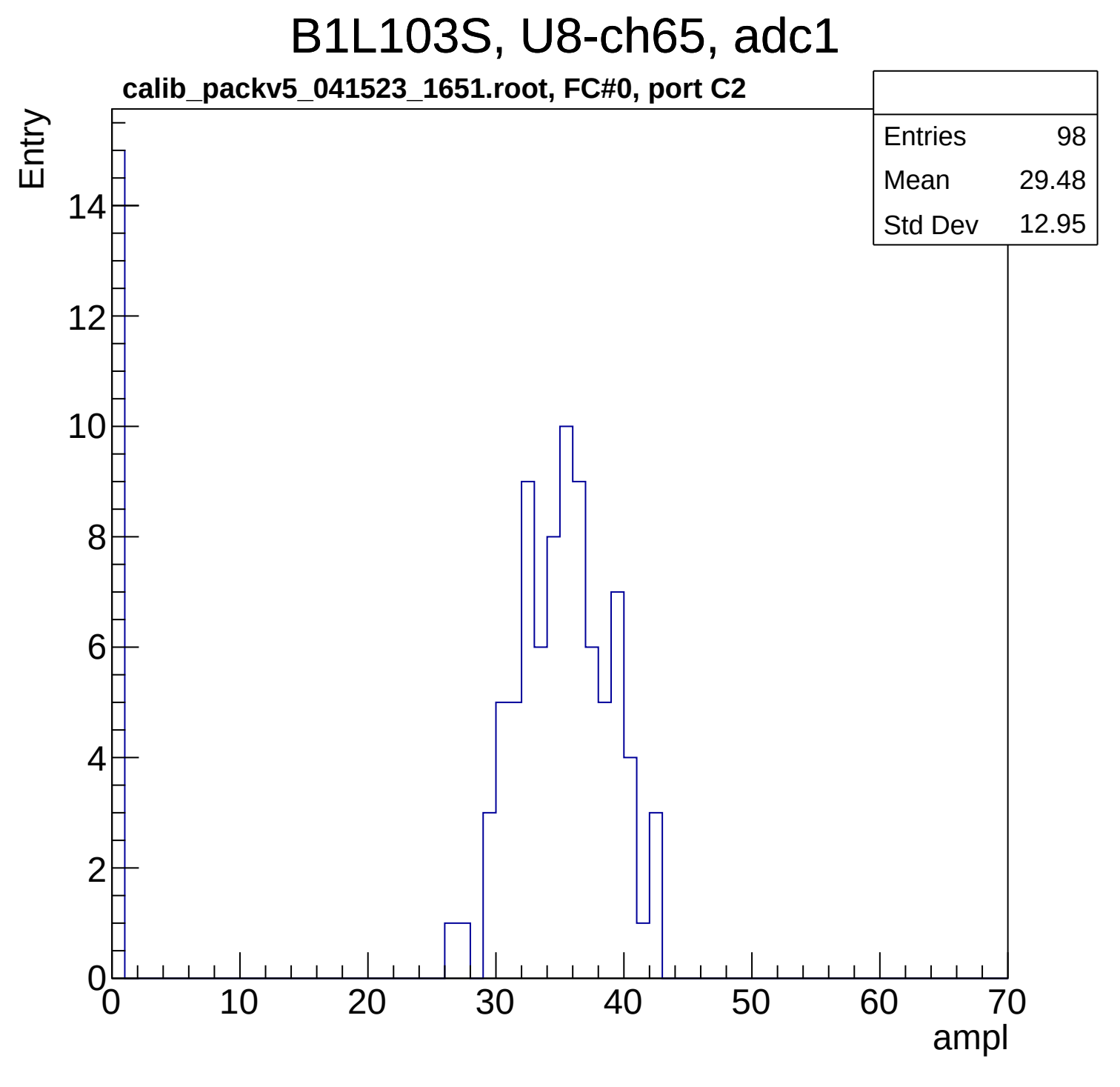

B1L103S, U8-ch64, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 61.35
Std Dev 1.747
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U8-ch64, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch65, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 23.58
Std Dev 10.69
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch65, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 98
Mean 29.48
Std Dev 12.95
Entry
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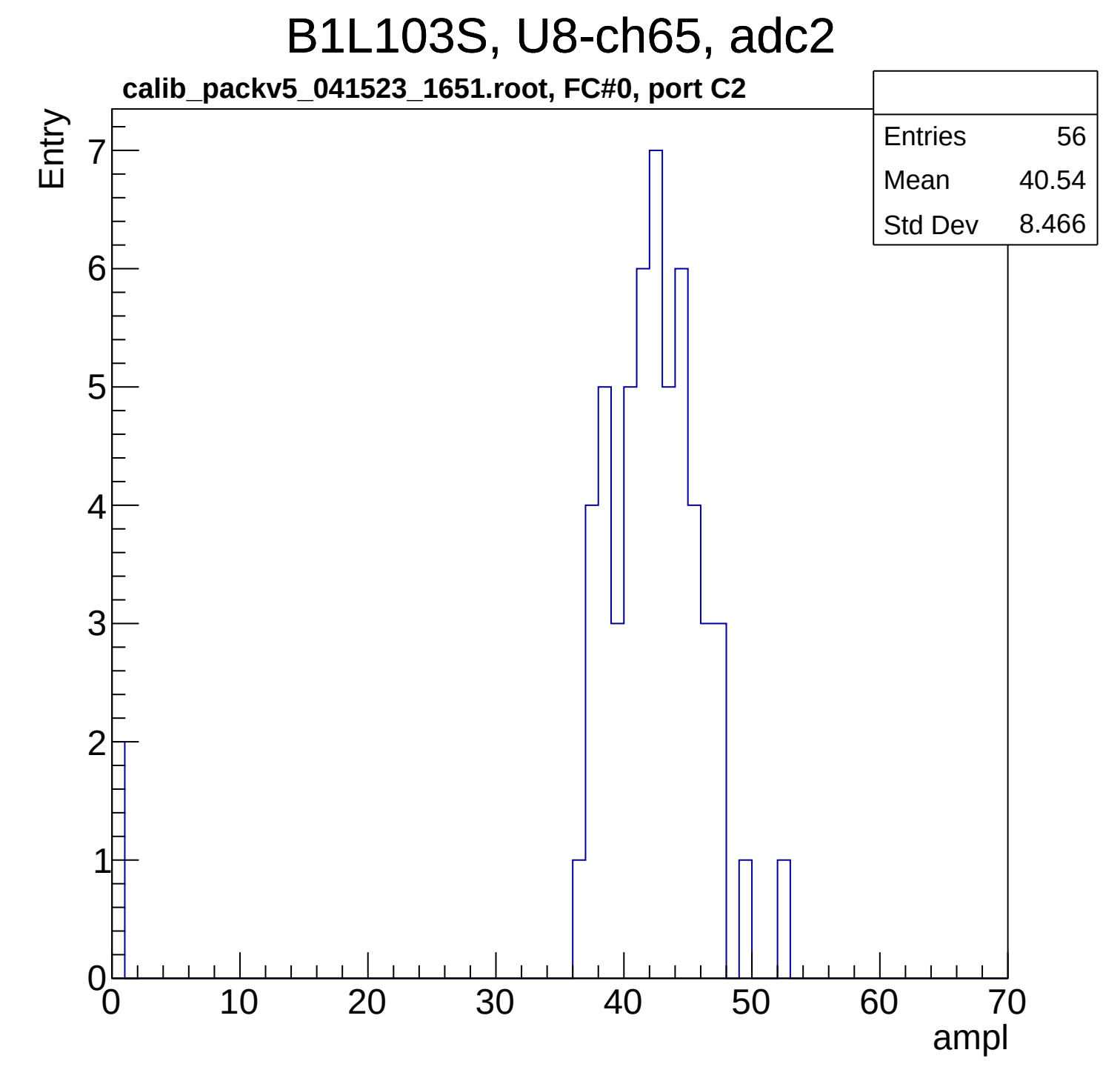
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch65, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 40.54
Std Dev 8.466
Entry
ampl
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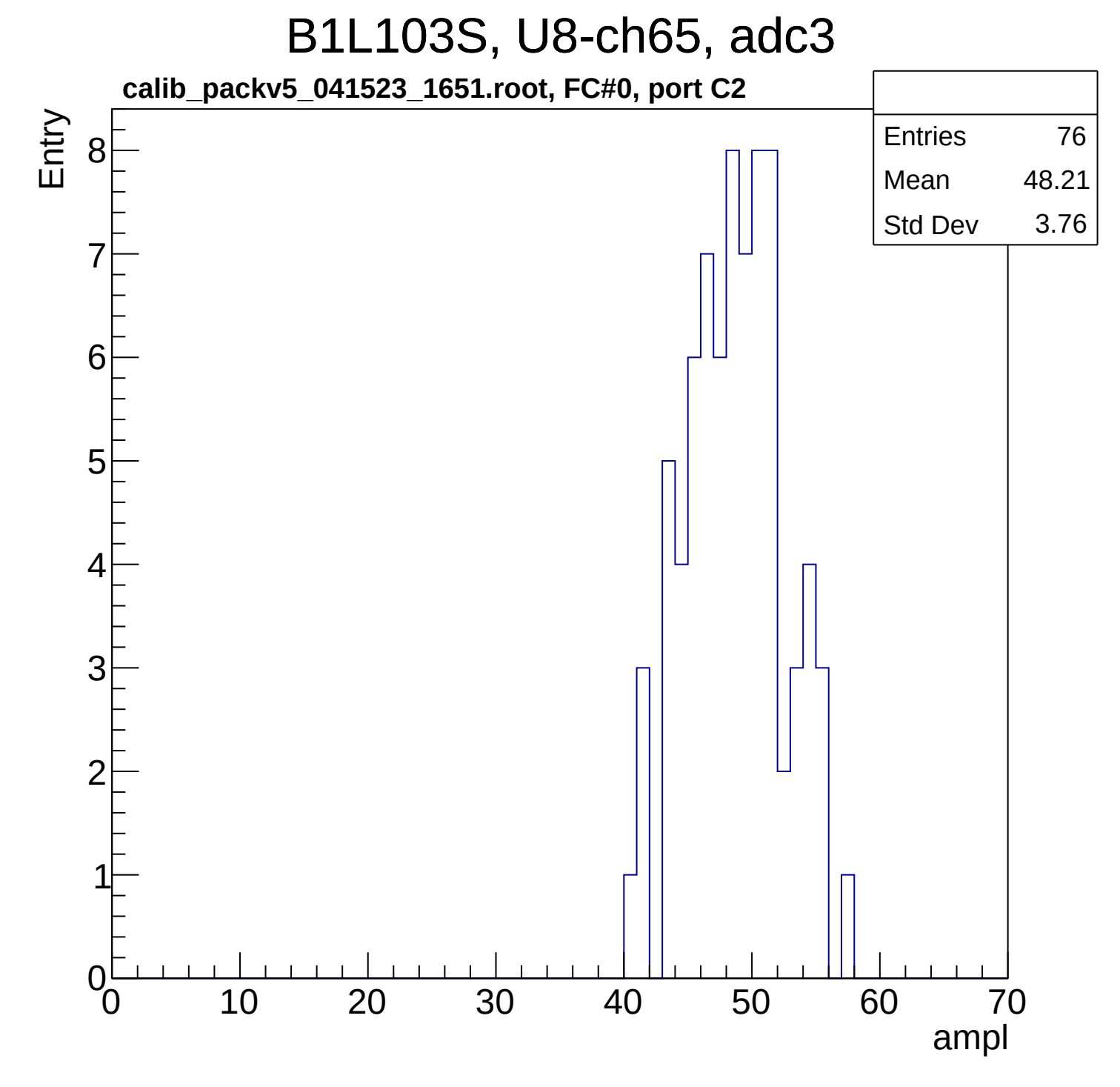
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U8-ch65, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 48.21
Std Dev 3.76
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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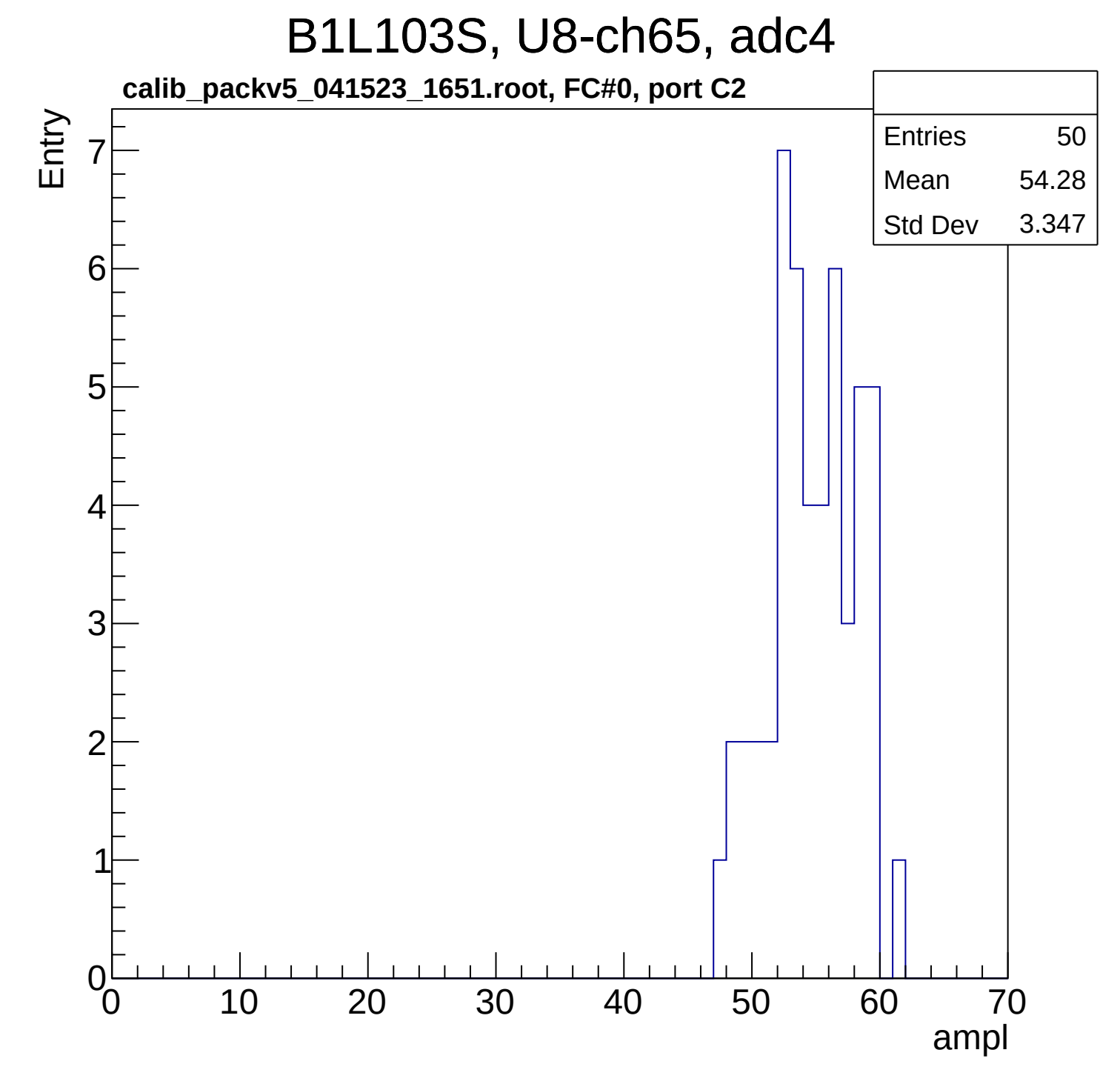
B1L103S, U8-ch65, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 54.28
Std Dev 3.347
Entry
ampl
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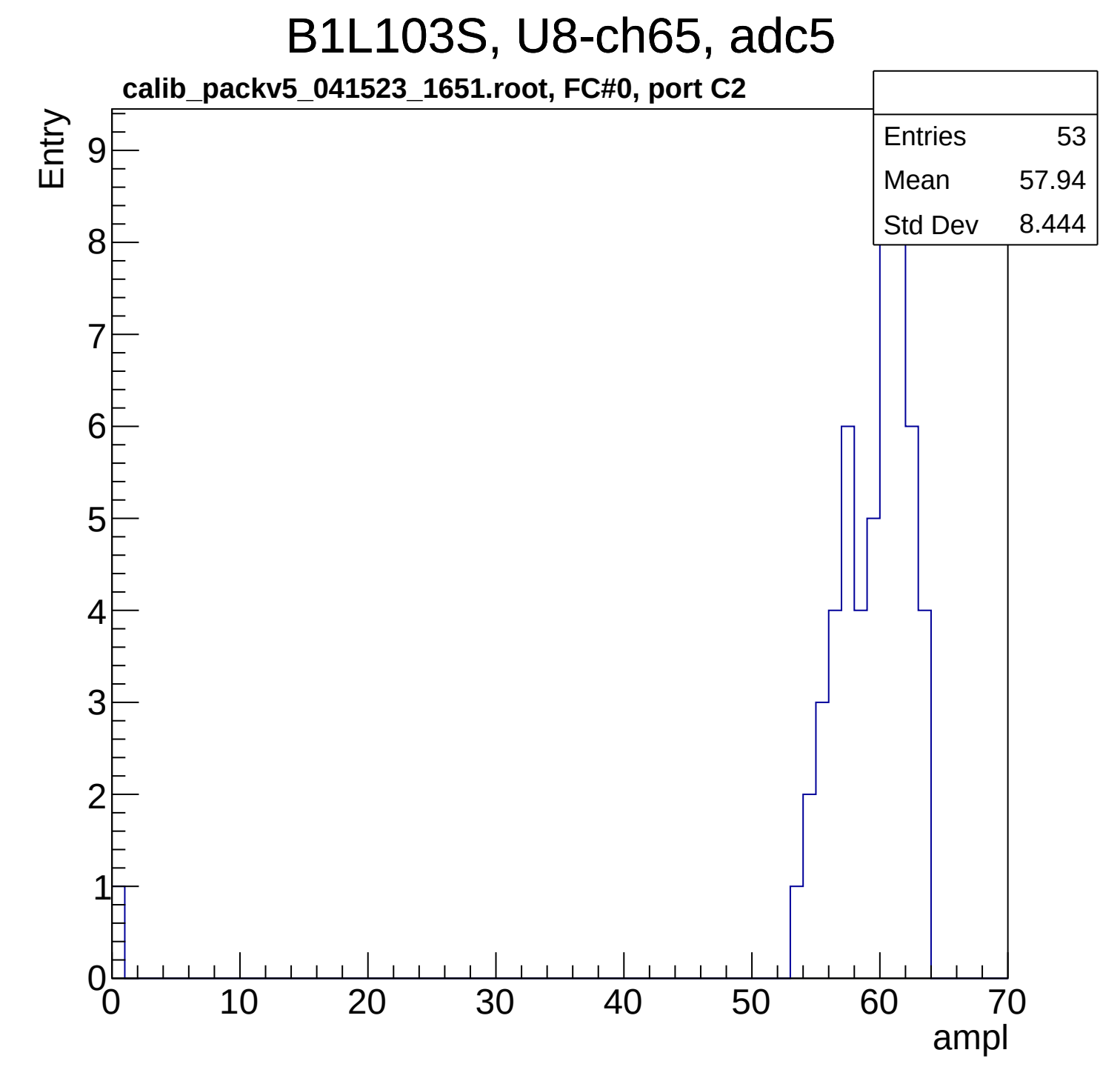
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U8-ch65, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 57.94
Std Dev 8.444
Entry
ampl
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3
4
5
6
7
8
9
0
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20
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40
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60
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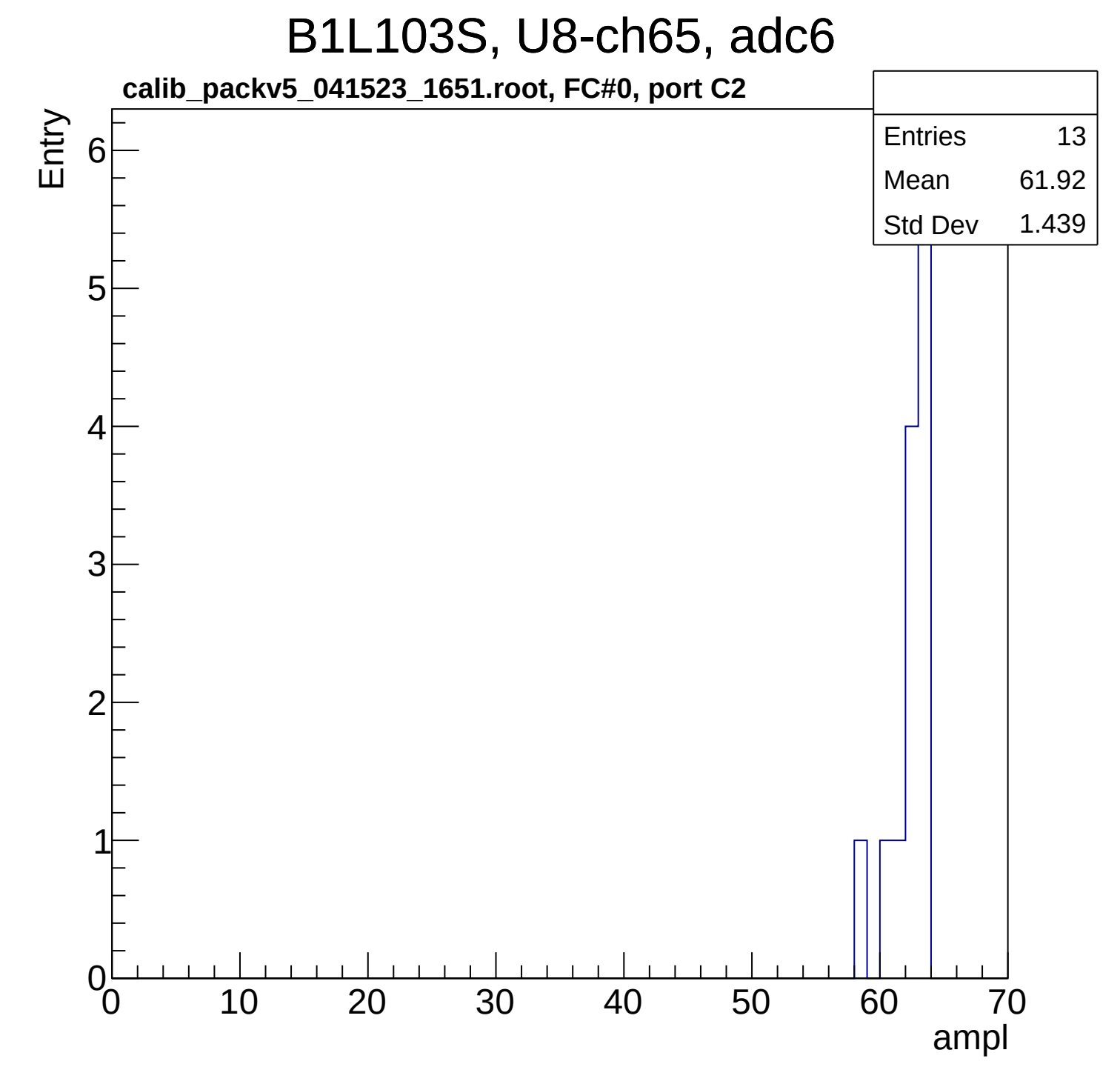
B1L103S, U8-ch65, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 61.92
Std Dev 1.439
Entry
ampl
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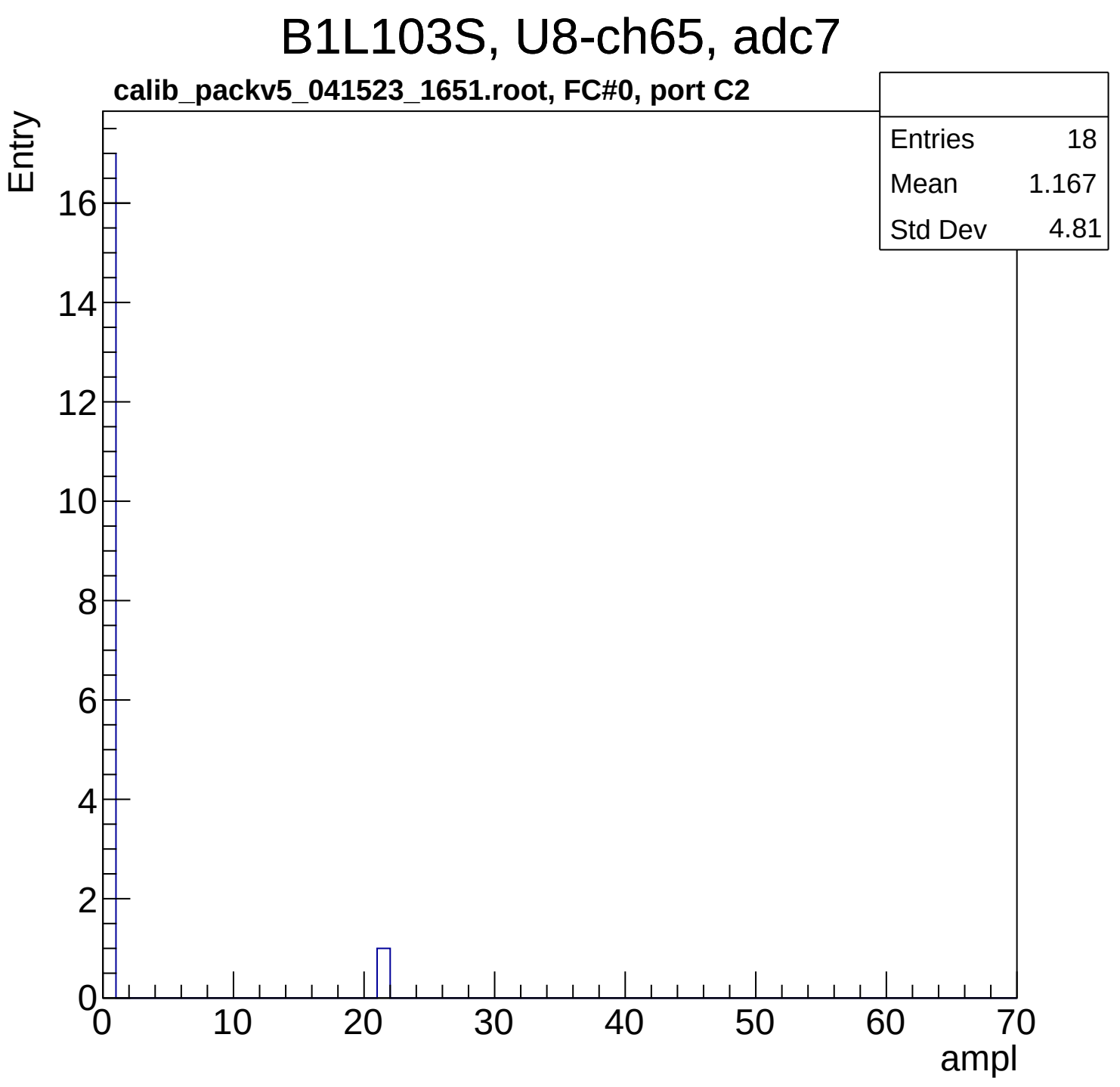
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U8-ch65, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.167
Std Dev 4.81
Entry
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4
6
8
10
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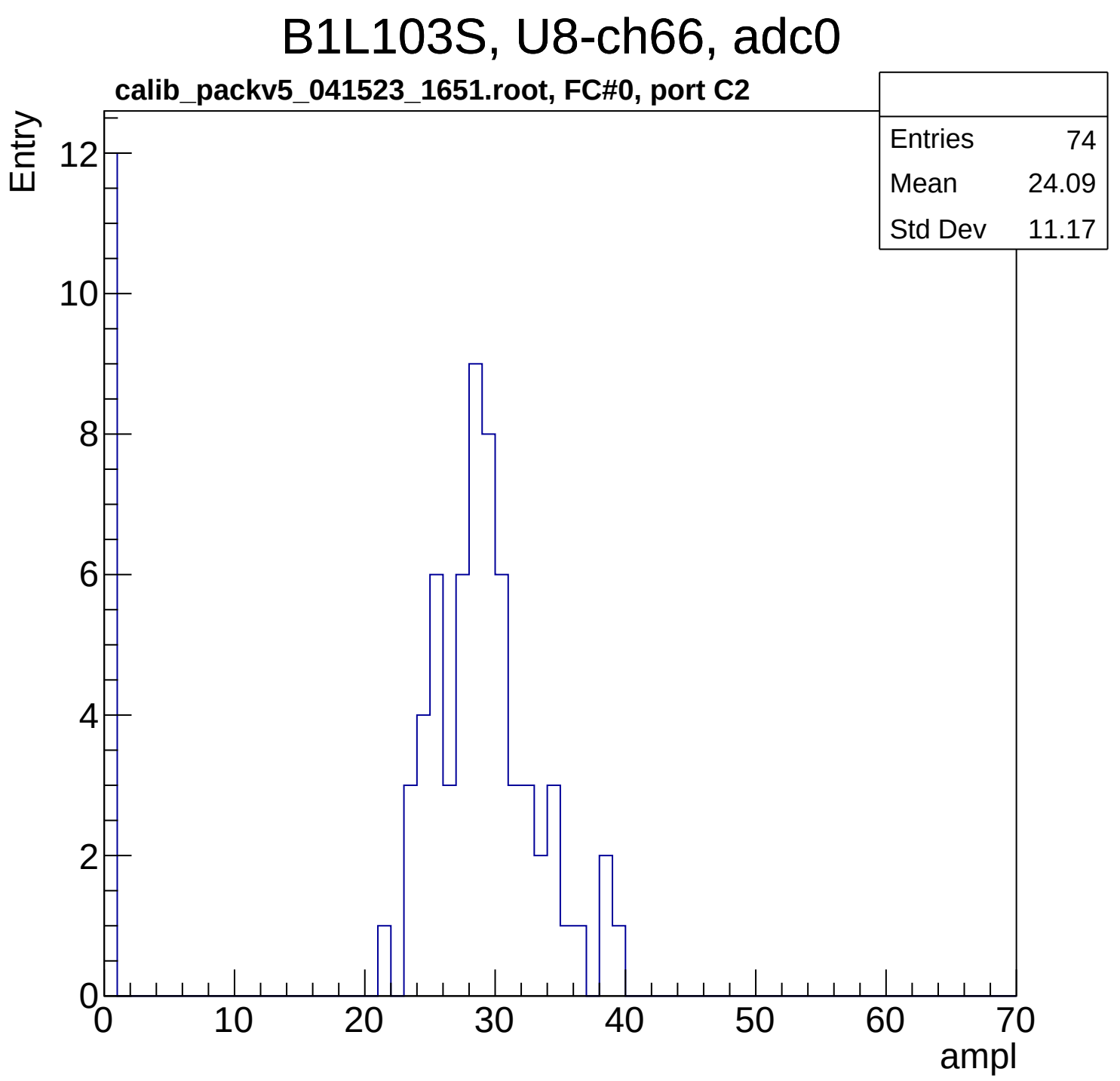
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch66, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 24.09
Std Dev 11.17
Entry
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12
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10
20
30
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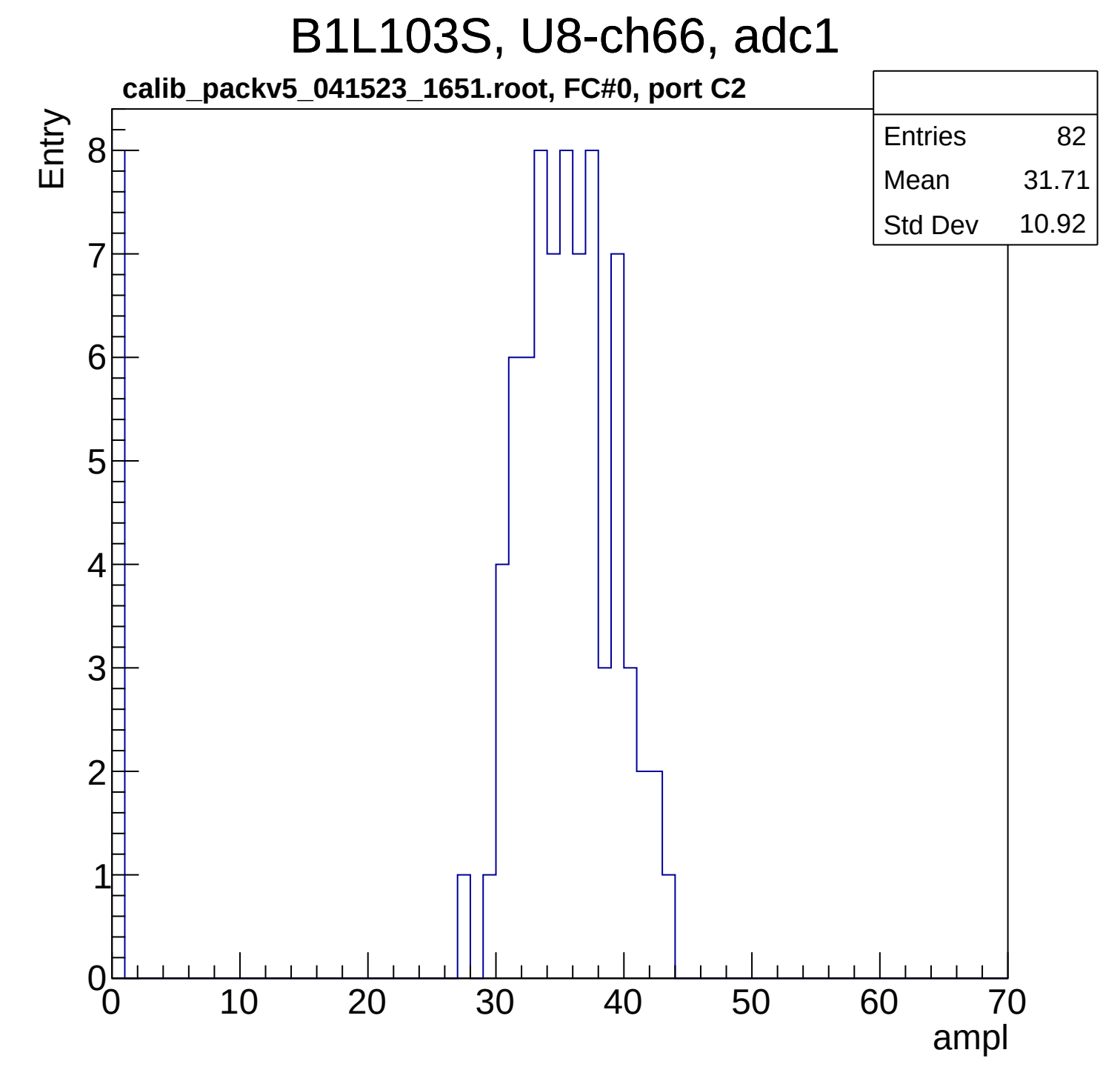
50
60
70
ampl


B1L103S, U8-ch66, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 31.71
Std Dev 10.92
Entry
ampl
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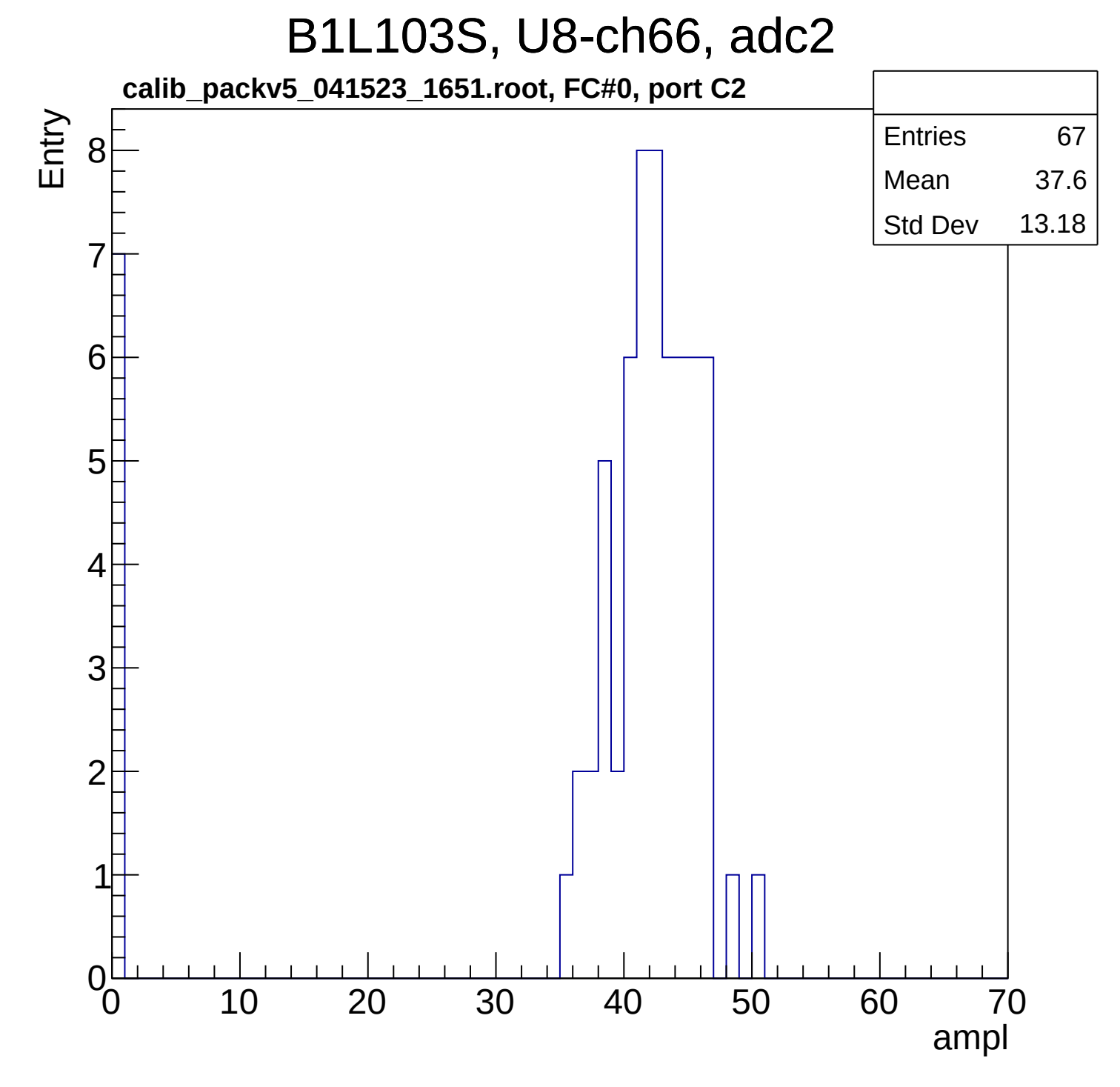
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch66, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 37.6
Std Dev 13.18
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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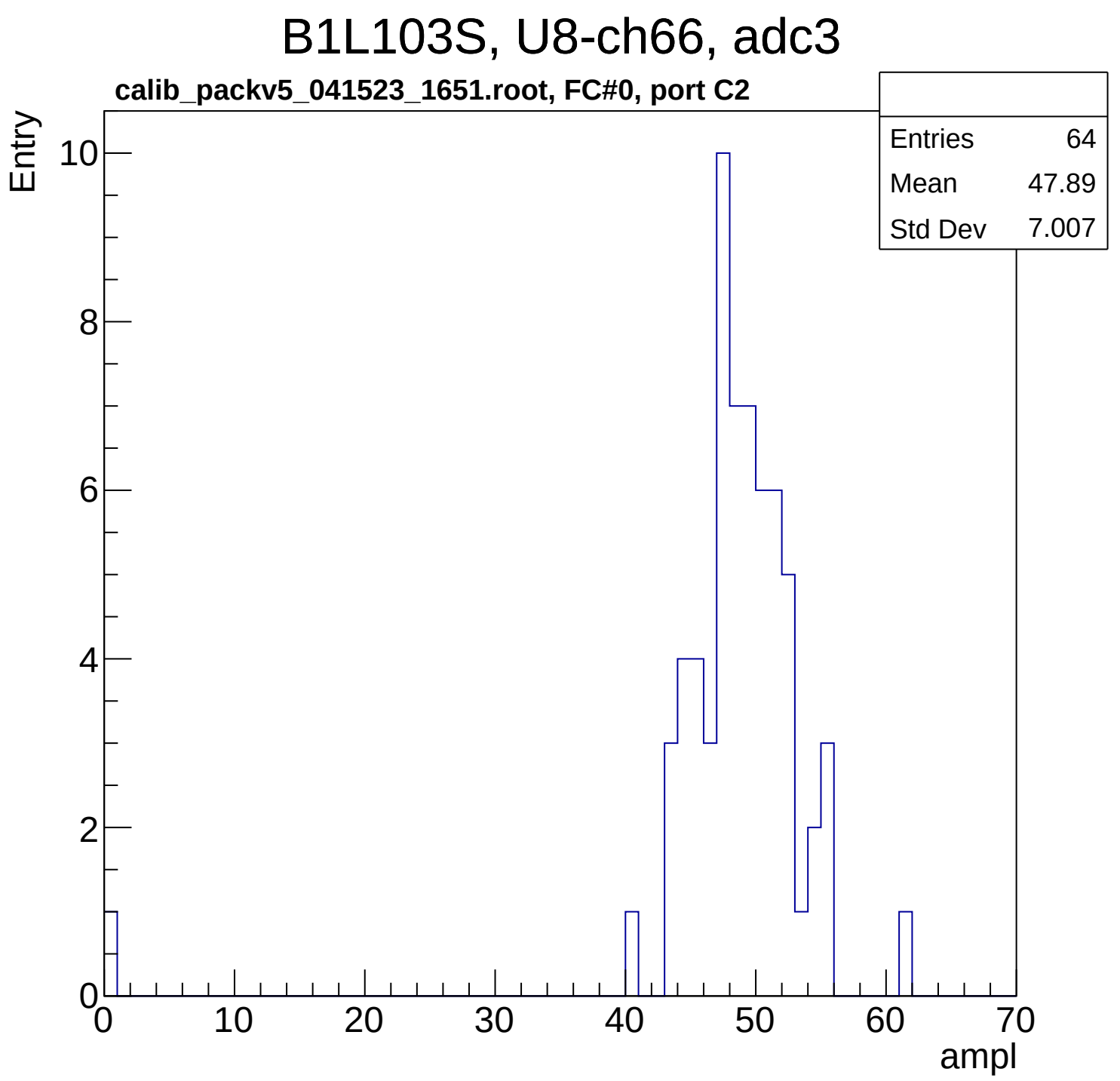
40
50
60
70


B1L103S, U8-ch66, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 47.89
Std Dev 7.007
Entry
ampl
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4
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8
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0
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20
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40
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60
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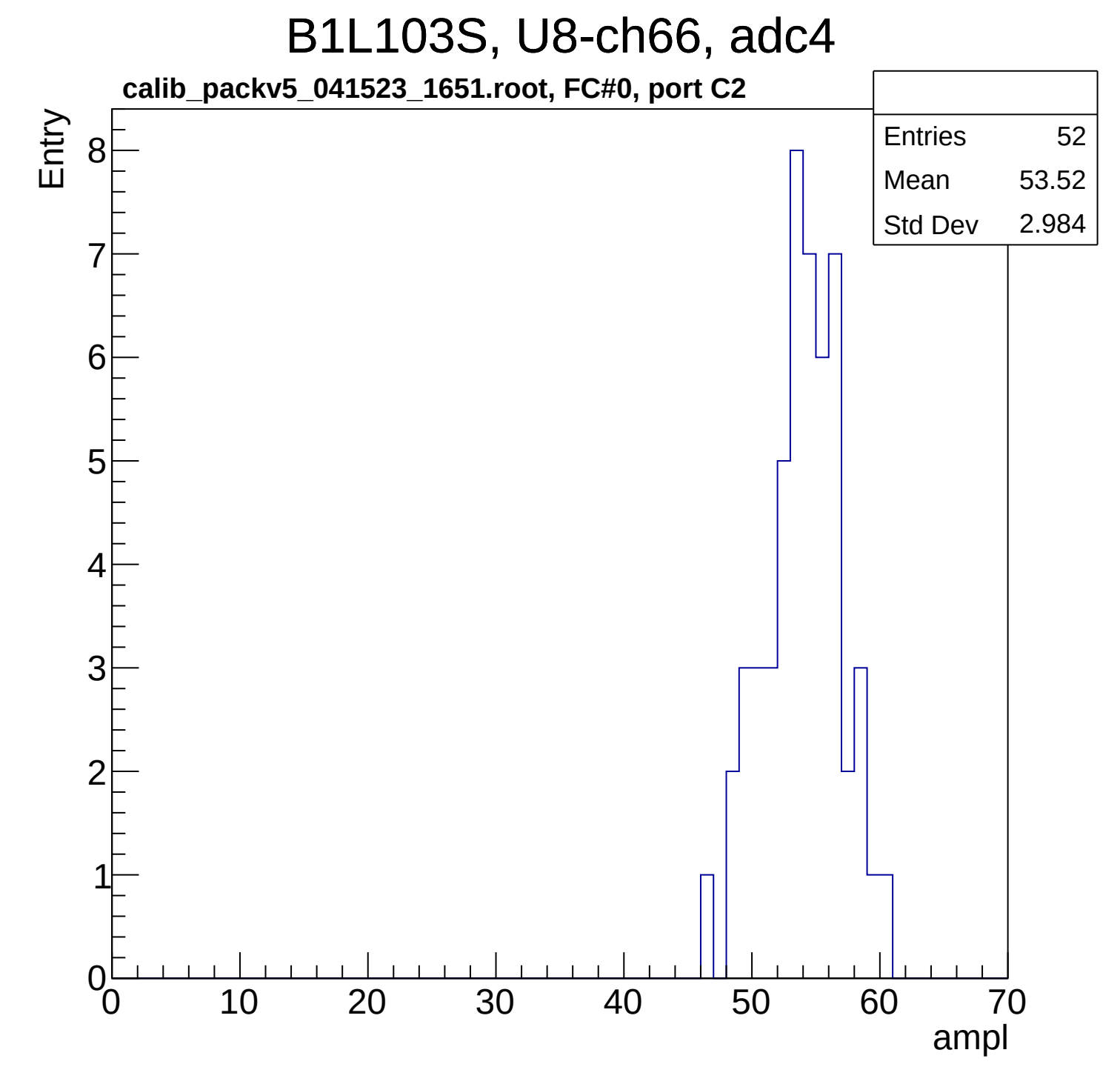
B1L103S, U8-ch66, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 53.52
Std Dev 2.984
Entry
ampl
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1
2
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4
5
6
7
8
0
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60
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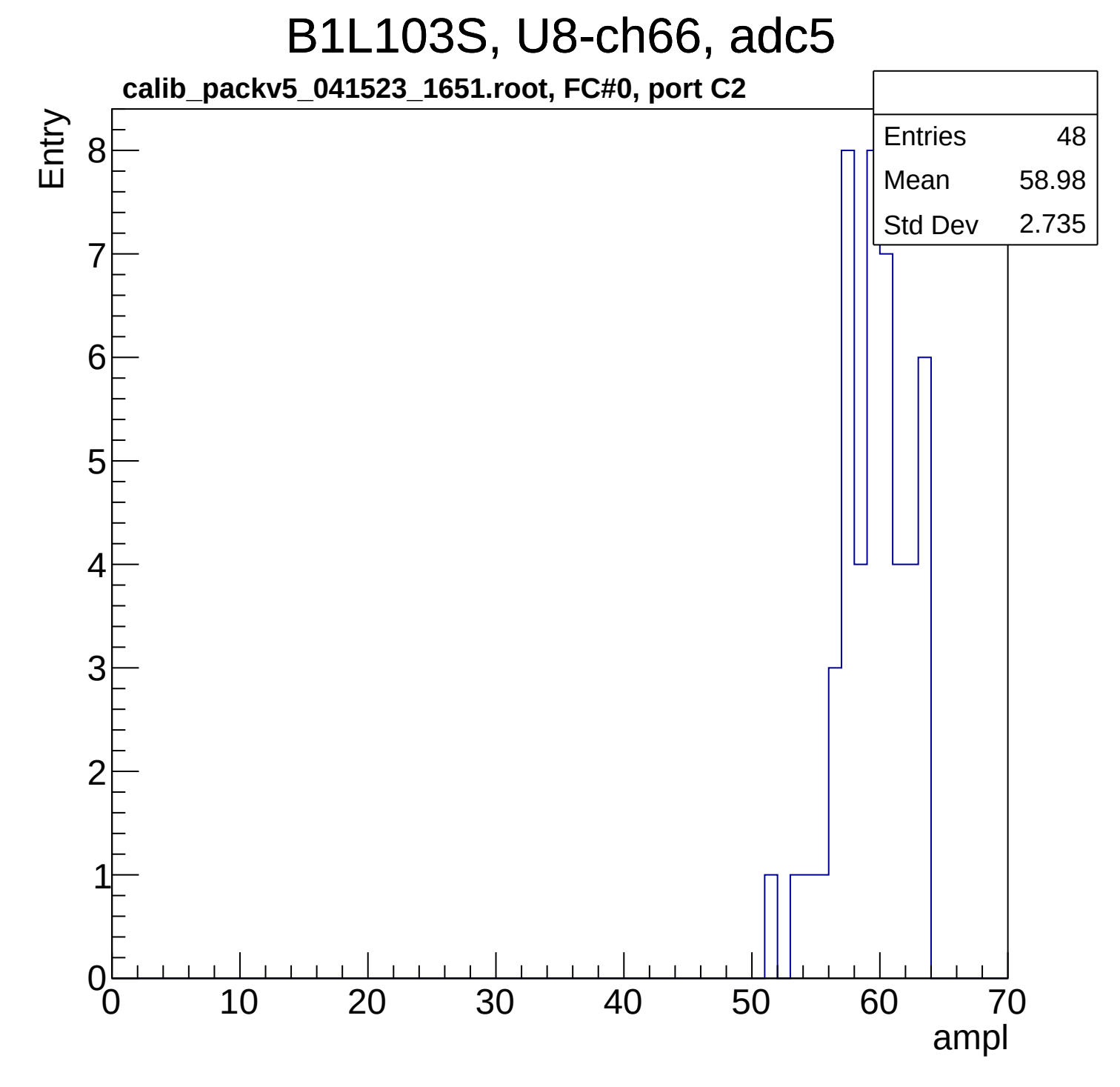
B1L103S, U8-ch66, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 58.98
Std Dev 2.735
Entry
ampl
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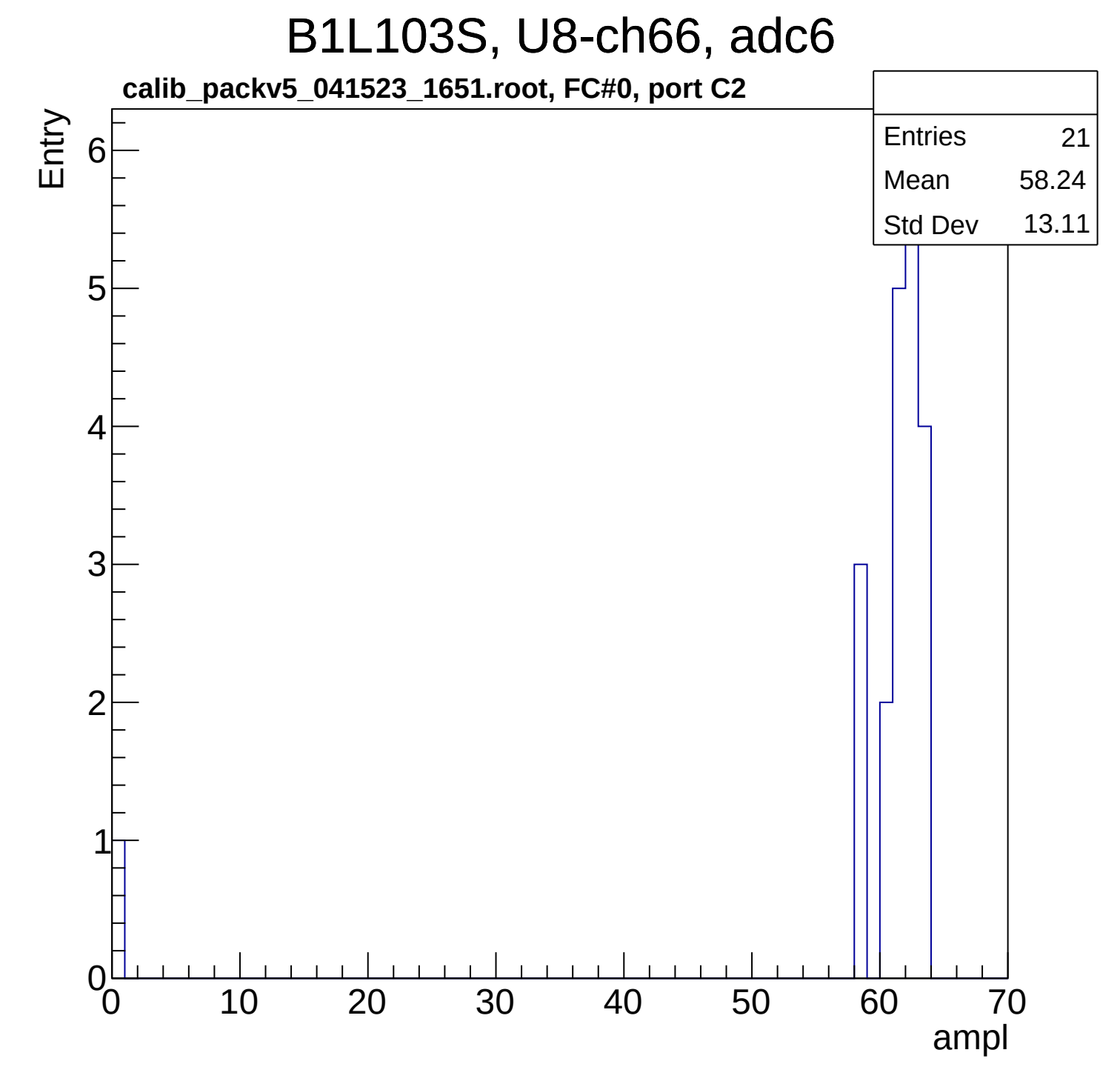
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch66, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 58.24
Std Dev 13.11
Entry
0
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2
3
4
5
6
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10
20
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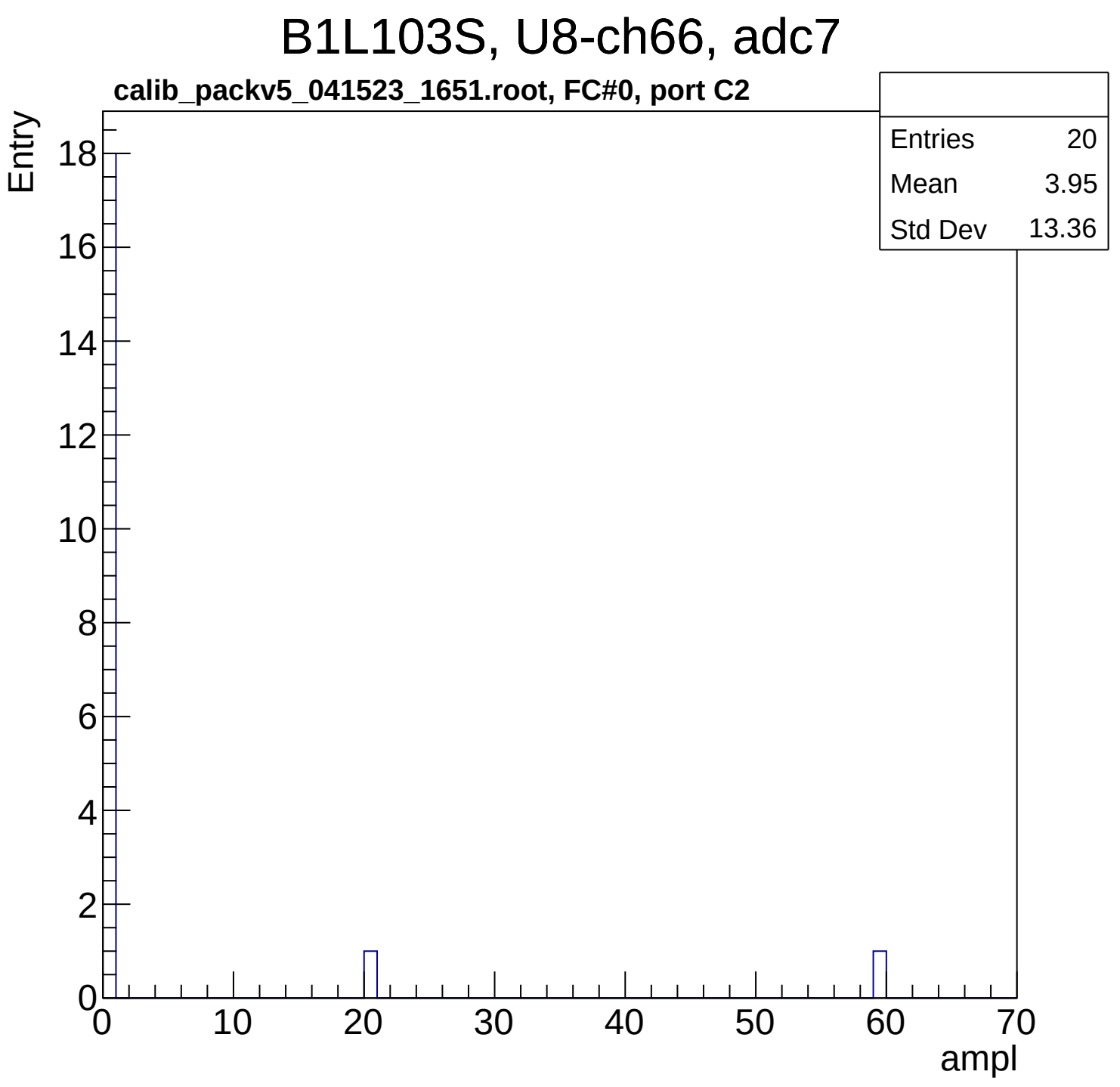
50
60
70
ampl


B1L103S, U8-ch66, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.95
Std Dev 13.36
Entry
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6
8
10
12
14
16
18
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20
30
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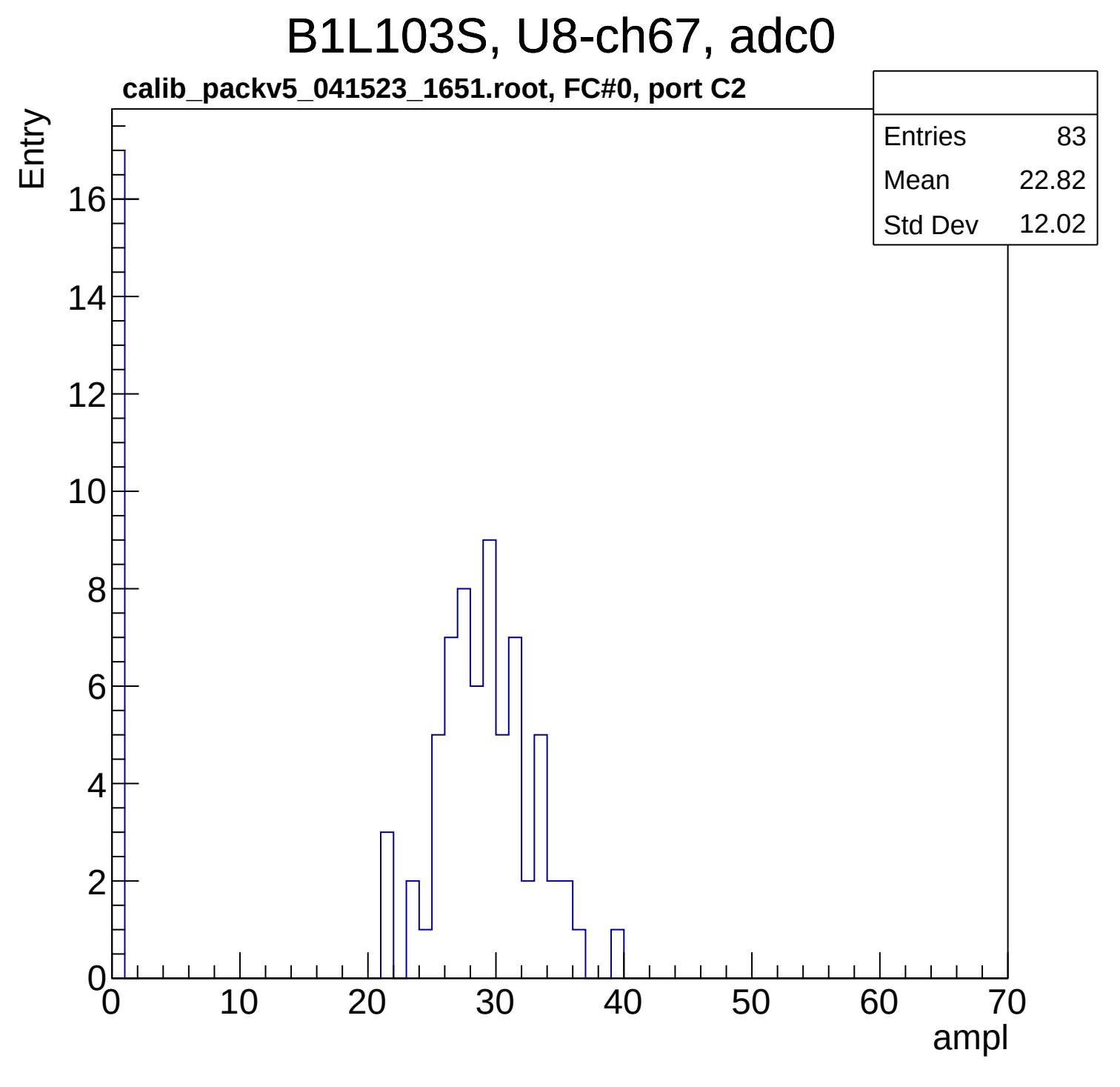
50
60
70
ampl


B1L103S, U8-ch67, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 22.82
Std Dev 12.02
Entry
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4
6
8
10
12
14
16
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10
20
30
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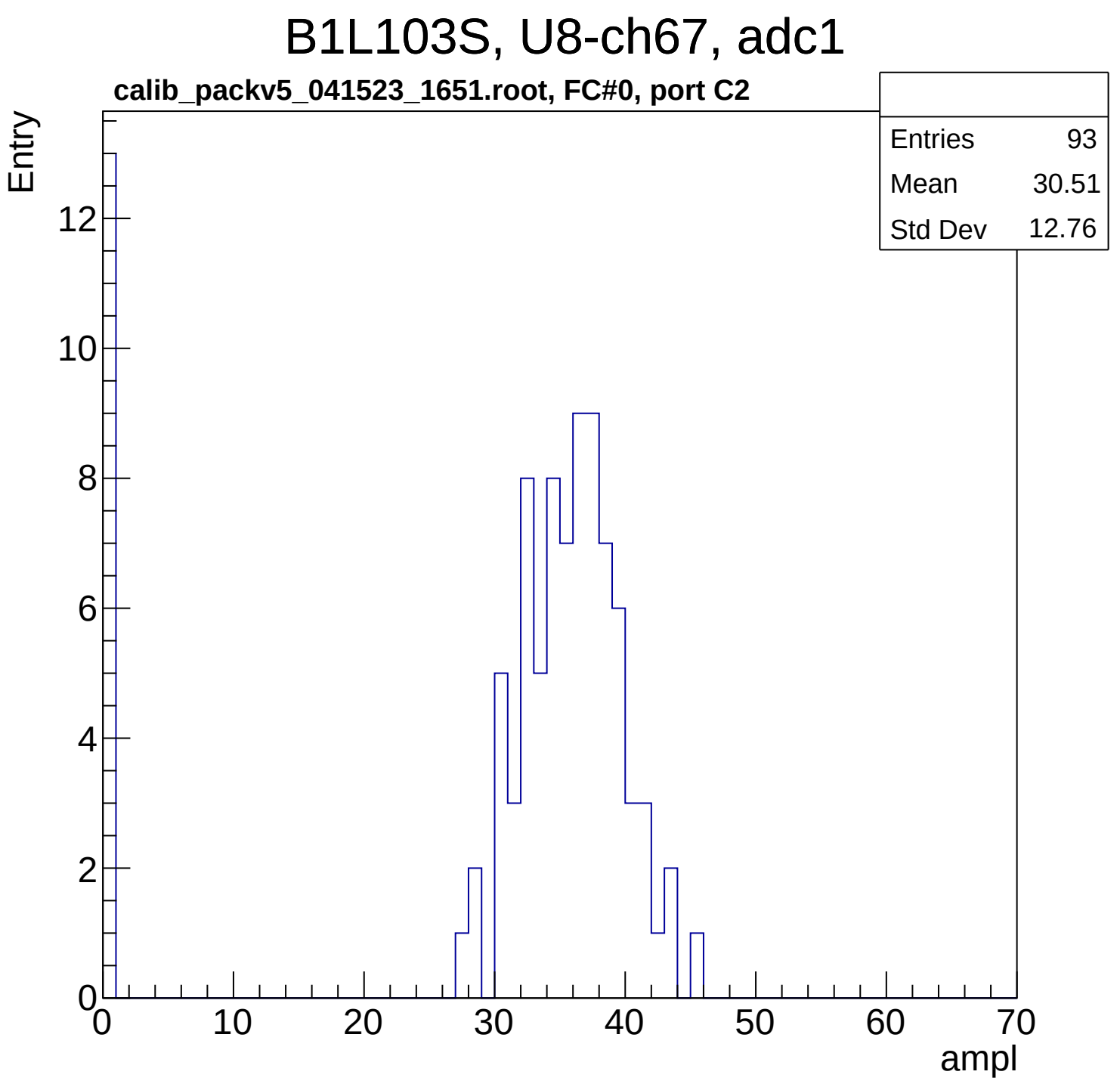
50
60
70
ampl


B1L103S, U8-ch67, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 30.51
Std Dev 12.76
Entry
0
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4
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8
10
12
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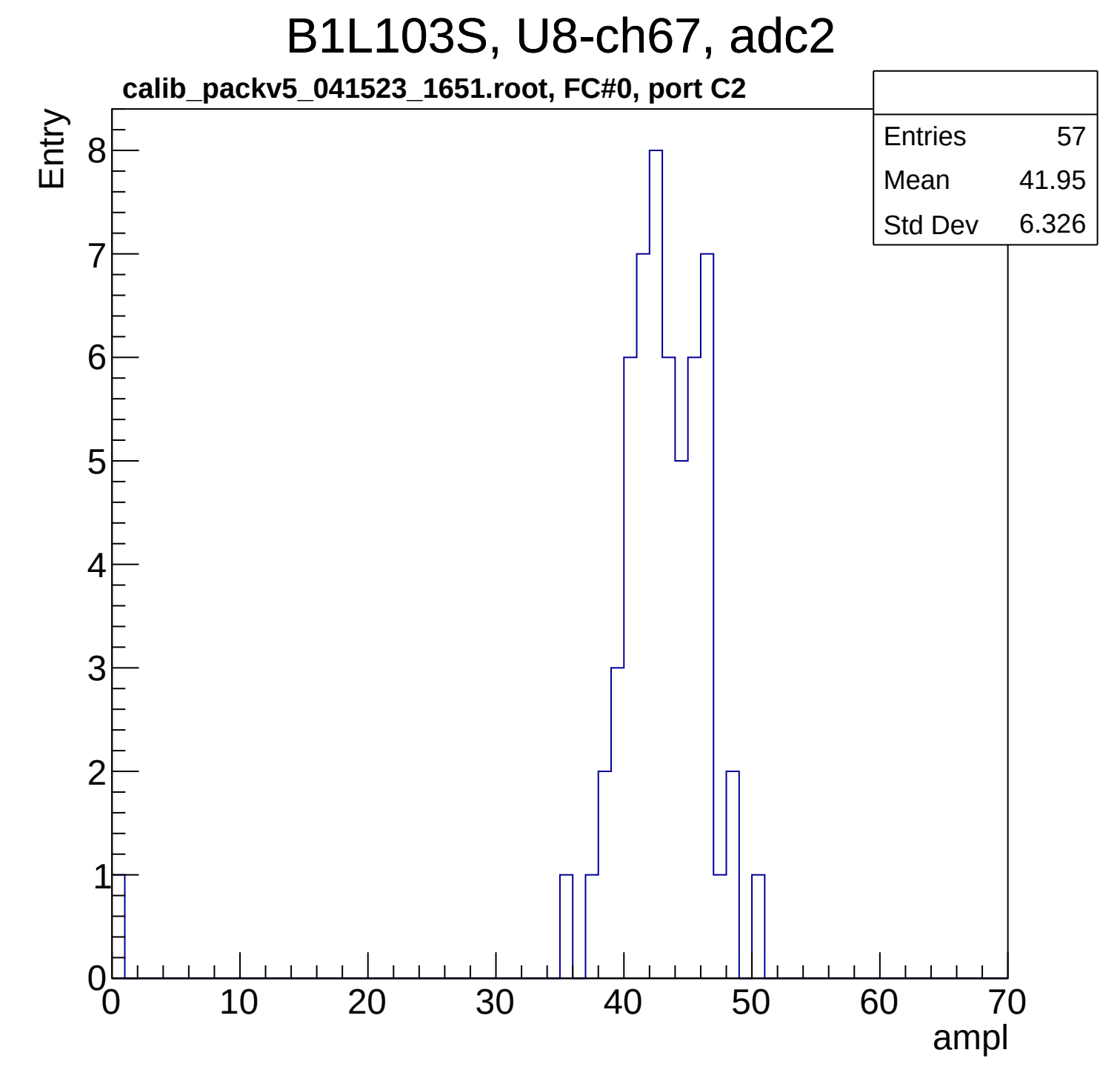
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch67, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 41.95
Std Dev 6.326
Entry
ampl
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2
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4
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6
7
8
0
10
20
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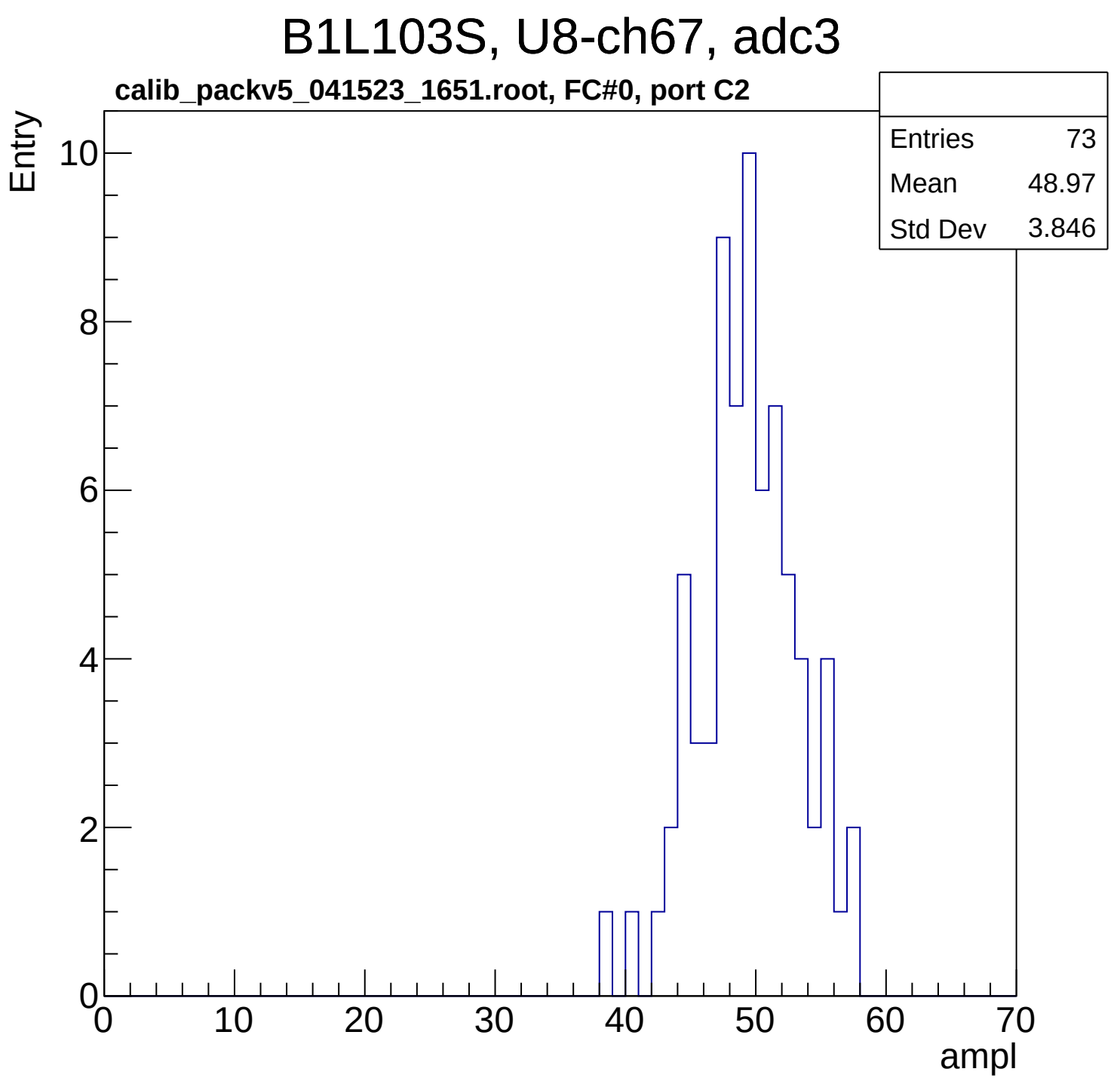
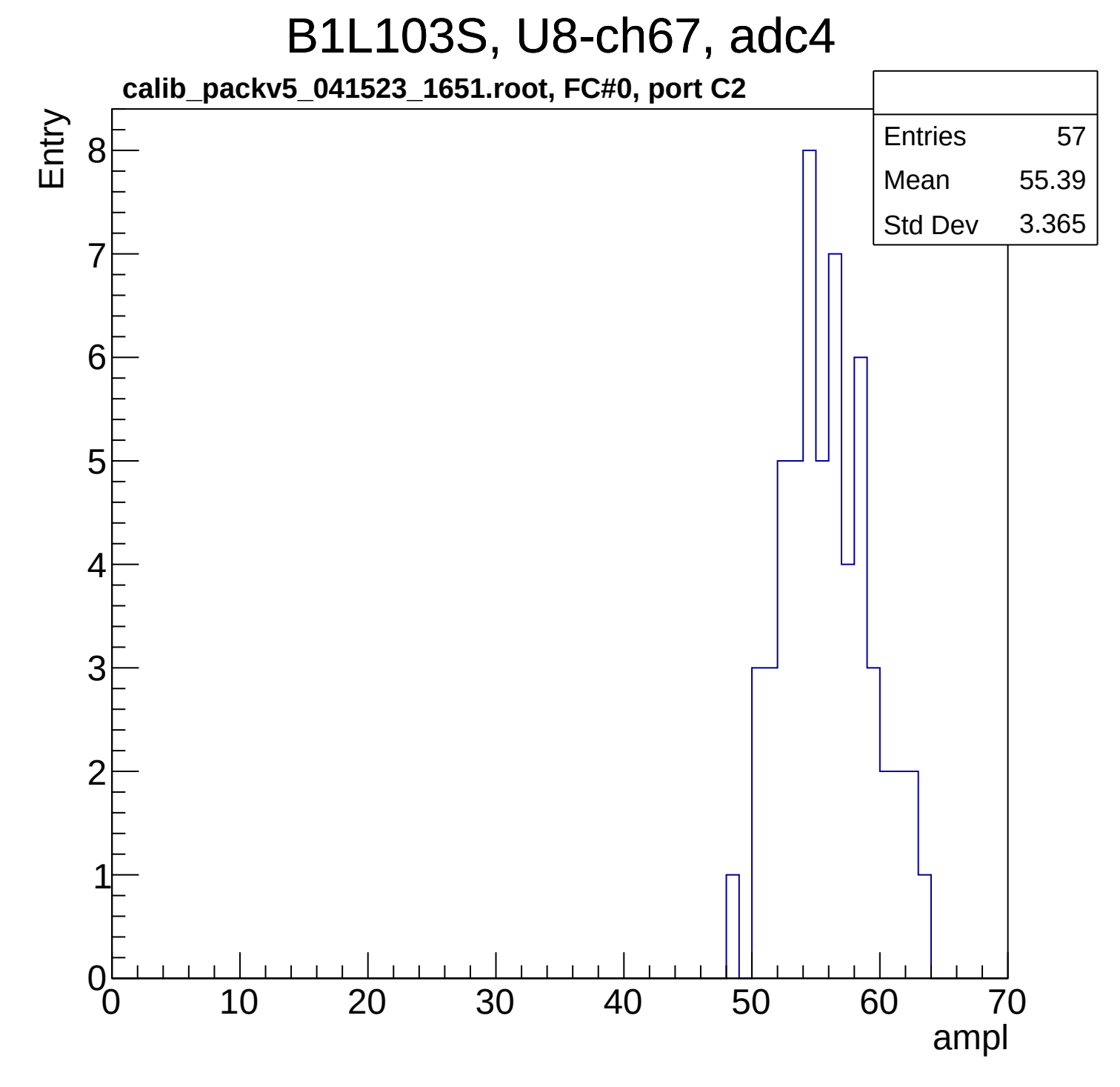
40
50
60
70


B1L103S, U8-ch67, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 48.97
Std Dev 3.846
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U8-ch67, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 55.39
Std Dev 3.365
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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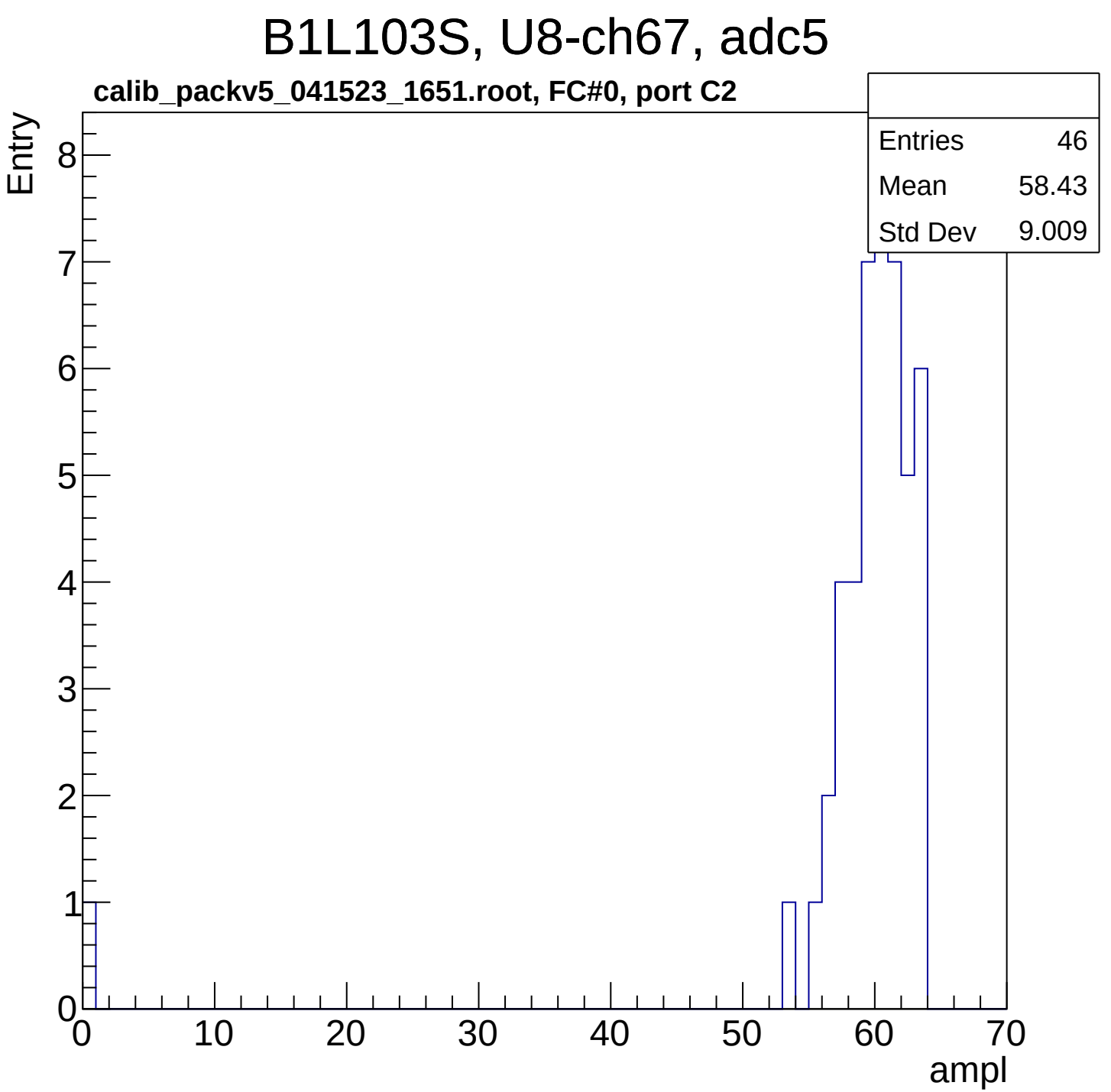
B1L103S, U8-ch67, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 58.43
Std Dev 9.009
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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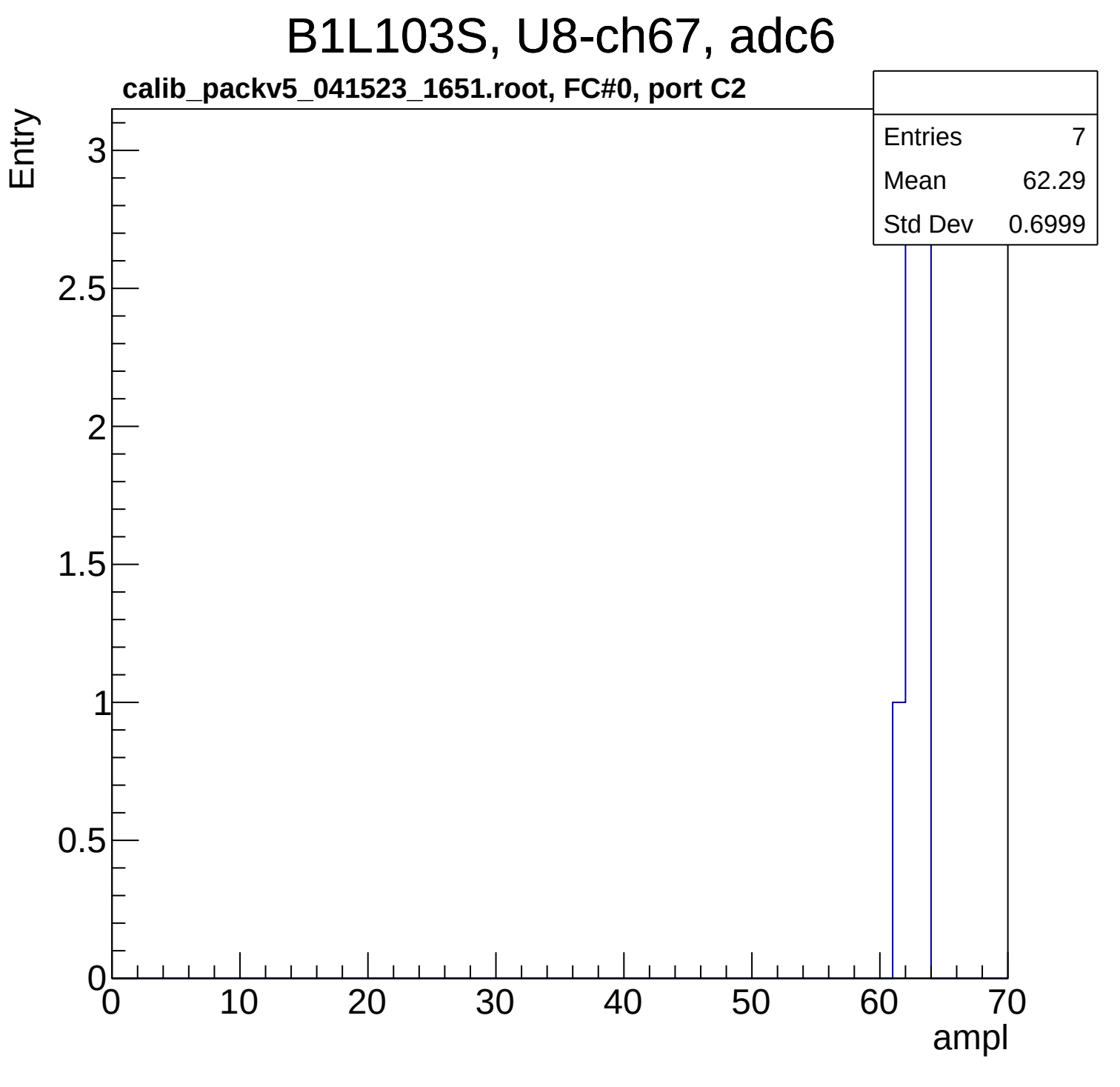
B1L103S, U8-ch67, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 62.29
Std Dev 0.6999
Entry
ampl
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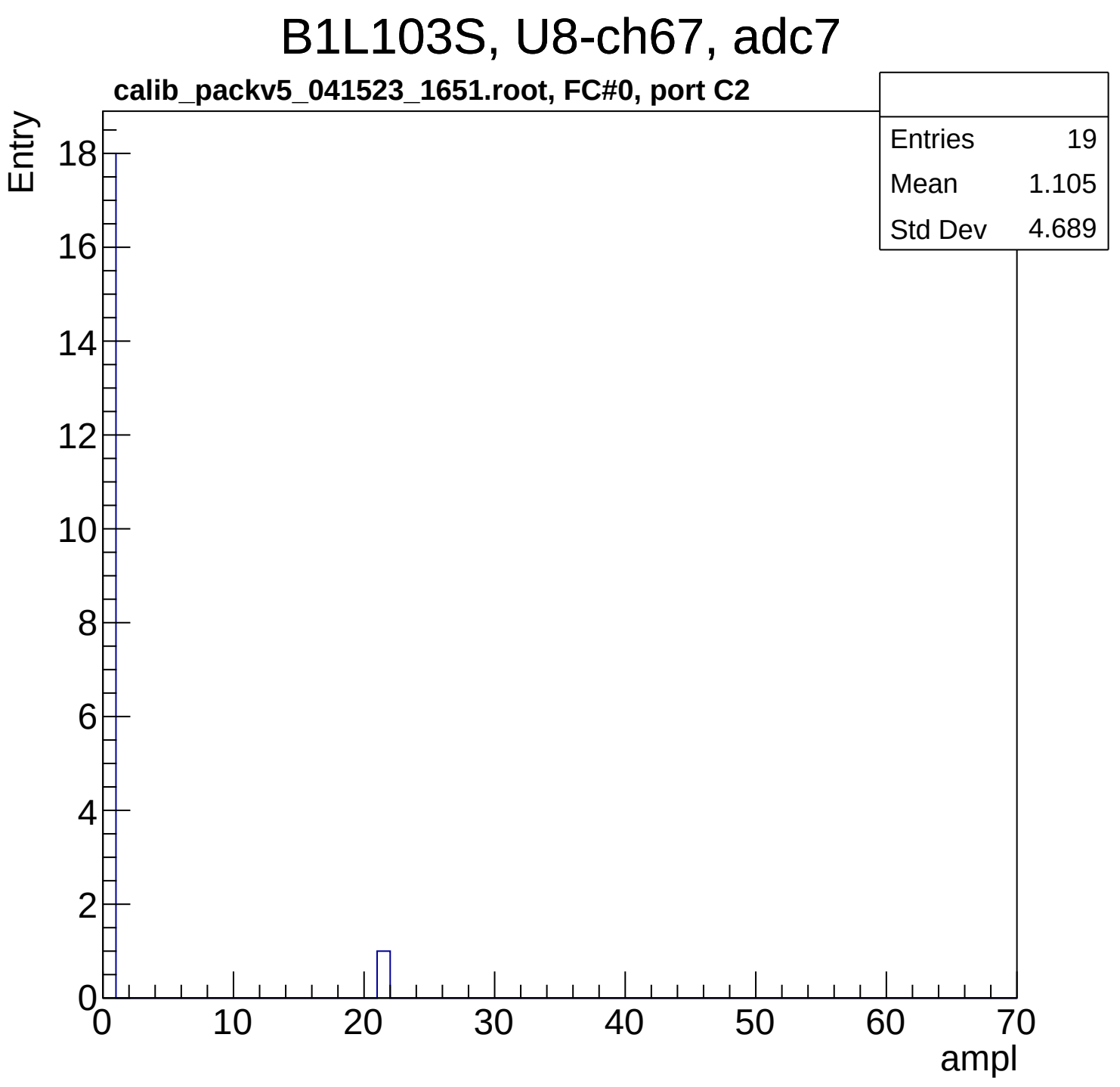
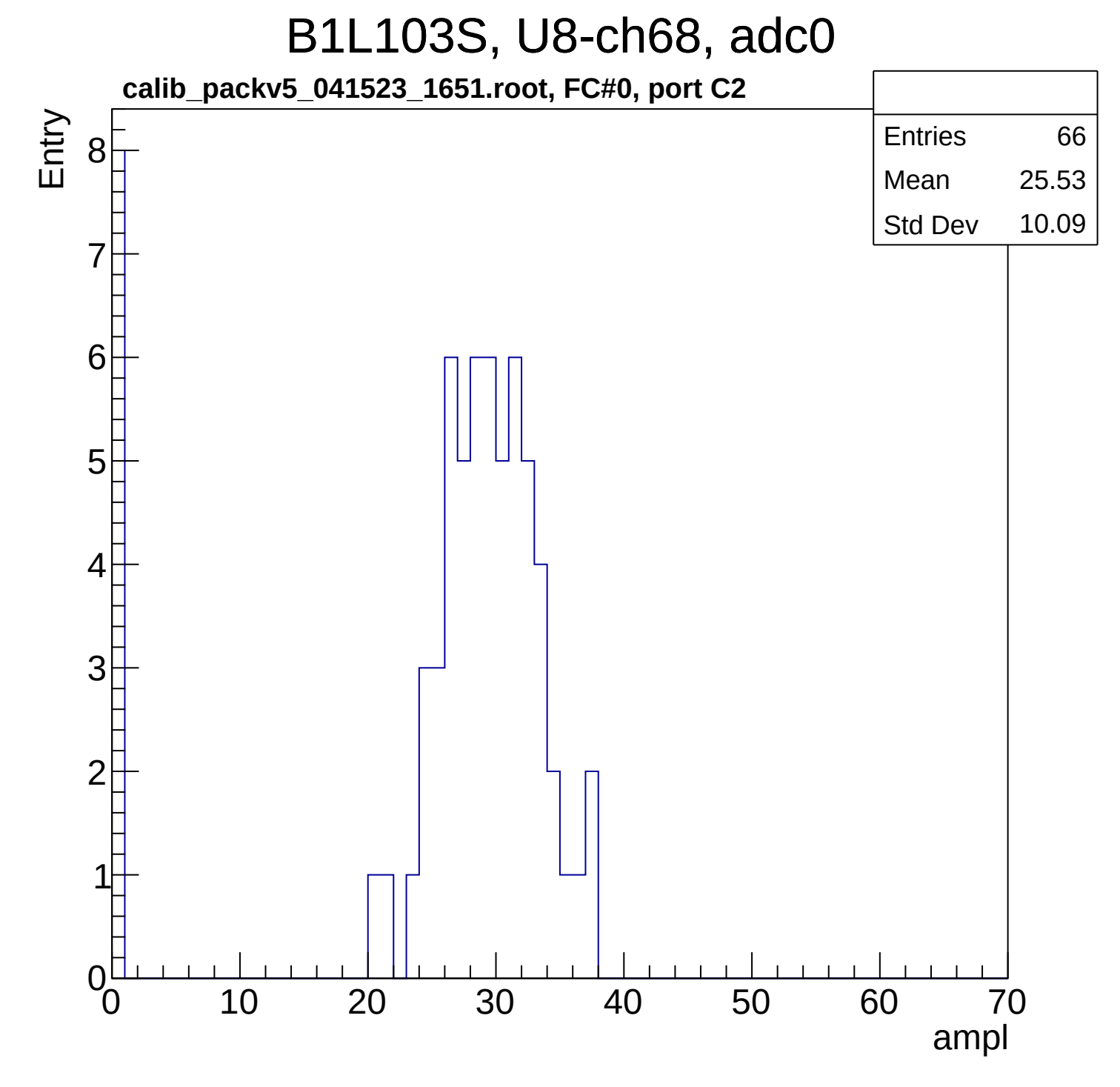
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U8-ch67, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.105
Std Dev 4.689
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch68, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 25.53
Std Dev 10.09
Entry
ampl
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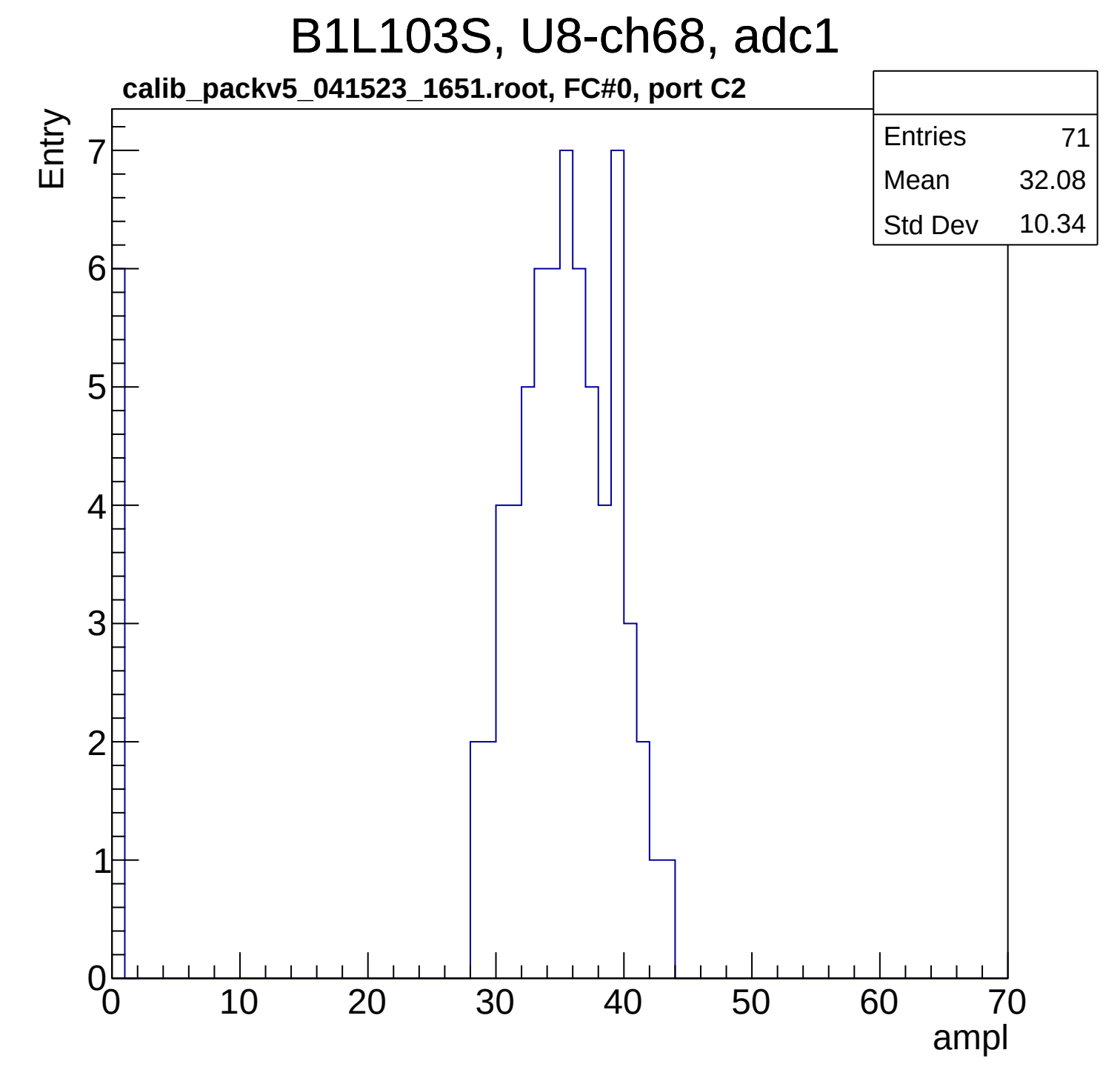
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch68, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 32.08
Std Dev 10.34
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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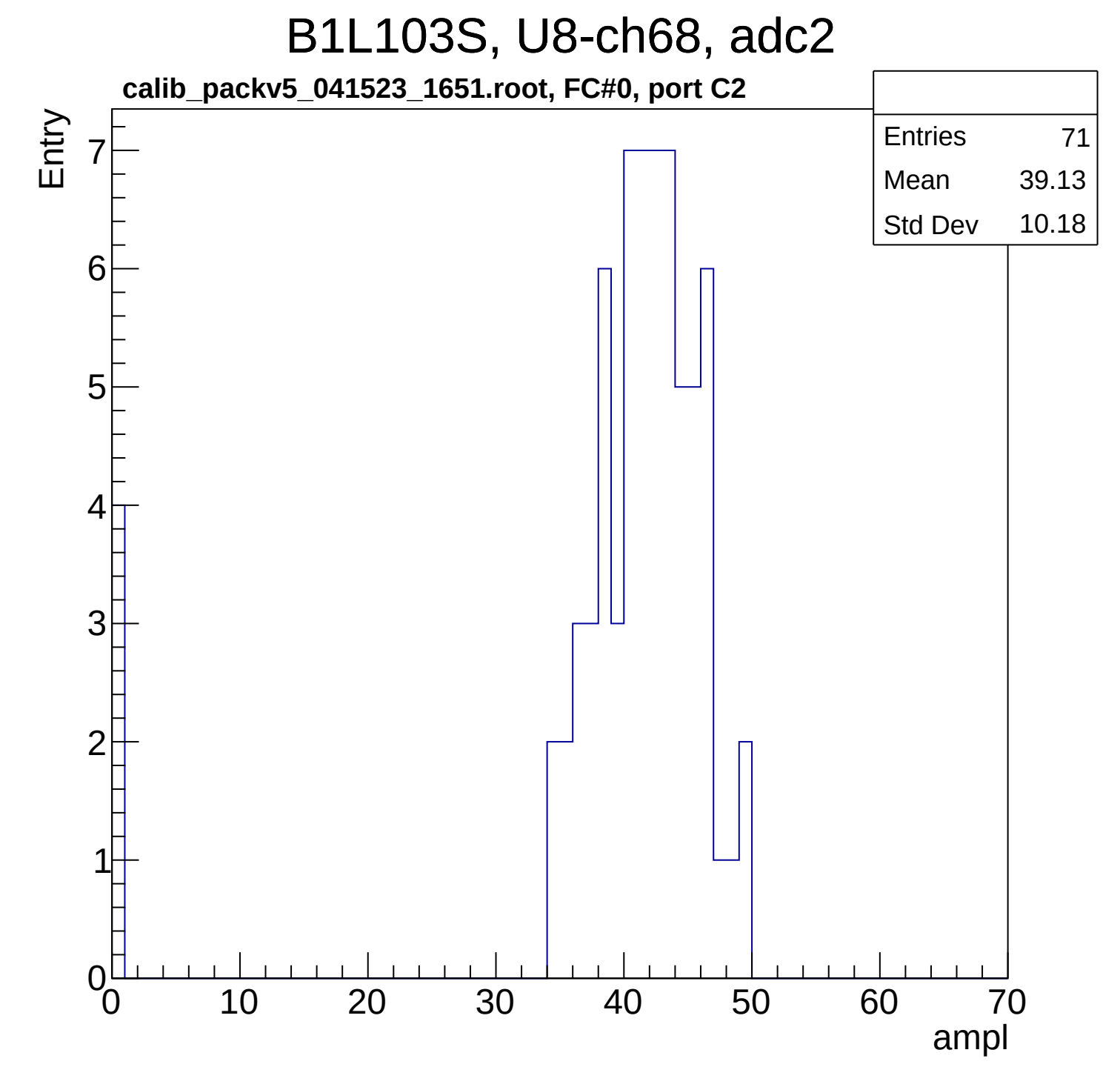
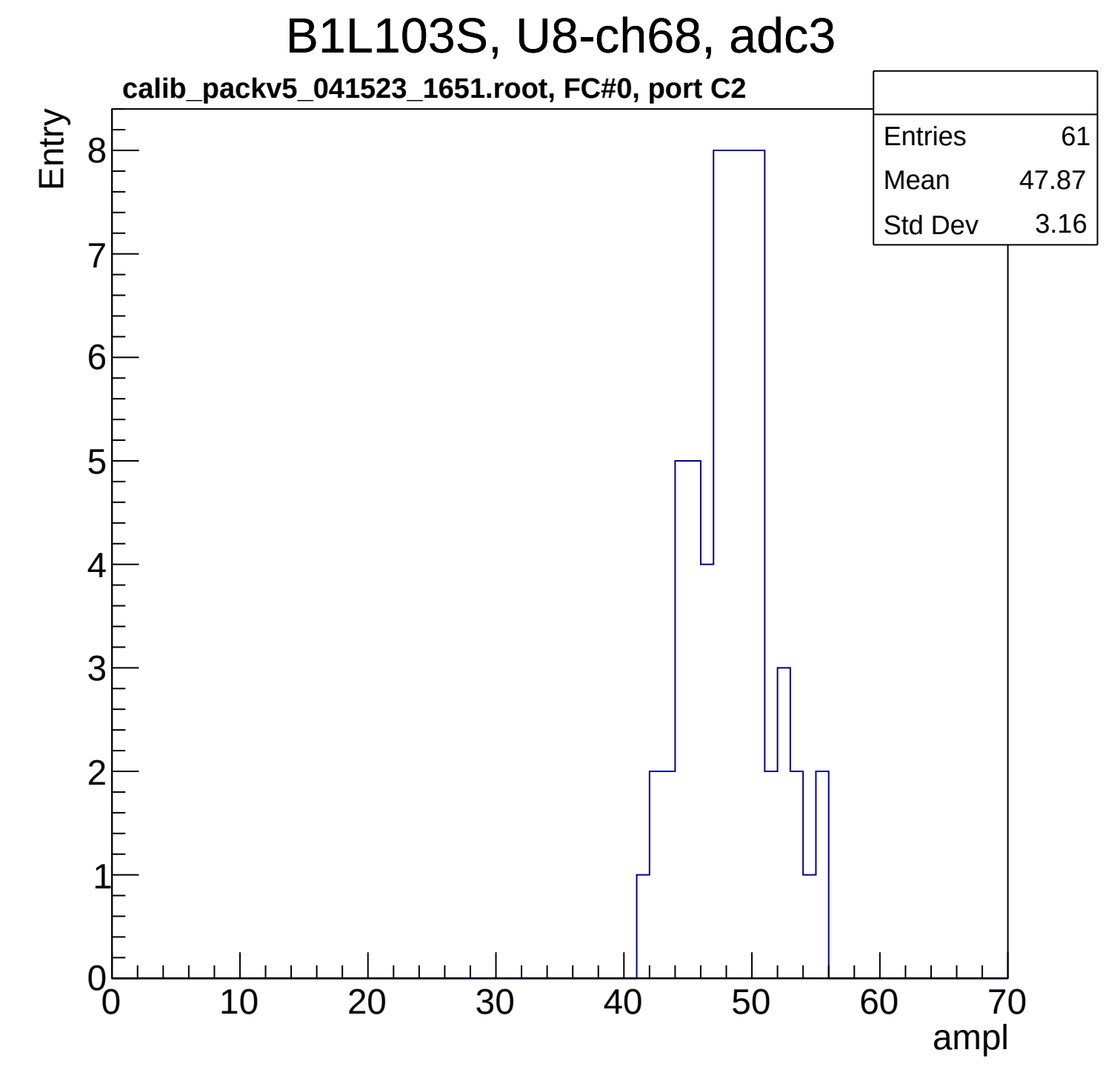

B1L103S, U8-ch68, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 39.13
Std Dev 10.18
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U8-ch68, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 47.87
Std Dev 3.16
Entry
ampl
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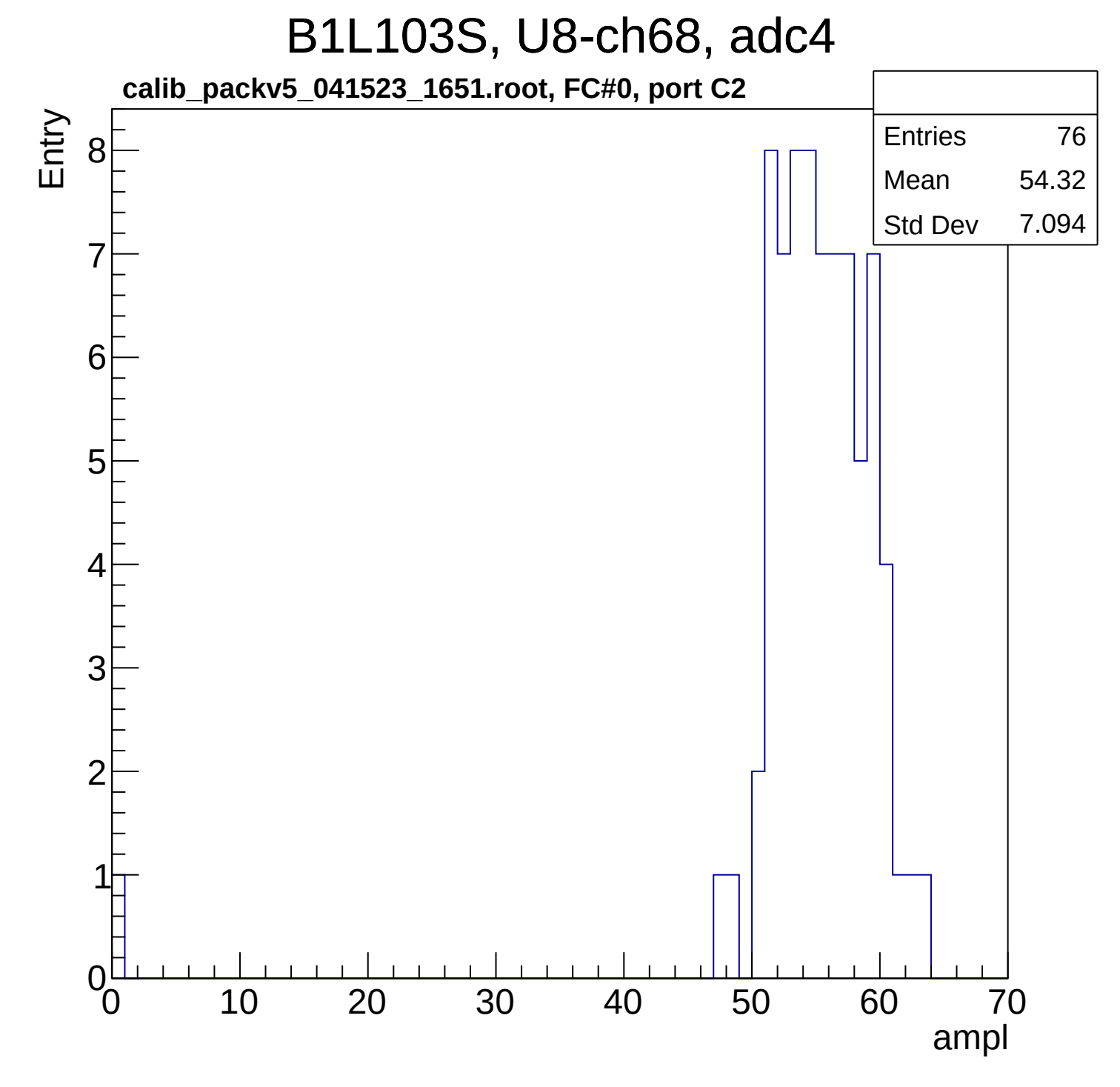
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch68, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 54.32
Std Dev 7.094
Entry
ampl
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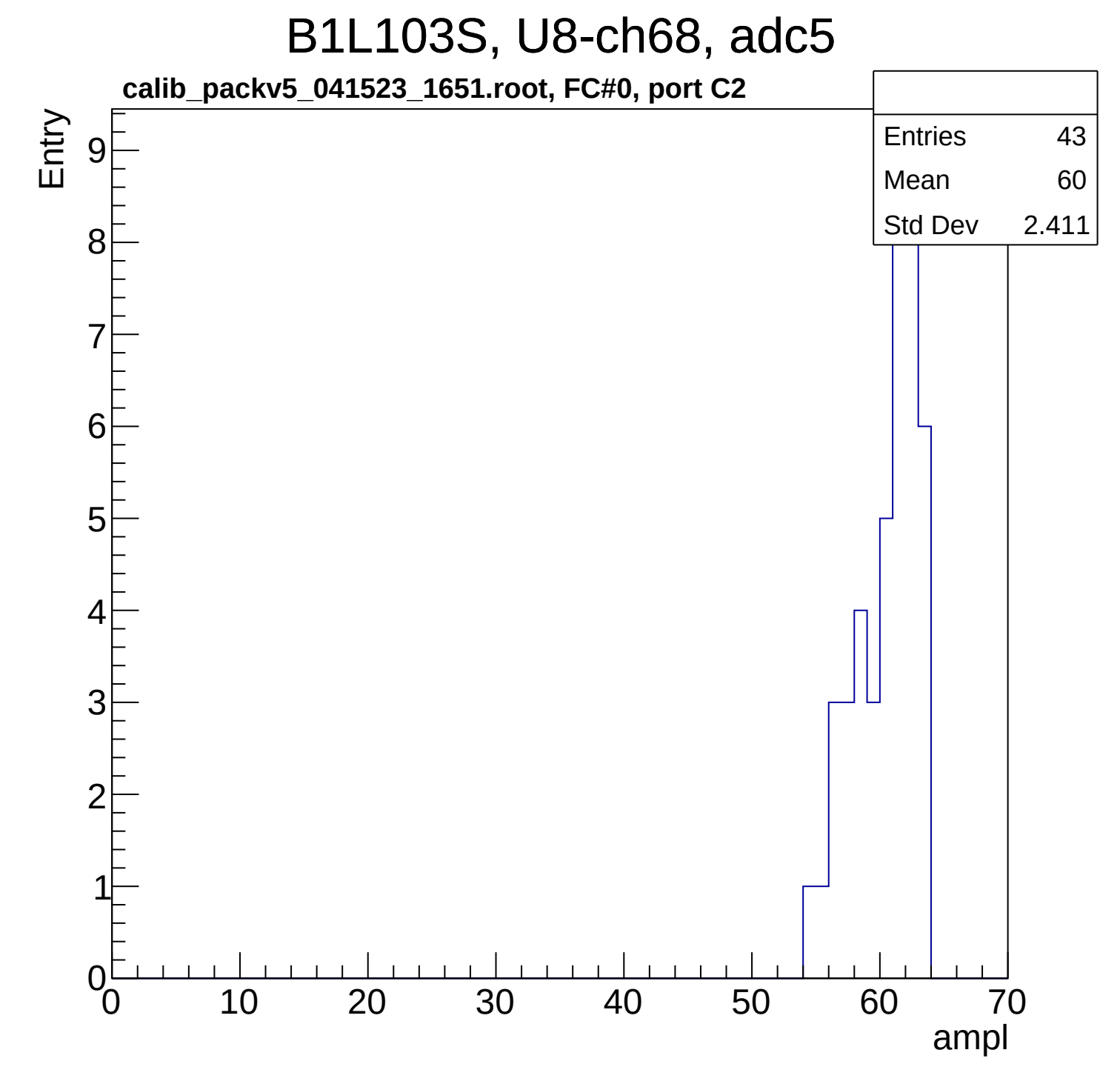
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch68, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 60
Std Dev 2.411
Entry
ampl
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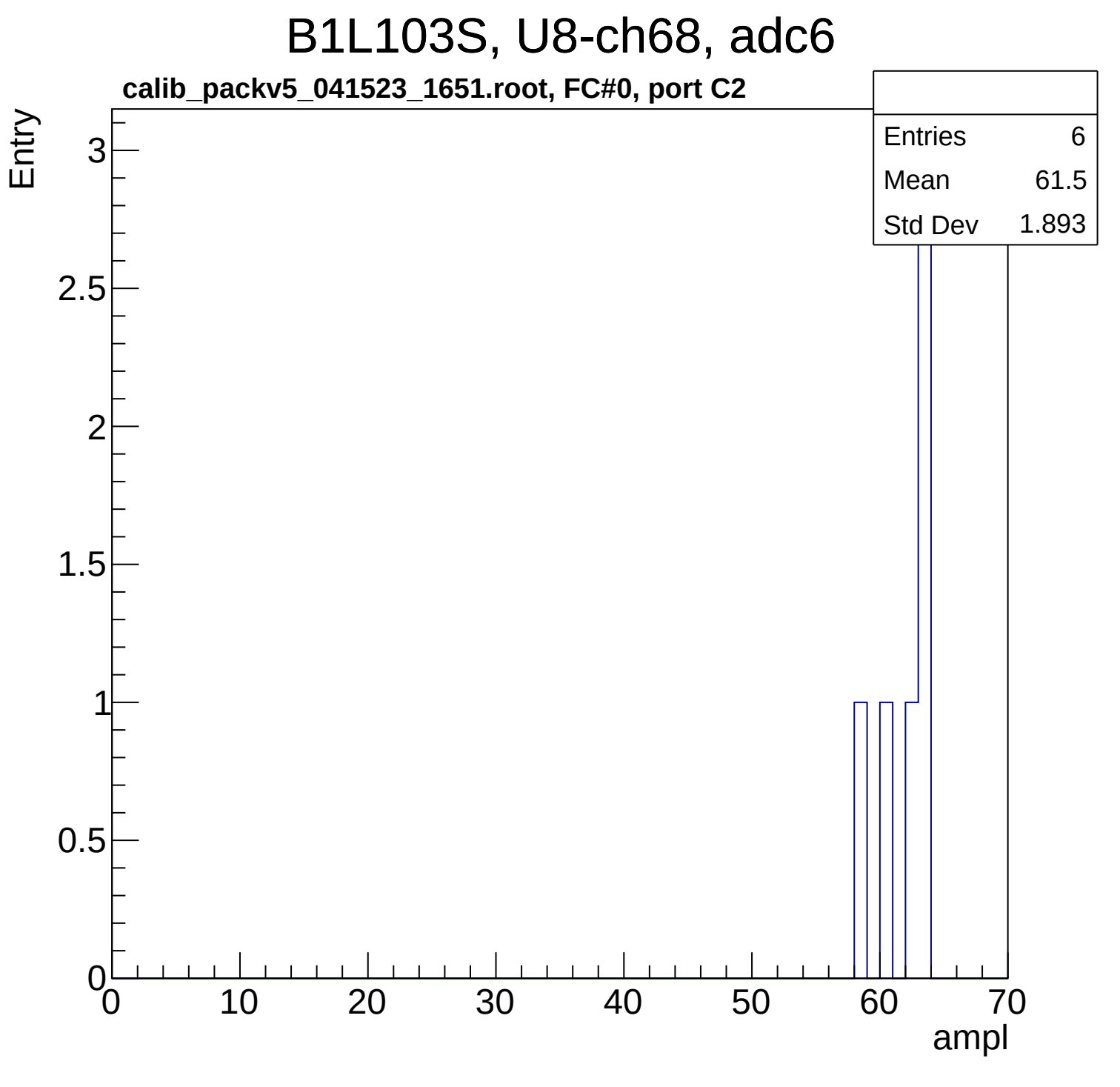
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U8-ch68, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 61.5
Std Dev 1.893
Entry
ampl
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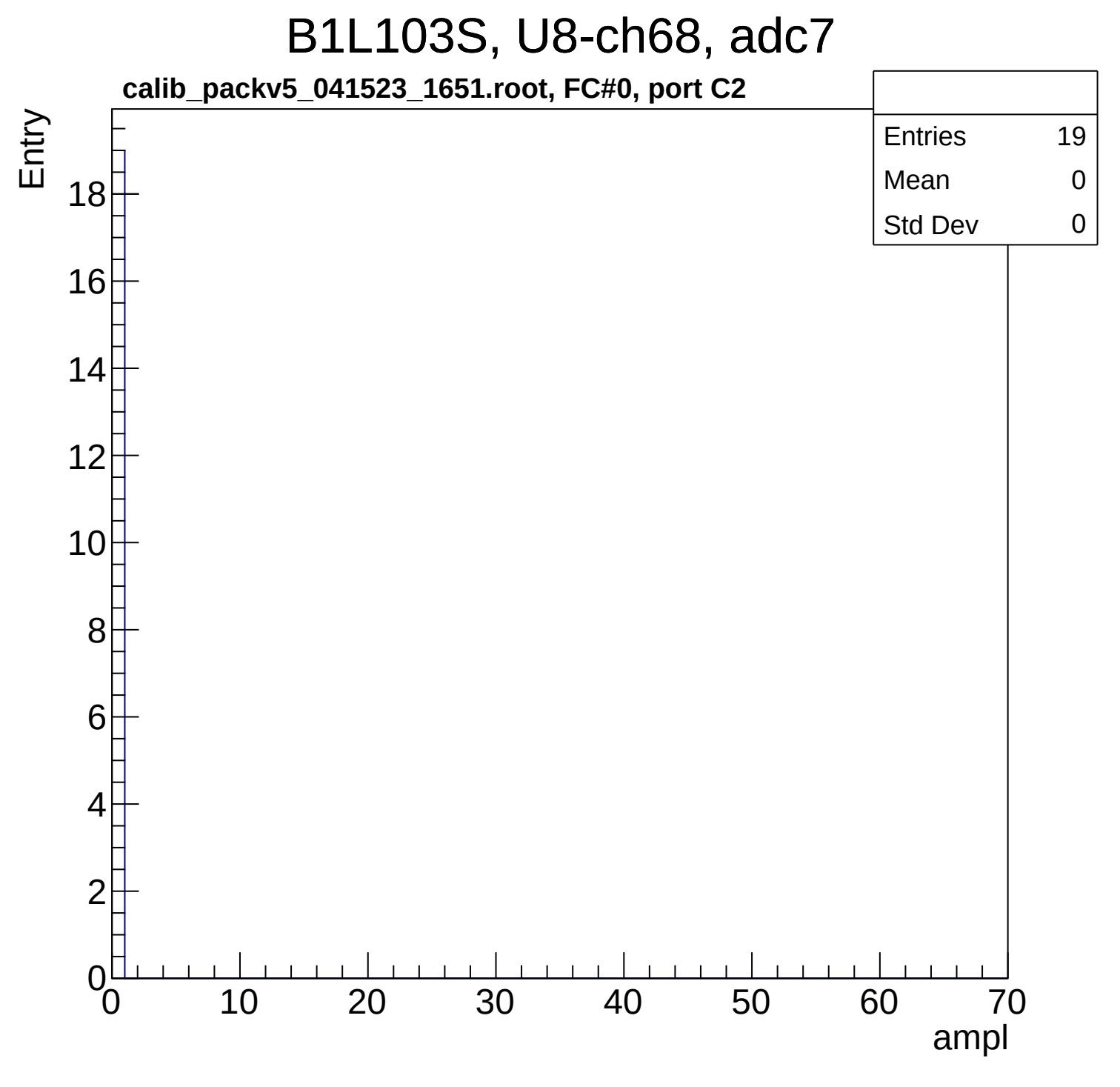
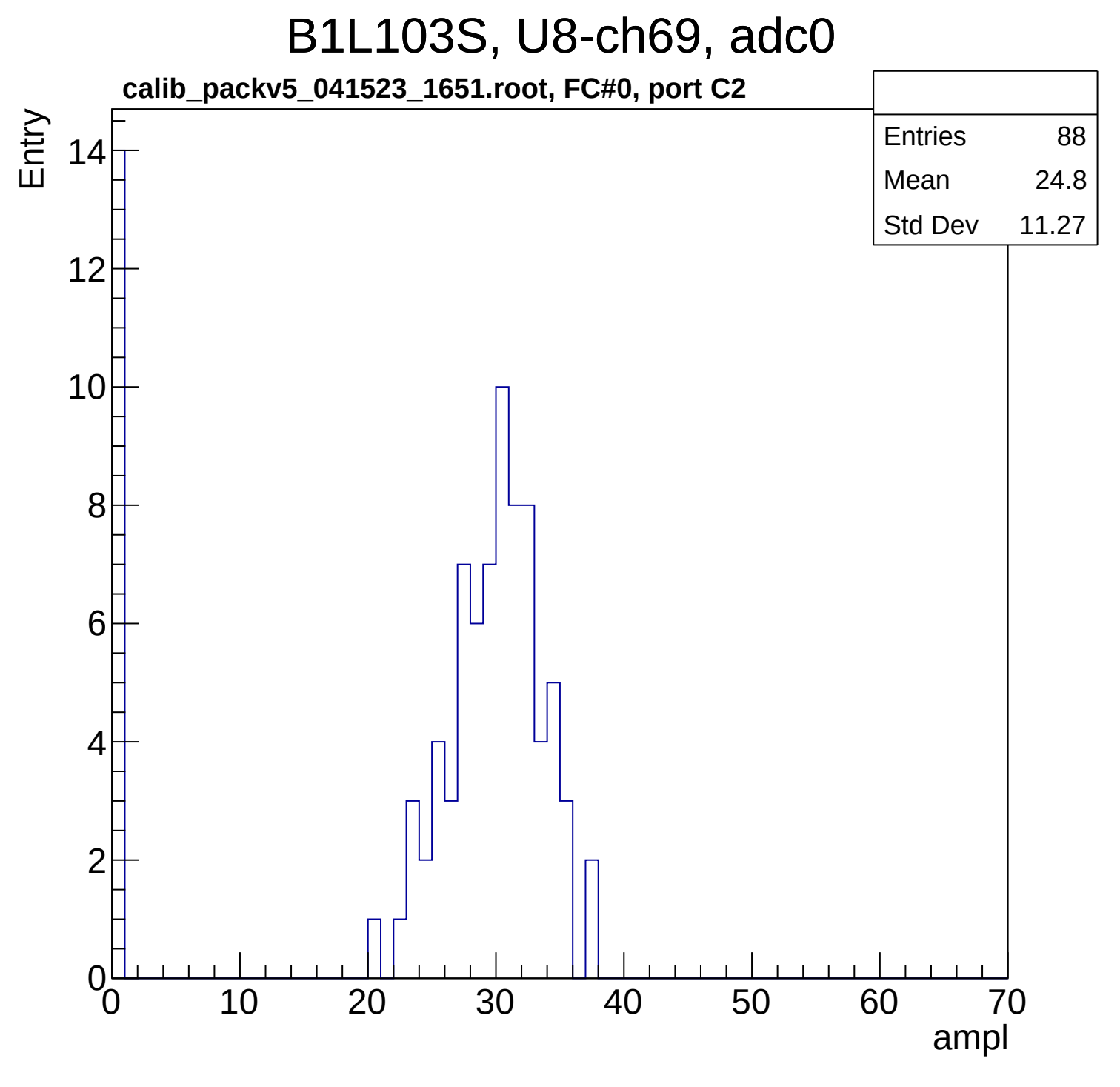
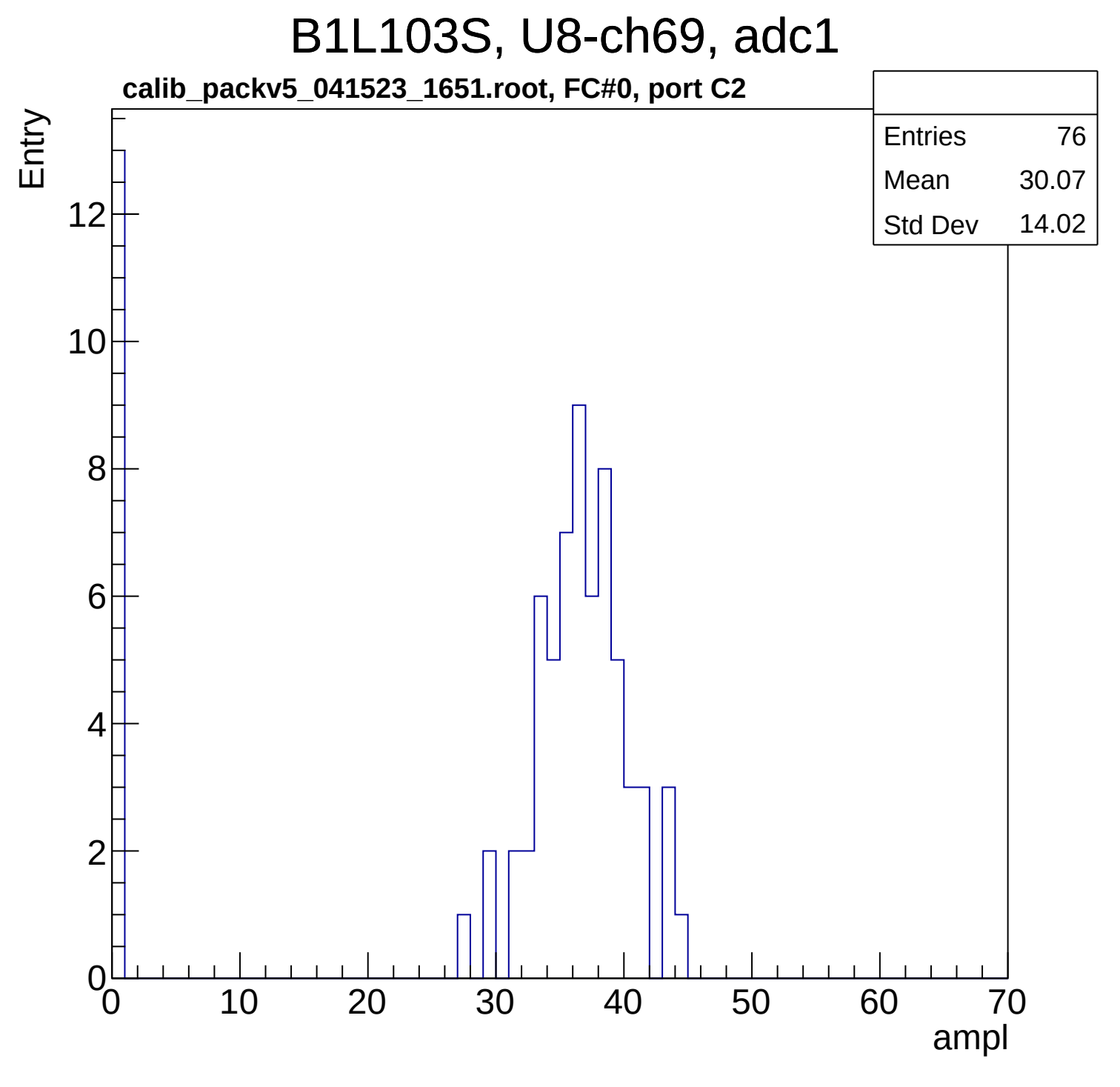
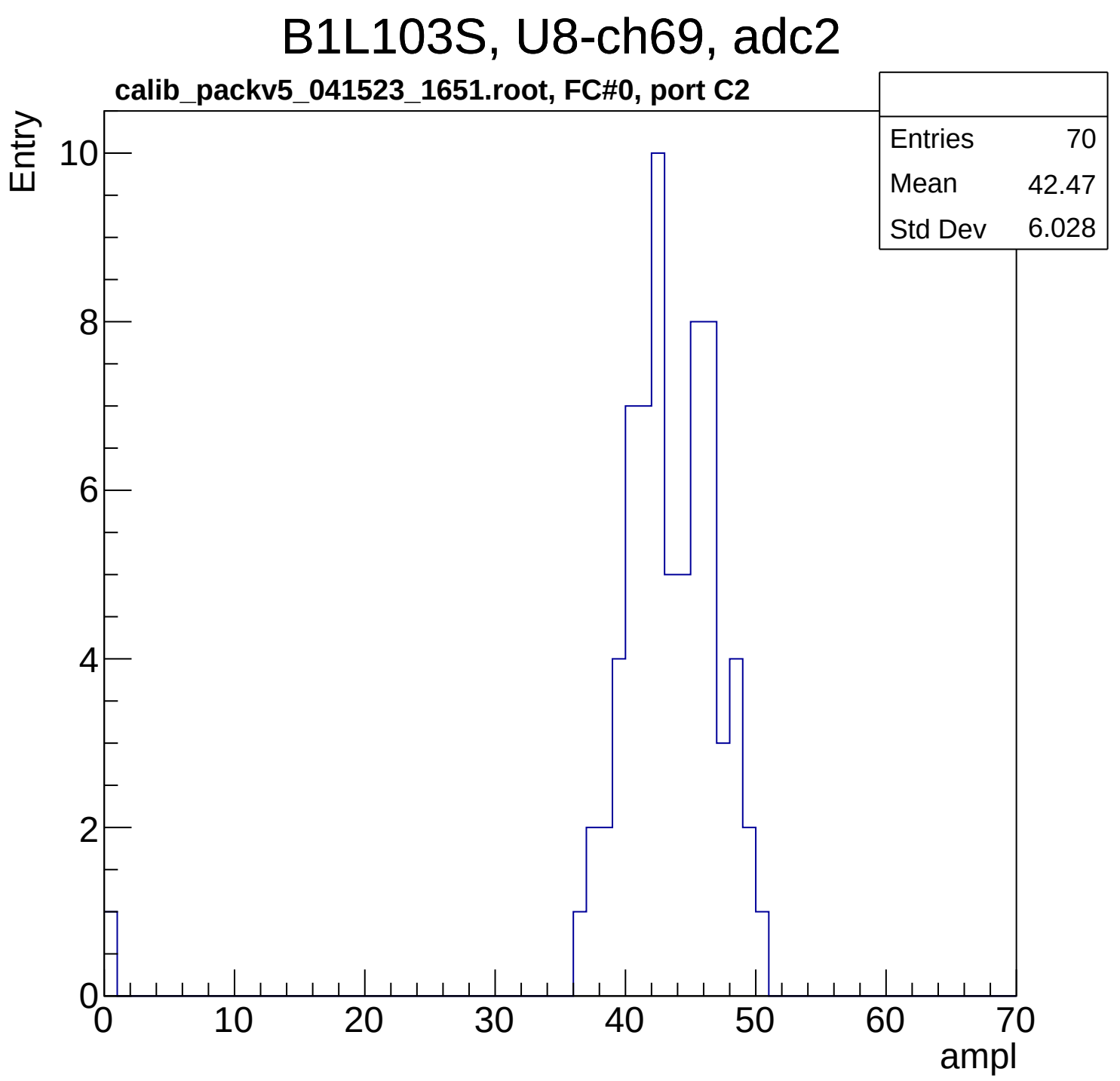
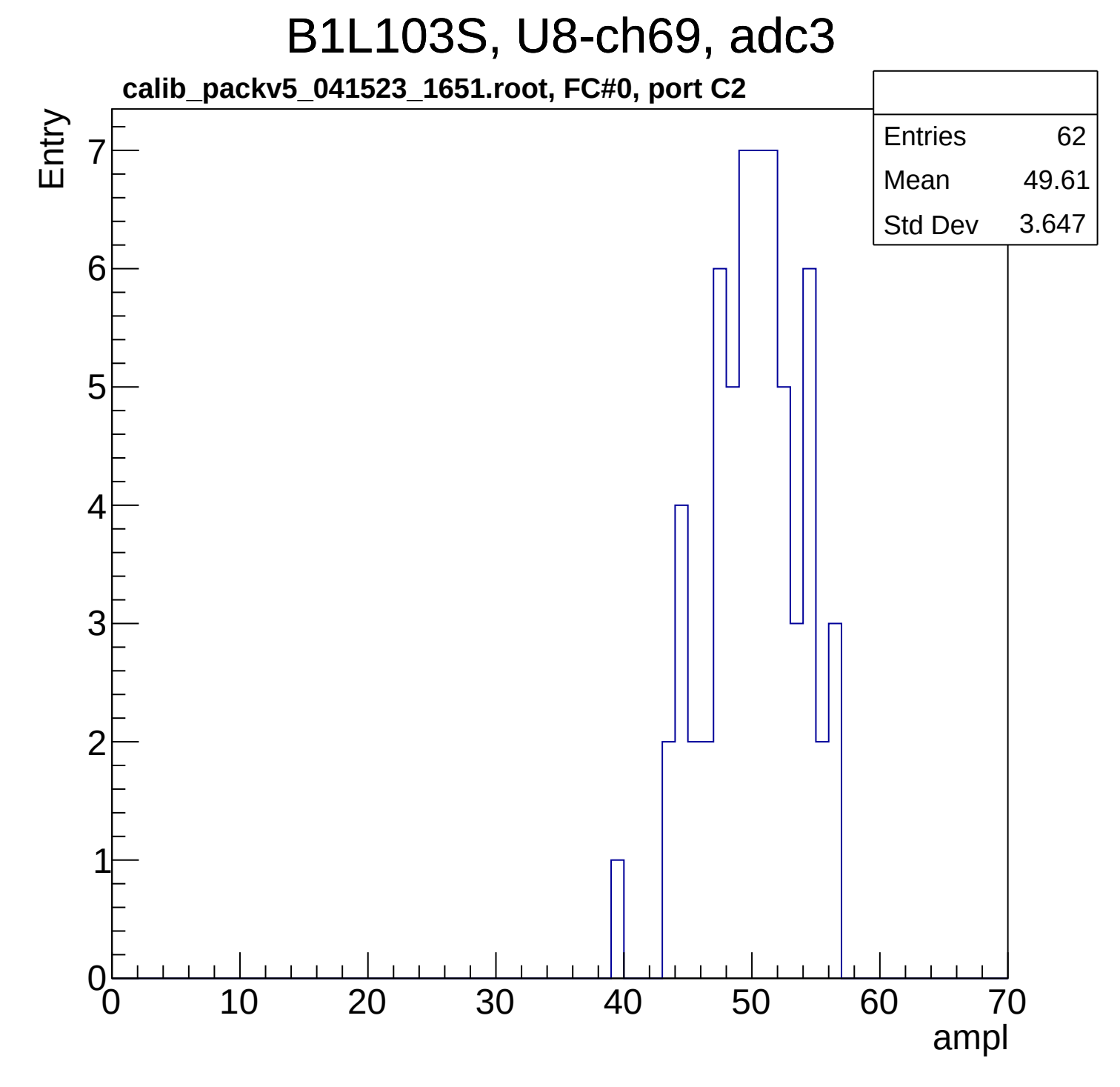
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

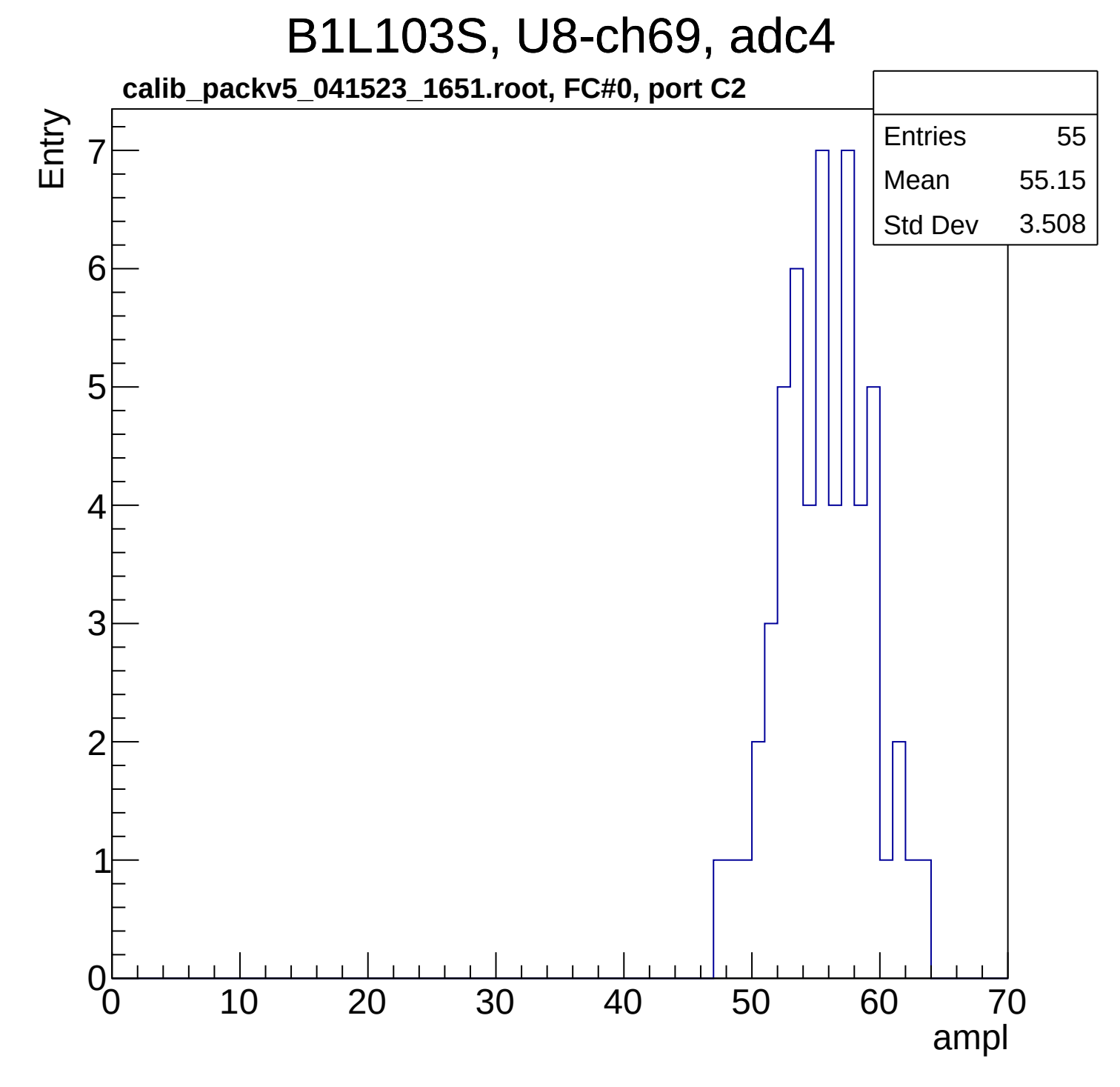

B1L103S, U8-ch68, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch69, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 24.8
Std Dev 11.27
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U8-ch69, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 30.07
Std Dev 14.02
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U8-ch69, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 42.47
Std Dev 6.028
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U8-ch69, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 49.61
Std Dev 3.647
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U8-ch69, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 55.15
Std Dev 3.508
Entry
ampl
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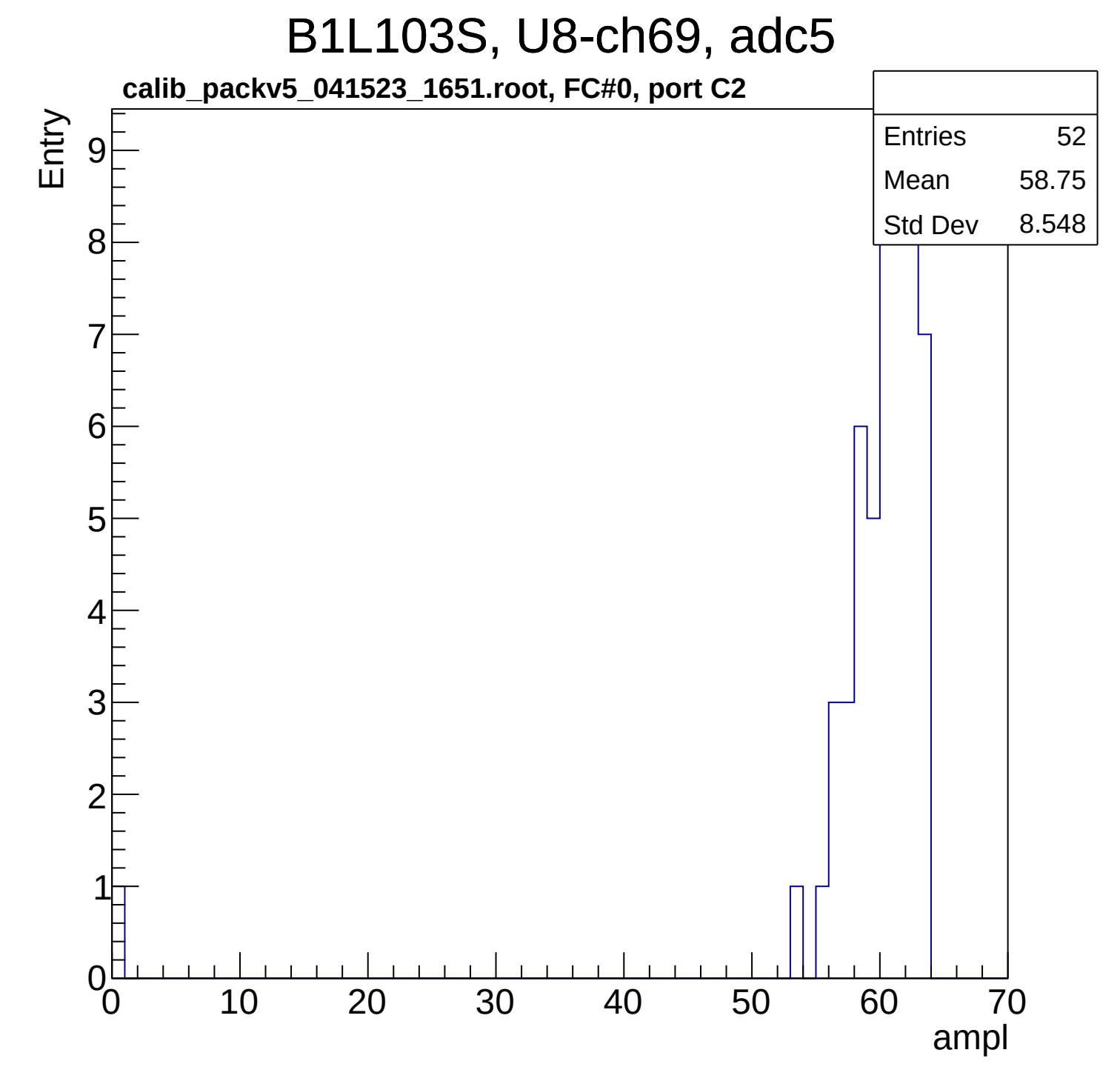
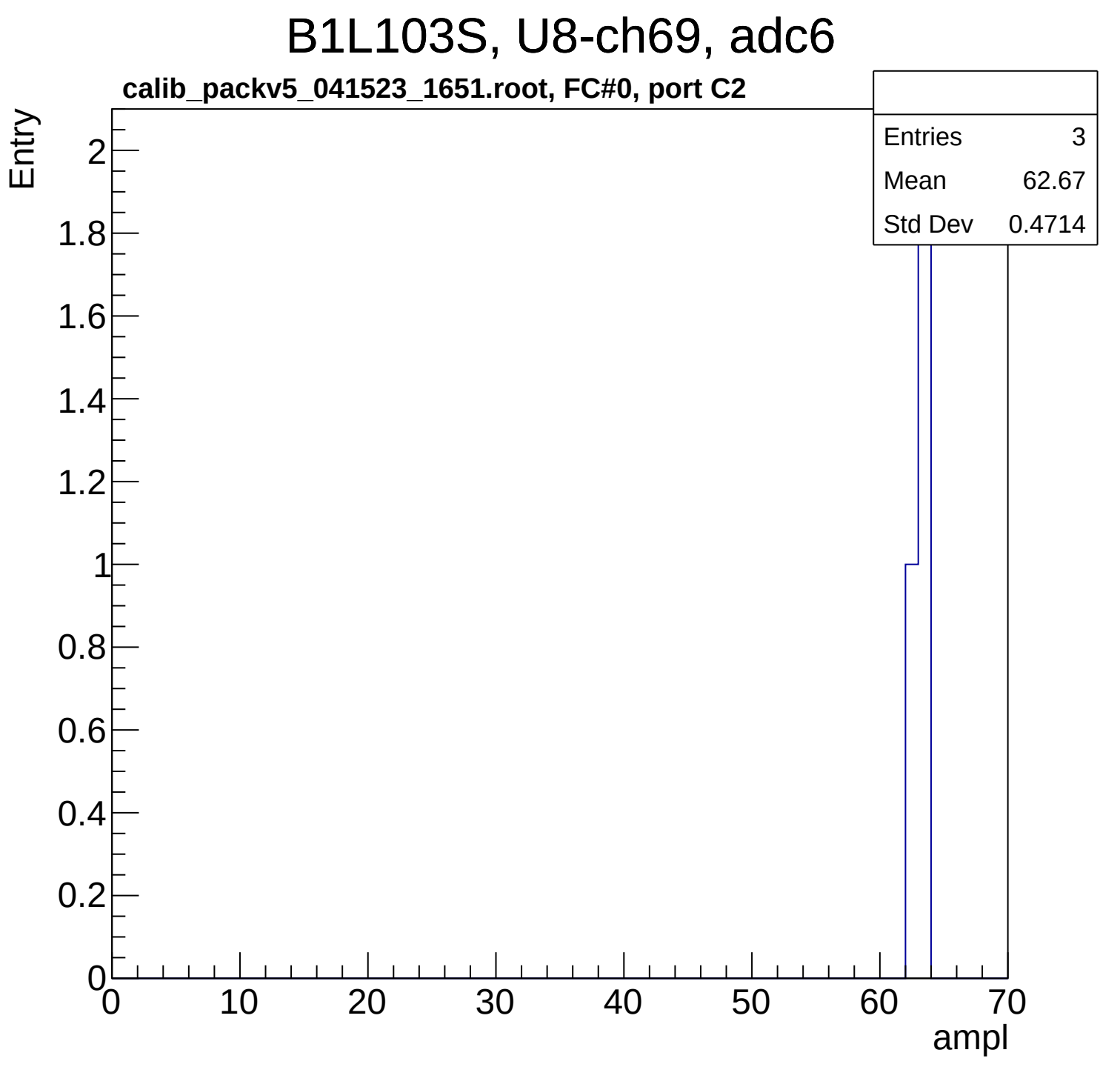
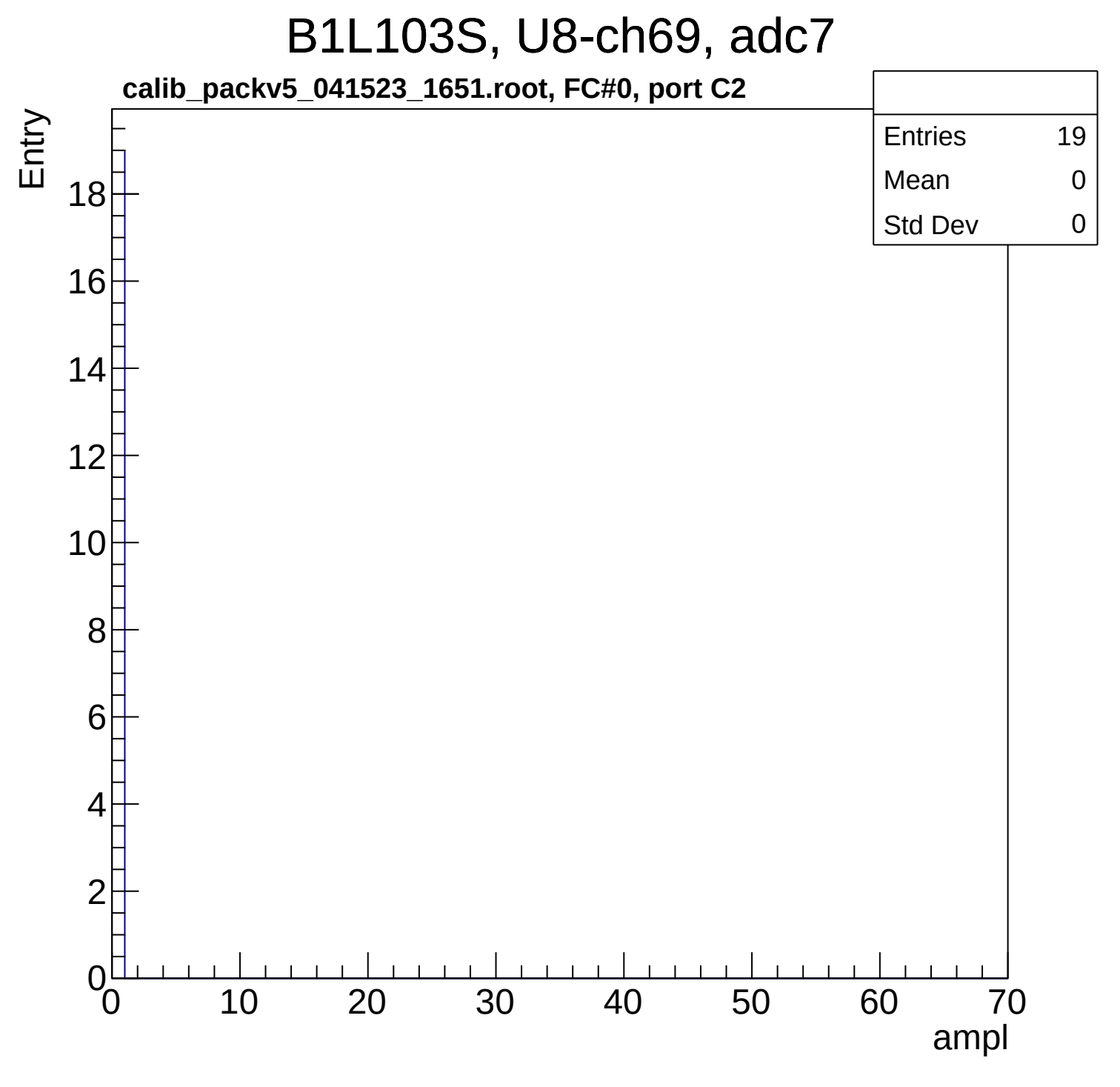
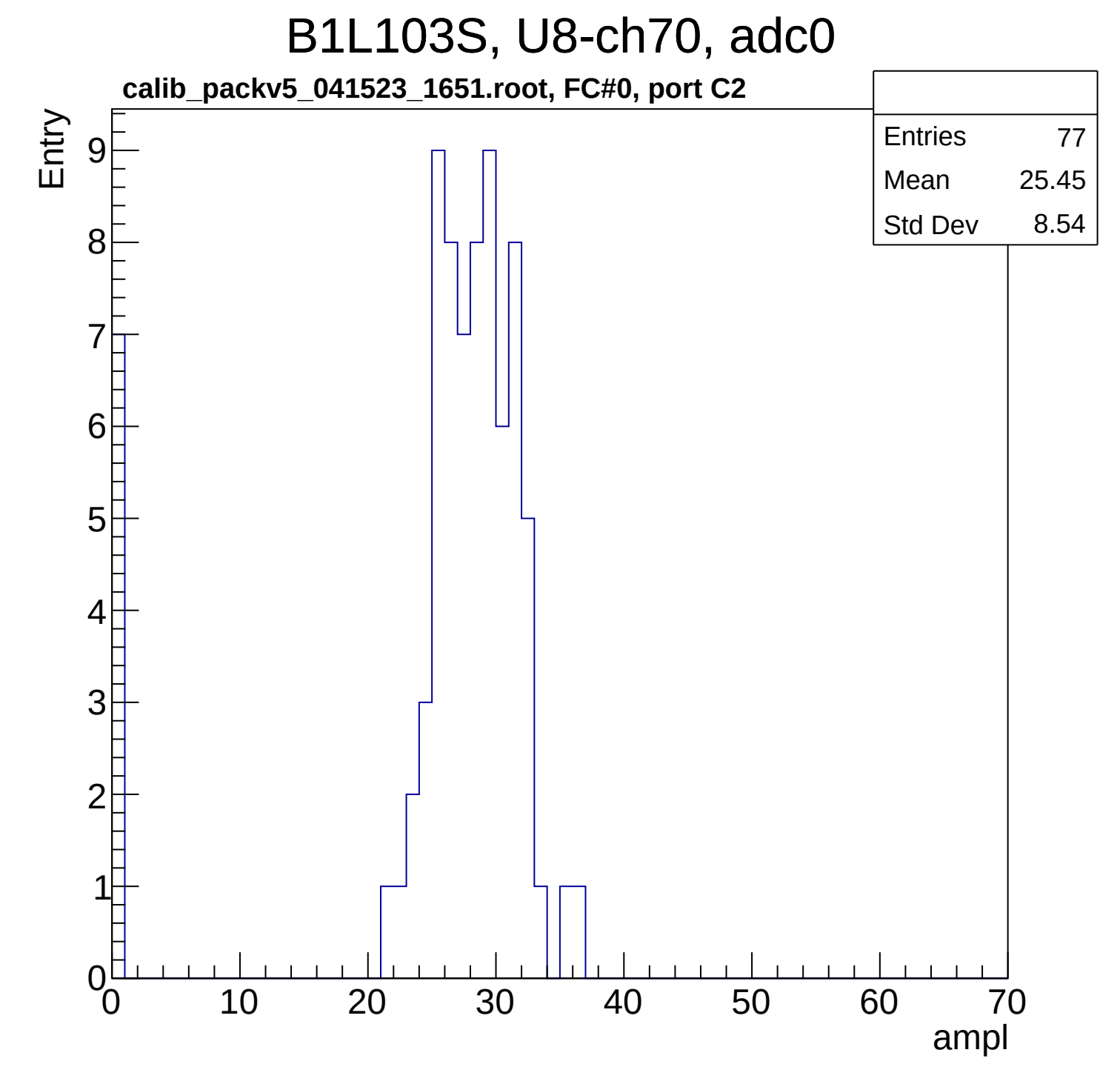
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U8-ch69, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 58.75
Std Dev 8.548
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U8-ch69, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 62.67
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U8-ch69, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch70, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 25.45
Std Dev 8.54
Entry
ampl
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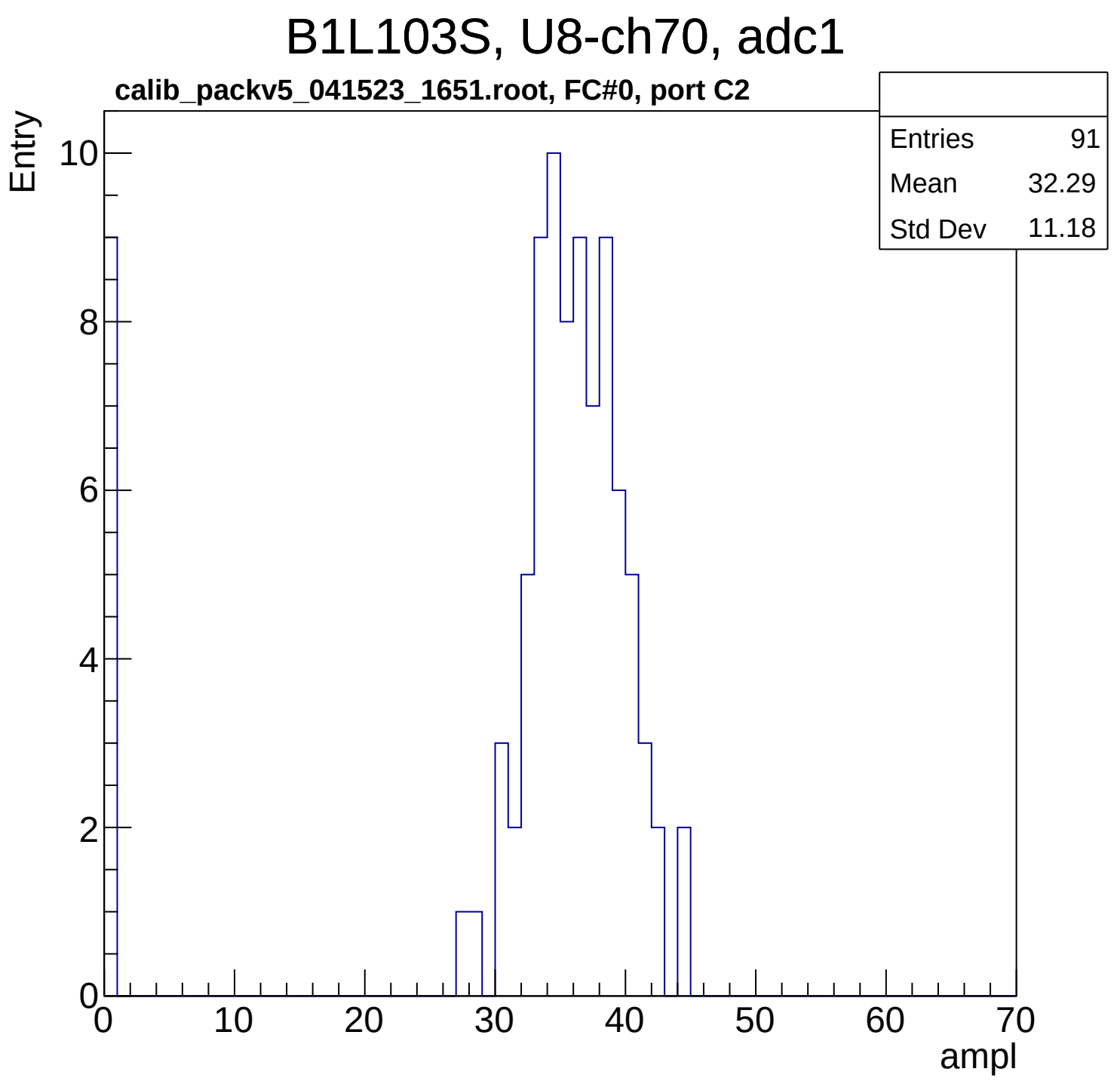
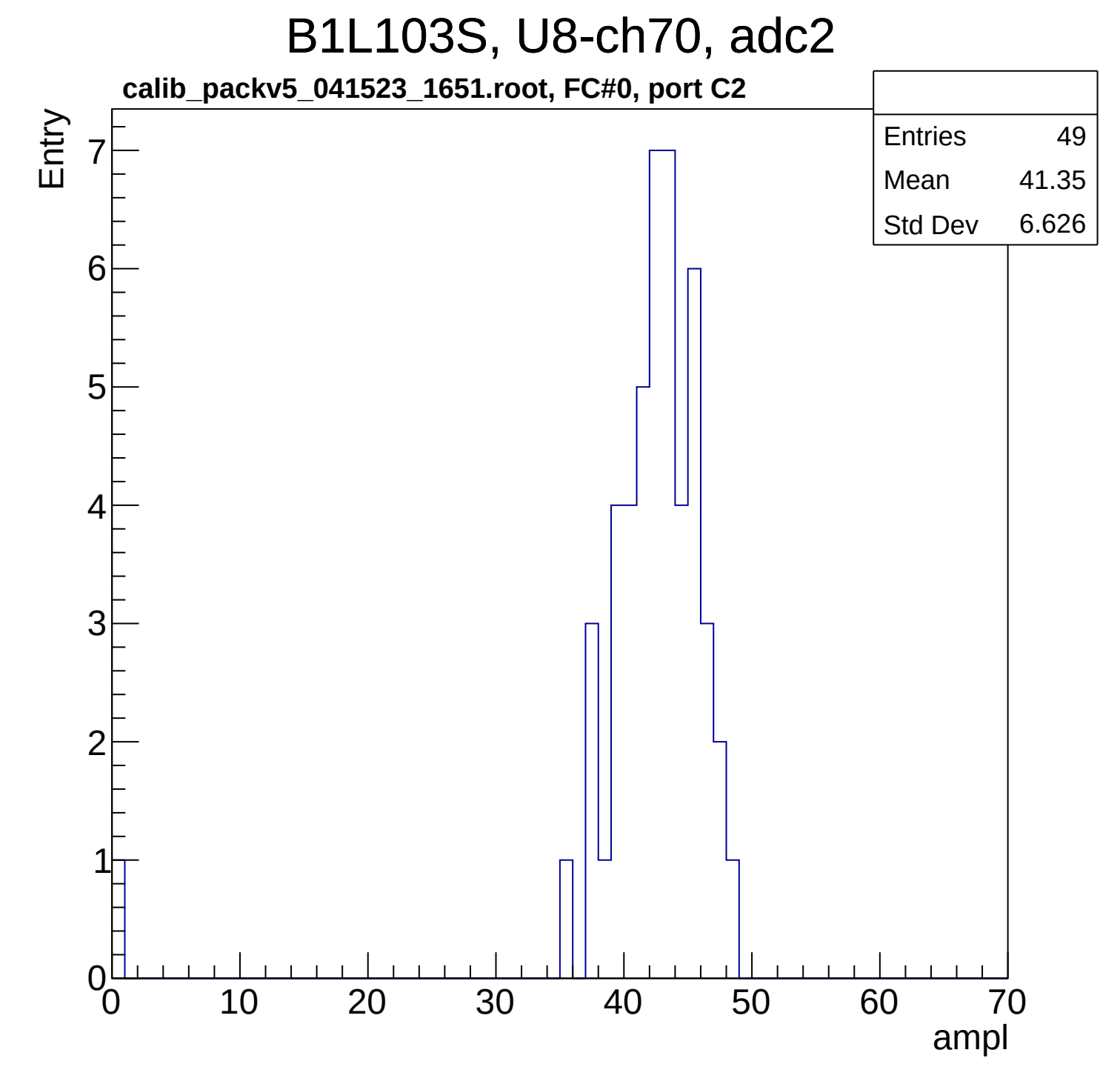
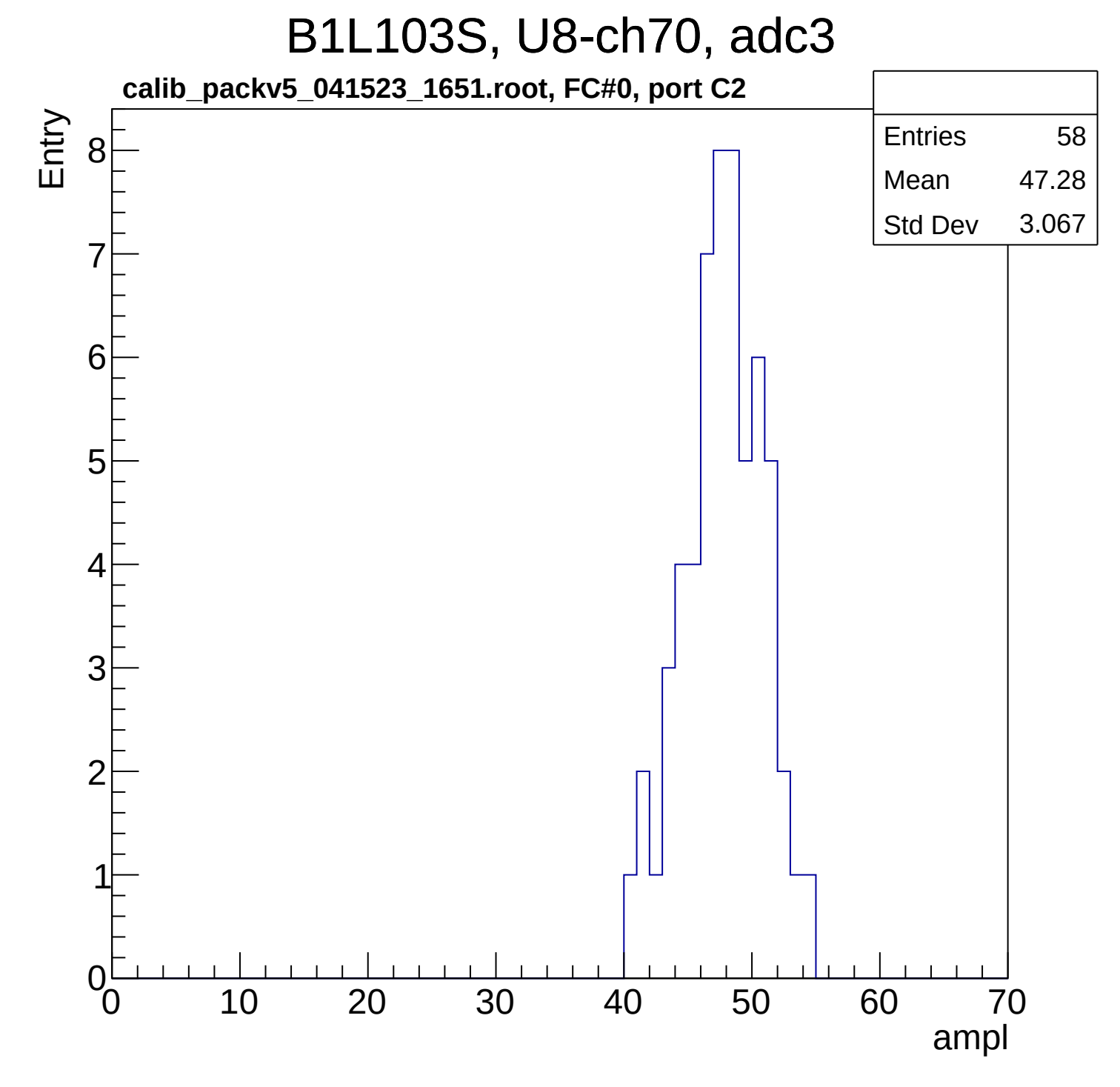
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U8-ch70, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 32.29
Std Dev 11.18
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U8-ch70, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 41.35
Std Dev 6.626
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U8-ch70, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 47.28
Std Dev 3.067
Entry
ampl
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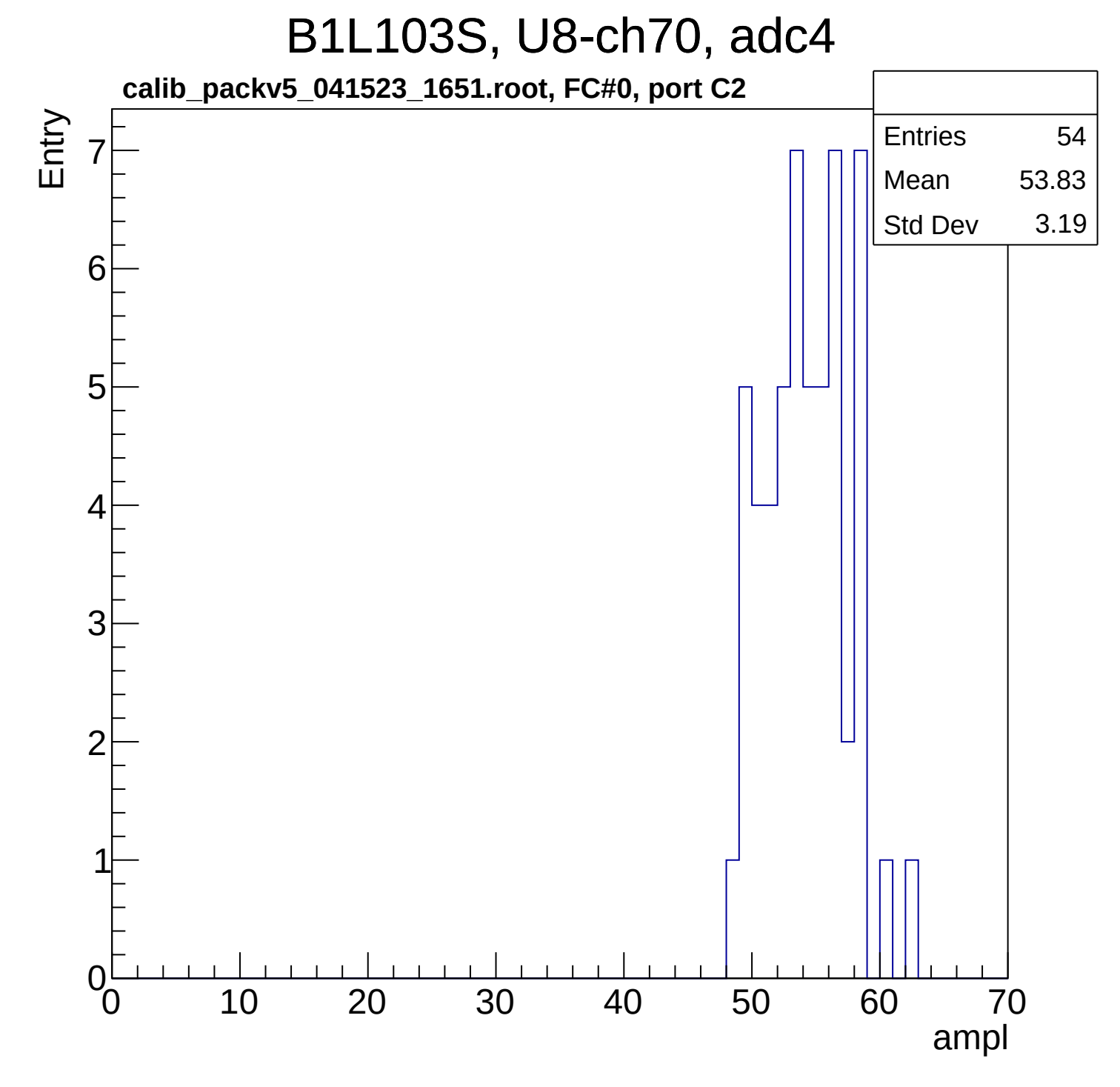
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch70, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 53.83
Std Dev 3.19
Entry
ampl
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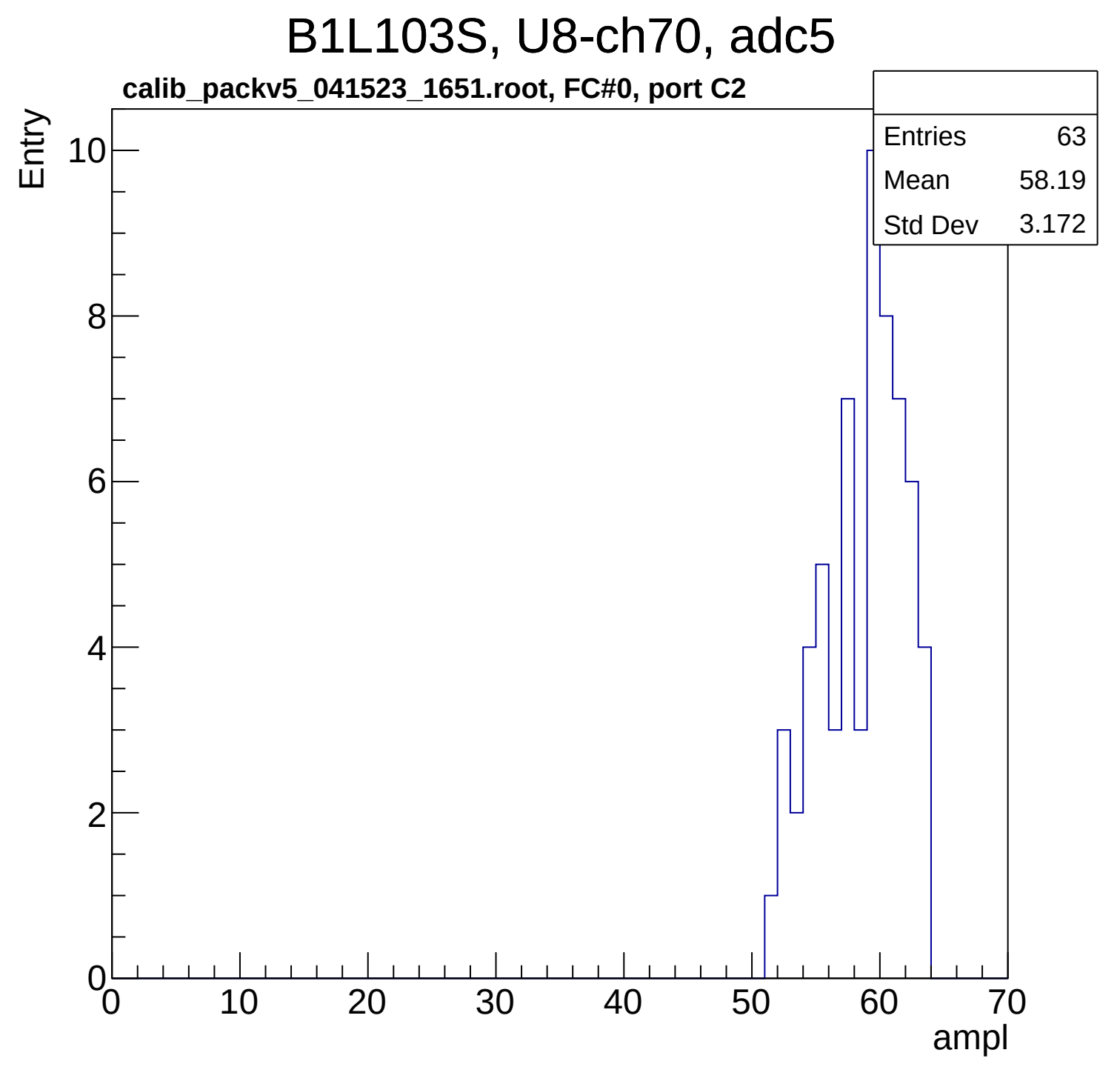
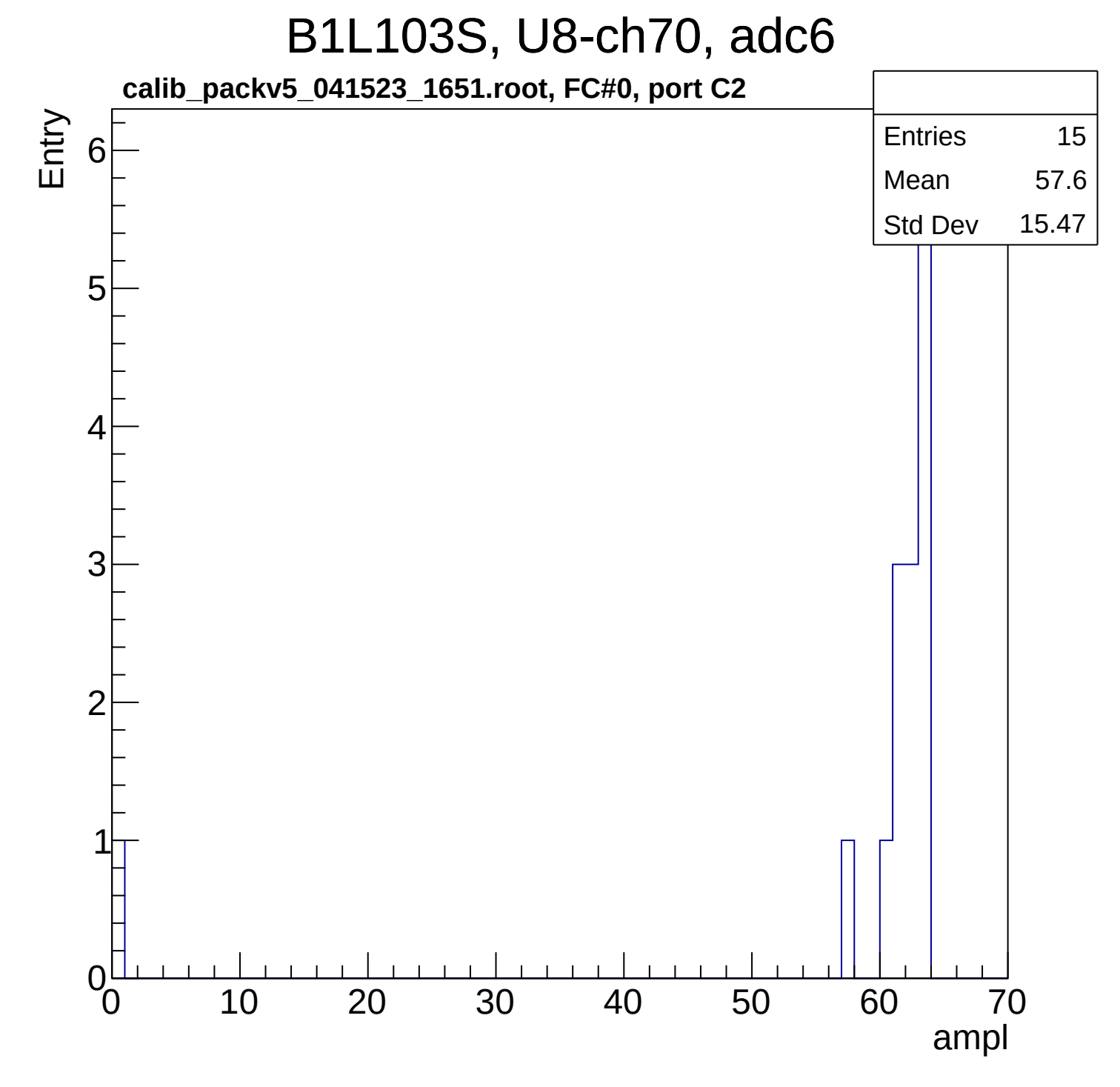
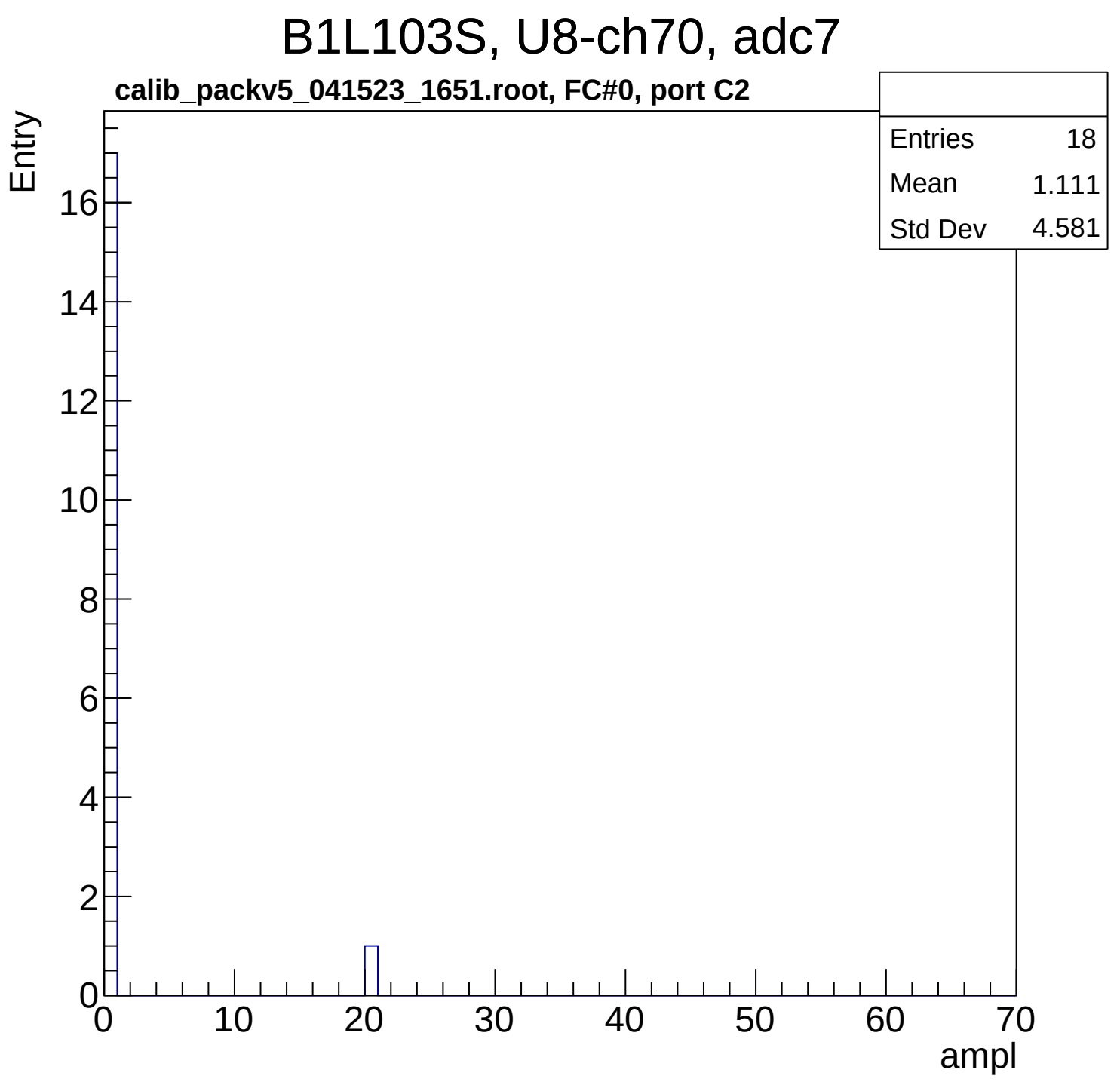
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U8-ch70, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 58.19
Std Dev 3.172
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U8-ch70, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 57.6
Std Dev 15.47
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch70, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.111
Std Dev 4.581
Entry
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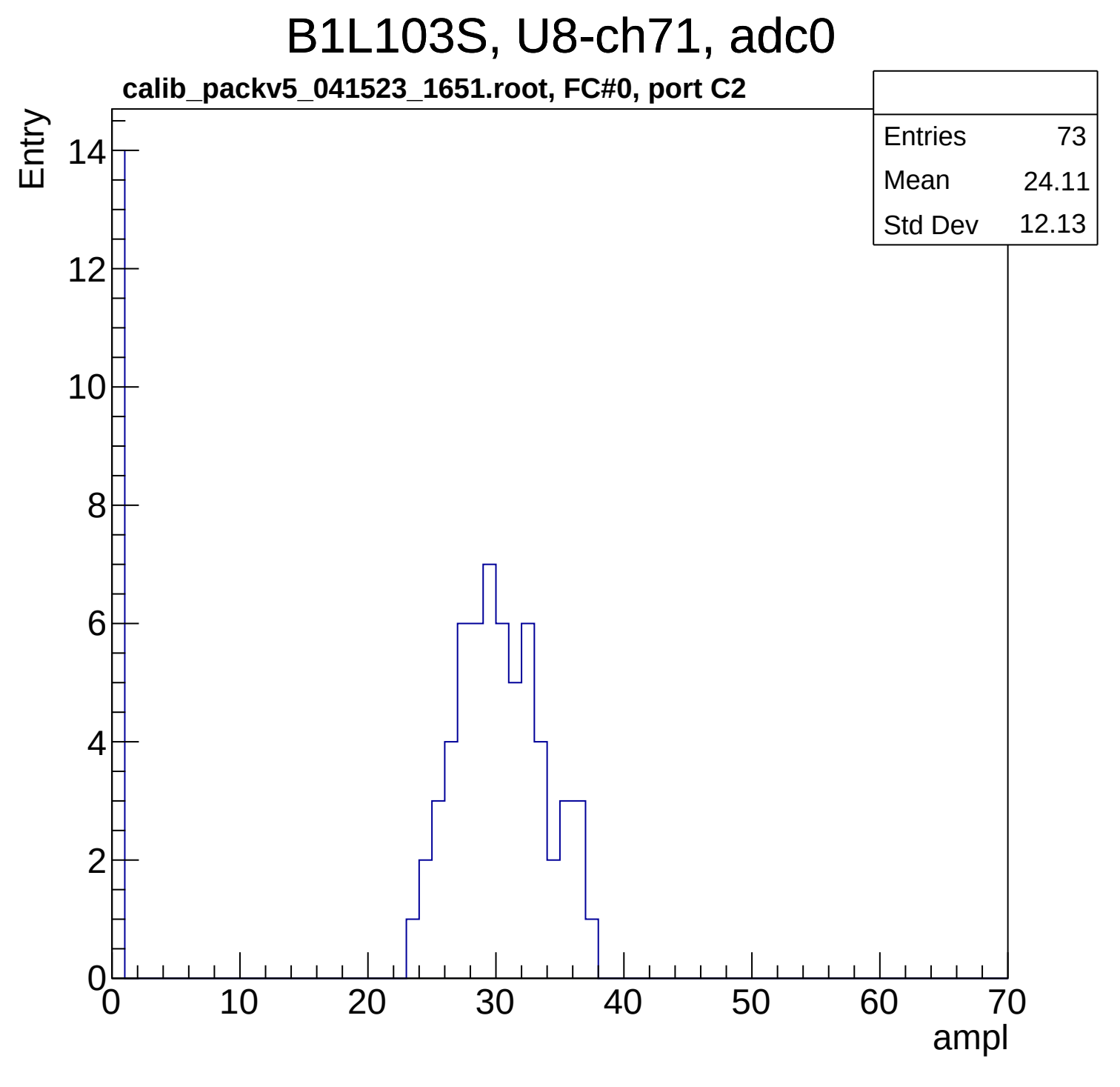
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch71, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 24.11
Std Dev 12.13
Entry
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2
4
6
8
10
12
14
0
10
20
30
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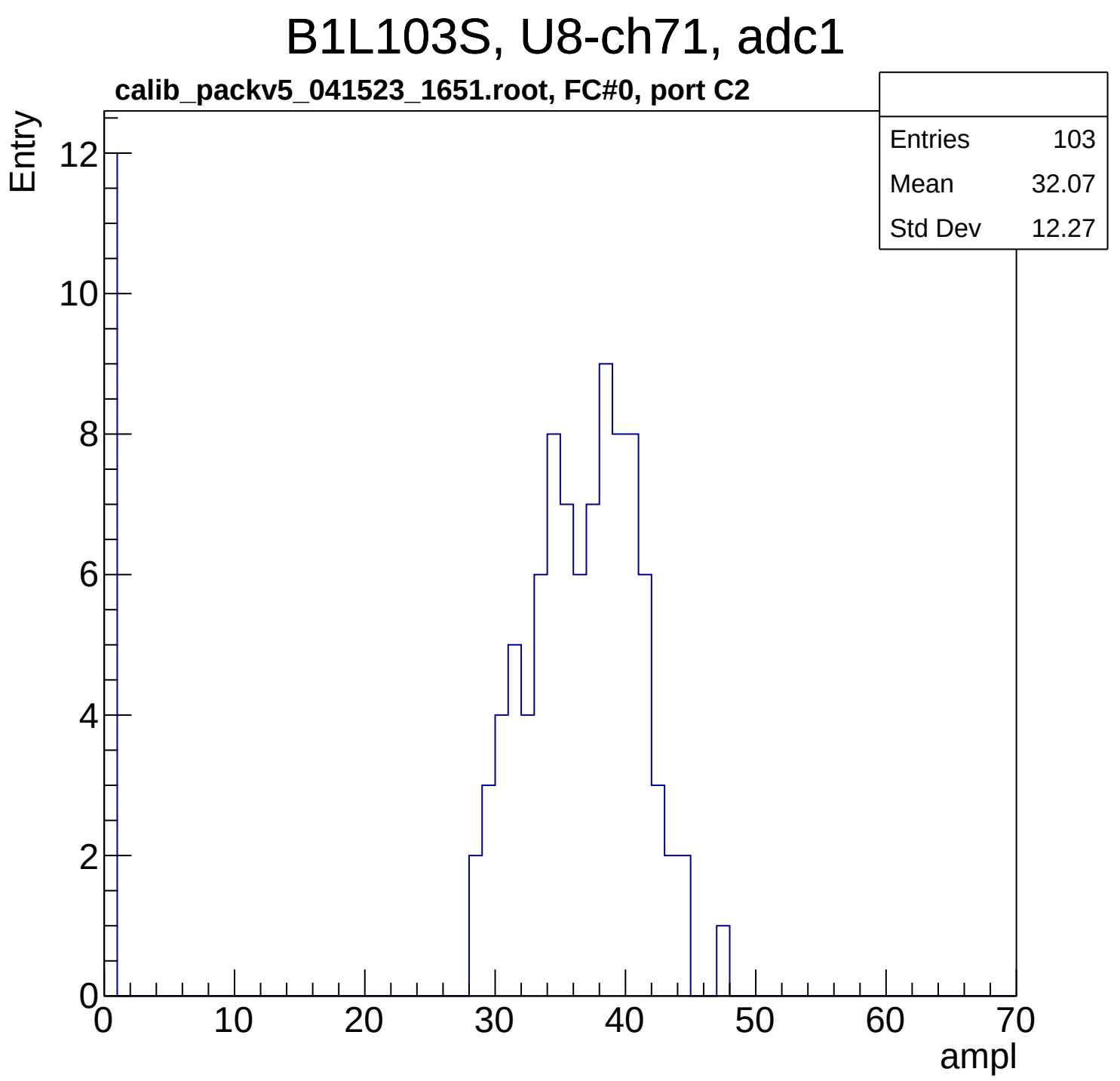
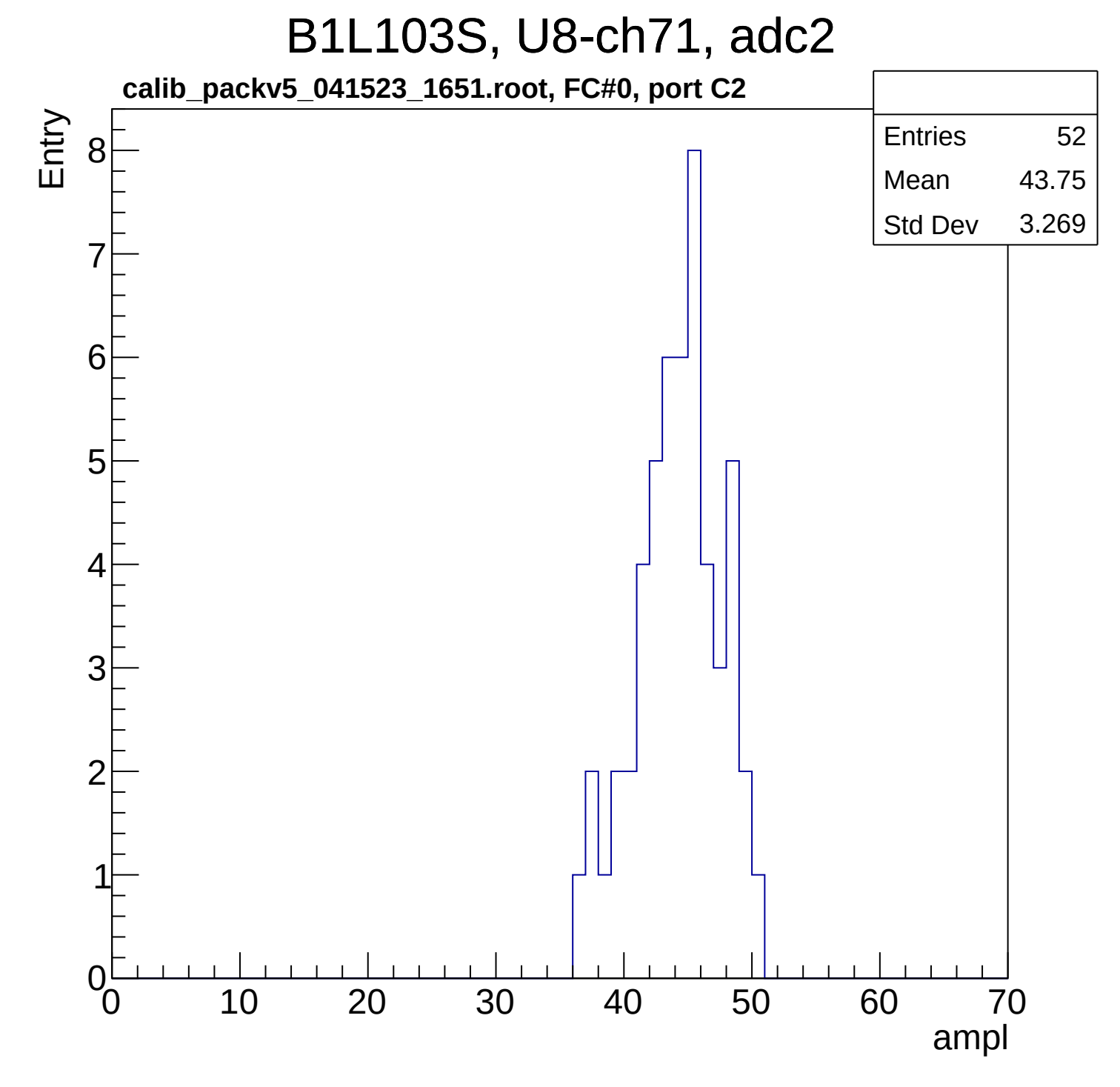
50
60
70
ampl


B1L103S, U8-ch71, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 103
Mean 32.07
Std Dev 12.27
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch71, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 43.75
Std Dev 3.269
Entry
ampl
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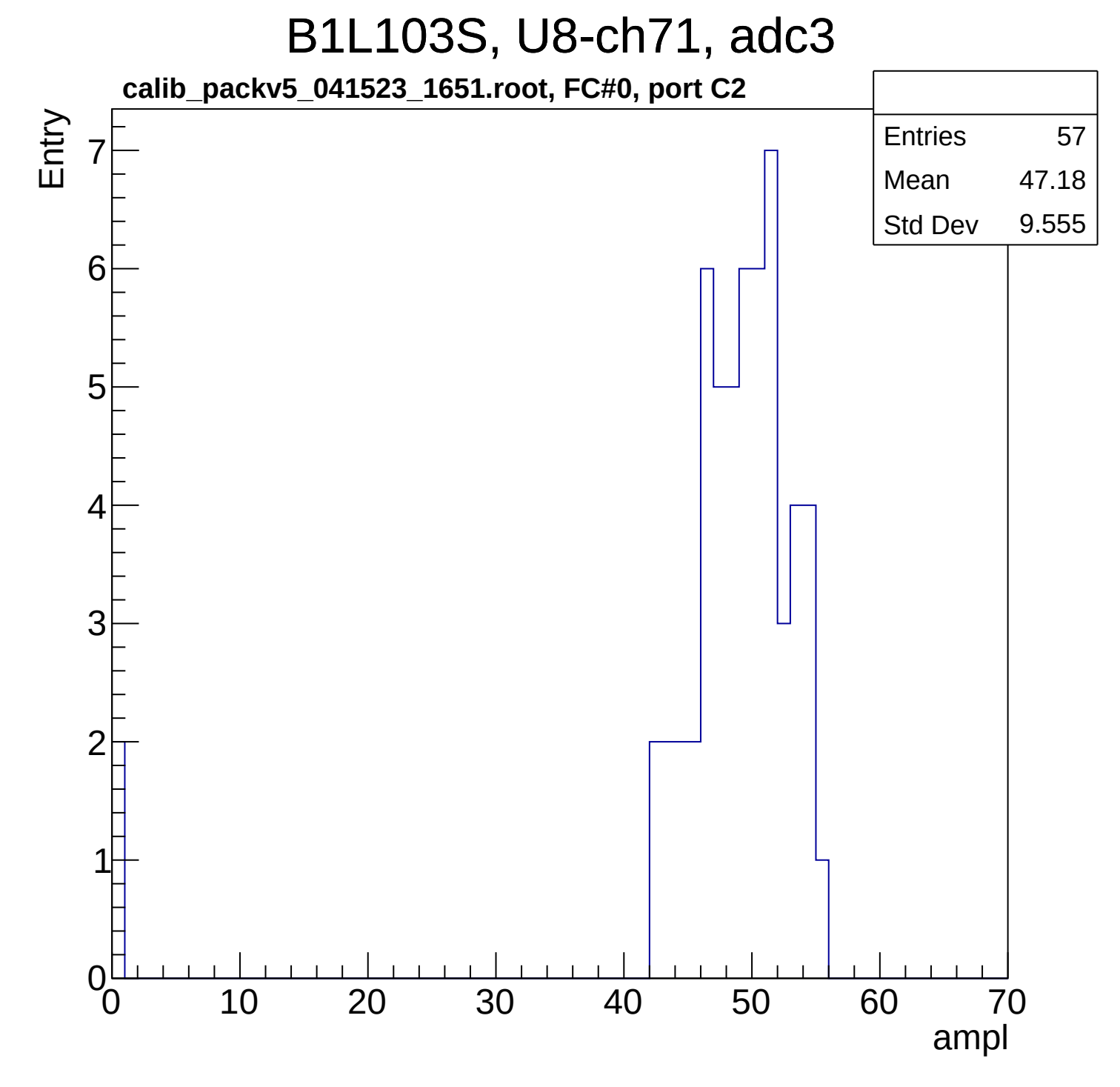
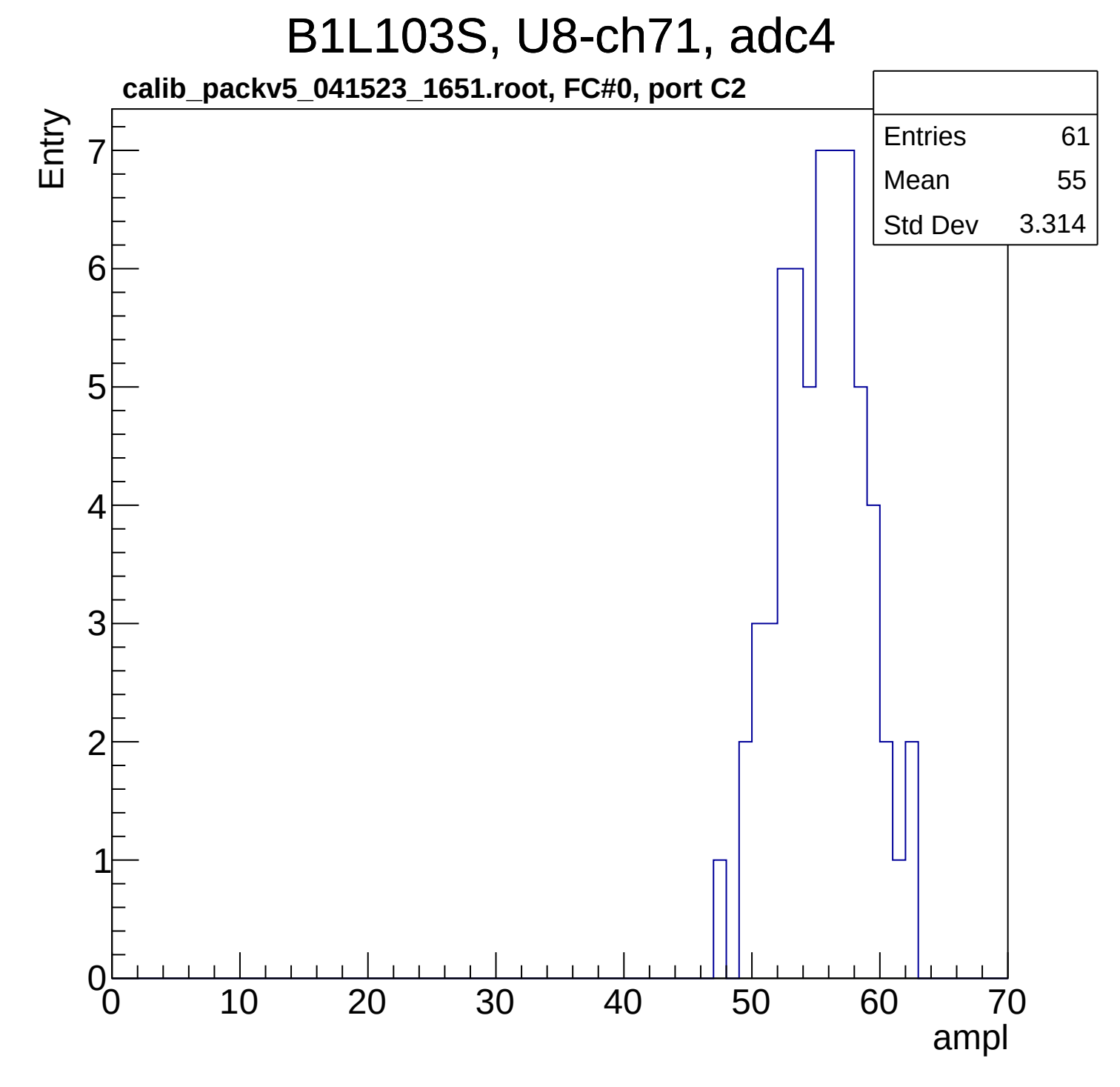
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch71, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 47.18
Std Dev 9.555
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U8-ch71, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 55
Std Dev 3.314
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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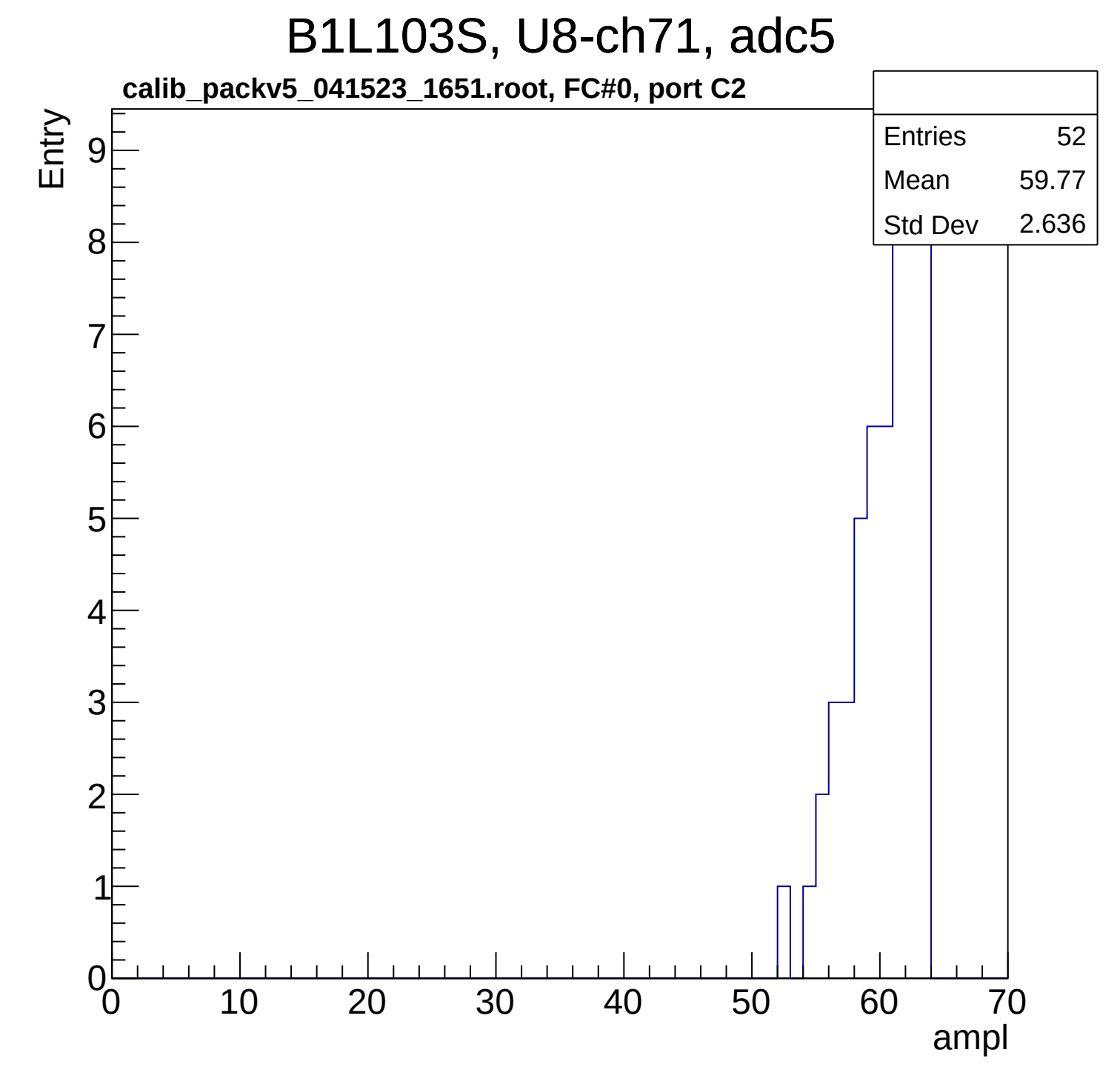
B1L103S, U8-ch71, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 59.77
Std Dev 2.636
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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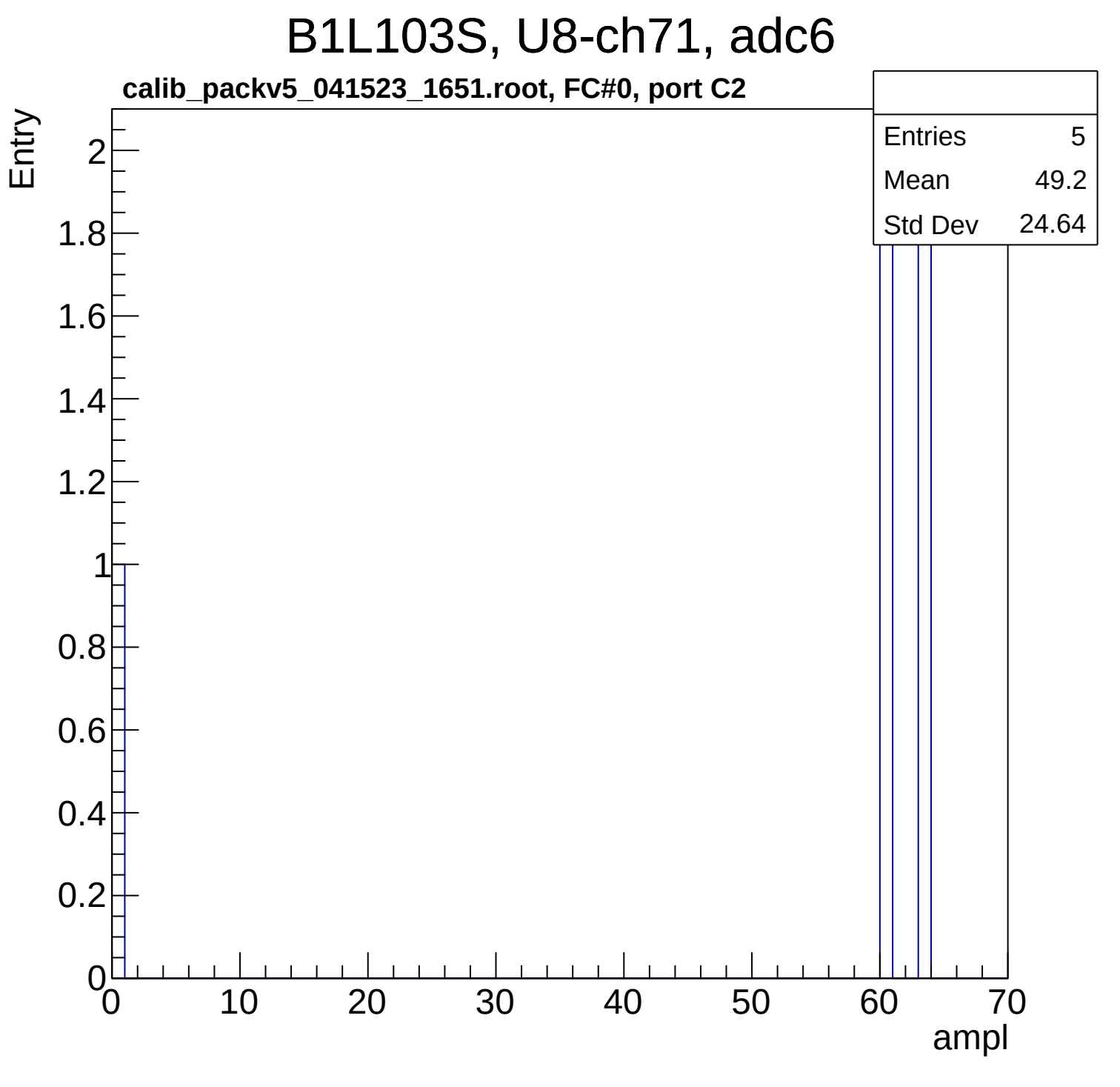
B1L103S, U8-ch71, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 49.2
Std Dev 24.64
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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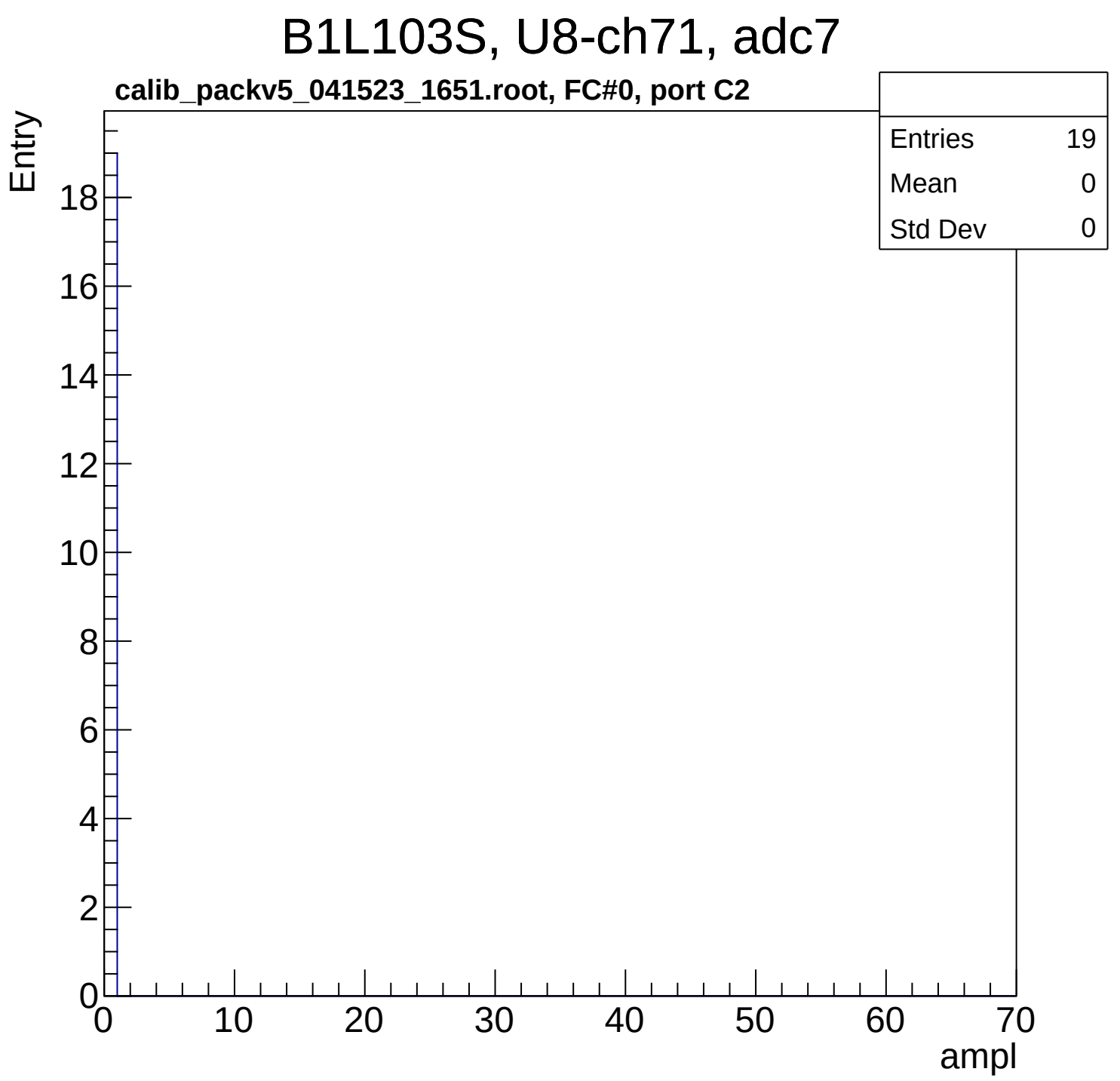
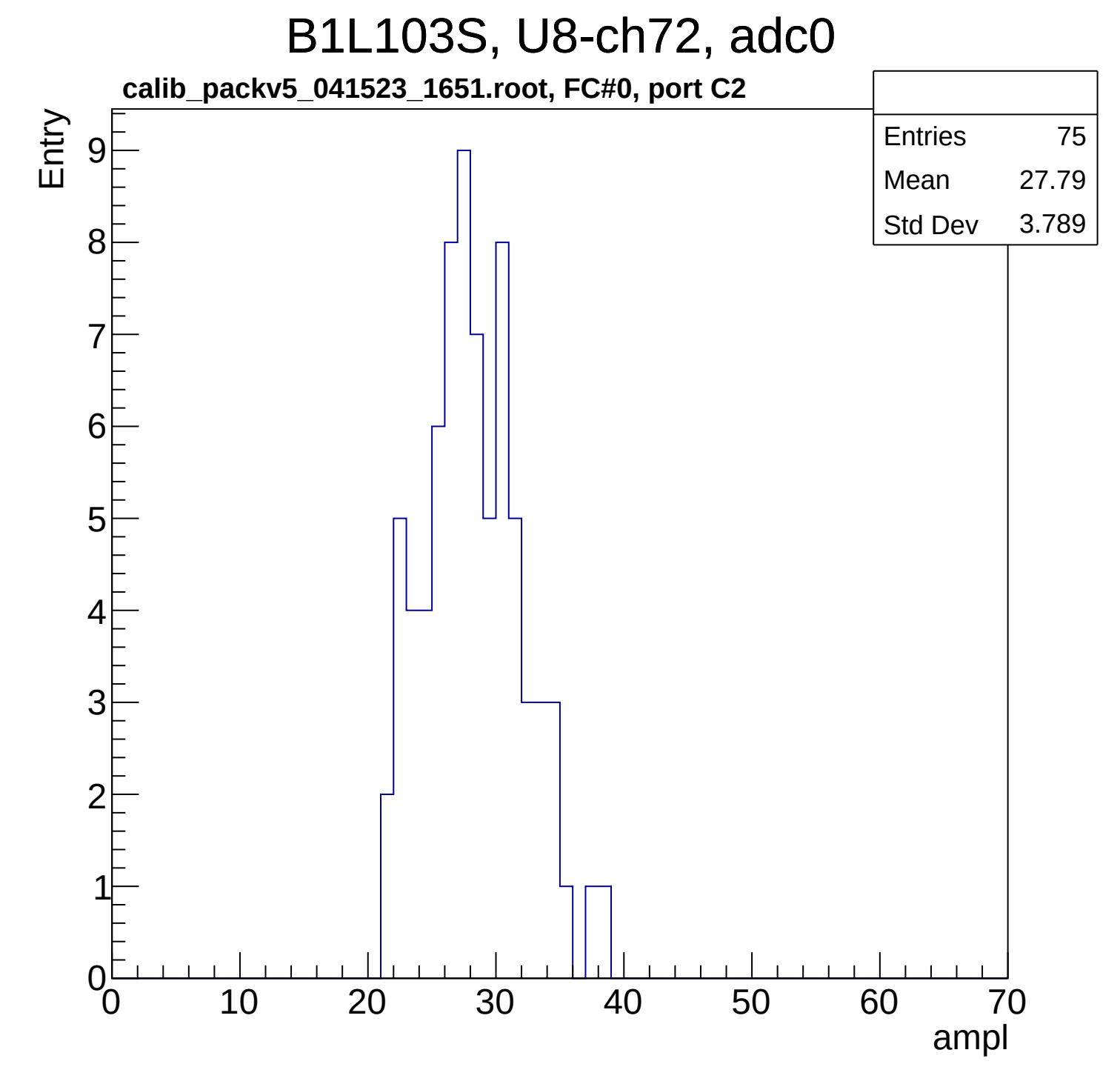
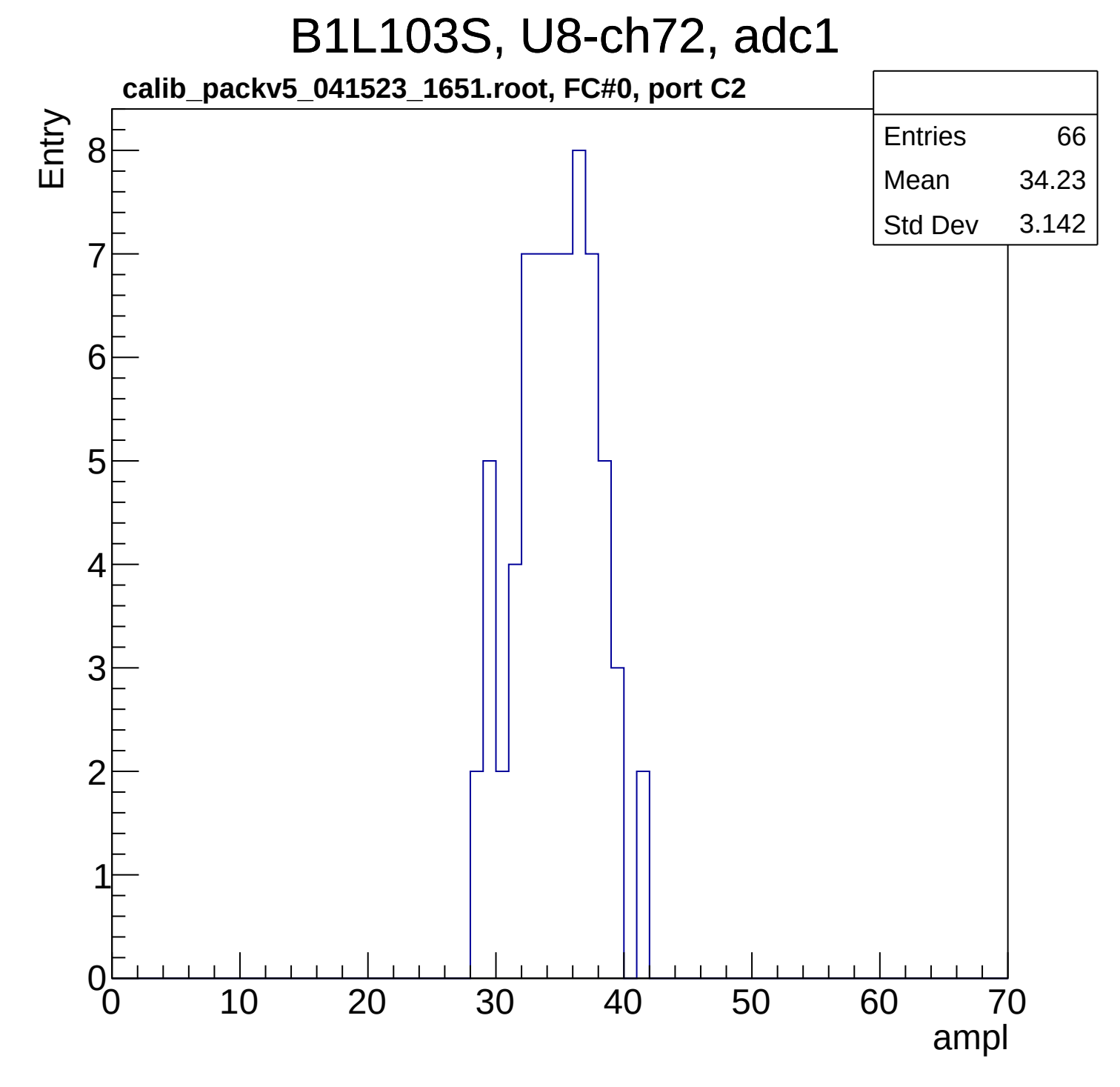
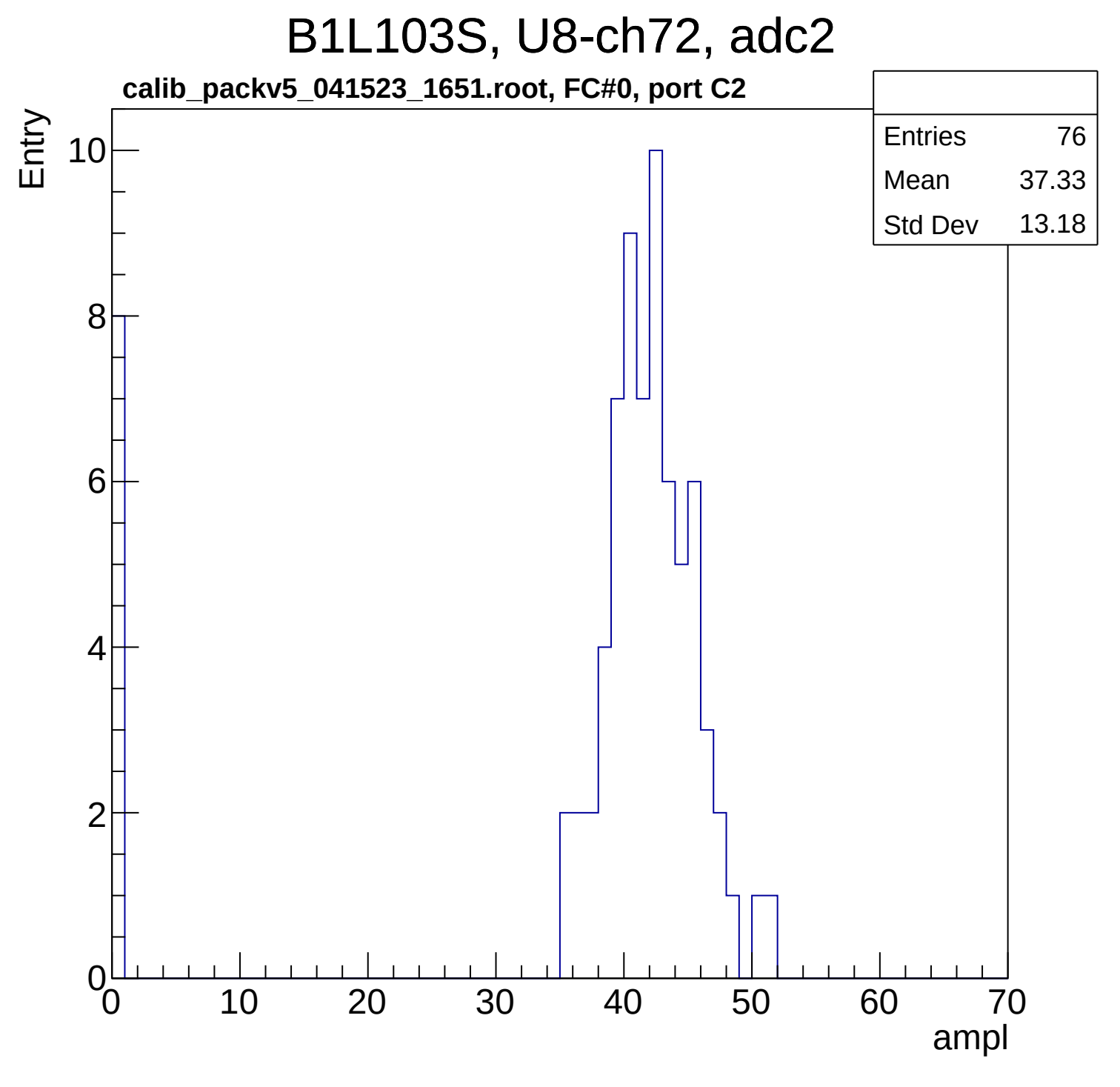
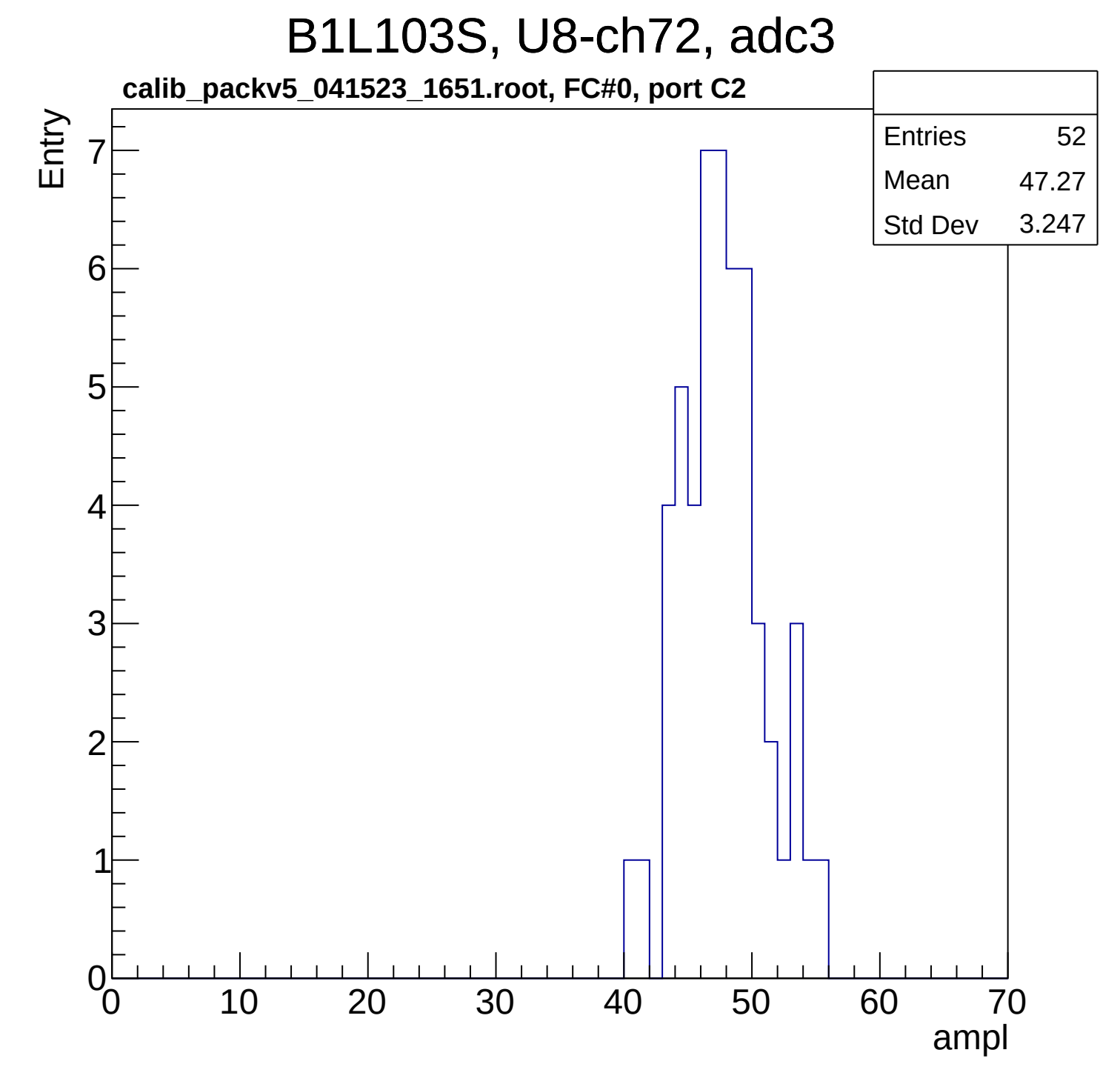

B1L103S, U8-ch71, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch72, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 27.79
Std Dev 3.789
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U8-ch72, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 34.23
Std Dev 3.142
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch72, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 37.33
Std Dev 13.18
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch72, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 47.27
Std Dev 3.247
Entry
ampl
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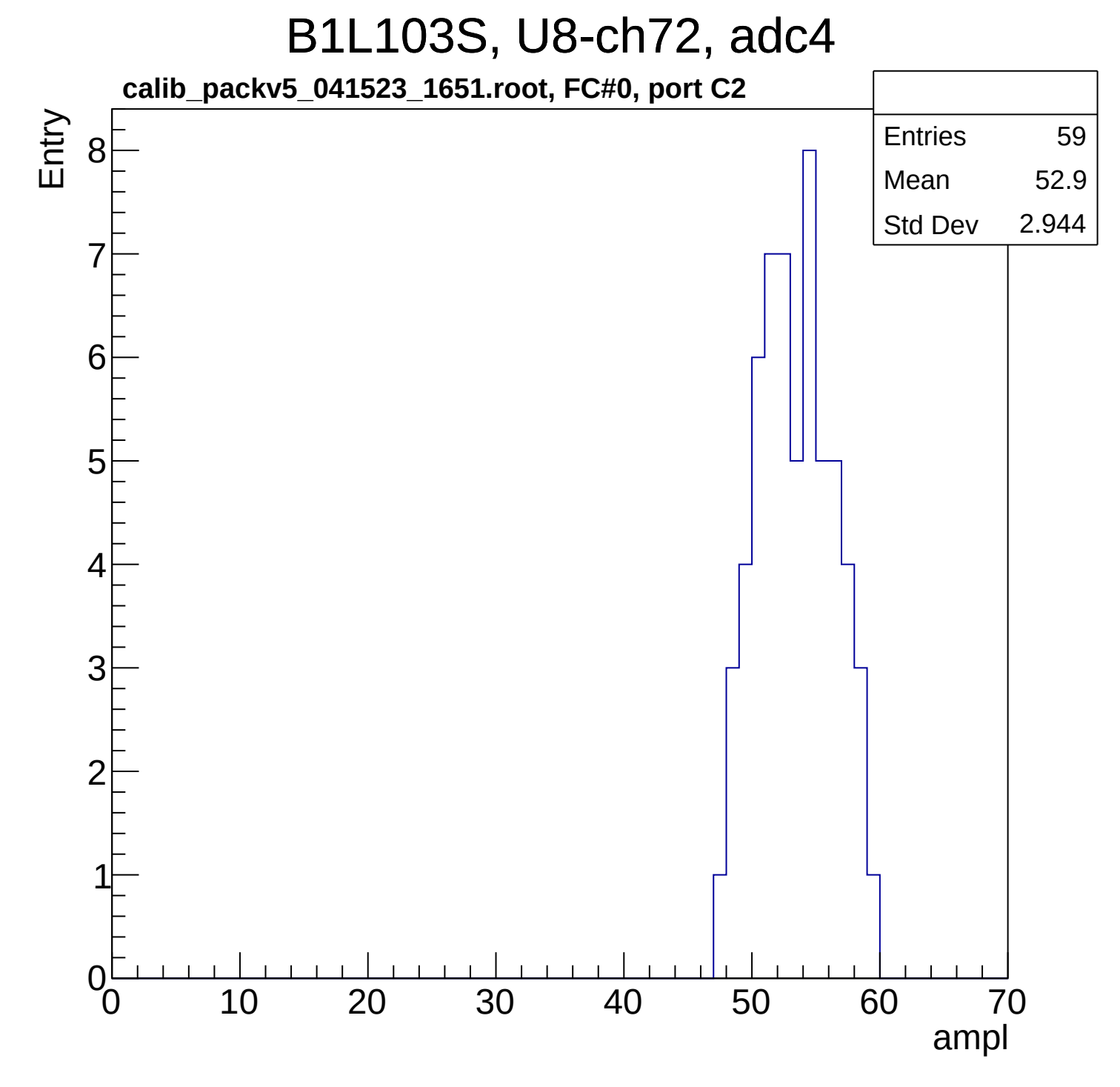
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U8-ch72, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 52.9
Std Dev 2.944
Entry
ampl
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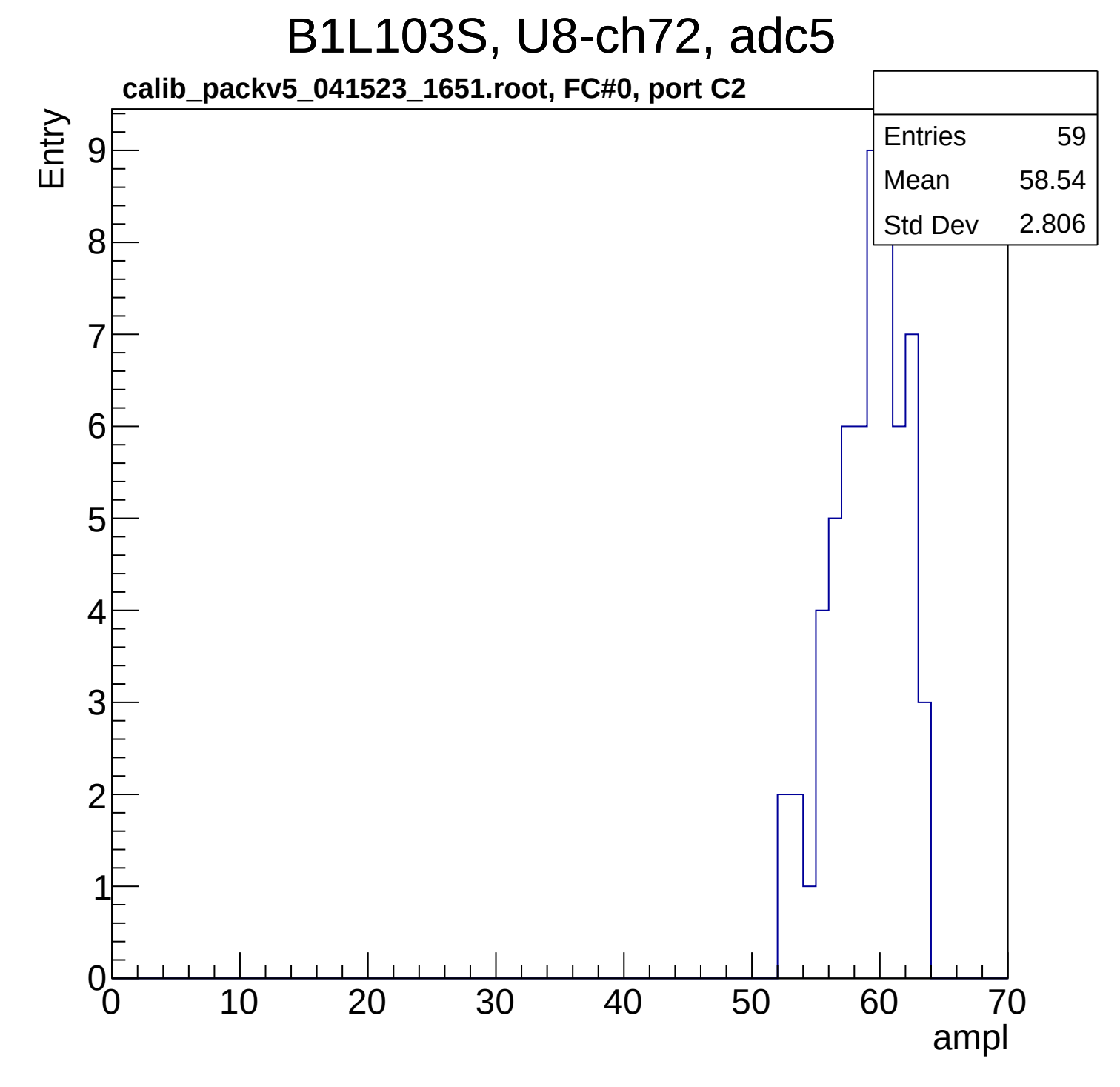
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch72, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 58.54
Std Dev 2.806
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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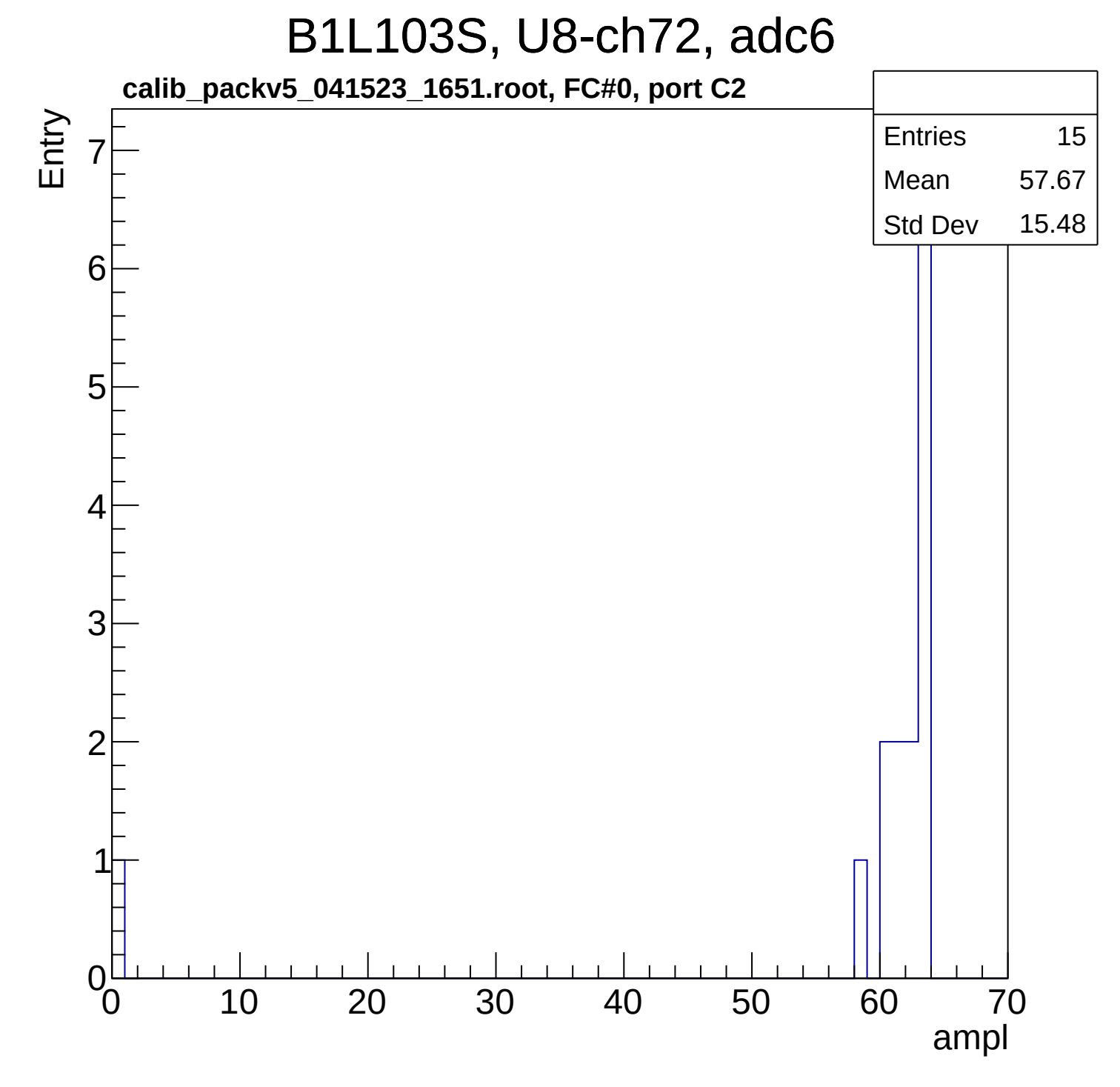
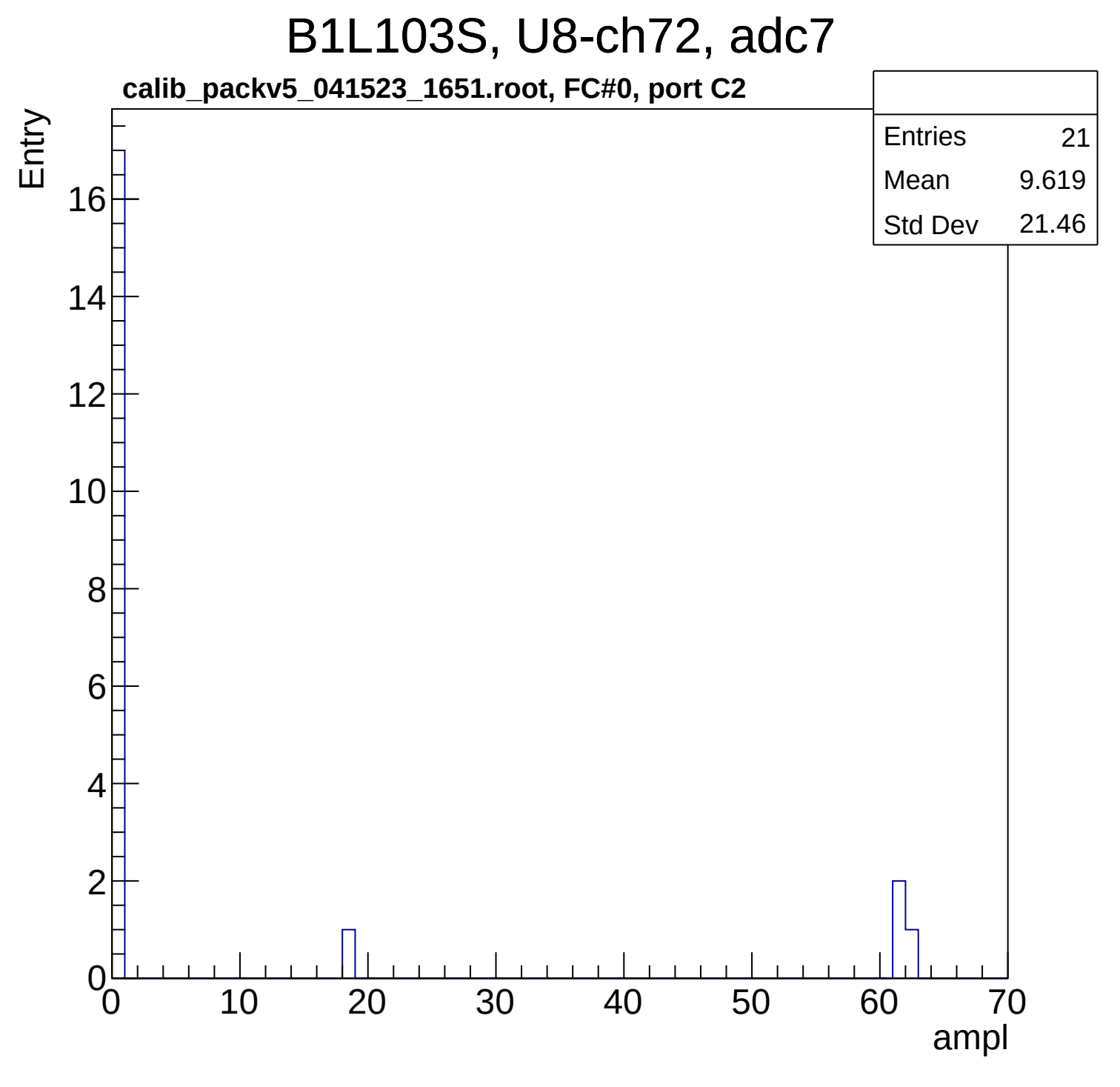
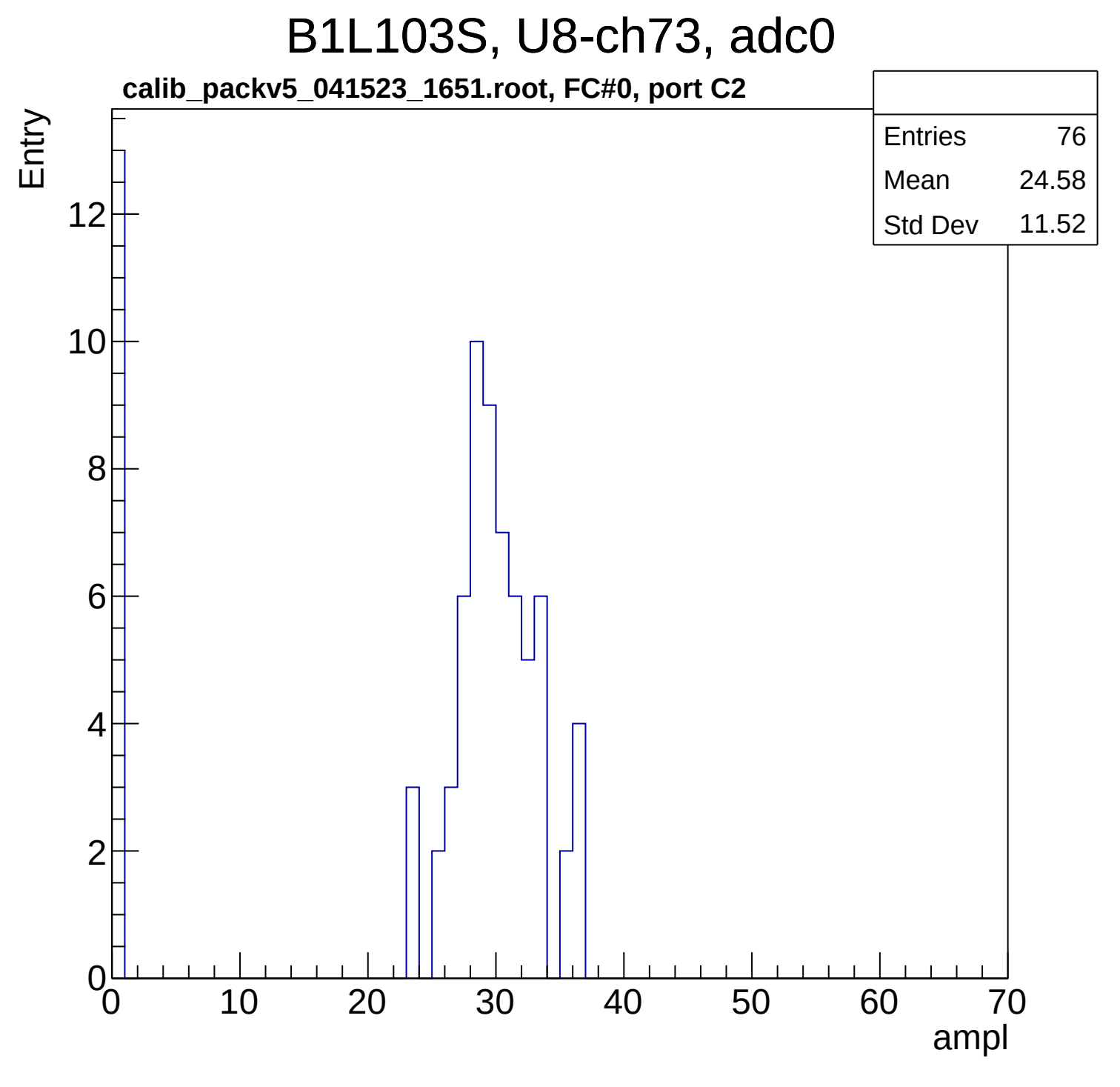
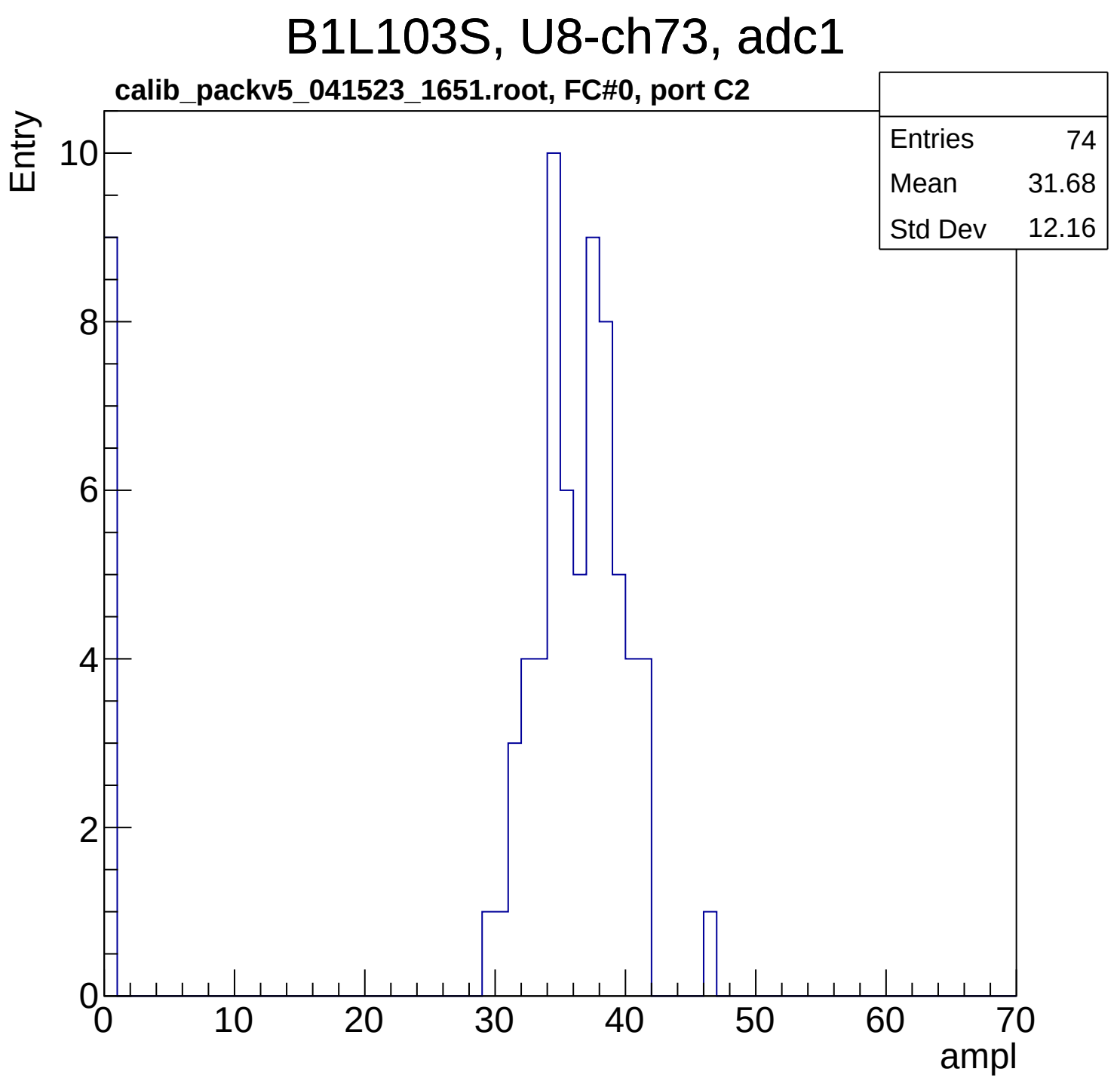
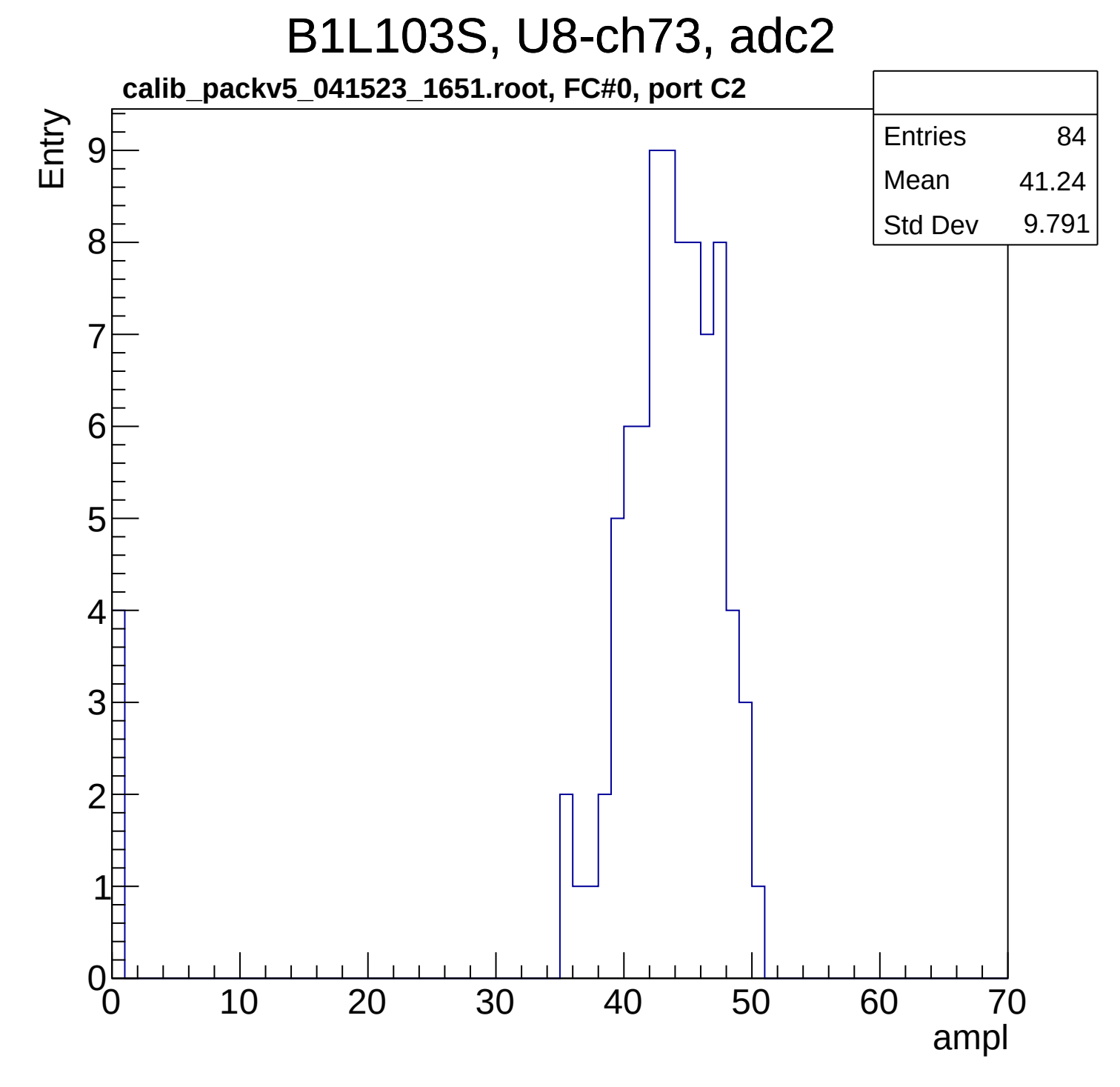

B1L103S, U8-ch72, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 57.67
Std Dev 15.48
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U8-ch72, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 9.619
Std Dev 21.46
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch73, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 24.58
Std Dev 11.52
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U8-ch73, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 31.68
Std Dev 12.16
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U8-ch73, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 41.24
Std Dev 9.791
Entry
ampl
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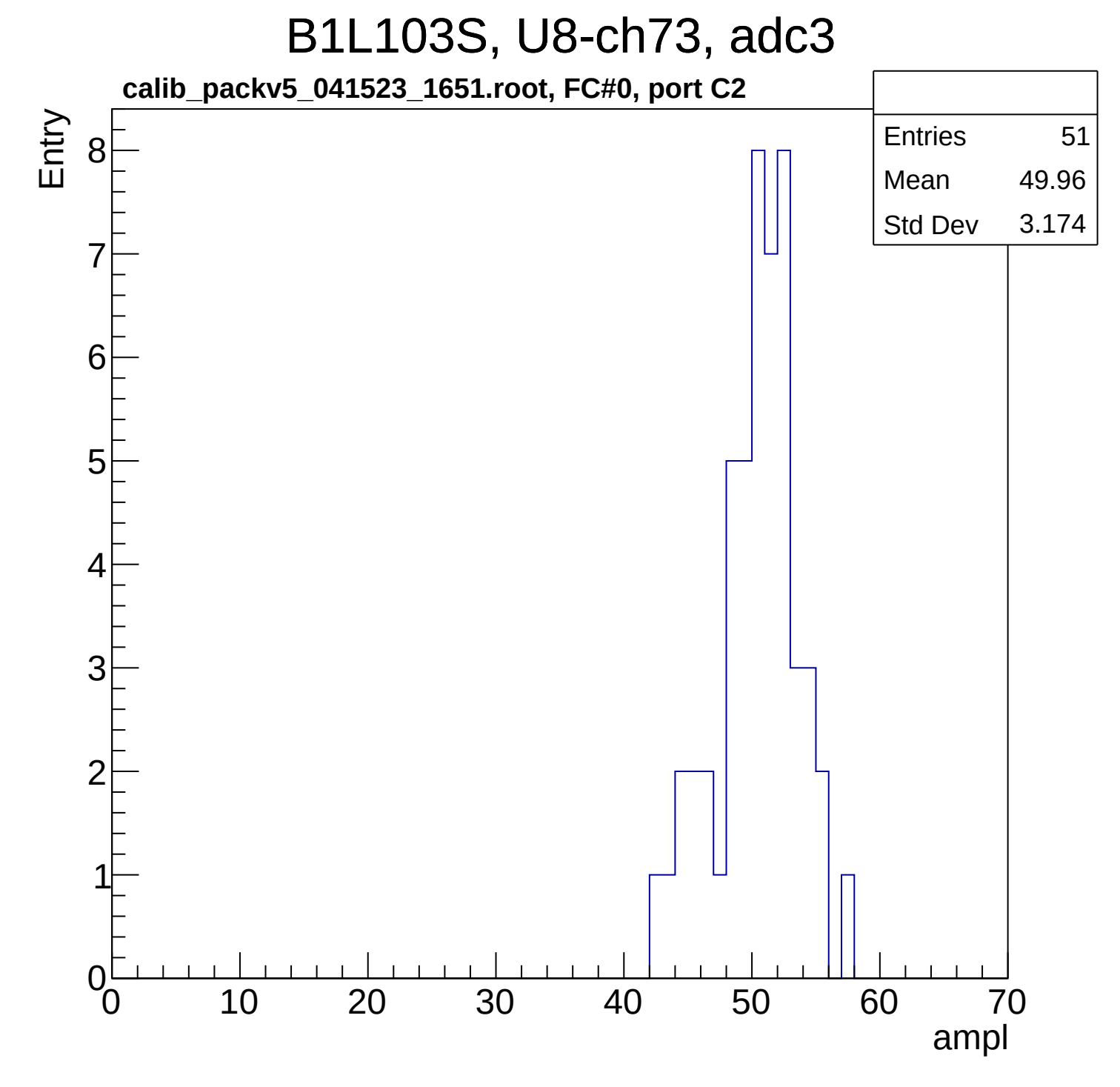
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U8-ch73, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 49.96
Std Dev 3.174
Entry
ampl
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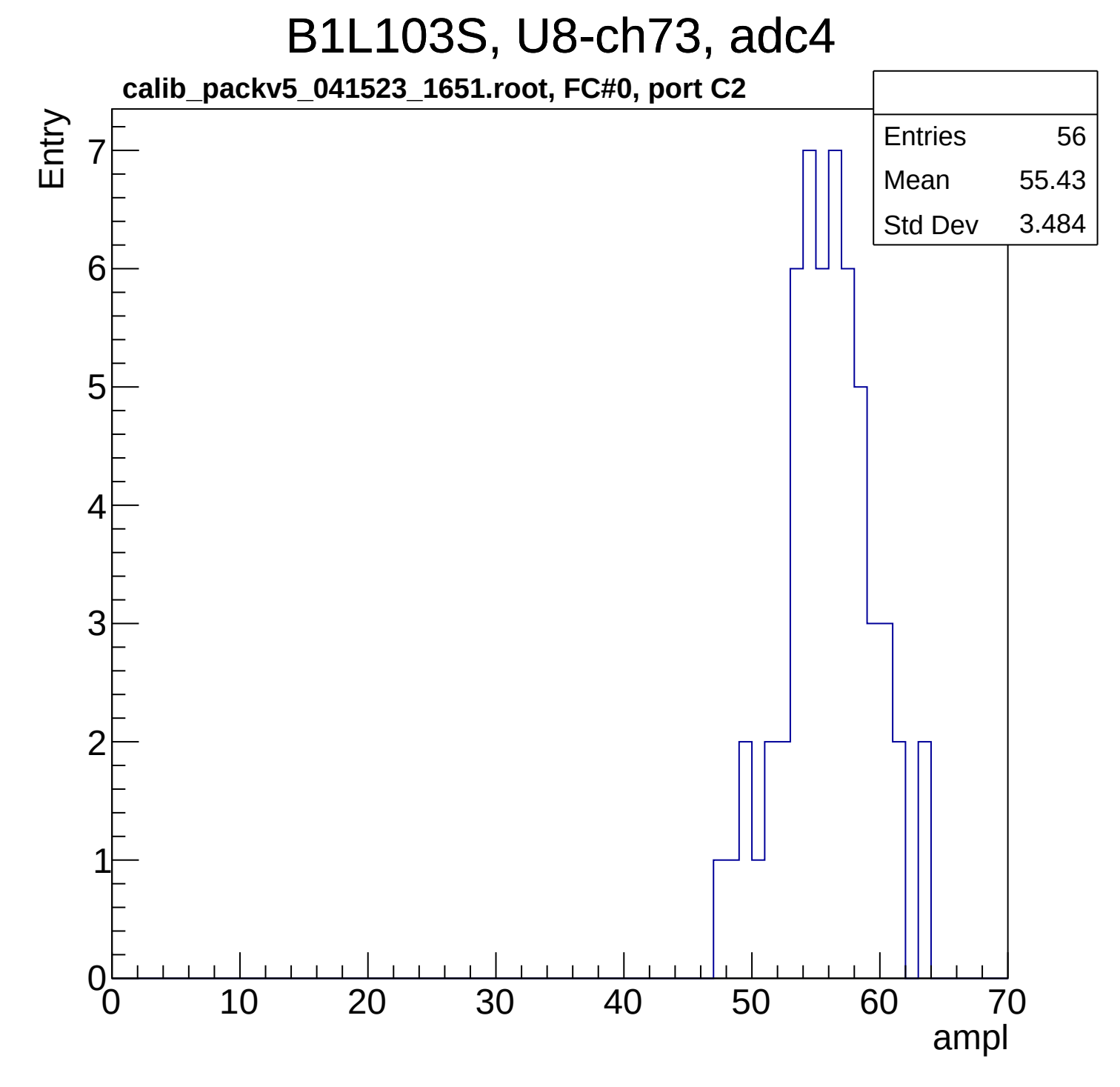
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch73, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 55.43
Std Dev 3.484
Entry
ampl
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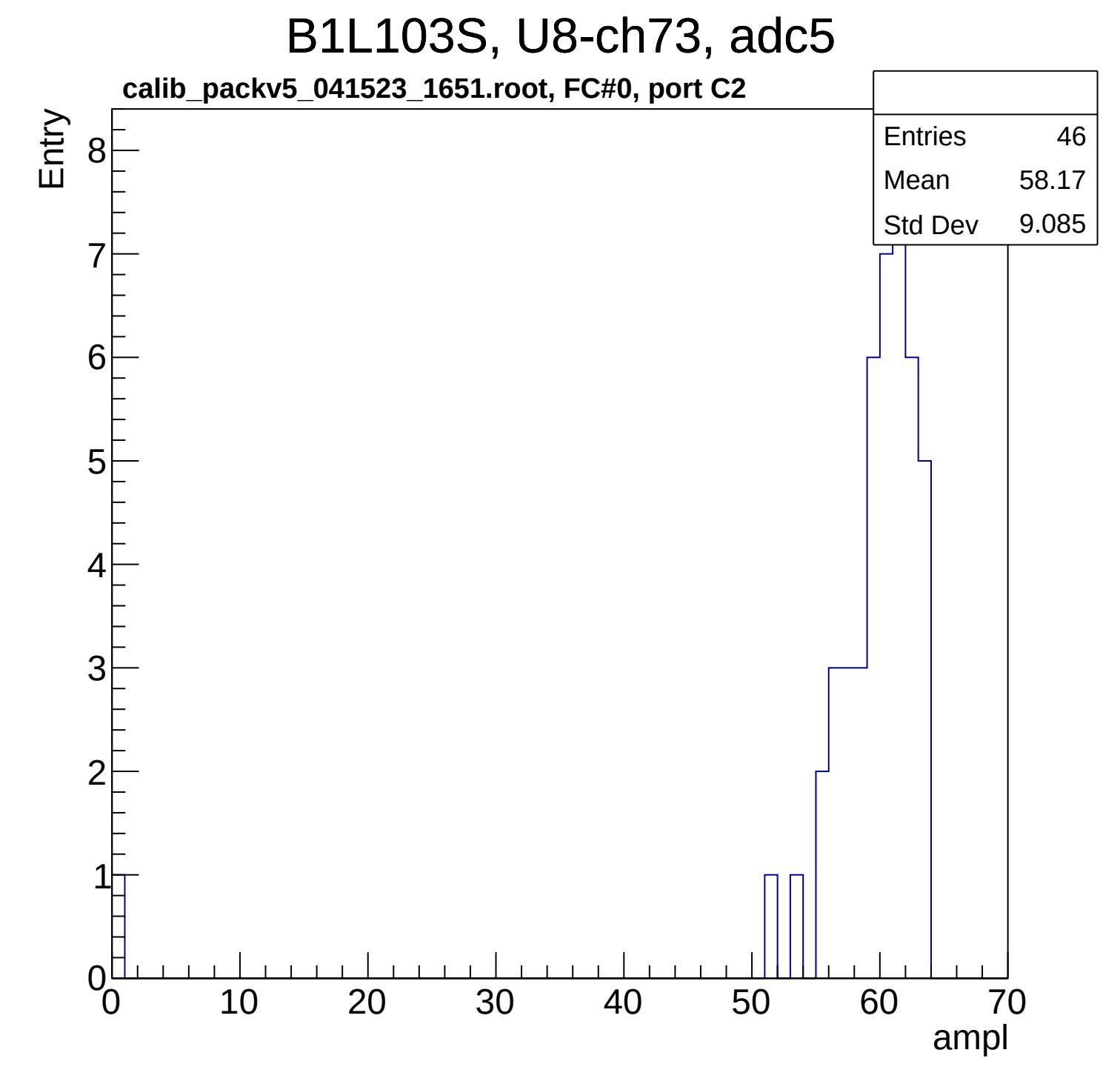
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U8-ch73, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 58.17
Std Dev 9.085
Entry
ampl
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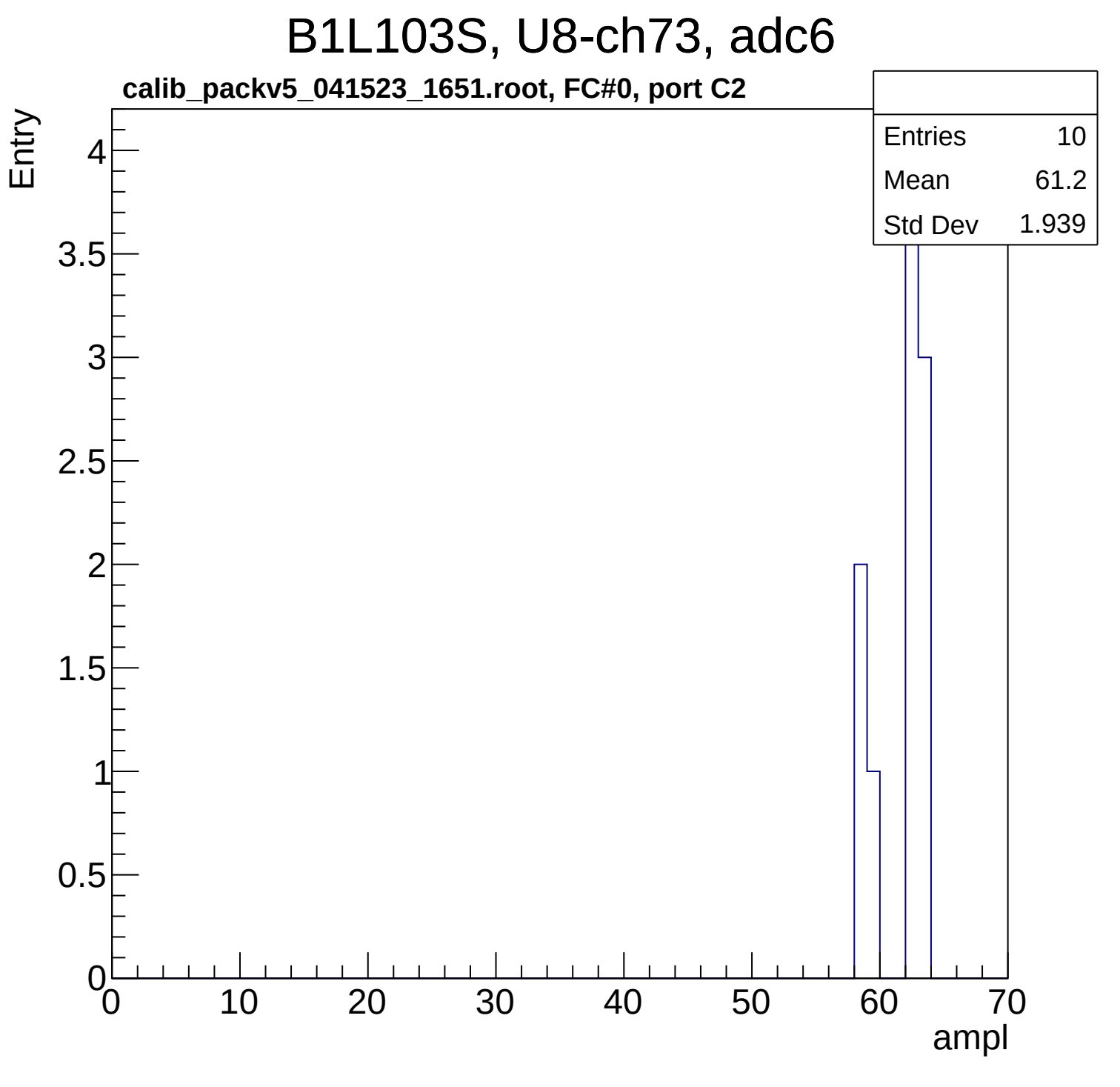
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch73, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61.2
Std Dev 1.939
Entry
ampl
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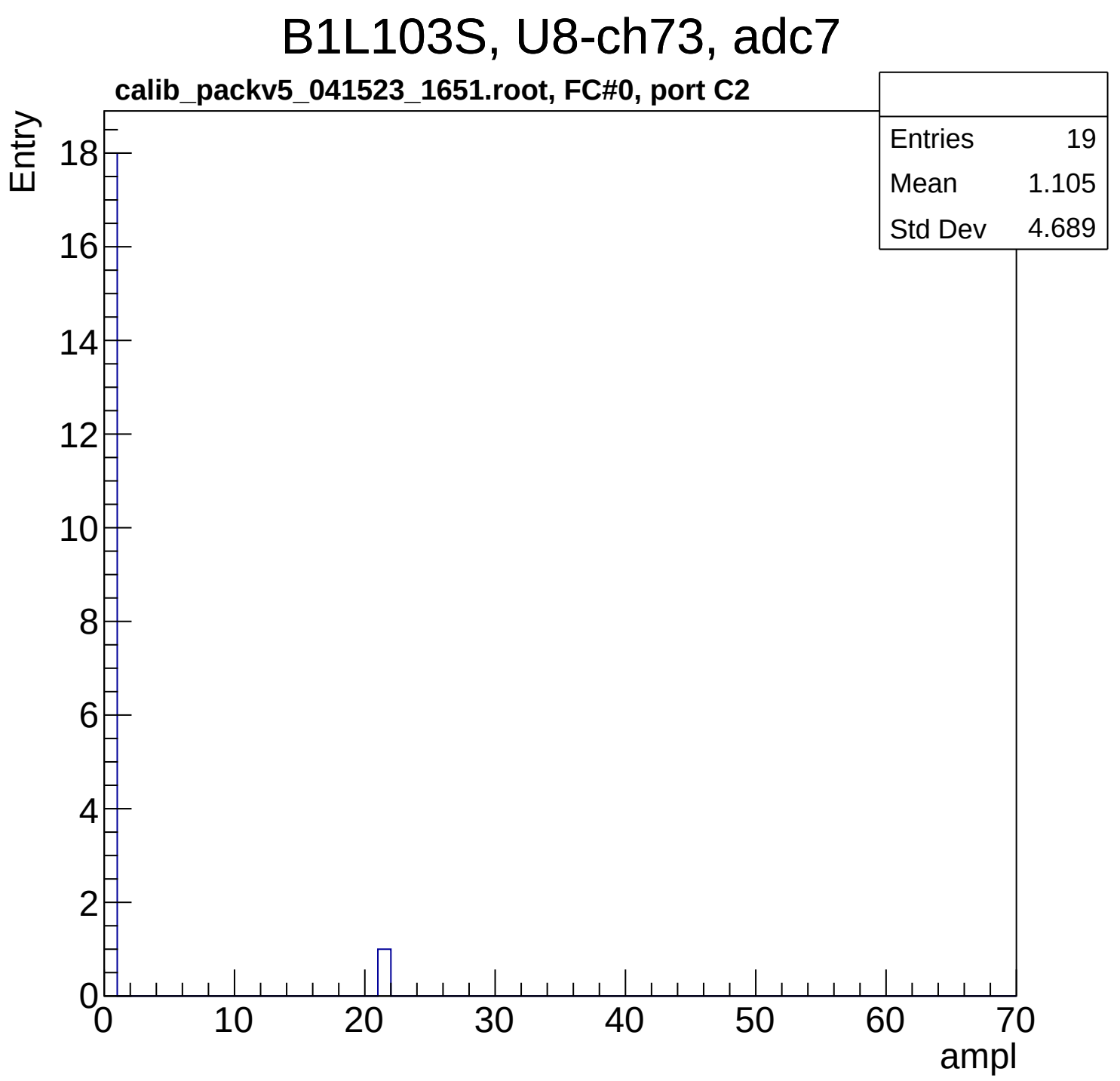
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U8-ch73, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.105
Std Dev 4.689
Entry
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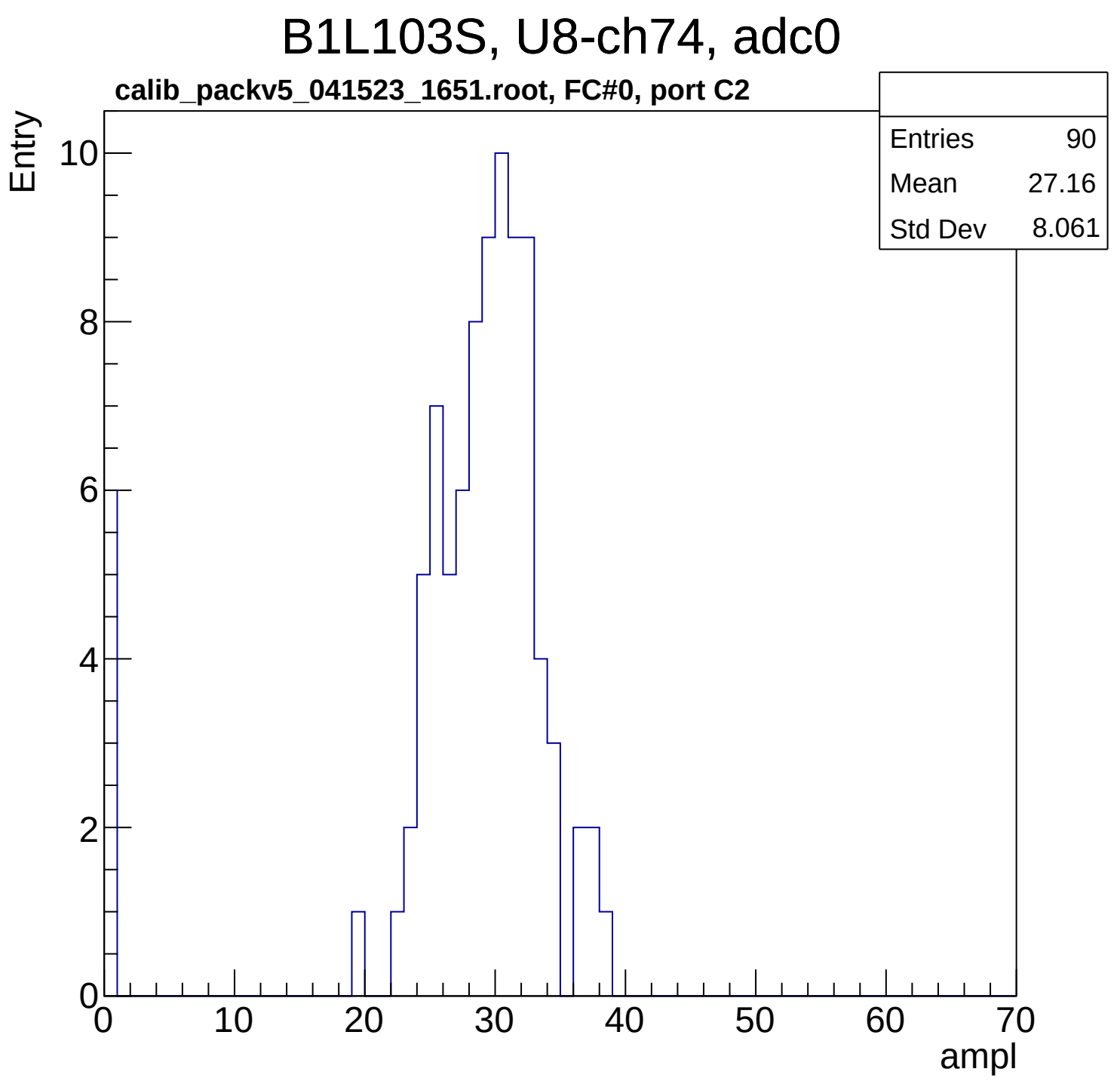
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch74, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 27.16
Std Dev 8.061
Entry
ampl
0
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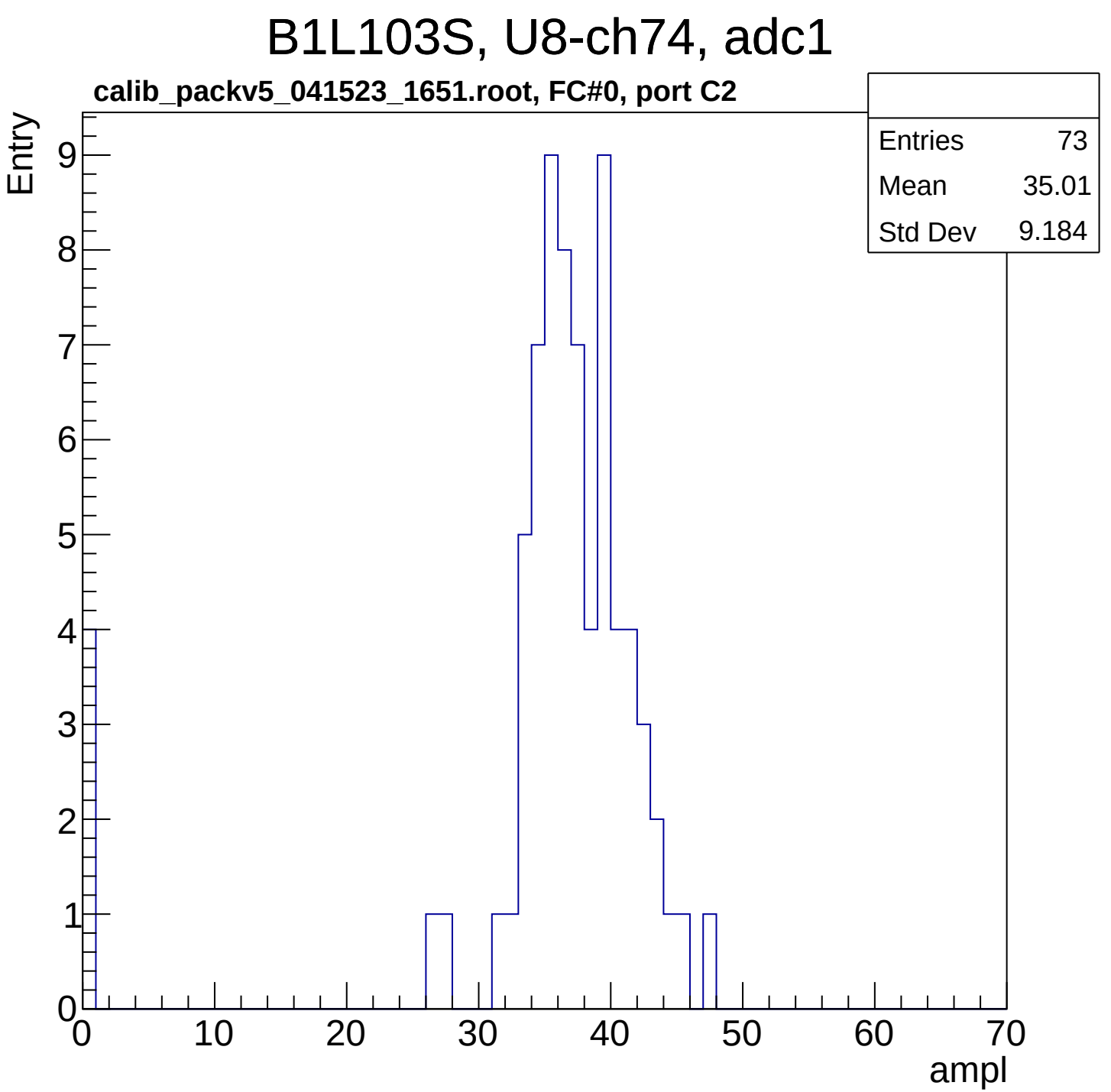
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U8-ch74, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 35.01
Std Dev 9.184
Entry
ampl
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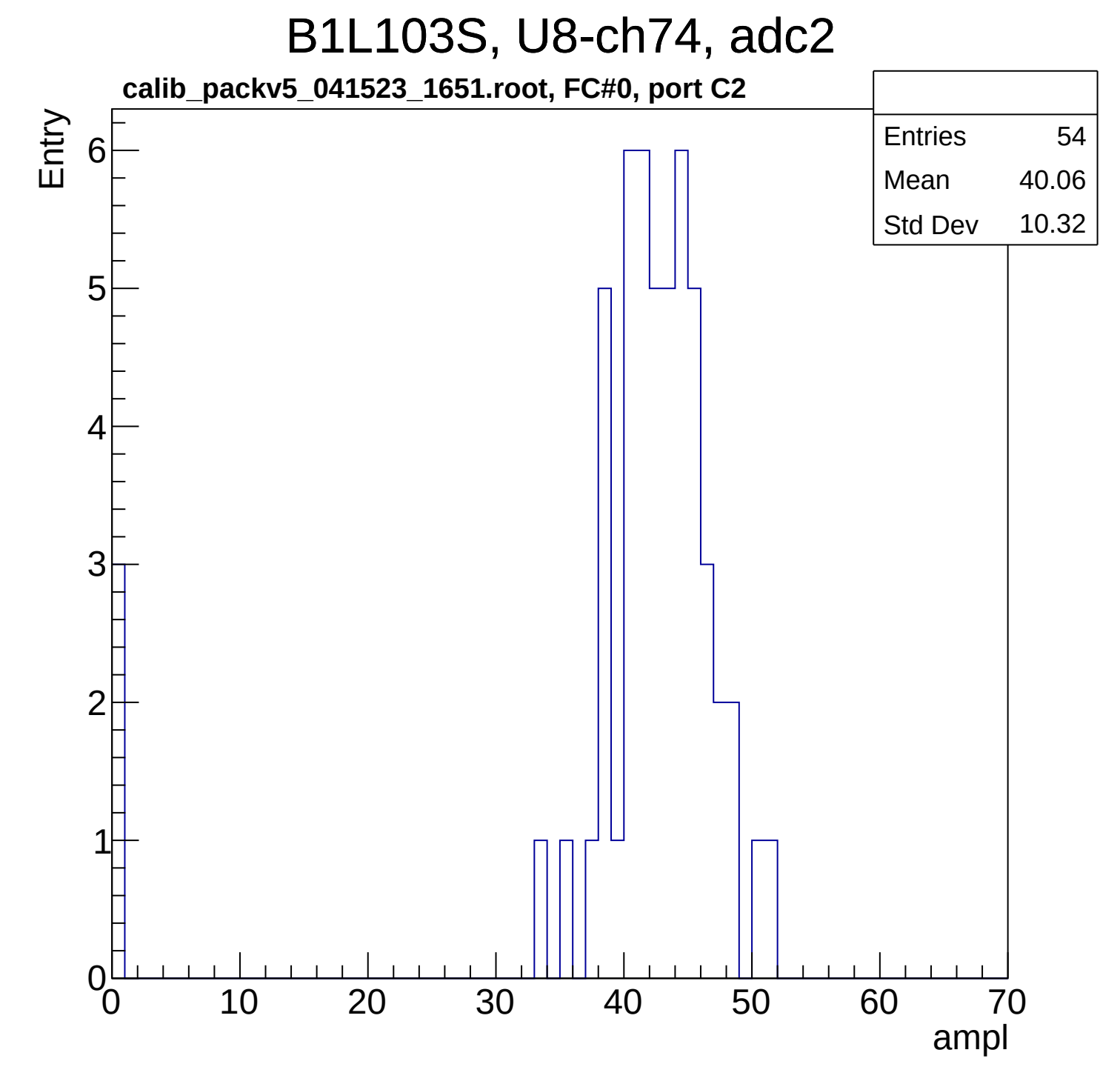
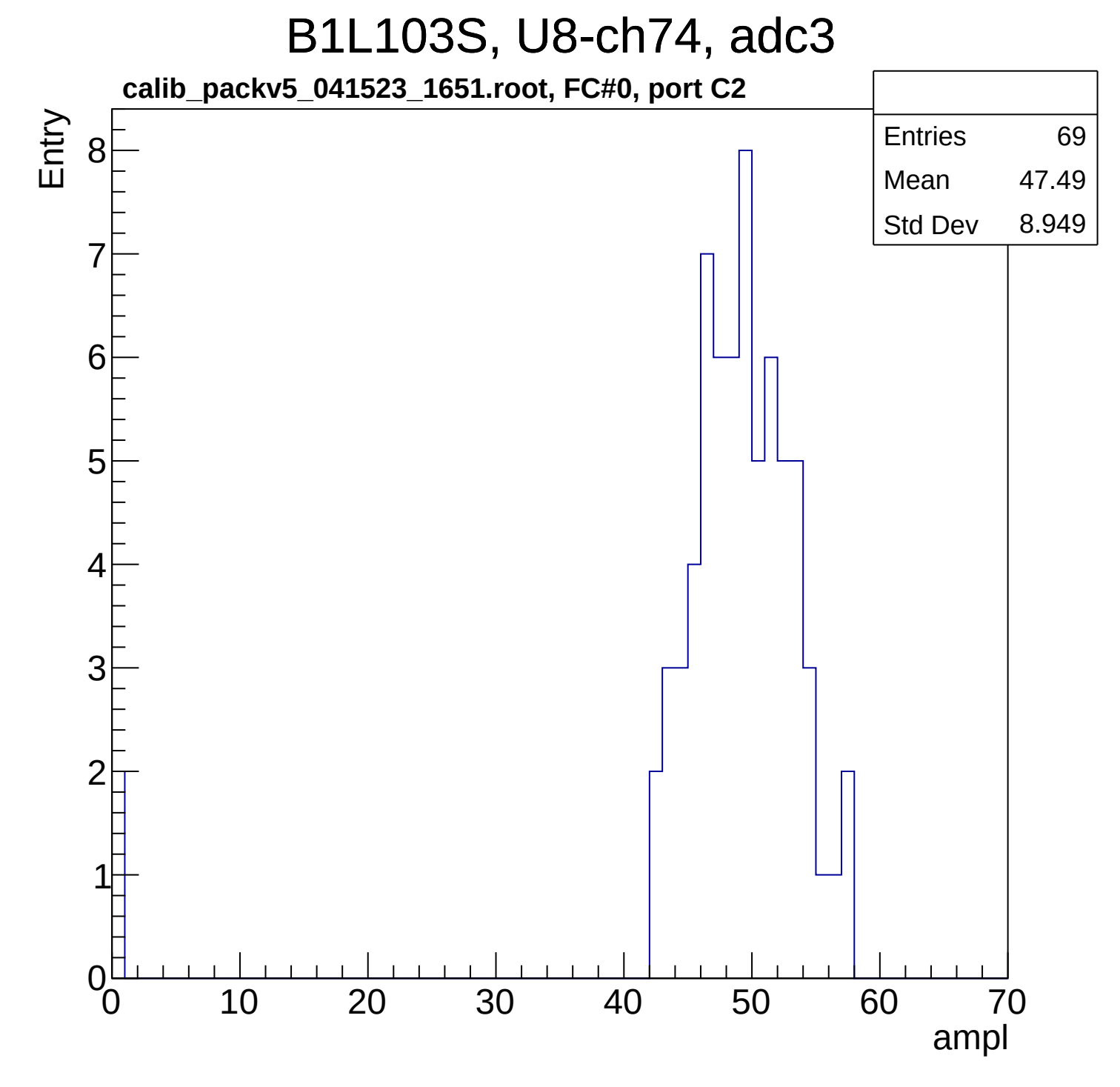
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U8-ch74, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 40.06
Std Dev 10.32
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch74, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 47.49
Std Dev 8.949
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
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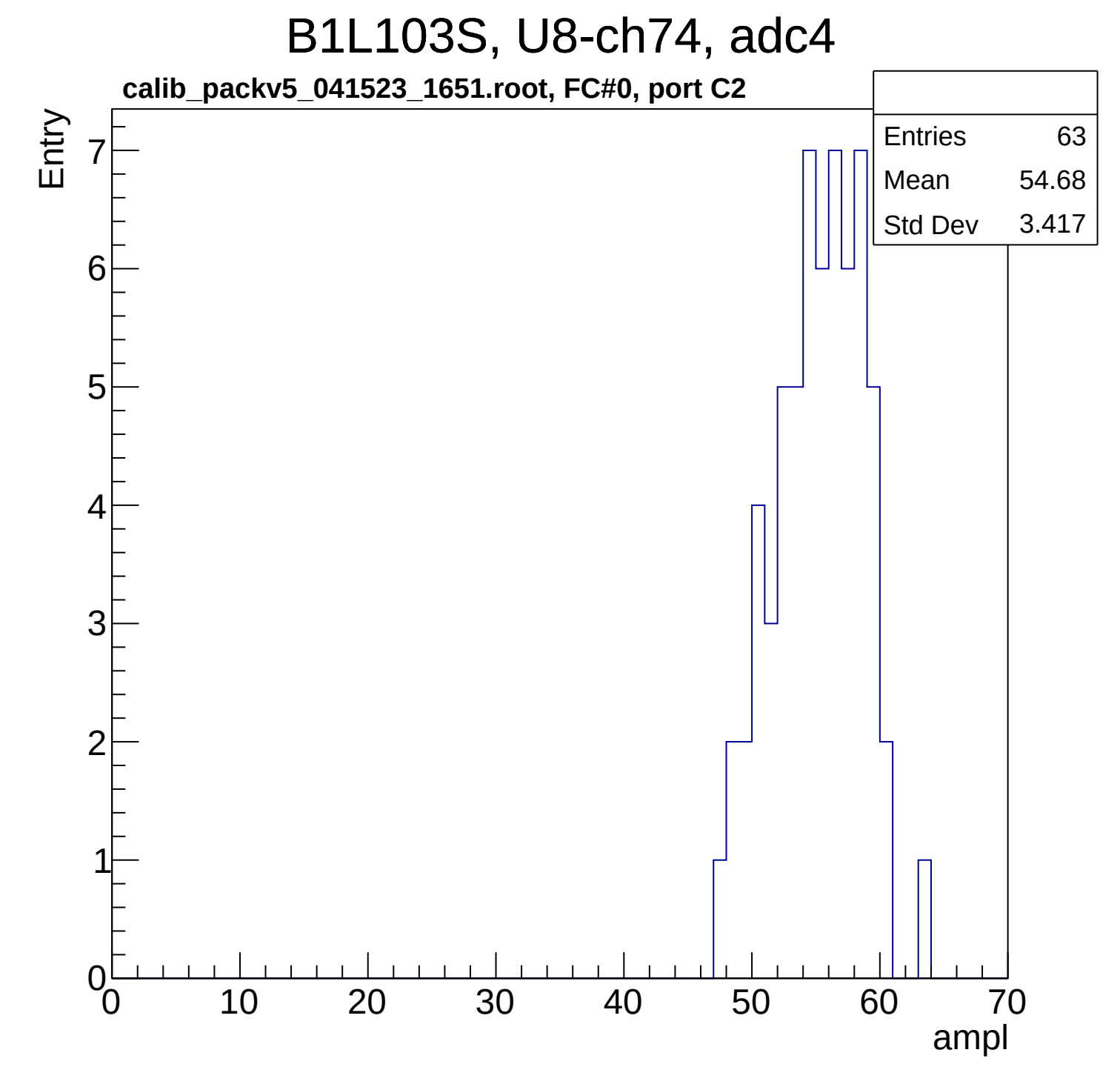
60
70


B1L103S, U8-ch74, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 54.68
Std Dev 3.417
Entry
ampl
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2
3
4
5
6
7
0
10
20
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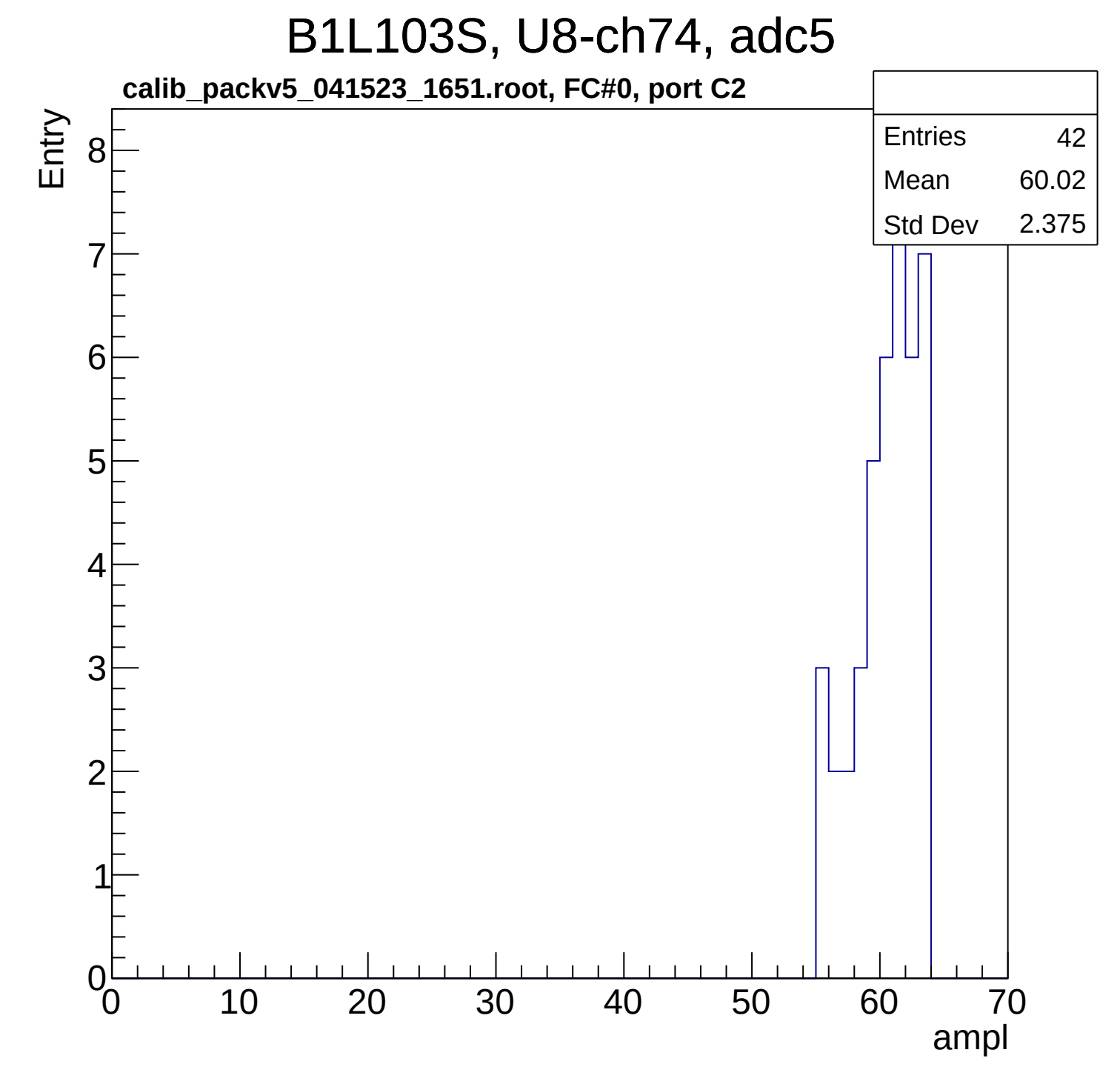
40
50
60
70


B1L103S, U8-ch74, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 60.02
Std Dev 2.375
Entry
ampl
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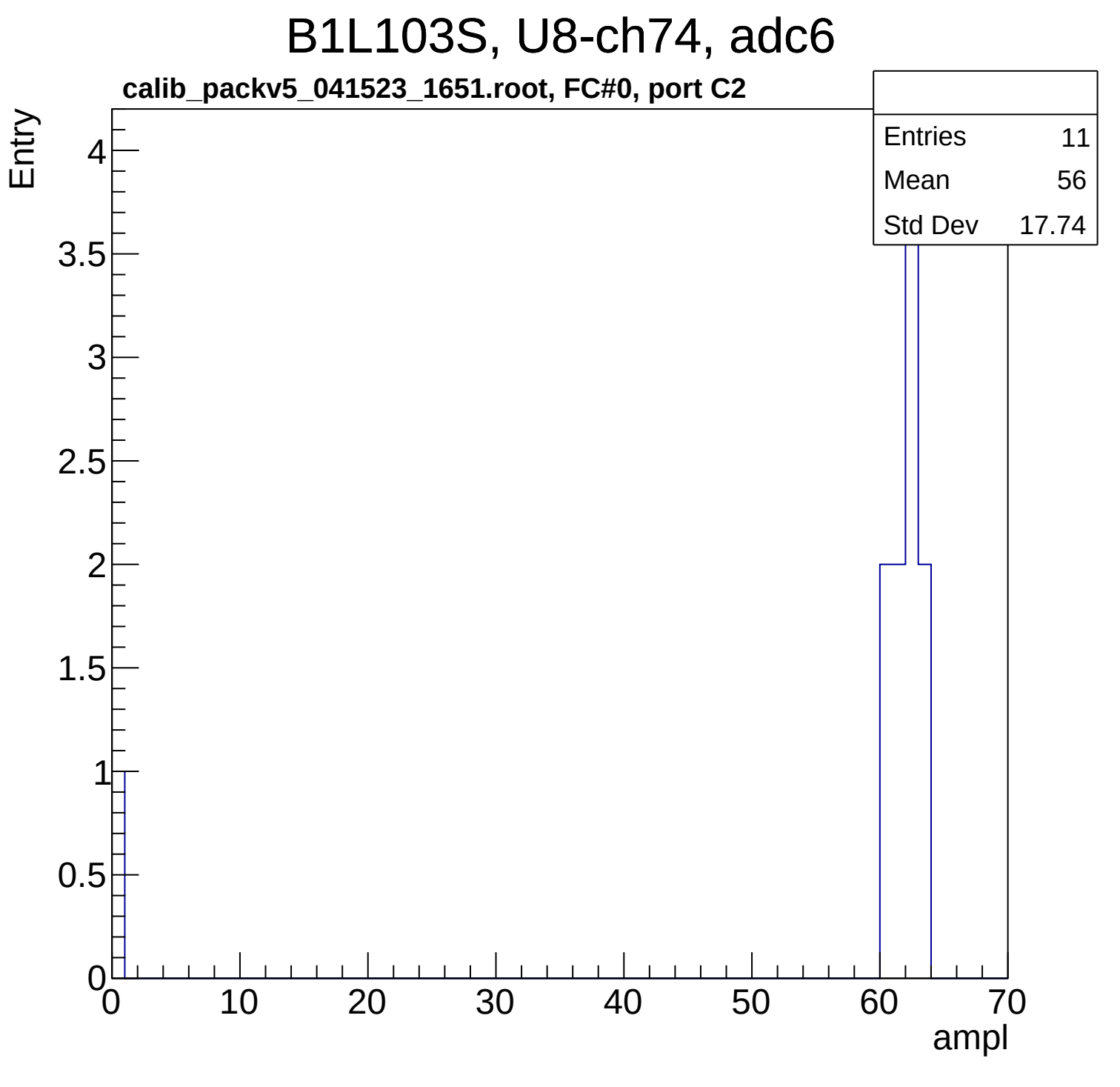
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch74, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 56
Std Dev 17.74
Entry
ampl
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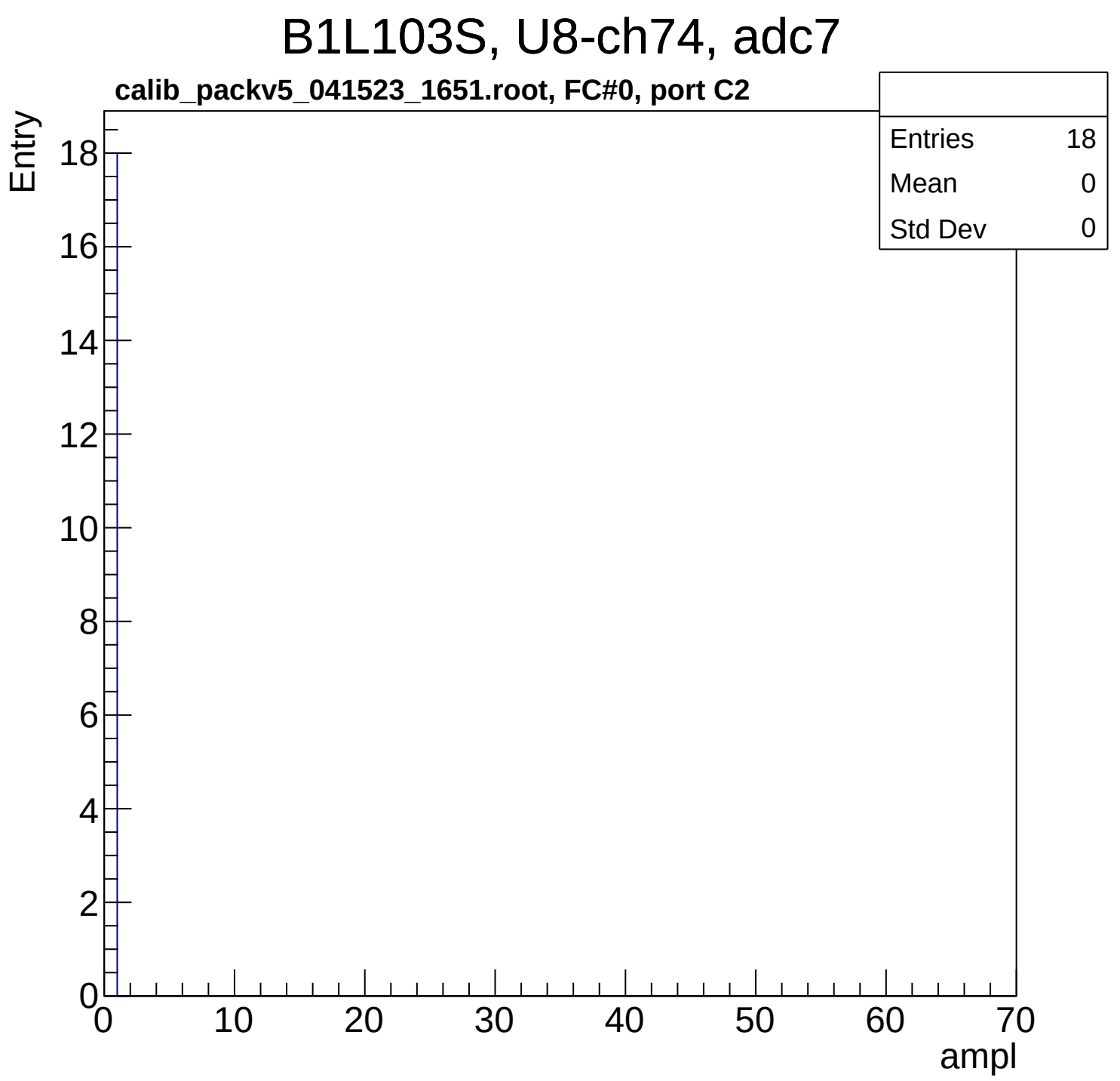
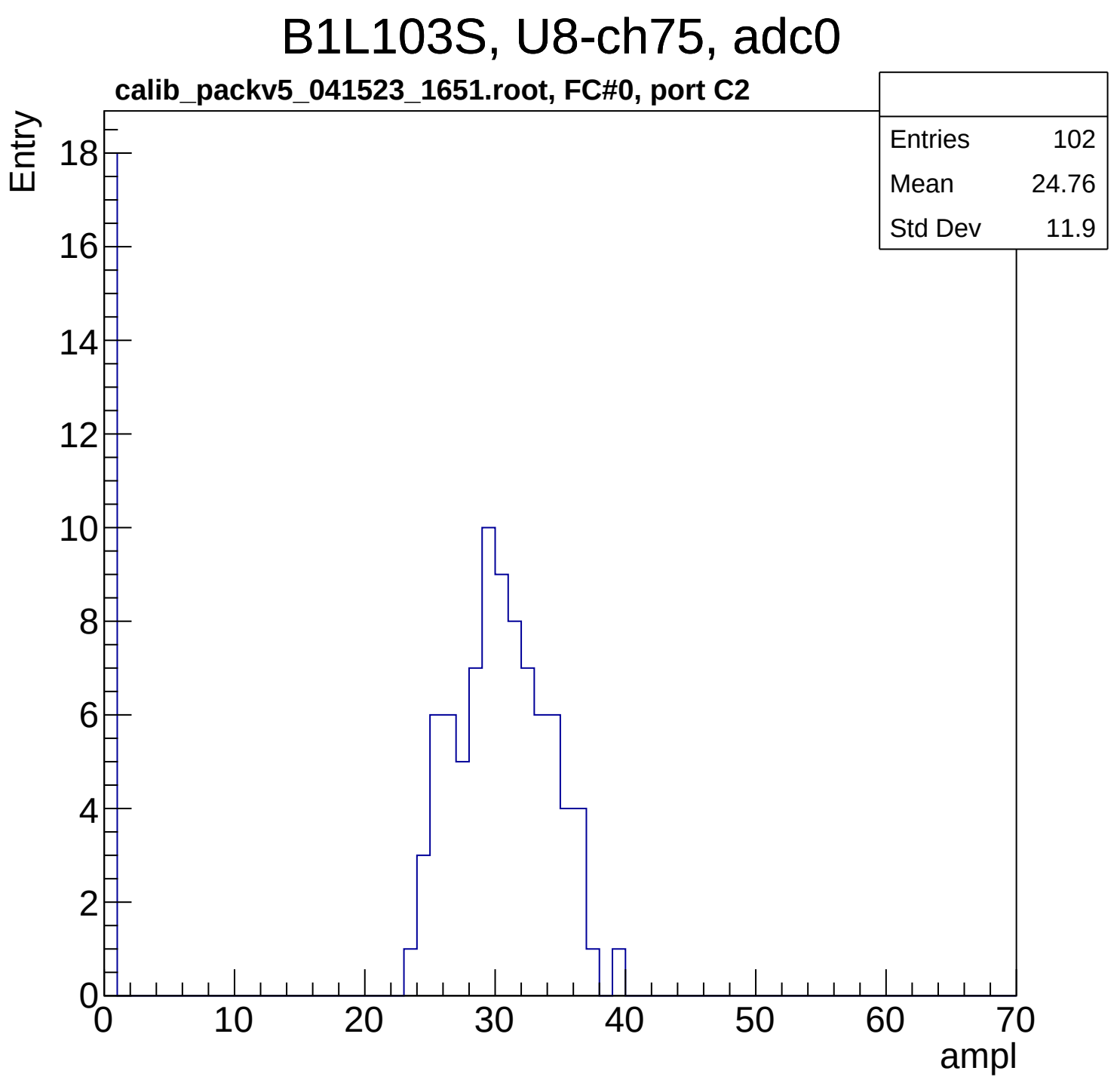
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U8-ch74, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch75, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 102
Mean 24.76
Std Dev 11.9
Entry
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8
10
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50
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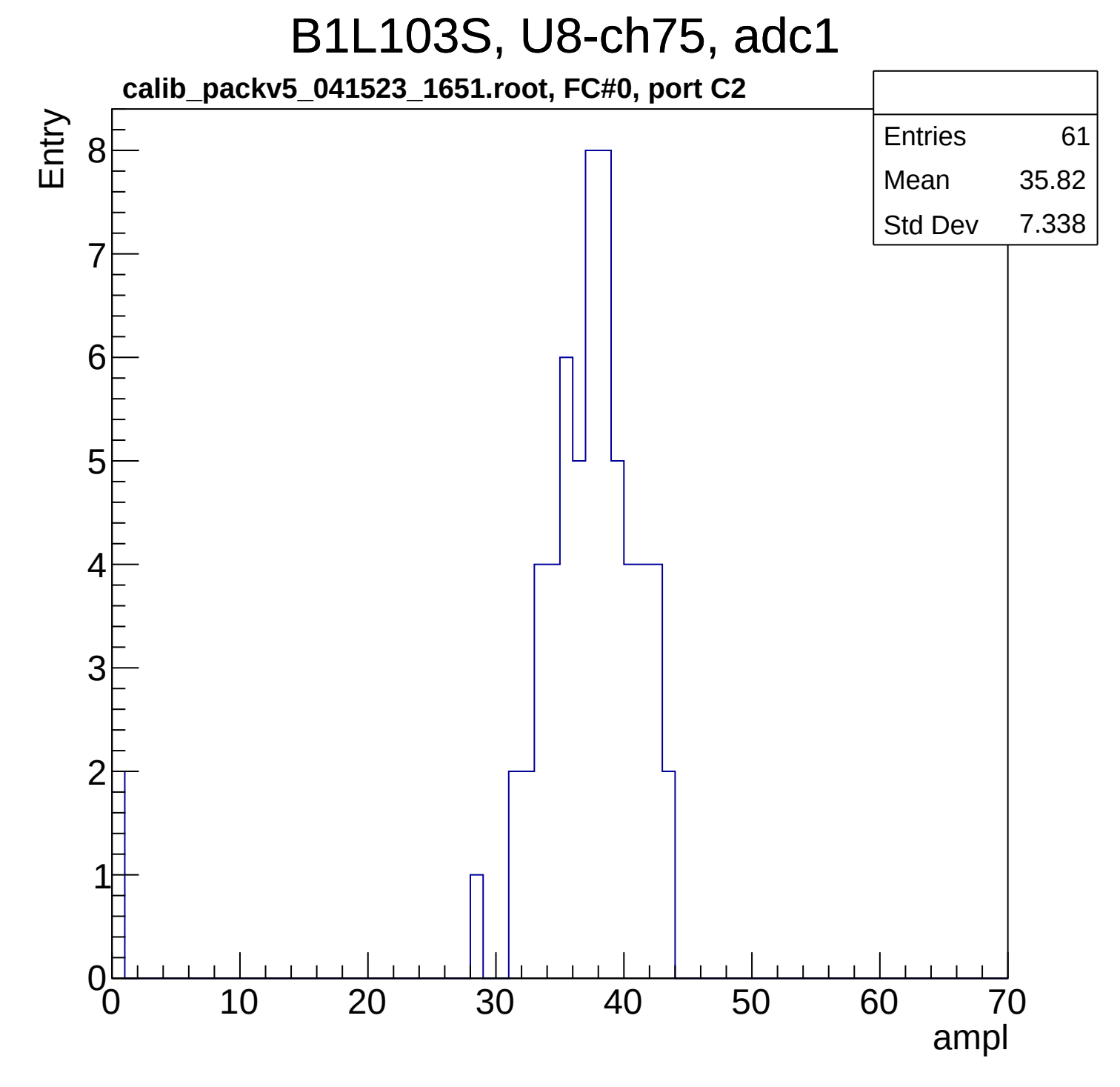
70
ampl


B1L103S, U8-ch75, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 35.82
Std Dev 7.338
Entry
ampl
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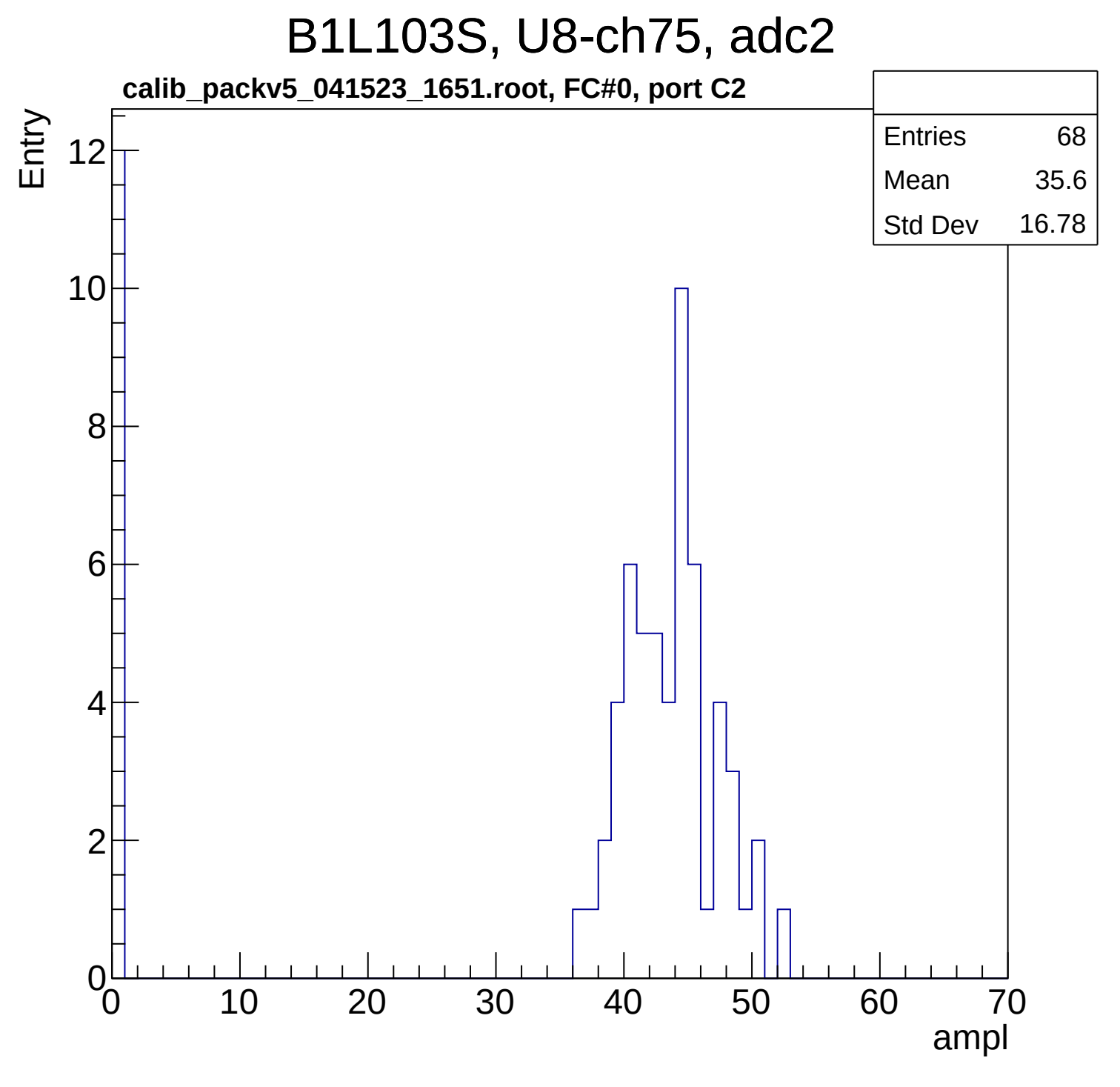
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch75, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 35.6
Std Dev 16.78
Entry
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10
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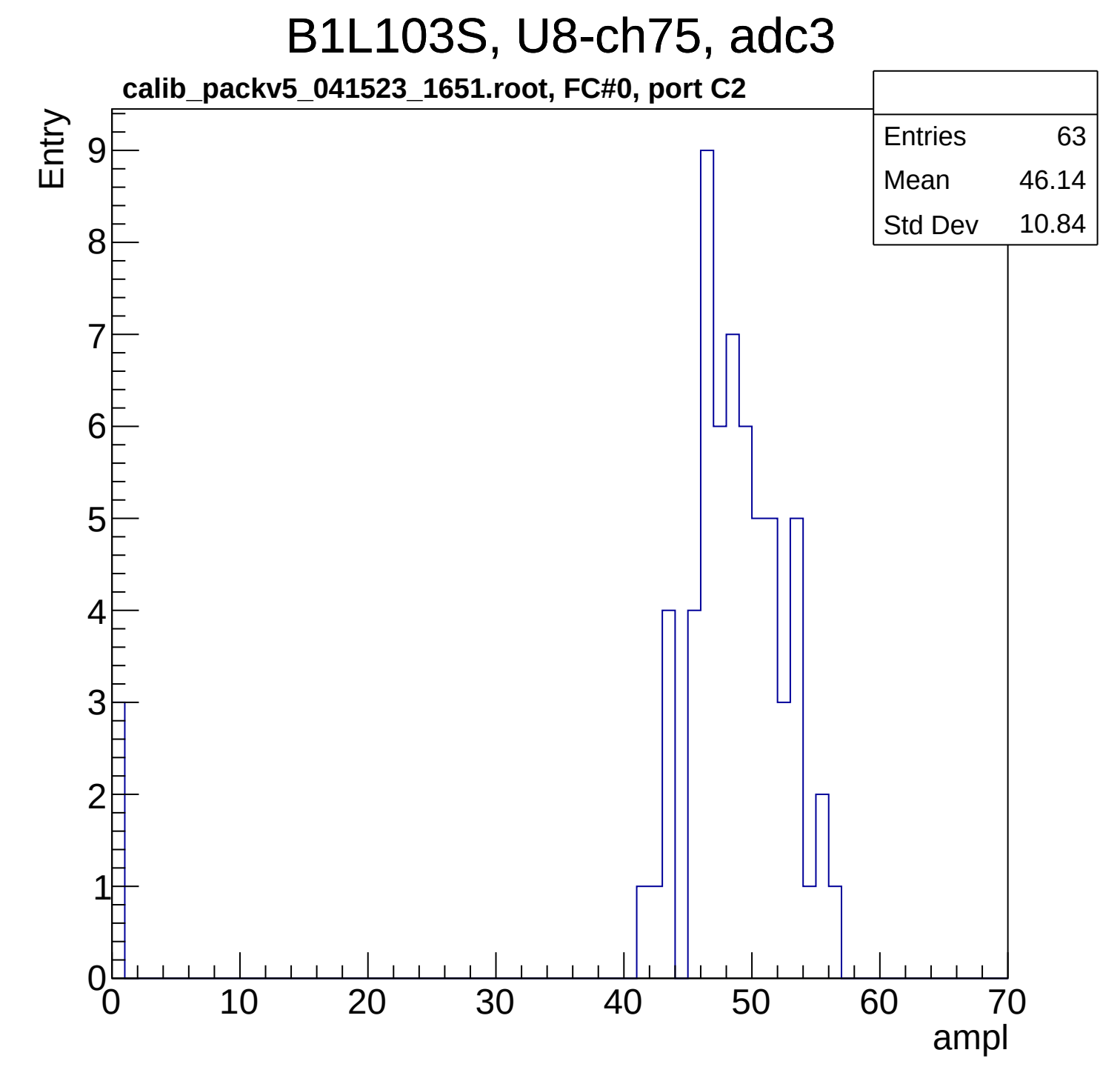
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch75, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 46.14
Std Dev 10.84
Entry
ampl
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2
3
4
5
6
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8
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0
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60
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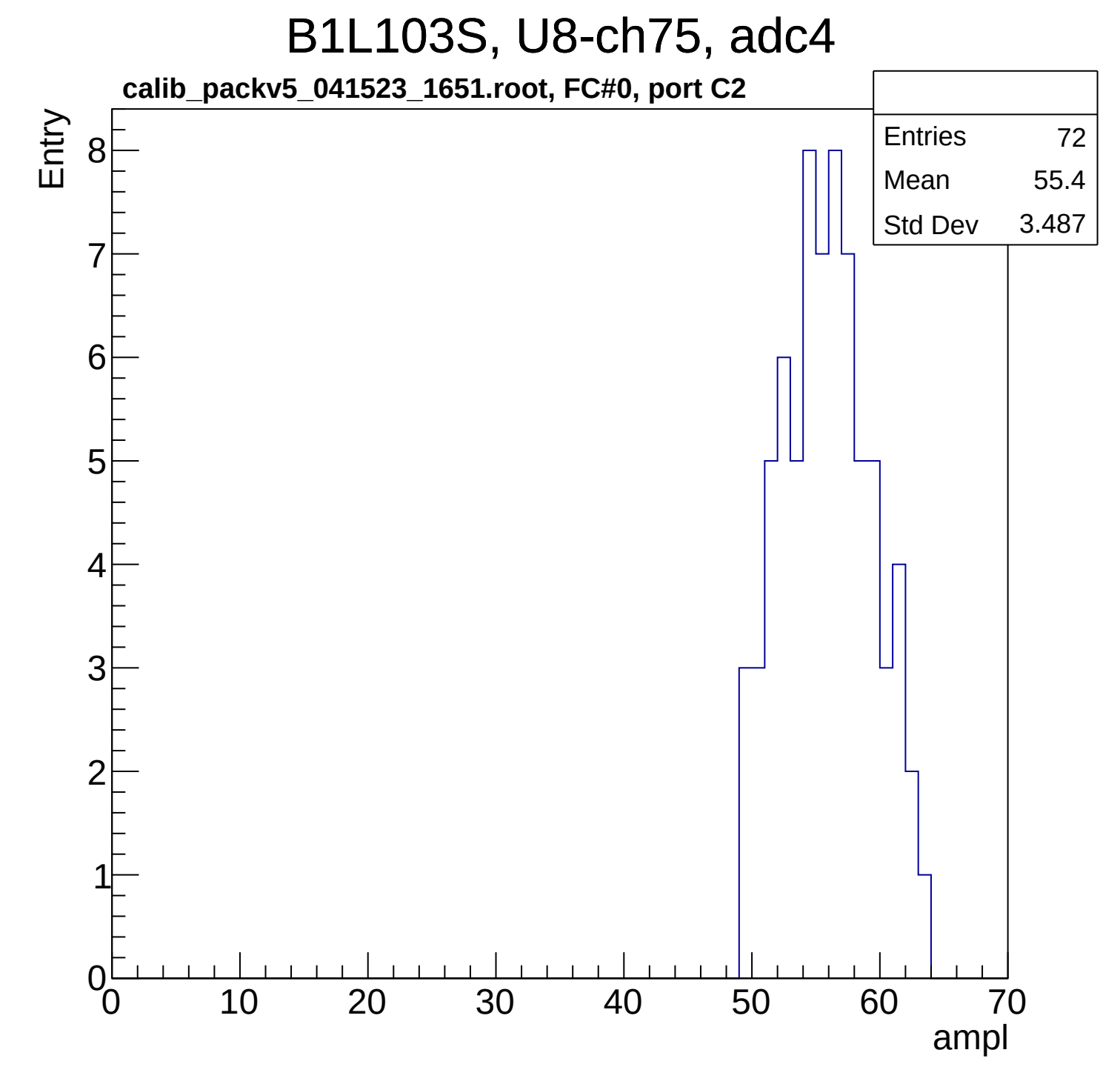
B1L103S, U8-ch75, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 55.4
Std Dev 3.487
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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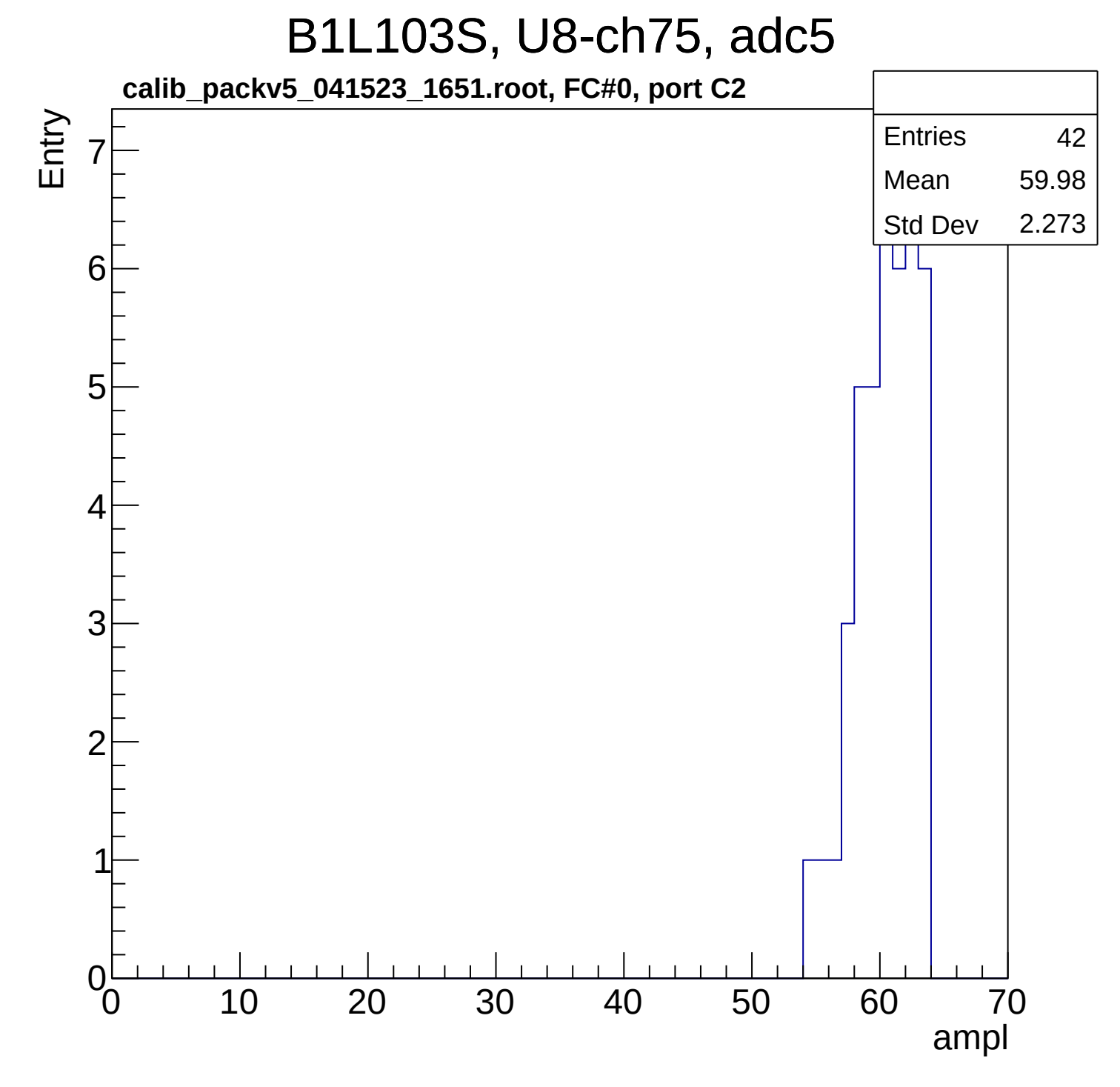
B1L103S, U8-ch75, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 59.98
Std Dev 2.273
Entry
ampl
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1
2
3
4
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6
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0
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40
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60
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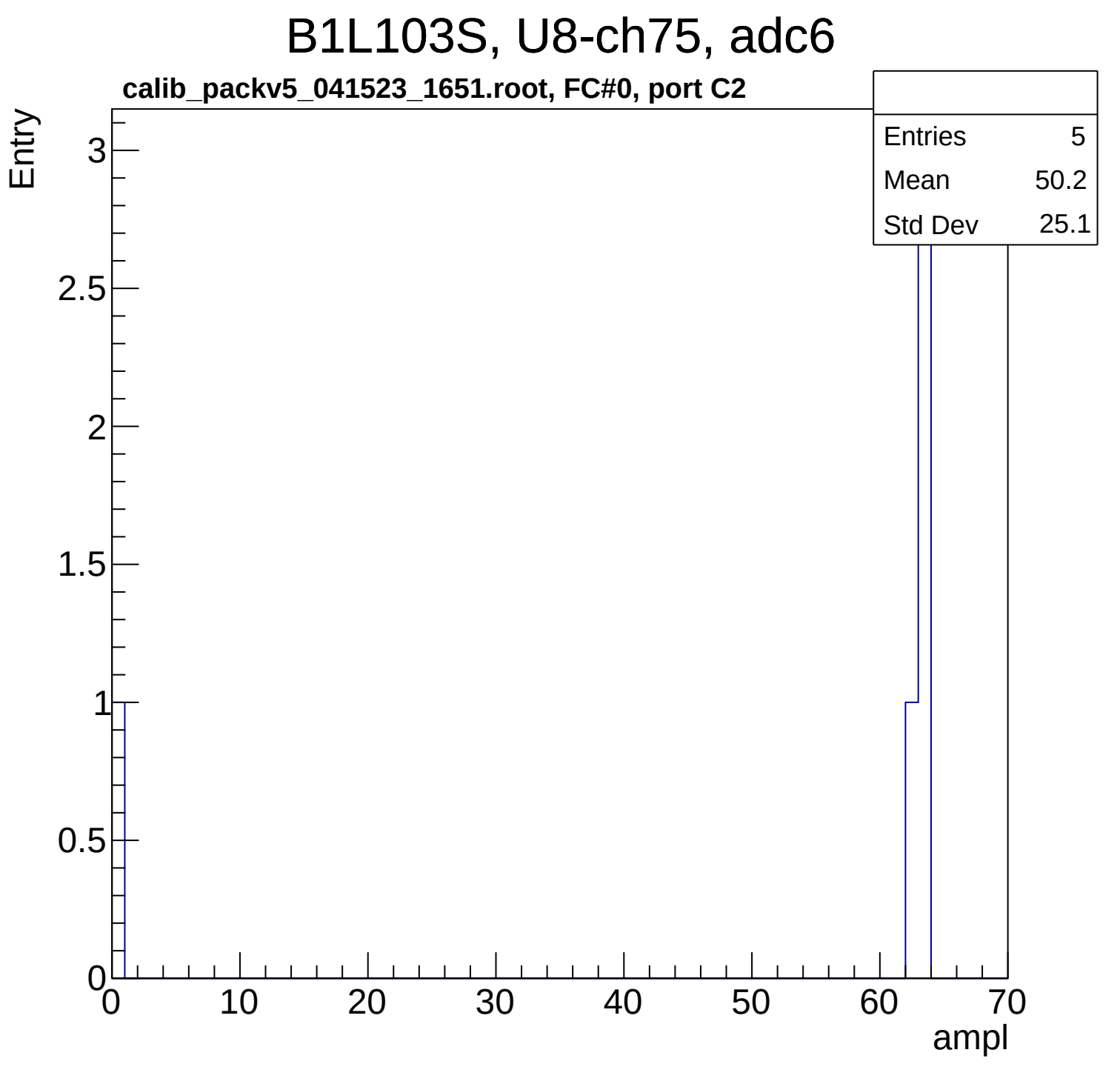
B1L103S, U8-ch75, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 50.2
Std Dev 25.1
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
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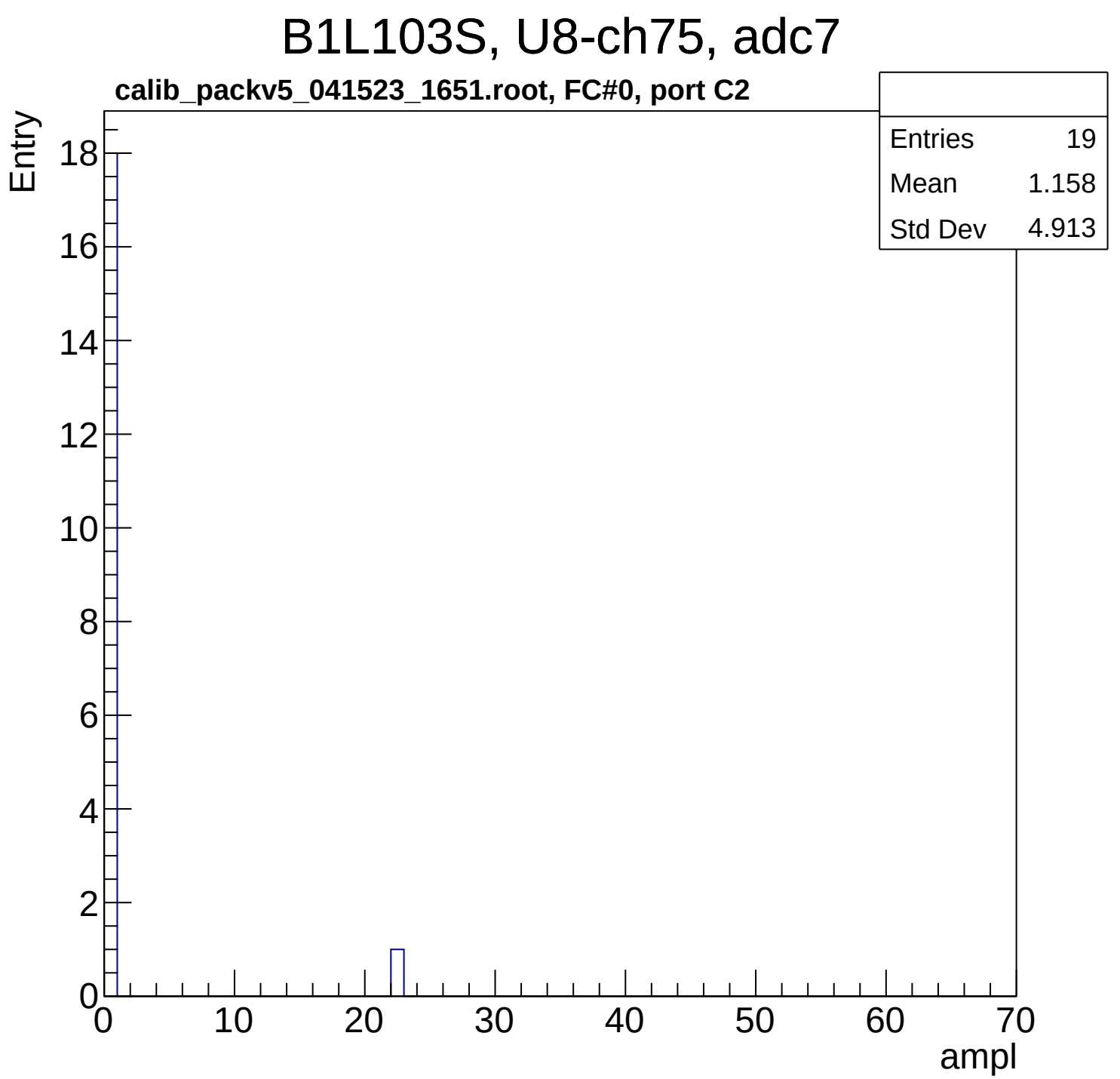
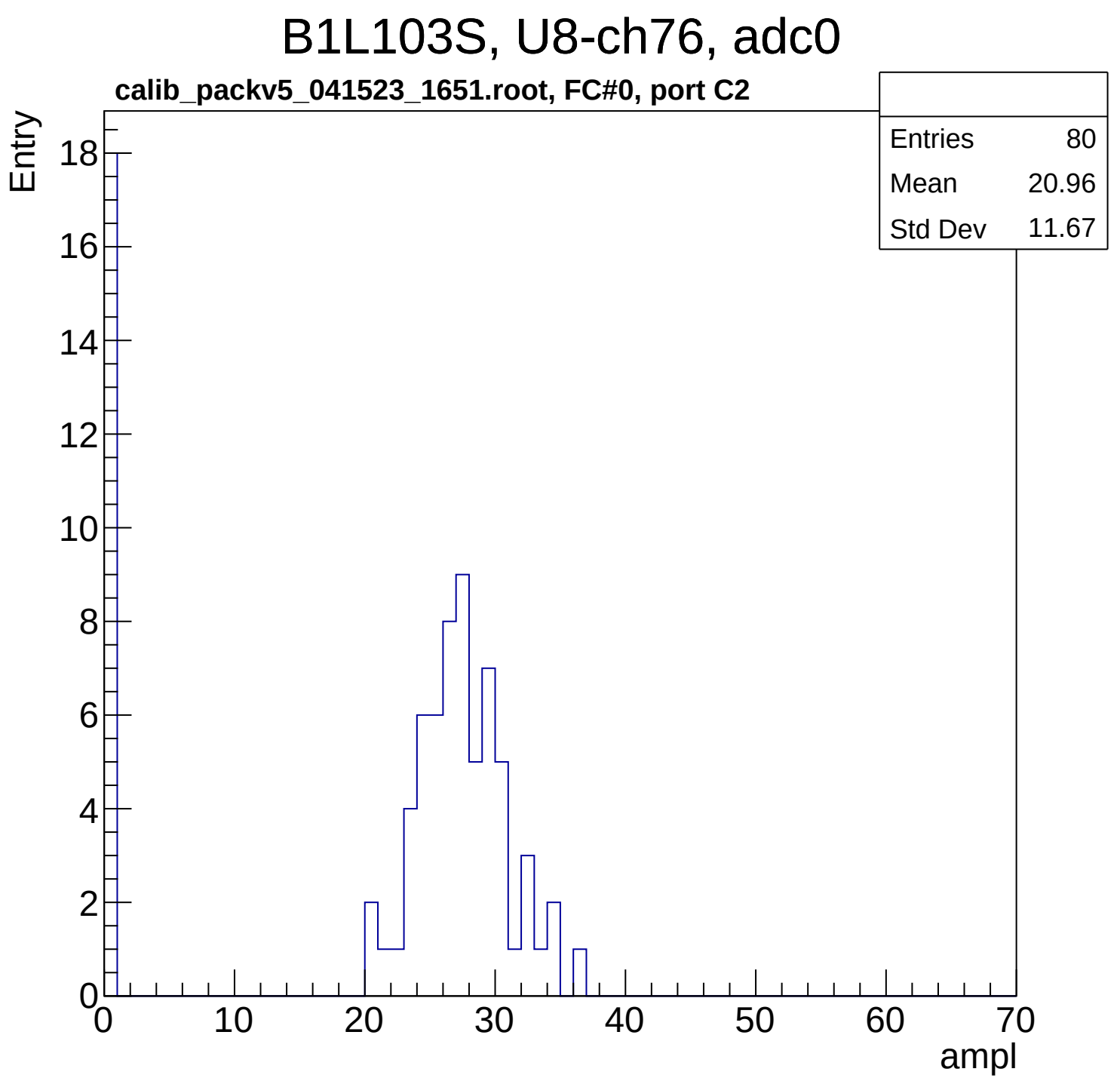

B1L103S, U8-ch75, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.158
Std Dev 4.913
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch76, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 20.96
Std Dev 11.67
Entry
0
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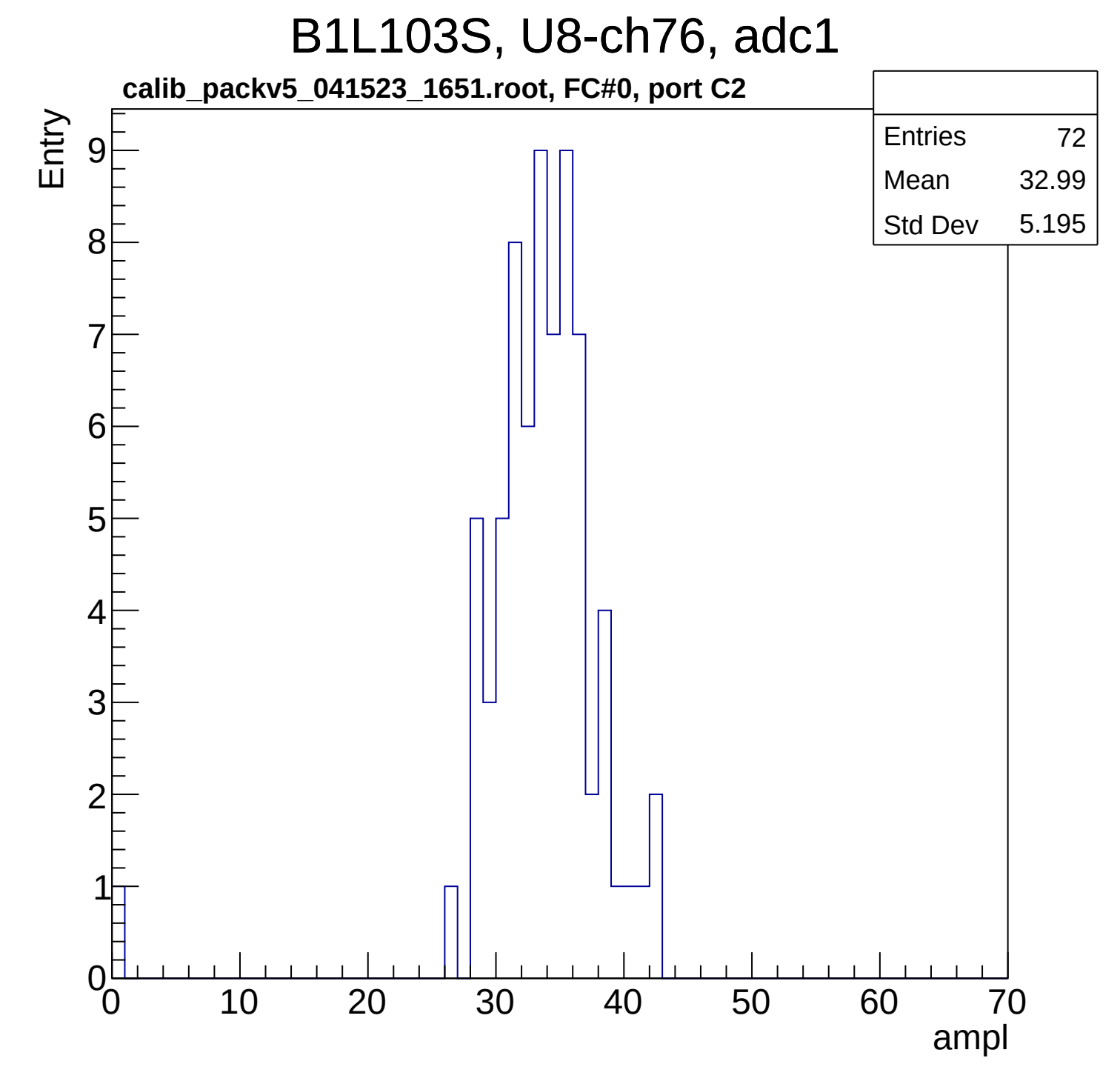
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch76, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 32.99
Std Dev 5.195
Entry
ampl
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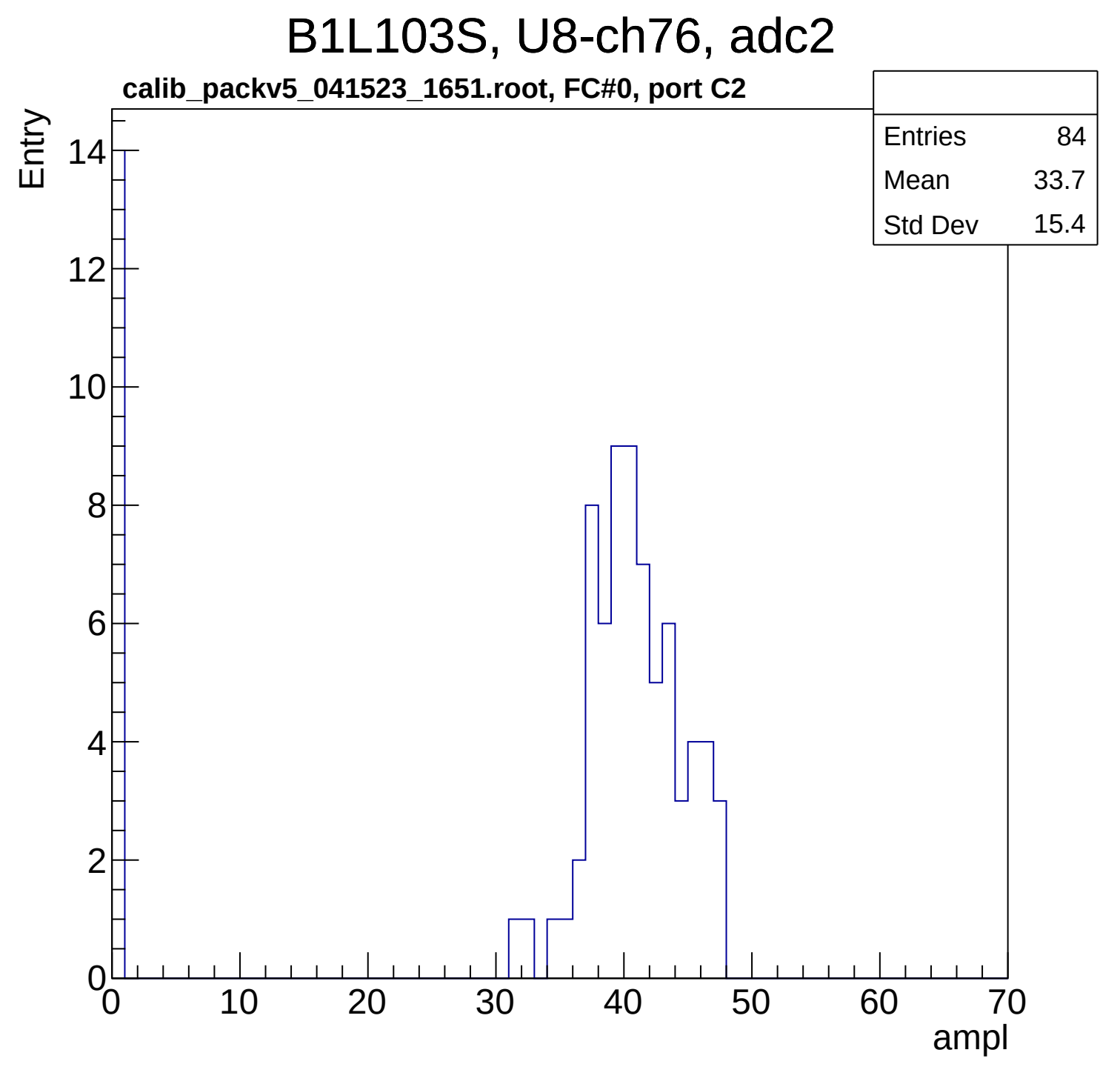
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U8-ch76, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 33.7
Std Dev 15.4
Entry
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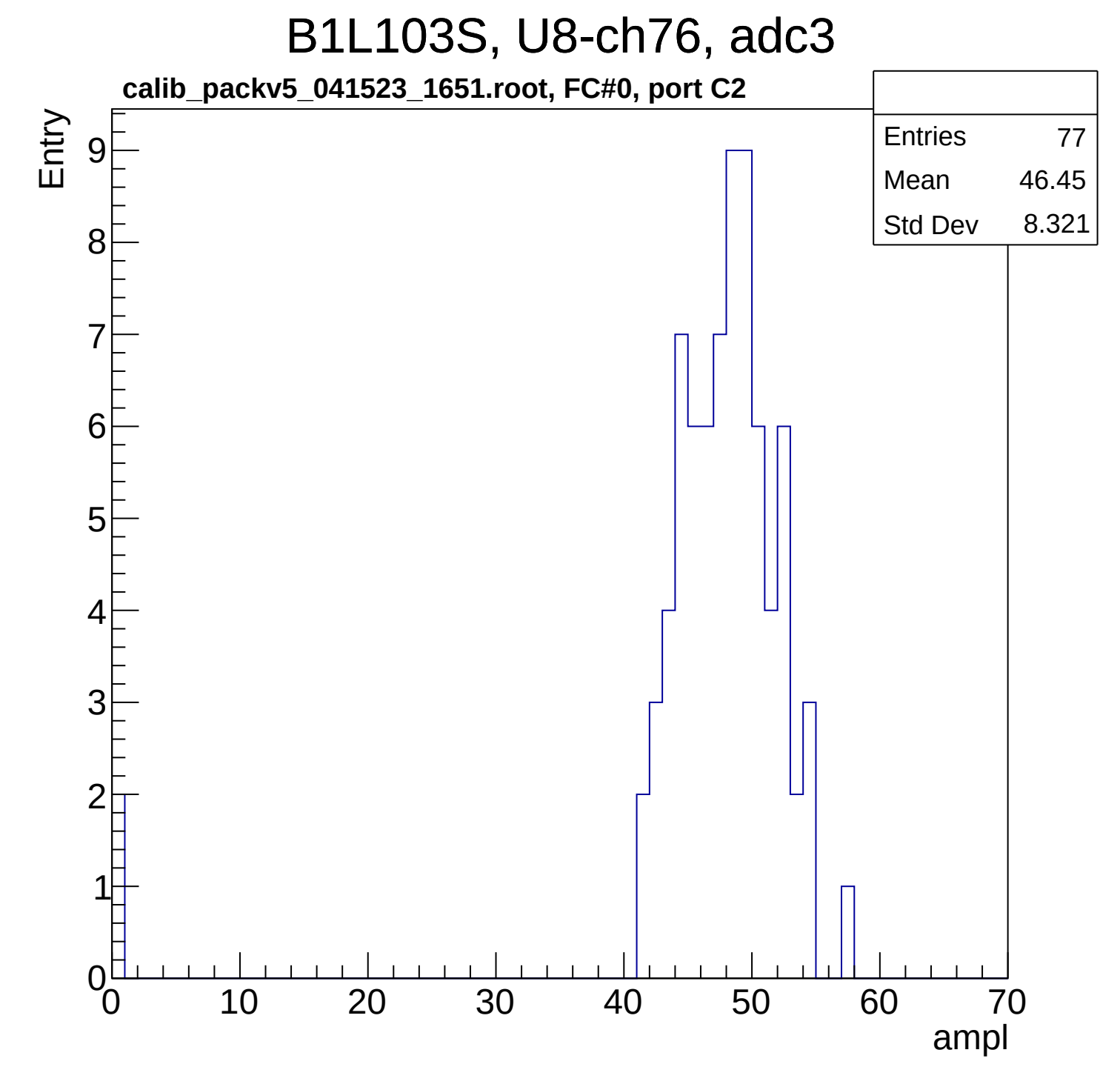
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch76, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 46.45
Std Dev 8.321
Entry
ampl
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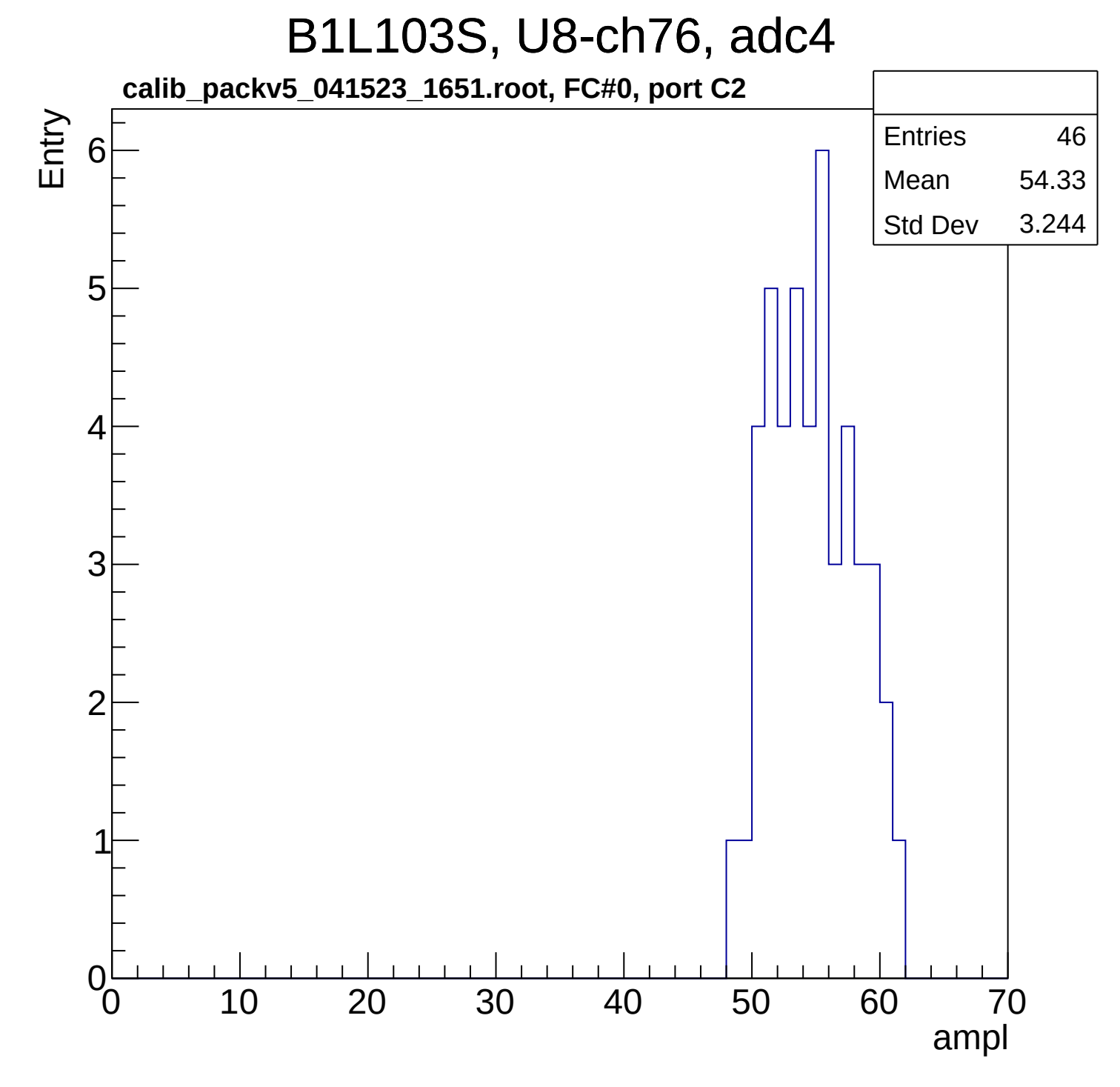
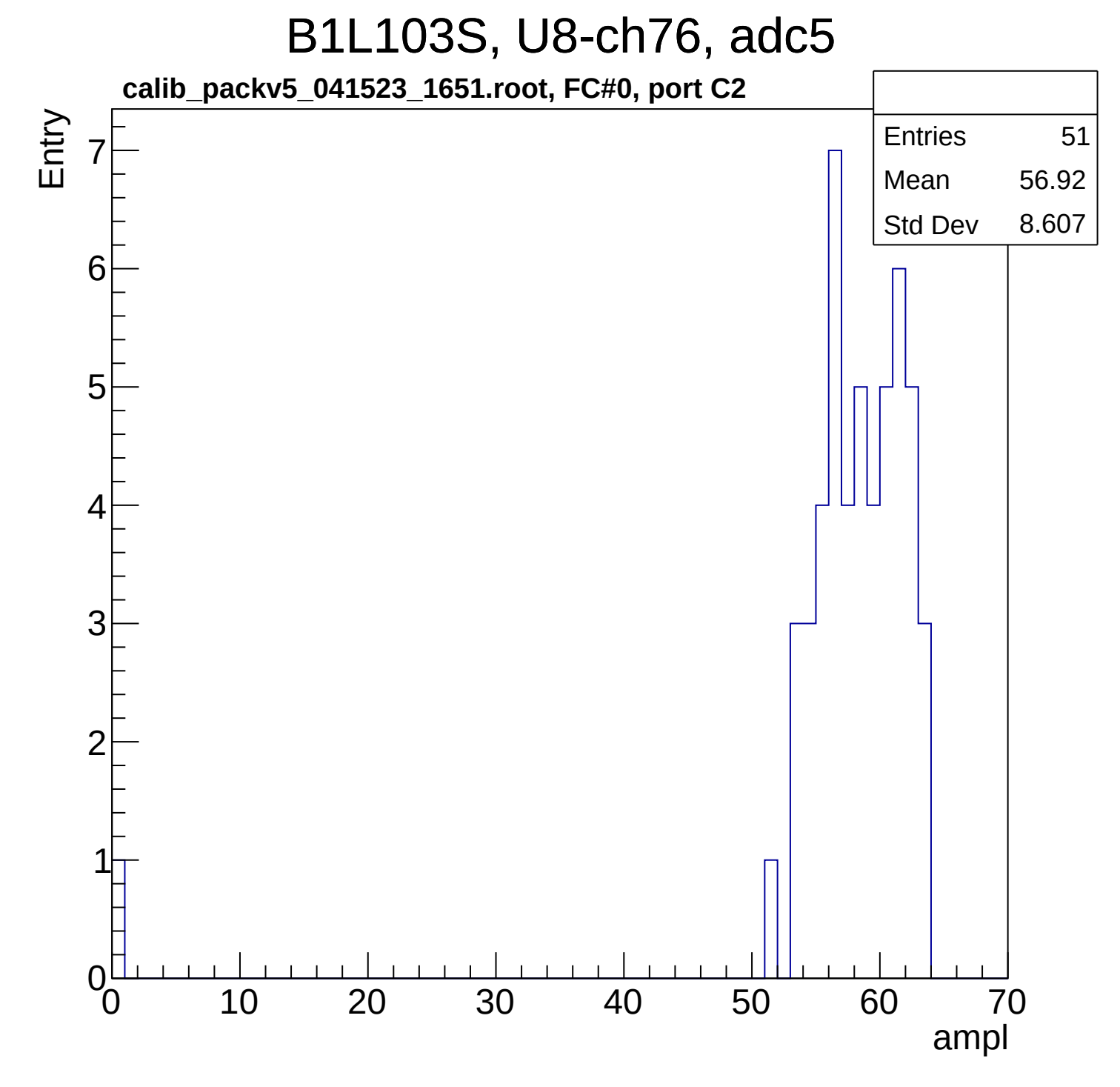
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U8-ch76, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 54.33
Std Dev 3.244
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U8-ch76, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 56.92
Std Dev 8.607
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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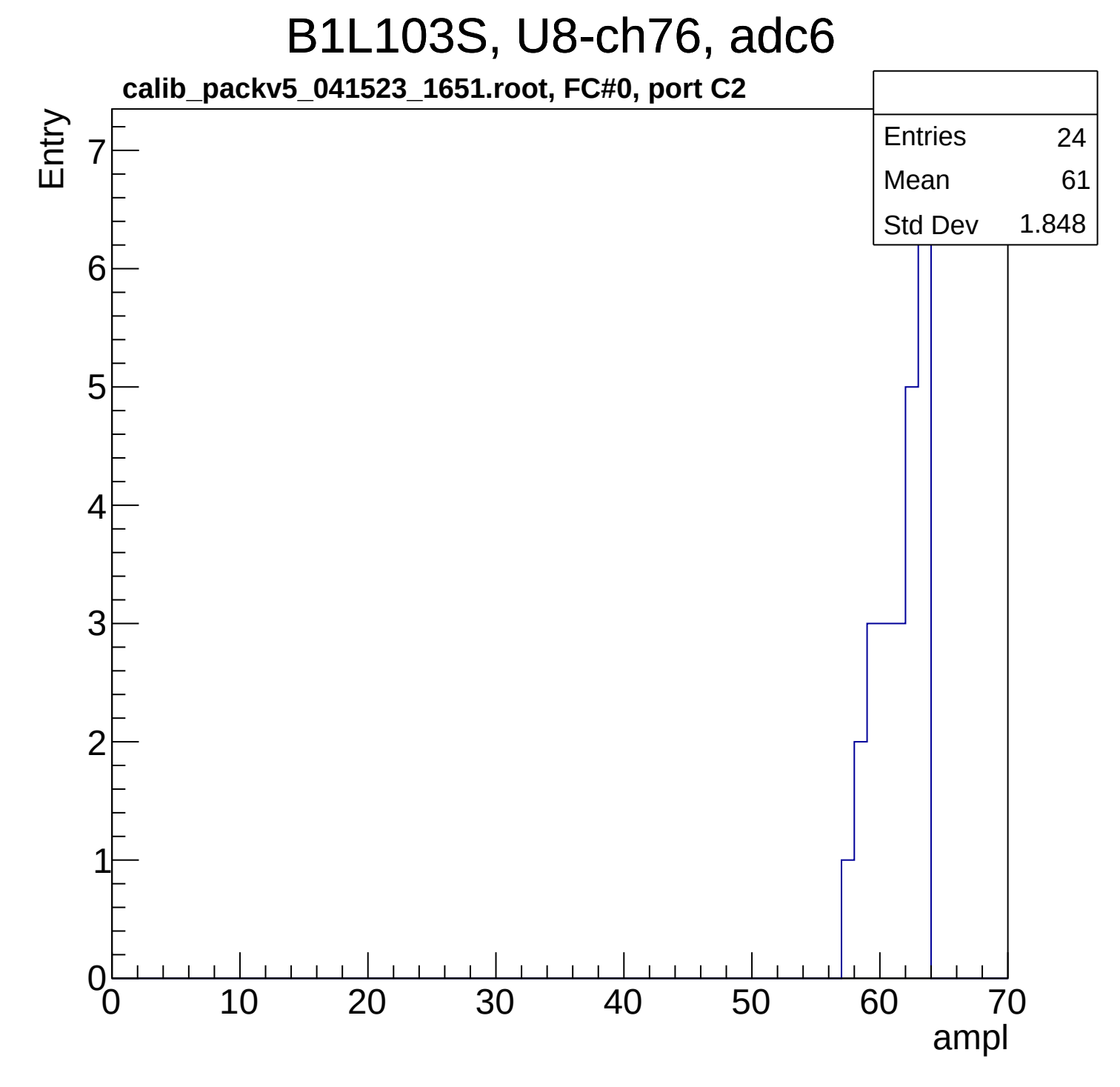
B1L103S, U8-ch76, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 61
Std Dev 1.848
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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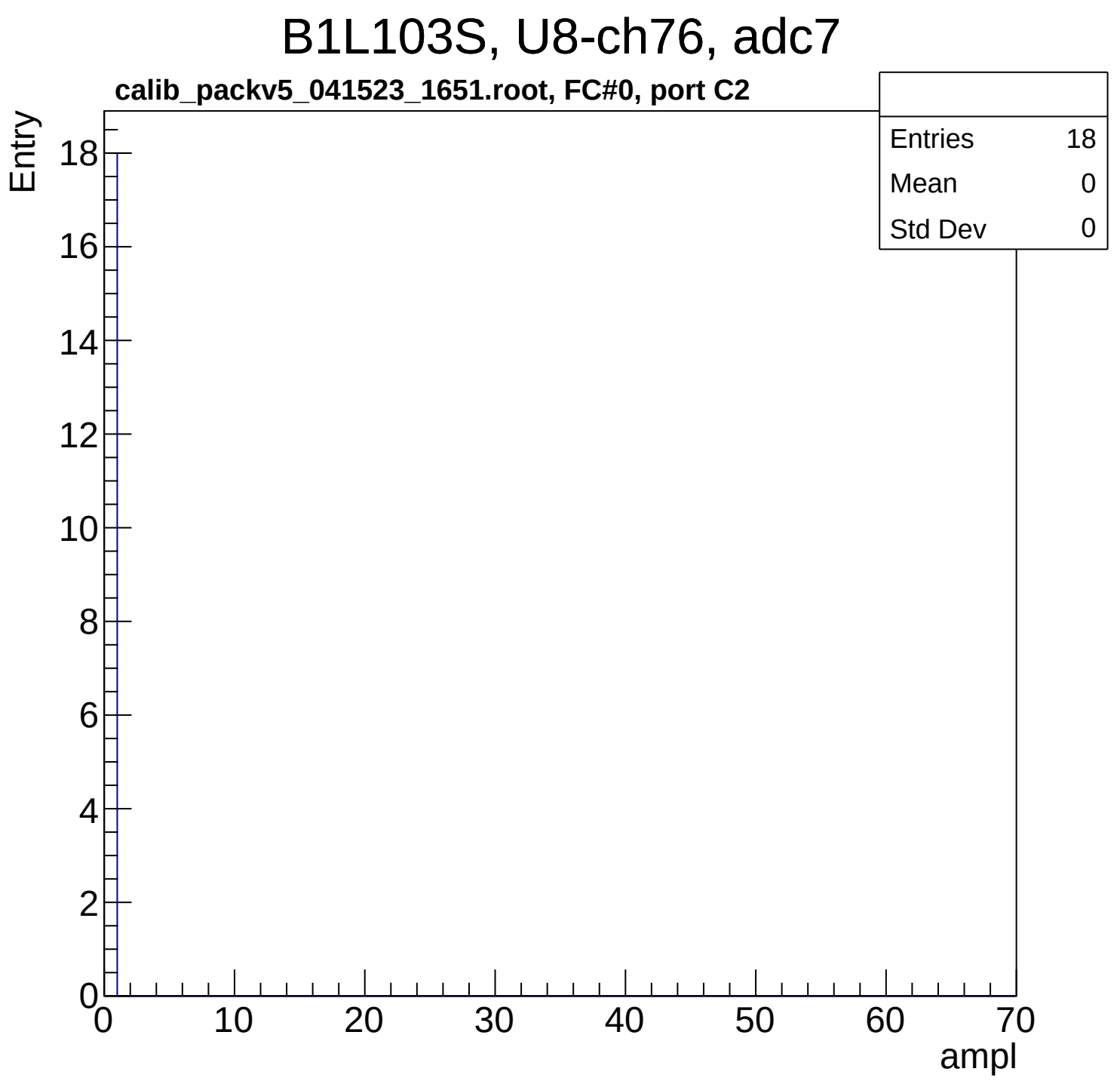
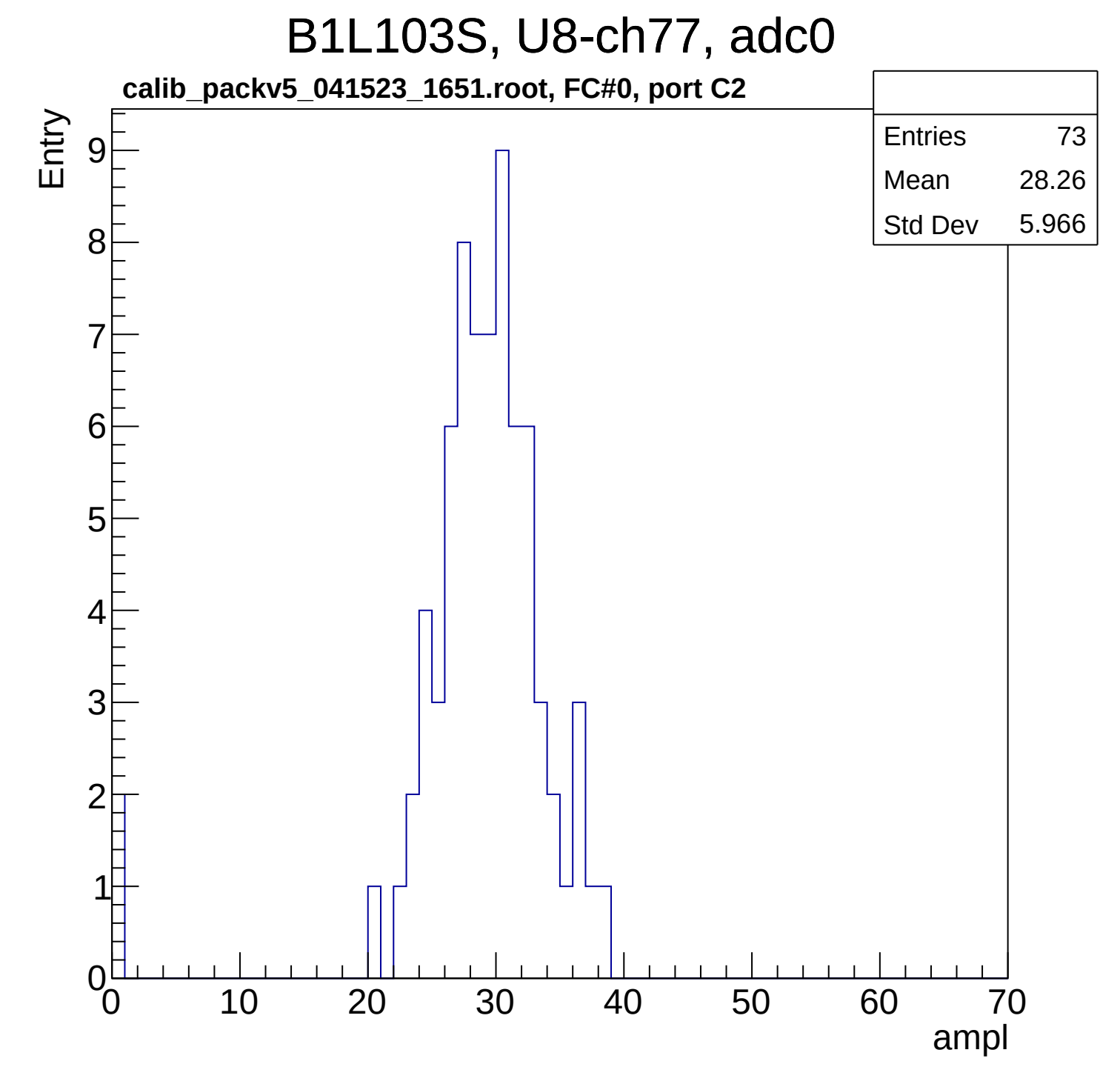

B1L103S, U8-ch76, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch77, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 28.26
Std Dev 5.966
Entry
ampl
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3
4
5
6
7
8
9
0
10
20
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60
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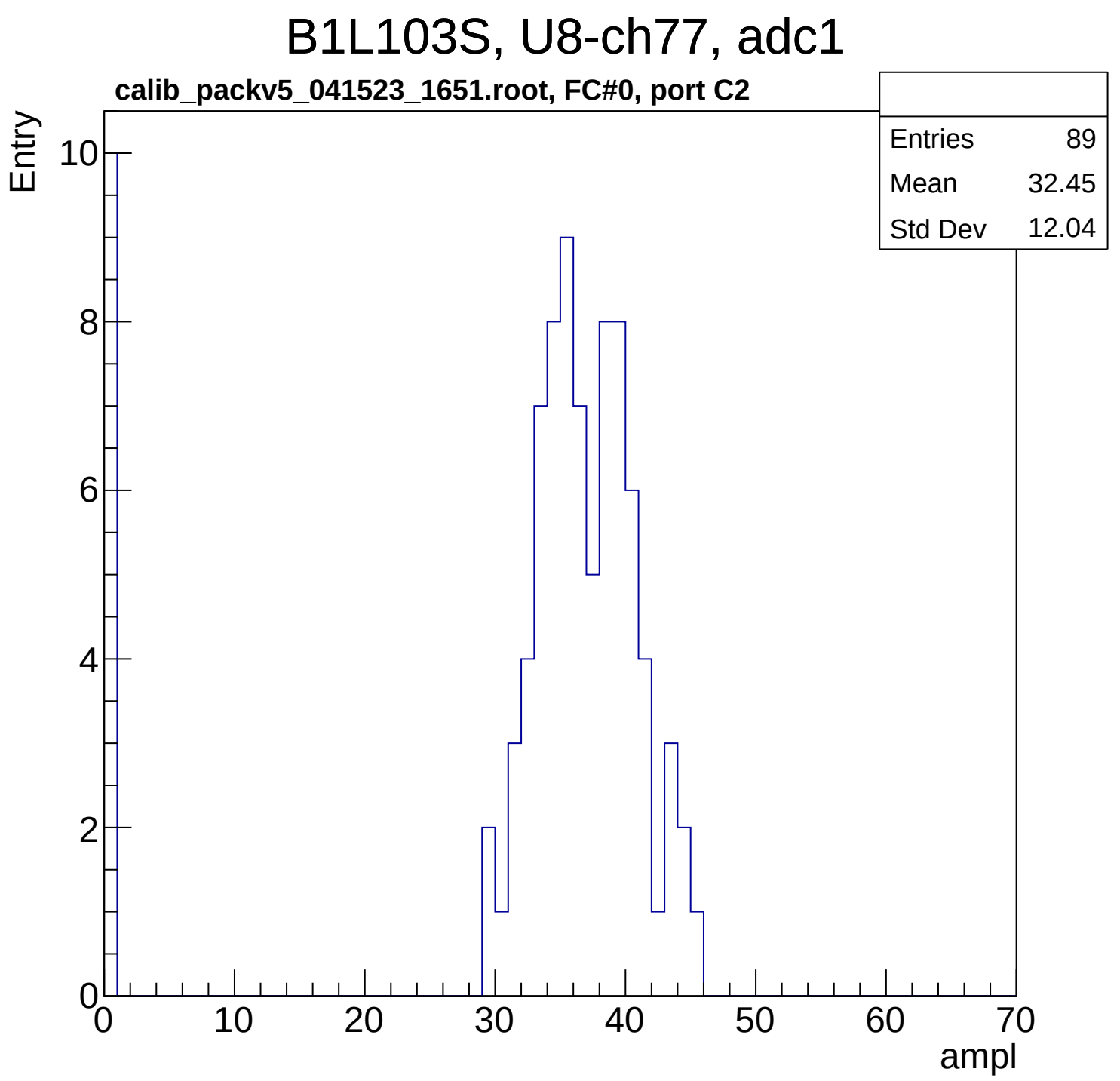
B1L103S, U8-ch77, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 32.45
Std Dev 12.04
Entry
ampl
0
2
4
6
8
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0
10
20
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40
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60
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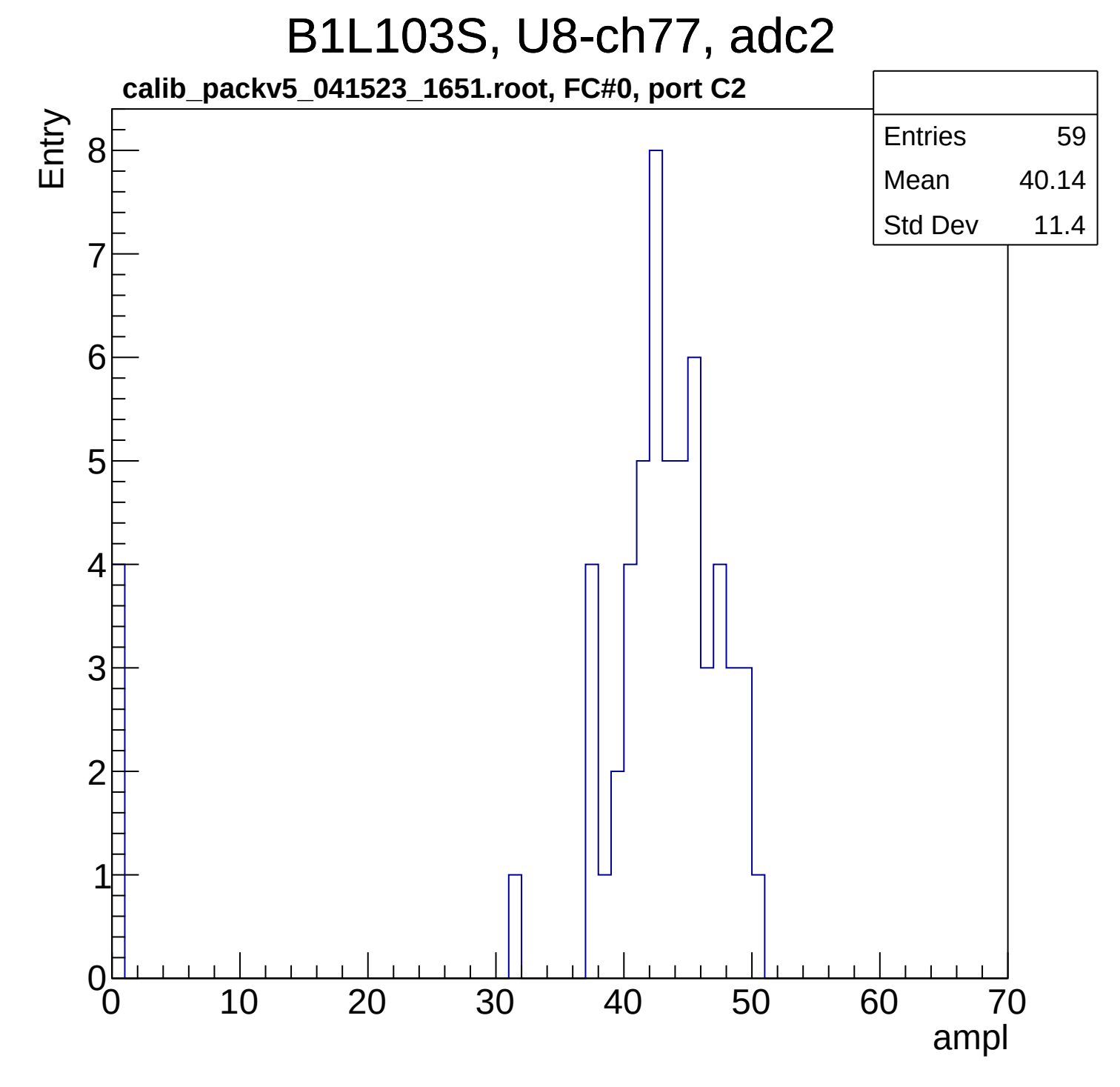
B1L103S, U8-ch77, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 40.14
Std Dev 11.4
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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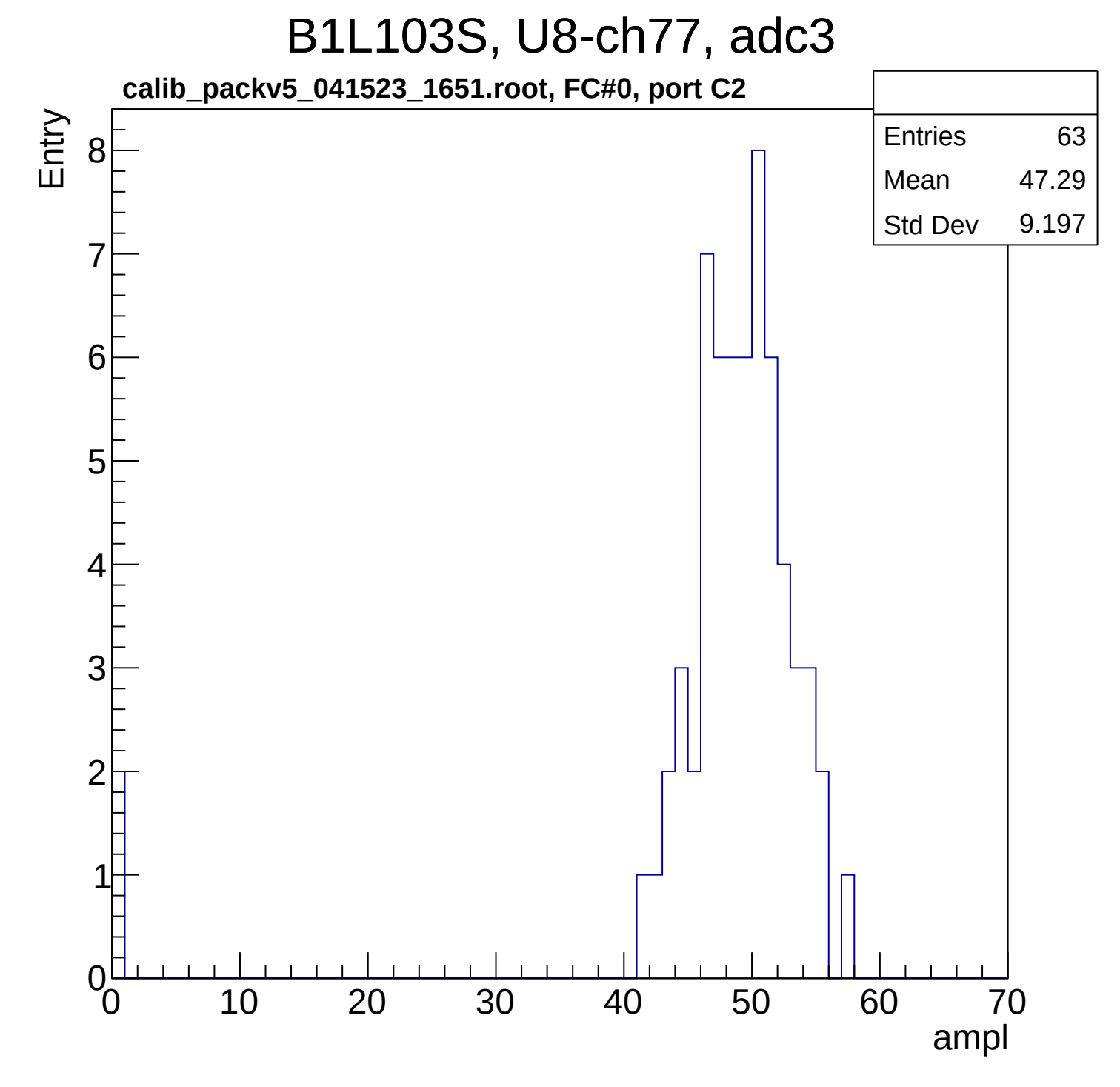
B1L103S, U8-ch77, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 47.29
Std Dev 9.197
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
50
60
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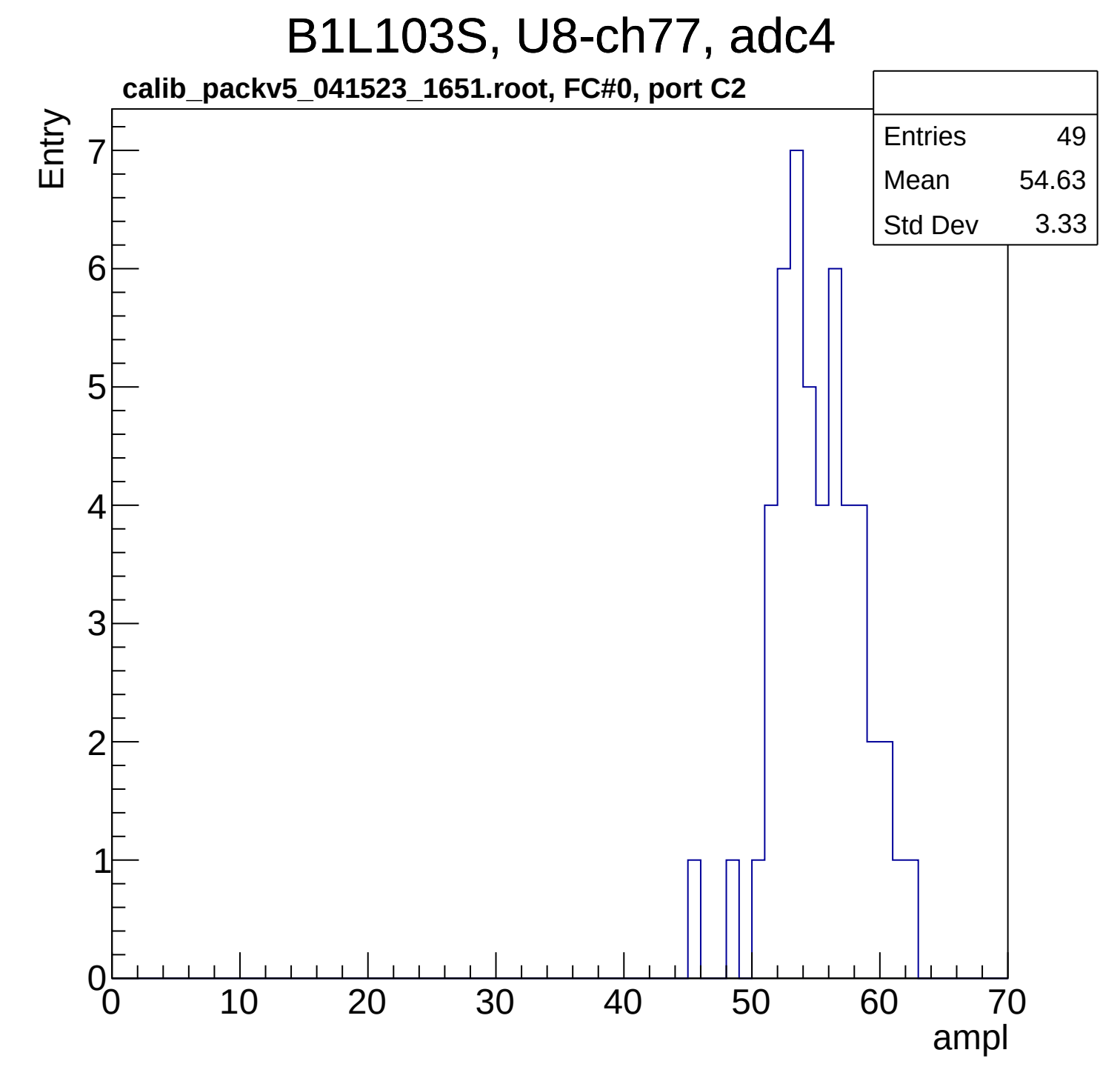
B1L103S, U8-ch77, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 54.63
Std Dev 3.33
Entry
ampl
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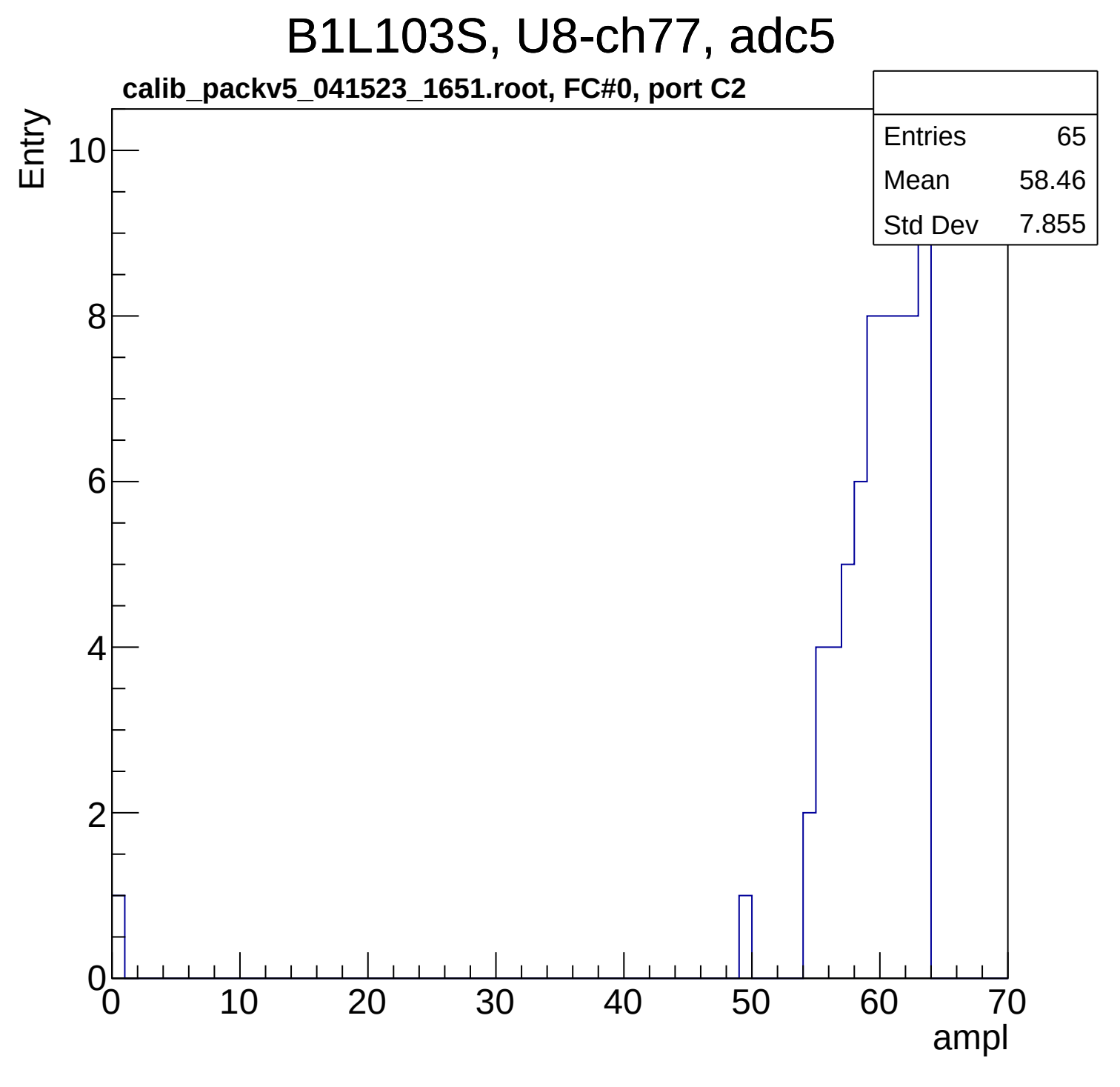
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U8-ch77, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 58.46
Std Dev 7.855
Entry
ampl
0
2
4
6
8
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0
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40
50
60
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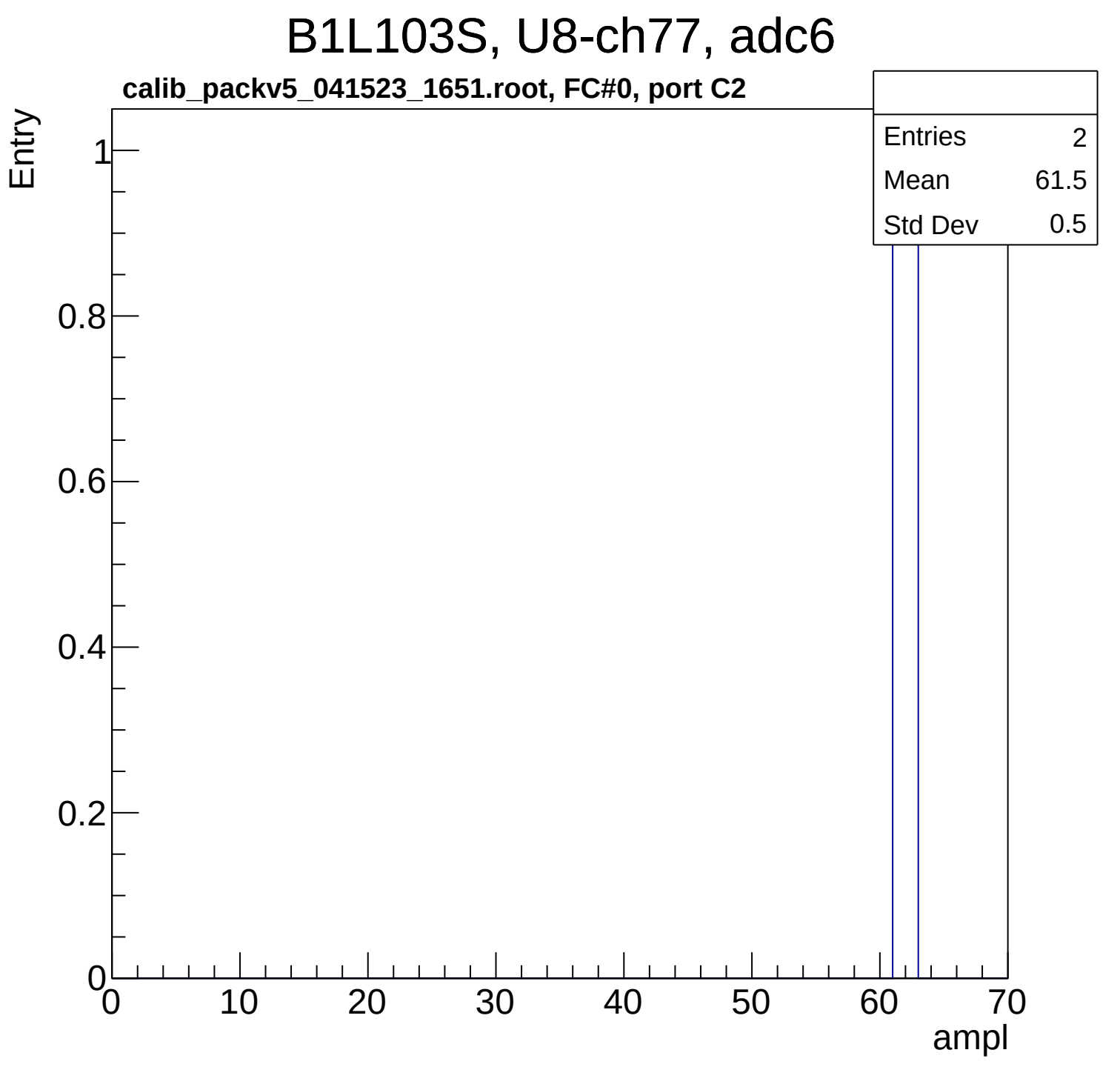
B1L103S, U8-ch77, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 61.5
Std Dev 0.5
Entry
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0.8
0.6
0.4
0.2
0
0
10
20
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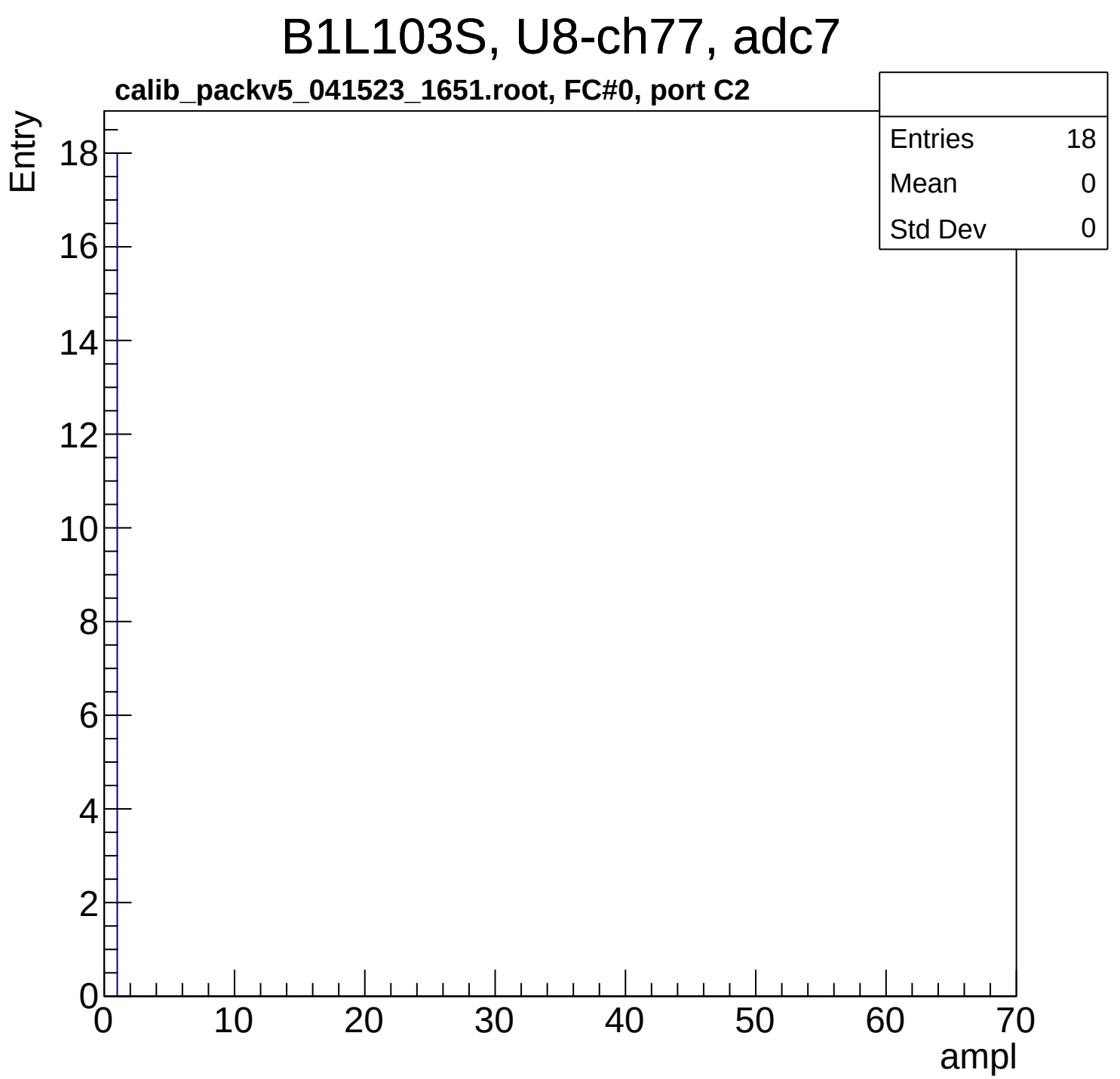
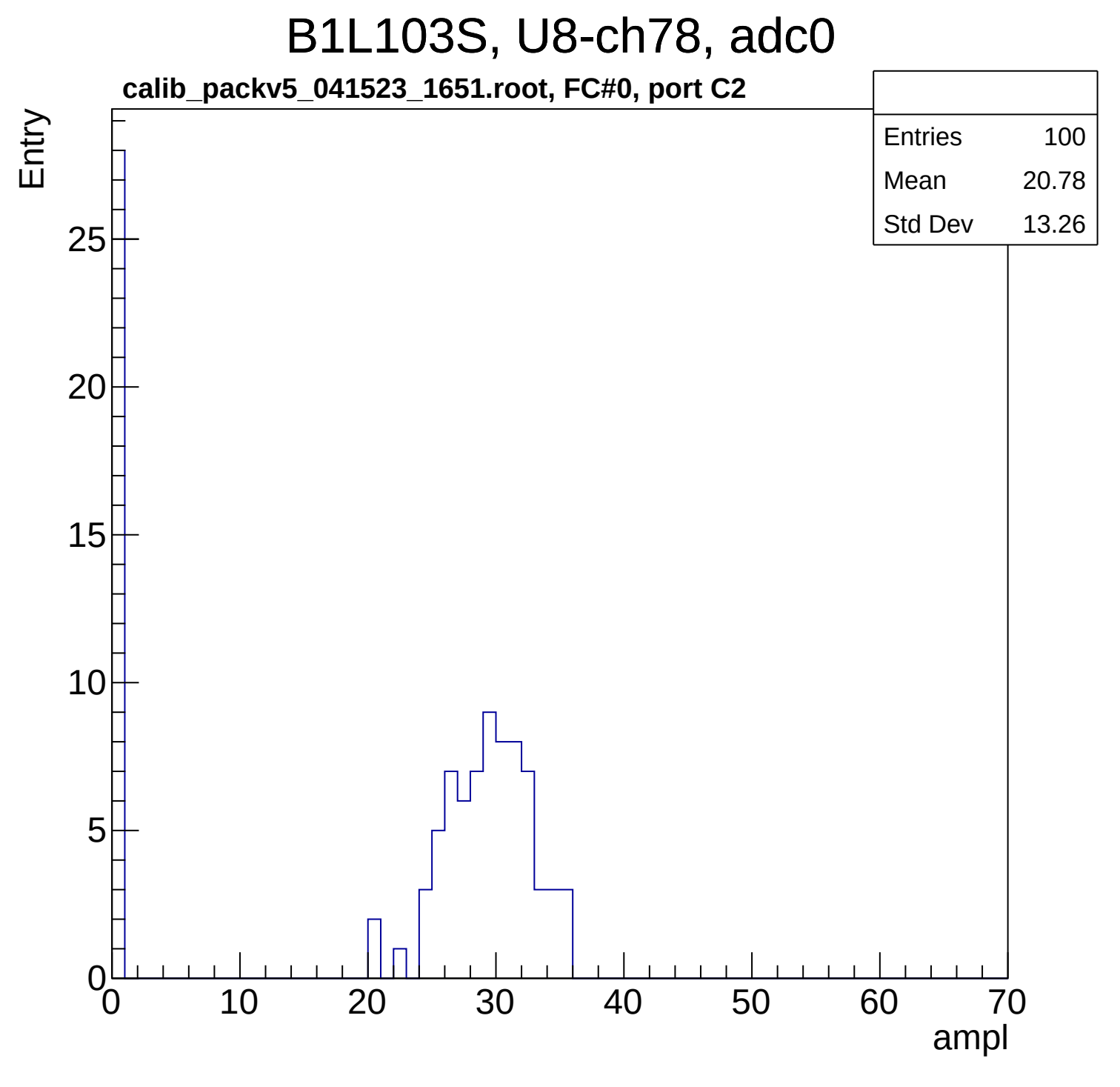
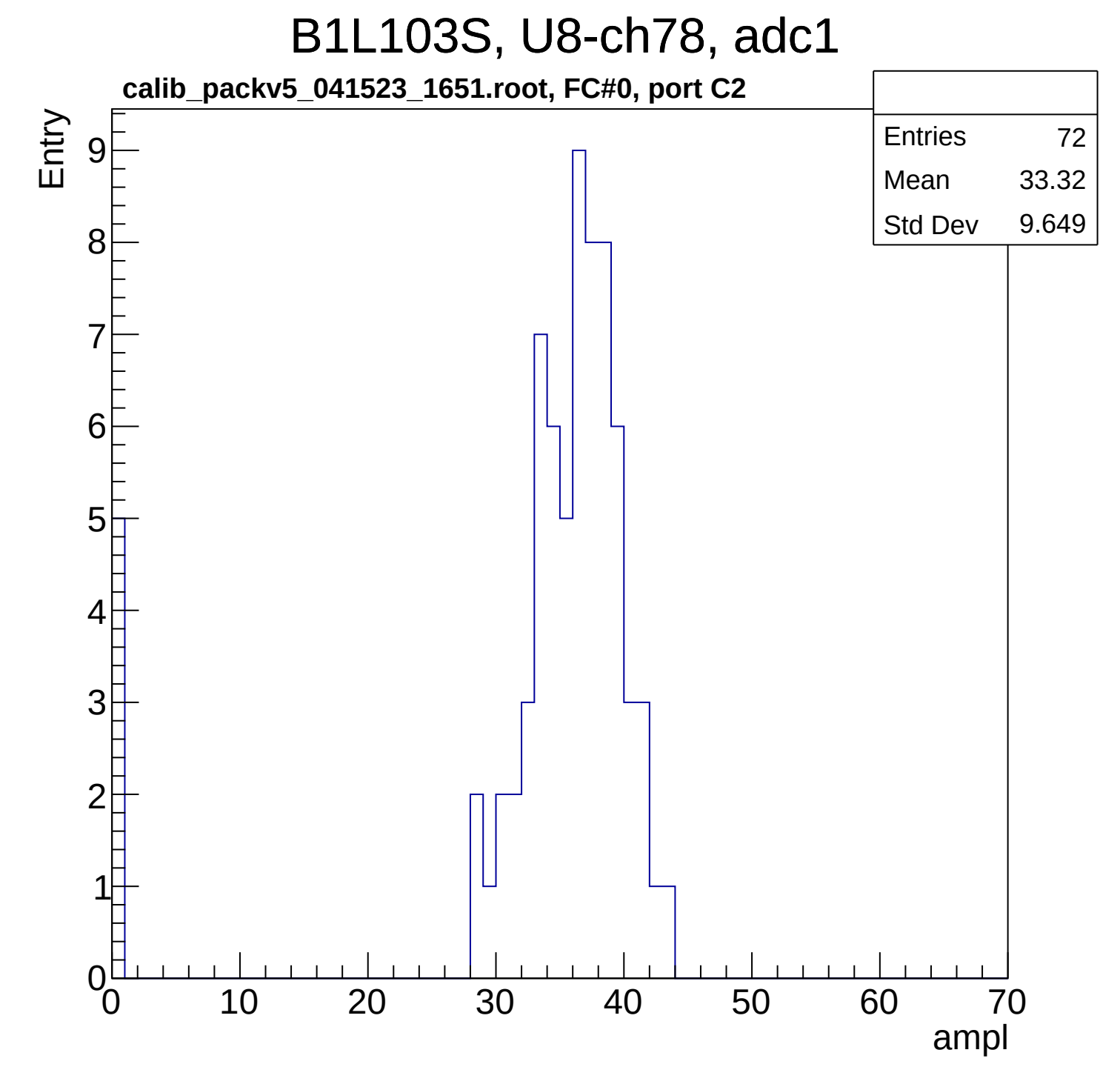
40
50
60
70
ampl


B1L103S, U8-ch77, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch78, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 100
Mean 20.78
Std Dev 13.26
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch78, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 33.32
Std Dev 9.649
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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60
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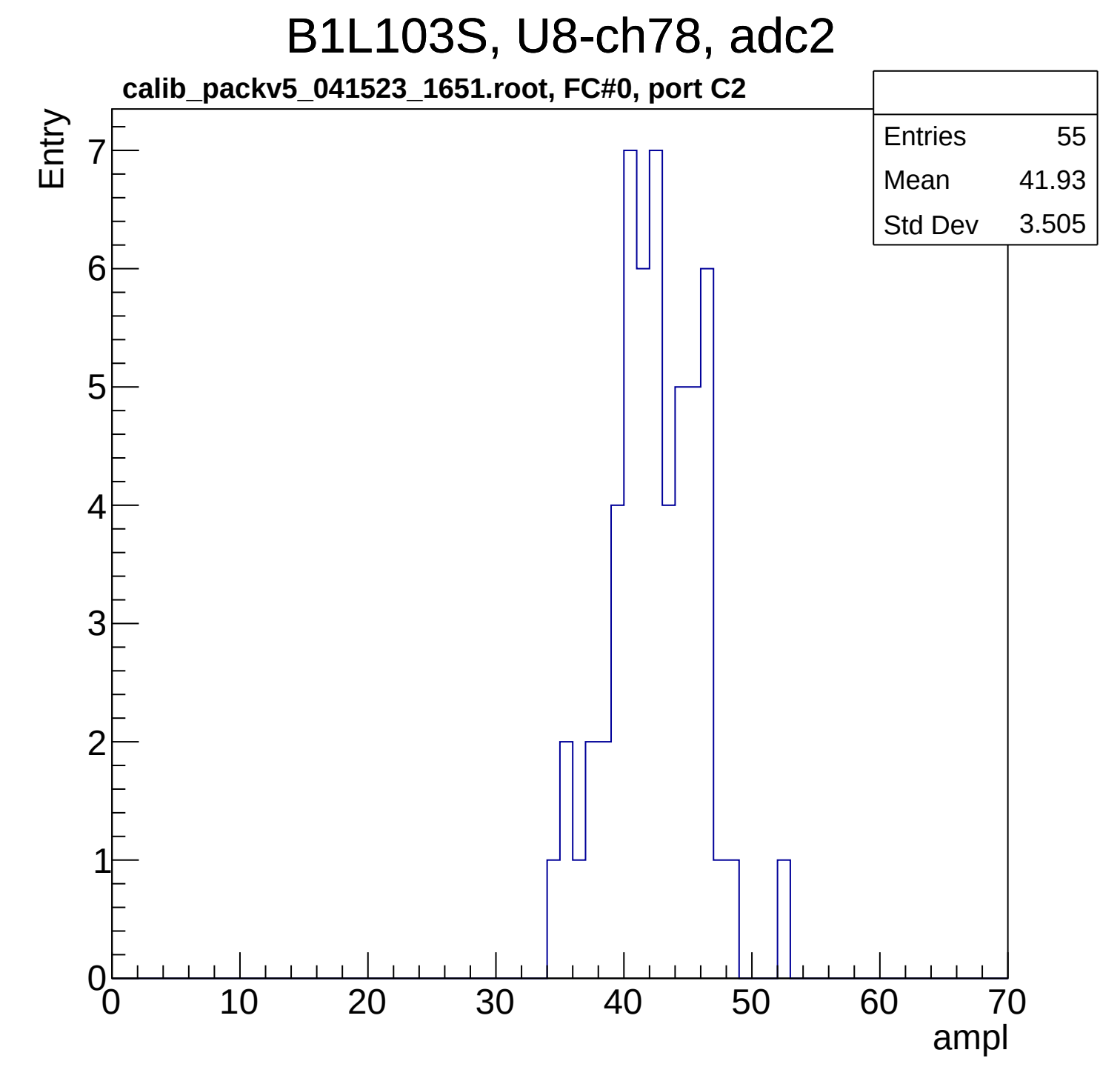
B1L103S, U8-ch78, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 41.93
Std Dev 3.505
Entry
ampl
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2
3
4
5
6
7
0
10
20
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40
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60
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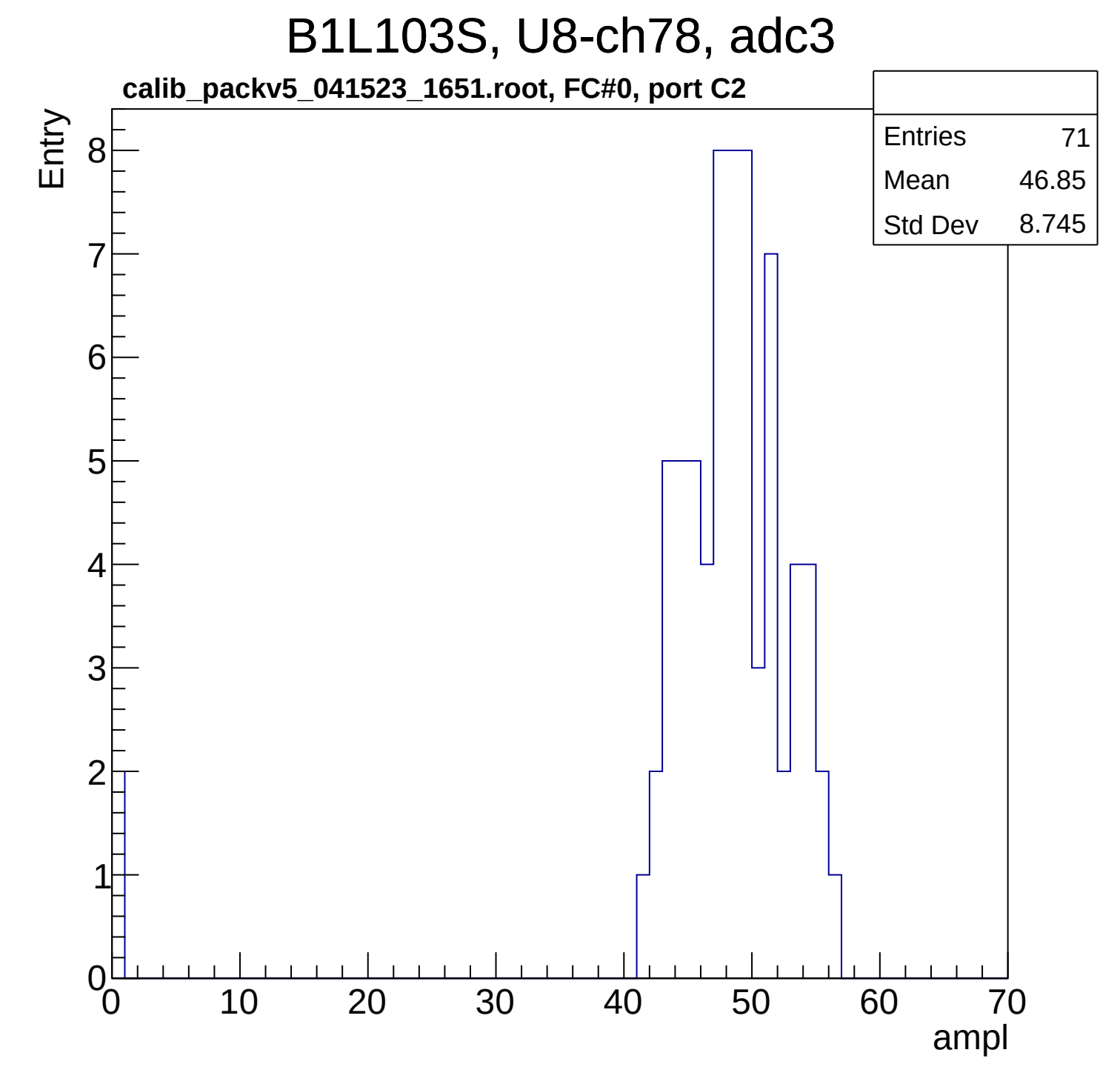
B1L103S, U8-ch78, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 46.85
Std Dev 8.745
Entry
ampl
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1
2
3
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5
6
7
8
0
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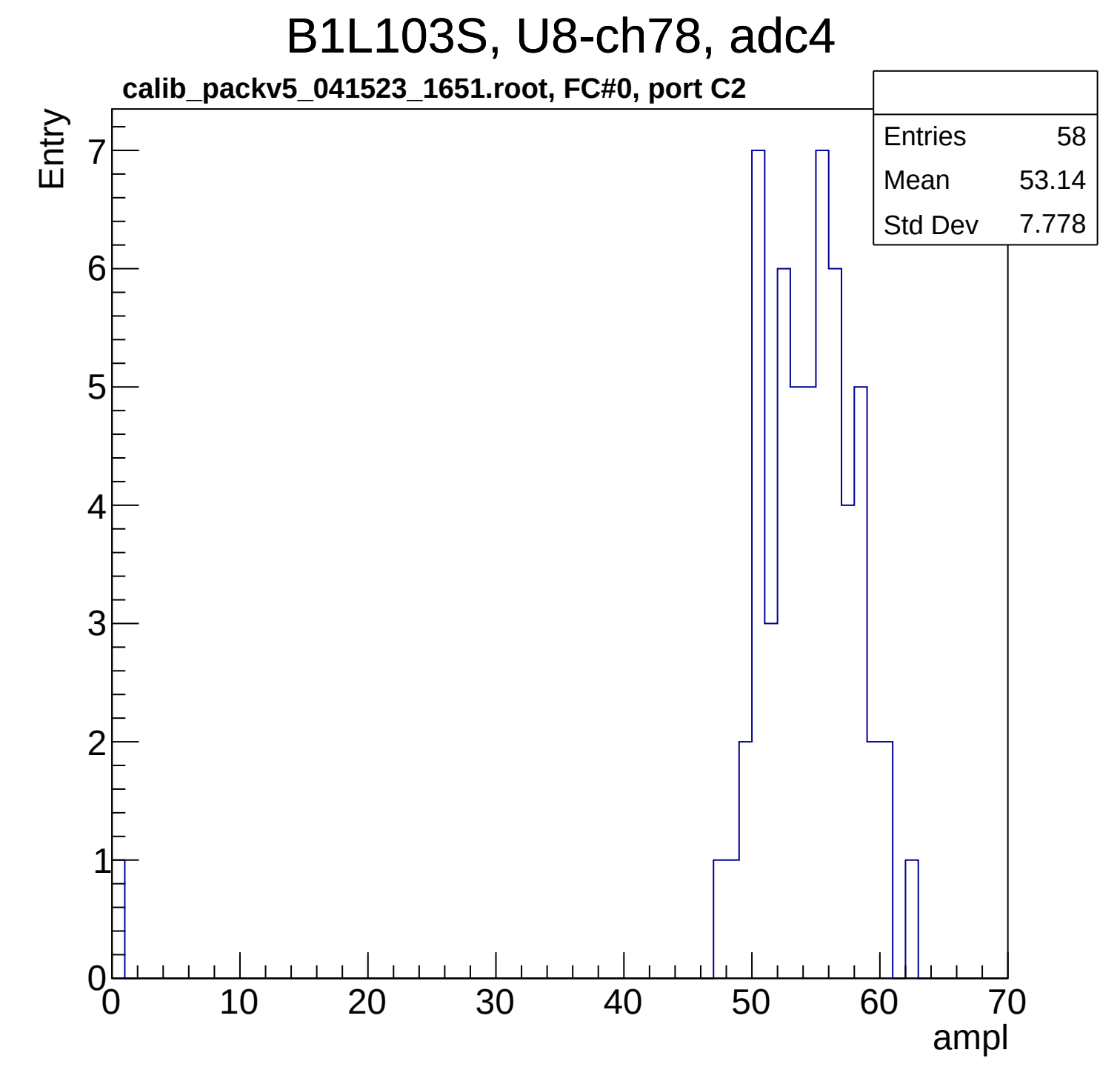
B1L103S, U8-ch78, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 53.14
Std Dev 7.778
Entry
ampl
0
1
2
3
4
5
6
7
0
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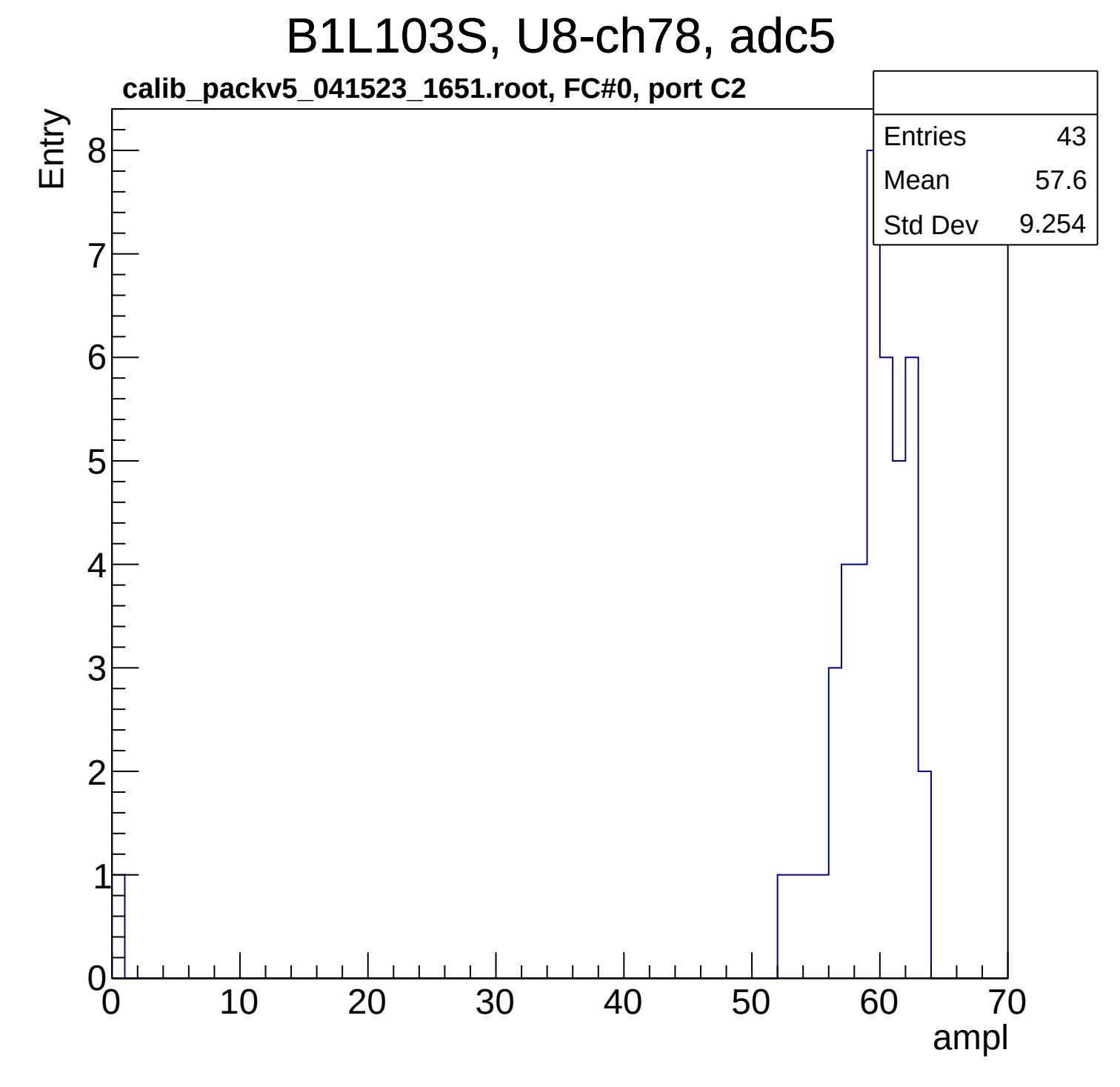
B1L103S, U8-ch78, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 57.6
Std Dev 9.254
Entry
ampl
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2
3
4
5
6
7
8
0
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60
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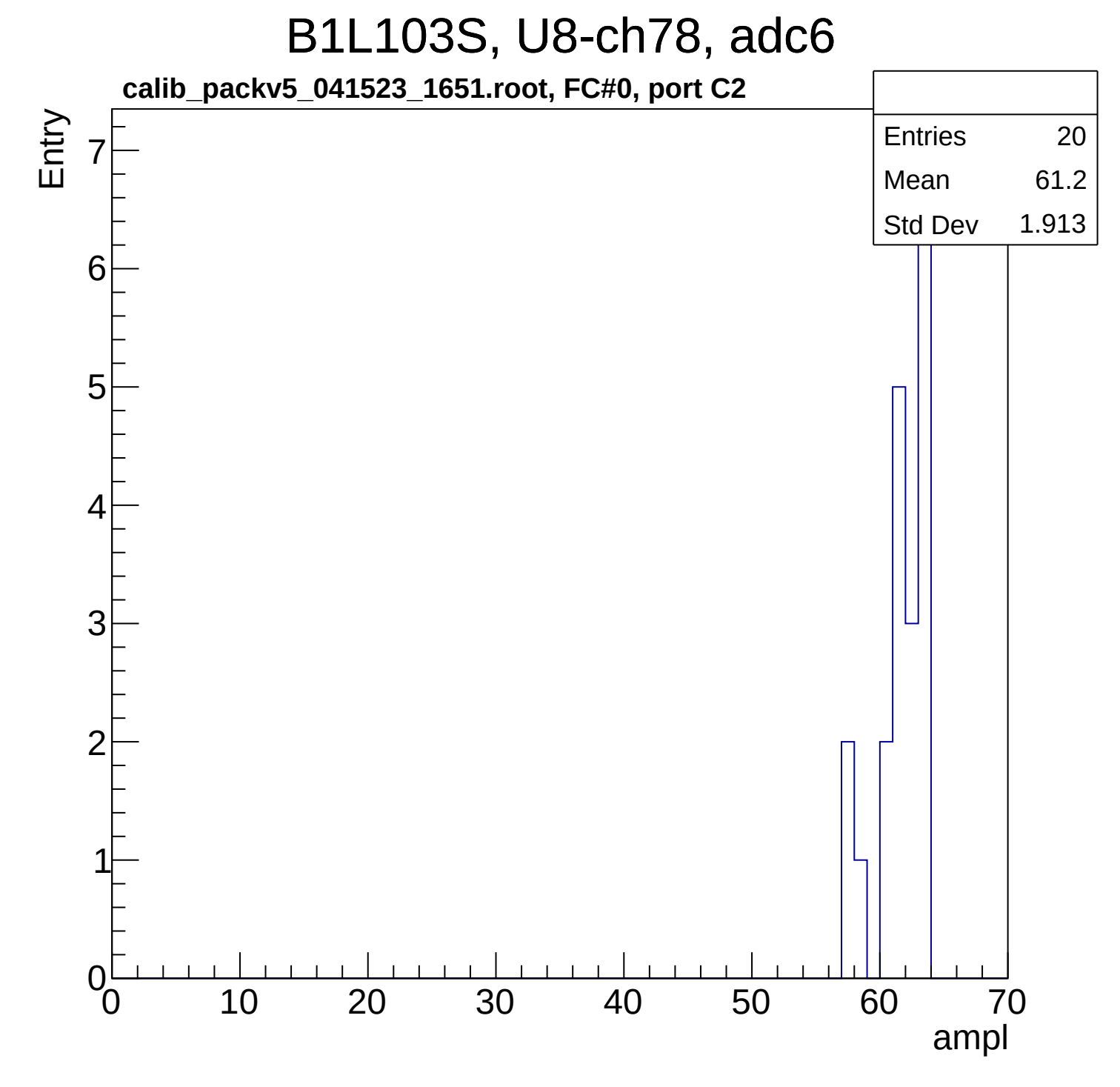
B1L103S, U8-ch78, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 61.2
Std Dev 1.913
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
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60
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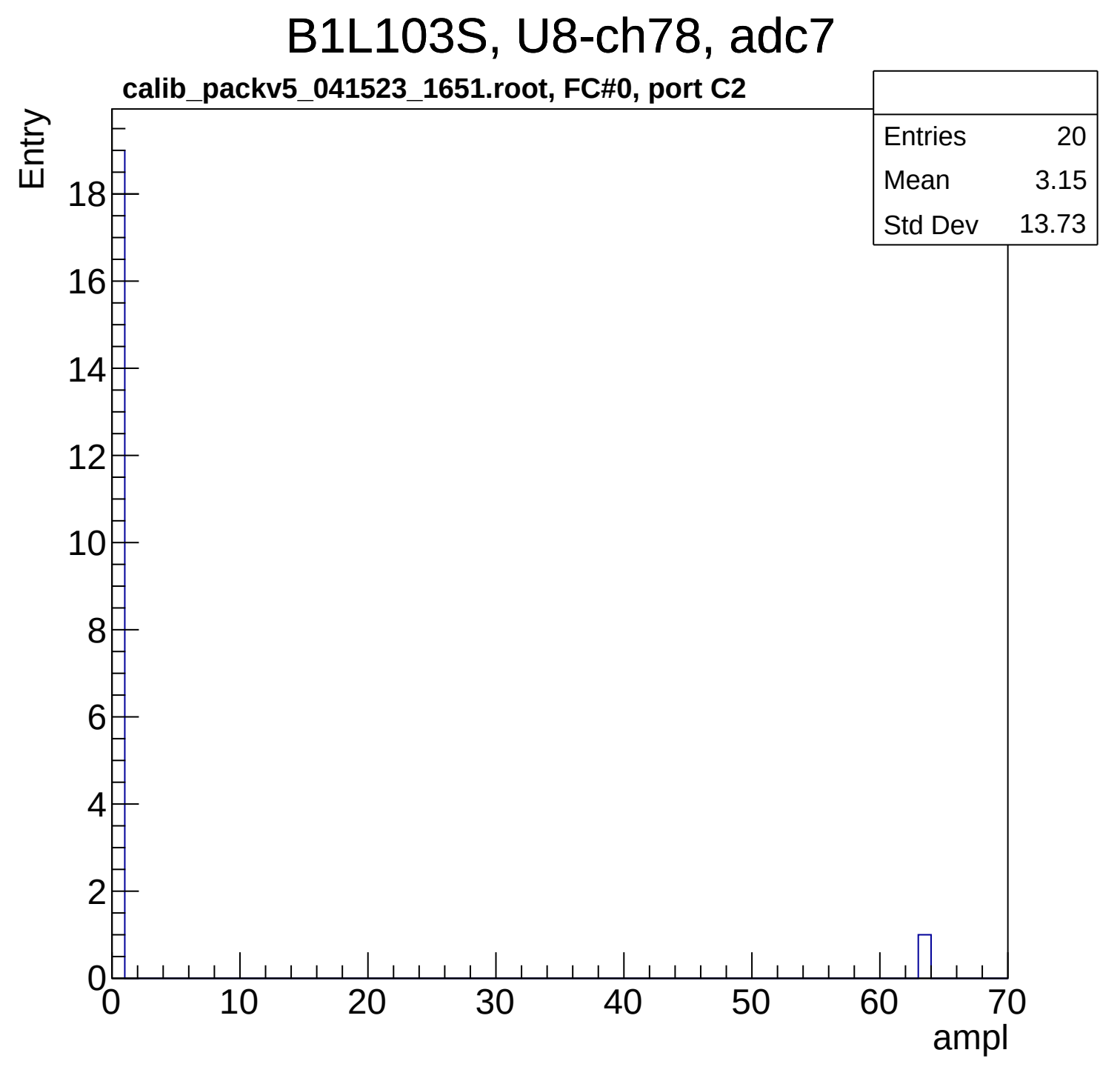
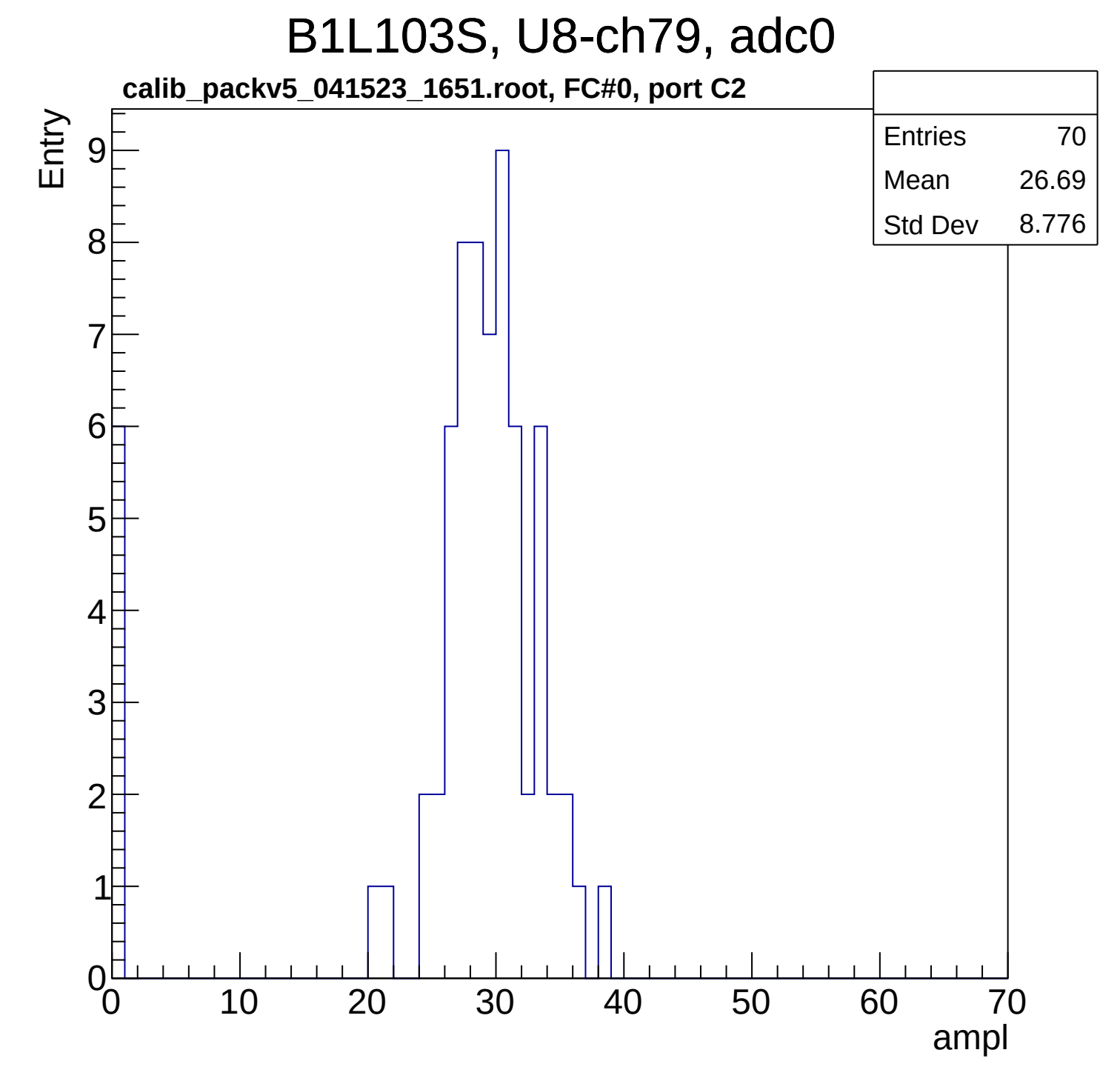

B1L103S, U8-ch78, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch79, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 26.69
Std Dev 8.776
Entry
ampl
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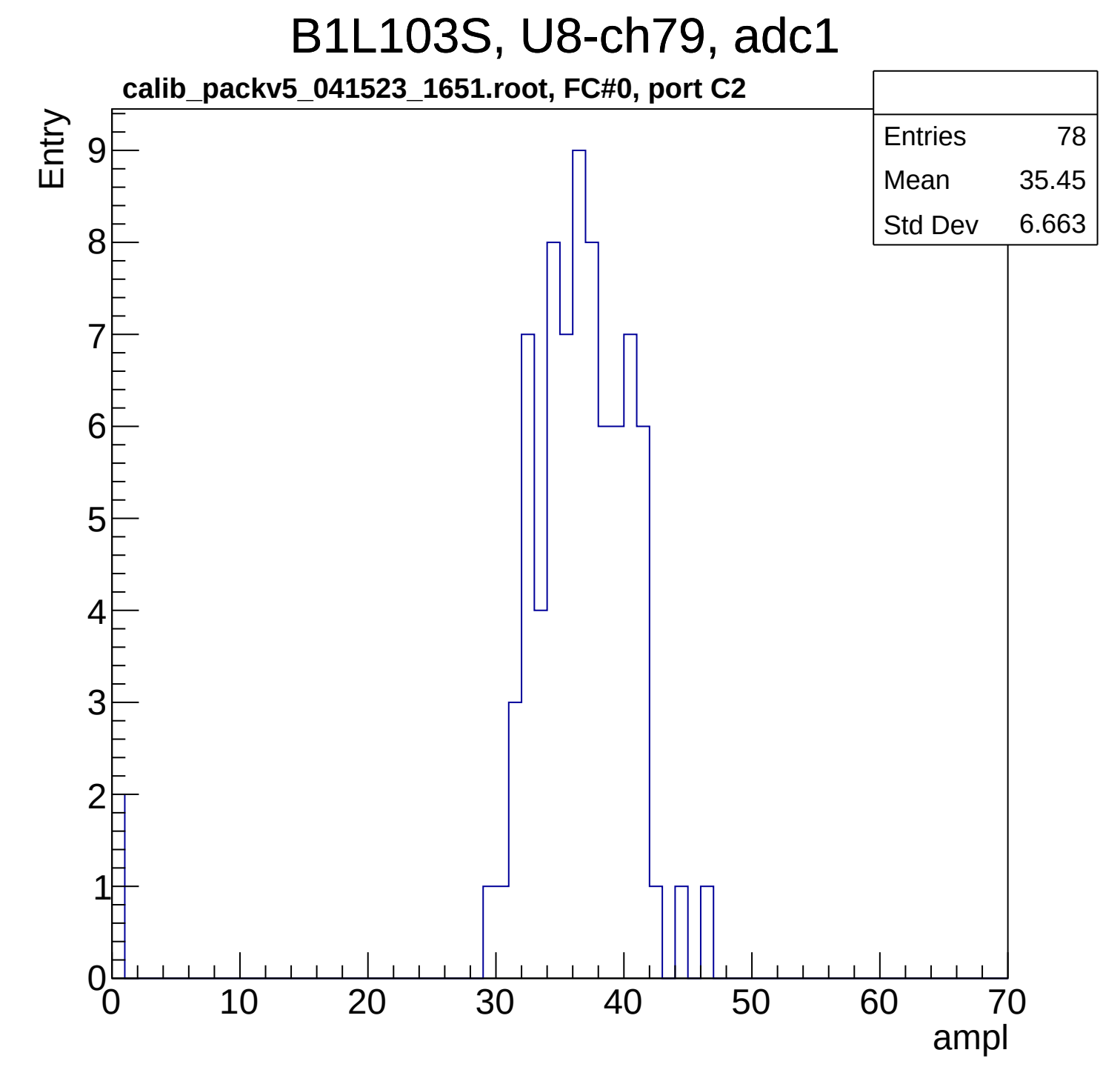
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U8-ch79, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 35.45
Std Dev 6.663
Entry
ampl
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2
3
4
5
6
7
8
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0
10
20
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40
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60
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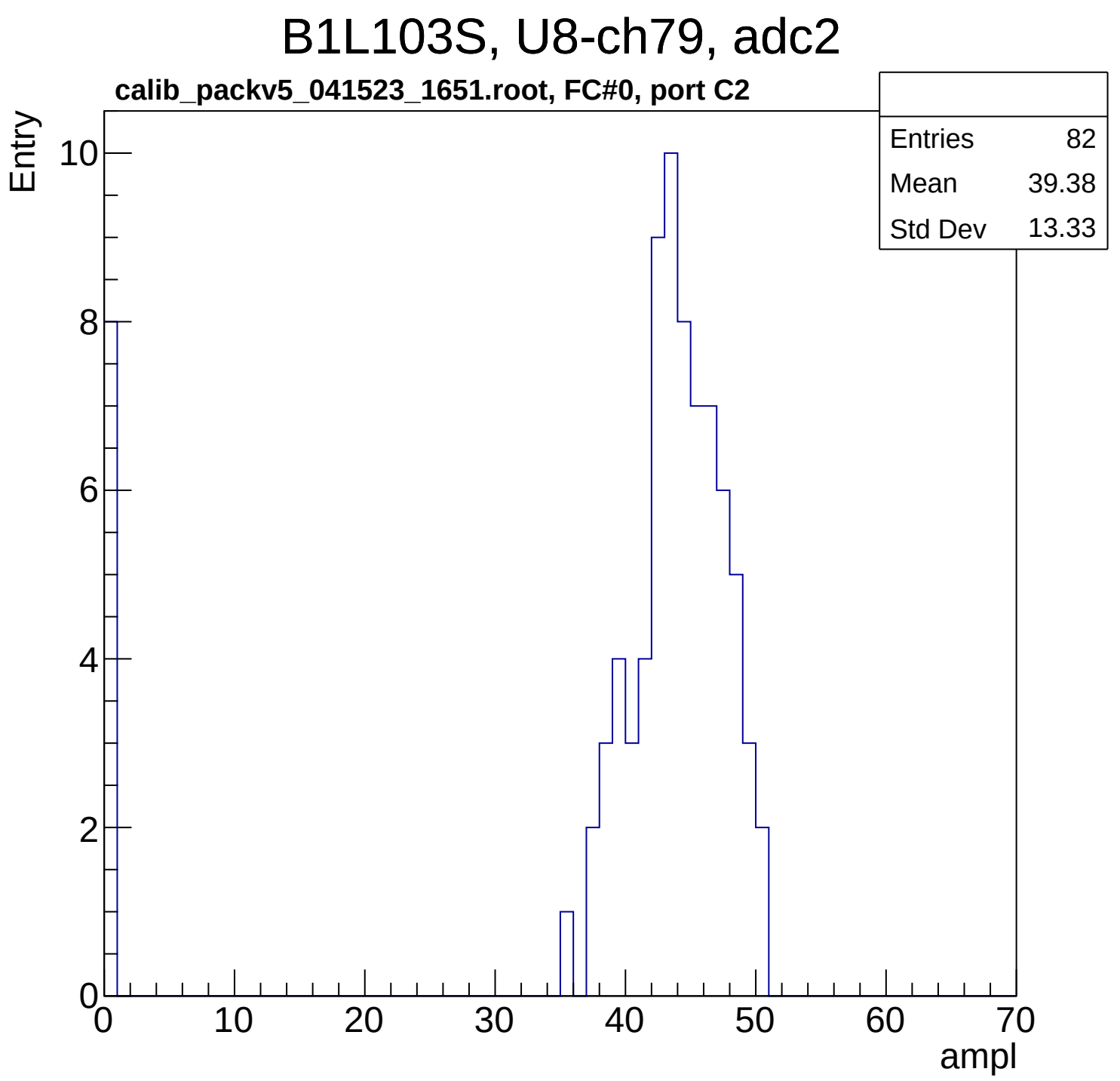
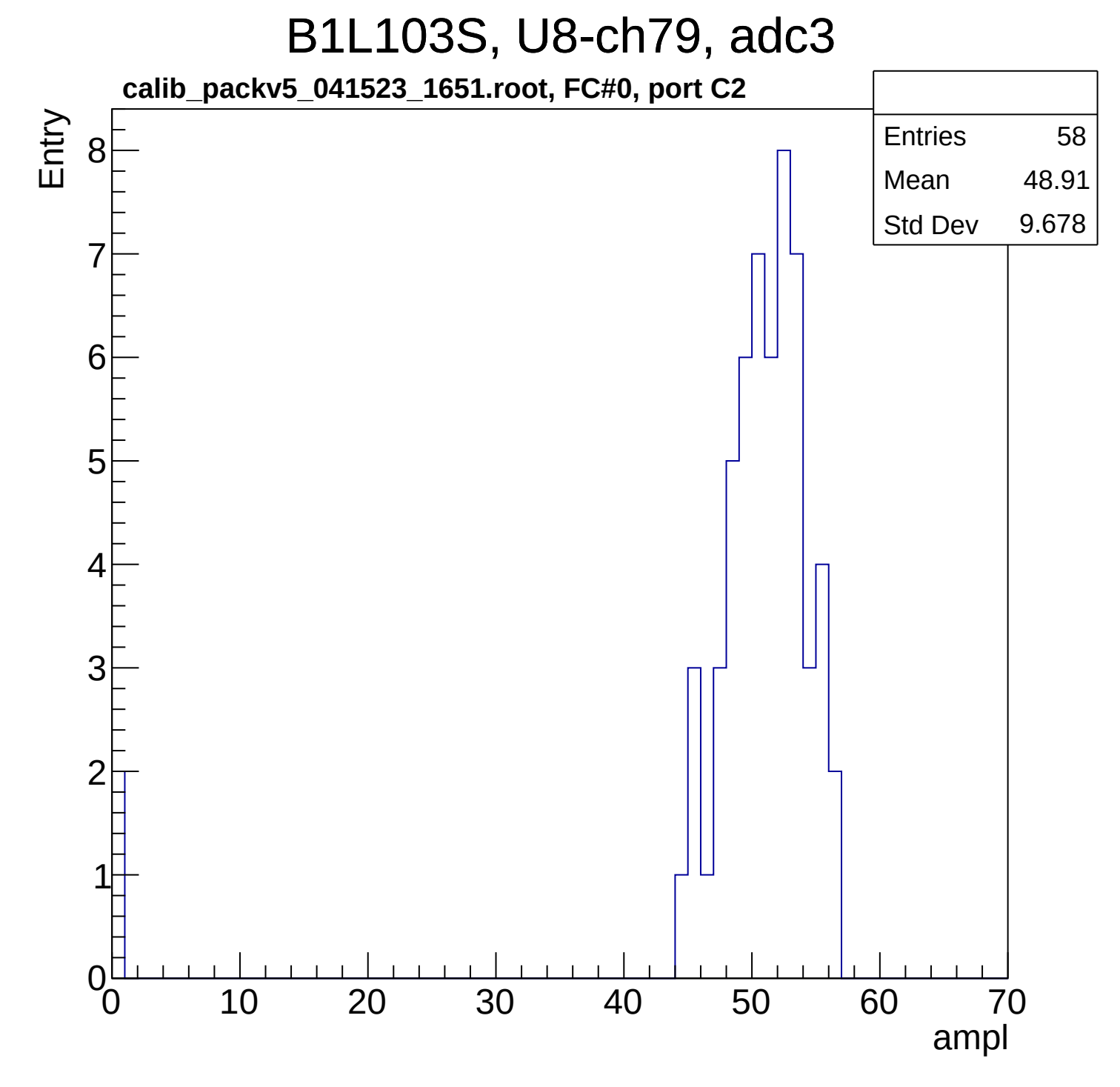

B1L103S, U8-ch79, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 39.38
Std Dev 13.33
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U8-ch79, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 48.91
Std Dev 9.678
Entry
ampl
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2
3
4
5
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7
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0
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60
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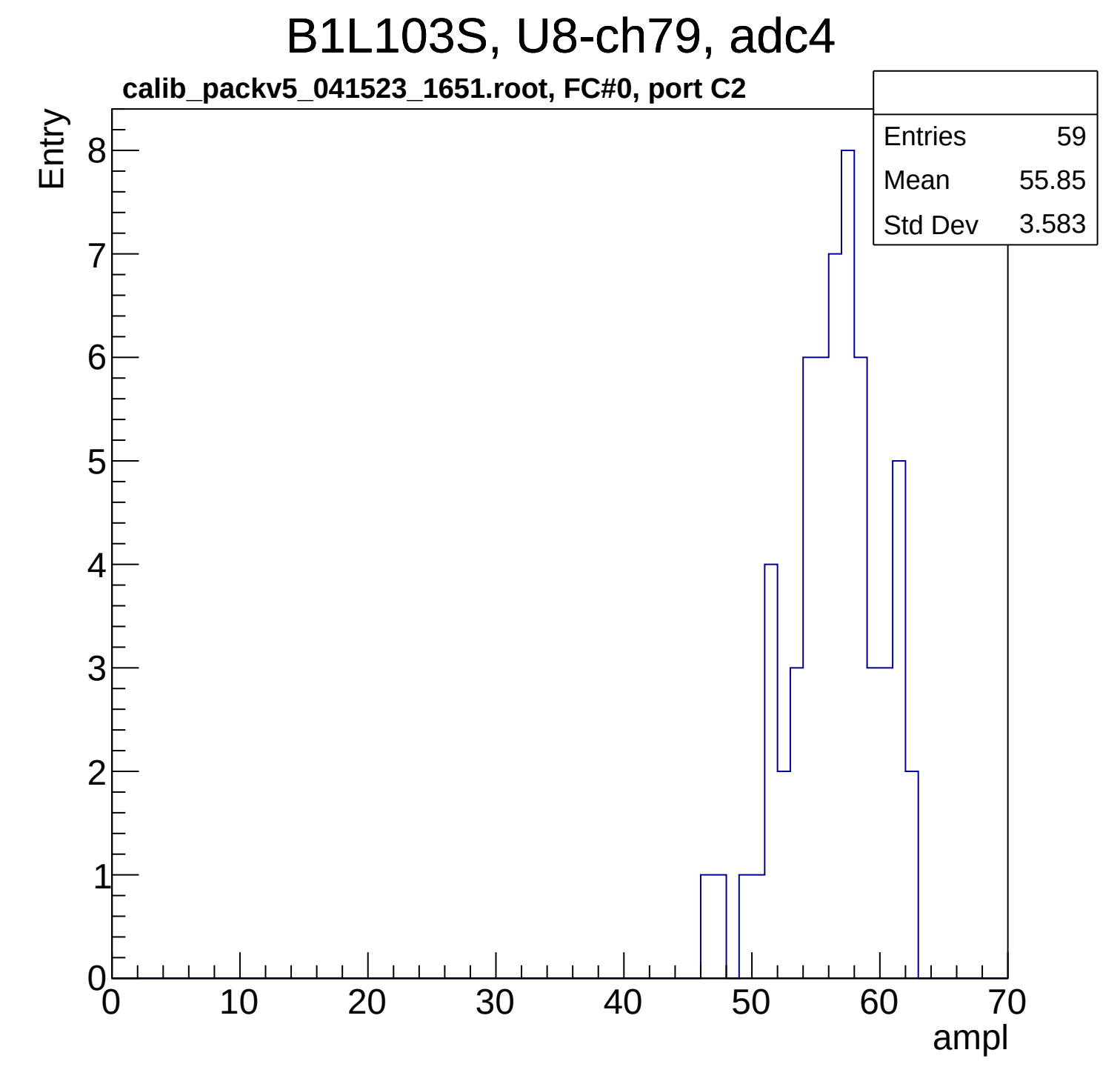
B1L103S, U8-ch79, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 55.85
Std Dev 3.583
Entry
ampl
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2
3
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5
6
7
8
0
10
20
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40
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60
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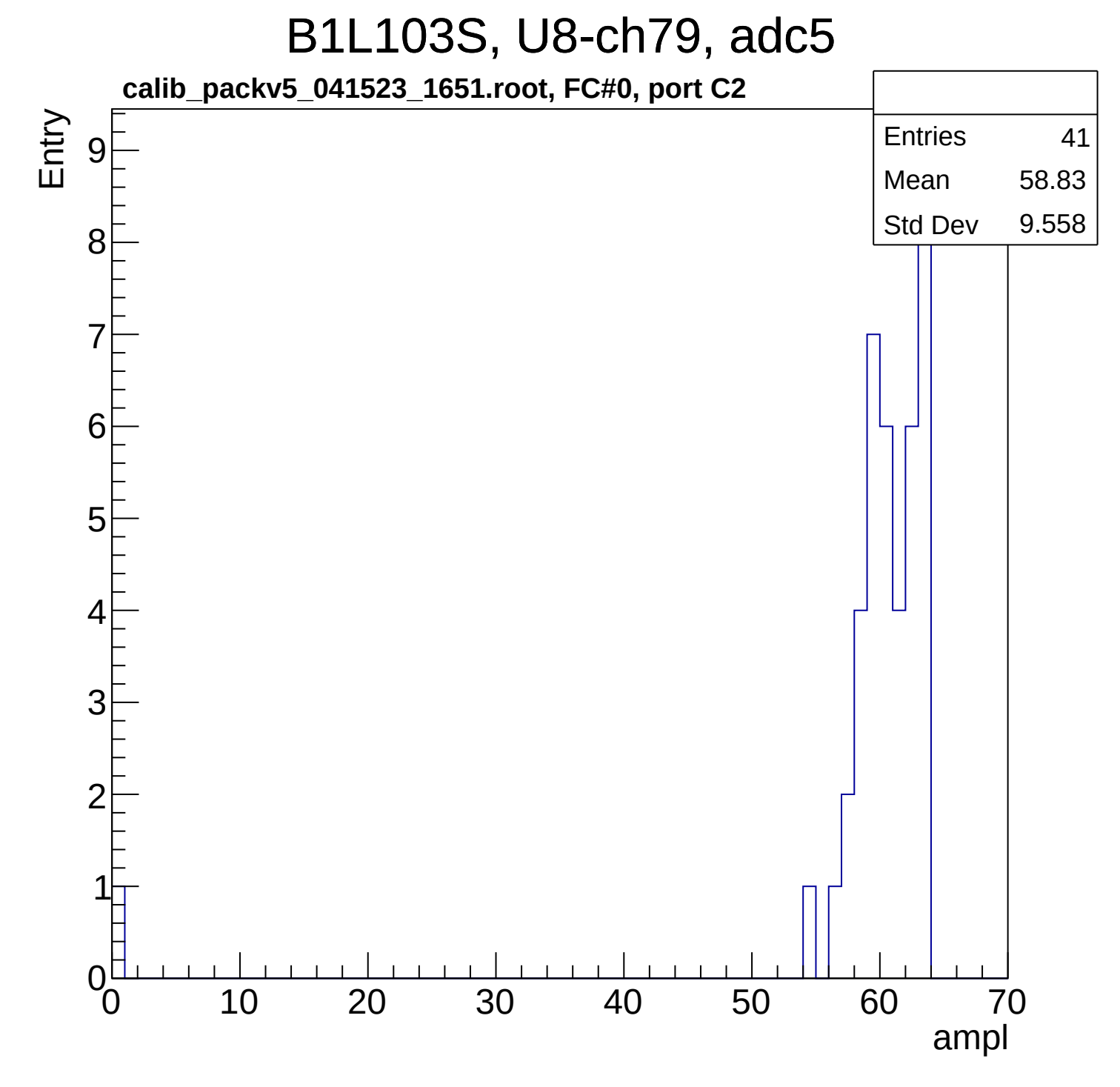
B1L103S, U8-ch79, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 58.83
Std Dev 9.558
Entry
ampl
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3
4
5
6
7
8
9
0
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40
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60
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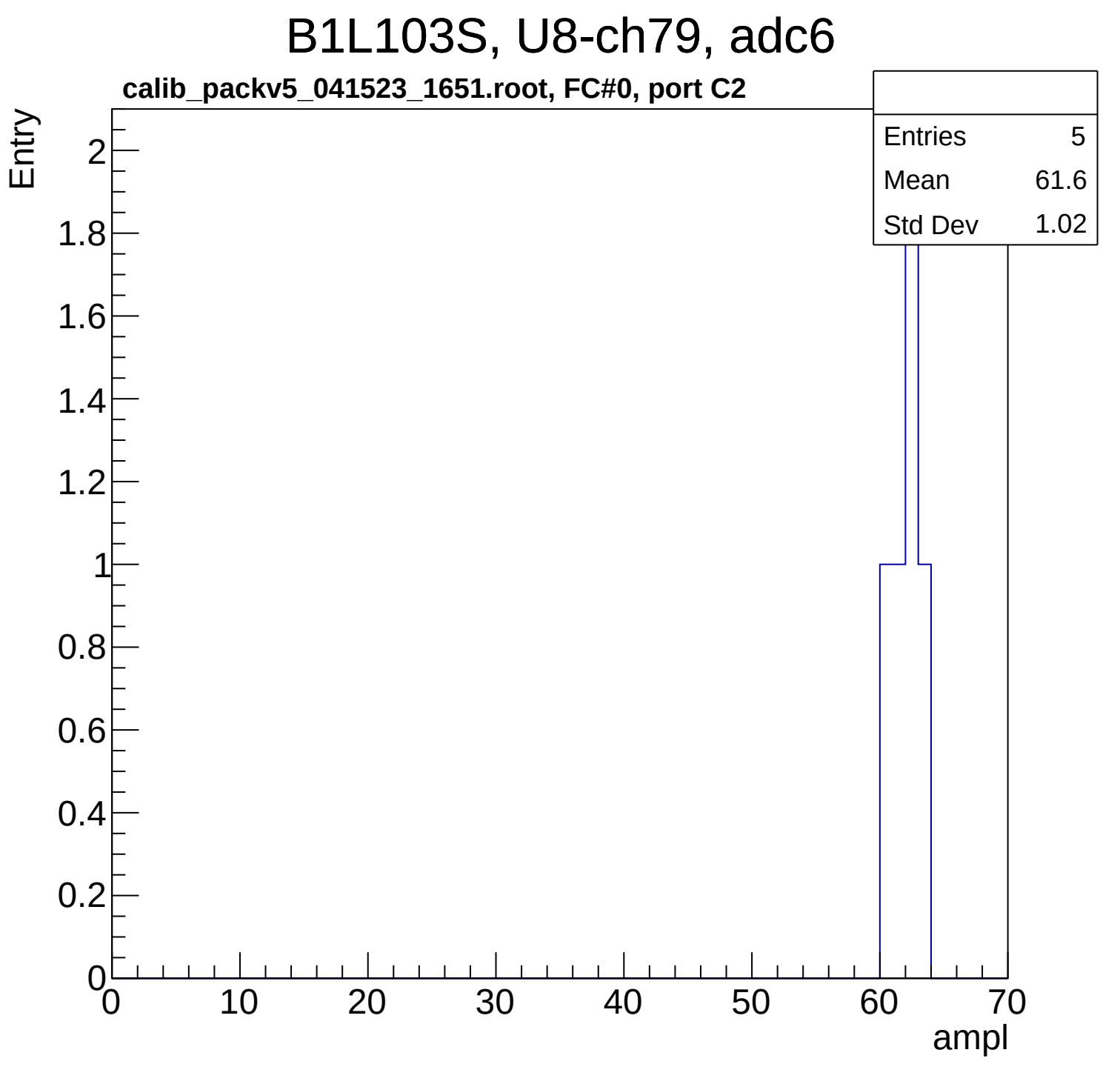
B1L103S, U8-ch79, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 61.6
Std Dev 1.02
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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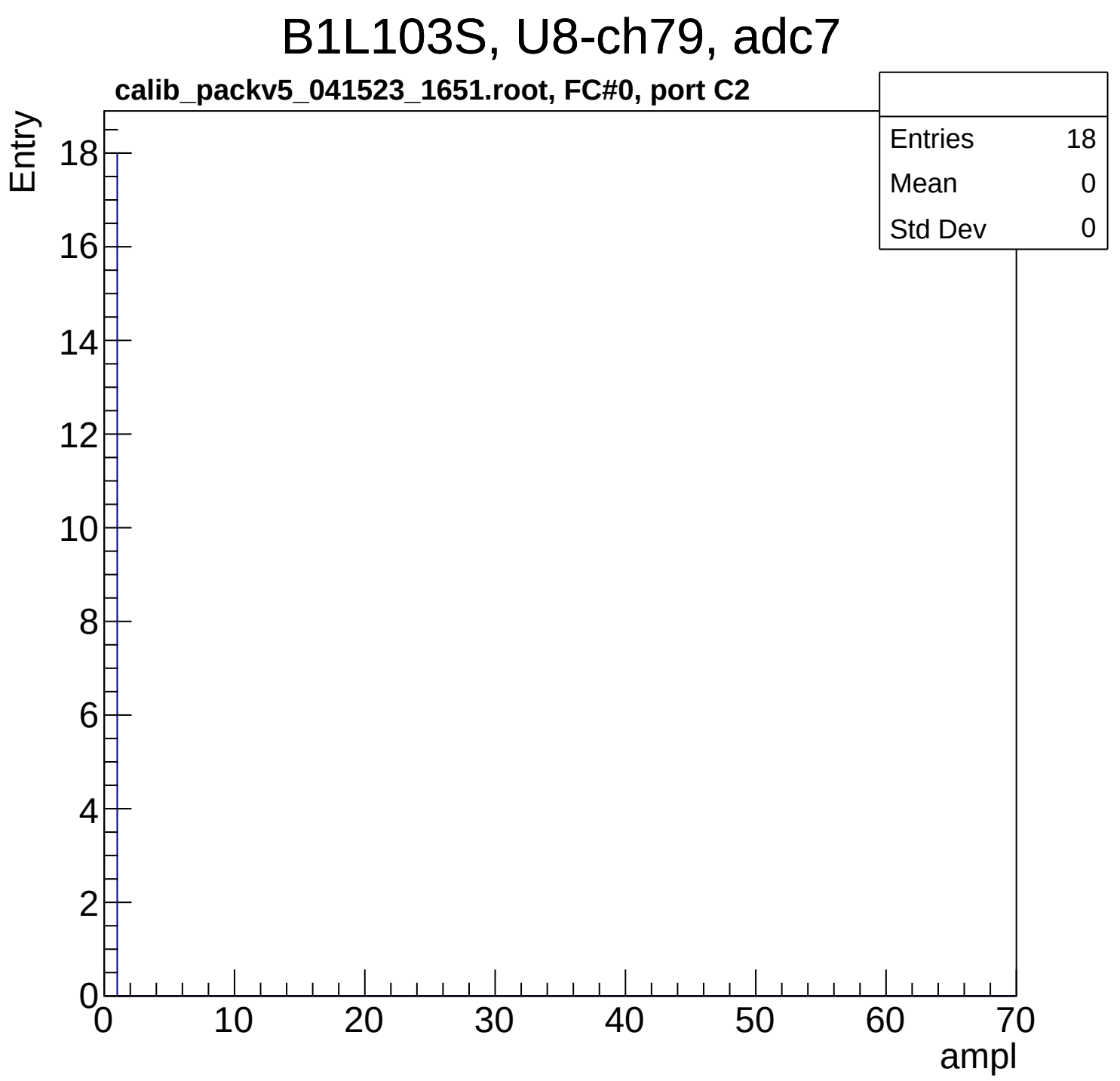
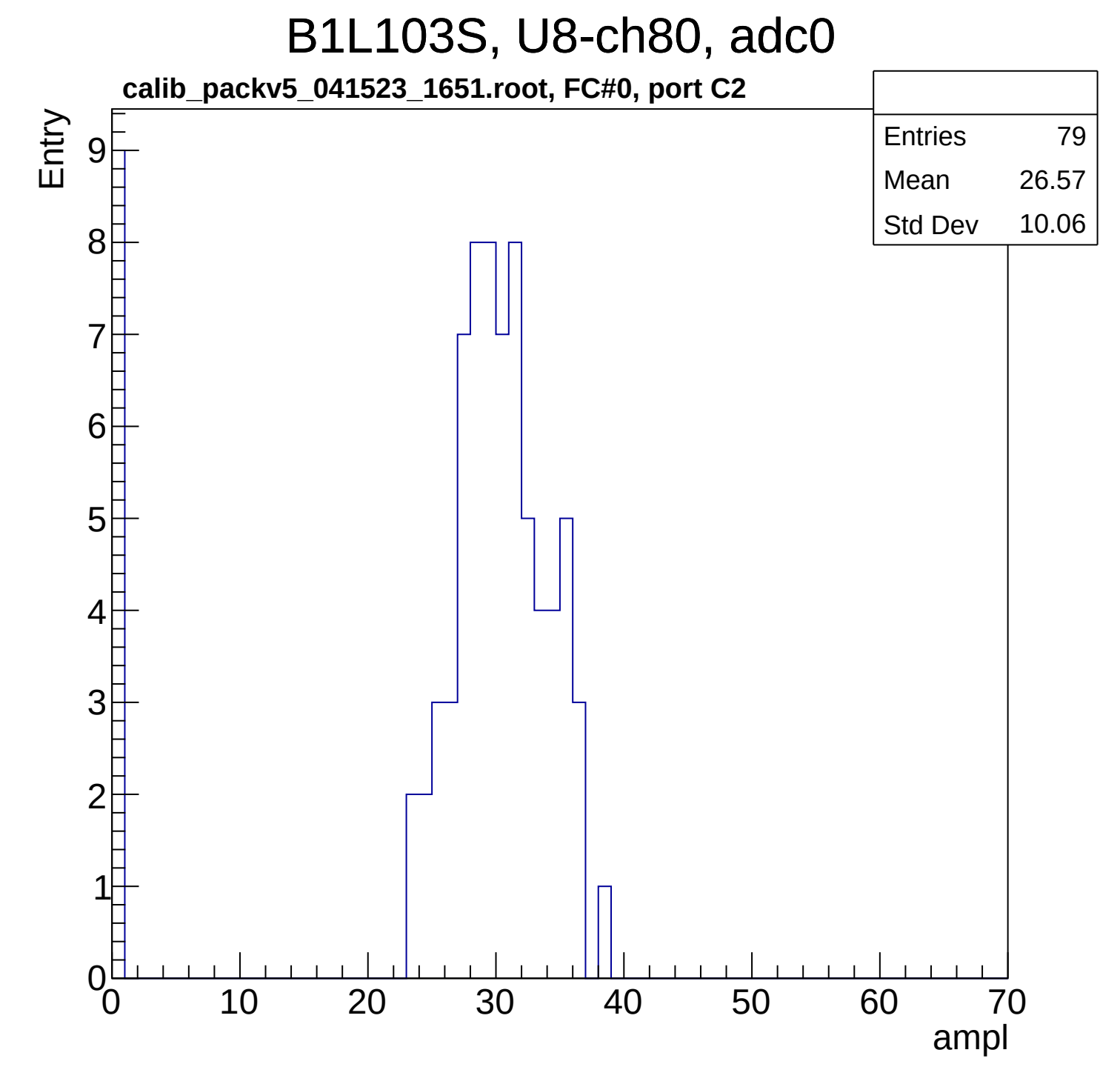

B1L103S, U8-ch79, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch80, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 26.57
Std Dev 10.06
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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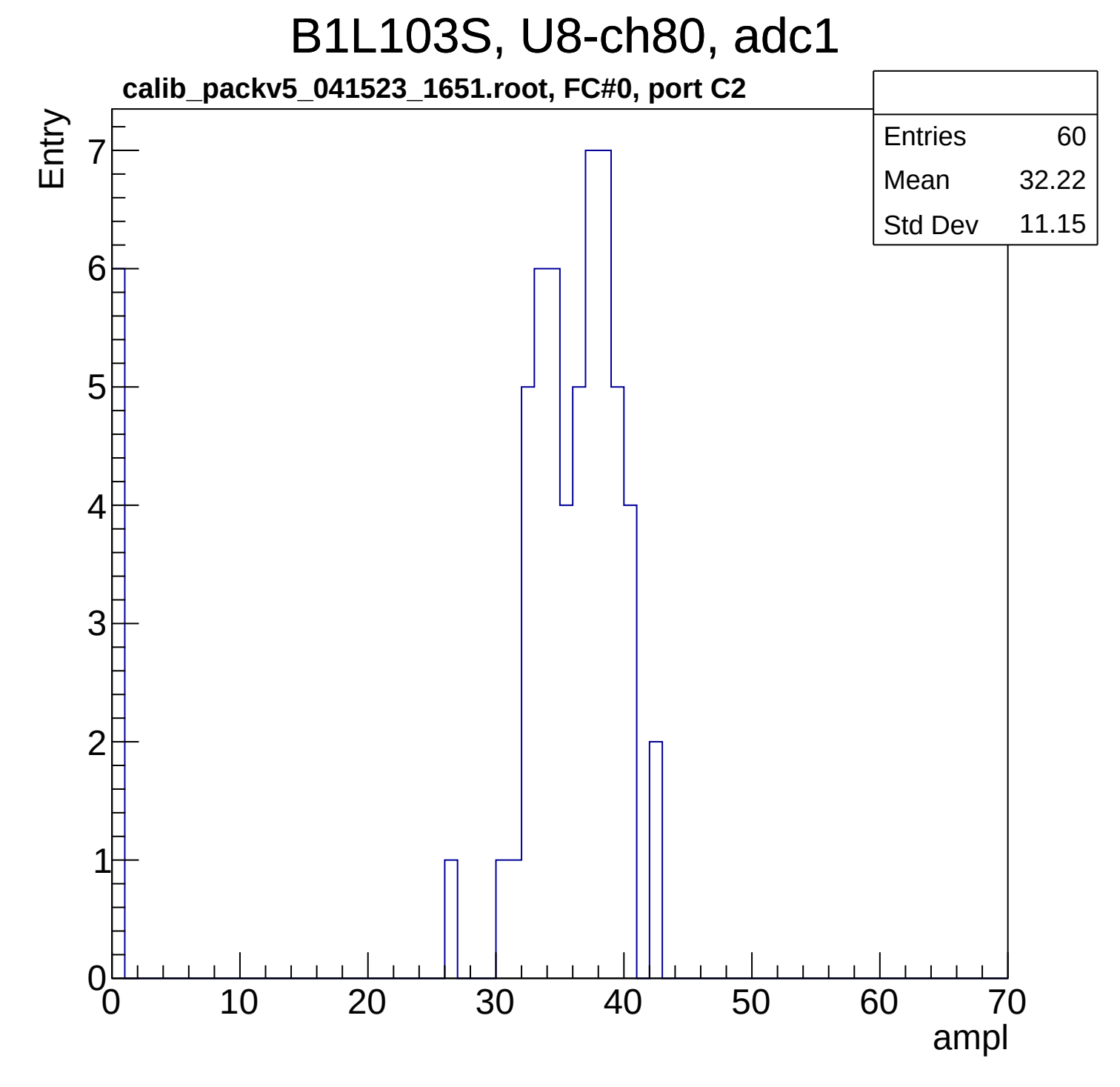
B1L103S, U8-ch80, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 32.22
Std Dev 11.15
Entry
ampl
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1
2
3
4
5
6
7
0
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20
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40
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60
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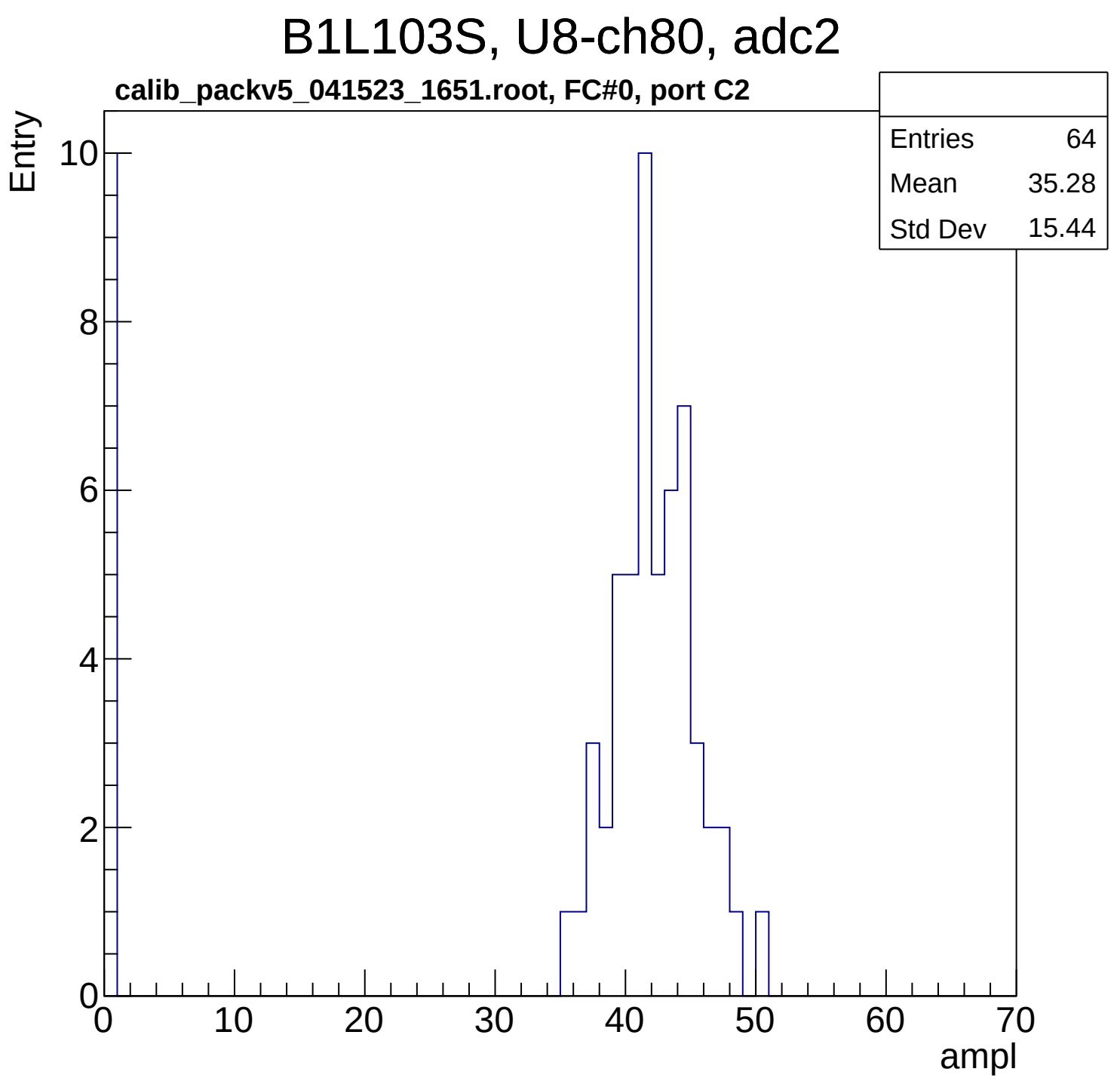
B1L103S, U8-ch80, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 35.28
Std Dev 15.44
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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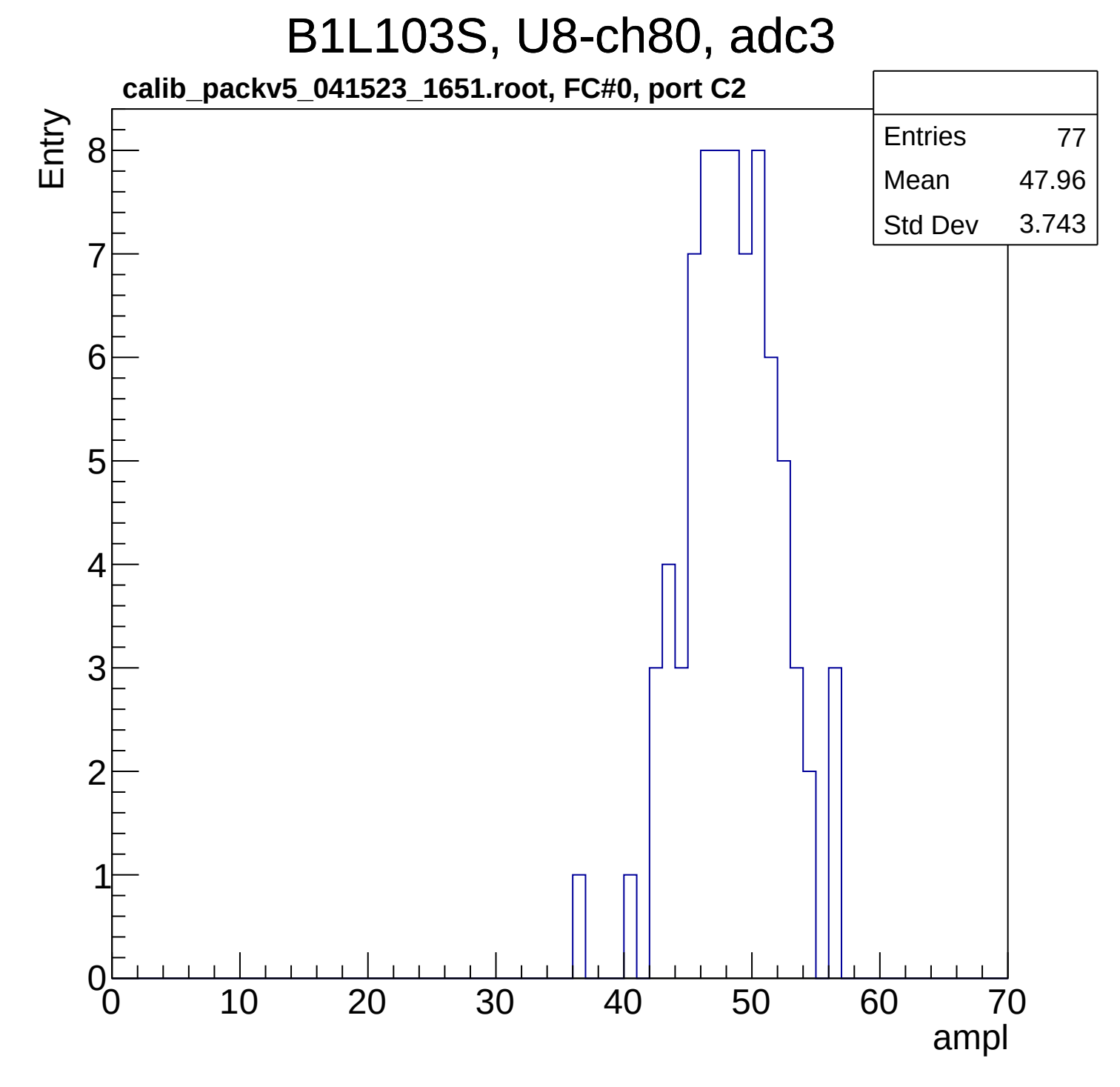
B1L103S, U8-ch80, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 47.96
Std Dev 3.743
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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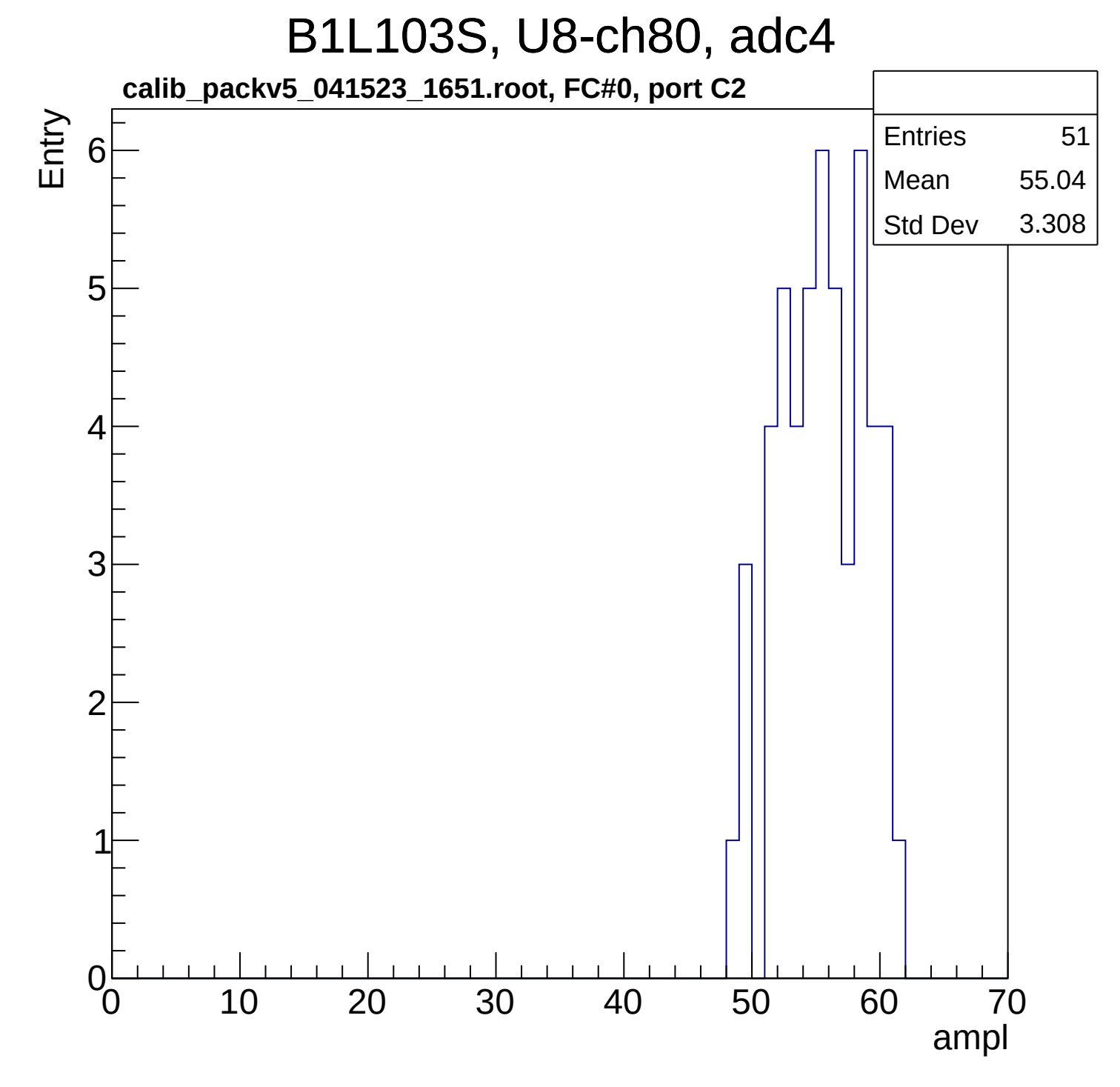
B1L103S, U8-ch80, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 55.04
Std Dev 3.308
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
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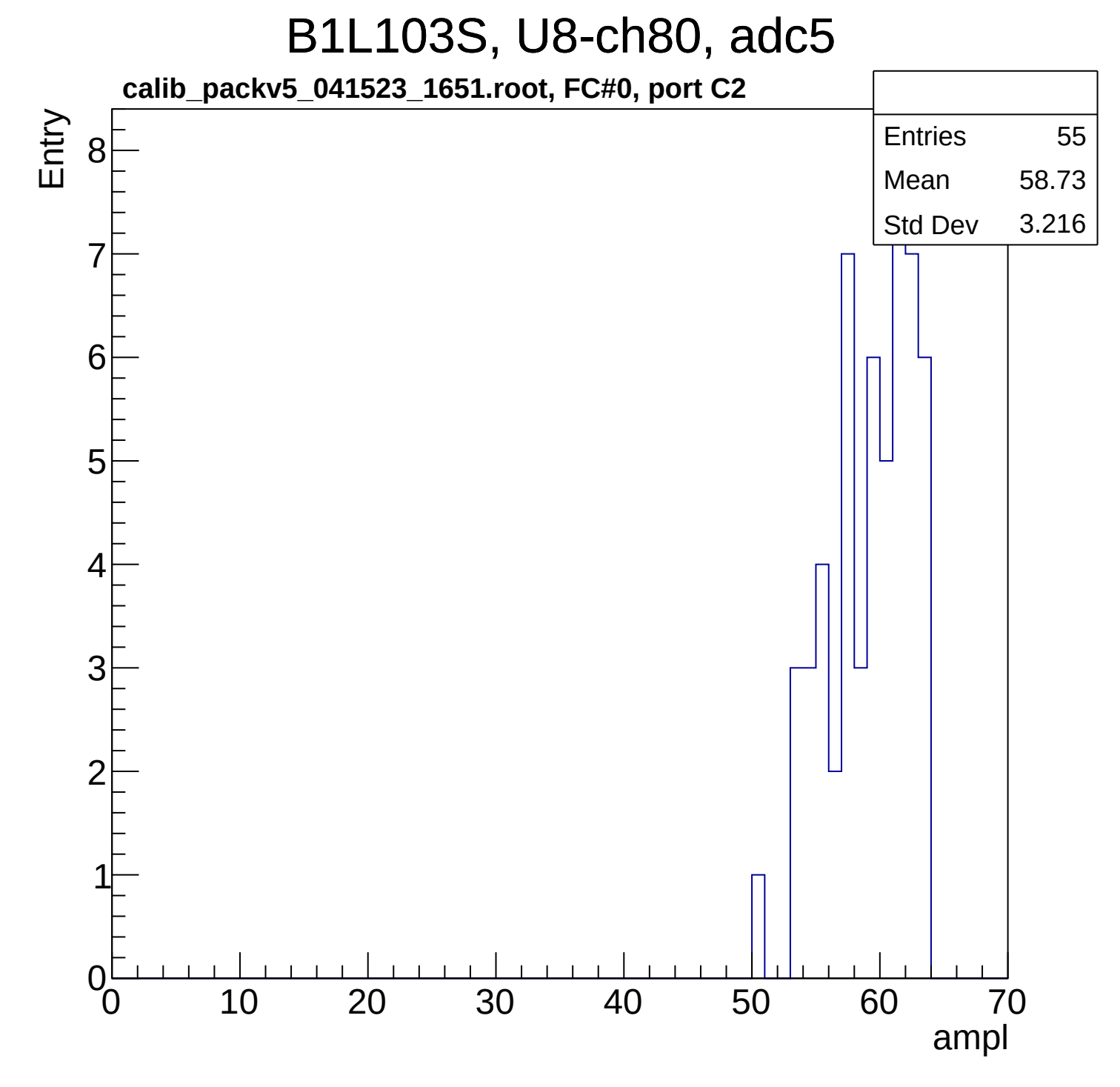
B1L103S, U8-ch80, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 58.73
Std Dev 3.216
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
50
60
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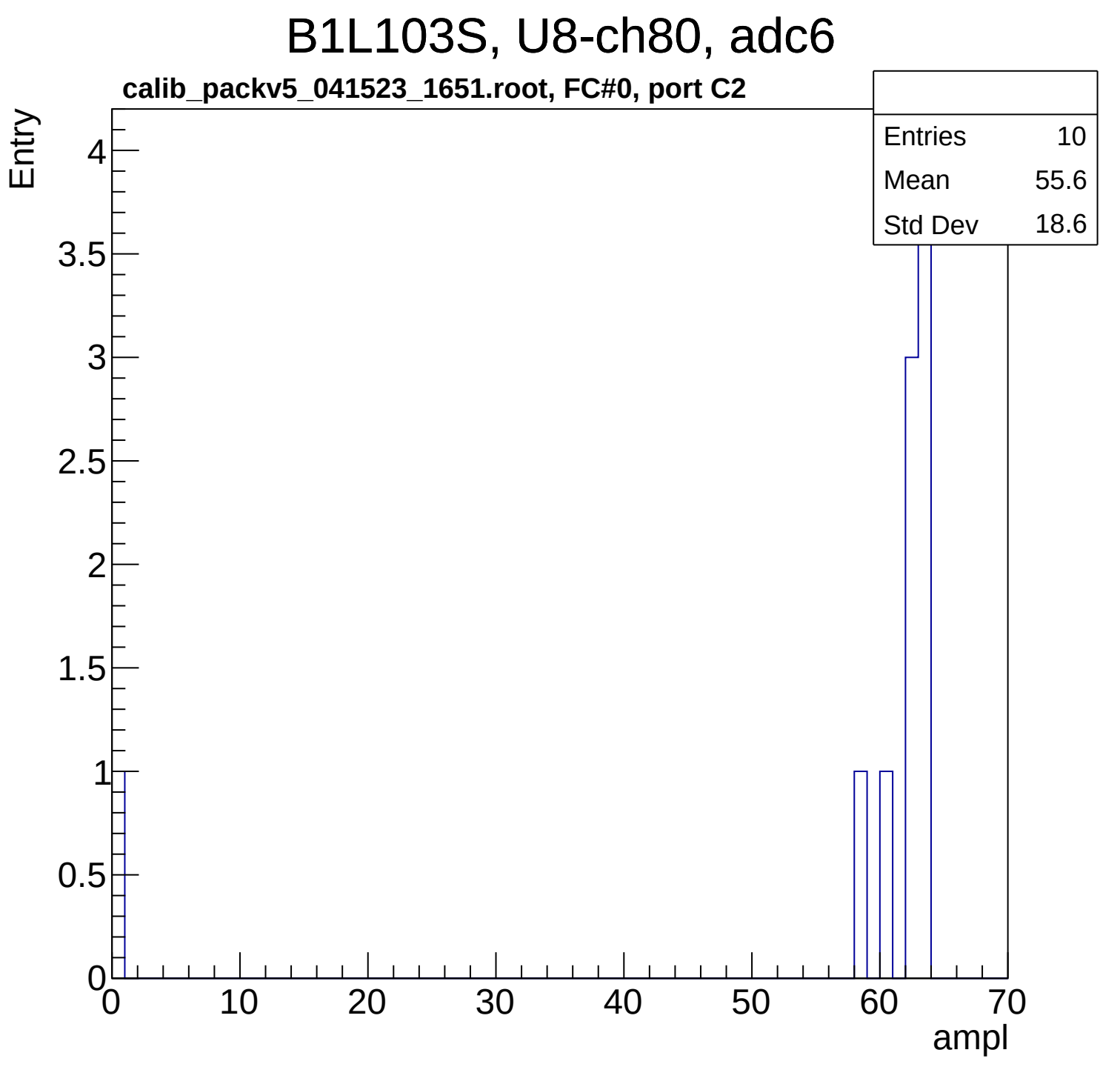
B1L103S, U8-ch80, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 55.6
Std Dev 18.6
Entry
ampl
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0.5
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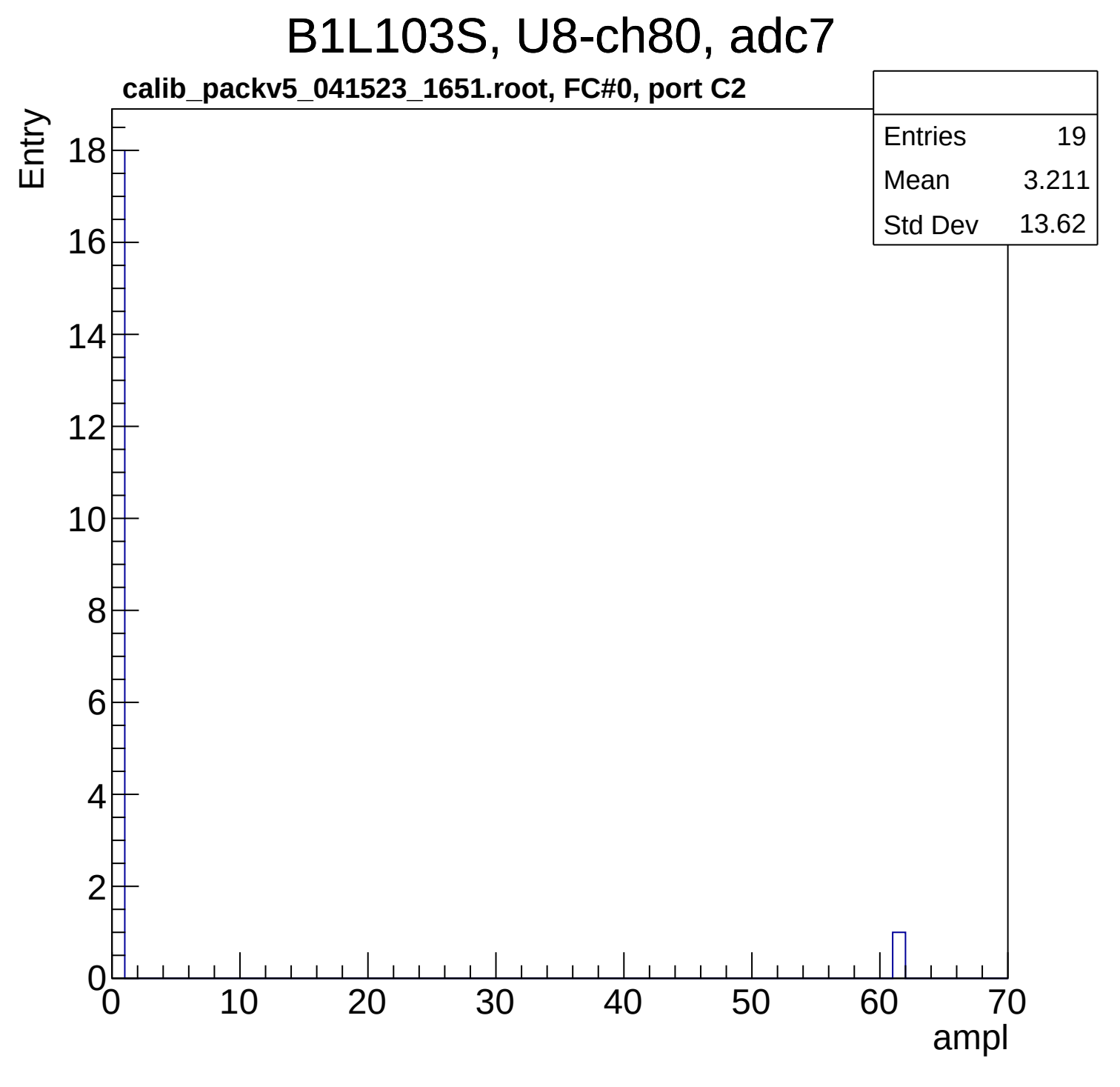
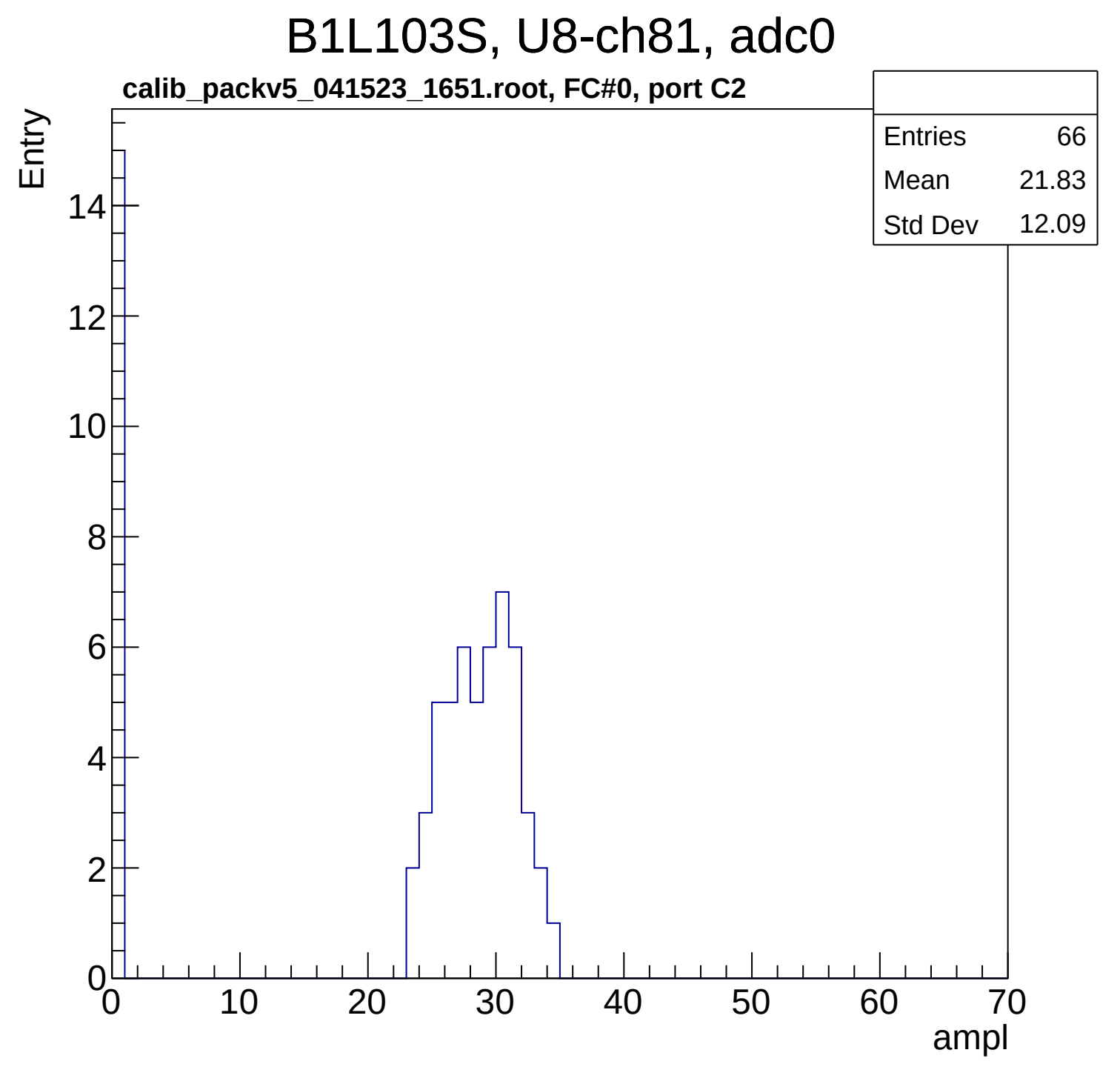
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U8-ch80, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.211
Std Dev 13.62
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch81, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 21.83
Std Dev 12.09
Entry
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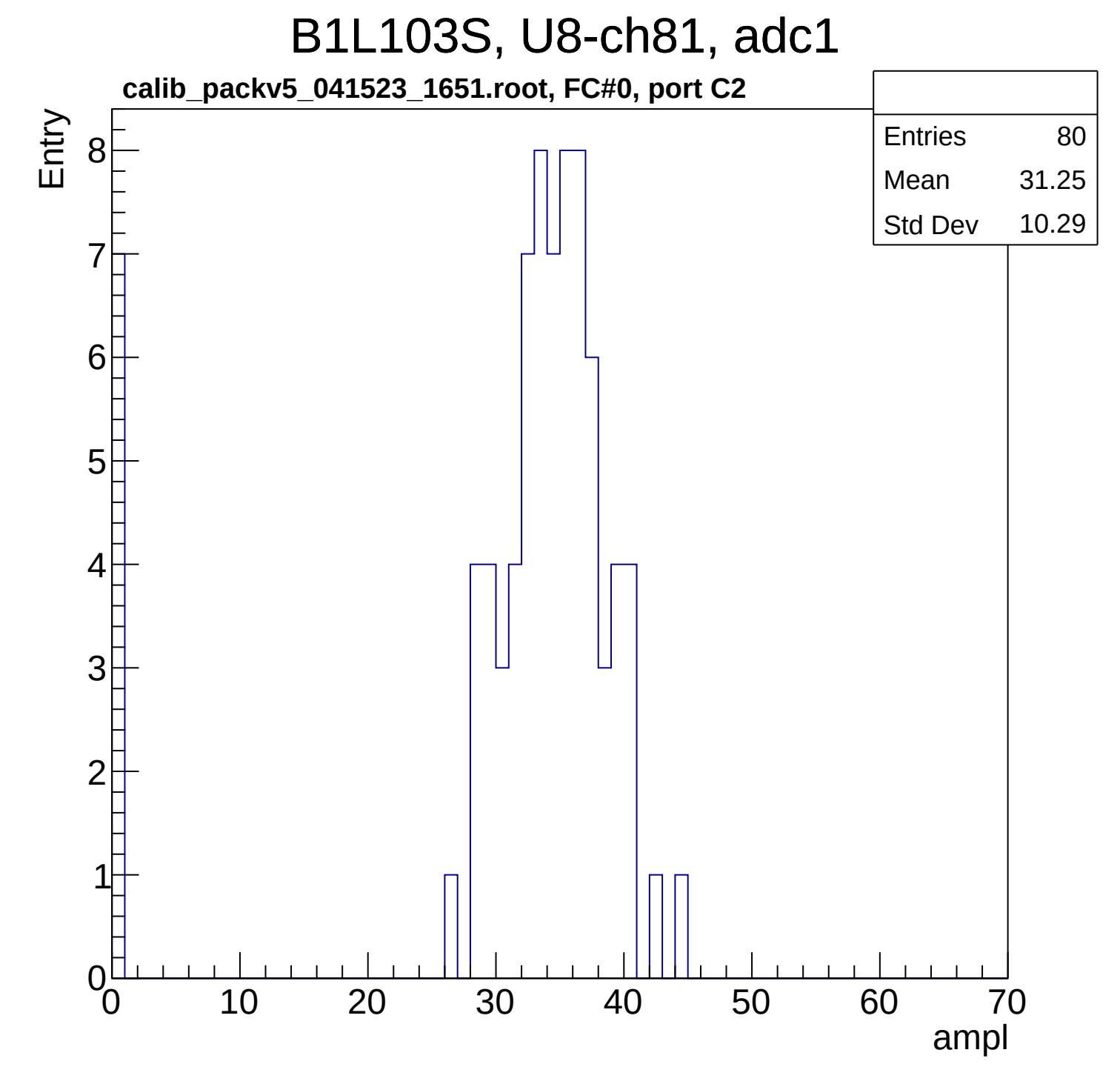
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch81, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 31.25
Std Dev 10.29
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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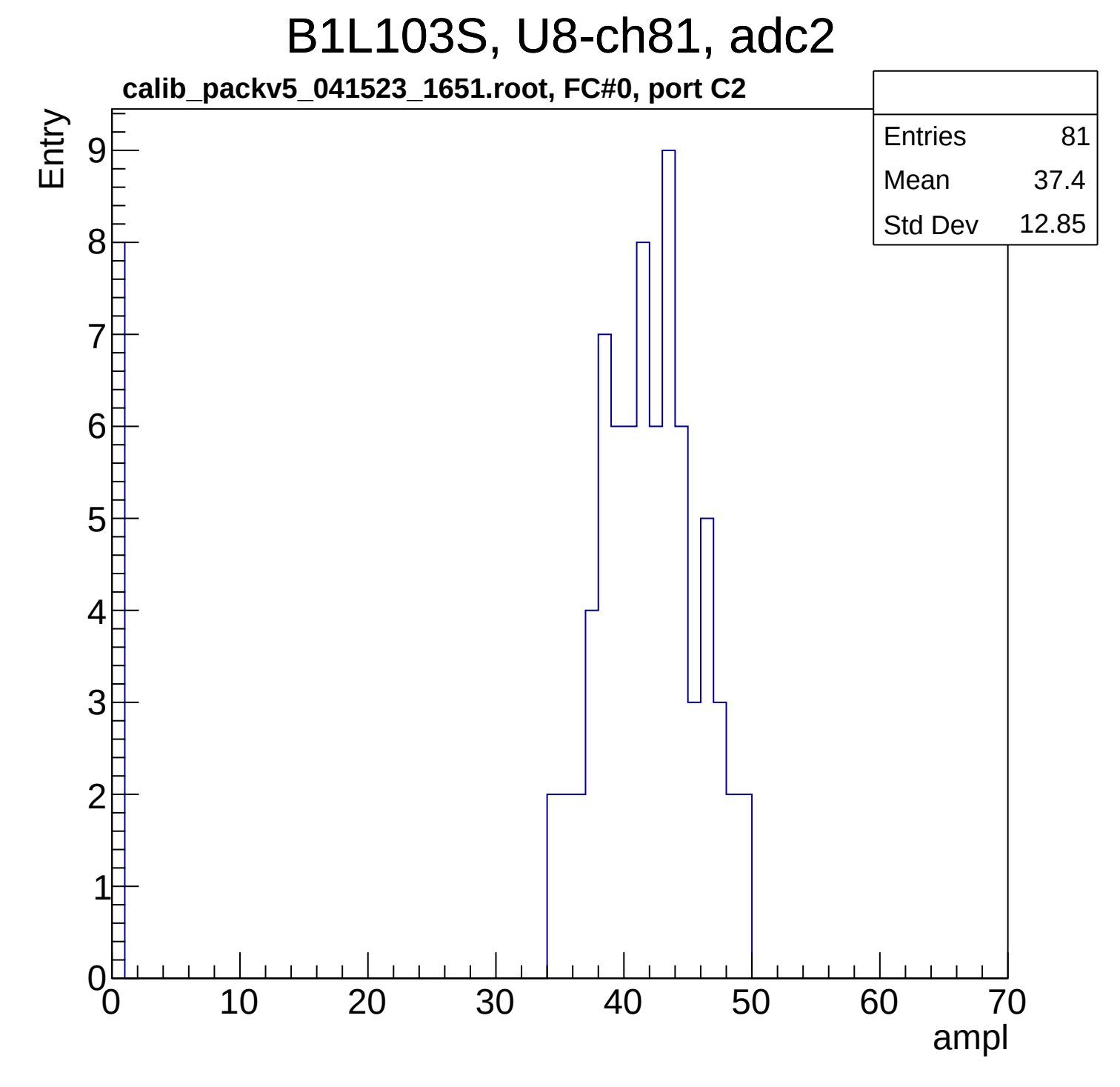
B1L103S, U8-ch81, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 37.4
Std Dev 12.85
Entry
ampl
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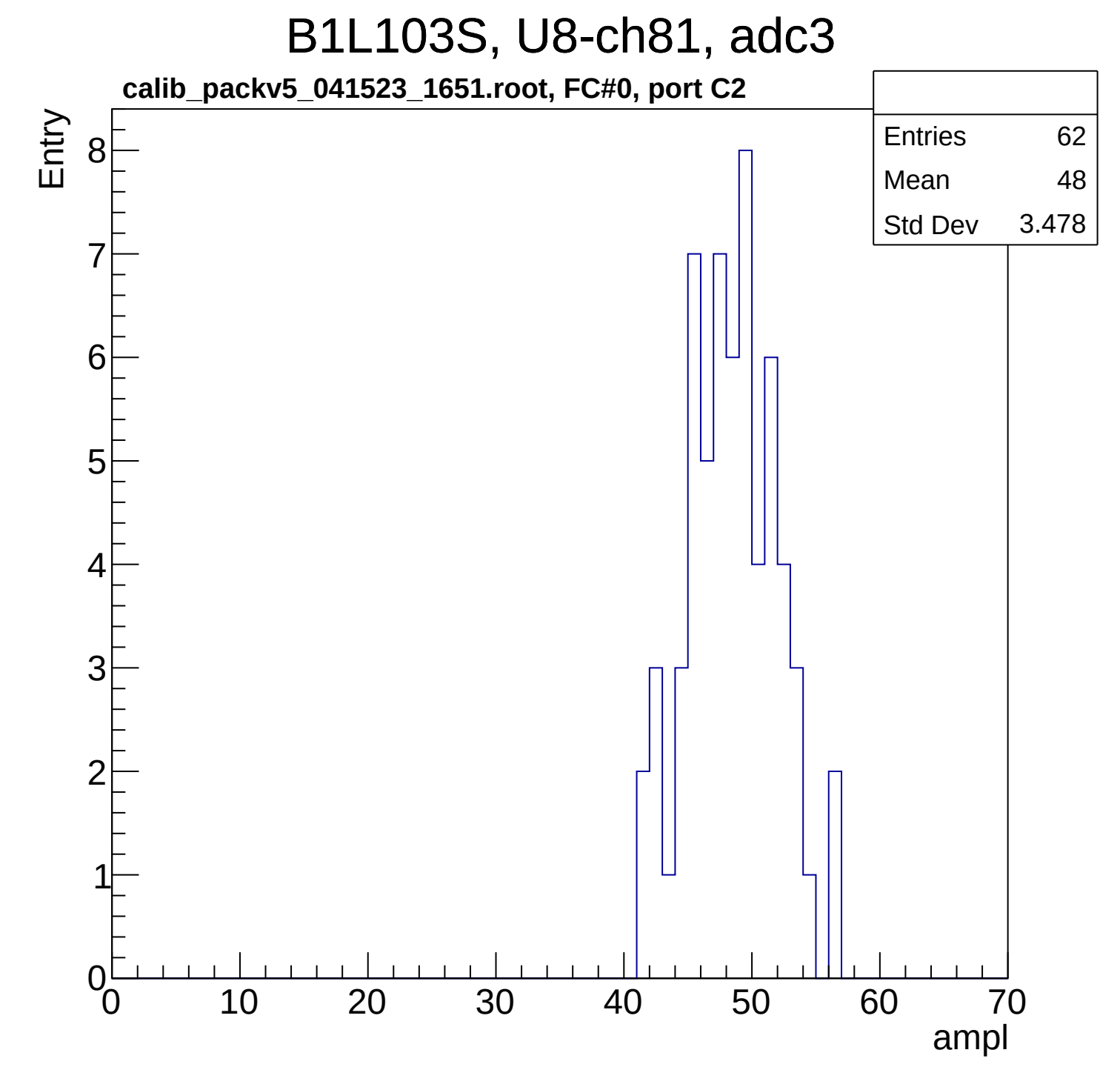
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U8-ch81, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 48
Std Dev 3.478
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
50
60
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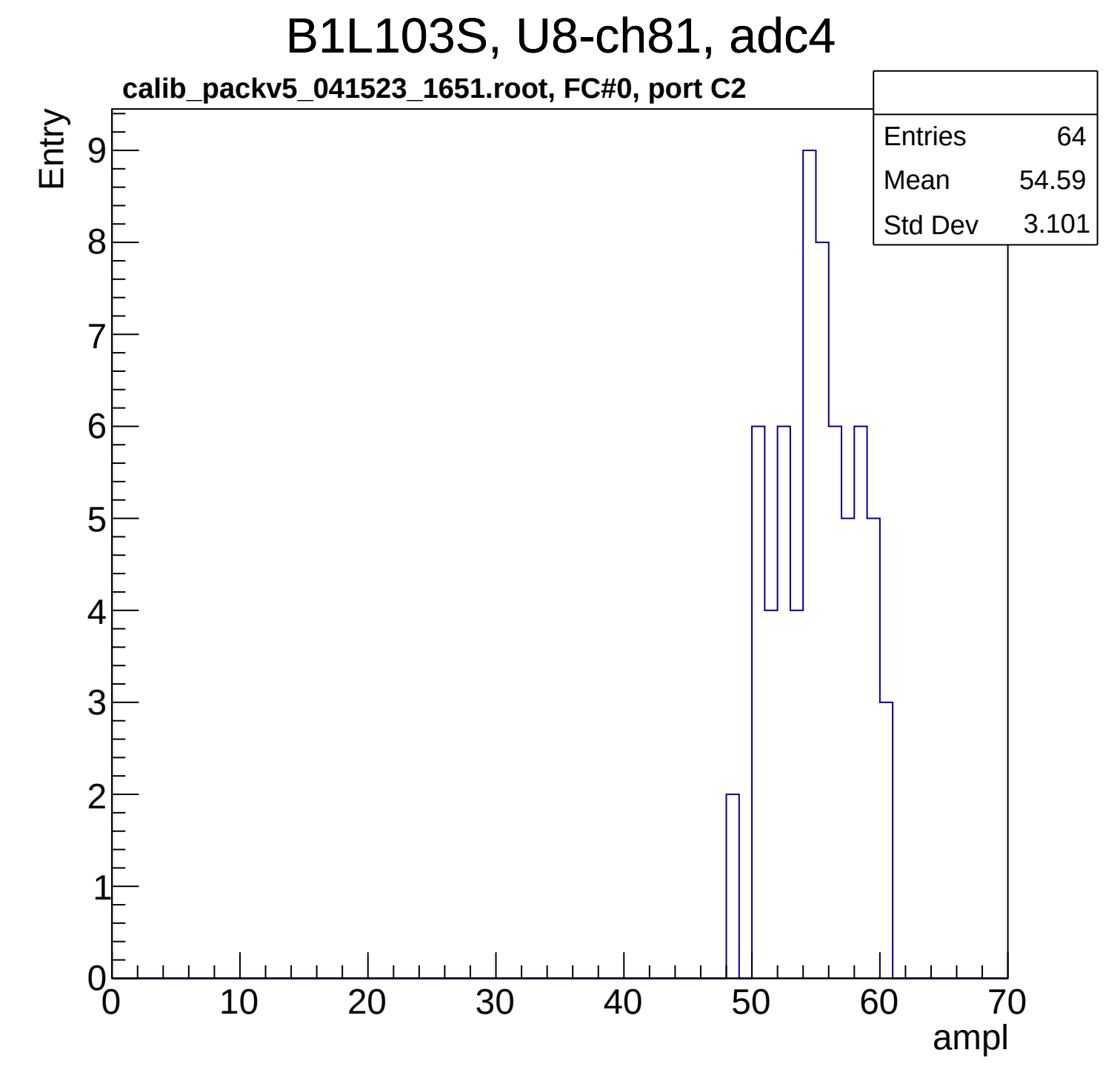
B1L103S, U8-ch81, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 54.59
Std Dev 3.101
Entry
ampl
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3
4
5
6
7
8
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0
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60
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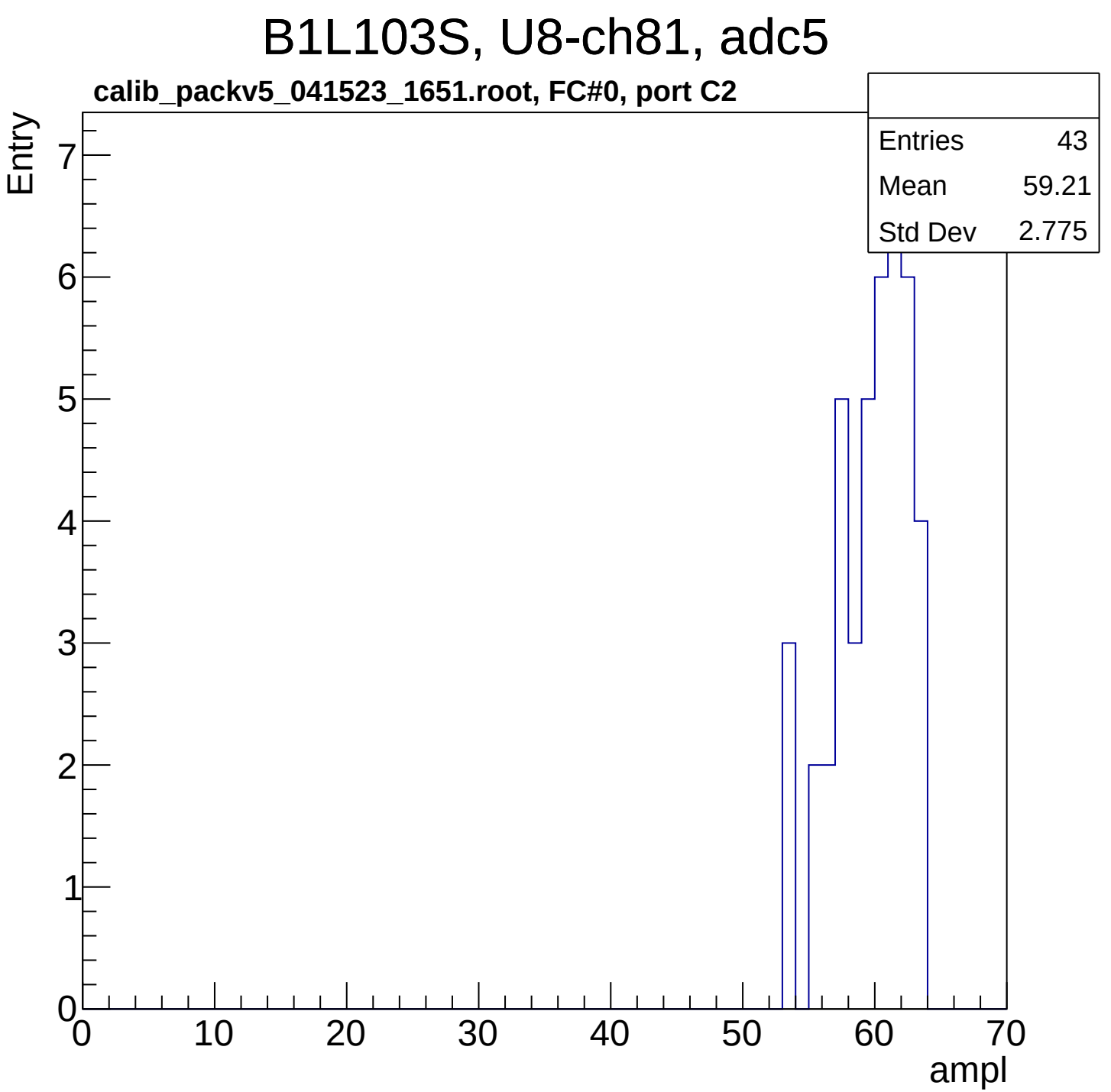
B1L103S, U8-ch81, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 59.21
Std Dev 2.775
Entry
ampl
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2
3
4
5
6
7
0
10
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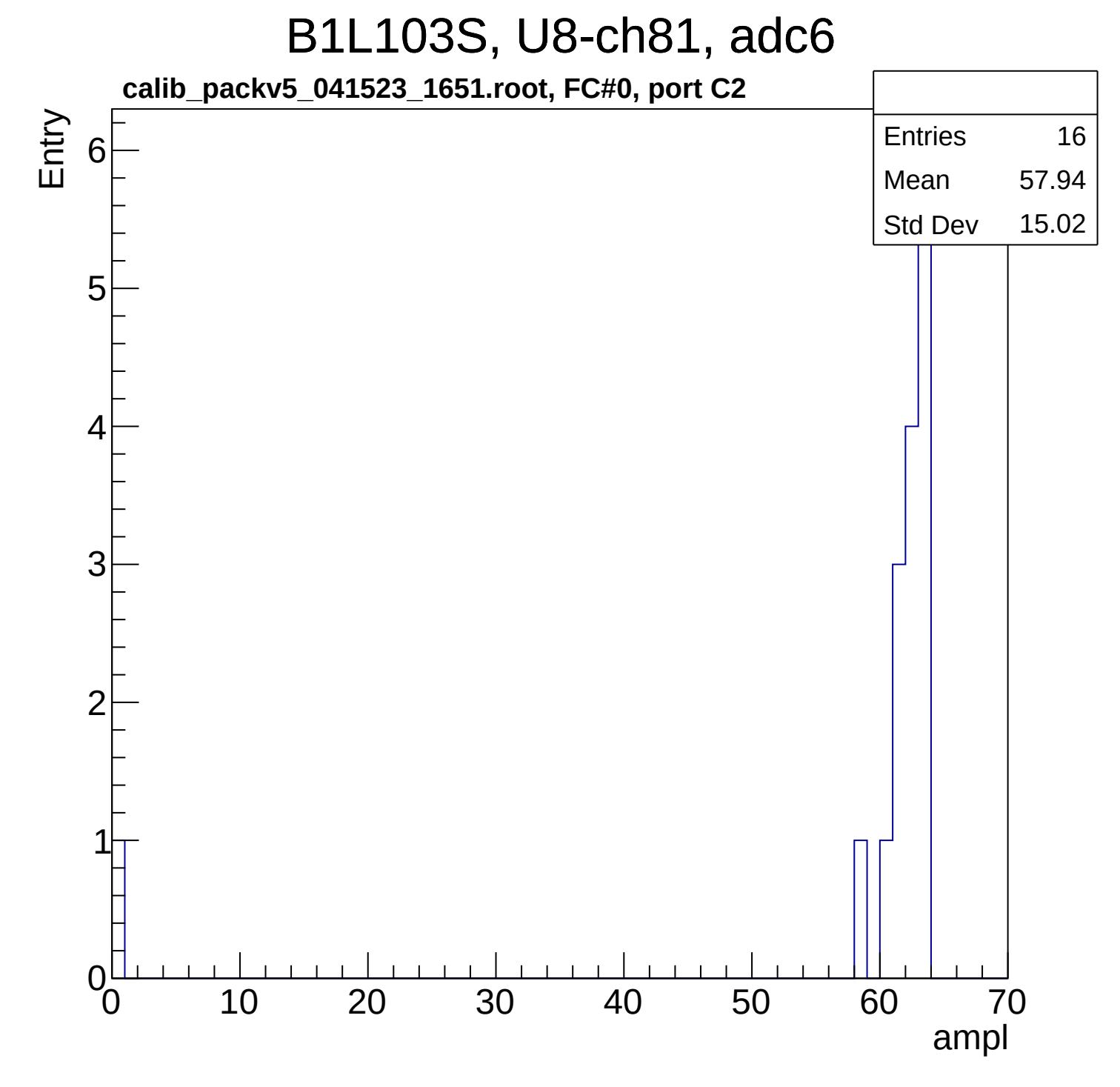
30
40
50
60
70


B1L103S, U8-ch81, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 57.94
Std Dev 15.02
Entry
ampl
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3
4
5
6
0
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60
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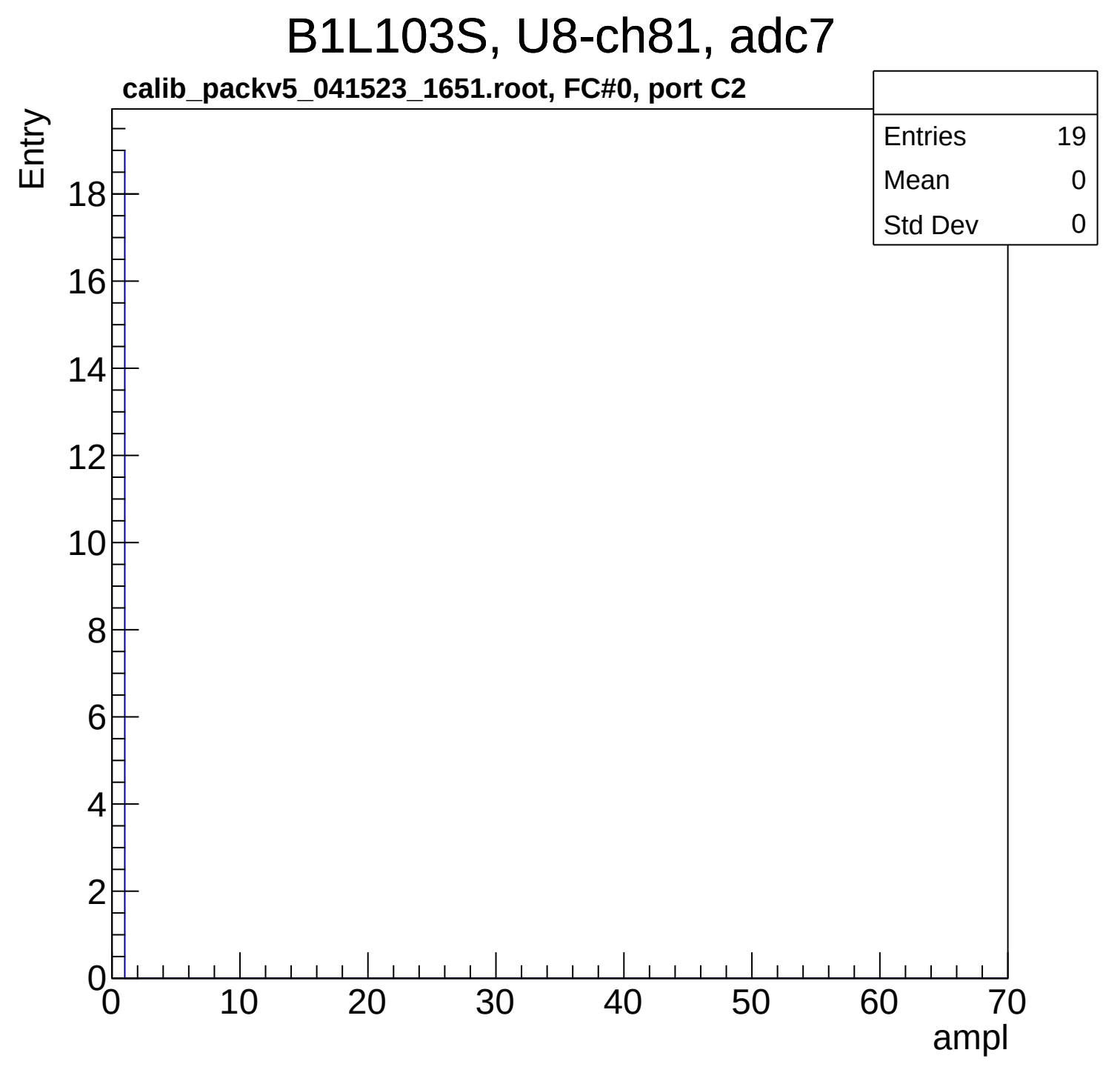
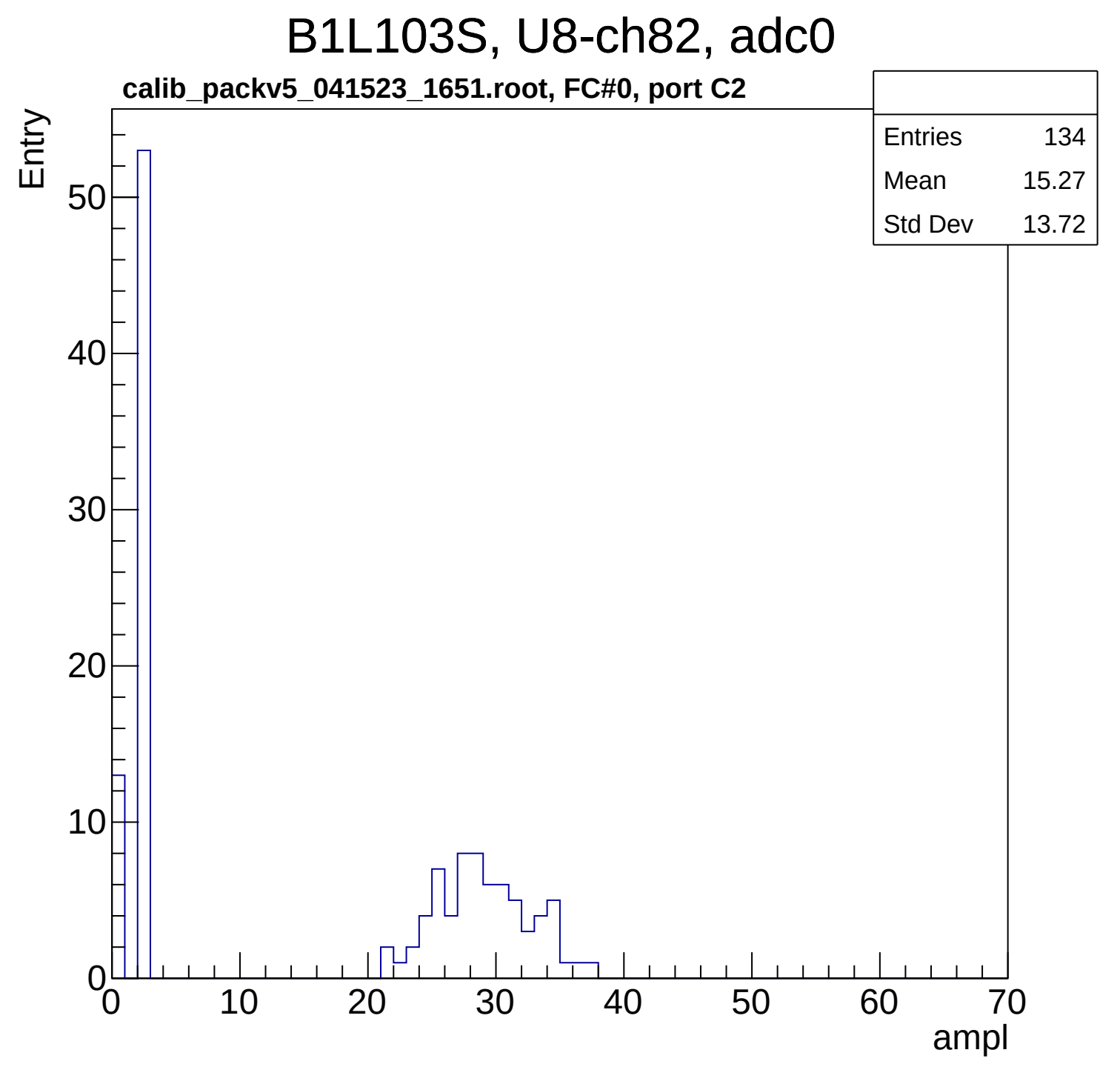

B1L103S, U8-ch81, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch82, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 134
Mean 15.27
Std Dev 13.72
Entry
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10
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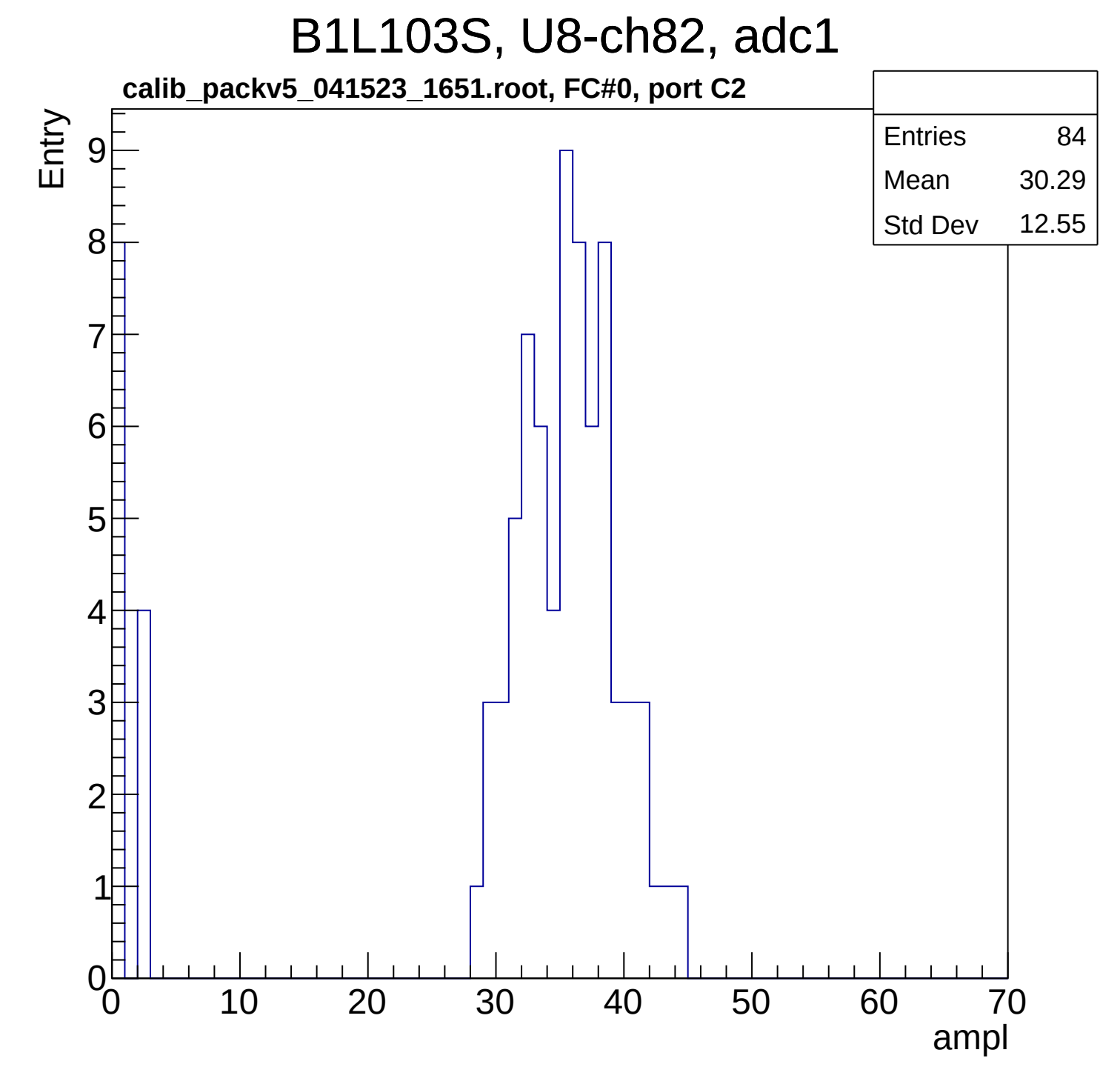
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch82, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 30.29
Std Dev 12.55
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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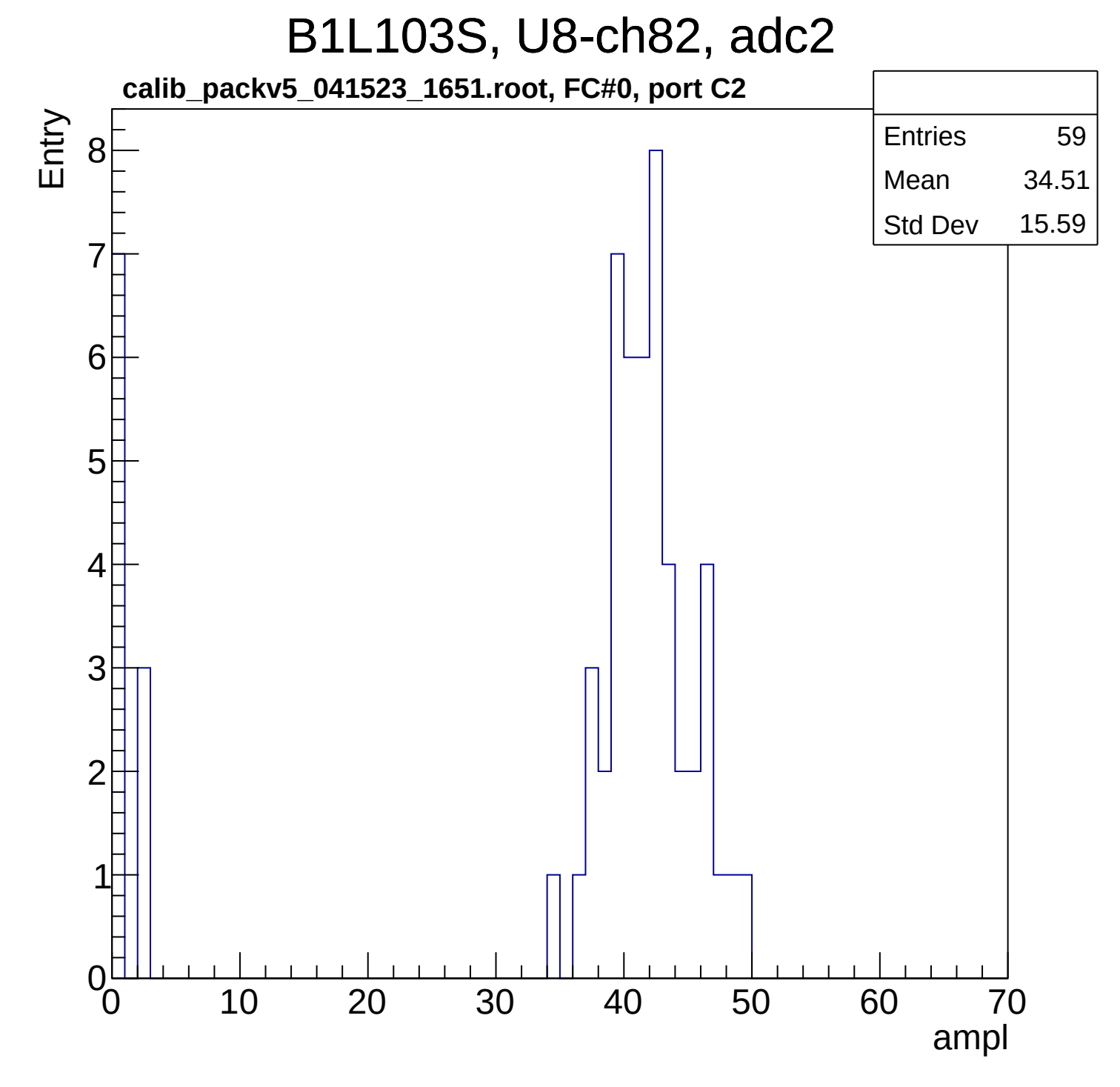
B1L103S, U8-ch82, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 34.51
Std Dev 15.59
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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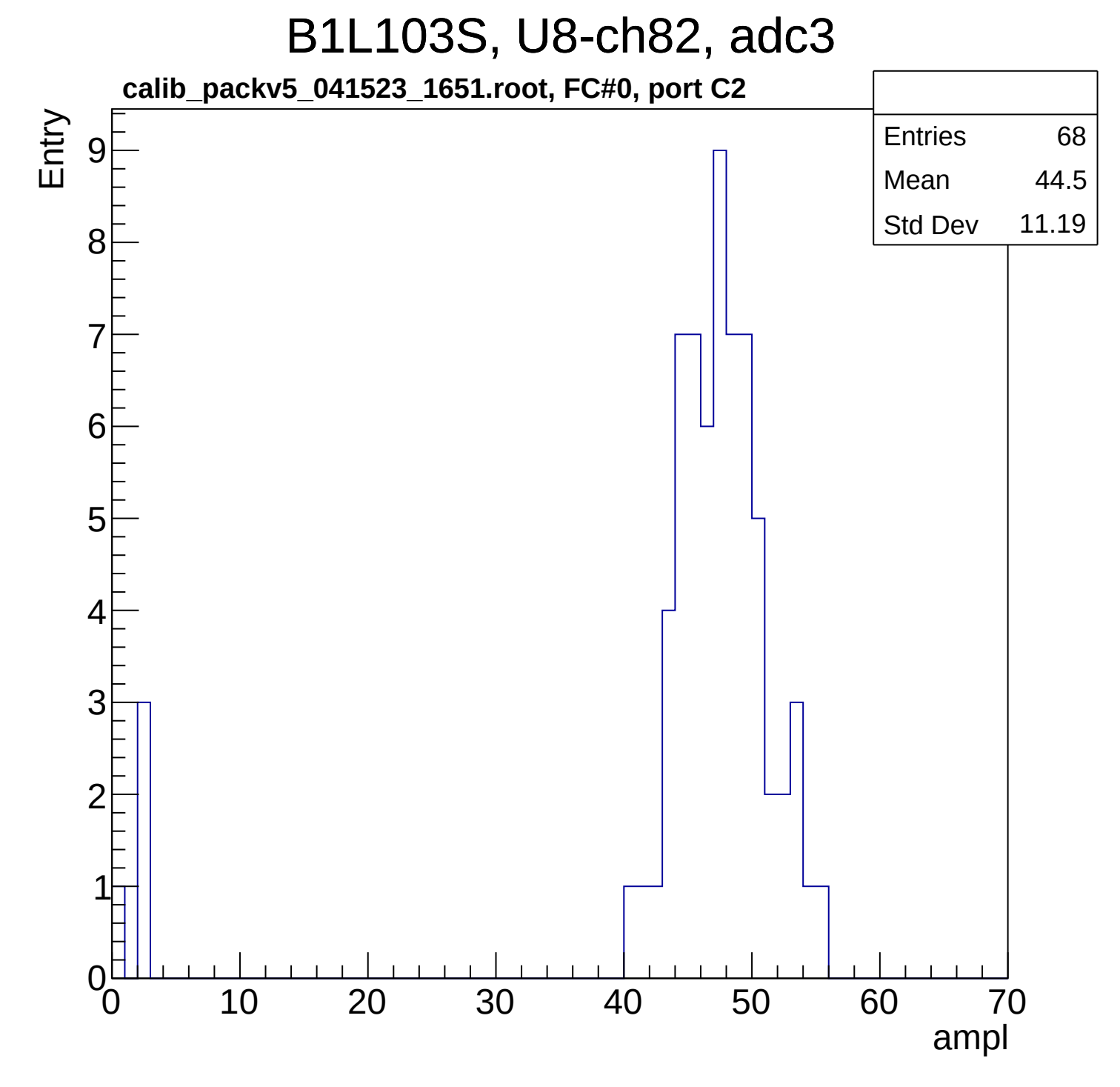
40
50
60
70


B1L103S, U8-ch82, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 44.5
Std Dev 11.19
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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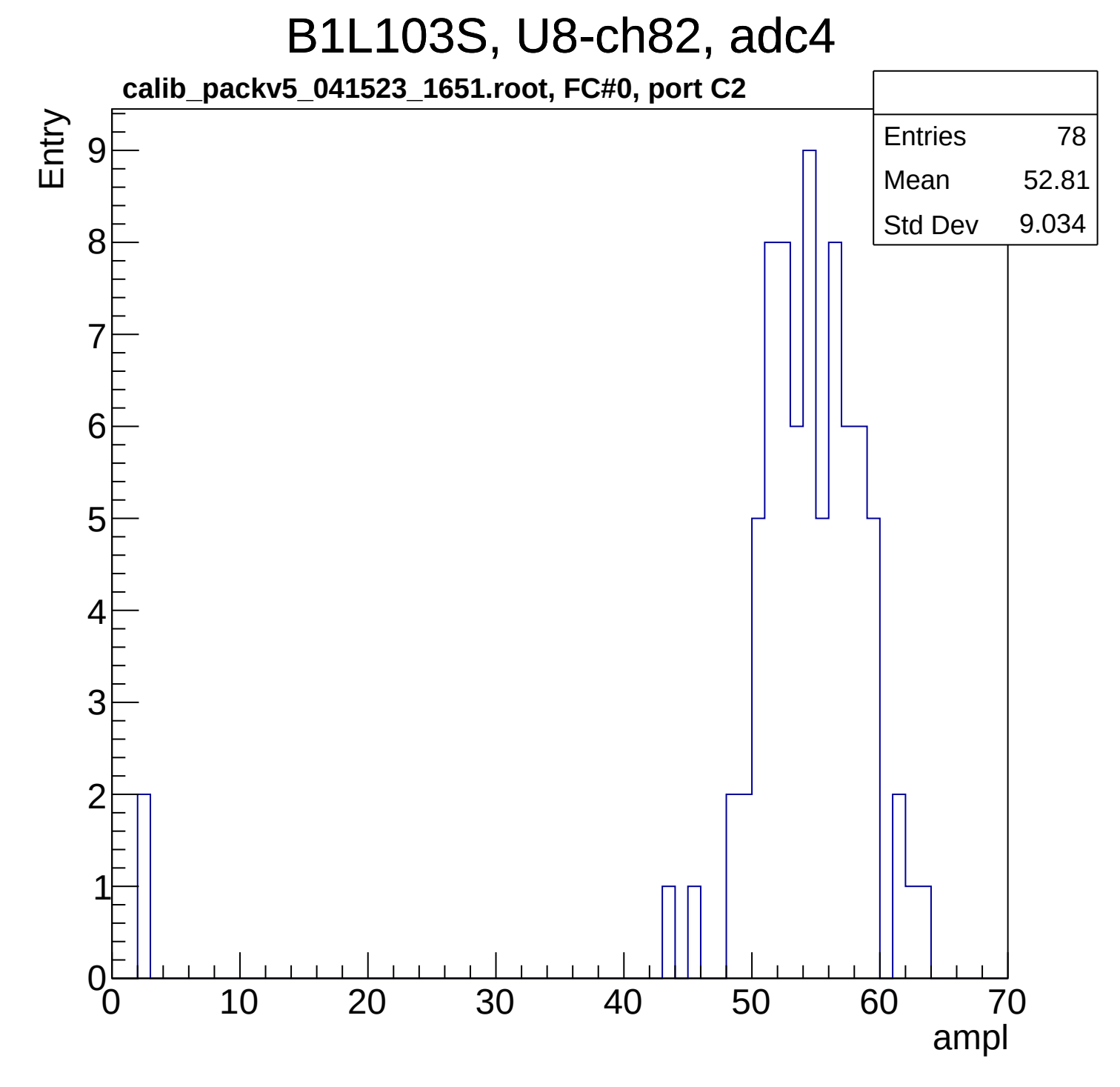
B1L103S, U8-ch82, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 52.81
Std Dev 9.034
Entry
ampl
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3
4
5
6
7
8
9
0
10
20
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40
50
60
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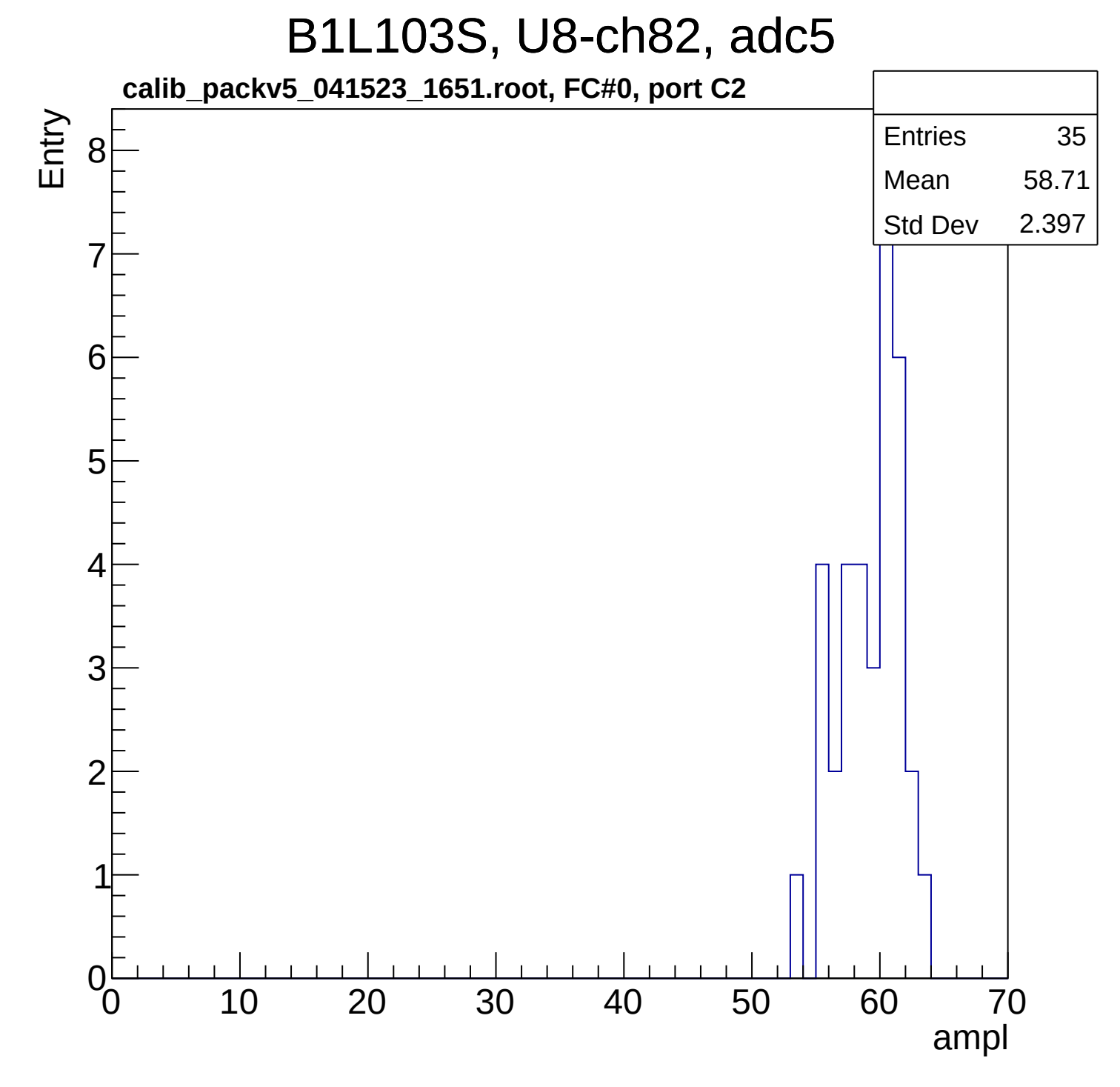
B1L103S, U8-ch82, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 58.71
Std Dev 2.397
Entry
ampl
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3
4
5
6
7
8
0
10
20
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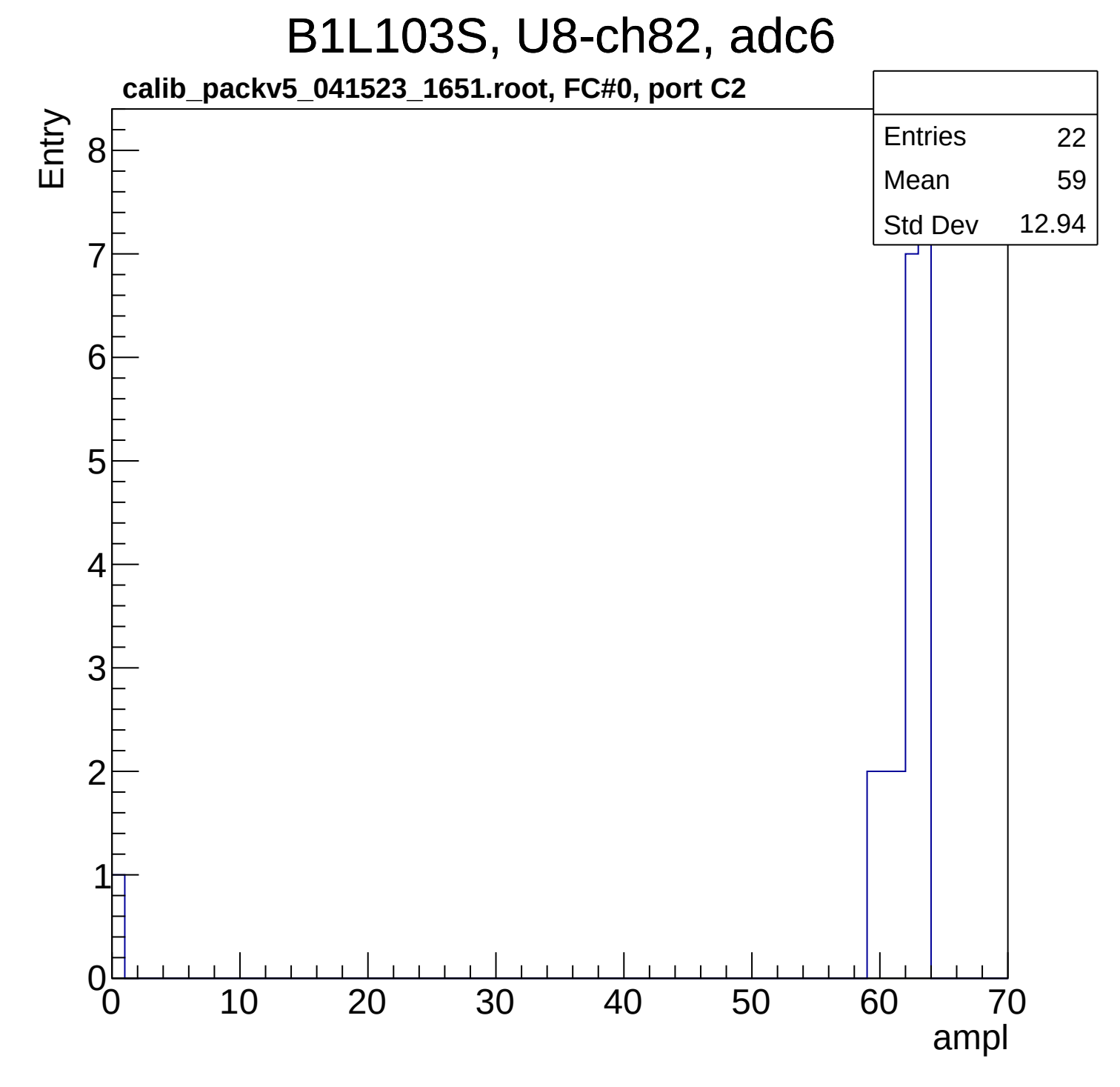
40
50
60
70


B1L103S, U8-ch82, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 59
Std Dev 12.94
Entry
ampl
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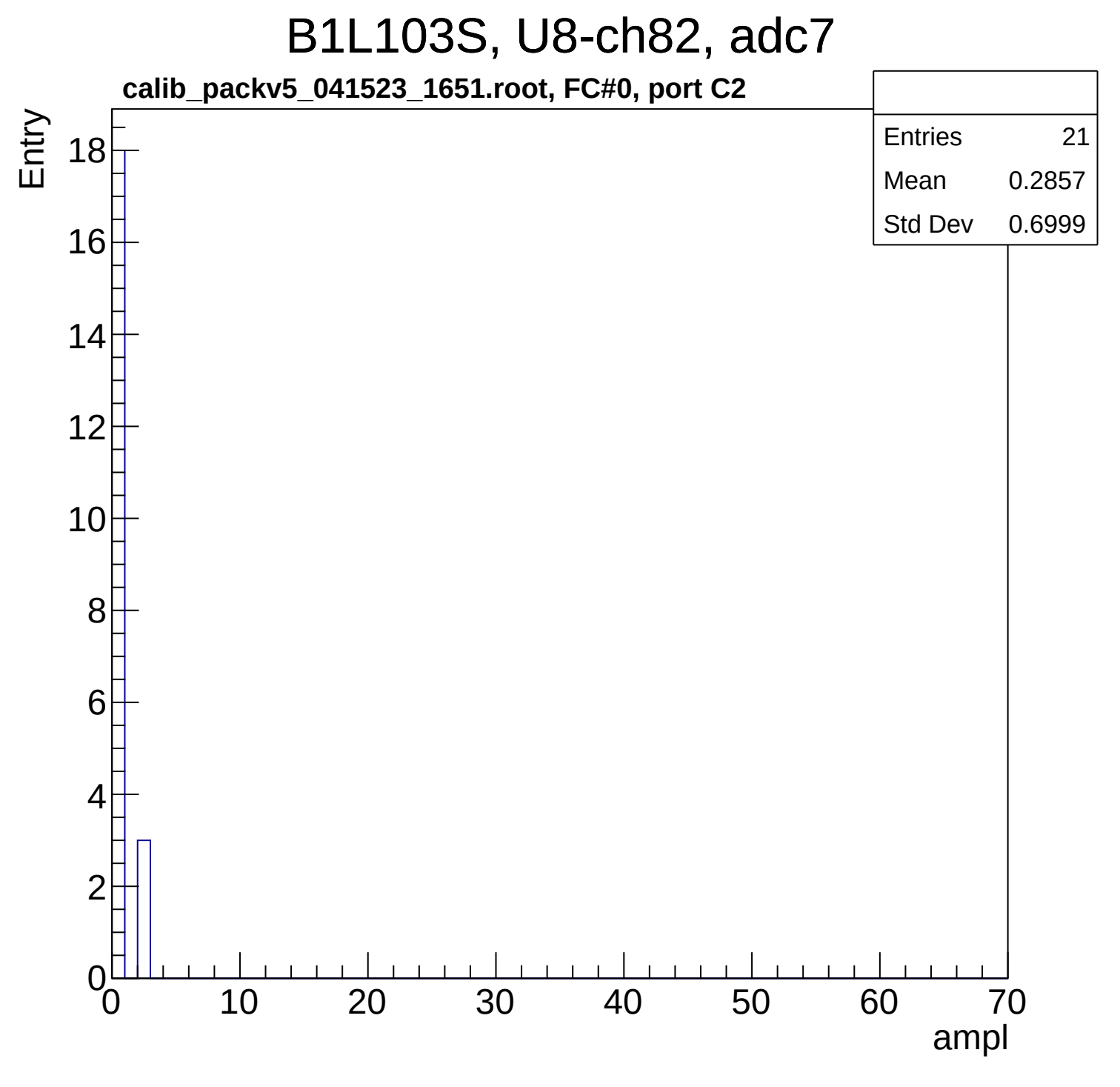
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch82, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 0.2857
Std Dev 0.6999
Entry
ampl
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6
8
10
12
14
16
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0
10
20
30
40
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60
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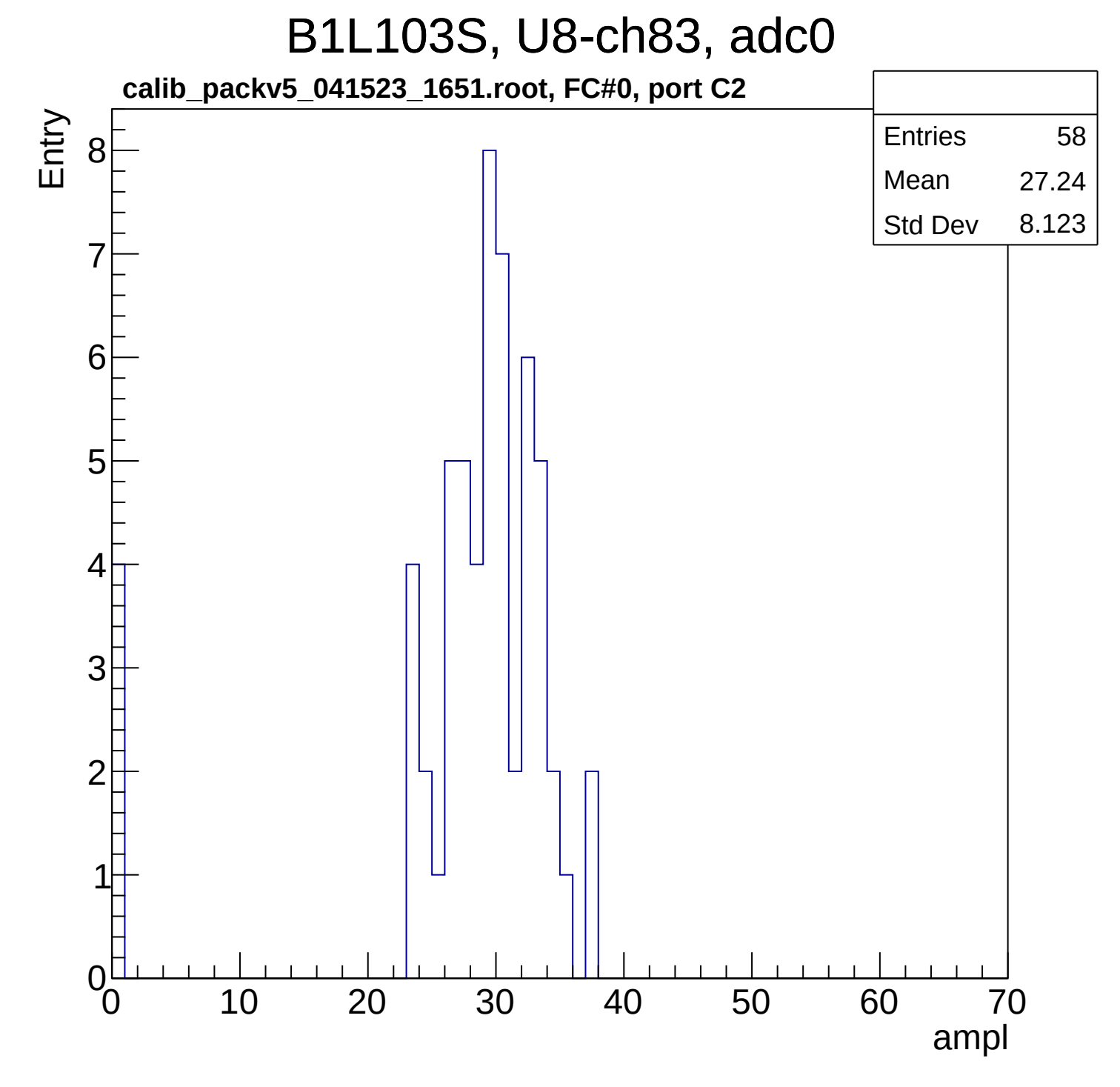
B1L103S, U8-ch83, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 27.24
Std Dev 8.123
Entry
ampl
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4
5
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7
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0
10
20
30
40
50
60
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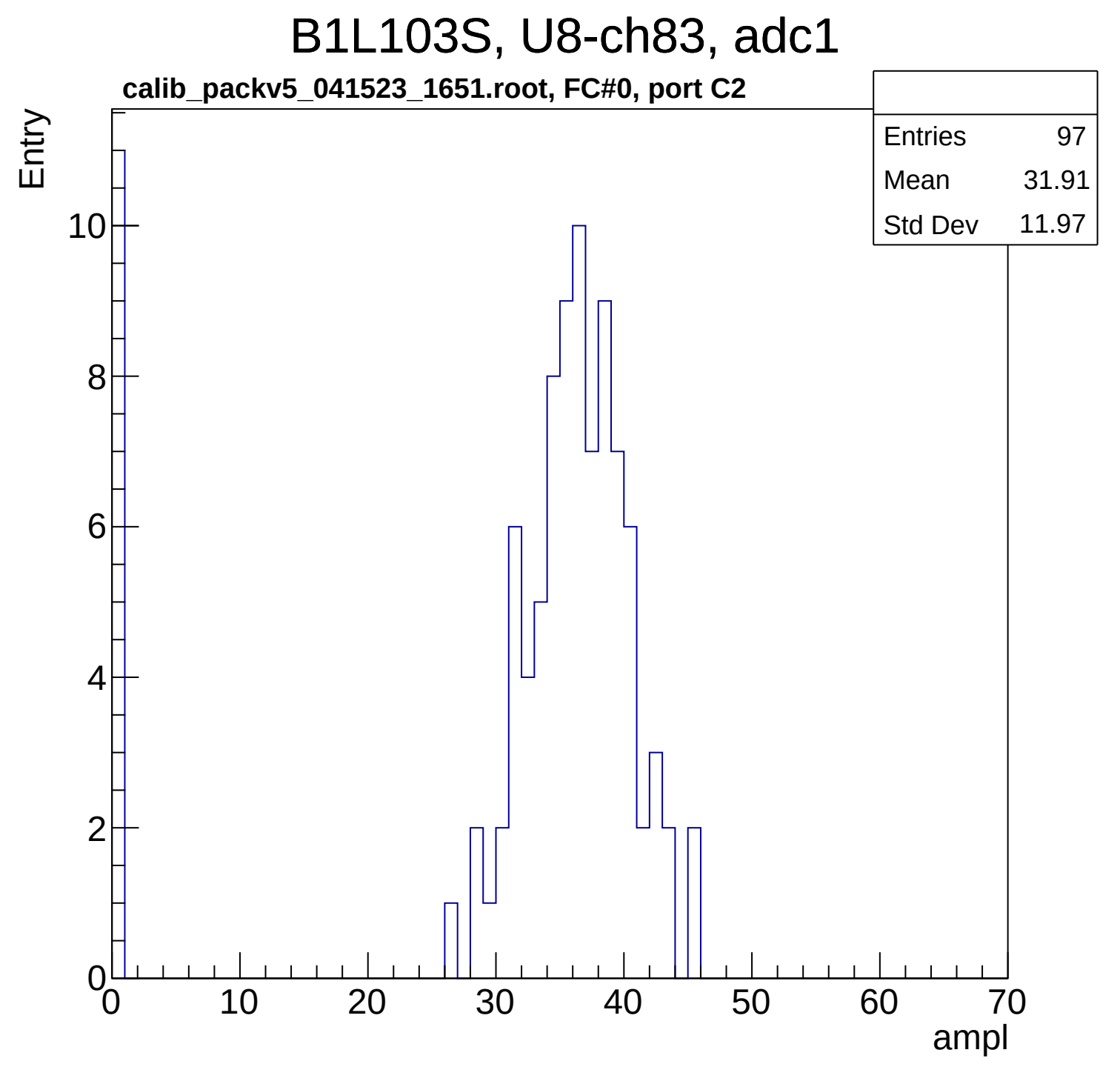
B1L103S, U8-ch83, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 31.91
Std Dev 11.97
Entry
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10
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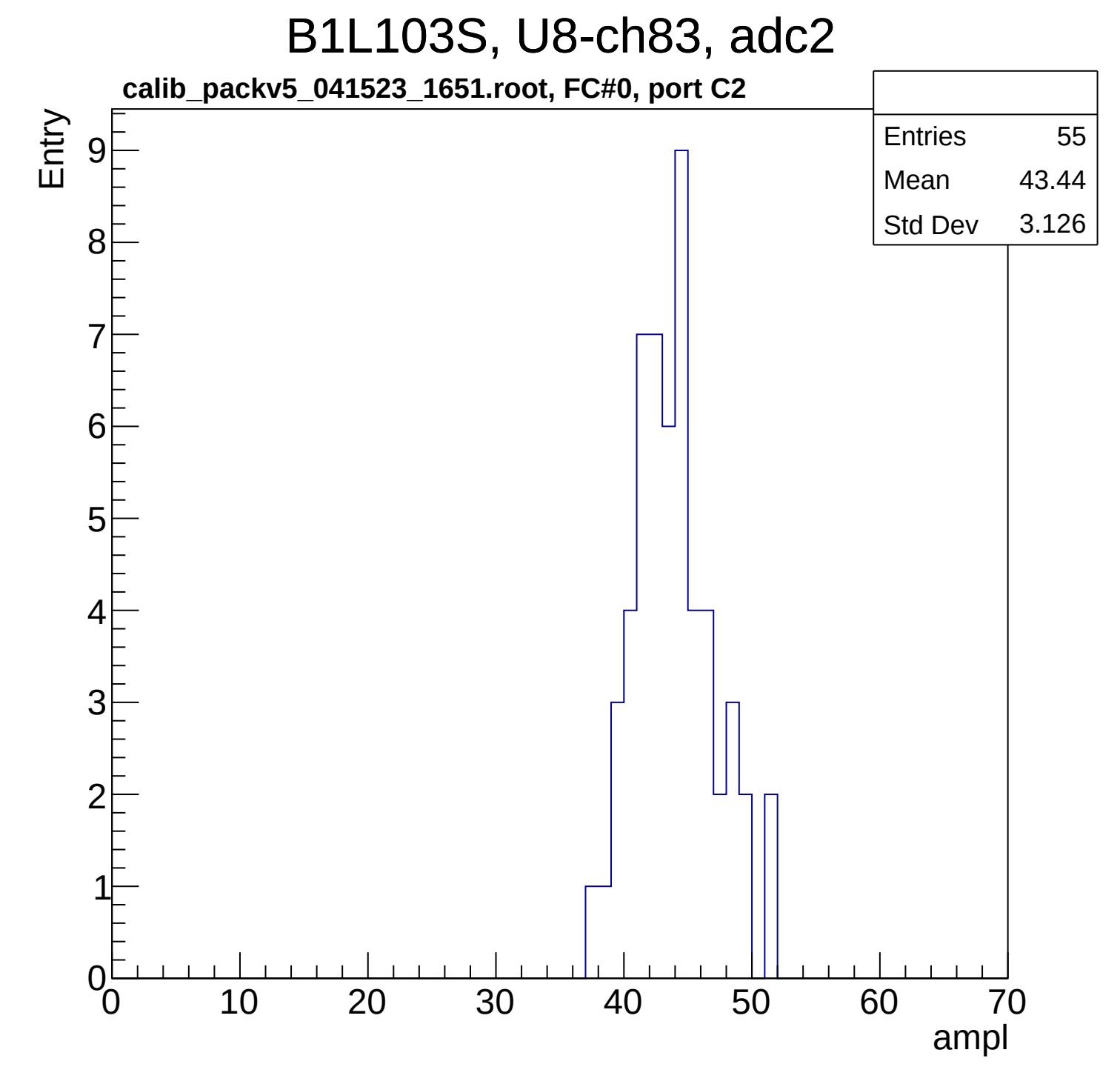
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch83, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 43.44
Std Dev 3.126
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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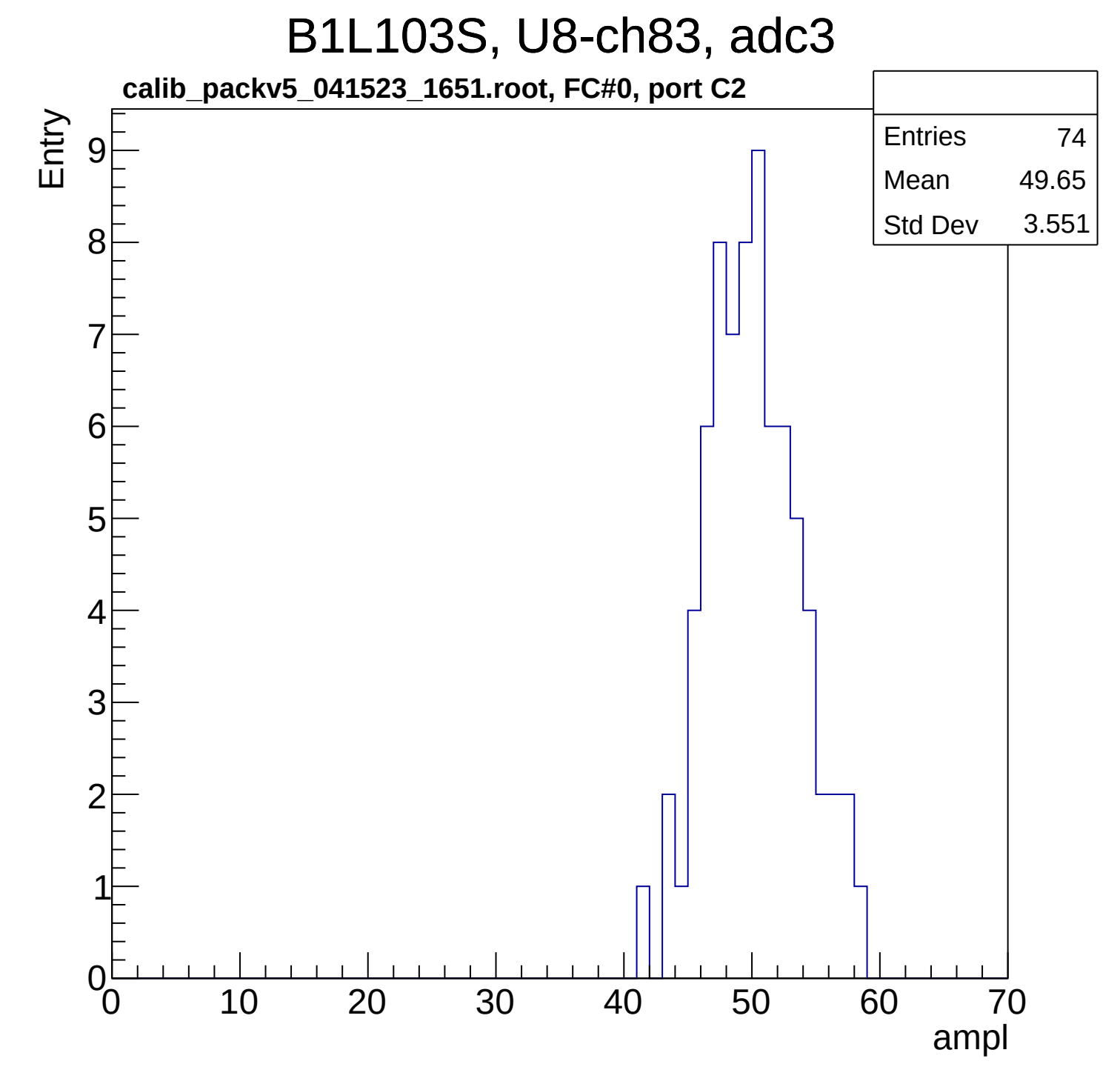
40
50
60
70


B1L103S, U8-ch83, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 49.65
Std Dev 3.551
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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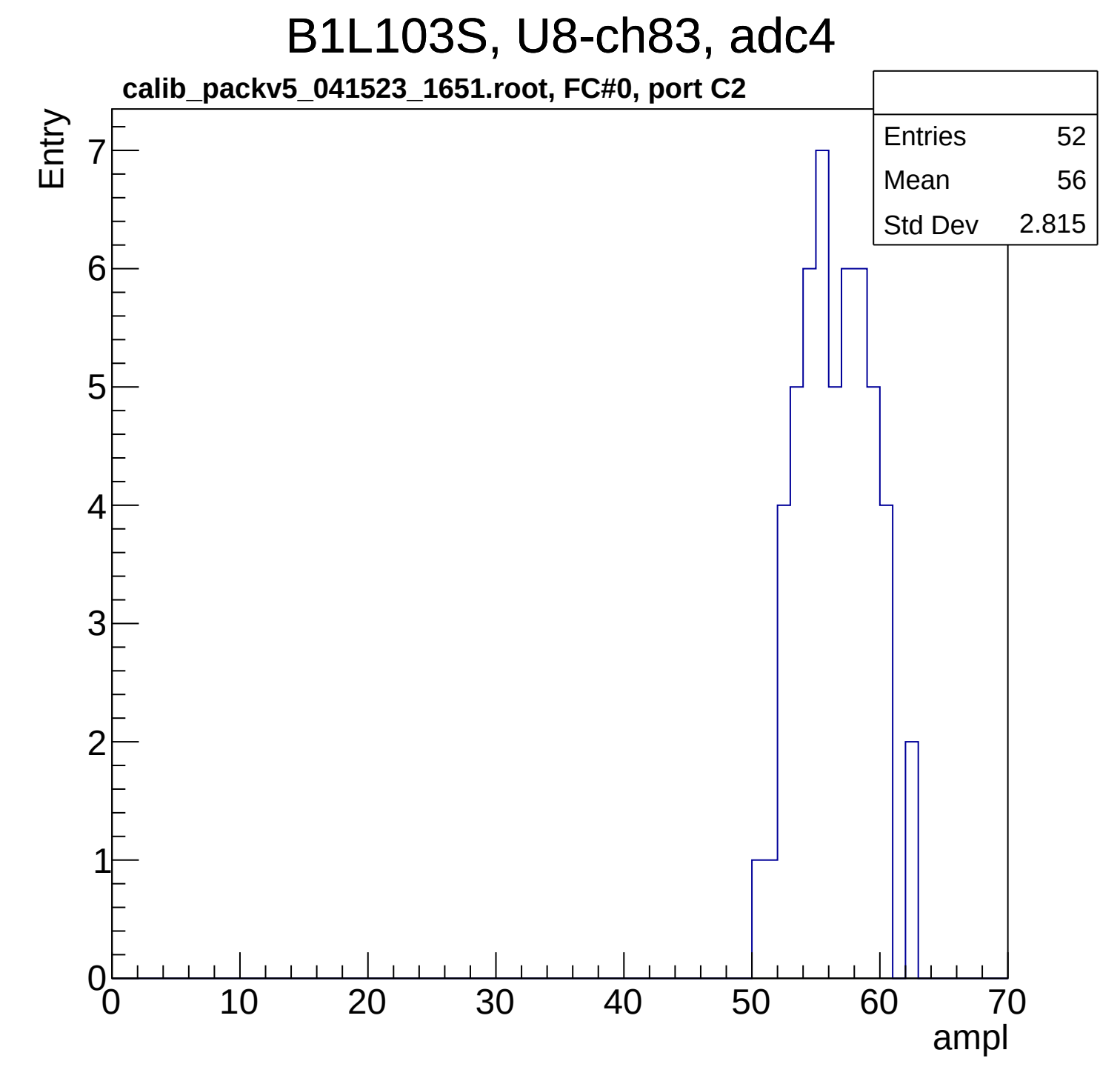
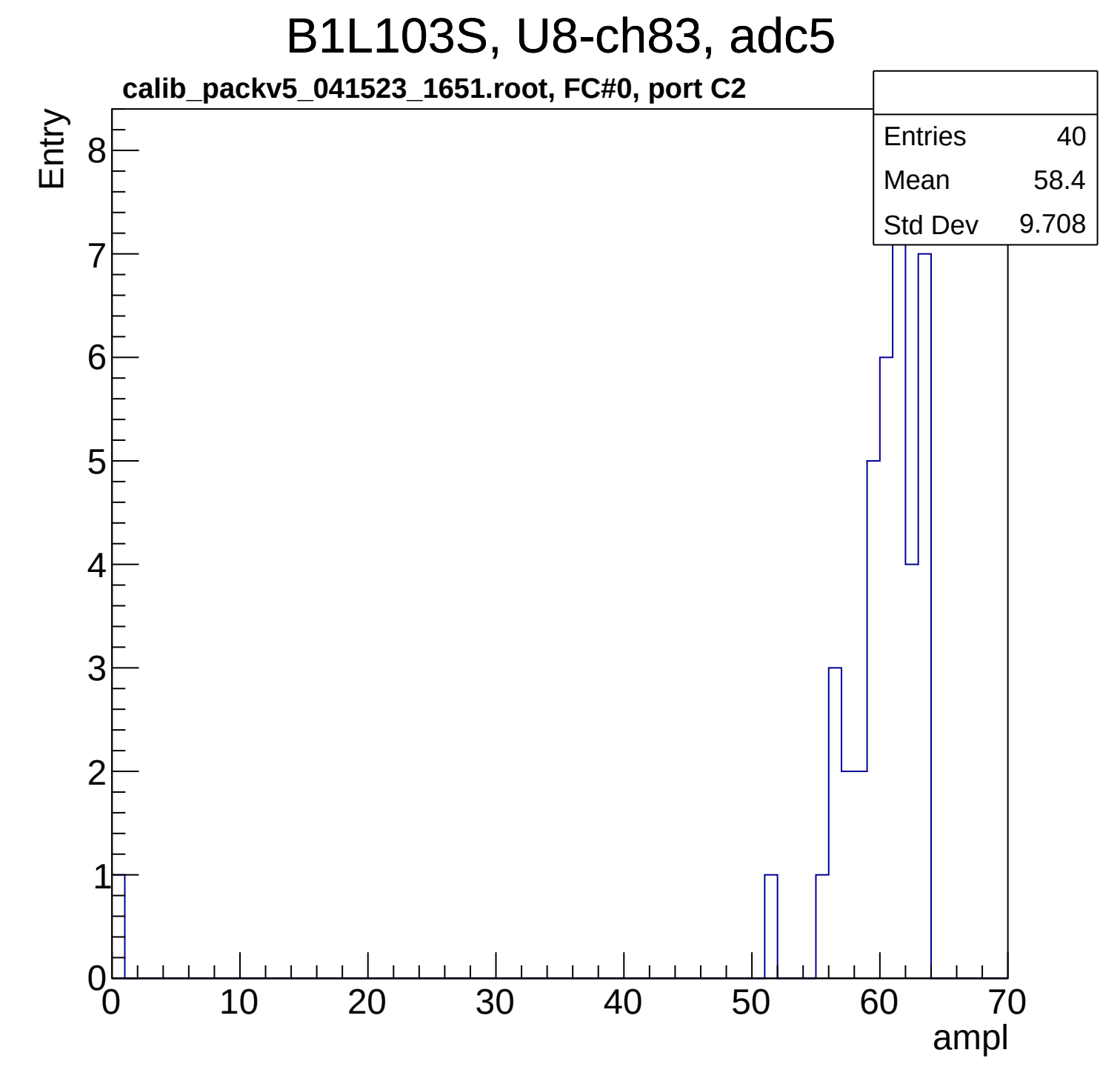
40
50
60
70


B1L103S, U8-ch83, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 56
Std Dev 2.815
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U8-ch83, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 58.4
Std Dev 9.708
Entry
ampl
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1
2
3
4
5
6
7
8
0
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40
50
60
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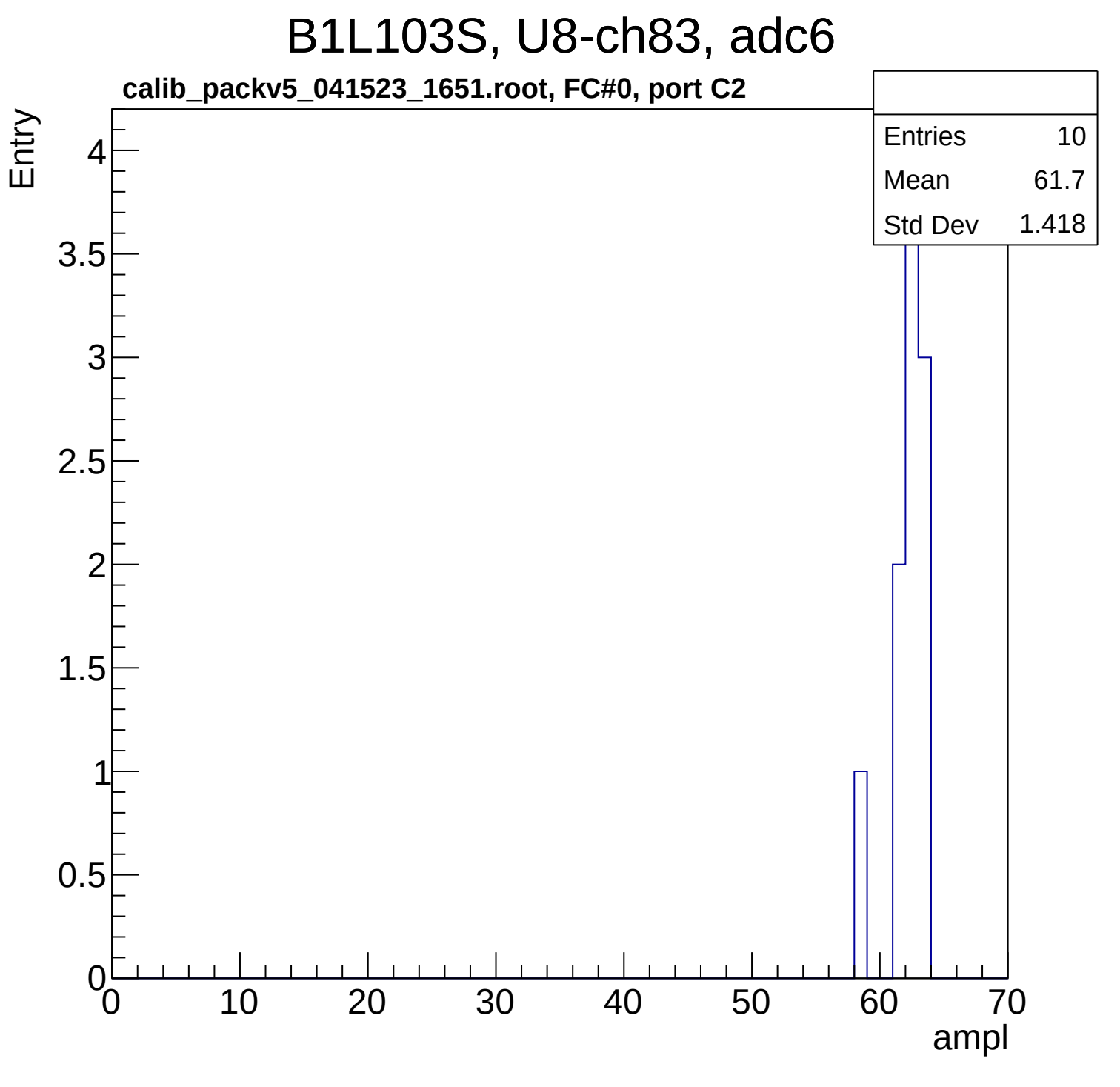
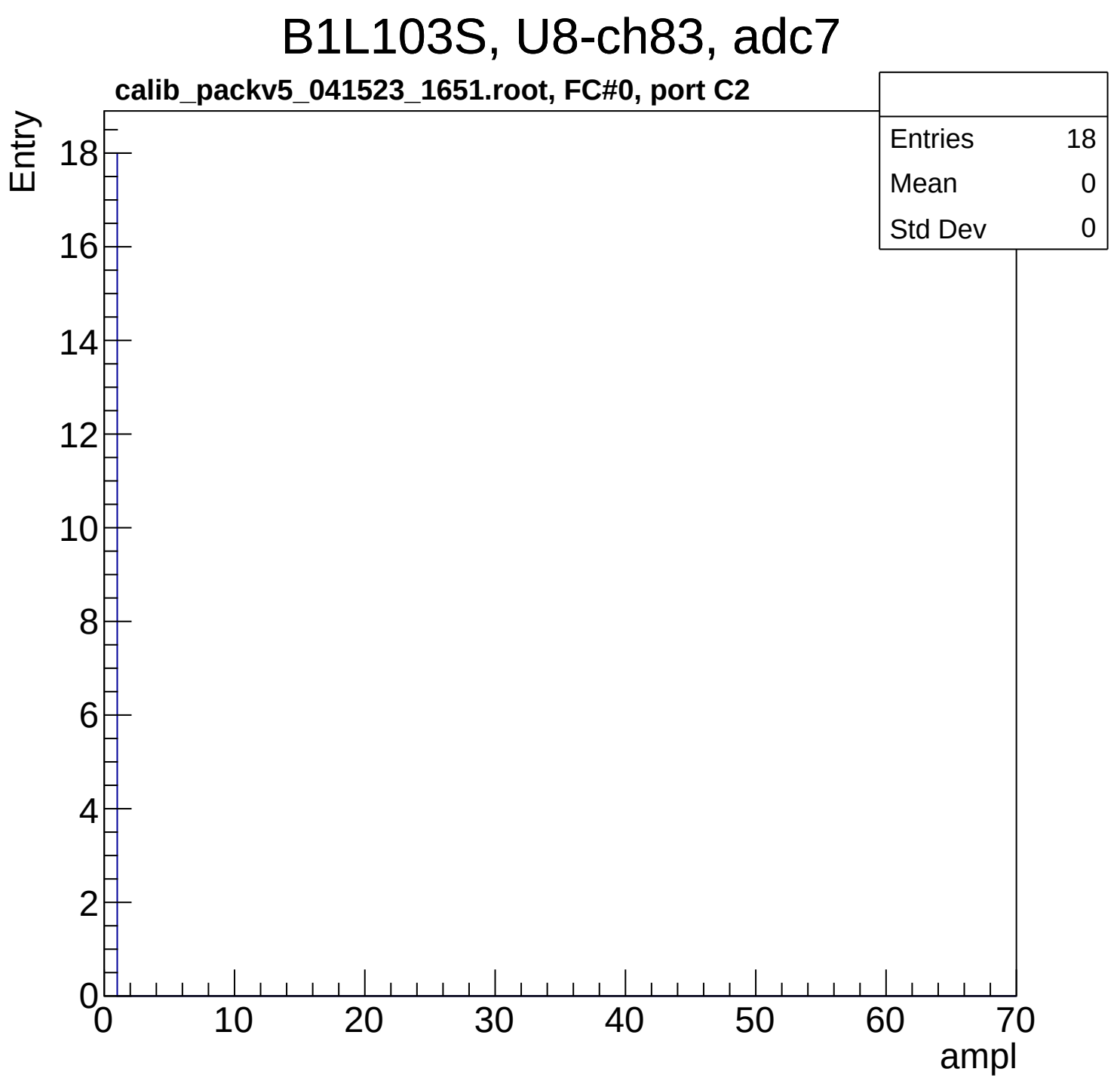
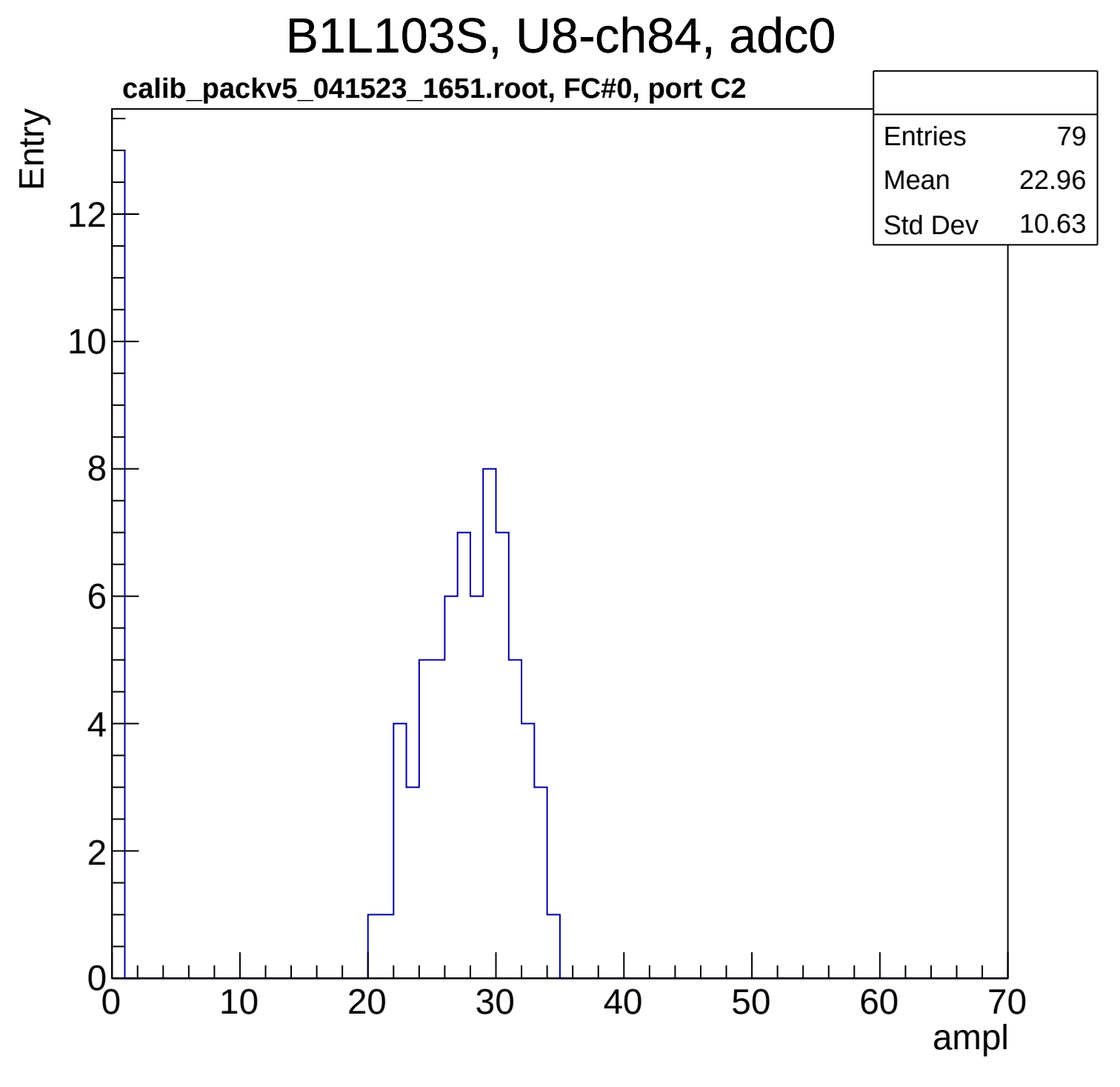
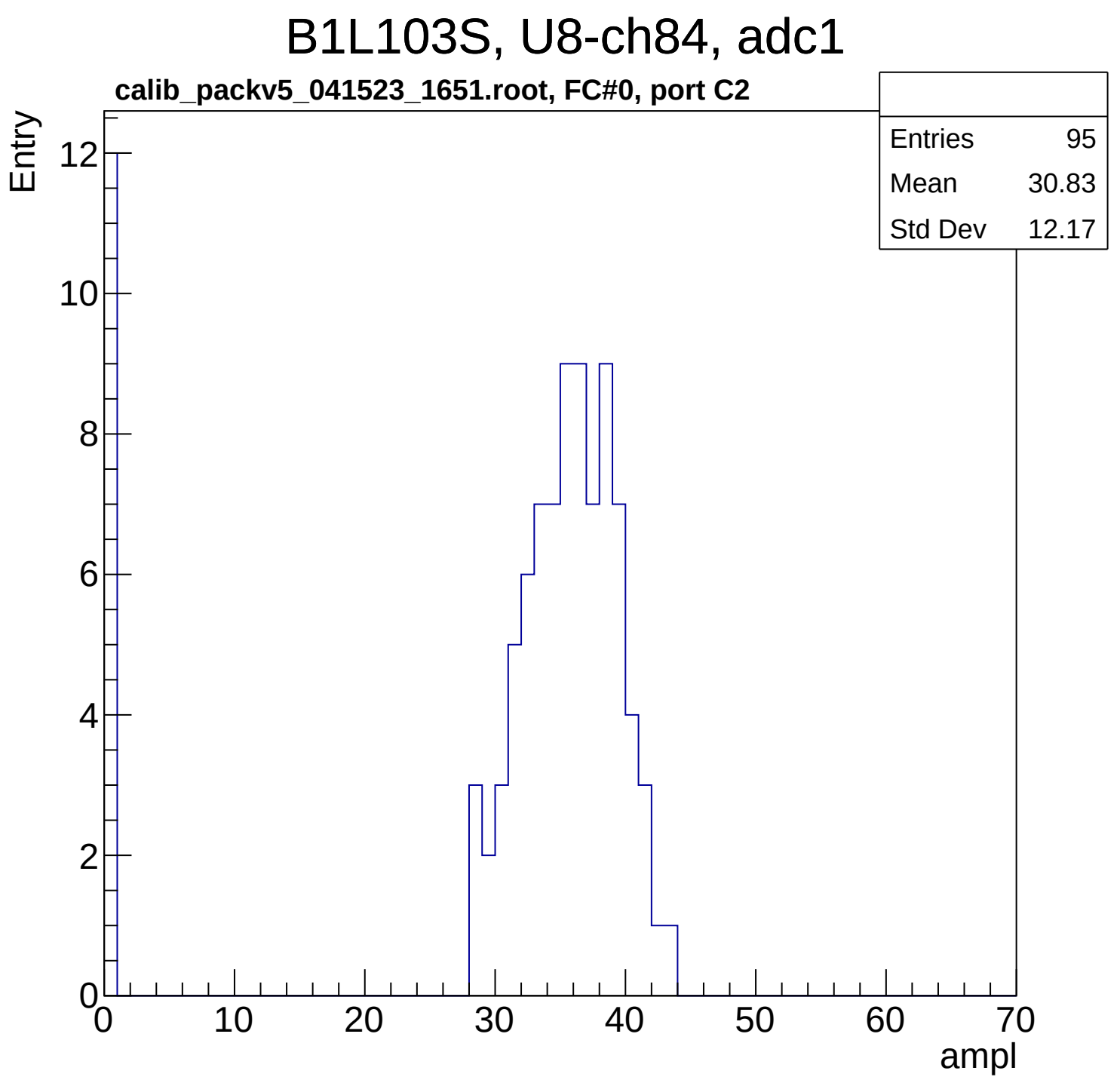
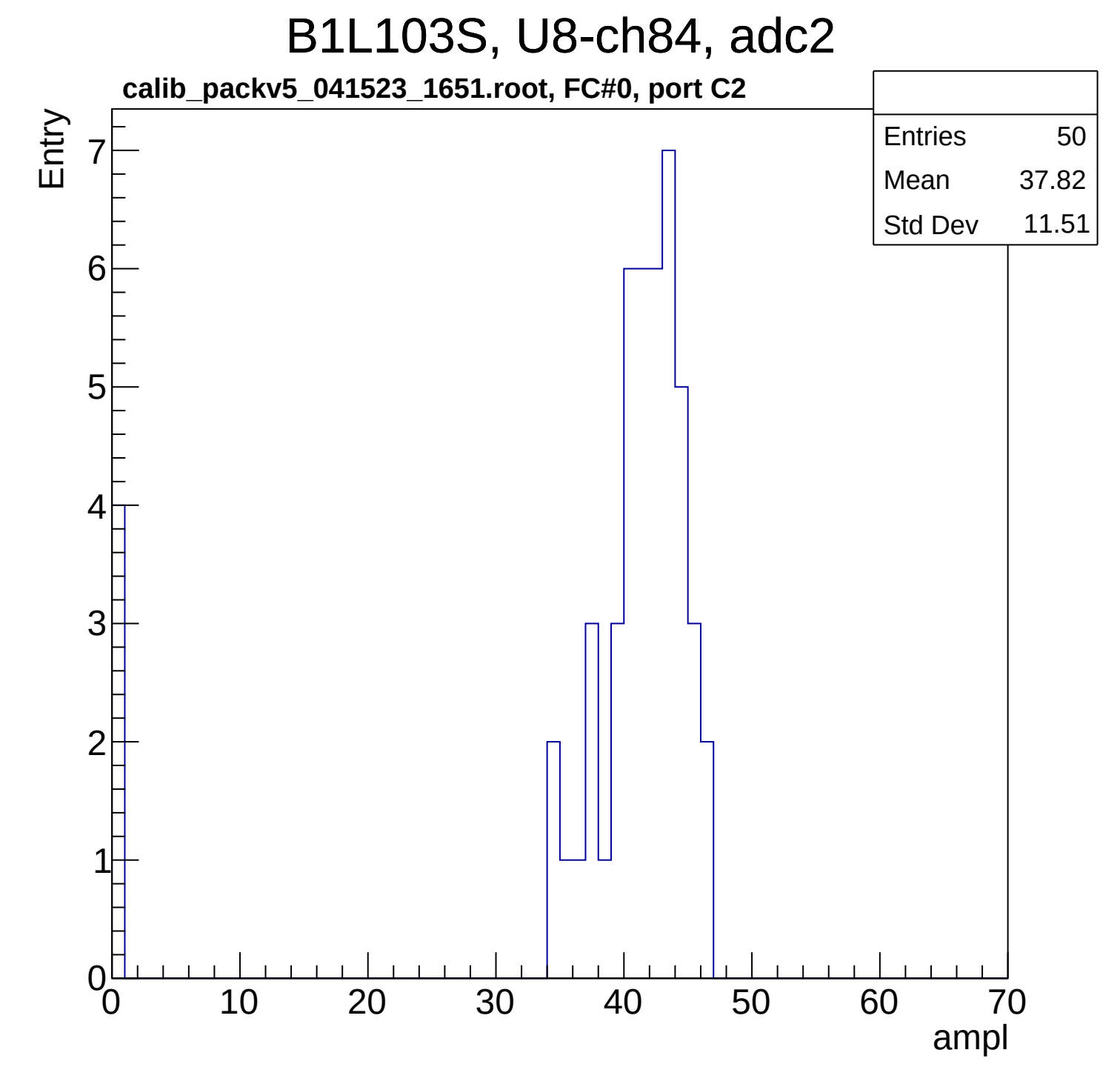
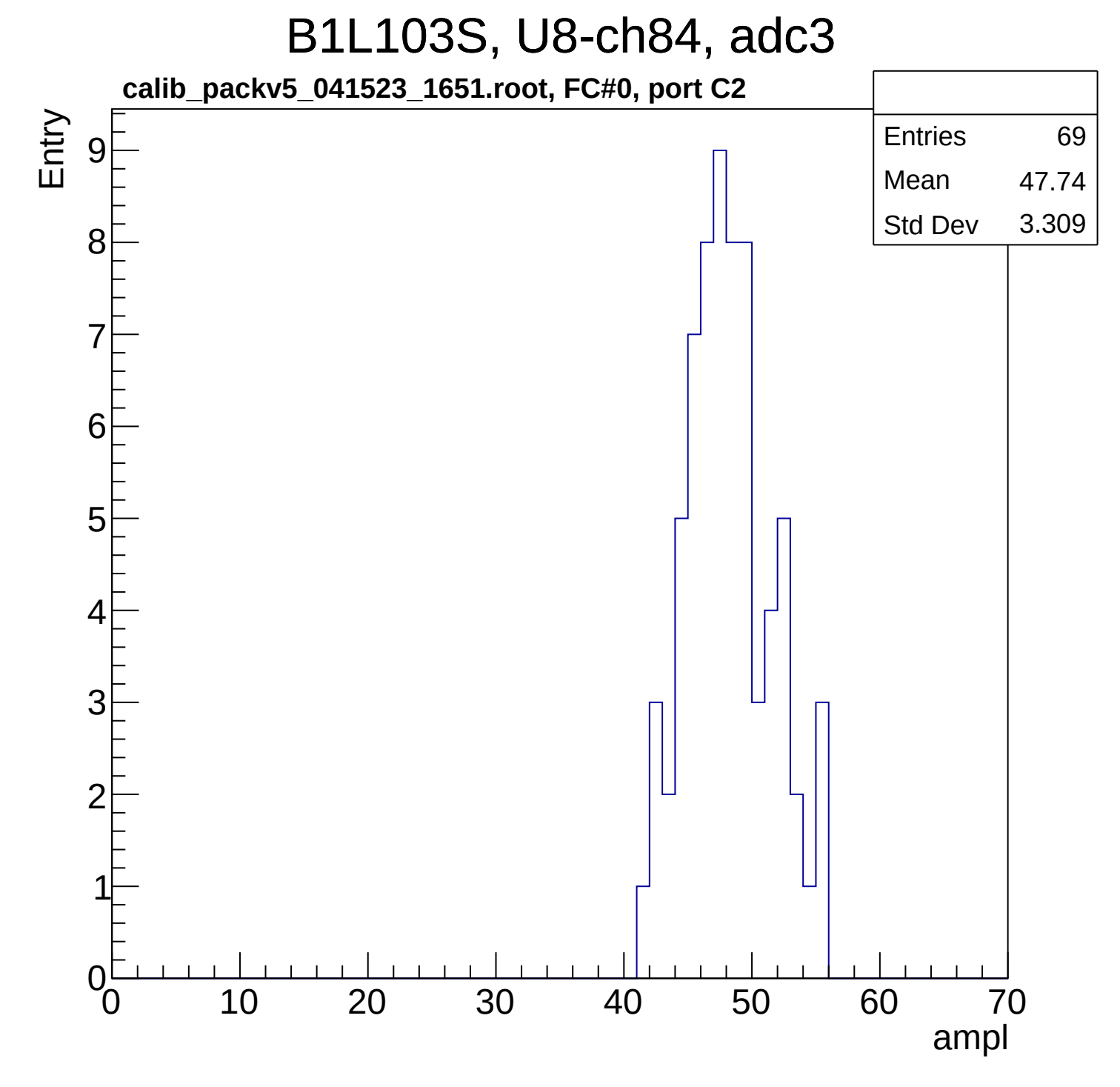

B1L103S, U8-ch83, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61.7
Std Dev 1.418
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U8-ch83, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch84, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 22.96
Std Dev 10.63
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch84, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 30.83
Std Dev 12.17
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch84, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 37.82
Std Dev 11.51
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U8-ch84, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 47.74
Std Dev 3.309
Entry
ampl
0
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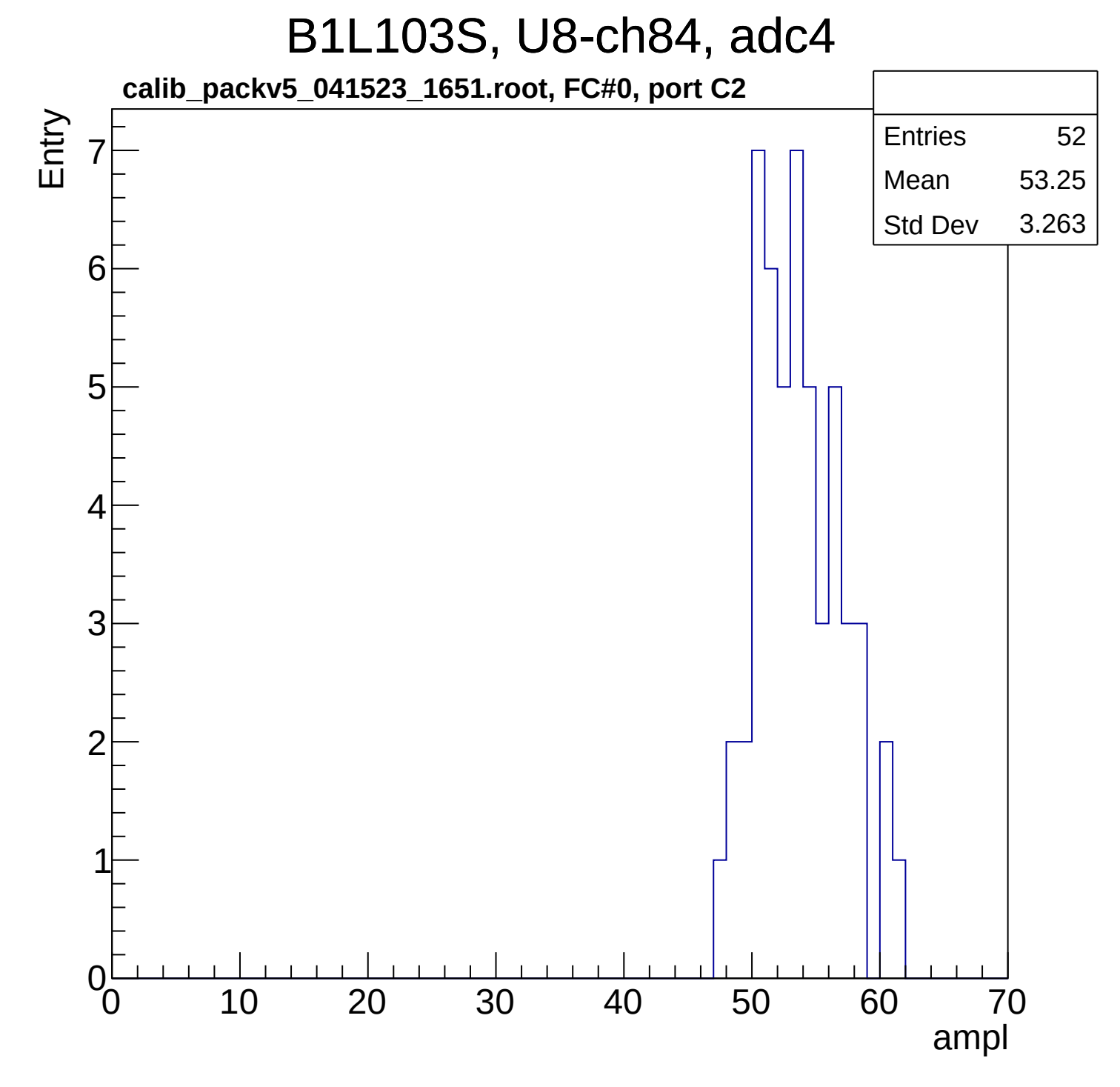
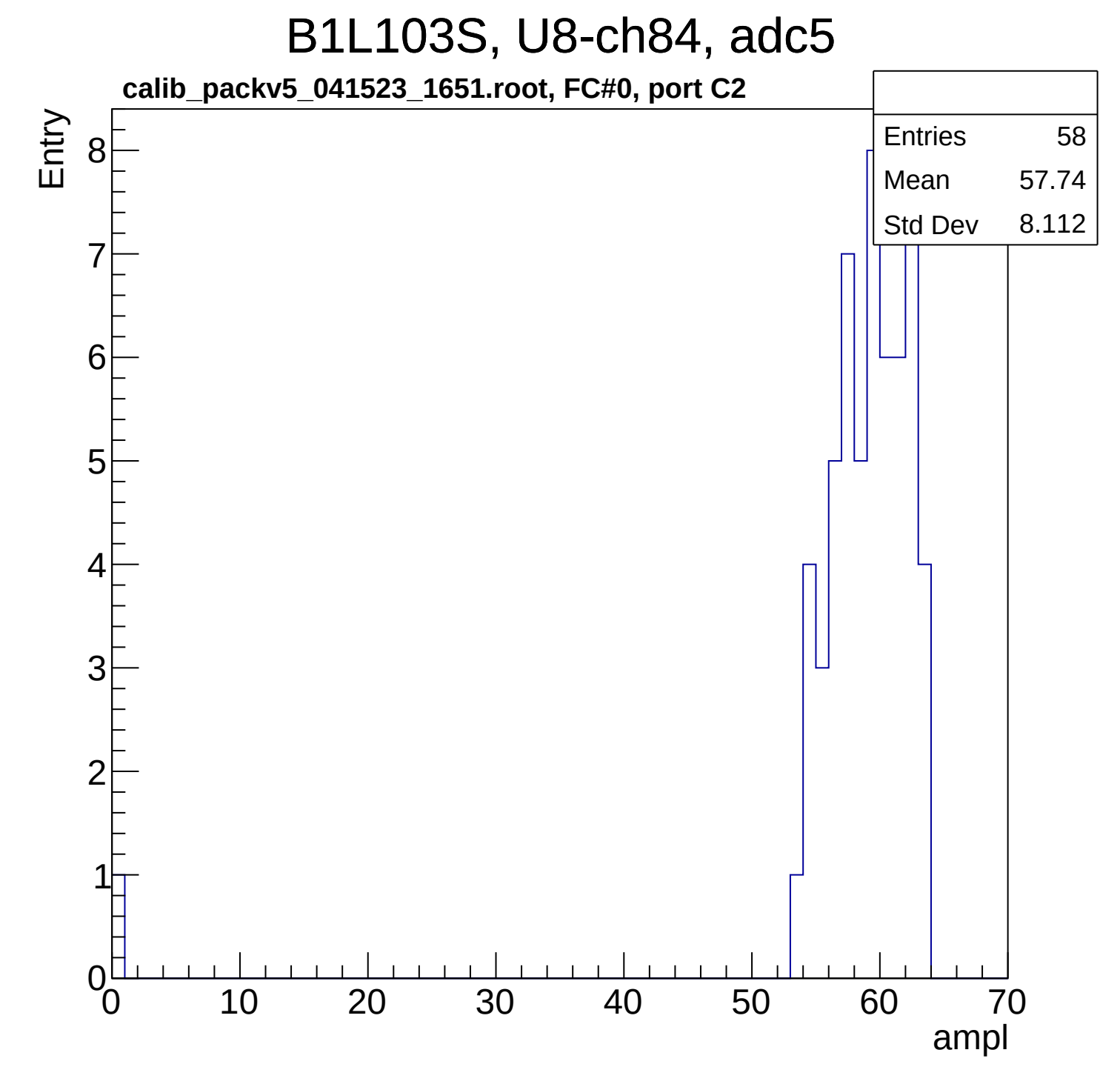
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U8-ch84, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 53.25
Std Dev 3.263
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U8-ch84, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 57.74
Std Dev 8.112
Entry
ampl
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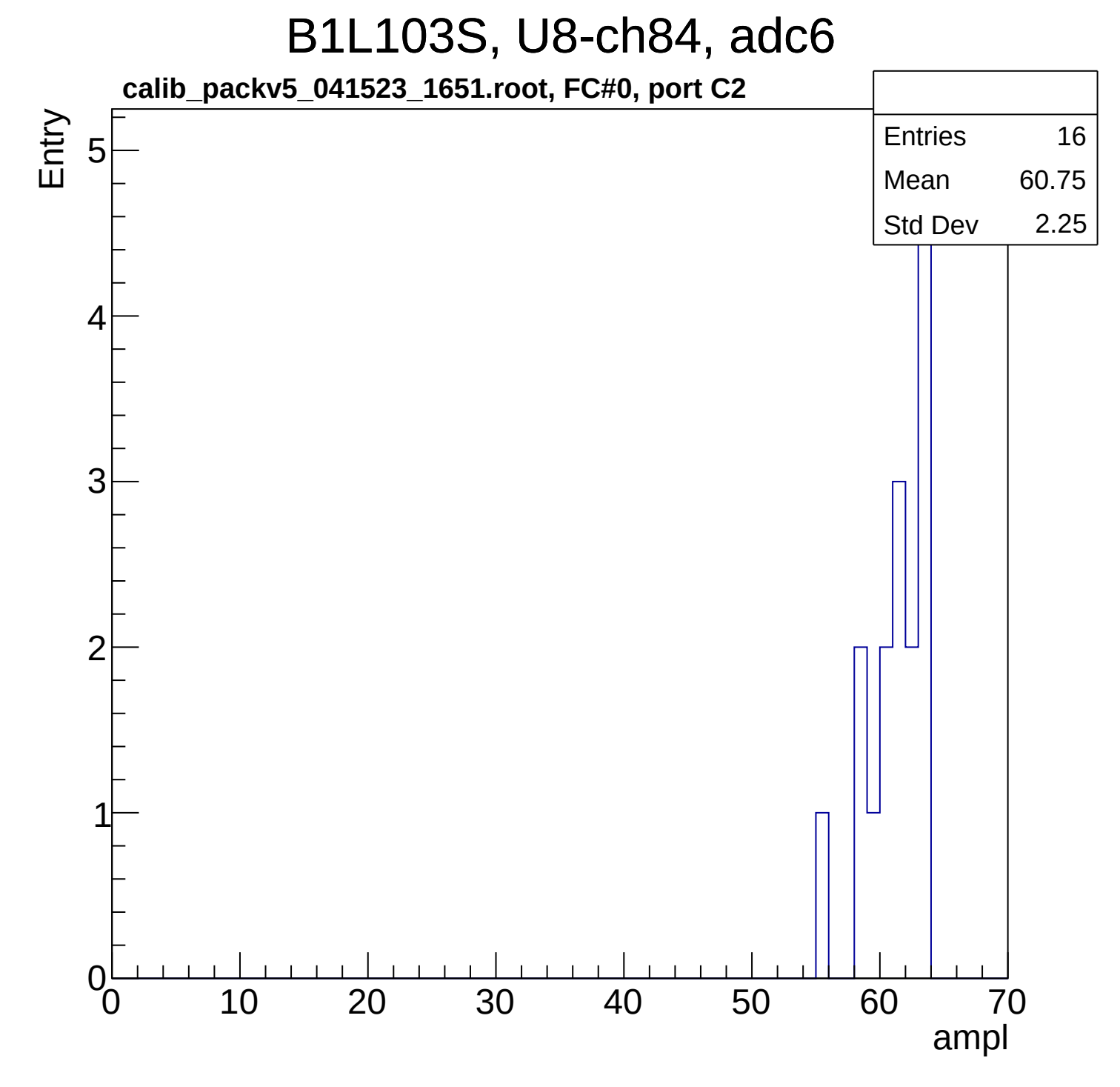
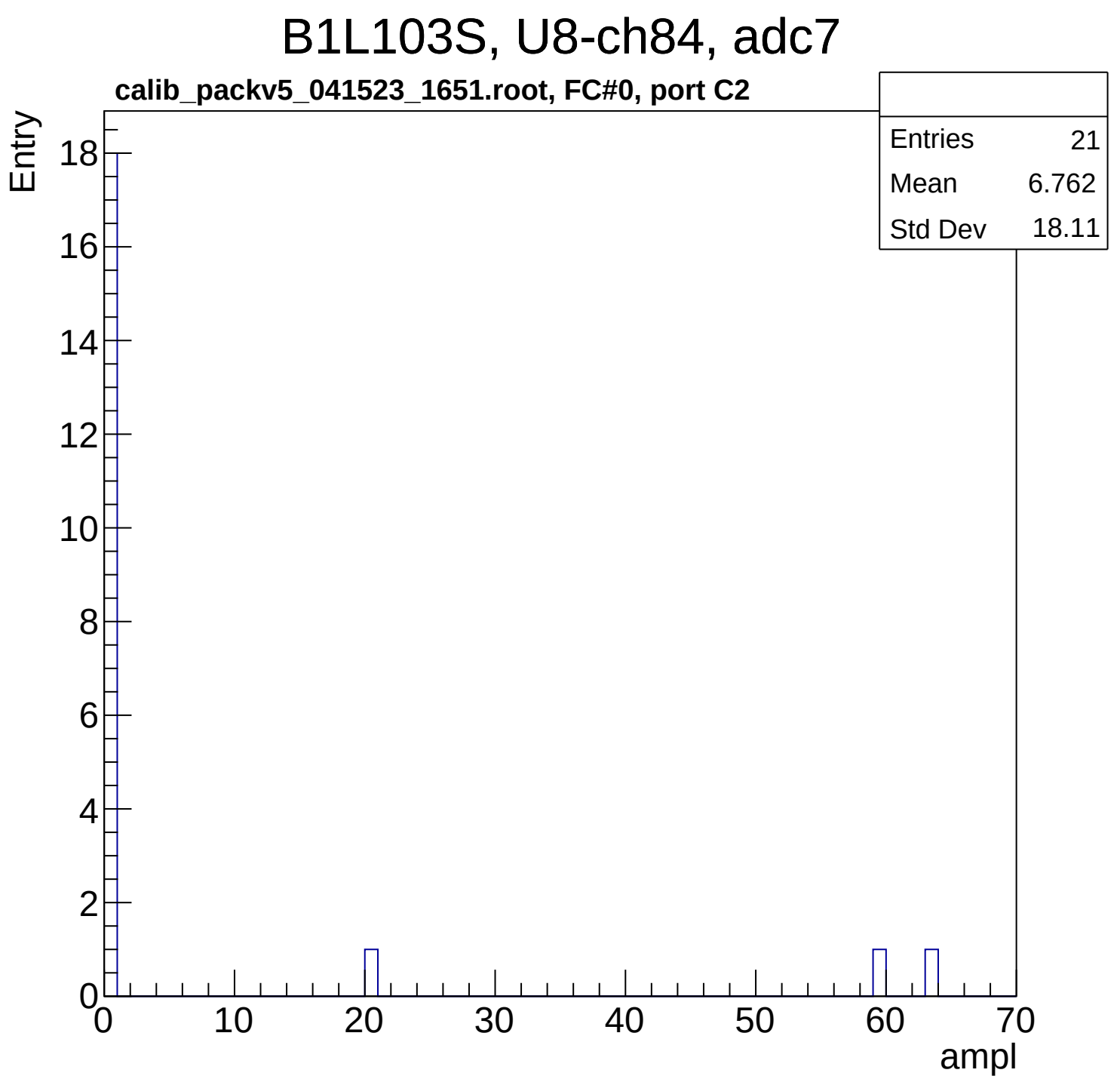
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch84, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 60.75
Std Dev 2.25
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch84, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 6.762
Std Dev 18.11
Entry
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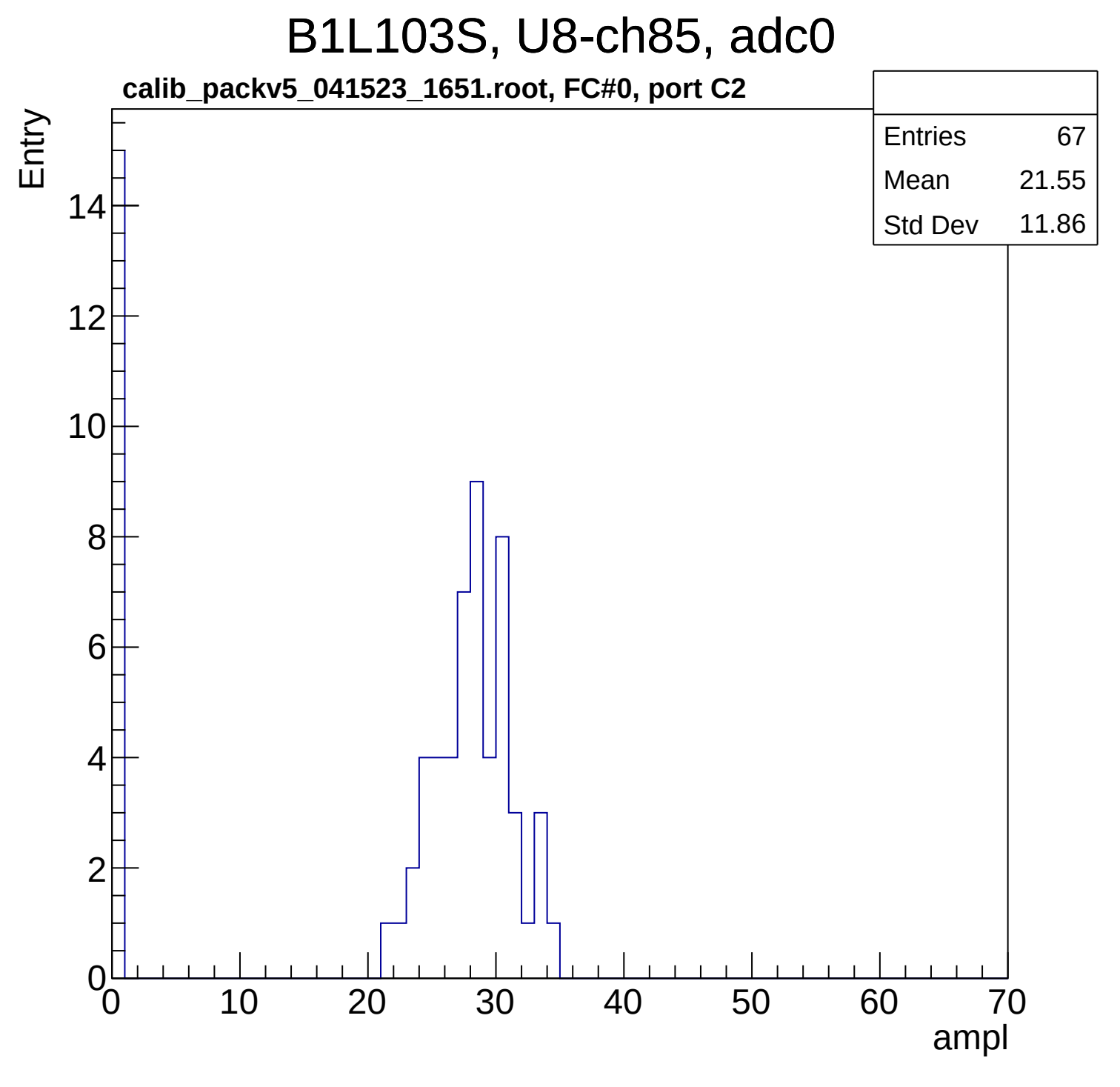
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch85, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 21.55
Std Dev 11.86
Entry
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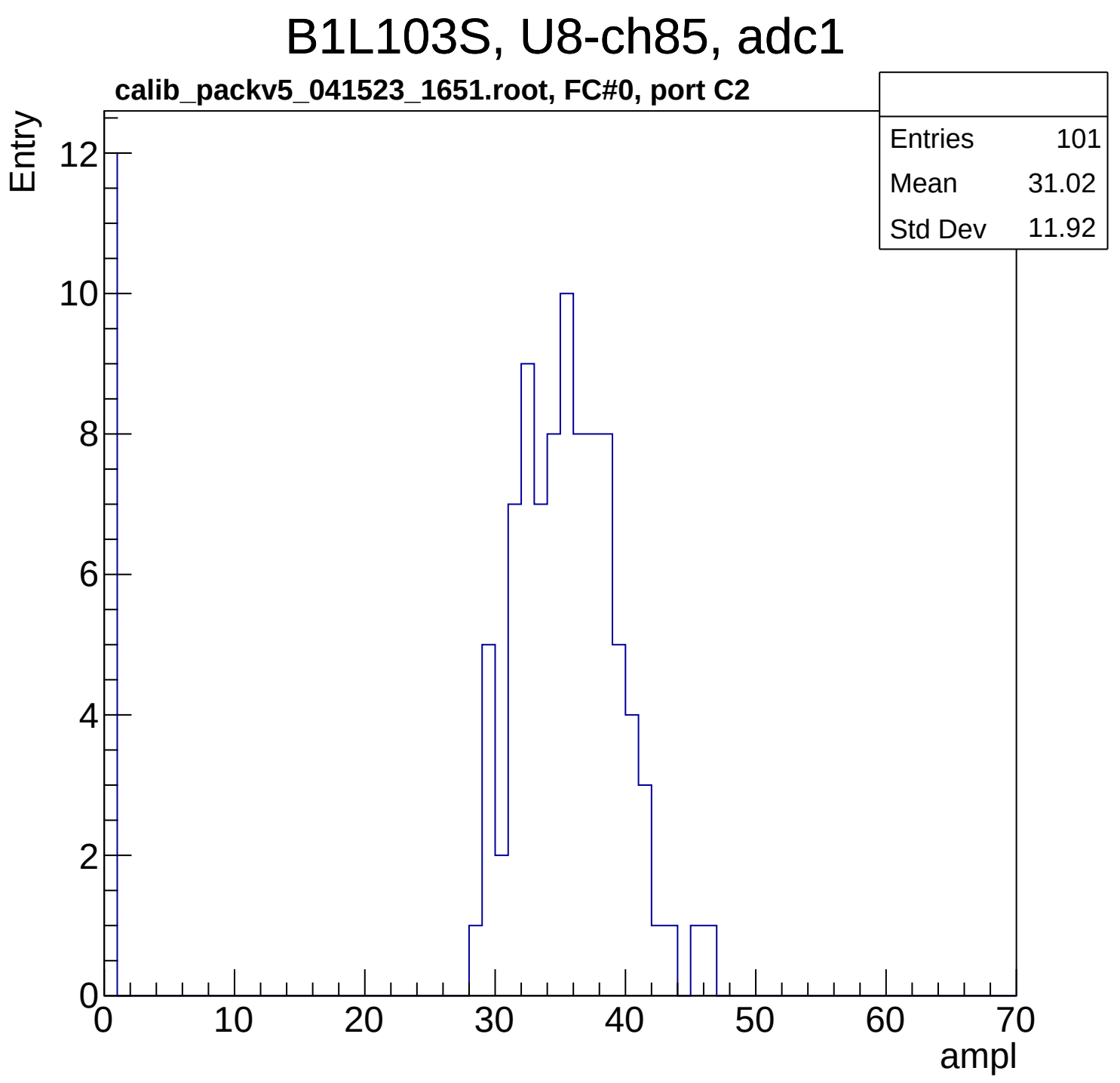
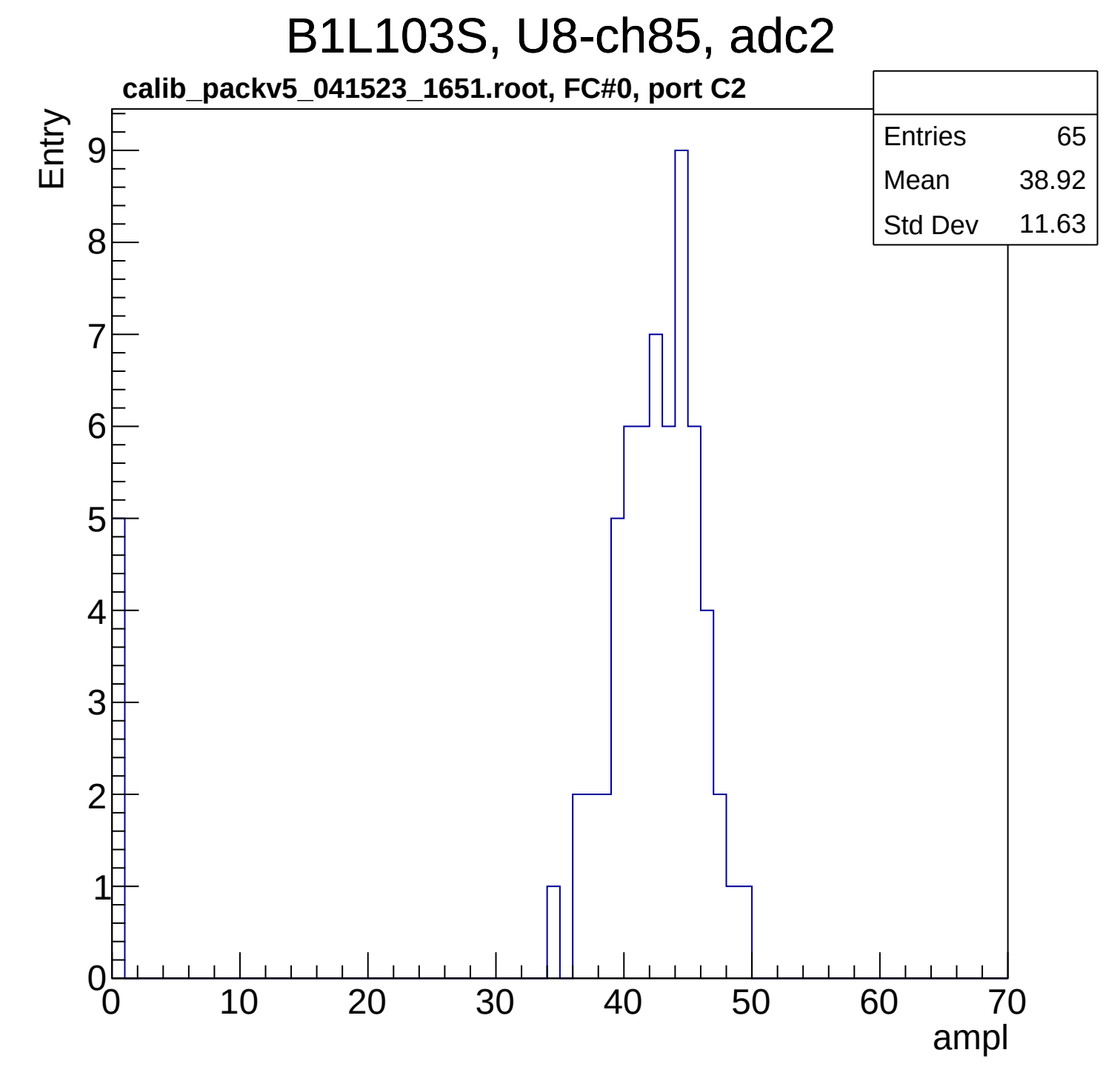
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch85, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 101
Mean 31.02
Std Dev 11.92
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch85, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 38.92
Std Dev 11.63
Entry
ampl
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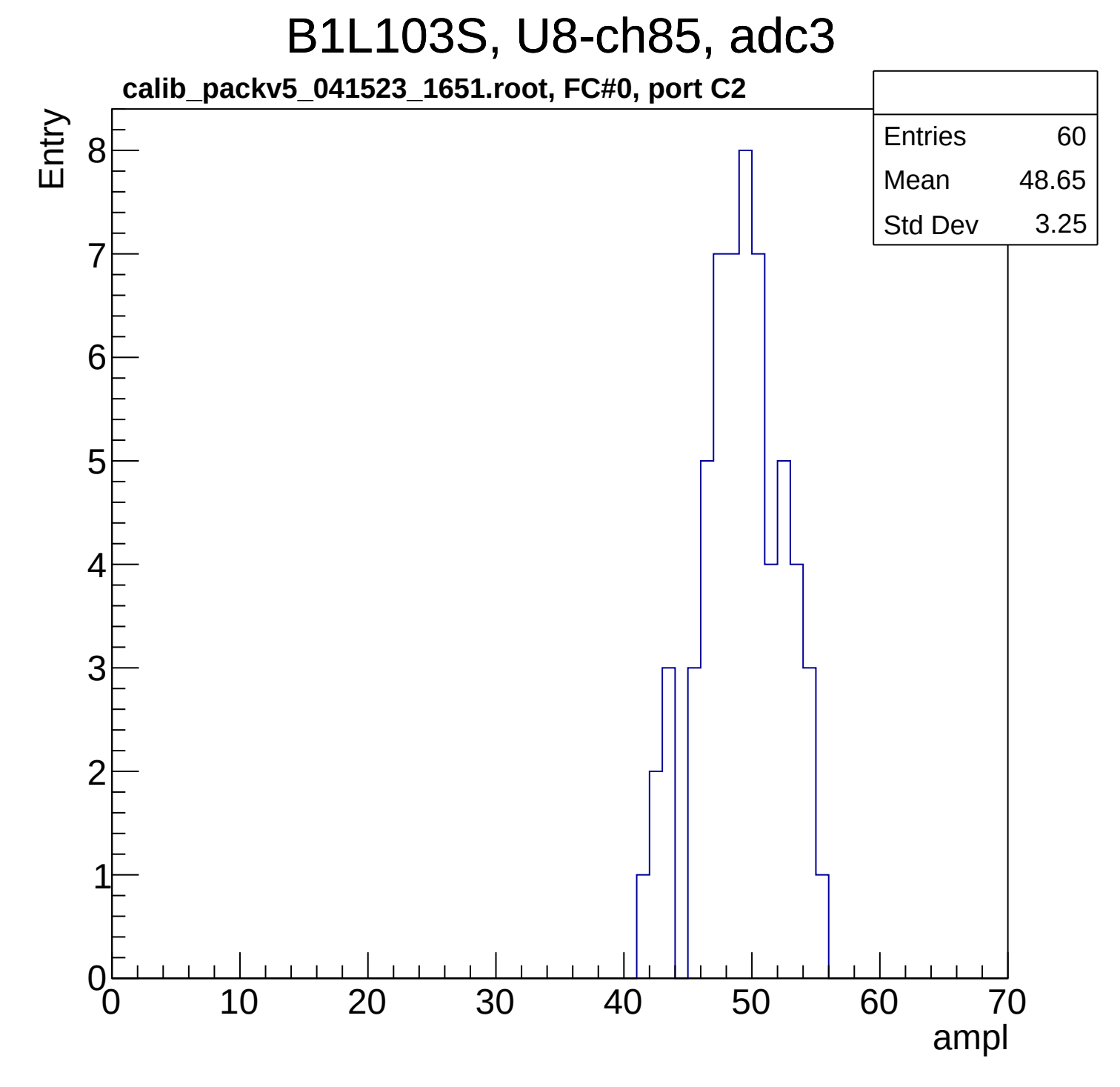
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U8-ch85, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 48.65
Std Dev 3.25
Entry
ampl
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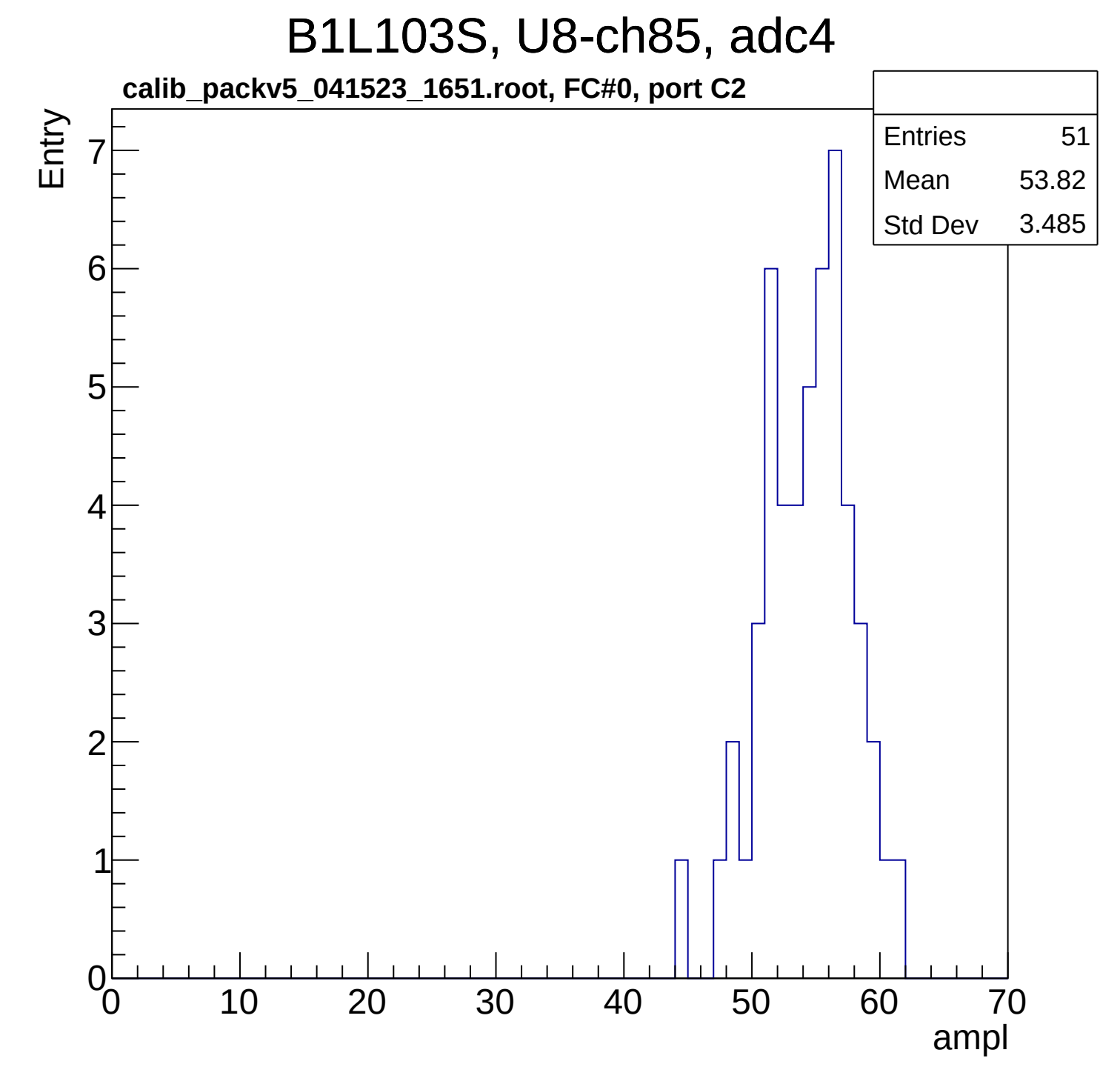
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch85, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 53.82
Std Dev 3.485
Entry
ampl
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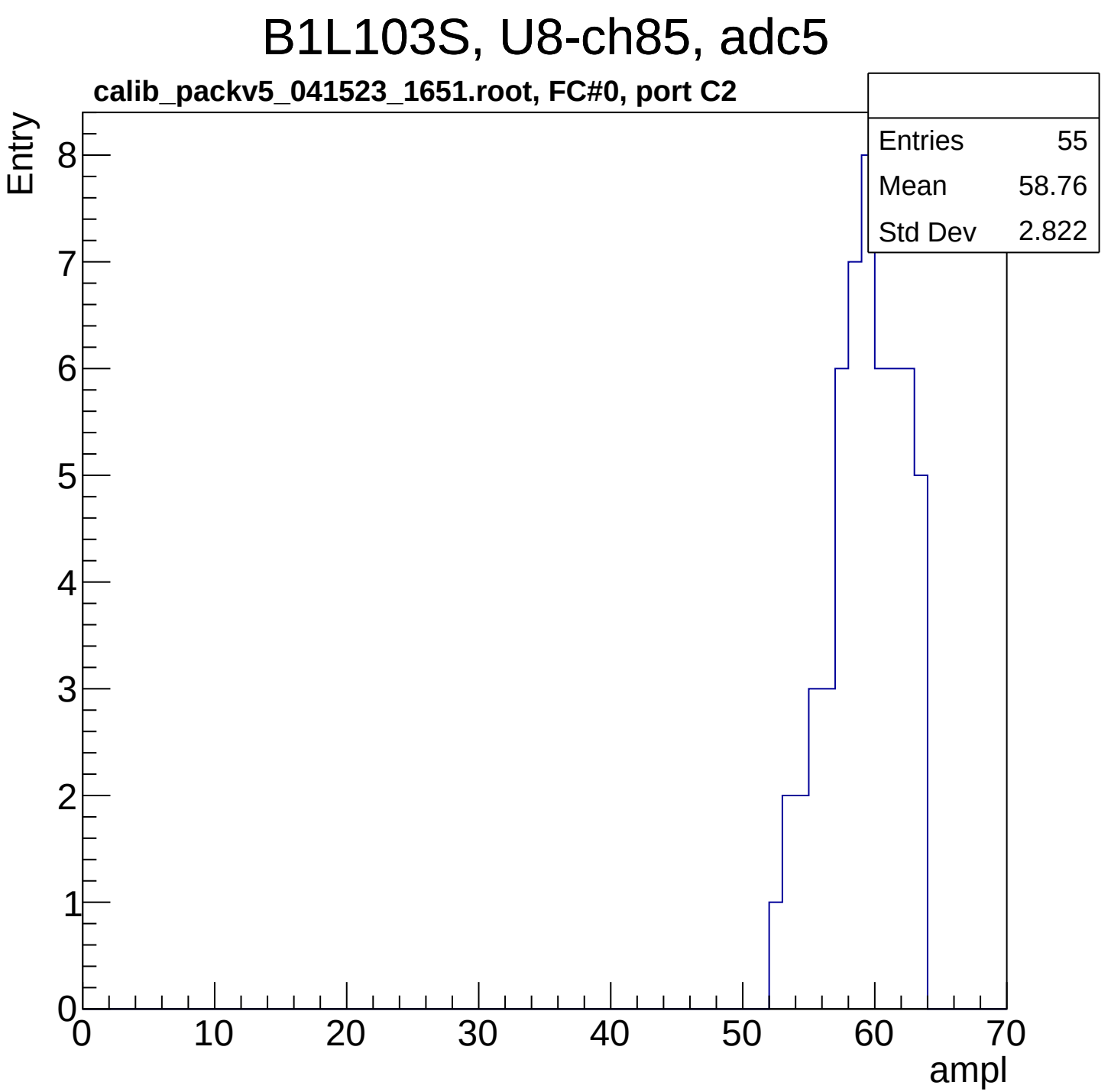
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U8-ch85, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 58.76
Std Dev 2.822
Entry
ampl
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2
3
4
5
6
7
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0
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20
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40
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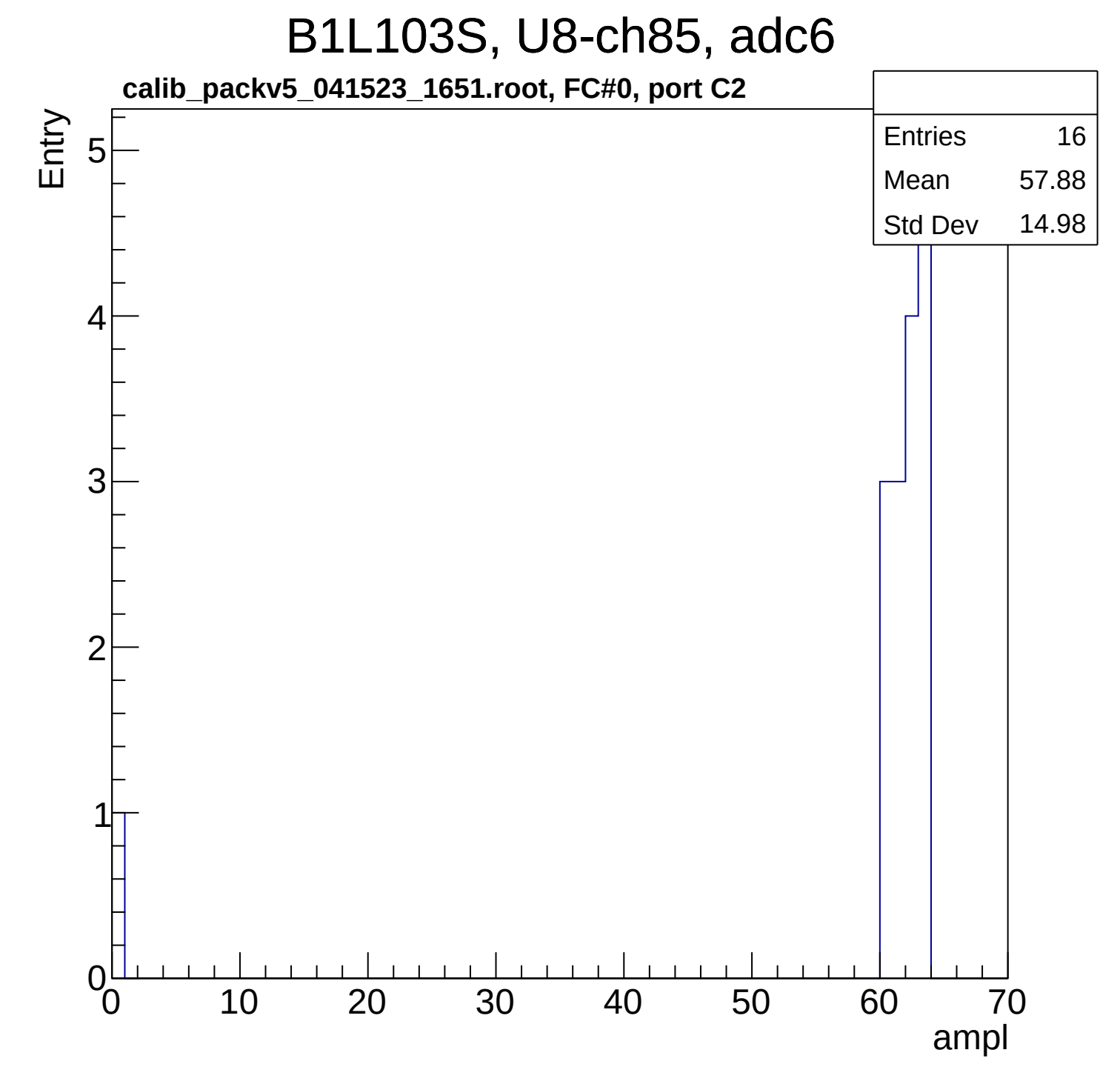
60
70


B1L103S, U8-ch85, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 57.88
Std Dev 14.98
Entry
ampl
0
1
2
3
4
5
0
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20
30
40
50
60
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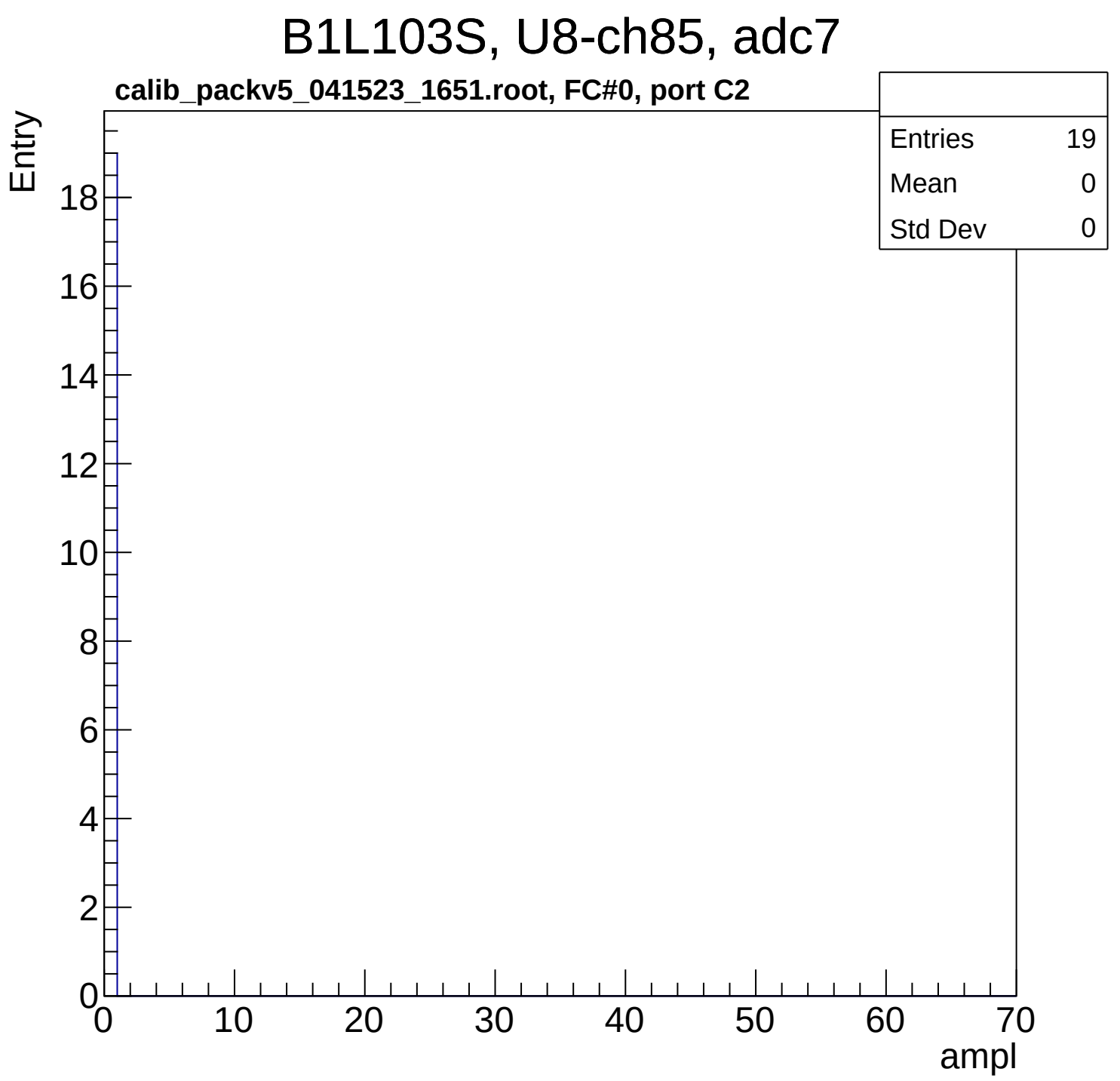
B1L103S, U8-ch85, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
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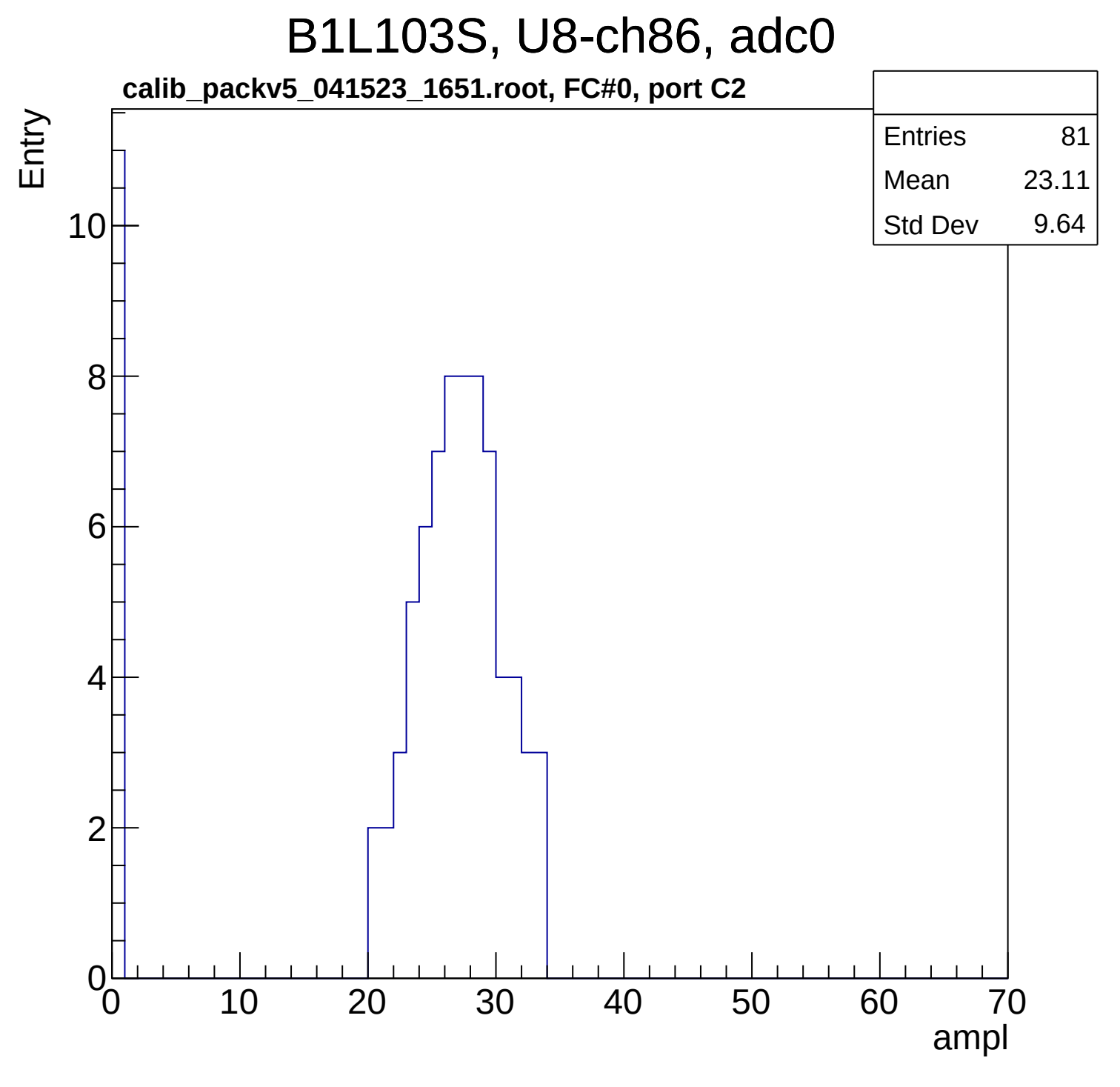
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch86, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 23.11
Std Dev 9.64
Entry
ampl
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4
6
8
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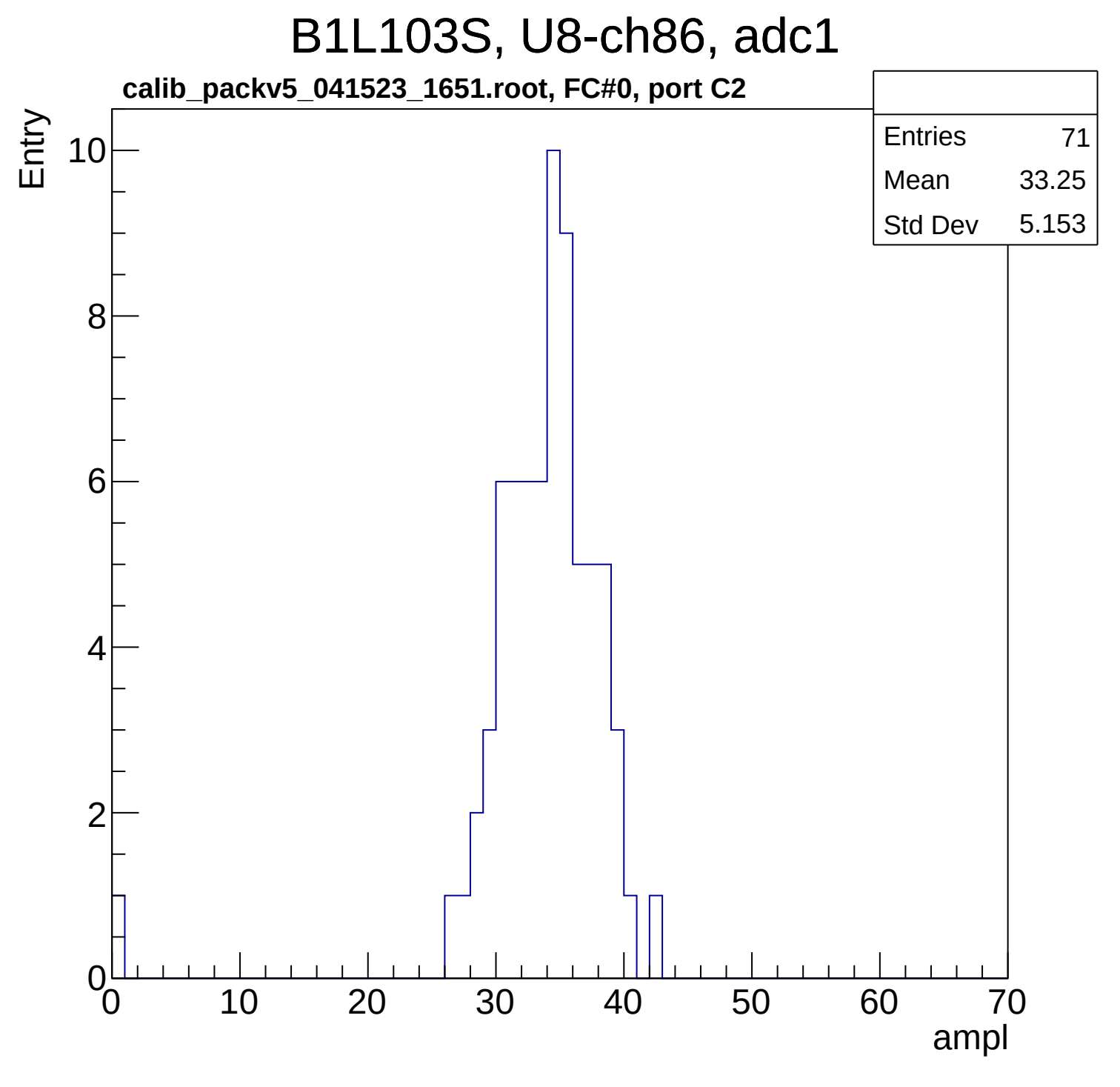
0
10
20
30
40
50
60
70


B1L103S, U8-ch86, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 33.25
Std Dev 5.153
Entry
ampl
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4
6
8
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0
10
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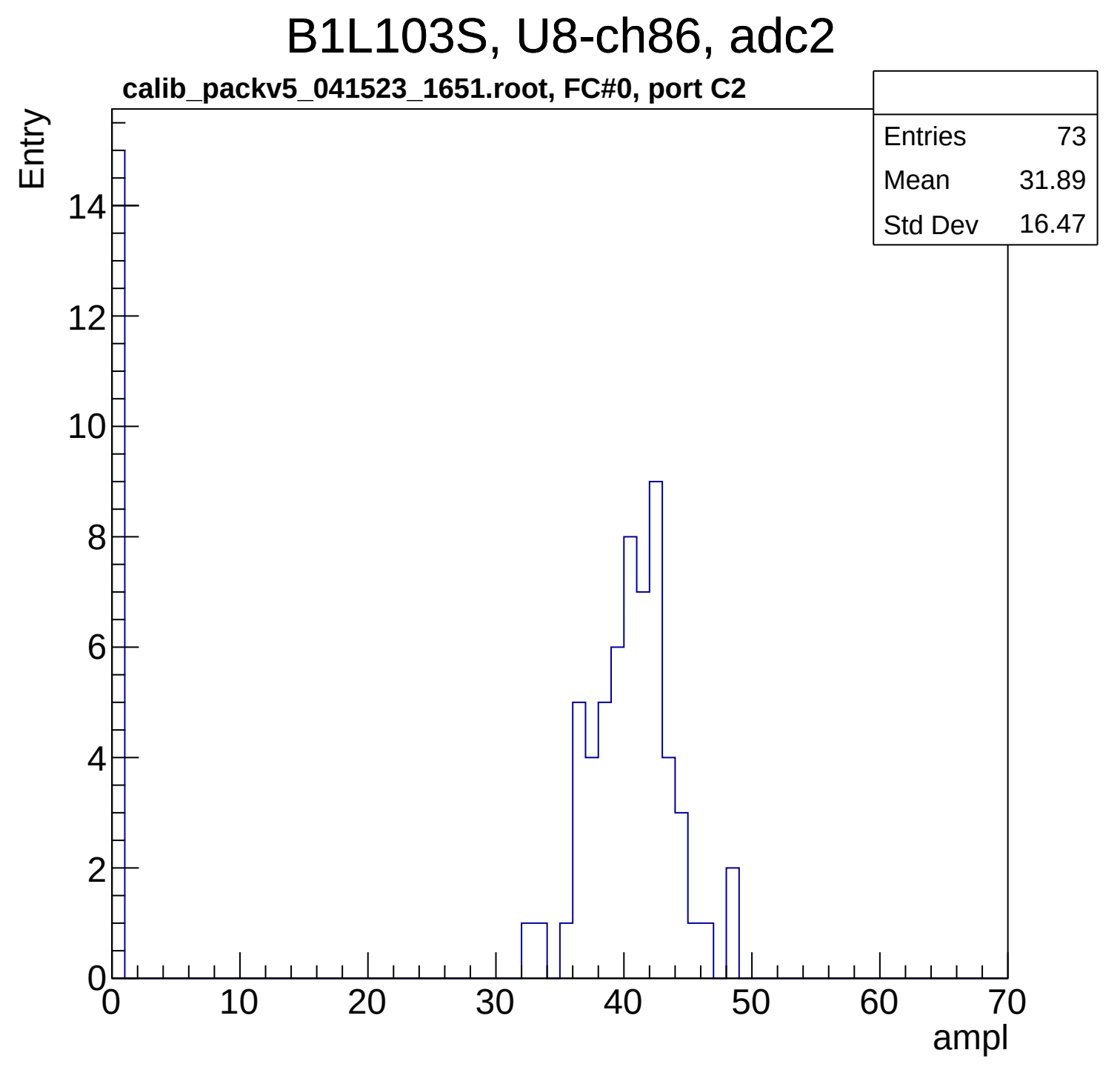
40
50
60
70


B1L103S, U8-ch86, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 31.89
Std Dev 16.47
Entry
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2
4
6
8
10
12
14
0
10
20
30
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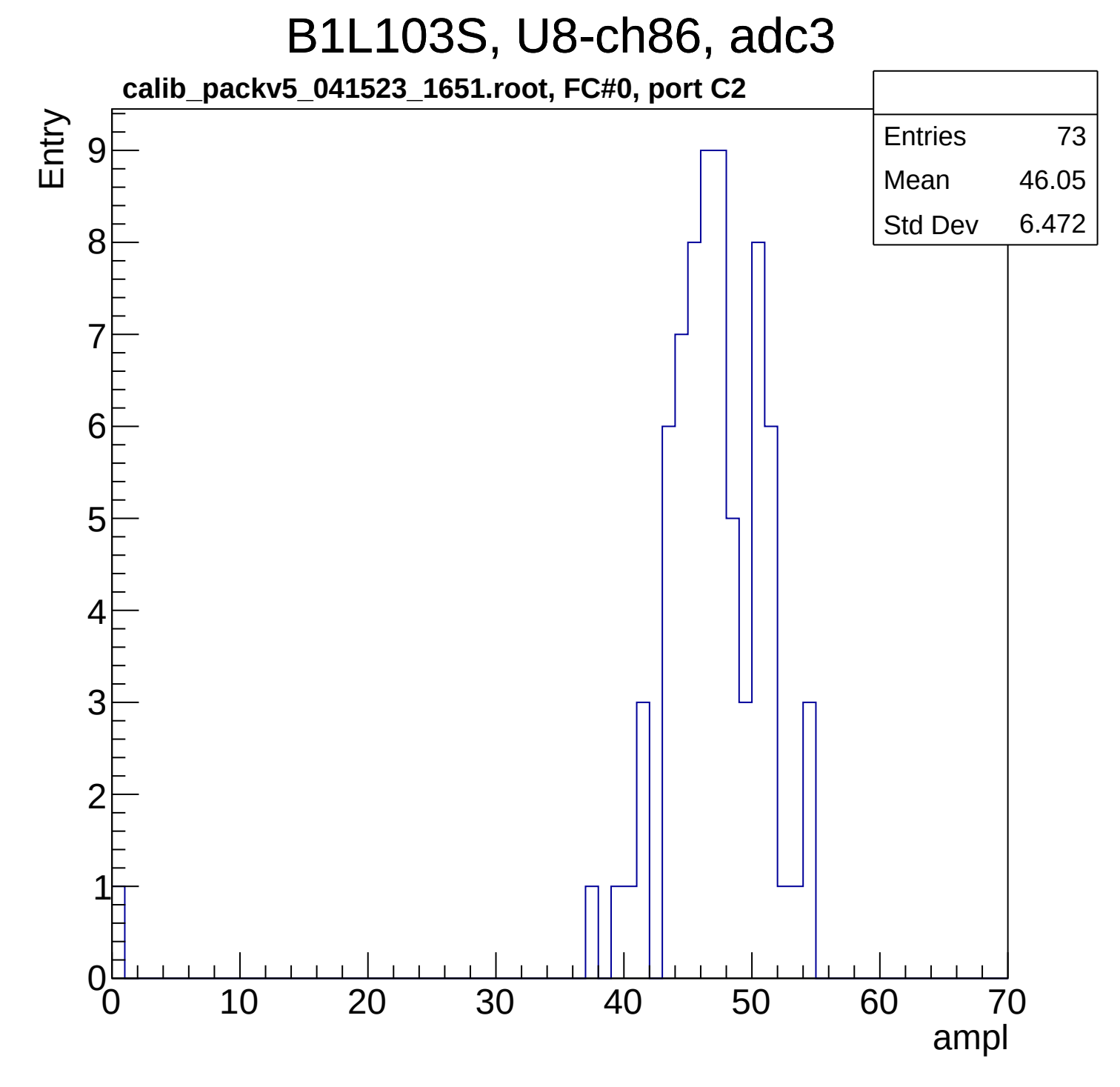
50
60
70
ampl


B1L103S, U8-ch86, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 46.05
Std Dev 6.472
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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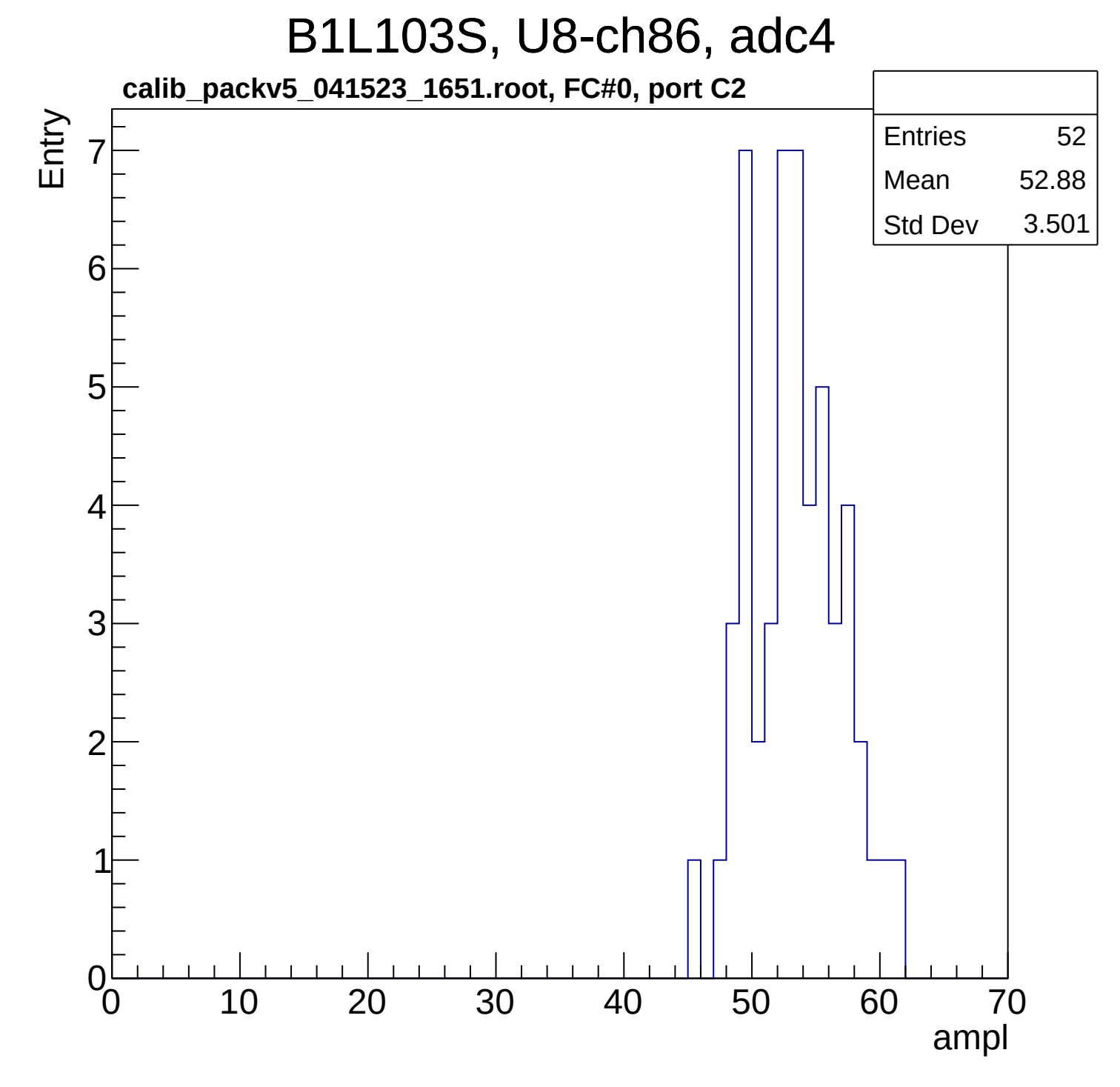
60
70


B1L103S, U8-ch86, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 52.88
Std Dev 3.501
Entry
ampl
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2
3
4
5
6
7
0
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60
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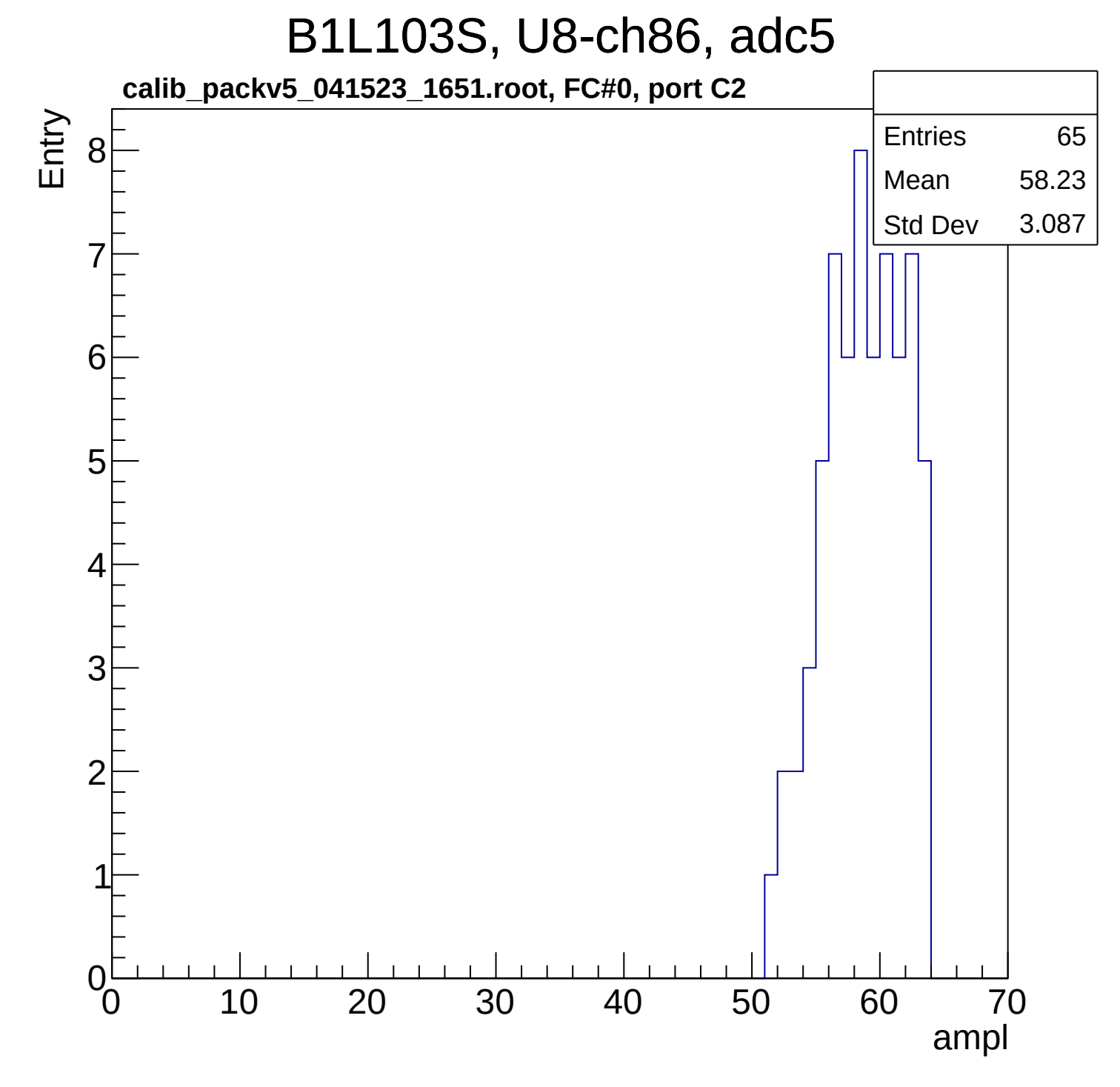
B1L103S, U8-ch86, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 58.23
Std Dev 3.087
Entry
ampl
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2
3
4
5
6
7
8
0
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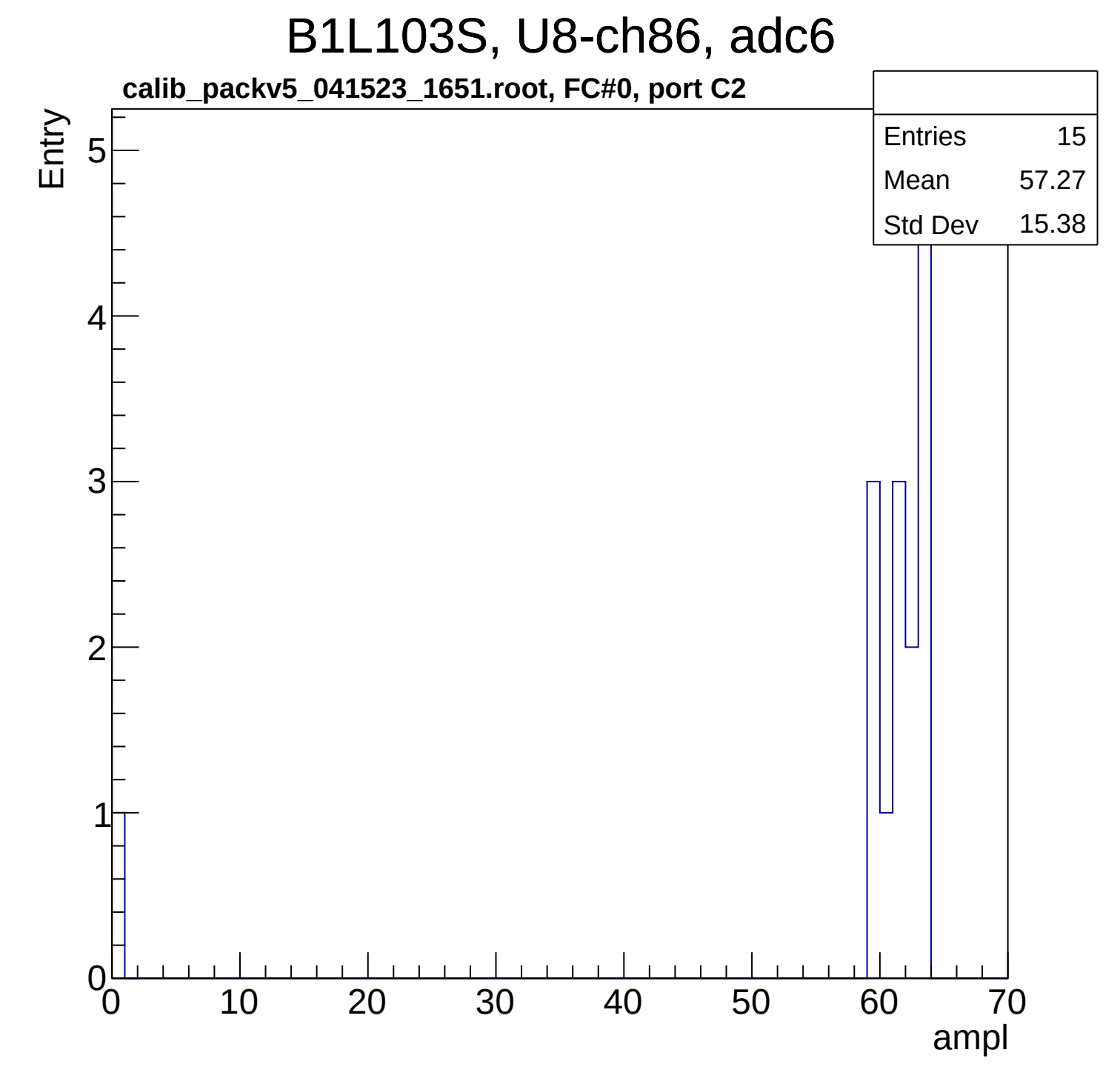
60
70


B1L103S, U8-ch86, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 57.27
Std Dev 15.38
Entry
ampl
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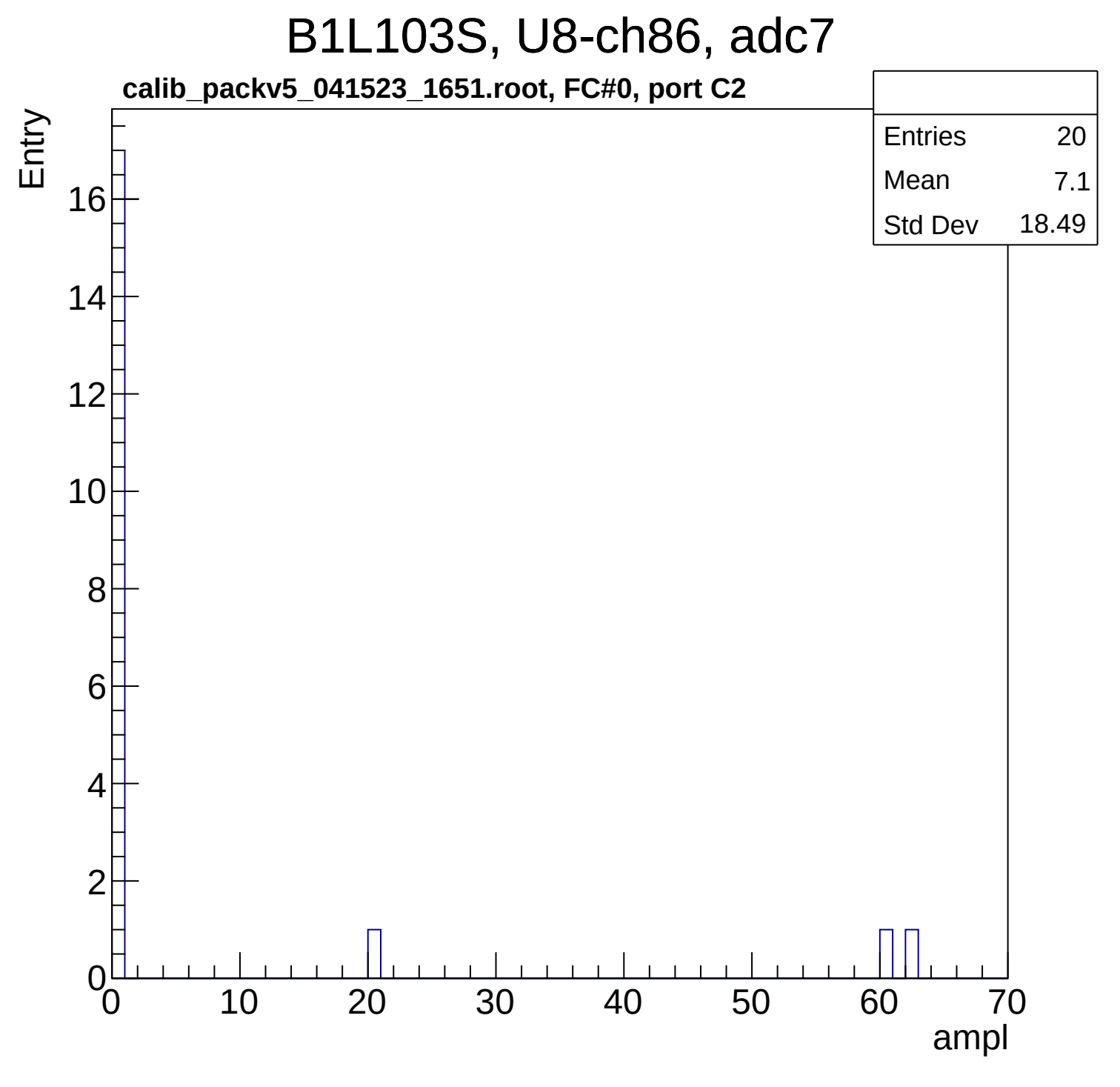
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U8-ch86, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 7.1
Std Dev 18.49
Entry
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4
6
8
10
12
14
16
0
10
20
30
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50
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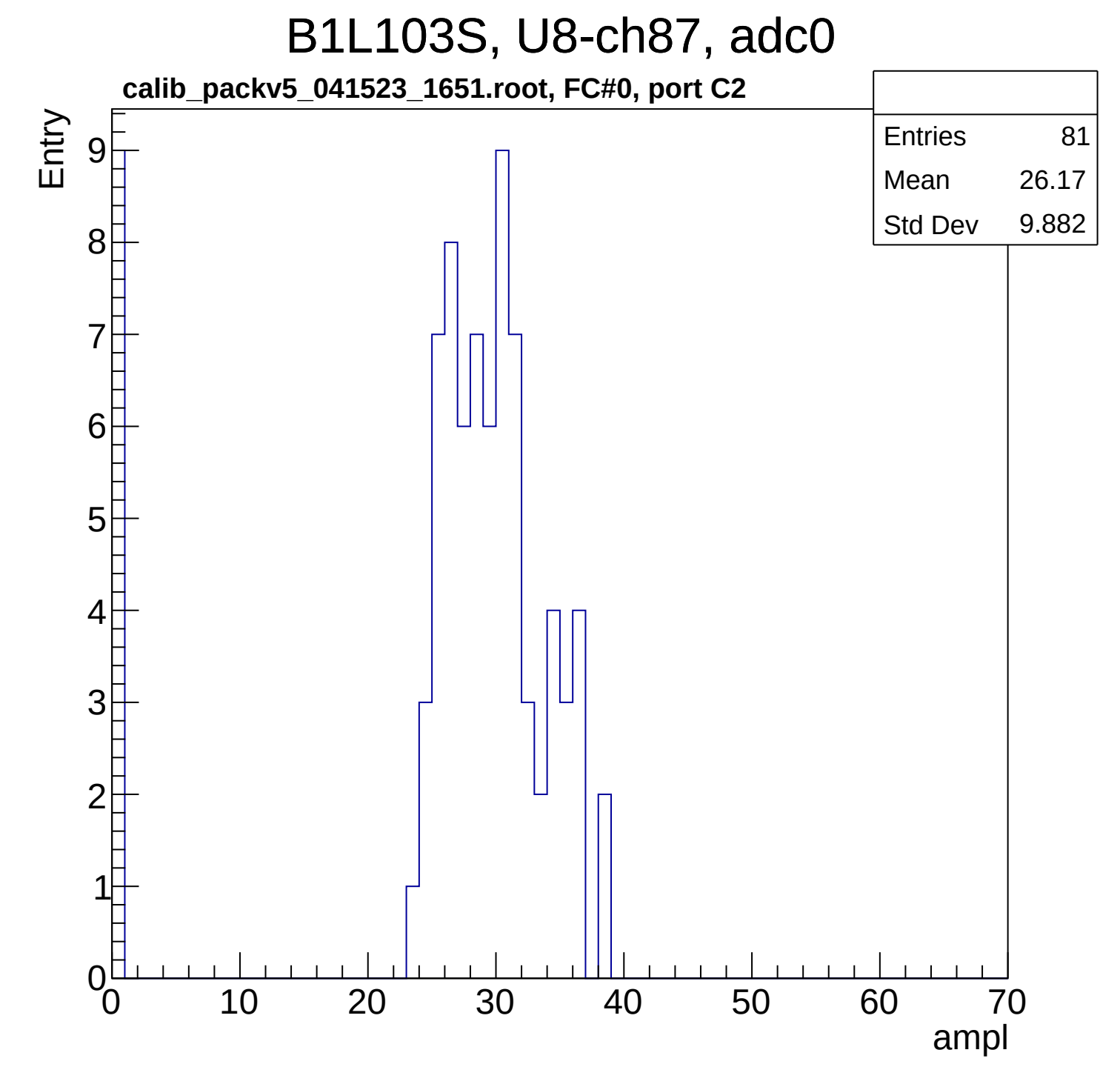
70
ampl


B1L103S, U8-ch87, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 26.17
Std Dev 9.882
Entry
ampl
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2
3
4
5
6
7
8
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0
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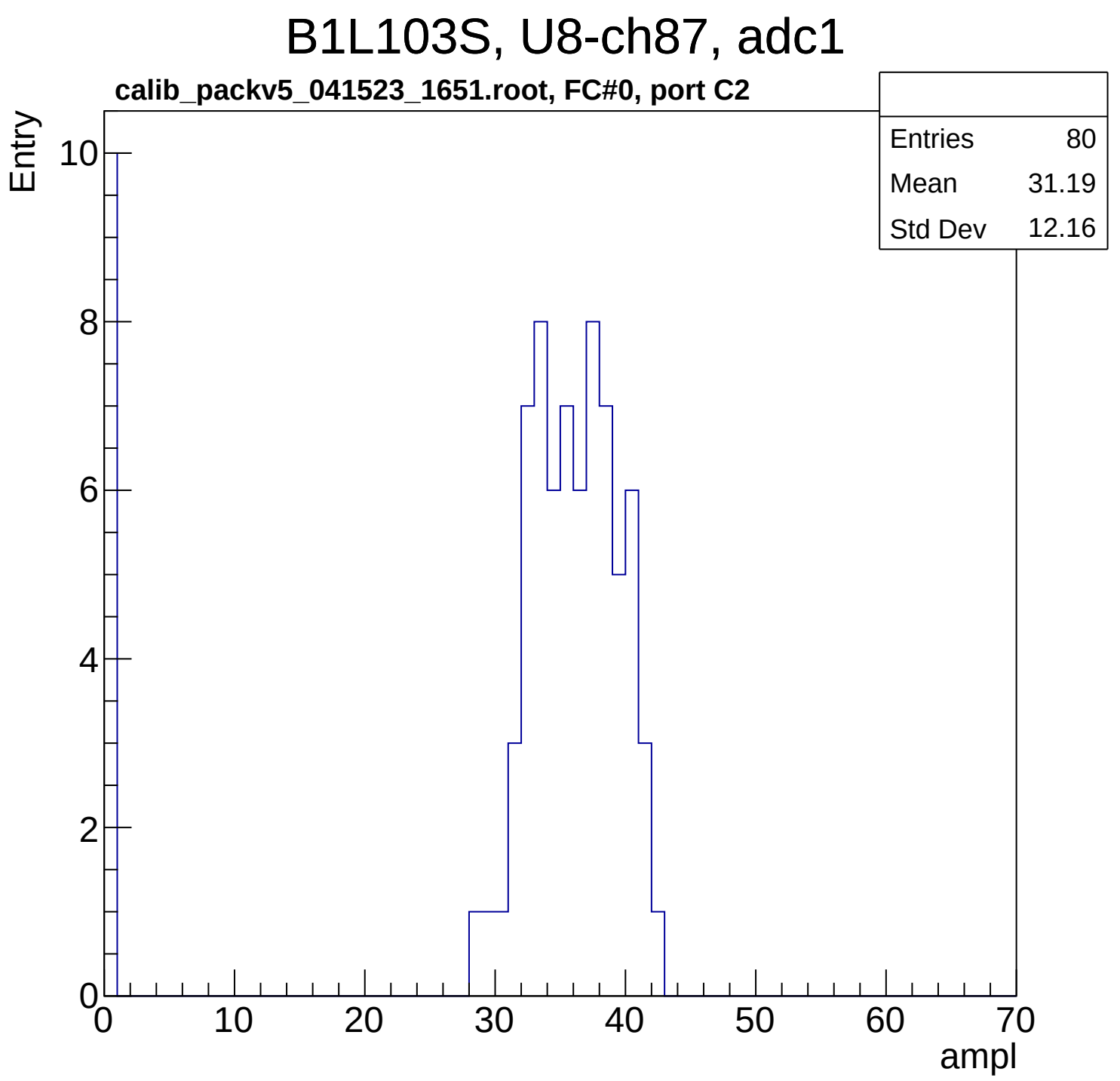
B1L103S, U8-ch87, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 31.19
Std Dev 12.16
Entry
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2
4
6
8
10
0
10
20
30
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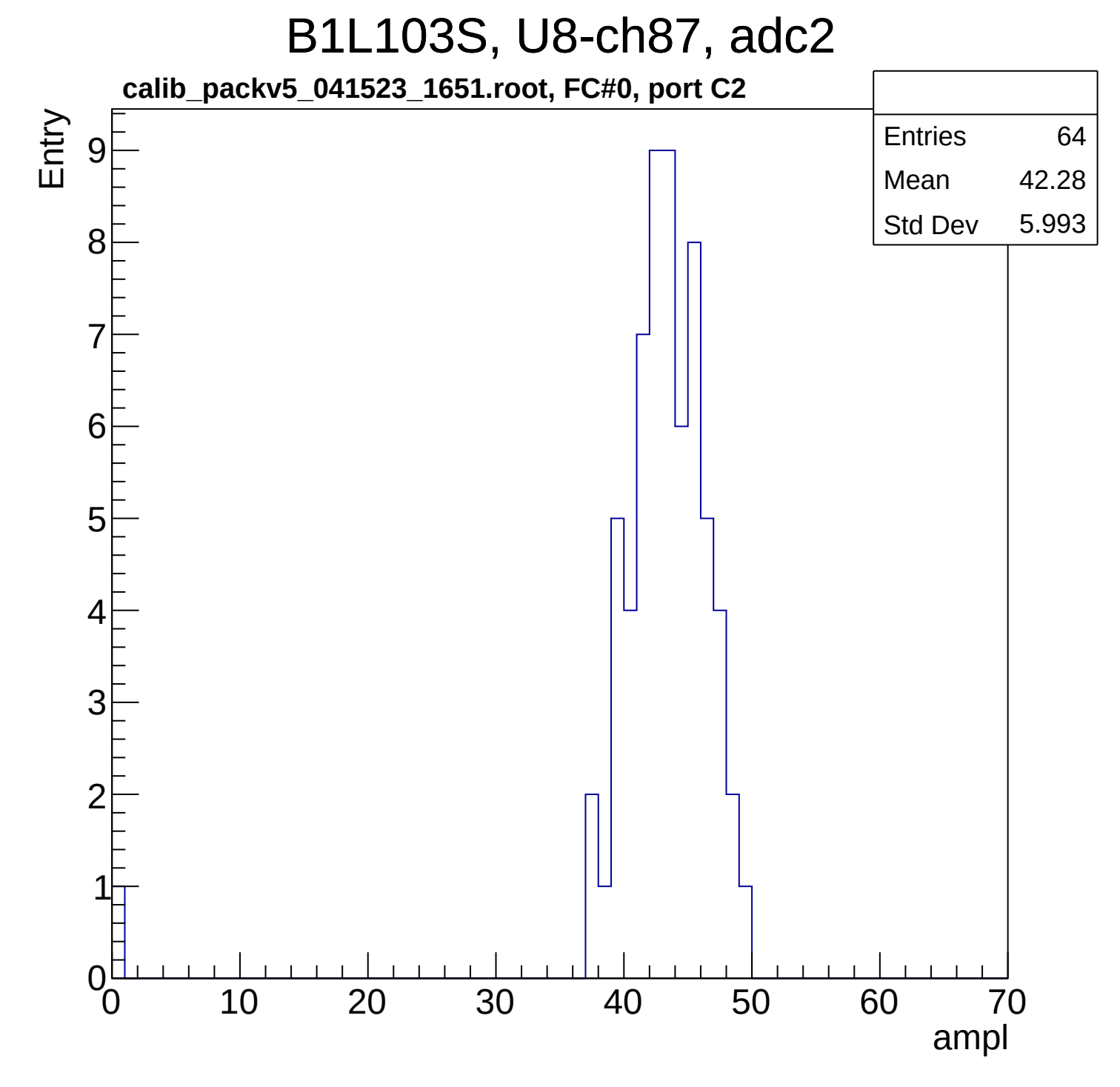
50
60
70
ampl


B1L103S, U8-ch87, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 42.28
Std Dev 5.993
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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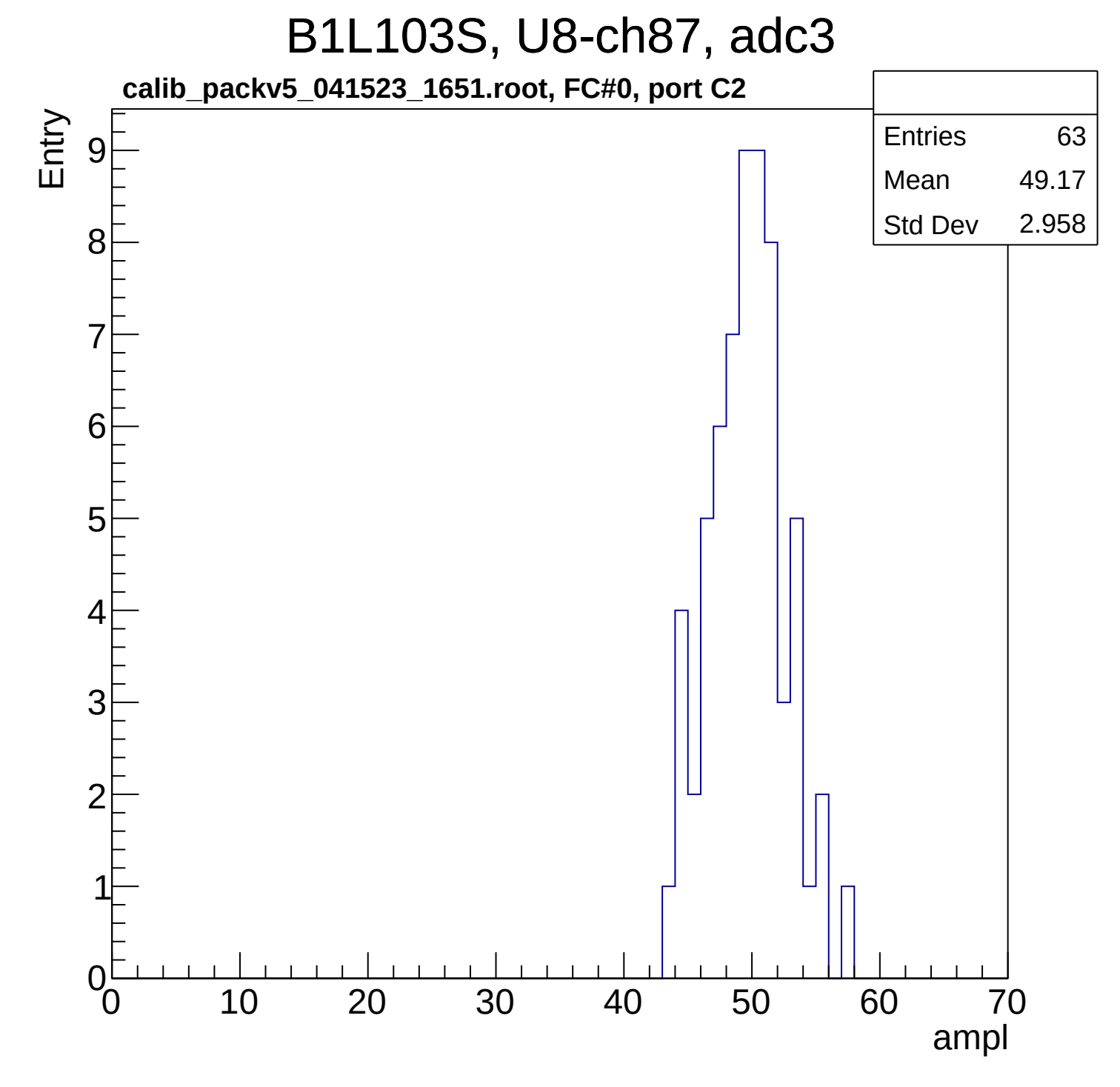
40
50
60
70


B1L103S, U8-ch87, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 49.17
Std Dev 2.958
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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40
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60
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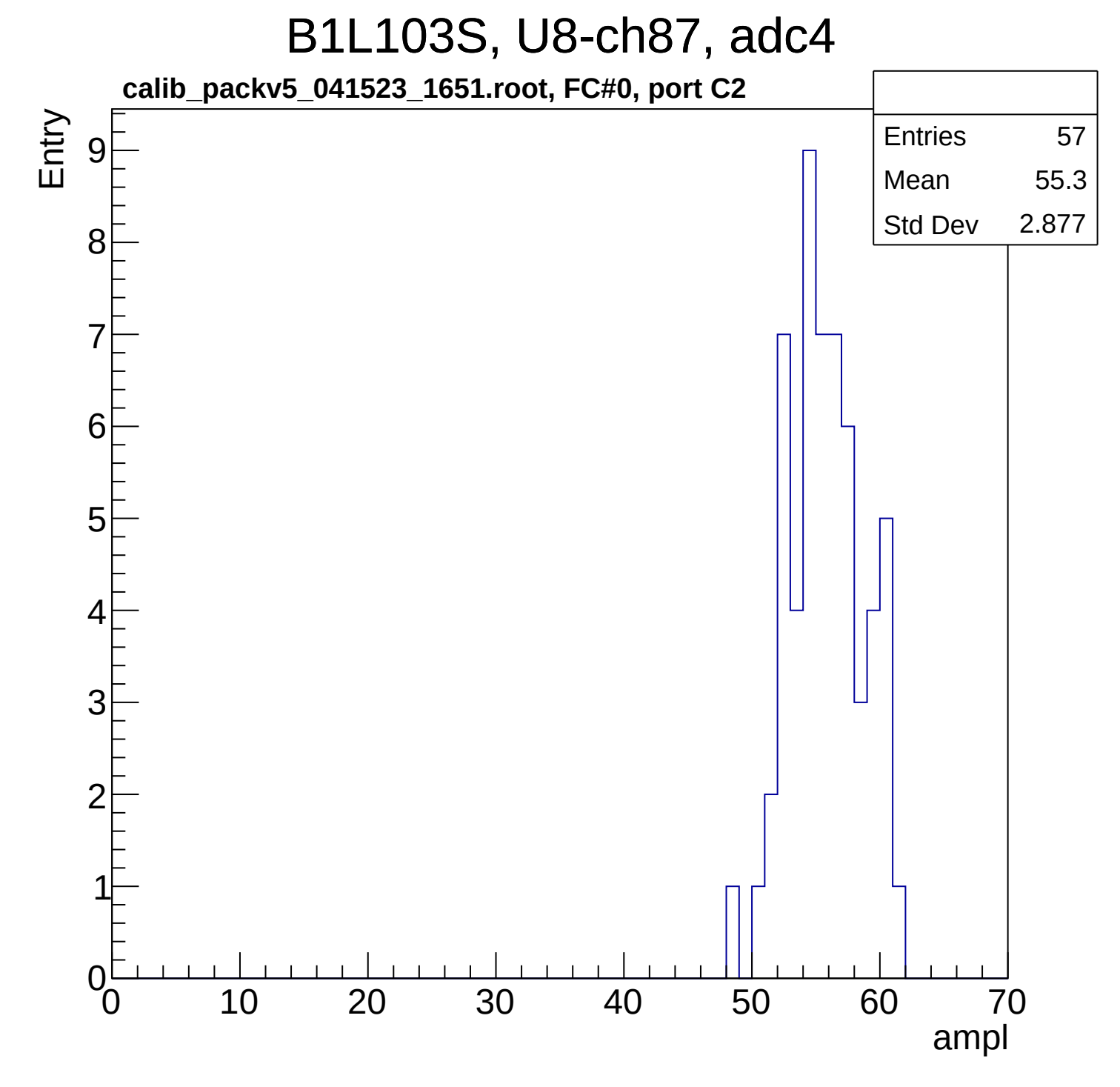
B1L103S, U8-ch87, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 55.3
Std Dev 2.877
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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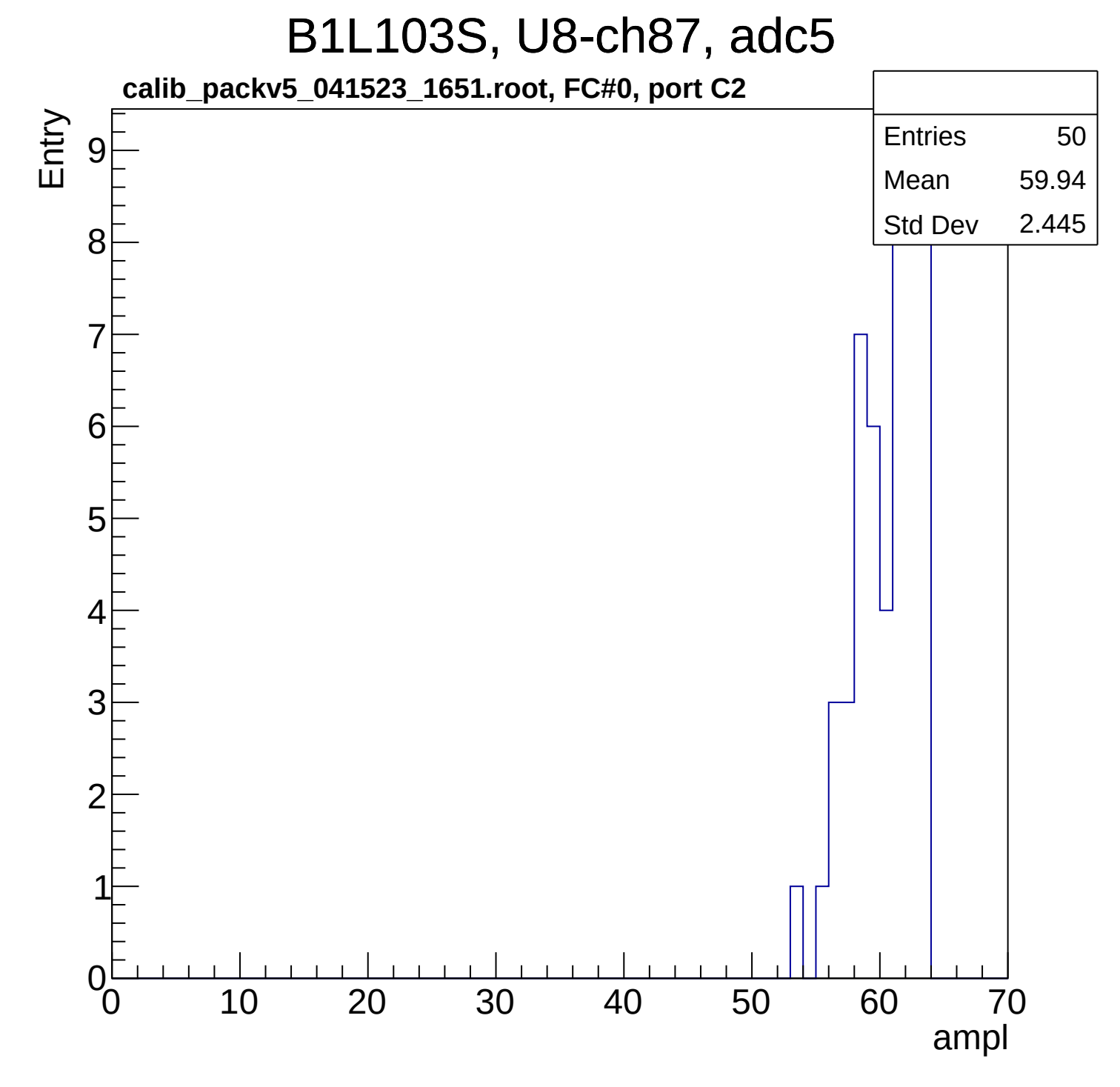
B1L103S, U8-ch87, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 59.94
Std Dev 2.445
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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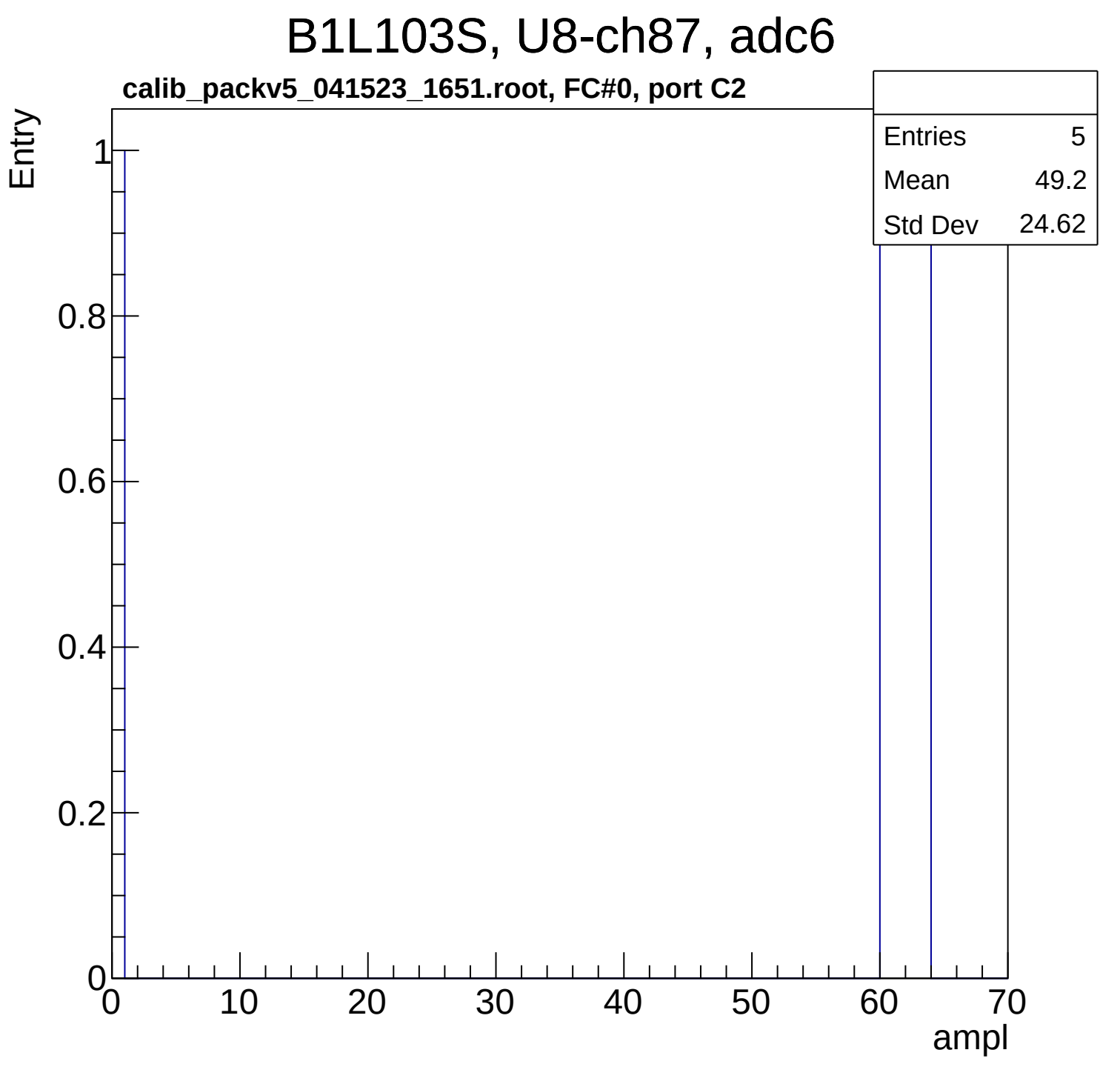
B1L103S, U8-ch87, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 49.2
Std Dev 24.62
Entry
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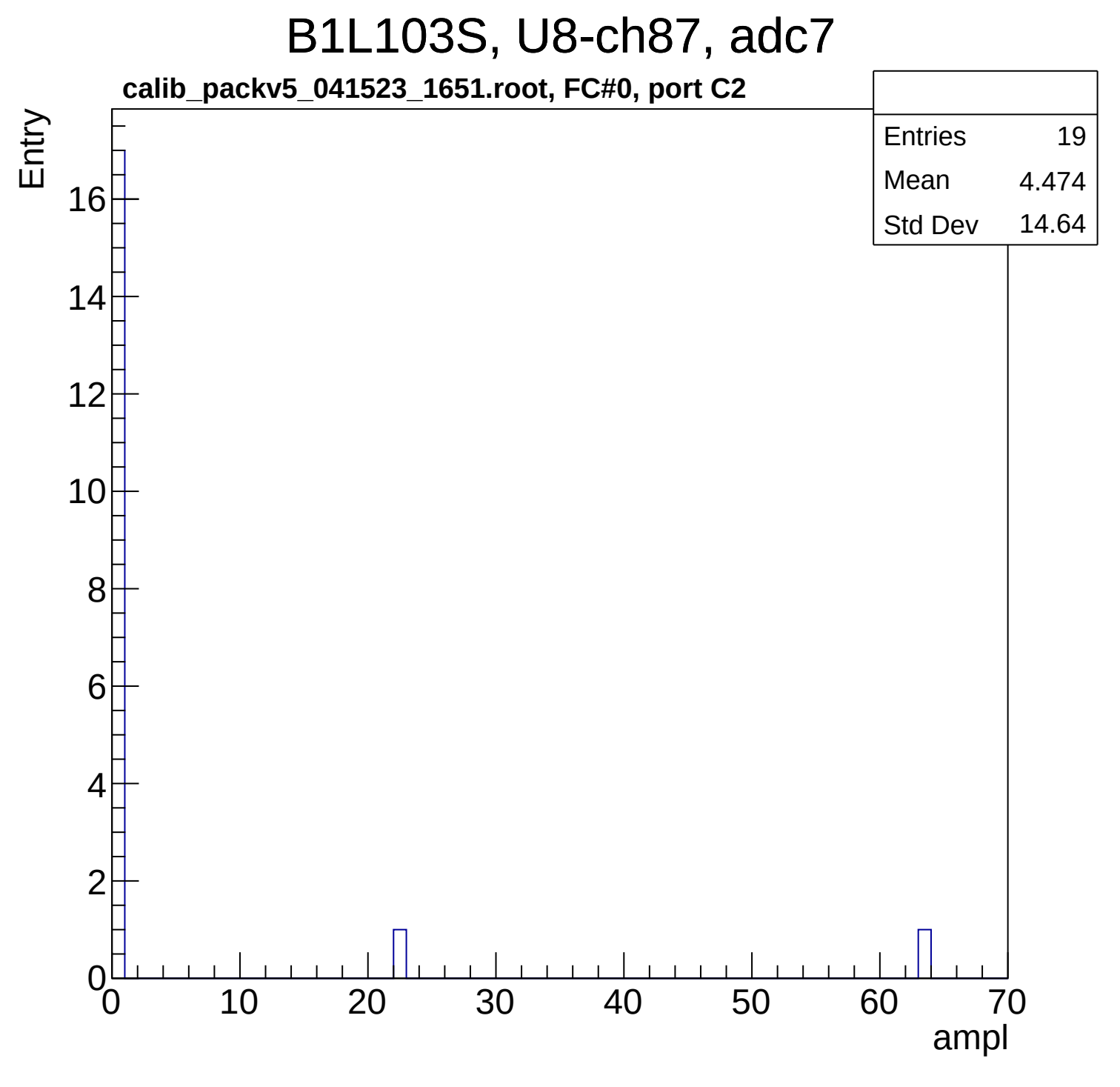
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch87, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 4.474
Std Dev 14.64
Entry
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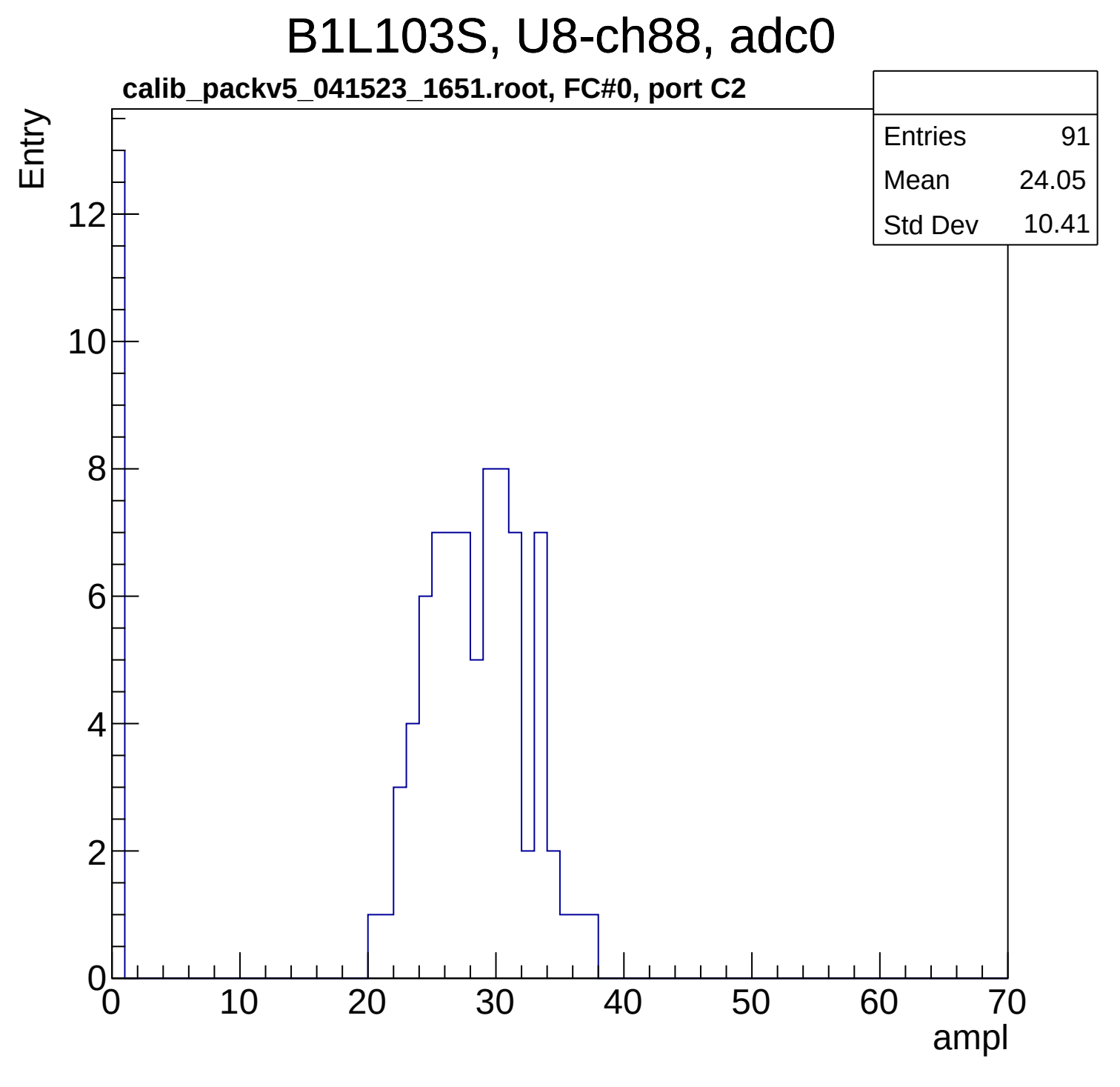
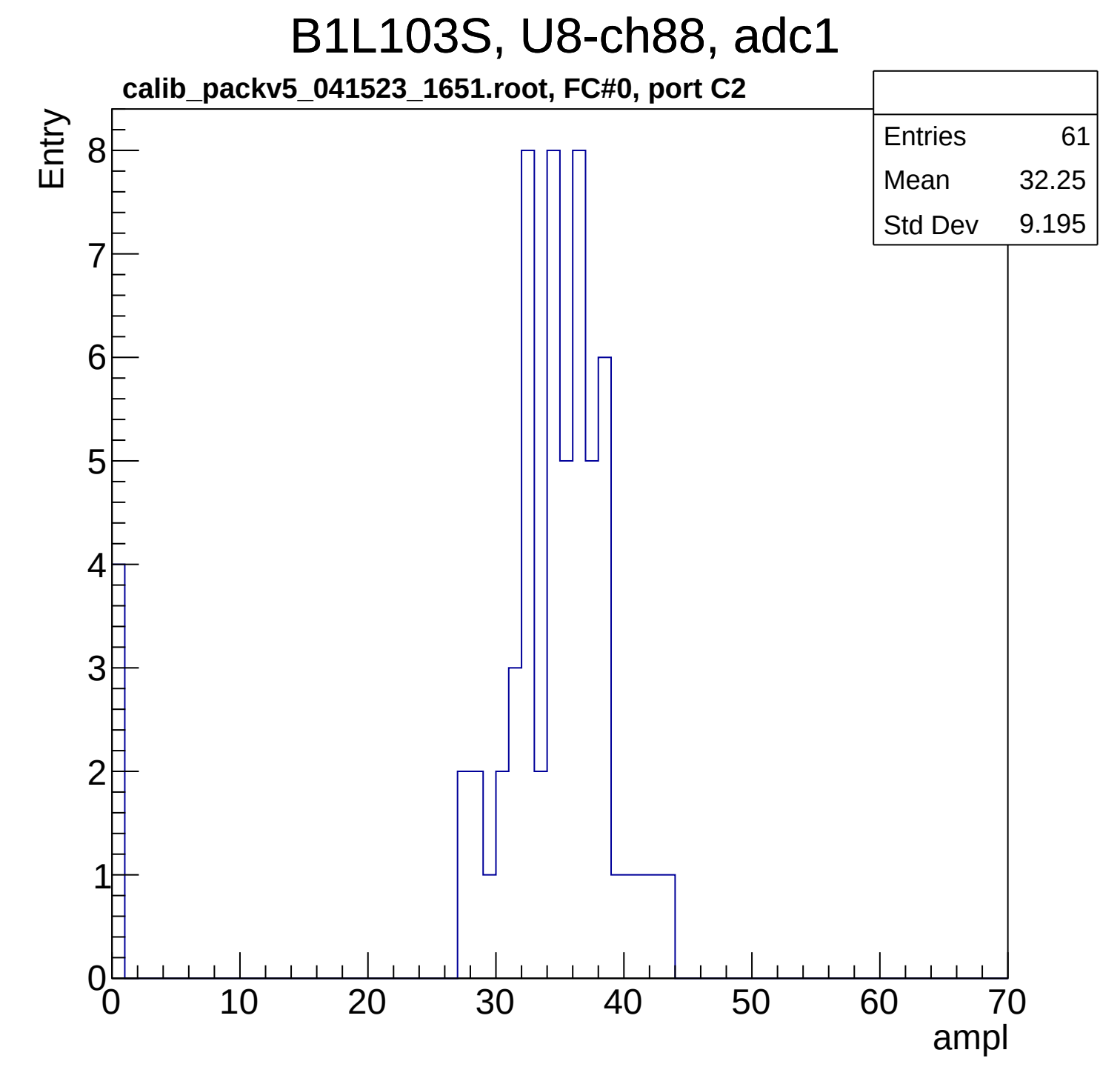
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch88, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 24.05
Std Dev 10.41
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch88, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 32.25
Std Dev 9.195
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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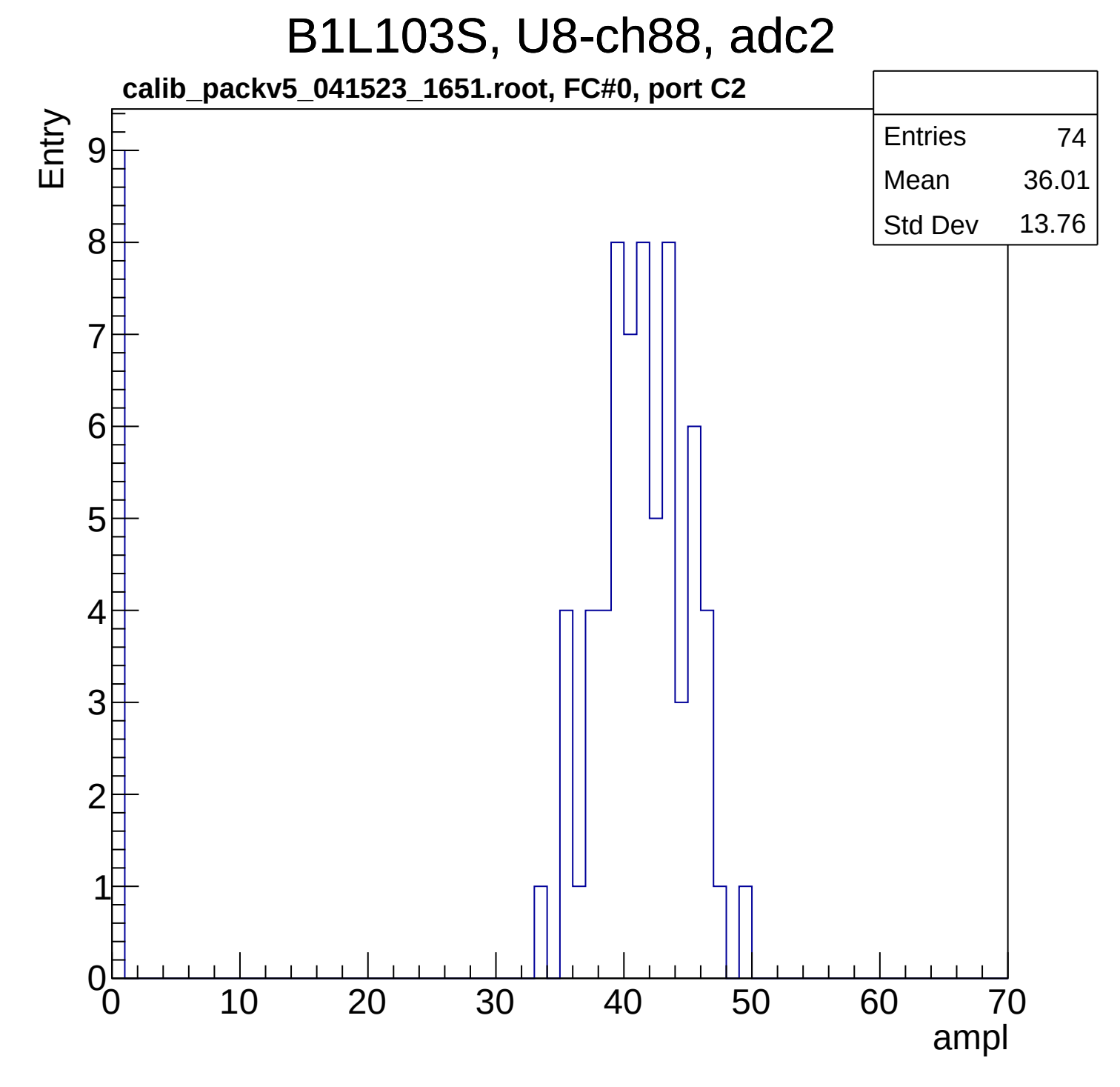
B1L103S, U8-ch88, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 36.01
Std Dev 13.76
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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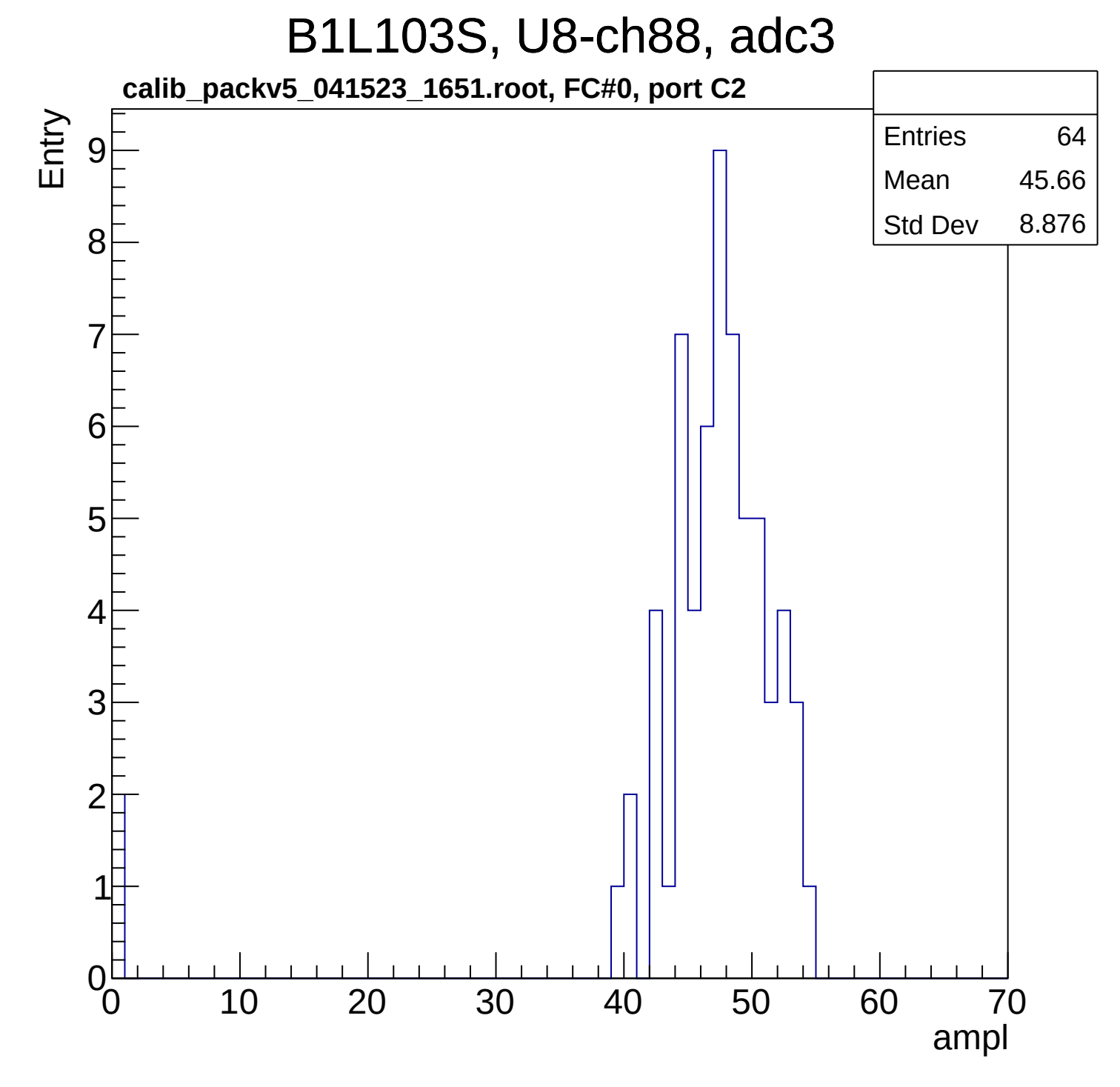
B1L103S, U8-ch88, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 45.66
Std Dev 8.876
Entry
ampl
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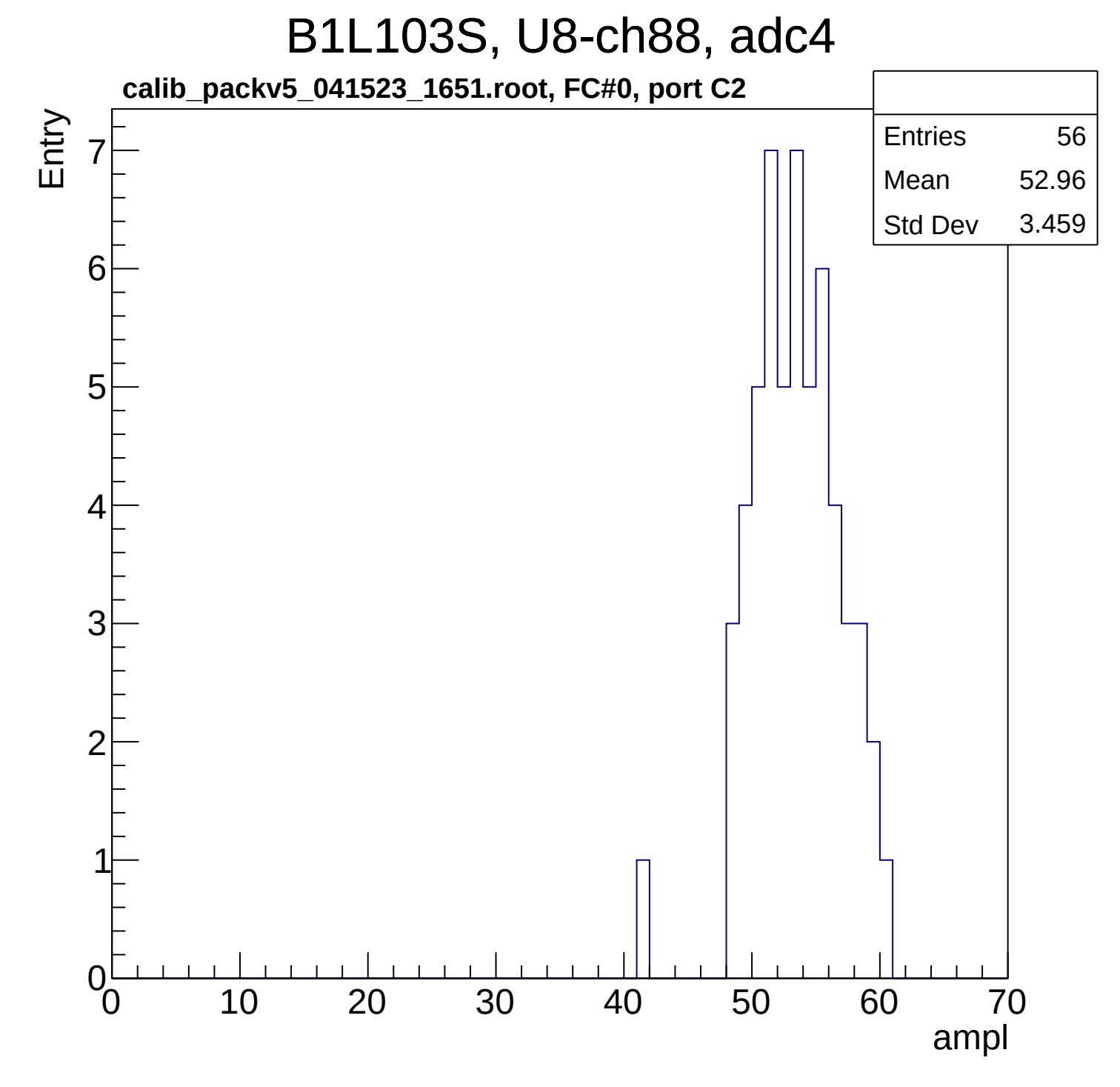
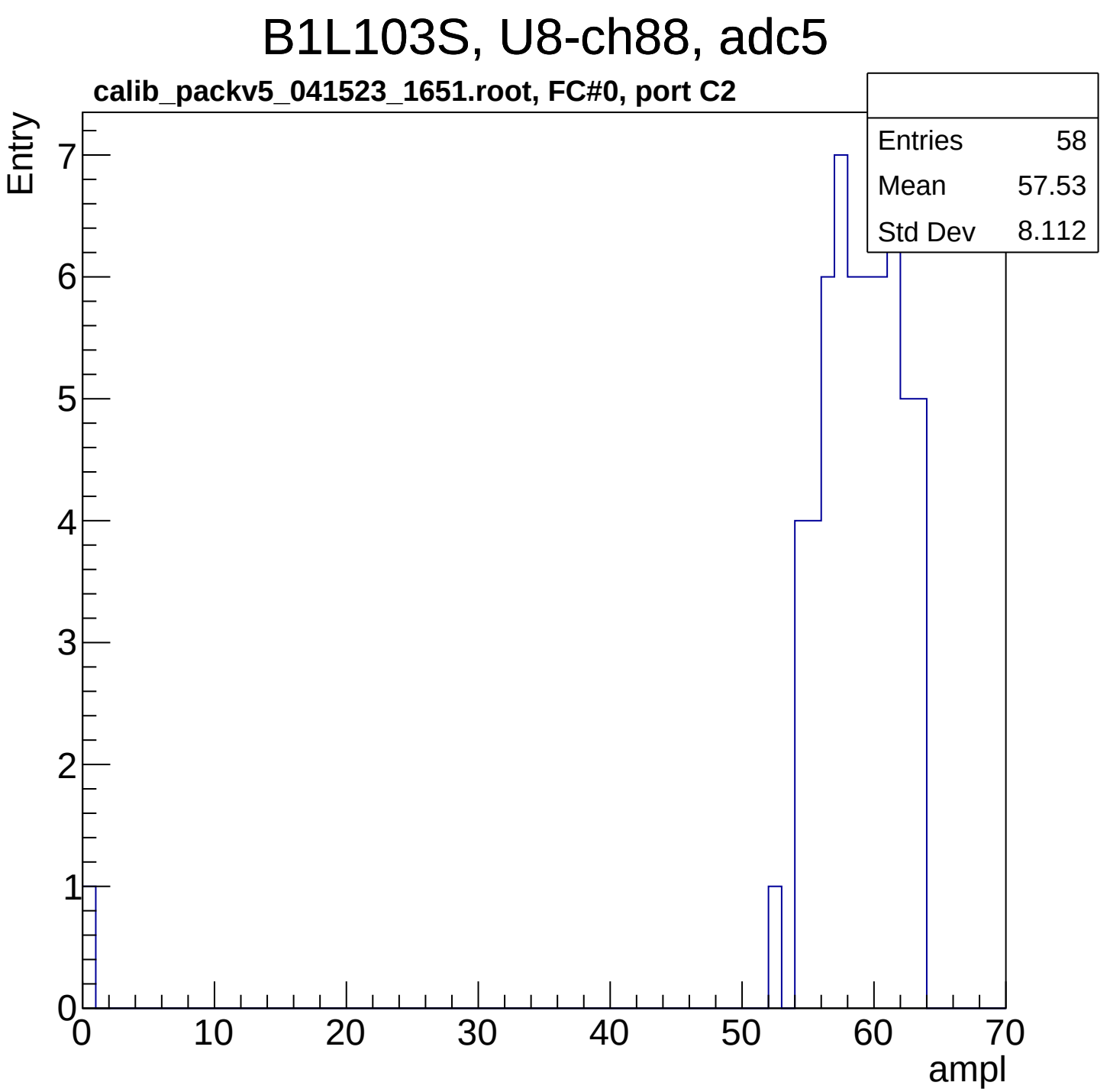
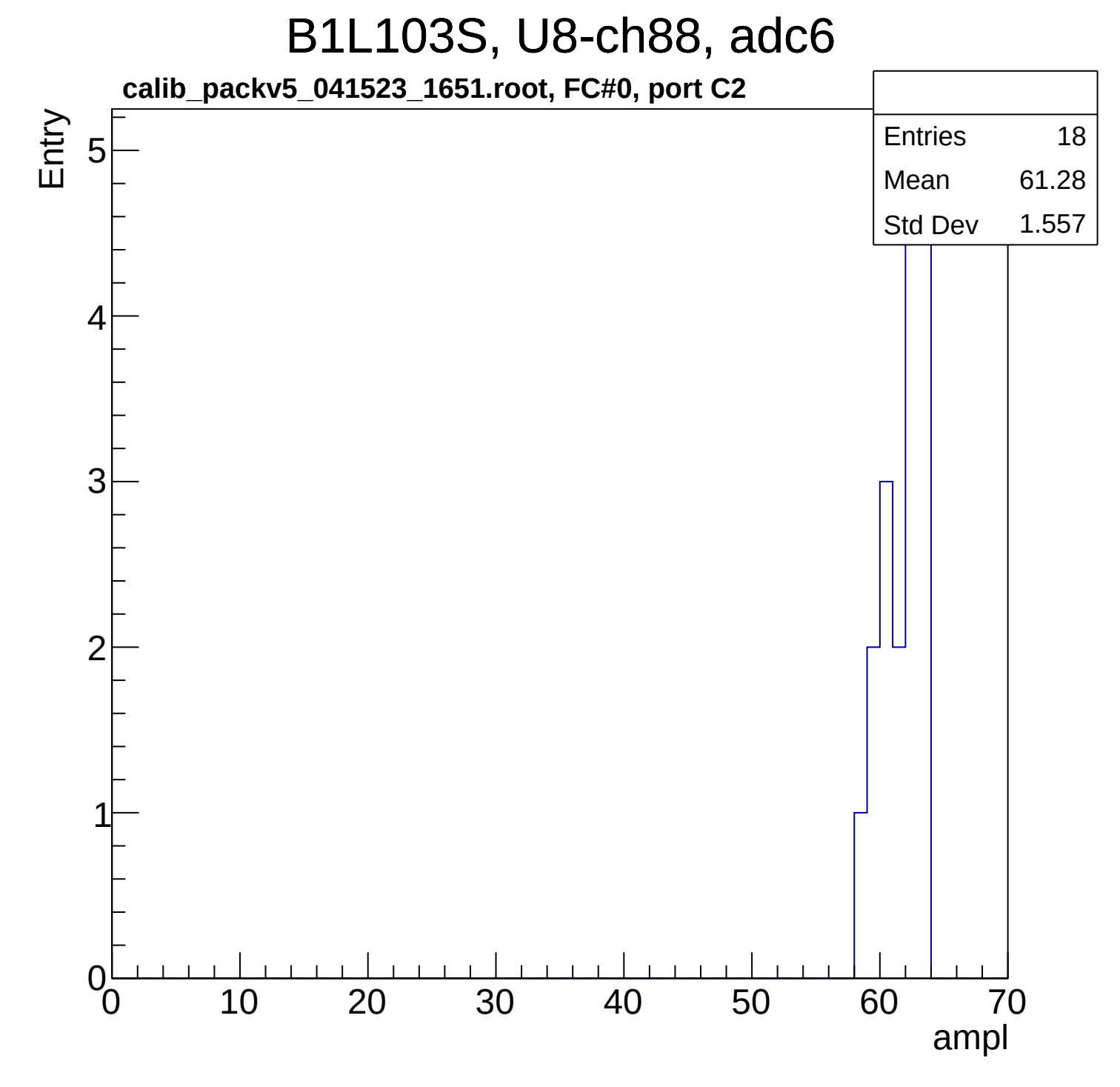
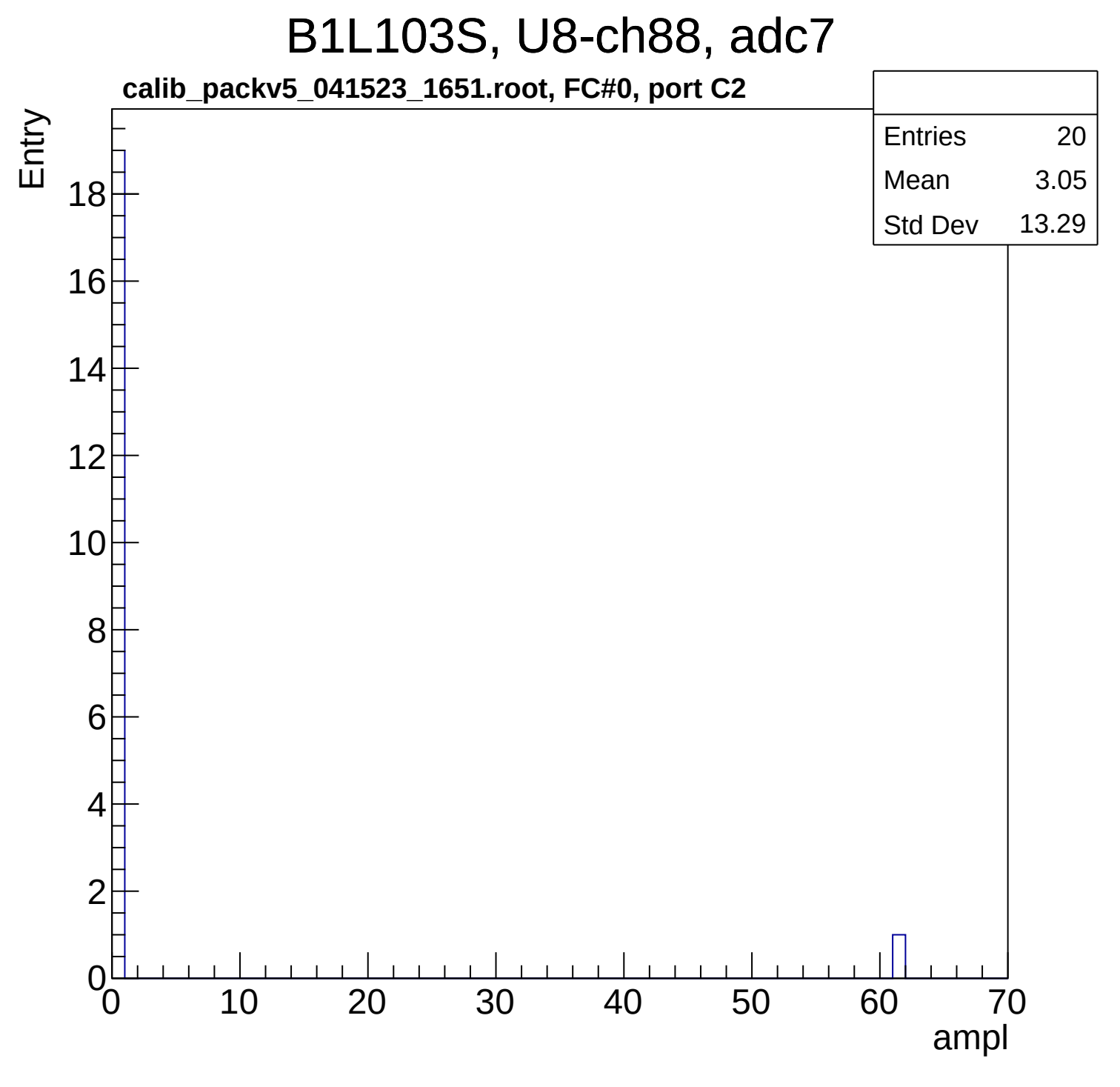
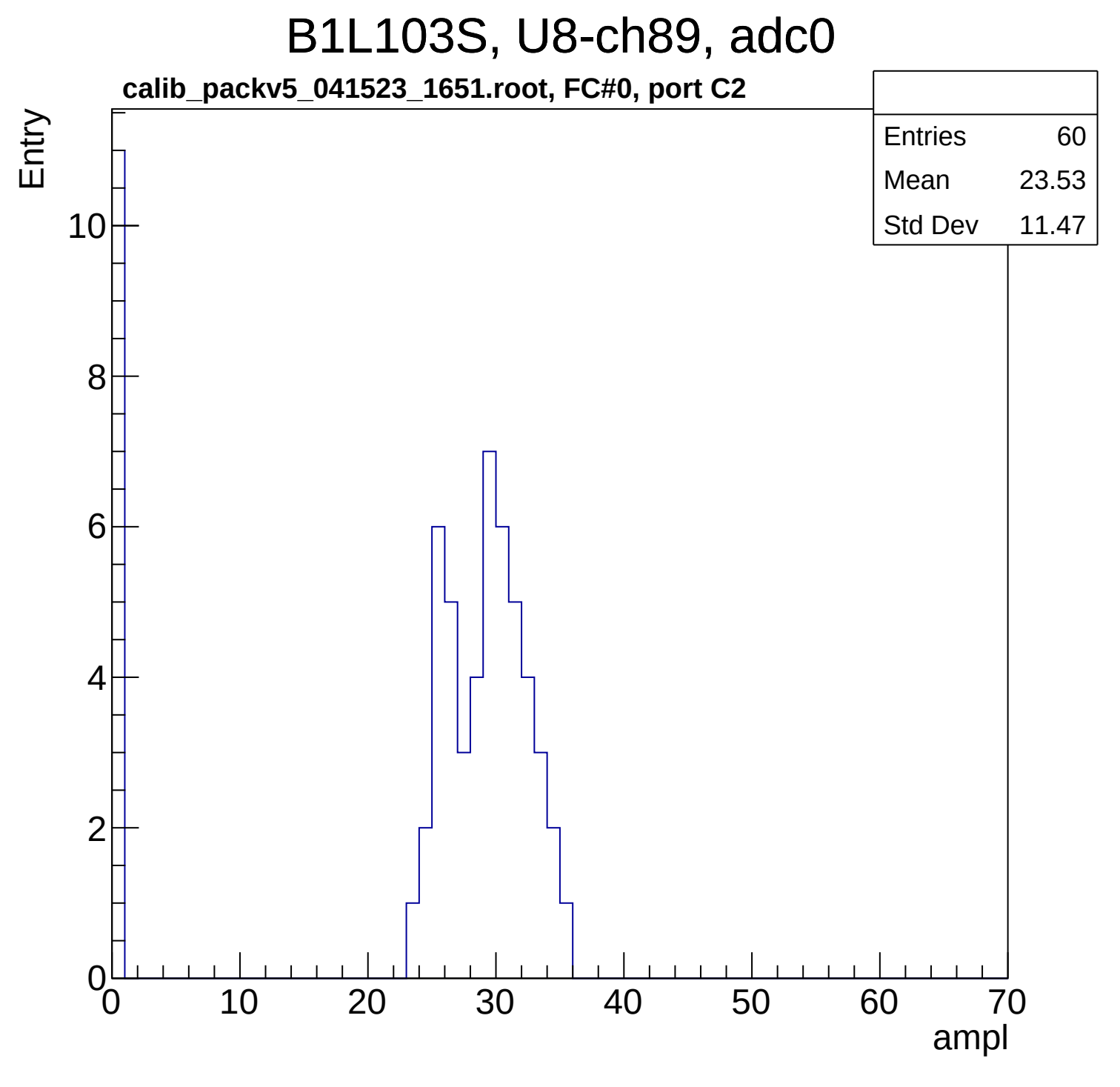
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

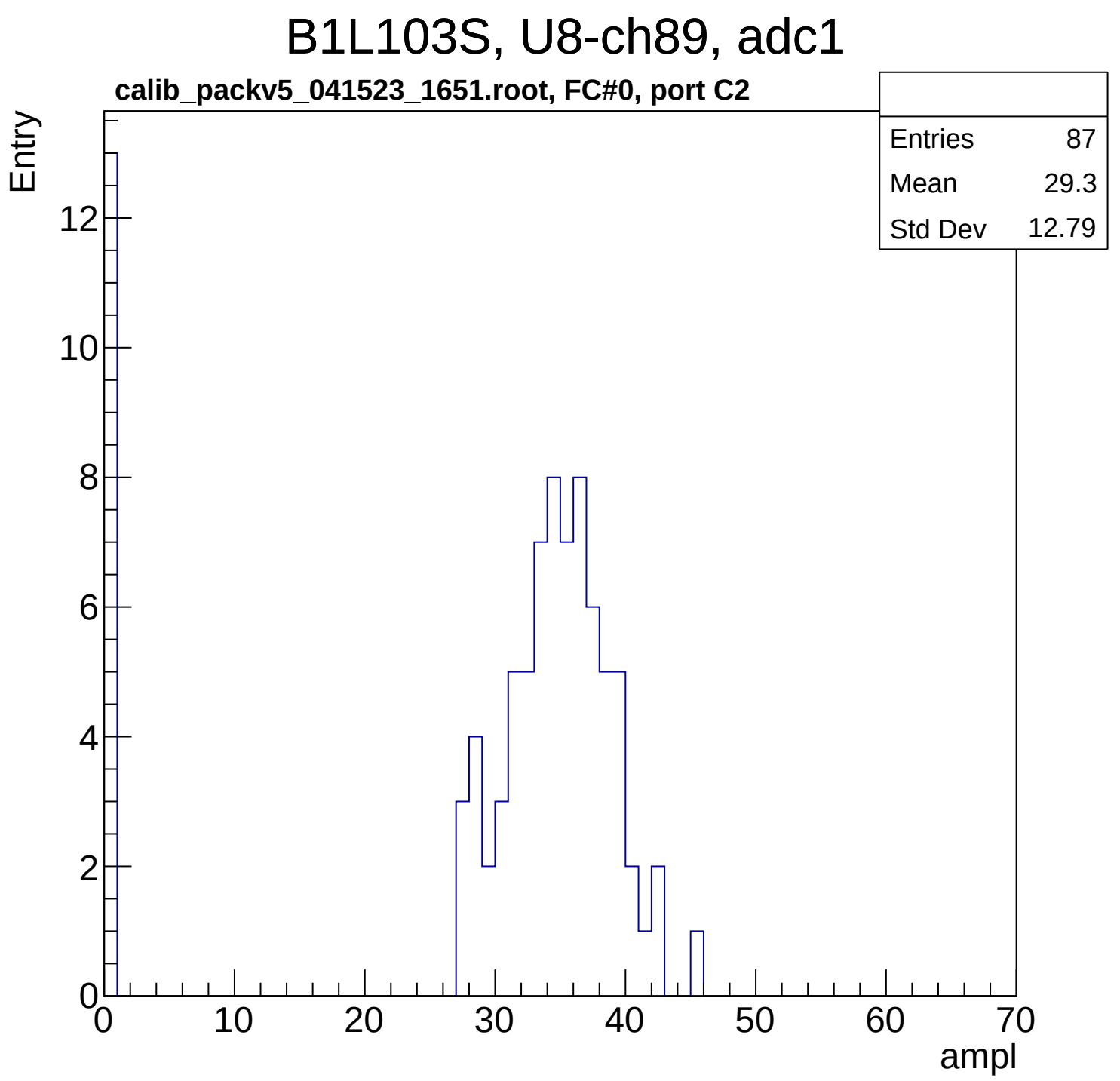

B1L103S, U8-ch88, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 52.96
Std Dev 3.459
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U8-ch88, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 57.53
Std Dev 8.112
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U8-ch88, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 61.28
Std Dev 1.557
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch88, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.05
Std Dev 13.29
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch89, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 23.53
Std Dev 11.47
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch89, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 29.3
Std Dev 12.79
Entry
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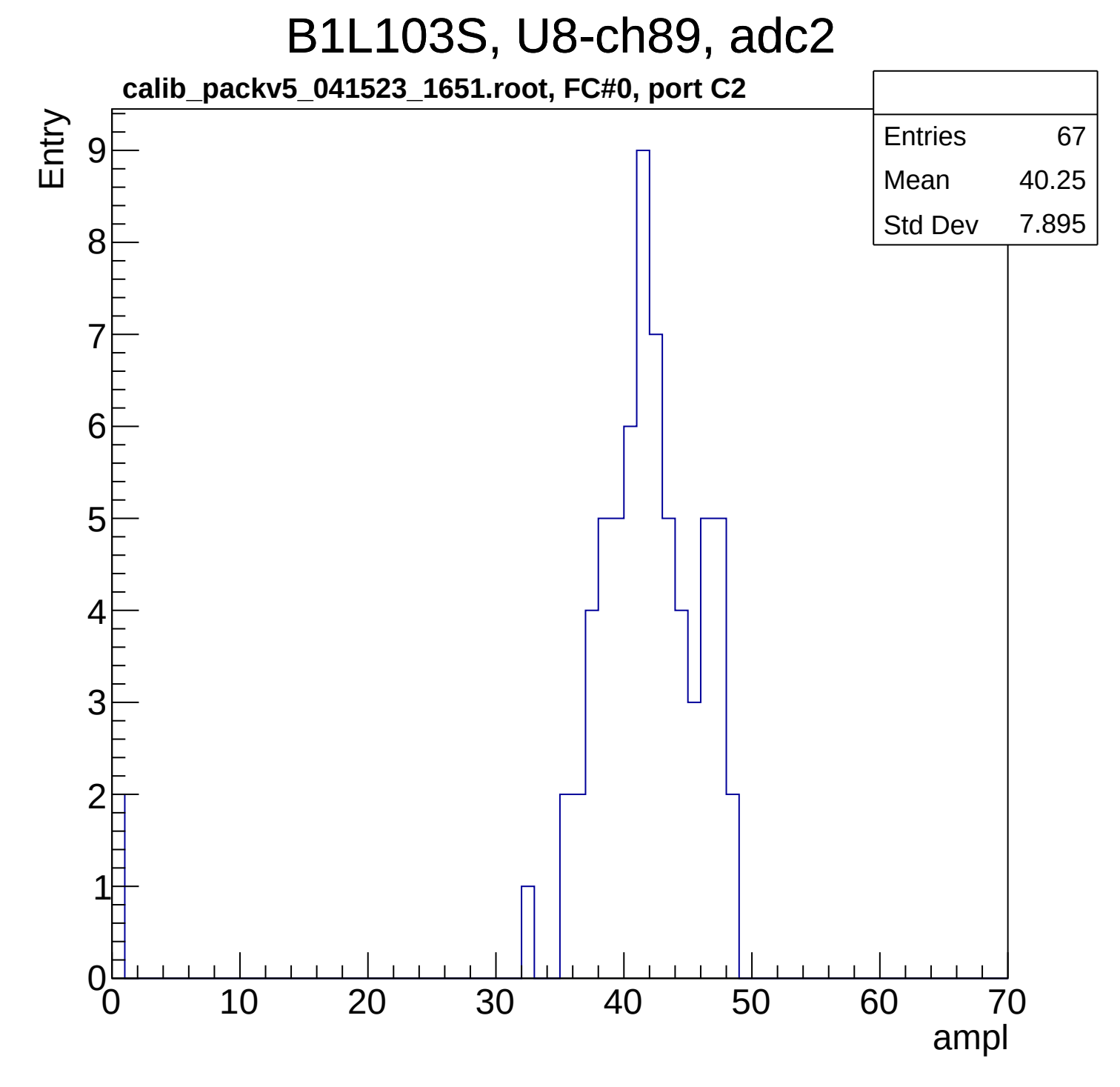
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch89, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 40.25
Std Dev 7.895
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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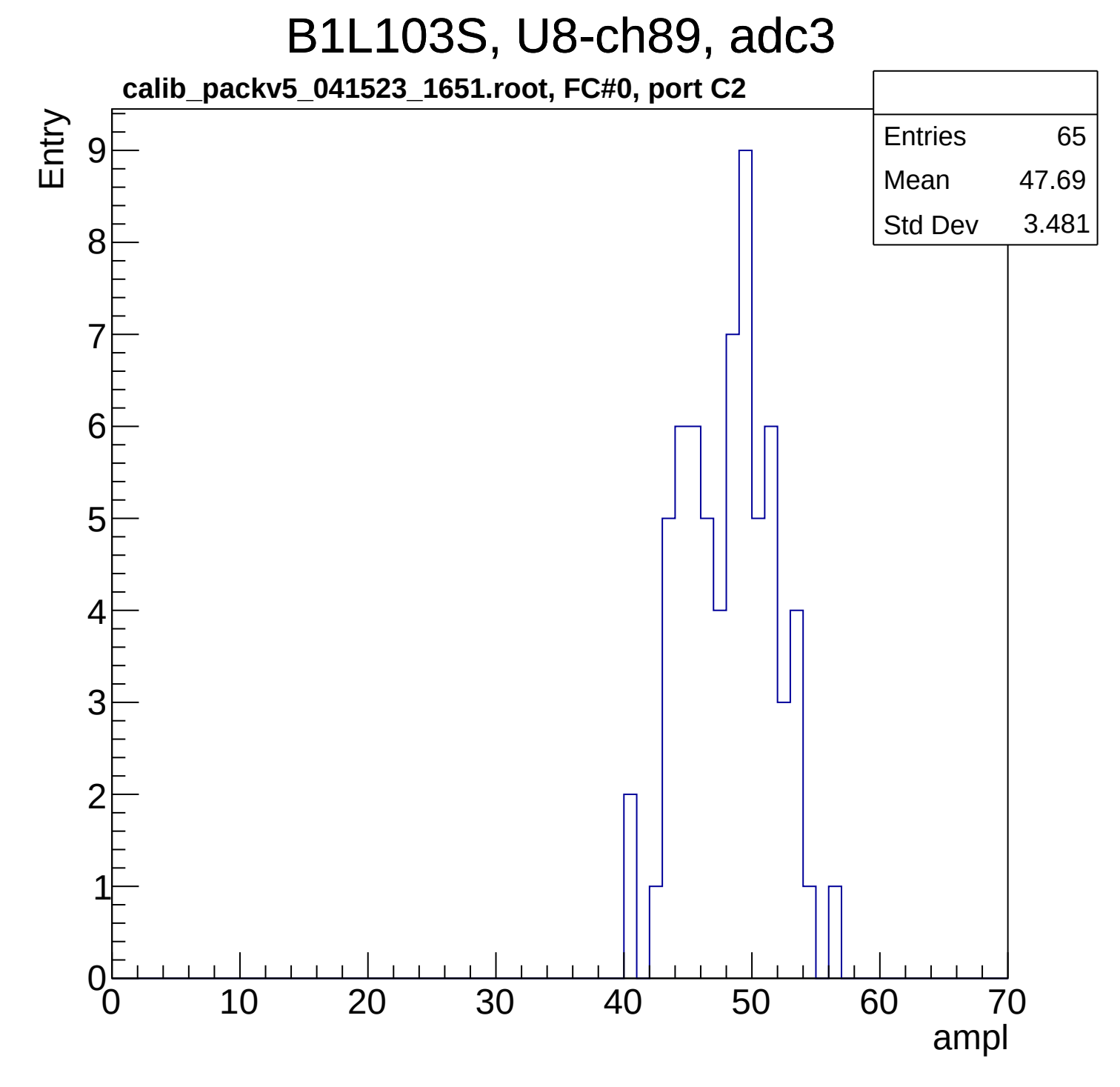
B1L103S, U8-ch89, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 47.69
Std Dev 3.481
Entry
ampl
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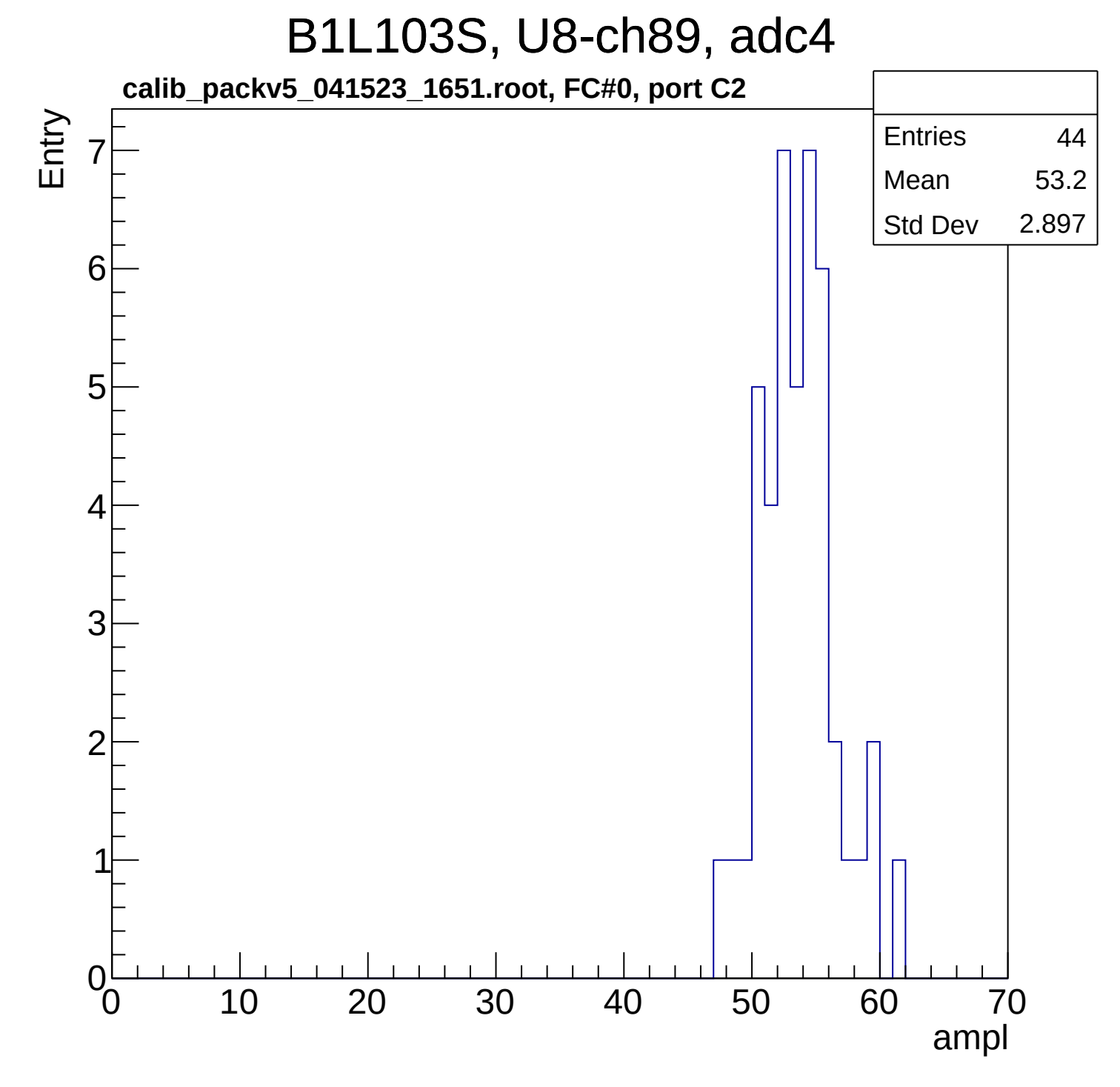
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U8-ch89, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 53.2
Std Dev 2.897
Entry
ampl
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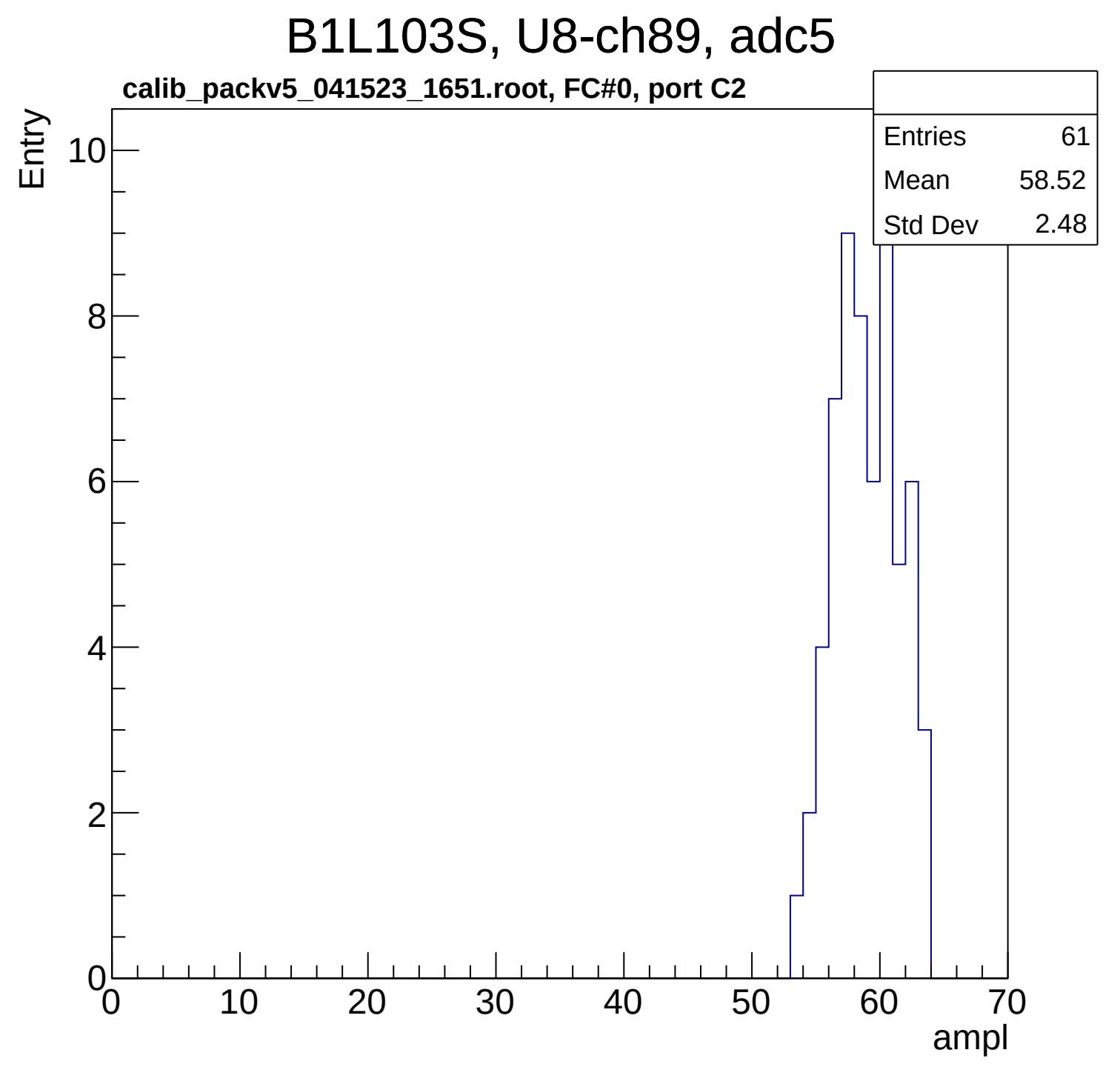
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U8-ch89, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 58.52
Std Dev 2.48
Entry
ampl
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0
10
20
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40
50
60
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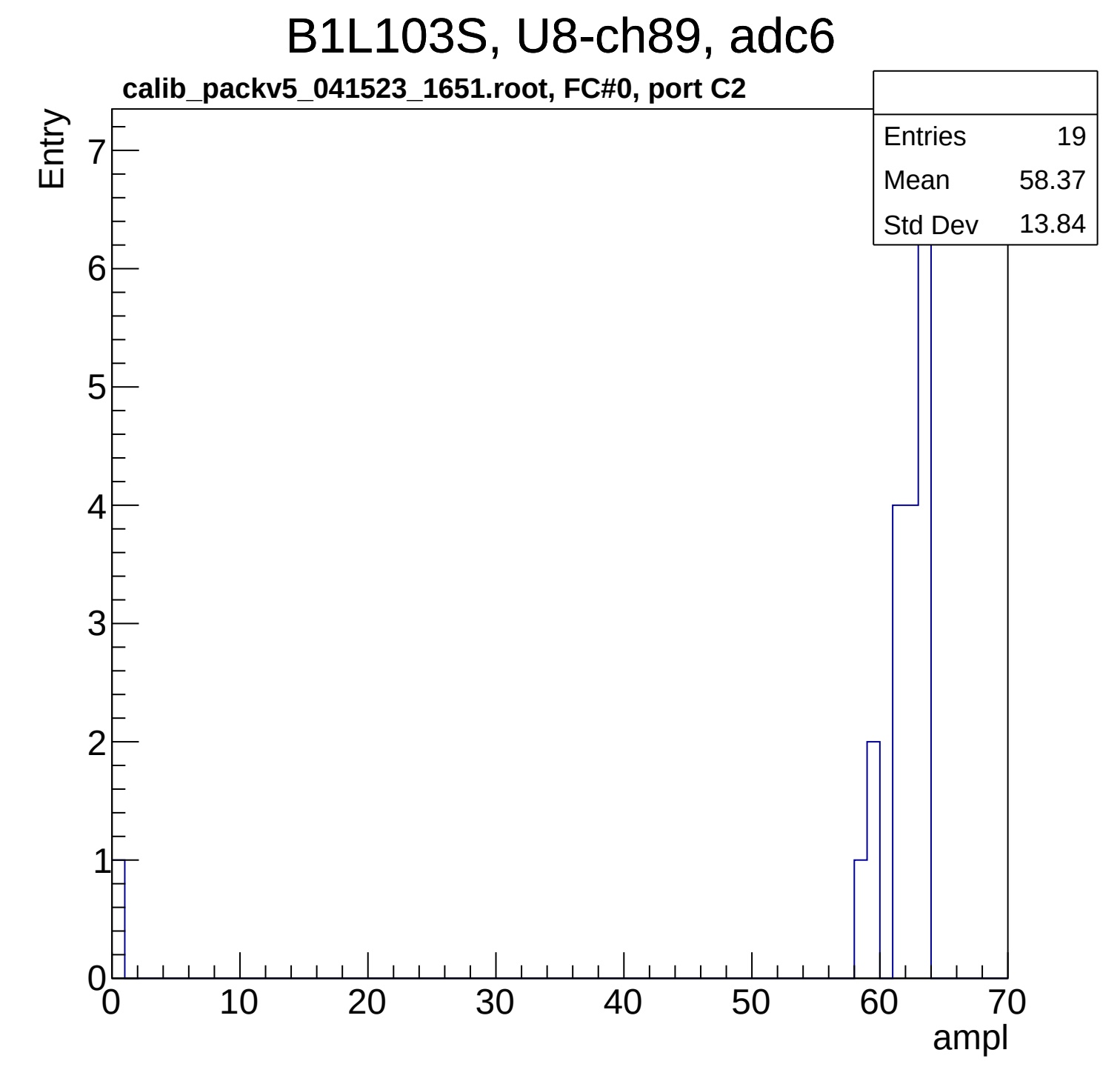
B1L103S, U8-ch89, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 58.37
Std Dev 13.84
Entry
ampl
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1
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3
4
5
6
7
0
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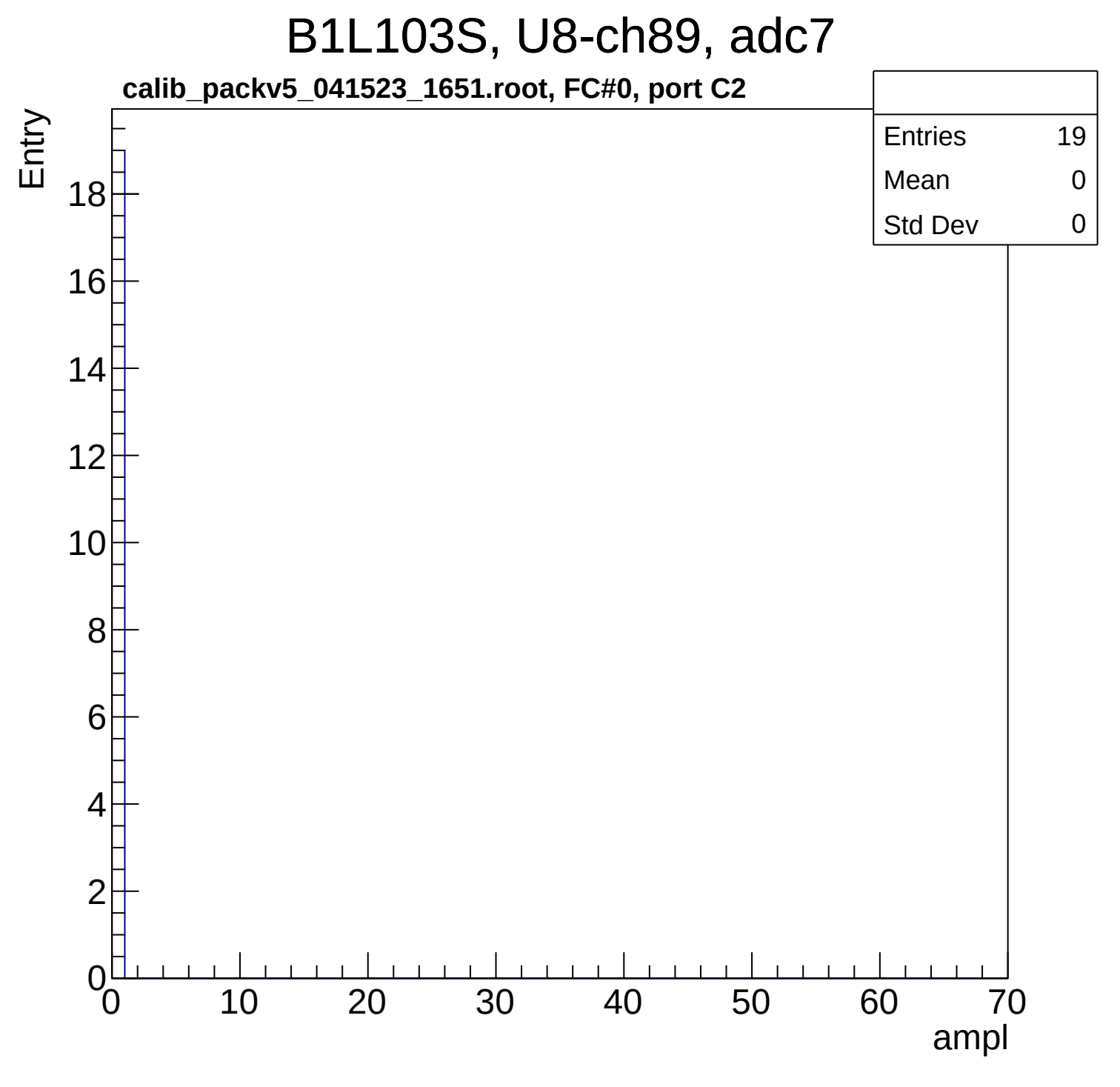
40
50
60
70


B1L103S, U8-ch89, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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2
4
6
8
10
12
14
16
18
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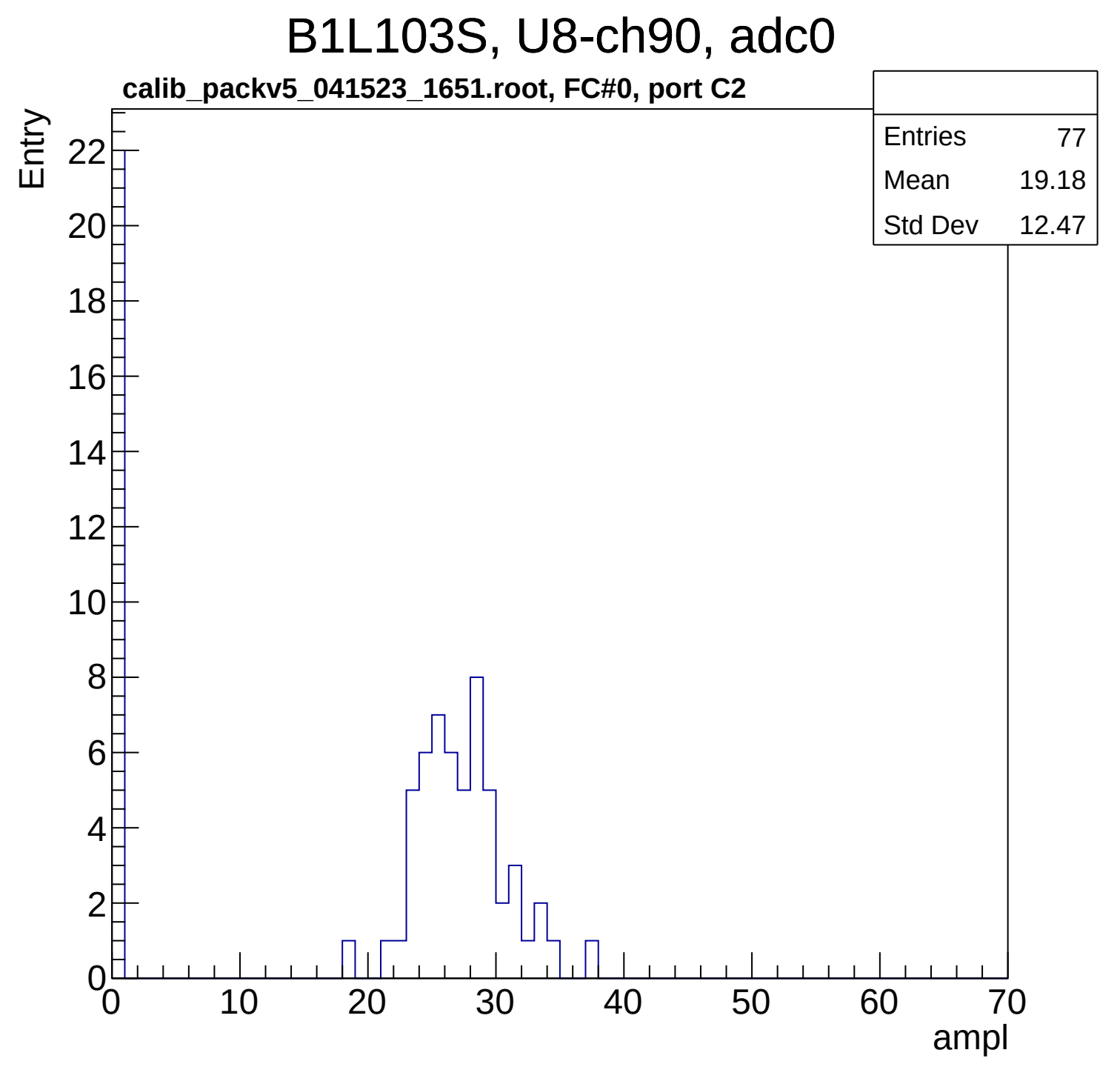
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch90, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 19.18
Std Dev 12.47
Entry
ampl
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8
10
12
14
16
18
20
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0
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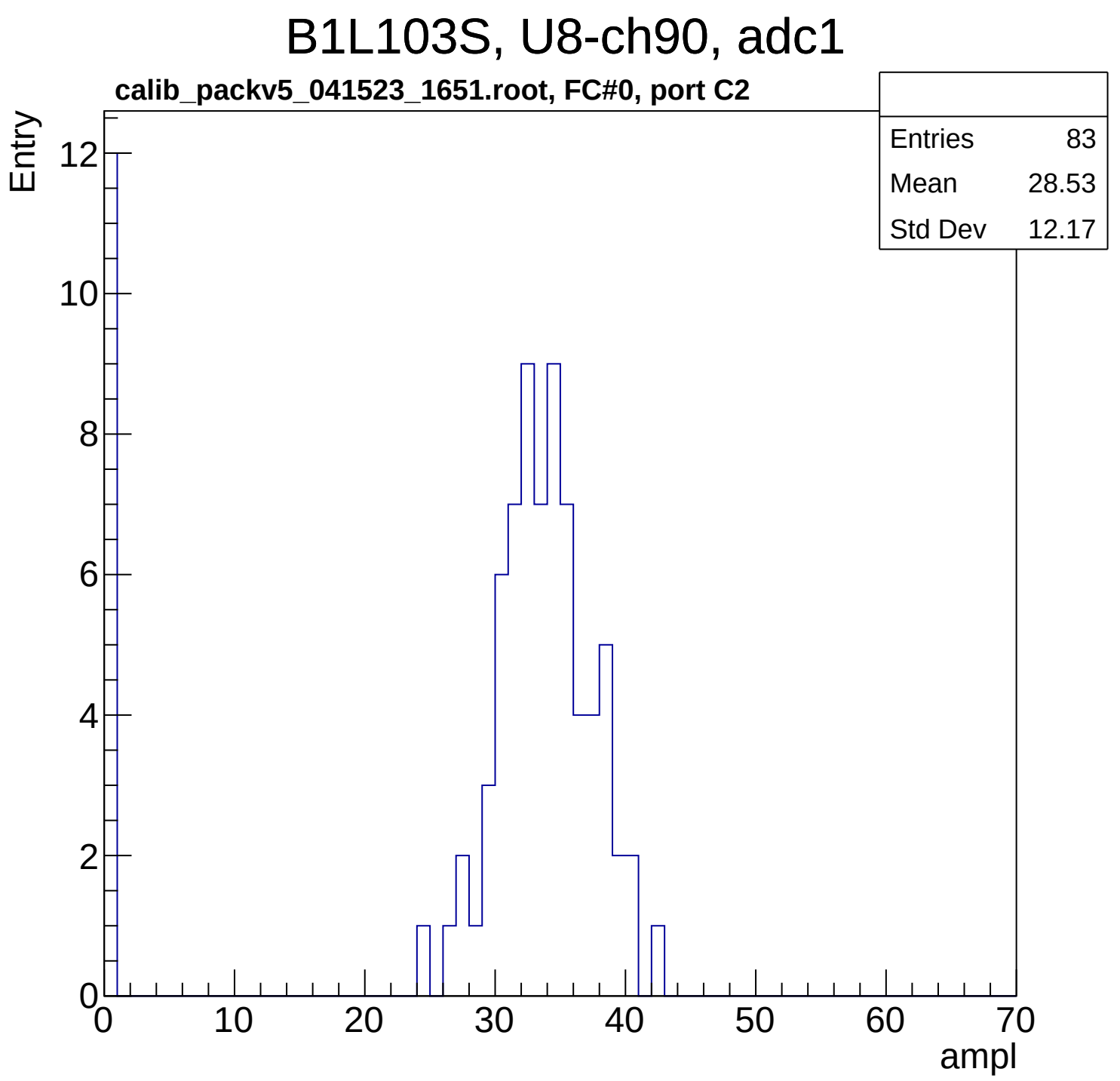
30
40
50
60
70


B1L103S, U8-ch90, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 28.53
Std Dev 12.17
Entry
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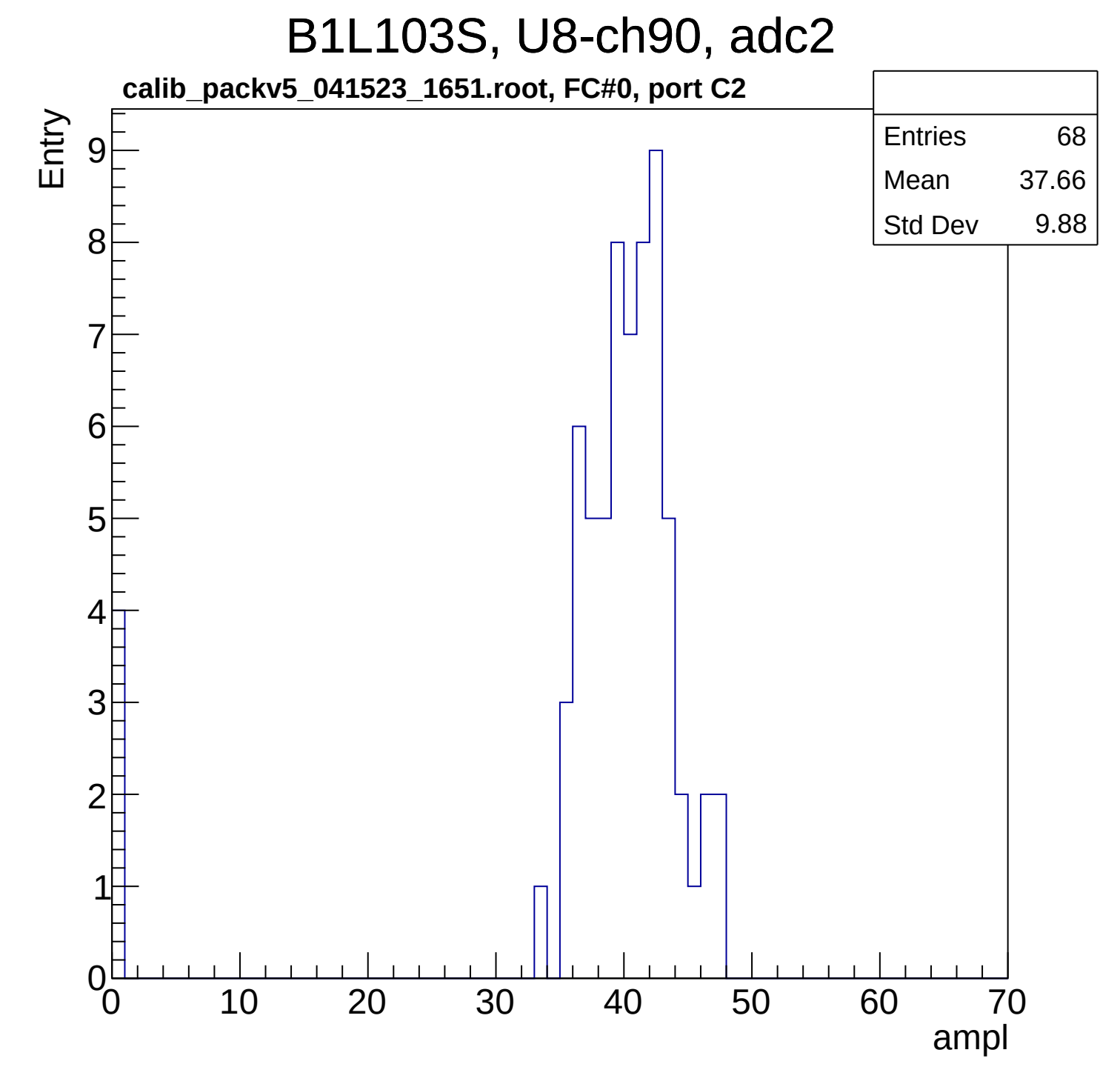
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch90, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 37.66
Std Dev 9.88
Entry
ampl
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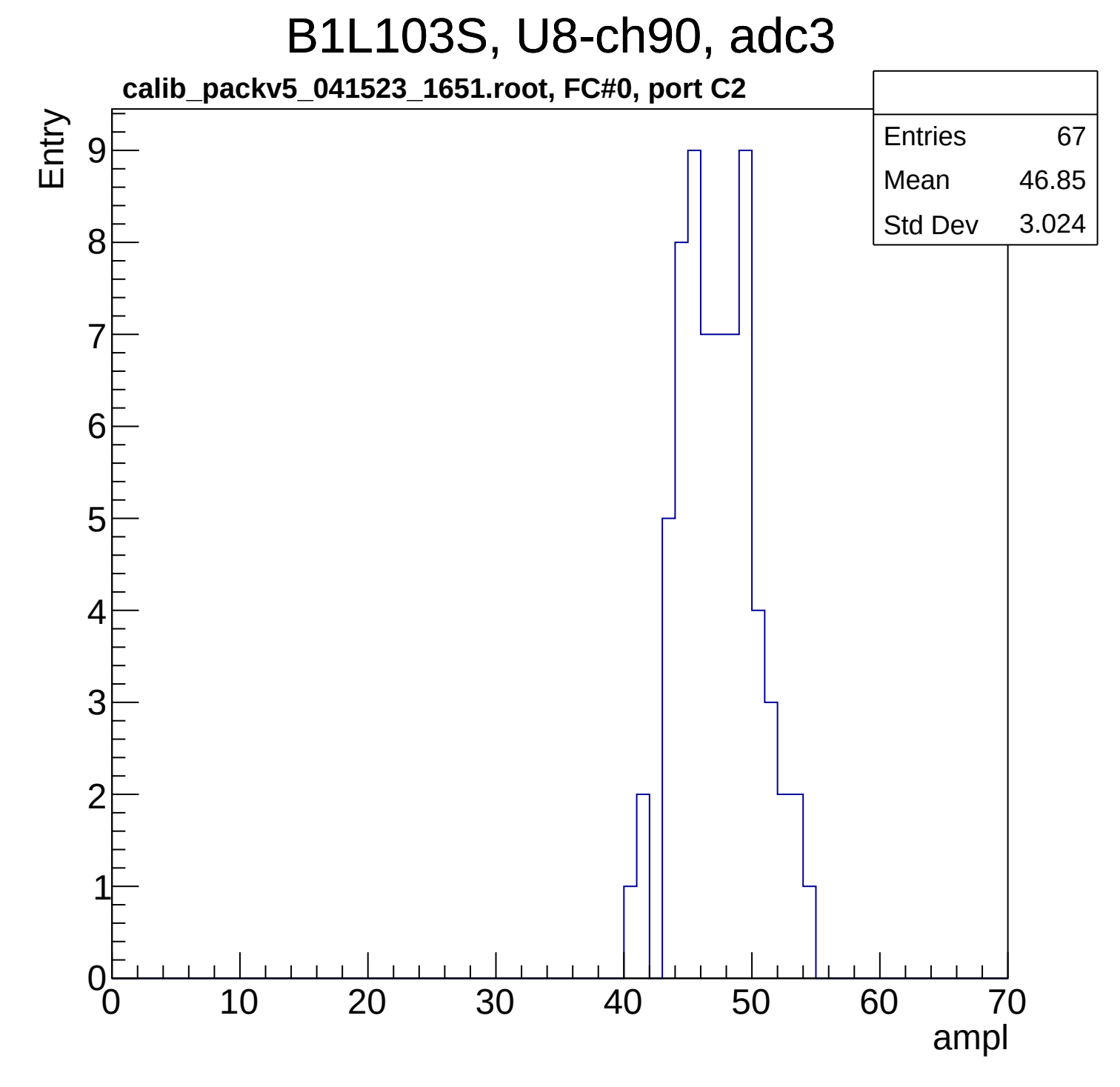
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U8-ch90, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 46.85
Std Dev 3.024
Entry
ampl
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2
3
4
5
6
7
8
9
0
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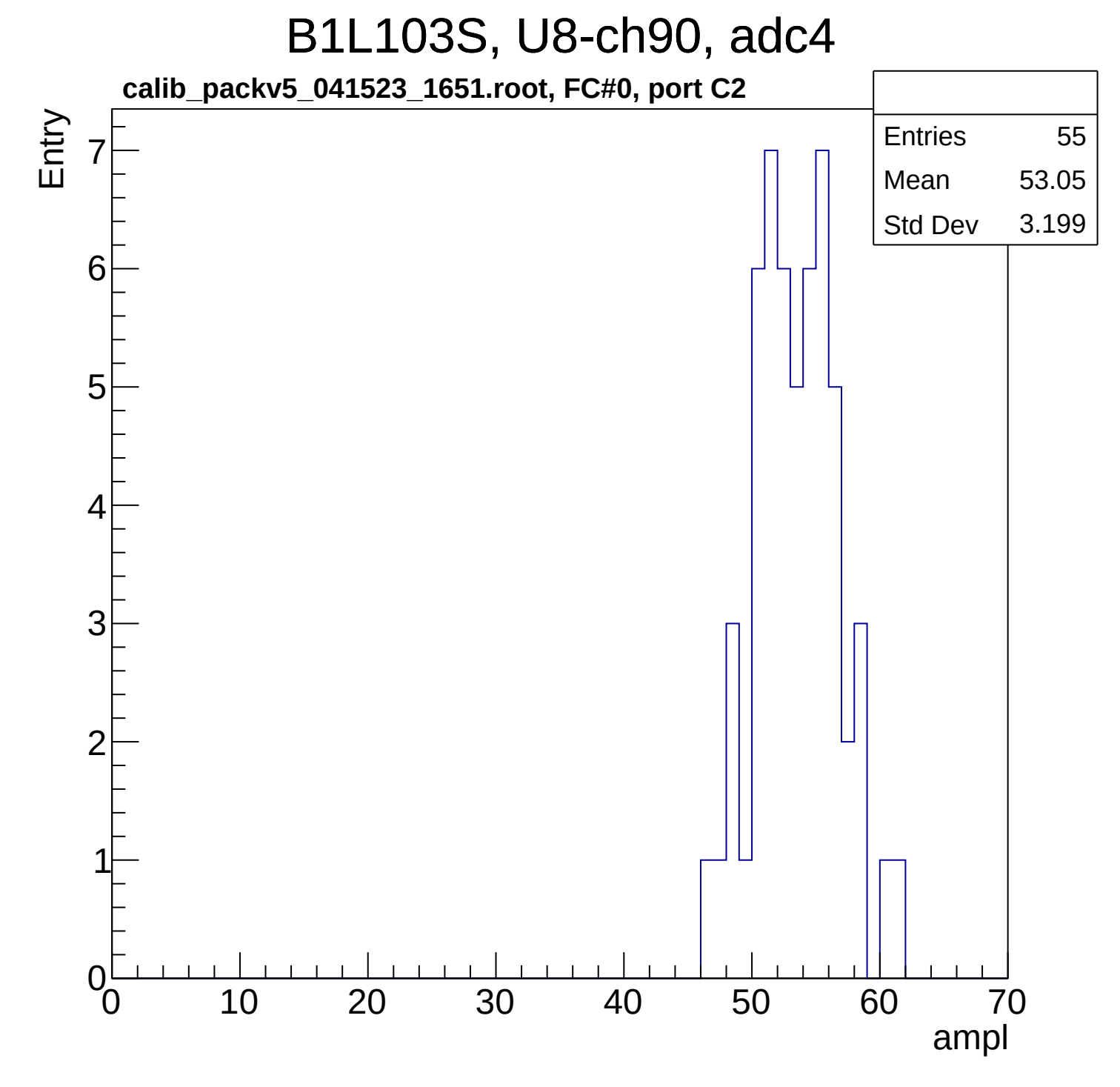
50
60
70


B1L103S, U8-ch90, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 53.05
Std Dev 3.199
Entry
ampl
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1
2
3
4
5
6
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0
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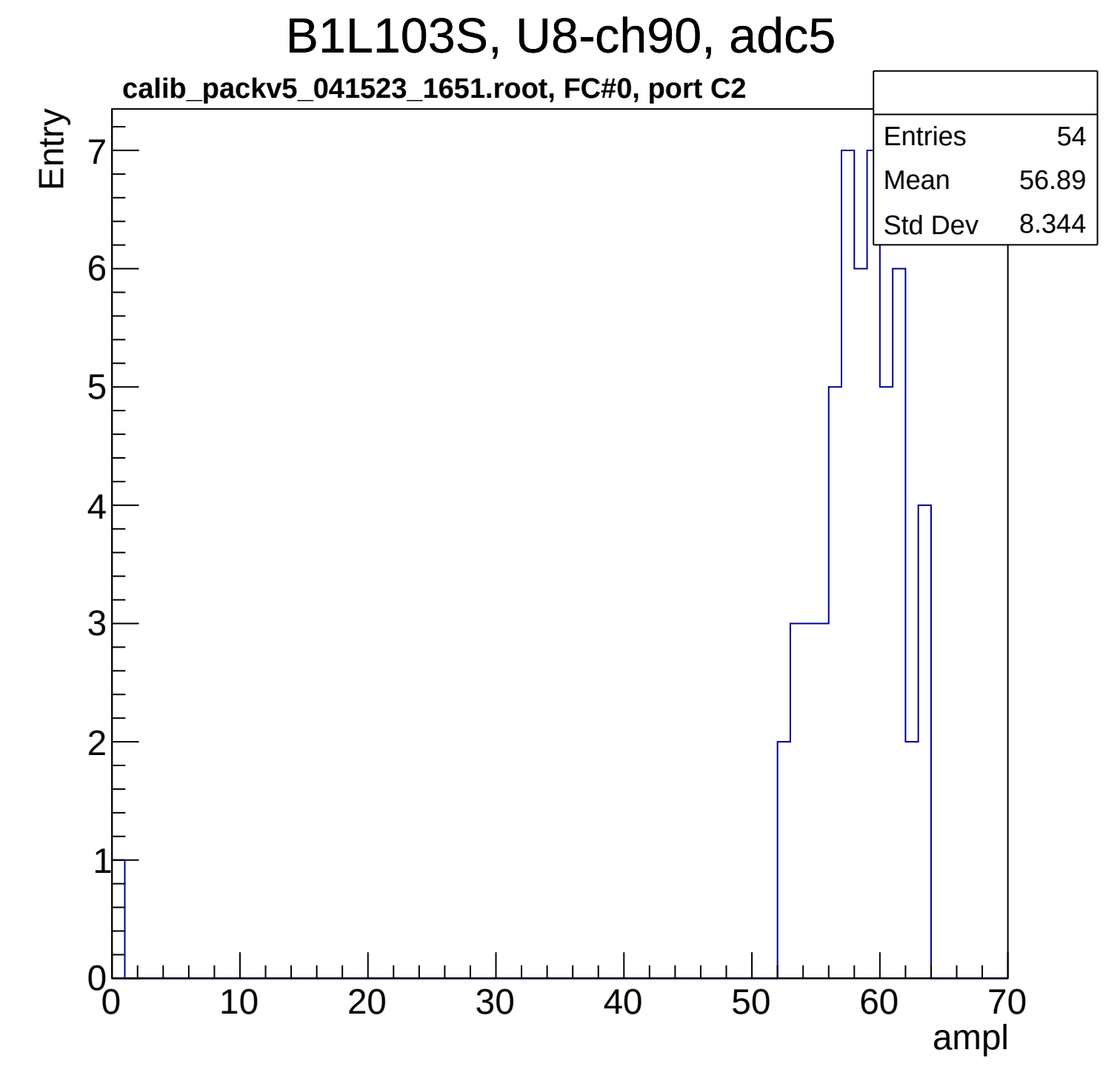
20
30
40
50
60
70


B1L103S, U8-ch90, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 56.89
Std Dev 8.344
Entry
ampl
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6
7
0
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40
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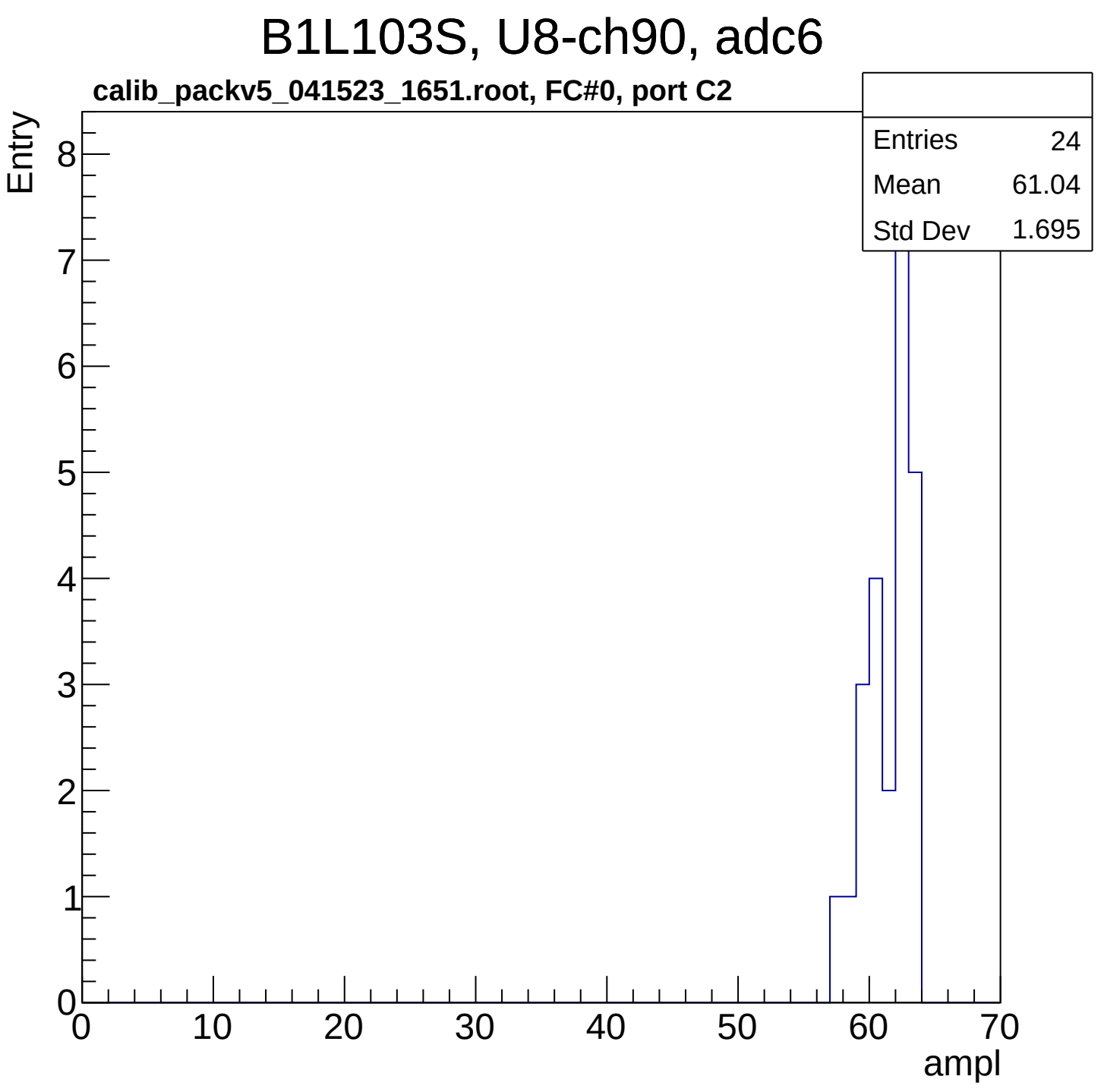
60
70


B1L103S, U8-ch90, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 61.04
Std Dev 1.695
Entry
ampl
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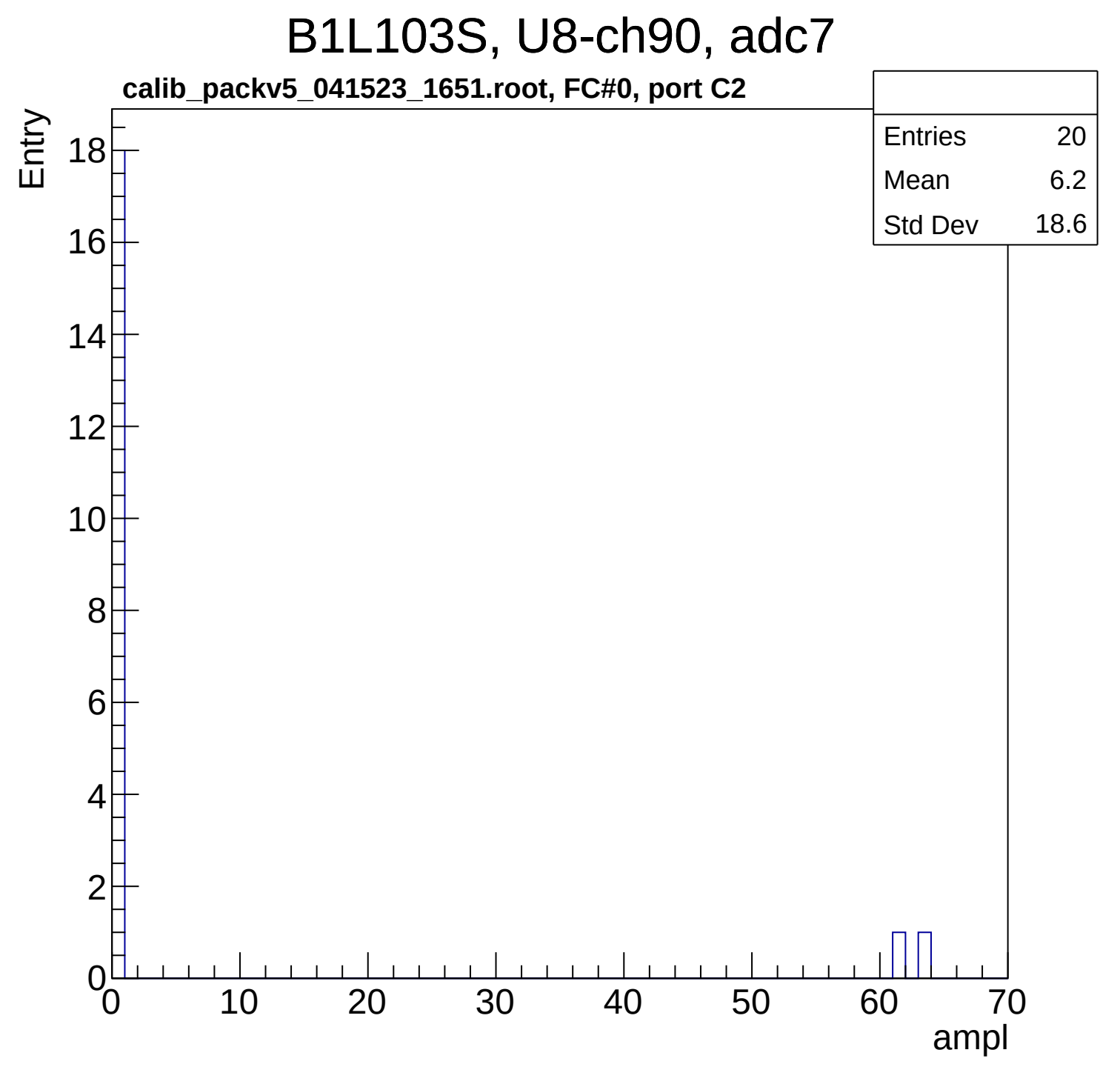
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch90, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 6.2
Std Dev 18.6
Entry
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6
8
10
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14
16
18
0
10
20
30
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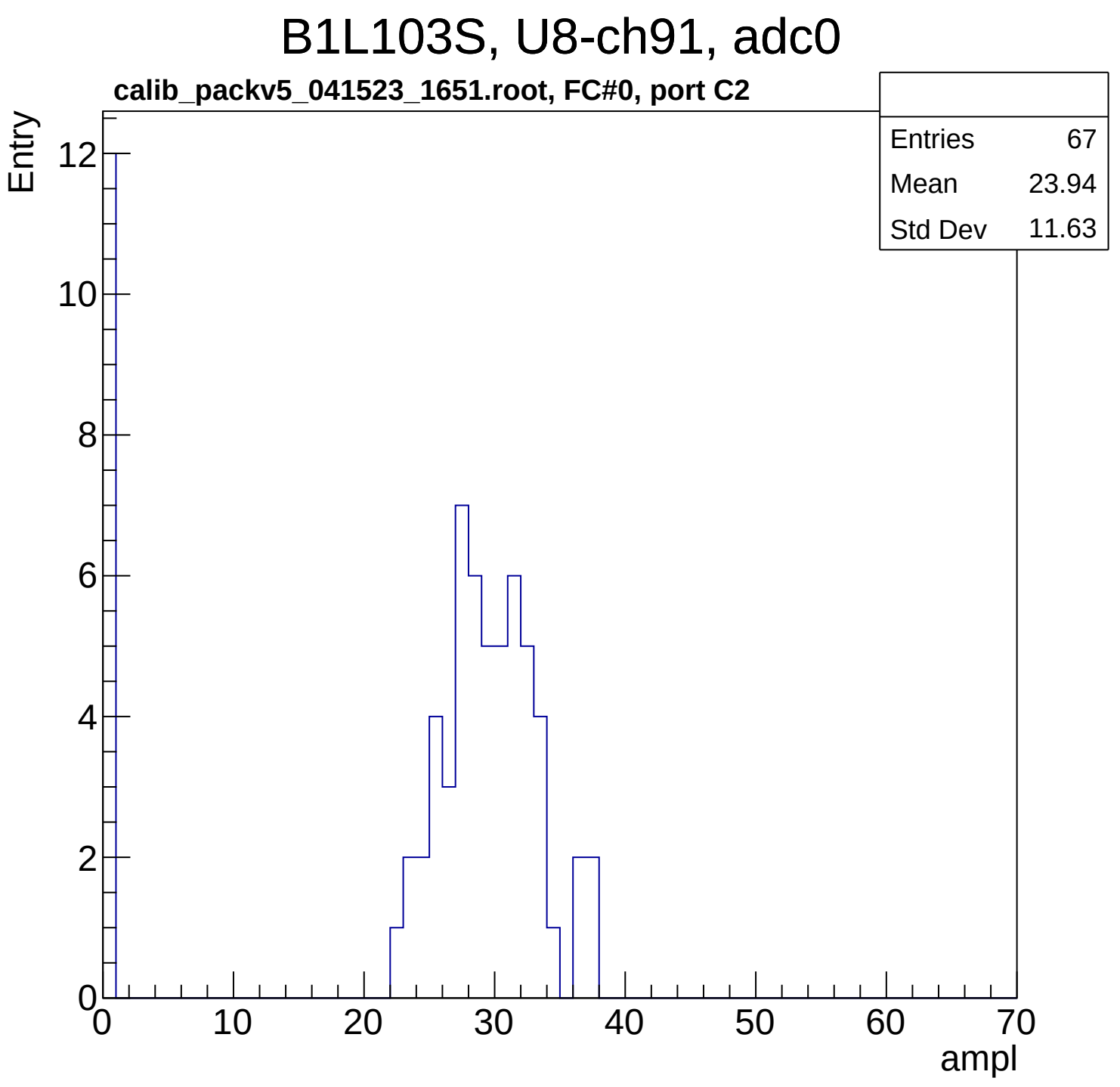
50
60
70
ampl


B1L103S, U8-ch91, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 23.94
Std Dev 11.63
Entry
0
2
4
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8
10
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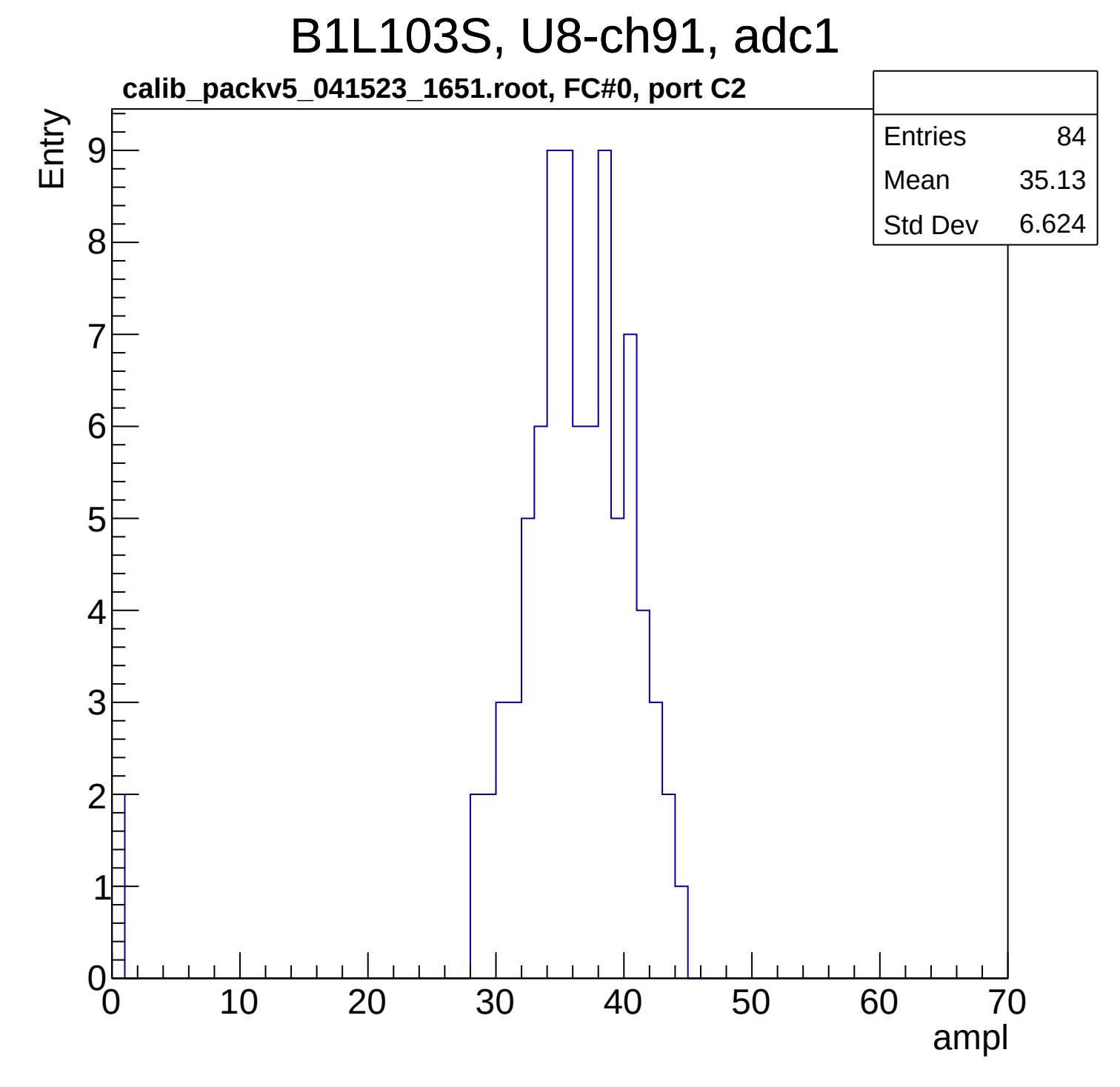
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch91, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 35.13
Std Dev 6.624
Entry
ampl
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3
4
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6
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8
9
0
10
20
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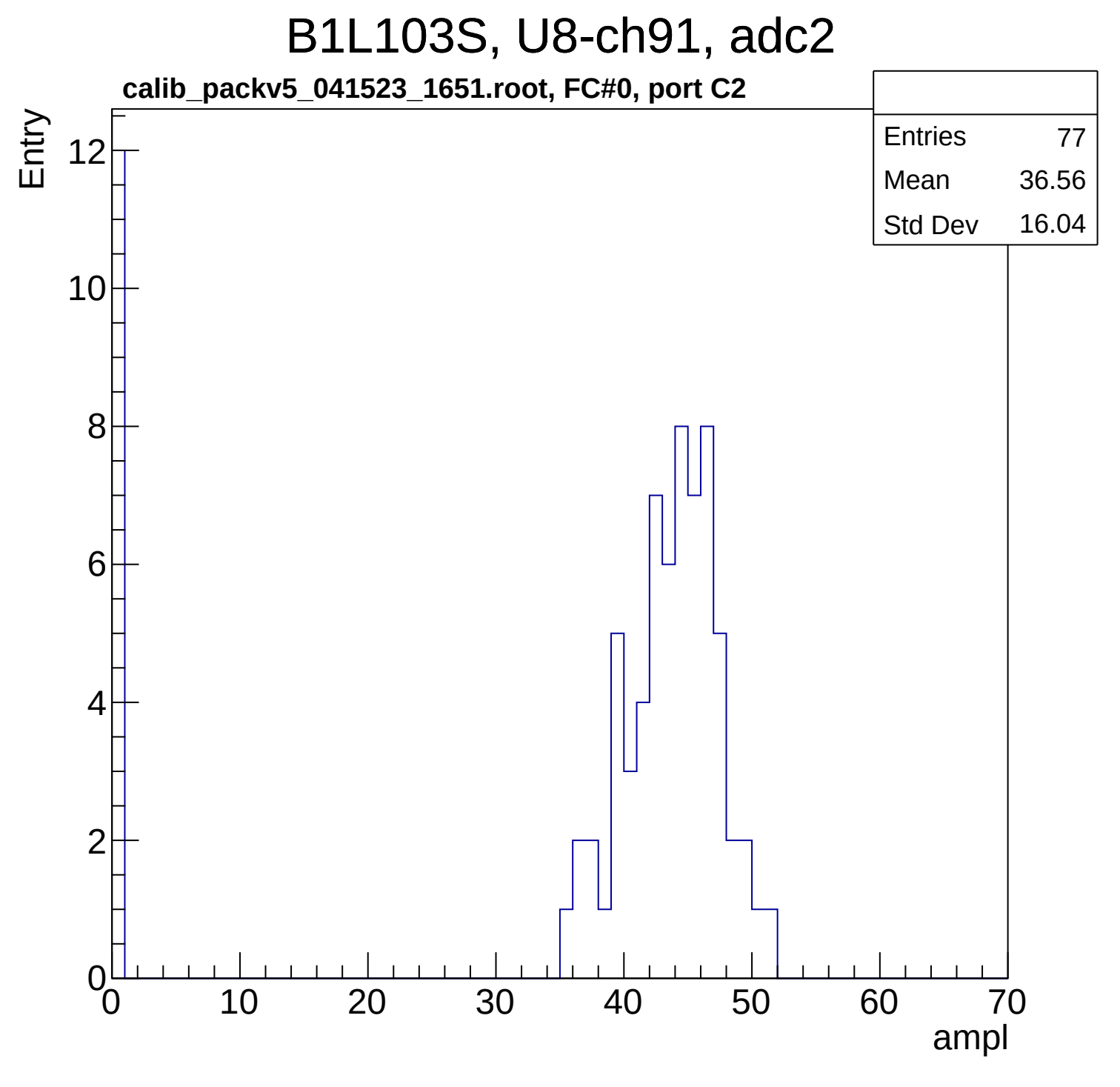
50
60
70


B1L103S, U8-ch91, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 36.56
Std Dev 16.04
Entry
0
2
4
6
8
10
12
0
10
20
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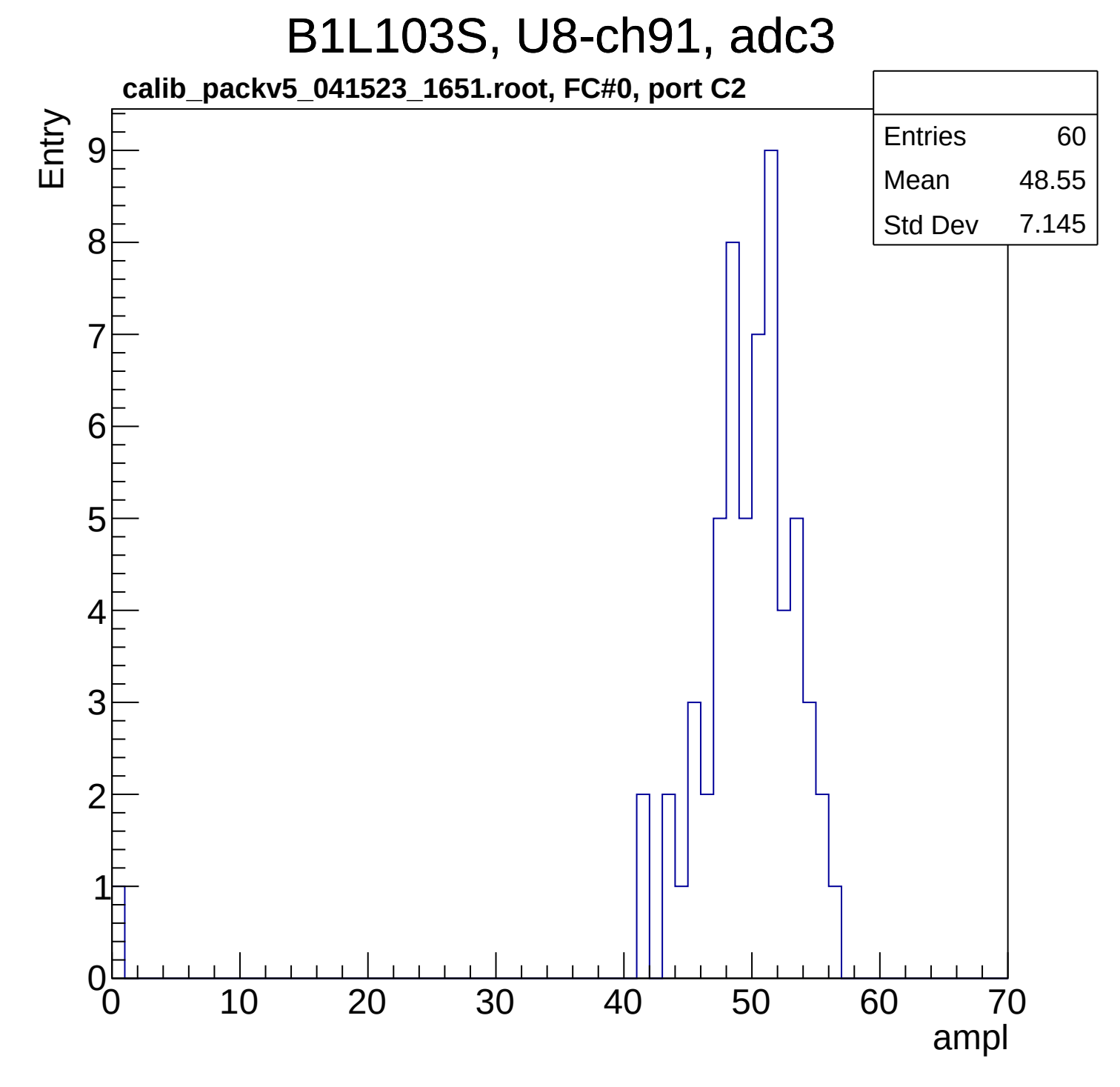
70
ampl


B1L103S, U8-ch91, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 48.55
Std Dev 7.145
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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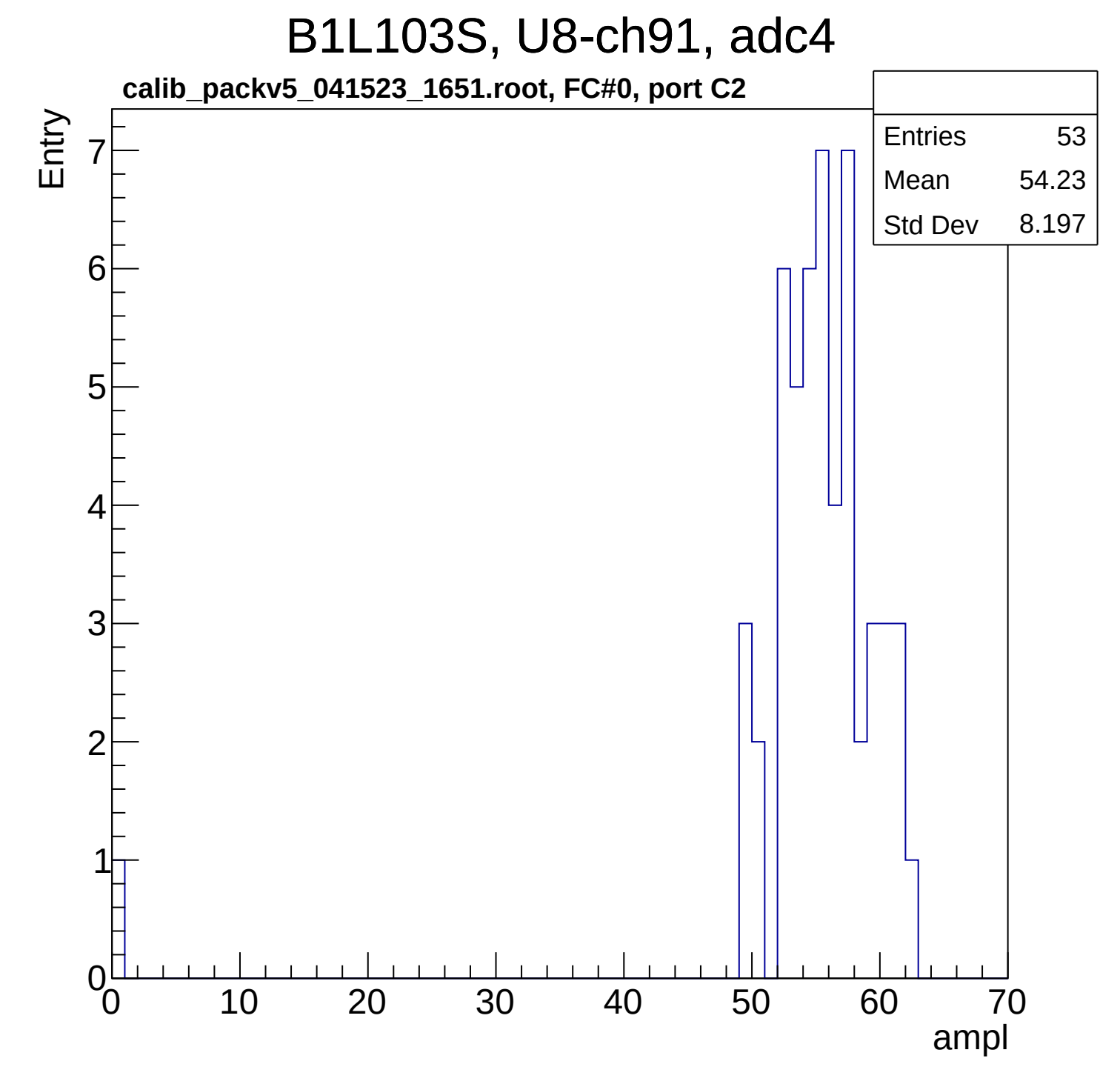
B1L103S, U8-ch91, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 54.23
Std Dev 8.197
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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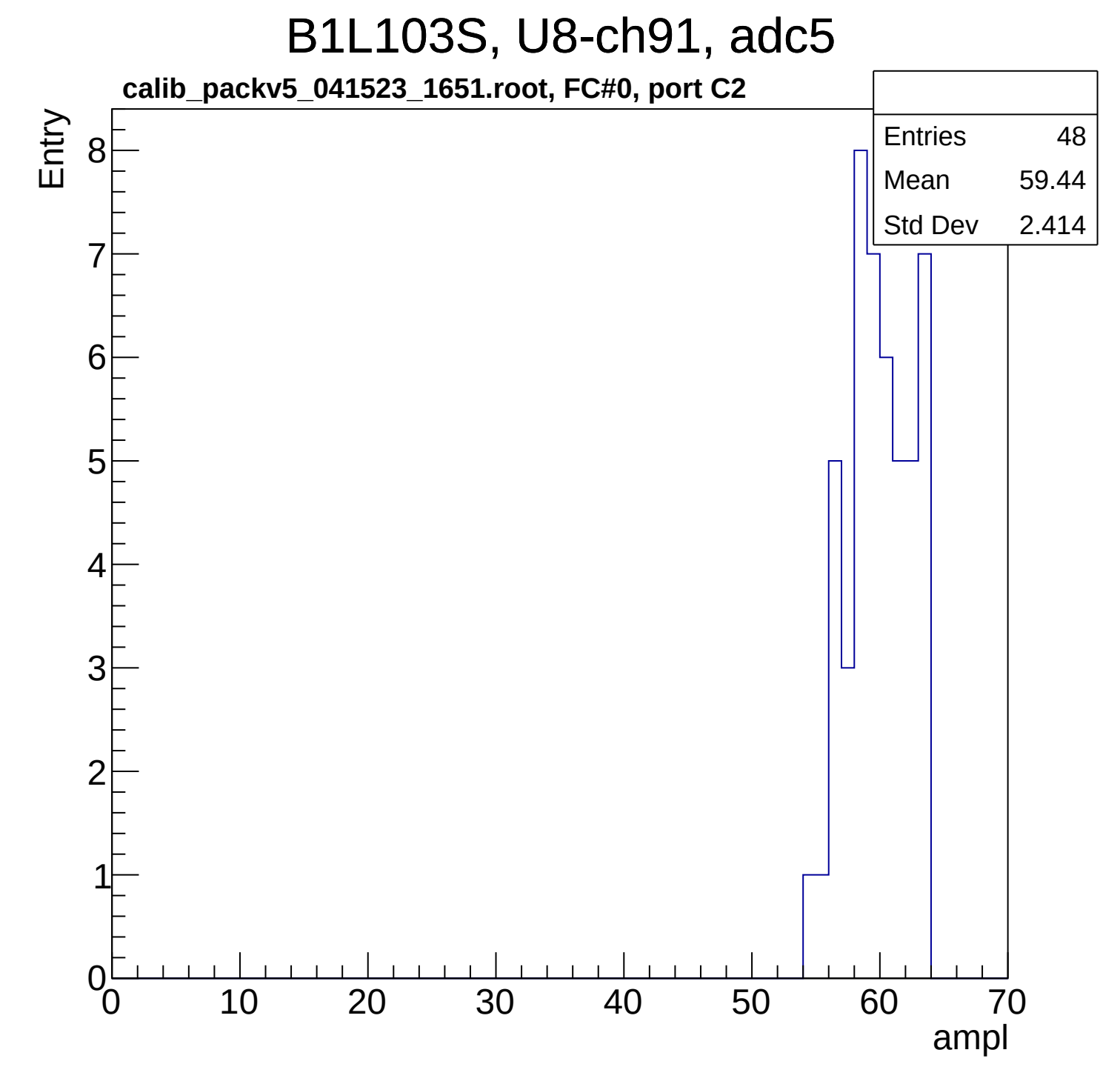
B1L103S, U8-ch91, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 59.44
Std Dev 2.414
Entry
ampl
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3
4
5
6
7
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0
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60
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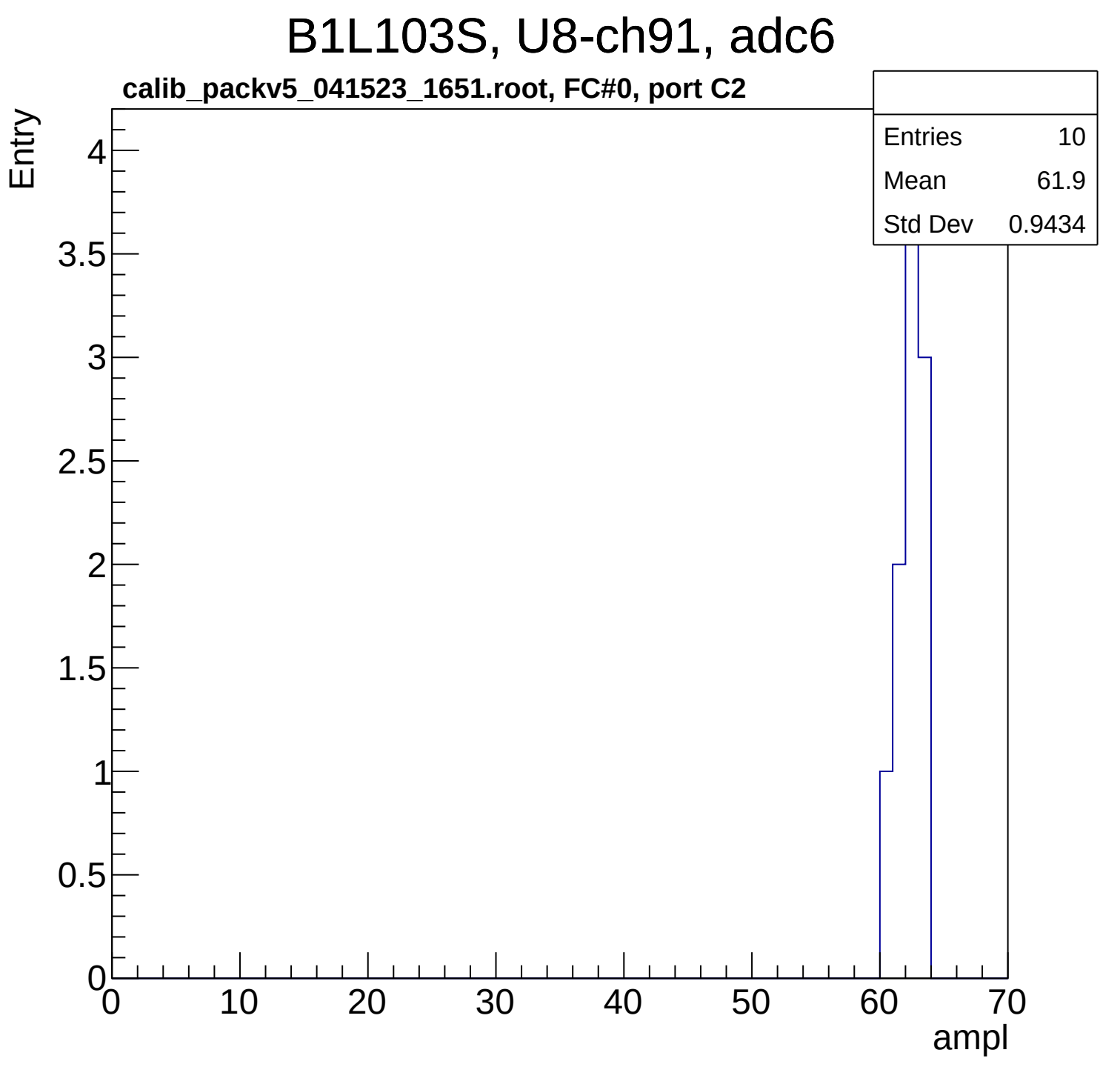
B1L103S, U8-ch91, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61.9
Std Dev 0.9434
Entry
ampl
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0.5
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1.5
2
2.5
3
3.5
4
0
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40
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60
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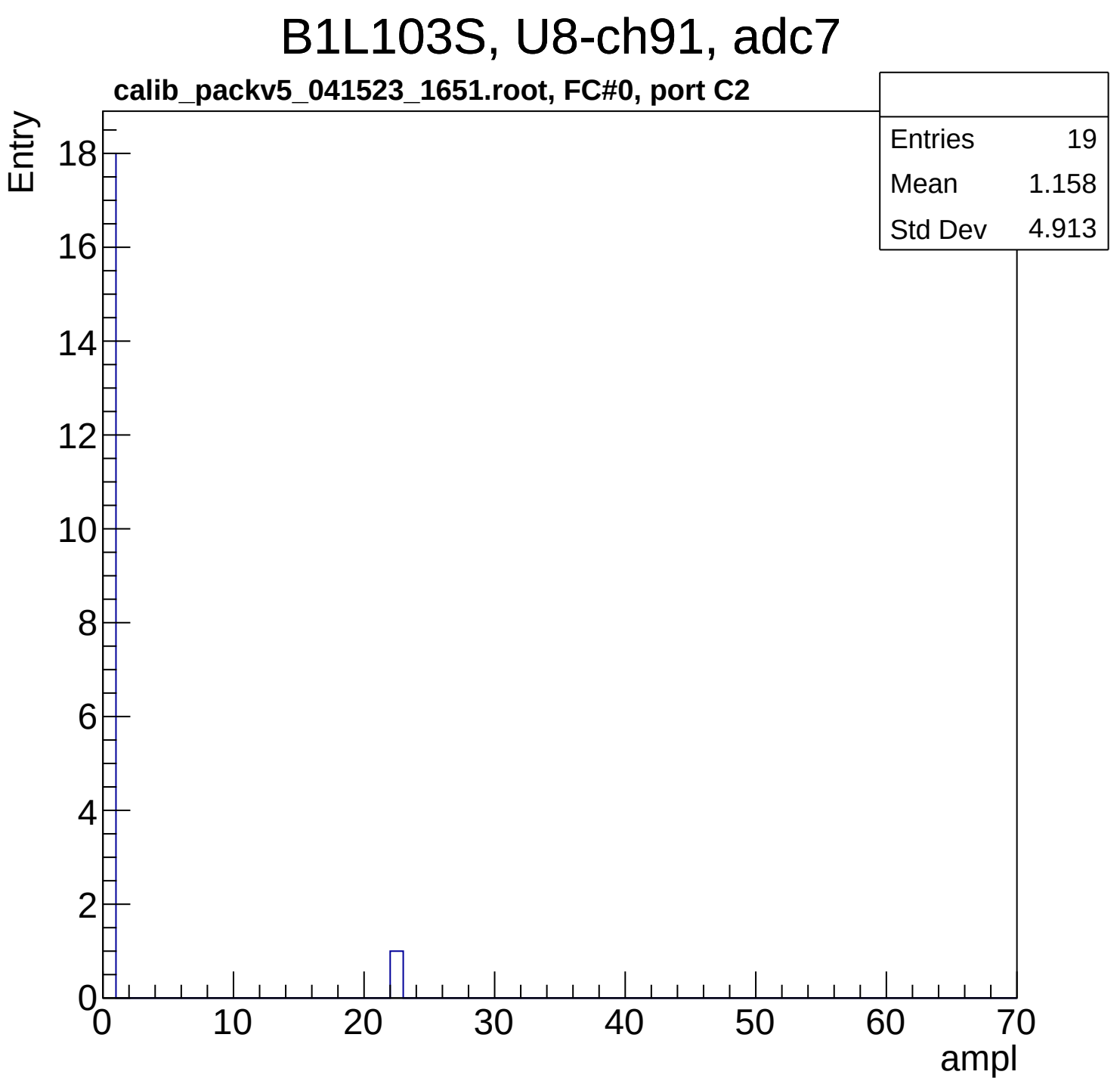
B1L103S, U8-ch91, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.158
Std Dev 4.913
Entry
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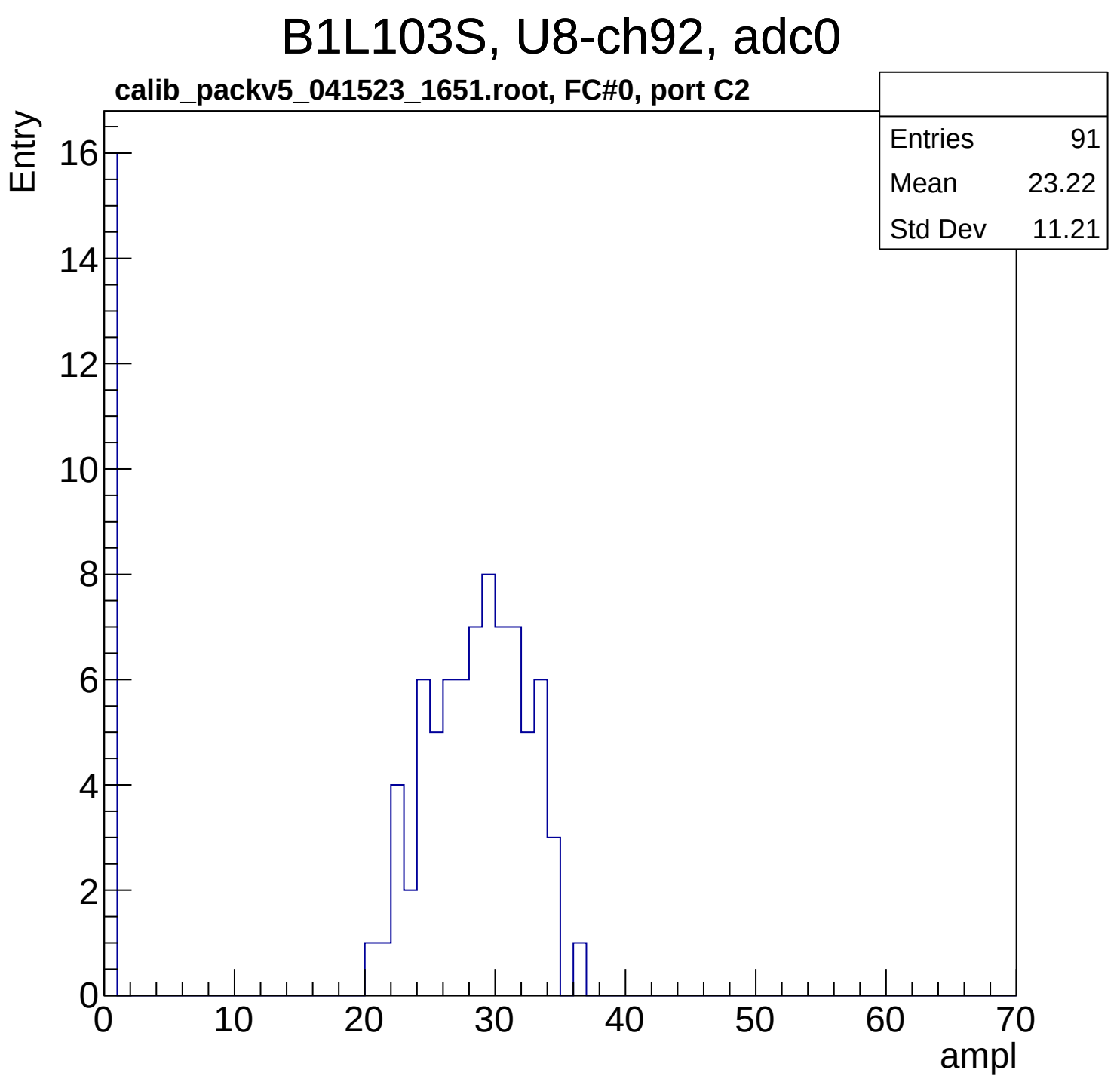
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch92, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 23.22
Std Dev 11.21
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
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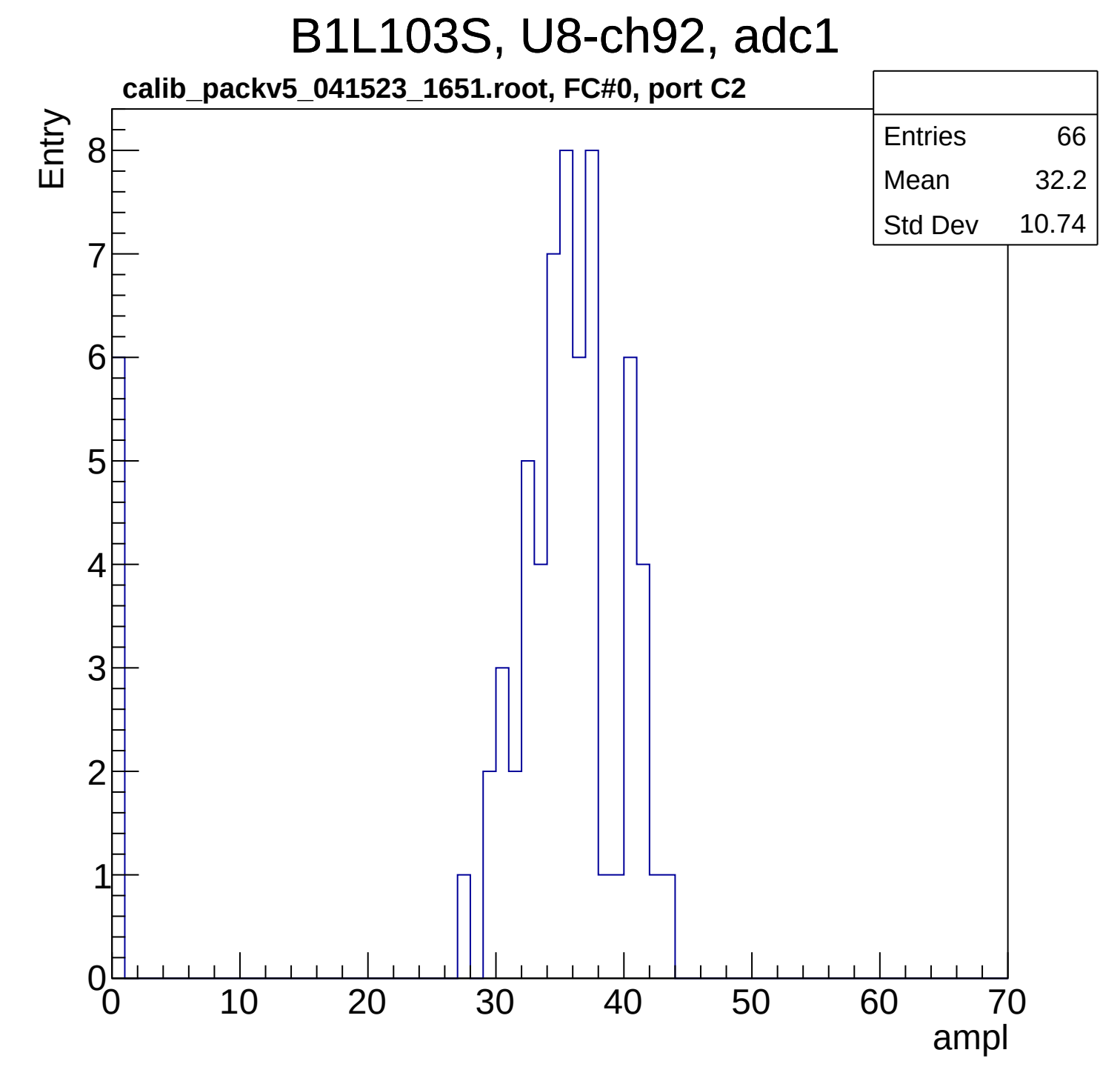
B1L103S, U8-ch92, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 32.2
Std Dev 10.74
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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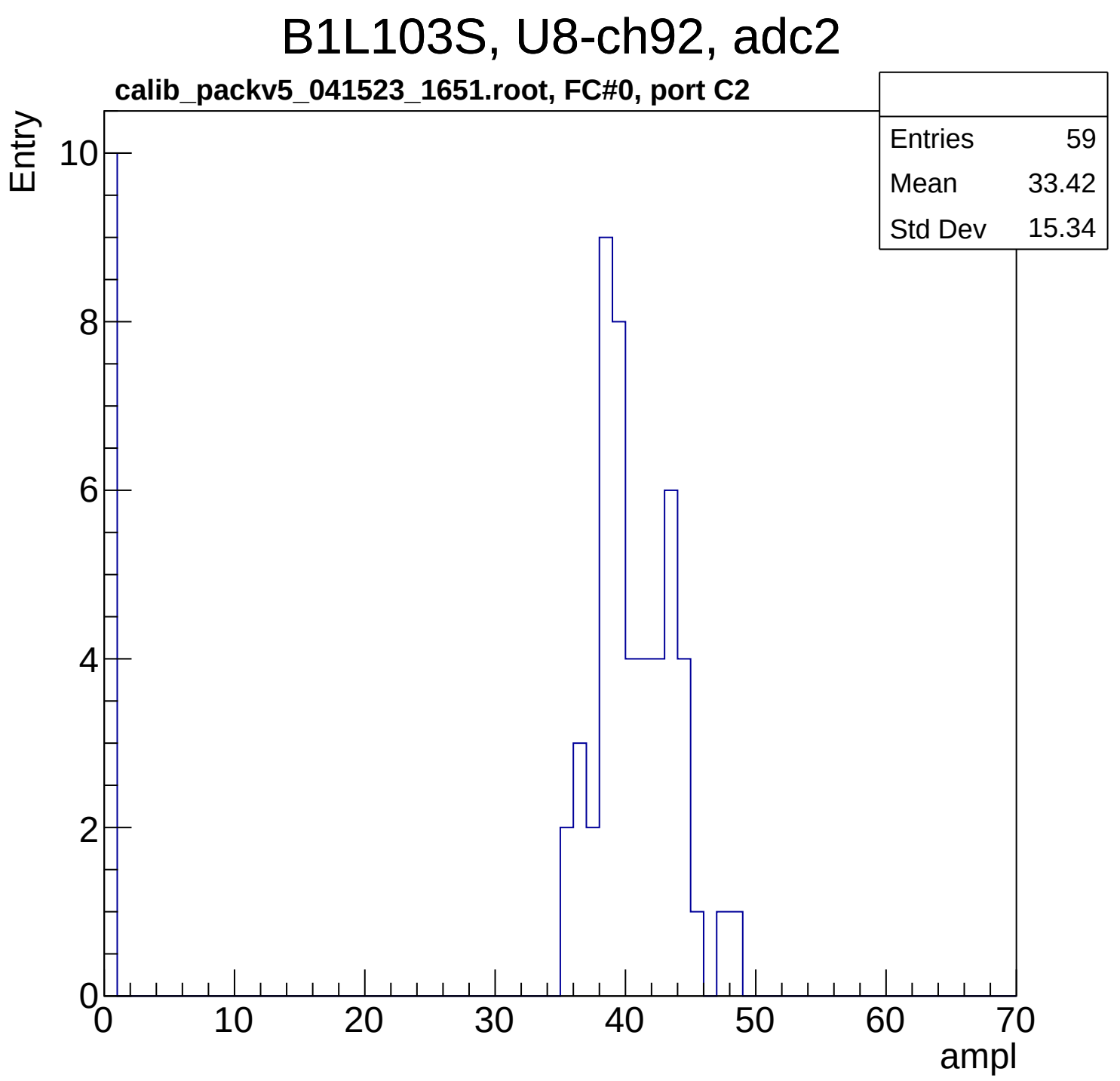
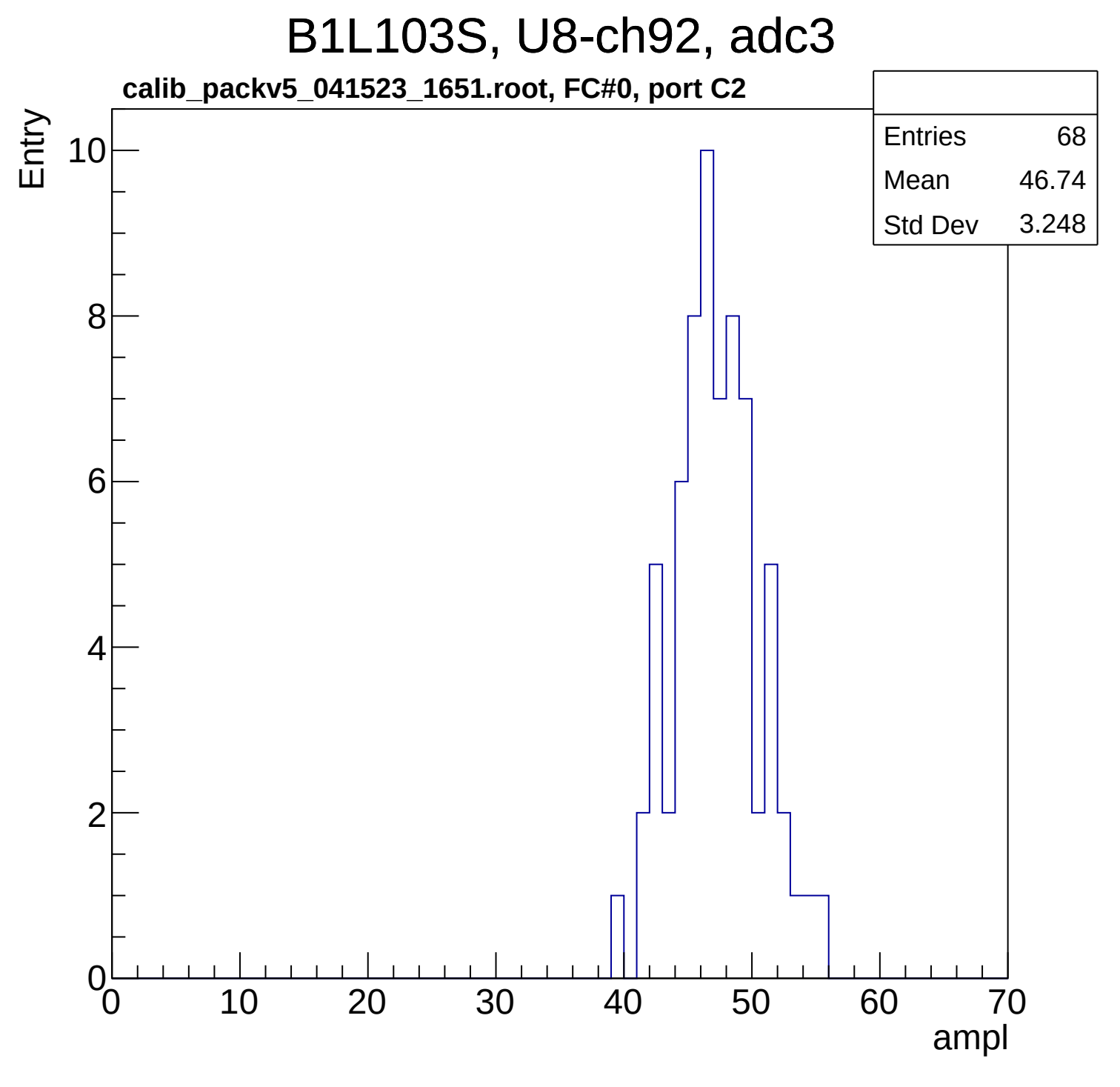
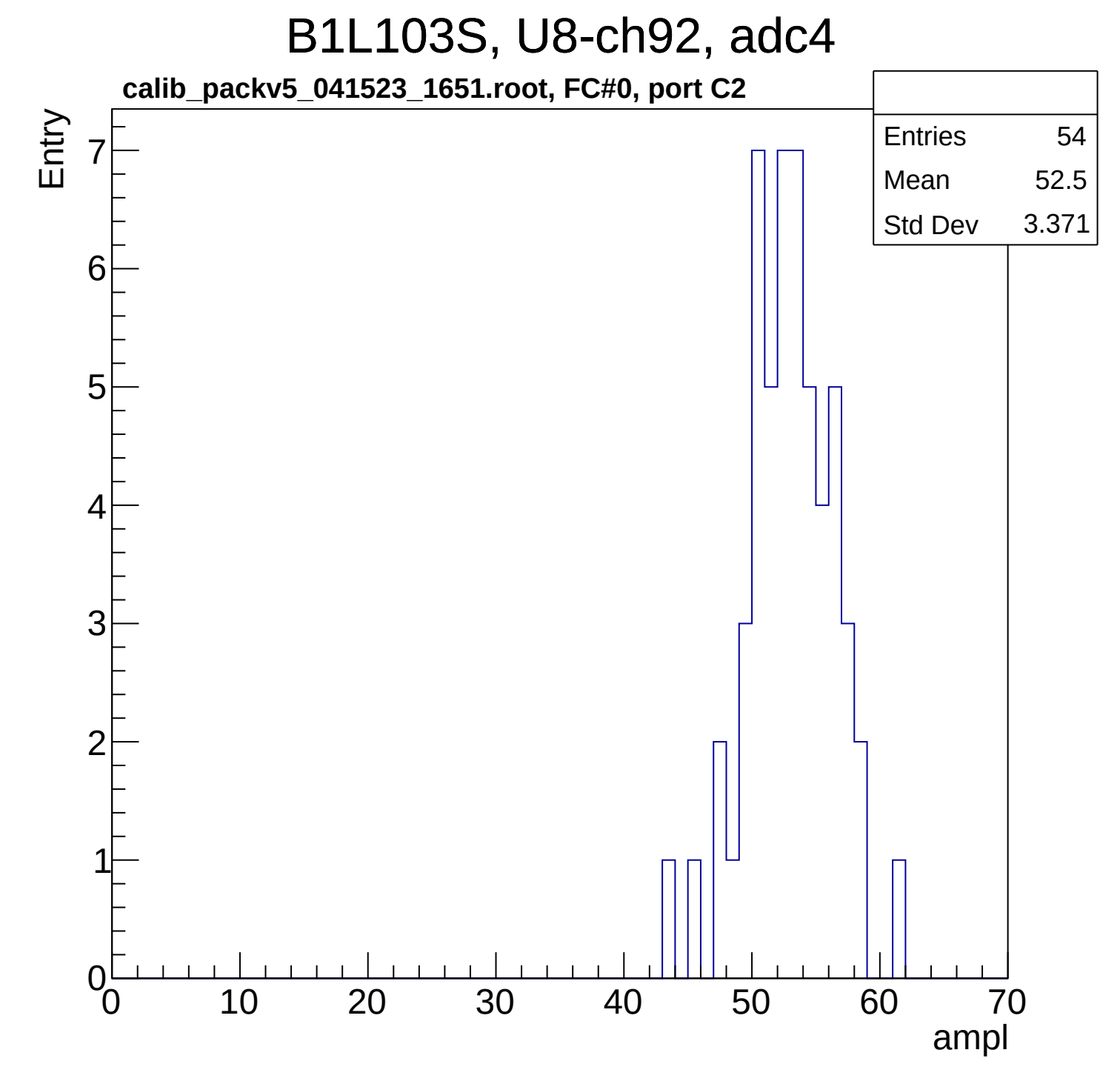
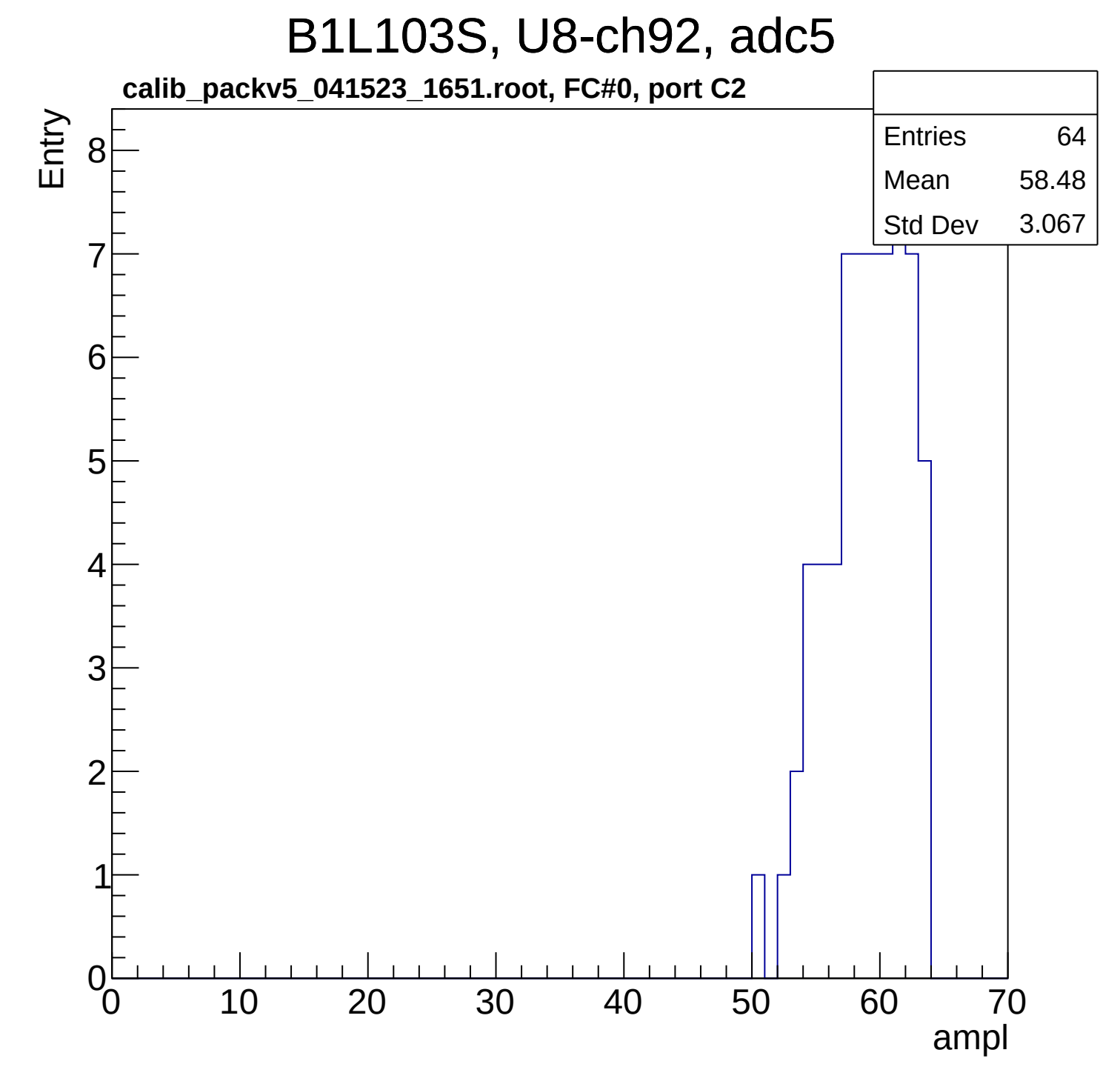

B1L103S, U8-ch92, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 33.42
Std Dev 15.34
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U8-ch92, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 46.74
Std Dev 3.248
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U8-ch92, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 52.5
Std Dev 3.371
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U8-ch92, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 58.48
Std Dev 3.067
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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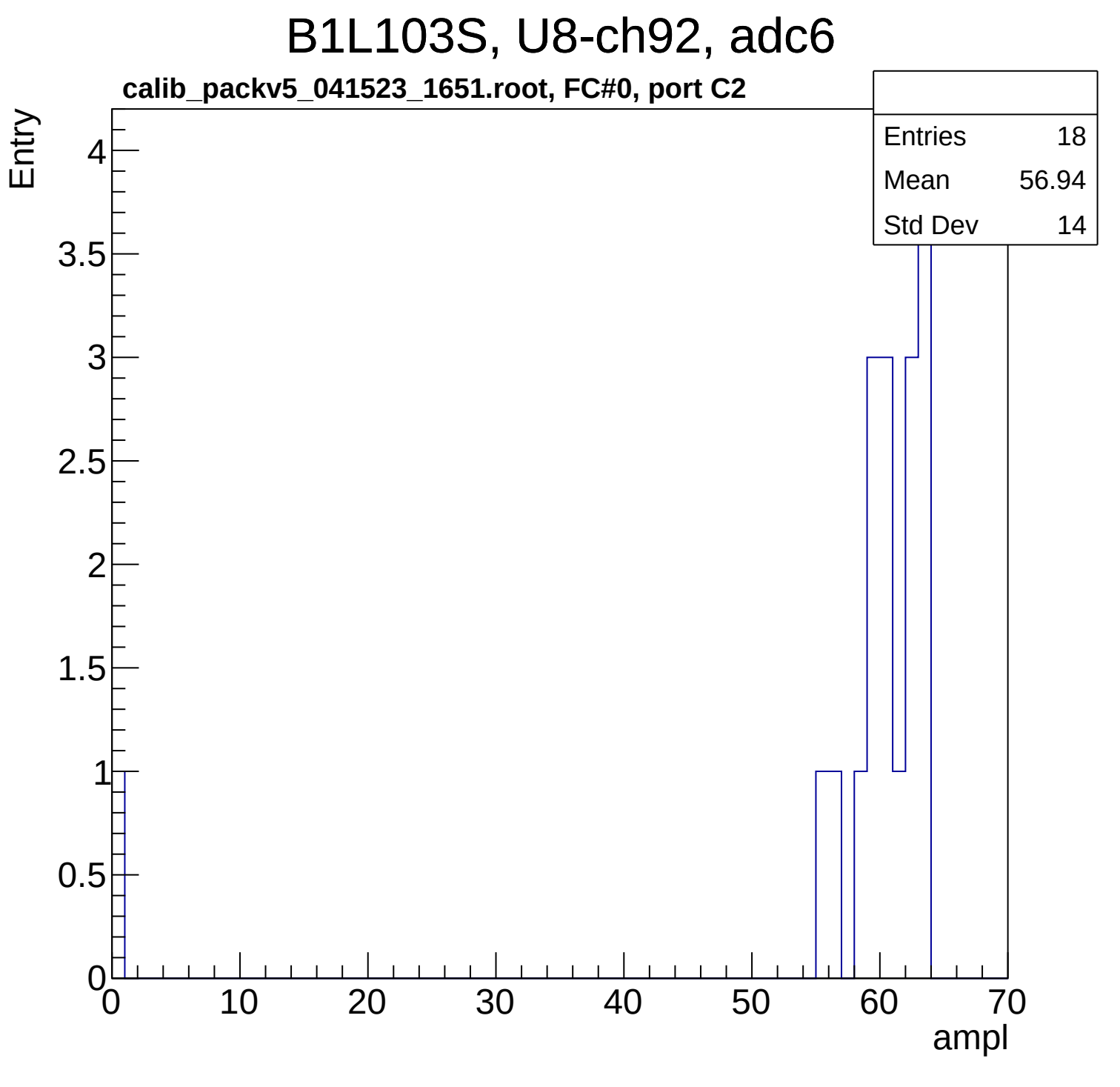
B1L103S, U8-ch92, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 56.94
Std Dev 14
Entry
ampl
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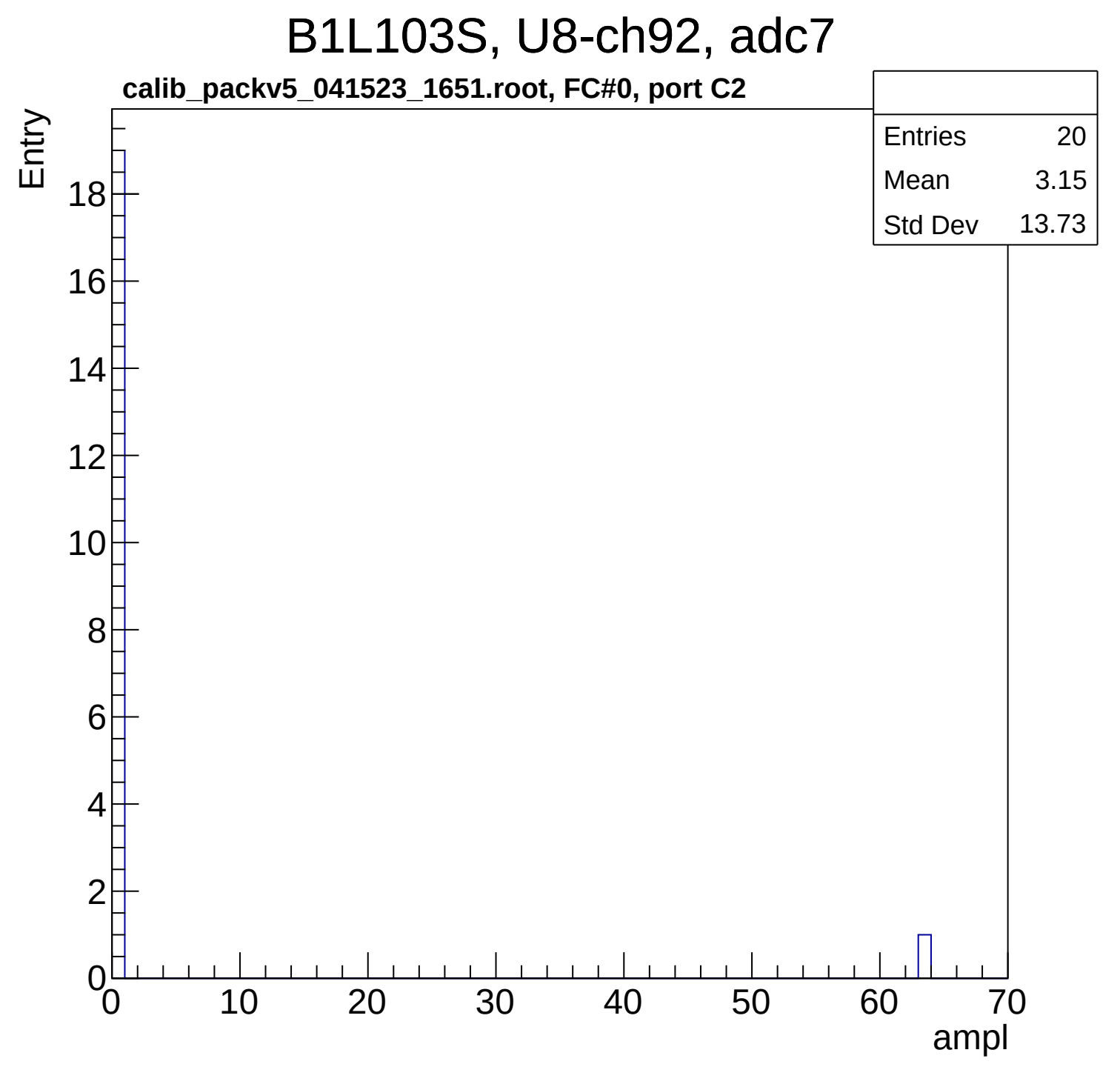
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U8-ch92, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
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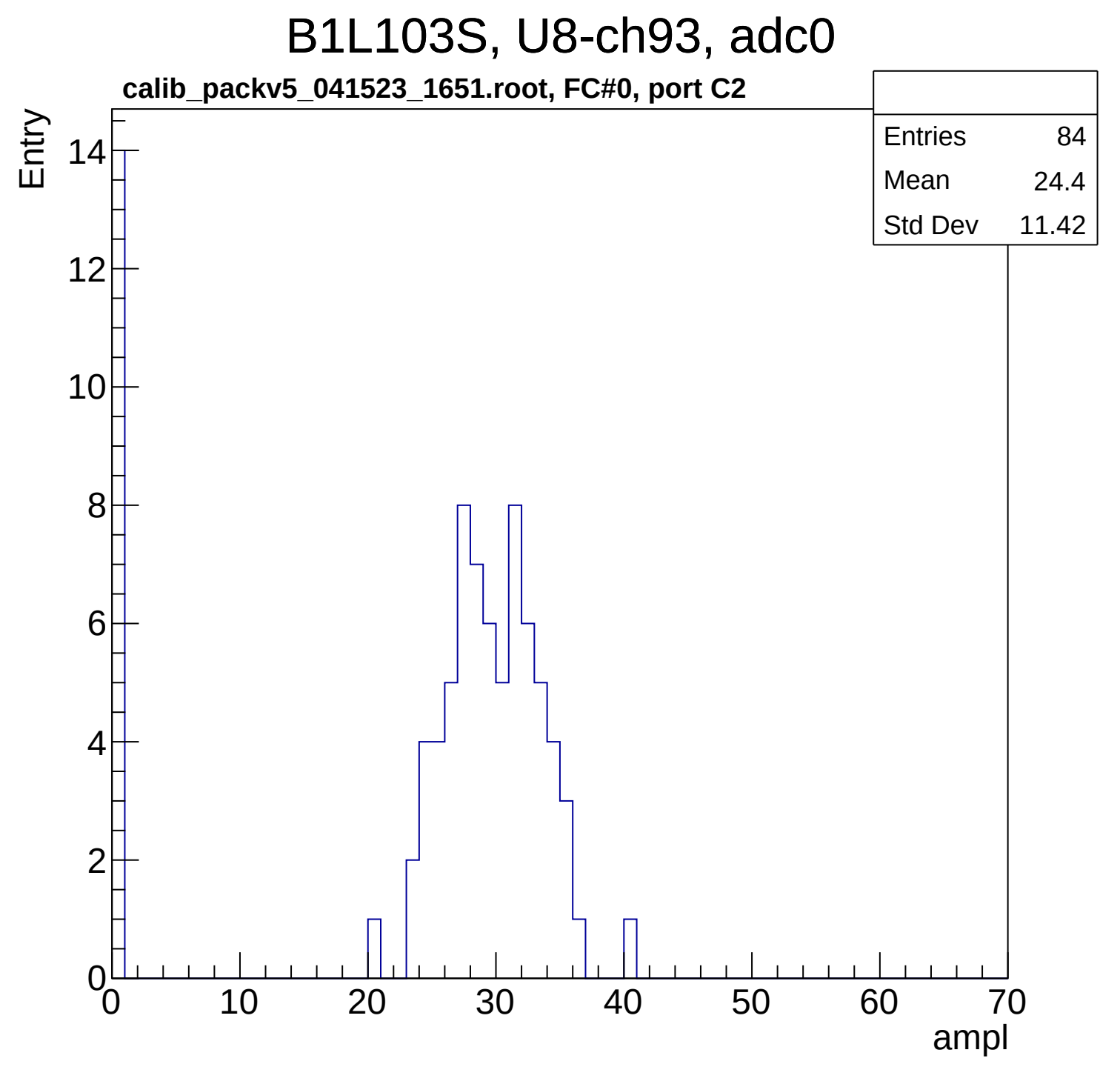
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch93, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 24.4
Std Dev 11.42
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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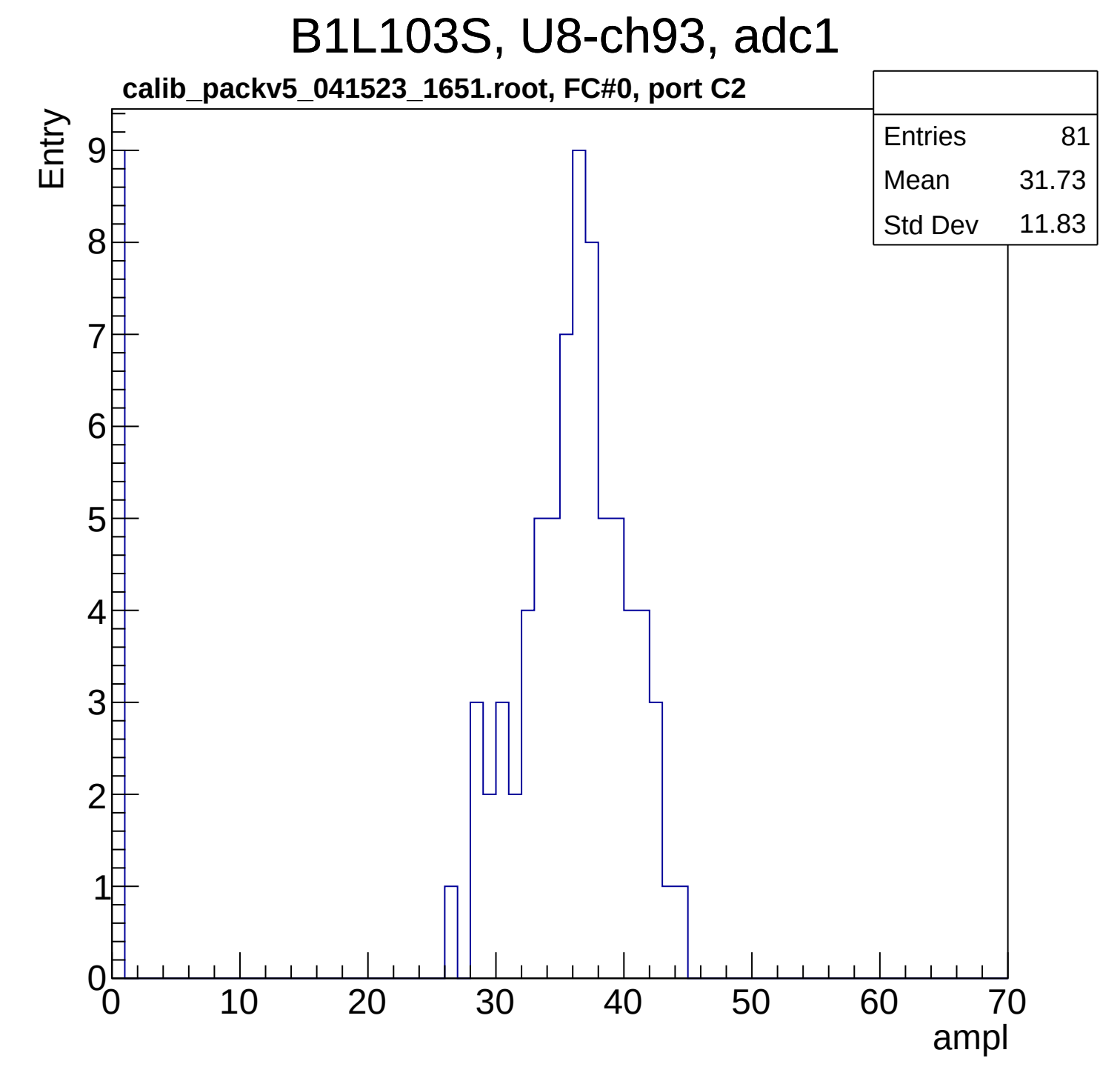
B1L103S, U8-ch93, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 31.73
Std Dev 11.83
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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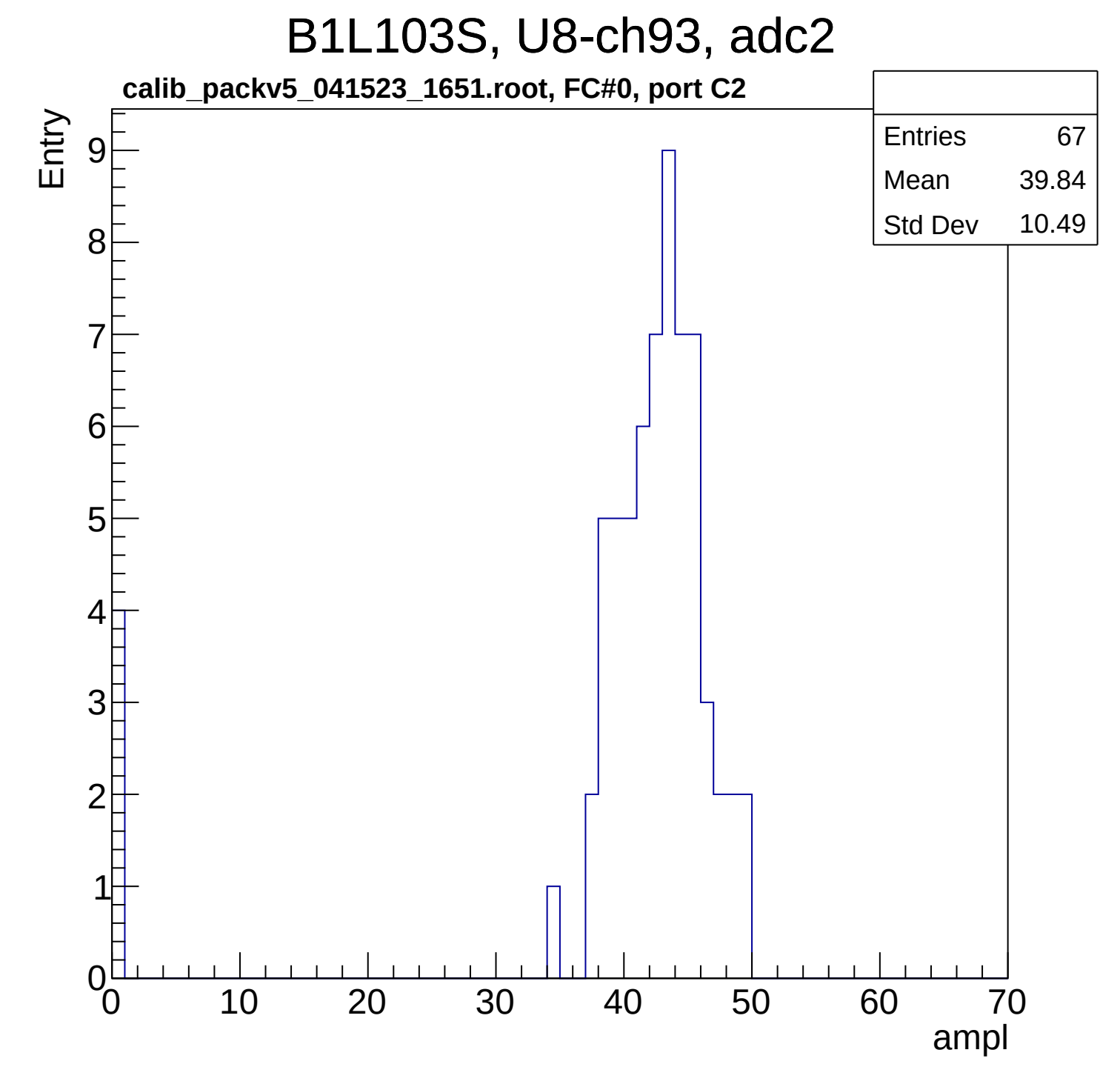
B1L103S, U8-ch93, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 39.84
Std Dev 10.49
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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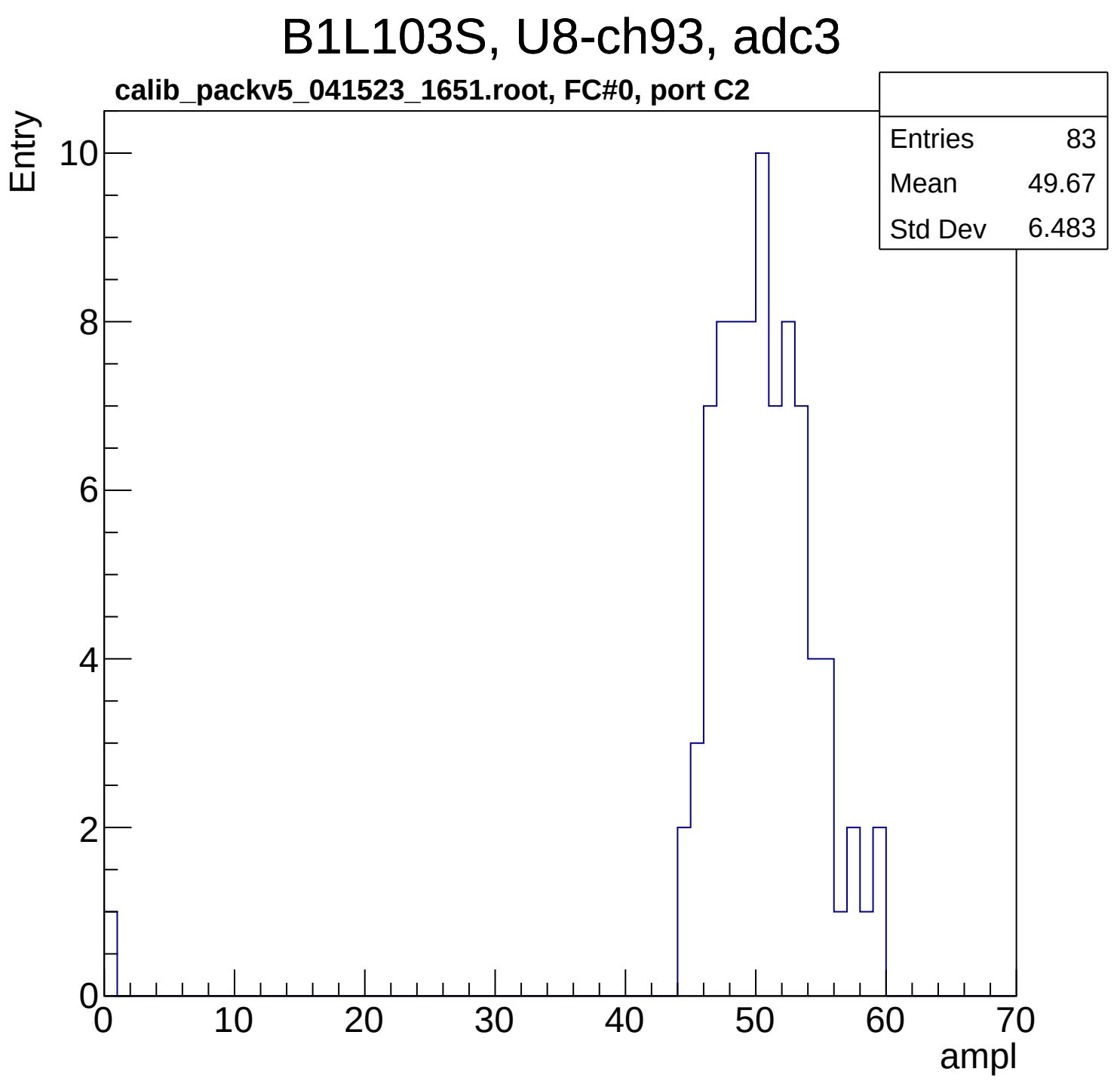
B1L103S, U8-ch93, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 49.67
Std Dev 6.483
Entry
ampl
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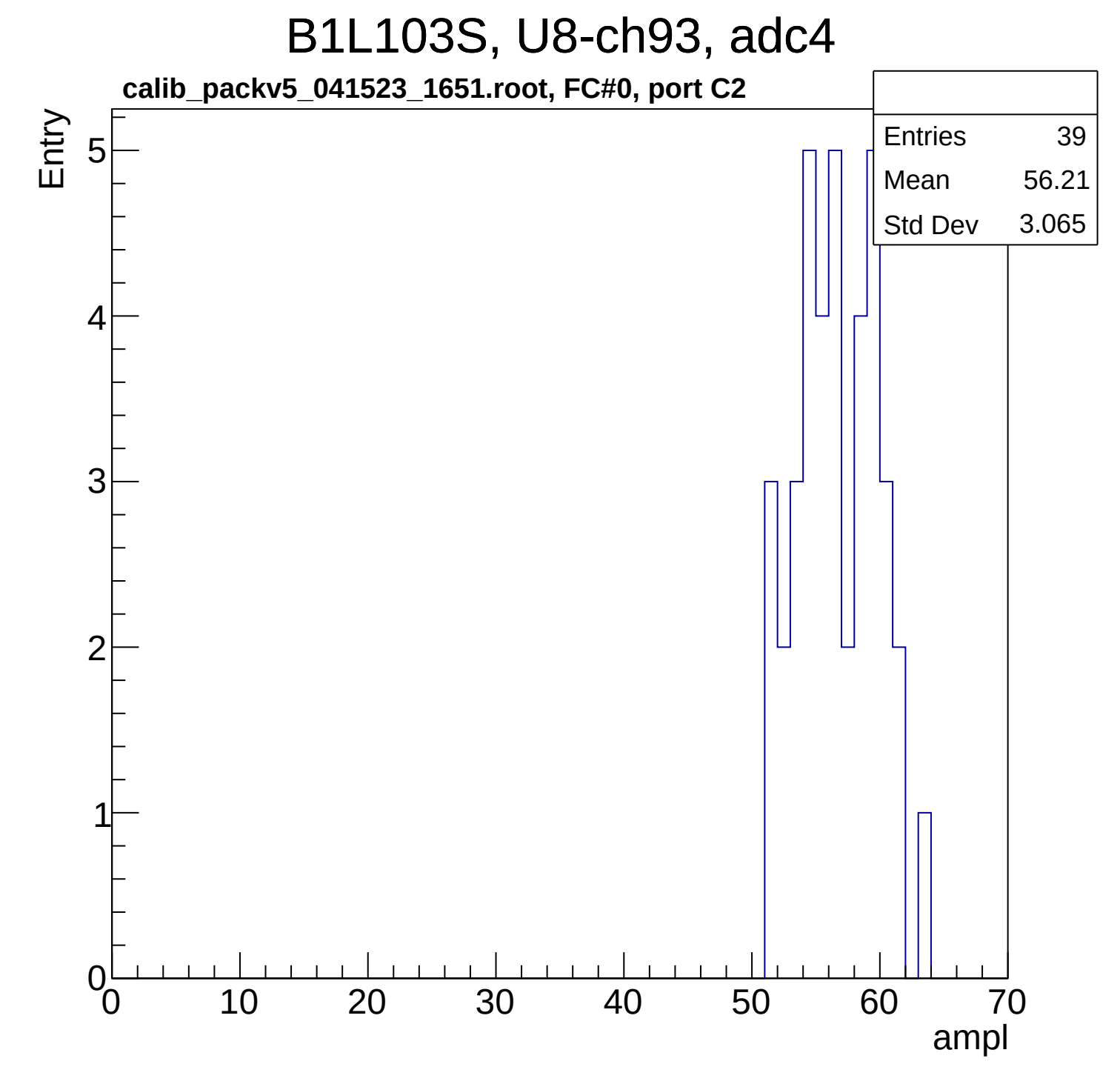
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U8-ch93, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 56.21
Std Dev 3.065
Entry
ampl
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2
3
4
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0
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20
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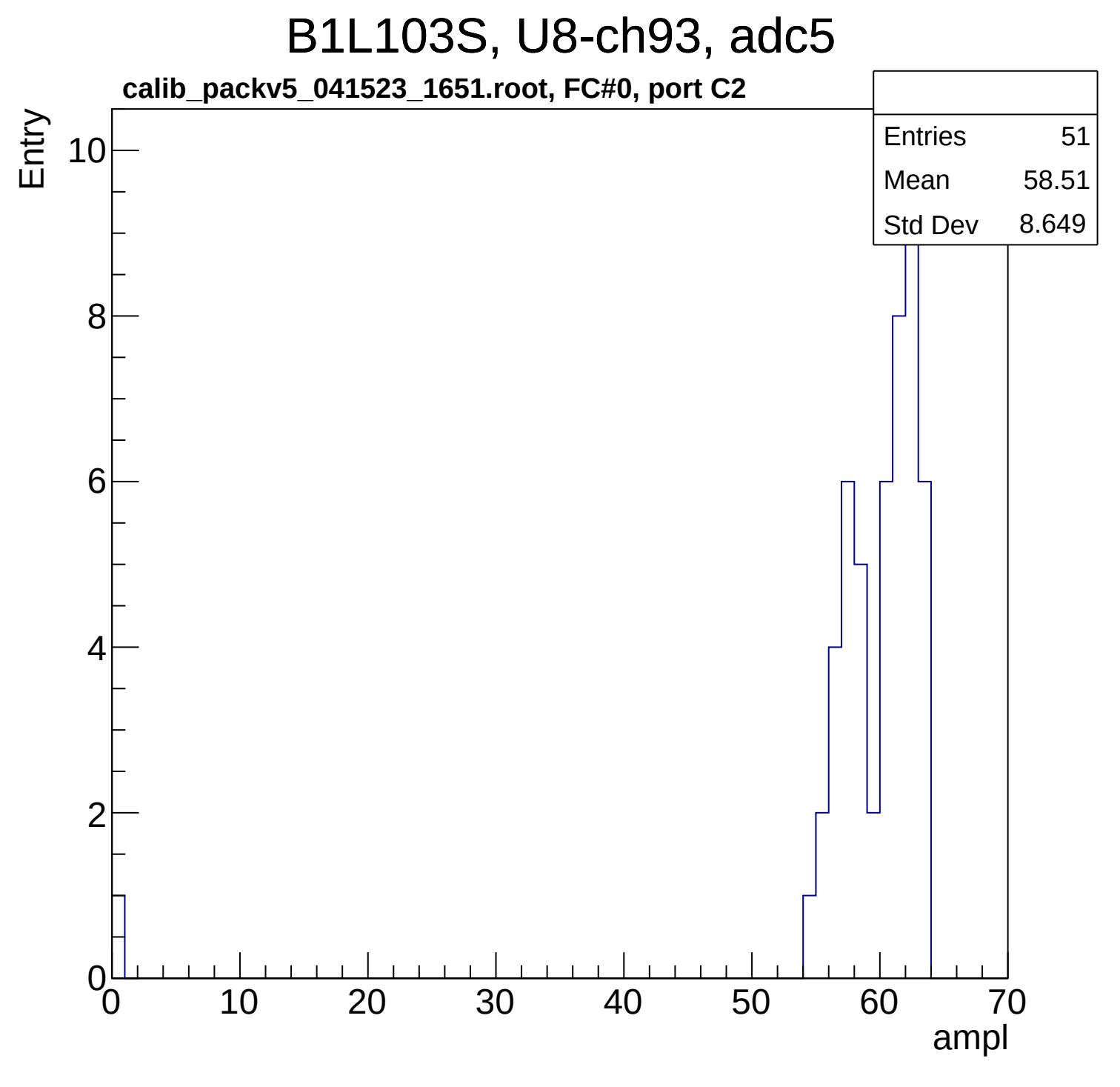
40
50
60
70


B1L103S, U8-ch93, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 58.51
Std Dev 8.649
Entry
ampl
0
2
4
6
8
10
0
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60
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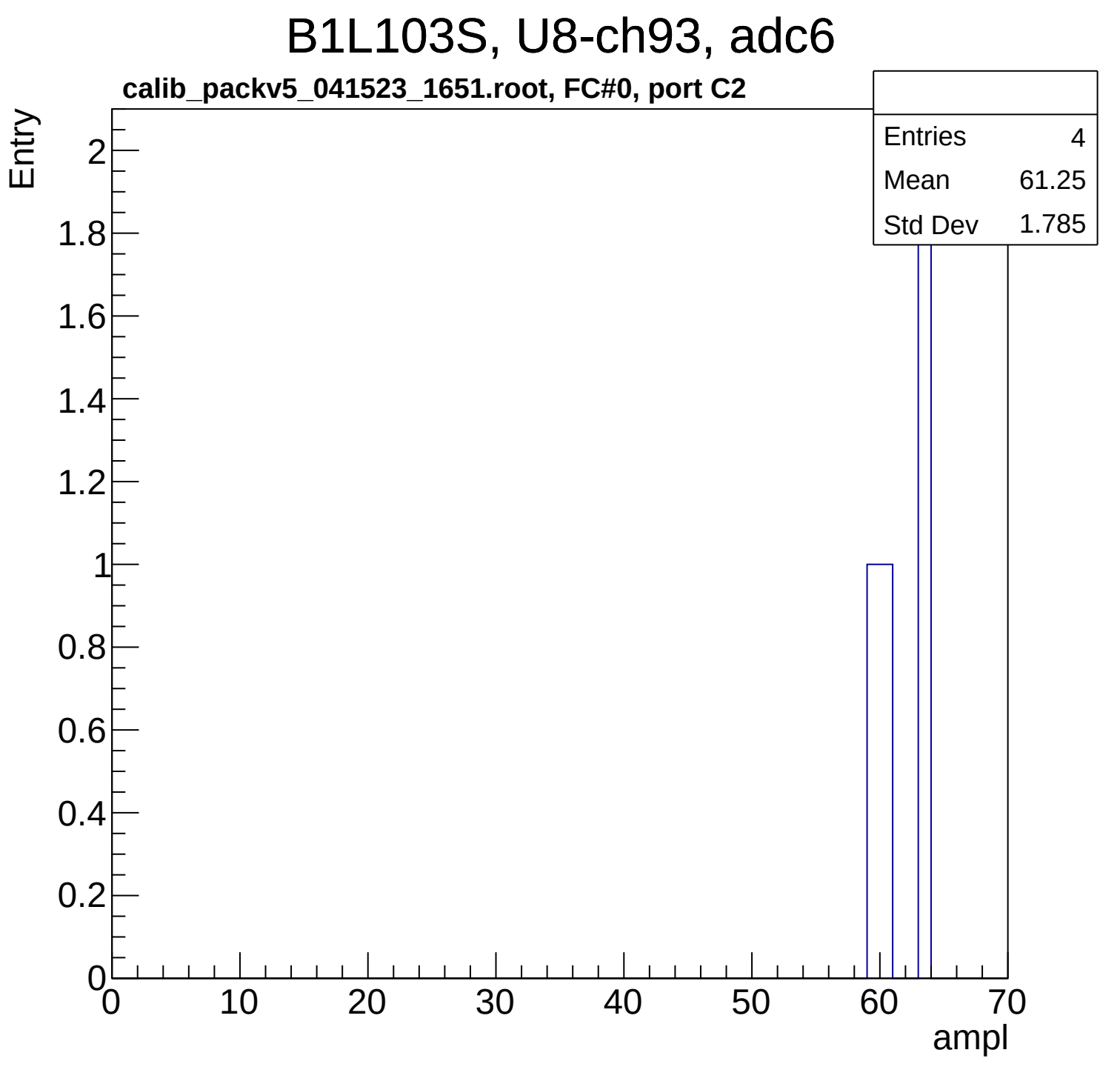
B1L103S, U8-ch93, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 61.25
Std Dev 1.785
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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50
60
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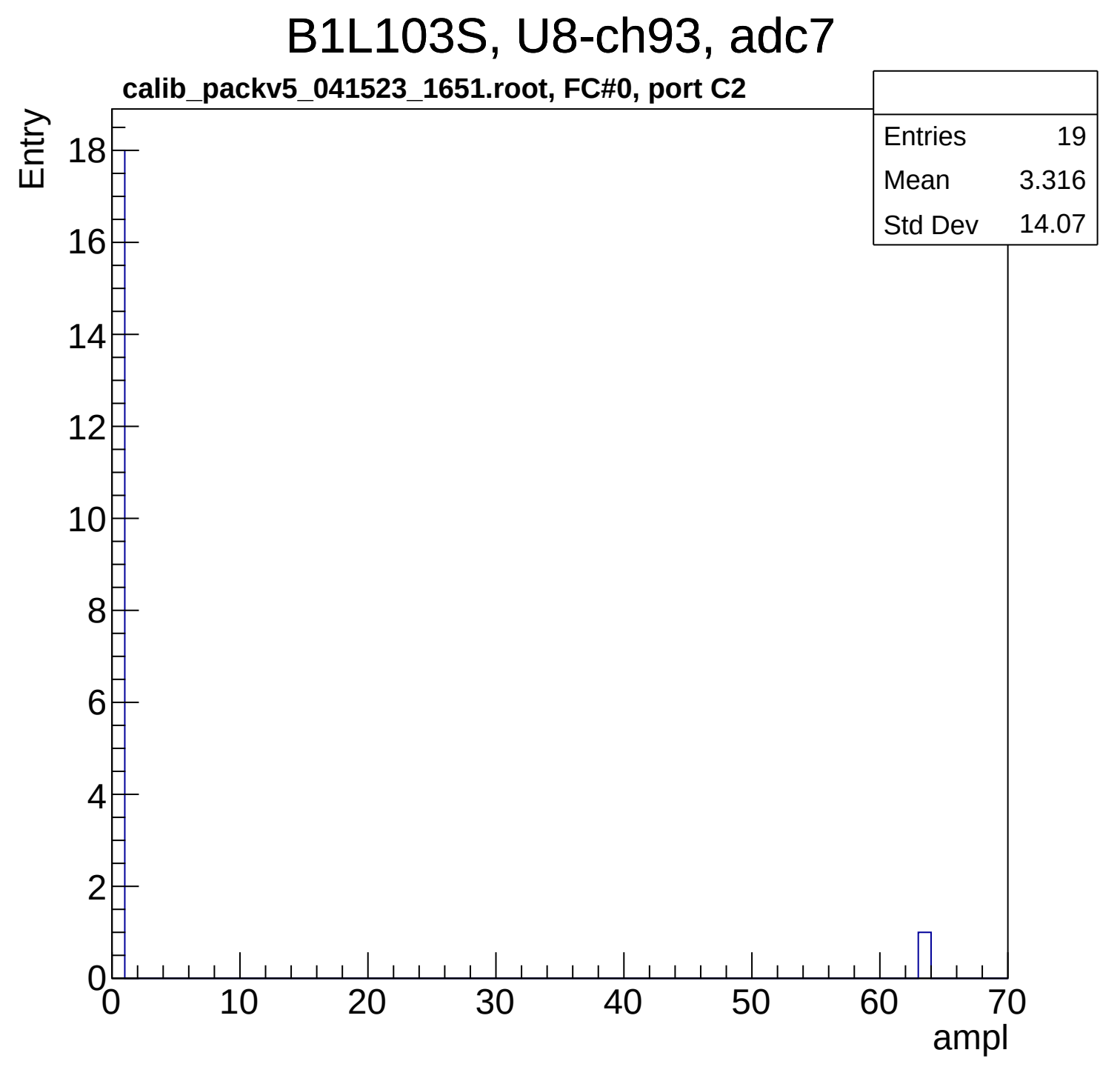
B1L103S, U8-ch93, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.316
Std Dev 14.07
Entry
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6
8
10
12
14
16
18
0
10
20
30
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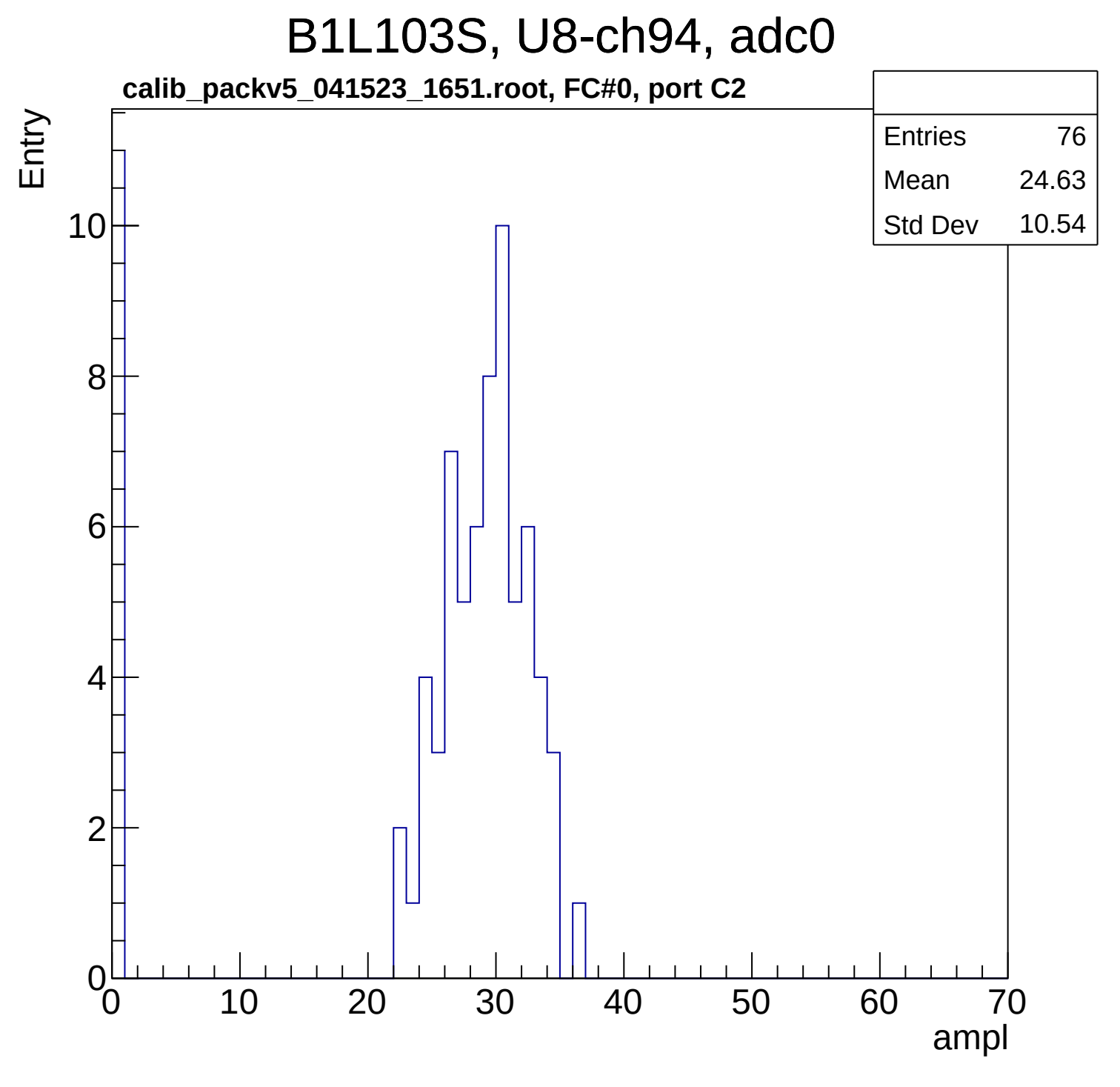
50
60
70
ampl


B1L103S, U8-ch94, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 24.63
Std Dev 10.54
Entry
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4
6
8
10
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30
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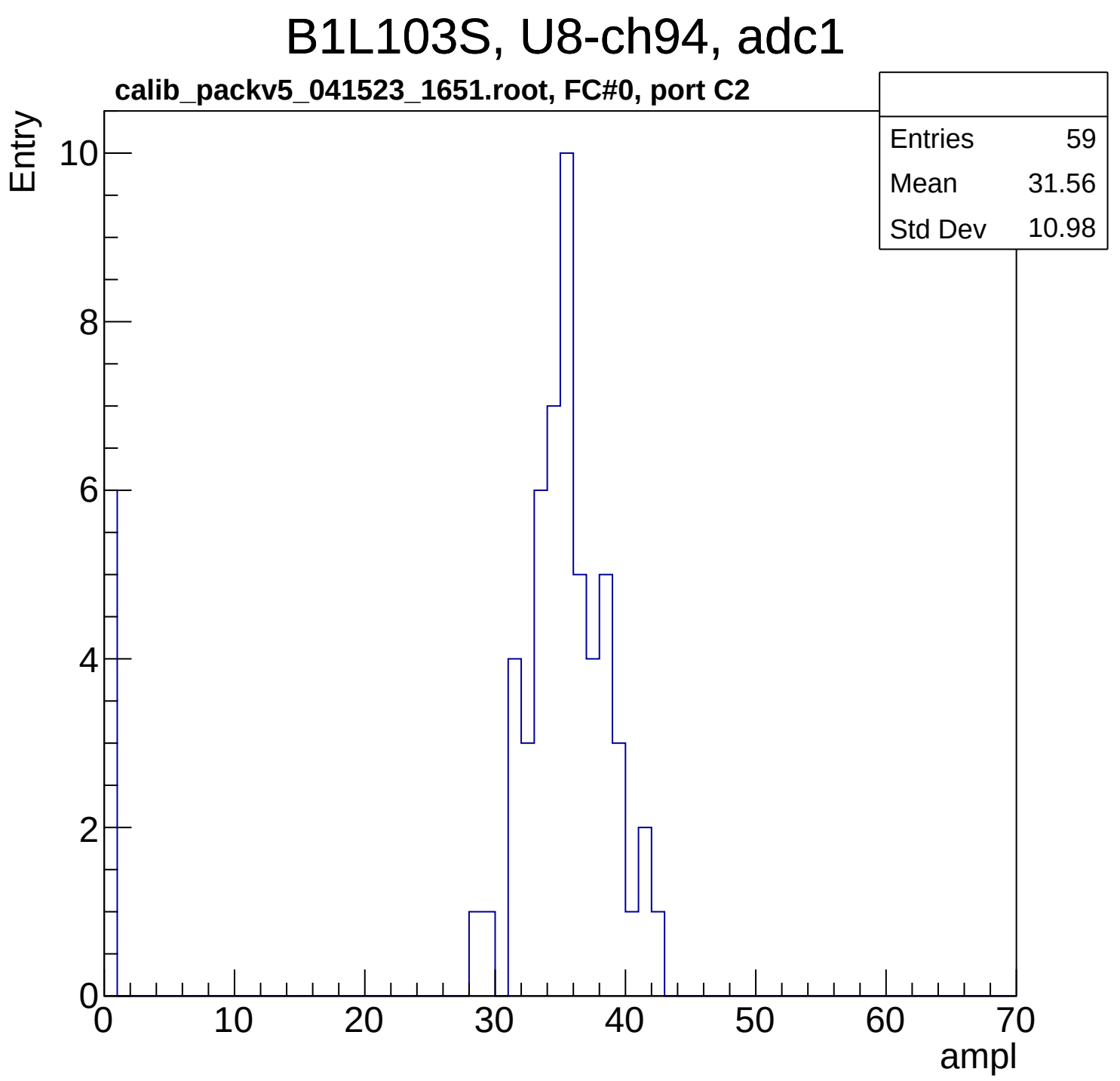
50
60
70
ampl


B1L103S, U8-ch94, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 31.56
Std Dev 10.98
Entry
0
2
4
6
8
10
0
10
20
30
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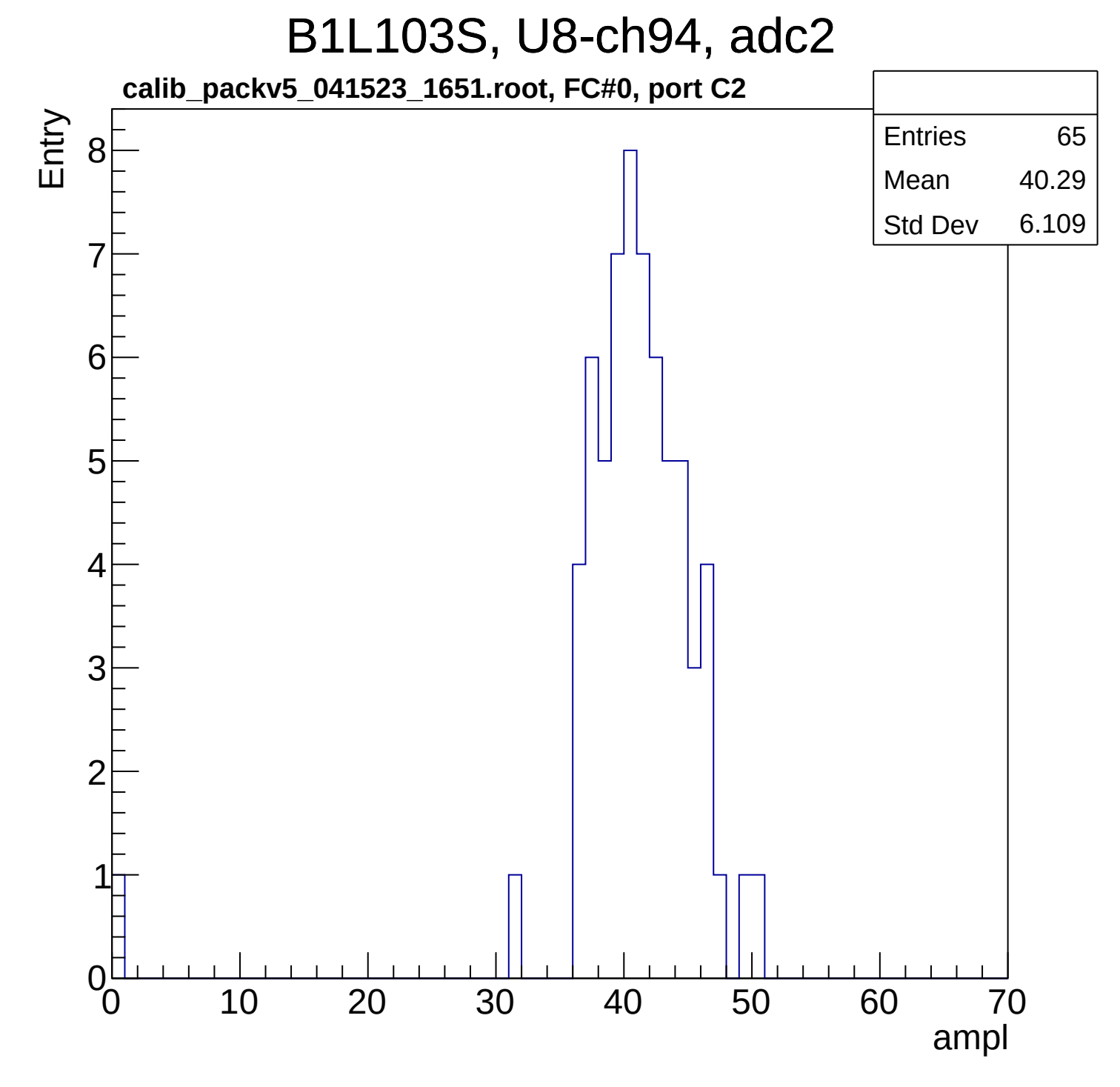
50
60
70
ampl


B1L103S, U8-ch94, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 40.29
Std Dev 6.109
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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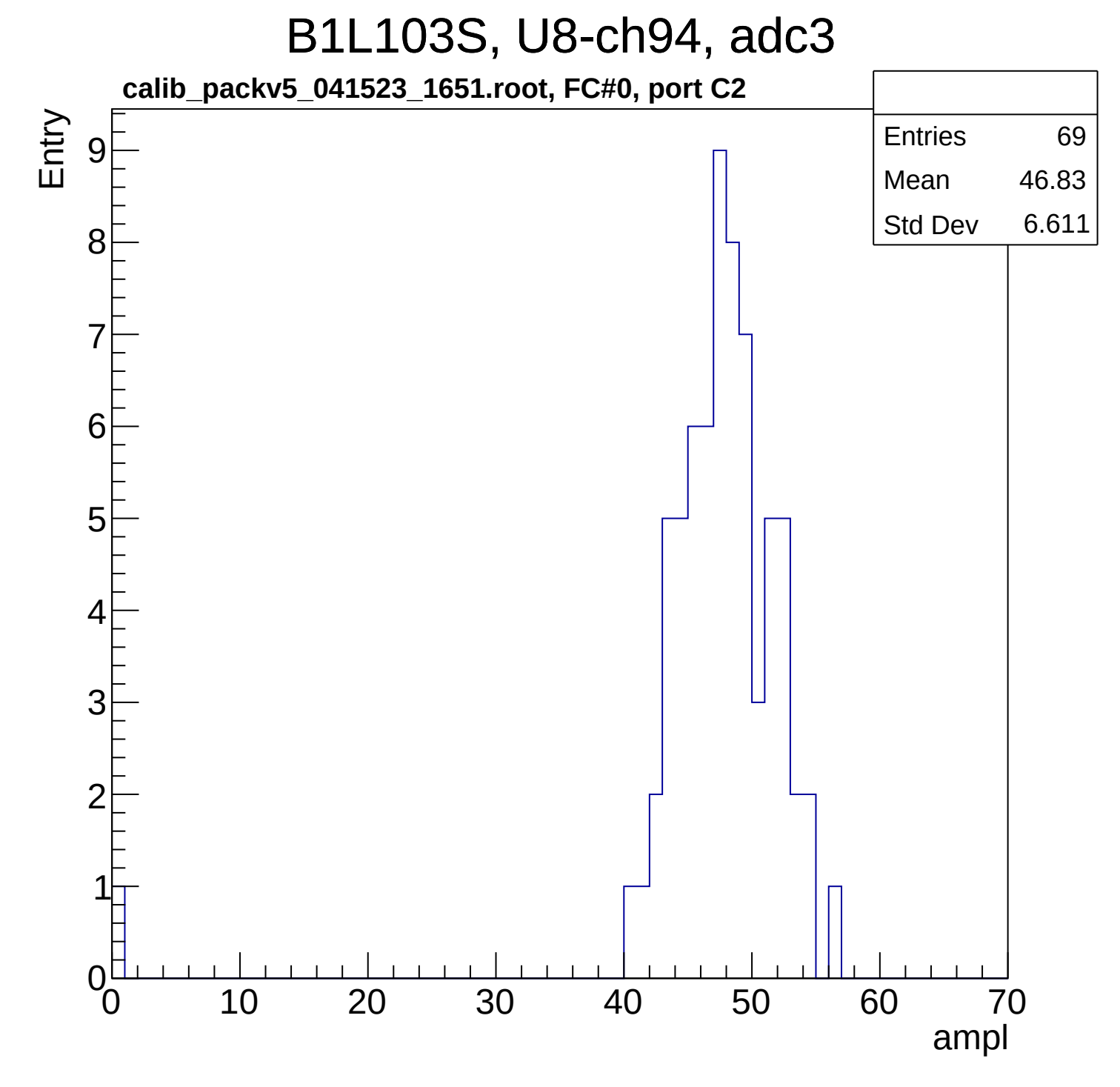
40
50
60
70


B1L103S, U8-ch94, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 46.83
Std Dev 6.611
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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60
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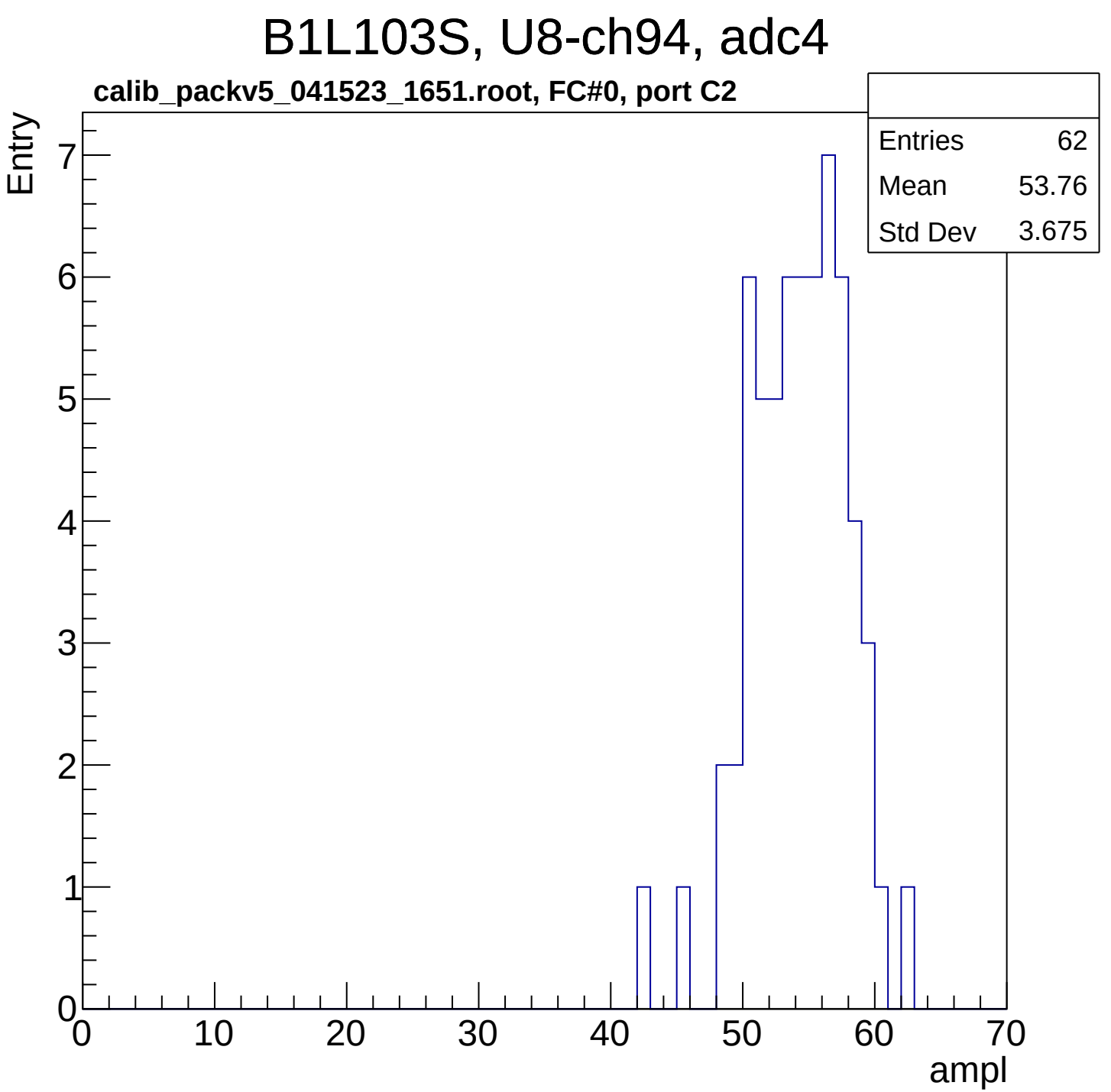
B1L103S, U8-ch94, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 53.76
Std Dev 3.675
Entry
ampl
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4
5
6
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0
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40
50
60
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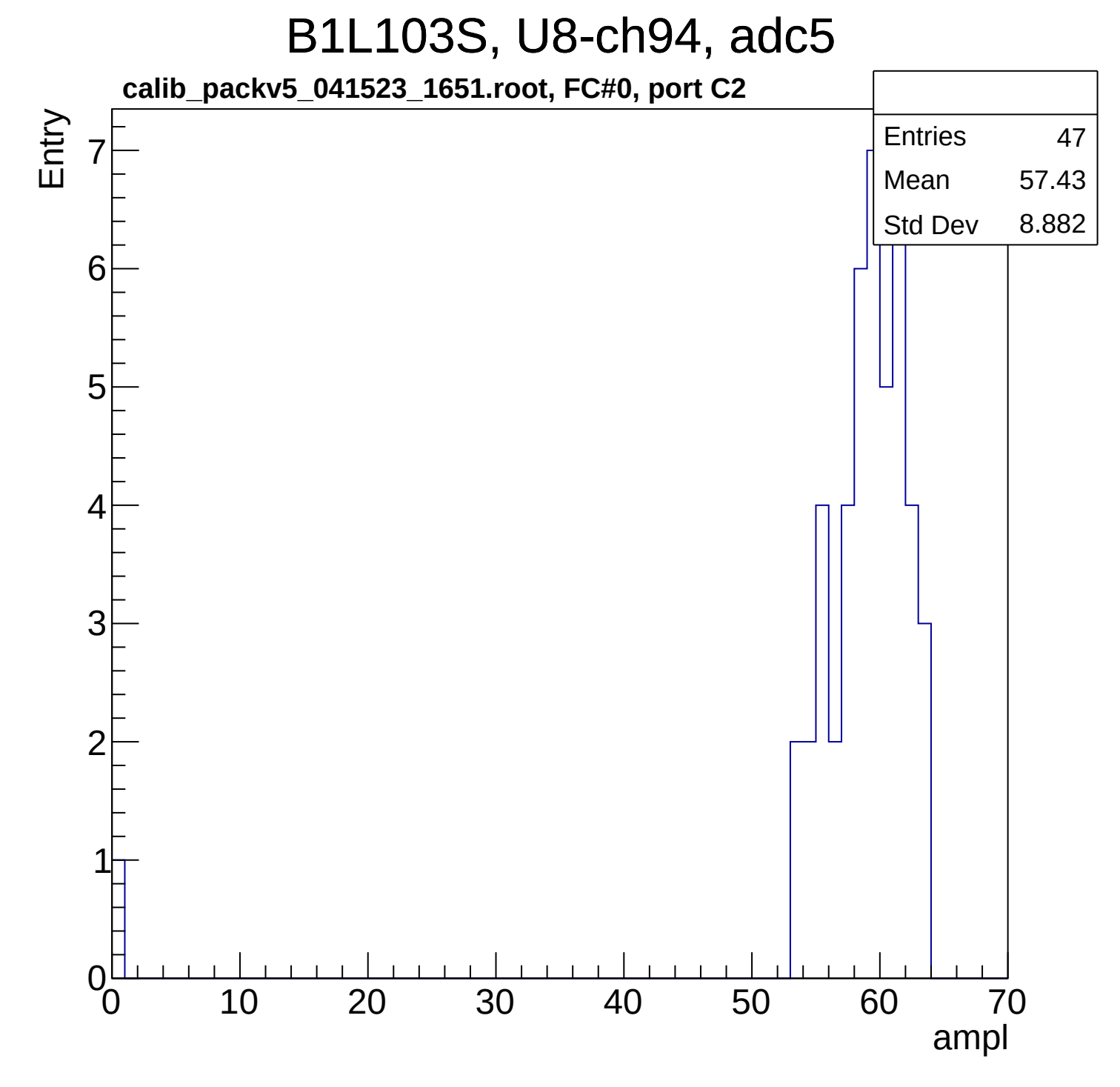
B1L103S, U8-ch94, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 57.43
Std Dev 8.882
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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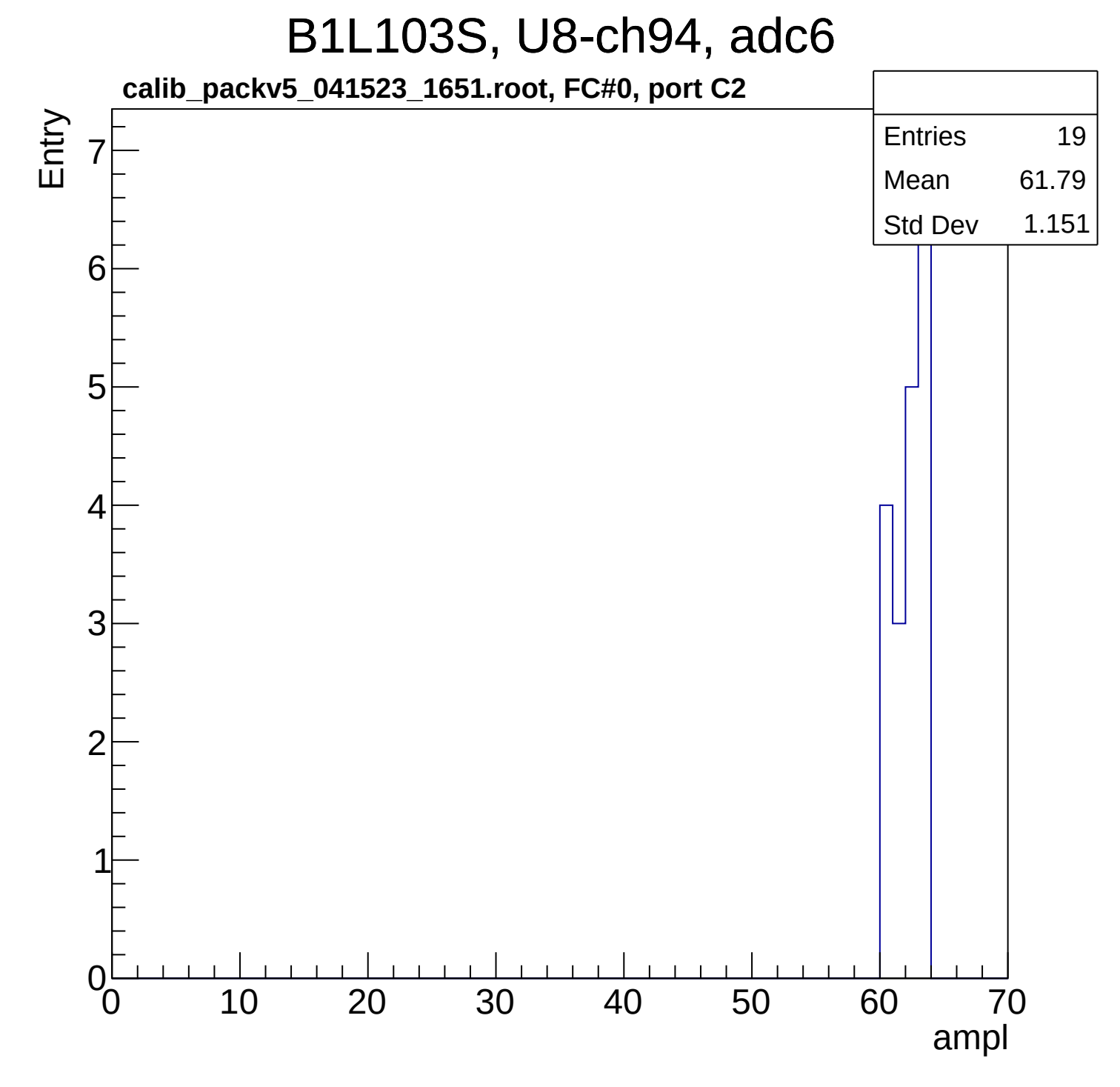
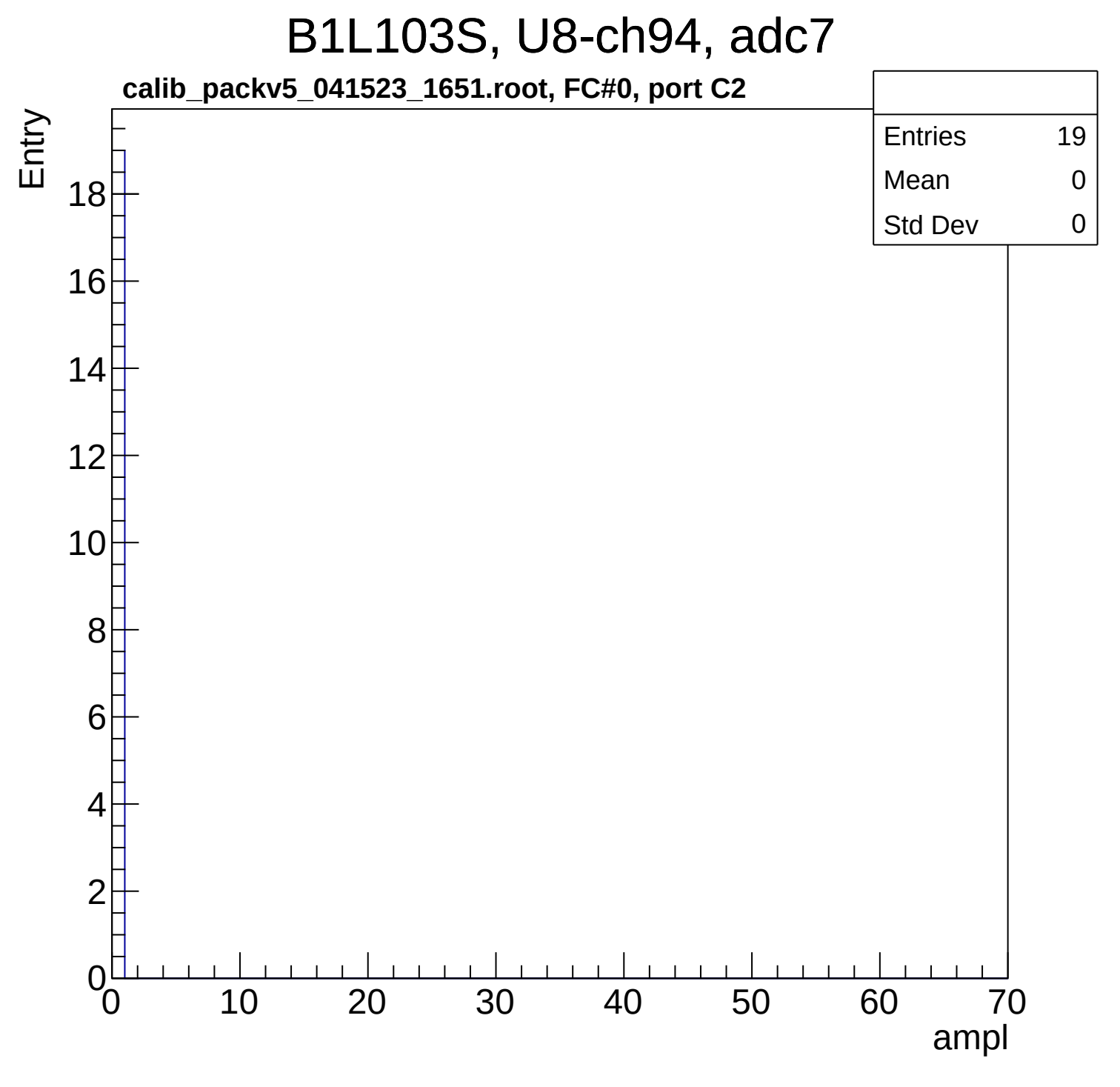
40
50
60
70


B1L103S, U8-ch94, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 61.79
Std Dev 1.151
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U8-ch94, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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2
4
6
8
10
12
14
16
18
0
10
20
30
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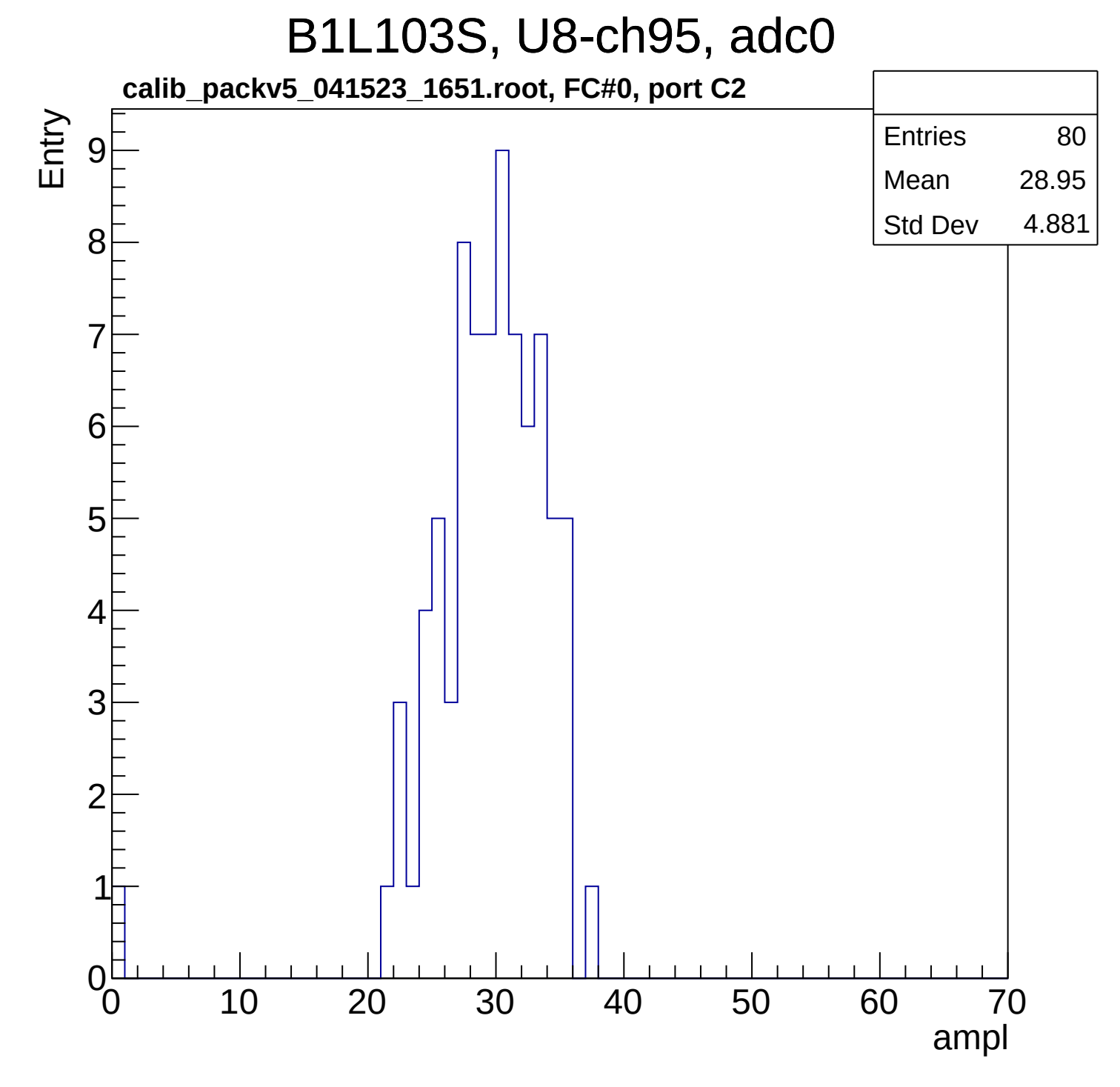
50
60
70
ampl


B1L103S, U8-ch95, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 28.95
Std Dev 4.881
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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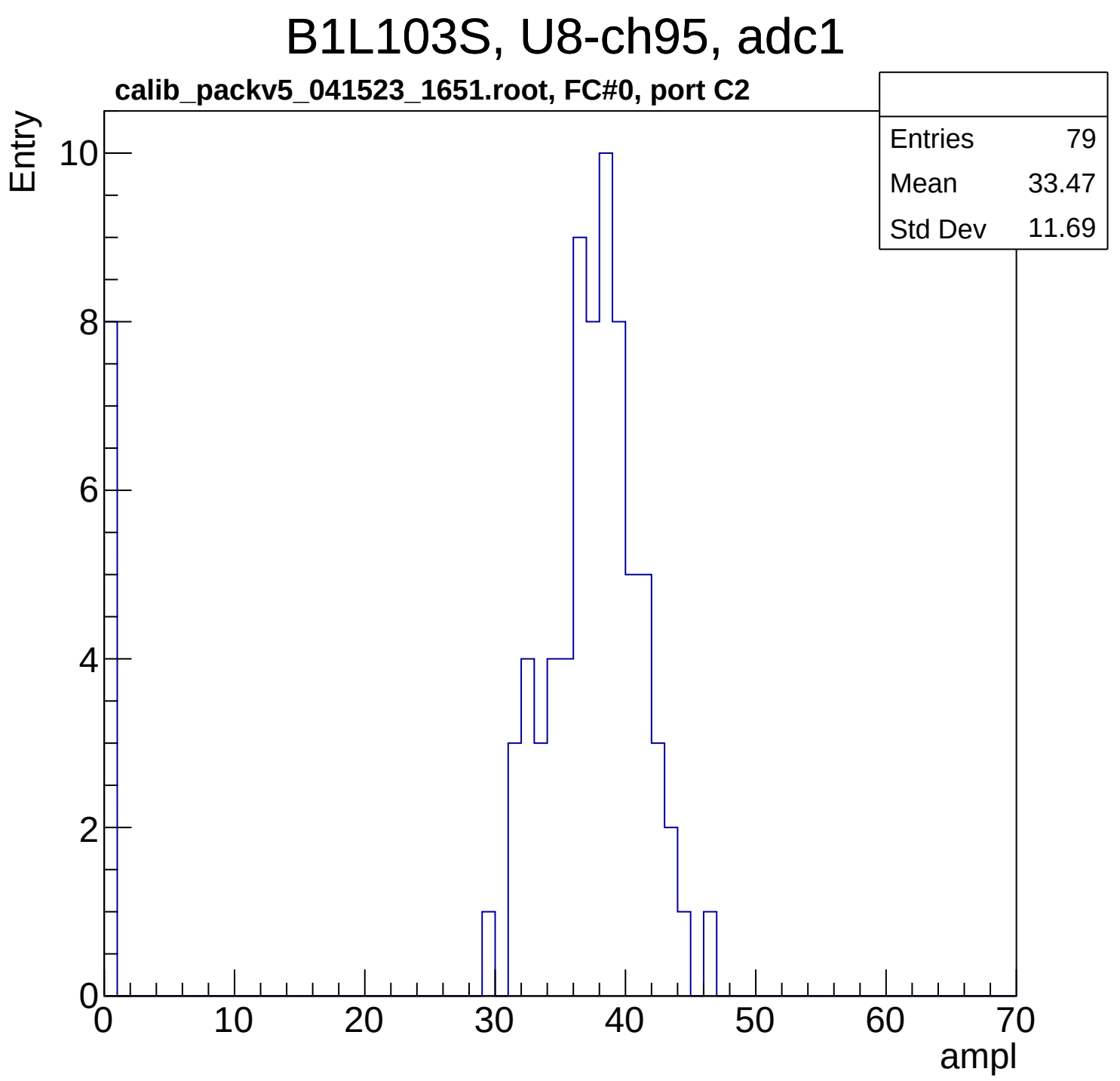
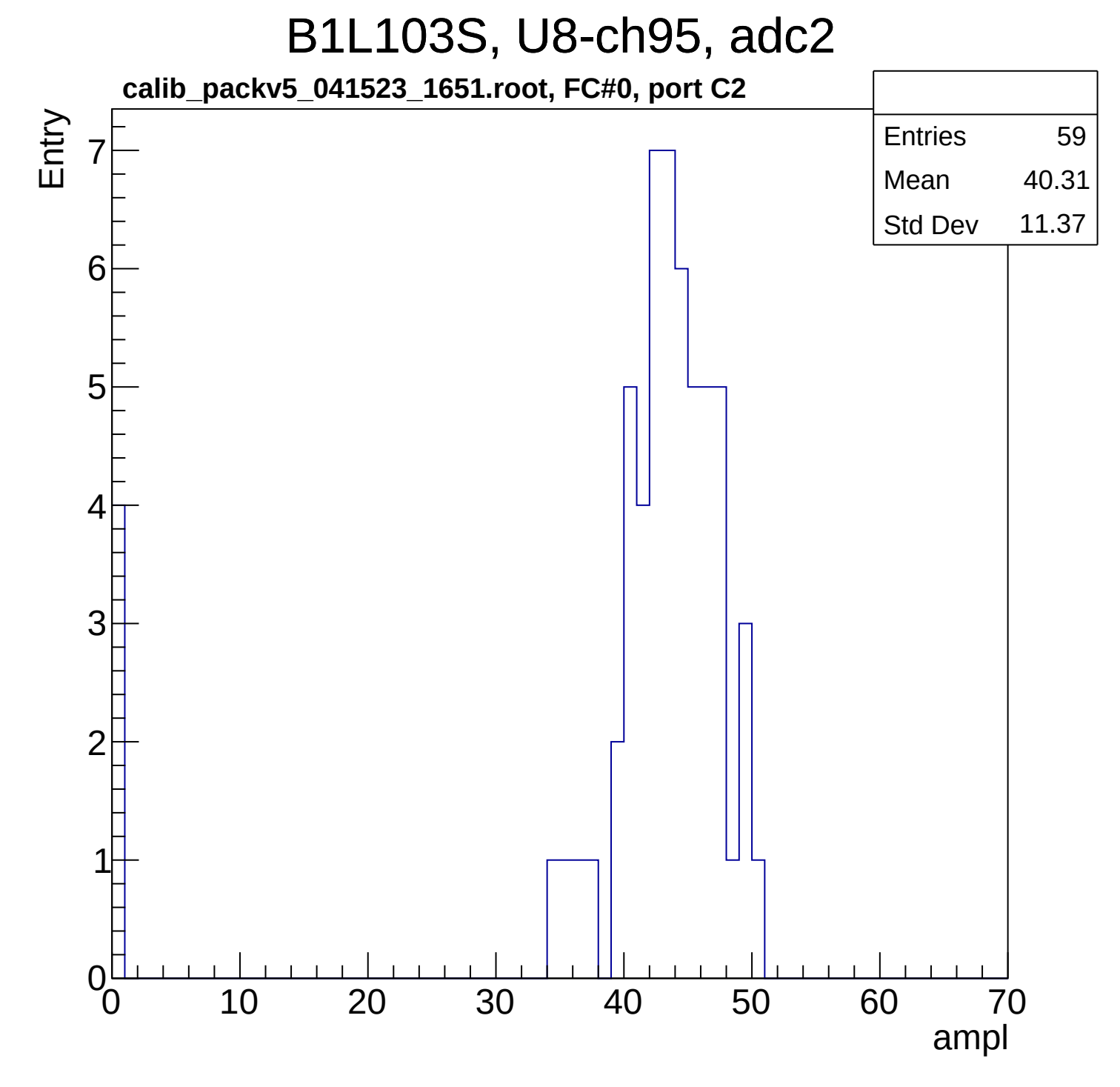
40
50
60
70


B1L103S, U8-ch95, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 33.47
Std Dev 11.69
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U8-ch95, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 40.31
Std Dev 11.37
Entry
ampl
0
1
2
3
4
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0
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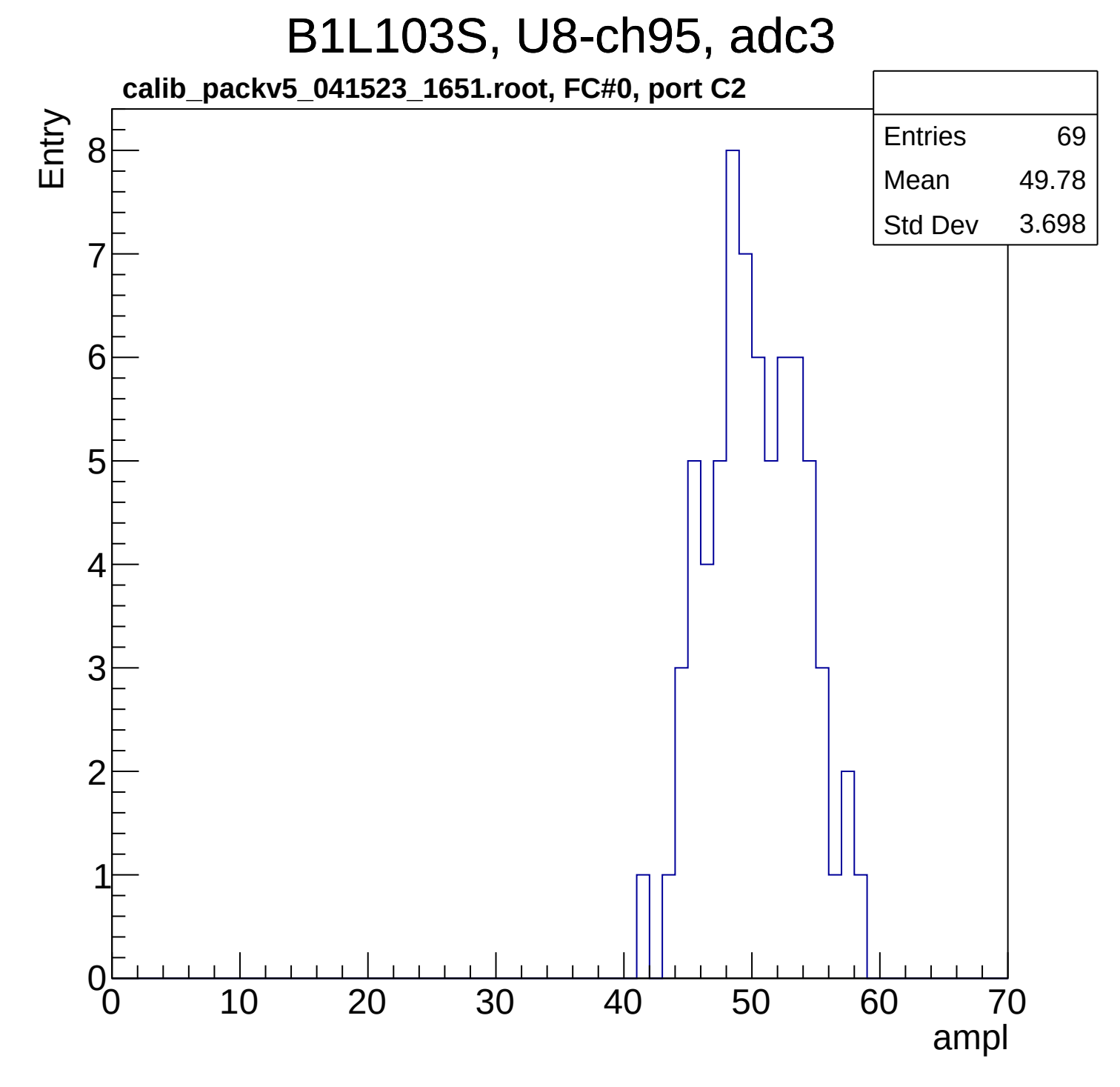
B1L103S, U8-ch95, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 49.78
Std Dev 3.698
Entry
ampl
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2
3
4
5
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7
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0
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20
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60
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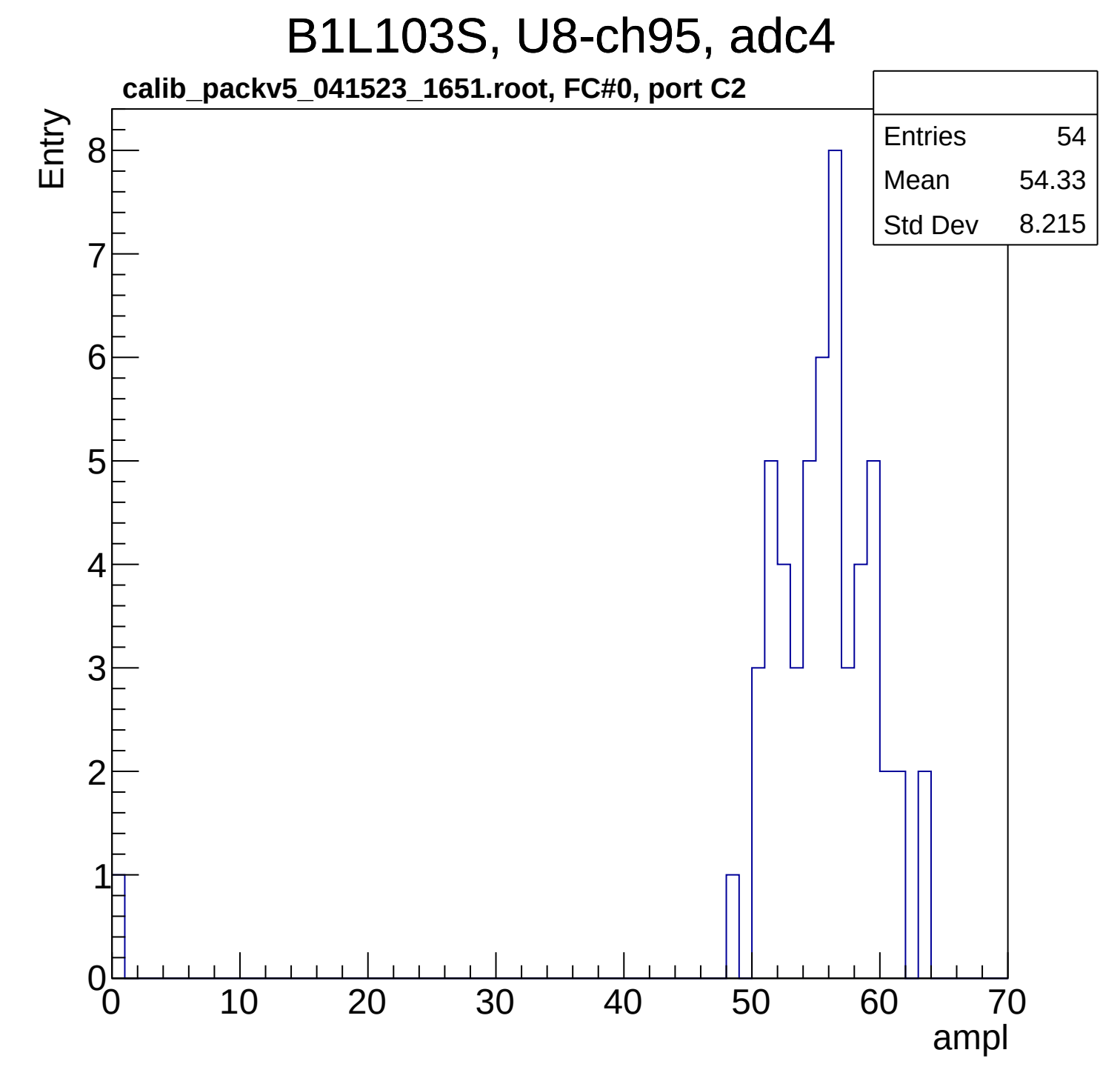
B1L103S, U8-ch95, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 54.33
Std Dev 8.215
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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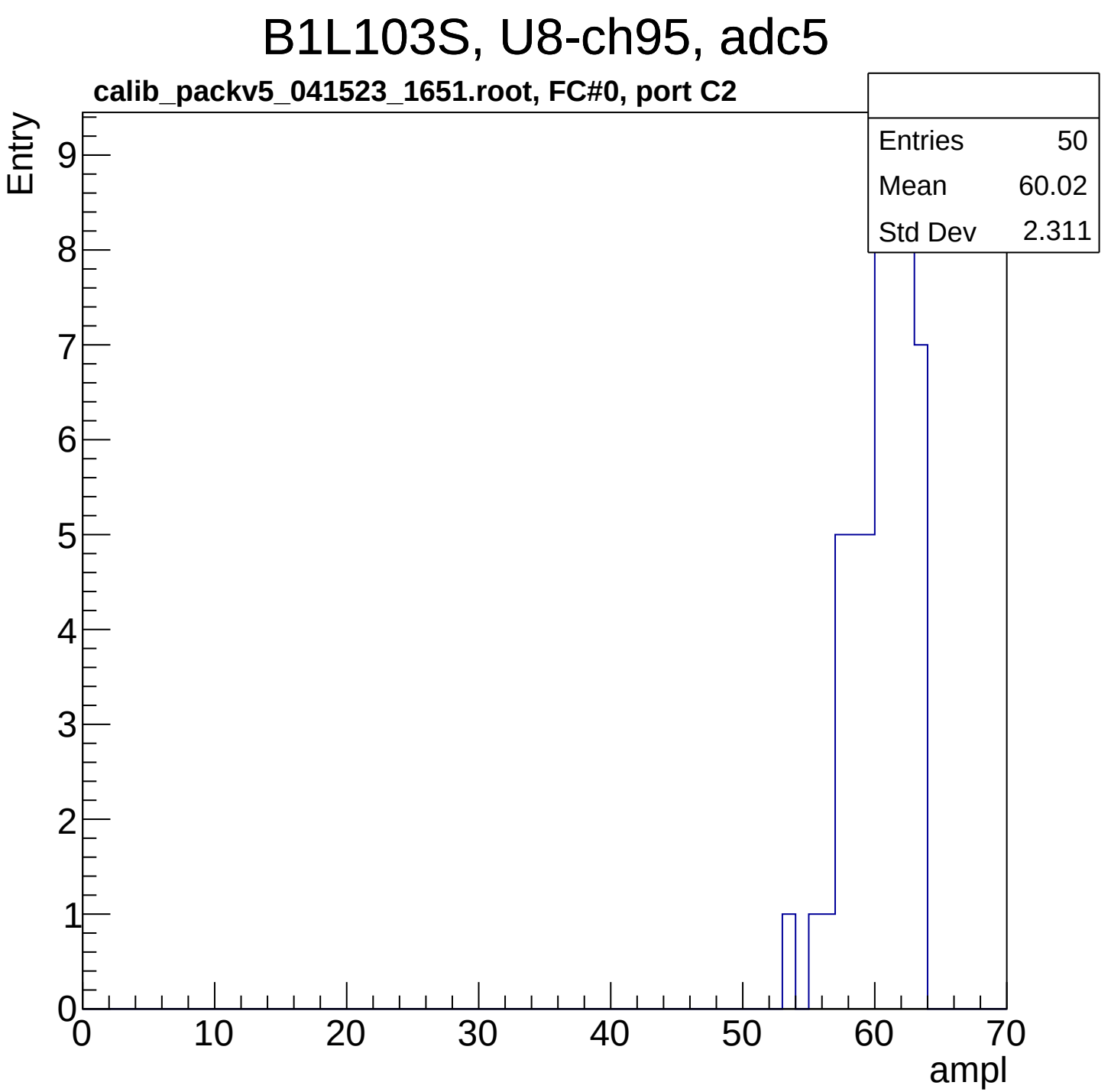
40
50
60
70


B1L103S, U8-ch95, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 60.02
Std Dev 2.311
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
30
40
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60
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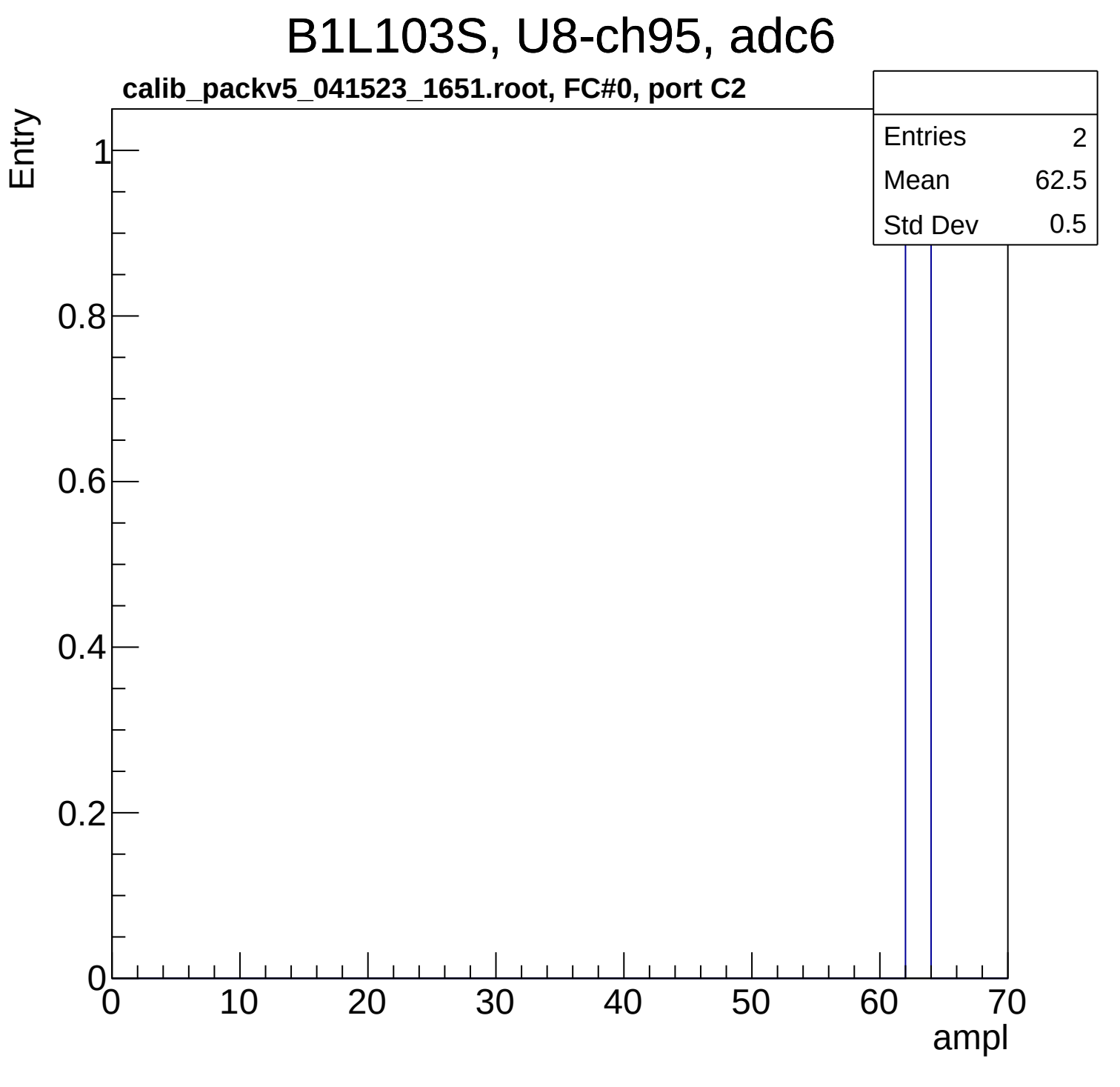
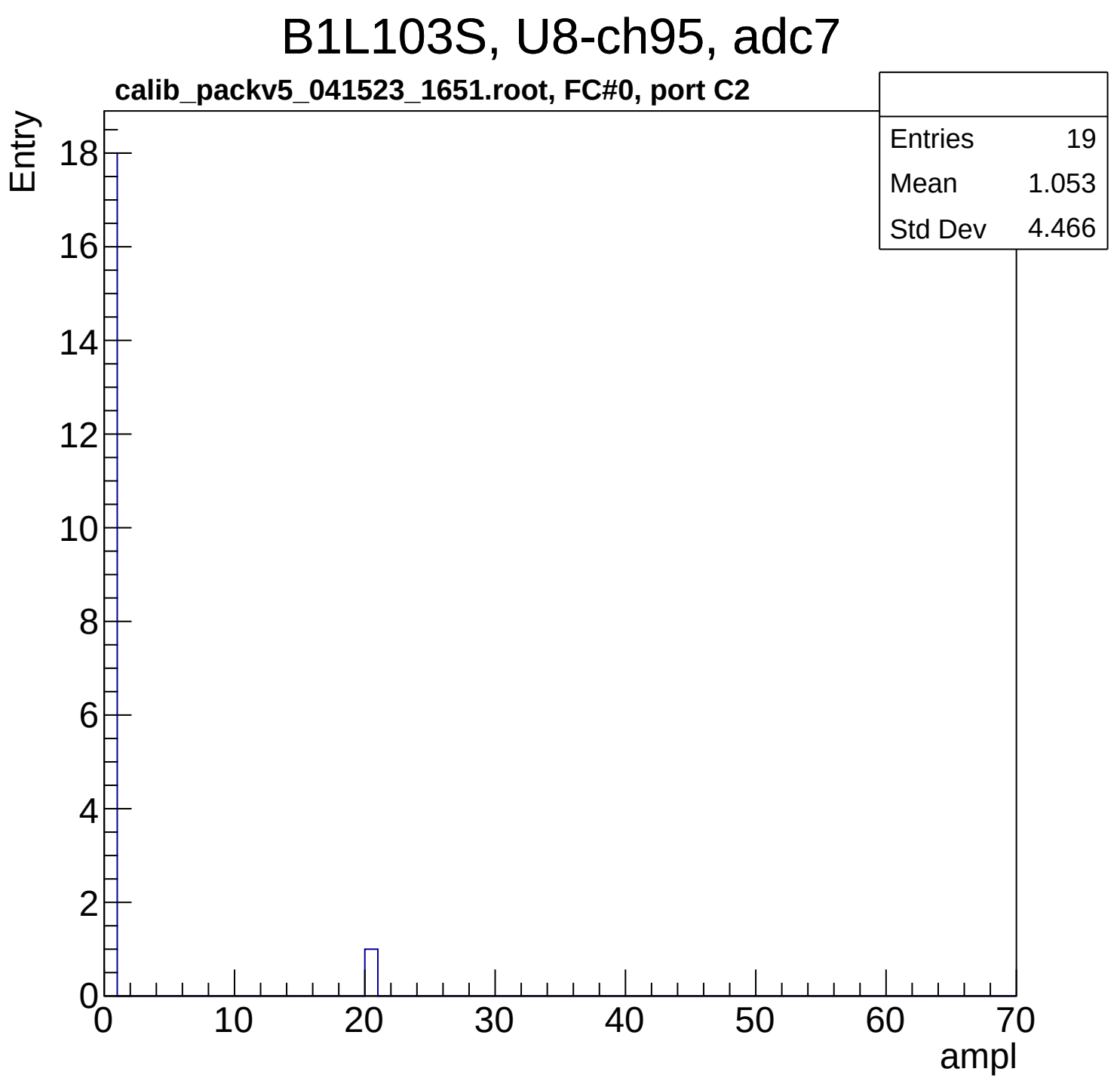

B1L103S, U8-ch95, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch95, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.053
Std Dev 4.466
Entry
ampl
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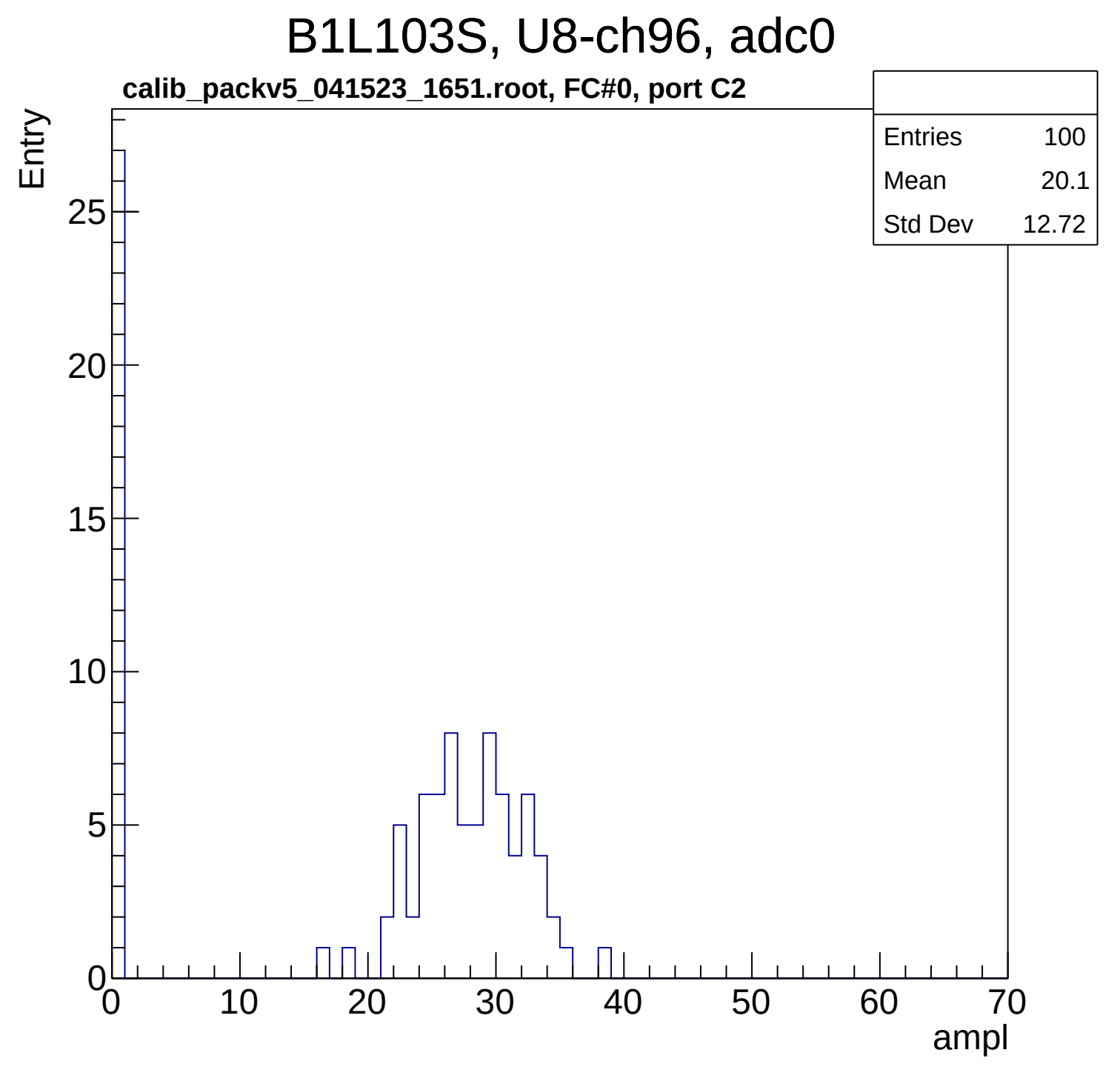
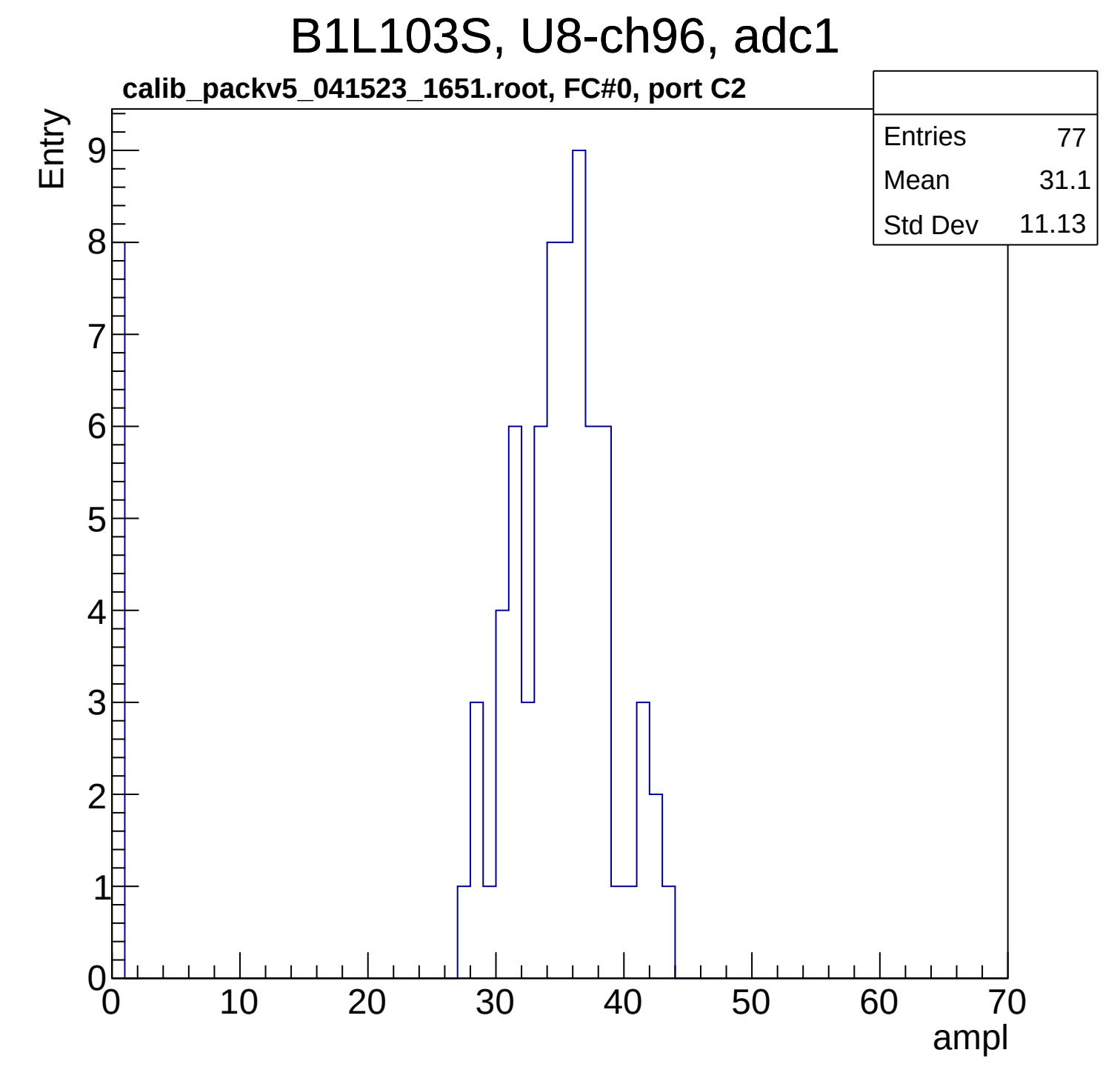
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L103S, U8-ch96, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 100
Mean 20.1
Std Dev 12.72
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch96, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 31.1
Std Dev 11.13
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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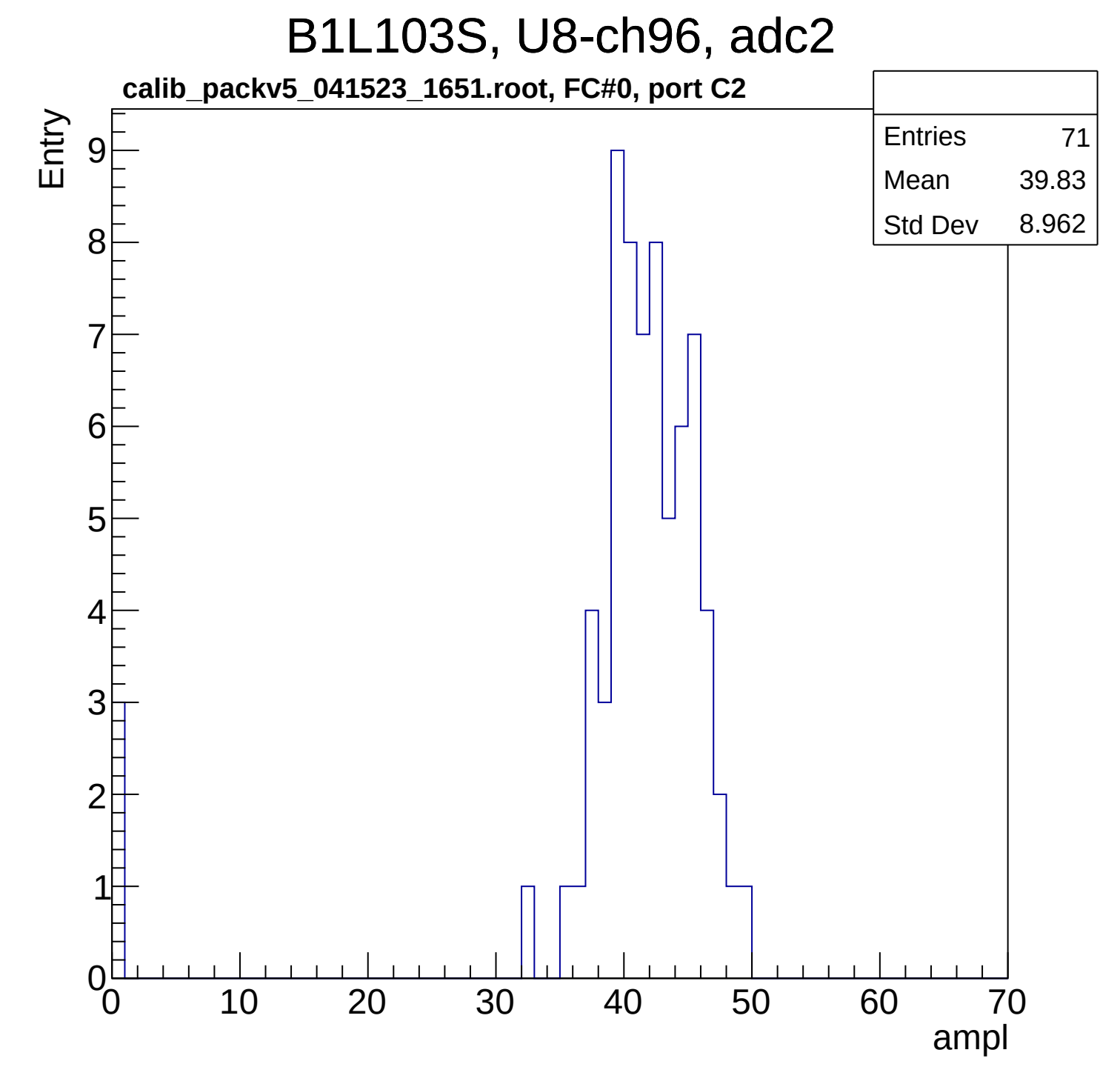
B1L103S, U8-ch96, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 39.83
Std Dev 8.962
Entry
ampl
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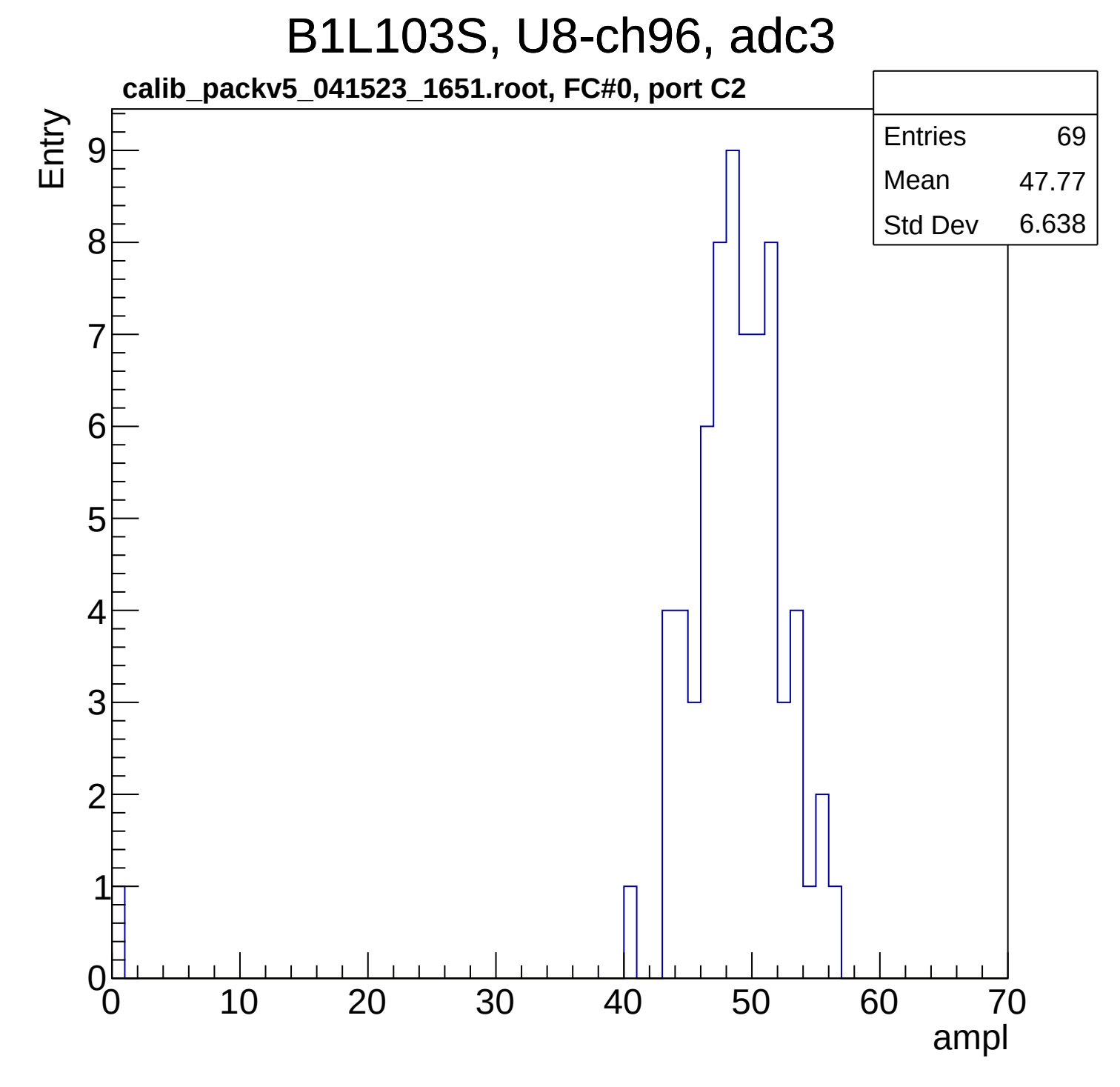
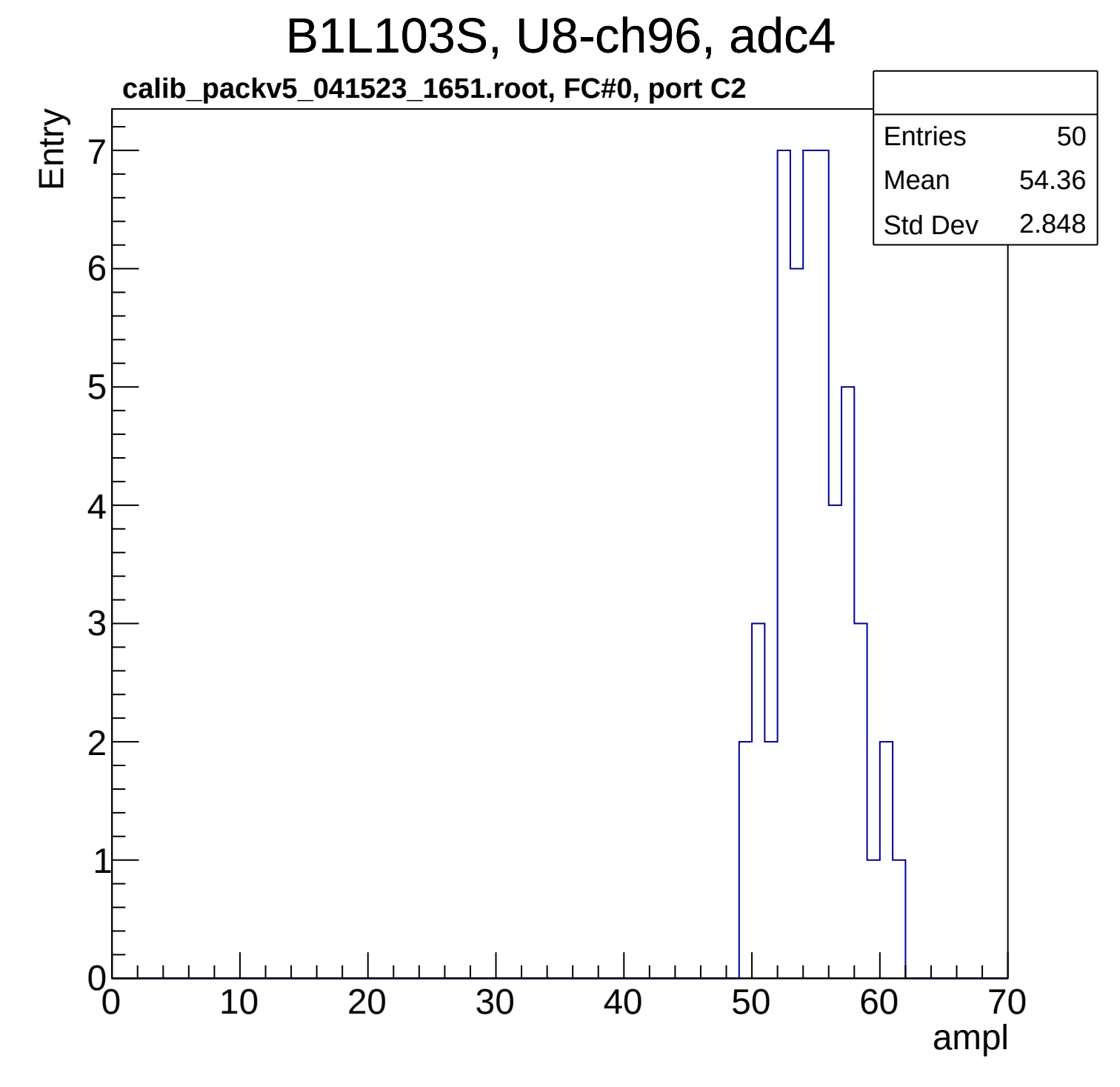
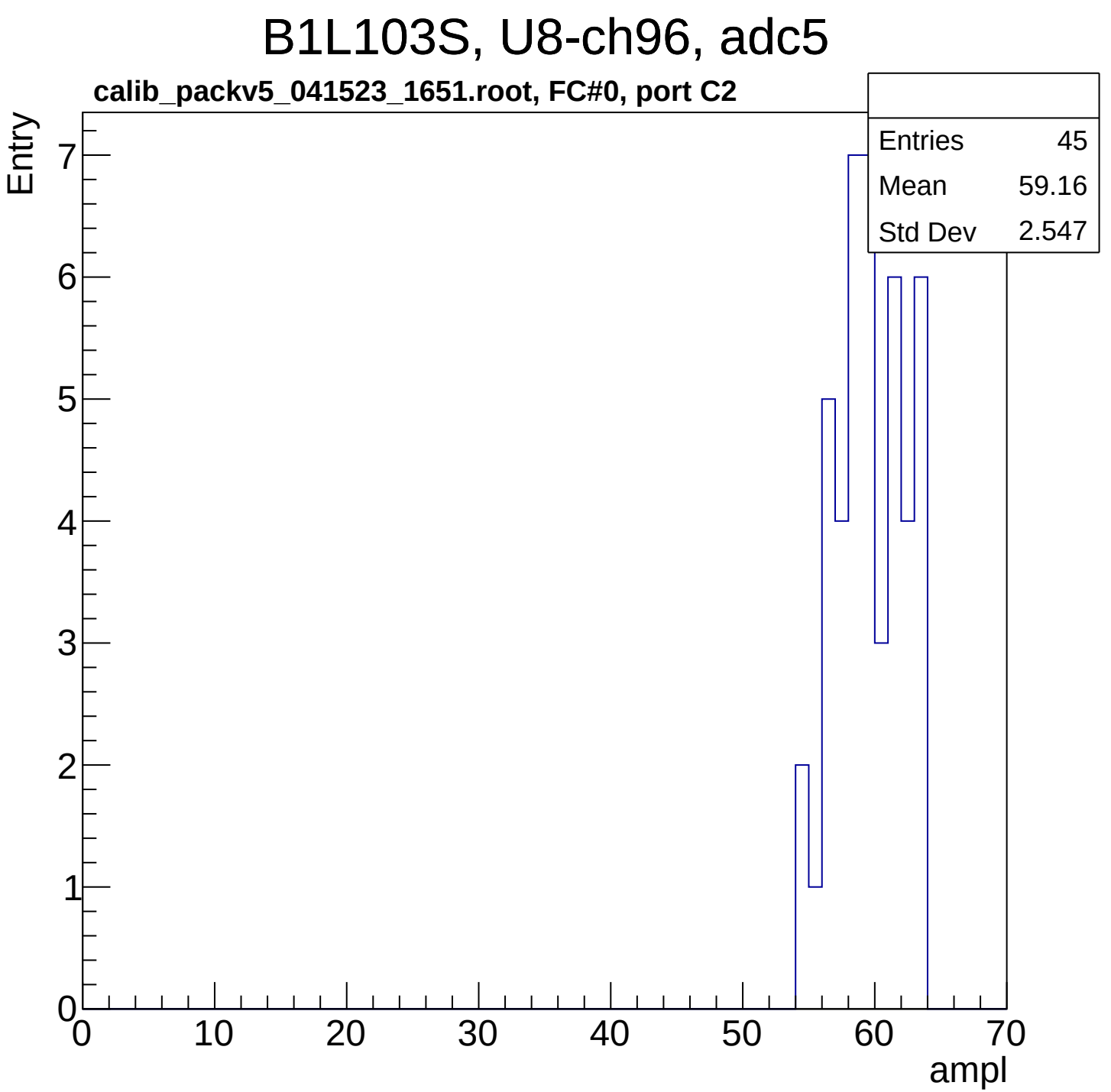
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U8-ch96, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 47.77
Std Dev 6.638
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U8-ch96, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 54.36
Std Dev 2.848
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U8-ch96, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 59.16
Std Dev 2.547
Entry
ampl
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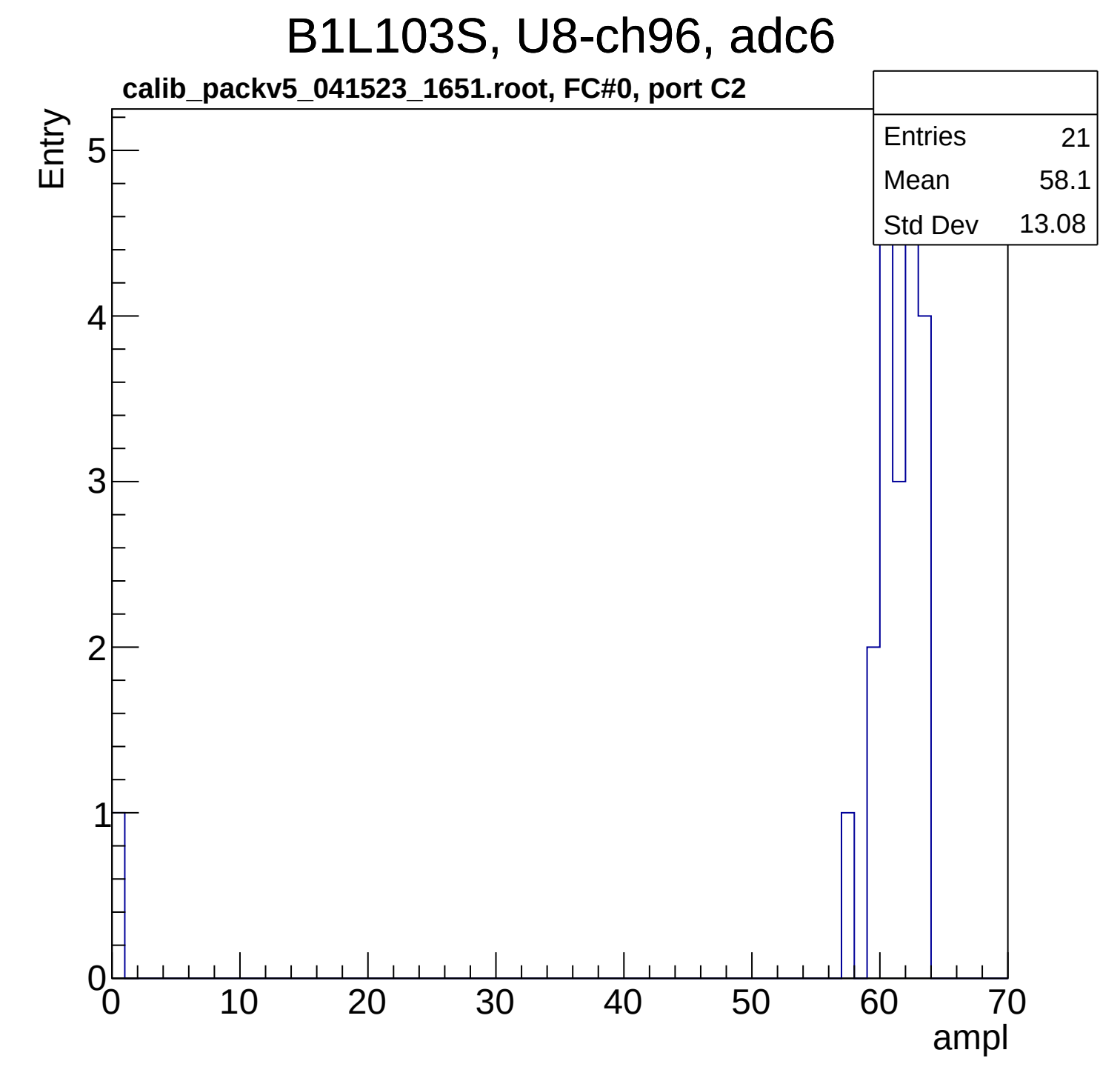
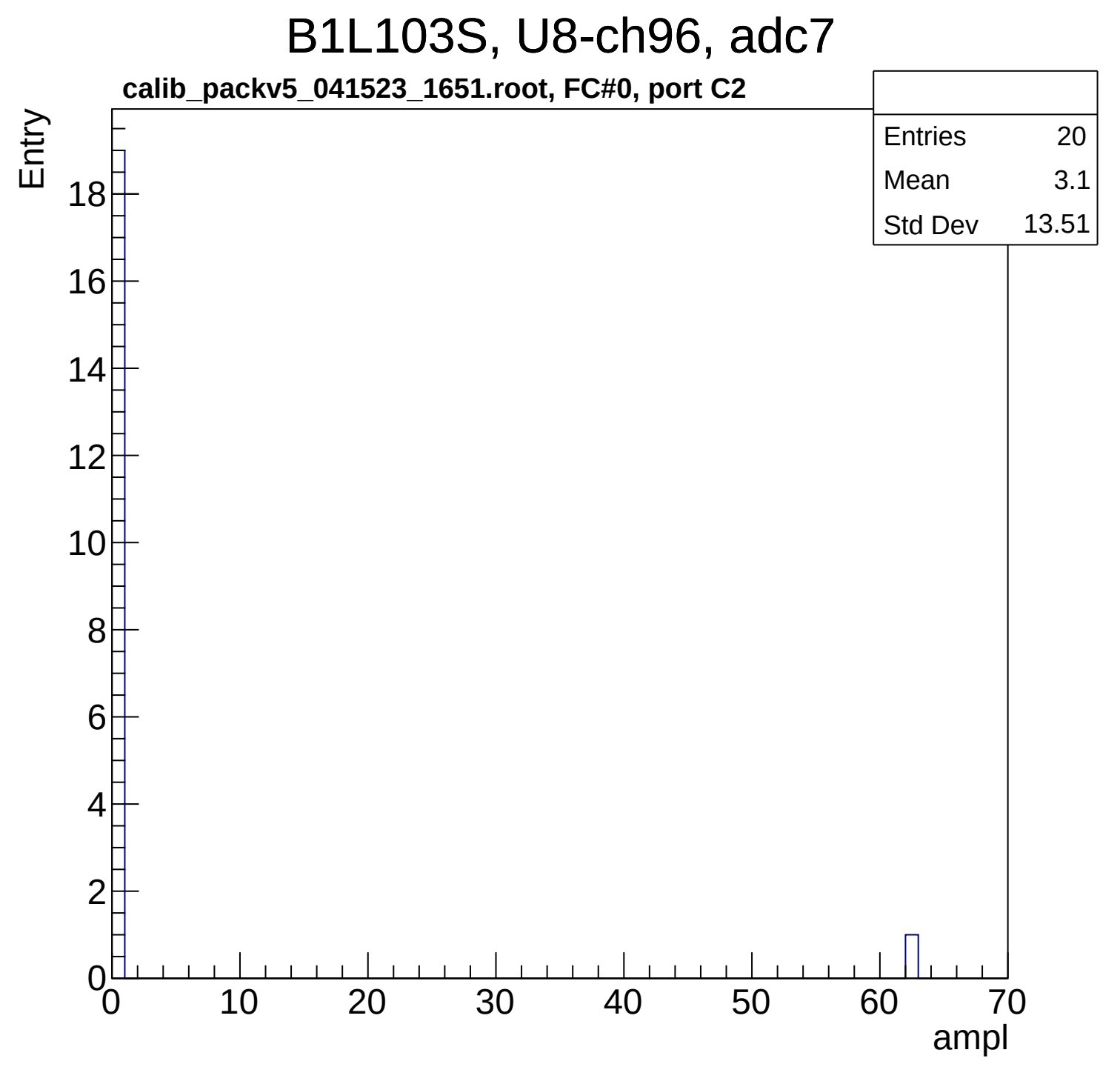
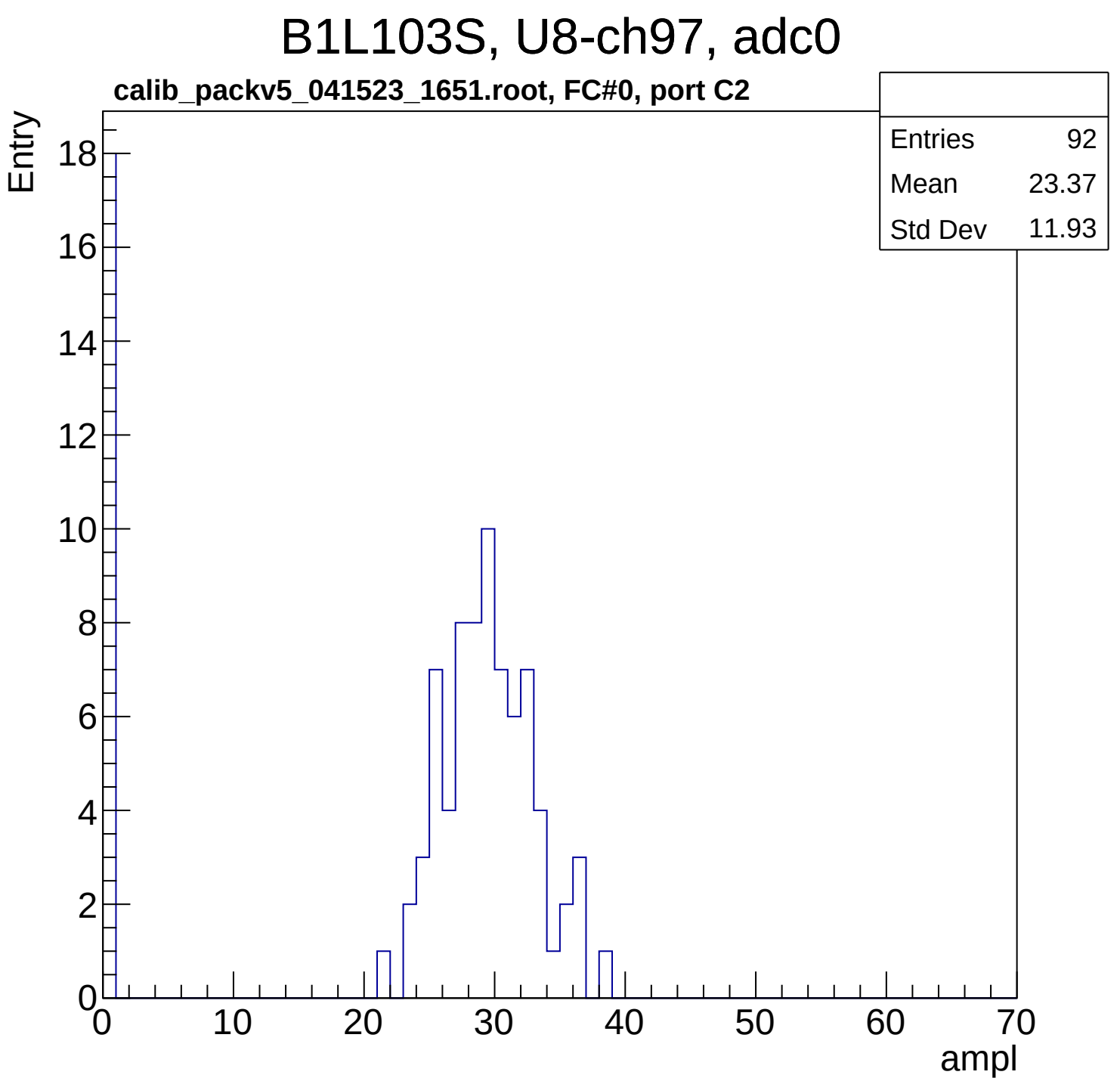
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U8-ch96, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 58.1
Std Dev 13.08
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch96, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch97, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 23.37
Std Dev 11.93
Entry
ampl
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4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
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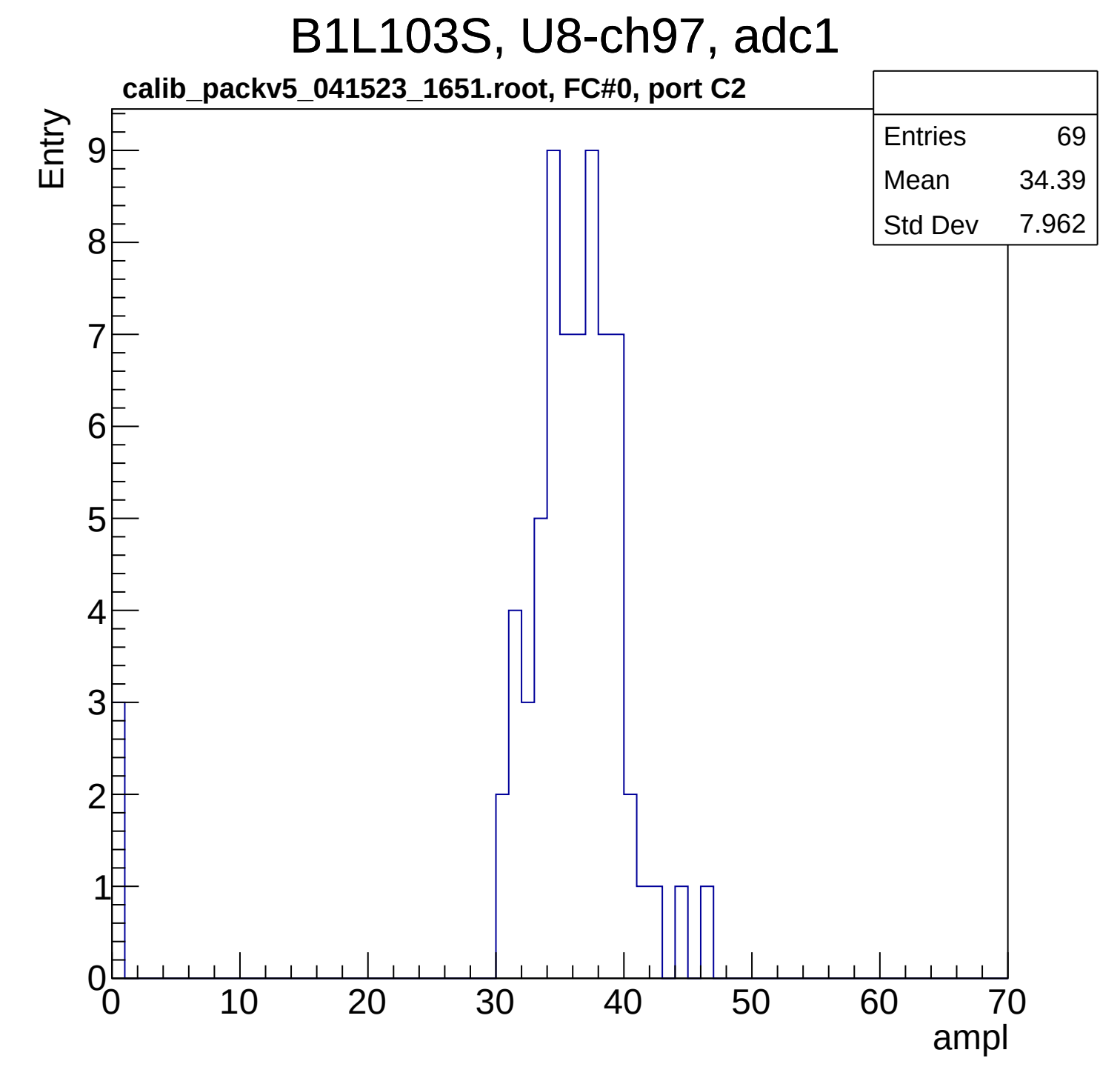
B1L103S, U8-ch97, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 34.39
Std Dev 7.962
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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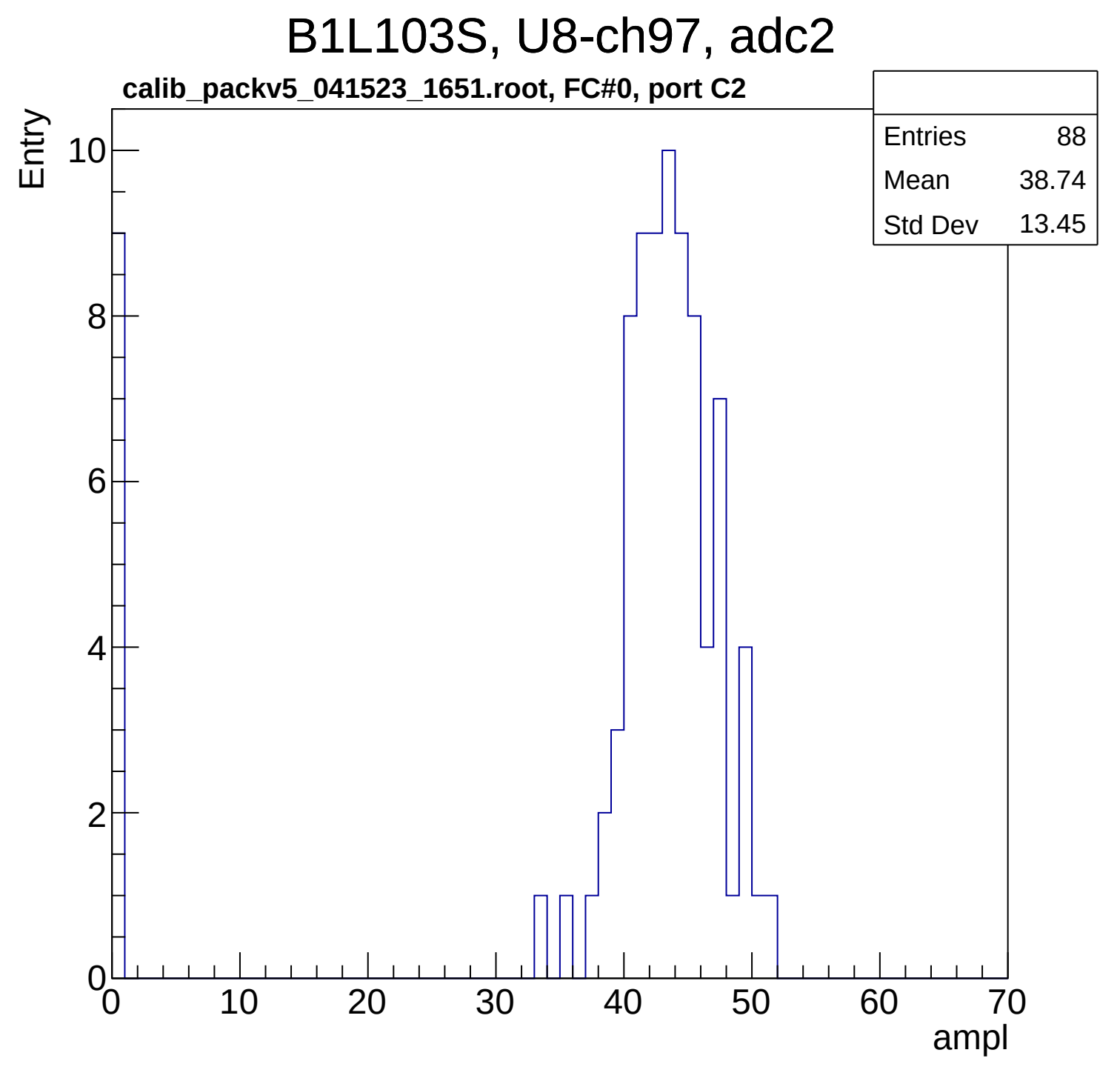
B1L103S, U8-ch97, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 38.74
Std Dev 13.45
Entry
ampl
0
2
4
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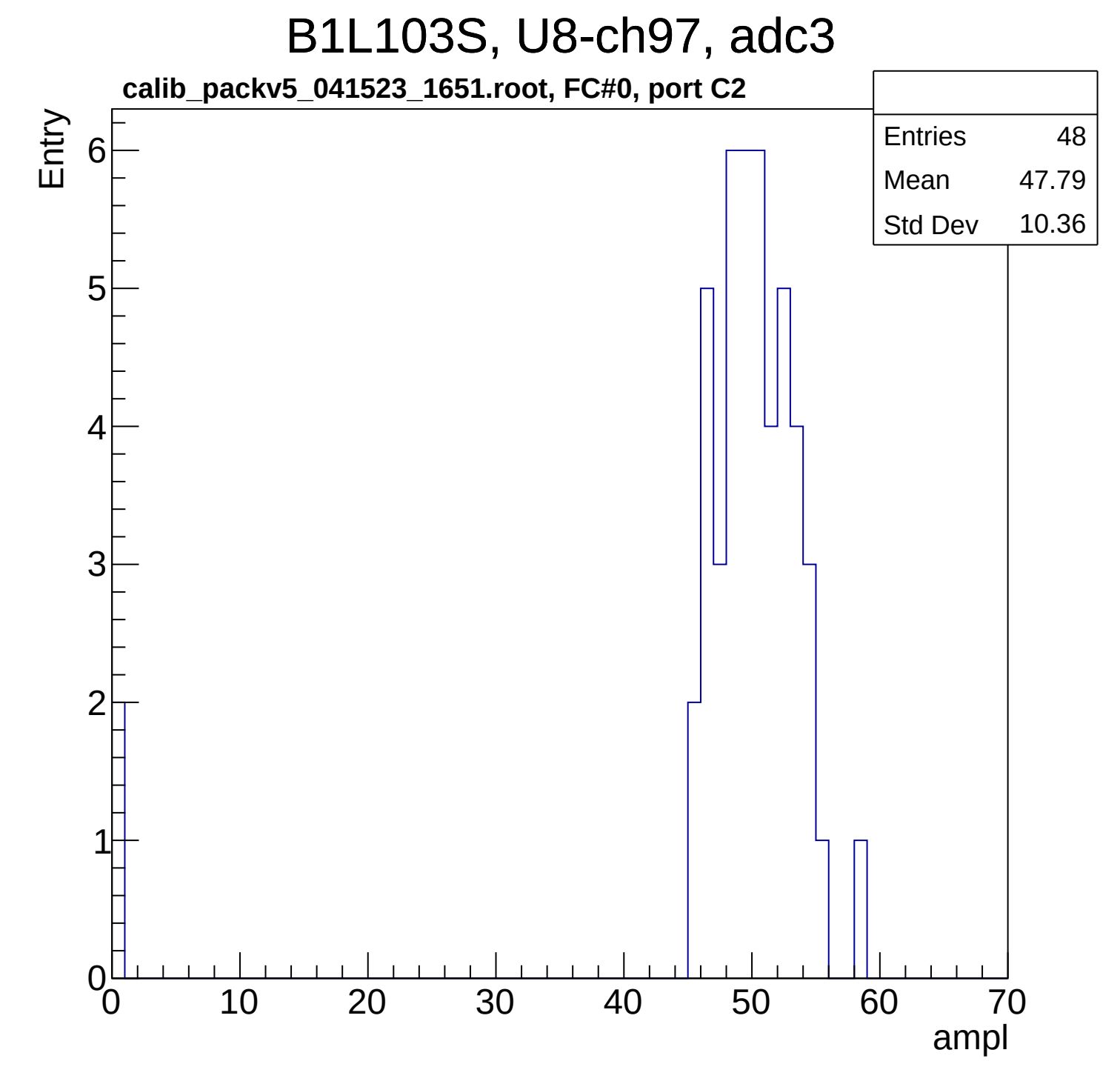
8
10
0
10
20
30
40
50
60
70


B1L103S, U8-ch97, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 47.79
Std Dev 10.36
Entry
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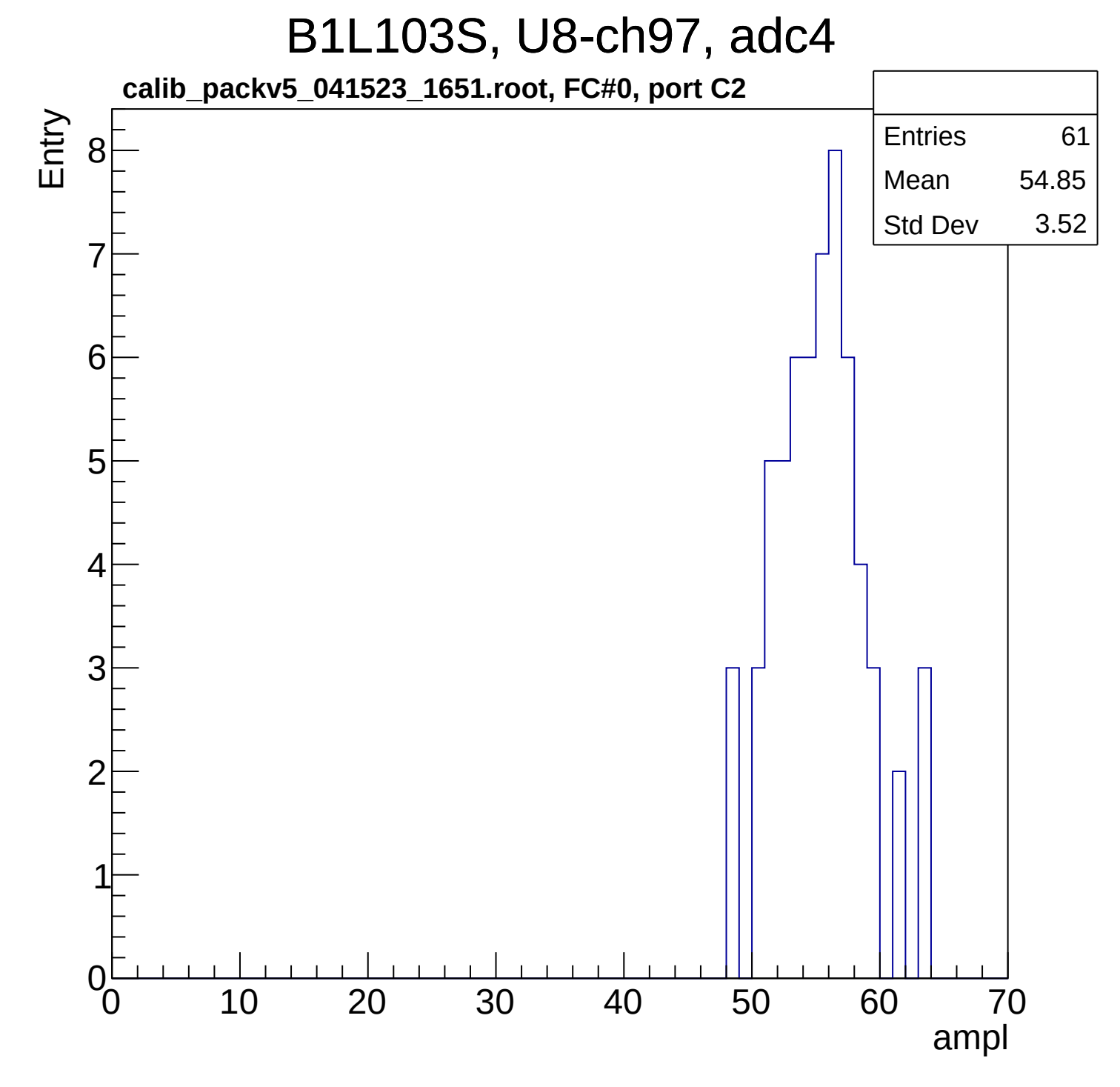
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch97, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 54.85
Std Dev 3.52
Entry
ampl
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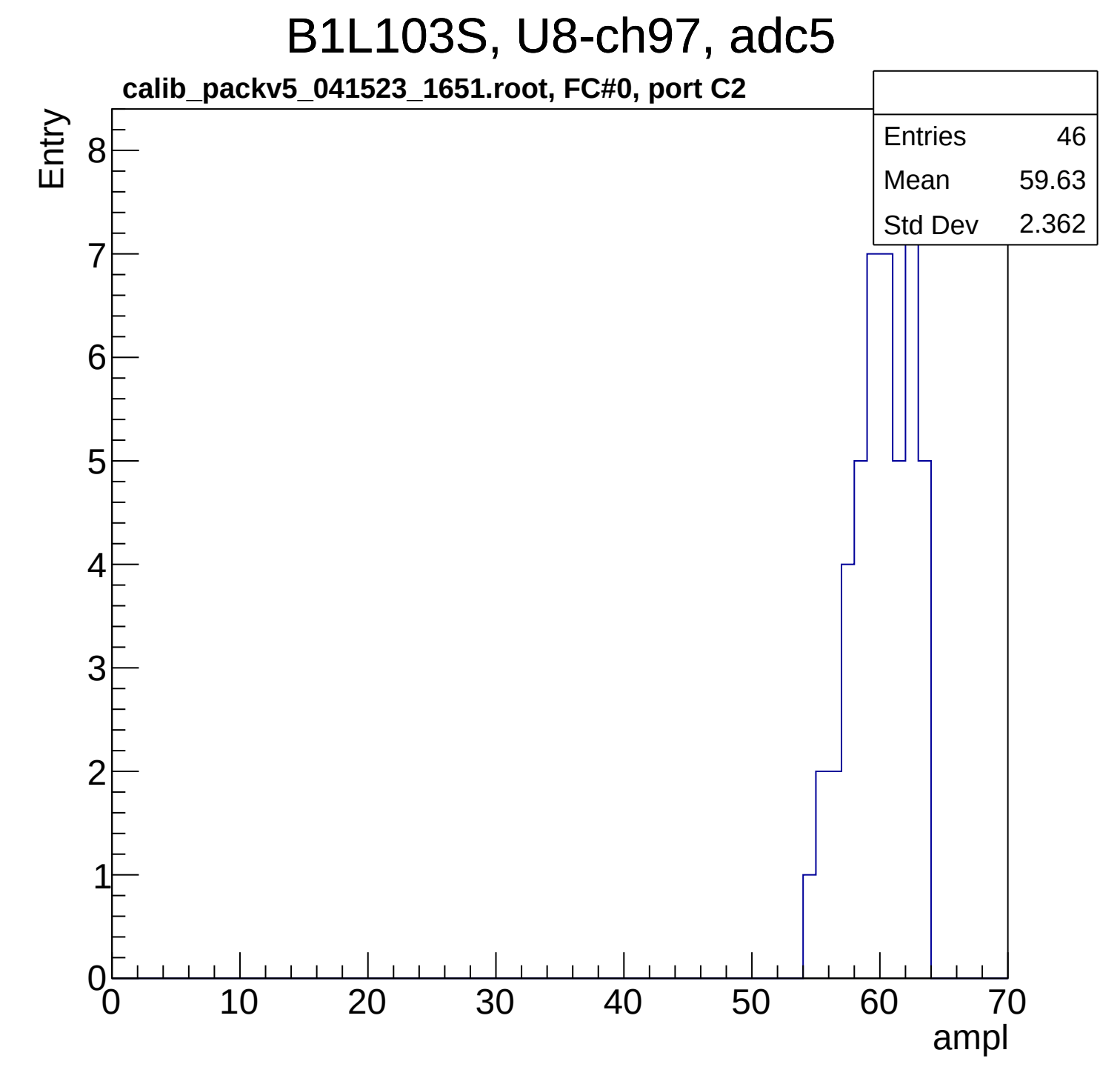
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch97, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 59.63
Std Dev 2.362
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
50
60
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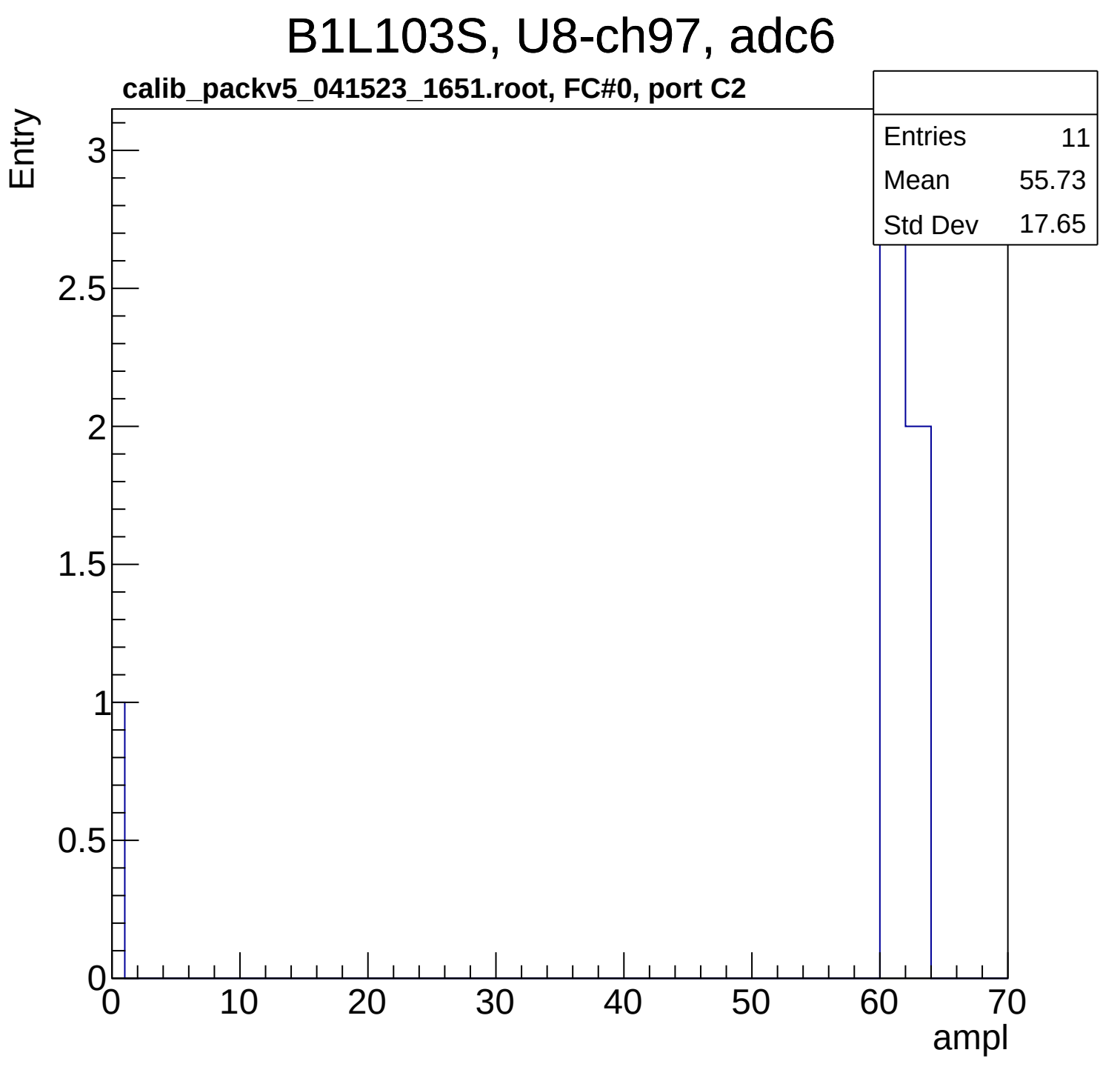
B1L103S, U8-ch97, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 55.73
Std Dev 17.65
Entry
ampl
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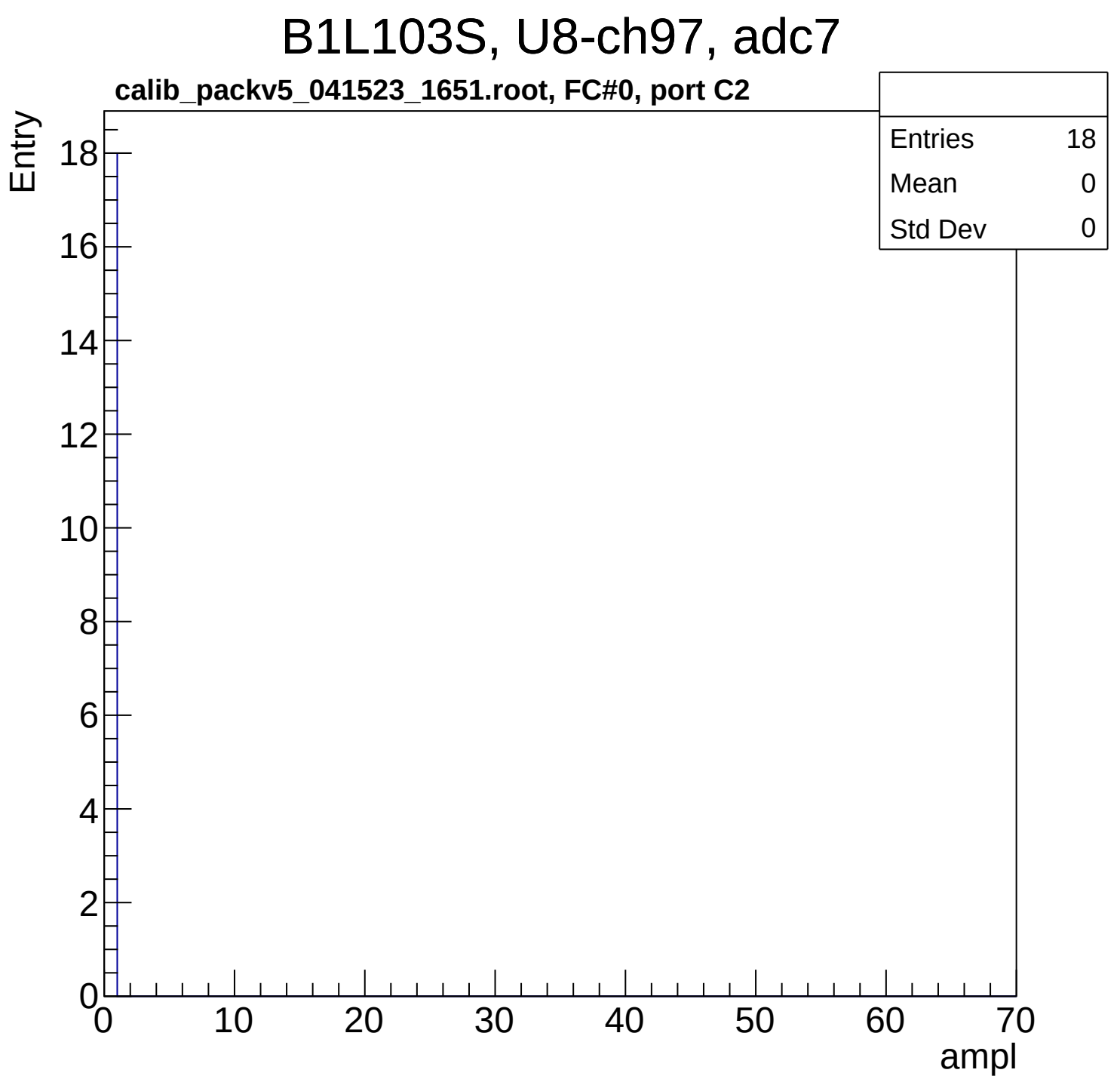
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U8-ch97, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
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6
8
10
12
14
16
18
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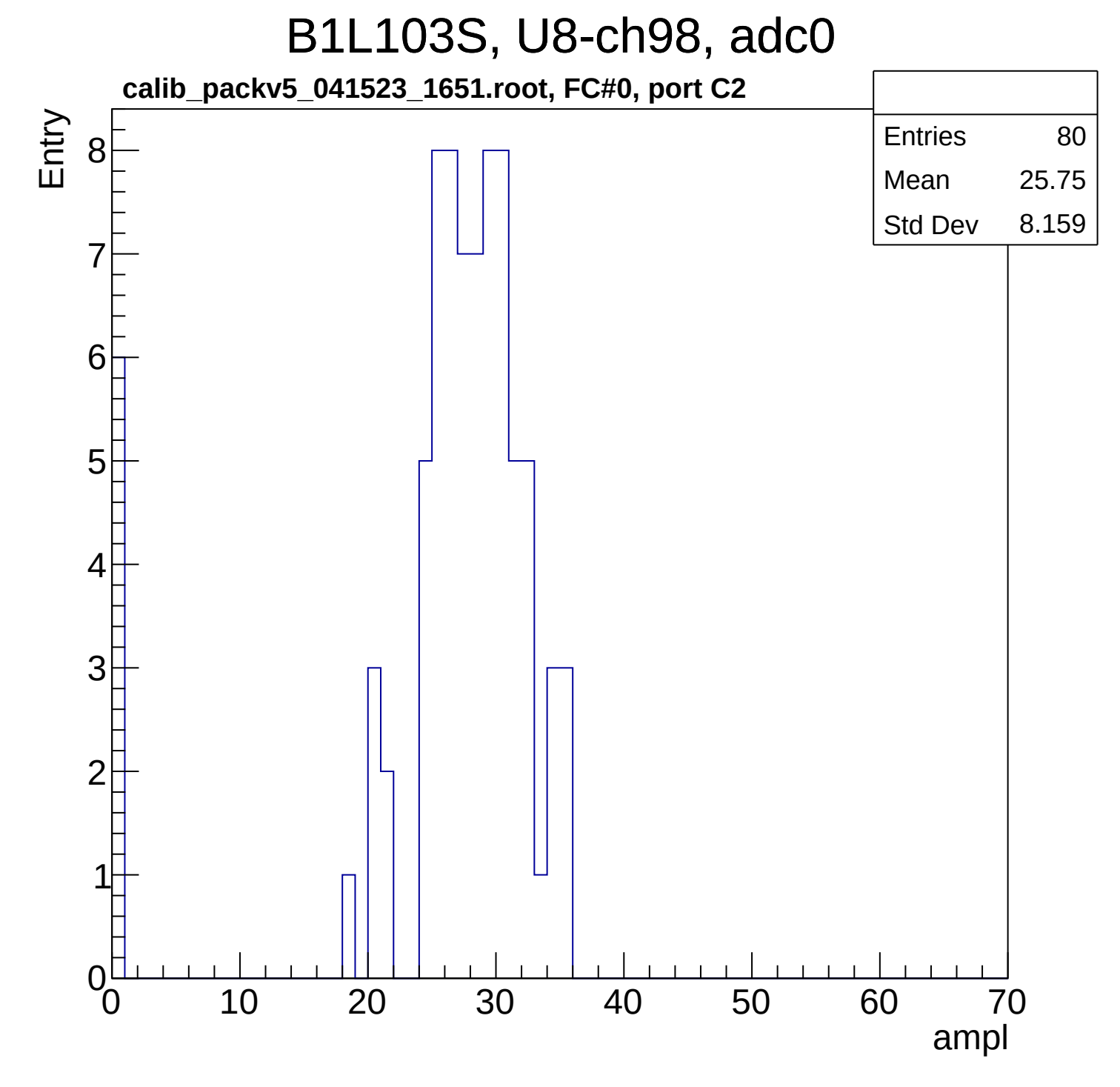
20
30
40
50
60
70
ampl


B1L103S, U8-ch98, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 25.75
Std Dev 8.159
Entry
ampl
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2
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5
6
7
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0
10
20
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40
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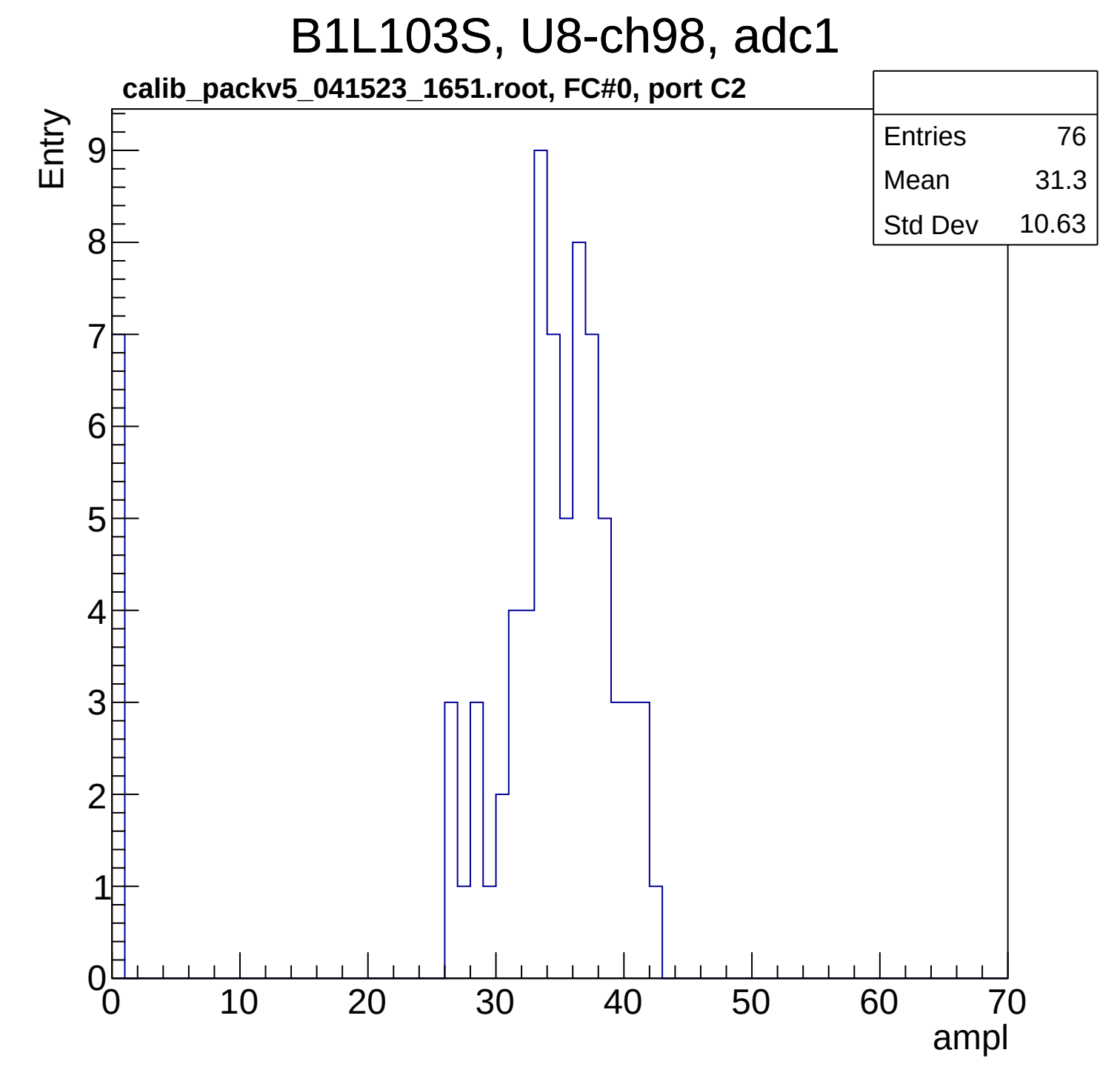
60
70


B1L103S, U8-ch98, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 31.3
Std Dev 10.63
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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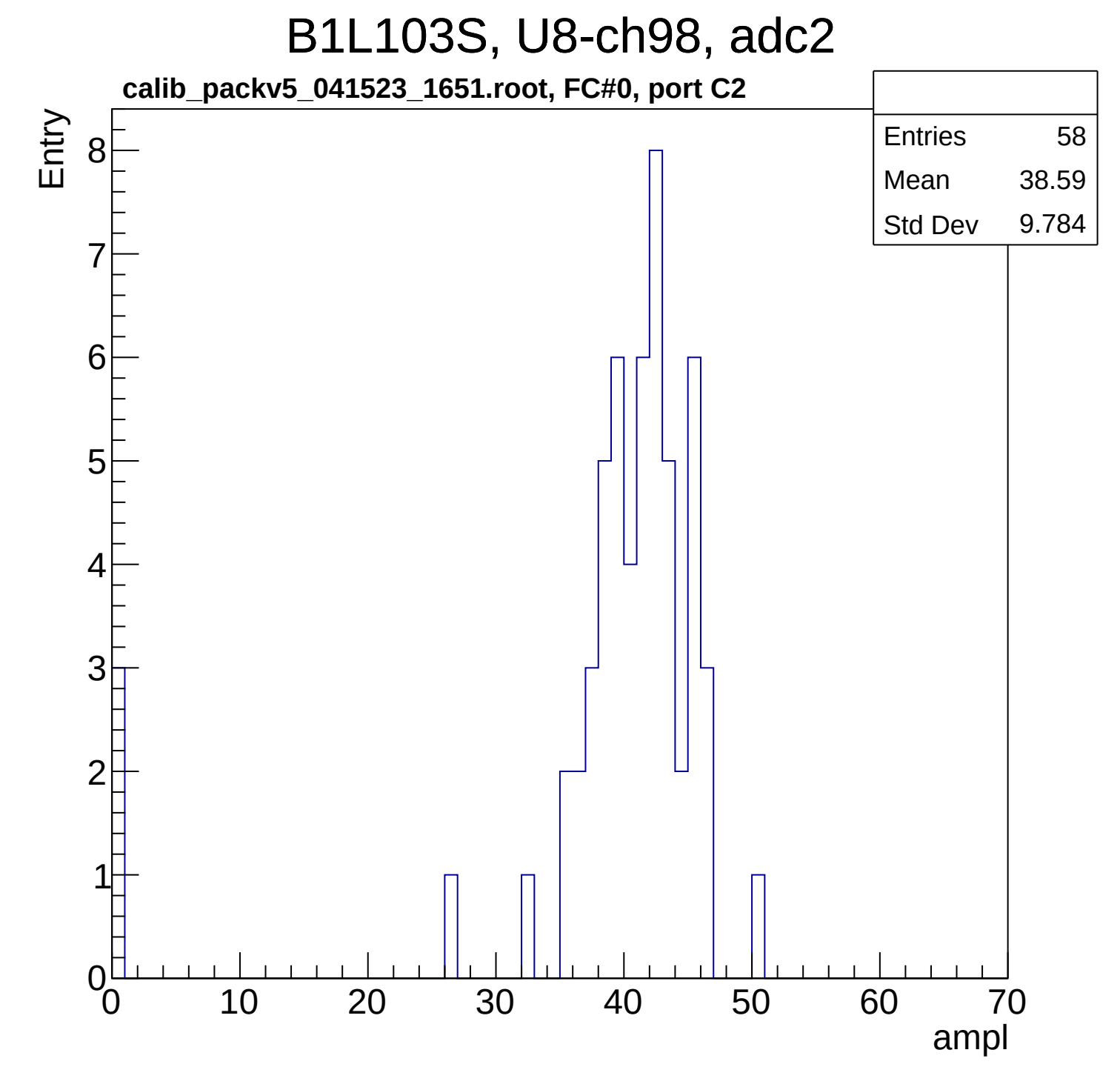
40
50
60
70


B1L103S, U8-ch98, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 38.59
Std Dev 9.784
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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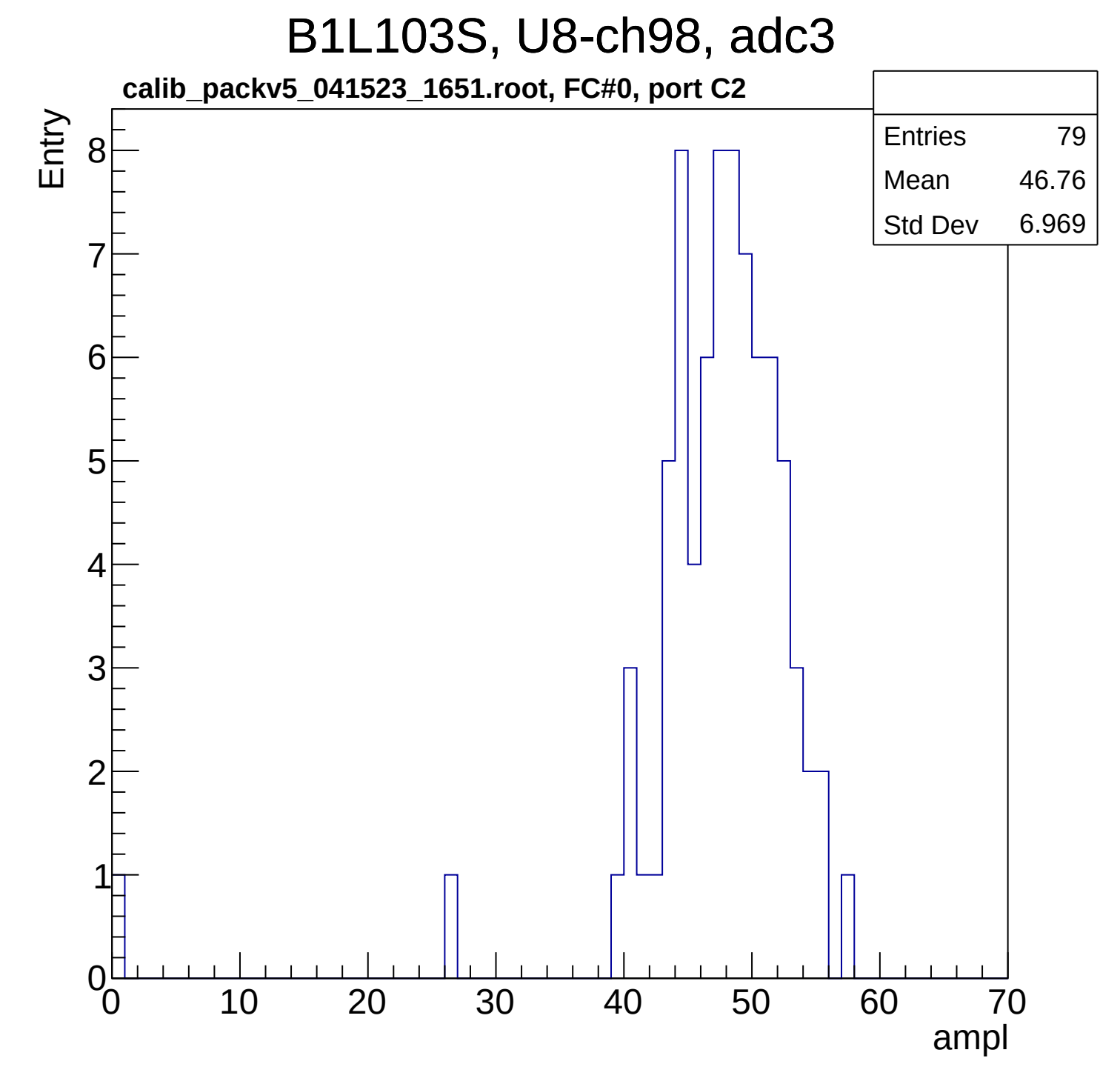
40
50
60
70


B1L103S, U8-ch98, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 46.76
Std Dev 6.969
Entry
ampl
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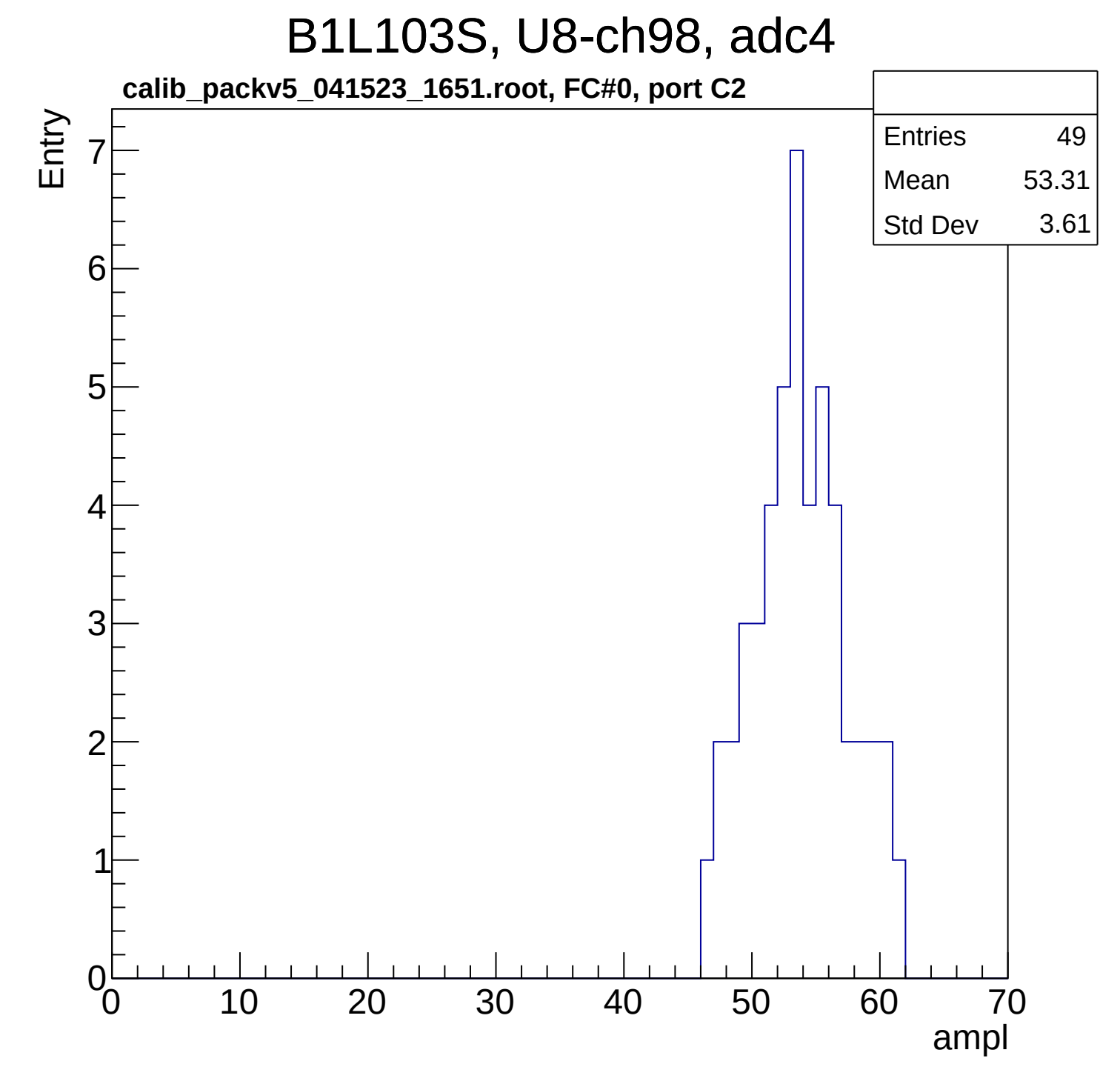
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch98, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 53.31
Std Dev 3.61
Entry
ampl
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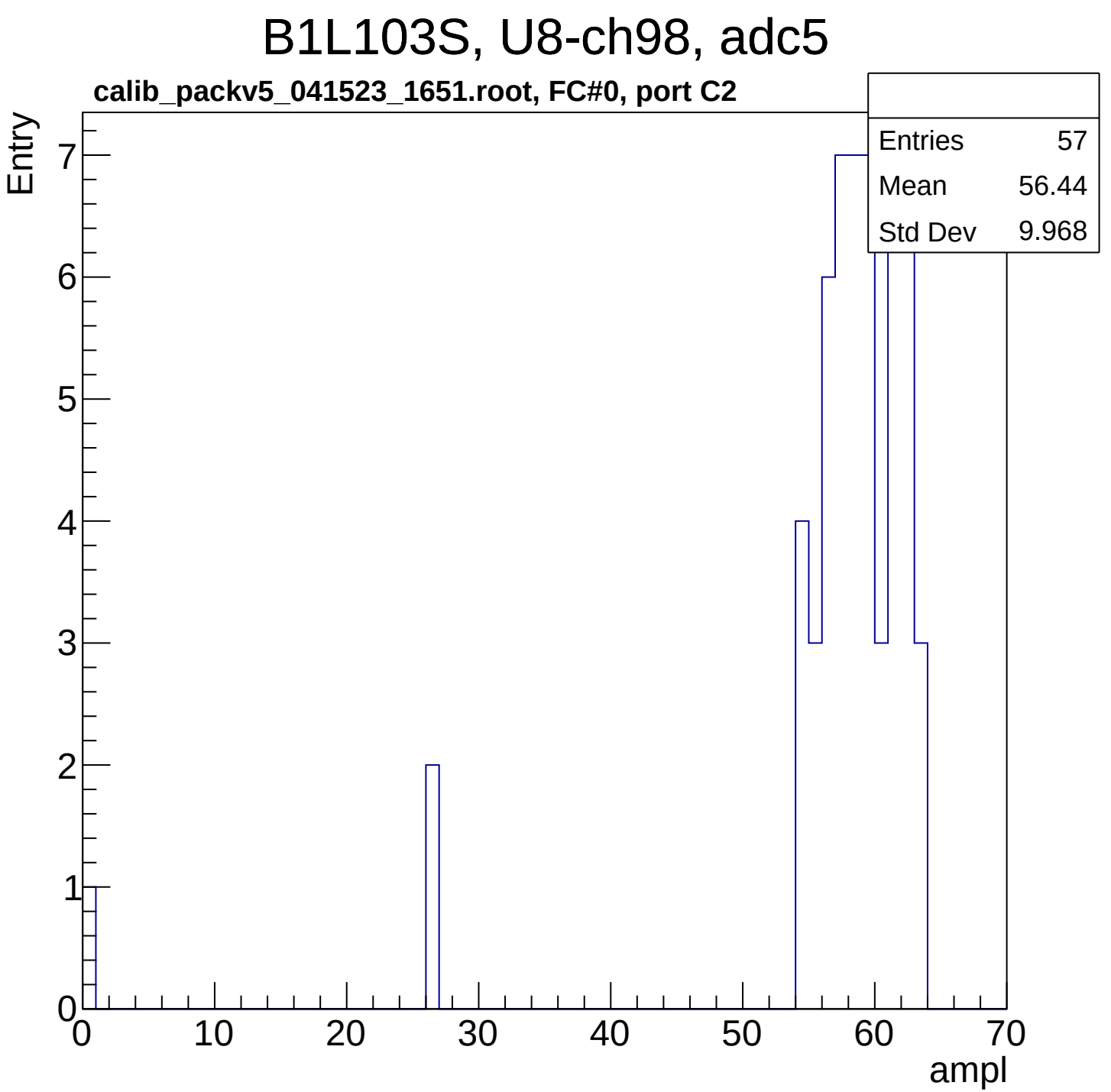
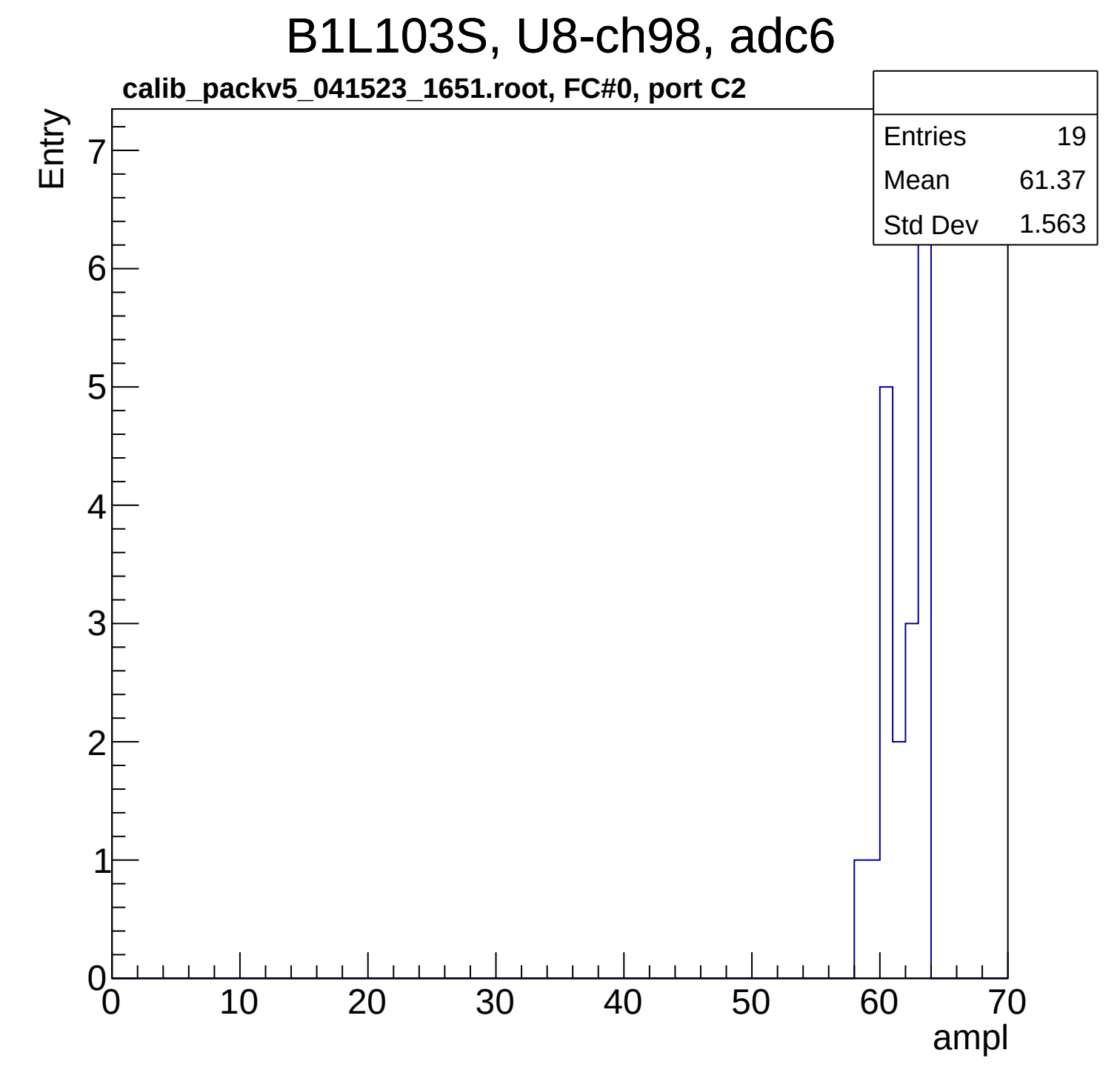
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U8-ch98, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 56.44
Std Dev 9.968
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U8-ch98, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 61.37
Std Dev 1.563
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
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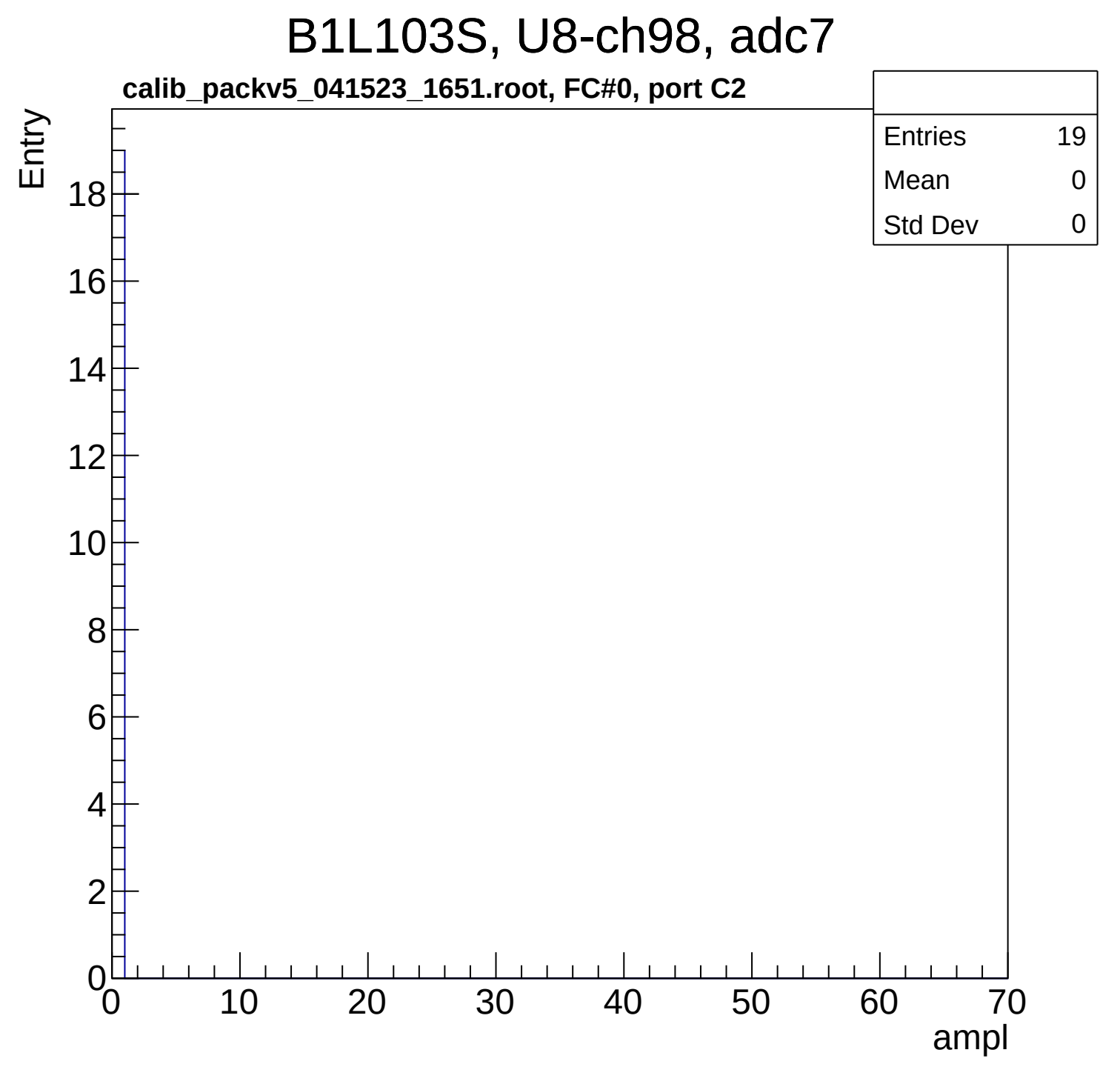
40
50
60
70


B1L103S, U8-ch98, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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8
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14
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18
0
10
20
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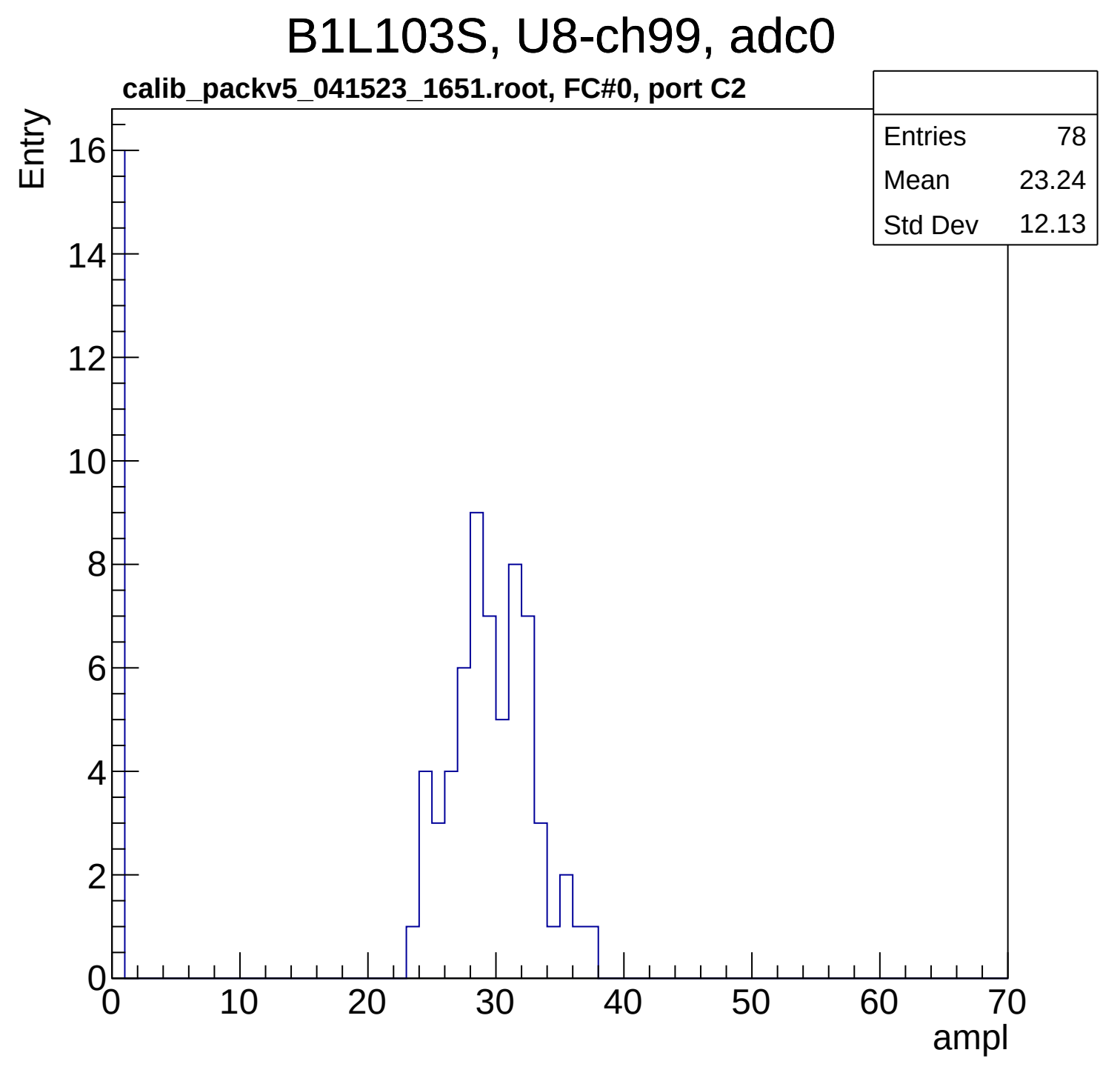
50
60
70
ampl


B1L103S, U8-ch99, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 23.24
Std Dev 12.13
Entry
ampl
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4
6
8
10
12
14
16
0
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40
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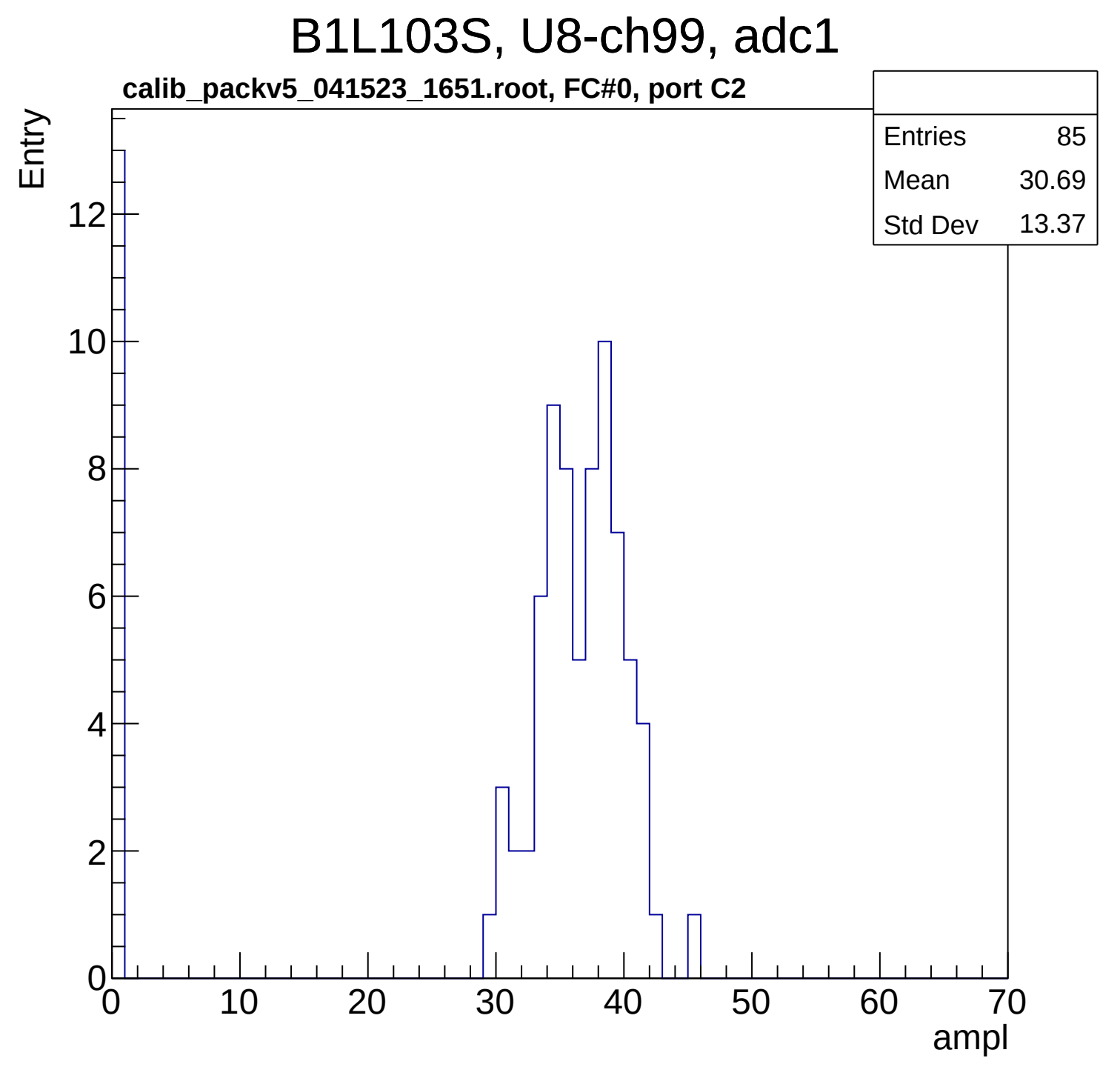
B1L103S, U8-ch99, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 30.69
Std Dev 13.37
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
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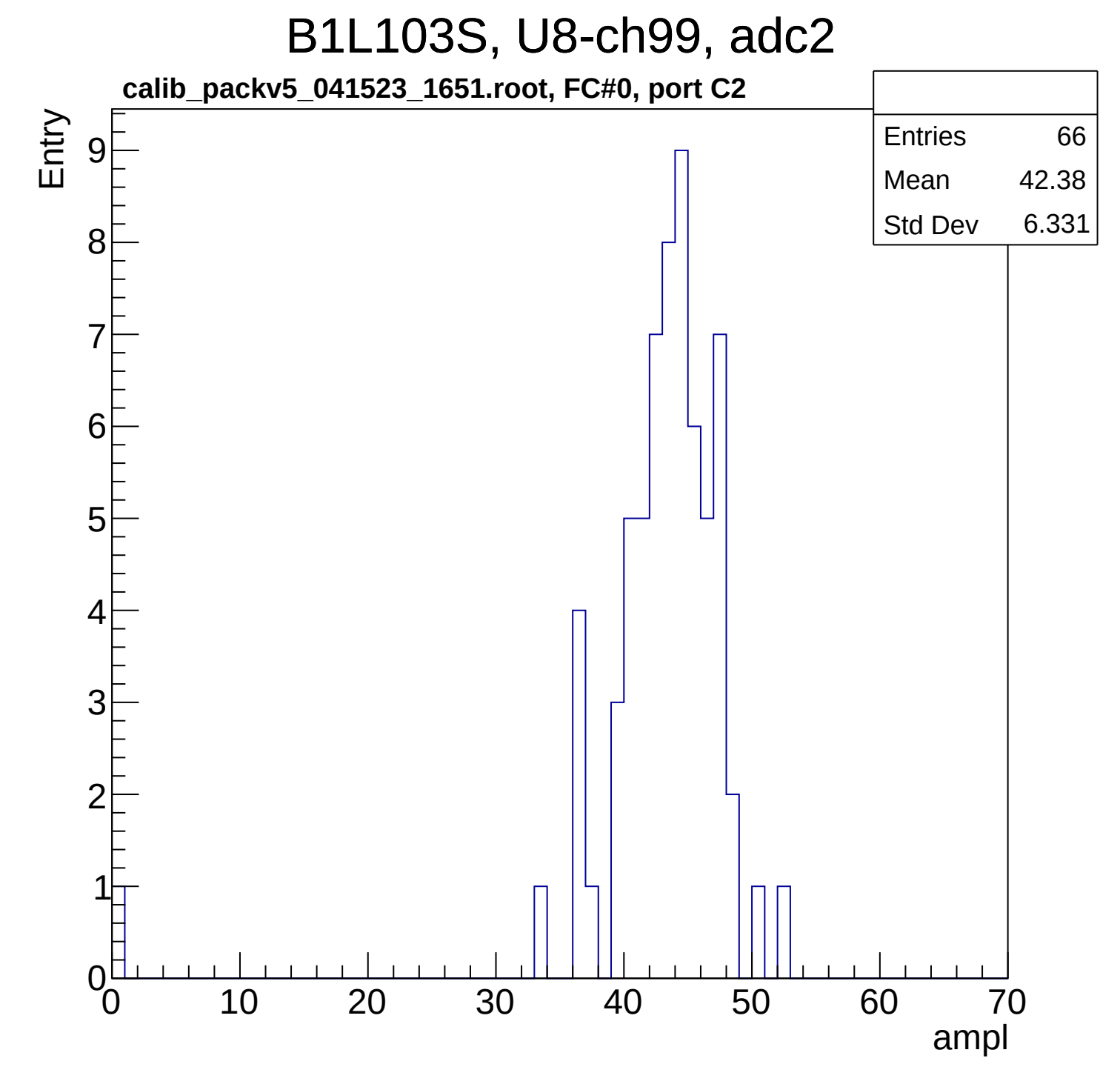
B1L103S, U8-ch99, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 42.38
Std Dev 6.331
Entry
ampl
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2
3
4
5
6
7
8
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0
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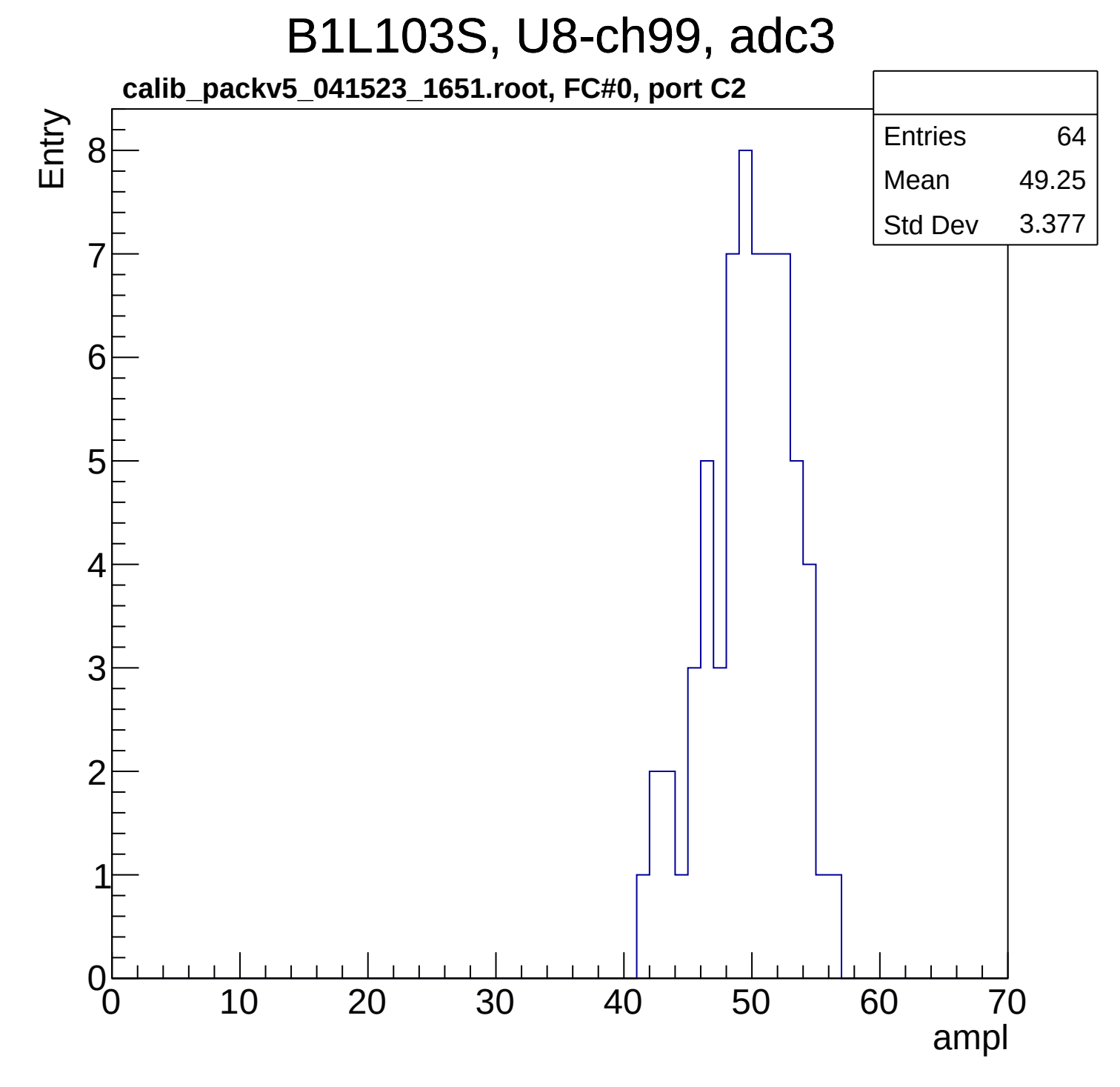
B1L103S, U8-ch99, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 49.25
Std Dev 3.377
Entry
ampl
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2
3
4
5
6
7
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0
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40
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60
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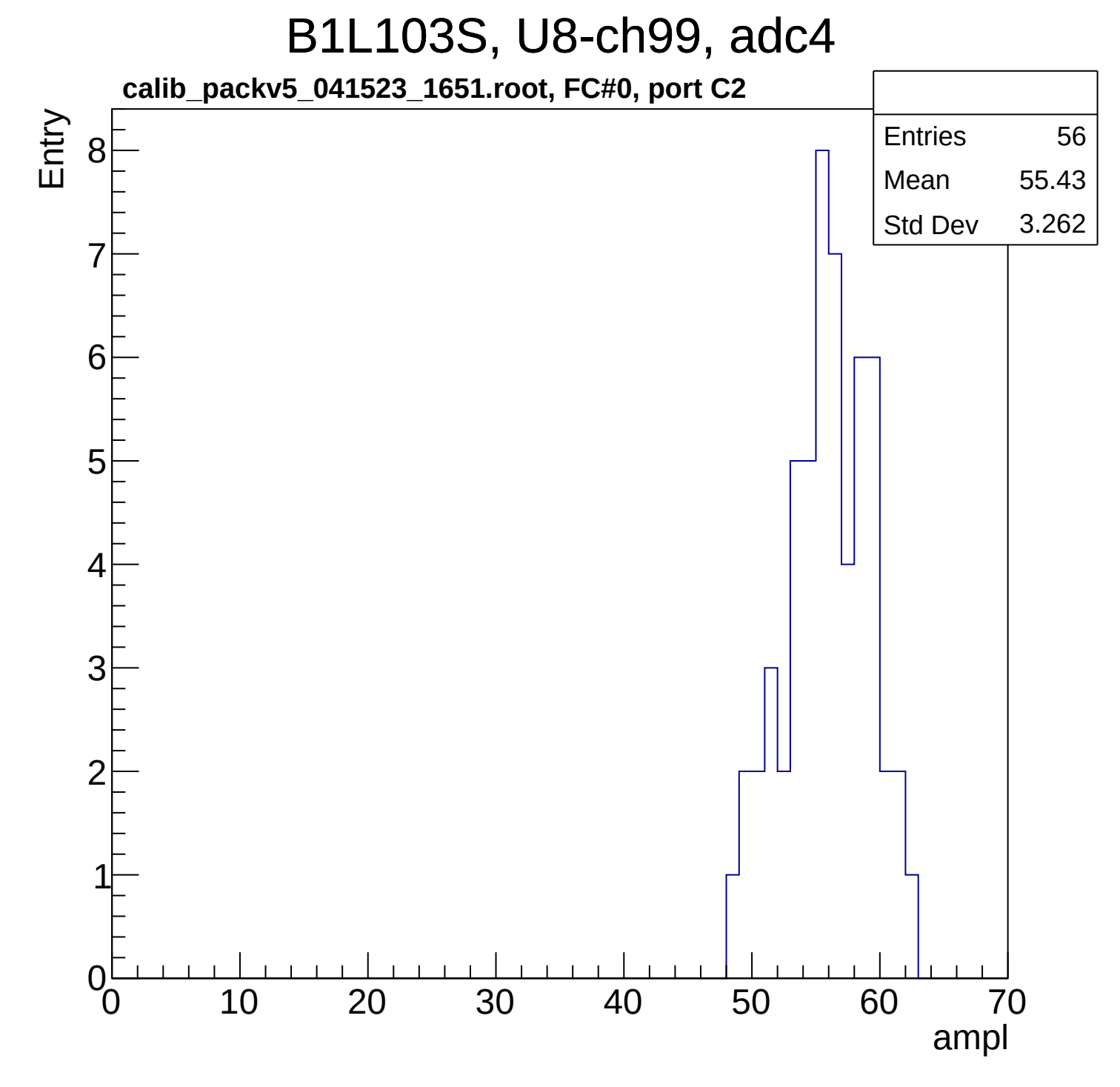
B1L103S, U8-ch99, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 55.43
Std Dev 3.262
Entry
ampl
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2
3
4
5
6
7
8
0
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40
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60
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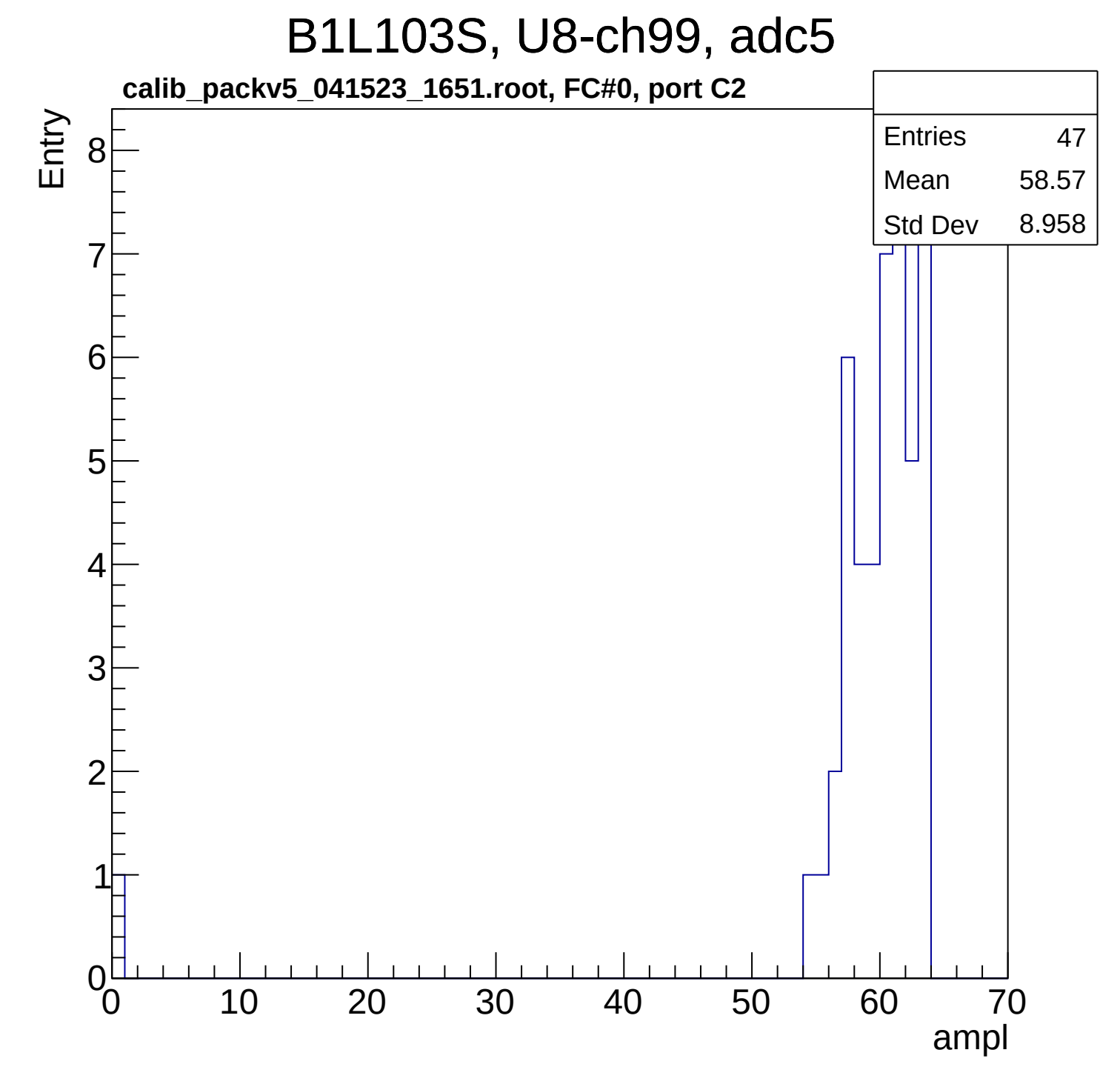
B1L103S, U8-ch99, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 58.57
Std Dev 8.958
Entry
ampl
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3
4
5
6
7
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0
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60
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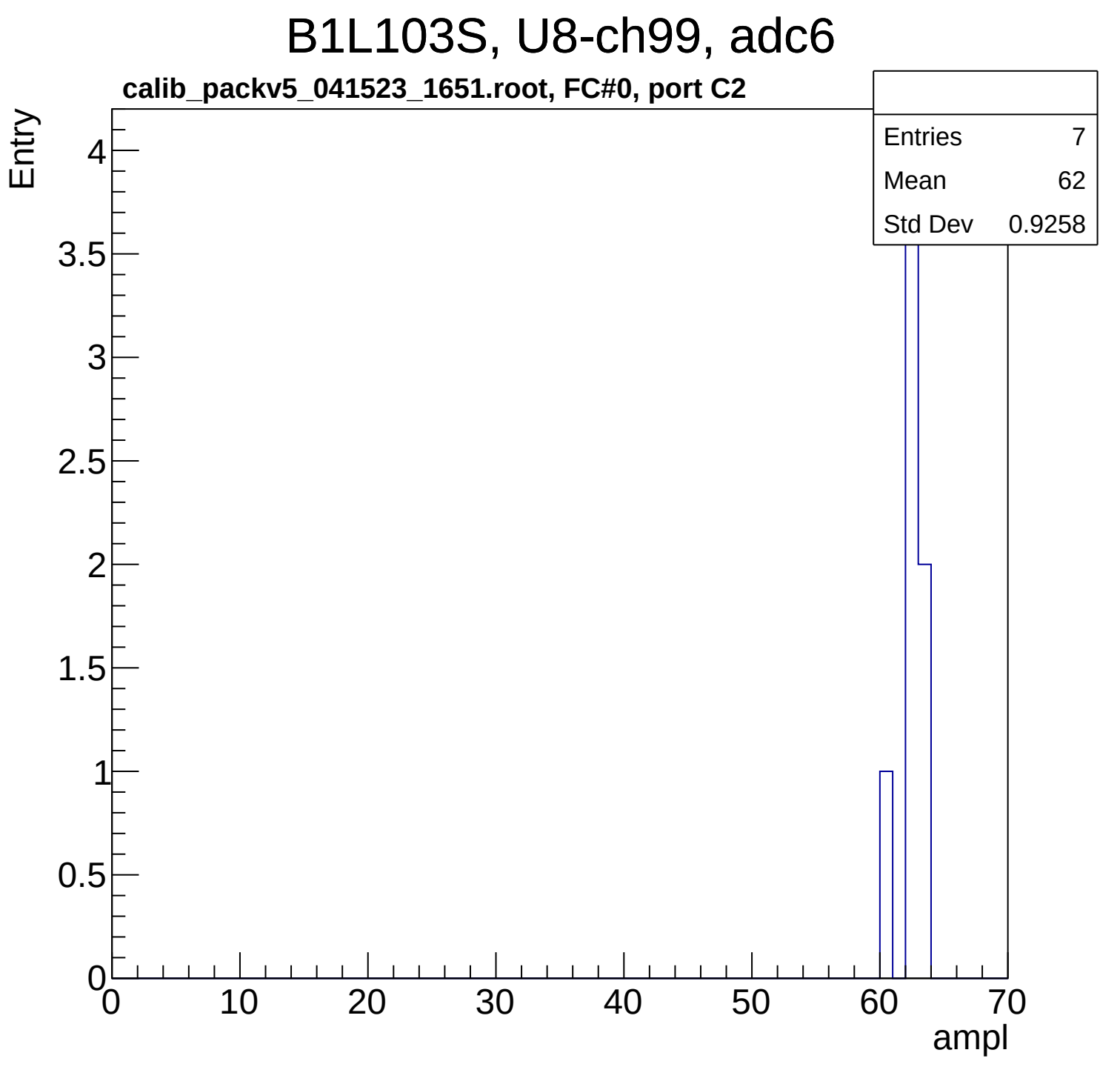
B1L103S, U8-ch99, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 62
Std Dev 0.9258
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
10
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60
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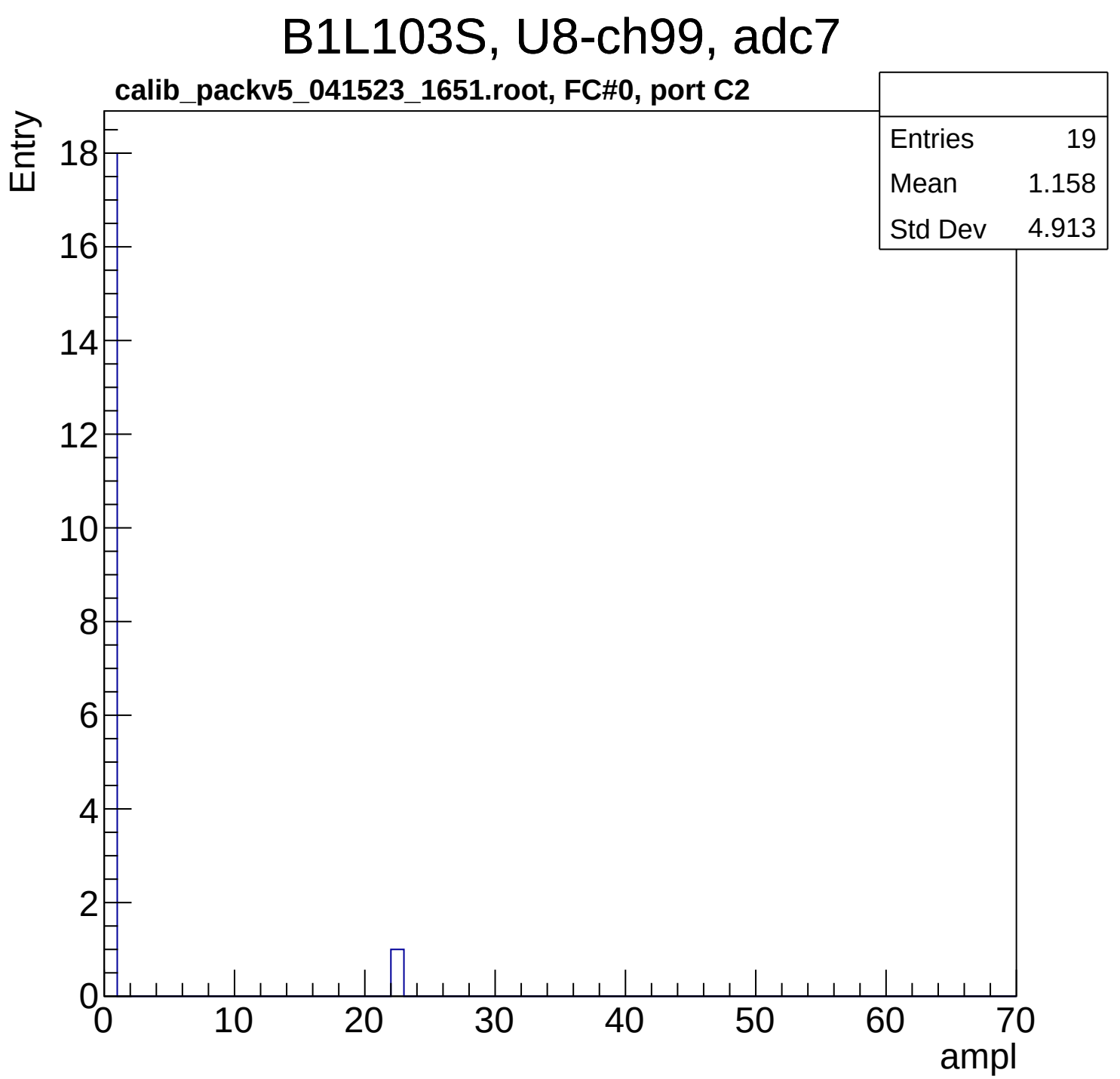
B1L103S, U8-ch99, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.158
Std Dev 4.913
Entry
0
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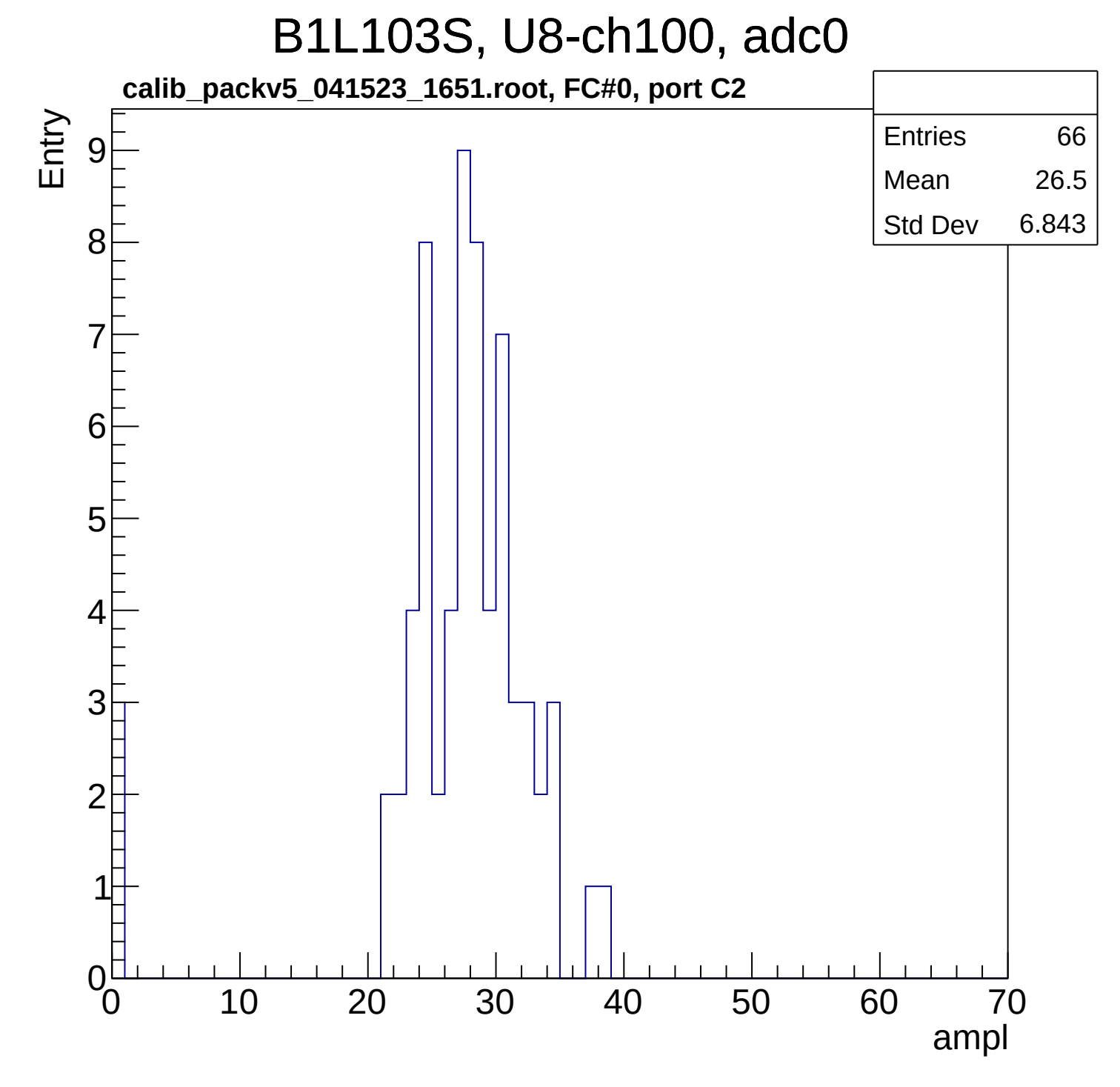
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch100, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 26.5
Std Dev 6.843
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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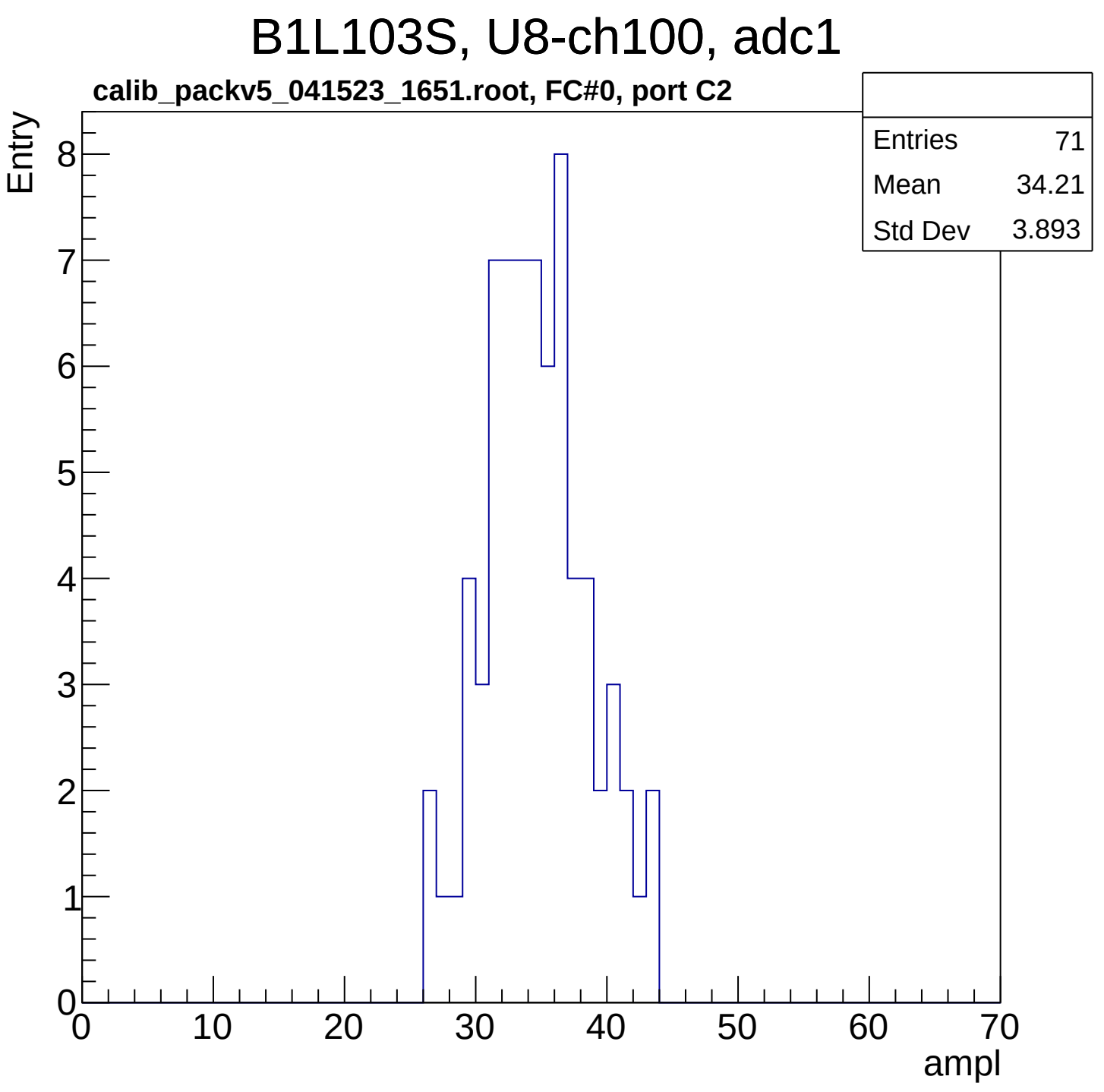
40
50
60
70


B1L103S, U8-ch100, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 34.21
Std Dev 3.893
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
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60
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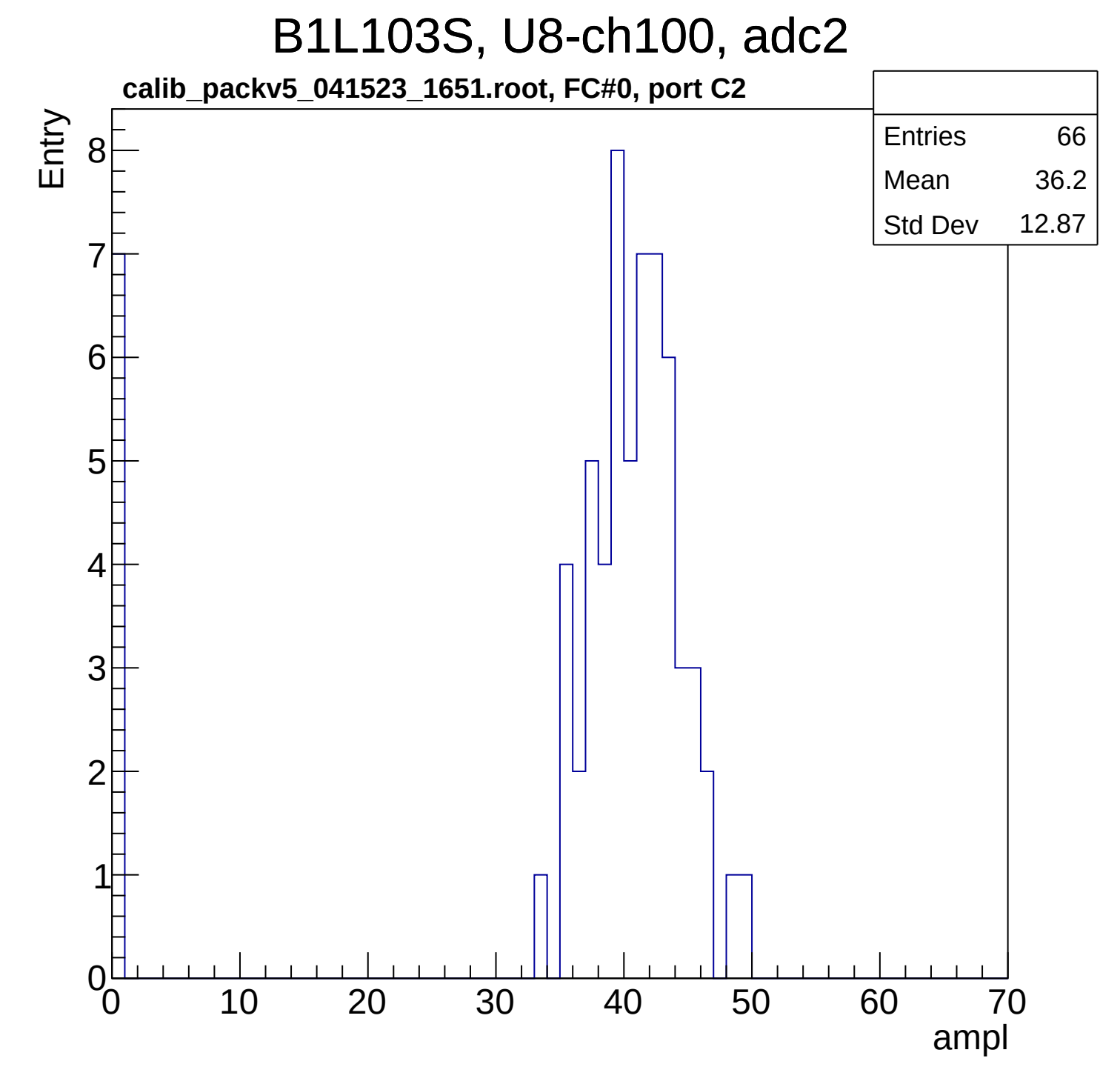
B1L103S, U8-ch100, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 36.2
Std Dev 12.87
Entry
ampl
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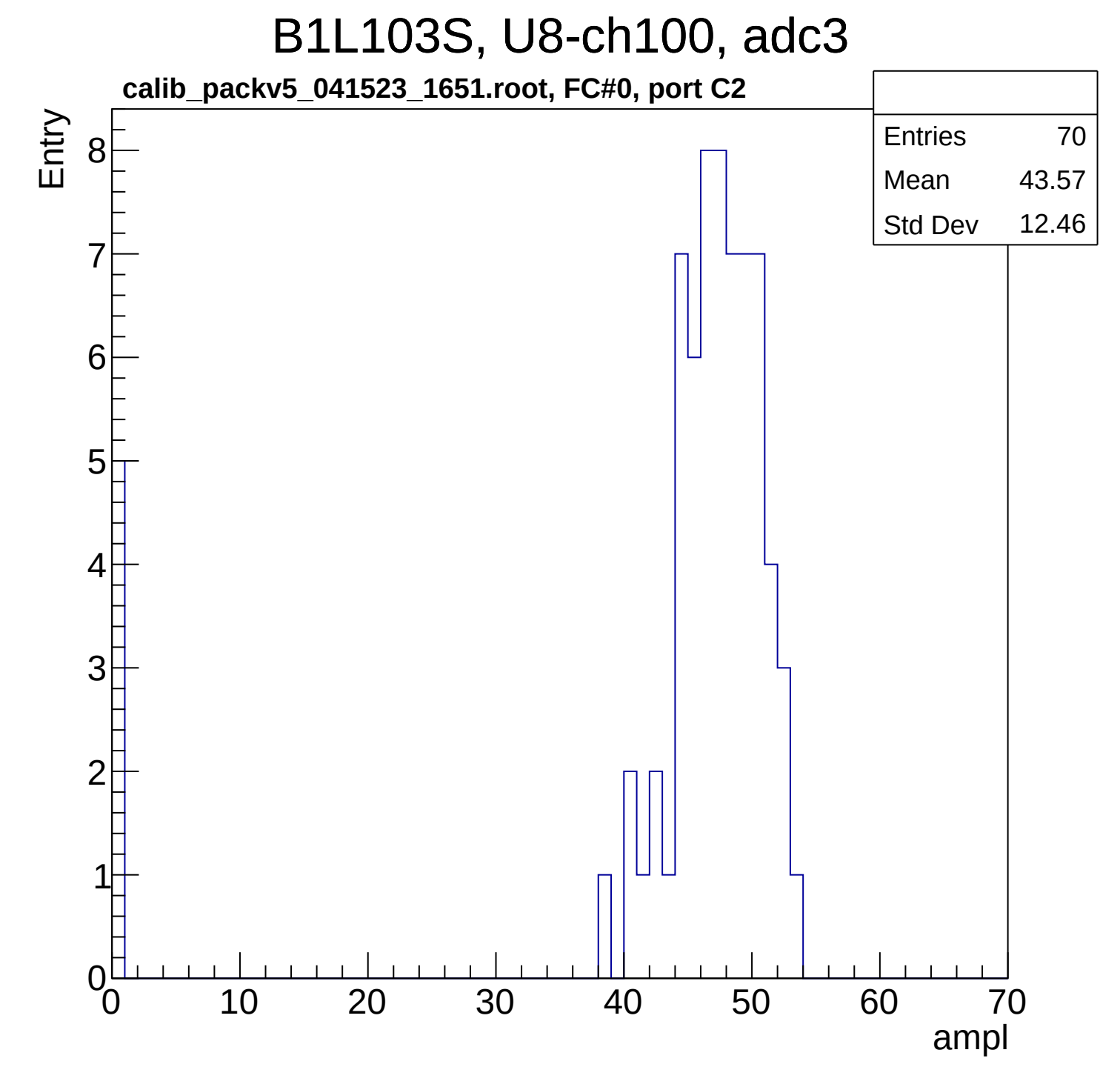
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch100, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 43.57
Std Dev 12.46
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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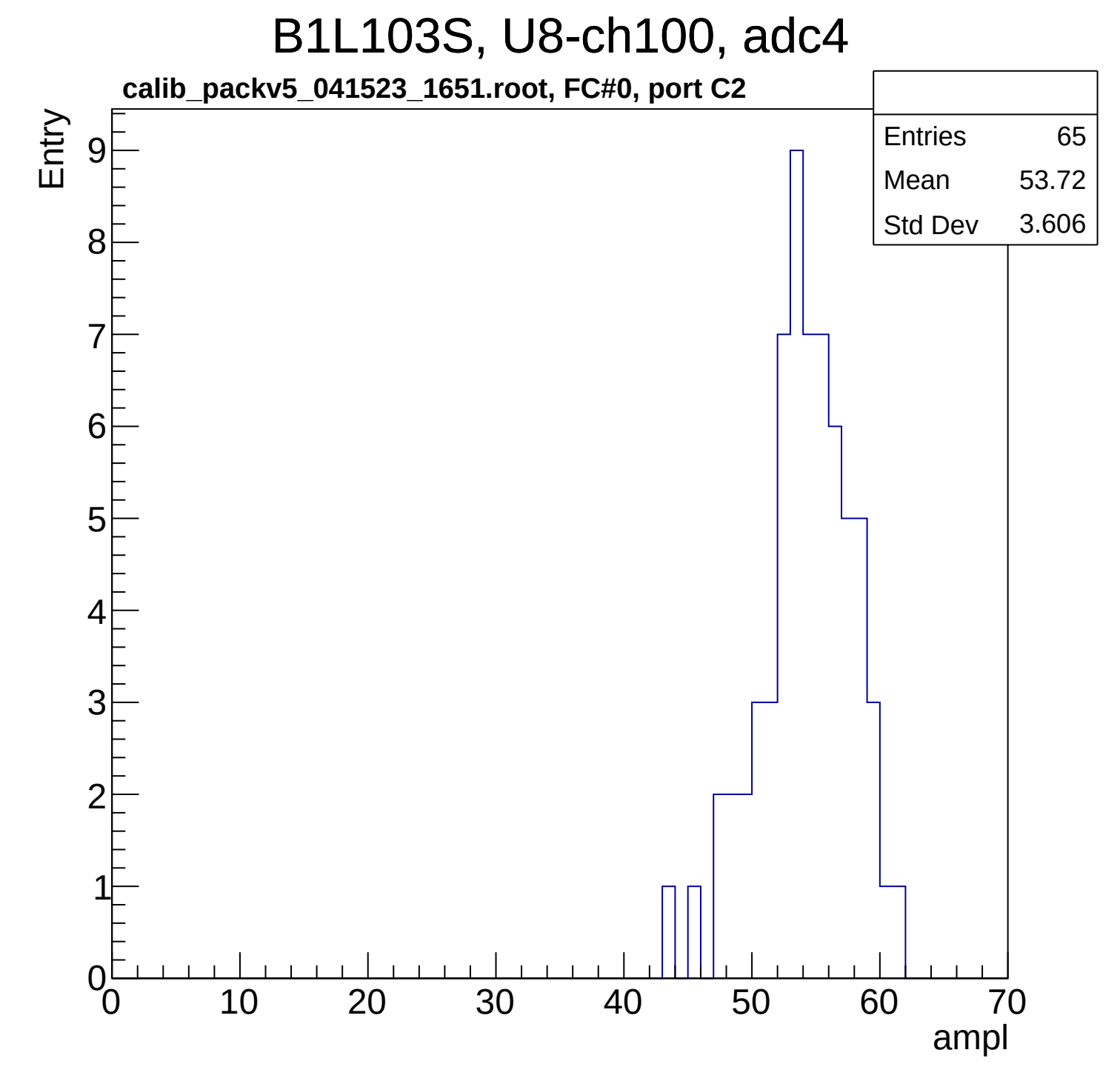
40
50
60
70


B1L103S, U8-ch100, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 53.72
Std Dev 3.606
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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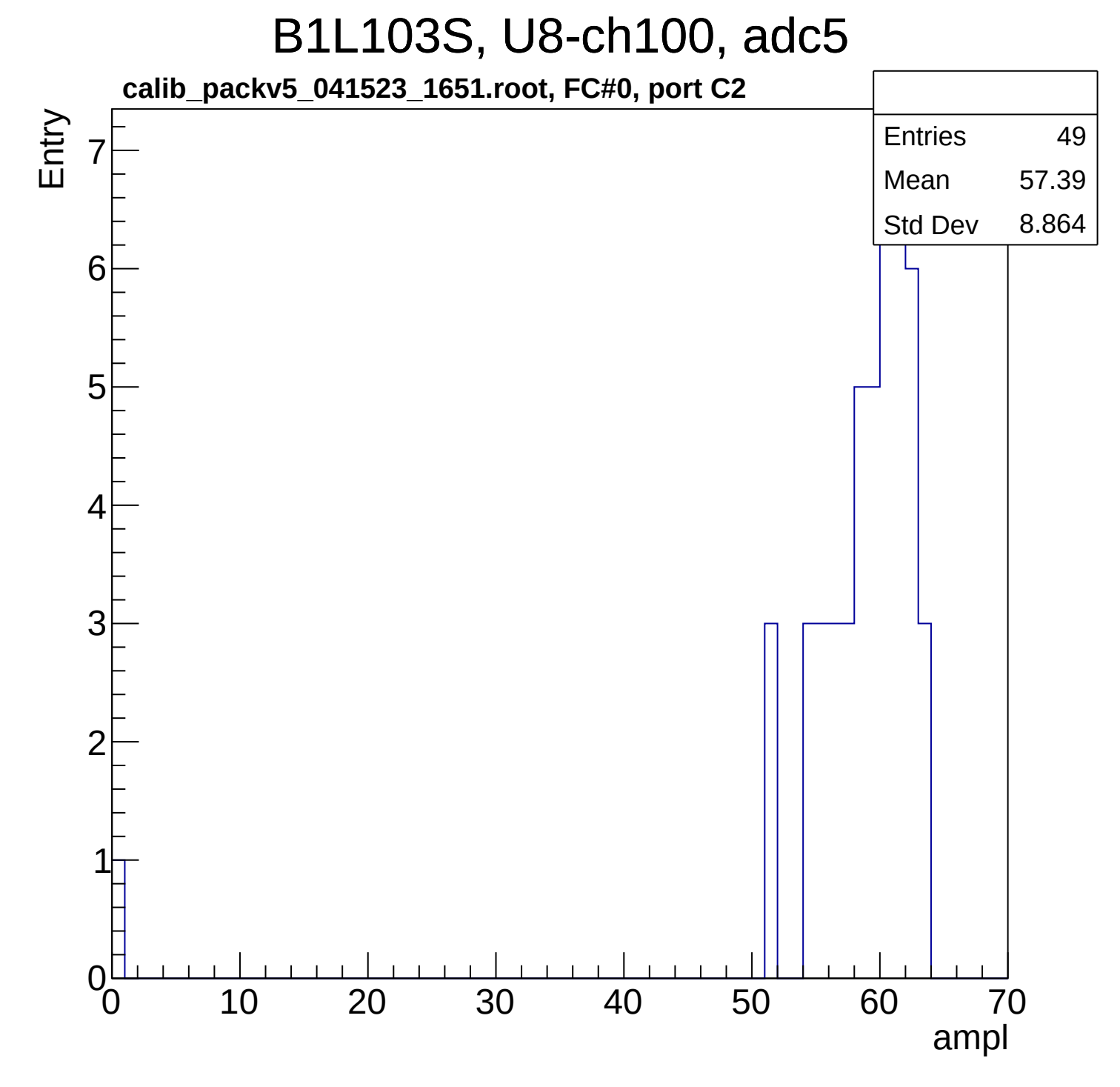
B1L103S, U8-ch100, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 57.39
Std Dev 8.864
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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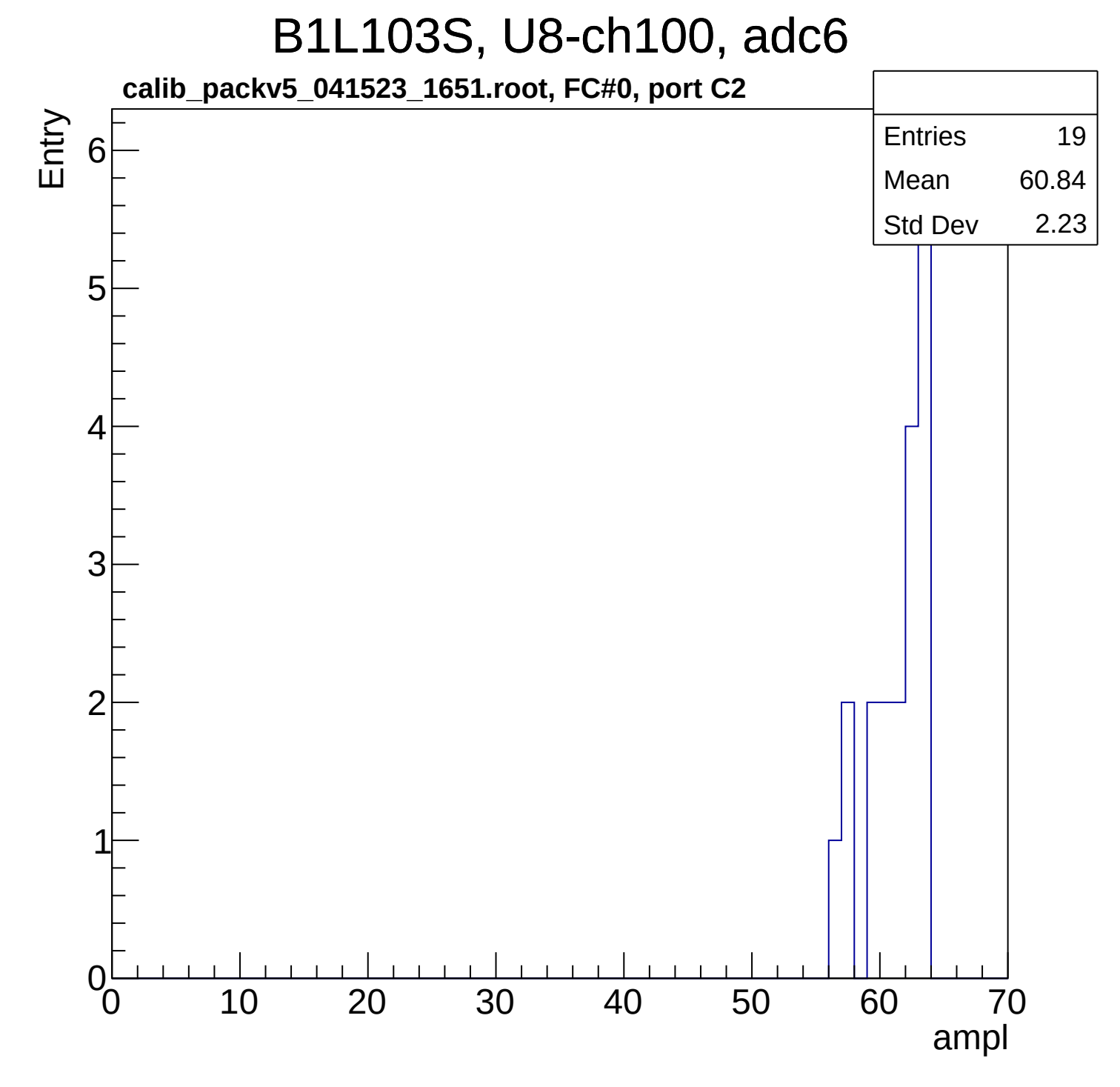
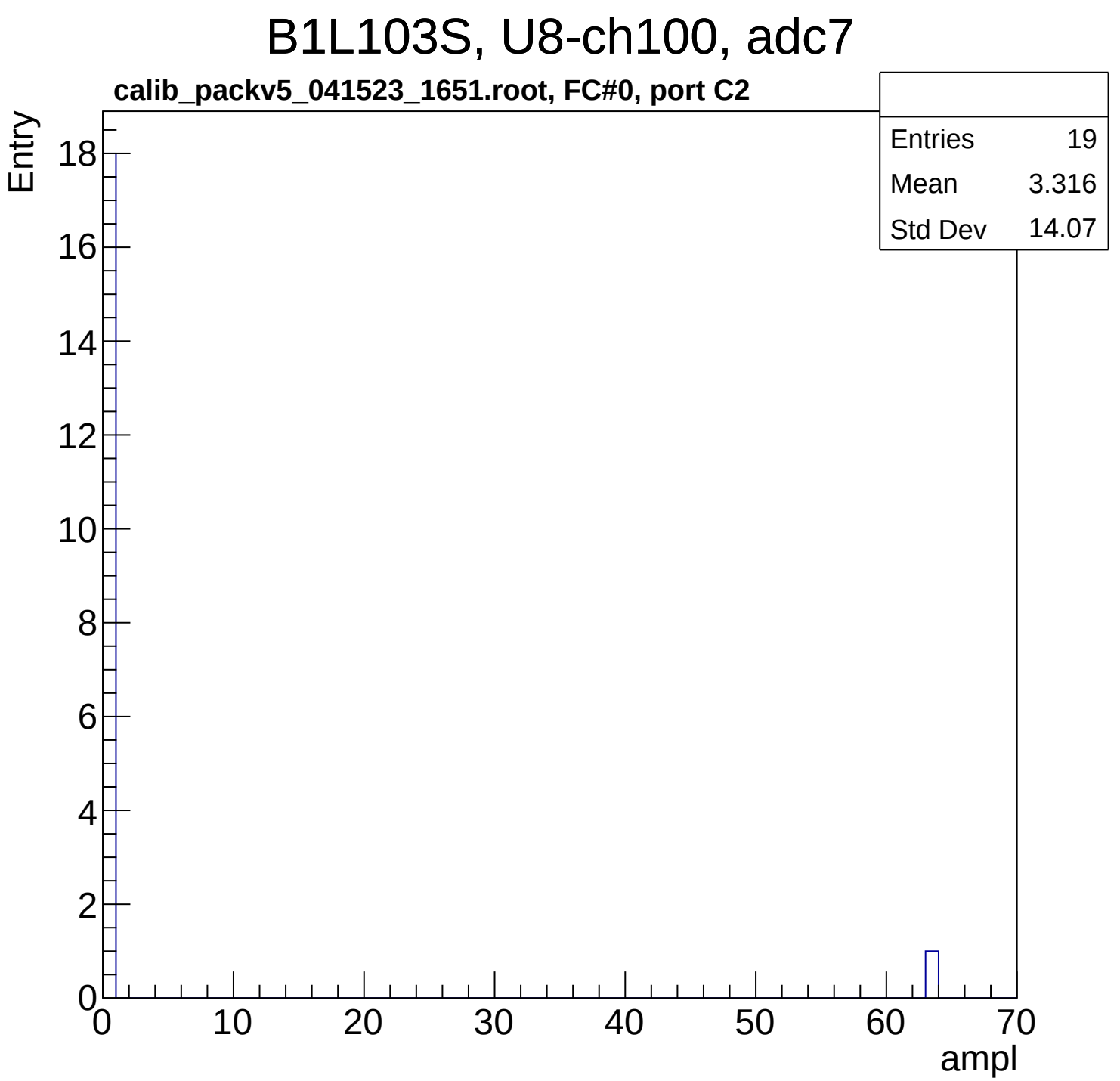

B1L103S, U8-ch100, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 60.84
Std Dev 2.23
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U8-ch100, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.316
Std Dev 14.07
Entry
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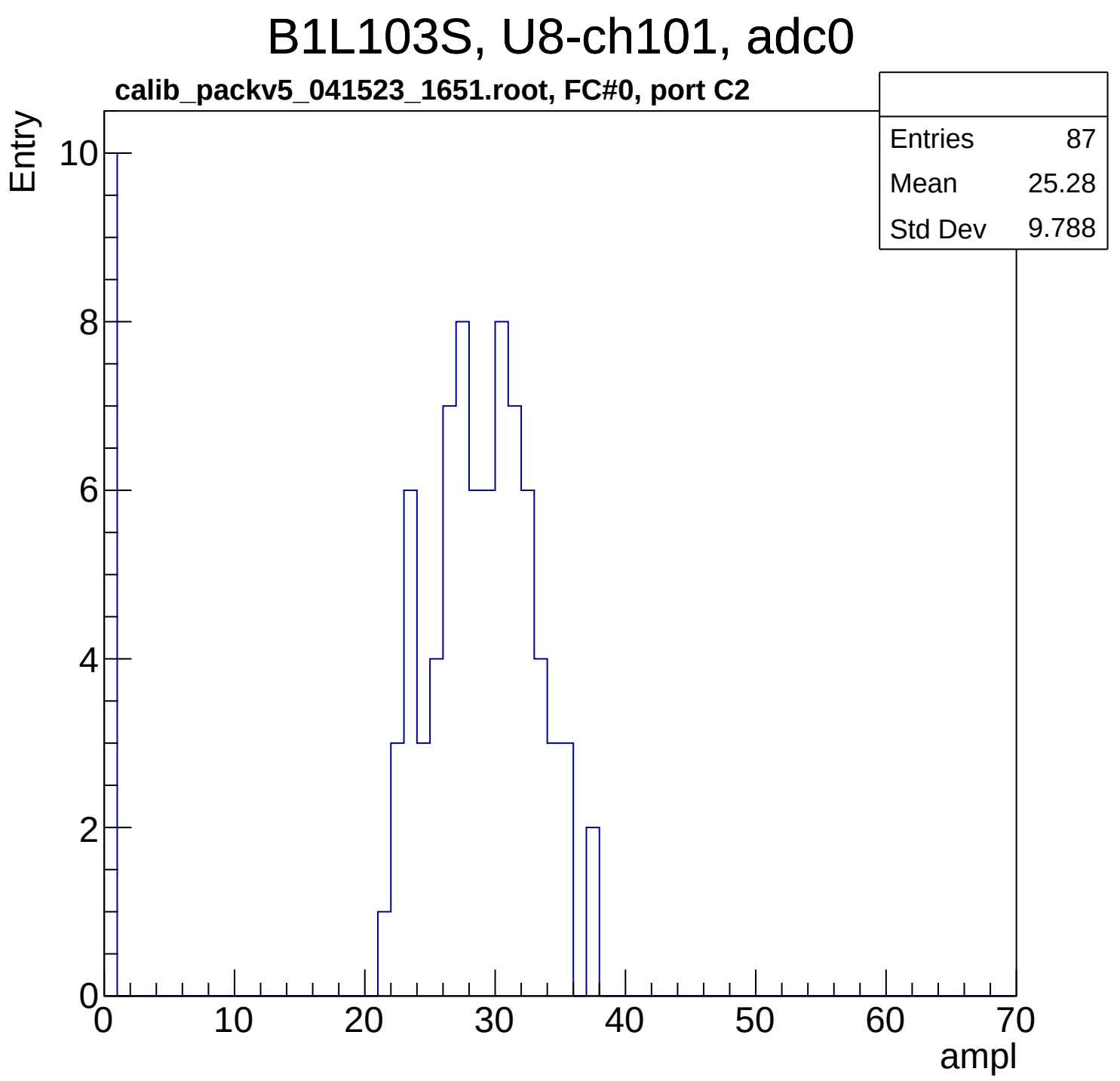
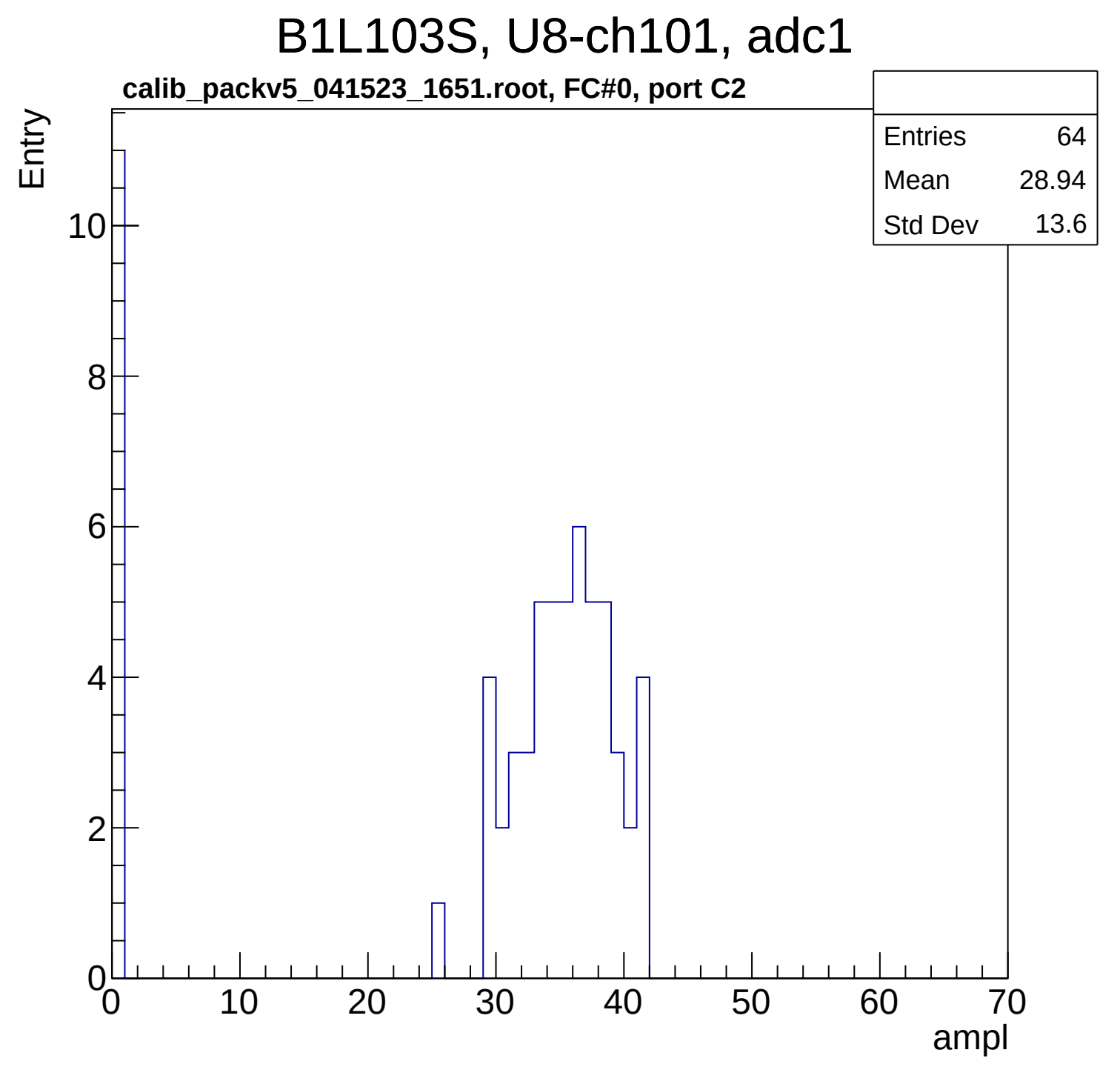
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch101, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 25.28
Std Dev 9.788
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U8-ch101, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 28.94
Std Dev 13.6
Entry
ampl
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4
6
8
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0
10
20
30
40
50
60
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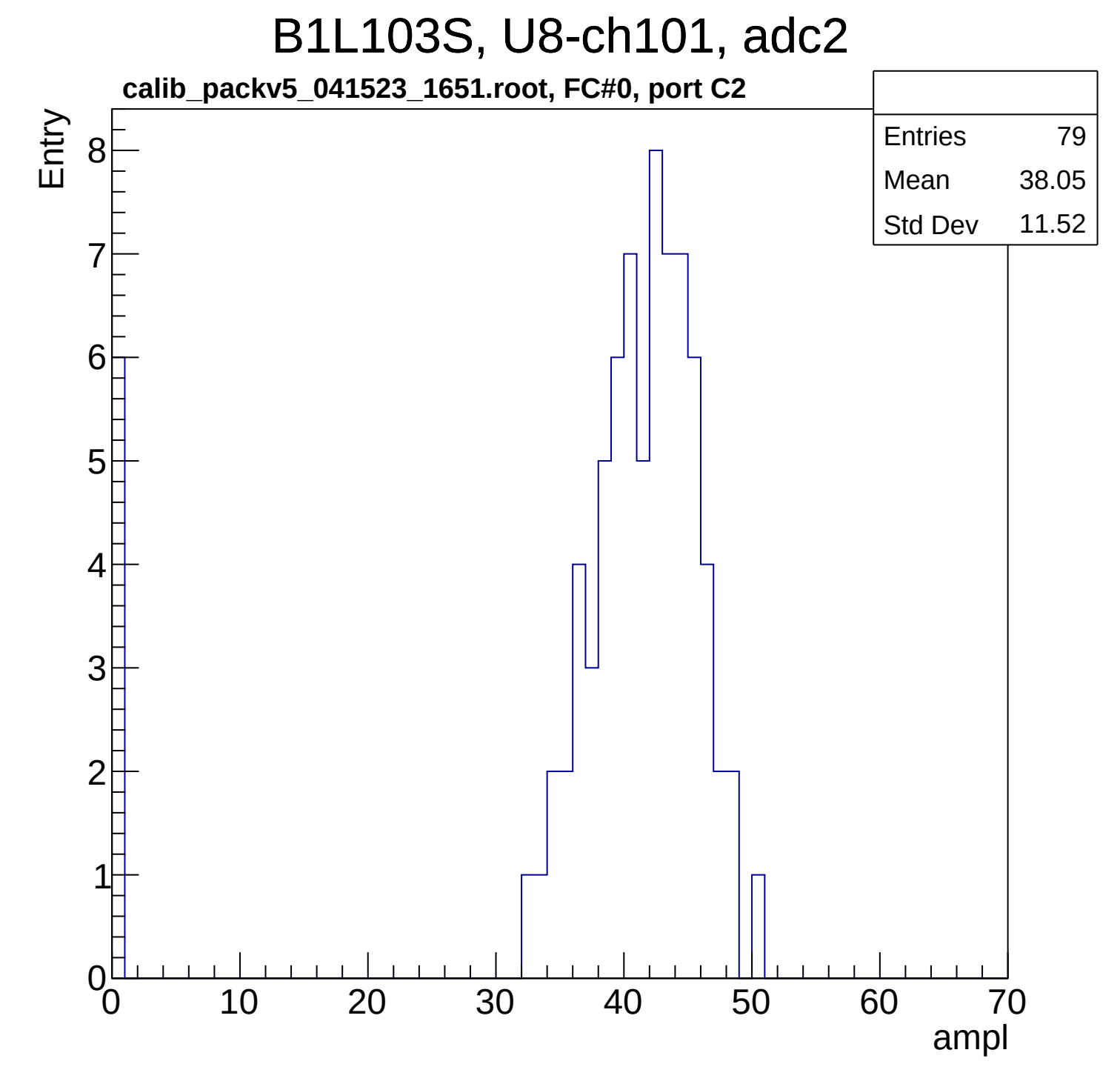
B1L103S, U8-ch101, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 38.05
Std Dev 11.52
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
50
60
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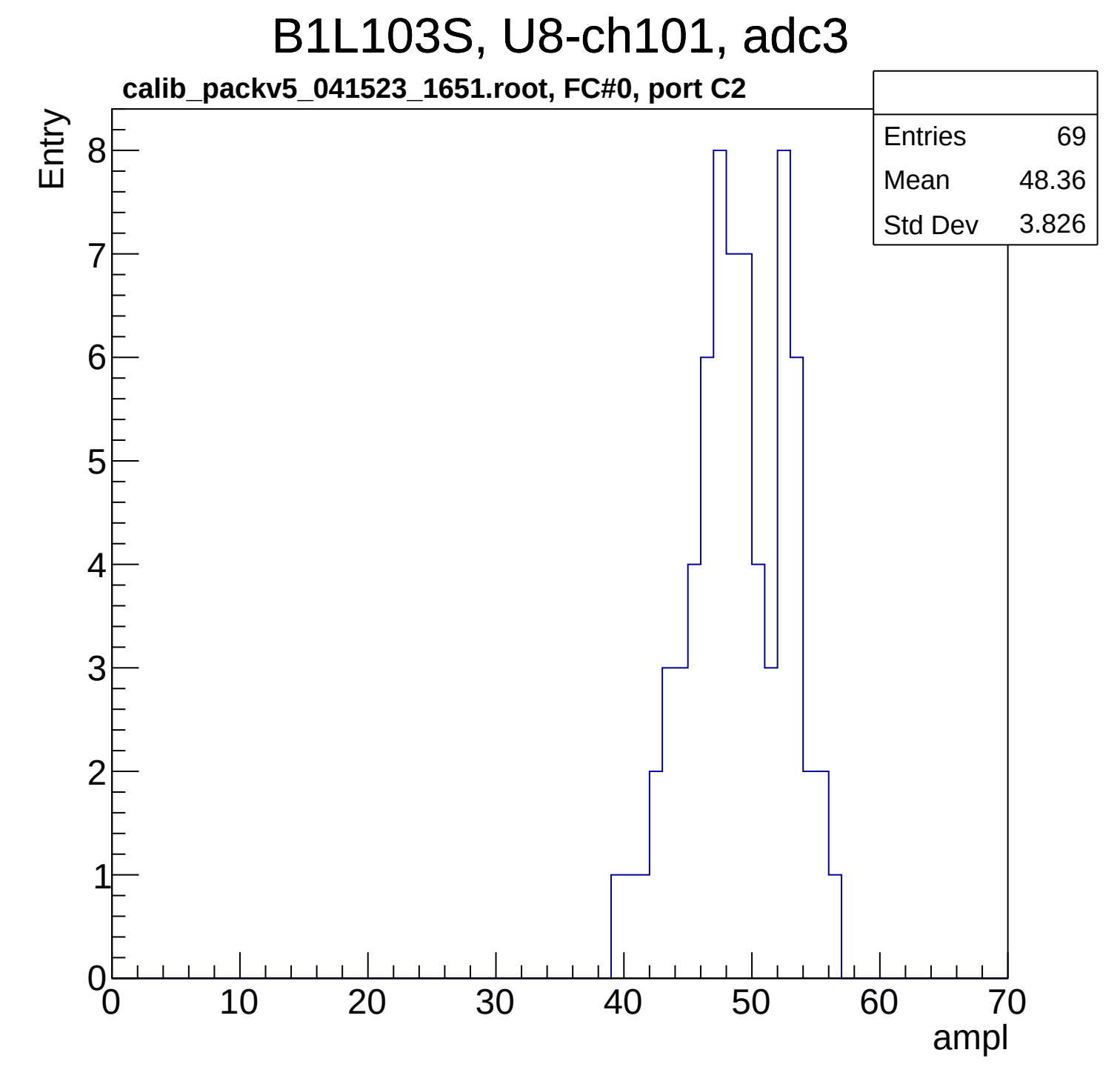
B1L103S, U8-ch101, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 48.36
Std Dev 3.826
Entry
ampl
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2
3
4
5
6
7
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0
10
20
30
40
50
60
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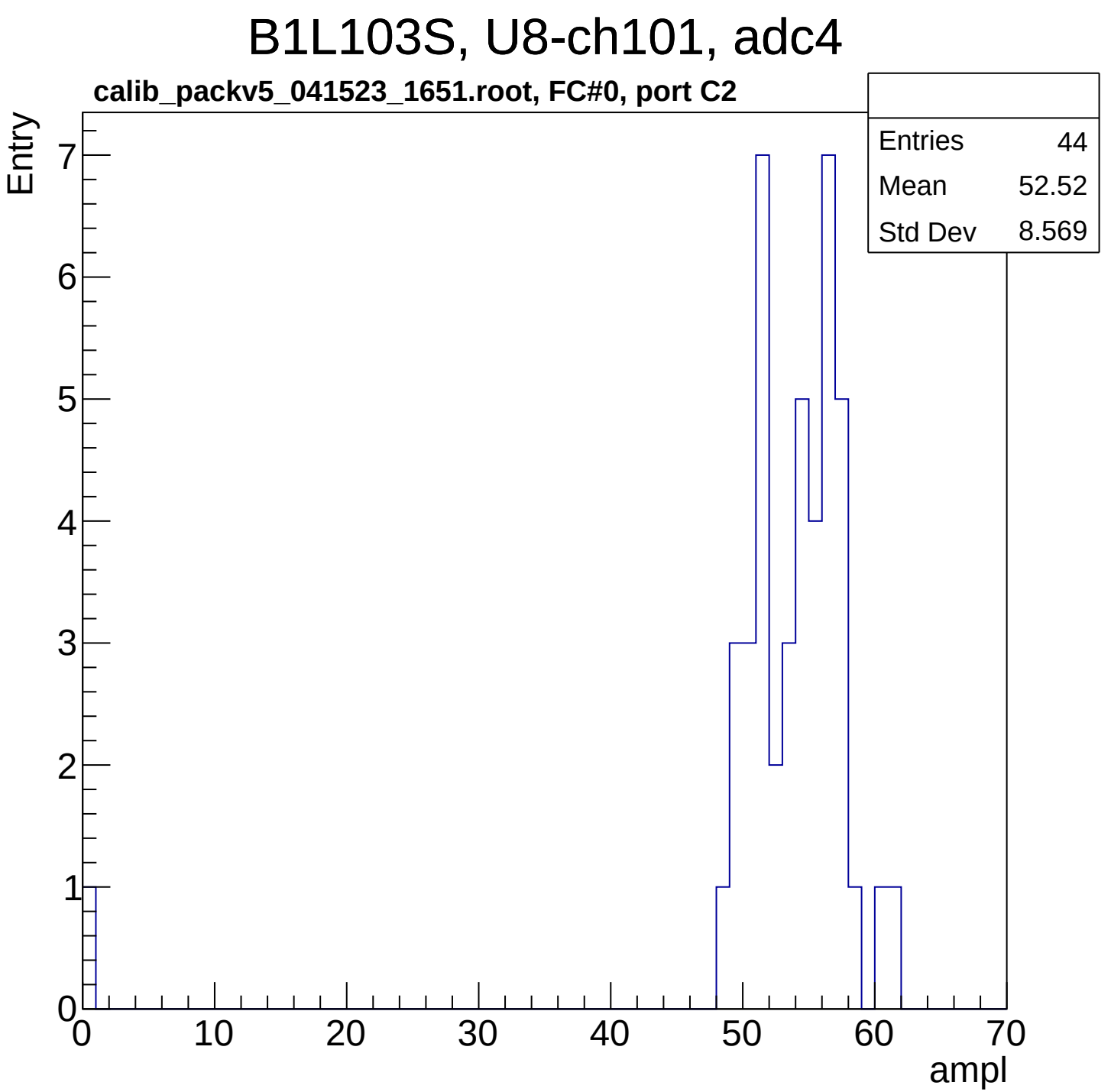
B1L103S, U8-ch101, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 52.52
Std Dev 8.569
Entry
ampl
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1
2
3
4
5
6
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0
10
20
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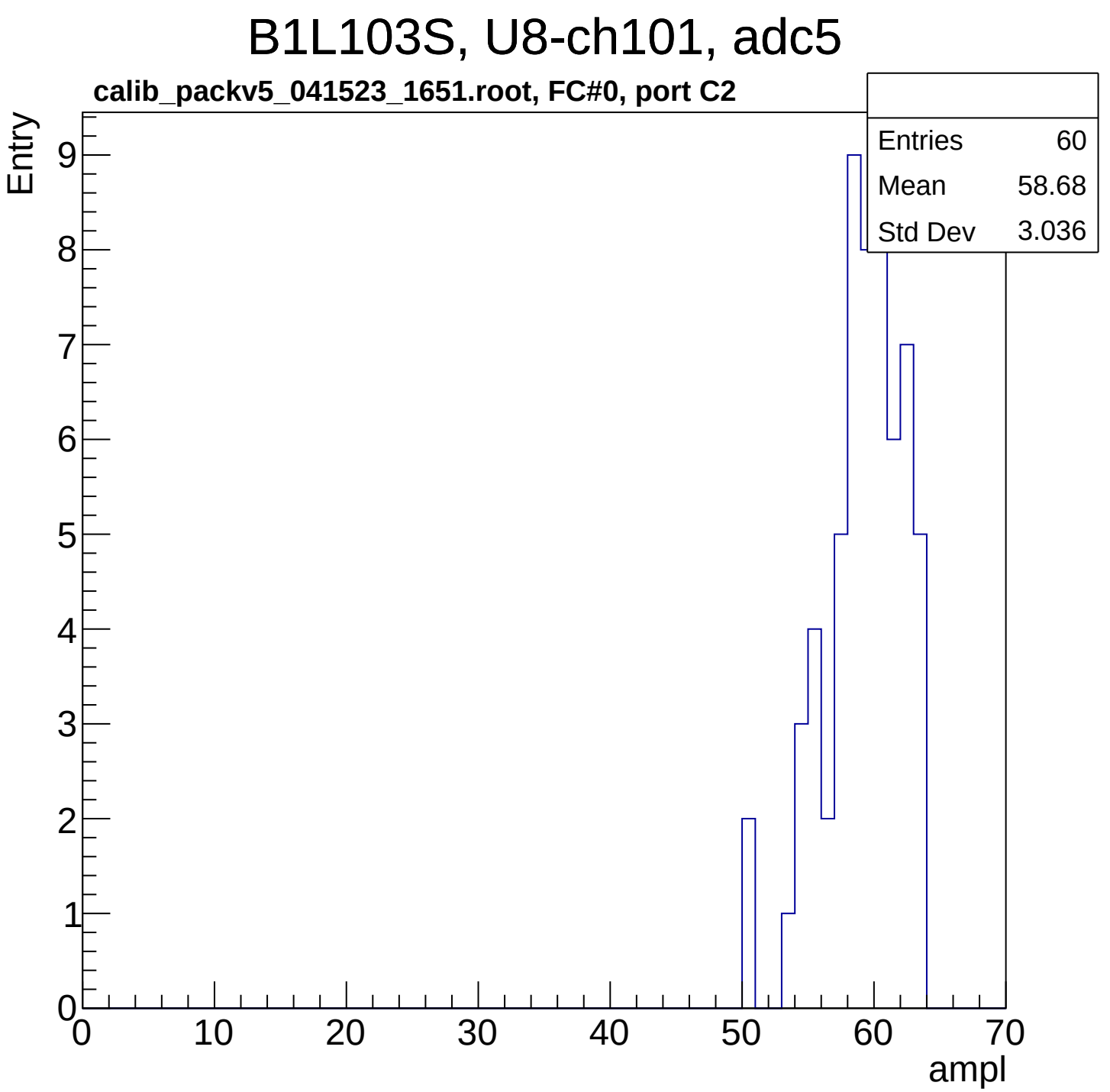
40
50
60
70


B1L103S, U8-ch101, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 58.68
Std Dev 3.036
Entry
ampl
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6
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0
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60
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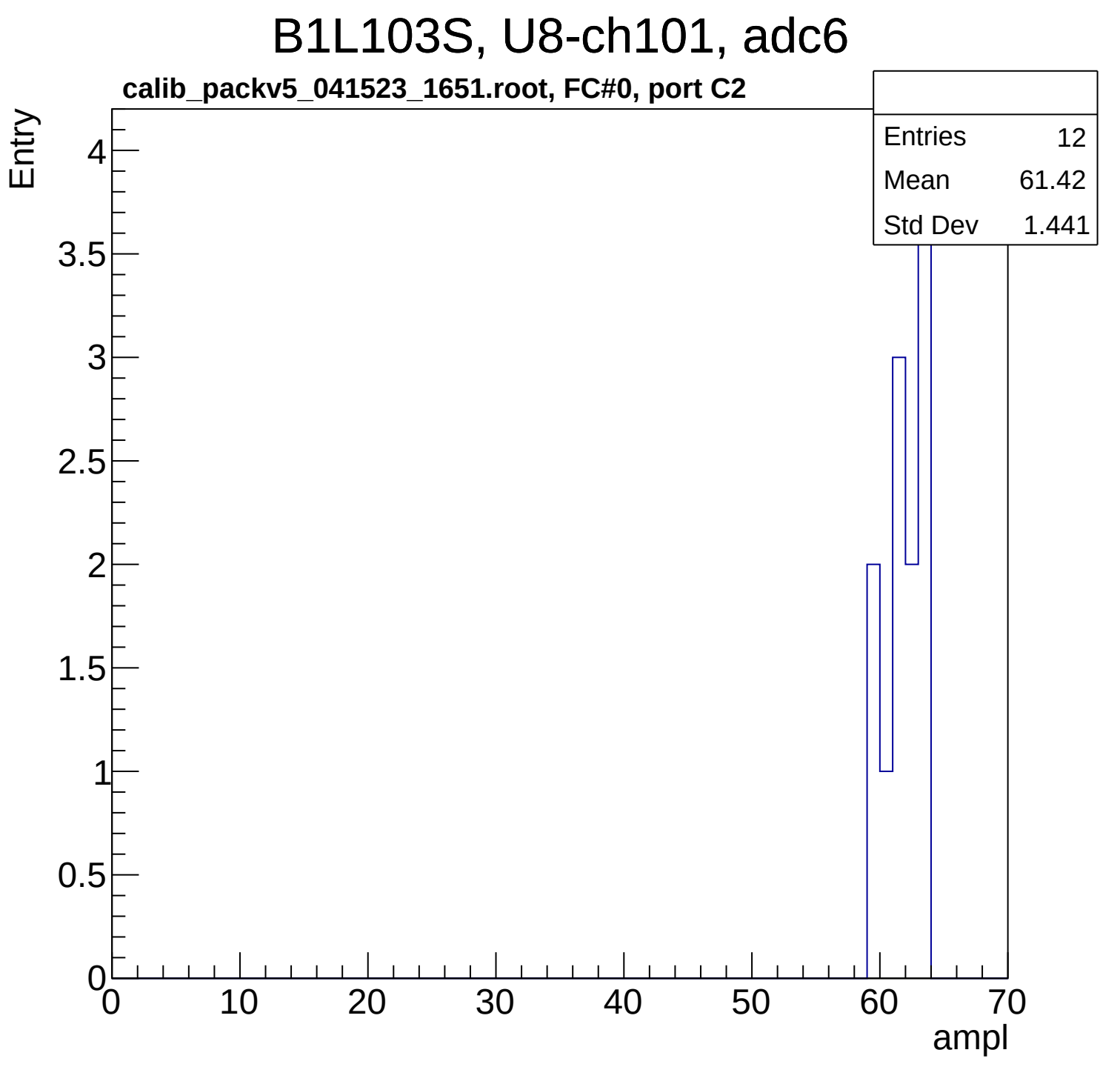
B1L103S, U8-ch101, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.42
Std Dev 1.441
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
10
20
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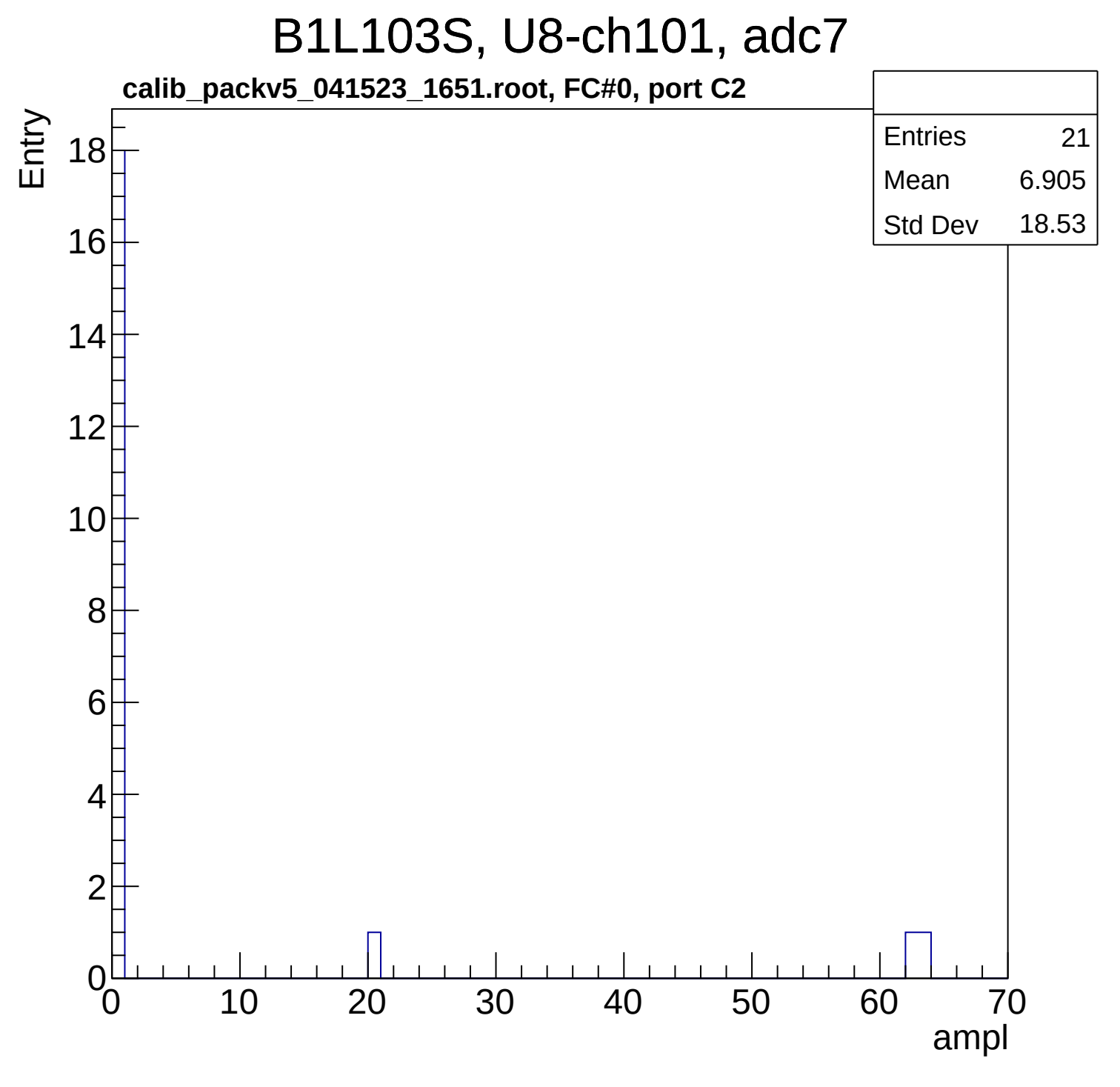
40
50
60
70


B1L103S, U8-ch101, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 6.905
Std Dev 18.53
Entry
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6
8
10
12
14
16
18
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10
20
30
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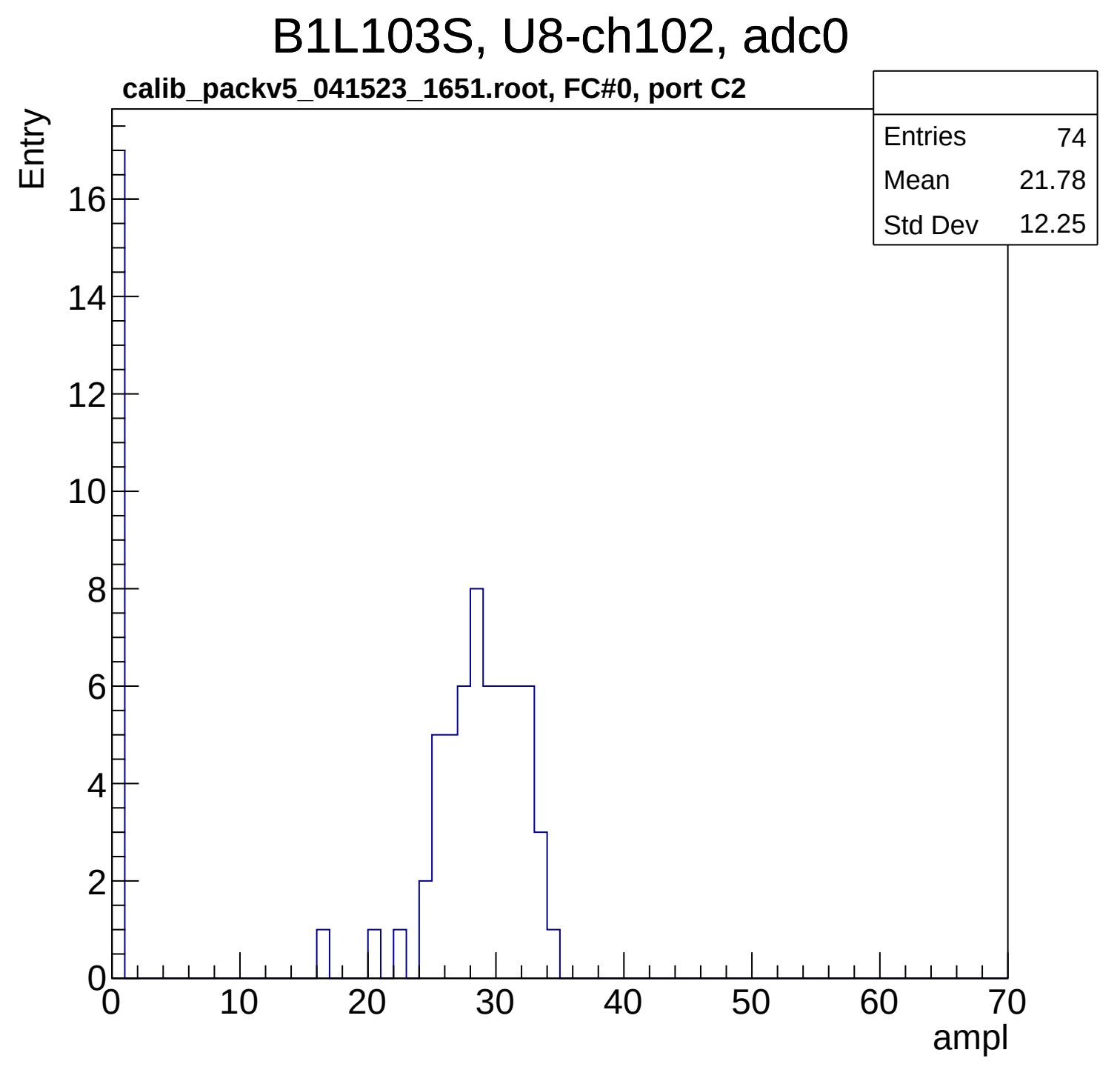
50
60
70
ampl


B1L103S, U8-ch102, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 21.78
Std Dev 12.25
Entry
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4
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8
10
12
14
16
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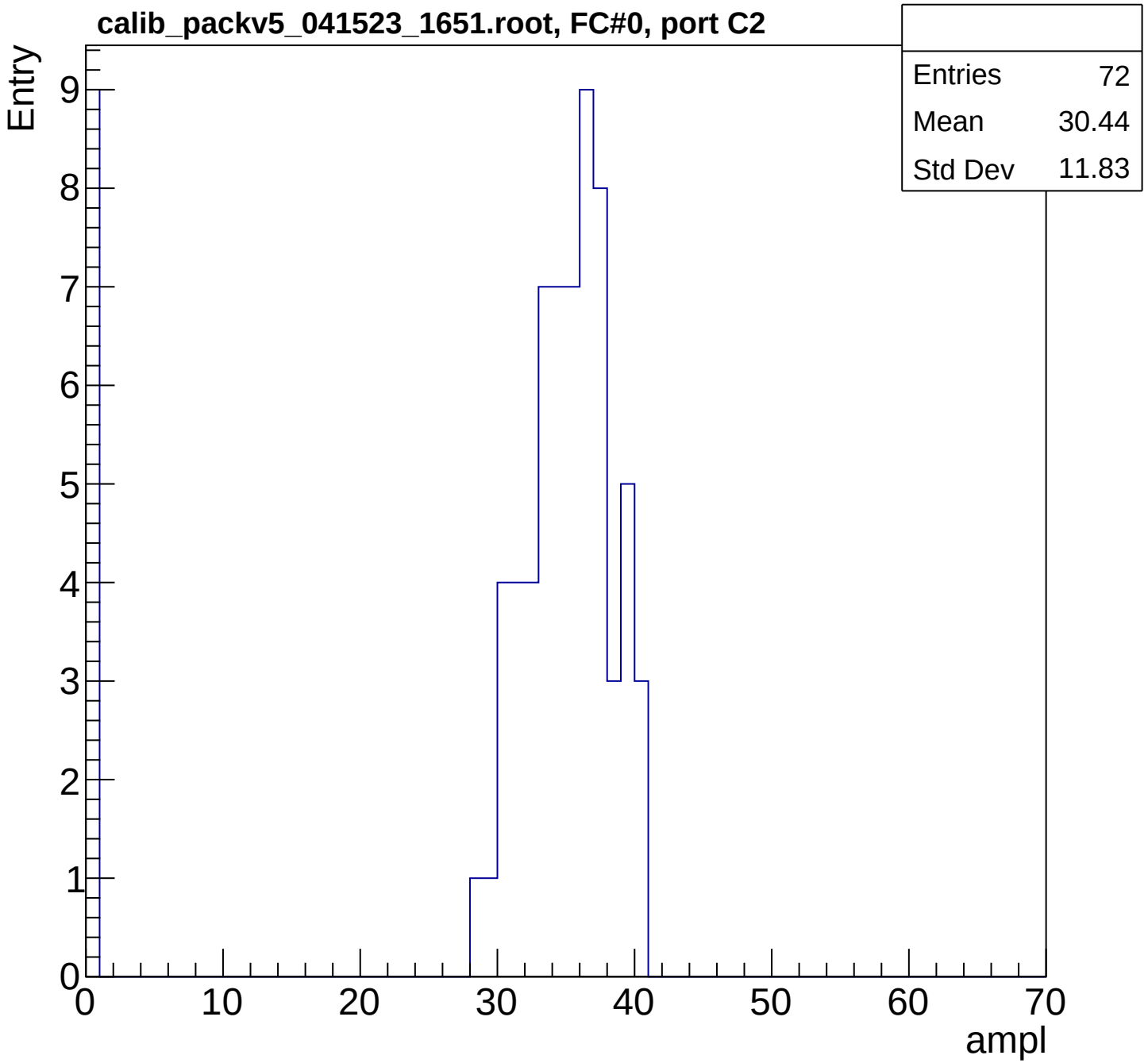
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch102, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 30.44
Std Dev 11.83
Entry
ampl
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3
4
5
6
7
8
9
0
10
20
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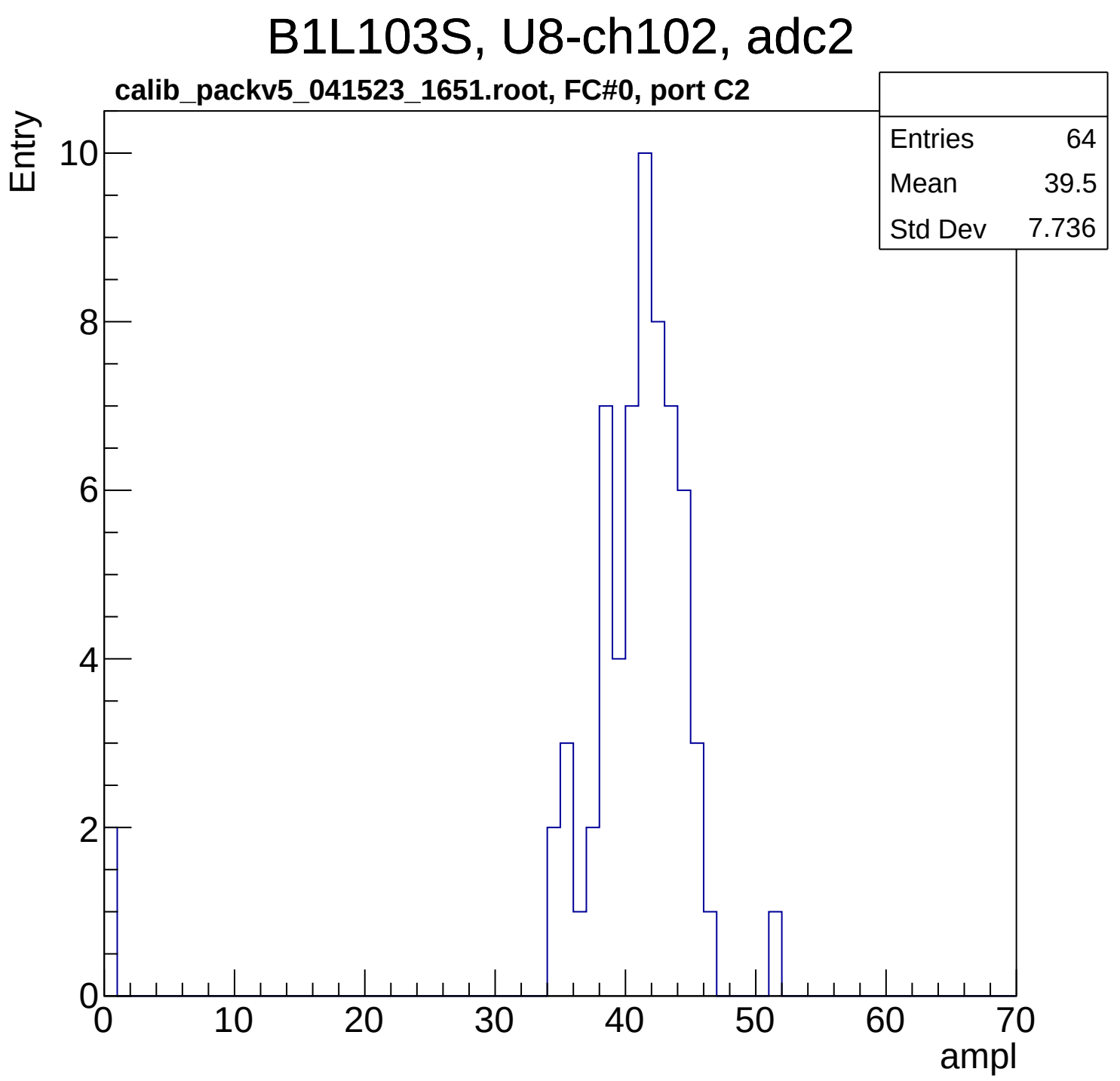
40
50
60
70


B1L103S, U8-ch102, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 39.5
Std Dev 7.736
Entry
ampl
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8
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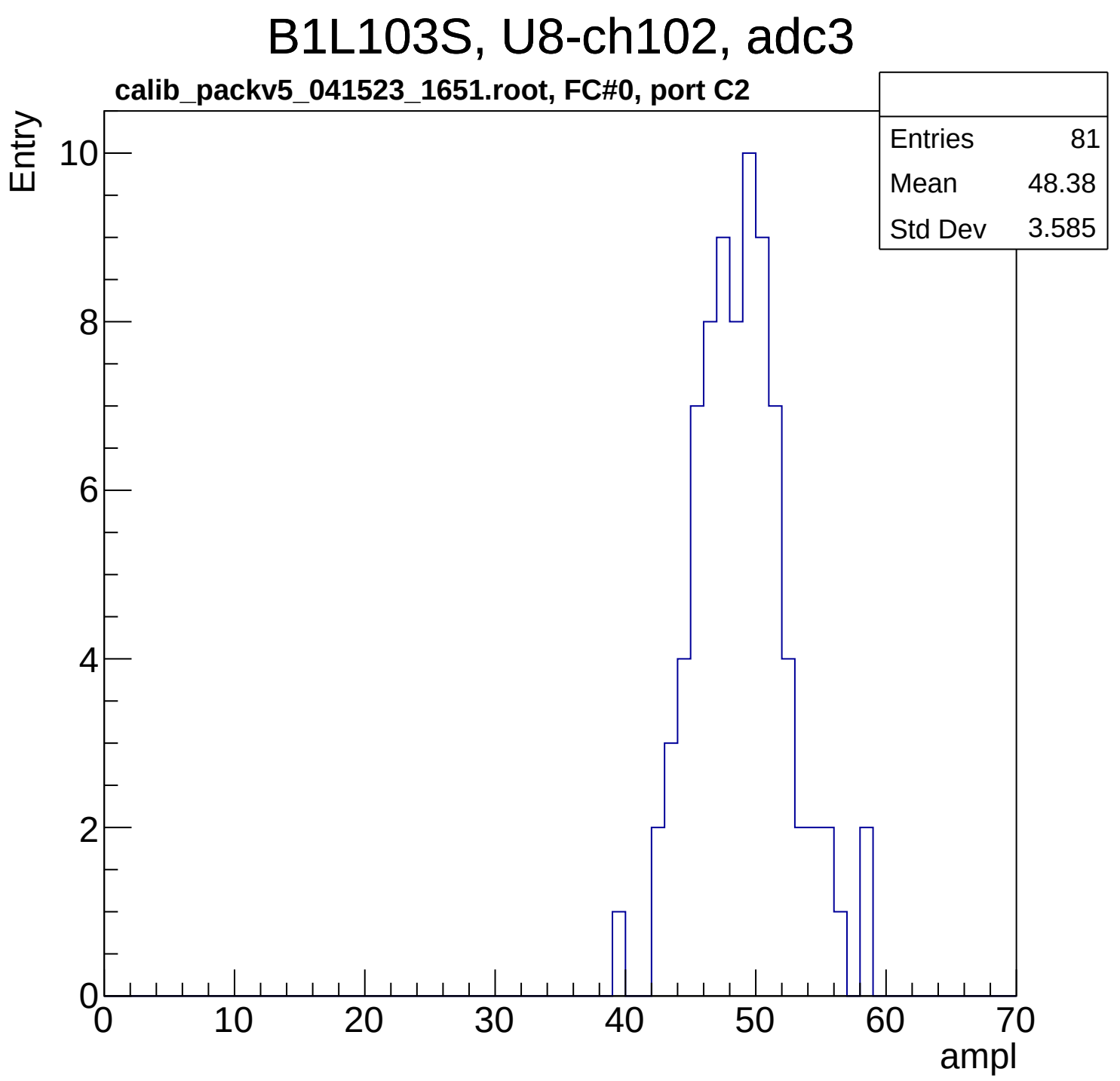
0
10
20
30
40
50
60
70


B1L103S, U8-ch102, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 48.38
Std Dev 3.585
Entry
ampl
0
2
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8
10
0
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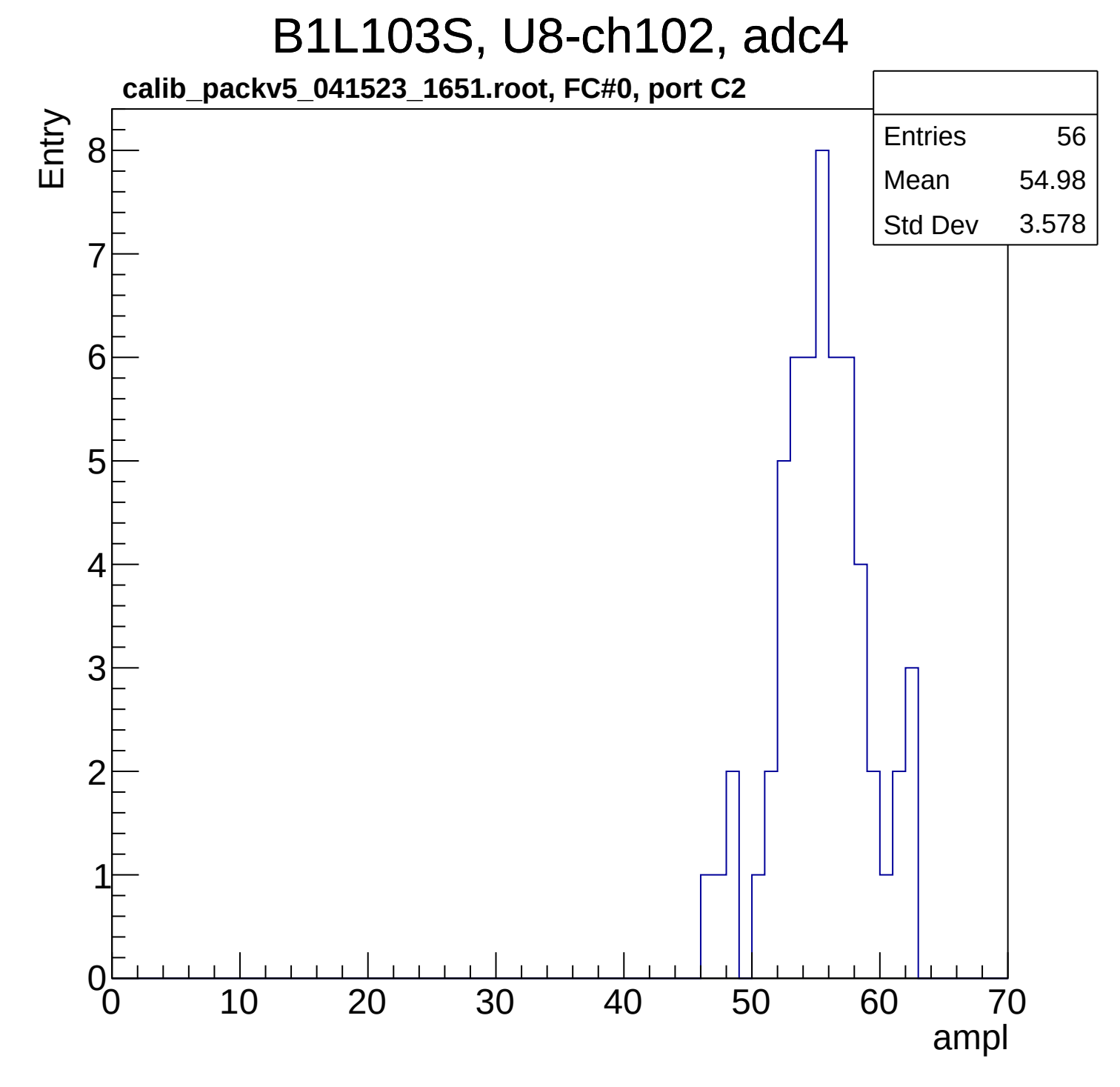
40
50
60
70


B1L103S, U8-ch102, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 54.98
Std Dev 3.578
Entry
ampl
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2
3
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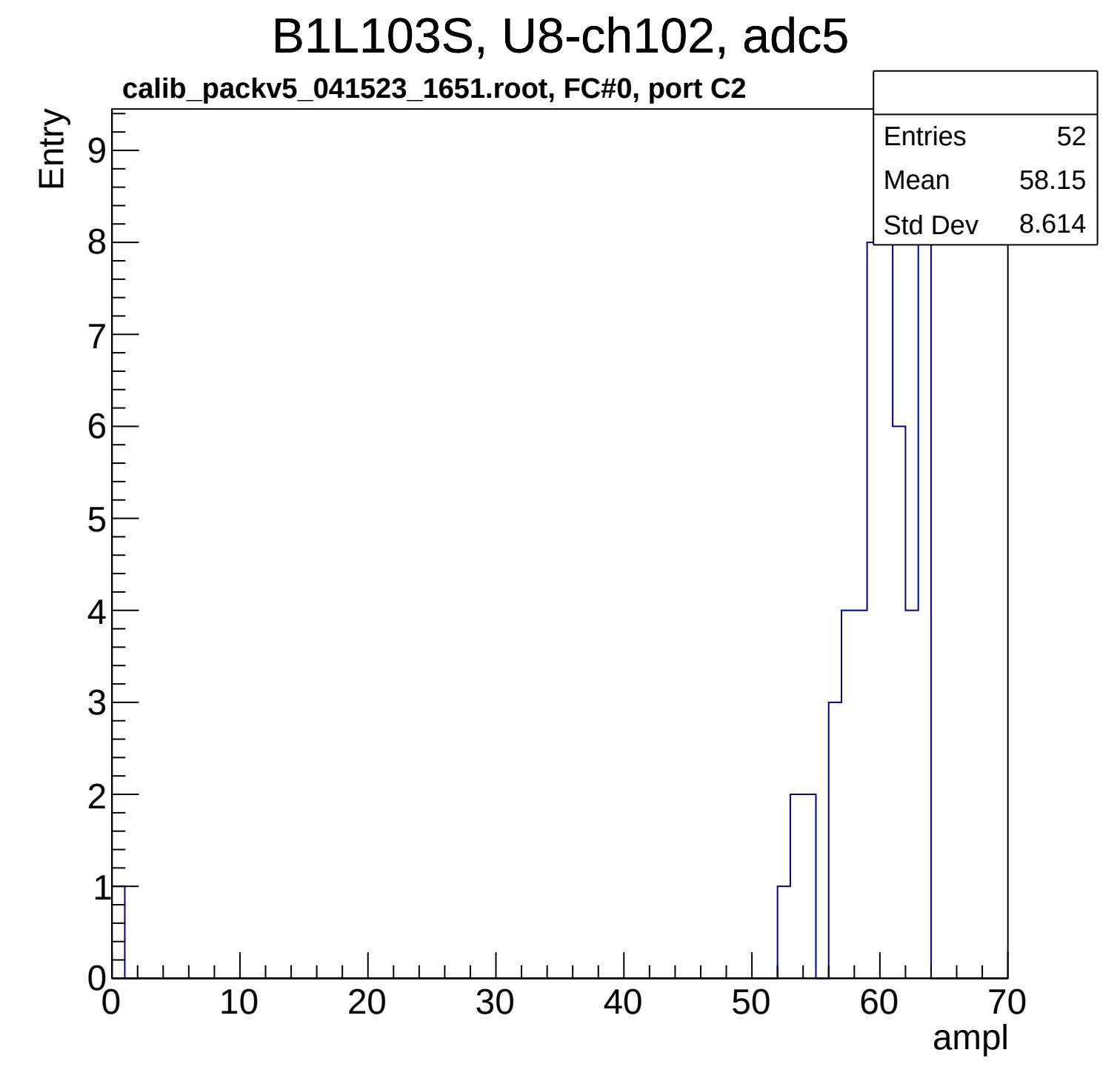
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch102, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 58.15
Std Dev 8.614
Entry
ampl
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4
5
6
7
8
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0
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60
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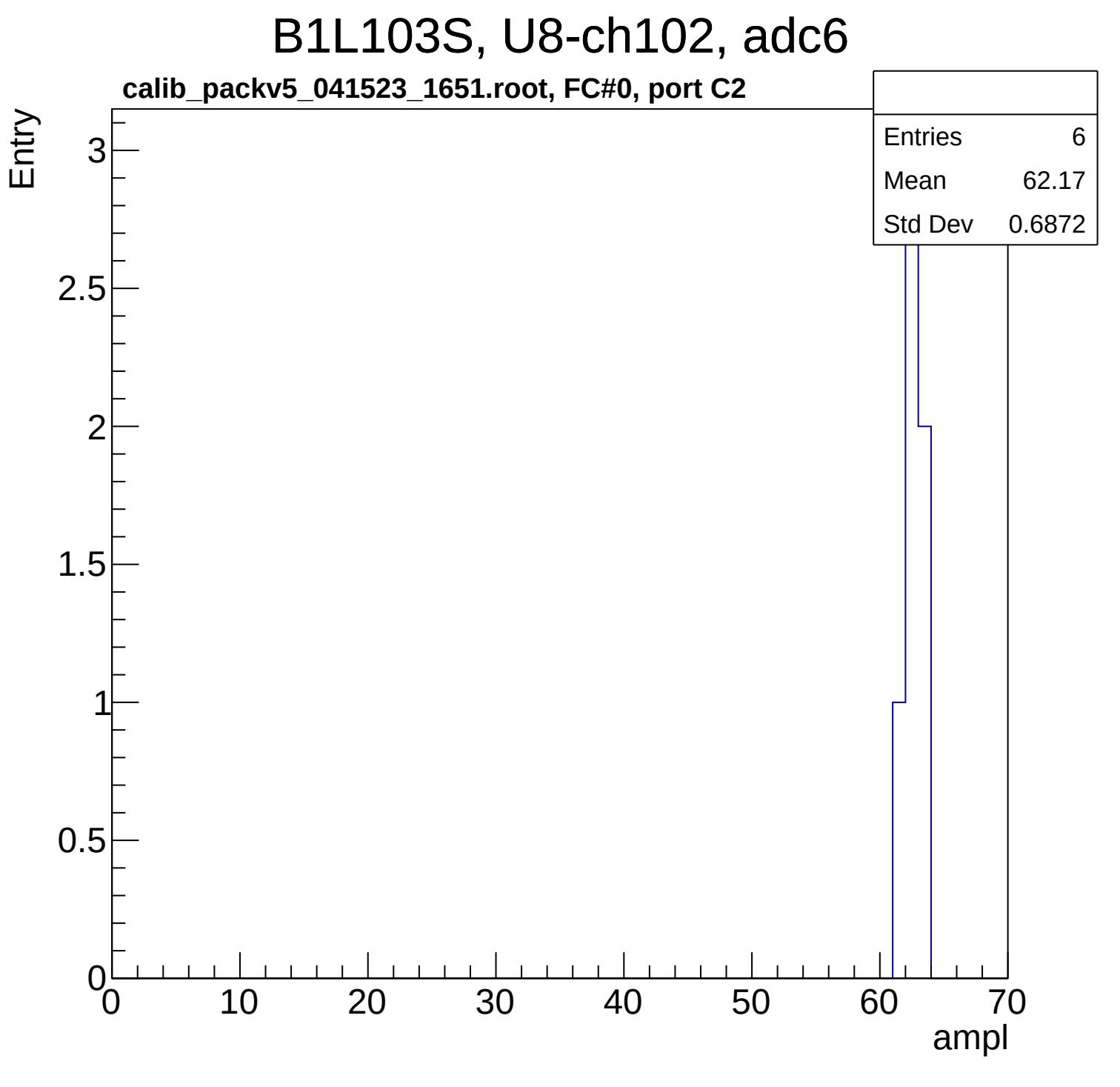
B1L103S, U8-ch102, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 62.17
Std Dev 0.6872
Entry
ampl
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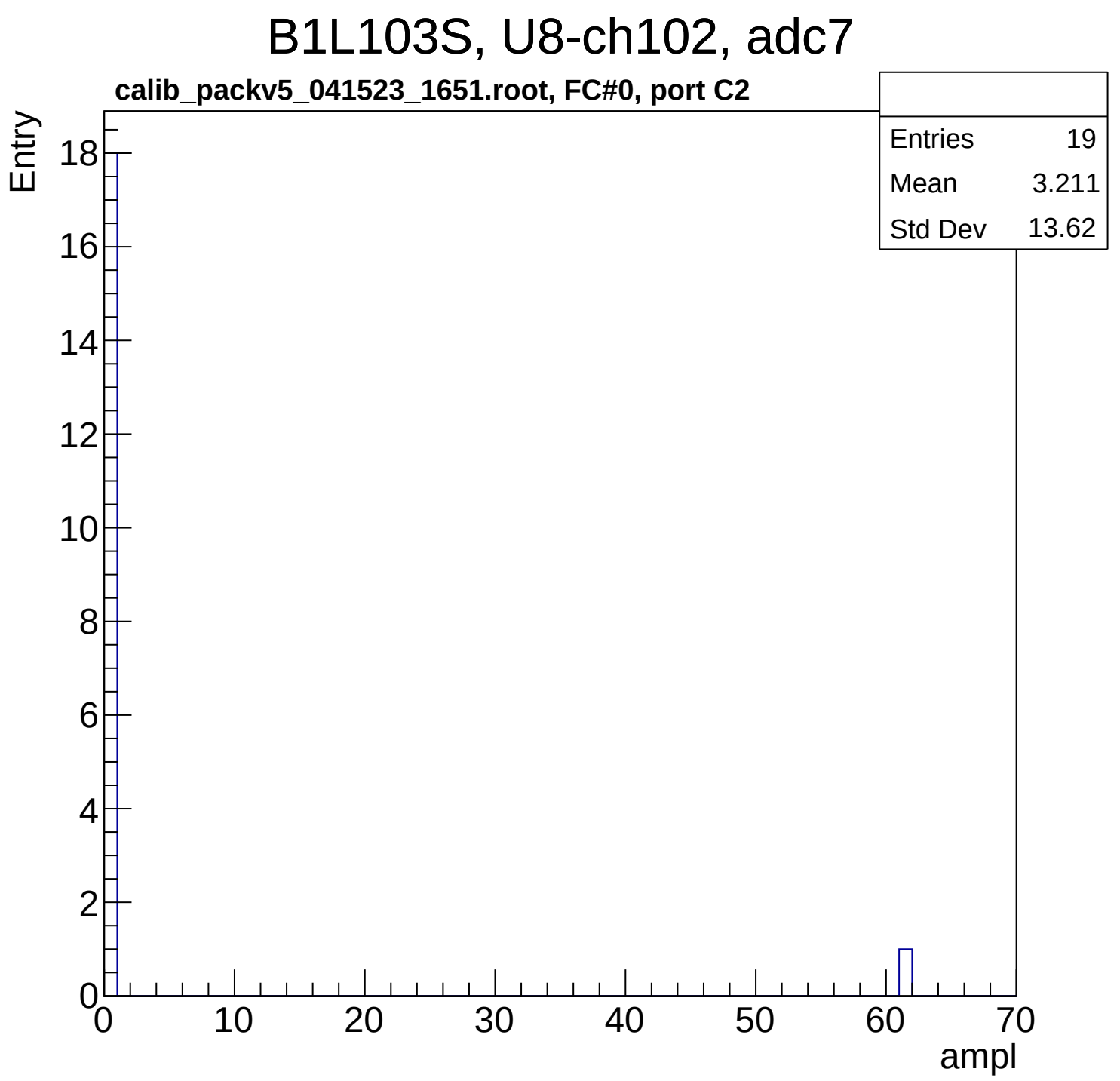
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U8-ch102, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.211
Std Dev 13.62
Entry
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6
8
10
12
14
16
18
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10
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30
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50
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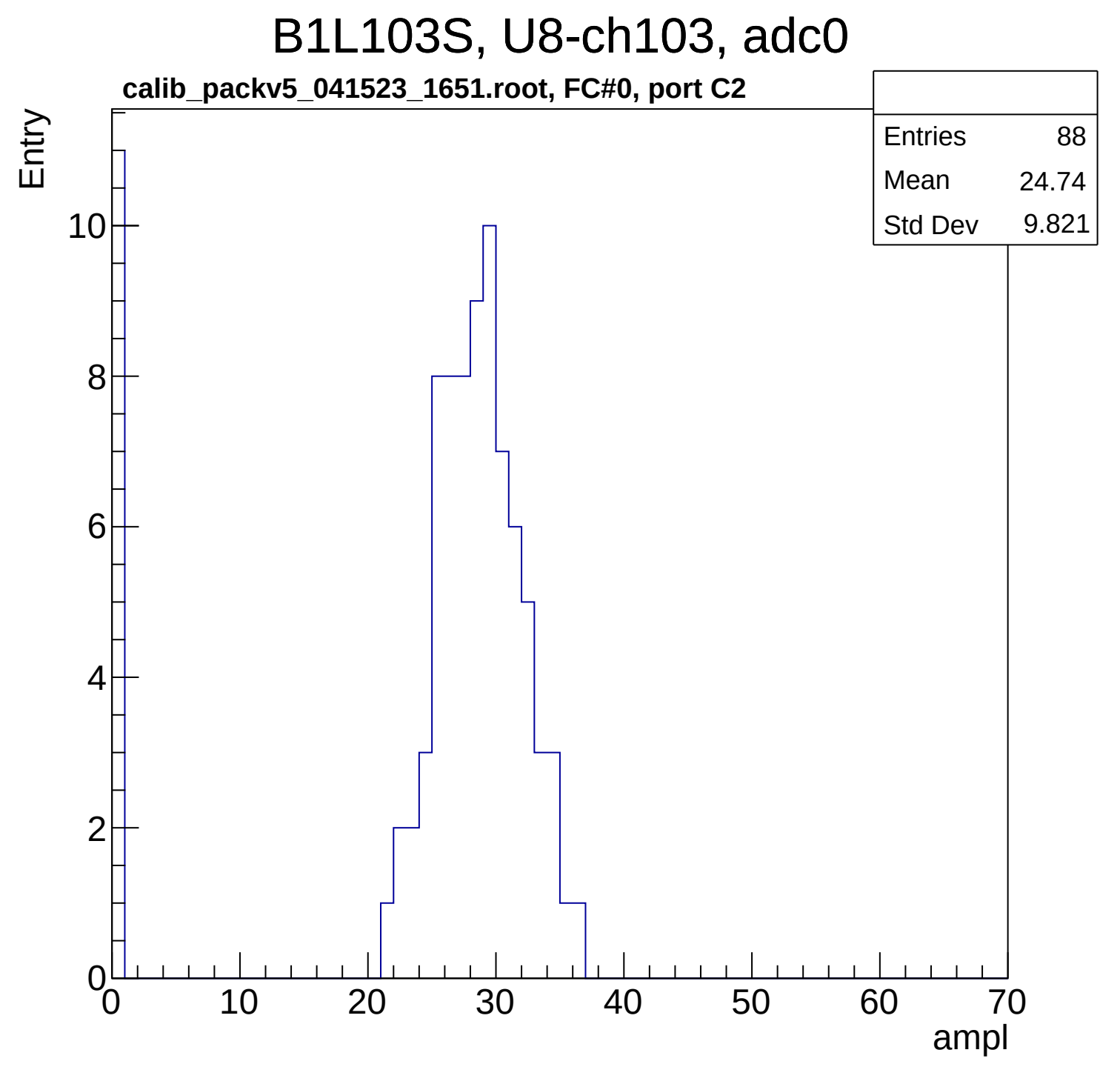
70
ampl


B1L103S, U8-ch103, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 24.74
Std Dev 9.821
Entry
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20
30
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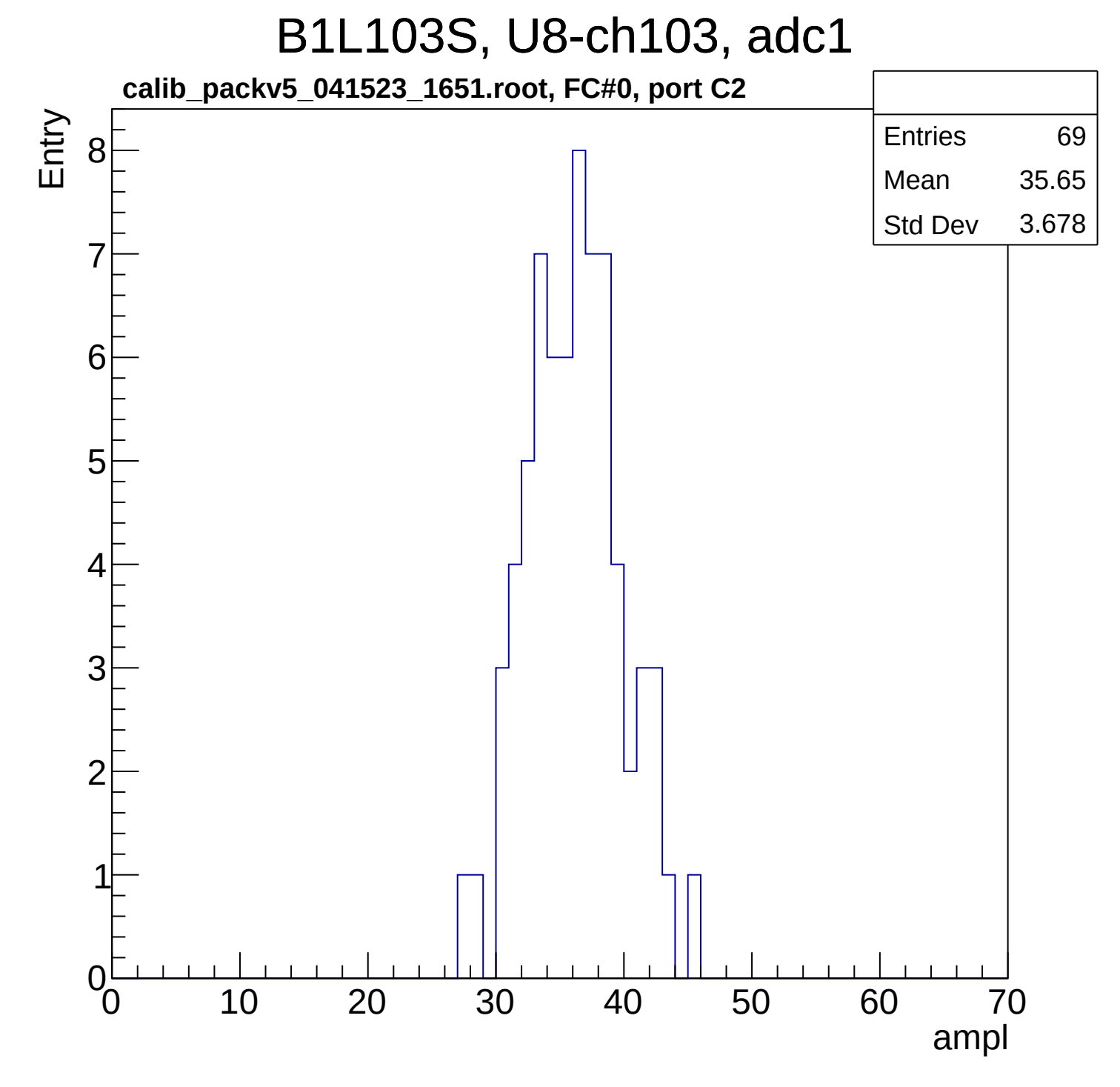
50
60
70
ampl


B1L103S, U8-ch103, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 35.65
Std Dev 3.678
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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60
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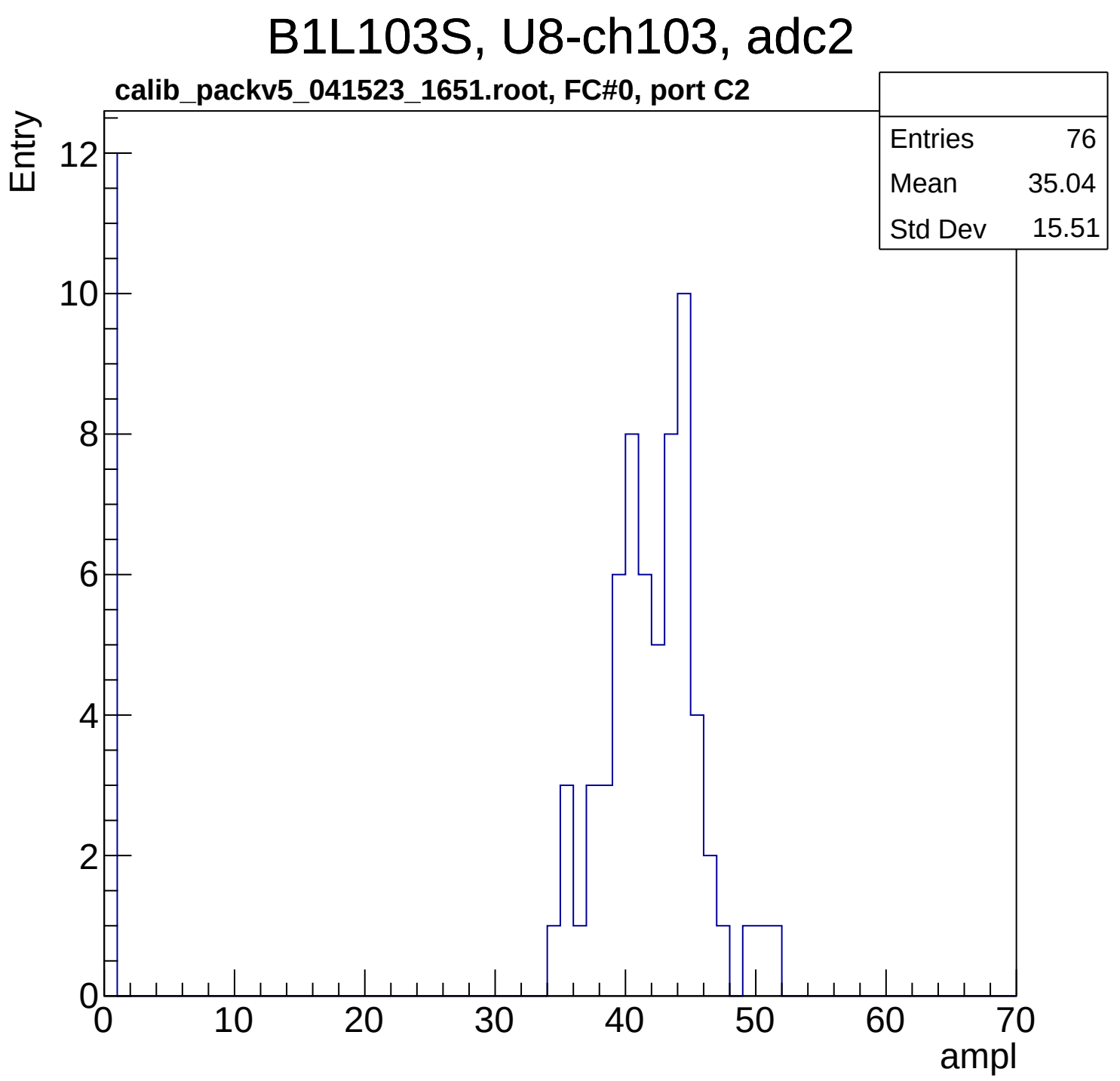
B1L103S, U8-ch103, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 35.04
Std Dev 15.51
Entry
0
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4
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8
10
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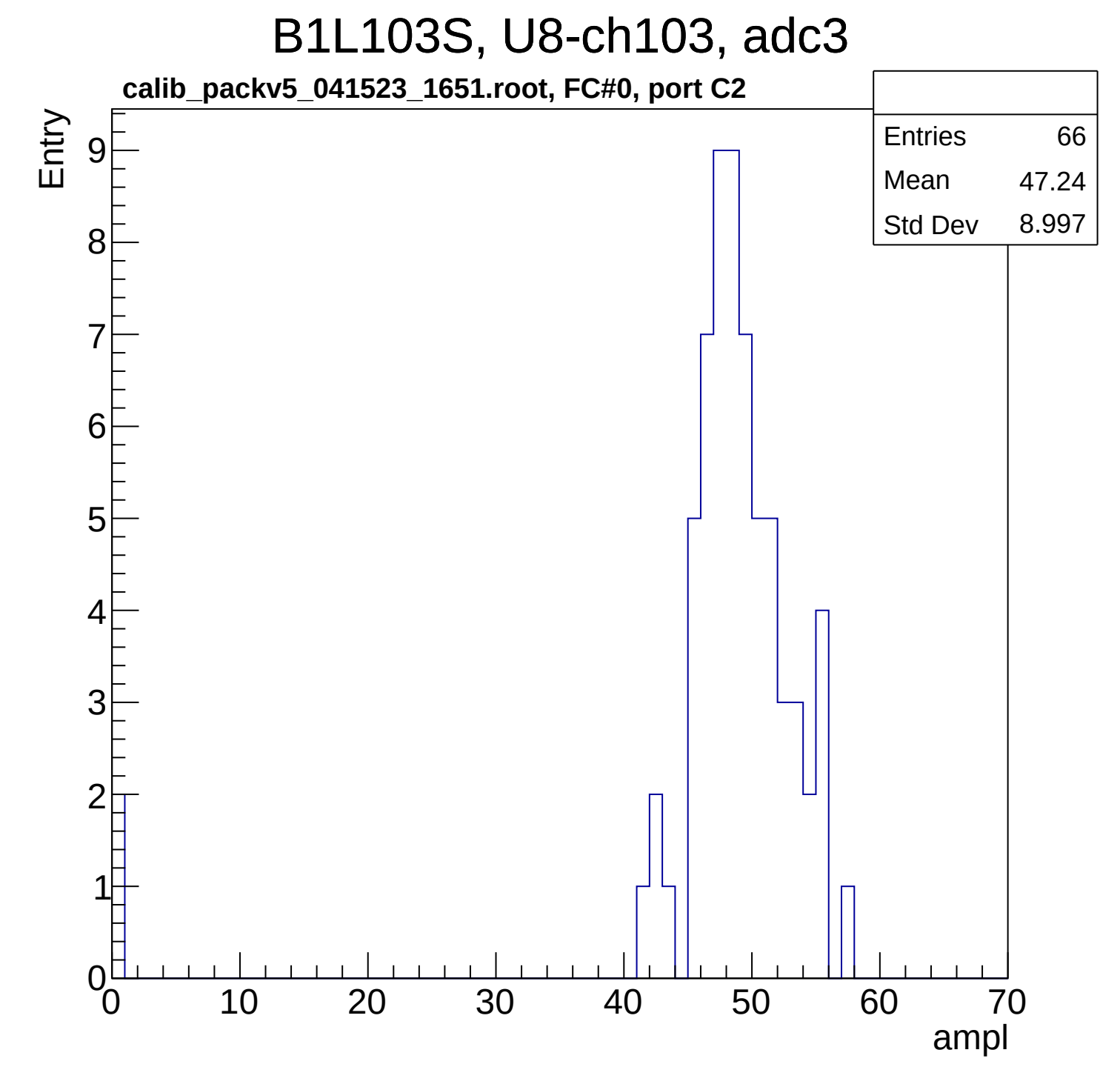
70
ampl


B1L103S, U8-ch103, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 47.24
Std Dev 8.997
Entry
ampl
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3
4
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6
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0
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60
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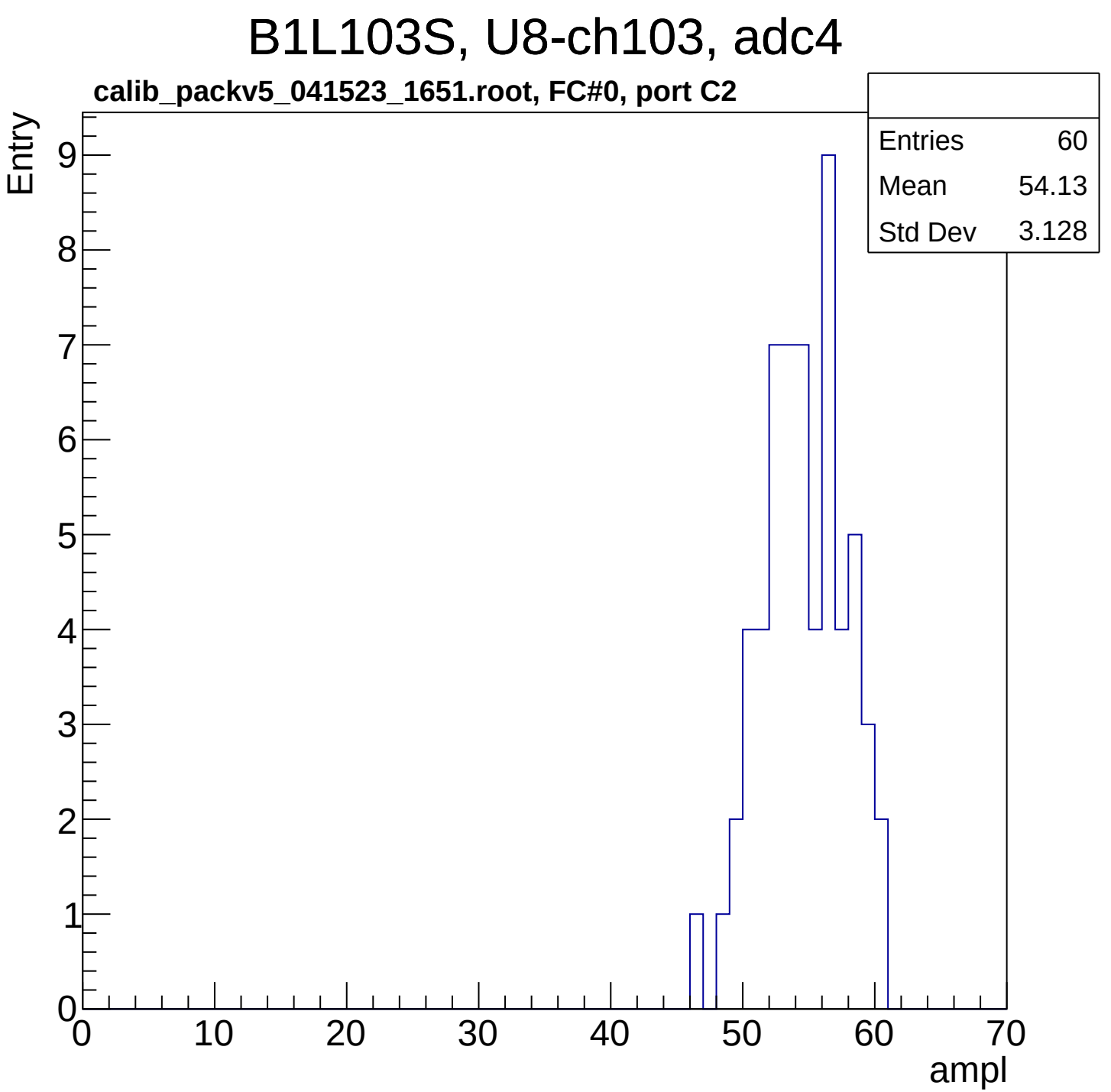
B1L103S, U8-ch103, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 54.13
Std Dev 3.128
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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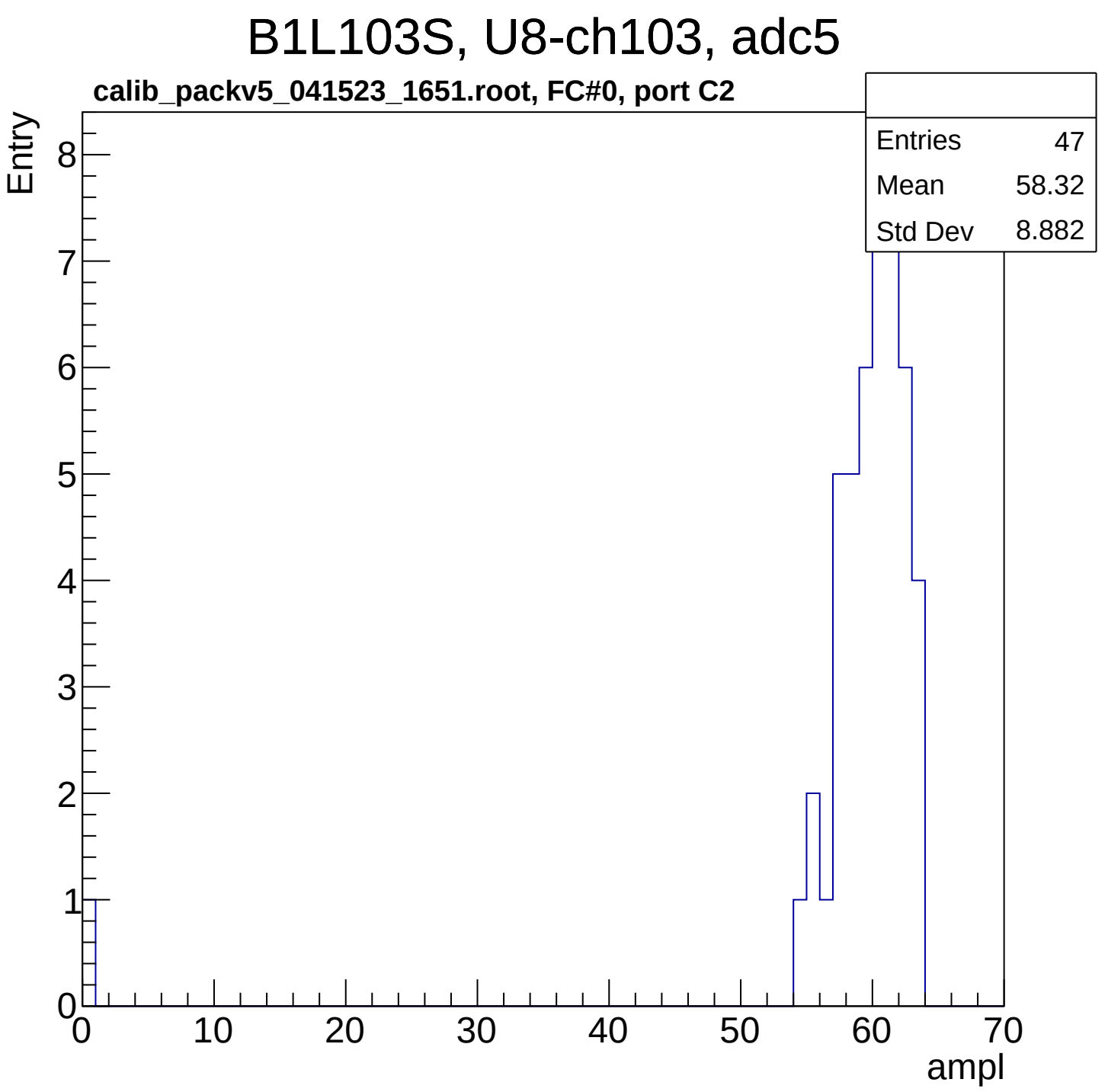
B1L103S, U8-ch103, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 58.32
Std Dev 8.882
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
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60
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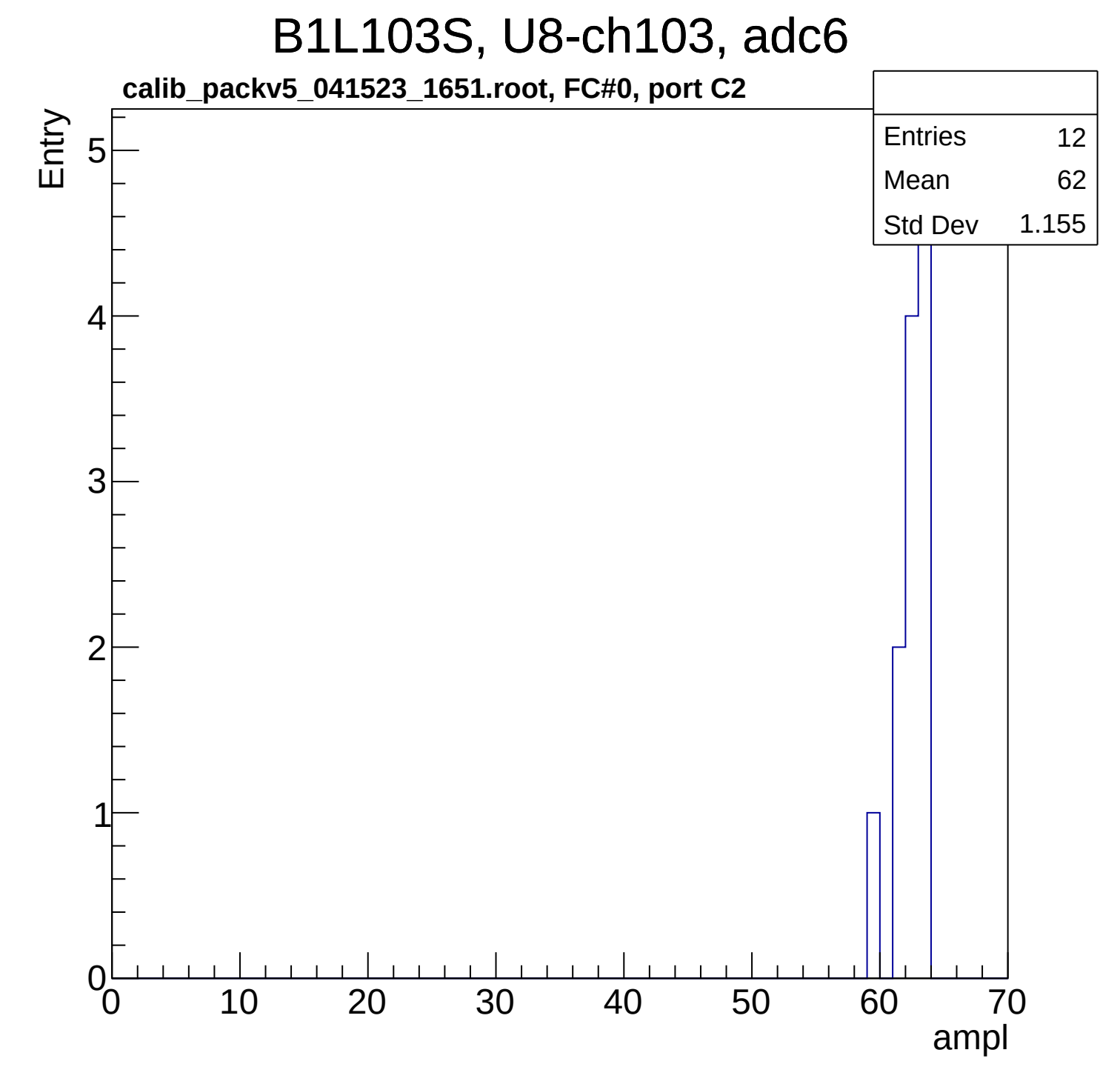
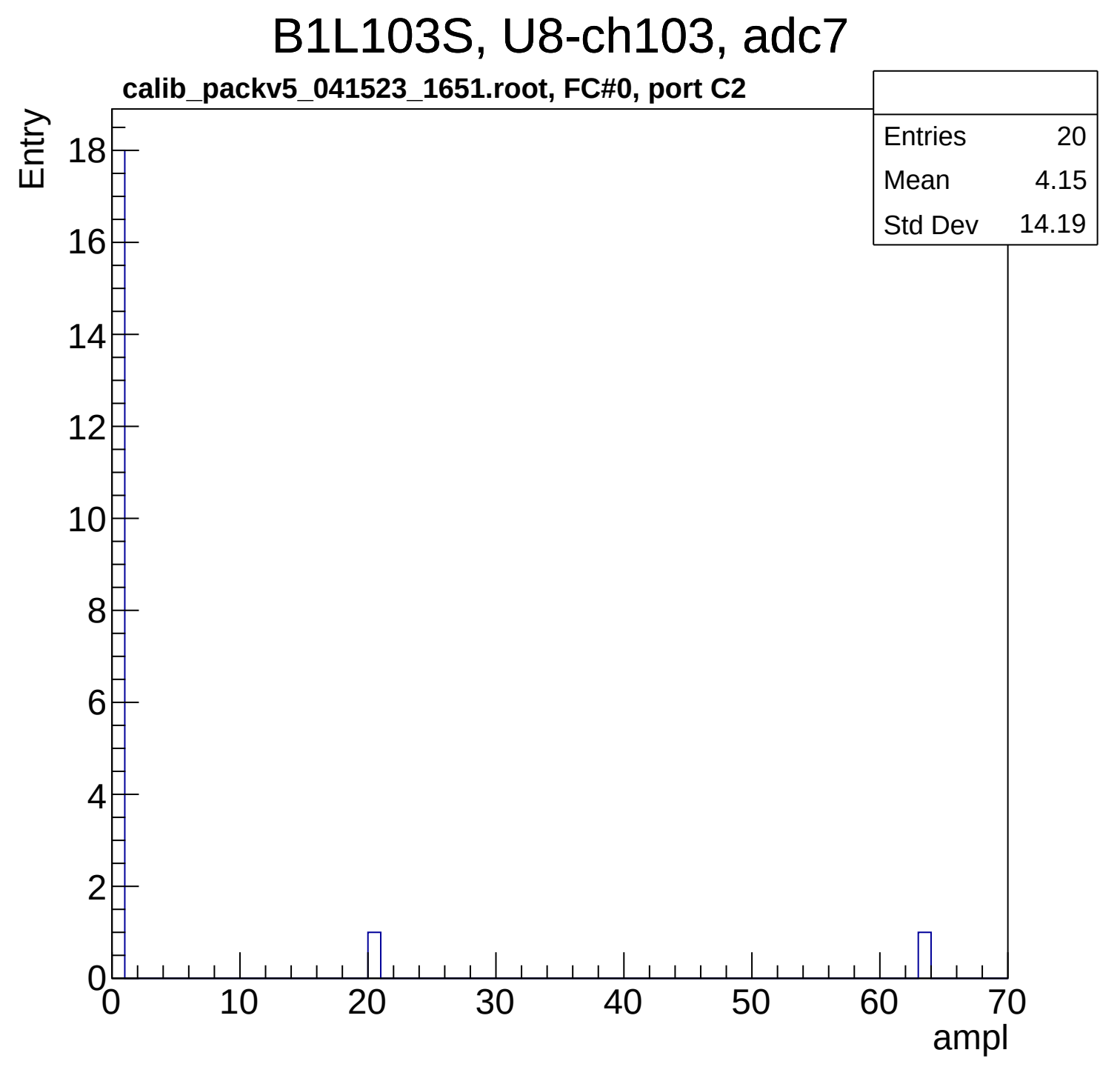
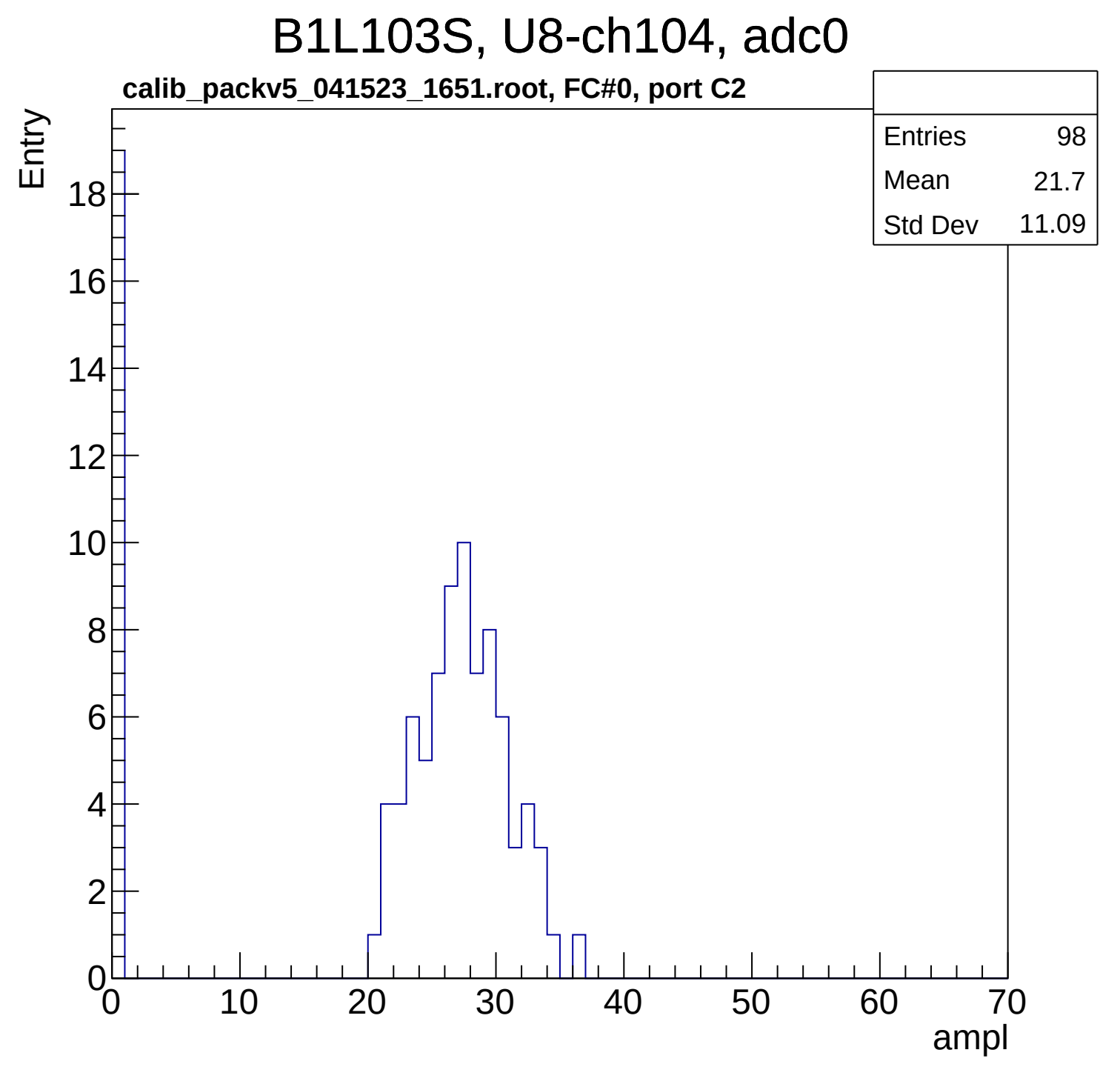

B1L103S, U8-ch103, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 62
Std Dev 1.155
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U8-ch103, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4.15
Std Dev 14.19
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch104, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 98
Mean 21.7
Std Dev 11.09
Entry
ampl
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4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
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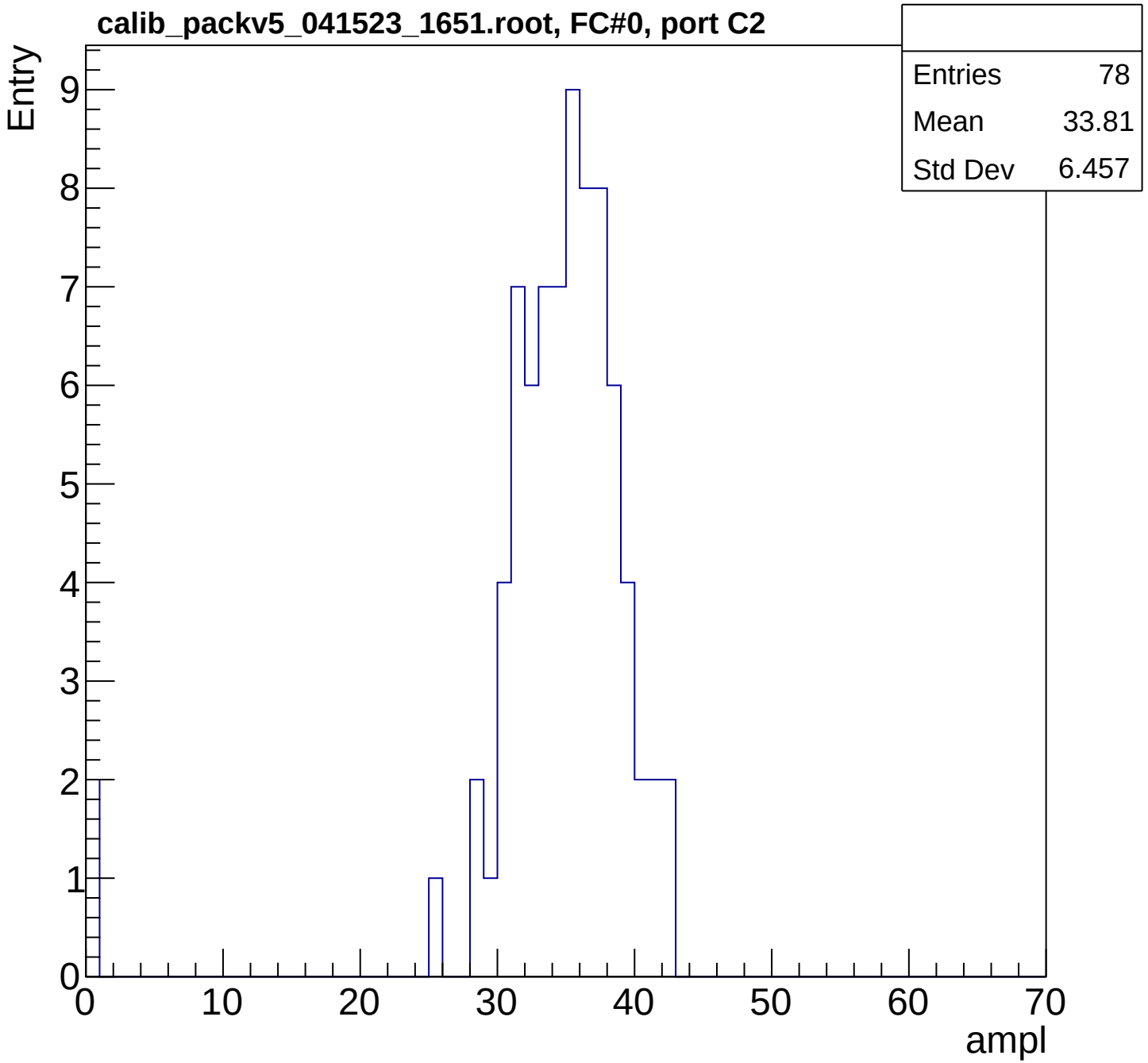
B1L103S, U8-ch104, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 33.81
Std Dev 6.457
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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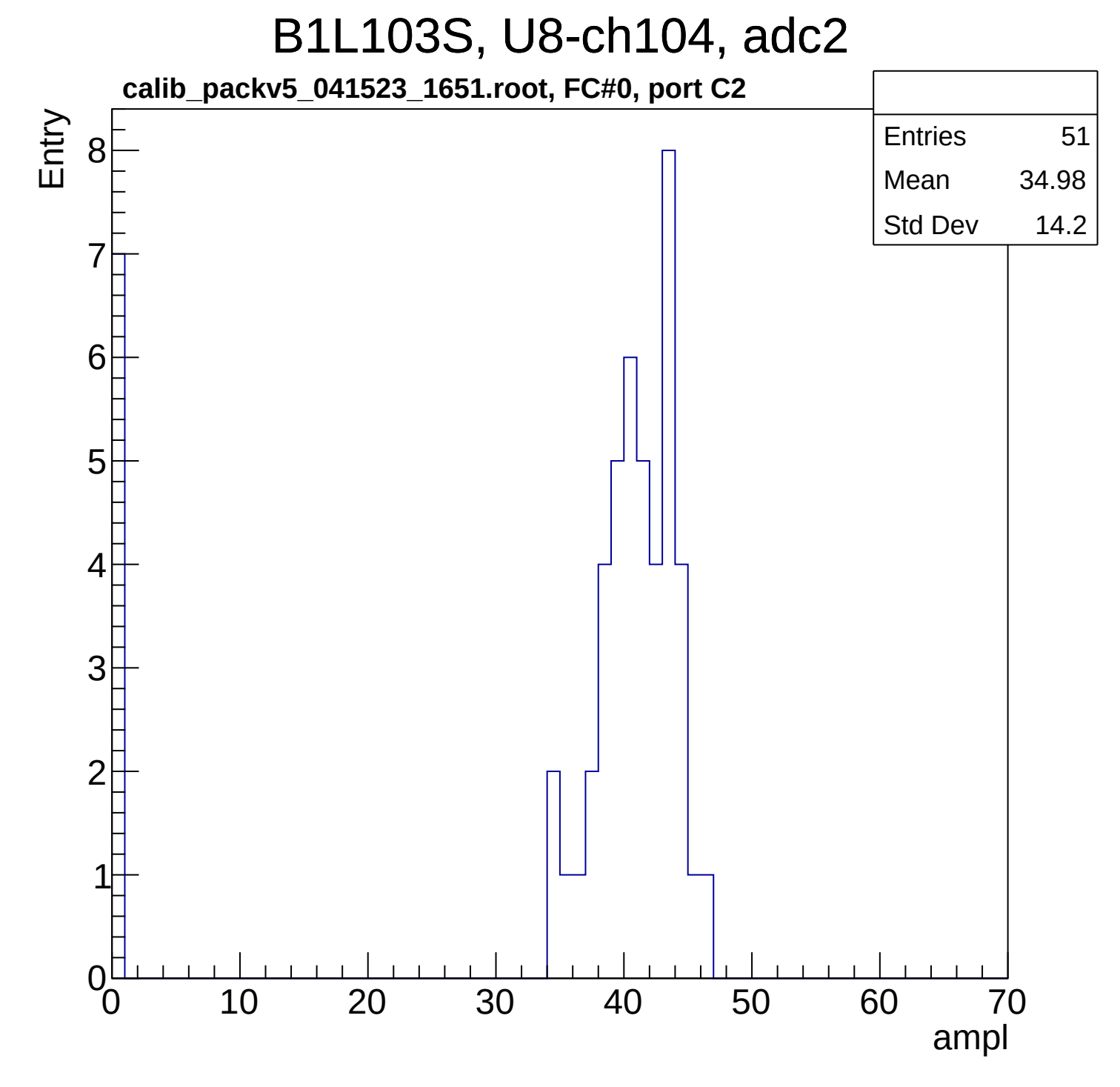
B1L103S, U8-ch104, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 34.98
Std Dev 14.2
Entry
ampl
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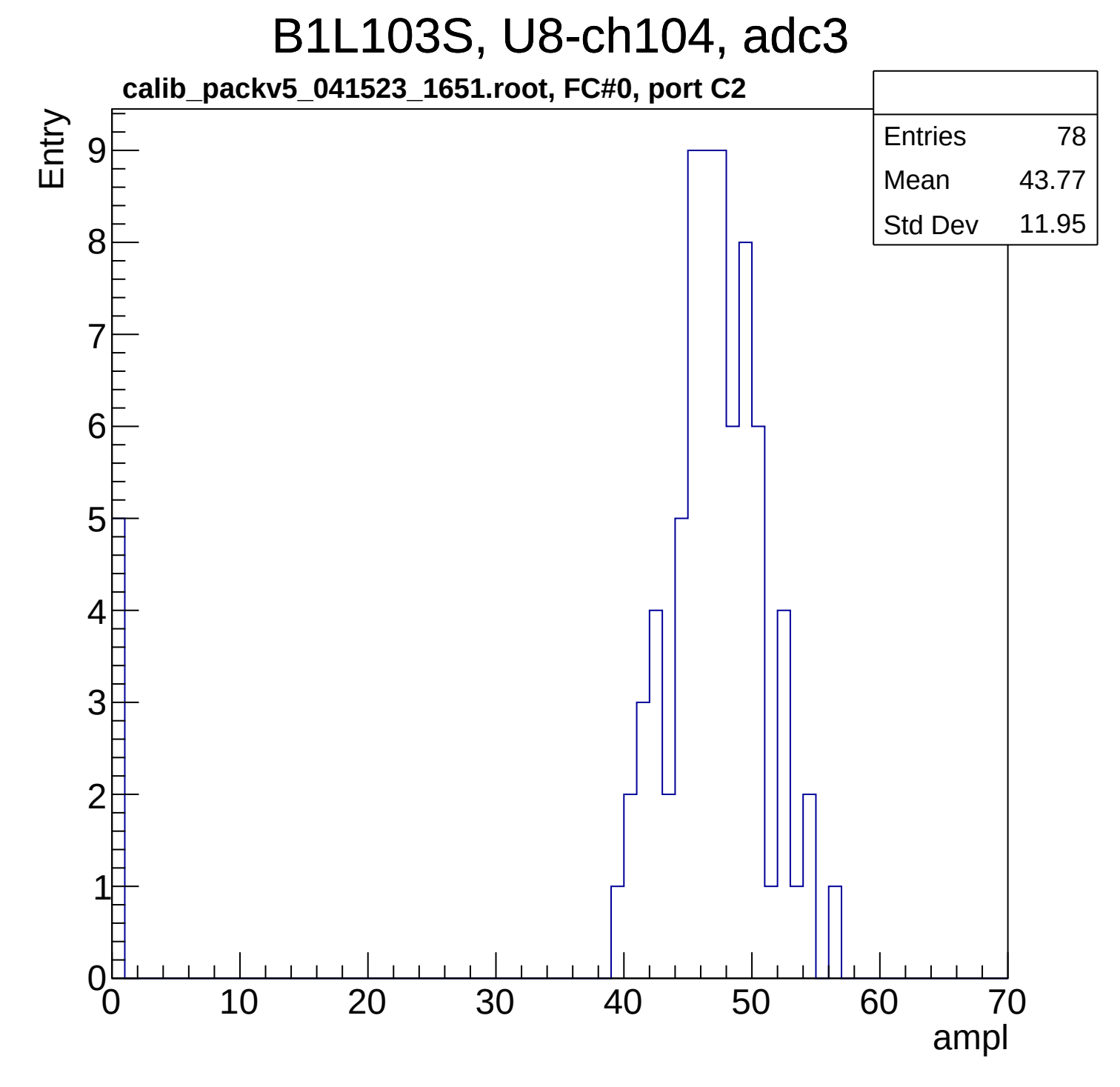
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch104, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 43.77
Std Dev 11.95
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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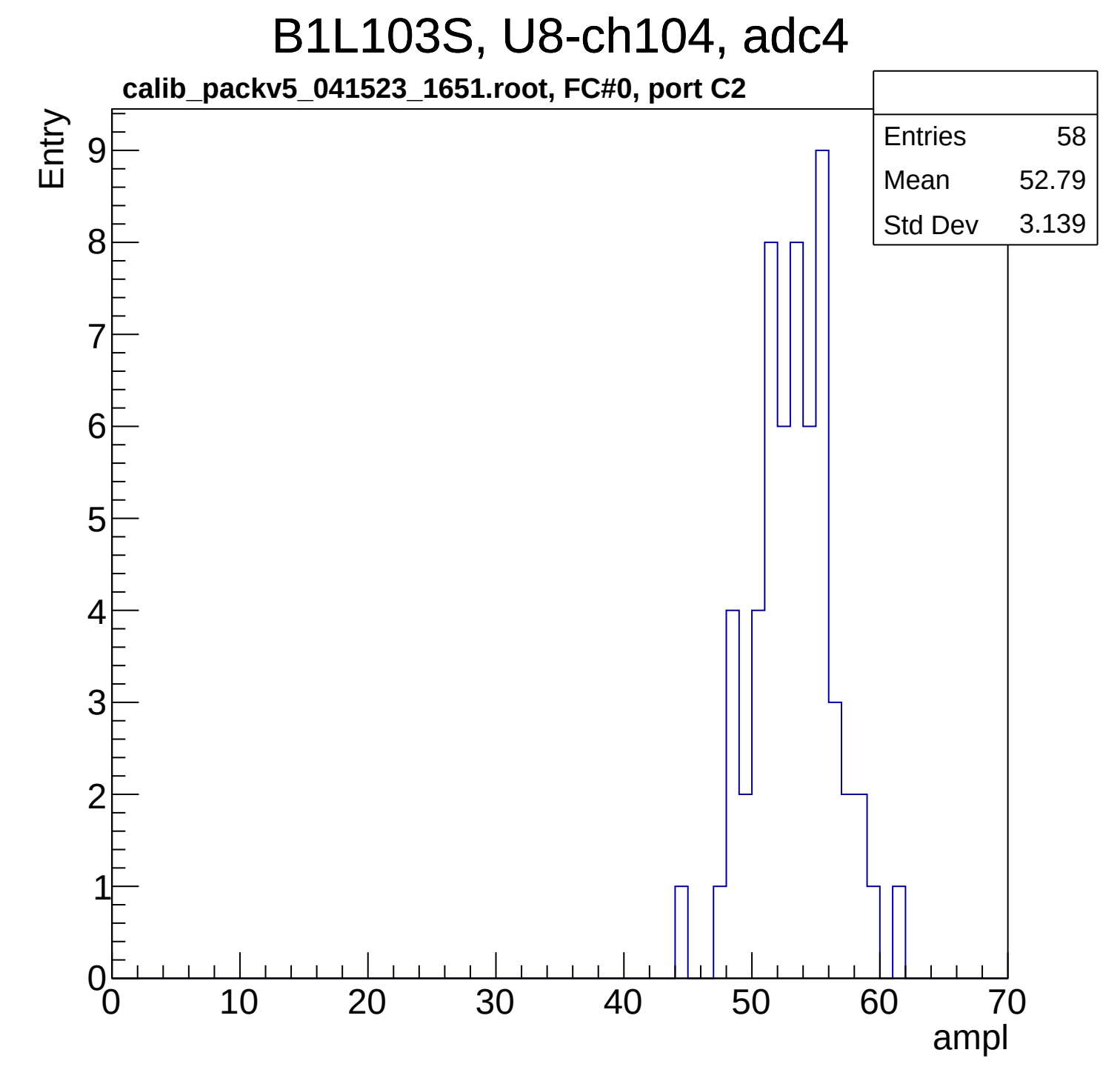
60
70


B1L103S, U8-ch104, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 52.79
Std Dev 3.139
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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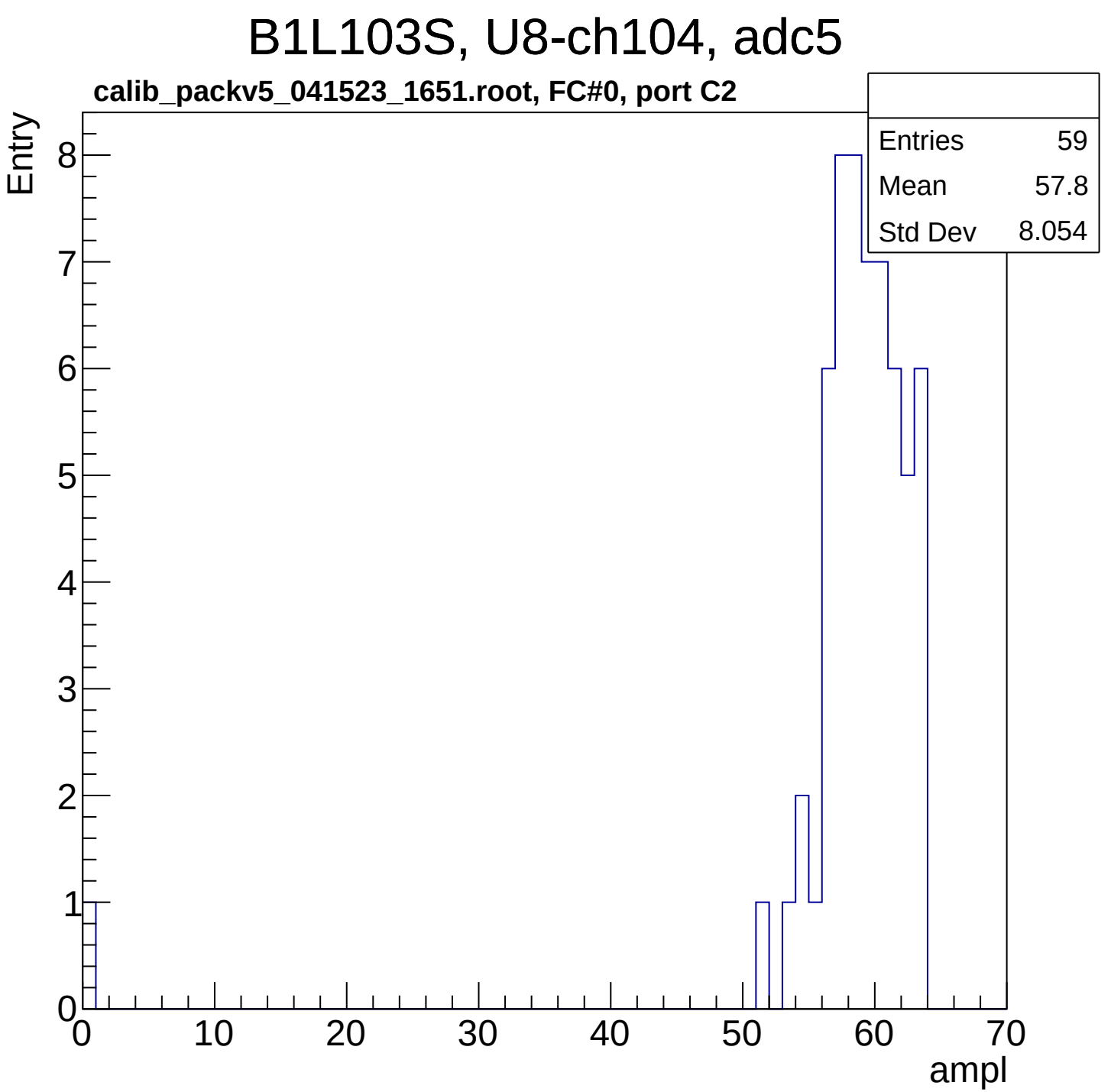
B1L103S, U8-ch104, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 57.8
Std Dev 8.054
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
50
60
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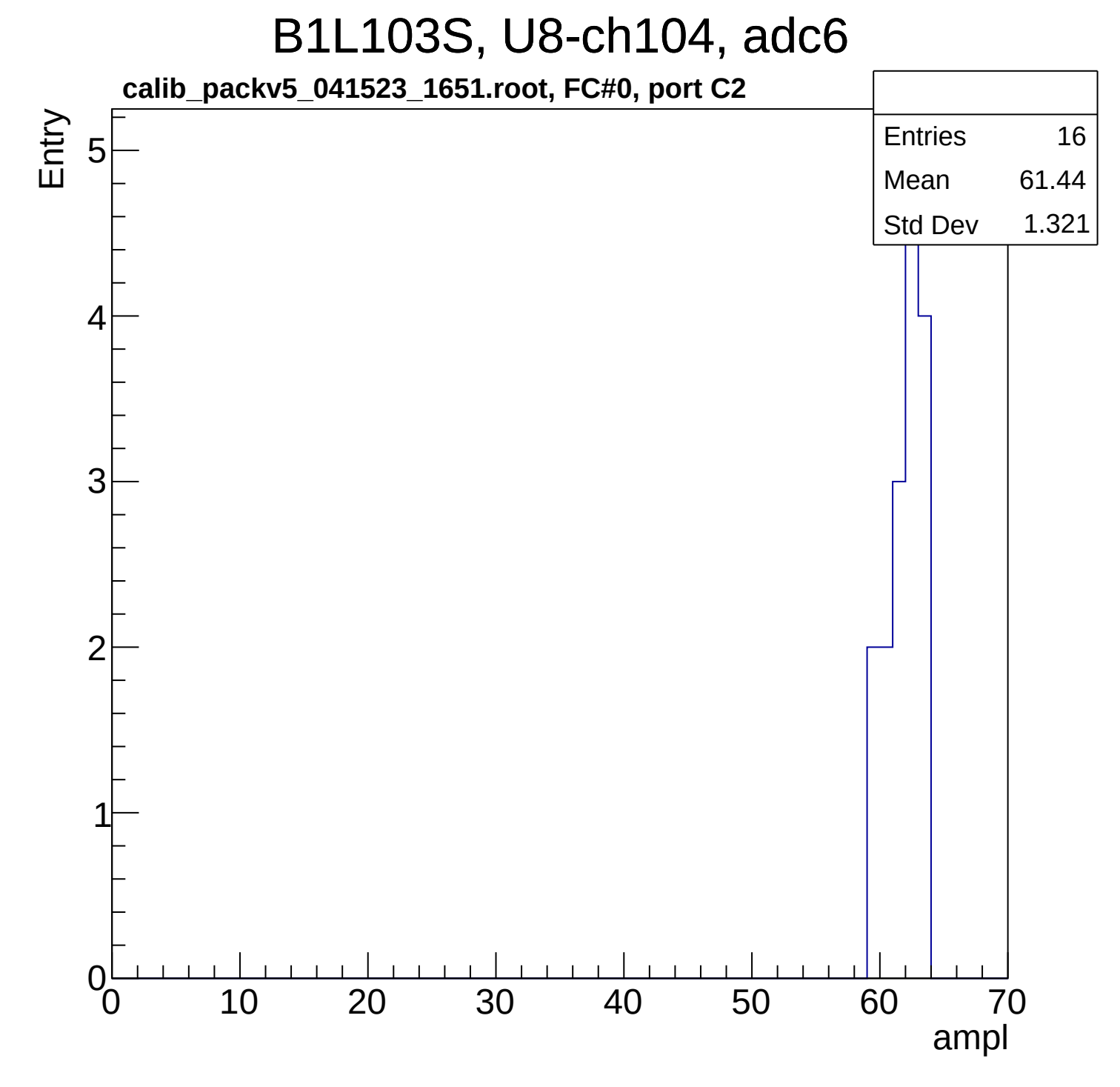
B1L103S, U8-ch104, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 61.44
Std Dev 1.321
Entry
0
1
2
3
4
5
0
10
20
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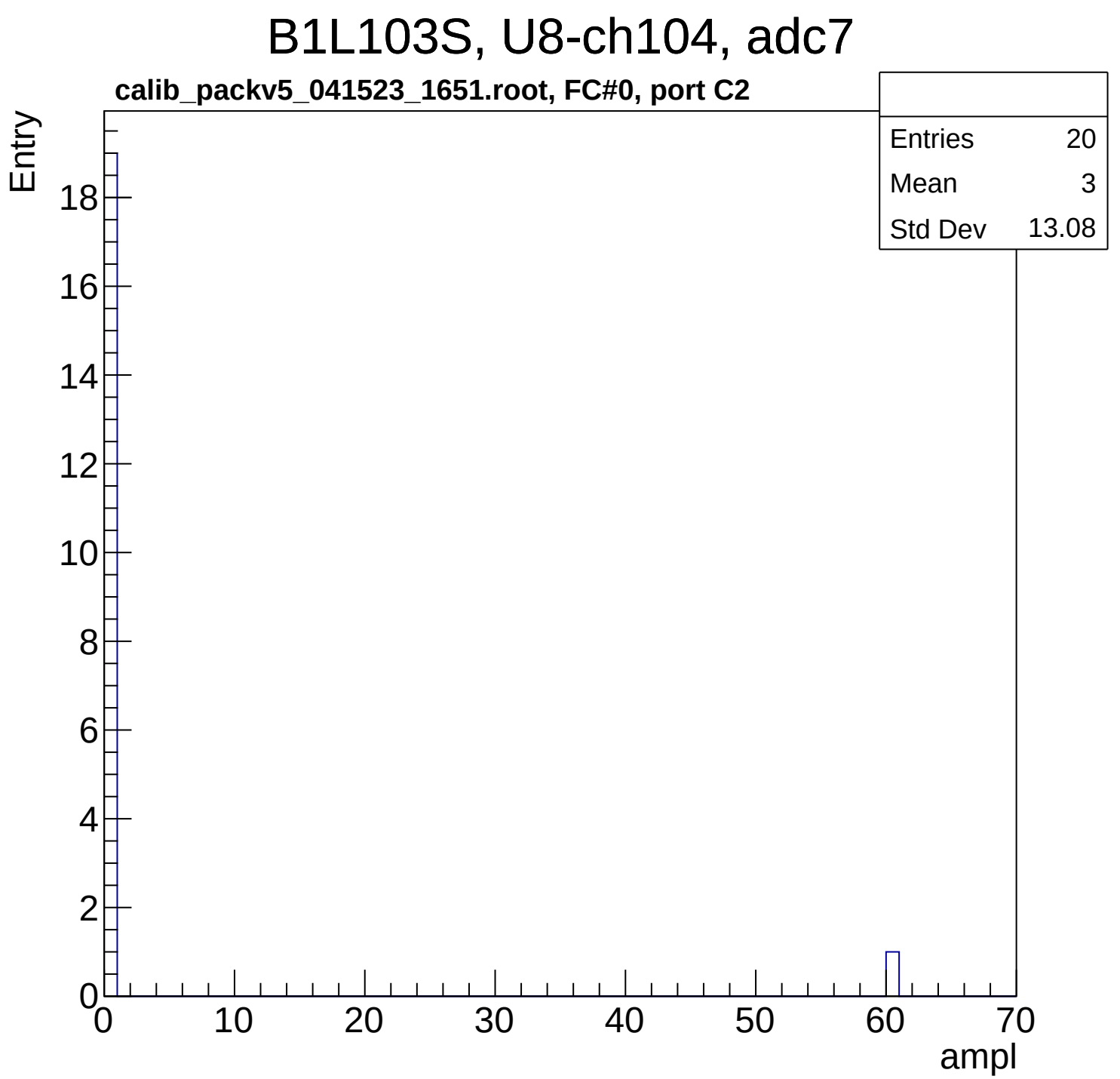
50
60
70
ampl


B1L103S, U8-ch104, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3
Std Dev 13.08
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
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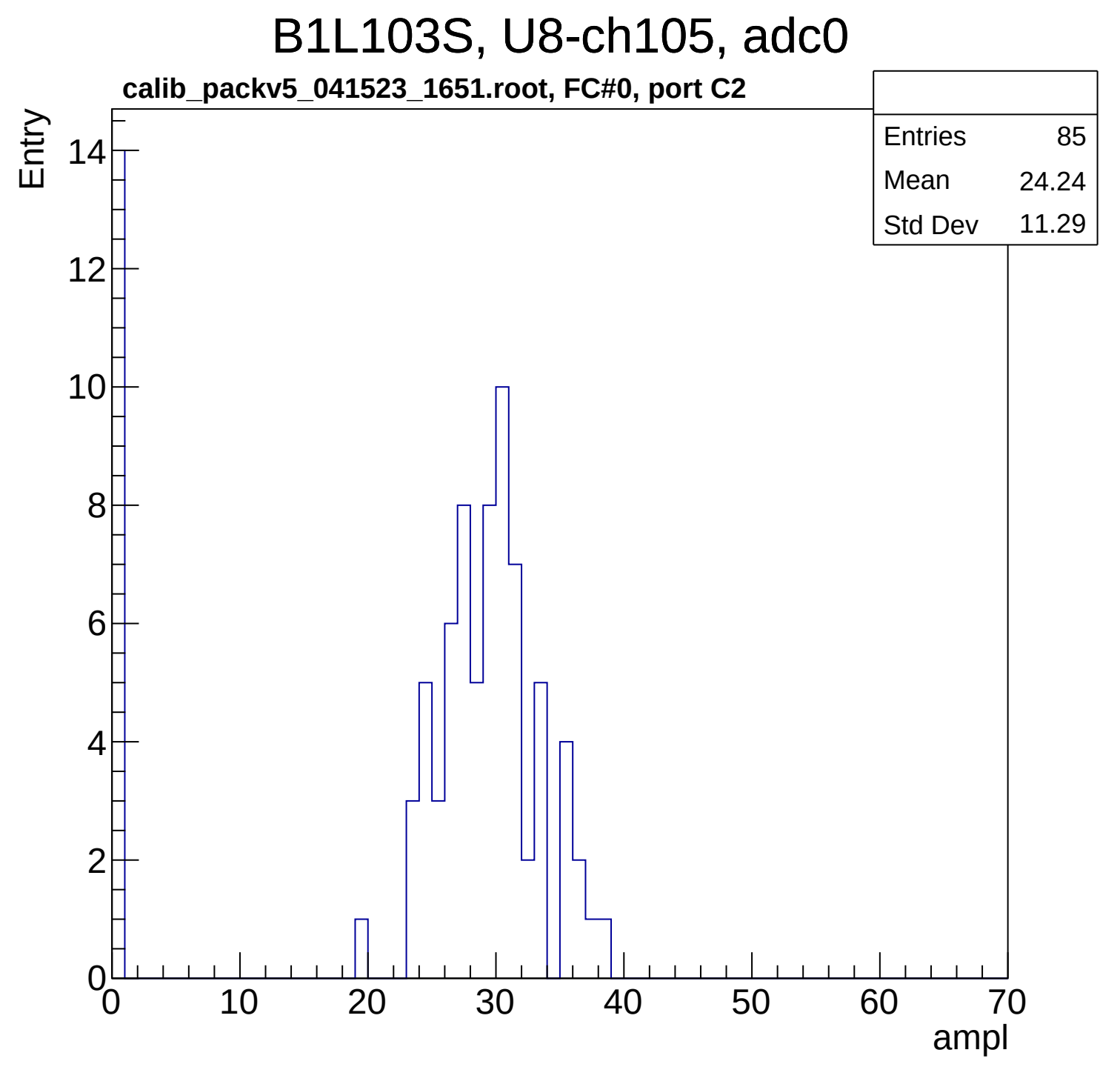
50
60
70
ampl


B1L103S, U8-ch105, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 24.24
Std Dev 11.29
Entry
ampl
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6
8
10
12
14
0
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60
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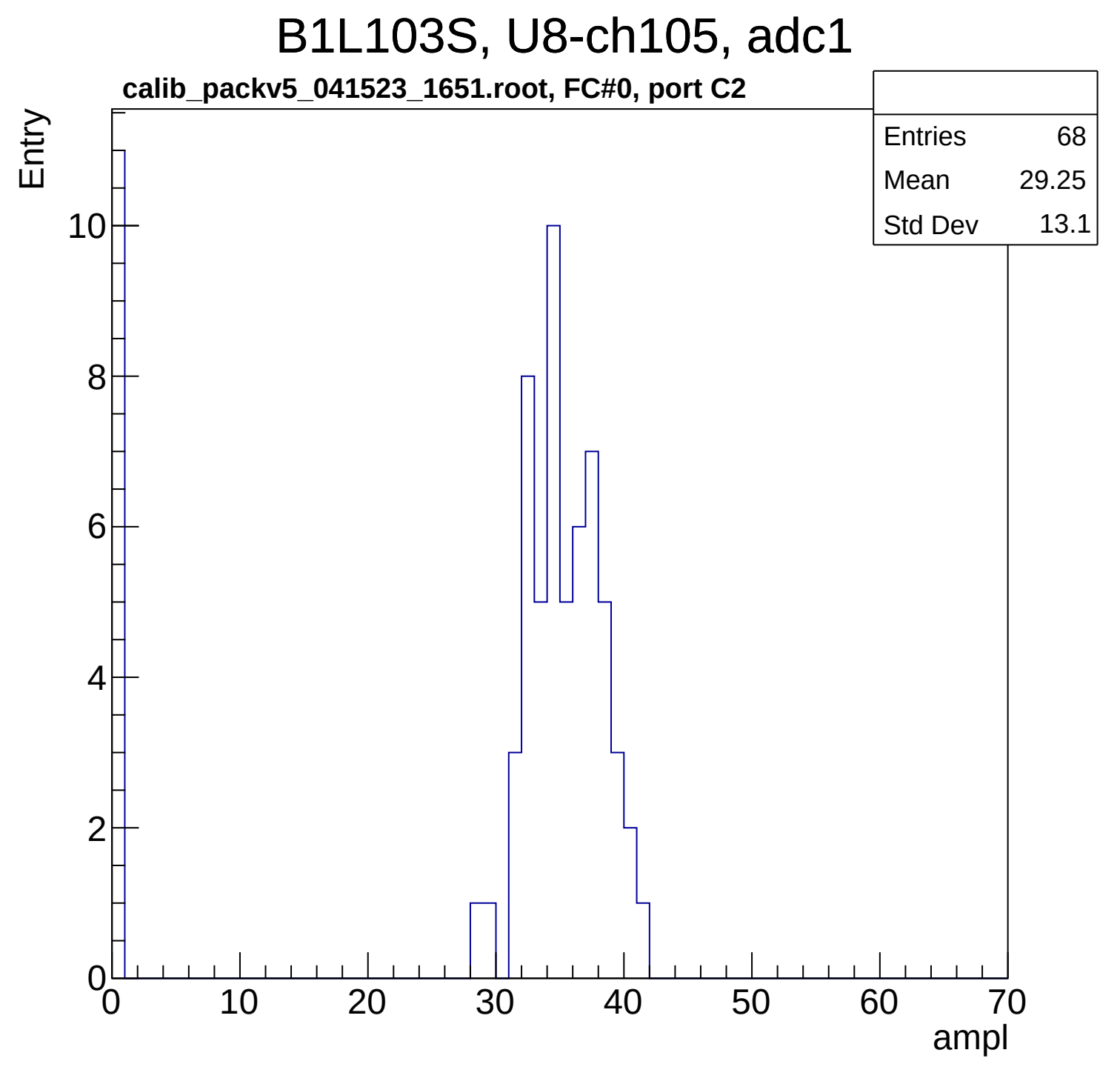
B1L103S, U8-ch105, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 29.25
Std Dev 13.1
Entry
0
2
4
6
8
10
0
10
20
30
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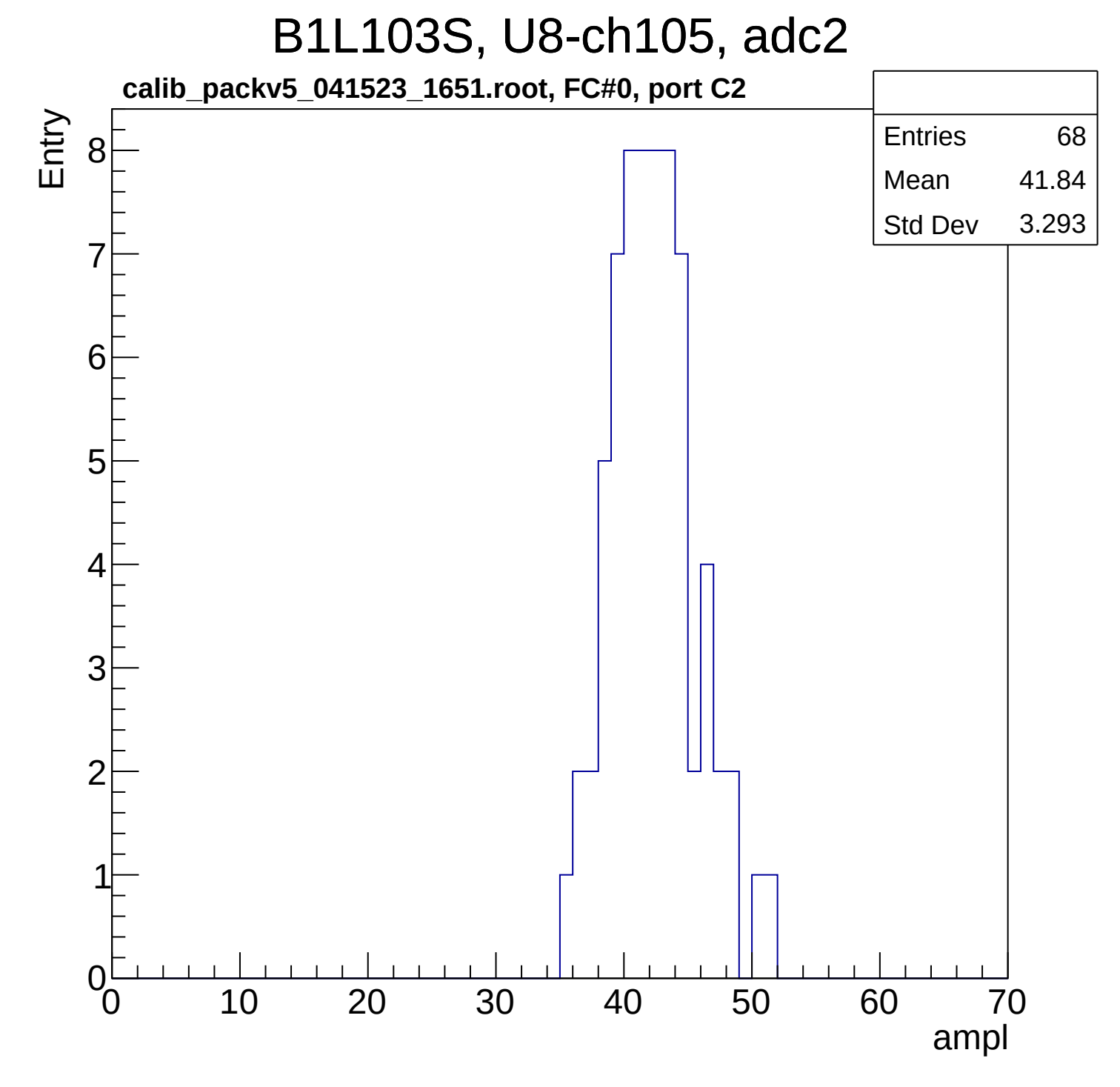
50
60
70
ampl


B1L103S, U8-ch105, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 41.84
Std Dev 3.293
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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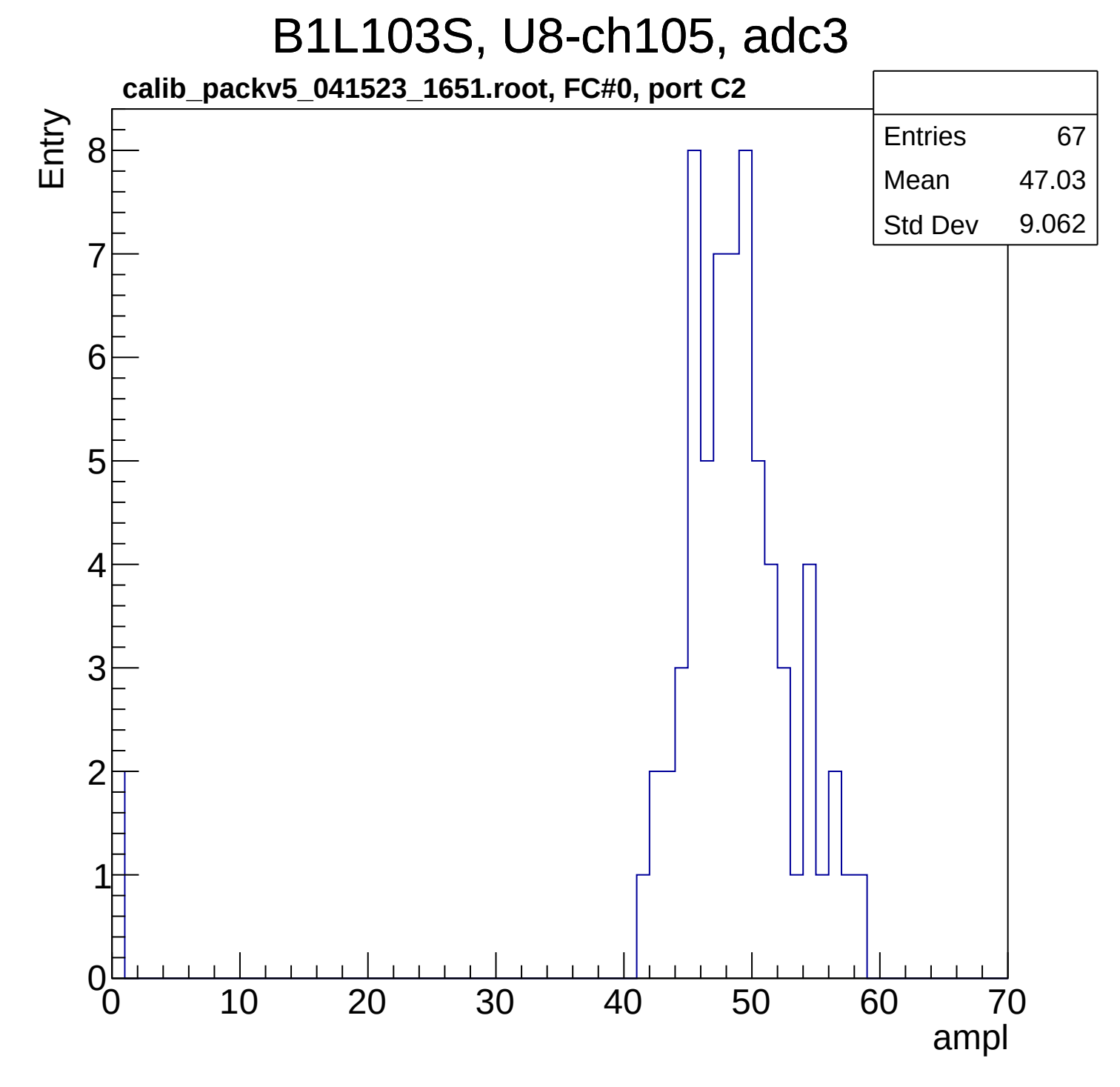
40
50
60
70


B1L103S, U8-ch105, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 47.03
Std Dev 9.062
Entry
ampl
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1
2
3
4
5
6
7
8
0
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40
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60
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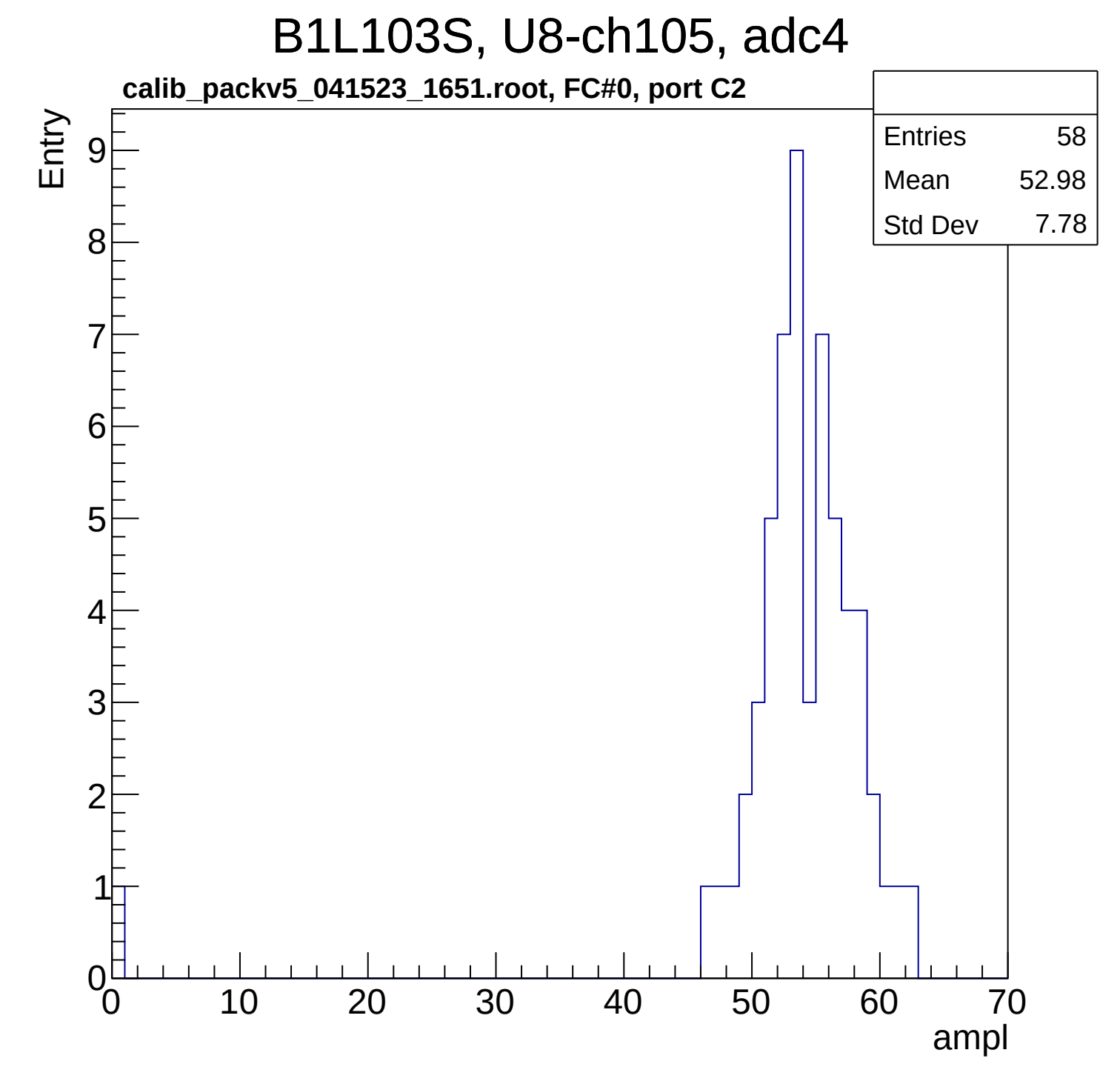
B1L103S, U8-ch105, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 52.98
Std Dev 7.78
Entry
ampl
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10
20
30
40
50
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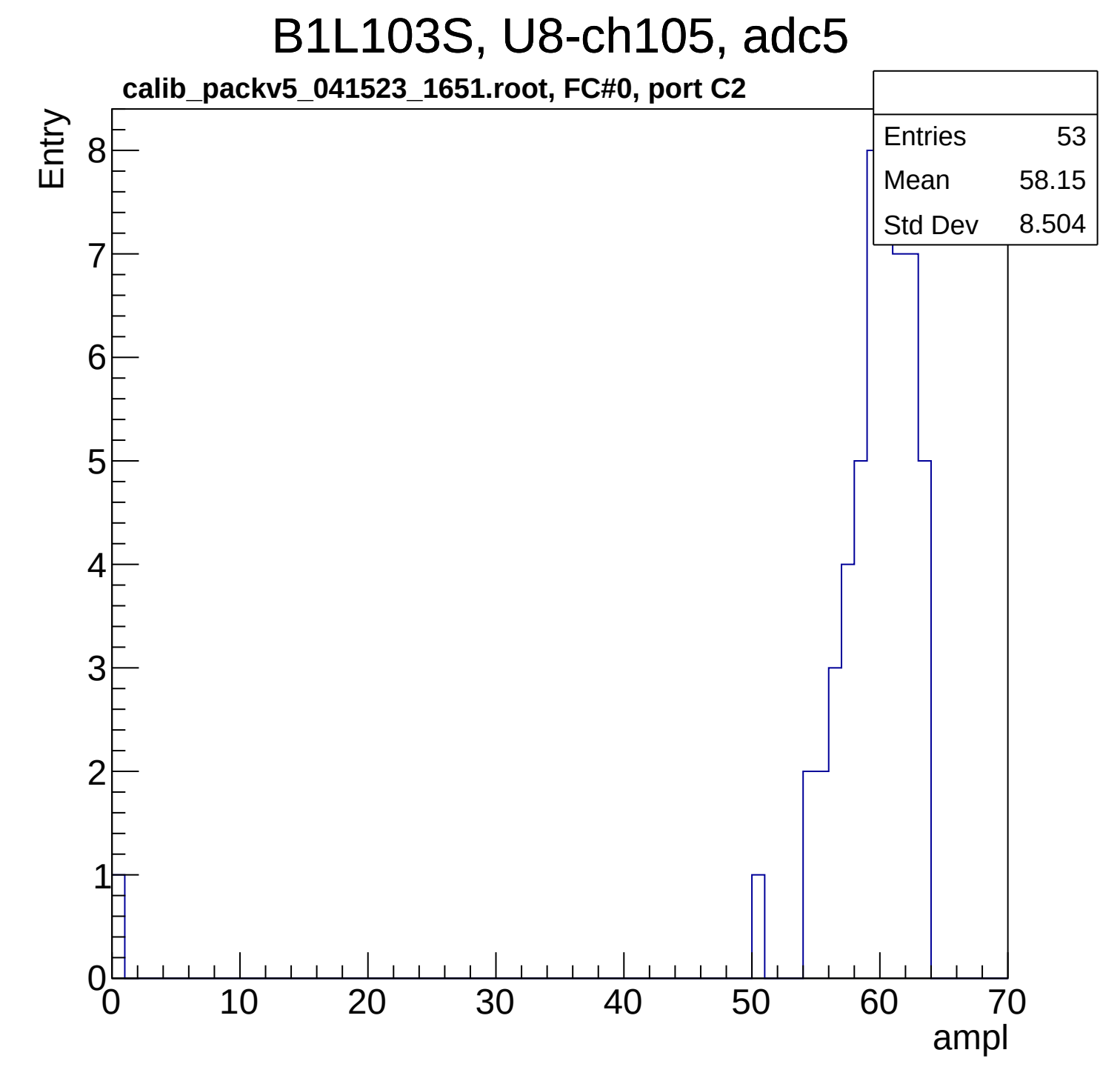
1
2
3
4
5
6
7
8
9


B1L103S, U8-ch105, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 58.15
Std Dev 8.504
Entry
ampl
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0
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60
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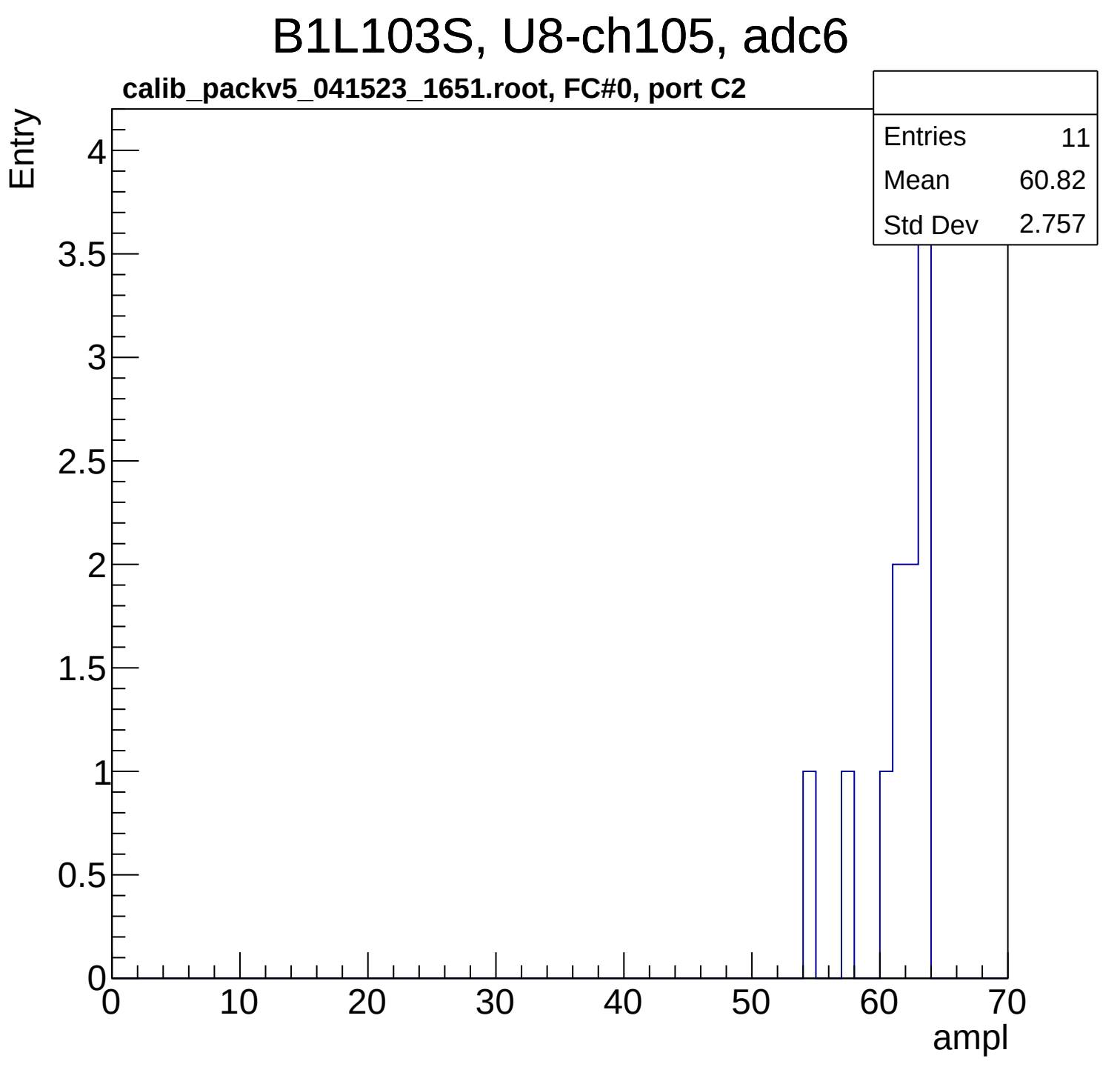
B1L103S, U8-ch105, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 60.82
Std Dev 2.757
Entry
ampl
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1
1.5
2
2.5
3
3.5
4
0
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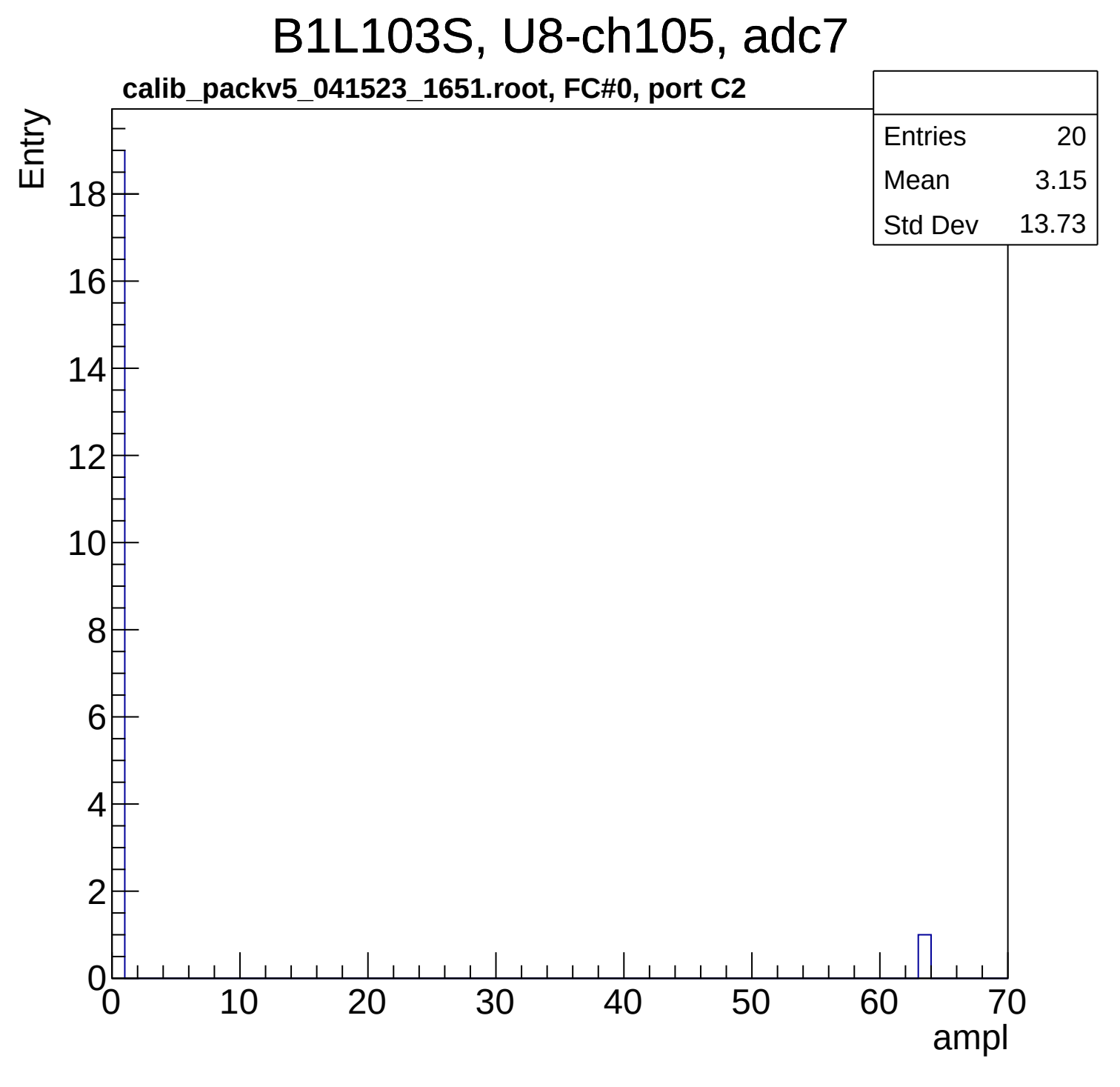
60
70


B1L103S, U8-ch105, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
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6
8
10
12
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16
18
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10
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30
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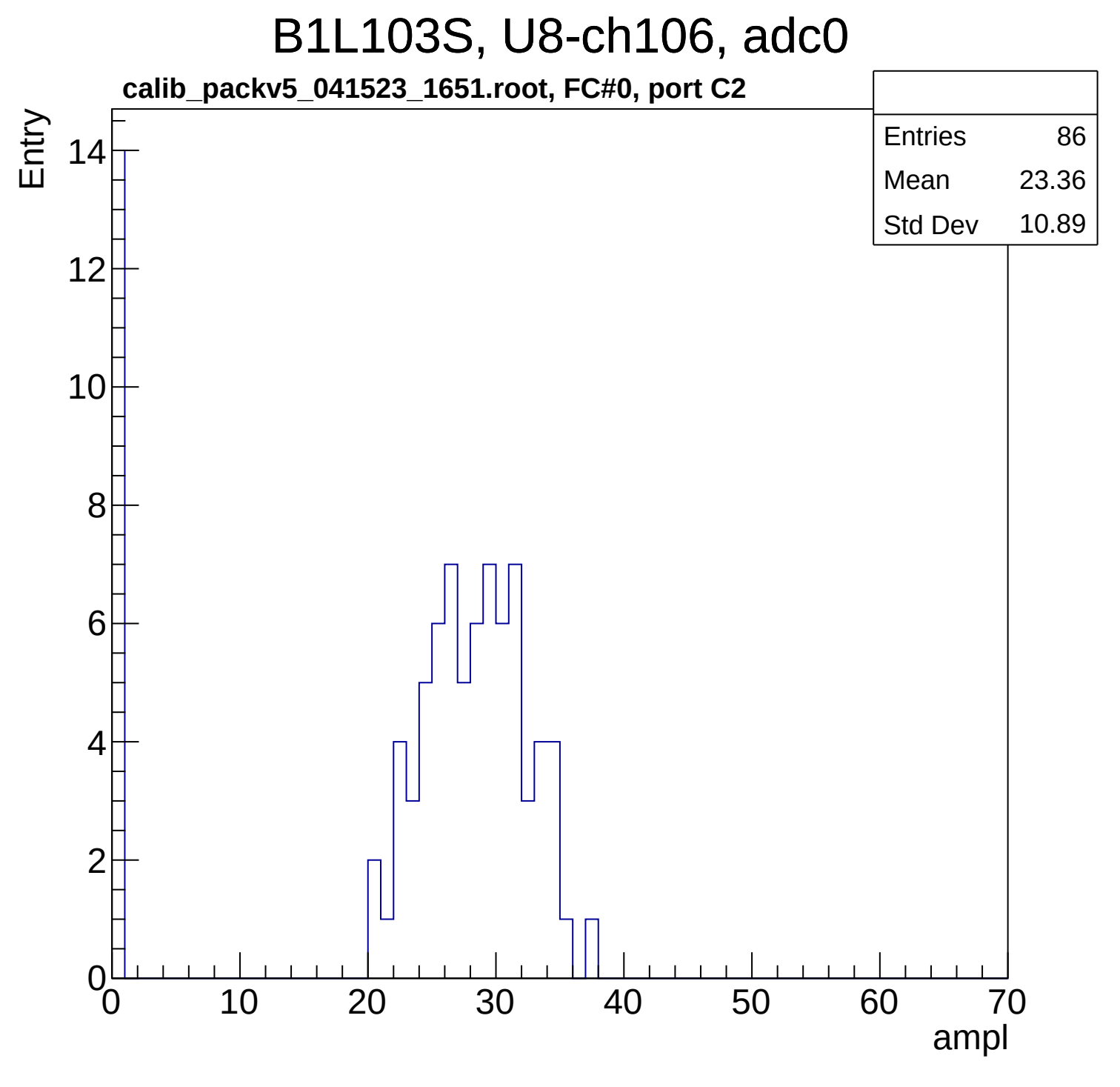
50
60
70
ampl


B1L103S, U8-ch106, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 23.36
Std Dev 10.89
Entry
ampl
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8
10
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0
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60
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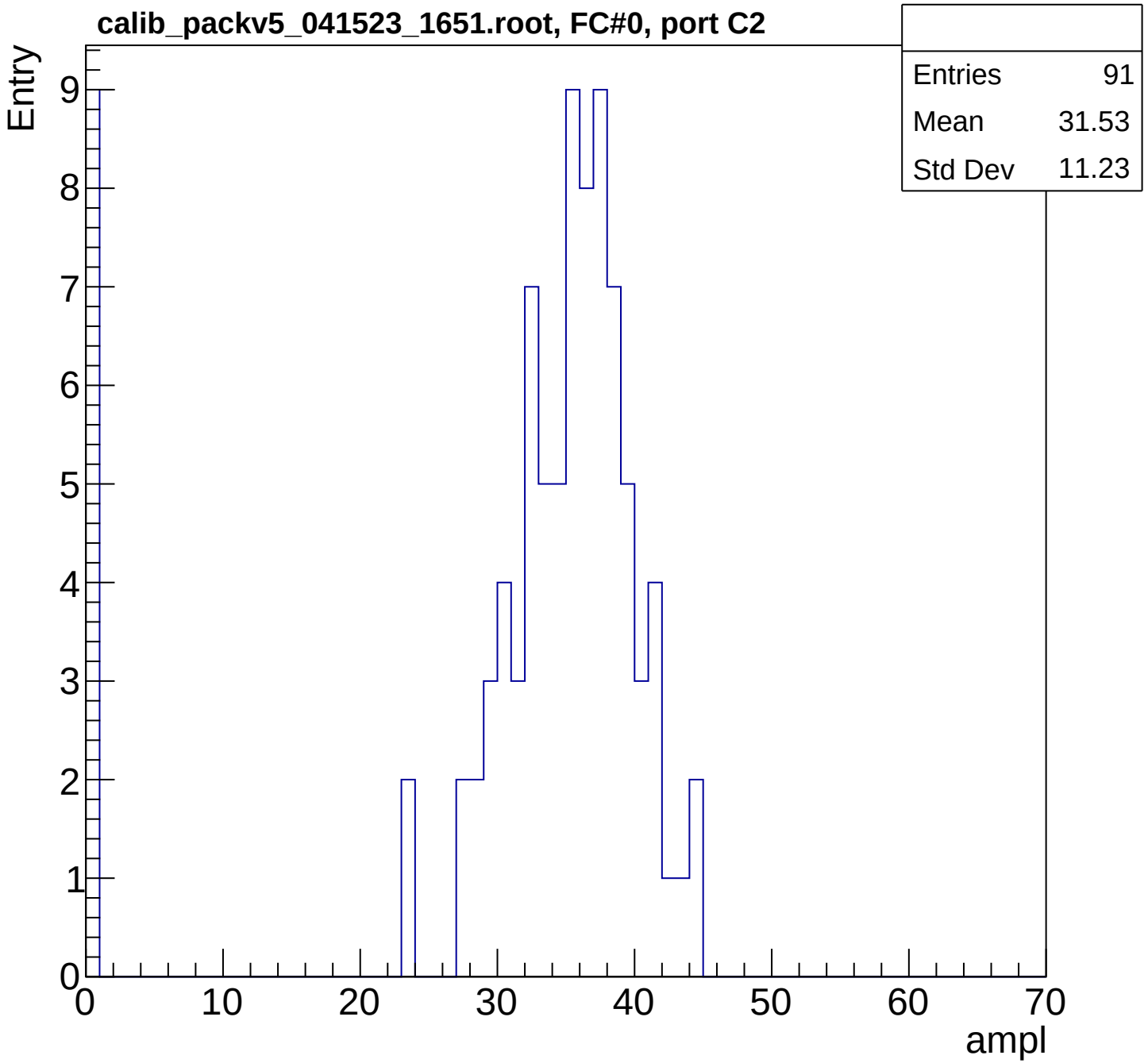
B1L103S, U8-ch106, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 31.53
Std Dev 11.23
Entry
ampl
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6
7
8
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0
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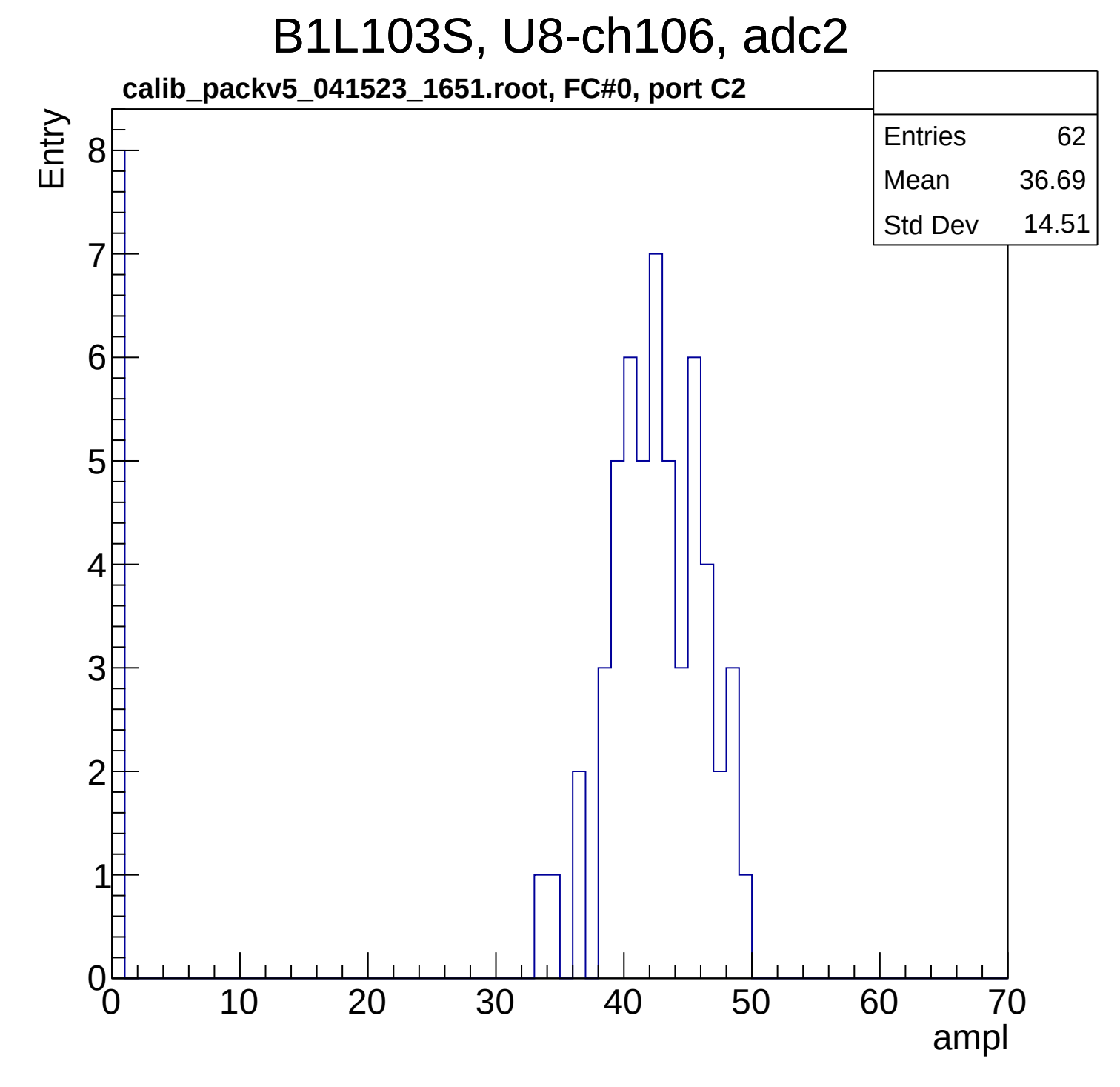
60
70


B1L103S, U8-ch106, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 36.69
Std Dev 14.51
Entry
ampl
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2
3
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5
6
7
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0
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50
60
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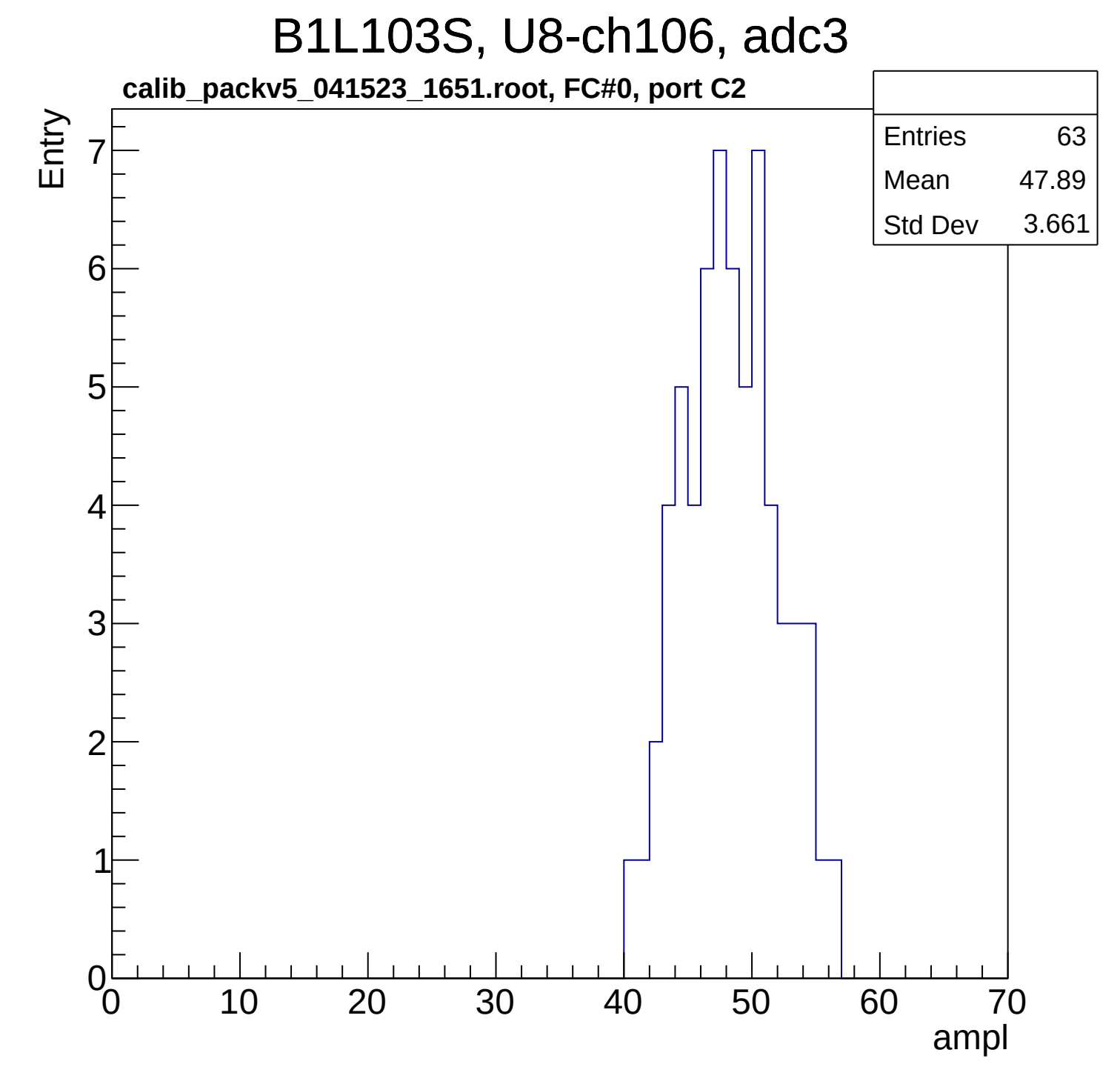
B1L103S, U8-ch106, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 47.89
Std Dev 3.661
Entry
ampl
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3
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5
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0
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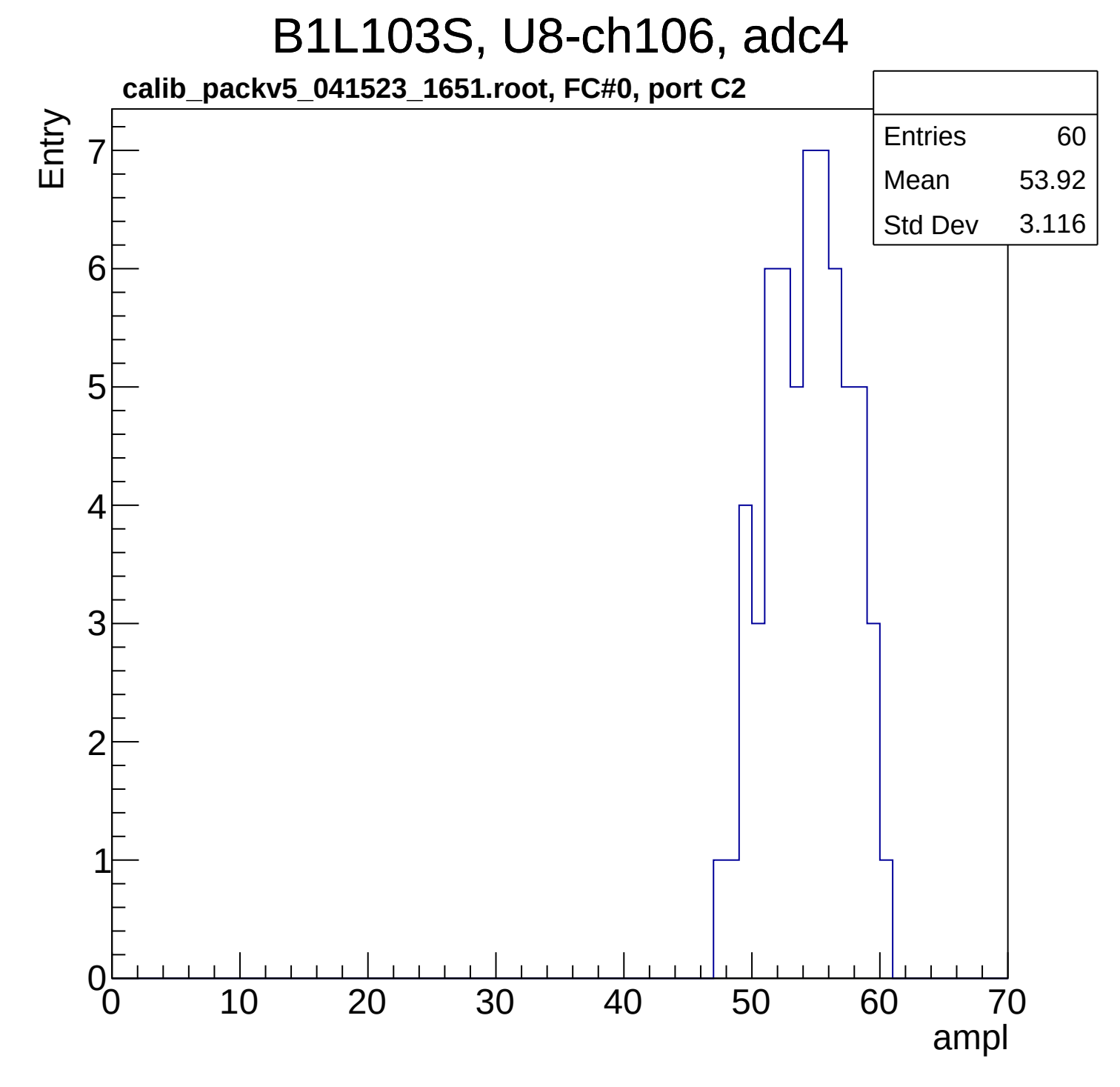
60
70


B1L103S, U8-ch106, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 53.92
Std Dev 3.116
Entry
ampl
0
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5
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0
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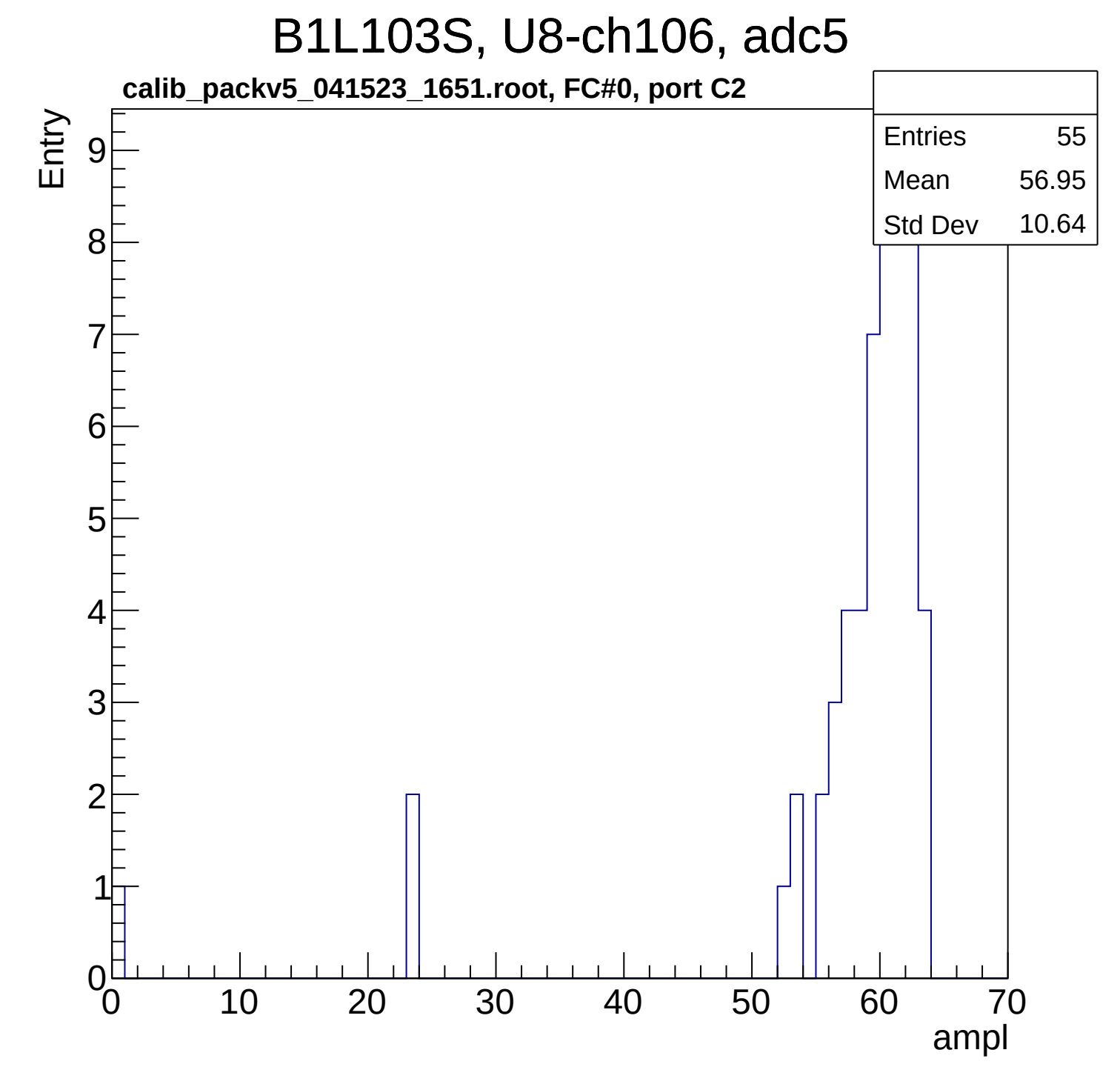
40
50
60
70


B1L103S, U8-ch106, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 56.95
Std Dev 10.64
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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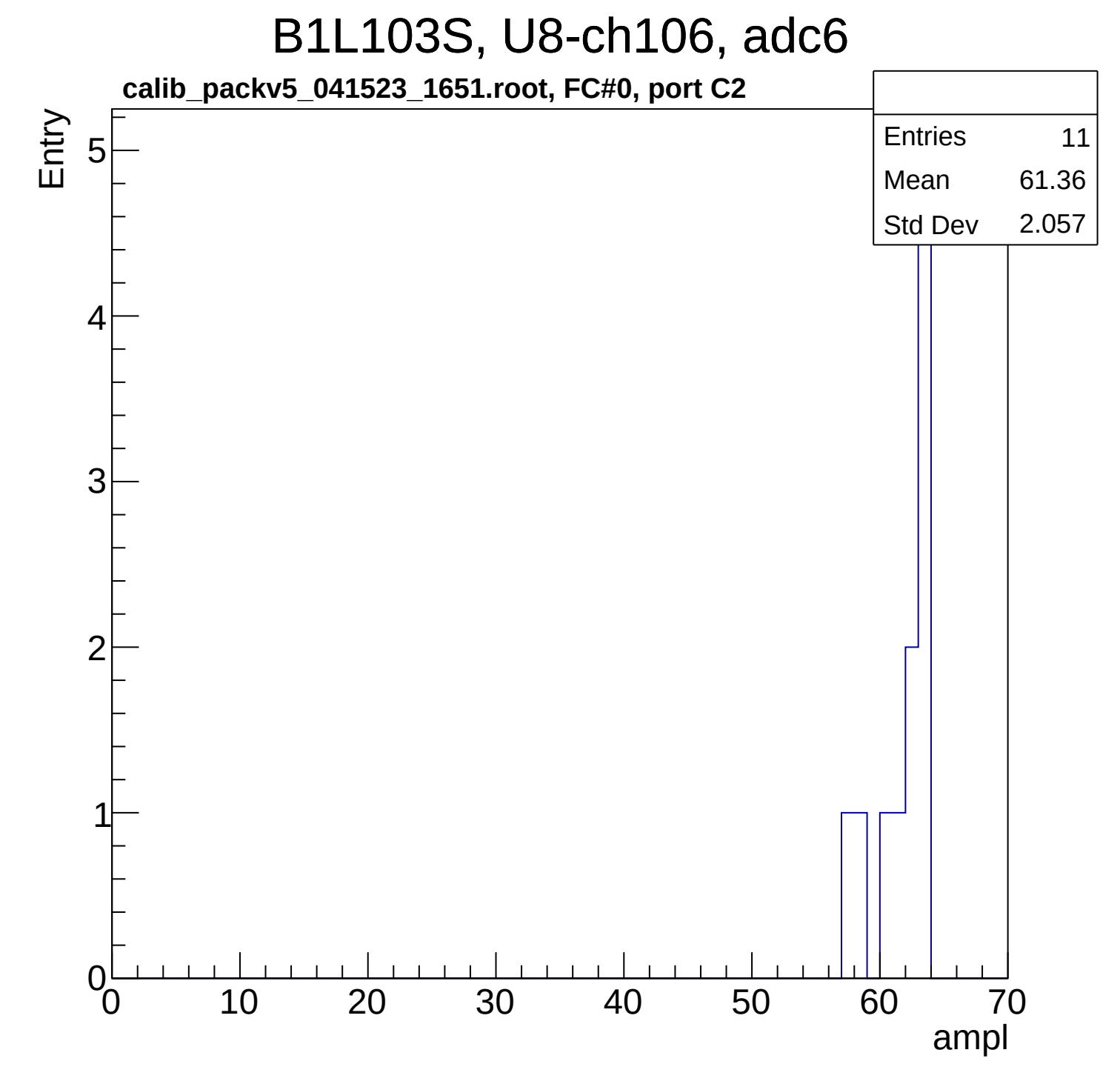
50
60
70


B1L103S, U8-ch106, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 61.36
Std Dev 2.057
Entry
ampl
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2
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4
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0
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20
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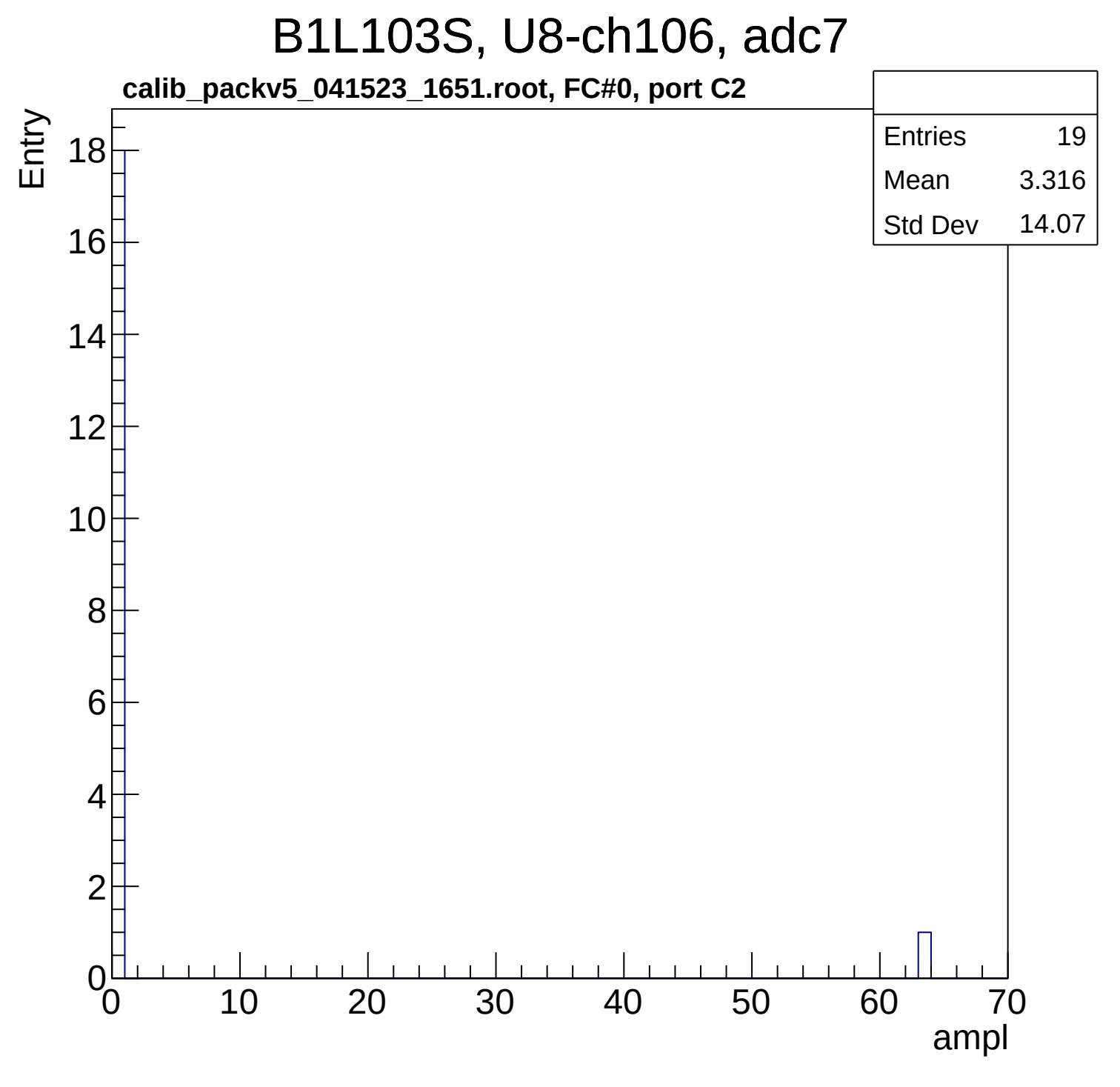
40
50
60
70


B1L103S, U8-ch106, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.316
Std Dev 14.07
Entry
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6
8
10
12
14
16
18
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10
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30
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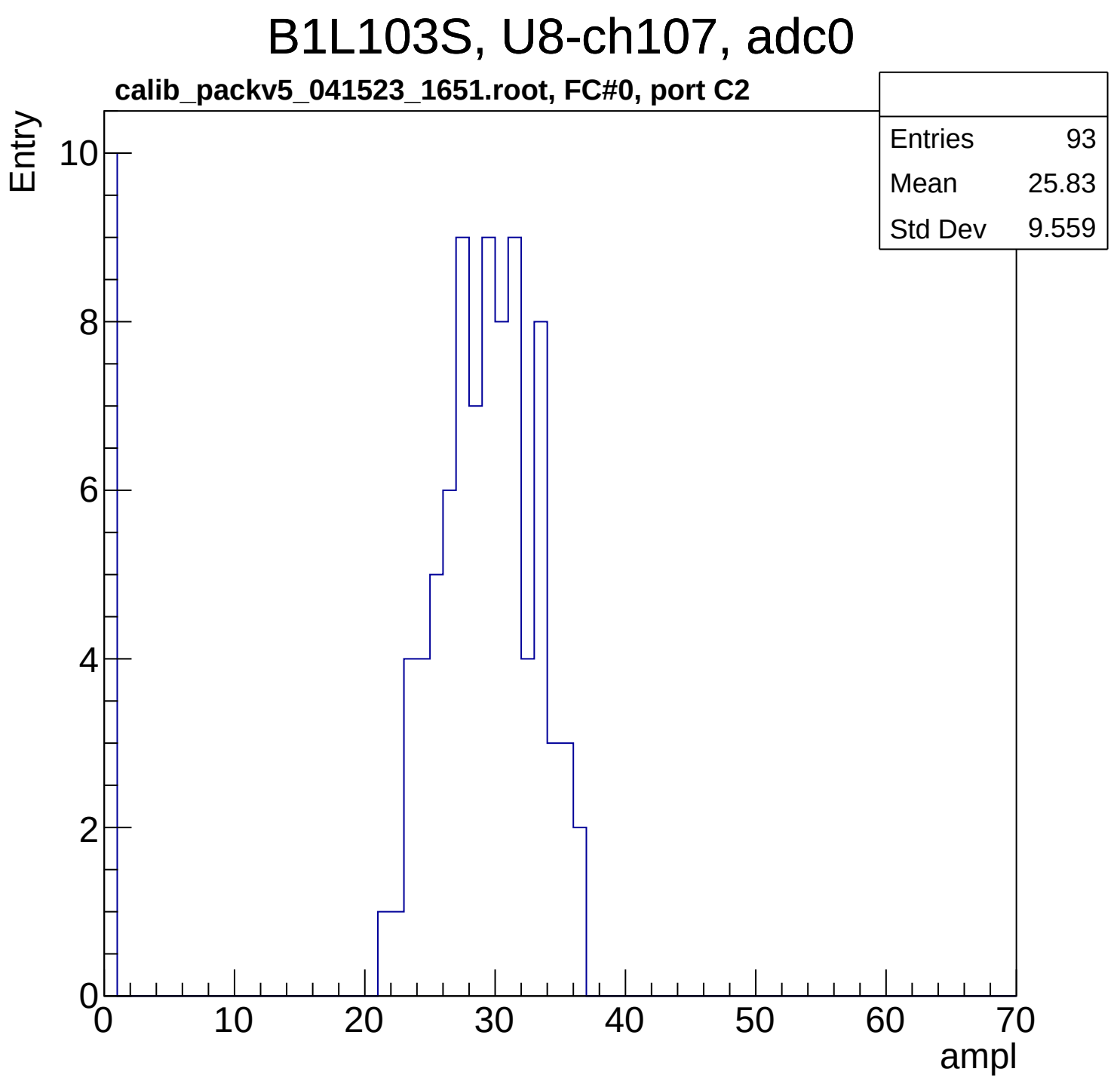
50
60
70
ampl


B1L103S, U8-ch107, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 25.83
Std Dev 9.559
Entry
ampl
0
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4
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10
0
10
20
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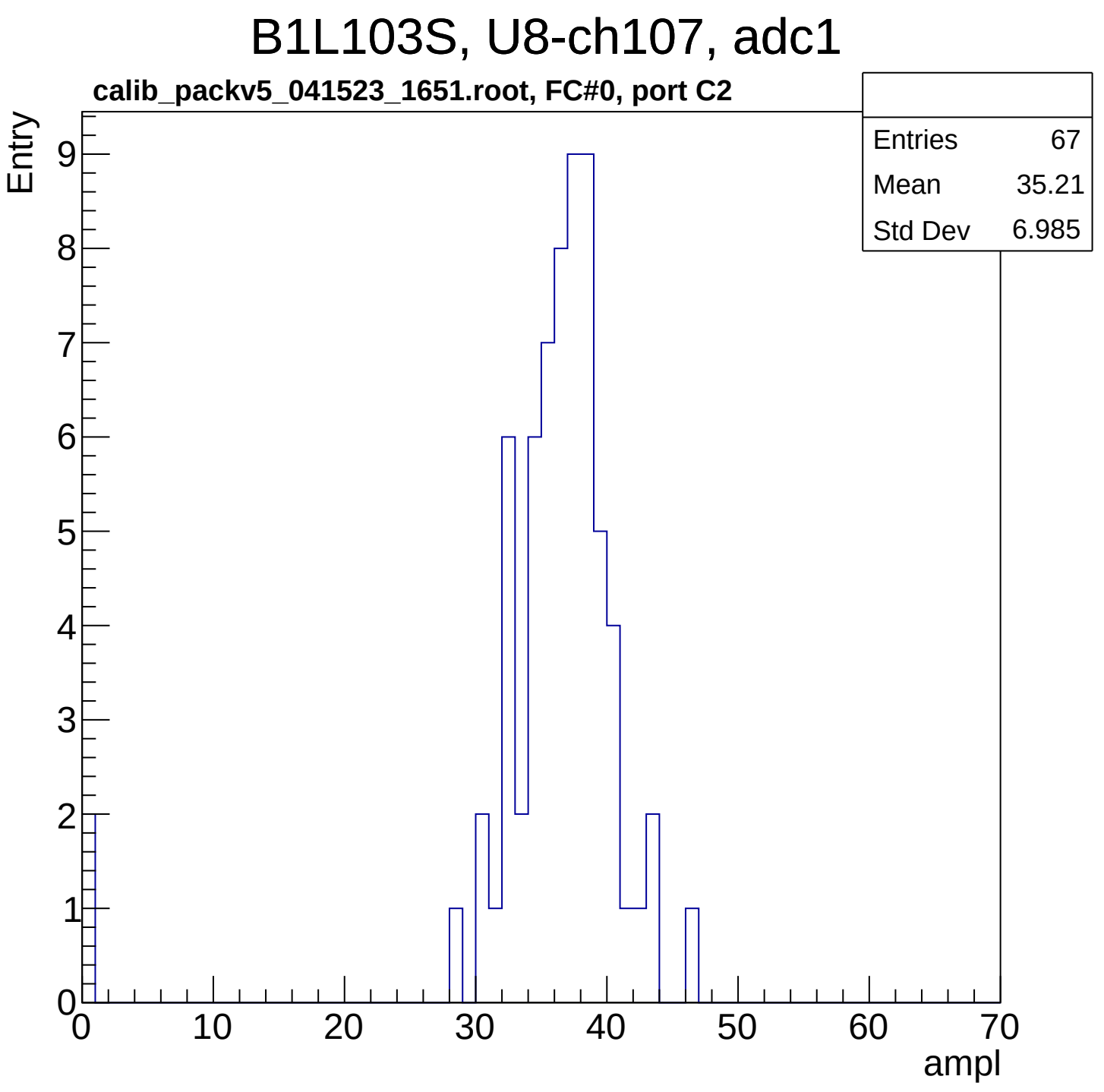
40
50
60
70


B1L103S, U8-ch107, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 35.21
Std Dev 6.985
Entry
ampl
0
1
2
3
4
5
6
7
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0
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60
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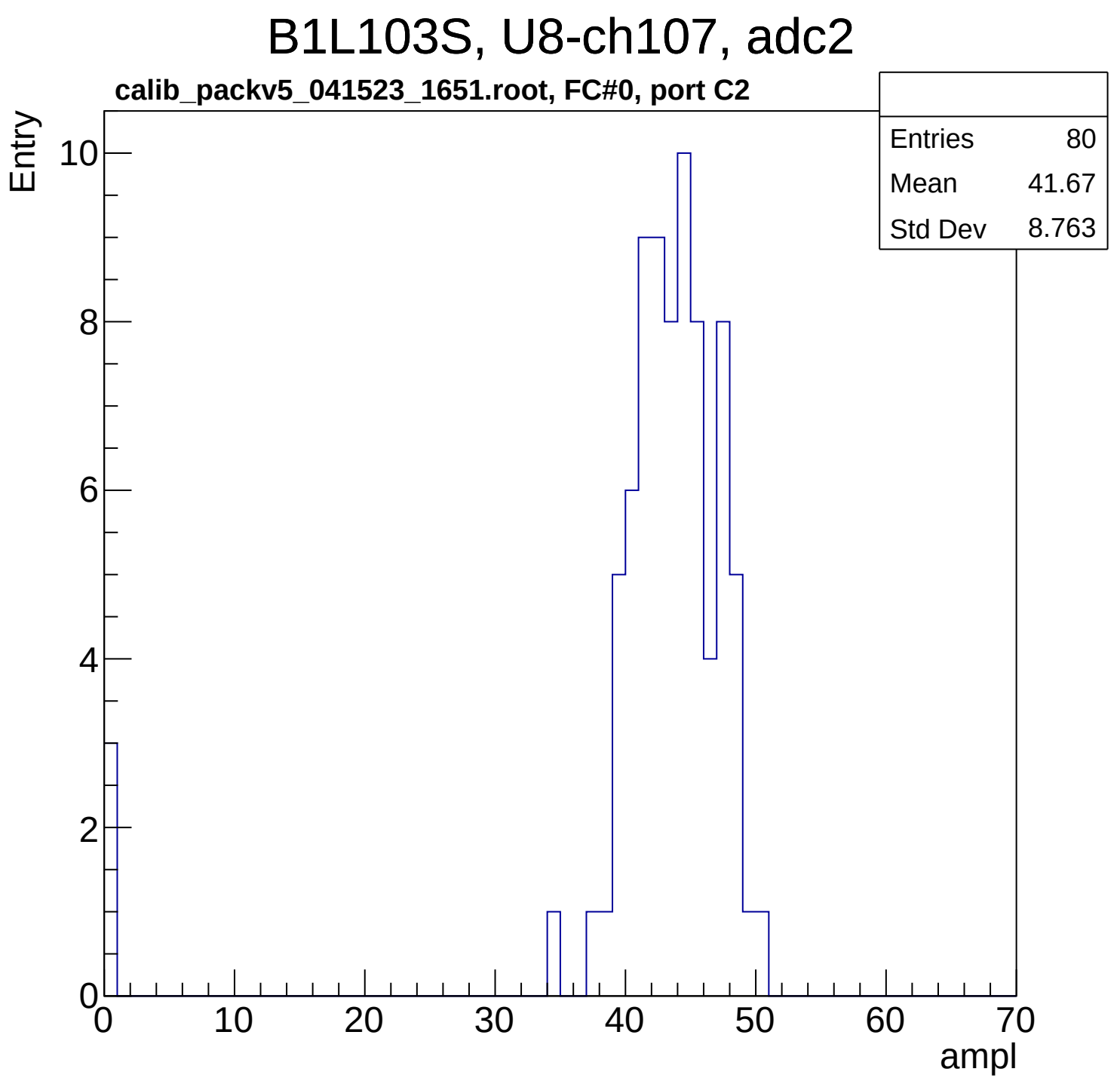
B1L103S, U8-ch107, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 41.67
Std Dev 8.763
Entry
0
2
4
6
8
10
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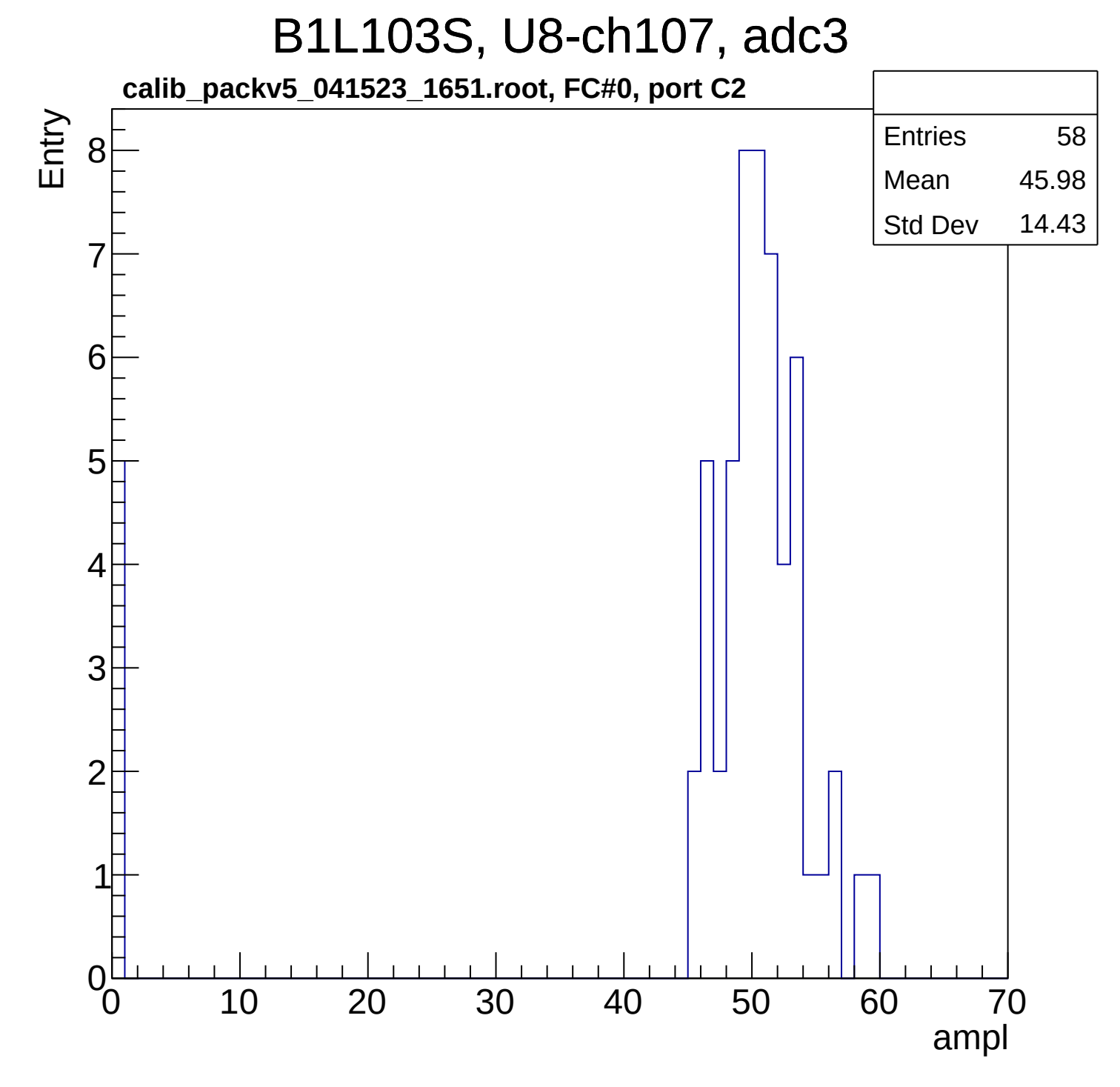
70
ampl


B1L103S, U8-ch107, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 45.98
Std Dev 14.43
Entry
ampl
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3
4
5
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7
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0
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40
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60
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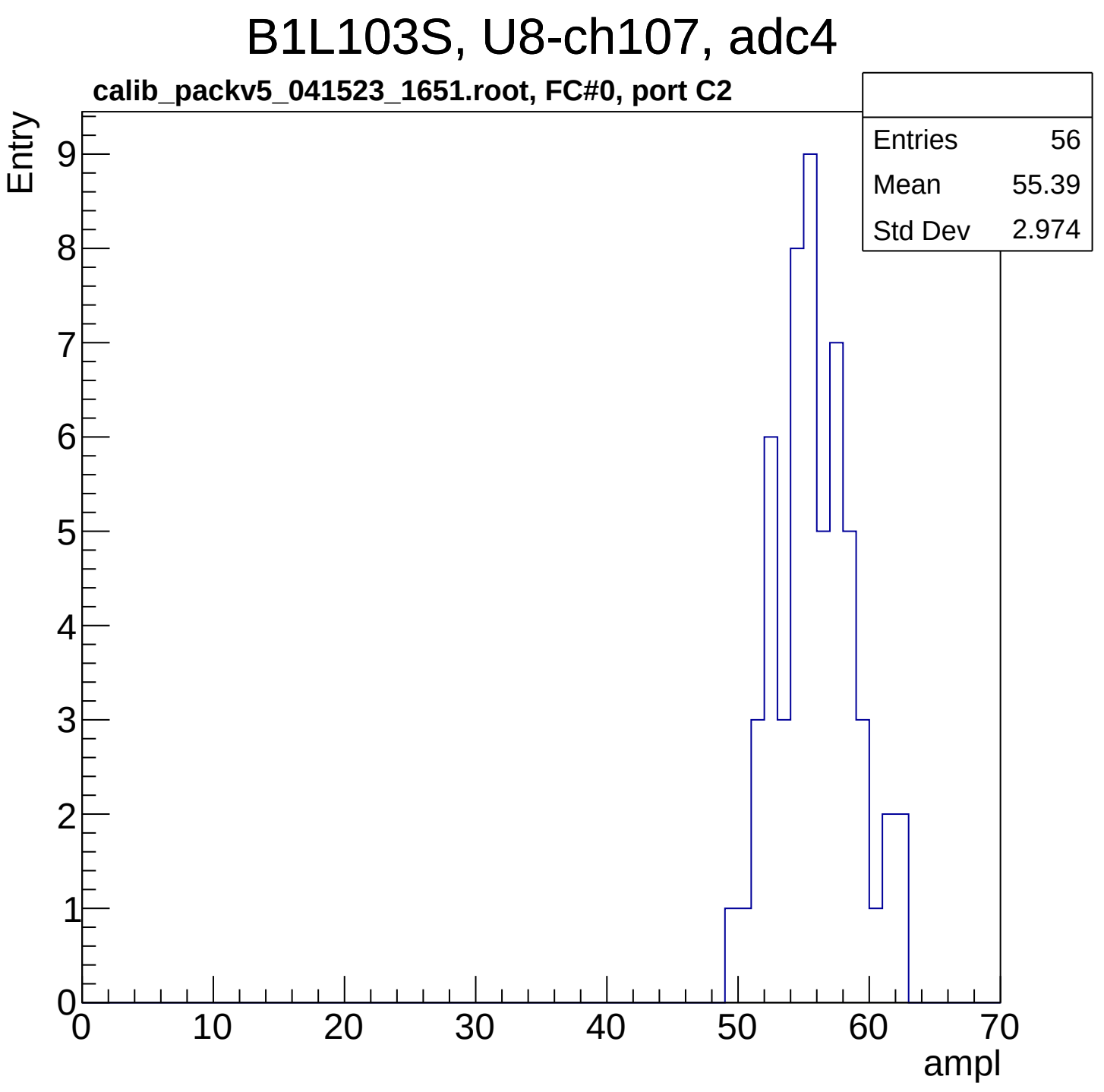
B1L103S, U8-ch107, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 55.39
Std Dev 2.974
Entry
ampl
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3
4
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6
7
8
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0
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60
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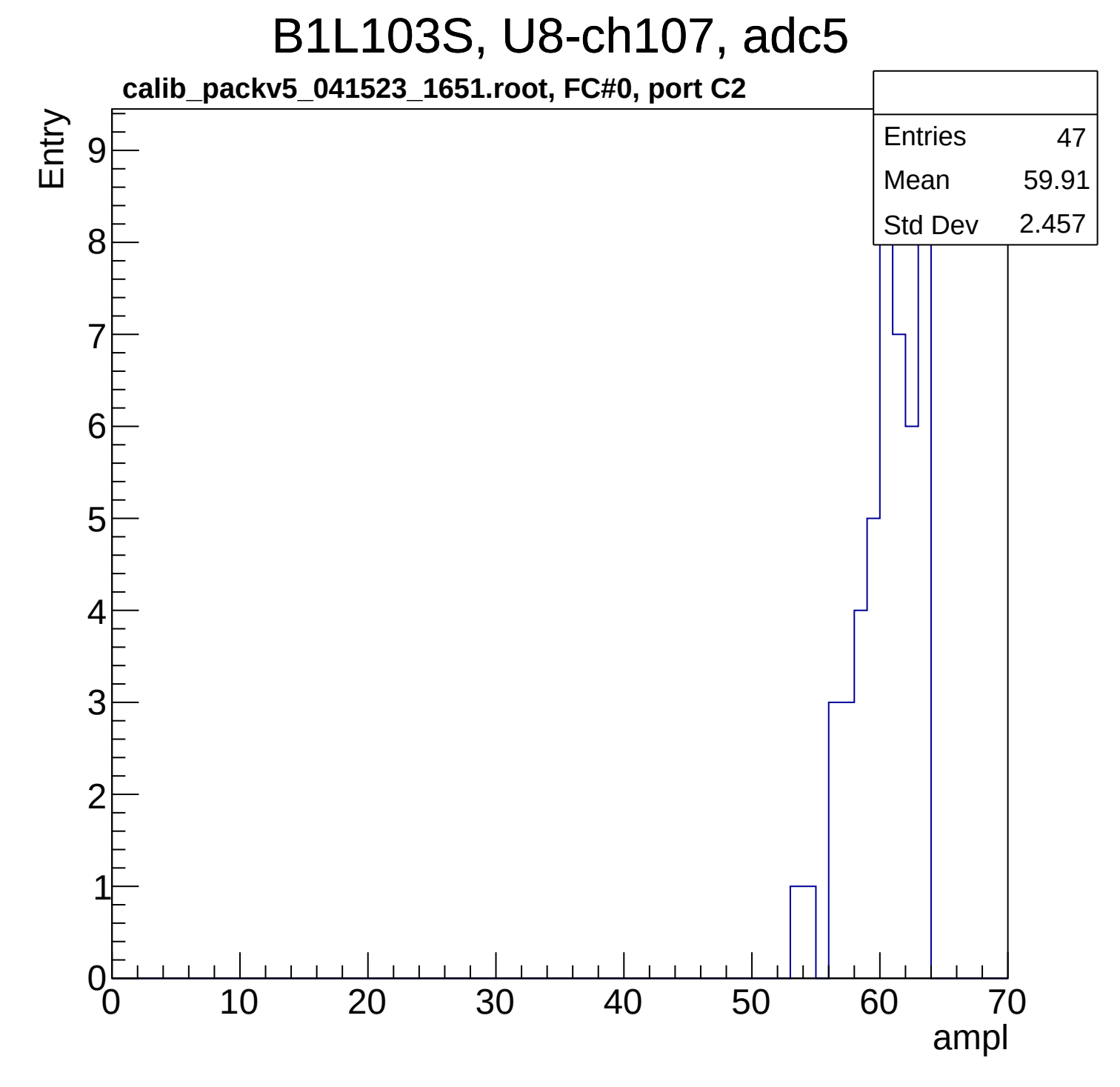
B1L103S, U8-ch107, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 59.91
Std Dev 2.457
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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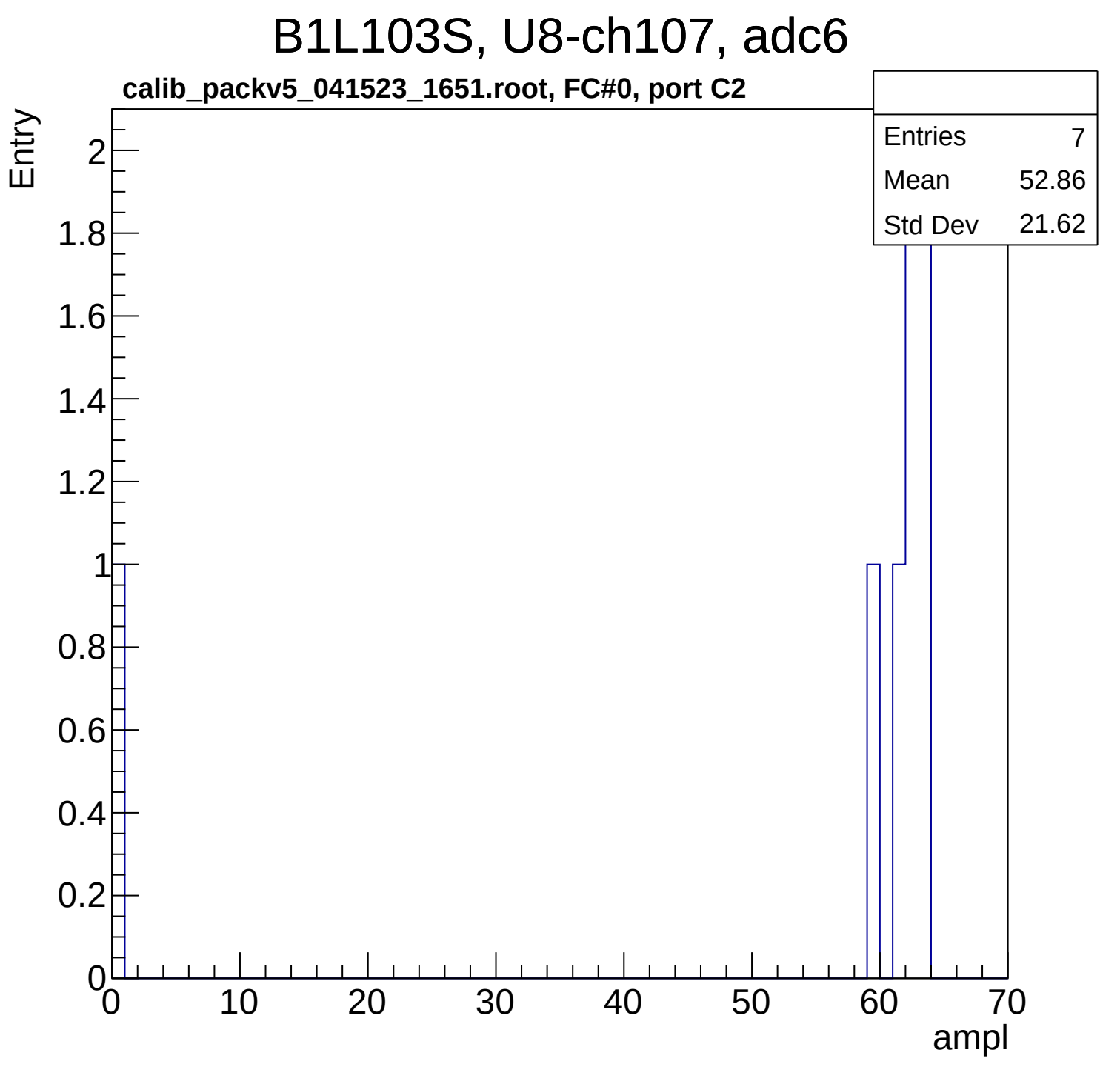
B1L103S, U8-ch107, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 52.86
Std Dev 21.62
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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40
50
60
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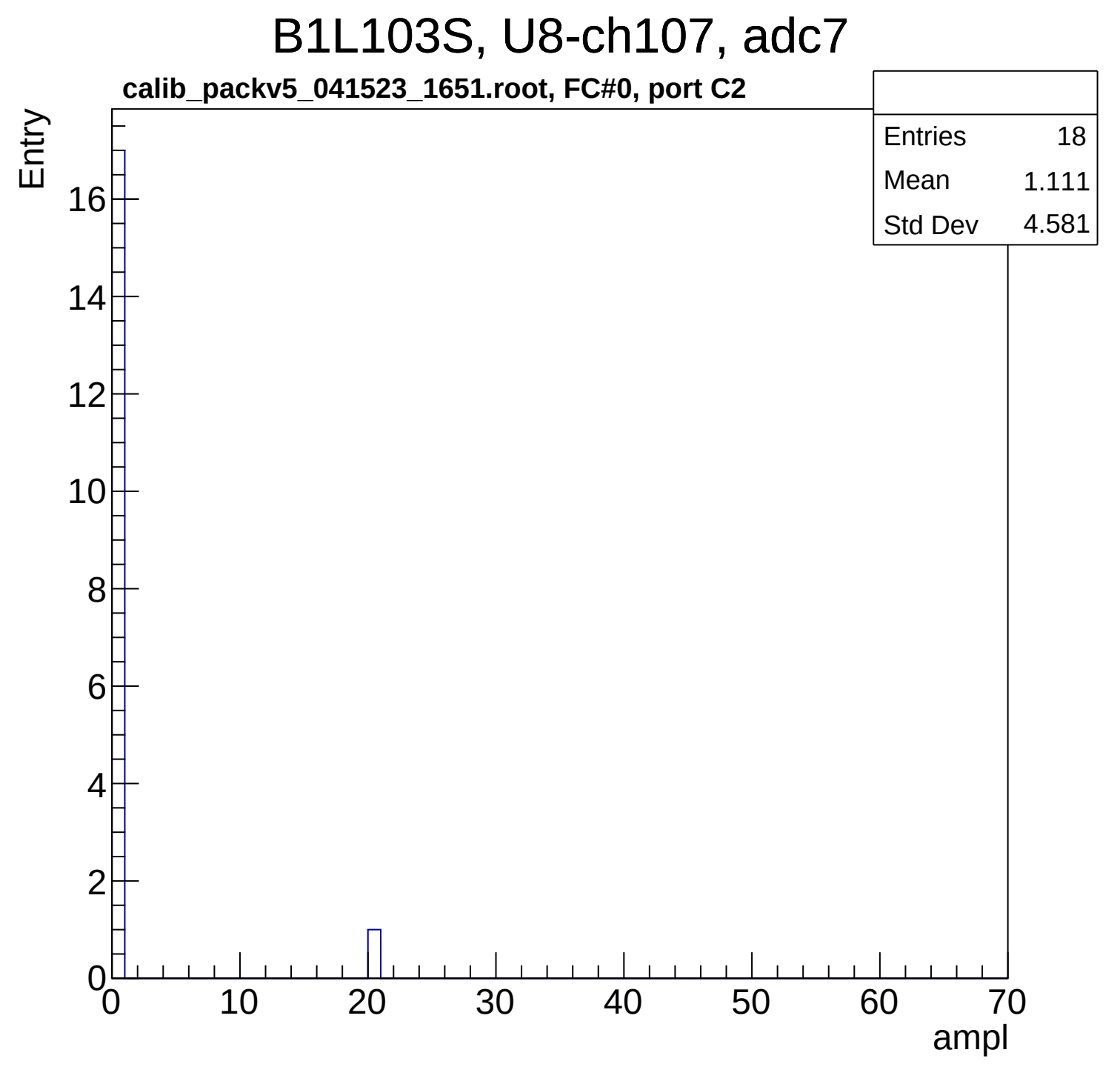
B1L103S, U8-ch107, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.111
Std Dev 4.581
Entry
0
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4
6
8
10
12
14
16
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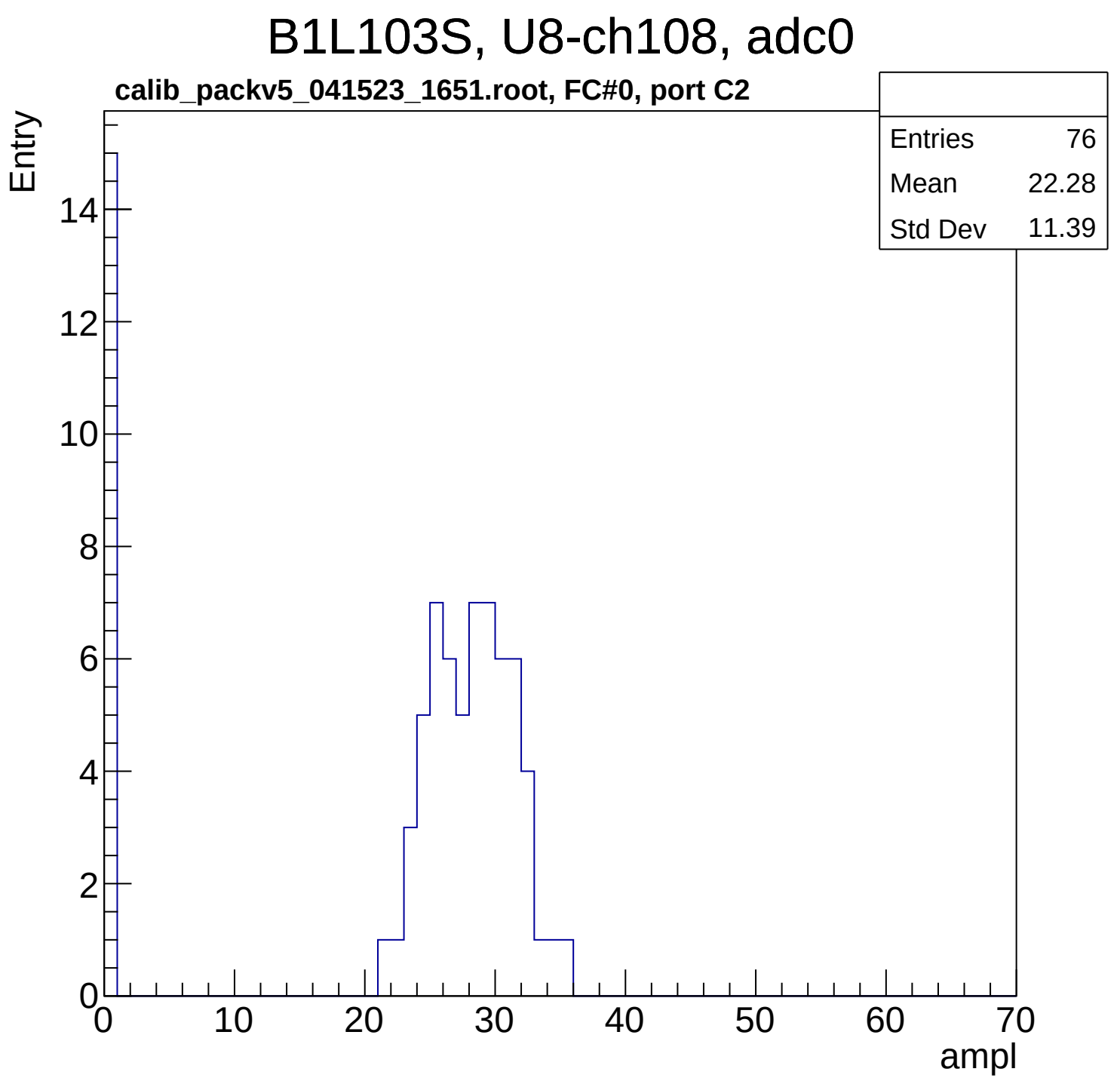
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch108, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 22.28
Std Dev 11.39
Entry
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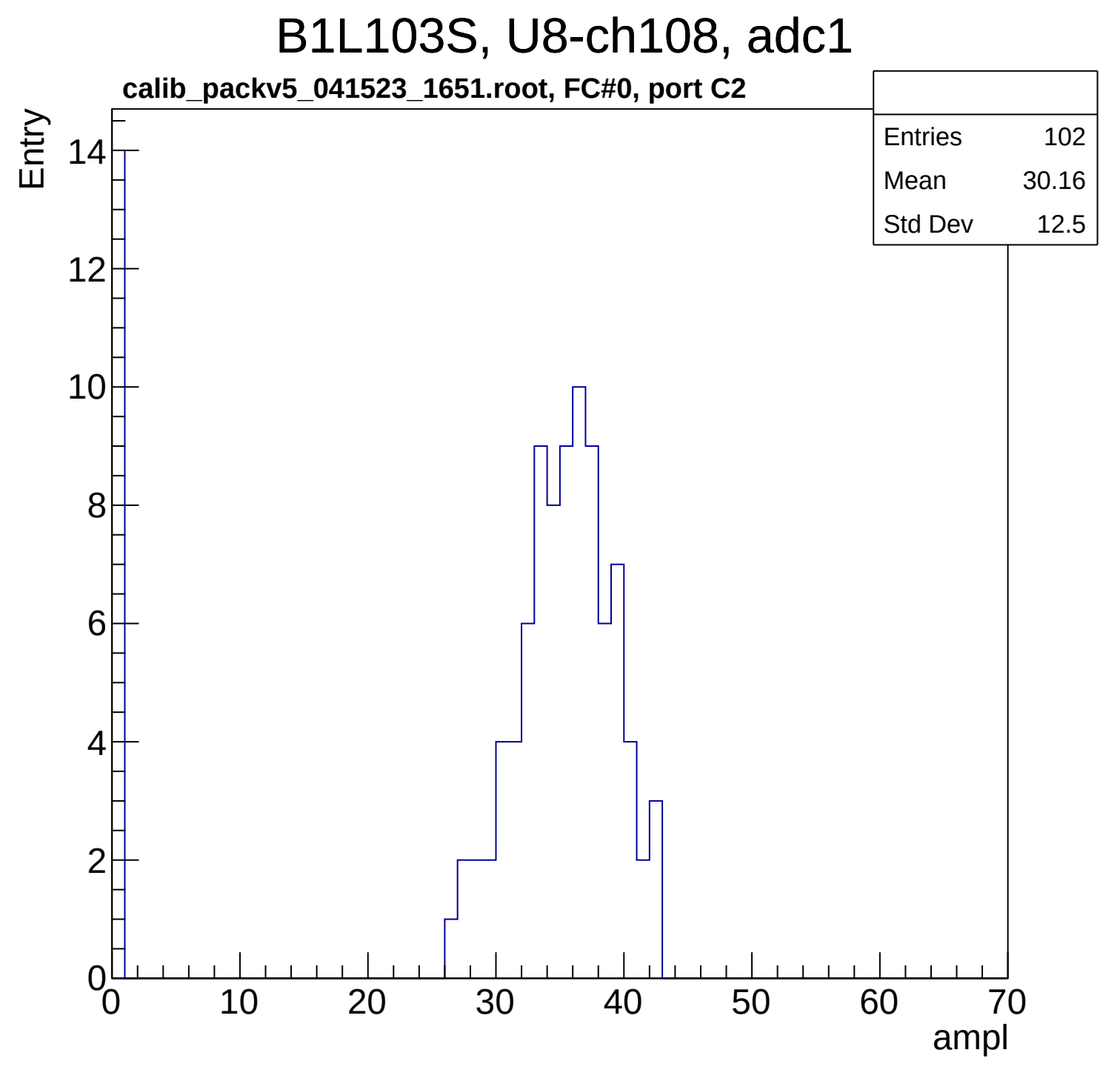
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch108, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 102
Mean 30.16
Std Dev 12.5
Entry
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2
4
6
8
10
12
14
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10
20
30
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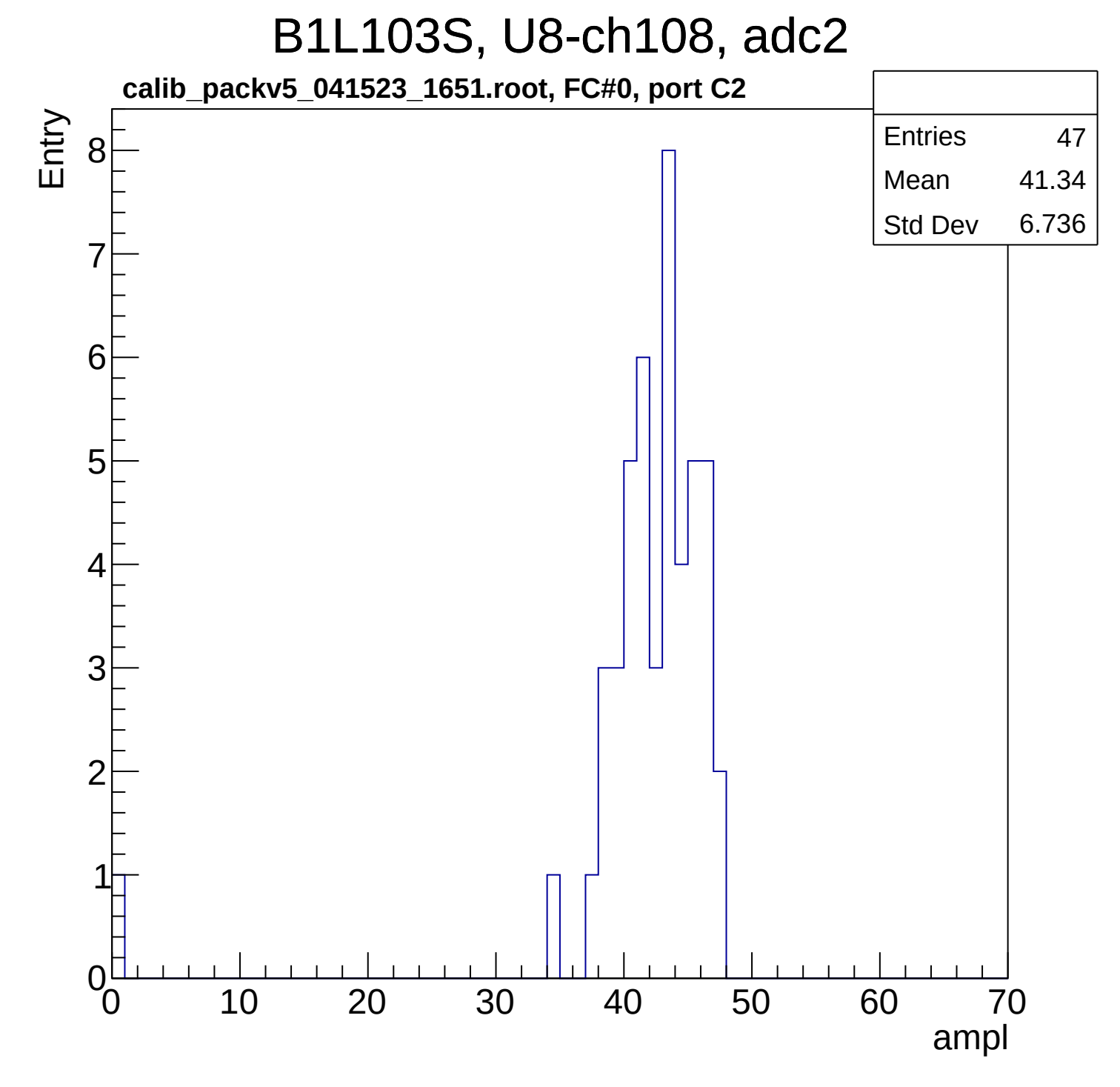
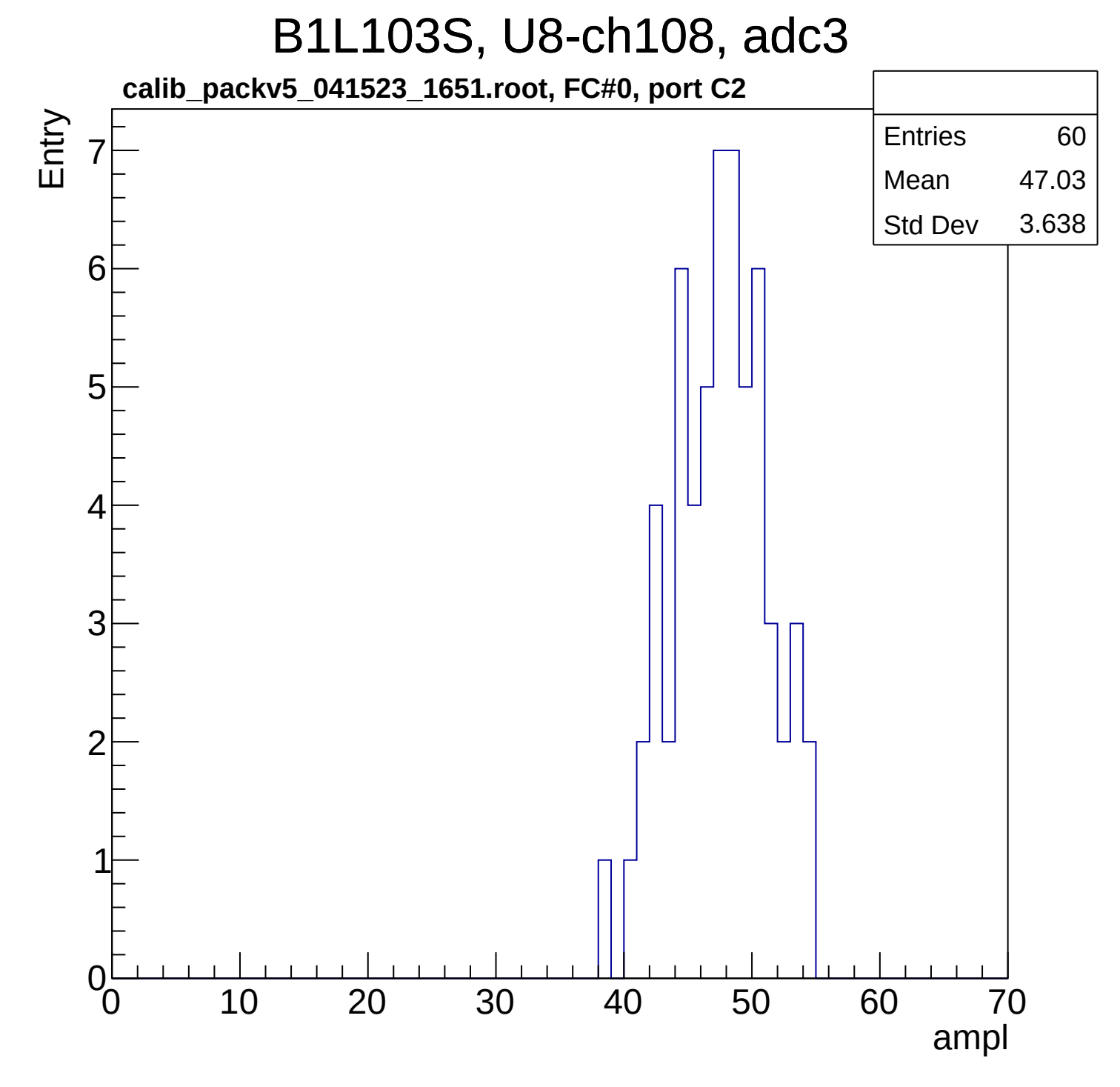
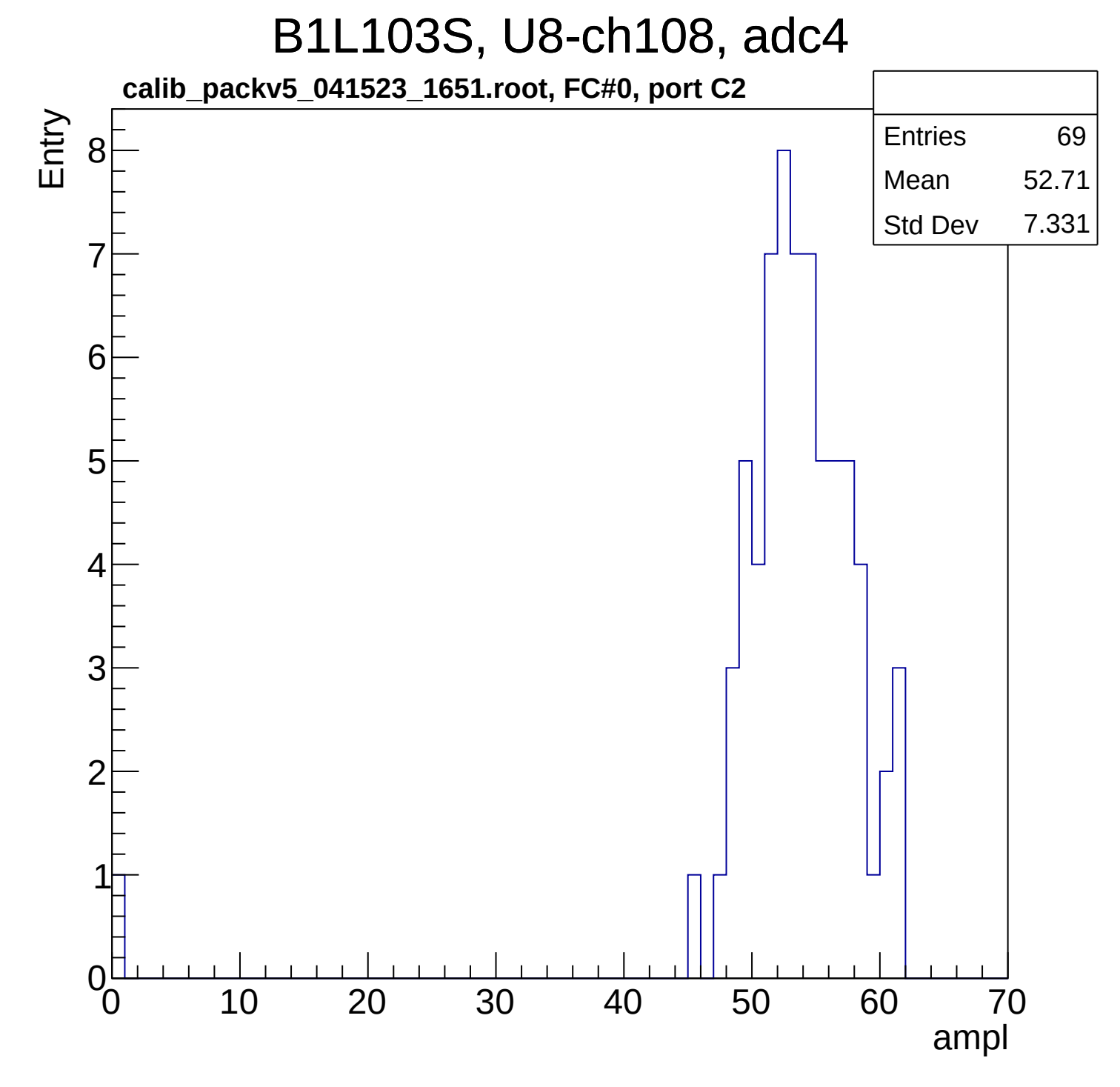
50
60
70
ampl


B1L103S, U8-ch108, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 41.34
Std Dev 6.736
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch108, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 47.03
Std Dev 3.638
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U8-ch108, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 52.71
Std Dev 7.331
Entry
ampl
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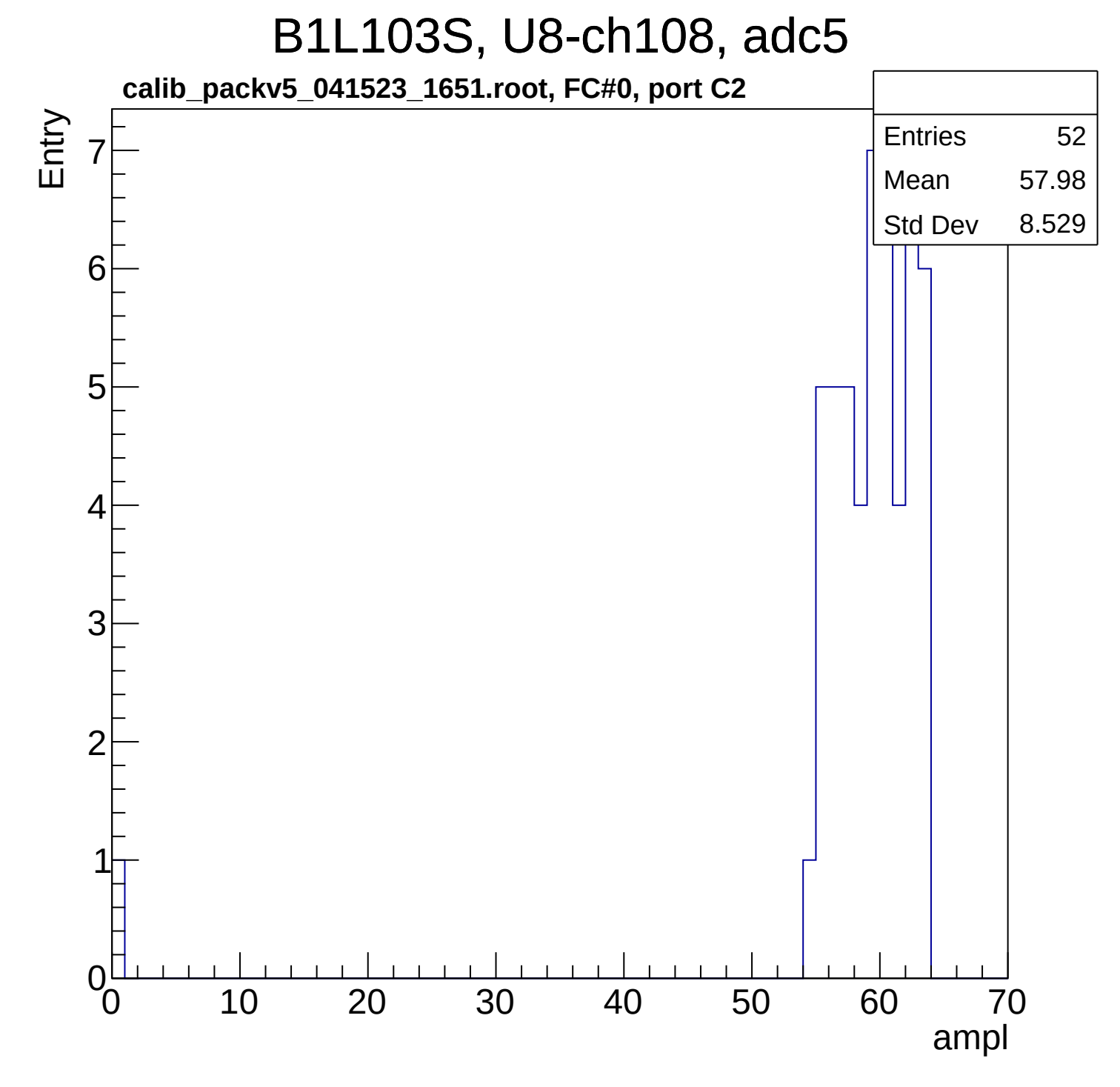
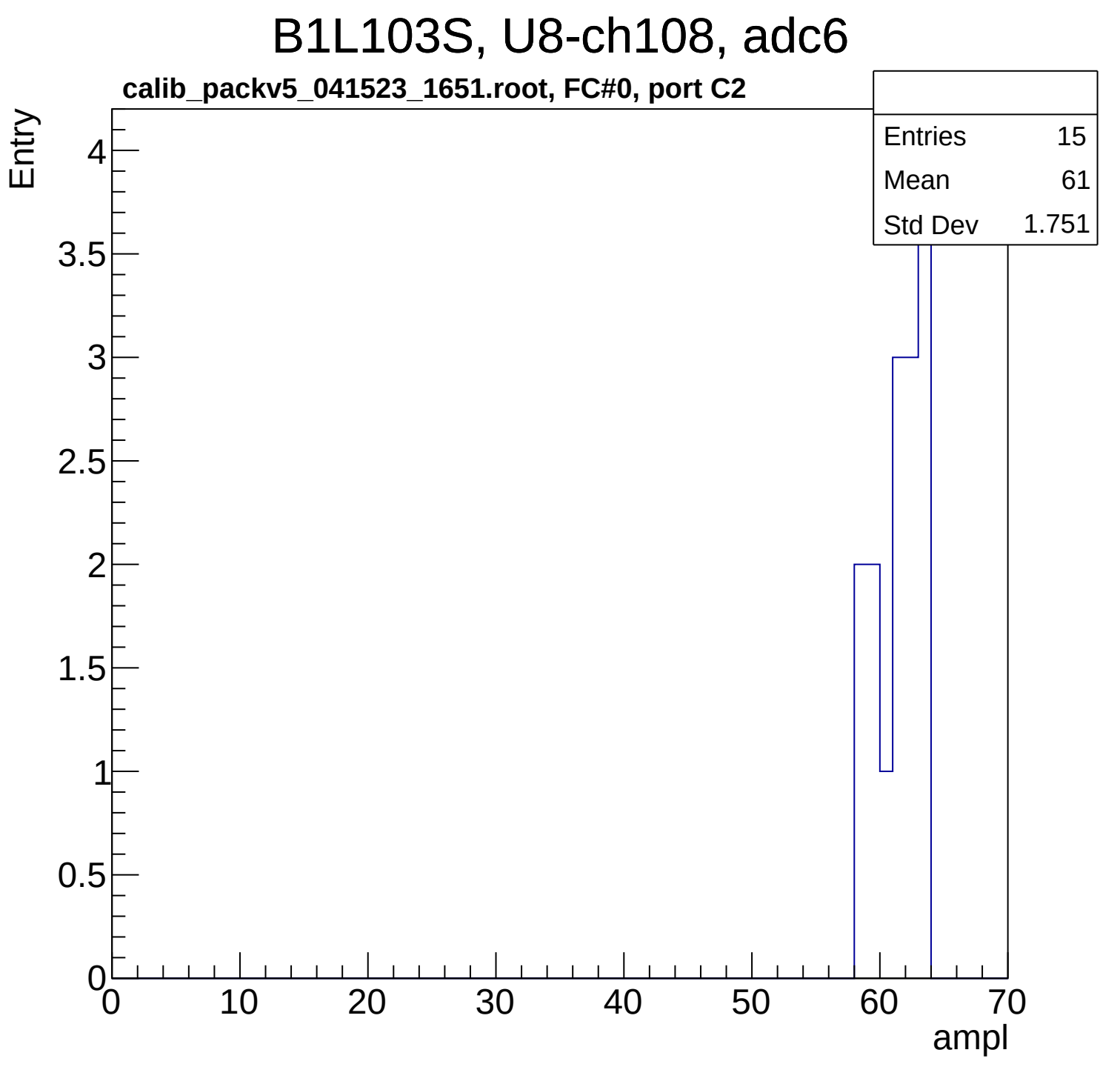
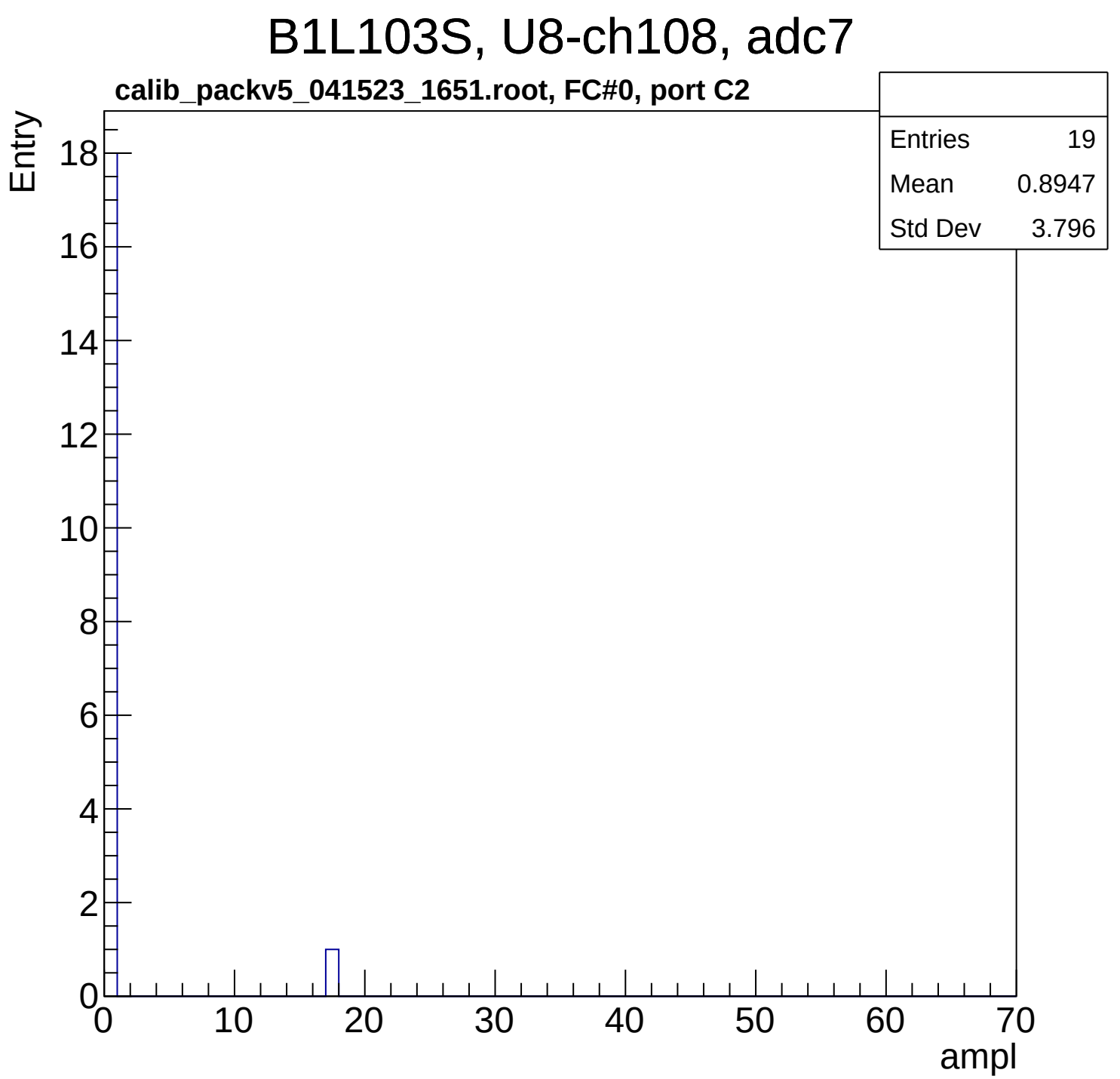
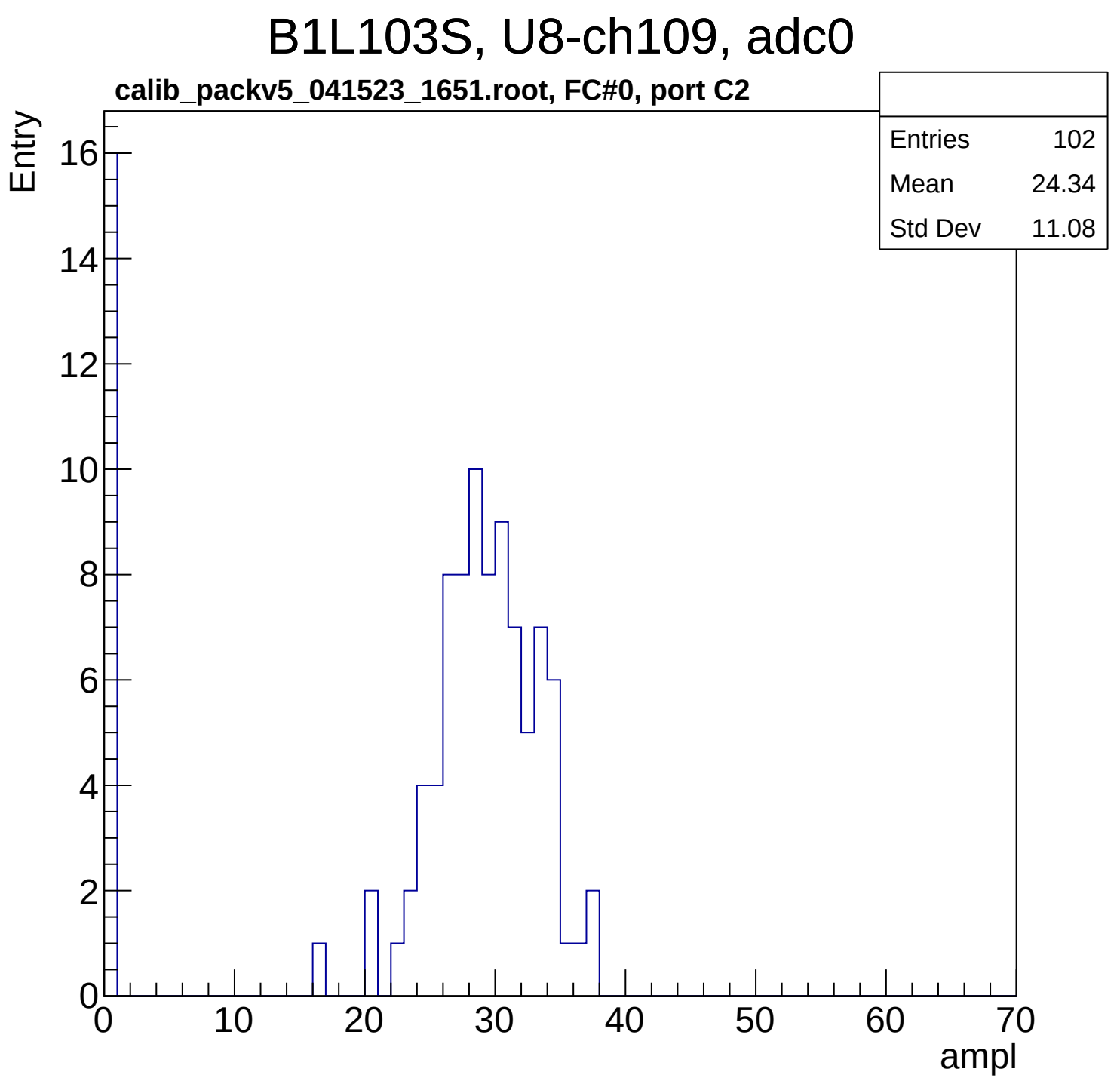
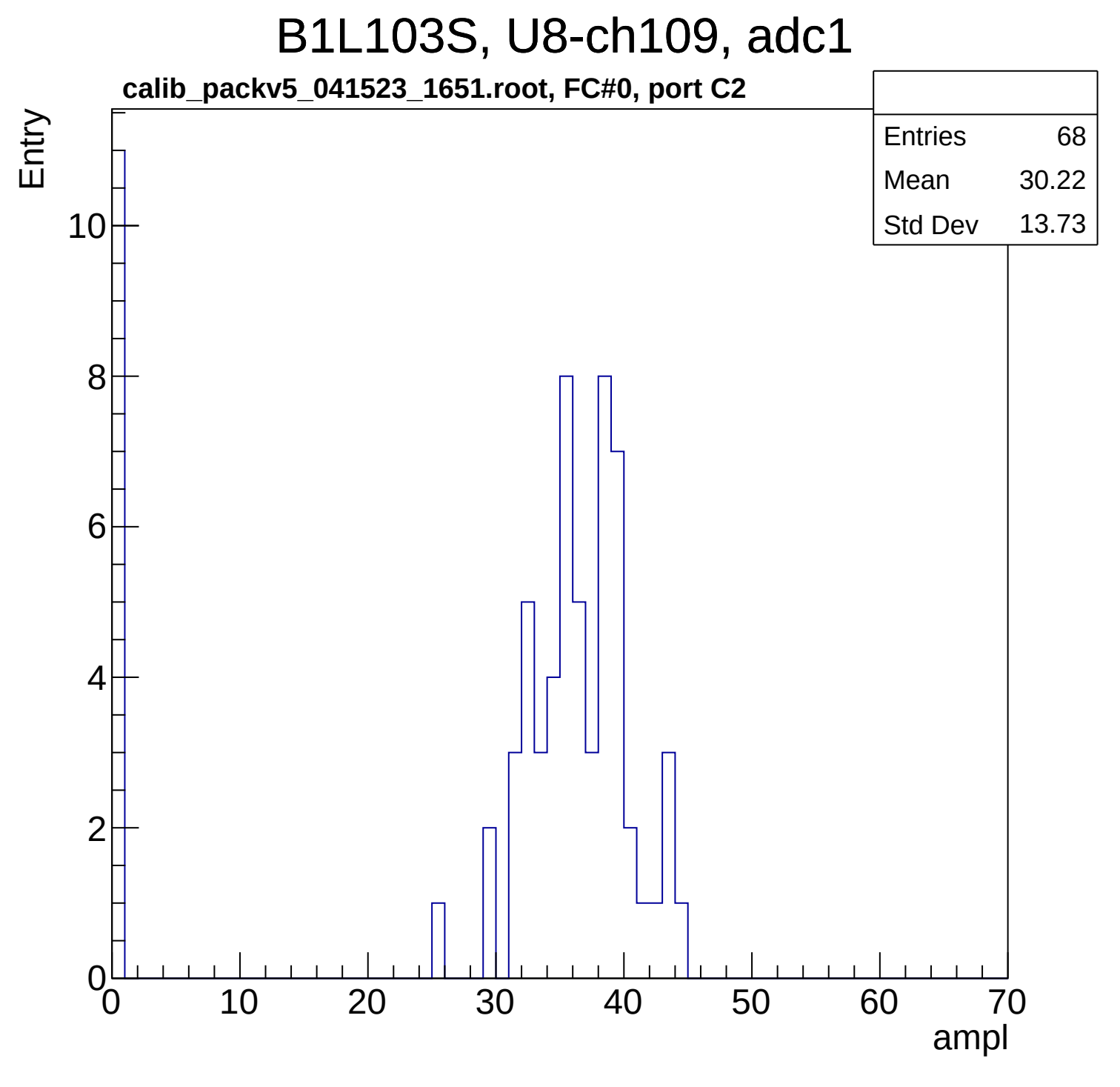
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

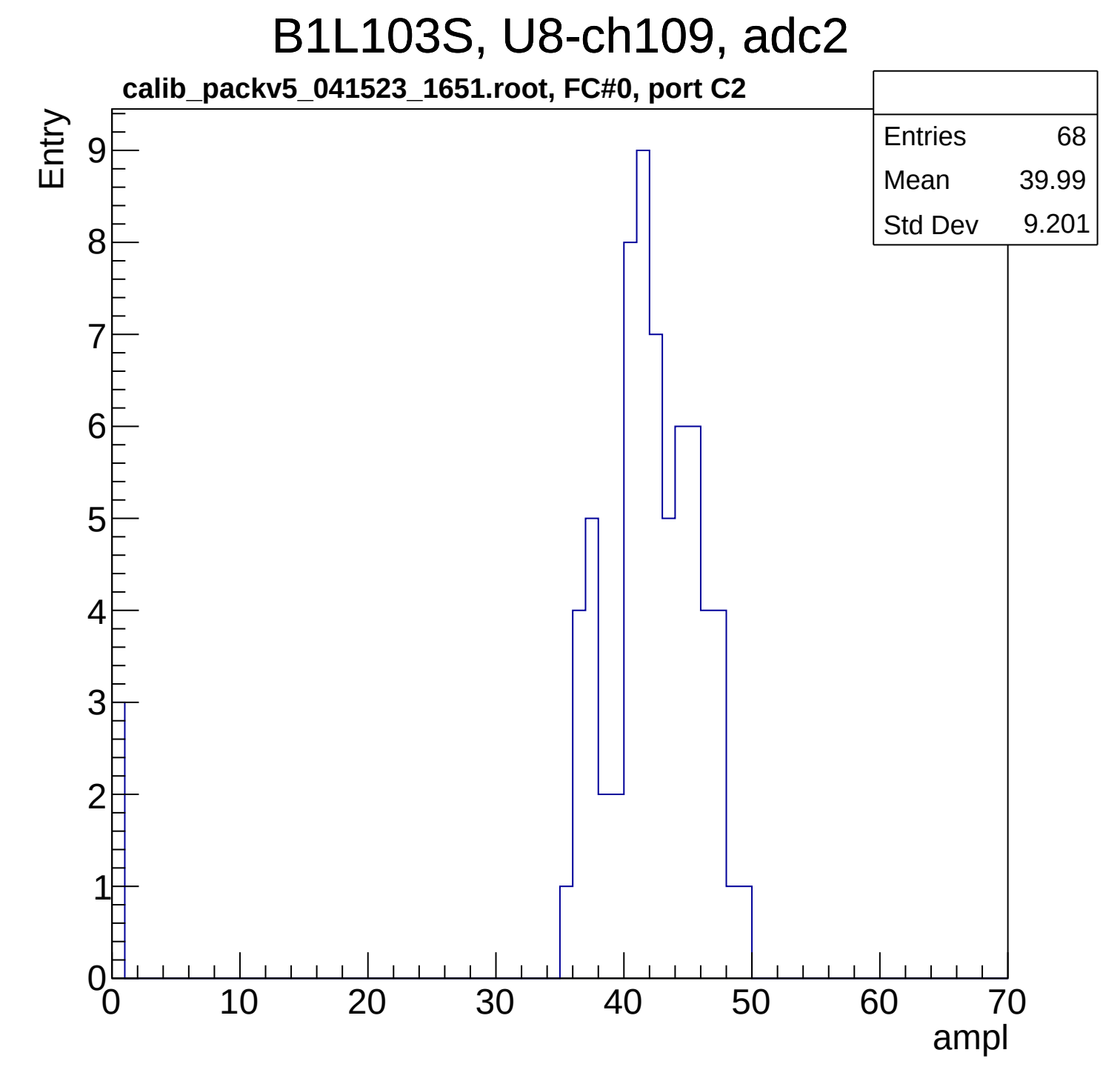

B1L103S, U8-ch108, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 57.98
Std Dev 8.529
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U8-ch108, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 61
Std Dev 1.751
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U8-ch108, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0.8947
Std Dev 3.796
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch109, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 102
Mean 24.34
Std Dev 11.08
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L103S, U8-ch109, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 30.22
Std Dev 13.73
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch109, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 39.99
Std Dev 9.201
Entry
ampl
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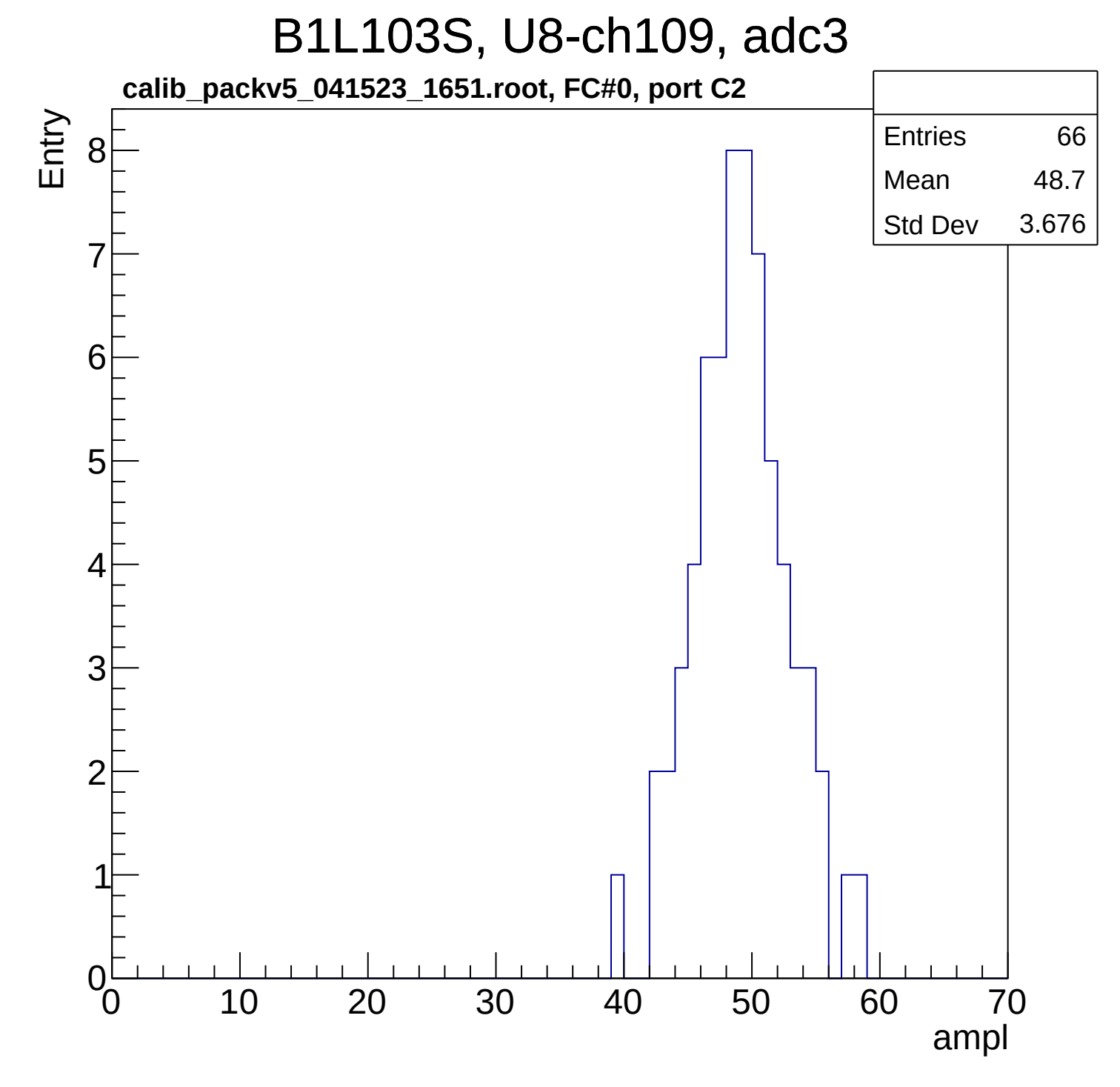
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U8-ch109, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 48.7
Std Dev 3.676
Entry
ampl
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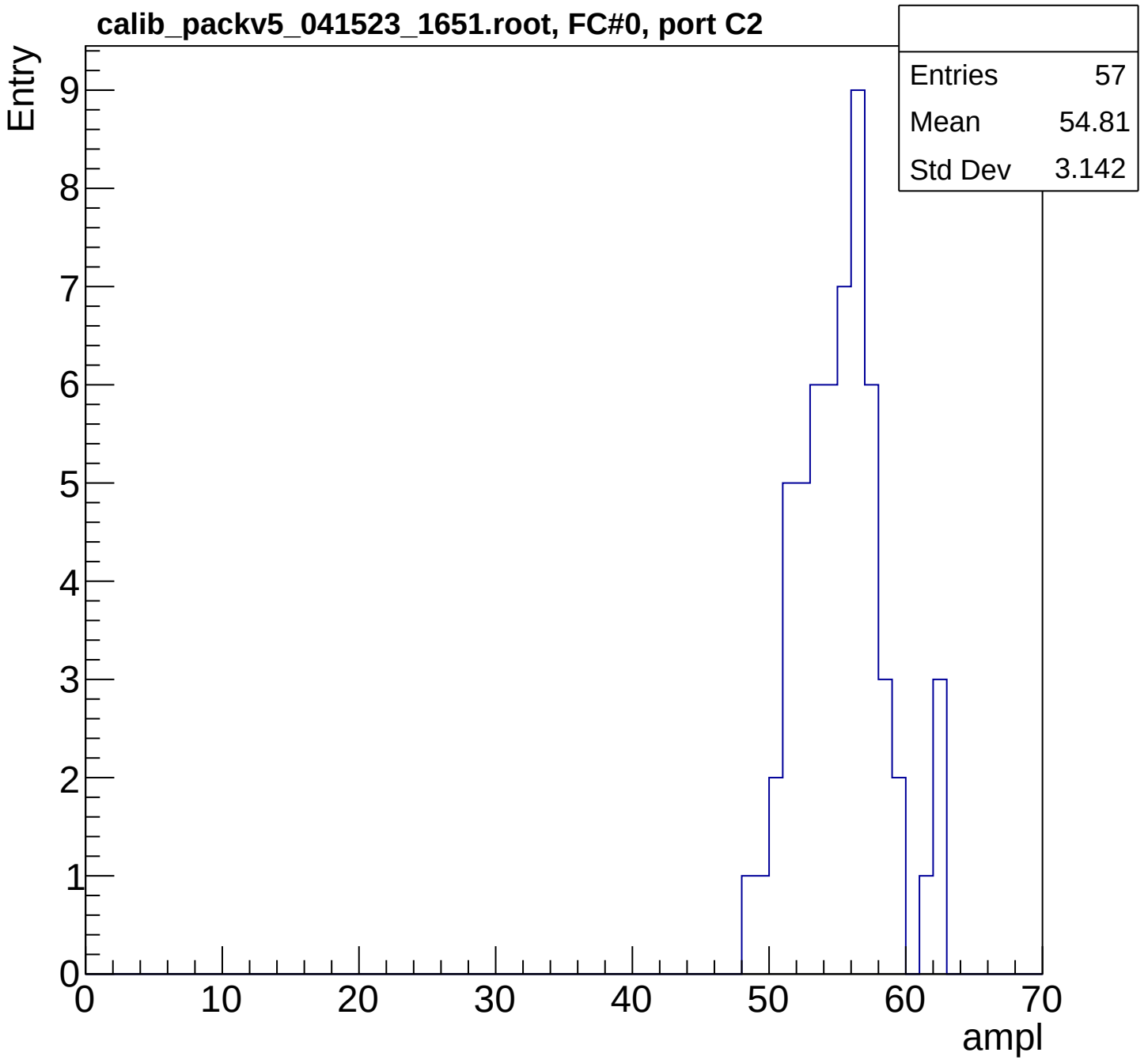
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch109, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 54.81
Std Dev 3.142
Entry
ampl
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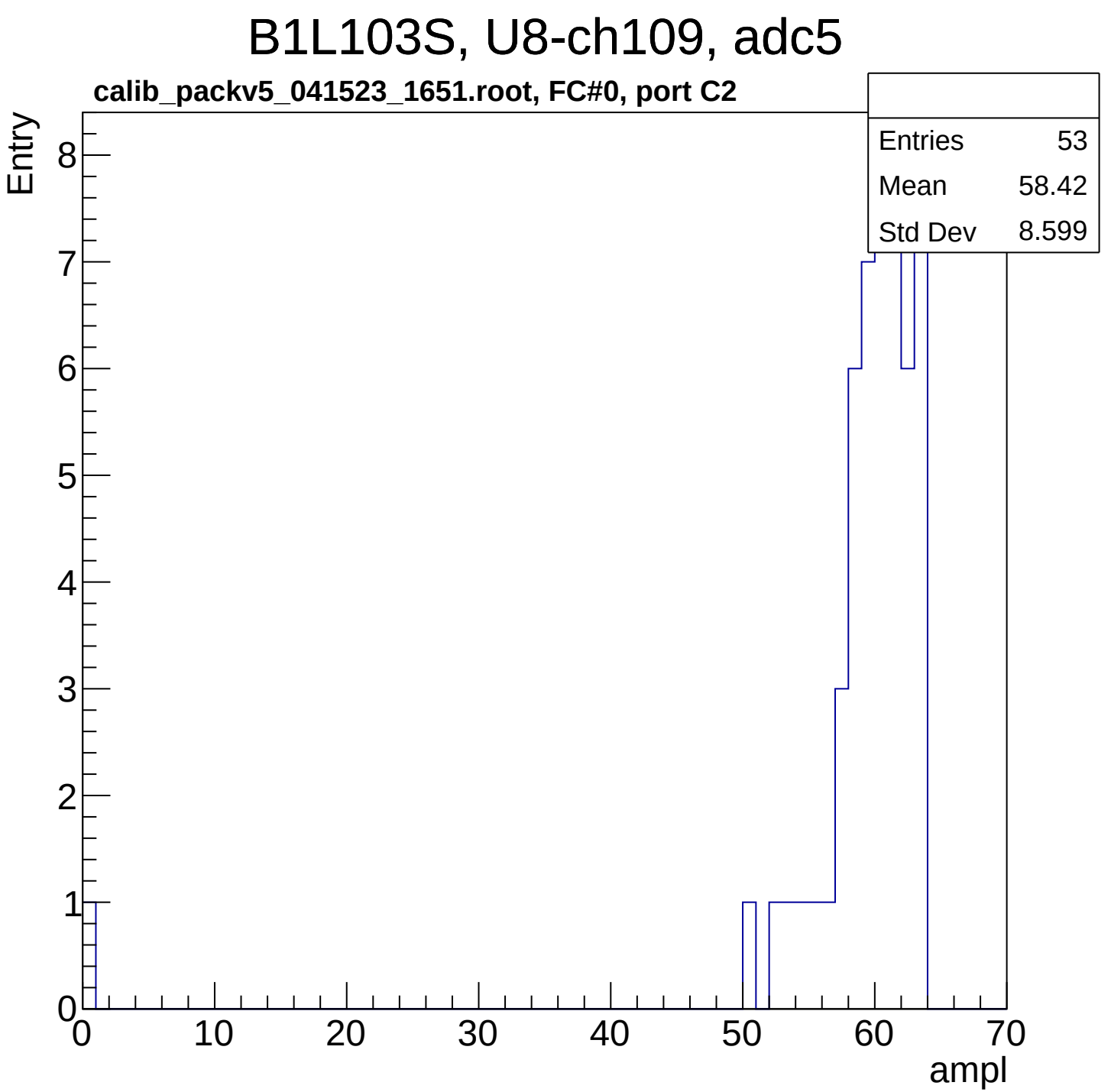
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U8-ch109, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 58.42
Std Dev 8.599
Entry
ampl
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2
3
4
5
6
7
8
0
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40
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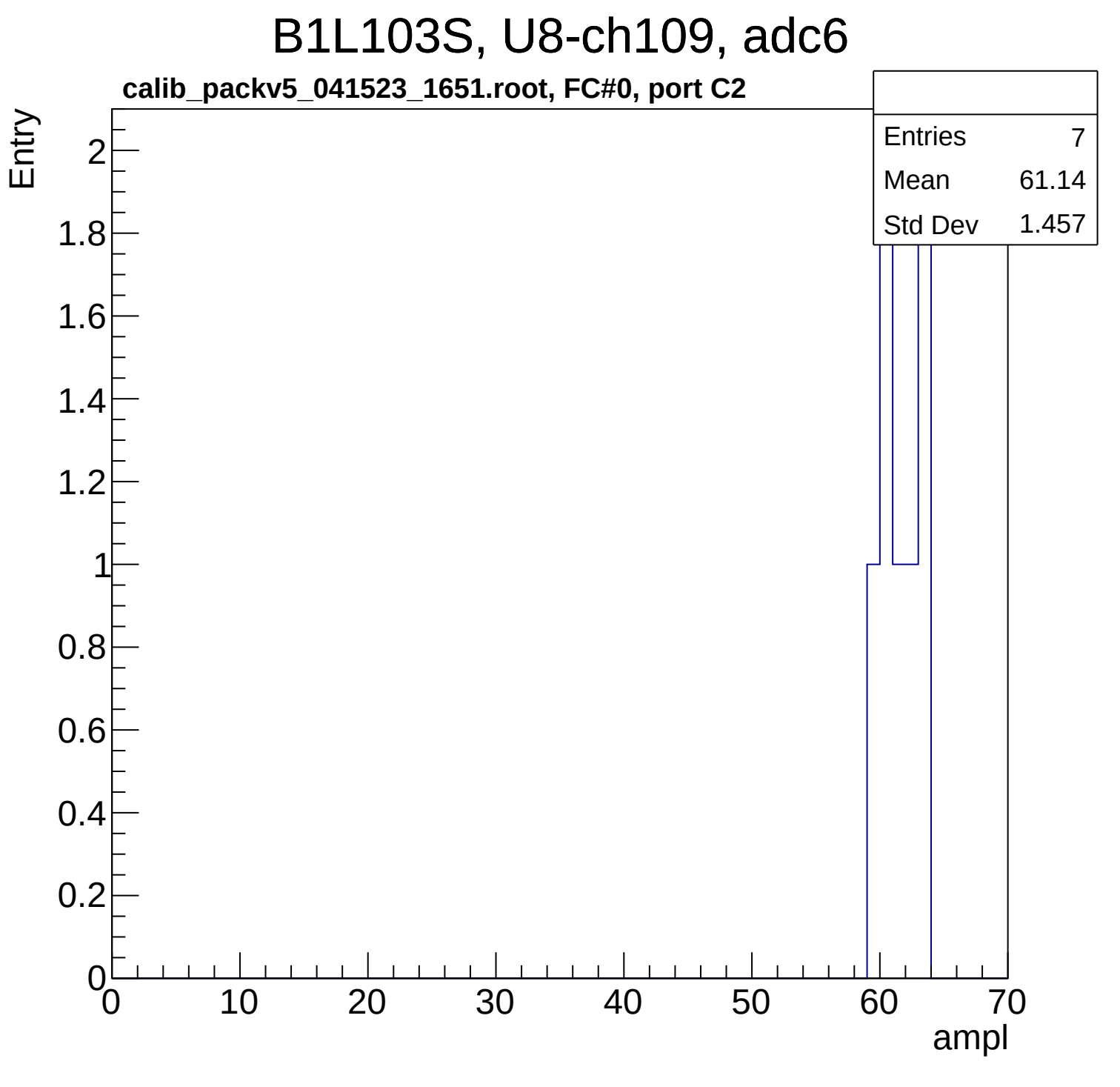
60
70


B1L103S, U8-ch109, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 61.14
Std Dev 1.457
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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30
40
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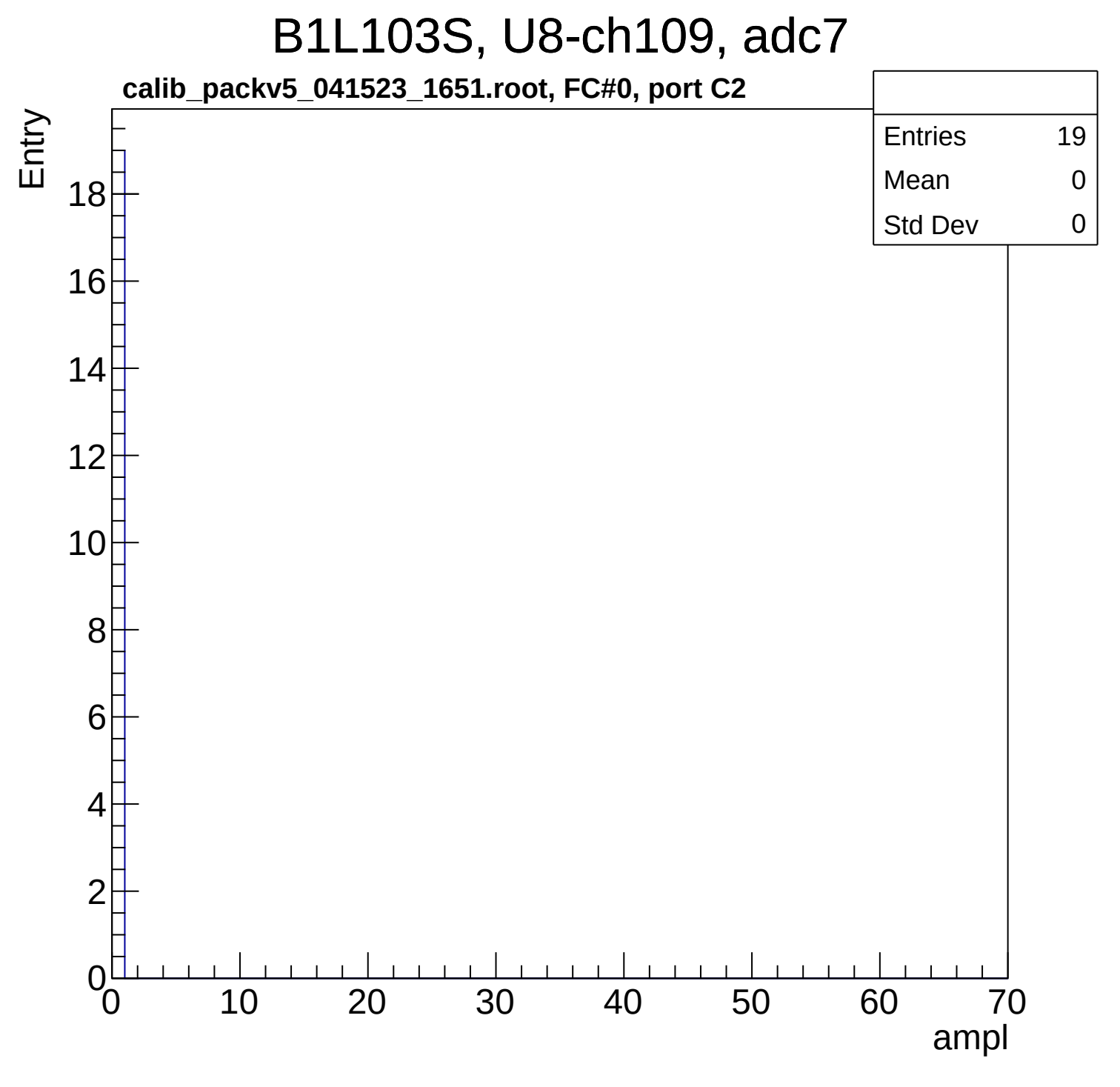
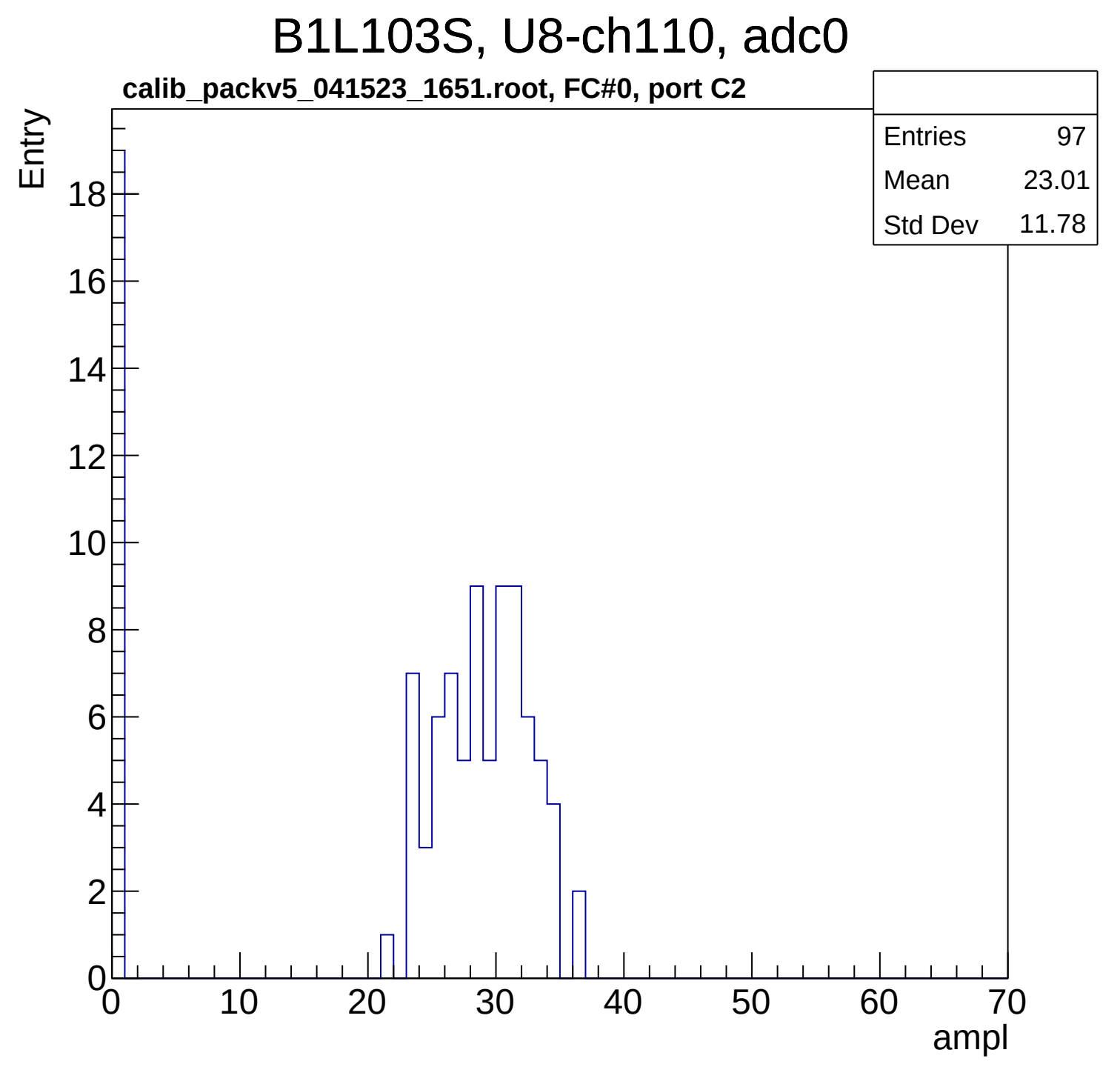
60
70


B1L103S, U8-ch109, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch110, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 23.01
Std Dev 11.78
Entry
ampl
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4
6
8
10
12
14
16
18
0
10
20
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40
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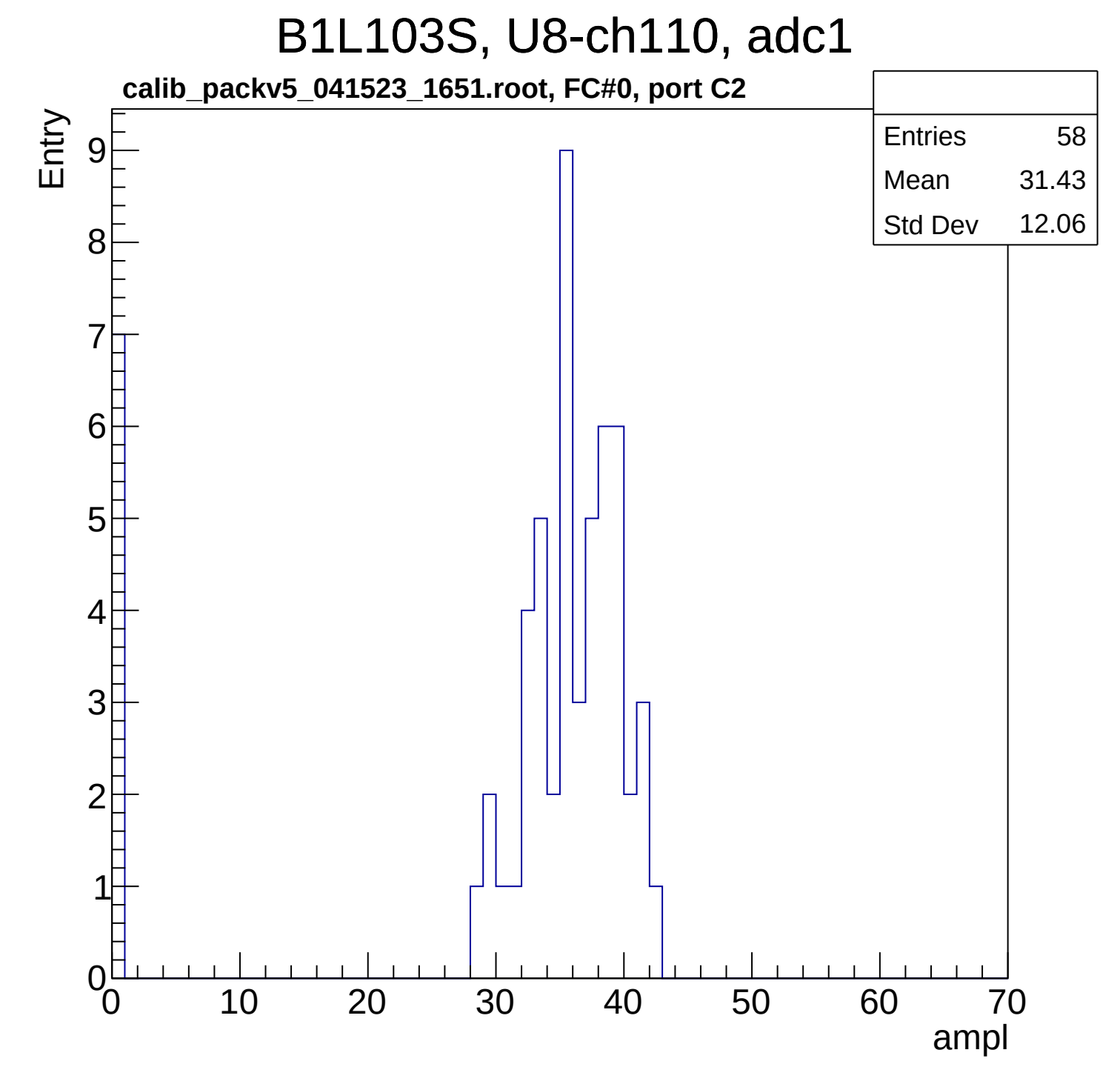
60
70


B1L103S, U8-ch110, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 31.43
Std Dev 12.06
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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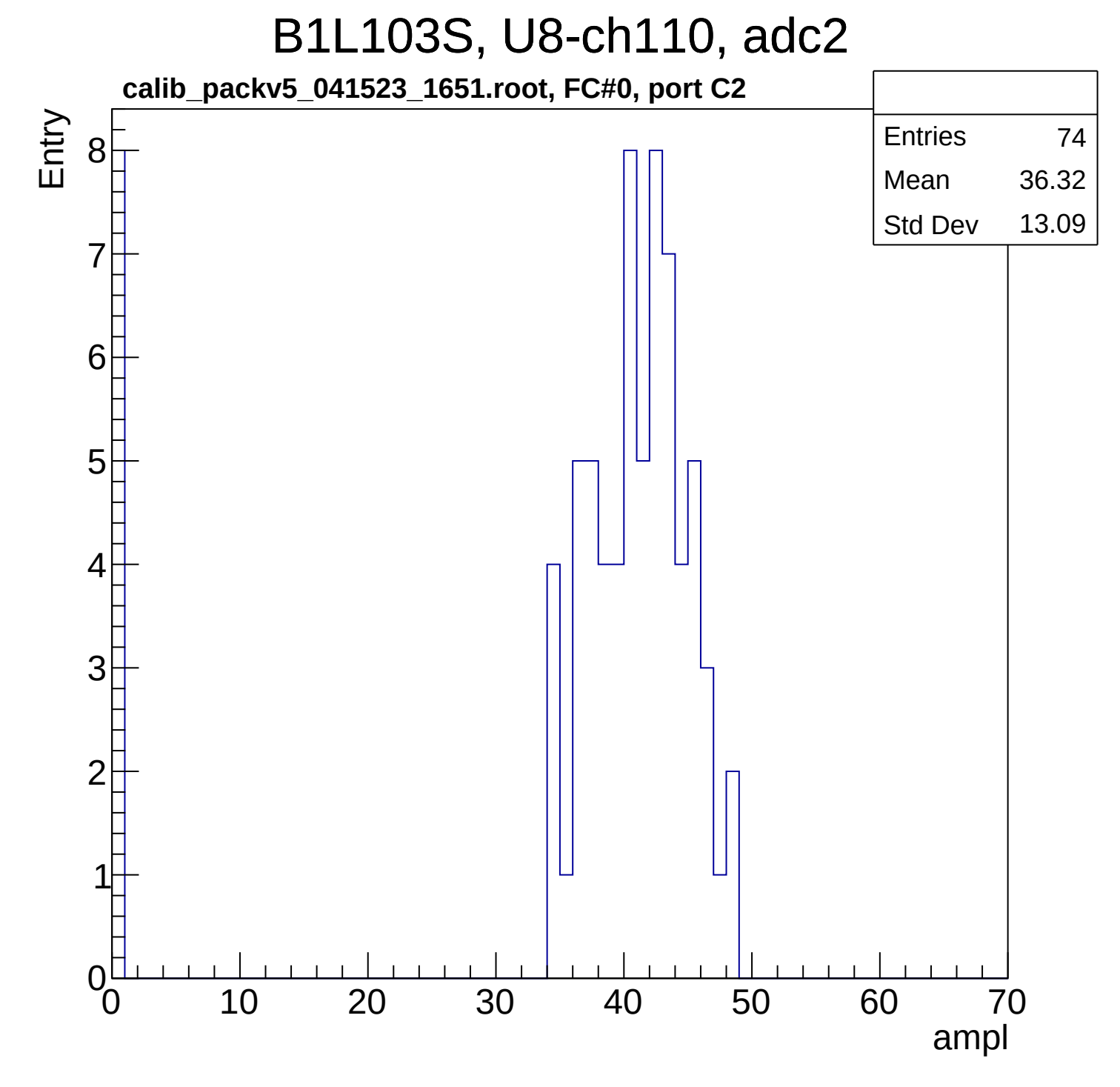
60
70


B1L103S, U8-ch110, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 36.32
Std Dev 13.09
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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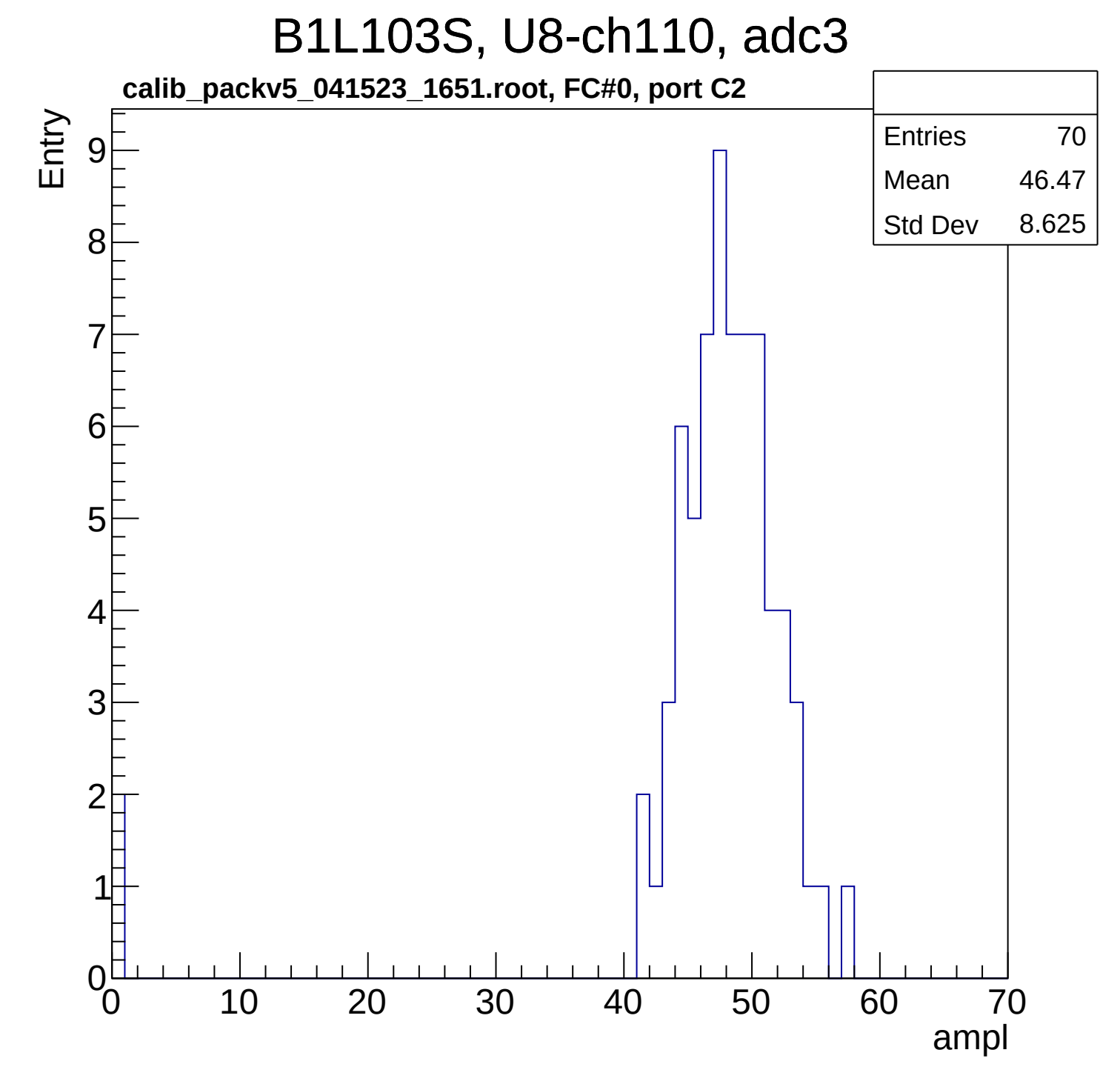
40
50
60
70


B1L103S, U8-ch110, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 46.47
Std Dev 8.625
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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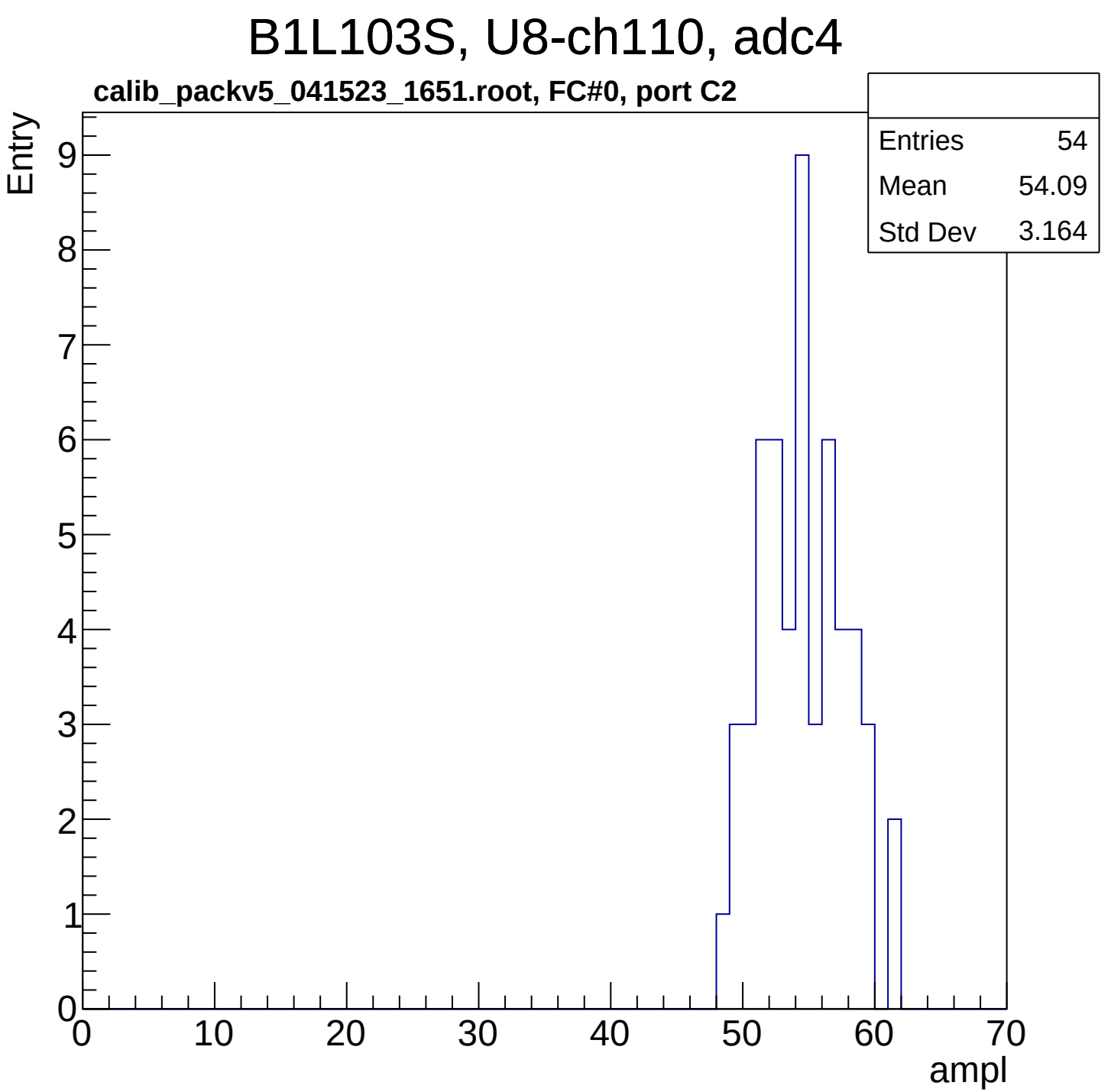
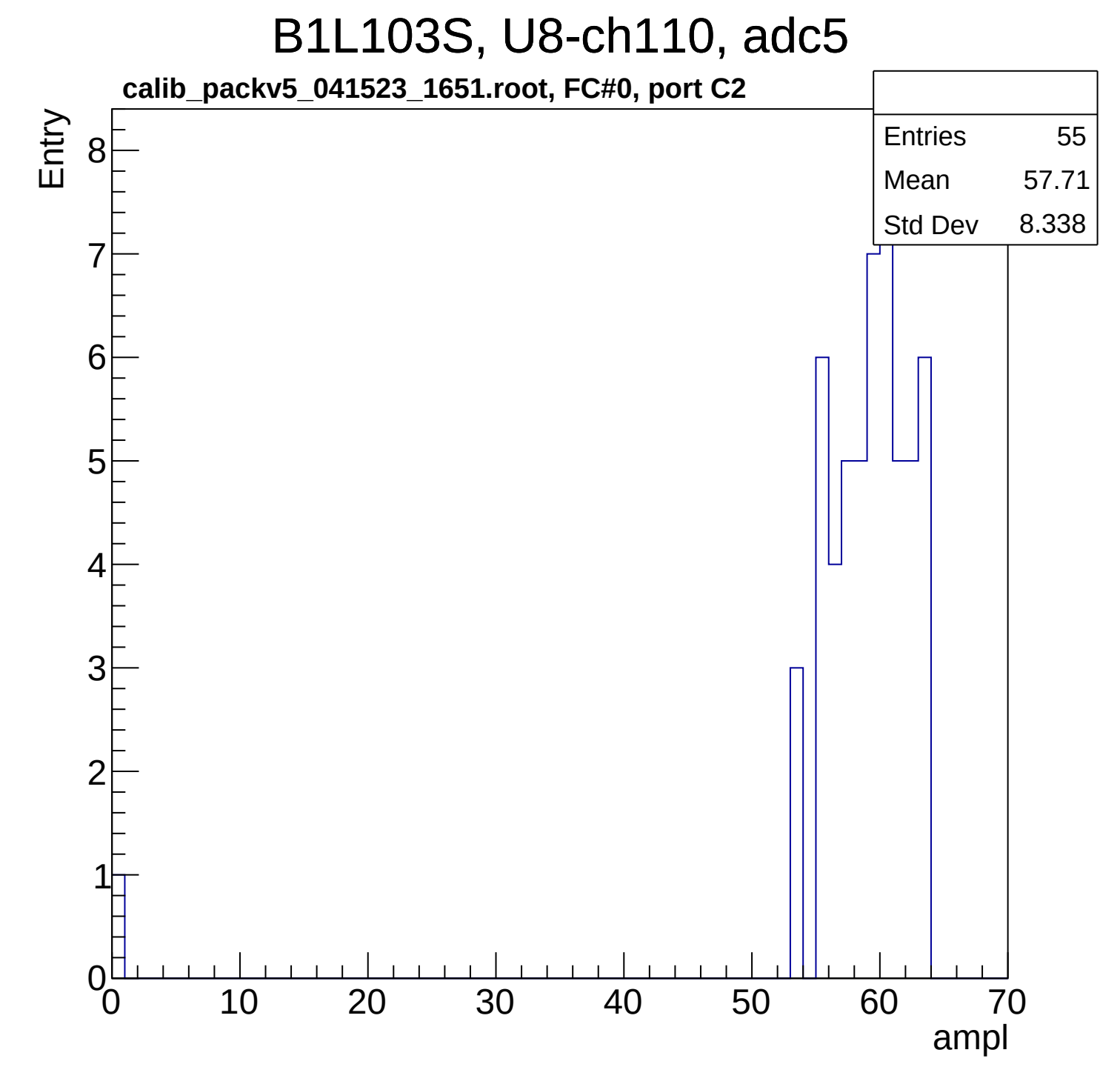
60
70


B1L103S, U8-ch110, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 54.09
Std Dev 3.164
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U8-ch110, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 57.71
Std Dev 8.338
Entry
ampl
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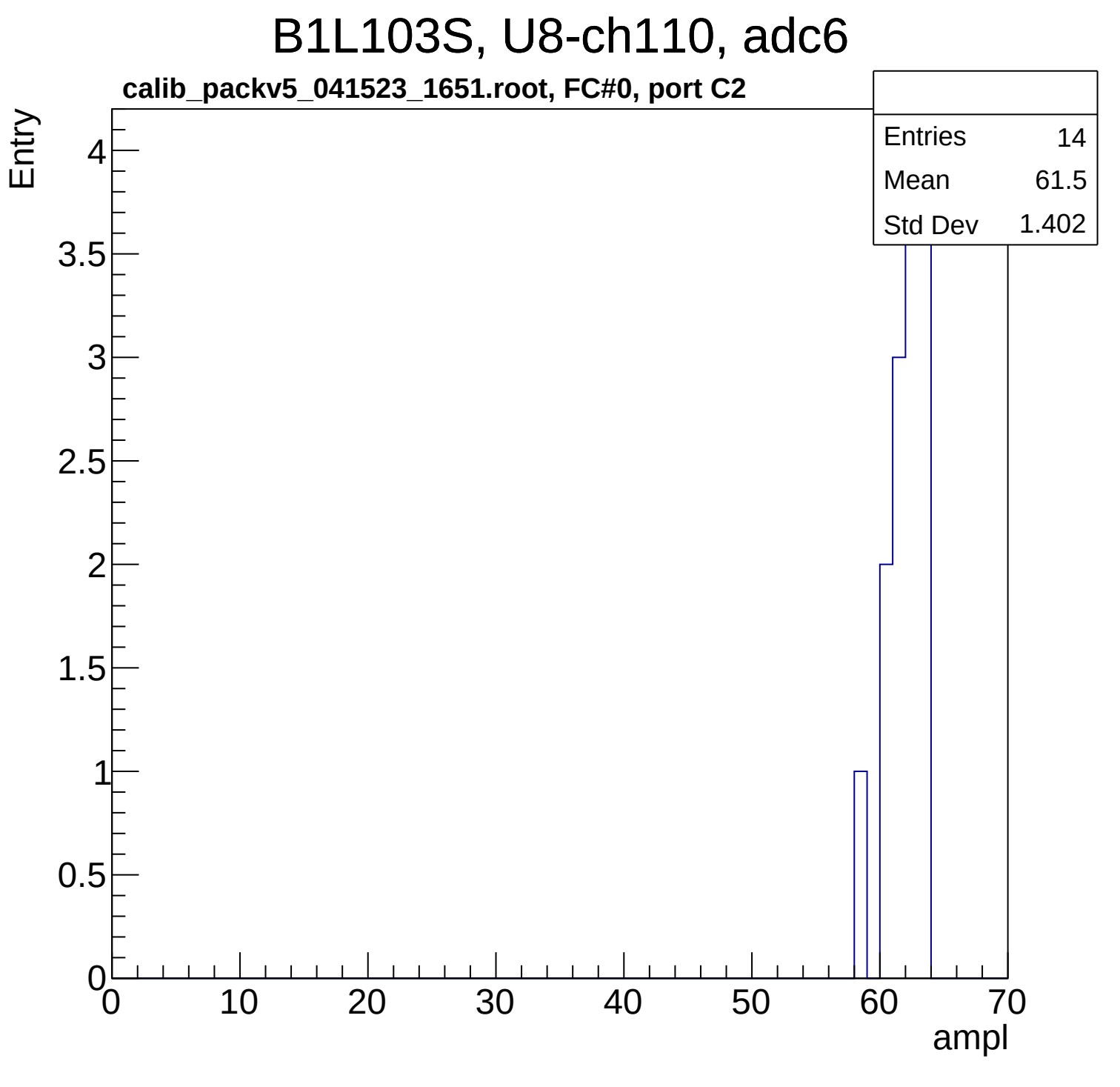
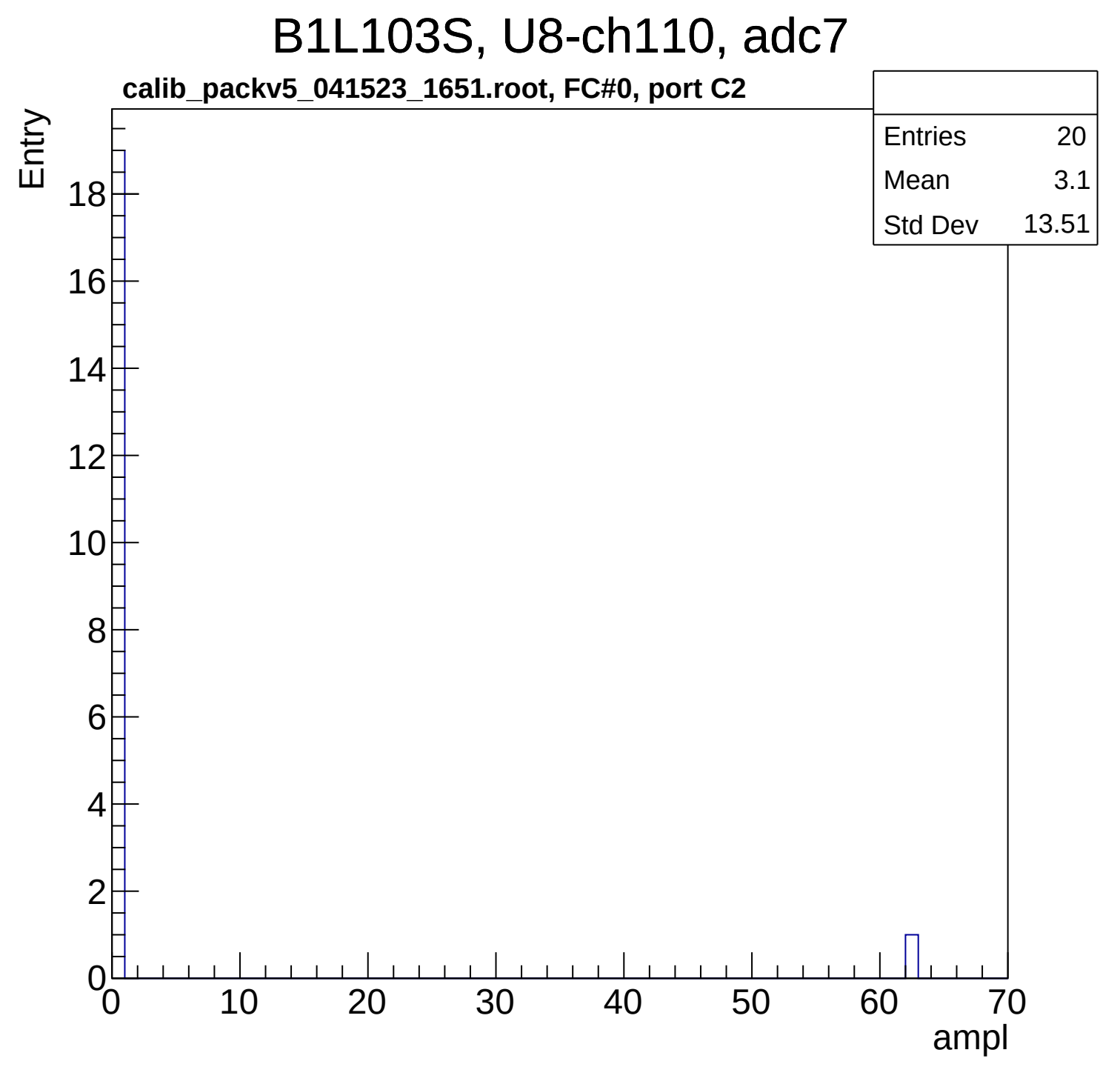
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch110, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 61.5
Std Dev 1.402
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U8-ch110, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
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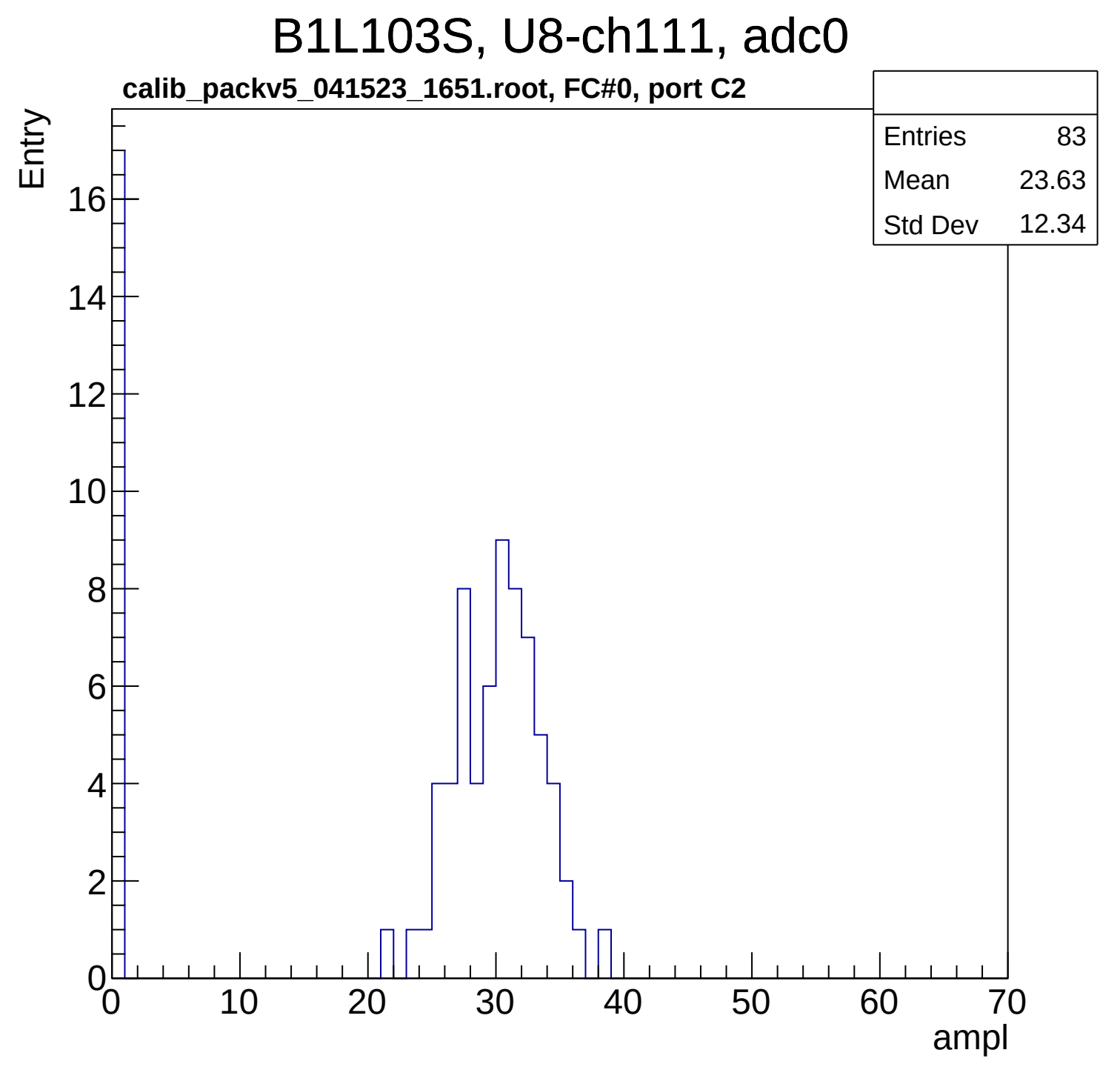
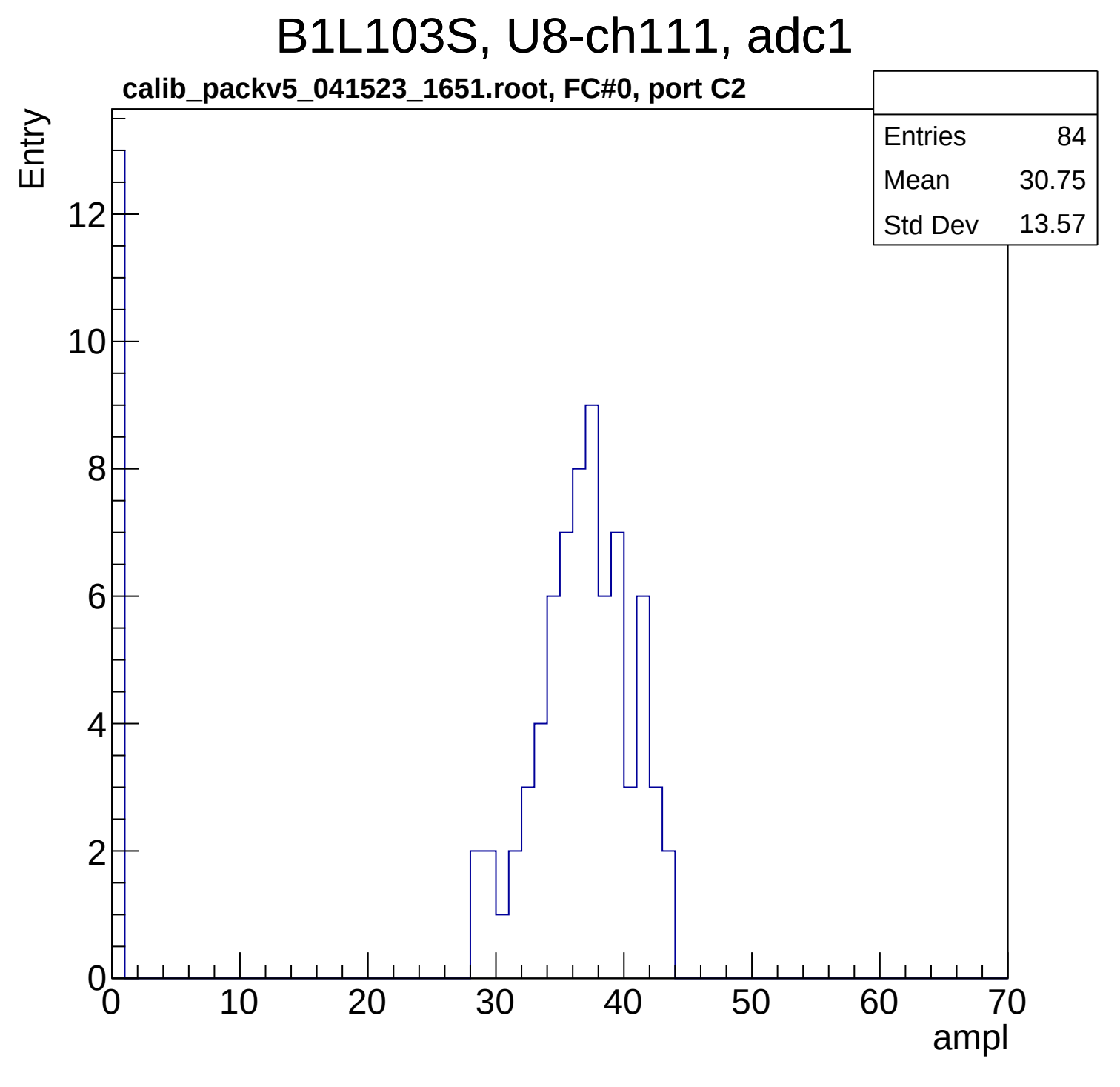
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch111, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 23.63
Std Dev 12.34
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch111, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 30.75
Std Dev 13.57
Entry
0
2
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8
10
12
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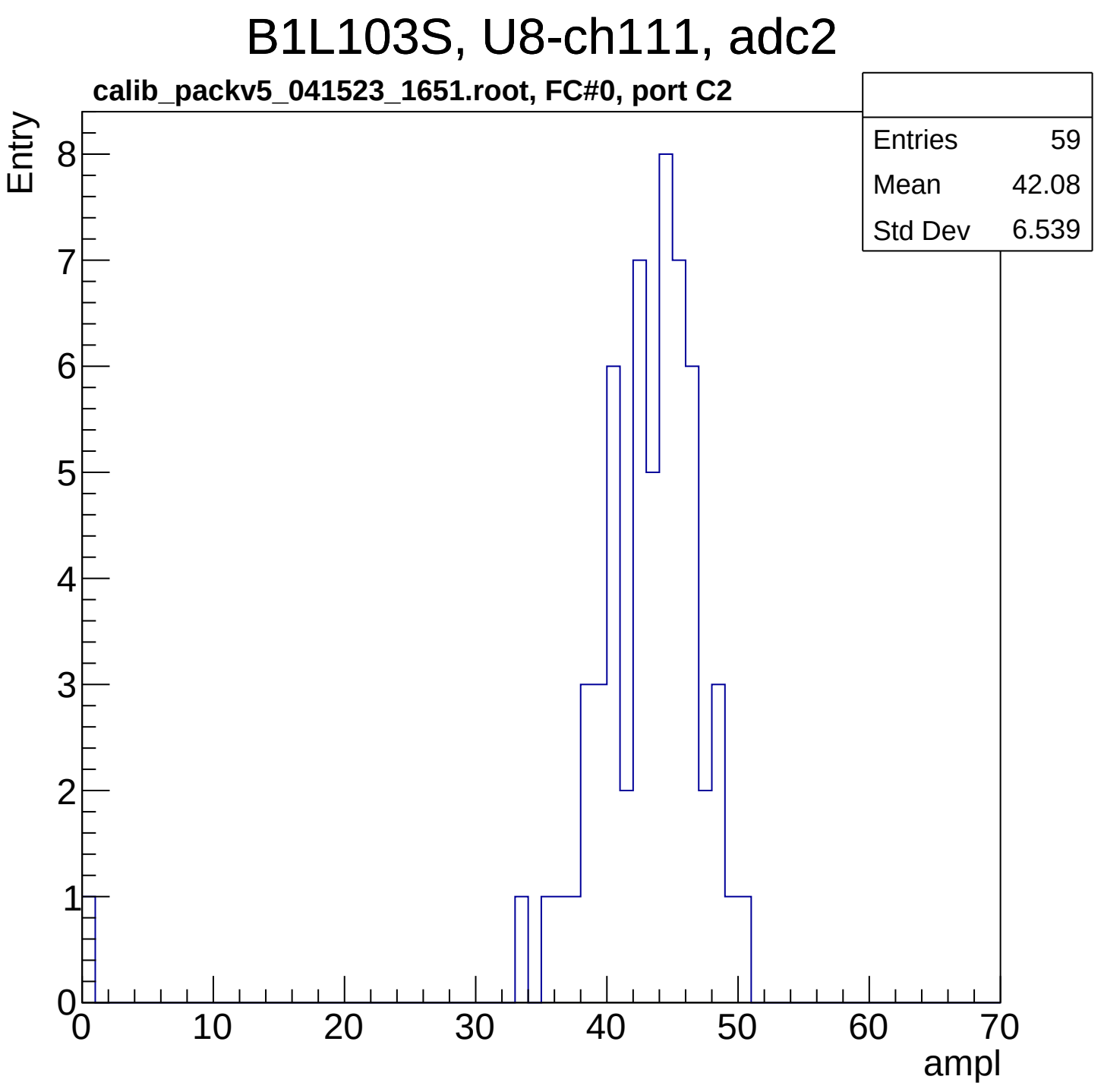
ampl


B1L103S, U8-ch111, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 42.08
Std Dev 6.539
Entry
ampl
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3
4
5
6
7
8
0
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40
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60
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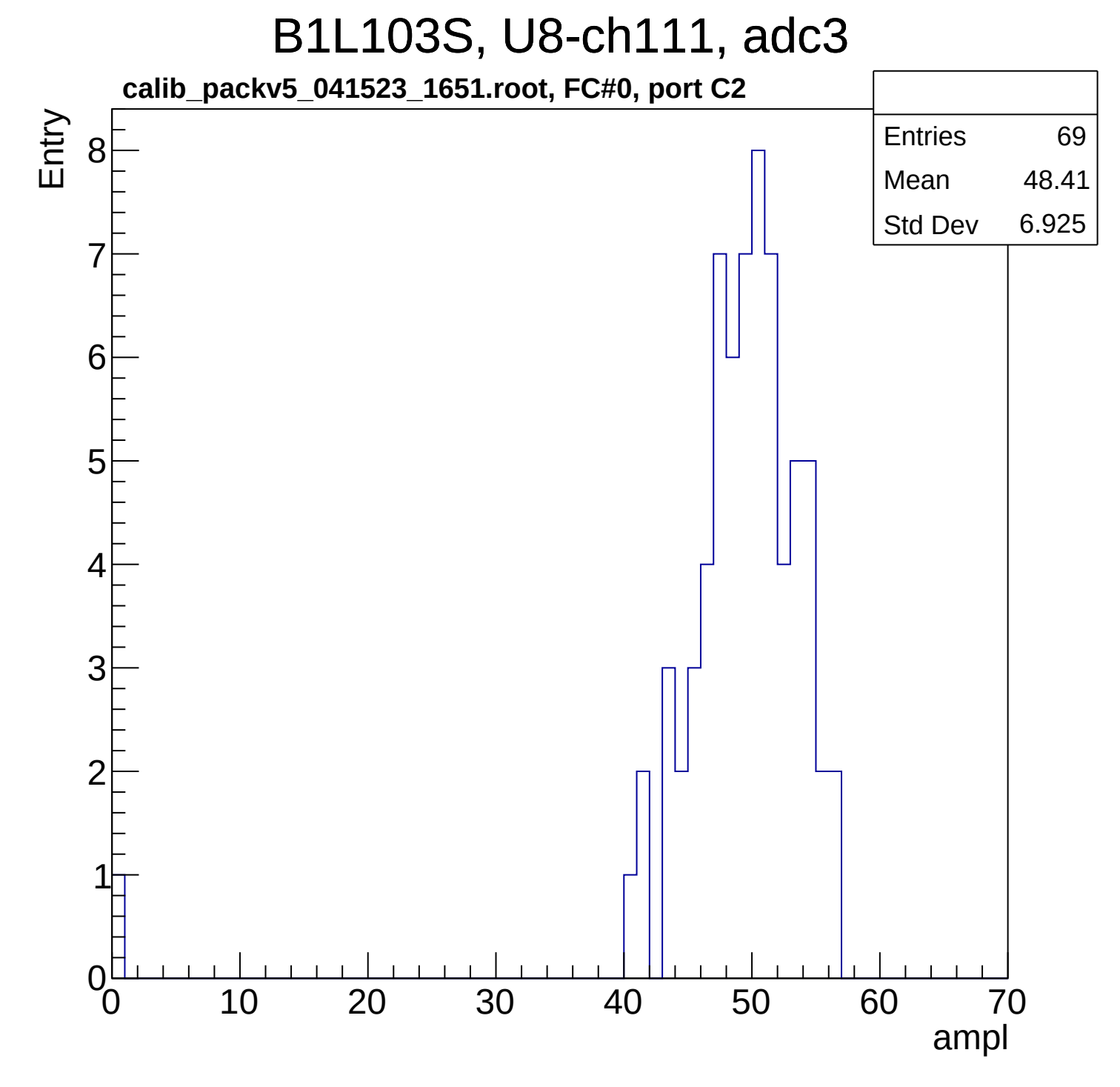
B1L103S, U8-ch111, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 48.41
Std Dev 6.925
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
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40
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60
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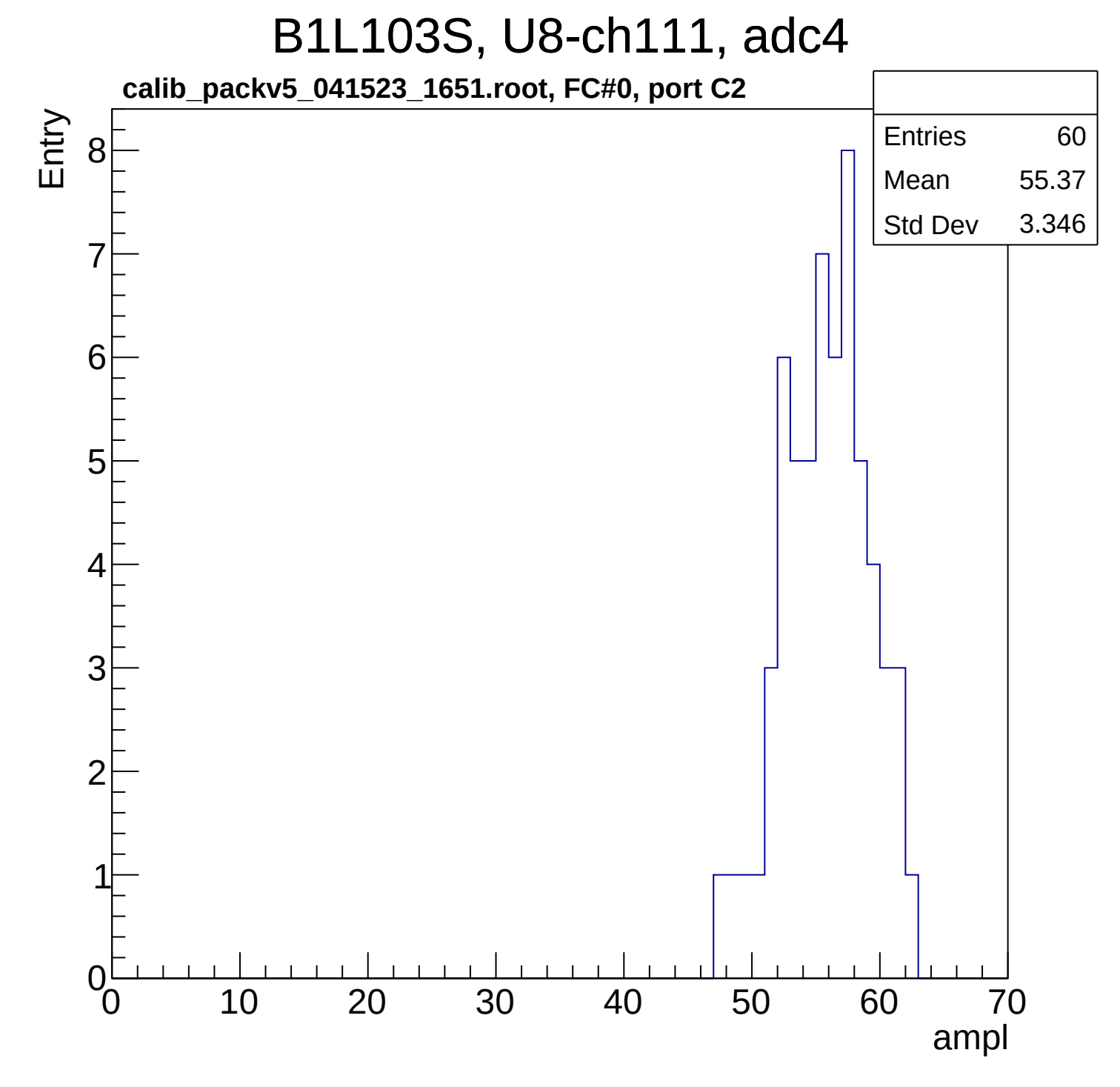
B1L103S, U8-ch111, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 55.37
Std Dev 3.346
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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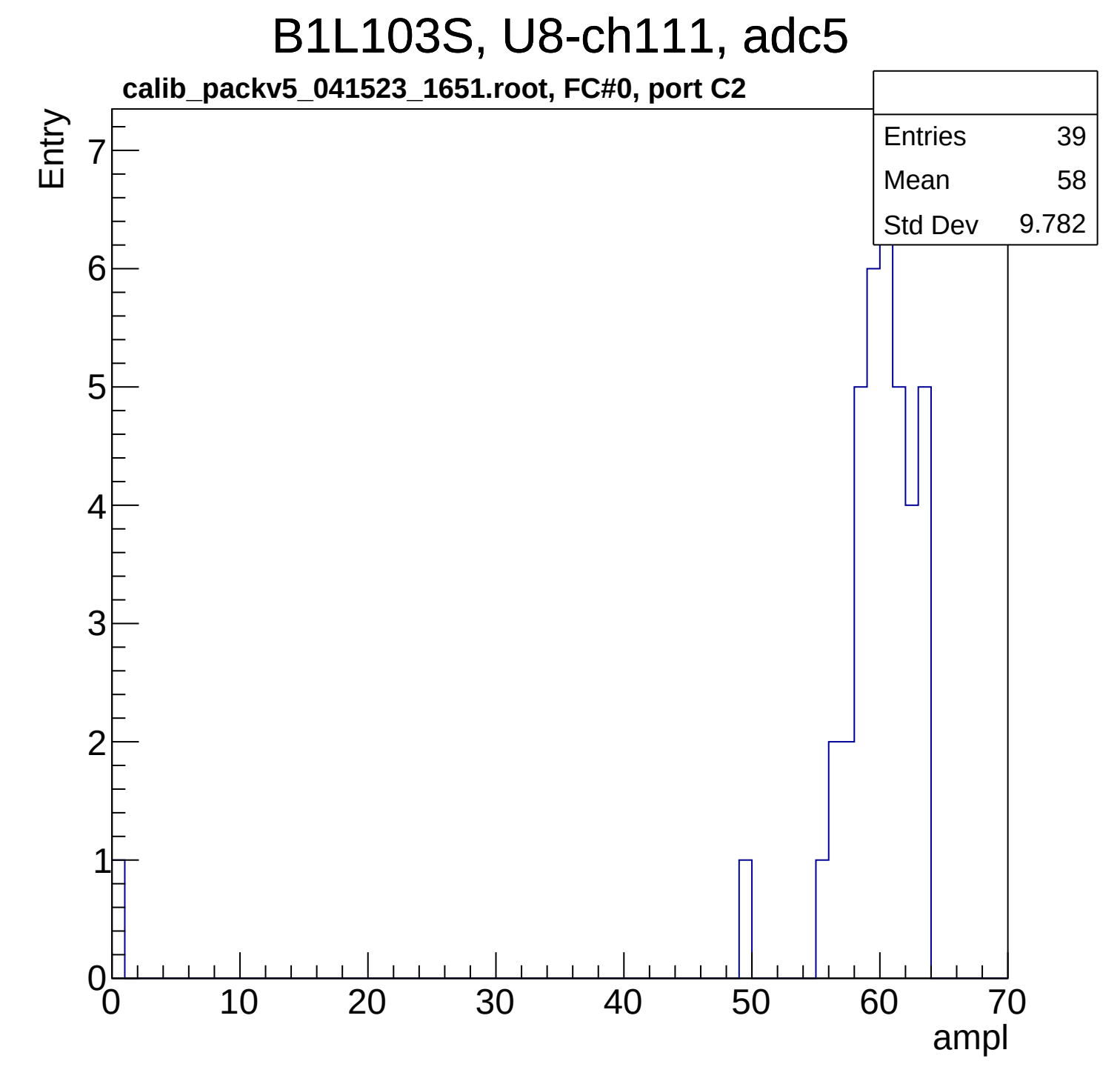
B1L103S, U8-ch111, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 58
Std Dev 9.782
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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40
50
60
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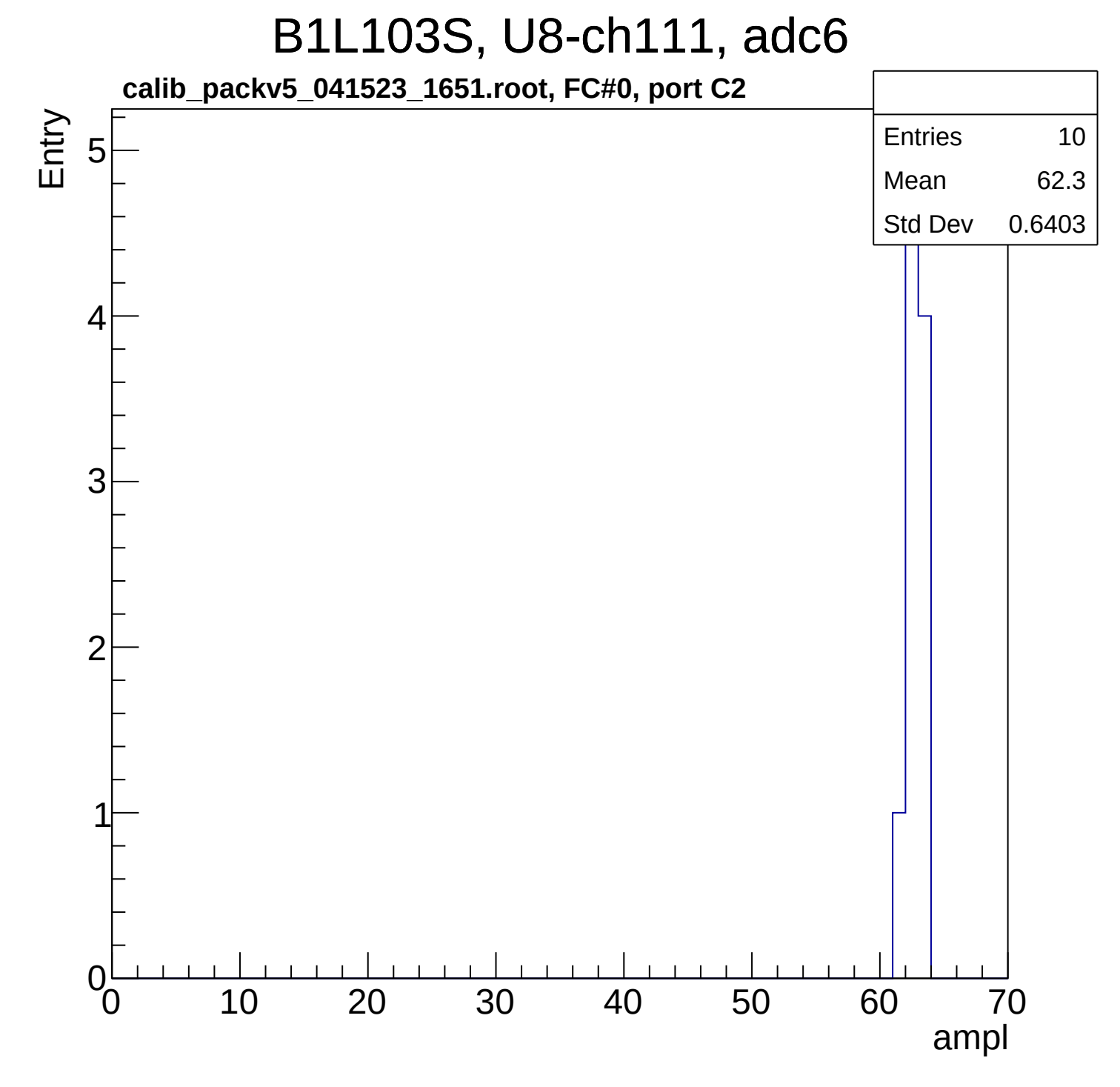
B1L103S, U8-ch111, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 62.3
Std Dev 0.6403
Entry
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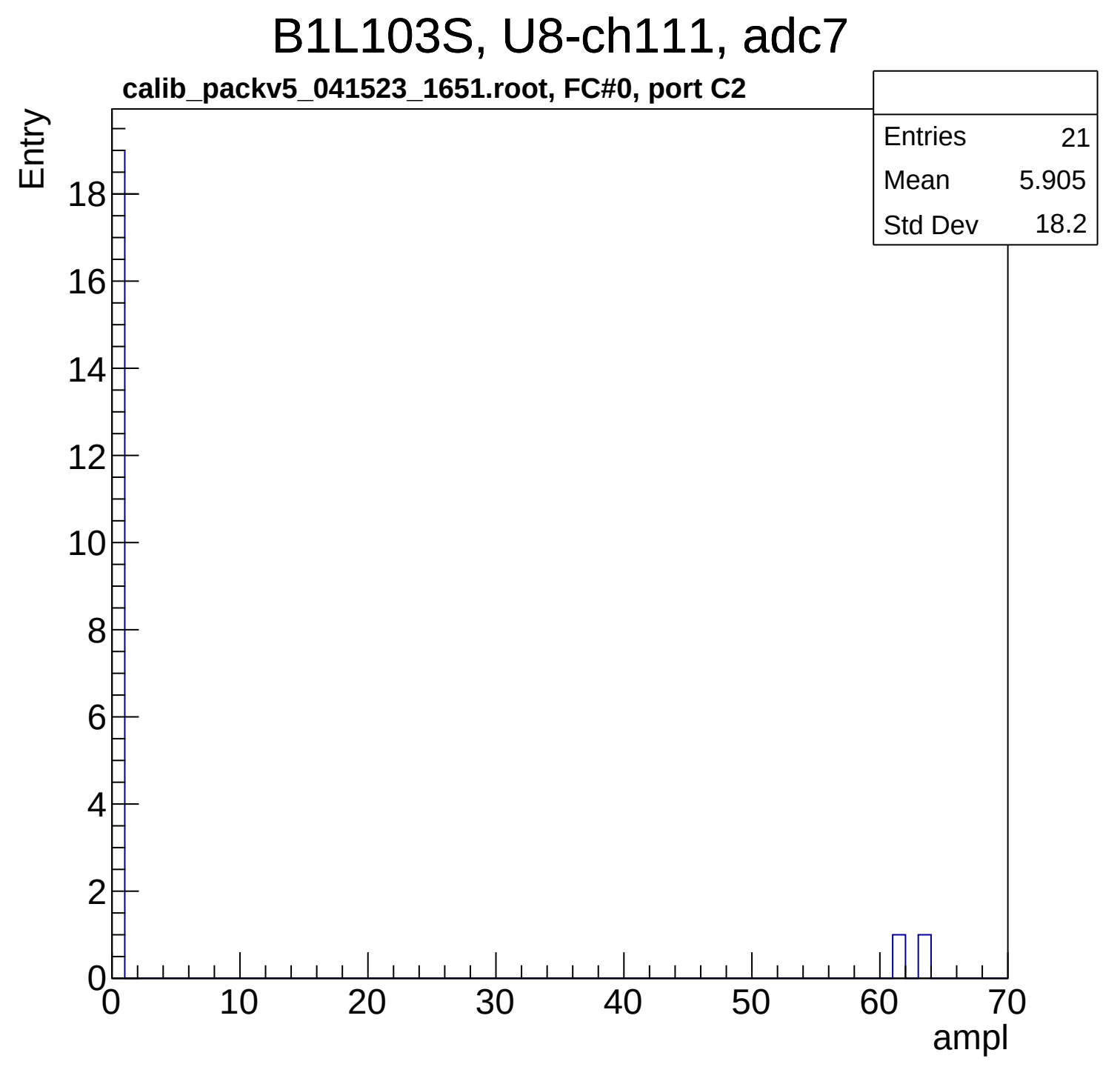
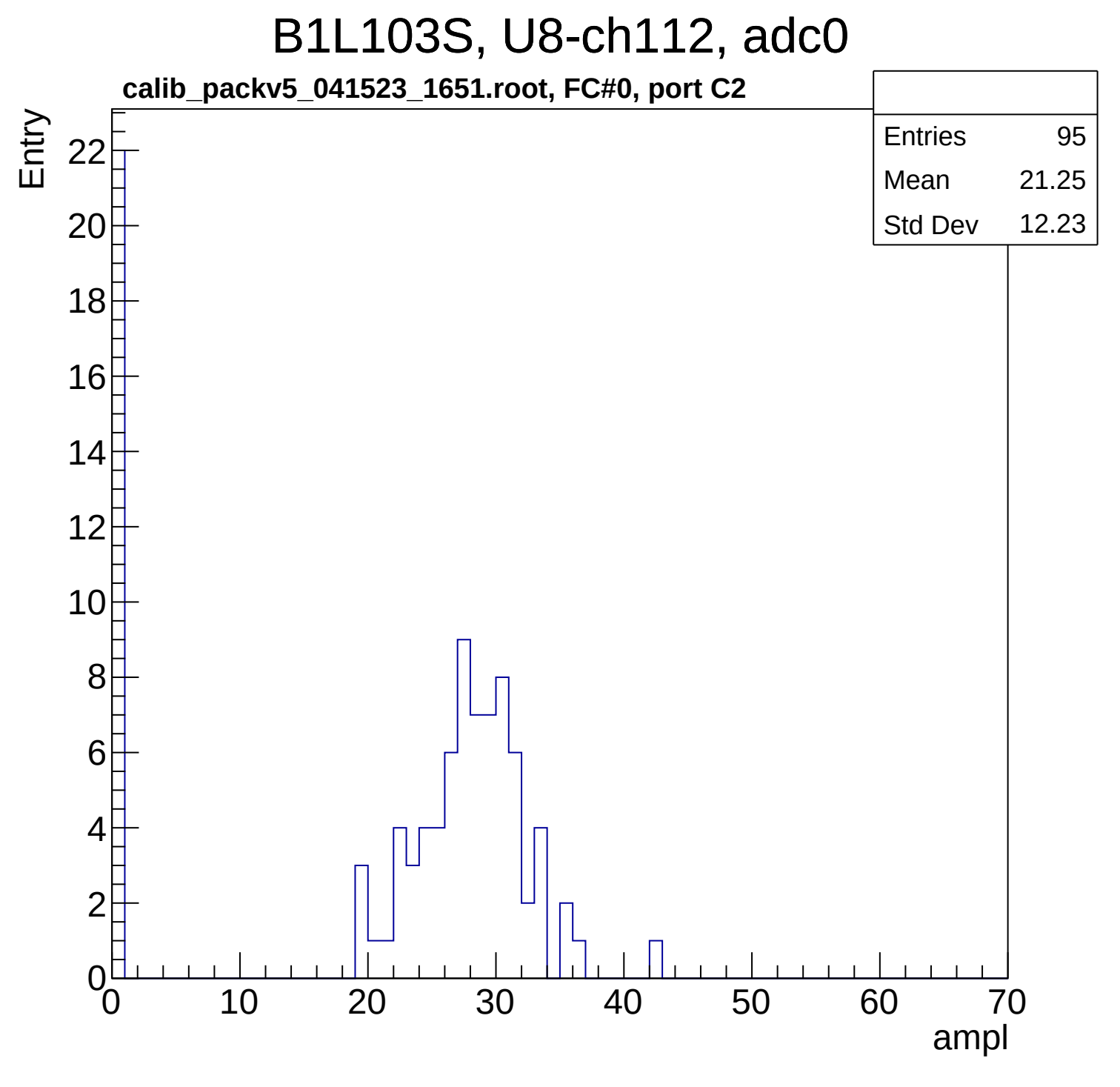
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch111, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.905
Std Dev 18.2
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch112, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 21.25
Std Dev 12.23
Entry
ampl
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2
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8
10
12
14
16
18
20
22
0
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60
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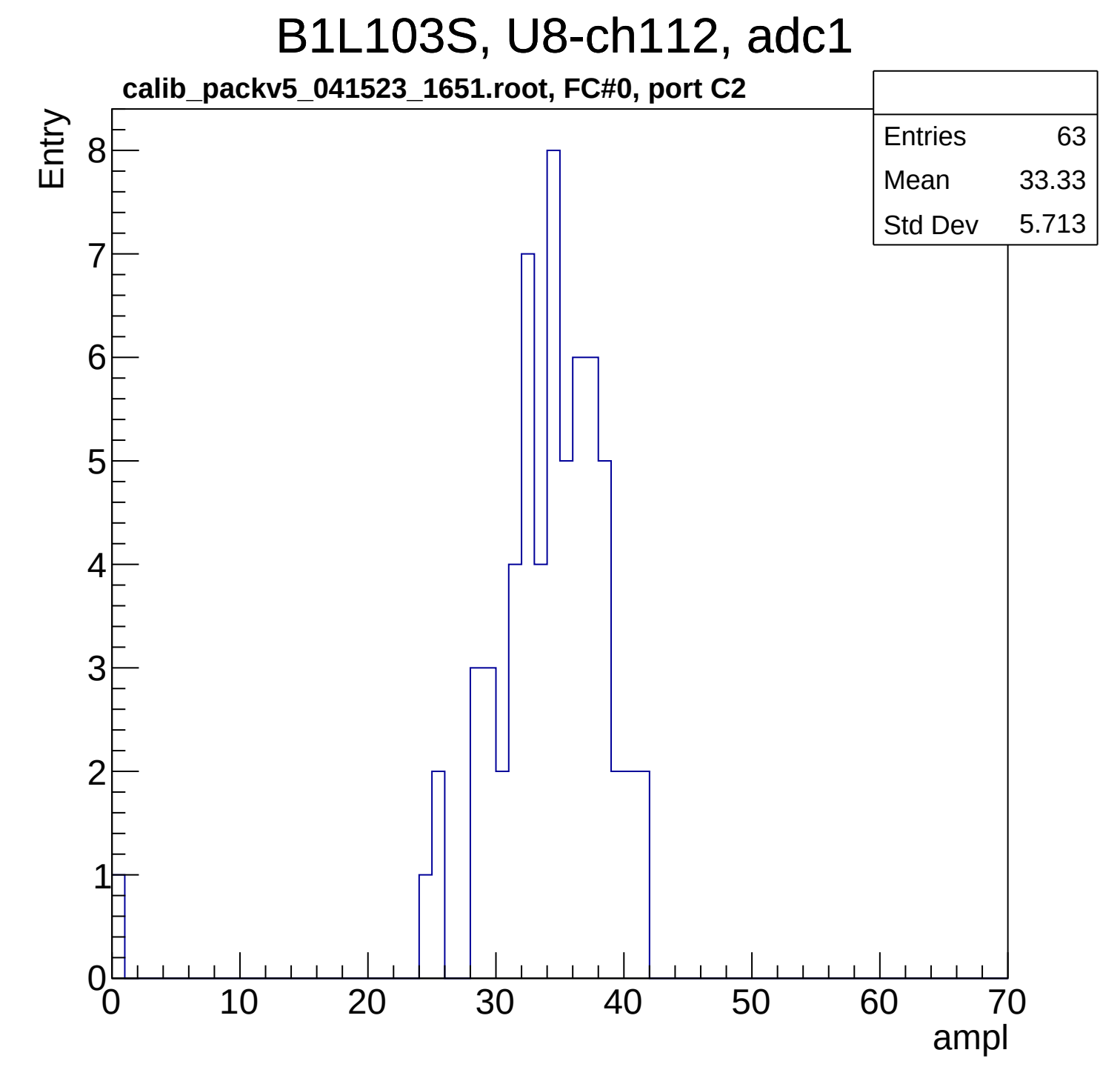
B1L103S, U8-ch112, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 33.33
Std Dev 5.713
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
50
60
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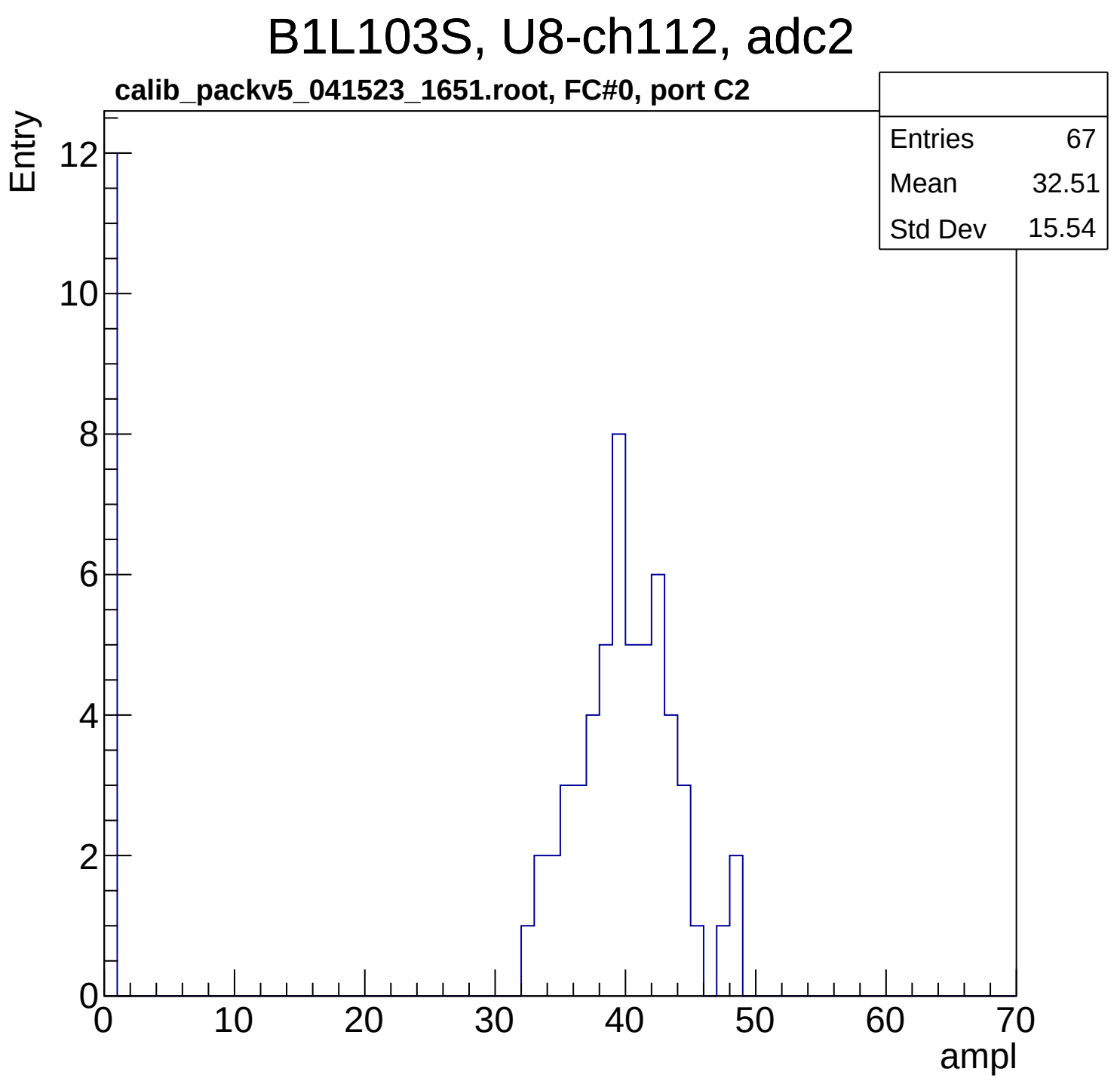
B1L103S, U8-ch112, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 32.51
Std Dev 15.54
Entry
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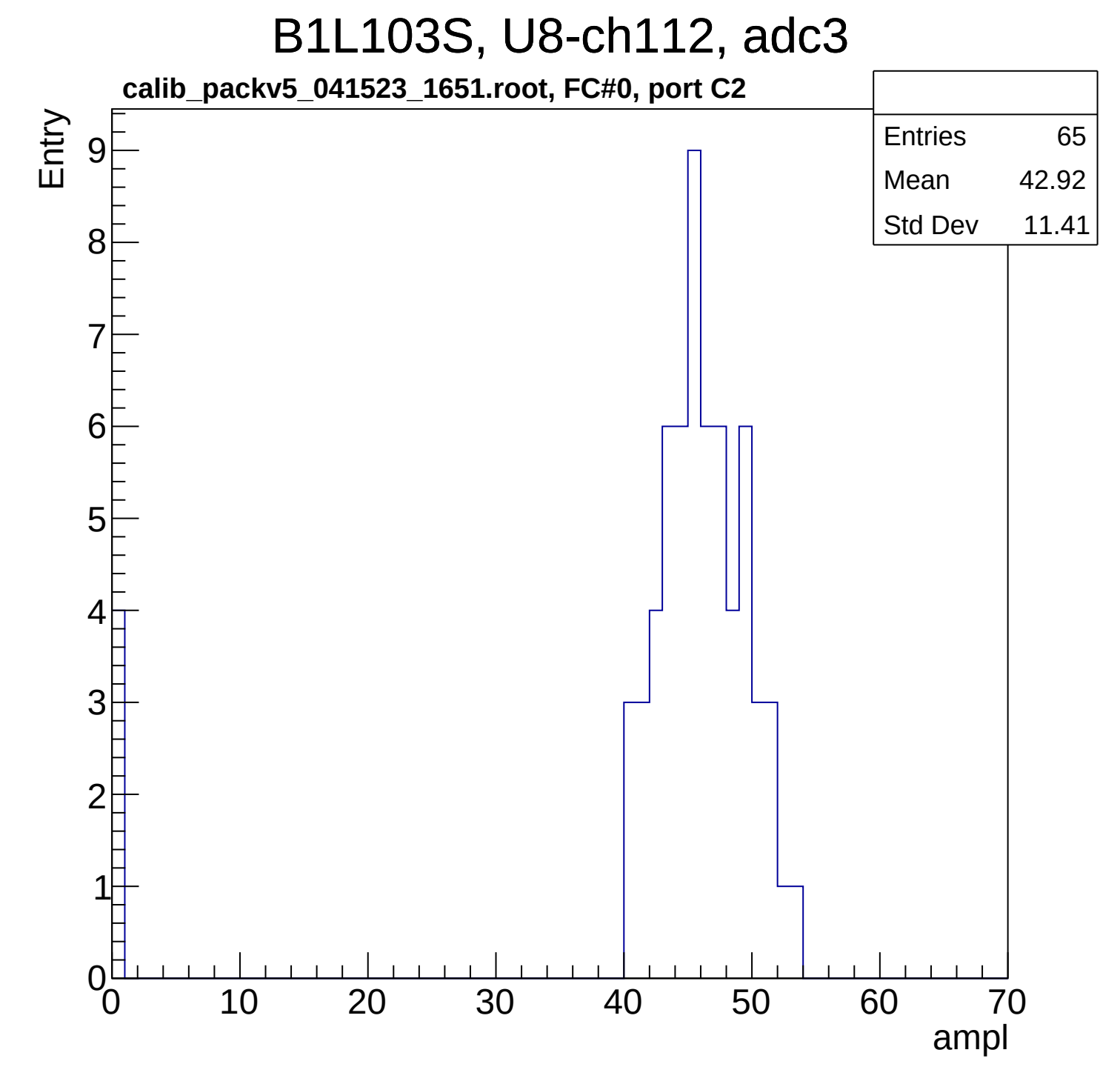
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch112, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 42.92
Std Dev 11.41
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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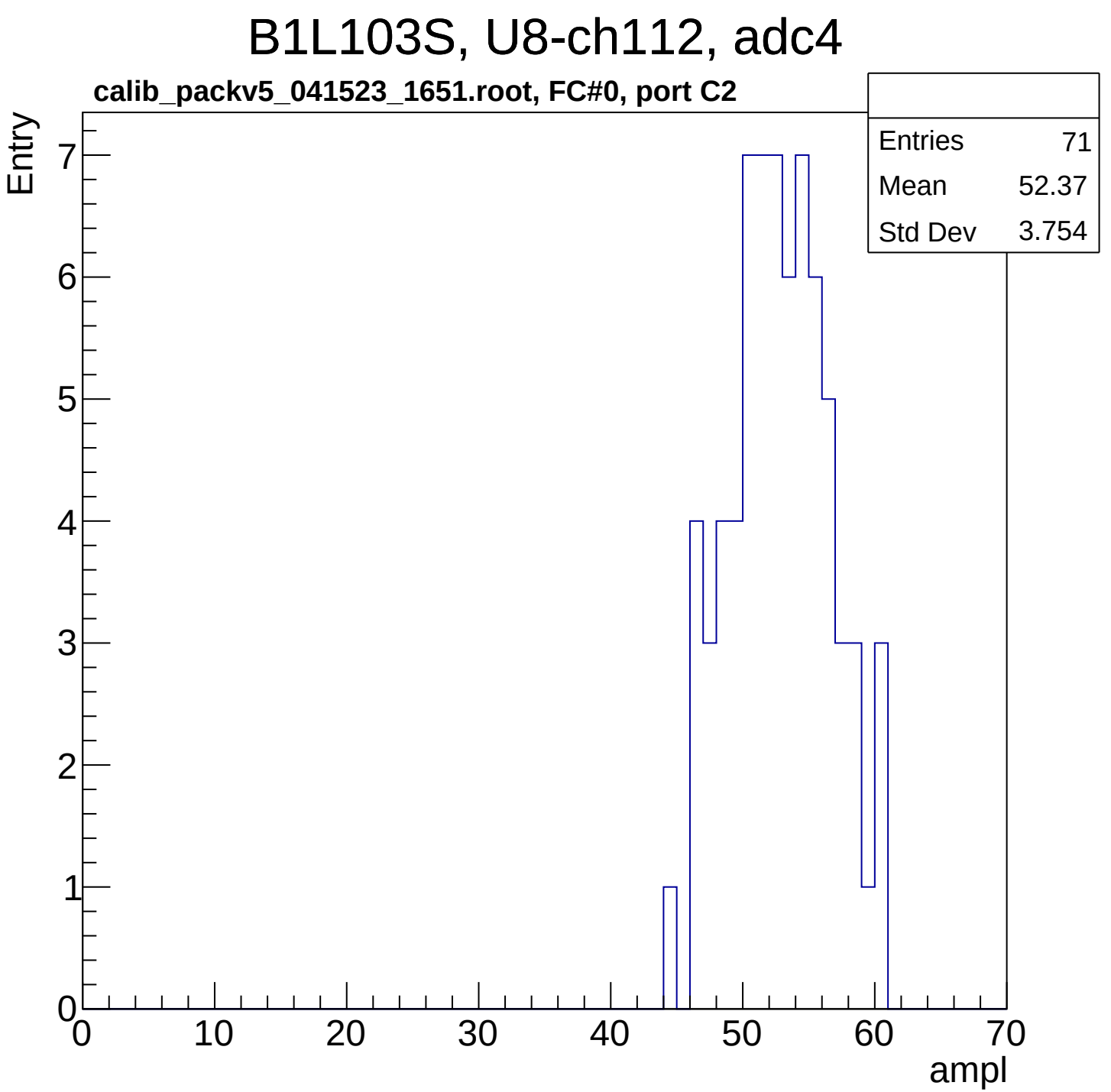
B1L103S, U8-ch112, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 52.37
Std Dev 3.754
Entry
ampl
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2
3
4
5
6
7
0
10
20
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40
50
60
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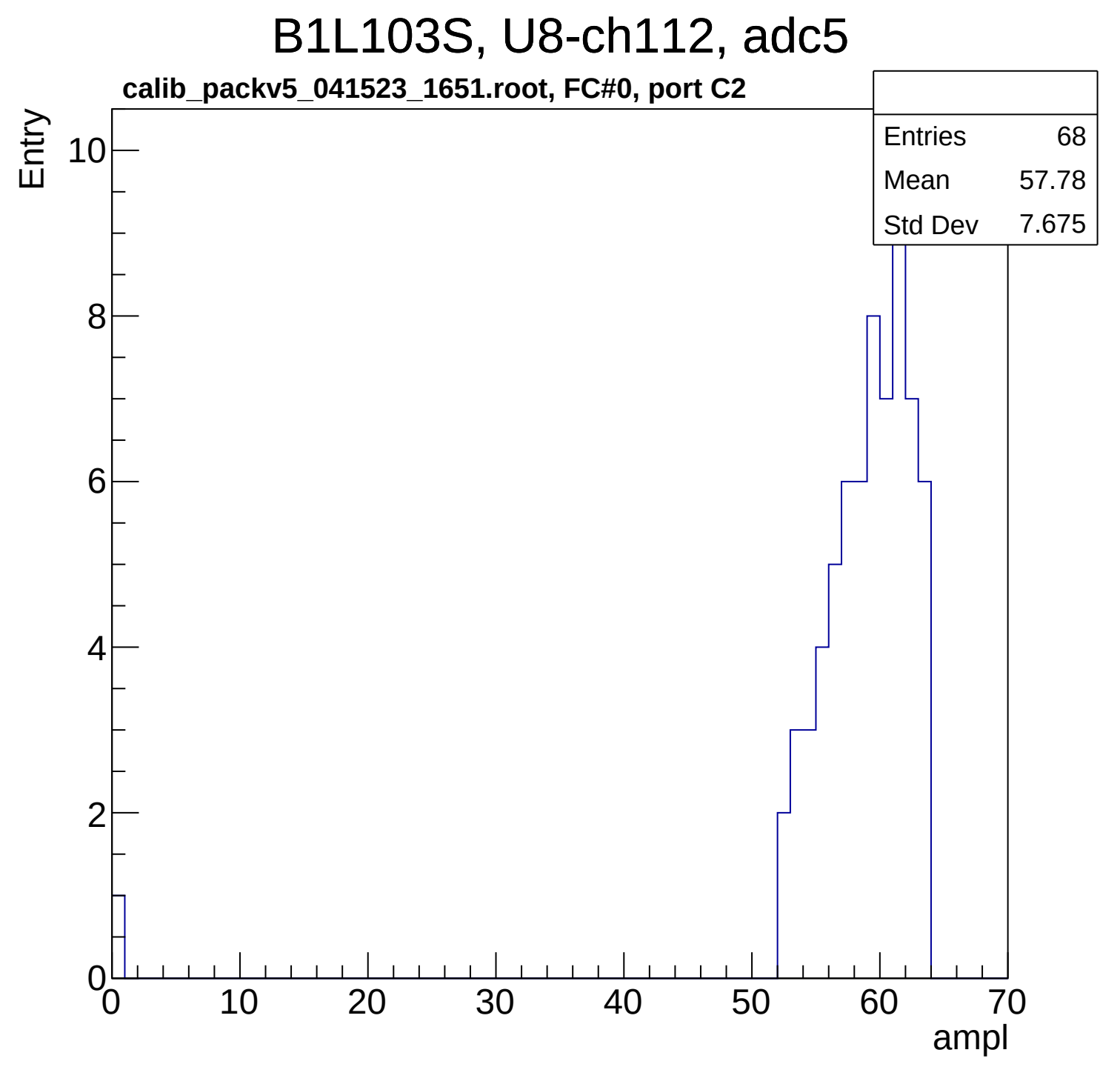
B1L103S, U8-ch112, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 57.78
Std Dev 7.675
Entry
ampl
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4
6
8
10
0
10
20
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40
50
60
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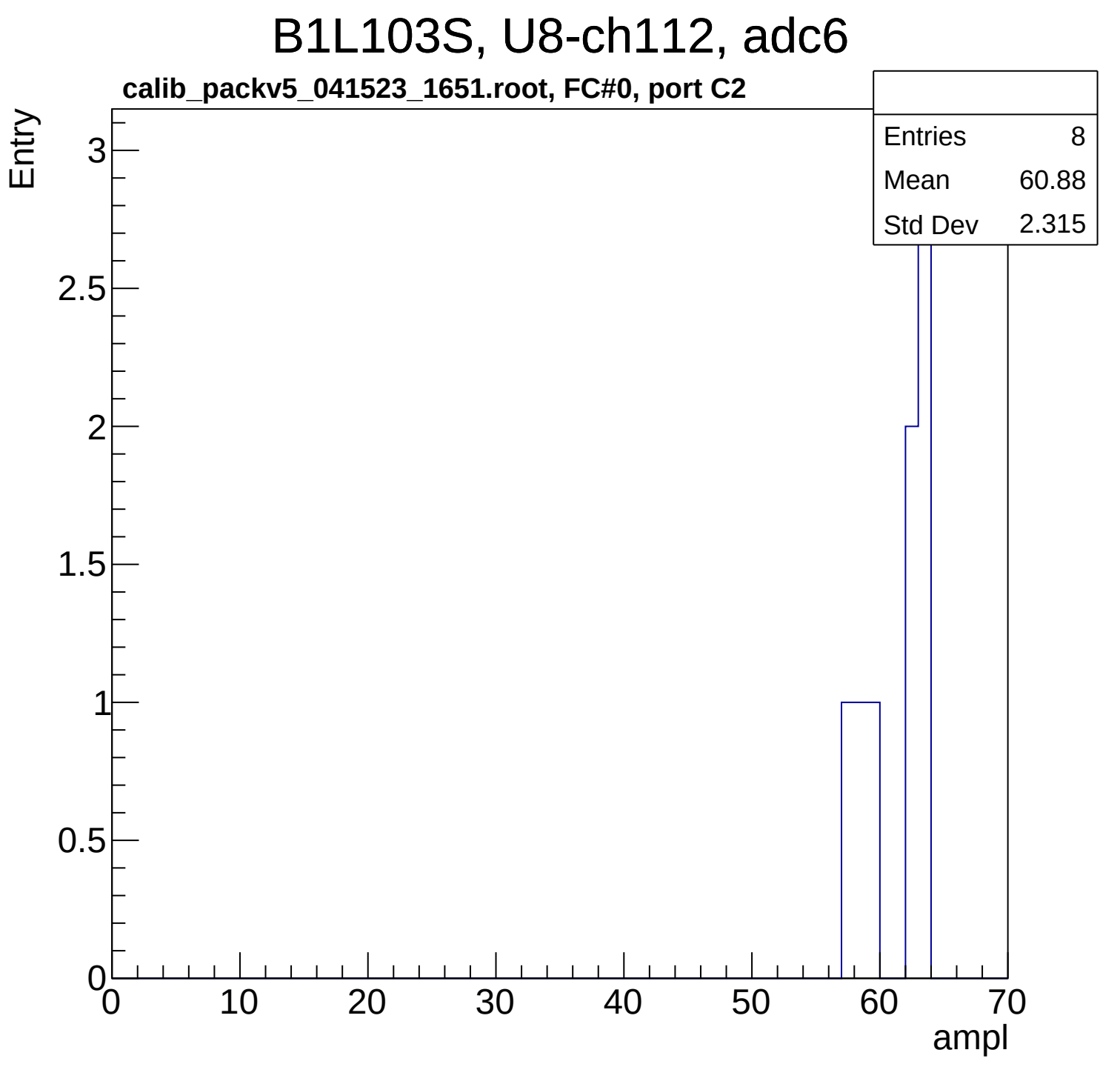
B1L103S, U8-ch112, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 60.88
Std Dev 2.315
Entry
ampl
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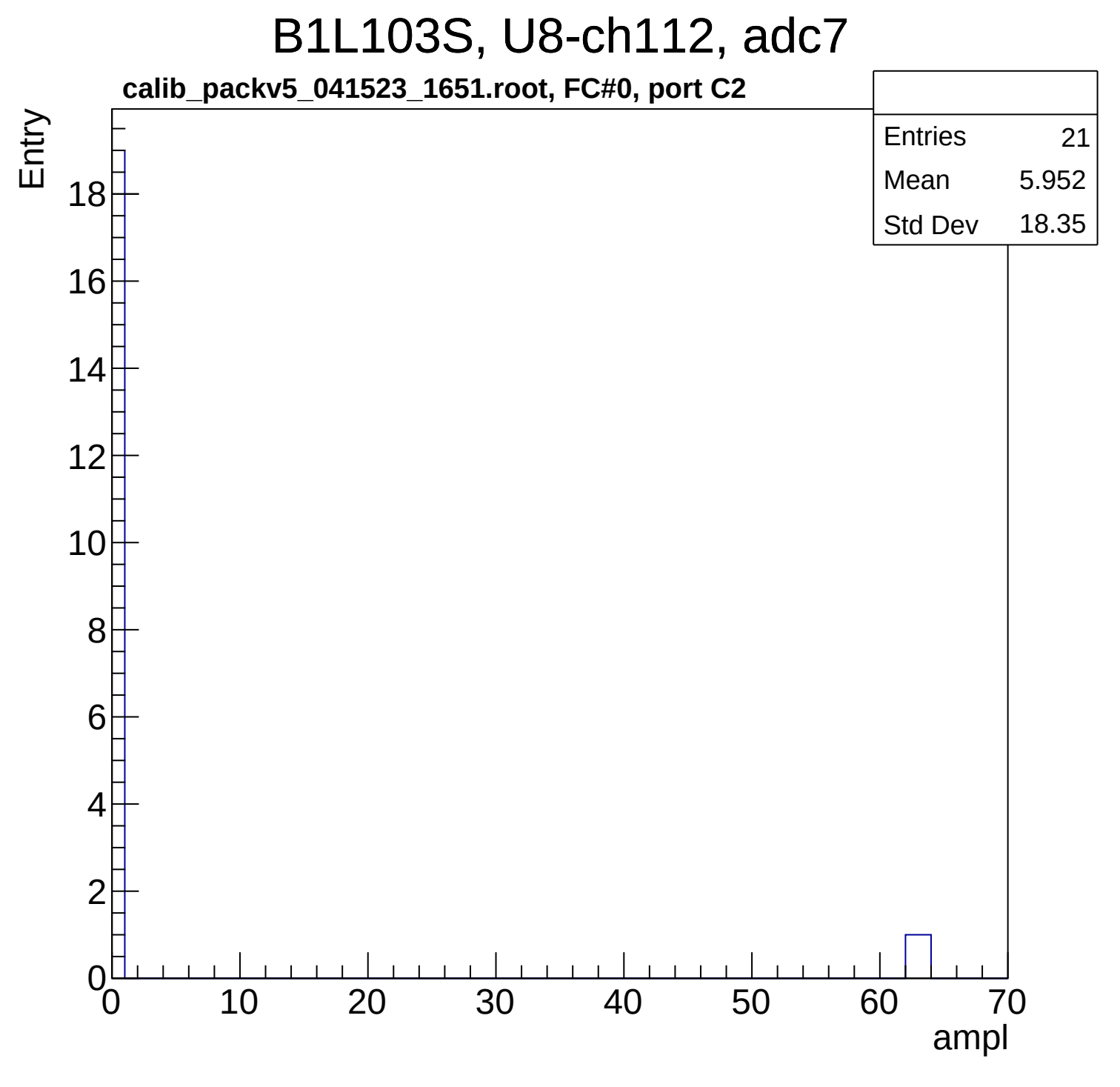
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U8-ch112, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.952
Std Dev 18.35
Entry
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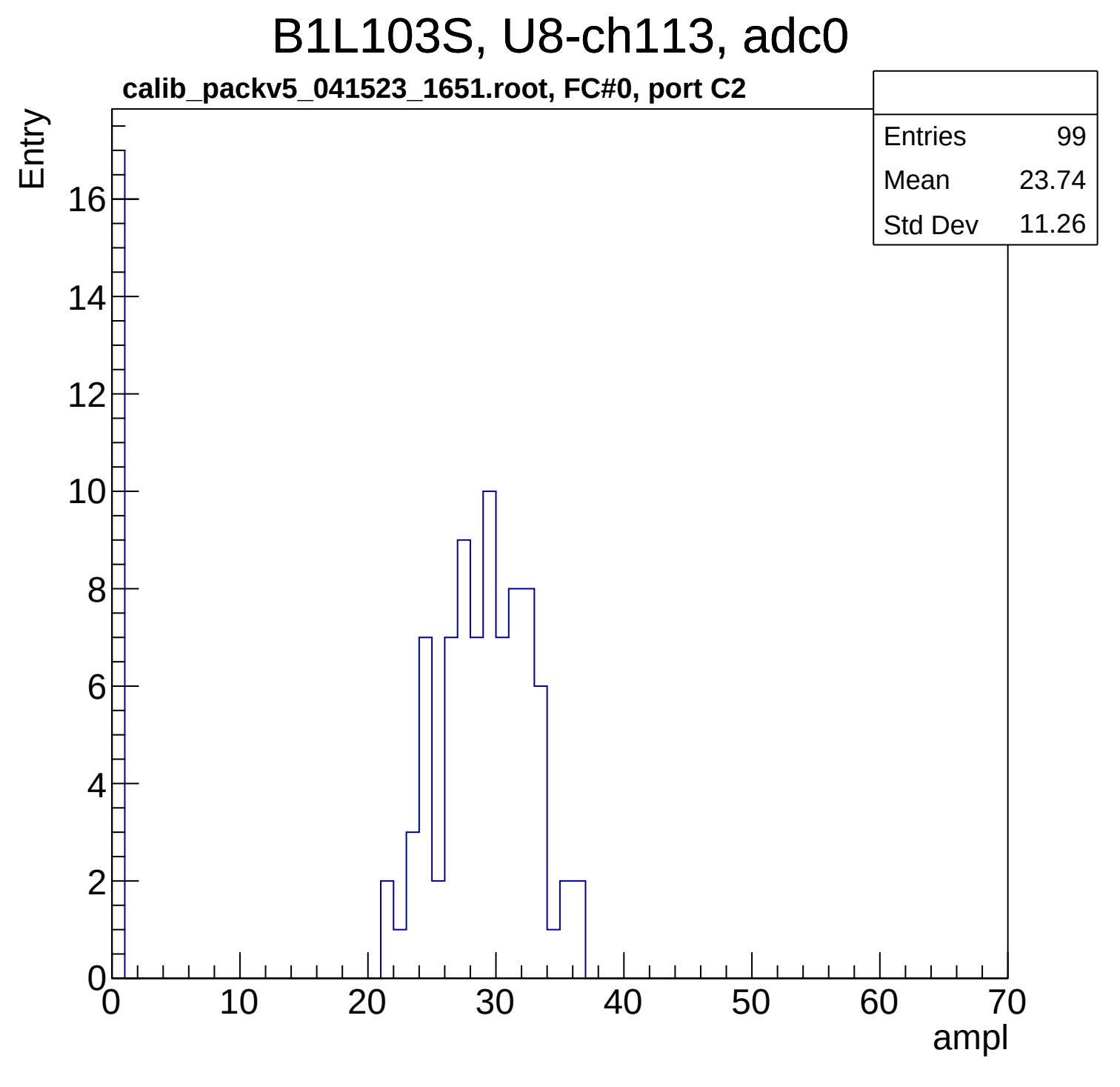
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch113, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 23.74
Std Dev 11.26
Entry
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4
6
8
10
12
14
16
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10
20
30
40
50
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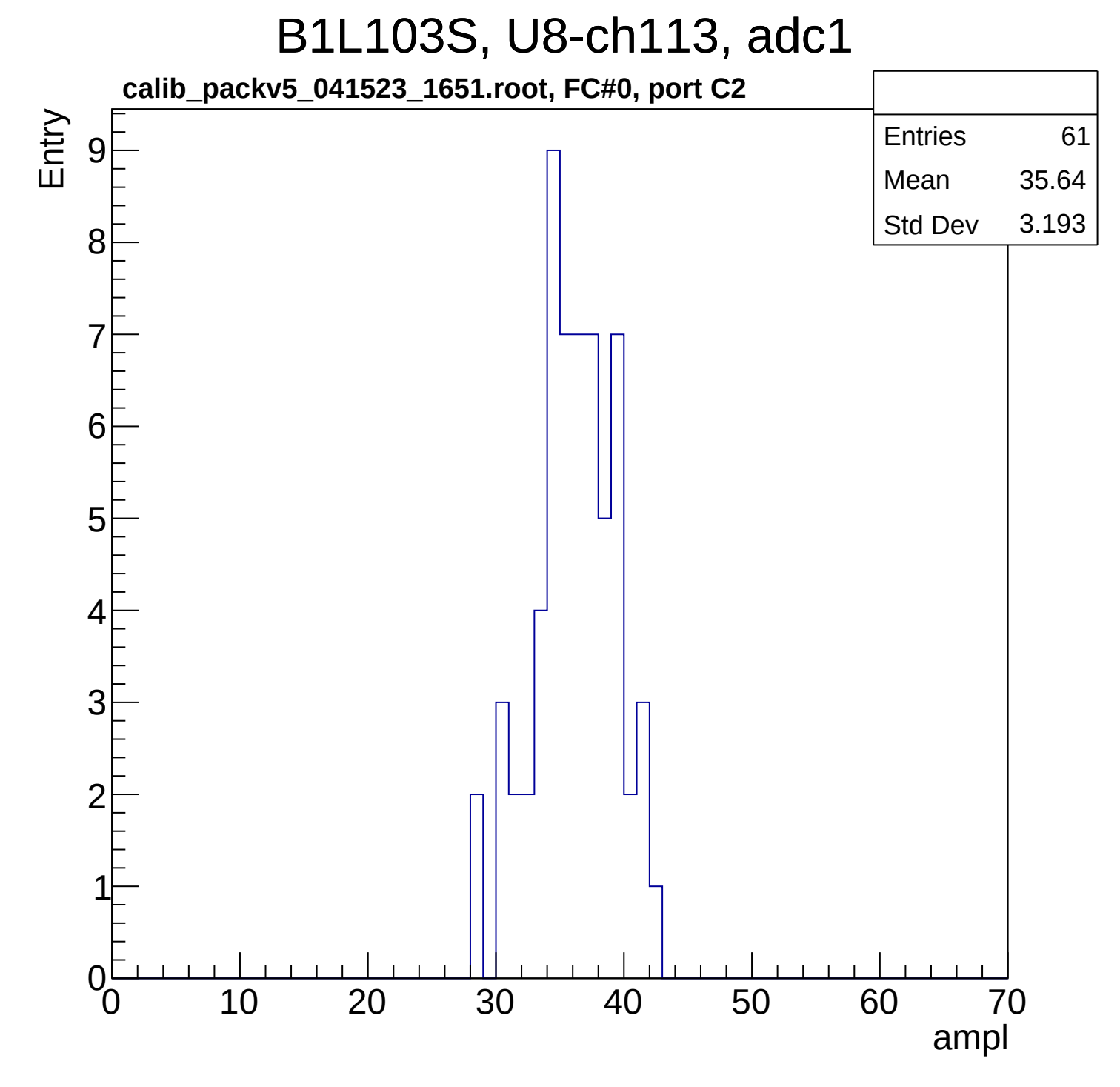
70
ampl


B1L103S, U8-ch113, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 35.64
Std Dev 3.193
Entry
ampl
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3
4
5
6
7
8
9
0
10
20
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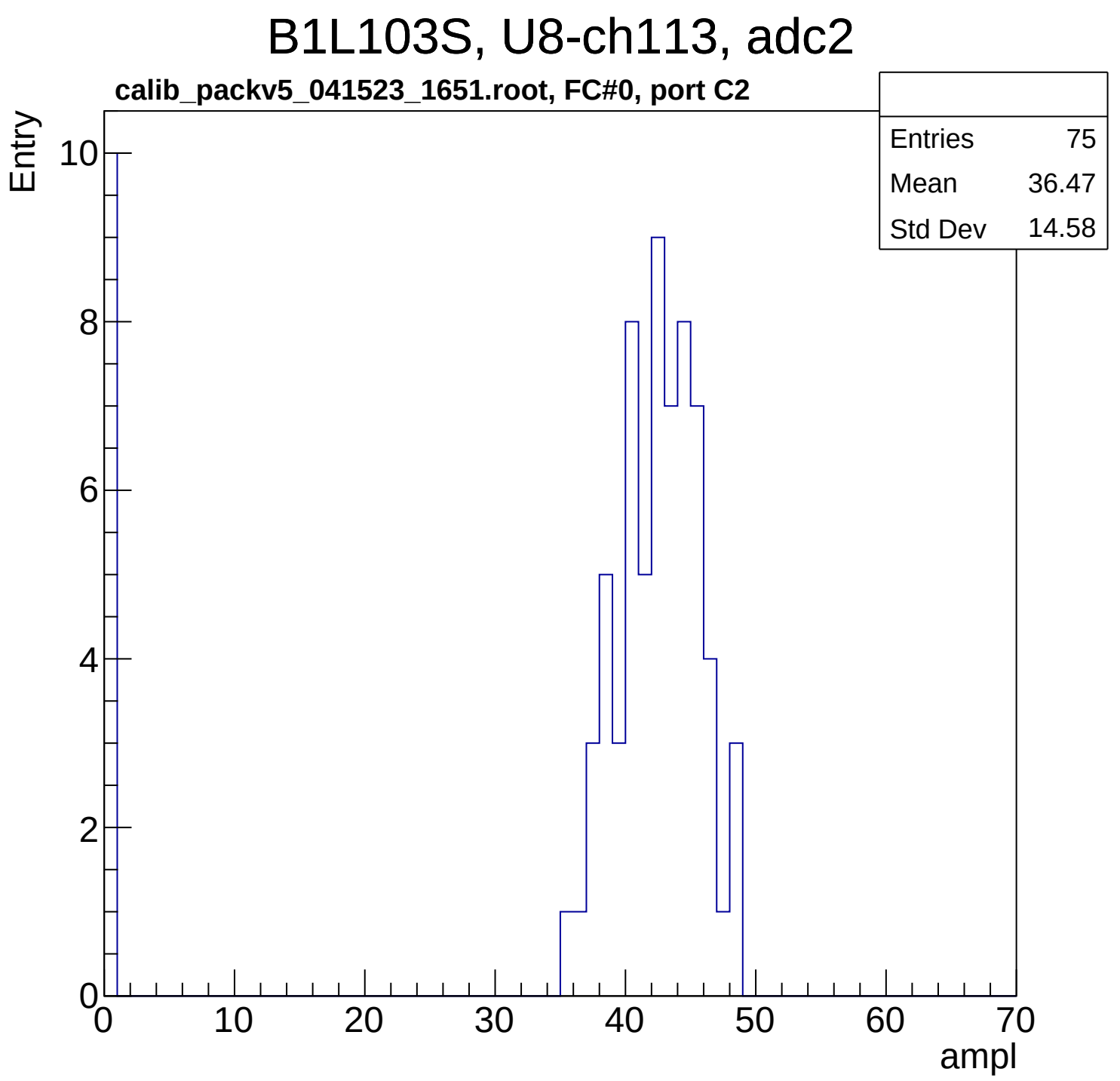
40
50
60
70


B1L103S, U8-ch113, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 36.47
Std Dev 14.58
Entry
ampl
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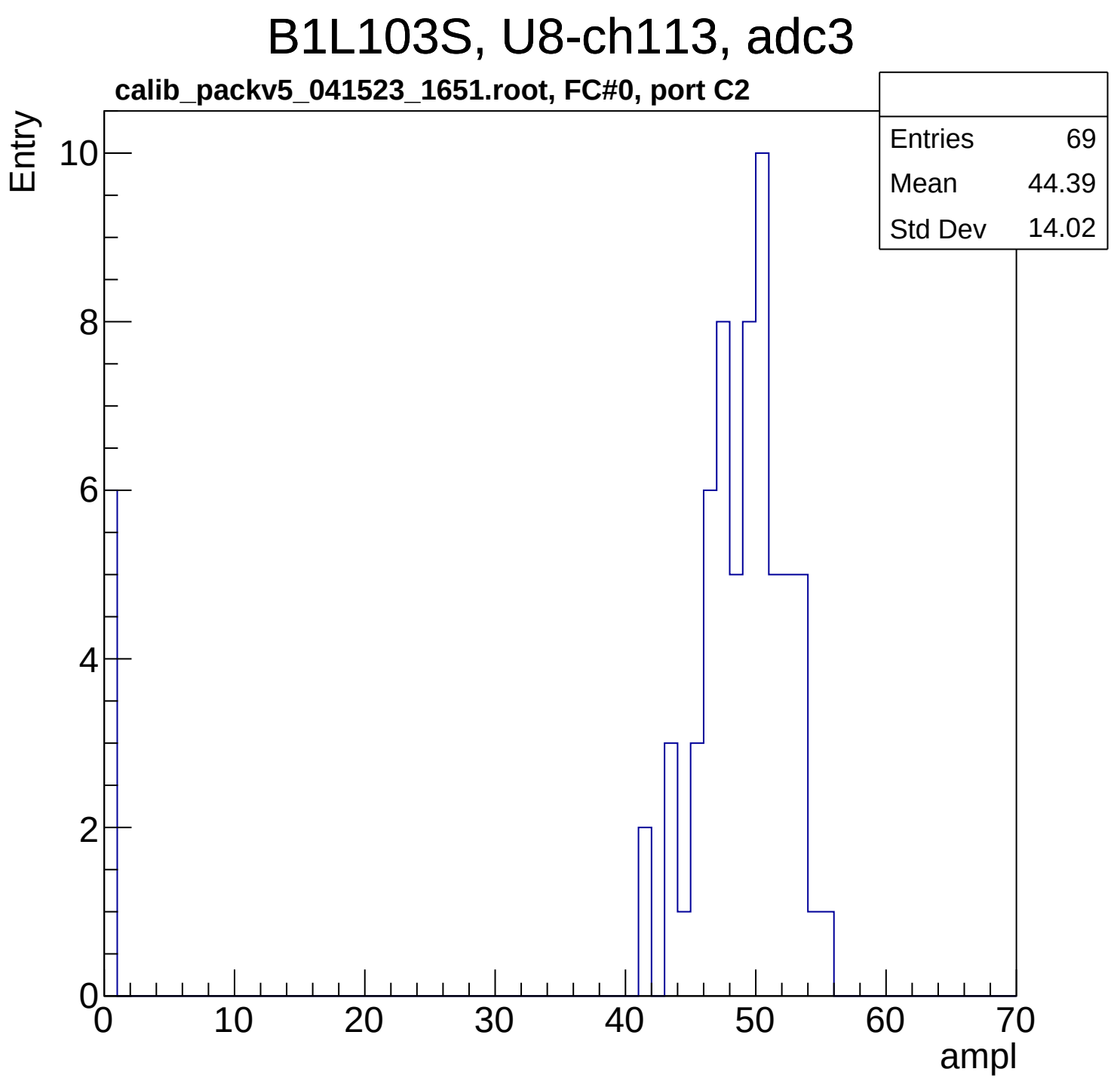
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U8-ch113, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 44.39
Std Dev 14.02
Entry
ampl
0
2
4
6
8
10
0
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20
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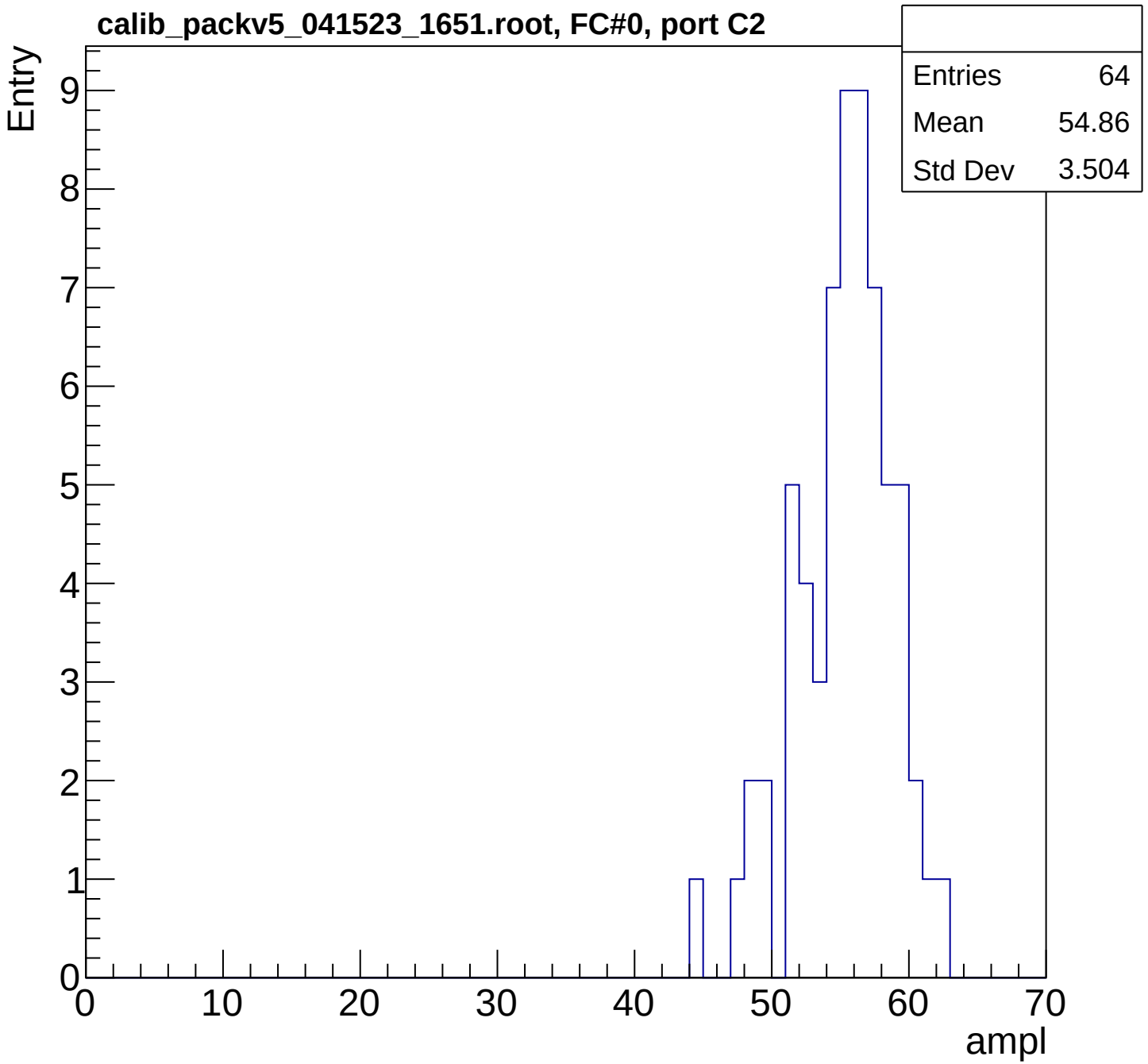
60
70


B1L103S, U8-ch113, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 54.86
Std Dev 3.504
Entry
ampl
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3
4
5
6
7
8
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0
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40
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60
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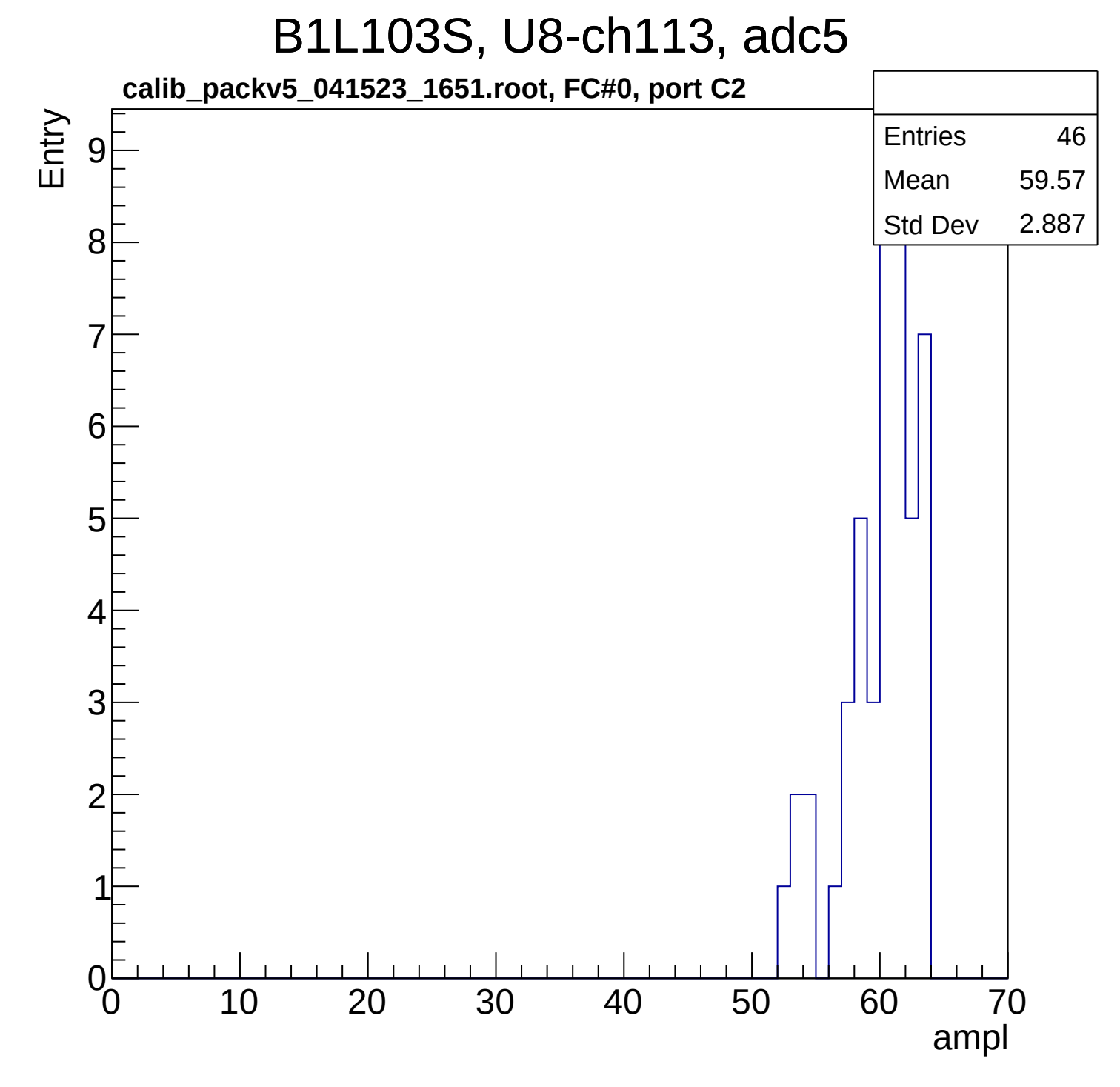
B1L103S, U8-ch113, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 59.57
Std Dev 2.887
Entry
ampl
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6
7
8
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0
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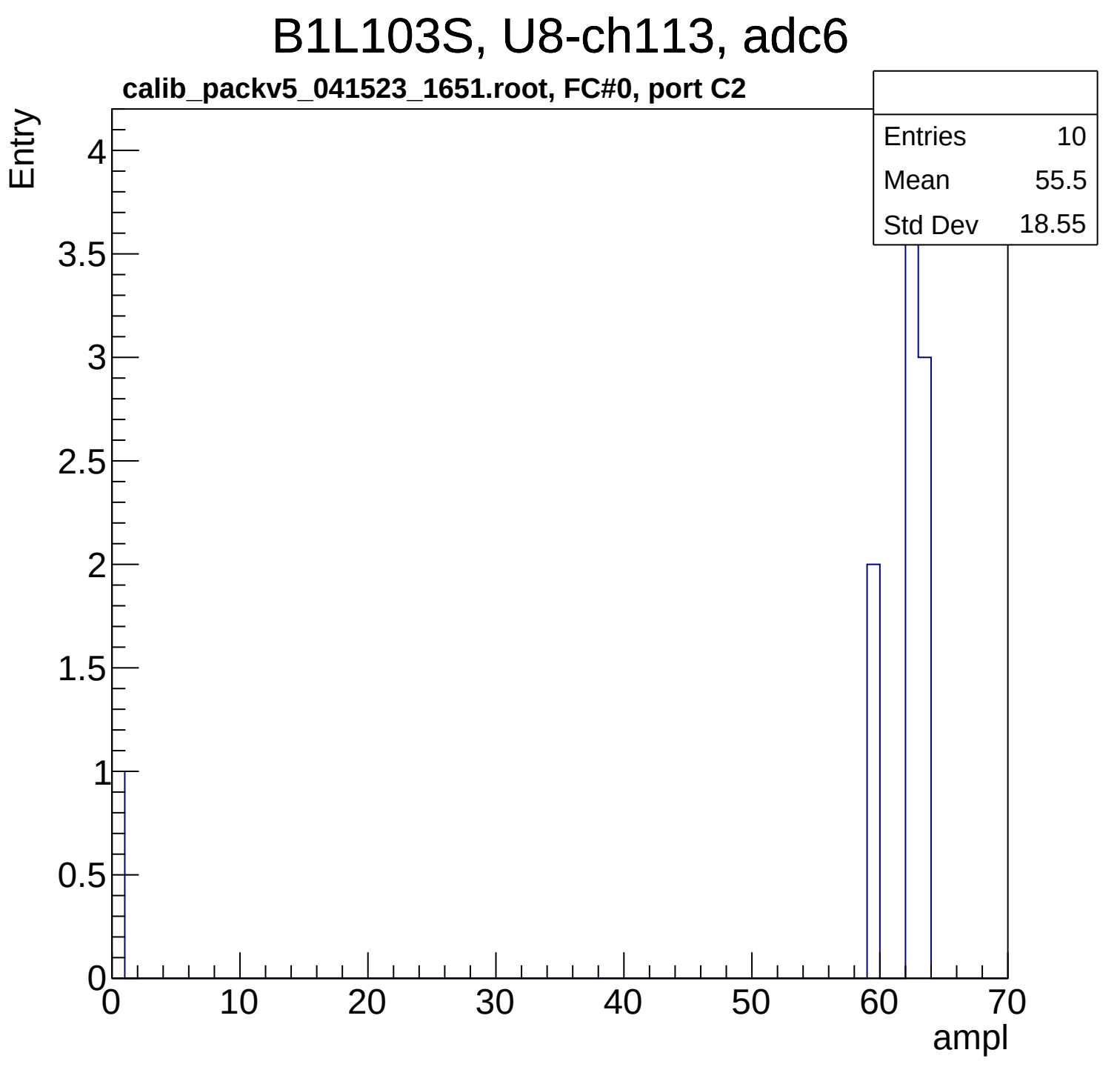
B1L103S, U8-ch113, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 55.5
Std Dev 18.55
Entry
ampl
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0.5
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1.5
2
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3
3.5
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0
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20
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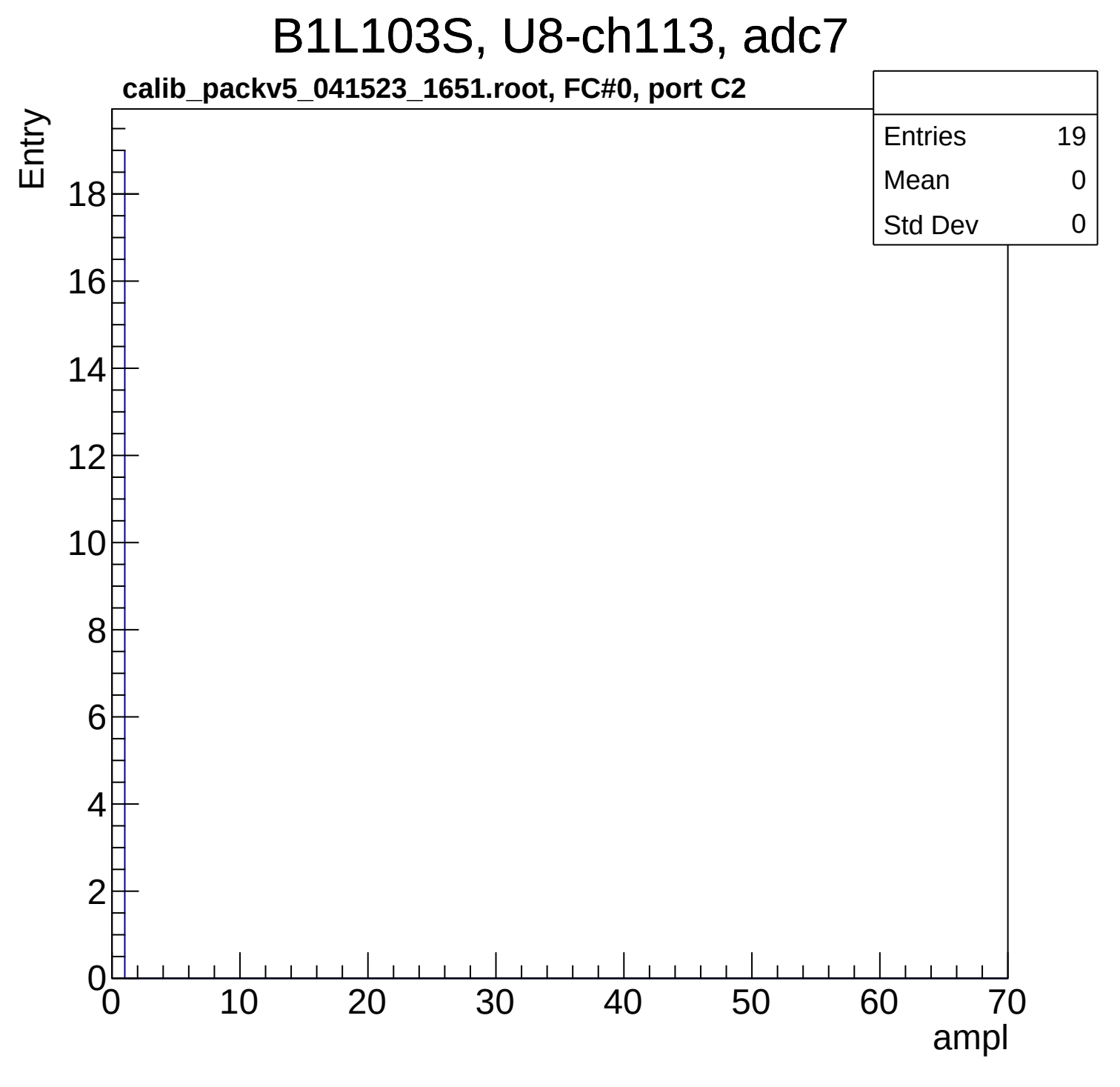
60
70


B1L103S, U8-ch113, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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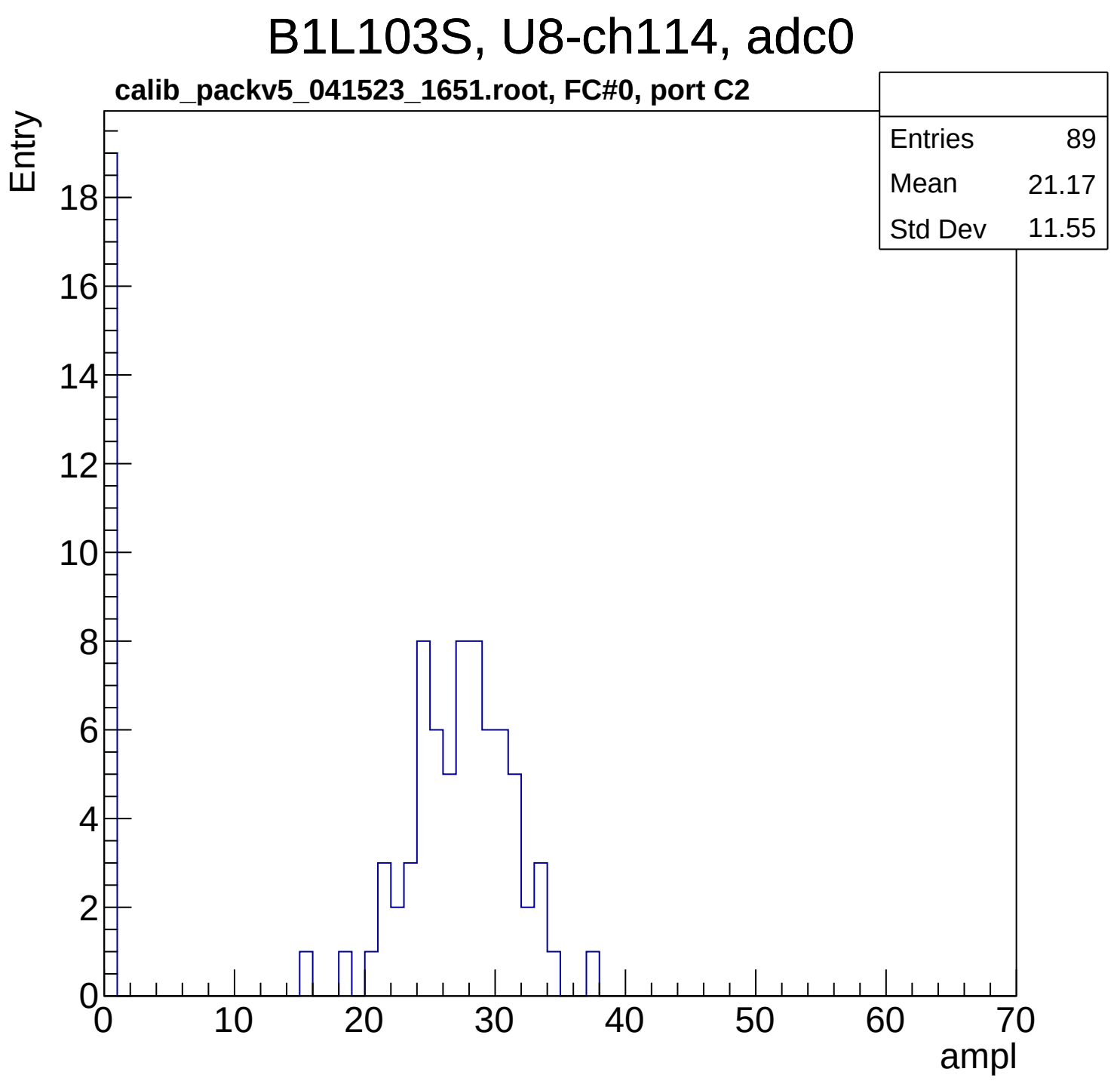
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch114, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 21.17
Std Dev 11.55
Entry
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6
8
10
12
14
16
18
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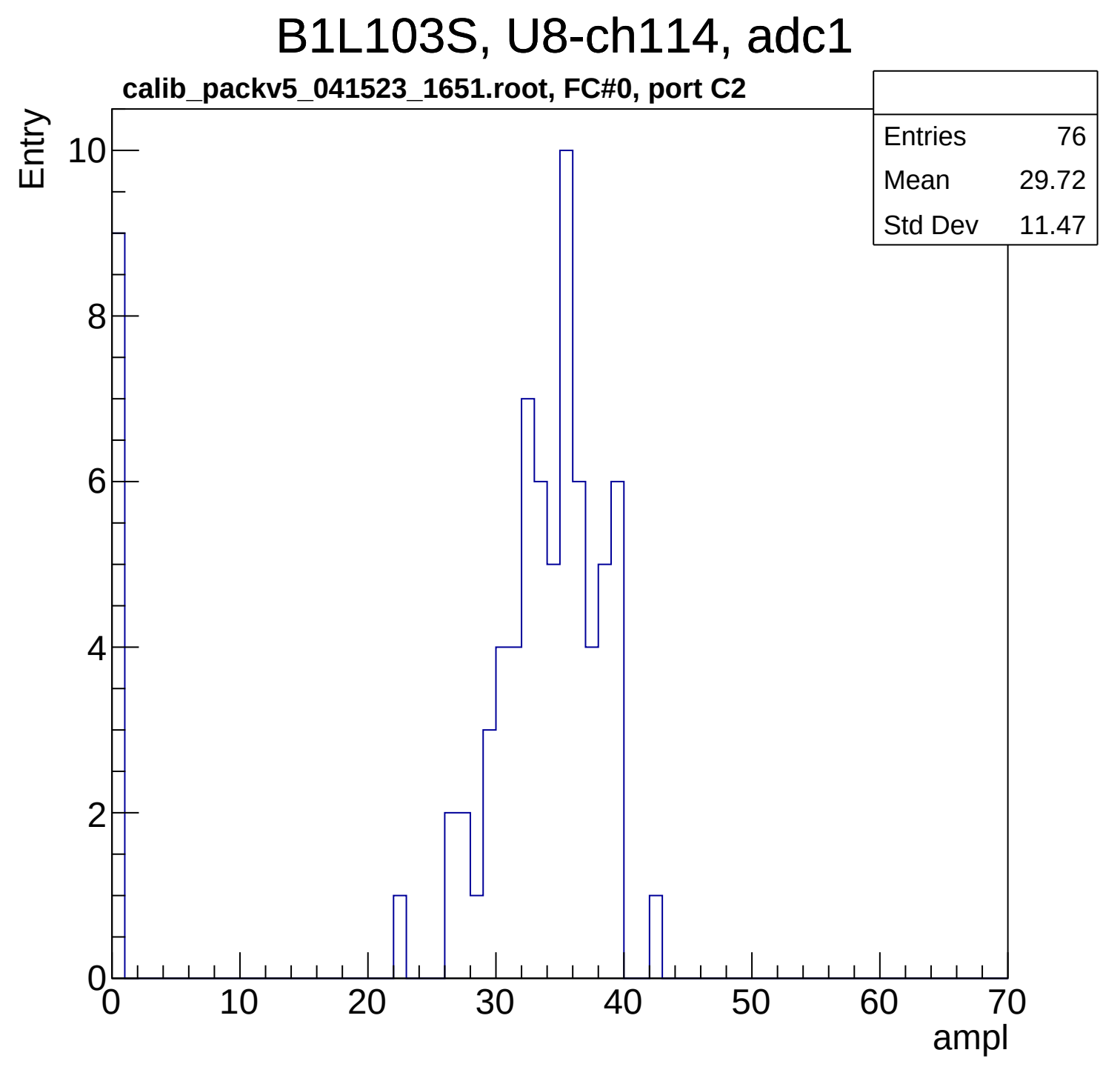
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch114, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 29.72
Std Dev 11.47
Entry
ampl
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6
8
10
0
10
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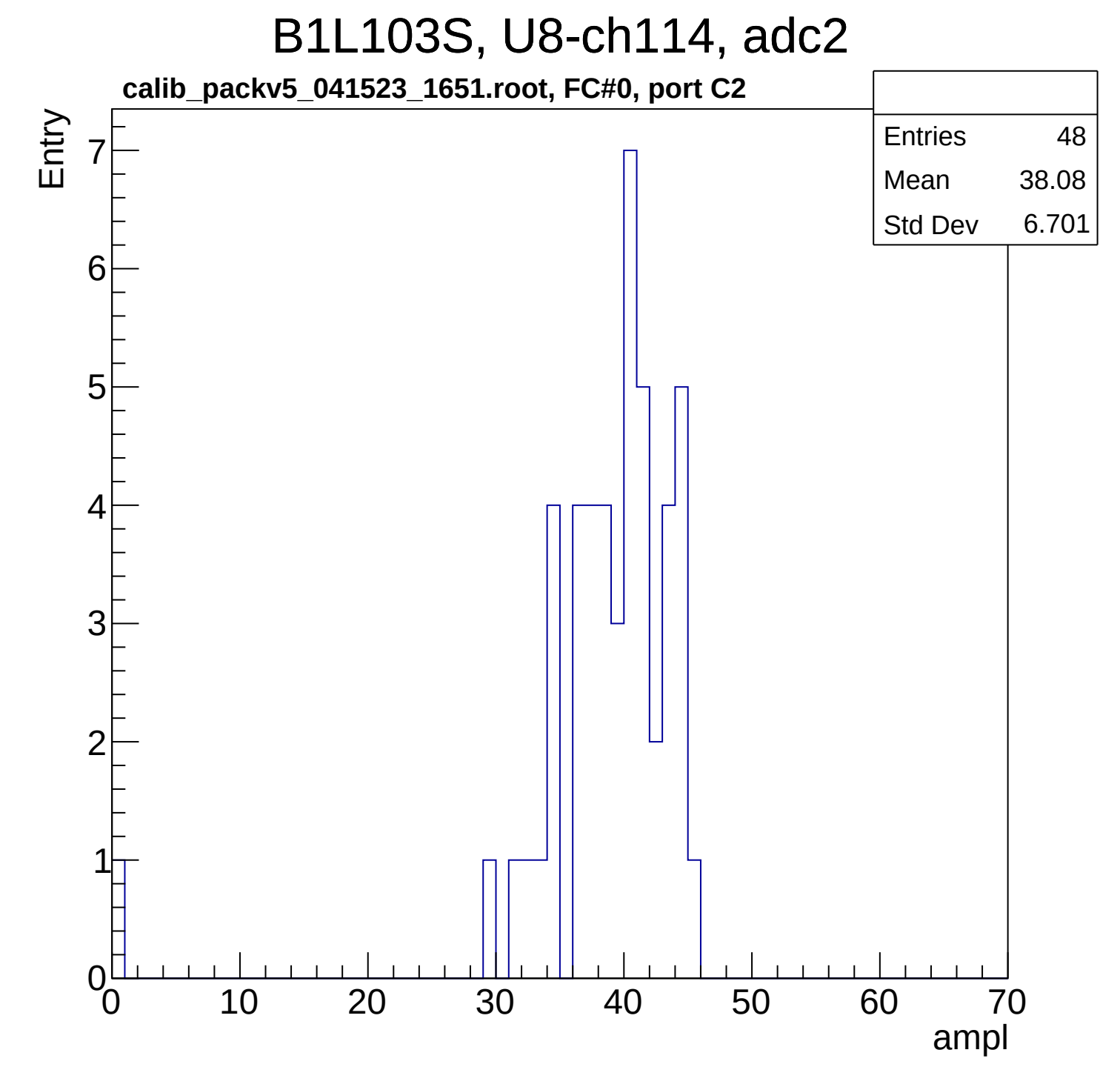
40
50
60
70


B1L103S, U8-ch114, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 38.08
Std Dev 6.701
Entry
ampl
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3
4
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6
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0
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60
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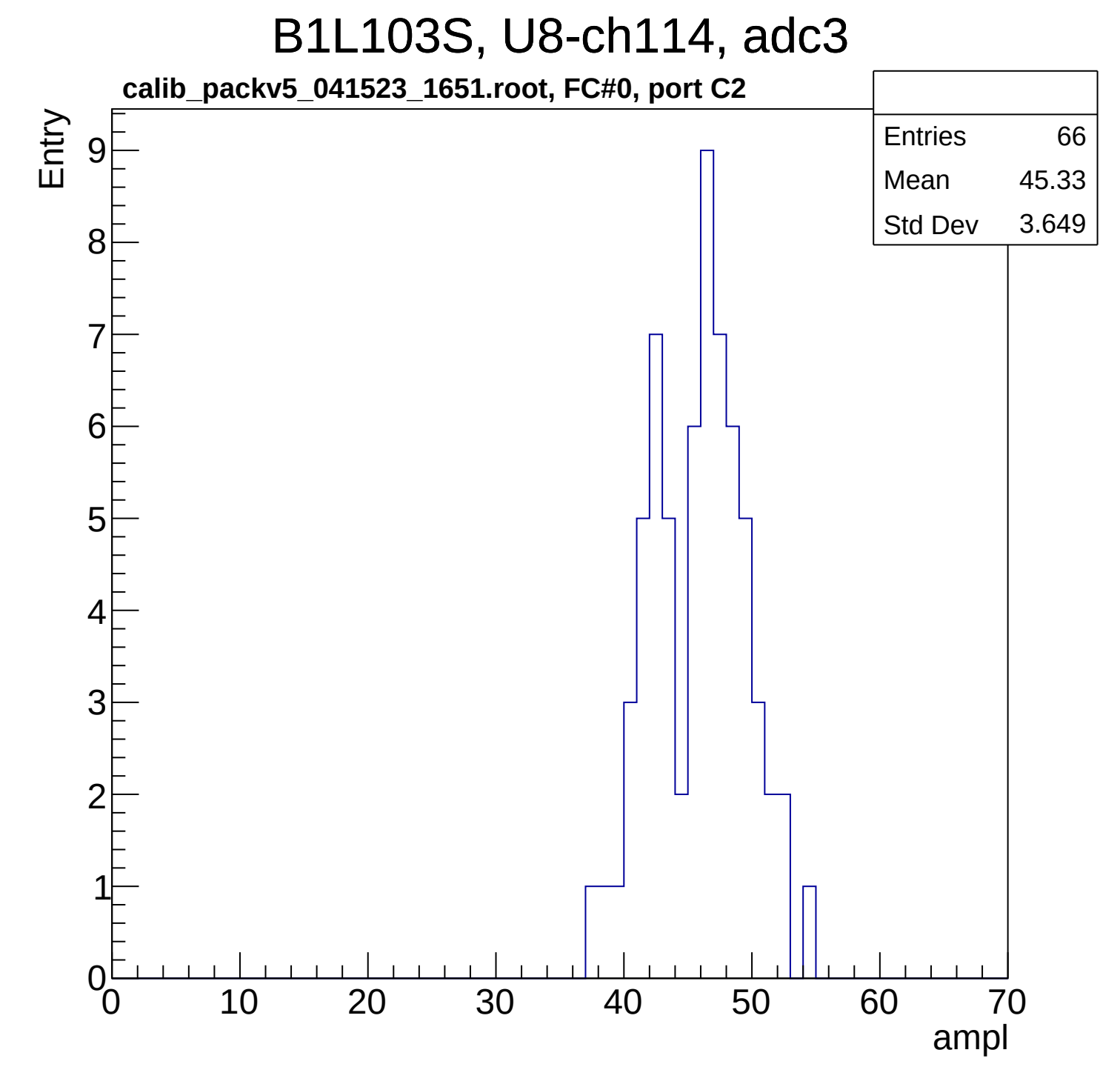
B1L103S, U8-ch114, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 45.33
Std Dev 3.649
Entry
ampl
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2
3
4
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6
7
8
9
0
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50
60
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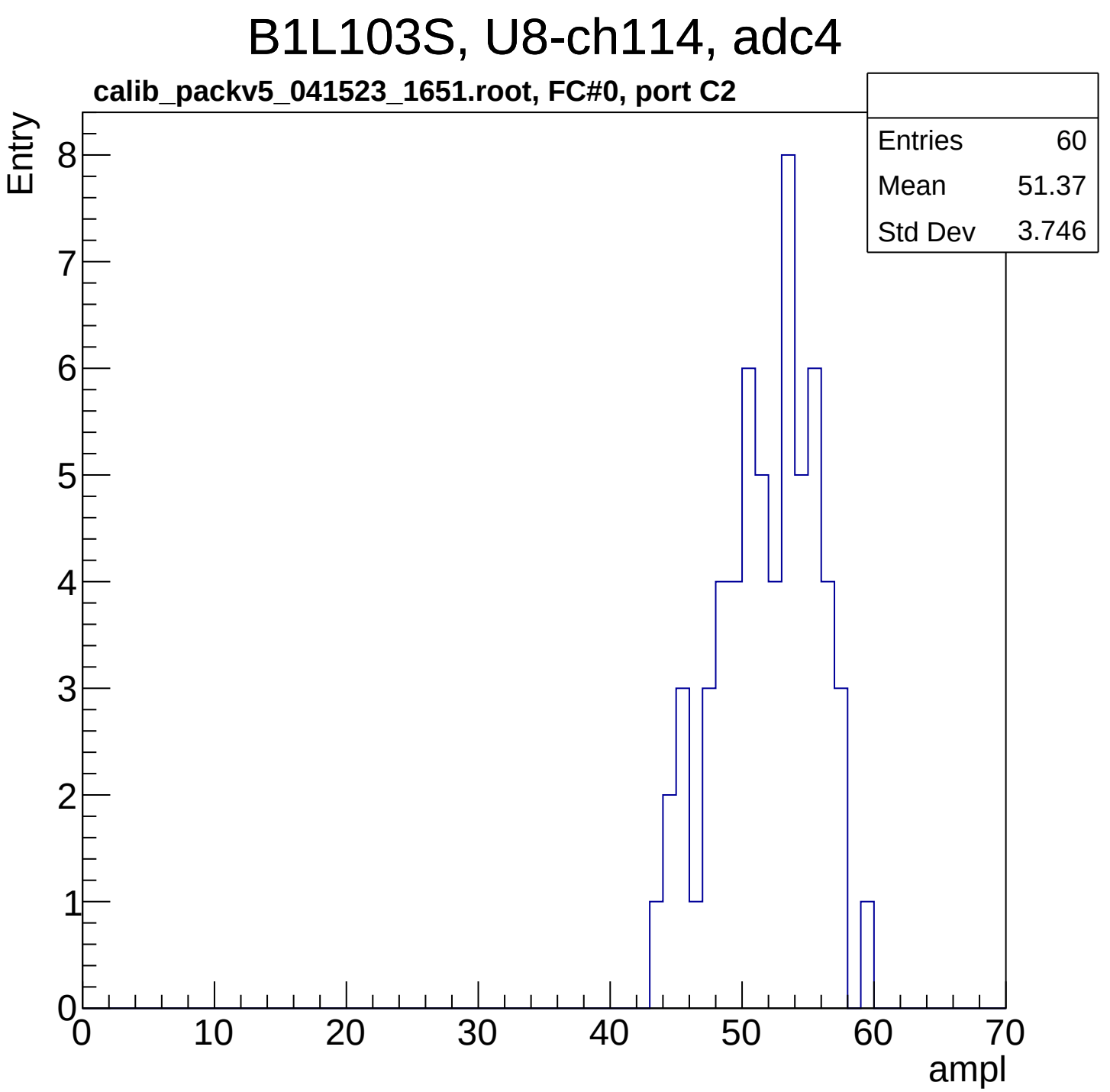
B1L103S, U8-ch114, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 51.37
Std Dev 3.746
Entry
ampl
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1
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5
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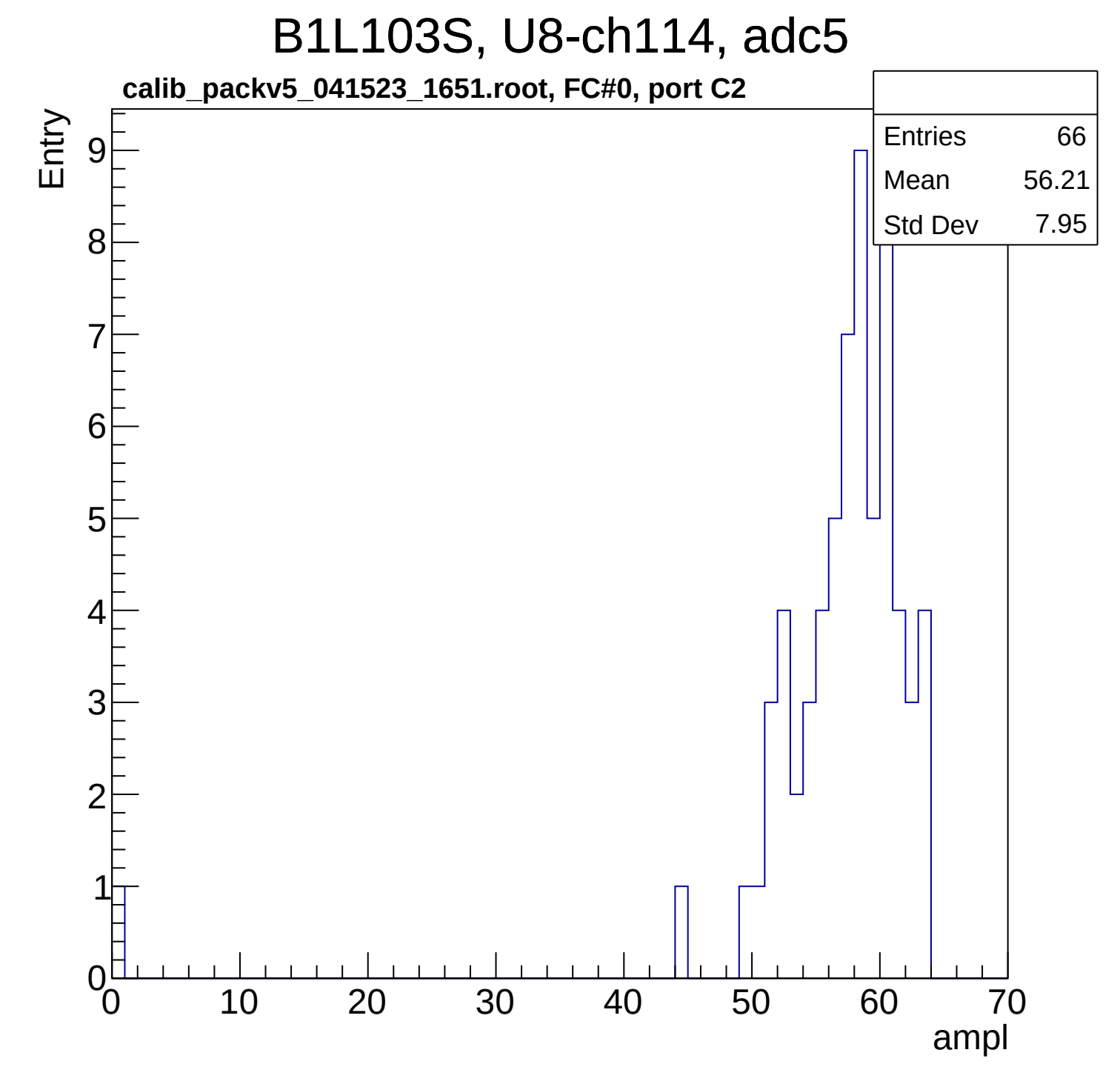
B1L103S, U8-ch114, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 56.21
Std Dev 7.95
Entry
ampl
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3
4
5
6
7
8
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0
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20
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40
50
60
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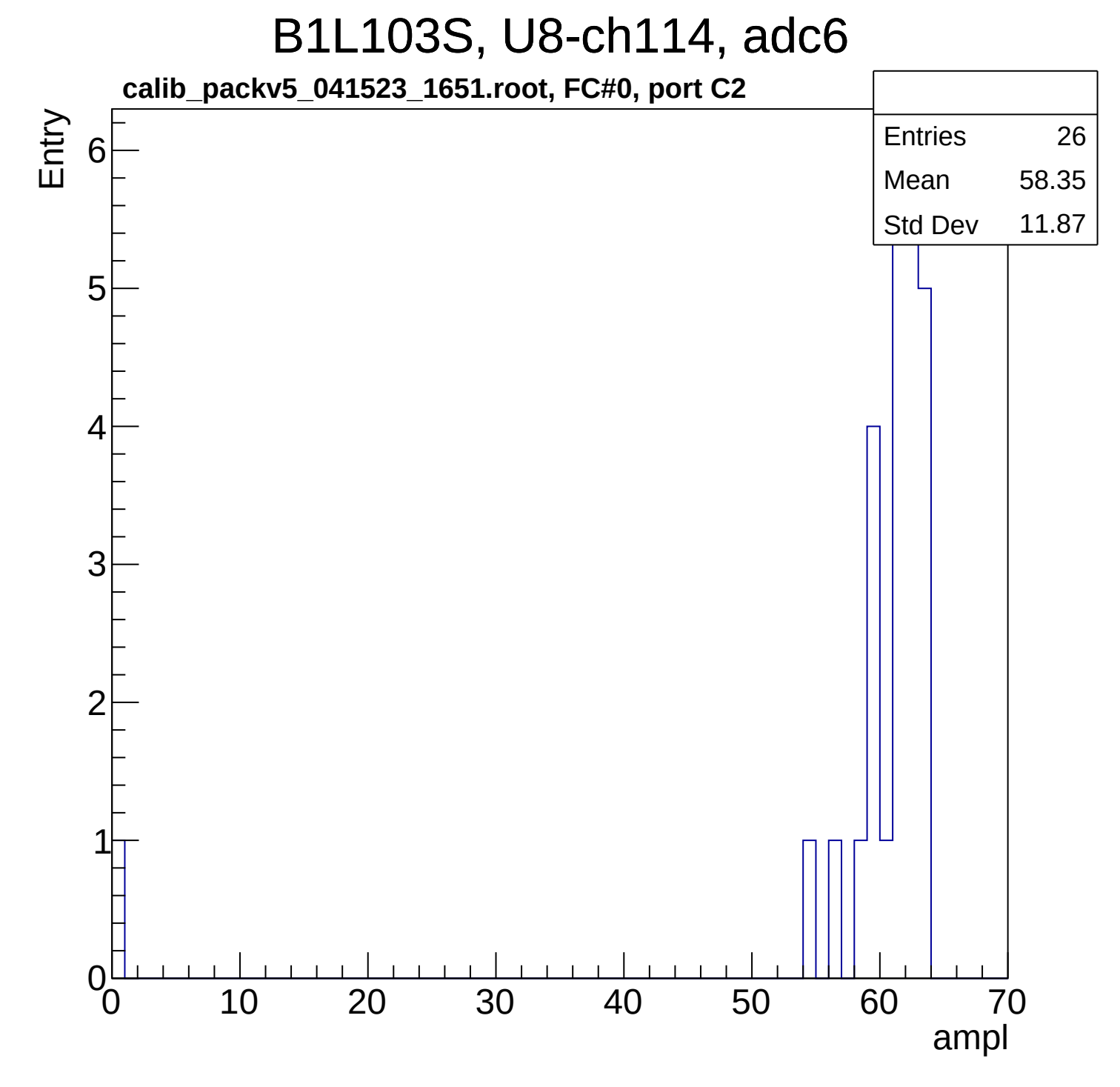
B1L103S, U8-ch114, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 58.35
Std Dev 11.87
Entry
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6
0
10
20
30
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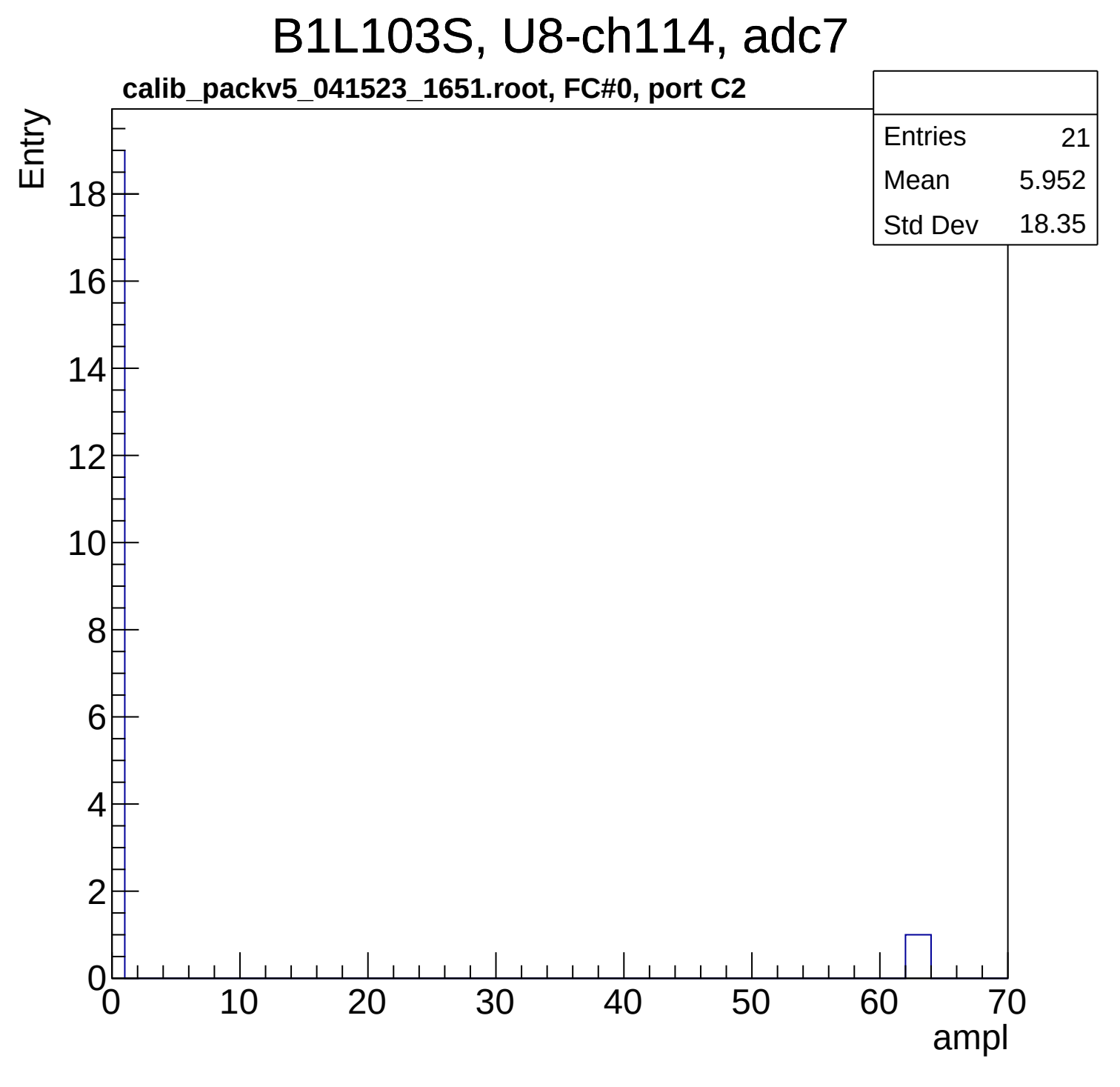
50
60
70
ampl


B1L103S, U8-ch114, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.952
Std Dev 18.35
Entry
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6
8
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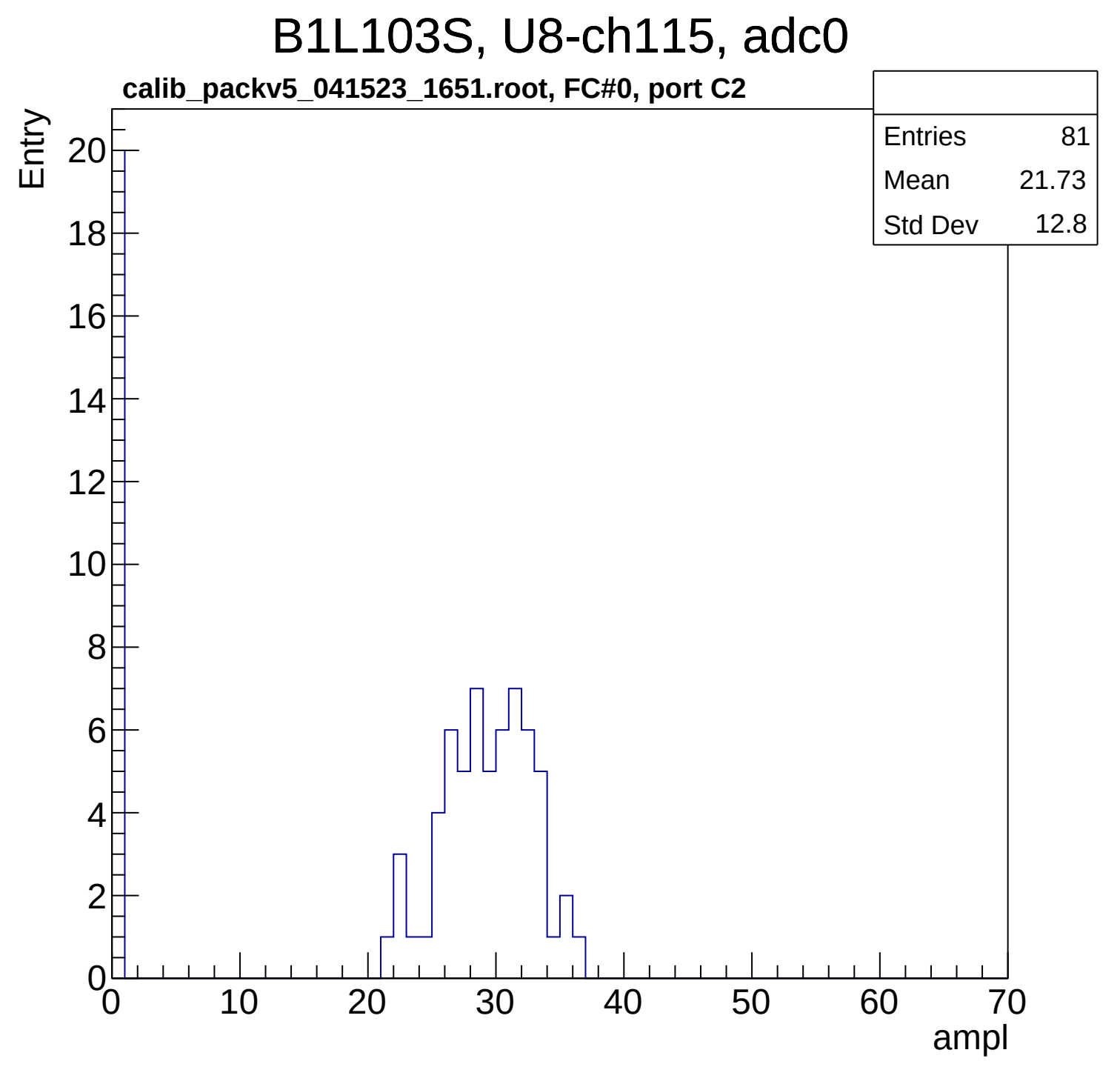
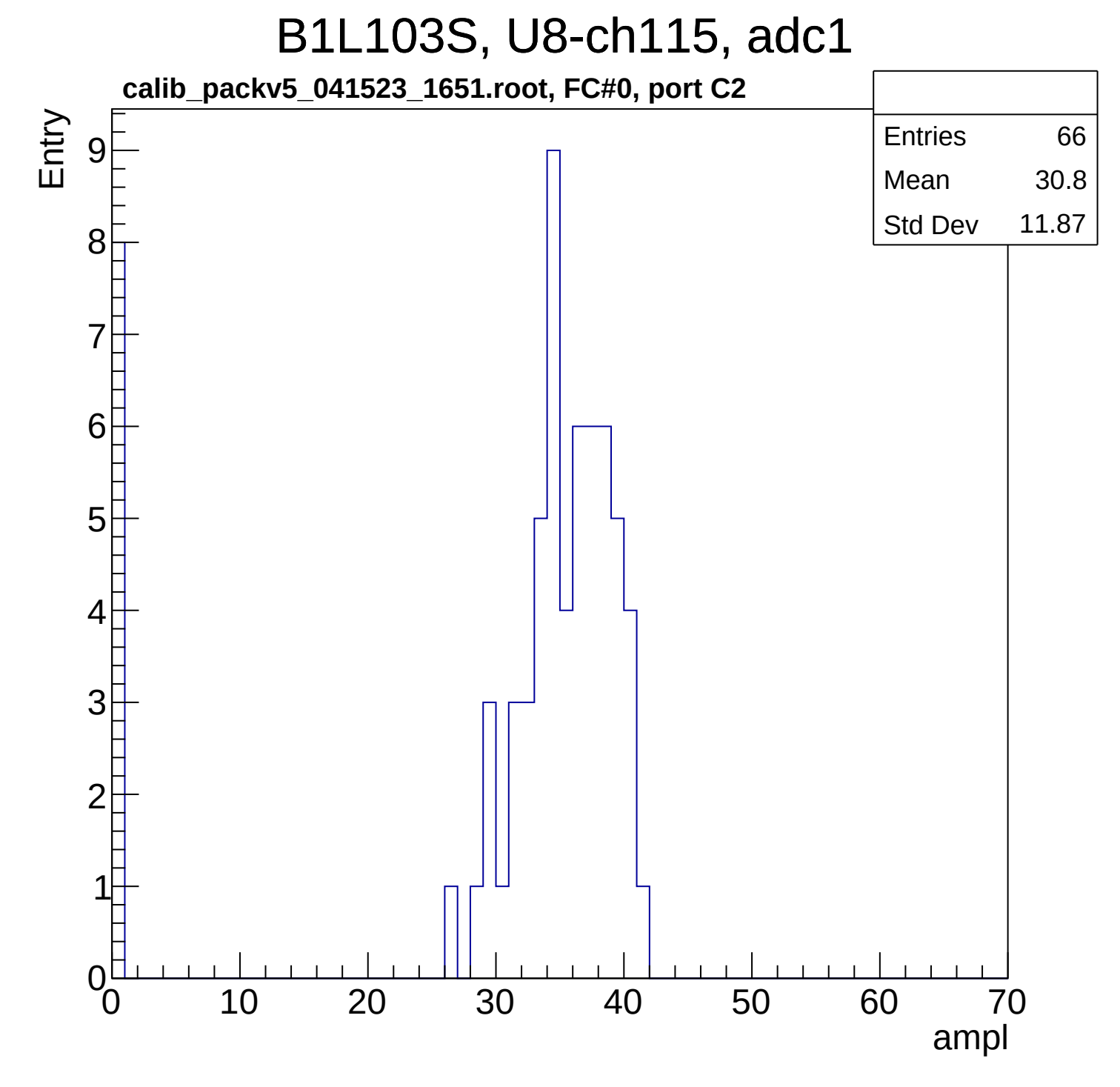
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch115, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 21.73
Std Dev 12.8
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70


B1L103S, U8-ch115, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 30.8
Std Dev 11.87
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
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40
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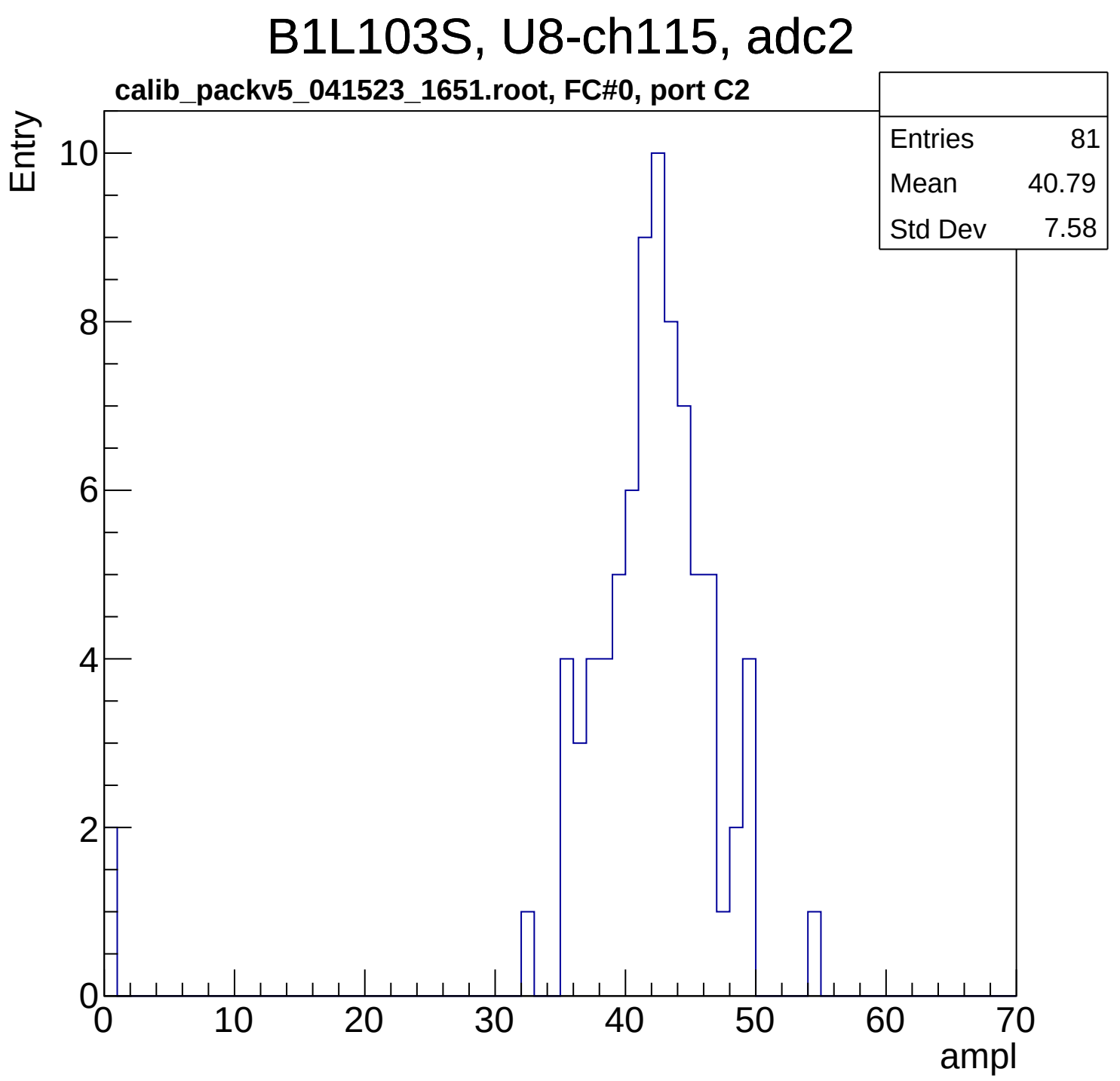
B1L103S, U8-ch115, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 40.79
Std Dev 7.58
Entry
ampl
0
2
4
6
8
10
0
10
20
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40
50
60
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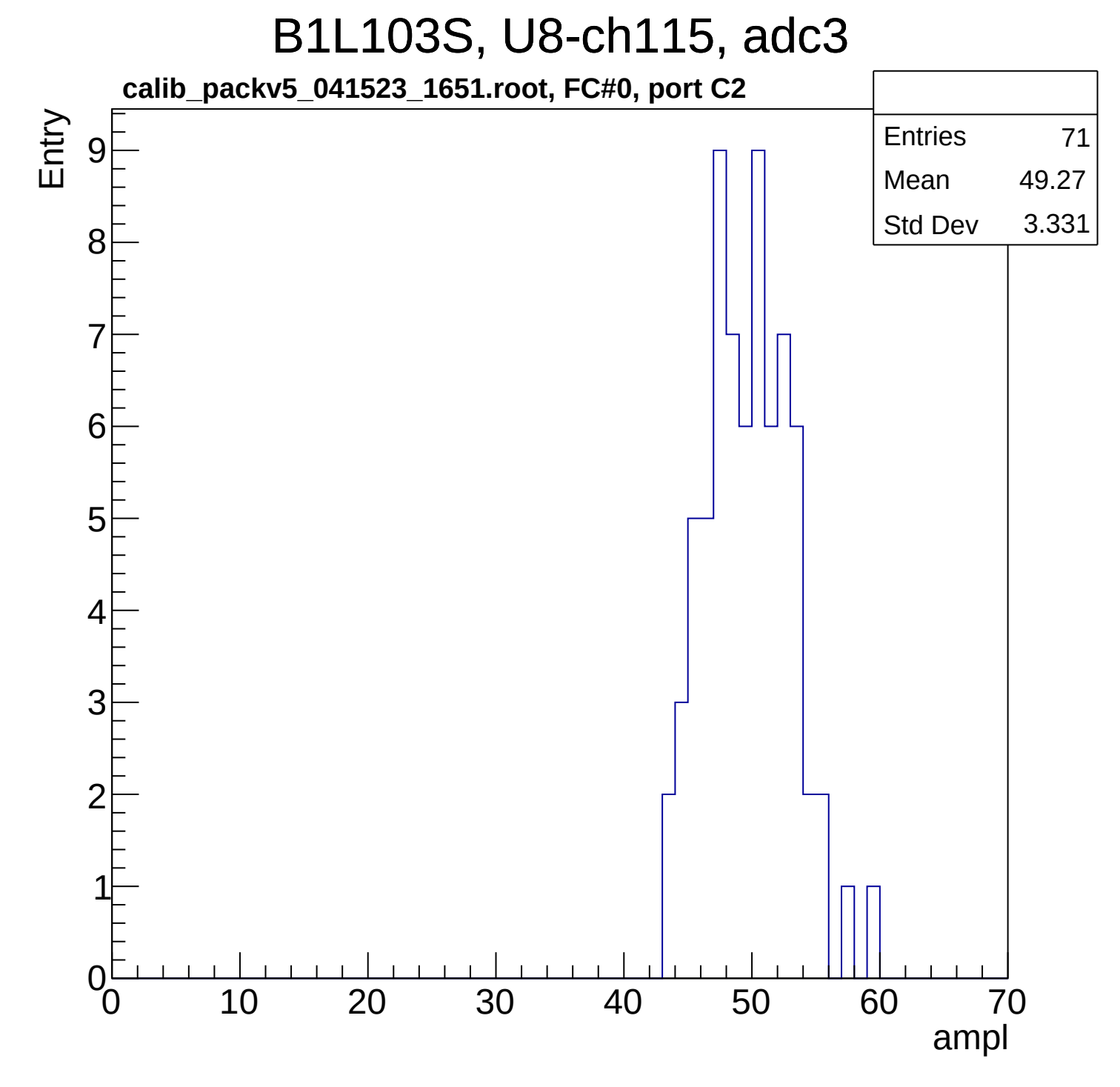
B1L103S, U8-ch115, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 49.27
Std Dev 3.331
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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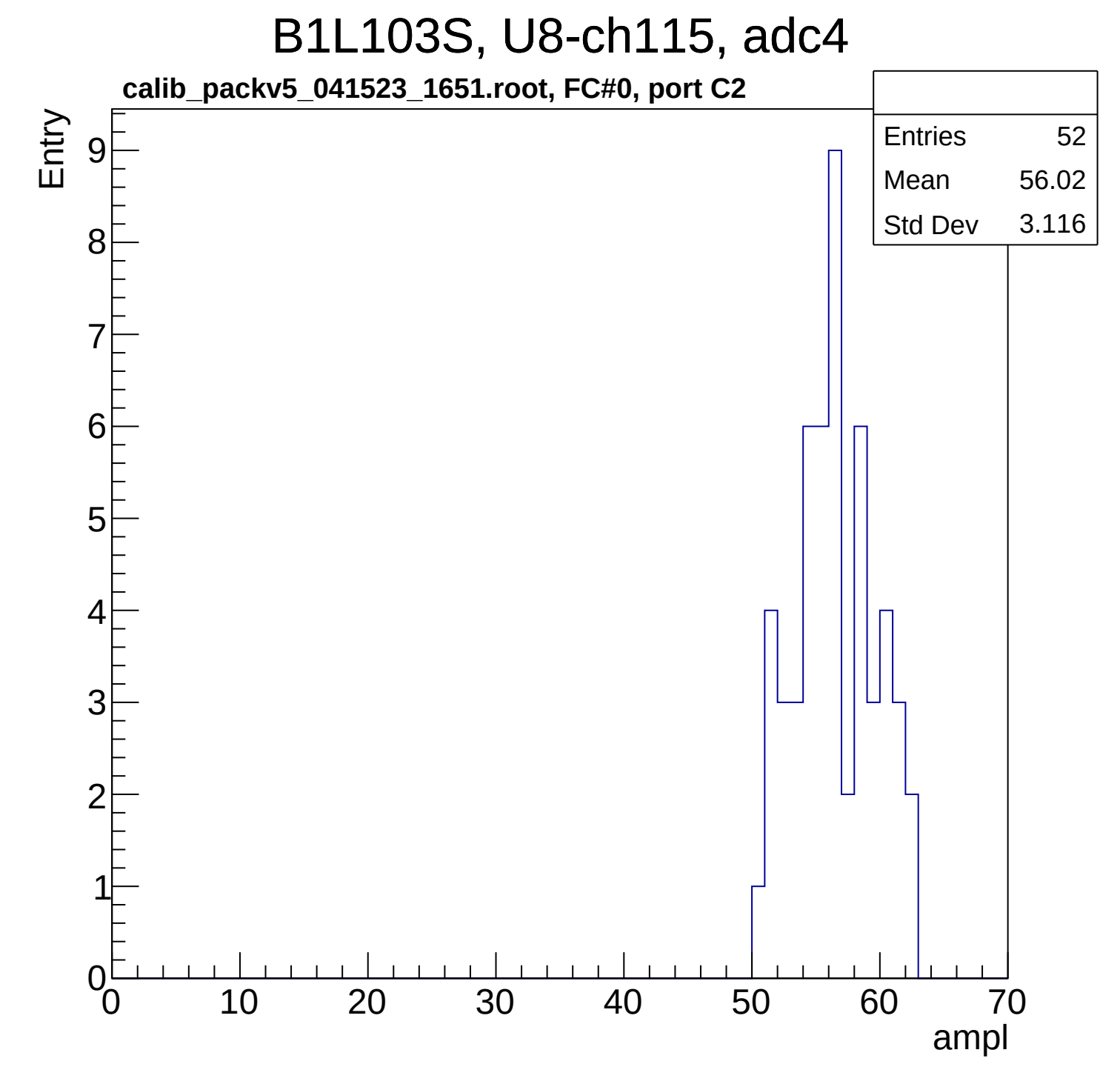
B1L103S, U8-ch115, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 56.02
Std Dev 3.116
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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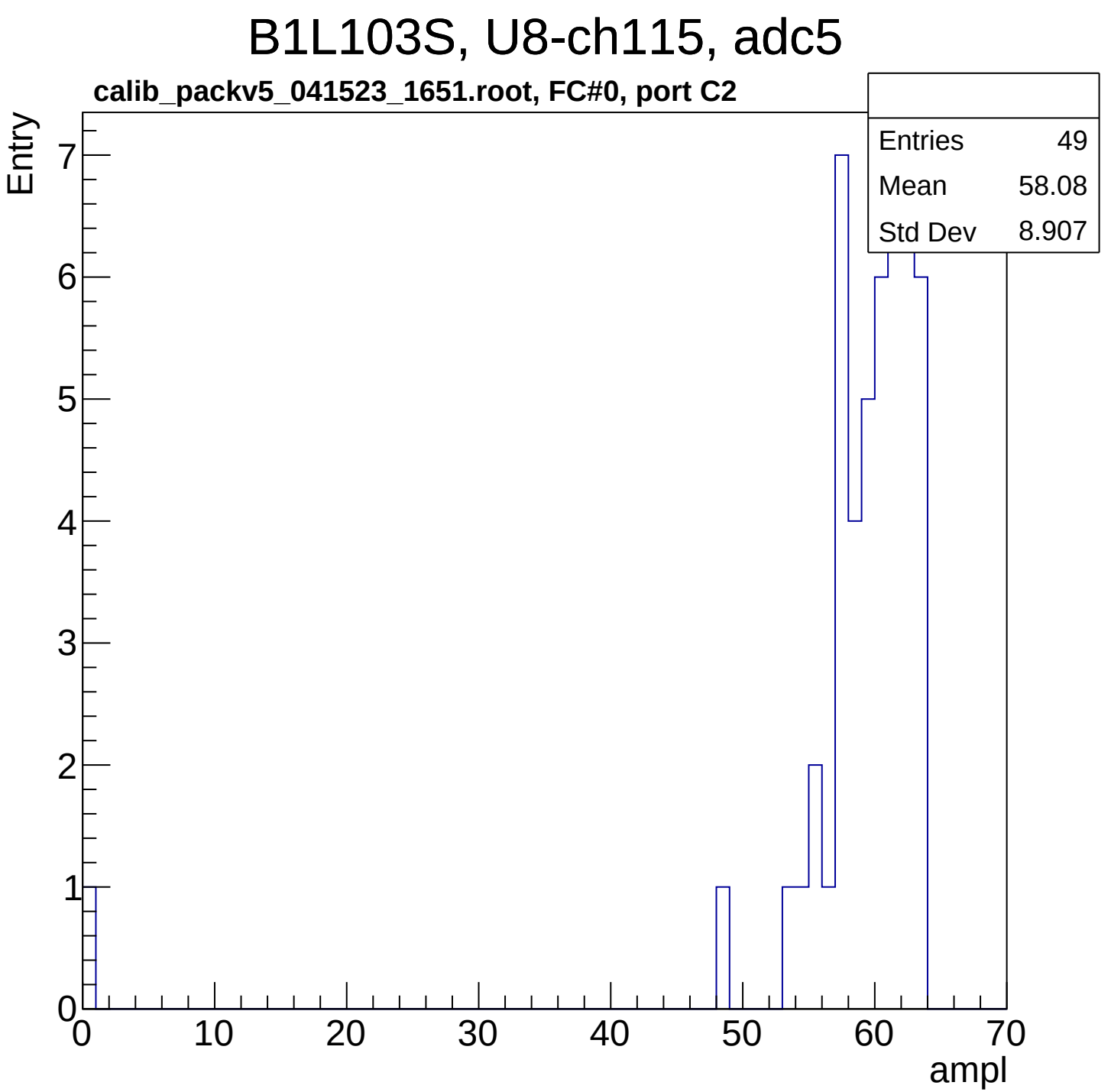
B1L103S, U8-ch115, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 58.08
Std Dev 8.907
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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40
50
60
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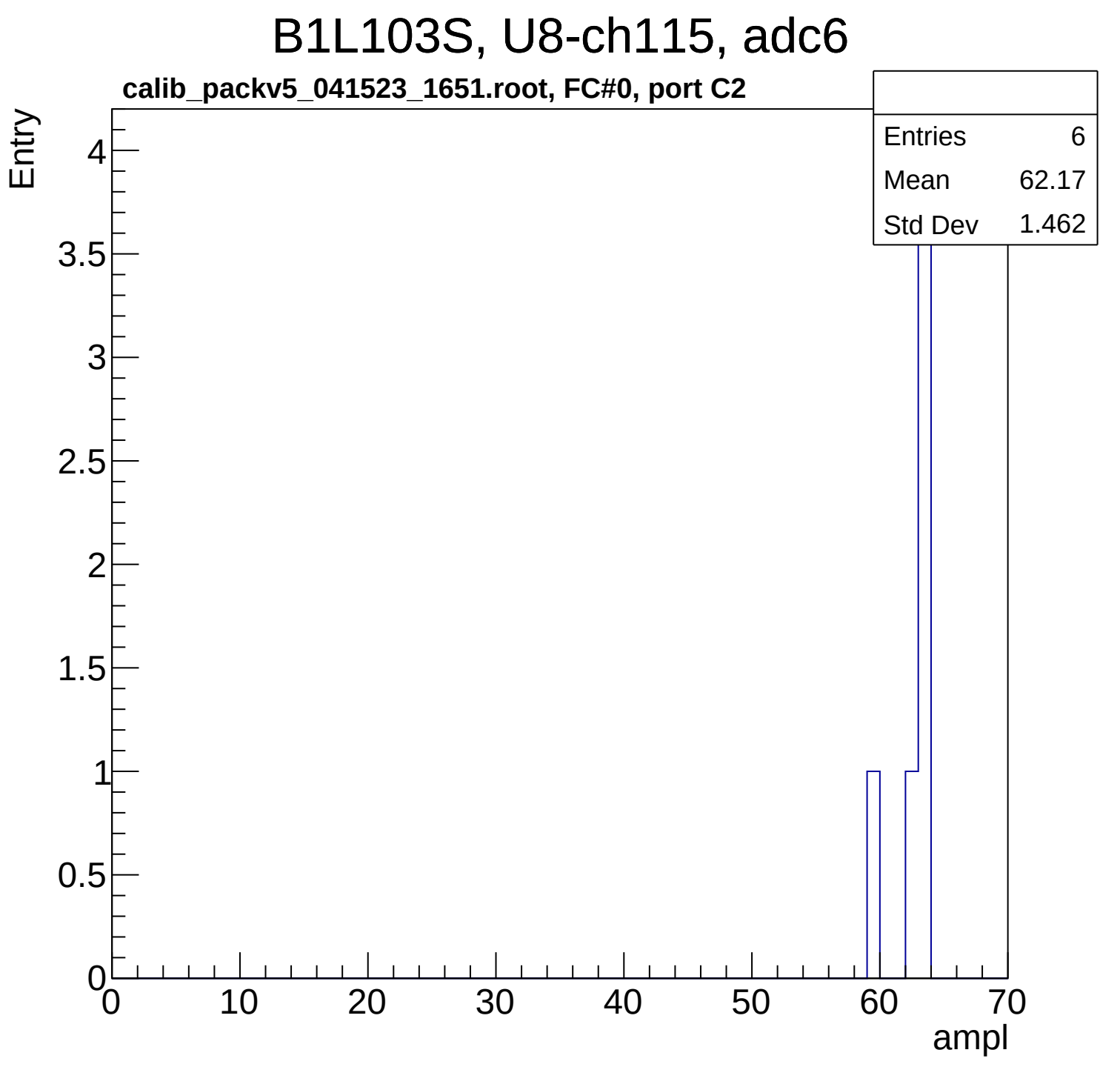
B1L103S, U8-ch115, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 62.17
Std Dev 1.462
Entry
ampl
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0.5
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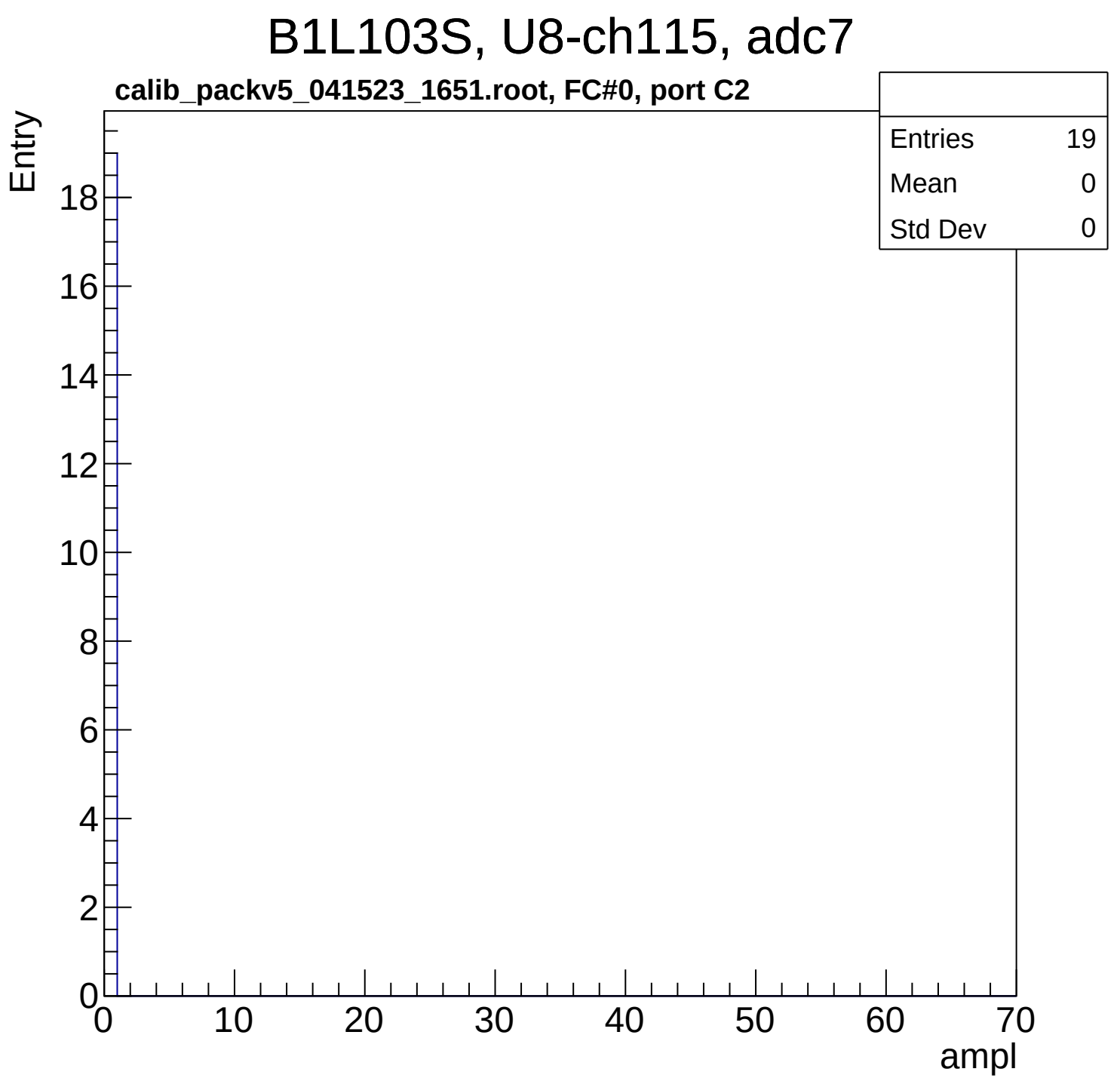
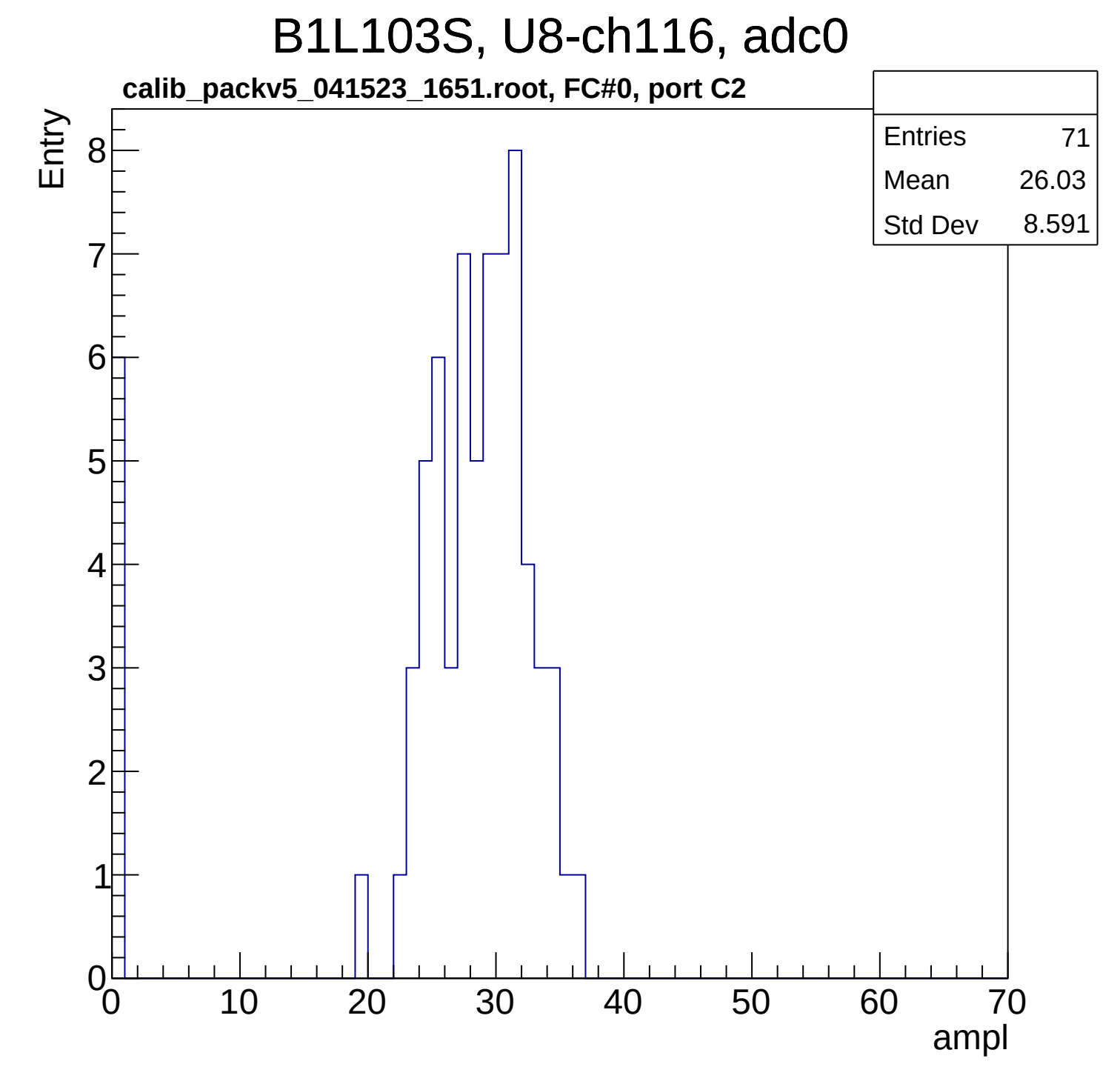
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U8-ch115, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch116, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 26.03
Std Dev 8.591
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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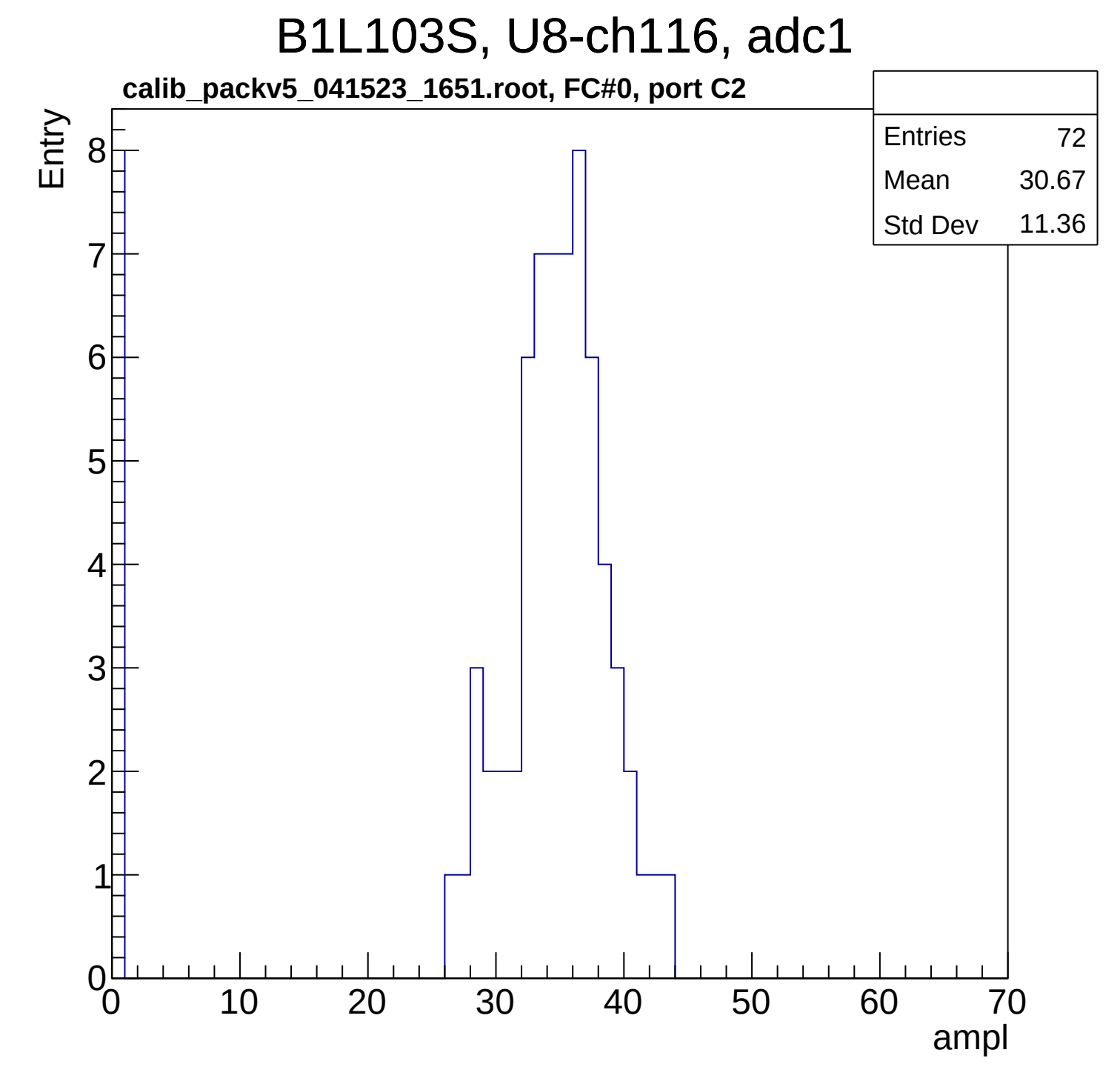
B1L103S, U8-ch116, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 30.67
Std Dev 11.36
Entry
ampl
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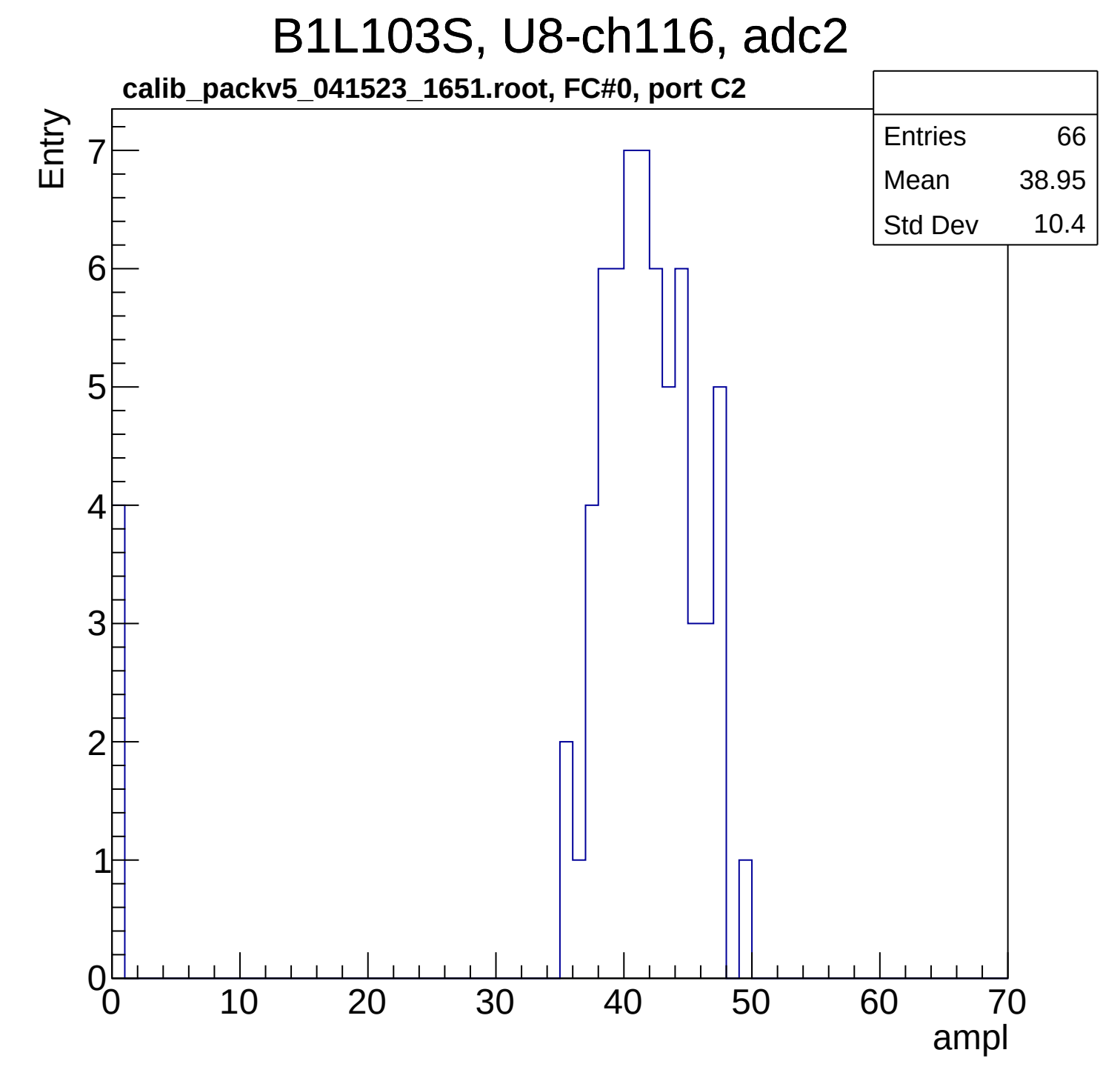
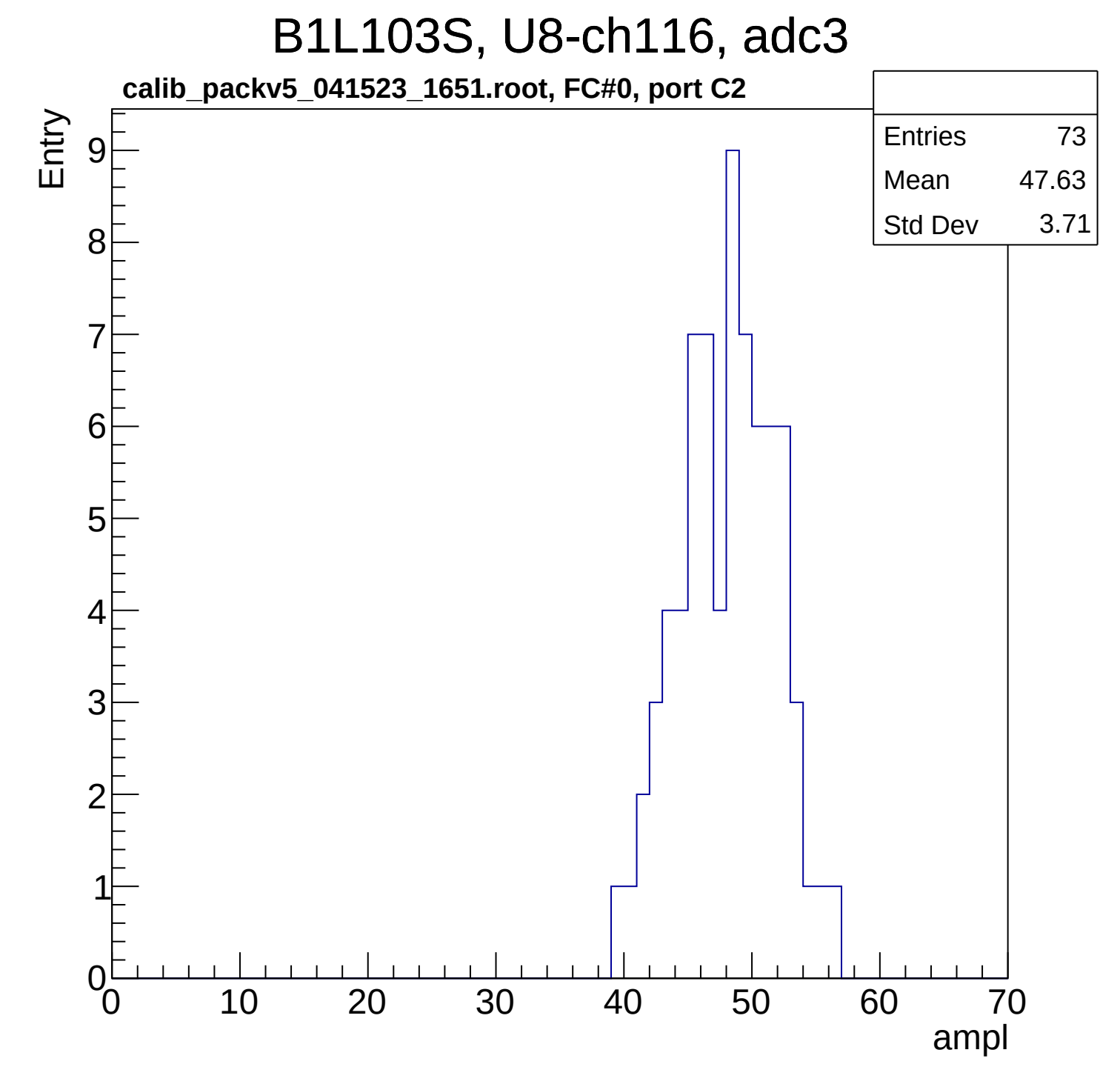
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch116, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 38.95
Std Dev 10.4
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U8-ch116, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 47.63
Std Dev 3.71
Entry
ampl
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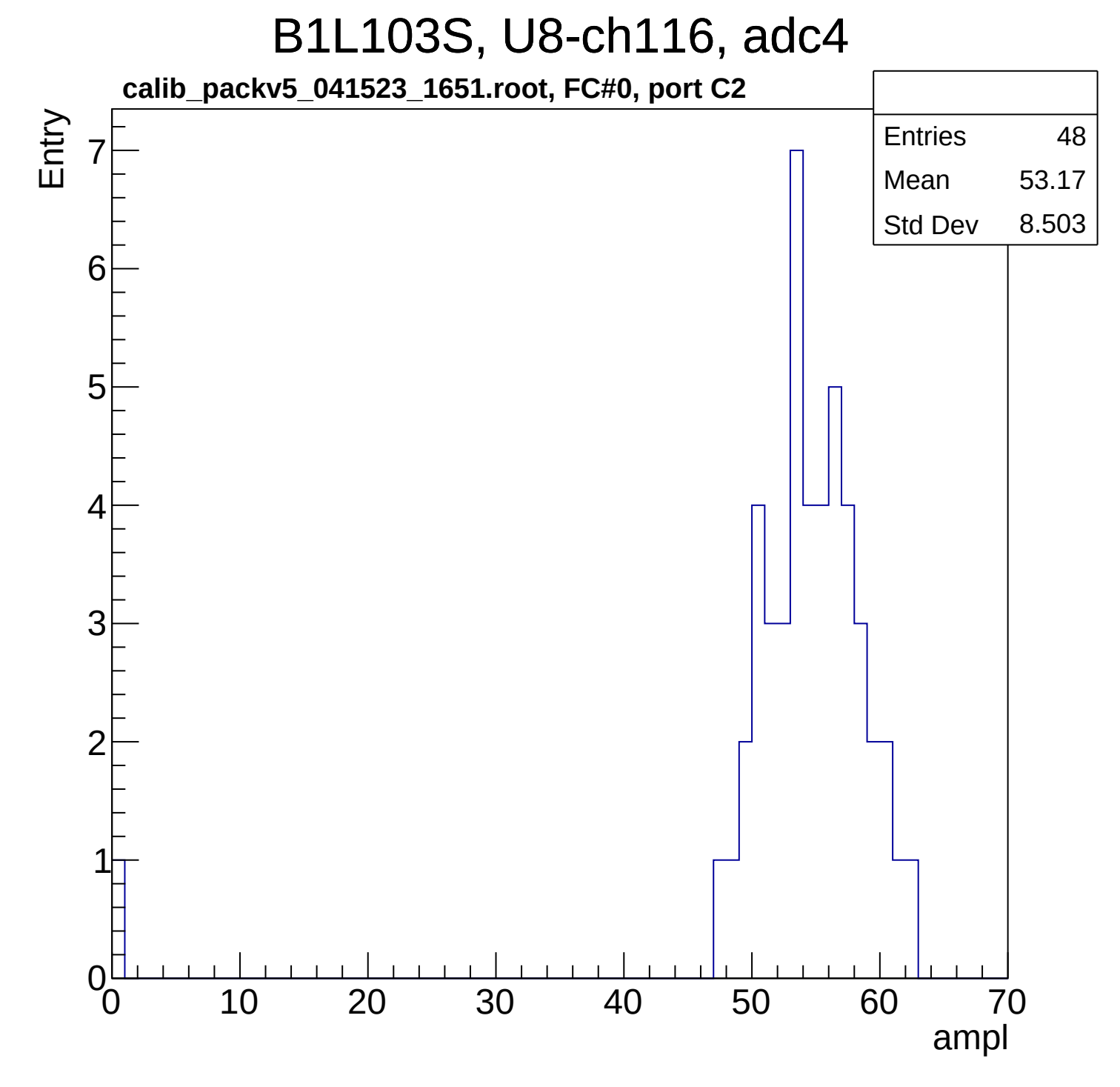
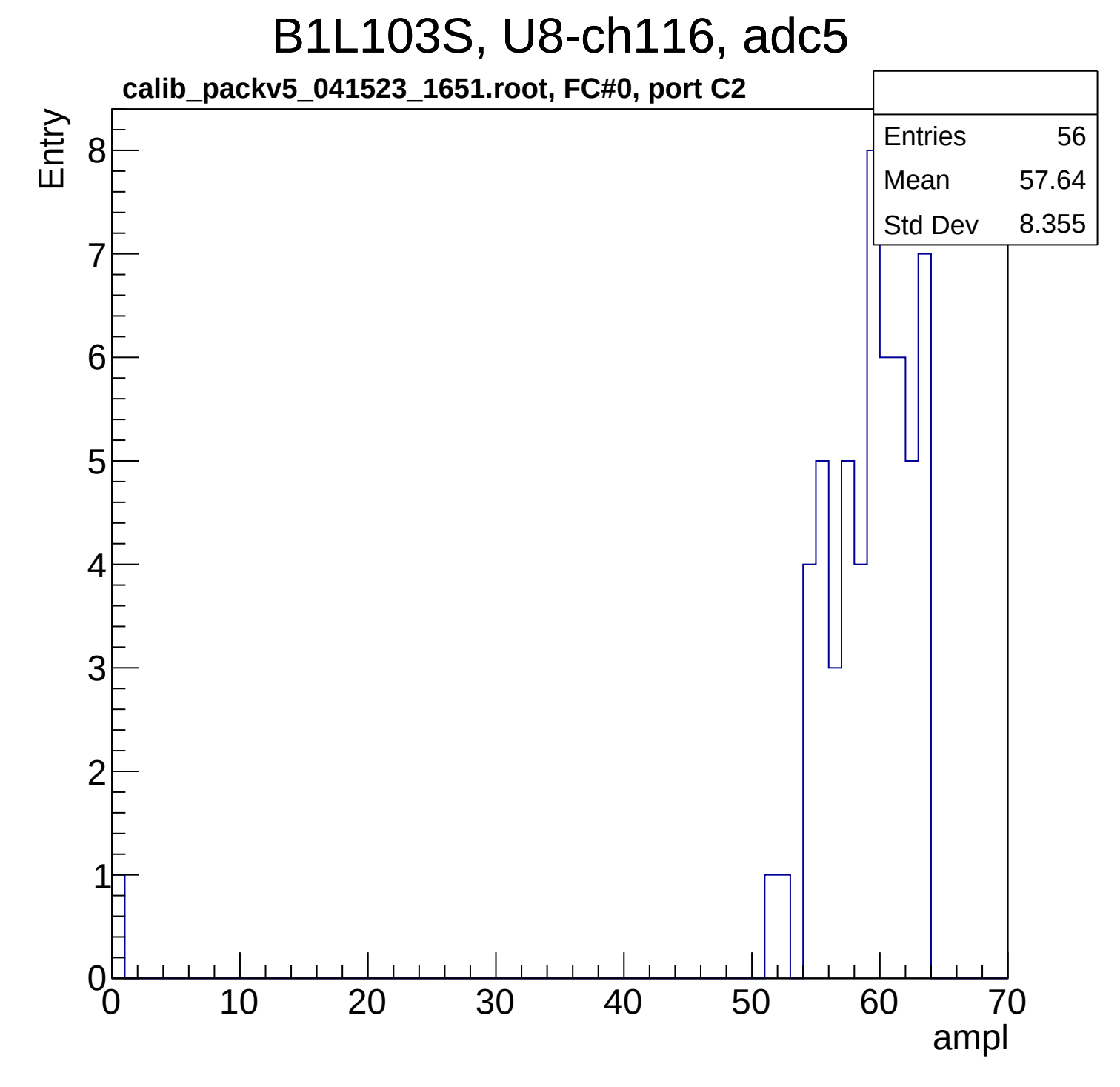
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U8-ch116, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 53.17
Std Dev 8.503
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U8-ch116, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 57.64
Std Dev 8.355
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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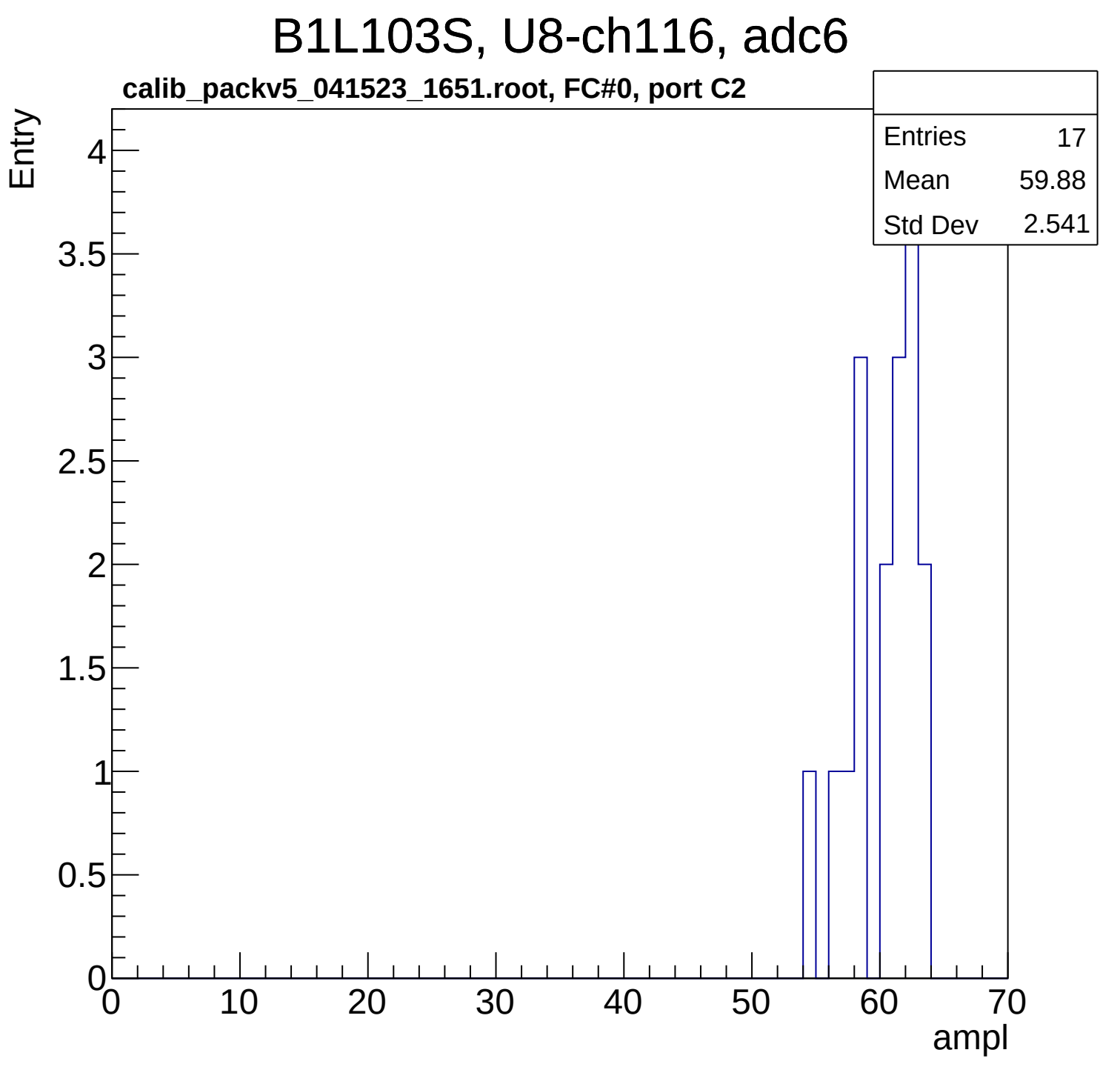
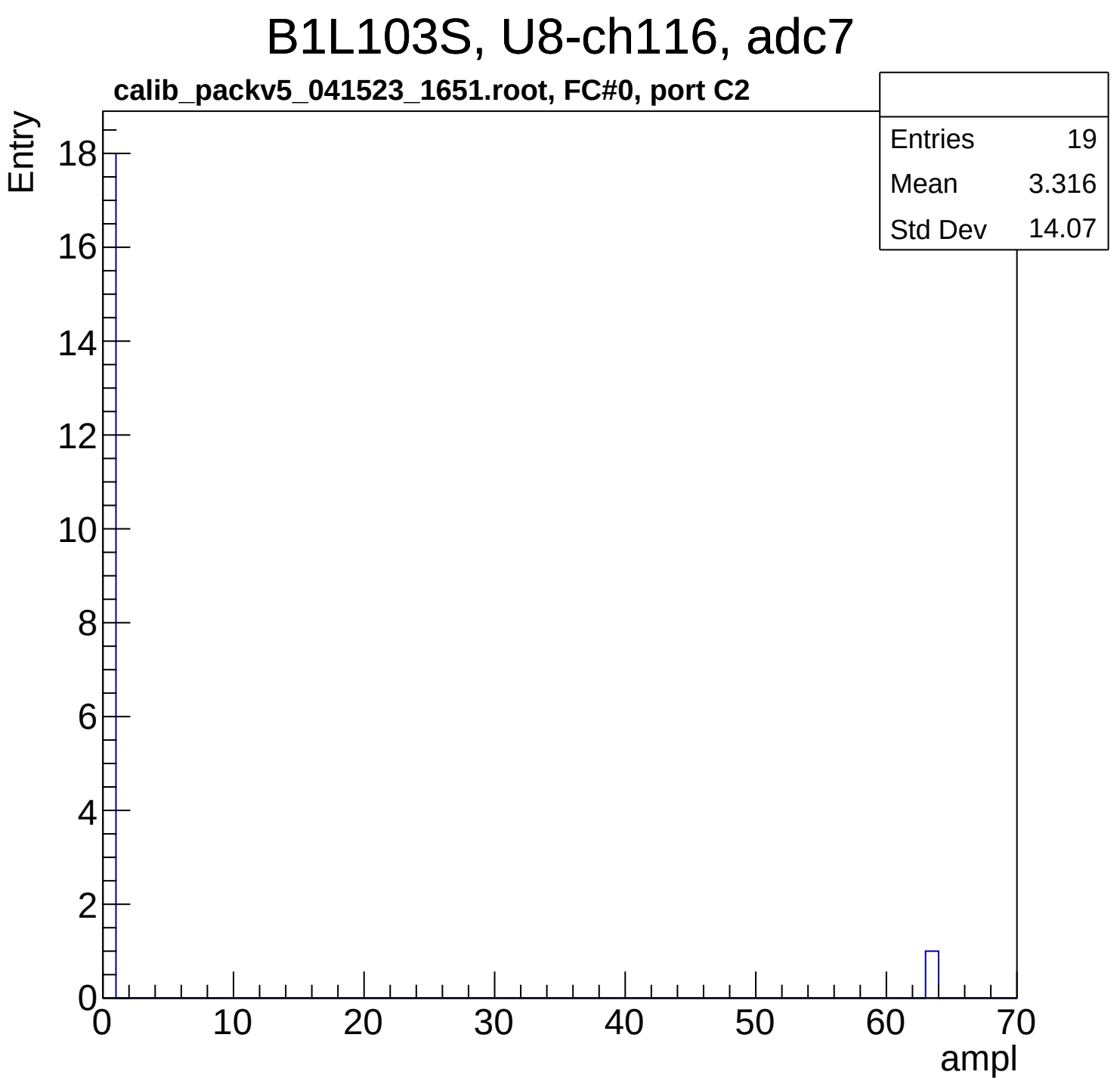
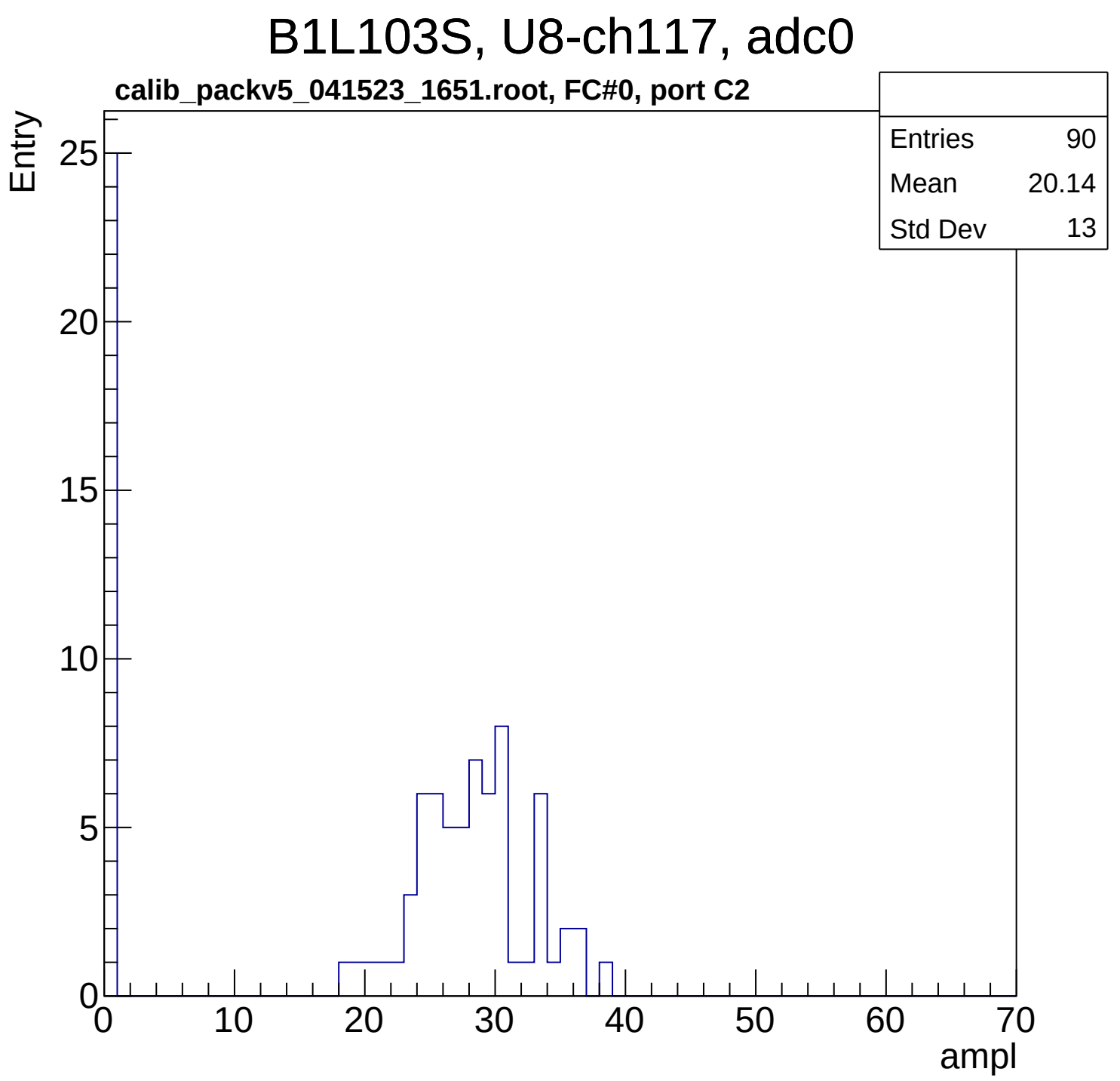
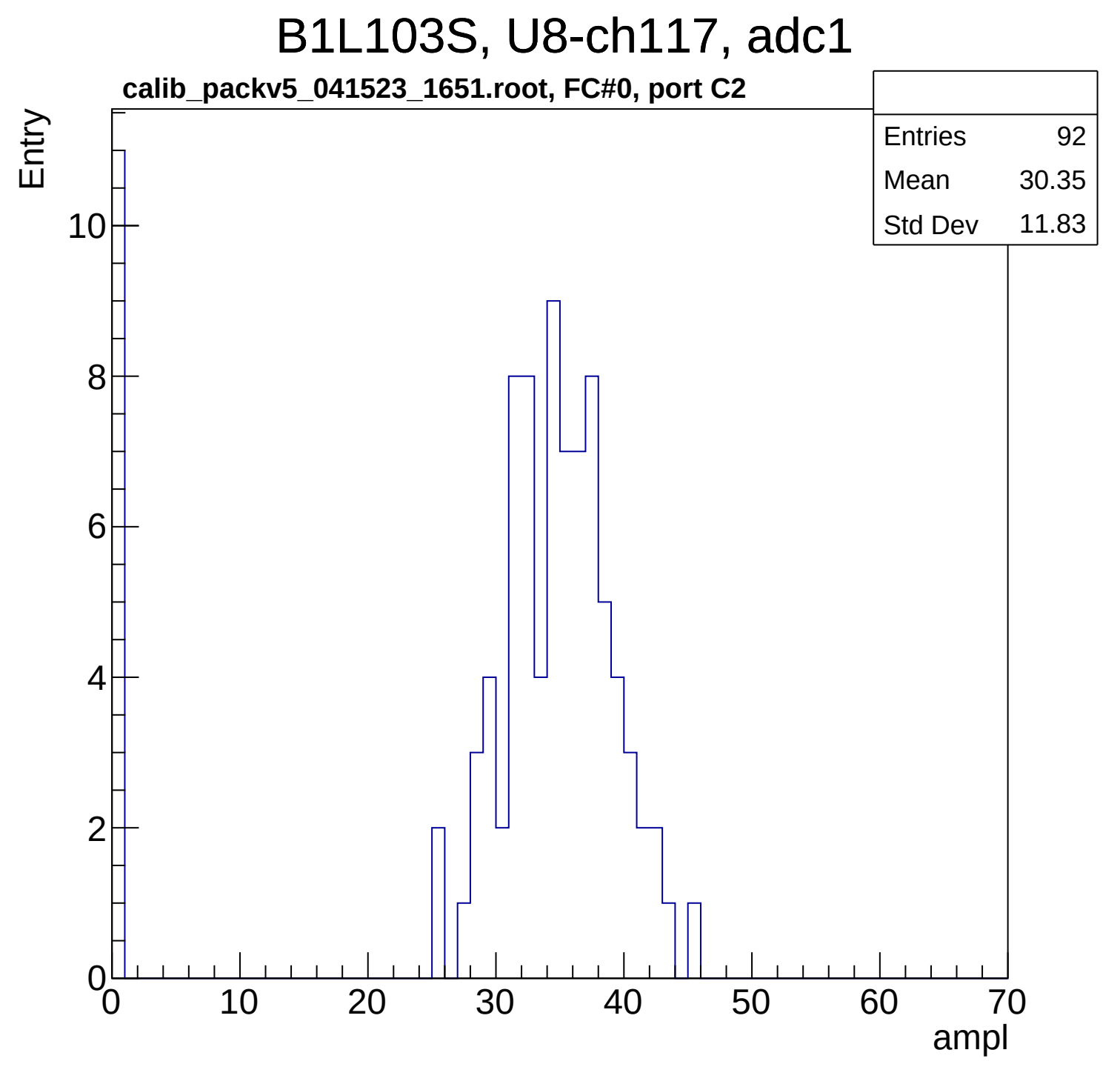
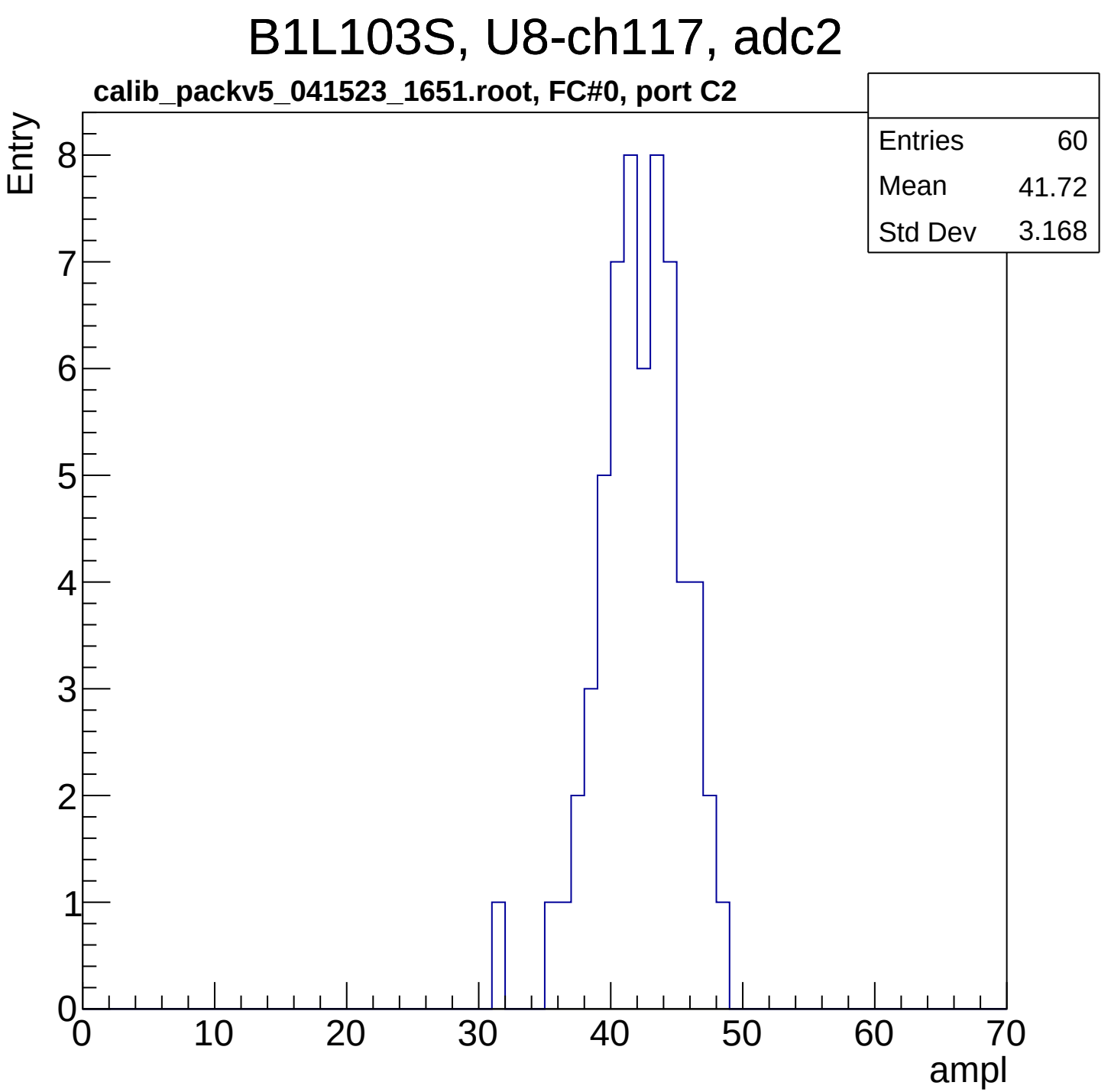

B1L103S, U8-ch116, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 59.88
Std Dev 2.541
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U8-ch116, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.316
Std Dev 14.07
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch117, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 20.14
Std Dev 13
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch117, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 30.35
Std Dev 11.83
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch117, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 41.72
Std Dev 3.168
Entry
ampl
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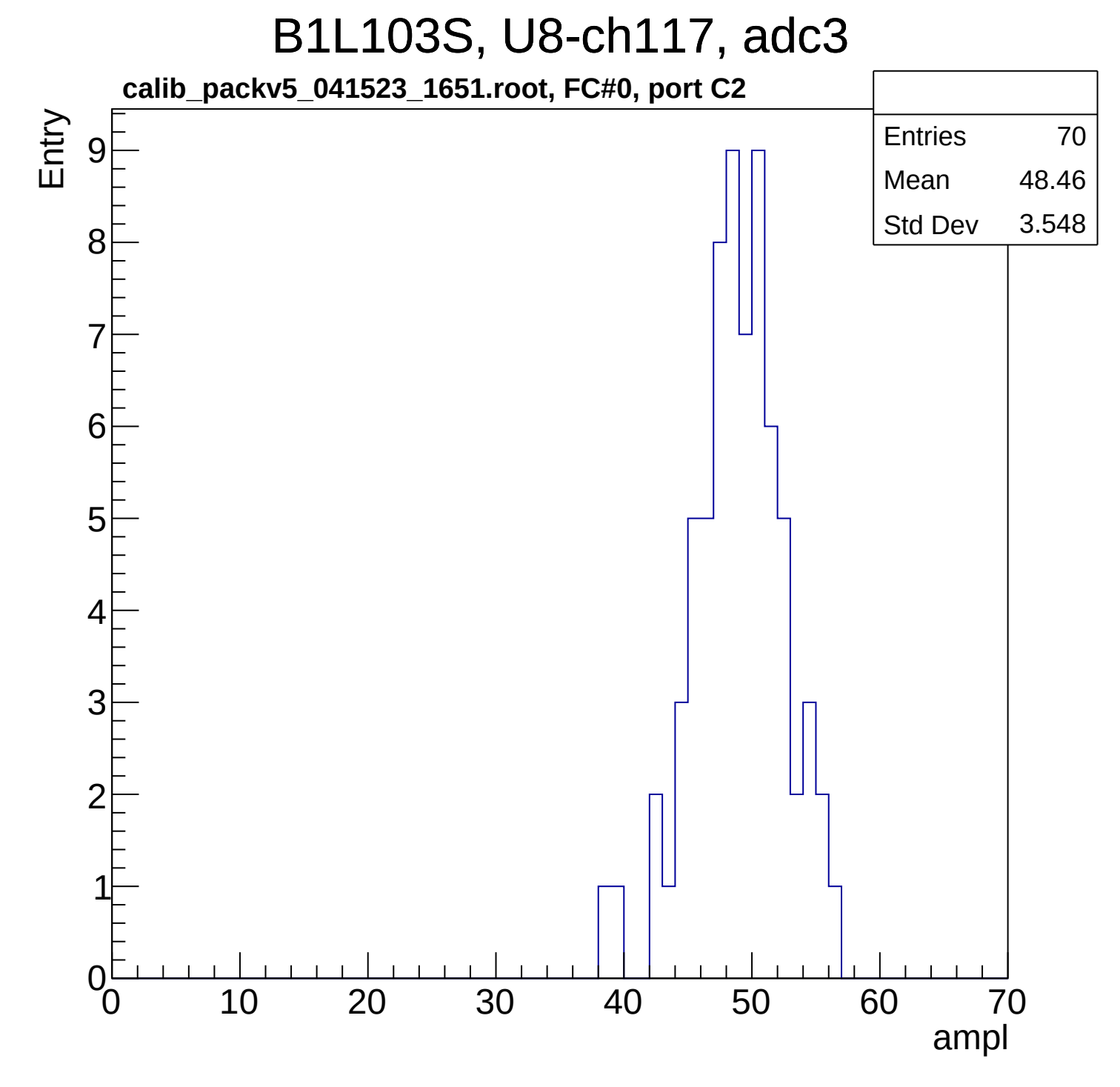
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch117, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 48.46
Std Dev 3.548
Entry
ampl
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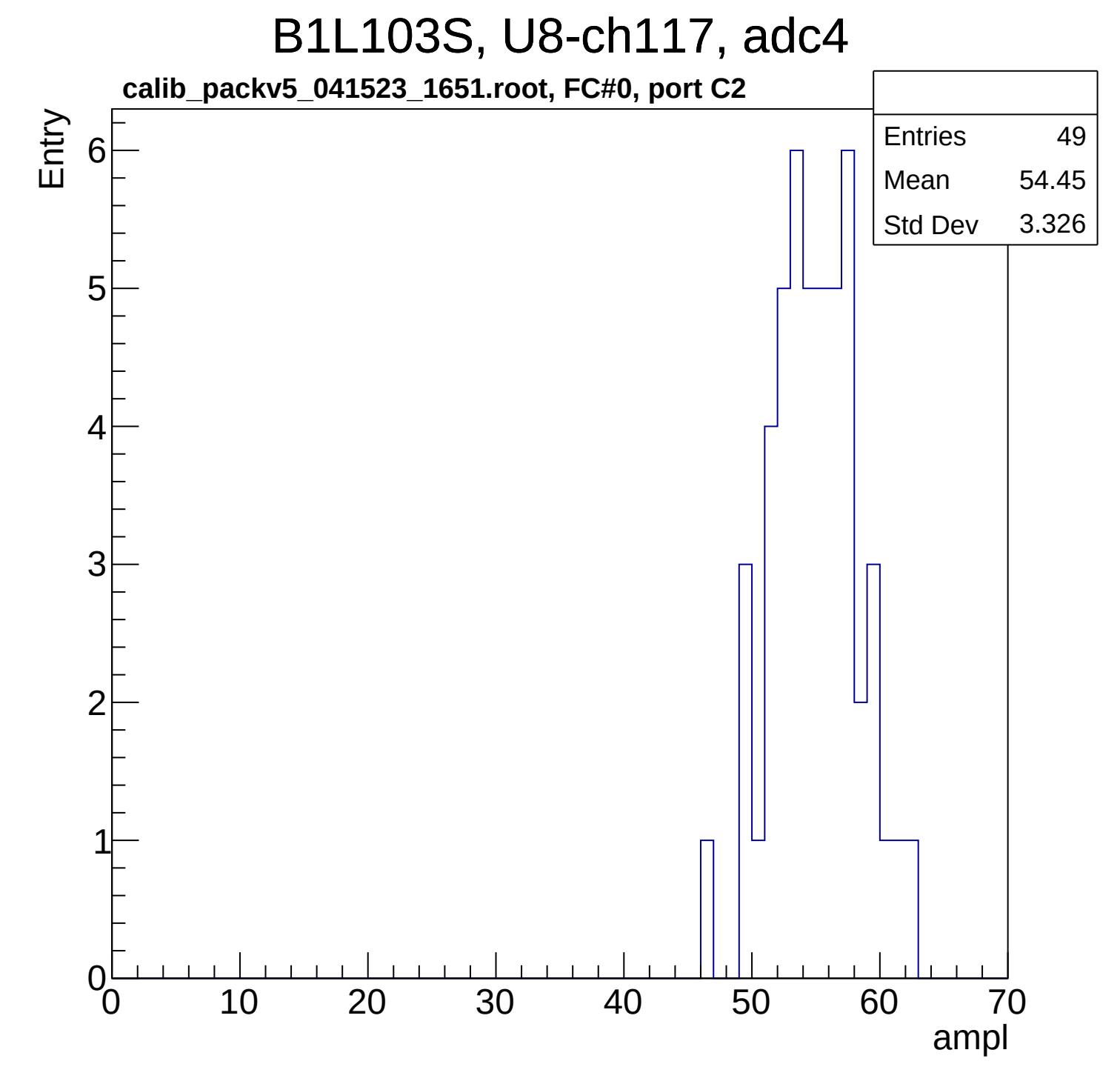
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U8-ch117, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 54.45
Std Dev 3.326
Entry
ampl
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2
3
4
5
6
0
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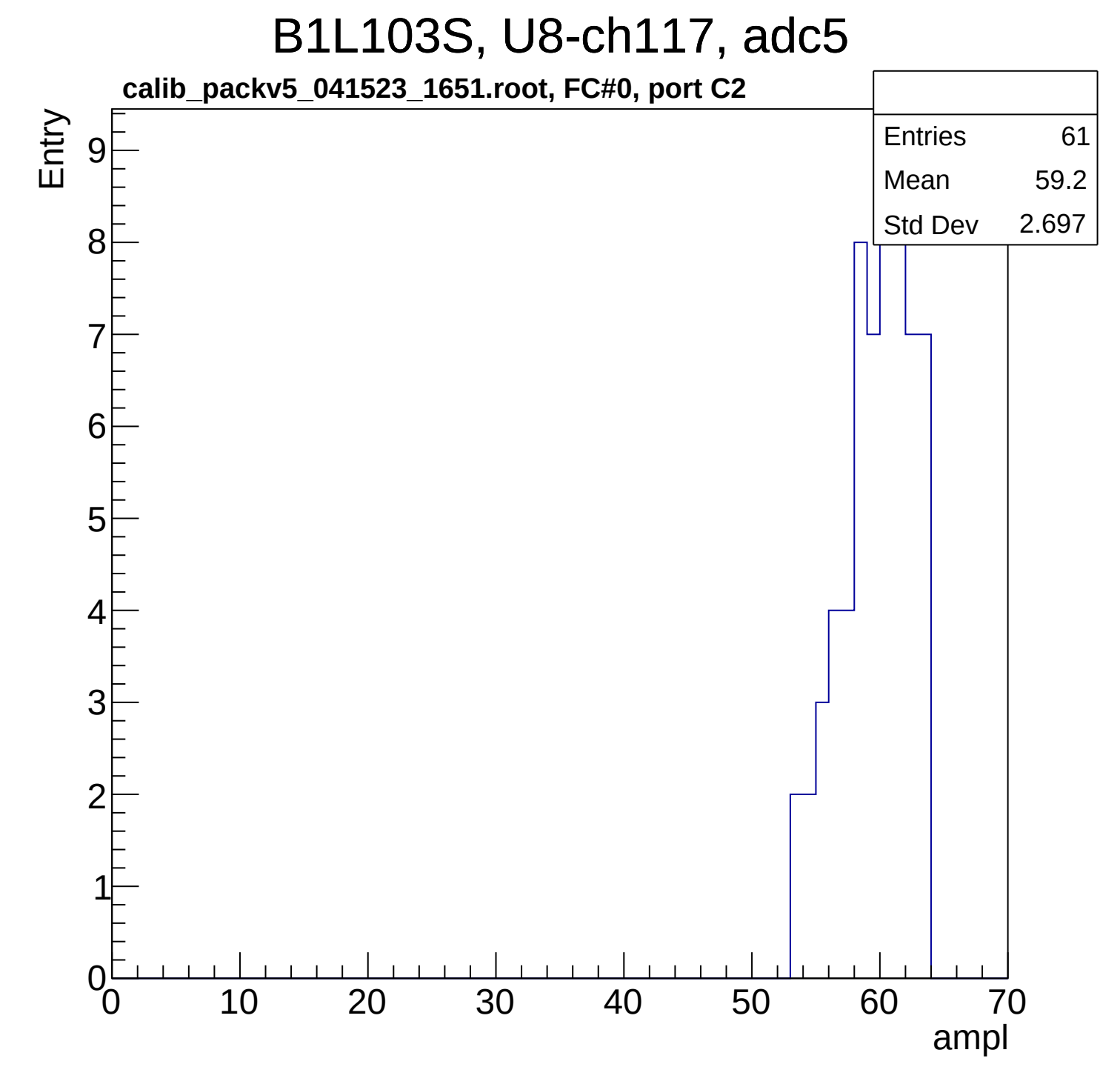
20
30
40
50
60
70


B1L103S, U8-ch117, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 59.2
Std Dev 2.697
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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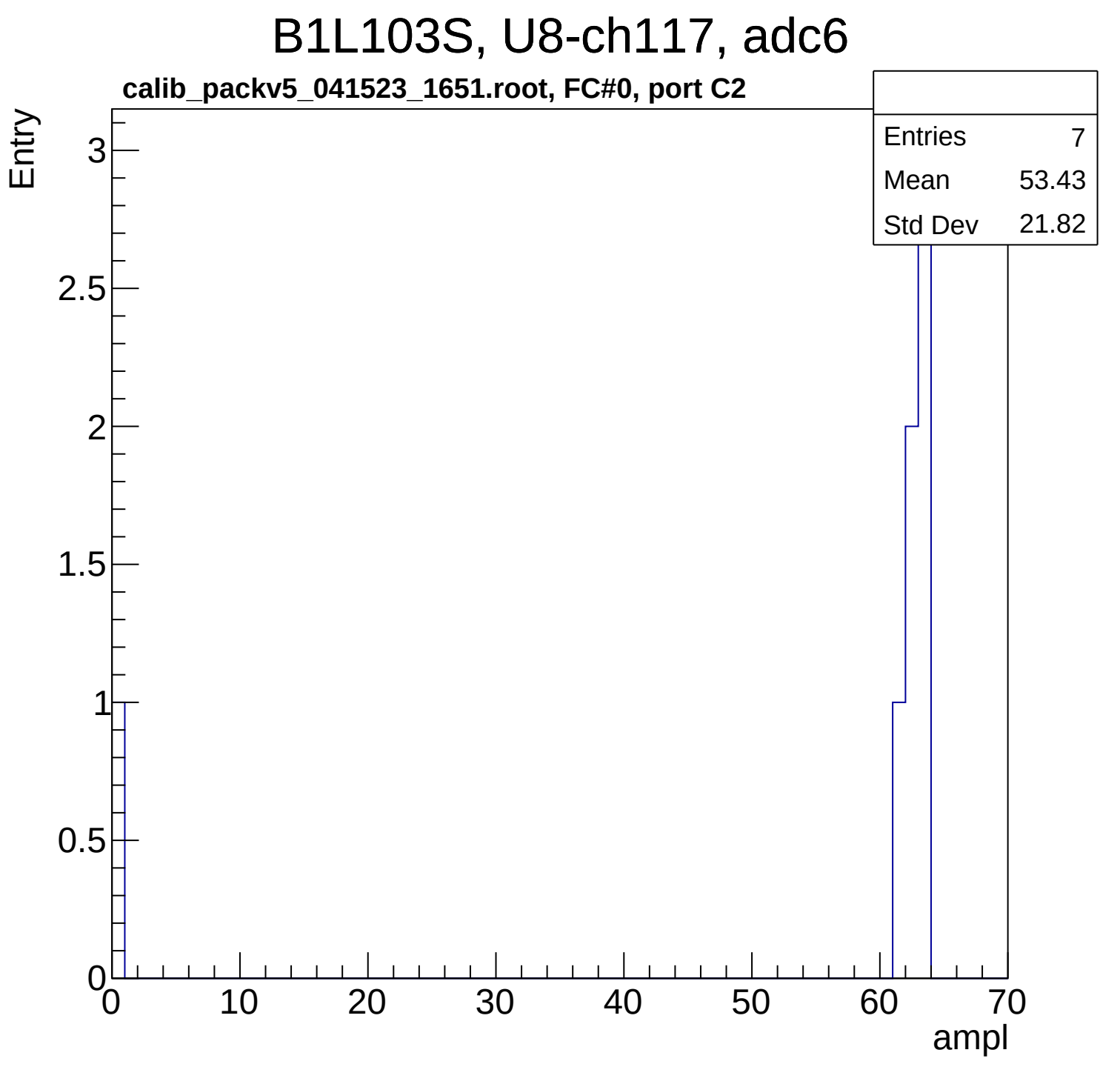
60
70


B1L103S, U8-ch117, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 53.43
Std Dev 21.82
Entry
ampl
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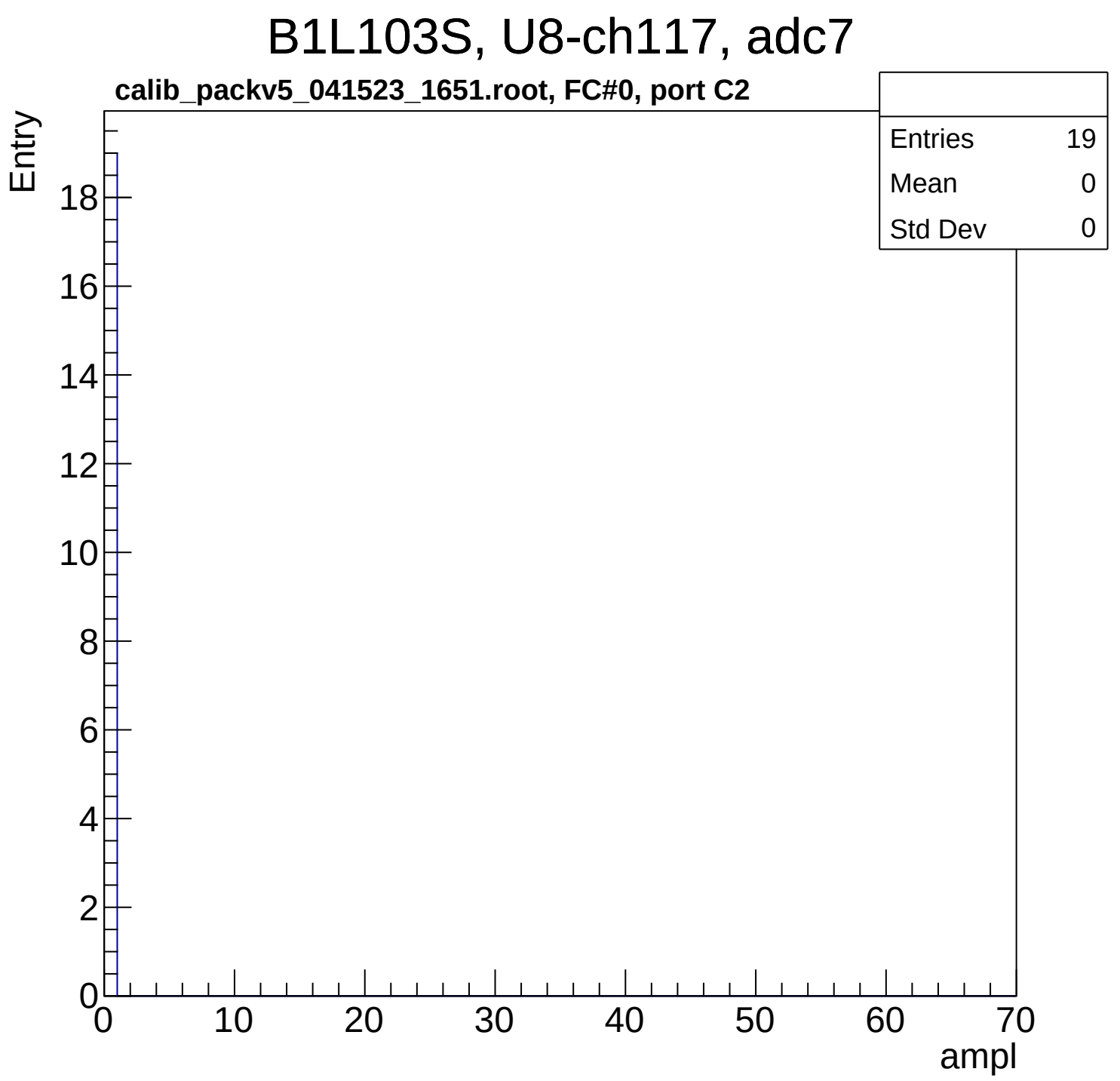
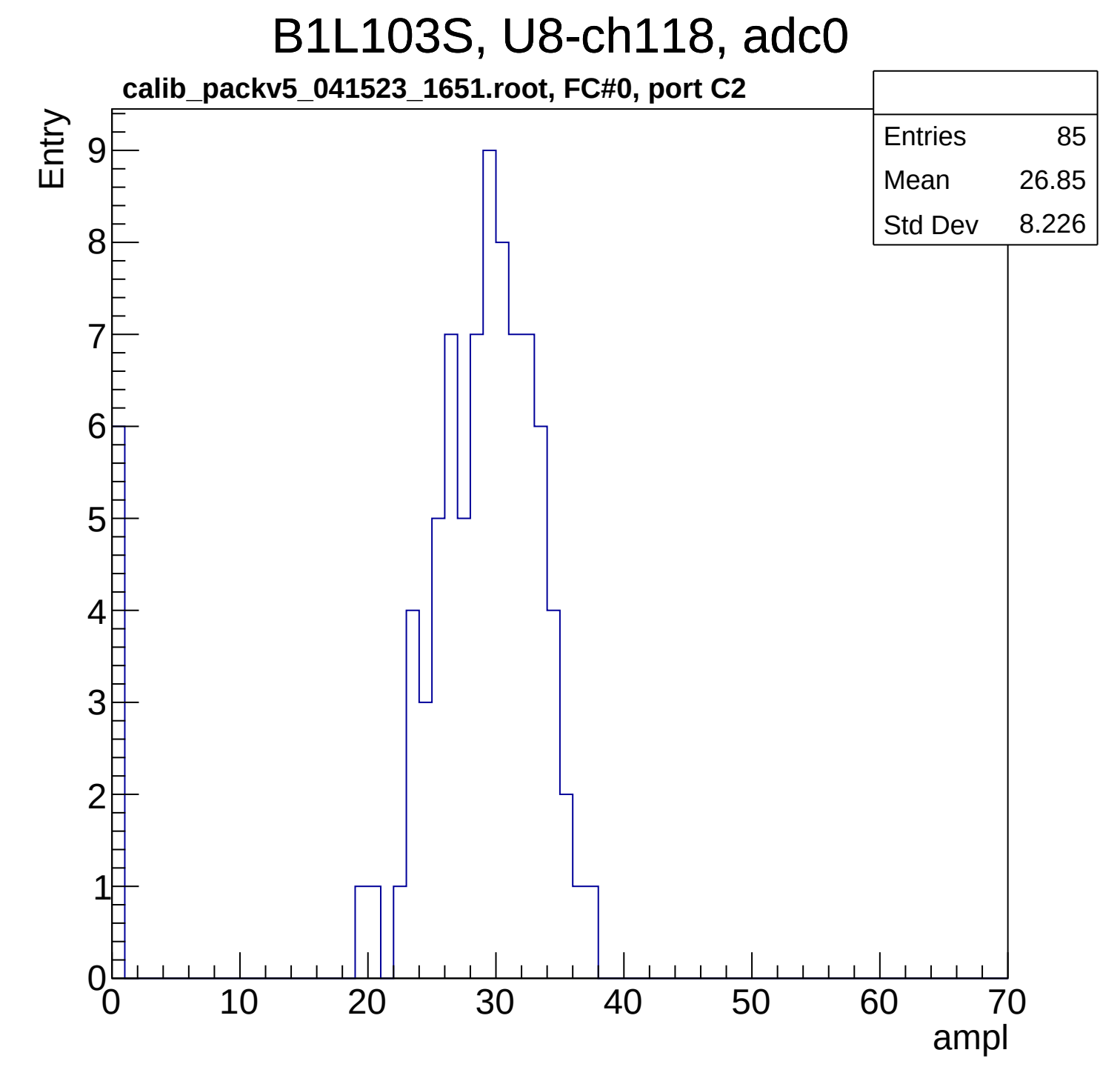
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U8-ch117, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch118, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 26.85
Std Dev 8.226
Entry
ampl
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2
3
4
5
6
7
8
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0
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20
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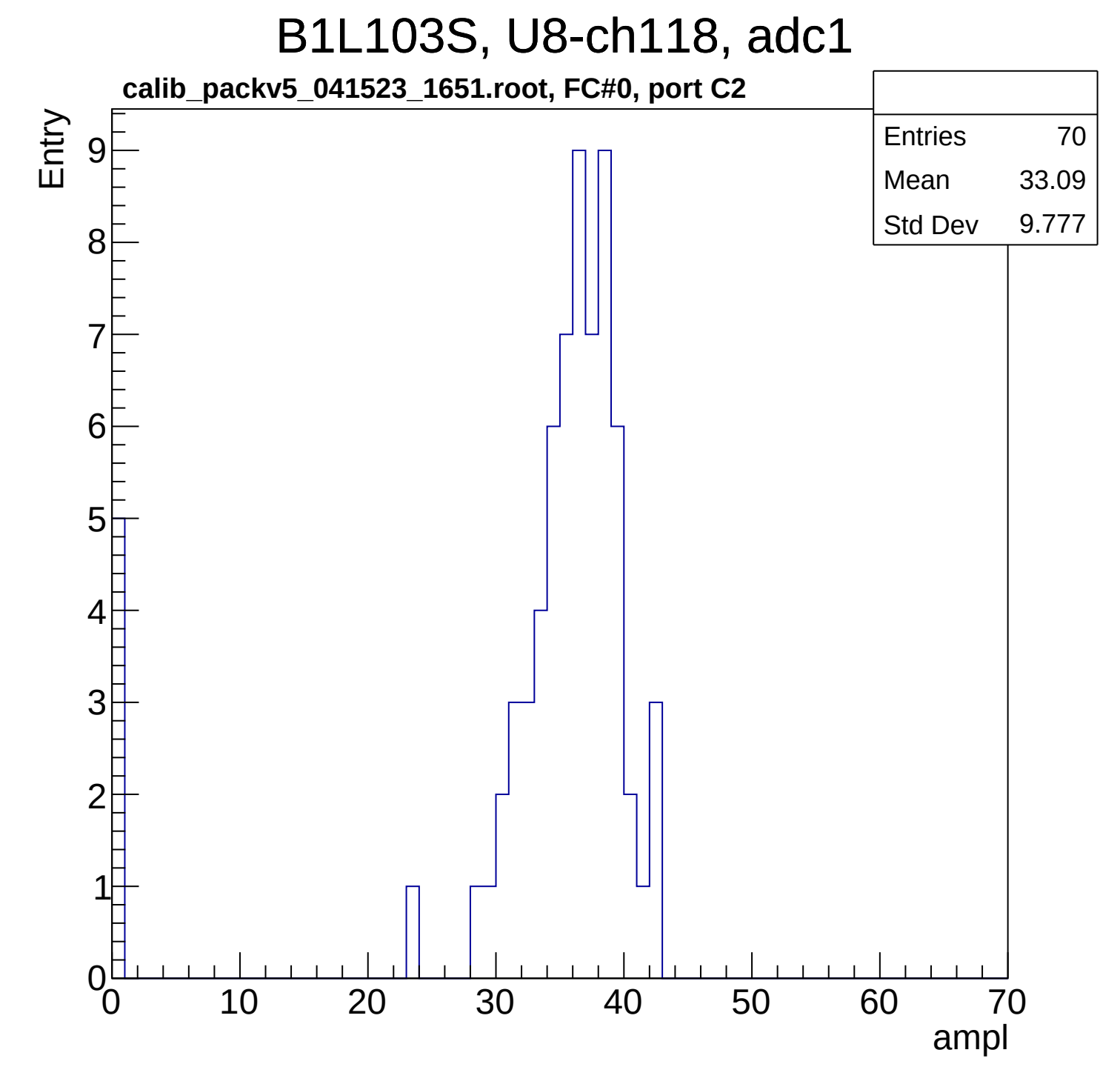
40
50
60
70


B1L103S, U8-ch118, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 33.09
Std Dev 9.777
Entry
ampl
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3
4
5
6
7
8
9
0
10
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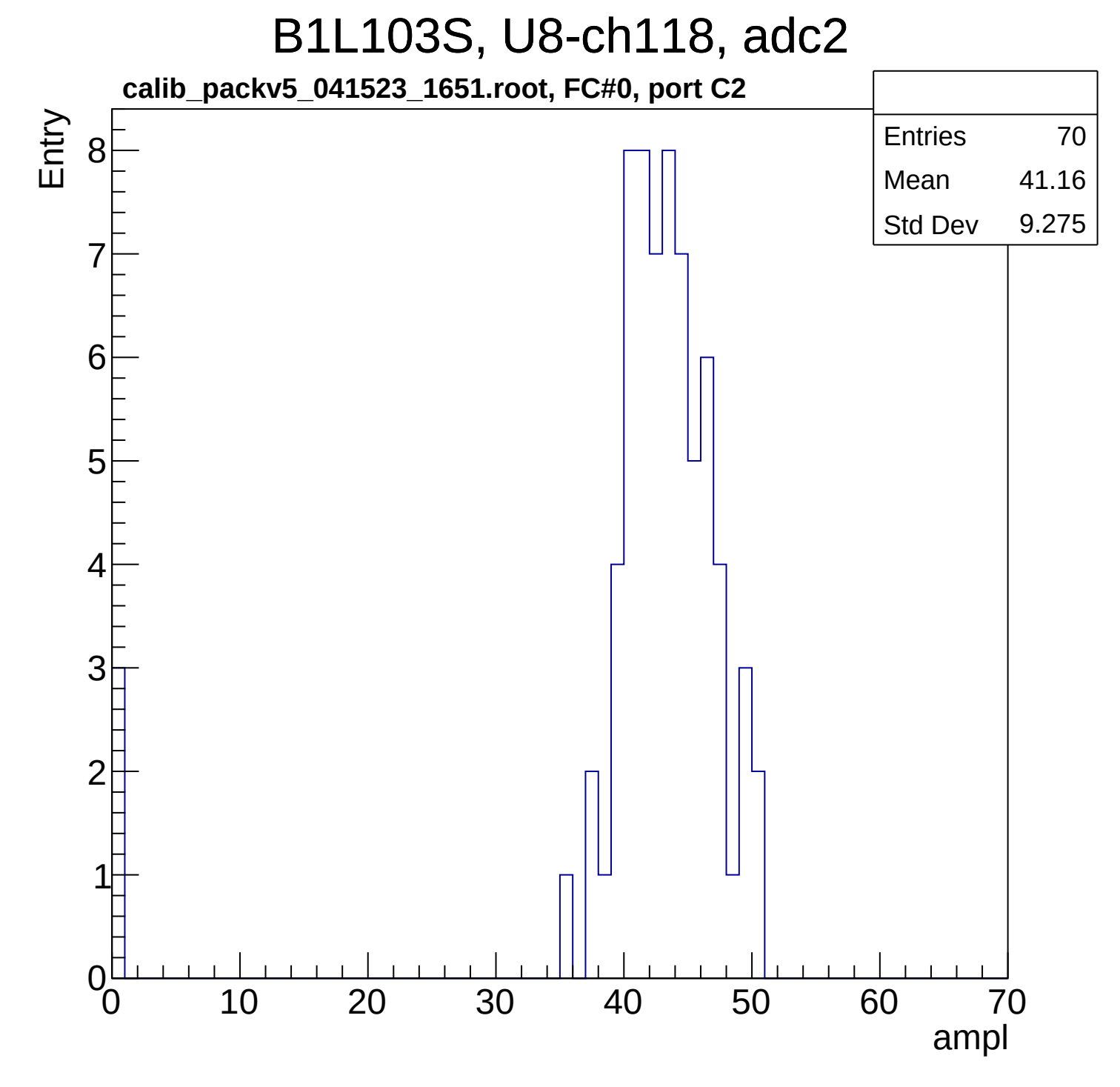
40
50
60
70


B1L103S, U8-ch118, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 41.16
Std Dev 9.275
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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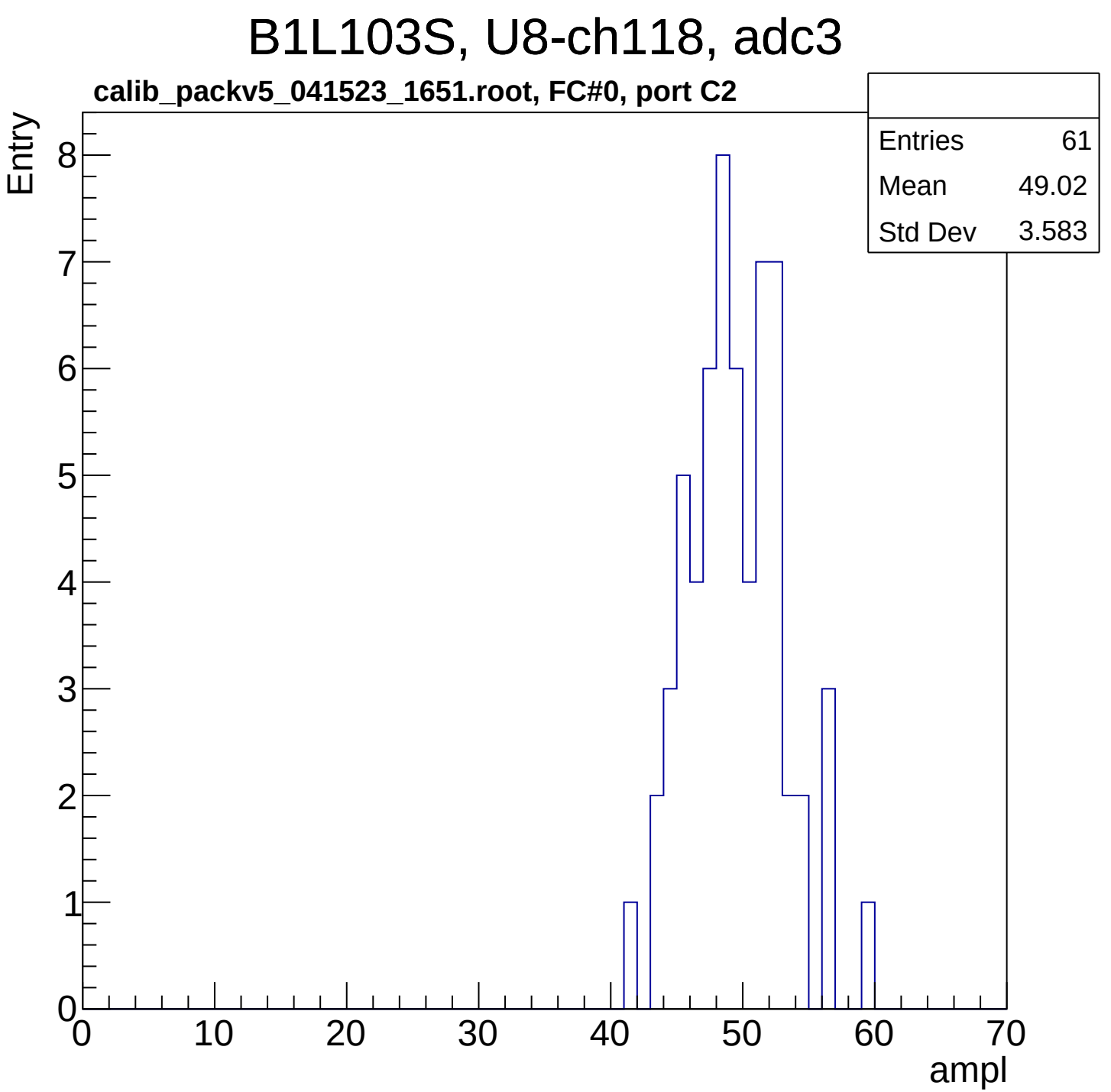
40
50
60
70


B1L103S, U8-ch118, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 49.02
Std Dev 3.583
Entry
ampl
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3
4
5
6
7
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0
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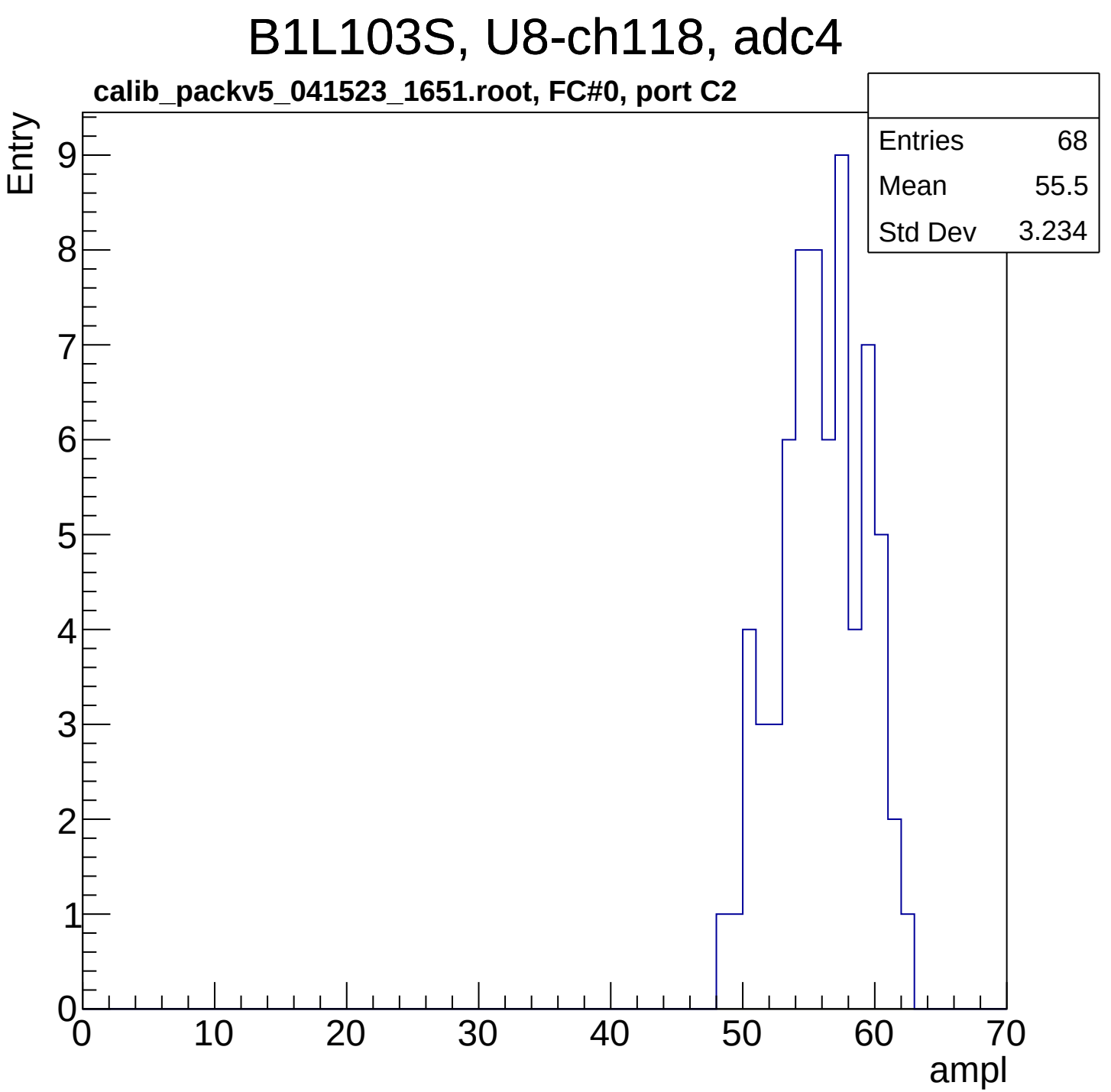
40
50
60
70


B1L103S, U8-ch118, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 55.5
Std Dev 3.234
Entry
ampl
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3
4
5
6
7
8
9
0
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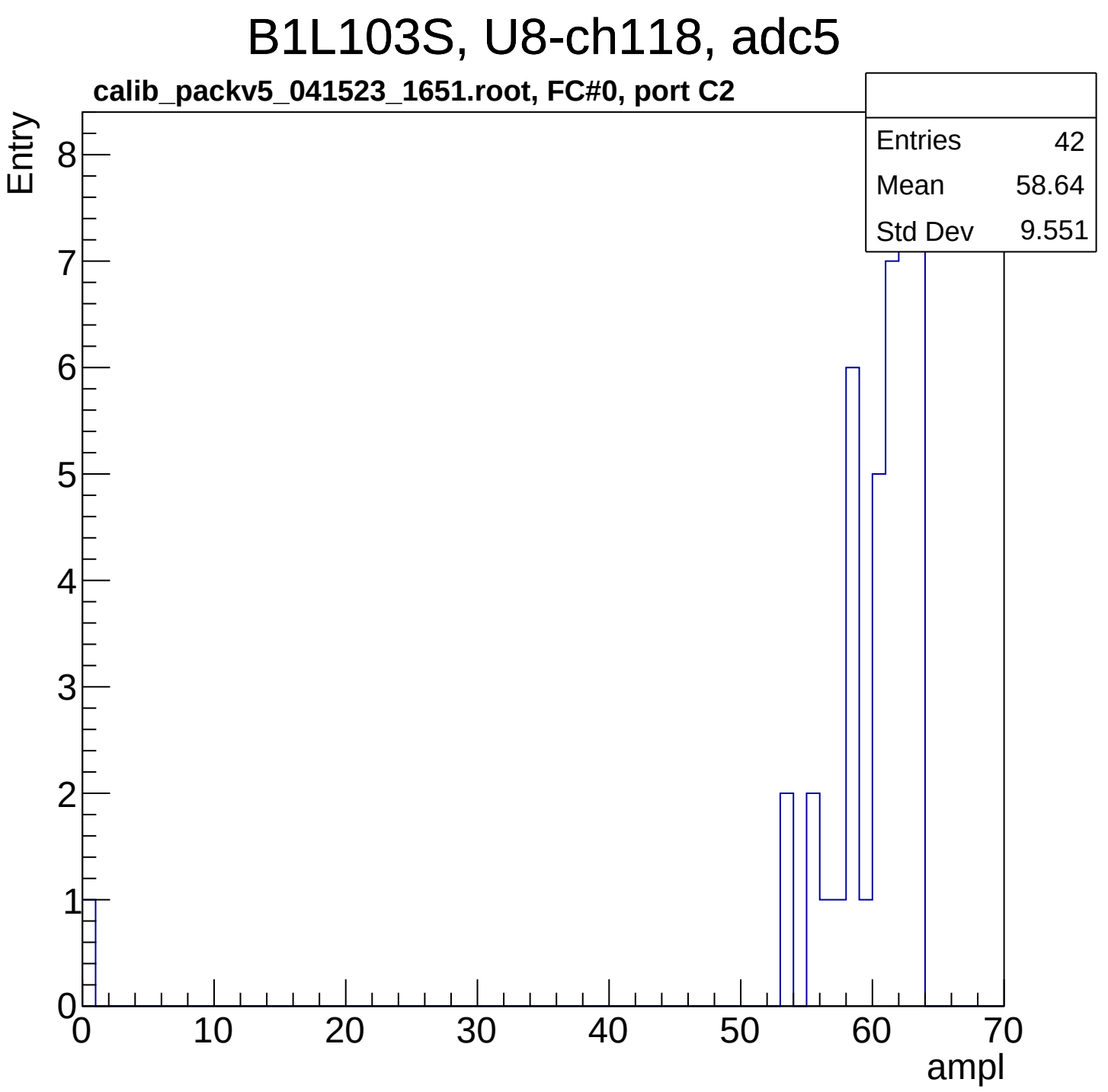
20
30
40
50
60
70


B1L103S, U8-ch118, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 58.64
Std Dev 9.551
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
50
60
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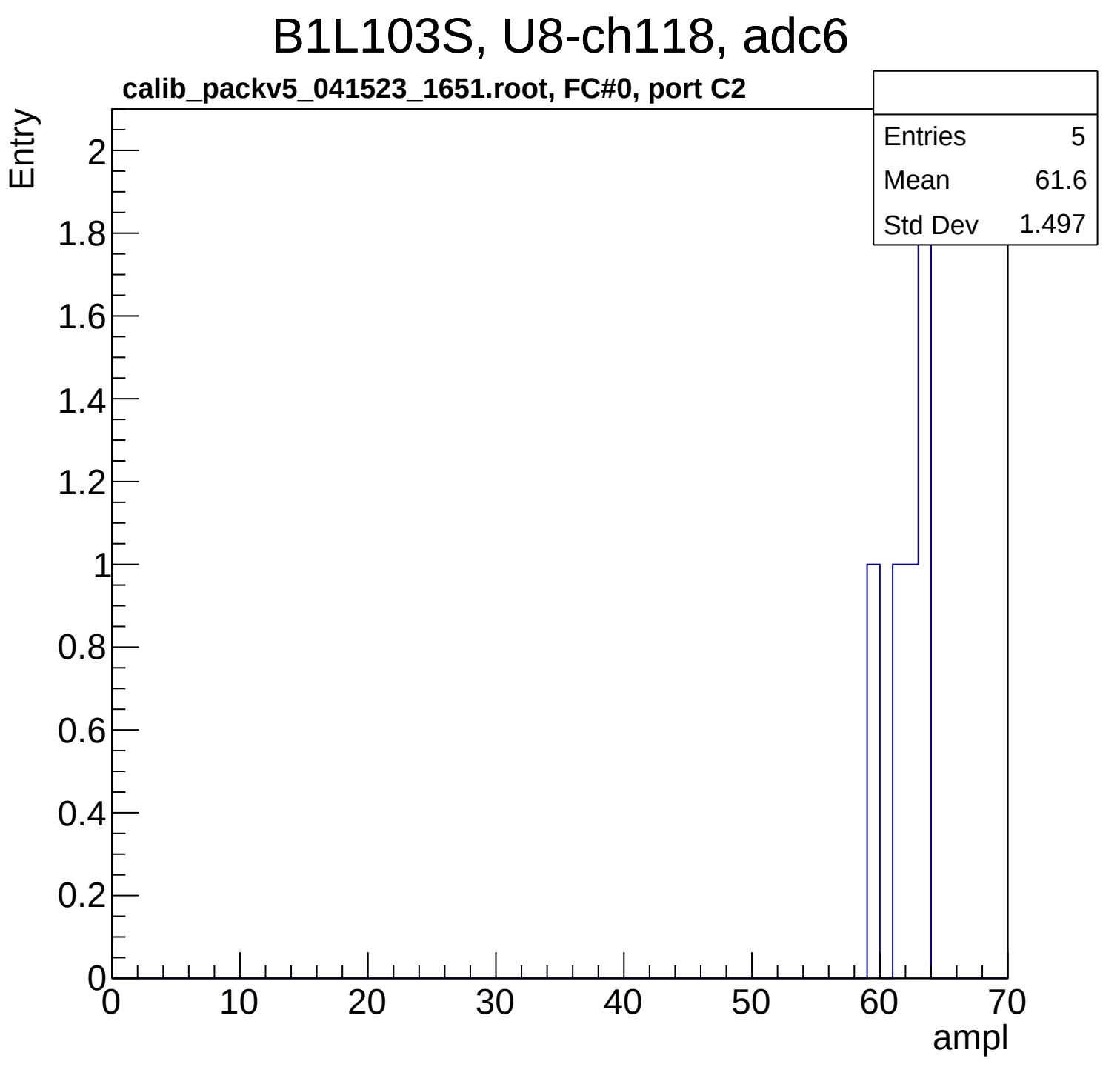
B1L103S, U8-ch118, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 61.6
Std Dev 1.497
Entry
ampl
0
0.2
0.4
0.6
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1
1.2
1.4
1.6
1.8
2
0
10
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40
50
60
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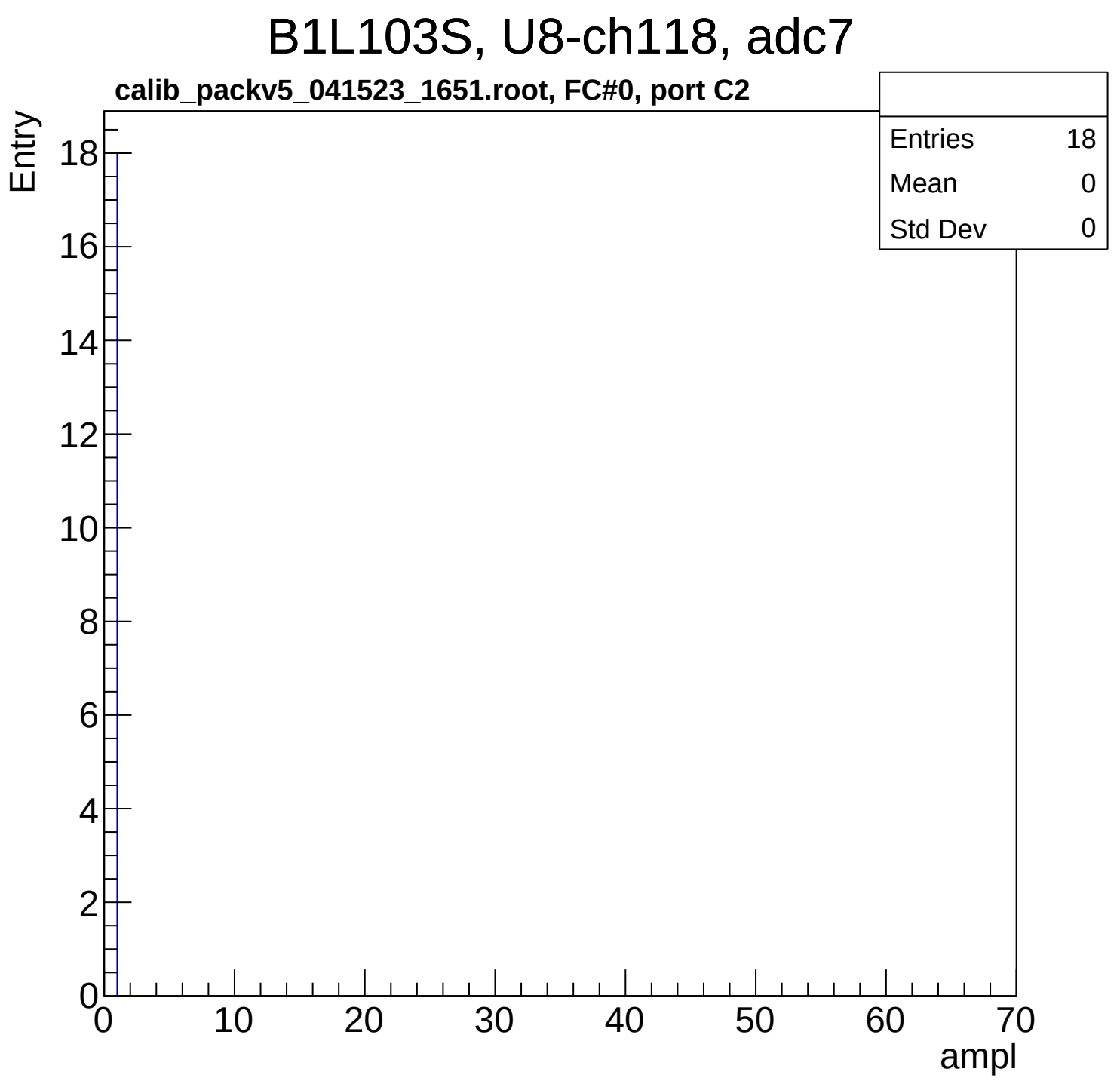
B1L103S, U8-ch118, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
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6
8
10
12
14
16
18
0
10
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30
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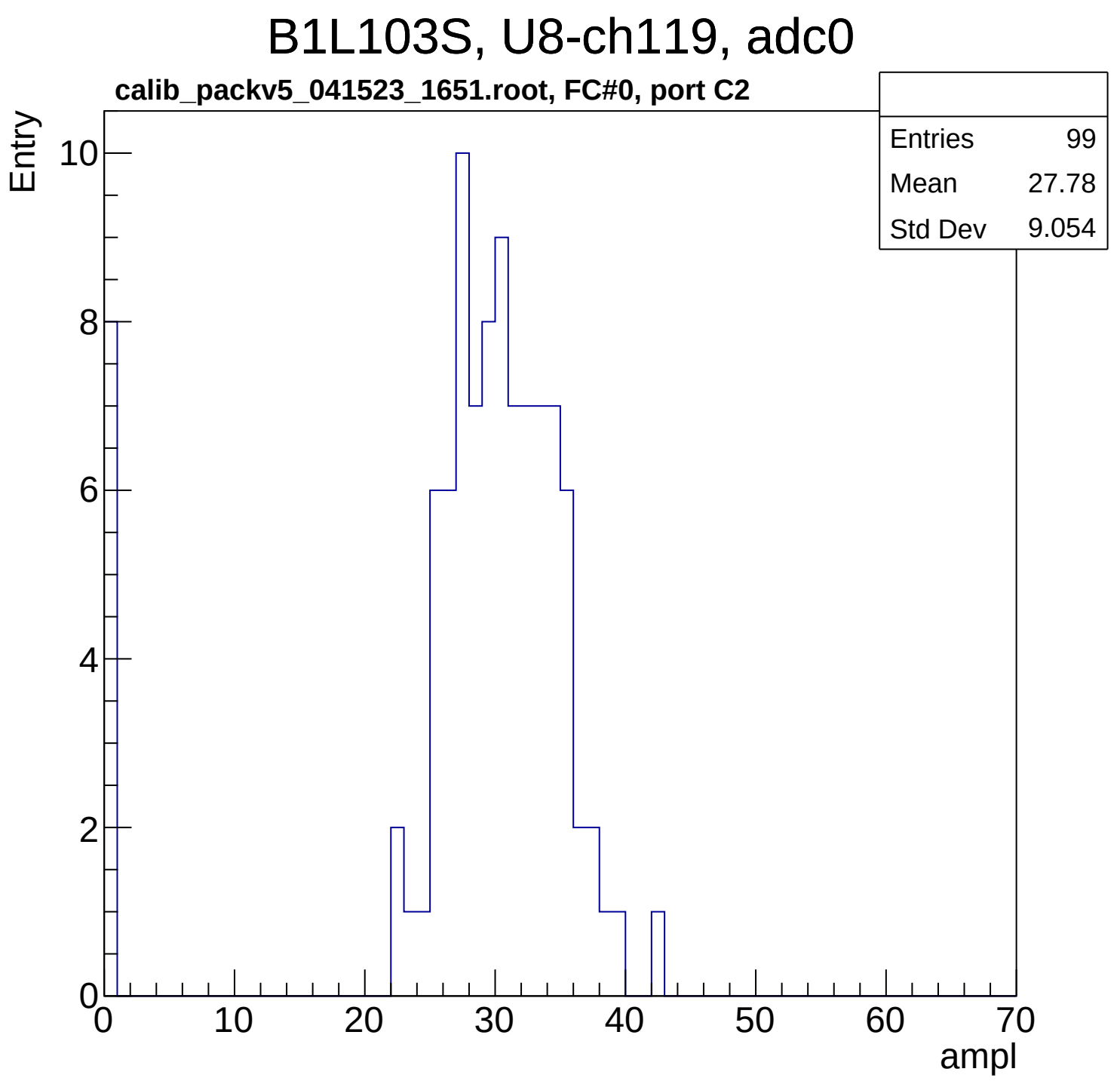
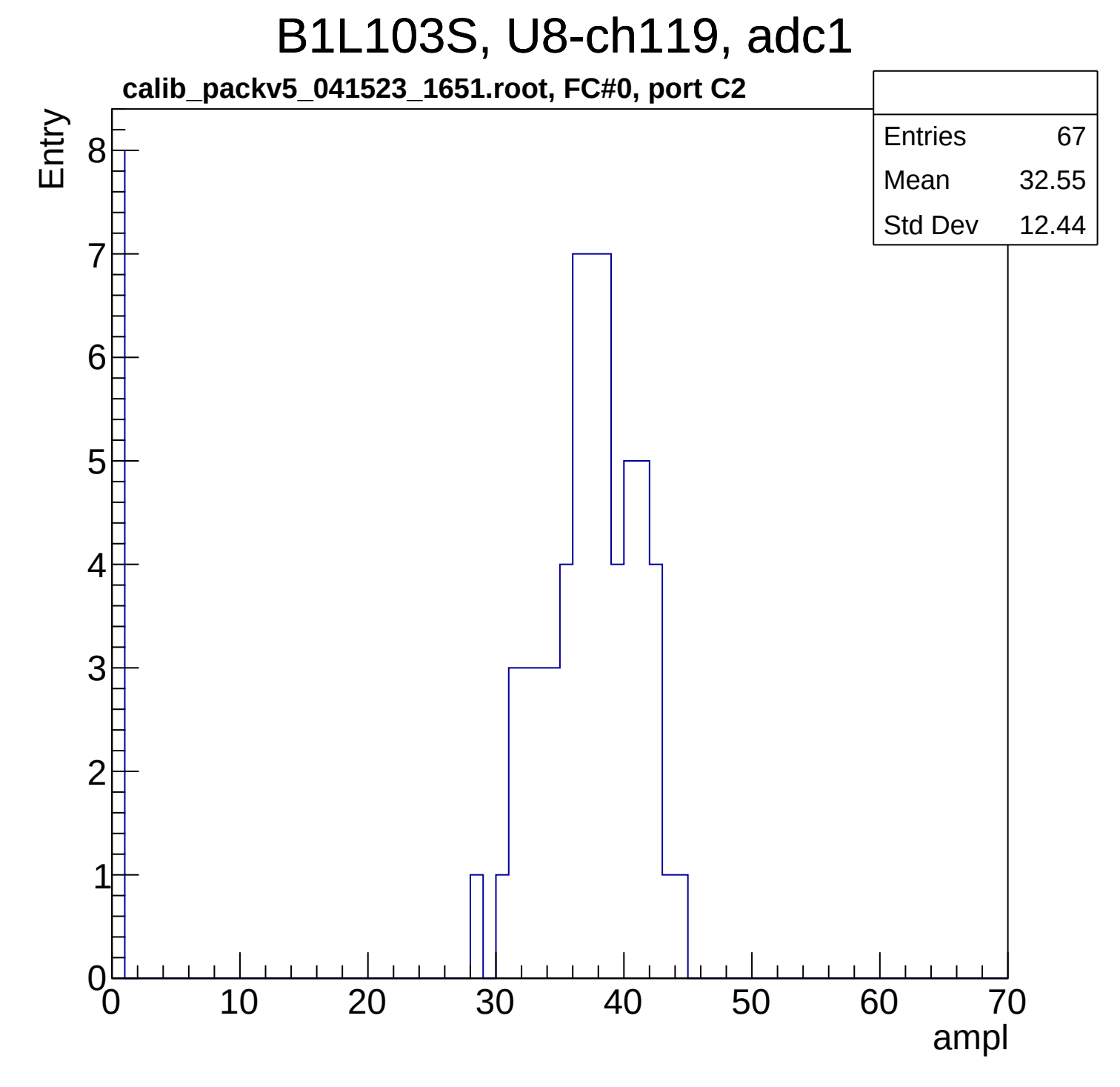
60
70
ampl


B1L103S, U8-ch119, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 27.78
Std Dev 9.054
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U8-ch119, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 32.55
Std Dev 12.44
Entry
ampl
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1
2
3
4
5
6
7
8
0
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40
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60
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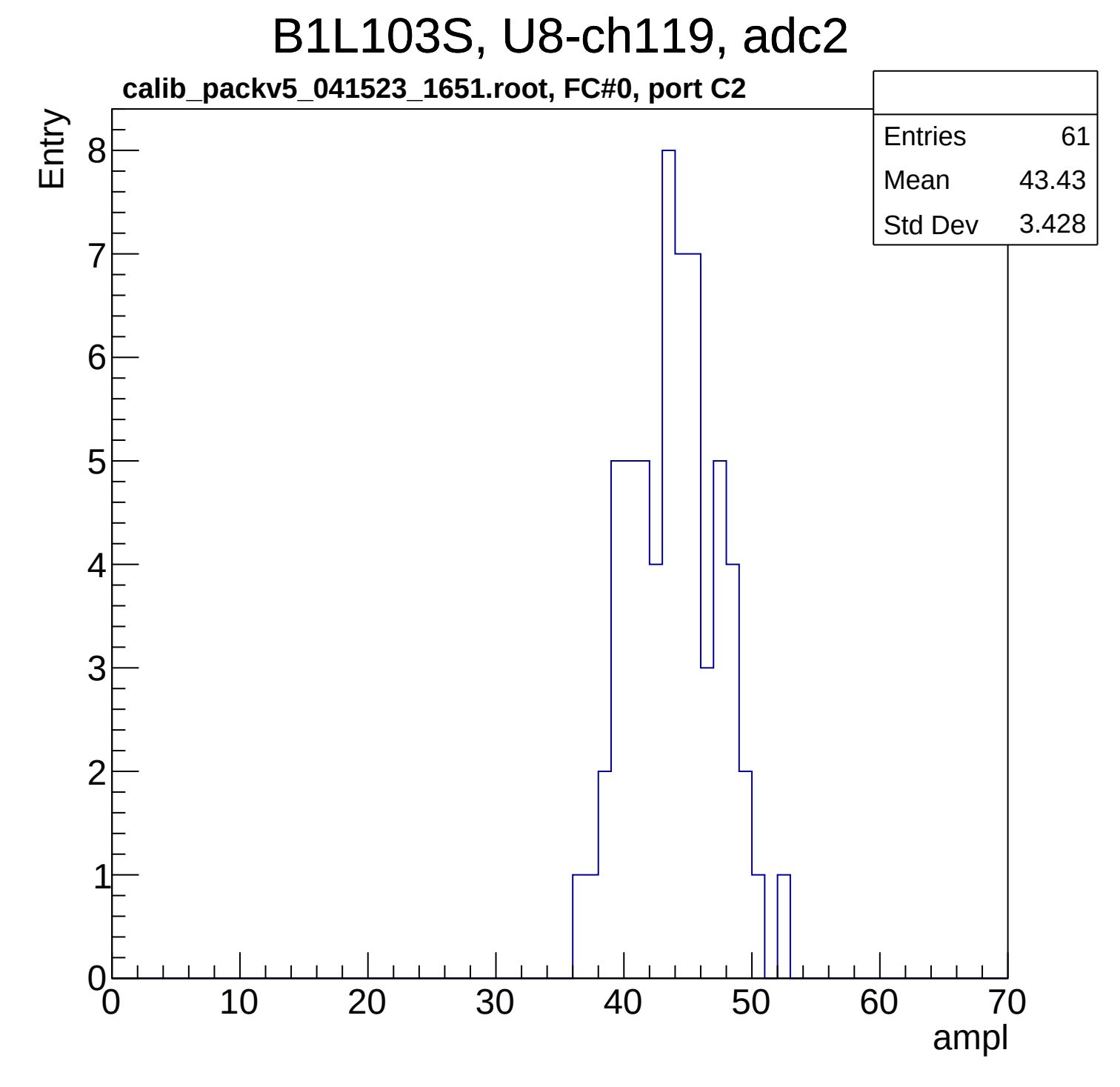
B1L103S, U8-ch119, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 43.43
Std Dev 3.428
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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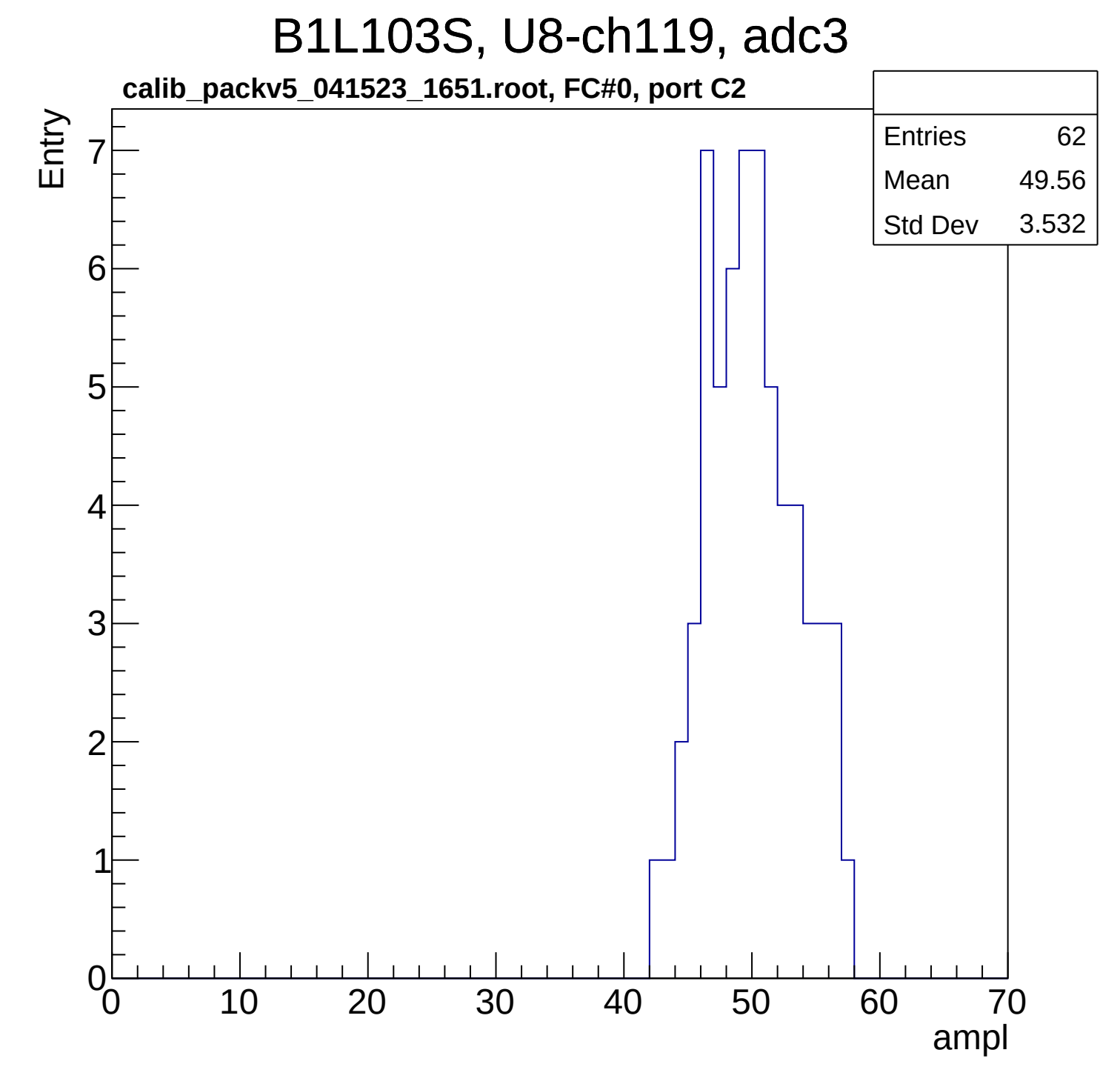
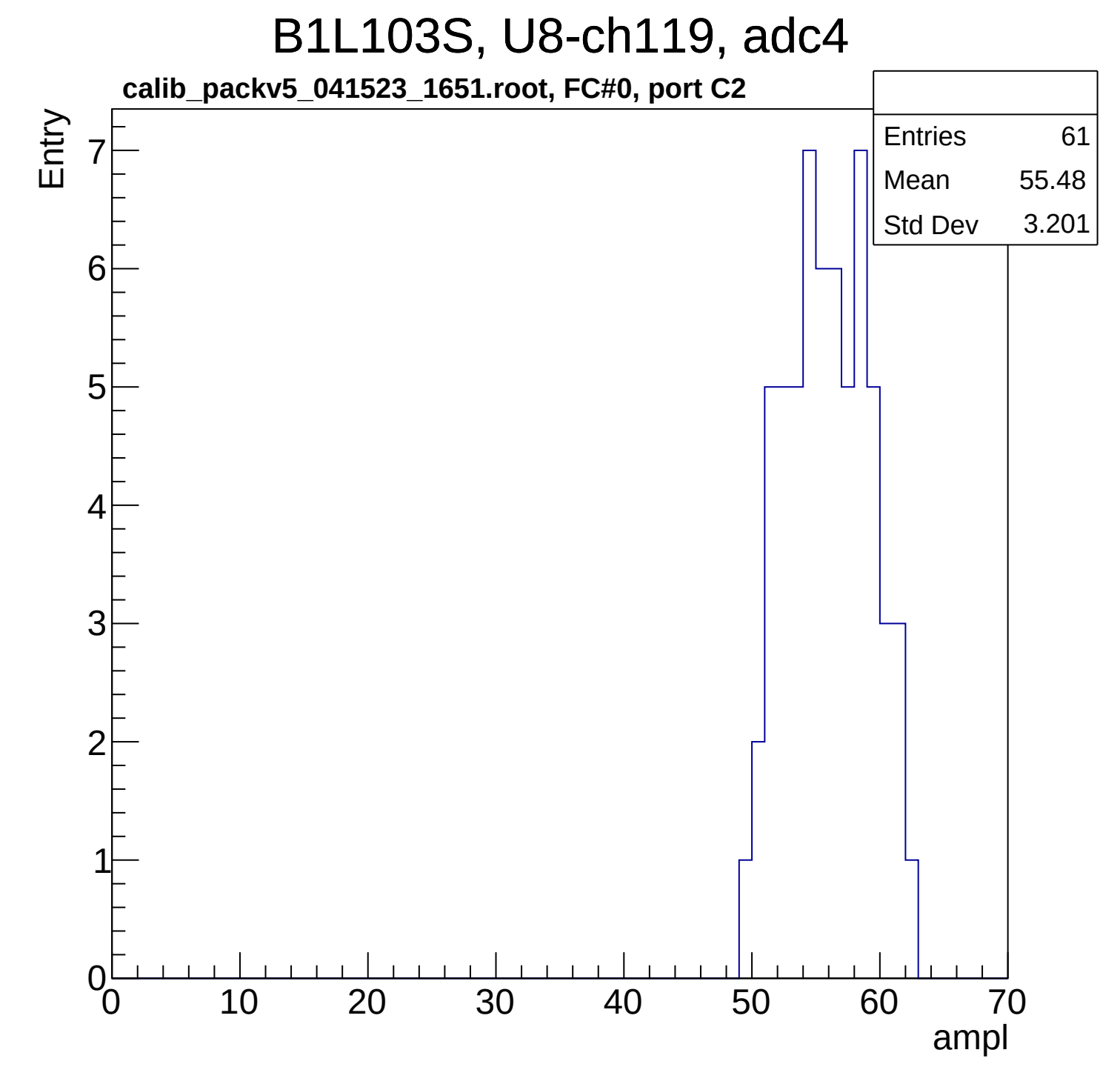

B1L103S, U8-ch119, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 49.56
Std Dev 3.532
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U8-ch119, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 55.48
Std Dev 3.201
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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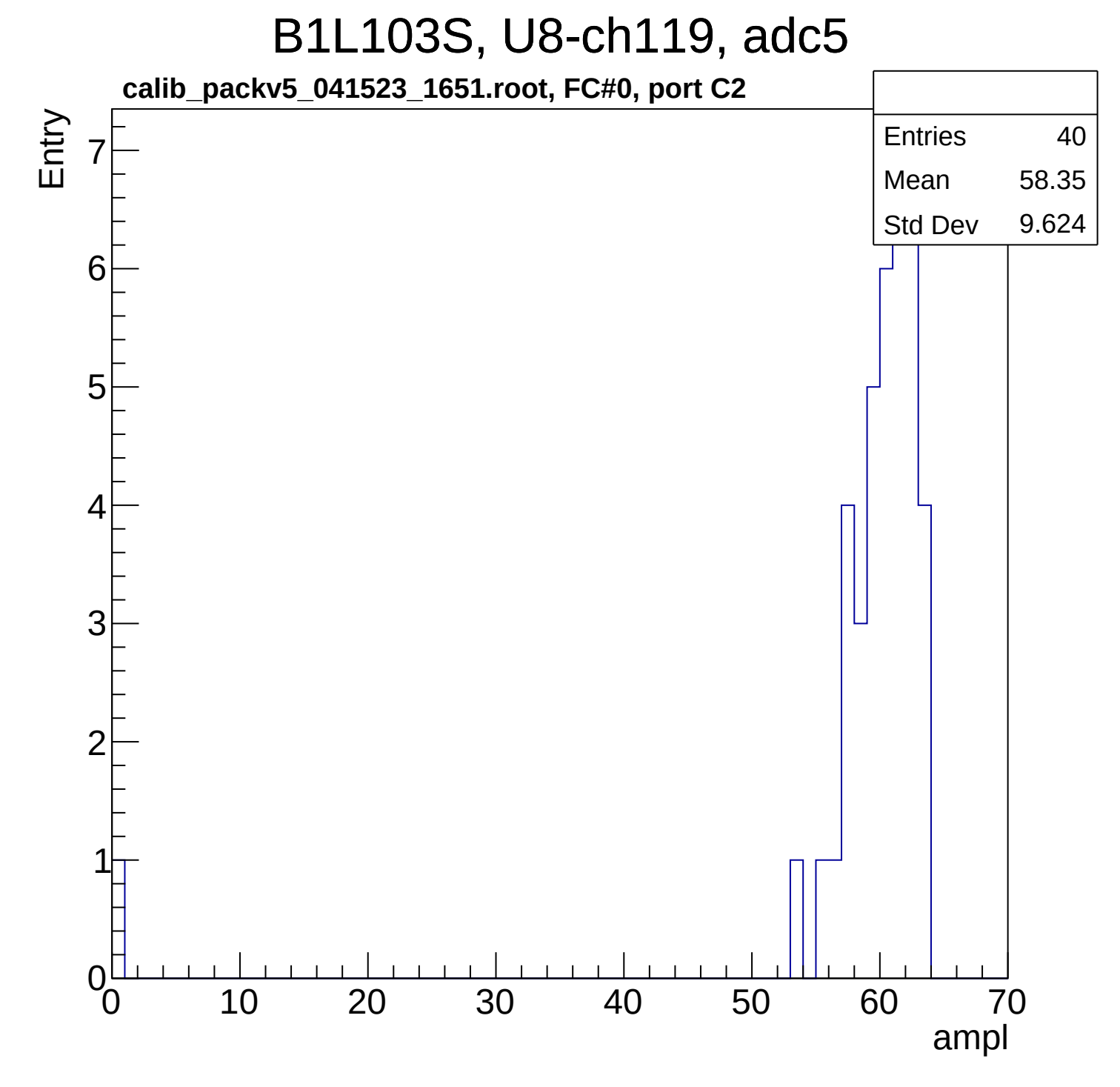
B1L103S, U8-ch119, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 58.35
Std Dev 9.624
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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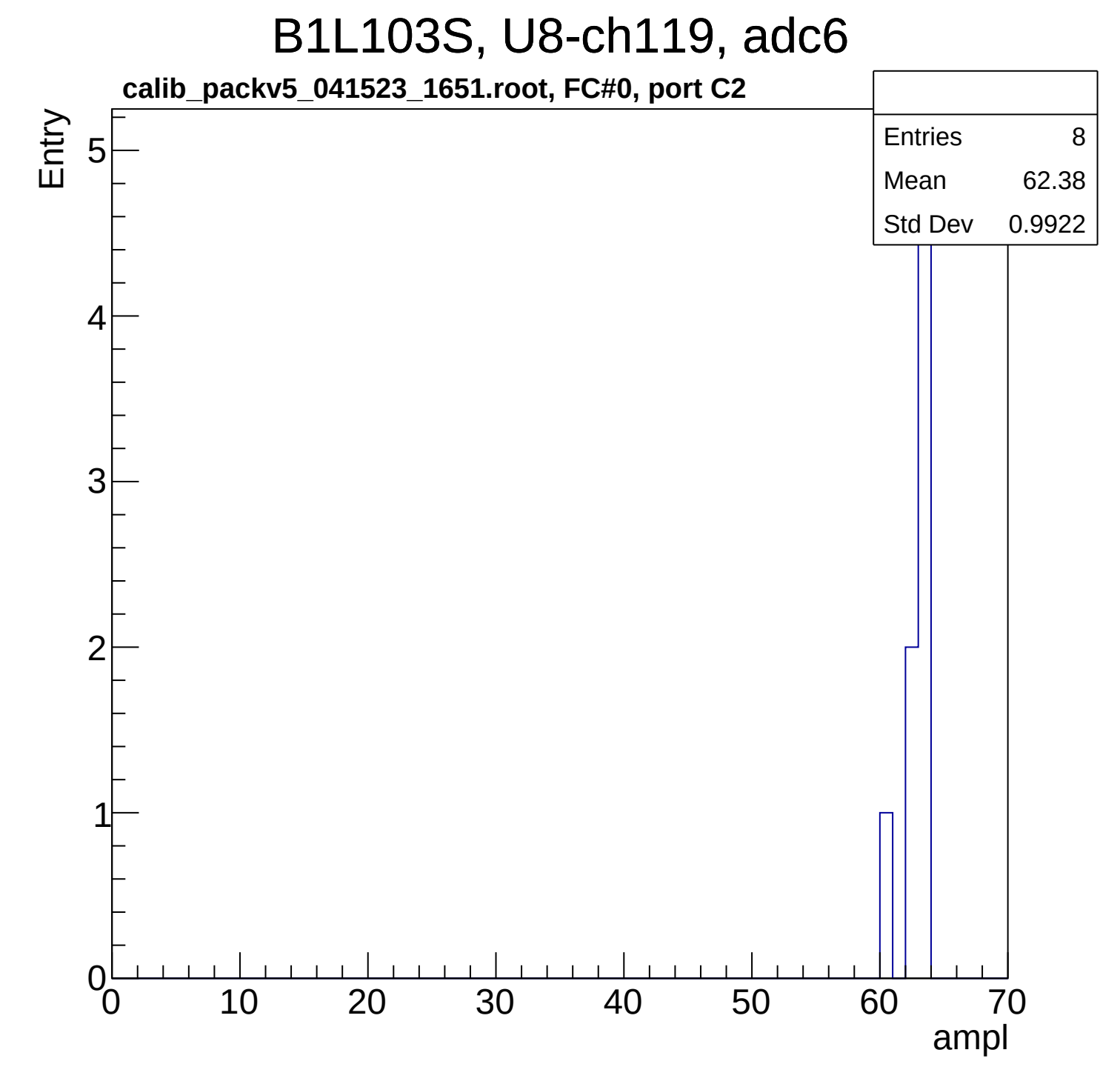
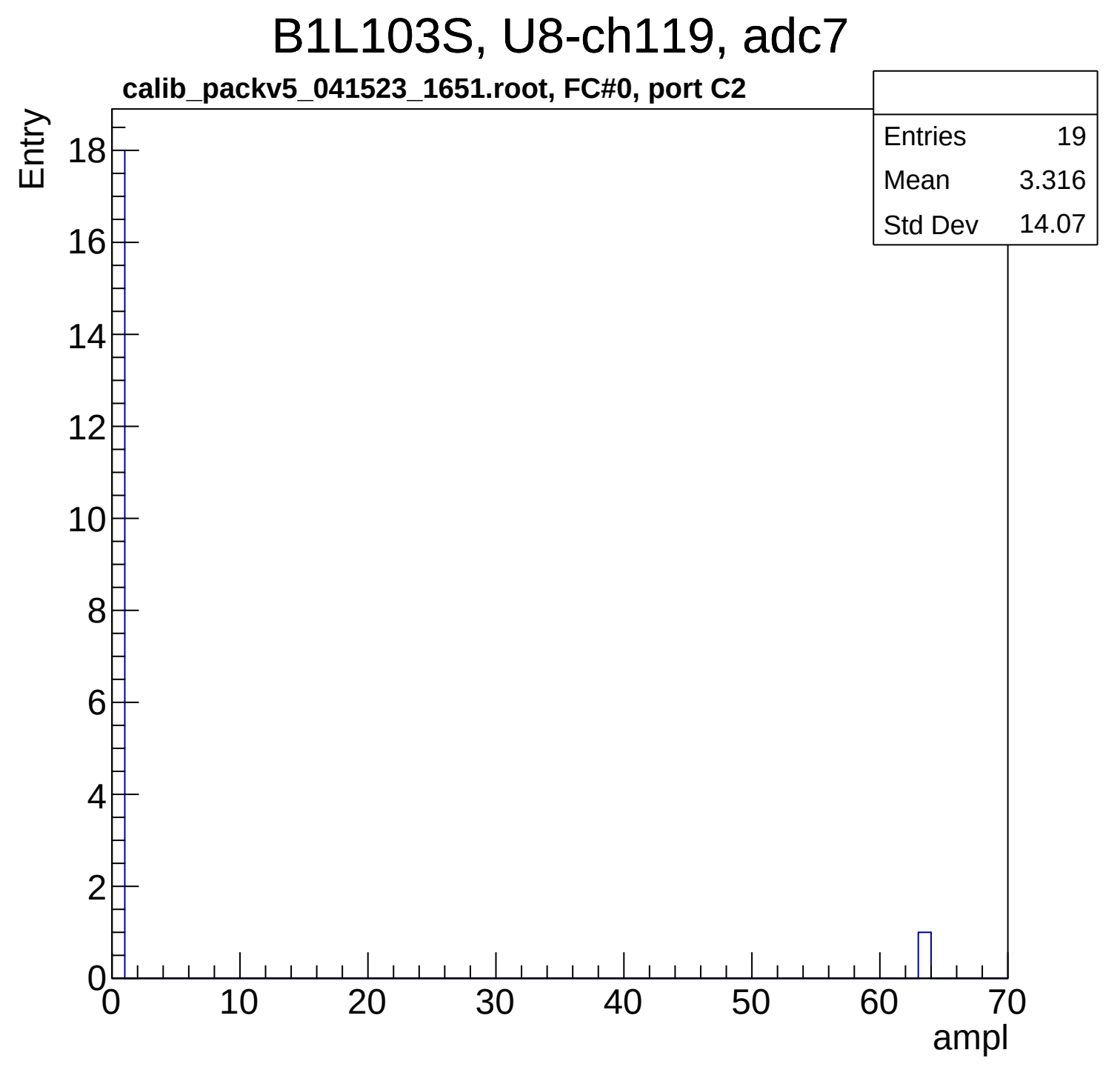

B1L103S, U8-ch119, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 62.38
Std Dev 0.9922
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U8-ch119, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.316
Std Dev 14.07
Entry
0
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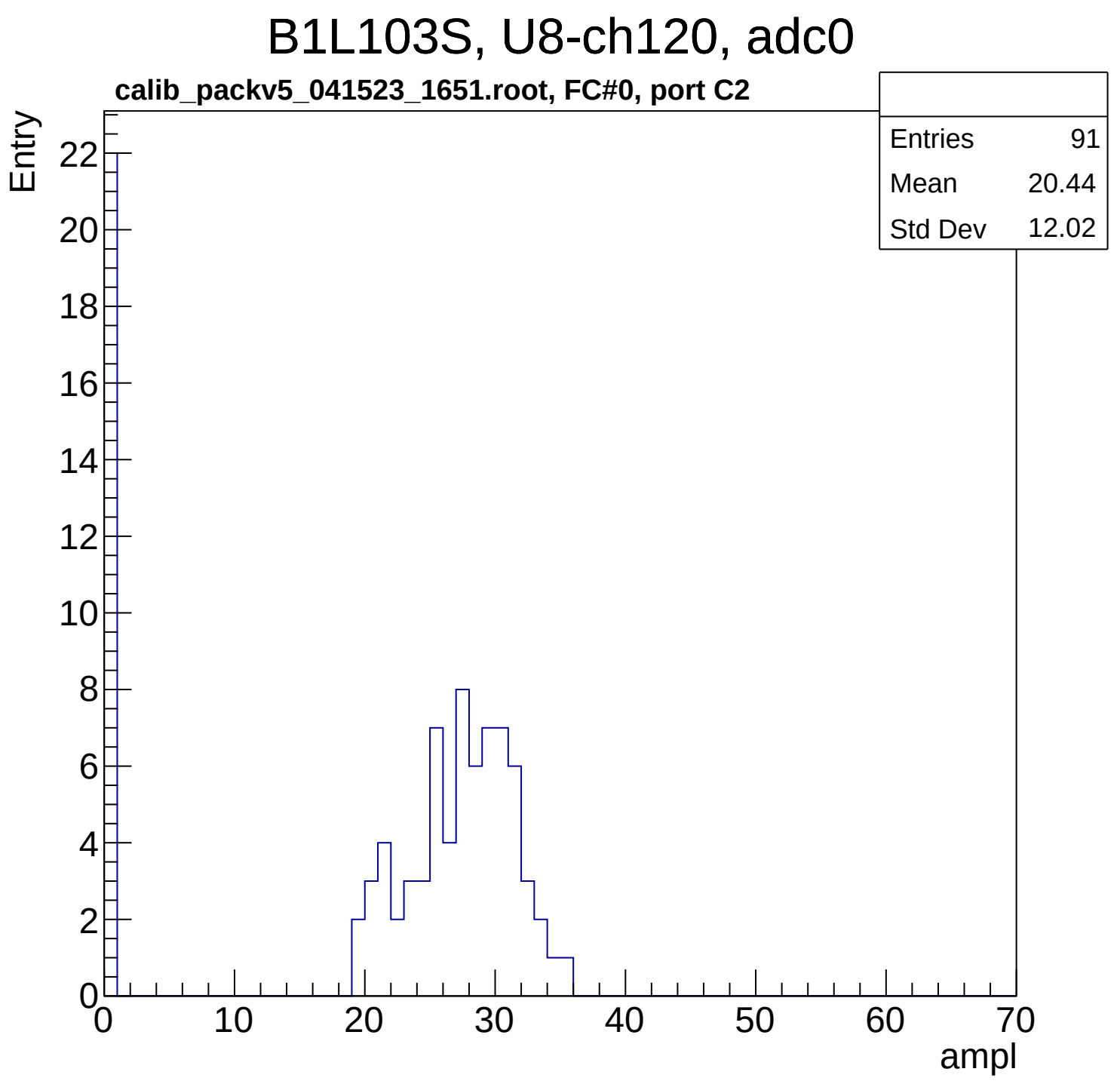
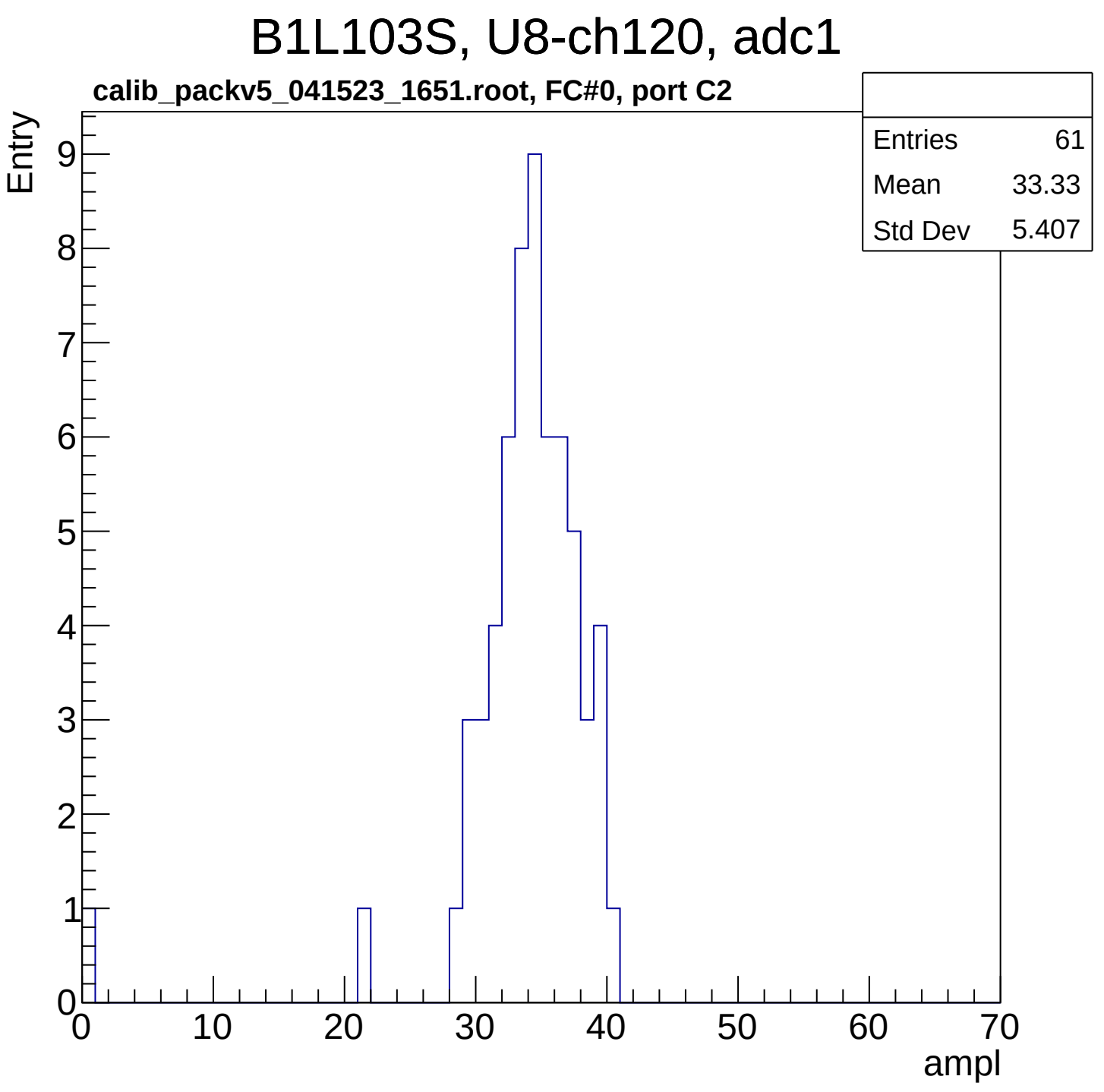
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch120, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 20.44
Std Dev 12.02
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70


B1L103S, U8-ch120, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 33.33
Std Dev 5.407
Entry
ampl
0
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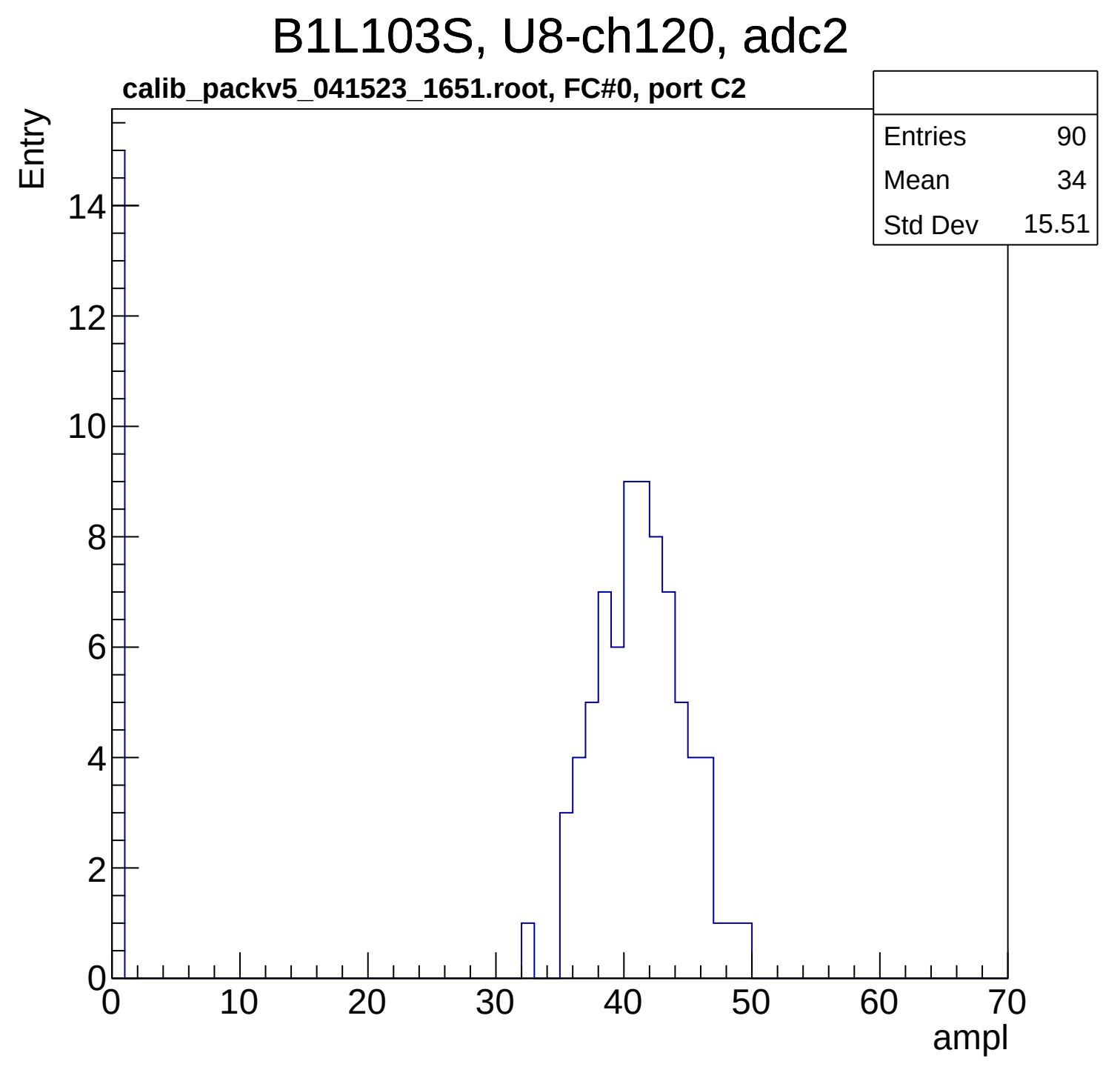
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U8-ch120, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 34
Std Dev 15.51
Entry
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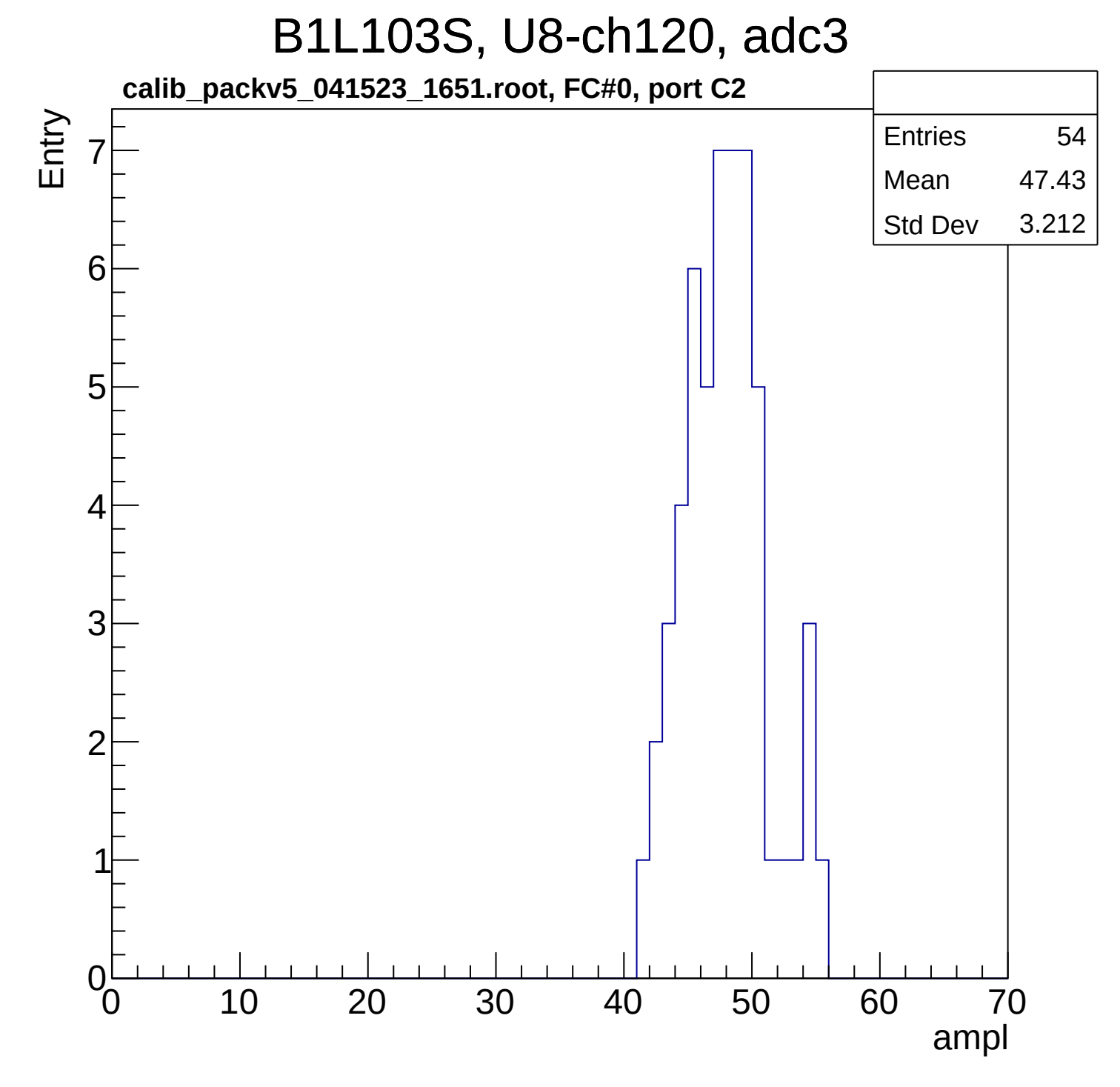
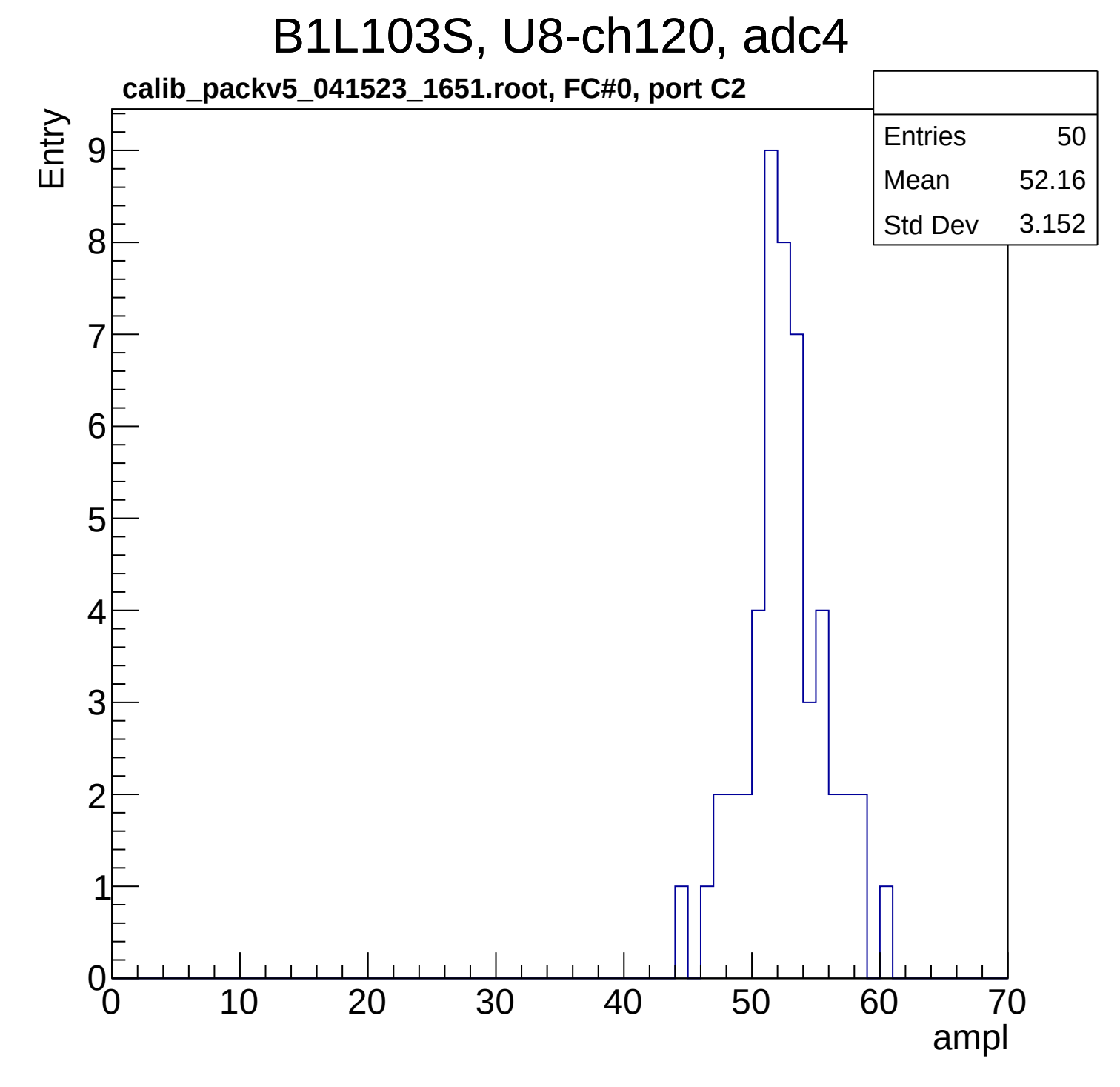
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch120, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 47.43
Std Dev 3.212
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U8-ch120, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 52.16
Std Dev 3.152
Entry
ampl
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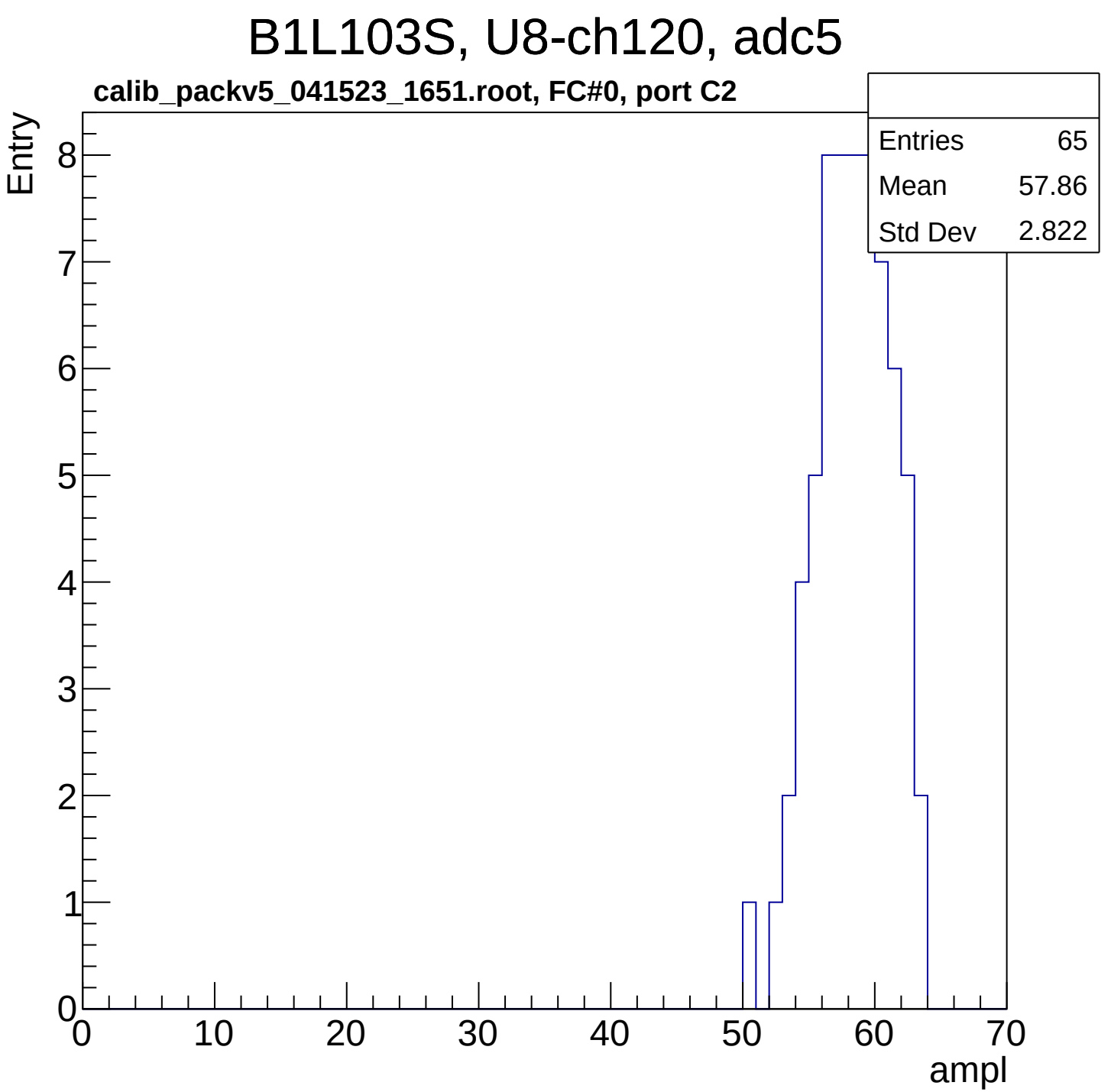
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L103S, U8-ch120, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 57.86
Std Dev 2.822
Entry
ampl
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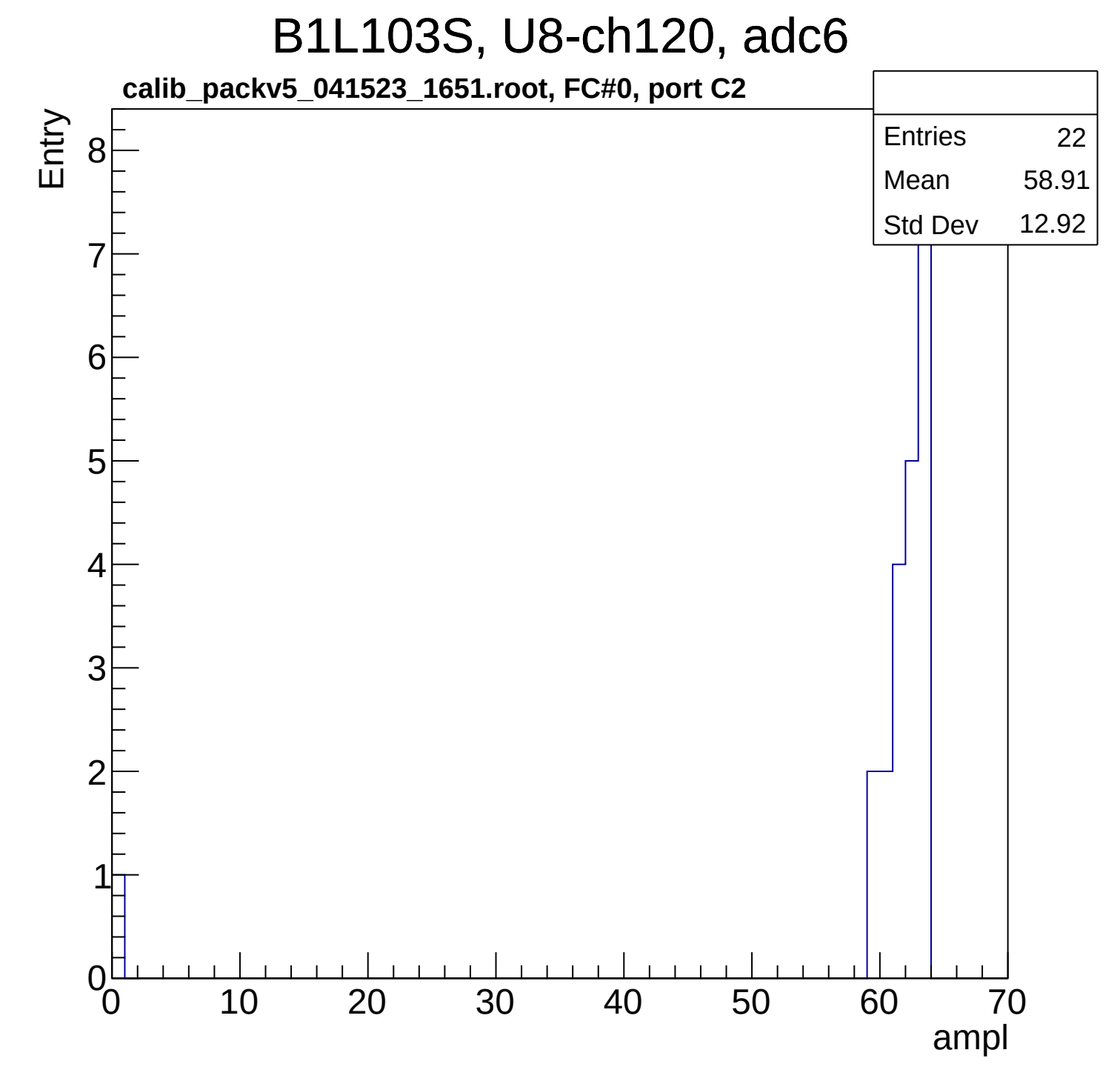
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch120, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 58.91
Std Dev 12.92
Entry
ampl
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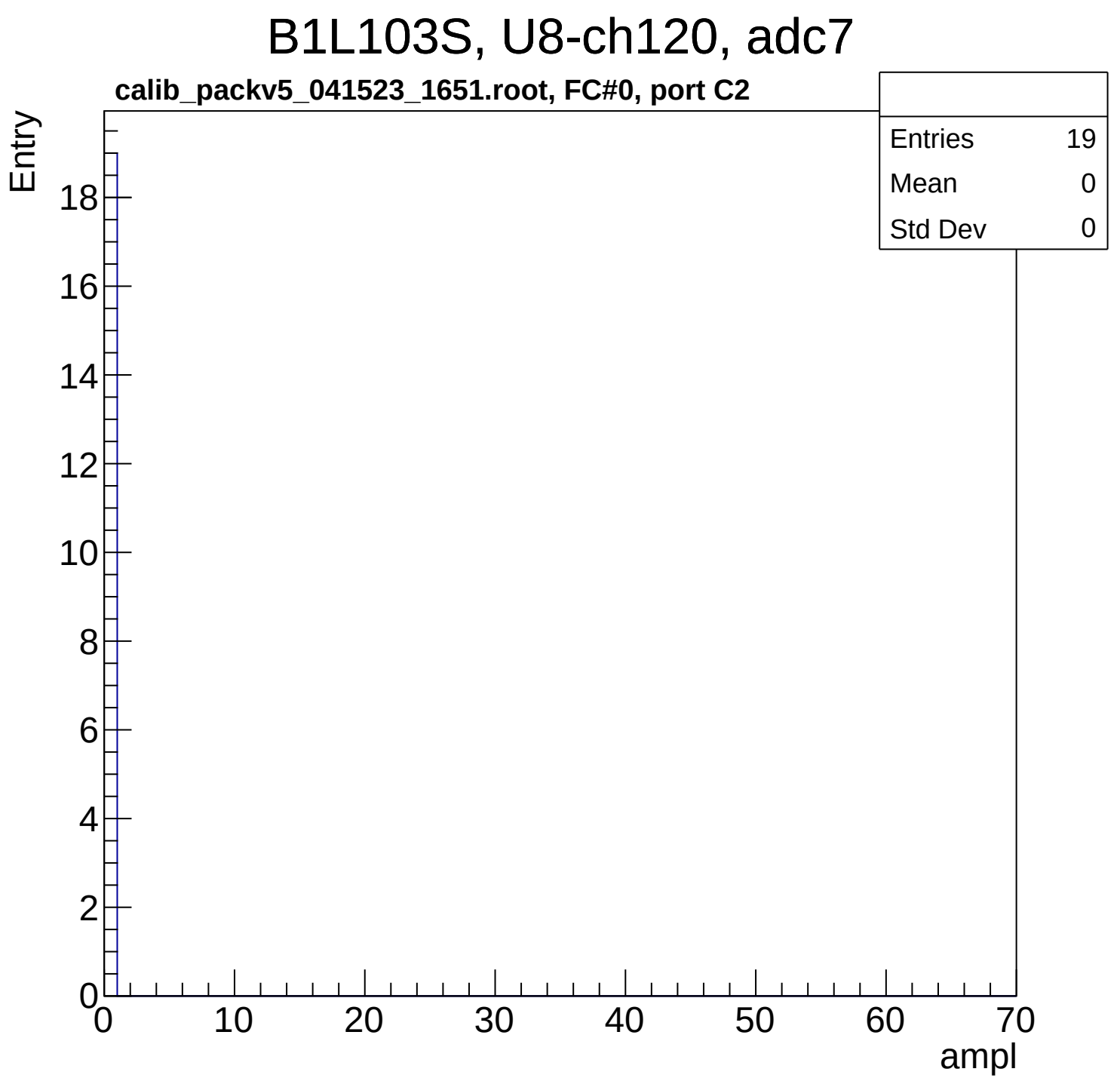
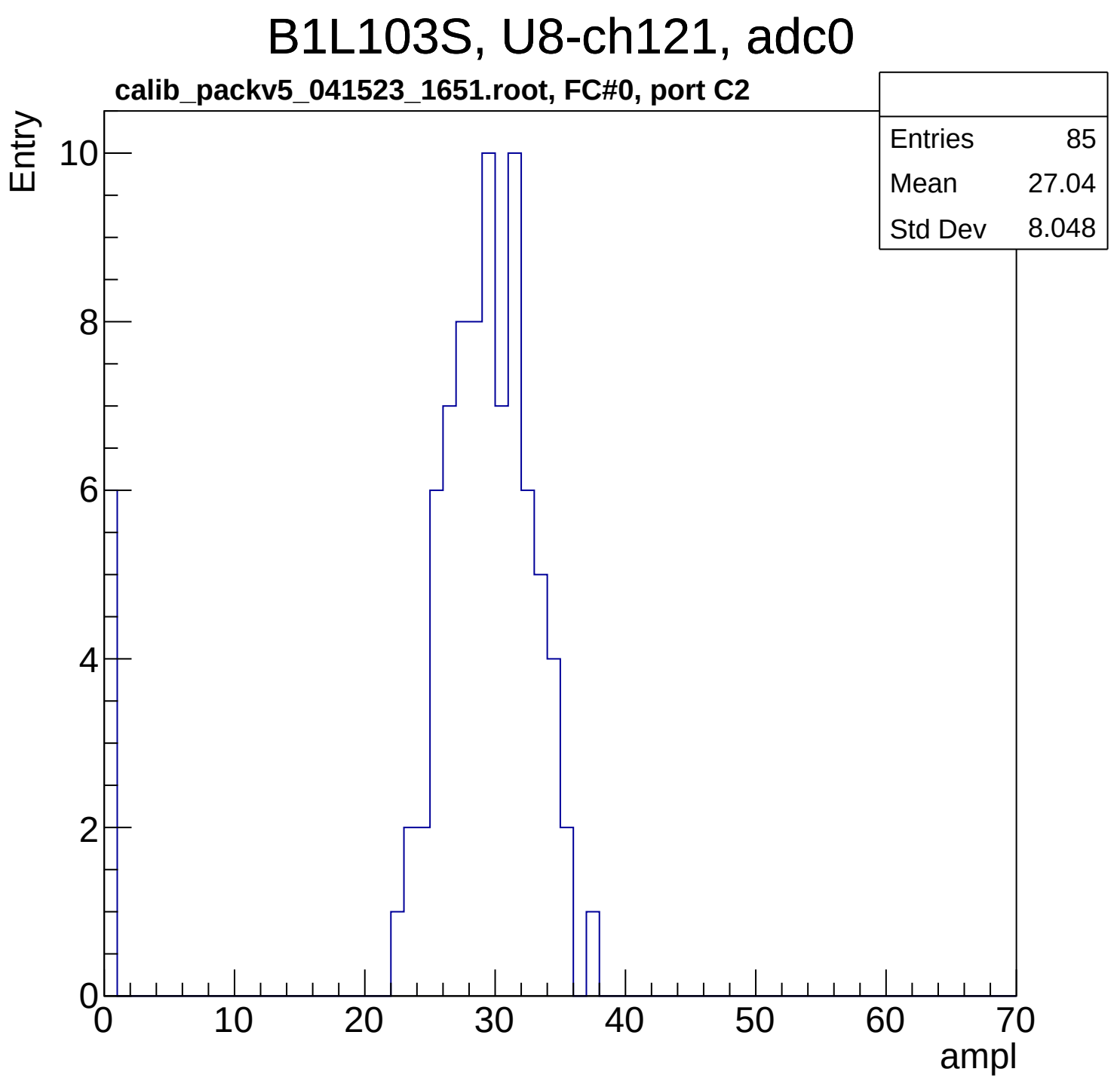
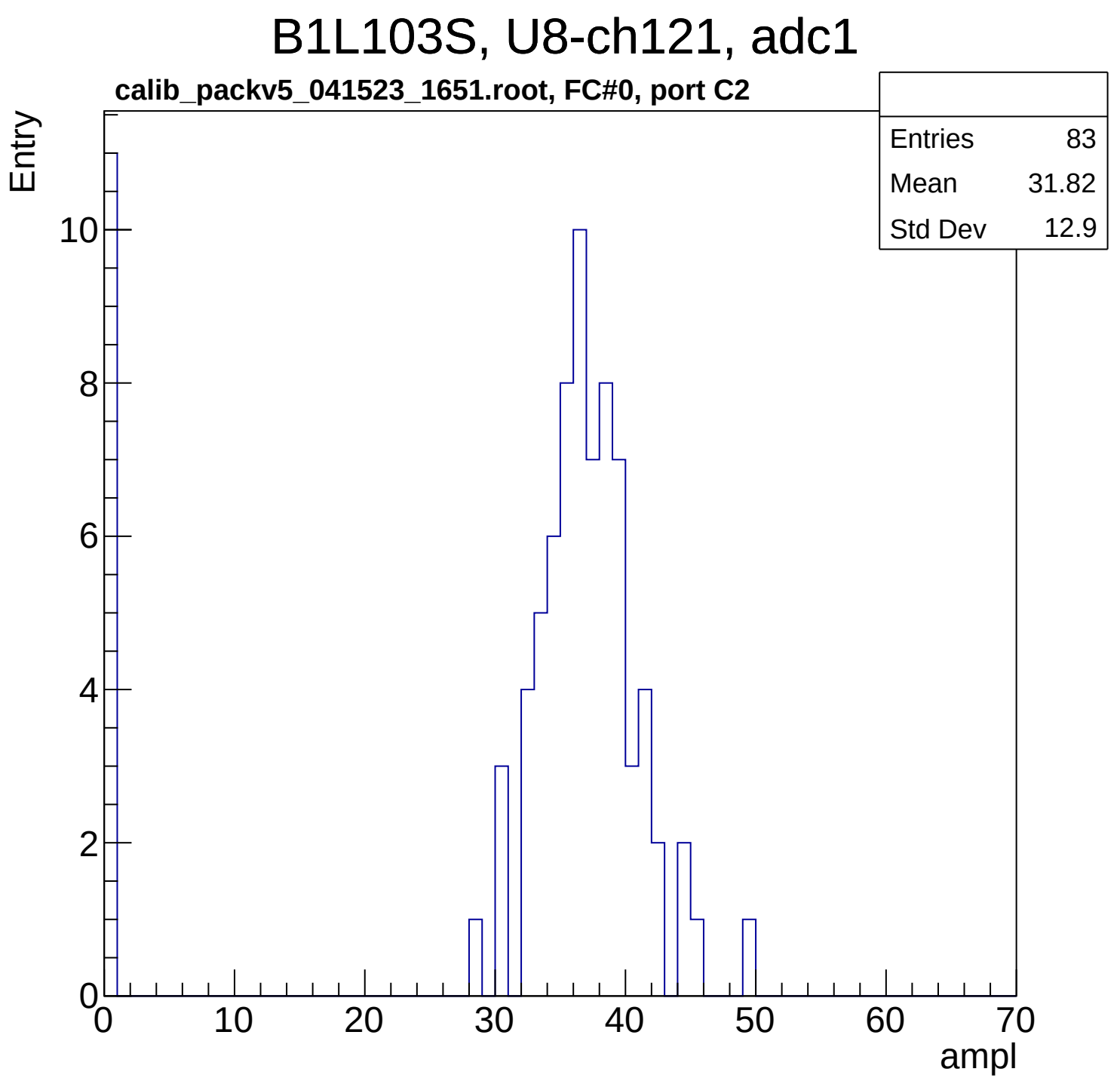
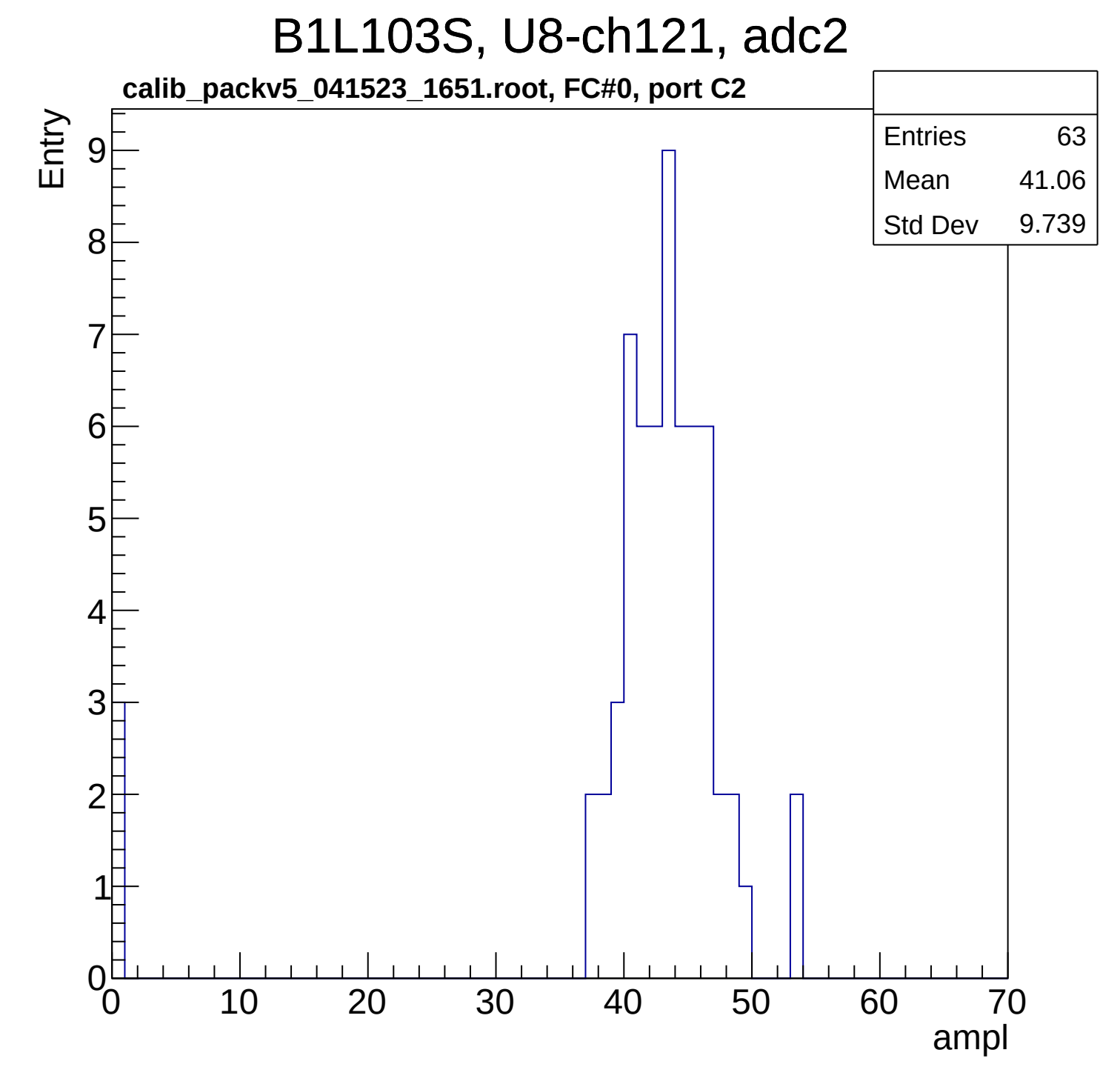
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch120, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch121, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 27.04
Std Dev 8.048
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U8-ch121, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 31.82
Std Dev 12.9
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch121, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 41.06
Std Dev 9.739
Entry
ampl
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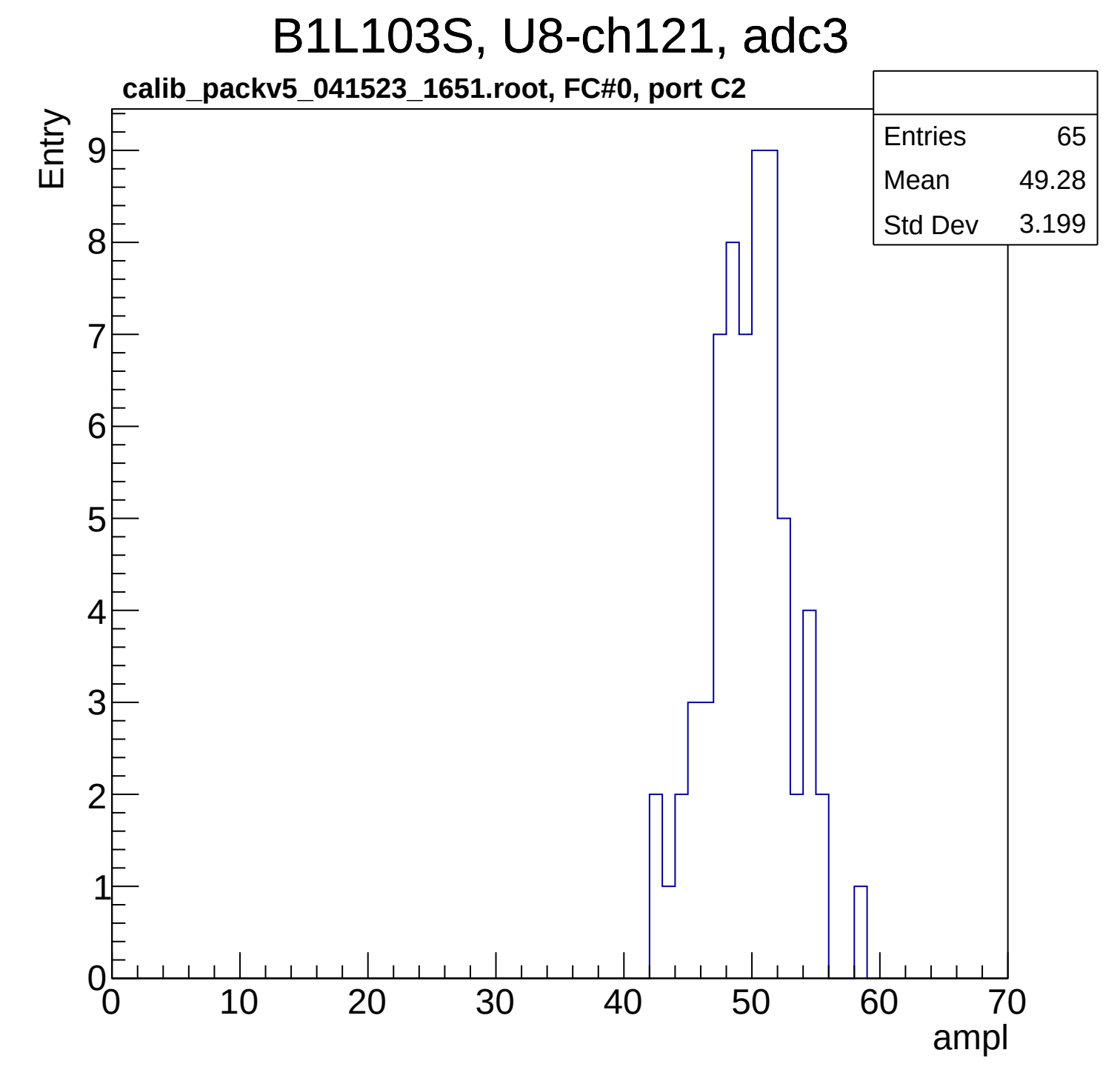
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U8-ch121, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 49.28
Std Dev 3.199
Entry
ampl
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10
20
30
40
50
60
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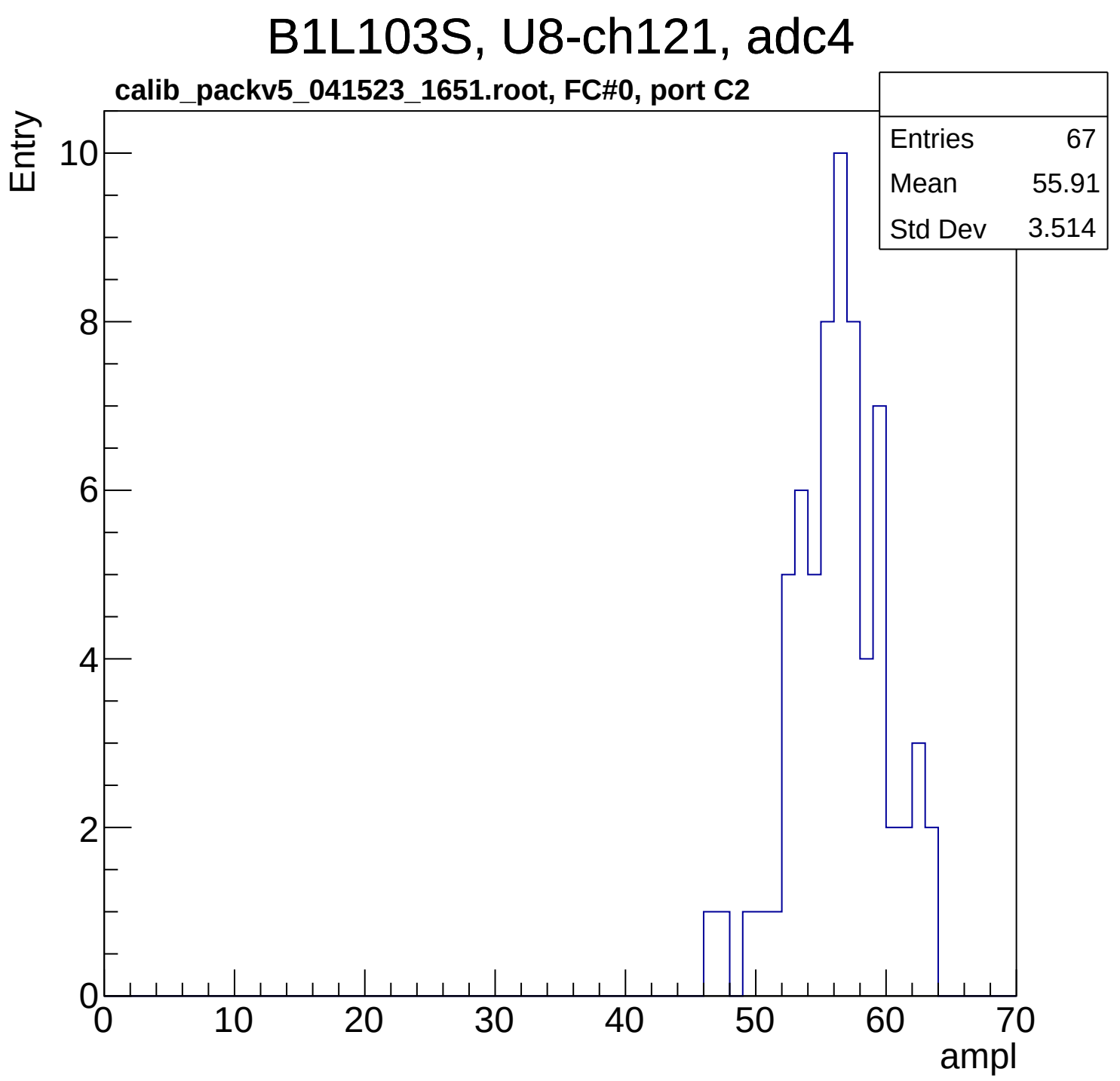
1
2
3
4
5
6
7
8
9


B1L103S, U8-ch121, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 55.91
Std Dev 3.514
Entry
ampl
0
2
4
6
8
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0
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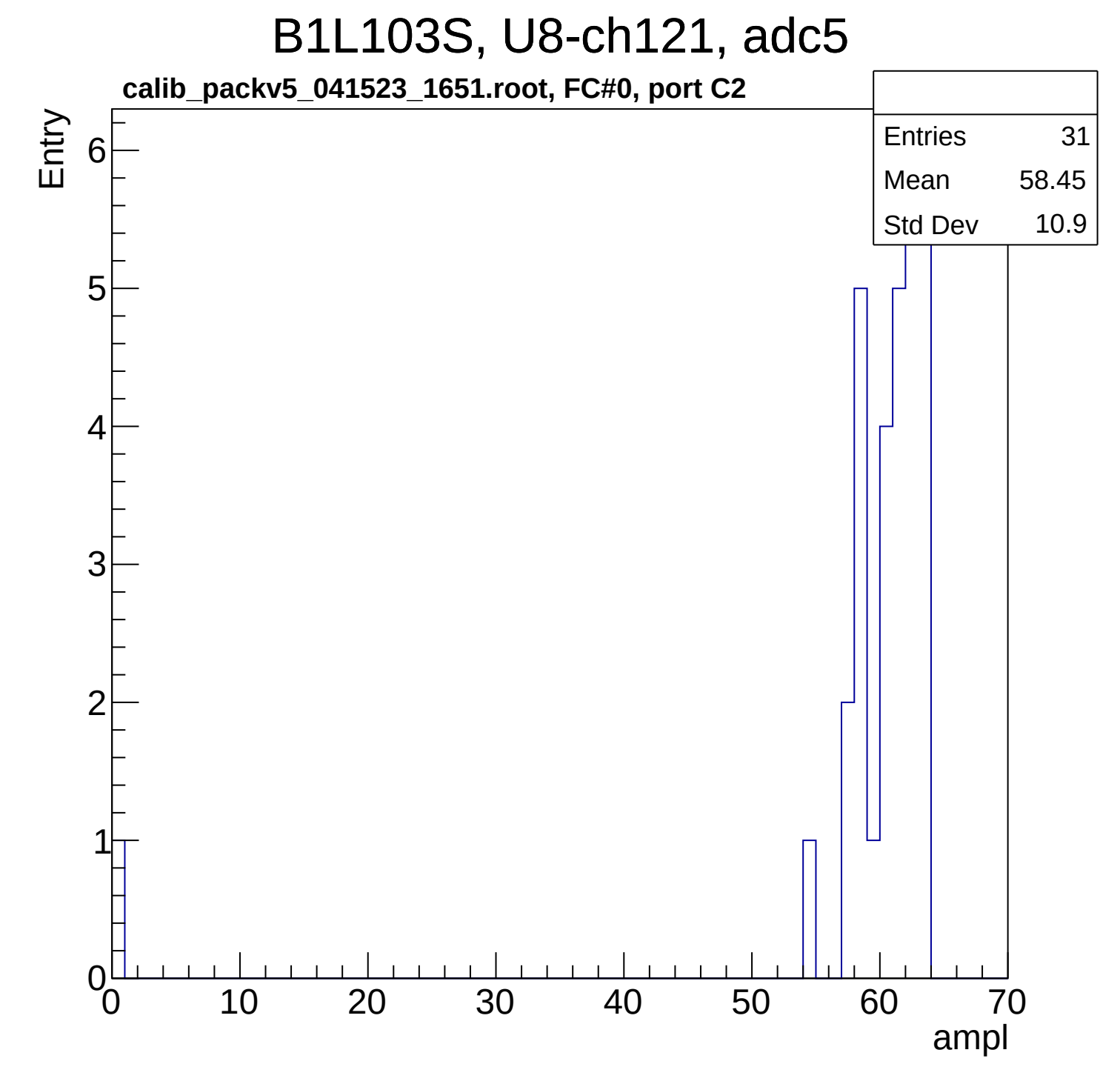
20
30
40
50
60
70


B1L103S, U8-ch121, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 58.45
Std Dev 10.9
Entry
ampl
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1
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3
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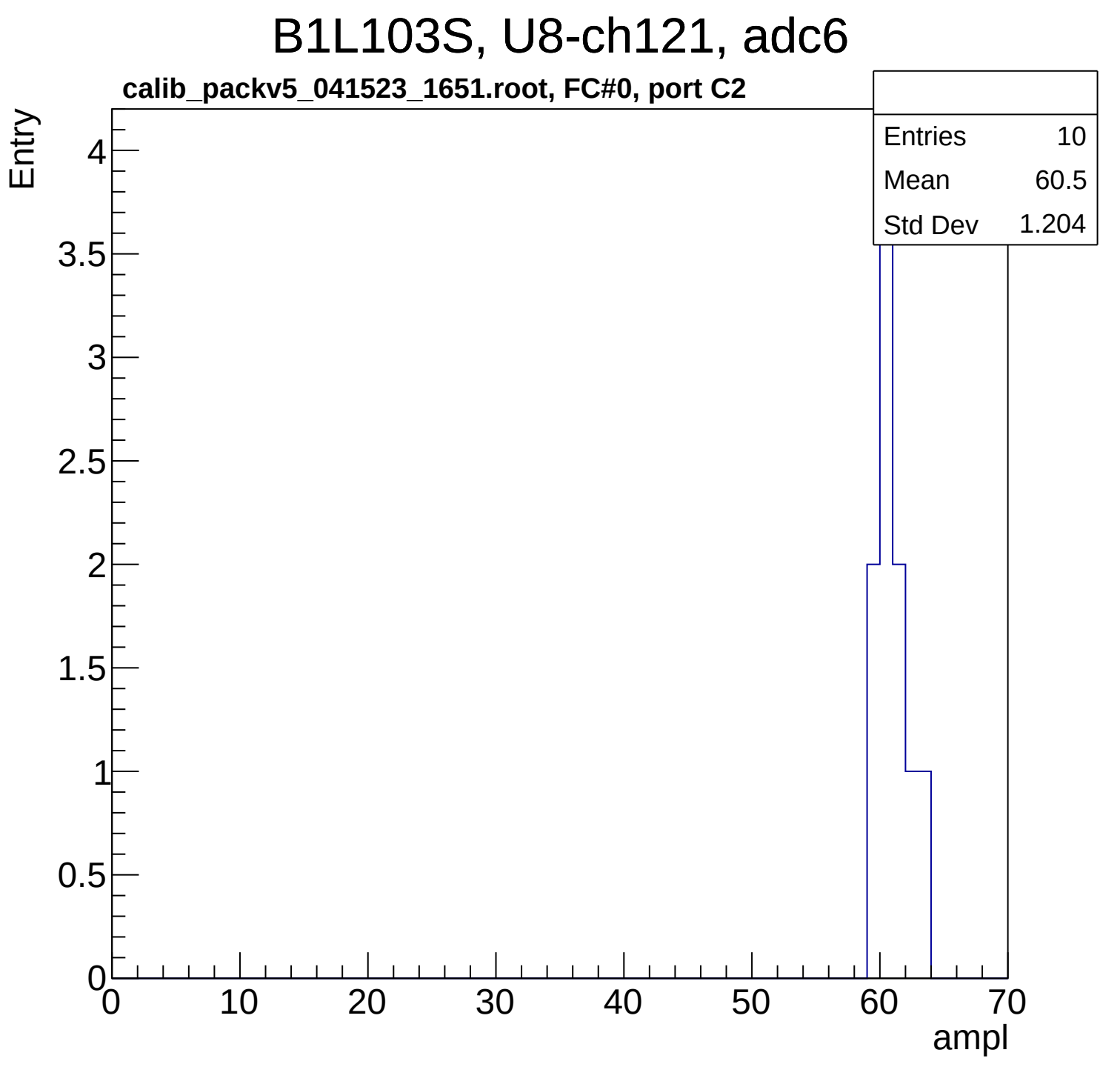
0
10
20
30
40
50
60
70


B1L103S, U8-ch121, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 60.5
Std Dev 1.204
Entry
ampl
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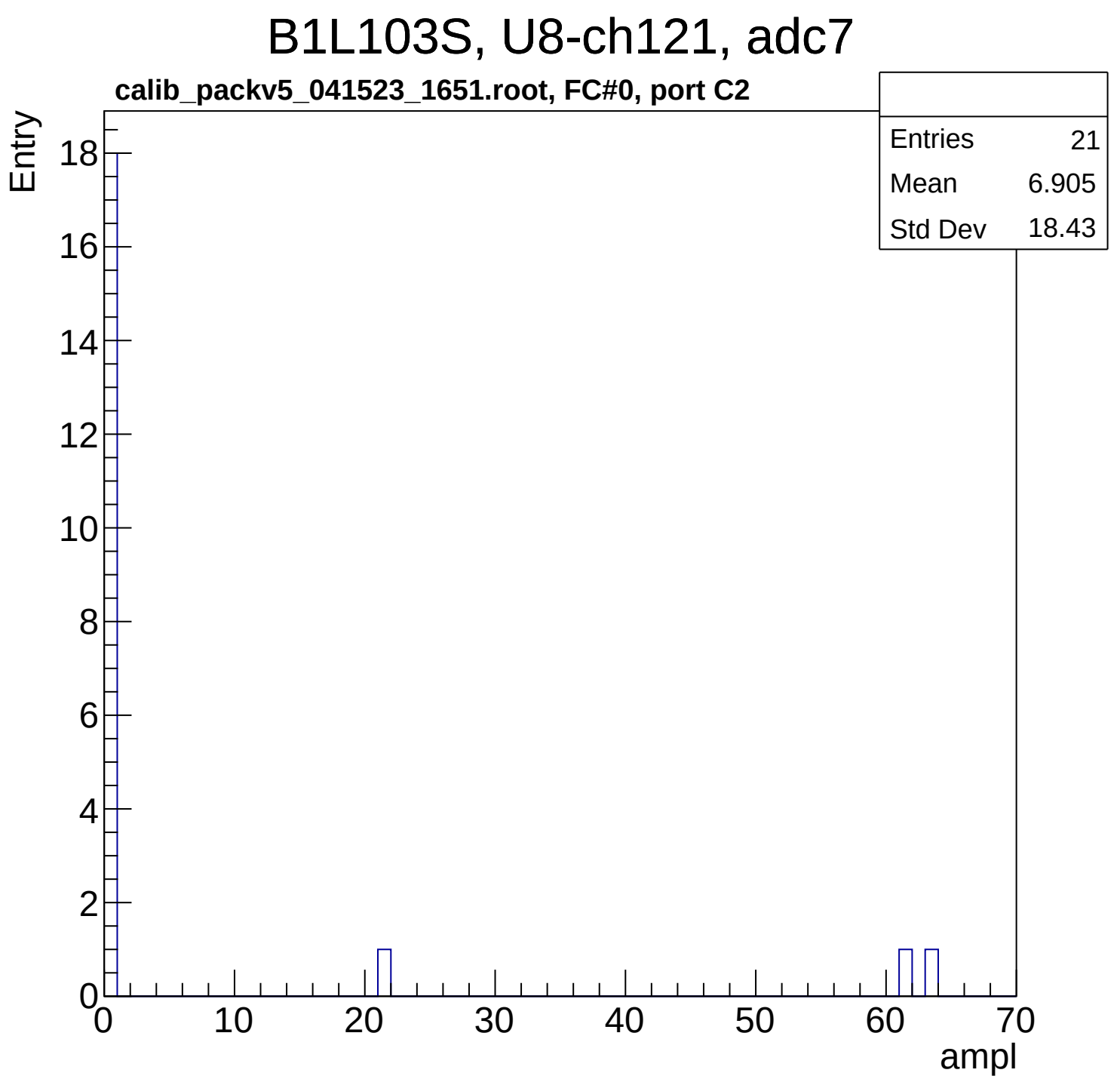
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U8-ch121, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 6.905
Std Dev 18.43
Entry
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6
8
10
12
14
16
18
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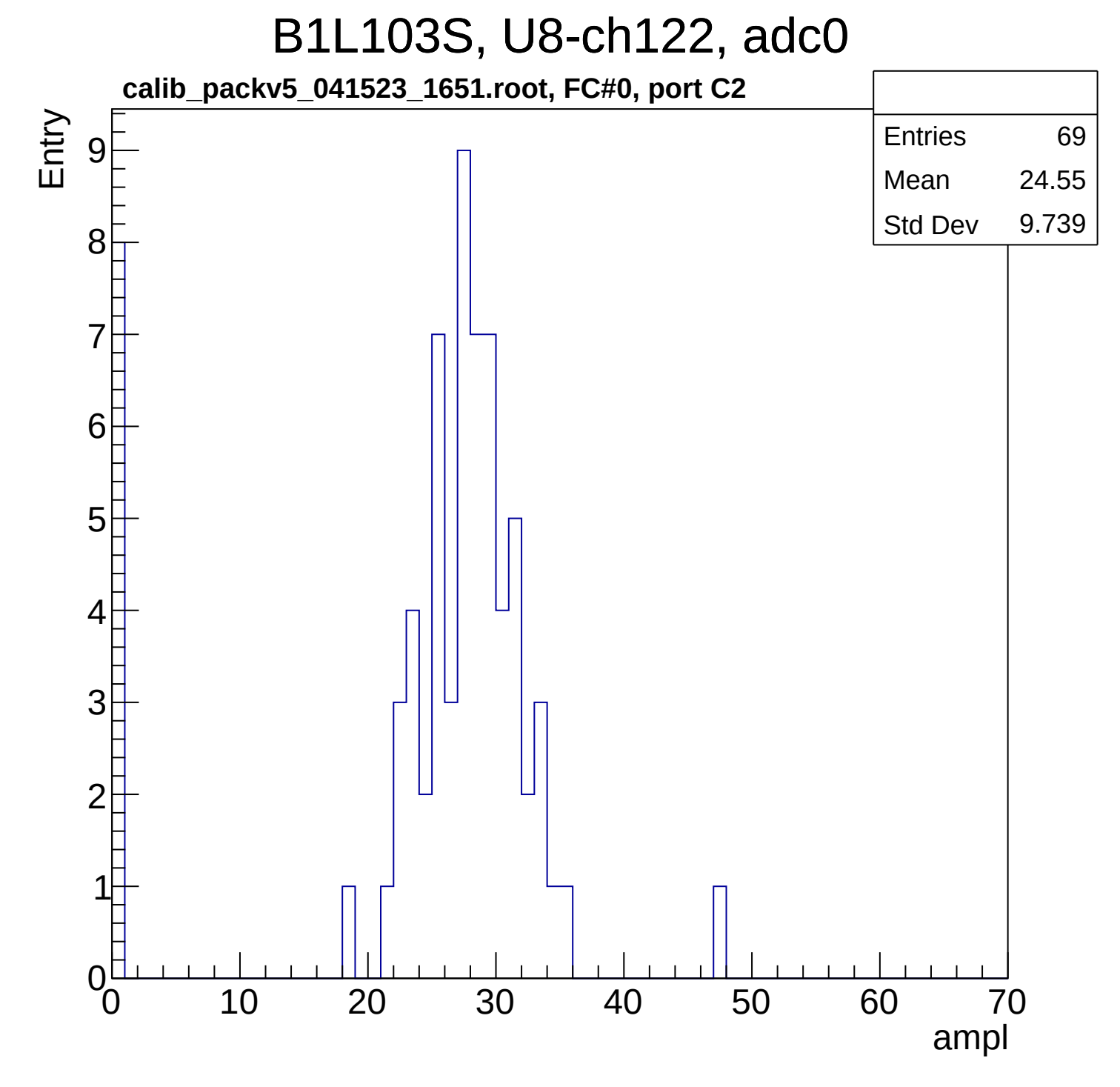
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch122, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 24.55
Std Dev 9.739
Entry
ampl
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3
4
5
6
7
8
9
0
10
20
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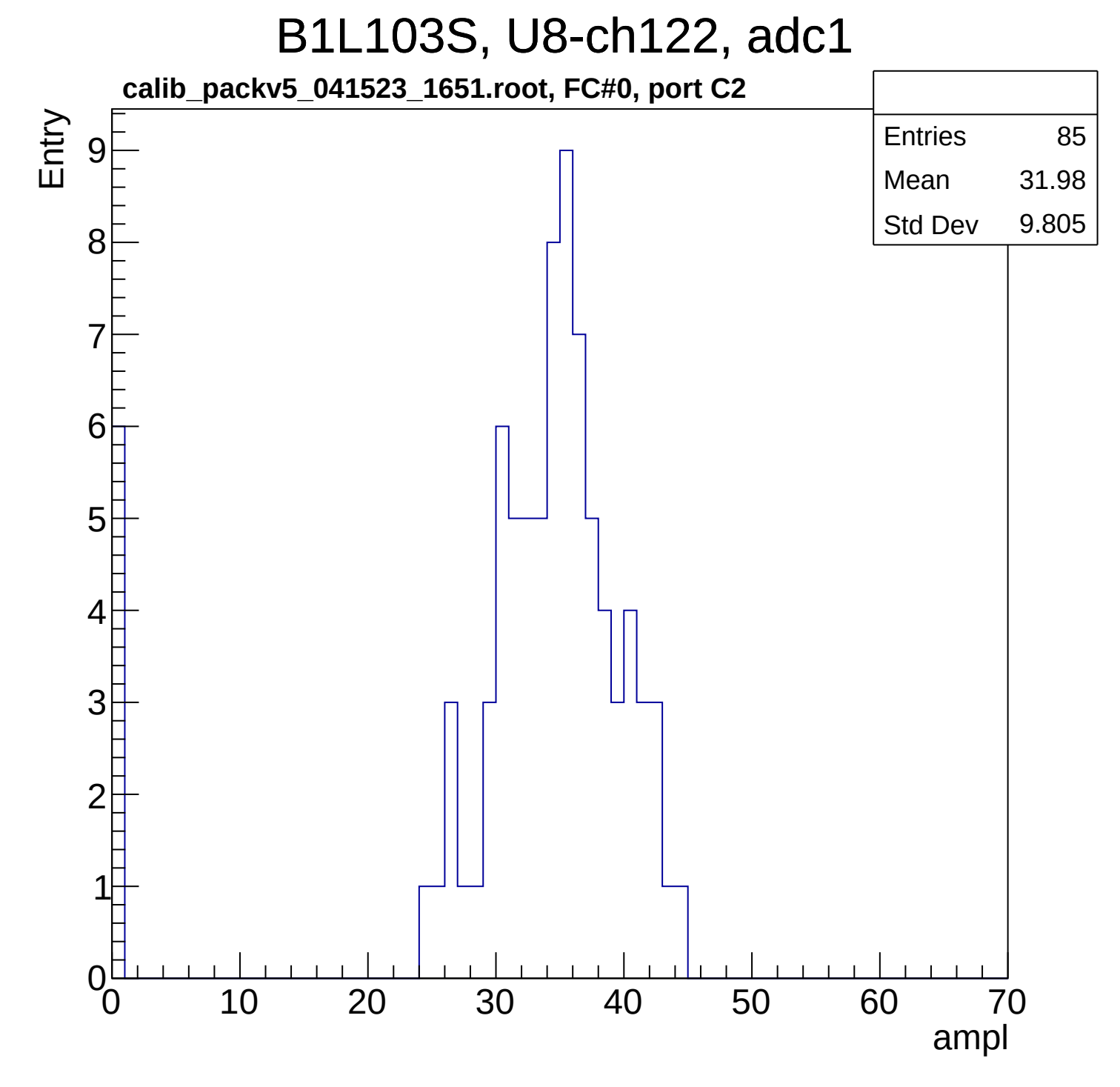
40
50
60
70


B1L103S, U8-ch122, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 31.98
Std Dev 9.805
Entry
ampl
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2
3
4
5
6
7
8
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0
10
20
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60
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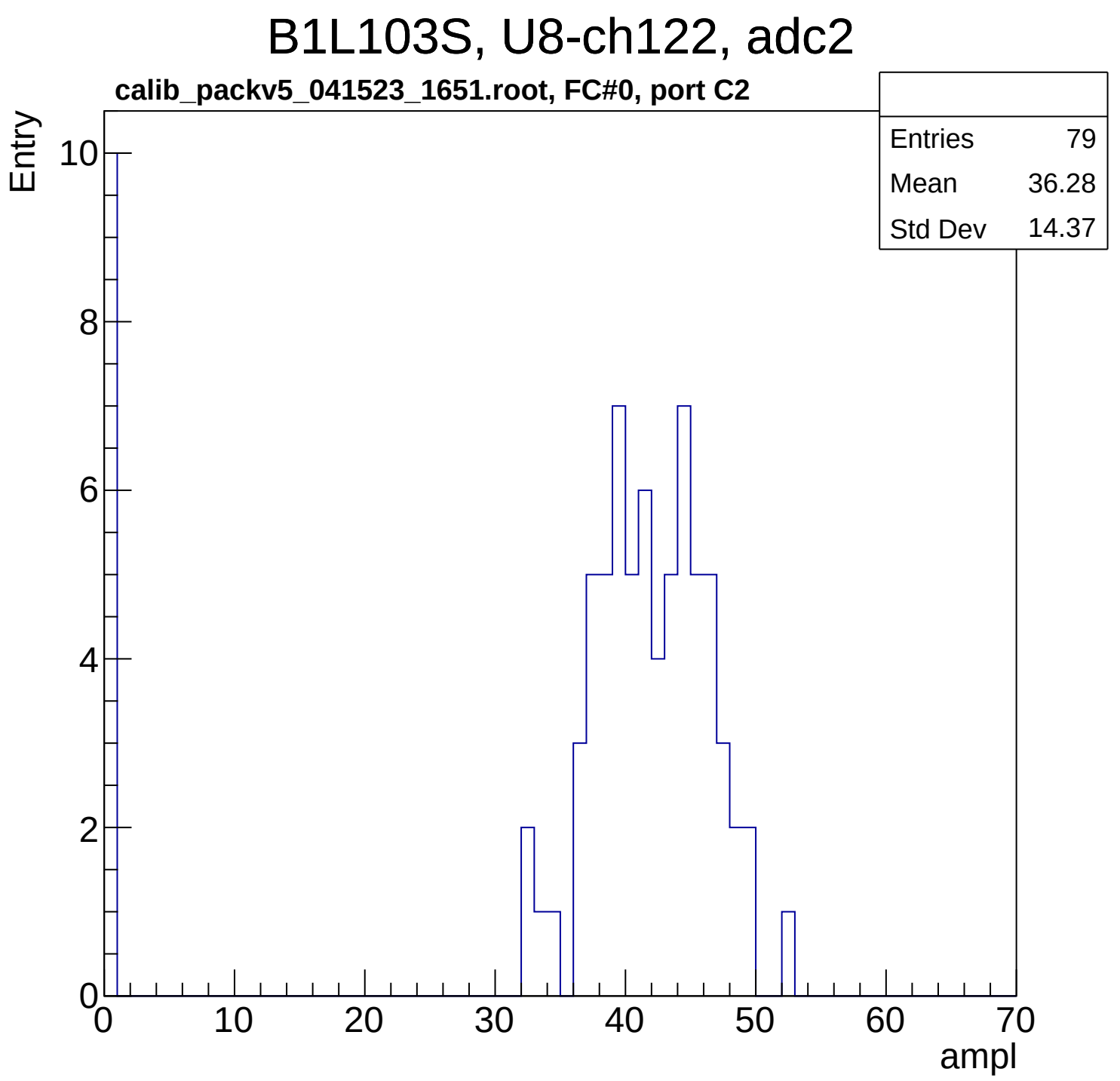
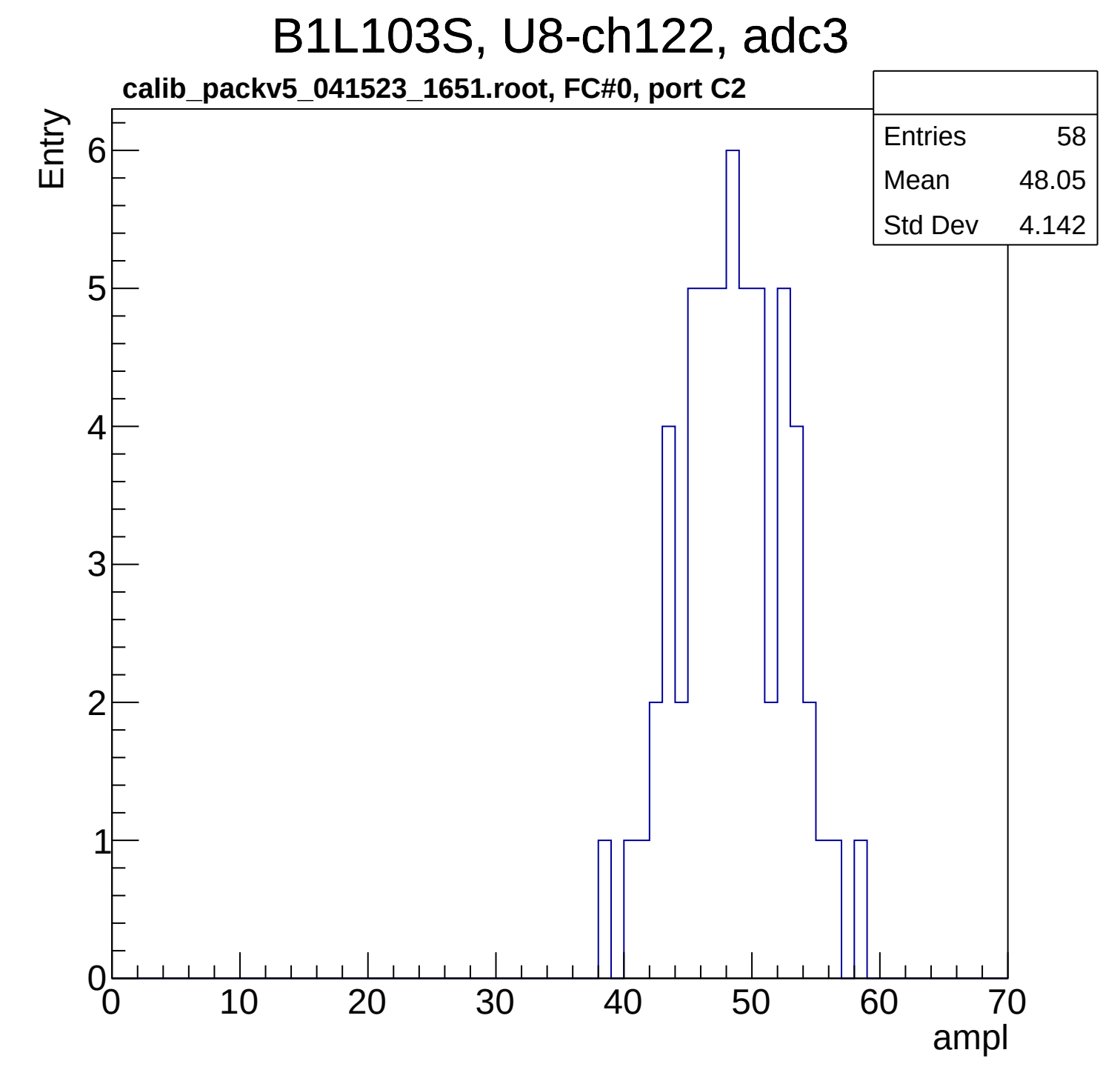

B1L103S, U8-ch122, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 36.28
Std Dev 14.37
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch122, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 48.05
Std Dev 4.142
Entry
ampl
0
1
2
3
4
5
6
0
10
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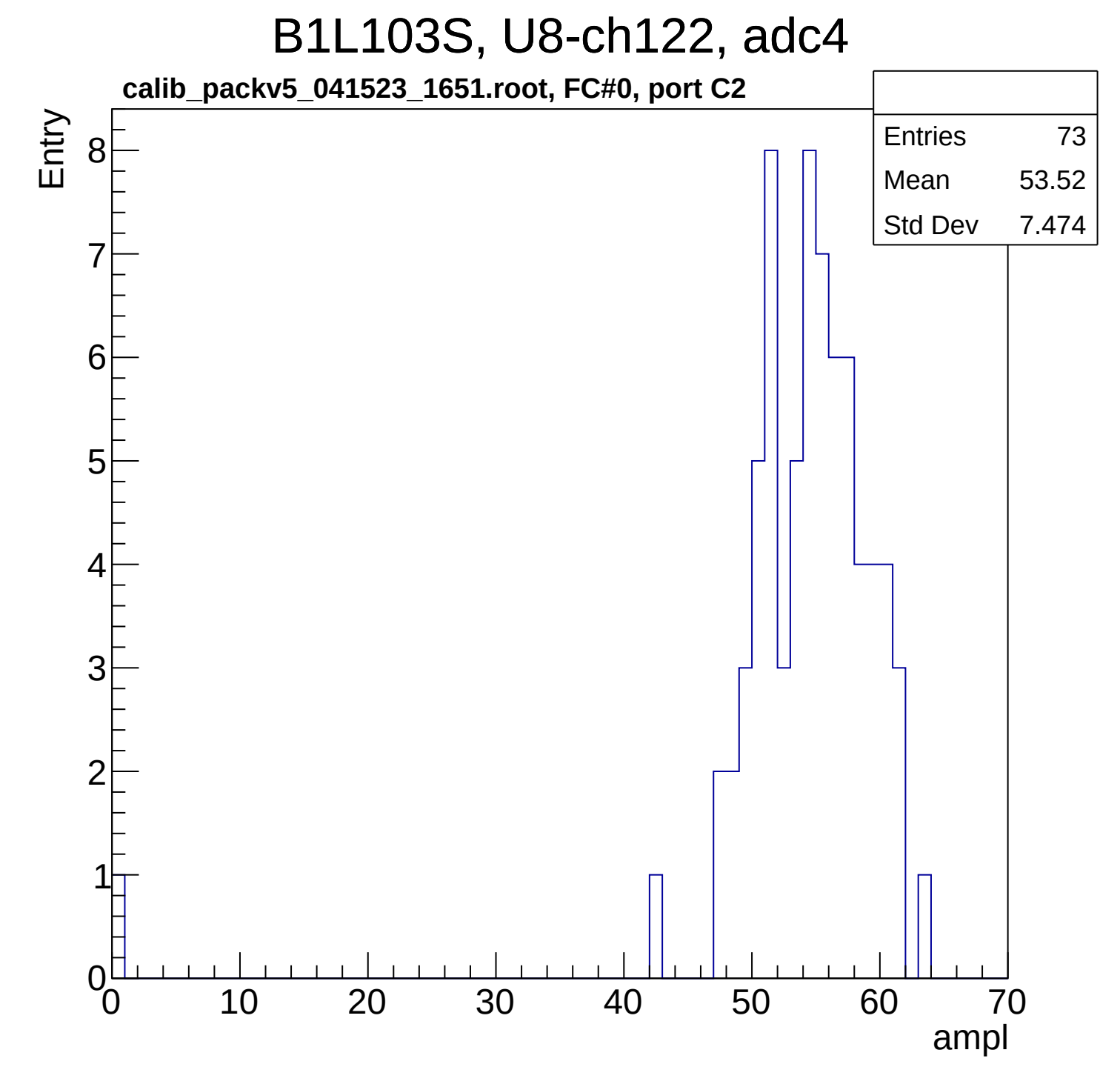
50
60
70


B1L103S, U8-ch122, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 53.52
Std Dev 7.474
Entry
ampl
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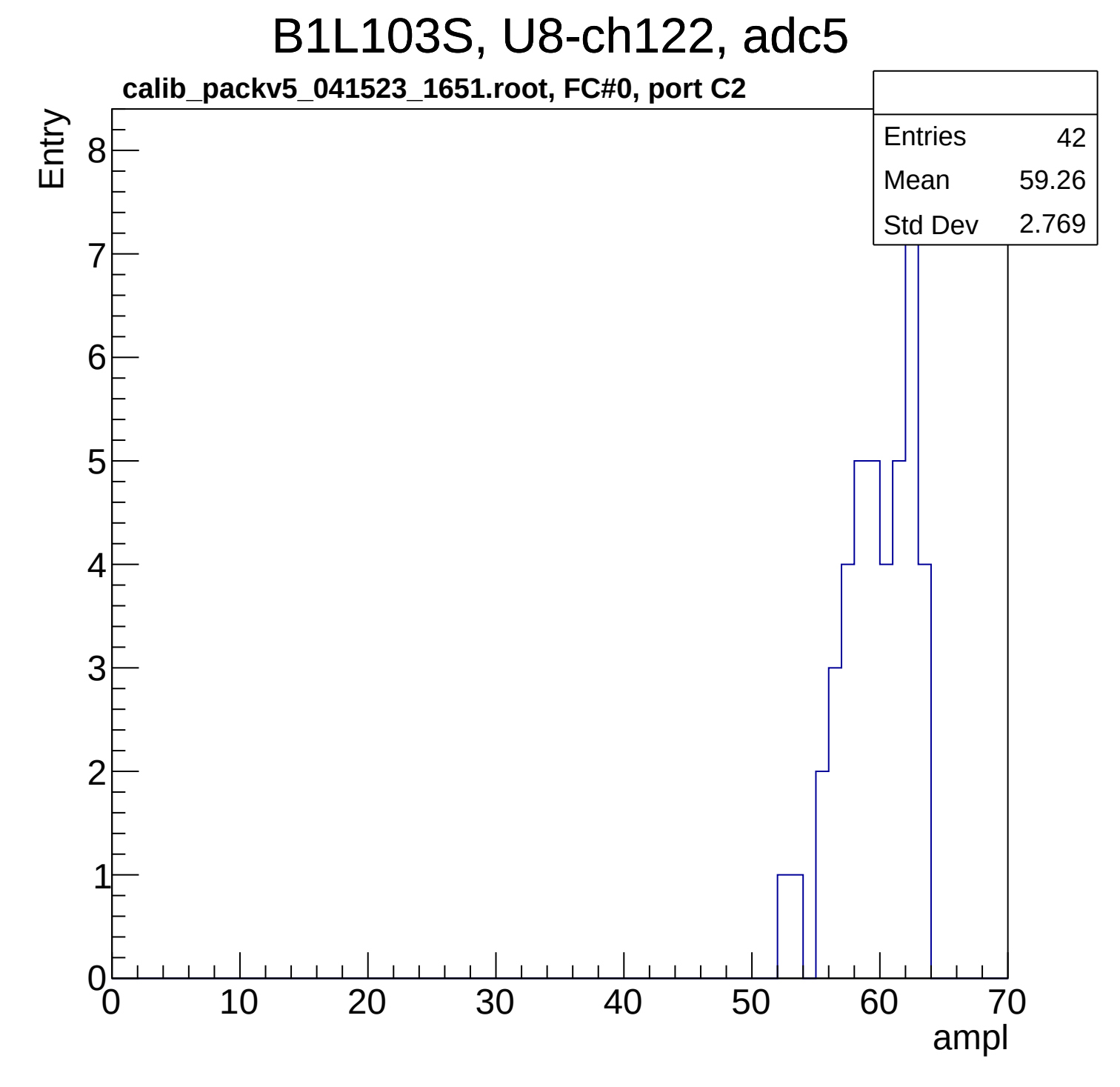
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch122, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 59.26
Std Dev 2.769
Entry
ampl
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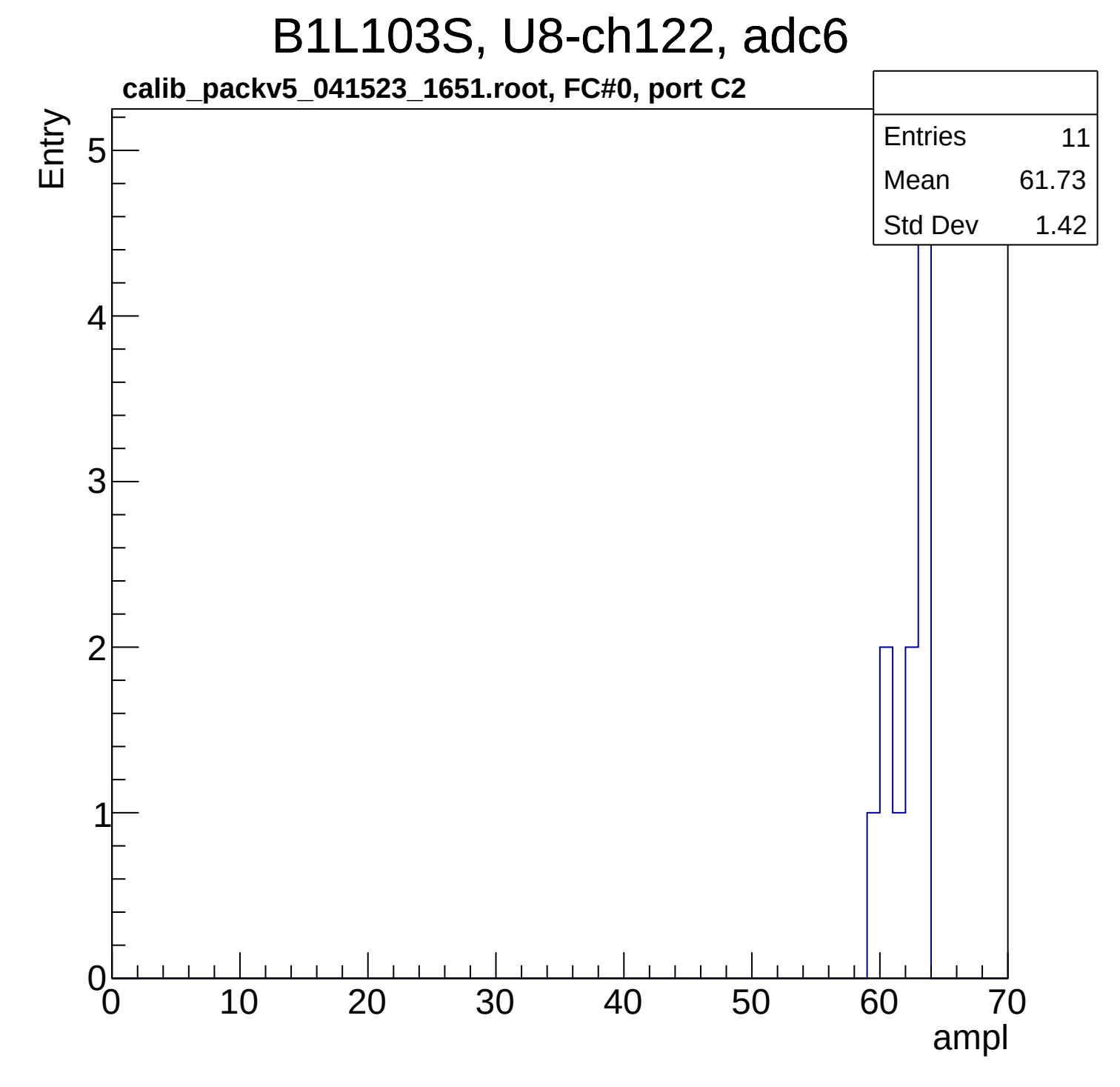
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch122, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 61.73
Std Dev 1.42
Entry
ampl
0
1
2
3
4
5
0
10
20
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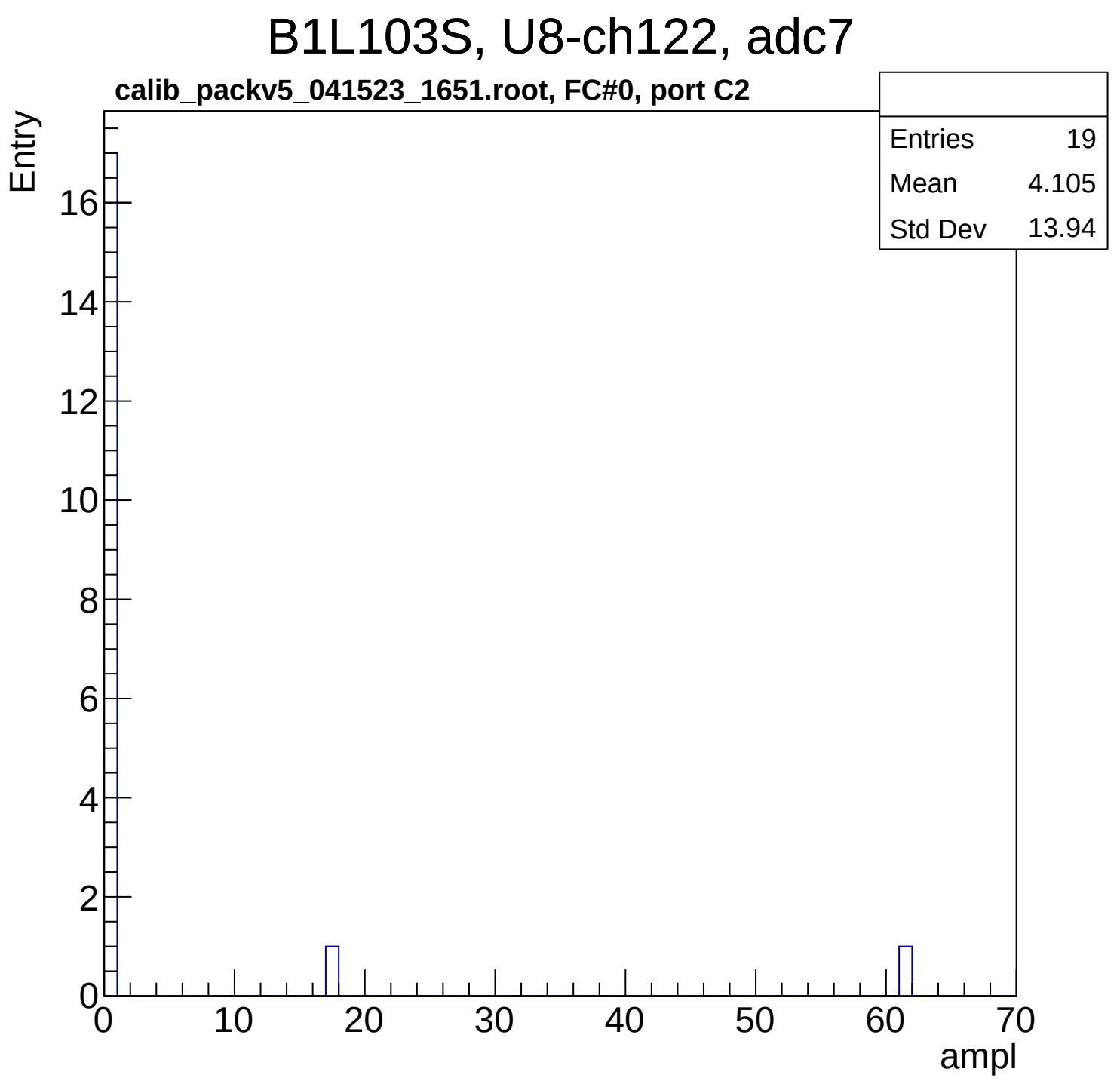
40
50
60
70


B1L103S, U8-ch122, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 4.105
Std Dev 13.94
Entry
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4
6
8
10
12
14
16
0
10
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30
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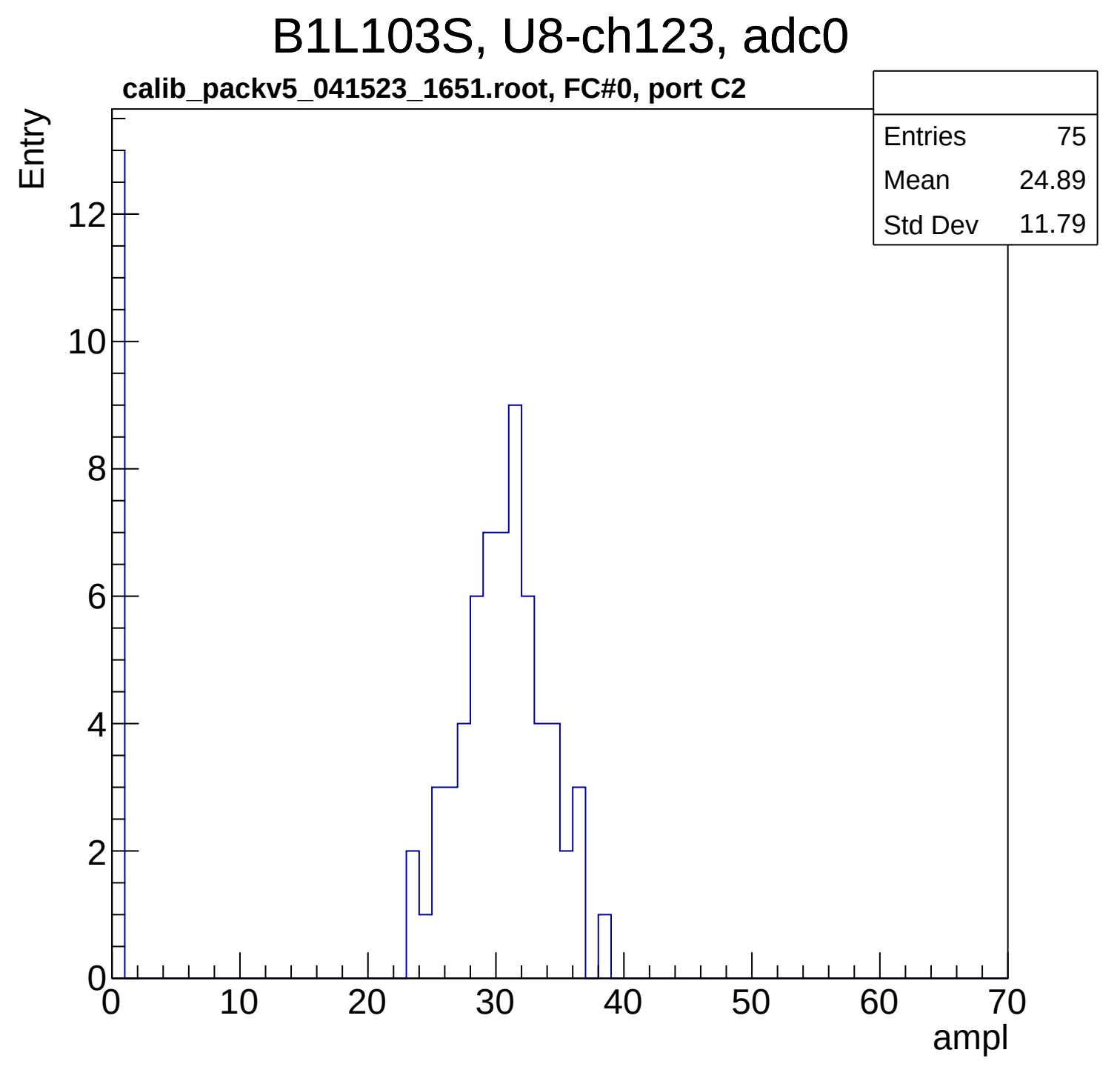
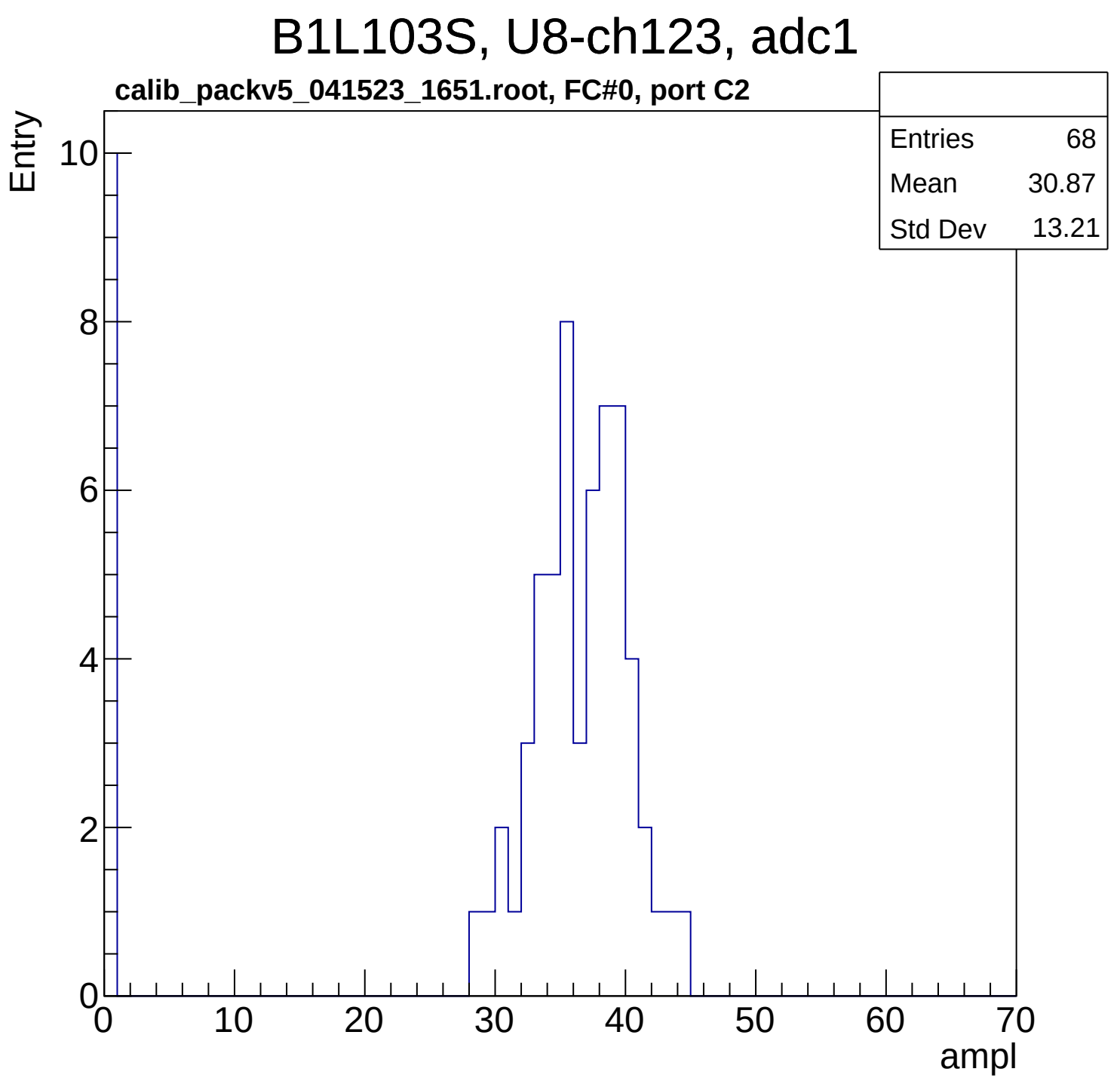
50
60
70
ampl


B1L103S, U8-ch123, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 24.89
Std Dev 11.79
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch123, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 30.87
Std Dev 13.21
Entry
ampl
0
2
4
6
8
10
0
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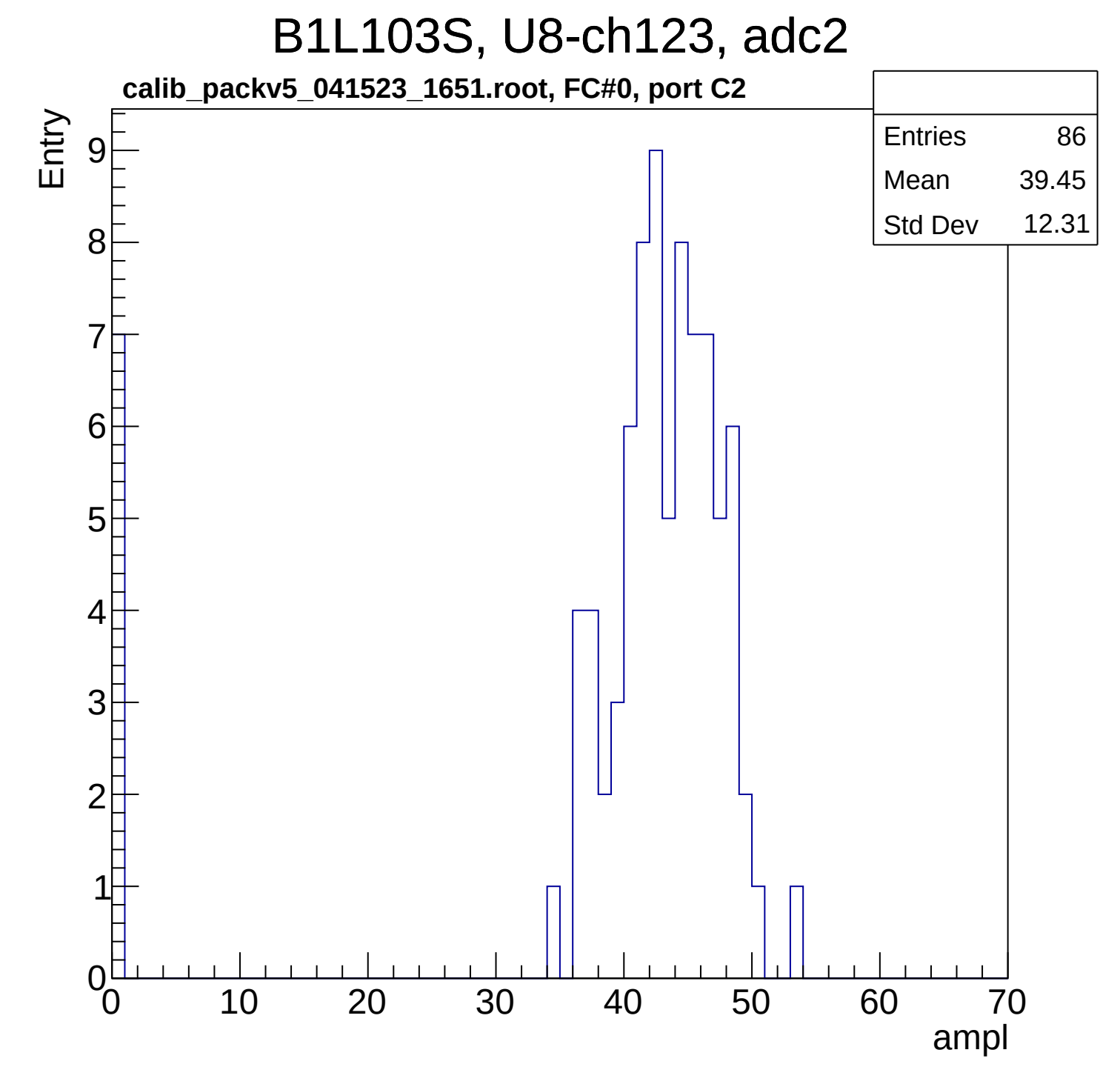
B1L103S, U8-ch123, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 39.45
Std Dev 12.31
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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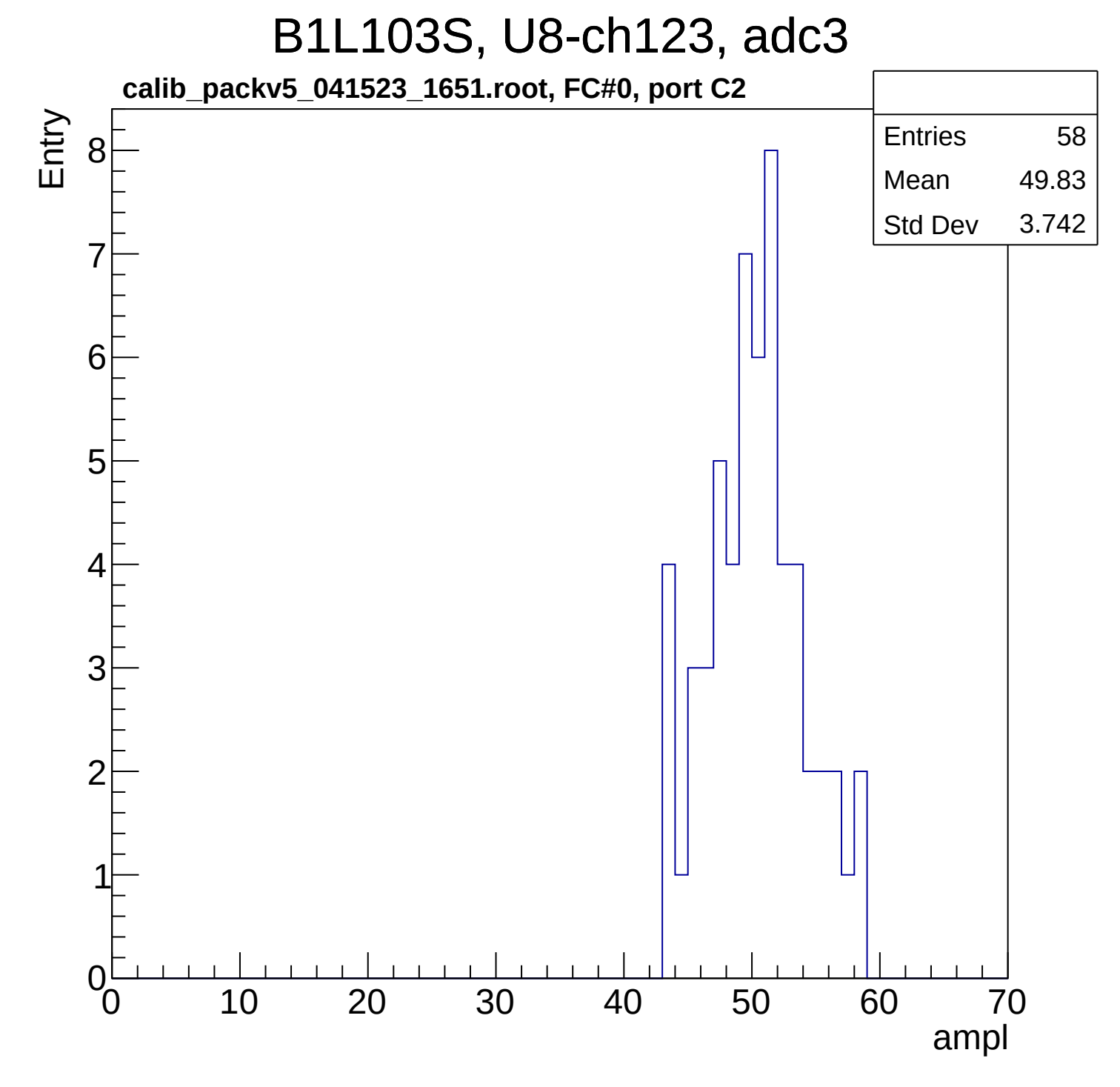
B1L103S, U8-ch123, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 49.83
Std Dev 3.742
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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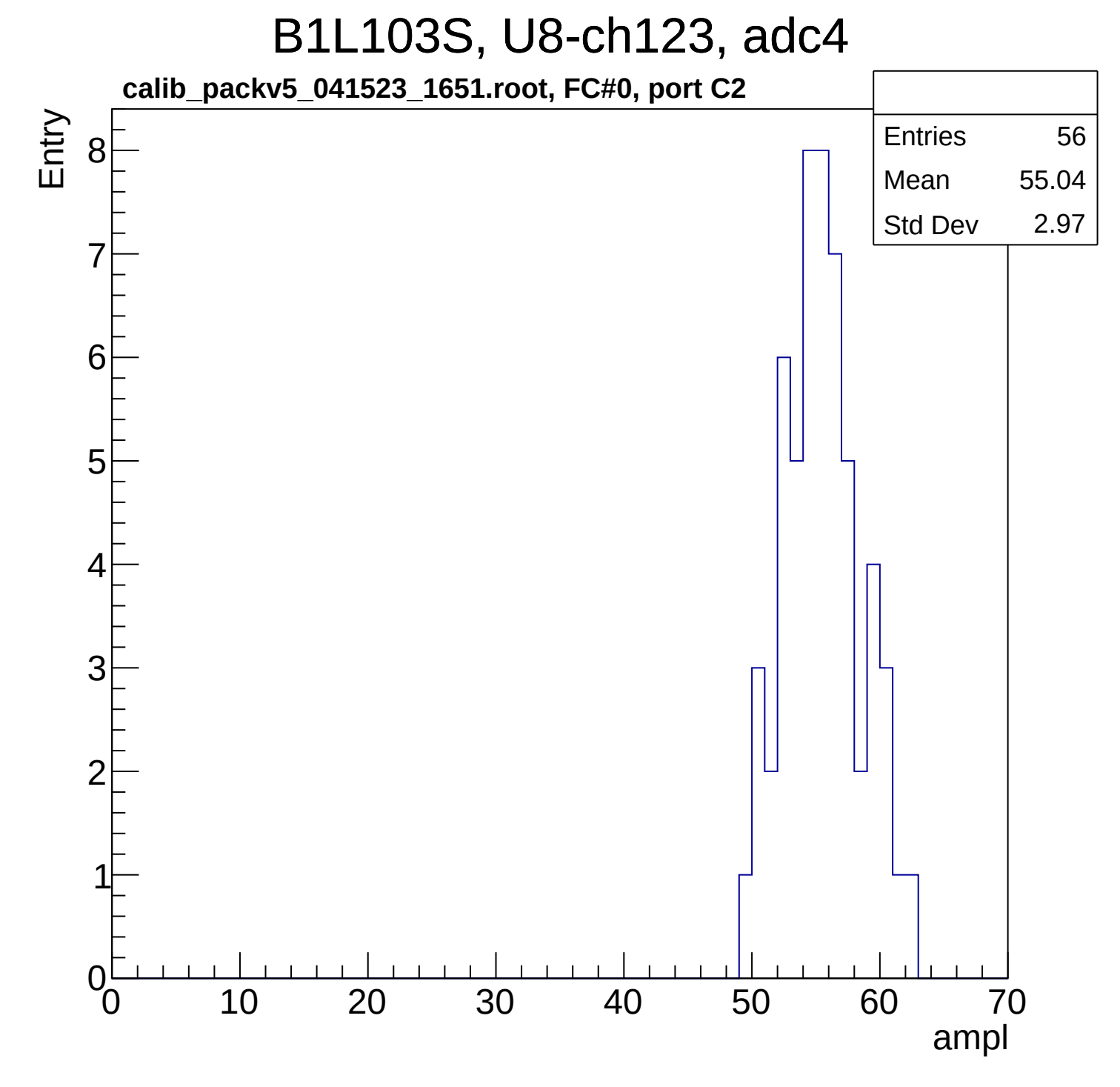
B1L103S, U8-ch123, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 55.04
Std Dev 2.97
Entry
ampl
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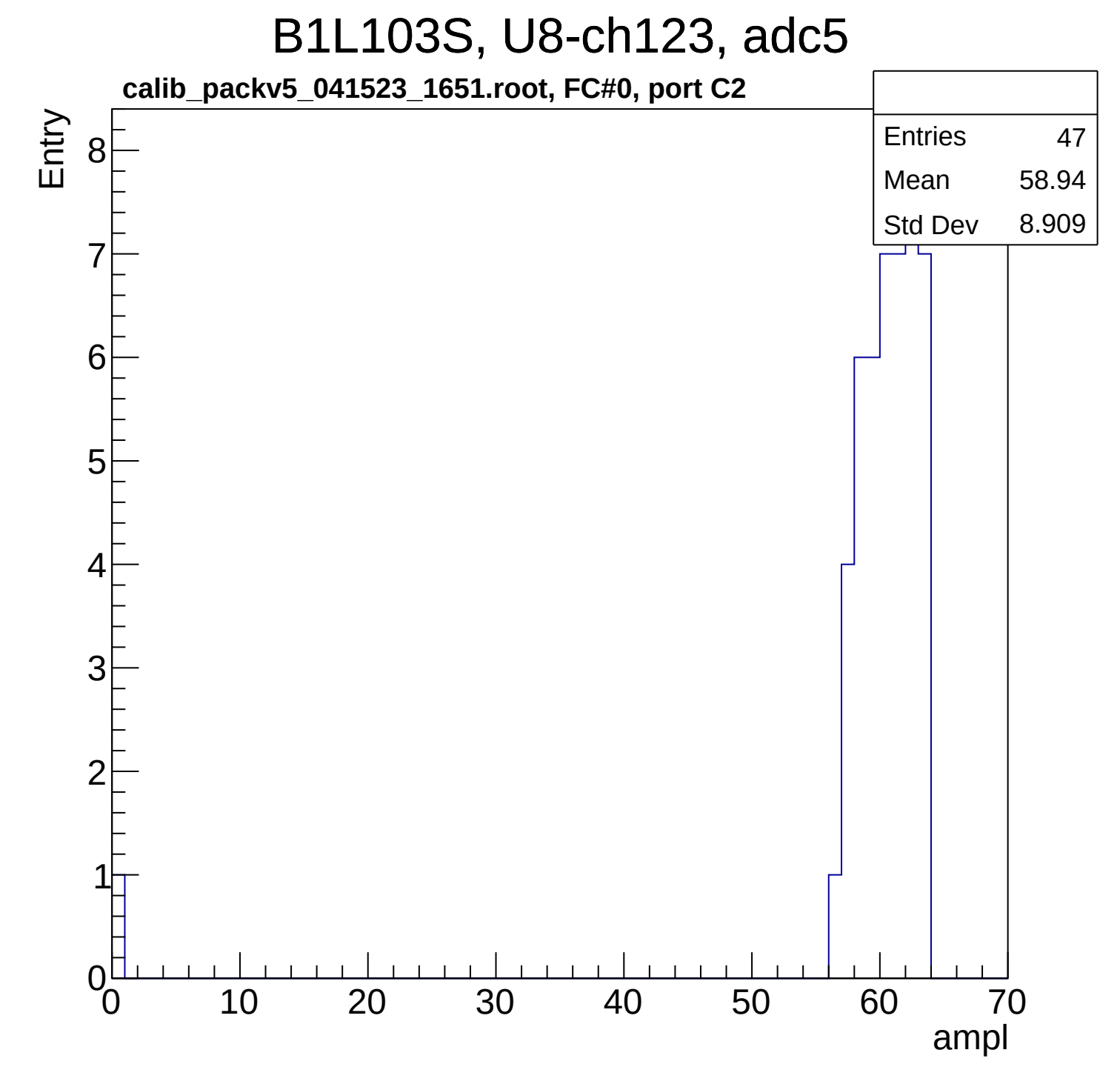
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch123, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 58.94
Std Dev 8.909
Entry
ampl
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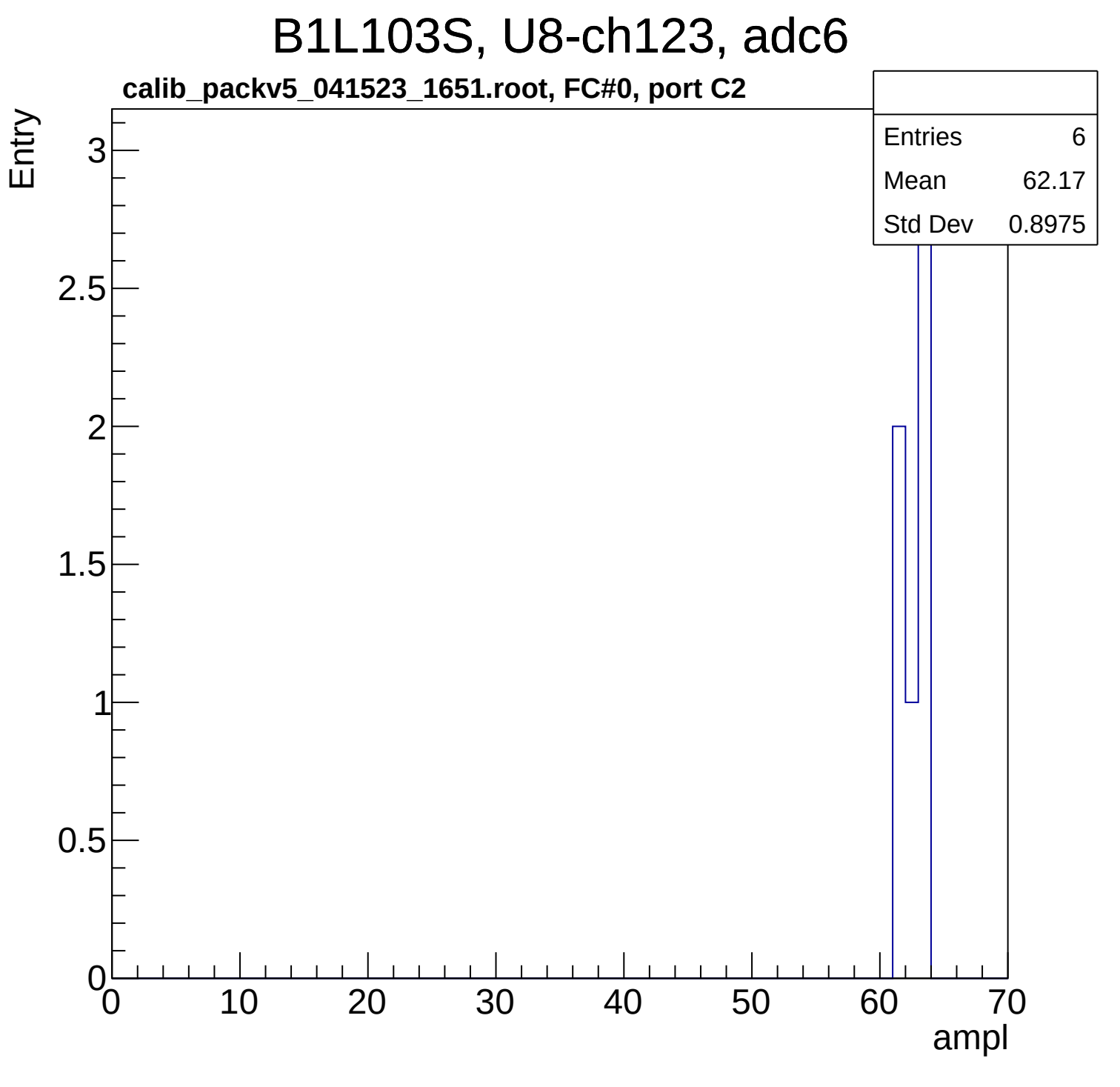
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch123, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 62.17
Std Dev 0.8975
Entry
ampl
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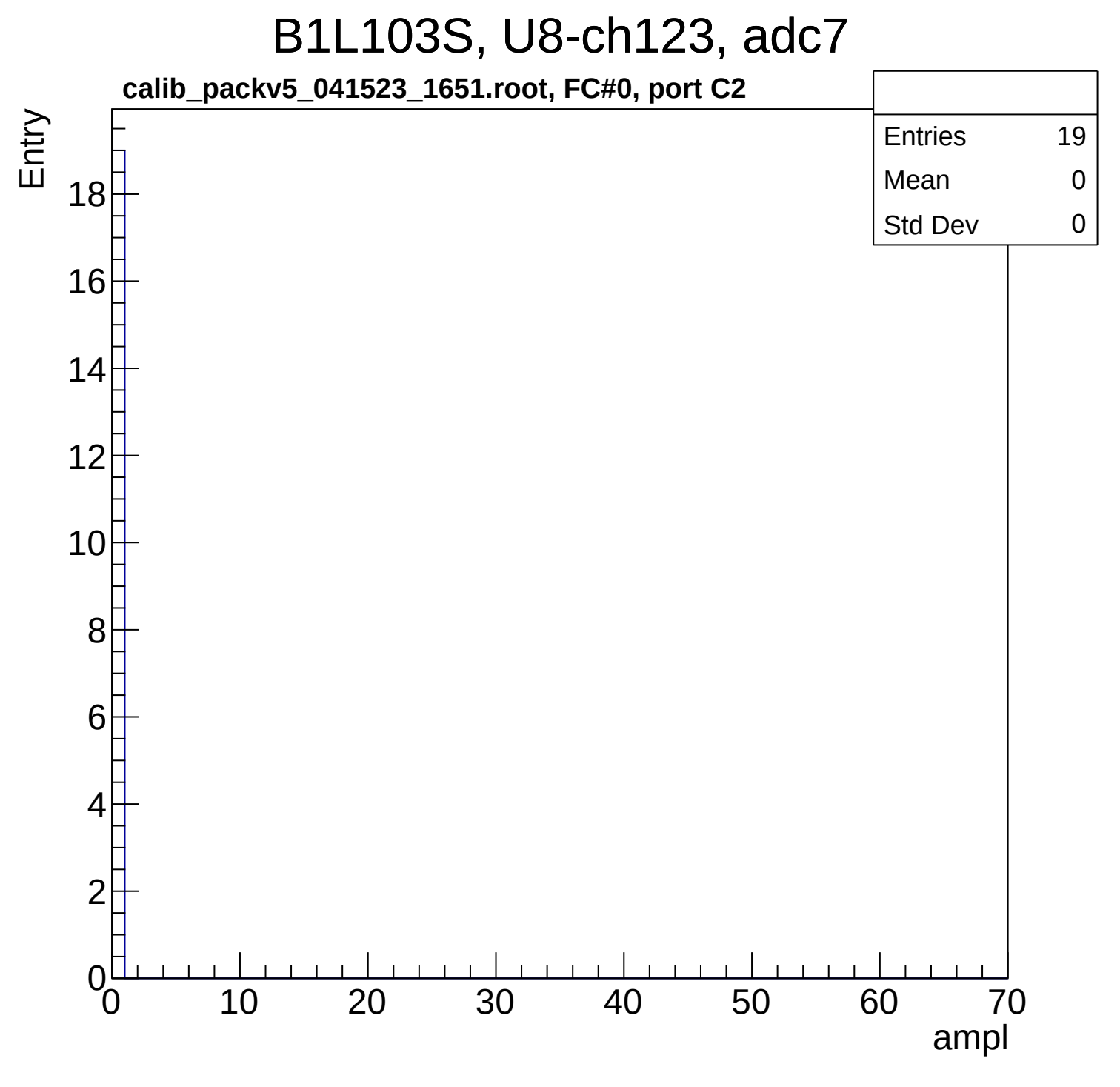
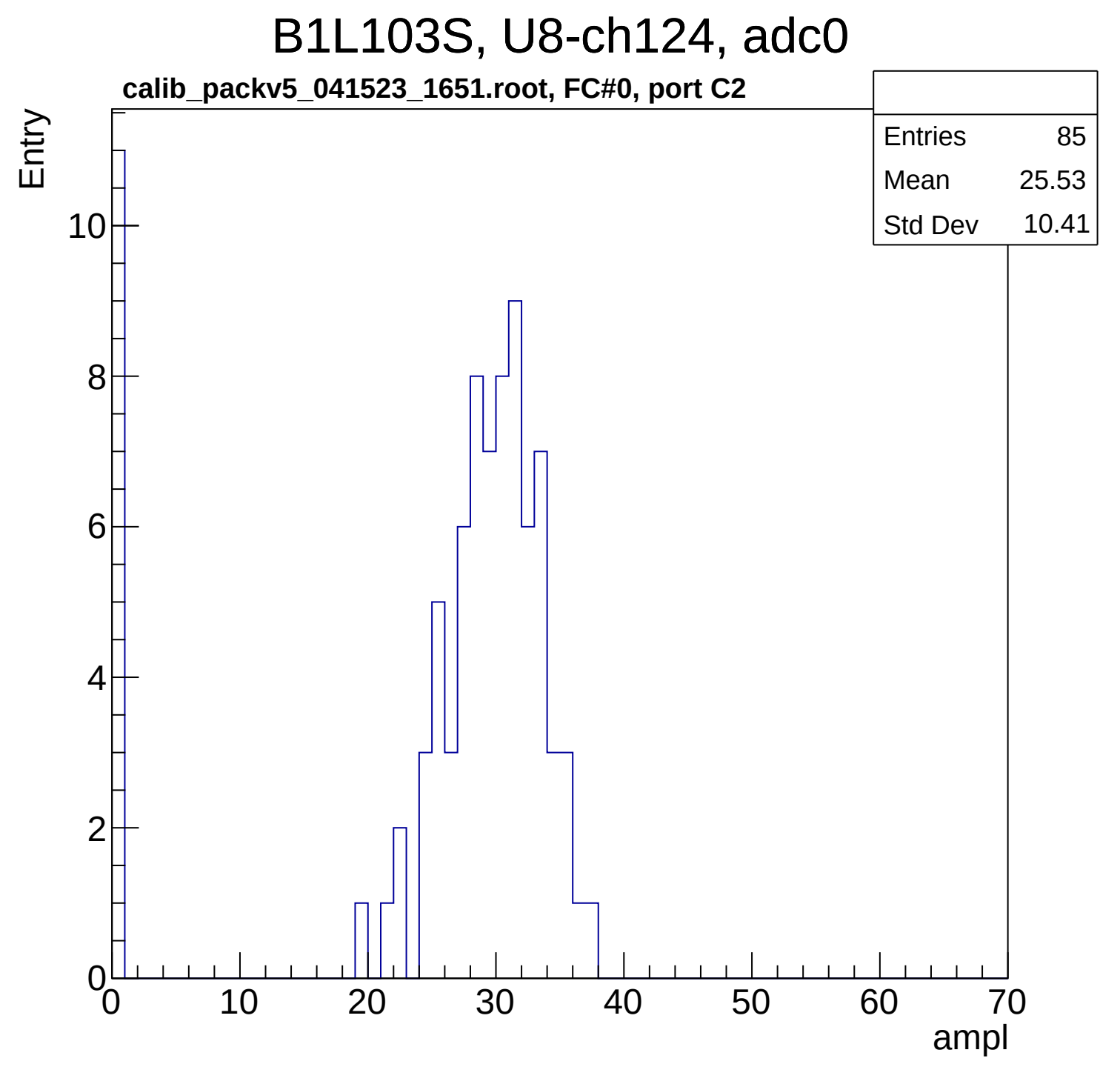
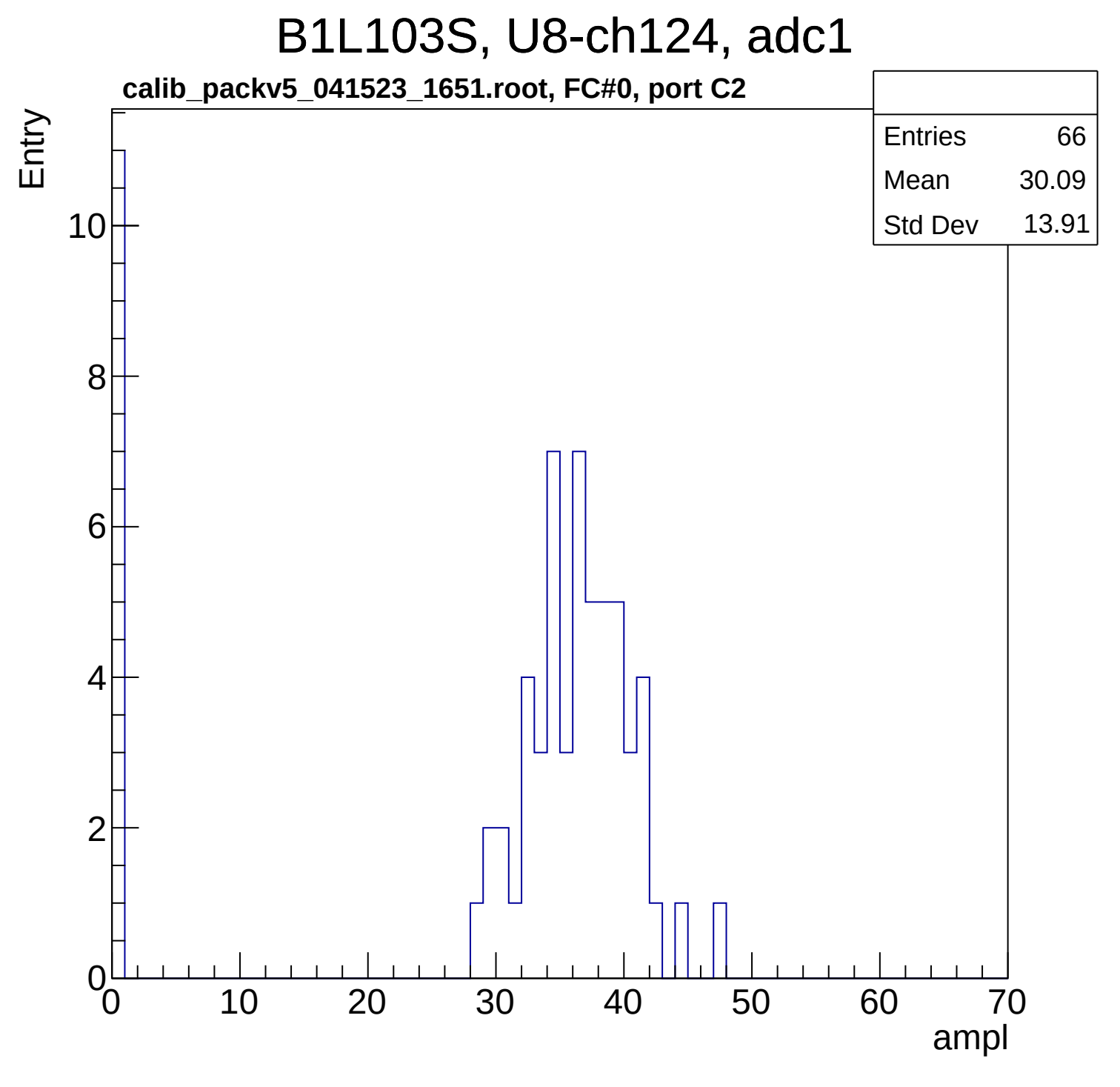
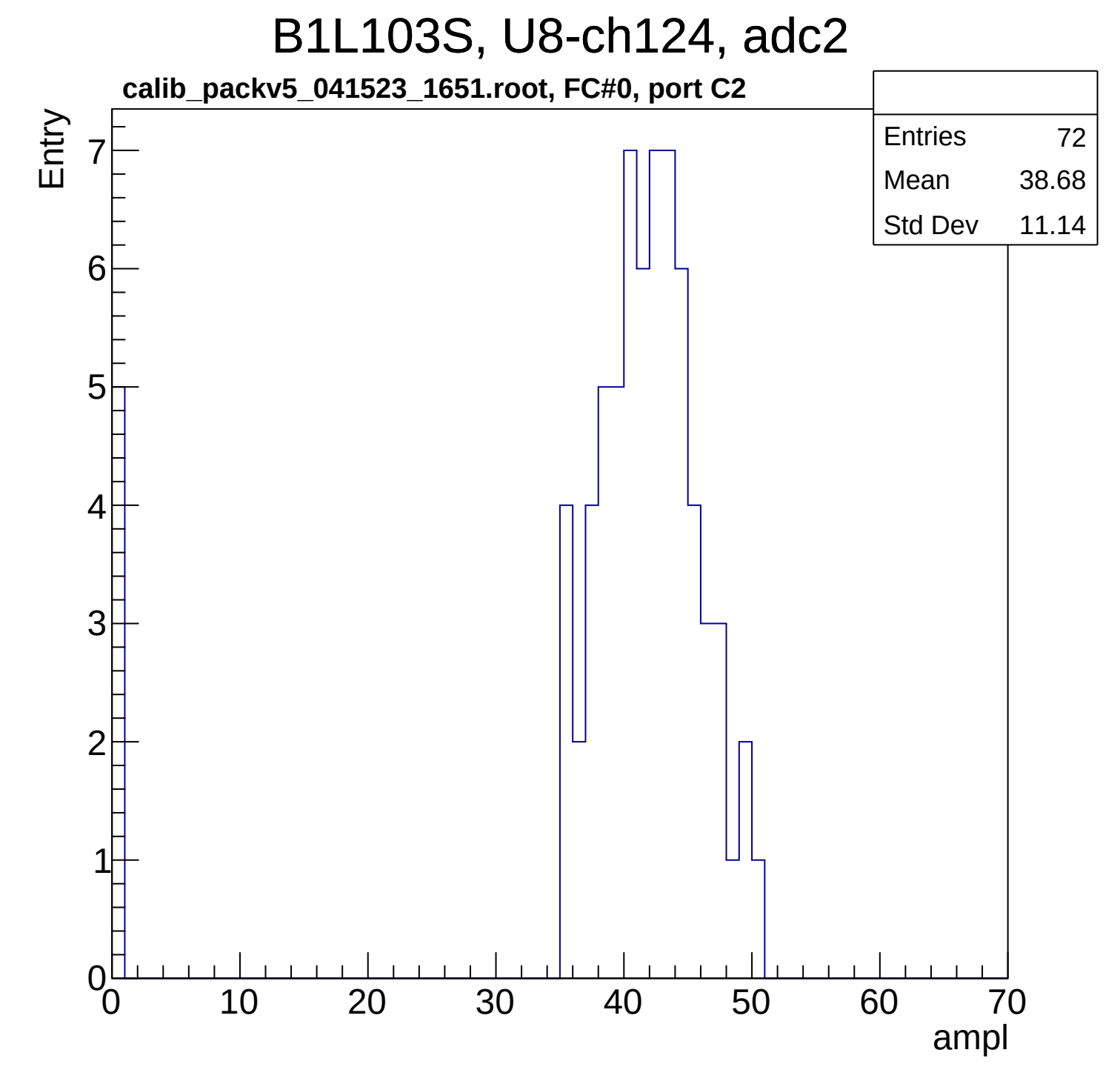
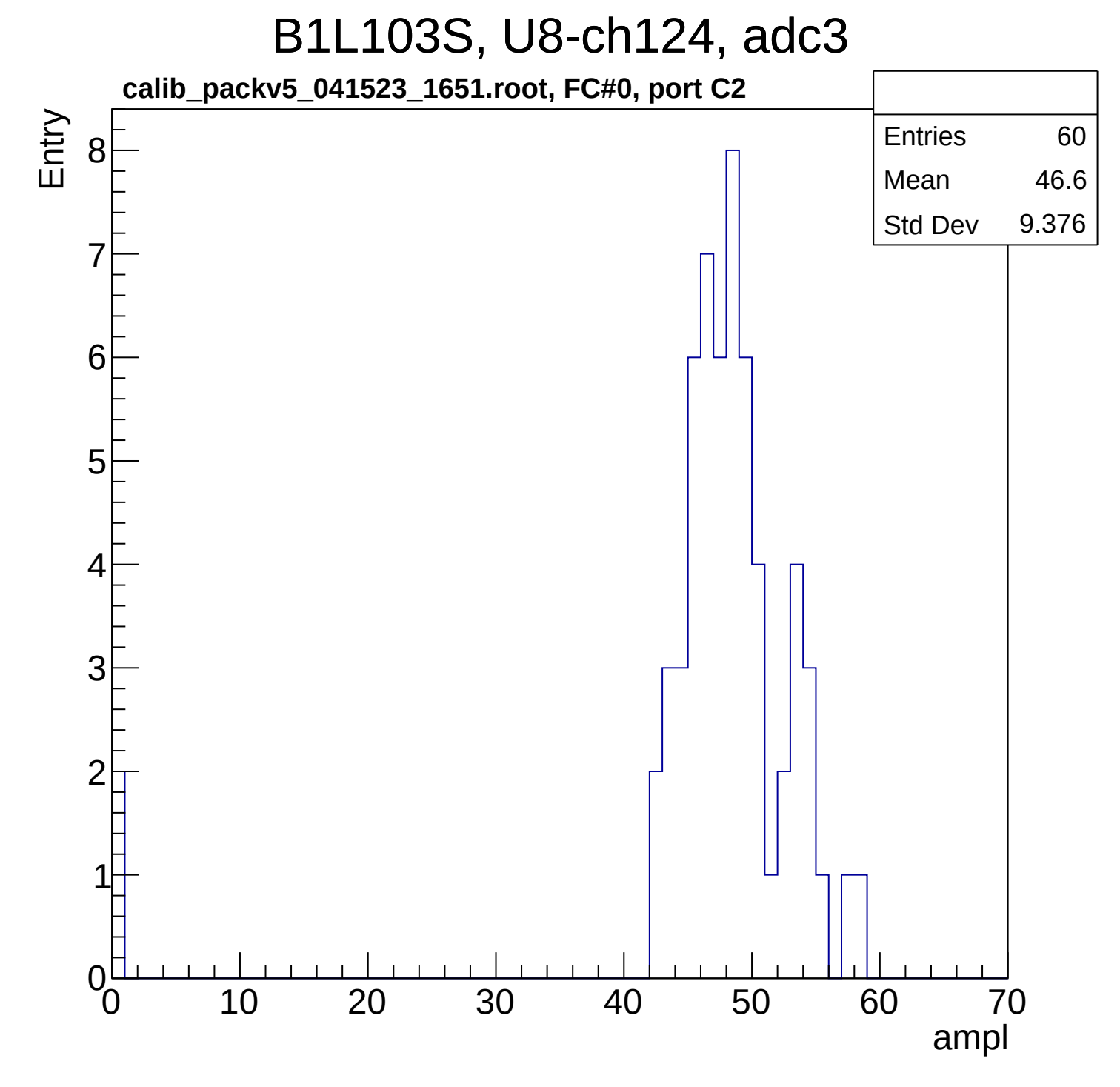
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U8-ch123, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch124, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 25.53
Std Dev 10.41
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch124, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 30.09
Std Dev 13.91
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch124, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 38.68
Std Dev 11.14
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U8-ch124, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 46.6
Std Dev 9.376
Entry
ampl
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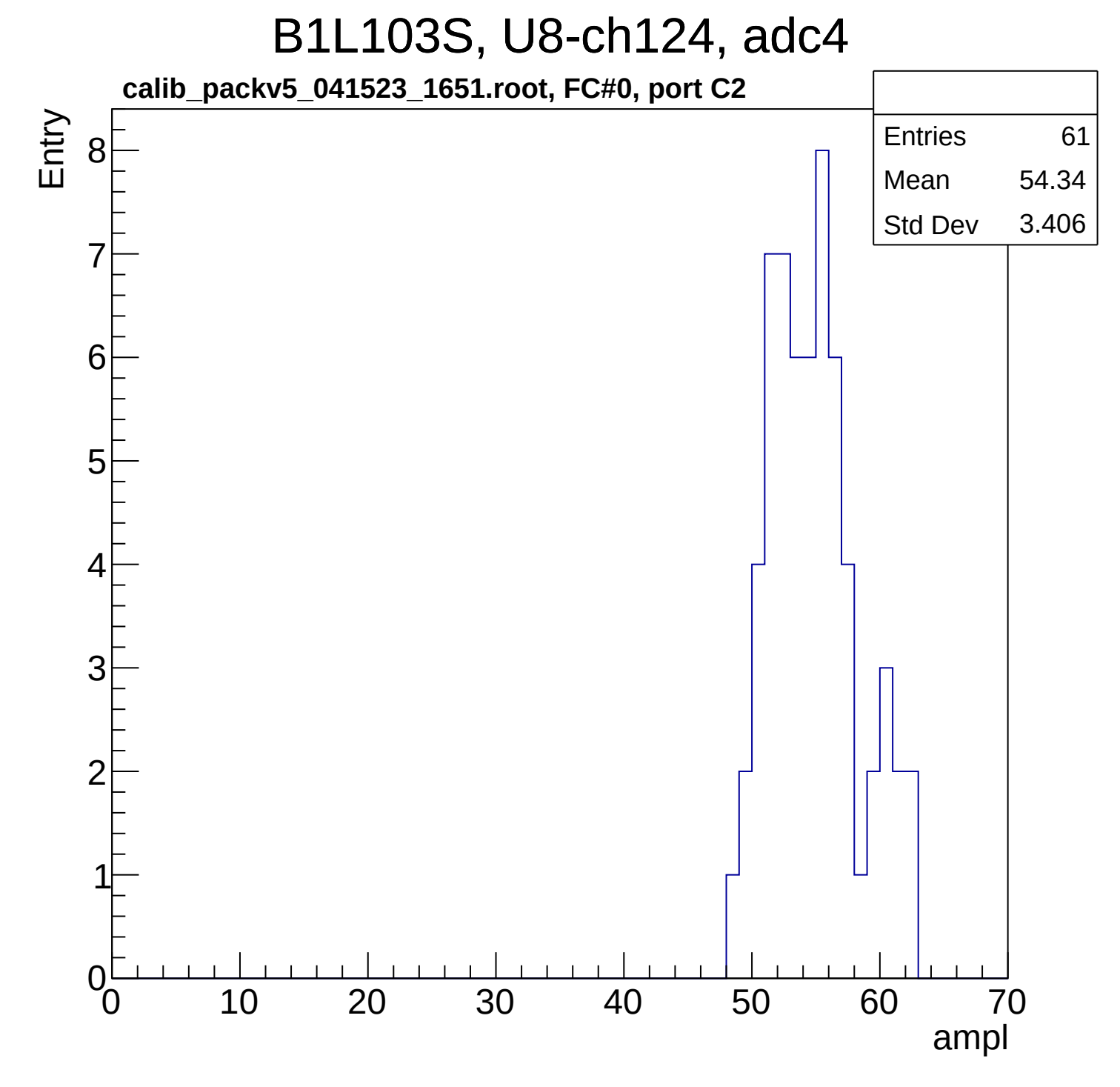
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch124, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 54.34
Std Dev 3.406
Entry
ampl
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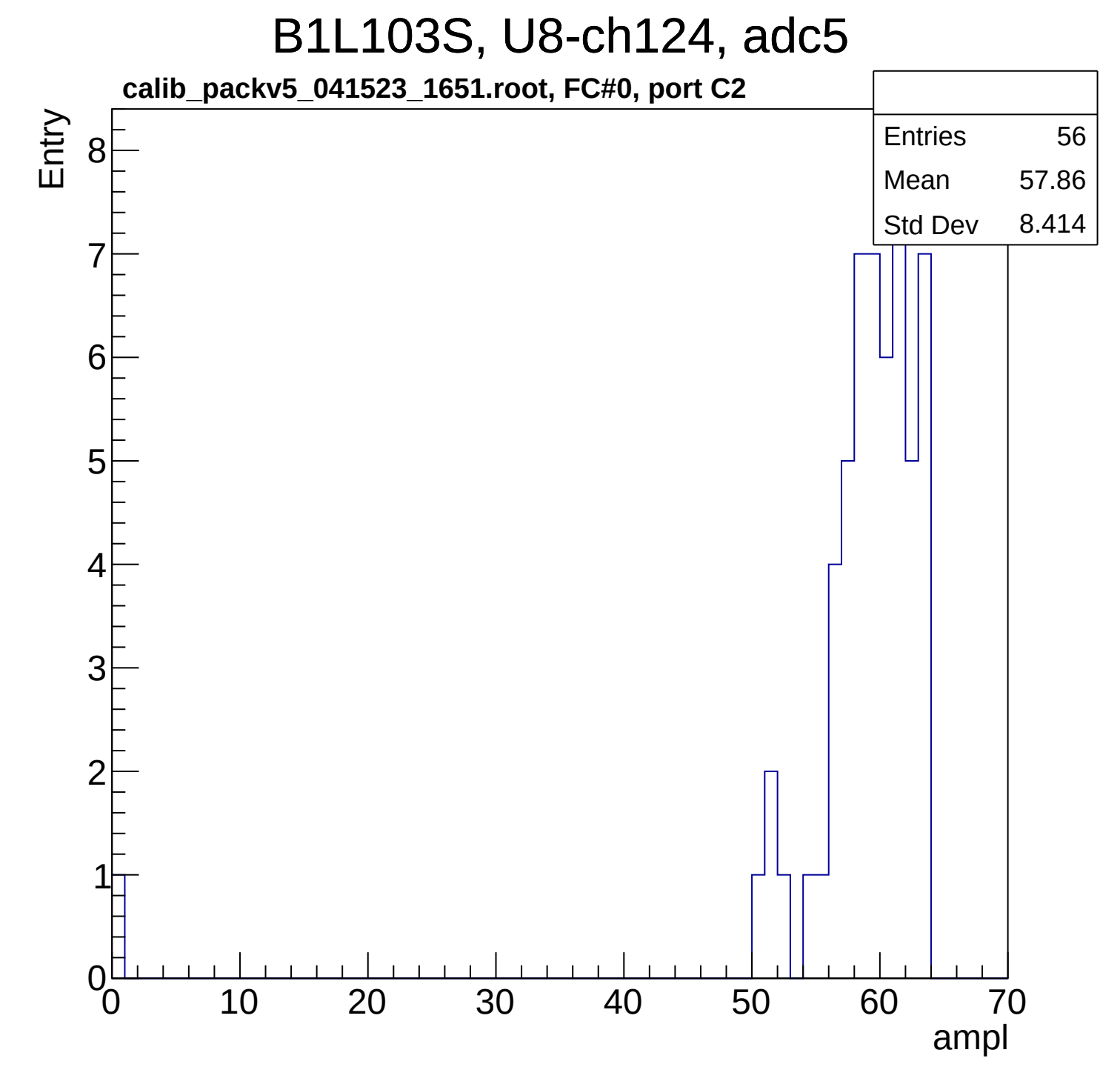
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch124, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 57.86
Std Dev 8.414
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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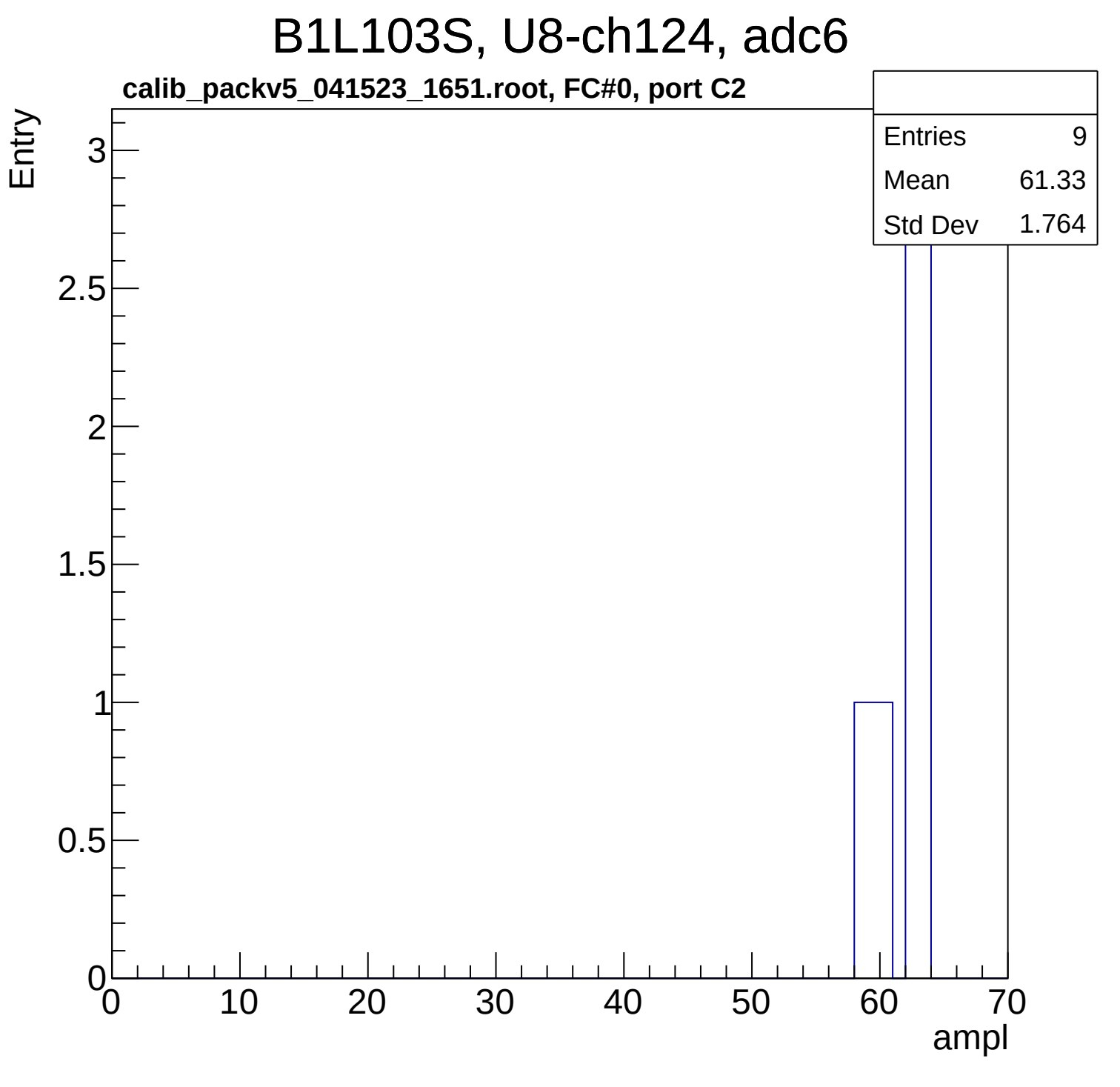
B1L103S, U8-ch124, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 61.33
Std Dev 1.764
Entry
ampl
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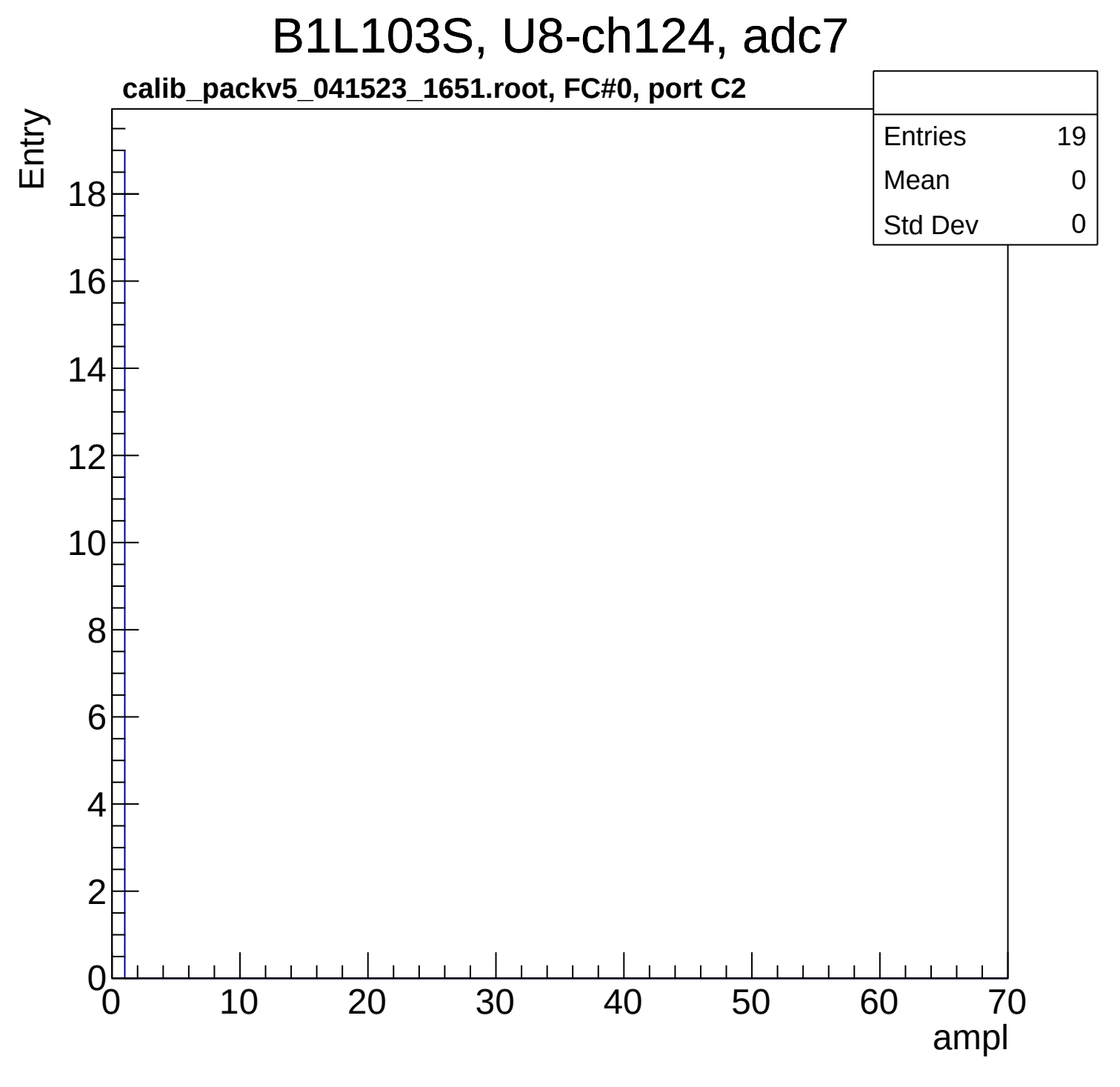
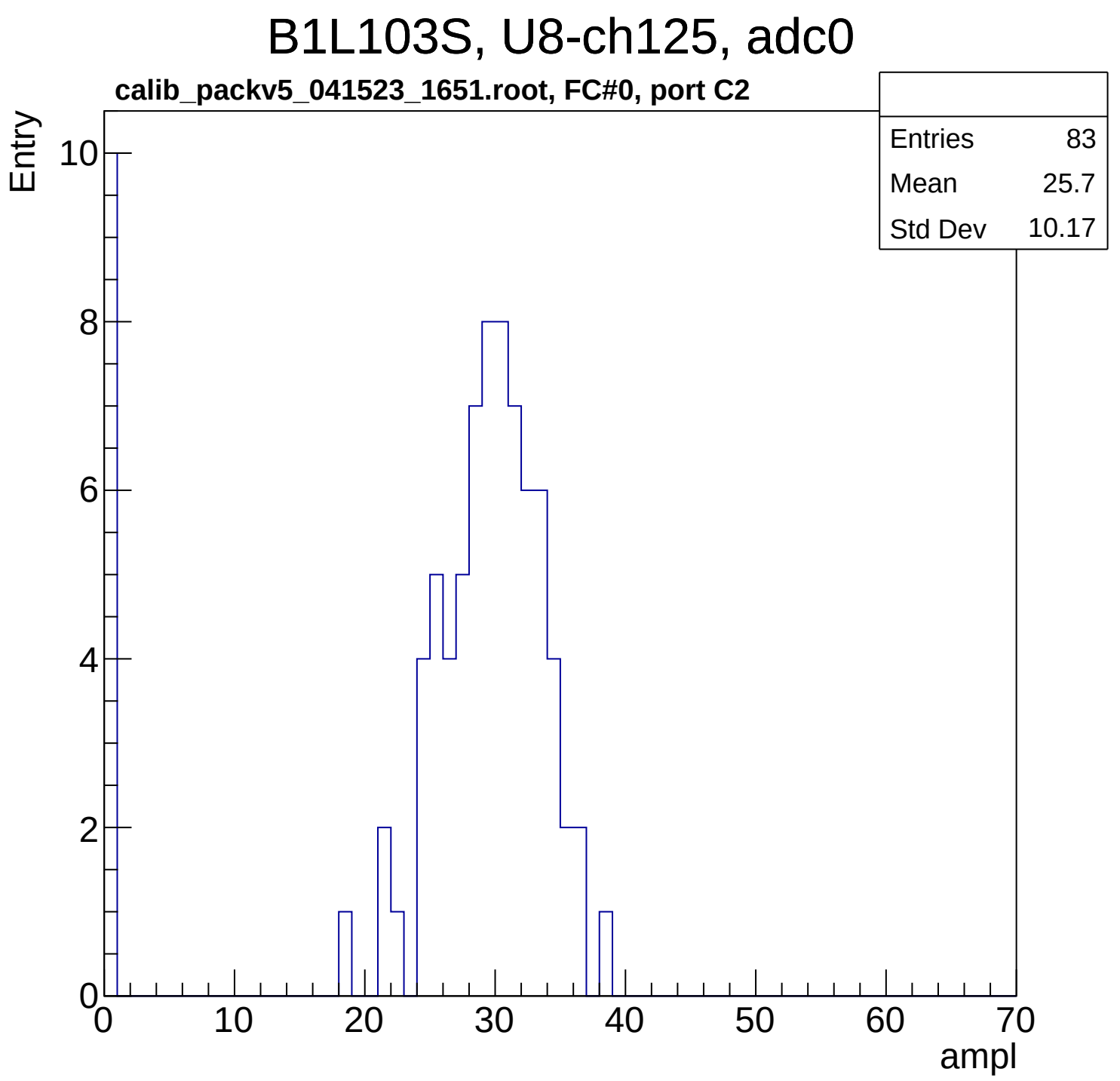
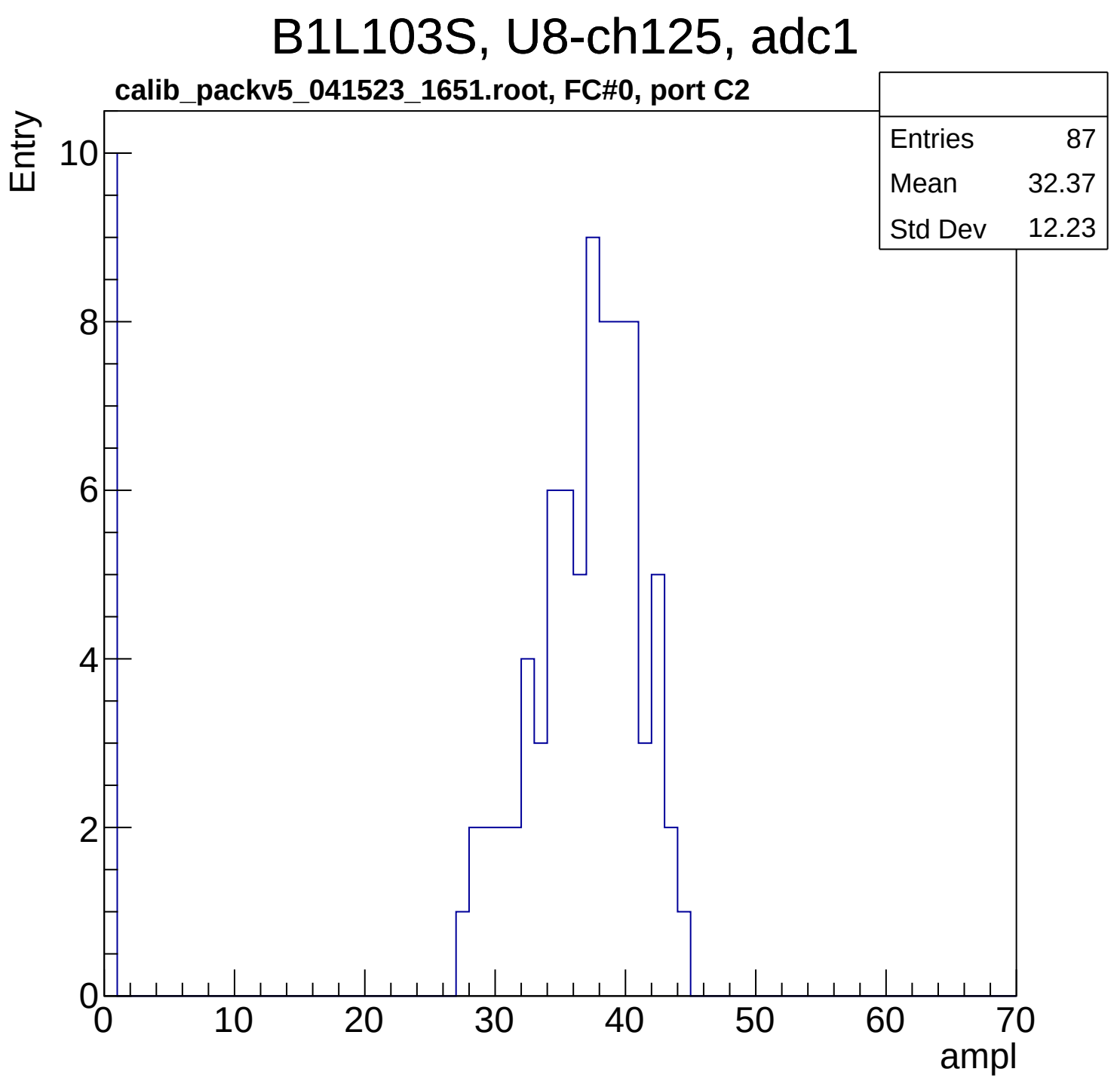
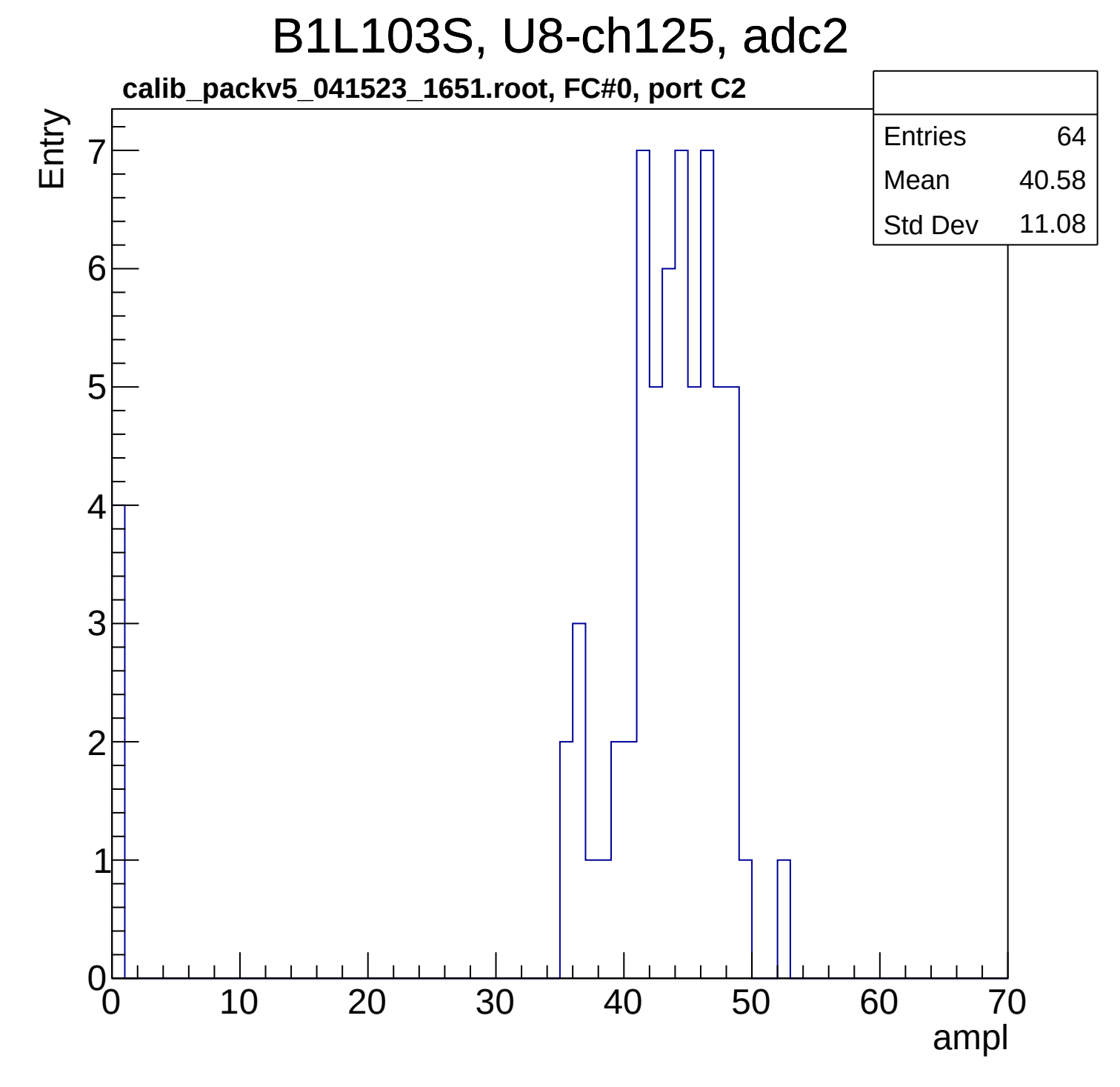
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U8-ch124, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch125, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 25.7
Std Dev 10.17
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U8-ch125, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 32.37
Std Dev 12.23
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U8-ch125, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 40.58
Std Dev 11.08
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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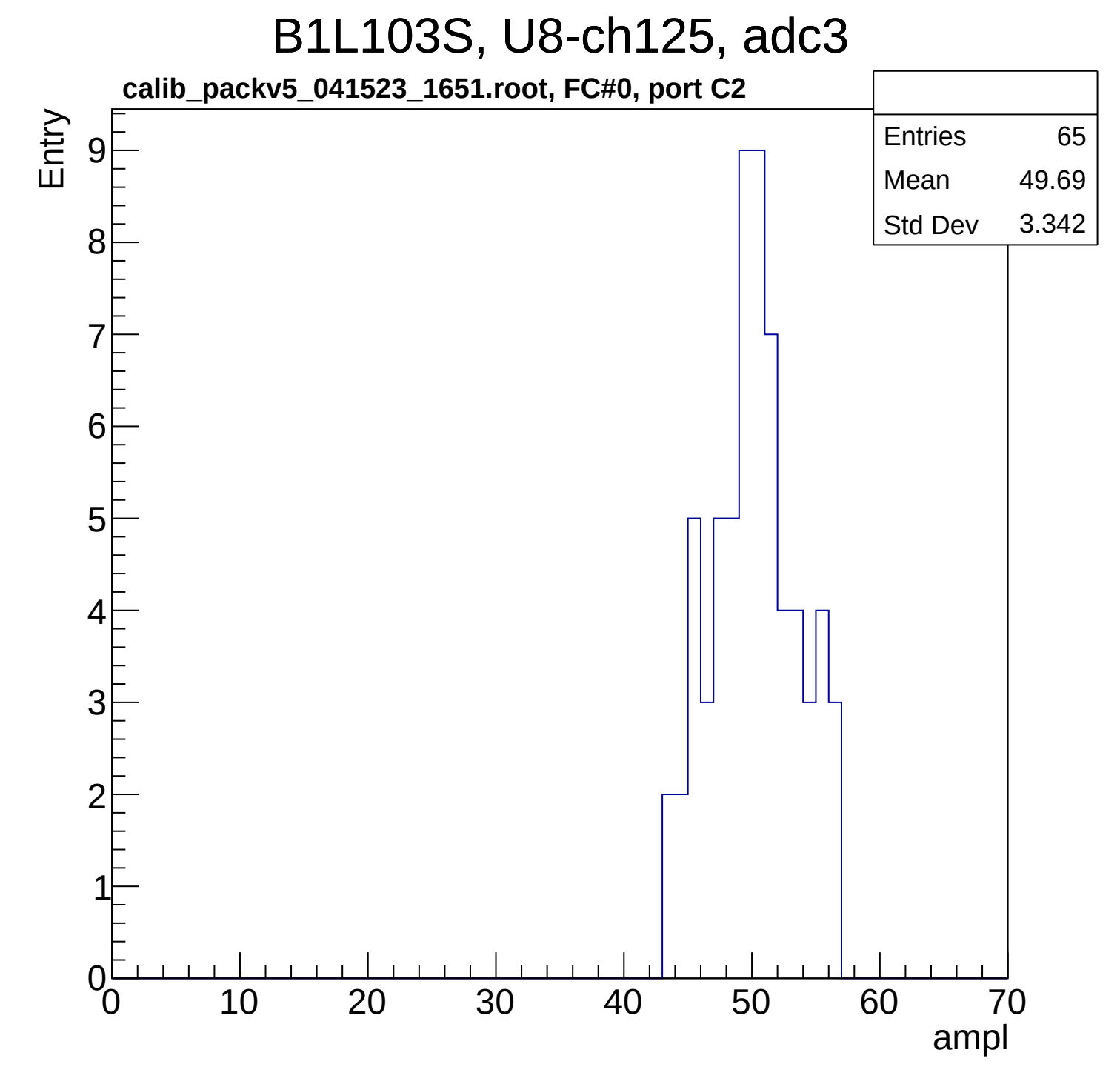
B1L103S, U8-ch125, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 49.69
Std Dev 3.342
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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60
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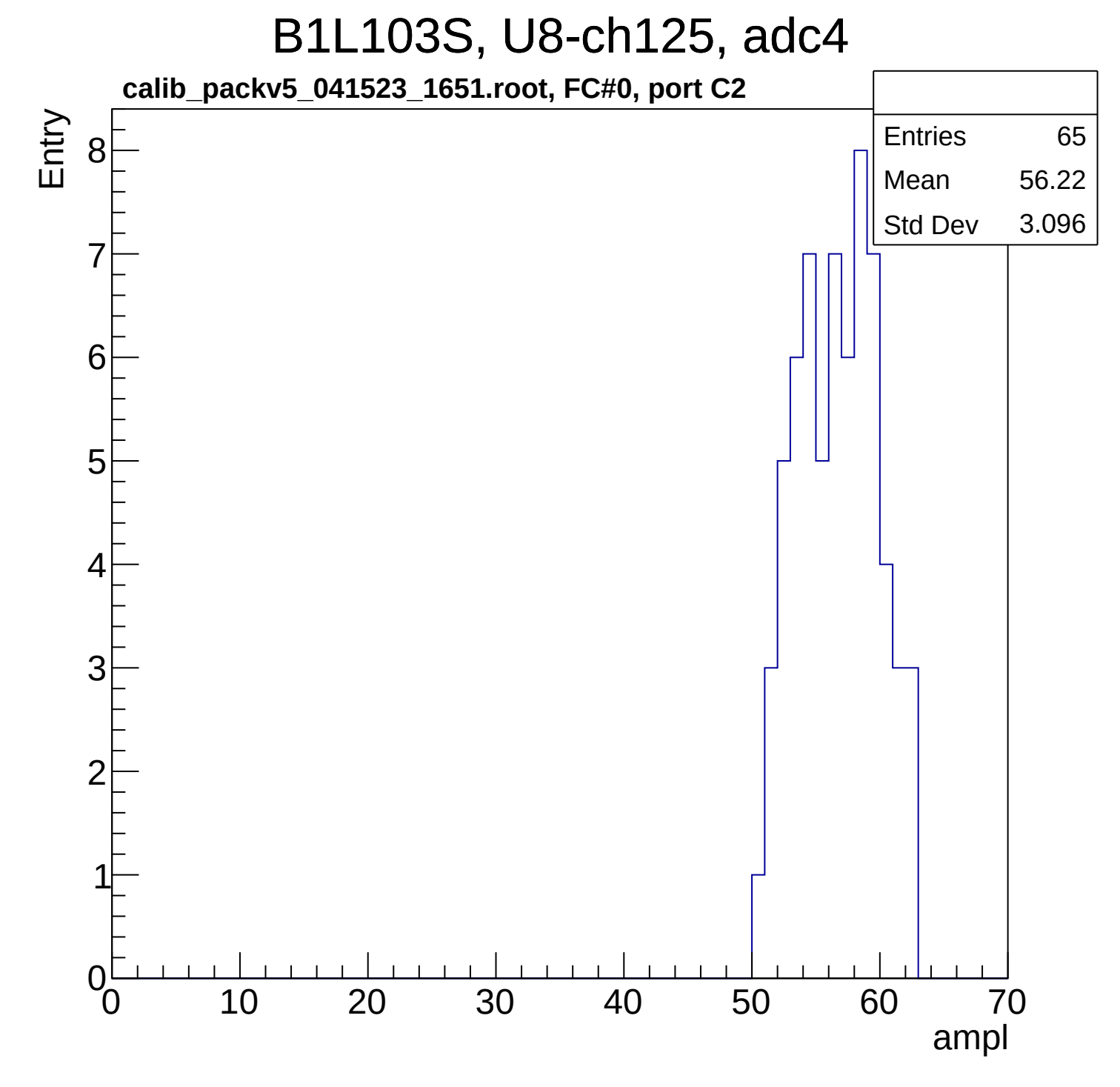
B1L103S, U8-ch125, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 56.22
Std Dev 3.096
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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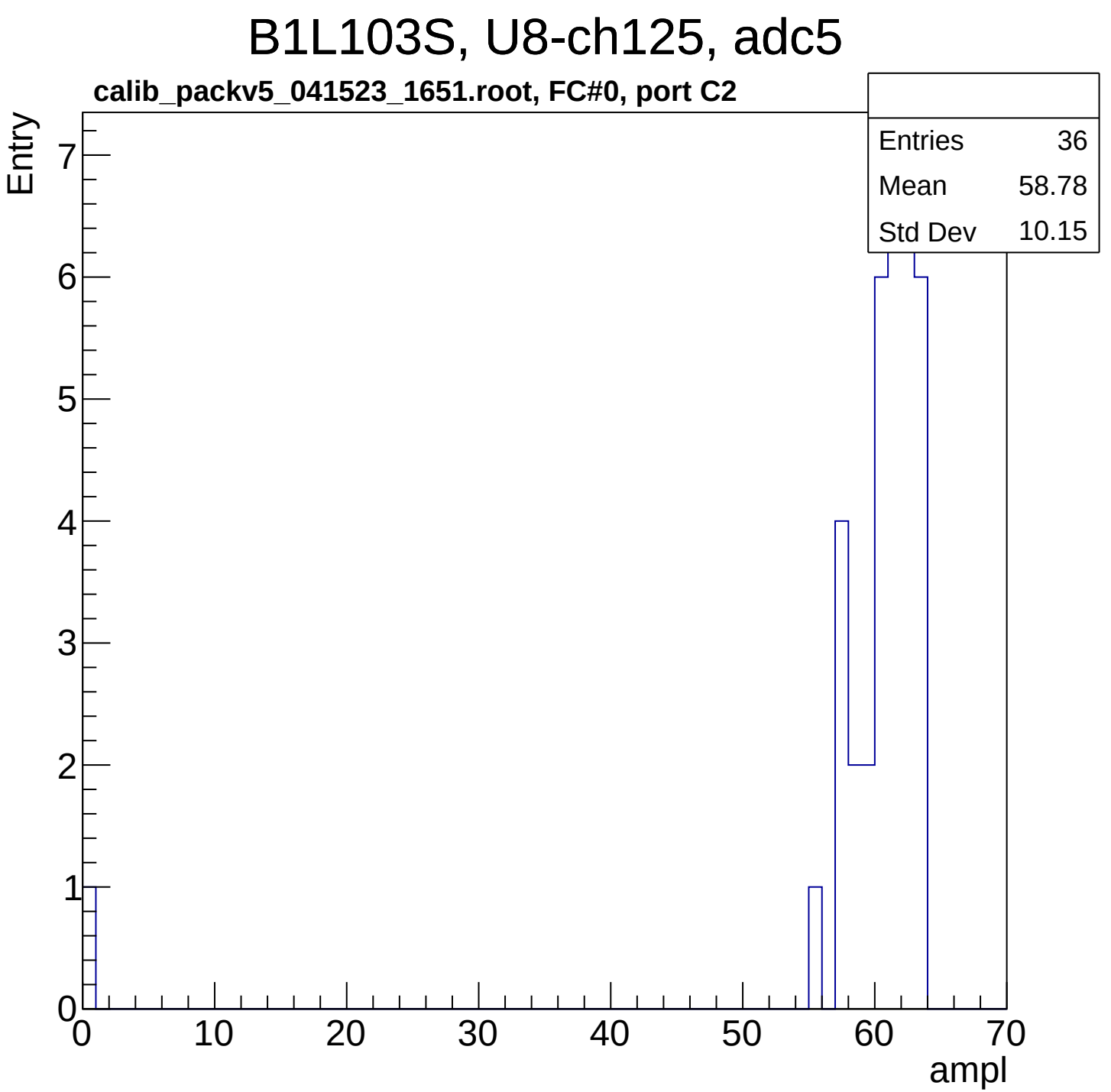
B1L103S, U8-ch125, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 58.78
Std Dev 10.15
Entry
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1
2
3
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5
6
7
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10
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30
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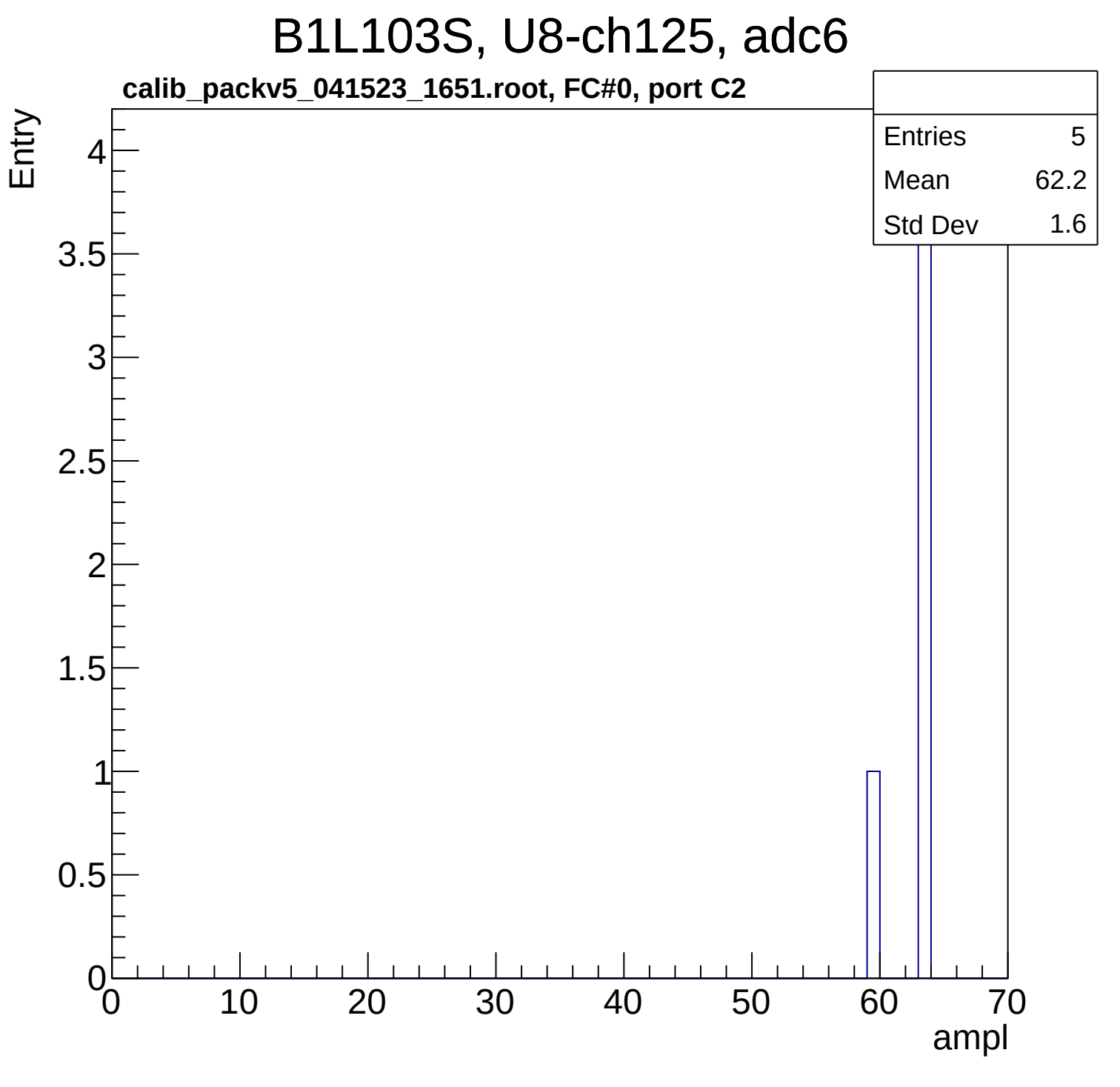
50
60
70
ampl


B1L103S, U8-ch125, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 62.2
Std Dev 1.6
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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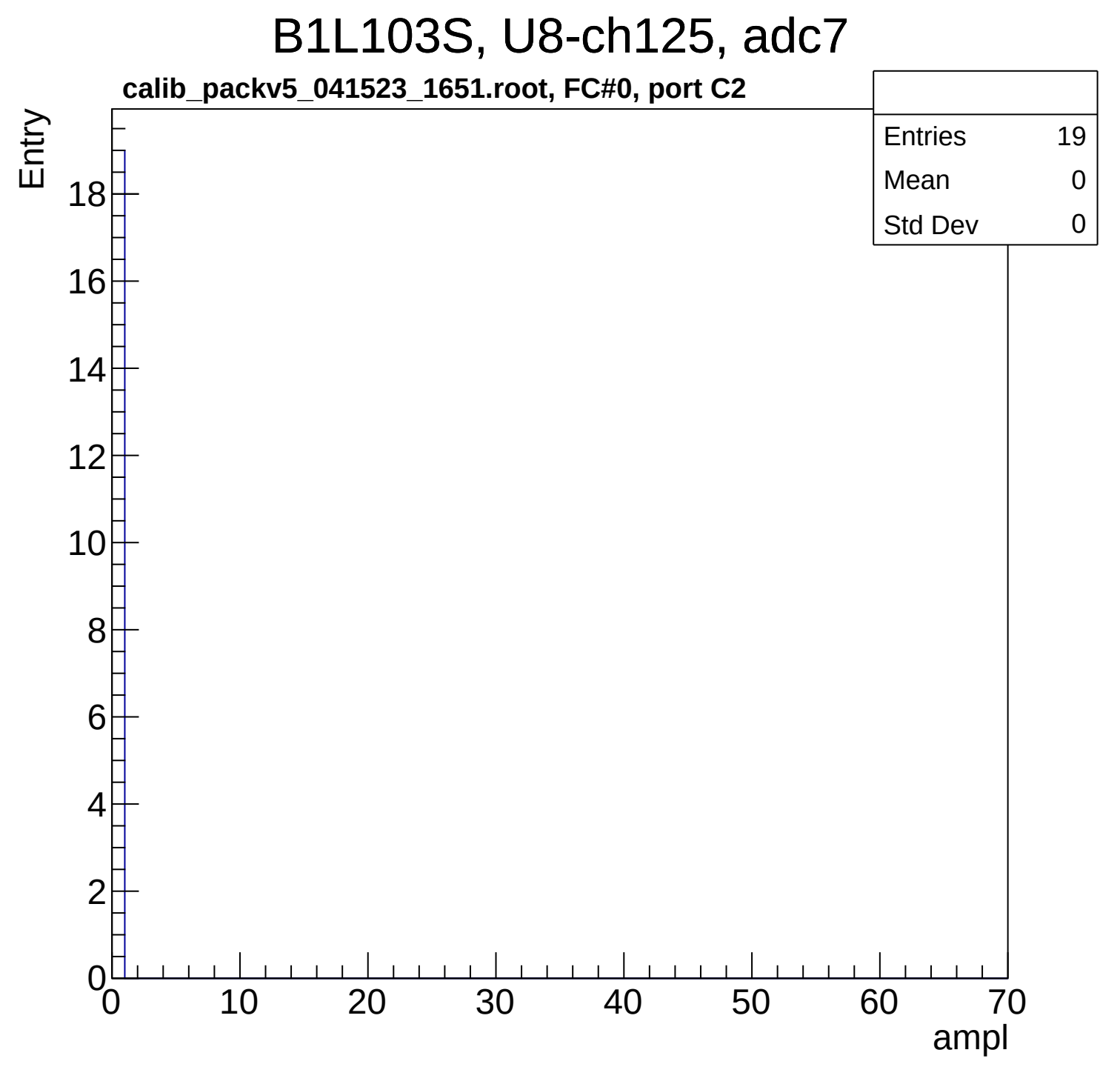
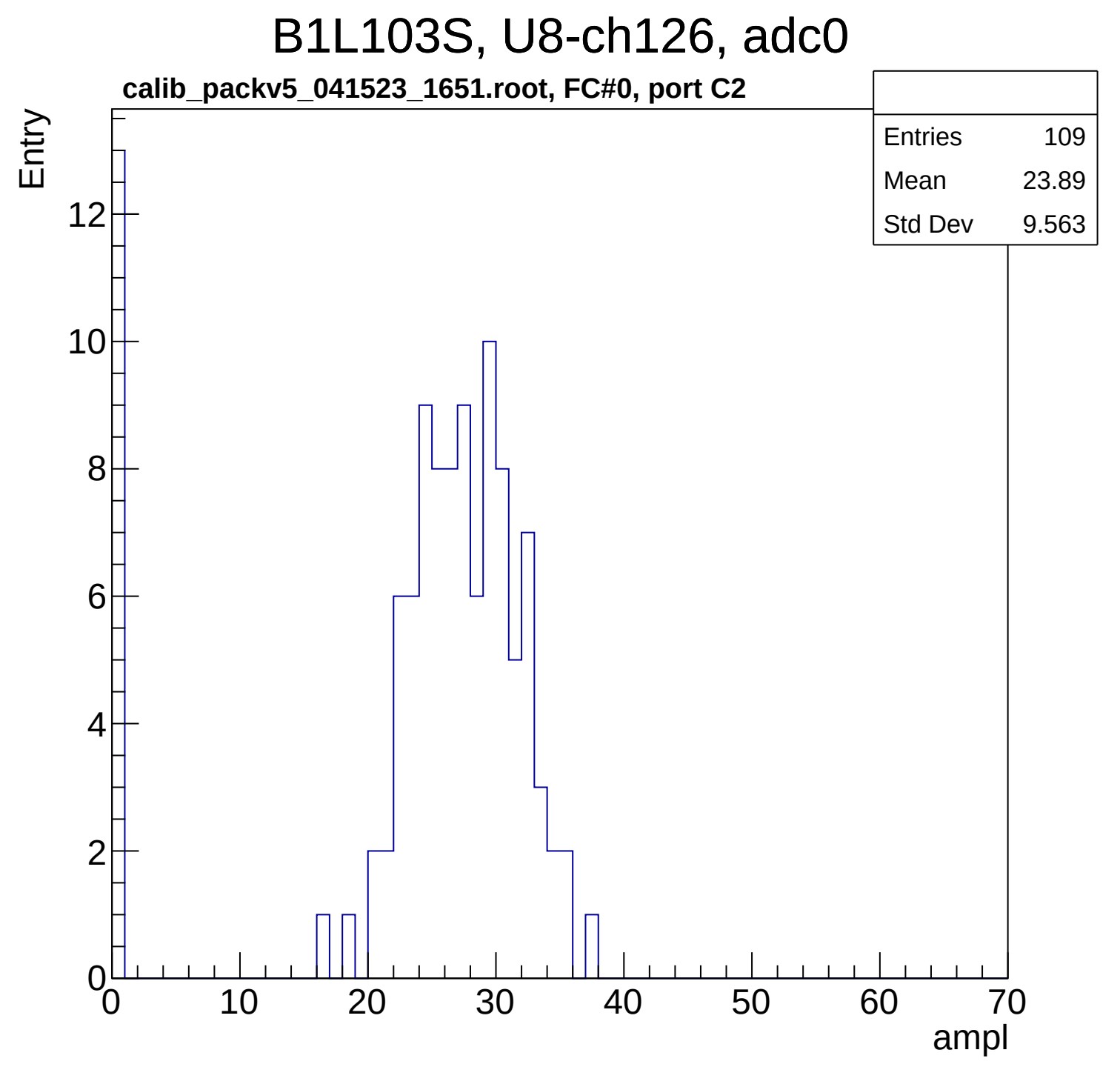
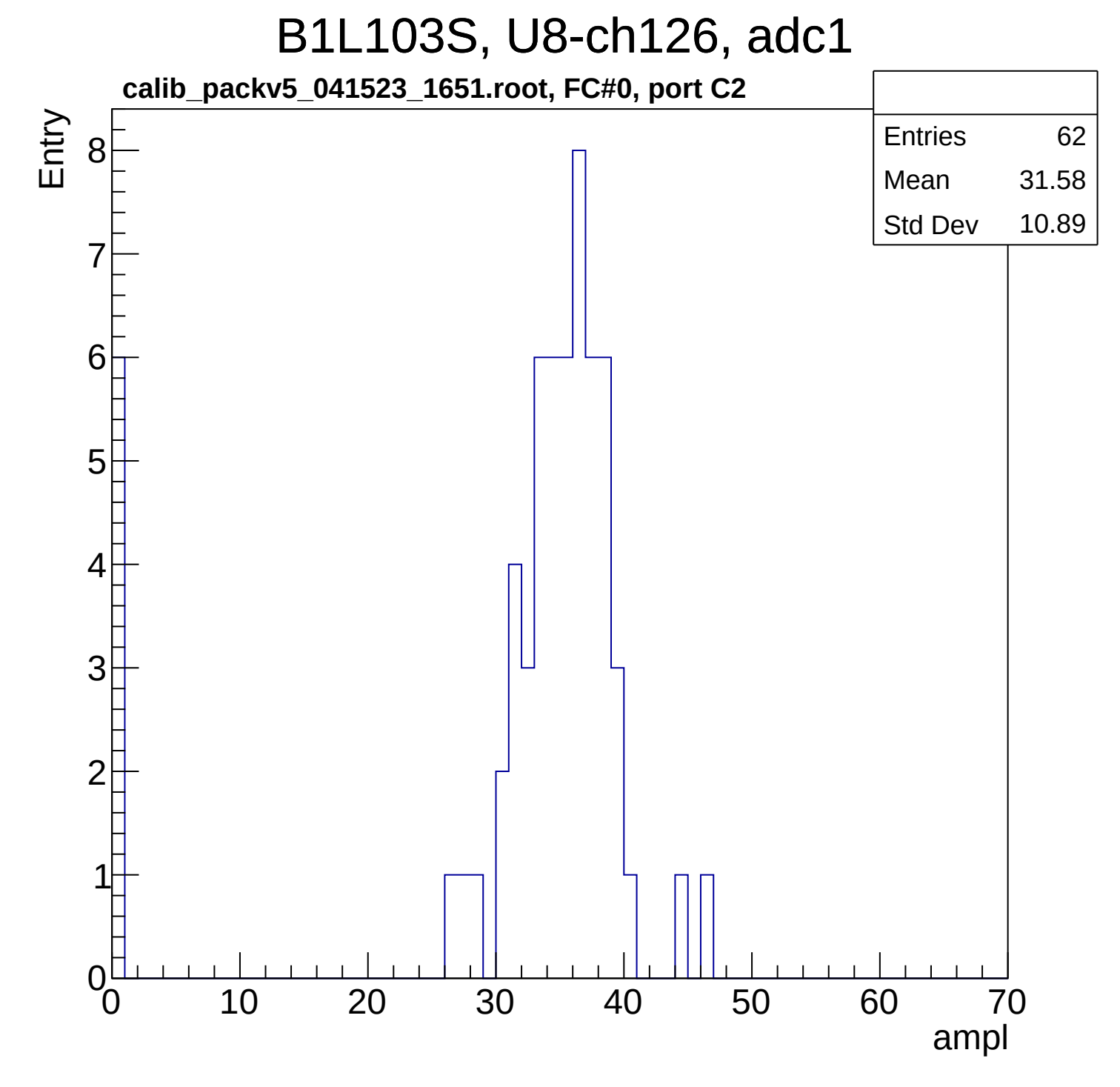
40
50
60
70


B1L103S, U8-ch125, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch126, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 109
Mean 23.89
Std Dev 9.563
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U8-ch126, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 31.58
Std Dev 10.89
Entry
ampl
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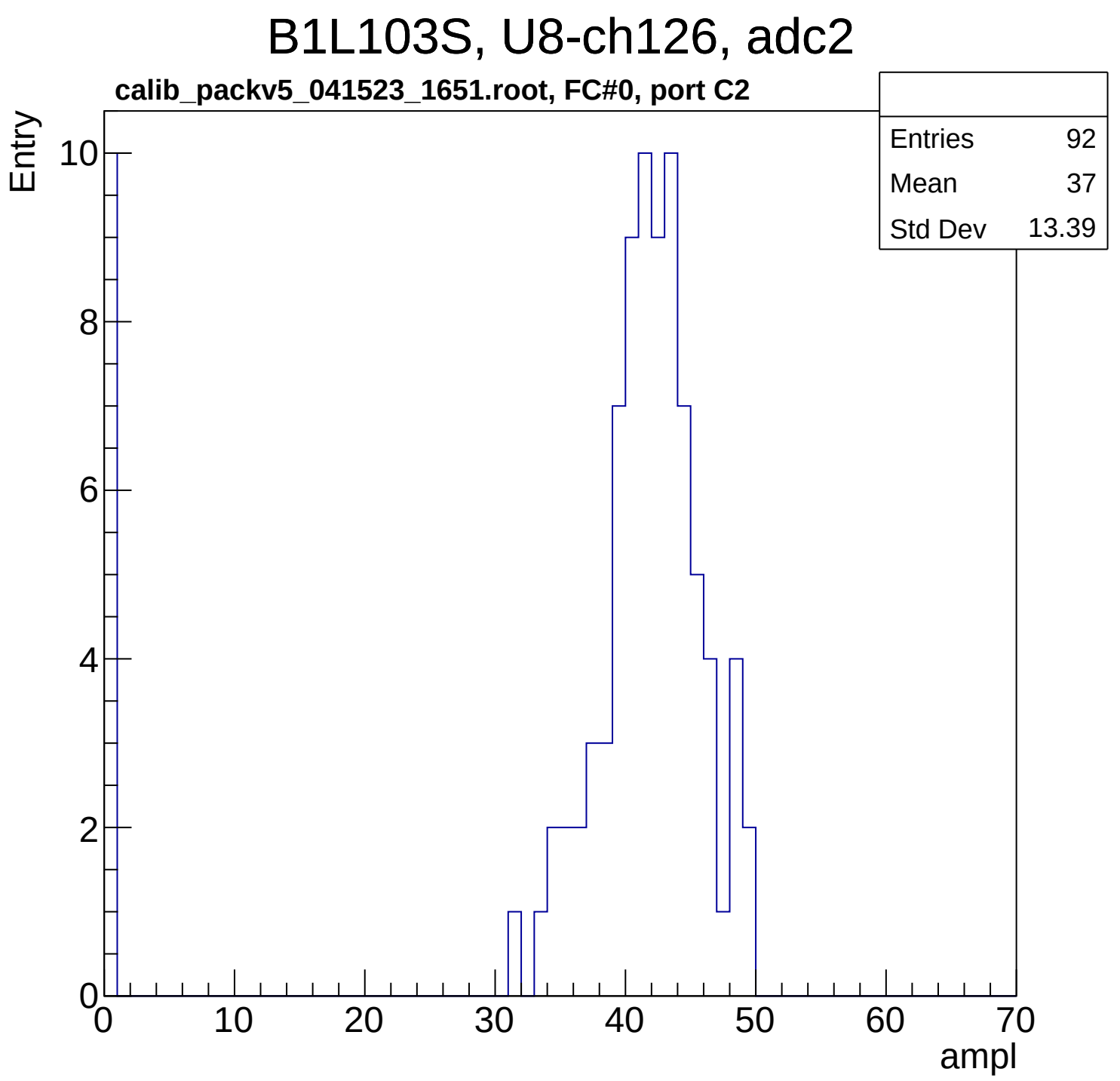
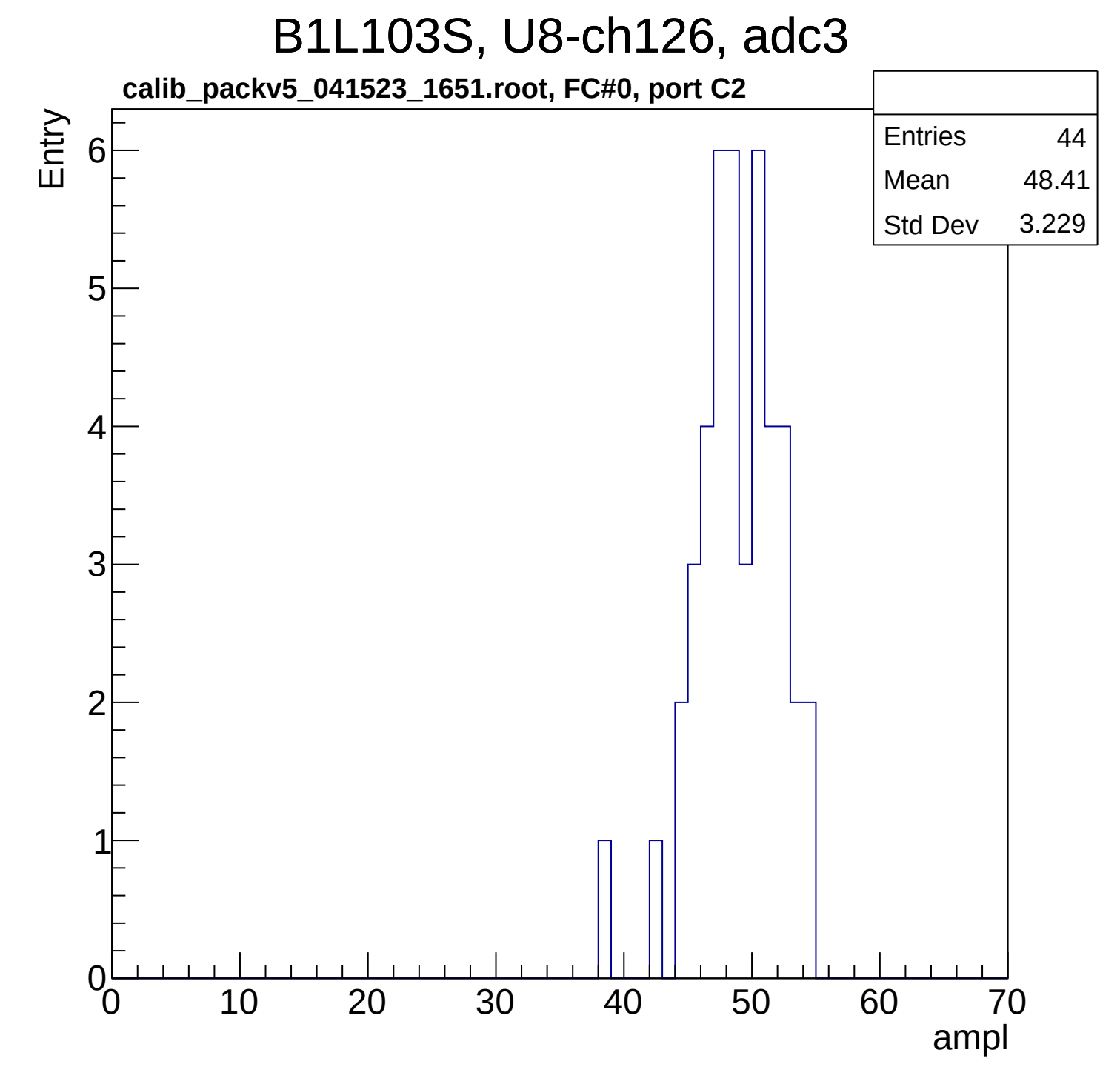
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch126, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 37
Std Dev 13.39
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U8-ch126, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 48.41
Std Dev 3.229
Entry
ampl
0
1
2
3
4
5
6
0
10
20
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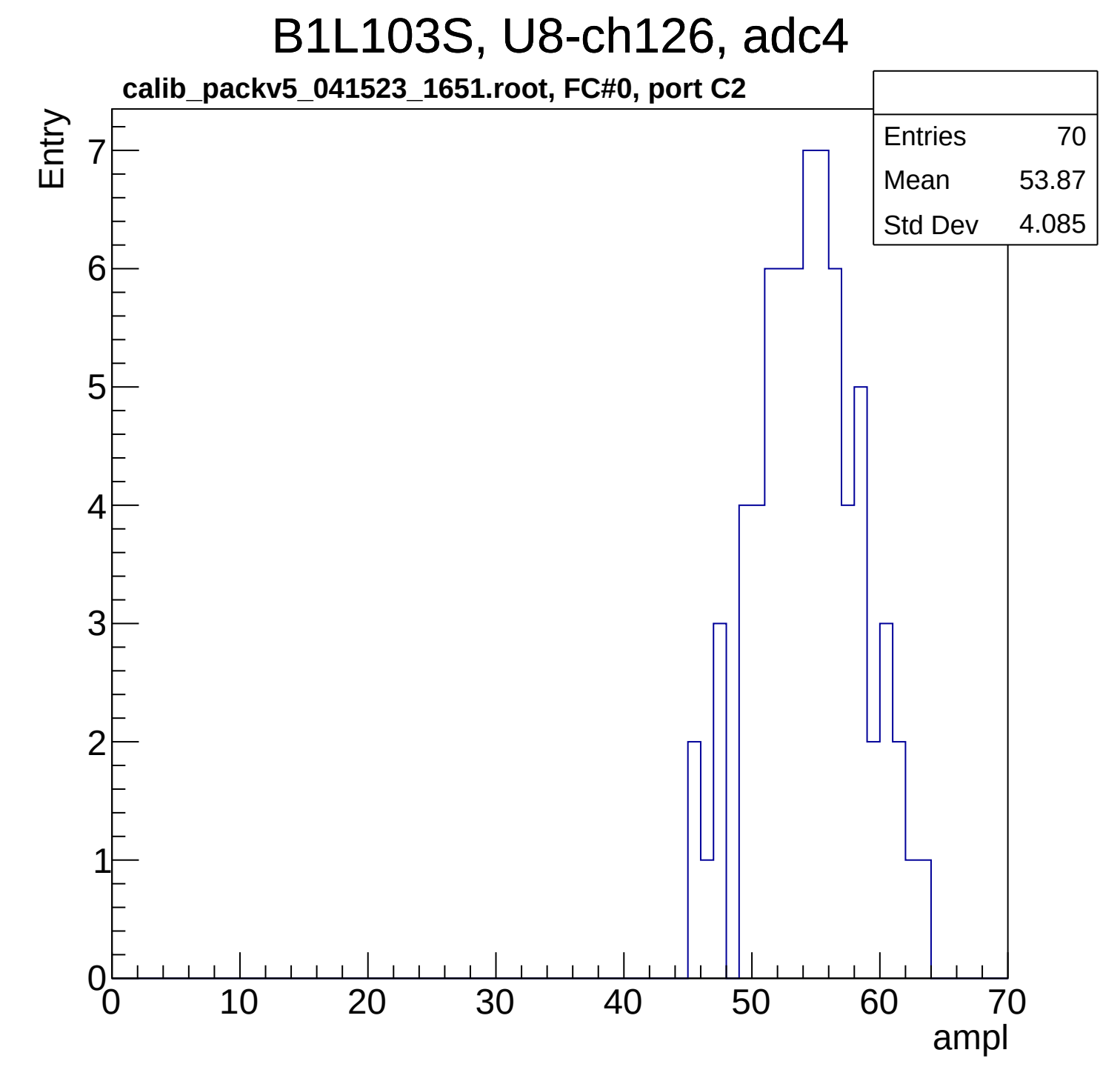
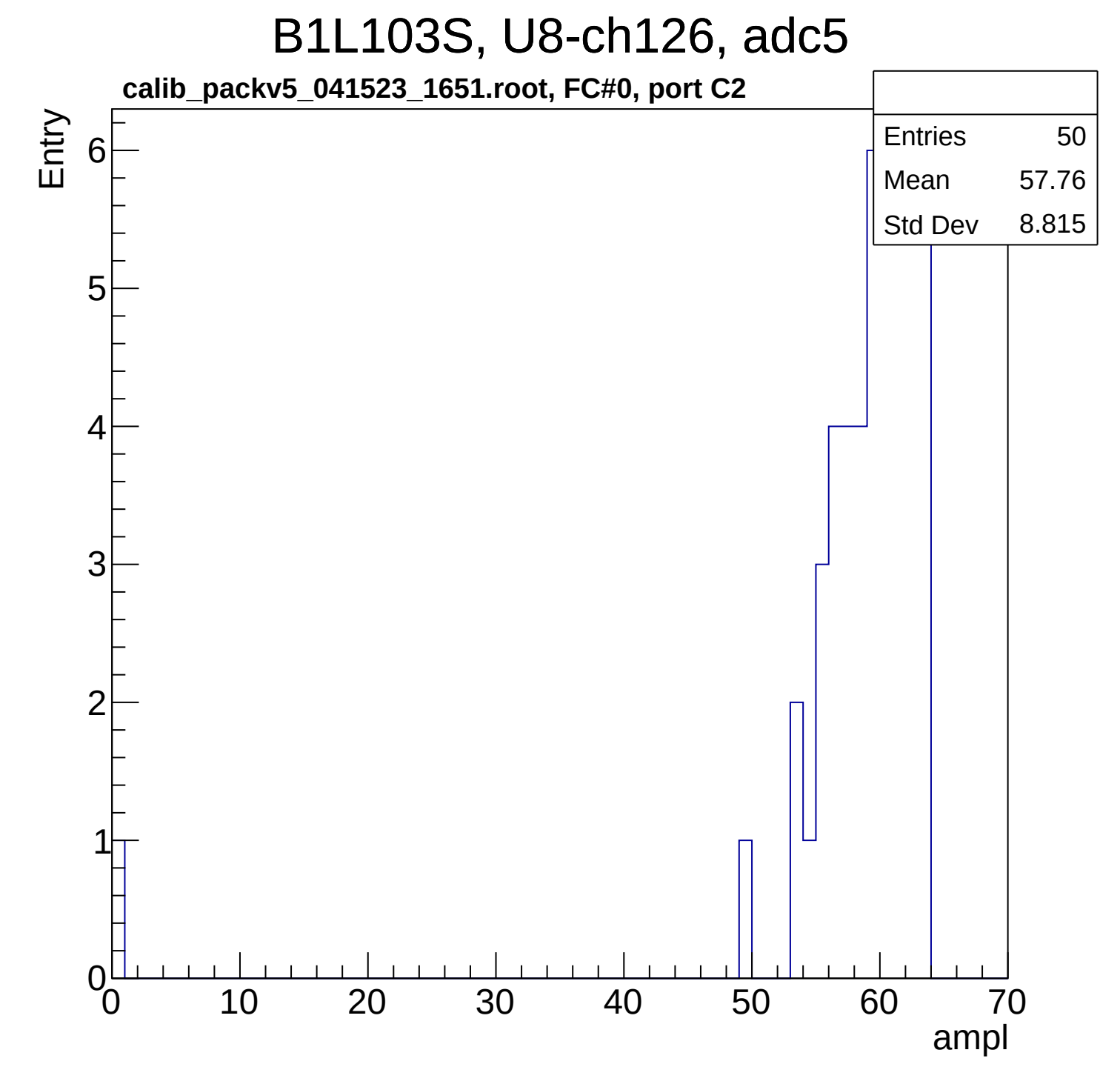
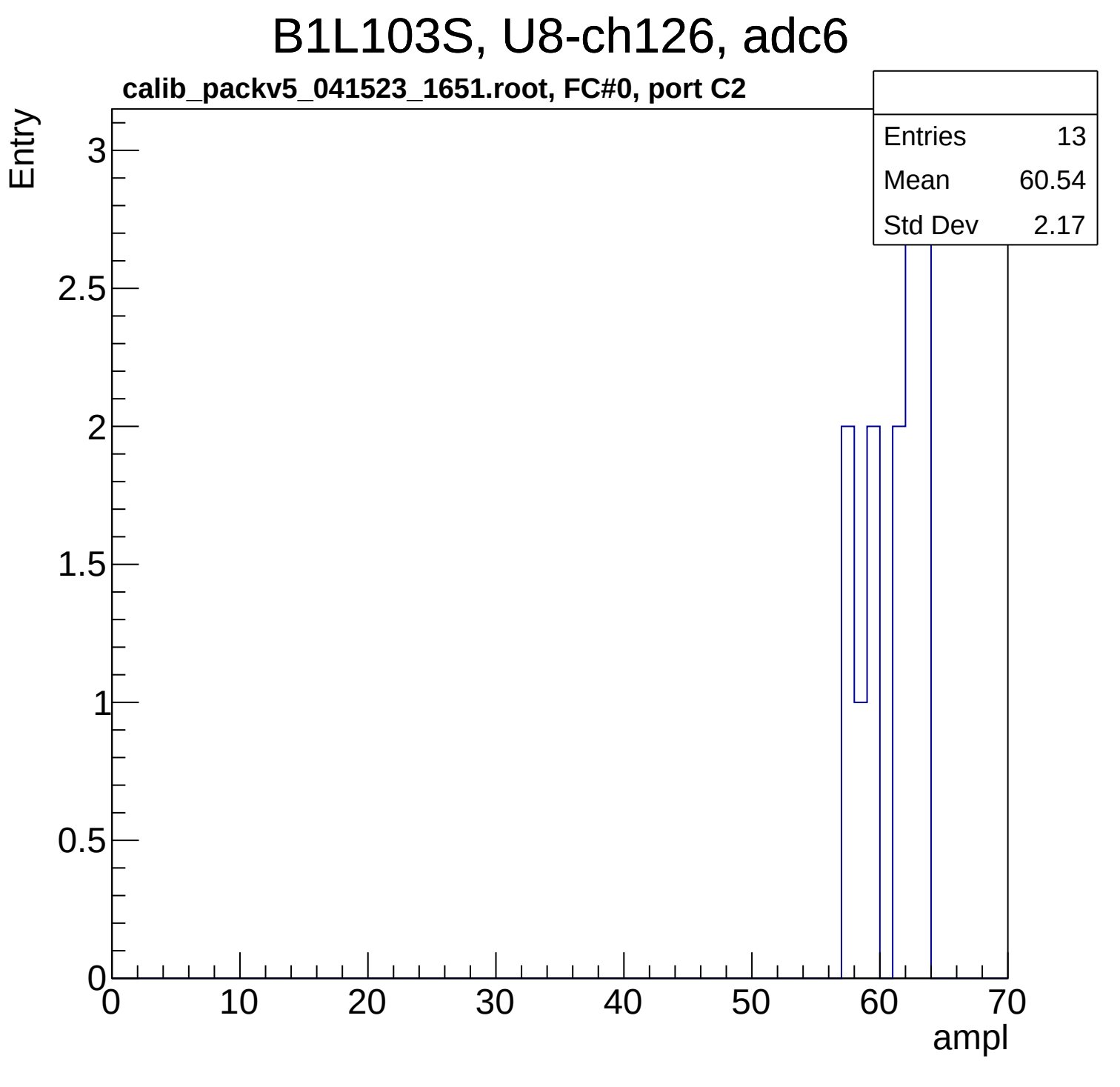
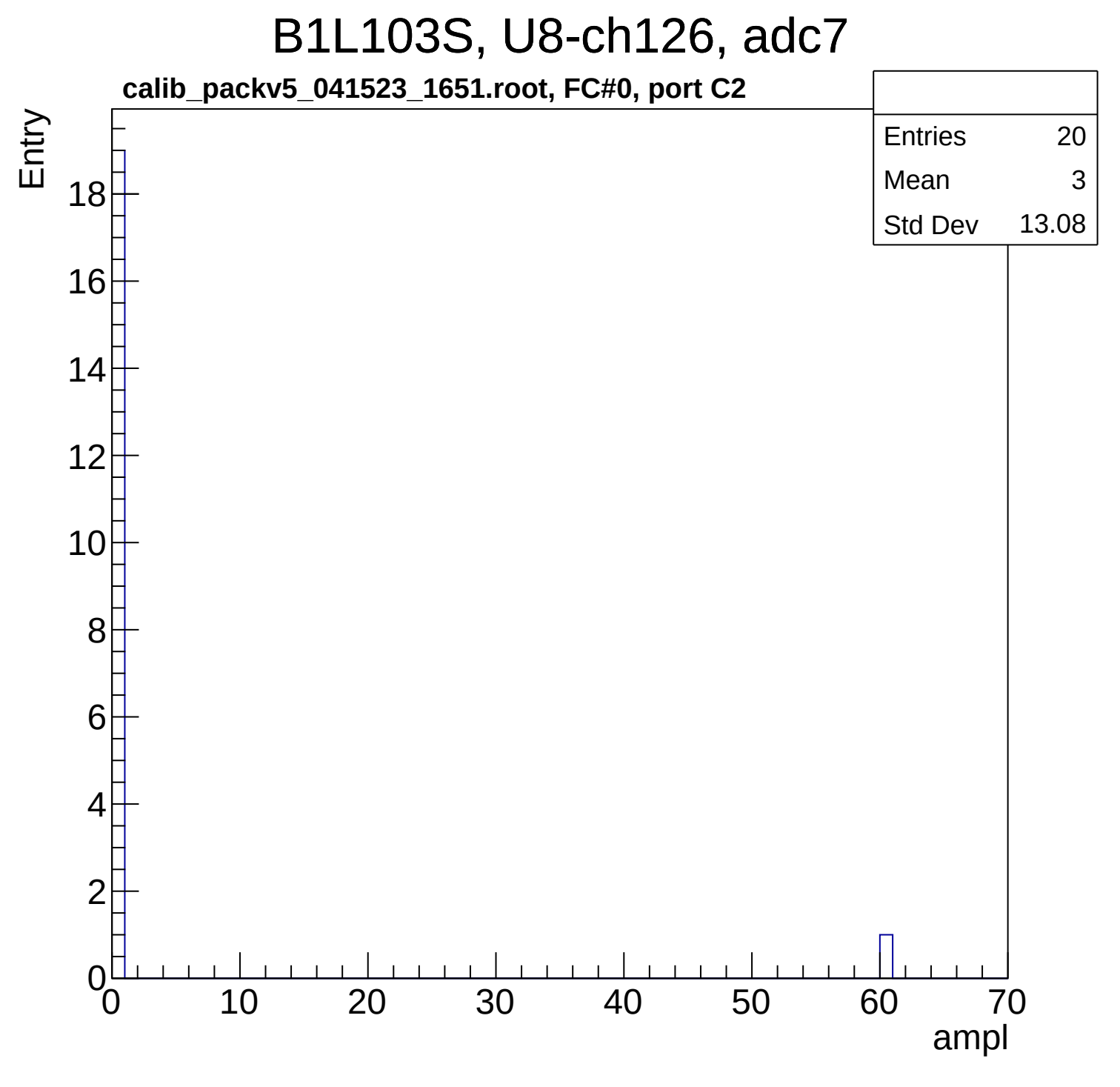
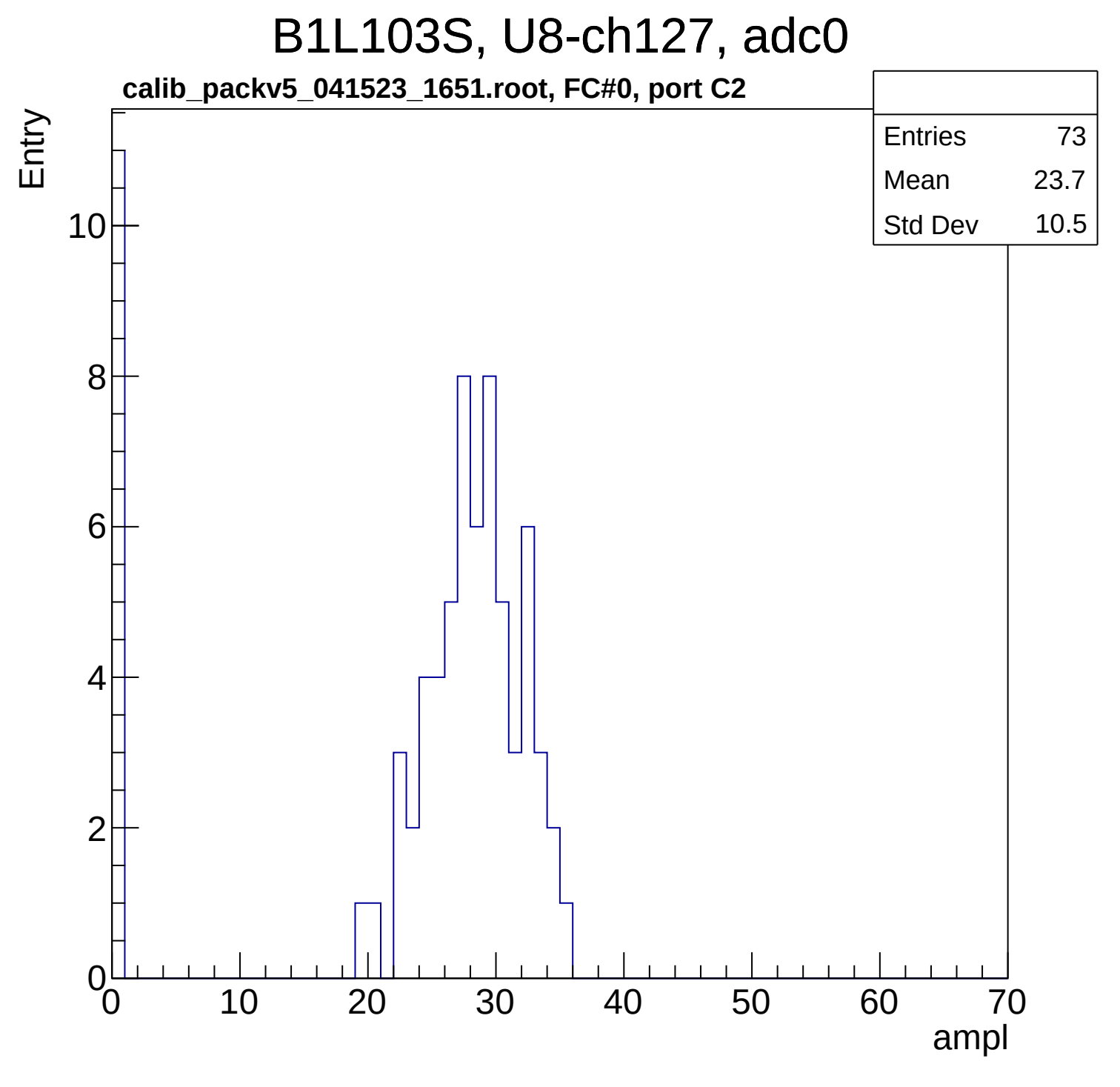
40
50
60
70

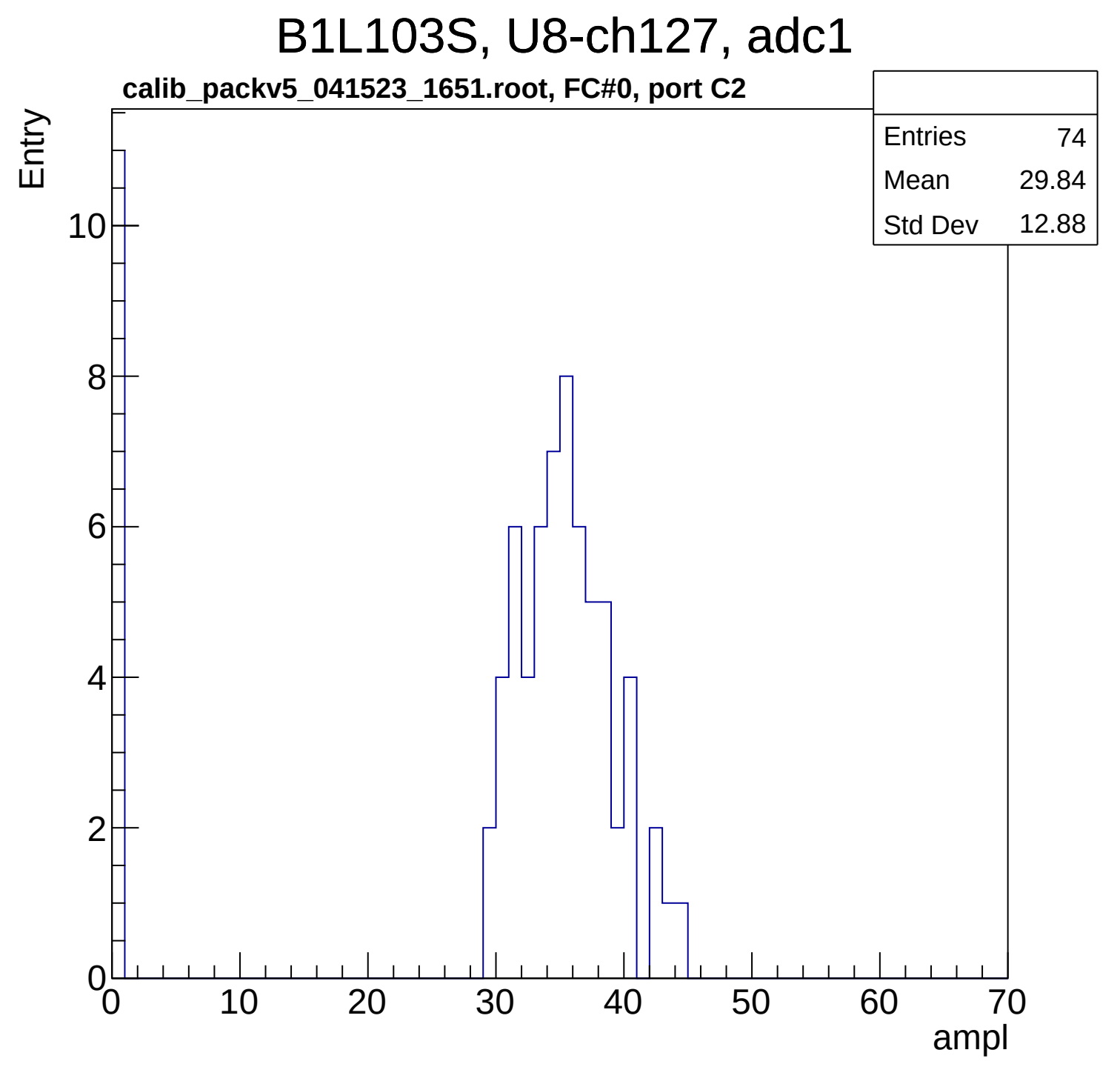

B1L103S, U8-ch126, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 53.87
Std Dev 4.085
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

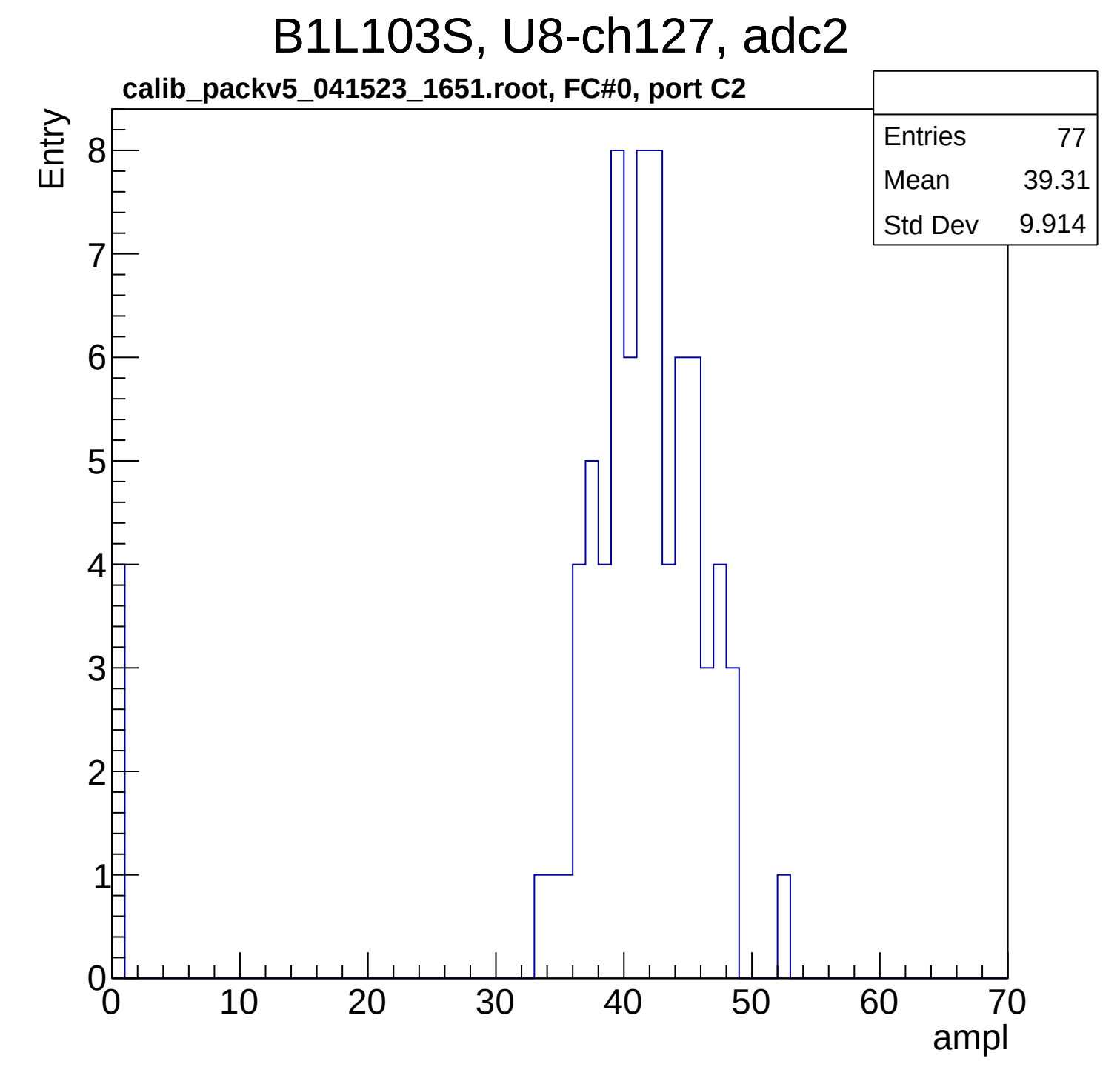

B1L103S, U8-ch126, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 57.76
Std Dev 8.815
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

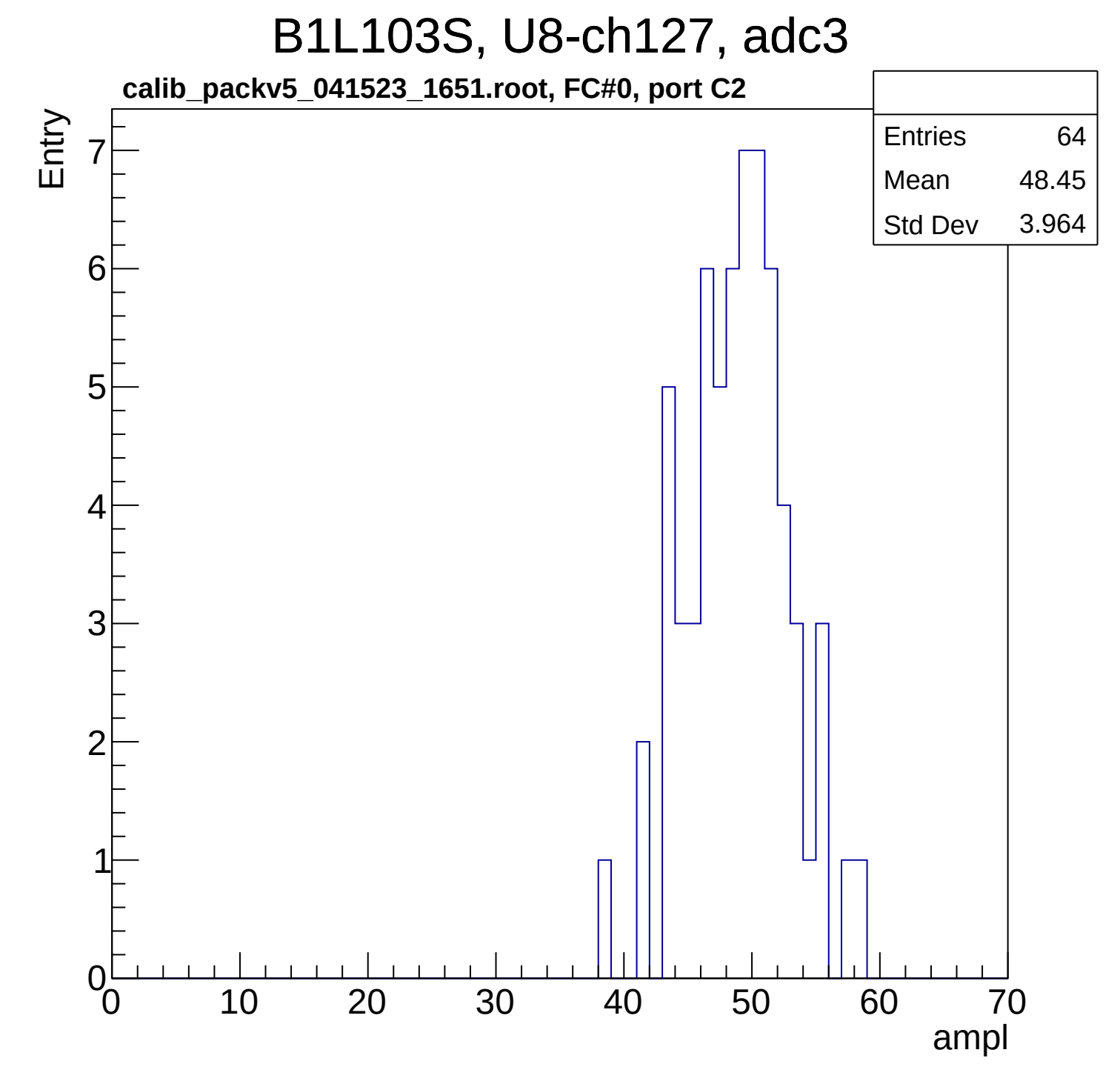

B1L103S, U8-ch126, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 60.54
Std Dev 2.17
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

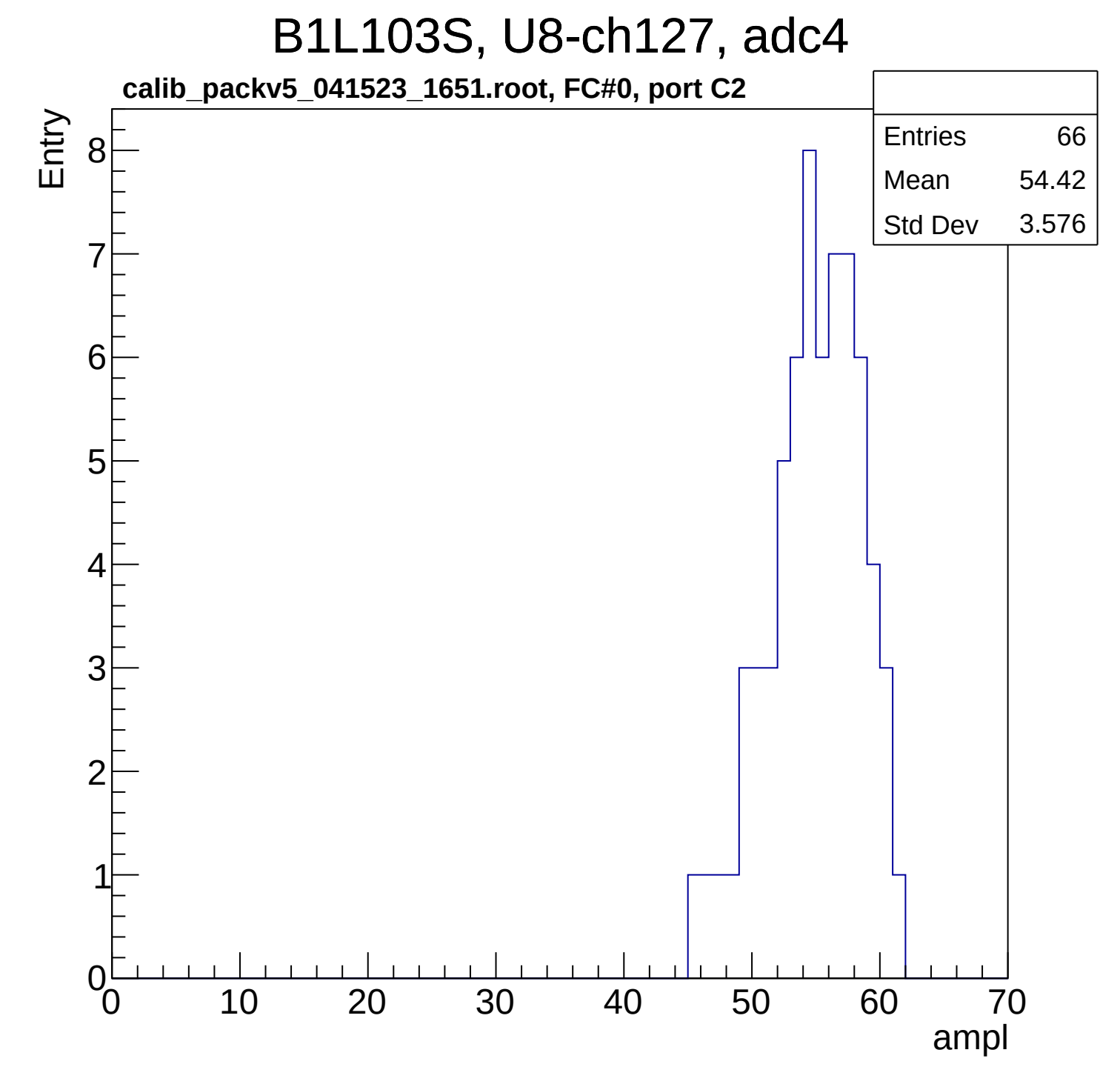

B1L103S, U8-ch126, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3
Std Dev 13.08
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

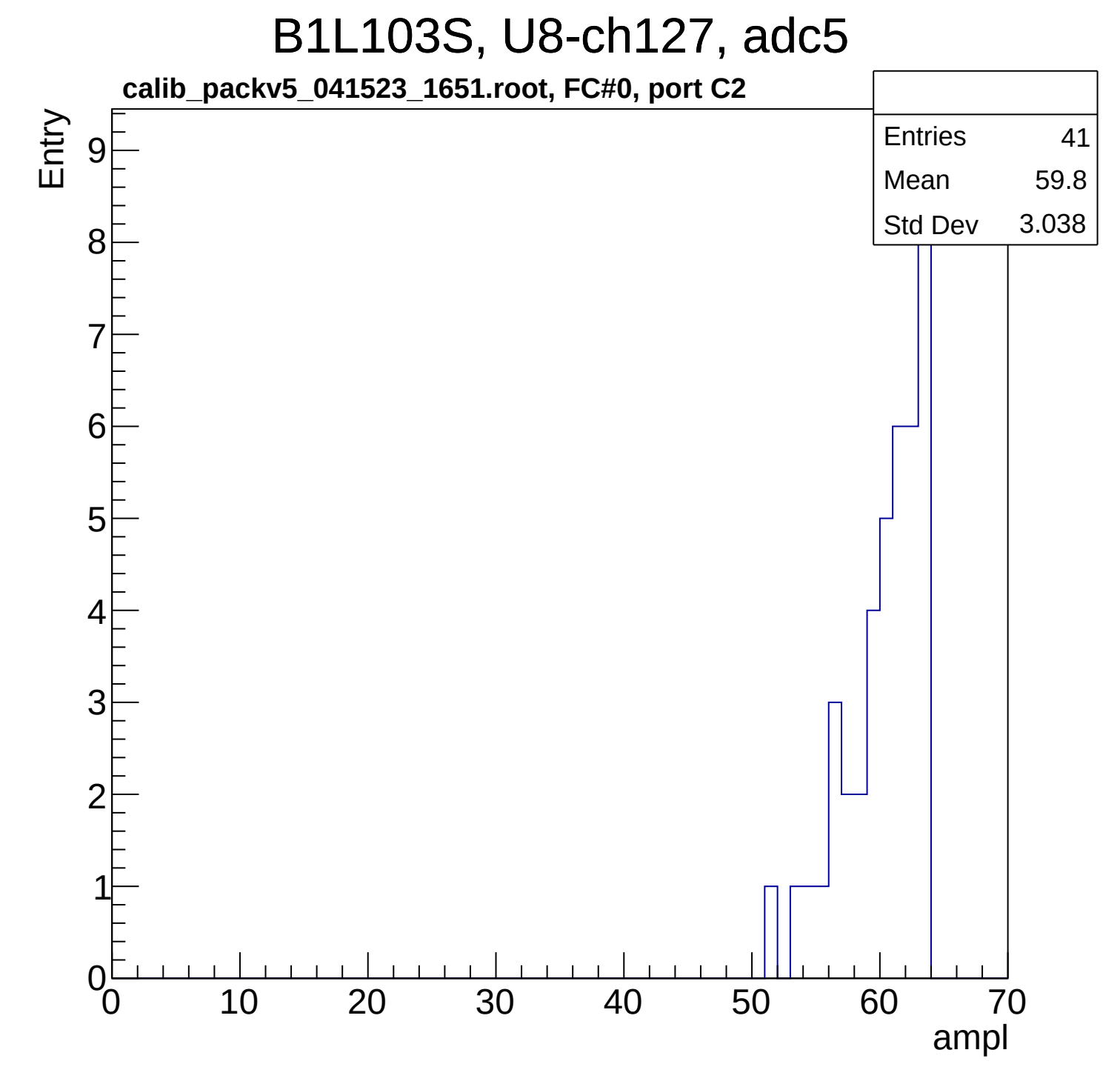

B1L103S, U8-ch127, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 23.7
Std Dev 10.5
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

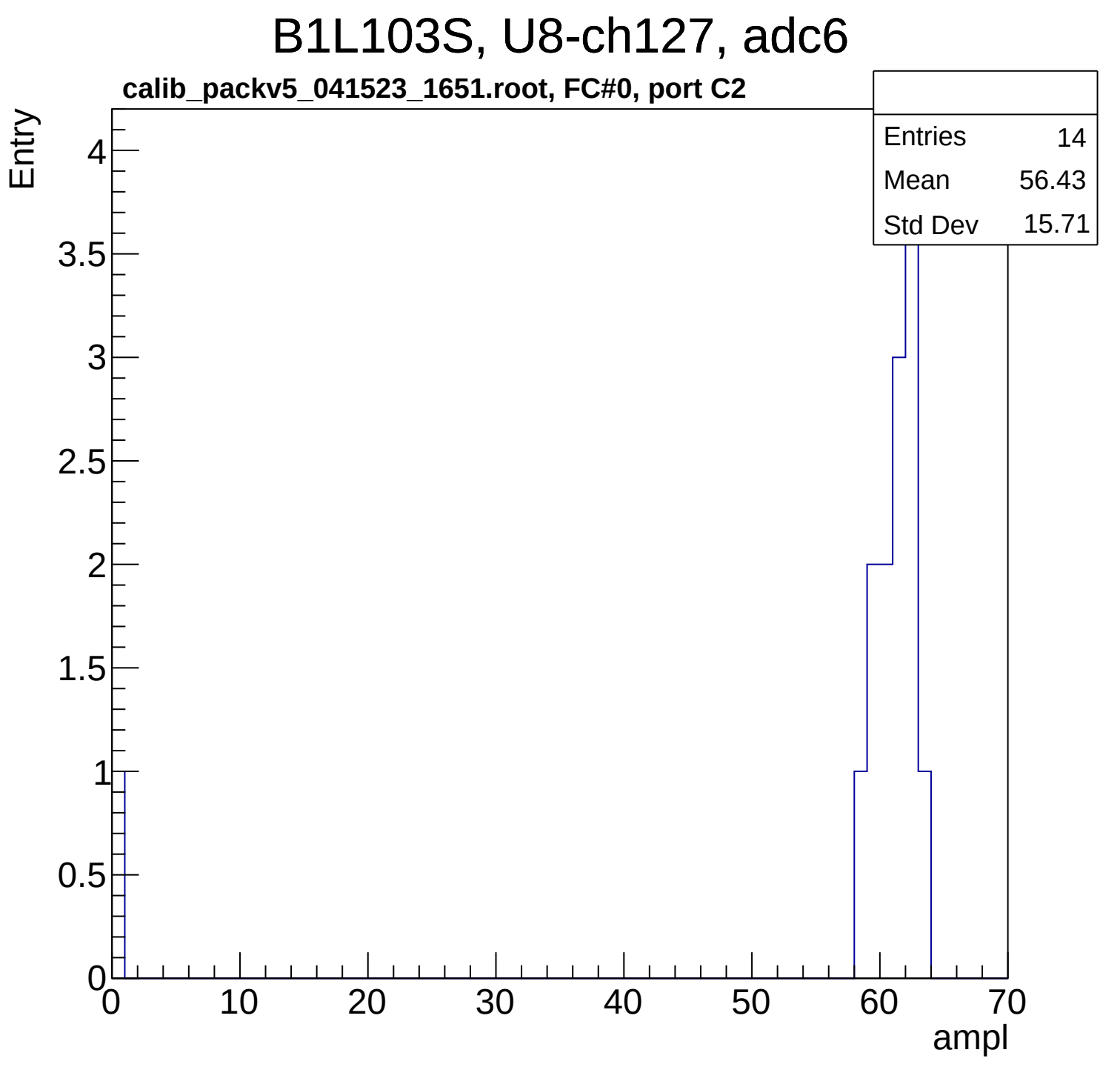

B1L103S, U8-ch127, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 29.84
Std Dev 12.88
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

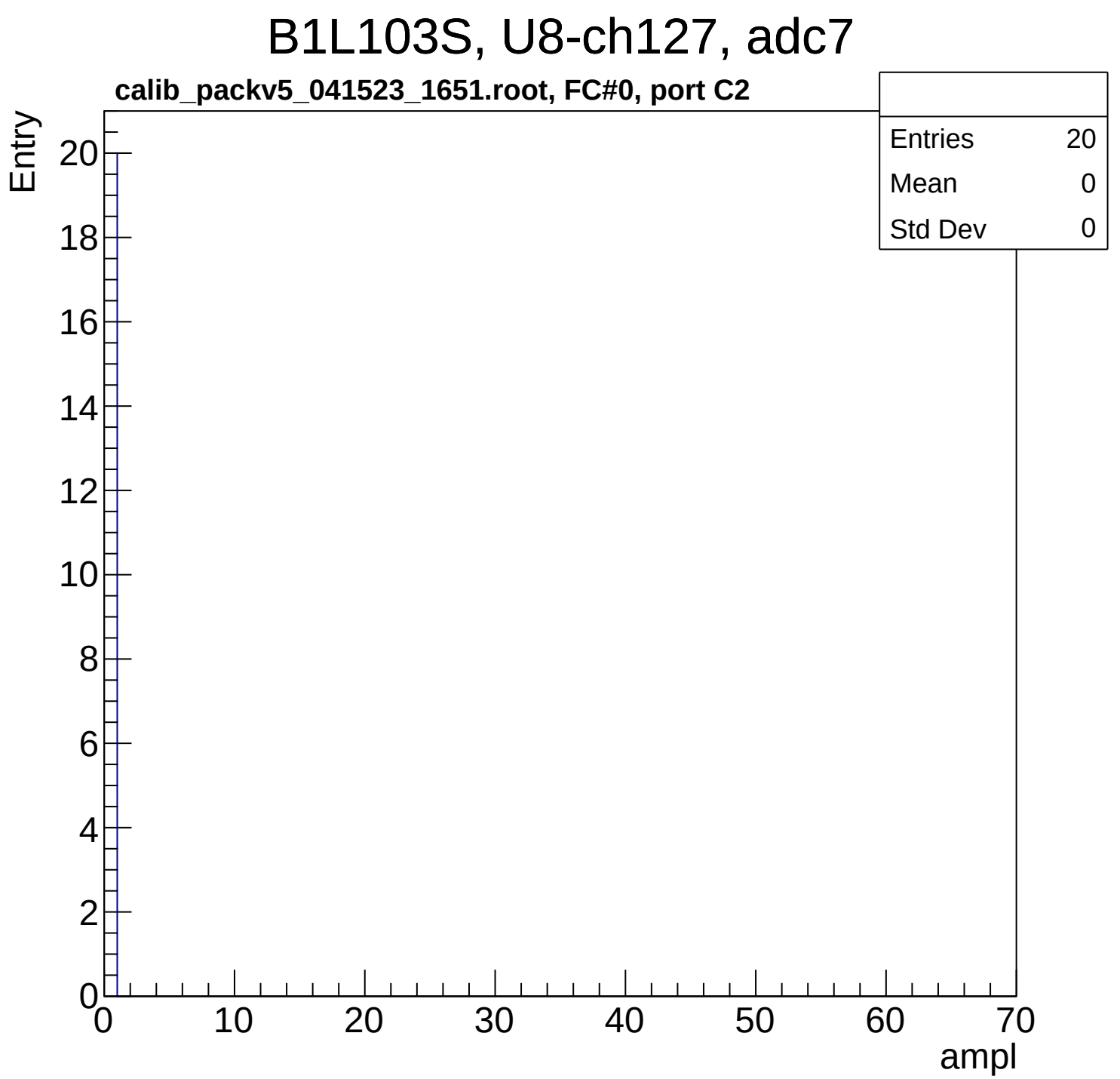

B1L103S, U8-ch127, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 39.31
Std Dev 9.914
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

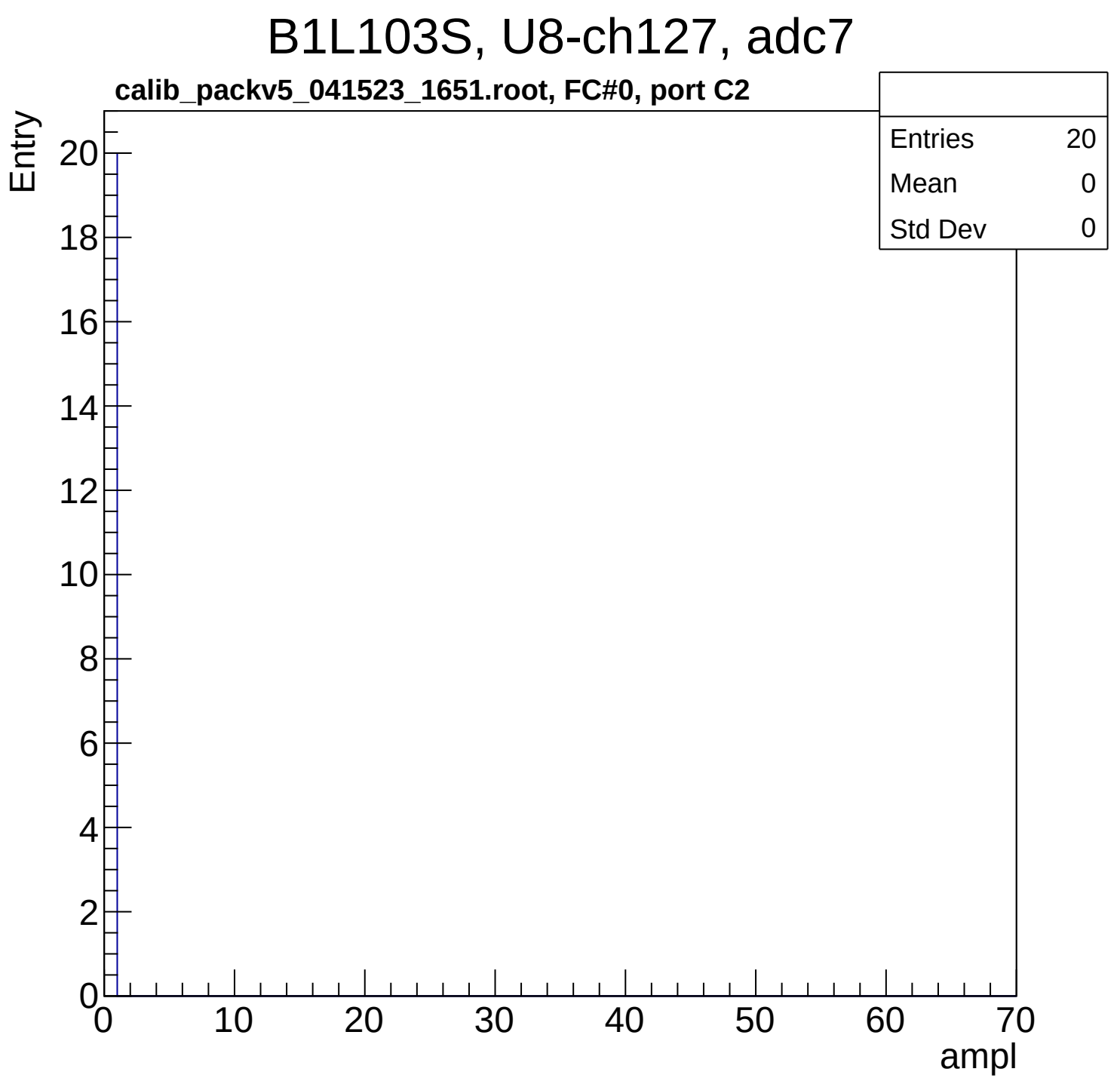

B1L103S, U8-ch127, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 48.45
Std Dev 3.964
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U8-ch127, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 54.42
Std Dev 3.576
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch127, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 59.8
Std Dev 3.038
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U8-ch127, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 56.43
Std Dev 15.71
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U8-ch127, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch127, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70
ampl