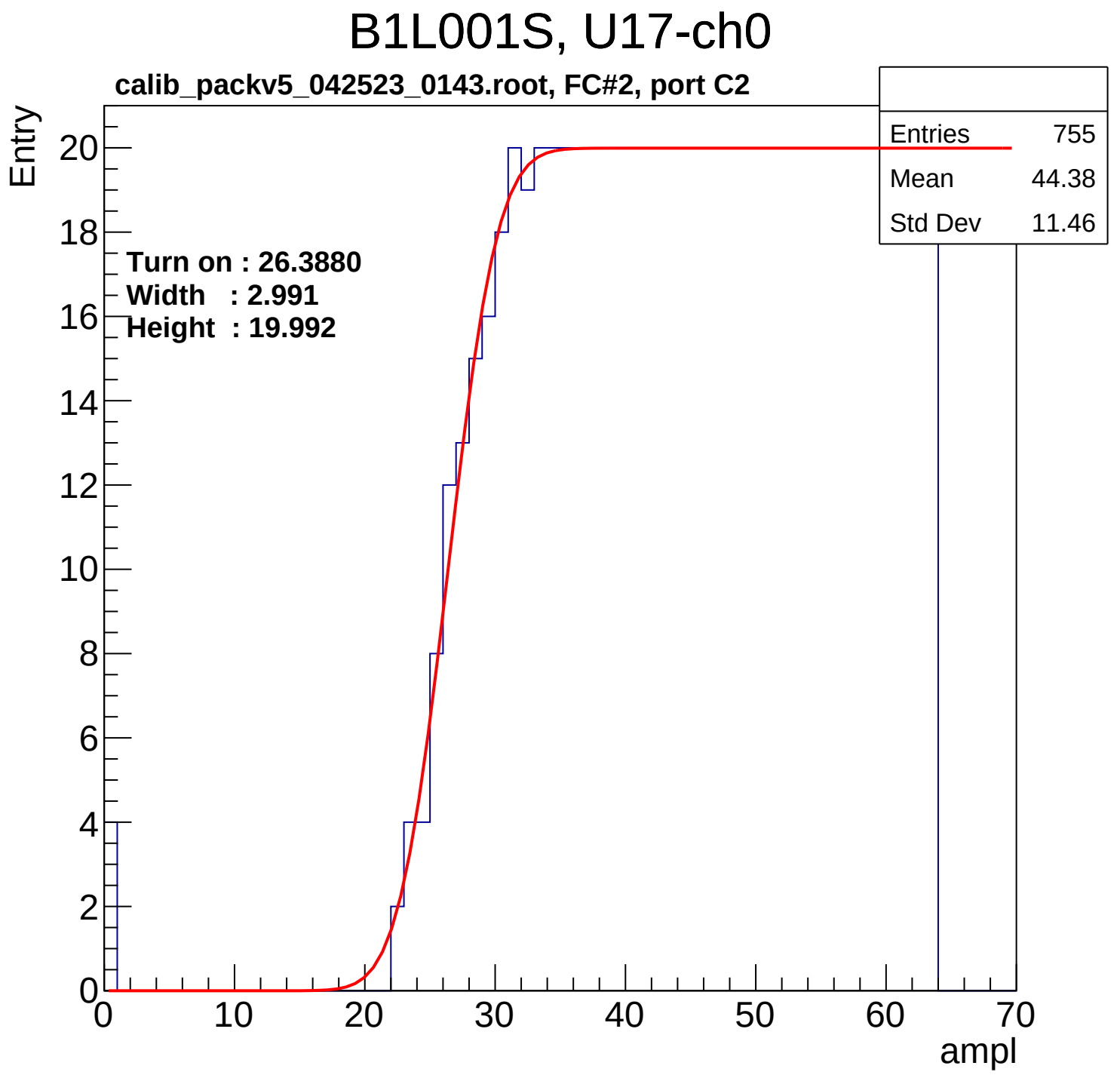
B1L001S, U17-ch0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 755
Mean 44.38
Std Dev 11.46
Turn on : 26.3880
Width : 2.991
Height : 19.992
Entry
ampl
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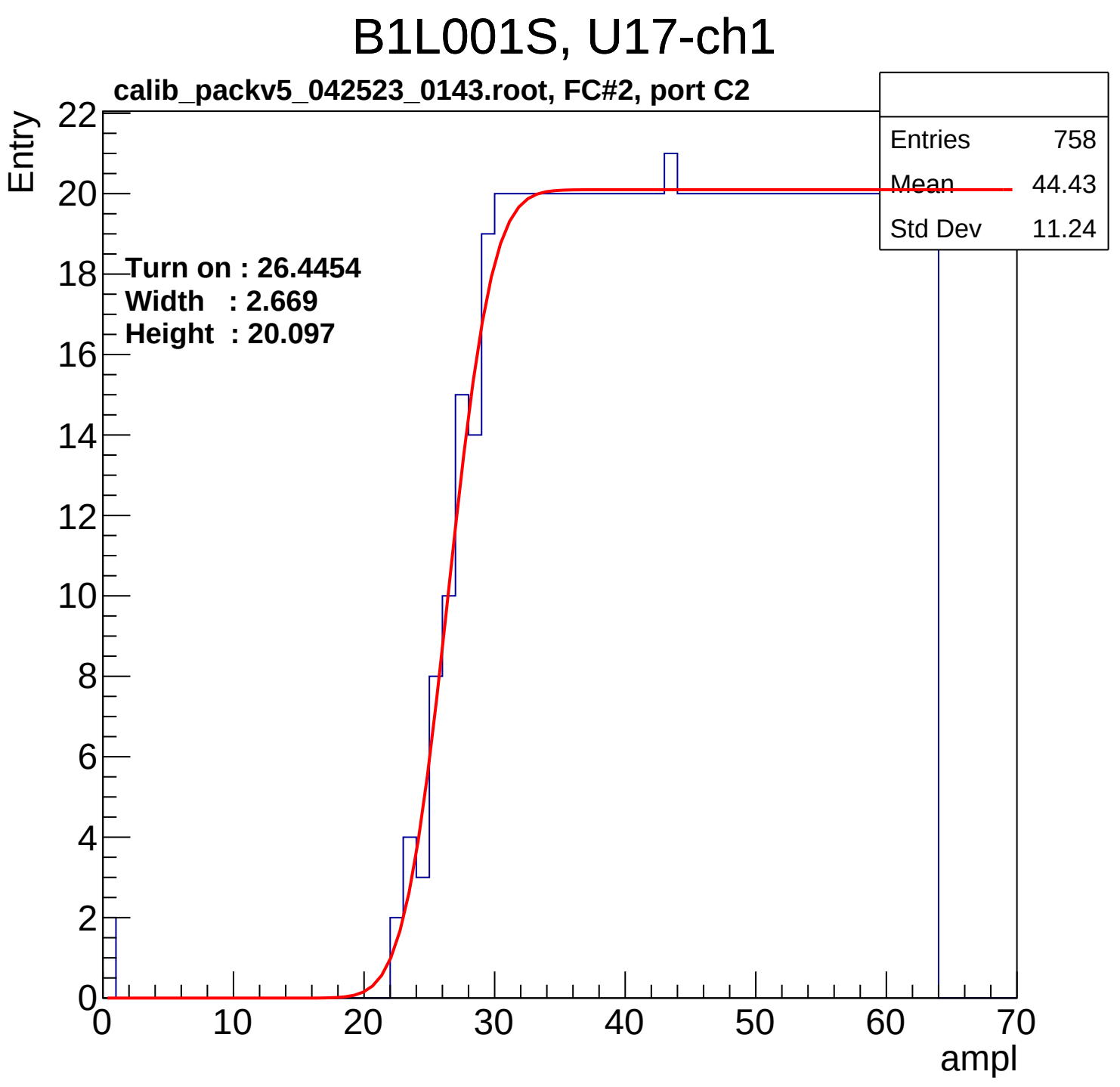
B1L001S, U17-ch1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 758
Mean 44.43
Std Dev 11.24
Turn on : 26.4454
Width : 2.669
Height : 20.097
Entry
ampl
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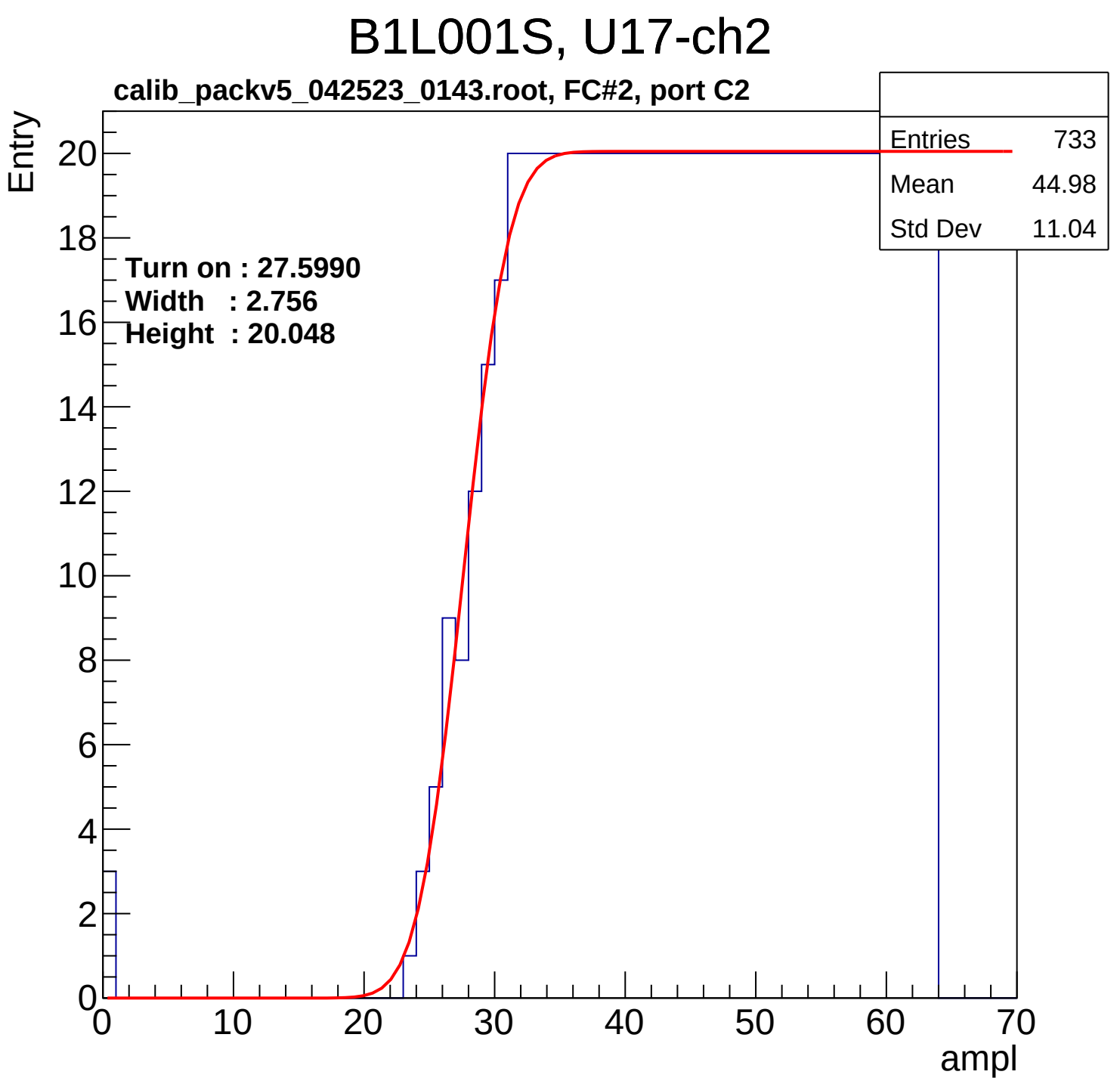
B1L001S, U17-ch2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 733
Mean 44.98
Std Dev 11.04
Turn on : 27.5990
Width : 2.756
Height : 20.048
Entry
ampl
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6
8
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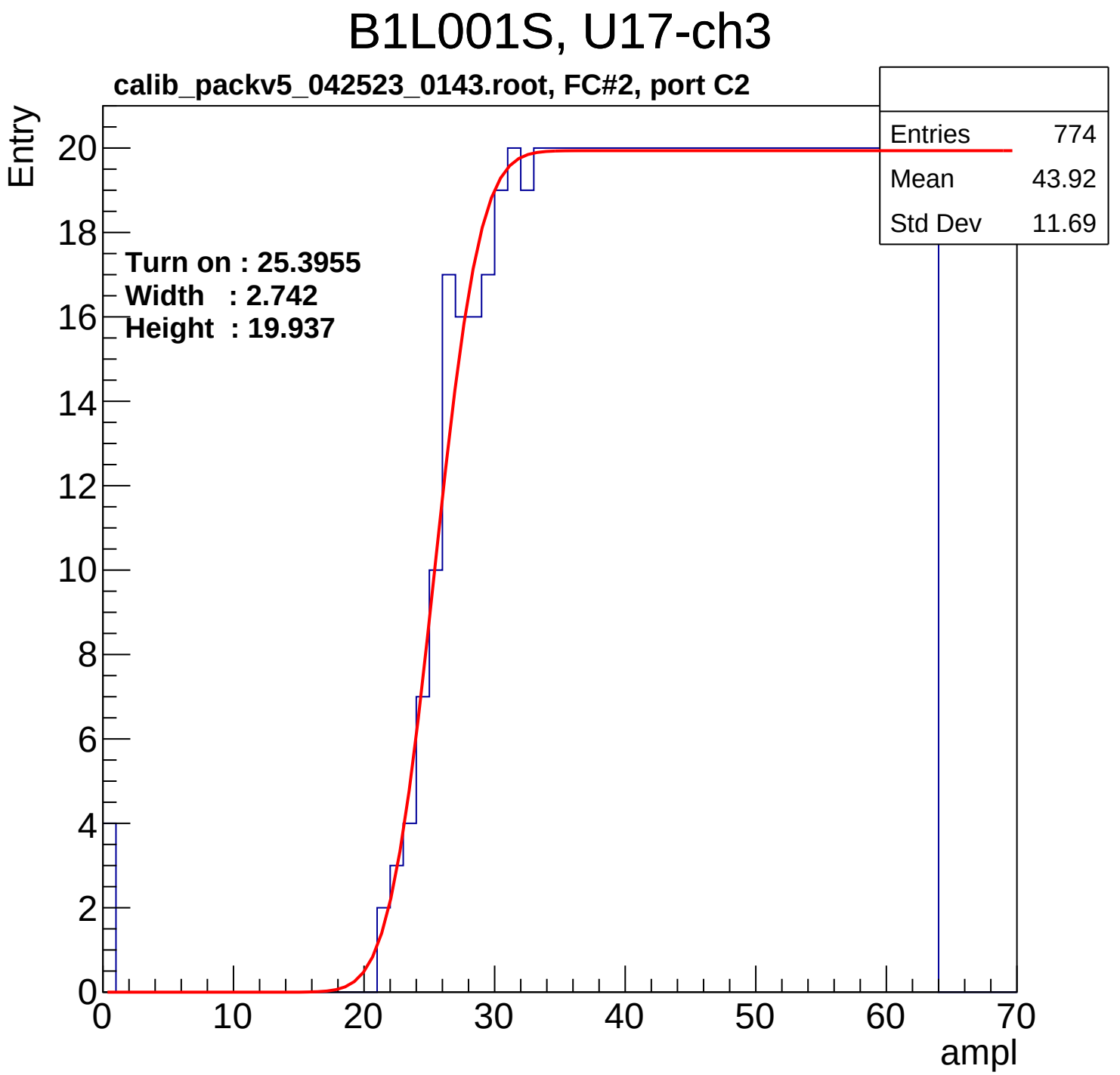
B1L001S, U17-ch3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 774
Mean 43.92
Std Dev 11.69
Turn on : 25.3955
Width : 2.742
Height : 19.937
Entry
ampl
0
2
4
6
8
10
12
14
16
18
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0
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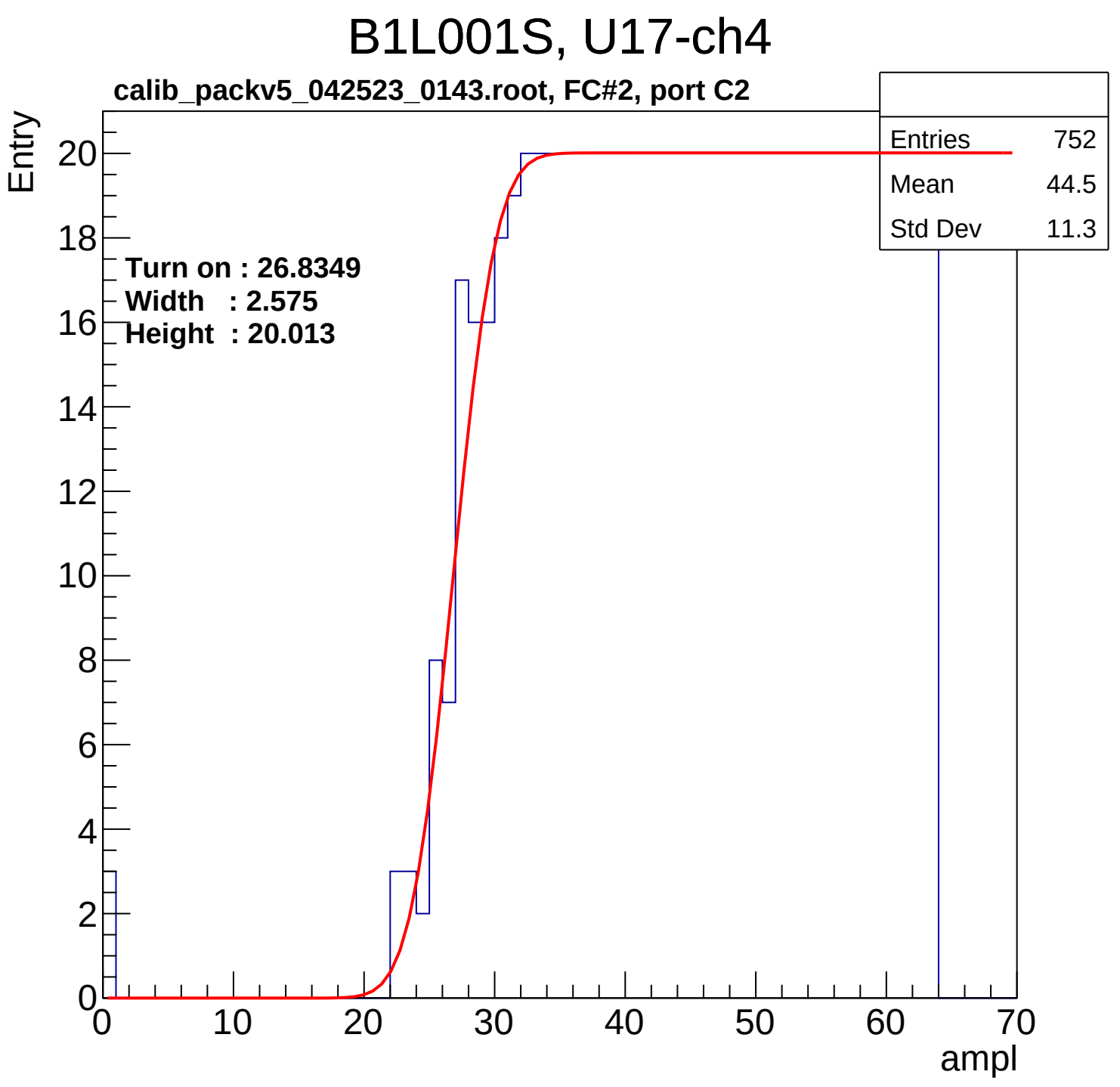
B1L001S, U17-ch4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 752
Mean 44.5
Std Dev 11.3
Turn on : 26.8349
Width : 2.575
Height : 20.013
Entry
ampl
0
2
4
6
8
10
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14
16
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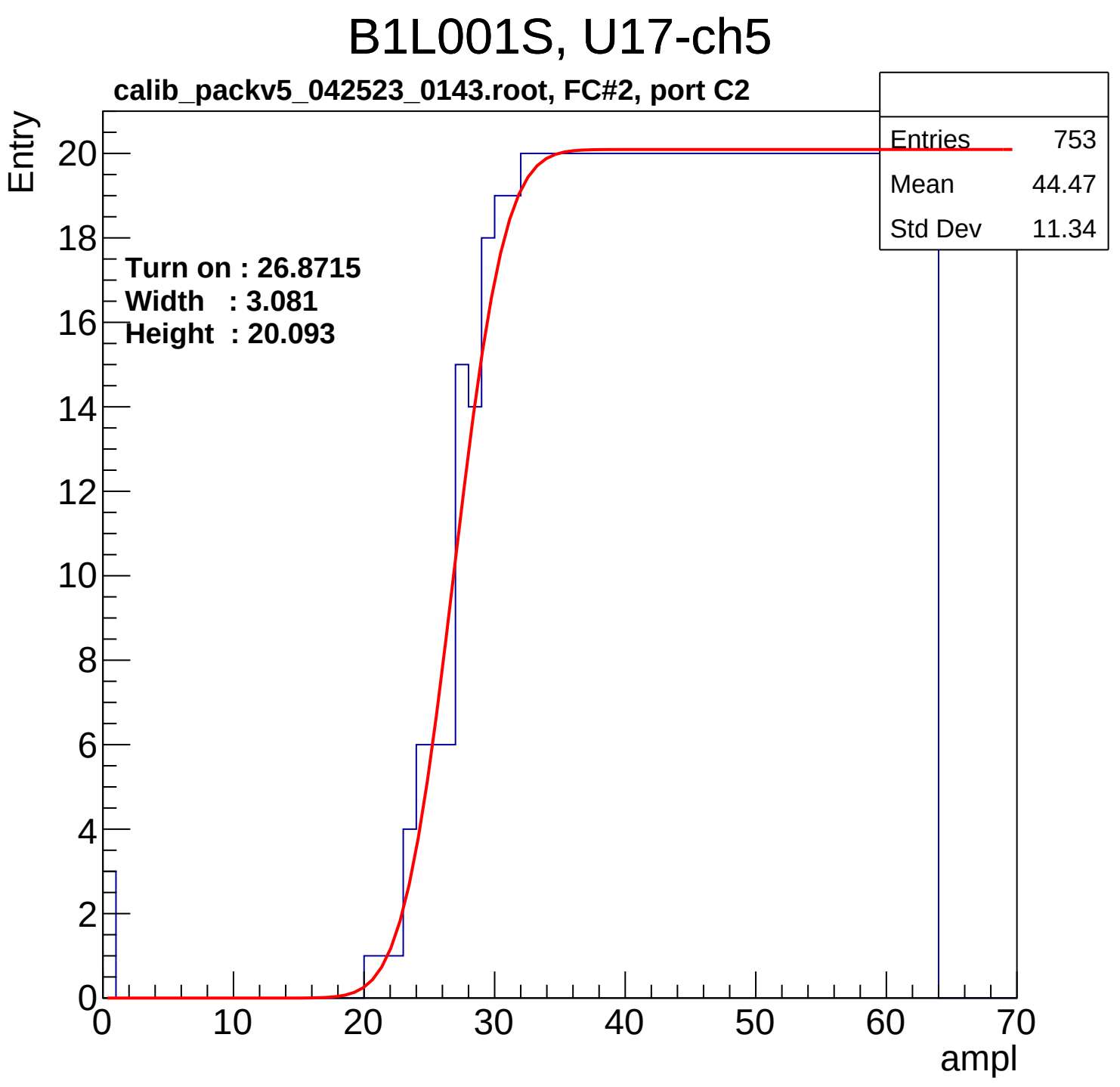
B1L001S, U17-ch5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 753
Mean 44.47
Std Dev 11.34
Turn on : 26.8715
Width : 3.081
Height : 20.093
Entry
ampl
0
2
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6
8
10
12
14
16
18
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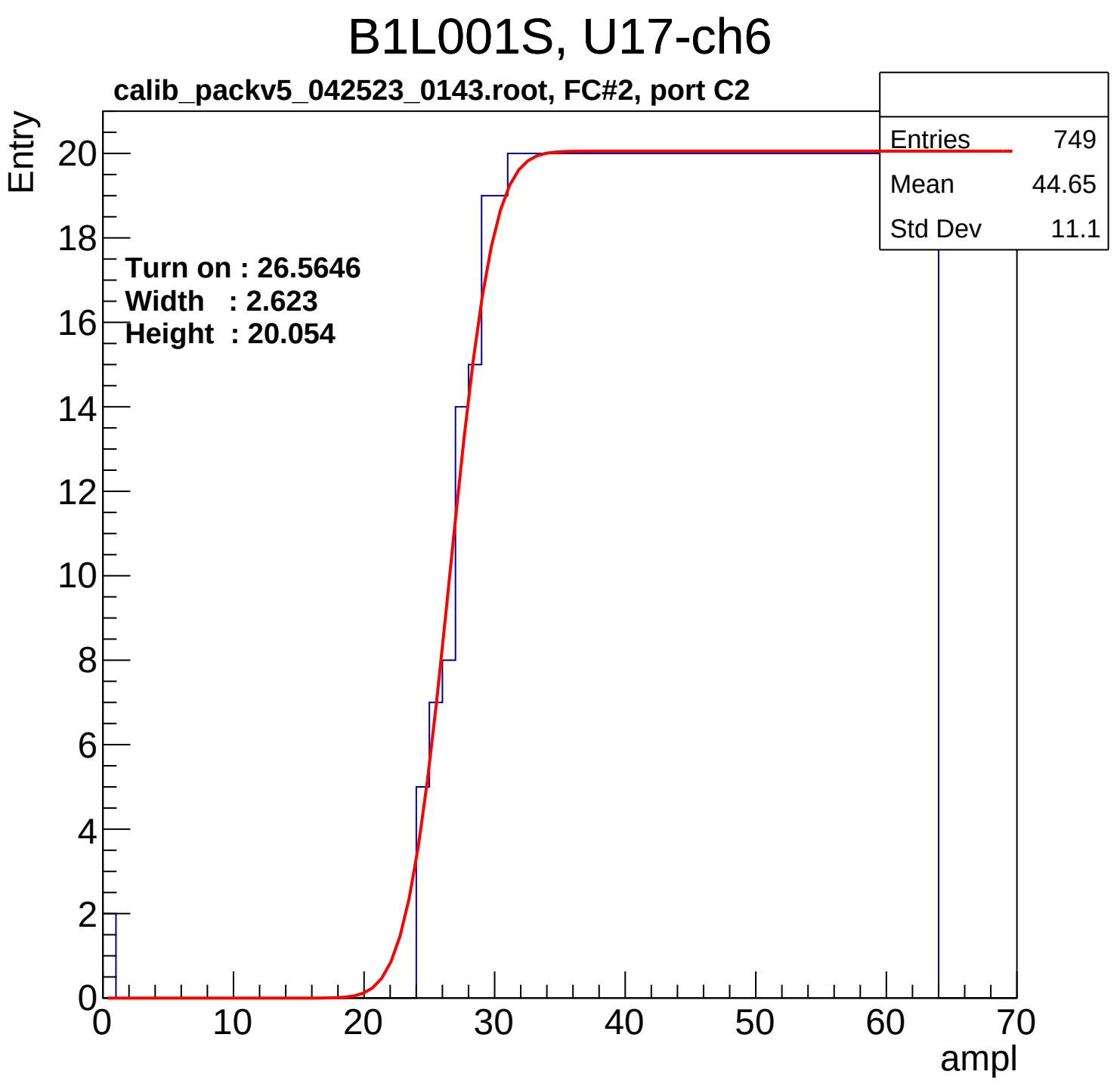
B1L001S, U17-ch6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 749
Mean 44.65
Std Dev 11.1
Turn on : 26.5646
Width : 2.623
Height : 20.054
Entry
ampl
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6
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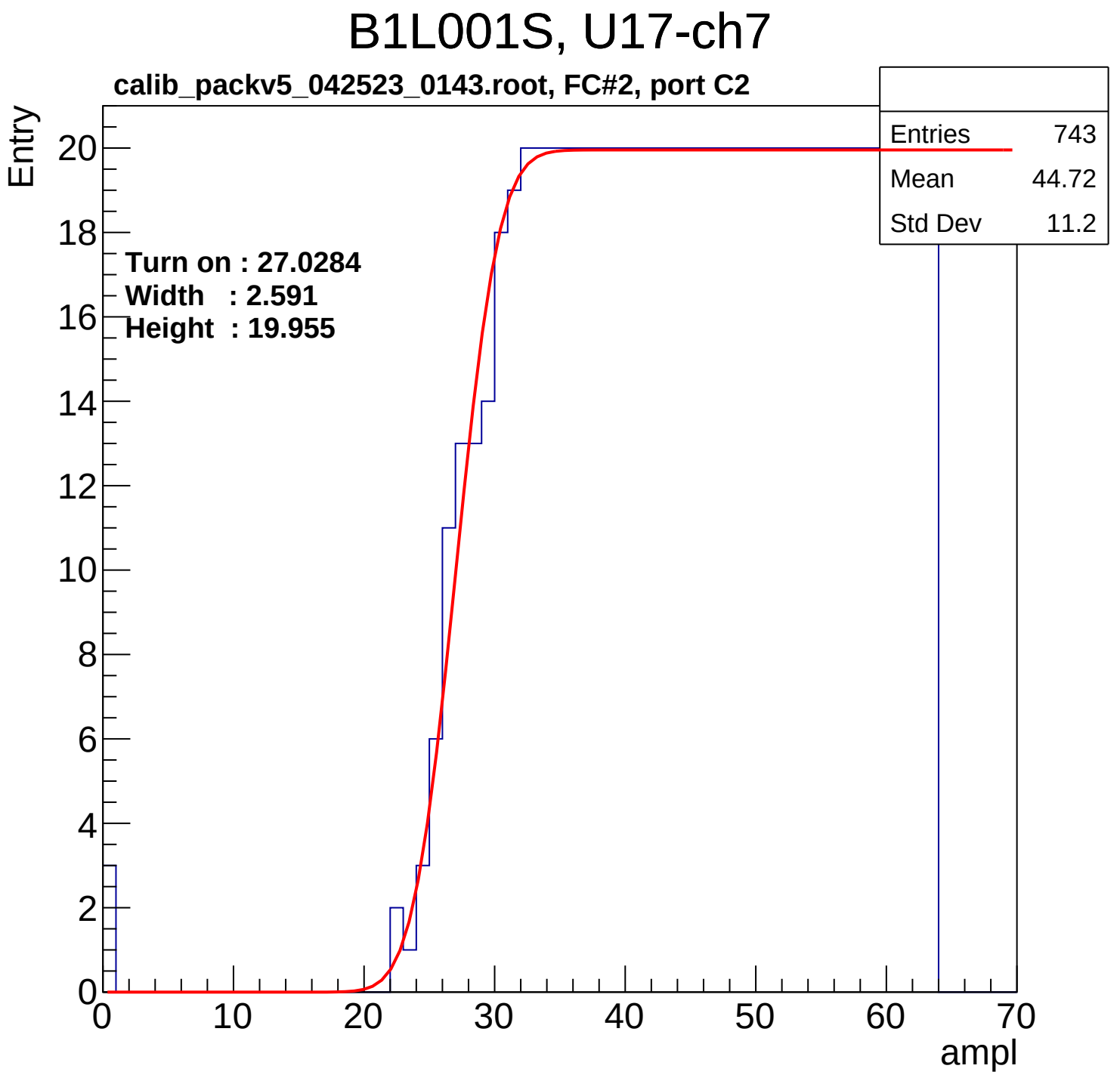
B1L001S, U17-ch7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 743
Mean 44.72
Std Dev 11.2
Turn on : 27.0284
Width : 2.591
Height : 19.955
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
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40
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60
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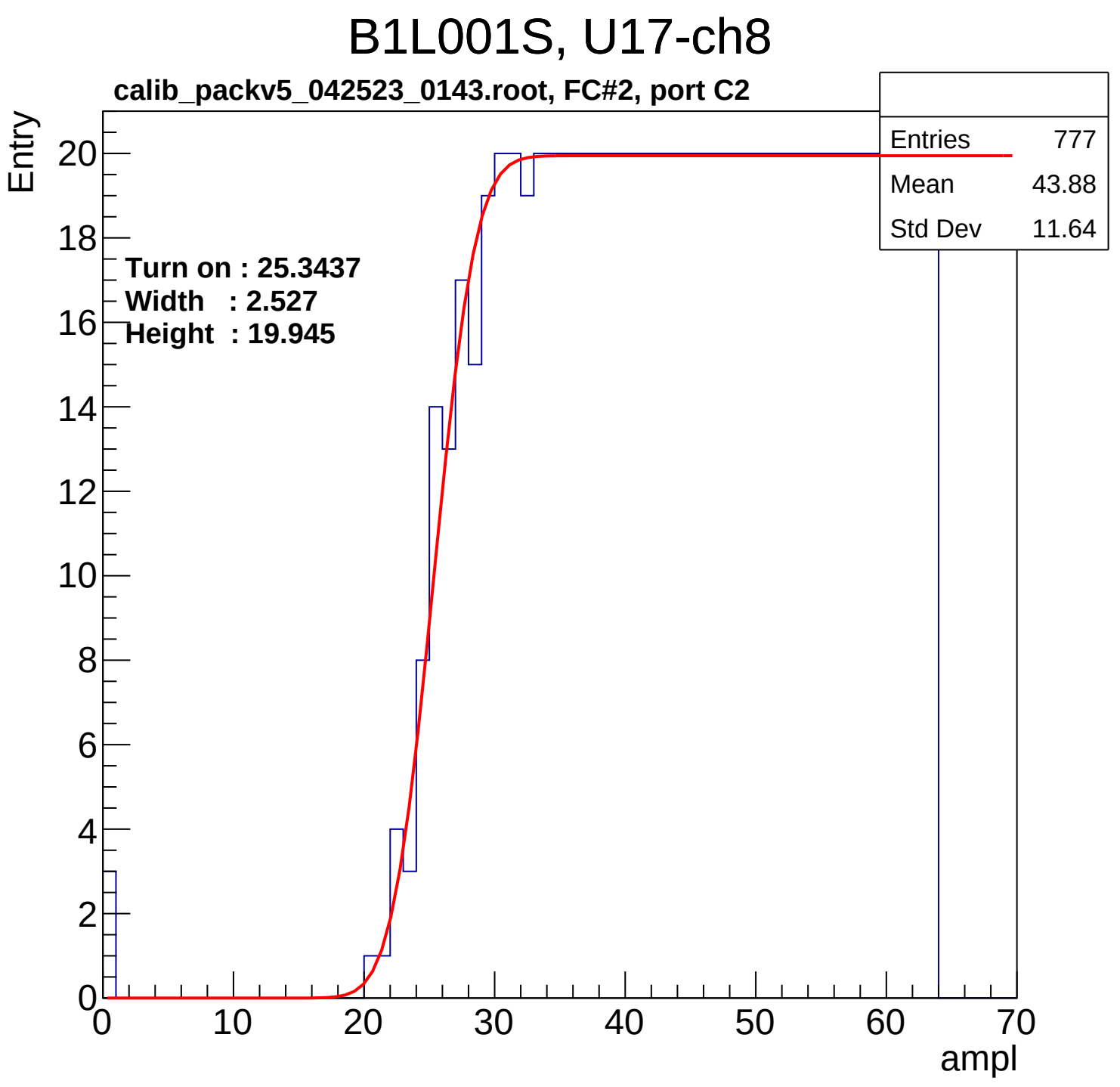
B1L001S, U17-ch8
calib_packv5_042523_0143.root, FC#2, port C2
Entries 777
Mean 43.88
Std Dev 11.64
Turn on : 25.3437
Width : 2.527
Height : 19.945
Entry
ampl
0
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6
8
10
12
14
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18
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0
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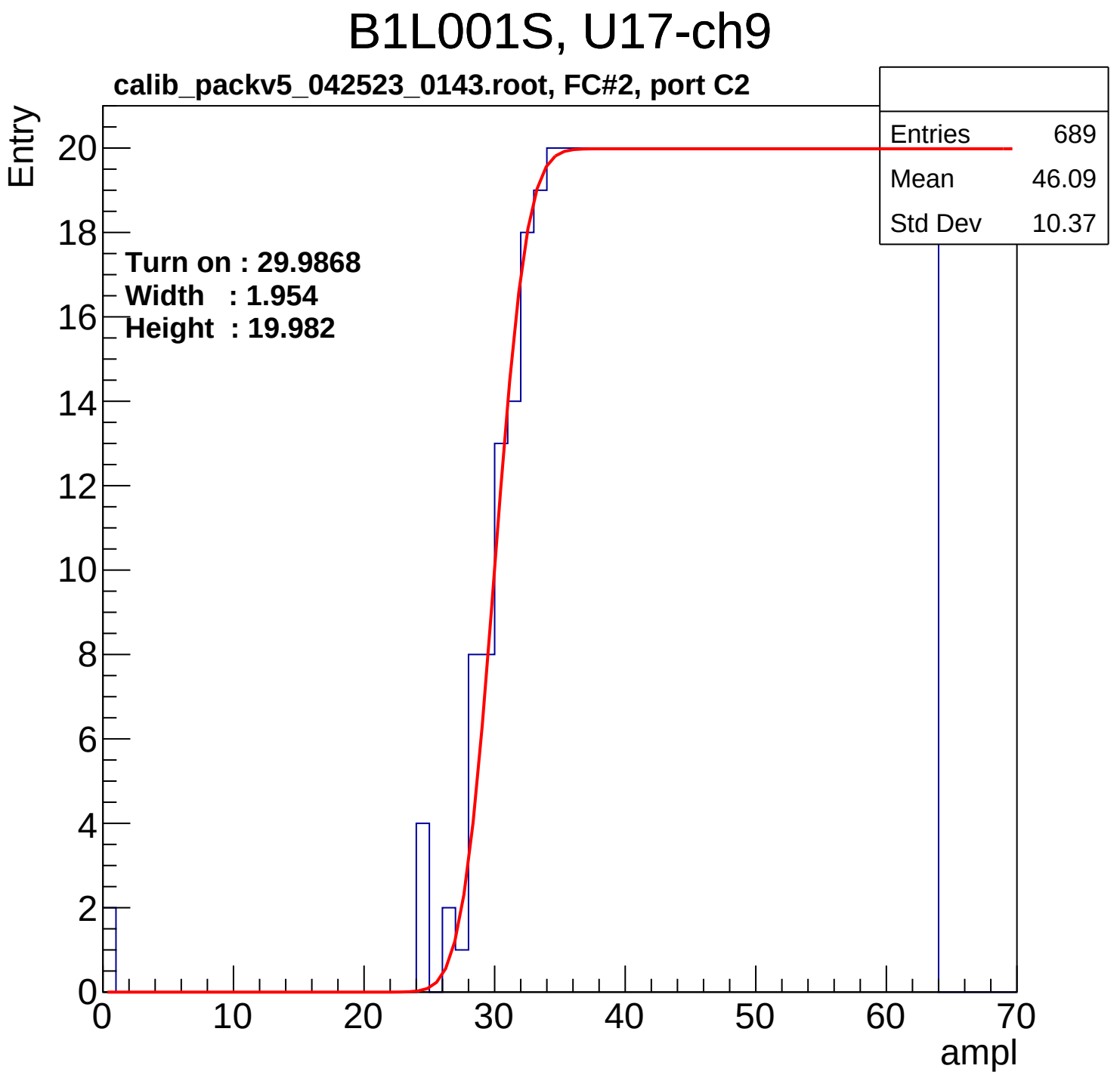
B1L001S, U17-ch9
calib_packv5_042523_0143.root, FC#2, port C2
Entries 689
Mean 46.09
Std Dev 10.37
Turn on : 29.9868
Width : 1.954
Height : 19.982
Entry
ampl
0
2
4
6
8
10
12
14
16
18
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0
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20
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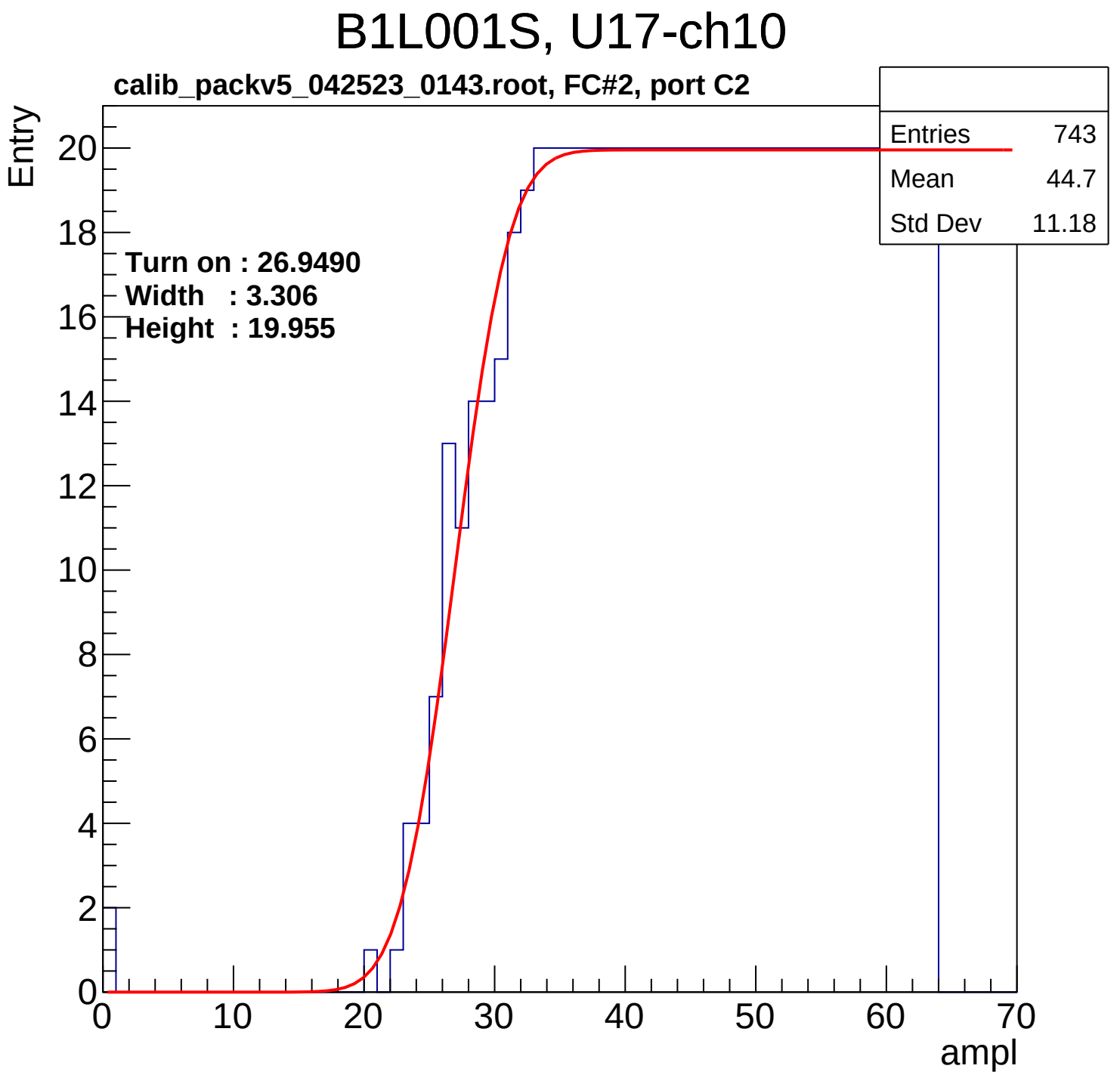
B1L001S, U17-ch10
calib_packv5_042523_0143.root, FC#2, port C2
Entries 743
Mean 44.7
Std Dev 11.18
Turn on : 26.9490
Width : 3.306
Height : 19.955
Entry
ampl
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6
8
10
12
14
16
18
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0
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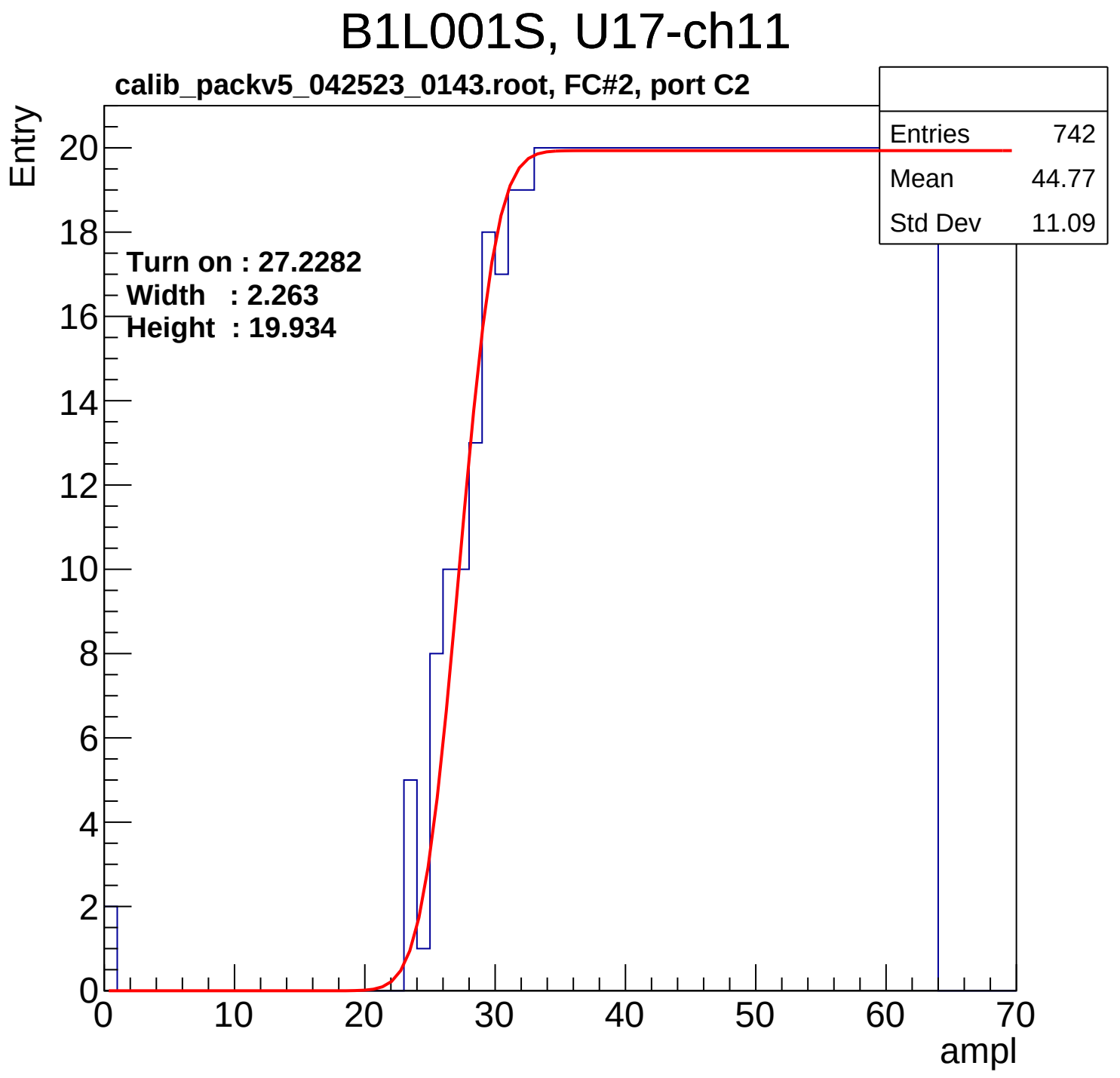
B1L001S, U17-ch11
calib_packv5_042523_0143.root, FC#2, port C2
Entries 742
Mean 44.77
Std Dev 11.09
Turn on : 27.2282
Width : 2.263
Height : 19.934
Entry
ampl
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4
6
8
10
12
14
16
18
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0
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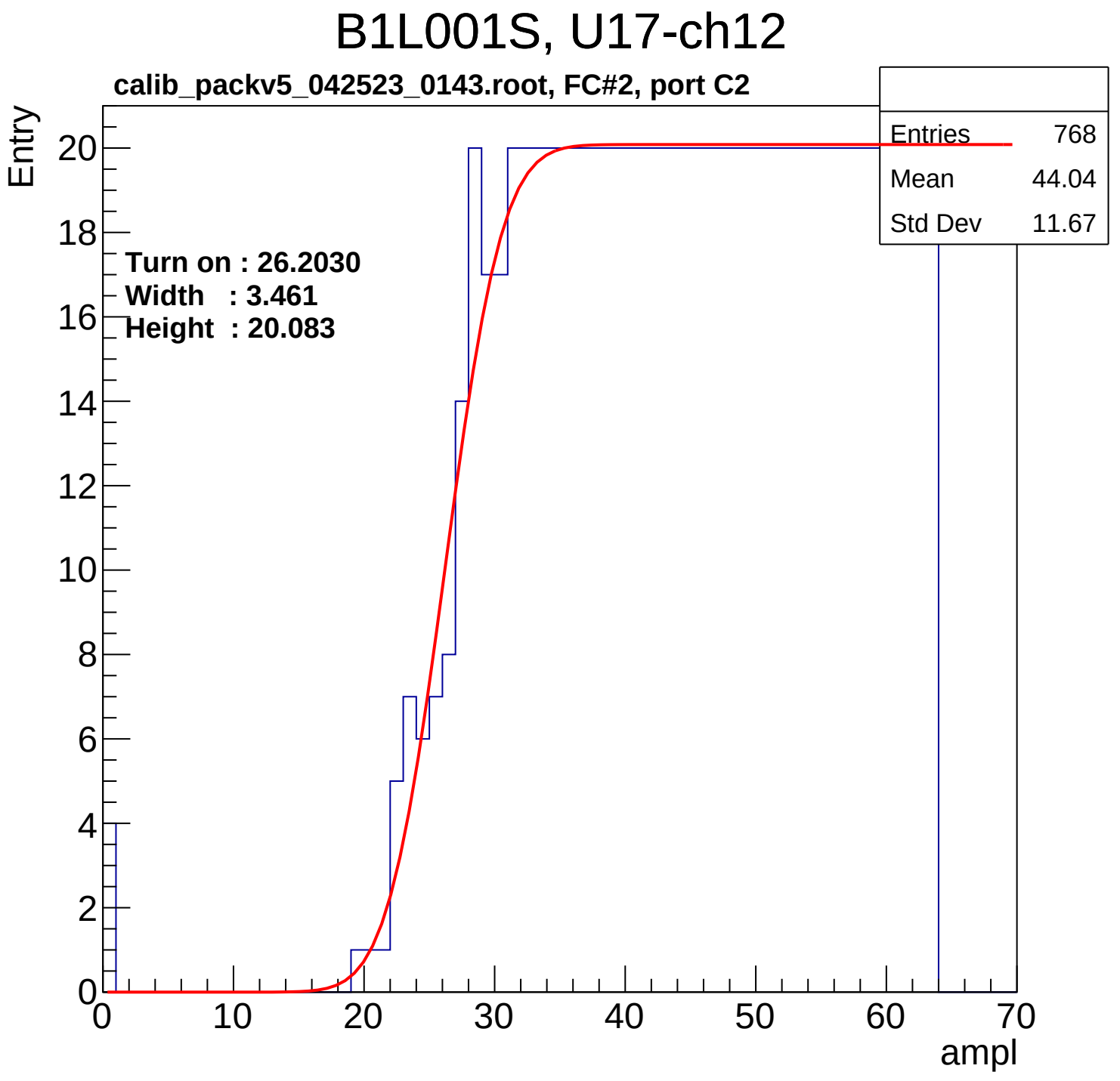
B1L001S, U17-ch12
calib_packv5_042523_0143.root, FC#2, port C2
Entries 768
Mean 44.04
Std Dev 11.67
Turn on : 26.2030
Width : 3.461
Height : 20.083
Entry
ampl
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6
8
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12
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0
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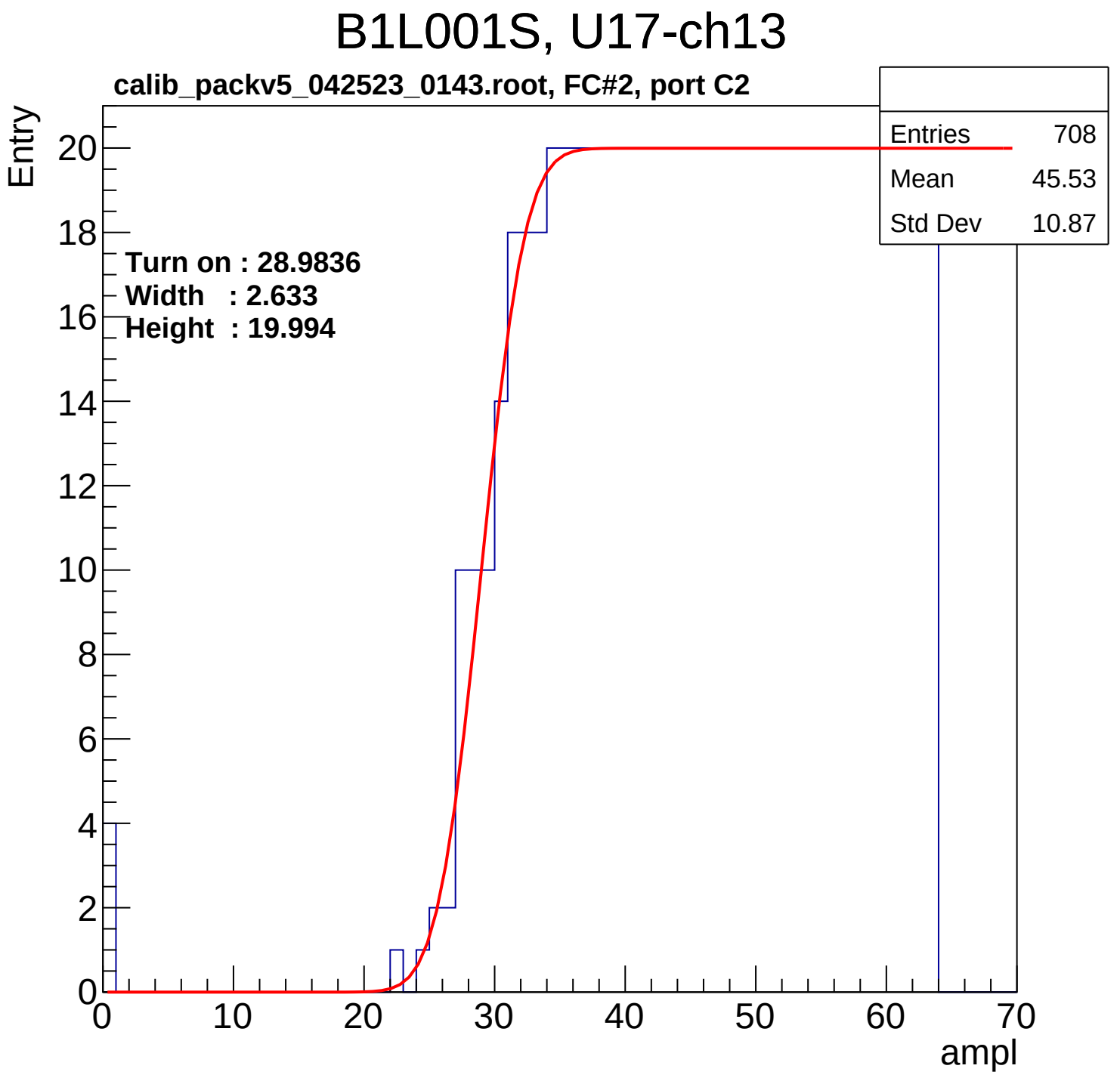
B1L001S, U17-ch13
calib_packv5_042523_0143.root, FC#2, port C2
Entries 708
Mean 45.53
Std Dev 10.87
Turn on : 28.9836
Width : 2.633
Height : 19.994
Entry
ampl
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6
8
10
12
14
16
18
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0
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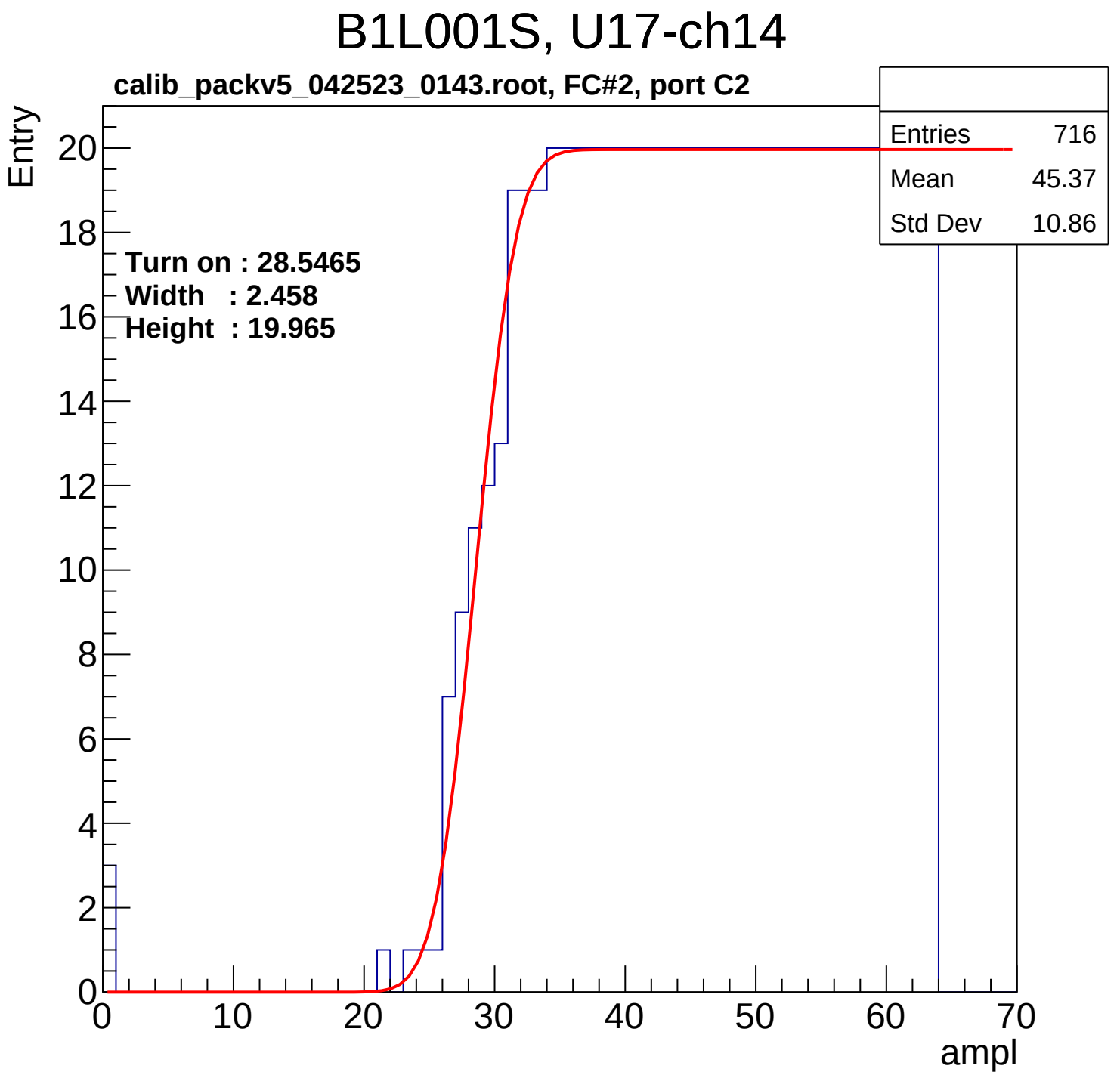
B1L001S, U17-ch14
calib_packv5_042523_0143.root, FC#2, port C2
Entries 716
Mean 45.37
Std Dev 10.86
Turn on : 28.5465
Width : 2.458
Height : 19.965
Entry
ampl
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6
8
10
12
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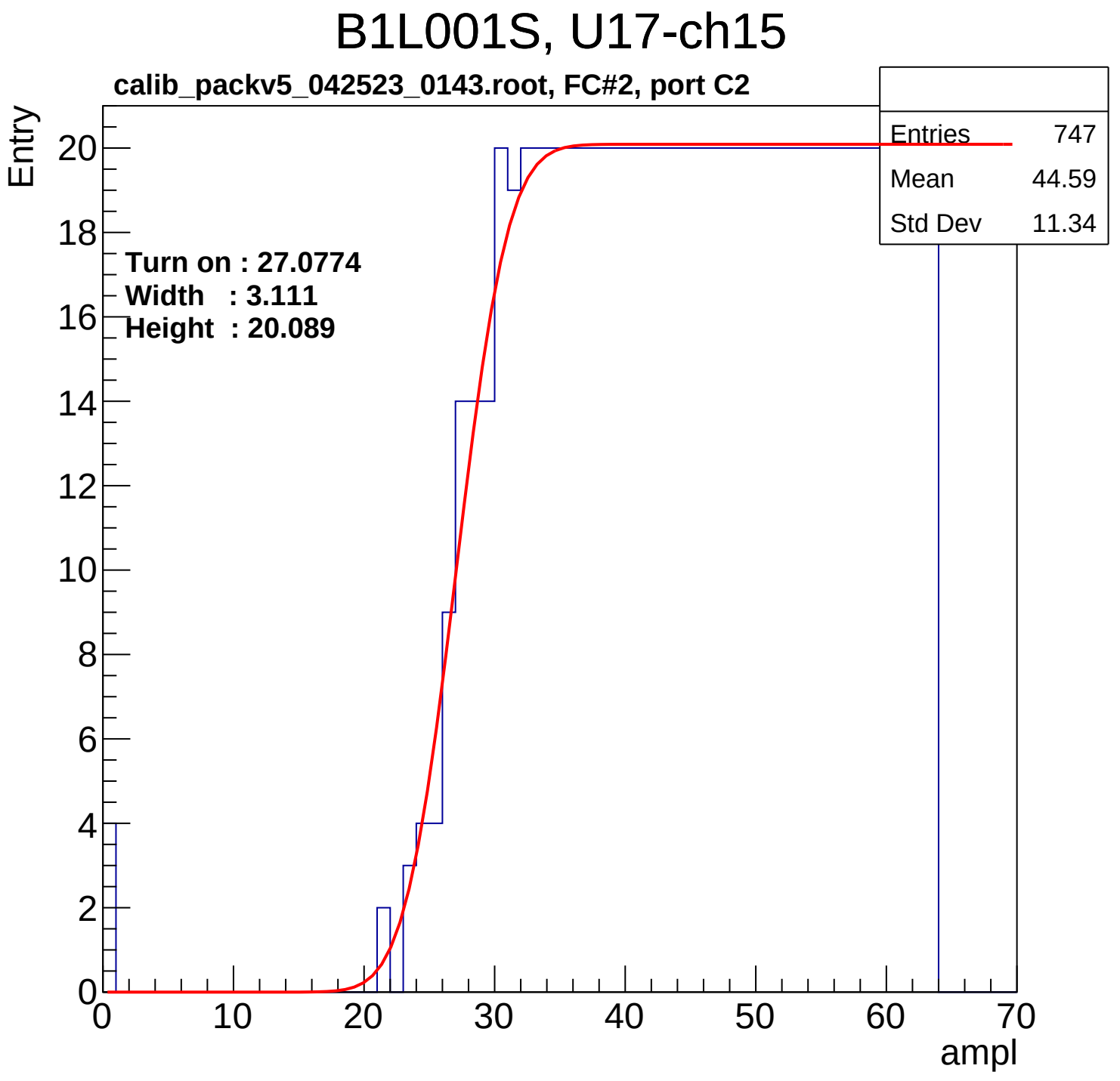
B1L001S, U17-ch15
calib_packv5_042523_0143.root, FC#2, port C2
Entries 747
Mean 44.59
Std Dev 11.34
Turn on : 27.0774
Width : 3.111
Height : 20.089
Entry
ampl
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6
8
10
12
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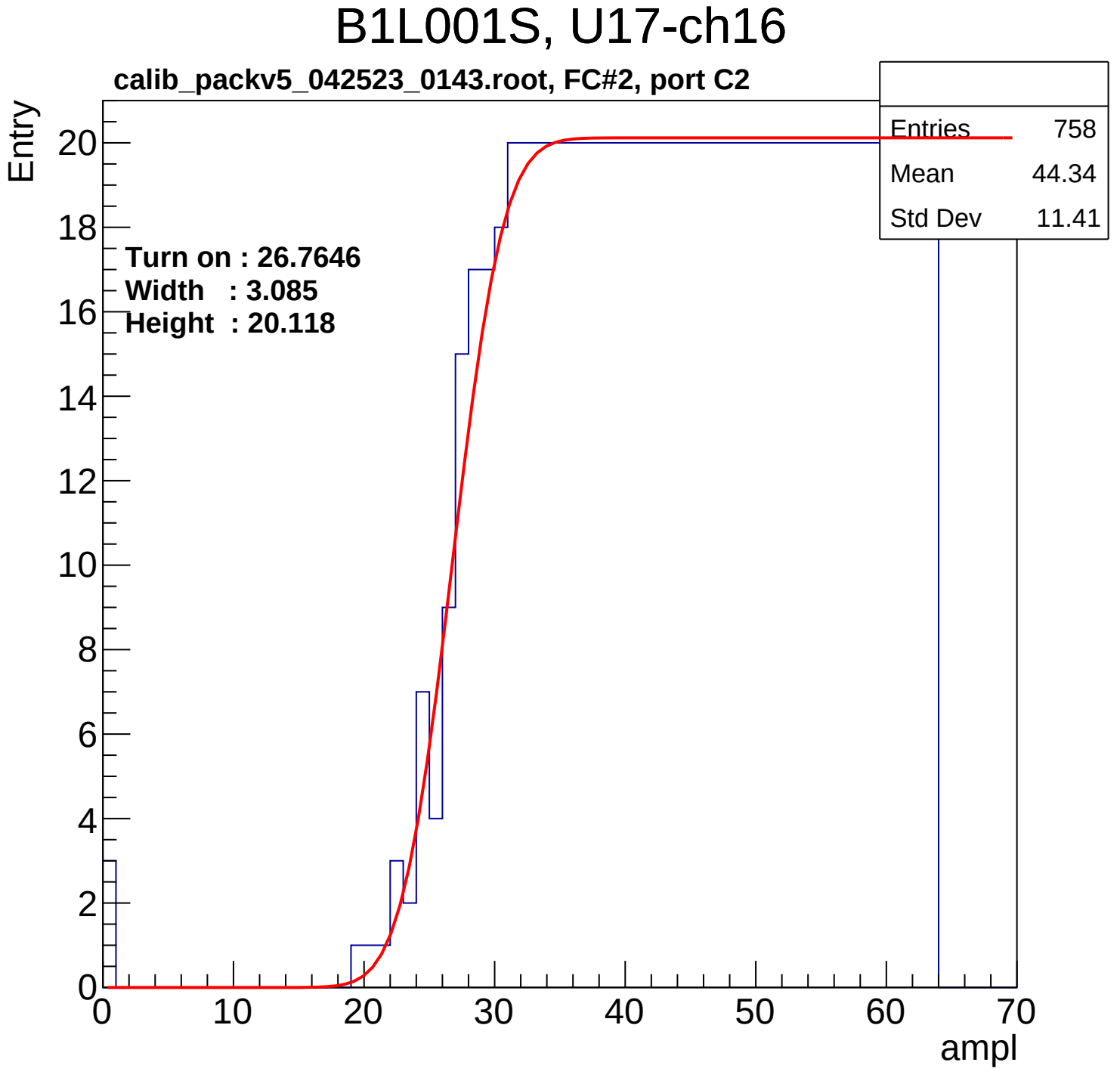
B1L001S, U17-ch16
calib_packv5_042523_0143.root, FC#2, port C2
Entries 758
Mean 44.34
Std Dev 11.41
Turn on : 26.7646
Width : 3.085
Height : 20.118
Entry
ampl
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10
12
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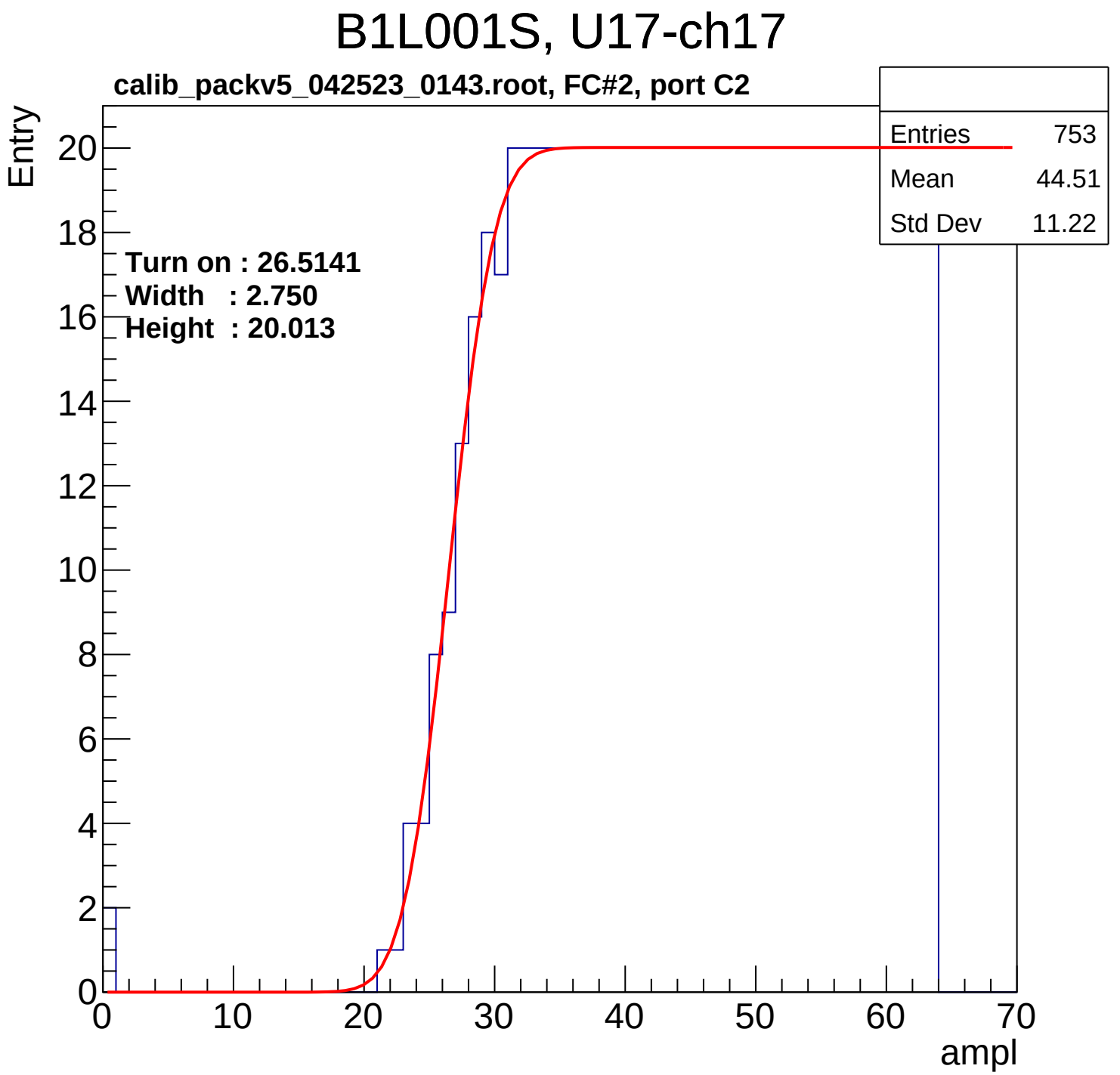
B1L001S, U17-ch17
calib_packv5_042523_0143.root, FC#2, port C2
Entries 753
Mean 44.51
Std Dev 11.22
Turn on : 26.5141
Width : 2.750
Height : 20.013
Entry
ampl
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6
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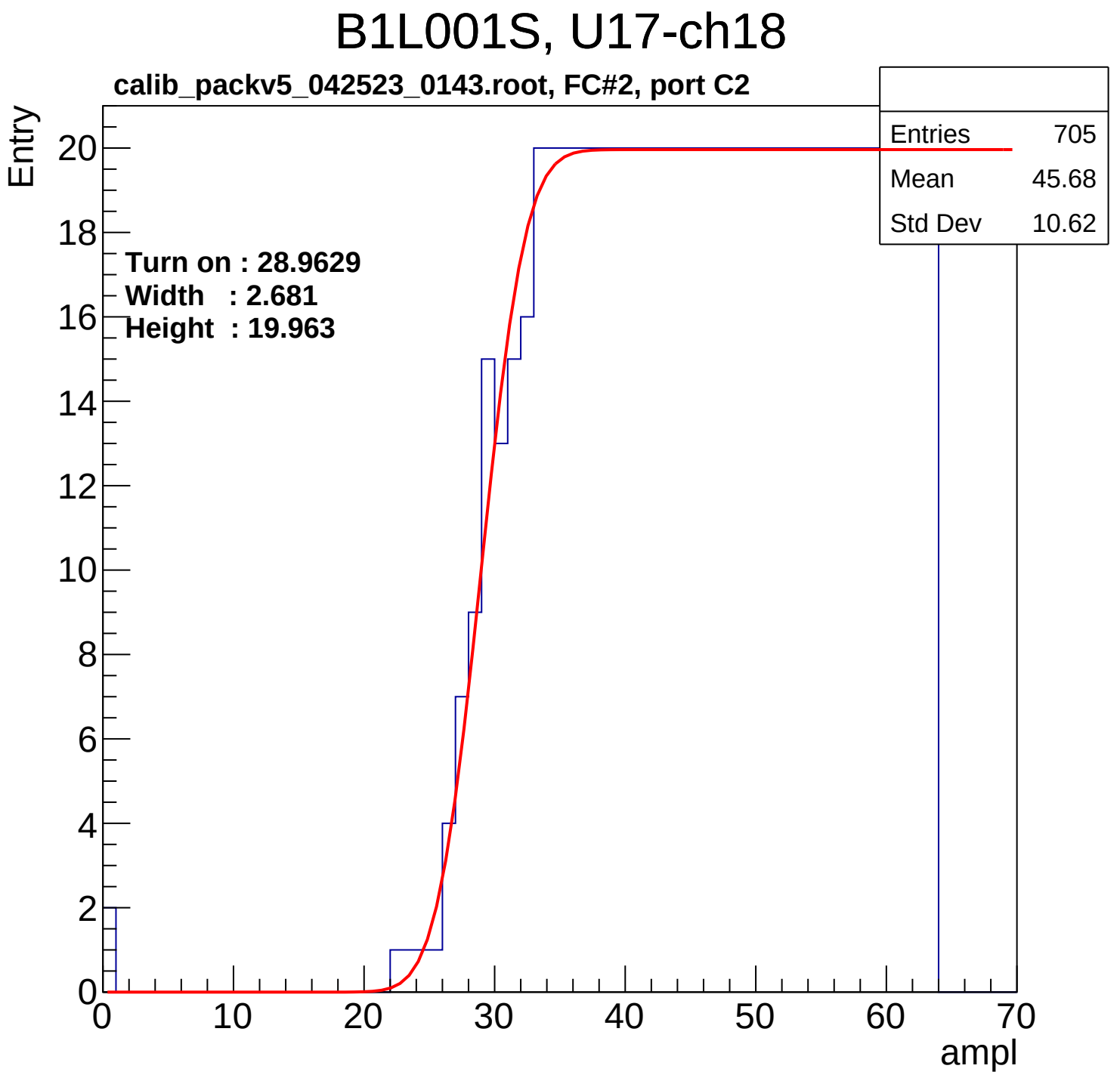
B1L001S, U17-ch18
calib_packv5_042523_0143.root, FC#2, port C2
Entries 705
Mean 45.68
Std Dev 10.62
Turn on : 28.9629
Width : 2.681
Height : 19.963
Entry
ampl
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6
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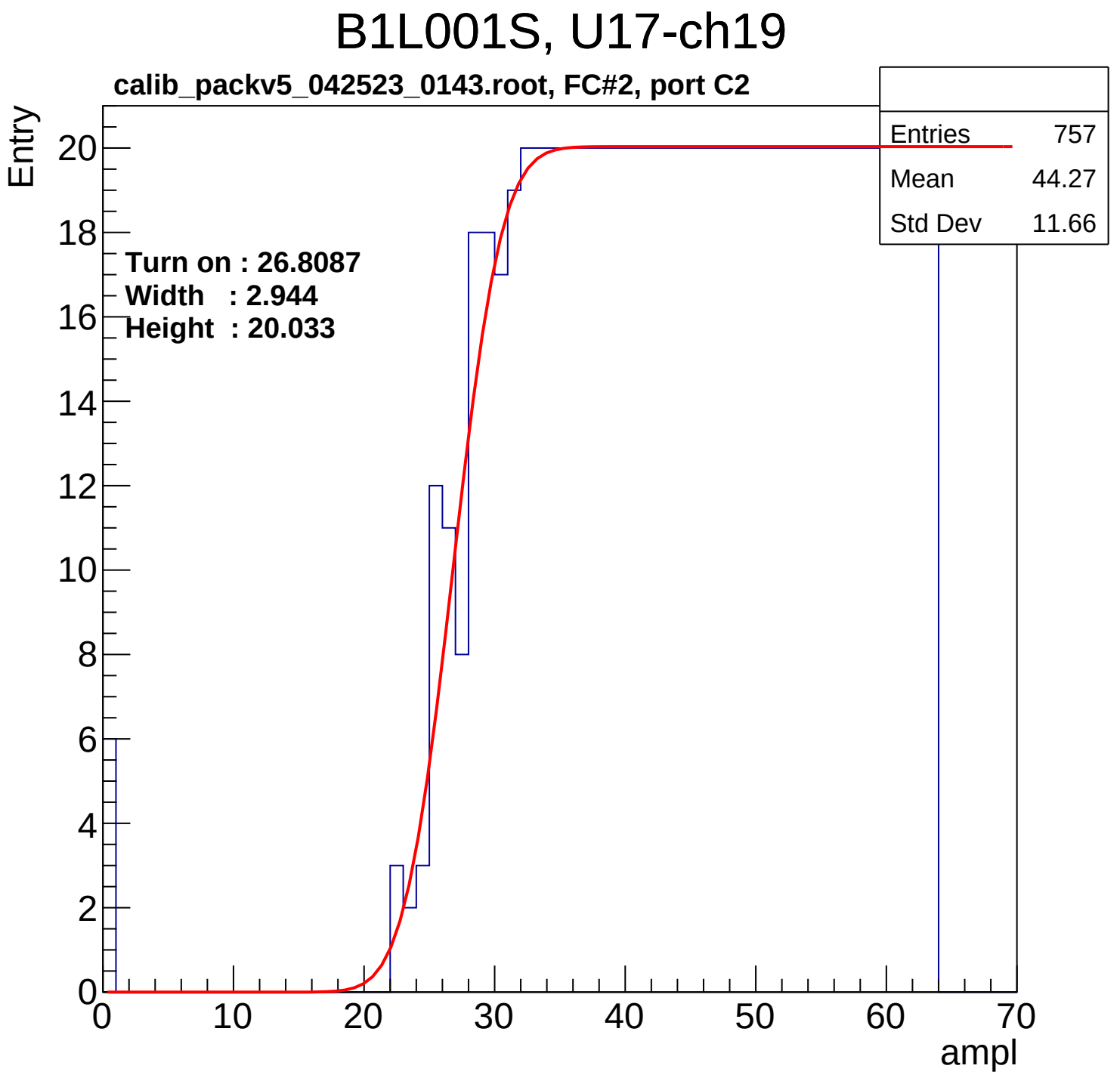
B1L001S, U17-ch19
calib_packv5_042523_0143.root, FC#2, port C2
Entries 757
Mean 44.27
Std Dev 11.66
Turn on : 26.8087
Width : 2.944
Height : 20.033
Entry
ampl
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6
8
10
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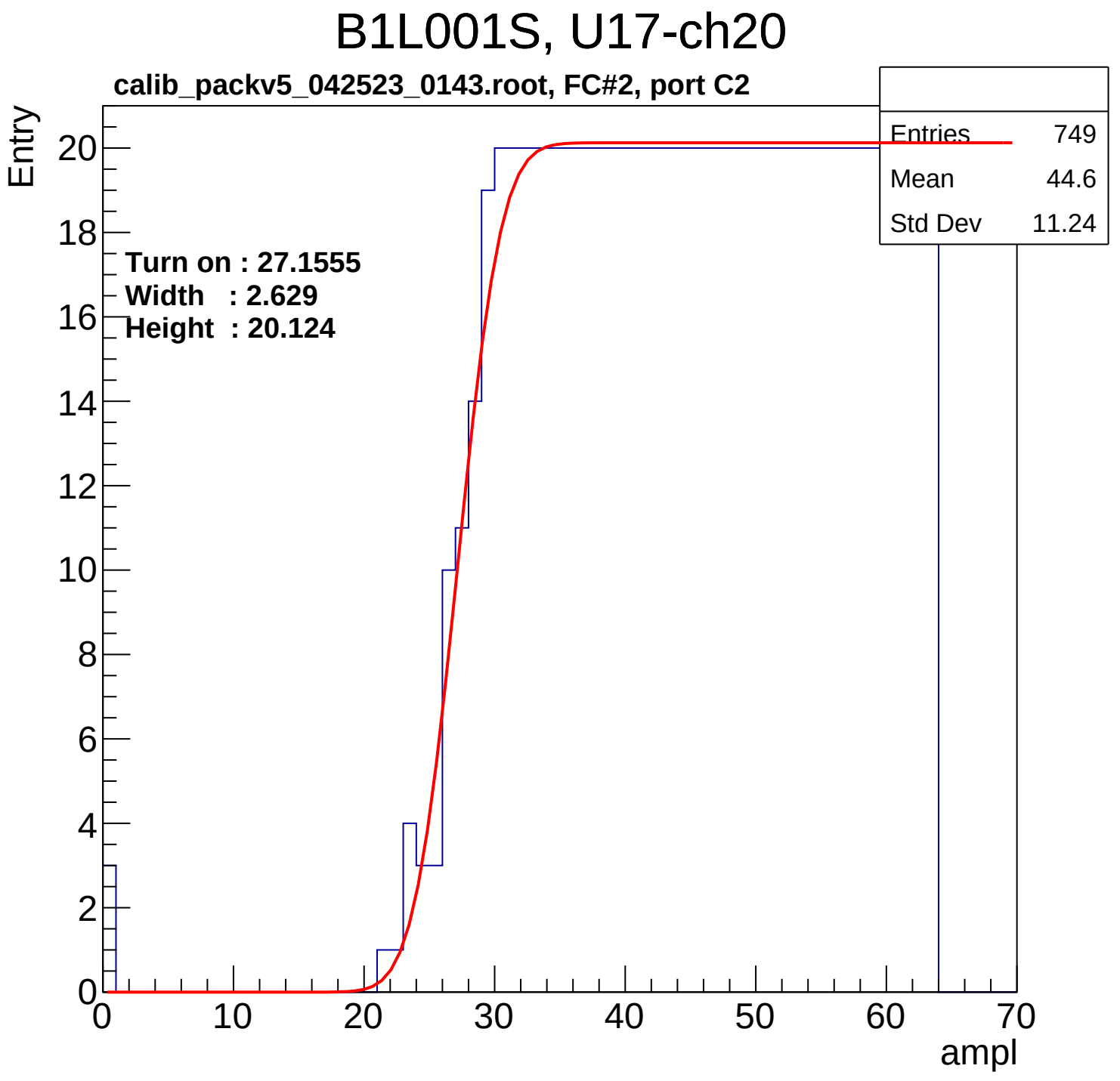
B1L001S, U17-ch20
calib_packv5_042523_0143.root, FC#2, port C2
Entries 749
Mean 44.6
Std Dev 11.24
Turn on : 27.1555
Width : 2.629
Height : 20.124
Entry
ampl
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6
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10
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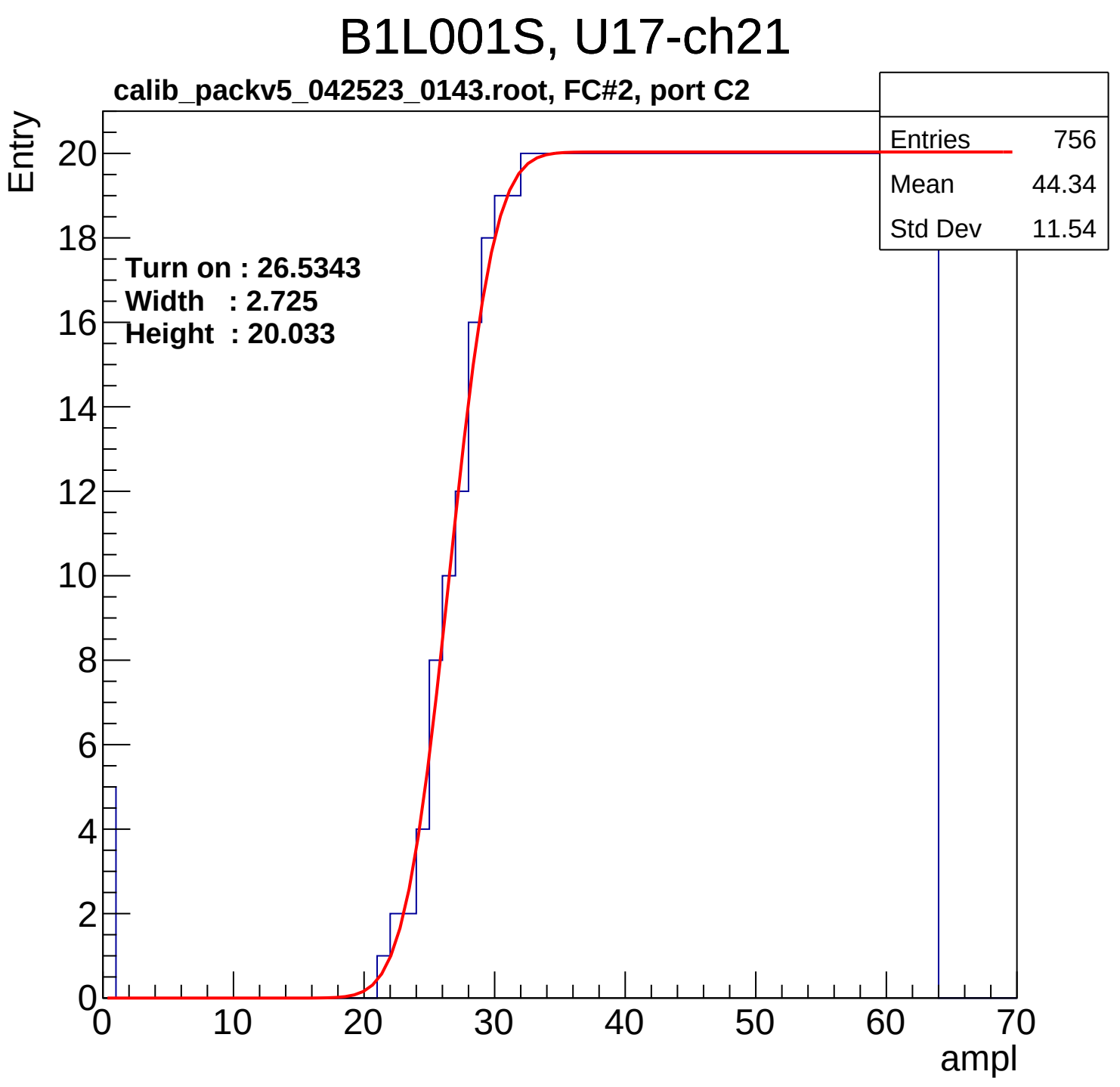
B1L001S, U17-ch21
calib_packv5_042523_0143.root, FC#2, port C2
Entries 756
Mean 44.34
Std Dev 11.54
Turn on : 26.5343
Width : 2.725
Height : 20.033
Entry
ampl
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6
8
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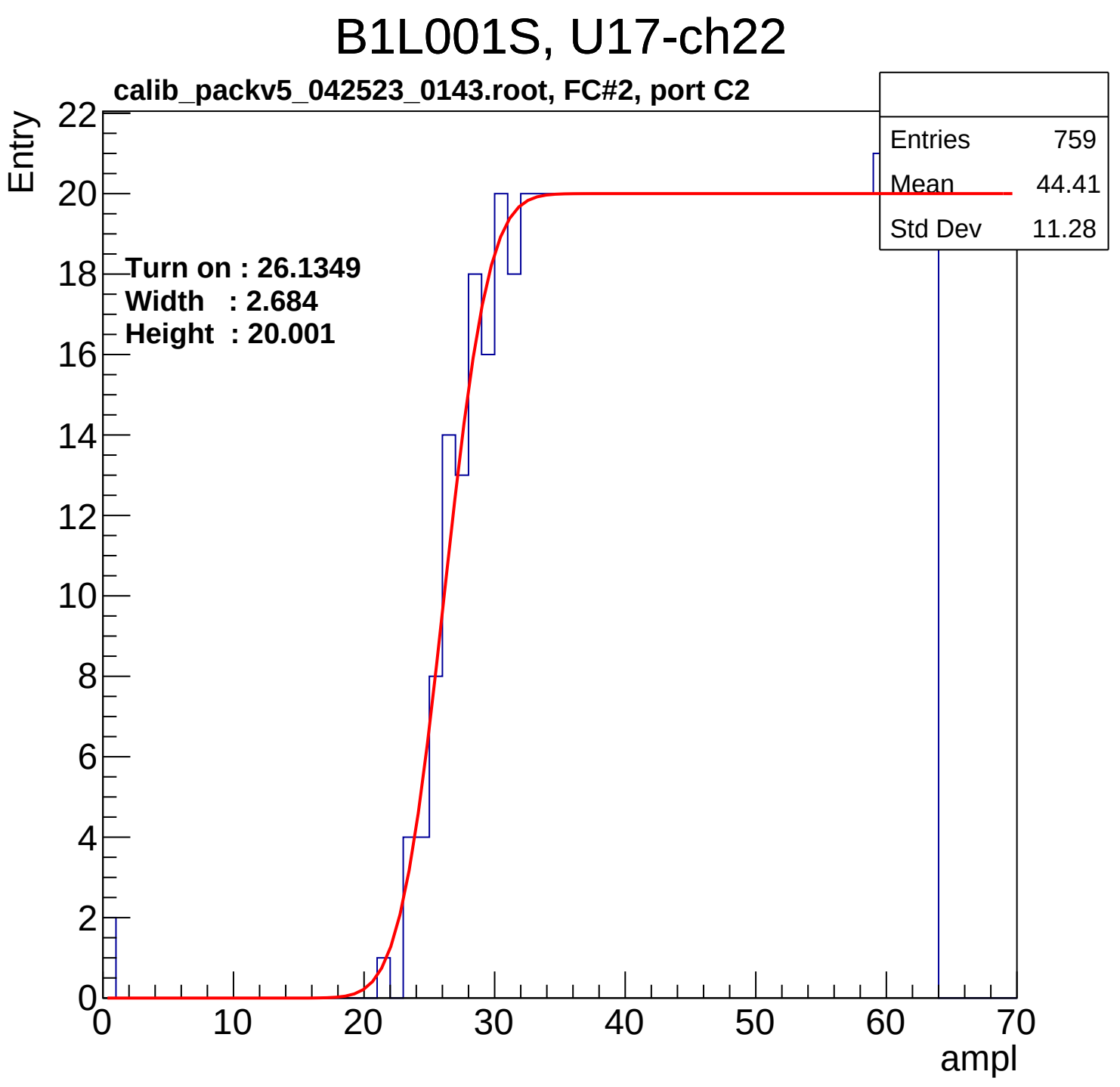
B1L001S, U17-ch22
calib_packv5_042523_0143.root, FC#2, port C2
Entries 759
Mean 44.41
Std Dev 11.28
Turn on : 26.1349
Width : 2.684
Height : 20.001
Entry
ampl
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10
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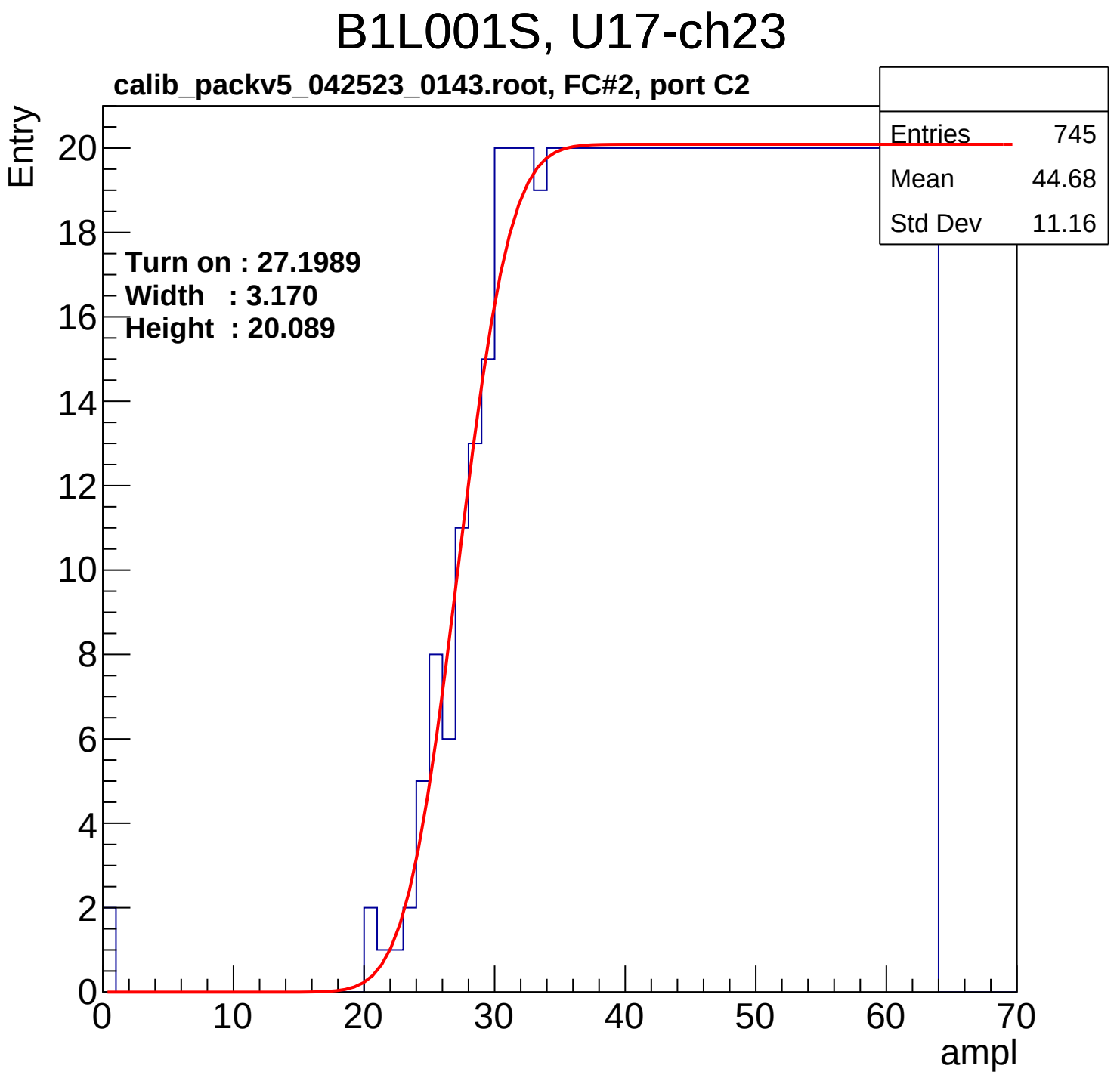
B1L001S, U17-ch23
calib_packv5_042523_0143.root, FC#2, port C2
Entries 745
Mean 44.68
Std Dev 11.16
Turn on : 27.1989
Width : 3.170
Height : 20.089
Entry
ampl
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6
8
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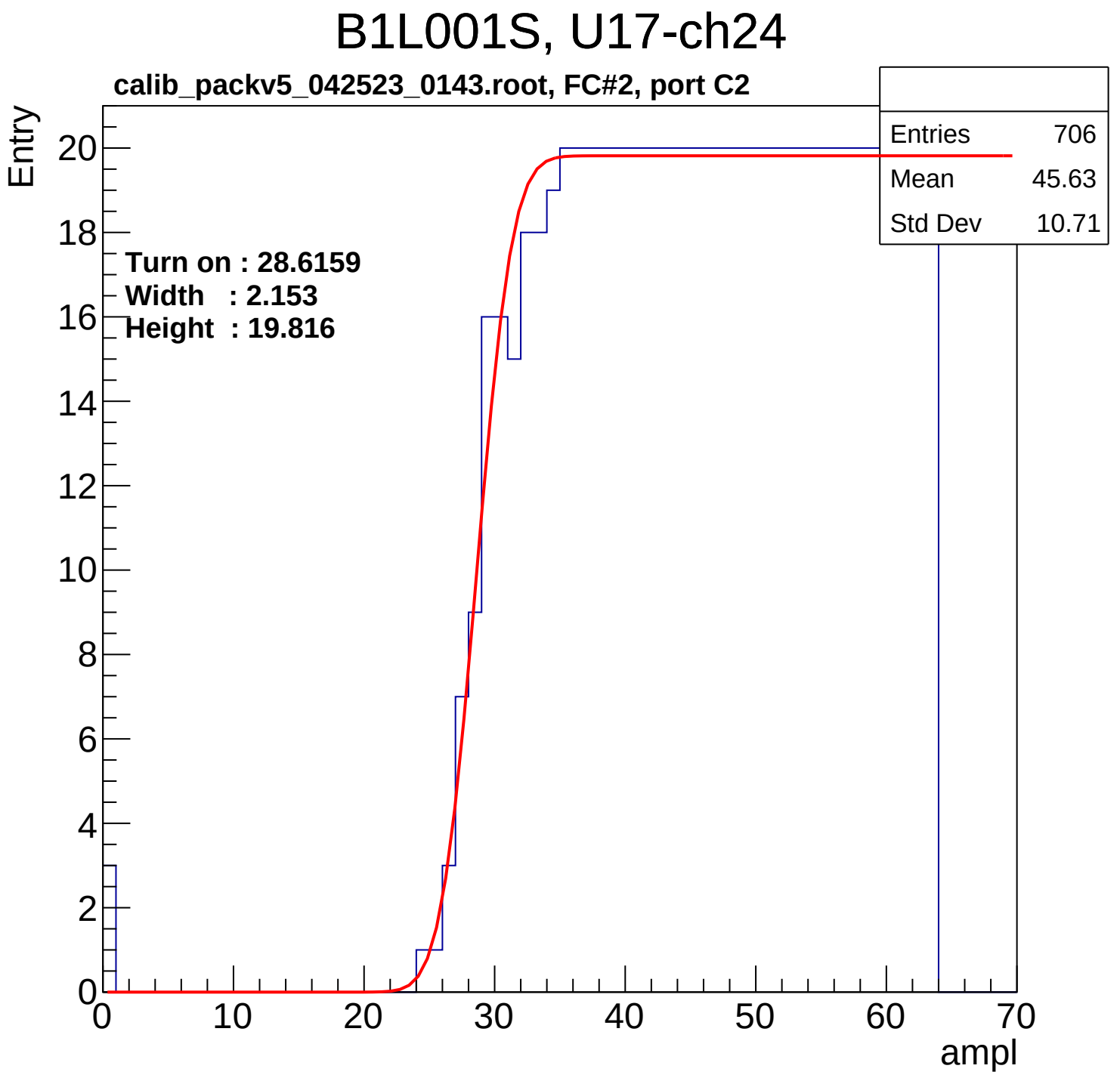
B1L001S, U17-ch24
calib_packv5_042523_0143.root, FC#2, port C2
Entries 706
Mean 45.63
Std Dev 10.71
Turn on : 28.6159
Width : 2.153
Height : 19.816
Entry
ampl
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8
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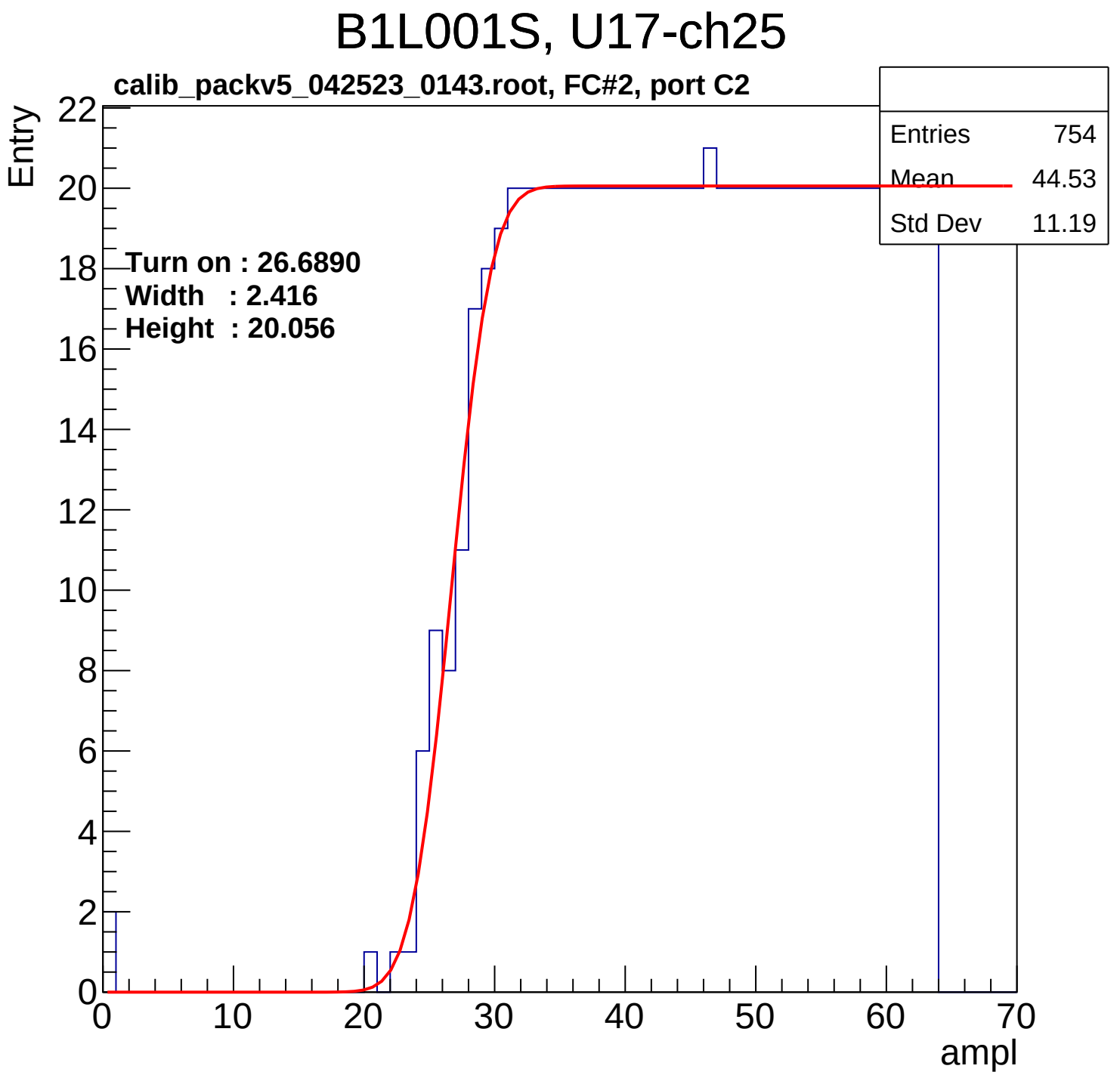
B1L001S, U17-ch25
calib_packv5_042523_0143.root, FC#2, port C2
Entry
ampl
Entries 754
Mean 44.53
Std Dev 11.19
Turn on : 26.6890
Width : 2.416
Height : 20.056
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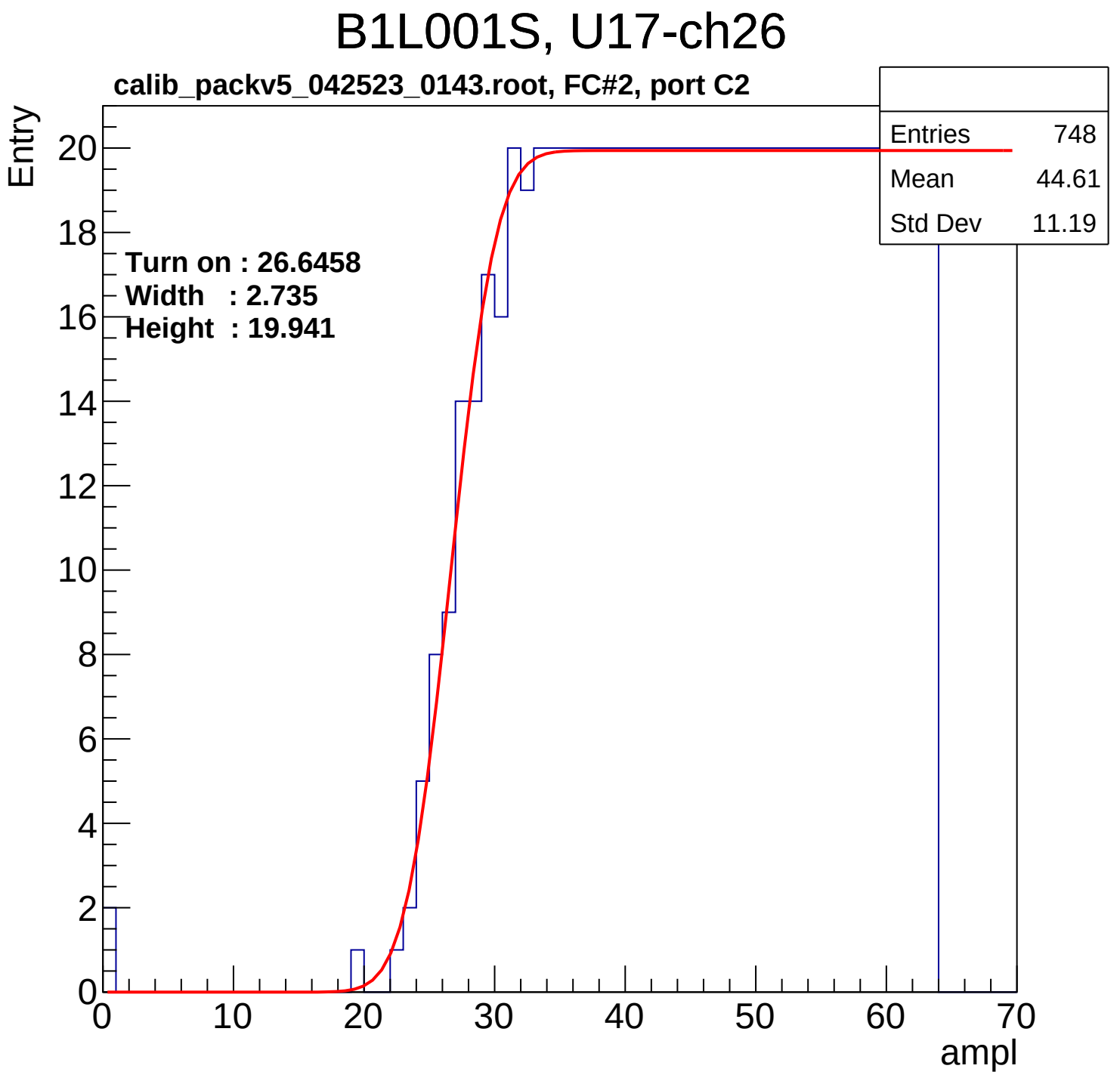
B1L001S, U17-ch26
calib_packv5_042523_0143.root, FC#2, port C2
Entries 748
Mean 44.61
Std Dev 11.19
Turn on : 26.6458
Width : 2.735
Height : 19.941
Entry
ampl
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6
8
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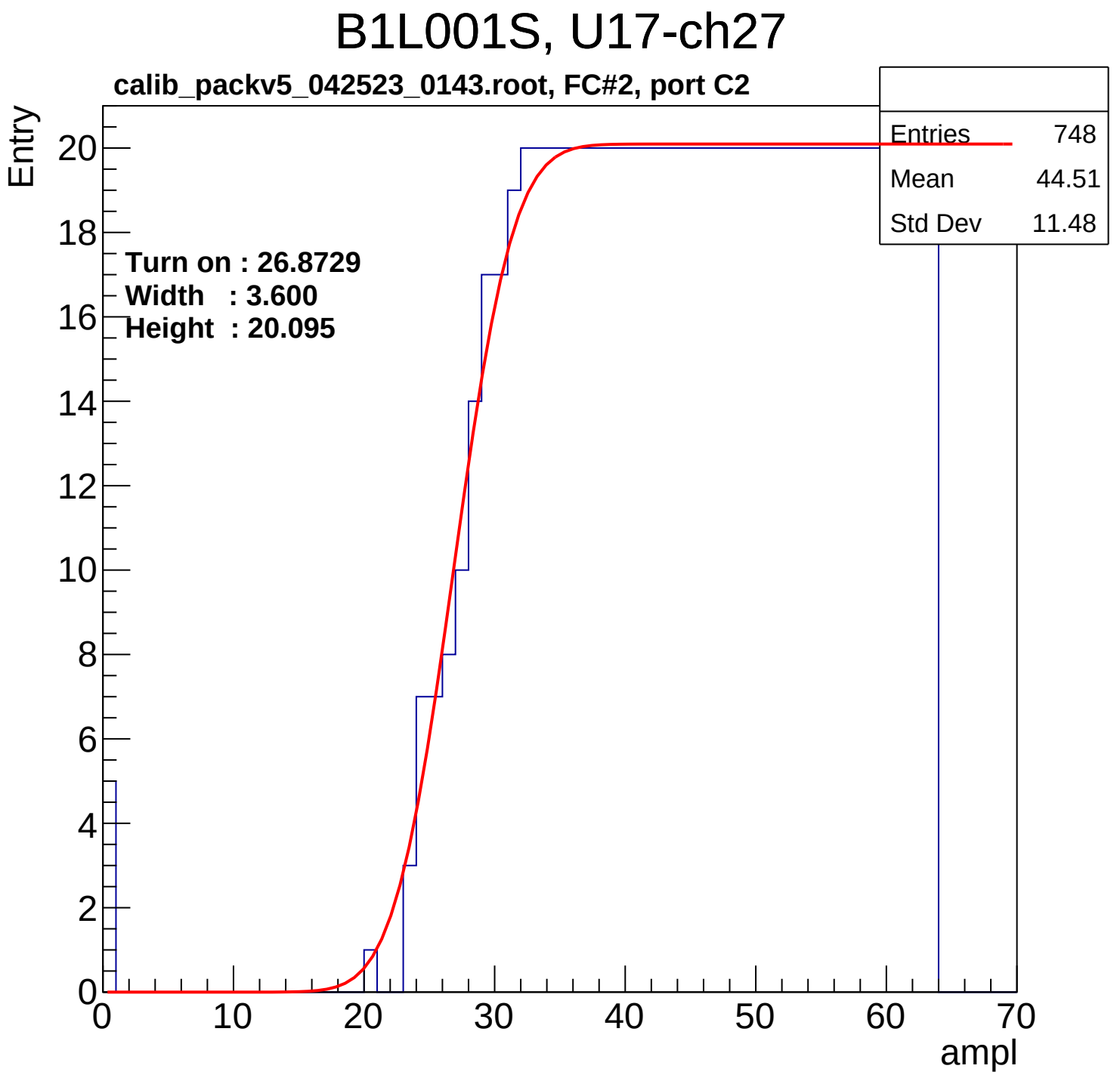
B1L001S, U17-ch27
calib_packv5_042523_0143.root, FC#2, port C2
Entries 748
Mean 44.51
Std Dev 11.48
Turn on : 26.8729
Width : 3.600
Height : 20.095
Entry
ampl
0
2
4
6
8
10
12
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16
18
20
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10
20
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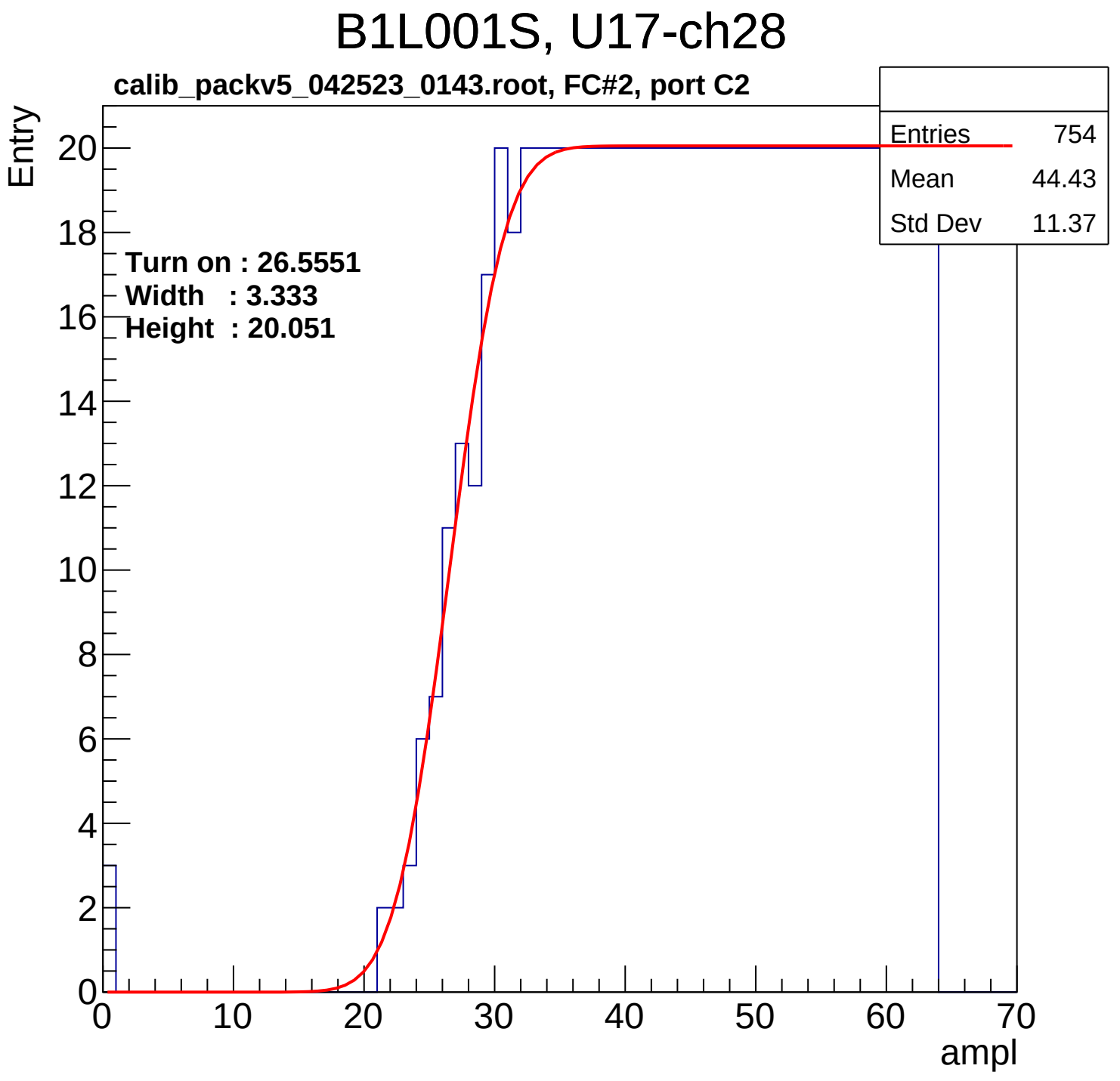
B1L001S, U17-ch28
calib_packv5_042523_0143.root, FC#2, port C2
Entries 754
Mean 44.43
Std Dev 11.37
Turn on : 26.5551
Width : 3.333
Height : 20.051
Entry
ampl
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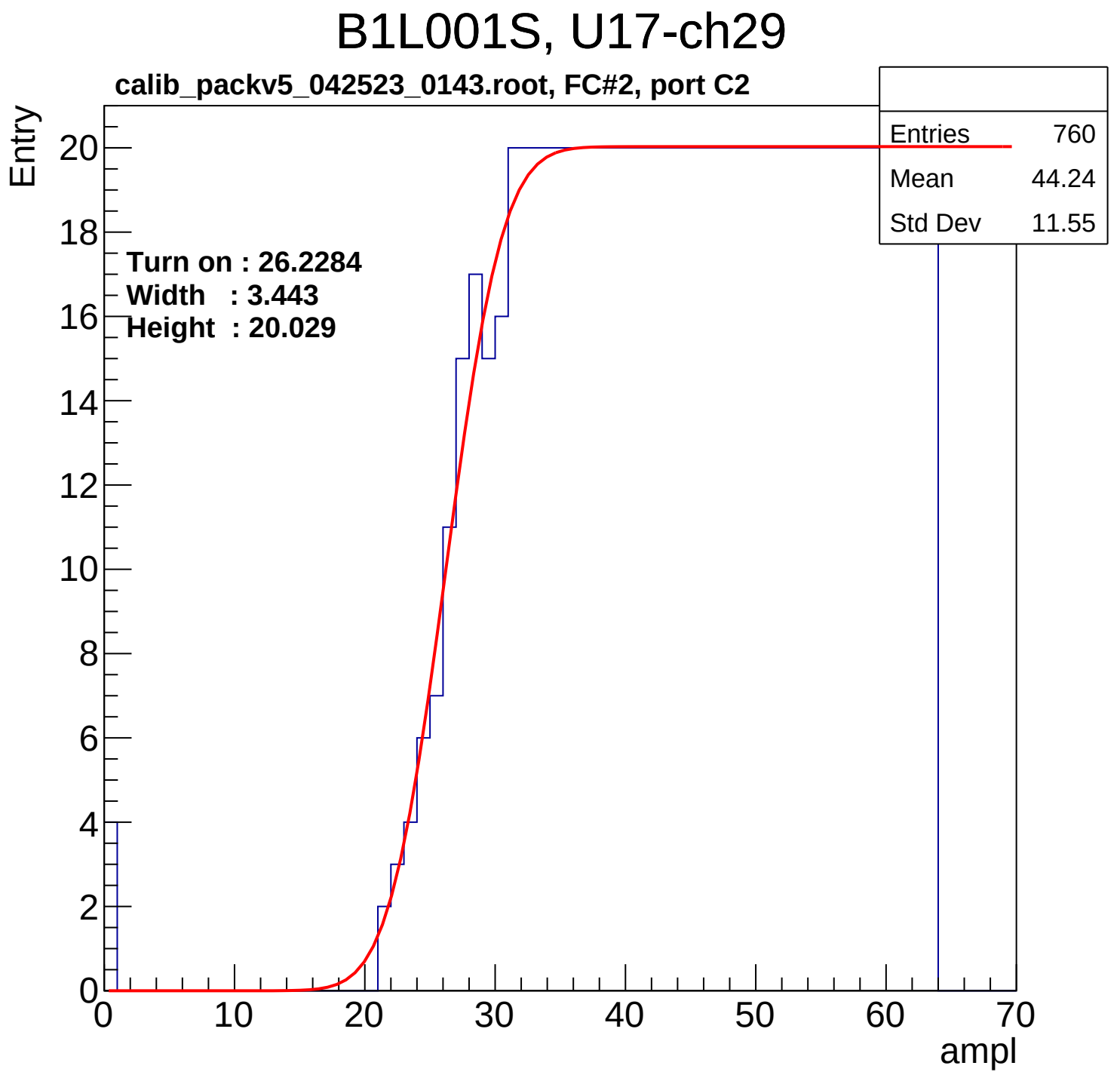
B1L001S, U17-ch29
calib_packv5_042523_0143.root, FC#2, port C2
Entries 760
Mean 44.24
Std Dev 11.55
Turn on : 26.2284
Width : 3.443
Height : 20.029
Entry
ampl
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6
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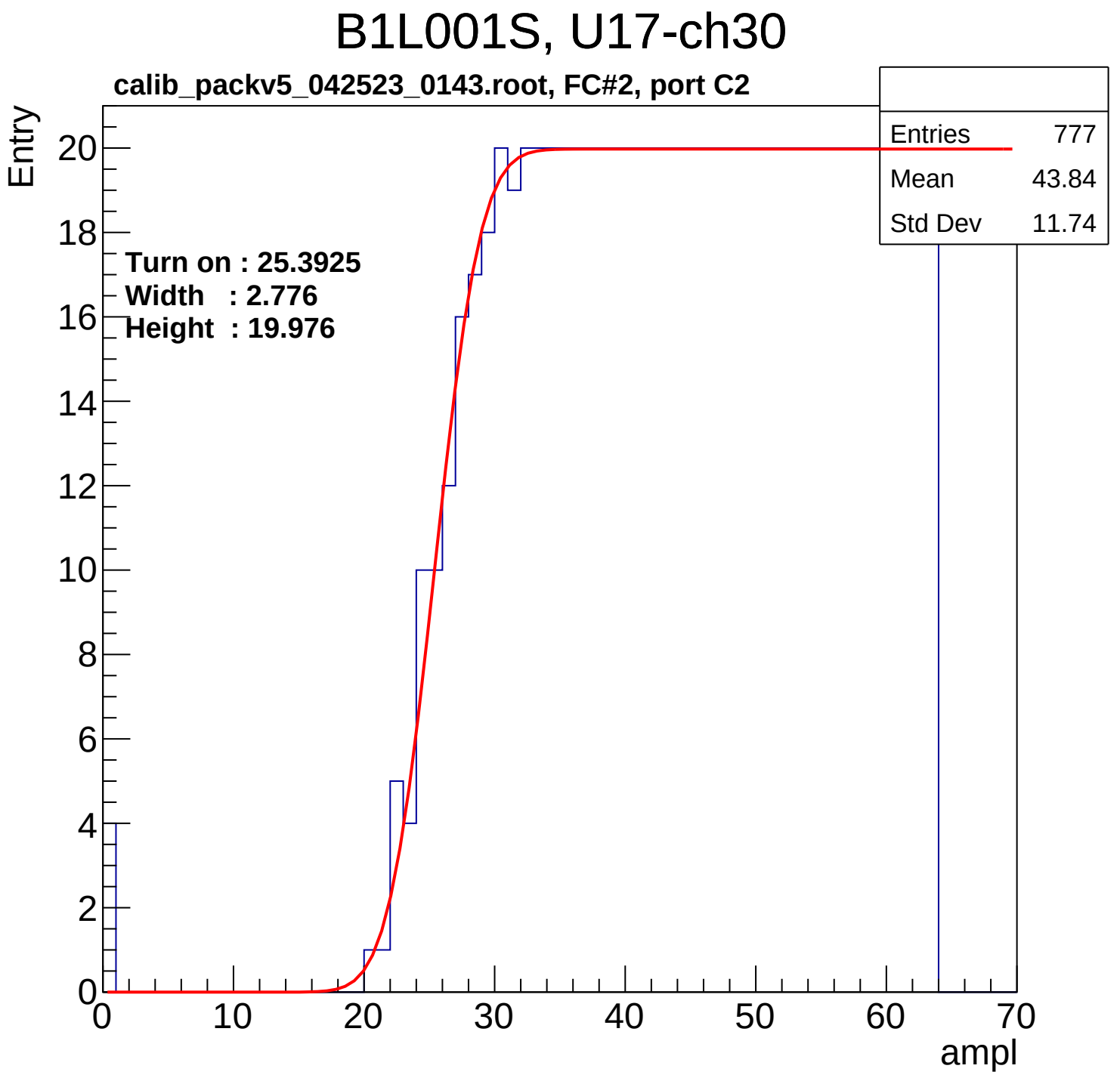
B1L001S, U17-ch30
calib_packv5_042523_0143.root, FC#2, port C2
Entries 777
Mean 43.84
Std Dev 11.74
Turn on : 25.3925
Width : 2.776
Height : 19.976
Entry
ampl
0
2
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6
8
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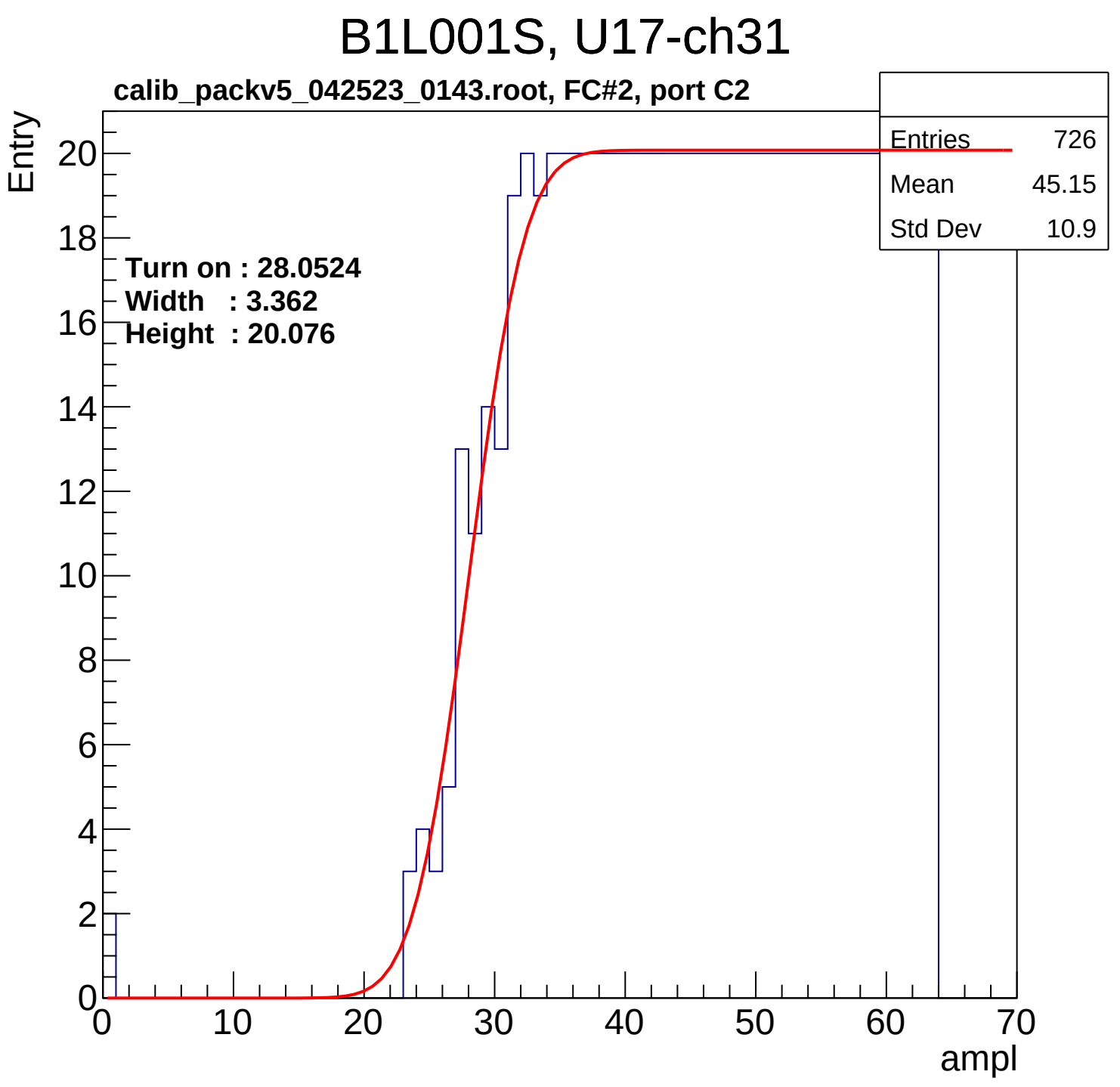
B1L001S, U17-ch31
calib_packv5_042523_0143.root, FC#2, port C2
Entries 726
Mean 45.15
Std Dev 10.9
Turn on : 28.0524
Width : 3.362
Height : 20.076
Entry
ampl
0
2
4
6
8
10
12
14
16
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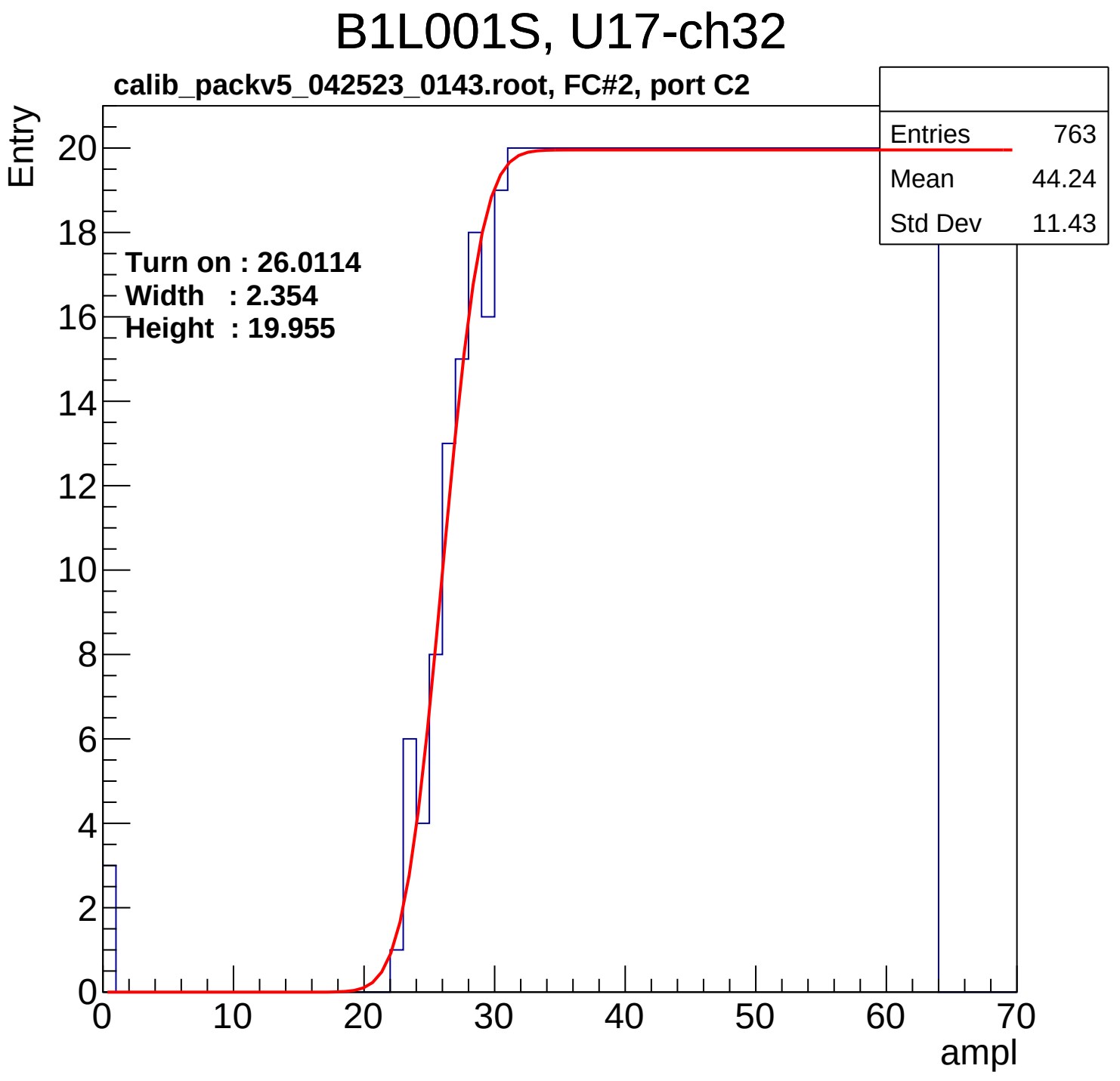
B1L001S, U17-ch32
calib_packv5_042523_0143.root, FC#2, port C2
Entries 763
Mean 44.24
Std Dev 11.43
Turn on : 26.0114
Width : 2.354
Height : 19.955
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
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20
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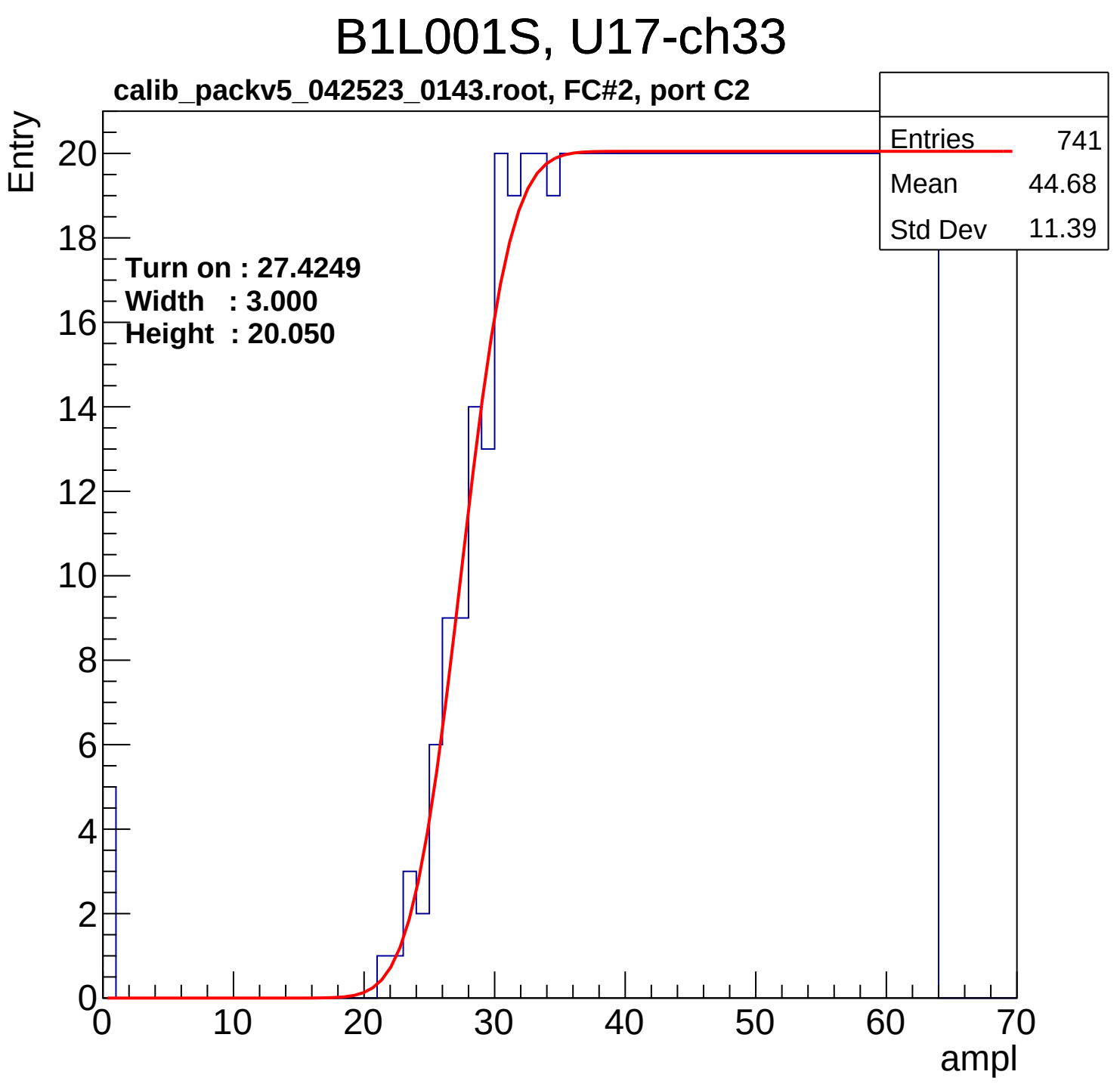
B1L001S, U17-ch33
calib_packv5_042523_0143.root, FC#2, port C2
Entries 741
Mean 44.68
Std Dev 11.39
Turn on : 27.4249
Width : 3.000
Height : 20.050
Entry
ampl
0
2
4
6
8
10
12
14
16
18
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0
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40
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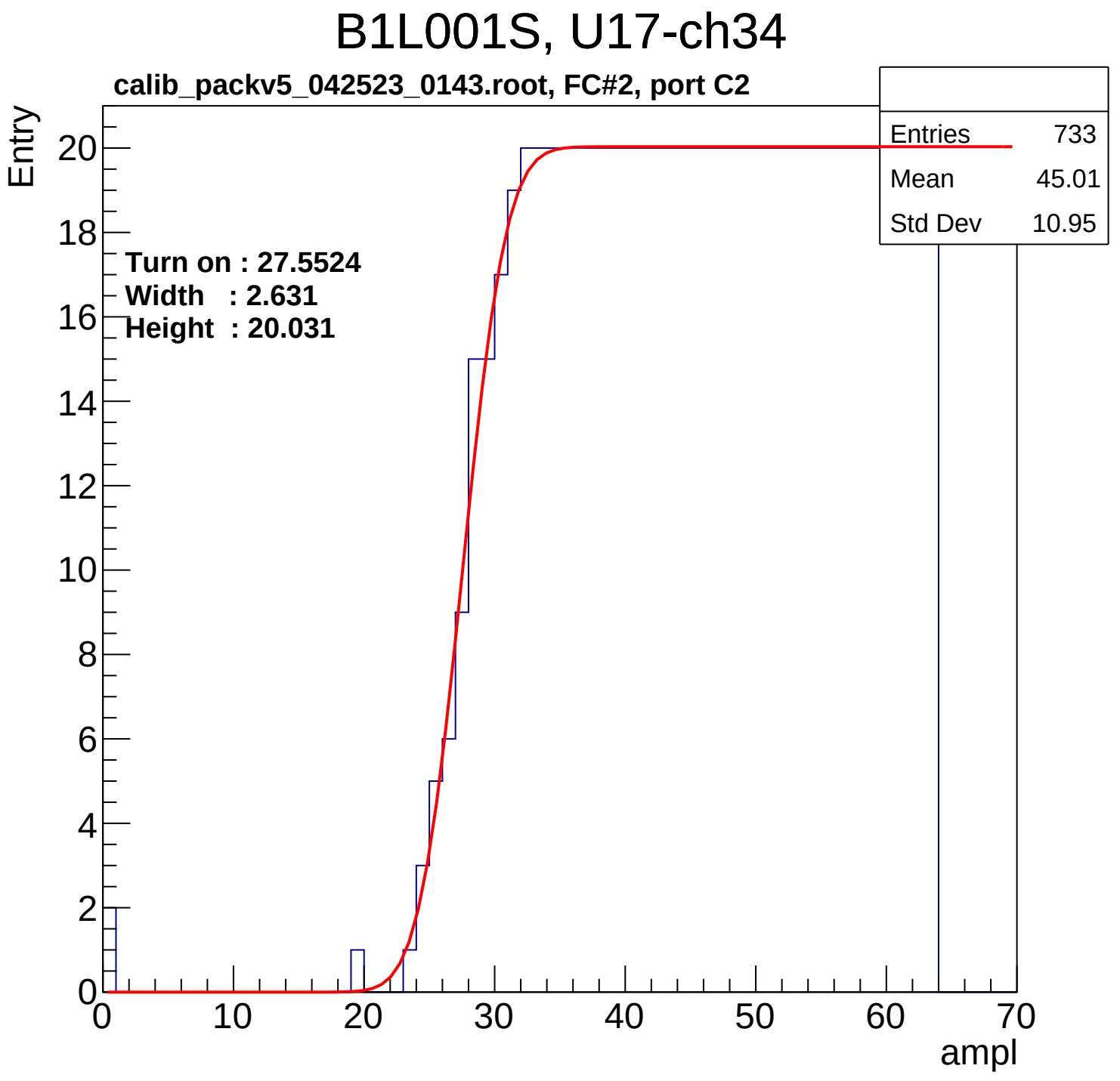
B1L001S, U17-ch34
calib_packv5_042523_0143.root, FC#2, port C2
Entries 733
Mean 45.01
Std Dev 10.95
Turn on : 27.5524
Width : 2.631
Height : 20.031
Entry
ampl
0
2
4
6
8
10
12
14
16
18
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0
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60
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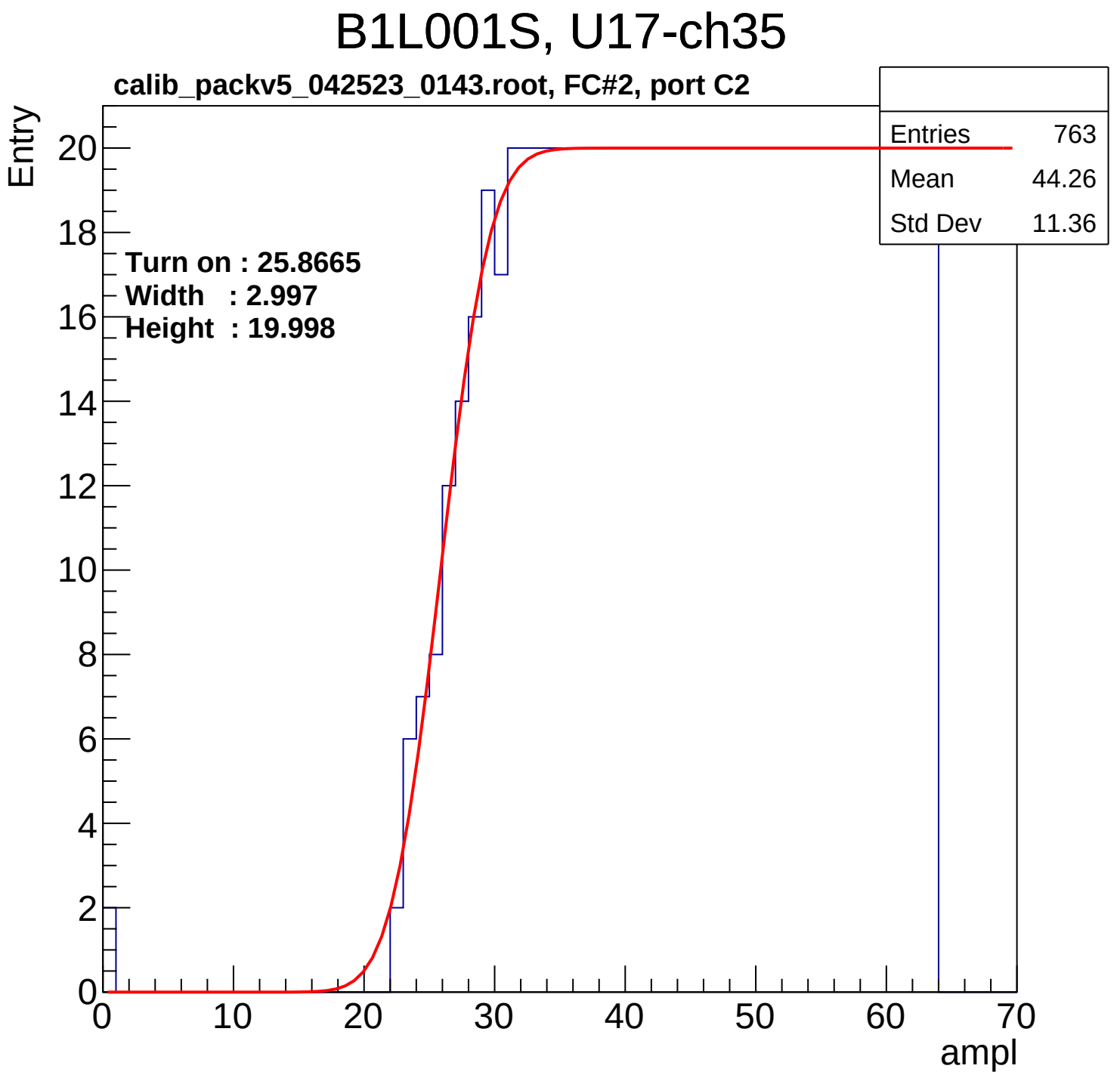
B1L001S, U17-ch35
calib_packv5_042523_0143.root, FC#2, port C2
Entries 763
Mean 44.26
Std Dev 11.36
Turn on : 25.8665
Width : 2.997
Height : 19.998
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
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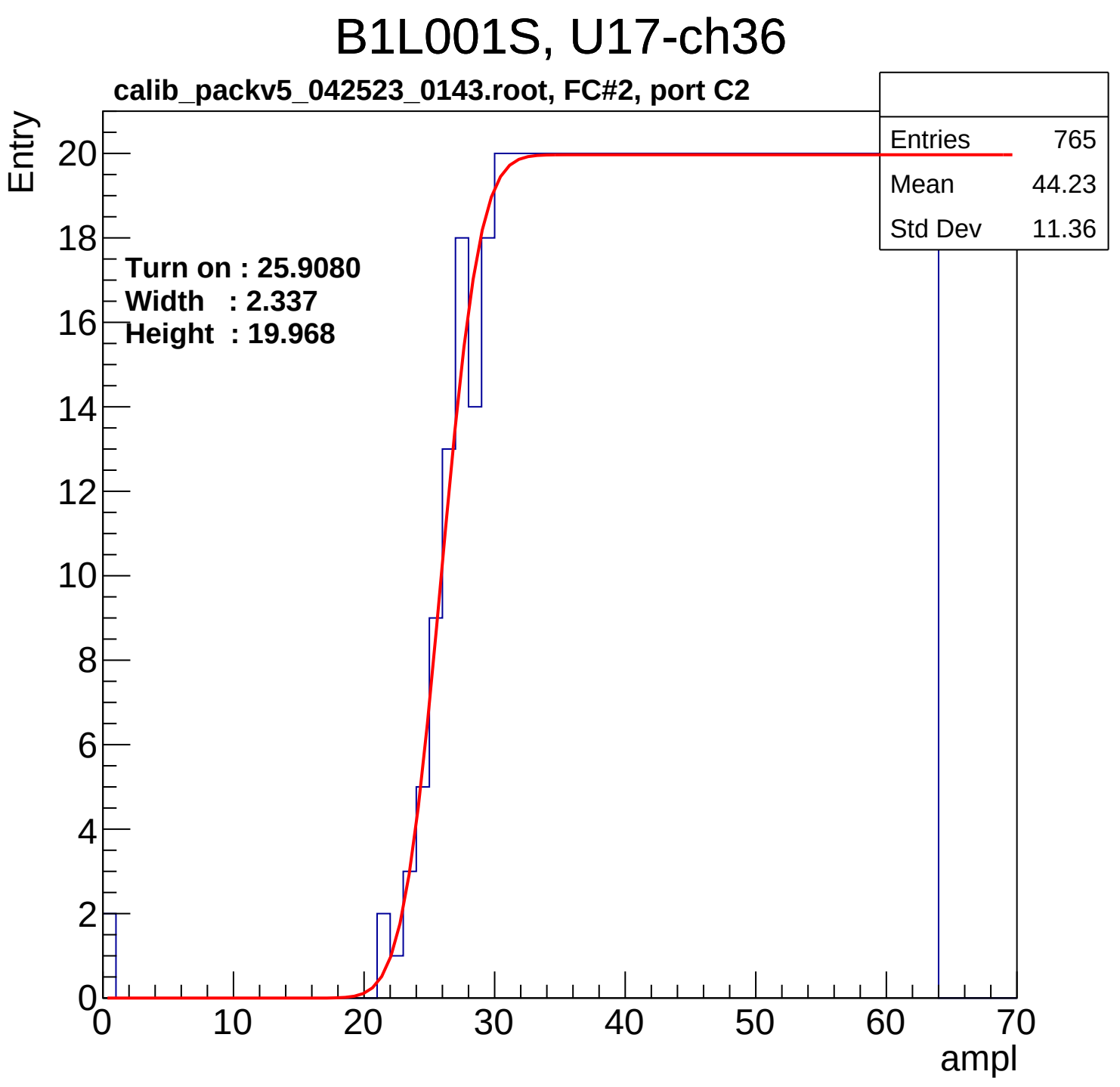
B1L001S, U17-ch36
calib_packv5_042523_0143.root, FC#2, port C2
Entries 765
Mean 44.23
Std Dev 11.36
Turn on : 25.9080
Width : 2.337
Height : 19.968
Entry
ampl
0
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4
6
8
10
12
14
16
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0
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20
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60
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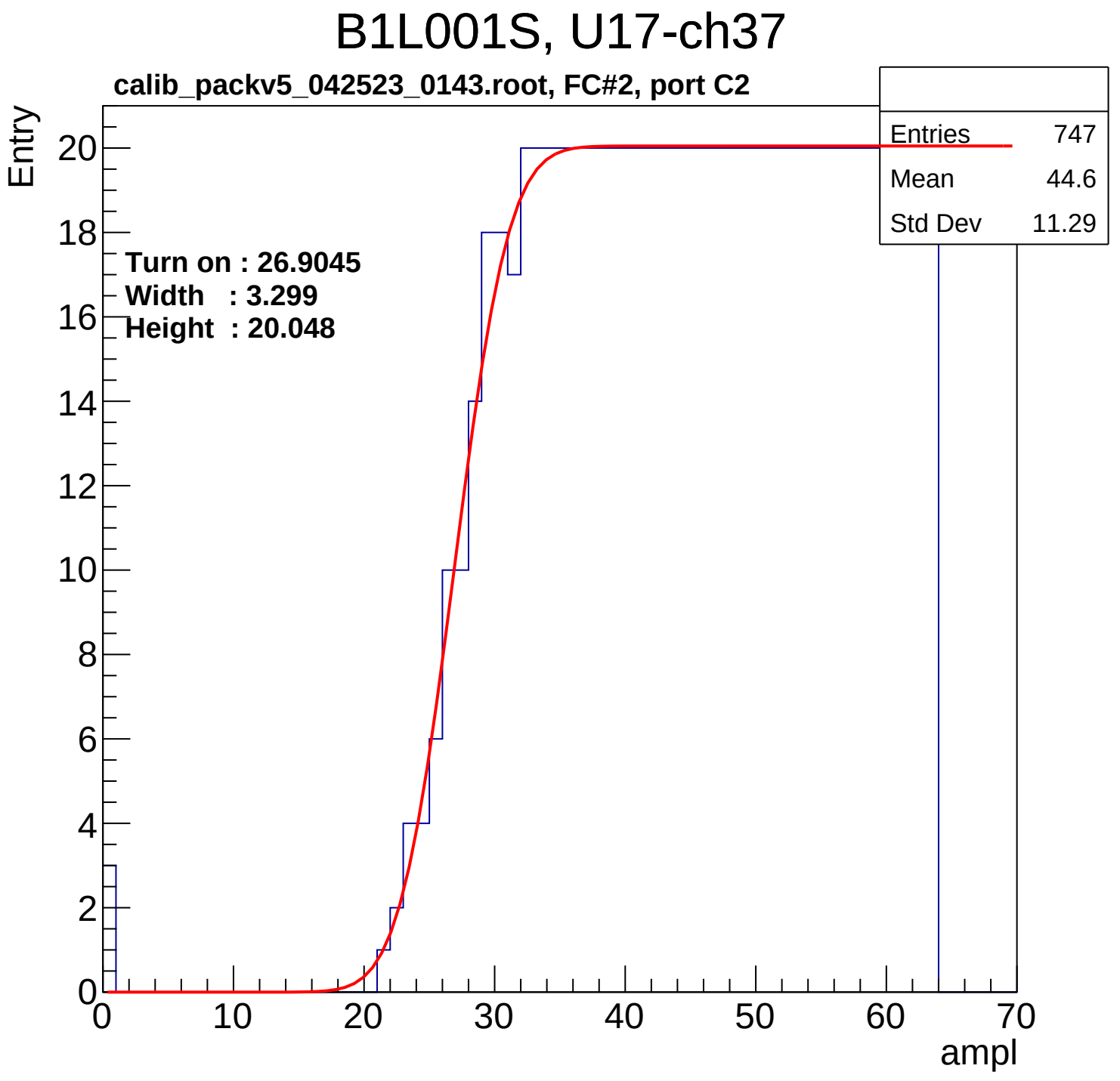
B1L001S, U17-ch37
calib_packv5_042523_0143.root, FC#2, port C2
Entries 747
Mean 44.6
Std Dev 11.29
Turn on : 26.9045
Width : 3.299
Height : 20.048
Entry
ampl
0
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6
8
10
12
14
16
18
20
0
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60
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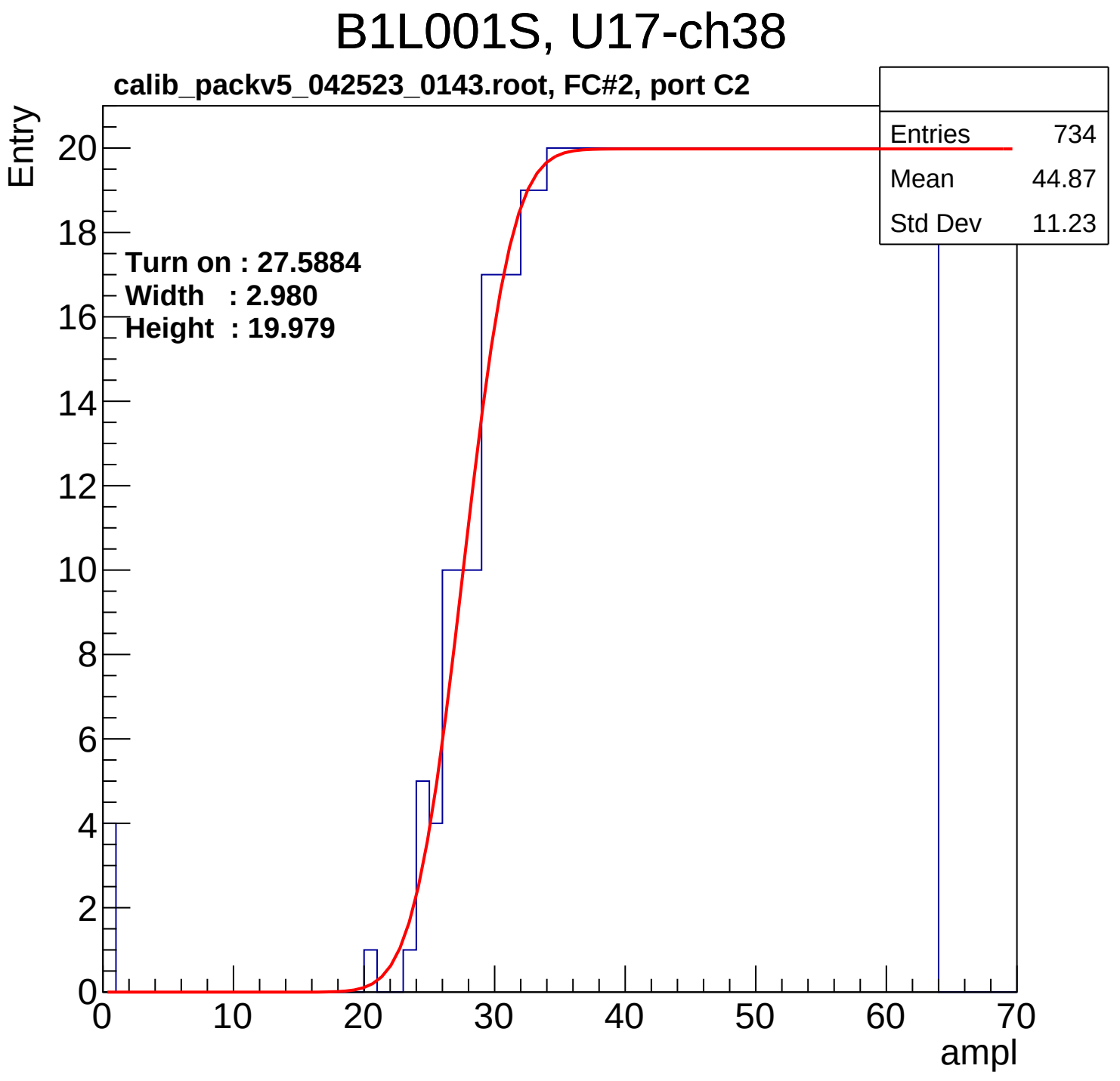
B1L001S, U17-ch38
calib_packv5_042523_0143.root, FC#2, port C2
Entries 734
Mean 44.87
Std Dev 11.23
Turn on : 27.5884
Width : 2.980
Height : 19.979
Entry
ampl
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6
8
10
12
14
16
18
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0
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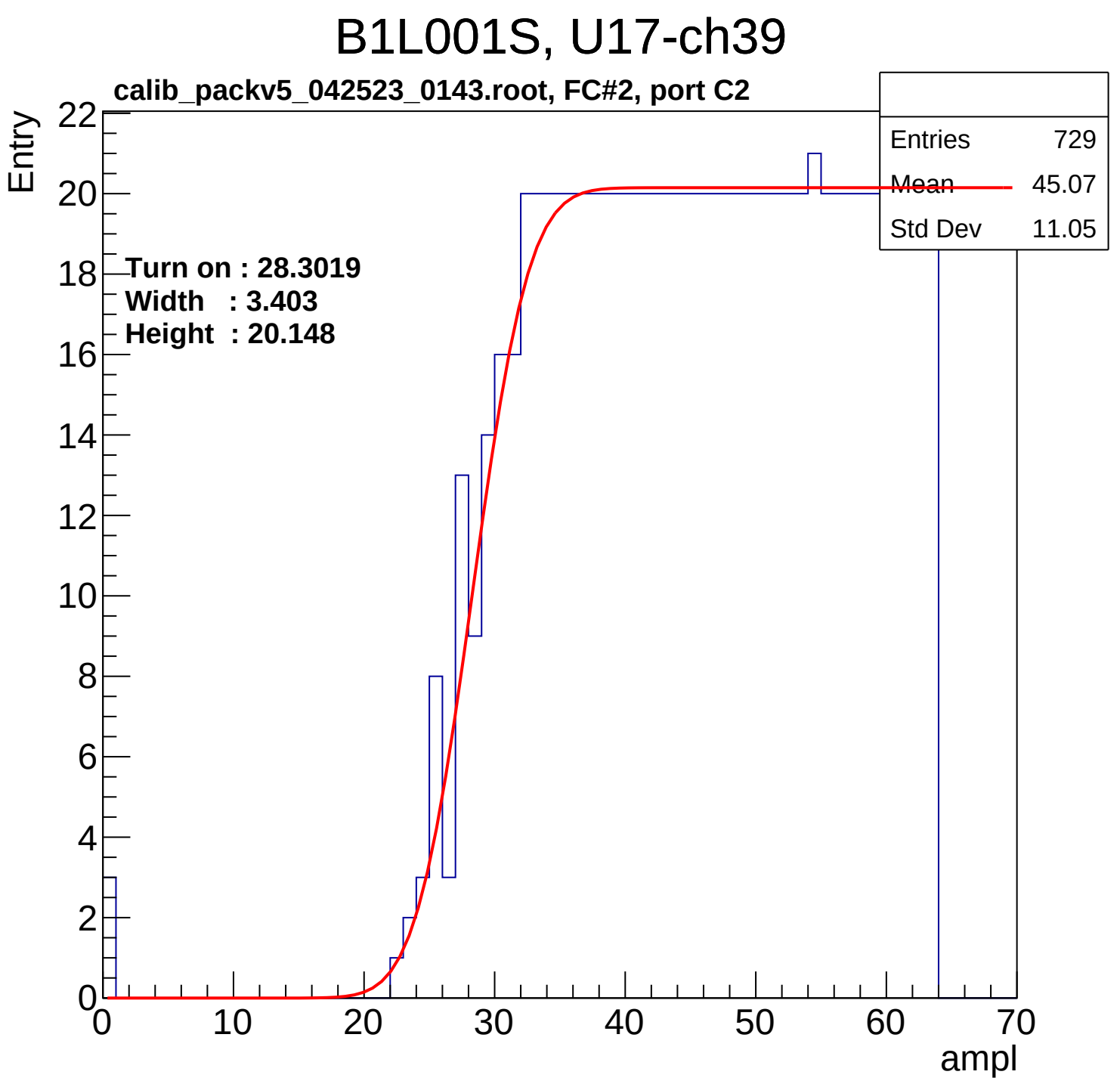
B1L001S, U17-ch39
calib_packv5_042523_0143.root, FC#2, port C2
Entries 729
Mean 45.07
Std Dev 11.05
Turn on : 28.3019
Width : 3.403
Height : 20.148
Entry
ampl
0
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6
8
10
12
14
16
18
20
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0
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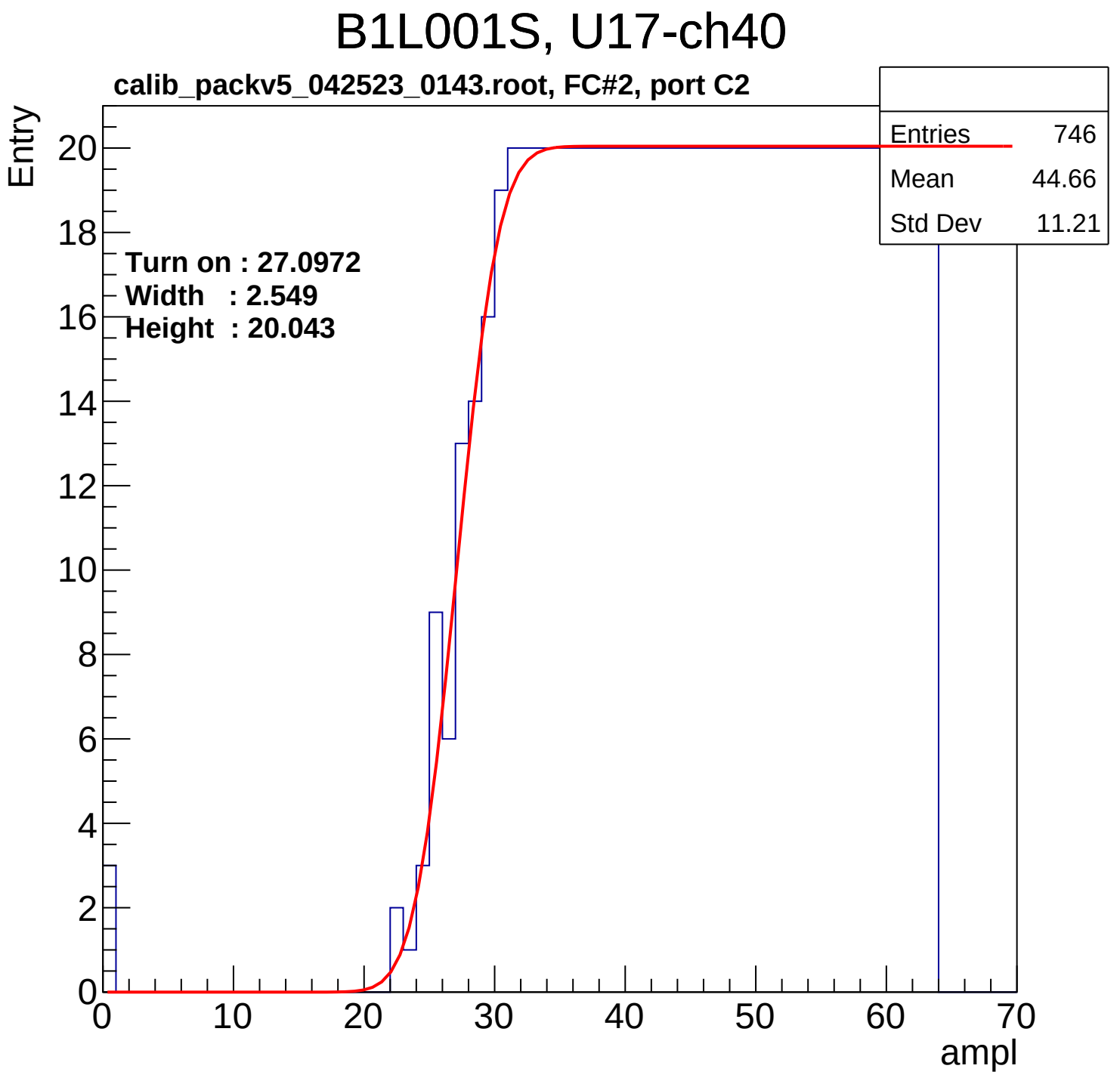
B1L001S, U17-ch40
calib_packv5_042523_0143.root, FC#2, port C2
Entries 746
Mean 44.66
Std Dev 11.21
Turn on : 27.0972
Width : 2.549
Height : 20.043
Entry
ampl
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6
8
10
12
14
16
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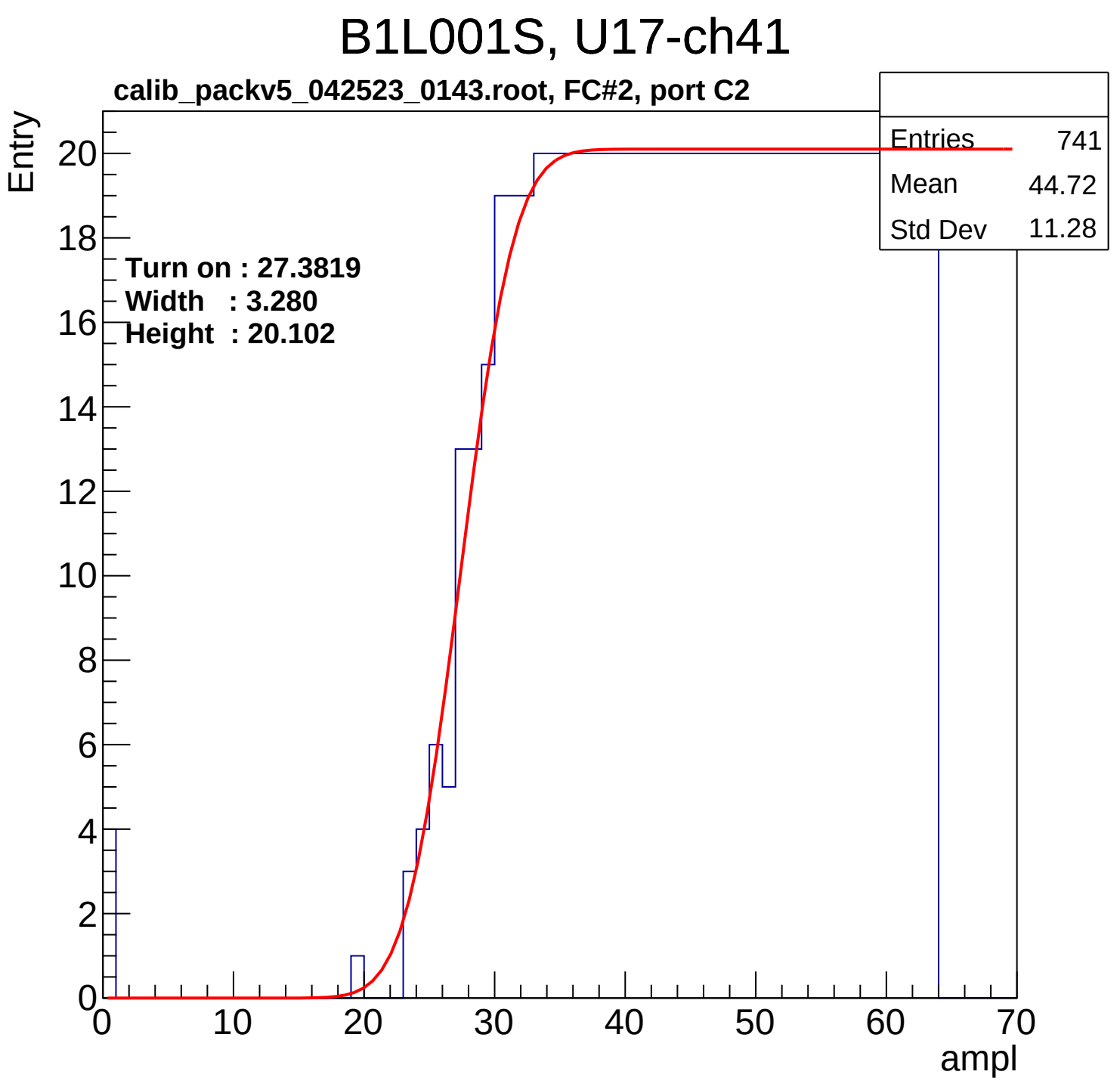
B1L001S, U17-ch41
calib_packv5_042523_0143.root, FC#2, port C2
Entries 741
Mean 44.72
Std Dev 11.28
Turn on : 27.3819
Width : 3.280
Height : 20.102
Entry
ampl
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6
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10
12
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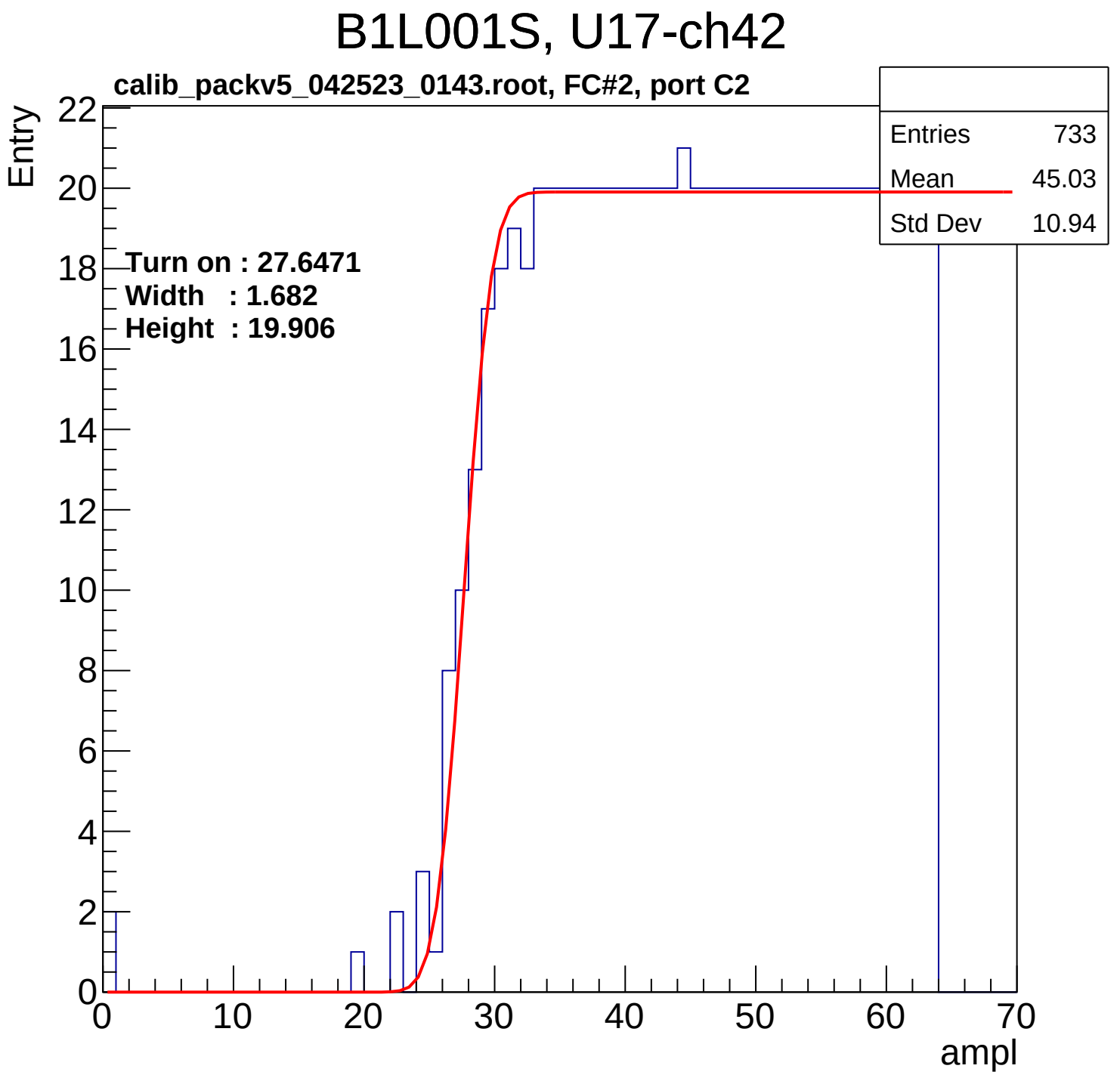
B1L001S, U17-ch42
calib_packv5_042523_0143.root, FC#2, port C2
Entries 733
Mean 45.03
Std Dev 10.94
Turn on : 27.6471
Width : 1.682
Height : 19.906
Entry
ampl
0
2
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6
8
10
12
14
16
18
20
22
0
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20
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60
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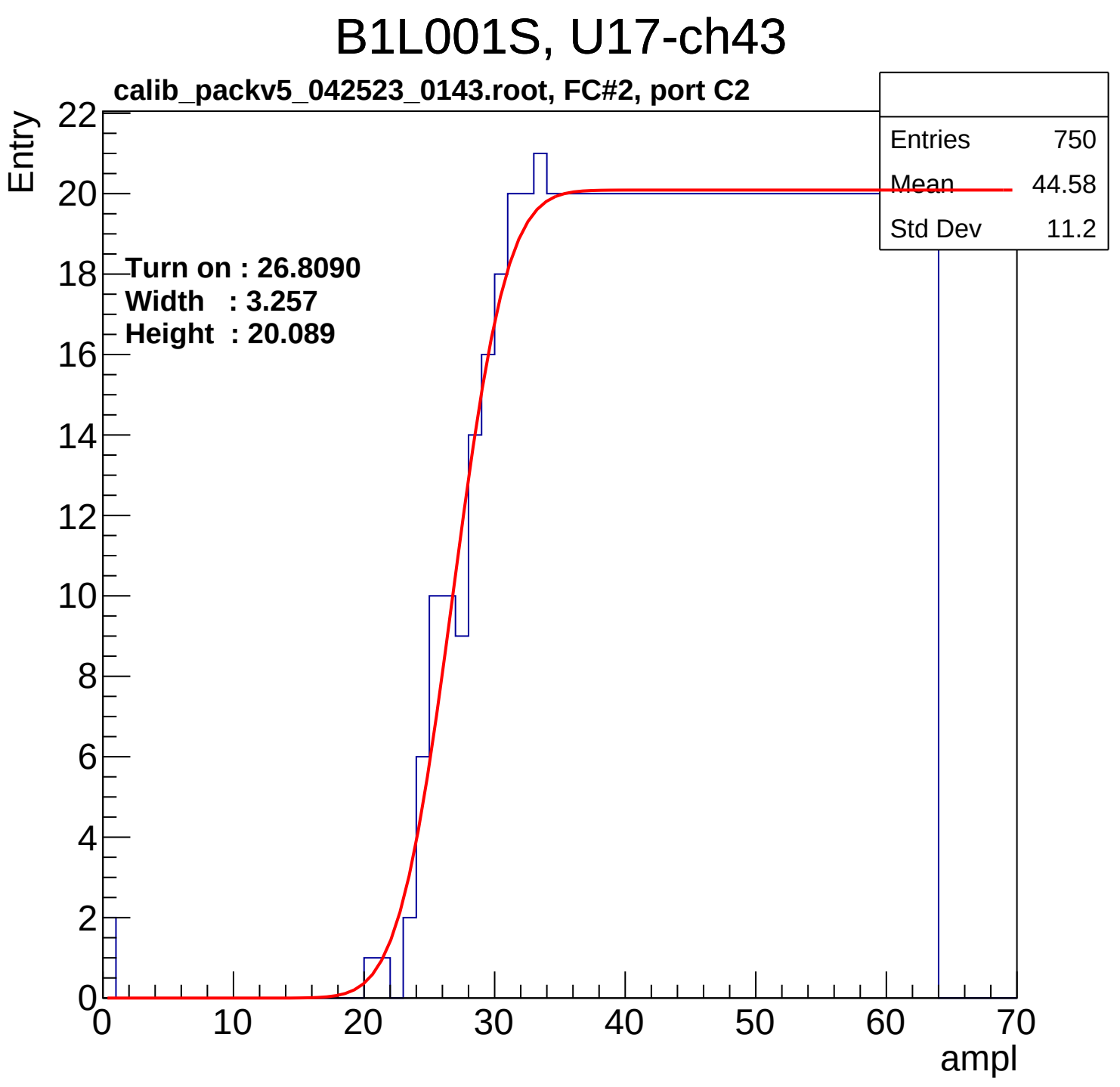
B1L001S, U17-ch43
calib_packv5_042523_0143.root, FC#2, port C2
Entries 750
Mean 44.58
Std Dev 11.2
Turn on : 26.8090
Width : 3.257
Height : 20.089
Entry
ampl
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8
10
12
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16
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20
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0
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20
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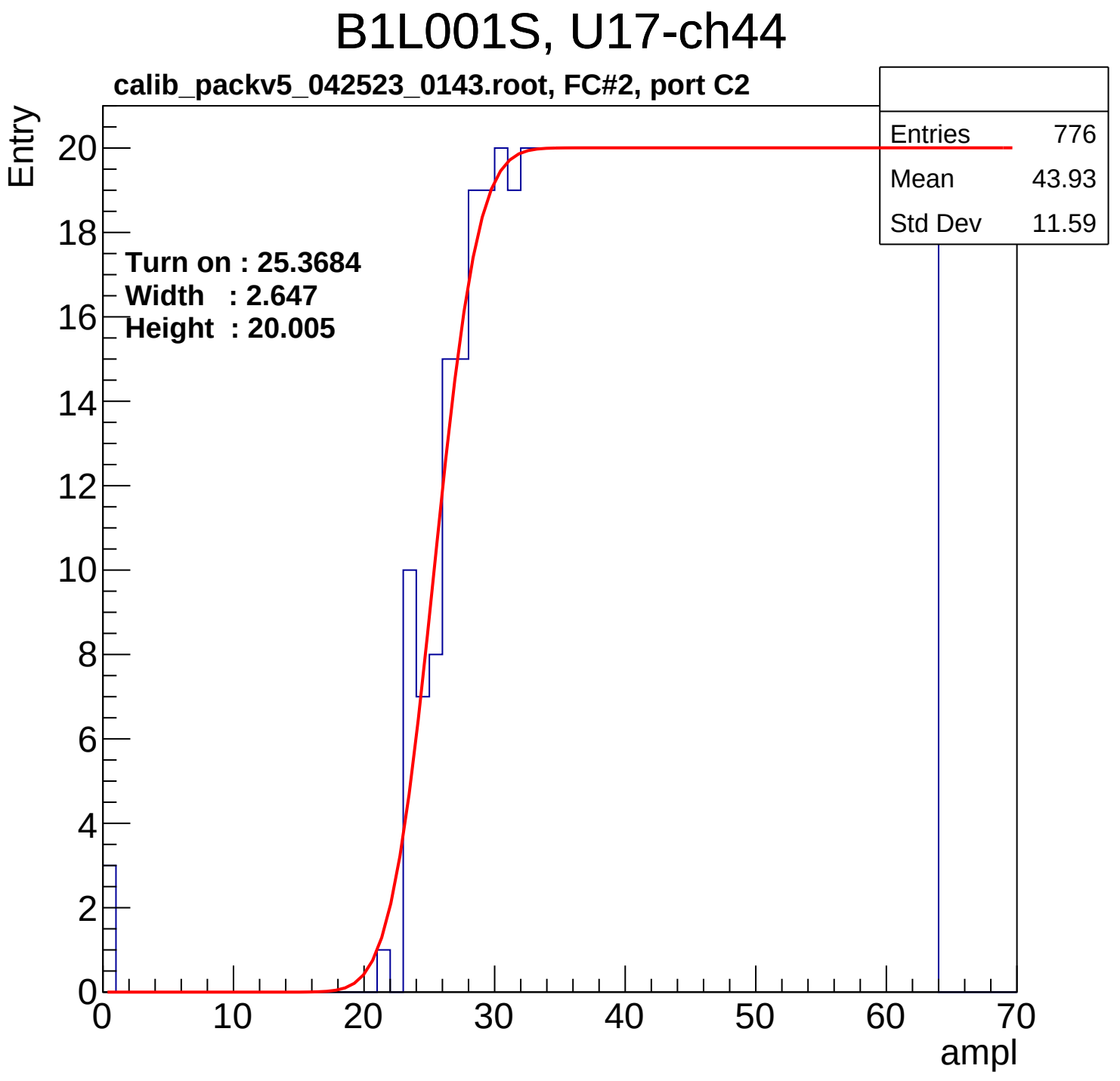
B1L001S, U17-ch44
calib_packv5_042523_0143.root, FC#2, port C2
Entries 776
Mean 43.93
Std Dev 11.59
Turn on : 25.3684
Width : 2.647
Height : 20.005
Entry
ampl
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6
8
10
12
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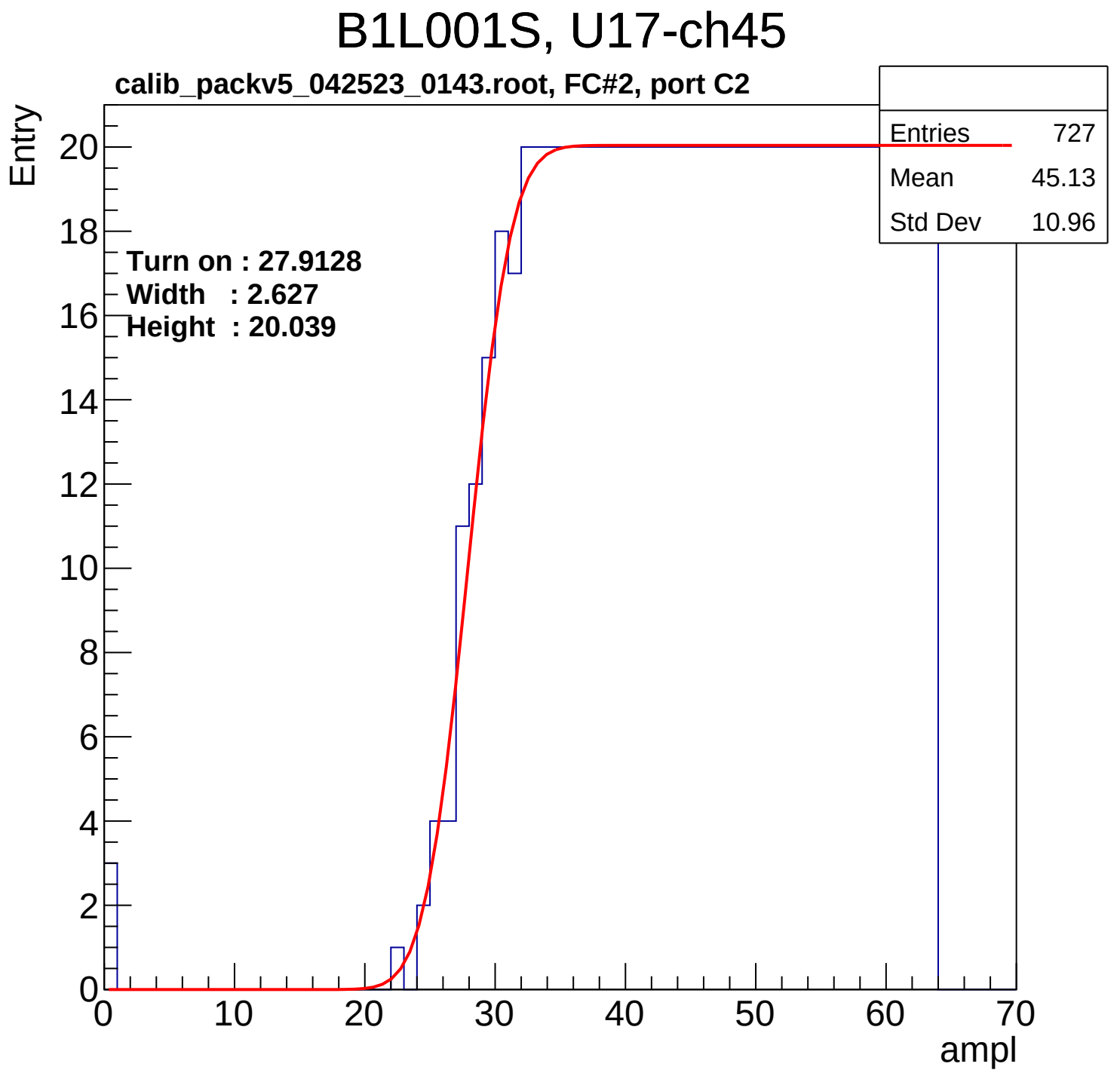
B1L001S, U17-ch45
calib_packv5_042523_0143.root, FC#2, port C2
Entries 727
Mean 45.13
Std Dev 10.96
Turn on : 27.9128
Width : 2.627
Height : 20.039
Entry
ampl
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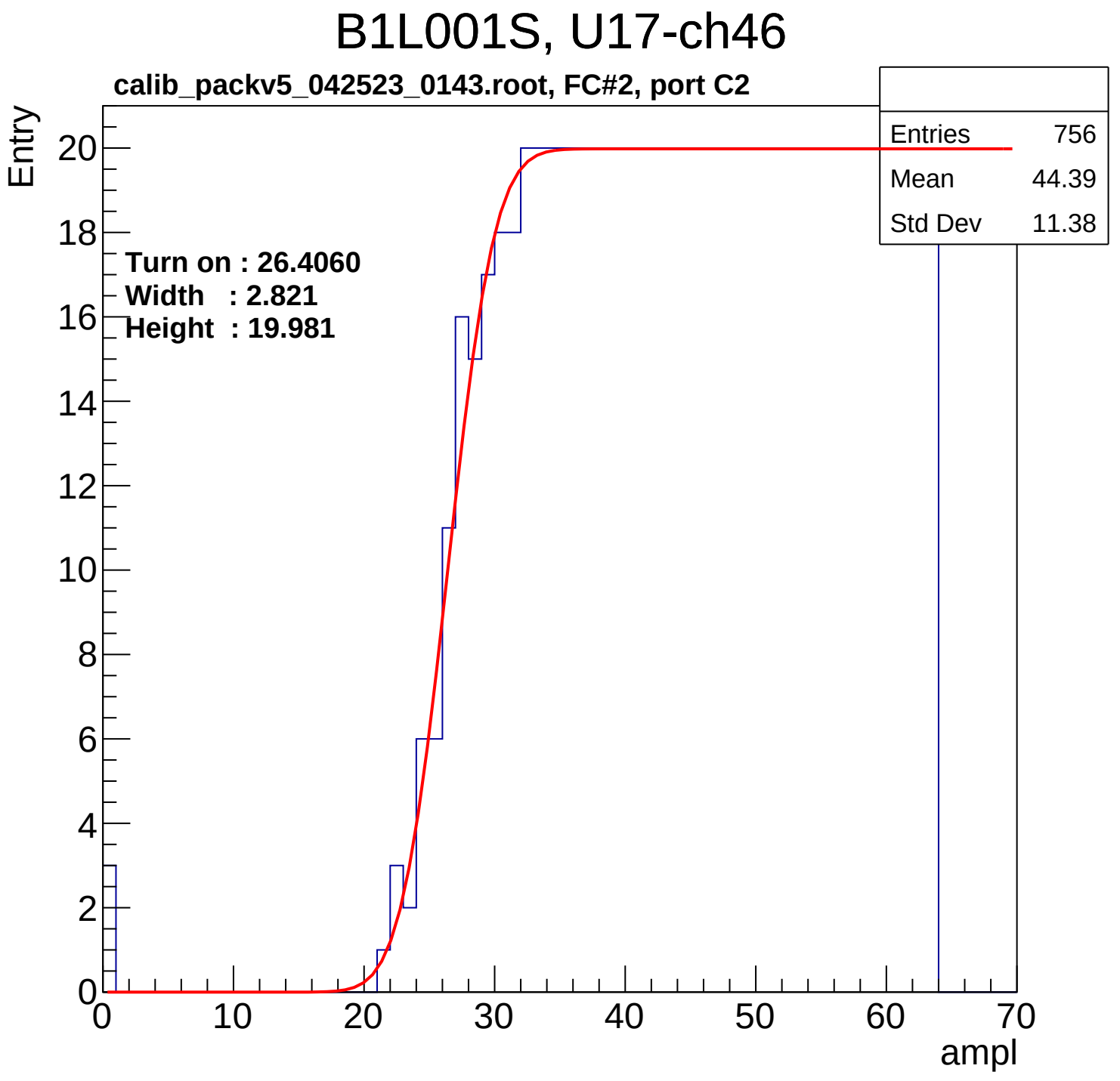
B1L001S, U17-ch46
calib_packv5_042523_0143.root, FC#2, port C2
Entries 756
Mean 44.39
Std Dev 11.38
Turn on : 26.4060
Width : 2.821
Height : 19.981
Entry
ampl
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6
8
10
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14
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60
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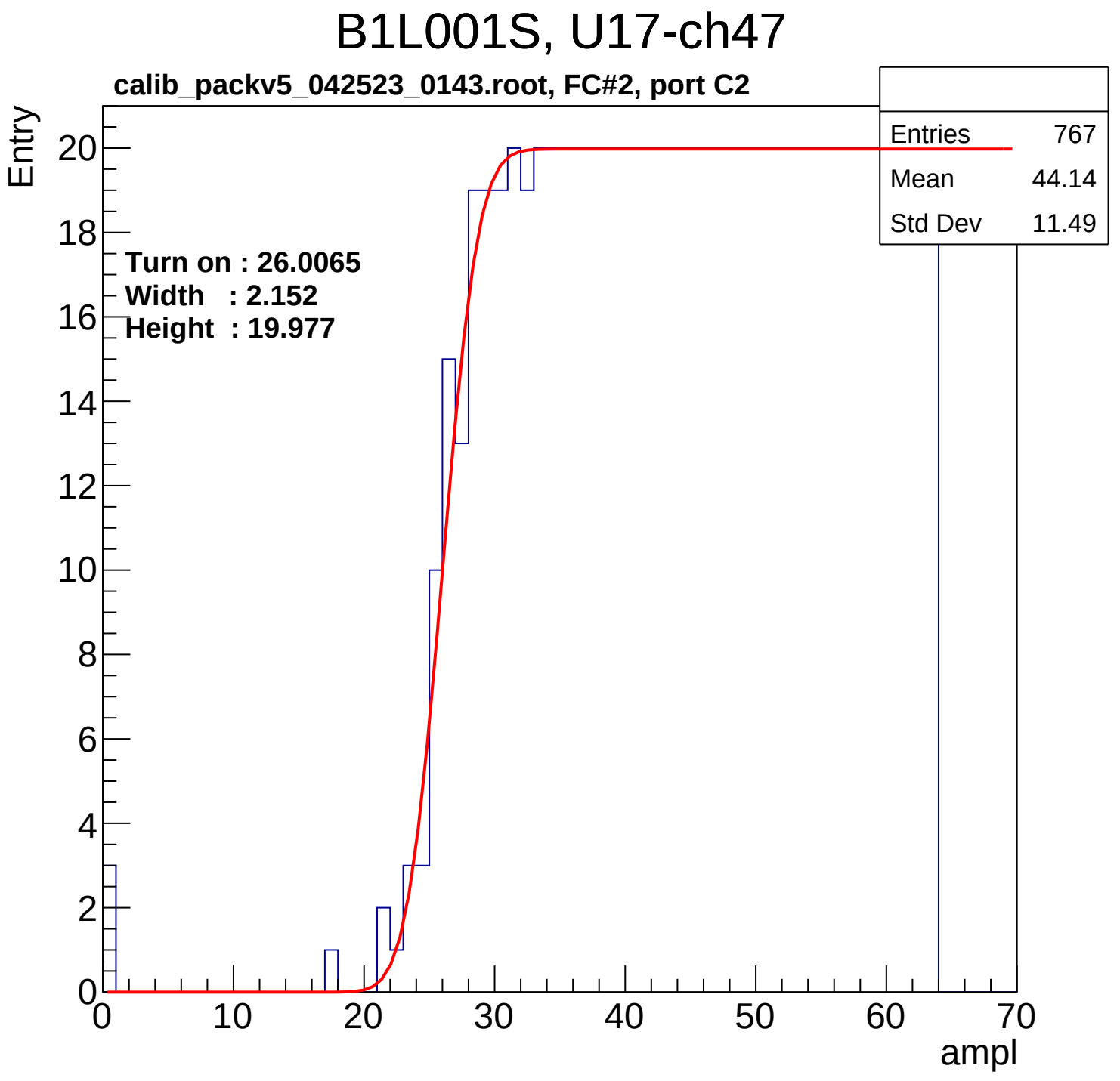
B1L001S, U17-ch47
calib_packv5_042523_0143.root, FC#2, port C2
Entries 767
Mean 44.14
Std Dev 11.49
Turn on : 26.0065
Width : 2.152
Height : 19.977
Entry
ampl
0
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6
8
10
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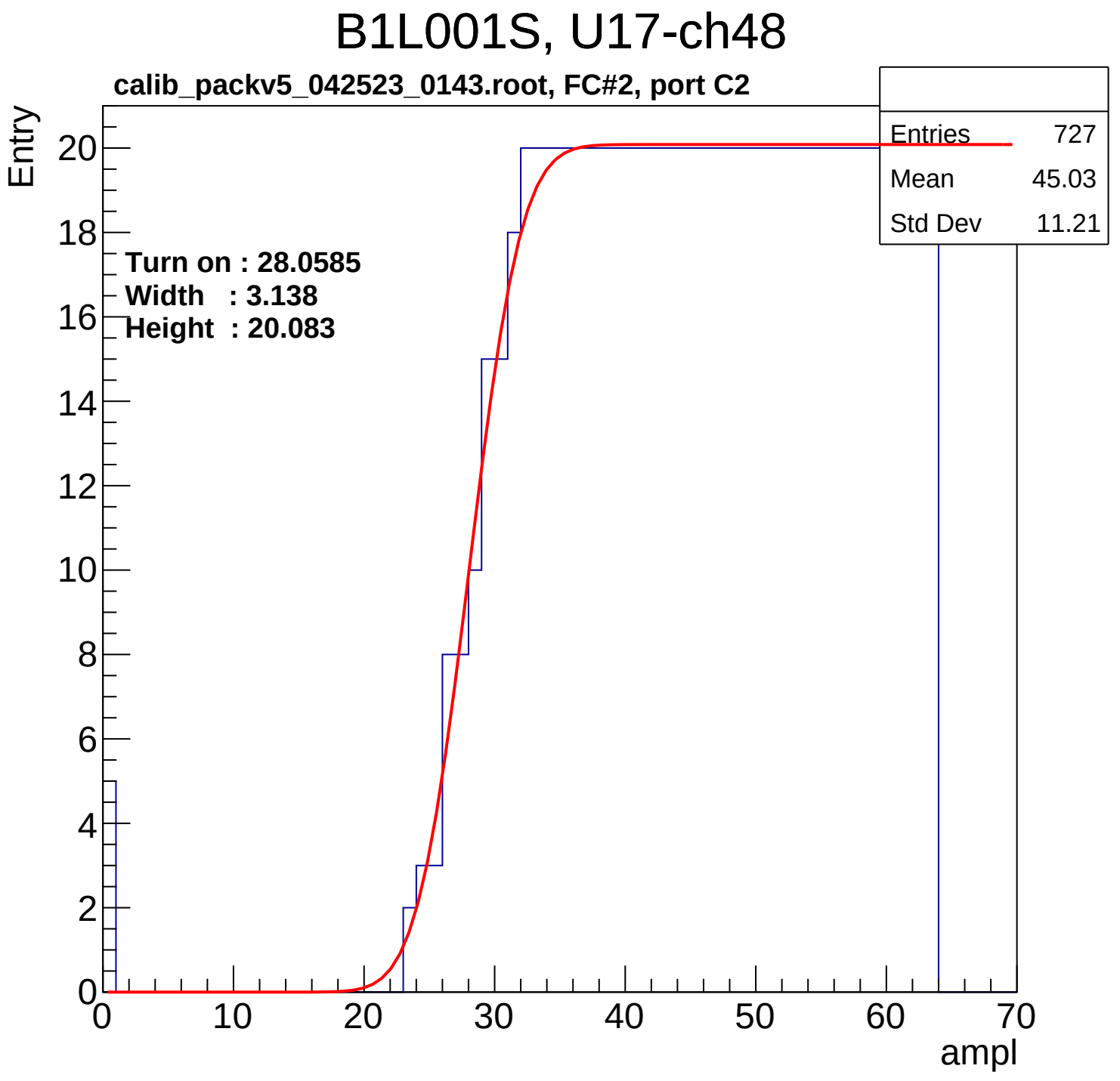
B1L001S, U17-ch48
calib_packv5_042523_0143.root, FC#2, port C2
Entries 727
Mean 45.03
Std Dev 11.21
Turn on : 28.0585
Width : 3.138
Height : 20.083
Entry
ampl
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6
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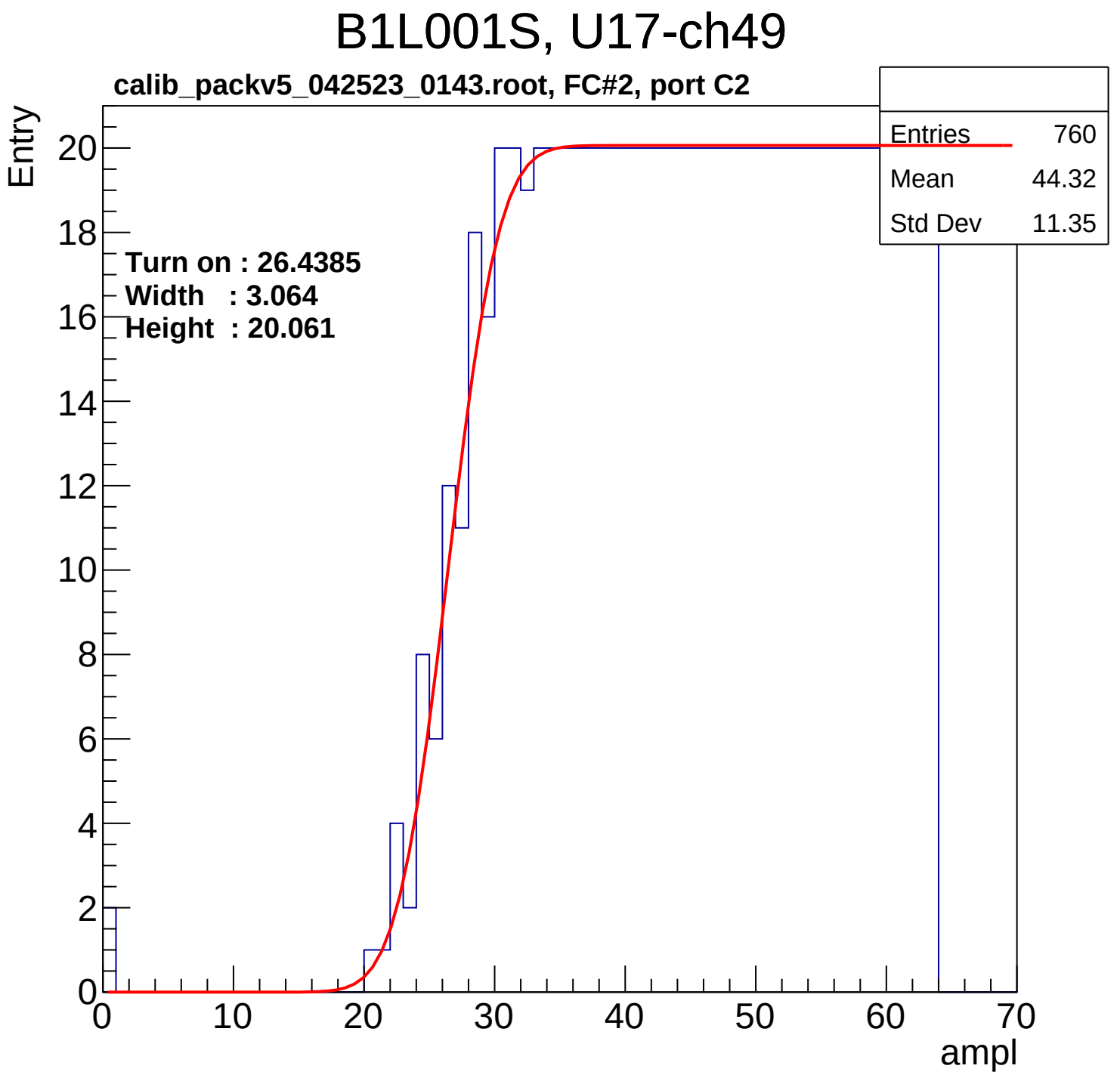
B1L001S, U17-ch49
calib_packv5_042523_0143.root, FC#2, port C2
Entries 760
Mean 44.32
Std Dev 11.35
Turn on : 26.4385
Width : 3.064
Height : 20.061
Entry
ampl
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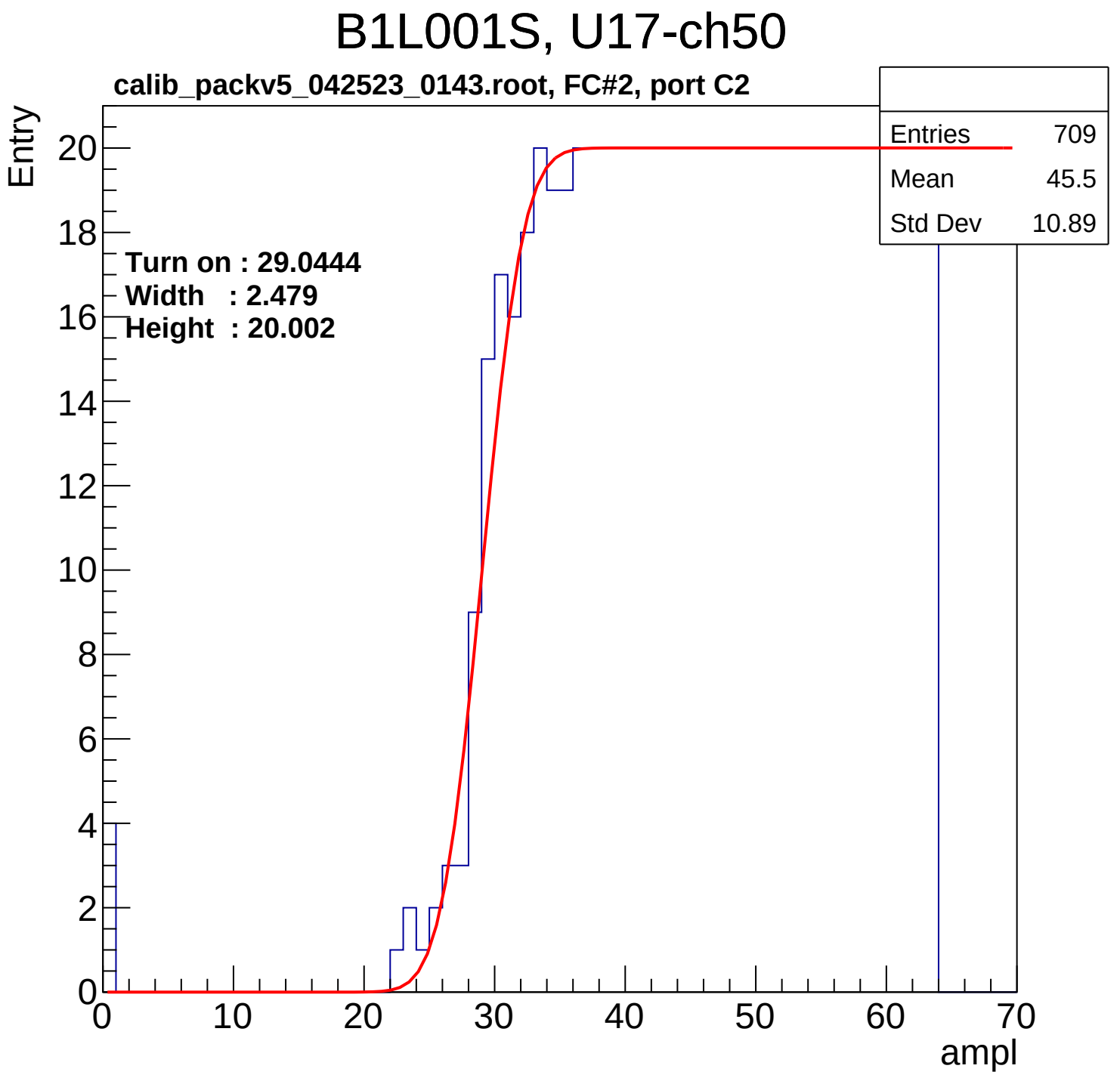
B1L001S, U17-ch50
calib_packv5_042523_0143.root, FC#2, port C2
Entries 709
Mean 45.5
Std Dev 10.89
Turn on : 29.0444
Width : 2.479
Height : 20.002
Entry
ampl
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6
8
10
12
14
16
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60
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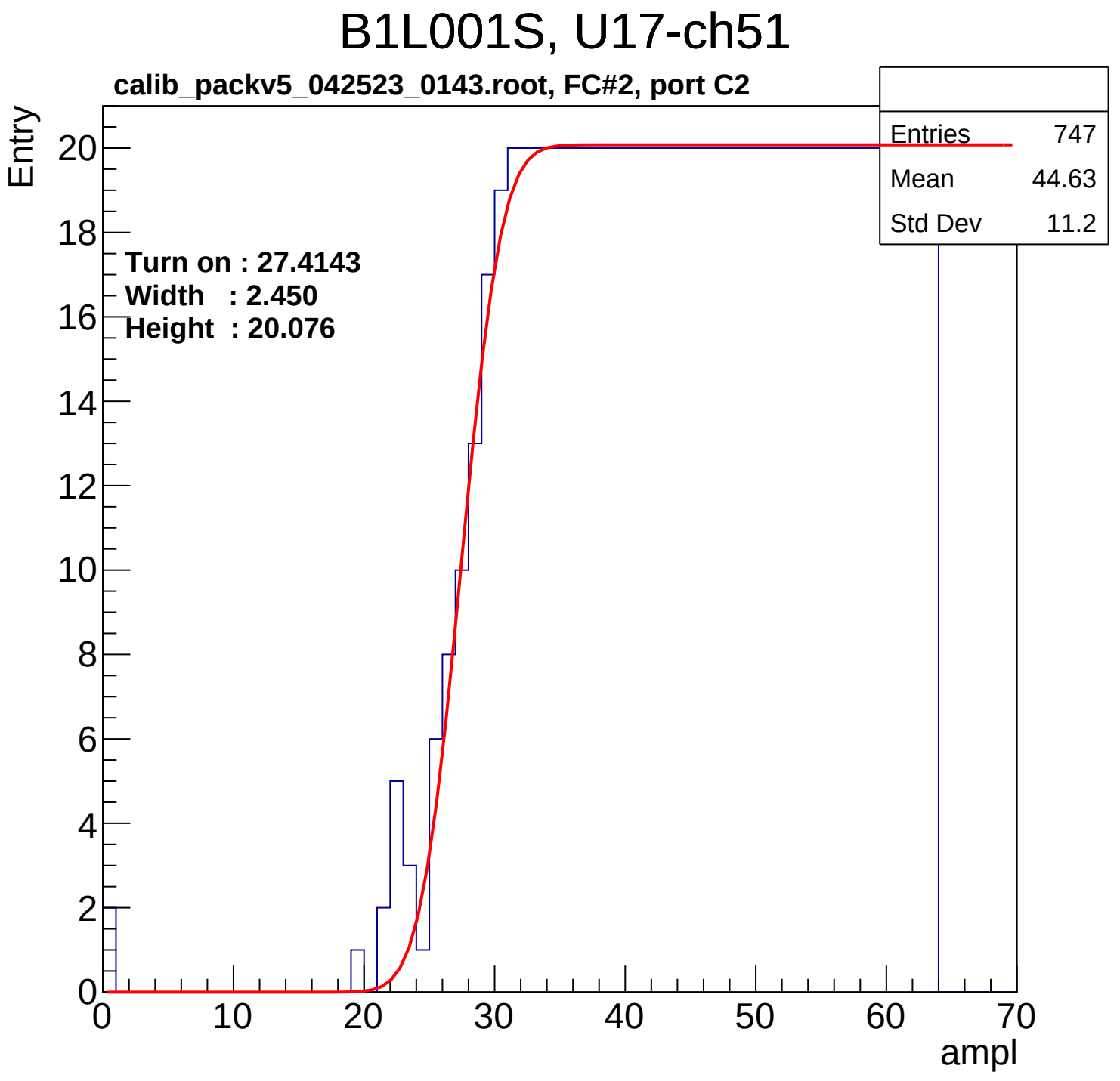
B1L001S, U17-ch51
calib_packv5_042523_0143.root, FC#2, port C2
Entries 747
Mean 44.63
Std Dev 11.2
Turn on : 27.4143
Width : 2.450
Height : 20.076
Entry
ampl
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8
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12
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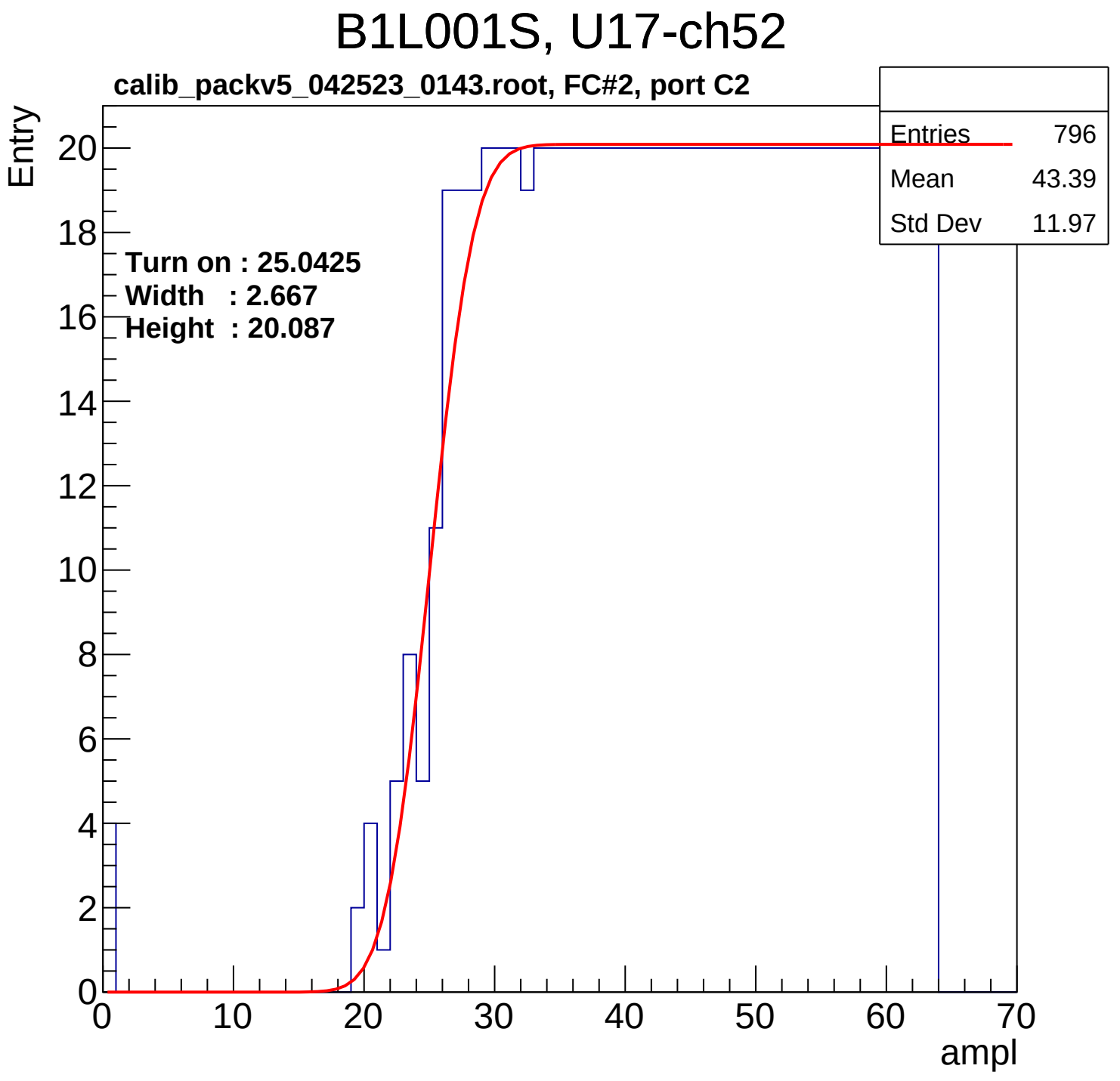
B1L001S, U17-ch52
calib_packv5_042523_0143.root, FC#2, port C2
Entries 796
Mean 43.39
Std Dev 11.97
Turn on : 25.0425
Width : 2.667
Height : 20.087
Entry
ampl
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6
8
10
12
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16
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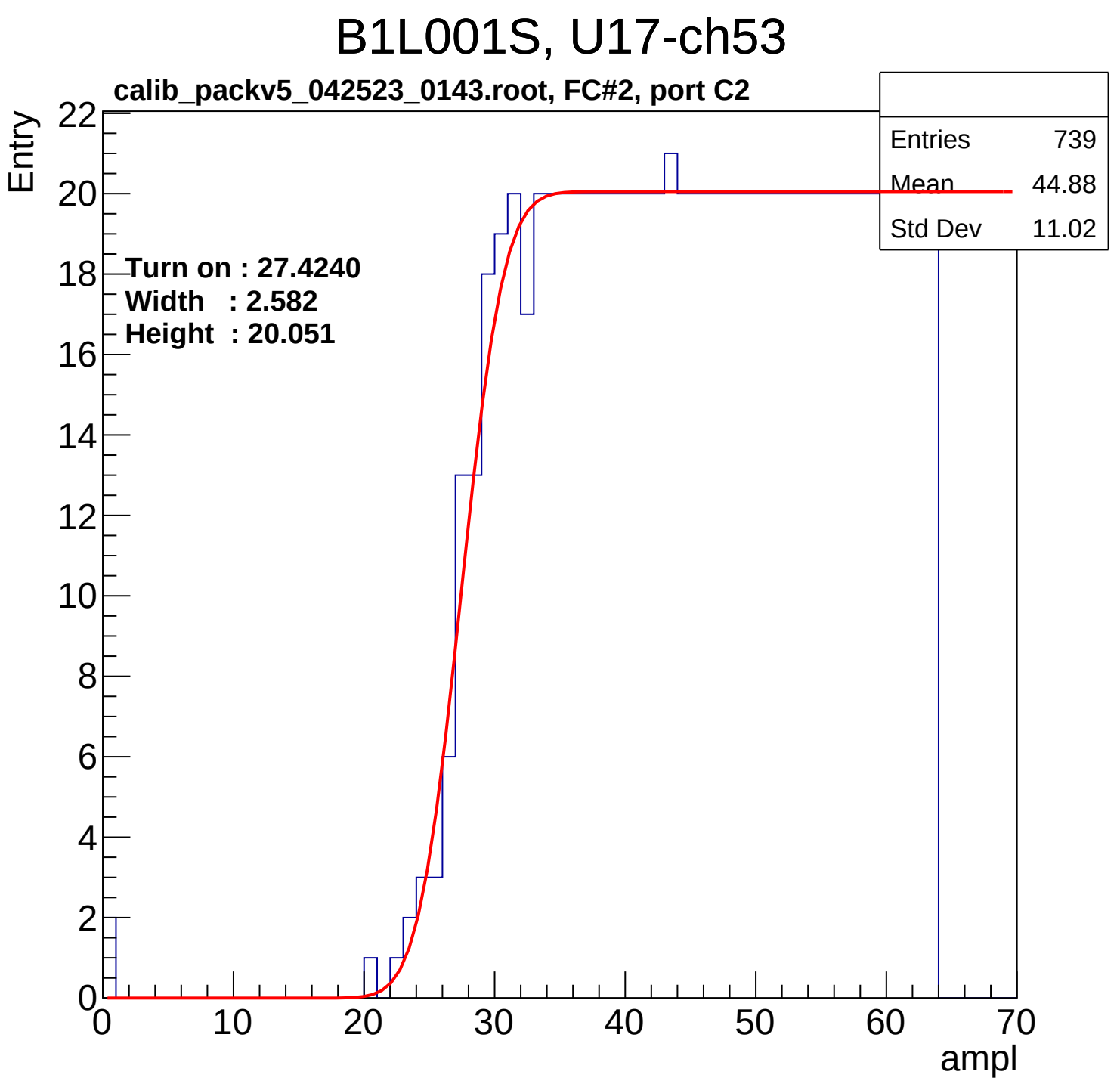
B1L001S, U17-ch53
calib_packv5_042523_0143.root, FC#2, port C2
Entries 739
Mean 44.88
Std Dev 11.02
Turn on : 27.4240
Width : 2.582
Height : 20.051
Entry
ampl
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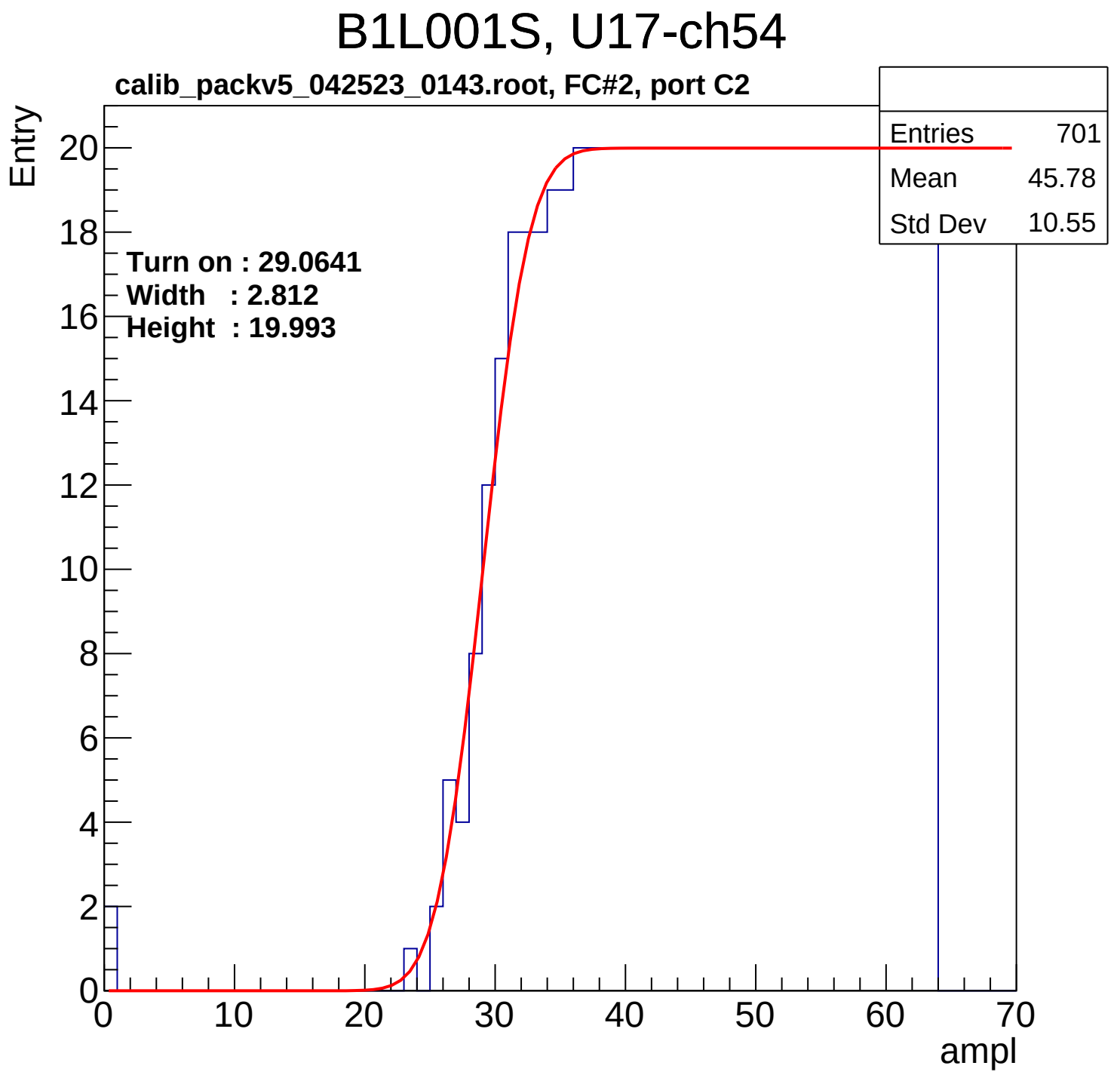
B1L001S, U17-ch54
calib_packv5_042523_0143.root, FC#2, port C2
Entries 701
Mean 45.78
Std Dev 10.55
Turn on : 29.0641
Width : 2.812
Height : 19.993
Entry
ampl
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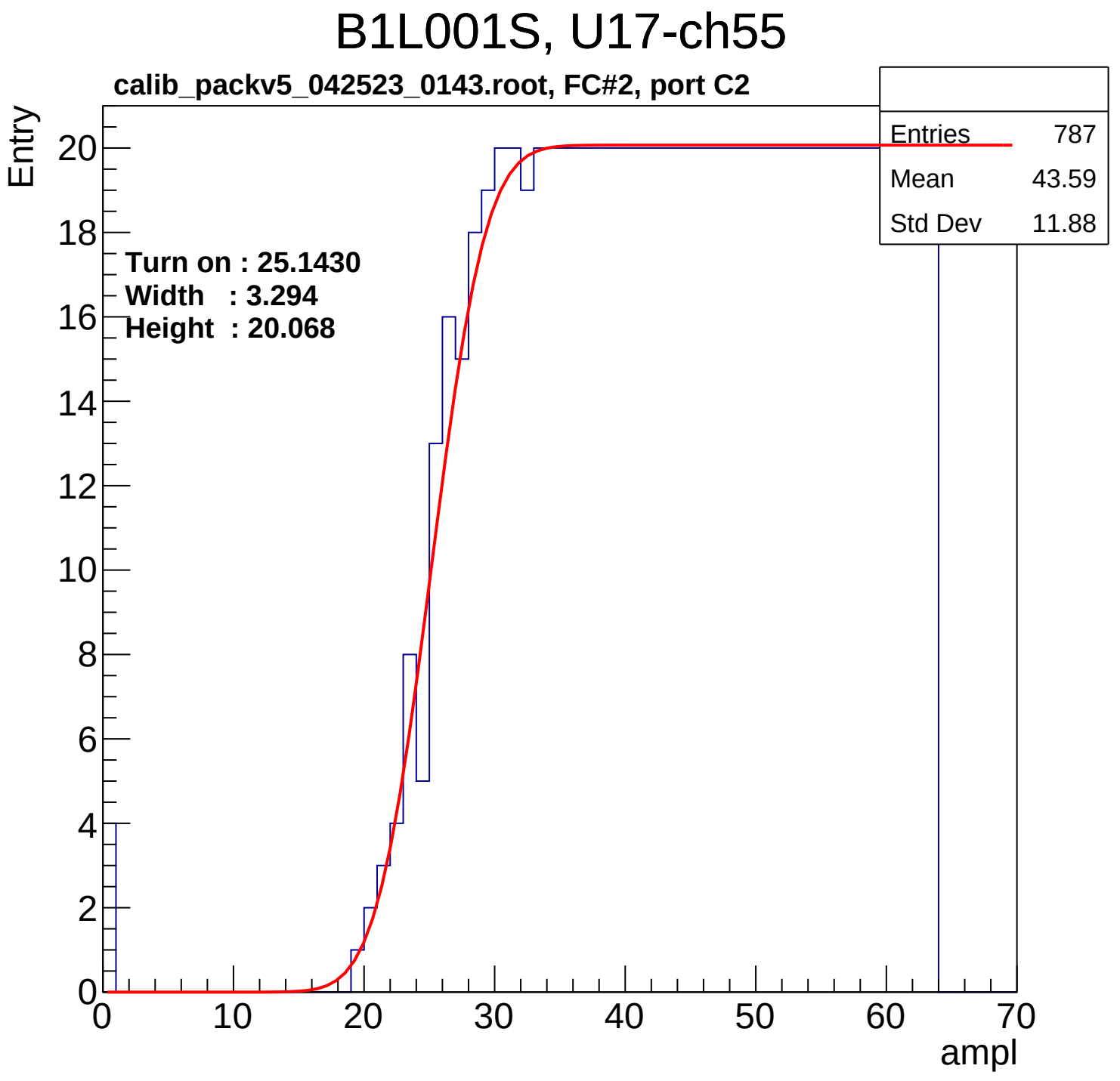
B1L001S, U17-ch55
calib_packv5_042523_0143.root, FC#2, port C2
Entries 787
Mean 43.59
Std Dev 11.88
Turn on : 25.1430
Width : 3.294
Height : 20.068
Entry
ampl
0
2
4
6
8
10
12
14
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18
20
0
10
20
30
40
50
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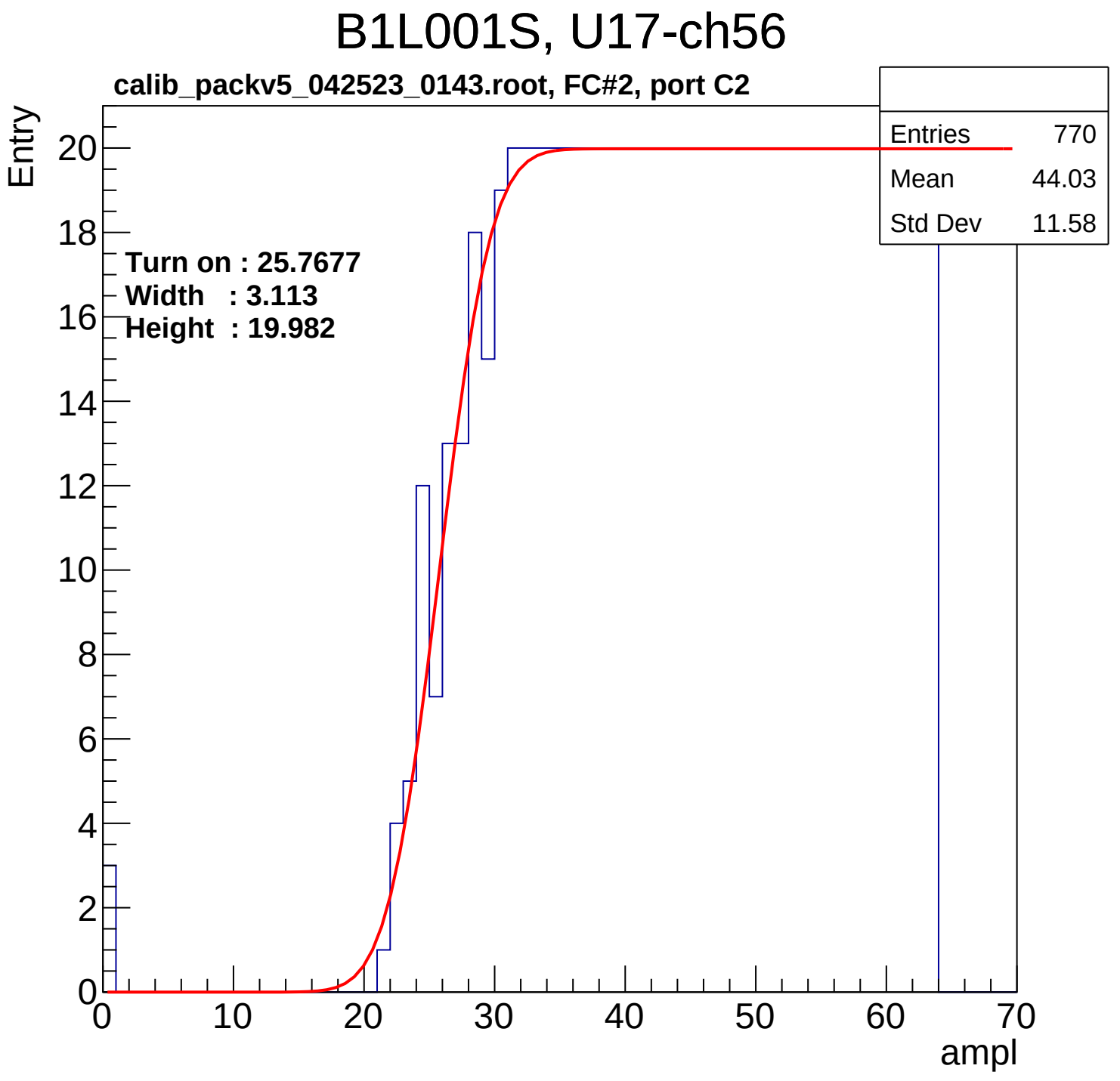
B1L001S, U17-ch56
calib_packv5_042523_0143.root, FC#2, port C2
Entries 770
Mean 44.03
Std Dev 11.58
Turn on : 25.7677
Width : 3.113
Height : 19.982
Entry
ampl
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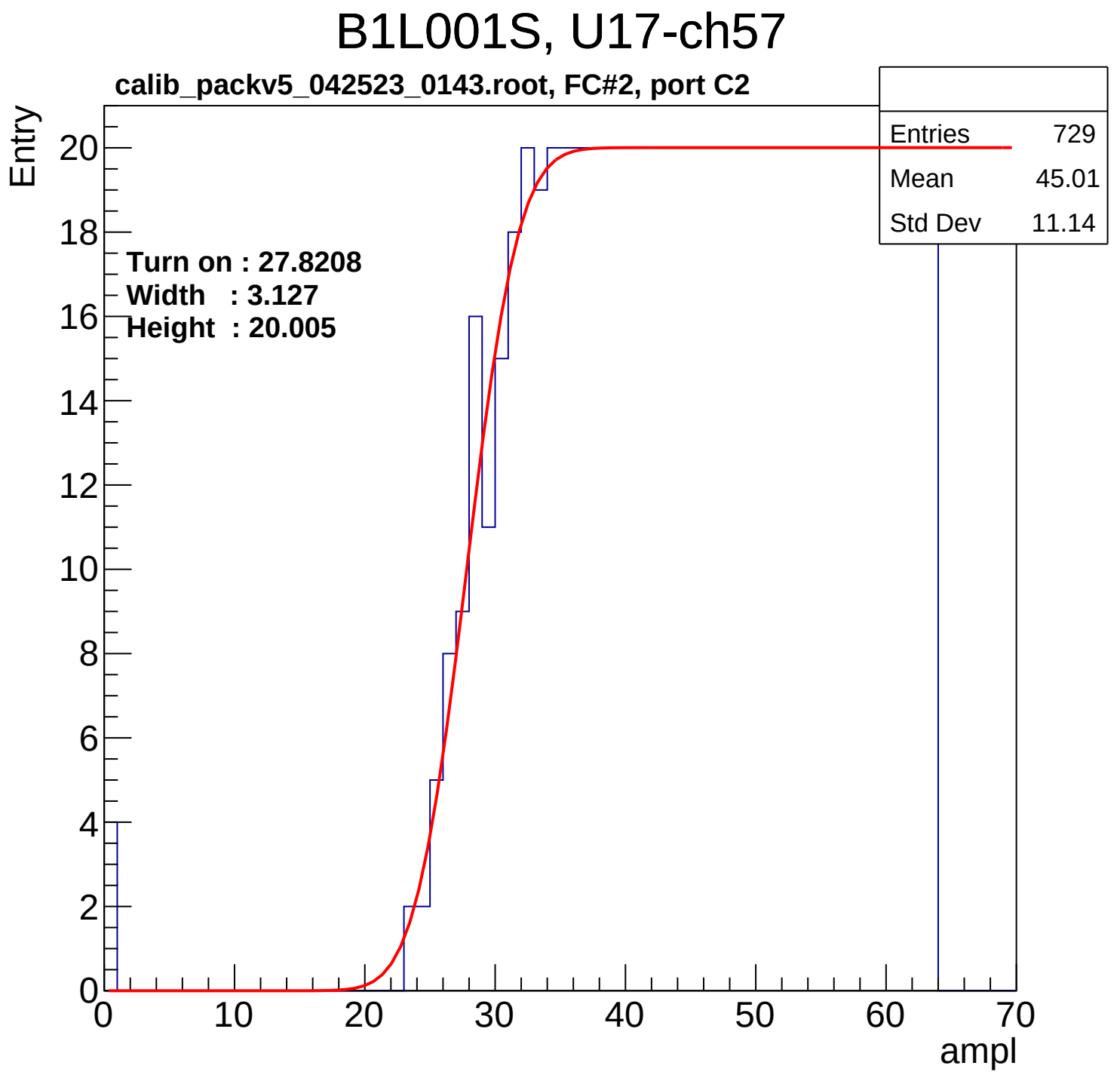
B1L001S, U17-ch57
calib_packv5_042523_0143.root, FC#2, port C2
Entries 729
Mean 45.01
Std Dev 11.14
Turn on : 27.8208
Width : 3.127
Height : 20.005
Entry
ampl
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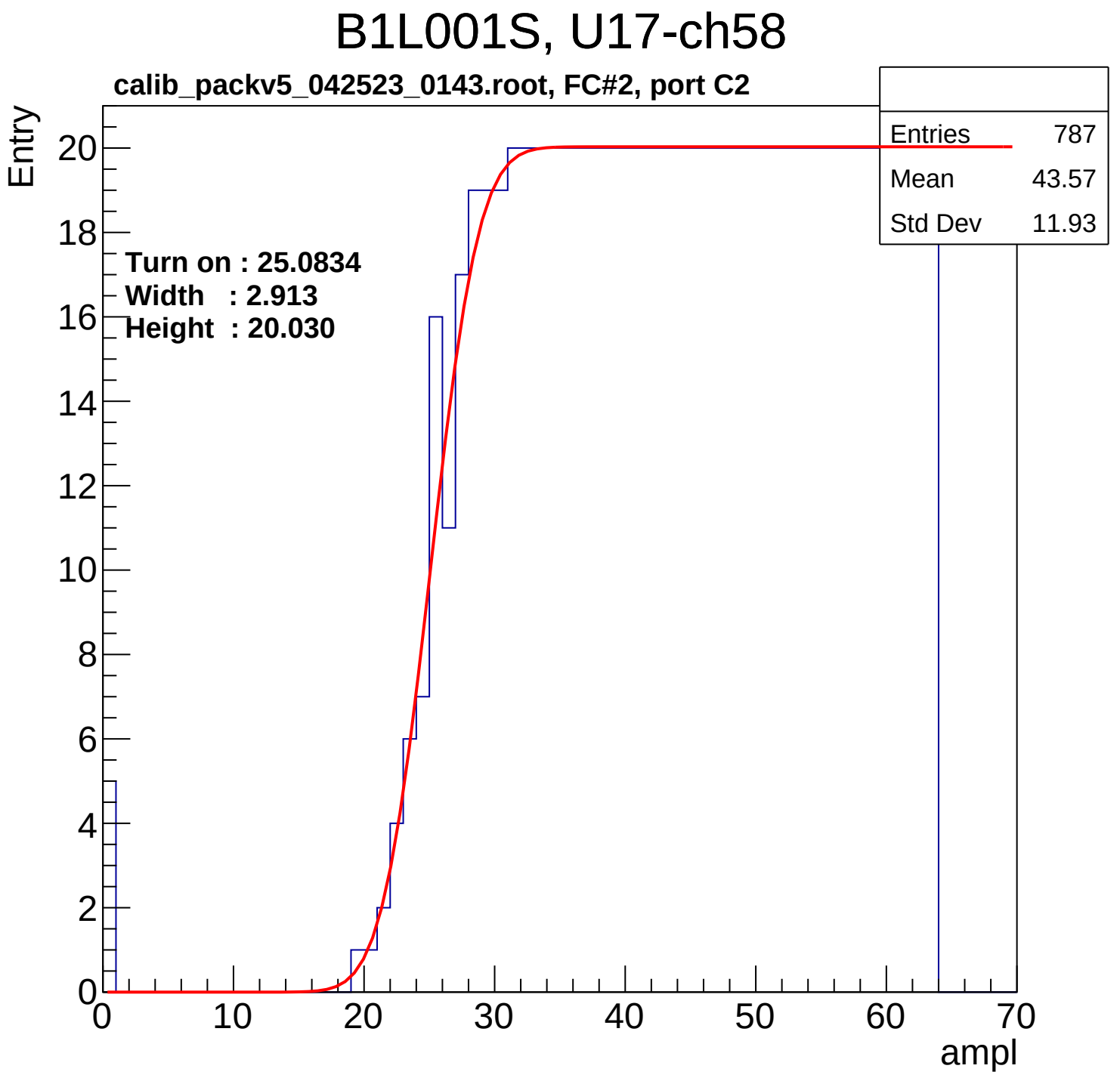
B1L001S, U17-ch58
calib_packv5_042523_0143.root, FC#2, port C2
Entries 787
Mean 43.57
Std Dev 11.93
Turn on : 25.0834
Width : 2.913
Height : 20.030
Entry
ampl
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6
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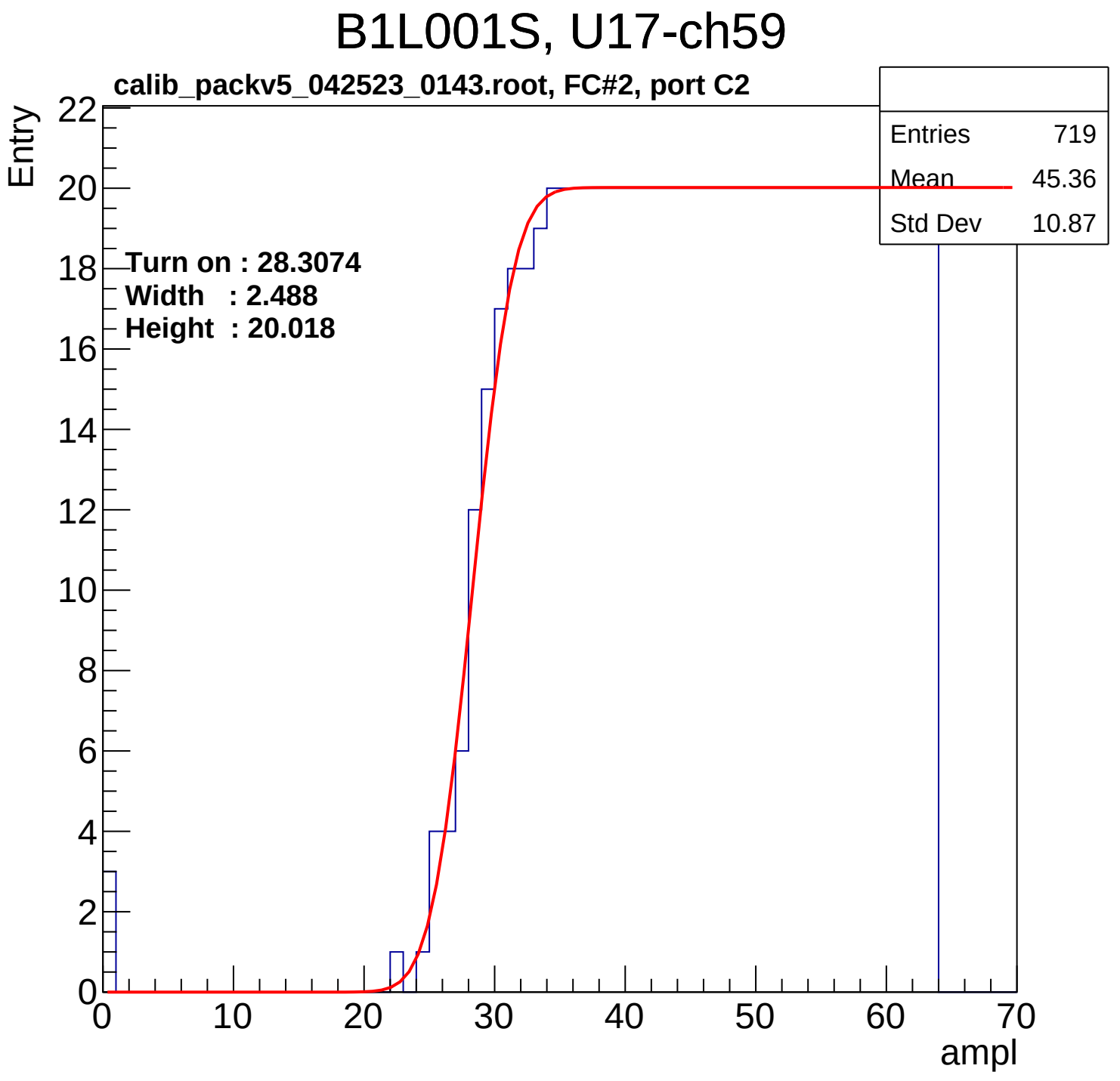
B1L001S, U17-ch59
calib_packv5_042523_0143.root, FC#2, port C2
Entries 719
Mean 45.36
Std Dev 10.87
Turn on : 28.3074
Width : 2.488
Height : 20.018
Entry
ampl
0
2
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6
8
10
12
14
16
18
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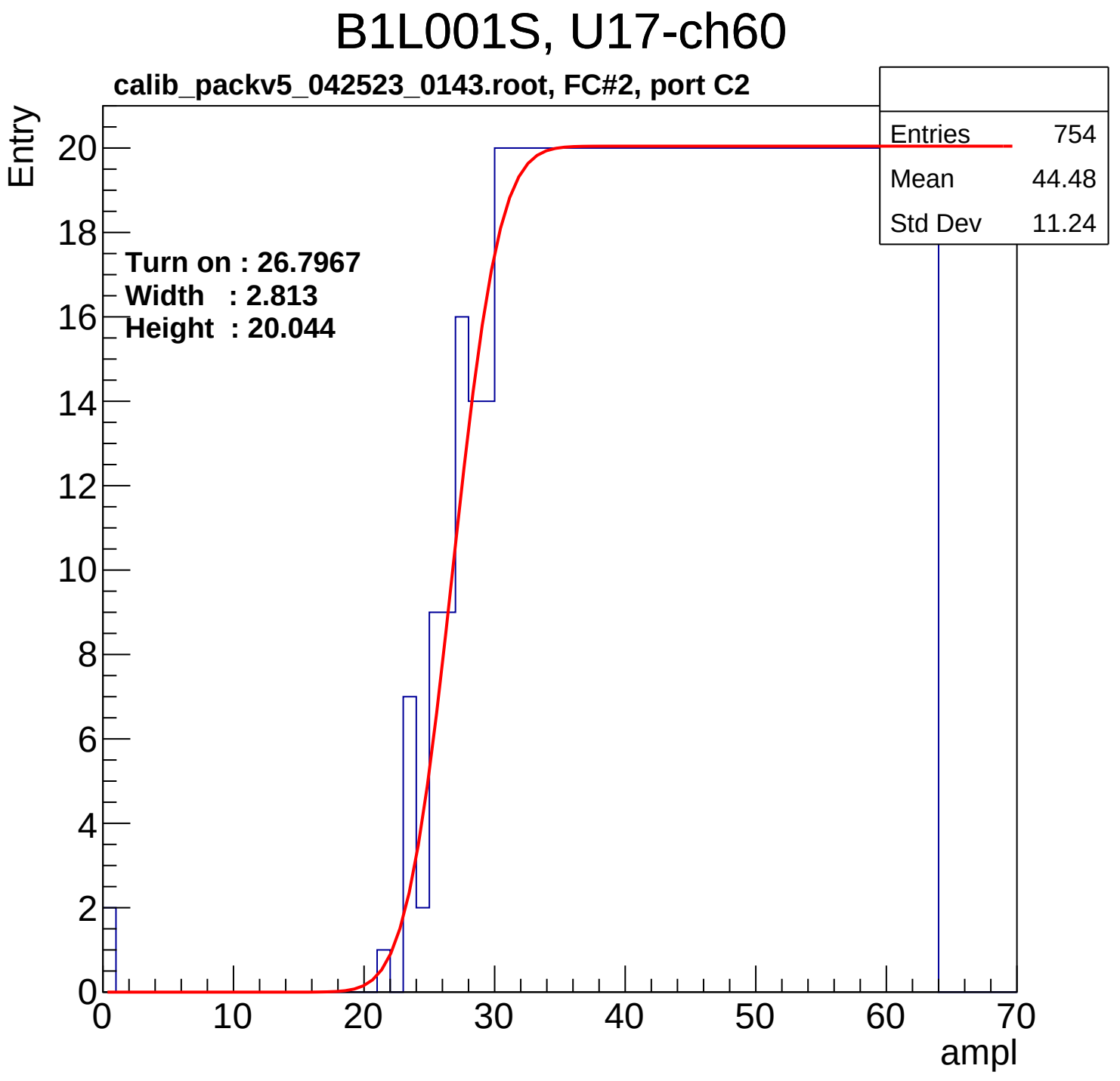
B1L001S, U17-ch60
calib_packv5_042523_0143.root, FC#2, port C2
Entries 754
Mean 44.48
Std Dev 11.24
Turn on : 26.7967
Width : 2.813
Height : 20.044
Entry
ampl
0
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4
6
8
10
12
14
16
18
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0
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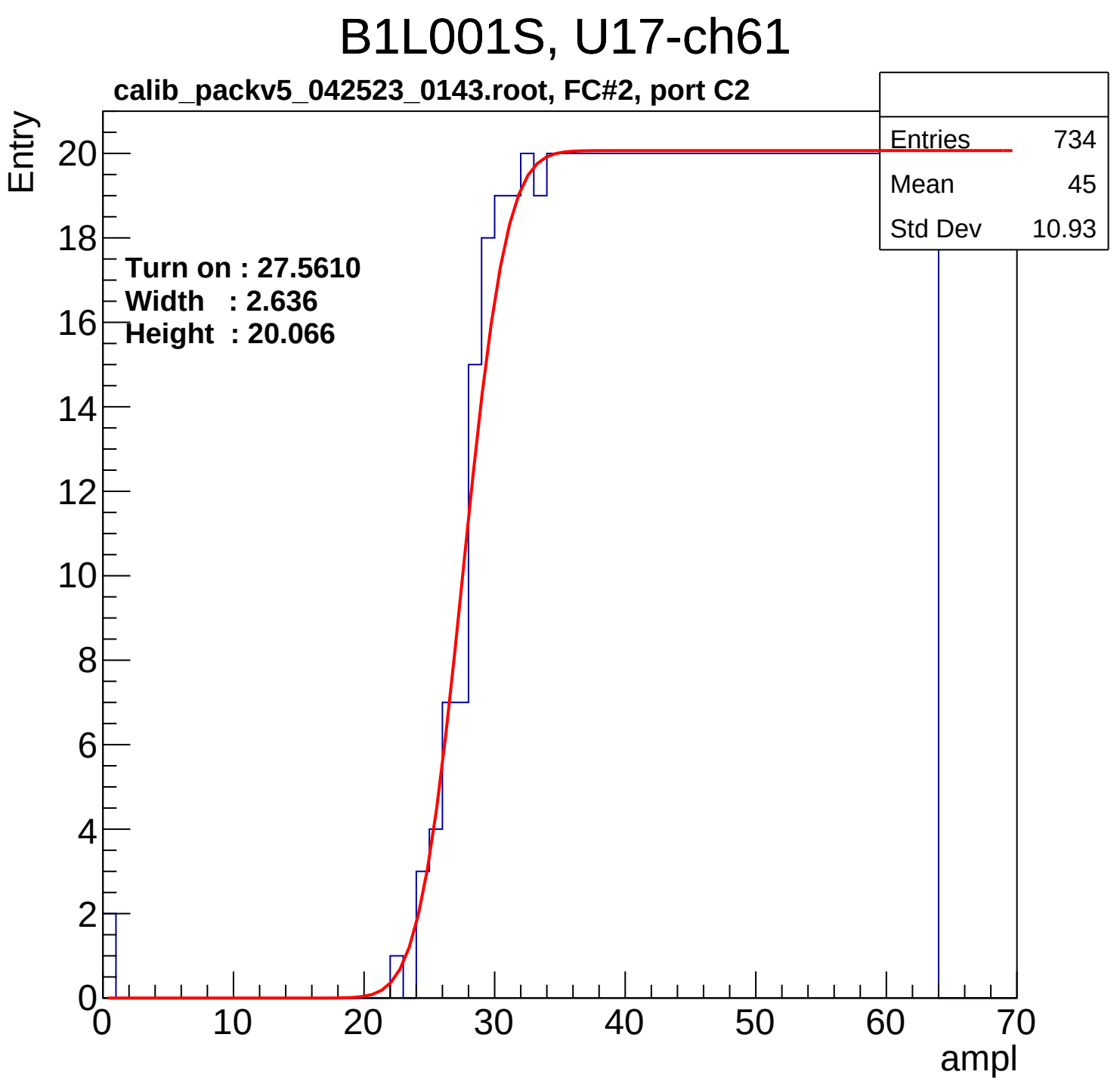
B1L001S, U17-ch61
calib_packv5_042523_0143.root, FC#2, port C2
Entries 734
Mean 45
Std Dev 10.93
Turn on : 27.5610
Width : 2.636
Height : 20.066
Entry
ampl
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6
8
10
12
14
16
18
20
0
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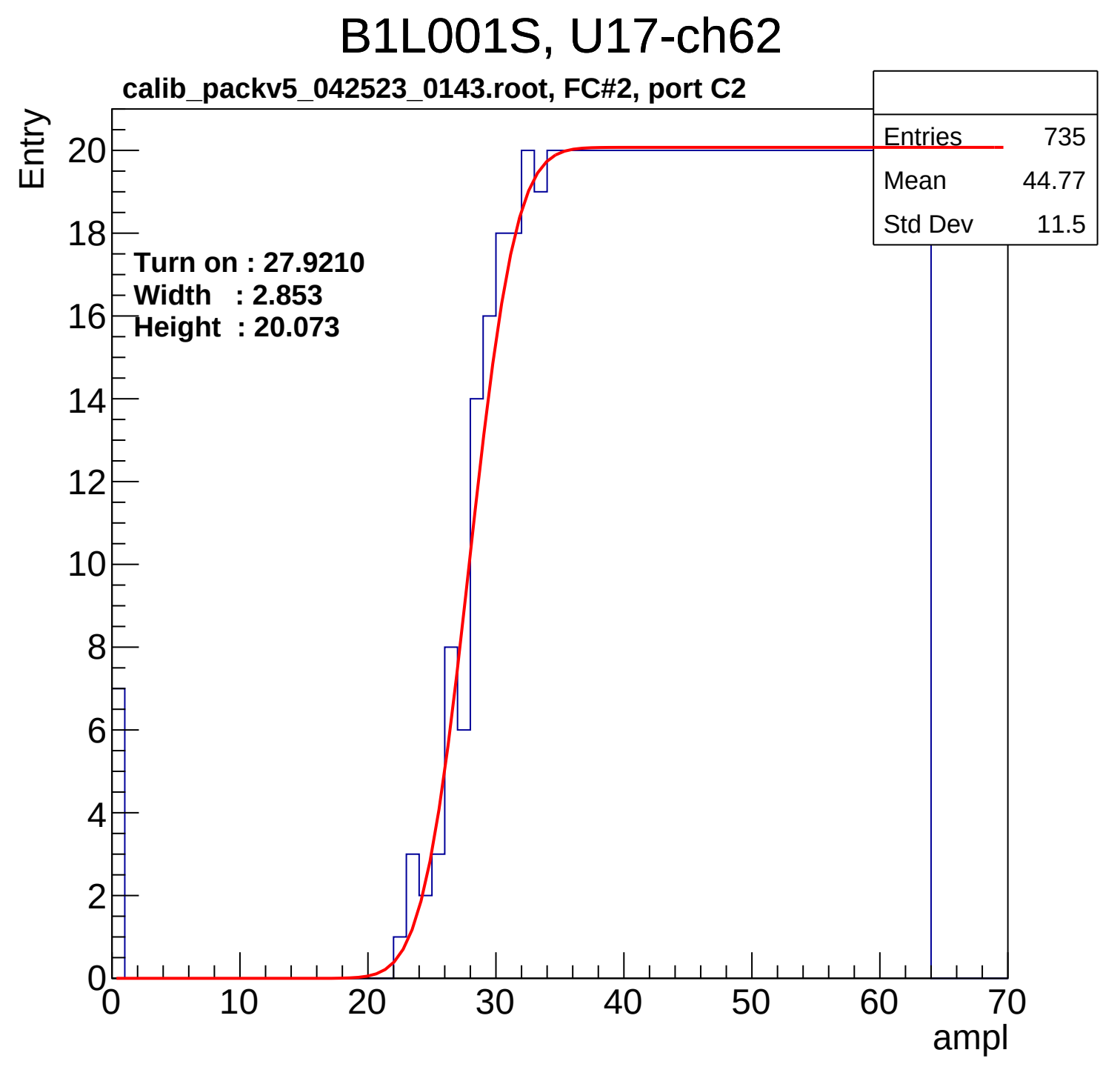
B1L001S, U17-ch62
calib_packv5_042523_0143.root, FC#2, port C2
Entries 735
Mean 44.77
Std Dev 11.5
Turn on : 27.9210
Width : 2.853
Height : 20.073
Entry
ampl
0
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6
8
10
12
14
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18
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0
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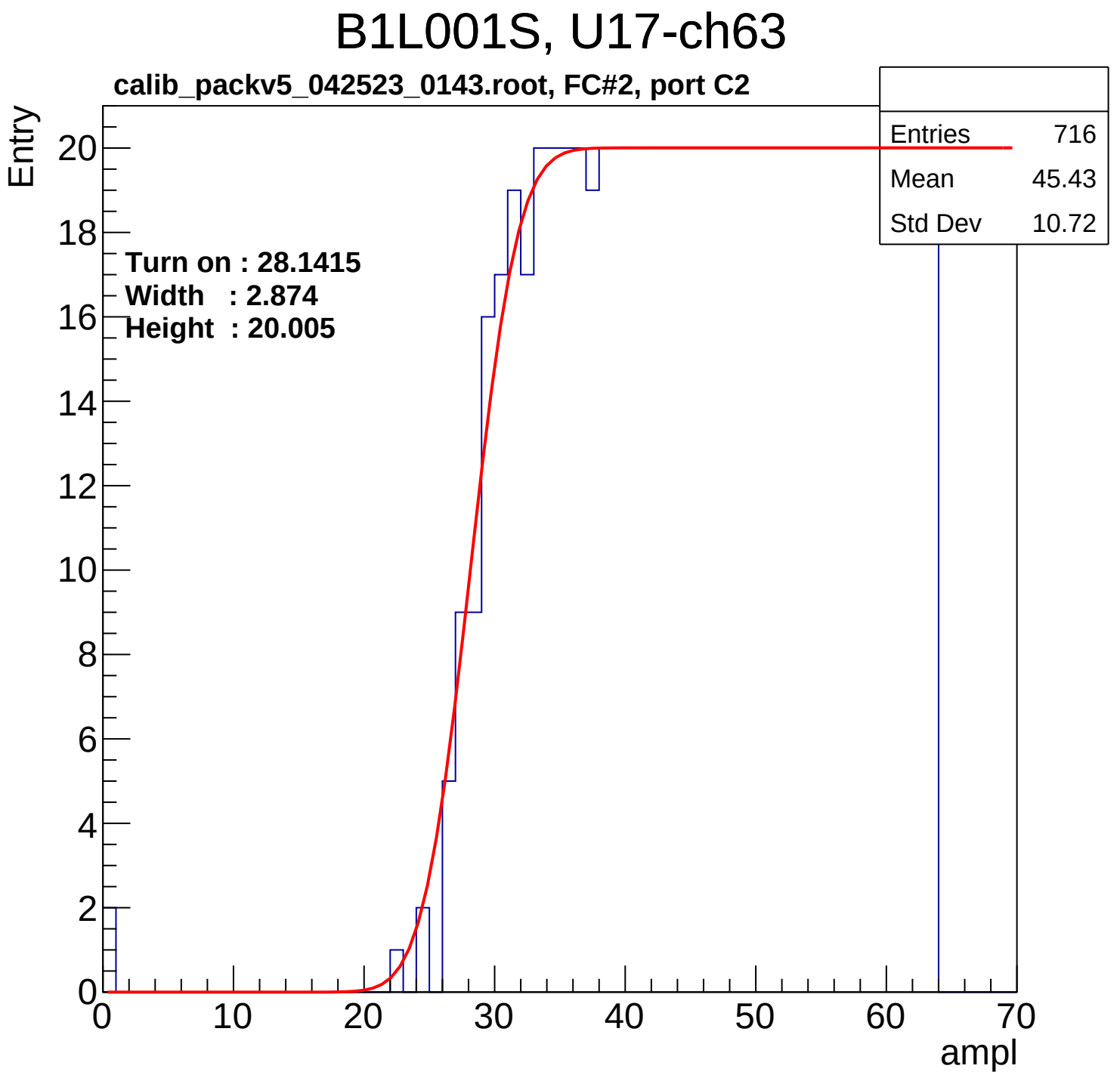
B1L001S, U17-ch63
calib_packv5_042523_0143.root, FC#2, port C2
Entries 716
Mean 45.43
Std Dev 10.72
Turn on : 28.1415
Width : 2.874
Height : 20.005
Entry
ampl
0
2
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6
8
10
12
14
16
18
20
0
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20
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60
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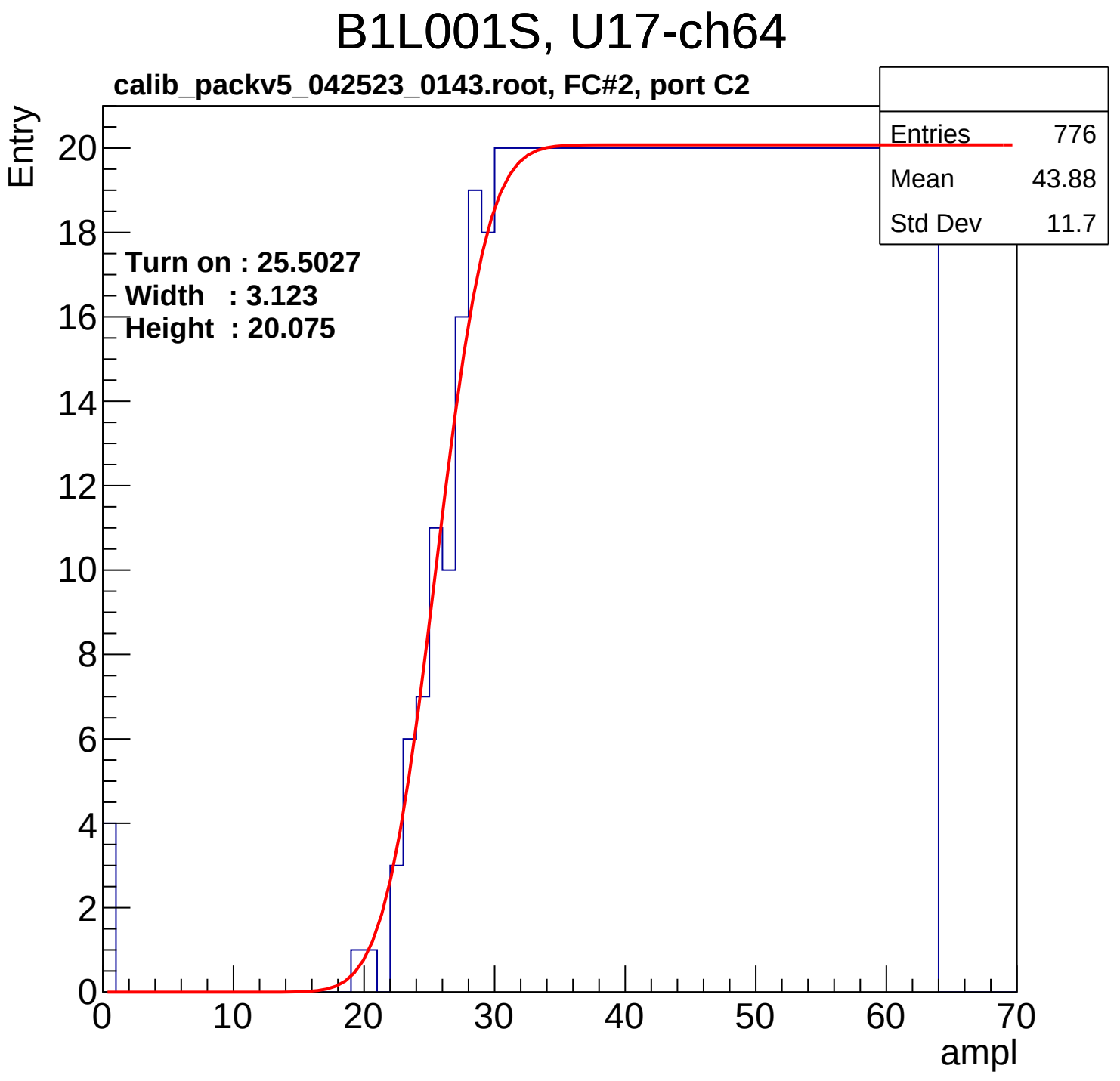
B1L001S, U17-ch64
calib_packv5_042523_0143.root, FC#2, port C2
Entries 776
Mean 43.88
Std Dev 11.7
Turn on : 25.5027
Width : 3.123
Height : 20.075
Entry
ampl
0
2
4
6
8
10
12
14
16
18
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0
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20
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60
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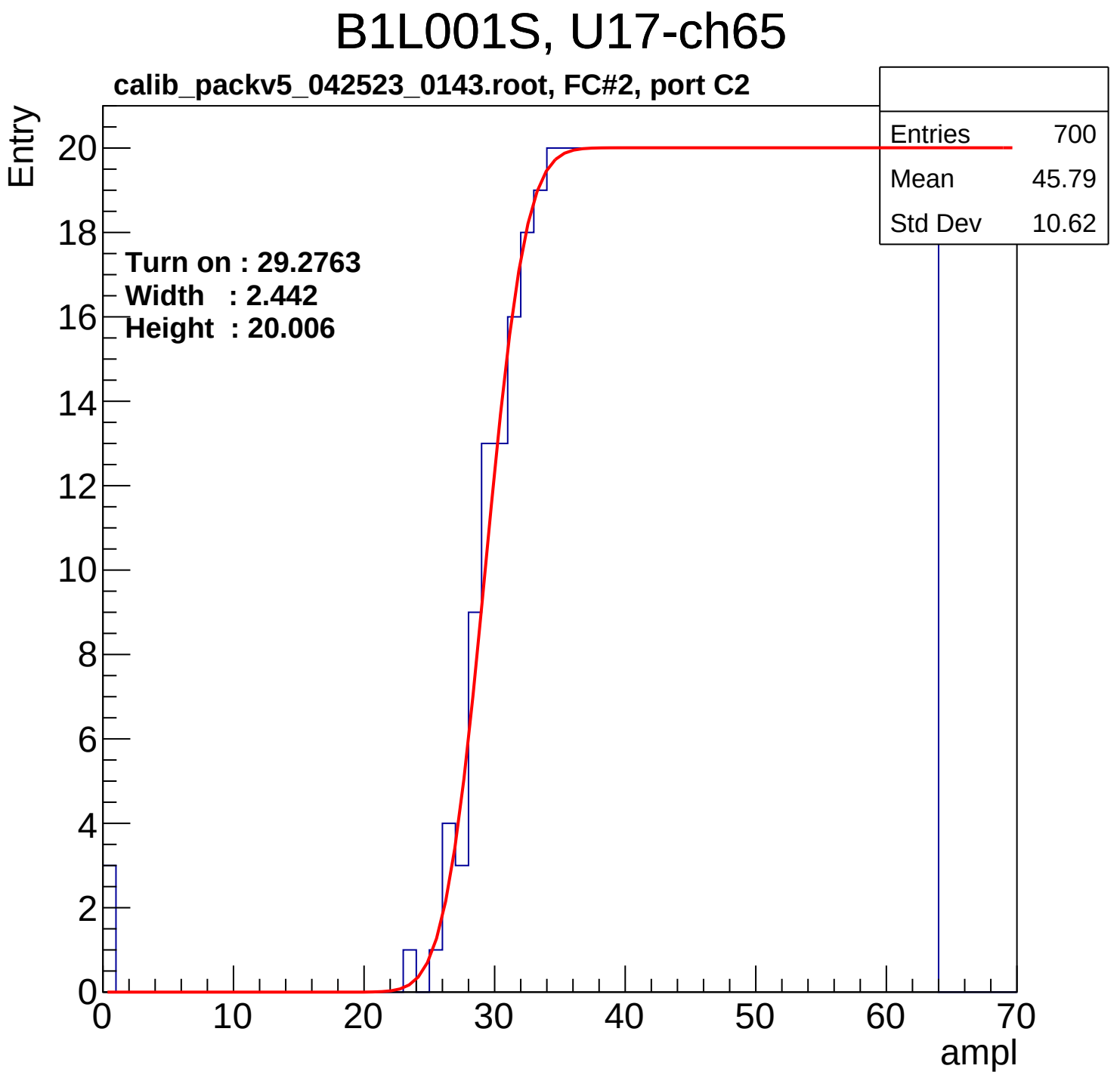
B1L001S, U17-ch65
calib_packv5_042523_0143.root, FC#2, port C2
Entries 700
Mean 45.79
Std Dev 10.62
Turn on : 29.2763
Width : 2.442
Height : 20.006
Entry
ampl
0
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6
8
10
12
14
16
18
20
0
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20
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60
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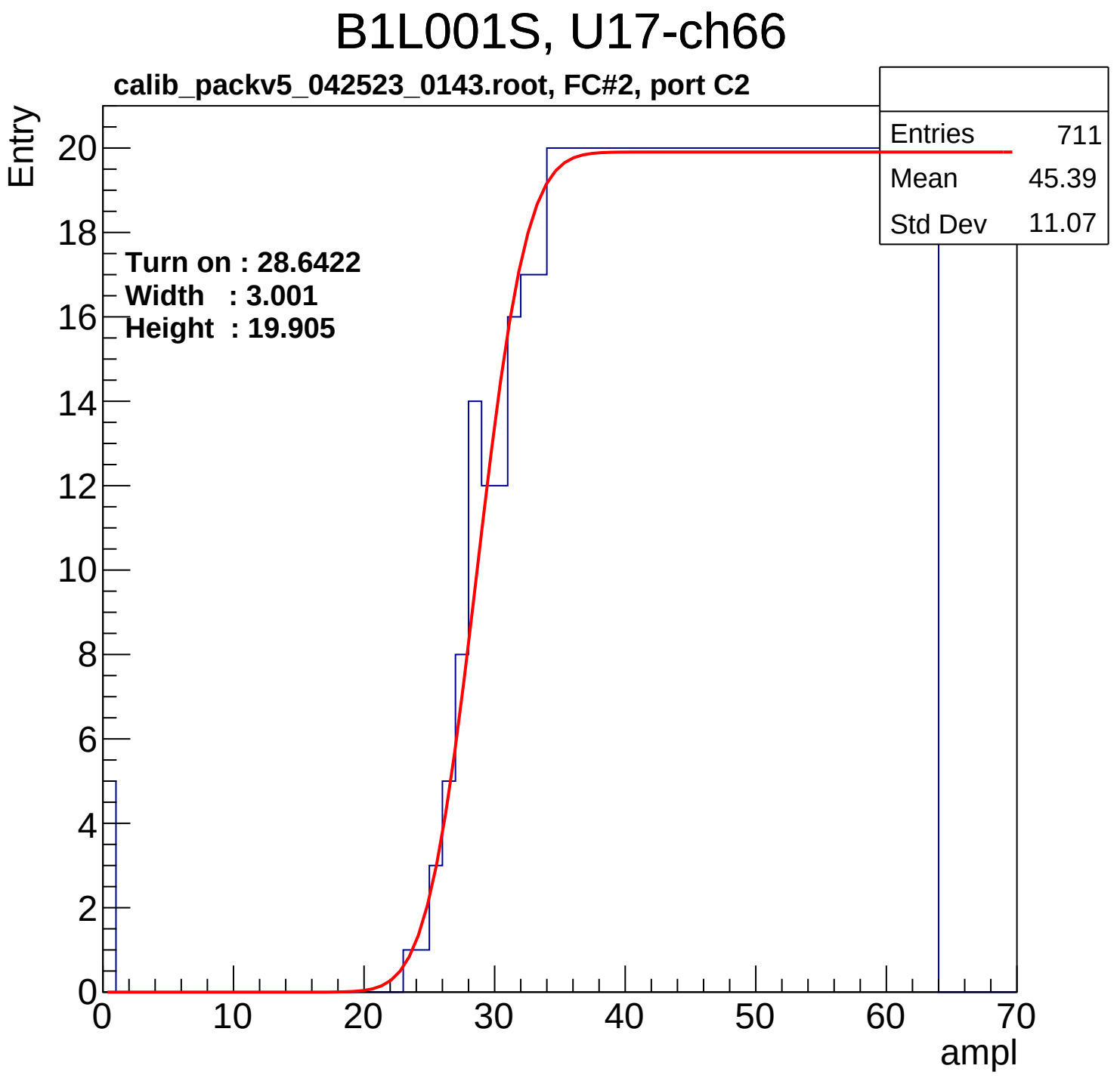
B1L001S, U17-ch66
calib_packv5_042523_0143.root, FC#2, port C2
Entries 711
Mean 45.39
Std Dev 11.07
Turn on : 28.6422
Width : 3.001
Height : 19.905
Entry
ampl
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6
8
10
12
14
16
18
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0
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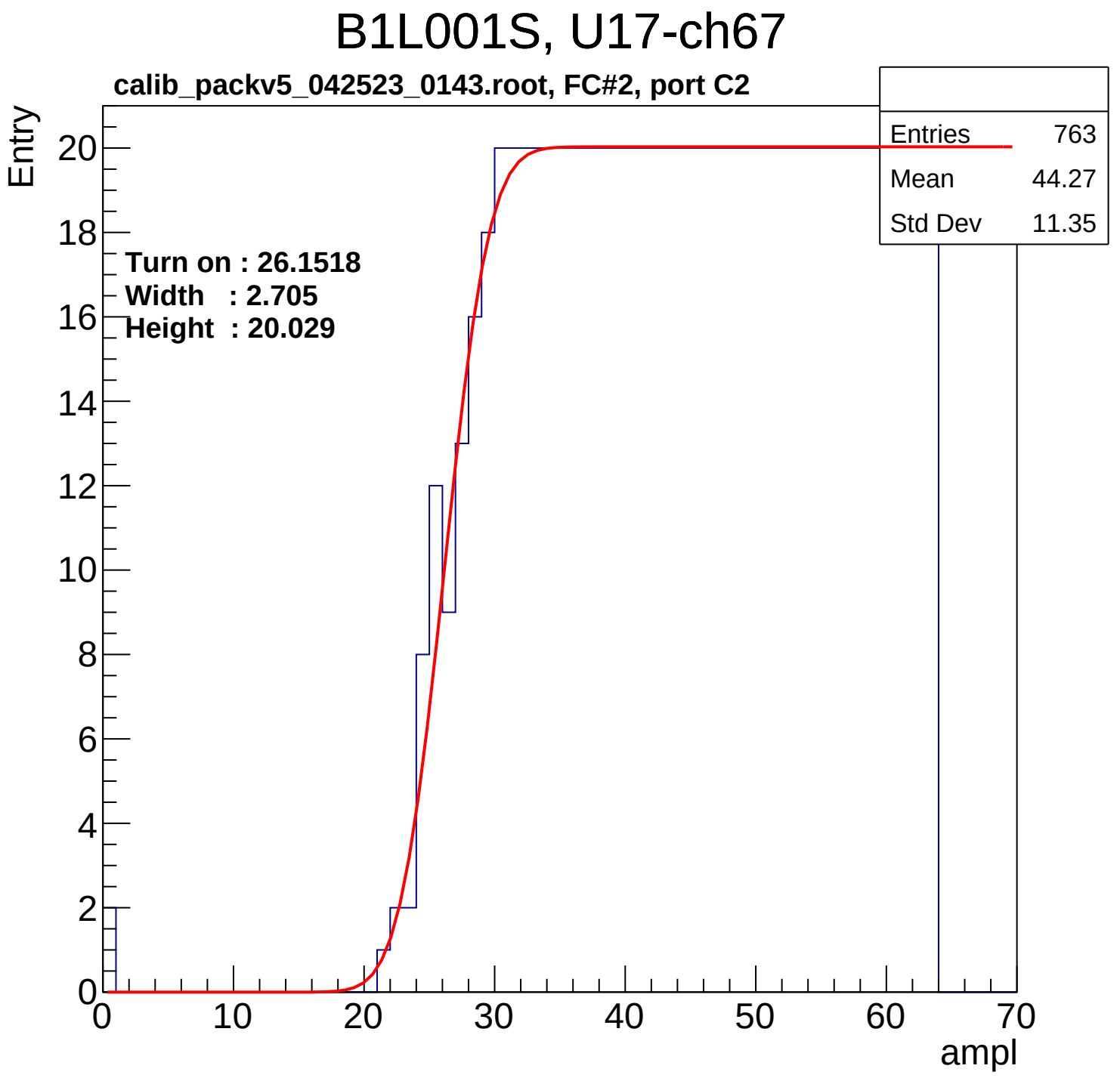
B1L001S, U17-ch67
calib_packv5_042523_0143.root, FC#2, port C2
Entries 763
Mean 44.27
Std Dev 11.35
Turn on : 26.1518
Width : 2.705
Height : 20.029
Entry
ampl
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4
6
8
10
12
14
16
18
20
0
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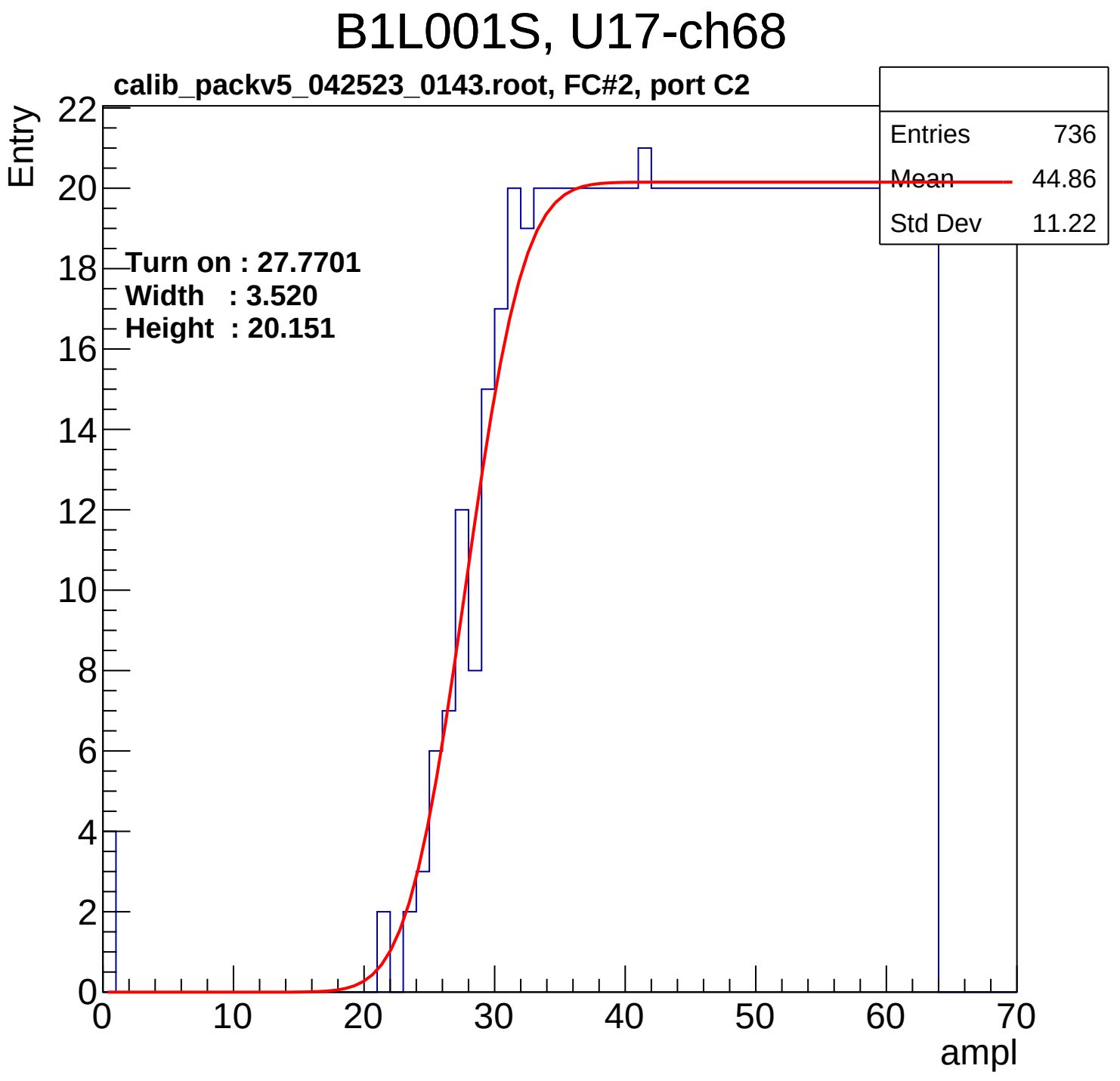
B1L001S, U17-ch68
calib_packv5_042523_0143.root, FC#2, port C2
Entries 736
Mean 44.86
Std Dev 11.22
Turn on : 27.7701
Width : 3.520
Height : 20.151
Entry
ampl
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12
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16
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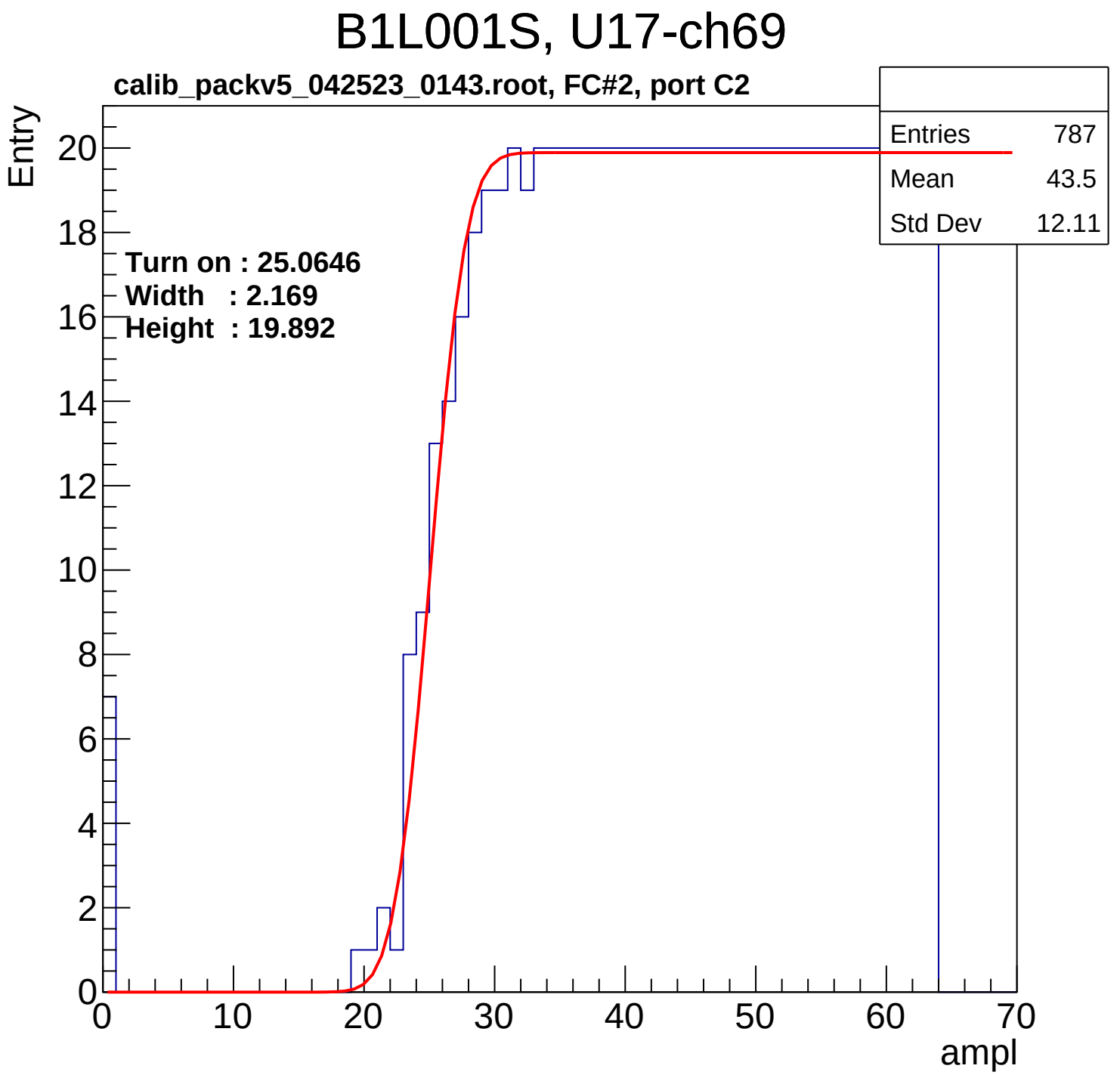
B1L001S, U17-ch69
calib_packv5_042523_0143.root, FC#2, port C2
Entries 787
Mean 43.5
Std Dev 12.11
Turn on : 25.0646
Width : 2.169
Height : 19.892
Entry
ampl
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6
8
10
12
14
16
18
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0
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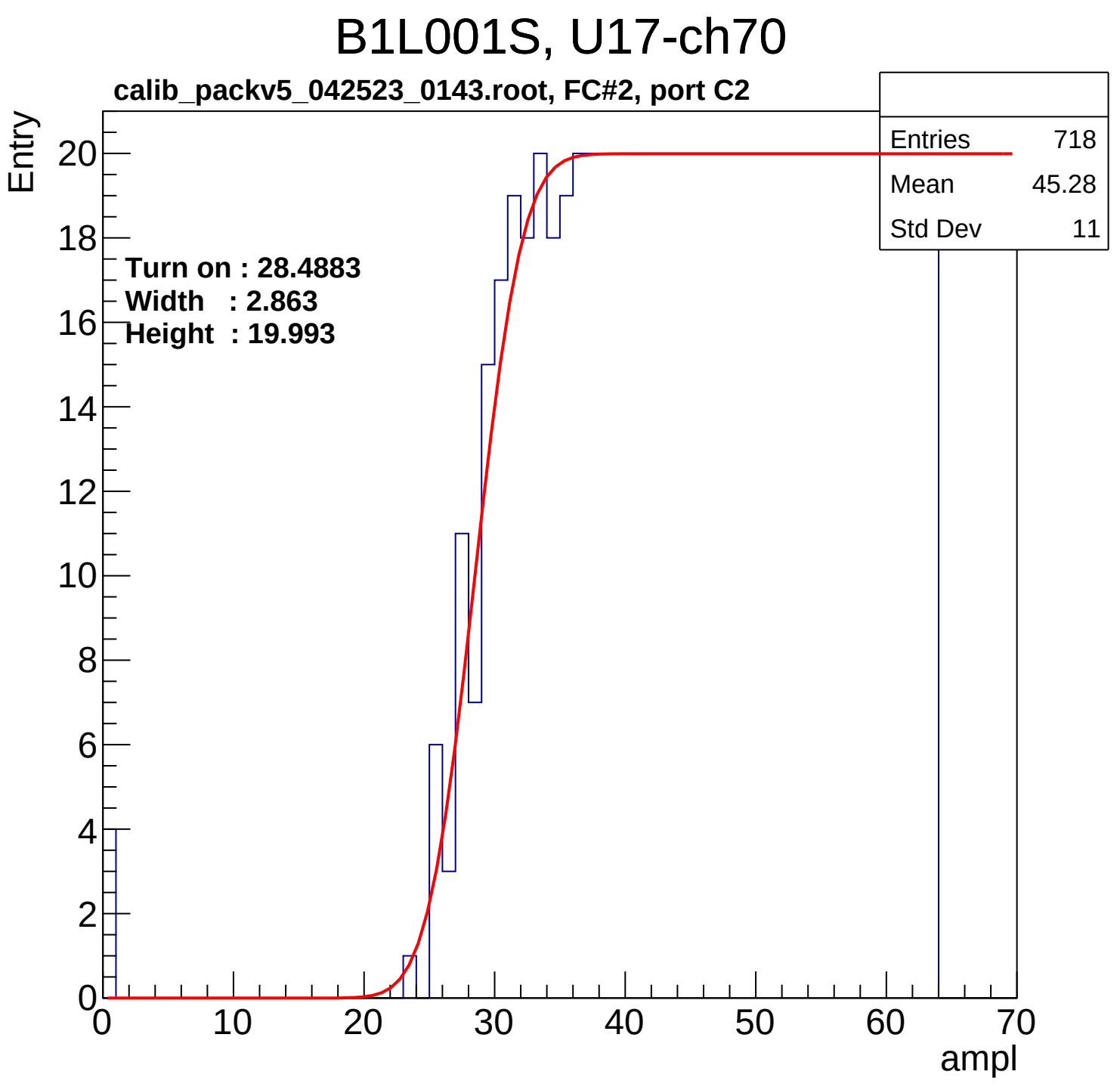
B1L001S, U17-ch70
calib_packv5_042523_0143.root, FC#2, port C2
Entries 718
Mean 45.28
Std Dev 11
Turn on : 28.4883
Width : 2.863
Height : 19.993
Entry
ampl
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6
8
10
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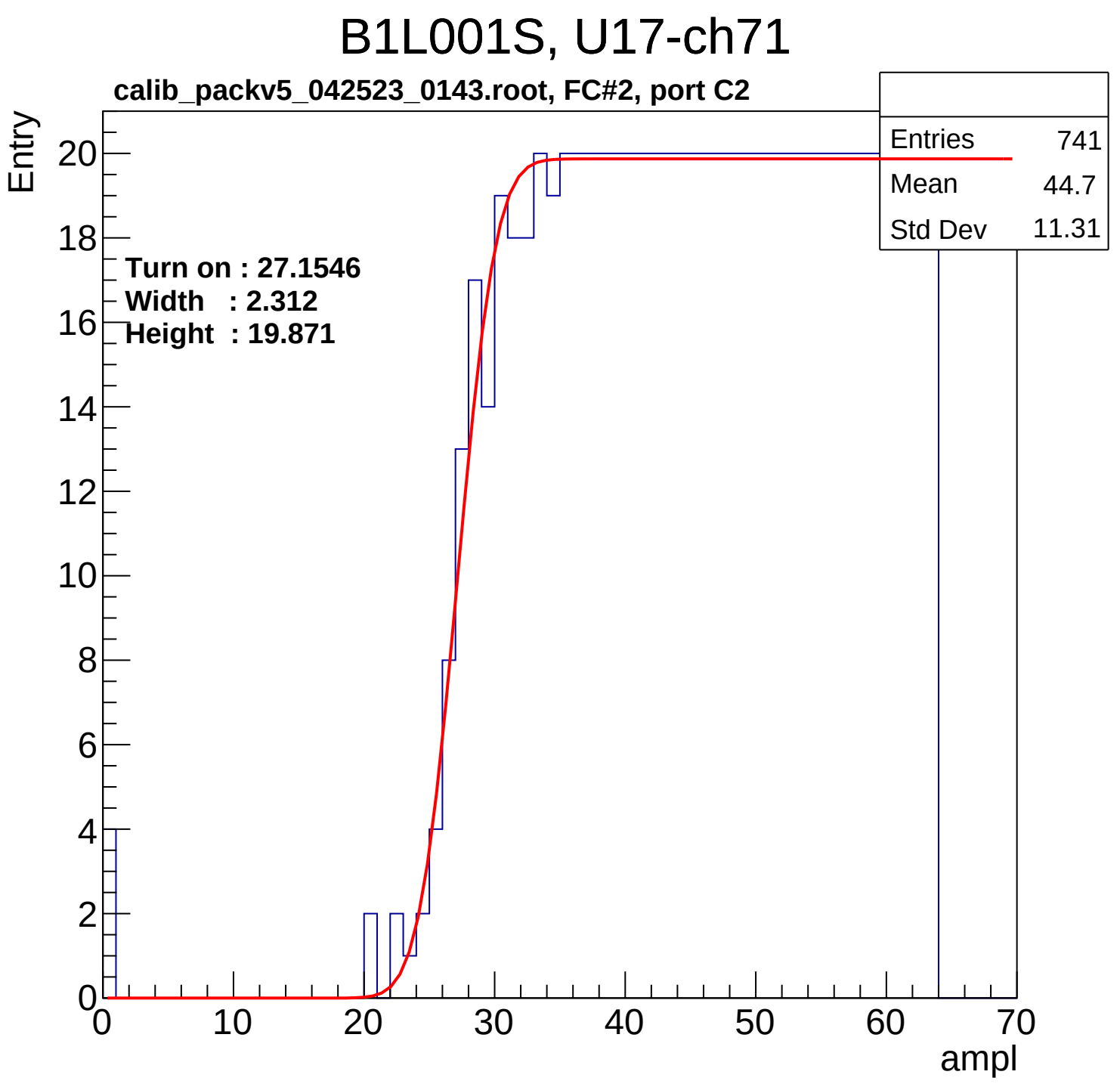
B1L001S, U17-ch71
calib_packv5_042523_0143.root, FC#2, port C2
Entries 741
Mean 44.7
Std Dev 11.31
Turn on : 27.1546
Width : 2.312
Height : 19.871
Entry
ampl
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6
8
10
12
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0
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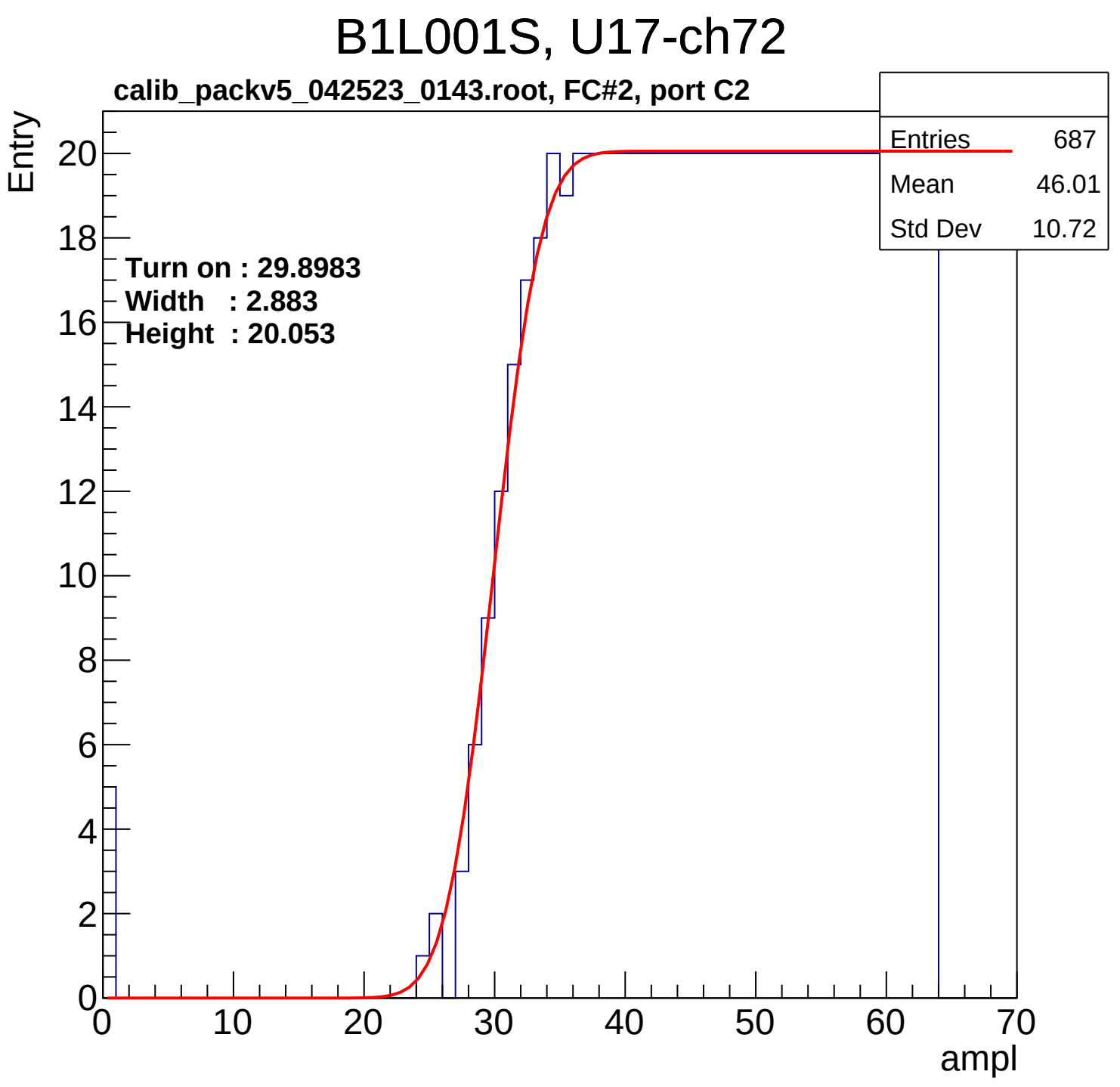
B1L001S, U17-ch72
calib_packv5_042523_0143.root, FC#2, port C2
Entries 687
Mean 46.01
Std Dev 10.72
Turn on : 29.8983
Width : 2.883
Height : 20.053
Entry
ampl
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6
8
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12
14
16
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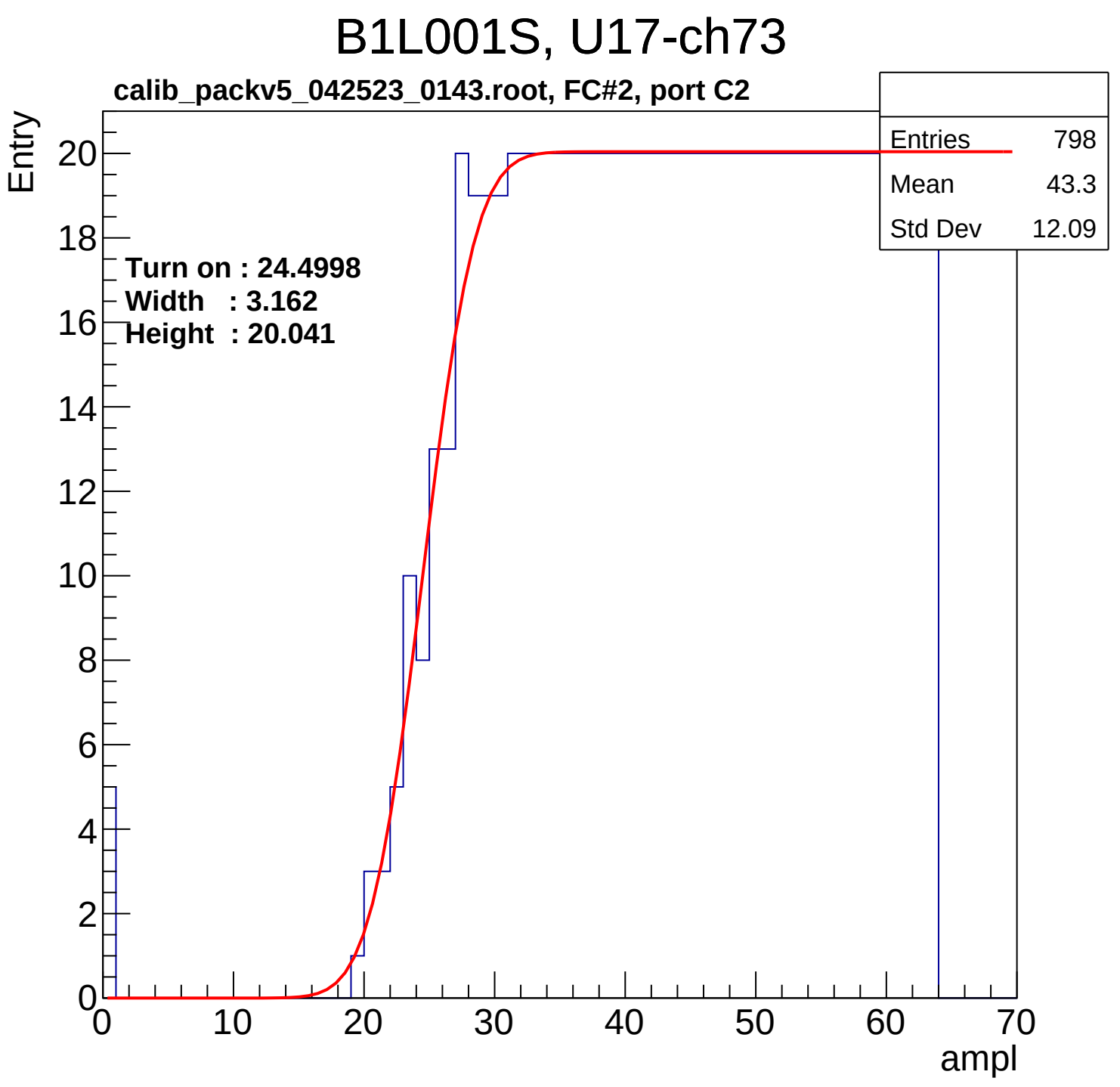
B1L001S, U17-ch73
calib_packv5_042523_0143.root, FC#2, port C2
Entries 798
Mean 43.3
Std Dev 12.09
Turn on : 24.4998
Width : 3.162
Height : 20.041
Entry
ampl
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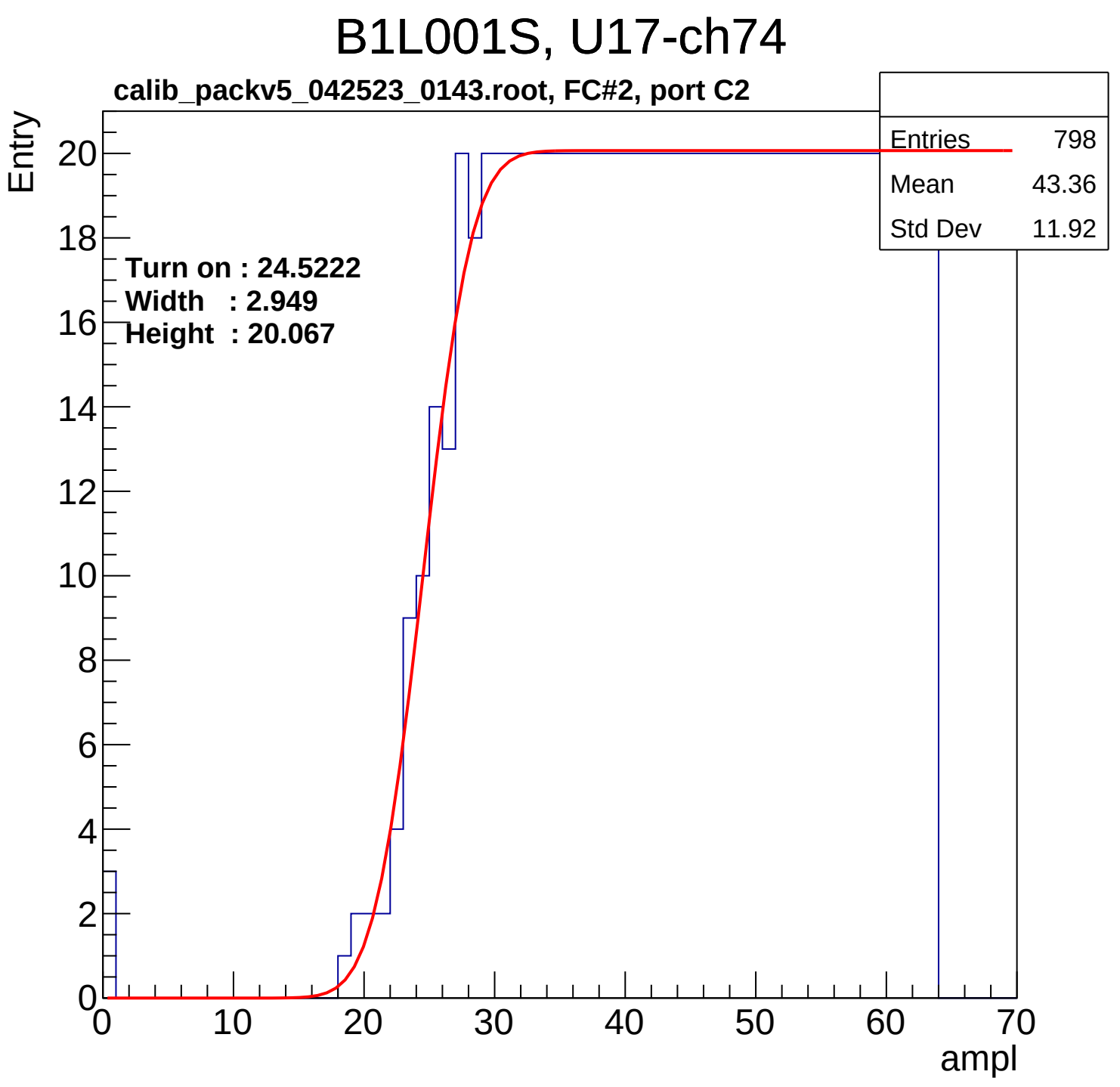
B1L001S, U17-ch74
calib_packv5_042523_0143.root, FC#2, port C2
Entries 798
Mean 43.36
Std Dev 11.92
Turn on : 24.5222
Width : 2.949
Height : 20.067
Entry
ampl
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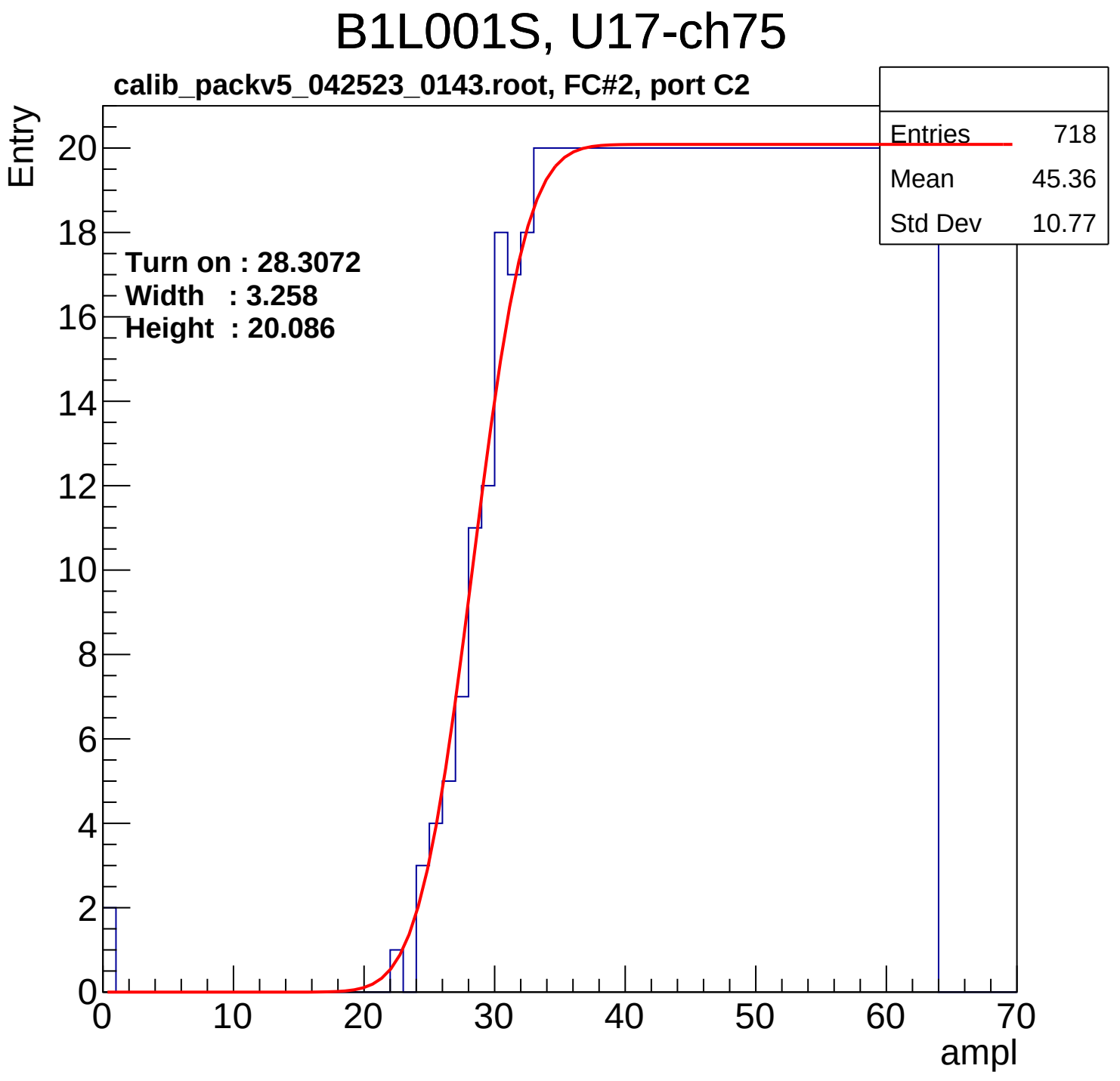
B1L001S, U17-ch75
calib_packv5_042523_0143.root, FC#2, port C2
Entries 718
Mean 45.36
Std Dev 10.77
Turn on : 28.3072
Width : 3.258
Height : 20.086
Entry
ampl
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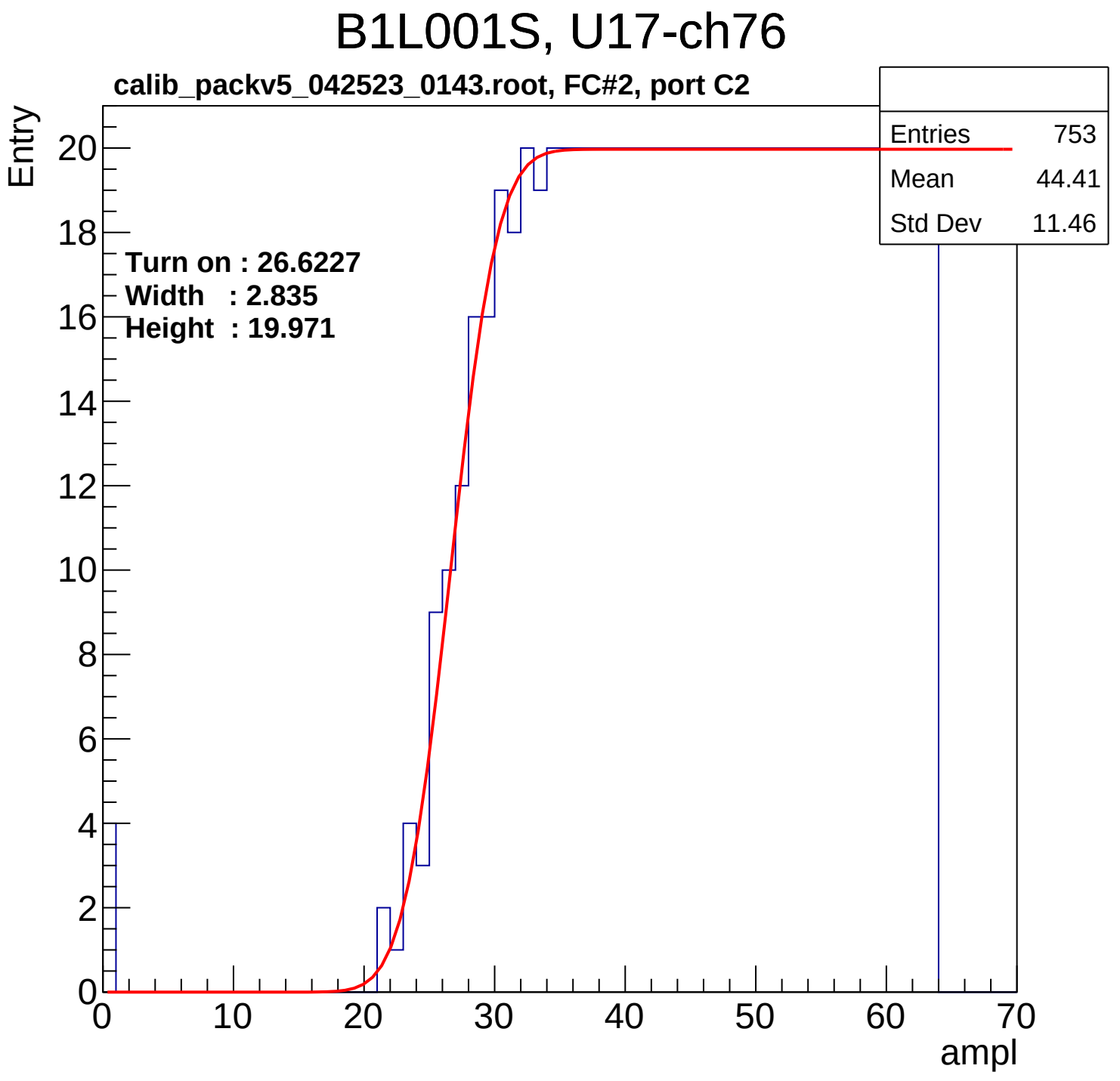
B1L001S, U17-ch76
calib_packv5_042523_0143.root, FC#2, port C2
Entries 753
Mean 44.41
Std Dev 11.46
Turn on : 26.6227
Width : 2.835
Height : 19.971
Entry
ampl
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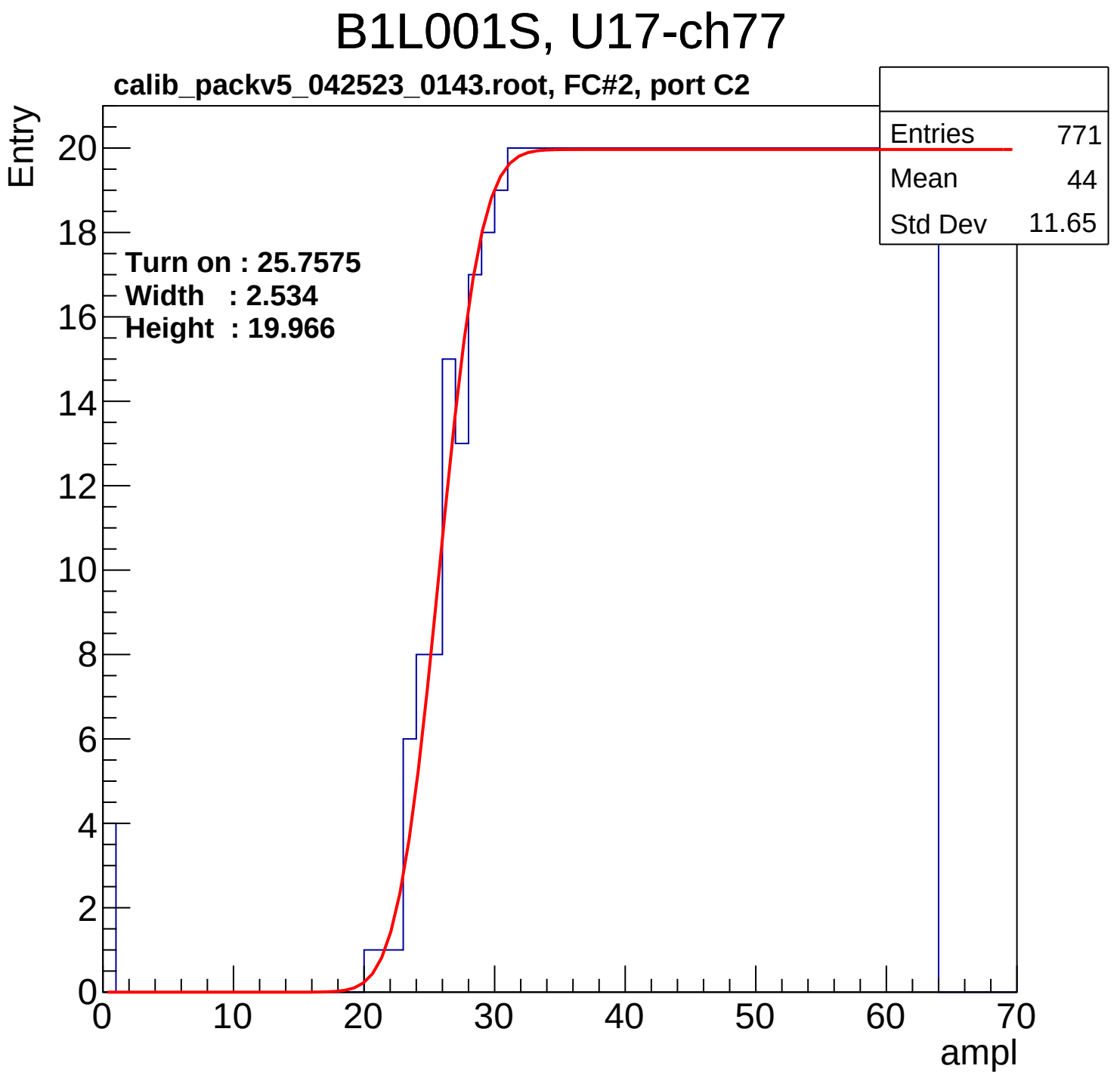
B1L001S, U17-ch77
calib_packv5_042523_0143.root, FC#2, port C2
Entries 771
Mean 44
Std Dev 11.65
Turn on : 25.7575
Width : 2.534
Height : 19.966
Entry
ampl
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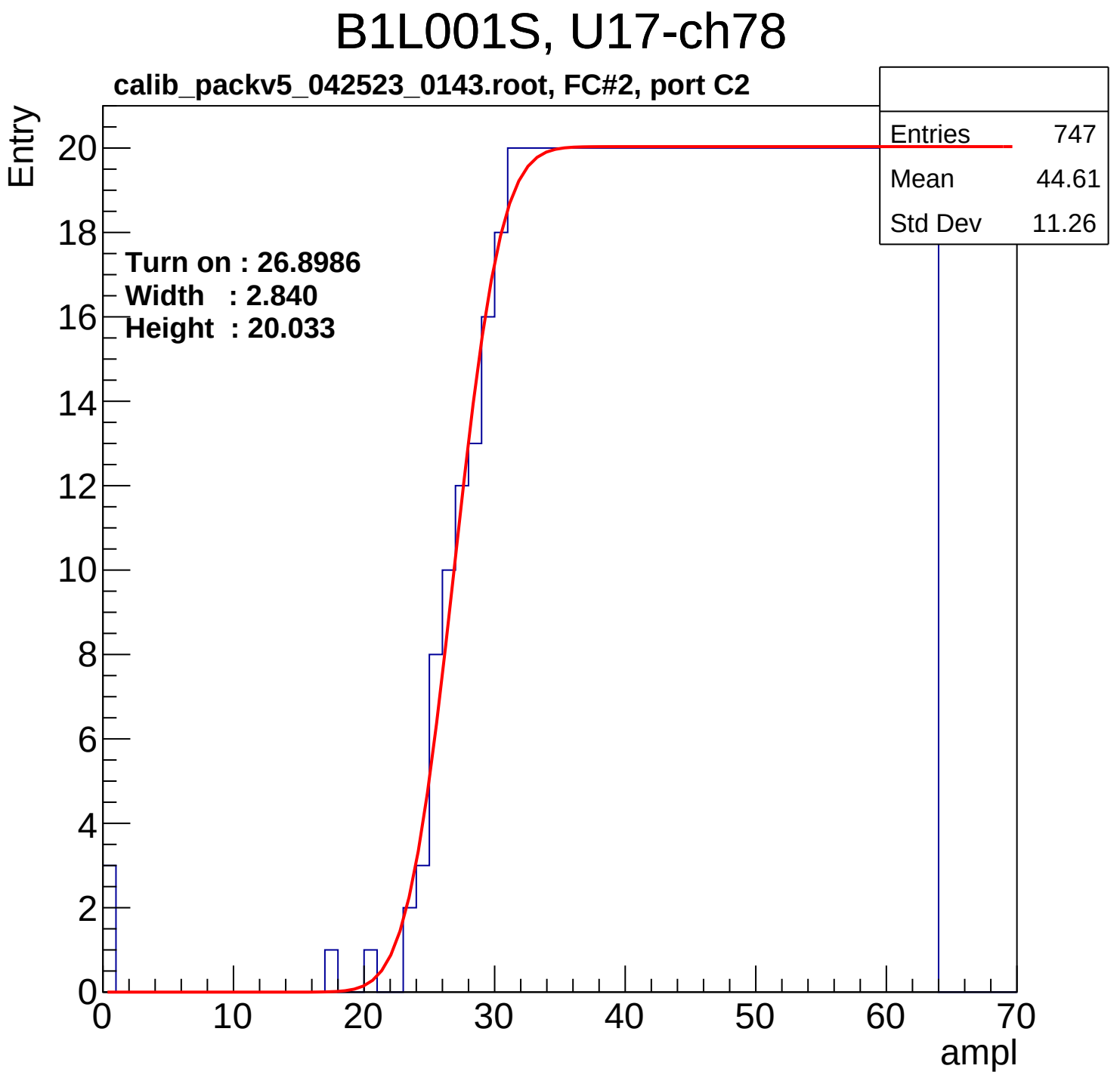
B1L001S, U17-ch78
calib_packv5_042523_0143.root, FC#2, port C2
Entries 747
Mean 44.61
Std Dev 11.26
Turn on : 26.8986
Width : 2.840
Height : 20.033
Entry
ampl
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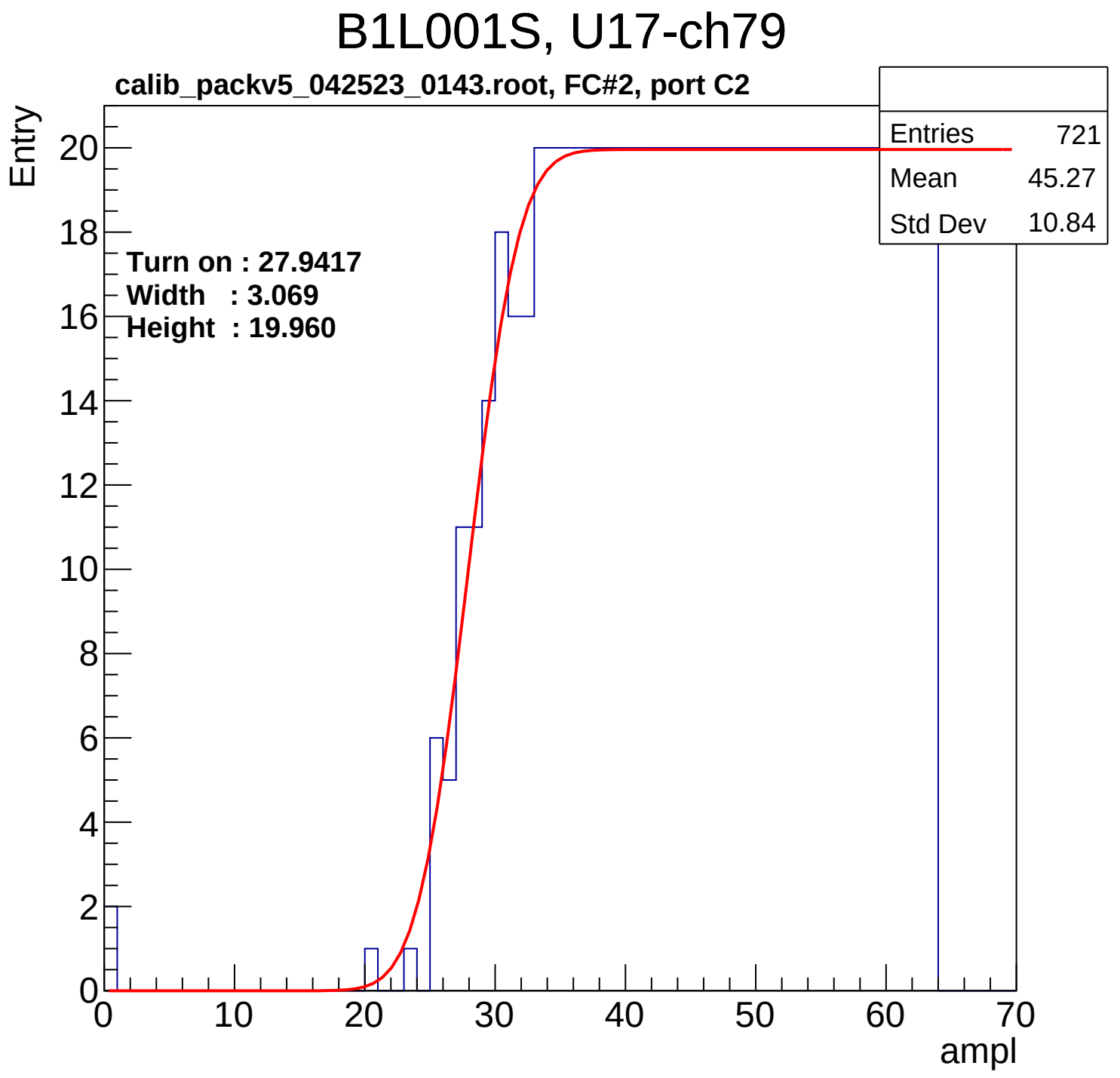
B1L001S, U17-ch79
calib_packv5_042523_0143.root, FC#2, port C2
Entries 721
Mean 45.27
Std Dev 10.84
Turn on : 27.9417
Width : 3.069
Height : 19.960
Entry
ampl
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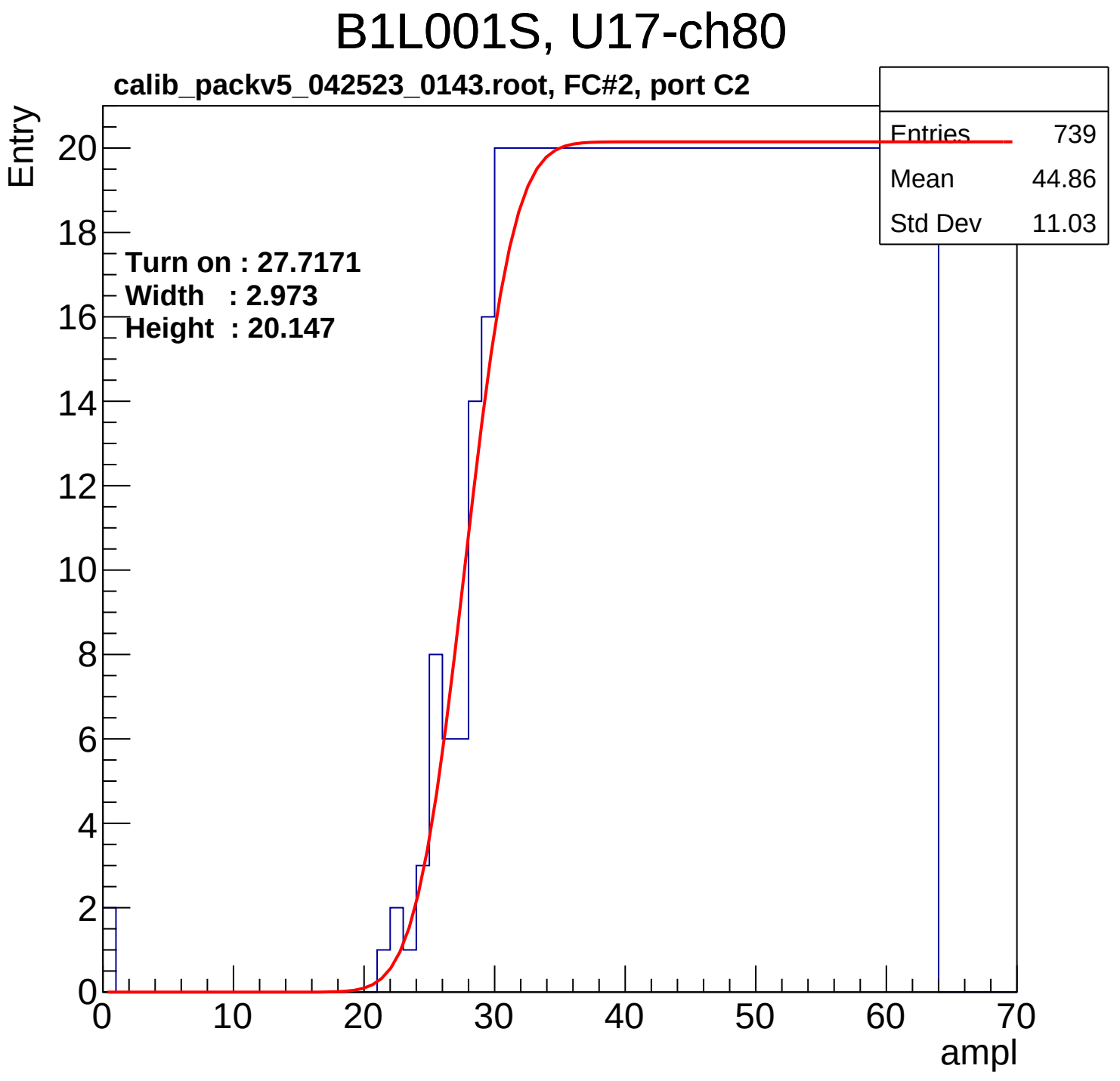
B1L001S, U17-ch80
calib_packv5_042523_0143.root, FC#2, port C2
Entries 739
Mean 44.86
Std Dev 11.03
Turn on : 27.7171
Width : 2.973
Height : 20.147
Entry
ampl
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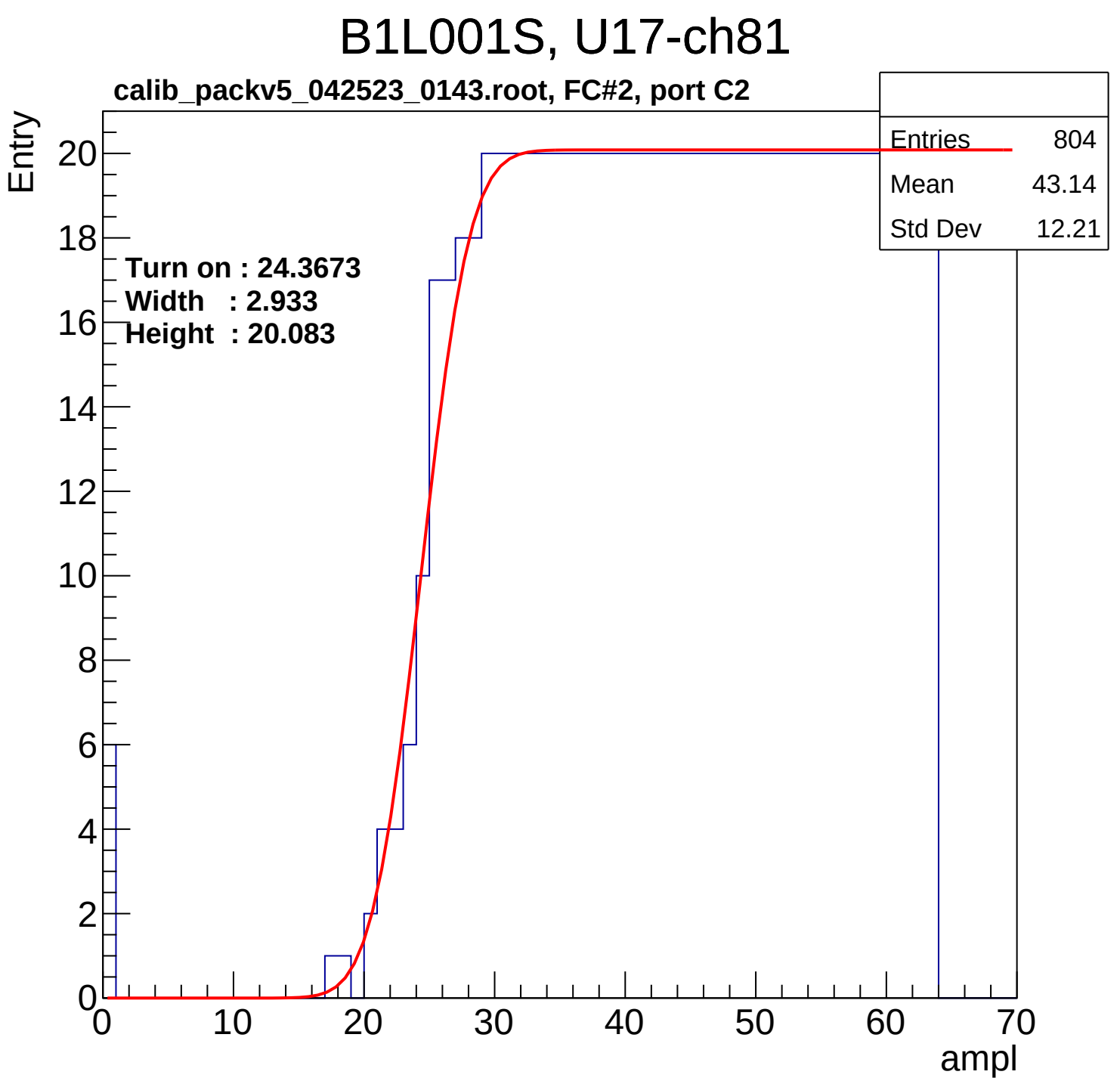
B1L001S, U17-ch81
calib_packv5_042523_0143.root, FC#2, port C2
Entries 804
Mean 43.14
Std Dev 12.21
Turn on : 24.3673
Width : 2.933
Height : 20.083
Entry
ampl
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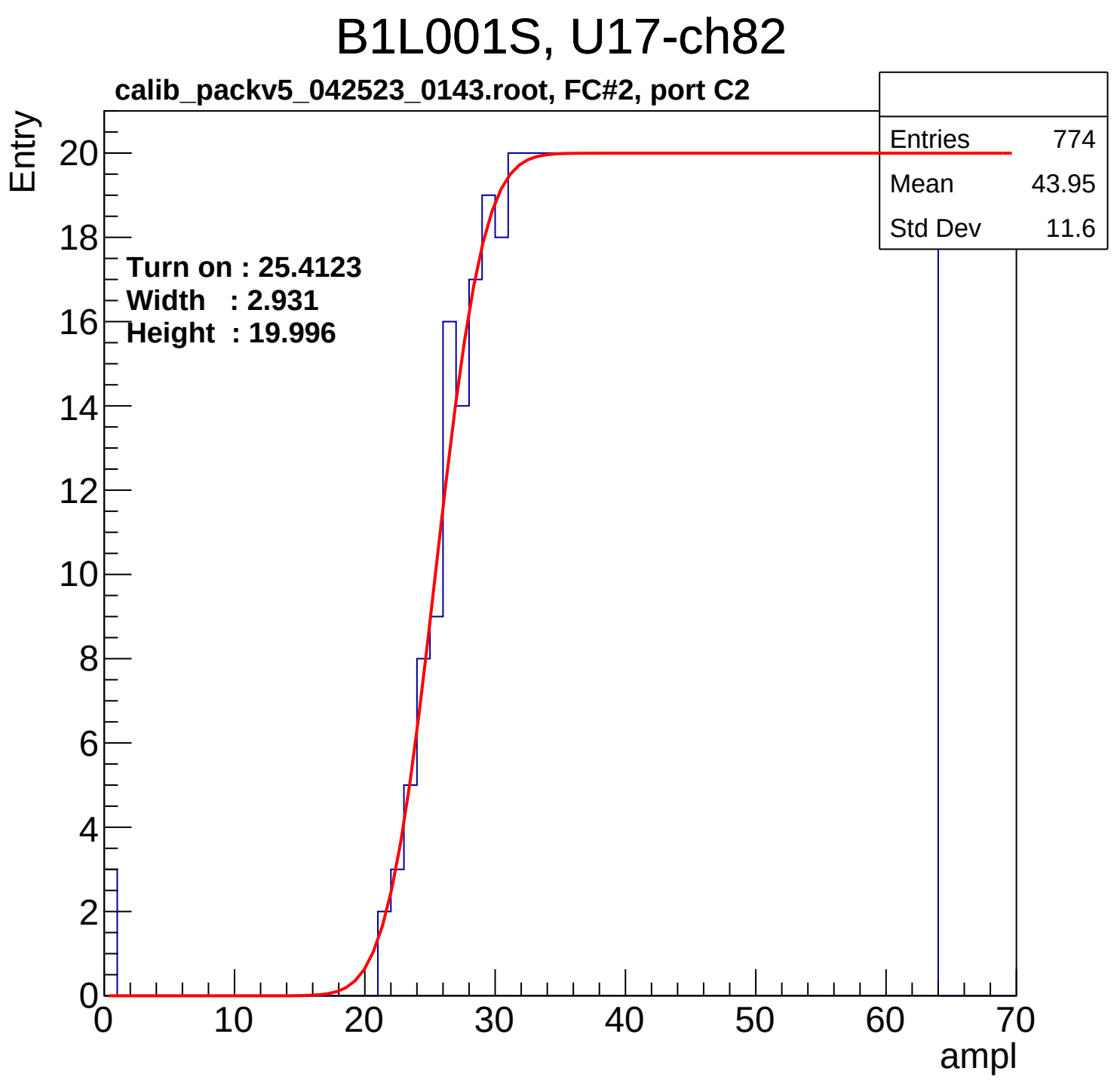
B1L001S, U17-ch82
calib_packv5_042523_0143.root, FC#2, port C2
Entries 774
Mean 43.95
Std Dev 11.6
Turn on : 25.4123
Width : 2.931
Height : 19.996
Entry
ampl
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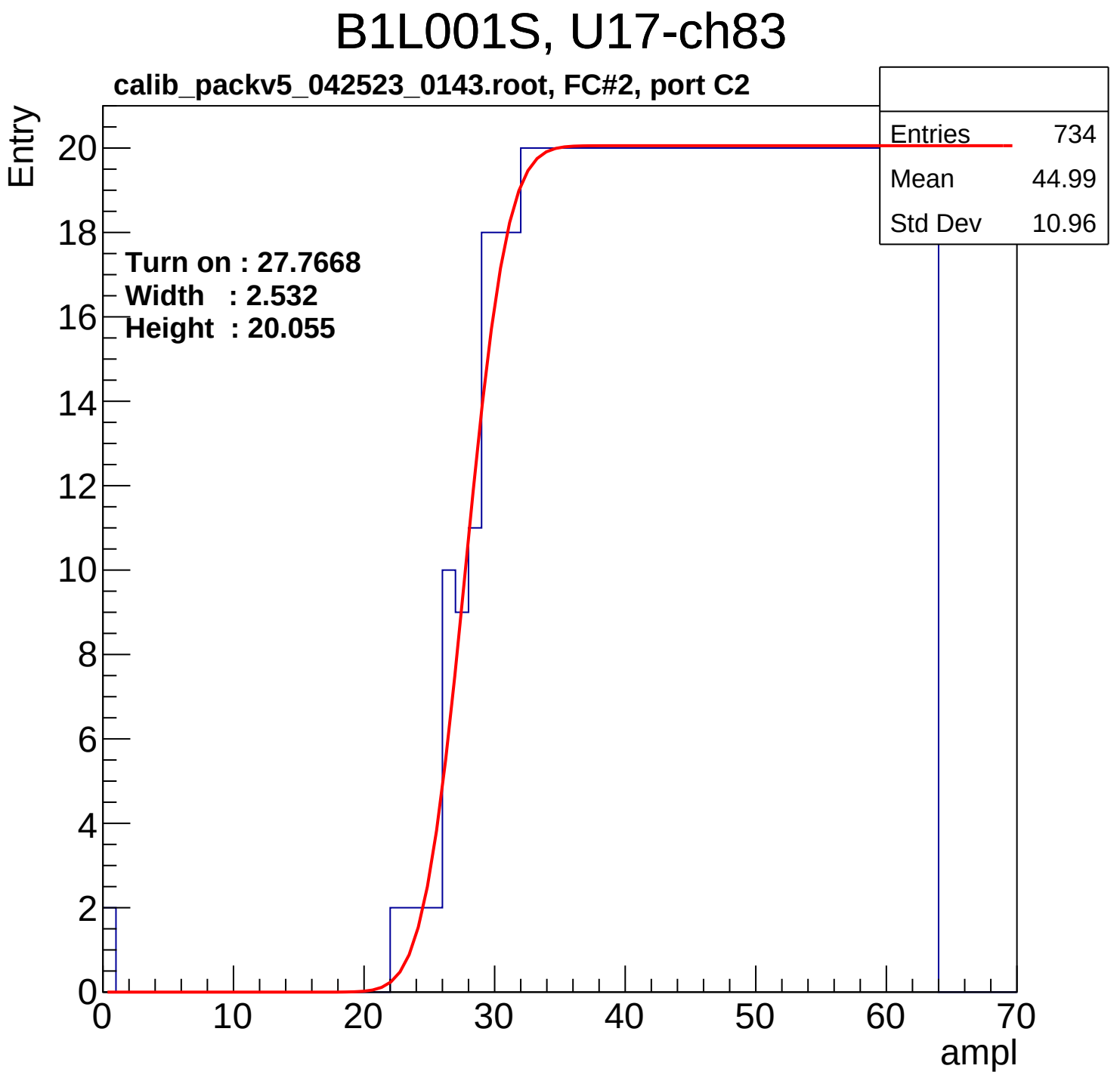
B1L001S, U17-ch83
calib_packv5_042523_0143.root, FC#2, port C2
Entries 734
Mean 44.99
Std Dev 10.96
Turn on : 27.7668
Width : 2.532
Height : 20.055
Entry
ampl
0
2
4
6
8
10
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18
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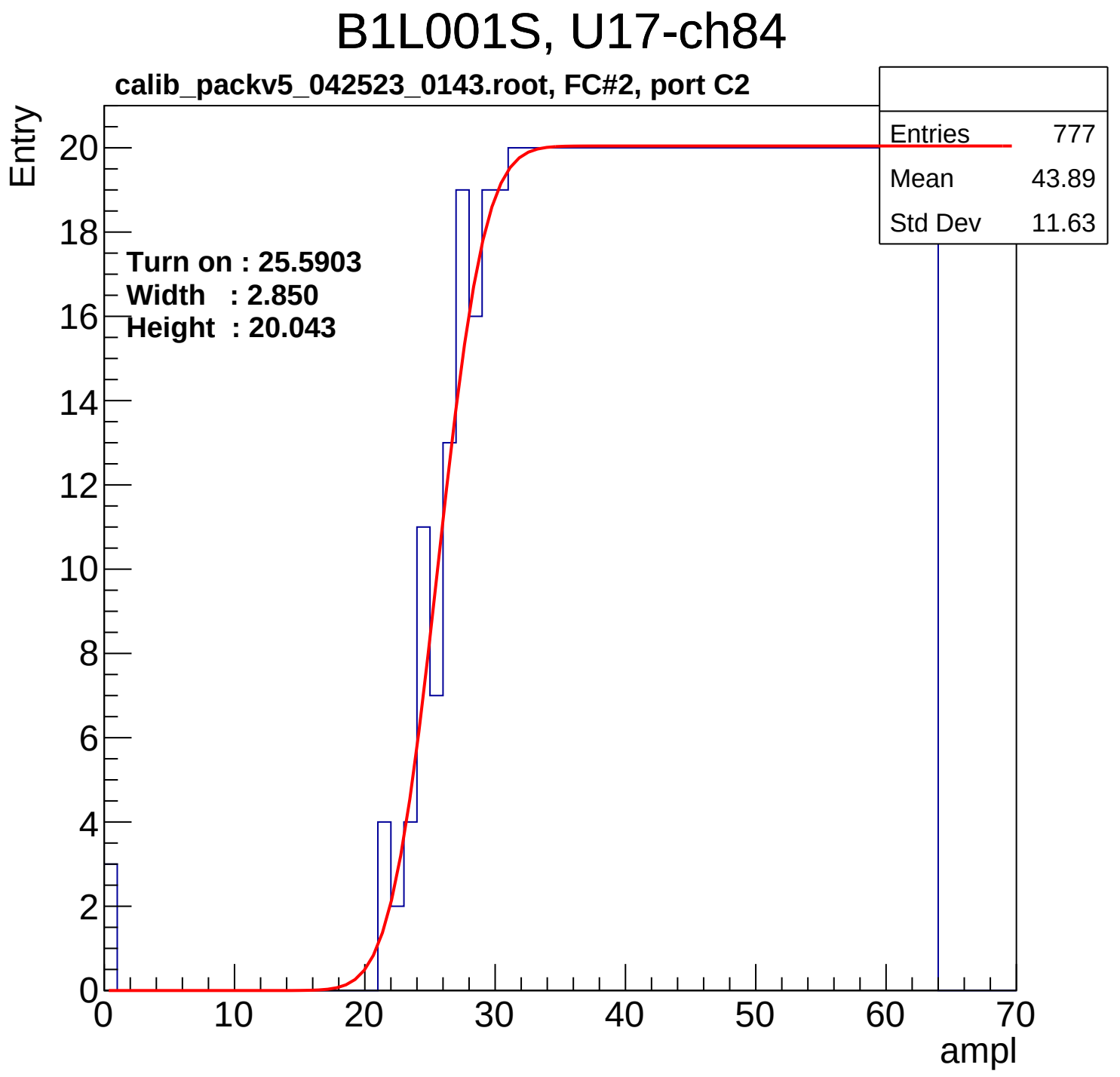
B1L001S, U17-ch84
calib_packv5_042523_0143.root, FC#2, port C2
Entries 777
Mean 43.89
Std Dev 11.63
Turn on : 25.5903
Width : 2.850
Height : 20.043
Entry
ampl
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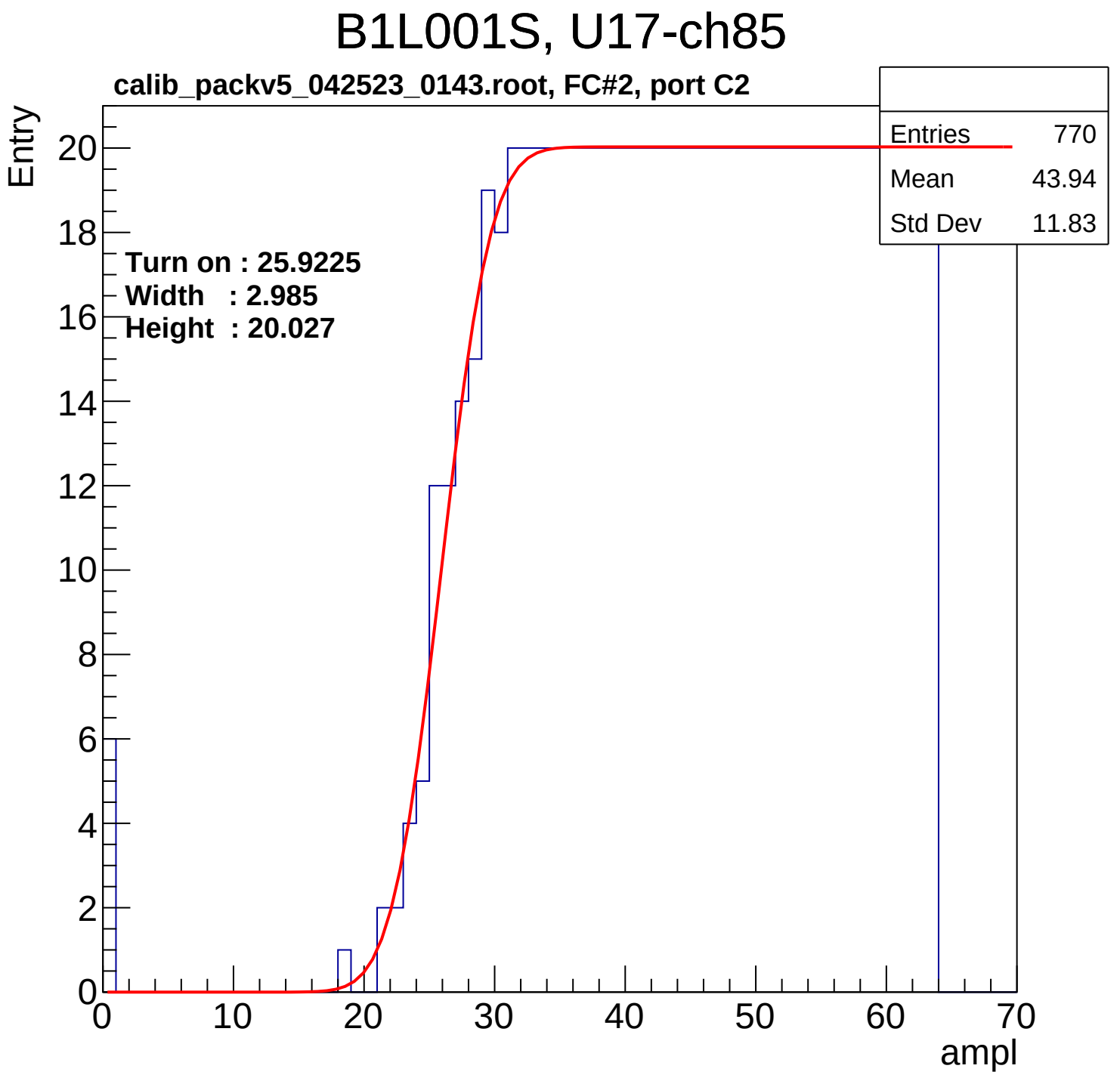
B1L001S, U17-ch85
calib_packv5_042523_0143.root, FC#2, port C2
Entries 770
Mean 43.94
Std Dev 11.83
Turn on : 25.9225
Width : 2.985
Height : 20.027
Entry
ampl
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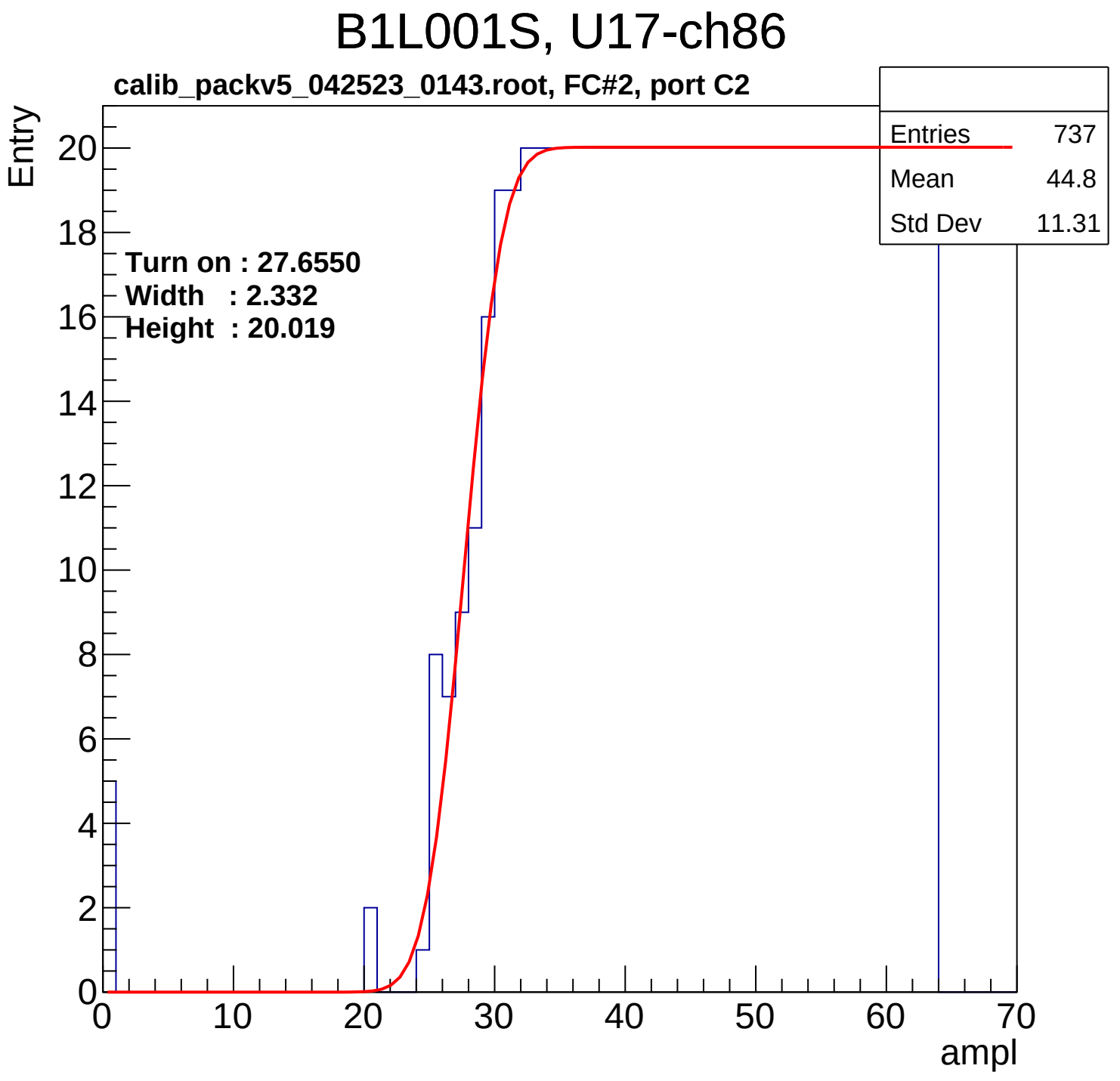
B1L001S, U17-ch86
calib_packv5_042523_0143.root, FC#2, port C2
Entries 737
Mean 44.8
Std Dev 11.31
Turn on : 27.6550
Width : 2.332
Height : 20.019
Entry
ampl
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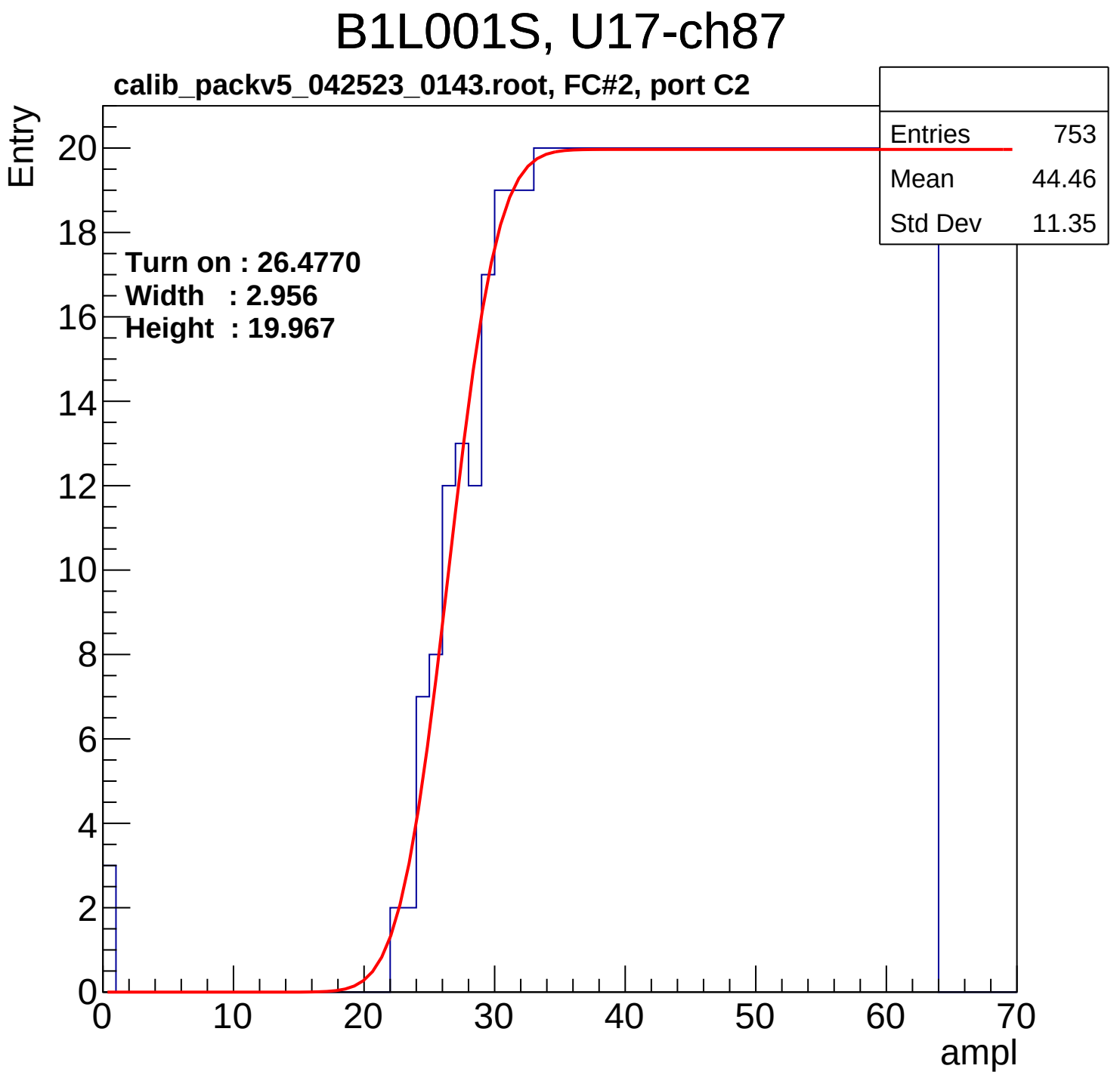
B1L001S, U17-ch87
calib_packv5_042523_0143.root, FC#2, port C2
Entries 753
Mean 44.46
Std Dev 11.35
Turn on : 26.4770
Width : 2.956
Height : 19.967
Entry
ampl
0
2
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6
8
10
12
14
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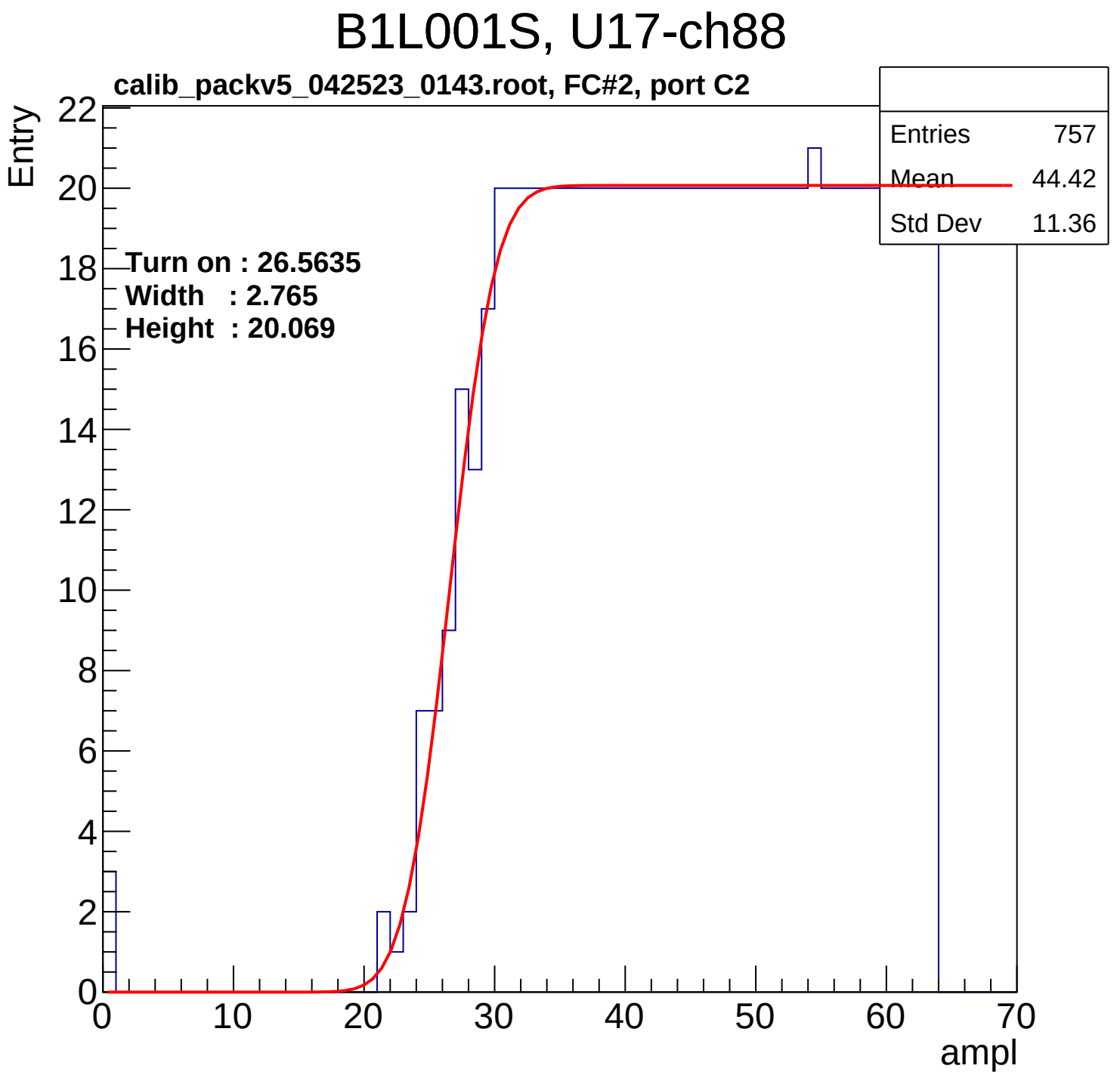
B1L001S, U17-ch88
calib_packv5_042523_0143.root, FC#2, port C2
Entries 757
Mean 44.42
Std Dev 11.36
Turn on : 26.5635
Width : 2.765
Height : 20.069
Entry
ampl
0
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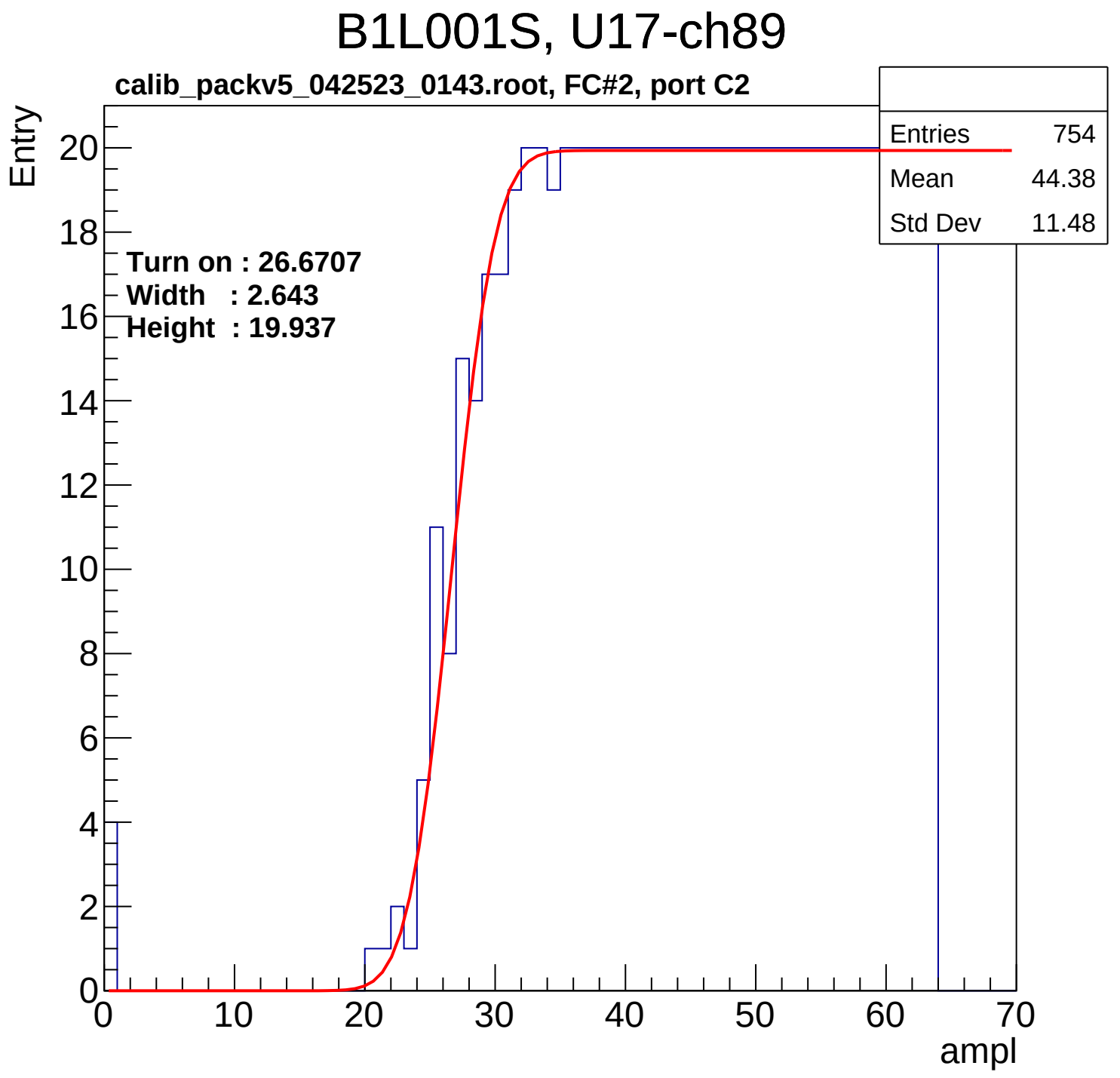
B1L001S, U17-ch89
calib_packv5_042523_0143.root, FC#2, port C2
Entries 754
Mean 44.38
Std Dev 11.48
Turn on : 26.6707
Width : 2.643
Height : 19.937
Entry
ampl
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6
8
10
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14
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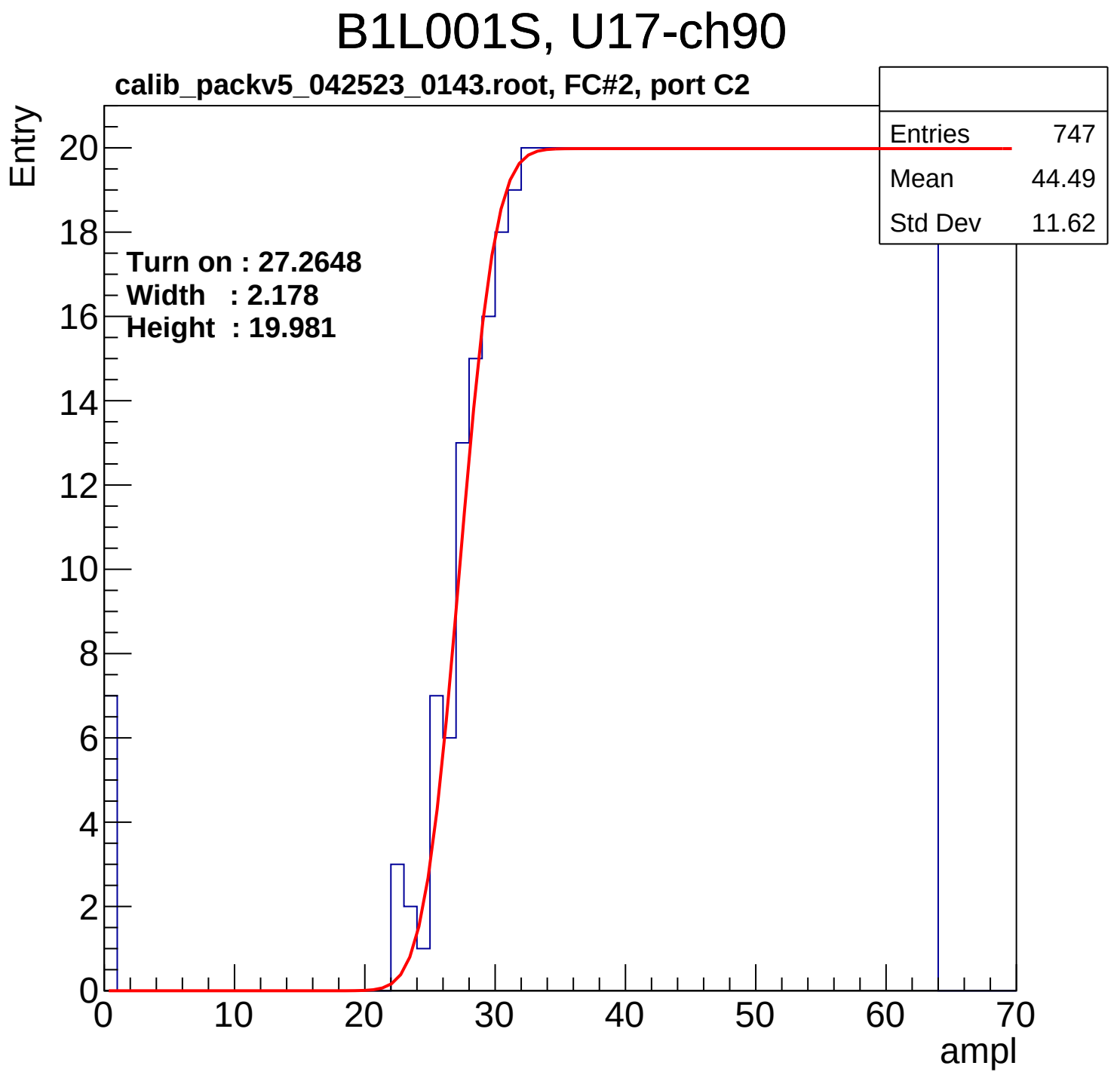
B1L001S, U17-ch90
calib_packv5_042523_0143.root, FC#2, port C2
Entries 747
Mean 44.49
Std Dev 11.62
Turn on : 27.2648
Width : 2.178
Height : 19.981
Entry
ampl
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6
8
10
12
14
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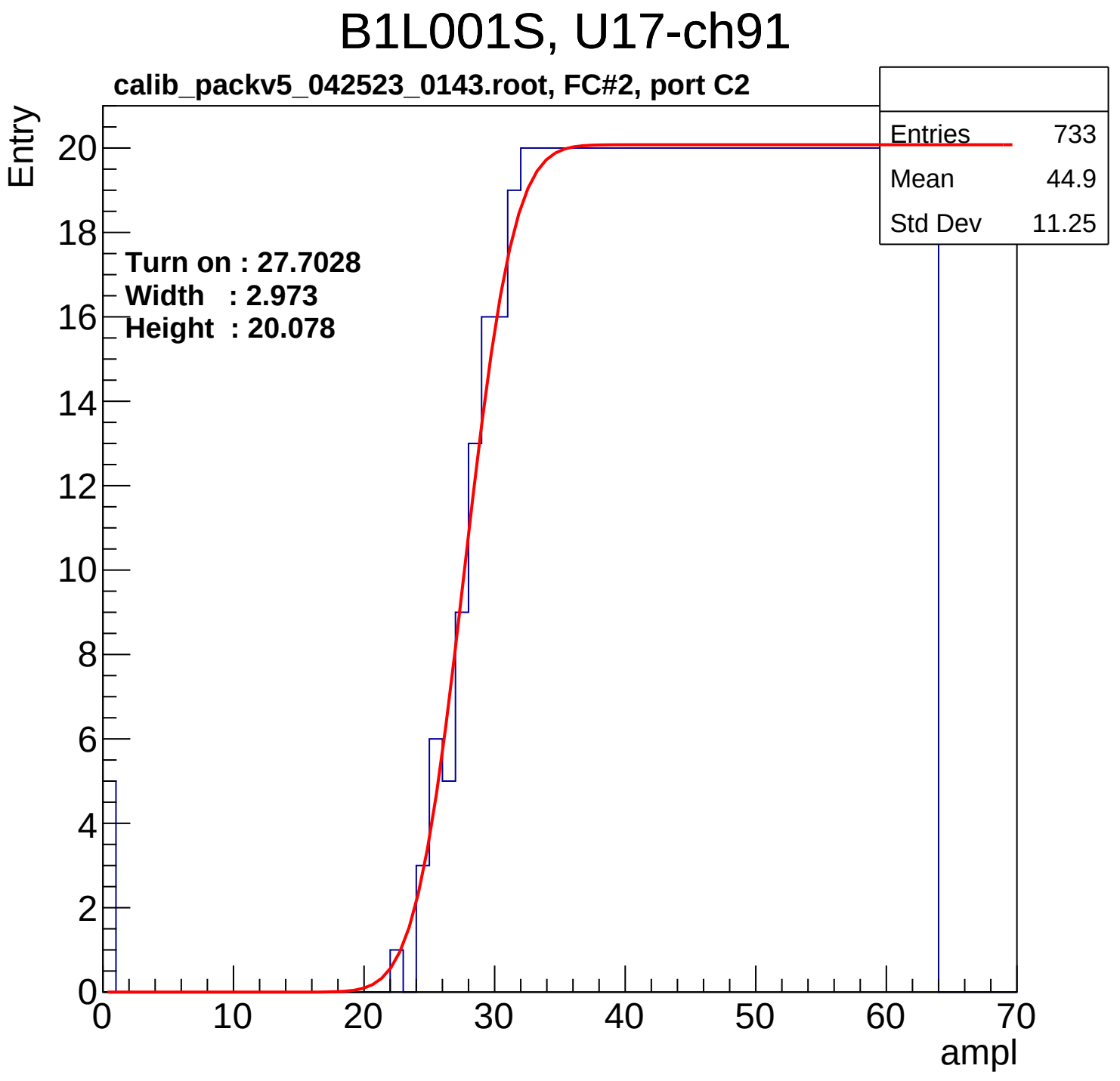
B1L001S, U17-ch91
calib_packv5_042523_0143.root, FC#2, port C2
Entries 733
Mean 44.9
Std Dev 11.25
Turn on : 27.7028
Width : 2.973
Height : 20.078
Entry
ampl
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2
4
6
8
10
12
14
16
18
20
0
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60
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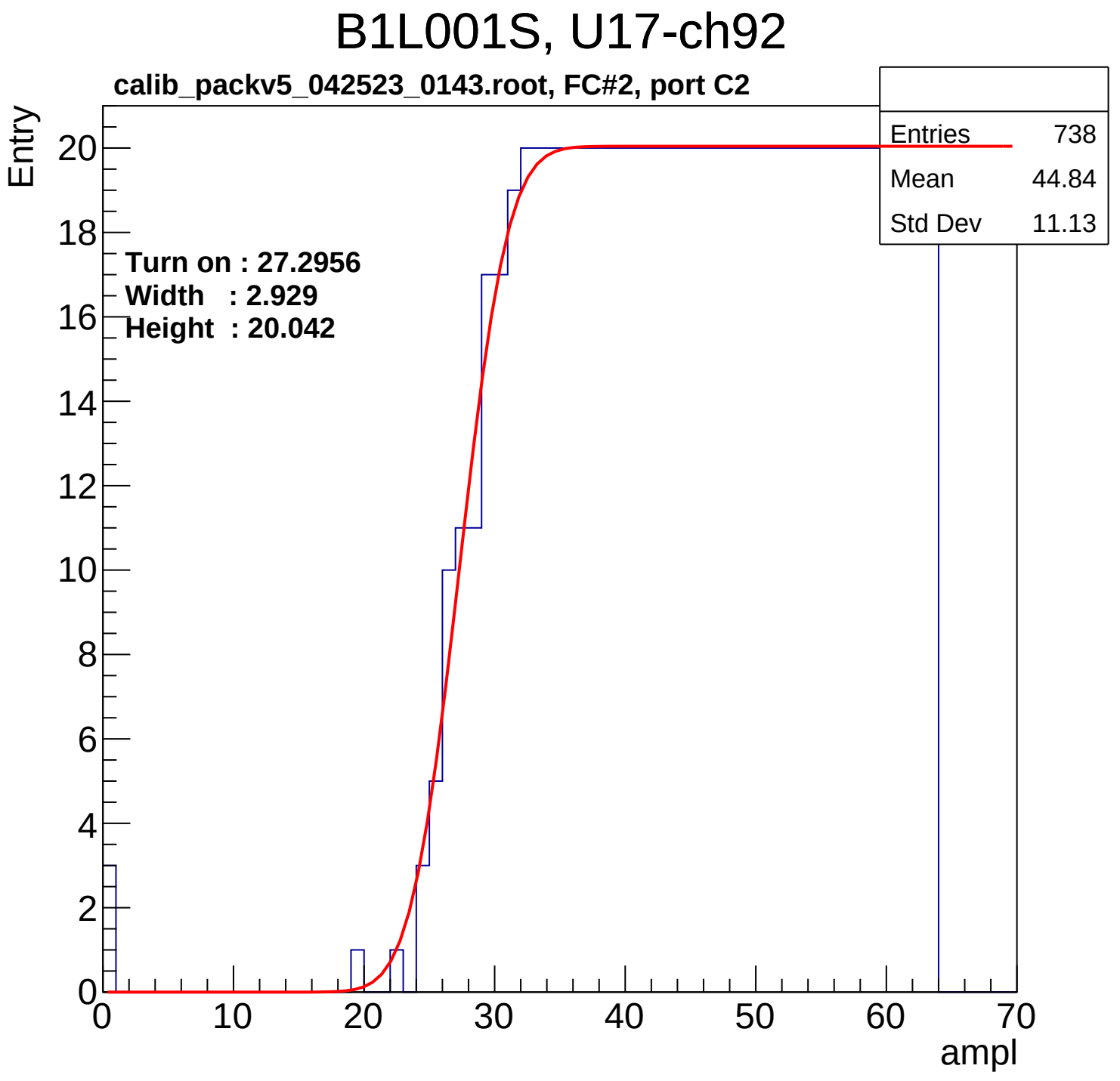
B1L001S, U17-ch92
calib_packv5_042523_0143.root, FC#2, port C2
Entries 738
Mean 44.84
Std Dev 11.13
Turn on : 27.2956
Width : 2.929
Height : 20.042
Entry
ampl
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6
8
10
12
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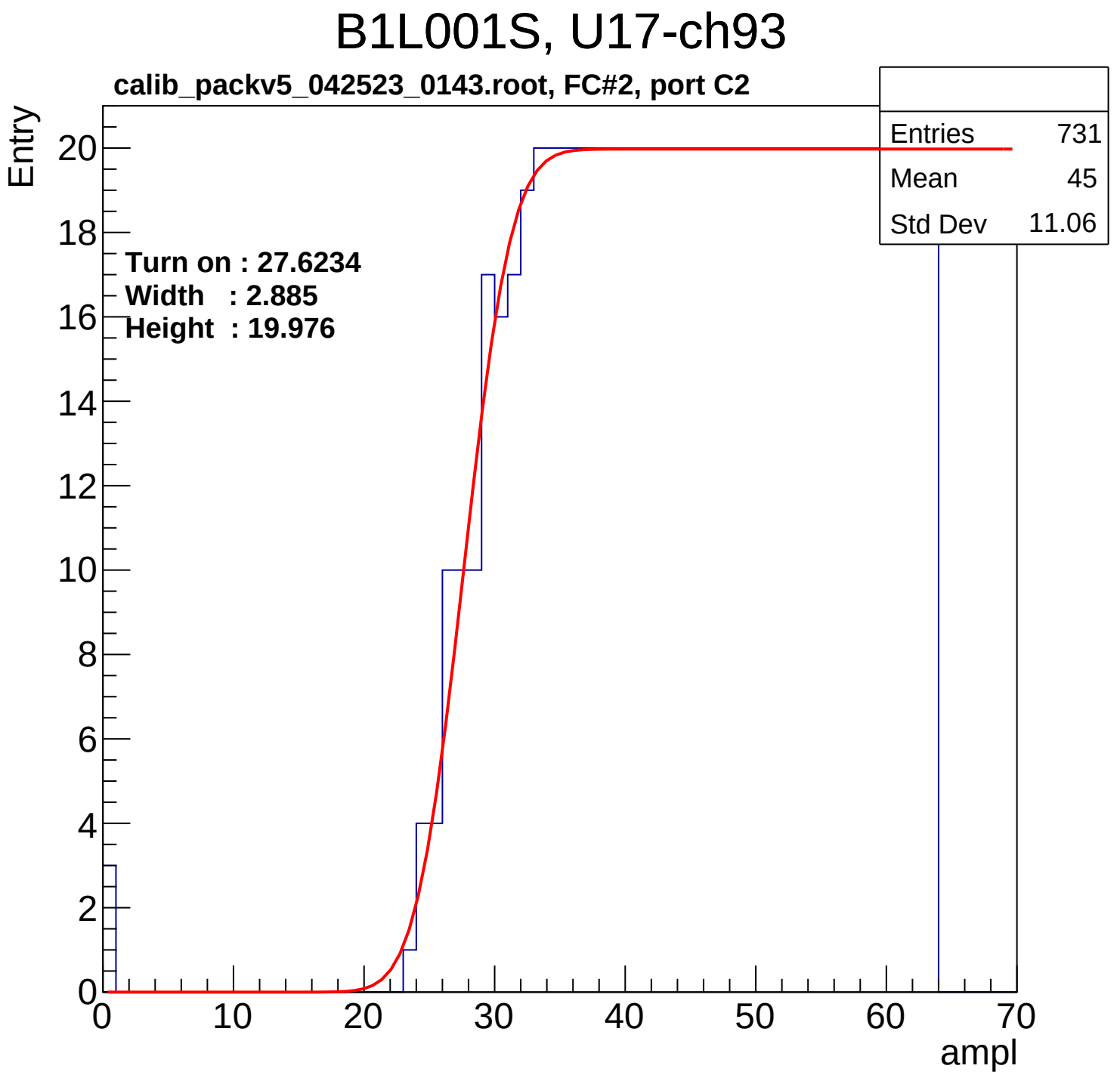
B1L001S, U17-ch93
calib_packv5_042523_0143.root, FC#2, port C2
Entries 731
Mean 45
Std Dev 11.06
Turn on : 27.6234
Width : 2.885
Height : 19.976
Entry
ampl
0
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6
8
10
12
14
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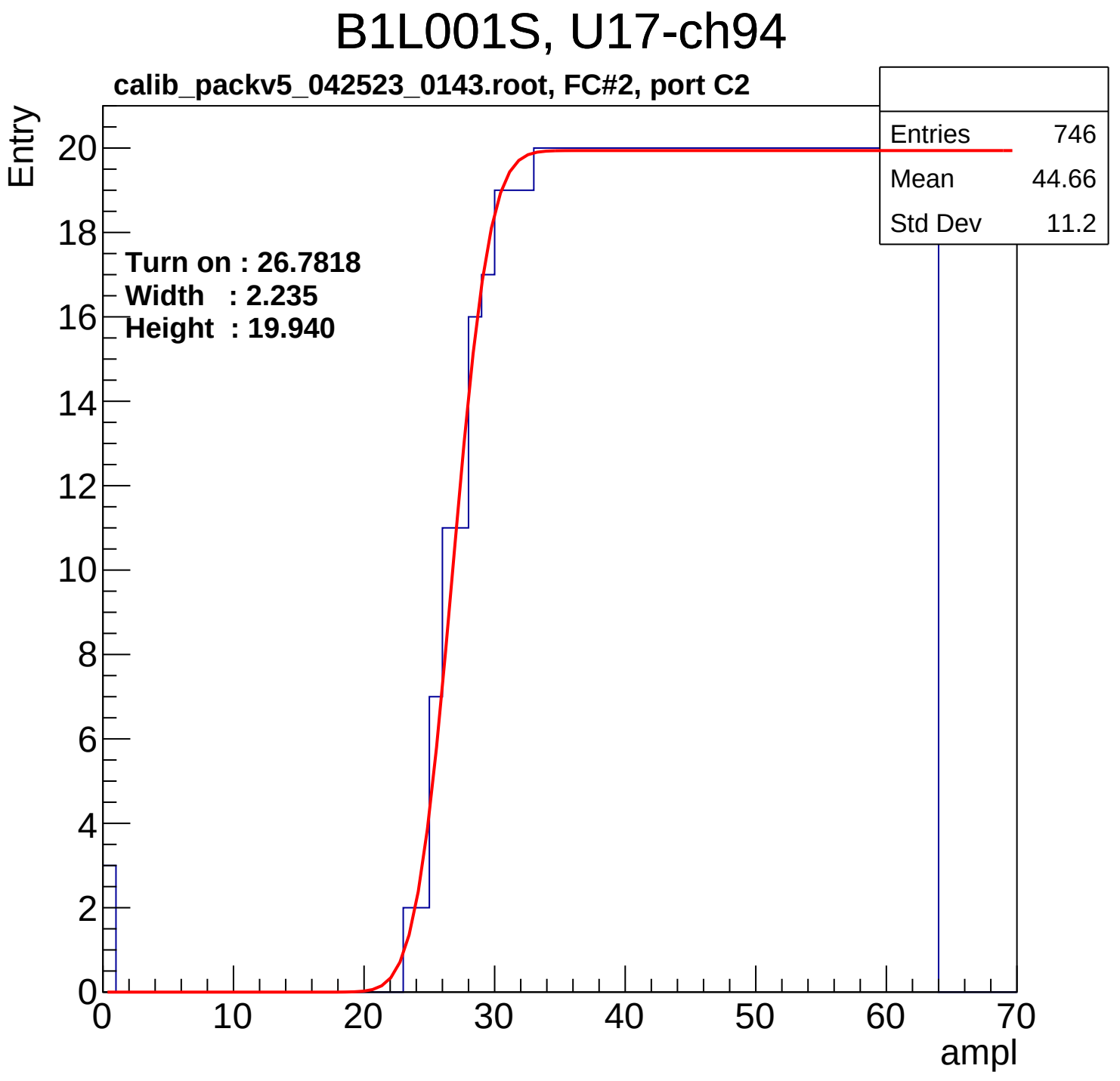
B1L001S, U17-ch94
calib_packv5_042523_0143.root, FC#2, port C2
Entries 746
Mean 44.66
Std Dev 11.2
Turn on : 26.7818
Width : 2.235
Height : 19.940
Entry
ampl
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6
8
10
12
14
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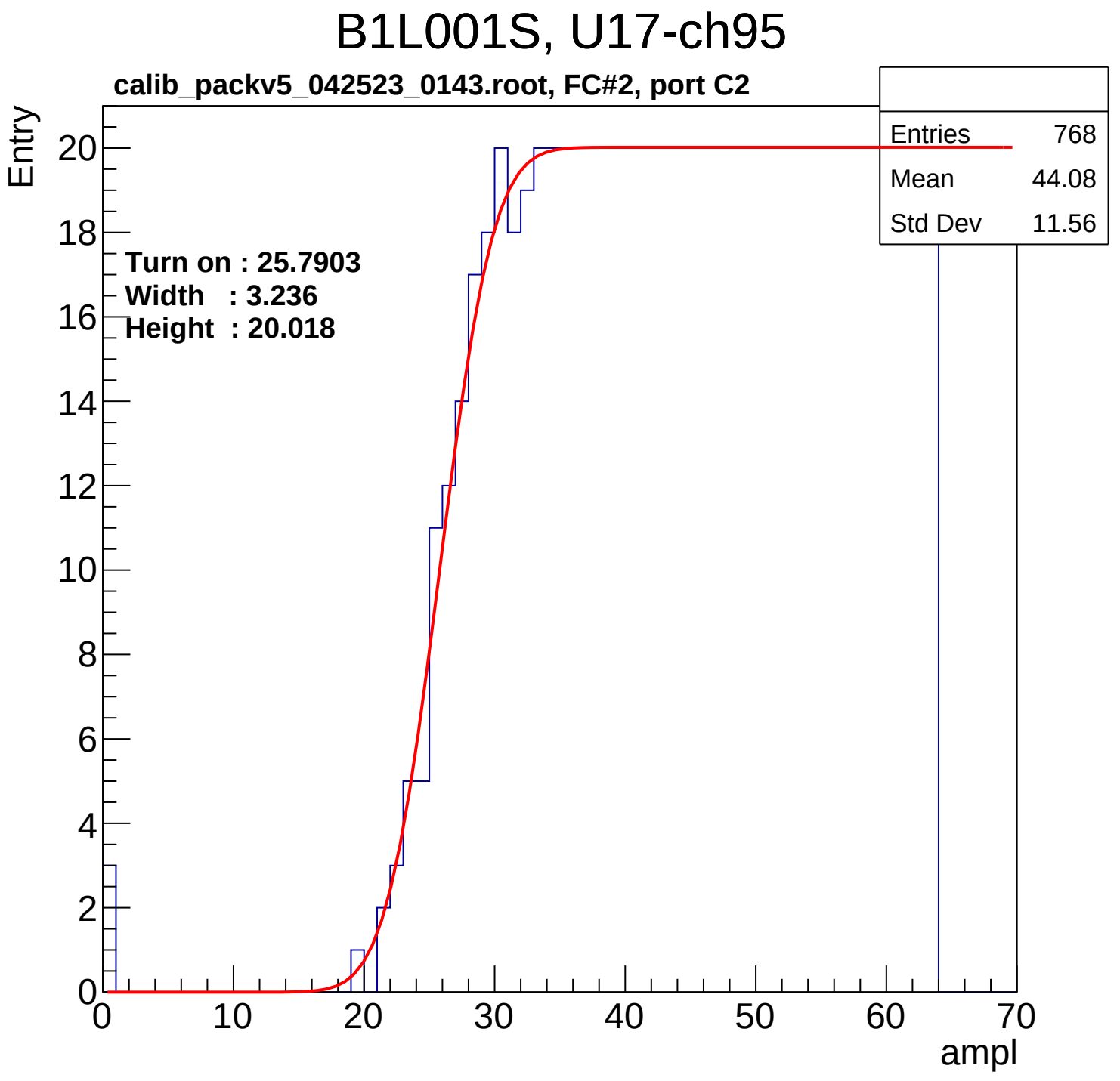
B1L001S, U17-ch95
calib_packv5_042523_0143.root, FC#2, port C2
Entries 768
Mean 44.08
Std Dev 11.56
Turn on : 25.7903
Width : 3.236
Height : 20.018
Entry
ampl
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6
8
10
12
14
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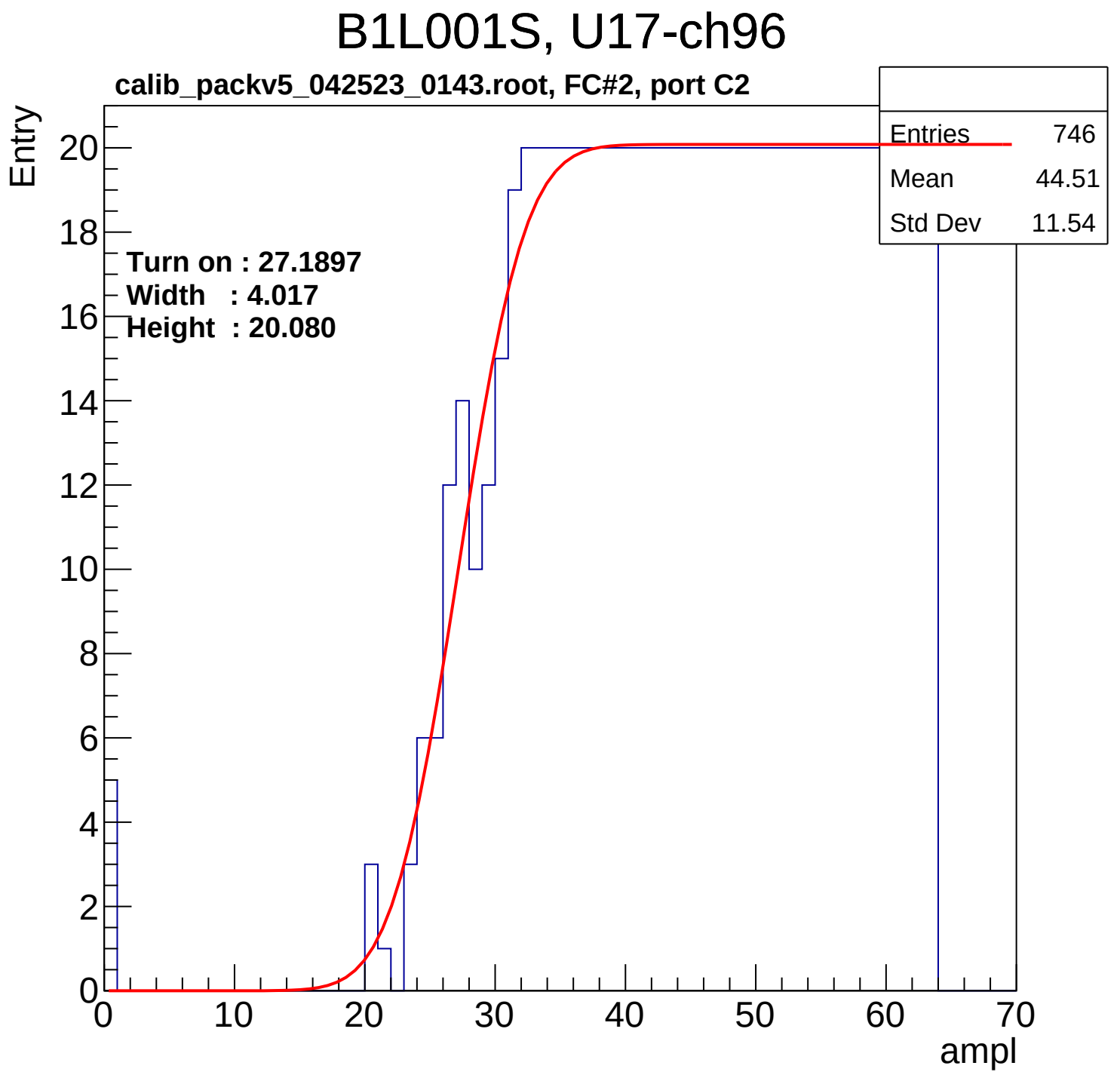
B1L001S, U17-ch96
calib_packv5_042523_0143.root, FC#2, port C2
Entries 746
Mean 44.51
Std Dev 11.54
Turn on : 27.1897
Width : 4.017
Height : 20.080
Entry
ampl
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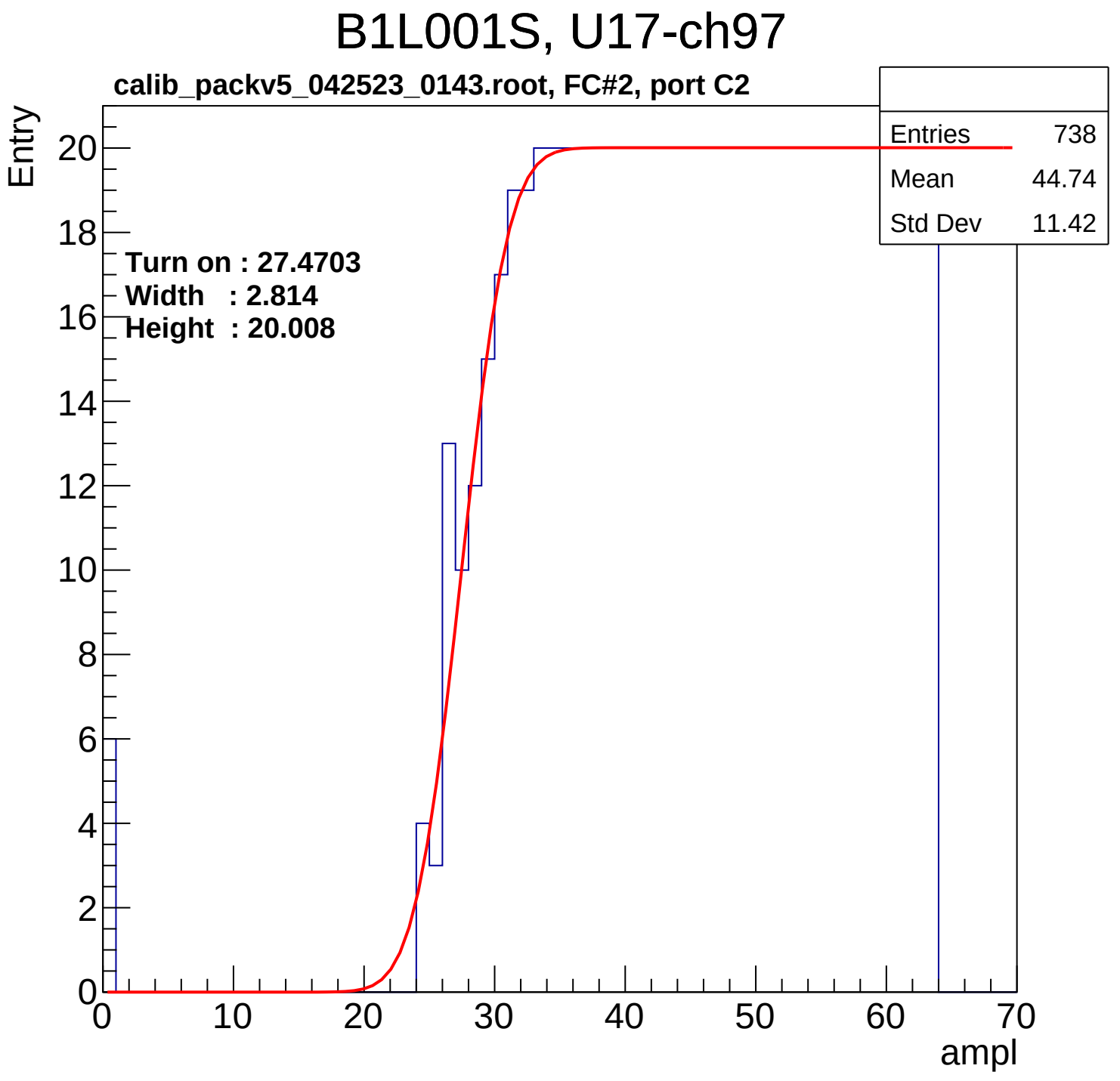
B1L001S, U17-ch97
calib_packv5_042523_0143.root, FC#2, port C2
Entries 738
Mean 44.74
Std Dev 11.42
Turn on : 27.4703
Width : 2.814
Height : 20.008
Entry
ampl
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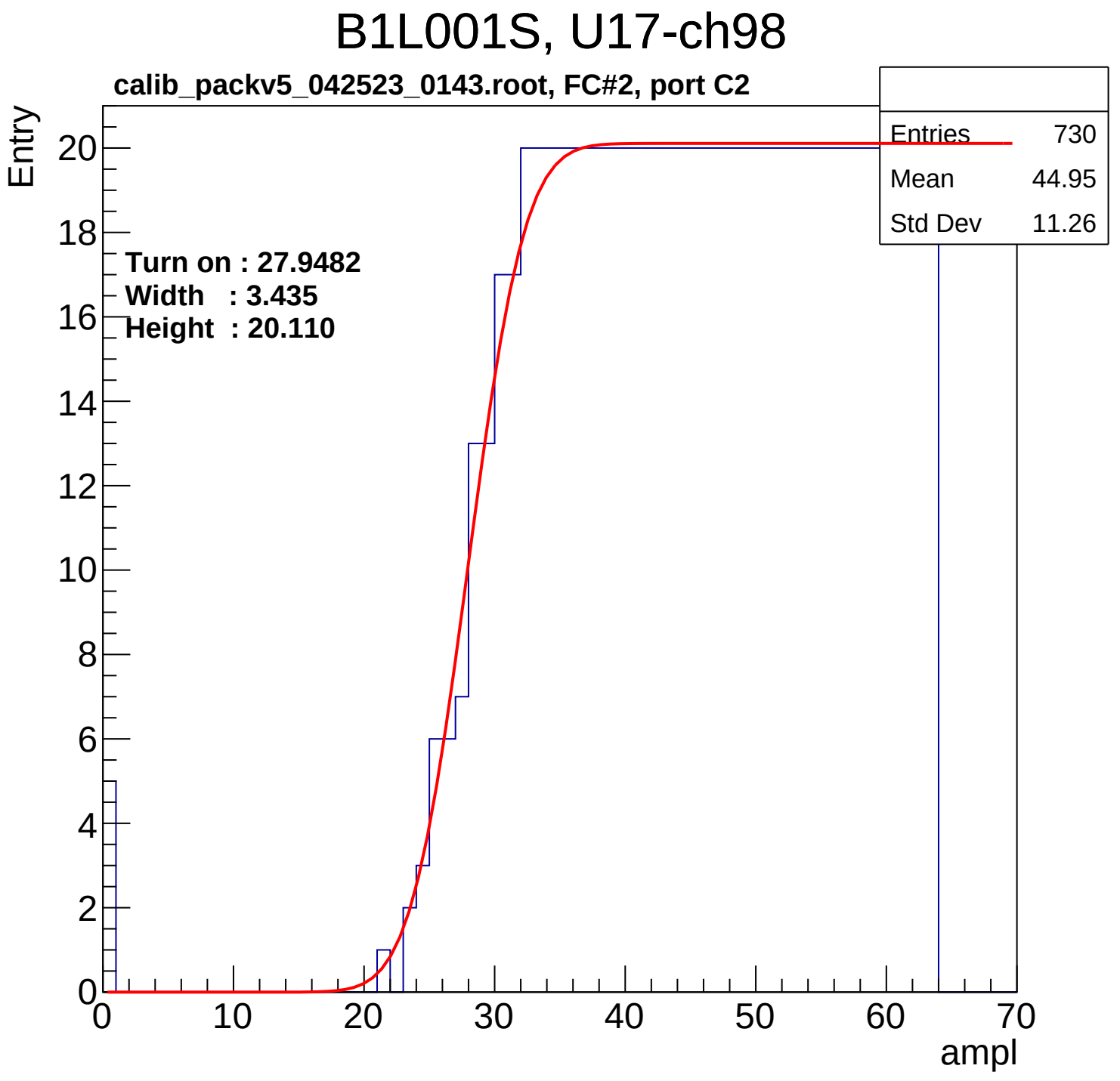
B1L001S, U17-ch98
calib_packv5_042523_0143.root, FC#2, port C2
Entries 730
Mean 44.95
Std Dev 11.26
Turn on : 27.9482
Width : 3.435
Height : 20.110
Entry
ampl
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12
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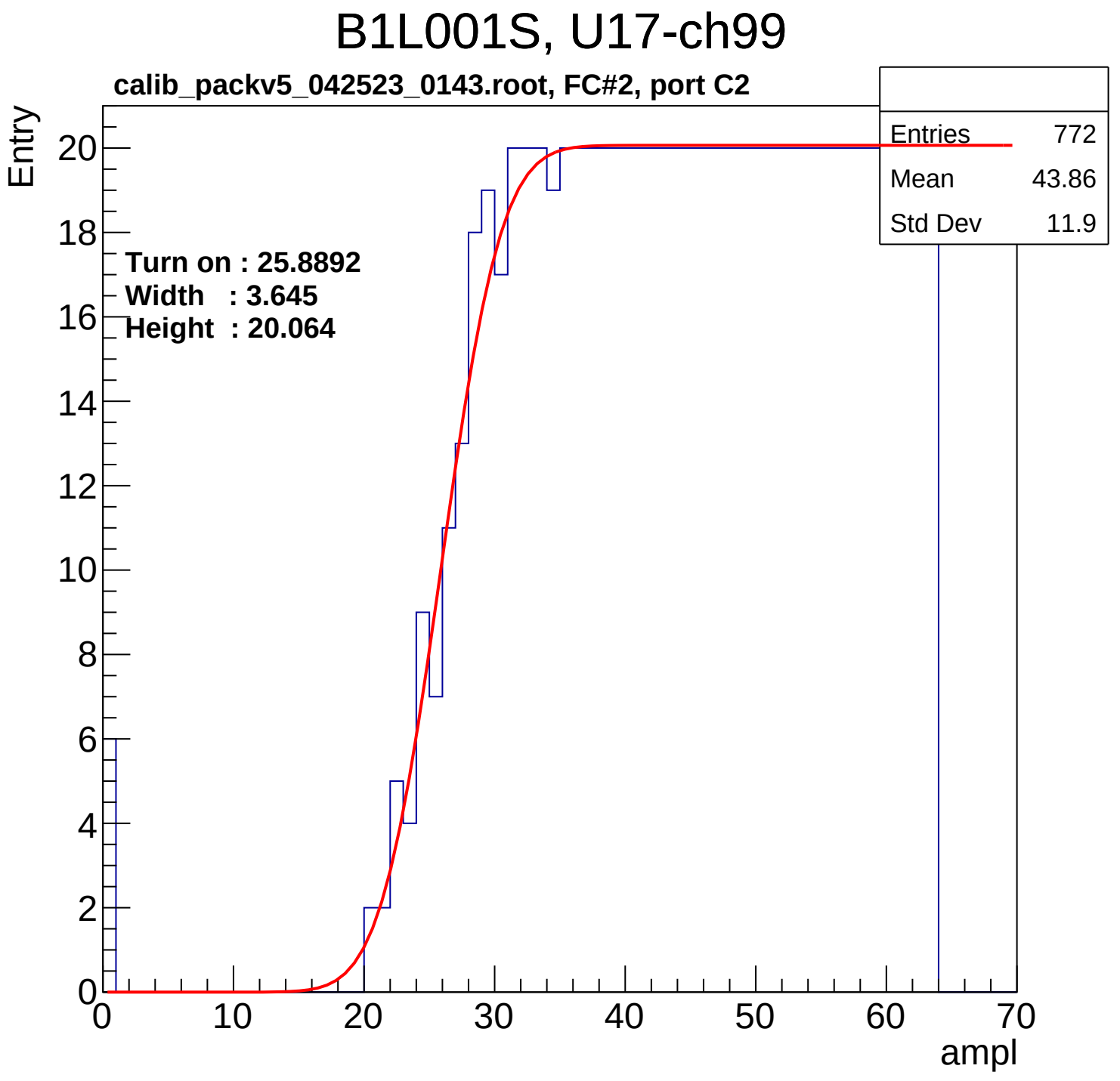
B1L001S, U17-ch99
calib_packv5_042523_0143.root, FC#2, port C2
Entries 772
Mean 43.86
Std Dev 11.9
Turn on : 25.8892
Width : 3.645
Height : 20.064
Entry
ampl
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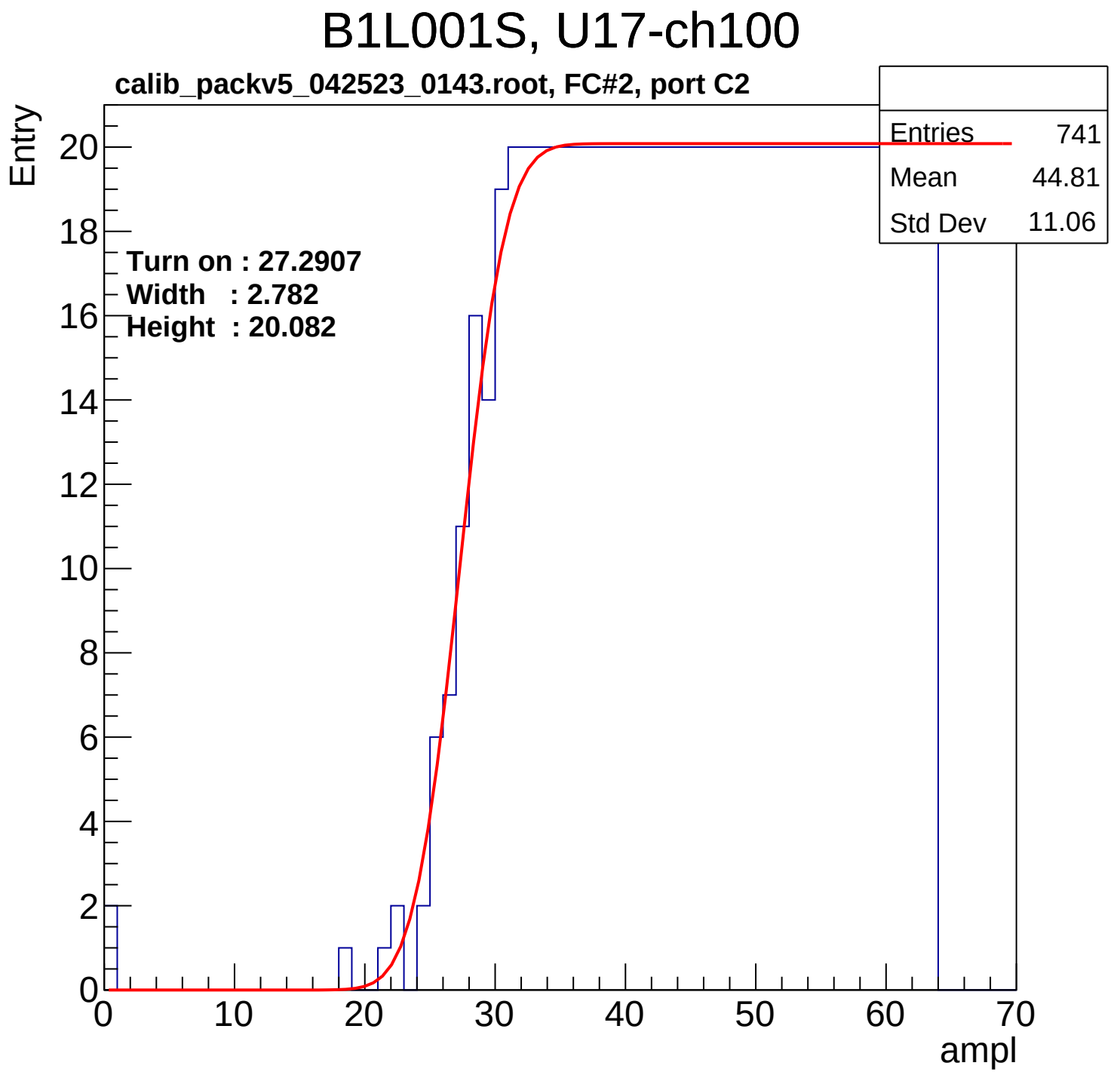
B1L001S, U17-ch100
calib_packv5_042523_0143.root, FC#2, port C2
Entries 741
Mean 44.81
Std Dev 11.06
Turn on : 27.2907
Width : 2.782
Height : 20.082
Entry
ampl
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6
8
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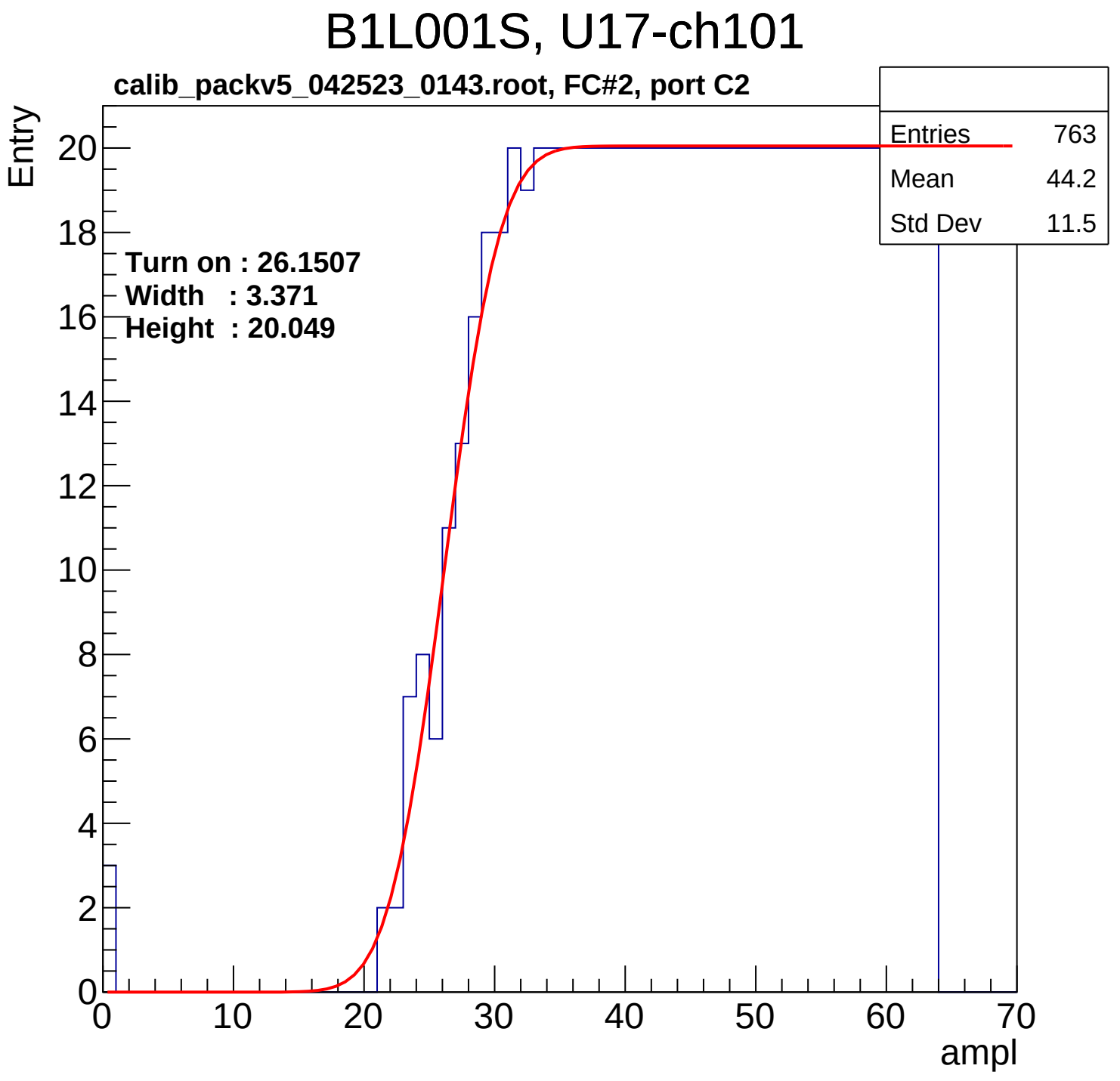
B1L001S, U17-ch101
calib_packv5_042523_0143.root, FC#2, port C2
Entries 763
Mean 44.2
Std Dev 11.5
Turn on : 26.1507
Width : 3.371
Height : 20.049
Entry
ampl
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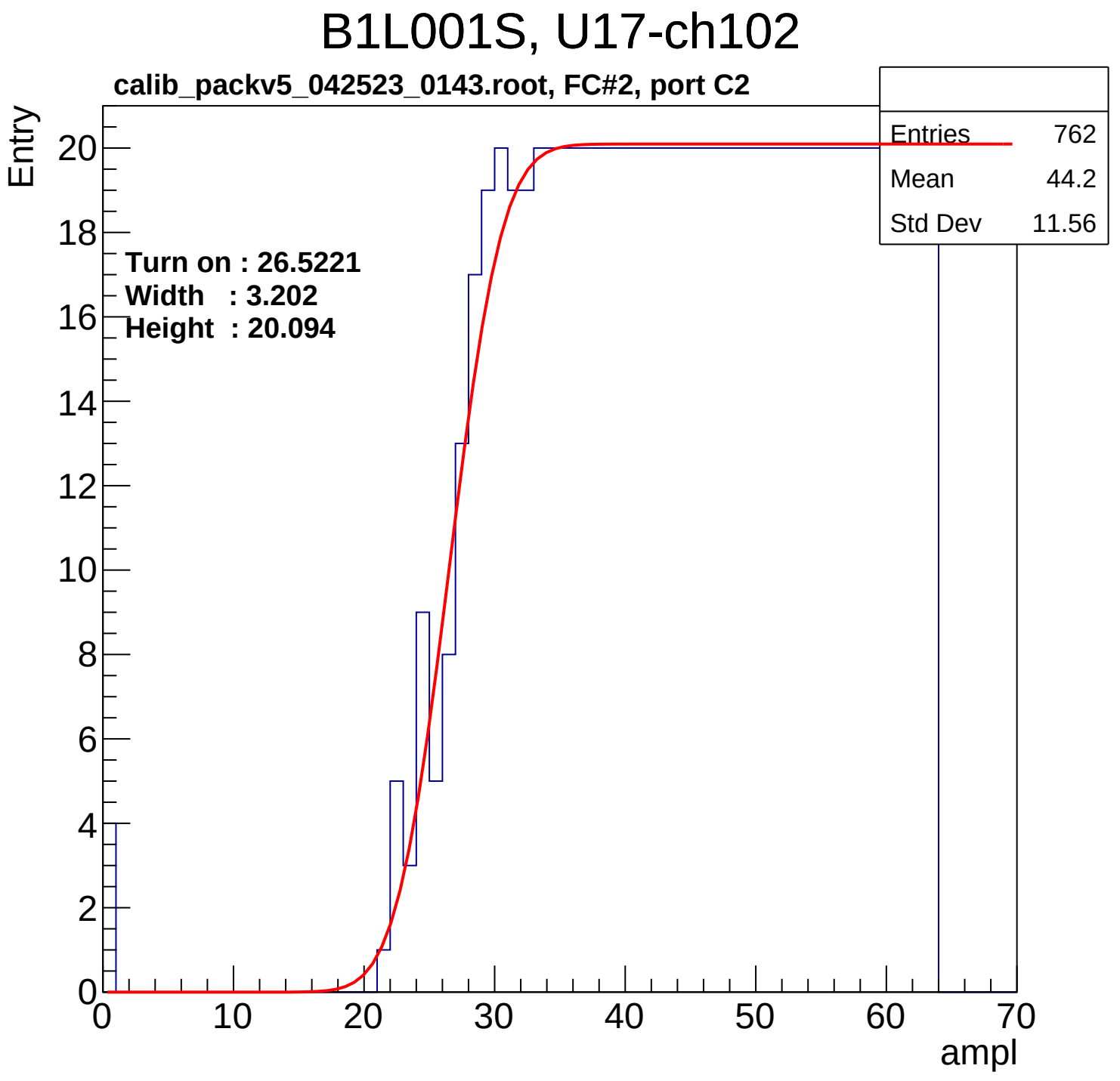
B1L001S, U17-ch102
calib_packv5_042523_0143.root, FC#2, port C2
Entries 762
Mean 44.2
Std Dev 11.56
Turn on : 26.5221
Width : 3.202
Height : 20.094
Entry
ampl
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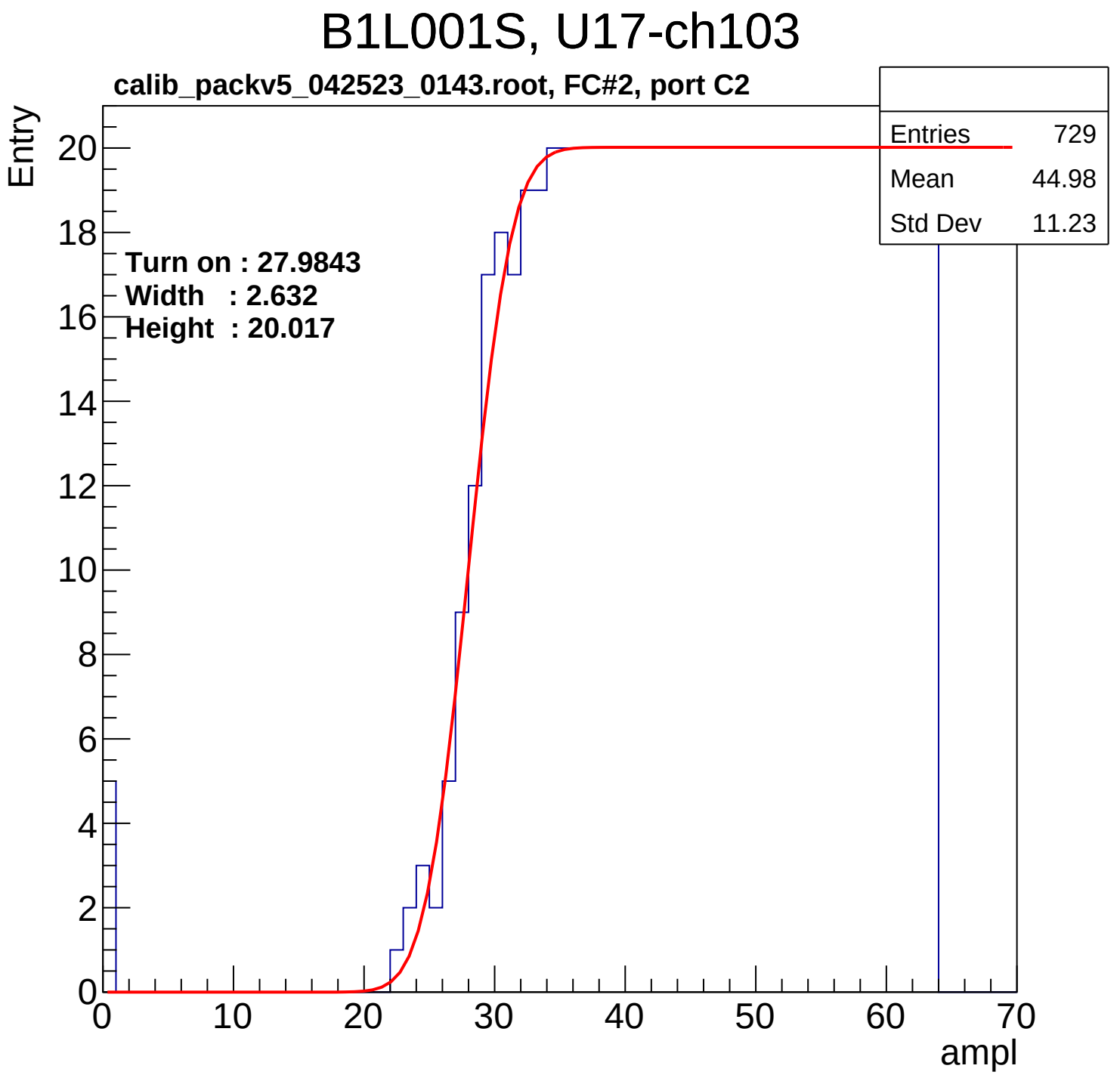
B1L001S, U17-ch103
calib_packv5_042523_0143.root, FC#2, port C2
Entries 729
Mean 44.98
Std Dev 11.23
Turn on : 27.9843
Width : 2.632
Height : 20.017
Entry
ampl
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6
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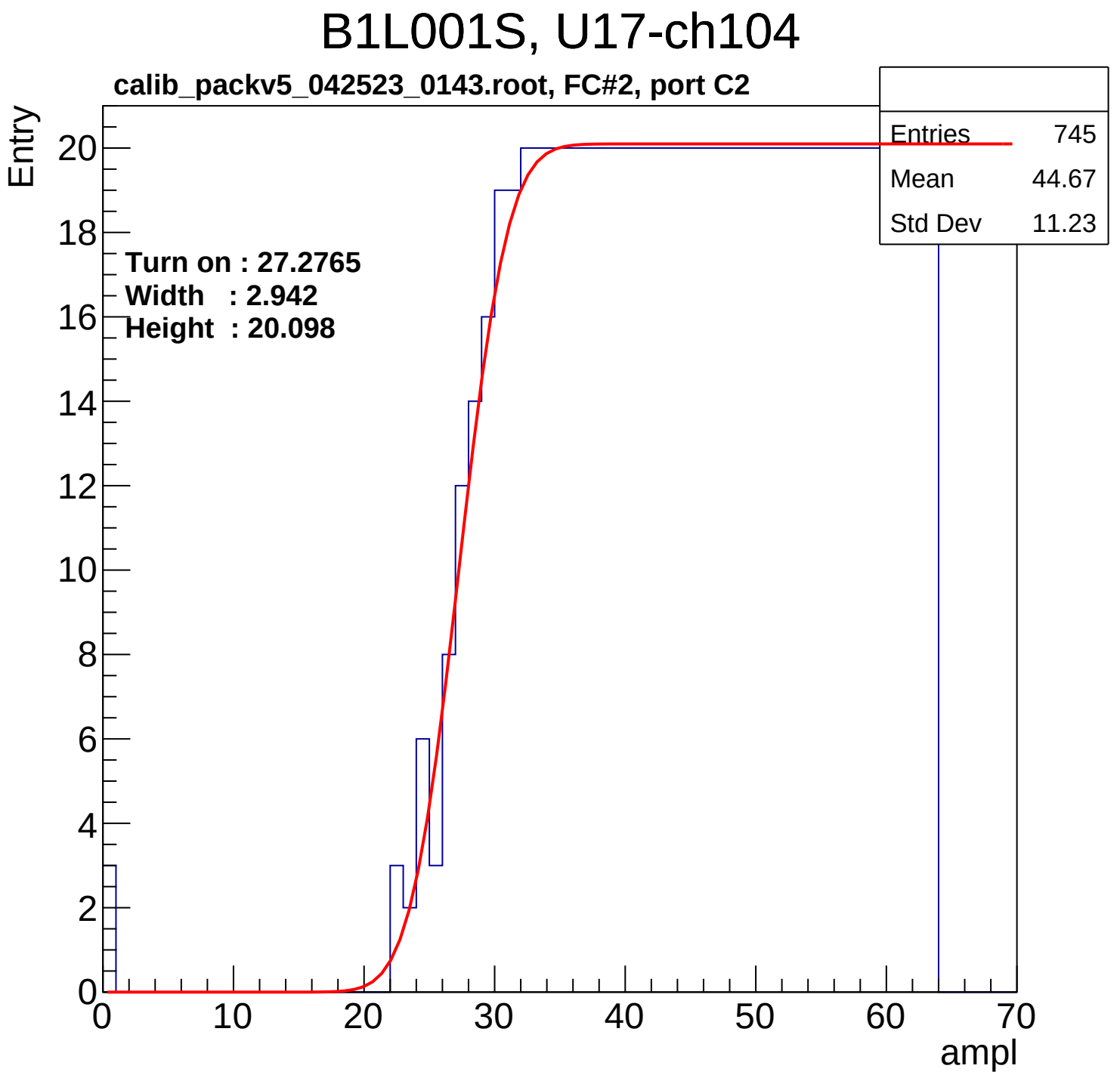
B1L001S, U17-ch104
calib_packv5_042523_0143.root, FC#2, port C2
Entries 745
Mean 44.67
Std Dev 11.23
Turn on : 27.2765
Width : 2.942
Height : 20.098
Entry
ampl
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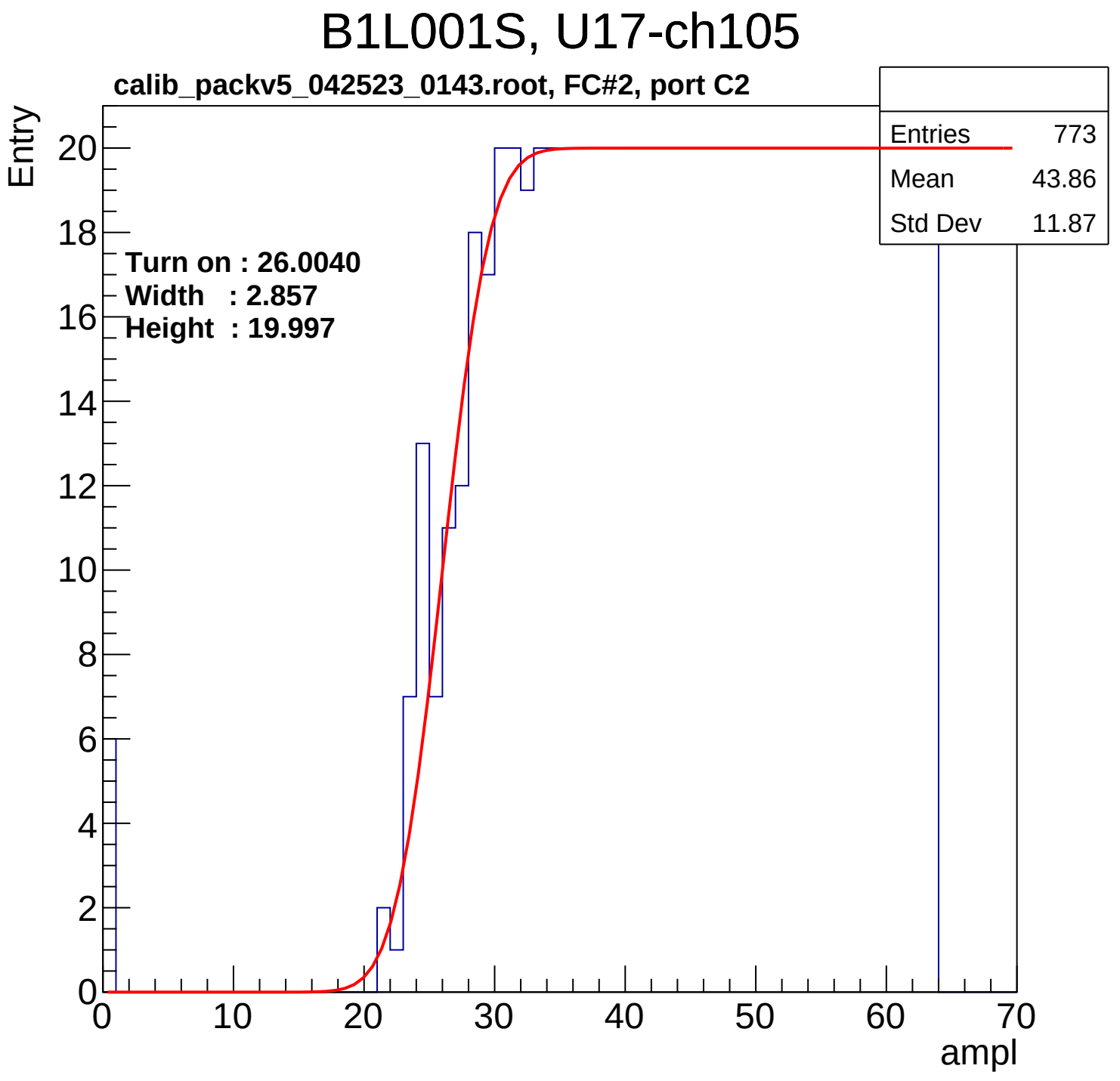
B1L001S, U17-ch105
calib_packv5_042523_0143.root, FC#2, port C2
Entries 773
Mean 43.86
Std Dev 11.87
Turn on : 26.0040
Width : 2.857
Height : 19.997
Entry
ampl
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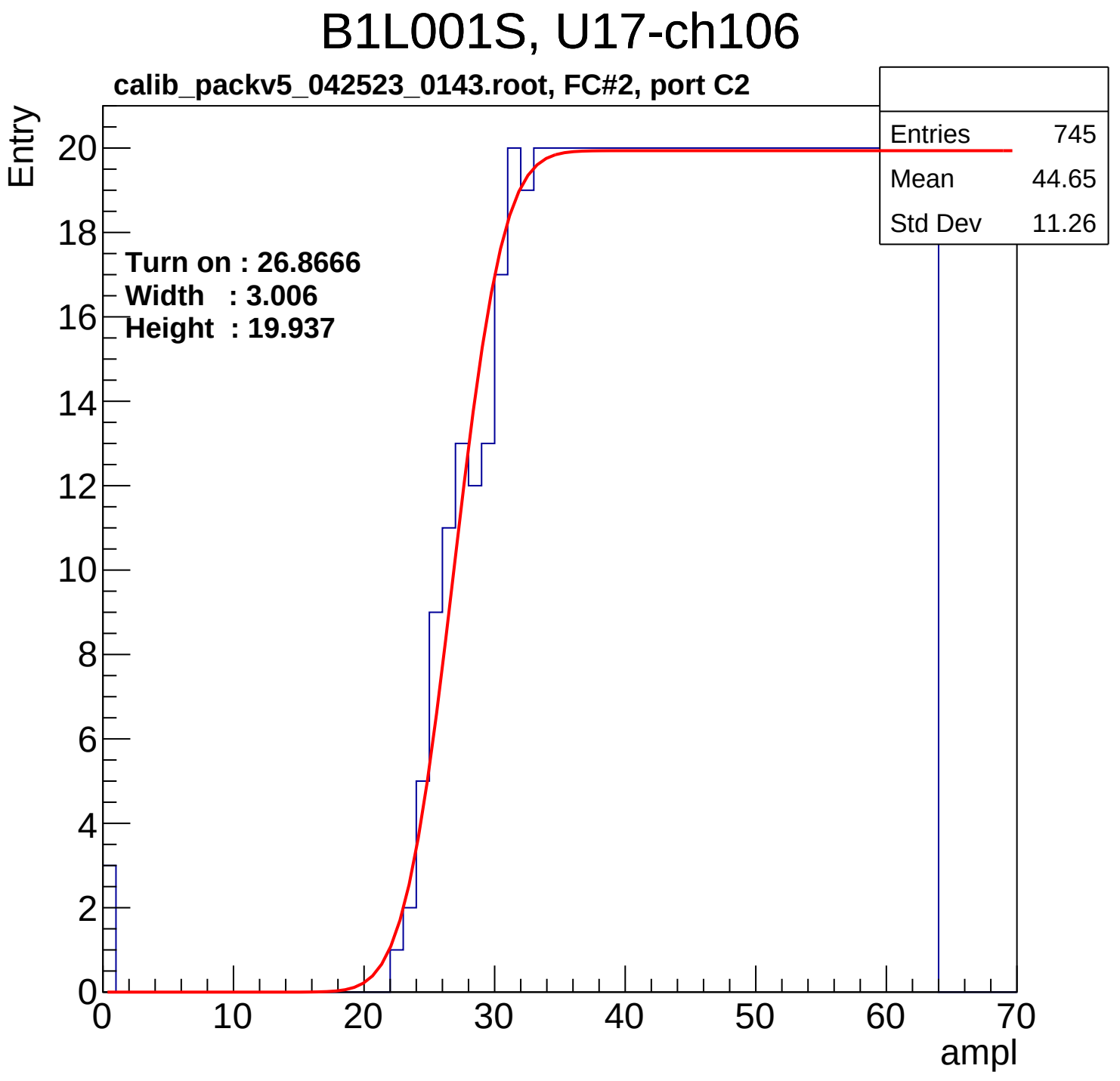
B1L001S, U17-ch106
calib_packv5_042523_0143.root, FC#2, port C2
Entries 745
Mean 44.65
Std Dev 11.26
Turn on : 26.8666
Width : 3.006
Height : 19.937
Entry
ampl
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6
8
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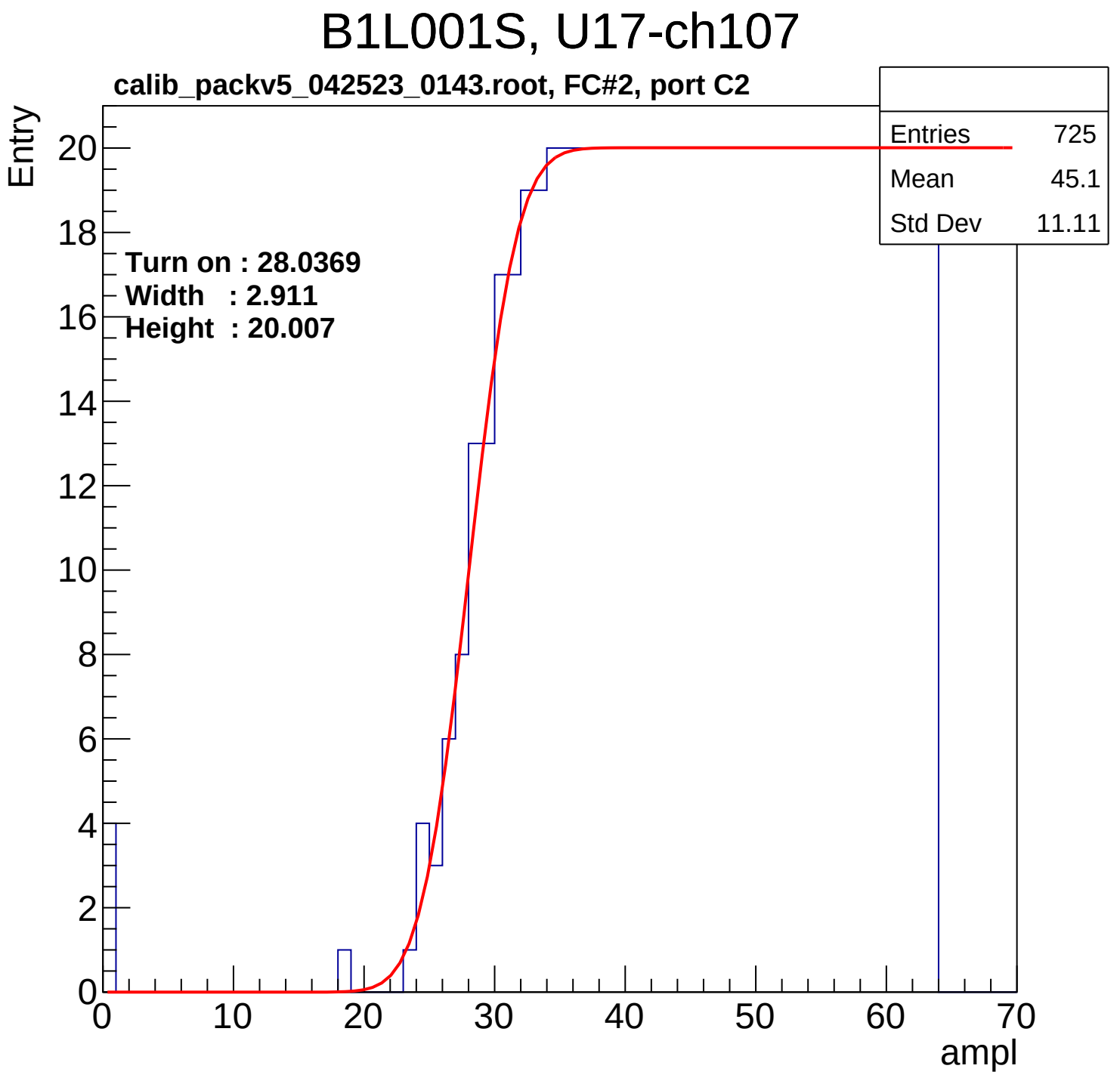
B1L001S, U17-ch107
calib_packv5_042523_0143.root, FC#2, port C2
Entries 725
Mean 45.1
Std Dev 11.11
Turn on : 28.0369
Width : 2.911
Height : 20.007
Entry
ampl
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6
8
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14
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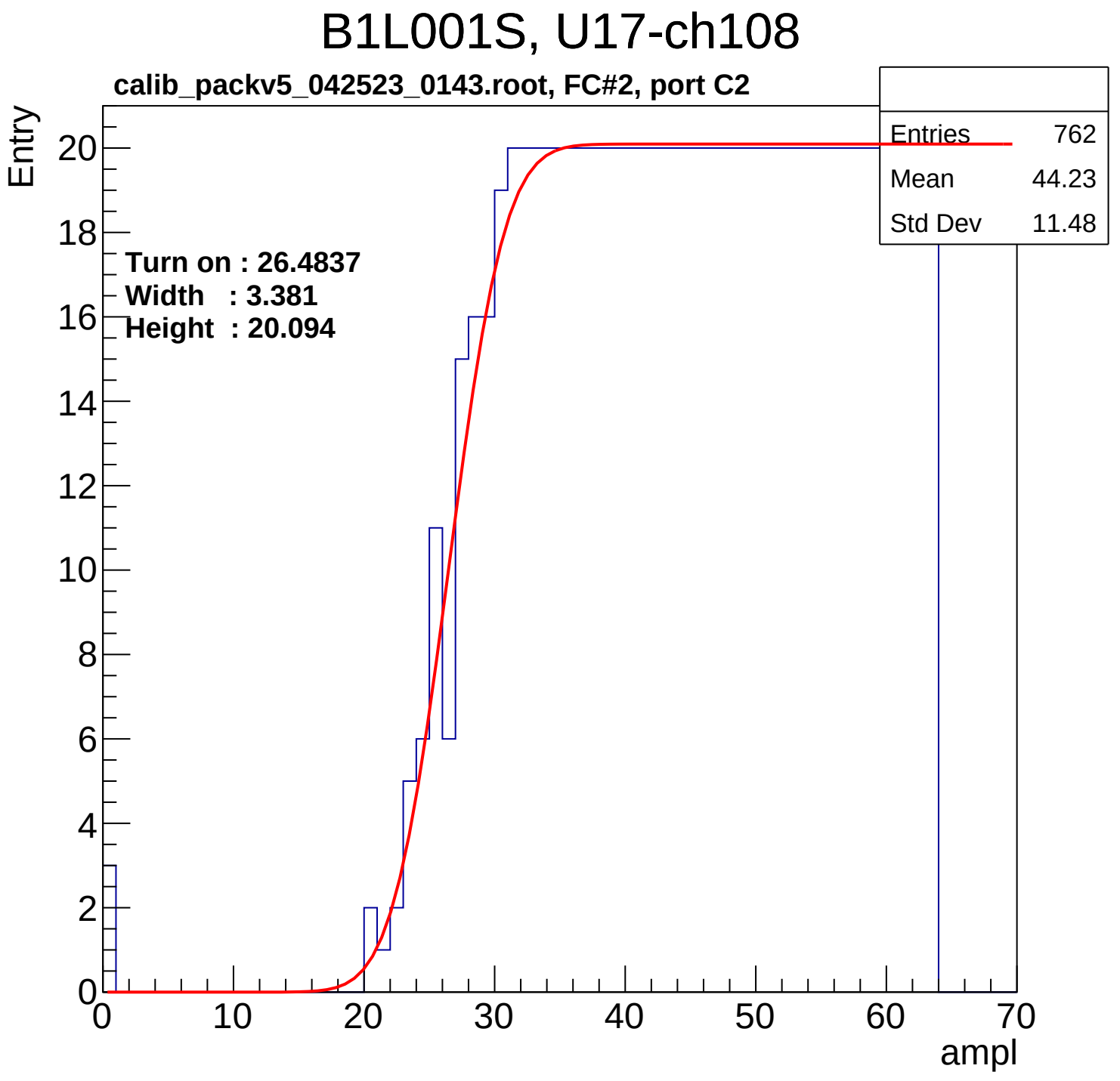
B1L001S, U17-ch108
calib_packv5_042523_0143.root, FC#2, port C2
Entries 762
Mean 44.23
Std Dev 11.48
Turn on : 26.4837
Width : 3.381
Height : 20.094
Entry
ampl
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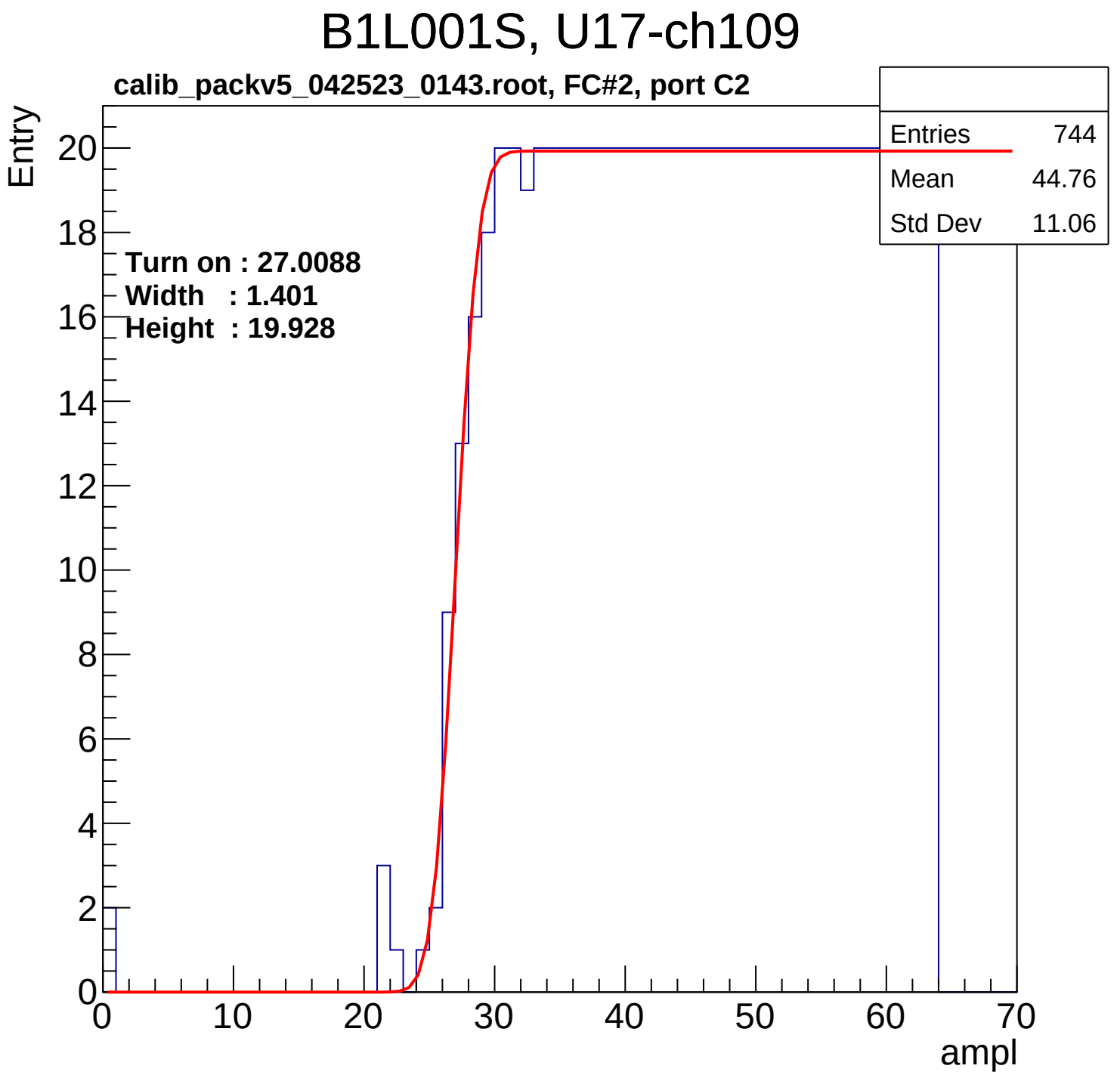
B1L001S, U17-ch109
calib_packv5_042523_0143.root, FC#2, port C2
Entries 744
Mean 44.76
Std Dev 11.06
Turn on : 27.0088
Width : 1.401
Height : 19.928
Entry
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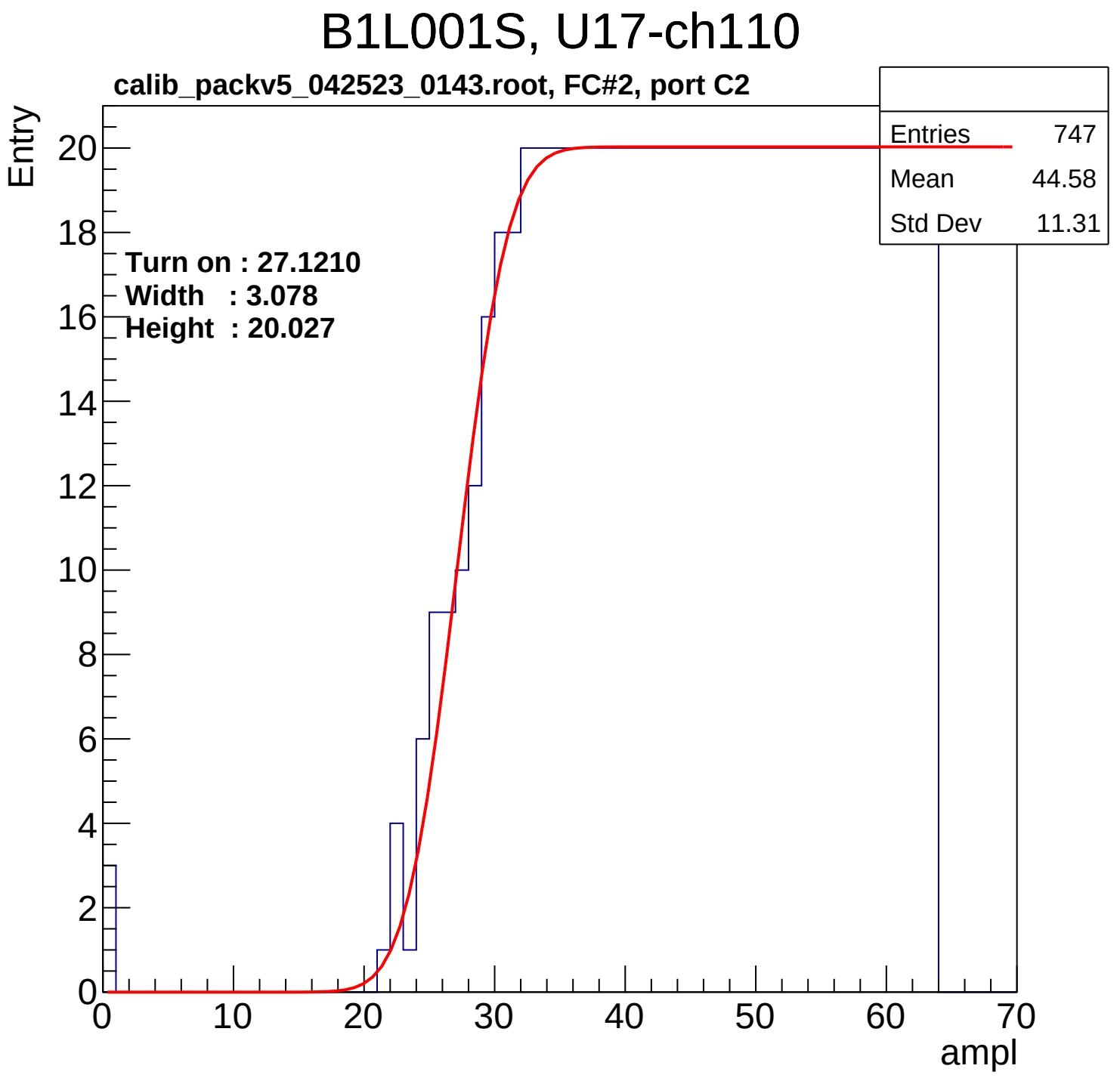
B1L001S, U17-ch110
calib_packv5_042523_0143.root, FC#2, port C2
Entries 747
Mean 44.58
Std Dev 11.31
Turn on : 27.1210
Width : 3.078
Height : 20.027
Entry
ampl
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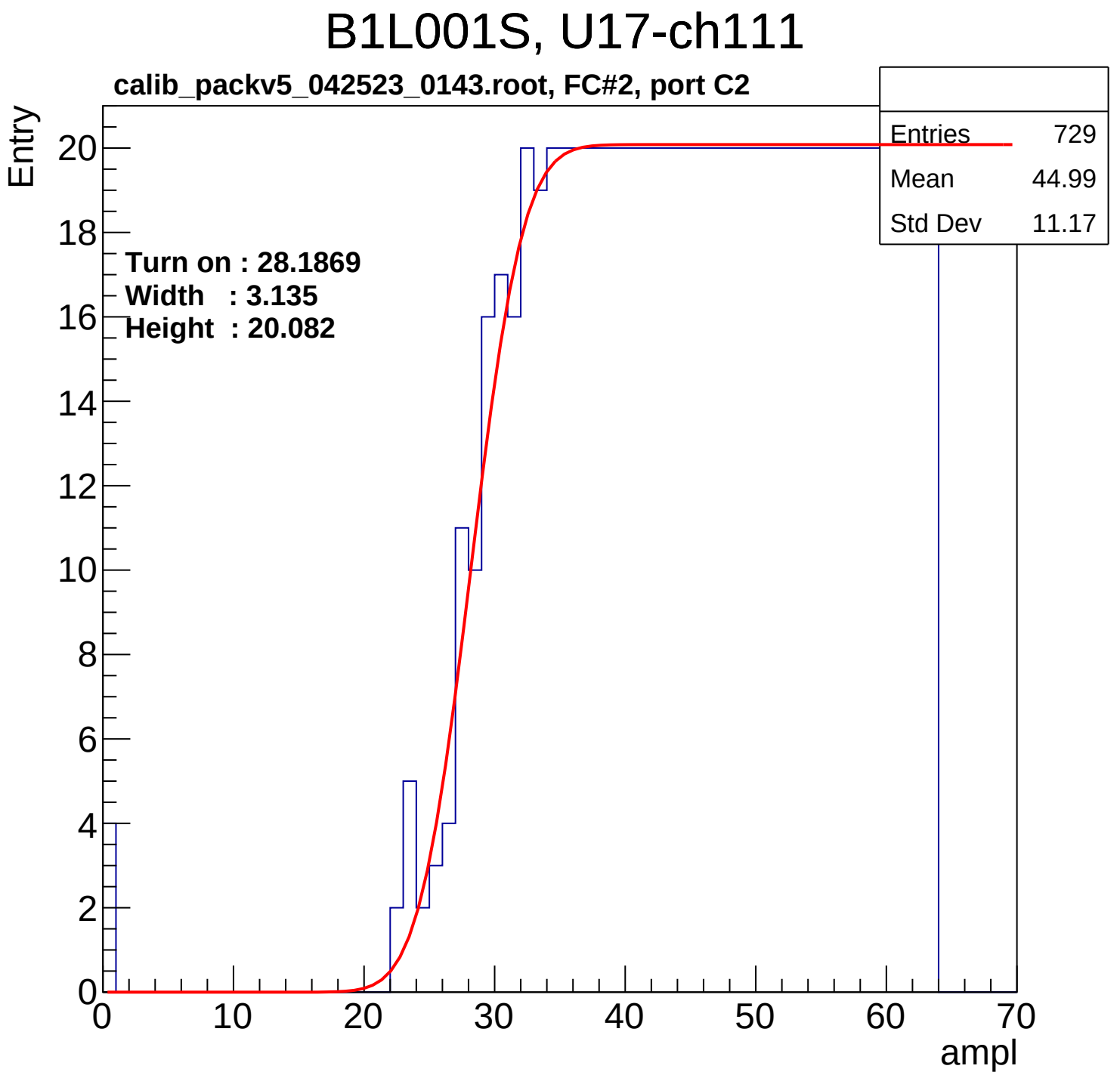
B1L001S, U17-ch111
calib_packv5_042523_0143.root, FC#2, port C2
Entries 729
Mean 44.99
Std Dev 11.17
Turn on : 28.1869
Width : 3.135
Height : 20.082
Entry
ampl
0
2
4
6
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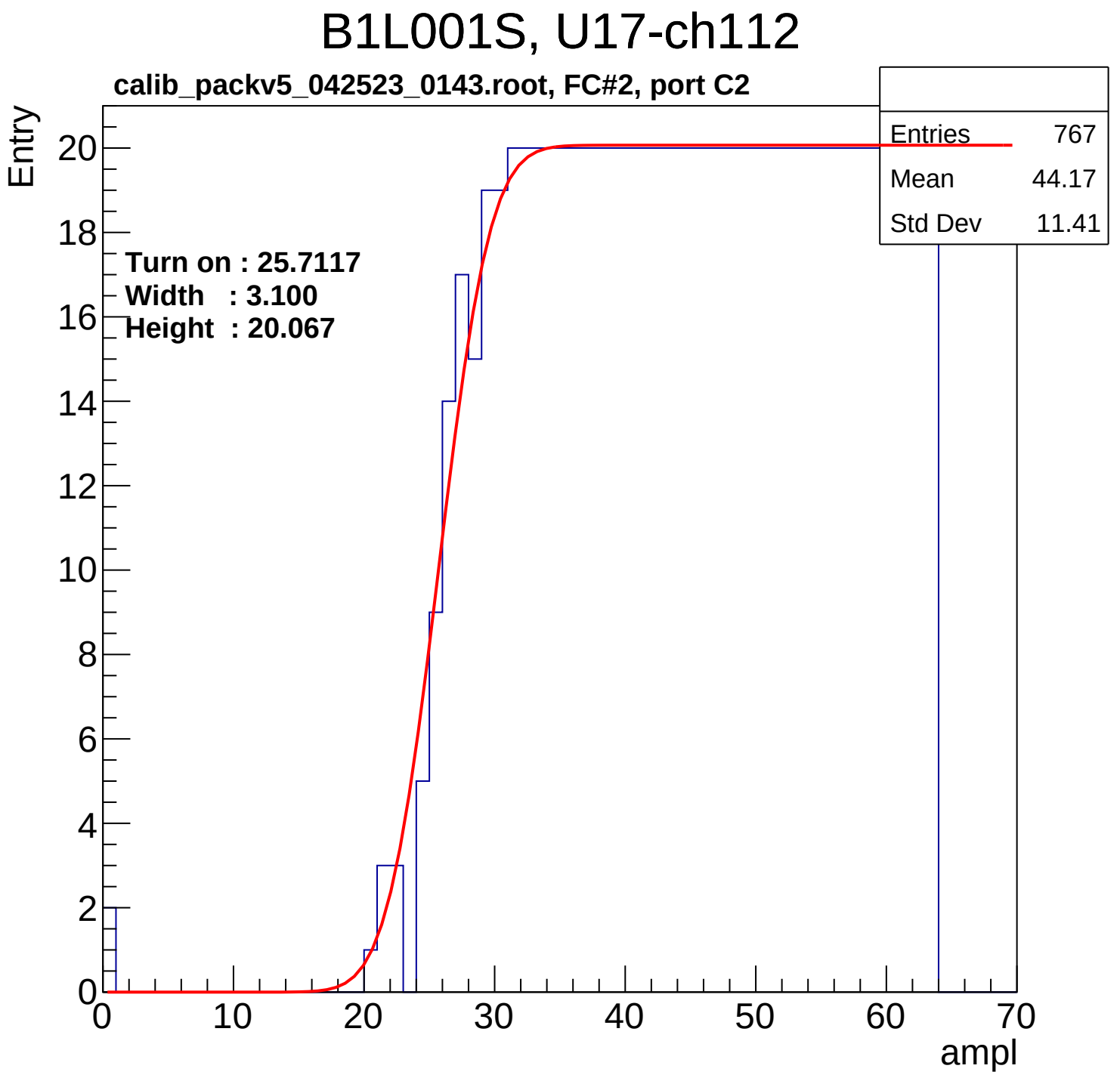
B1L001S, U17-ch112
calib_packv5_042523_0143.root, FC#2, port C2
Entries 767
Mean 44.17
Std Dev 11.41
Turn on : 25.7117
Width : 3.100
Height : 20.067
Entry
ampl
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6
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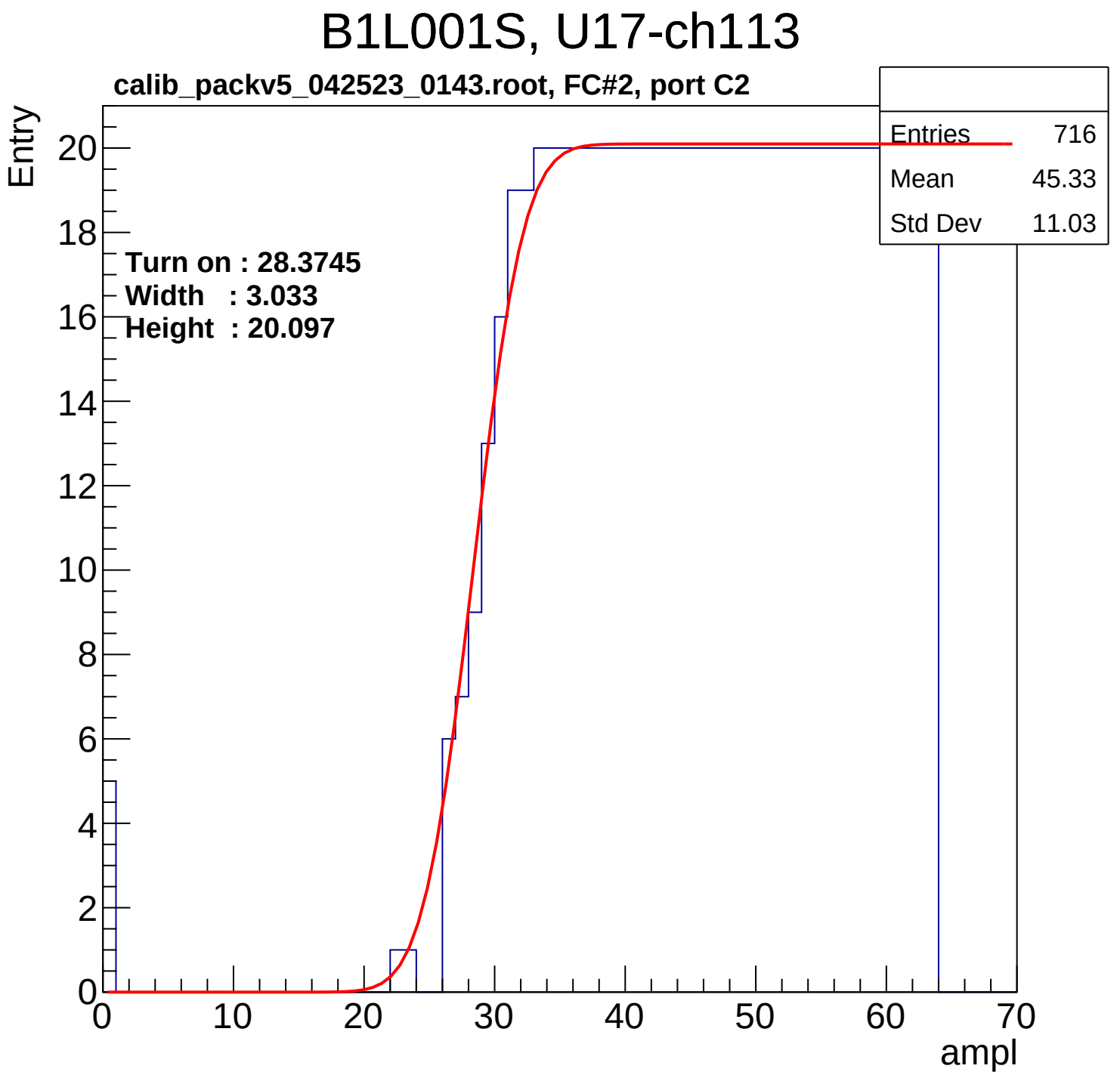
B1L001S, U17-ch113
calib_packv5_042523_0143.root, FC#2, port C2
Entries 716
Mean 45.33
Std Dev 11.03
Turn on : 28.3745
Width : 3.033
Height : 20.097
Entry
ampl
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6
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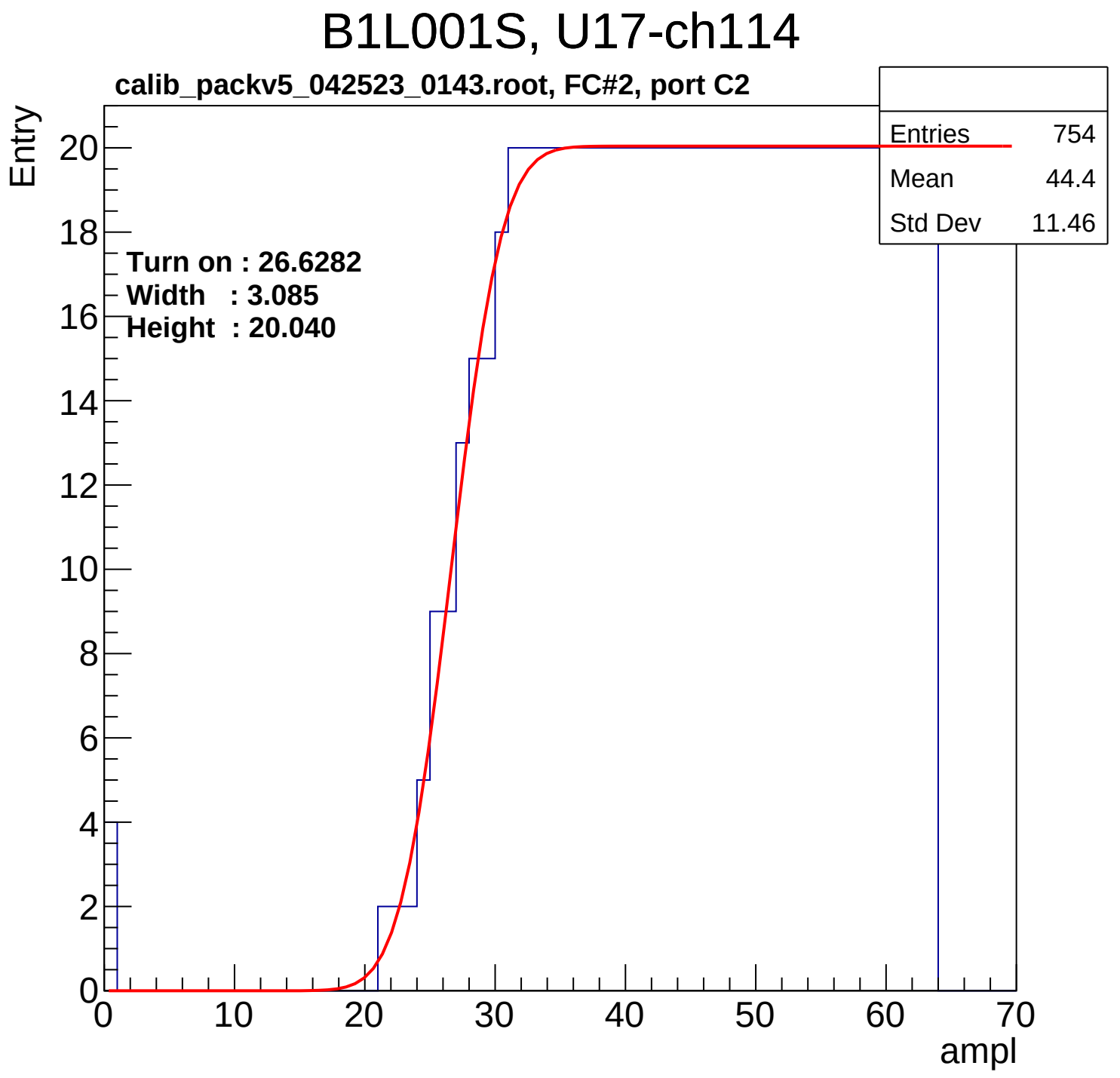
B1L001S, U17-ch114
calib_packv5_042523_0143.root, FC#2, port C2
Entries 754
Mean 44.4
Std Dev 11.46
Turn on : 26.6282
Width : 3.085
Height : 20.040
Entry
ampl
0
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6
8
10
12
14
16
18
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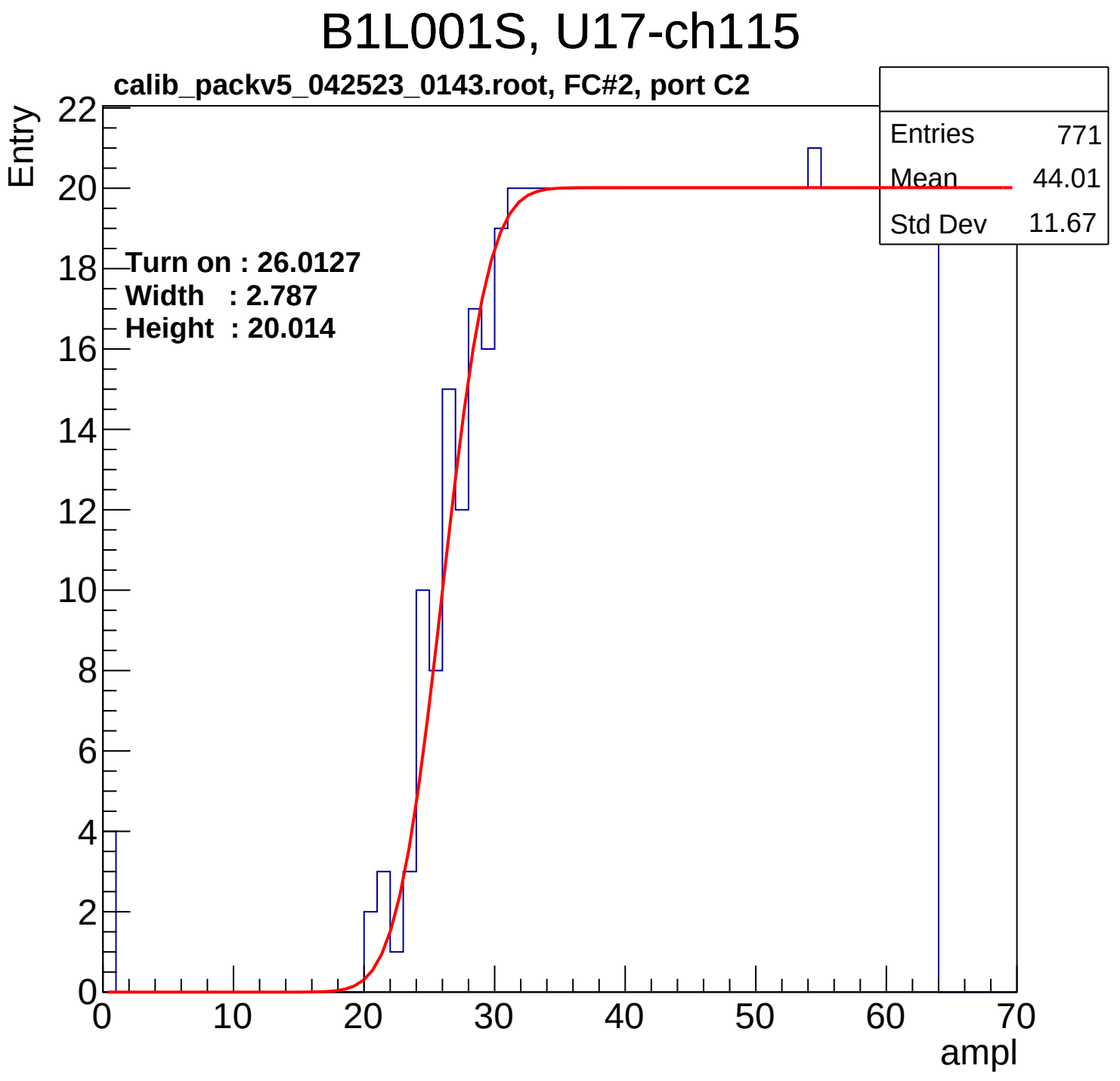
B1L001S, U17-ch115
calib_packv5_042523_0143.root, FC#2, port C2
Entries 771
Mean 44.01
Std Dev 11.67
Turn on : 26.0127
Width : 2.787
Height : 20.014
Entry
ampl
0
2
4
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8
10
12
14
16
18
20
22
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20
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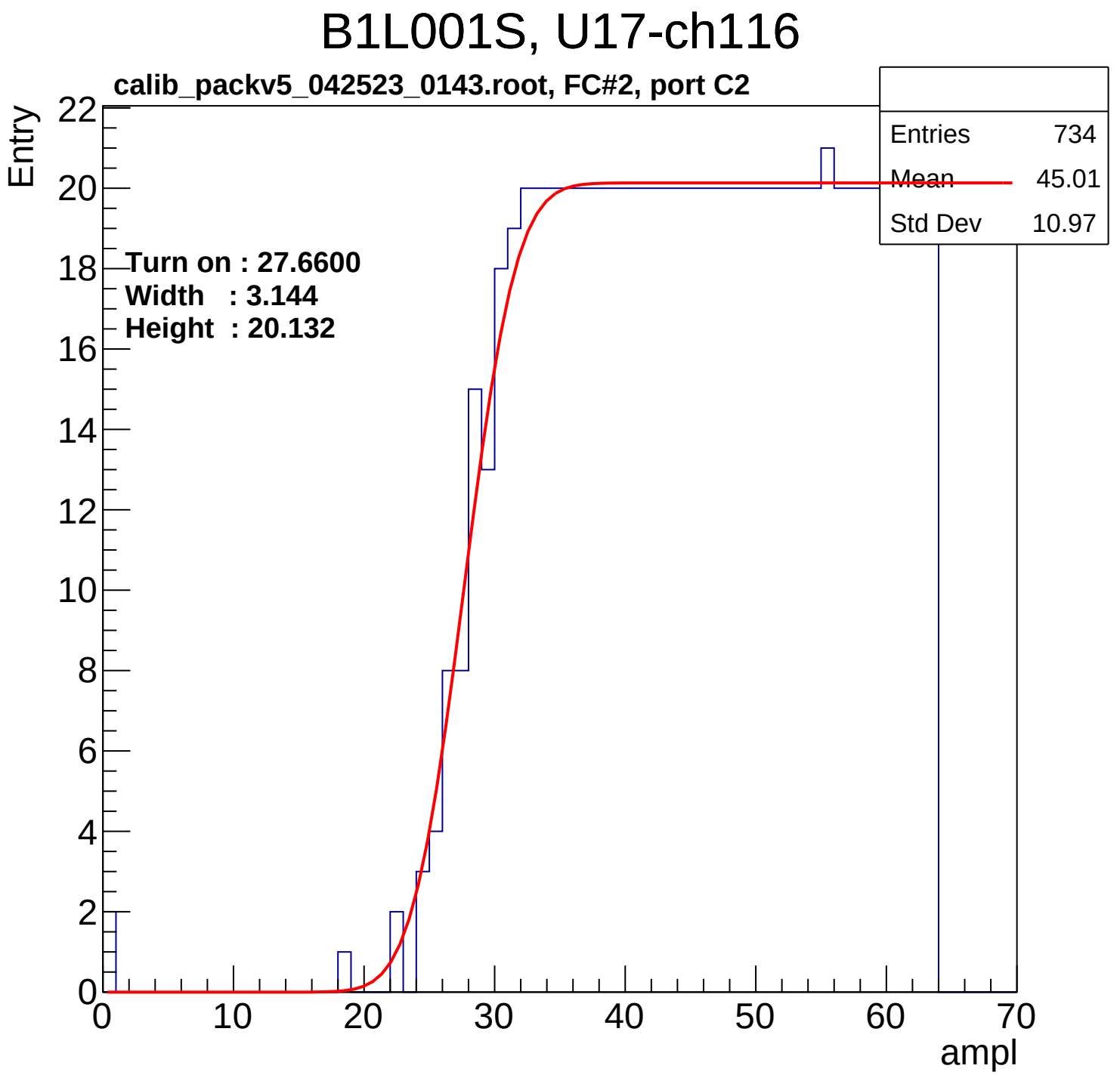
B1L001S, U17-ch116
calib_packv5_042523_0143.root, FC#2, port C2
Entries 734
Mean 45.01
Std Dev 10.97
Turn on : 27.6600
Width : 3.144
Height : 20.132
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
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20
30
40
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60
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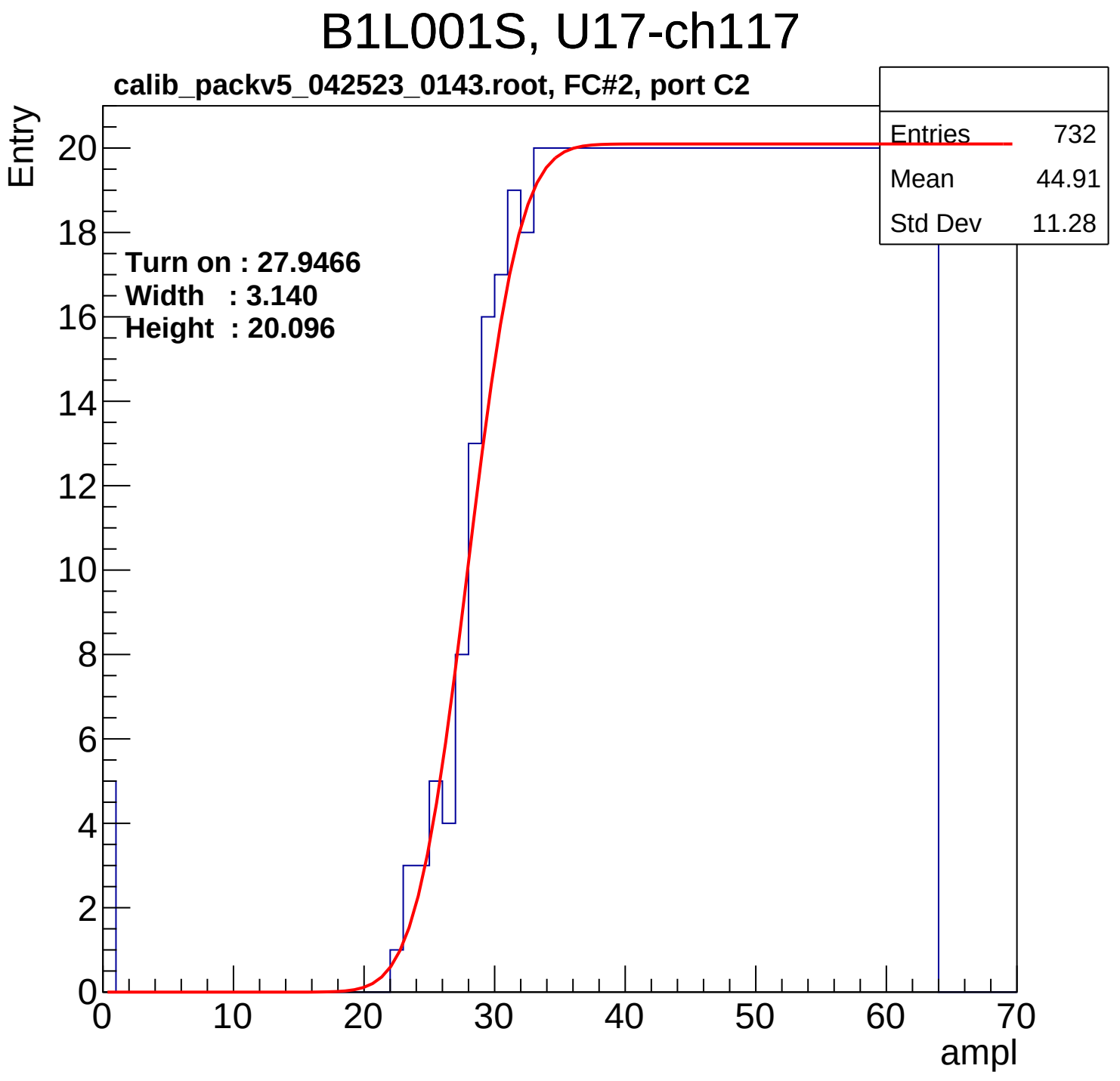
B1L001S, U17-ch117
calib_packv5_042523_0143.root, FC#2, port C2
Entries 732
Mean 44.91
Std Dev 11.28
Turn on : 27.9466
Width : 3.140
Height : 20.096
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
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20
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40
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60
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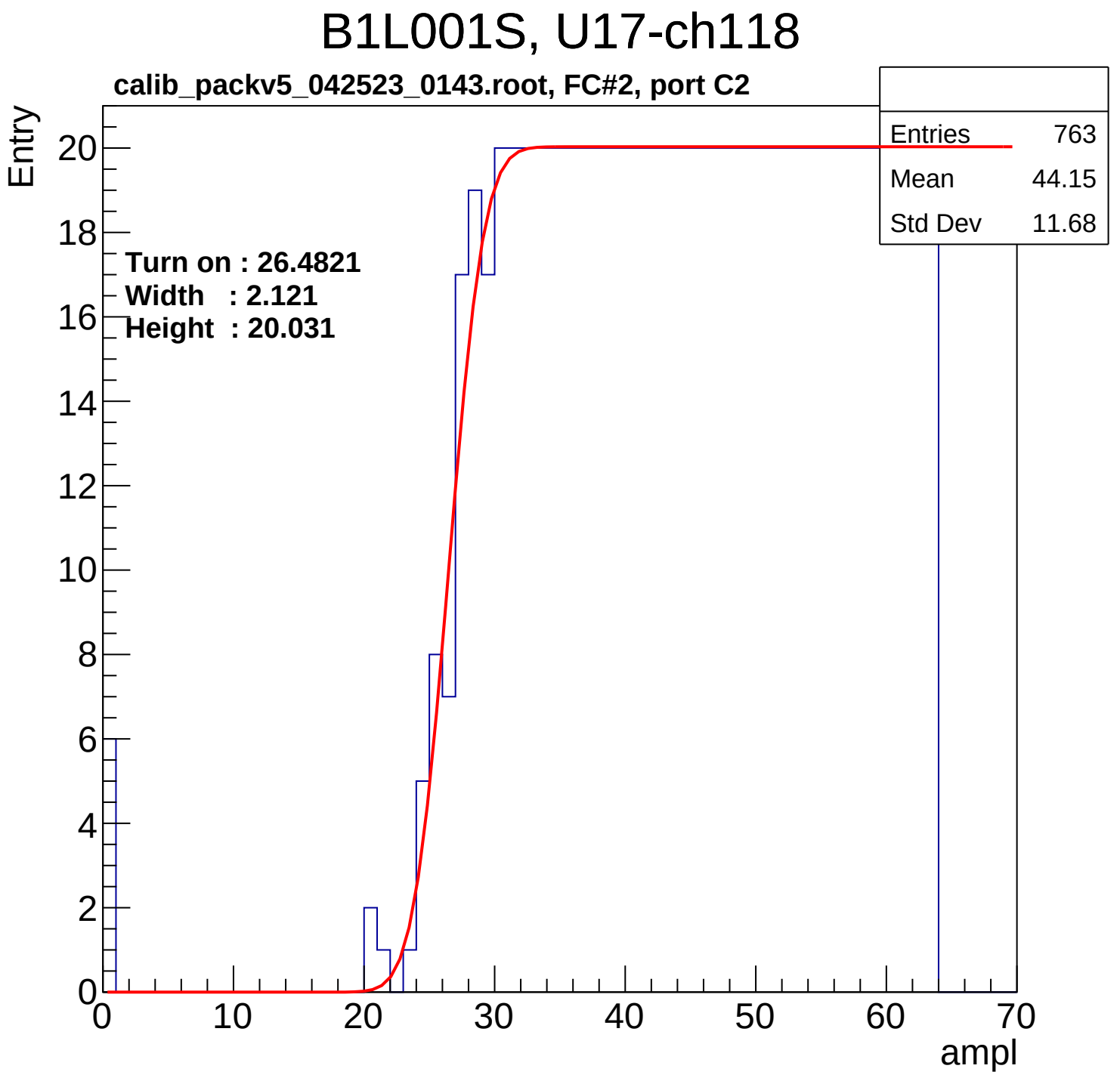
B1L001S, U17-ch118
calib_packv5_042523_0143.root, FC#2, port C2
Entries 763
Mean 44.15
Std Dev 11.68
Turn on : 26.4821
Width : 2.121
Height : 20.031
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
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20
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40
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60
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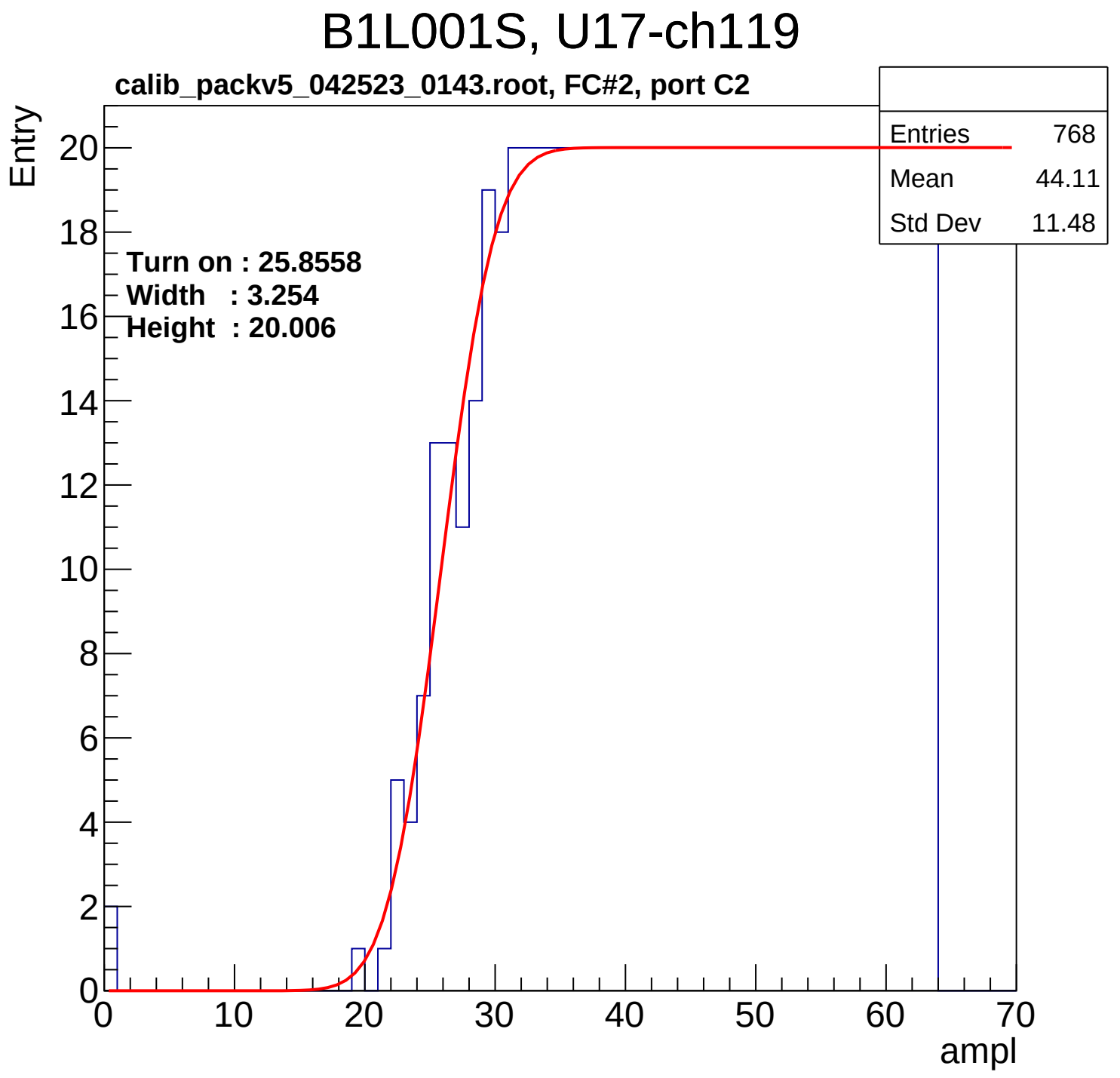
B1L001S, U17-ch119
calib_packv5_042523_0143.root, FC#2, port C2
Entries 768
Mean 44.11
Std Dev 11.48
Turn on : 25.8558
Width : 3.254
Height : 20.006
Entry
ampl
0
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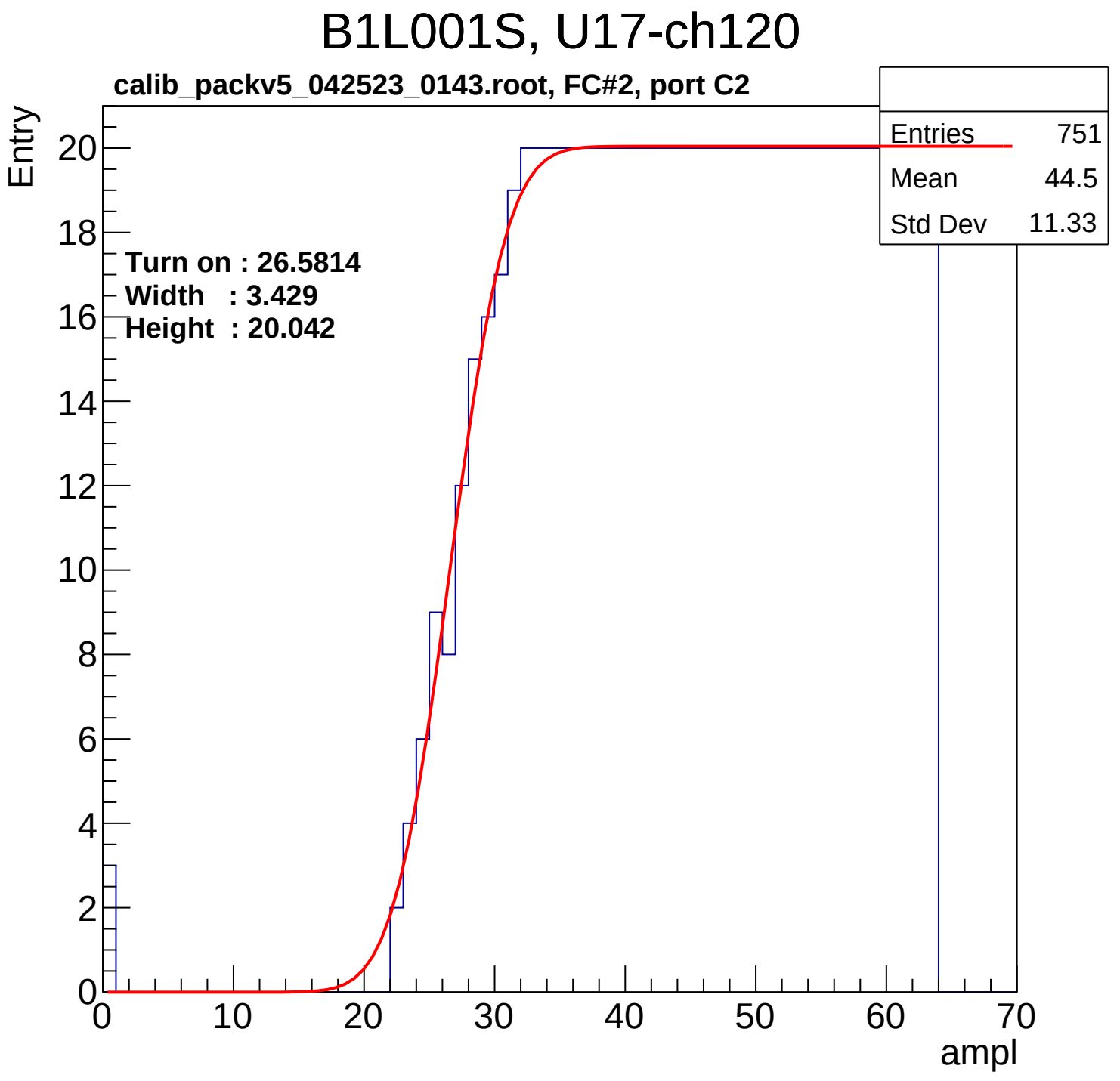
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70


B1L001S, U17-ch120
calib_packv5_042523_0143.root, FC#2, port C2
Entries 751
Mean 44.5
Std Dev 11.33
Turn on : 26.5814
Width : 3.429
Height : 20.042
Entry
ampl
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6
8
10
12
14
16
18
20
0
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20
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40
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60
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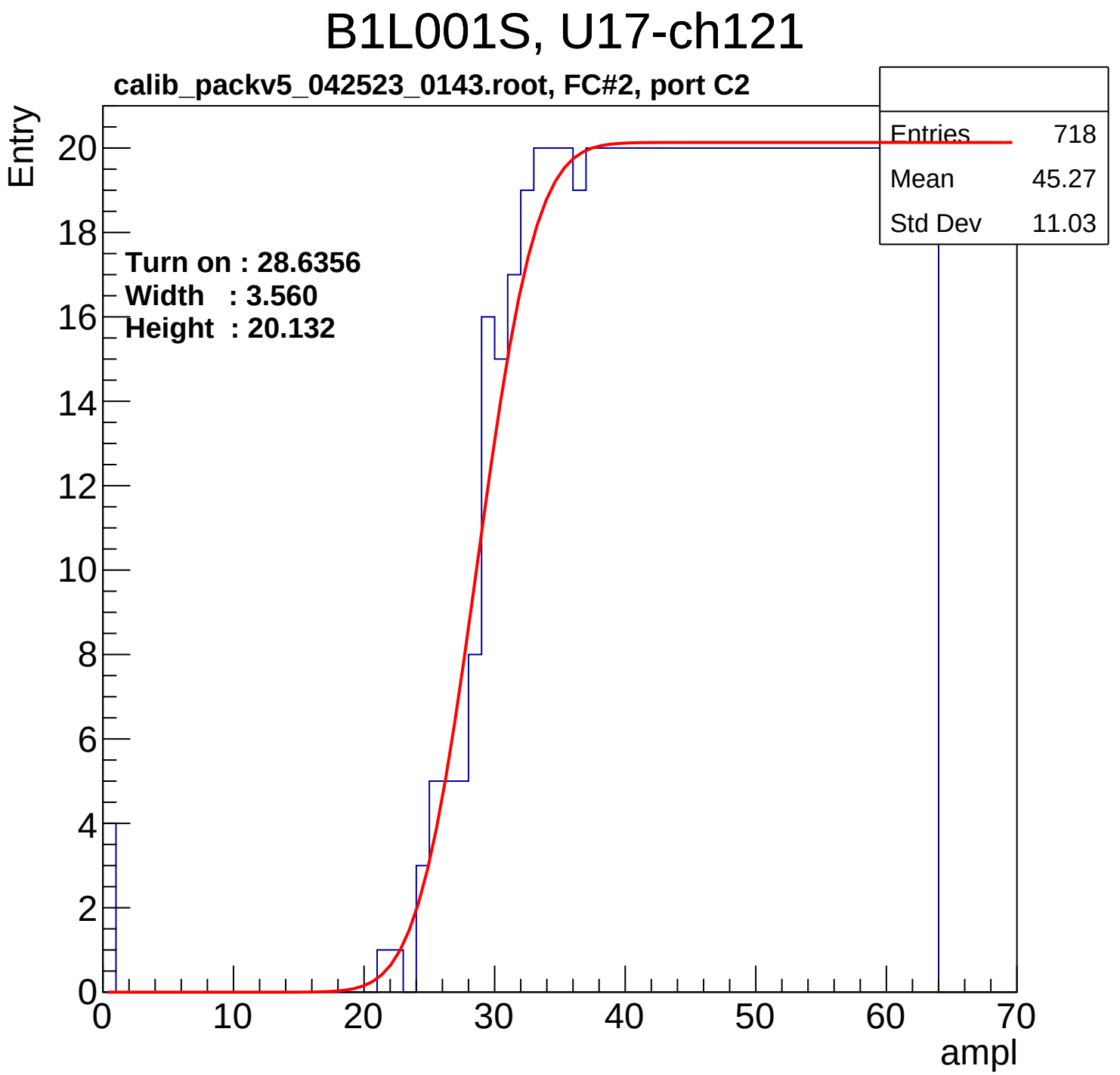
B1L001S, U17-ch121
calib_packv5_042523_0143.root, FC#2, port C2
Entries 718
Mean 45.27
Std Dev 11.03
Turn on : 28.6356
Width : 3.560
Height : 20.132
Entry
ampl
0
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4
6
8
10
12
14
16
18
20
0
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20
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60
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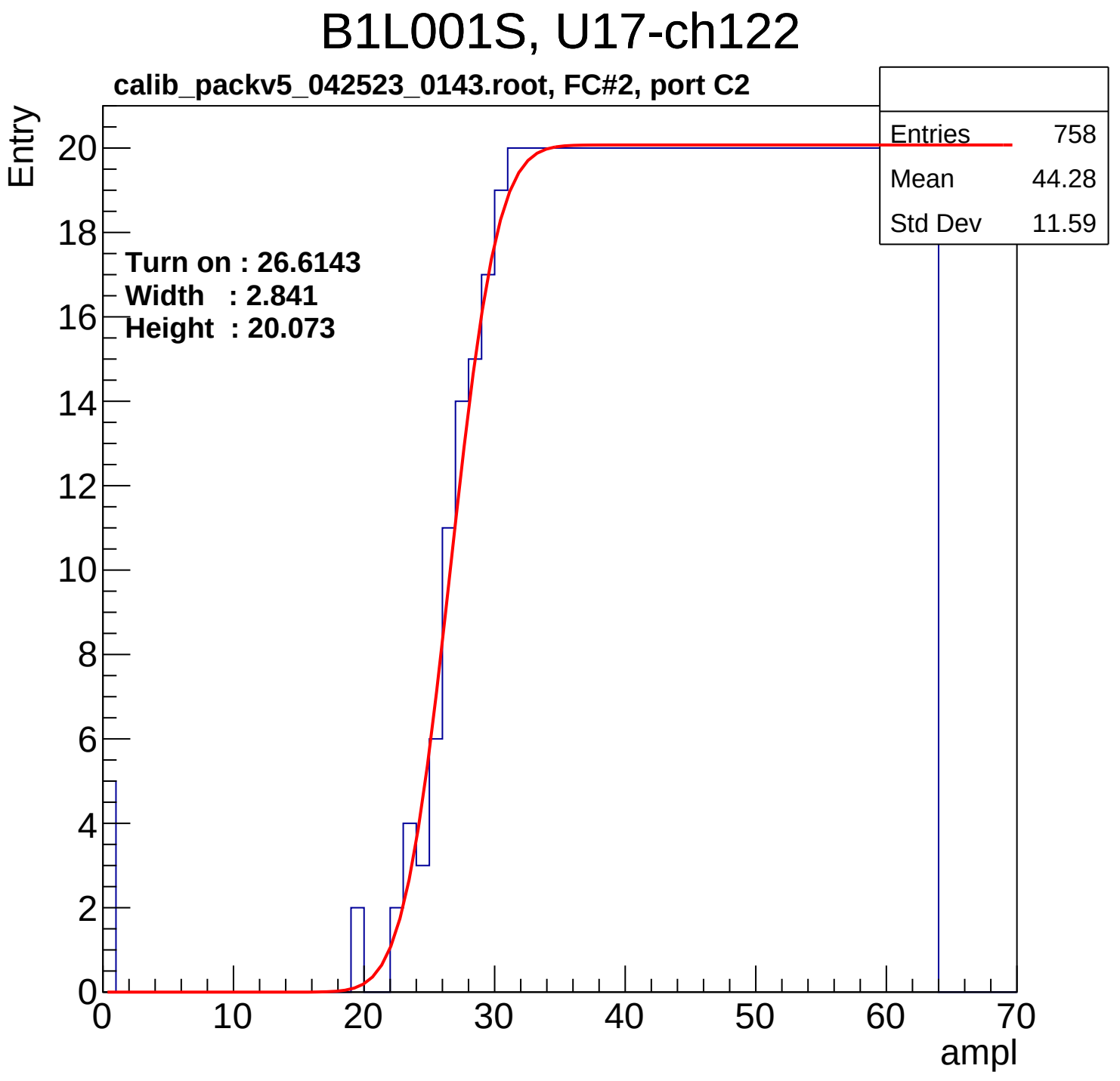
B1L001S, U17-ch122
calib_packv5_042523_0143.root, FC#2, port C2
Entries 758
Mean 44.28
Std Dev 11.59
Turn on : 26.6143
Width : 2.841
Height : 20.073
Entry
ampl
0
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4
6
8
10
12
14
16
18
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0
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20
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40
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60
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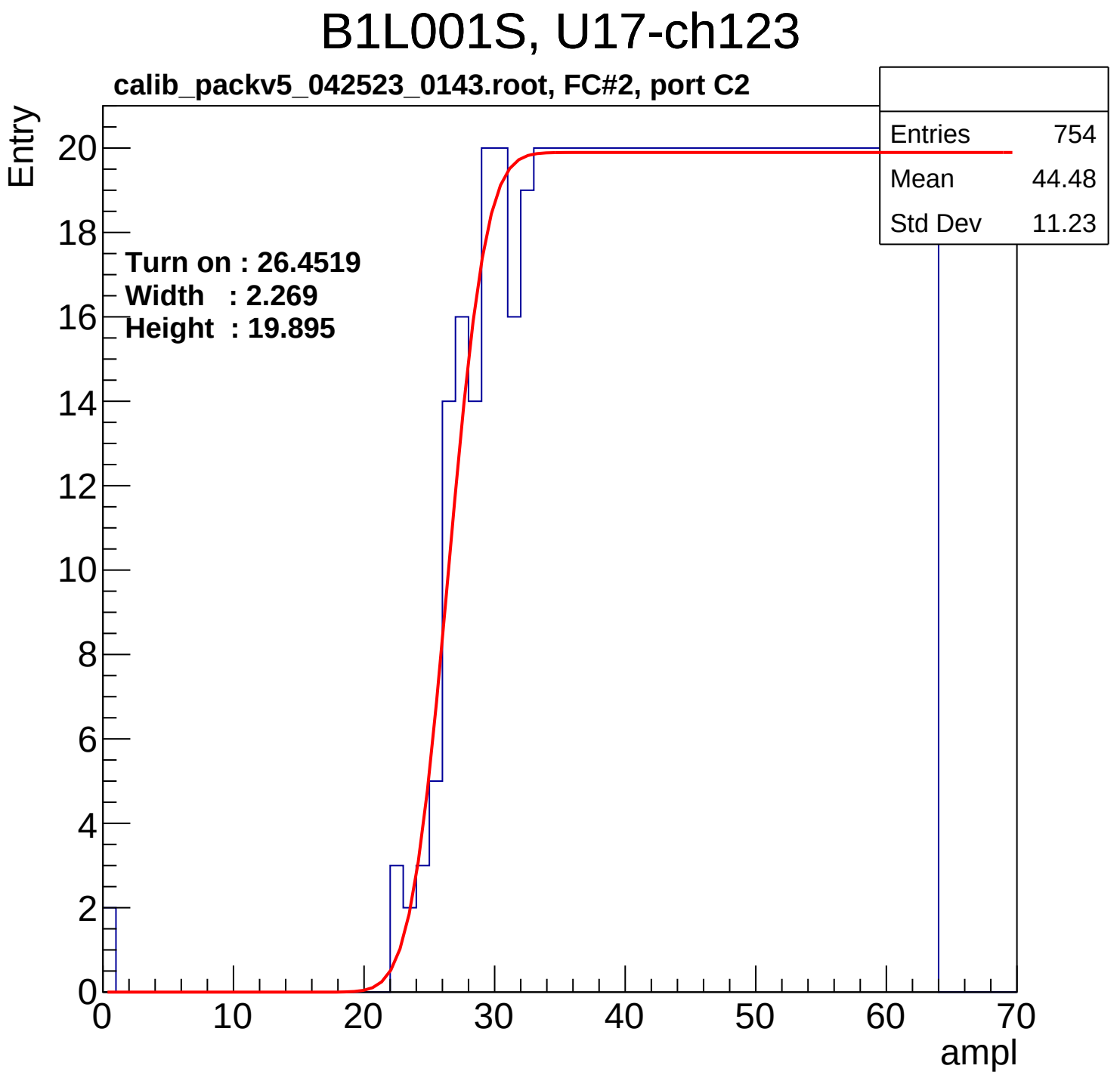
B1L001S, U17-ch123
calib_packv5_042523_0143.root, FC#2, port C2
Entries 754
Mean 44.48
Std Dev 11.23
Turn on : 26.4519
Width : 2.269
Height : 19.895
Entry
ampl
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4
6
8
10
12
14
16
18
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0
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20
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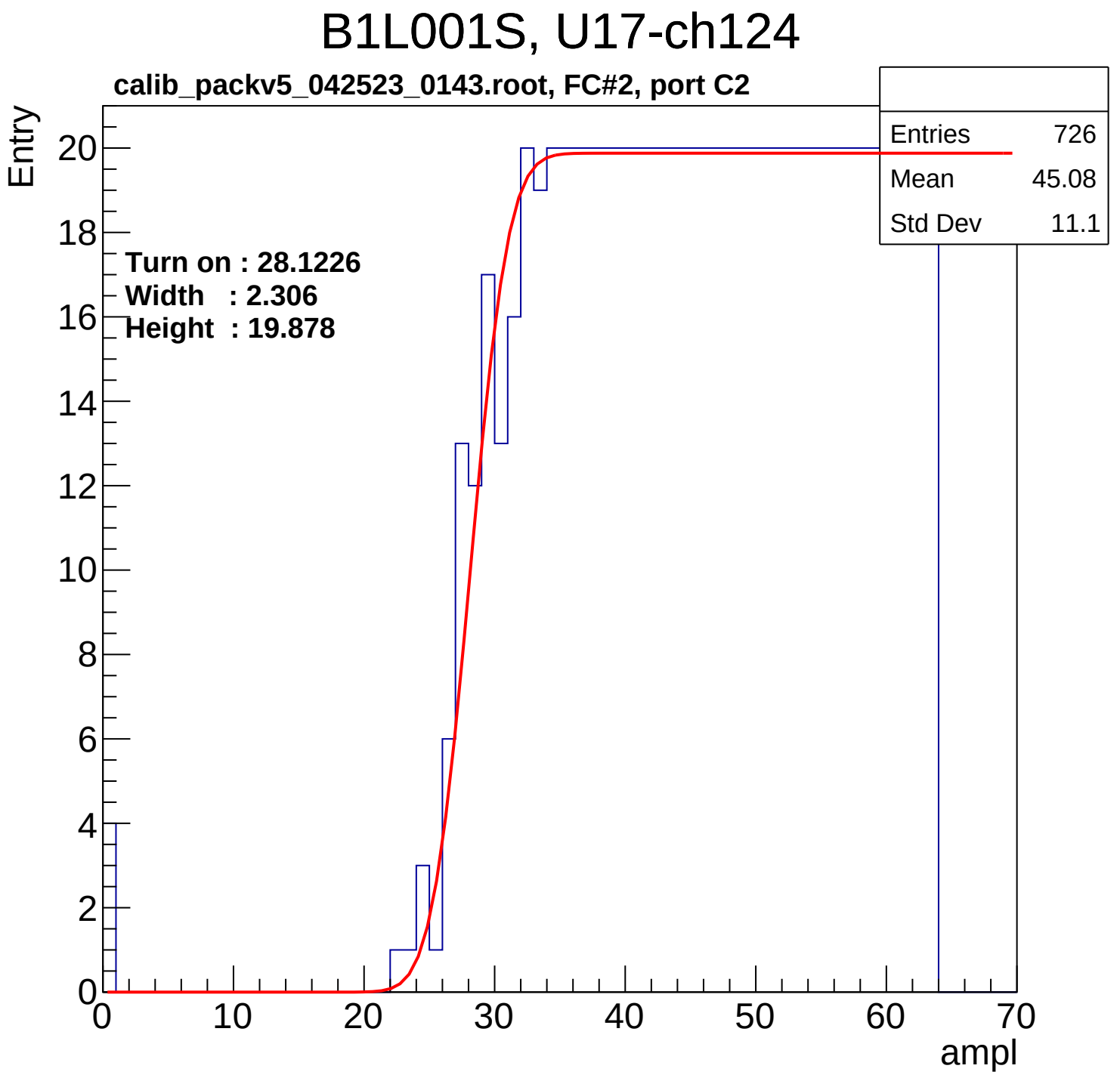
B1L001S, U17-ch124
calib_packv5_042523_0143.root, FC#2, port C2
Entries 726
Mean 45.08
Std Dev 11.1
Turn on : 28.1226
Width : 2.306
Height : 19.878
Entry
ampl
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6
8
10
12
14
16
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20
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60
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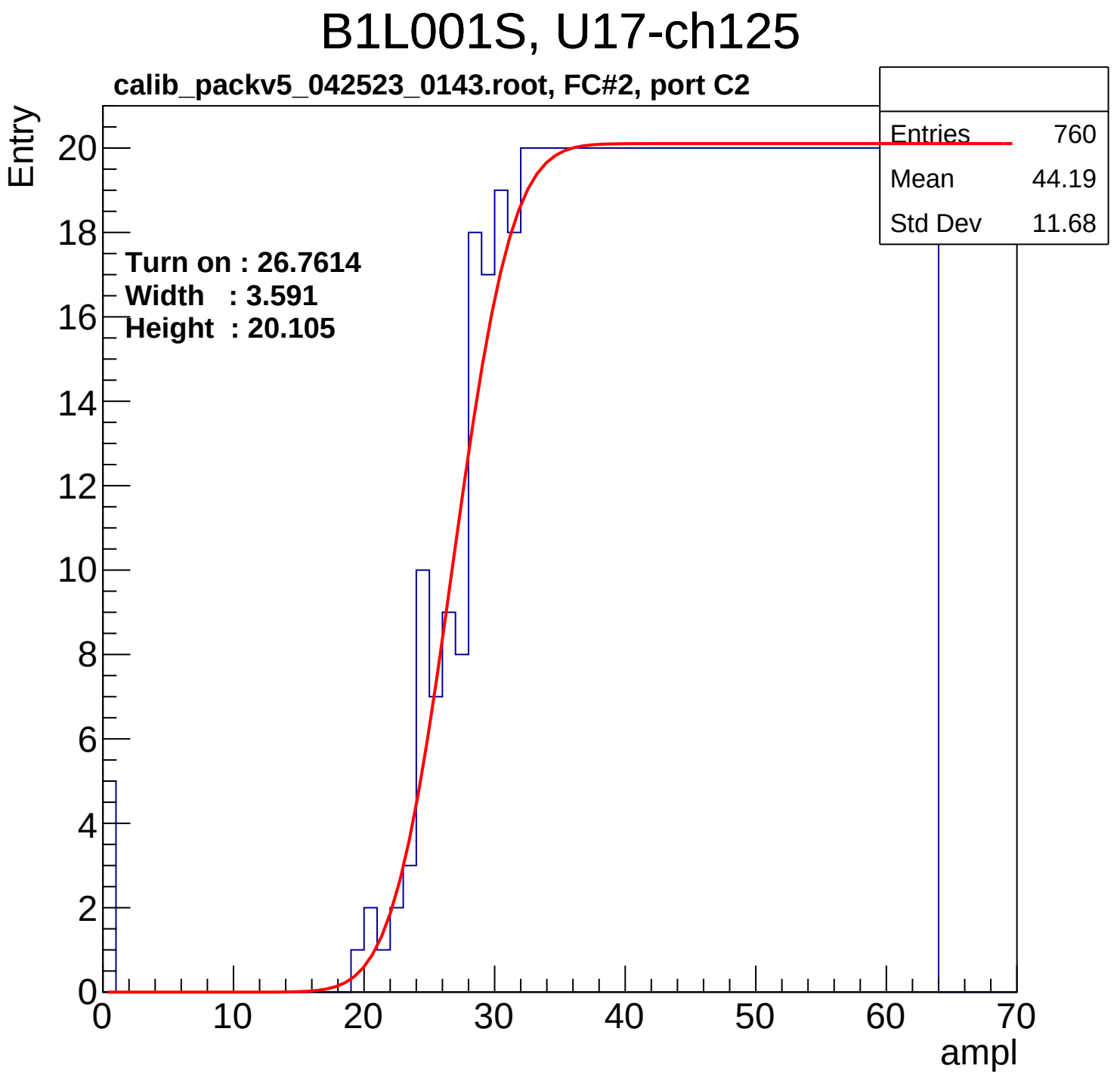
B1L001S, U17-ch125
calib_packv5_042523_0143.root, FC#2, port C2
Entries 760
Mean 44.19
Std Dev 11.68
Turn on : 26.7614
Width : 3.591
Height : 20.105
Entry
ampl
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6
8
10
12
14
16
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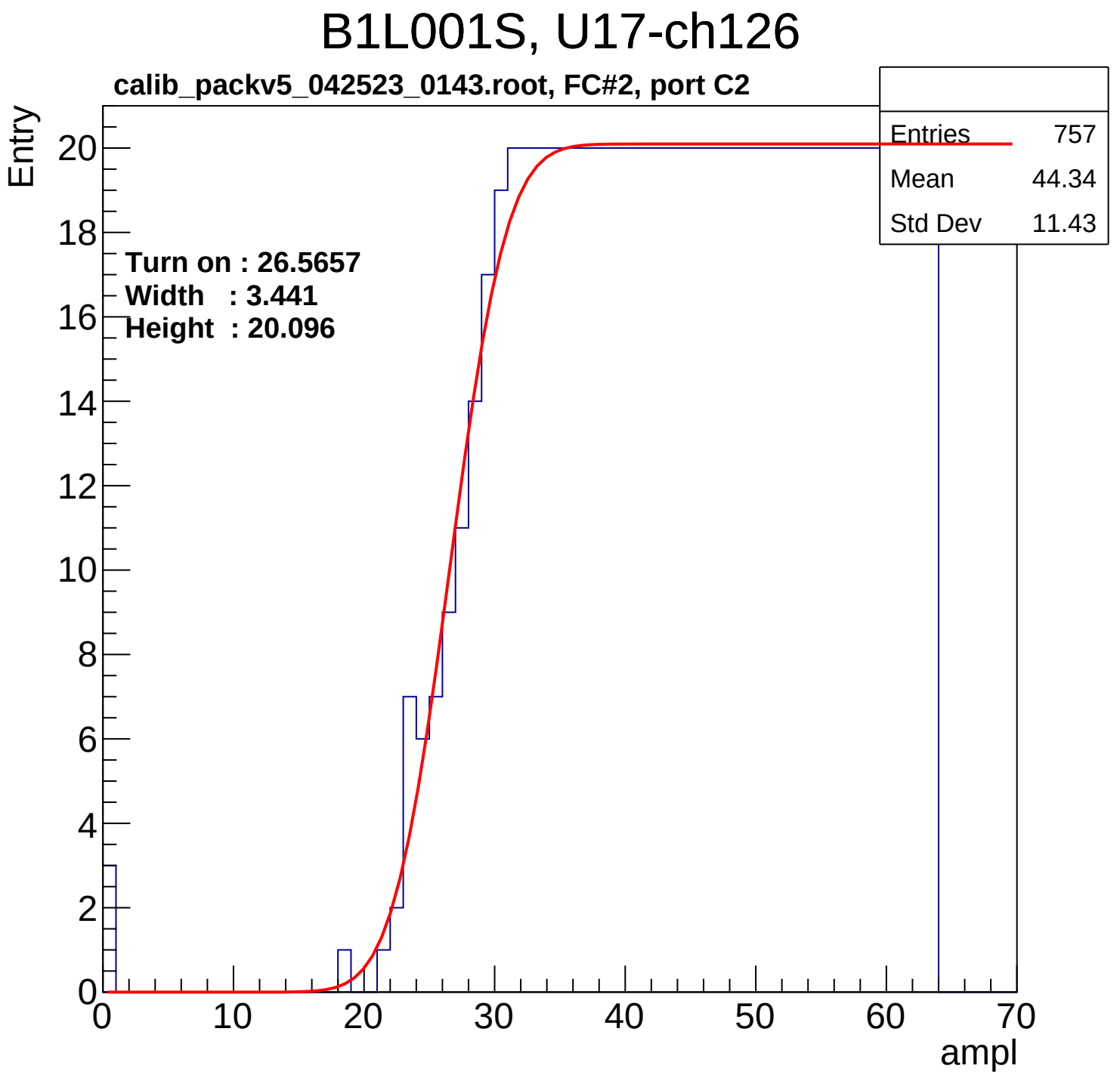
B1L001S, U17-ch126
calib_packv5_042523_0143.root, FC#2, port C2
Entries 757
Mean 44.34
Std Dev 11.43
Turn on : 26.5657
Width : 3.441
Height : 20.096
Entry
ampl
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6
8
10
12
14
16
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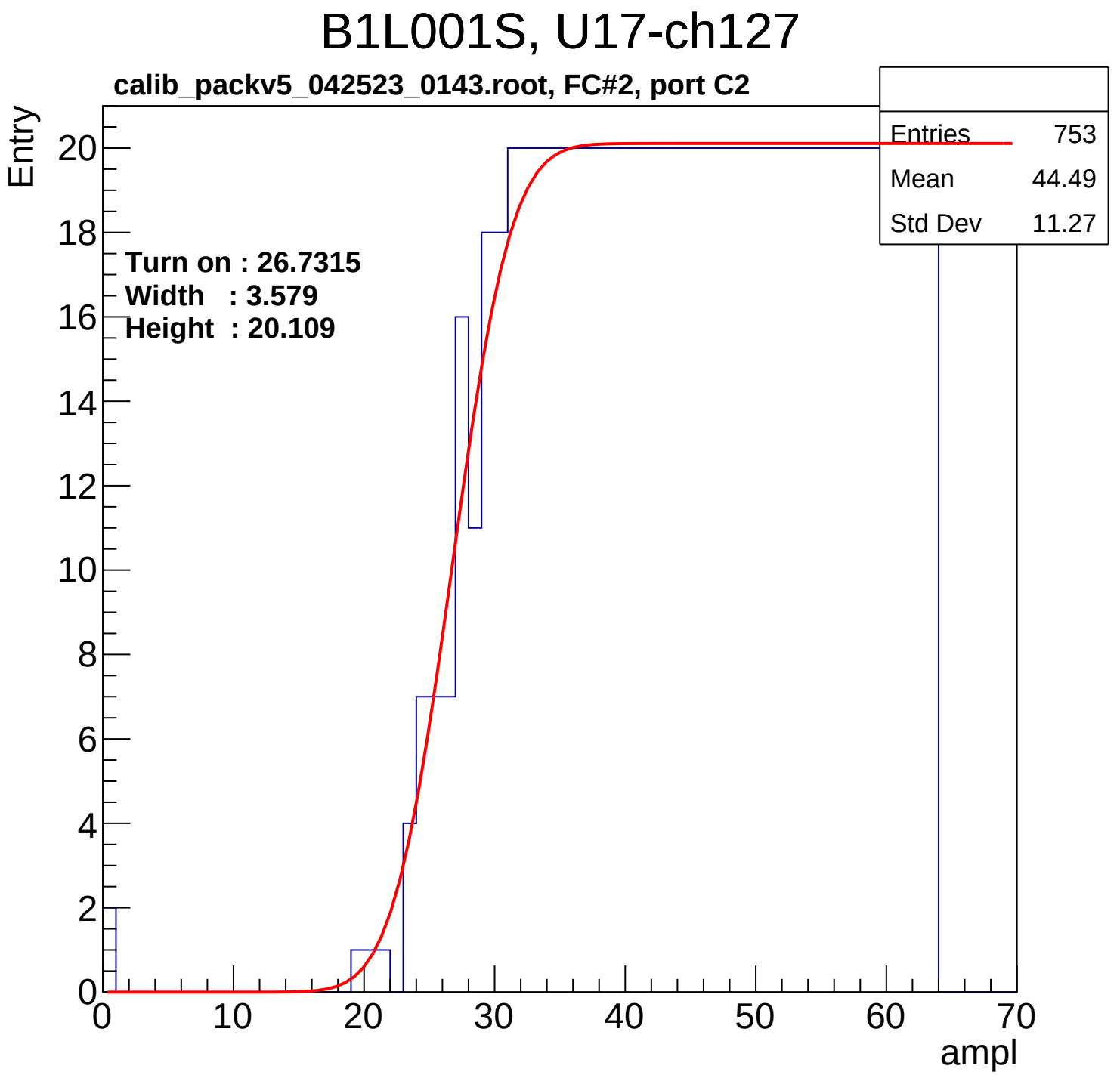
B1L001S, U17-ch127
calib_packv5_042523_0143.root, FC#2, port C2
Entries 753
Mean 44.49
Std Dev 11.27
Turn on : 26.7315
Width : 3.579
Height : 20.109
Entry
ampl
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6
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10
12
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0
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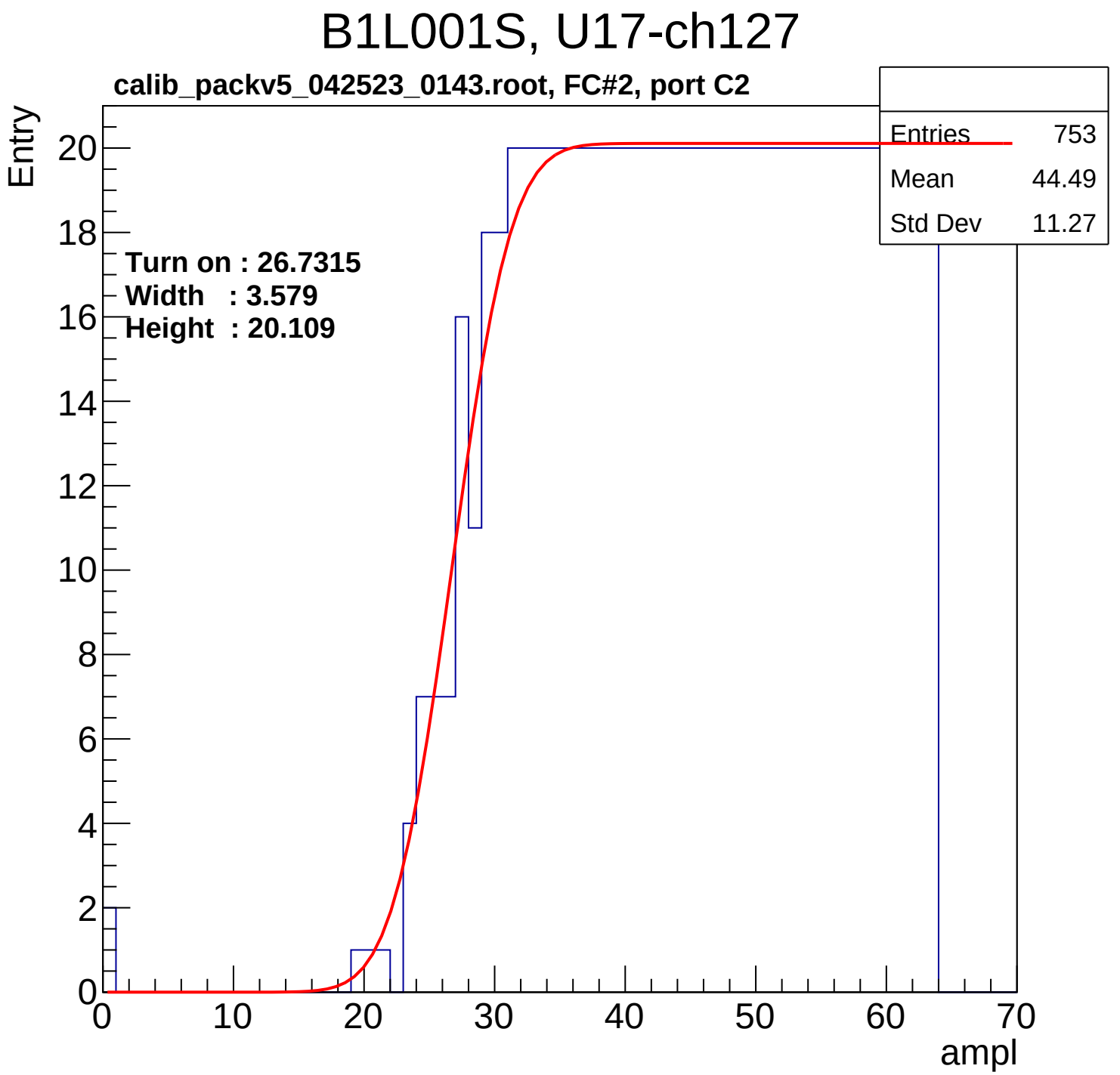
B1L001S, U17-ch127
calib_packv5_042523_0143.root, FC#2, port C2
Entries 753
Mean 44.49
Std Dev 11.27
Turn on : 26.7315
Width : 3.579
Height : 20.109
Entry
ampl
0
2
4
6
8
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16
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