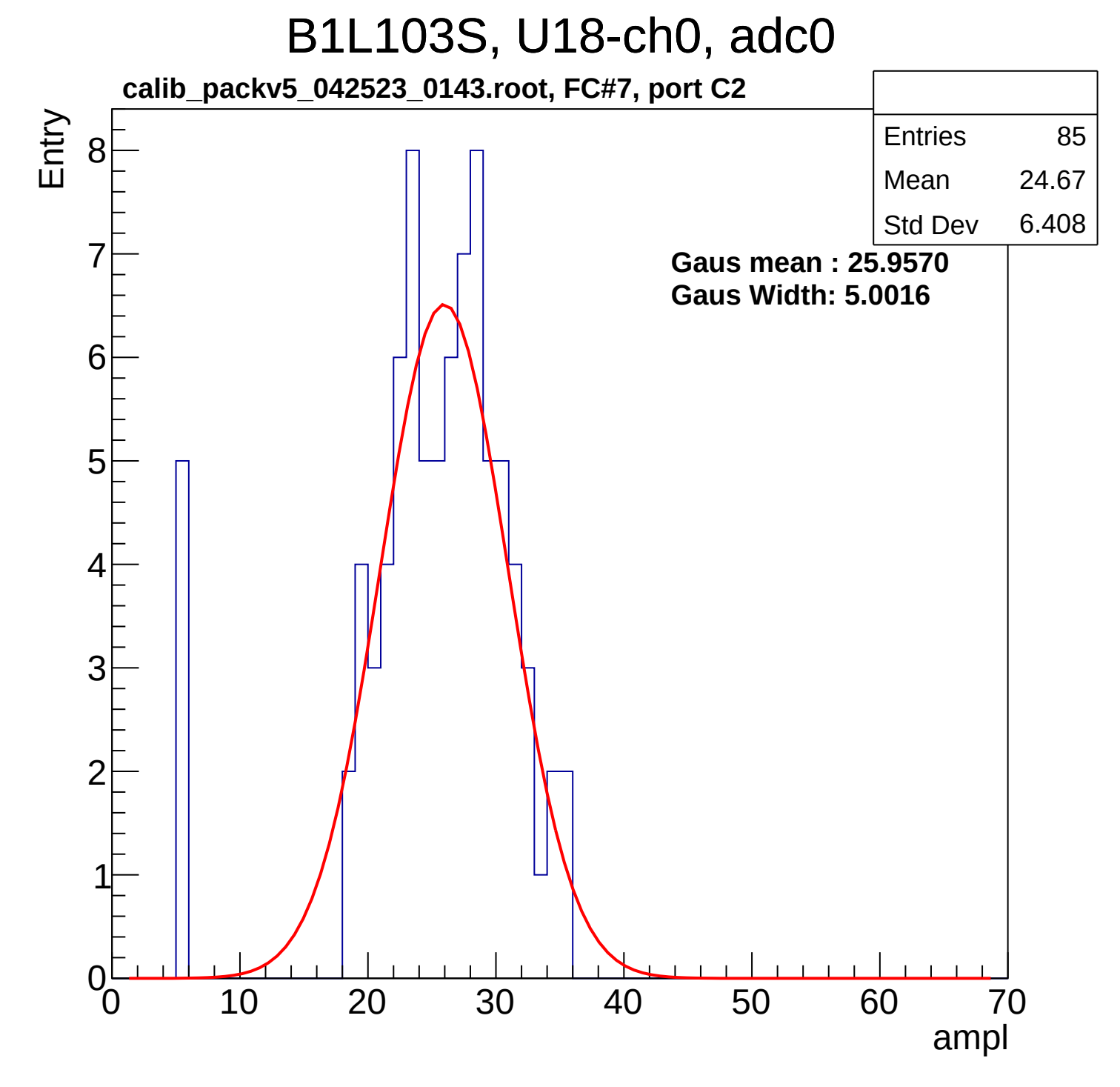
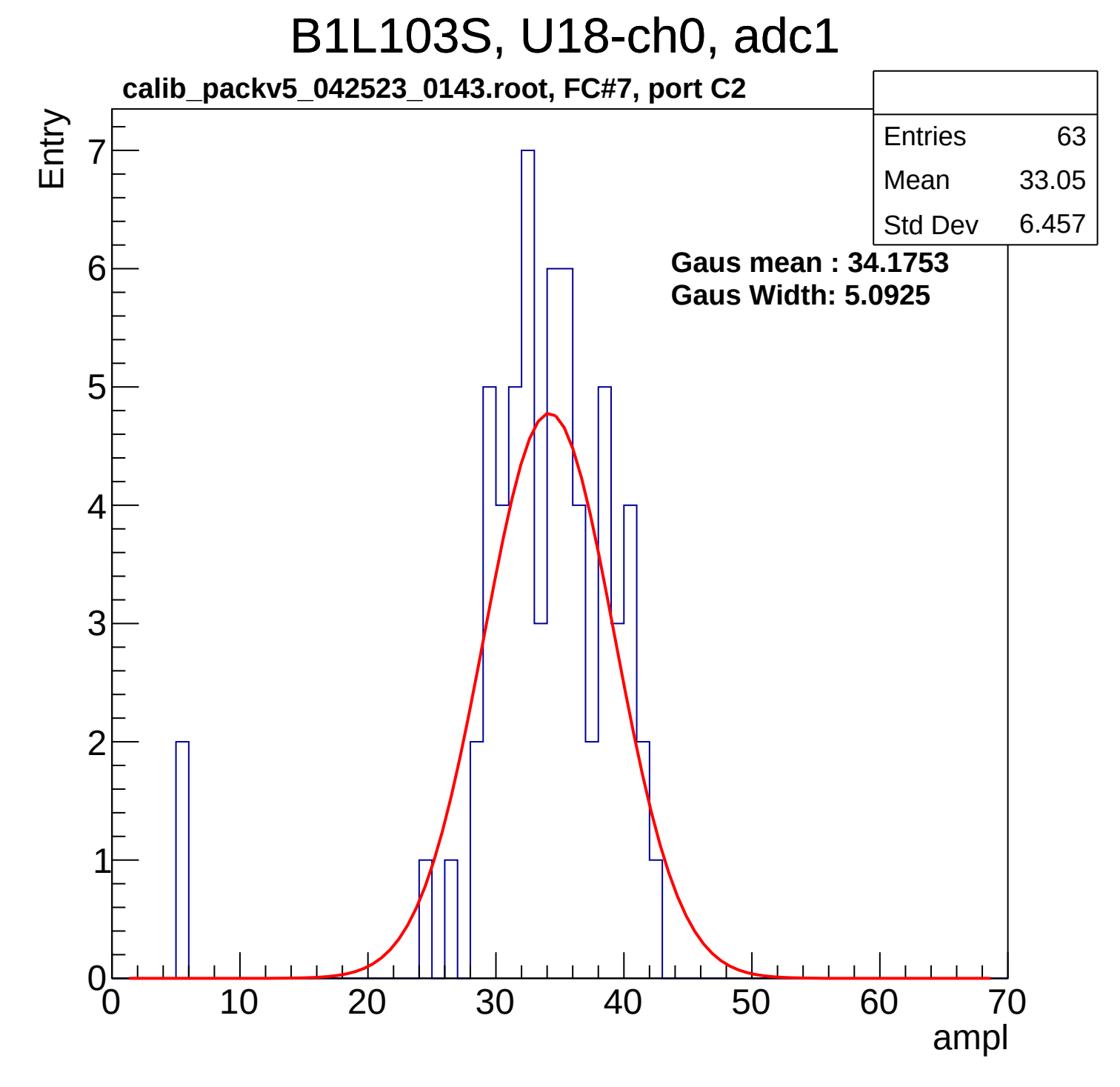

B1L103S, U18-ch0, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 85
Mean 24.67
Std Dev 6.408
Gaus mean : 25.9570
Gaus Width: 5.0016
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch0, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 33.05
Std Dev 6.457
Gaus mean : 34.1753
Gaus Width: 5.0925
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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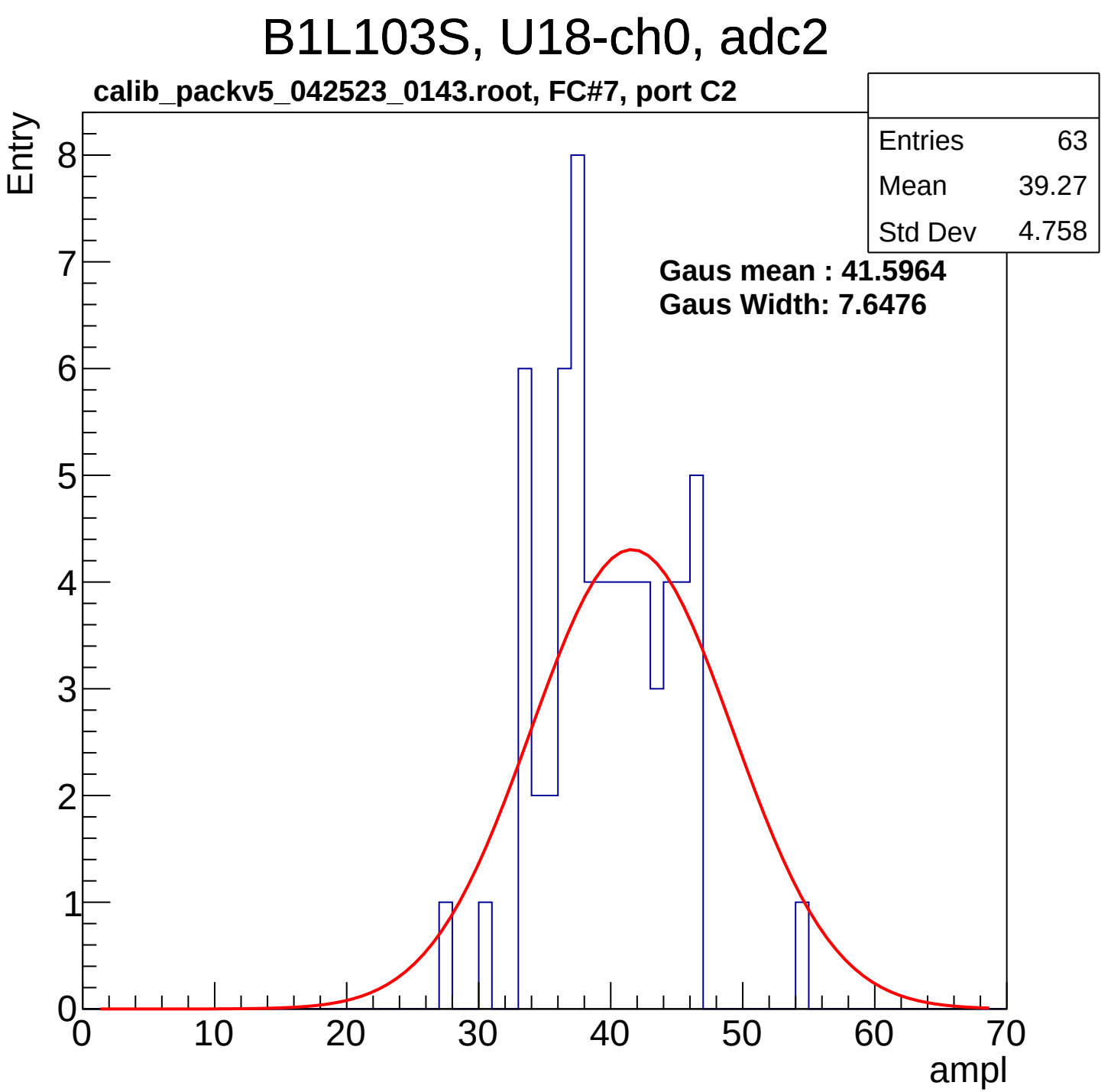
B1L103S, U18-ch0, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 39.27
Std Dev 4.758
Gaus mean : 41.5964
Gaus Width: 7.6476
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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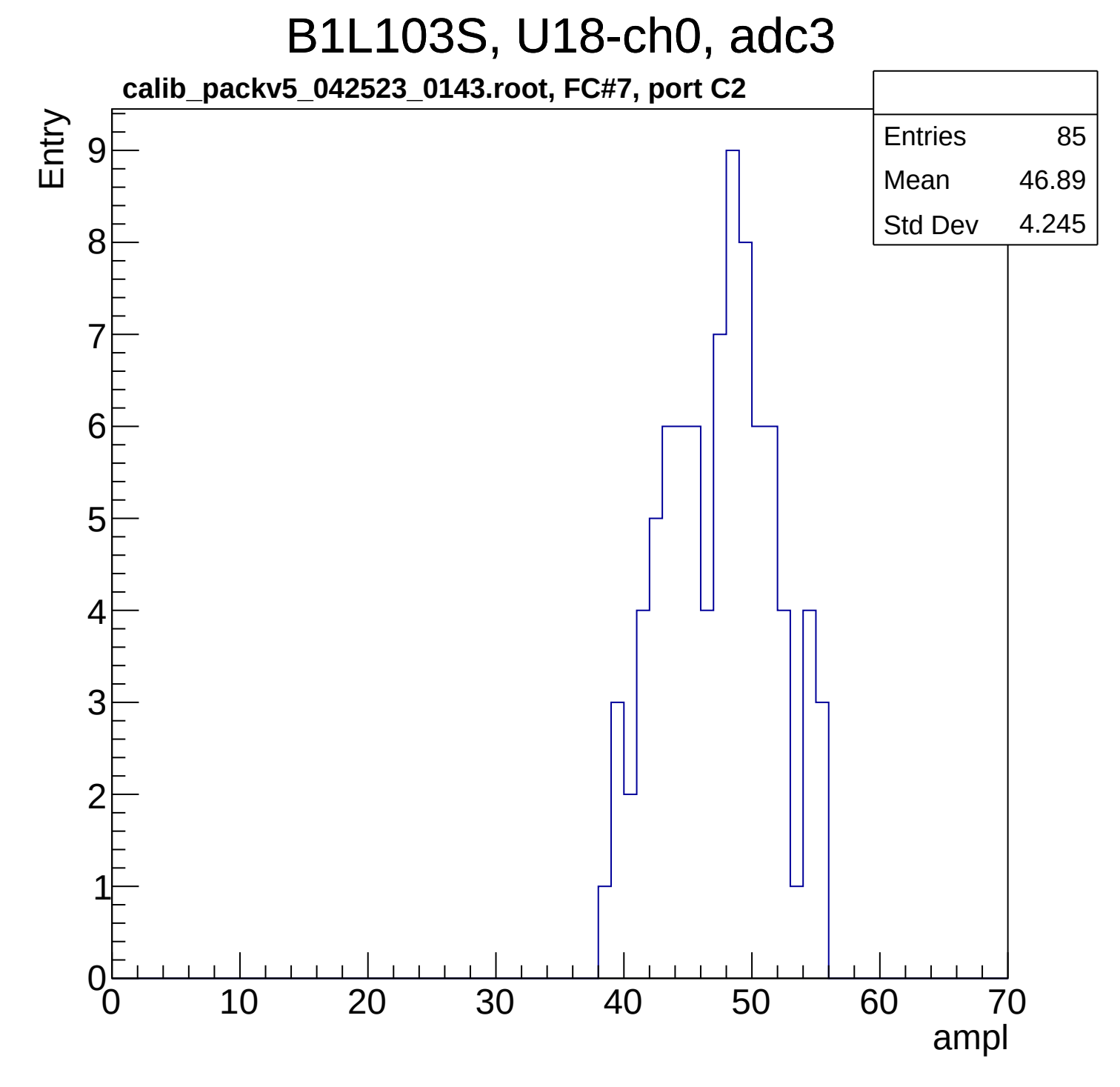
B1L103S, U18-ch0, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 85
Mean 46.89
Std Dev 4.245
Entry
ampl
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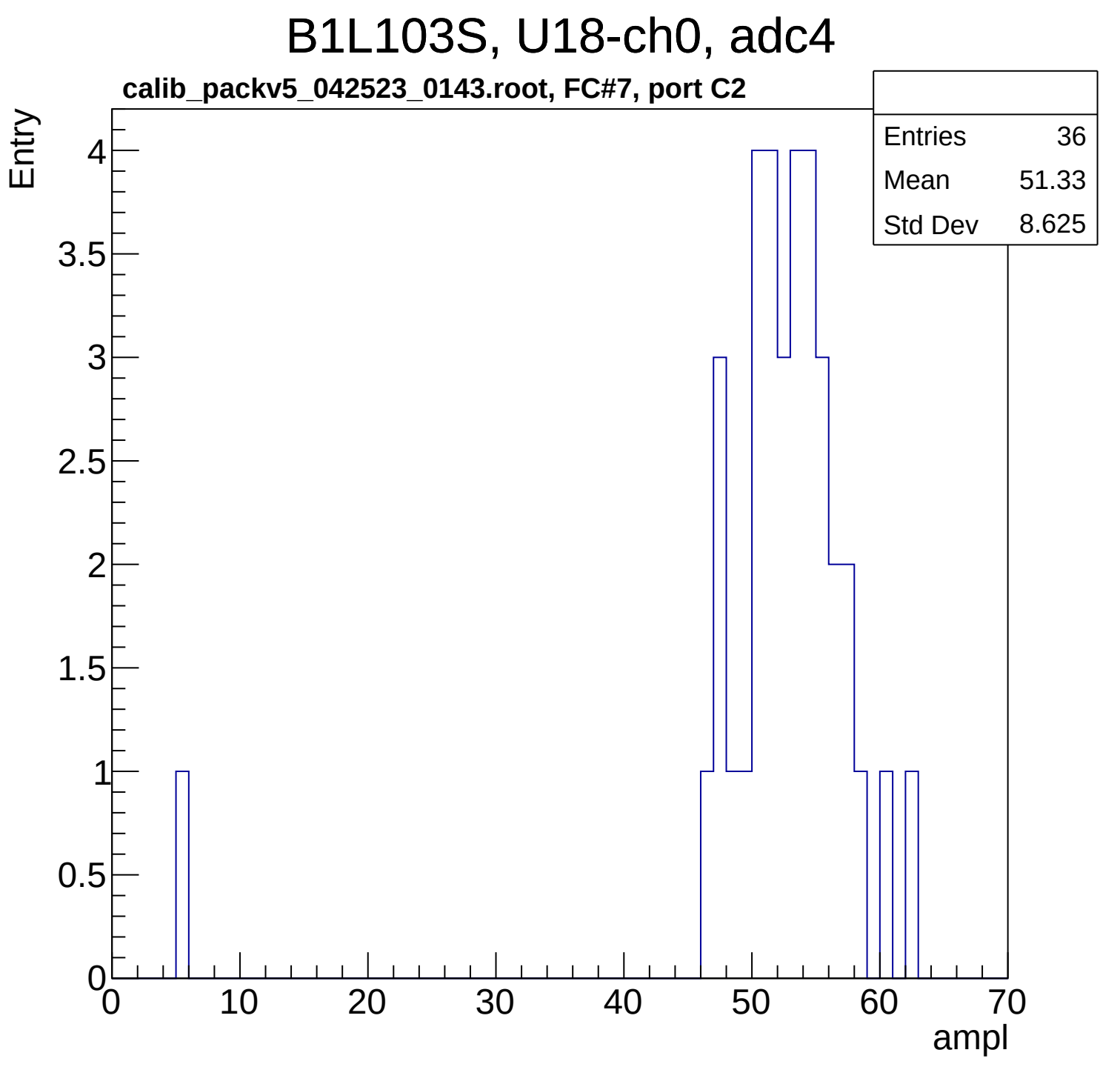
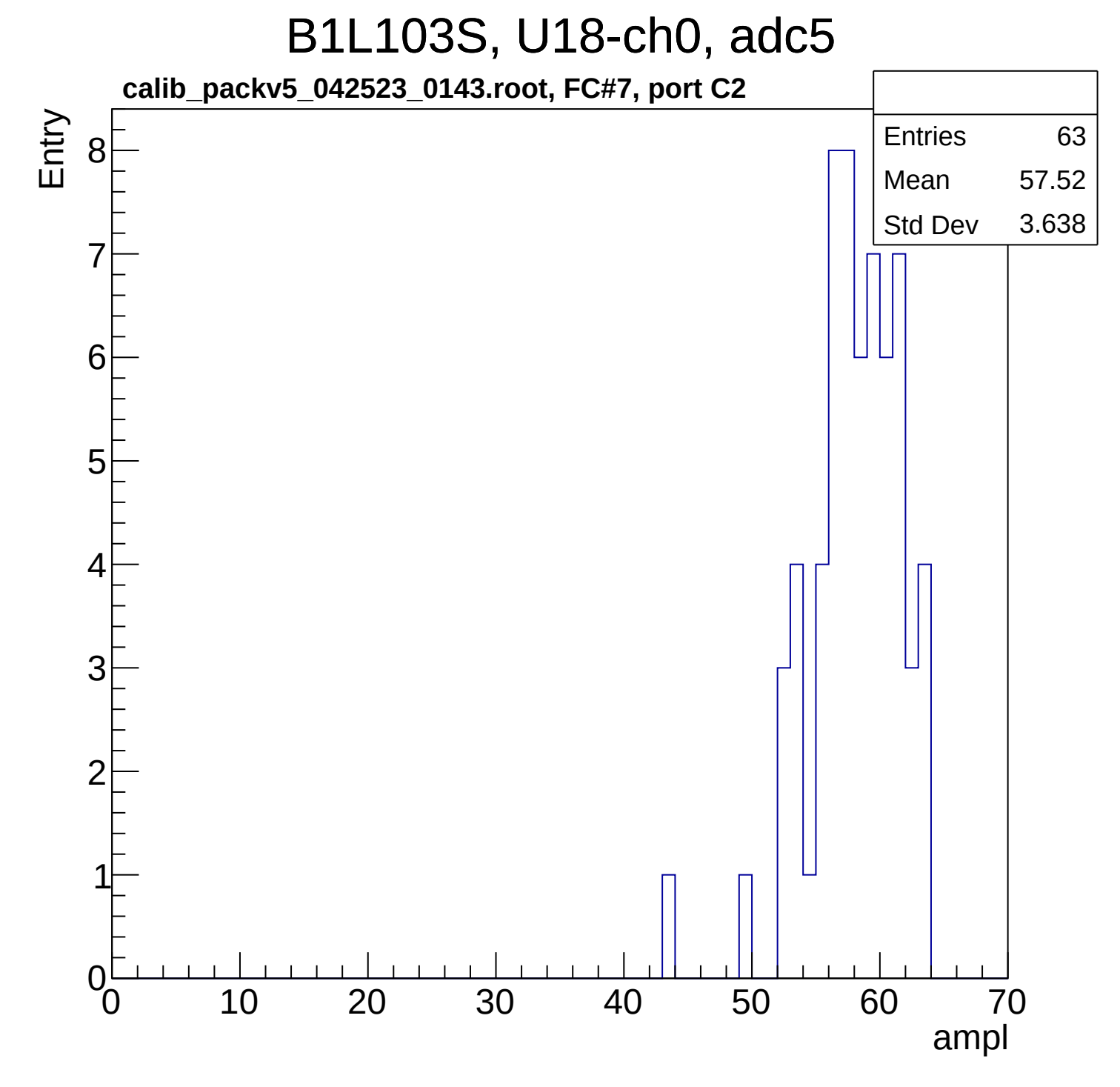
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch0, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 36
Mean 51.33
Std Dev 8.625
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U18-ch0, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 57.52
Std Dev 3.638
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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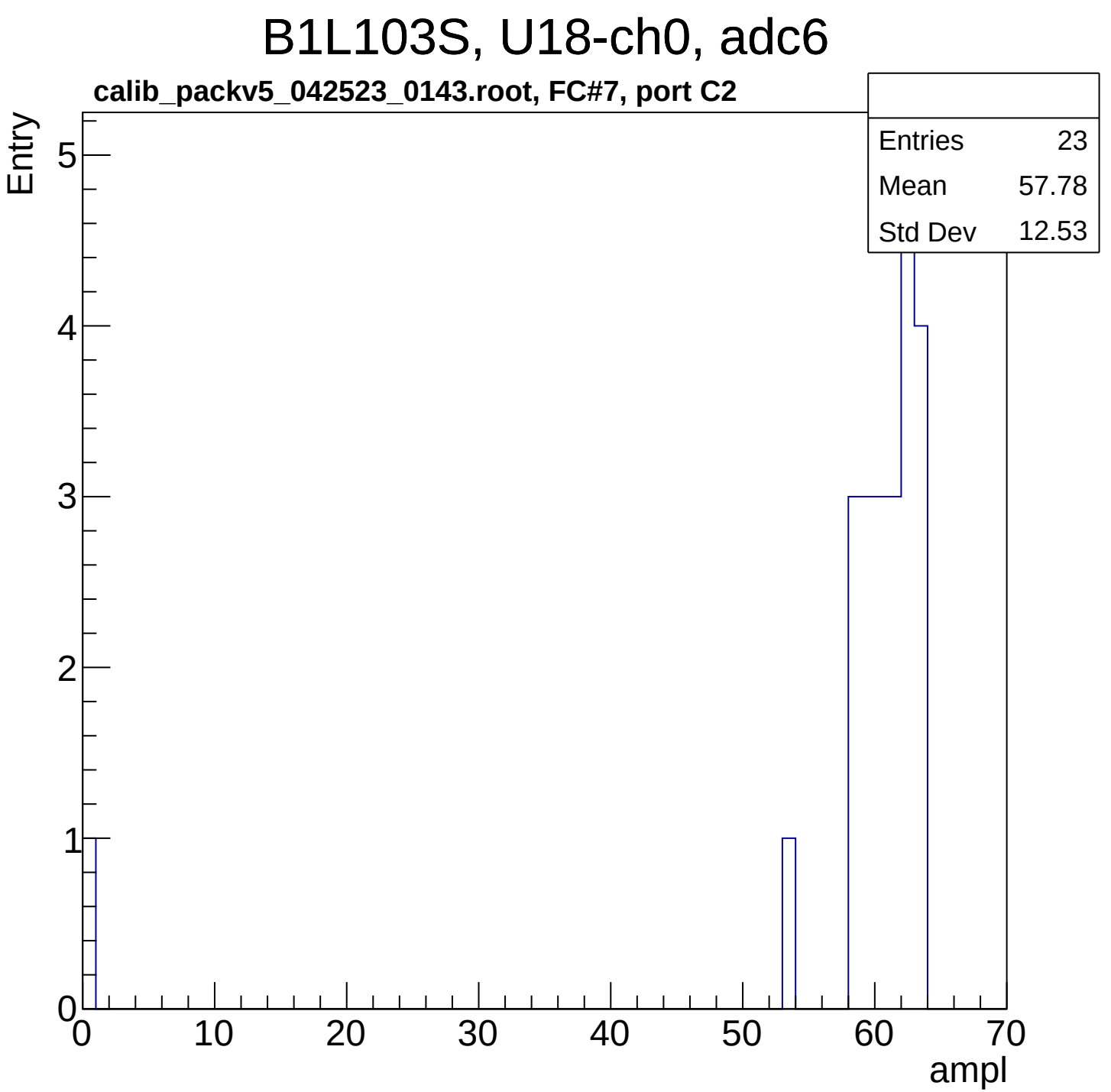
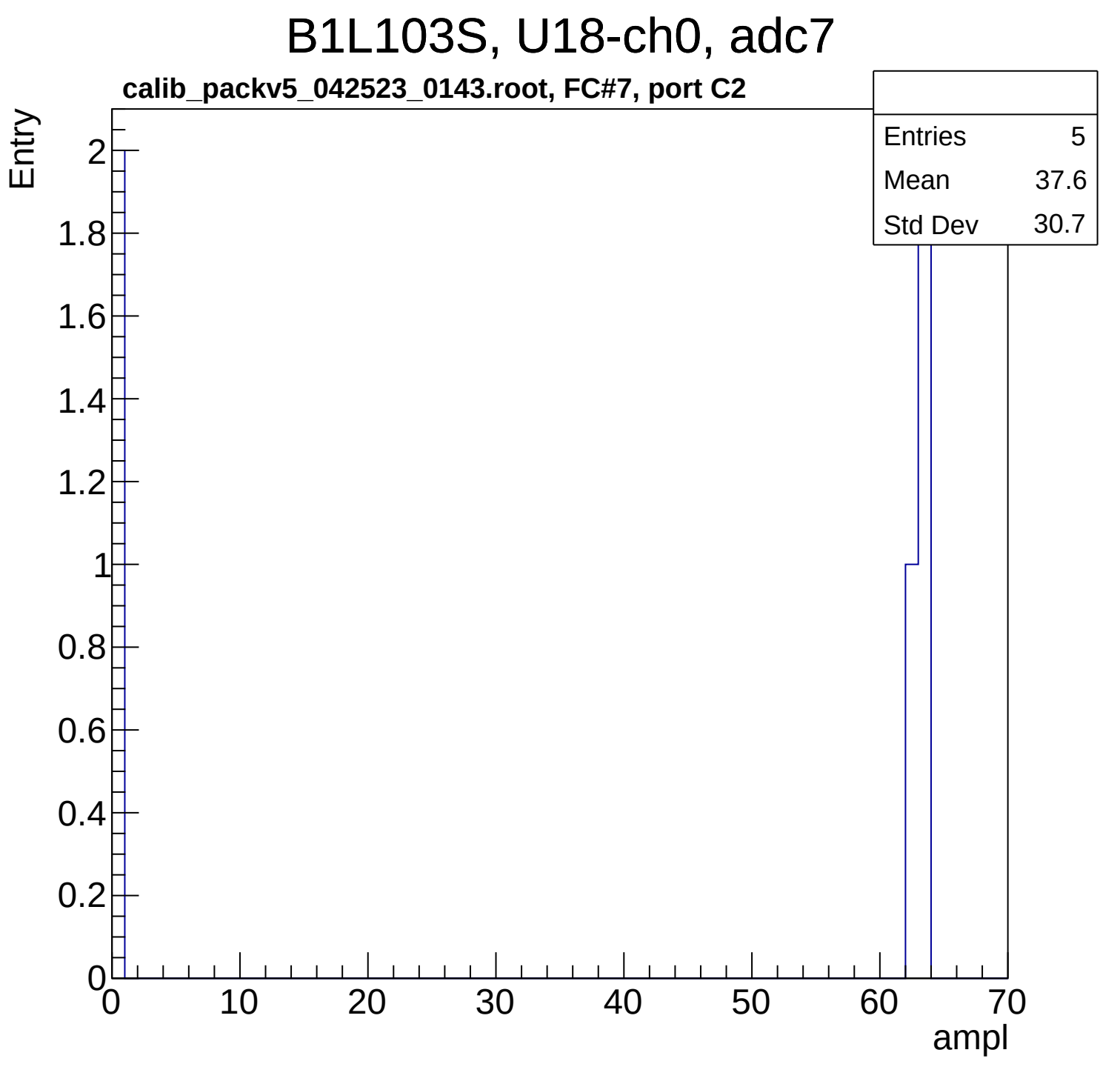
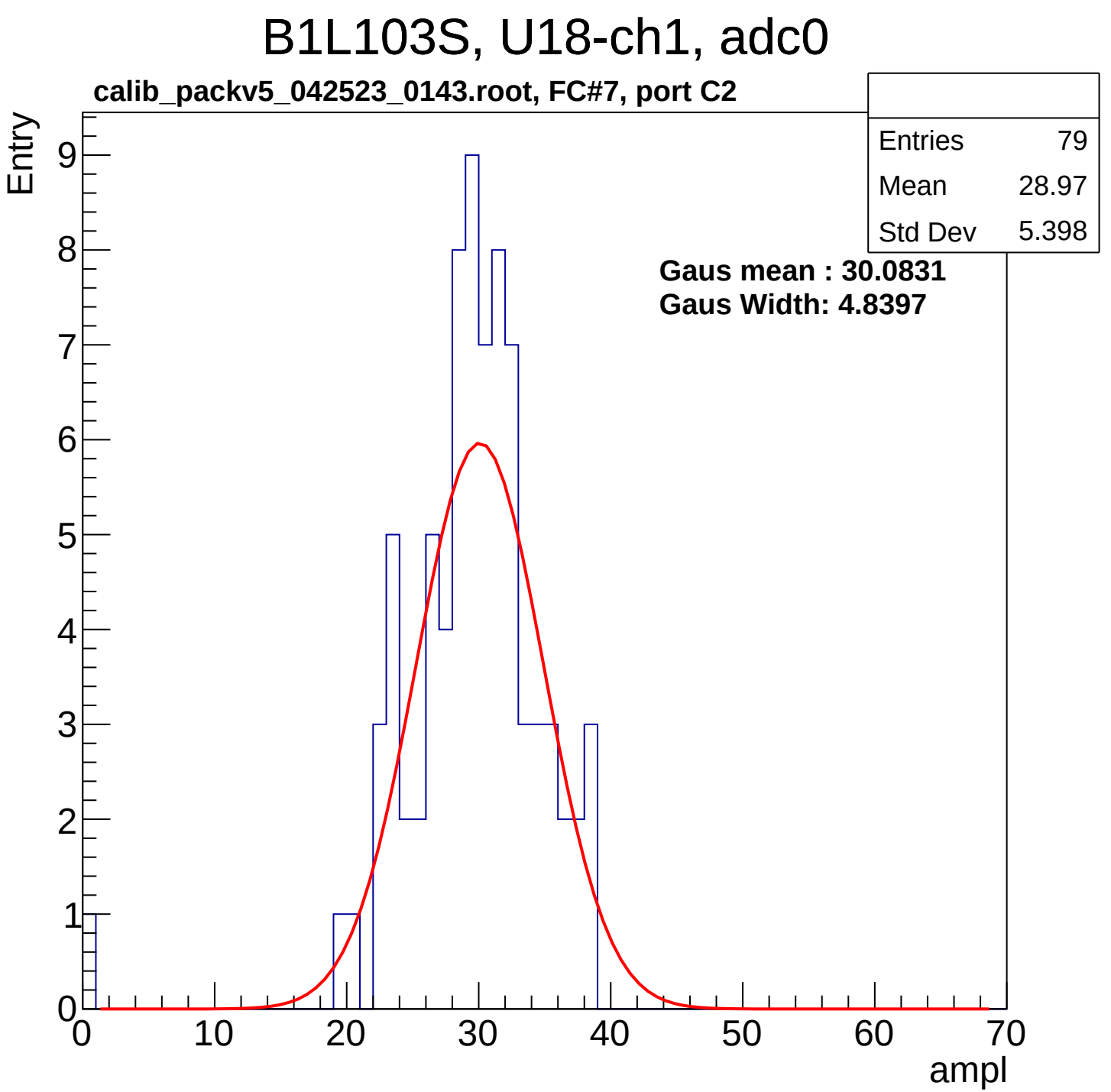

B1L103S, U18-ch0, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 23
Mean 57.78
Std Dev 12.53
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch0, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 5
Mean 37.6
Std Dev 30.7
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U18-ch1, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 79
Mean 28.97
Std Dev 5.398
Gaus mean : 30.0831
Gaus Width: 4.8397
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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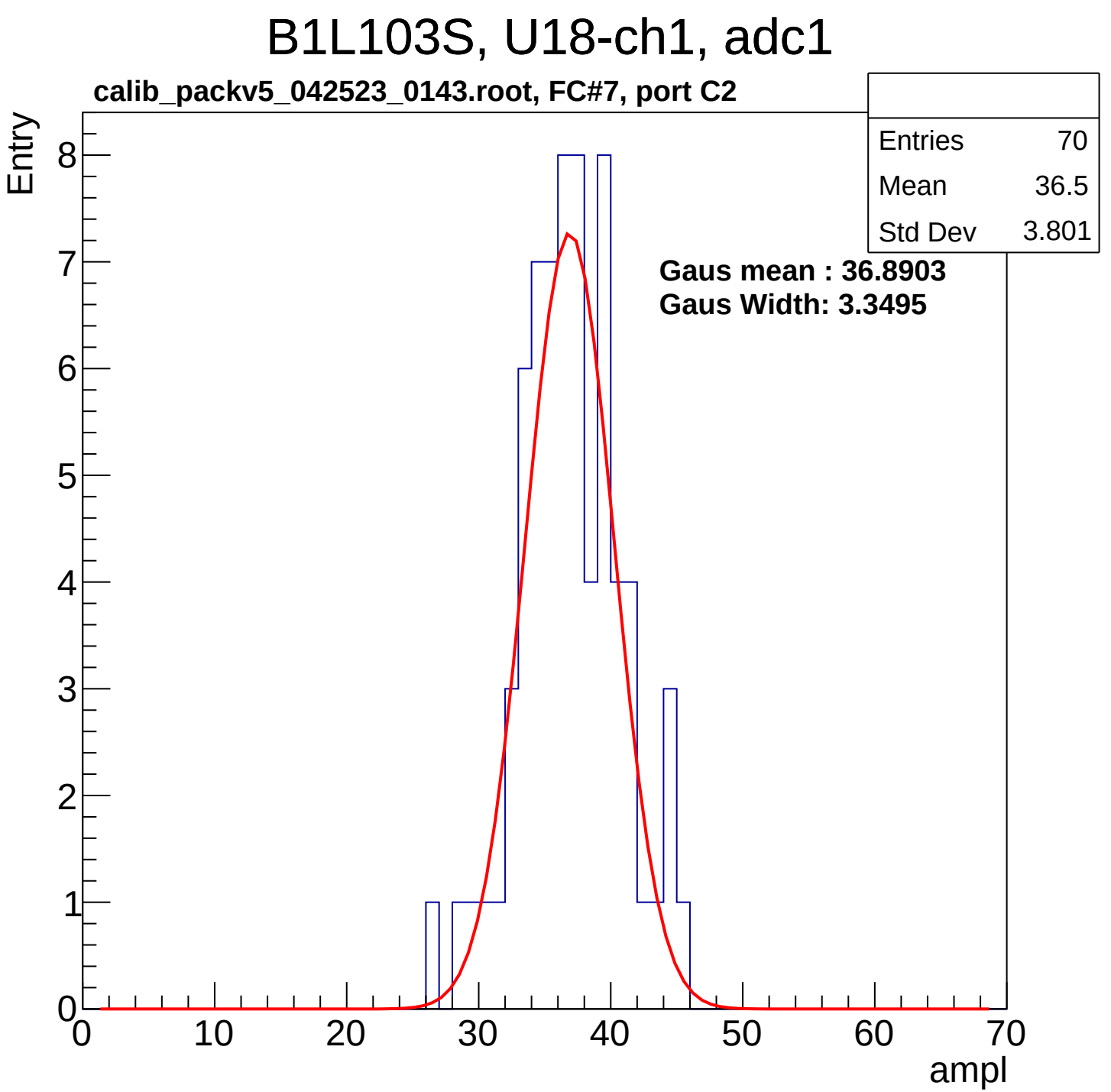
B1L103S, U18-ch1, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 36.5
Std Dev 3.801
Gaus mean : 36.8903
Gaus Width: 3.3495
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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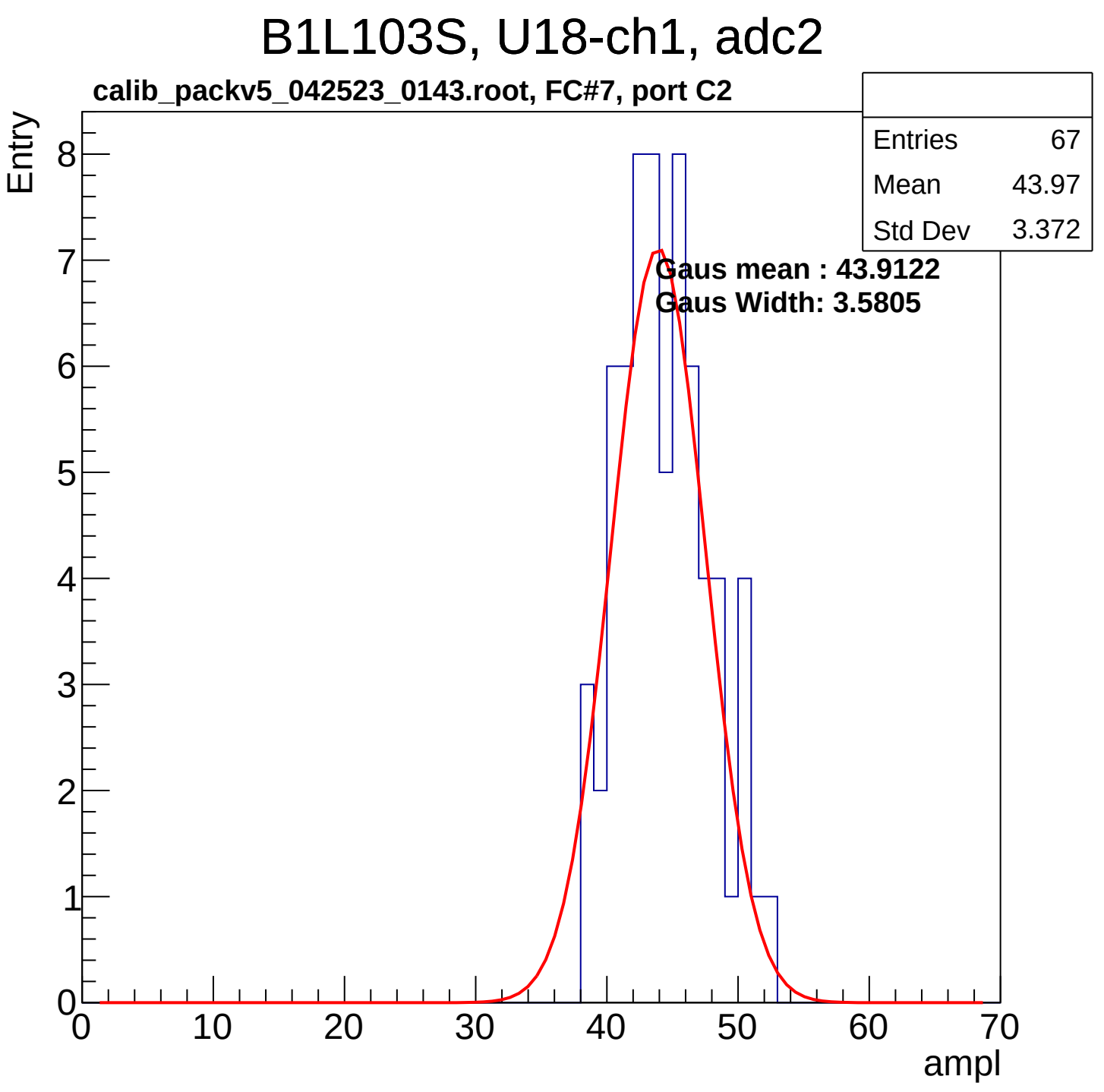
B1L103S, U18-ch1, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 43.97
Std Dev 3.372
Gaus mean : 43.9122
Gaus Width: 3.5805
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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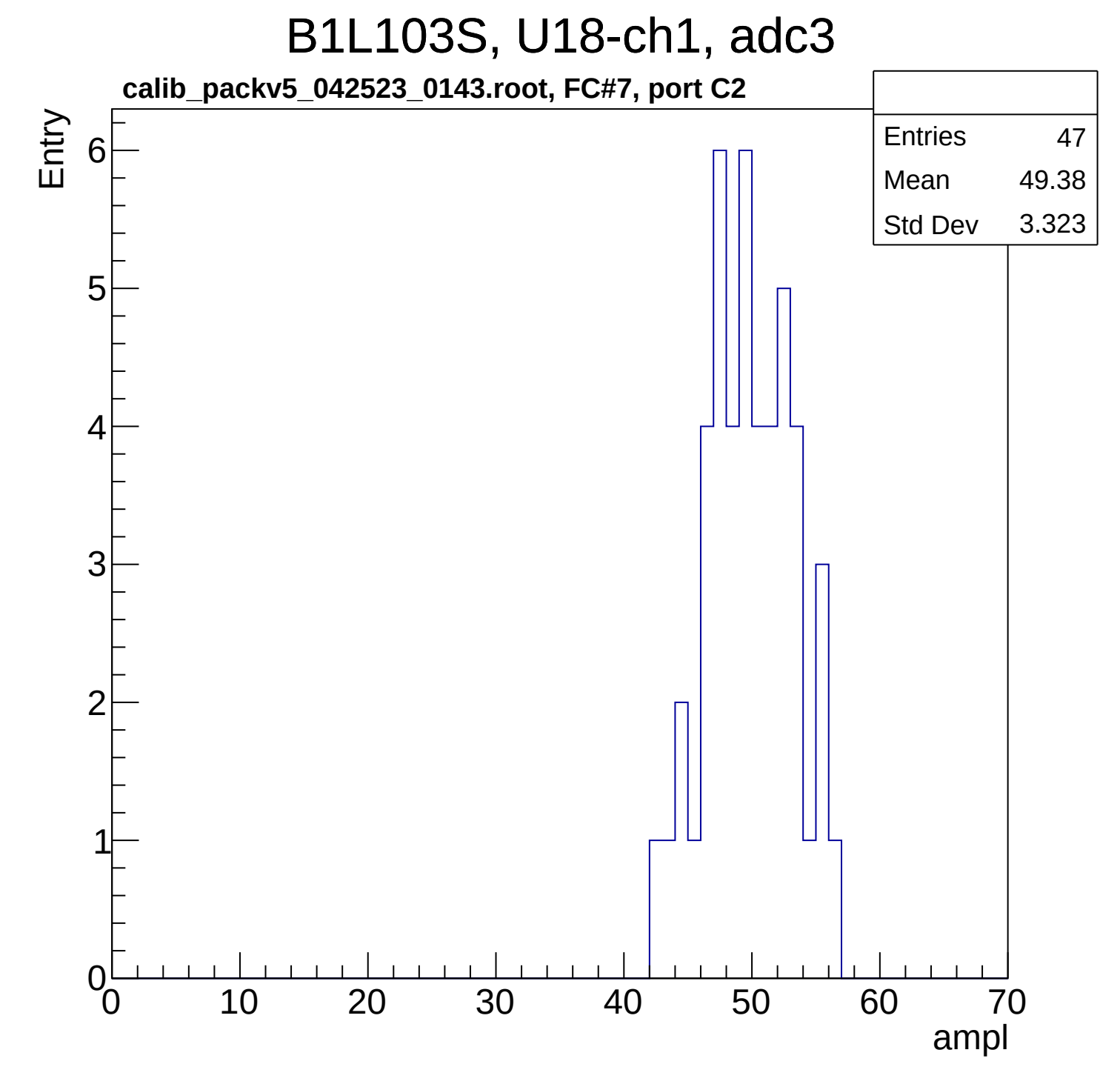
B1L103S, U18-ch1, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 47
Mean 49.38
Std Dev 3.323
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
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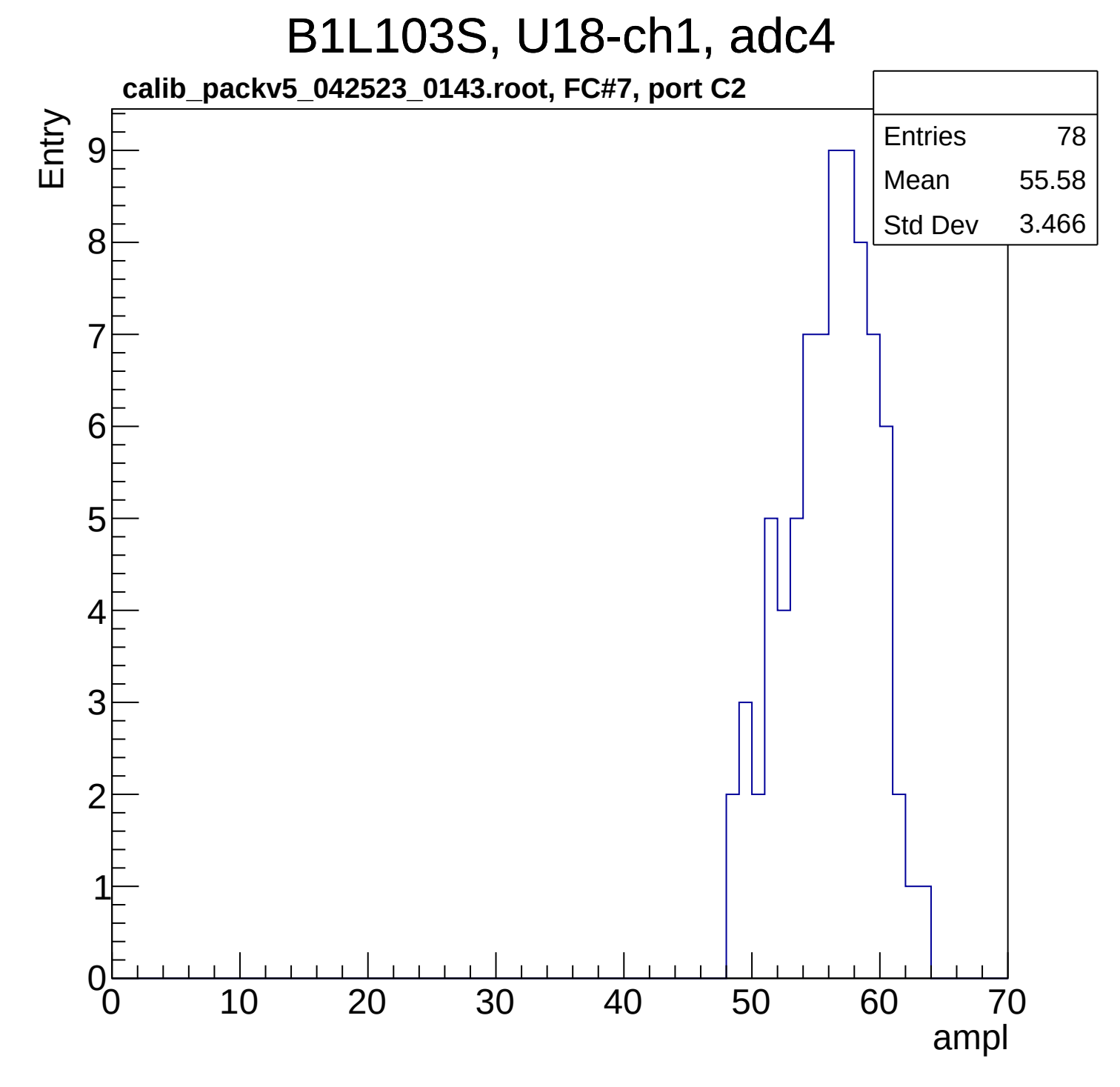
B1L103S, U18-ch1, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 78
Mean 55.58
Std Dev 3.466
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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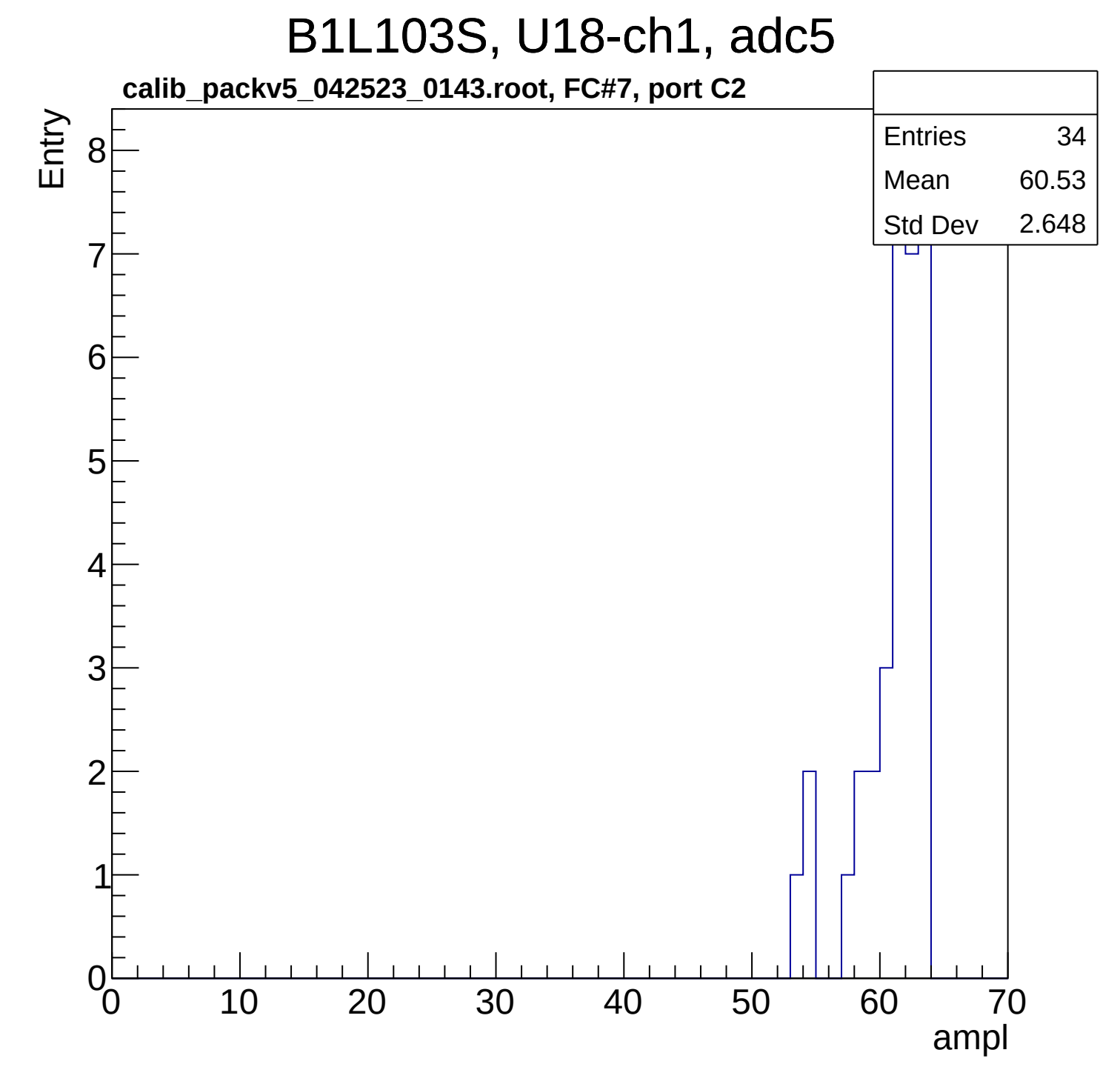
B1L103S, U18-ch1, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 34
Mean 60.53
Std Dev 2.648
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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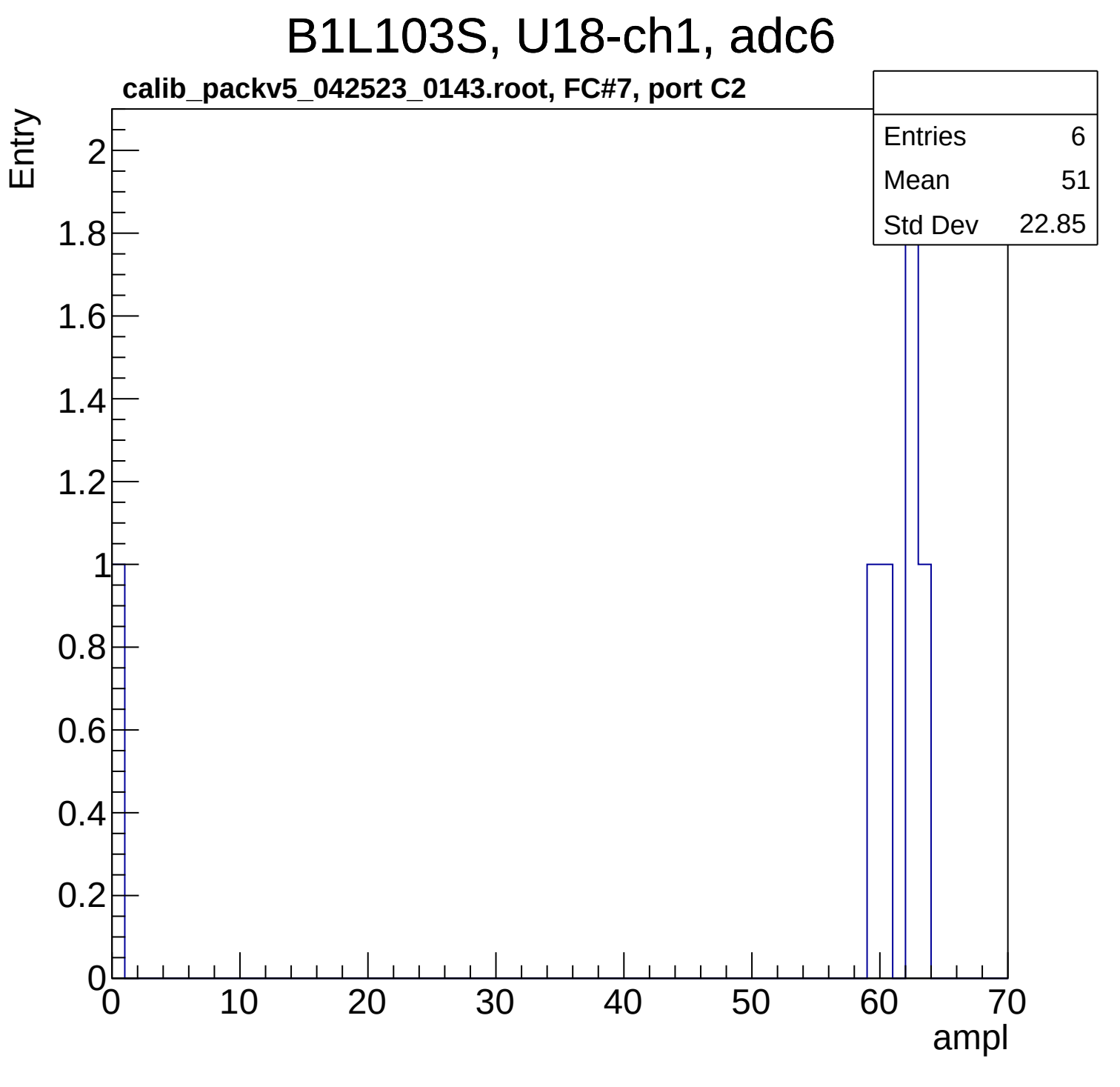
B1L103S, U18-ch1, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 6
Mean 51
Std Dev 22.85
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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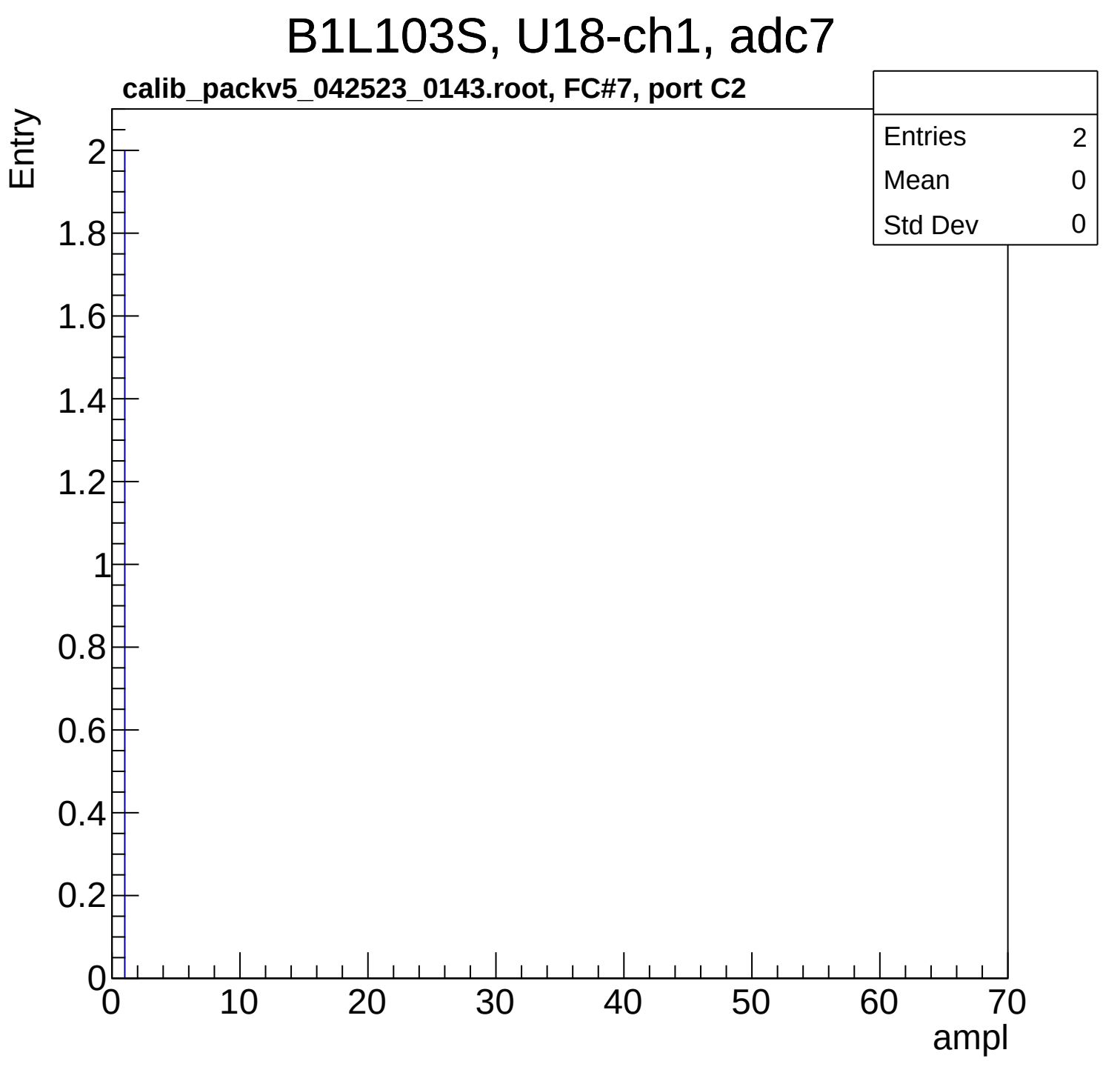
B1L103S, U18-ch1, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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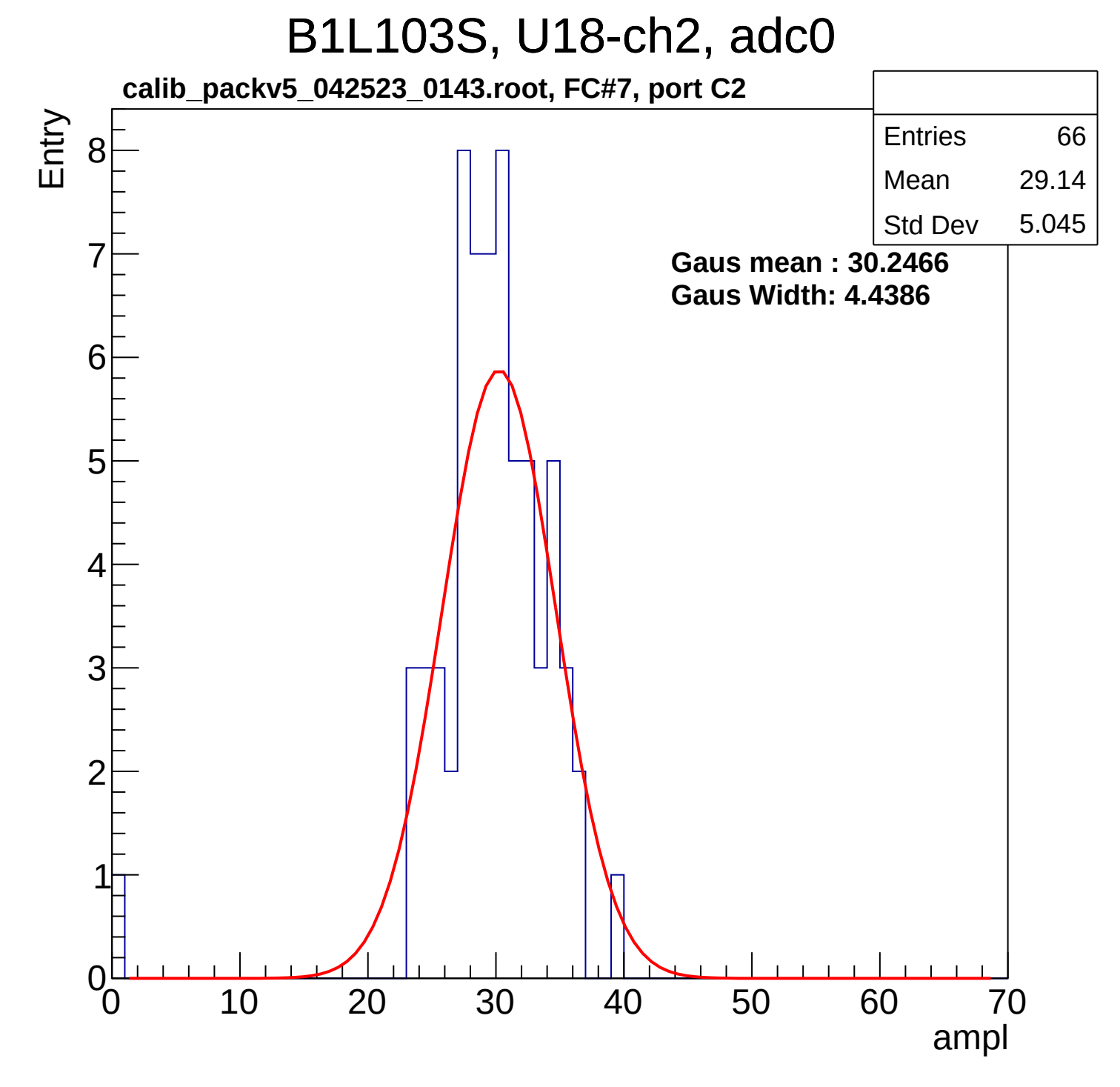
B1L103S, U18-ch2, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 29.14
Std Dev 5.045
Gaus mean : 30.2466
Gaus Width: 4.4386
Entry
ampl
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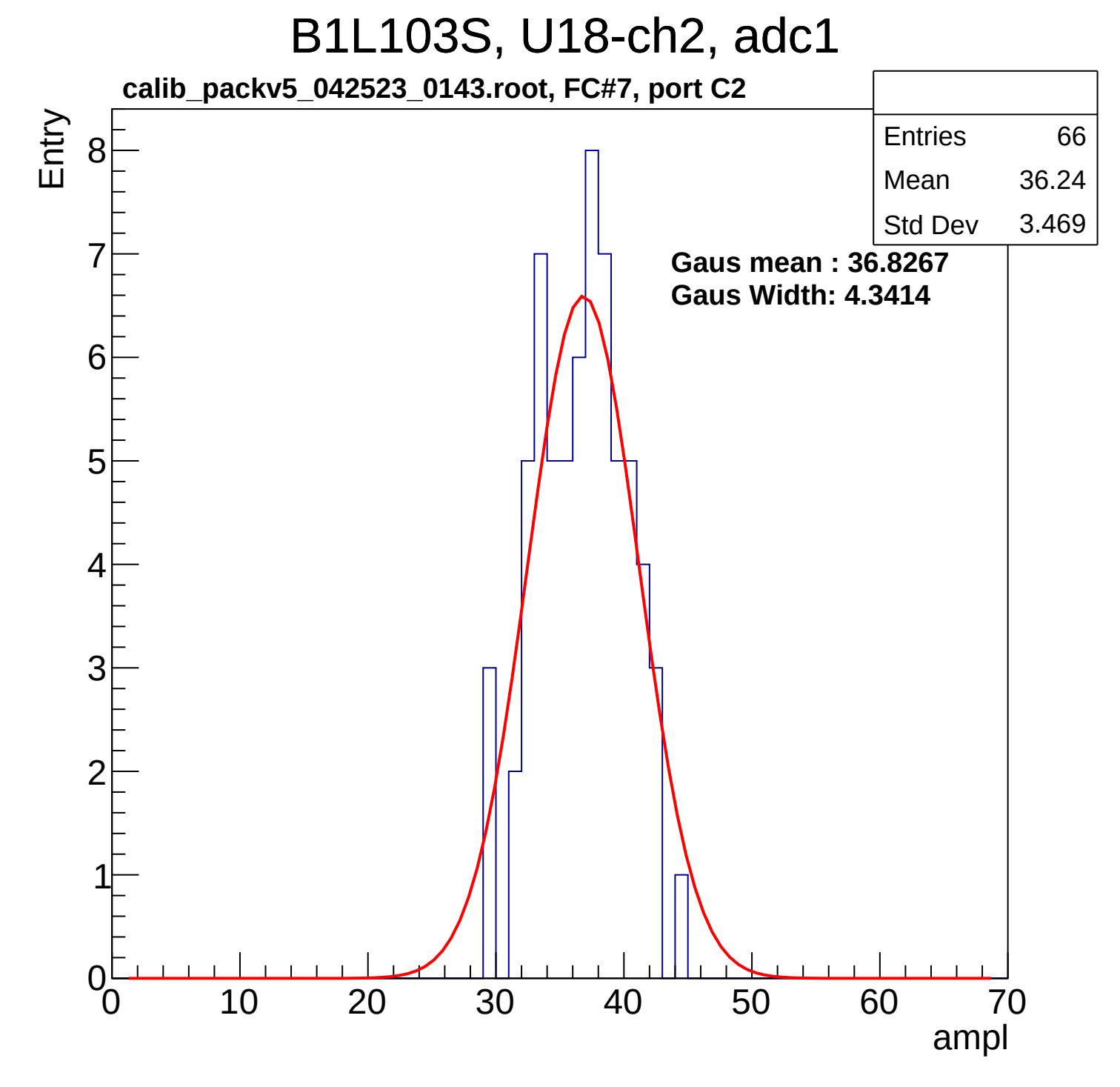
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch2, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 36.24
Std Dev 3.469
Gaus mean : 36.8267
Gaus Width: 4.3414
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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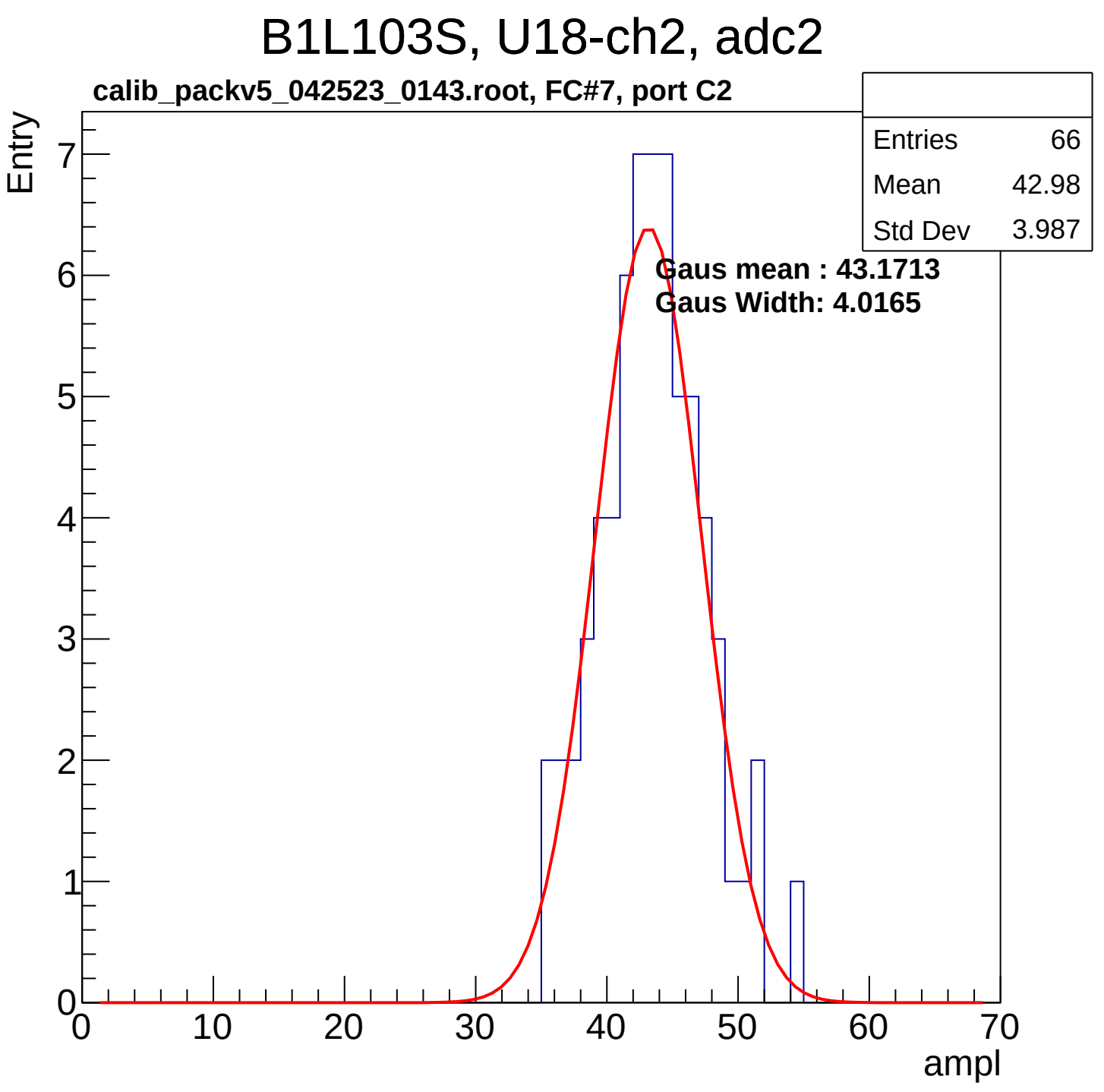
B1L103S, U18-ch2, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 42.98
Std Dev 3.987
Gaus mean : 43.1713
Gaus Width: 4.0165
Entry
ampl
0
1
2
3
4
5
6
7
0
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40
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60
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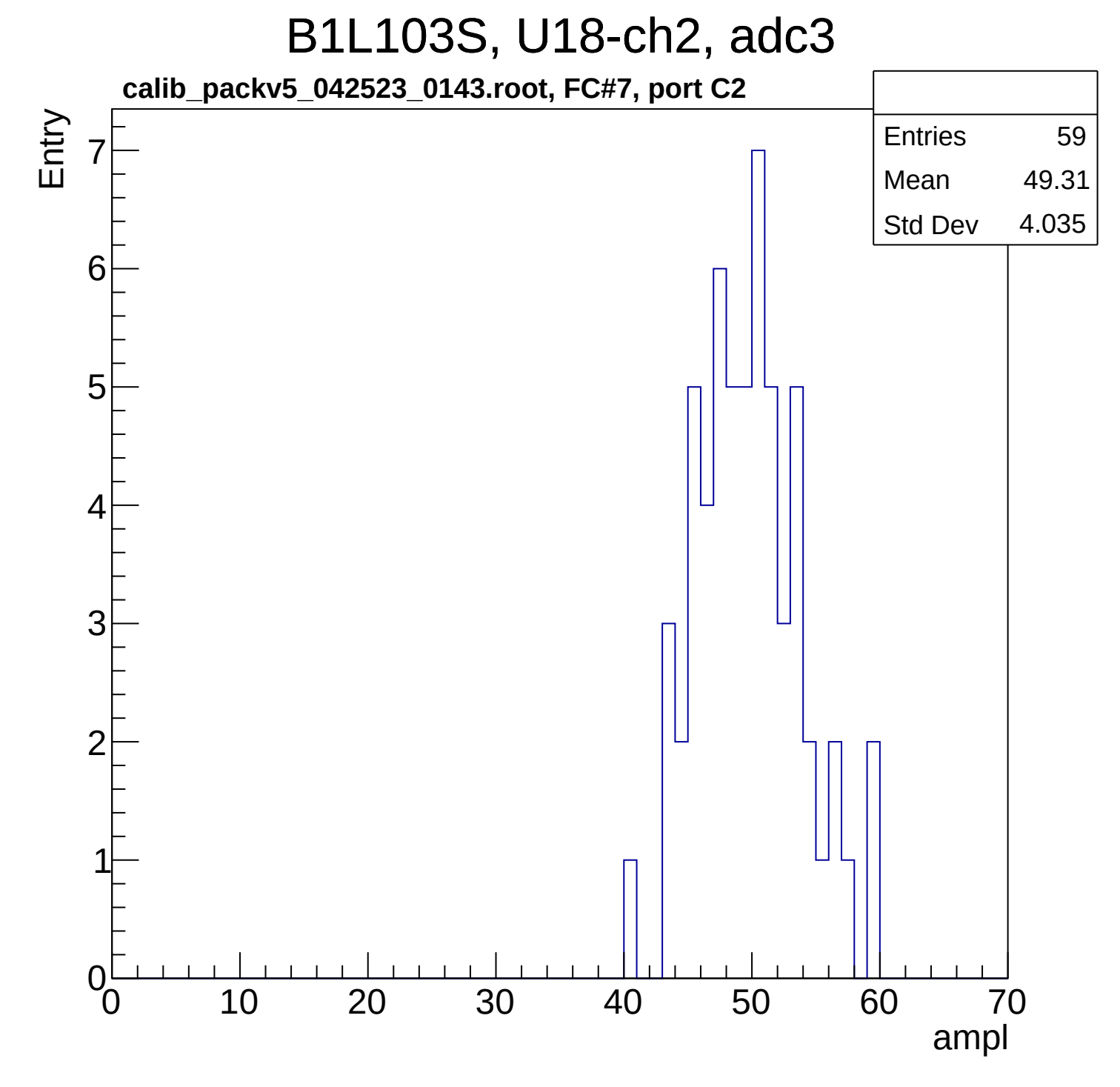
B1L103S, U18-ch2, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 49.31
Std Dev 4.035
Entry
ampl
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2
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4
5
6
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0
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20
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40
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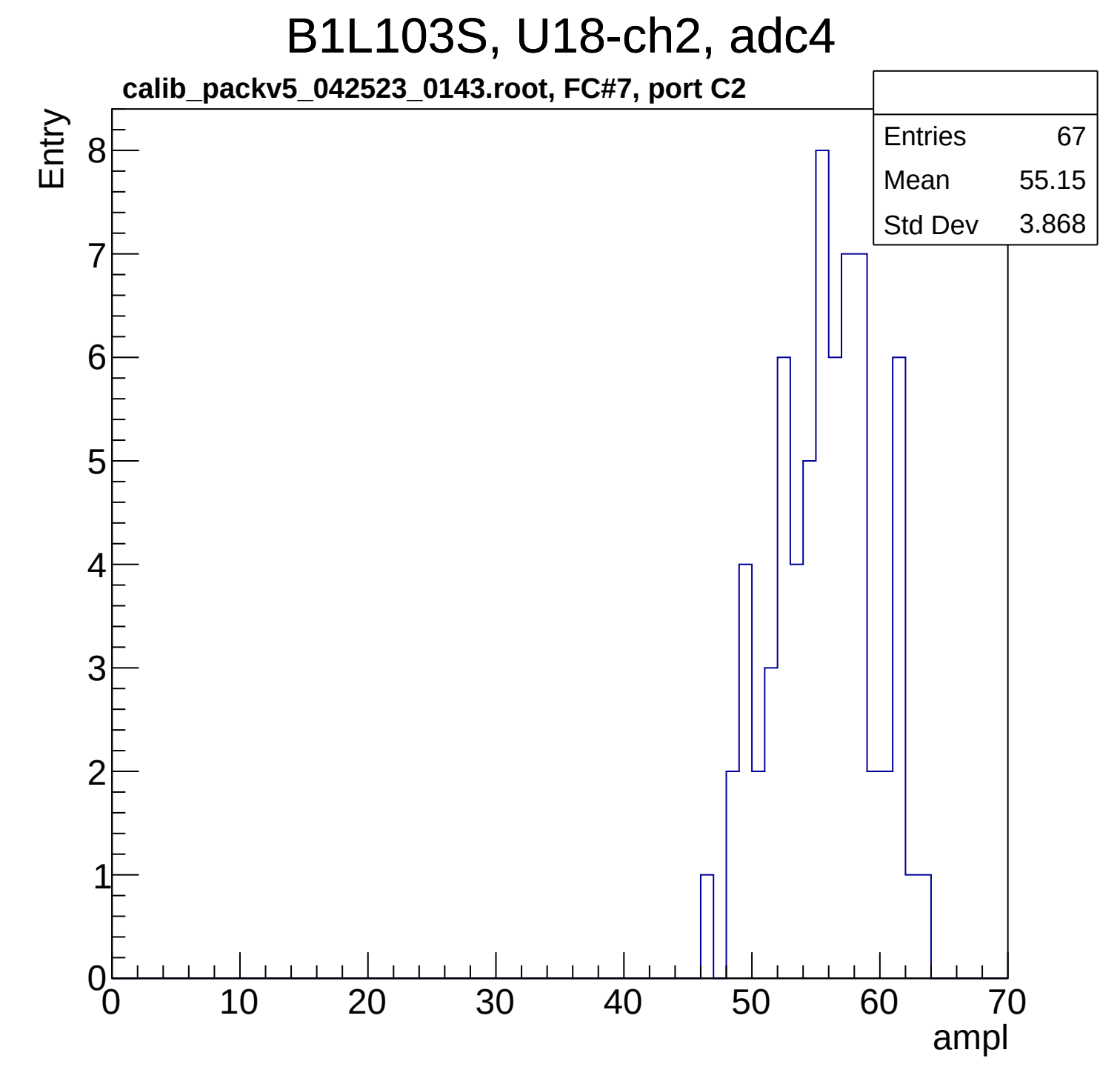
B1L103S, U18-ch2, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 55.15
Std Dev 3.868
Entry
ampl
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1
2
3
4
5
6
7
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0
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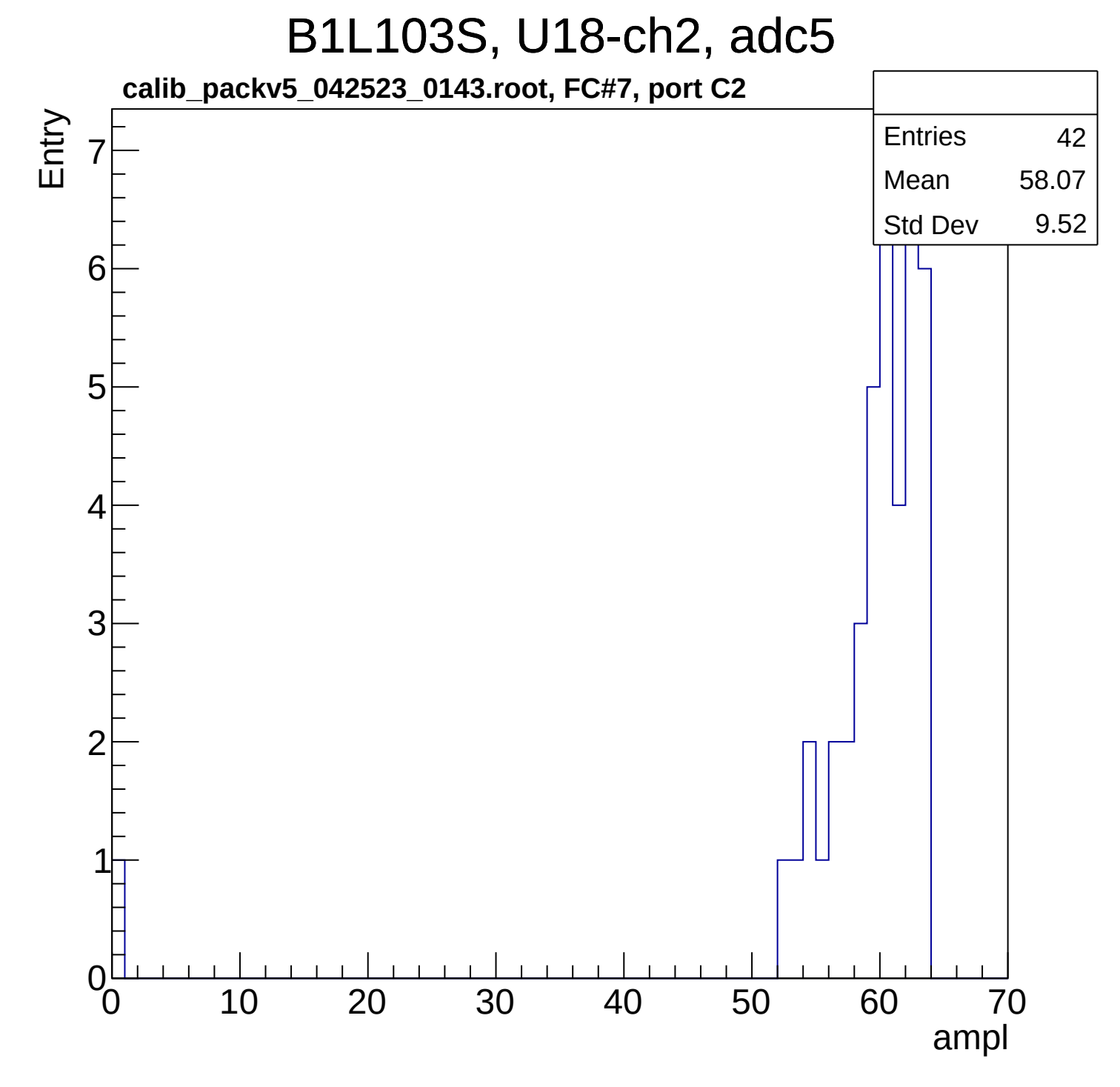
B1L103S, U18-ch2, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 42
Mean 58.07
Std Dev 9.52
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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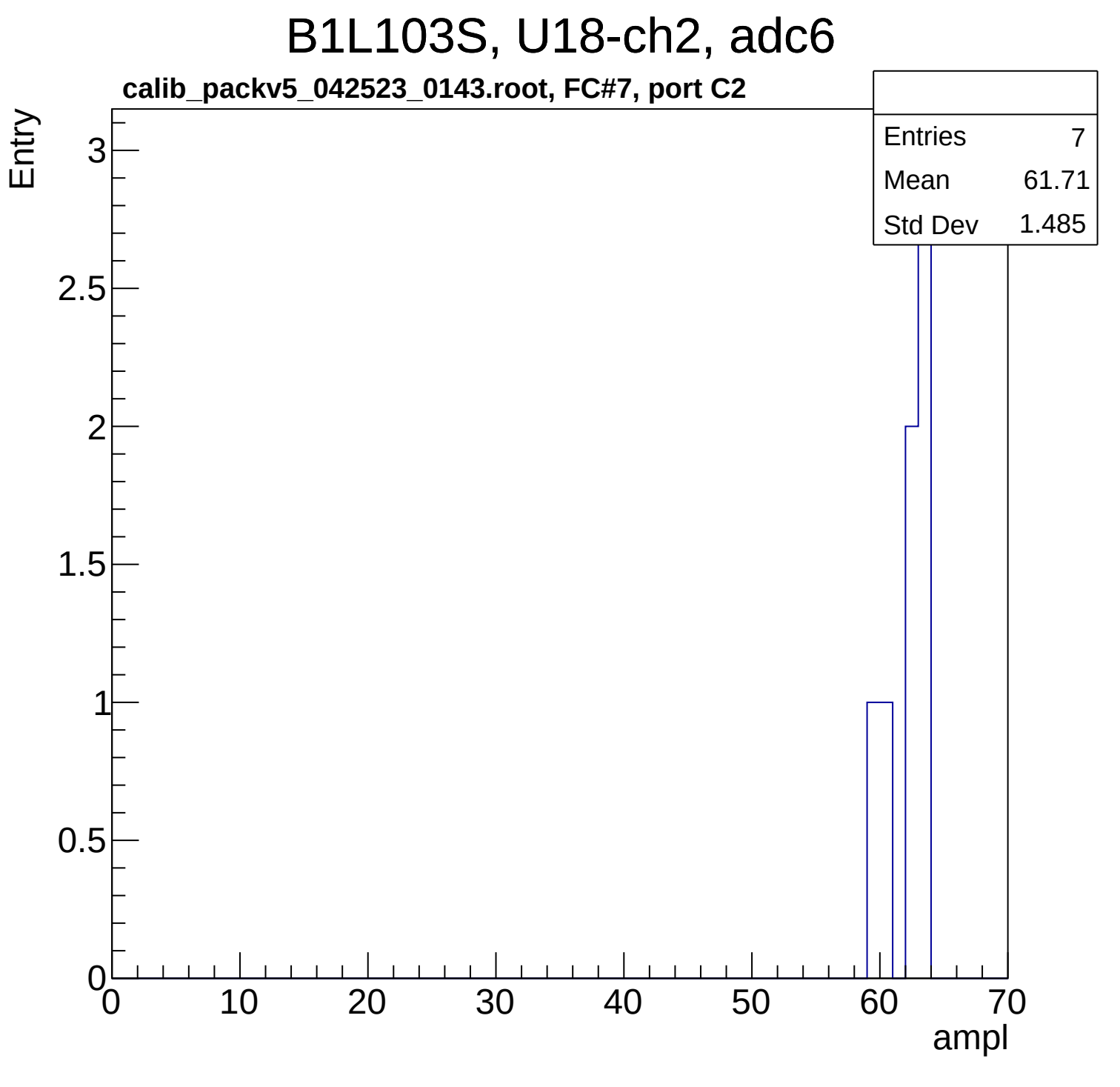
B1L103S, U18-ch2, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 7
Mean 61.71
Std Dev 1.485
Entry
ampl
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1
1.5
2
2.5
3
0
10
20
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40
50
60
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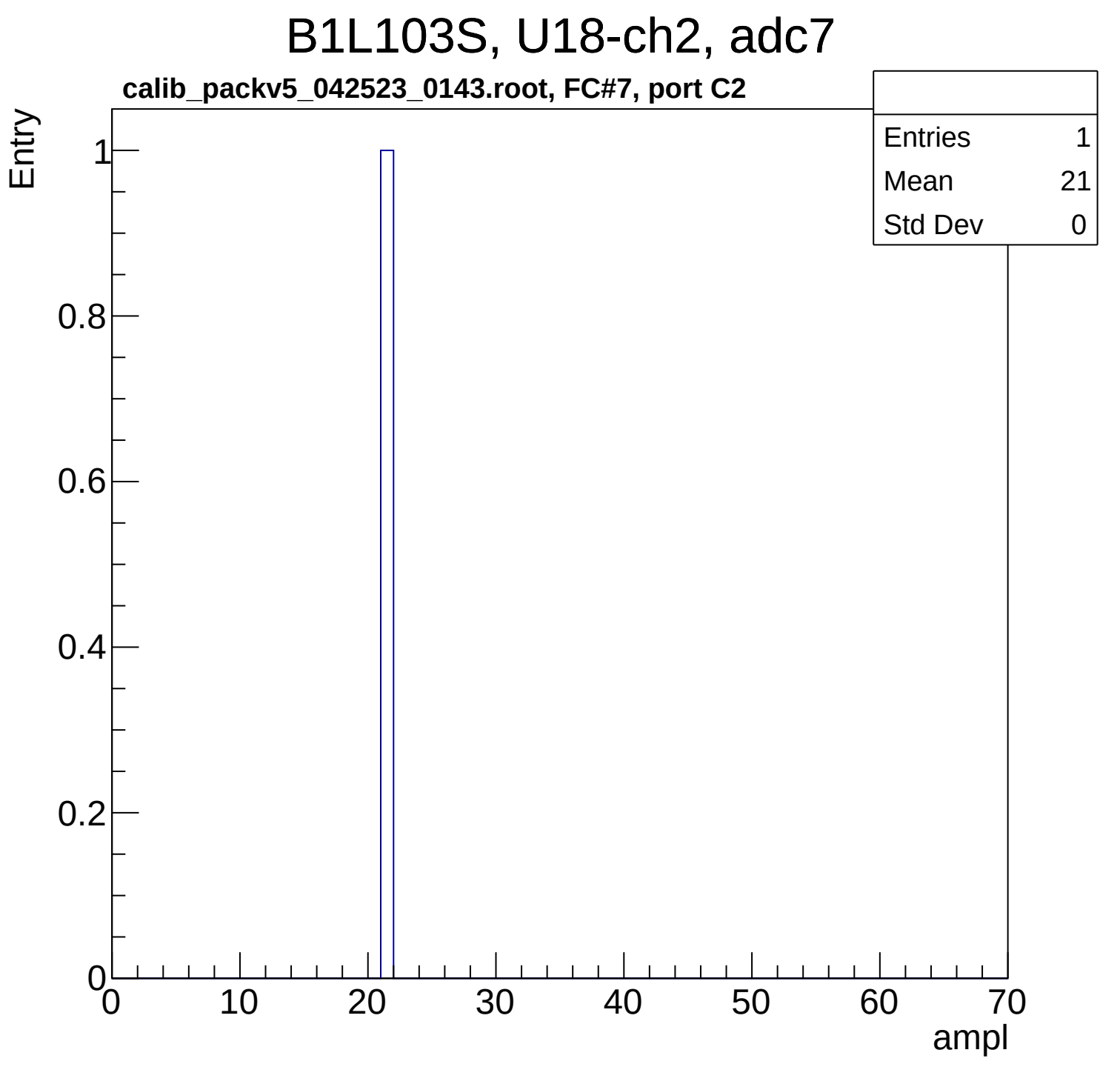
B1L103S, U18-ch2, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 21
Std Dev 0
Entry
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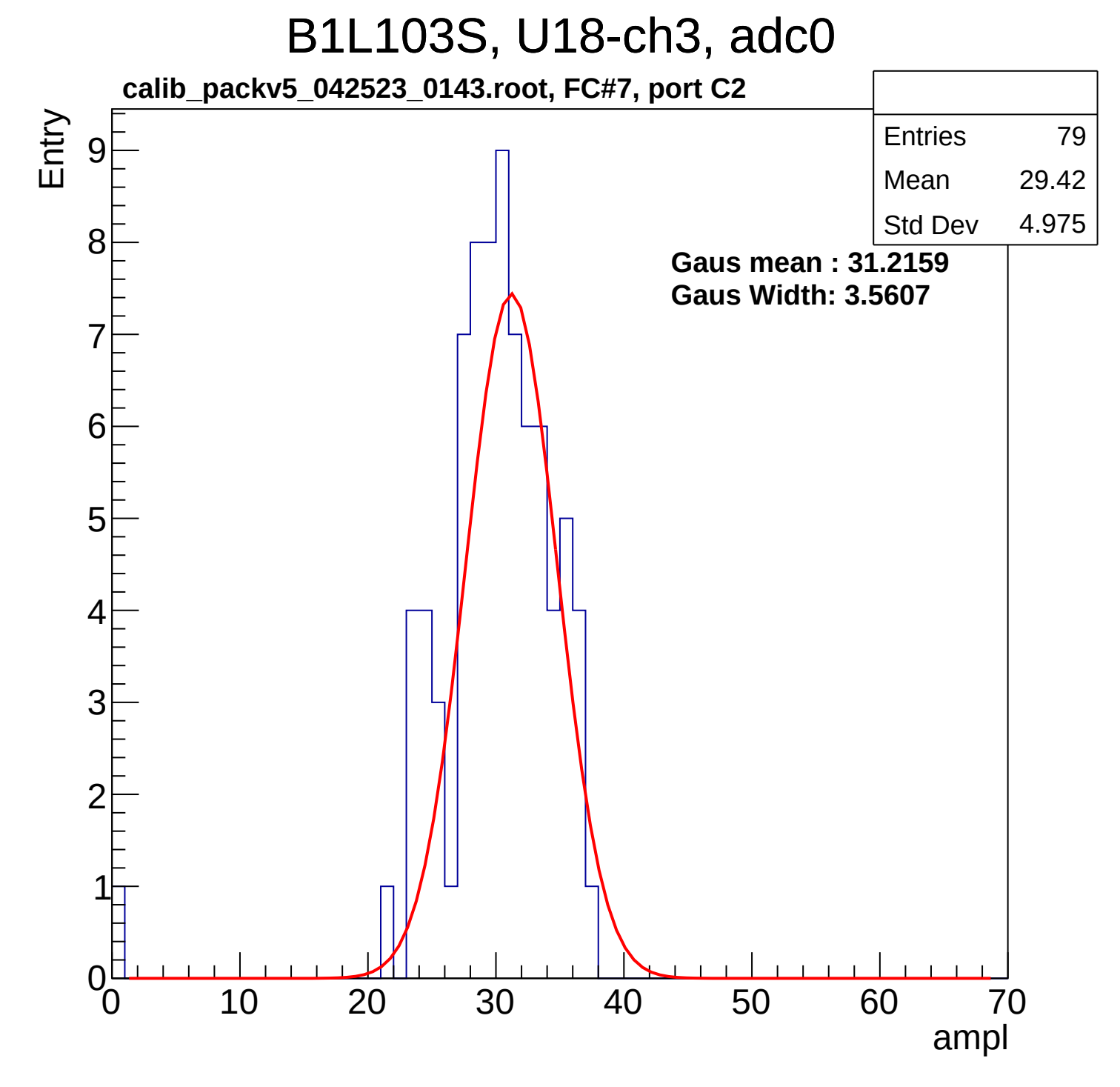
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch3, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 79
Mean 29.42
Std Dev 4.975
Gaus mean : 31.2159
Gaus Width: 3.5607
Entry
ampl
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2
3
4
5
6
7
8
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0
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60
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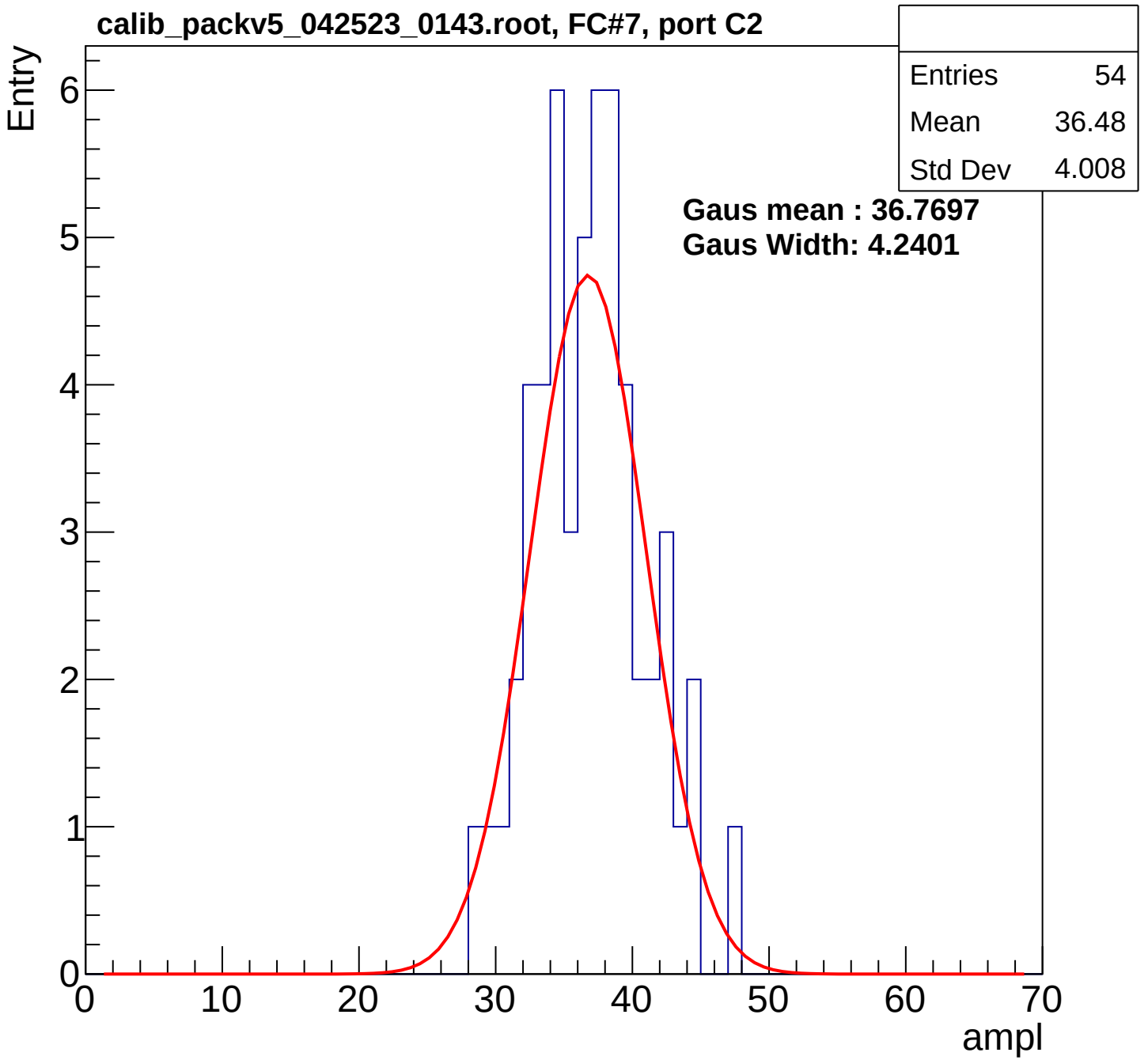
B1L103S, U18-ch3, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 54
Mean 36.48
Std Dev 4.008
Gaus mean : 36.7697
Gaus Width: 4.2401
Entry
ampl
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2
3
4
5
6
0
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20
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40
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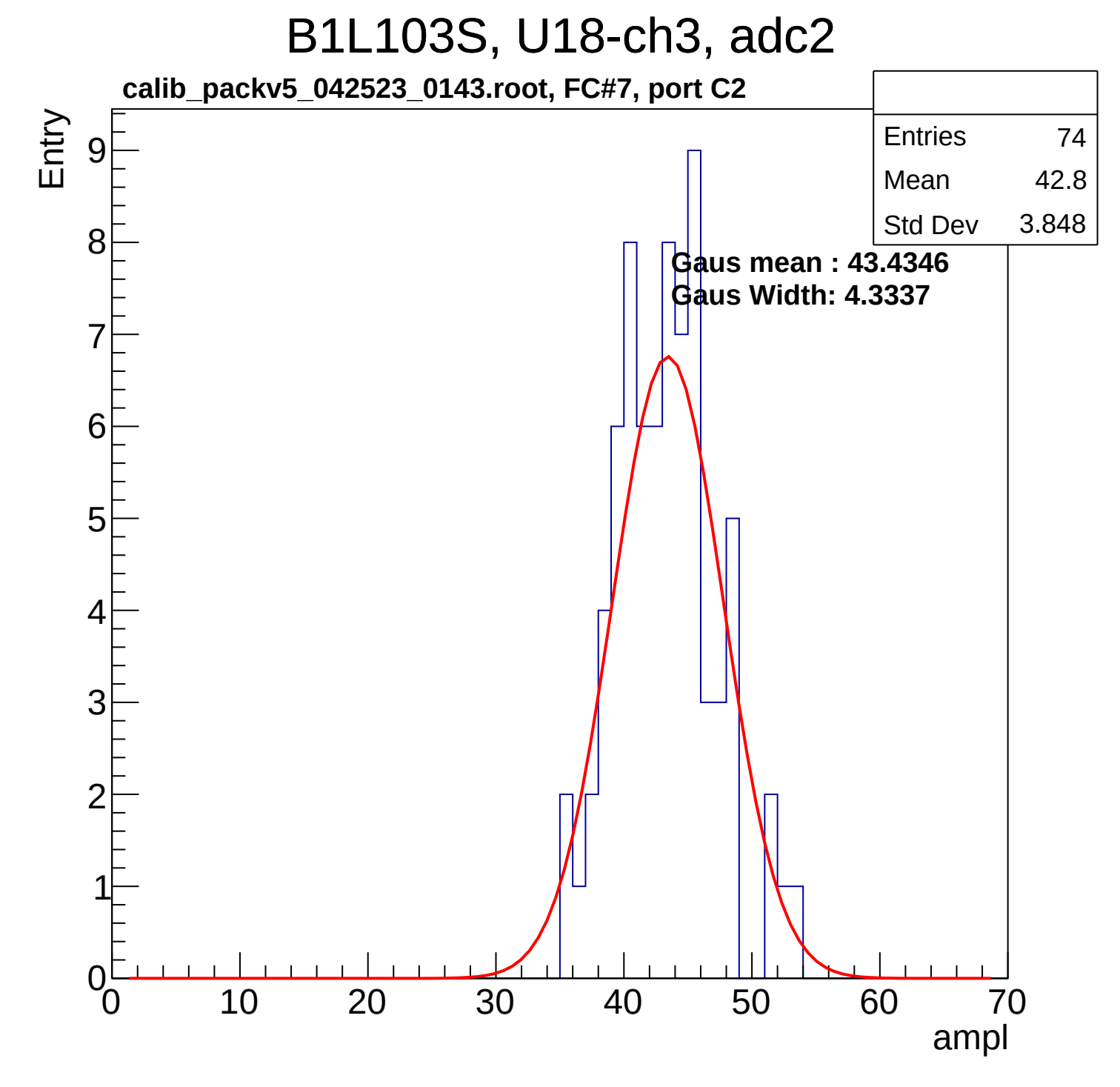
60
70


B1L103S, U18-ch3, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 74
Mean 42.8
Std Dev 3.848
Gaus mean : 43.4346
Gaus Width: 4.3337
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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20
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60
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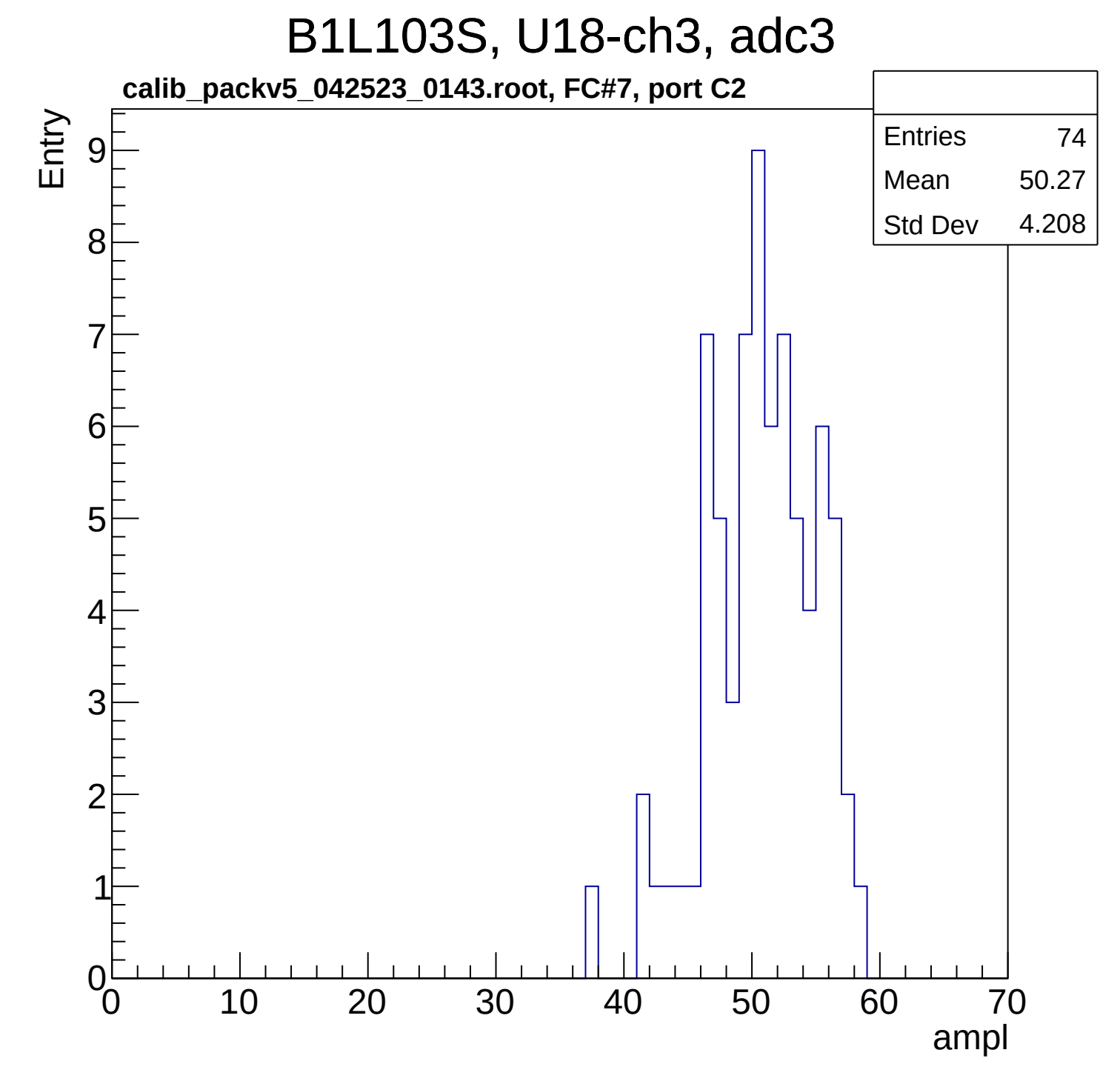
B1L103S, U18-ch3, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 74
Mean 50.27
Std Dev 4.208
Entry
ampl
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3
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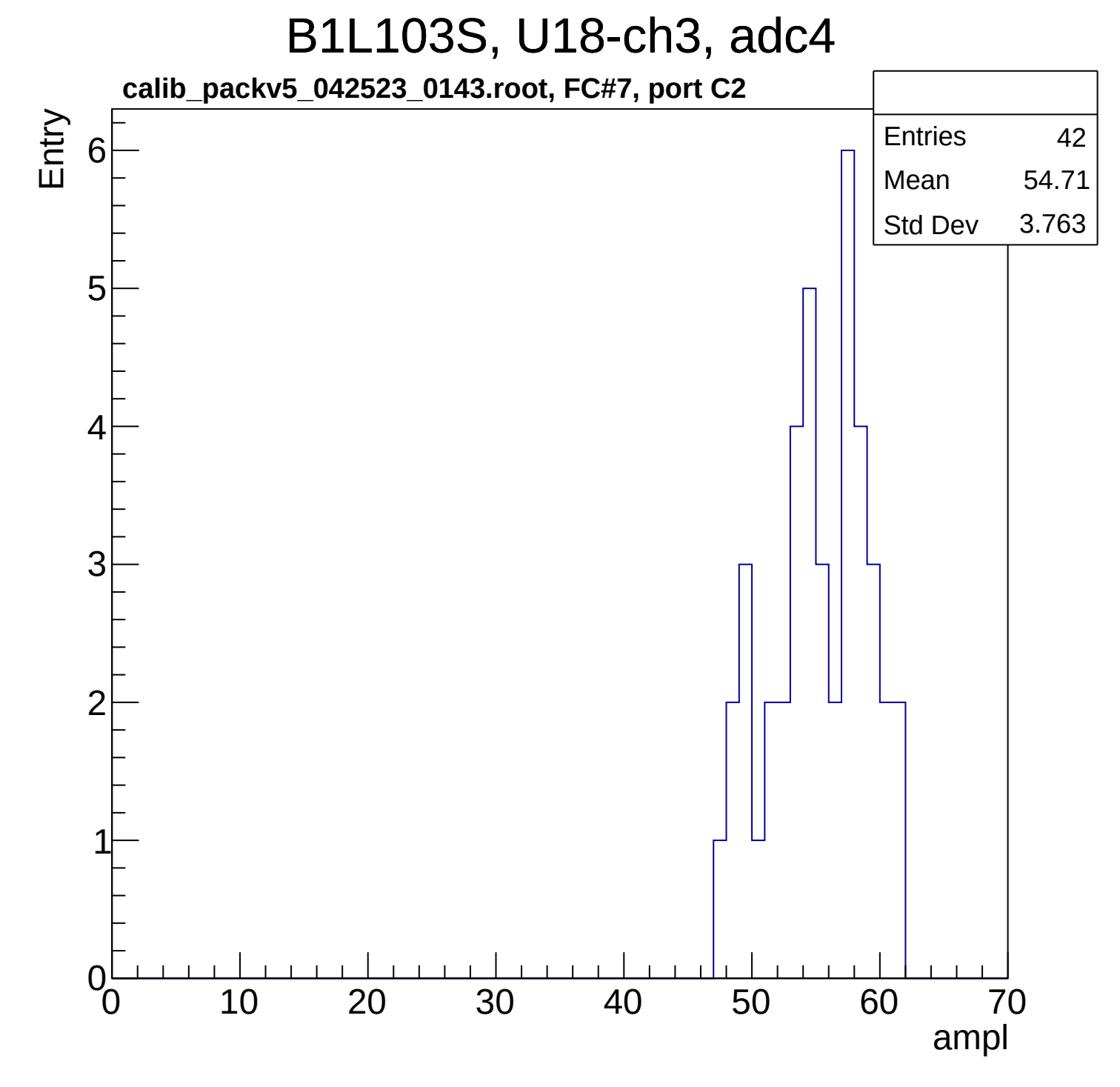
B1L103S, U18-ch3, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 42
Mean 54.71
Std Dev 3.763
Entry
ampl
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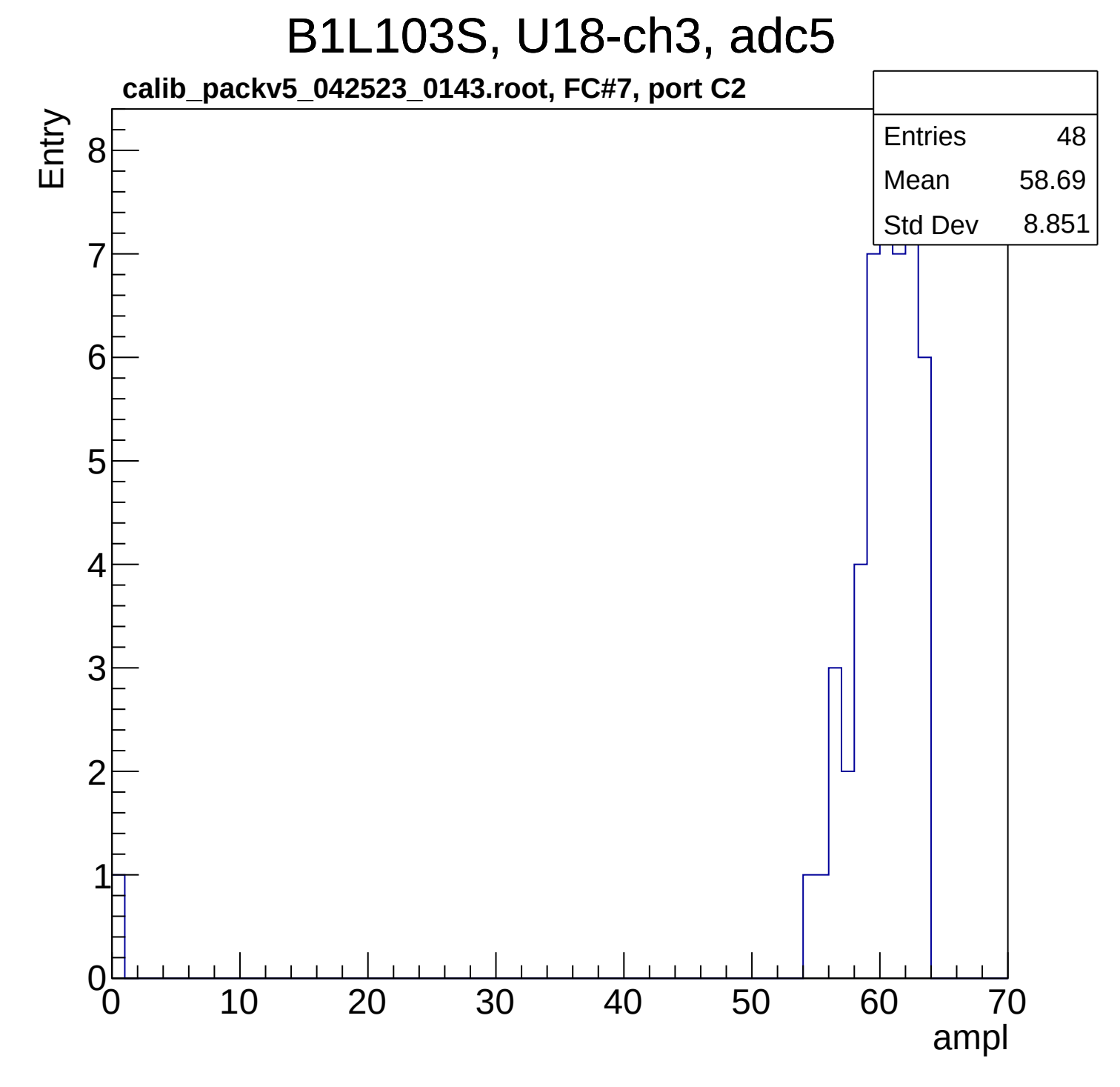
B1L103S, U18-ch3, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 48
Mean 58.69
Std Dev 8.851
Entry
ampl
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10
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60
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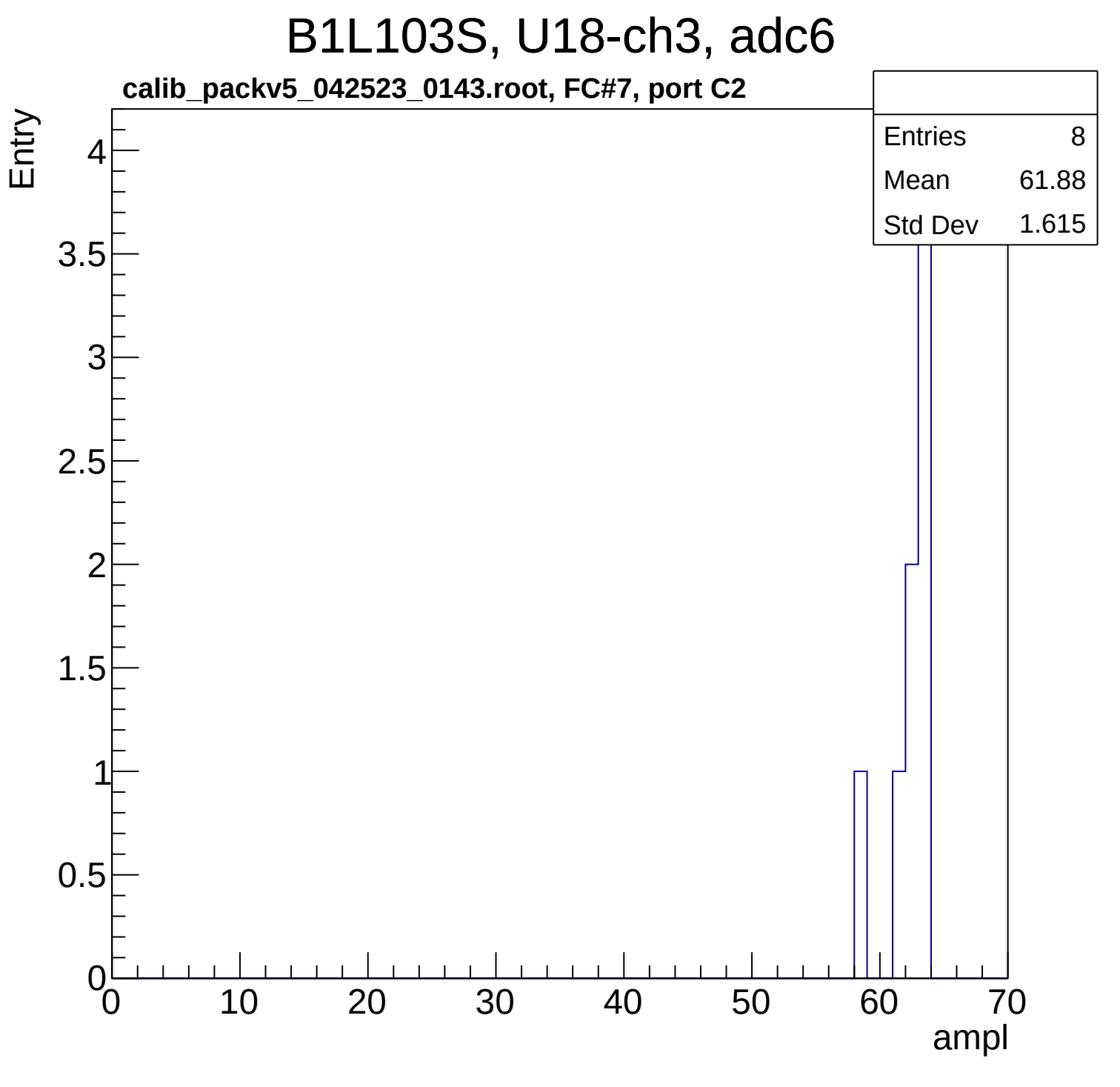
B1L103S, U18-ch3, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 8
Mean 61.88
Std Dev 1.615
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
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60
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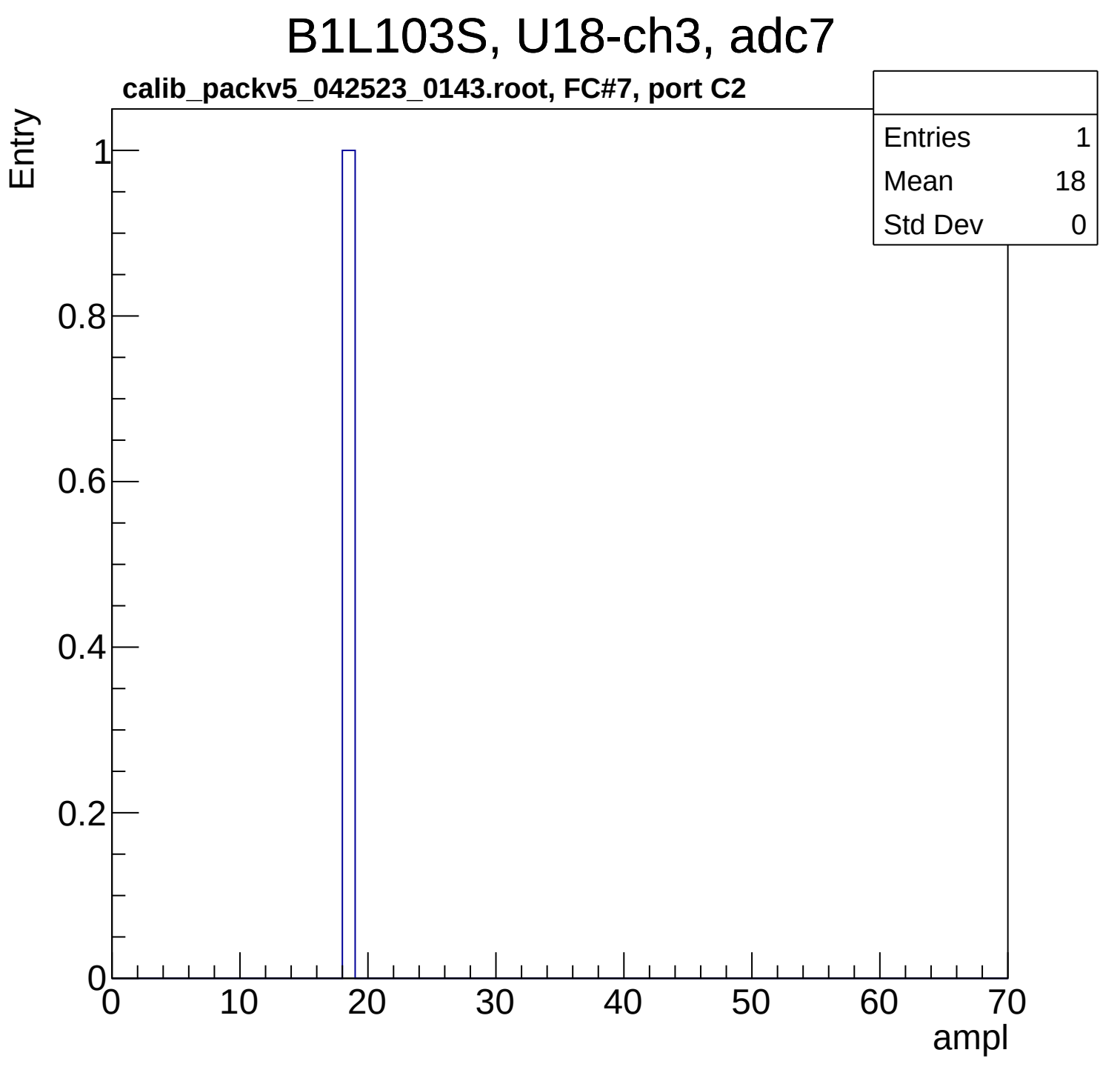
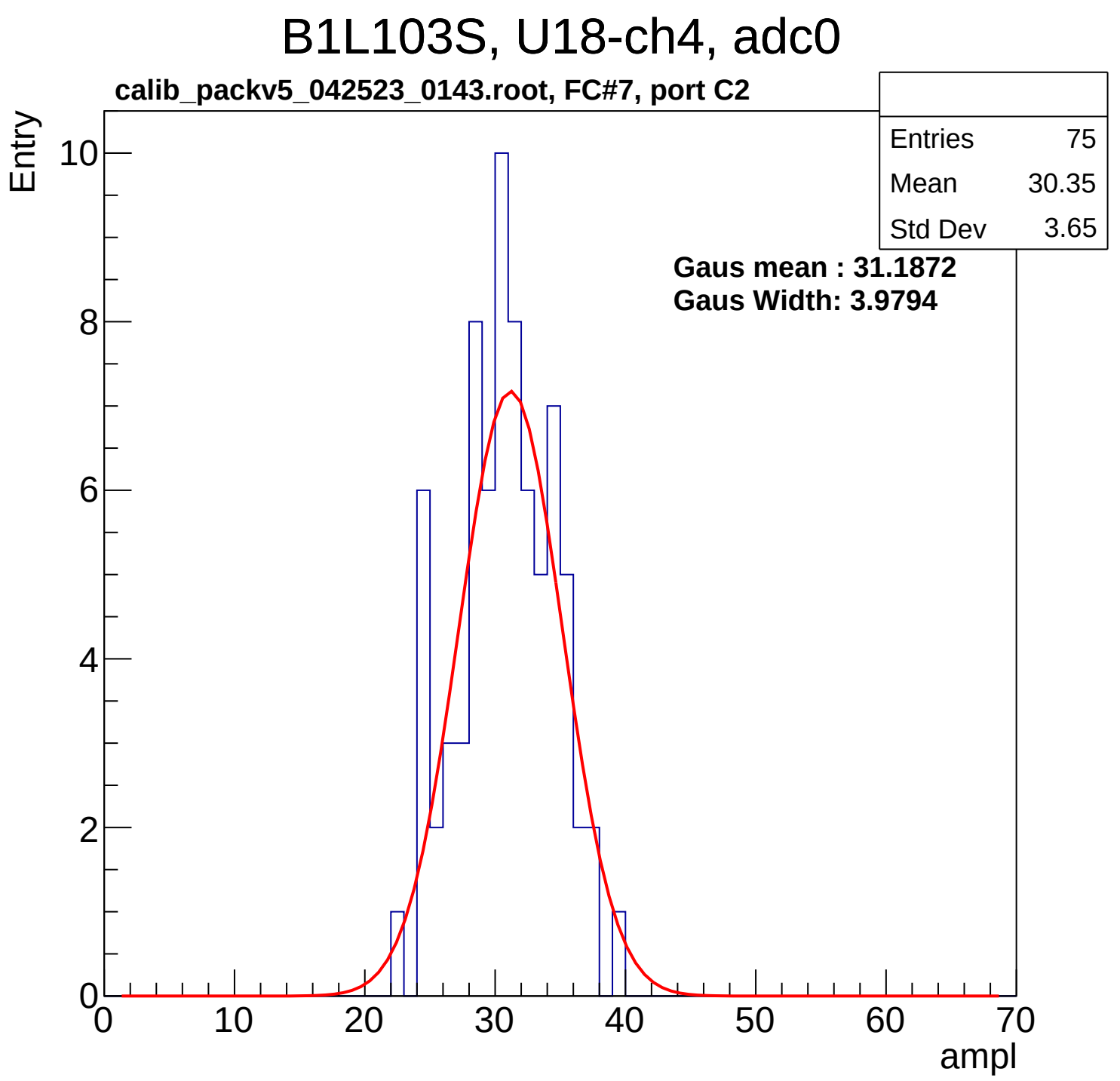

B1L103S, U18-ch3, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 18
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch4, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 75
Mean 30.35
Std Dev 3.65
Gaus mean : 31.1872
Gaus Width: 3.9794
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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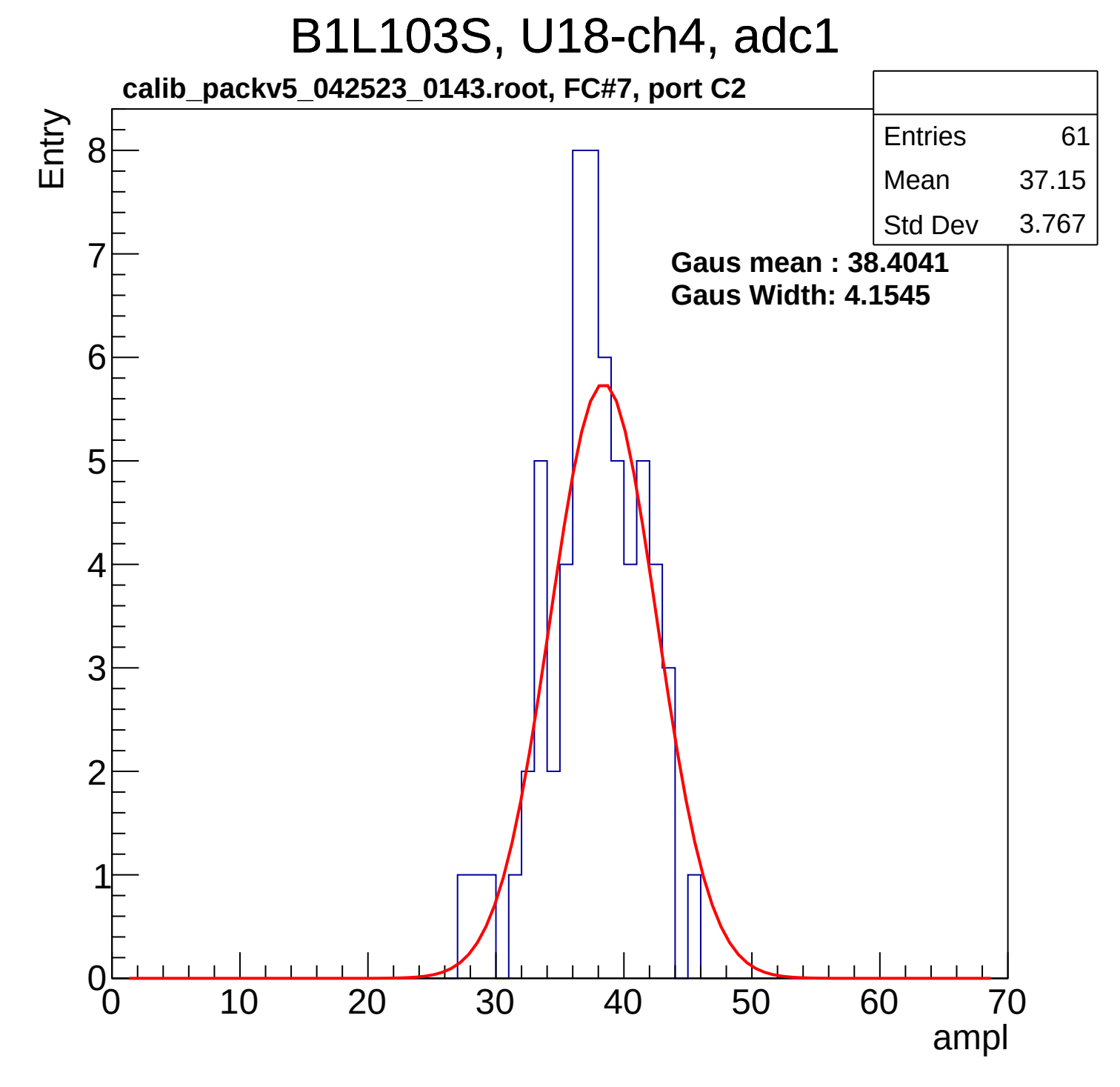
B1L103S, U18-ch4, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 61
Mean 37.15
Std Dev 3.767
Gaus mean : 38.4041
Gaus Width: 4.1545
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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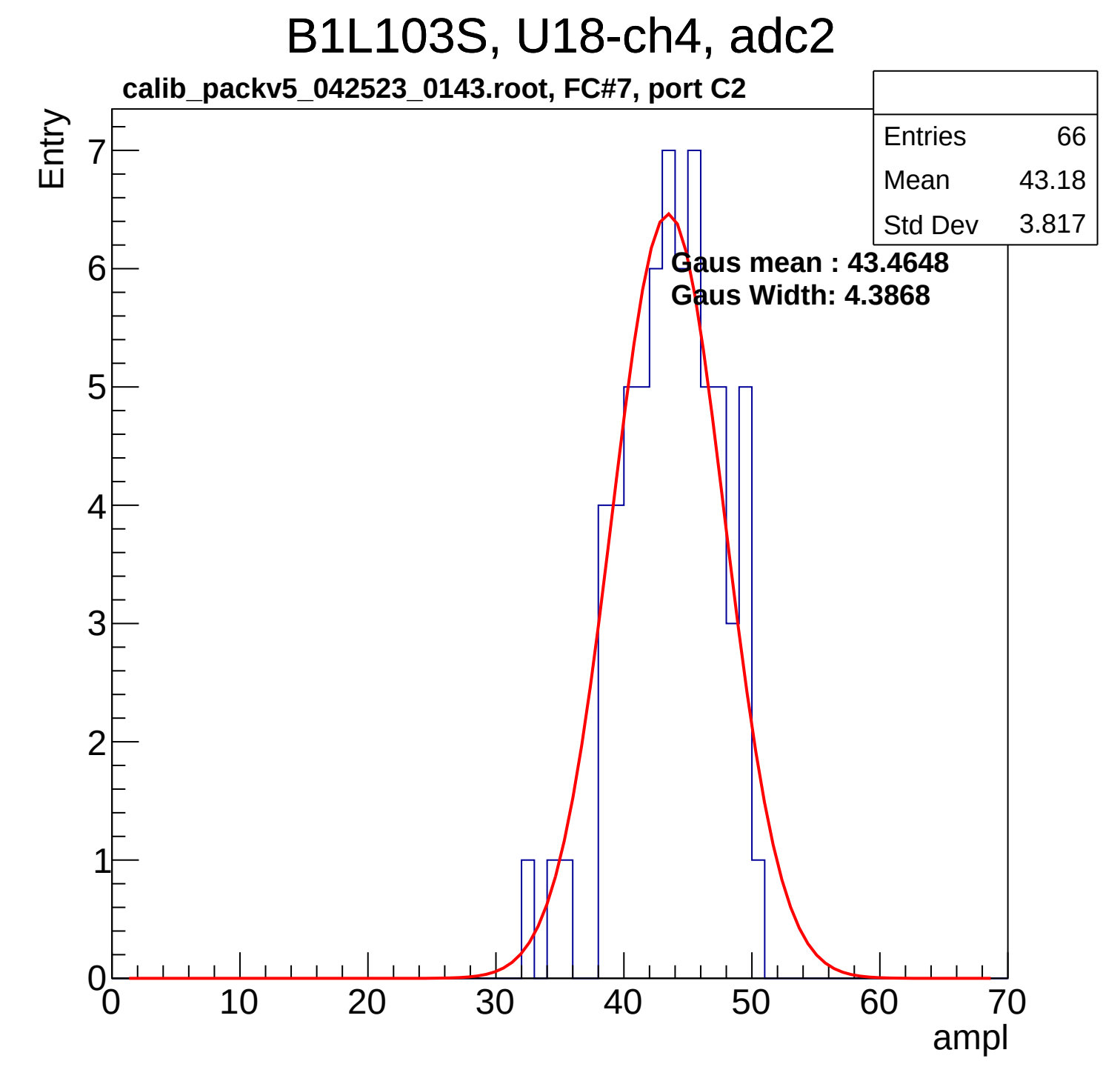
B1L103S, U18-ch4, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 43.18
Std Dev 3.817
Gaus mean : 43.4648
Gaus Width: 4.3868
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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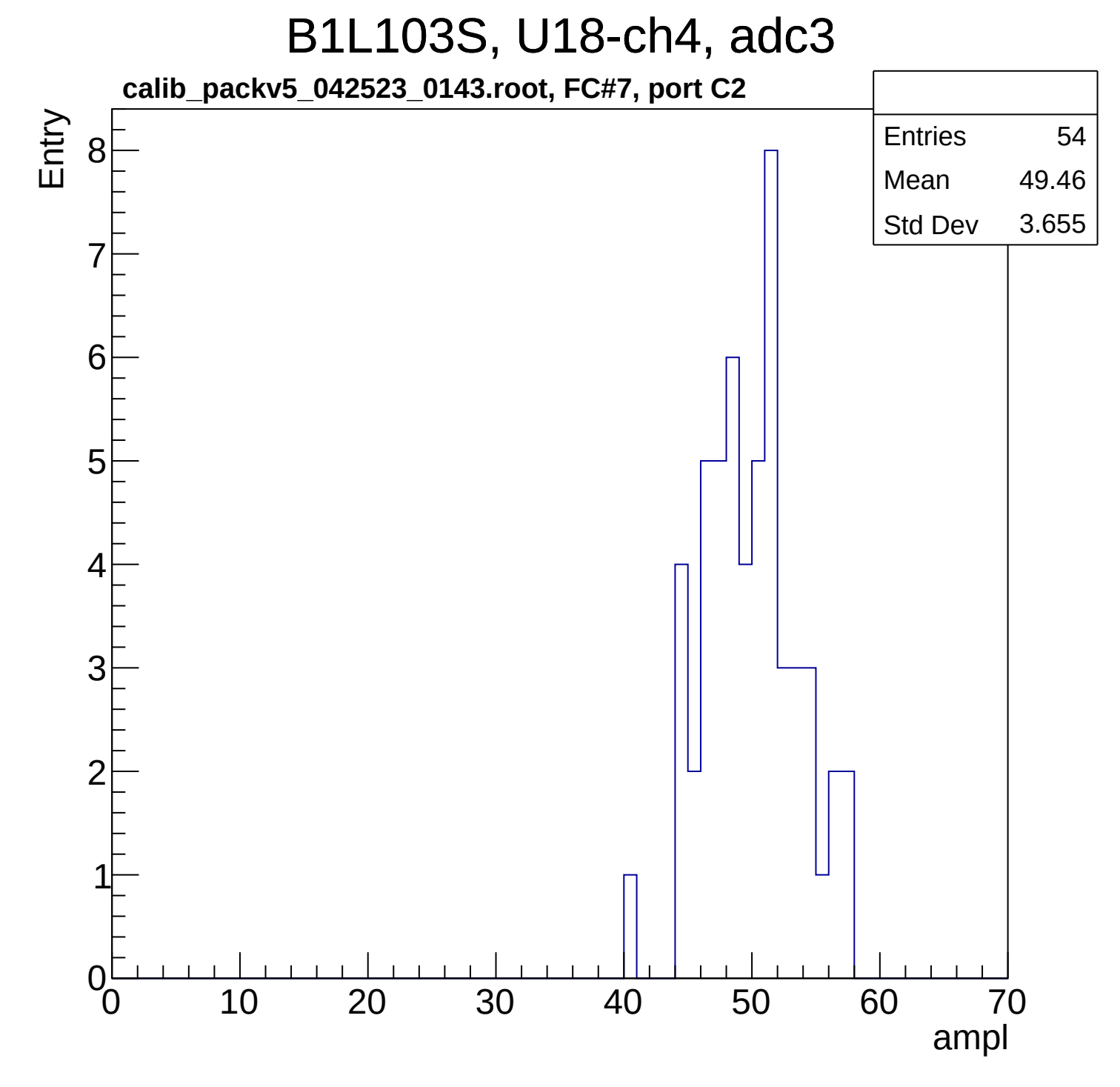
B1L103S, U18-ch4, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 54
Mean 49.46
Std Dev 3.655
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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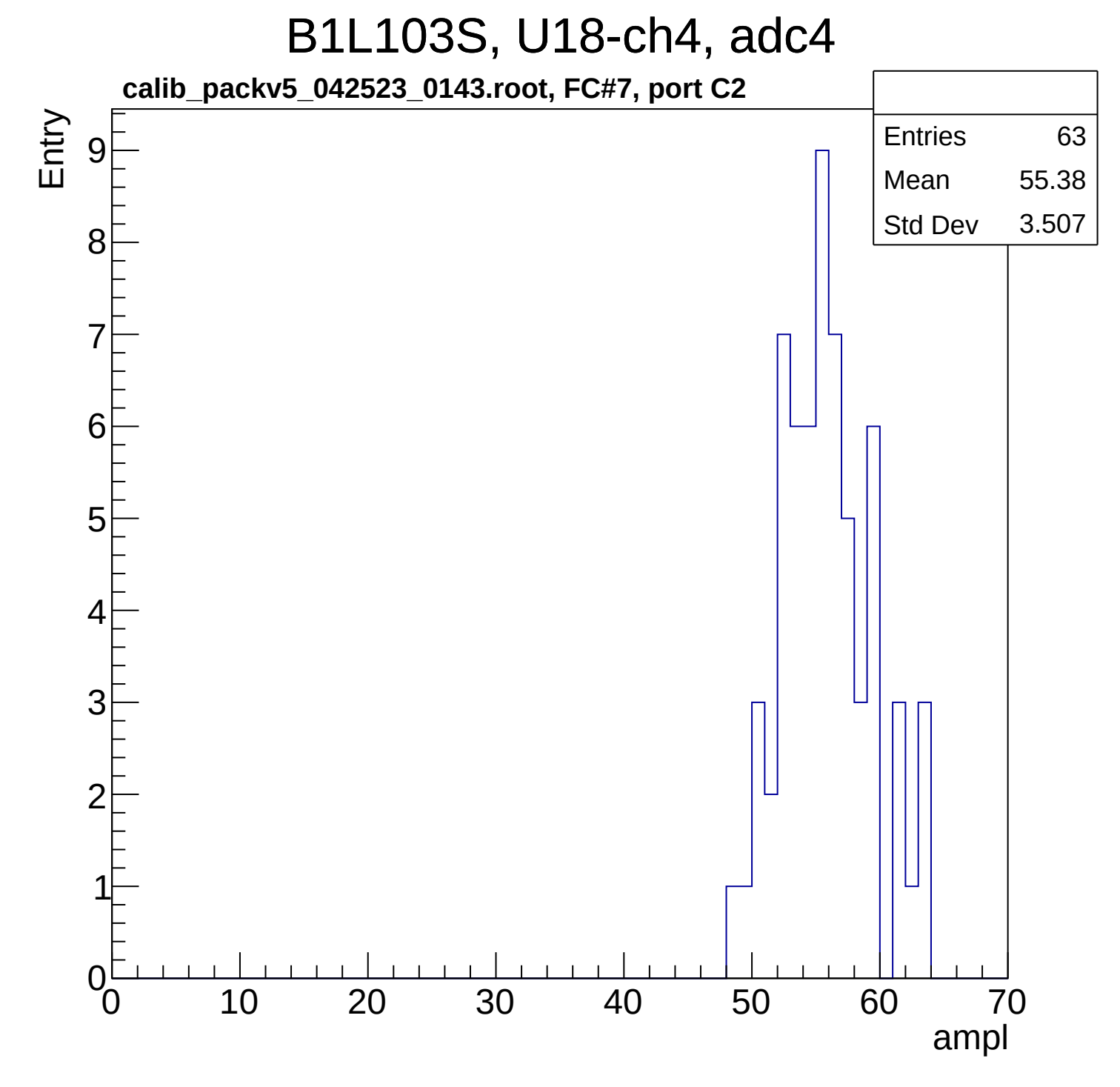
B1L103S, U18-ch4, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 55.38
Std Dev 3.507
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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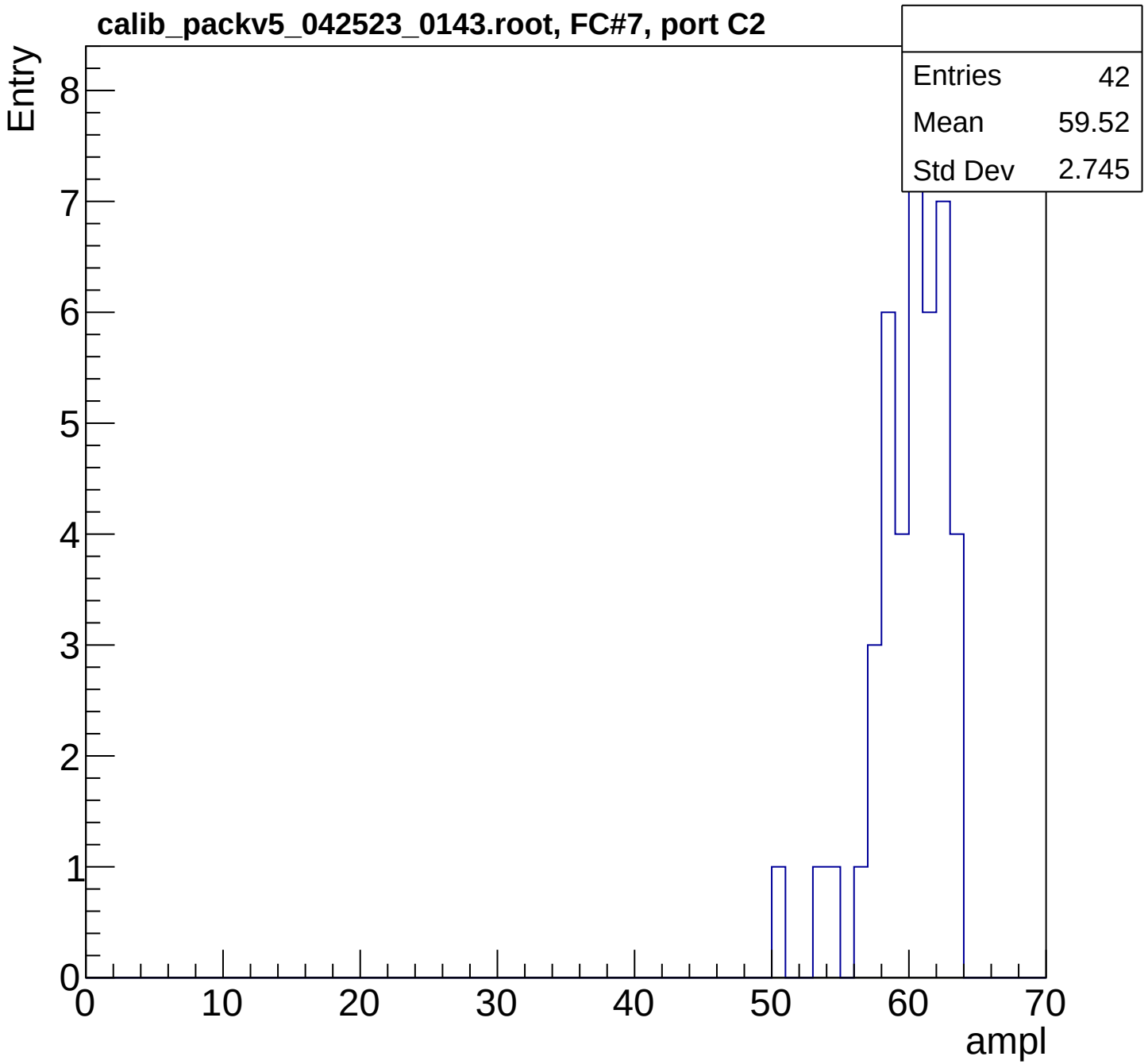
B1L103S, U18-ch4, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 42
Mean 59.52
Std Dev 2.745
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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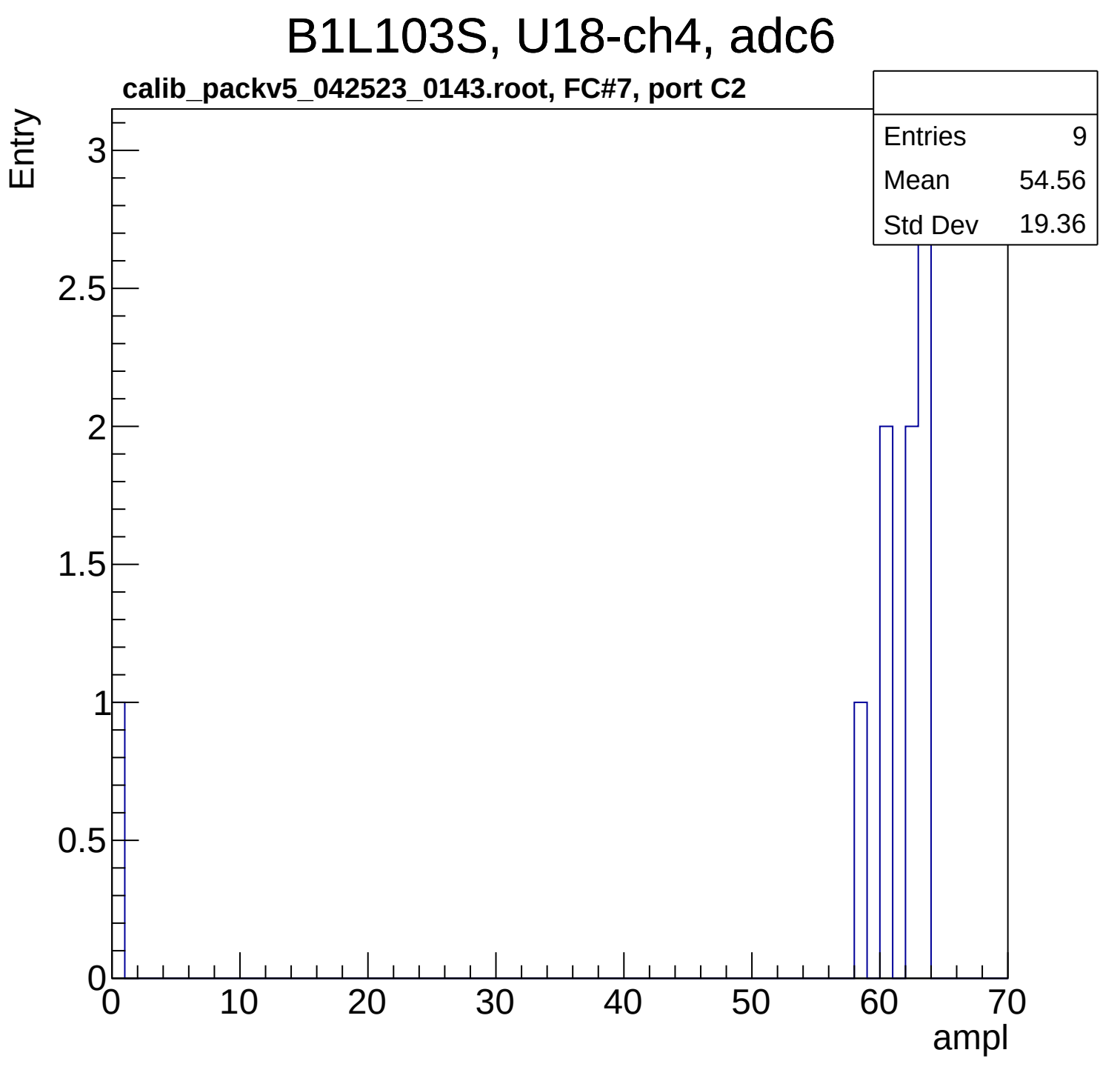
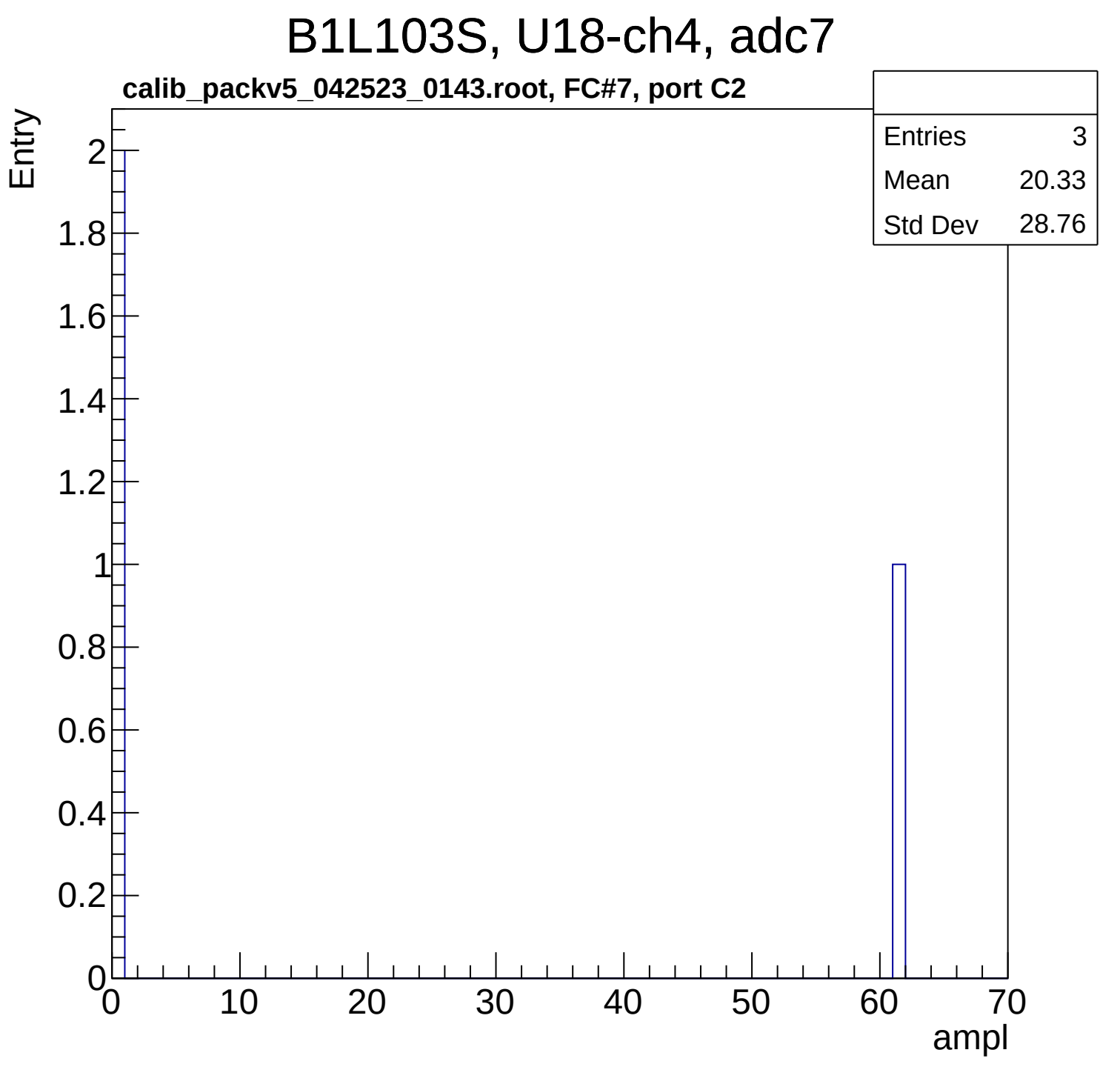
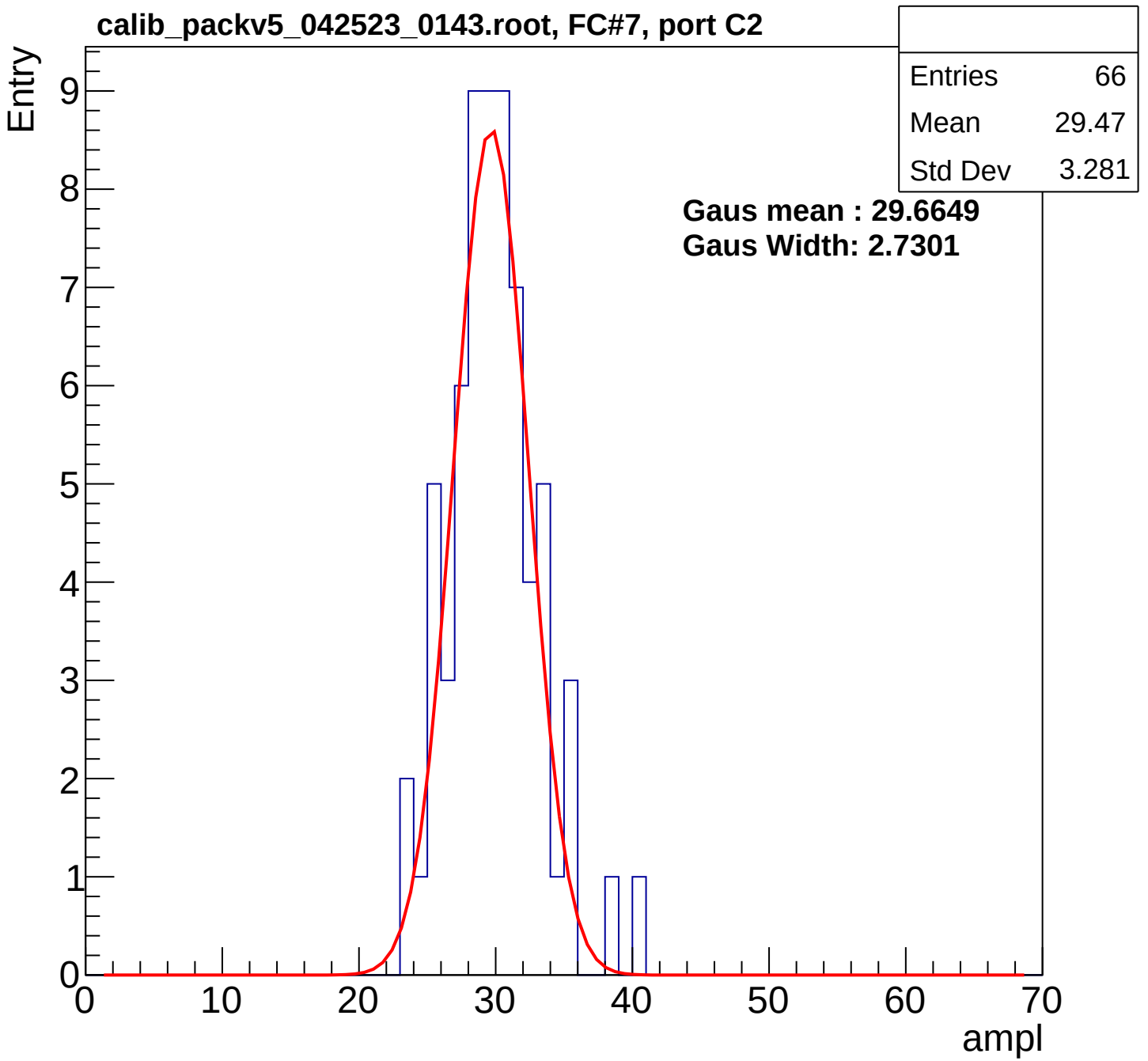

B1L103S, U18-ch4, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 9
Mean 54.56
Std Dev 19.36
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U18-ch4, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 20.33
Std Dev 28.76
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U18-ch5, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 29.47
Std Dev 3.281
Gaus mean : 29.6649
Gaus Width: 2.7301
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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40
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60
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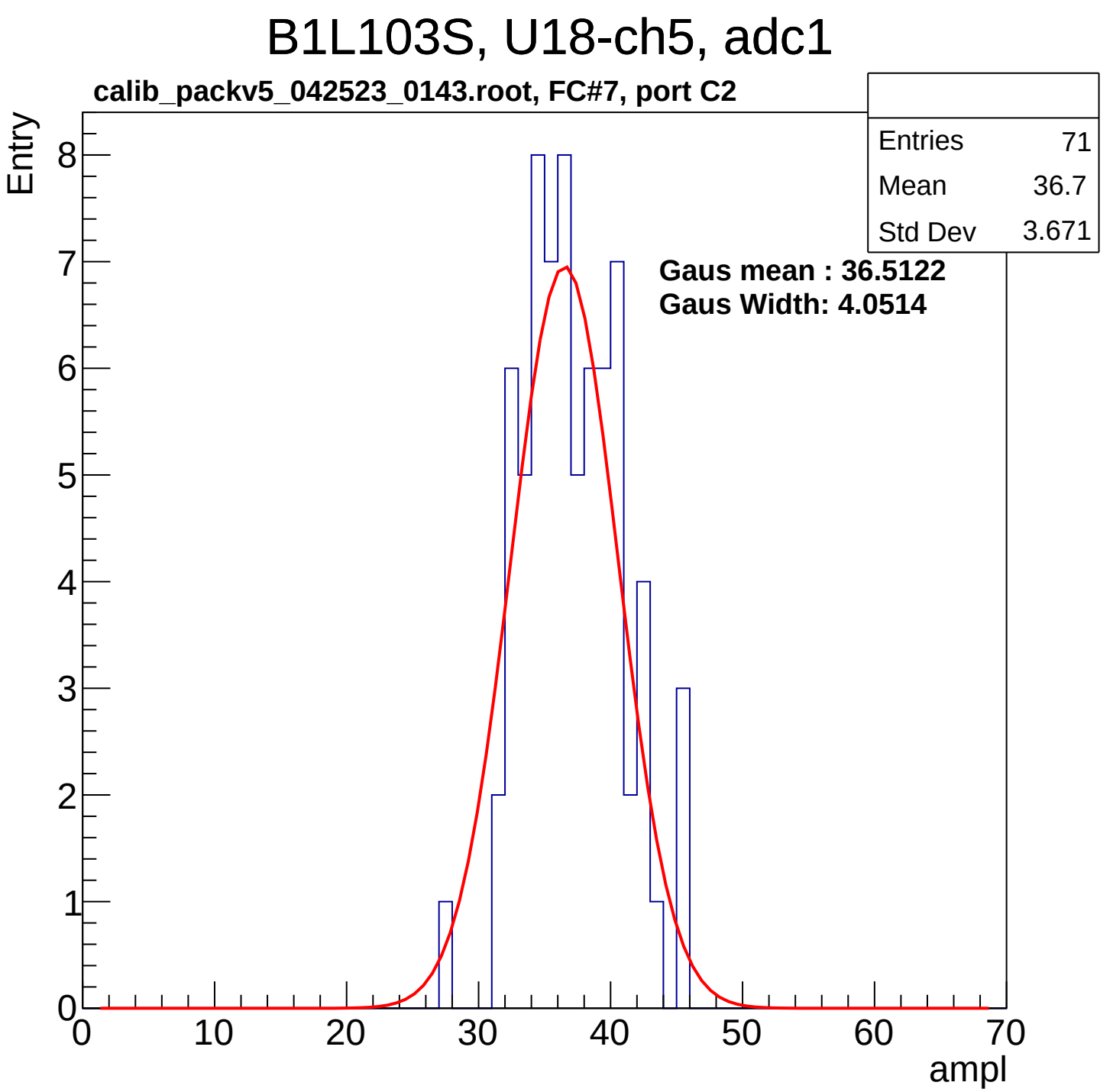
B1L103S, U18-ch5, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 71
Mean 36.7
Std Dev 3.671
Gaus mean : 36.5122
Gaus Width: 4.0514
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
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60
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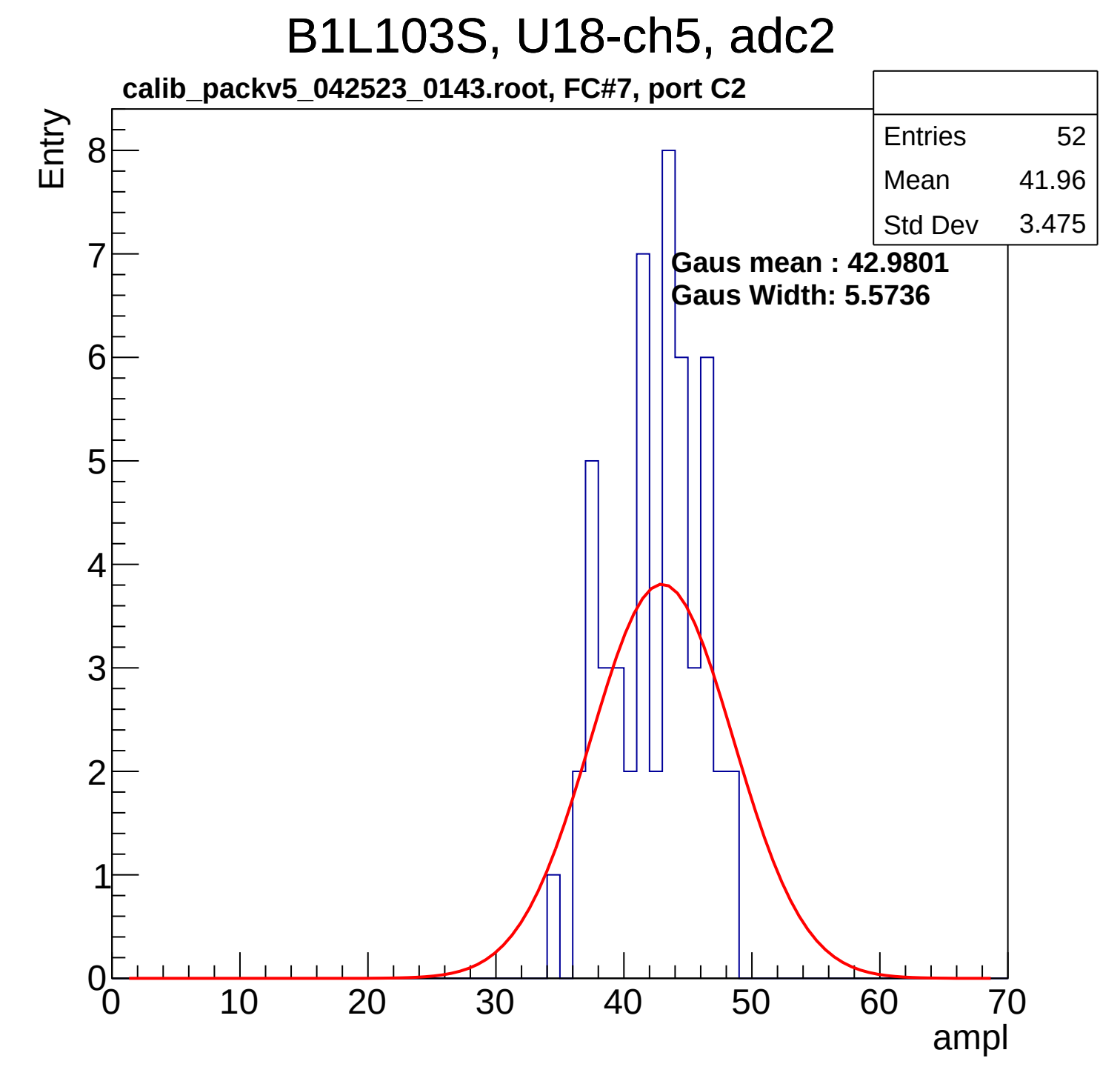
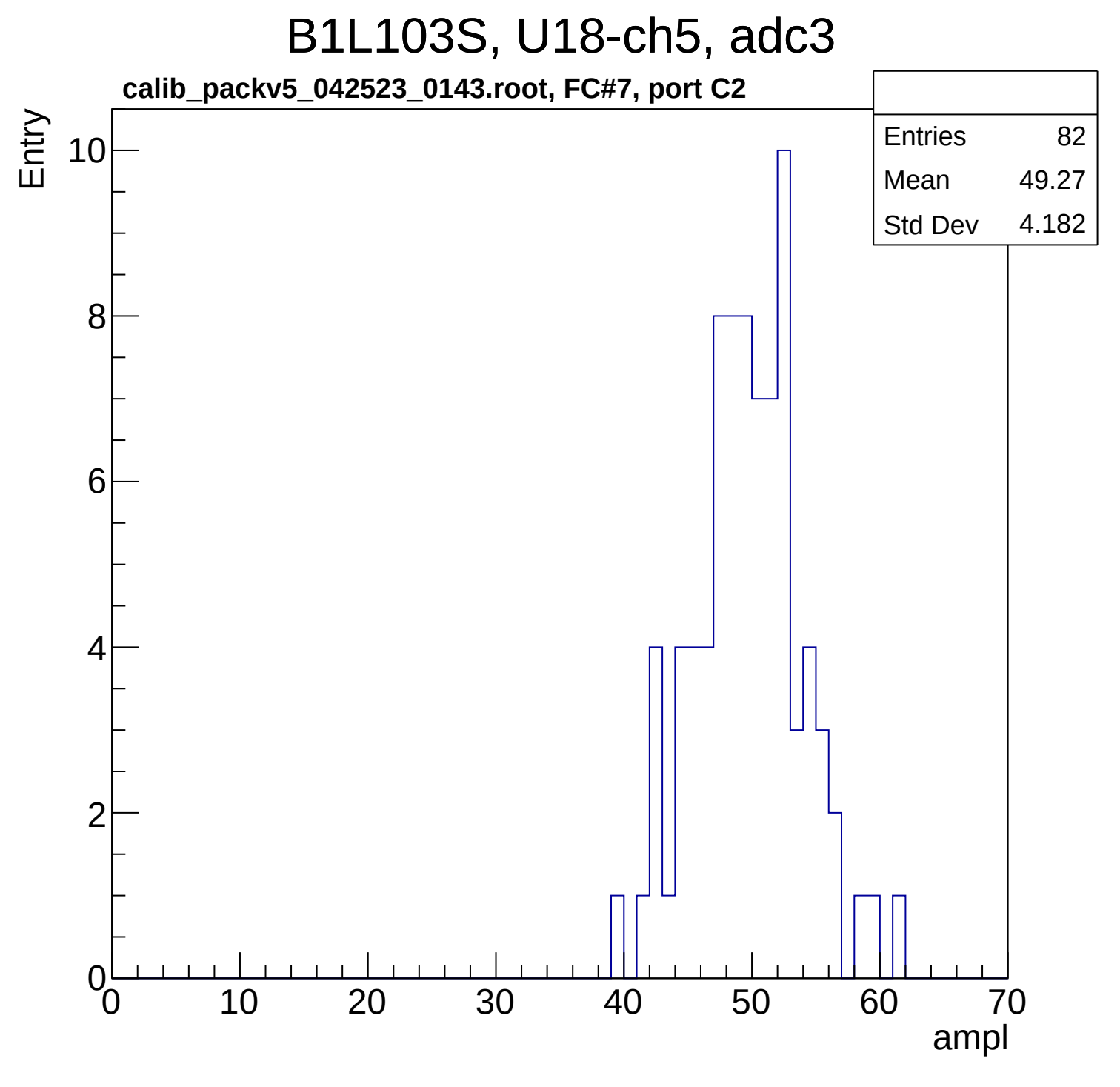
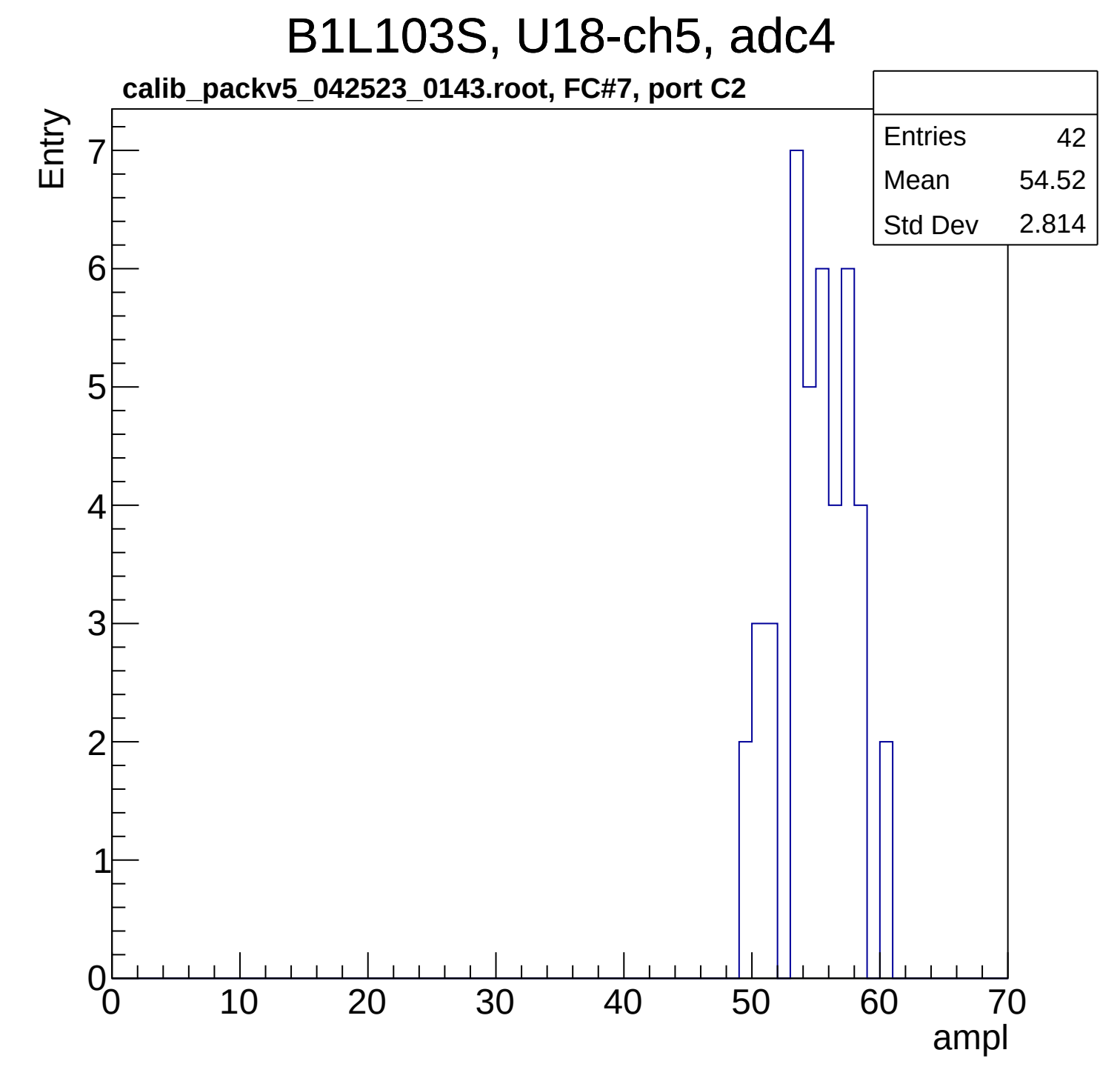

B1L103S, U18-ch5, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 52
Mean 41.96
Std Dev 3.475
Gaus mean : 42.9801
Gaus Width: 5.5736
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch5, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 82
Mean 49.27
Std Dev 4.182
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch5, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 42
Mean 54.52
Std Dev 2.814
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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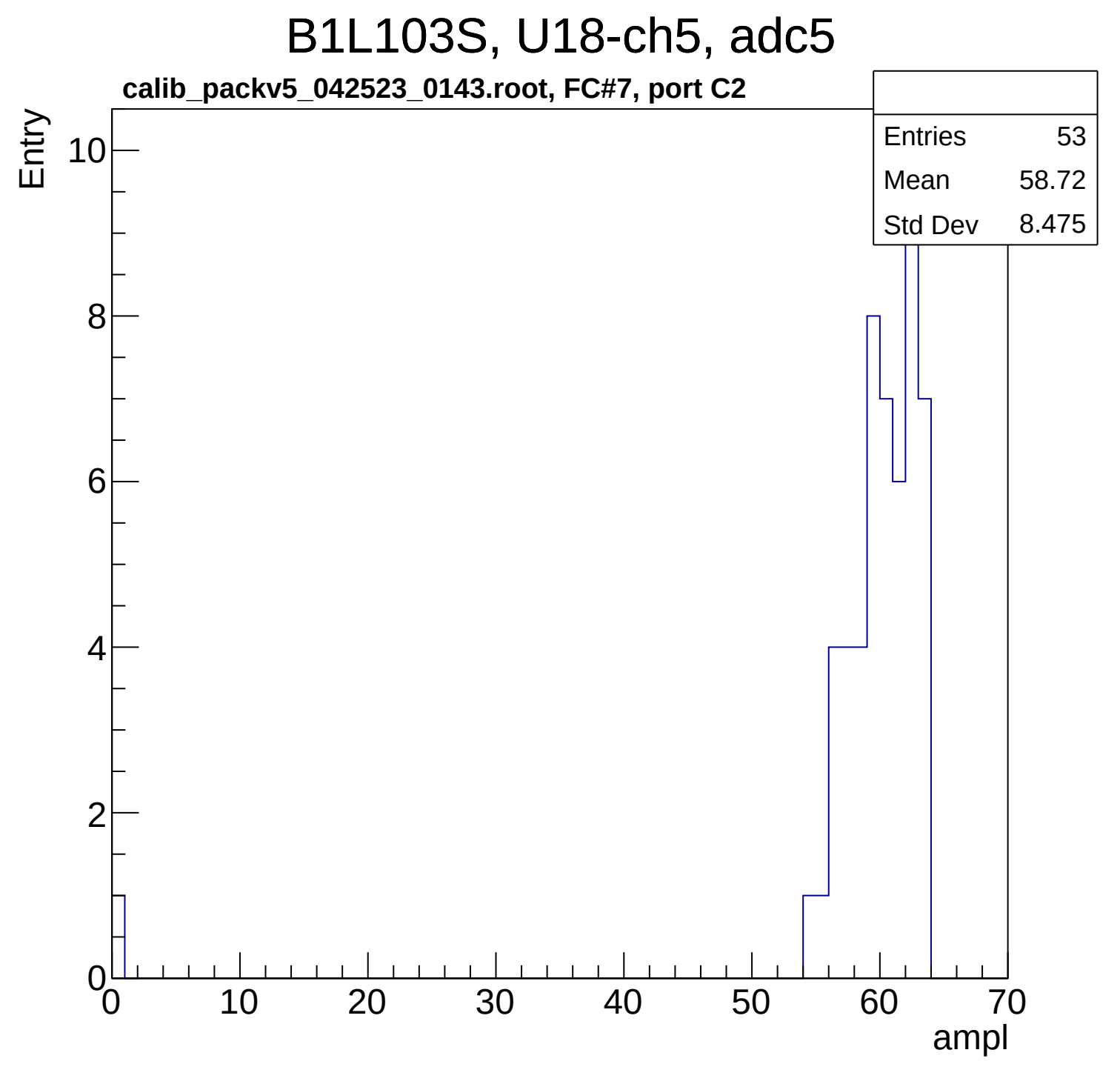
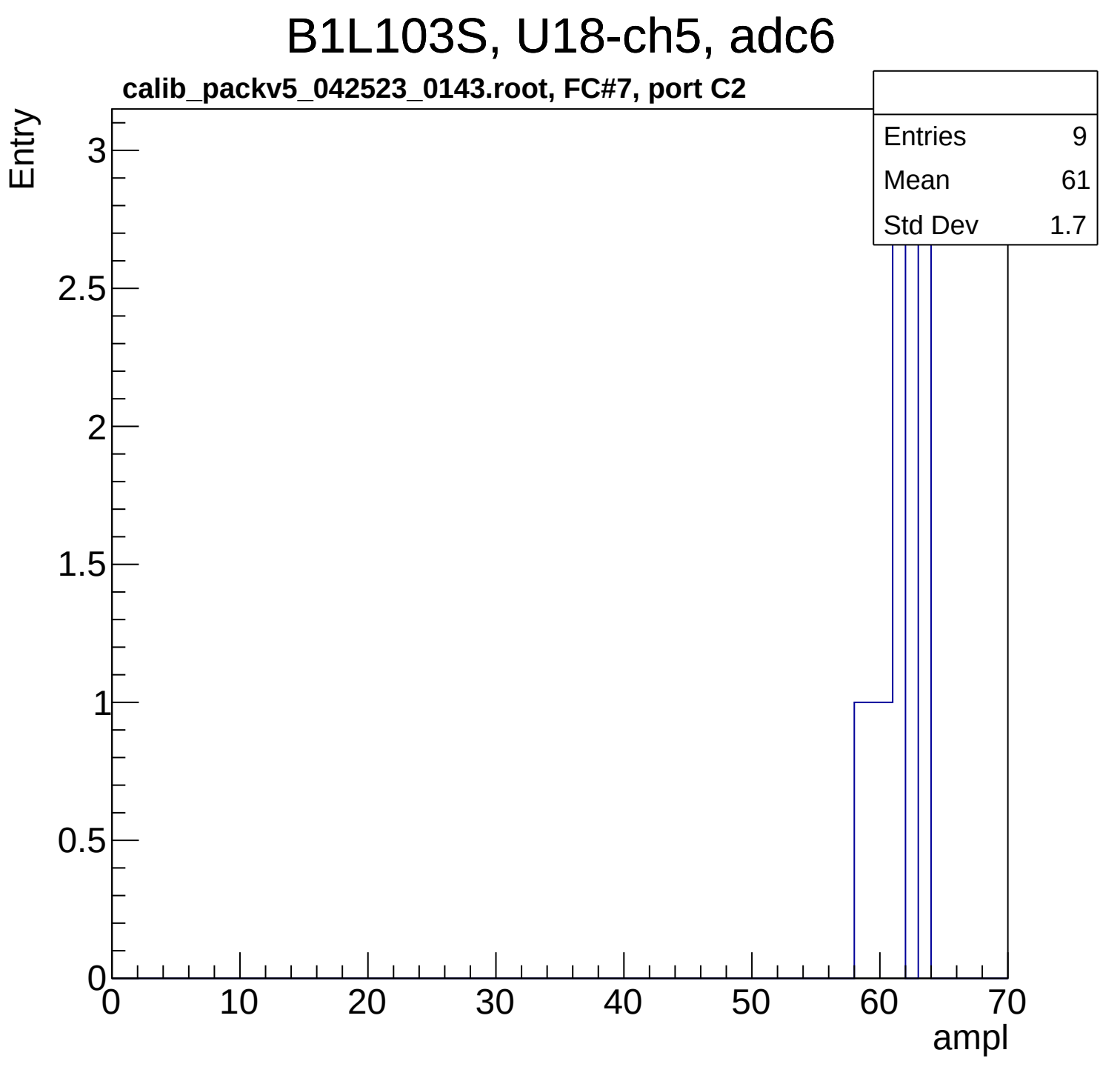
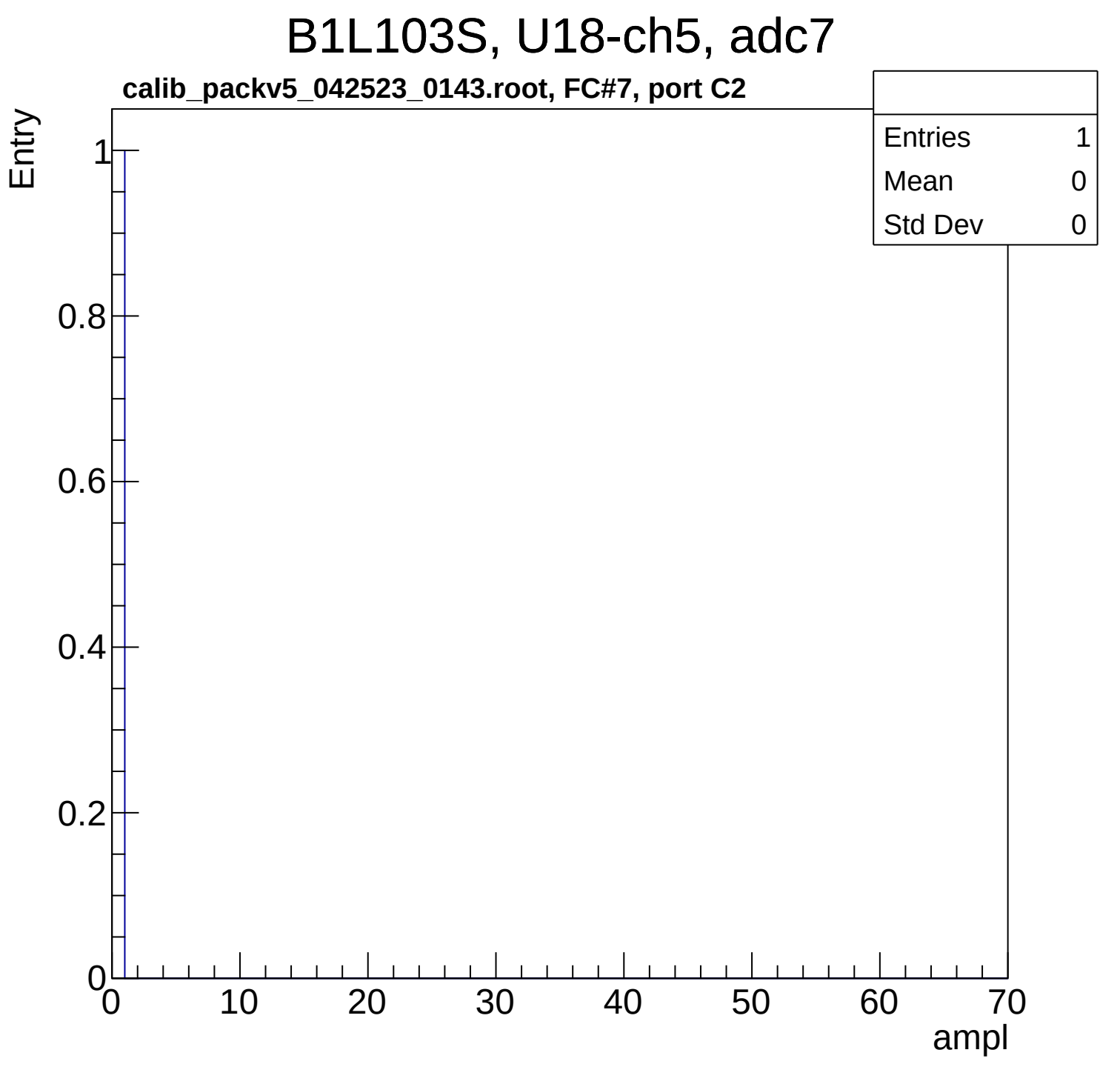
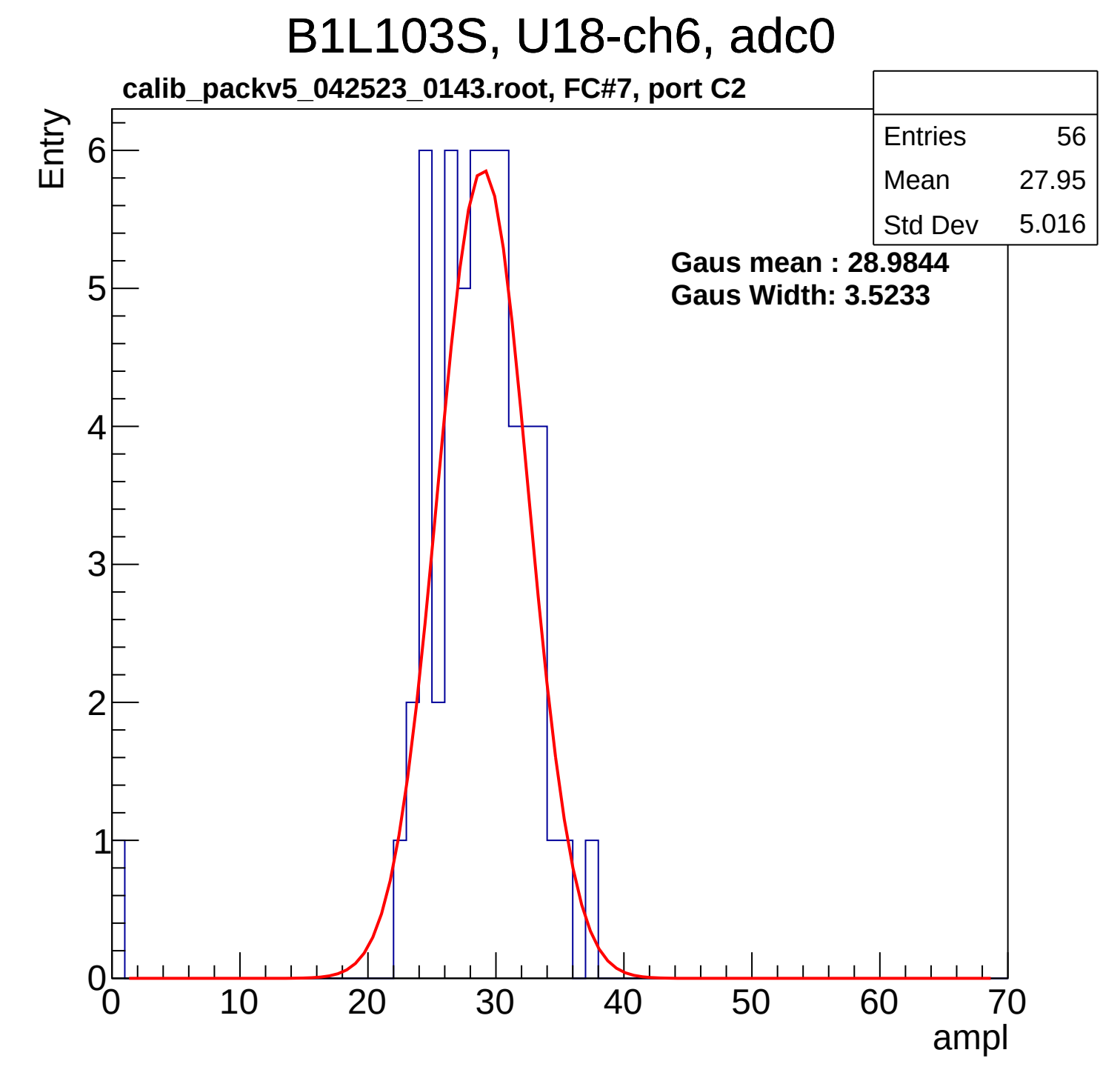
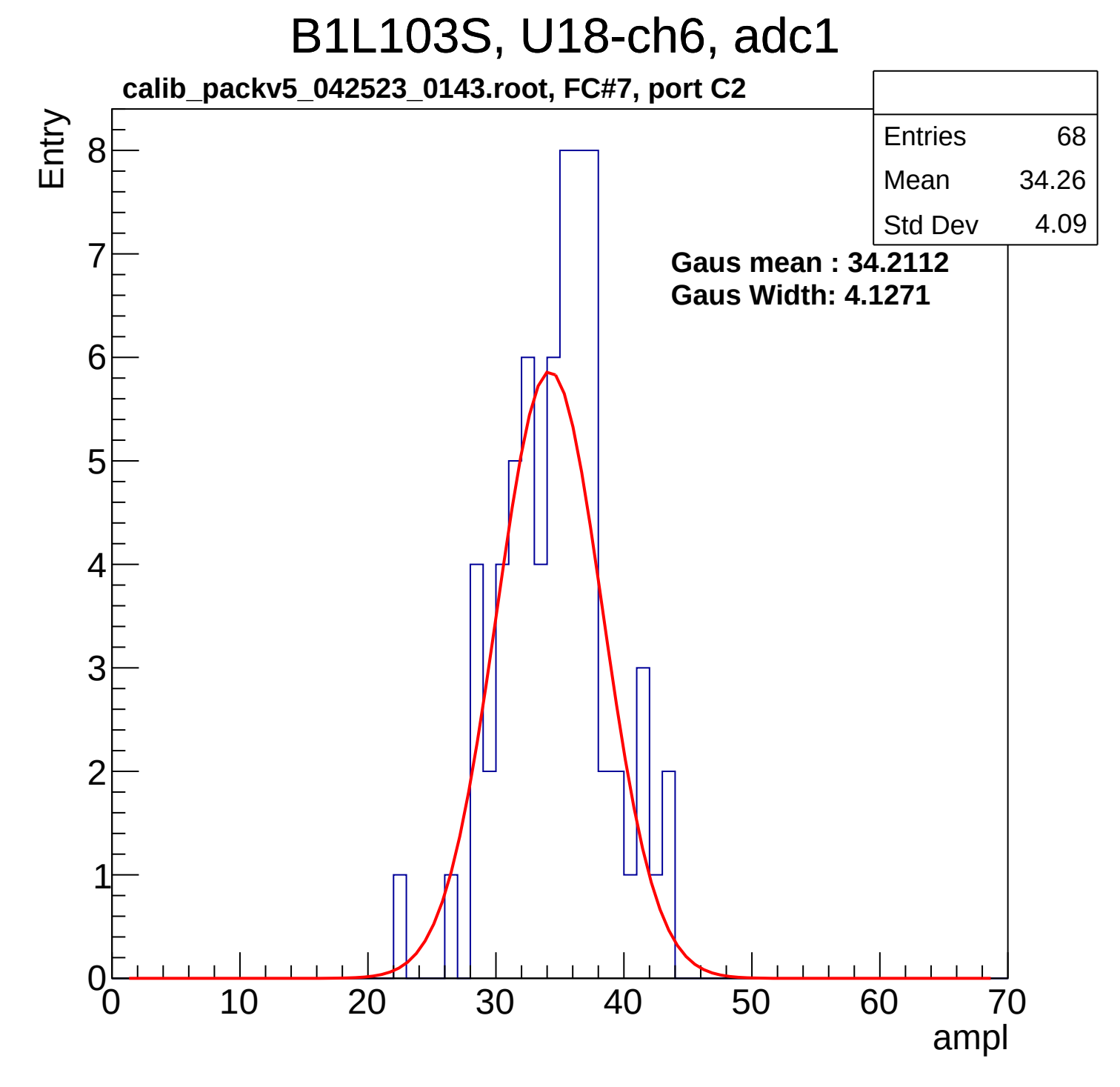
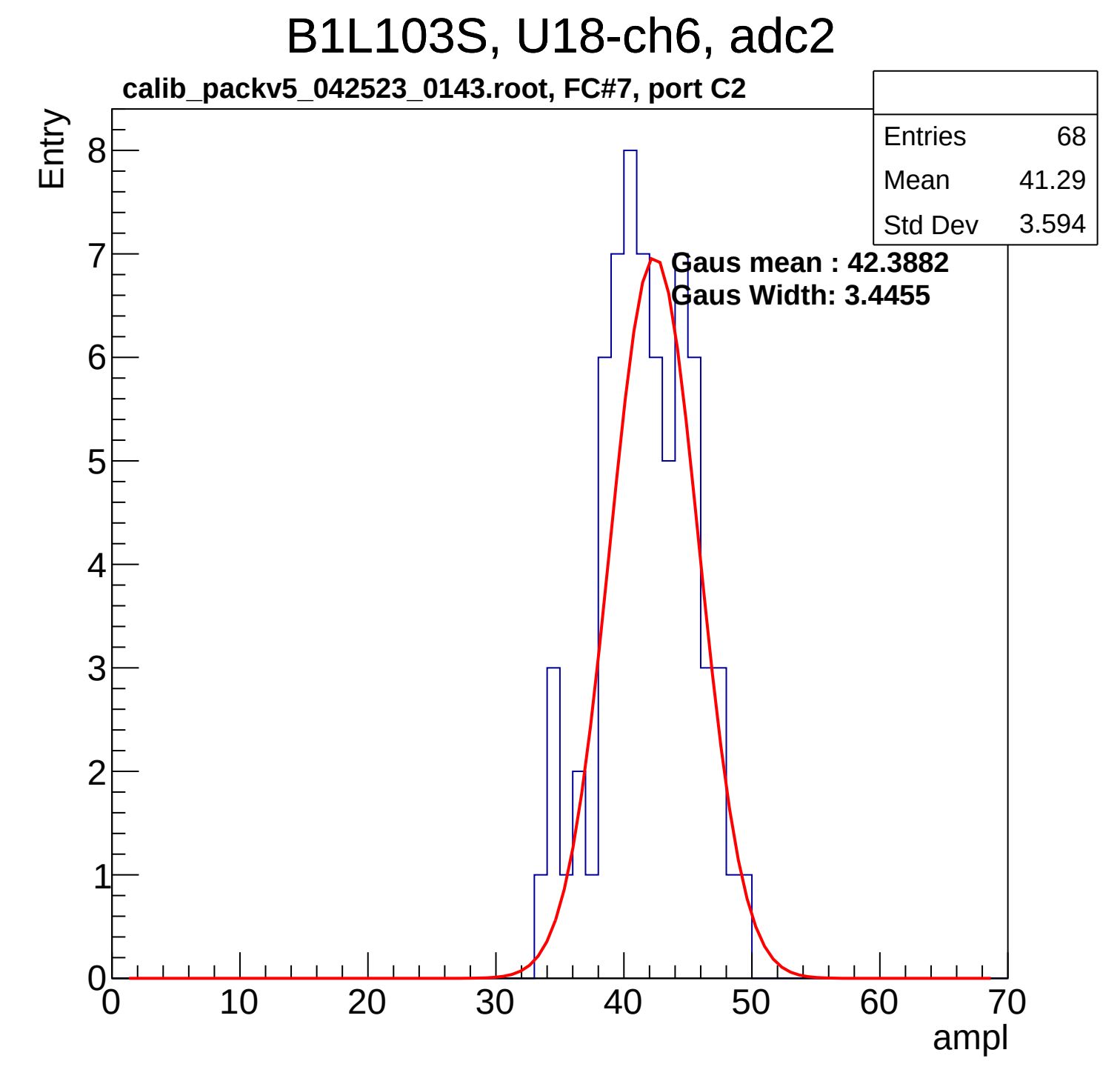

B1L103S, U18-ch5, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 58.72
Std Dev 8.475
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch5, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 9
Mean 61
Std Dev 1.7
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U18-ch5, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch6, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 27.95
Std Dev 5.016
Gaus mean : 28.9844
Gaus Width: 3.5233
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U18-ch6, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 34.26
Std Dev 4.09
Gaus mean : 34.2112
Gaus Width: 4.1271
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch6, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 41.29
Std Dev 3.594
Gaus mean : 42.3882
Gaus Width: 3.4455
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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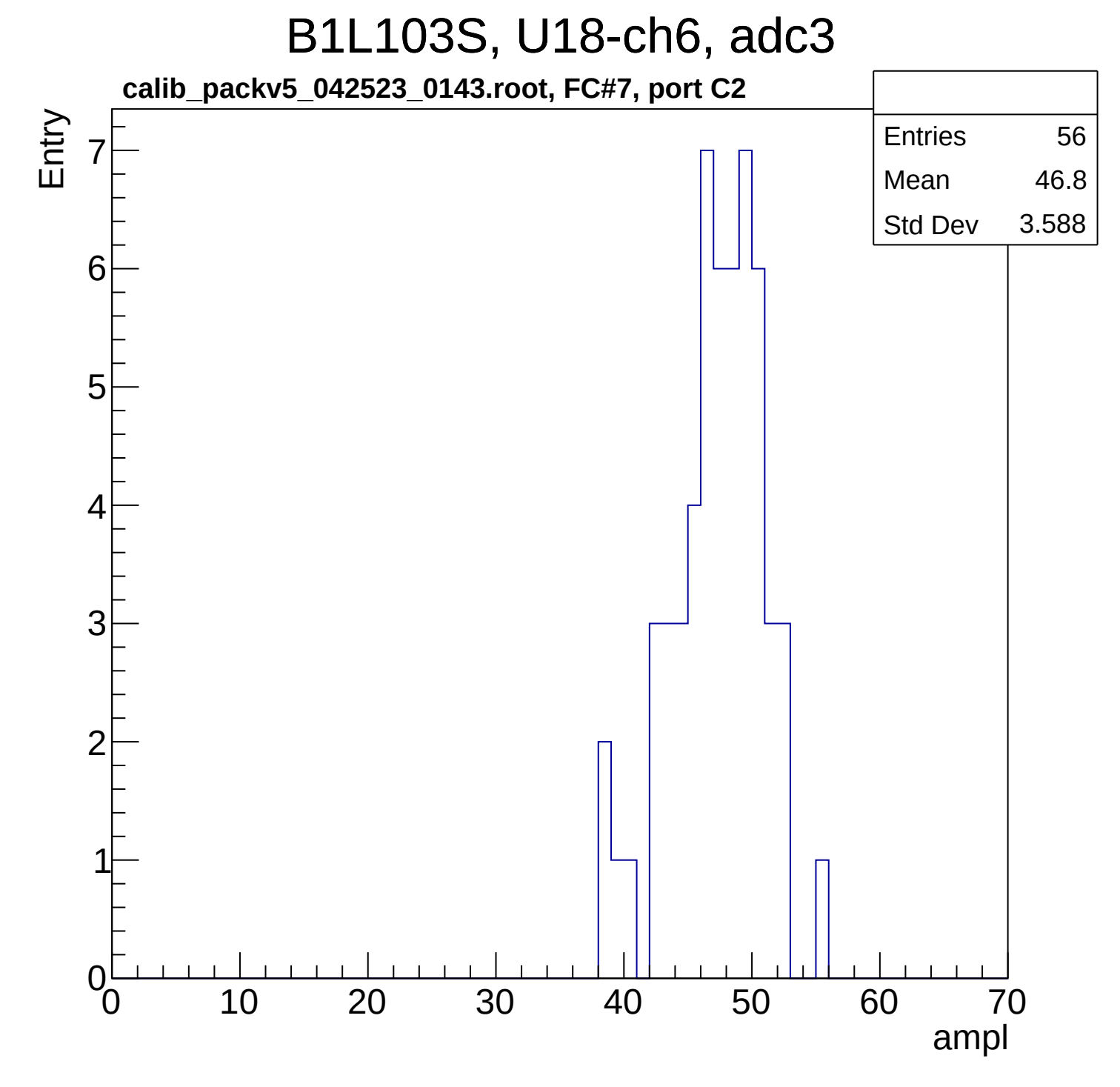
B1L103S, U18-ch6, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 46.8
Std Dev 3.588
Entry
ampl
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1
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4
5
6
7
0
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20
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40
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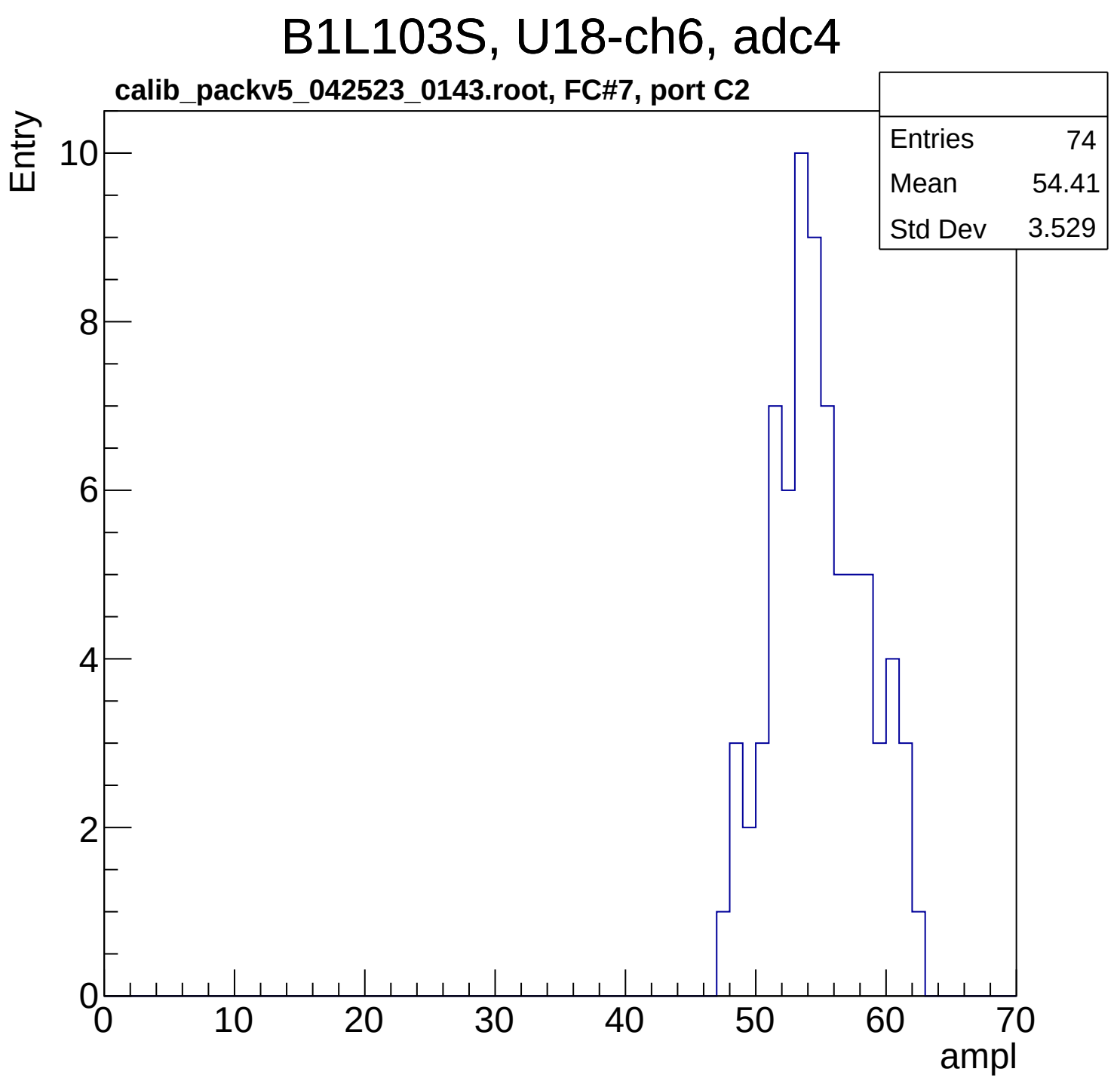
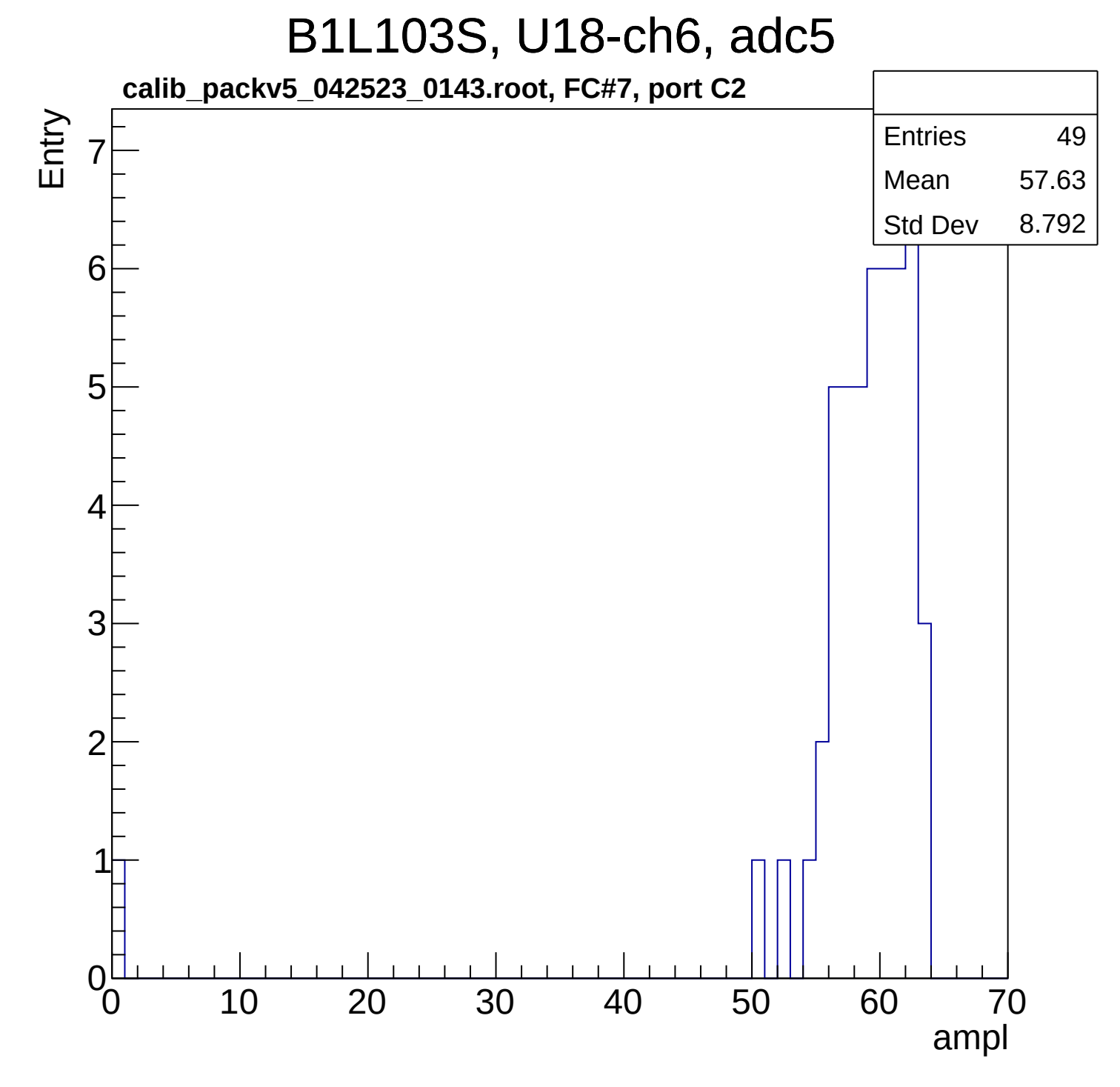
60
70


B1L103S, U18-ch6, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 74
Mean 54.41
Std Dev 3.529
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch6, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 49
Mean 57.63
Std Dev 8.792
Entry
ampl
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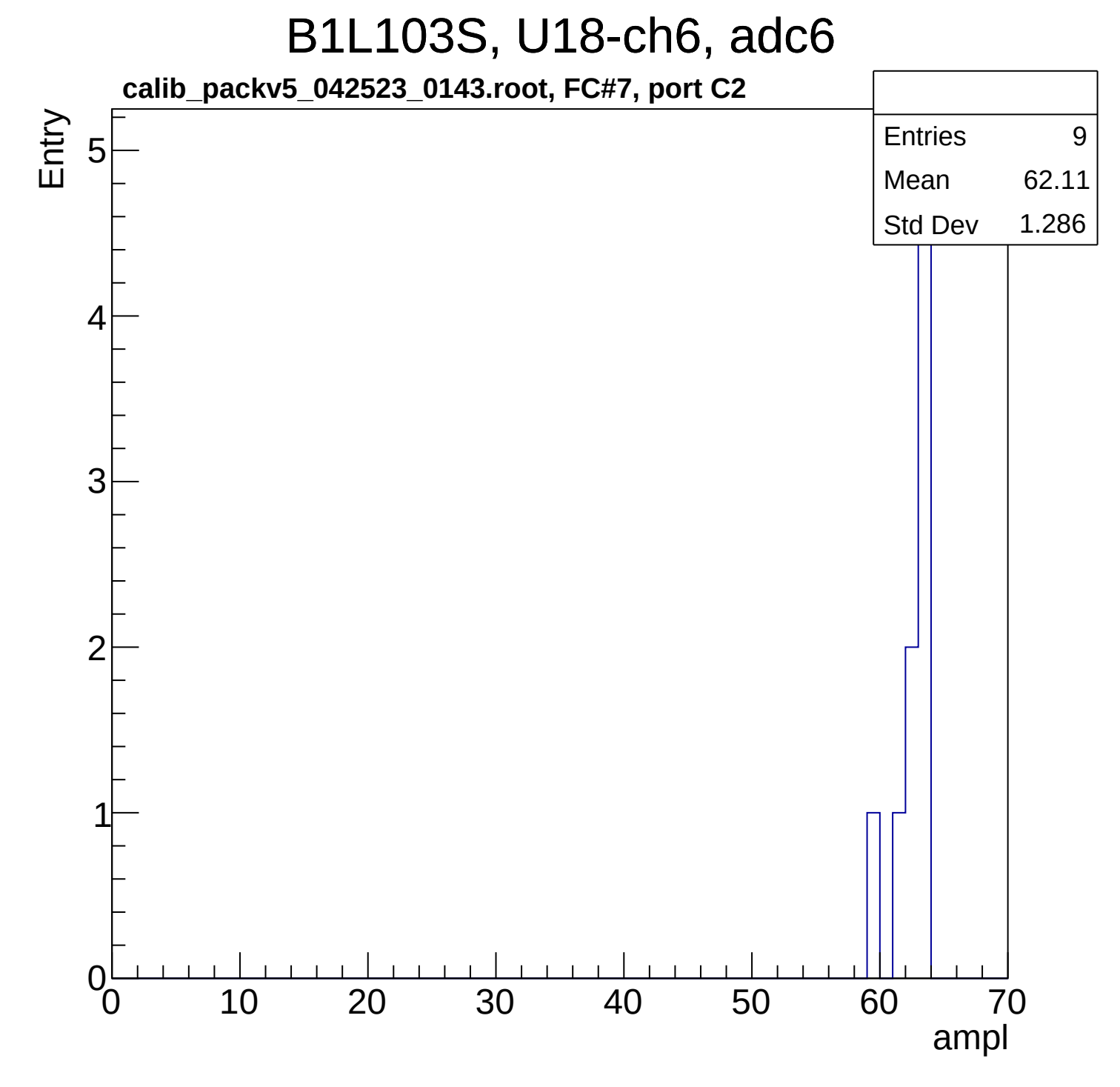
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch6, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 9
Mean 62.11
Std Dev 1.286
Entry
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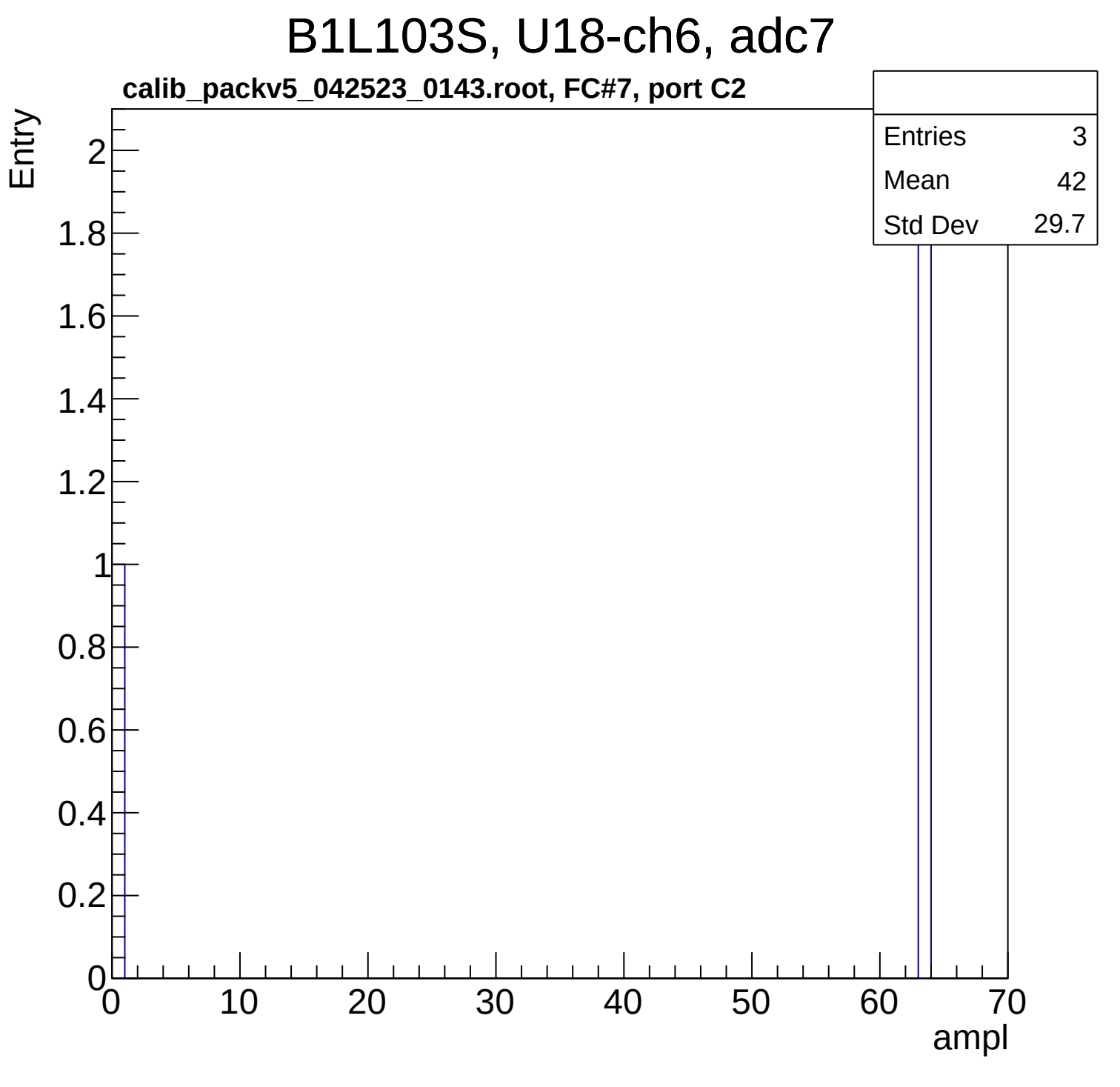
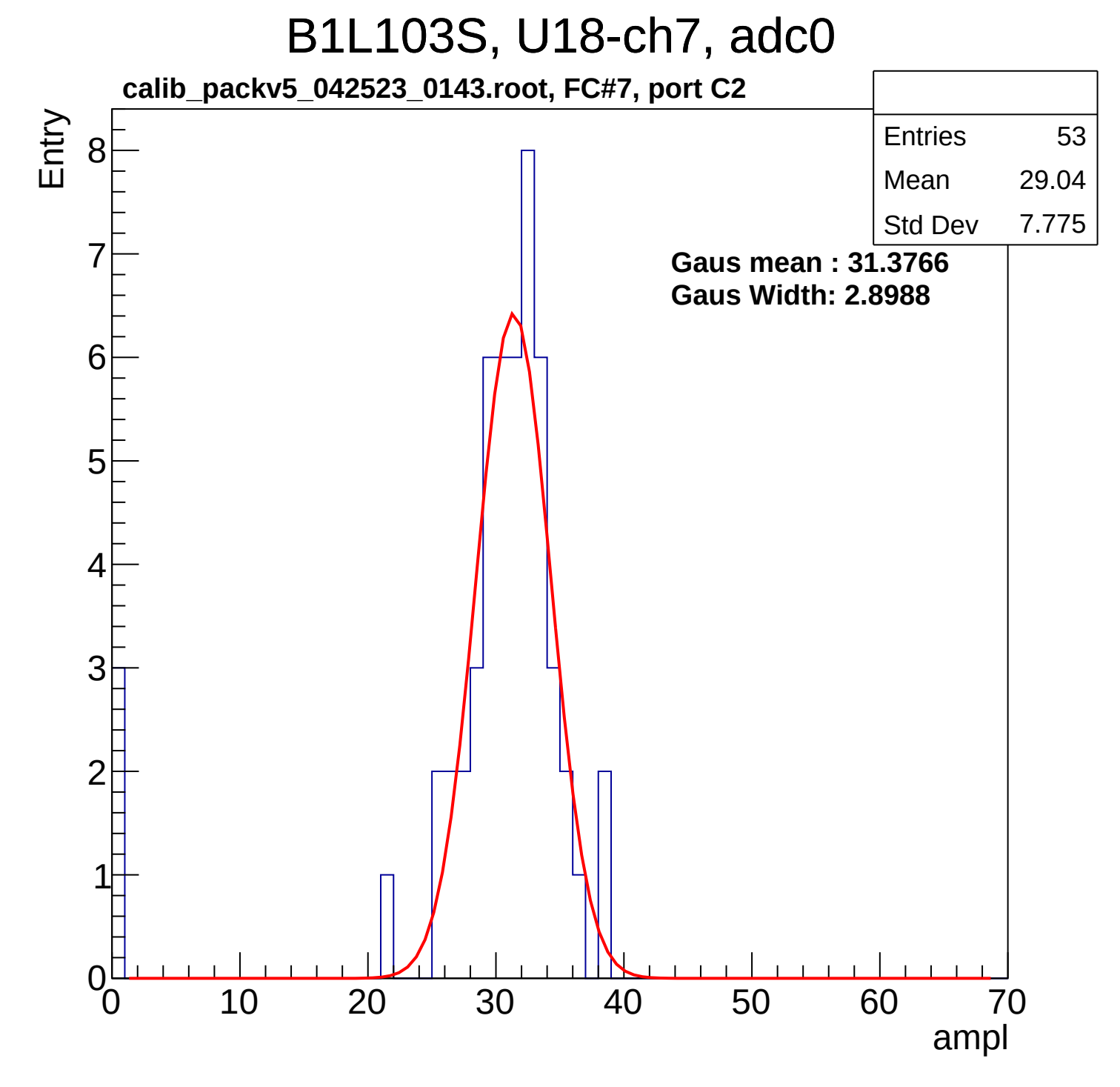
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch6, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 42
Std Dev 29.7
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U18-ch7, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 29.04
Std Dev 7.775
Gaus mean : 31.3766
Gaus Width: 2.8988
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
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40
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60
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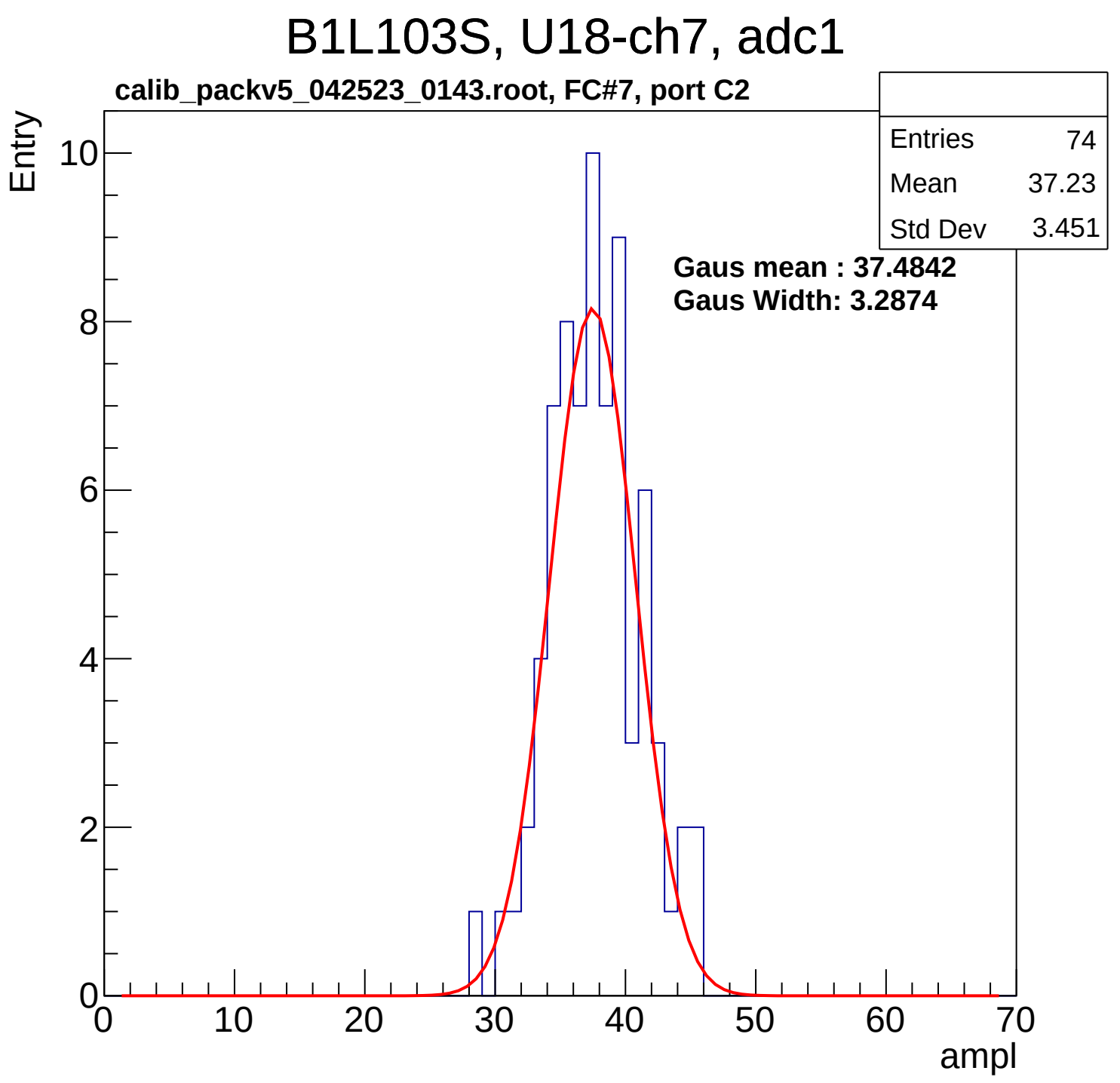
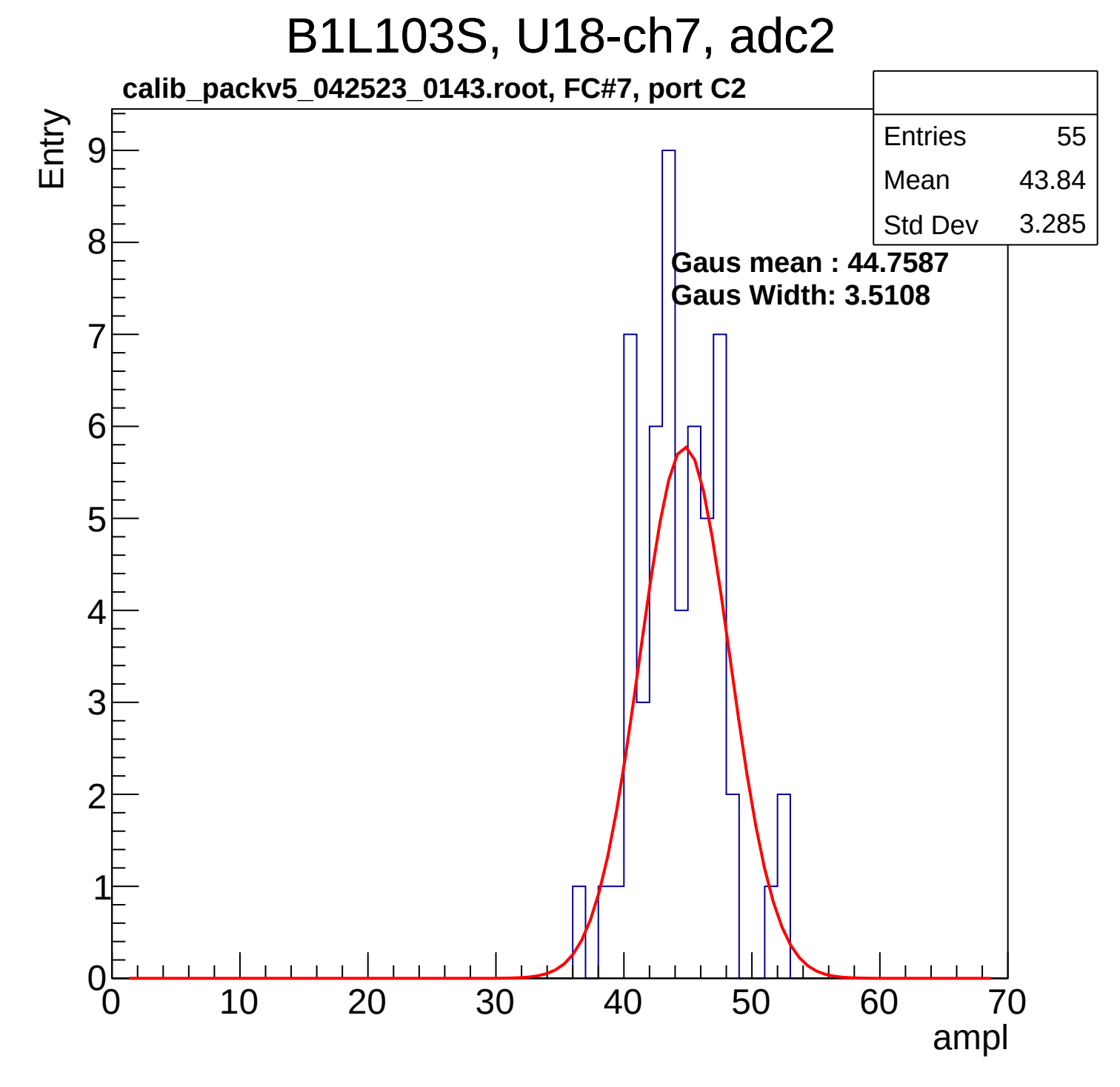

B1L103S, U18-ch7, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 74
Mean 37.23
Std Dev 3.451
Gaus mean : 37.4842
Gaus Width: 3.2874
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch7, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 43.84
Std Dev 3.285
Gaus mean : 44.7587
Gaus Width: 3.5108
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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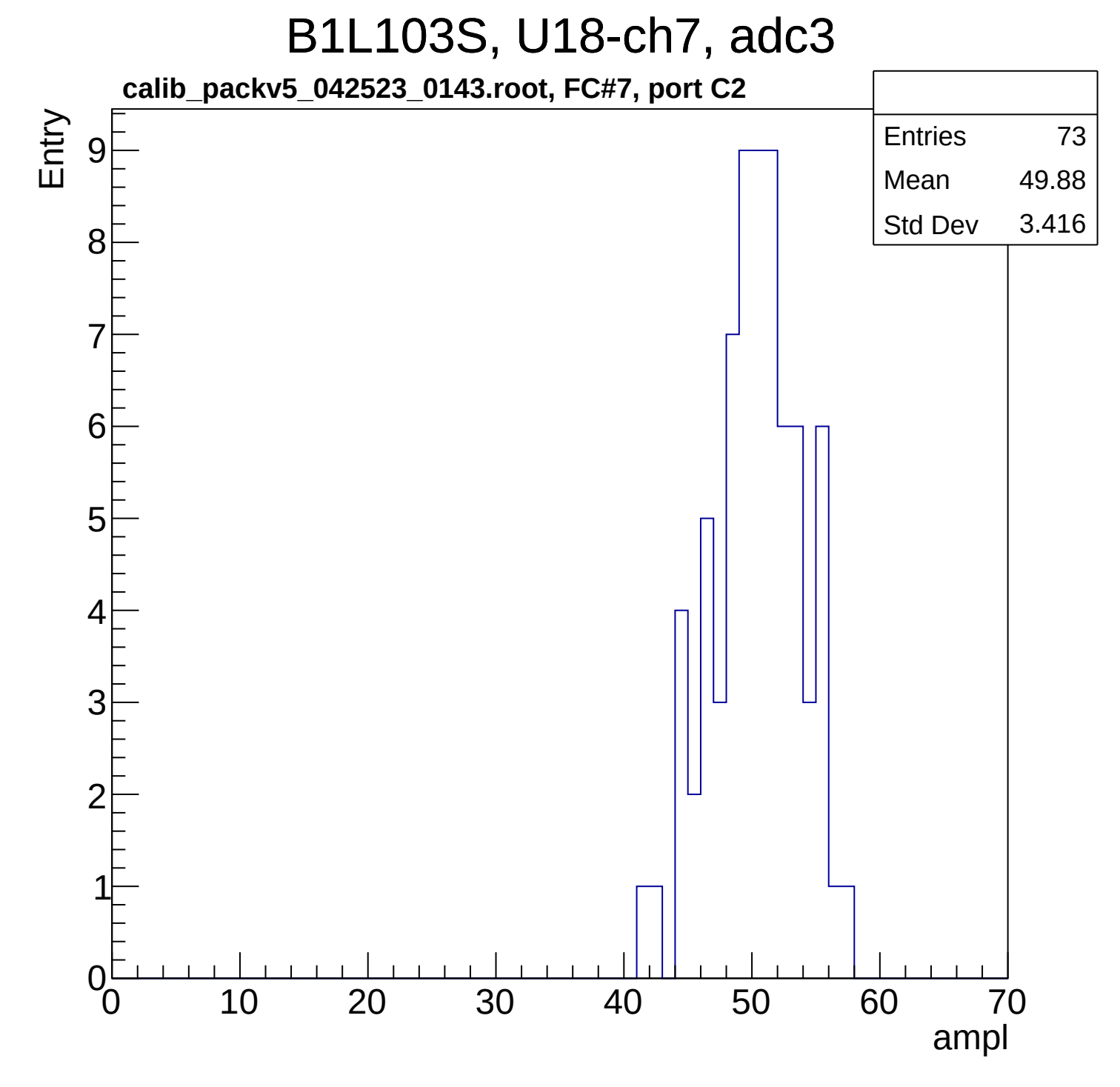
B1L103S, U18-ch7, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 73
Mean 49.88
Std Dev 3.416
Entry
ampl
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3
4
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6
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0
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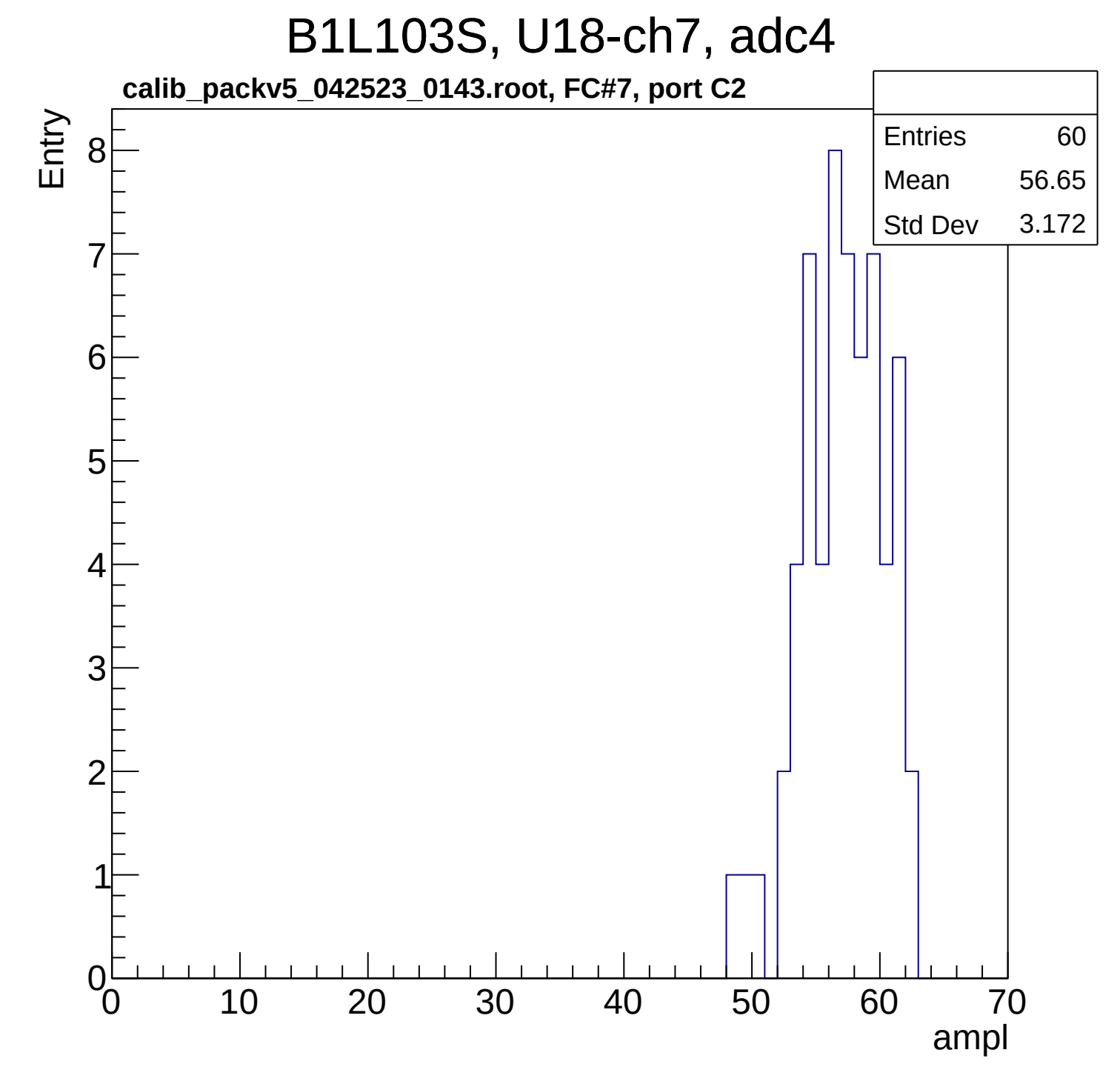
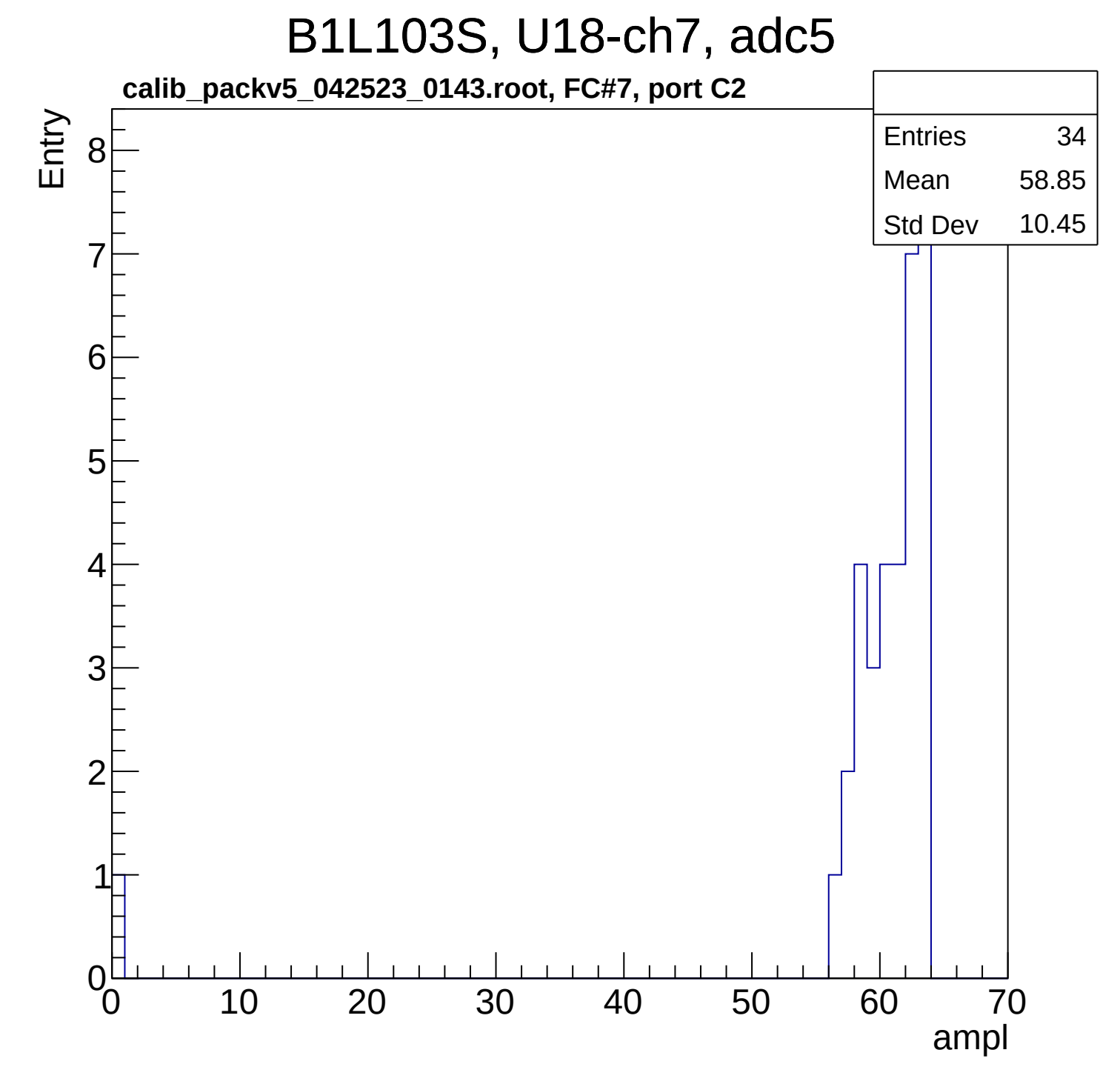

B1L103S, U18-ch7, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 60
Mean 56.65
Std Dev 3.172
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch7, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 34
Mean 58.85
Std Dev 10.45
Entry
ampl
0
1
2
3
4
5
6
7
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0
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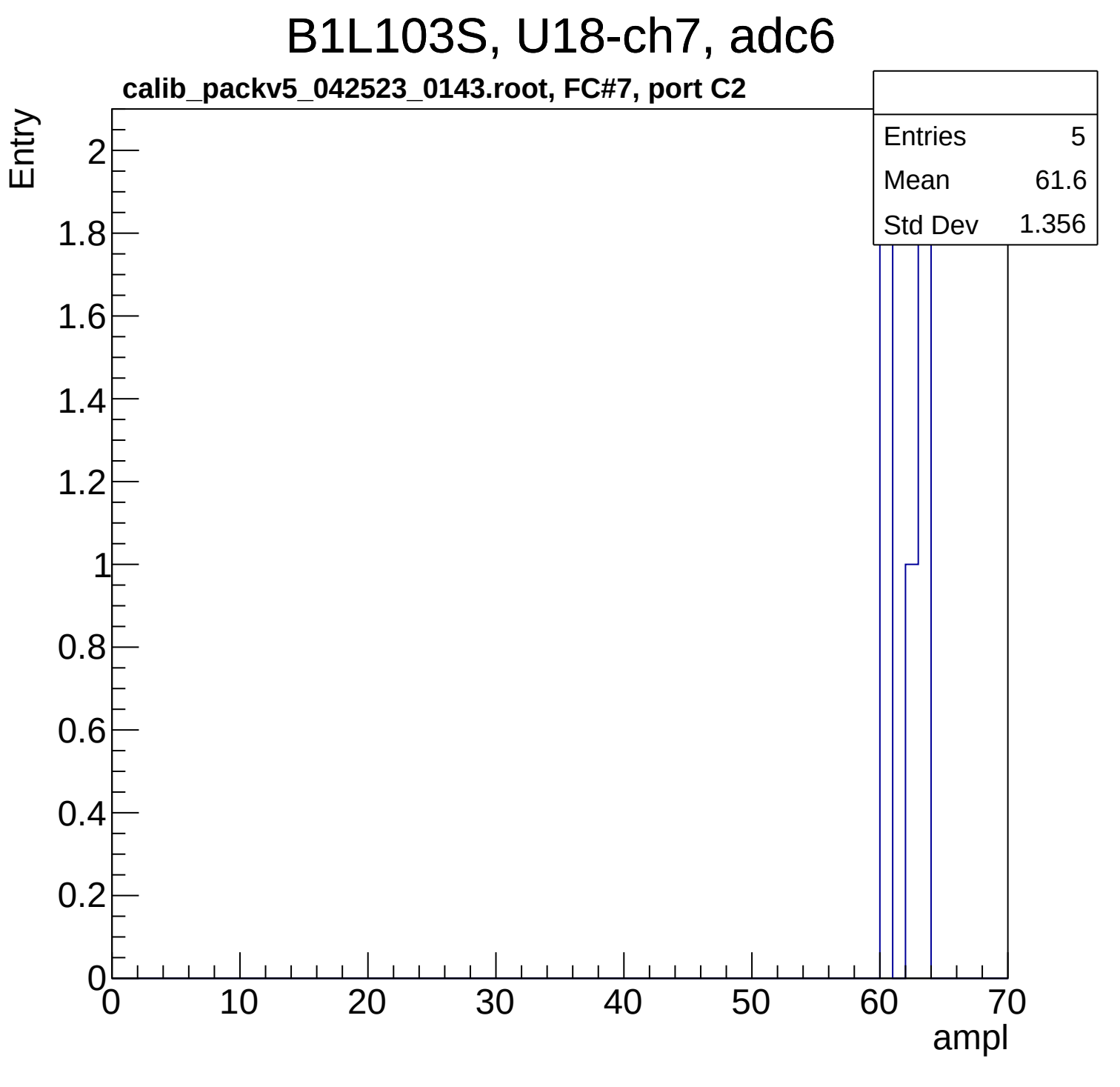
B1L103S, U18-ch7, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 5
Mean 61.6
Std Dev 1.356
Entry
ampl
0
0.2
0.4
0.6
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1.2
1.4
1.6
1.8
2
0
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40
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60
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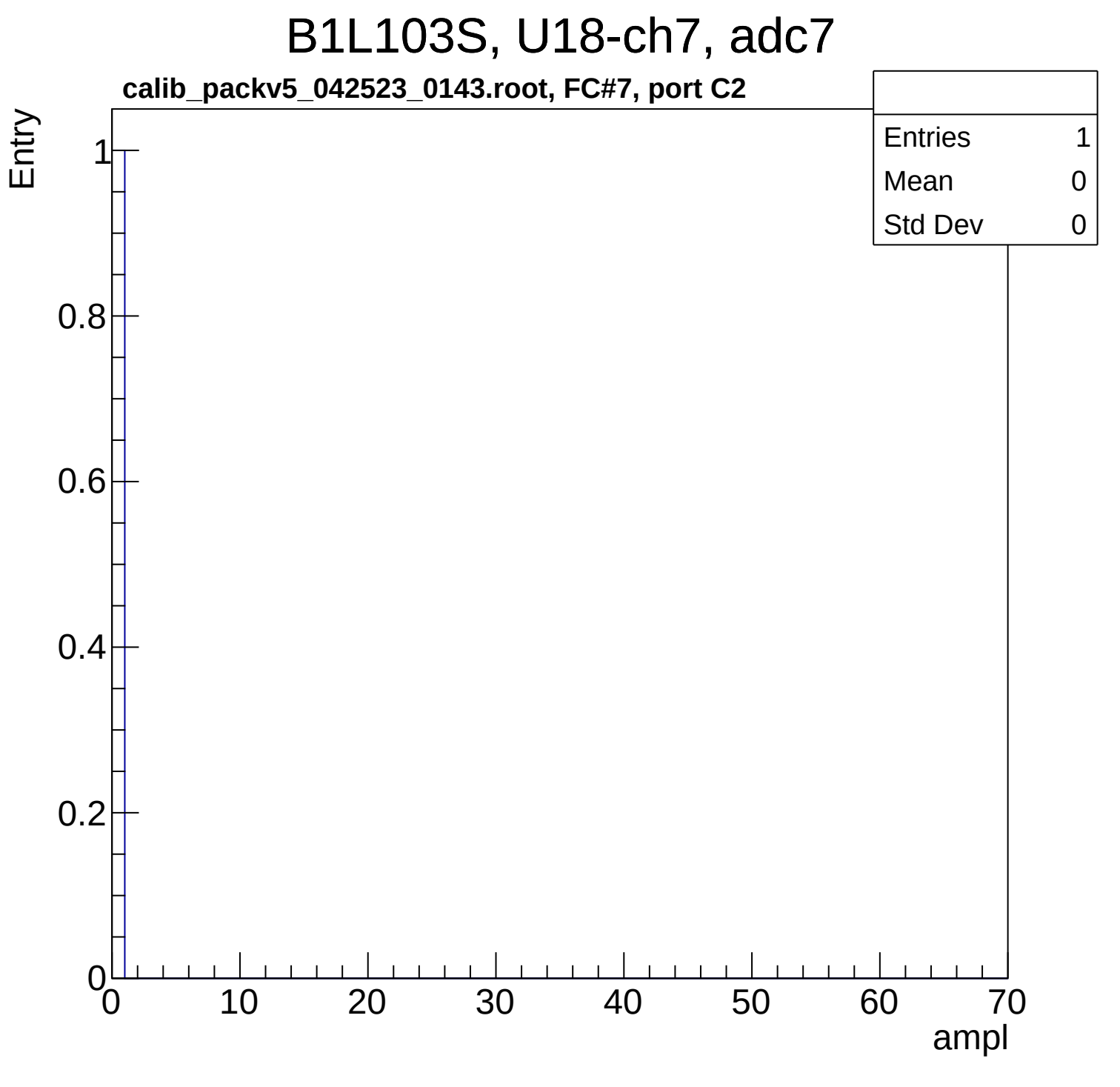
B1L103S, U18-ch7, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
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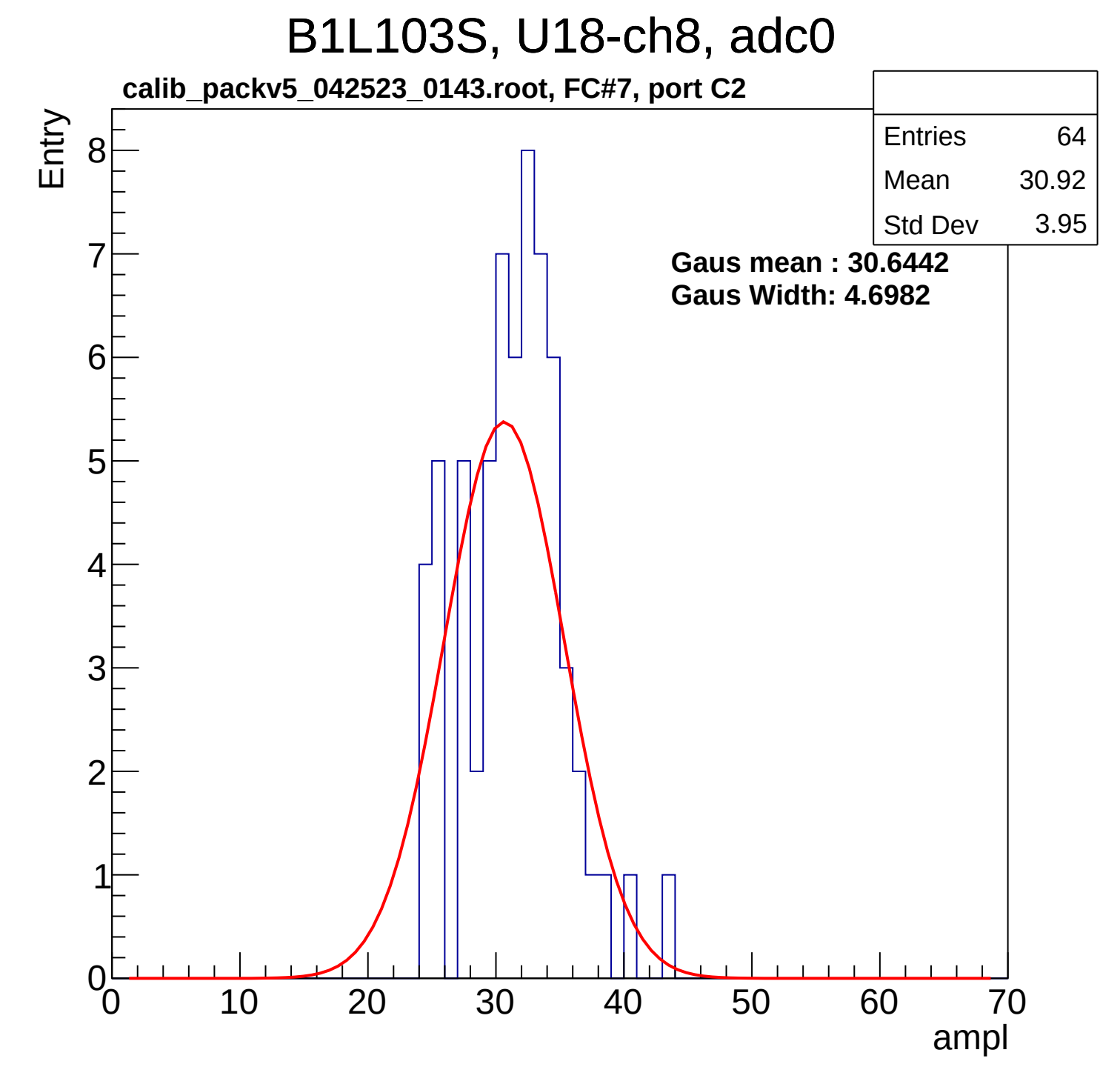
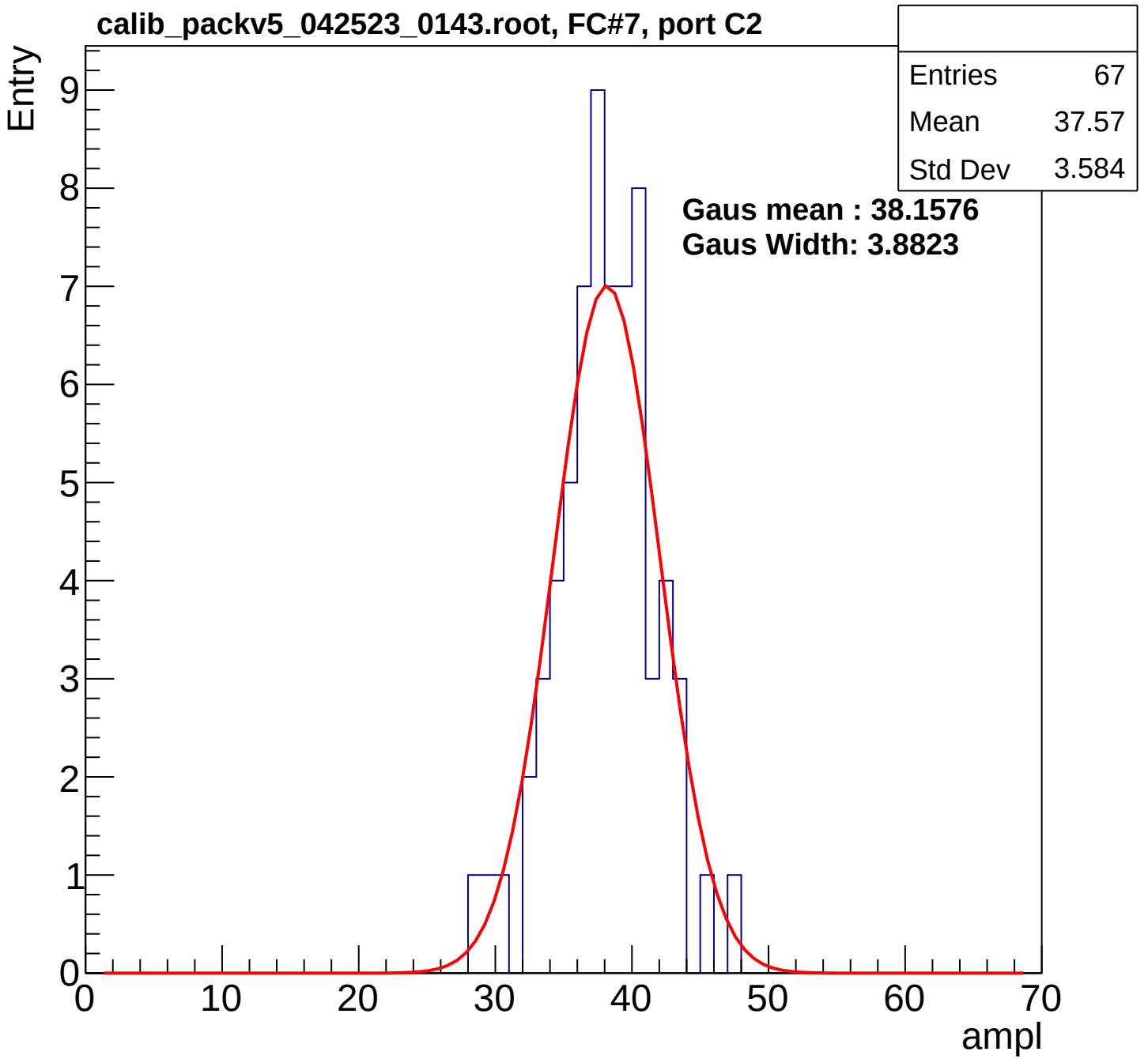
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch8, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 30.92
Std Dev 3.95
Gaus mean : 30.6442
Gaus Width: 4.6982
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch8, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 37.57
Std Dev 3.584
Gaus mean : 38.1576
Gaus Width: 3.8823
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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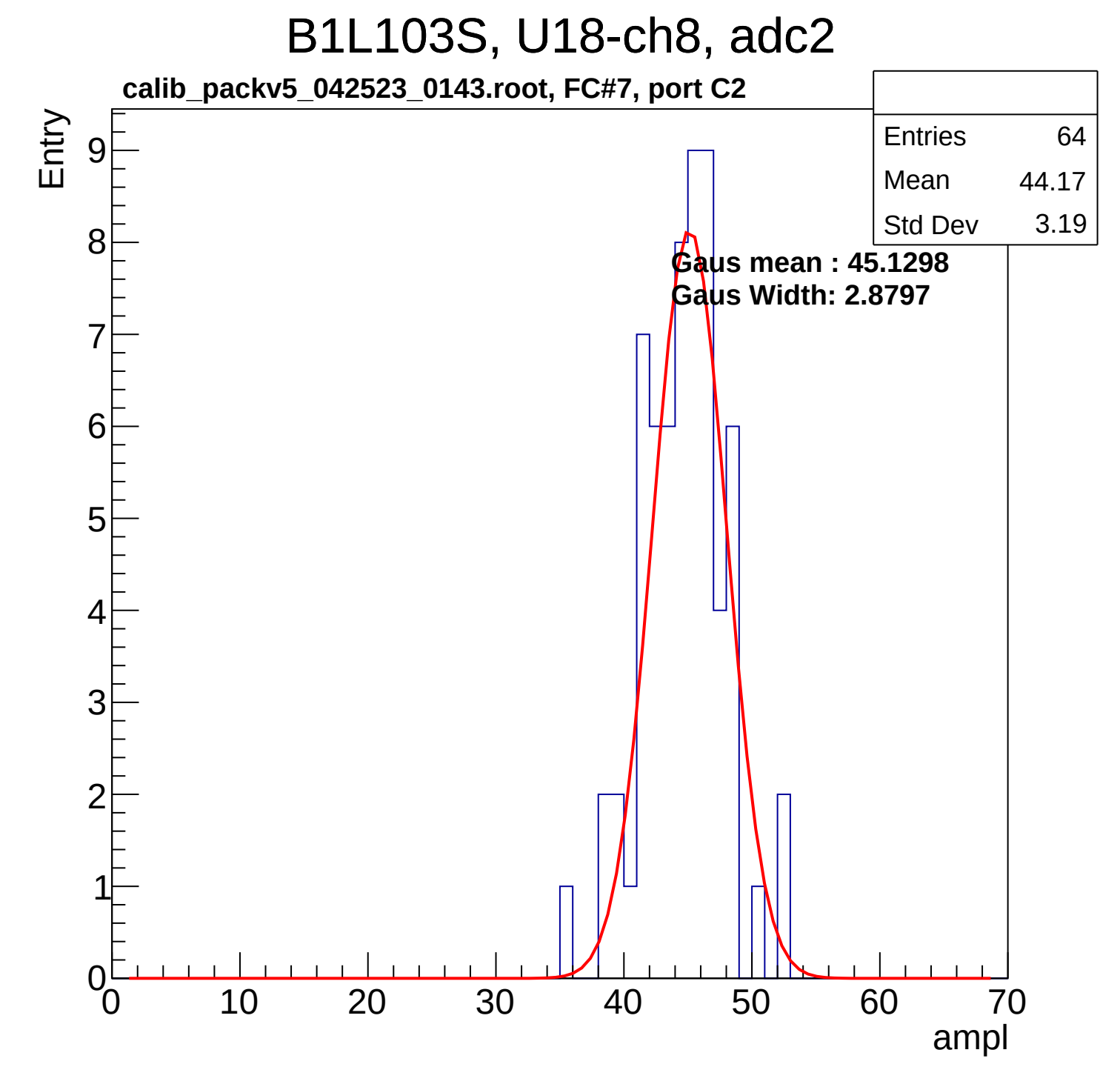
B1L103S, U18-ch8, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 44.17
Std Dev 3.19
Gaus mean : 45.1298
Gaus Width: 2.8797
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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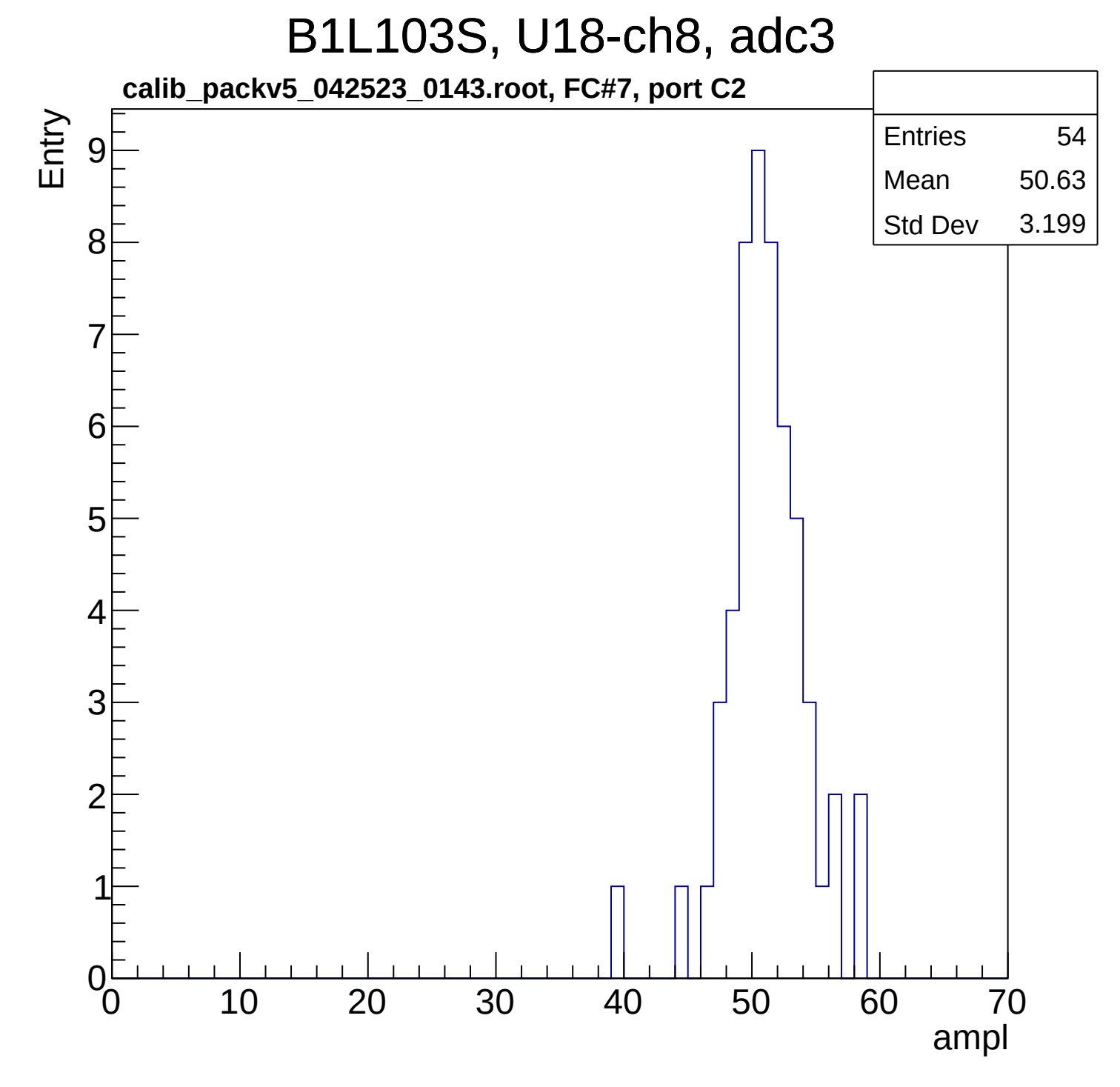
B1L103S, U18-ch8, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 54
Mean 50.63
Std Dev 3.199
Entry
ampl
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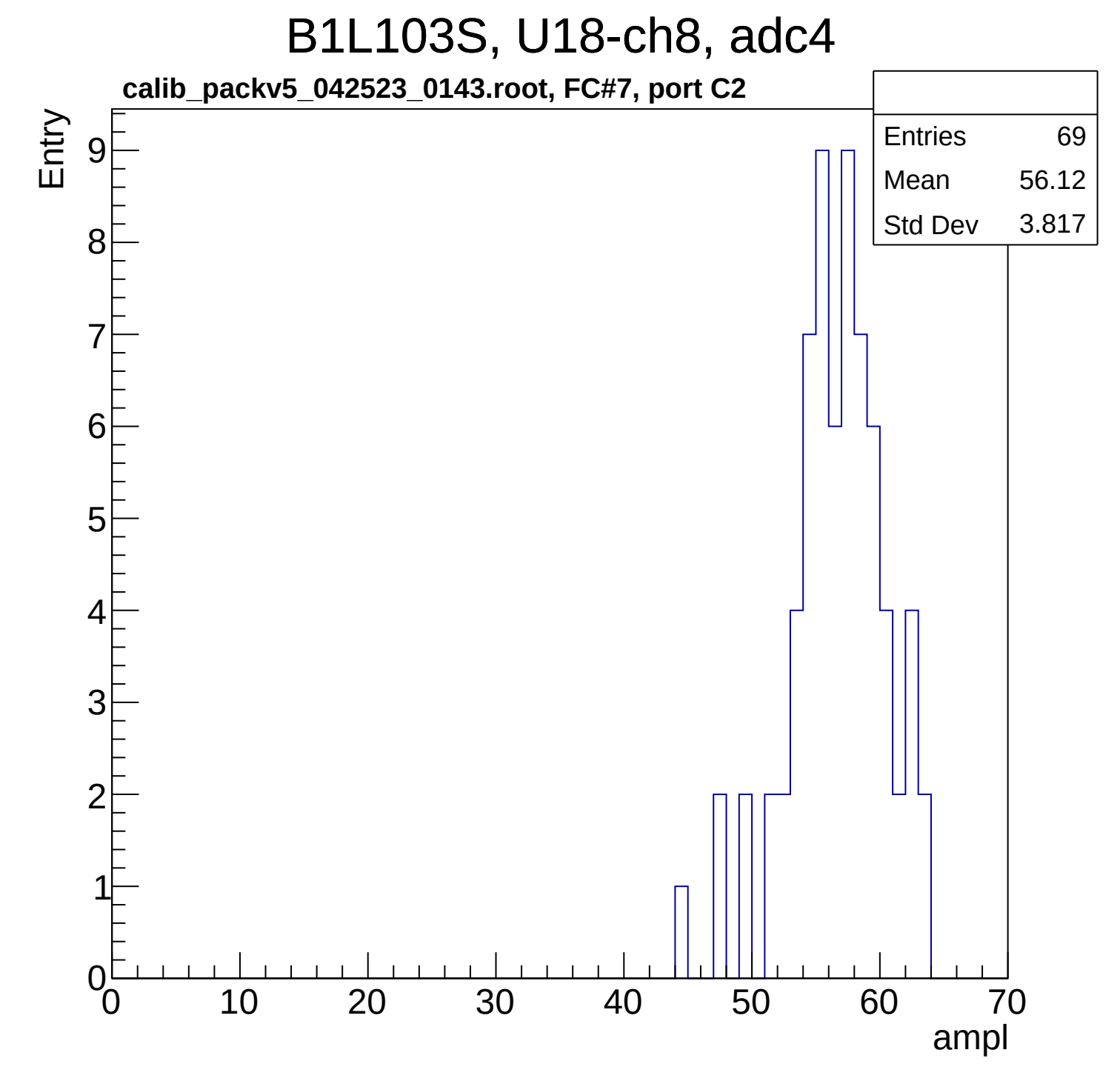
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch8, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 56.12
Std Dev 3.817
Entry
ampl
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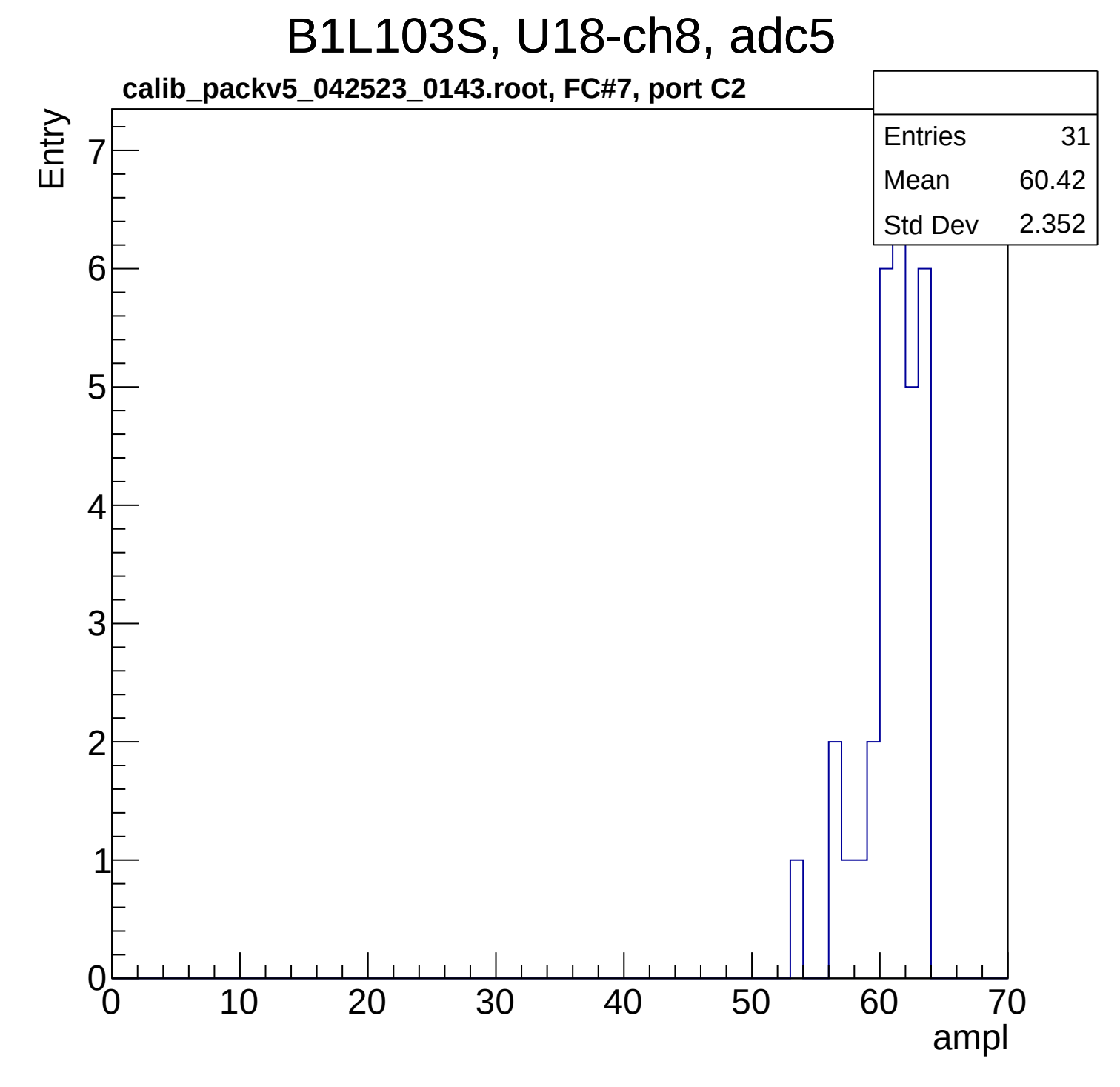
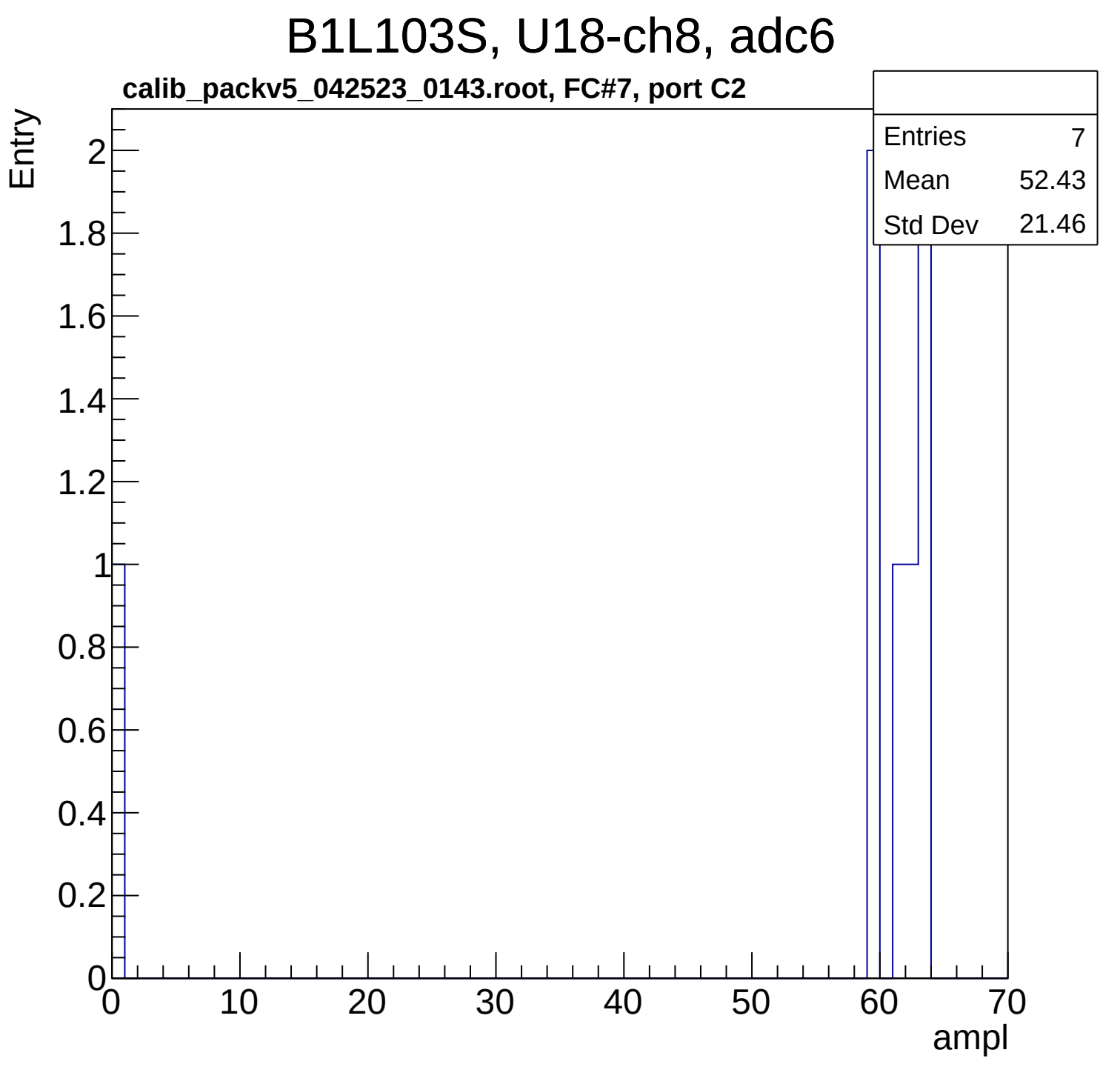
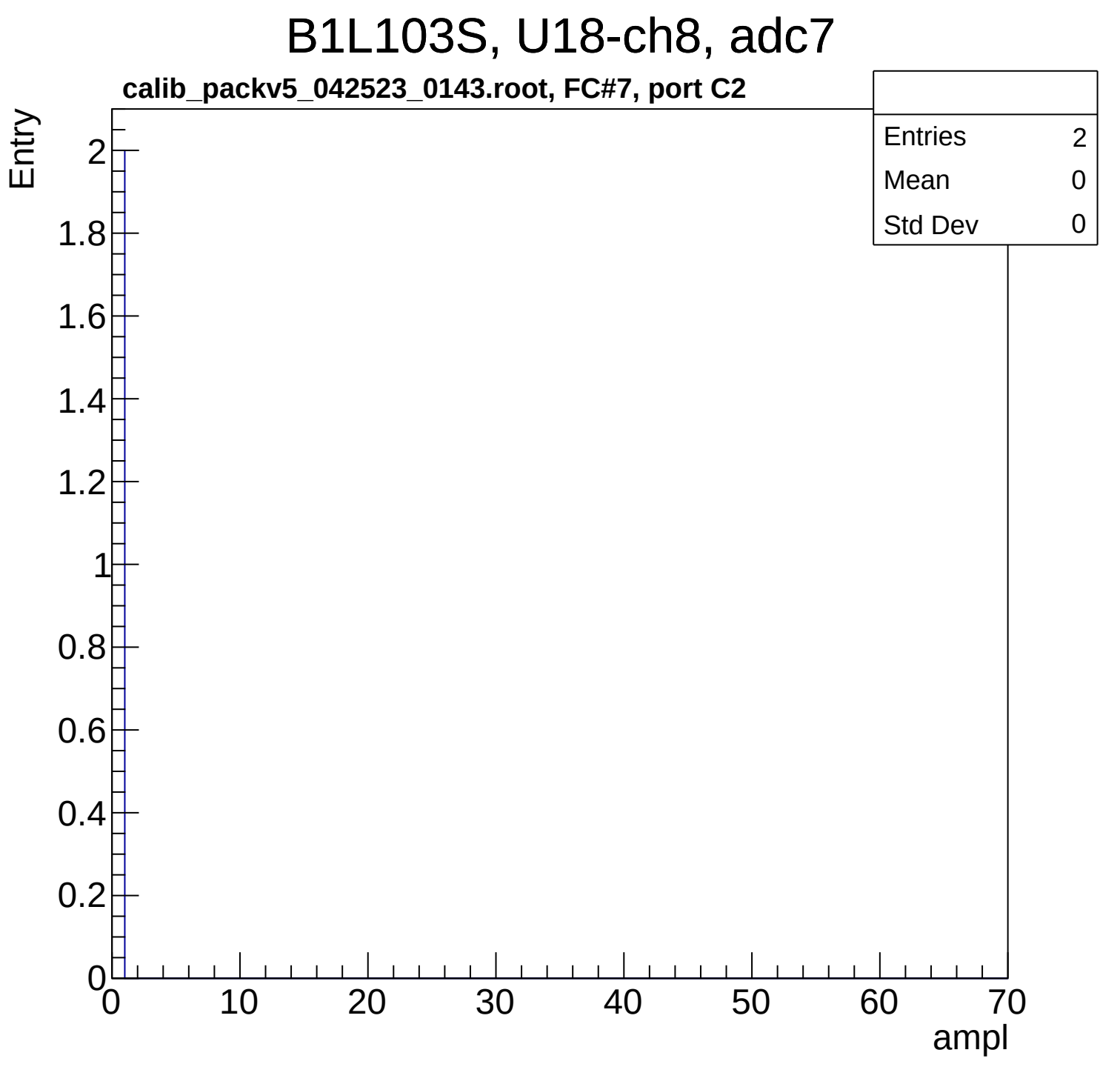
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch8, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 31
Mean 60.42
Std Dev 2.352
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch8, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 7
Mean 52.43
Std Dev 21.46
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U18-ch8, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
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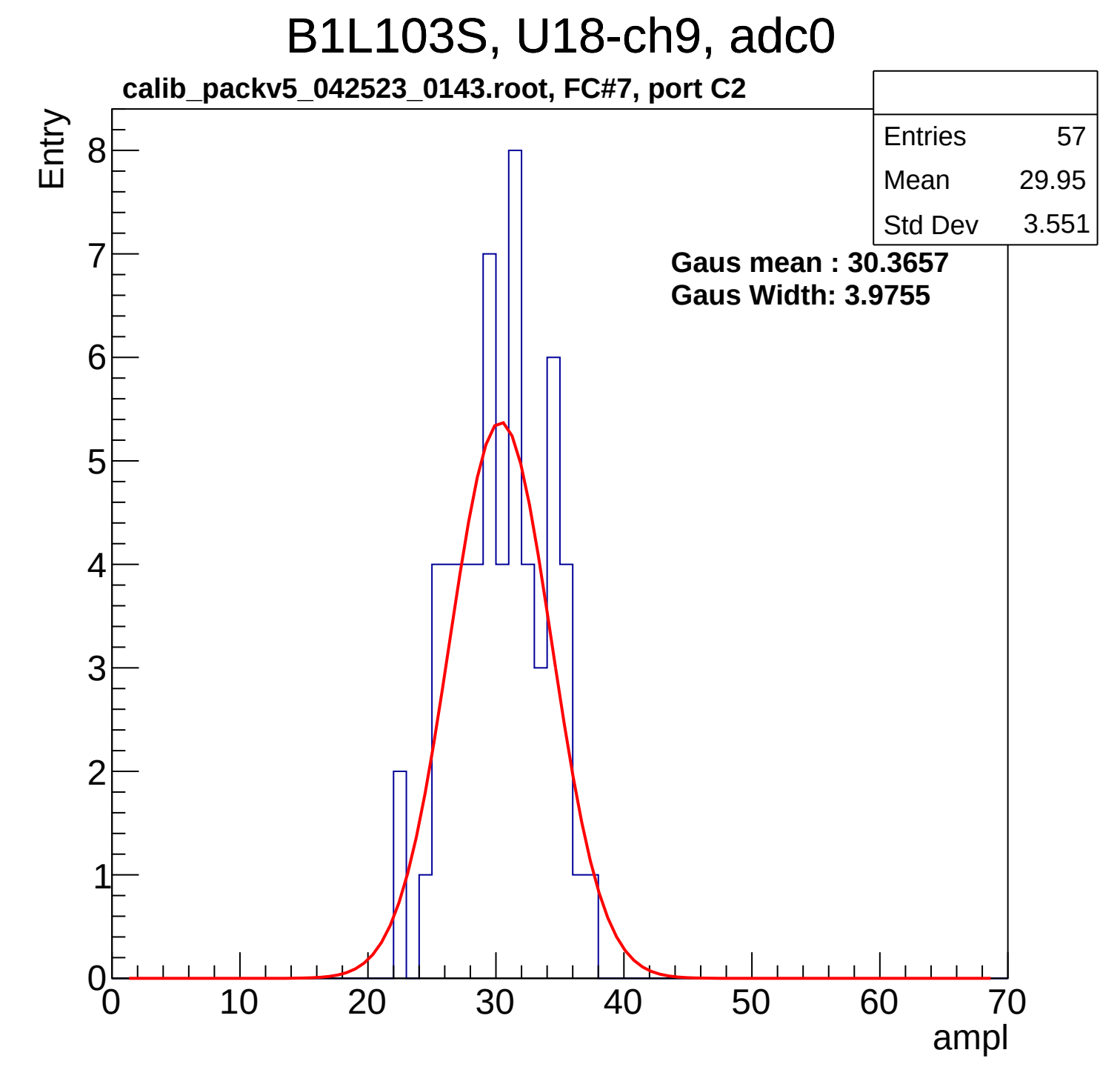
30
40
50
60
70
ampl


B1L103S, U18-ch9, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 29.95
Std Dev 3.551
Gaus mean : 30.3657
Gaus Width: 3.9755
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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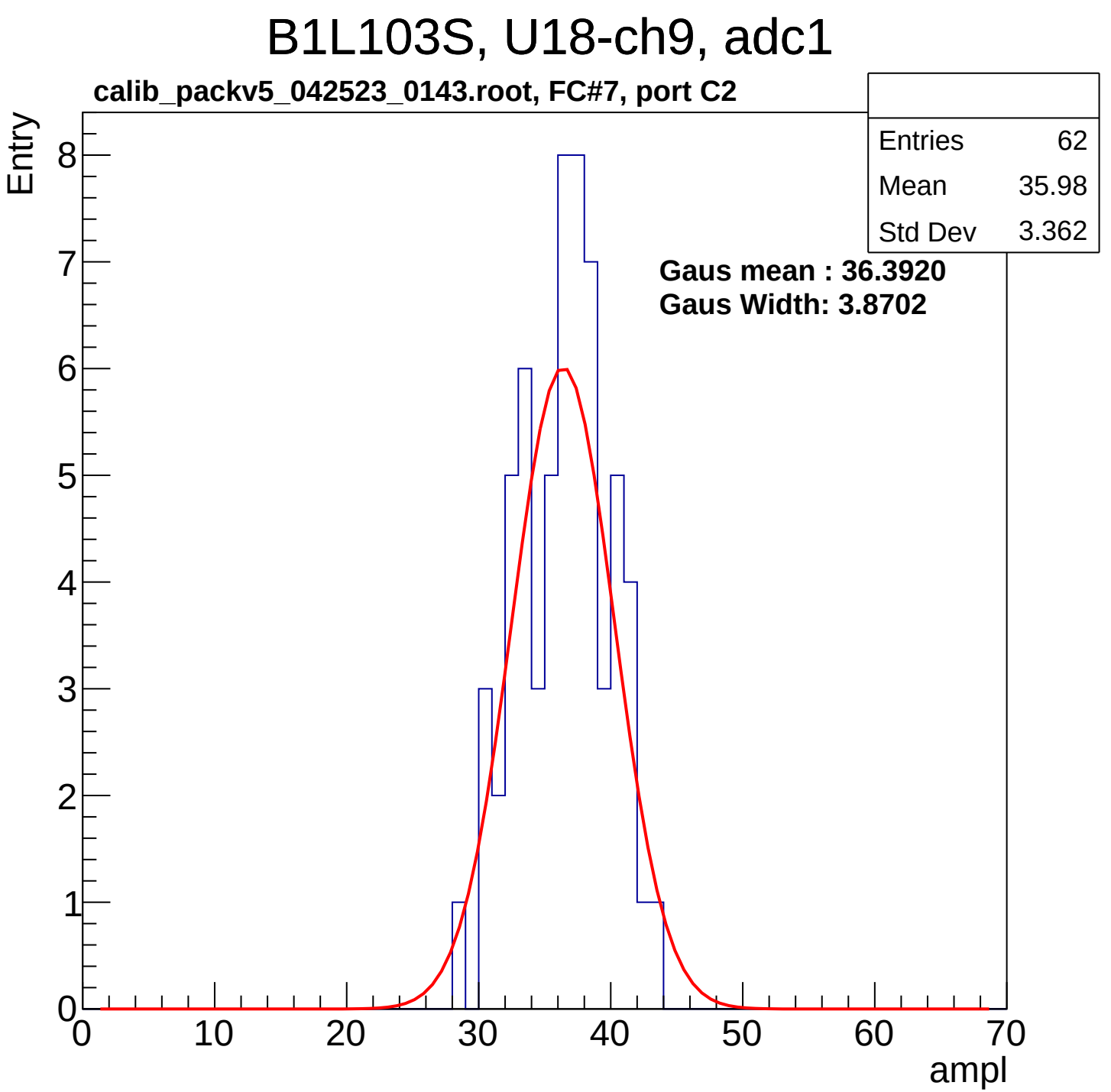
B1L103S, U18-ch9, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 62
Mean 35.98
Std Dev 3.362
Gaus mean : 36.3920
Gaus Width: 3.8702
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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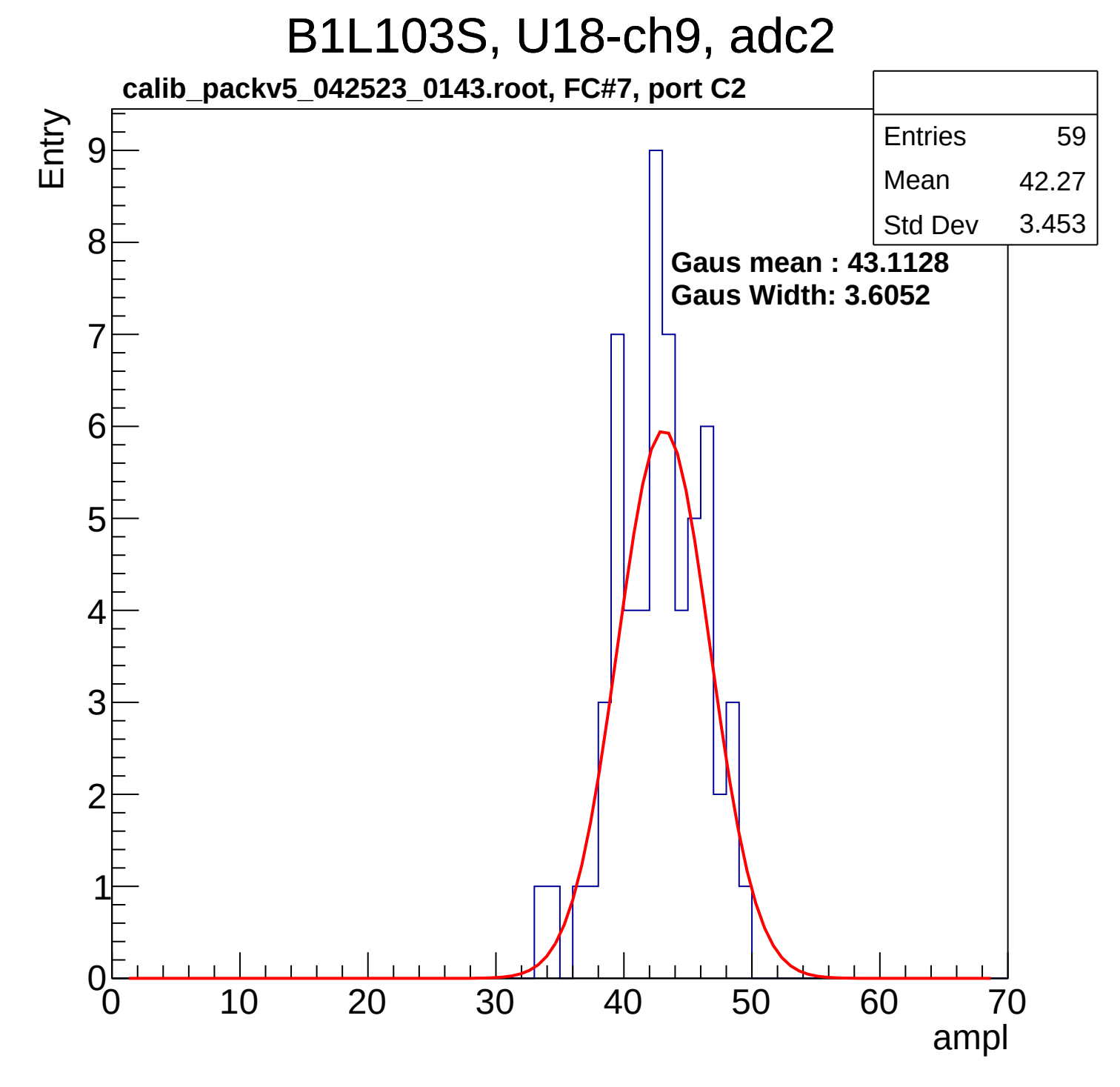
B1L103S, U18-ch9, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 42.27
Std Dev 3.453
Gaus mean : 43.1128
Gaus Width: 3.6052
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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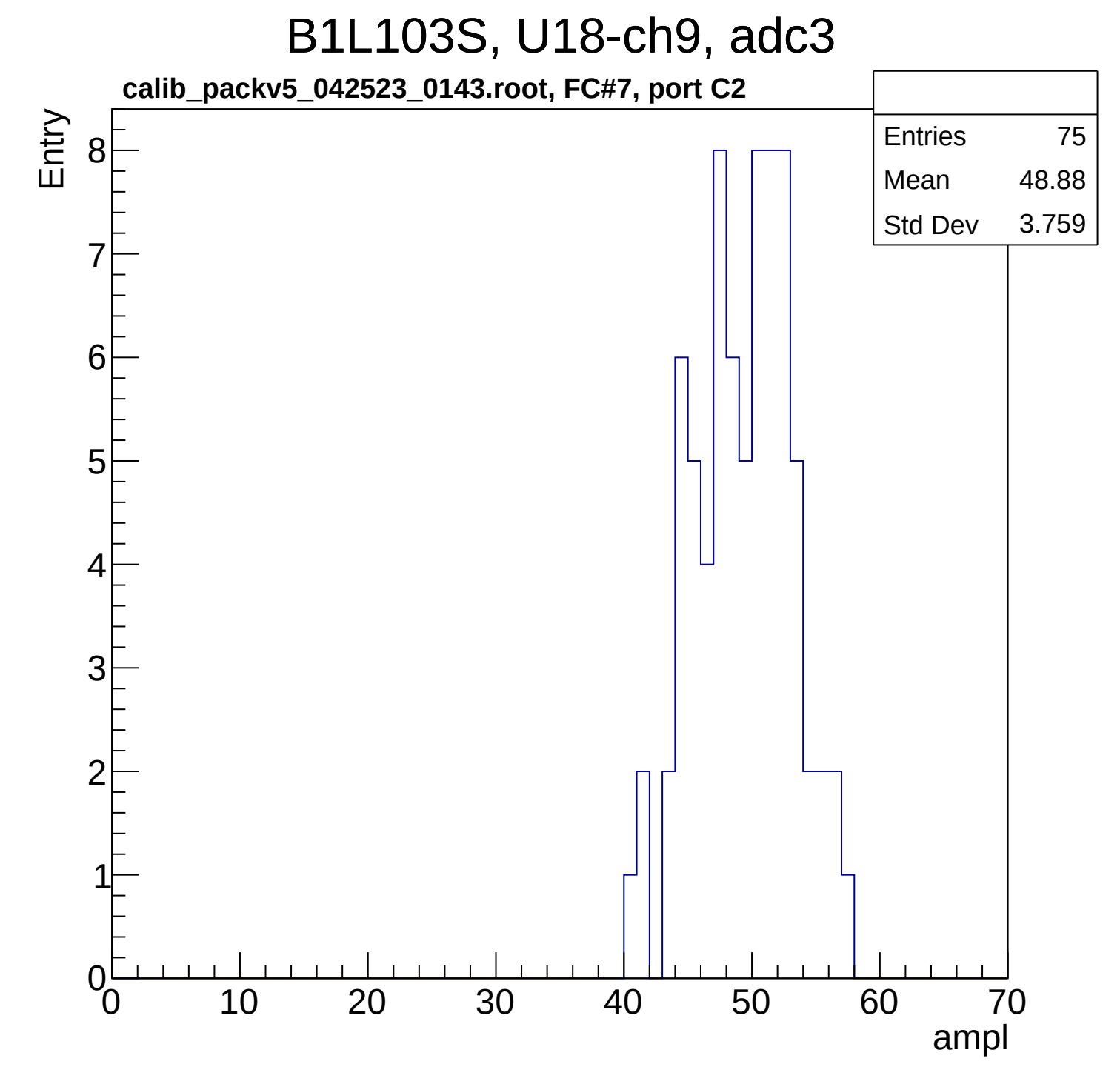
B1L103S, U18-ch9, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 75
Mean 48.88
Std Dev 3.759
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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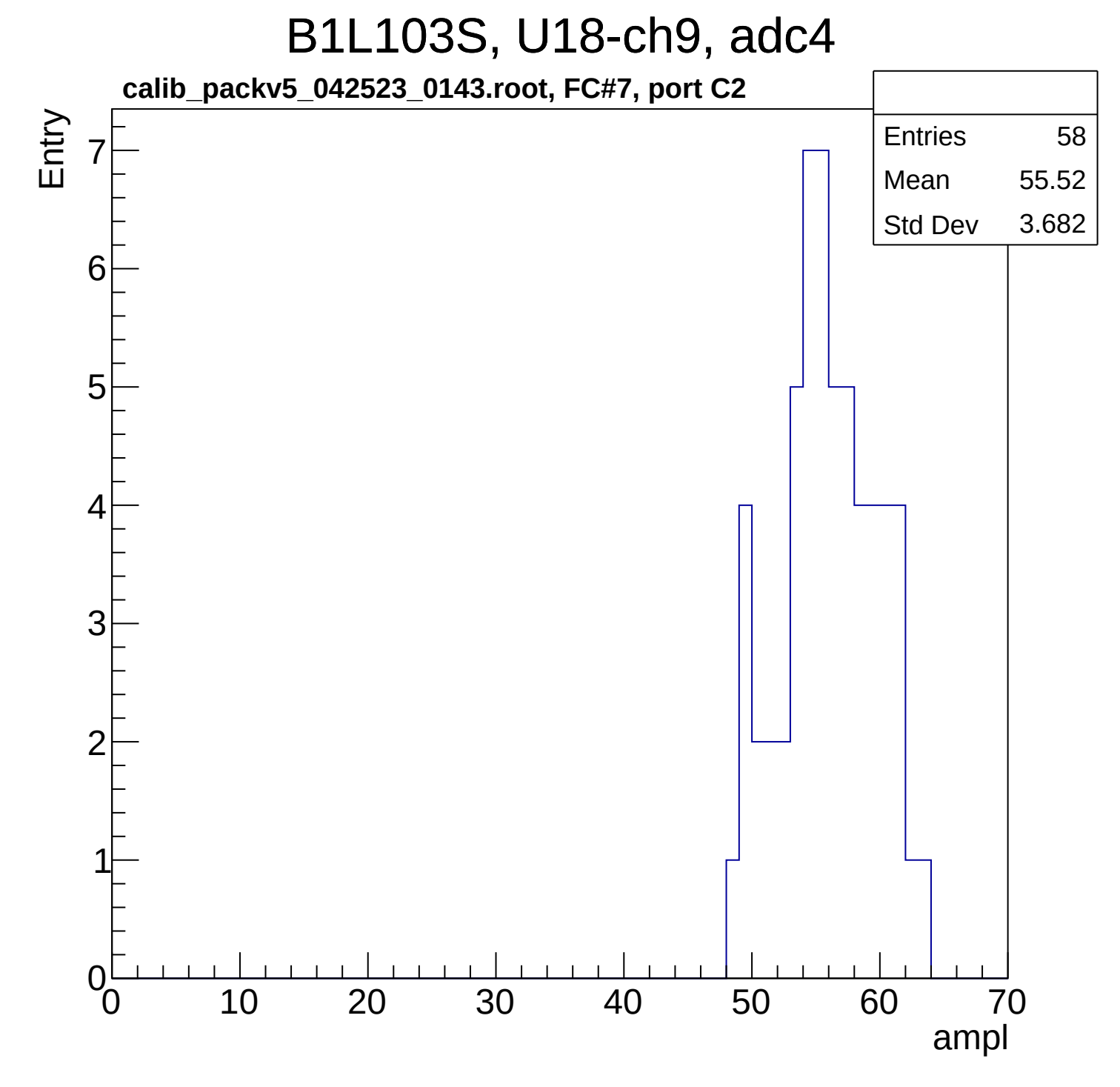
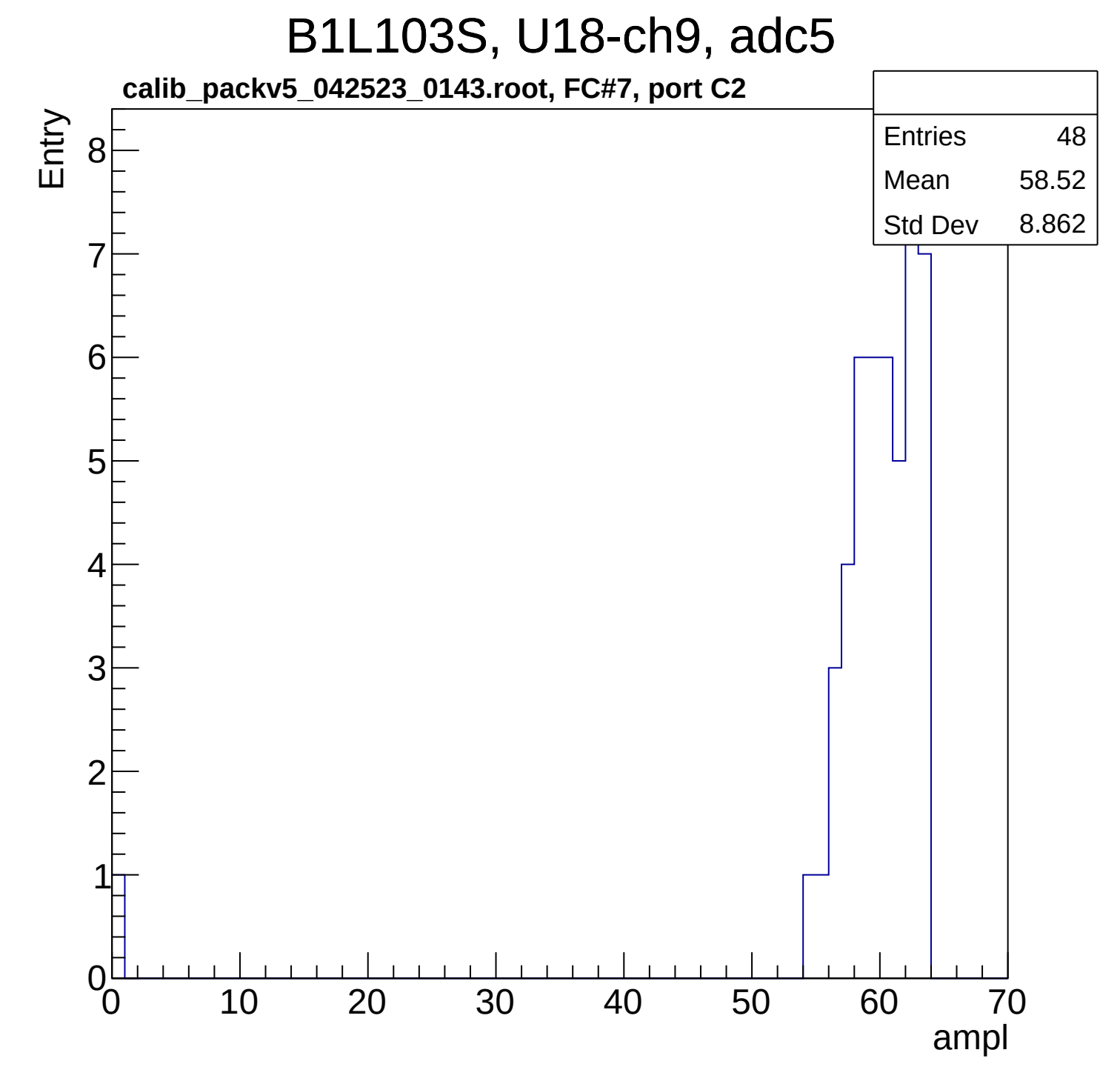

B1L103S, U18-ch9, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 58
Mean 55.52
Std Dev 3.682
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch9, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 48
Mean 58.52
Std Dev 8.862
Entry
ampl
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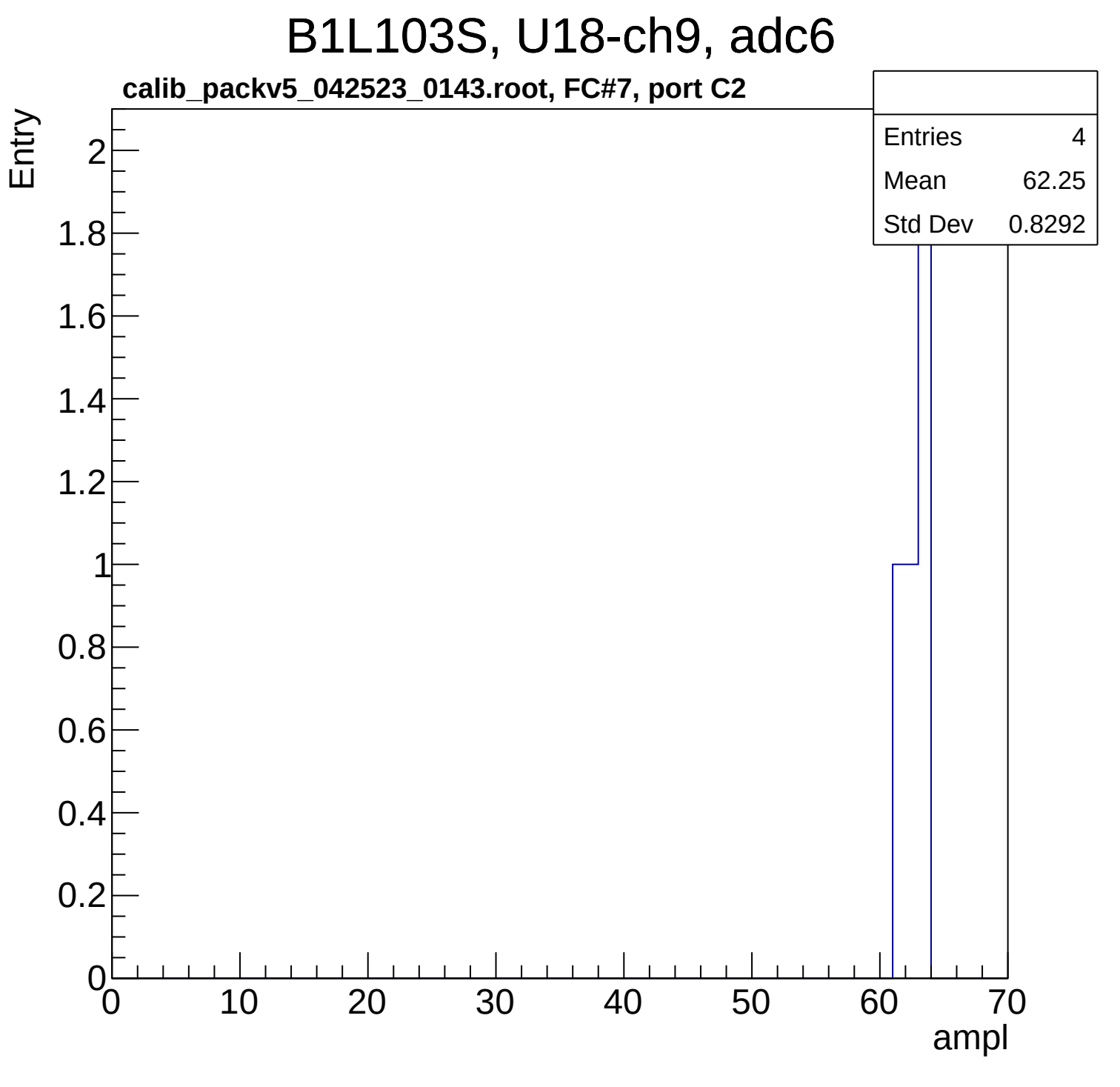
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch9, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 4
Mean 62.25
Std Dev 0.8292
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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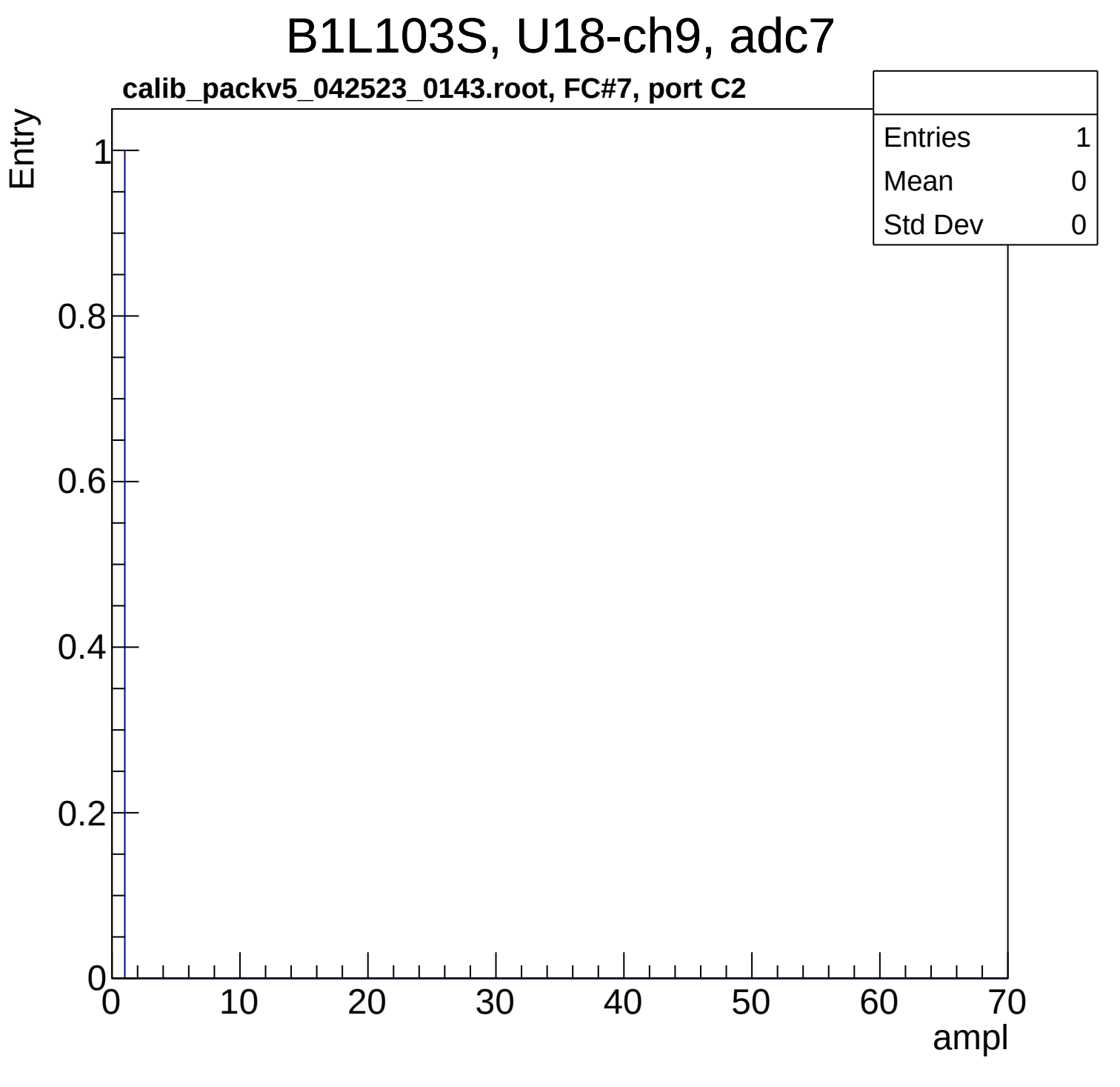
20
30
40
50
60
70


B1L103S, U18-ch9, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
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0.8
0.6
0.4
0.2
0
0
10
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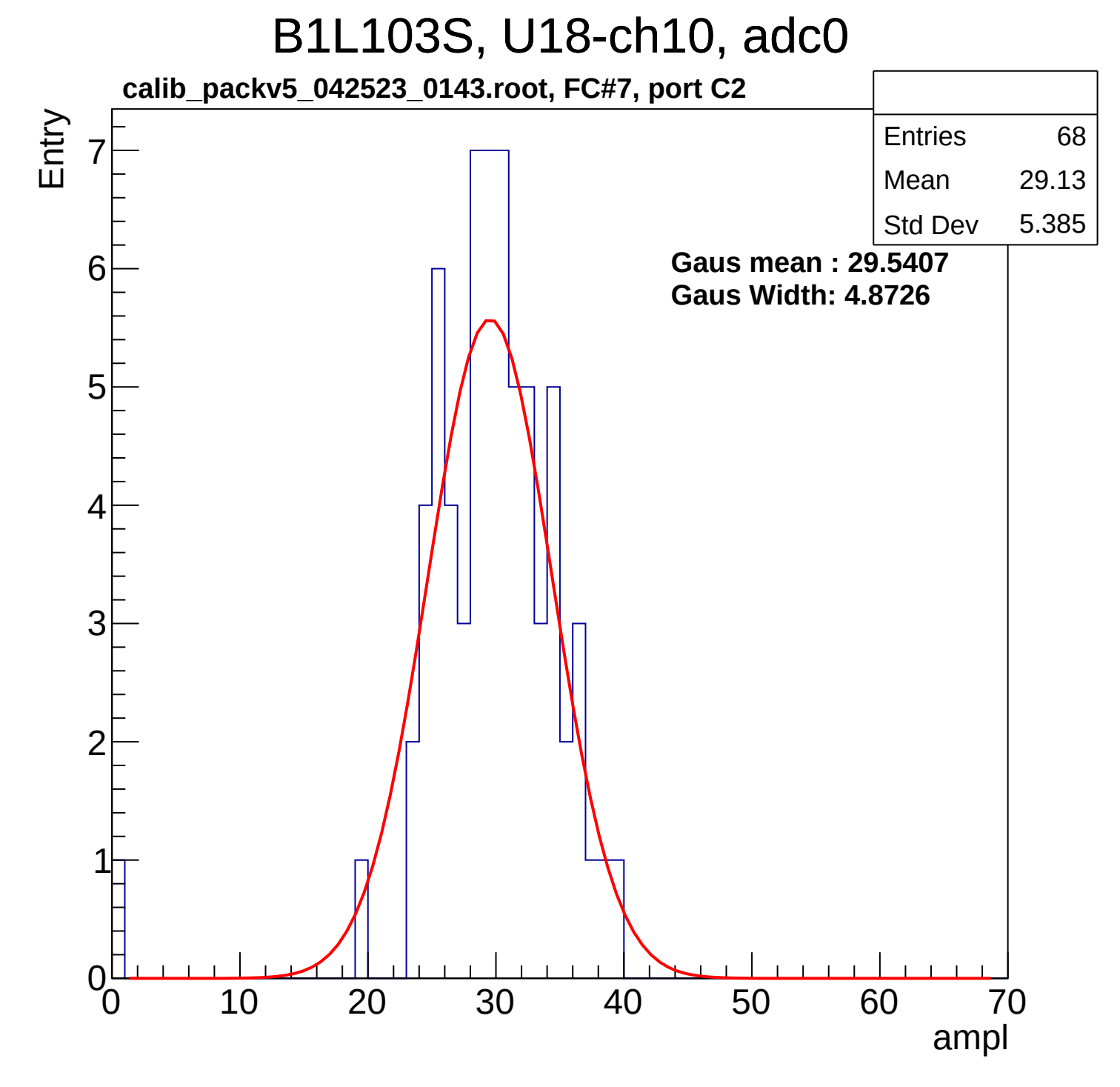
50
60
70
ampl


B1L103S, U18-ch10, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 29.13
Std Dev 5.385
Gaus mean : 29.5407
Gaus Width: 4.8726
Entry
ampl
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1
2
3
4
5
6
7
0
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20
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60
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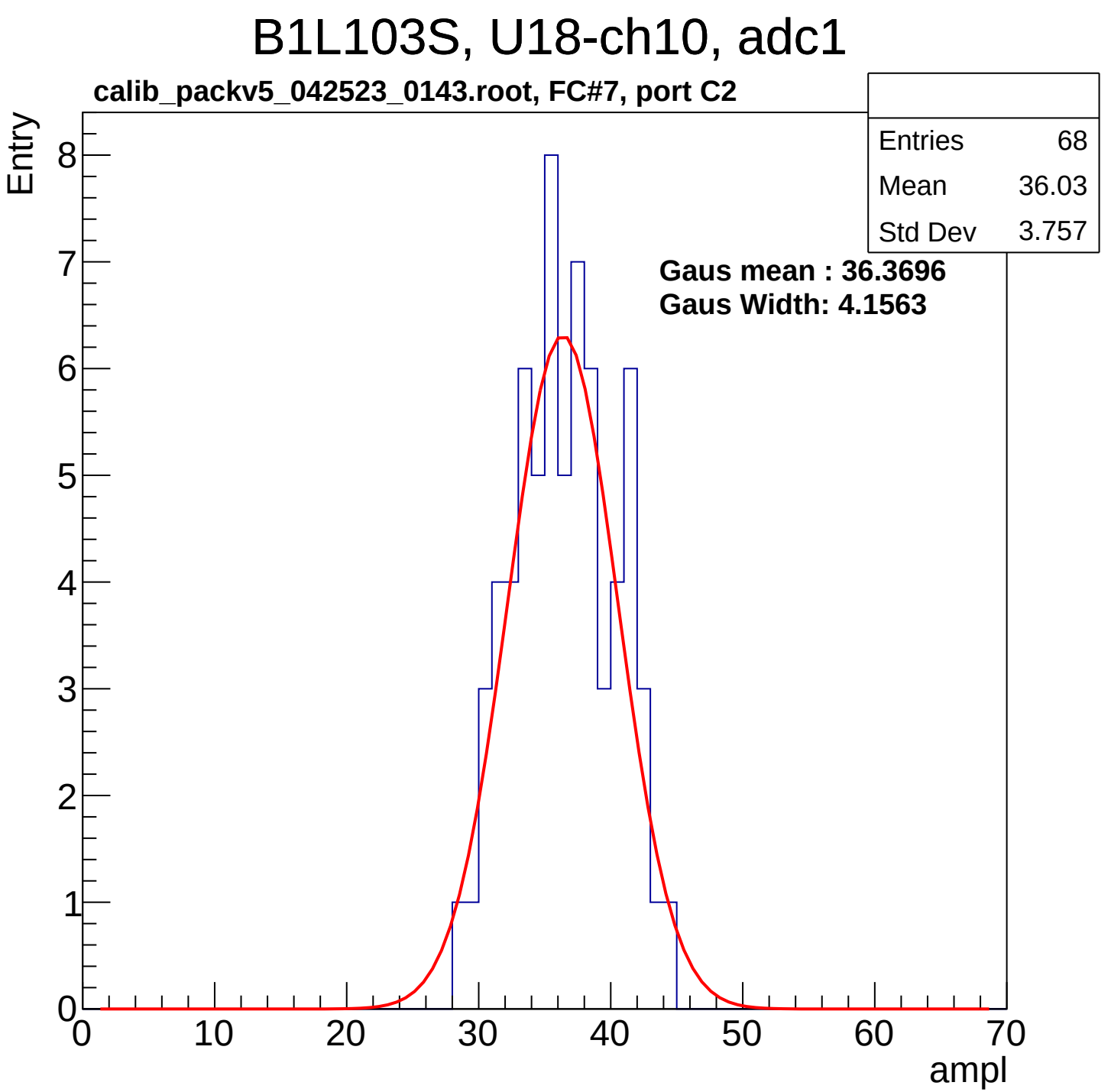
B1L103S, U18-ch10, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 36.03
Std Dev 3.757
Gaus mean : 36.3696
Gaus Width: 4.1563
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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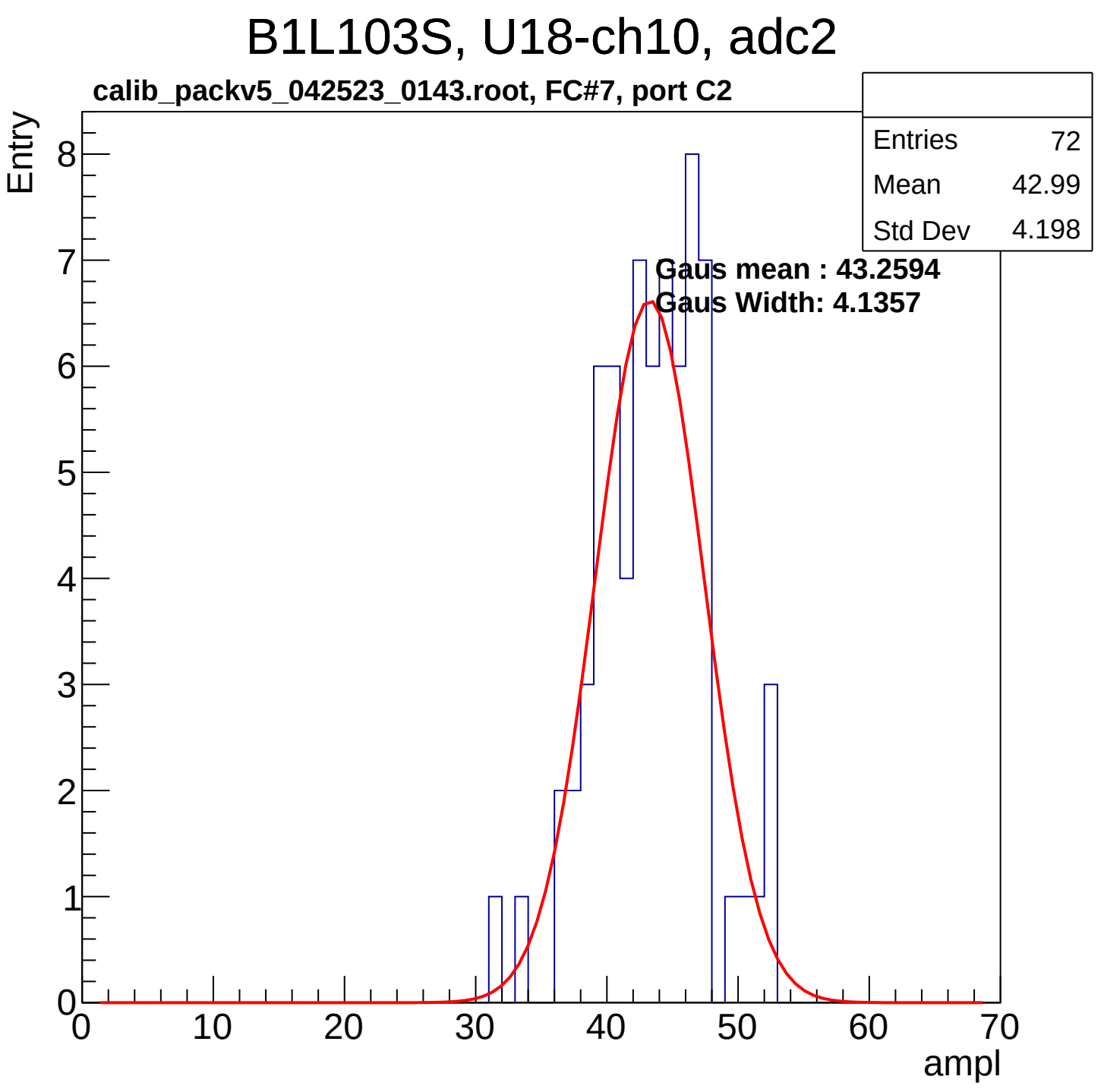
40
50
60
70


B1L103S, U18-ch10, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 72
Mean 42.99
Std Dev 4.198
Gaus mean : 43.2594
Gaus Width: 4.1357
Entry
ampl
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2
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4
5
6
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0
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40
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60
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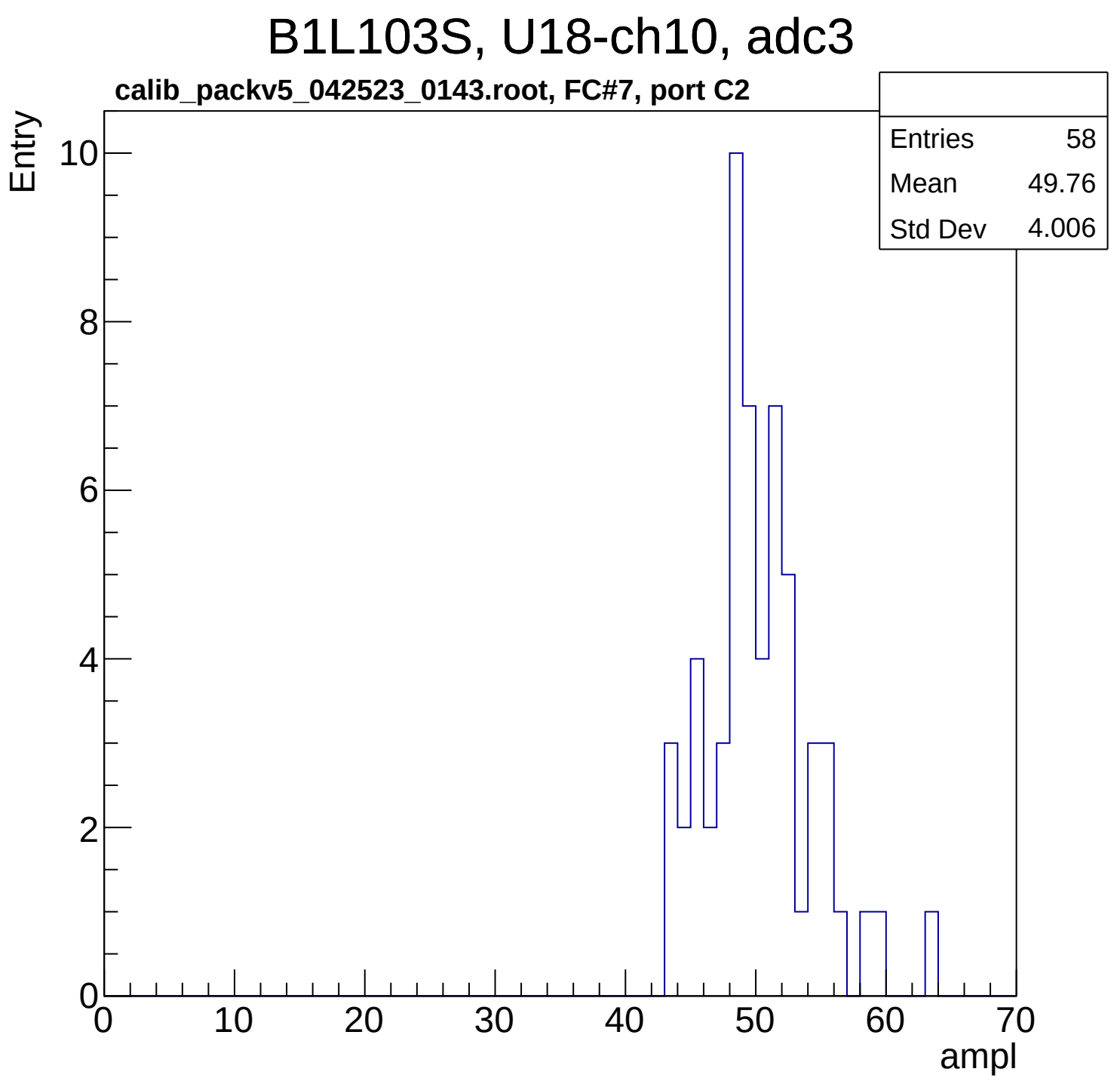
B1L103S, U18-ch10, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 58
Mean 49.76
Std Dev 4.006
Entry
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4
6
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10
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10
20
30
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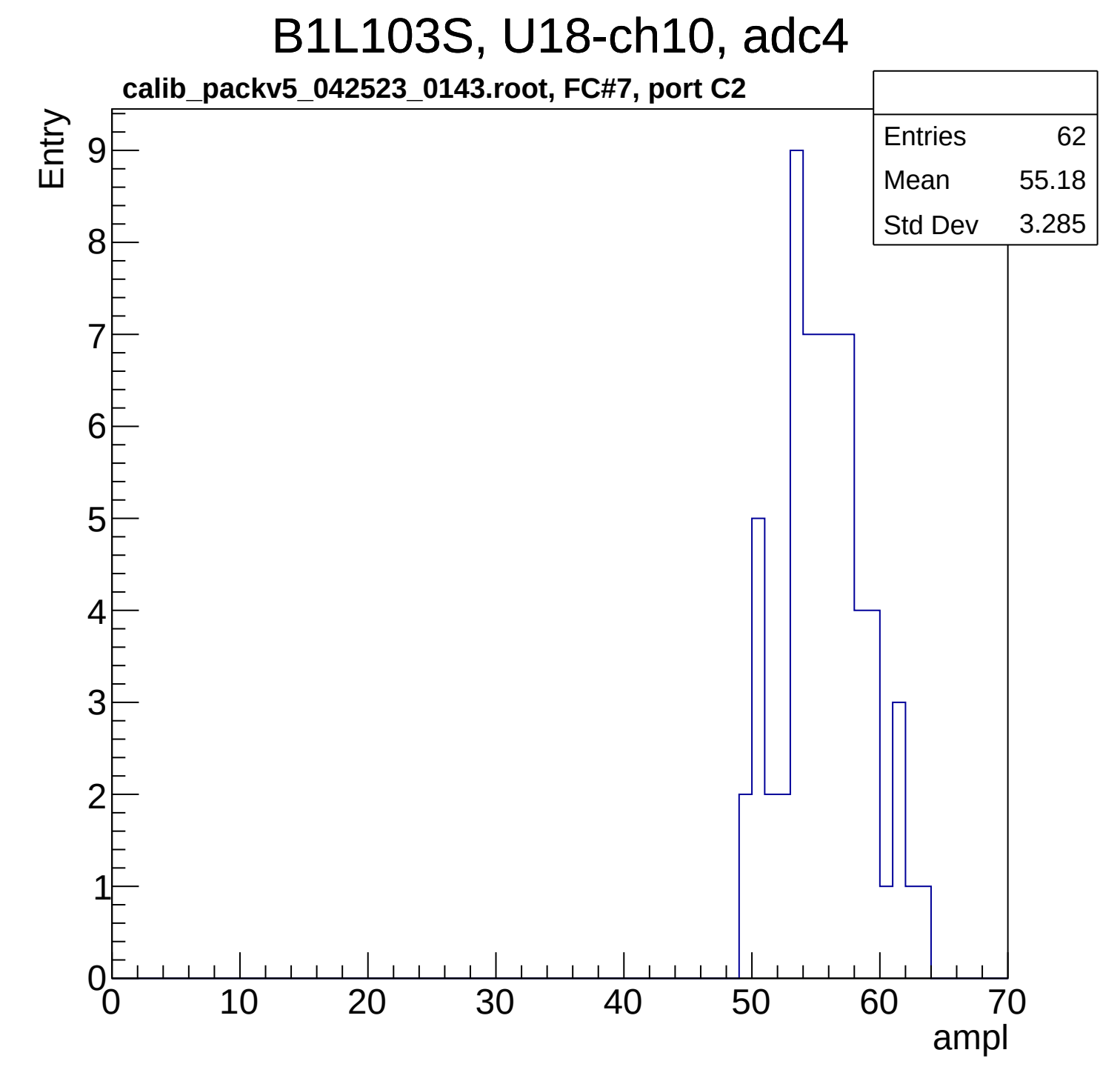
50
60
70
ampl


B1L103S, U18-ch10, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 62
Mean 55.18
Std Dev 3.285
Entry
ampl
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3
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7
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0
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60
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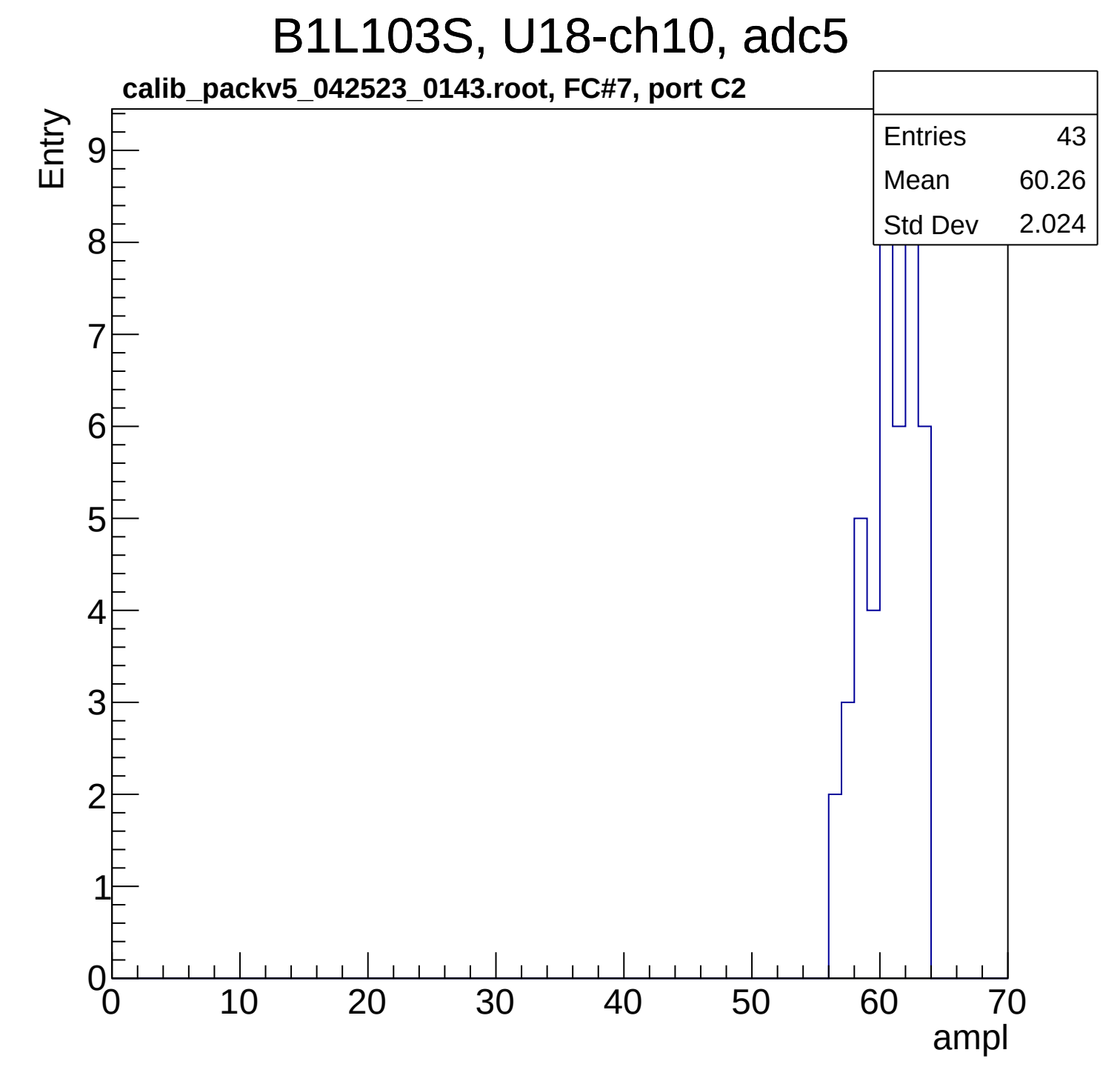
B1L103S, U18-ch10, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 43
Mean 60.26
Std Dev 2.024
Entry
ampl
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3
4
5
6
7
8
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0
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20
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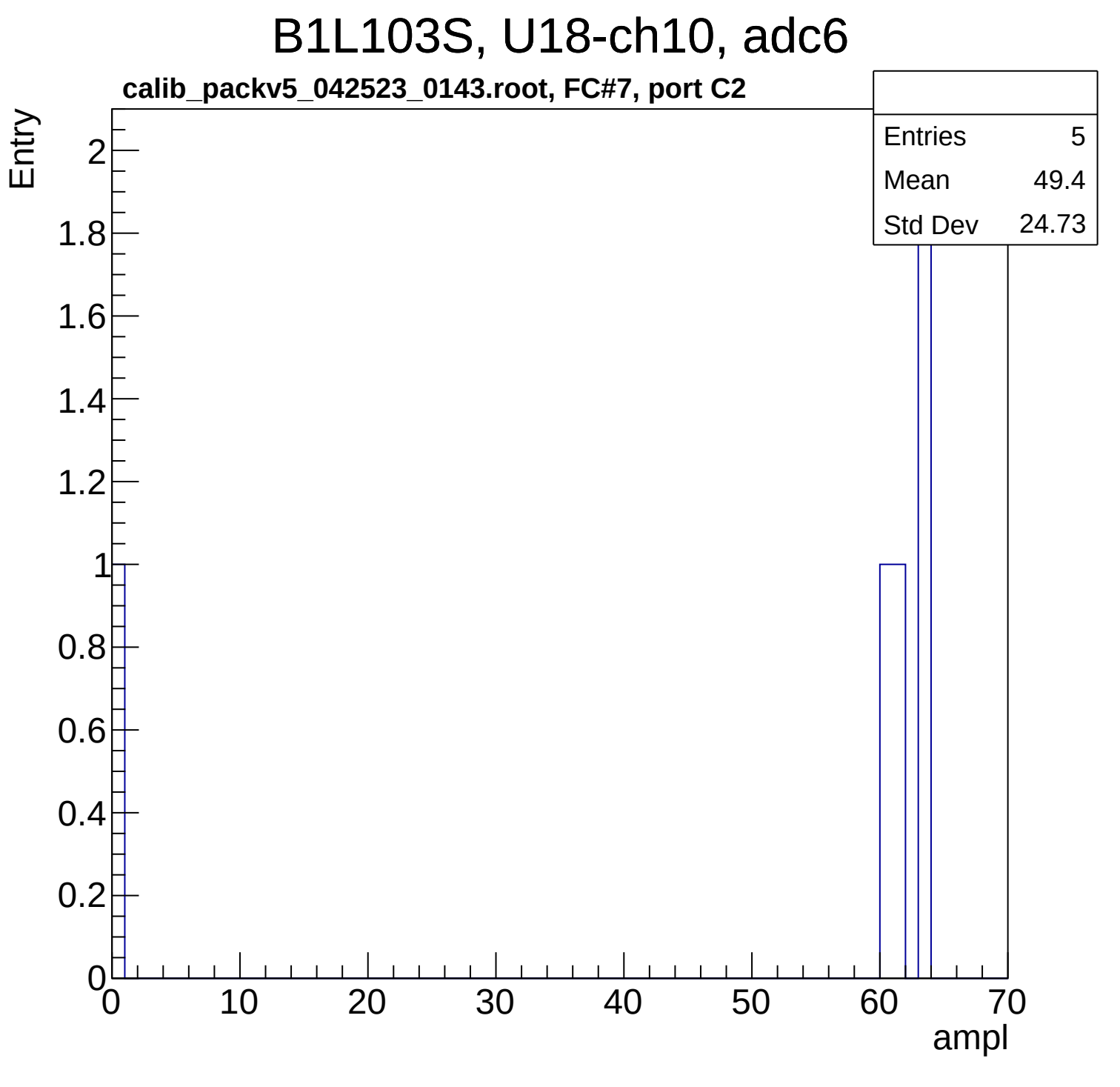
50
60
70


B1L103S, U18-ch10, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 5
Mean 49.4
Std Dev 24.73
Entry
ampl
0
0.2
0.4
0.6
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1.2
1.4
1.6
1.8
2
0
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20
30
40
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60
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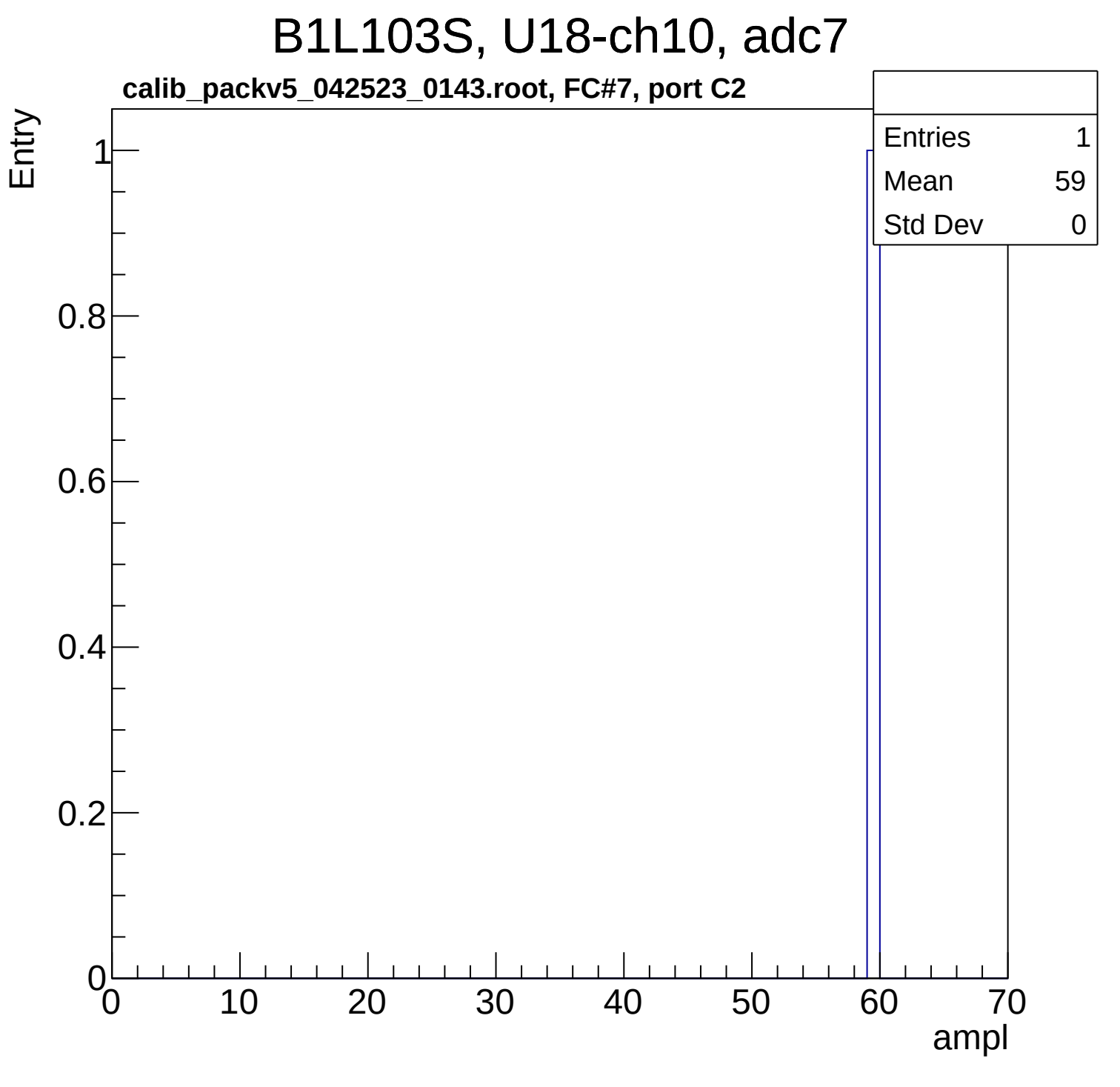
B1L103S, U18-ch10, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 59
Std Dev 0
Entry
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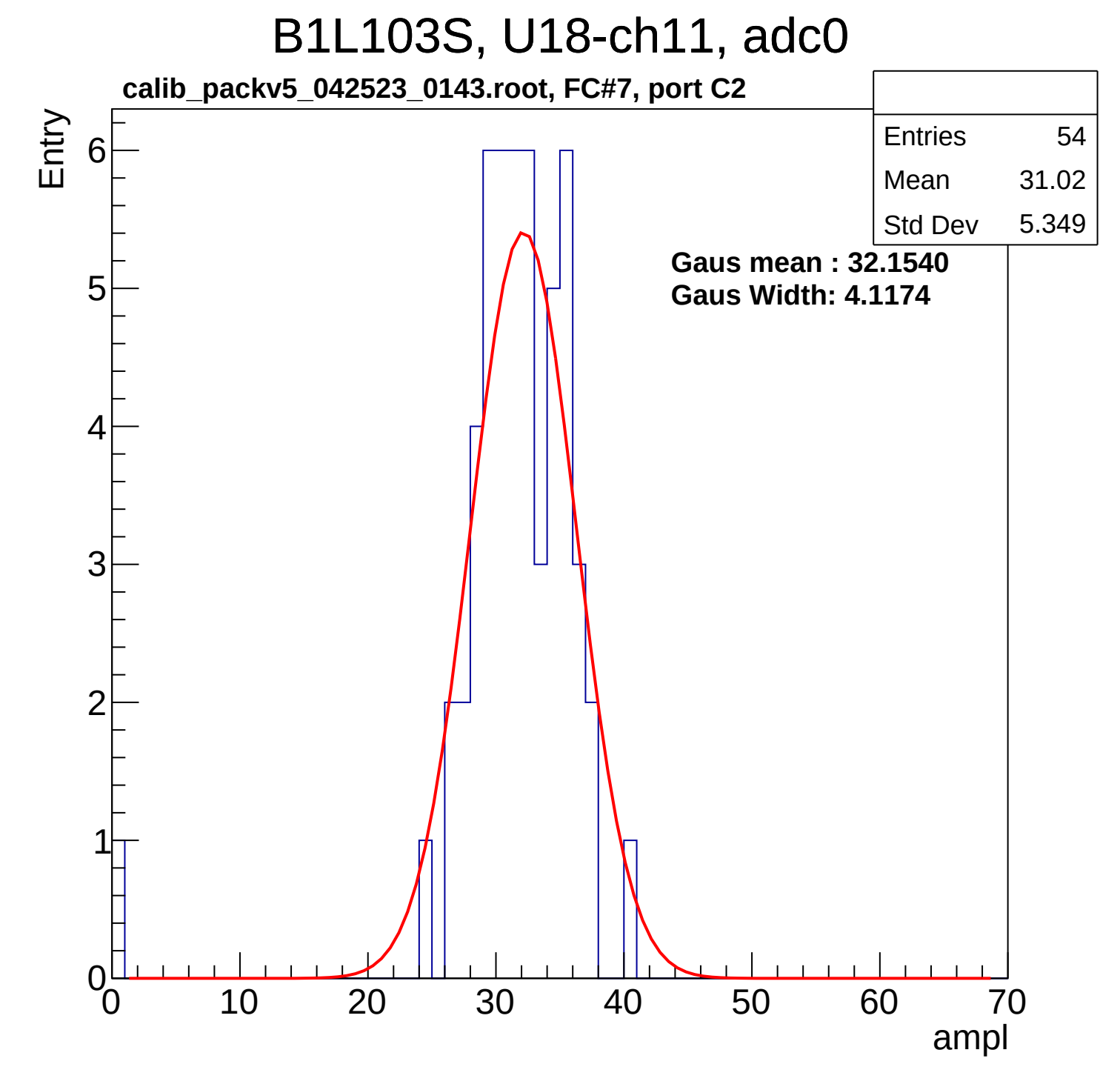
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch11, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 54
Mean 31.02
Std Dev 5.349
Gaus mean : 32.1540
Gaus Width: 4.1174
Entry
ampl
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3
4
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0
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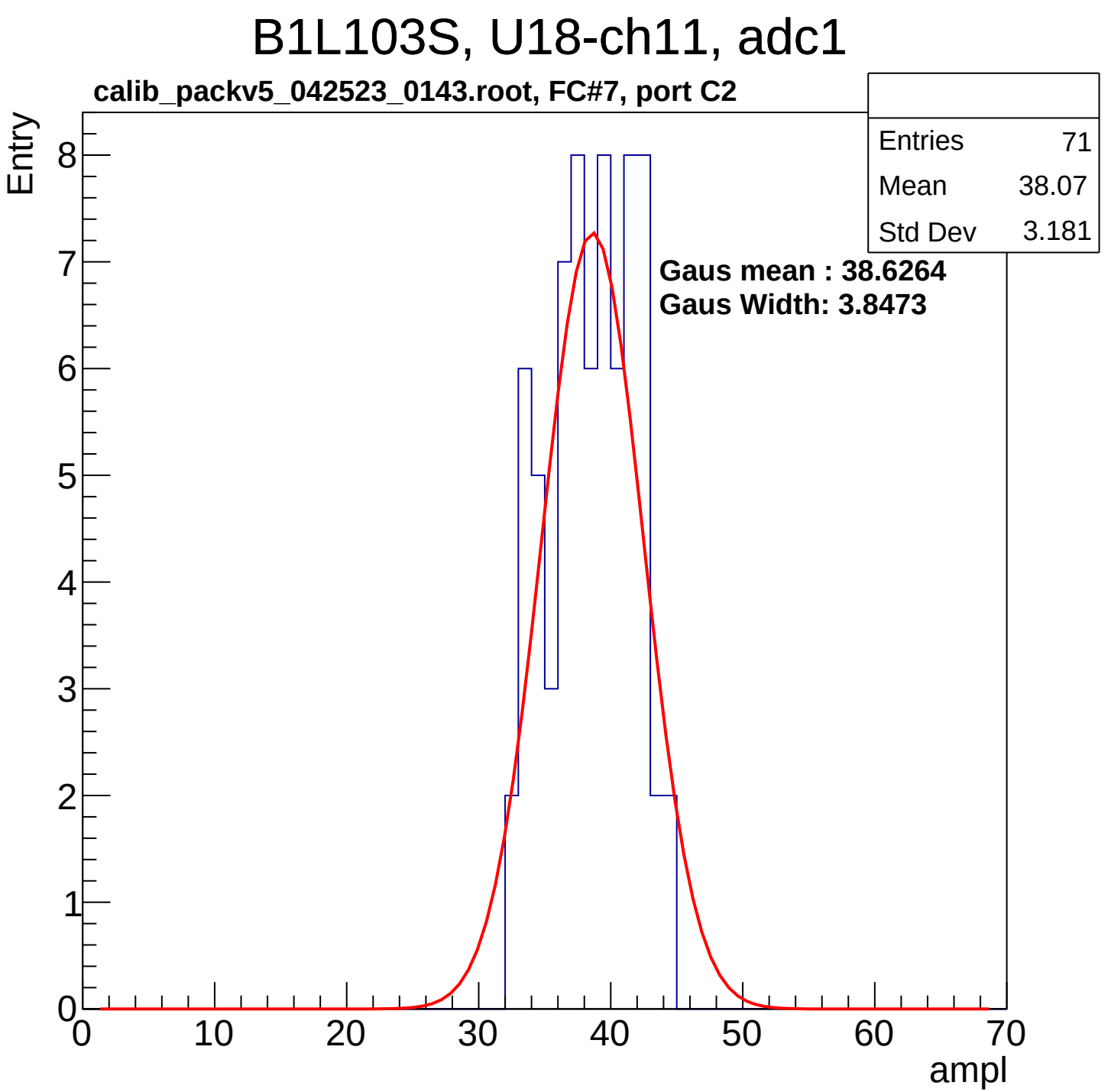
B1L103S, U18-ch11, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 71
Mean 38.07
Std Dev 3.181
Gaus mean : 38.6264
Gaus Width: 3.8473
Entry
ampl
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2
3
4
5
6
7
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0
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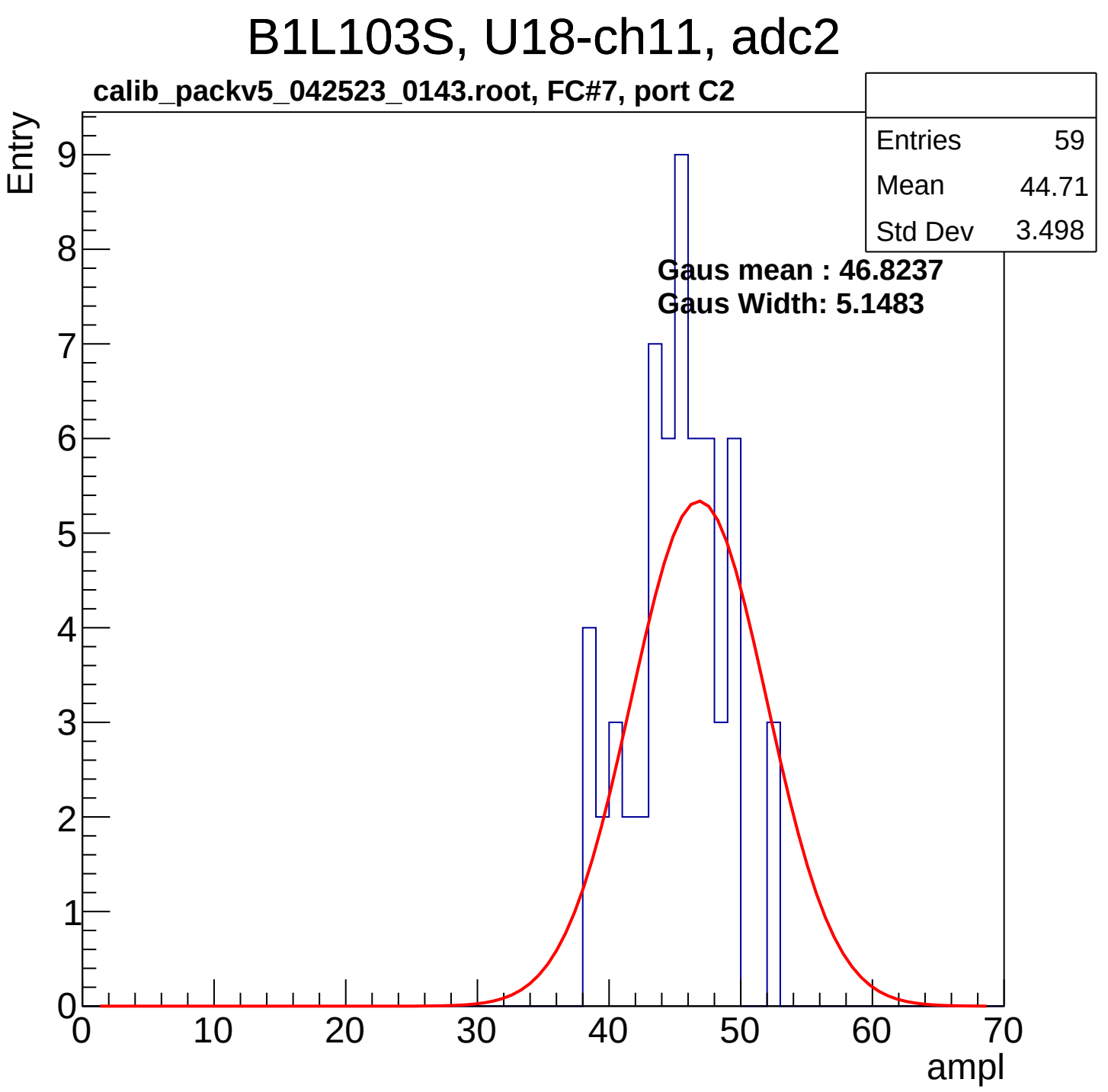
B1L103S, U18-ch11, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 44.71
Std Dev 3.498
Gaus mean : 46.8237
Gaus Width: 5.1483
Entry
ampl
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6
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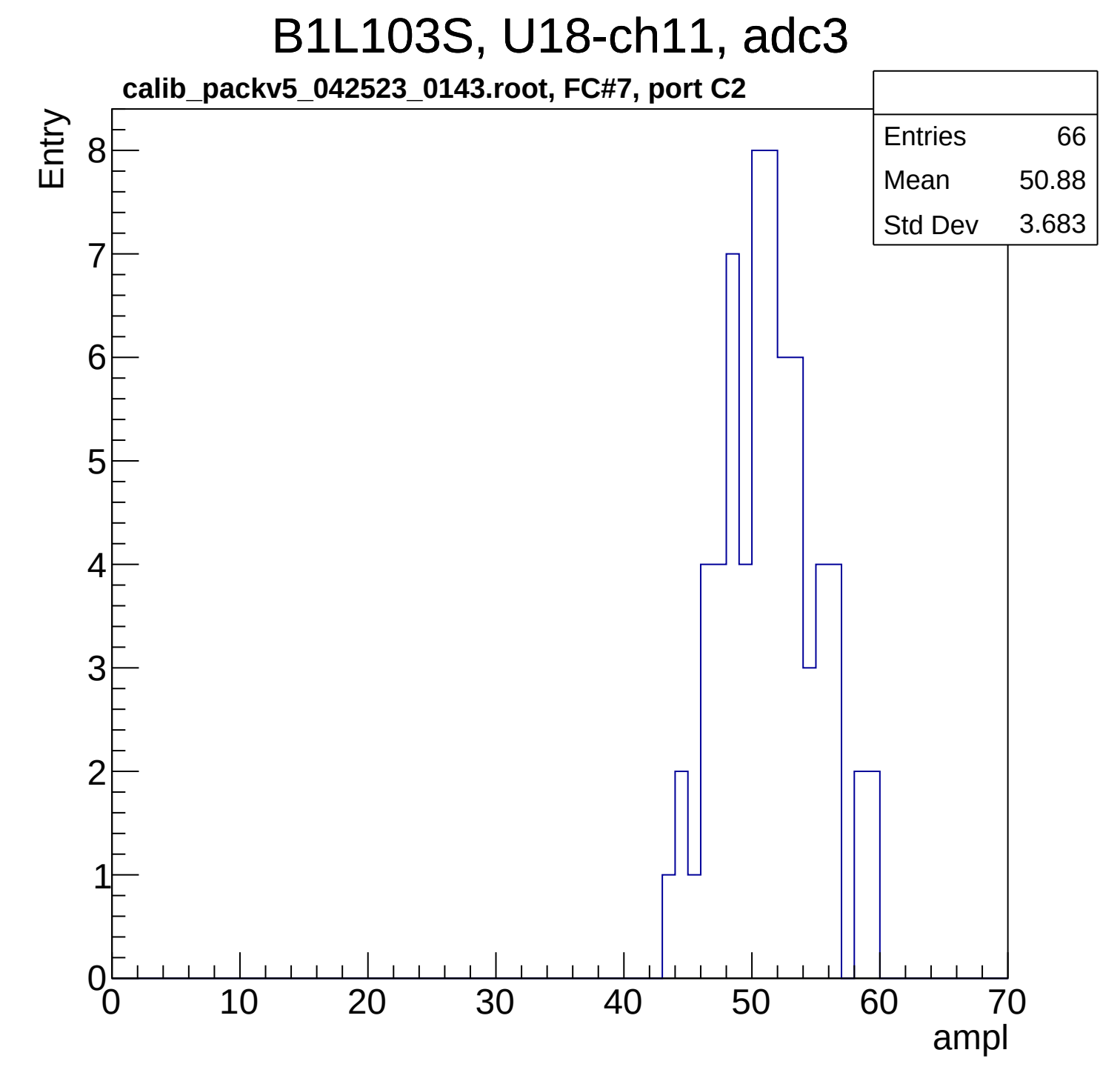
B1L103S, U18-ch11, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 50.88
Std Dev 3.683
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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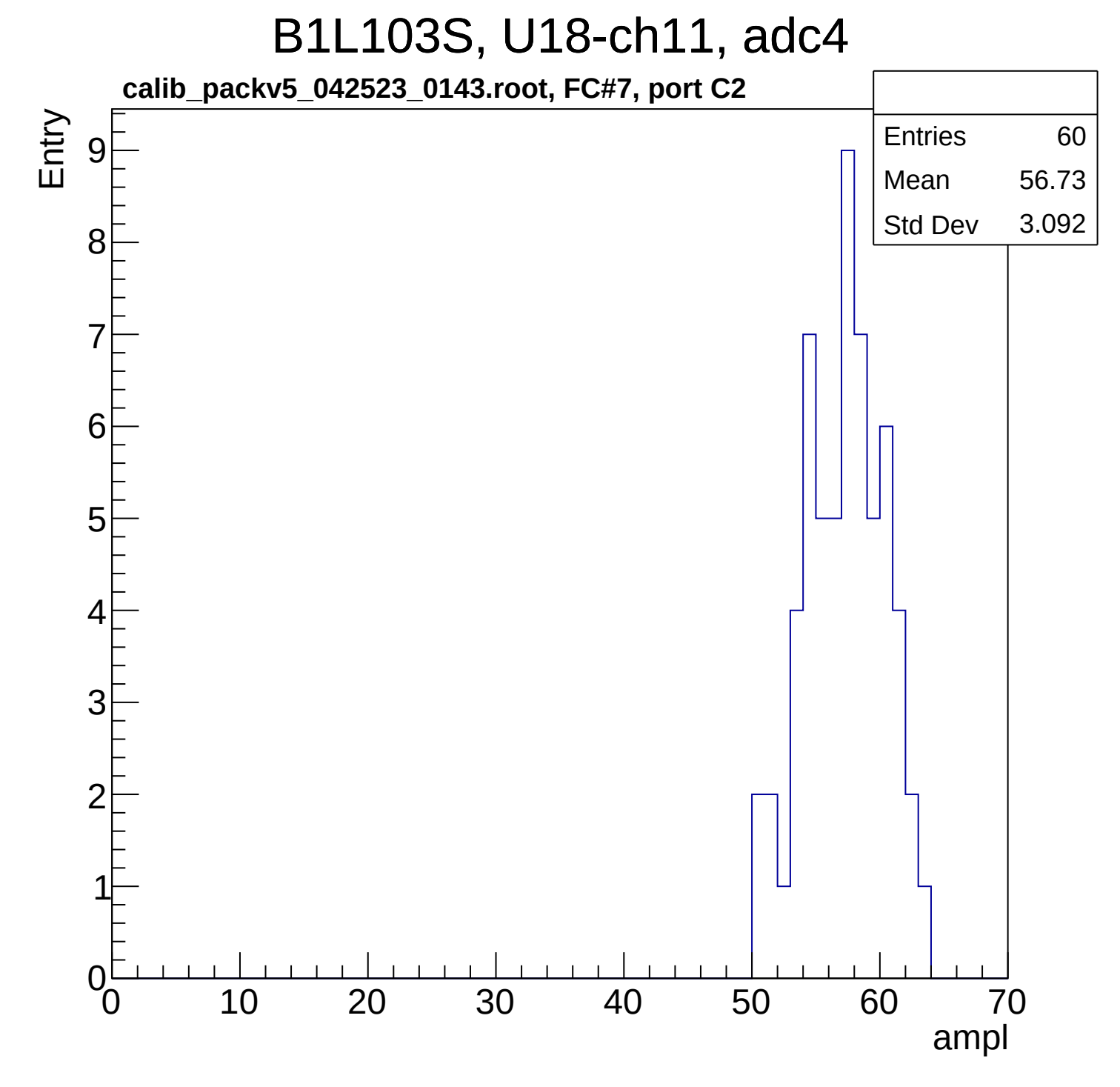
B1L103S, U18-ch11, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 60
Mean 56.73
Std Dev 3.092
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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20
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40
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60
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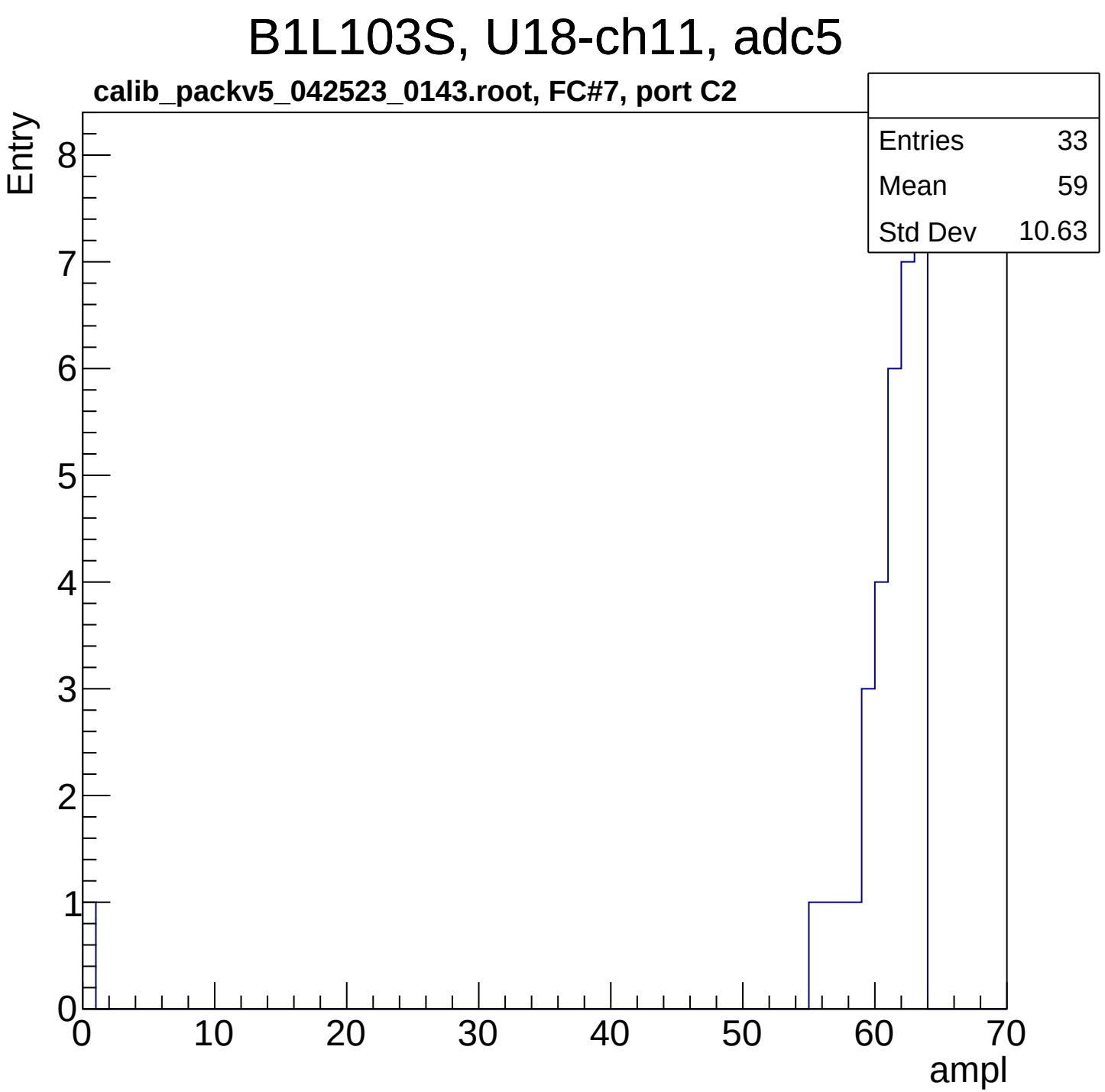
B1L103S, U18-ch11, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 33
Mean 59
Std Dev 10.63
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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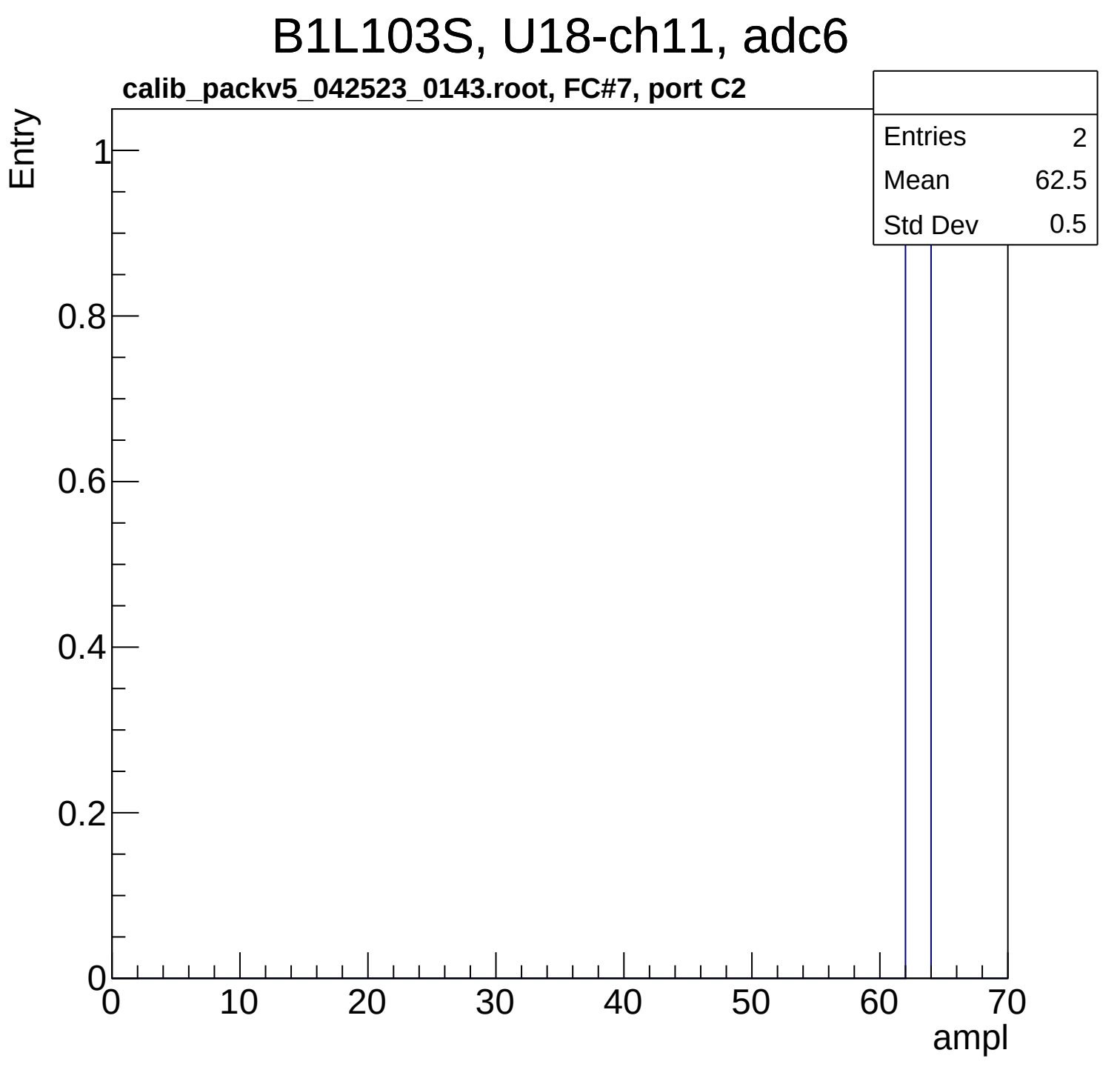
B1L103S, U18-ch11, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
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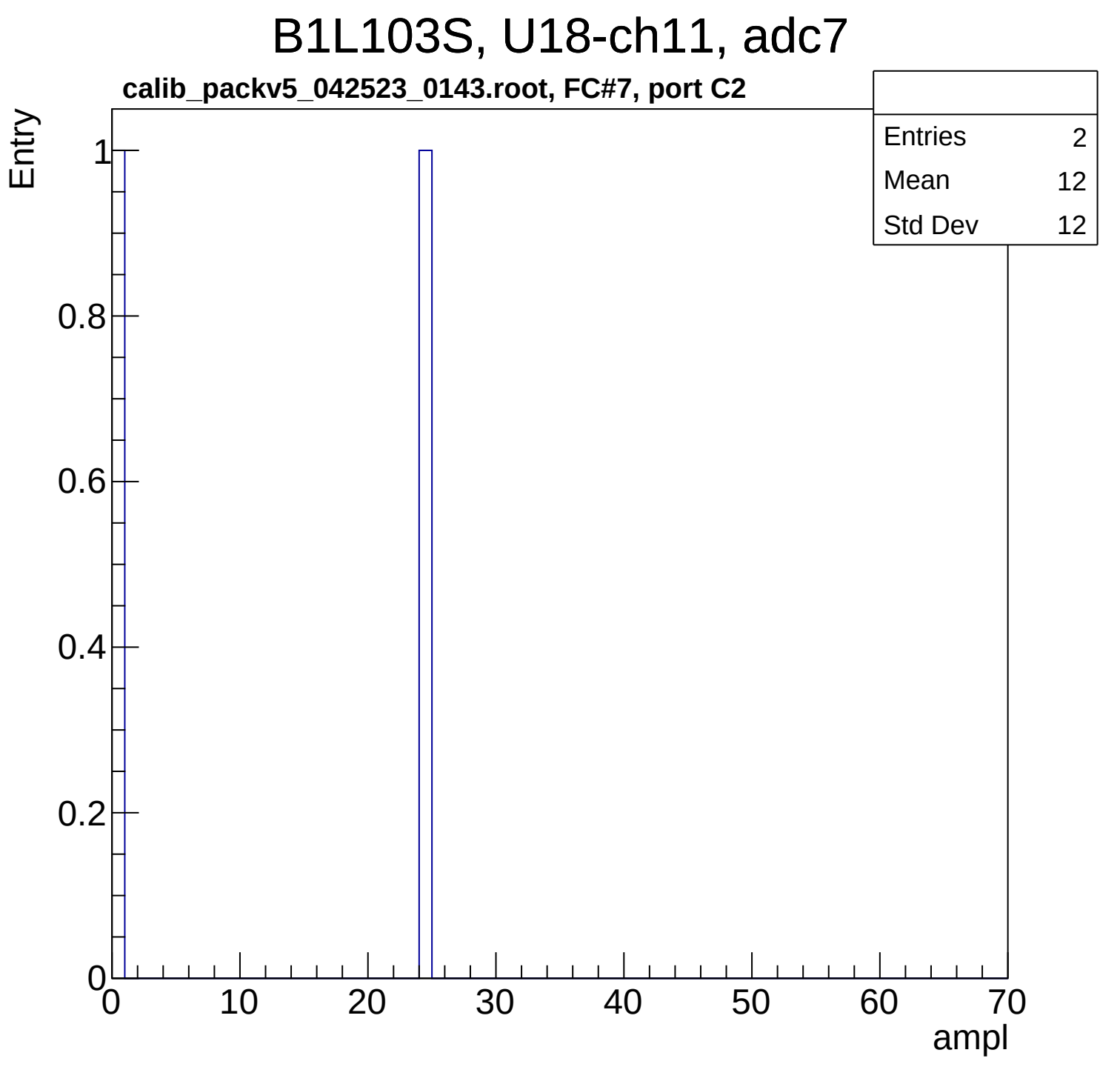
40
50
60
70
ampl


B1L103S, U18-ch11, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 12
Std Dev 12
Entry
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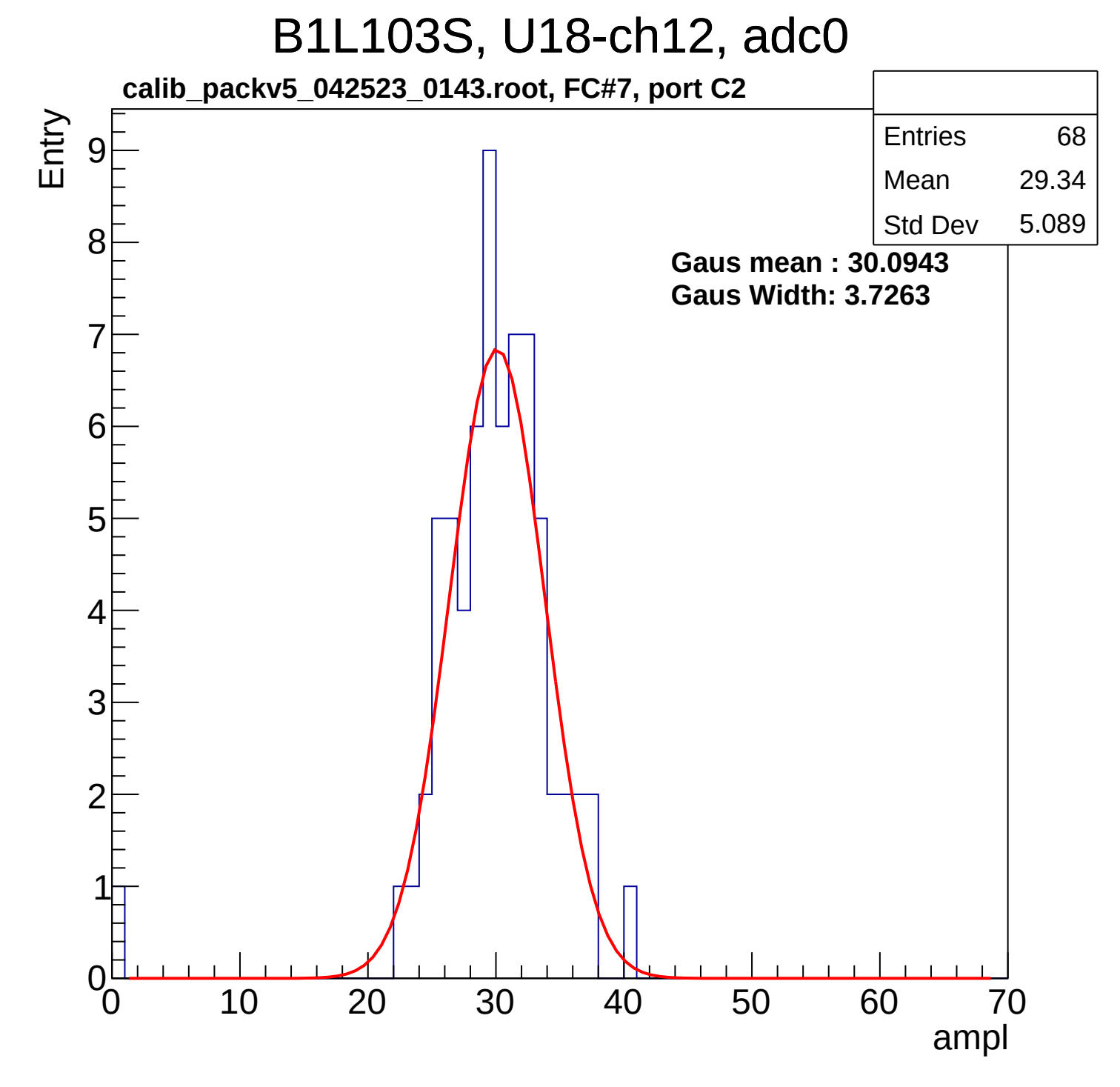
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch12, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 29.34
Std Dev 5.089
Gaus mean : 30.0943
Gaus Width: 3.7263
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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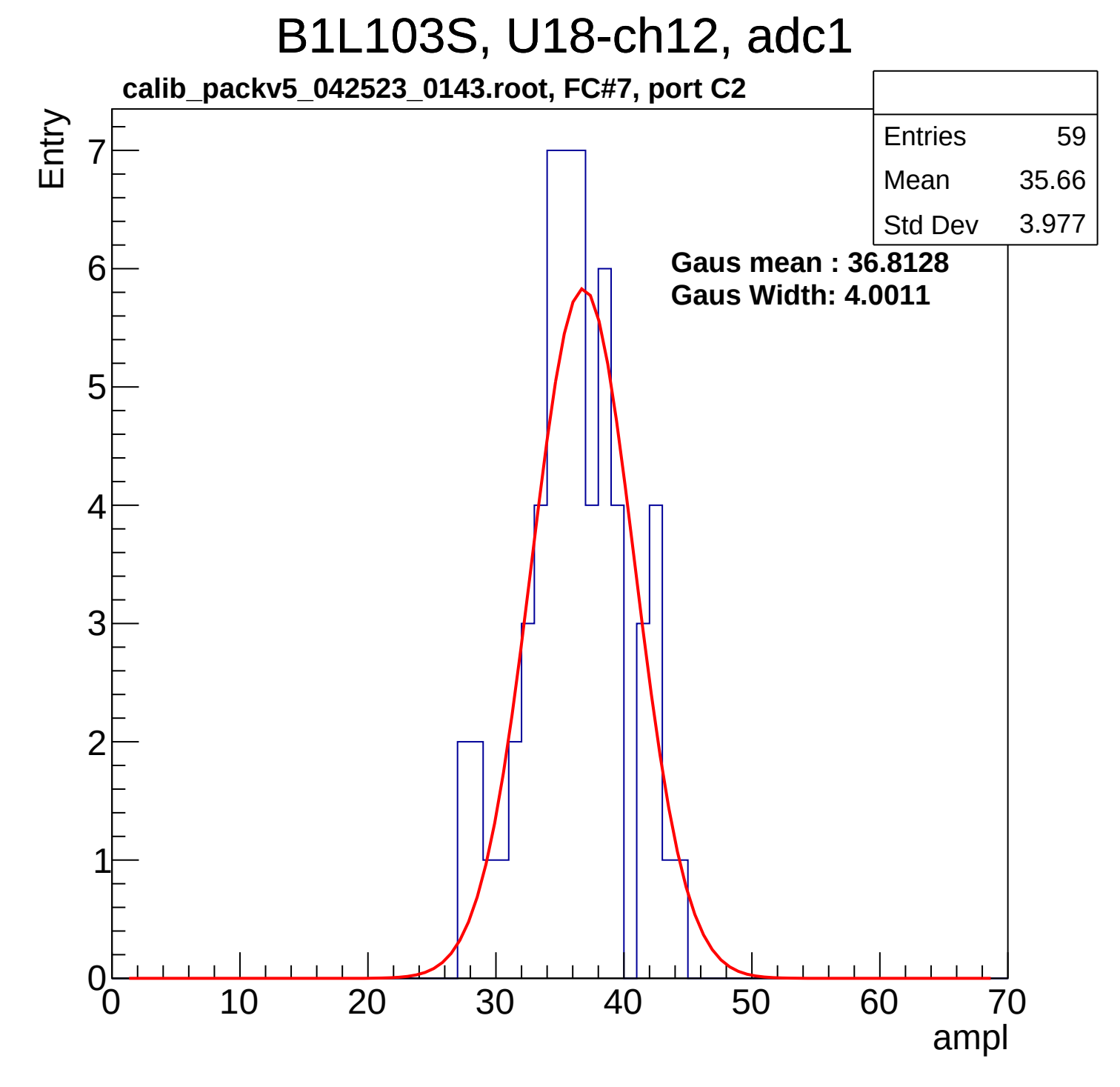
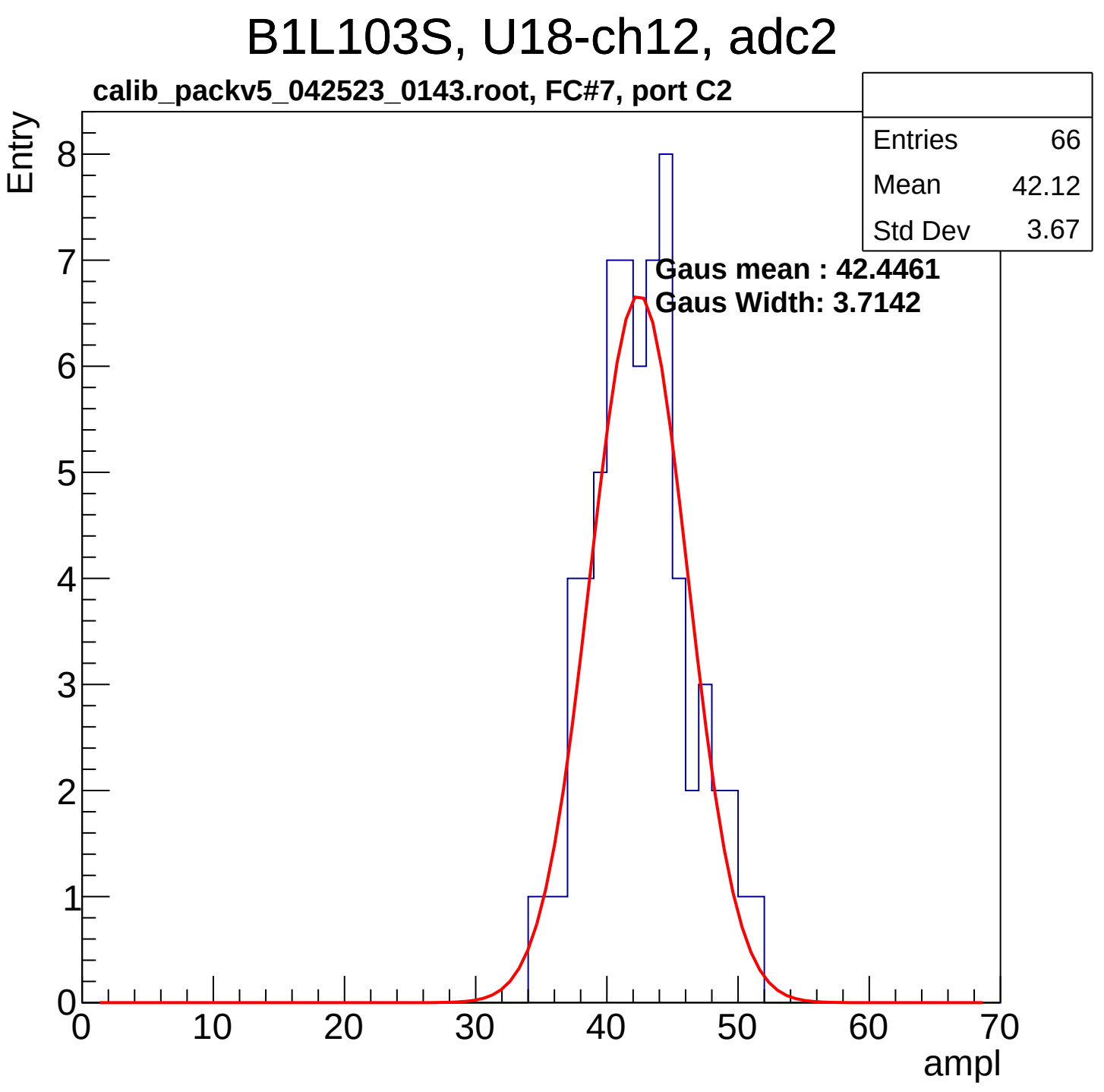

B1L103S, U18-ch12, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 35.66
Std Dev 3.977
Gaus mean : 36.8128
Gaus Width: 4.0011
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch12, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 42.12
Std Dev 3.67
Gaus mean : 42.4461
Gaus Width: 3.7142
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
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60
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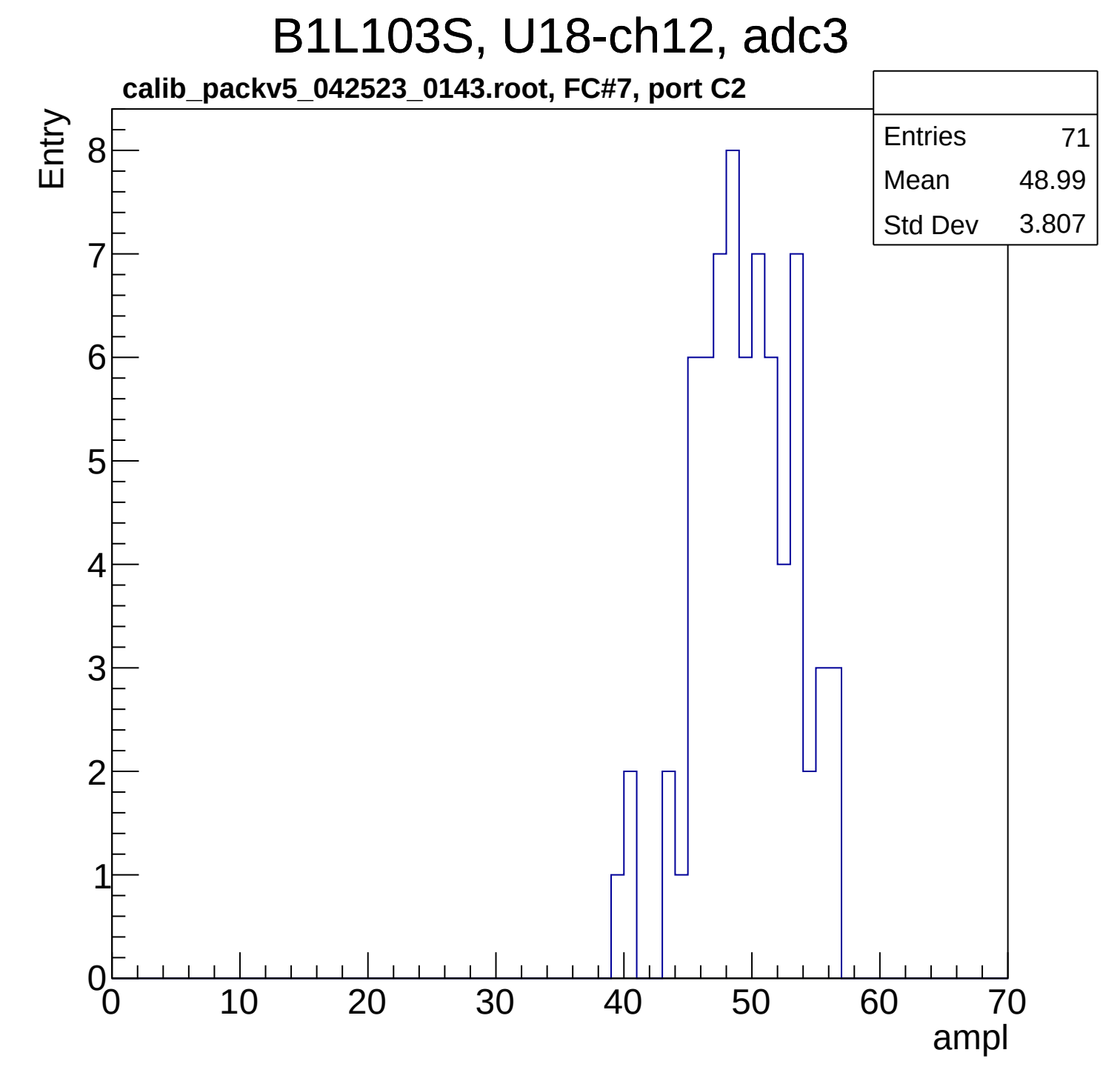
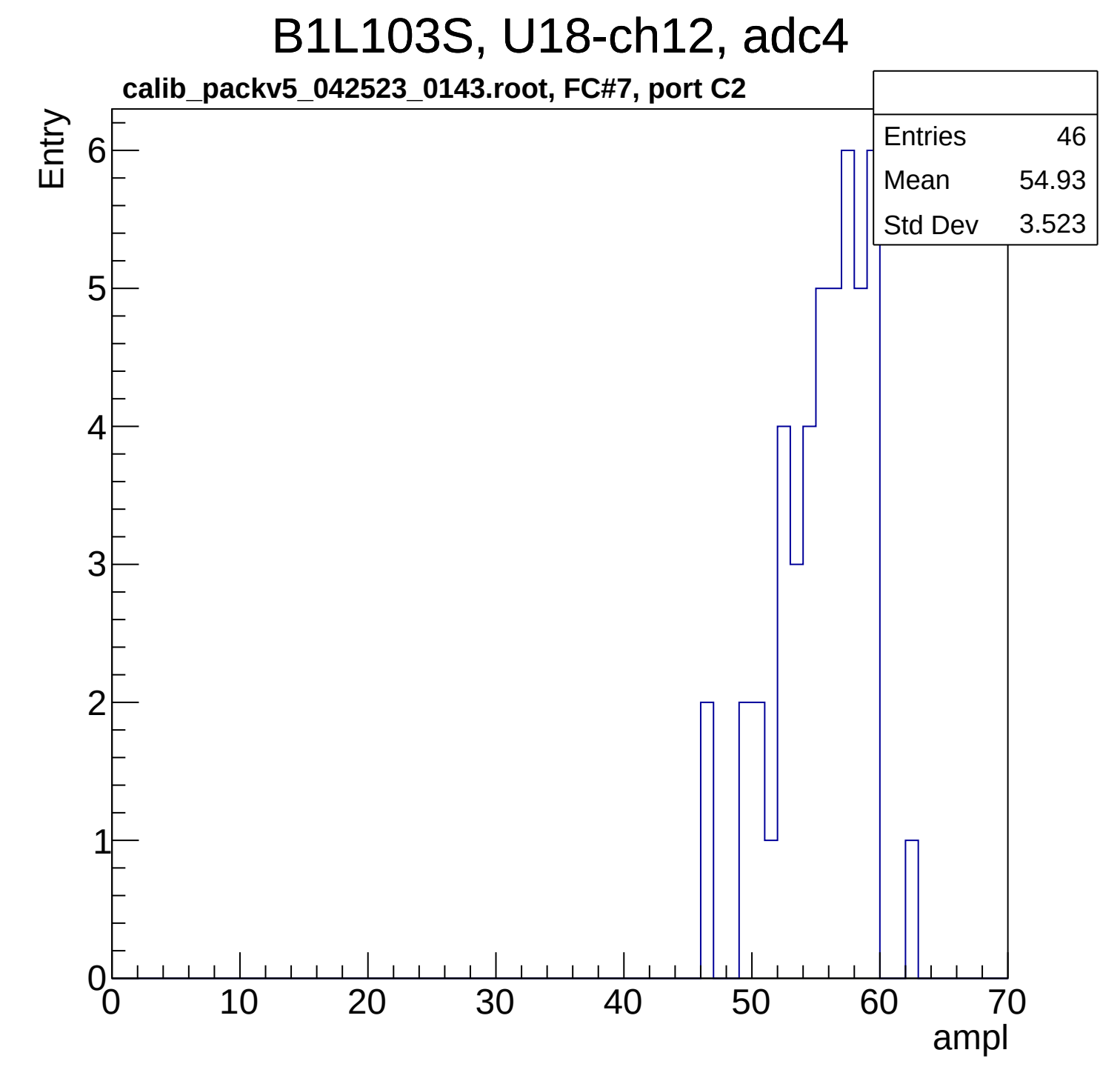
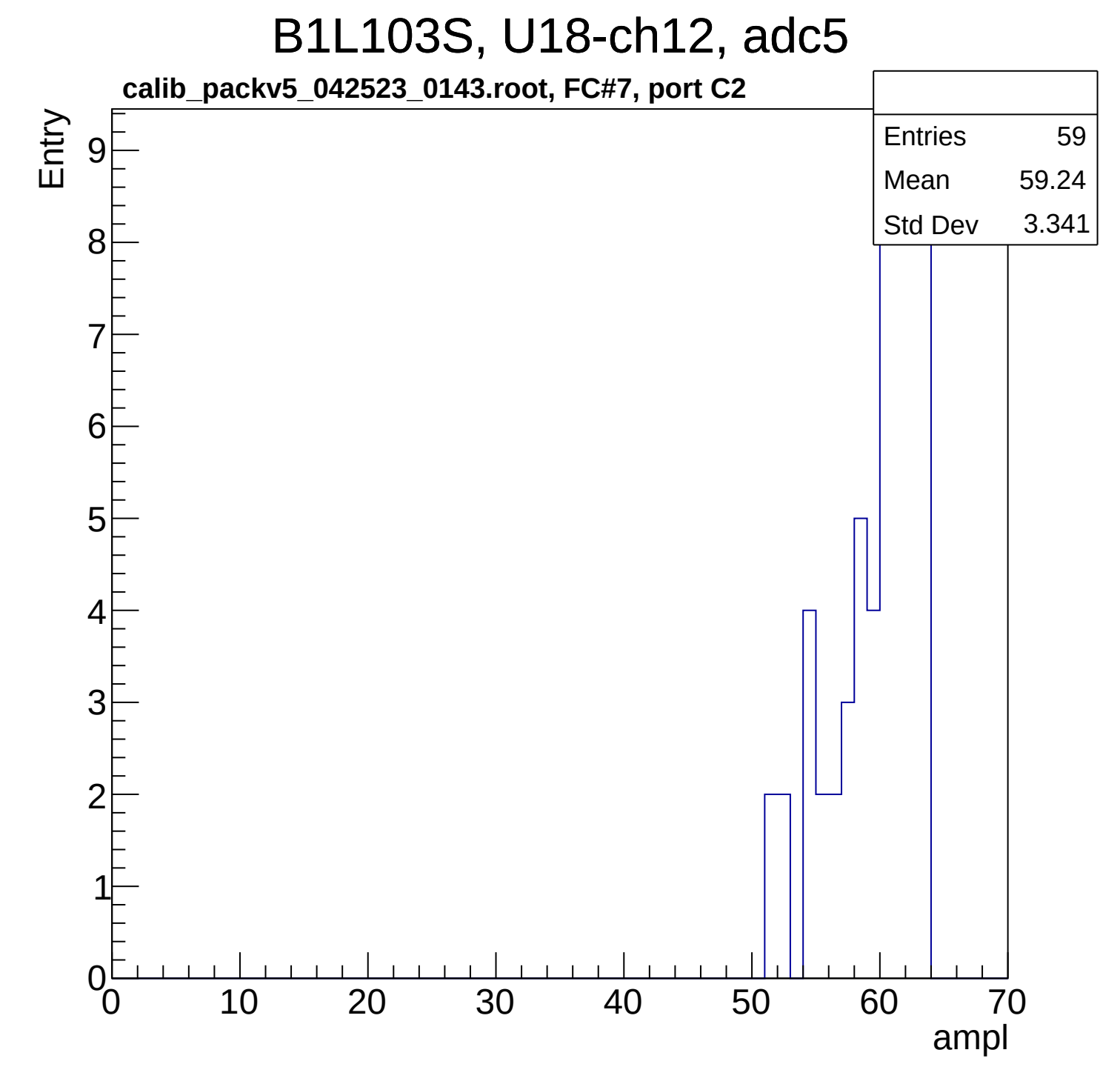

B1L103S, U18-ch12, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 71
Mean 48.99
Std Dev 3.807
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch12, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 46
Mean 54.93
Std Dev 3.523
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U18-ch12, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 59.24
Std Dev 3.341
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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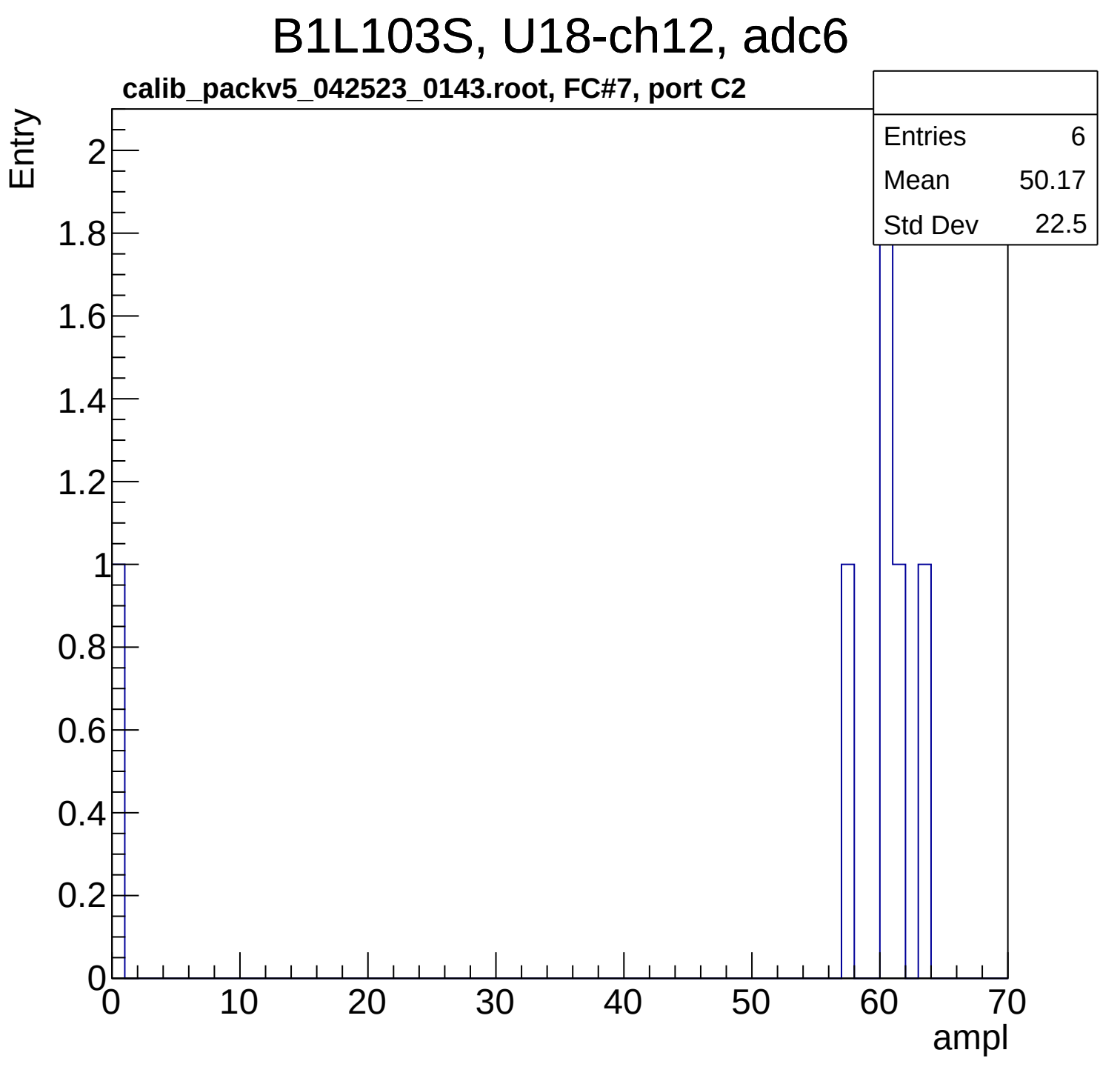
B1L103S, U18-ch12, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 6
Mean 50.17
Std Dev 22.5
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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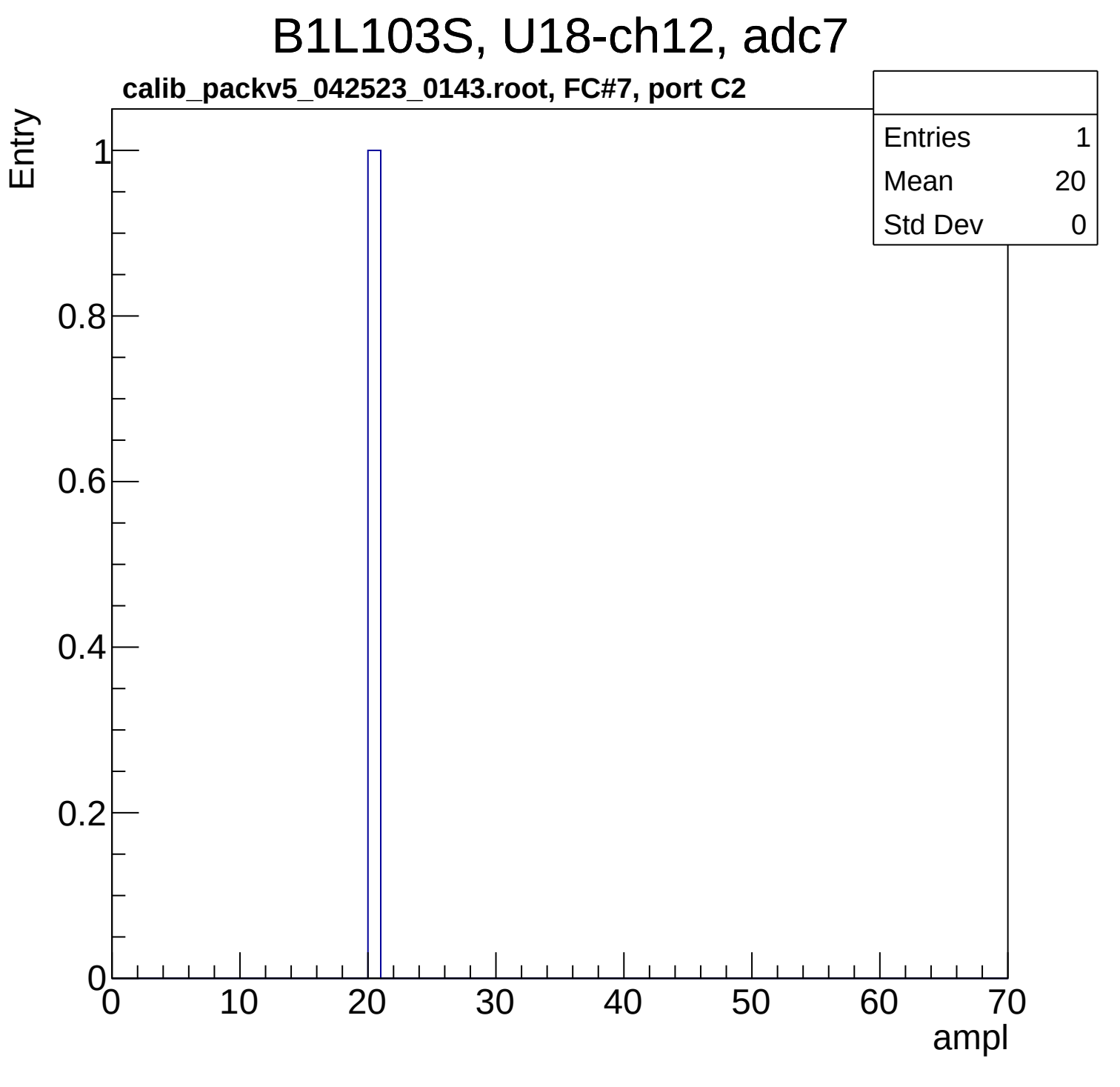
B1L103S, U18-ch12, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 20
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
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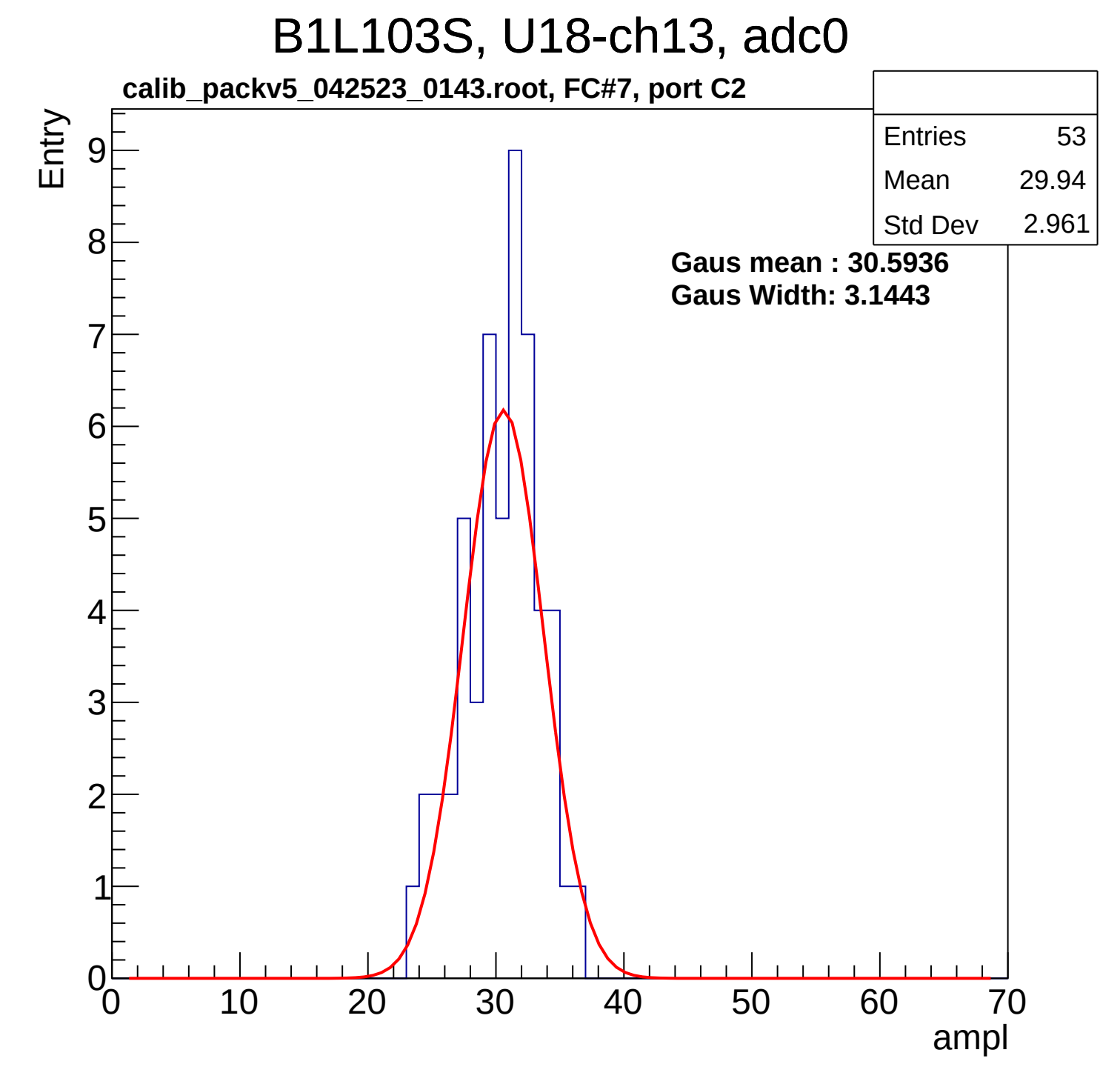
B1L103S, U18-ch13, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 29.94
Std Dev 2.961
Gaus mean : 30.5936
Gaus Width: 3.1443
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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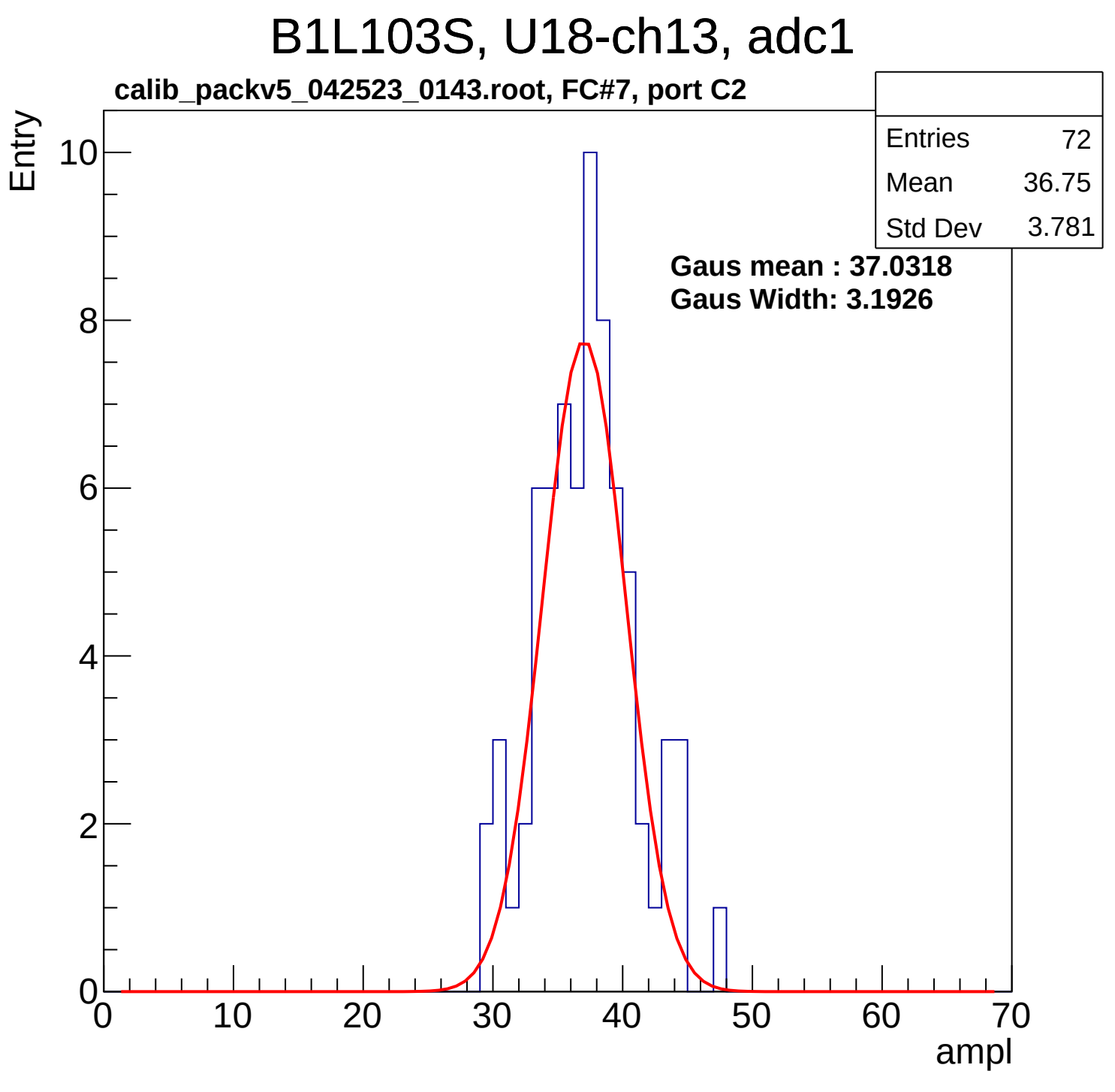
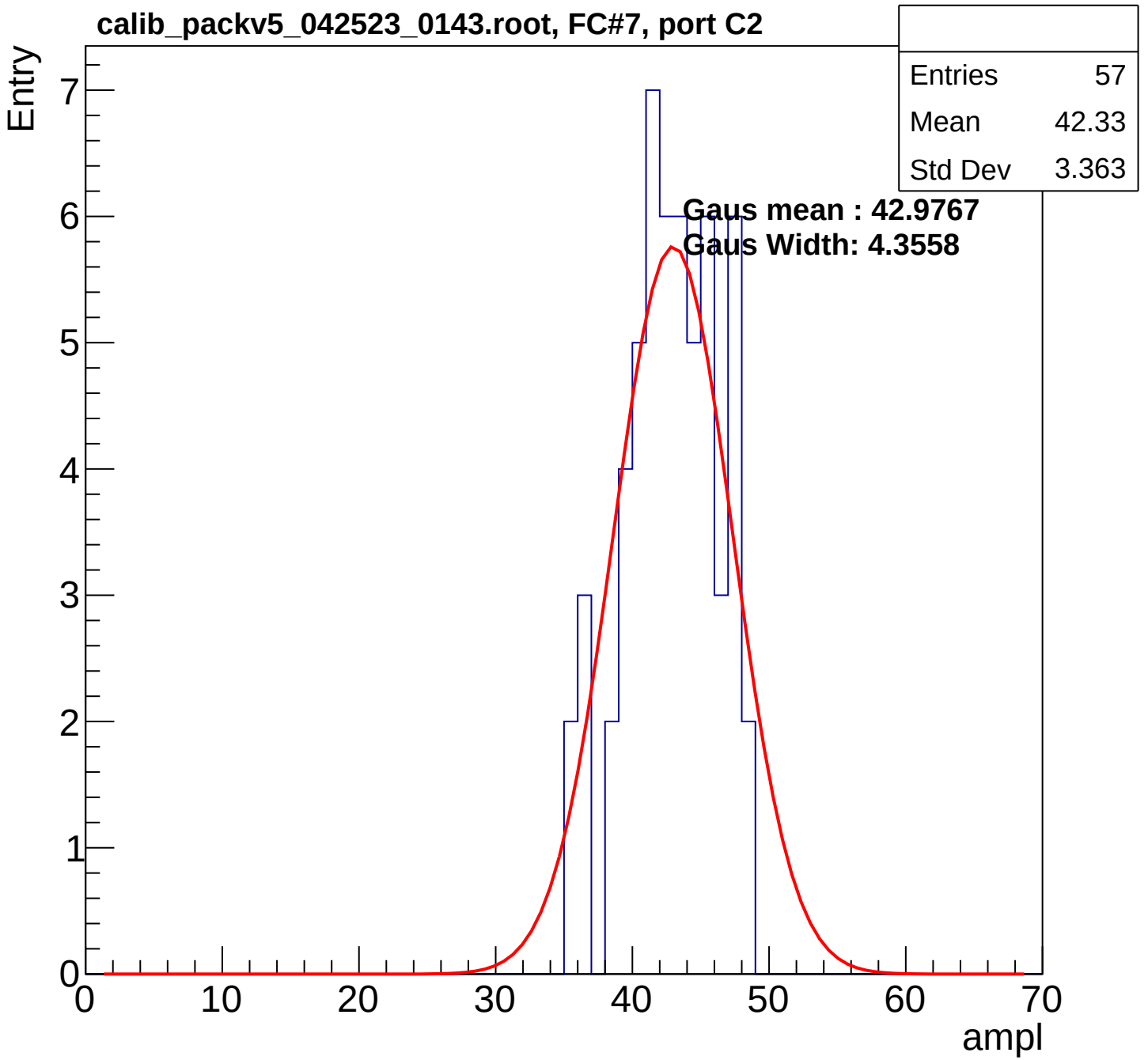

B1L103S, U18-ch13, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 72
Mean 36.75
Std Dev 3.781
Gaus mean : 37.0318
Gaus Width: 3.1926
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch13, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 42.33
Std Dev 3.363
Gaus mean : 42.9767
Gaus Width: 4.3558
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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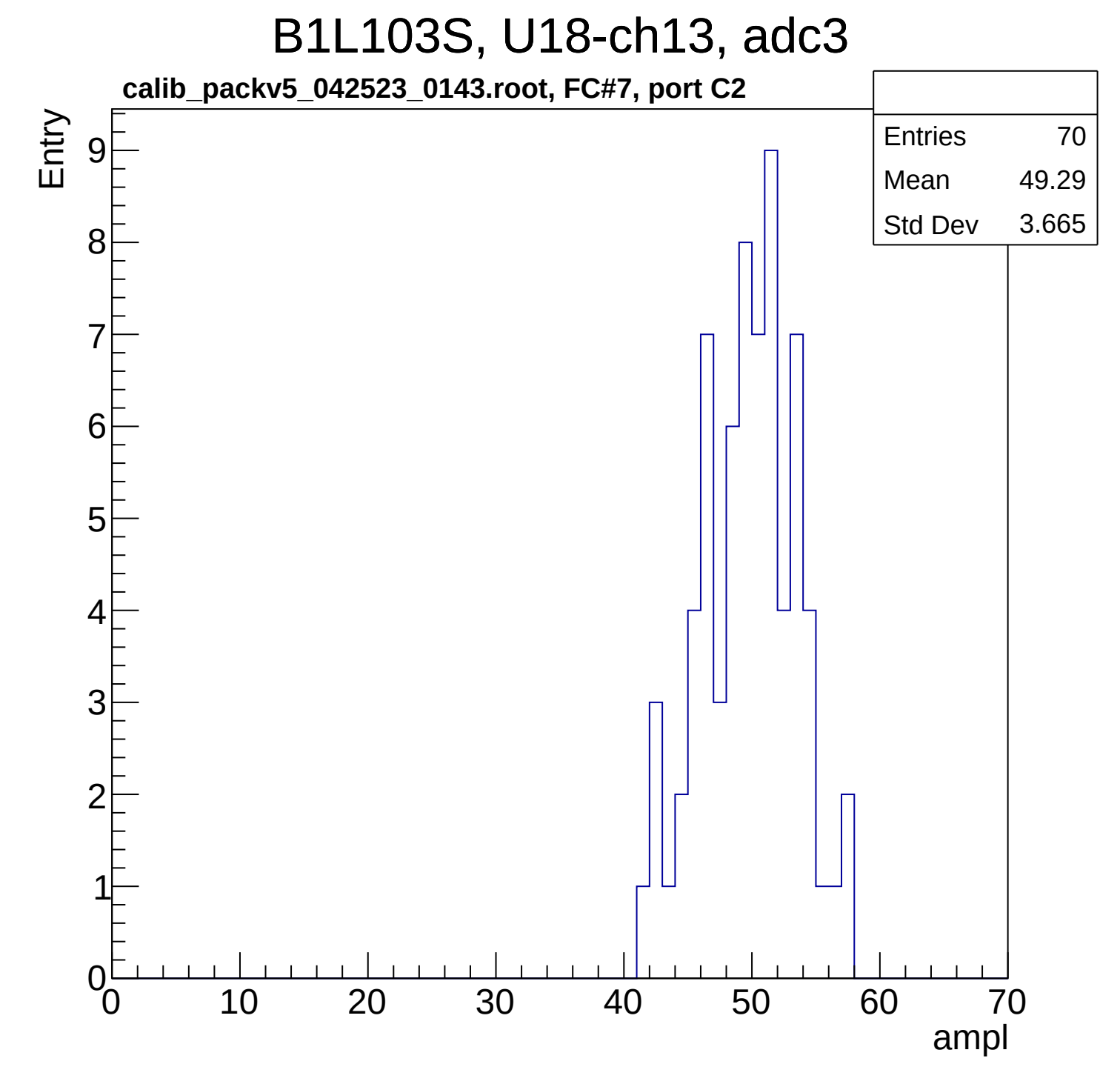
B1L103S, U18-ch13, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 49.29
Std Dev 3.665
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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60
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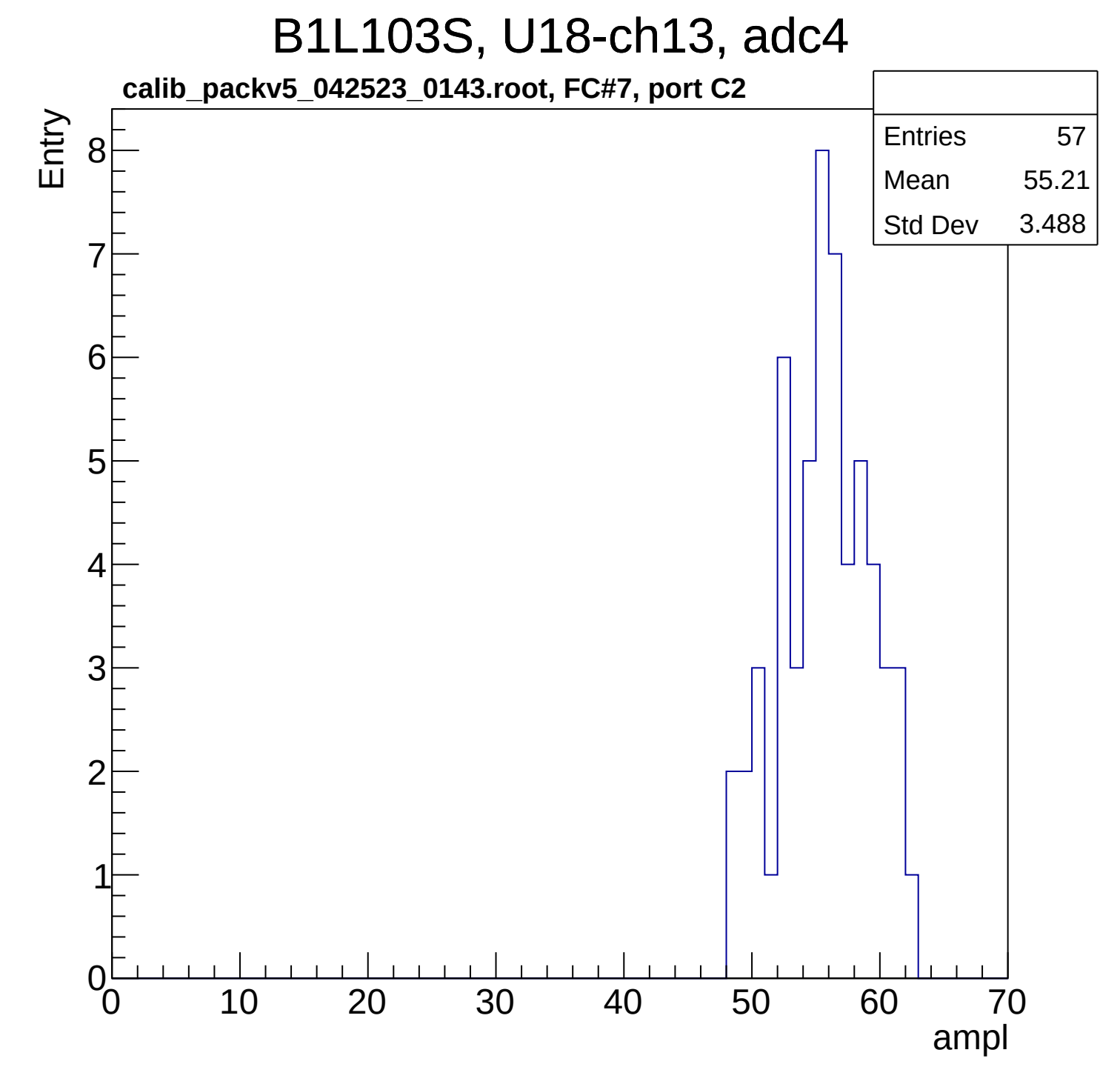
B1L103S, U18-ch13, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 55.21
Std Dev 3.488
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
50
60
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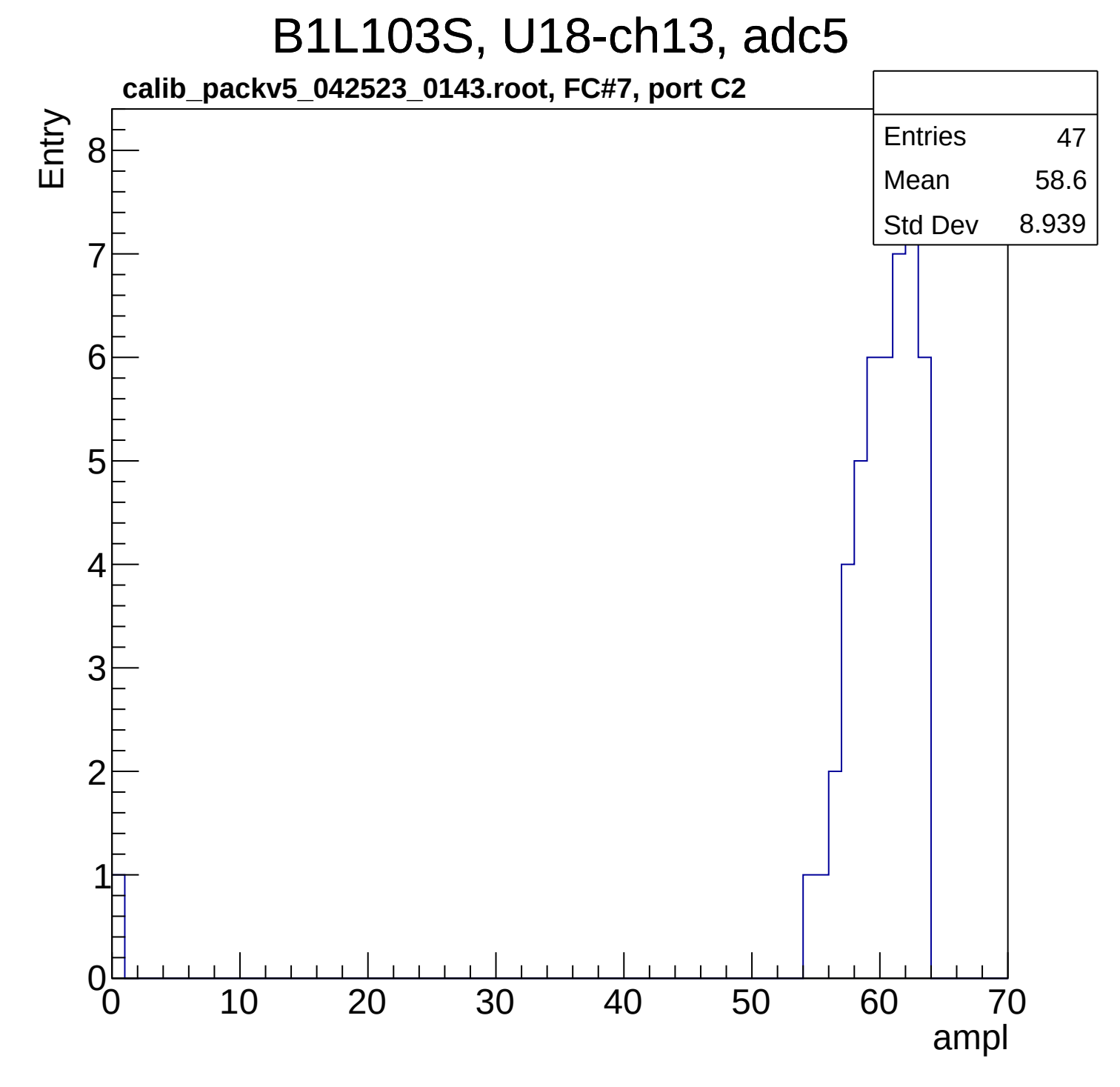
B1L103S, U18-ch13, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 47
Mean 58.6
Std Dev 8.939
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
30
40
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60
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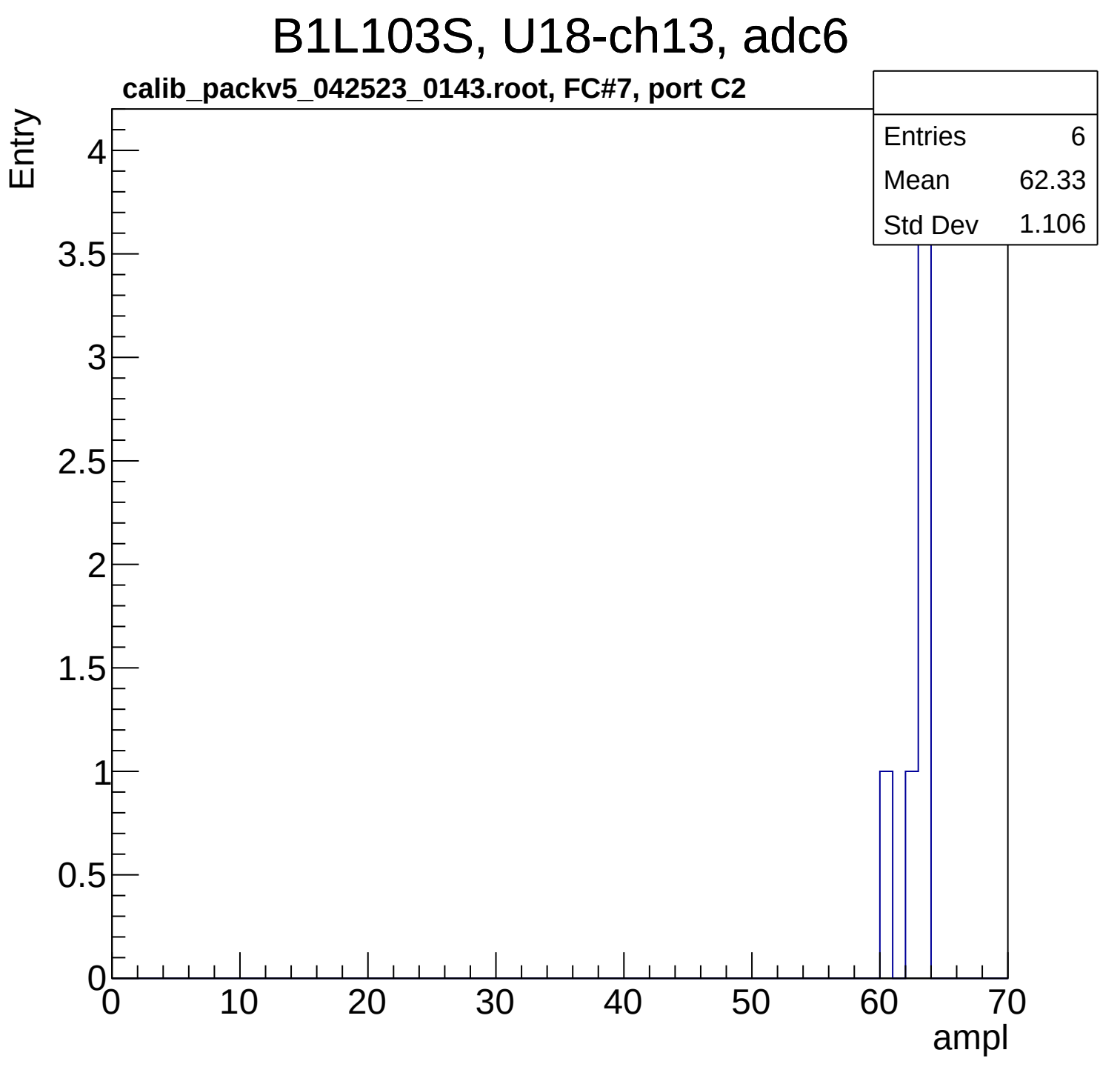
B1L103S, U18-ch13, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 6
Mean 62.33
Std Dev 1.106
Entry
ampl
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1
1.5
2
2.5
3
3.5
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0
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60
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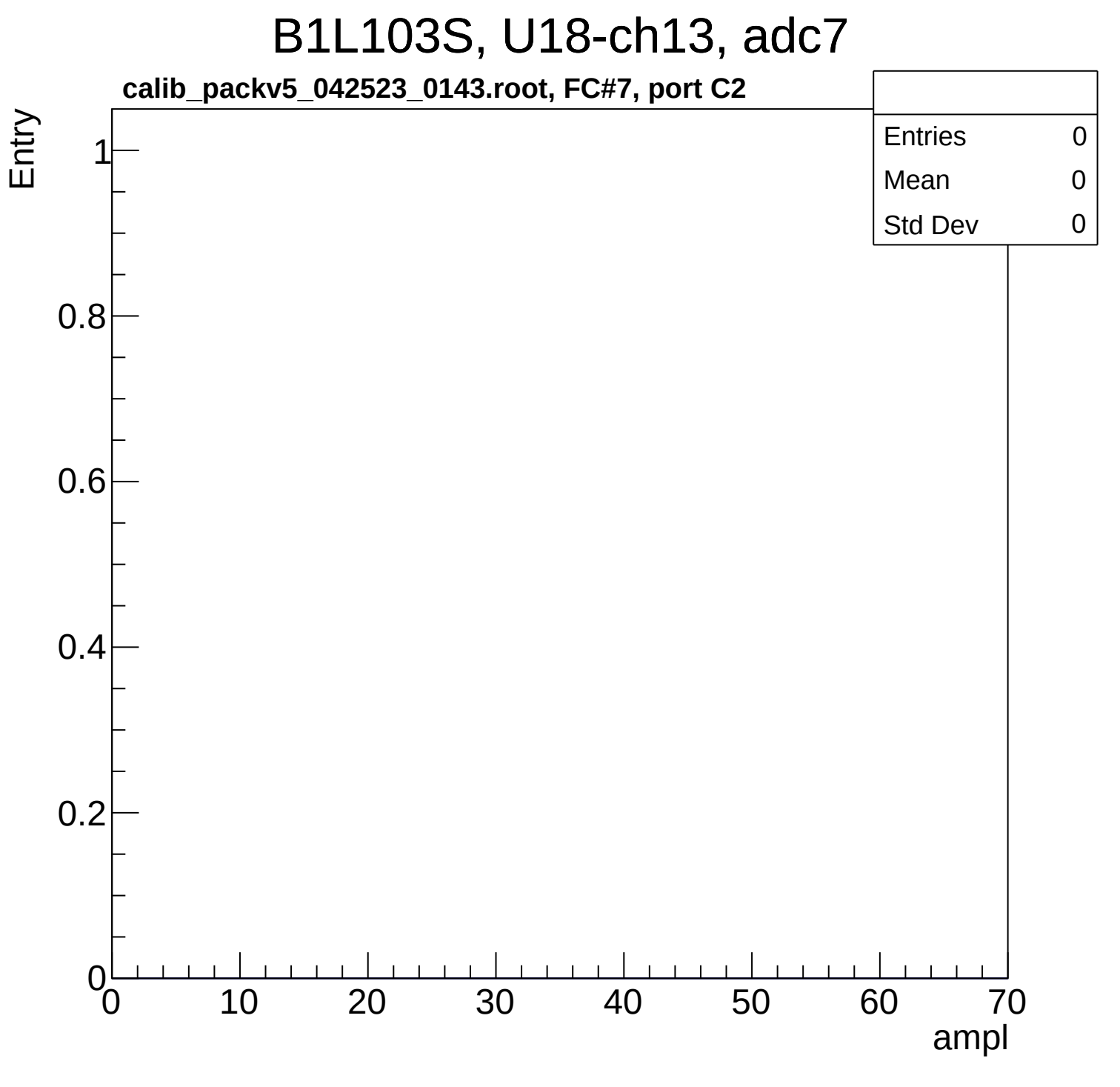
B1L103S, U18-ch13, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
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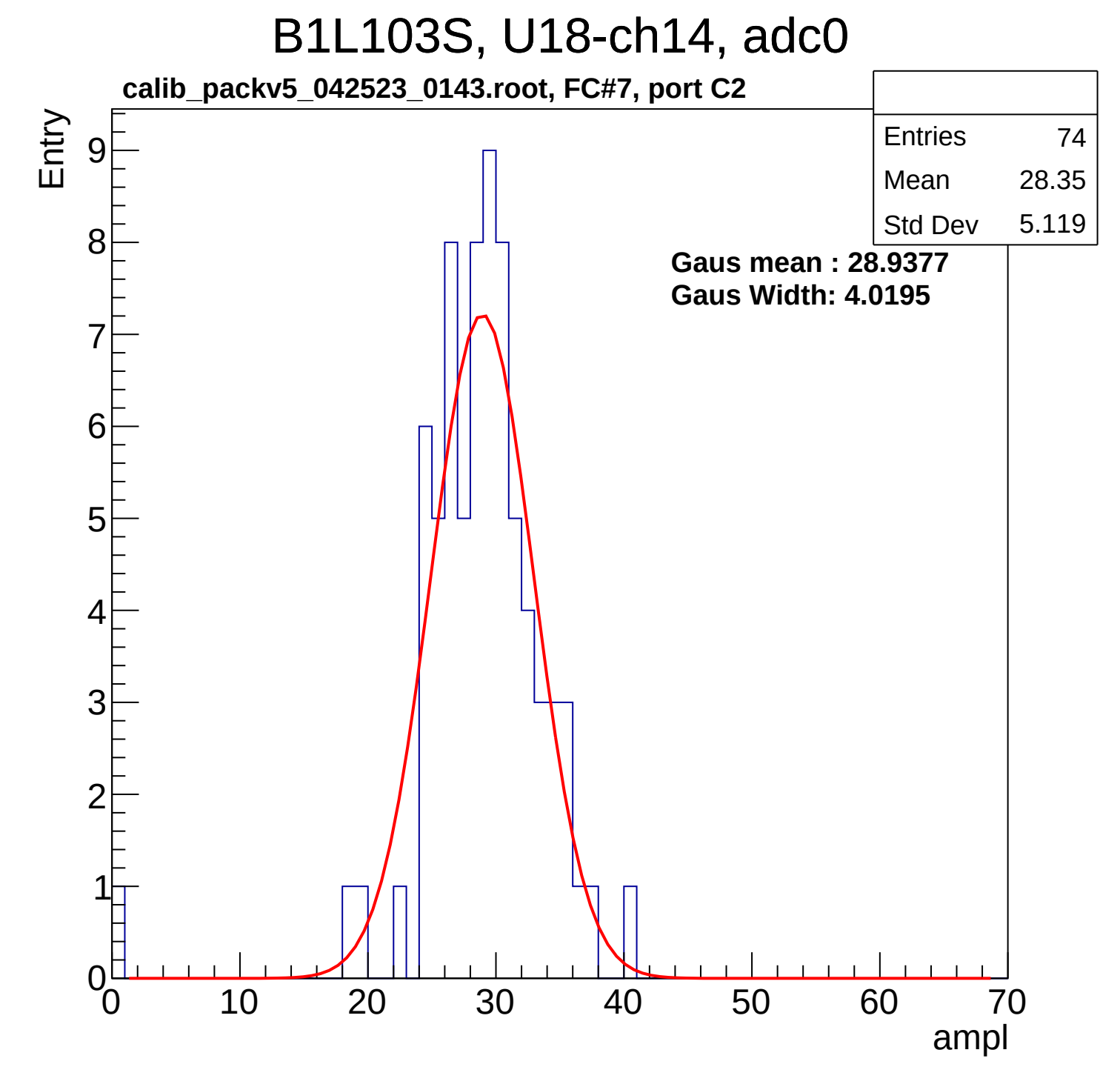
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch14, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 74
Mean 28.35
Std Dev 5.119
Gaus mean : 28.9377
Gaus Width: 4.0195
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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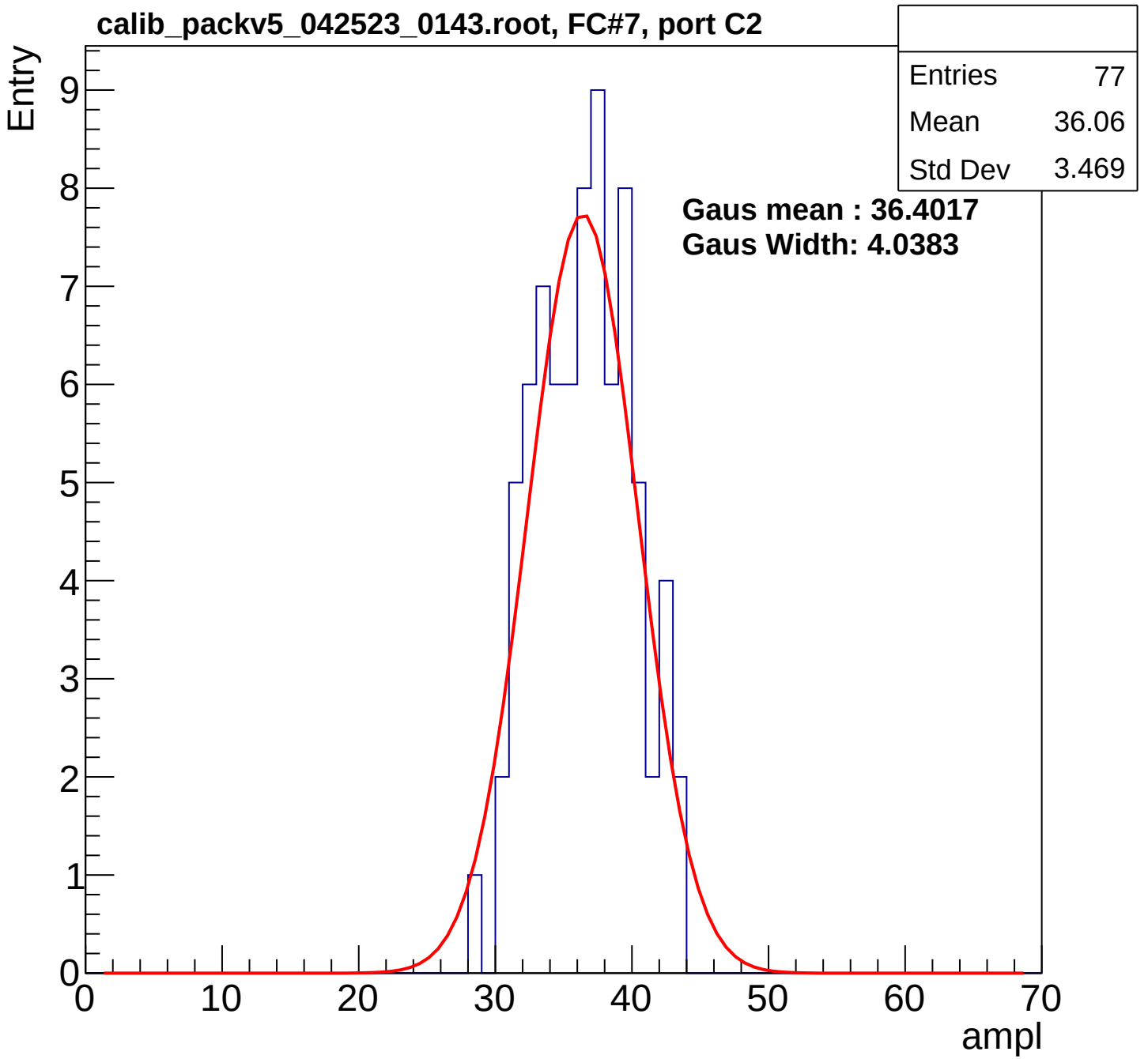
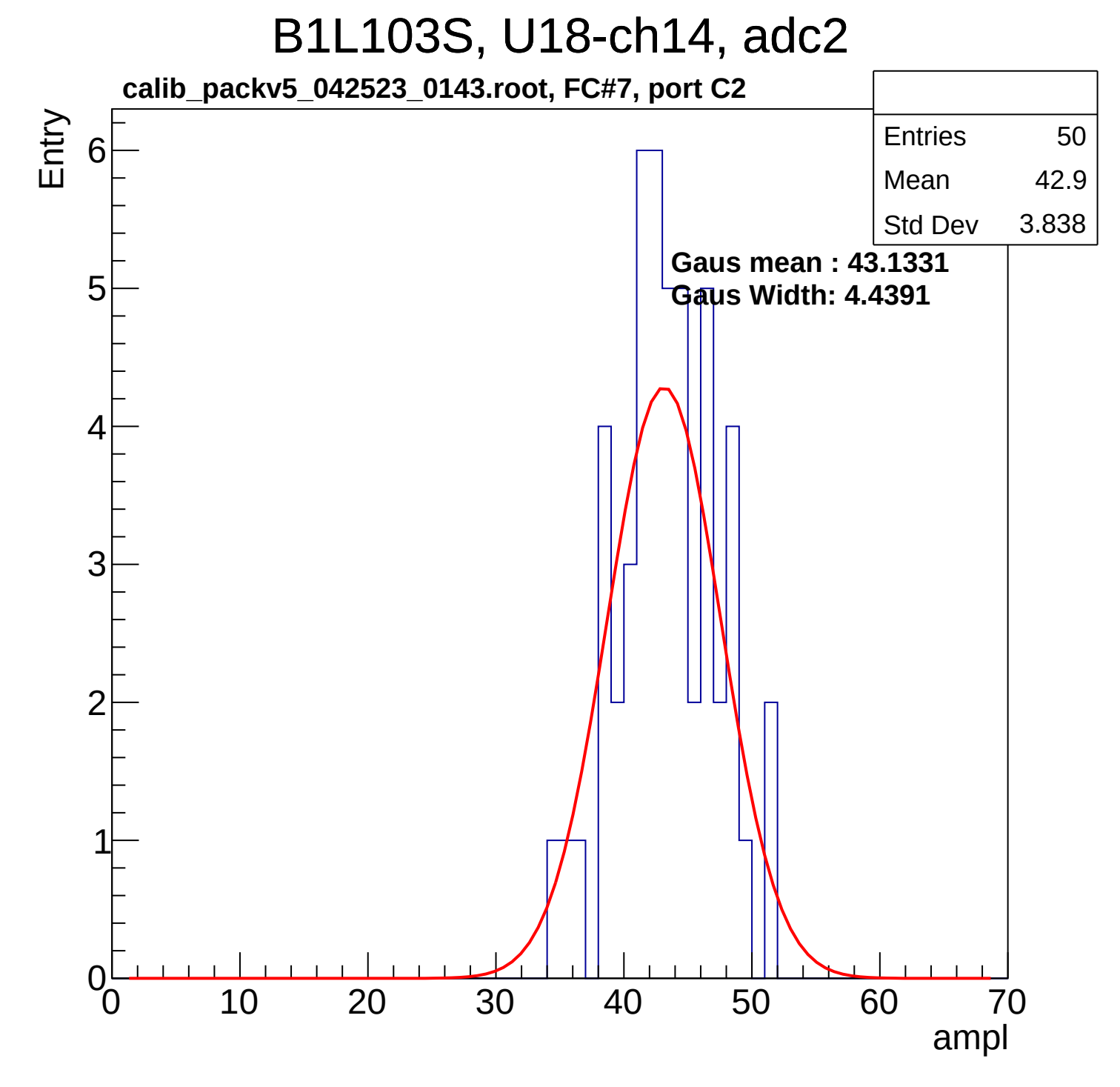

B1L103S, U18-ch14, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 77
Mean 36.06
Std Dev 3.469
Gaus mean : 36.4017
Gaus Width: 4.0383
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch14, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 50
Mean 42.9
Std Dev 3.838
Gaus mean : 43.1331
Gaus Width: 4.4391
Entry
ampl
0
1
2
3
4
5
6
0
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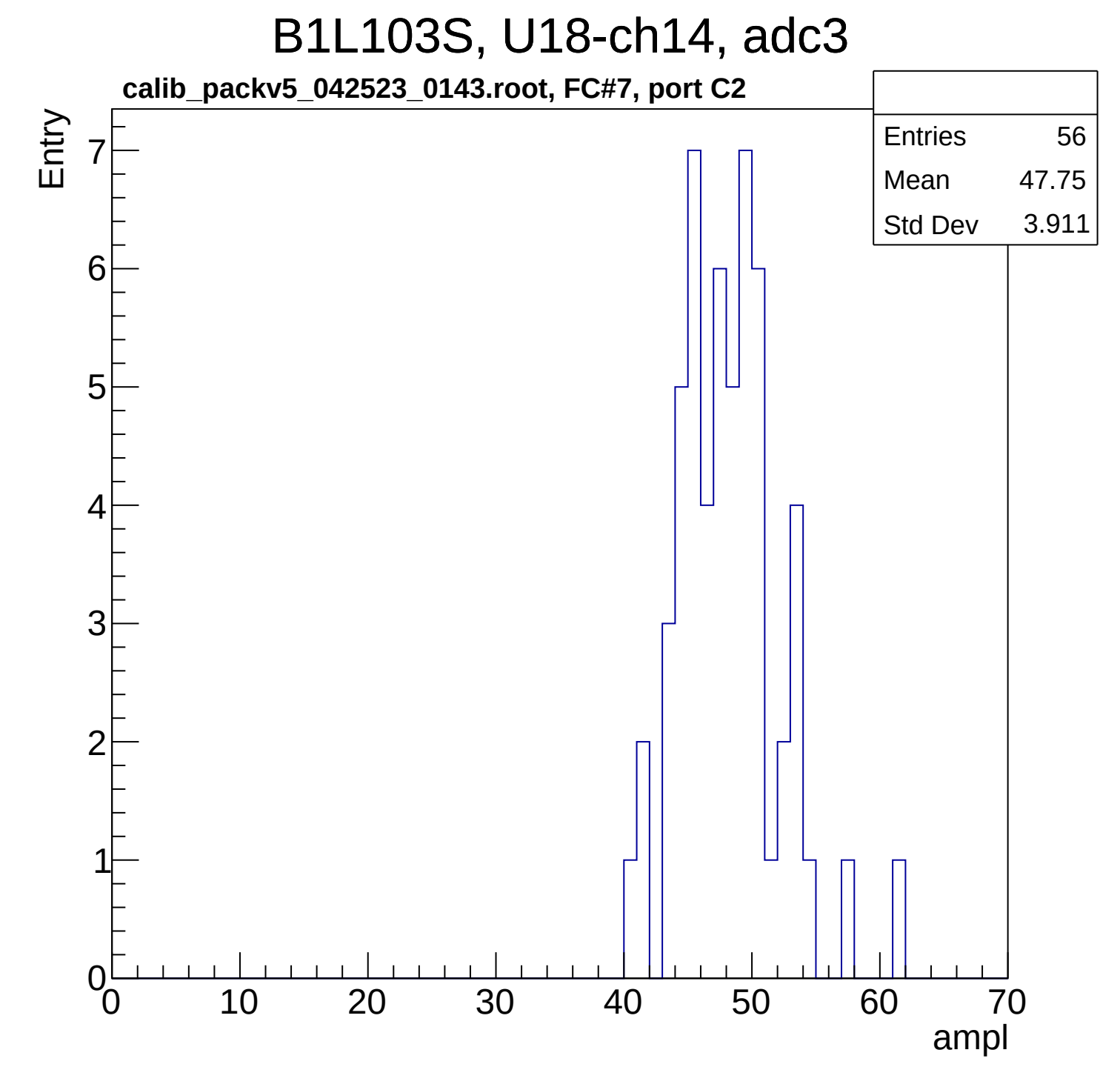
40
50
60
70


B1L103S, U18-ch14, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 47.75
Std Dev 3.911
Entry
ampl
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4
5
6
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0
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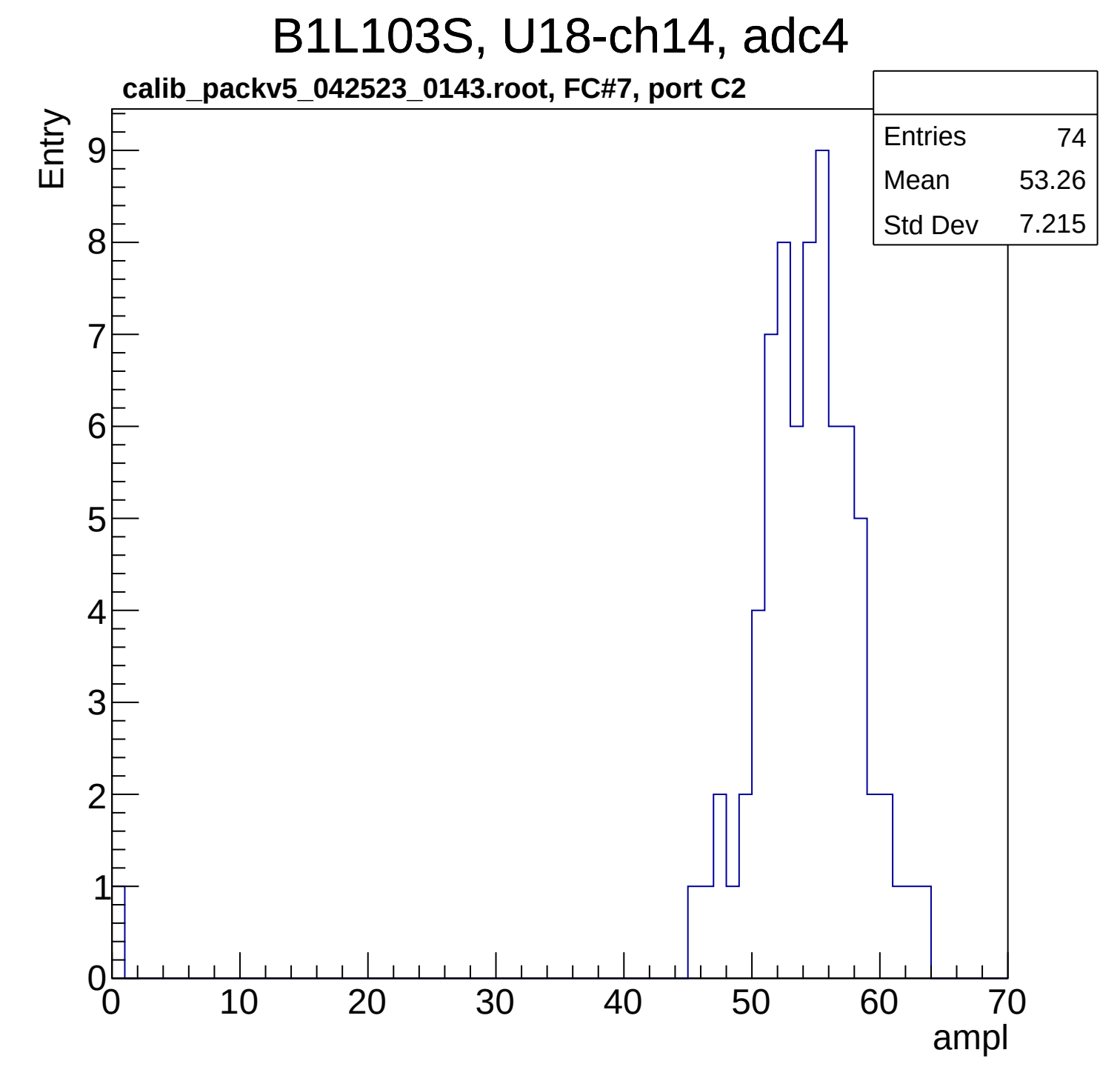
B1L103S, U18-ch14, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 74
Mean 53.26
Std Dev 7.215
Entry
ampl
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4
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6
7
8
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0
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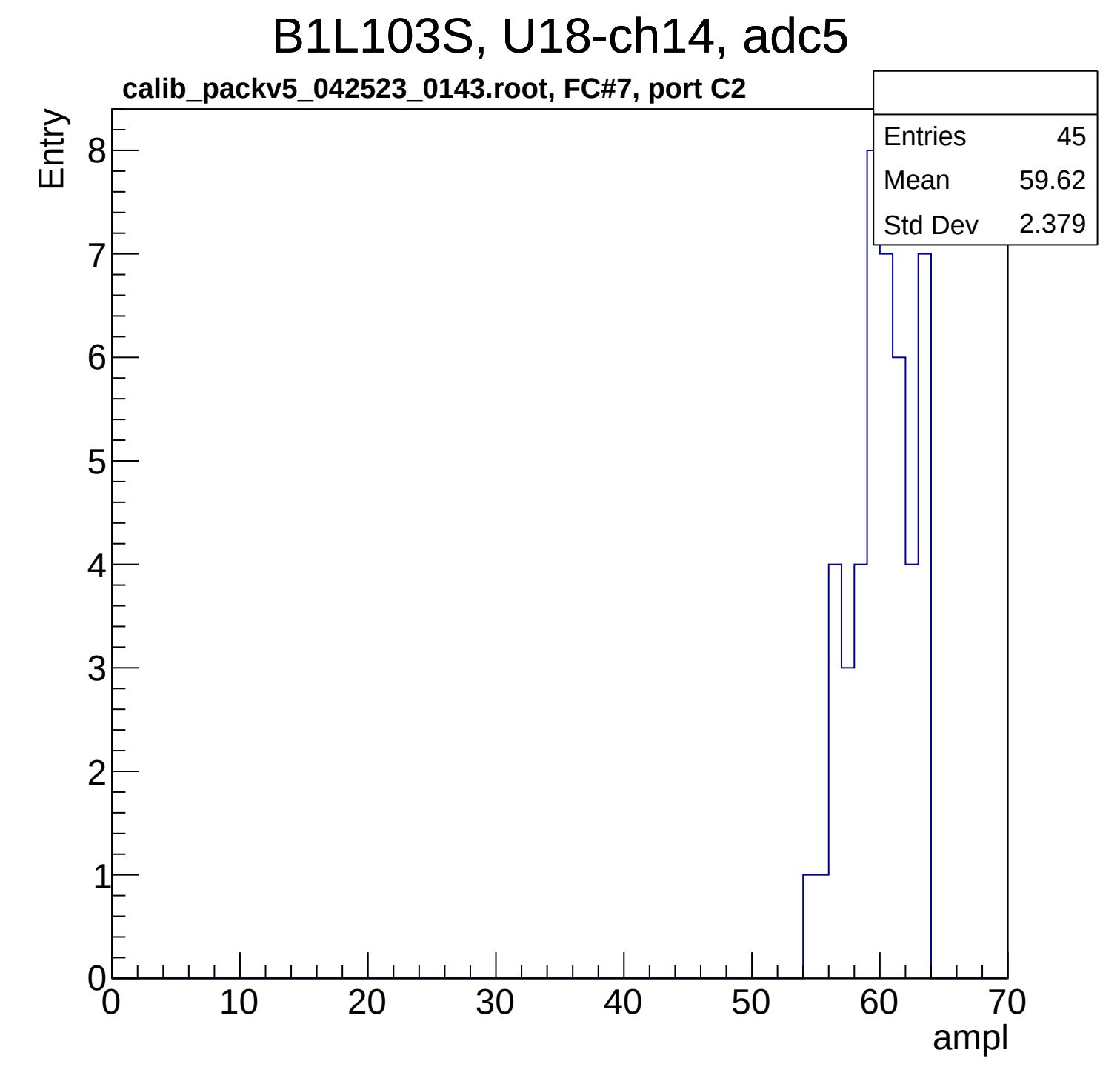
B1L103S, U18-ch14, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 45
Mean 59.62
Std Dev 2.379
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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60
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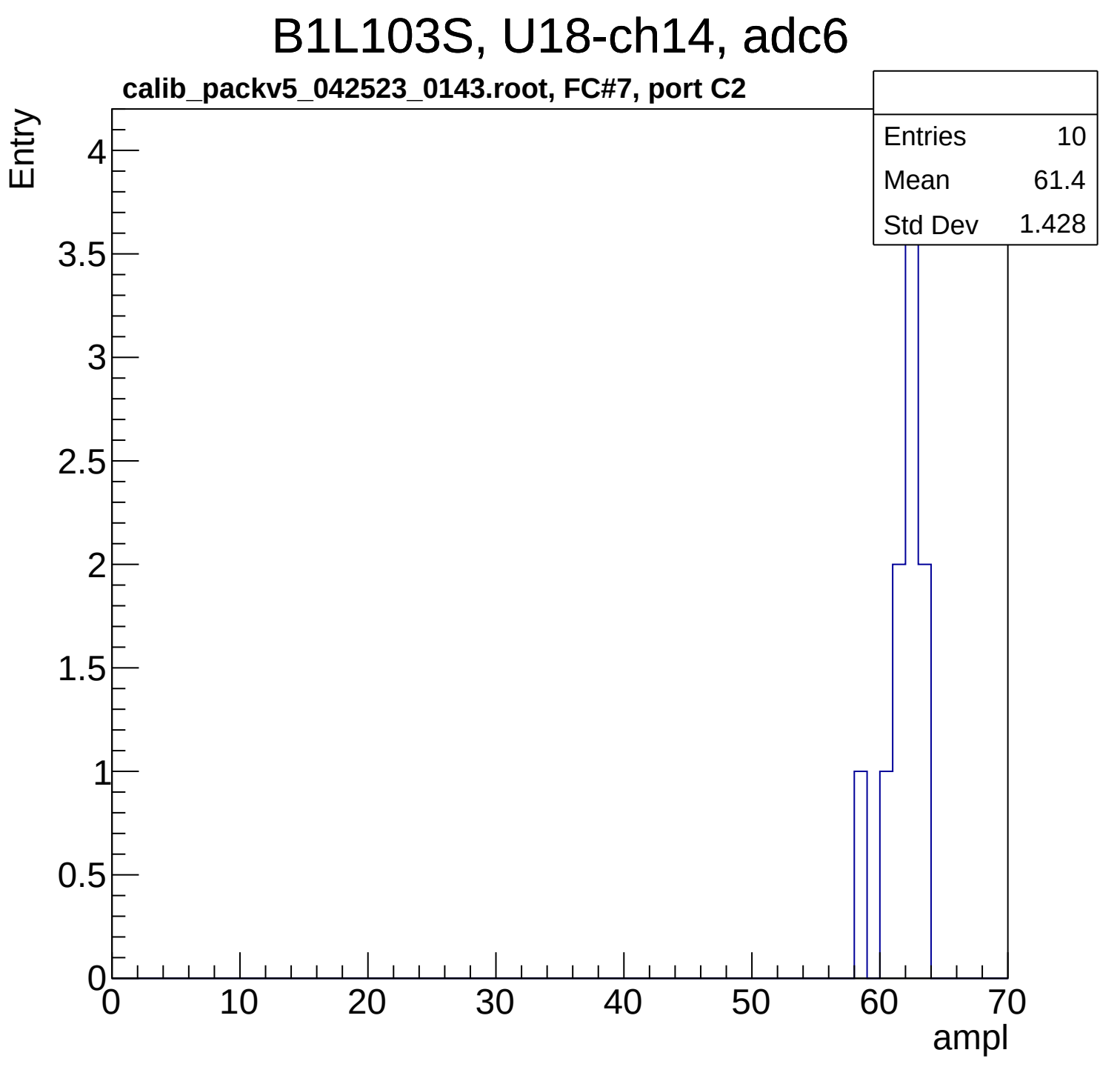
B1L103S, U18-ch14, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 10
Mean 61.4
Std Dev 1.428
Entry
ampl
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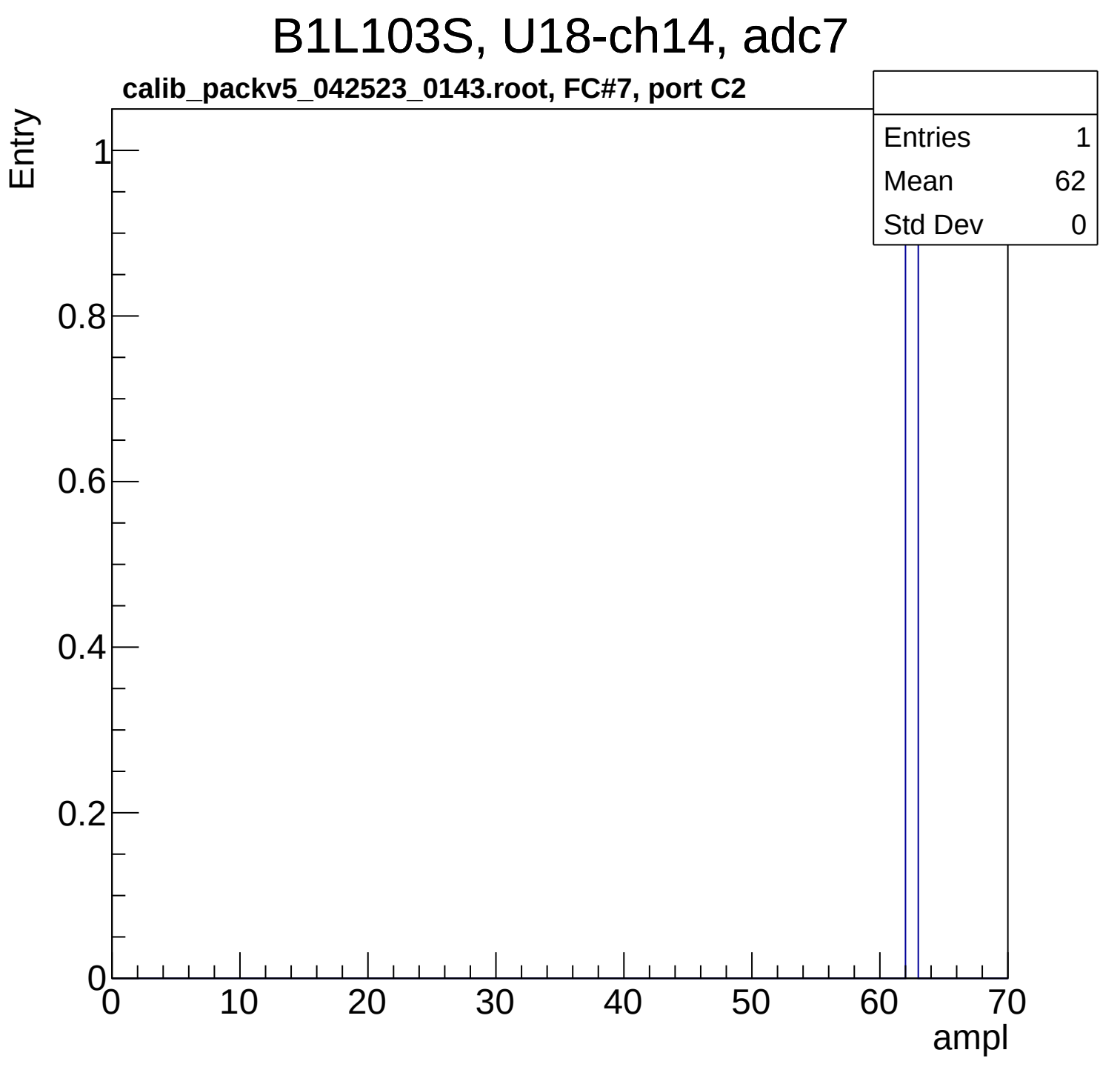
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U18-ch14, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 62
Std Dev 0
Entry
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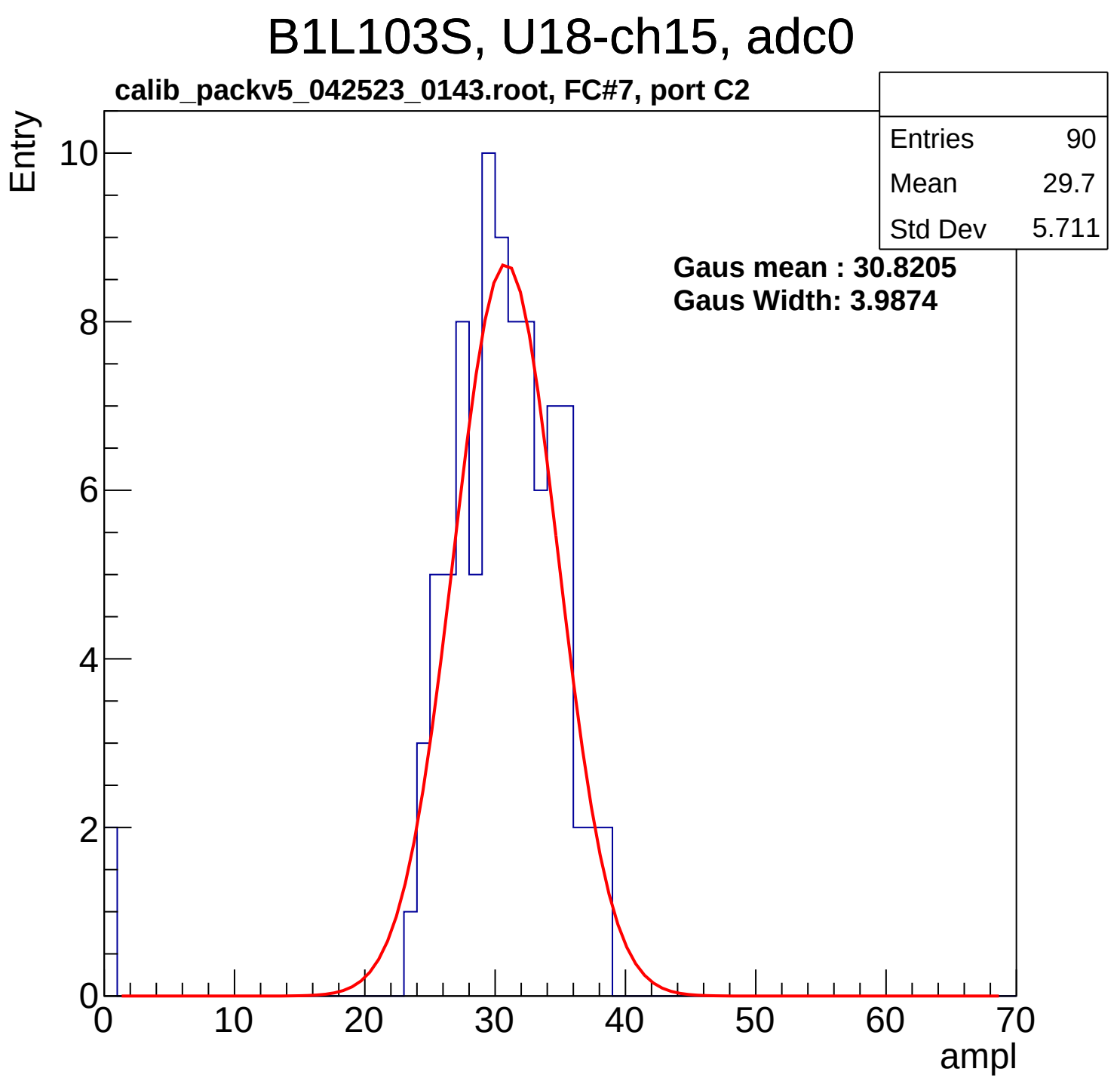
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch15, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 90
Mean 29.7
Std Dev 5.711
Gaus mean : 30.8205
Gaus Width: 3.9874
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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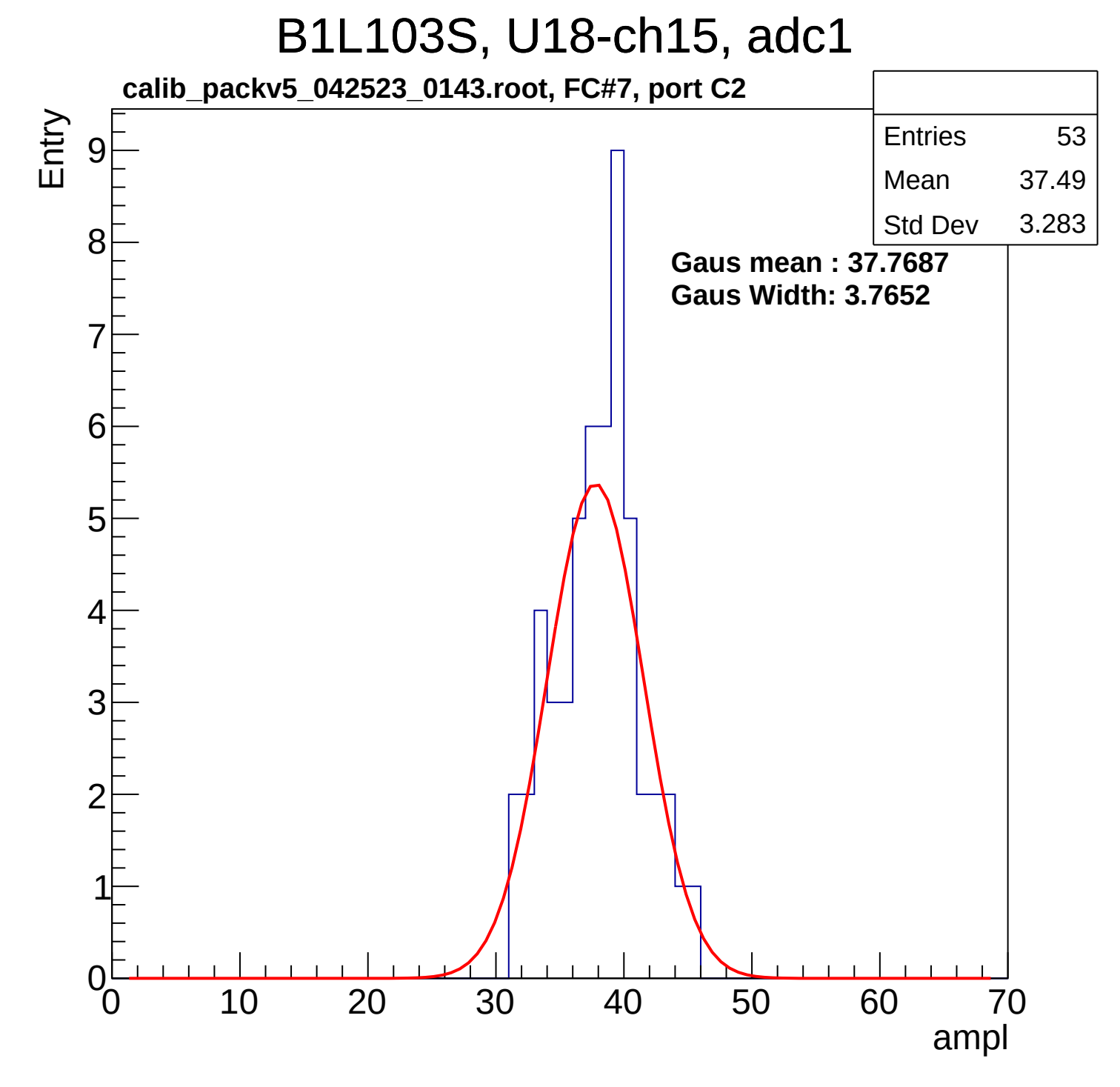
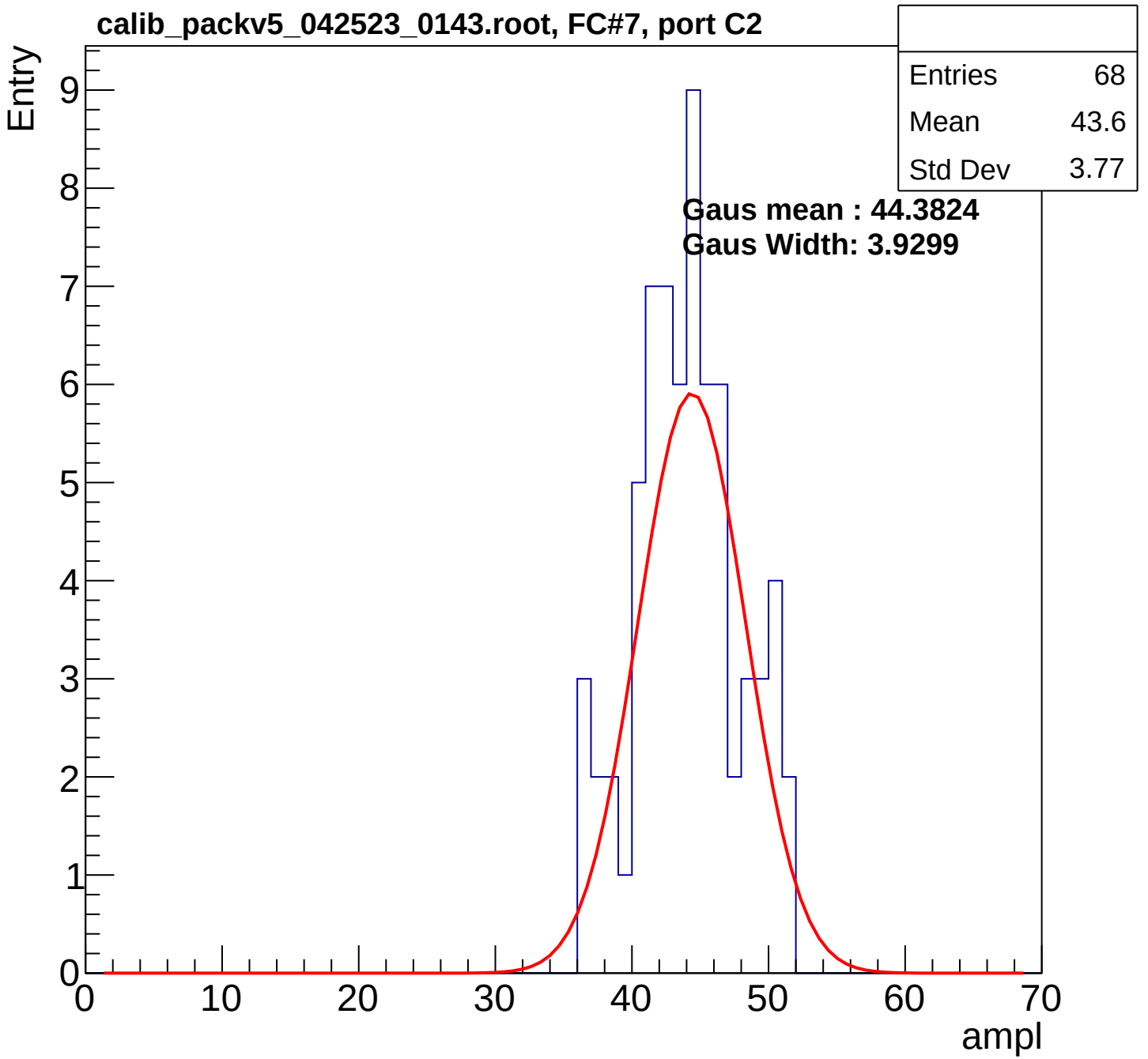

B1L103S, U18-ch15, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 37.49
Std Dev 3.283
Gaus mean : 37.7687
Gaus Width: 3.7652
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch15, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 43.6
Std Dev 3.77
Gaus mean : 44.3824
Gaus Width: 3.9299
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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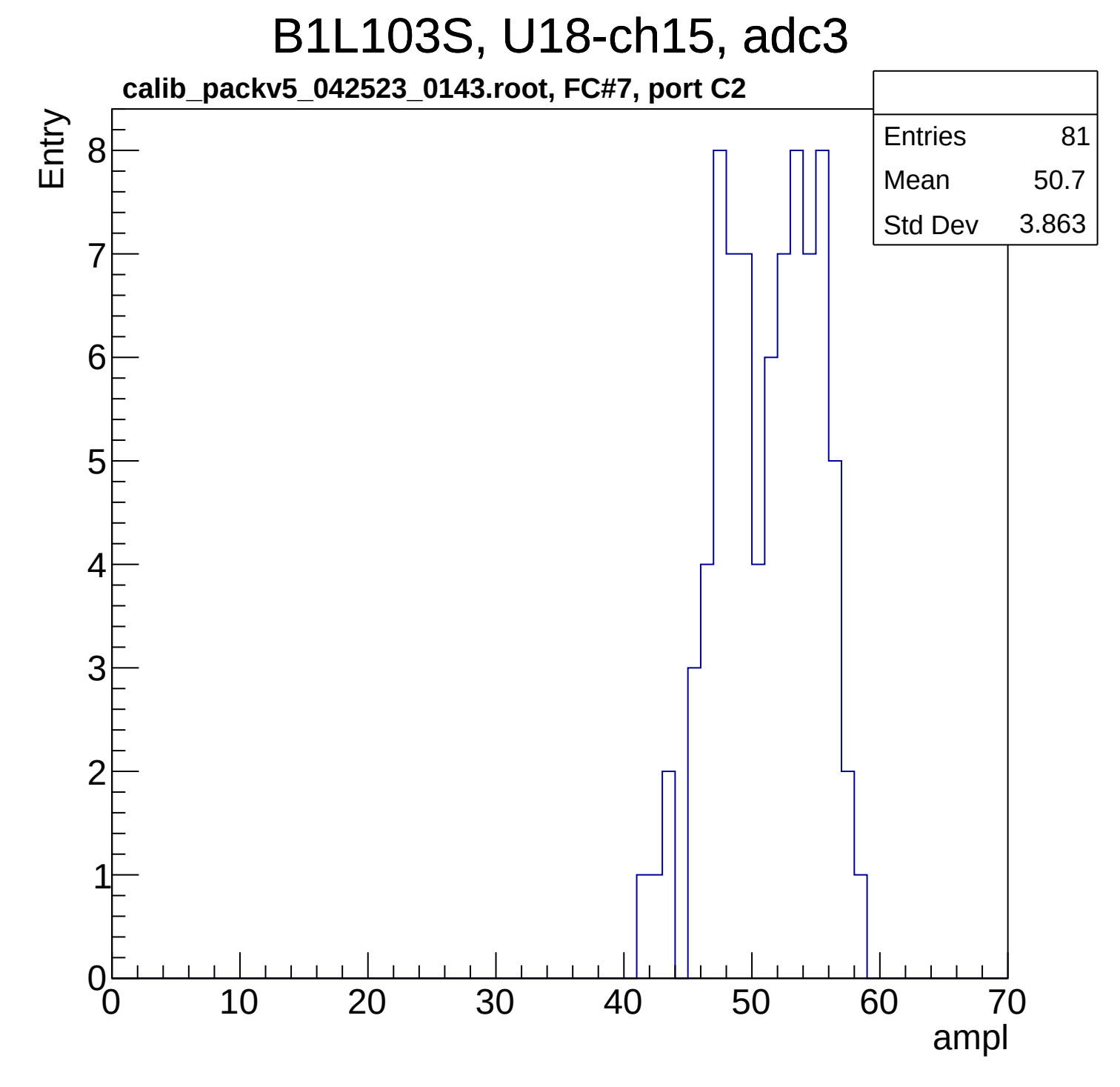
B1L103S, U18-ch15, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 81
Mean 50.7
Std Dev 3.863
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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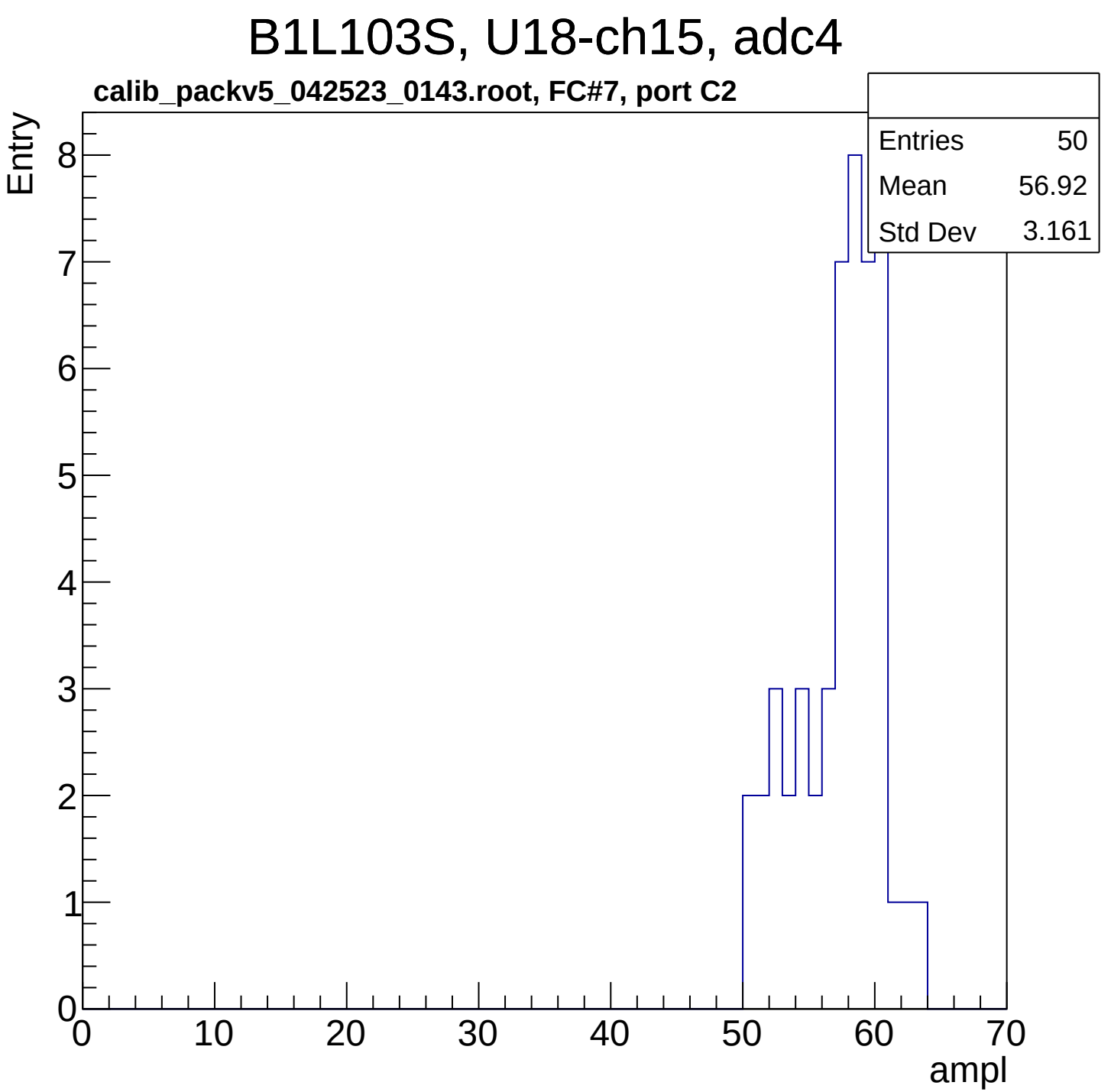
B1L103S, U18-ch15, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 50
Mean 56.92
Std Dev 3.161
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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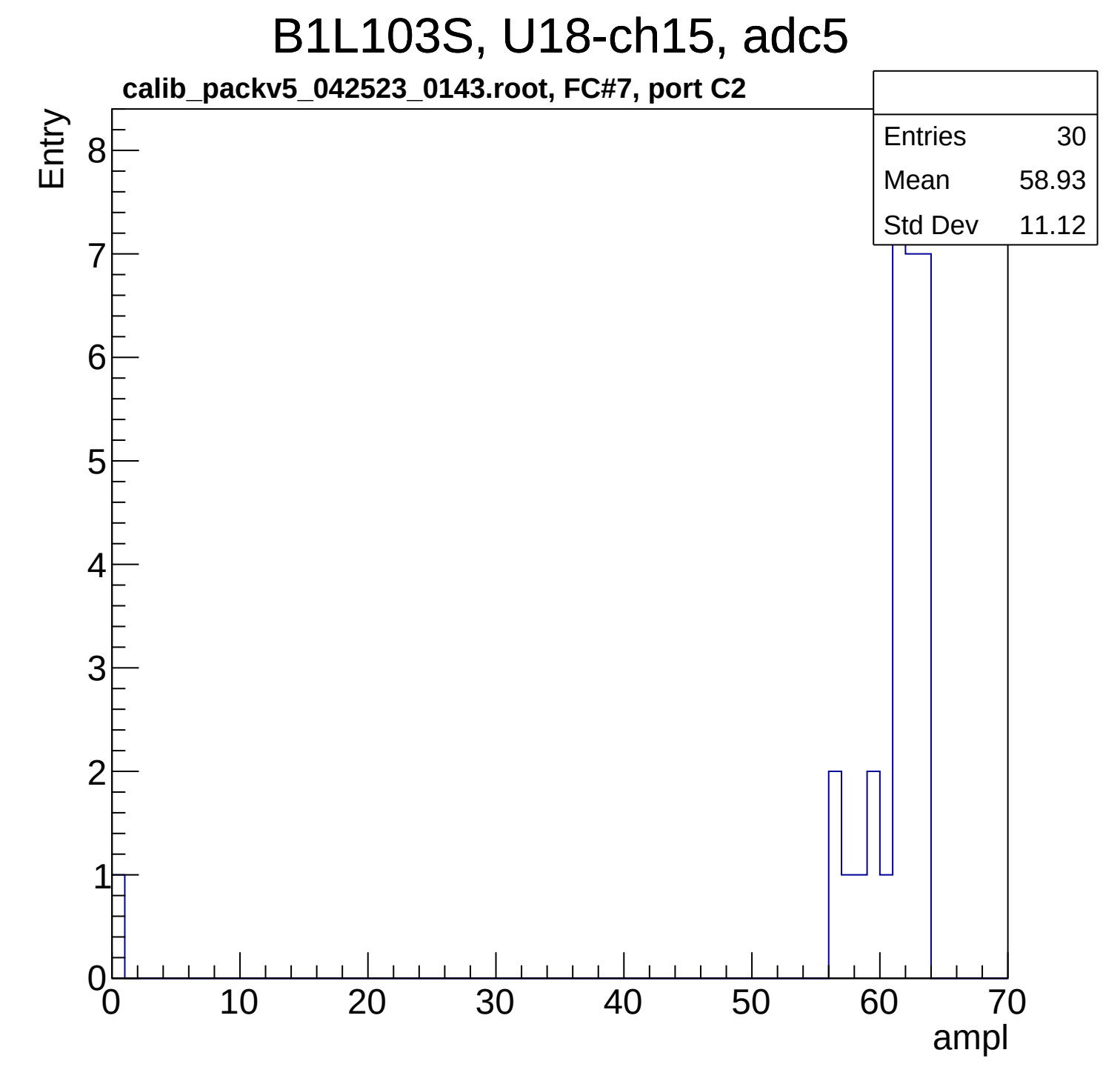
B1L103S, U18-ch15, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 30
Mean 58.93
Std Dev 11.12
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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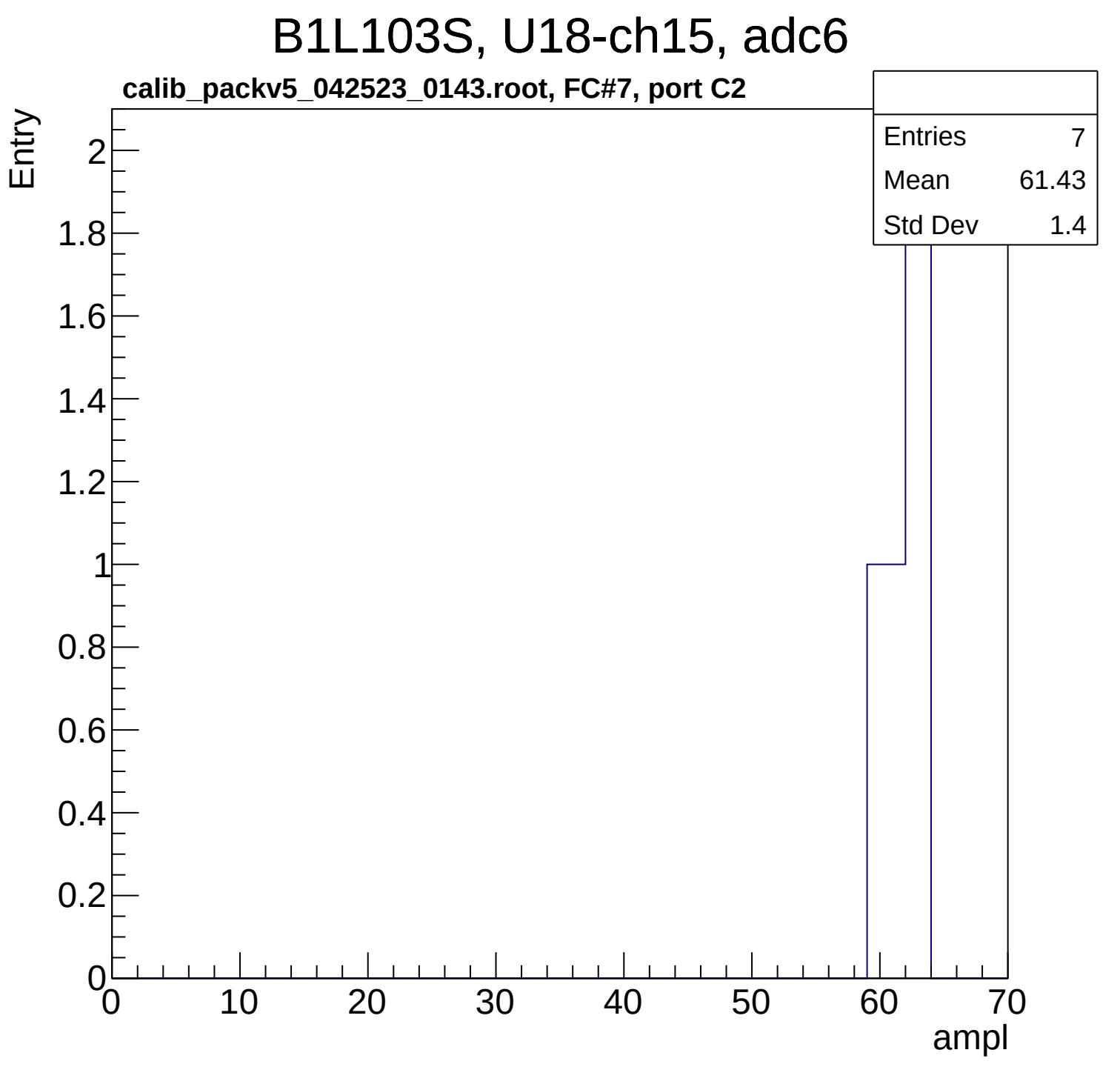
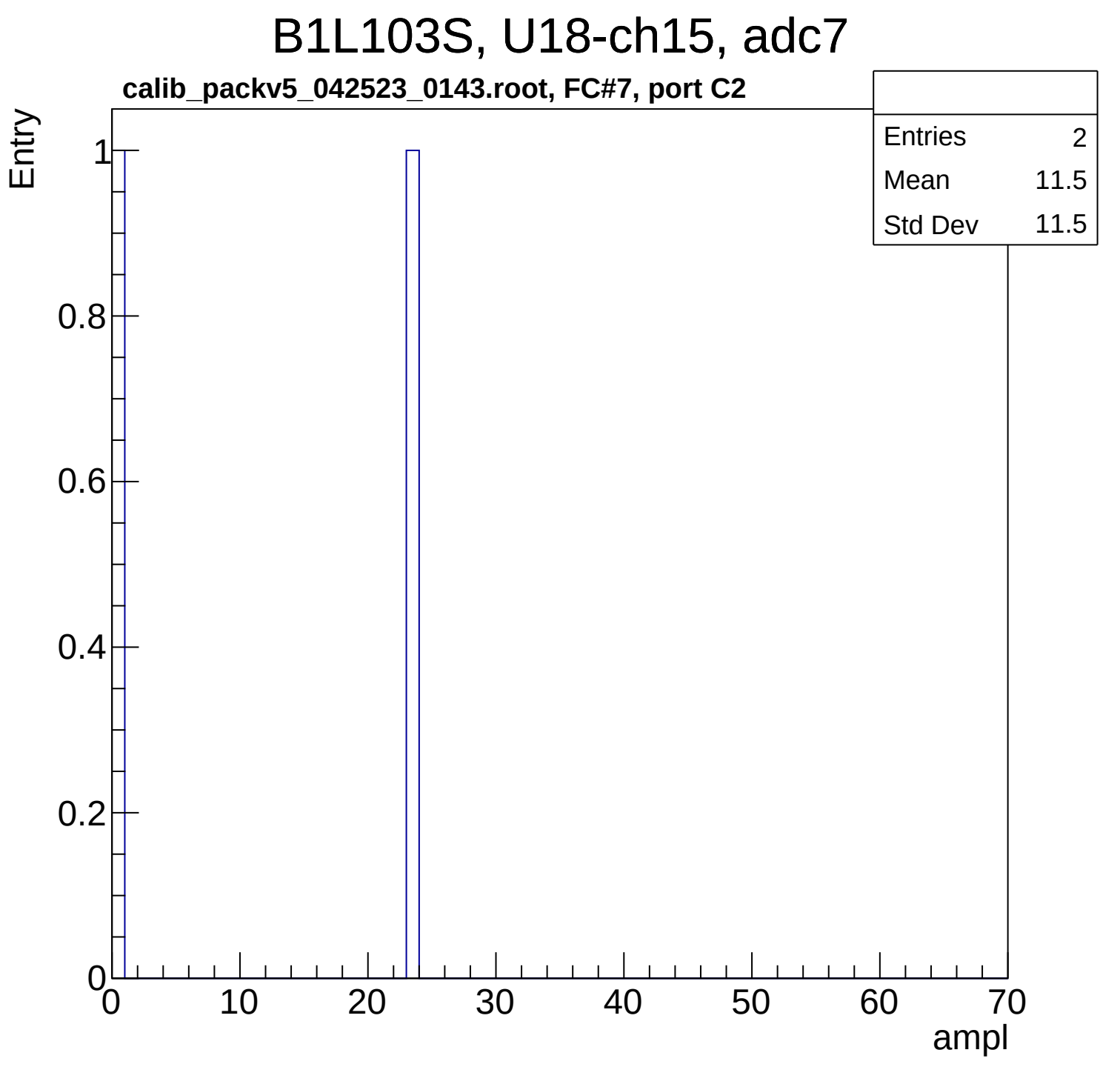
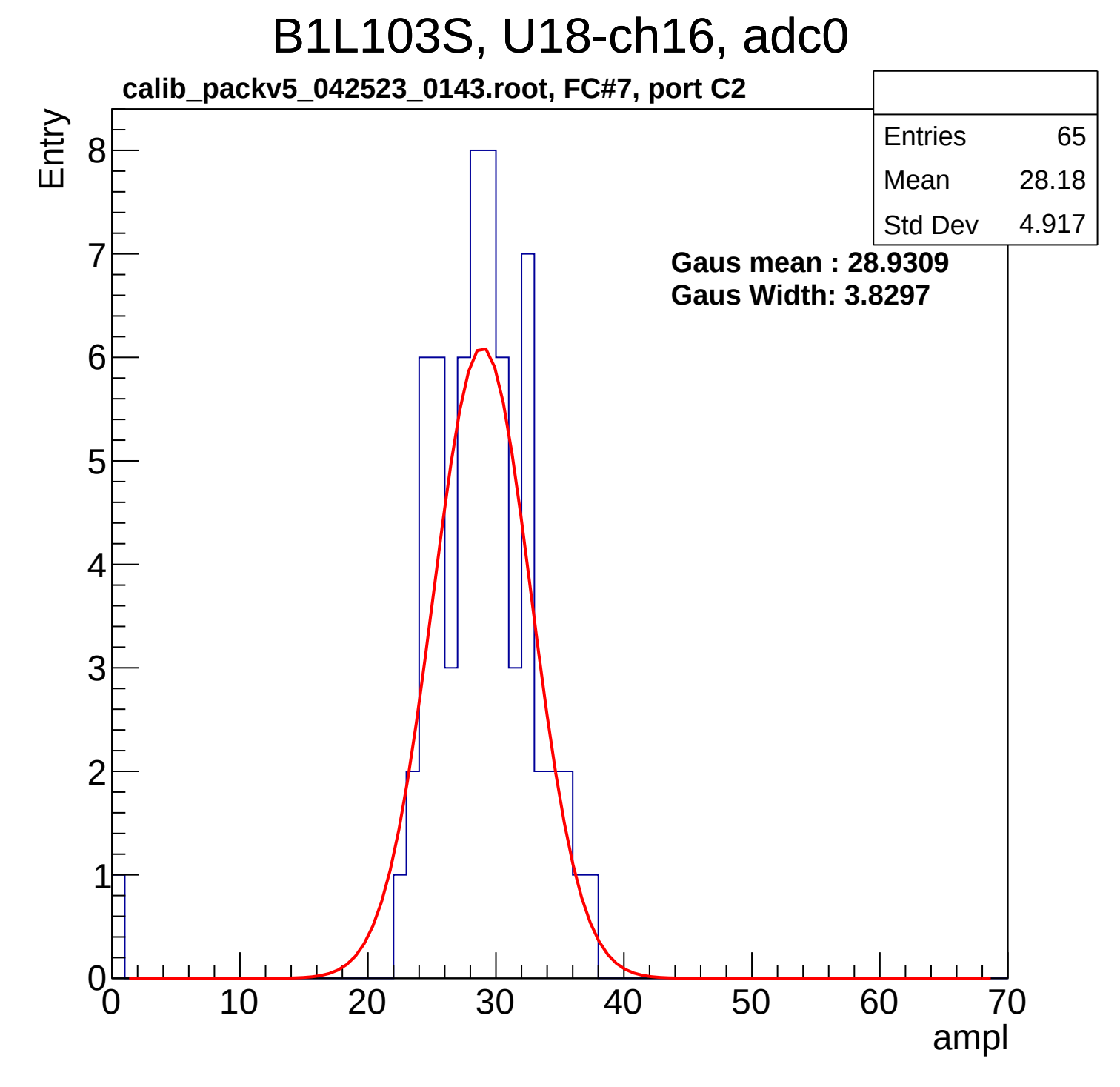
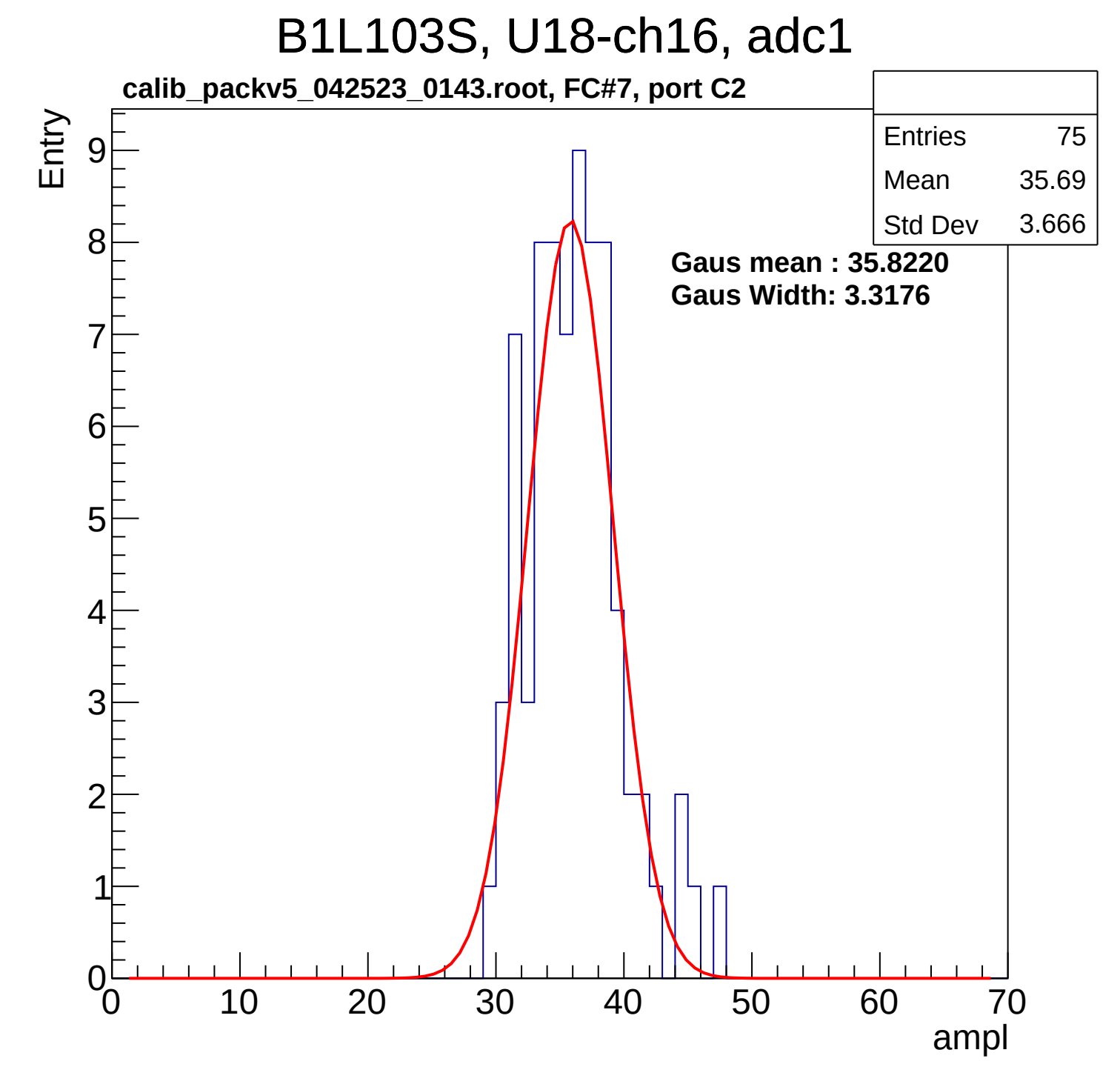

B1L103S, U18-ch15, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 7
Mean 61.43
Std Dev 1.4
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U18-ch15, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 11.5
Std Dev 11.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch16, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 28.18
Std Dev 4.917
Gaus mean : 28.9309
Gaus Width: 3.8297
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch16, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 75
Mean 35.69
Std Dev 3.666
Gaus mean : 35.8220
Gaus Width: 3.3176
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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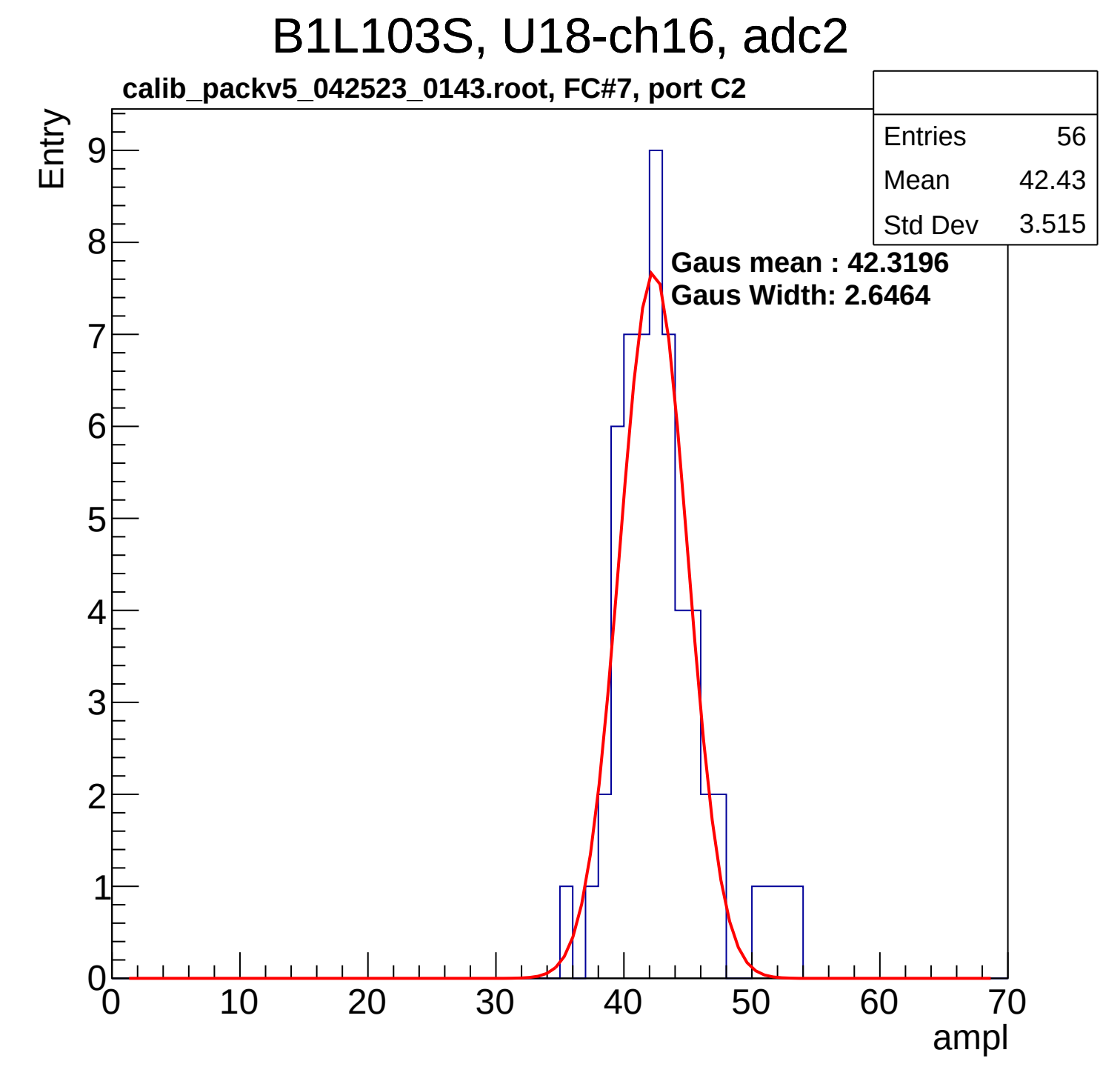
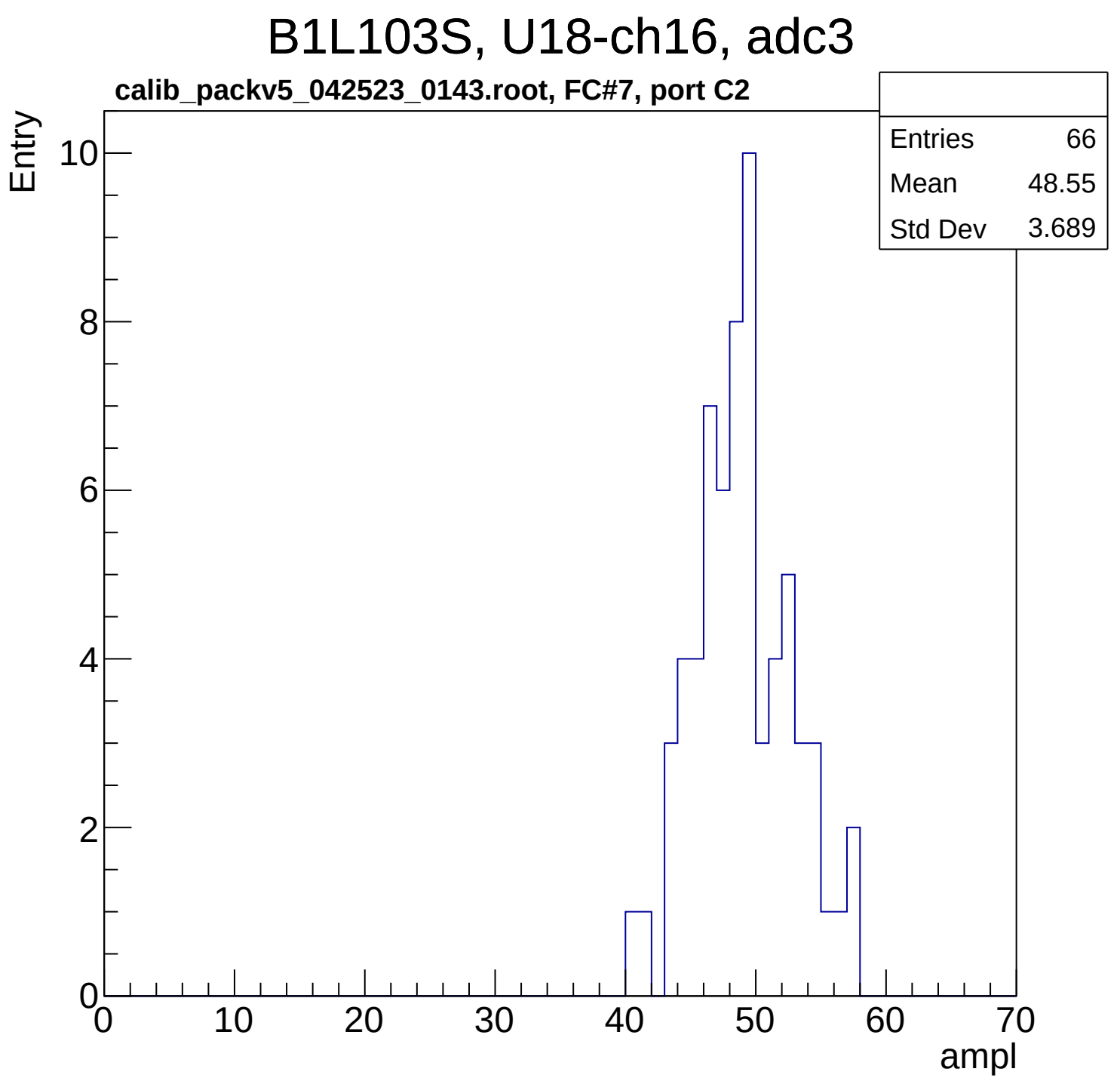
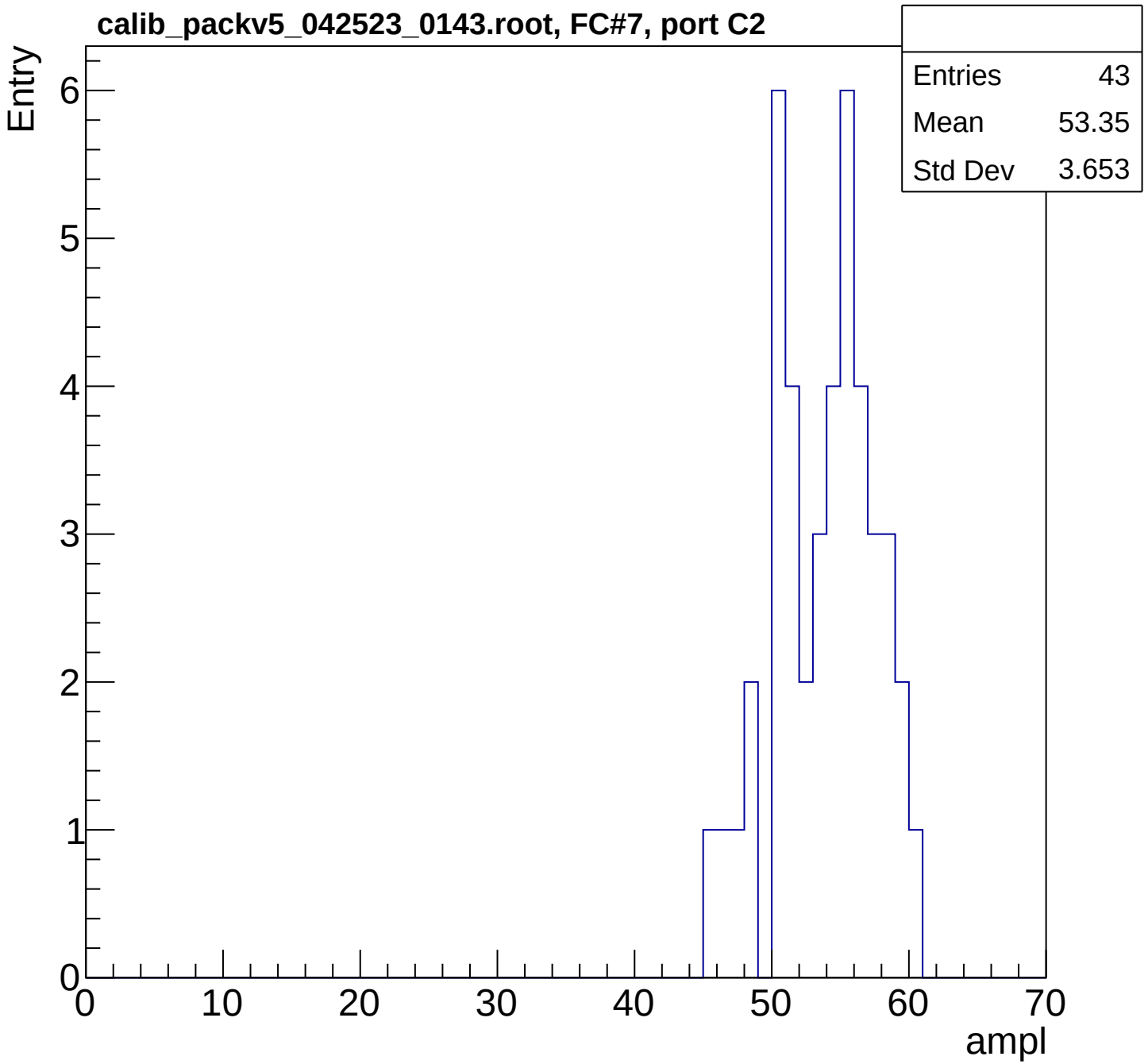
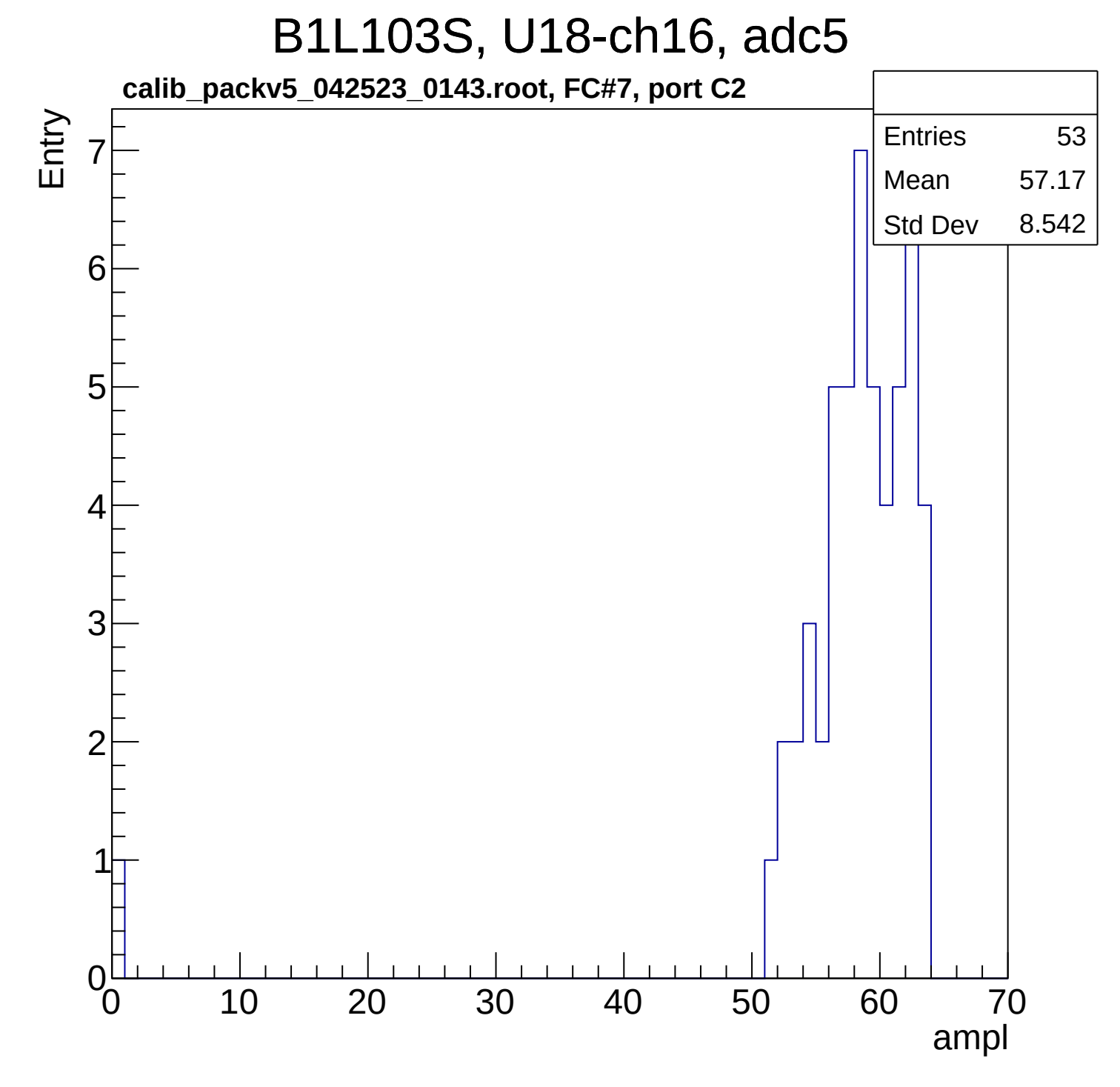
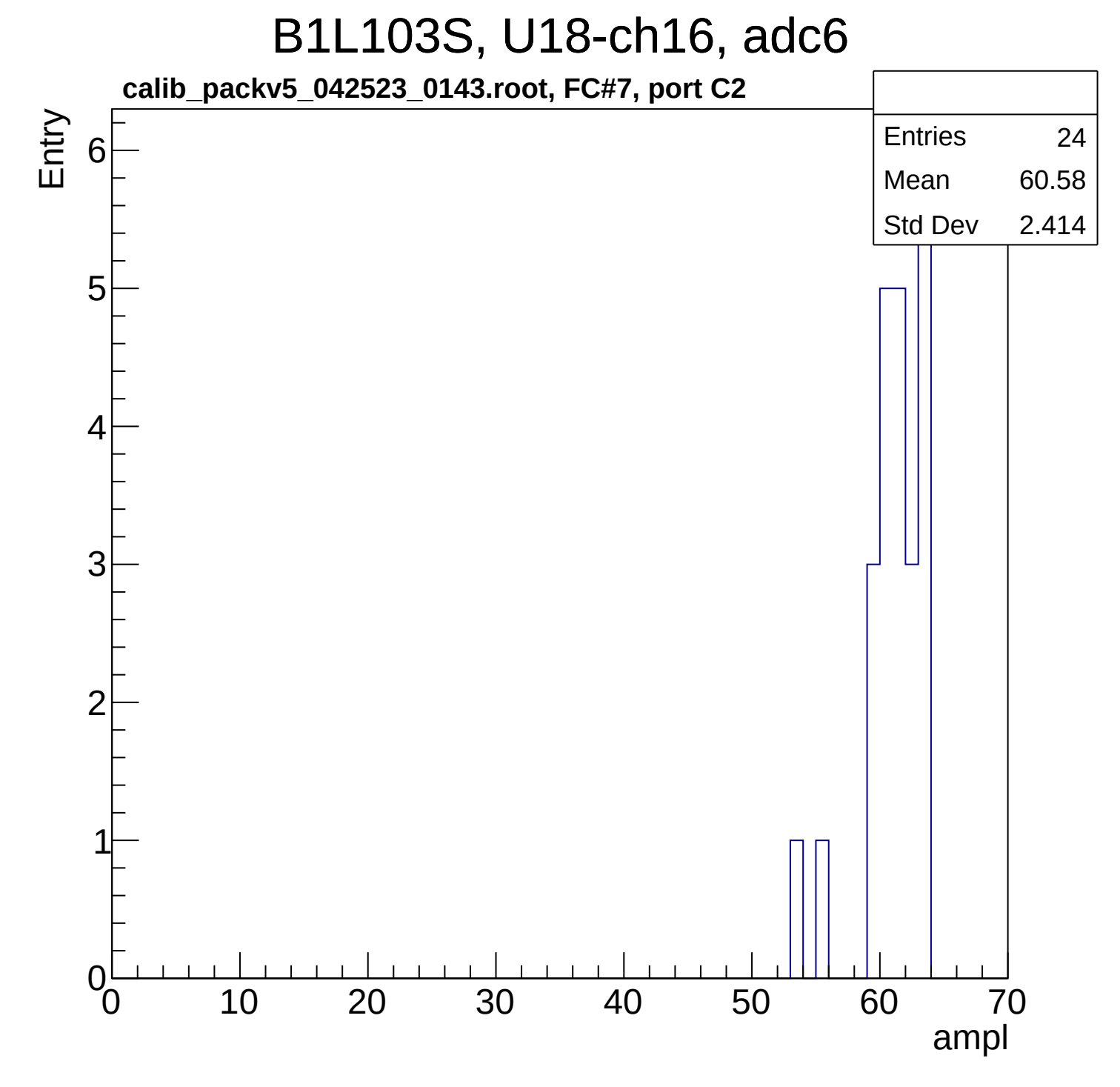
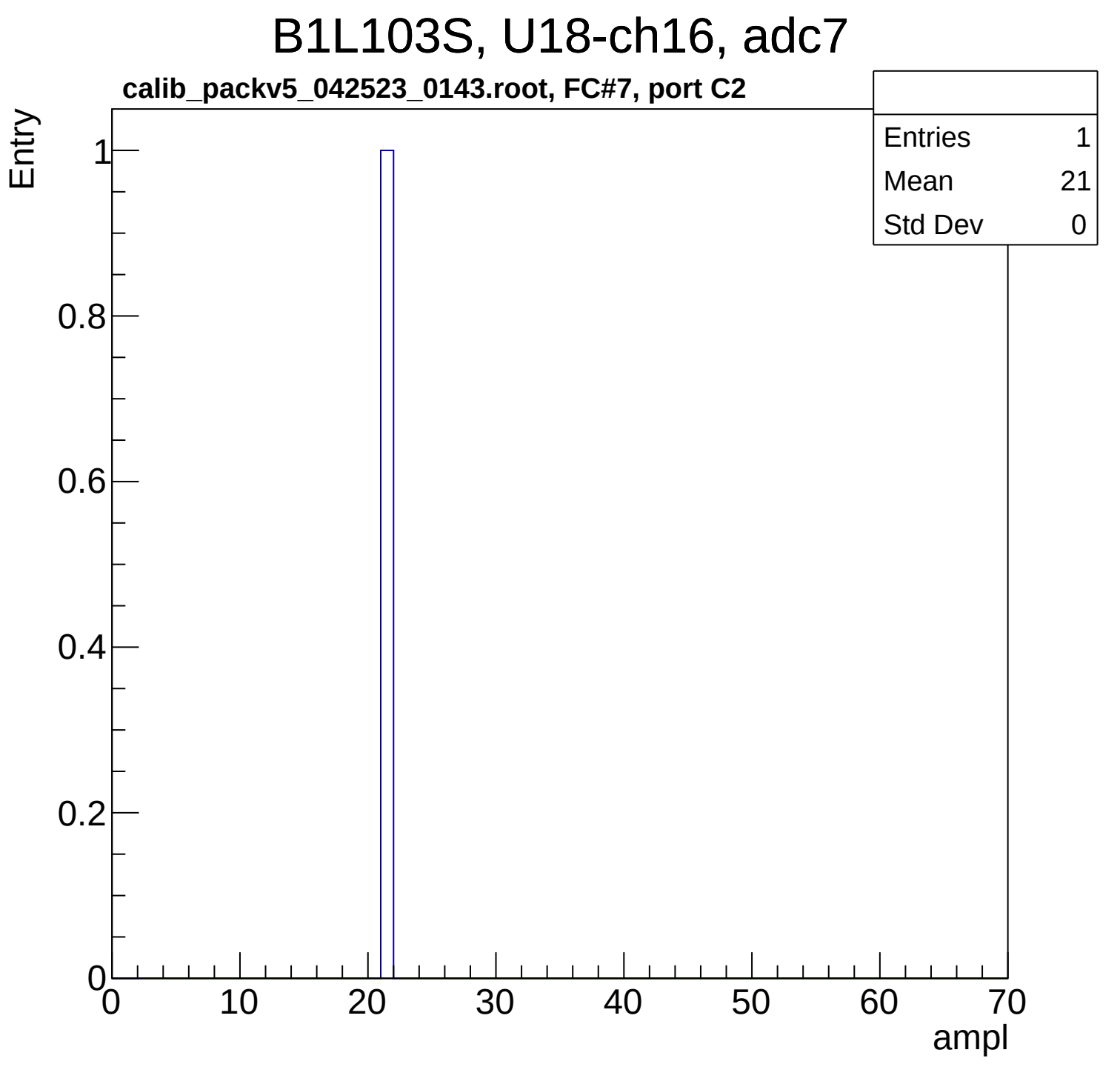

B1L103S, U18-ch16, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 42.43
Std Dev 3.515
Gaus mean : 42.3196
Gaus Width: 2.6464
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

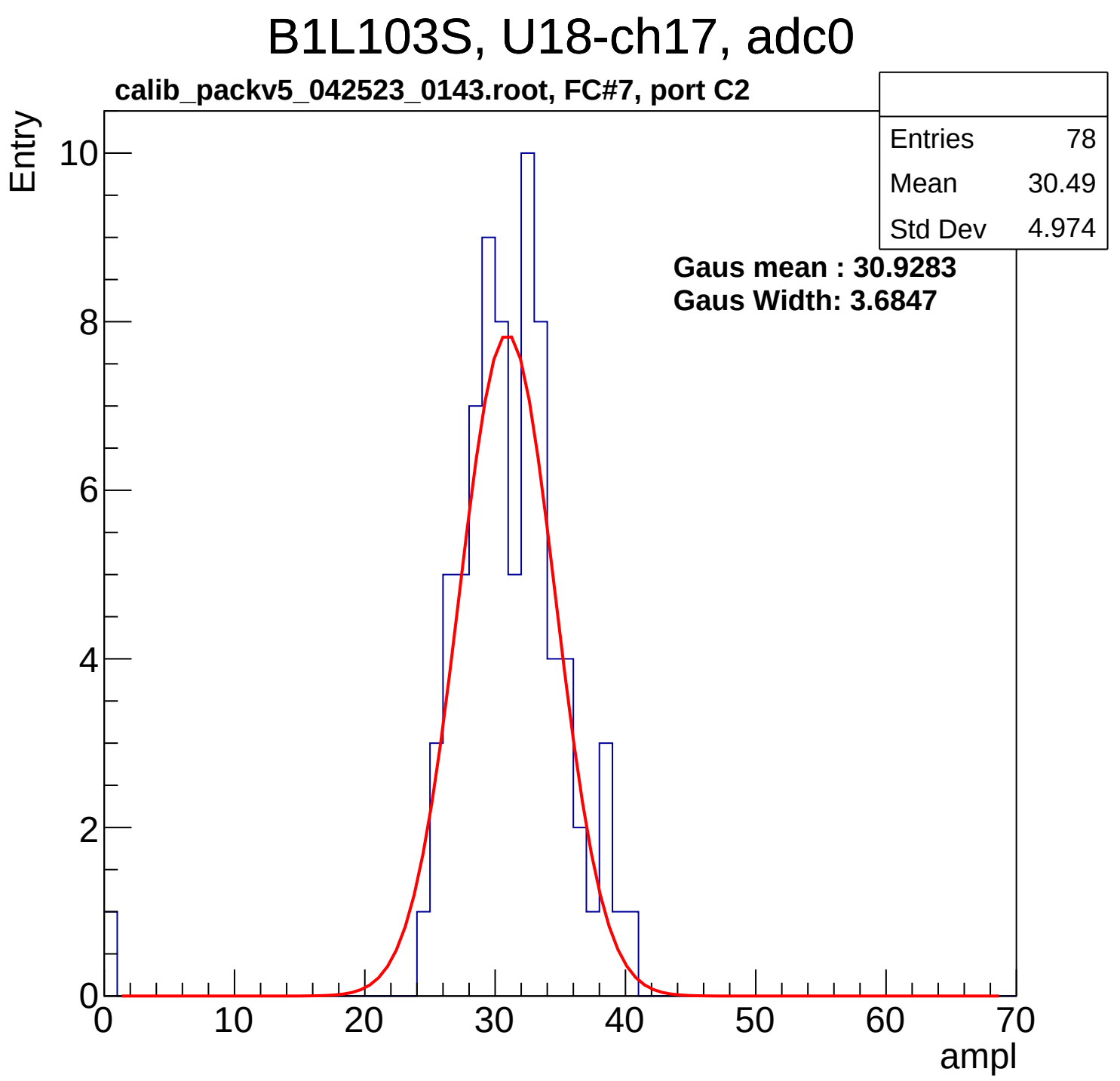

B1L103S, U18-ch16, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 48.55
Std Dev 3.689
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

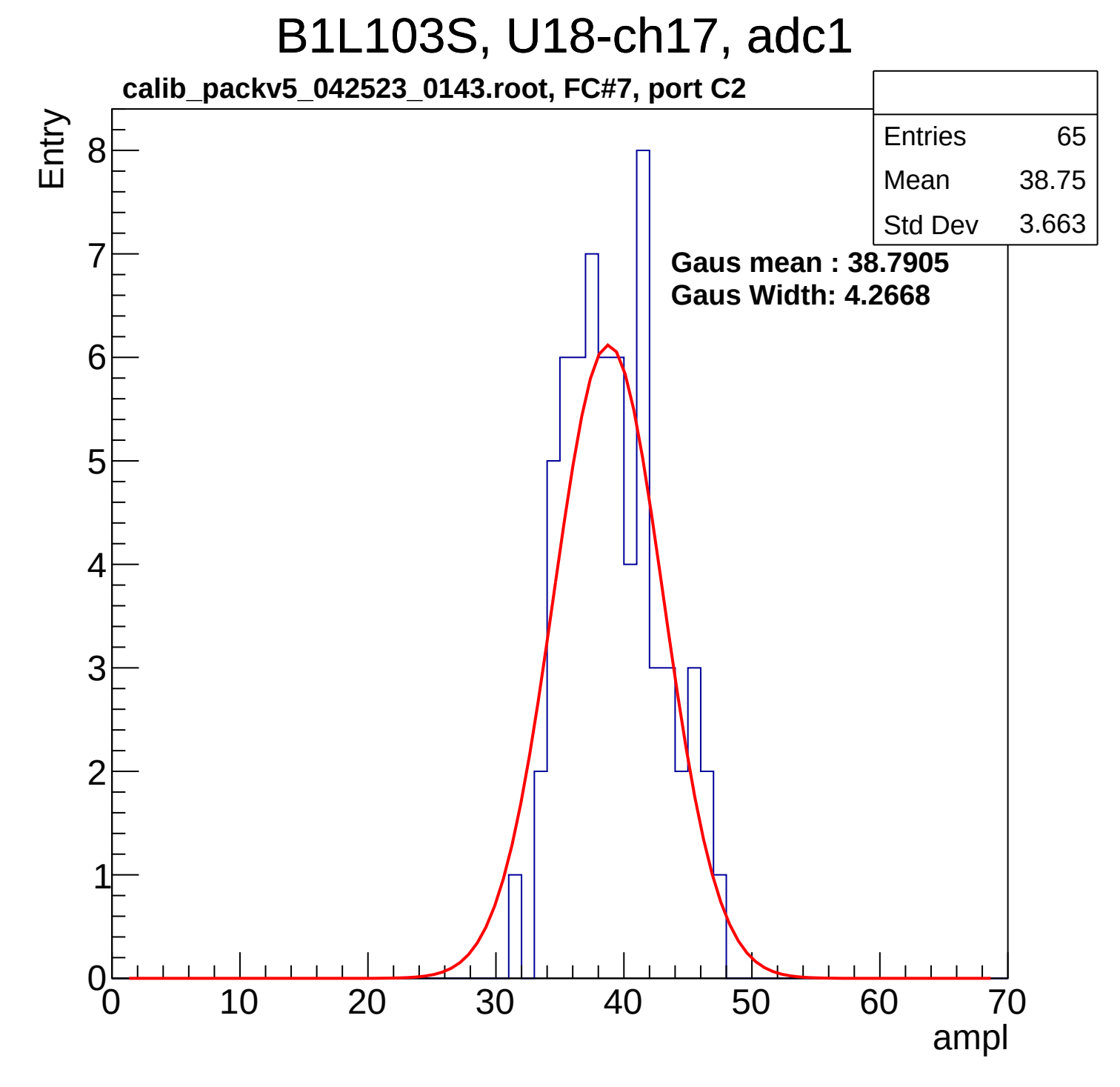

B1L103S, U18-ch16, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 43
Mean 53.35
Std Dev 3.653
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

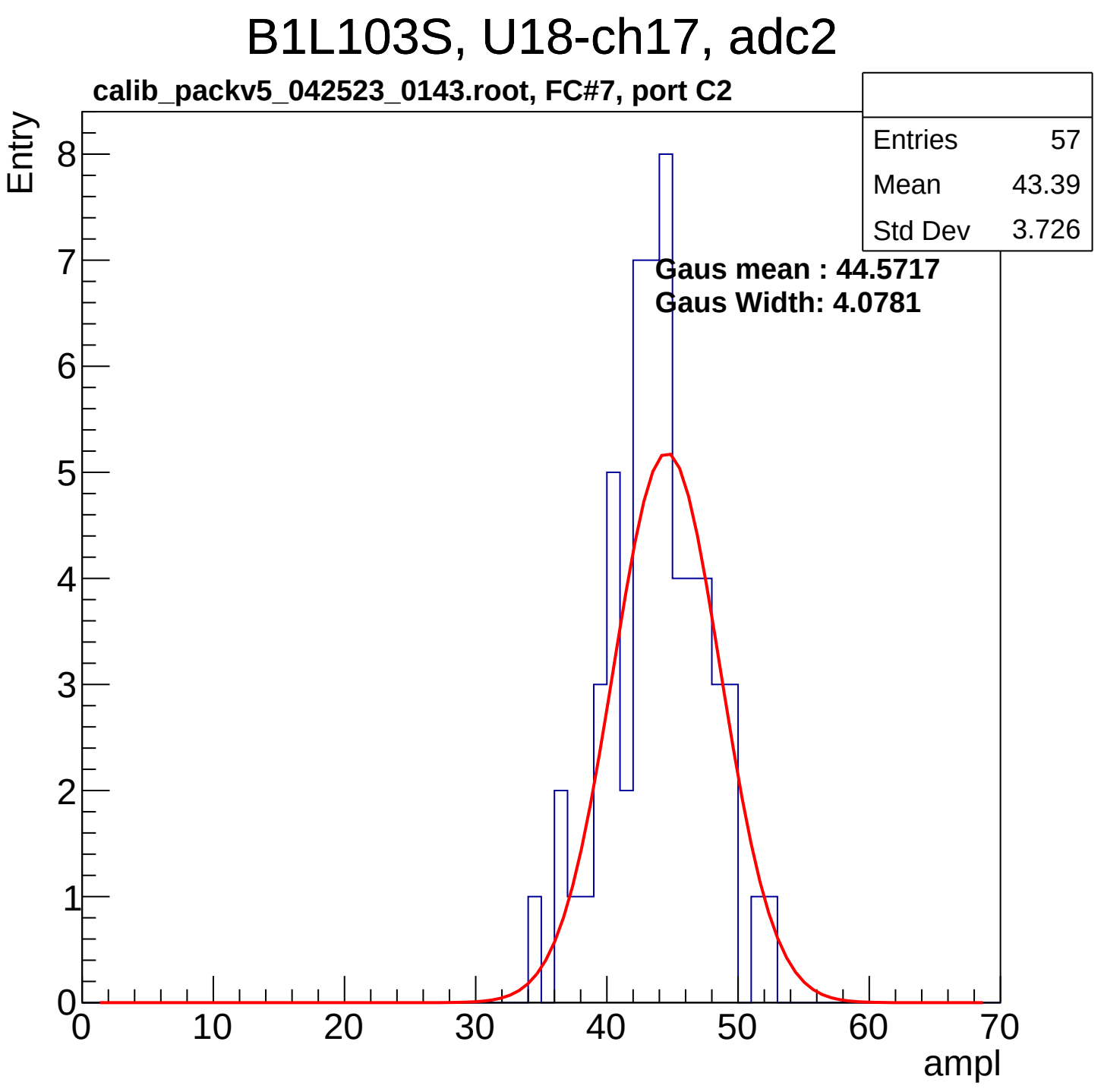

B1L103S, U18-ch16, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 57.17
Std Dev 8.542
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

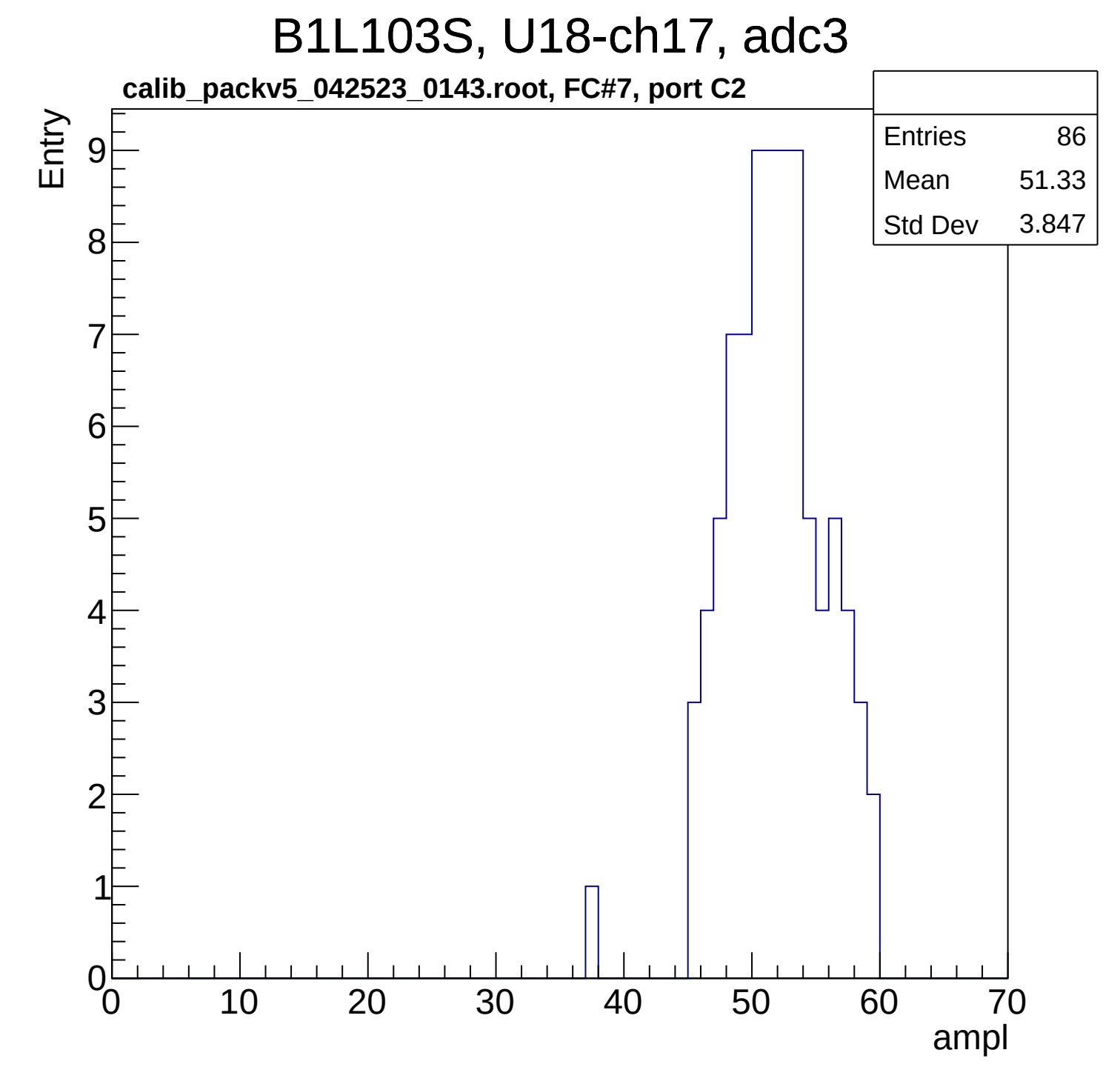

B1L103S, U18-ch16, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 24
Mean 60.58
Std Dev 2.414
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

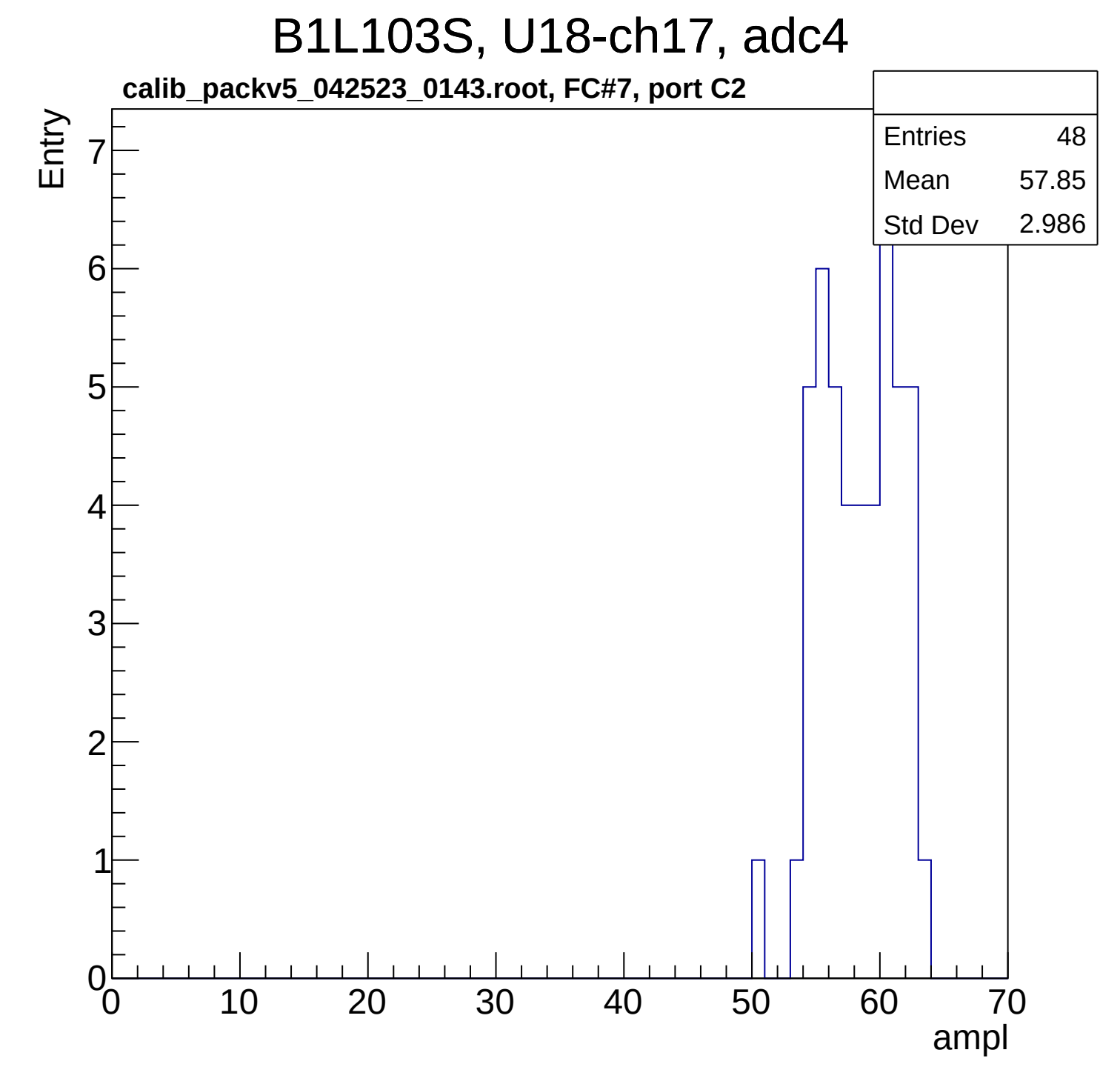

B1L103S, U18-ch16, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 21
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

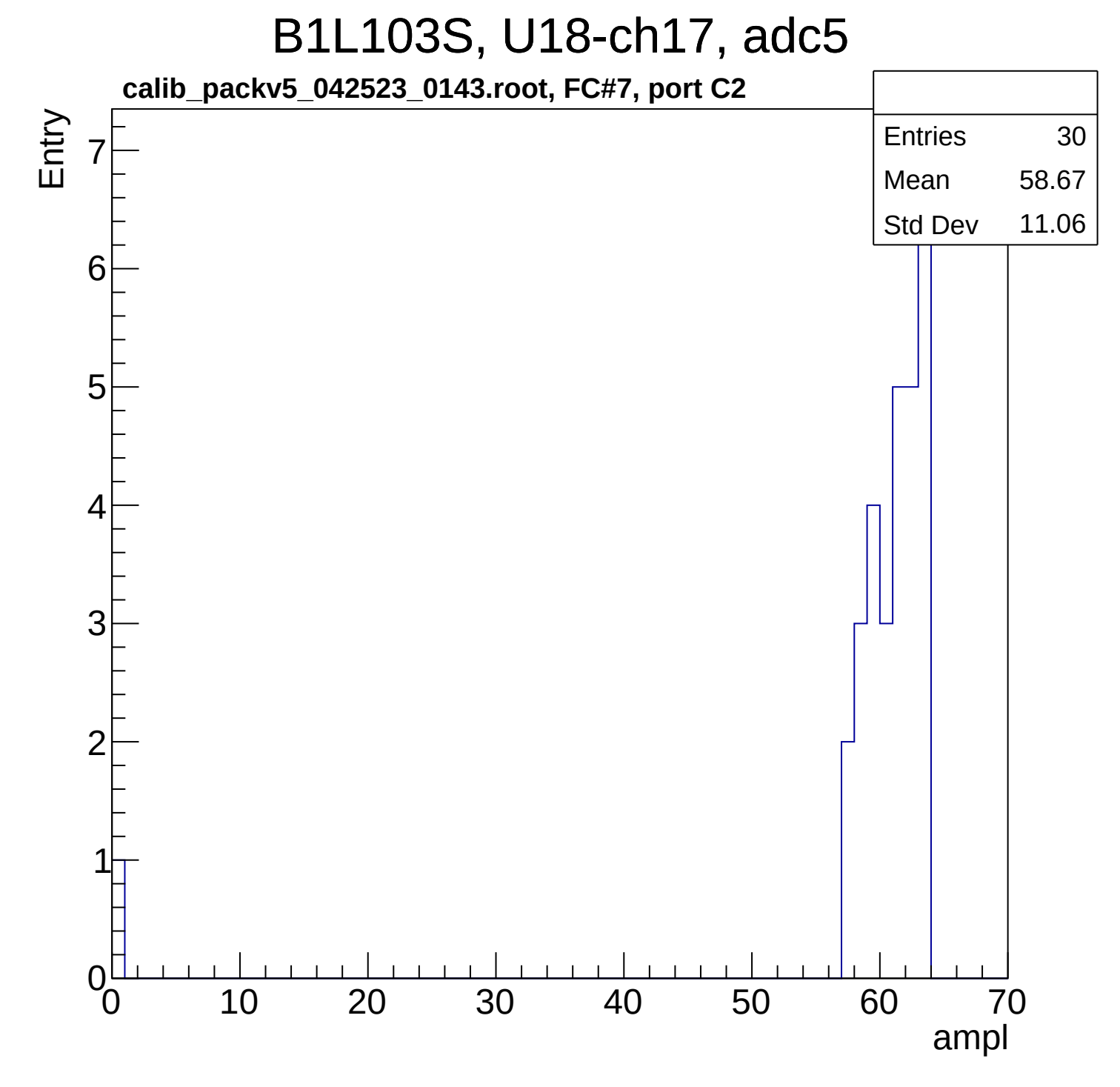

B1L103S, U18-ch17, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 78
Mean 30.49
Std Dev 4.974
Gaus mean : 30.9283
Gaus Width: 3.6847
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

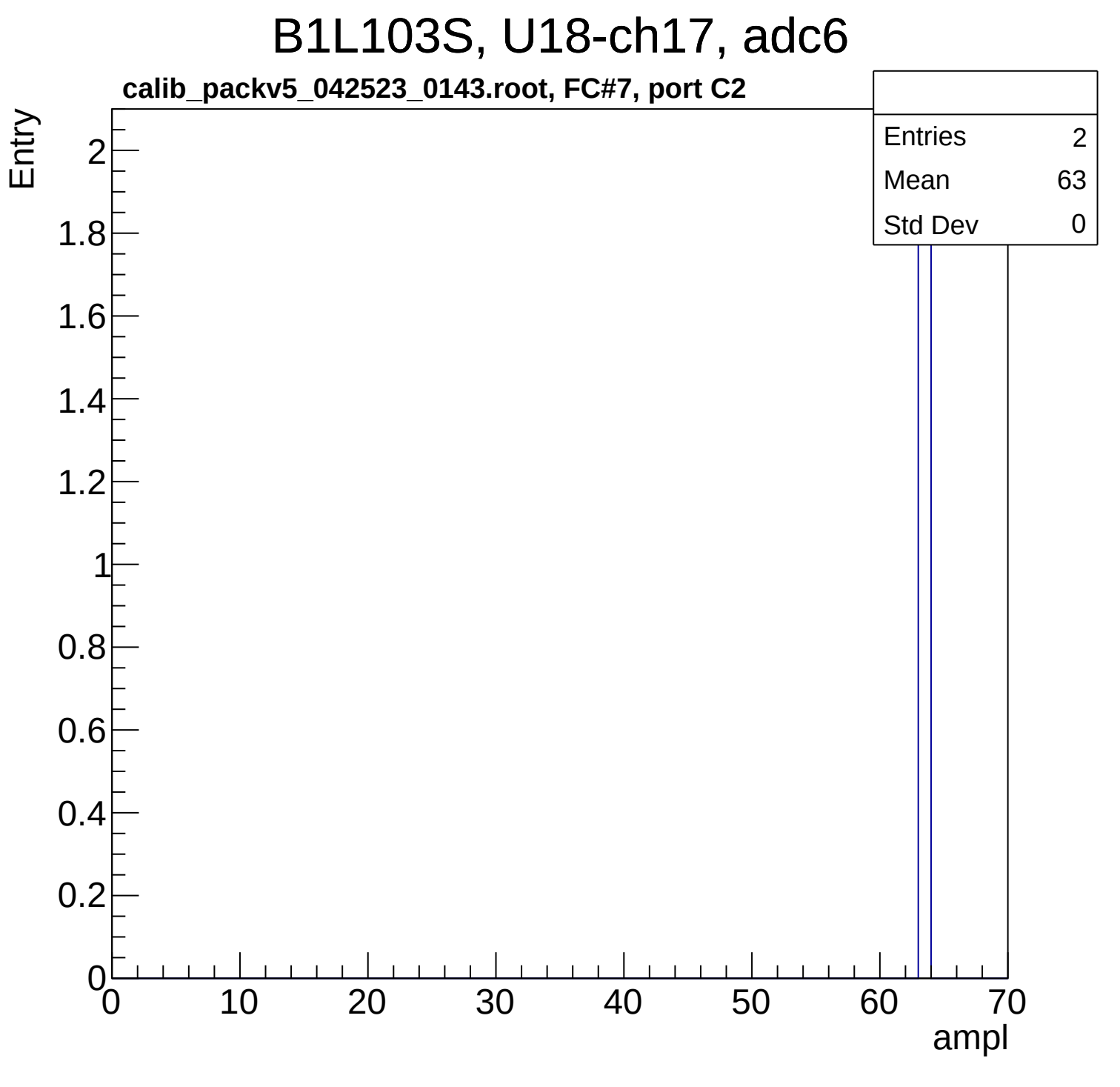

B1L103S, U18-ch17, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 38.75
Std Dev 3.663
Gaus mean : 38.7905
Gaus Width: 4.2668
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

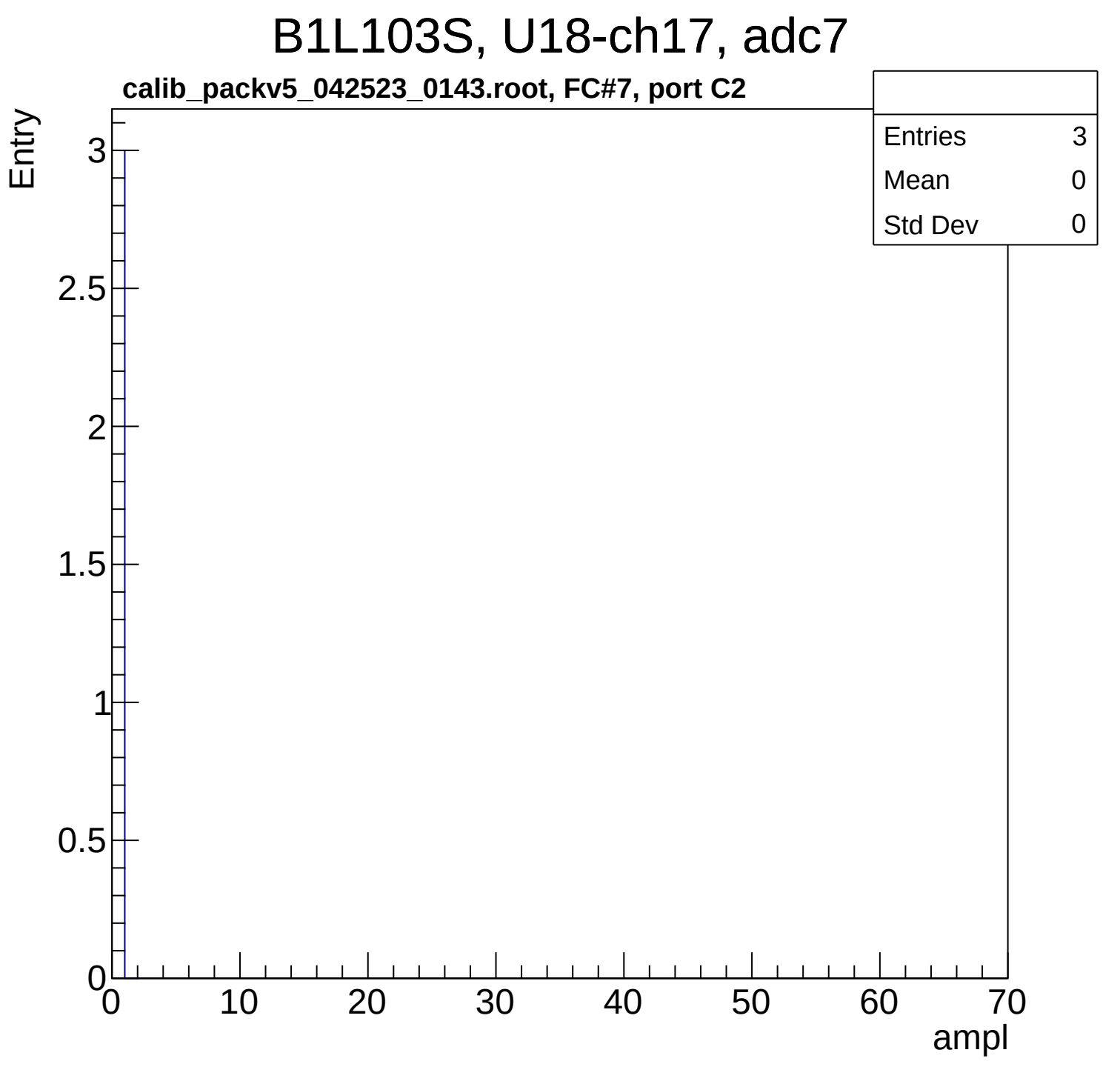

B1L103S, U18-ch17, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 43.39
Std Dev 3.726
Gaus mean : 44.5717
Gaus Width: 4.0781
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

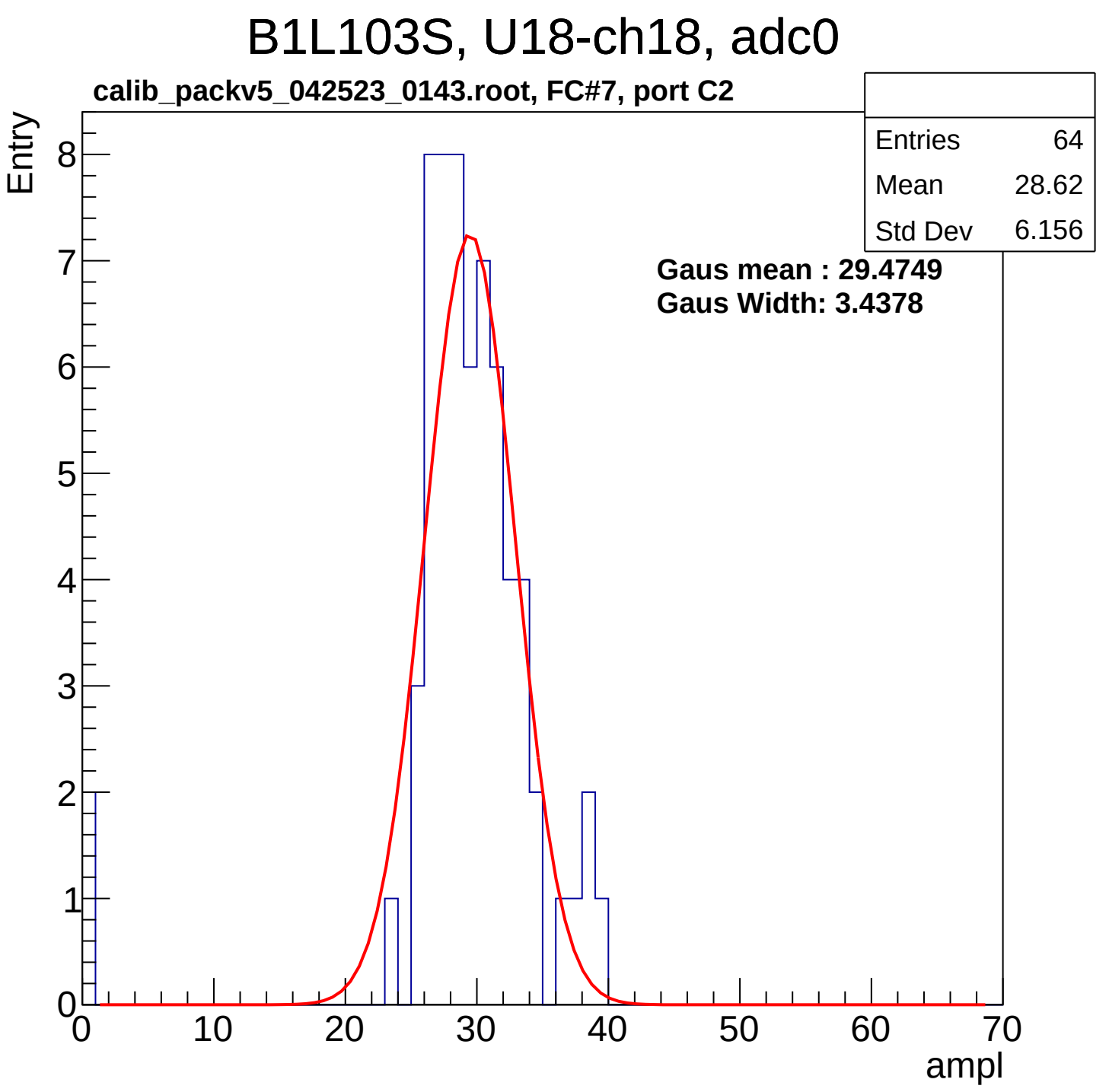

B1L103S, U18-ch17, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 86
Mean 51.33
Std Dev 3.847
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

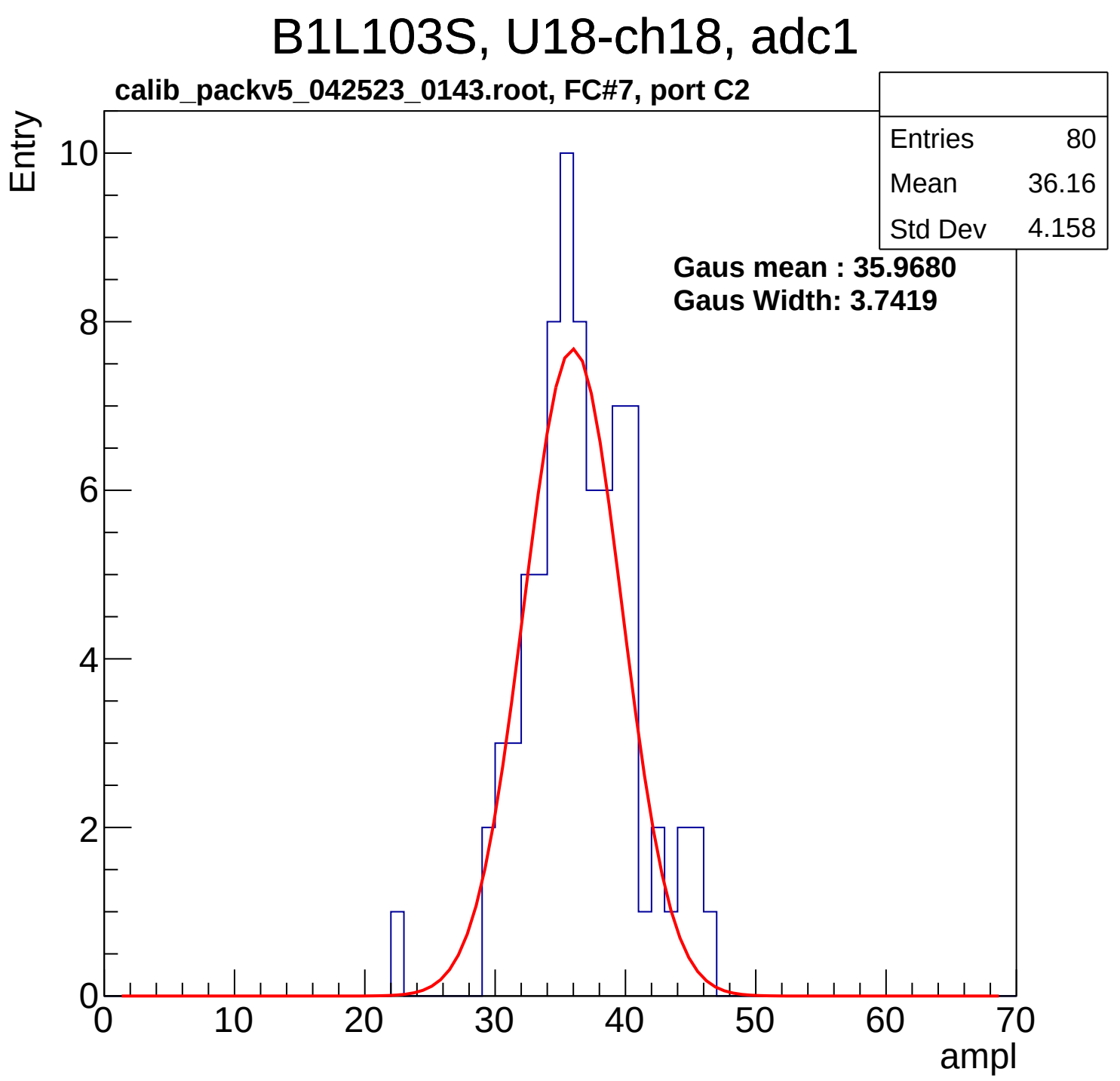

B1L103S, U18-ch17, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 48
Mean 57.85
Std Dev 2.986
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

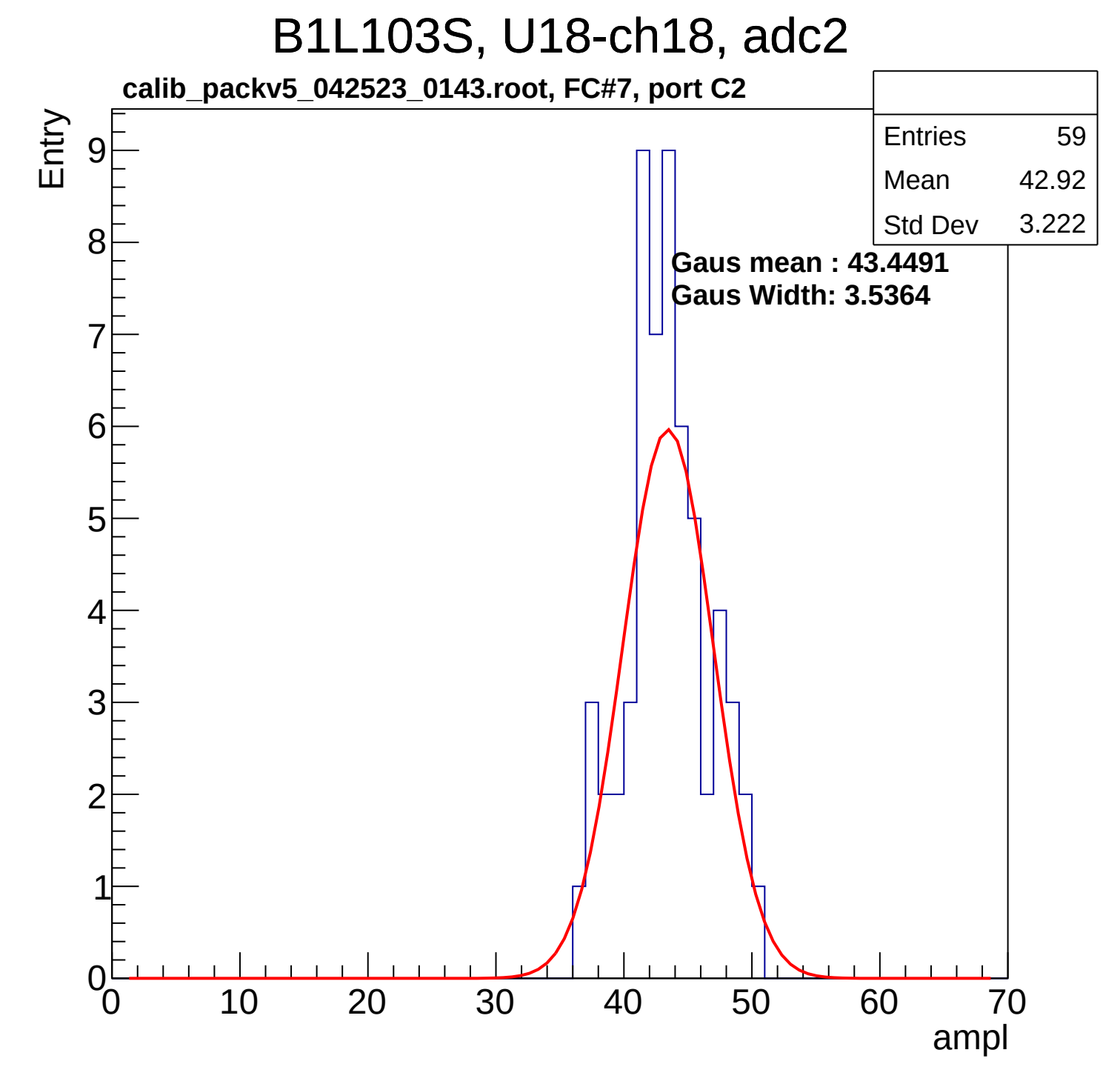

B1L103S, U18-ch17, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 30
Mean 58.67
Std Dev 11.06
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch17, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 63
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U18-ch17, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 0
Std Dev 0
Entry
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch18, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 28.62
Std Dev 6.156
Gaus mean : 29.4749
Gaus Width: 3.4378
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch18, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 80
Mean 36.16
Std Dev 4.158
Gaus mean : 35.9680
Gaus Width: 3.7419
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch18, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 42.92
Std Dev 3.222
Gaus mean : 43.4491
Gaus Width: 3.5364
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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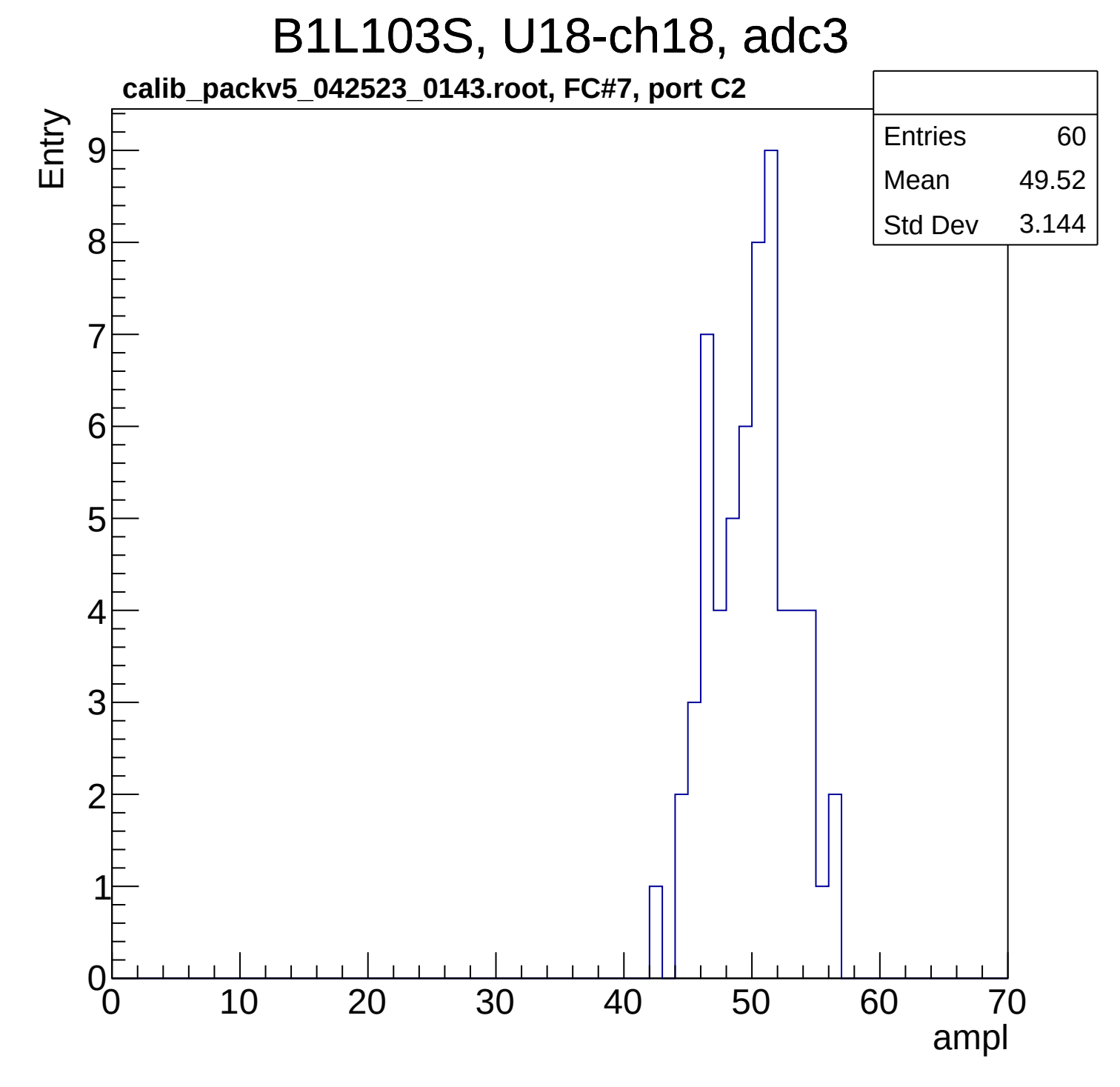
B1L103S, U18-ch18, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 60
Mean 49.52
Std Dev 3.144
Entry
ampl
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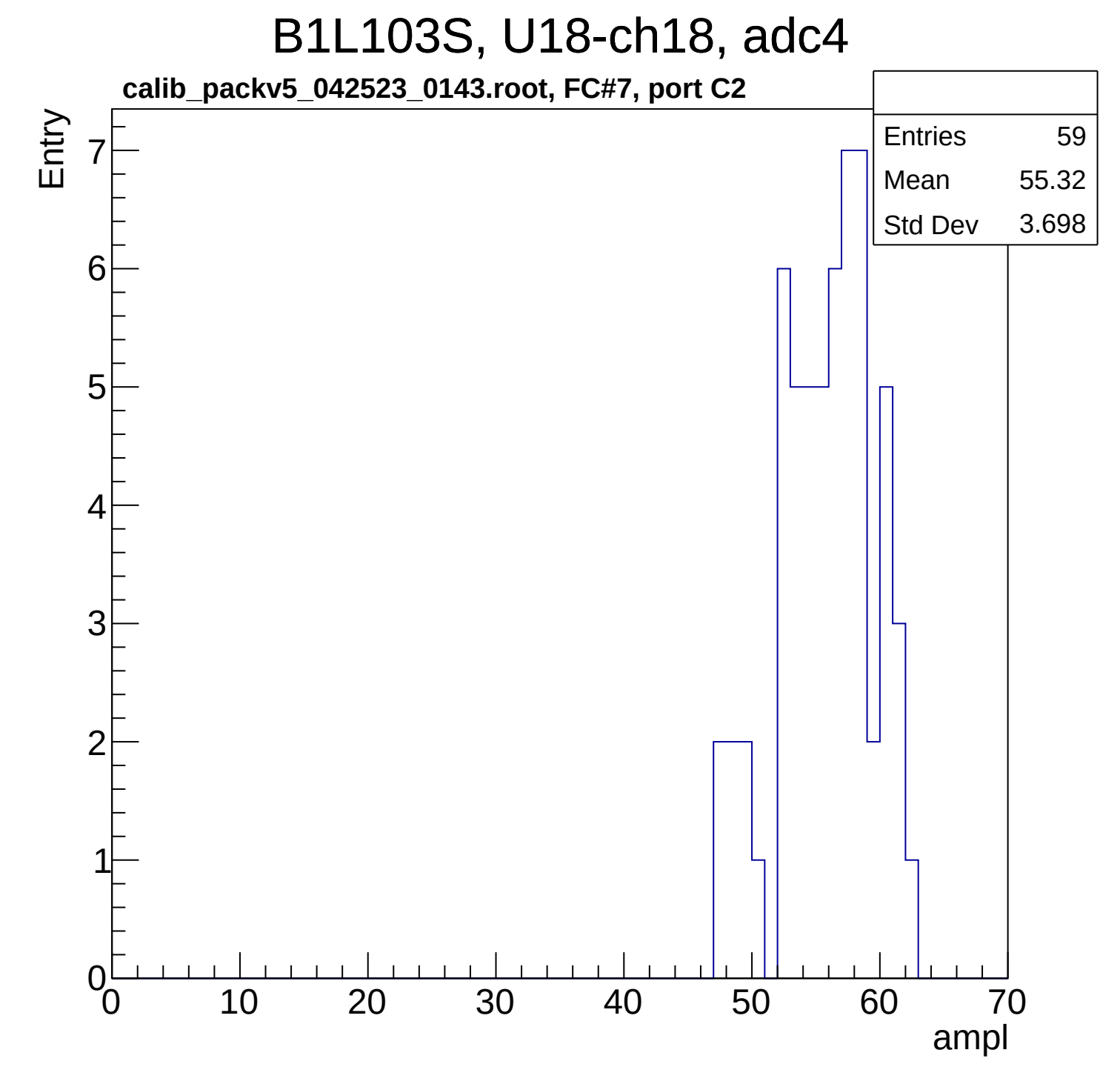
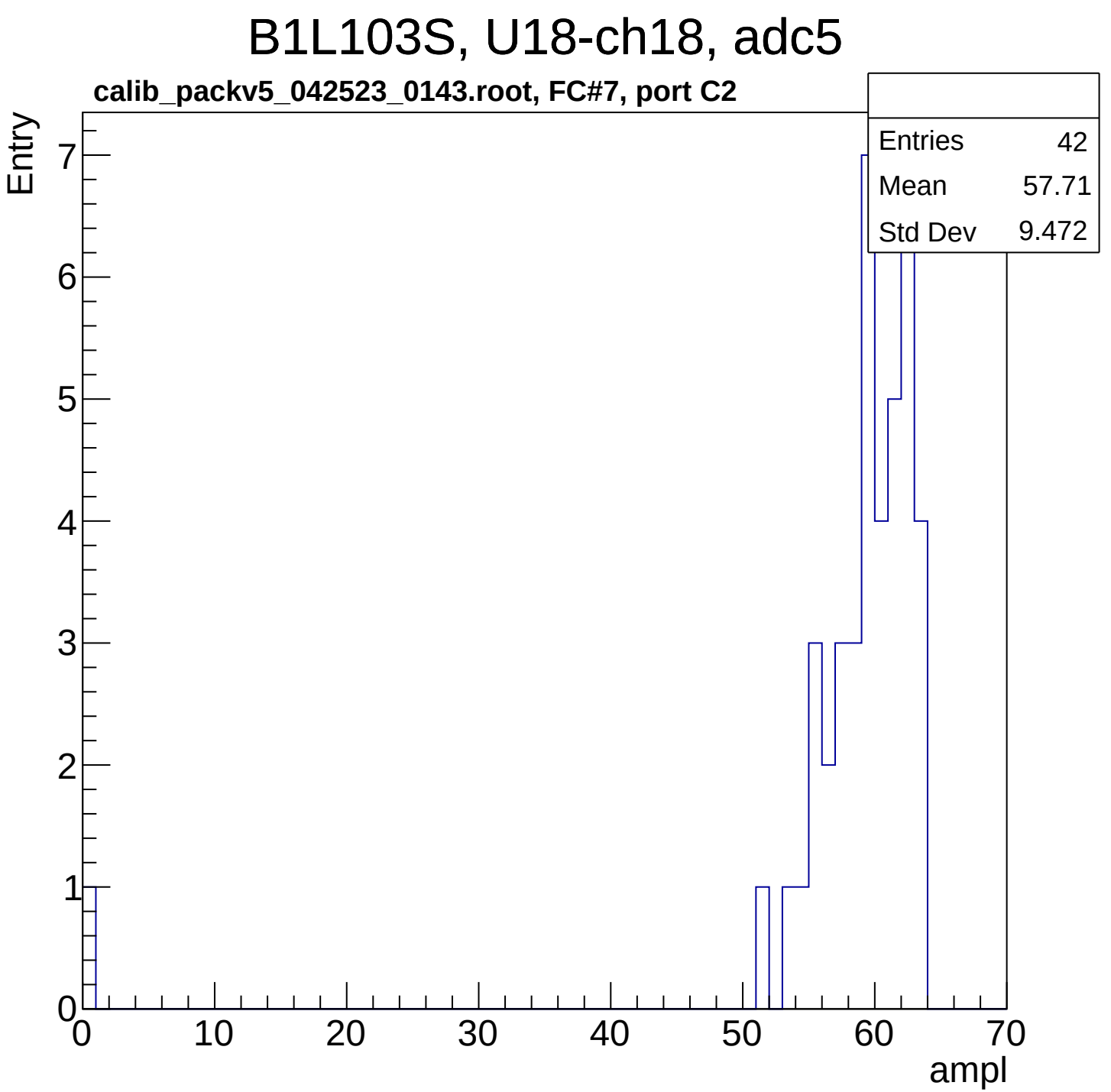
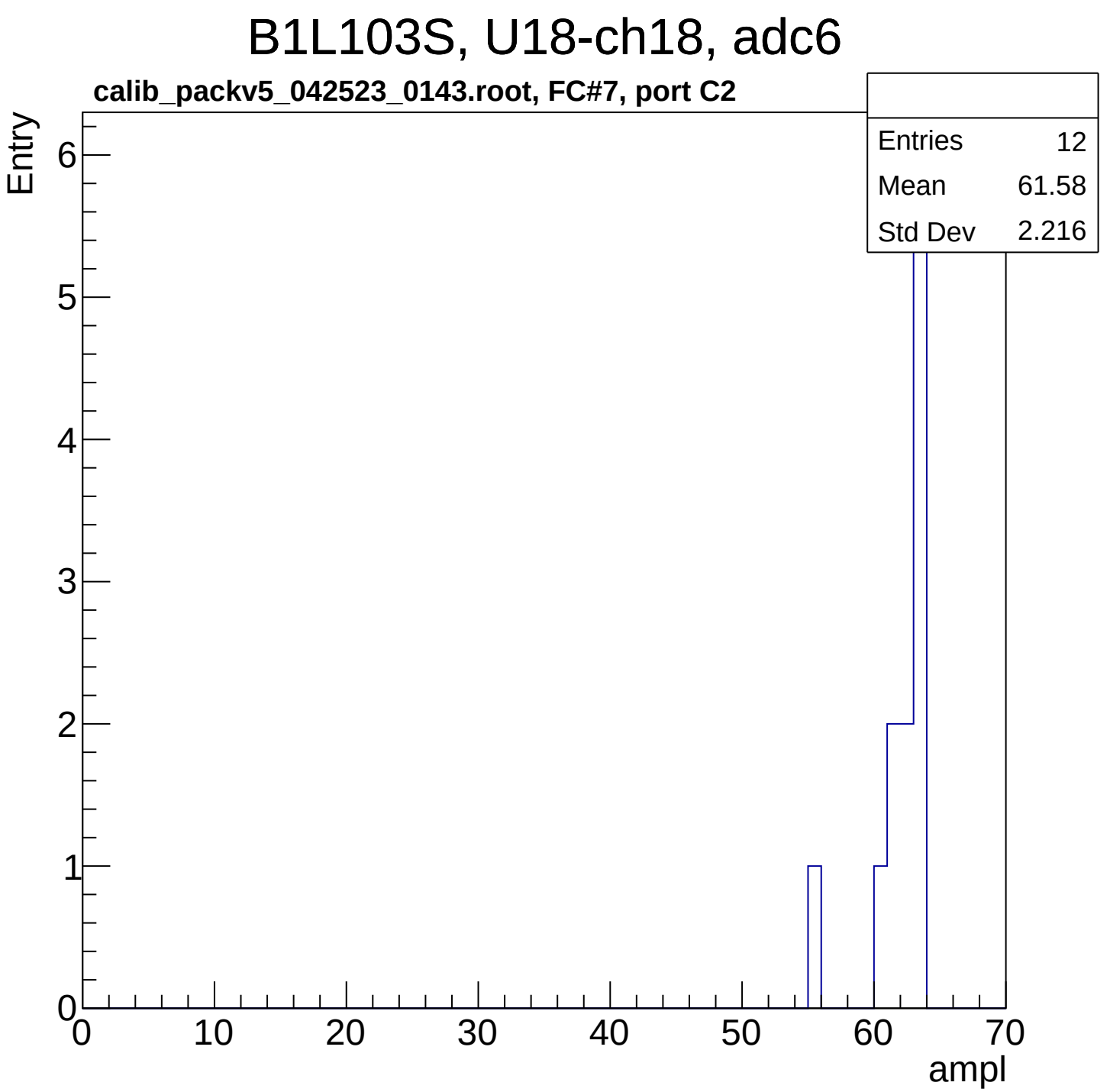
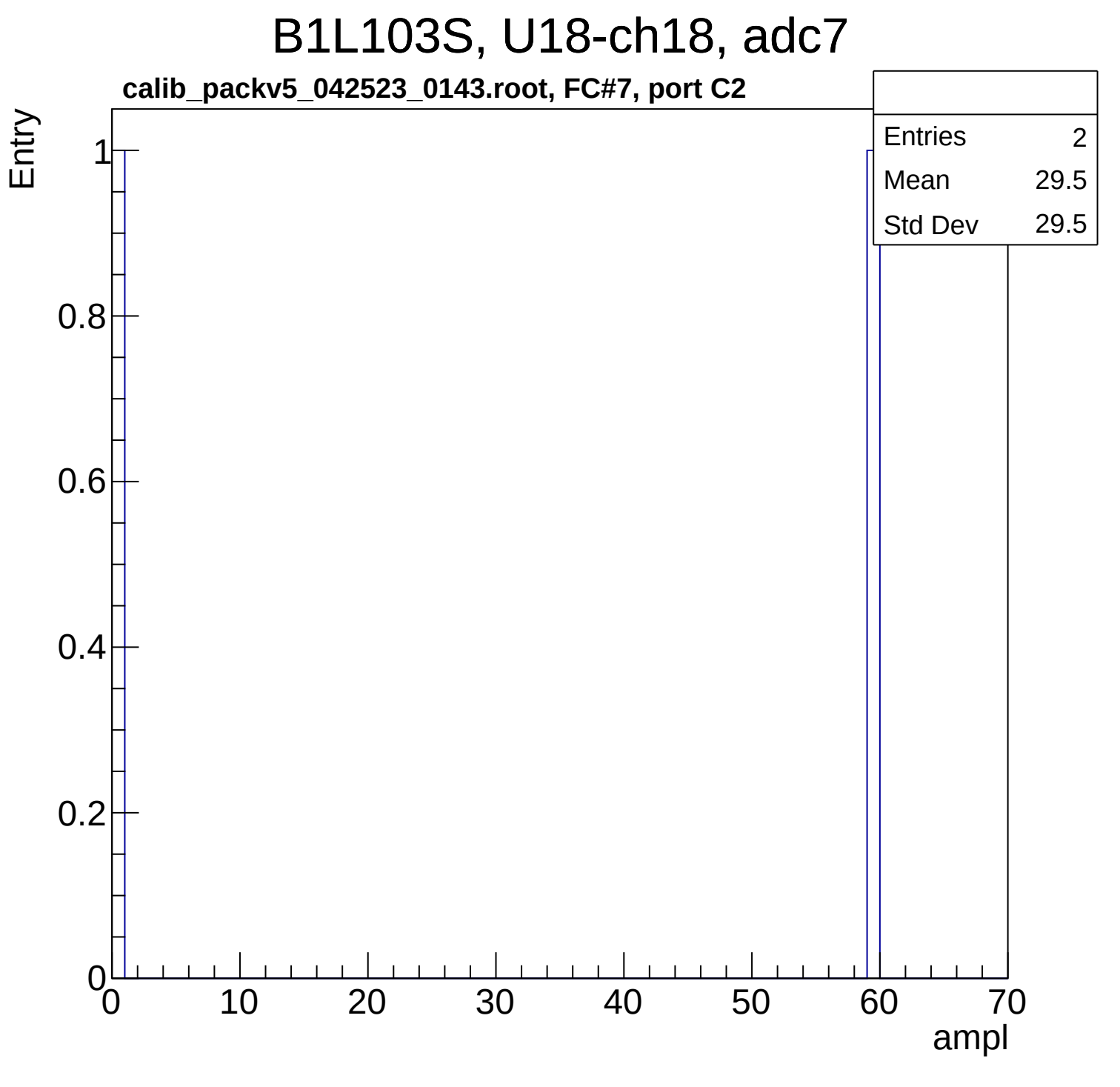
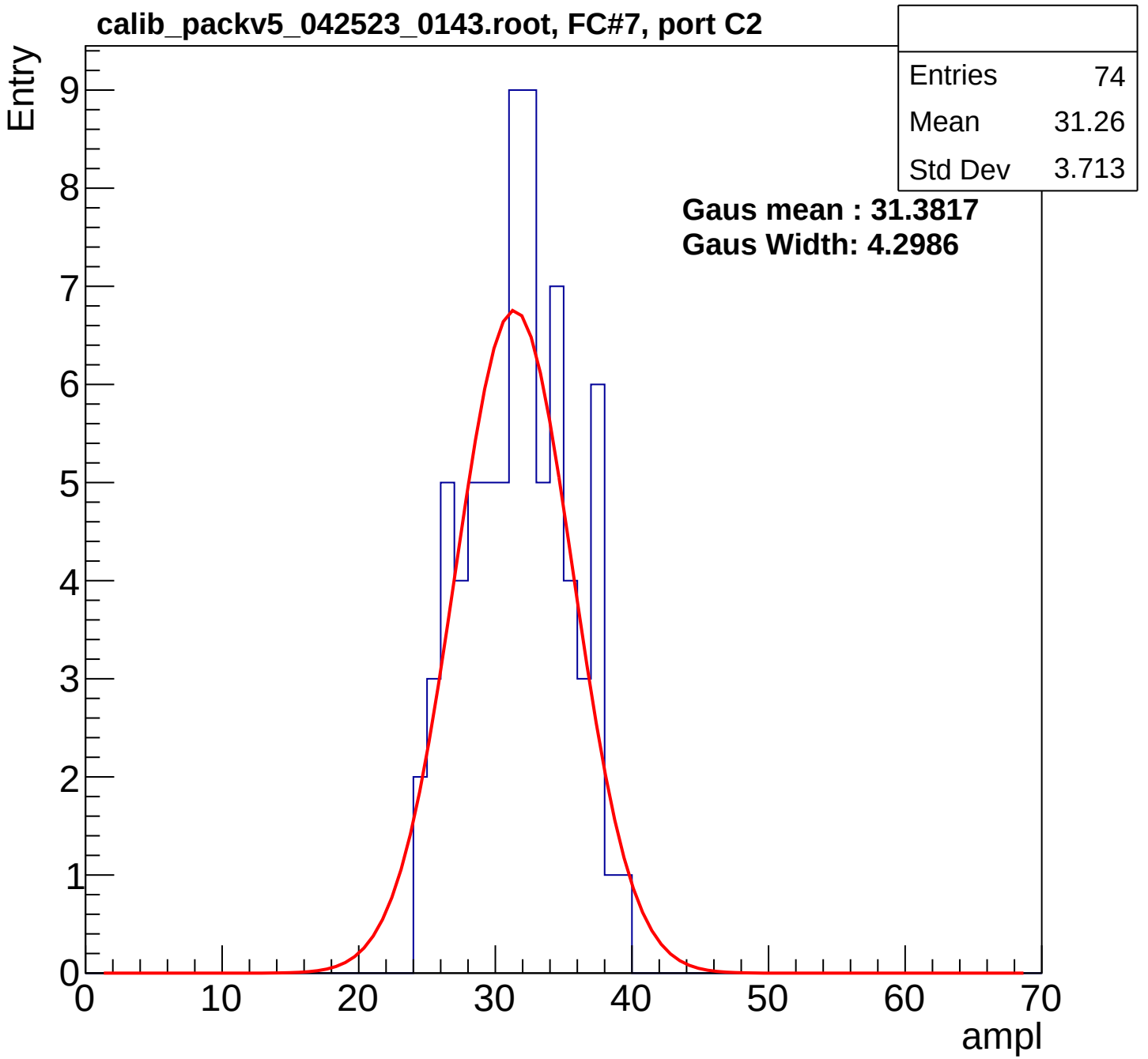
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch18, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 55.32
Std Dev 3.698
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch18, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 42
Mean 57.71
Std Dev 9.472
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch18, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 12
Mean 61.58
Std Dev 2.216
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch18, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 29.5
Std Dev 29.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch19, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 74
Mean 31.26
Std Dev 3.713
Gaus mean : 31.3817
Gaus Width: 4.2986
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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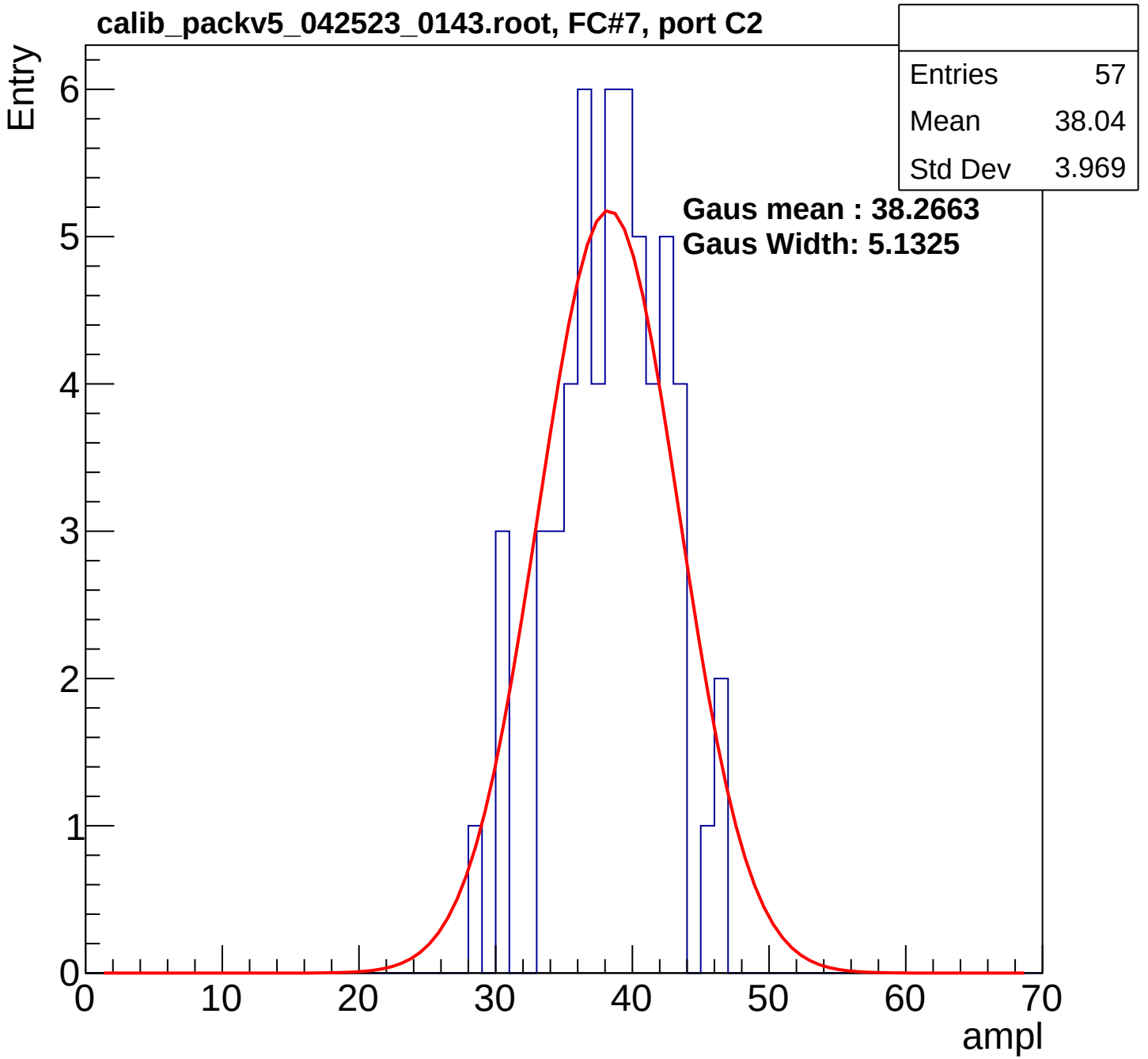
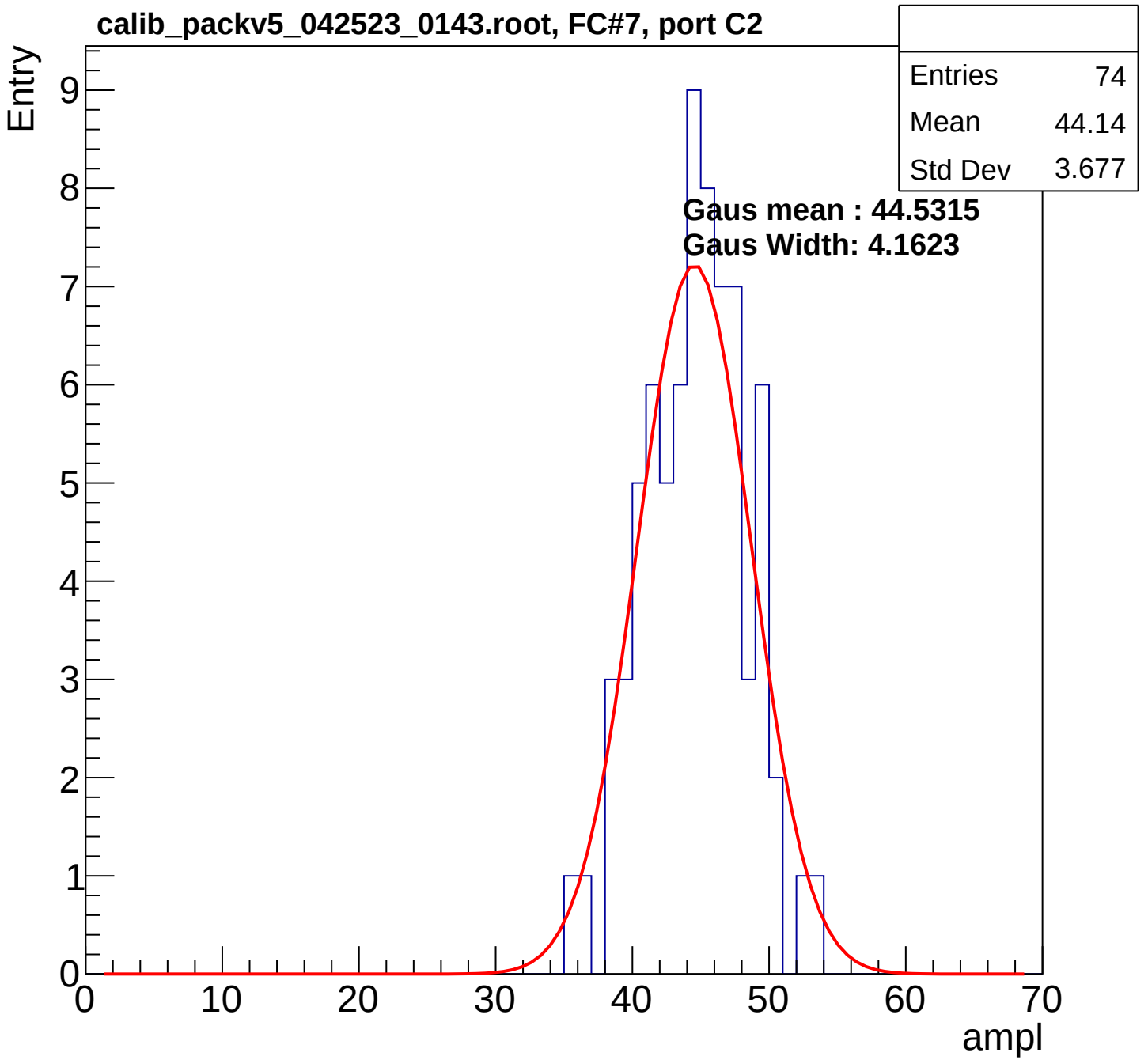

B1L103S, U18-ch19, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 38.04
Std Dev 3.969
Gaus mean : 38.2663
Gaus Width: 5.1325
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U18-ch19, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 74
Mean 44.14
Std Dev 3.677
Gaus mean : 44.5315
Gaus Width: 4.1623
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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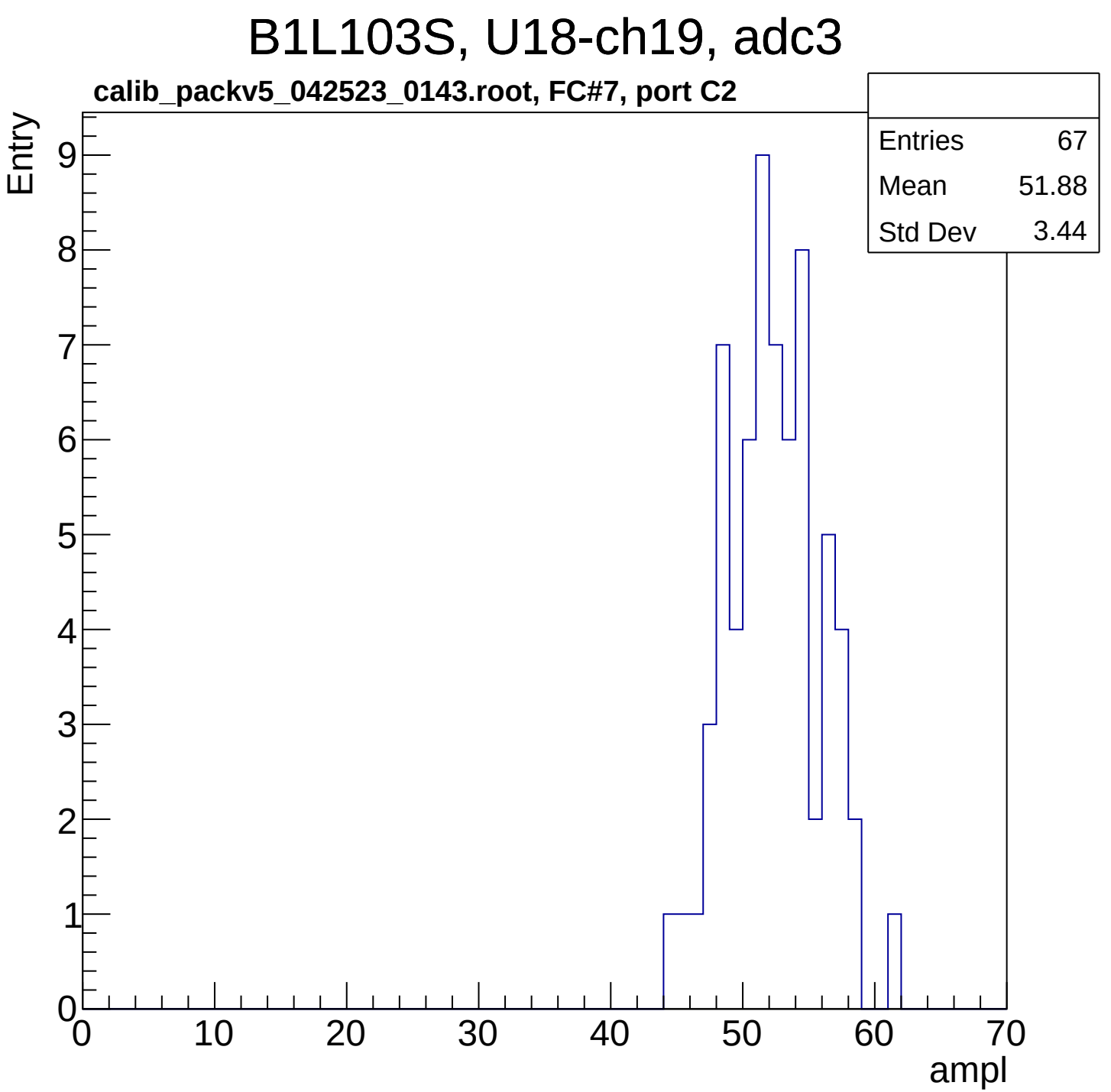
B1L103S, U18-ch19, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 51.88
Std Dev 3.44
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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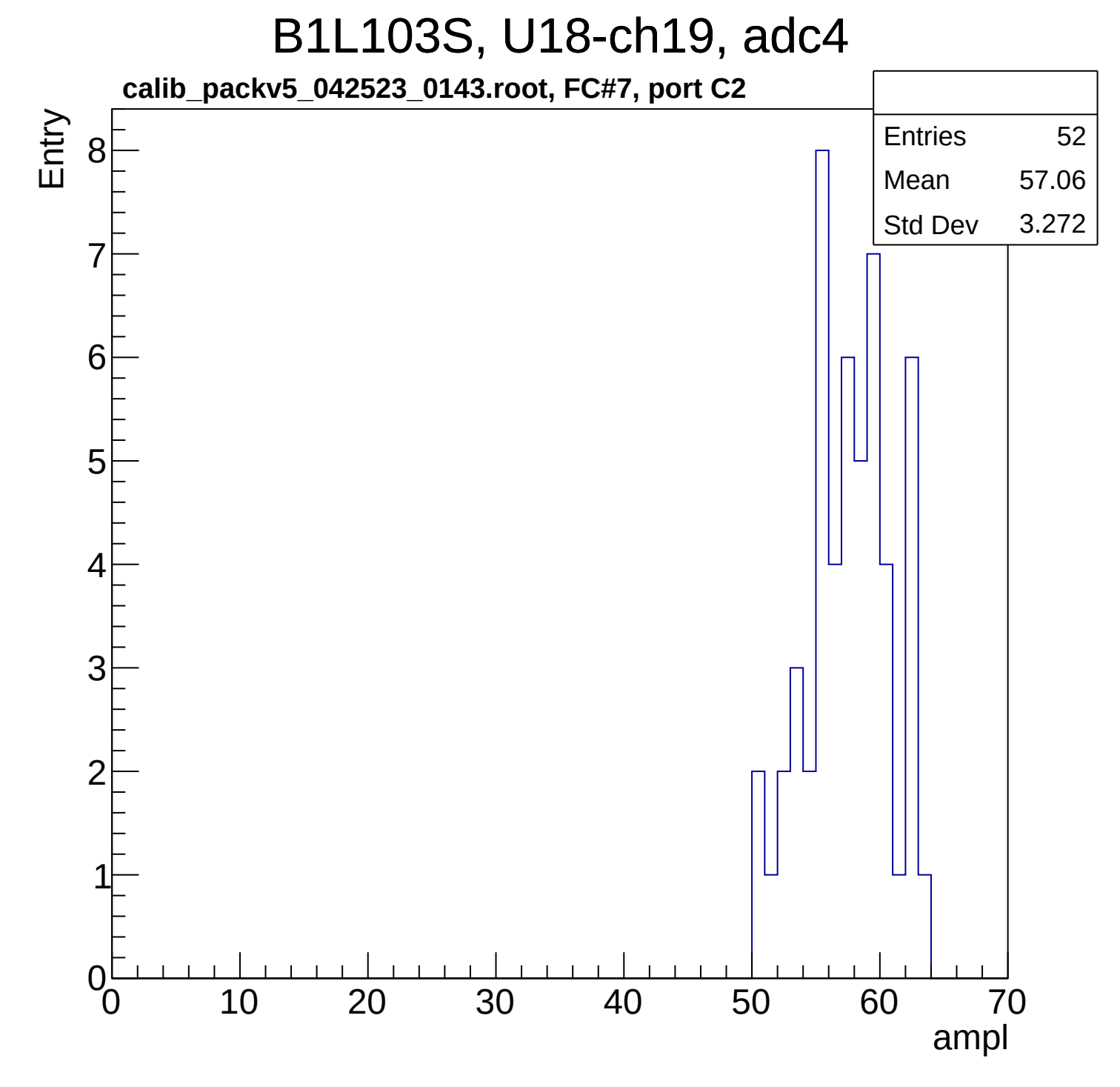
B1L103S, U18-ch19, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 52
Mean 57.06
Std Dev 3.272
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
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60
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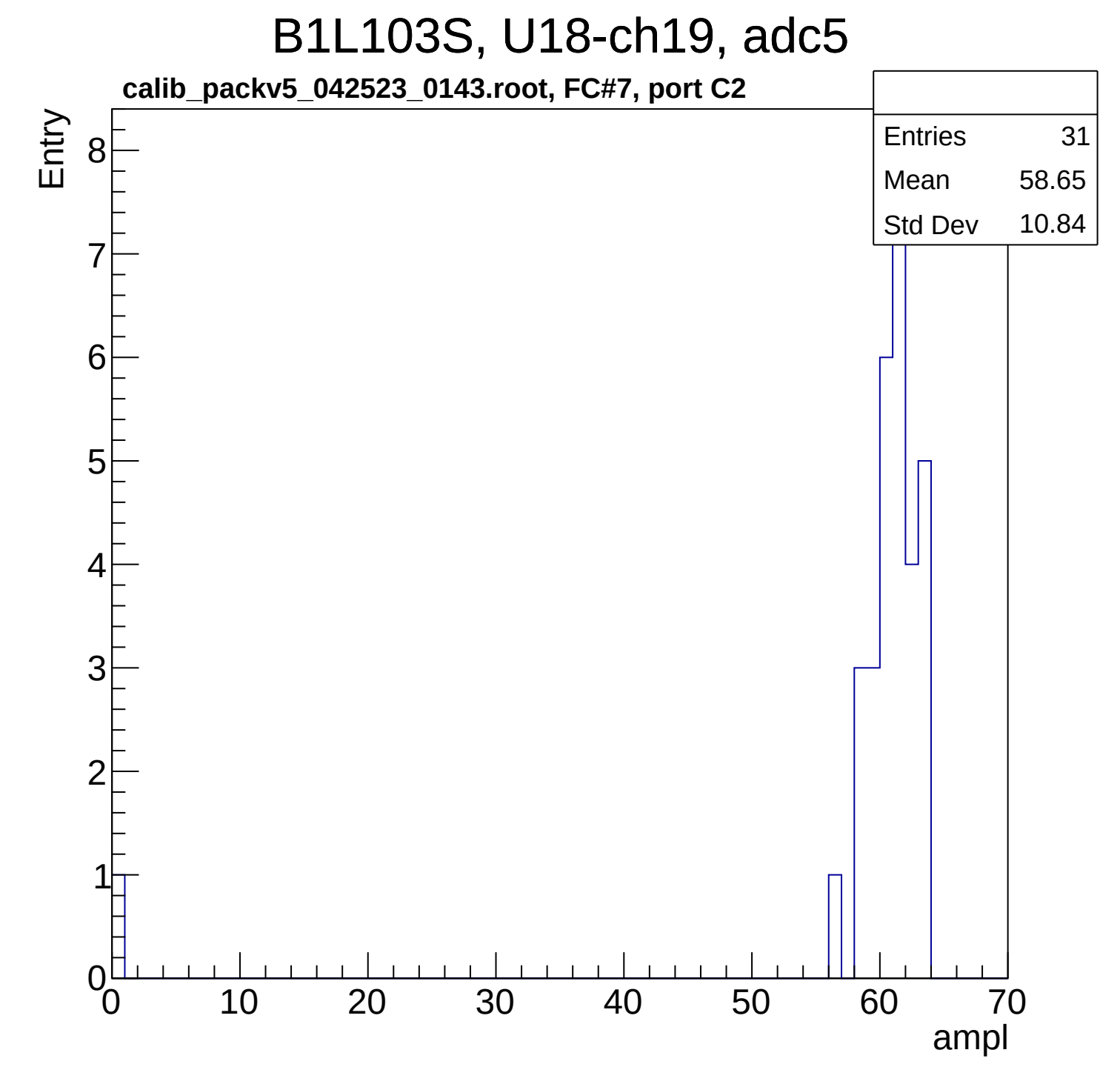
B1L103S, U18-ch19, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 31
Mean 58.65
Std Dev 10.84
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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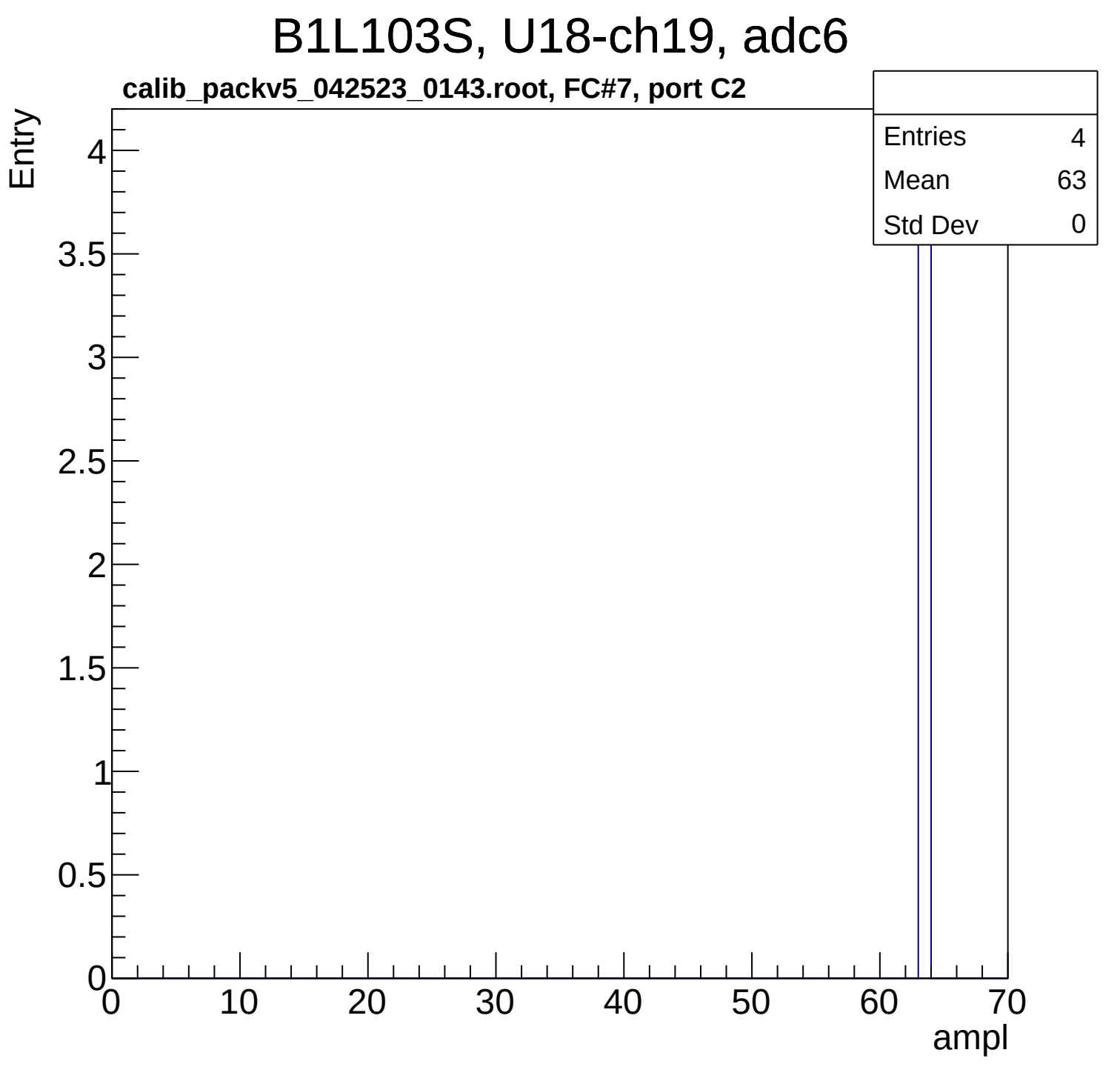
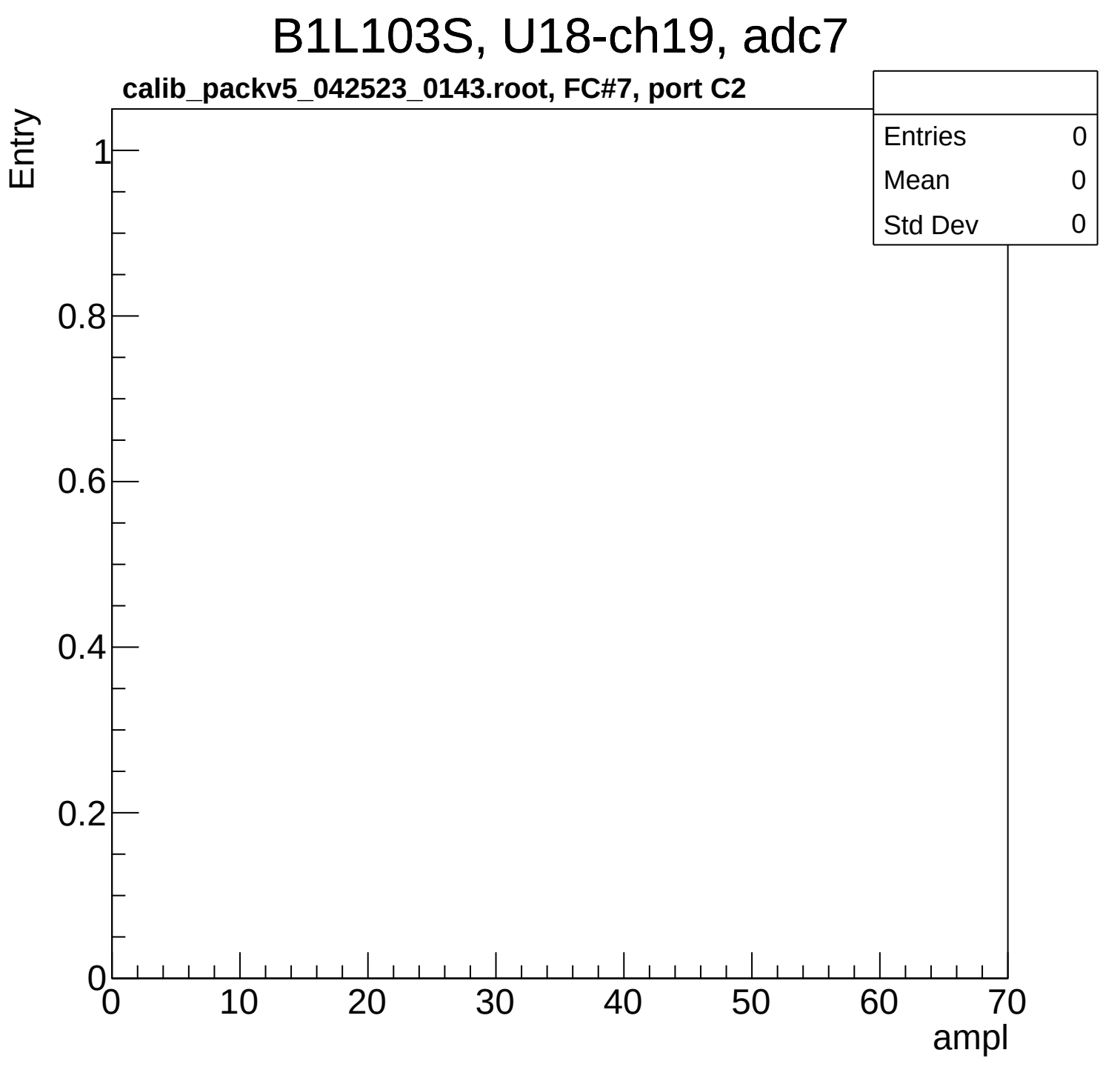
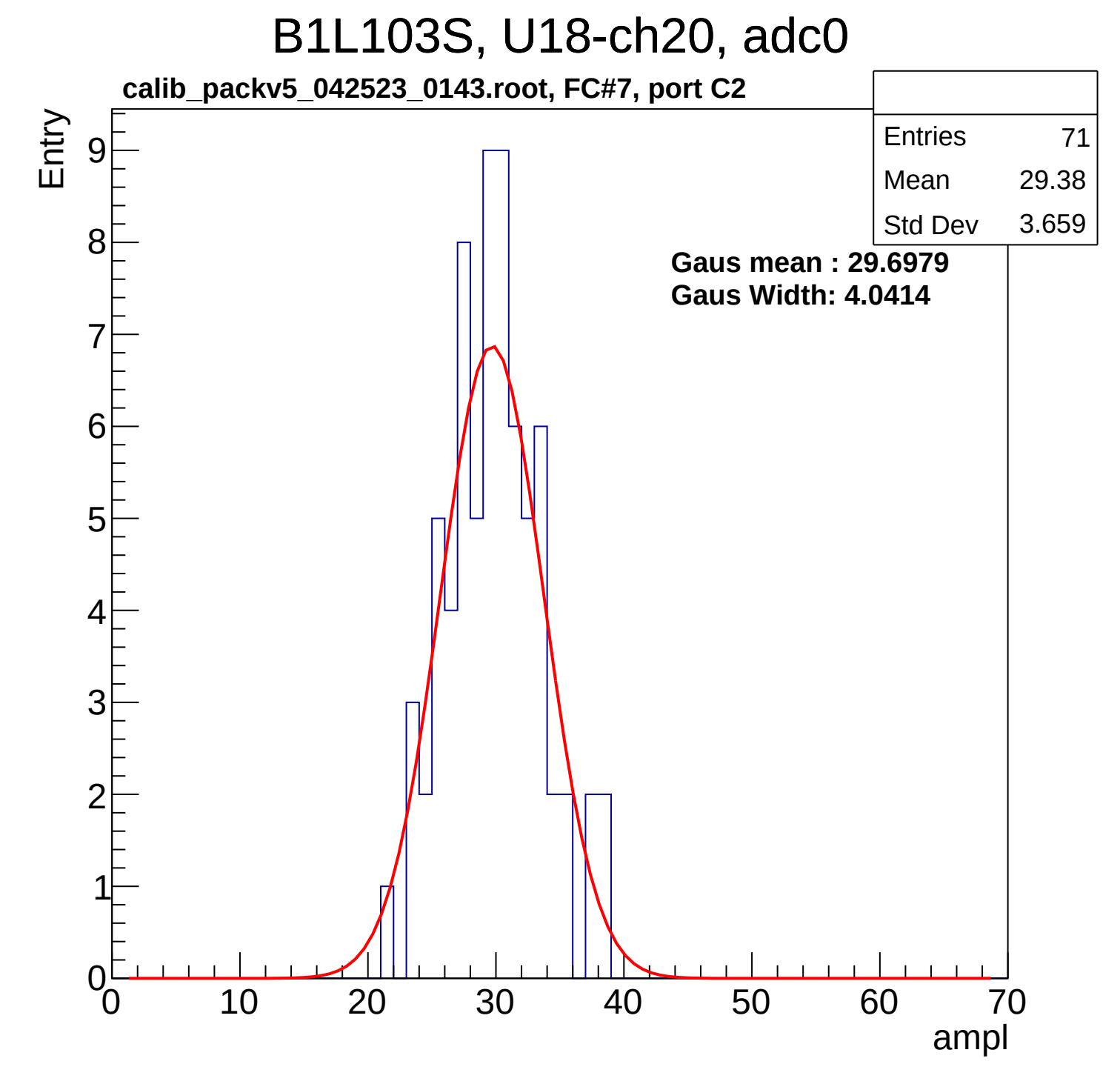

B1L103S, U18-ch19, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 4
Mean 63
Std Dev 0
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U18-ch19, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch20, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 71
Mean 29.38
Std Dev 3.659
Gaus mean : 29.6979
Gaus Width: 4.0414
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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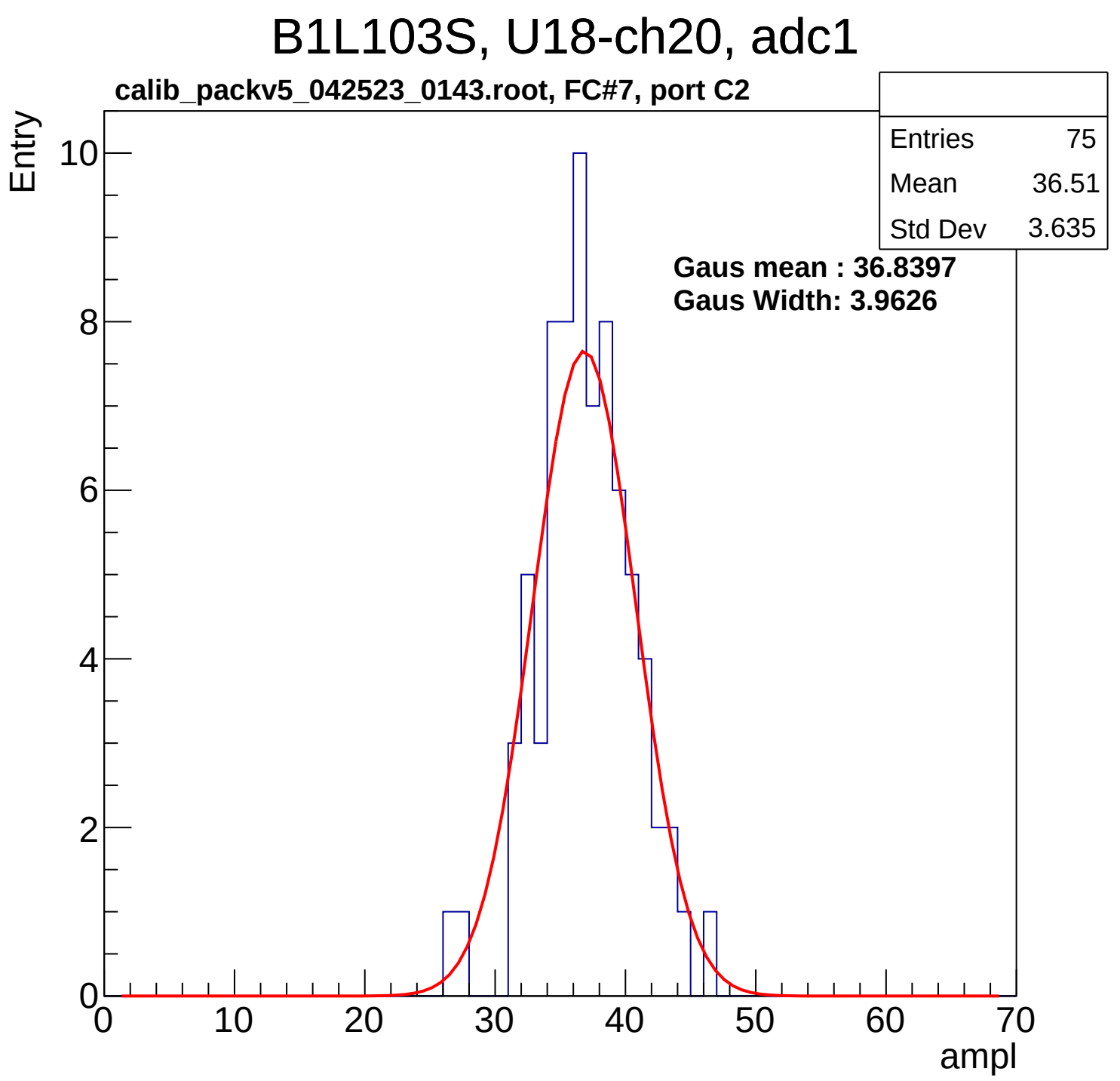
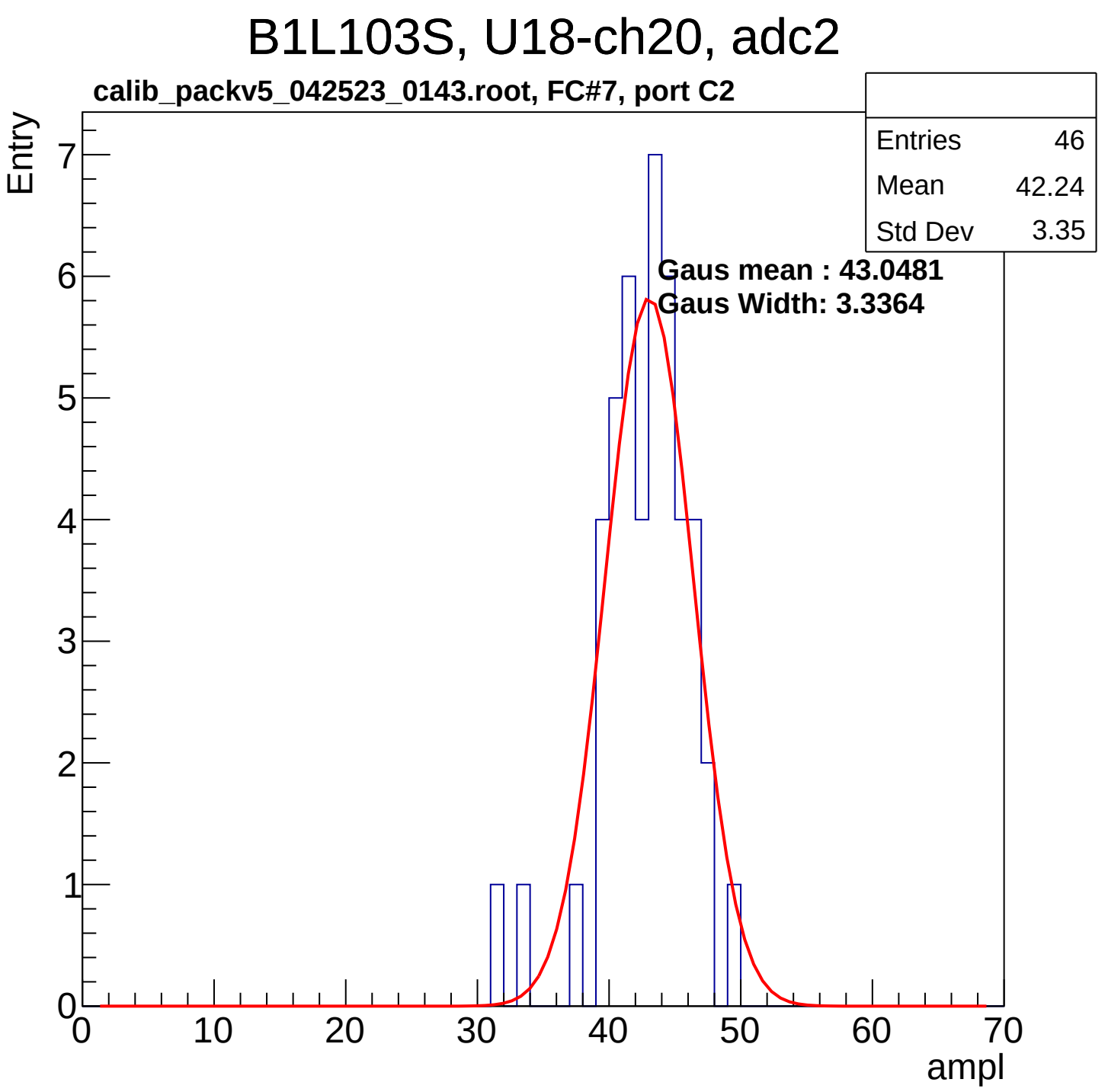

B1L103S, U18-ch20, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 75
Mean 36.51
Std Dev 3.635
Gaus mean : 36.8397
Gaus Width: 3.9626
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch20, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 46
Mean 42.24
Std Dev 3.35
Gaus mean : 43.0481
Gaus Width: 3.3364
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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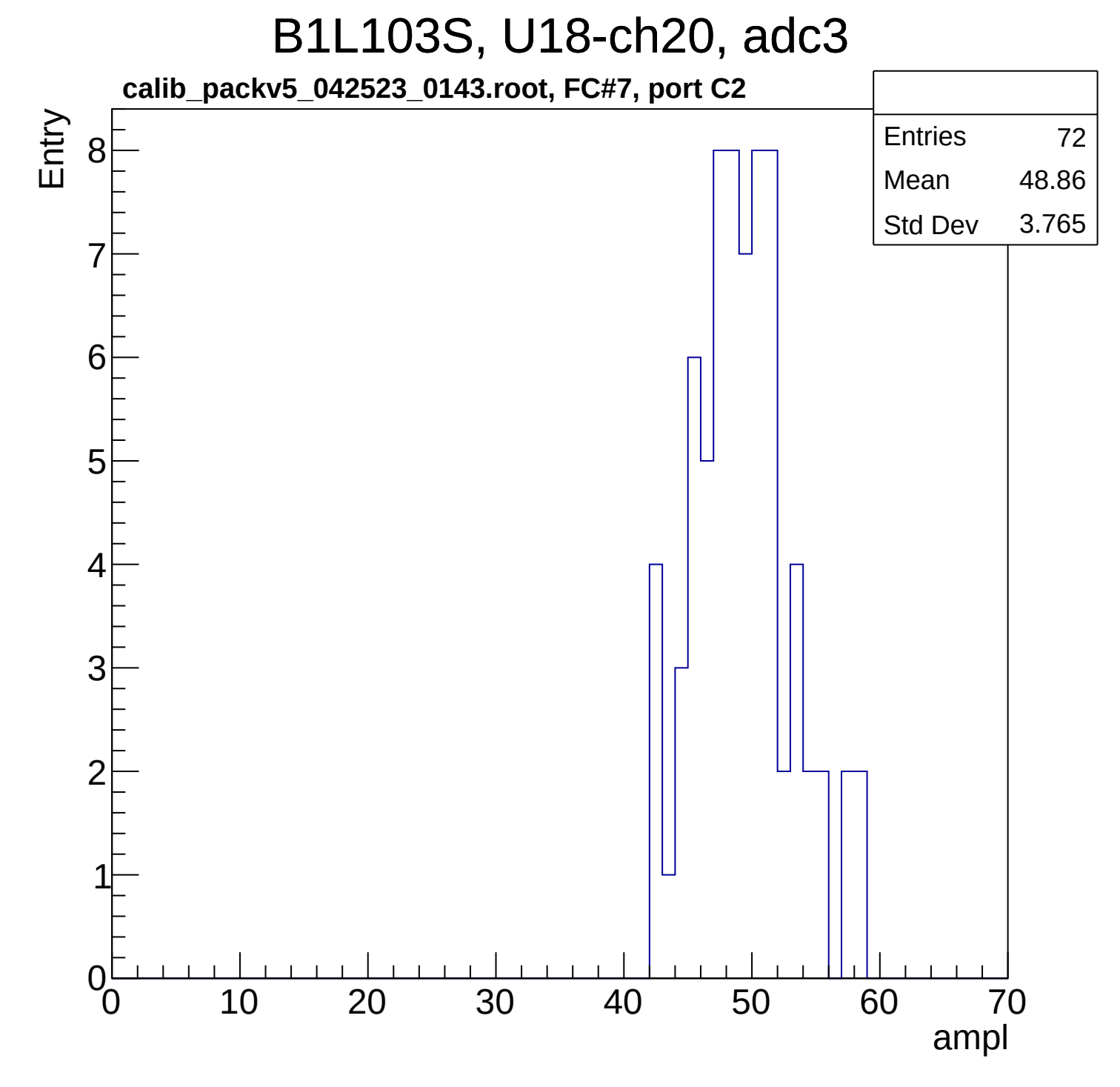
B1L103S, U18-ch20, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 72
Mean 48.86
Std Dev 3.765
Entry
ampl
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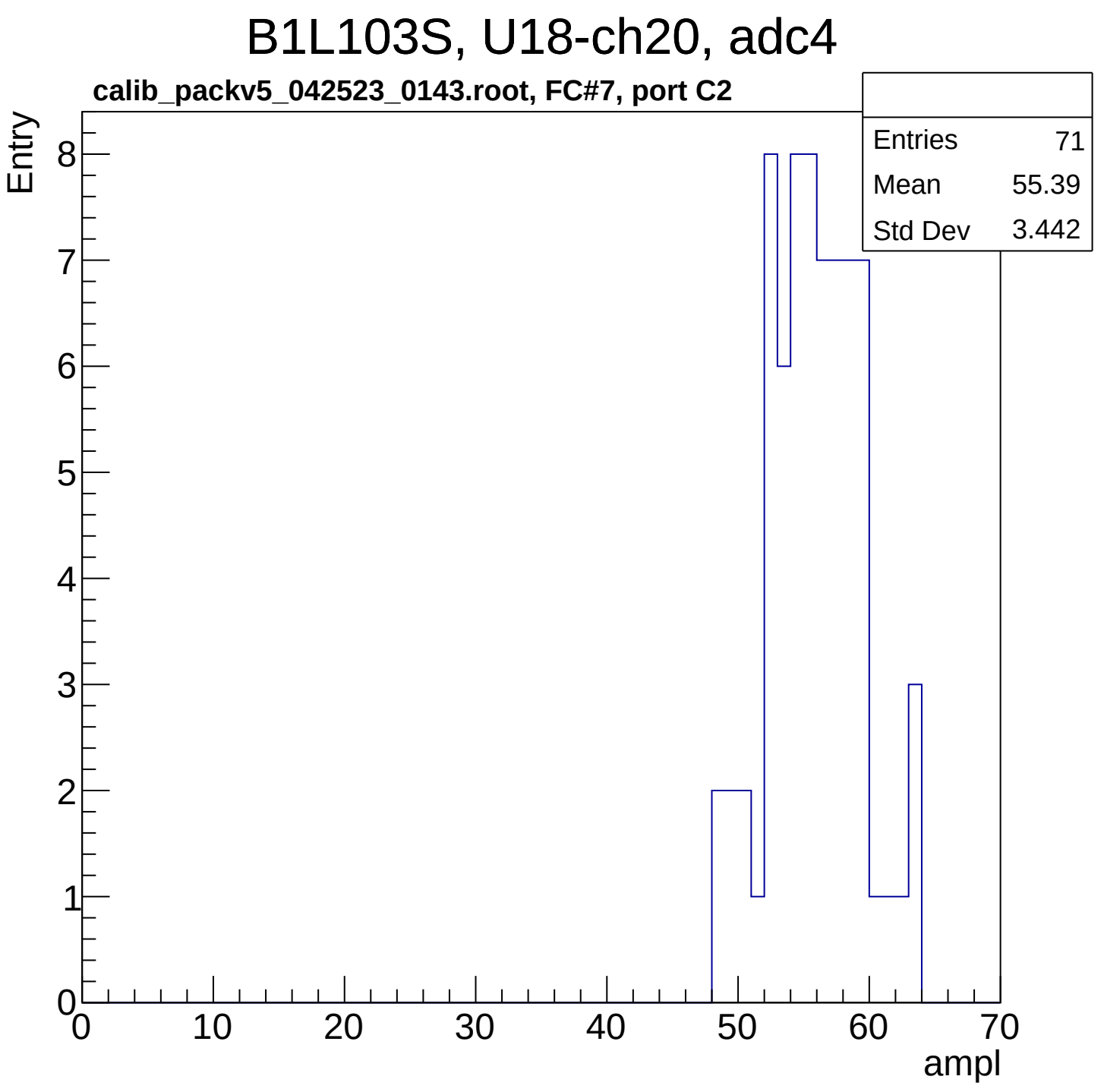
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch20, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 71
Mean 55.39
Std Dev 3.442
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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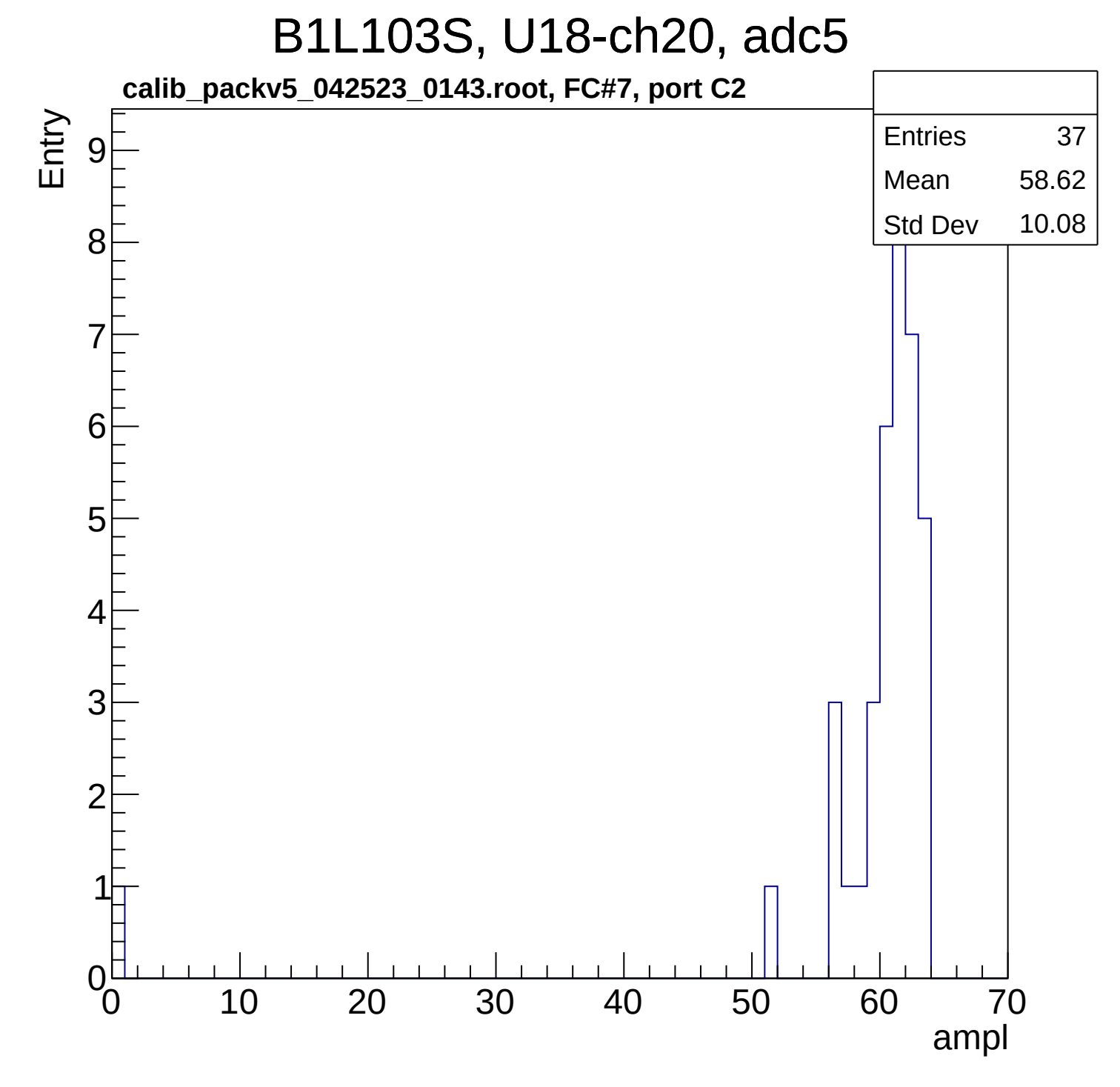
B1L103S, U18-ch20, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 37
Mean 58.62
Std Dev 10.08
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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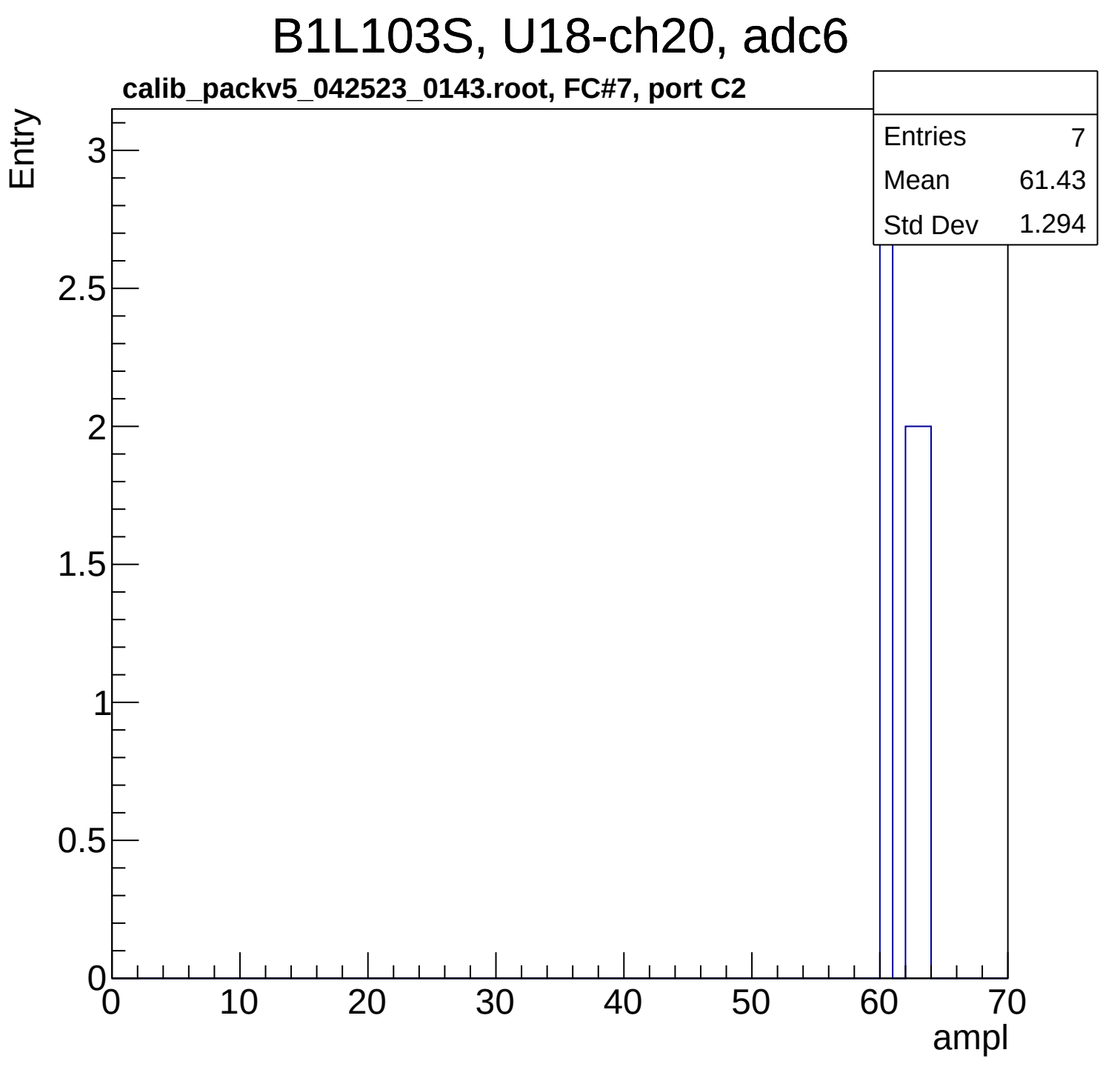
B1L103S, U18-ch20, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 7
Mean 61.43
Std Dev 1.294
Entry
ampl
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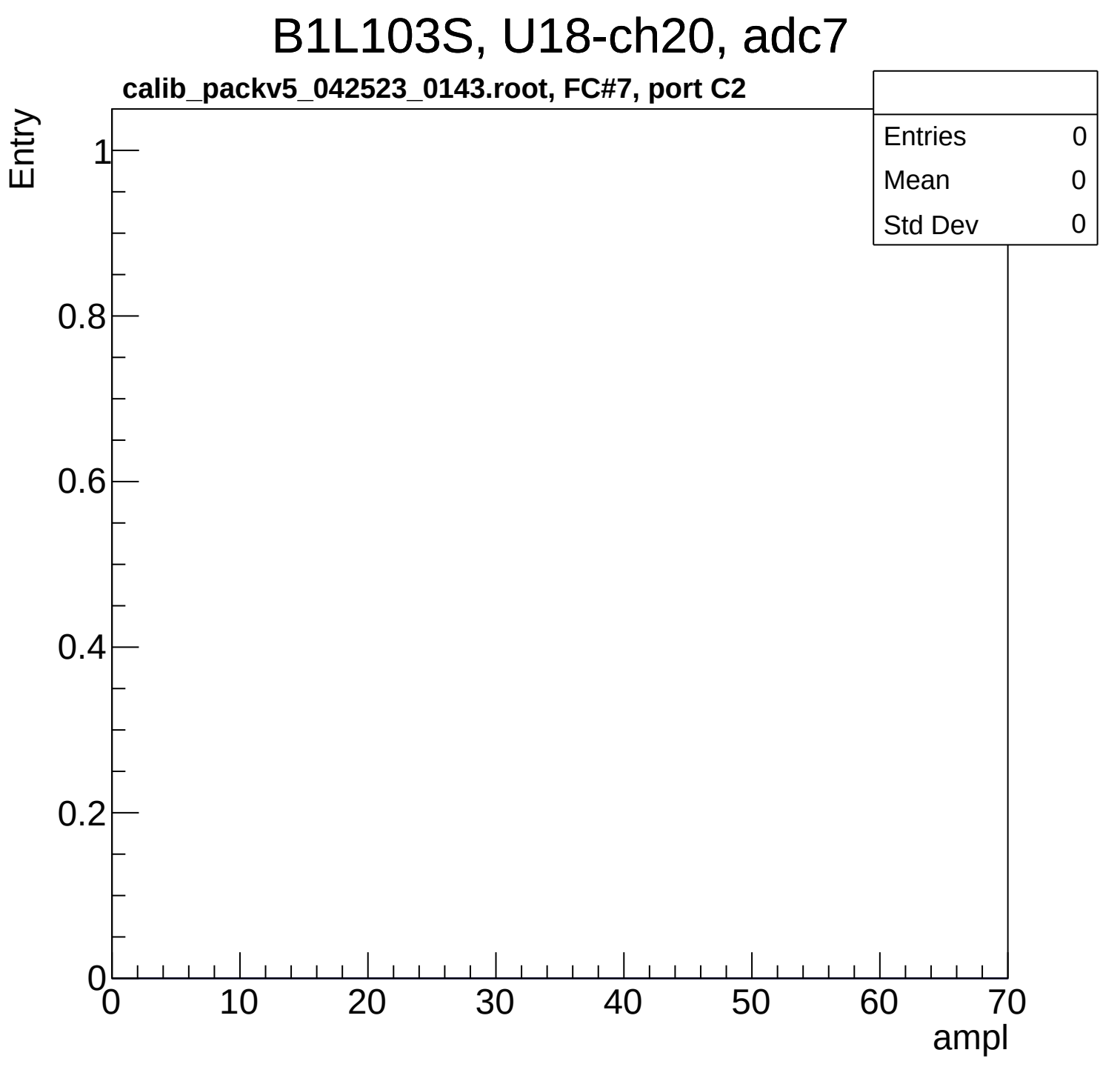
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U18-ch20, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
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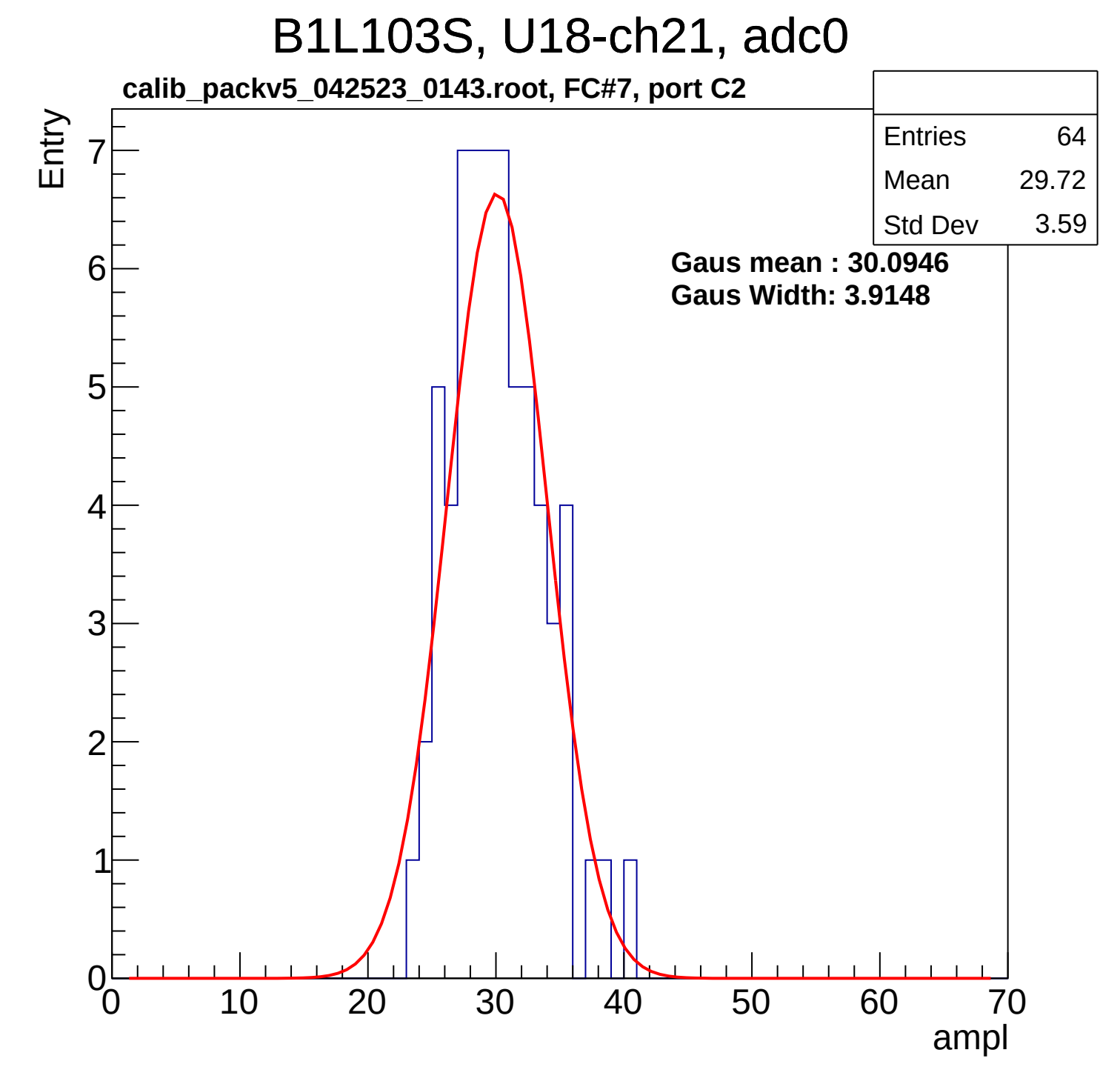
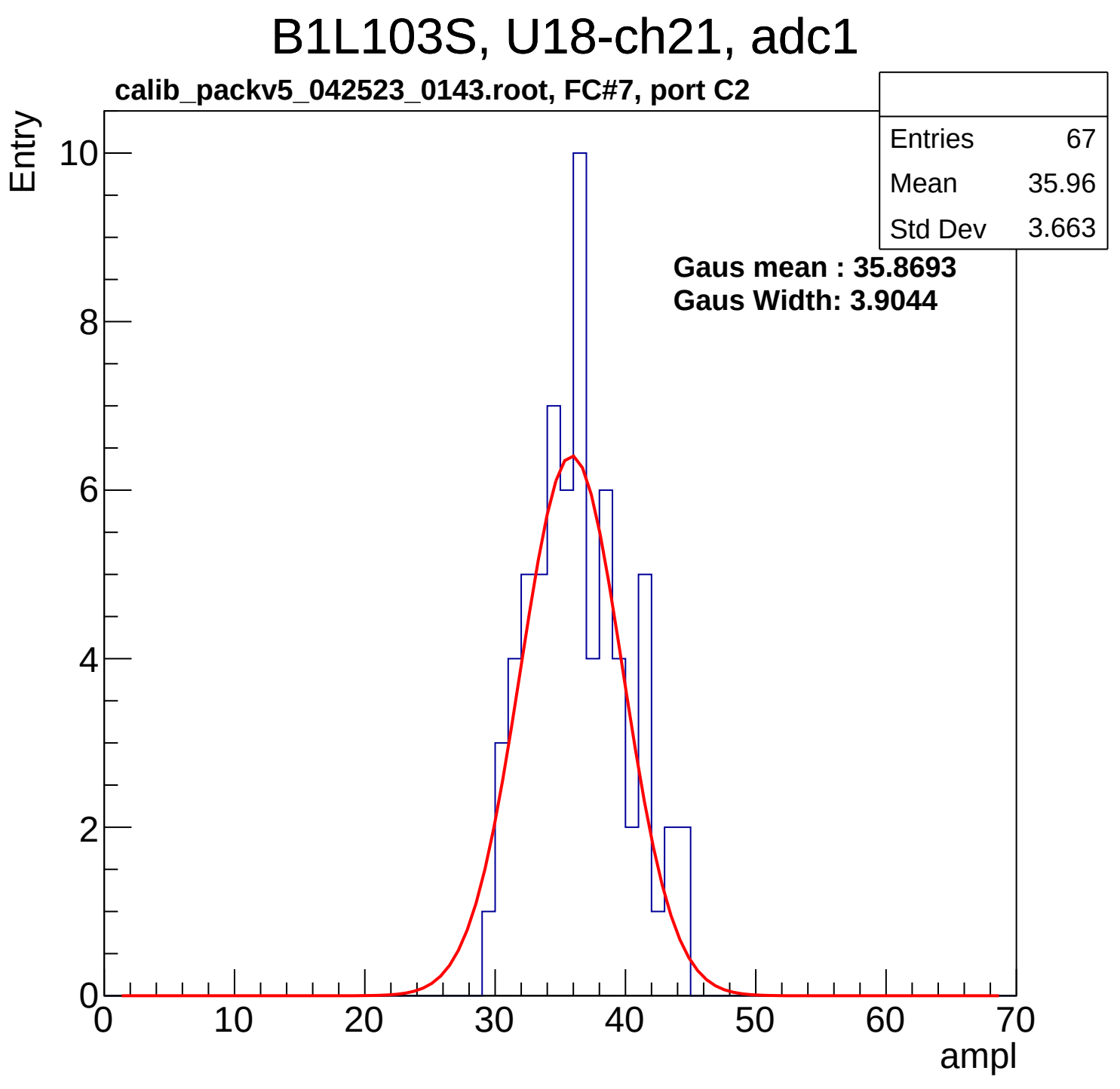
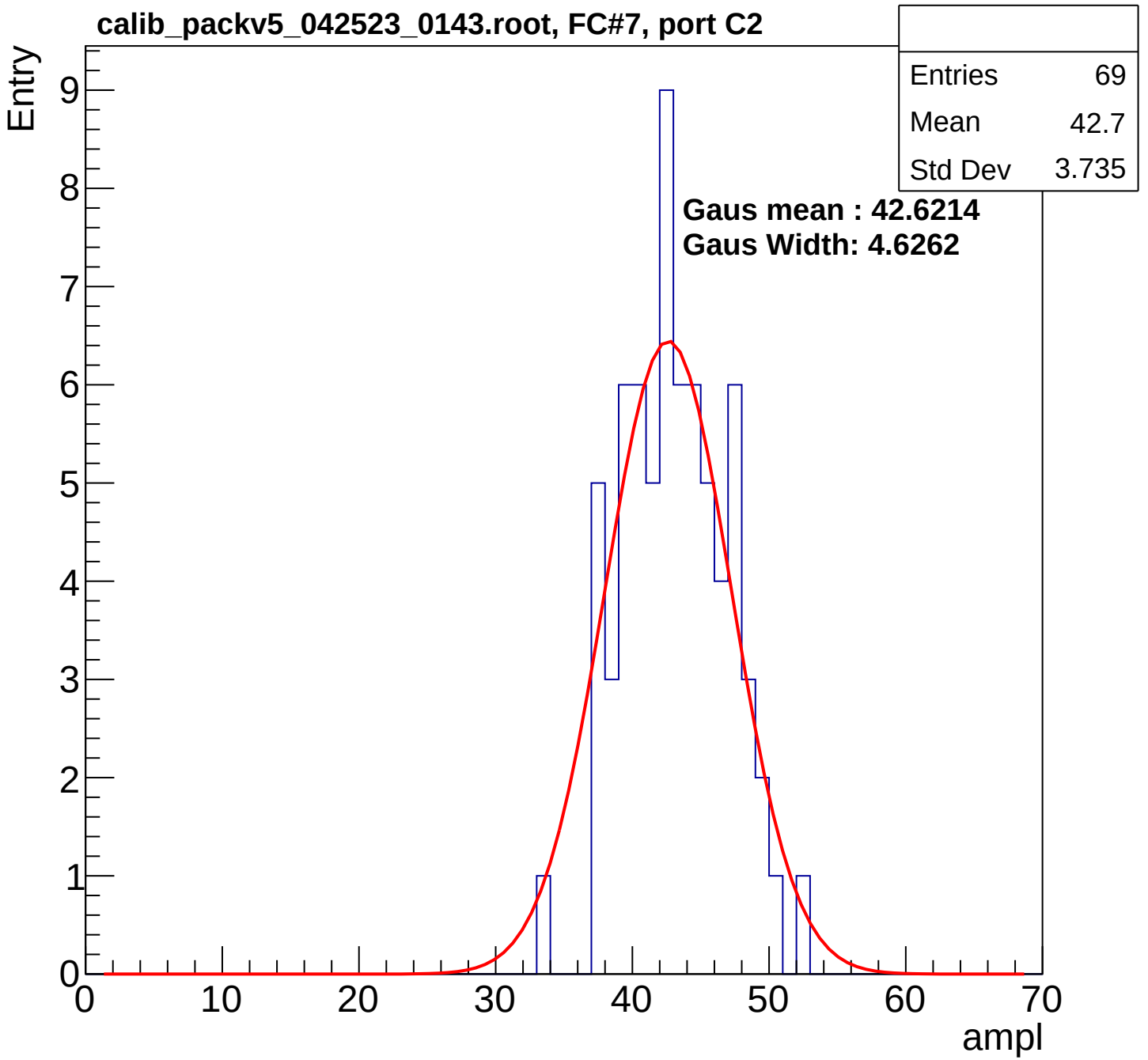
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch21, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 29.72
Std Dev 3.59
Gaus mean : 30.0946
Gaus Width: 3.9148
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch21, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 35.96
Std Dev 3.663
Gaus mean : 35.8693
Gaus Width: 3.9044
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch21, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 42.7
Std Dev 3.735
Gaus mean : 42.6214
Gaus Width: 4.6262
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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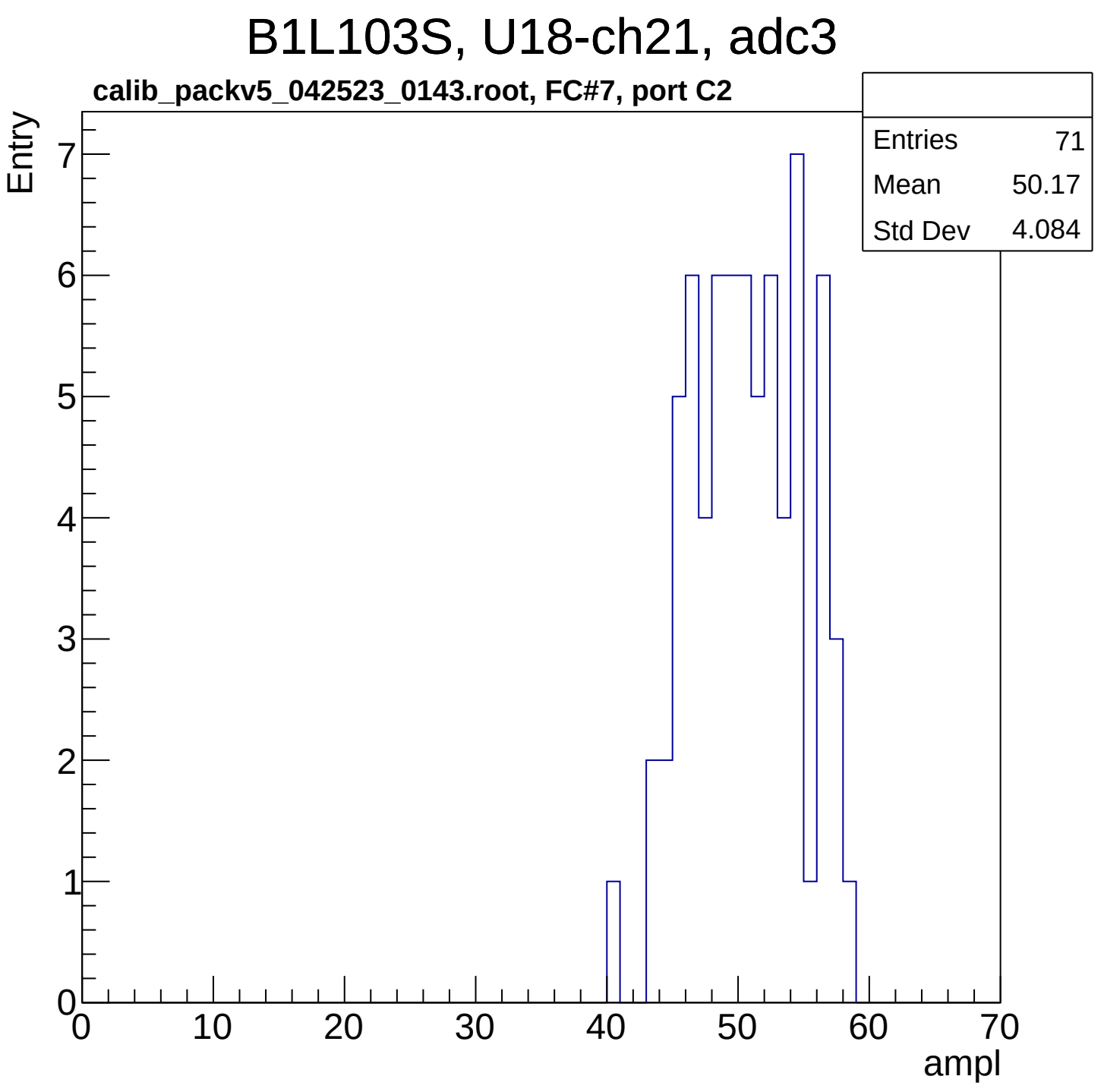
B1L103S, U18-ch21, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 71
Mean 50.17
Std Dev 4.084
Entry
ampl
0
1
2
3
4
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6
7
0
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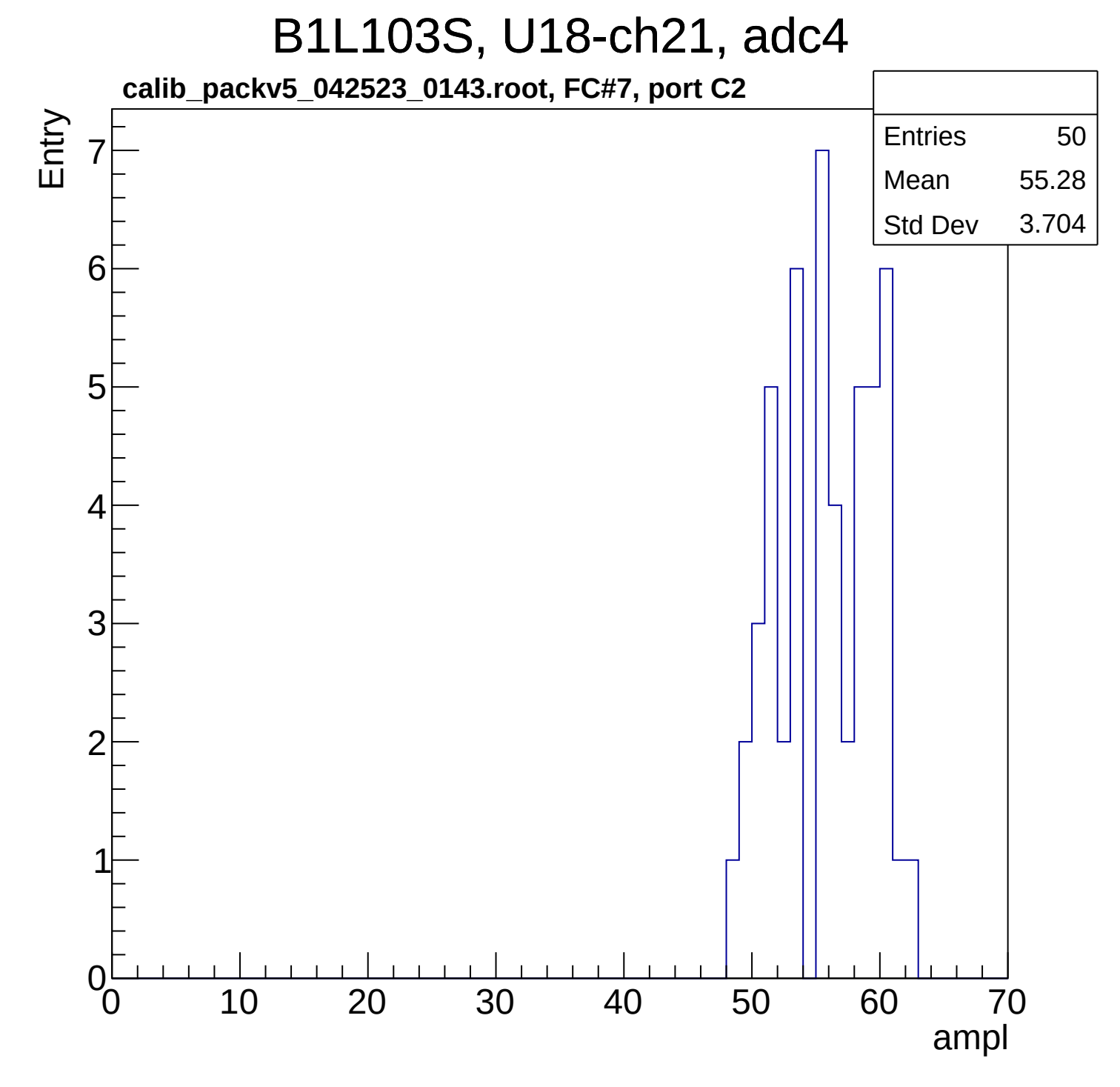
20
30
40
50
60
70


B1L103S, U18-ch21, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 50
Mean 55.28
Std Dev 3.704
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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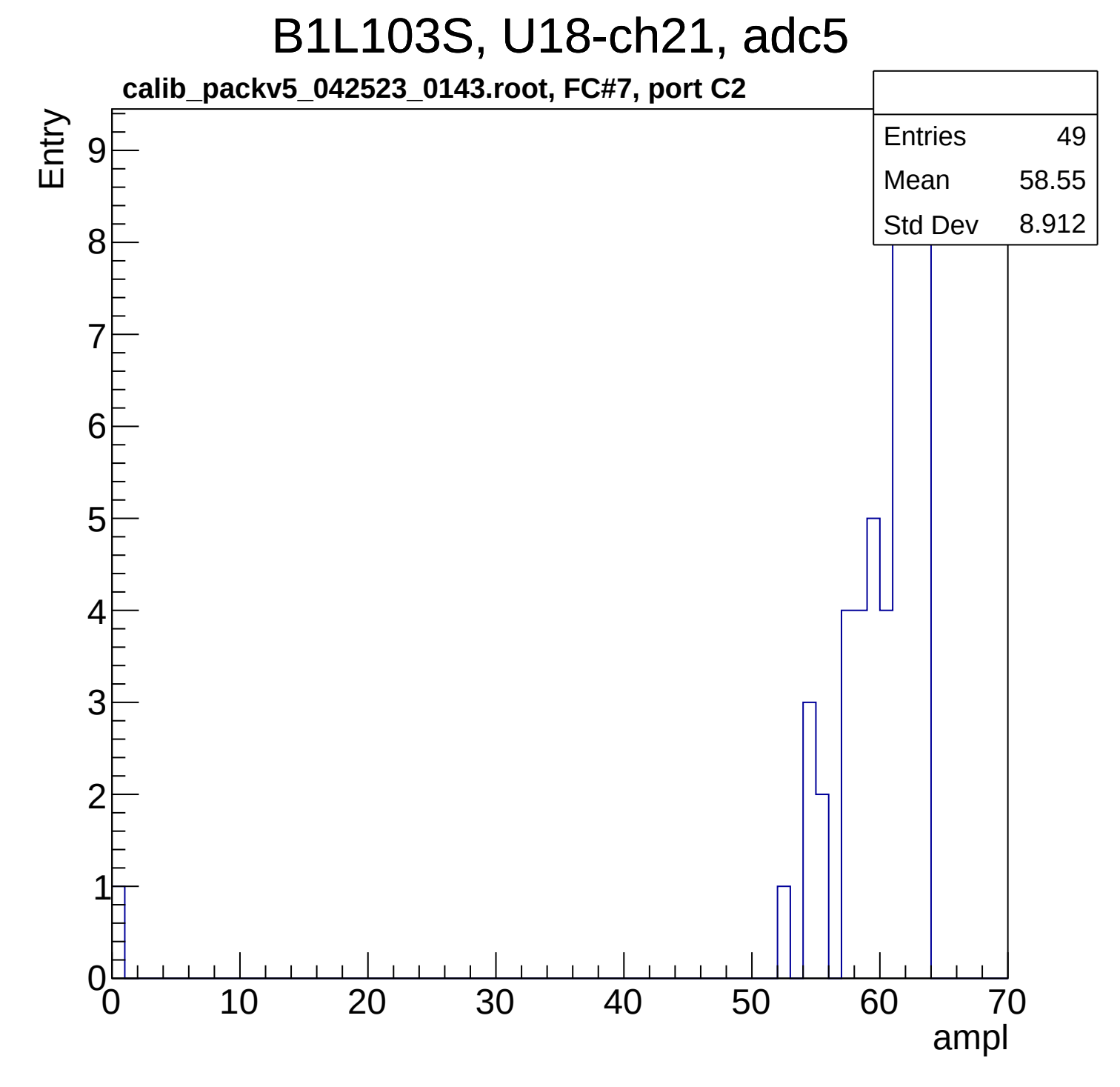
B1L103S, U18-ch21, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 49
Mean 58.55
Std Dev 8.912
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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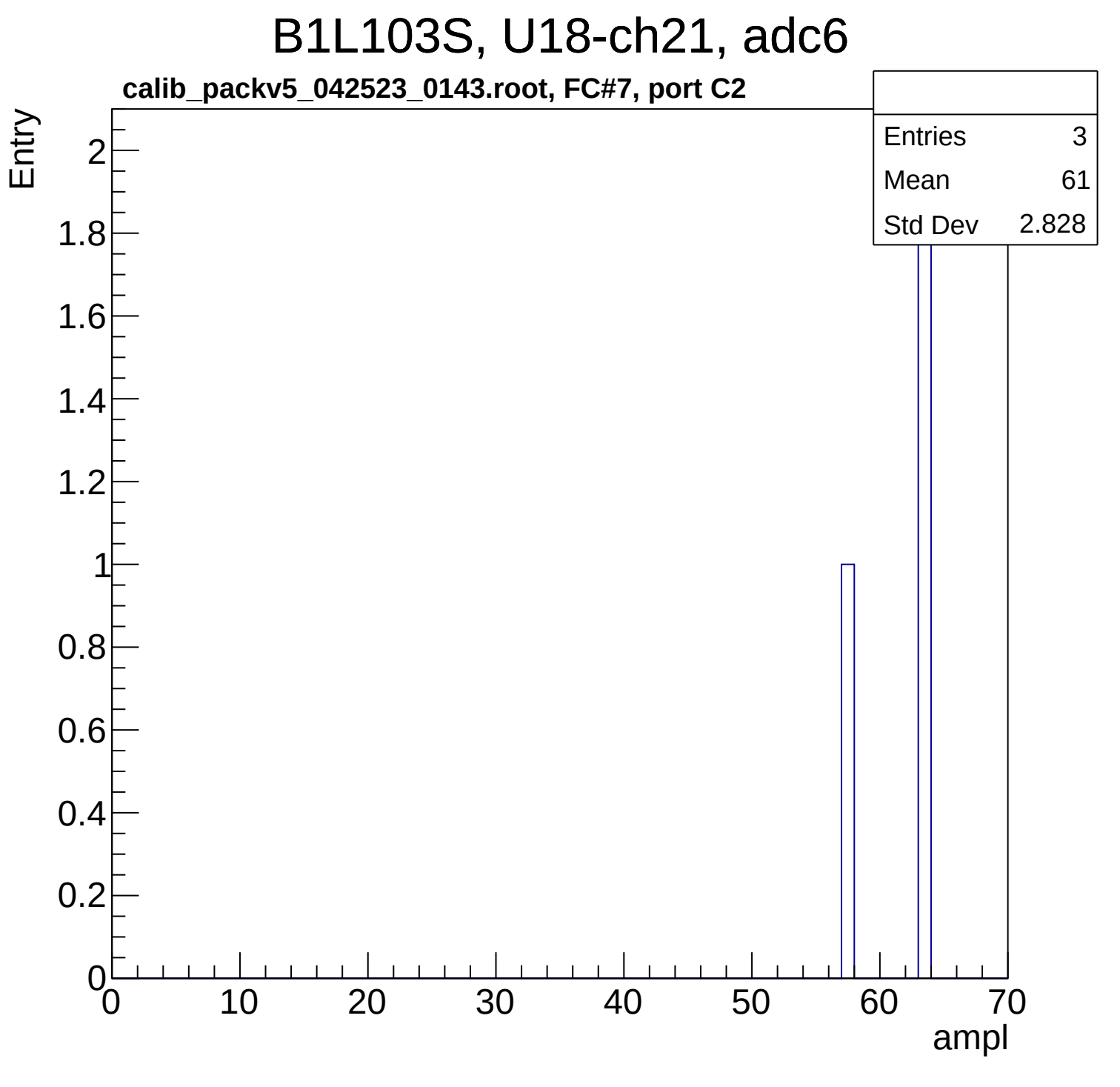
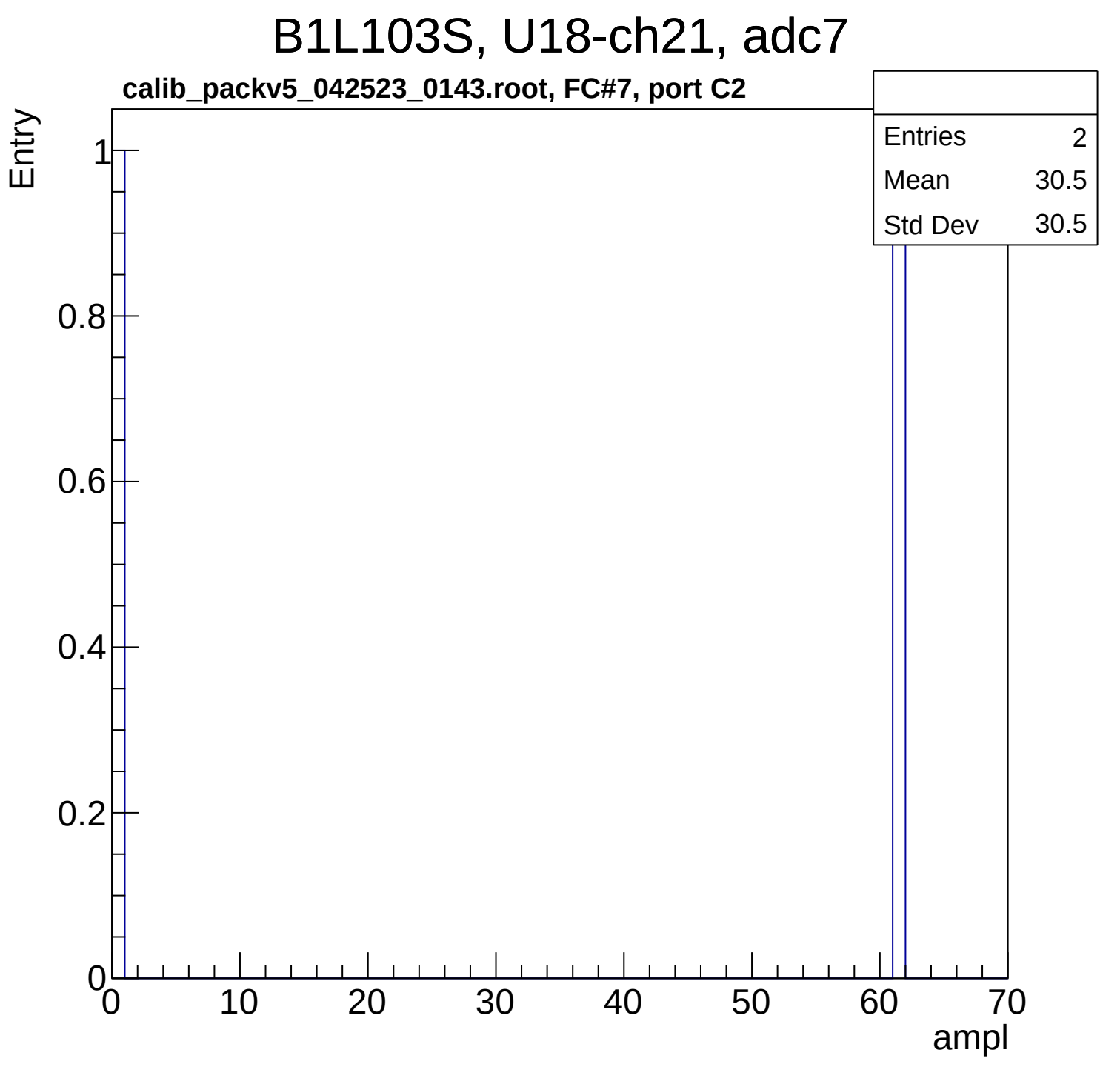
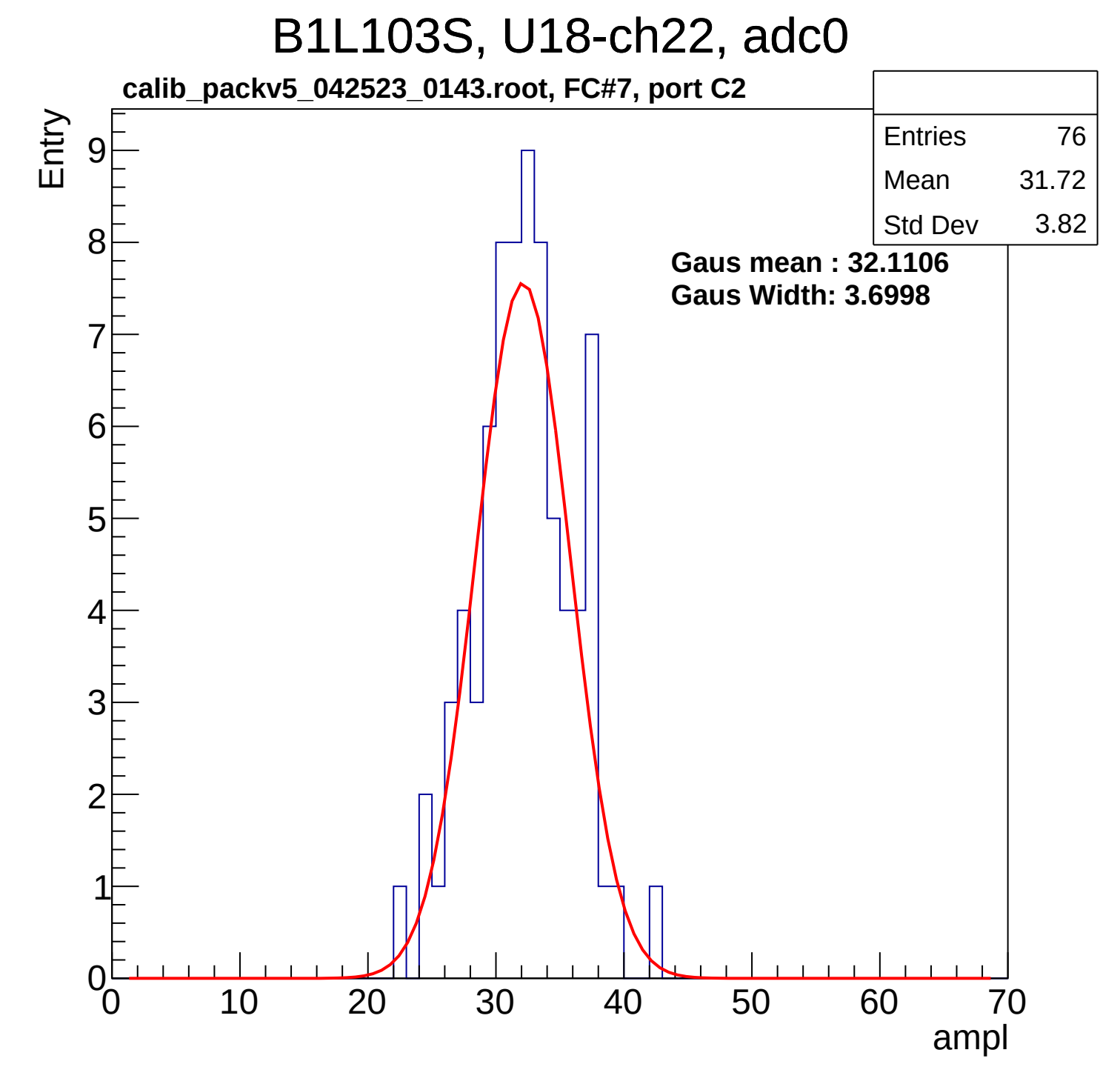
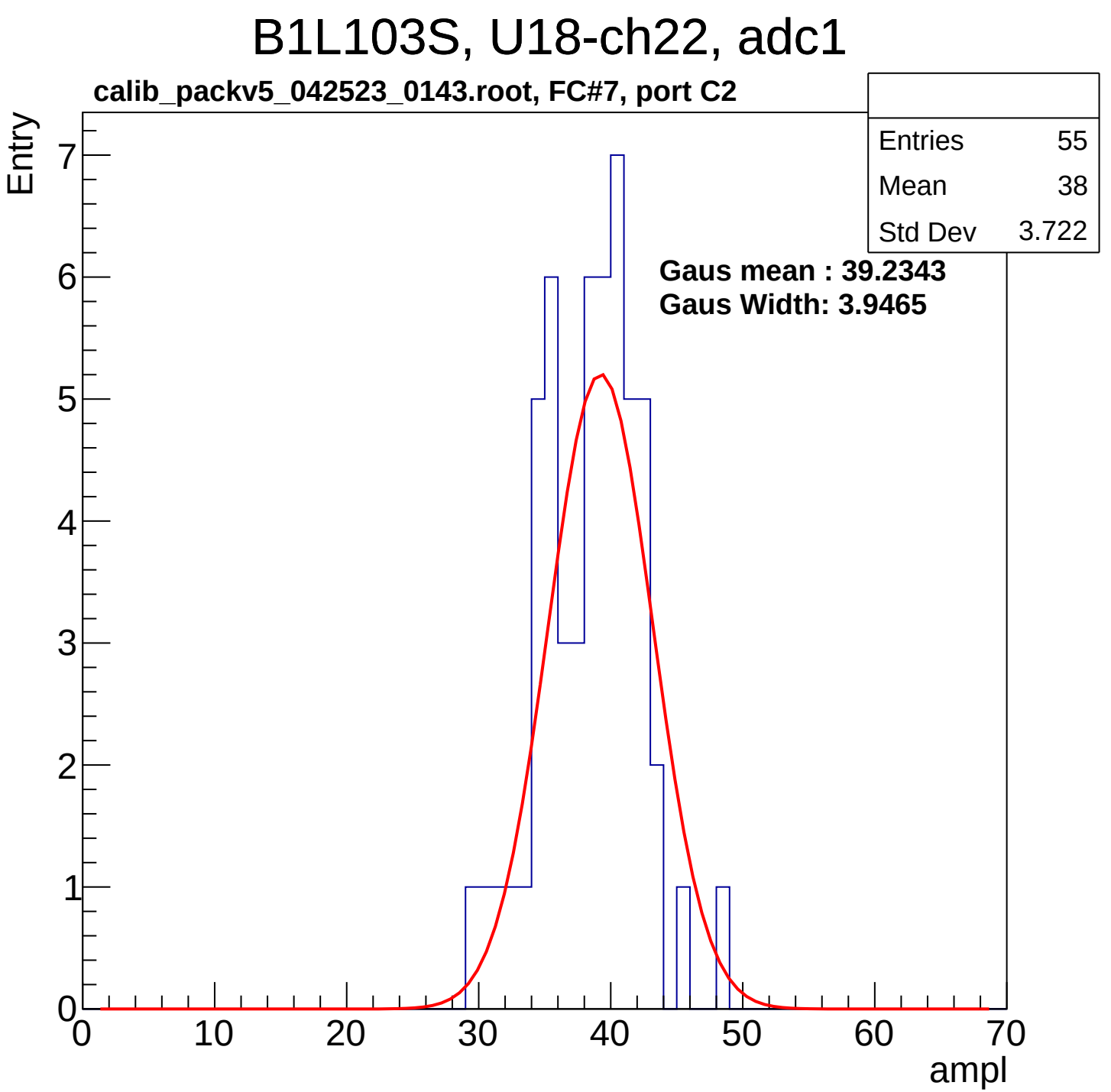
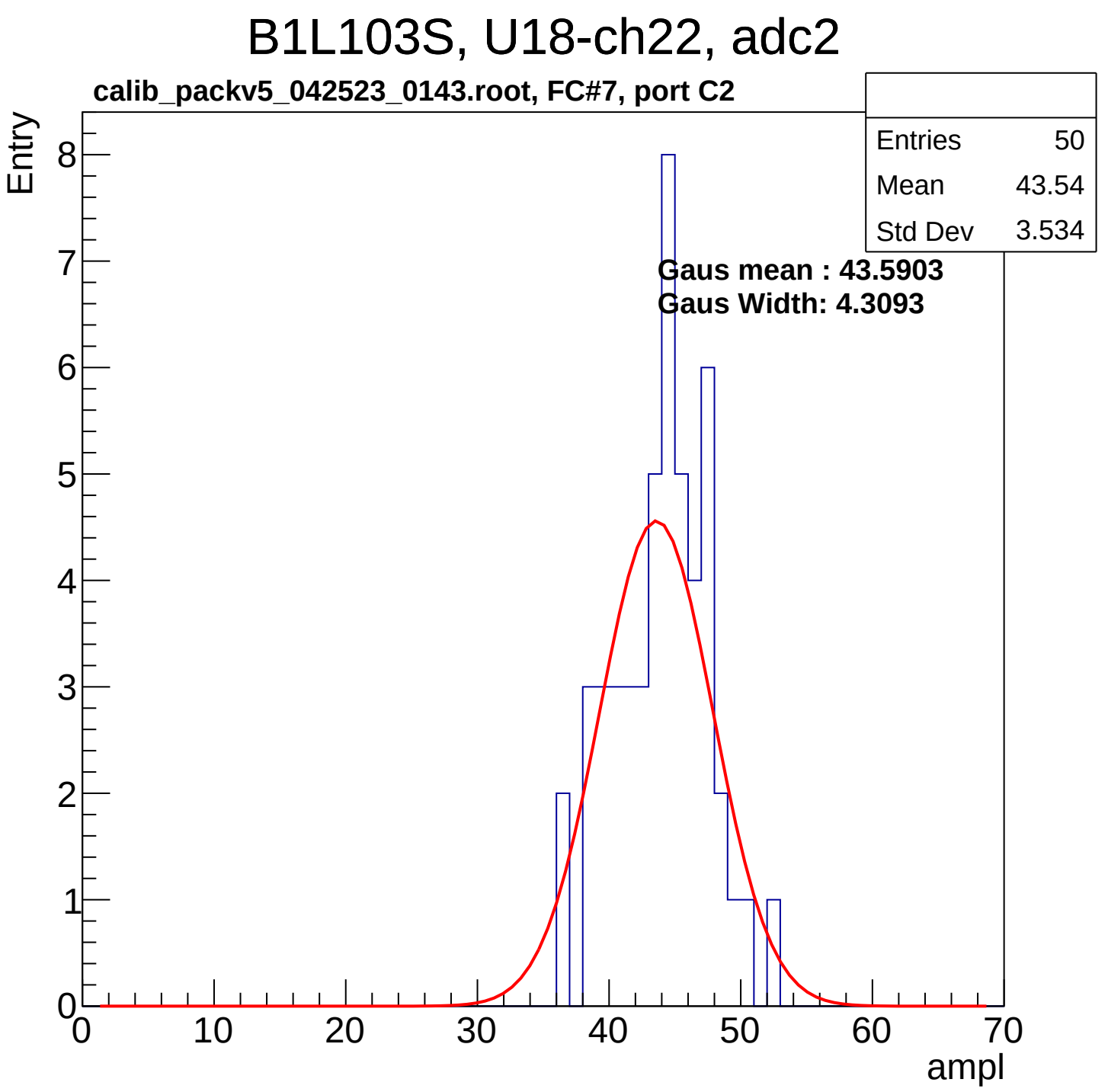

B1L103S, U18-ch21, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 61
Std Dev 2.828
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U18-ch21, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 30.5
Std Dev 30.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch22, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 76
Mean 31.72
Std Dev 3.82
Gaus mean : 32.1106
Gaus Width: 3.6998
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch22, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 38
Std Dev 3.722
Gaus mean : 39.2343
Gaus Width: 3.9465
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch22, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 50
Mean 43.54
Std Dev 3.534
Gaus mean : 43.5903
Gaus Width: 4.3093
Entry
ampl
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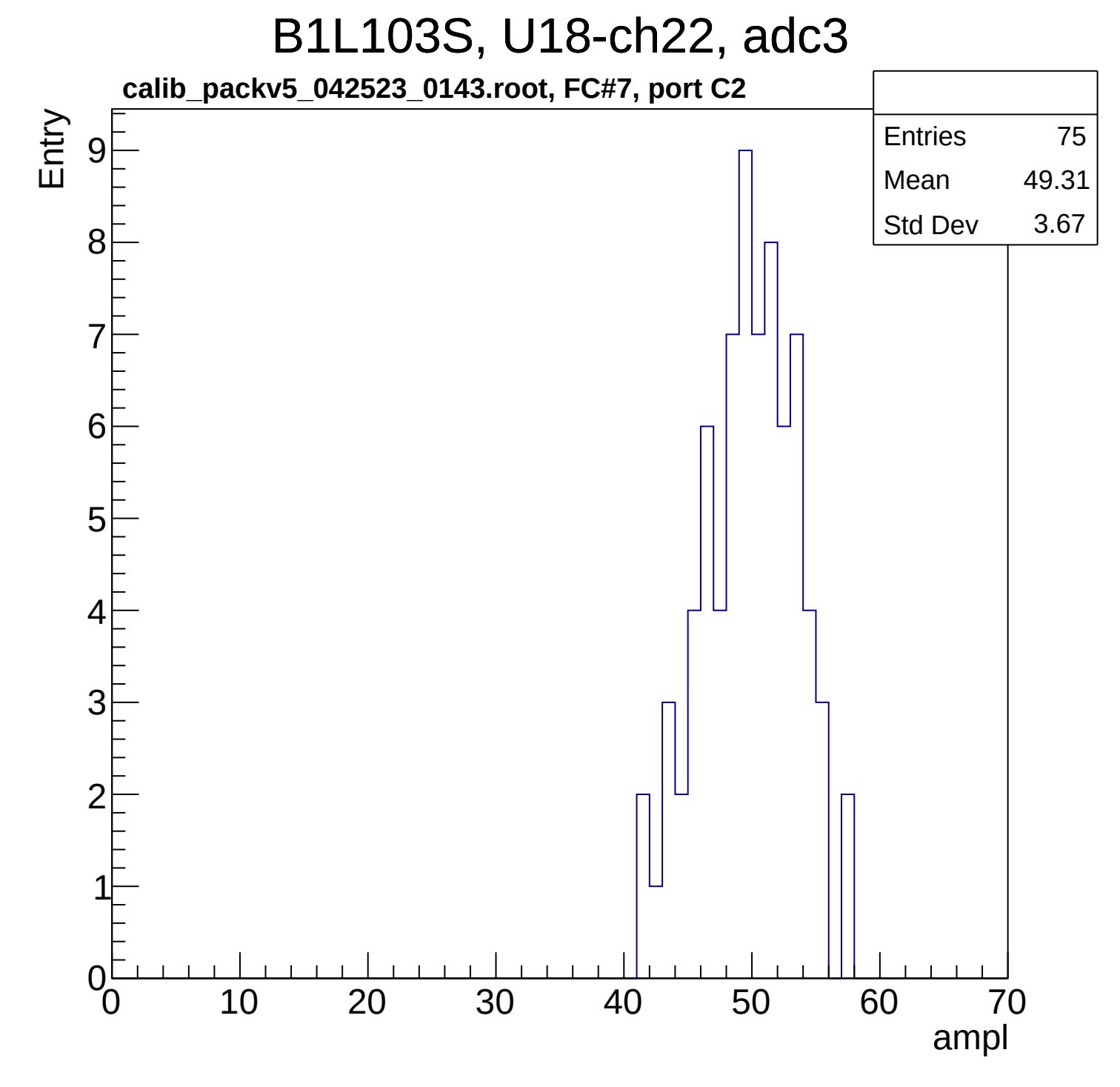
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch22, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 75
Mean 49.31
Std Dev 3.67
Entry
ampl
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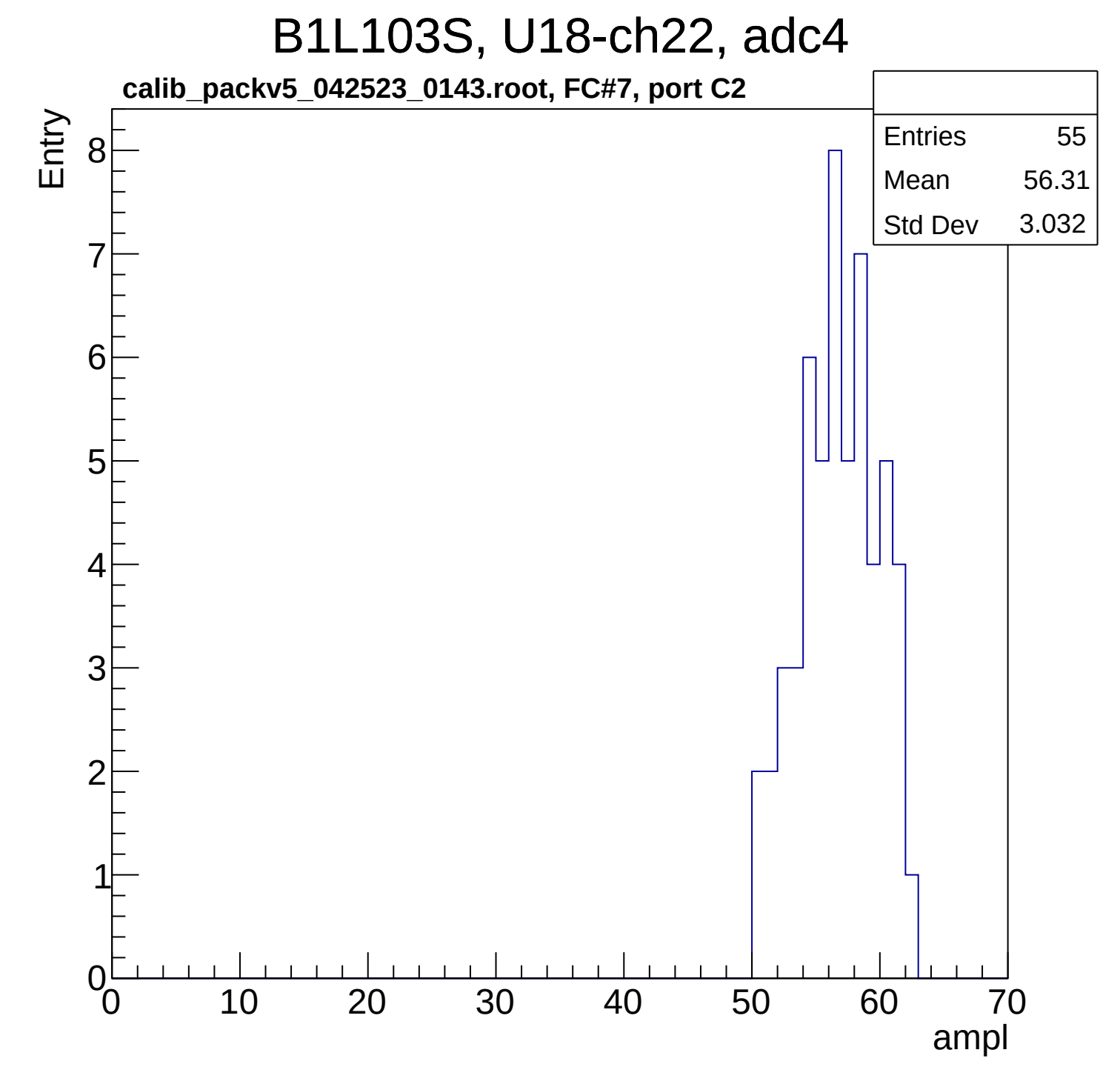
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch22, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 56.31
Std Dev 3.032
Entry
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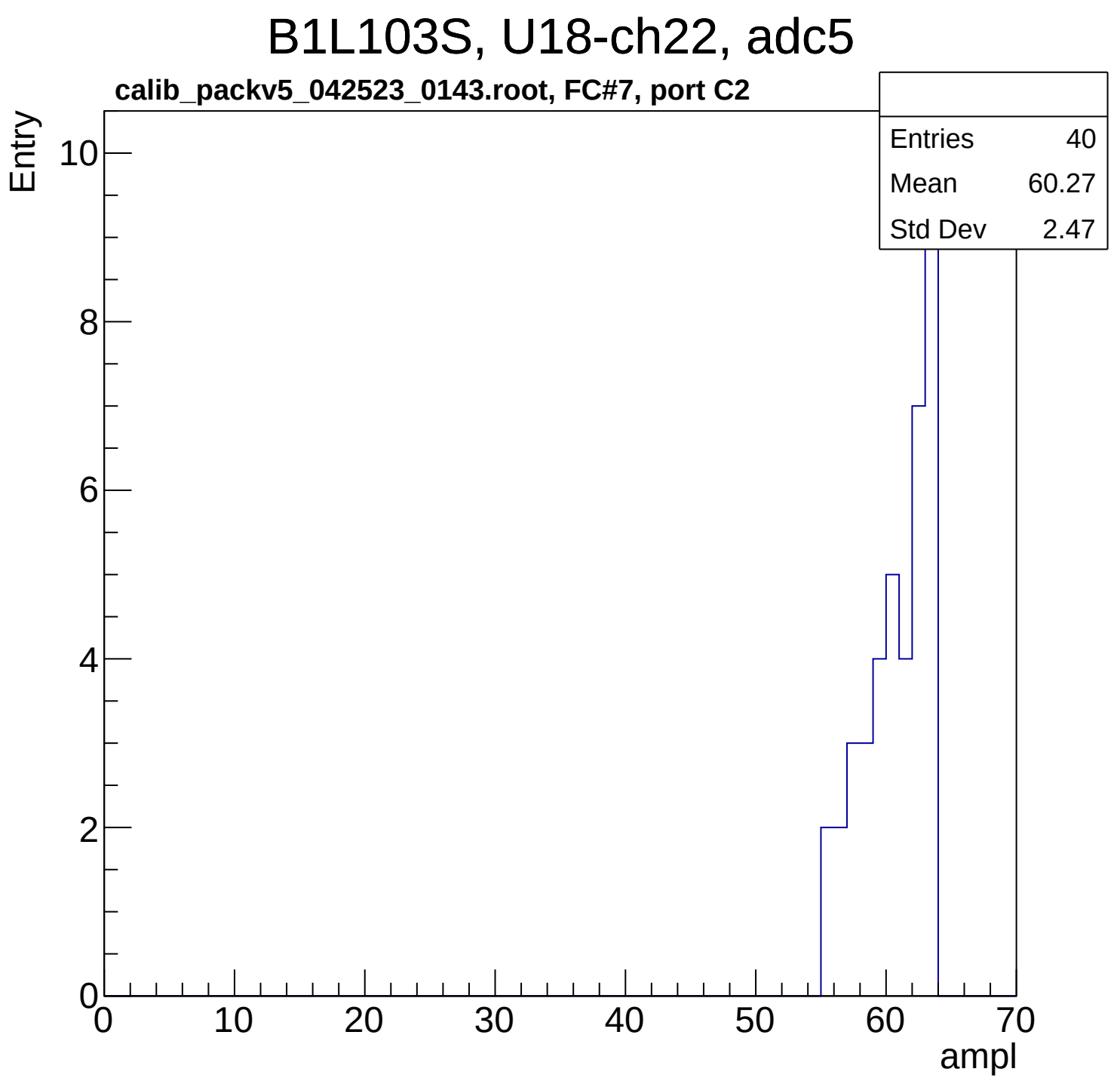
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch22, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 40
Mean 60.27
Std Dev 2.47
Entry
0
2
4
6
8
10
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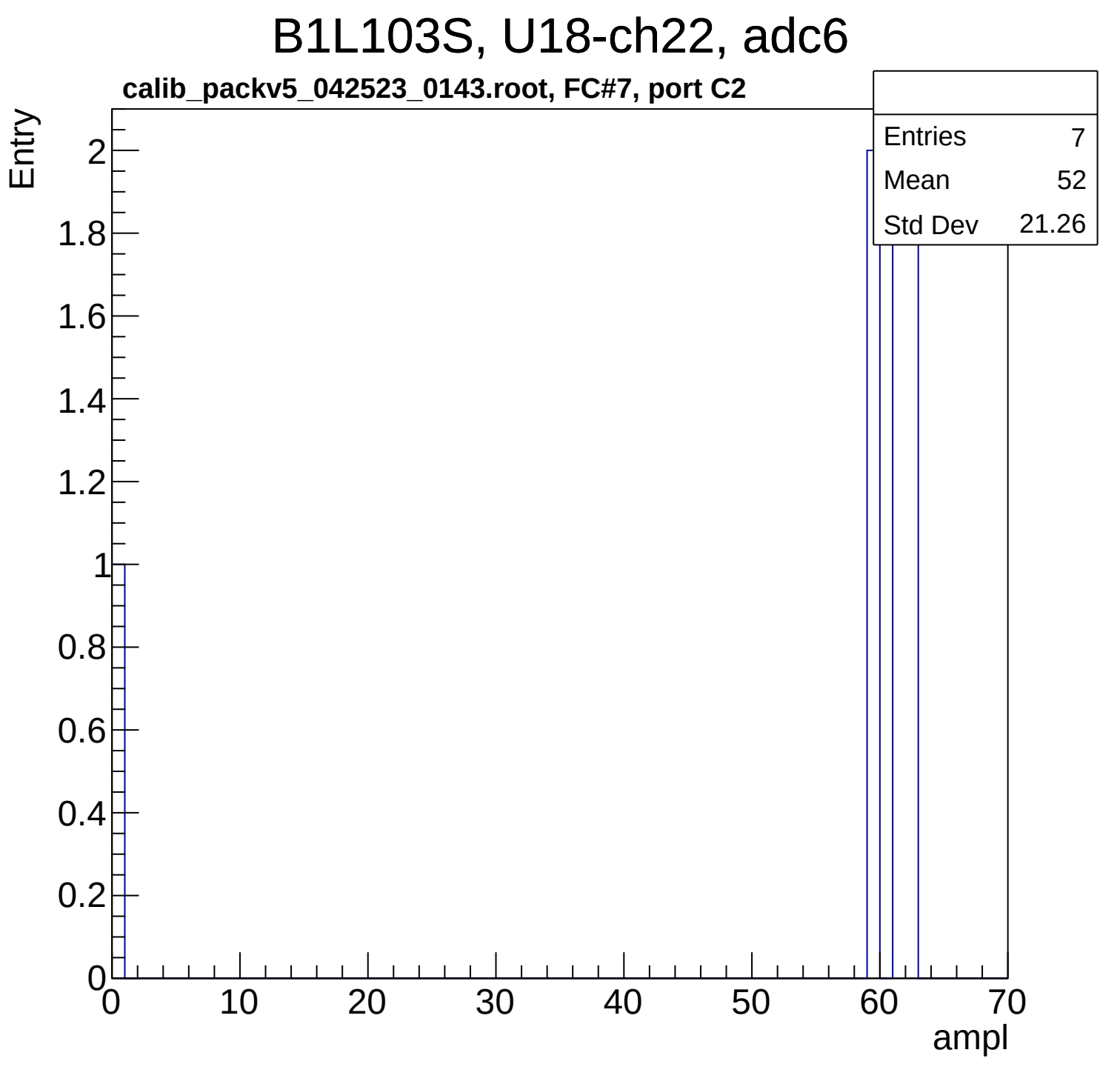
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch22, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 7
Mean 52
Std Dev 21.26
Entry
ampl
0
0.2
0.4
0.6
0.8
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1.2
1.4
1.6
1.8
2
0
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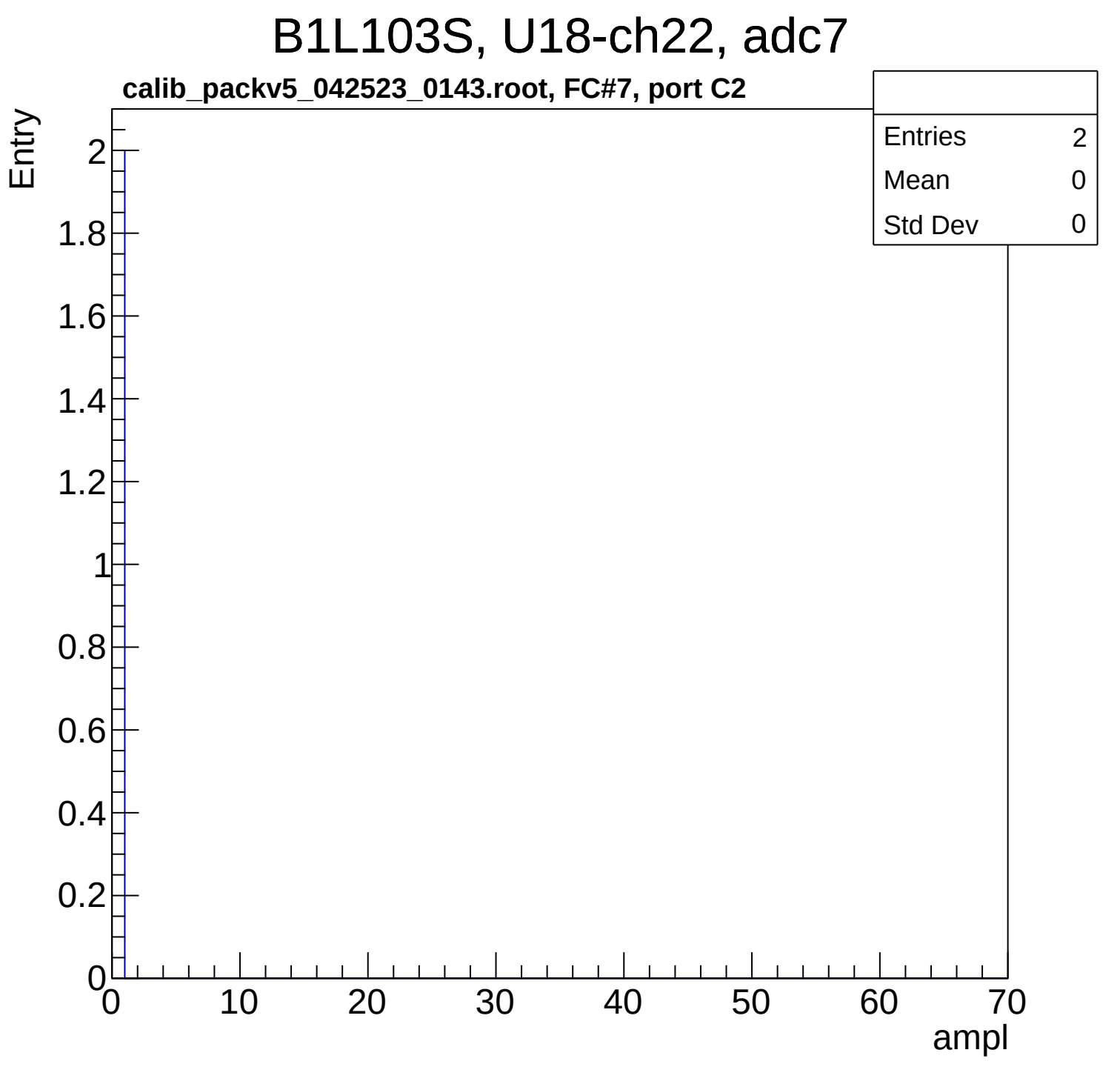
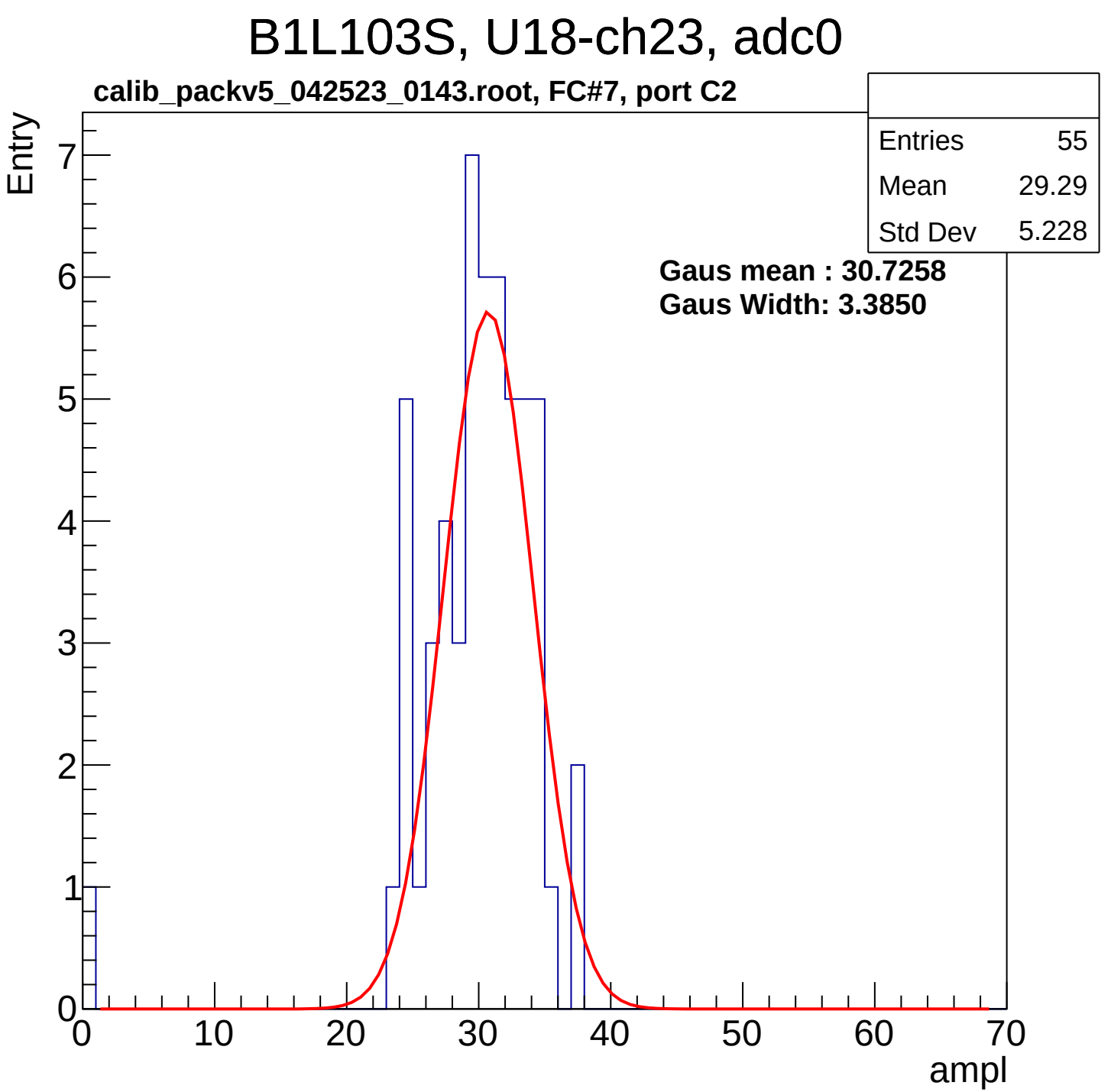
20
30
40
50
60
70


B1L103S, U18-ch22, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch23, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 29.29
Std Dev 5.228
Gaus mean : 30.7258
Gaus Width: 3.3850
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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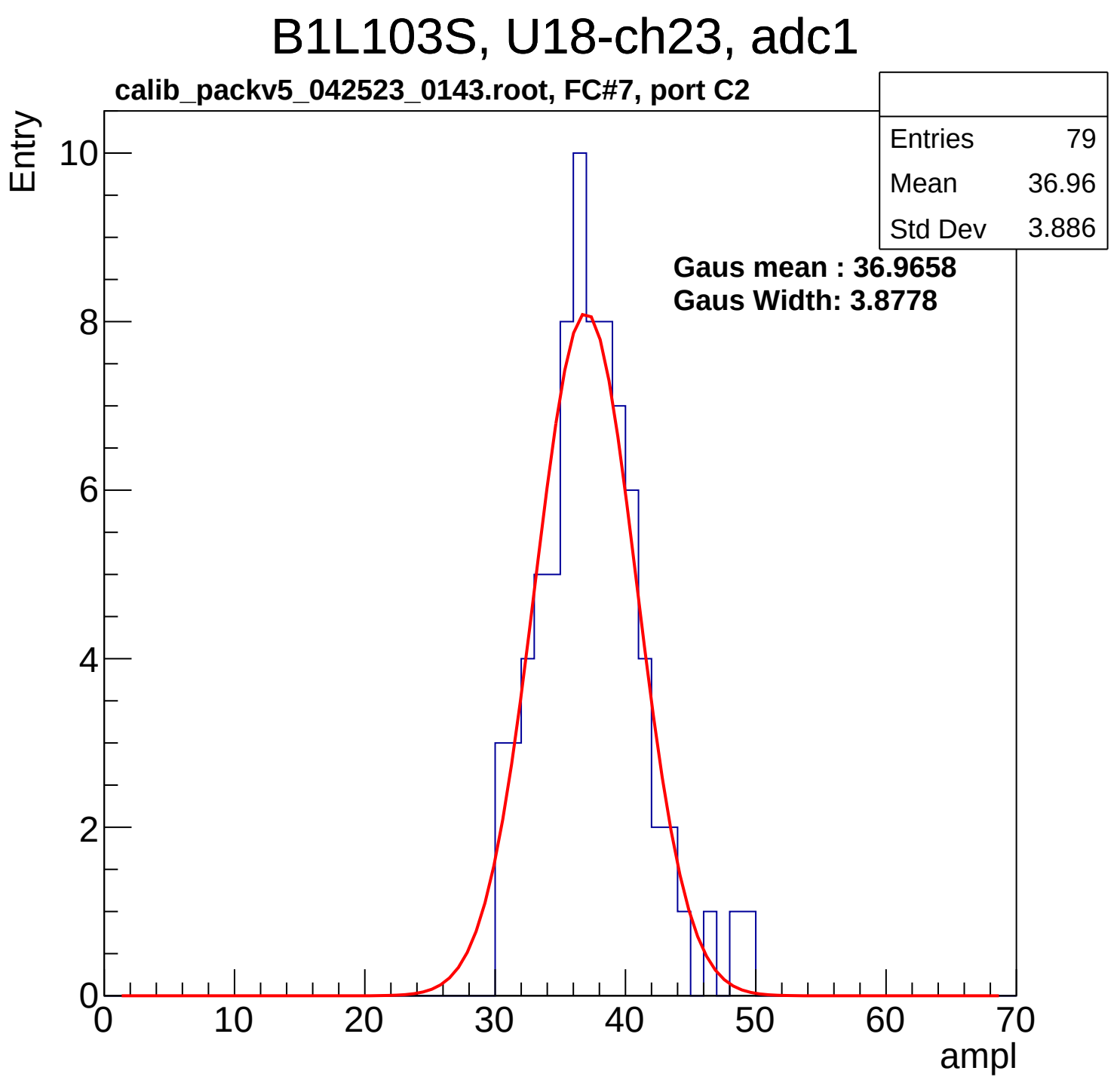
B1L103S, U18-ch23, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 79
Mean 36.96
Std Dev 3.886
Gaus mean : 36.9658
Gaus Width: 3.8778
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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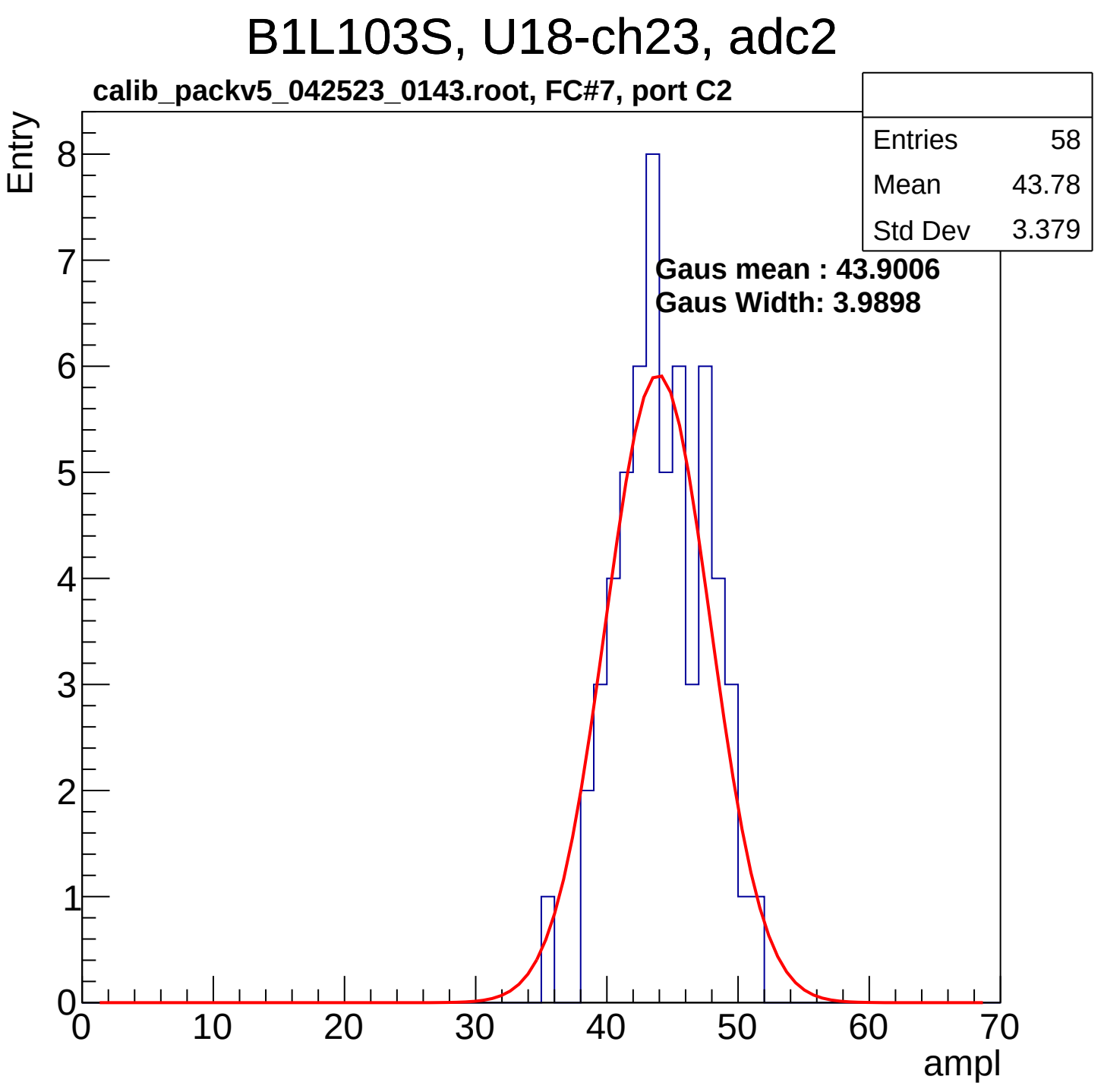
B1L103S, U18-ch23, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 58
Mean 43.78
Std Dev 3.379
Gaus mean : 43.9006
Gaus Width: 3.9898
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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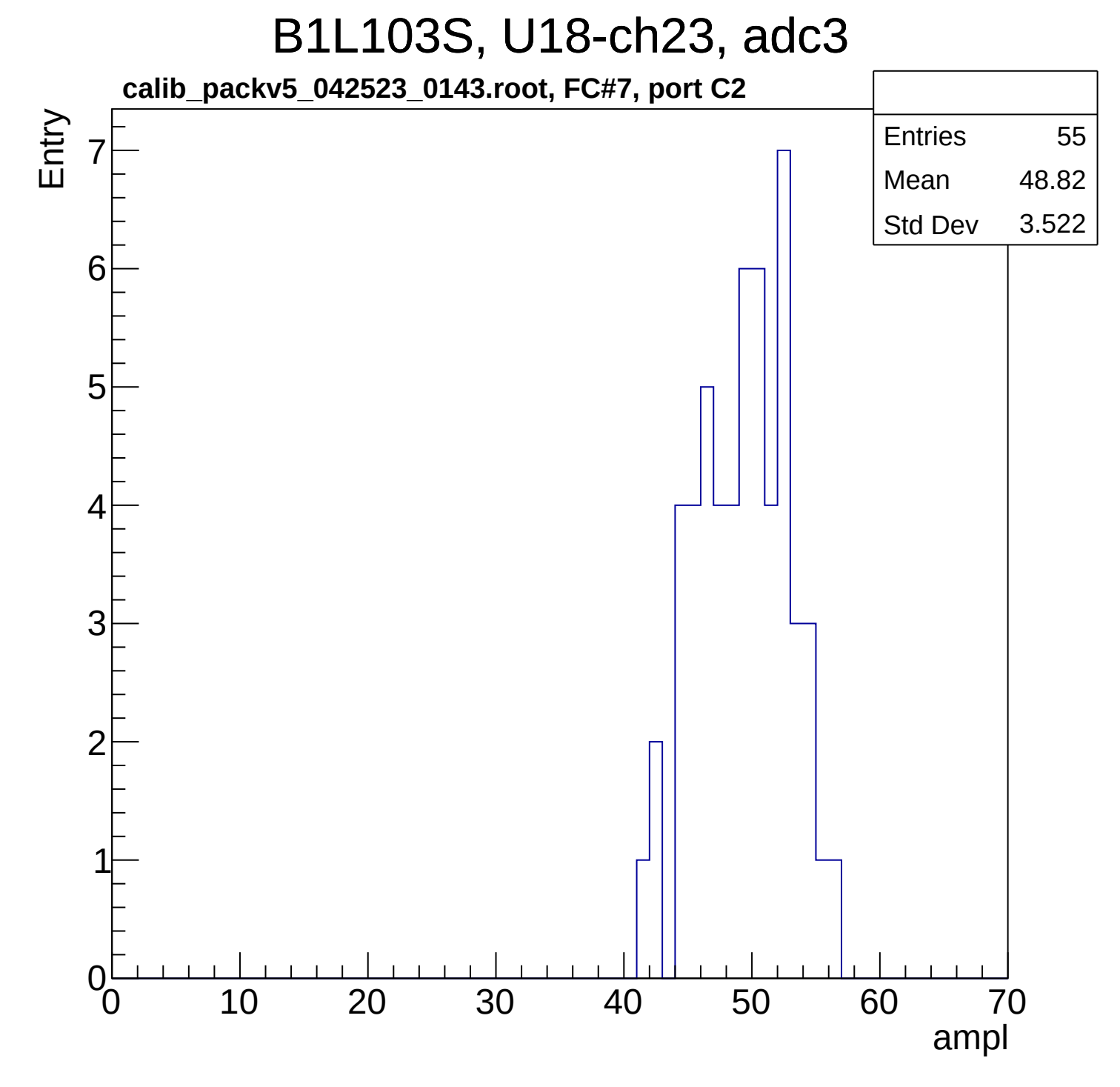
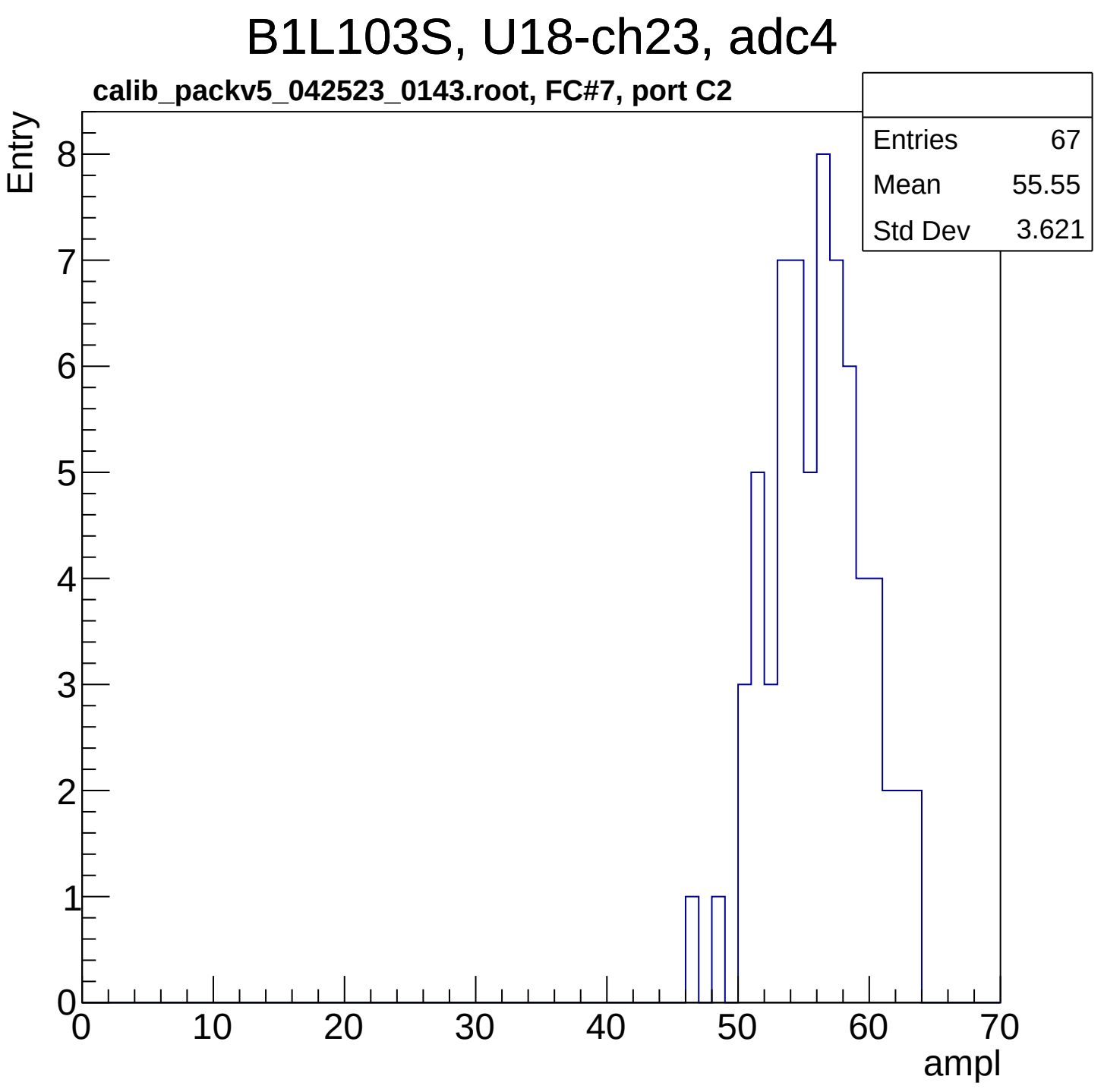

B1L103S, U18-ch23, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 48.82
Std Dev 3.522
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch23, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 55.55
Std Dev 3.621
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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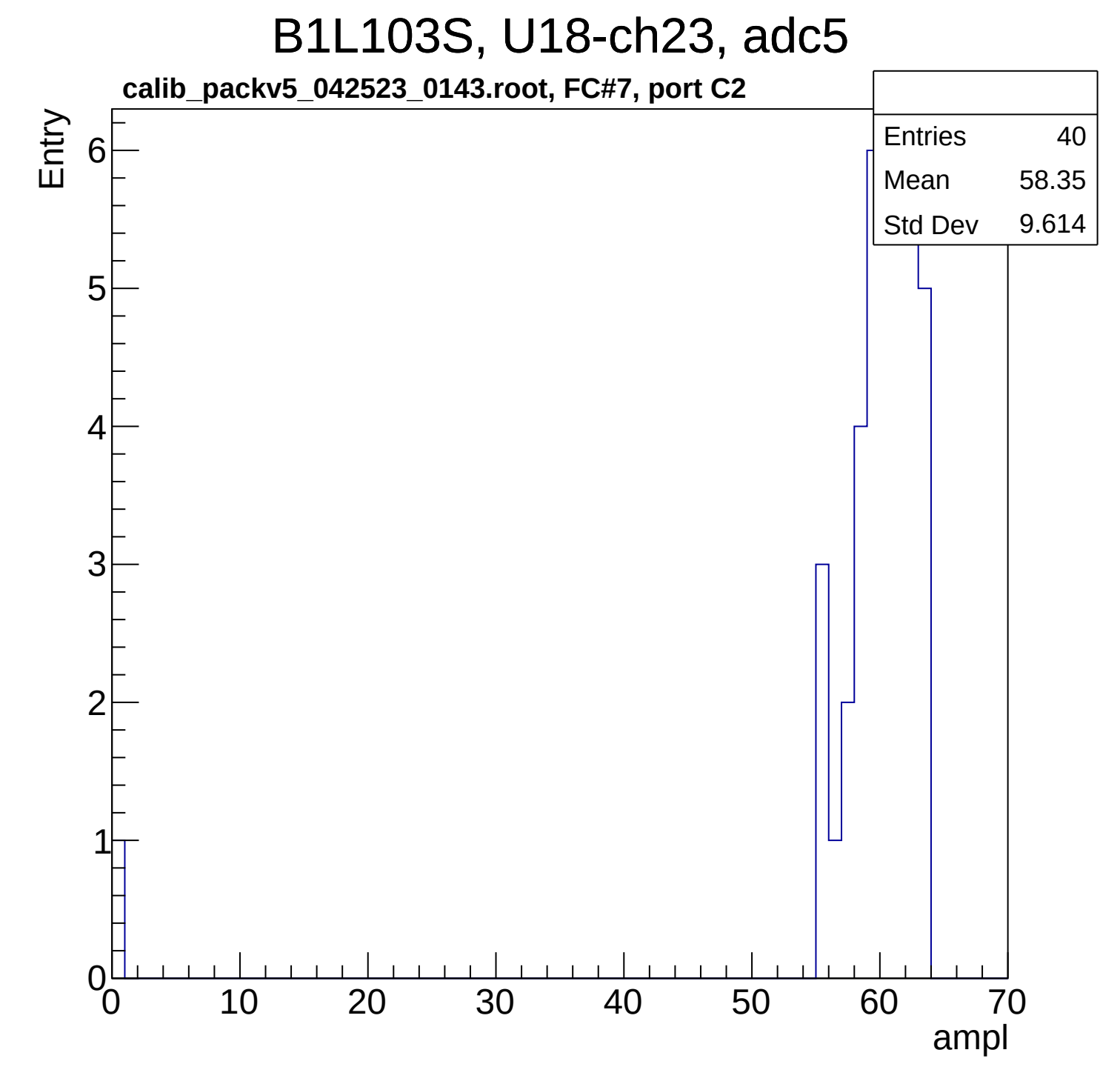
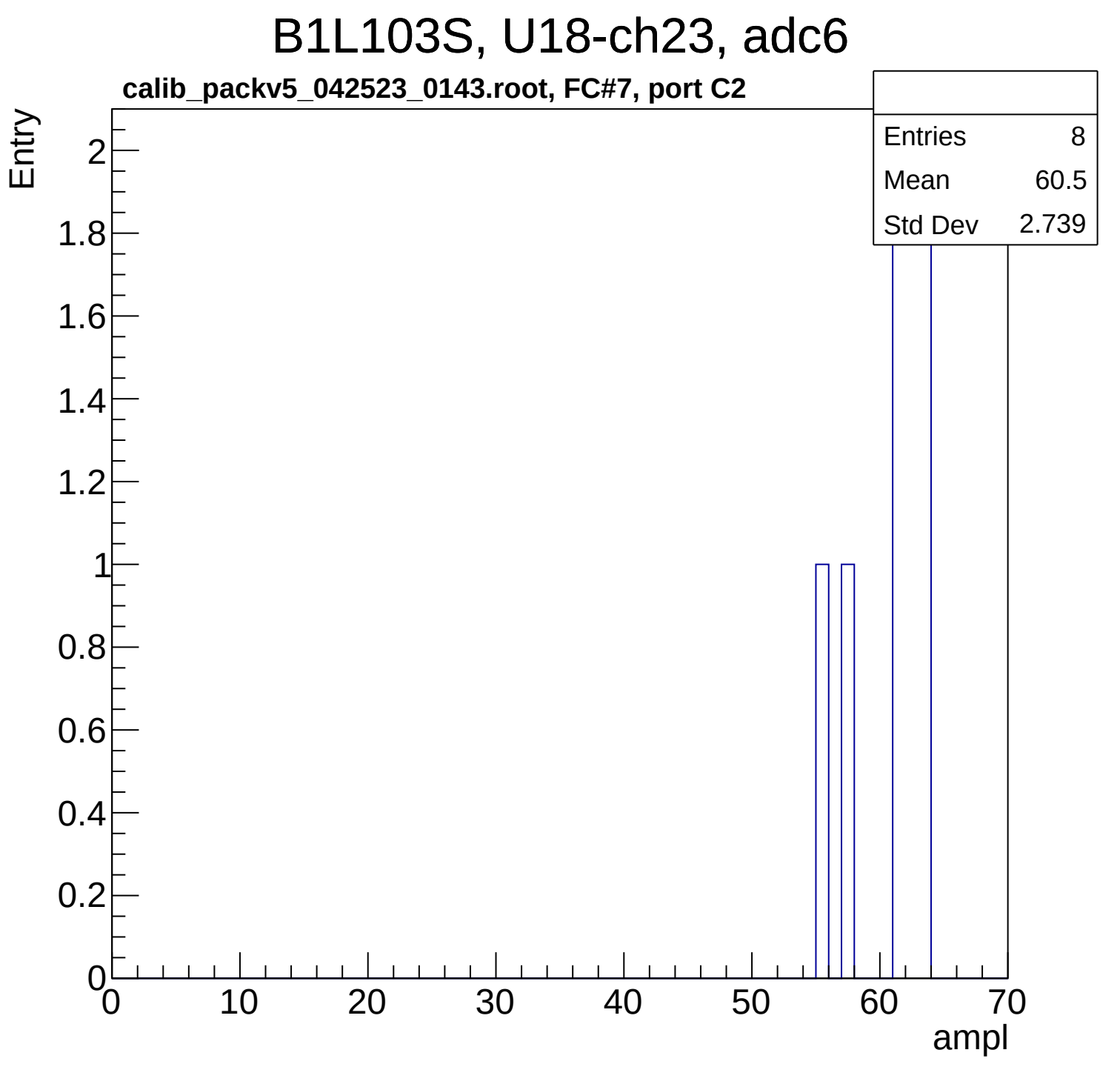
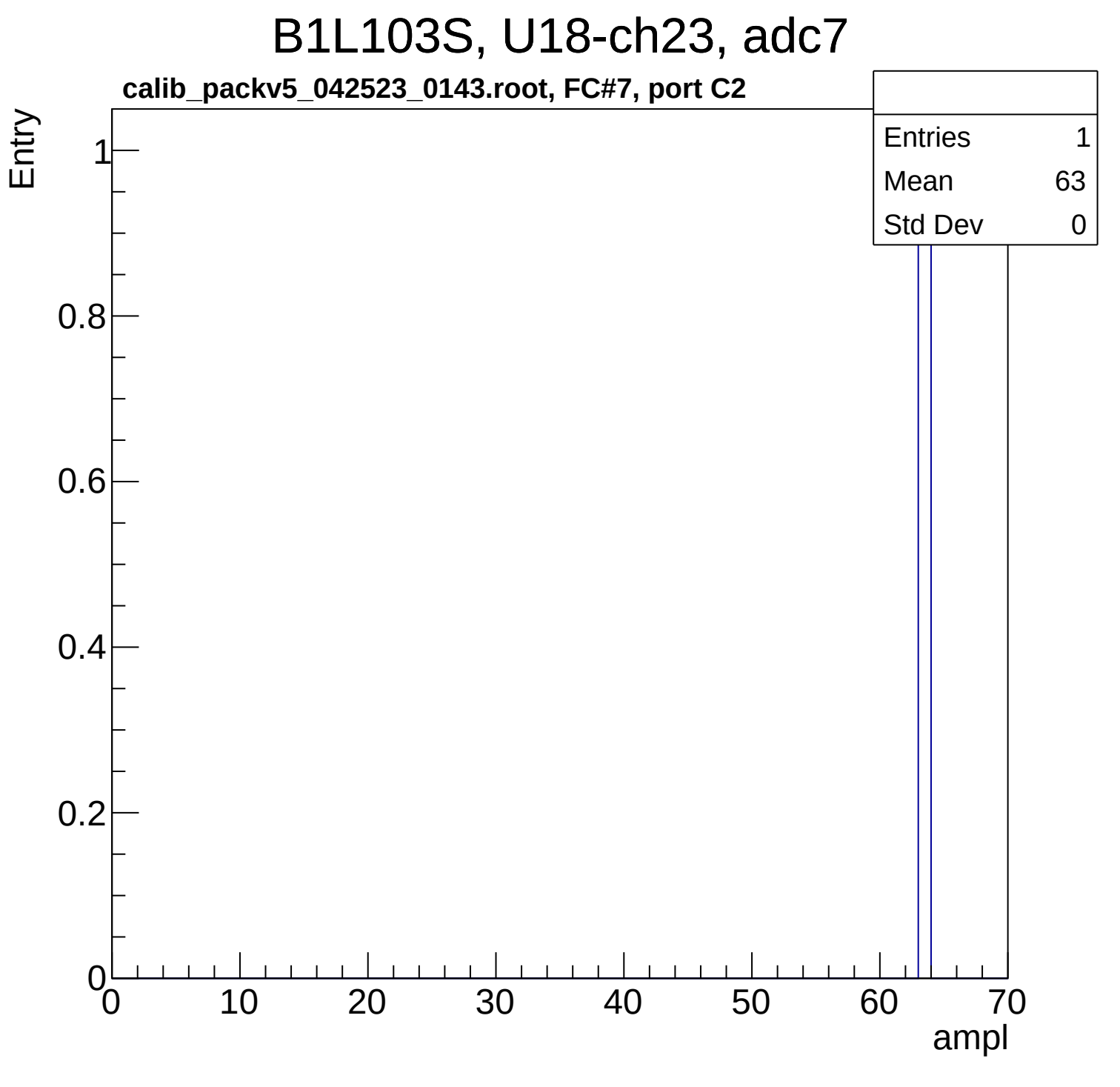
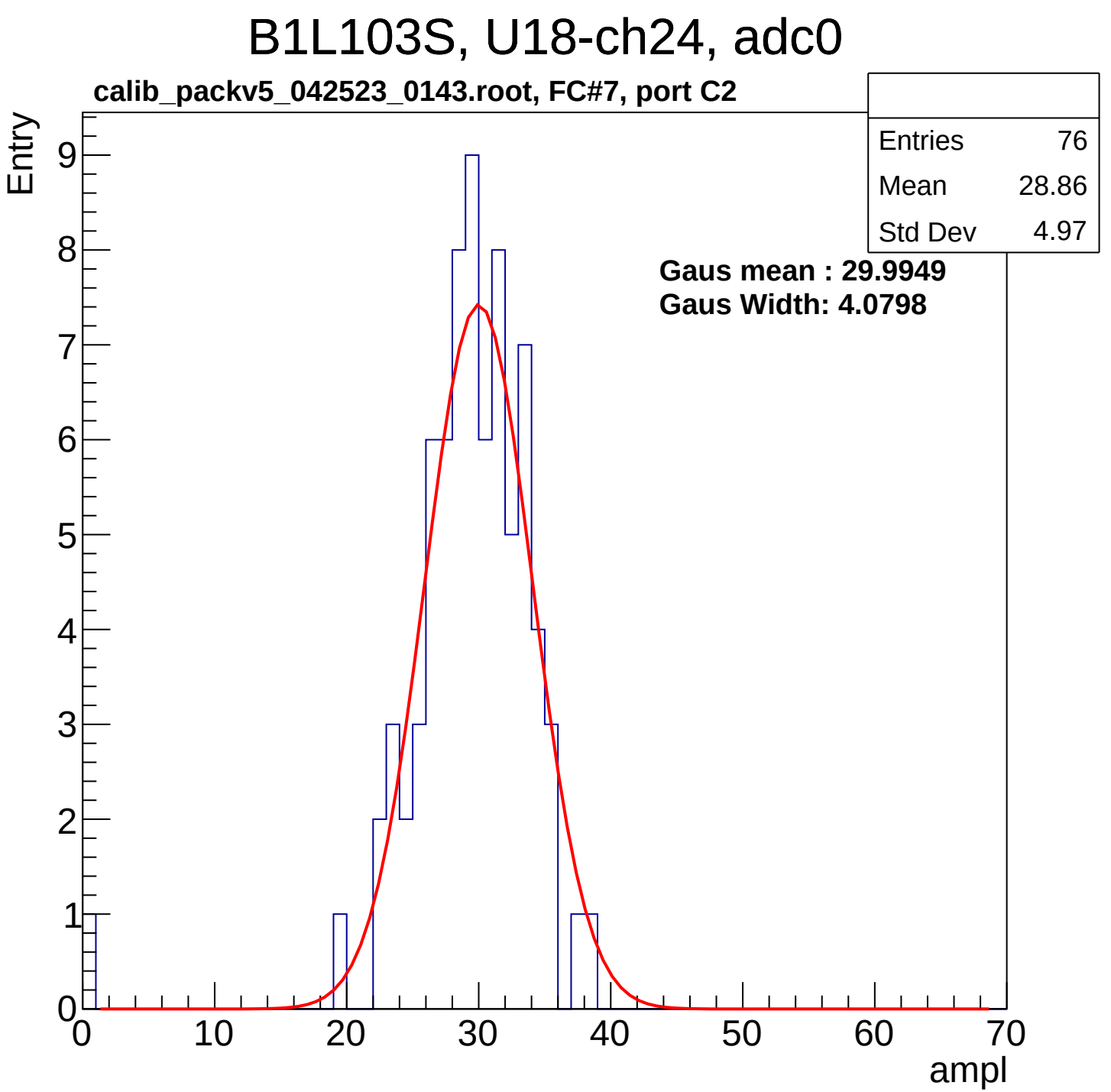
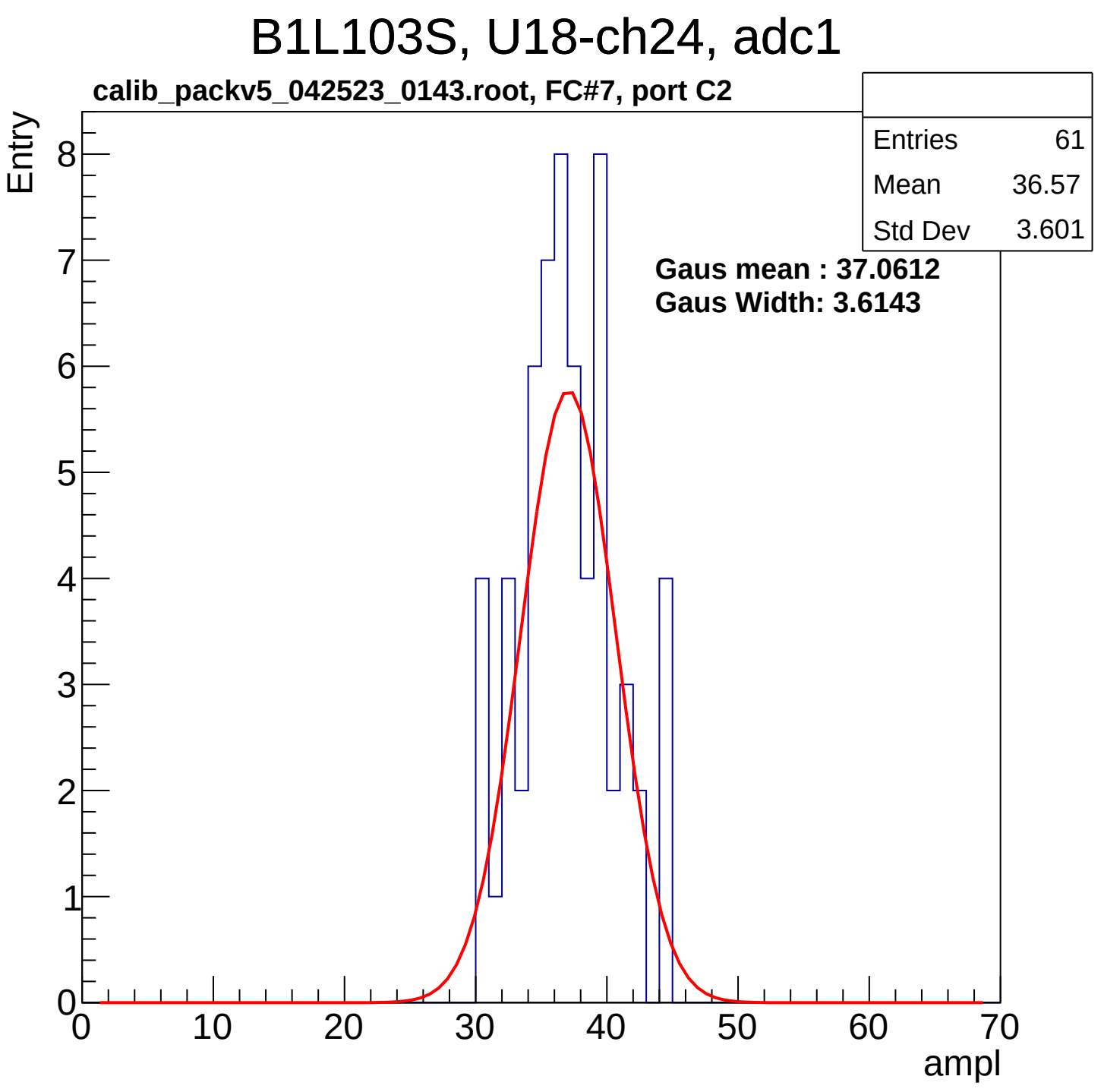
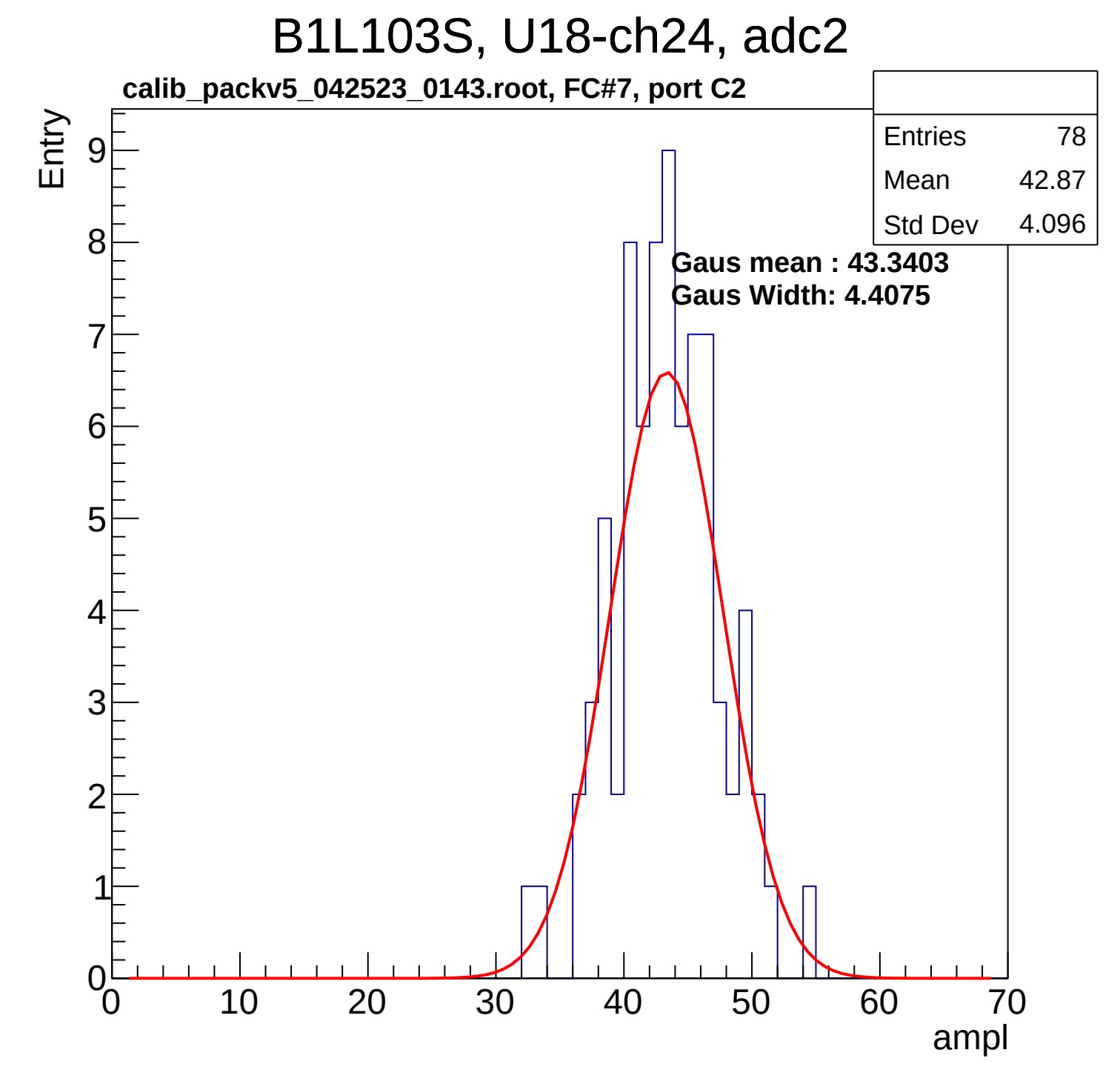

B1L103S, U18-ch23, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 40
Mean 58.35
Std Dev 9.614
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U18-ch23, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 8
Mean 60.5
Std Dev 2.739
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U18-ch23, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch24, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 76
Mean 28.86
Std Dev 4.97
Gaus mean : 29.9949
Gaus Width: 4.0798
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch24, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 61
Mean 36.57
Std Dev 3.601
Gaus mean : 37.0612
Gaus Width: 3.6143
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch24, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 78
Mean 42.87
Std Dev 4.096
Gaus mean : 43.3403
Gaus Width: 4.4075
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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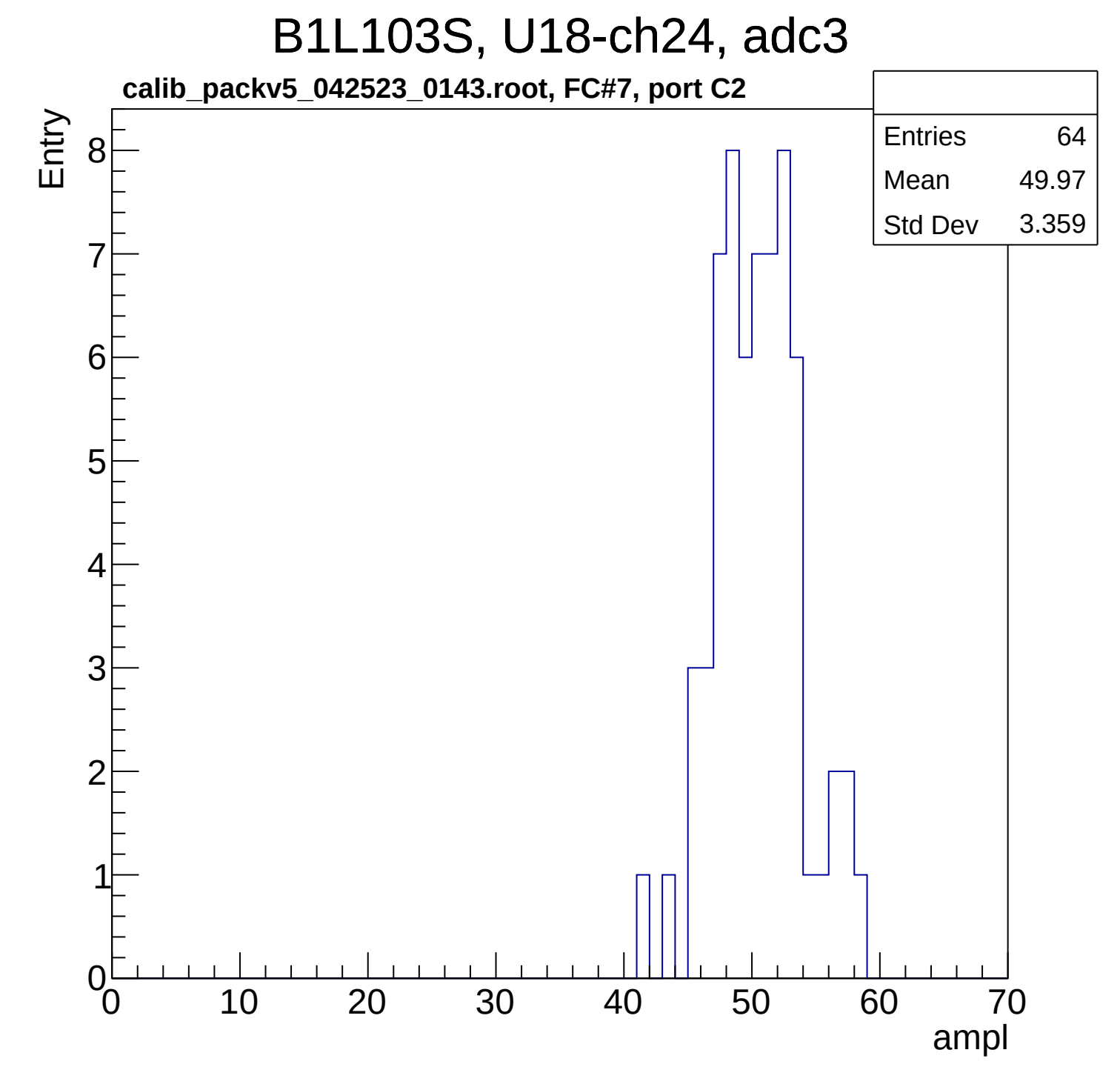
B1L103S, U18-ch24, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 49.97
Std Dev 3.359
Entry
ampl
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2
3
4
5
6
7
8
0
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60
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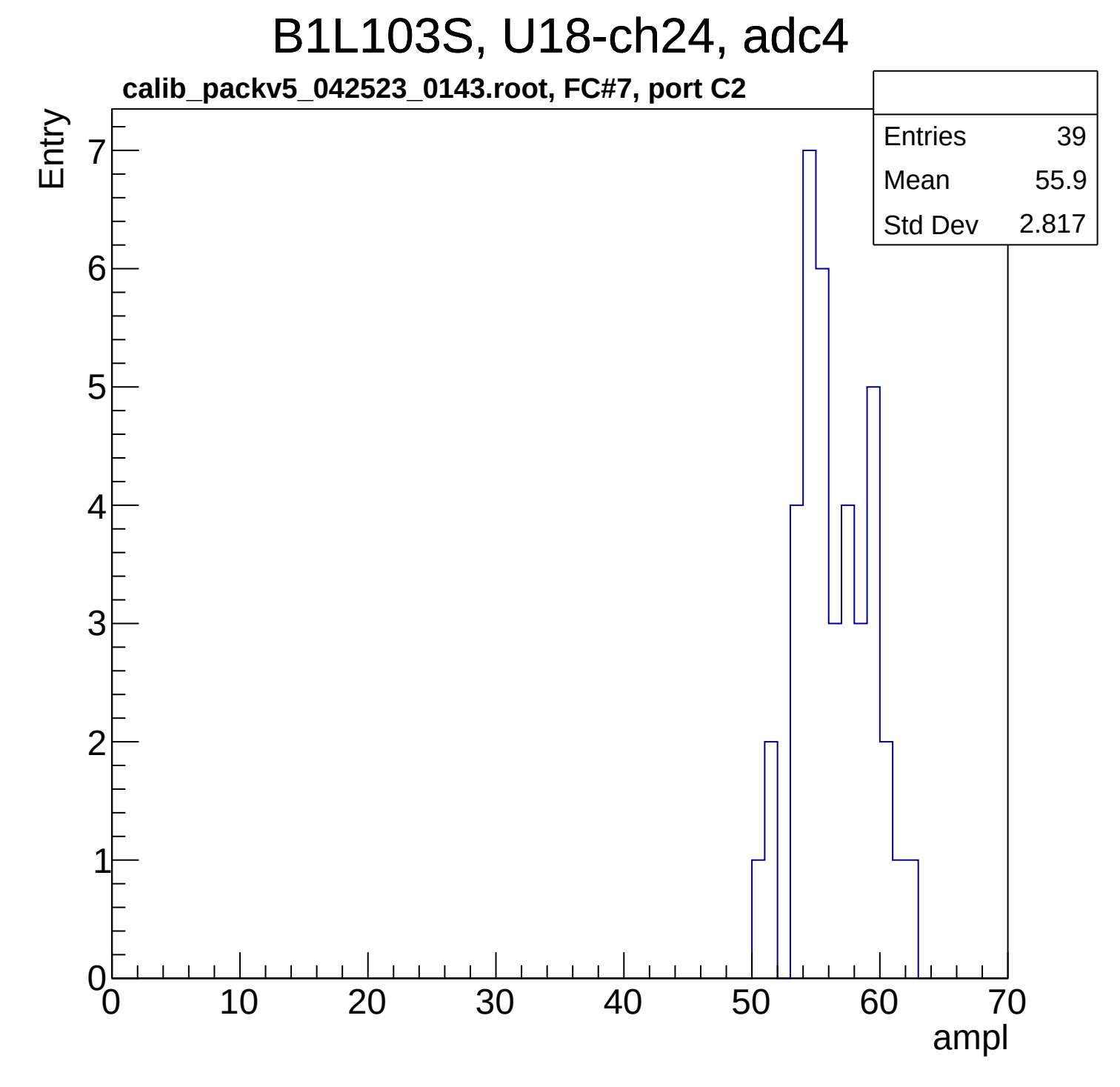
B1L103S, U18-ch24, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 39
Mean 55.9
Std Dev 2.817
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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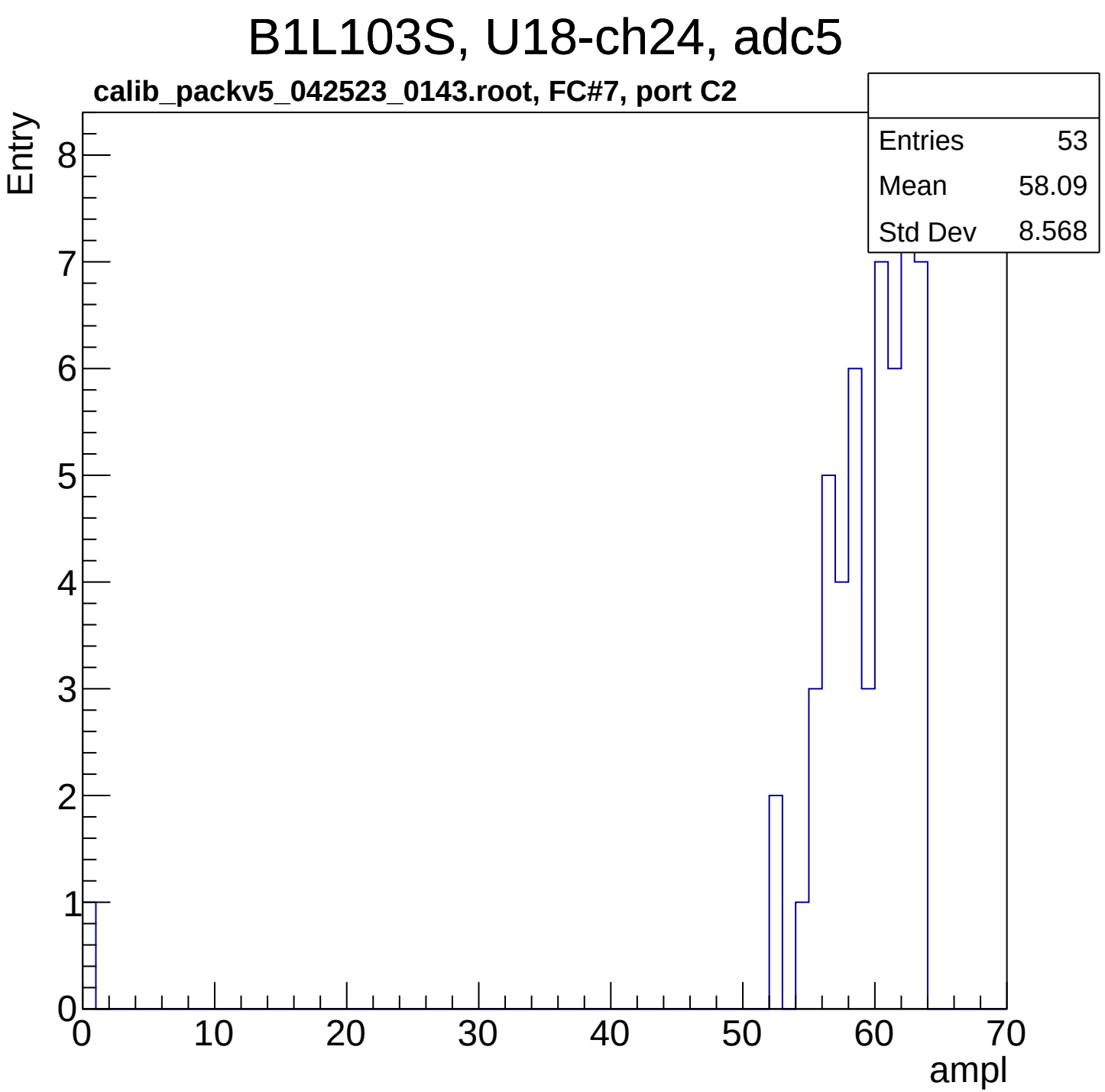
B1L103S, U18-ch24, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 58.09
Std Dev 8.568
Entry
ampl
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1
2
3
4
5
6
7
8
0
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60
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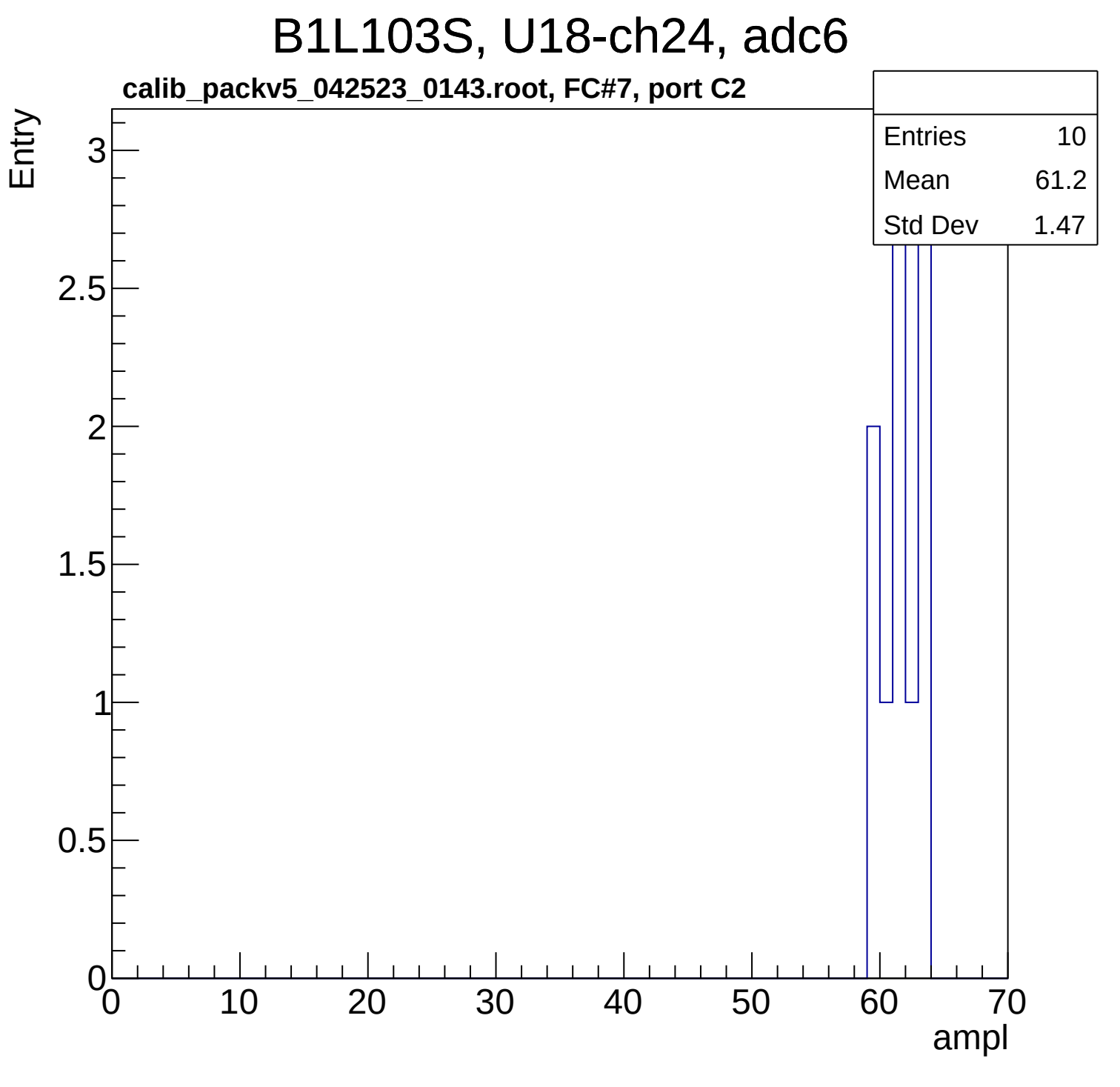
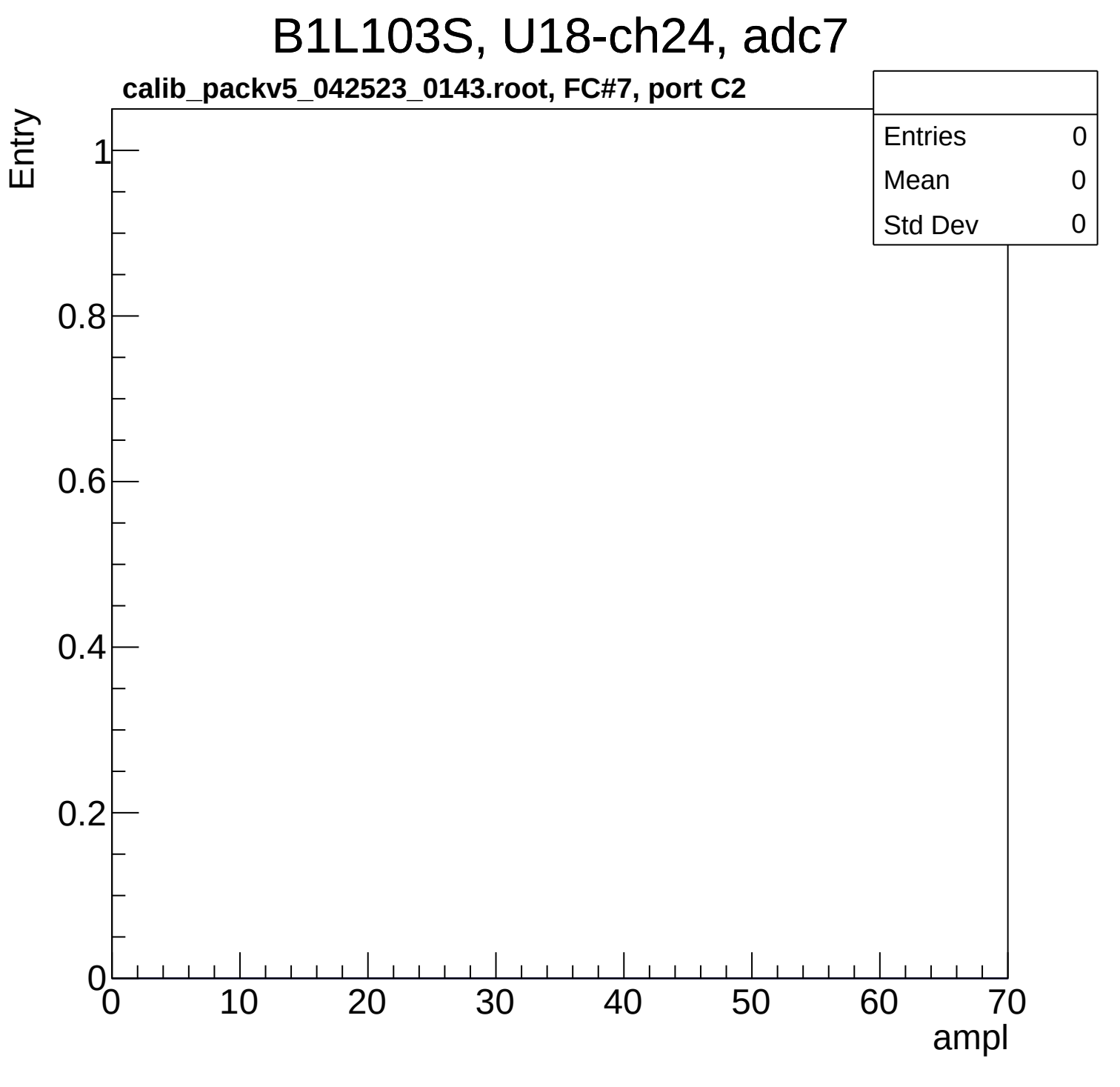
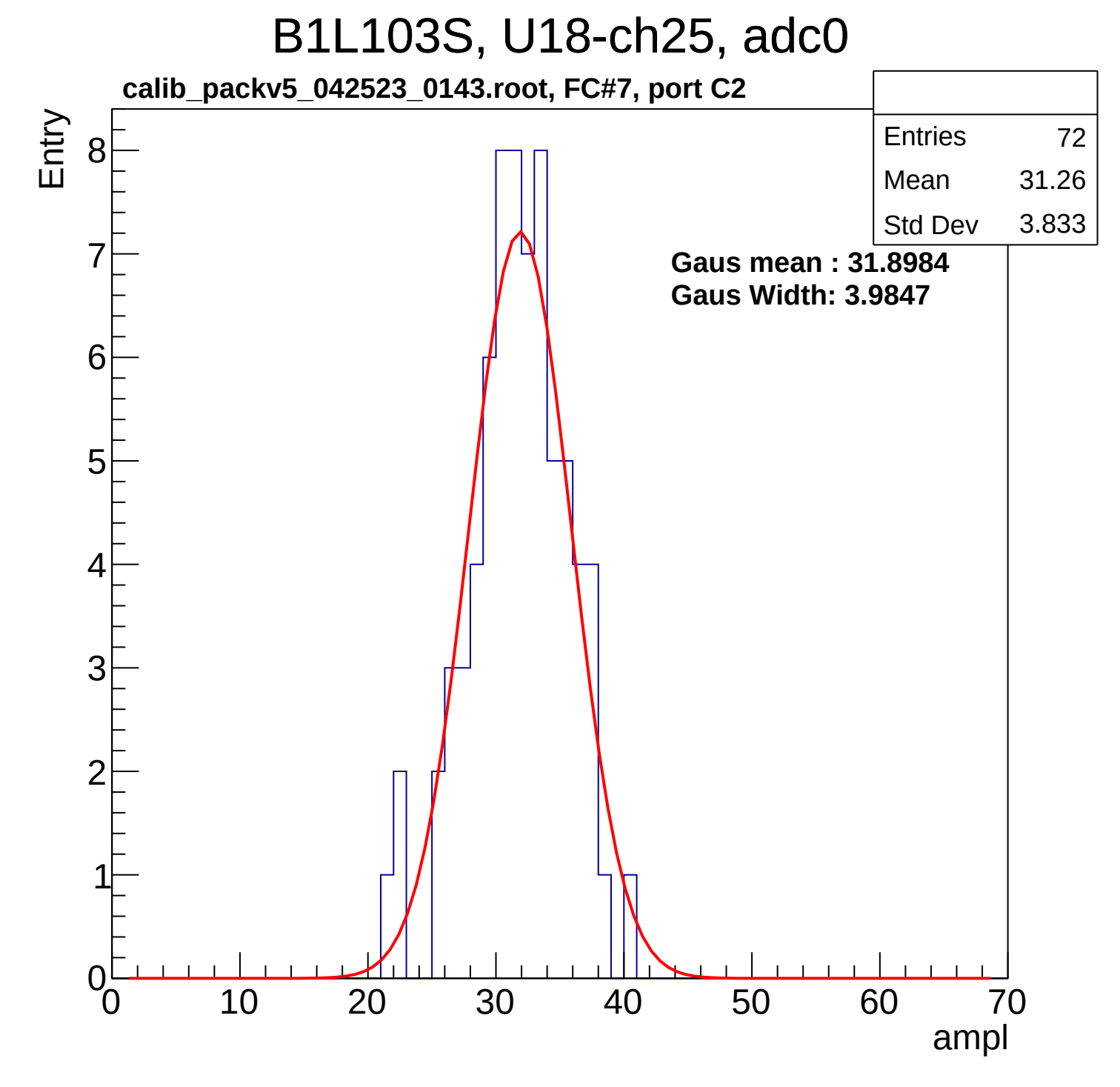

B1L103S, U18-ch24, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 10
Mean 61.2
Std Dev 1.47
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U18-ch24, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch25, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 72
Mean 31.26
Std Dev 3.833
Gaus mean : 31.8984
Gaus Width: 3.9847
Entry
ampl
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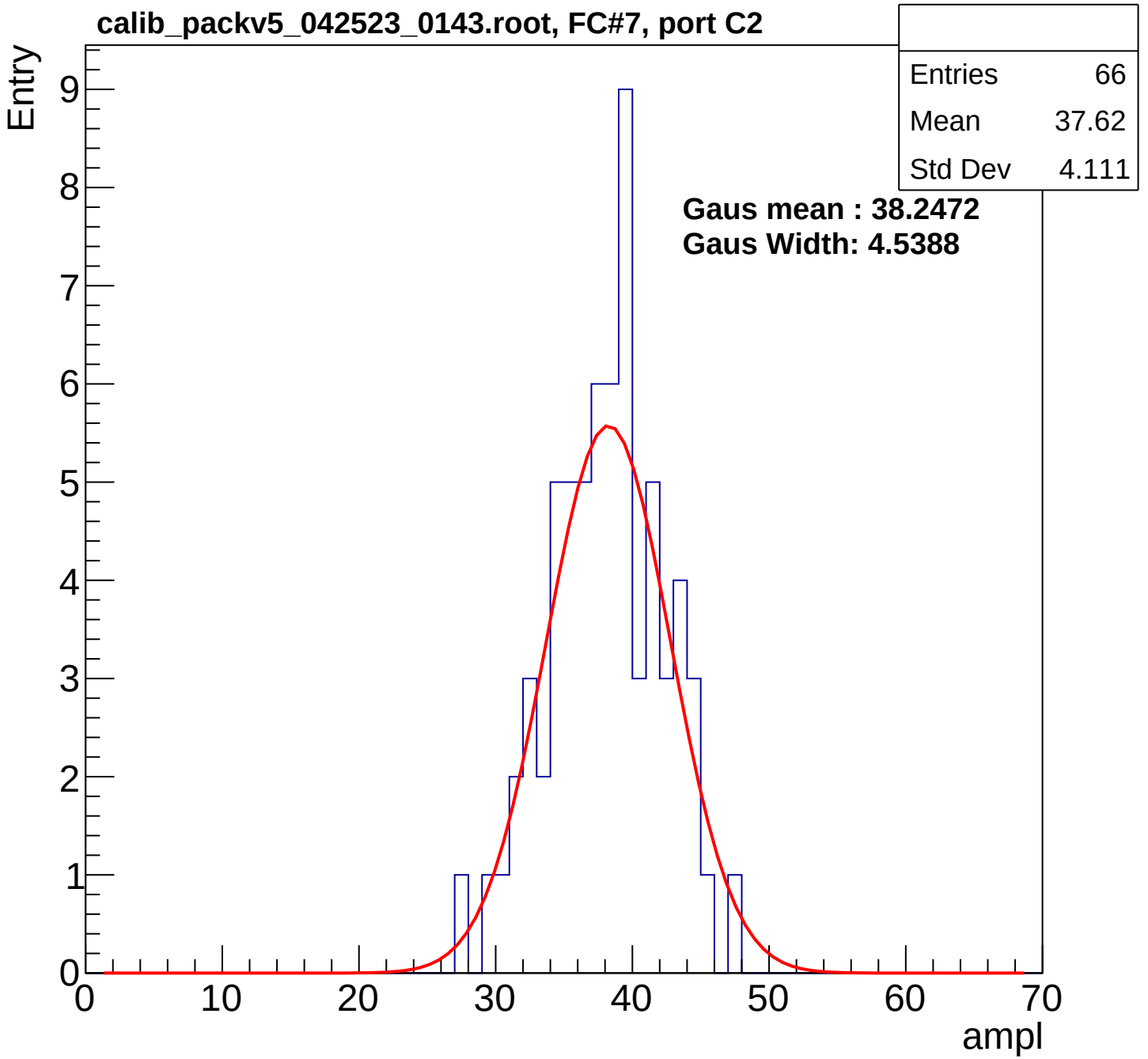
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch25, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 37.62
Std Dev 4.111
Gaus mean : 38.2472
Gaus Width: 4.5388
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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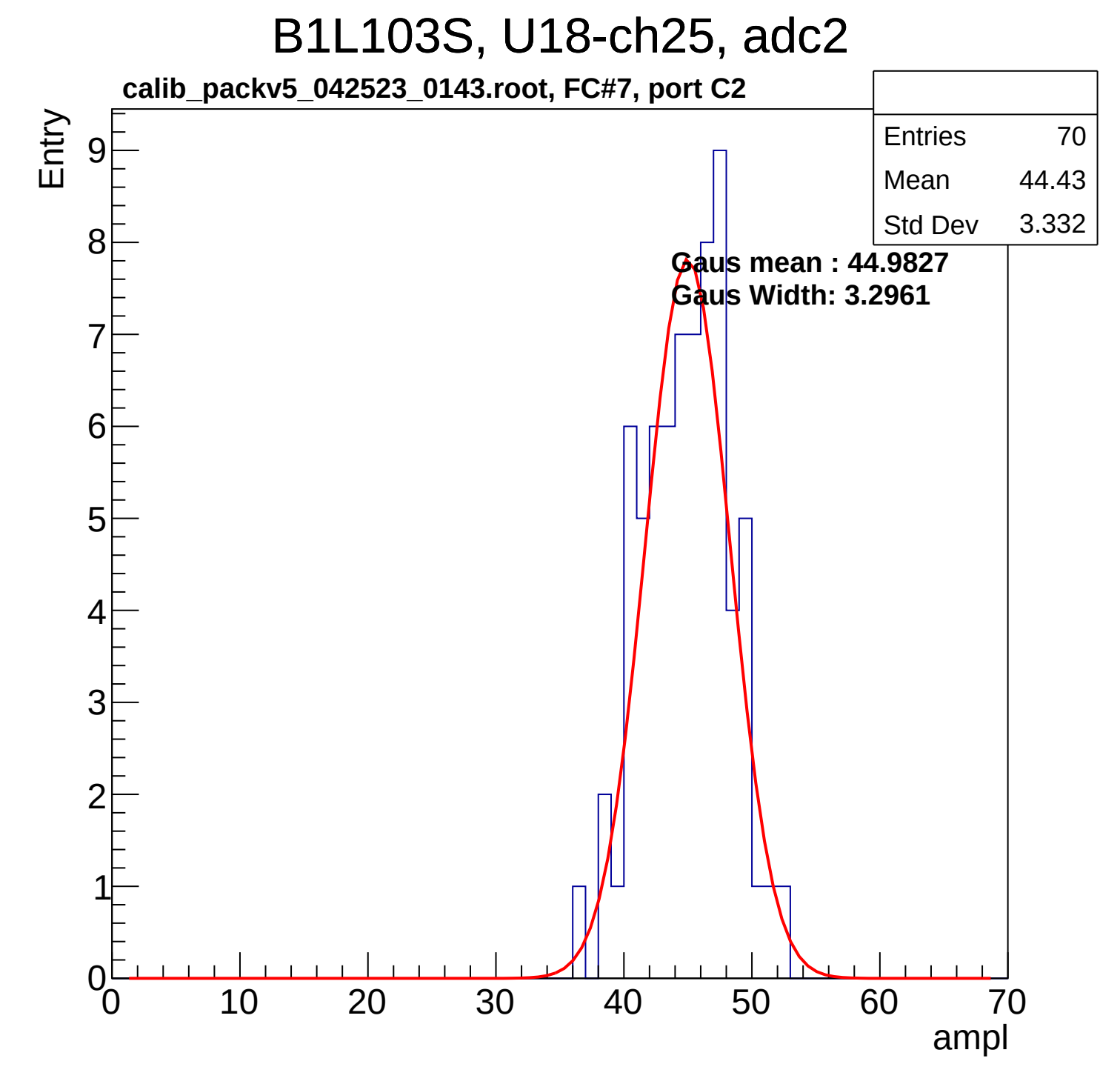
B1L103S, U18-ch25, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 44.43
Std Dev 3.332
Gaus mean : 44.9827
Gaus Width: 3.2961
Entry
ampl
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2
3
4
5
6
7
8
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0
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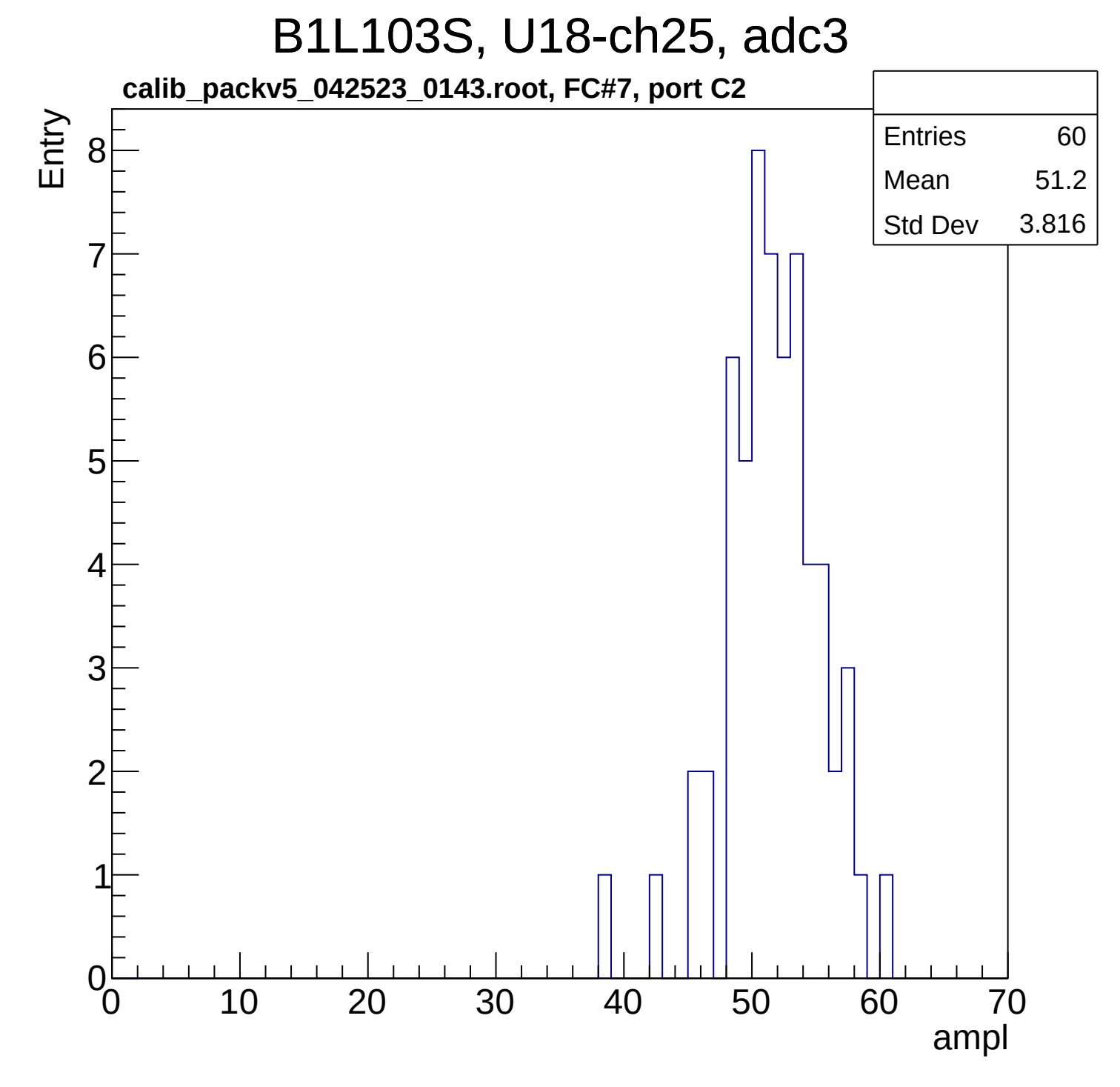
B1L103S, U18-ch25, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 60
Mean 51.2
Std Dev 3.816
Entry
ampl
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60
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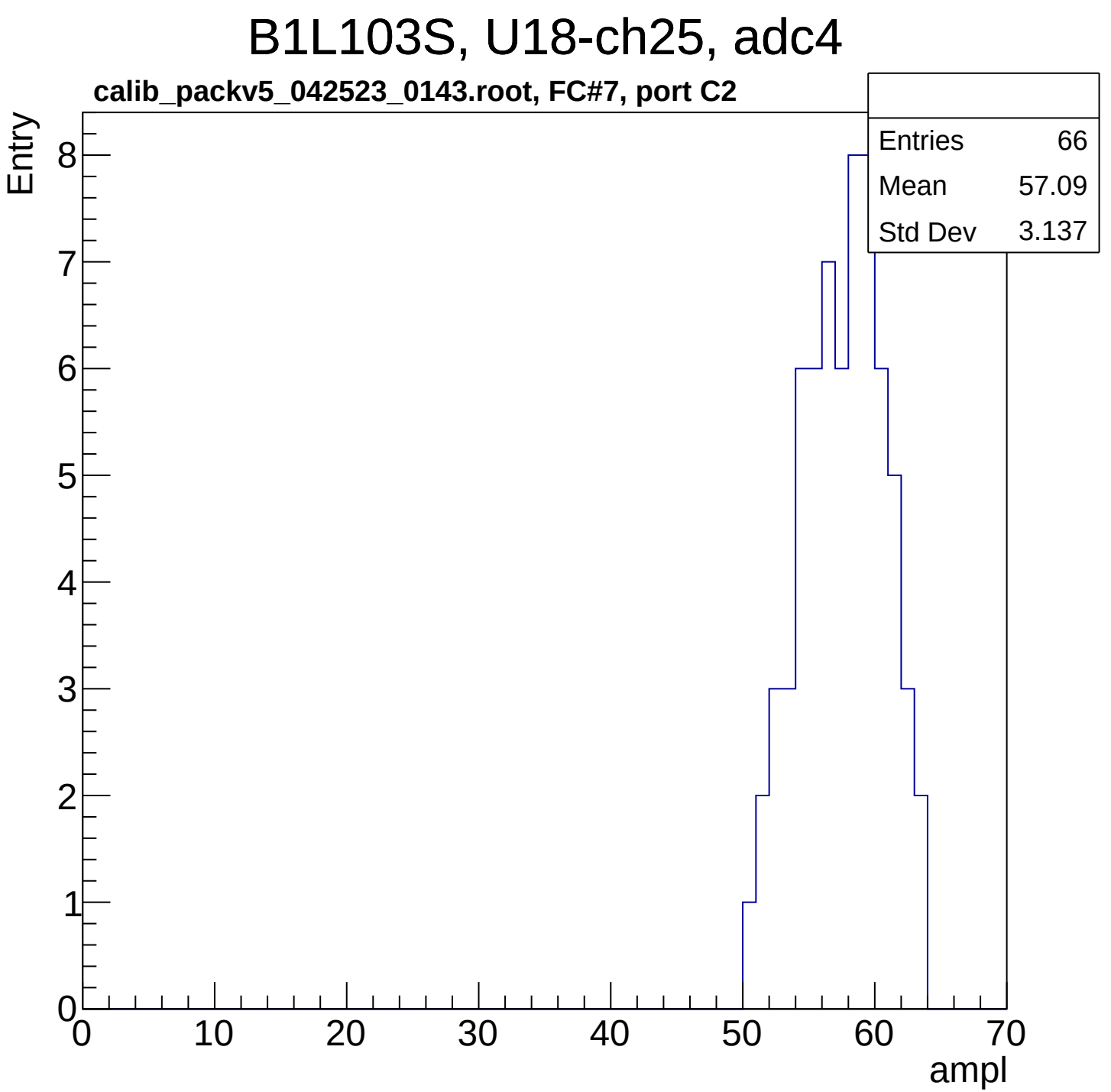
B1L103S, U18-ch25, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 57.09
Std Dev 3.137
Entry
ampl
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1
2
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4
5
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0
10
20
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40
50
60
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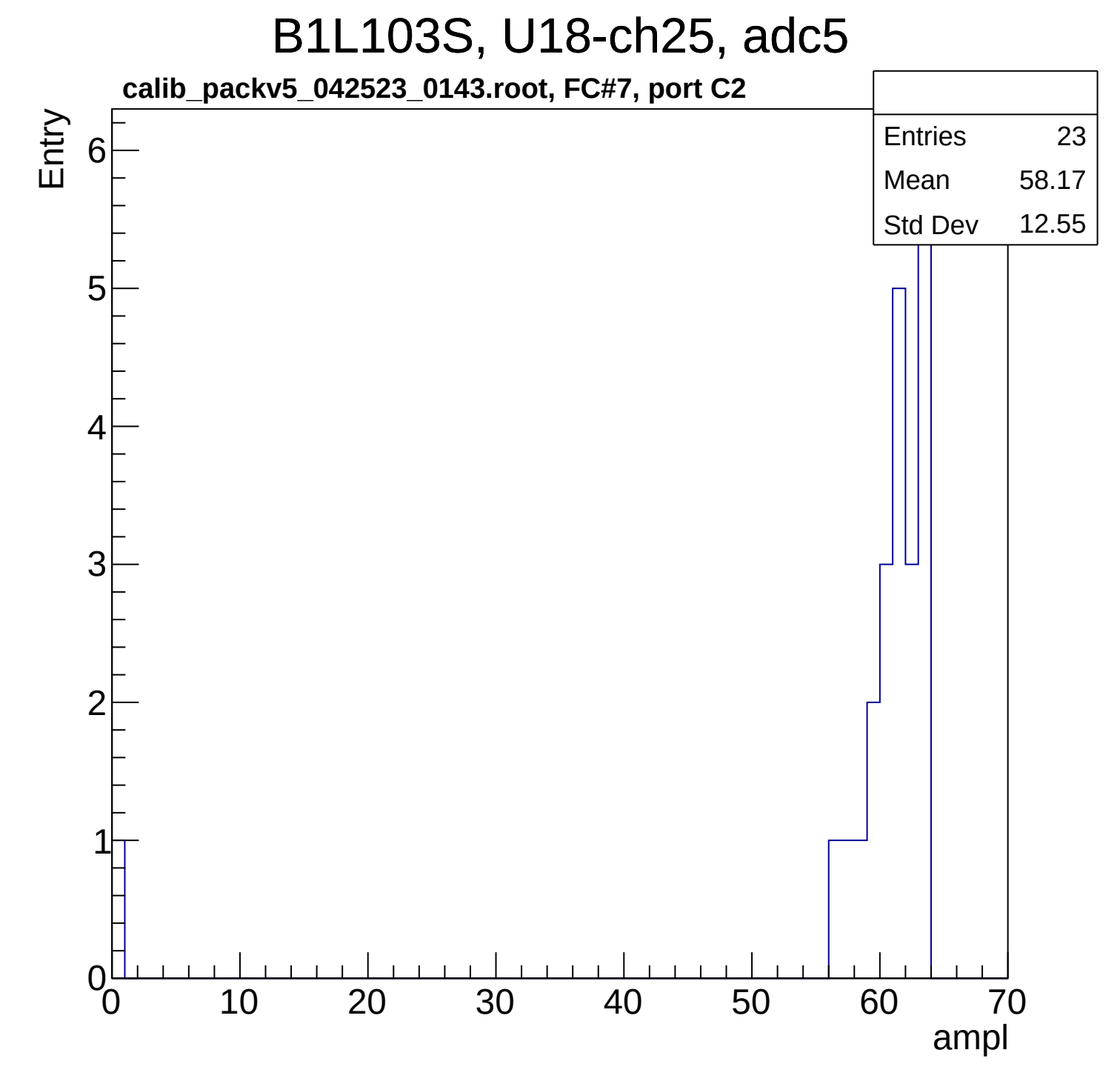
B1L103S, U18-ch25, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 23
Mean 58.17
Std Dev 12.55
Entry
0
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2
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4
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10
20
30
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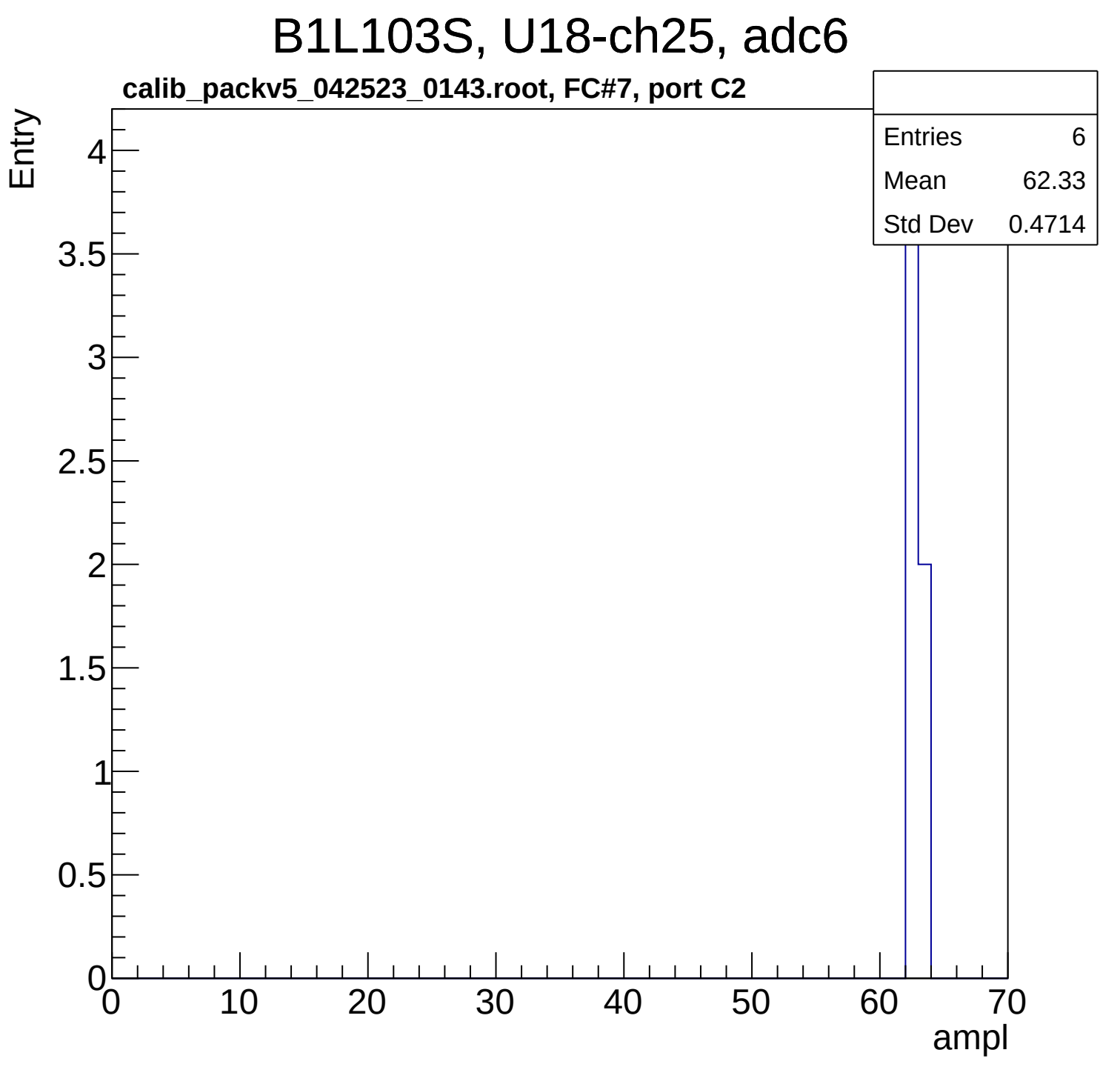
50
60
70
ampl


B1L103S, U18-ch25, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 6
Mean 62.33
Std Dev 0.4714
Entry
ampl
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1
1.5
2
2.5
3
3.5
4
0
10
20
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40
50
60
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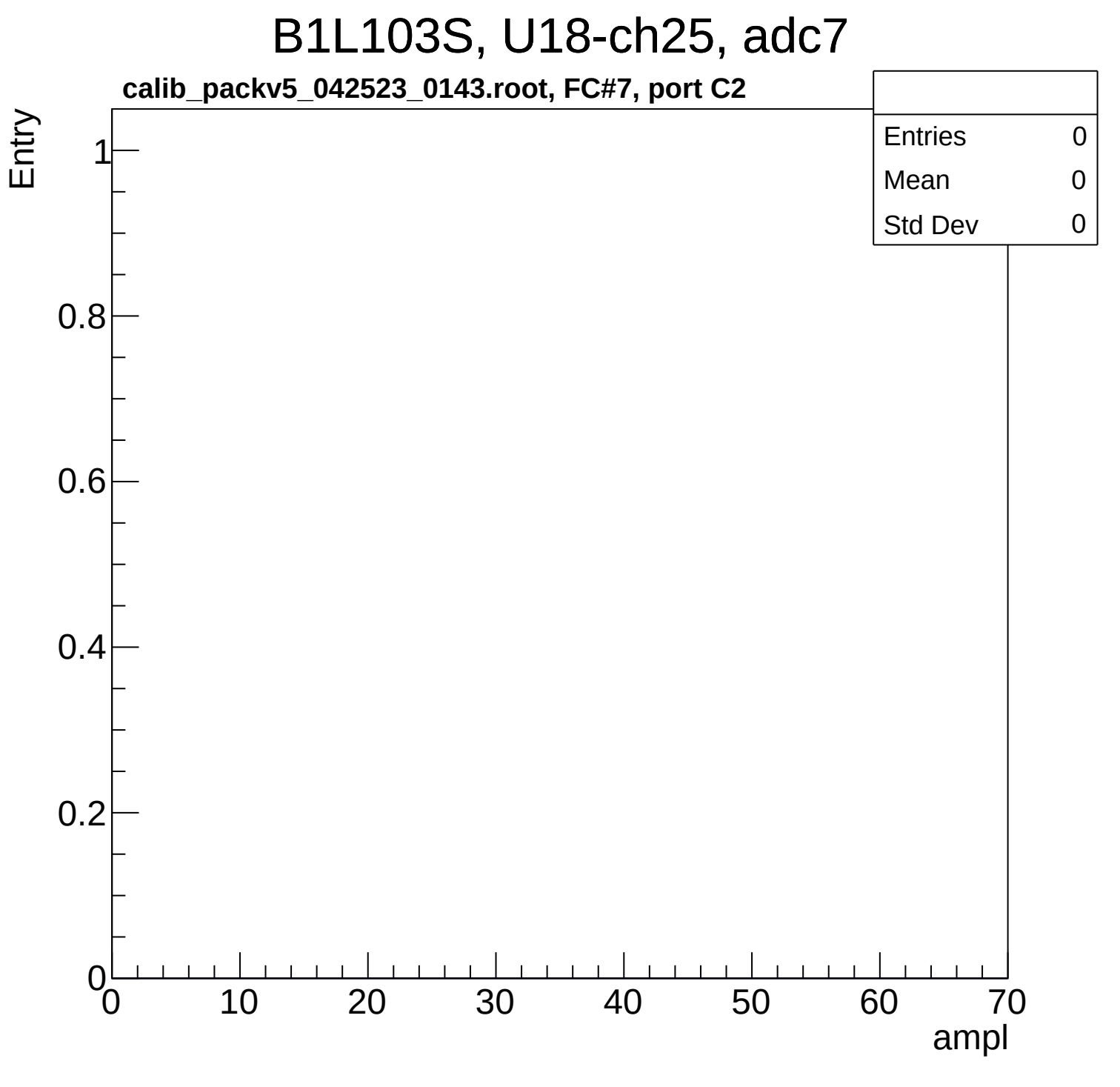
B1L103S, U18-ch25, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
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0.6
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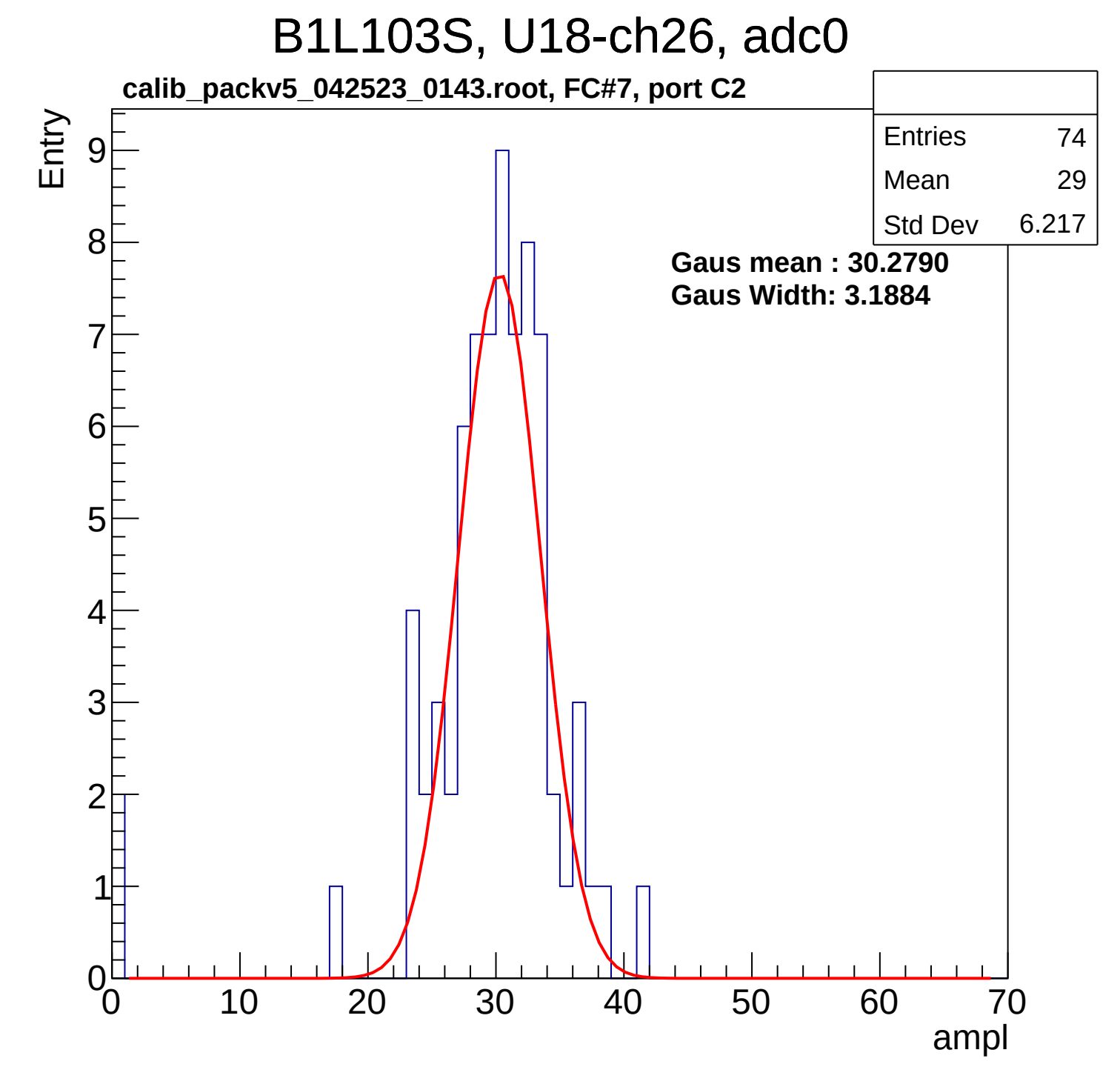
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch26, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 74
Mean 29
Std Dev 6.217
Gaus mean : 30.2790
Gaus Width: 3.1884
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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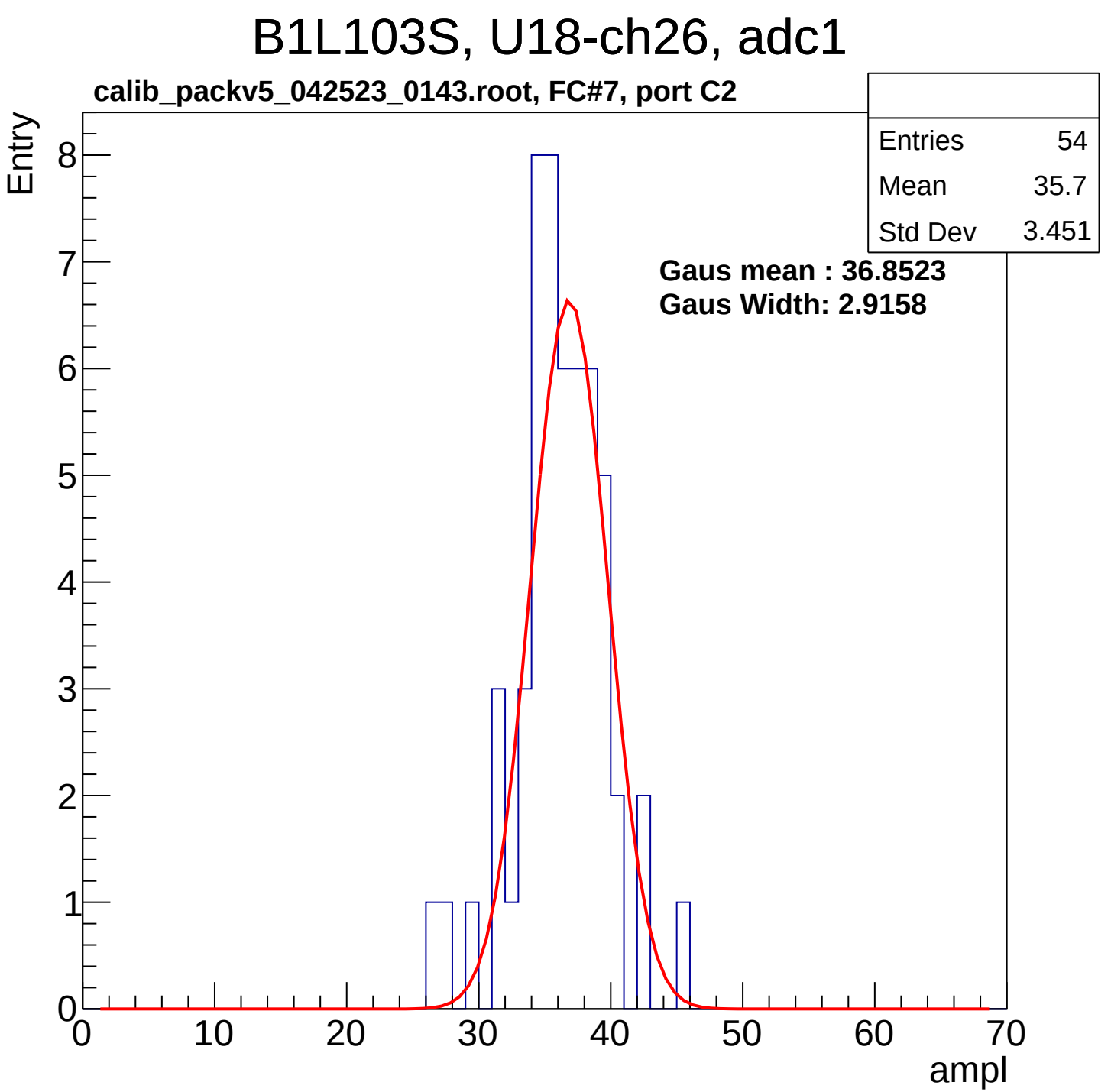
B1L103S, U18-ch26, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 54
Mean 35.7
Std Dev 3.451
Gaus mean : 36.8523
Gaus Width: 2.9158
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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40
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60
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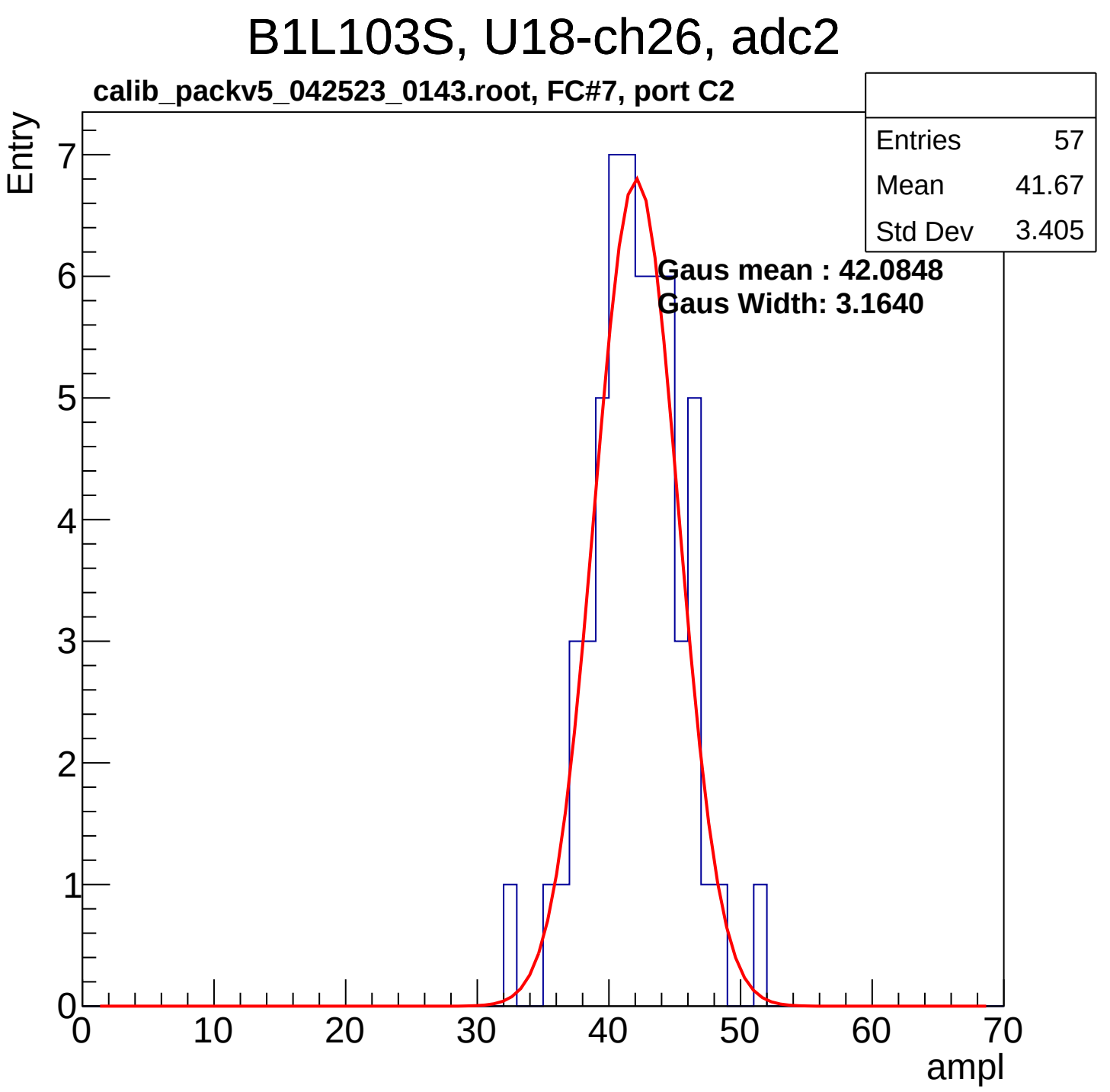
B1L103S, U18-ch26, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 41.67
Std Dev 3.405
Gaus mean : 42.0848
Gaus Width: 3.1640
Entry
ampl
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1
2
3
4
5
6
7
0
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40
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60
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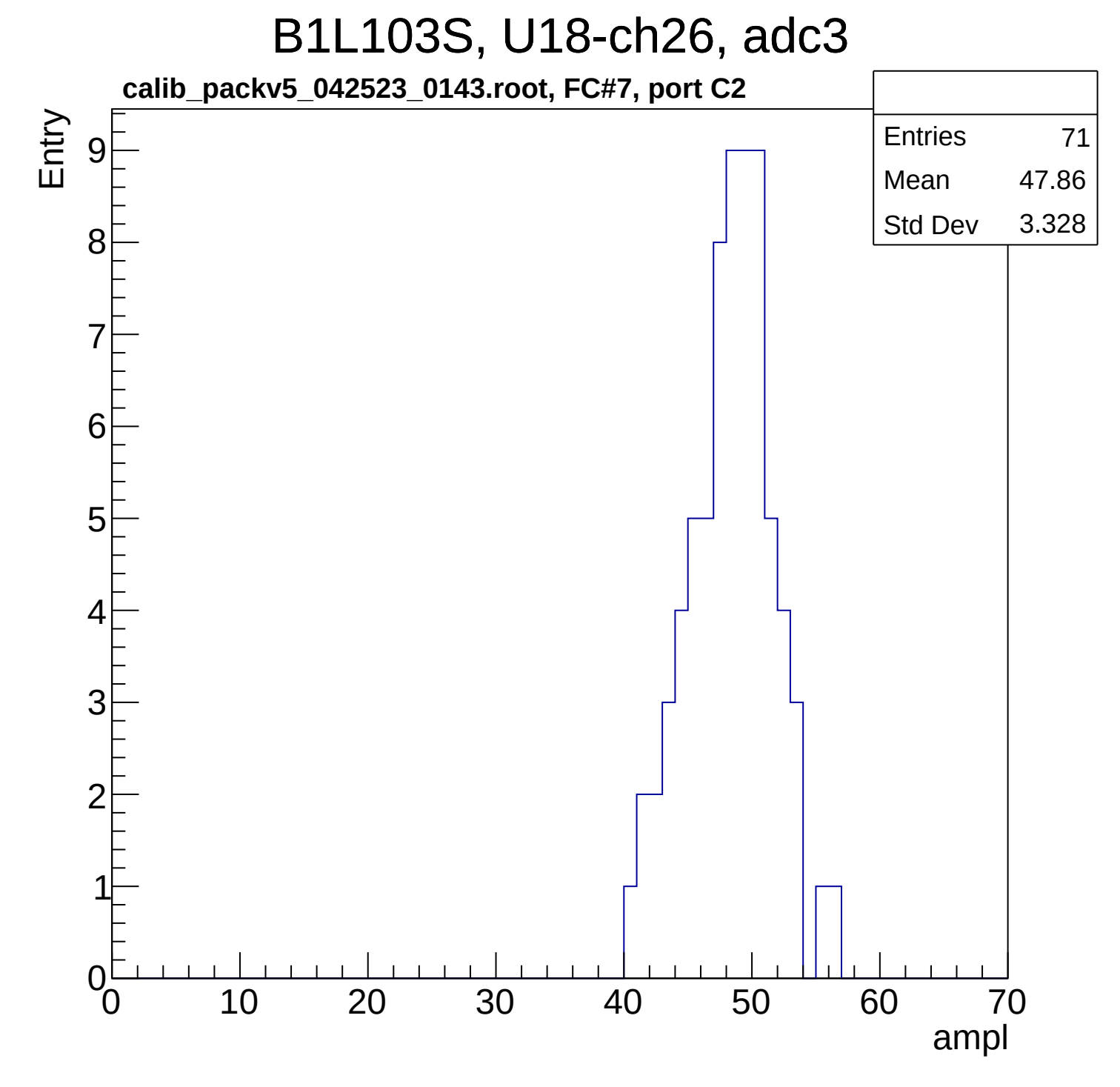
B1L103S, U18-ch26, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 71
Mean 47.86
Std Dev 3.328
Entry
ampl
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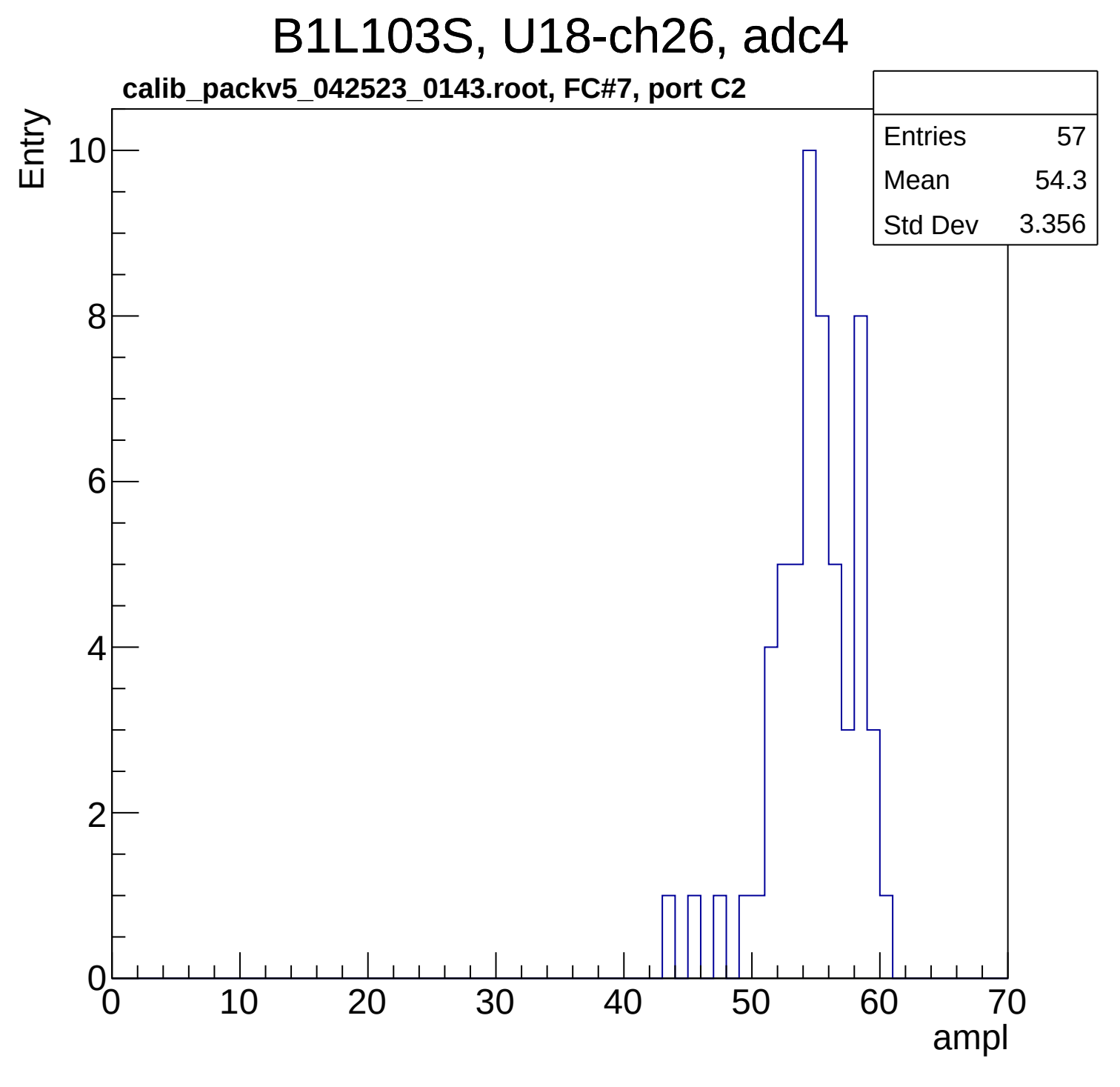
B1L103S, U18-ch26, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 54.3
Std Dev 3.356
Entry
ampl
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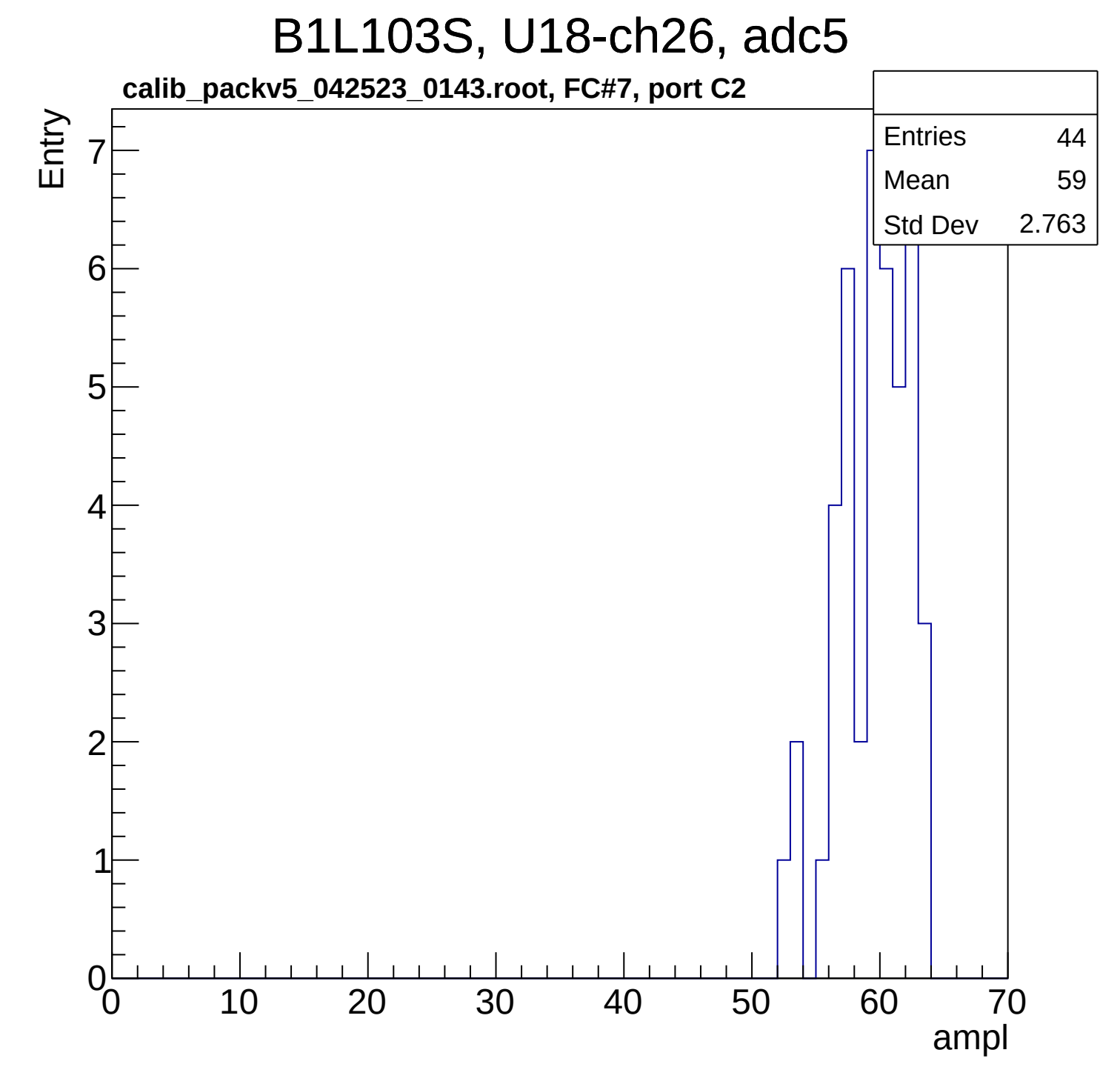
B1L103S, U18-ch26, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 44
Mean 59
Std Dev 2.763
Entry
ampl
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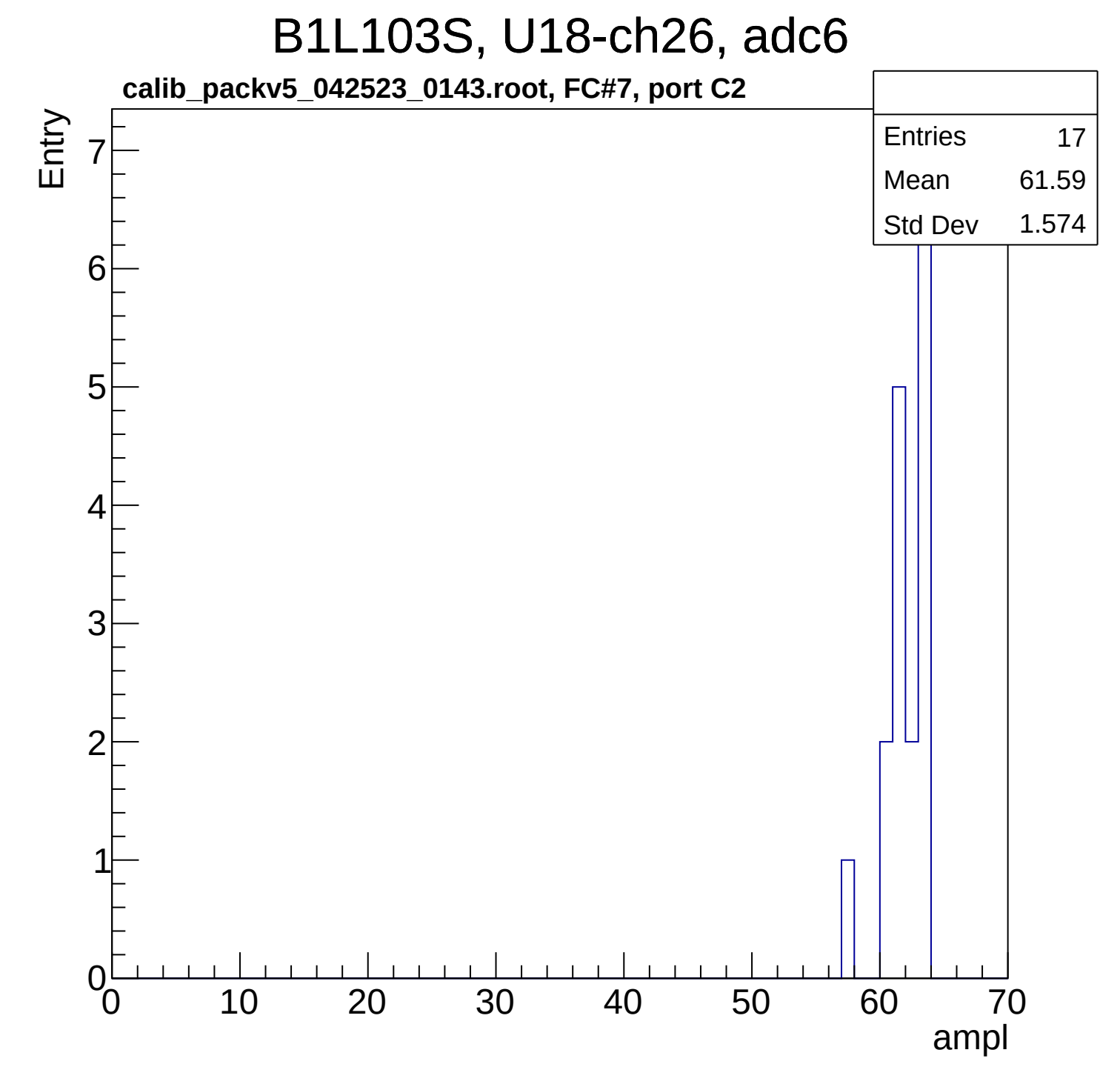
B1L103S, U18-ch26, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 17
Mean 61.59
Std Dev 1.574
Entry
ampl
0
1
2
3
4
5
6
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0
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20
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40
50
60
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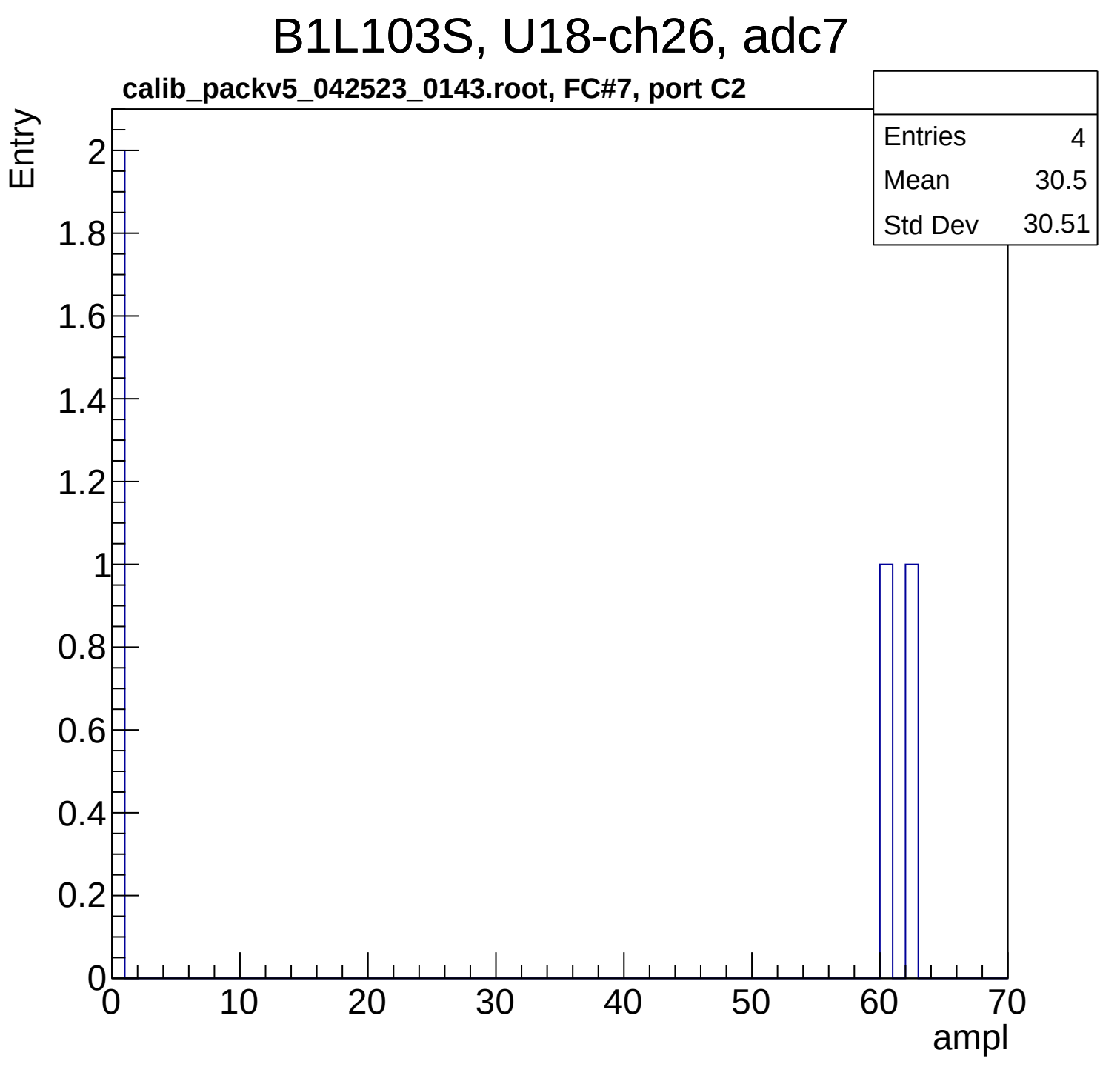
B1L103S, U18-ch26, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 4
Mean 30.5
Std Dev 30.51
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
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60
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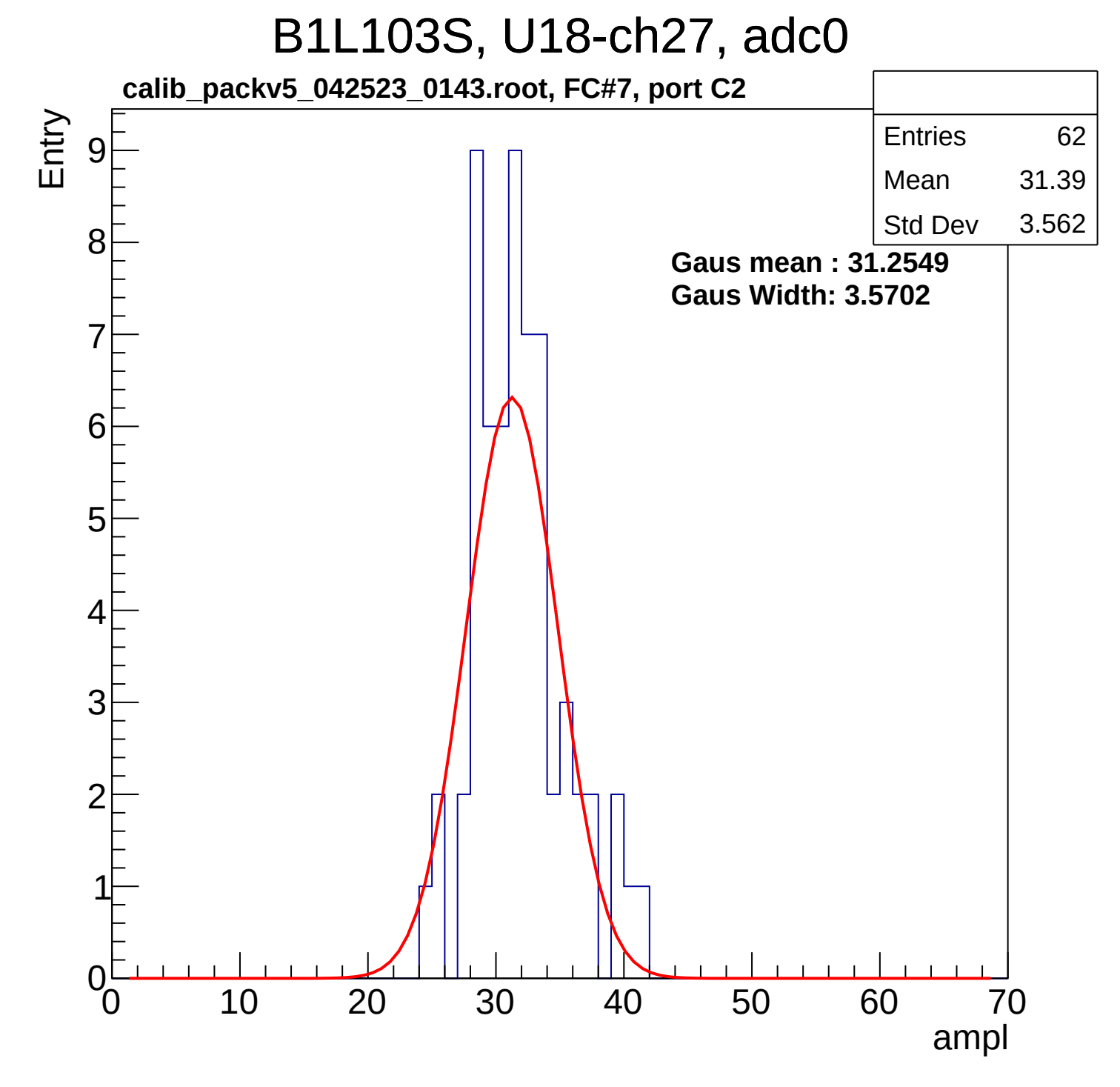
B1L103S, U18-ch27, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 62
Mean 31.39
Std Dev 3.562
Gaus mean : 31.2549
Gaus Width: 3.5702
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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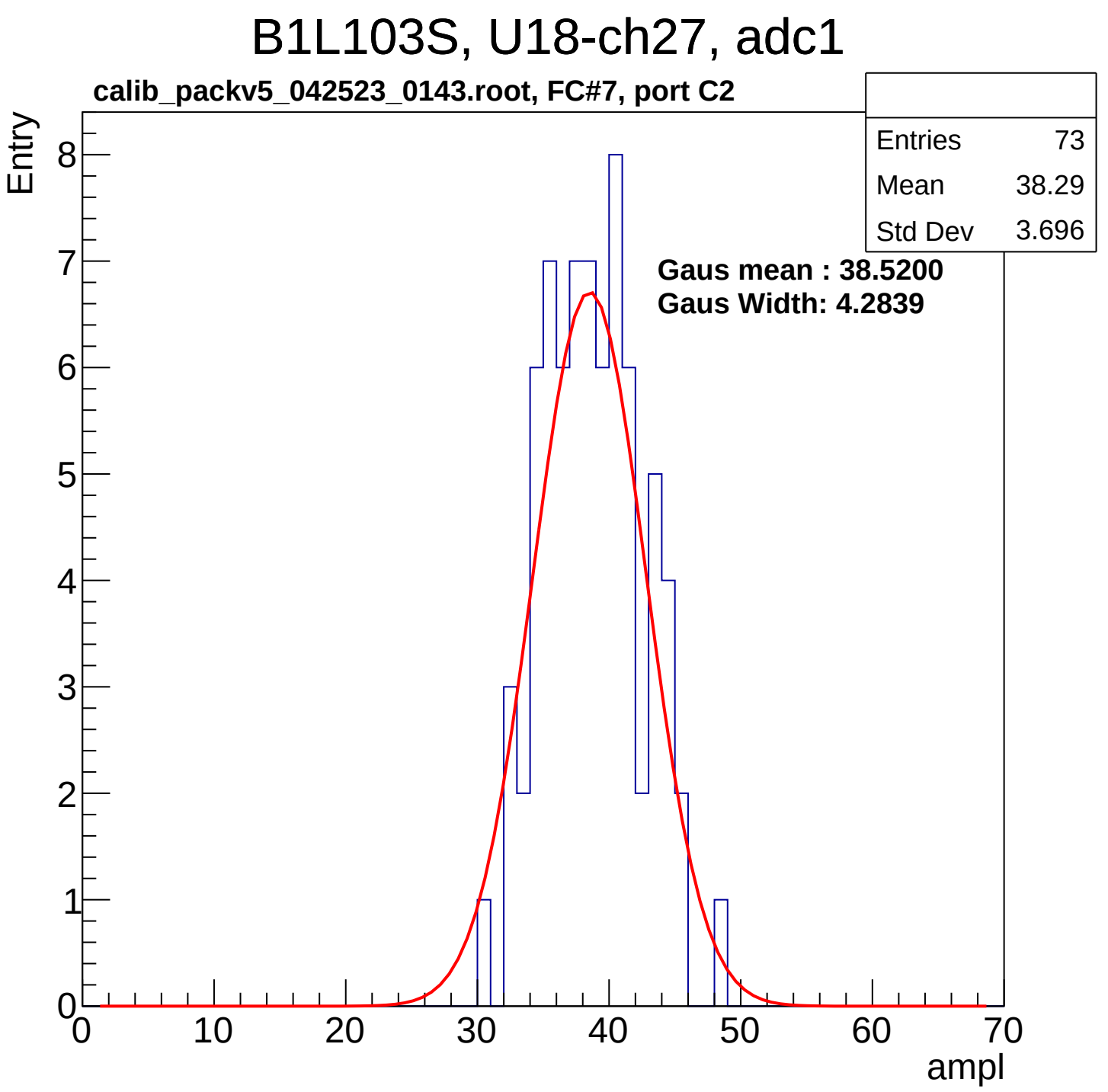
B1L103S, U18-ch27, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 73
Mean 38.29
Std Dev 3.696
Gaus mean : 38.5200
Gaus Width: 4.2839
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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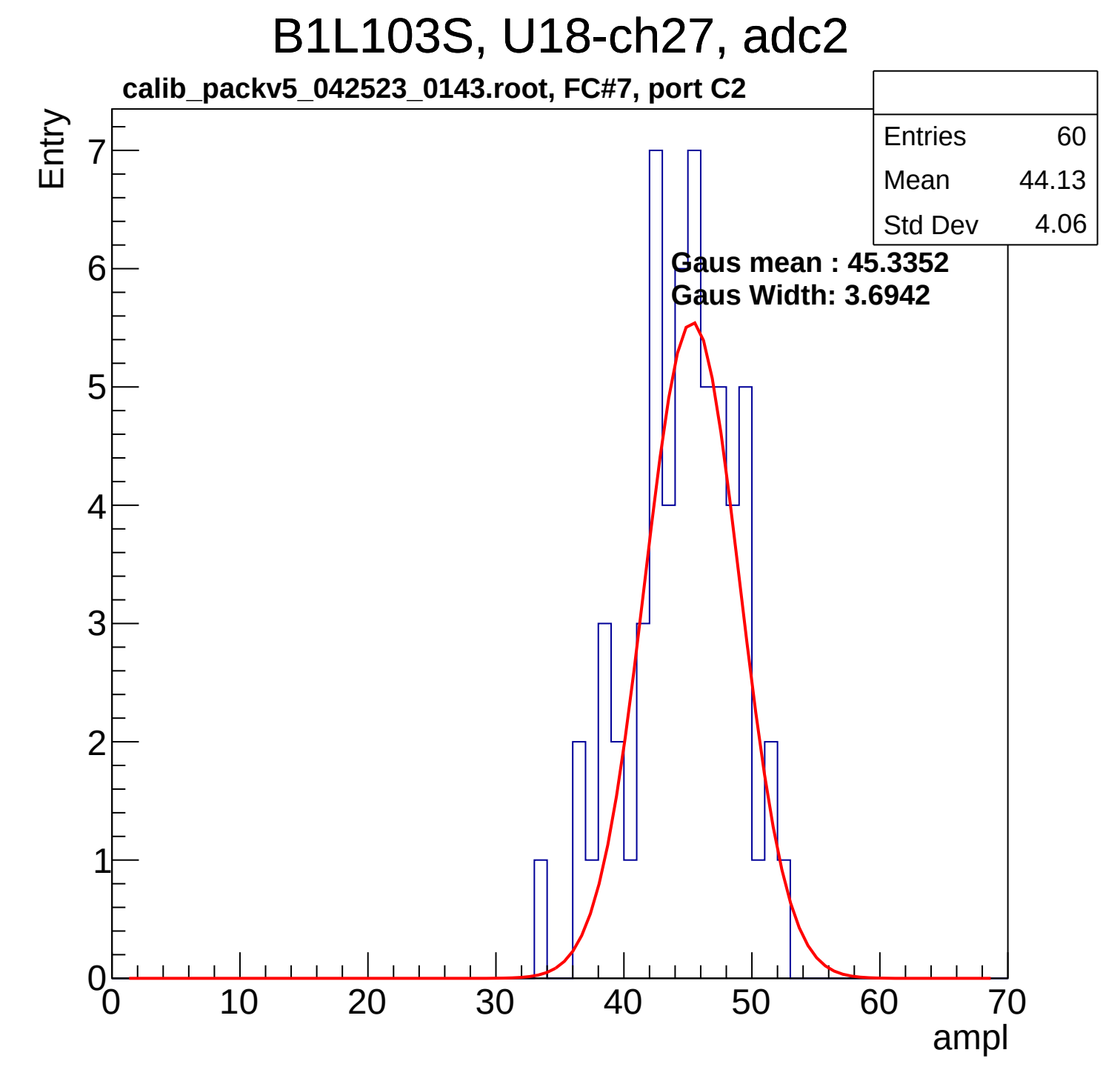
B1L103S, U18-ch27, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 60
Mean 44.13
Std Dev 4.06
Gaus mean : 45.3352
Gaus Width: 3.6942
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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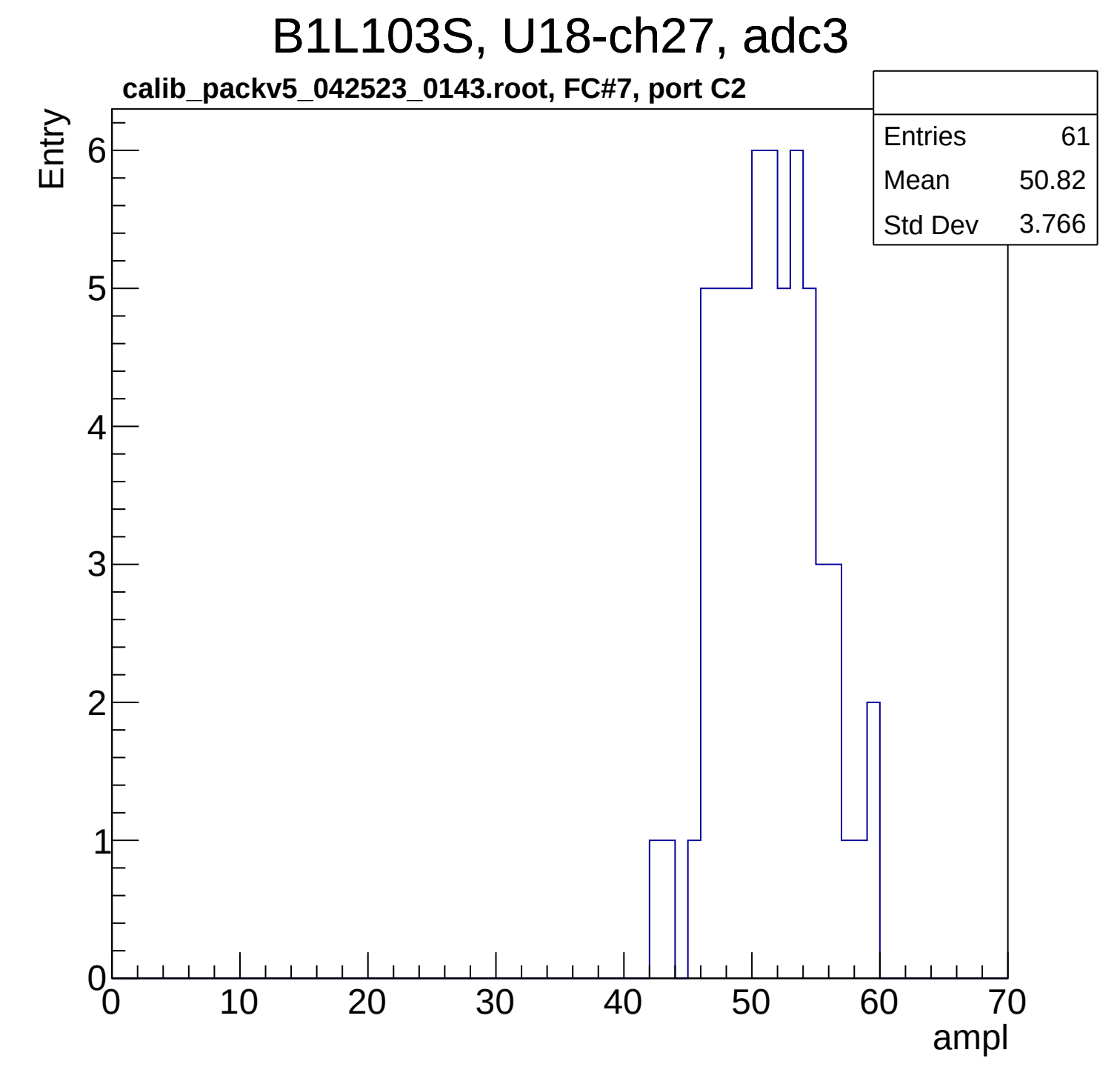
B1L103S, U18-ch27, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 61
Mean 50.82
Std Dev 3.766
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
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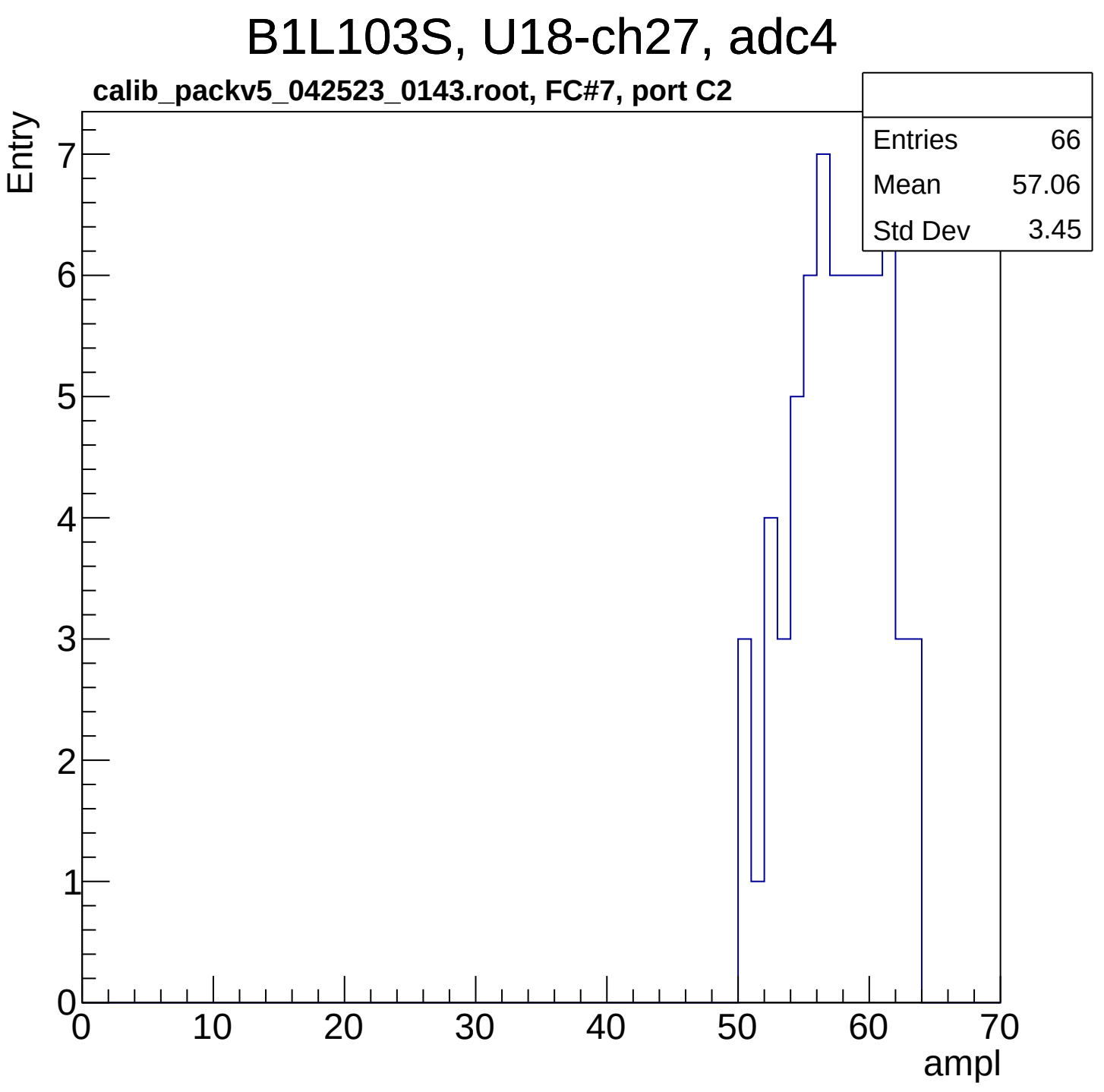
B1L103S, U18-ch27, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 57.06
Std Dev 3.45
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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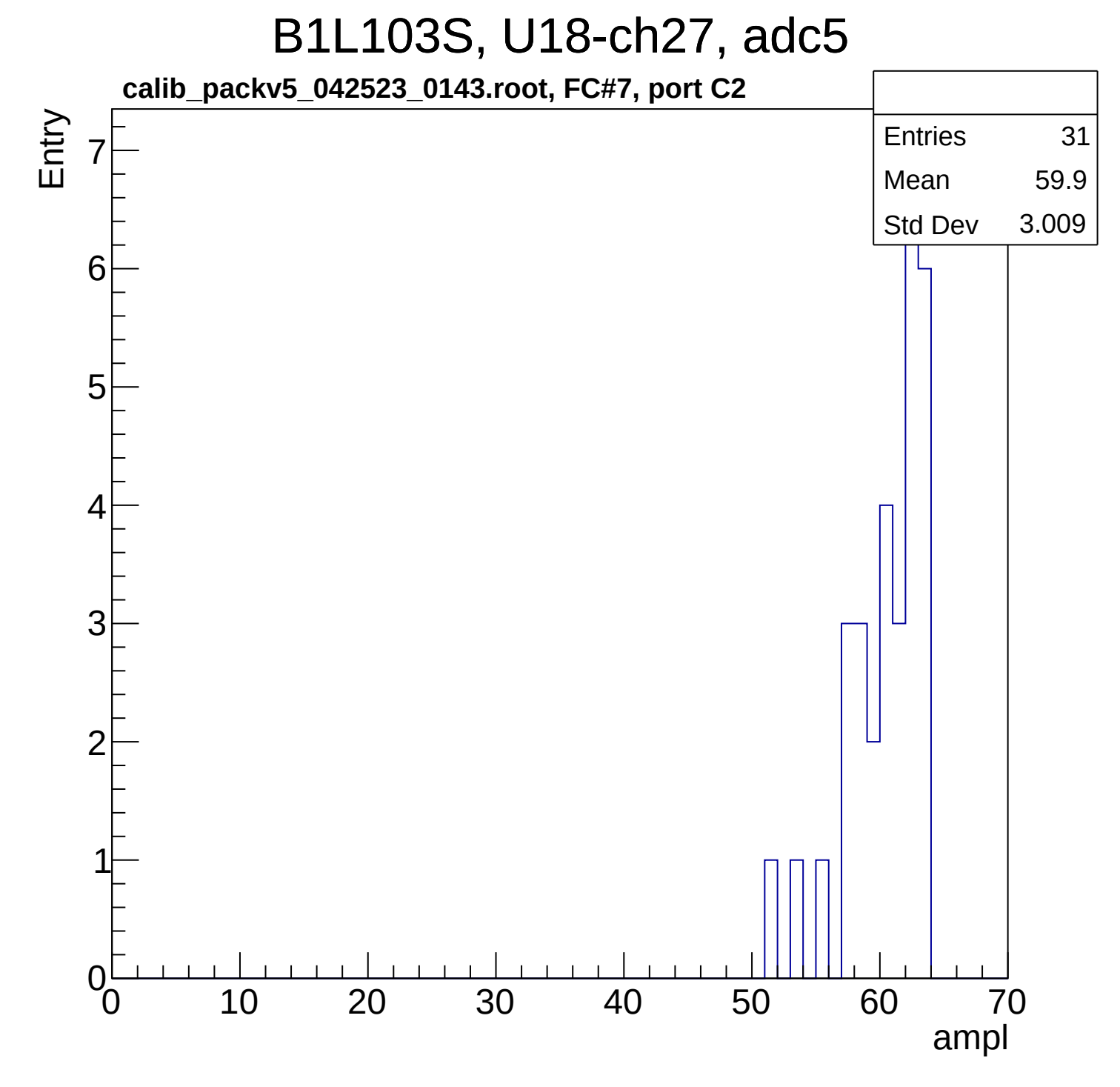
B1L103S, U18-ch27, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 31
Mean 59.9
Std Dev 3.009
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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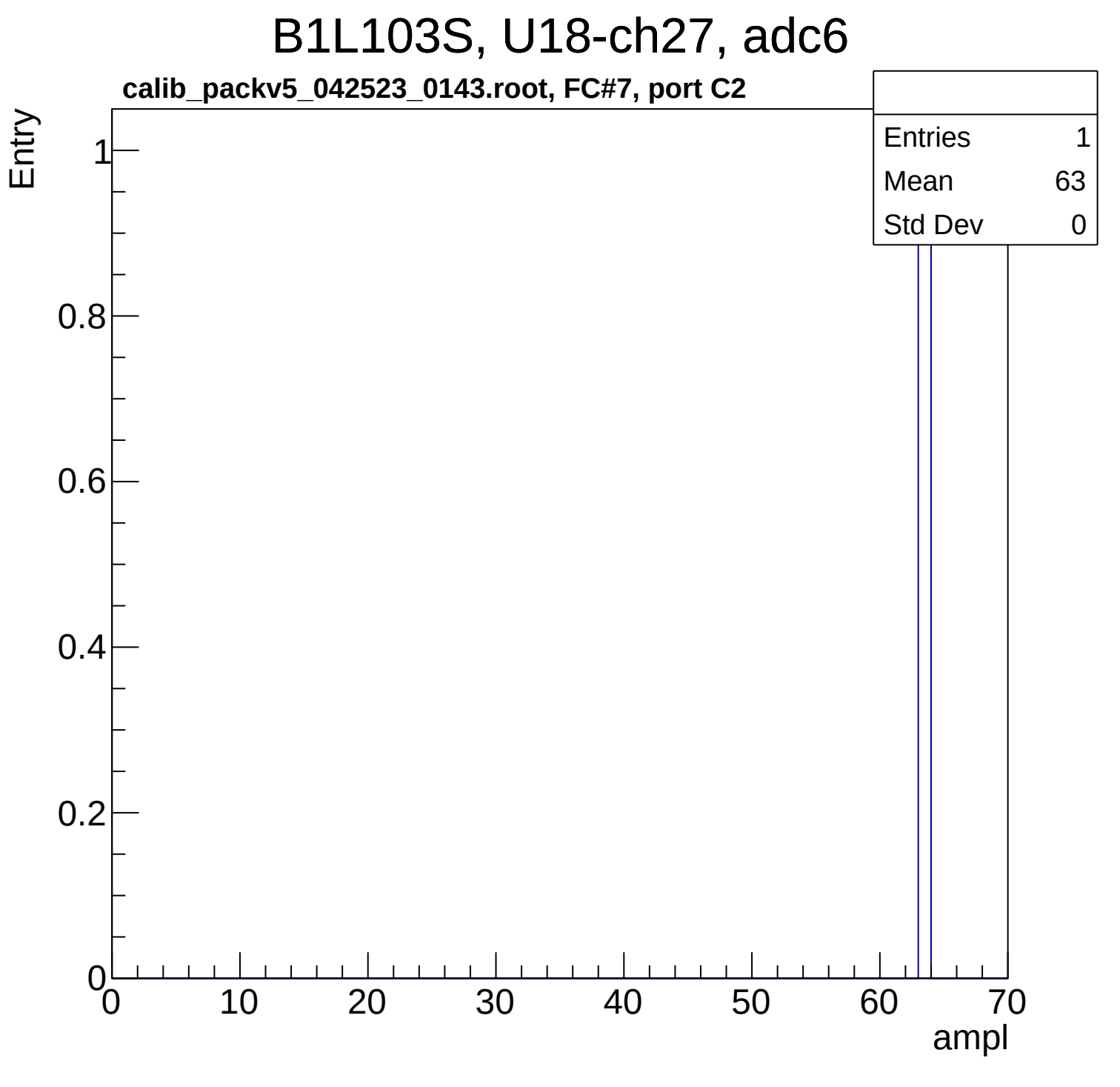
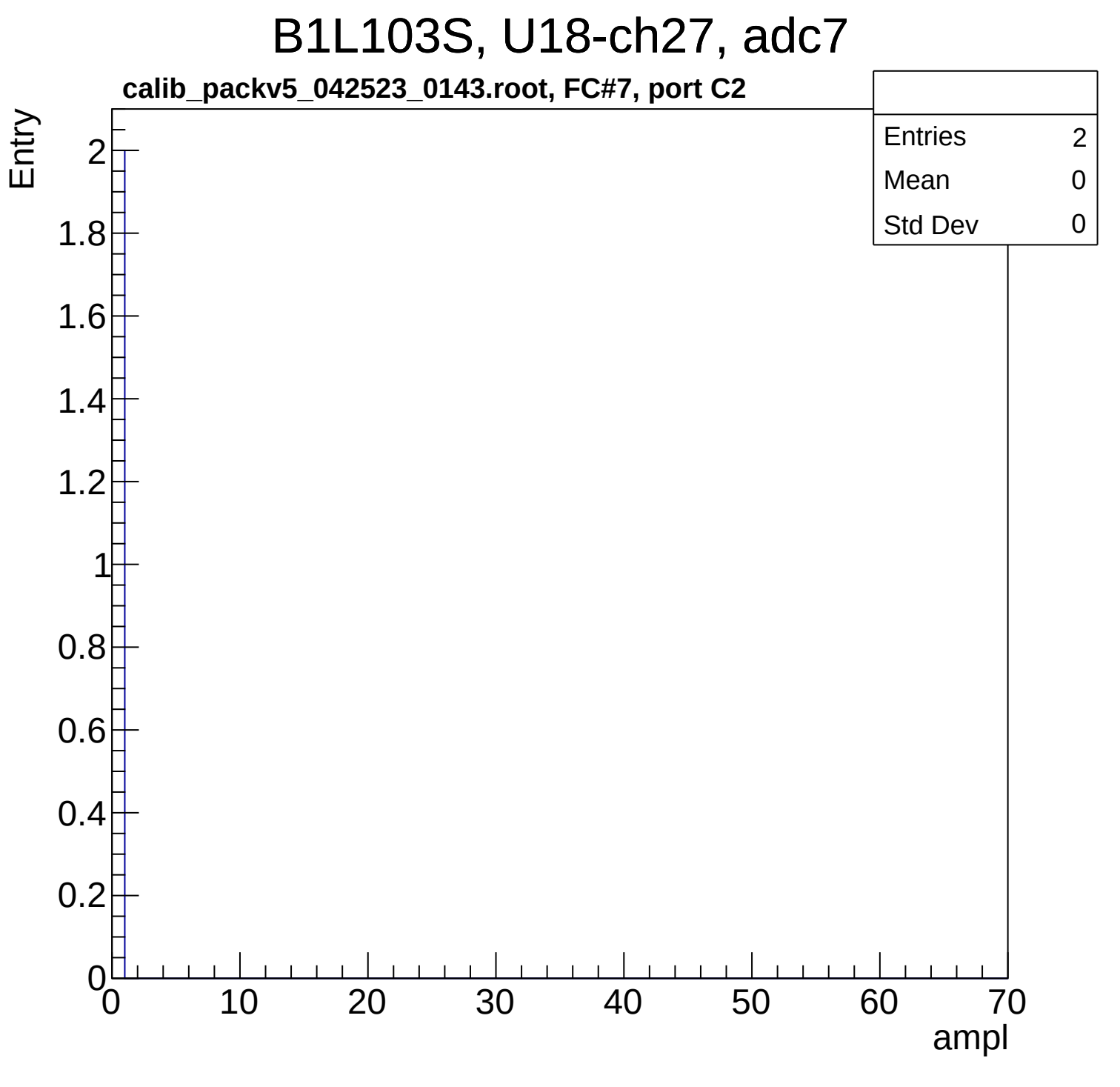
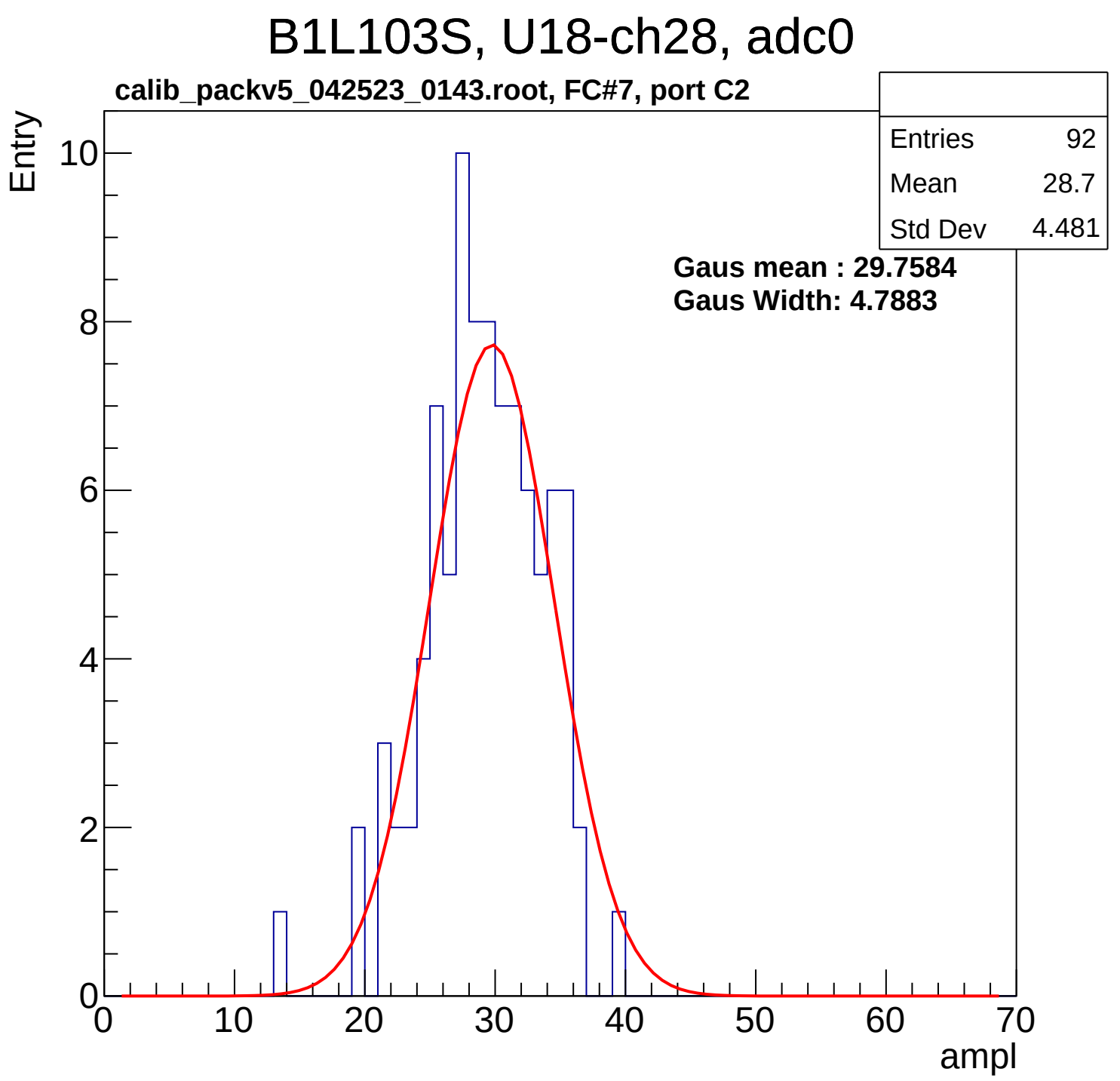
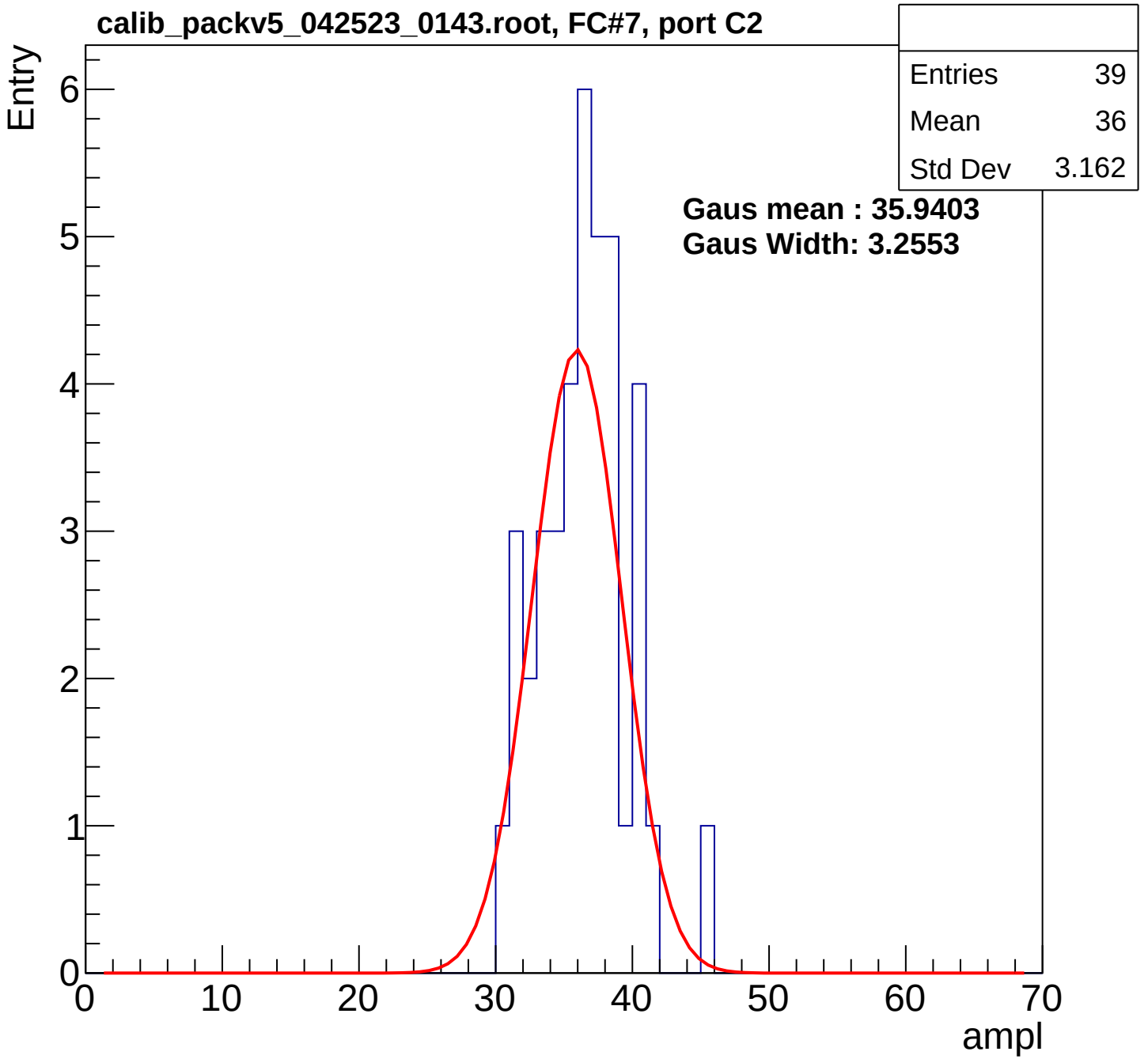

B1L103S, U18-ch27, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch27, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch28, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 92
Mean 28.7
Std Dev 4.481
Gaus mean : 29.7584
Gaus Width: 4.7883
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch28, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 39
Mean 36
Std Dev 3.162
Gaus mean : 35.9403
Gaus Width: 3.2553
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
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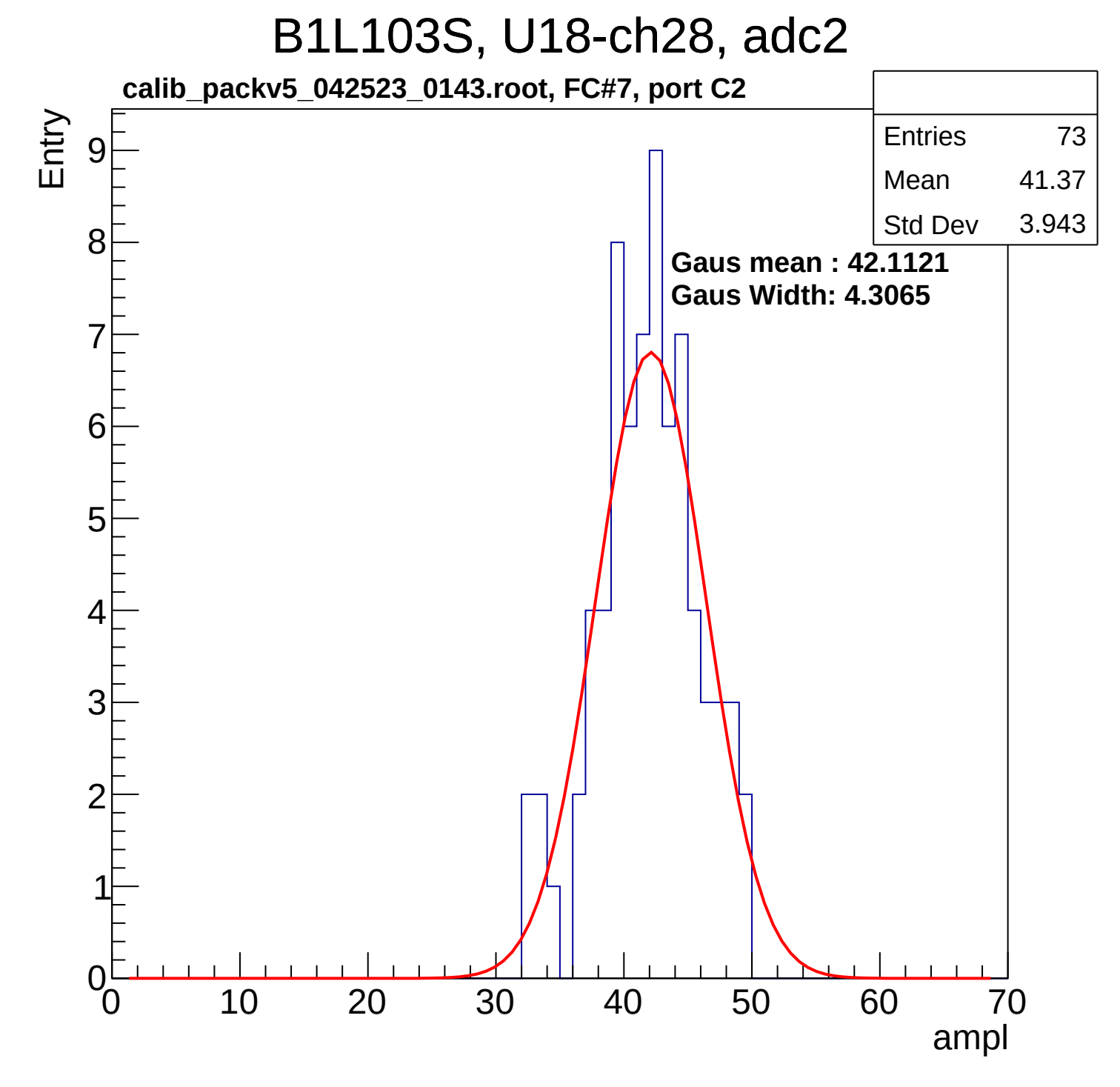
B1L103S, U18-ch28, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 73
Mean 41.37
Std Dev 3.943
Gaus mean : 42.1121
Gaus Width: 4.3065
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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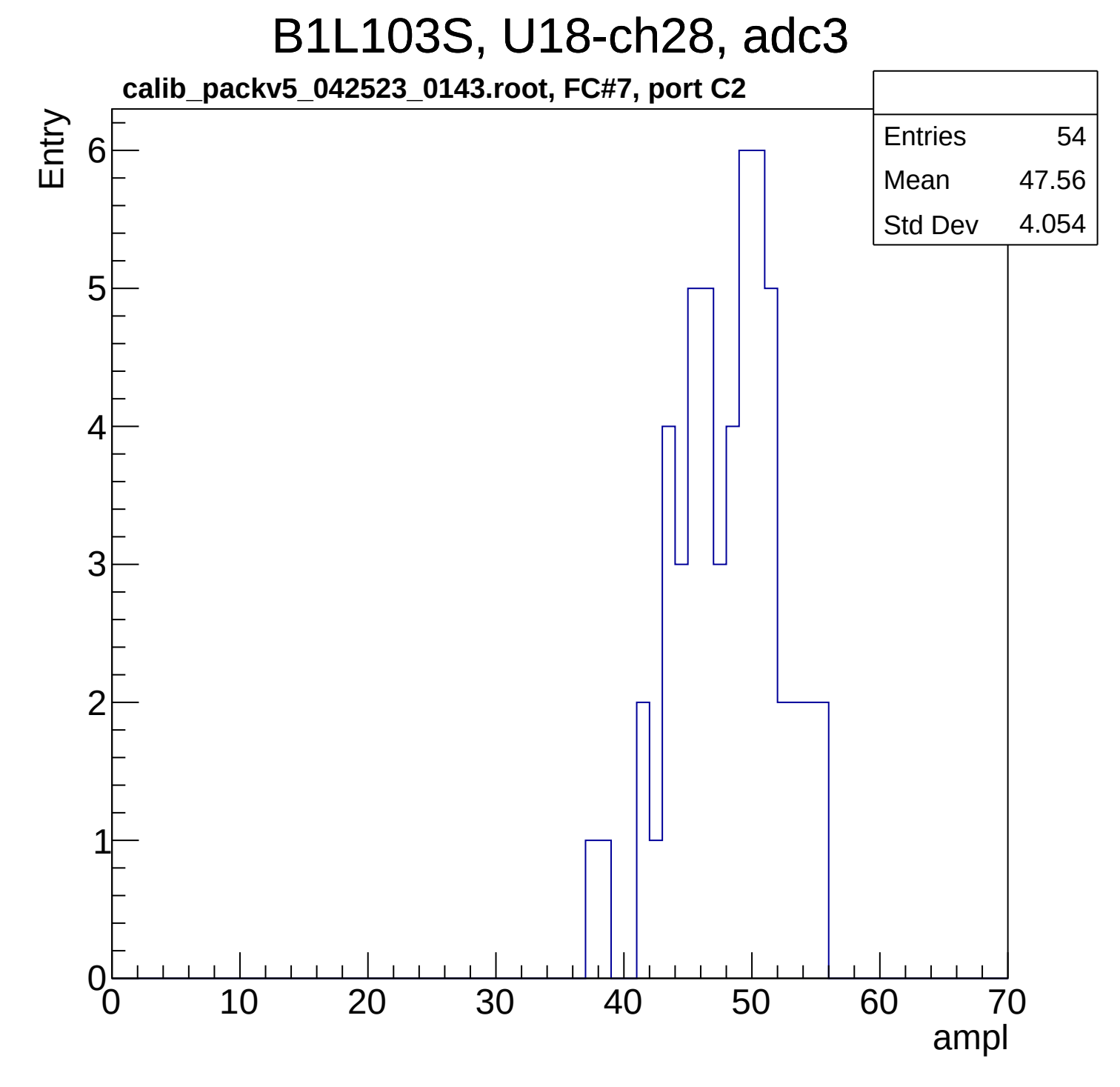
B1L103S, U18-ch28, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 54
Mean 47.56
Std Dev 4.054
Entry
ampl
0
1
2
3
4
5
6
0
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20
30
40
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60
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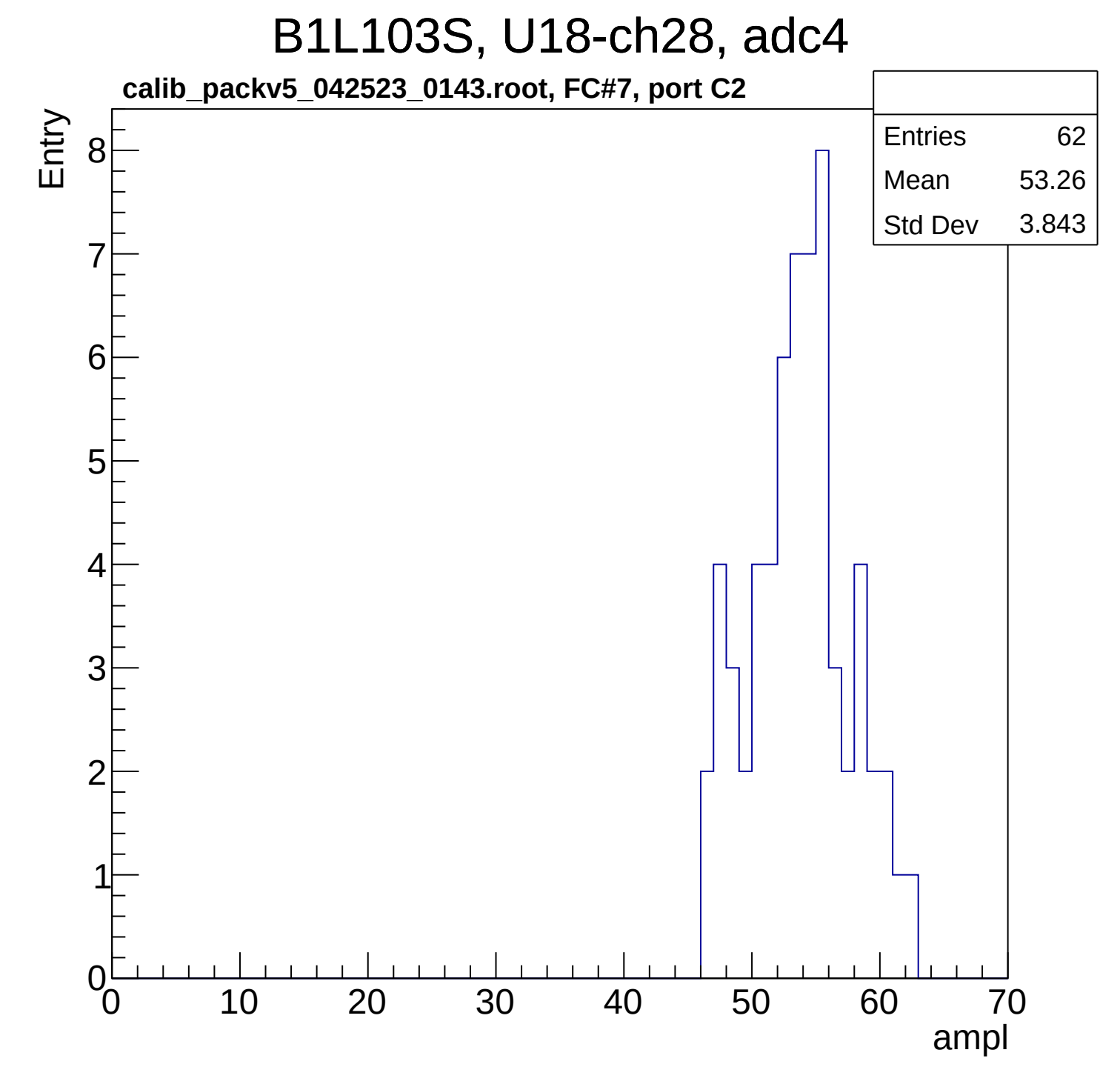
B1L103S, U18-ch28, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 62
Mean 53.26
Std Dev 3.843
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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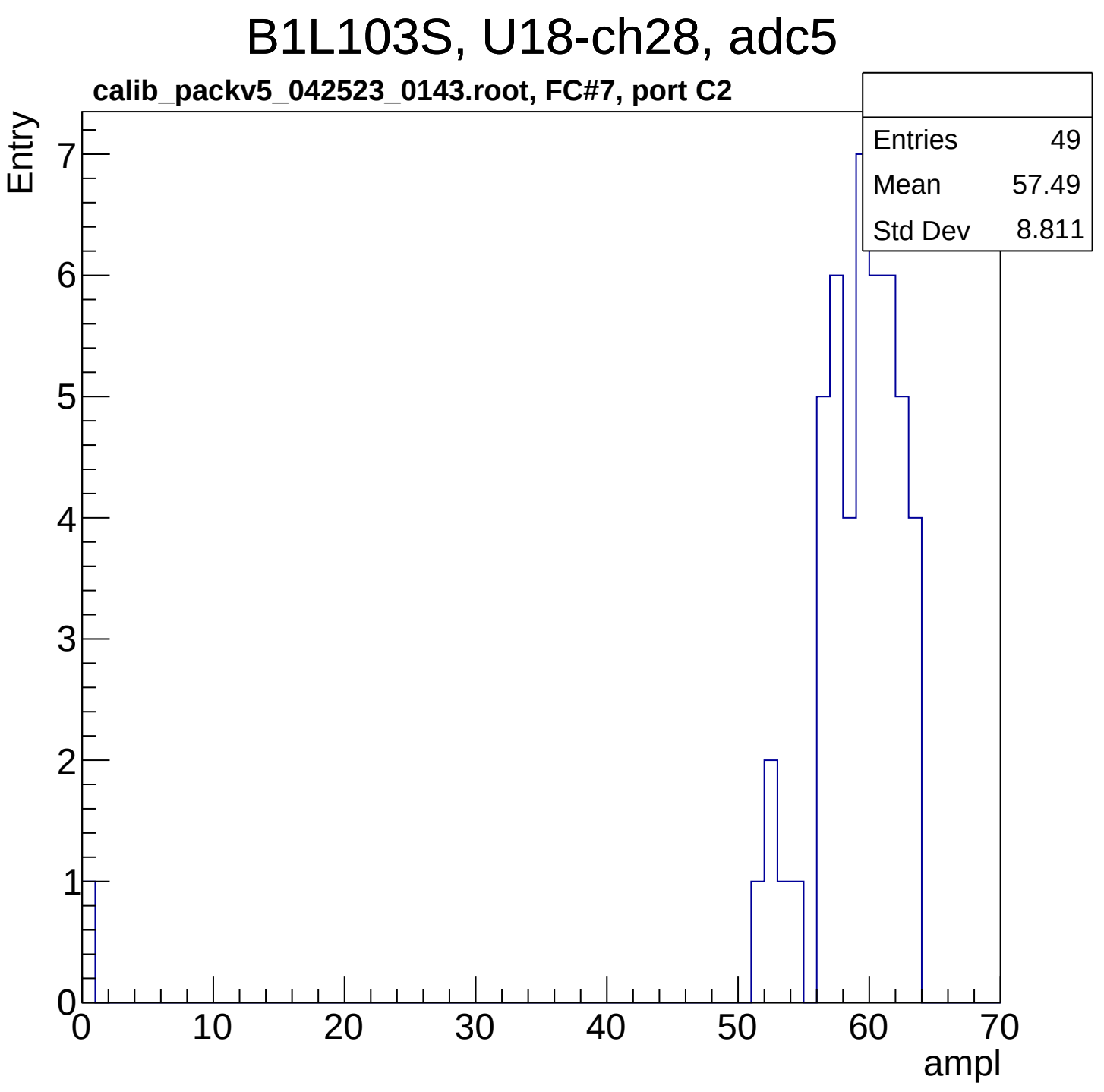
B1L103S, U18-ch28, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 49
Mean 57.49
Std Dev 8.811
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
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60
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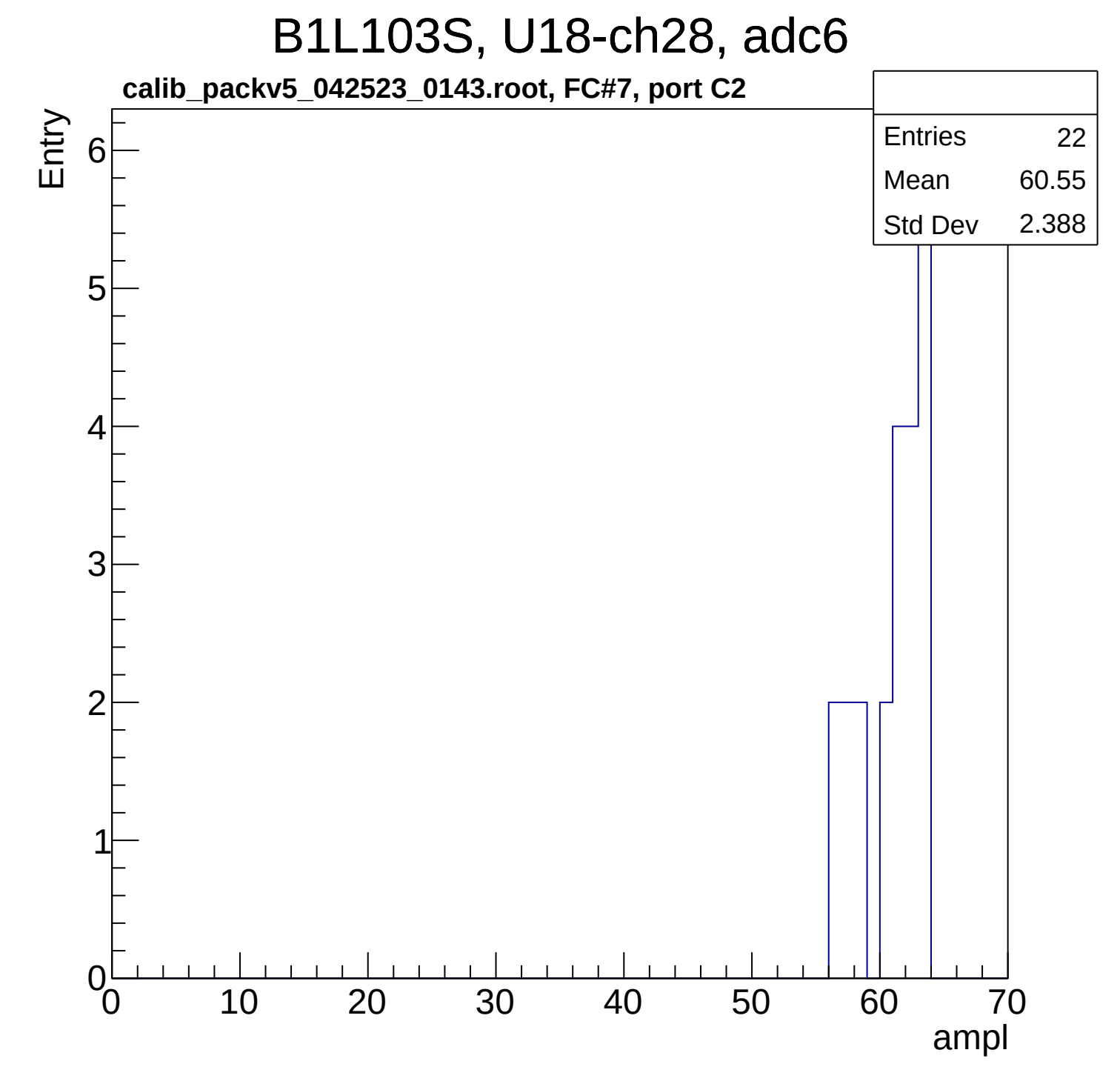
B1L103S, U18-ch28, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 22
Mean 60.55
Std Dev 2.388
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
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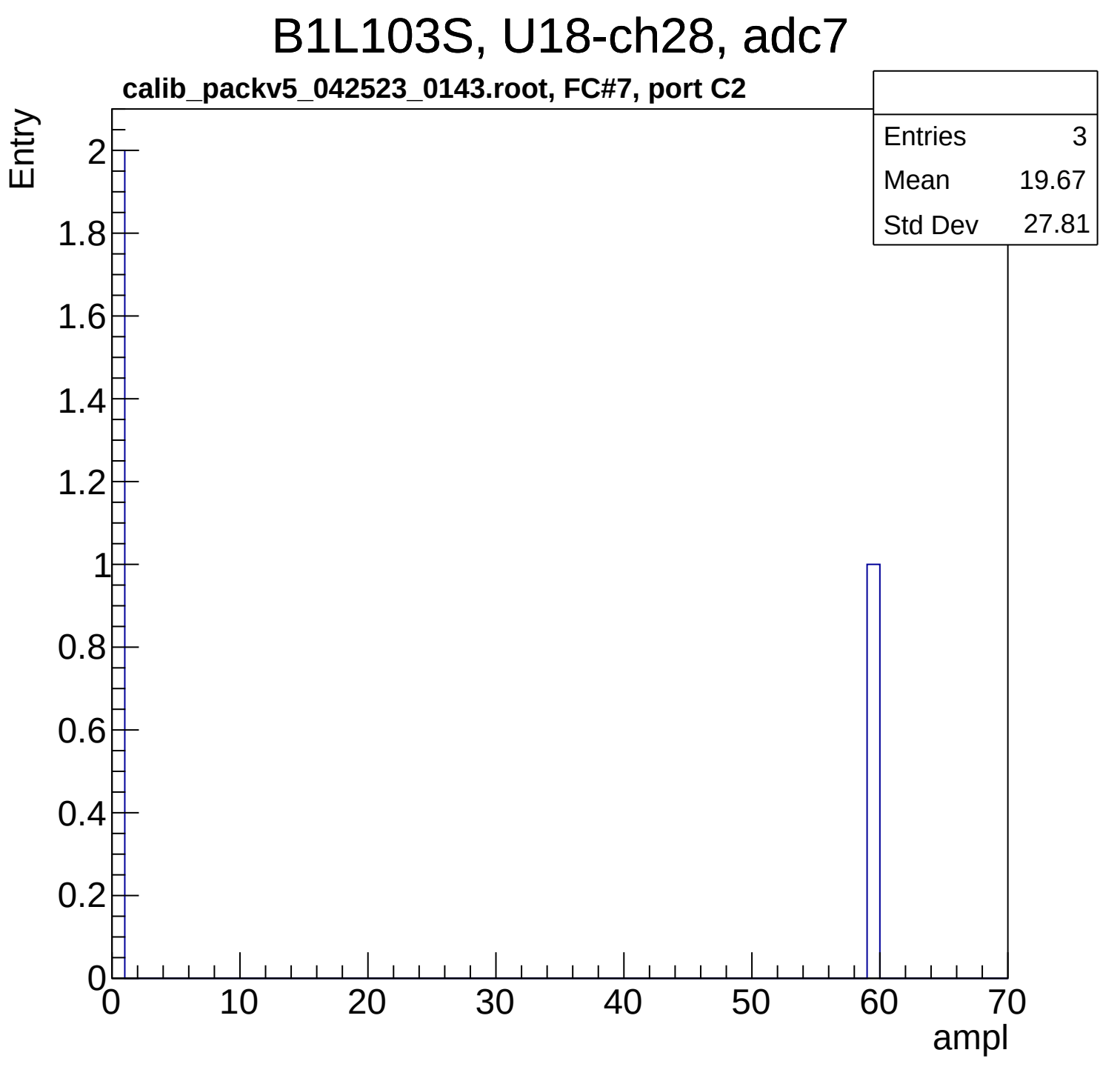
B1L103S, U18-ch28, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 19.67
Std Dev 27.81
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
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60
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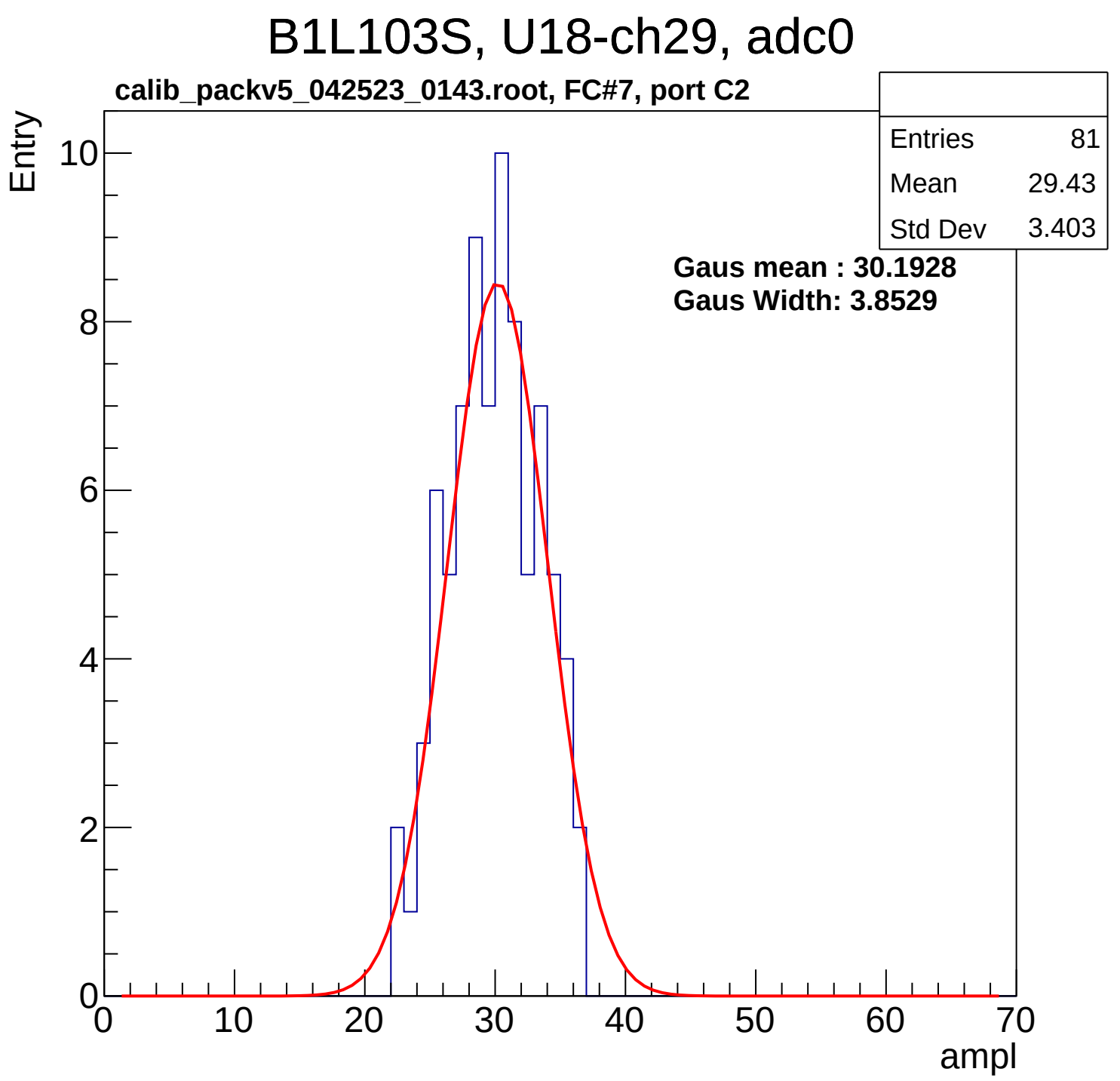
B1L103S, U18-ch29, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 81
Mean 29.43
Std Dev 3.403
Gaus mean : 30.1928
Gaus Width: 3.8529
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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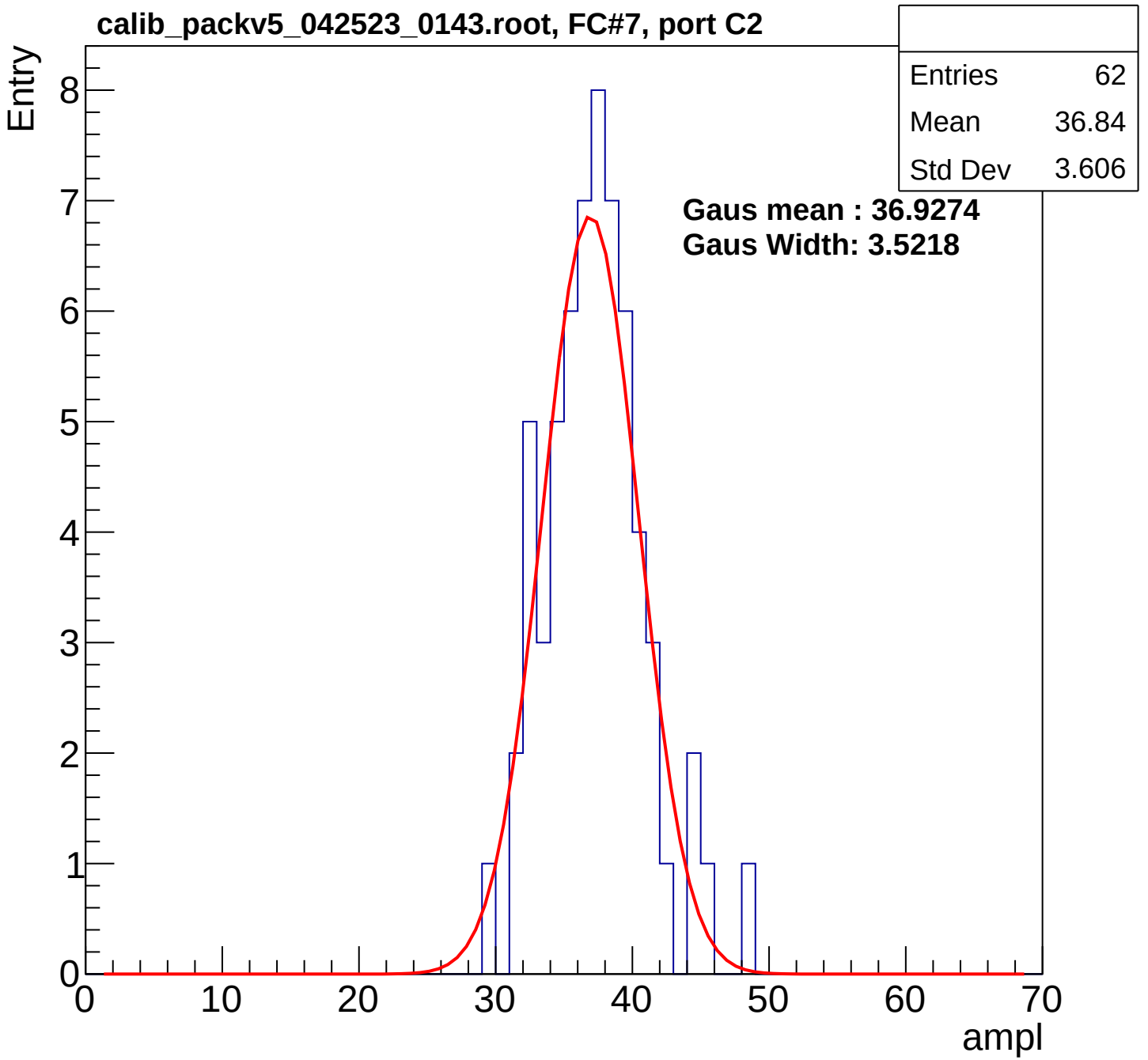
B1L103S, U18-ch29, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 62
Mean 36.84
Std Dev 3.606
Gaus mean : 36.9274
Gaus Width: 3.5218
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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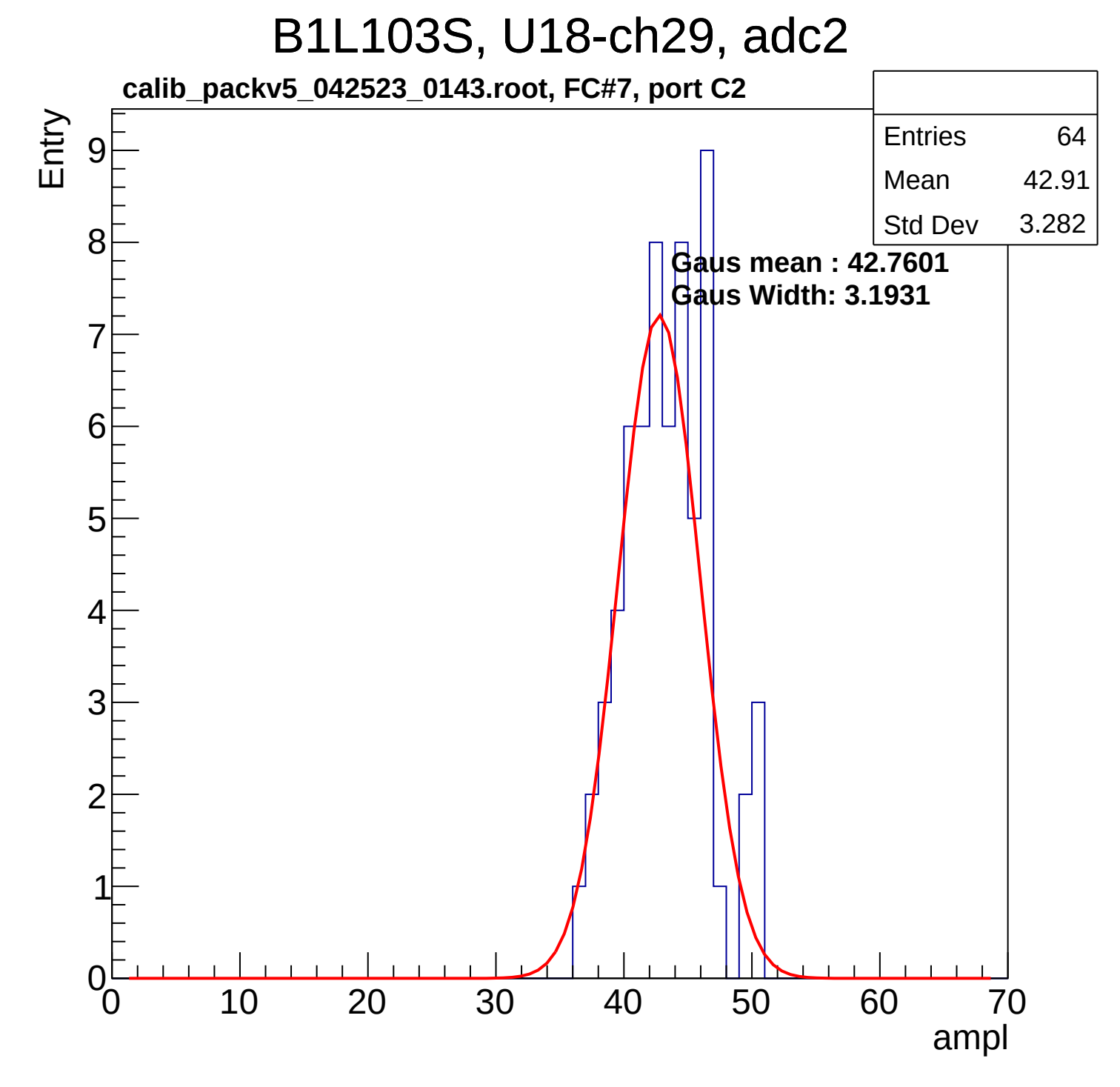
B1L103S, U18-ch29, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 42.91
Std Dev 3.282
Gaus mean : 42.7601
Gaus Width: 3.1931
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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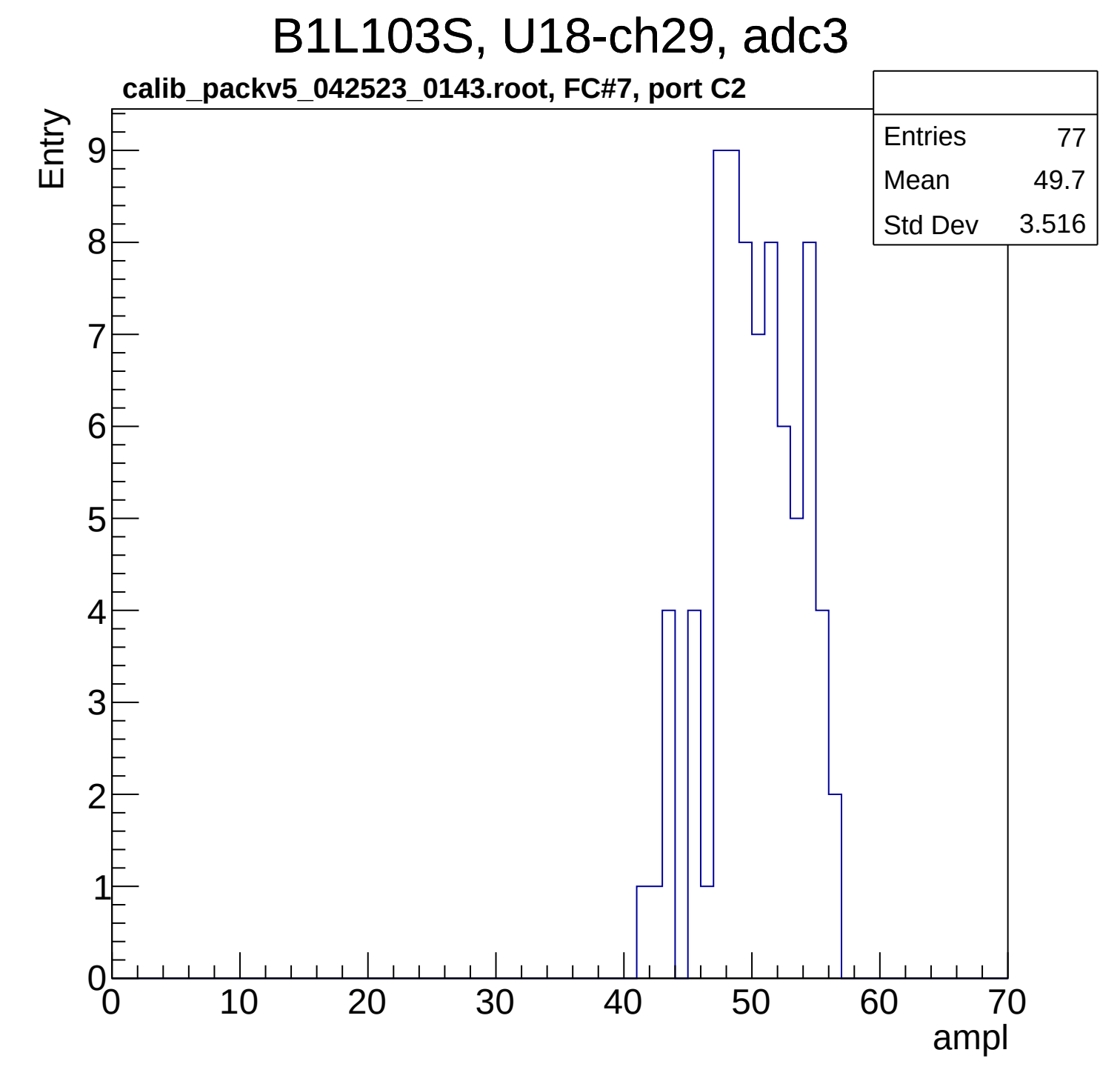
B1L103S, U18-ch29, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 77
Mean 49.7
Std Dev 3.516
Entry
ampl
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2
3
4
5
6
7
8
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0
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20
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60
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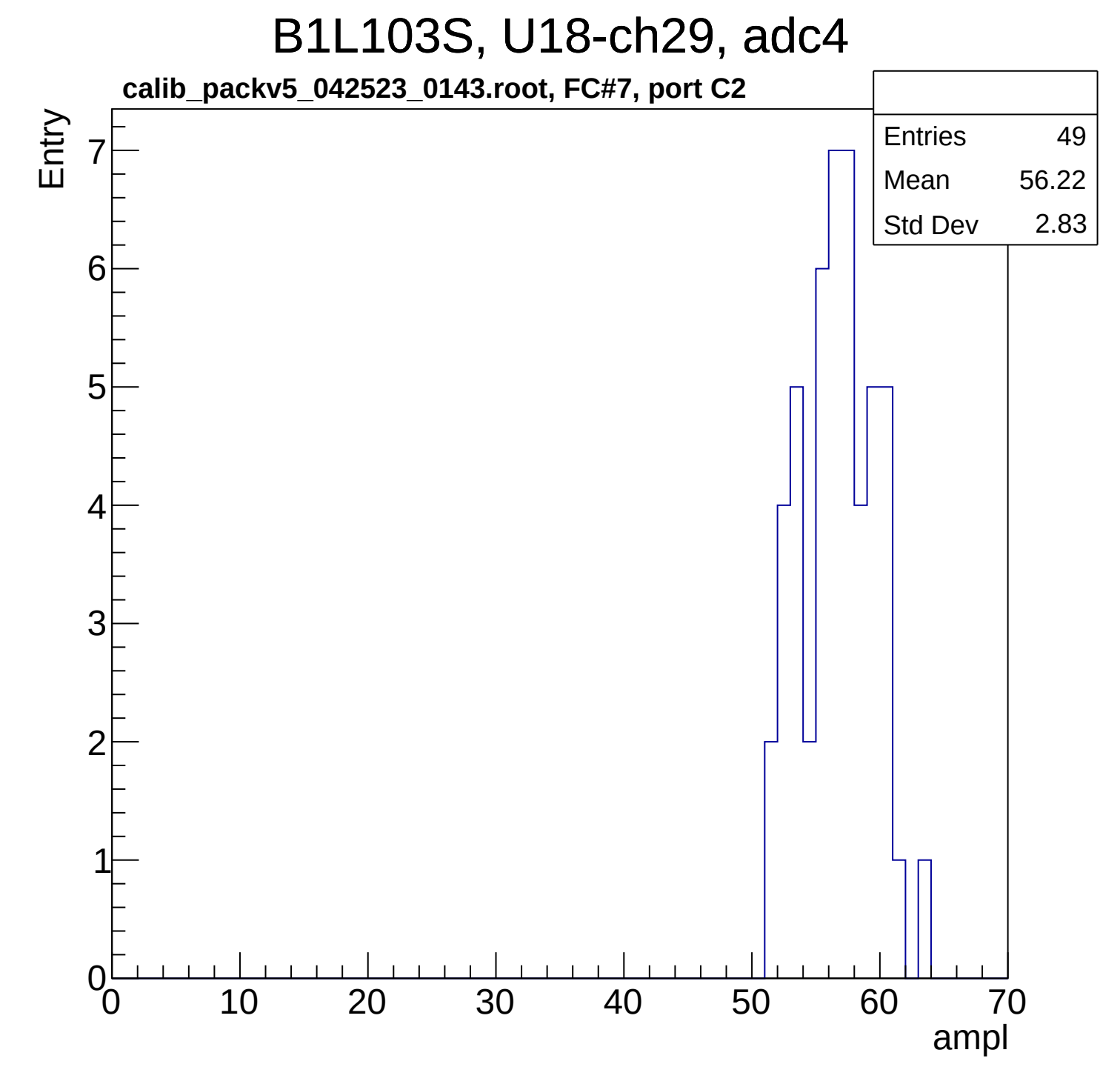
B1L103S, U18-ch29, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 49
Mean 56.22
Std Dev 2.83
Entry
ampl
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4
5
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0
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20
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40
50
60
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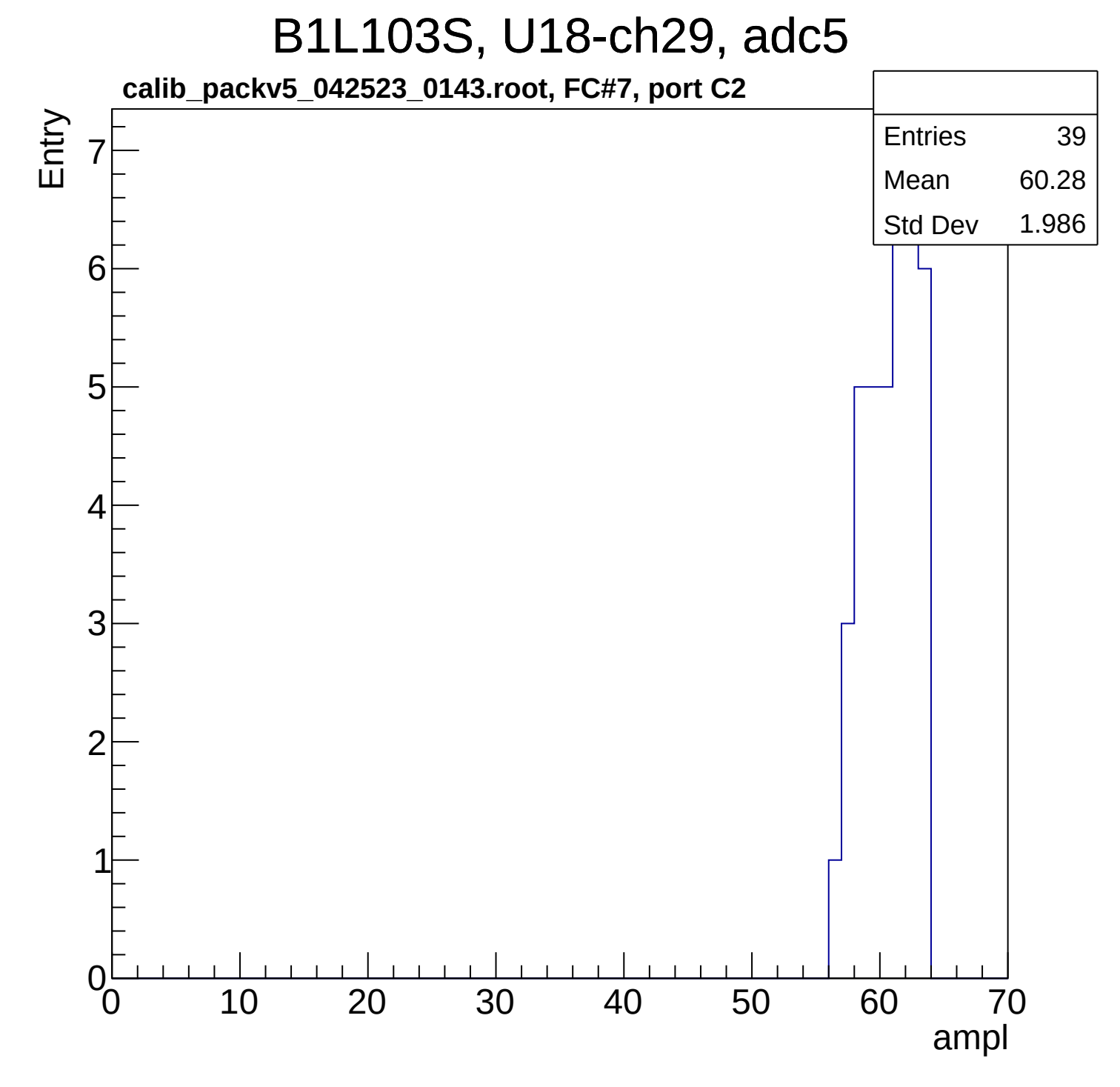
B1L103S, U18-ch29, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 39
Mean 60.28
Std Dev 1.986
Entry
ampl
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1
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3
4
5
6
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0
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20
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40
50
60
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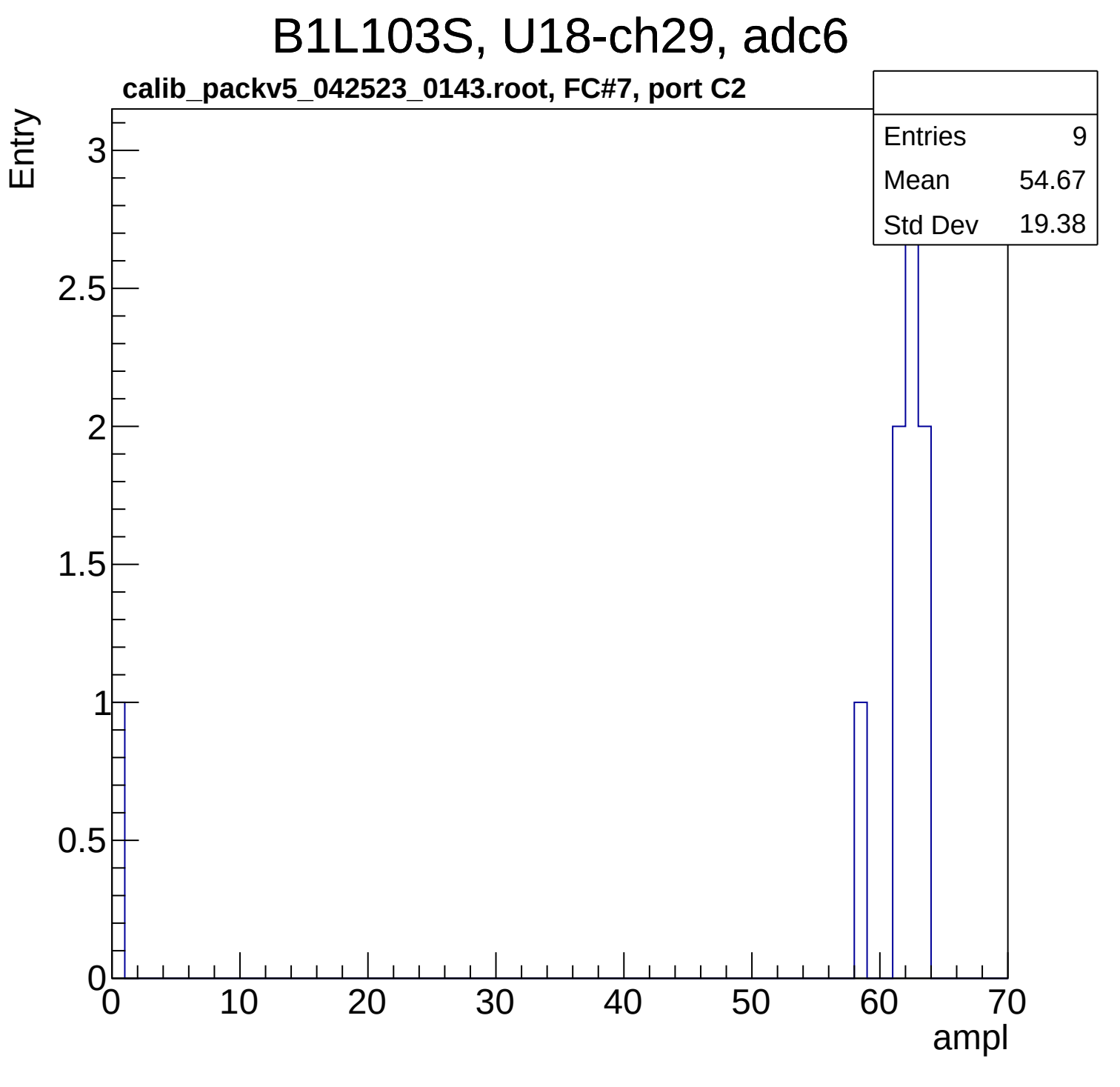
B1L103S, U18-ch29, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 9
Mean 54.67
Std Dev 19.38
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
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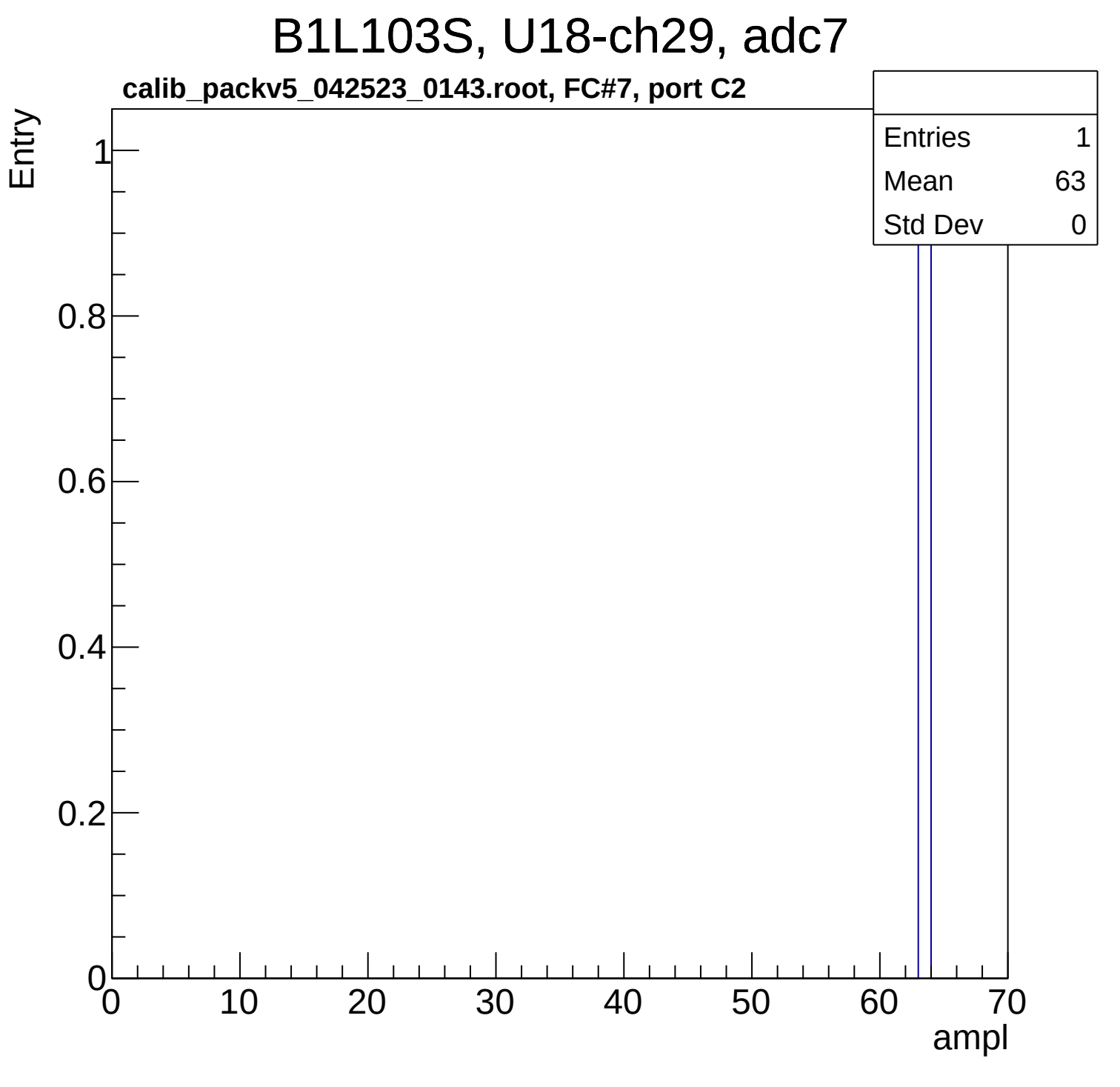
B1L103S, U18-ch29, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 63
Std Dev 0
Entry
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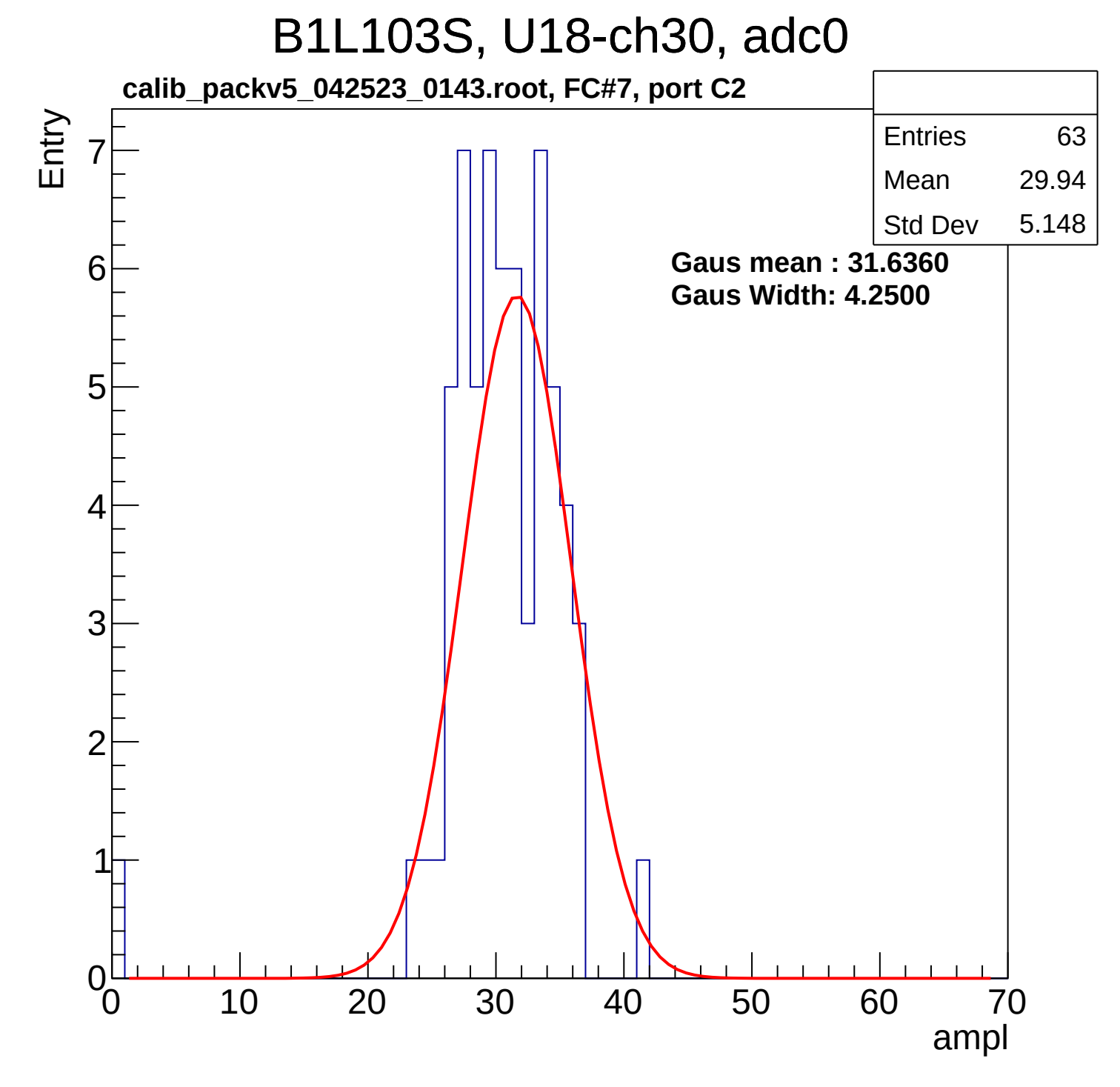
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch30, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 29.94
Std Dev 5.148
Gaus mean : 31.6360
Gaus Width: 4.2500
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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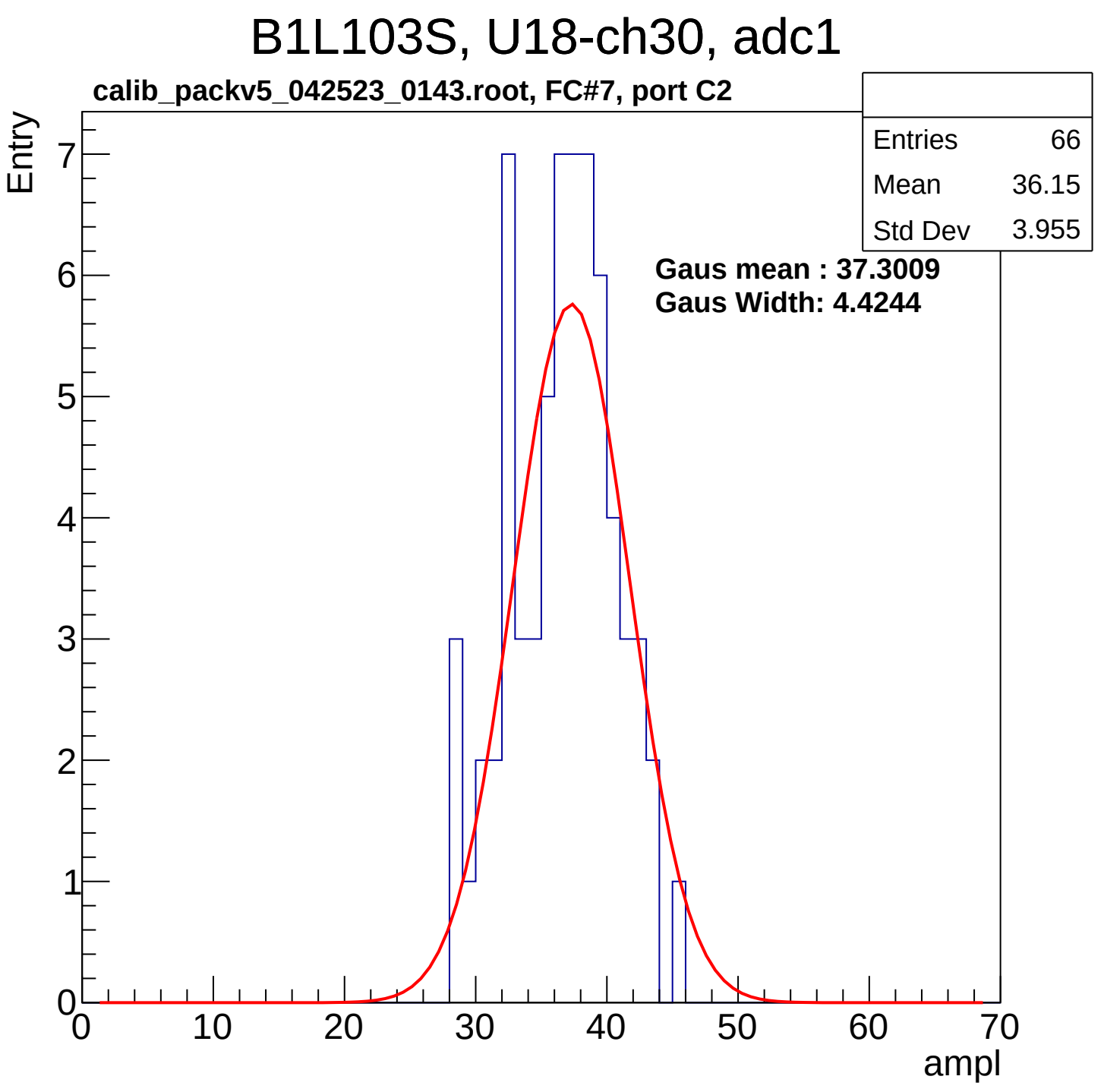
B1L103S, U18-ch30, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 36.15
Std Dev 3.955
Gaus mean : 37.3009
Gaus Width: 4.4244
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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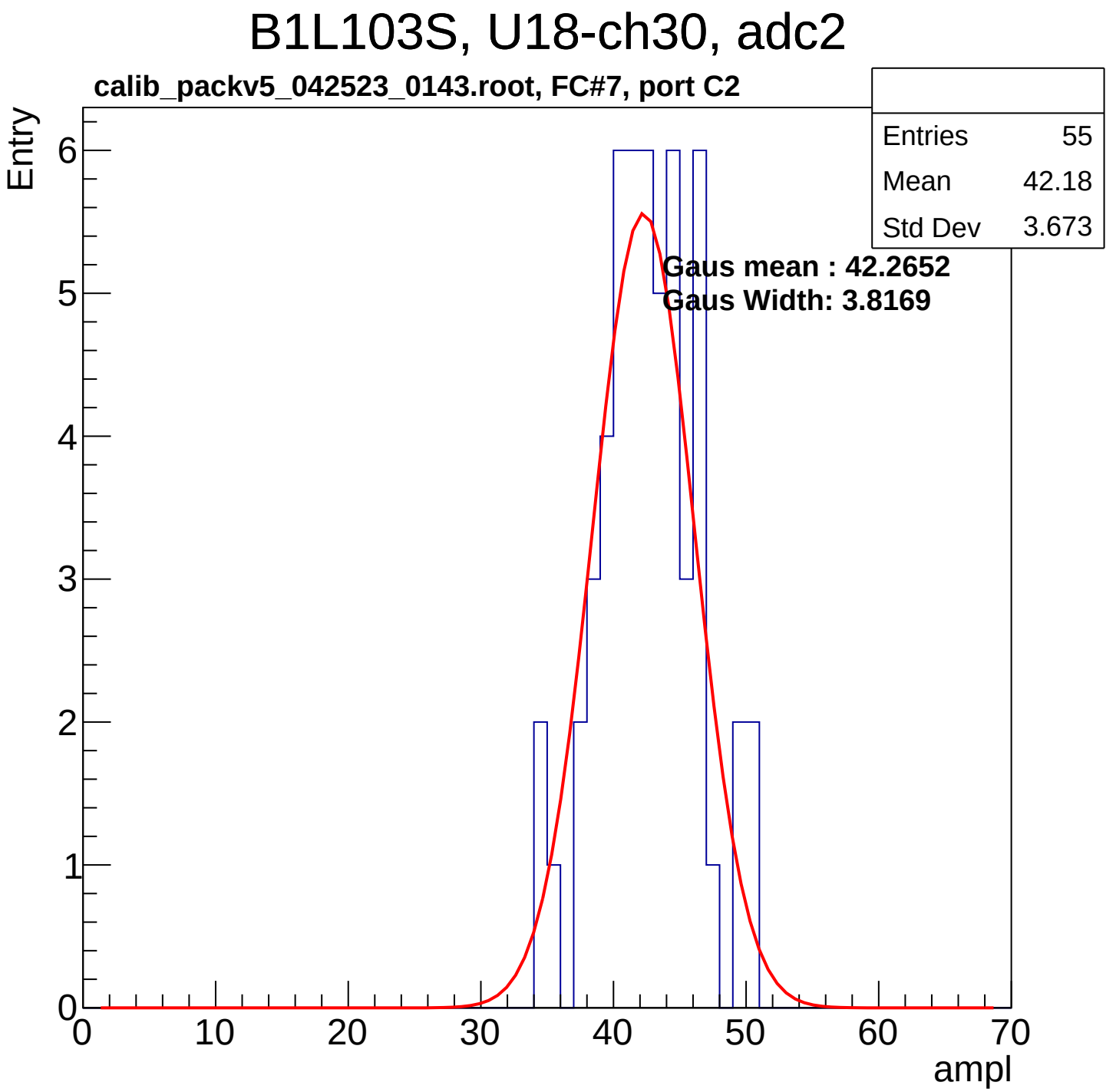
B1L103S, U18-ch30, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 42.18
Std Dev 3.673
Gaus mean : 42.2652
Gaus Width: 3.8169
Entry
ampl
0
1
2
3
4
5
6
0
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40
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60
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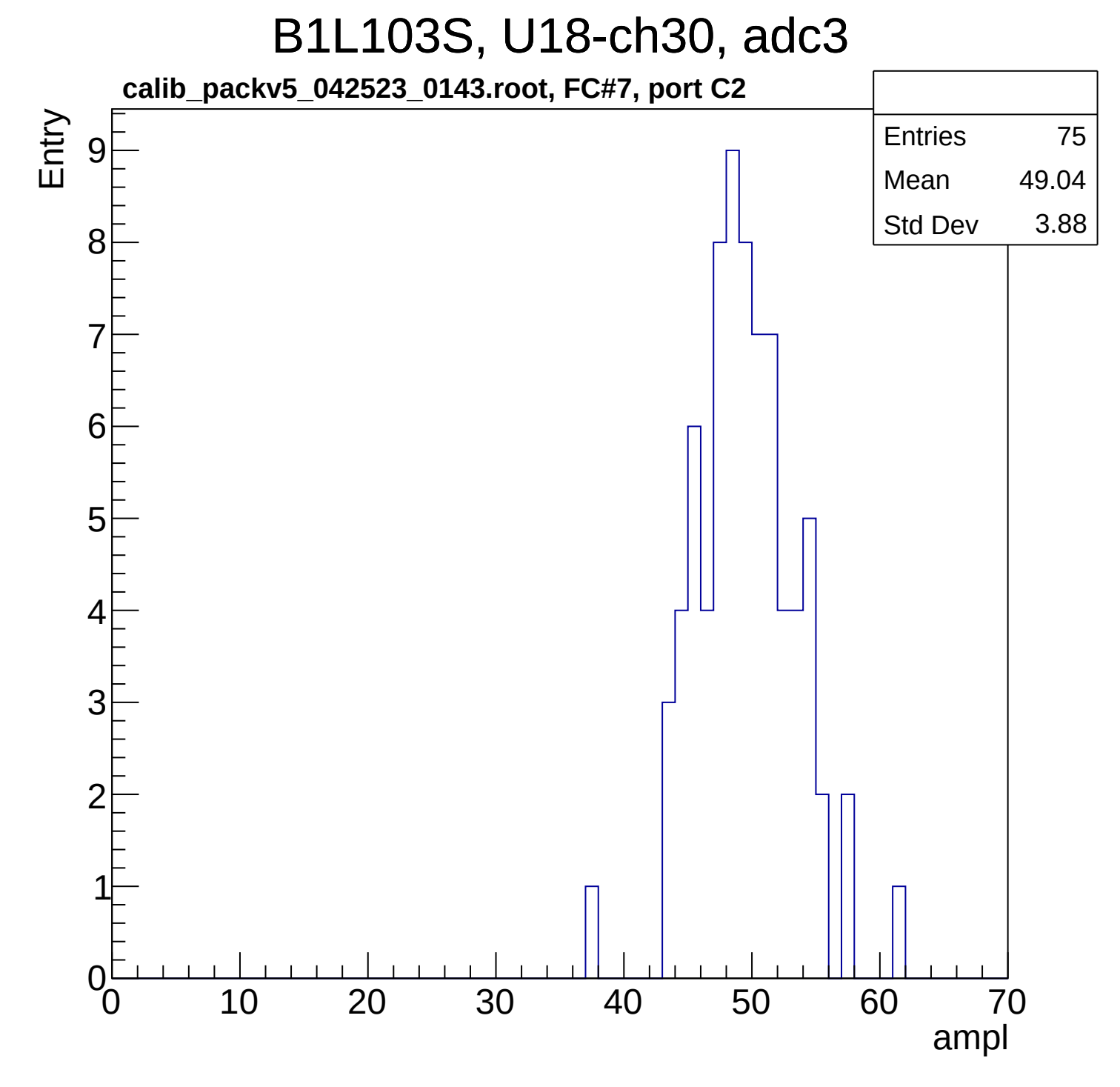
B1L103S, U18-ch30, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 75
Mean 49.04
Std Dev 3.88
Entry
ampl
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2
3
4
5
6
7
8
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0
10
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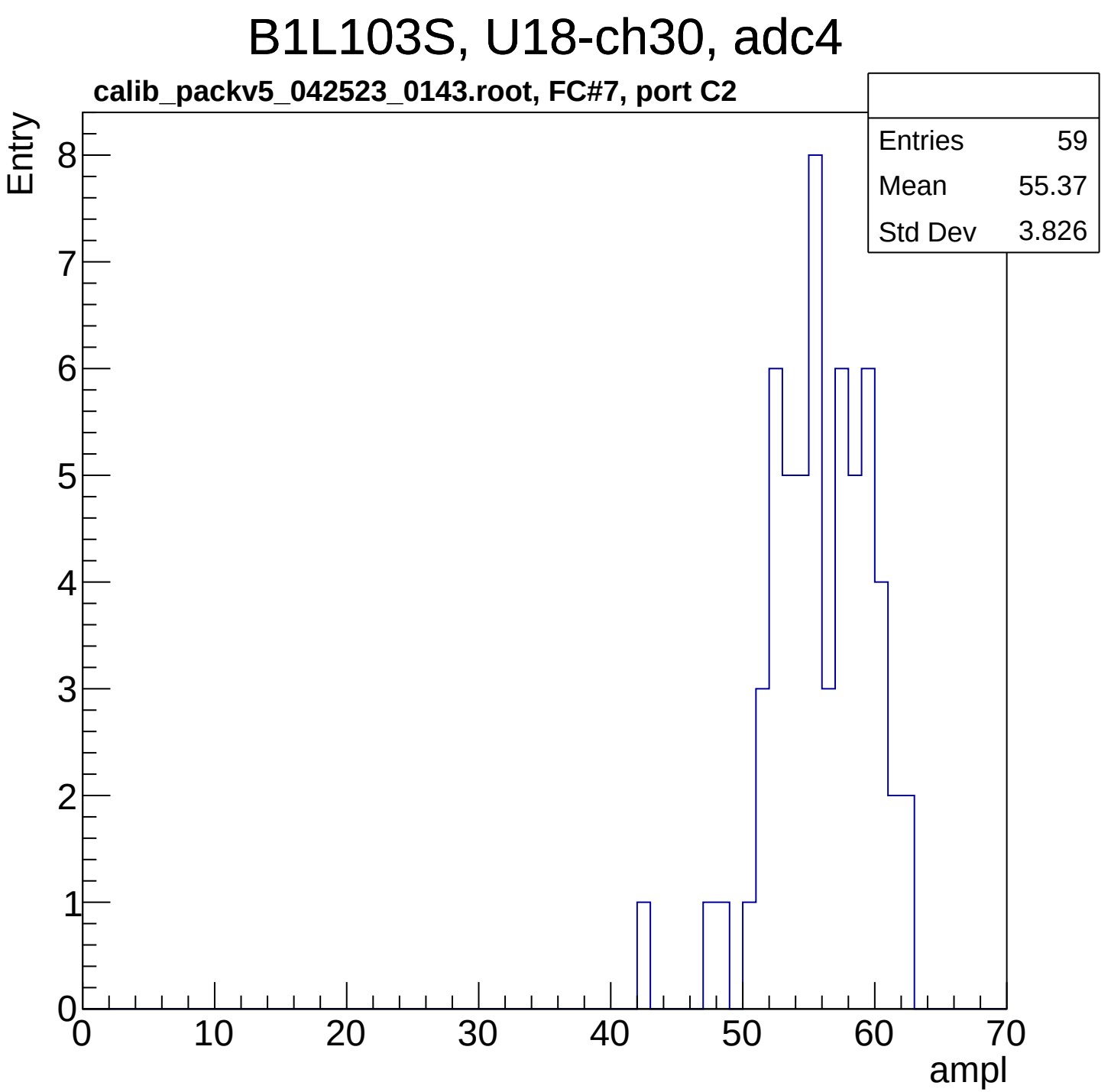
B1L103S, U18-ch30, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 55.37
Std Dev 3.826
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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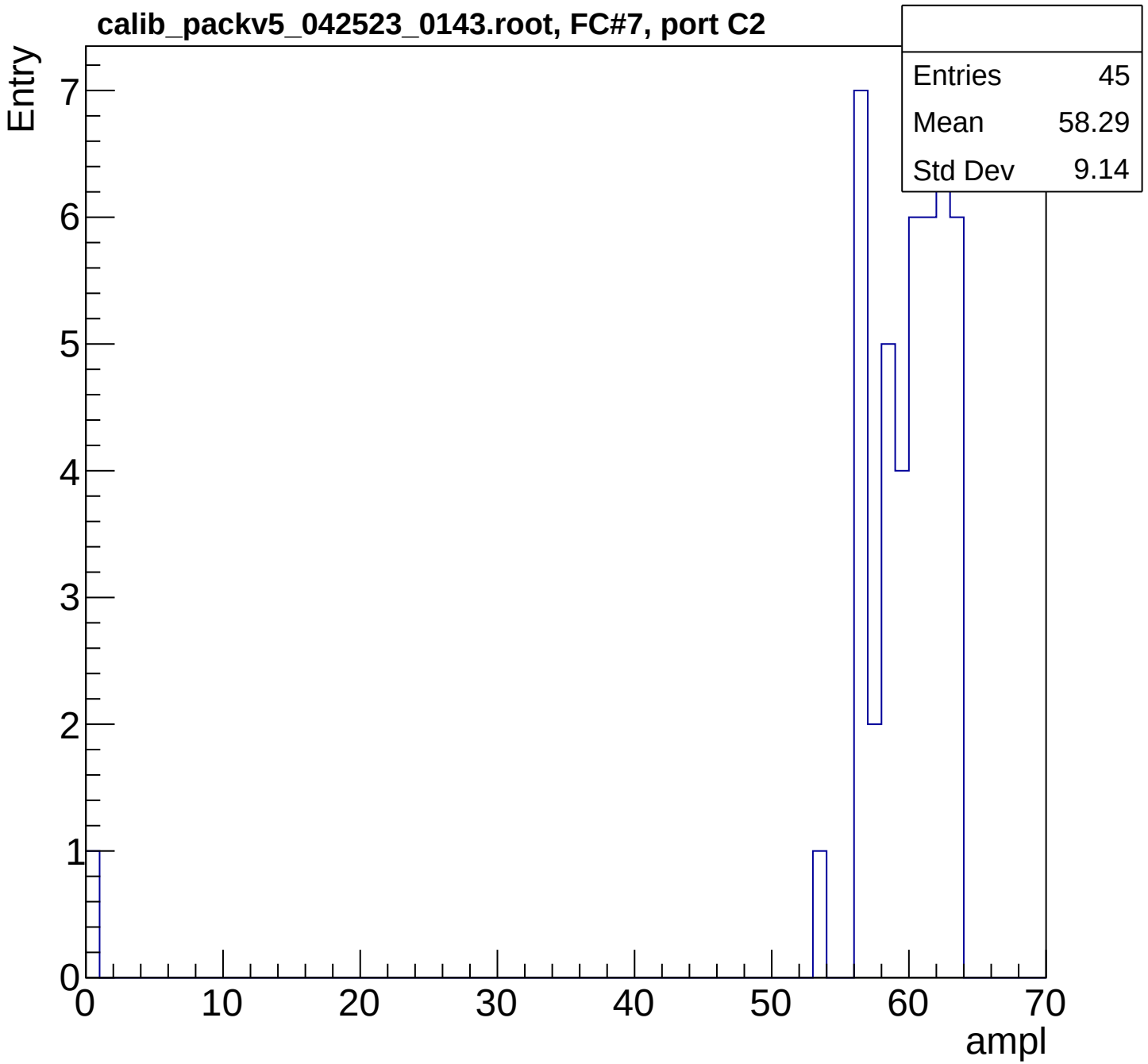
B1L103S, U18-ch30, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 45
Mean 58.29
Std Dev 9.14
Entry
ampl
0
1
2
3
4
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6
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0
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60
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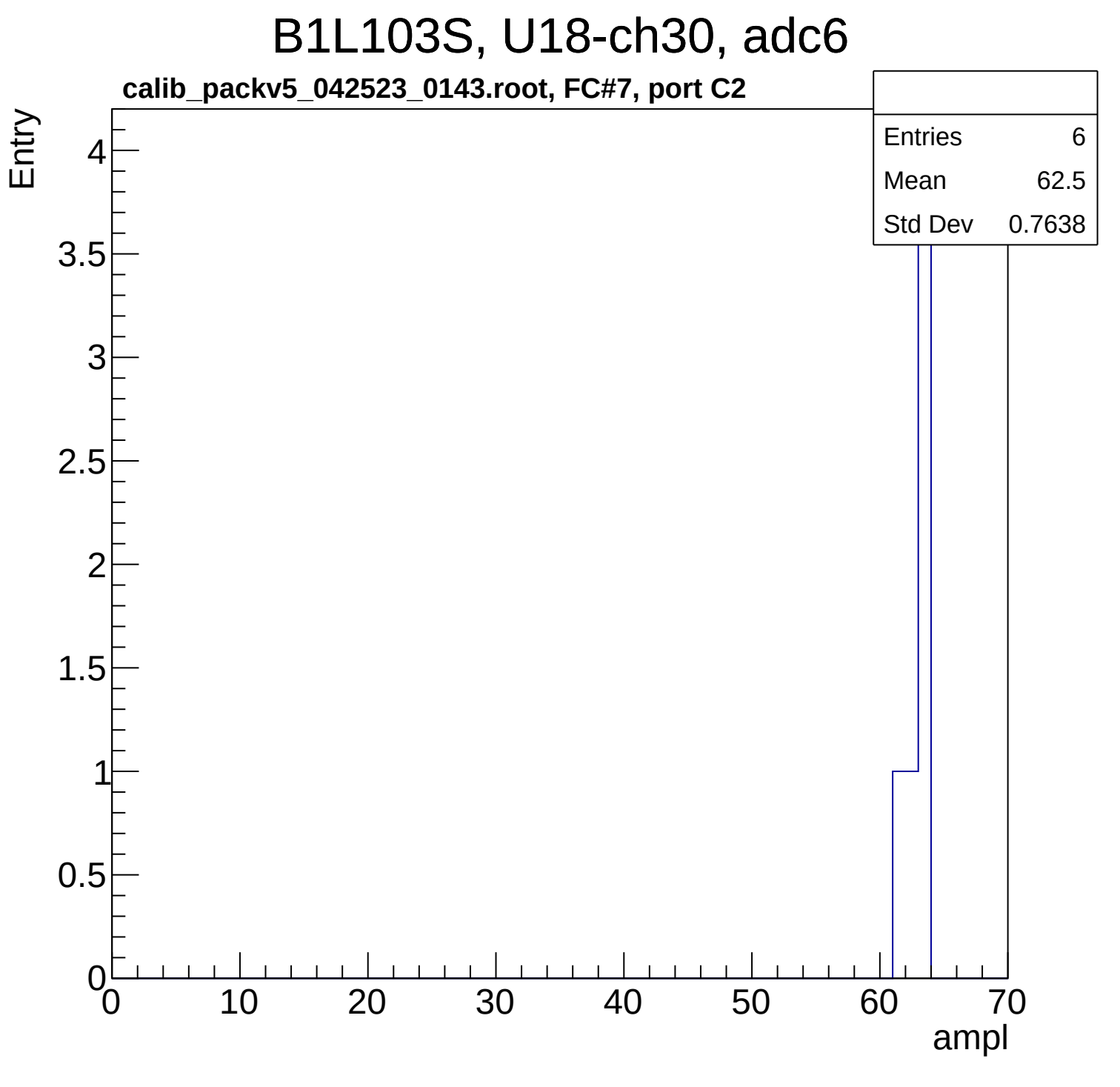
B1L103S, U18-ch30, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 6
Mean 62.5
Std Dev 0.7638
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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40
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60
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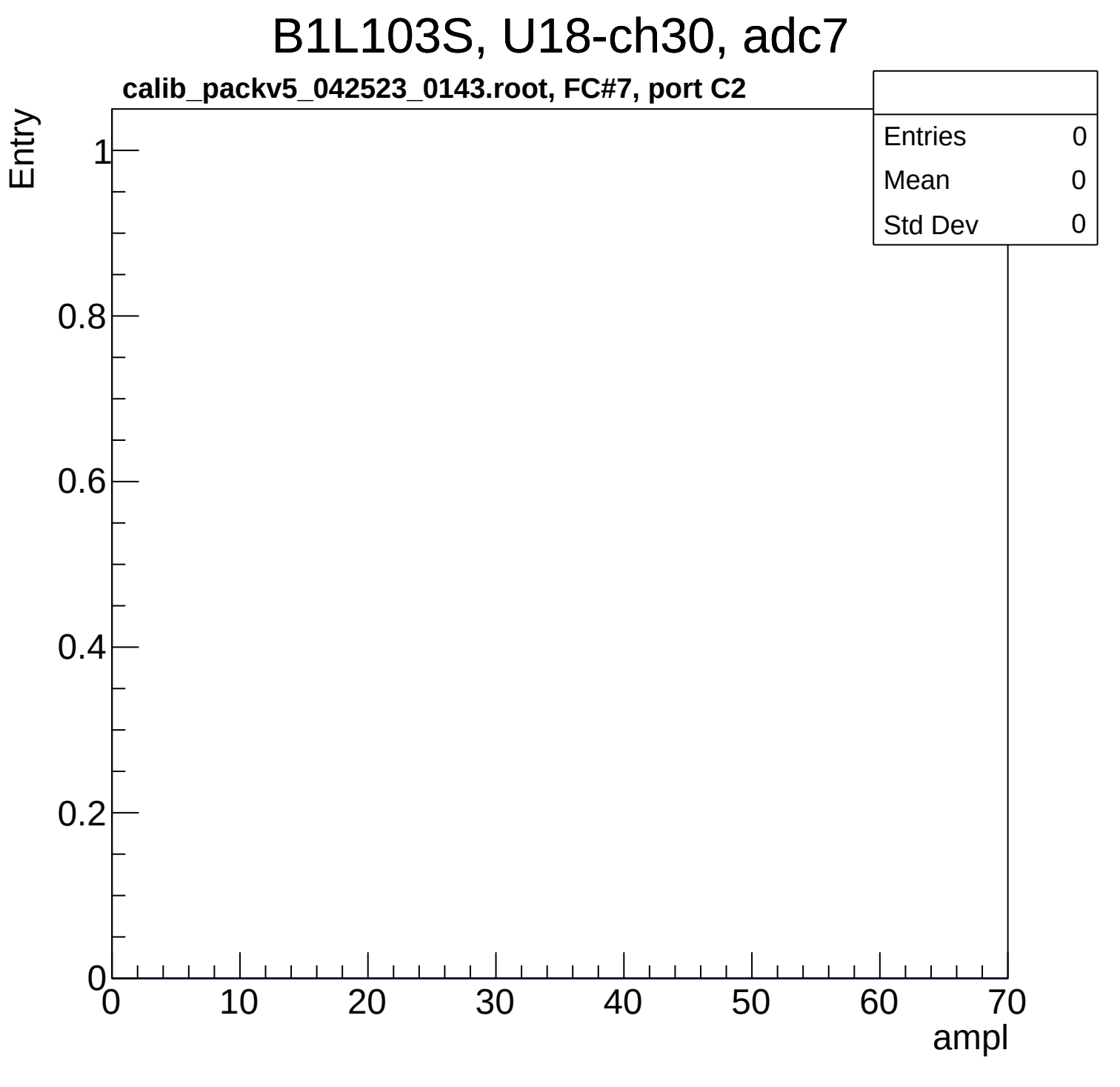
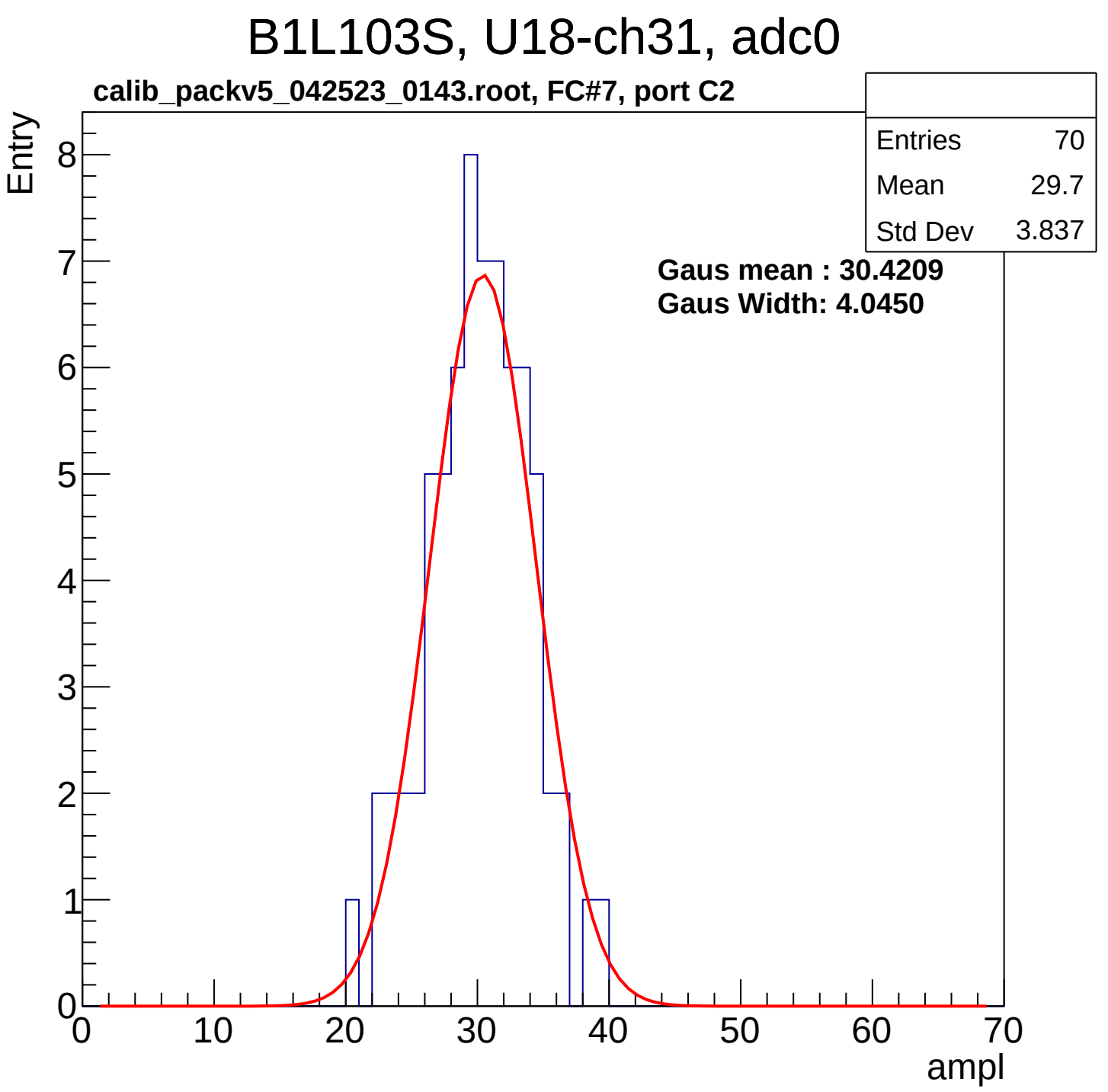

B1L103S, U18-ch30, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch31, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 29.7
Std Dev 3.837
Gaus mean : 30.4209
Gaus Width: 4.0450
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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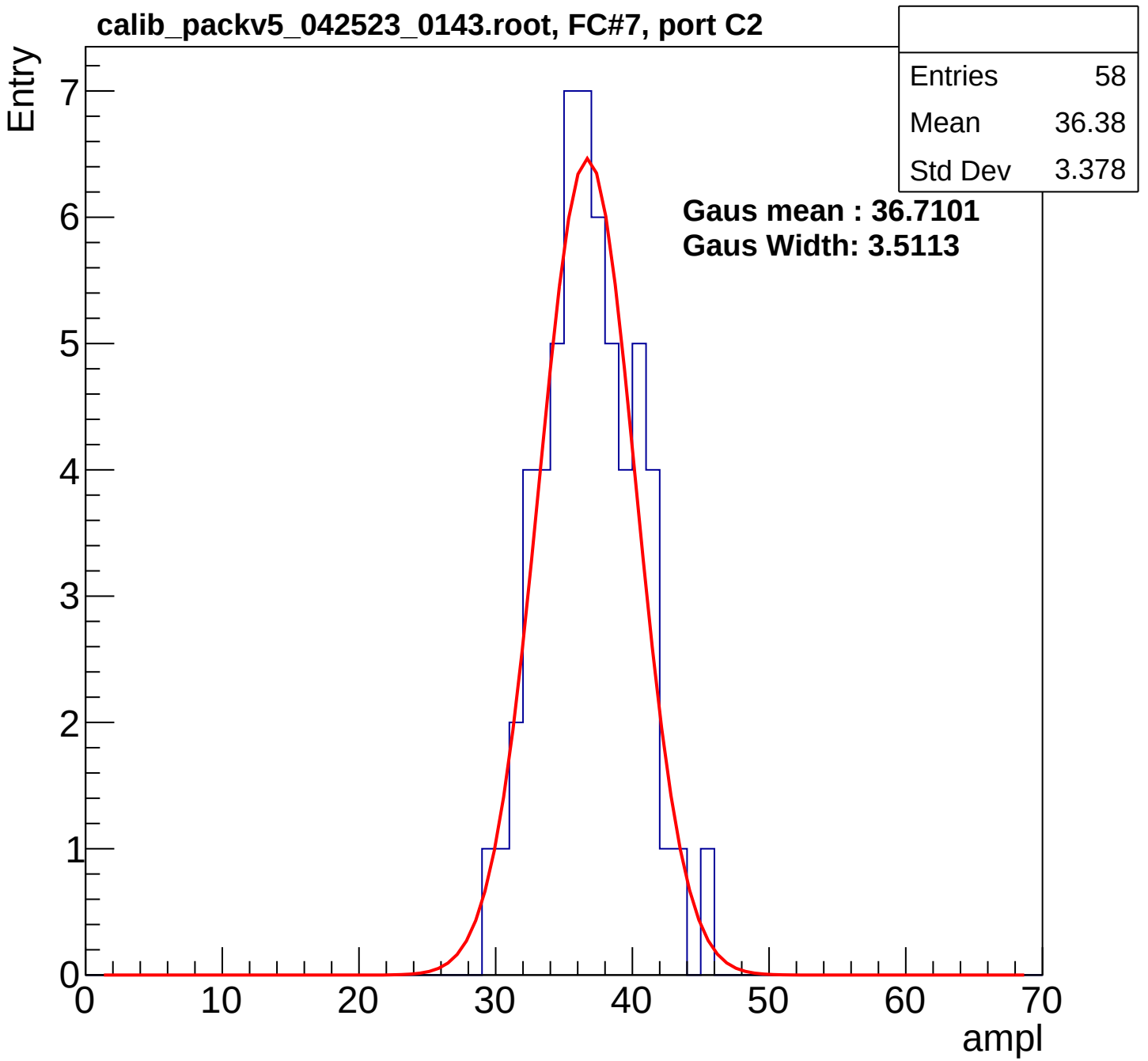
B1L103S, U18-ch31, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 58
Mean 36.38
Std Dev 3.378
Gaus mean : 36.7101
Gaus Width: 3.5113
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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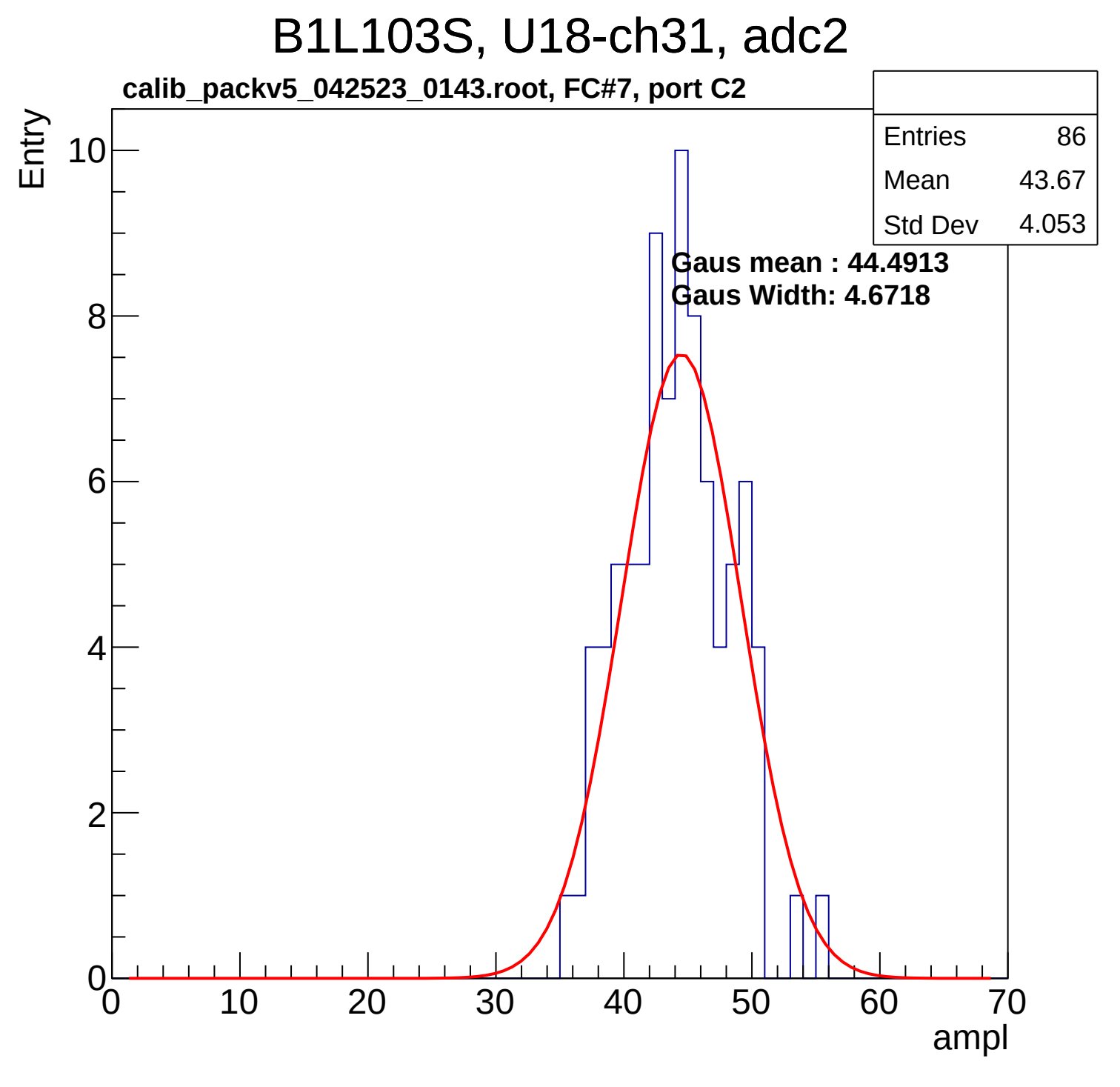
B1L103S, U18-ch31, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 86
Mean 43.67
Std Dev 4.053
Gaus mean : 44.4913
Gaus Width: 4.6718
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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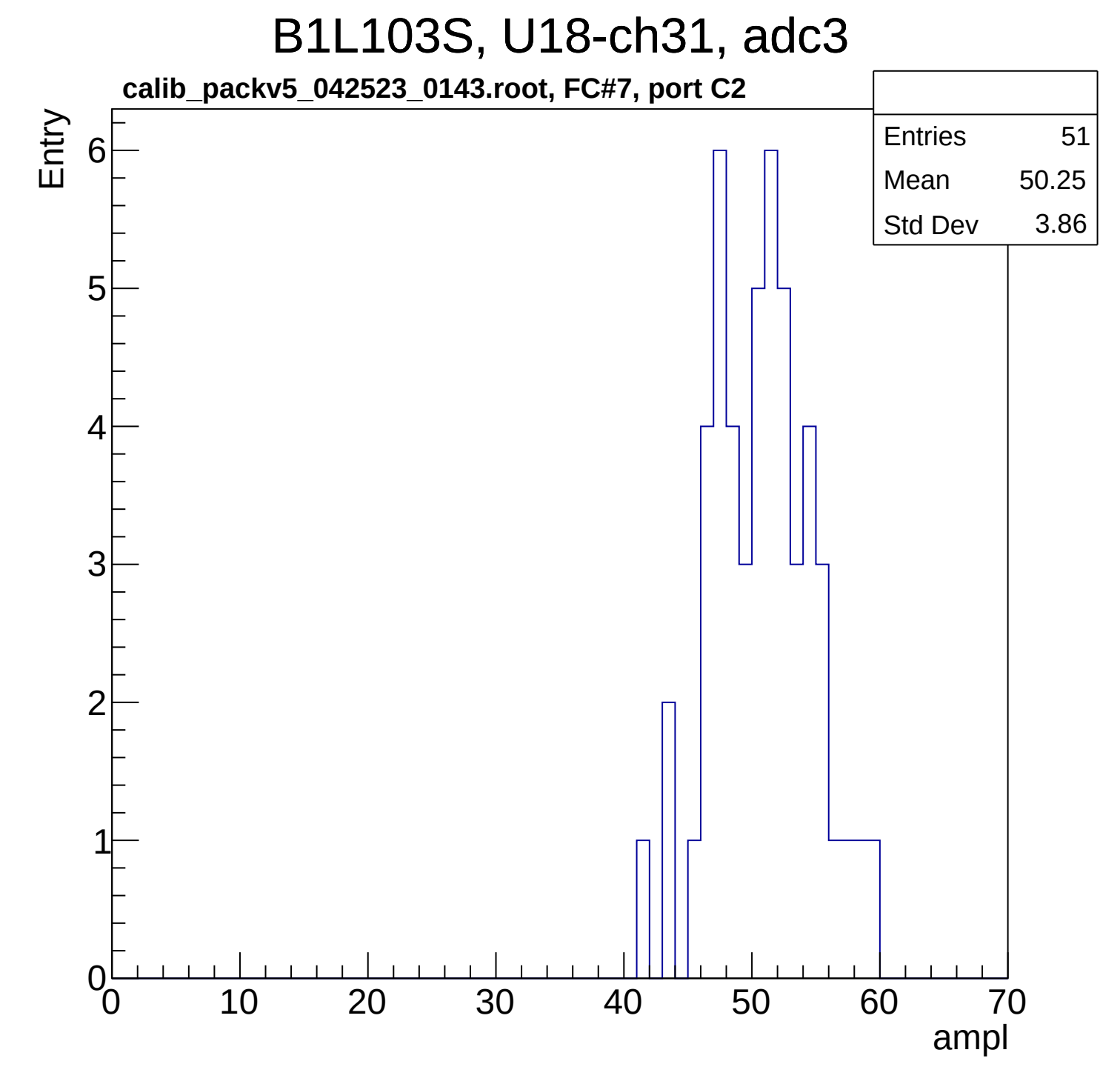
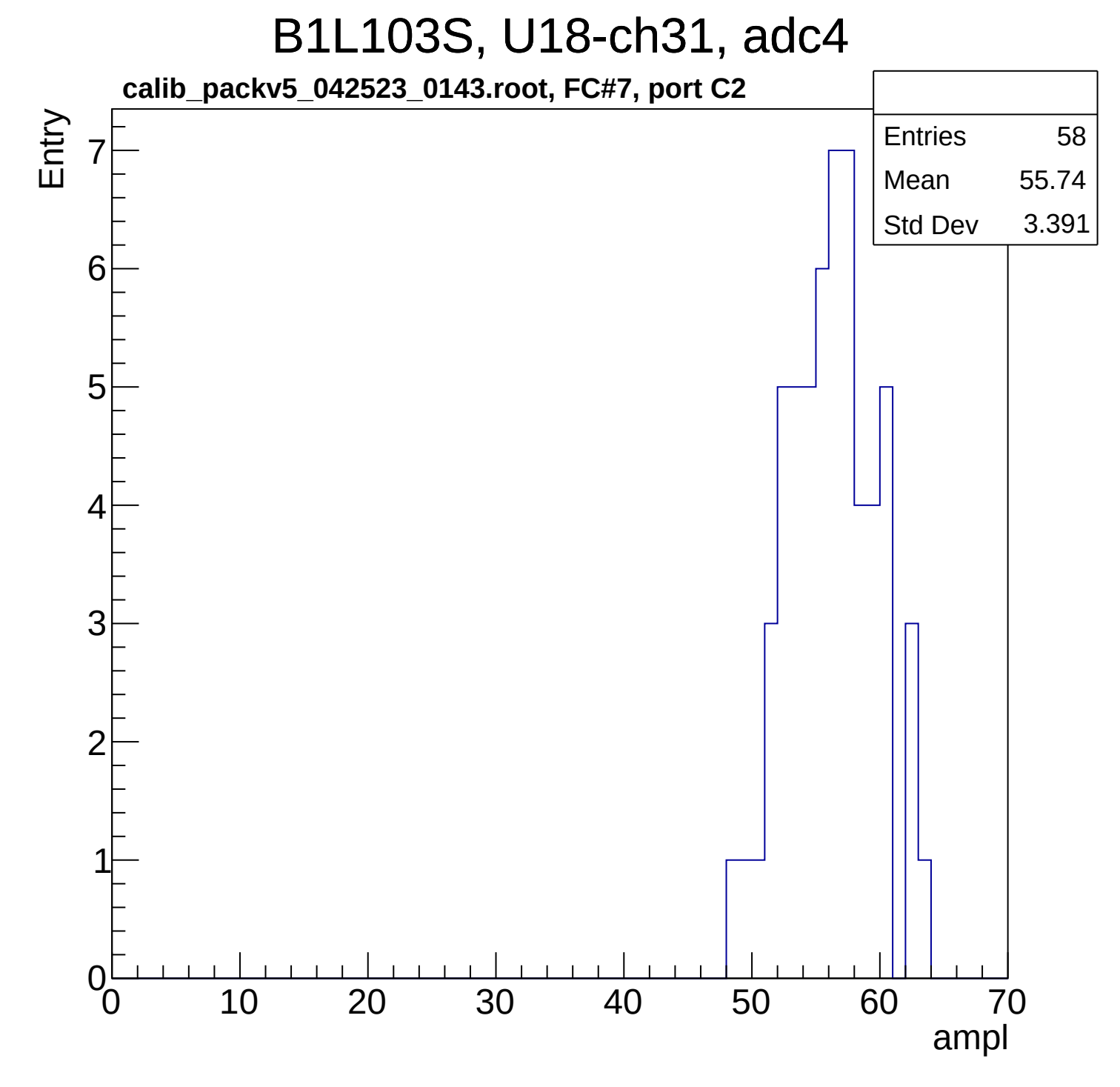

B1L103S, U18-ch31, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 51
Mean 50.25
Std Dev 3.86
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U18-ch31, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 58
Mean 55.74
Std Dev 3.391
Entry
ampl
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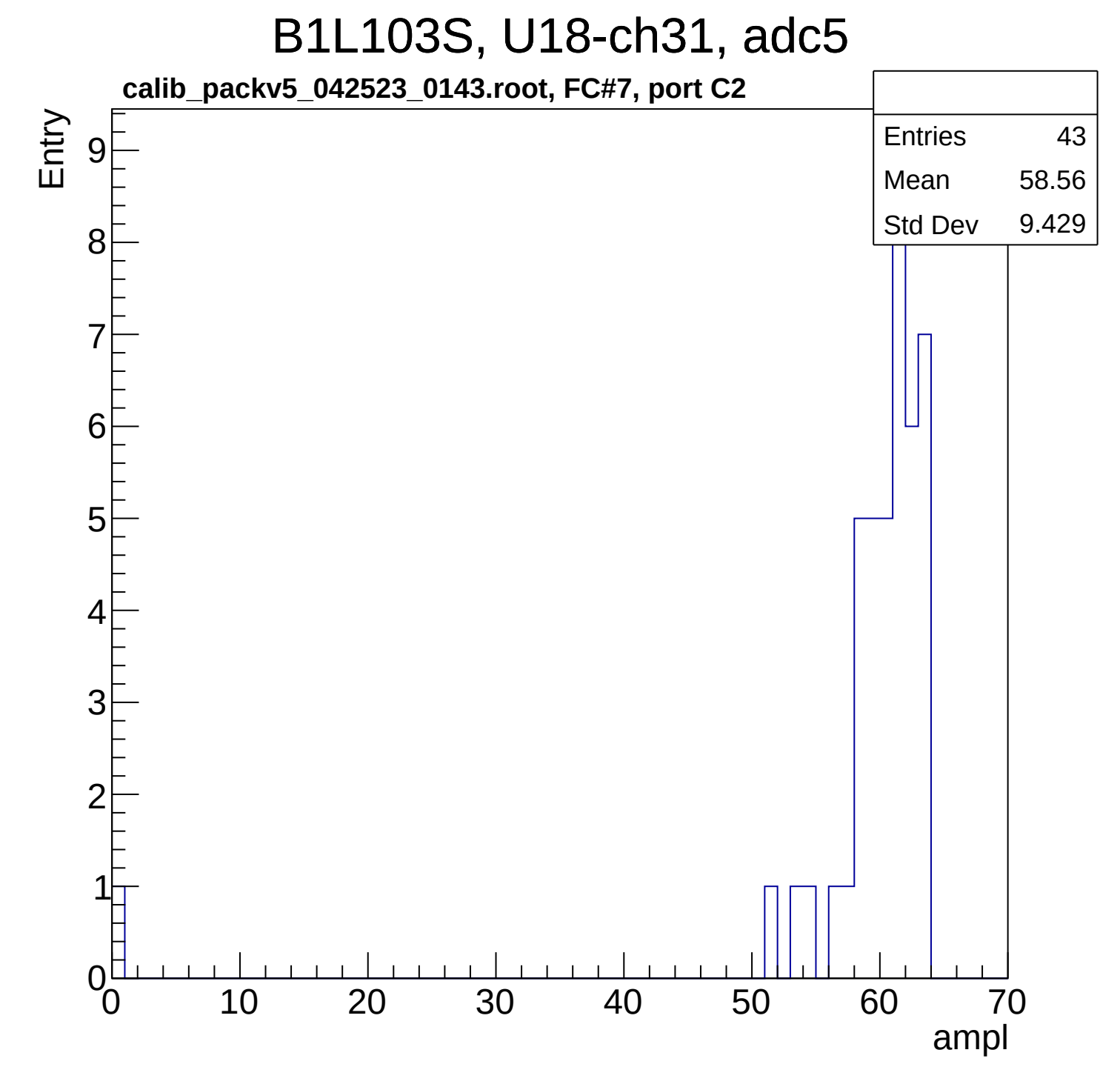
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch31, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 43
Mean 58.56
Std Dev 9.429
Entry
ampl
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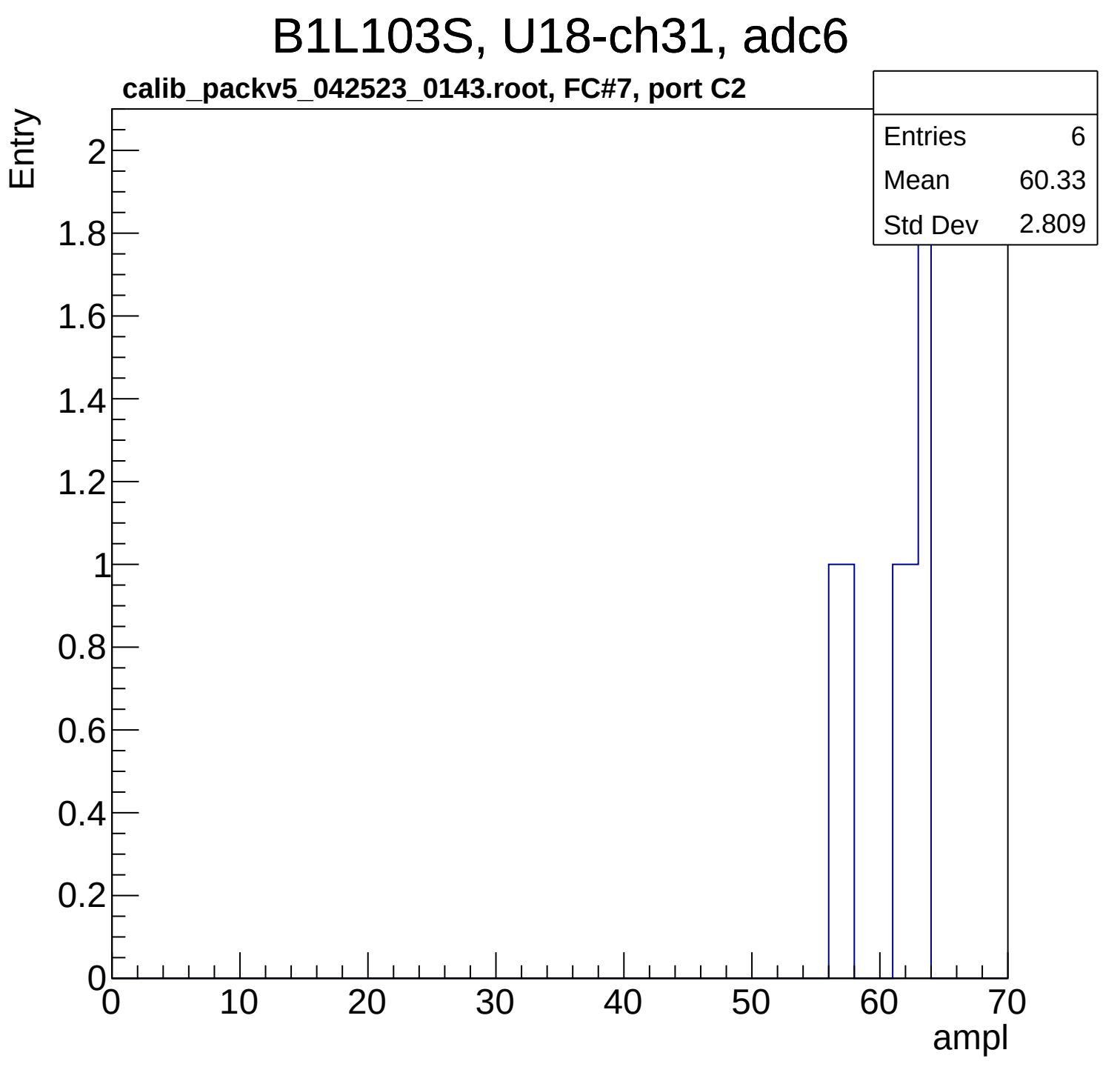
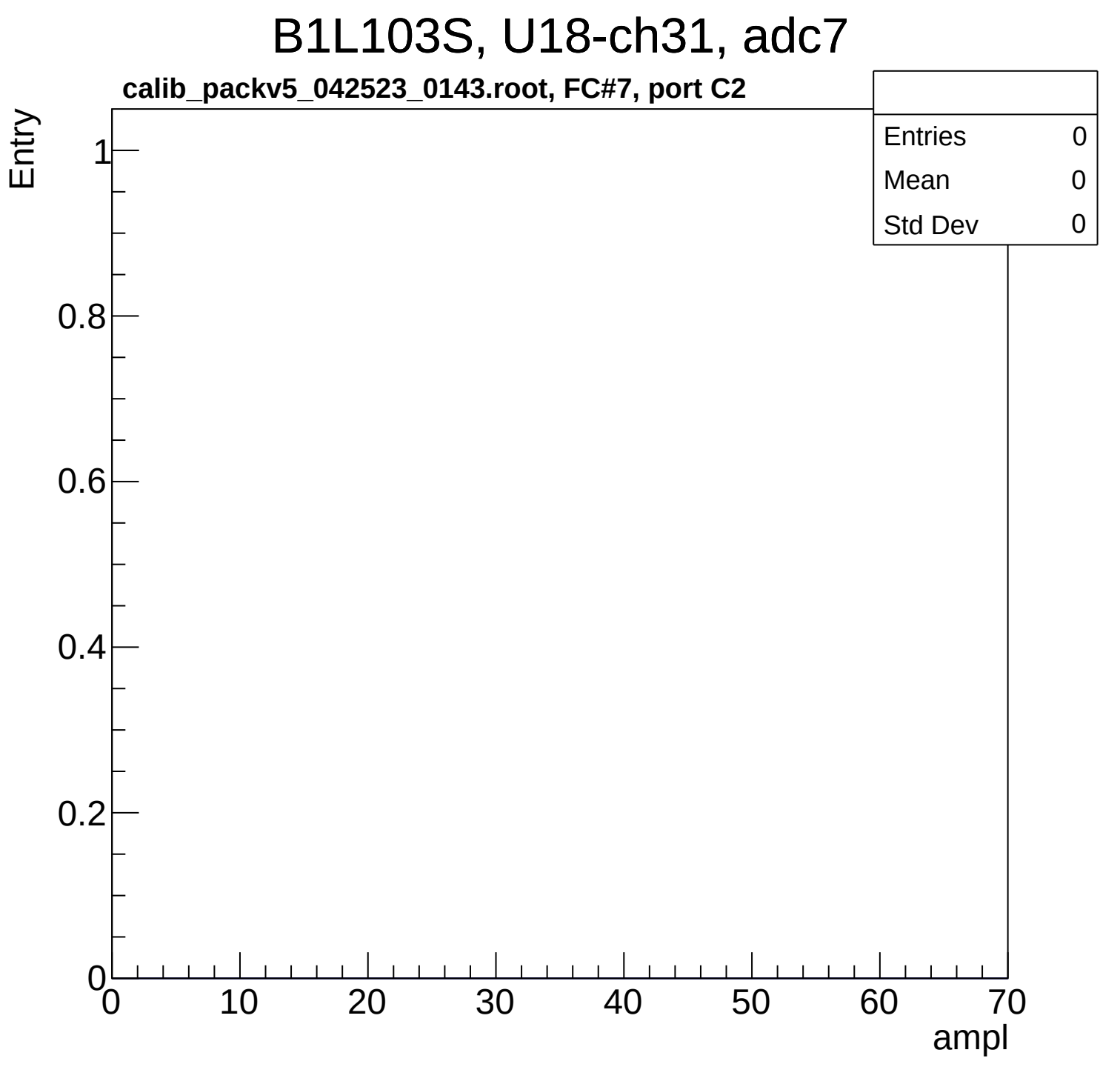
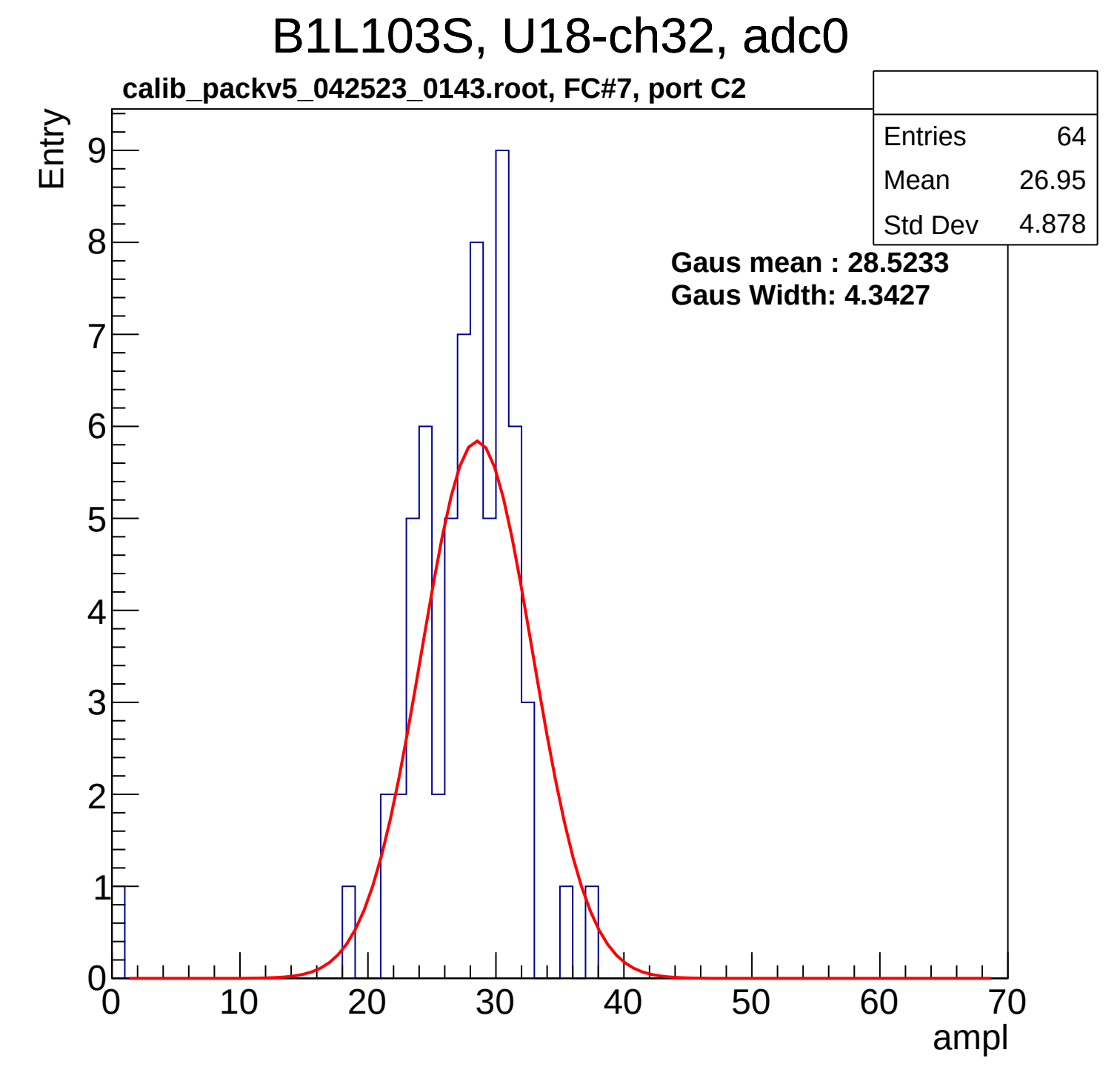
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch31, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 6
Mean 60.33
Std Dev 2.809
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U18-ch31, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch32, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 26.95
Std Dev 4.878
Gaus mean : 28.5233
Gaus Width: 4.3427
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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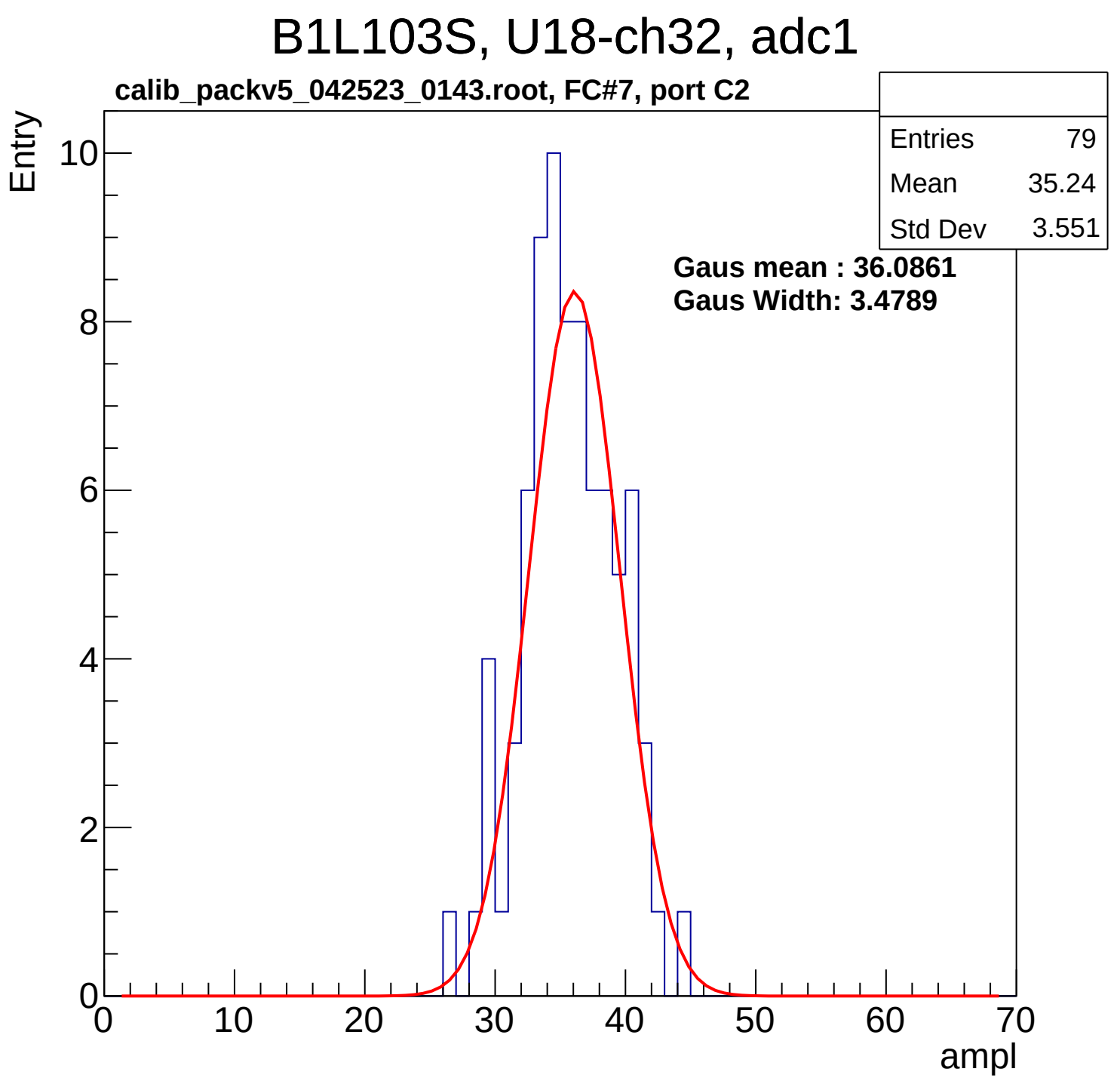
B1L103S, U18-ch32, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 79
Mean 35.24
Std Dev 3.551
Gaus mean : 36.0861
Gaus Width: 3.4789
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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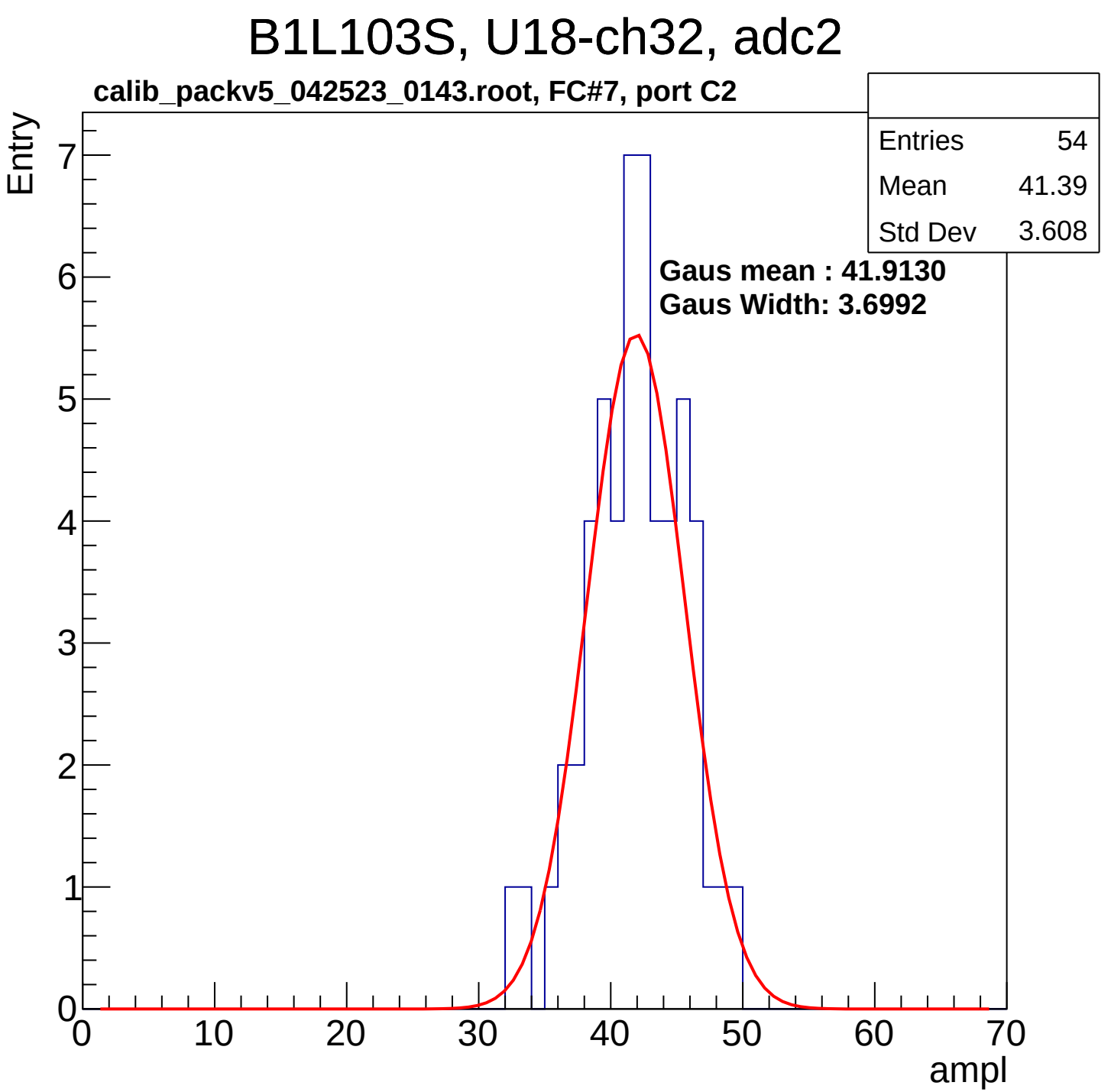
B1L103S, U18-ch32, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 54
Mean 41.39
Std Dev 3.608
Gaus mean : 41.9130
Gaus Width: 3.6992
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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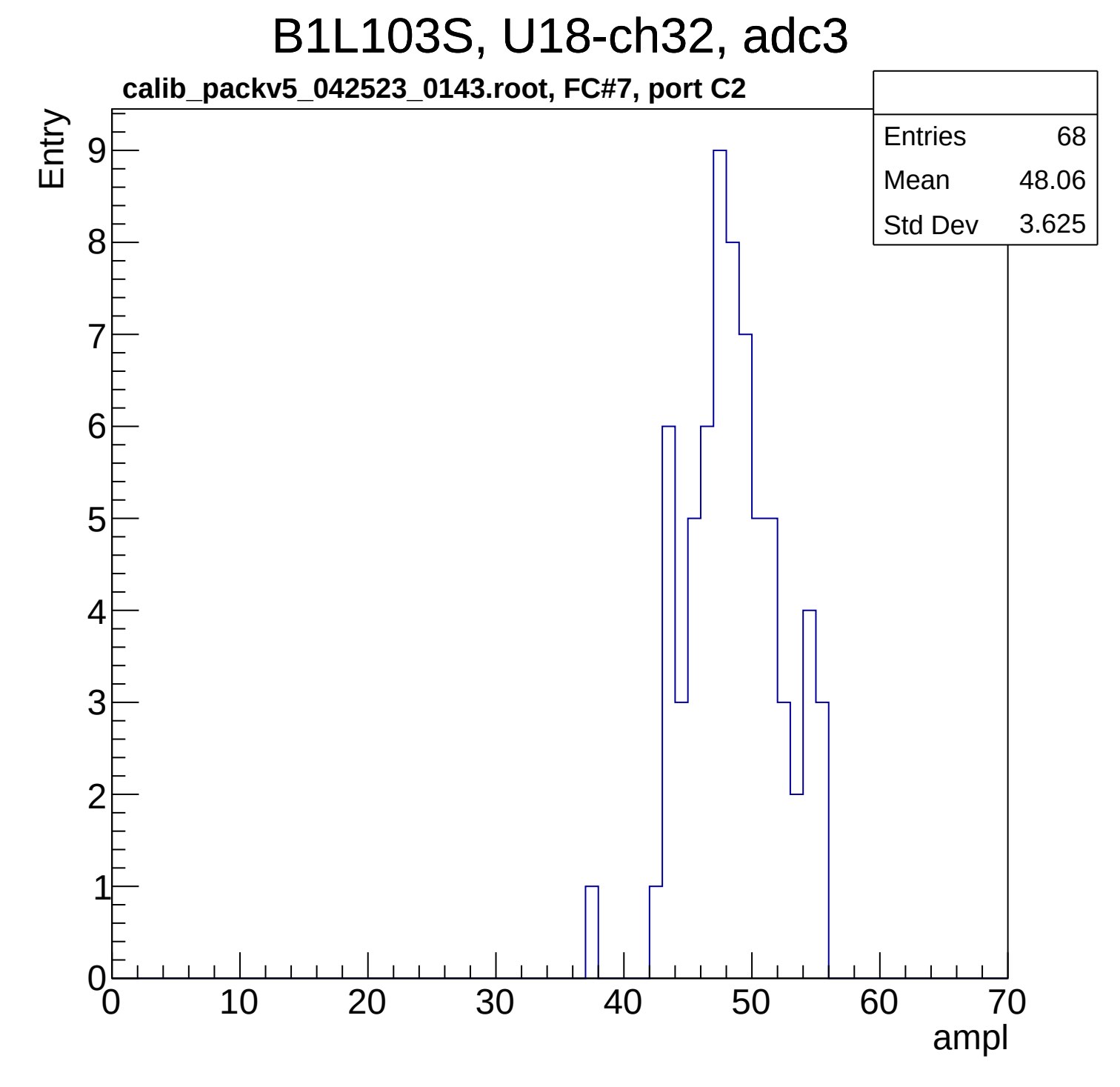
B1L103S, U18-ch32, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 48.06
Std Dev 3.625
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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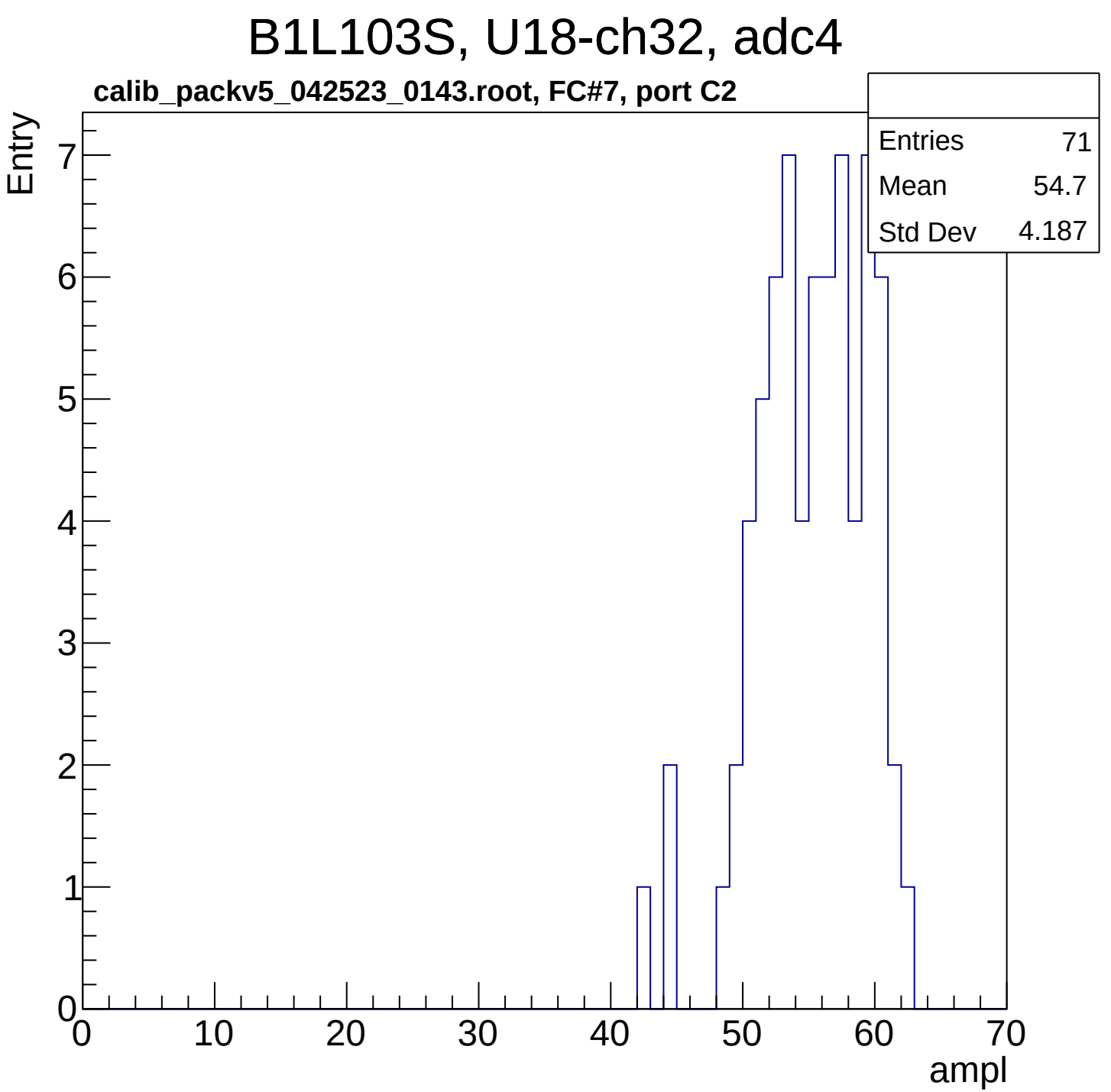
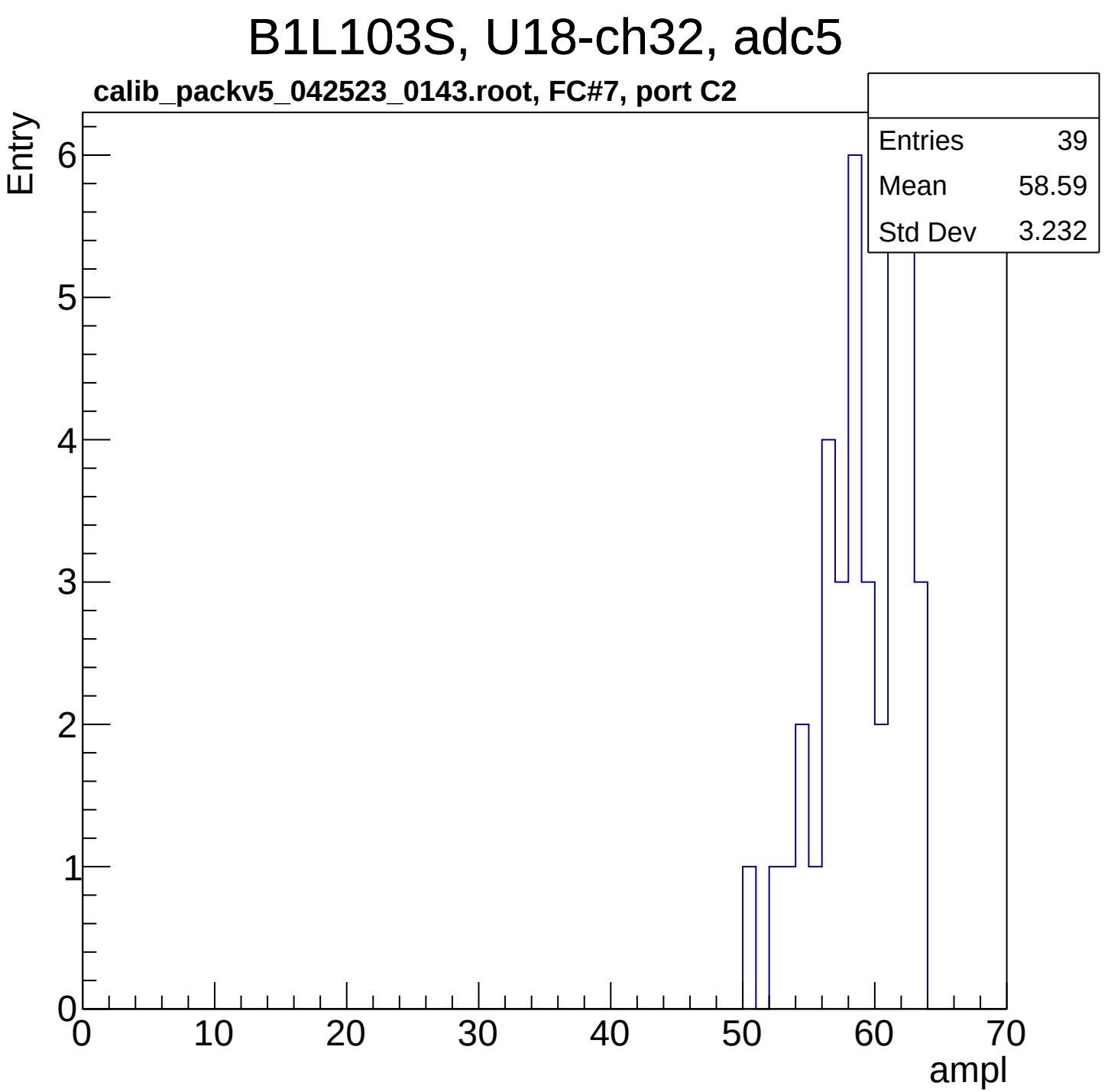

B1L103S, U18-ch32, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 71
Mean 54.7
Std Dev 4.187
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch32, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 39
Mean 58.59
Std Dev 3.232
Entry
ampl
0
1
2
3
4
5
6
0
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20
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40
50
60
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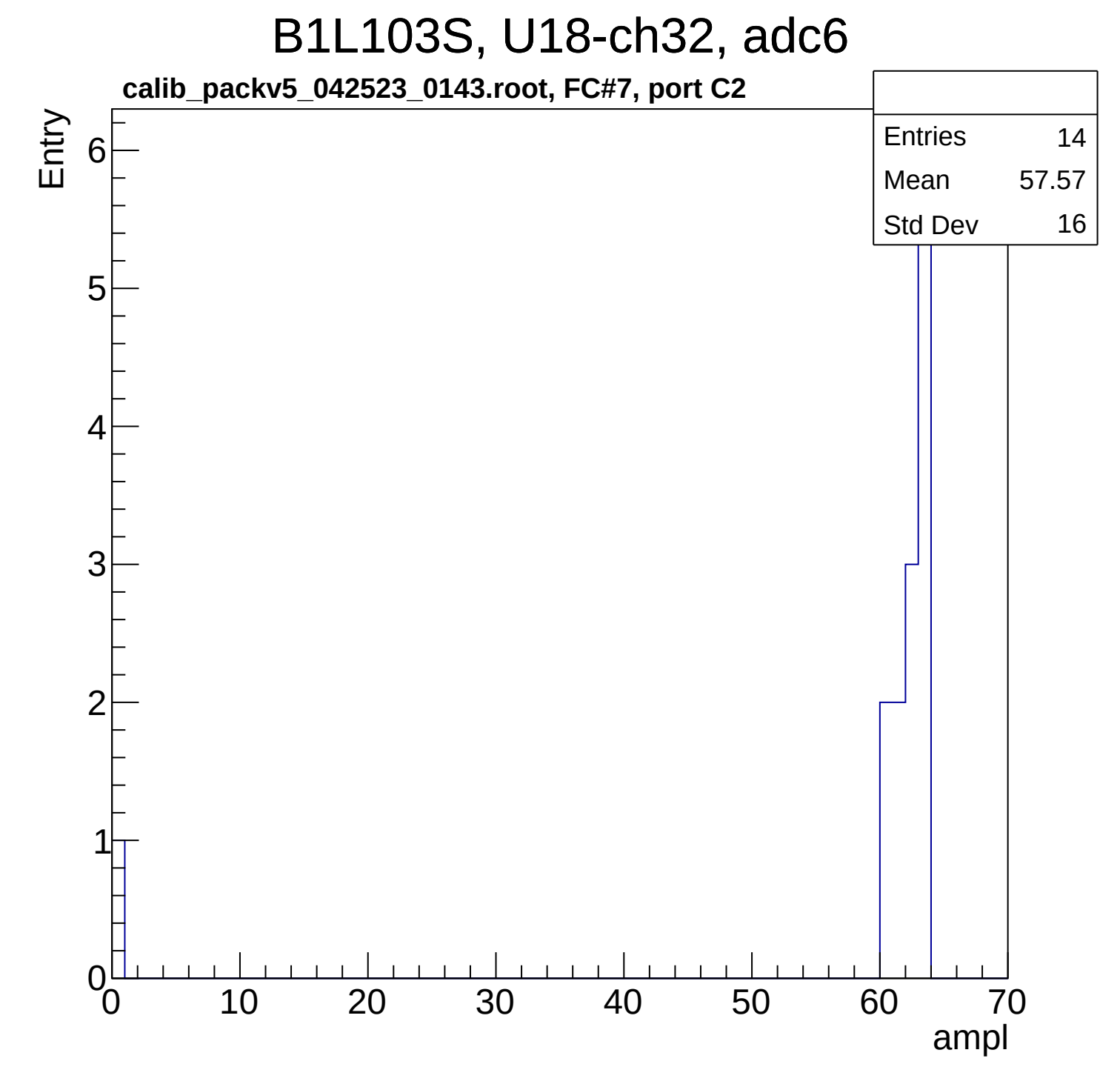
B1L103S, U18-ch32, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 14
Mean 57.57
Std Dev 16
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
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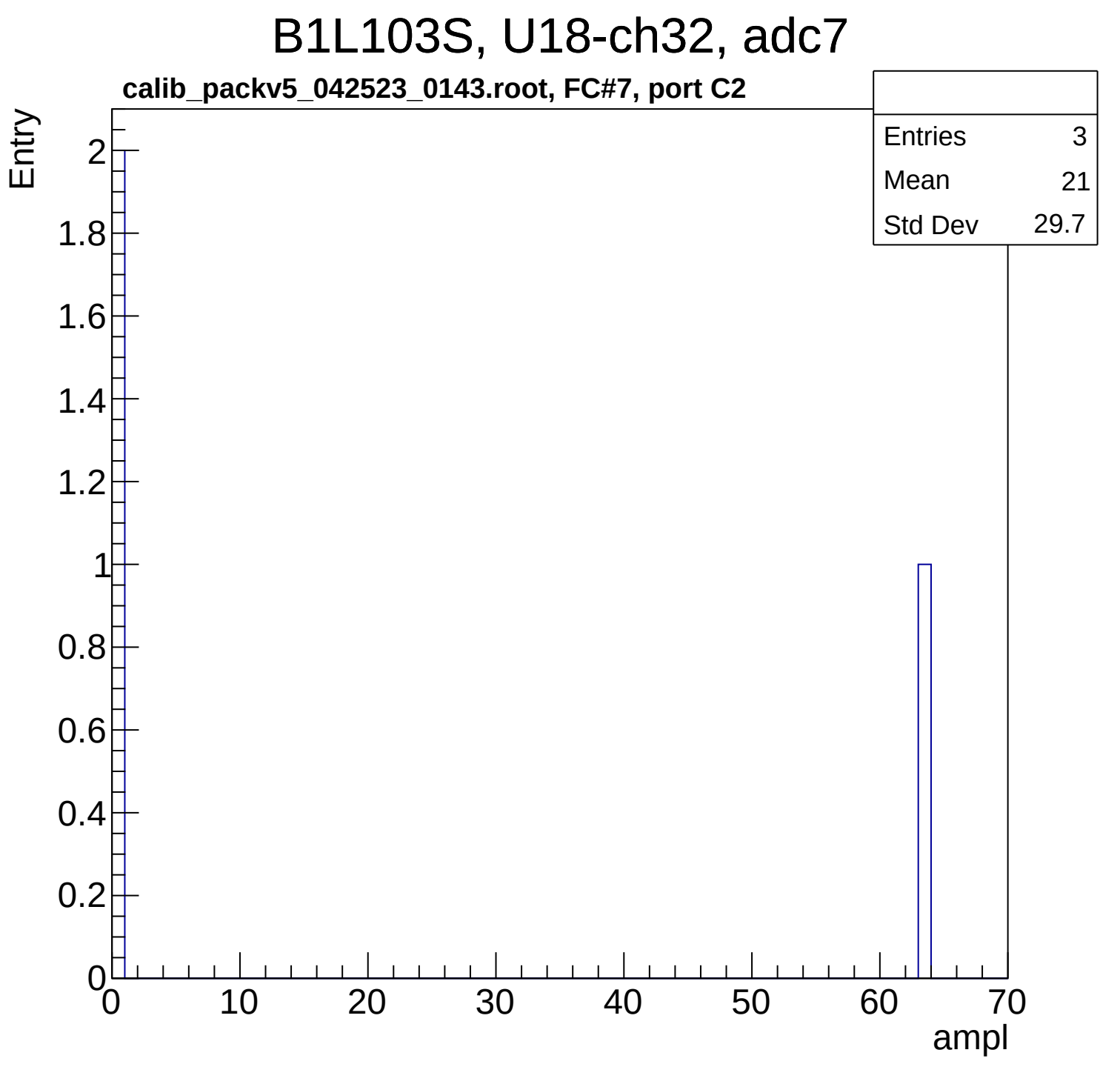
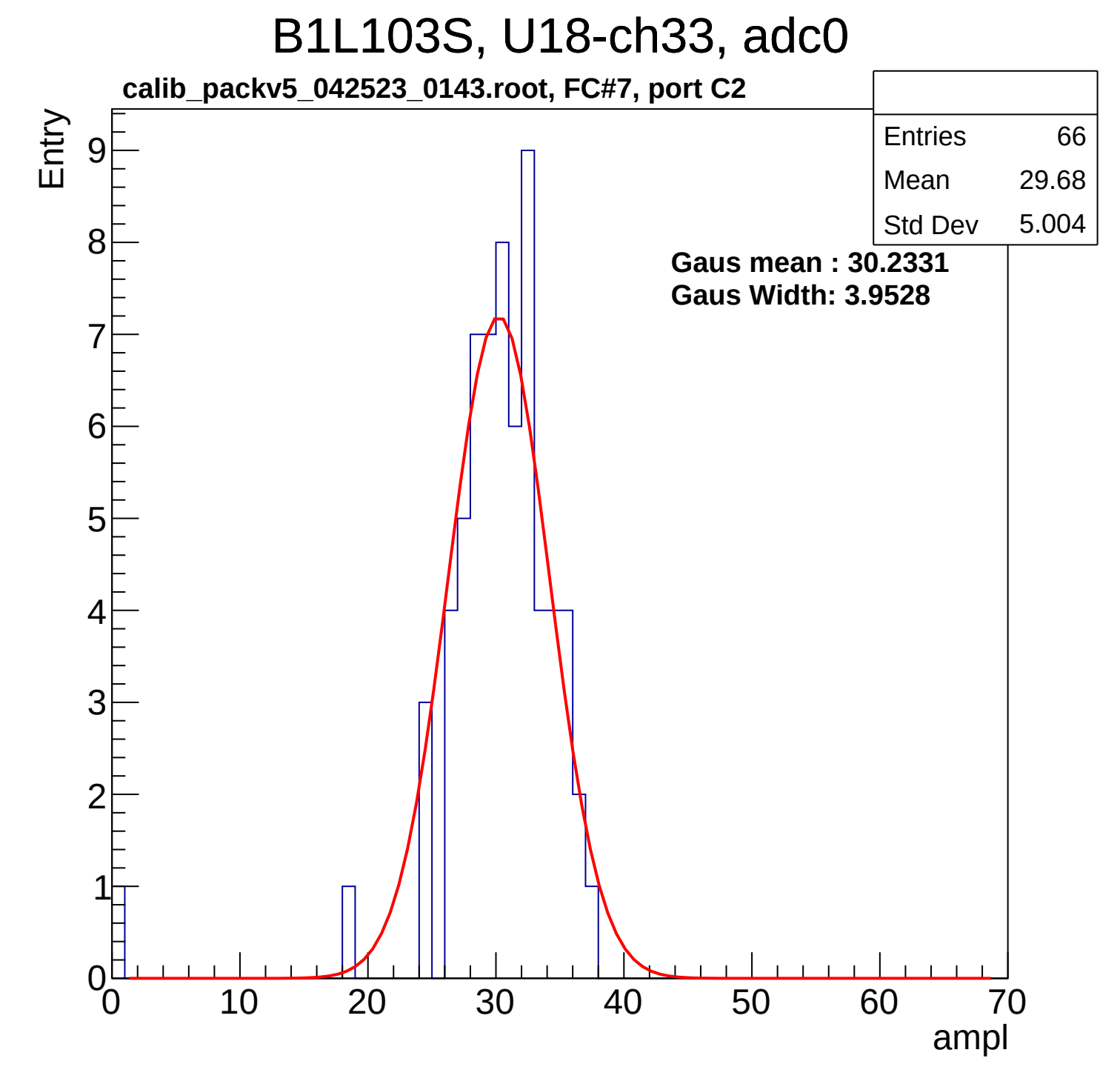
60
70


B1L103S, U18-ch32, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 21
Std Dev 29.7
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U18-ch33, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 29.68
Std Dev 5.004
Gaus mean : 30.2331
Gaus Width: 3.9528
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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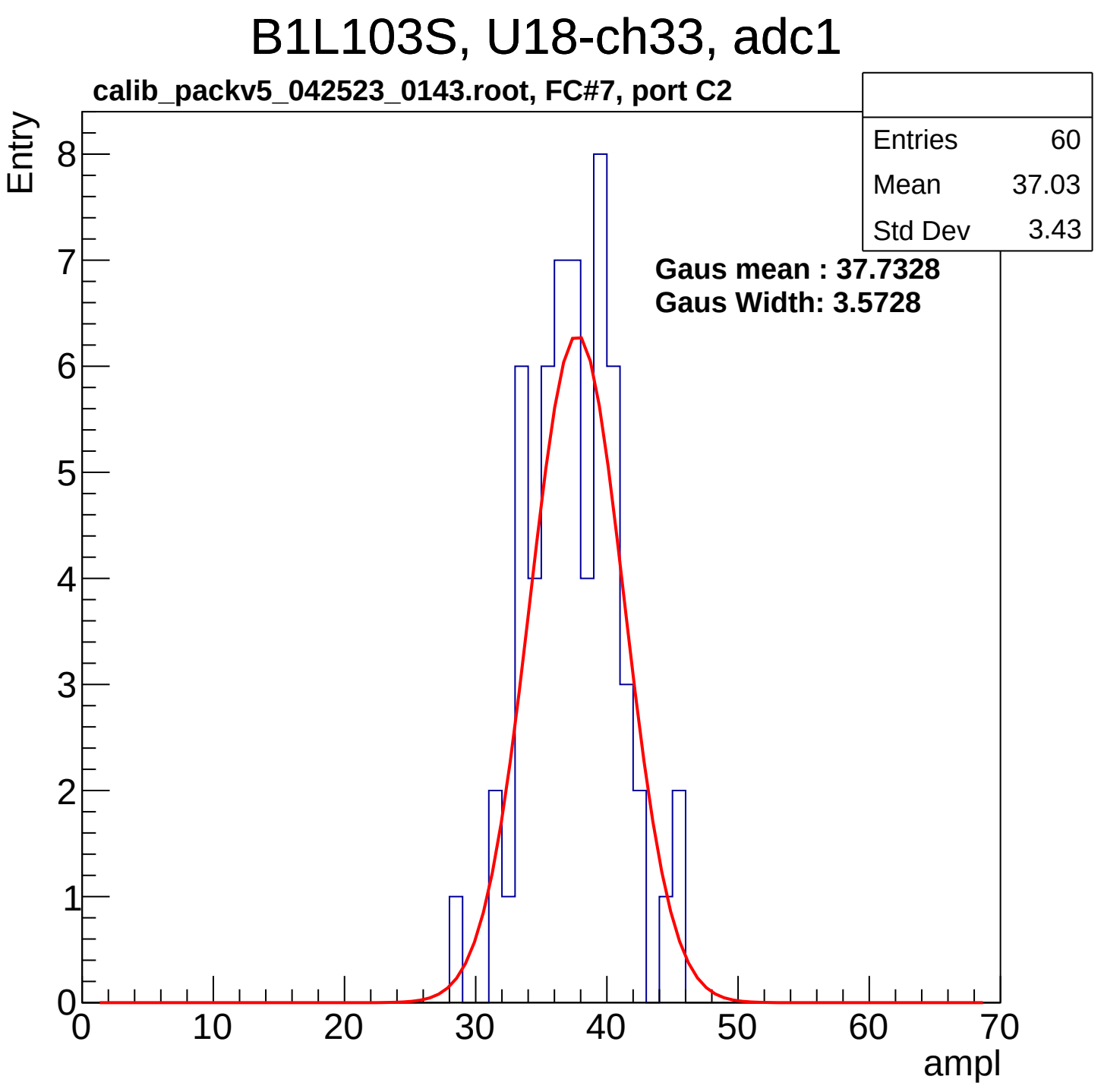
B1L103S, U18-ch33, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 60
Mean 37.03
Std Dev 3.43
Gaus mean : 37.7328
Gaus Width: 3.5728
Entry
ampl
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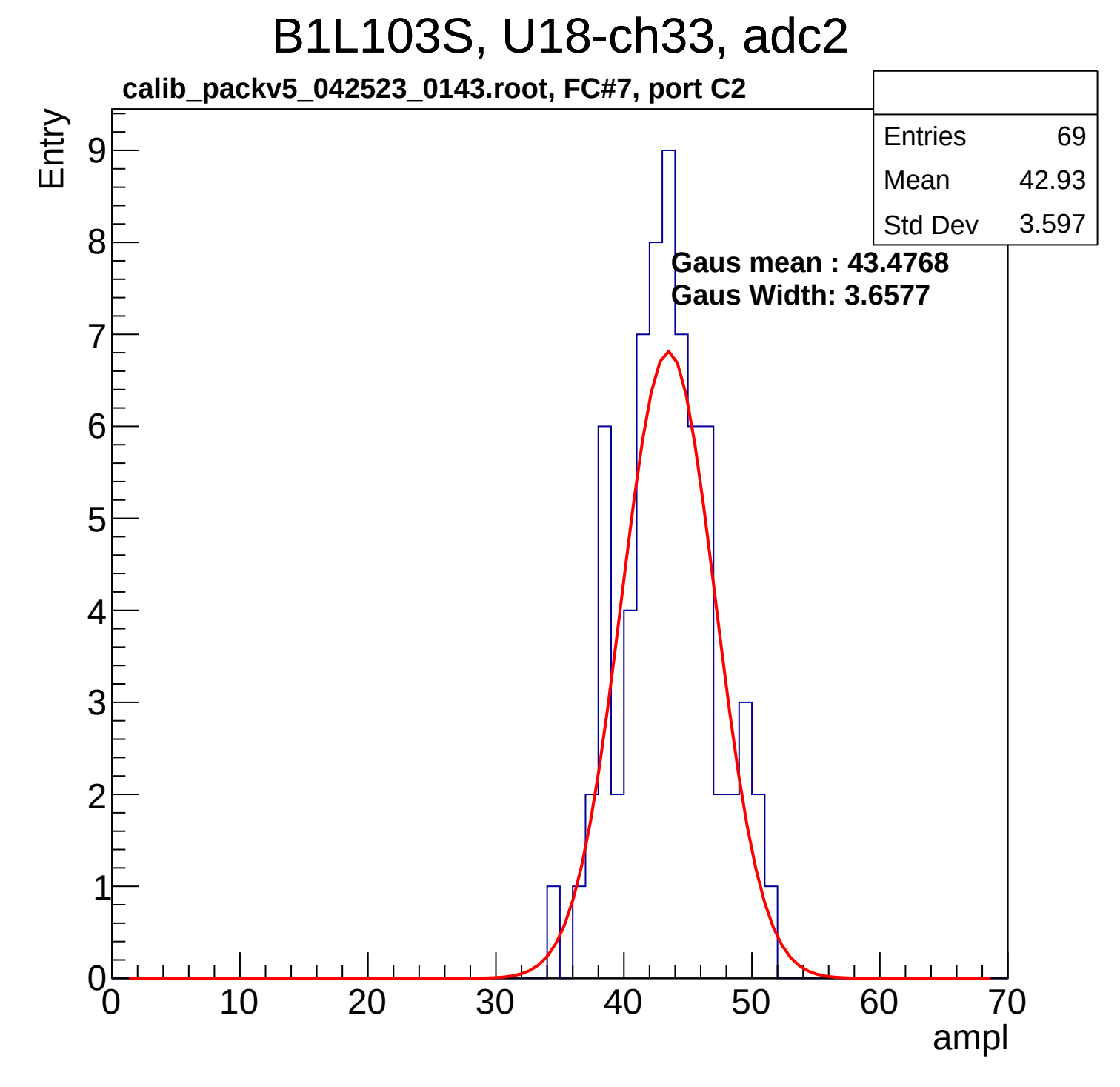
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch33, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 42.93
Std Dev 3.597
Gaus mean : 43.4768
Gaus Width: 3.6577
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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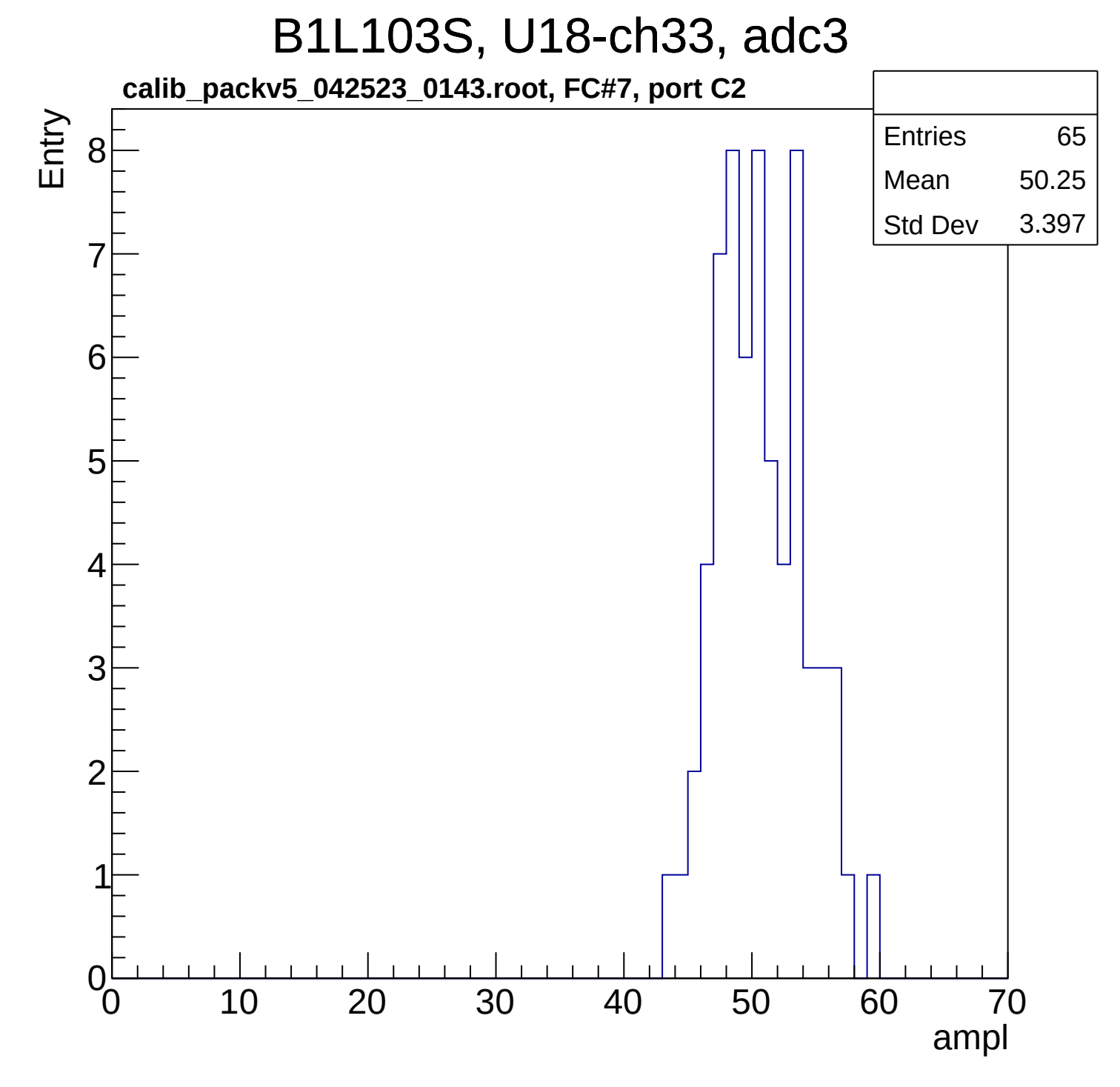
B1L103S, U18-ch33, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 50.25
Std Dev 3.397
Entry
ampl
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4
5
6
7
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0
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20
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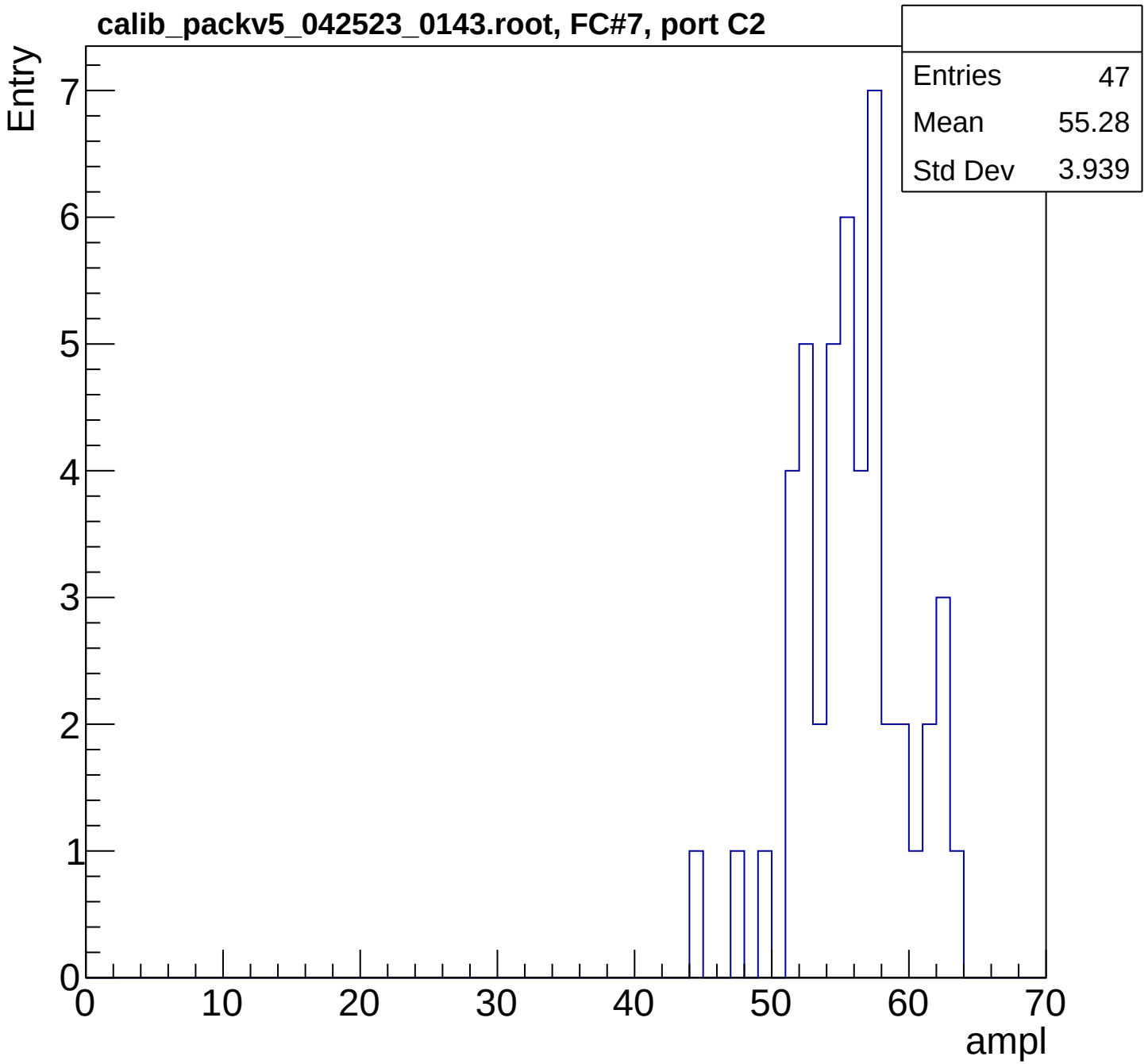
40
50
60
70


B1L103S, U18-ch33, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 47
Mean 55.28
Std Dev 3.939
Entry
ampl
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4
5
6
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0
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40
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60
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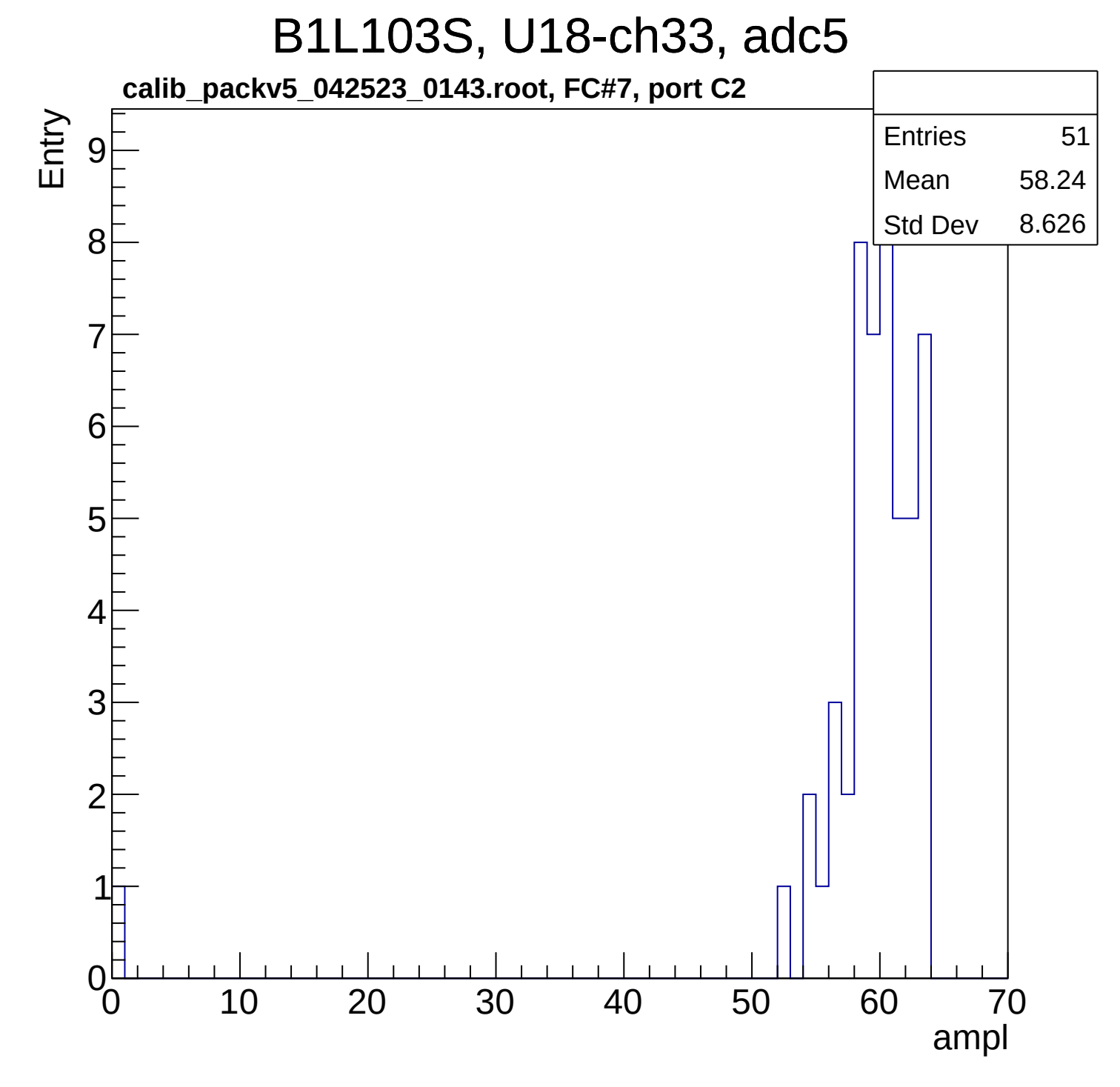
B1L103S, U18-ch33, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 51
Mean 58.24
Std Dev 8.626
Entry
ampl
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2
3
4
5
6
7
8
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0
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20
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40
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60
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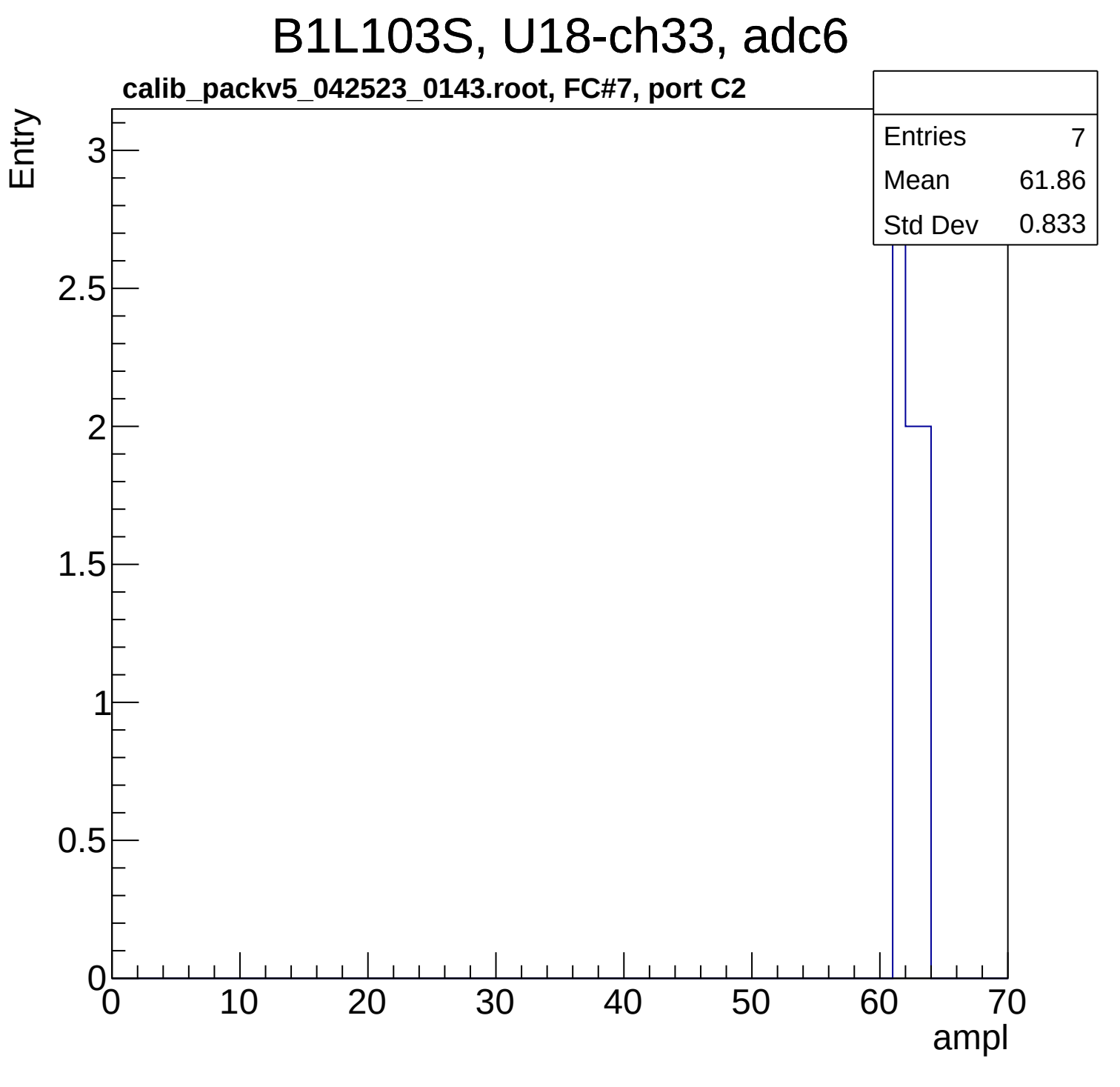
B1L103S, U18-ch33, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 7
Mean 61.86
Std Dev 0.833
Entry
ampl
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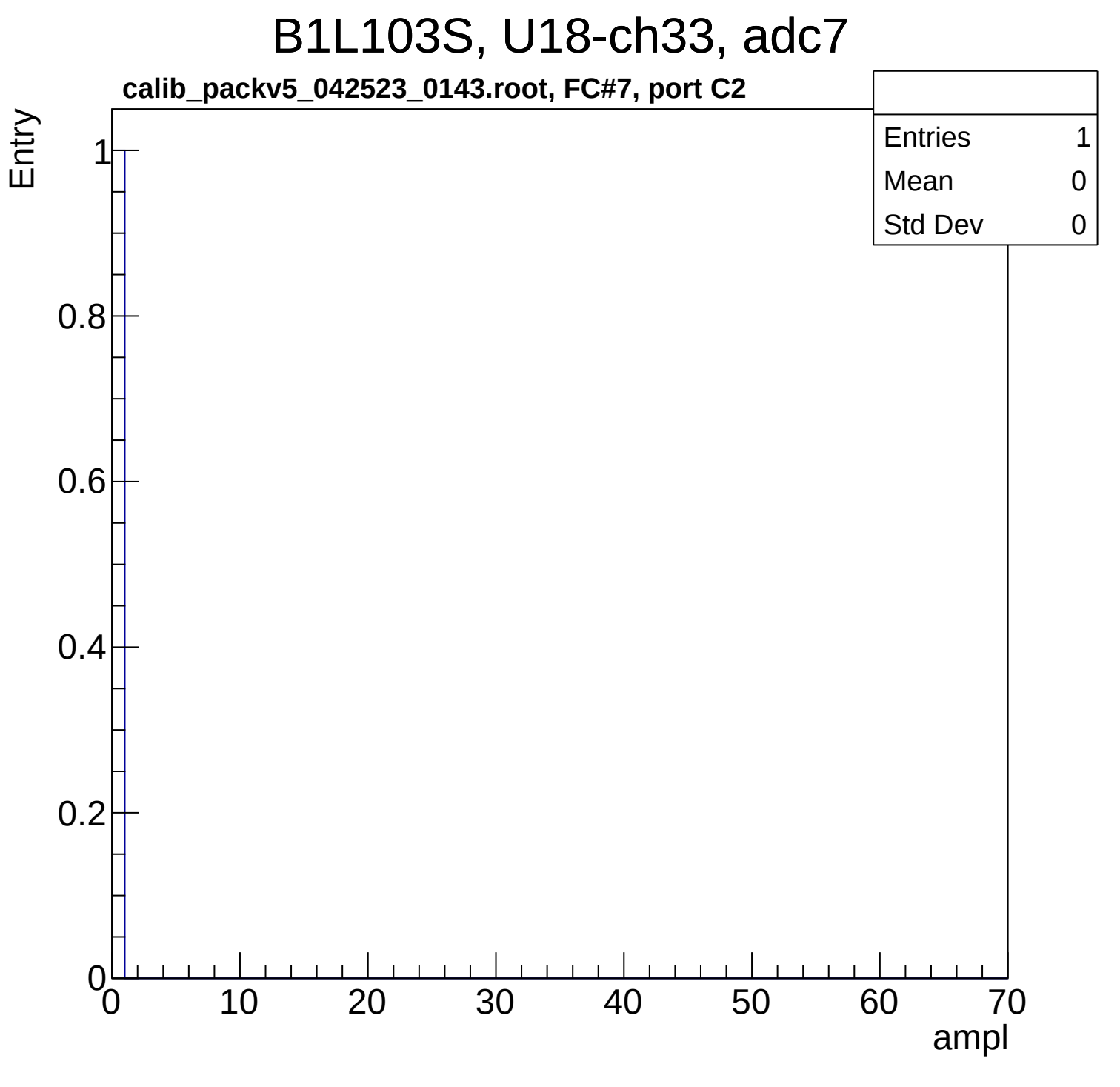
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U18-ch33, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
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0.6
0.4
0.2
0
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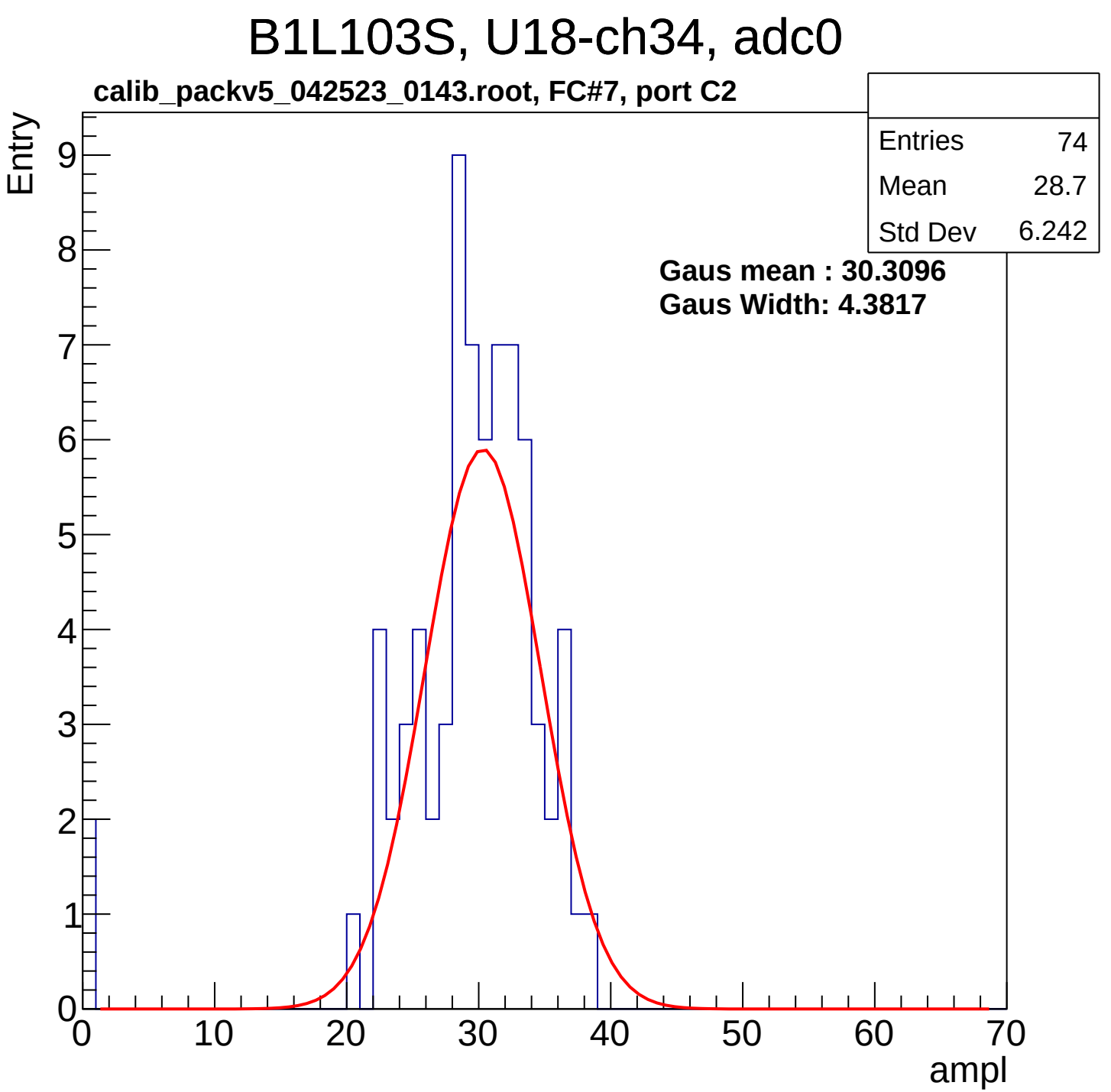
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch34, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 74
Mean 28.7
Std Dev 6.242
Gaus mean : 30.3096
Gaus Width: 4.3817
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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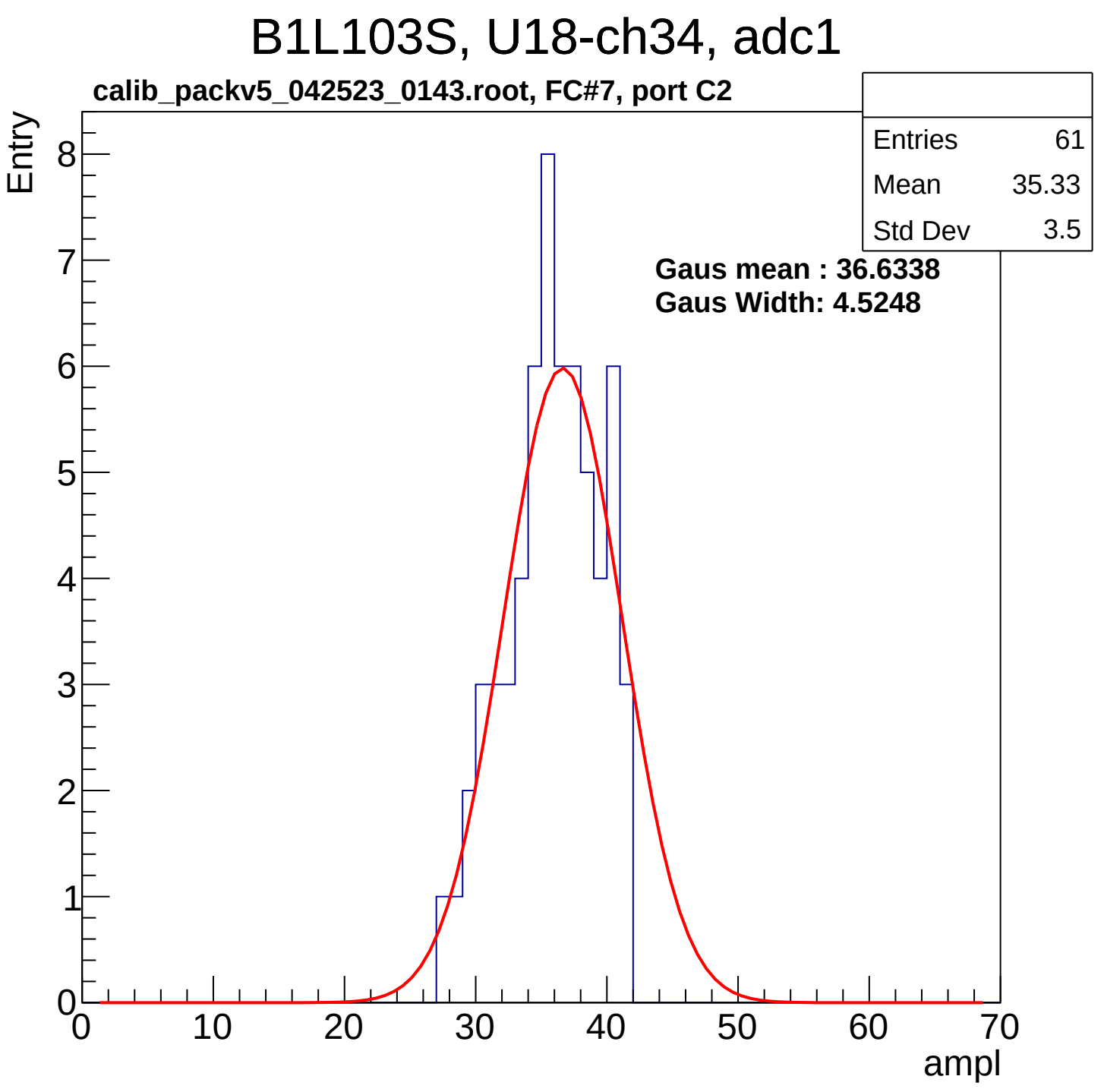
B1L103S, U18-ch34, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 61
Mean 35.33
Std Dev 3.5
Gaus mean : 36.6338
Gaus Width: 4.5248
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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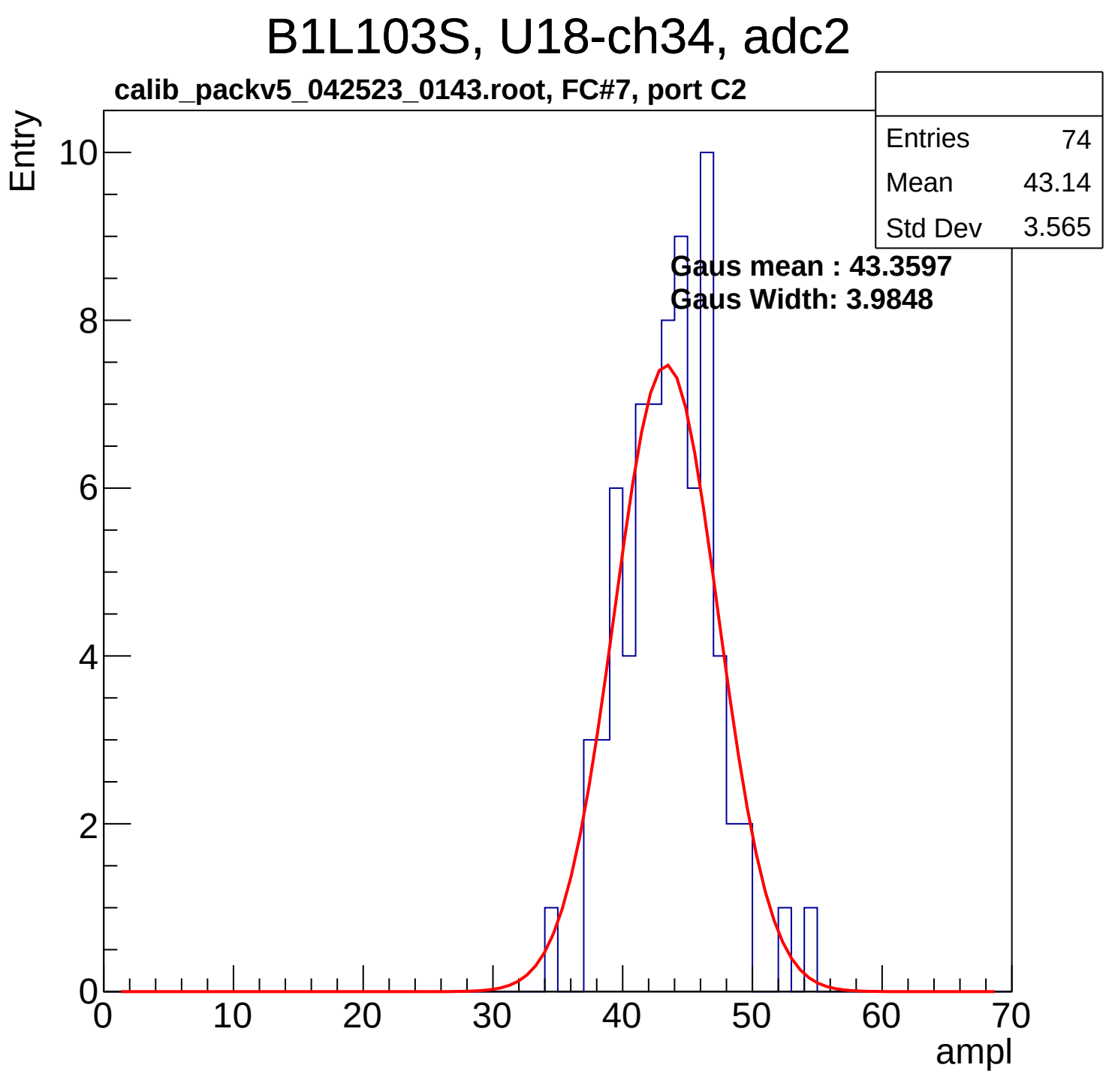
B1L103S, U18-ch34, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 74
Mean 43.14
Std Dev 3.565
Gaus mean : 43.3597
Gaus Width: 3.9848
Entry
ampl
0
2
4
6
8
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0
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20
30
40
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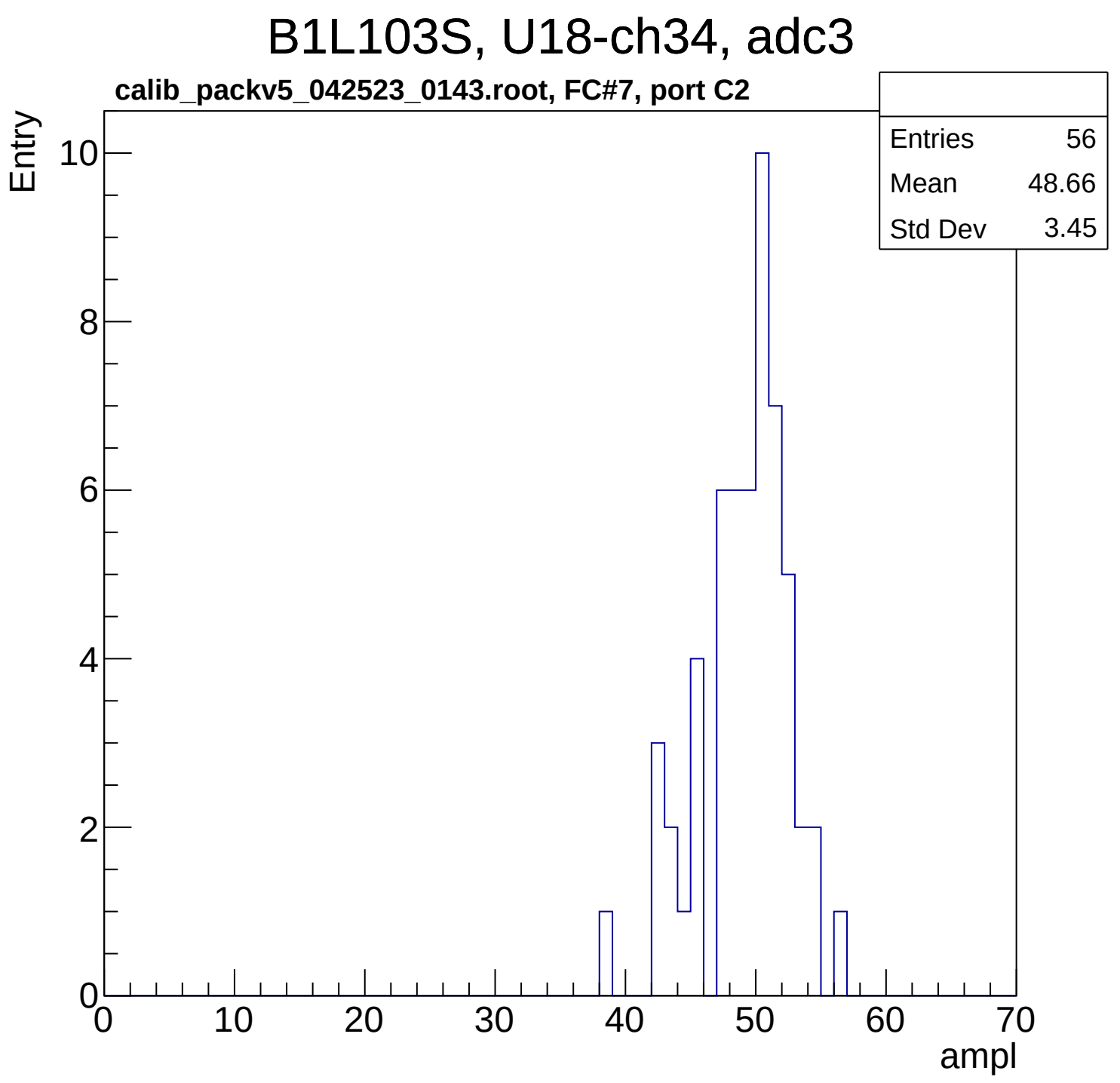
B1L103S, U18-ch34, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 48.66
Std Dev 3.45
Entry
ampl
0
2
4
6
8
10
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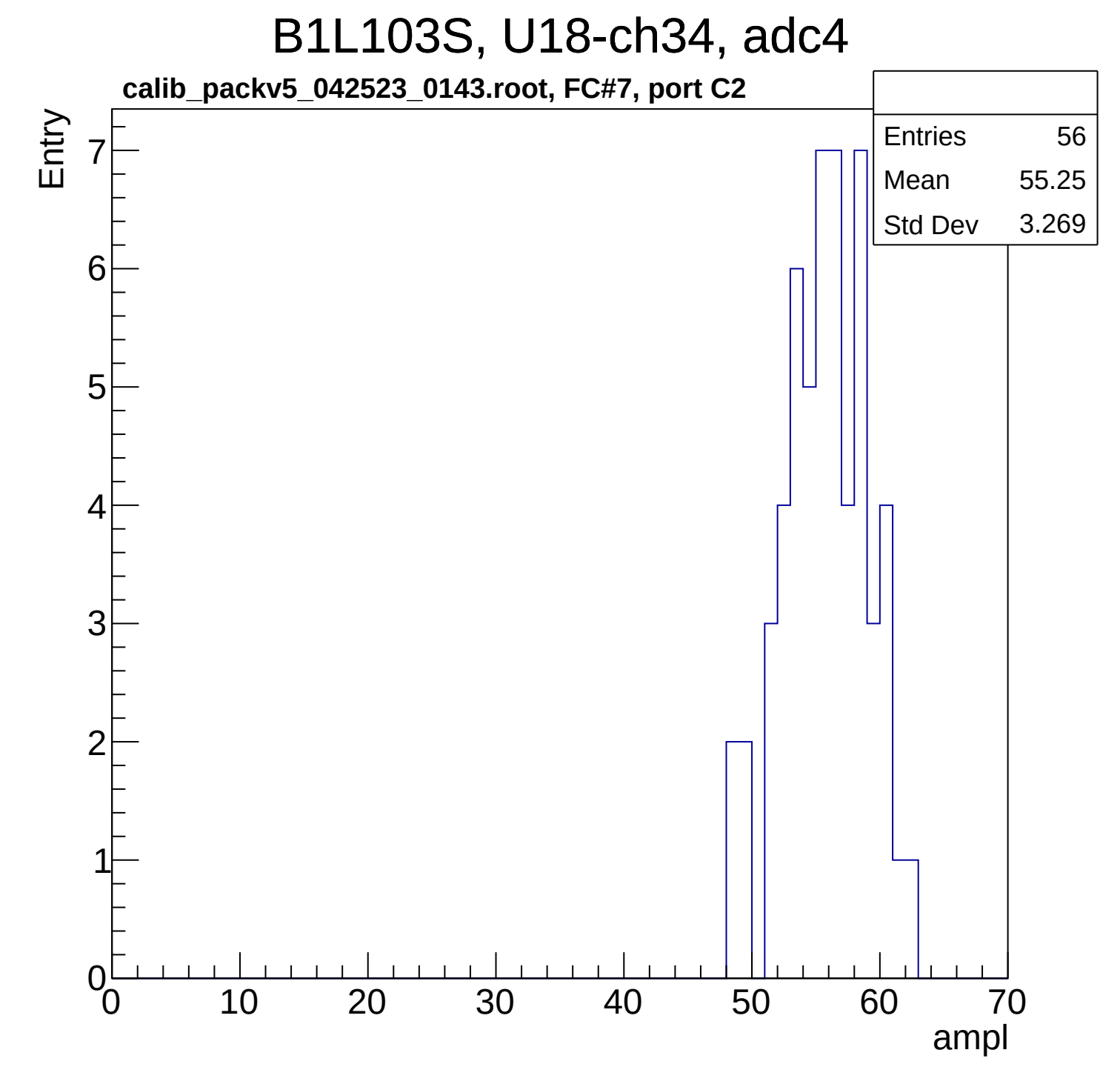
B1L103S, U18-ch34, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 55.25
Std Dev 3.269
Entry
ampl
0
1
2
3
4
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0
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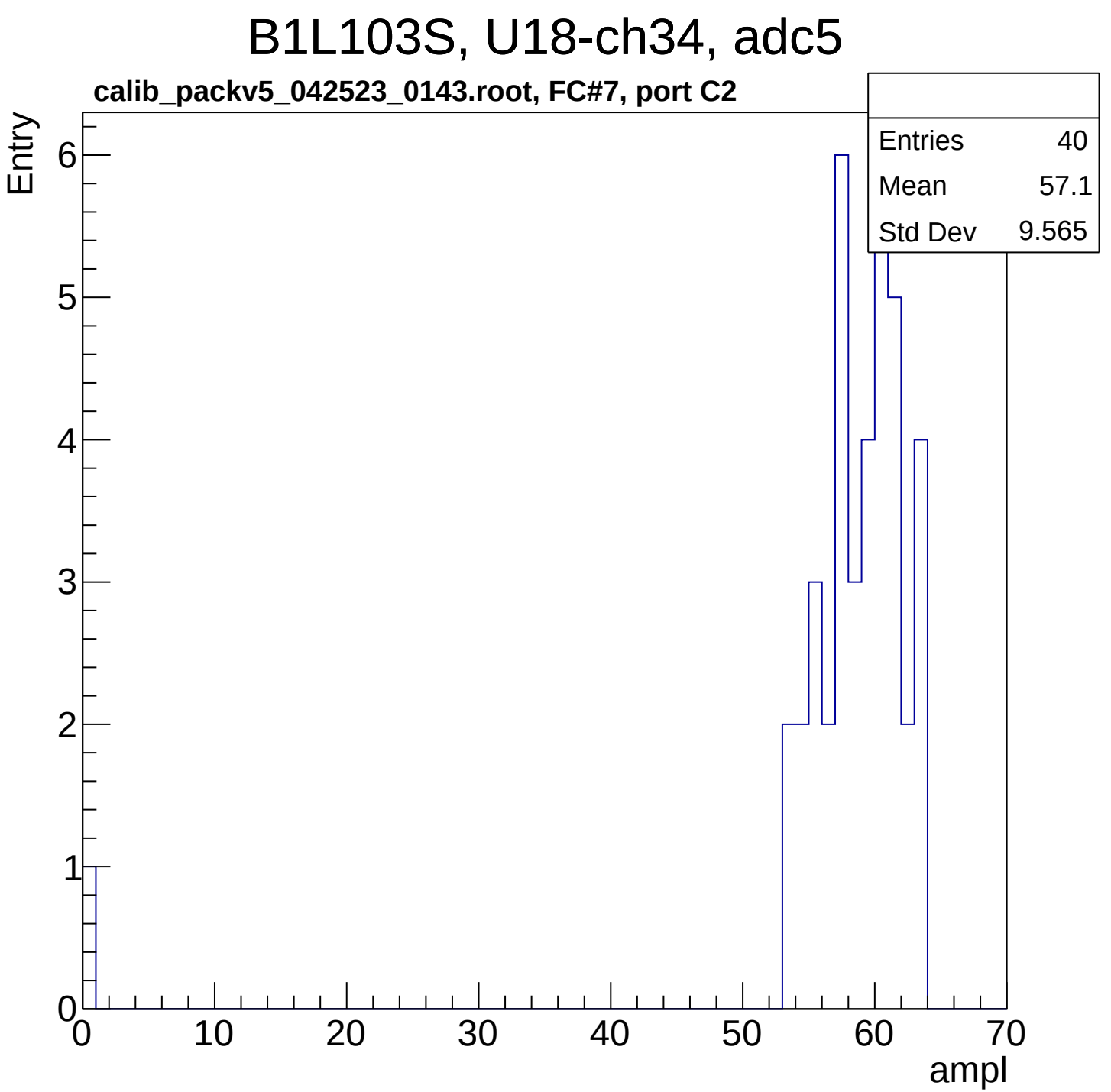
B1L103S, U18-ch34, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 40
Mean 57.1
Std Dev 9.565
Entry
0
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4
5
6
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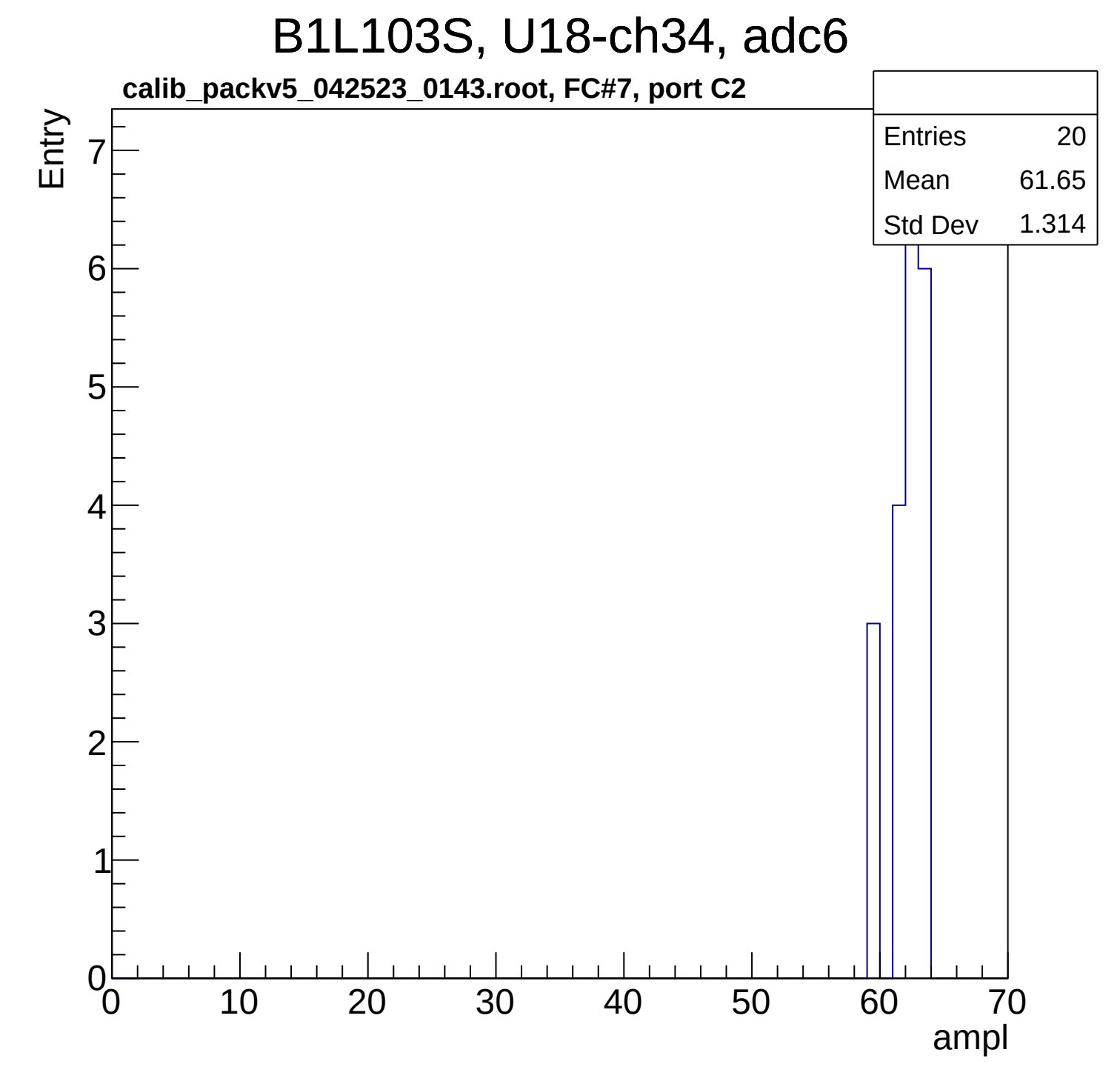
60
70
ampl


B1L103S, U18-ch34, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 20
Mean 61.65
Std Dev 1.314
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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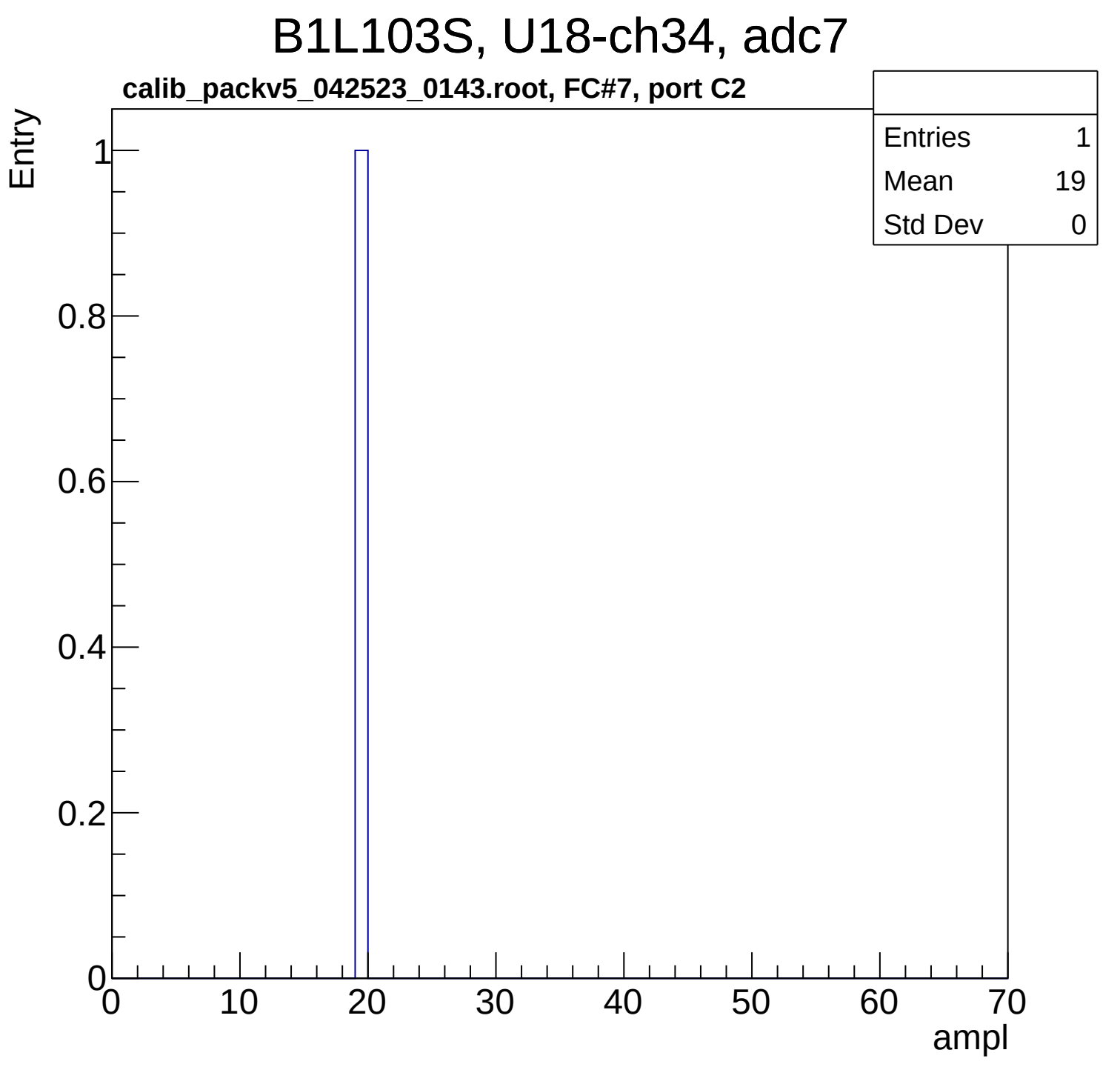
B1L103S, U18-ch34, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 19
Std Dev 0
Entry
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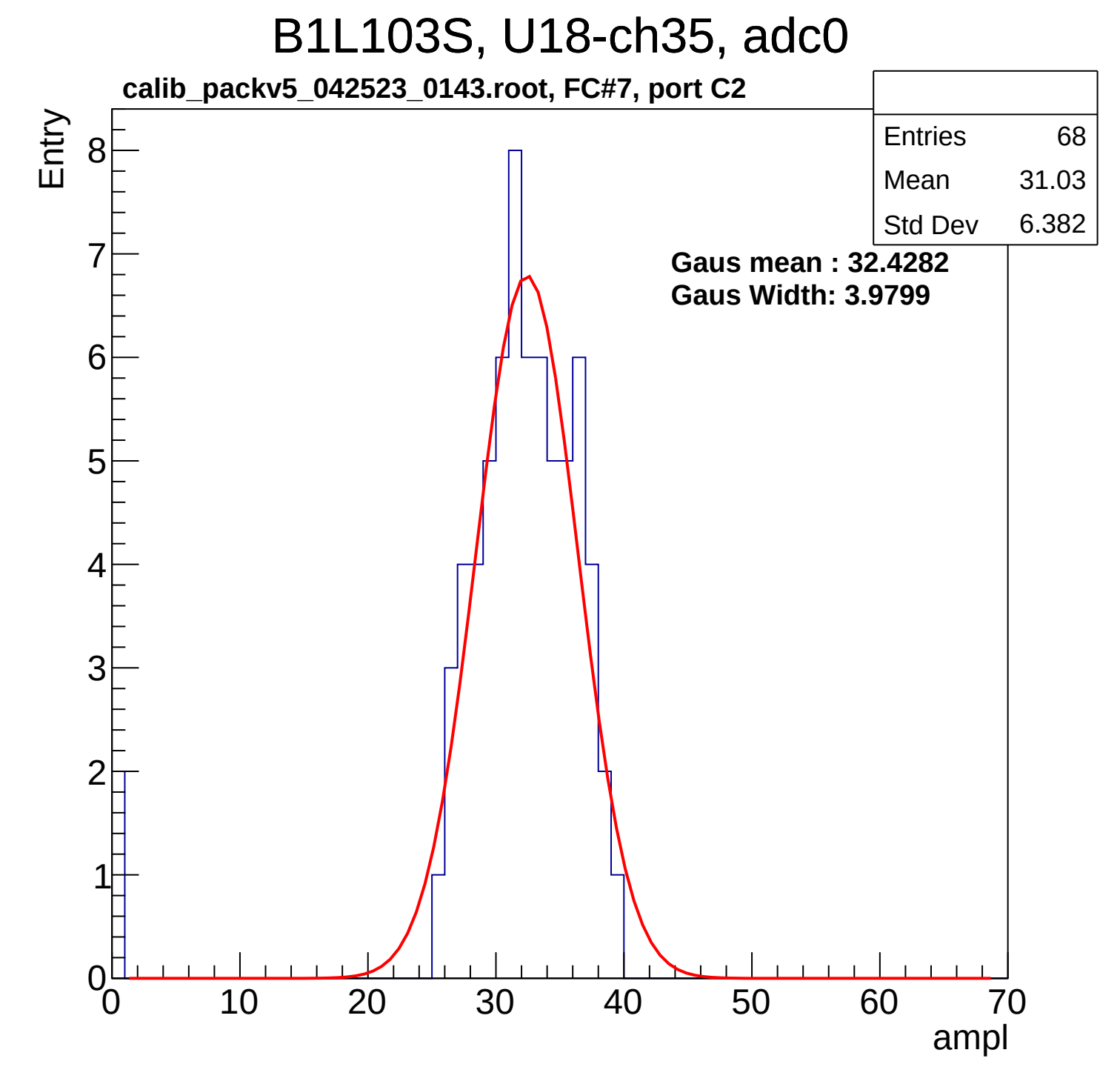
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch35, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 31.03
Std Dev 6.382
Gaus mean : 32.4282
Gaus Width: 3.9799
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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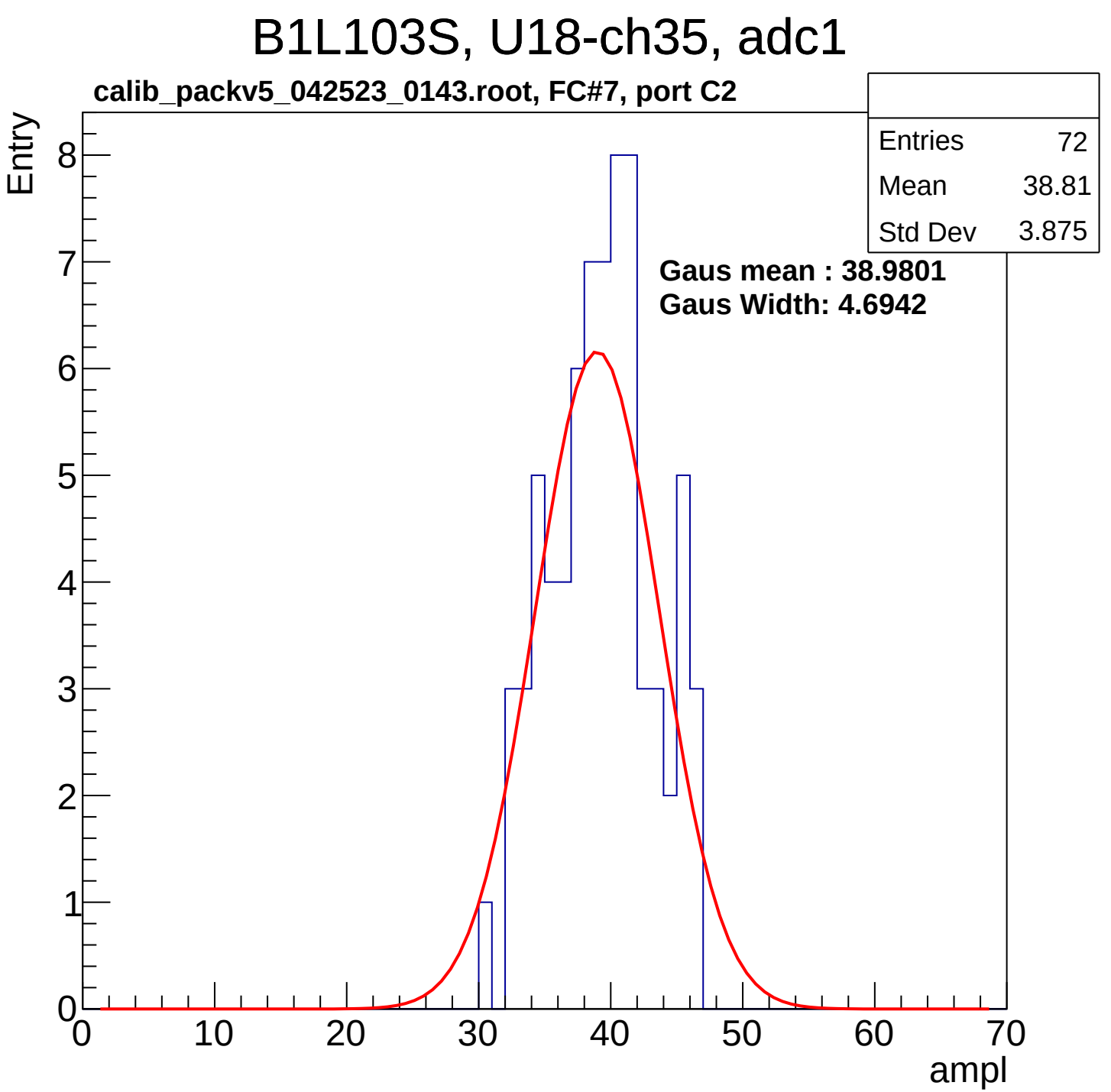
B1L103S, U18-ch35, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 72
Mean 38.81
Std Dev 3.875
Gaus mean : 38.9801
Gaus Width: 4.6942
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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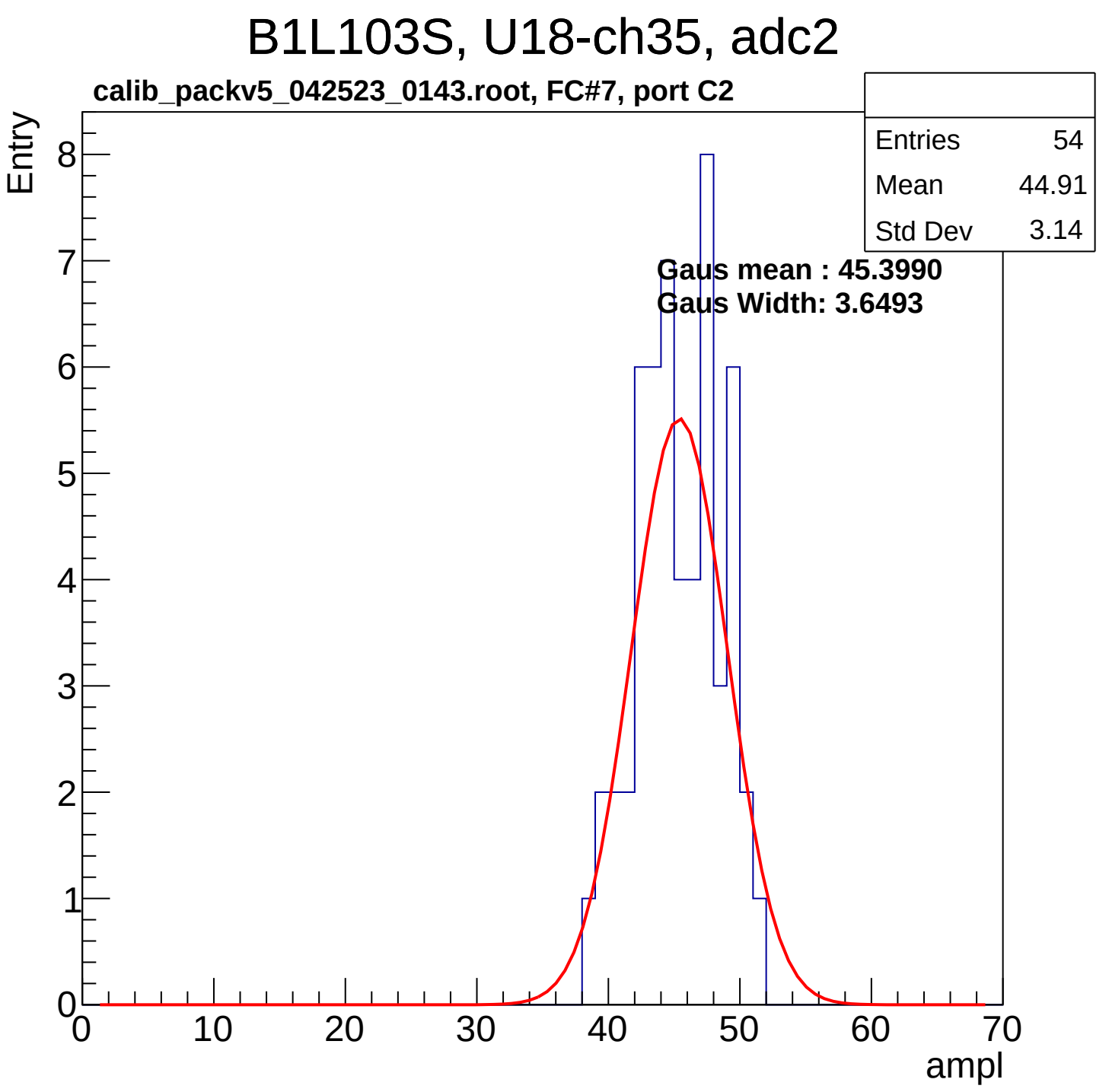
B1L103S, U18-ch35, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 54
Mean 44.91
Std Dev 3.14
Gaus mean : 45.3990
Gaus Width: 3.6493
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
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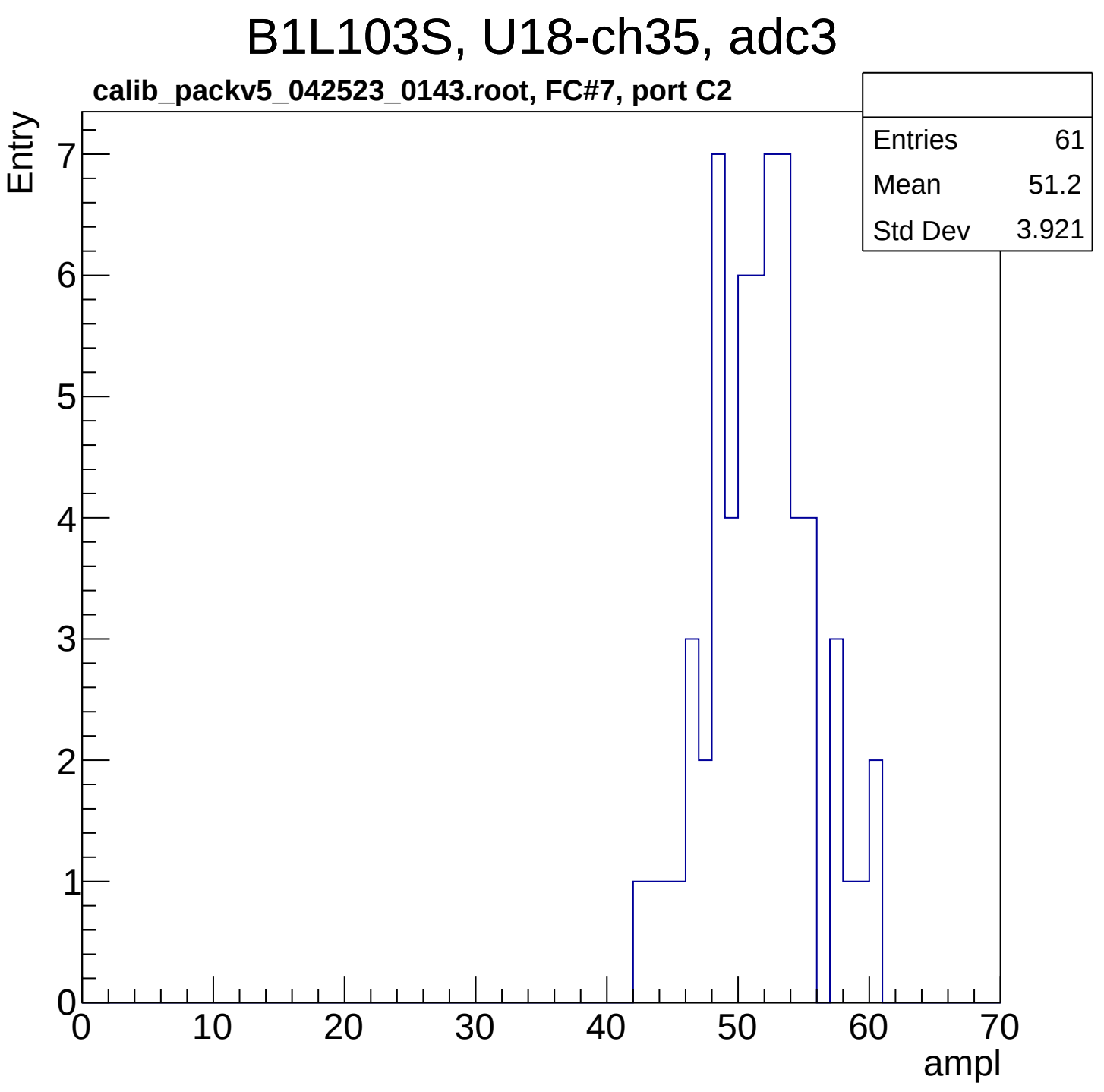
B1L103S, U18-ch35, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 61
Mean 51.2
Std Dev 3.921
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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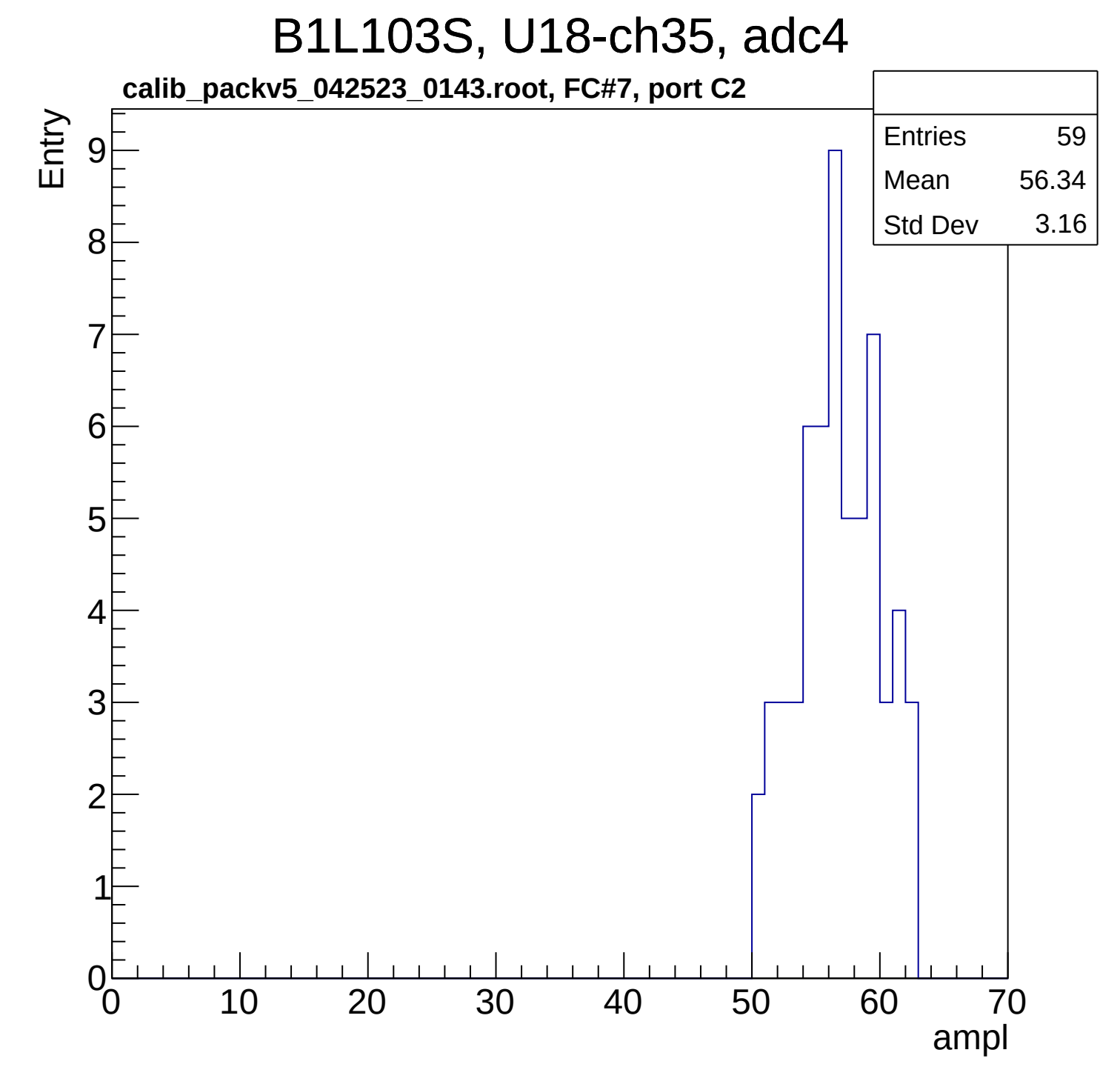
B1L103S, U18-ch35, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 56.34
Std Dev 3.16
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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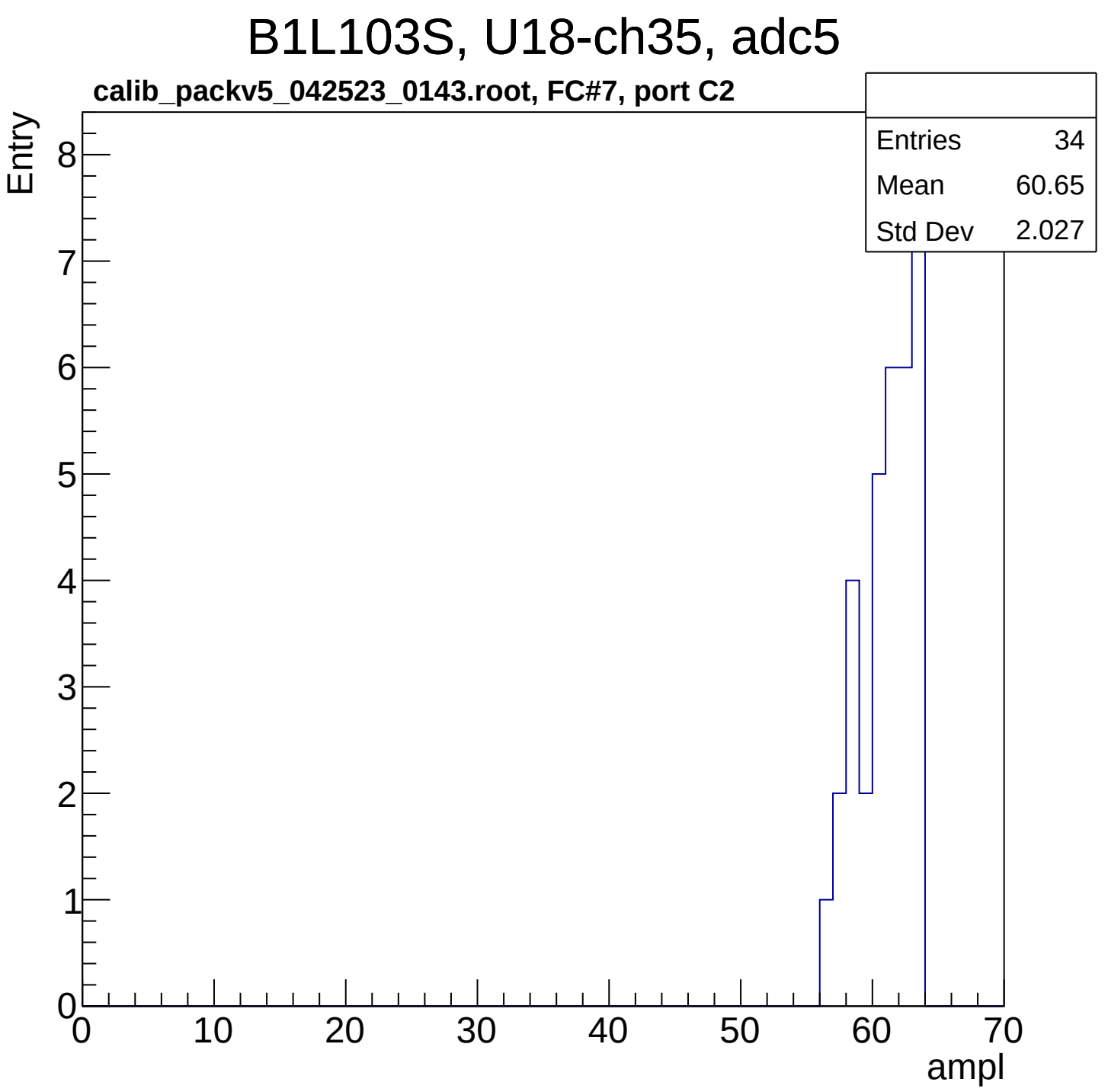
B1L103S, U18-ch35, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 34
Mean 60.65
Std Dev 2.027
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
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60
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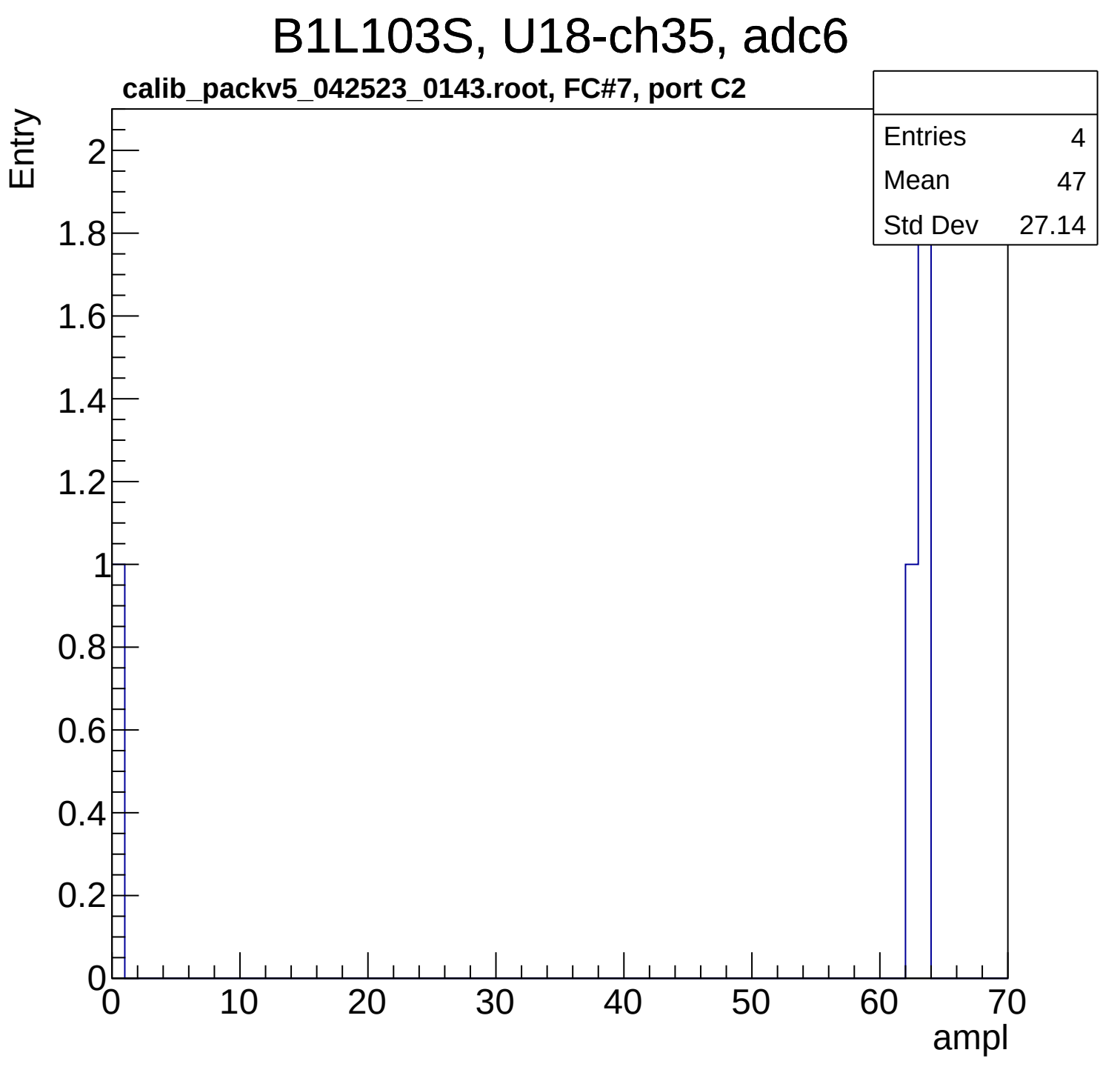
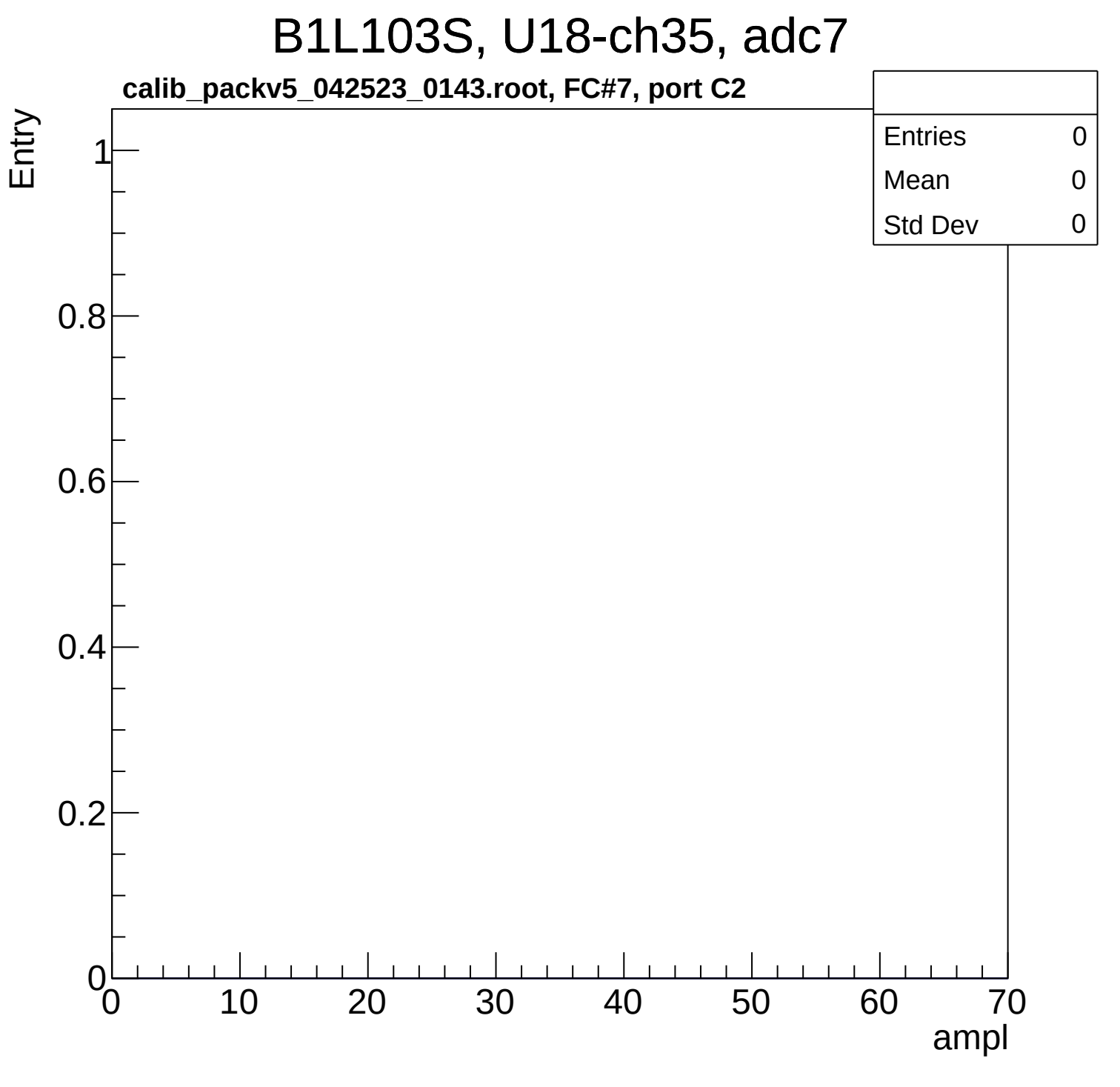
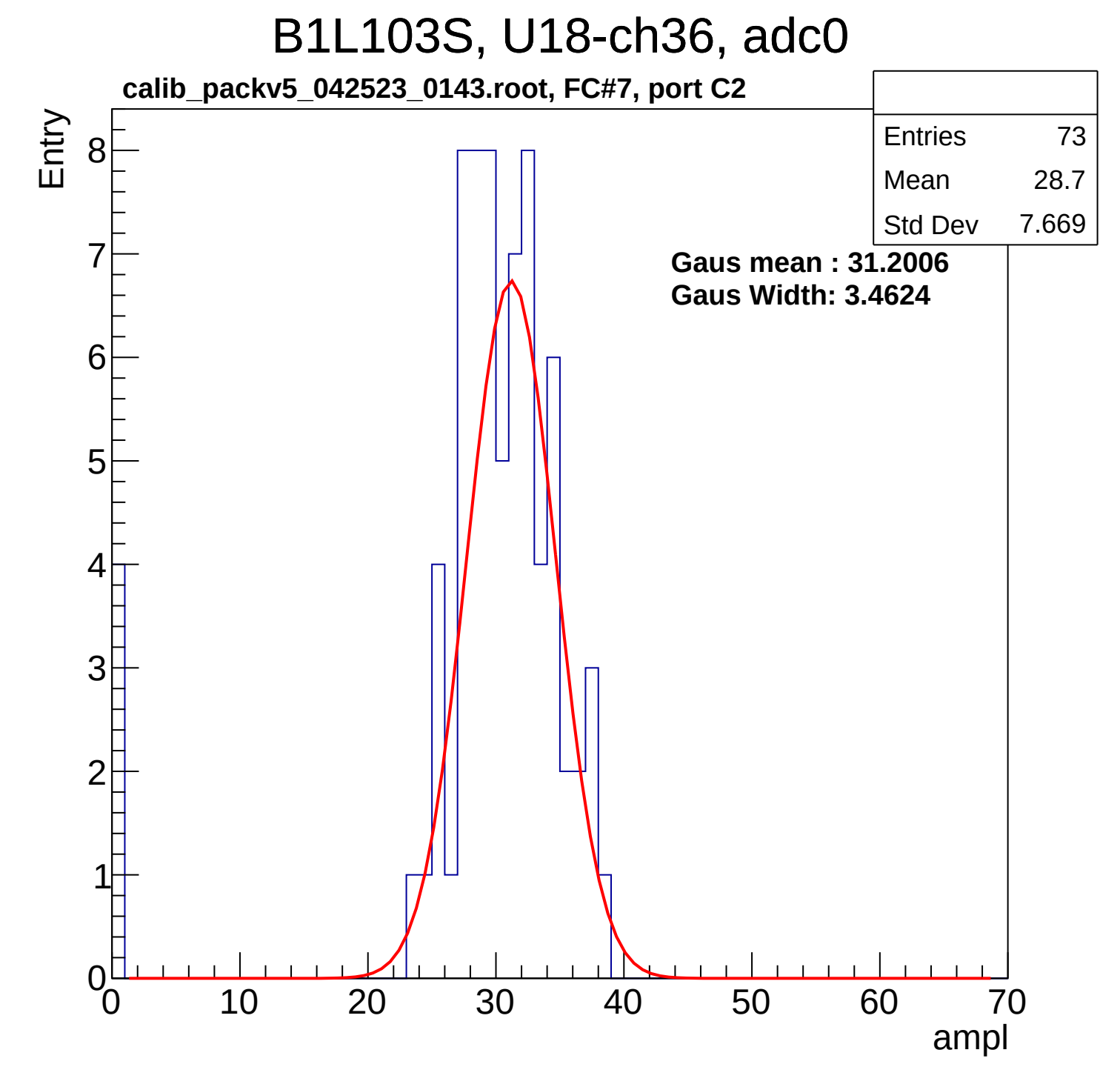

B1L103S, U18-ch35, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 4
Mean 47
Std Dev 27.14
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U18-ch35, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch36, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 73
Mean 28.7
Std Dev 7.669
Gaus mean : 31.2006
Gaus Width: 3.4624
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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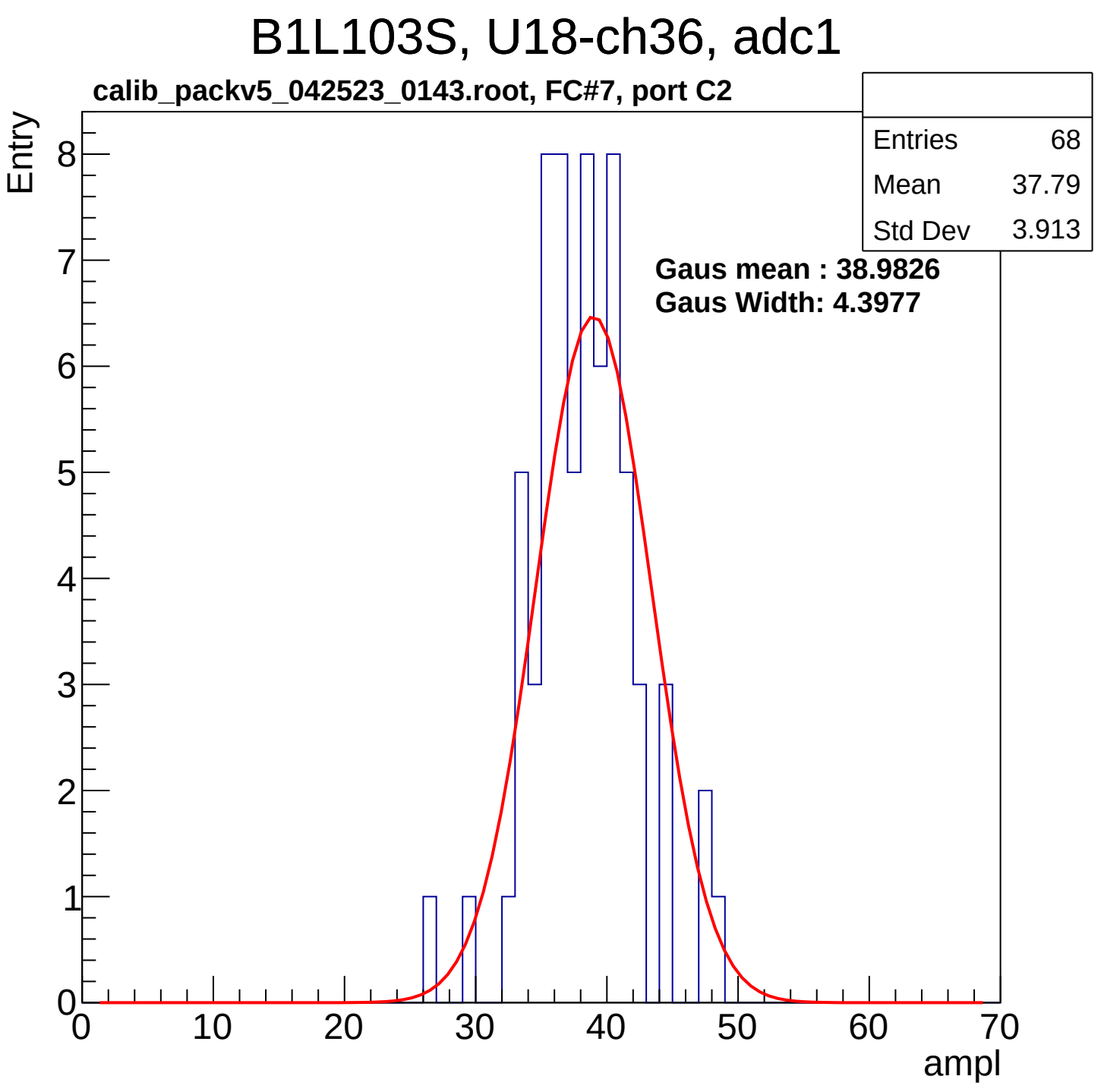
40
50
60
70


B1L103S, U18-ch36, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 37.79
Std Dev 3.913
Gaus mean : 38.9826
Gaus Width: 4.3977
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
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60
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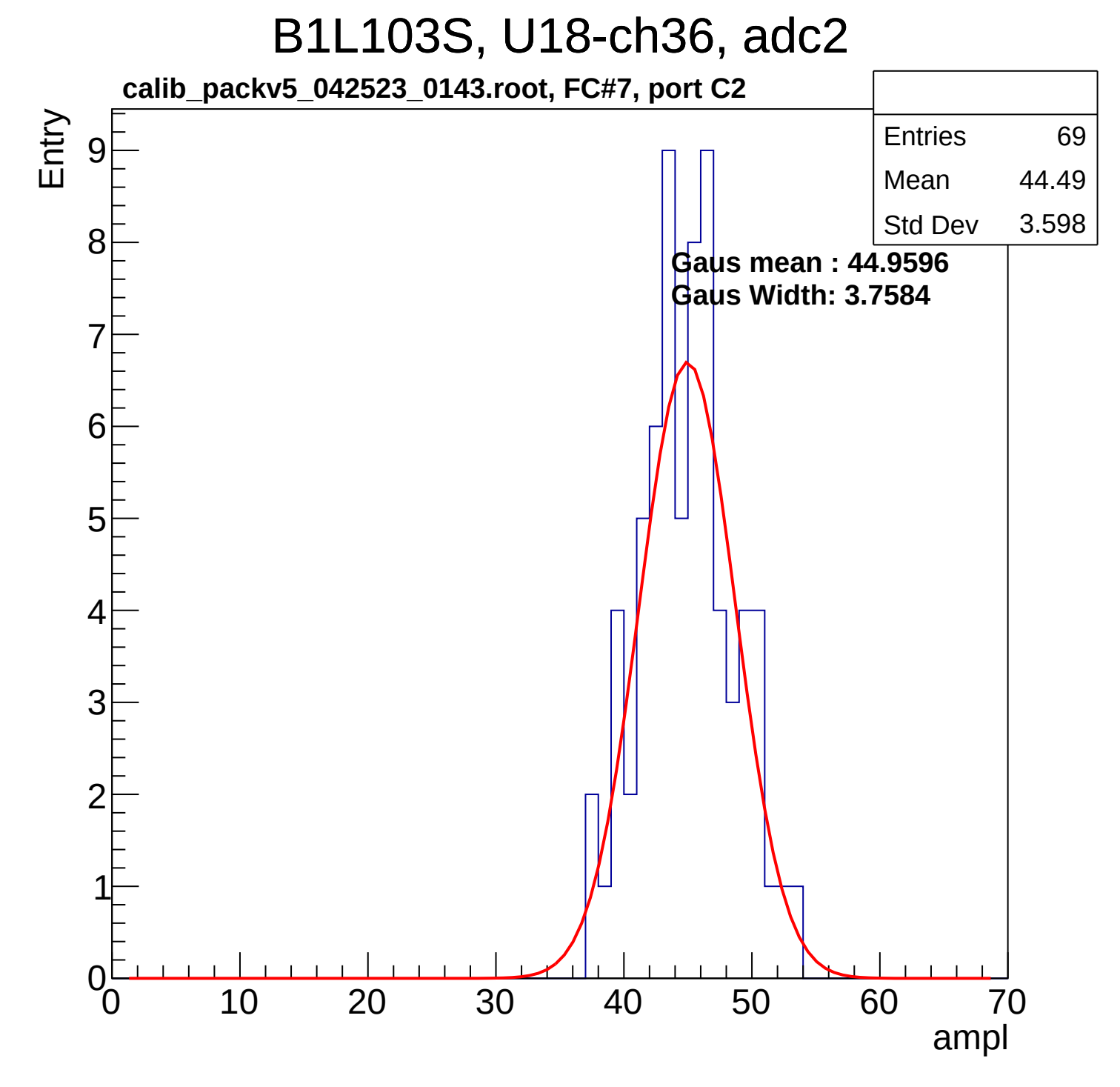
B1L103S, U18-ch36, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 44.49
Std Dev 3.598
Gaus mean : 44.9596
Gaus Width: 3.7584
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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20
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40
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60
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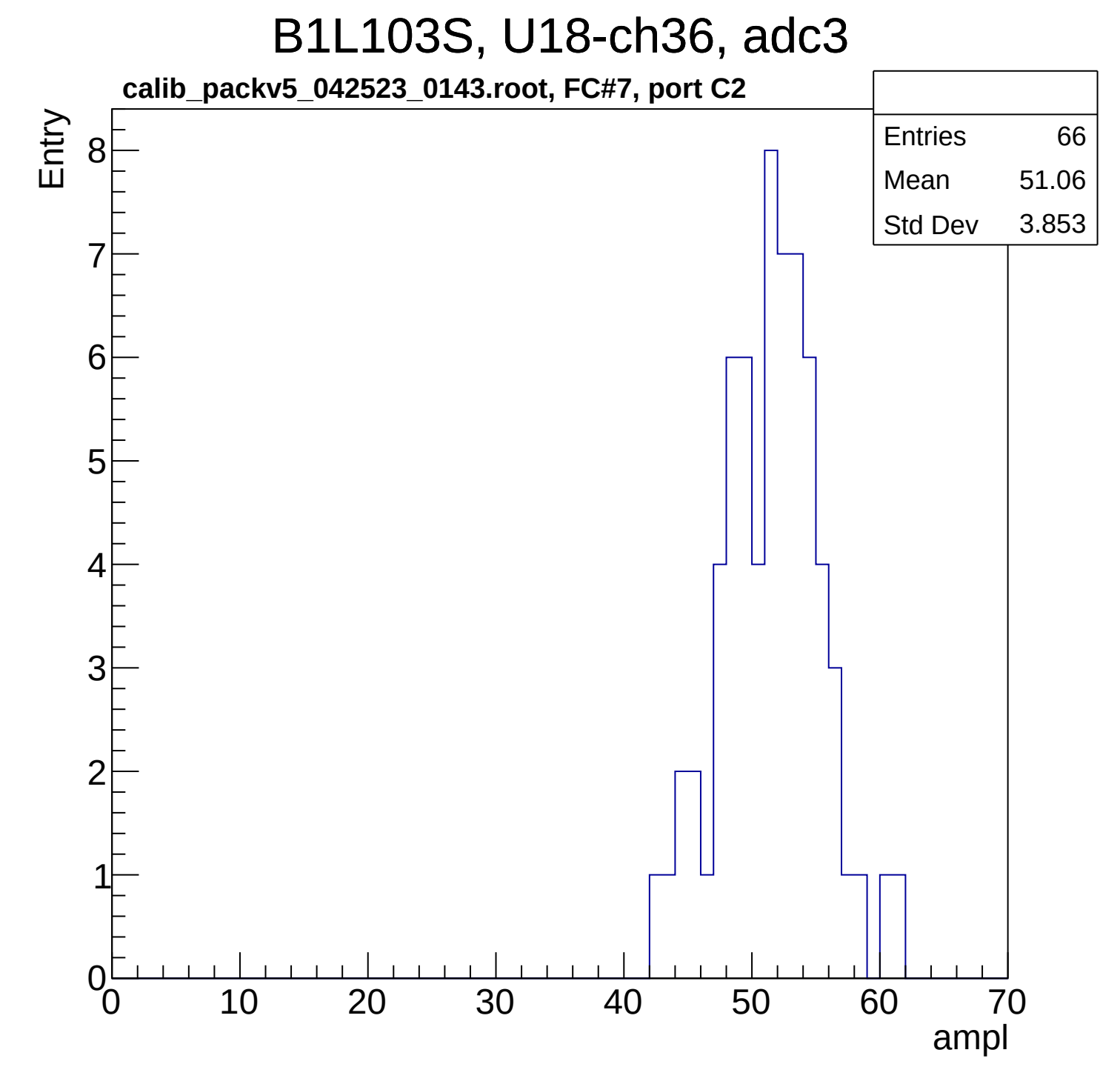
B1L103S, U18-ch36, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 51.06
Std Dev 3.853
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
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60
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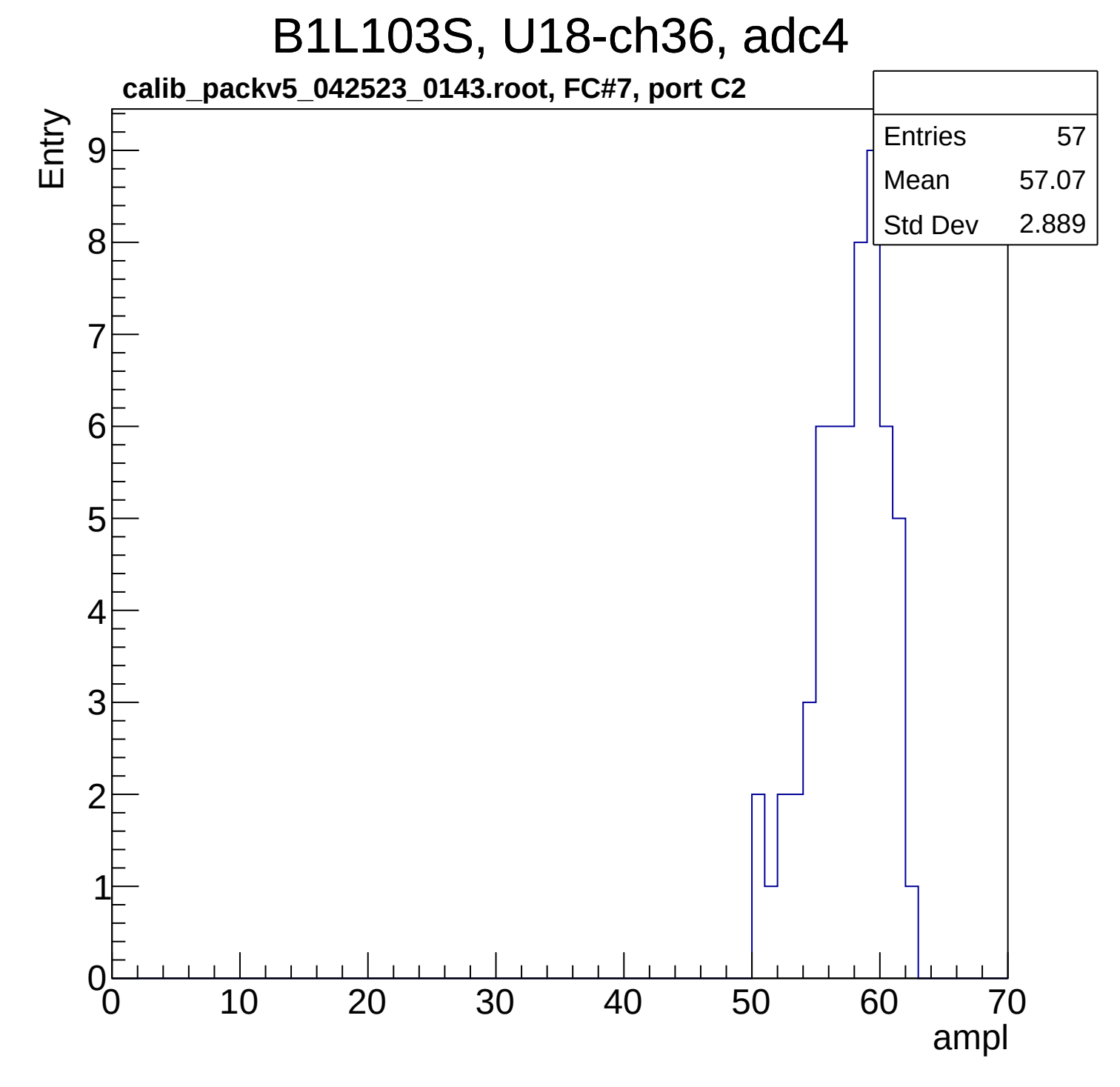
B1L103S, U18-ch36, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 57.07
Std Dev 2.889
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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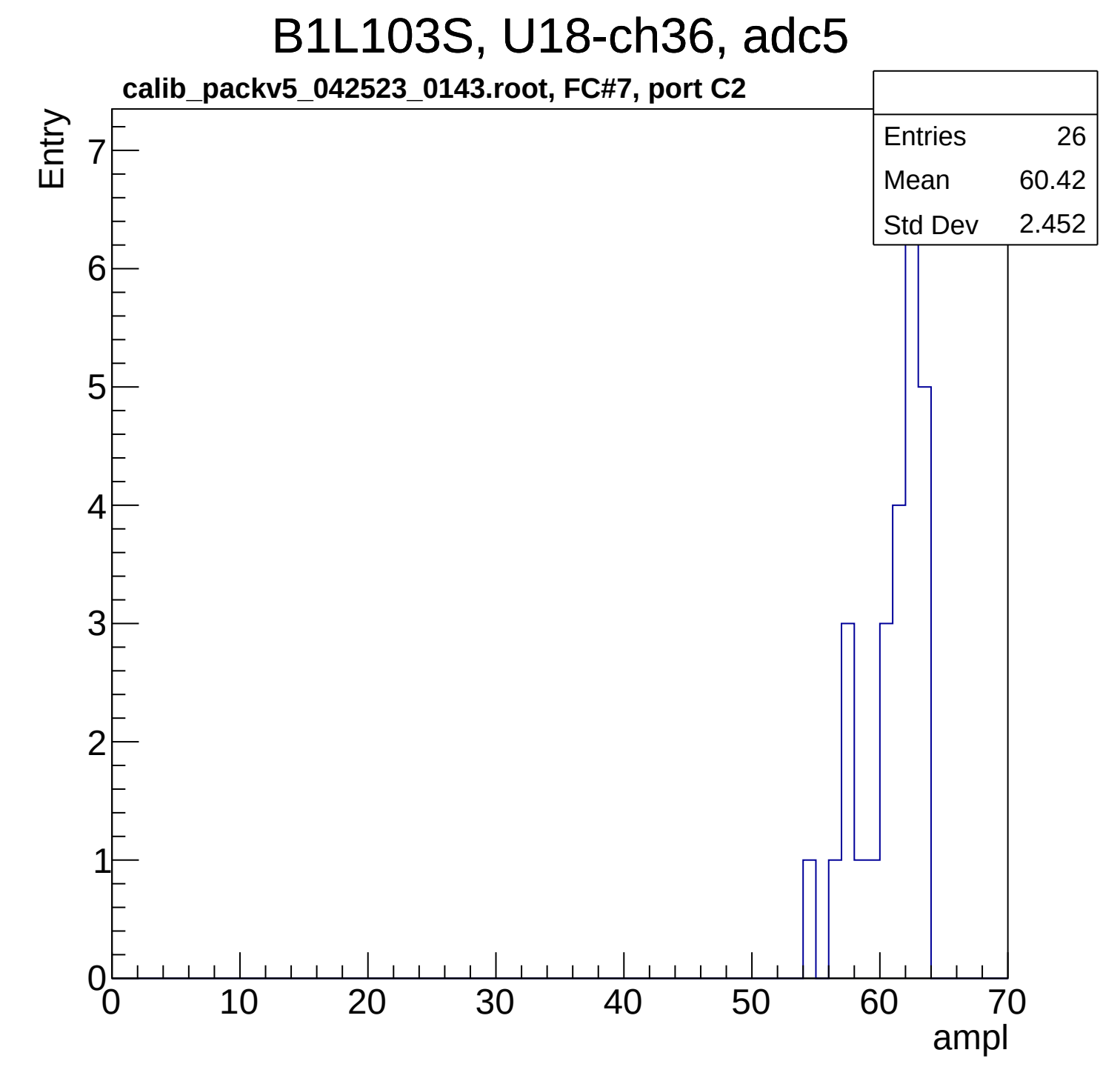
B1L103S, U18-ch36, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 26
Mean 60.42
Std Dev 2.452
Entry
ampl
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6
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0
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20
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60
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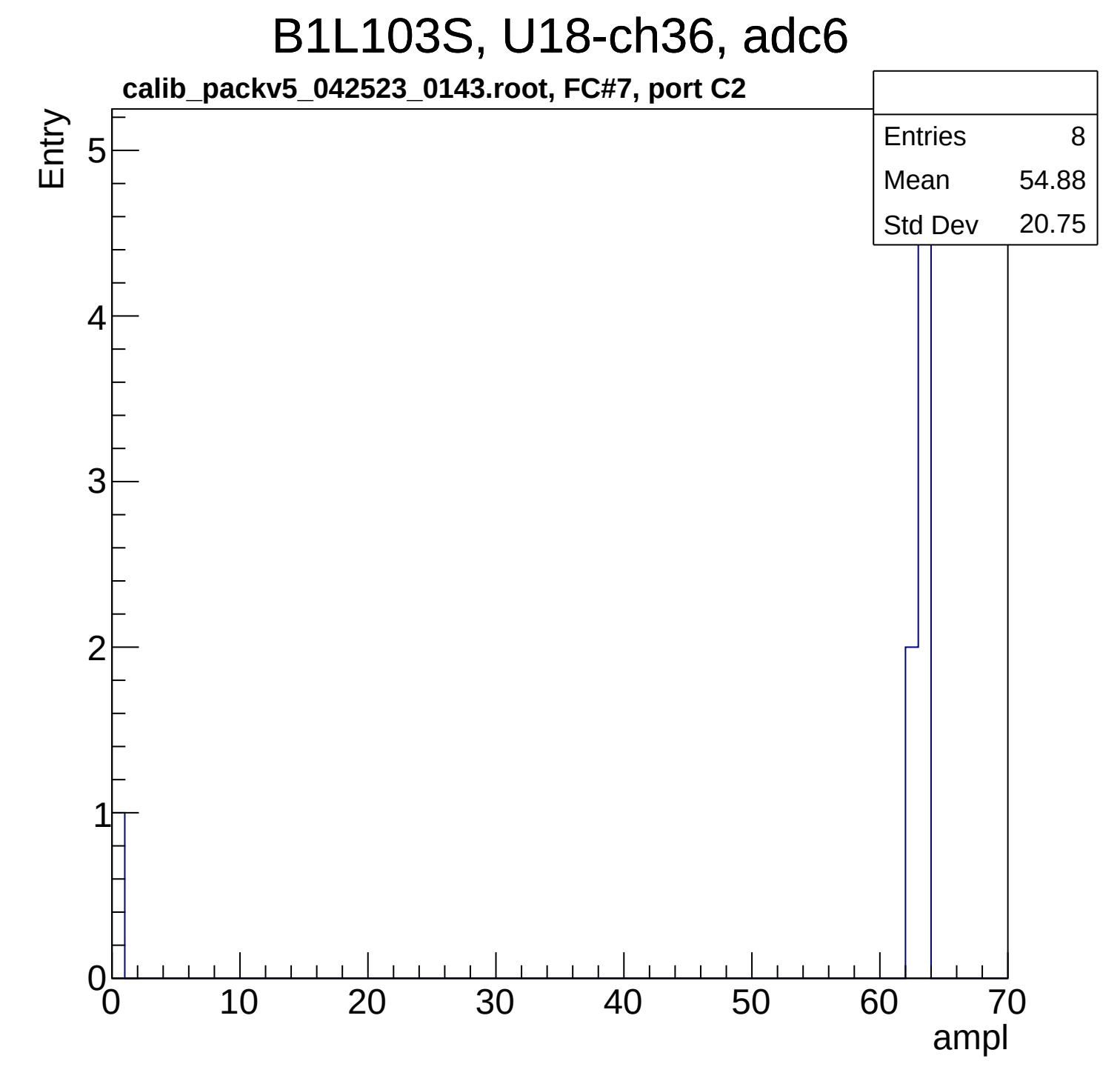
B1L103S, U18-ch36, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 8
Mean 54.88
Std Dev 20.75
Entry
0
1
2
3
4
5
0
10
20
30
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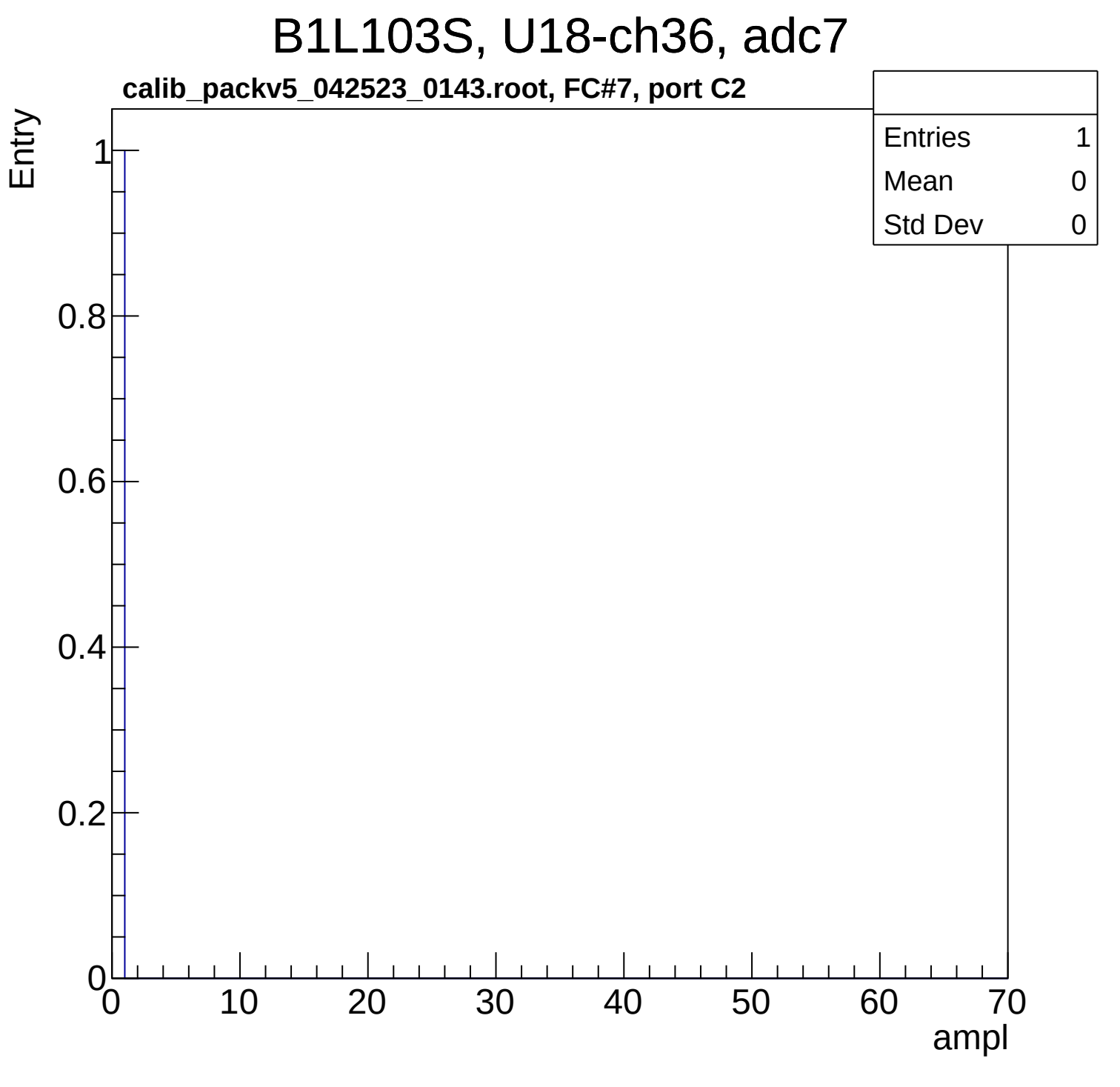
50
60
70
ampl


B1L103S, U18-ch36, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
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0.6
0.4
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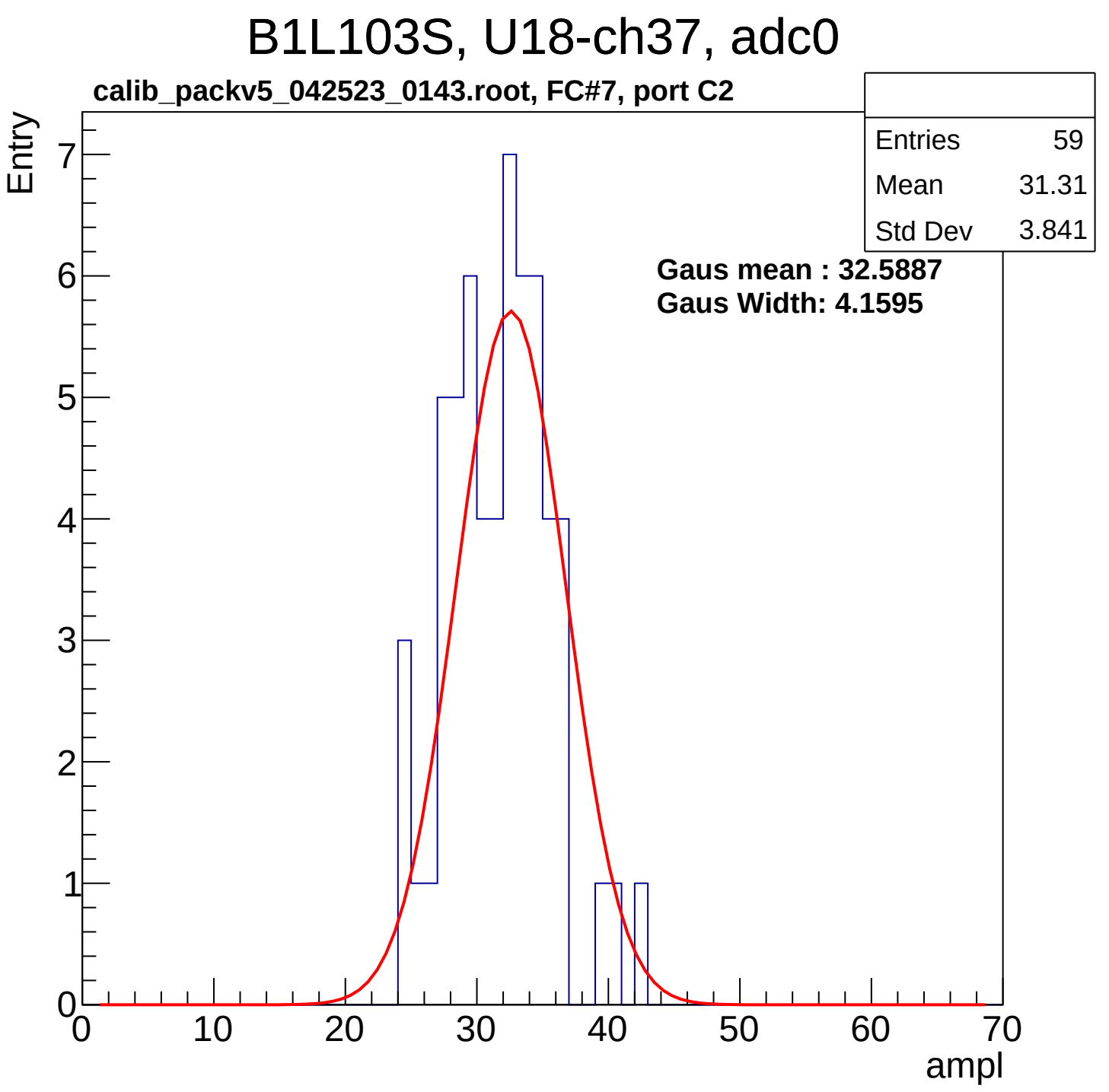
50
60
70
ampl


B1L103S, U18-ch37, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 31.31
Std Dev 3.841
Gaus mean : 32.5887
Gaus Width: 4.1595
Entry
ampl
0
1
2
3
4
5
6
7
0
10
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40
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60
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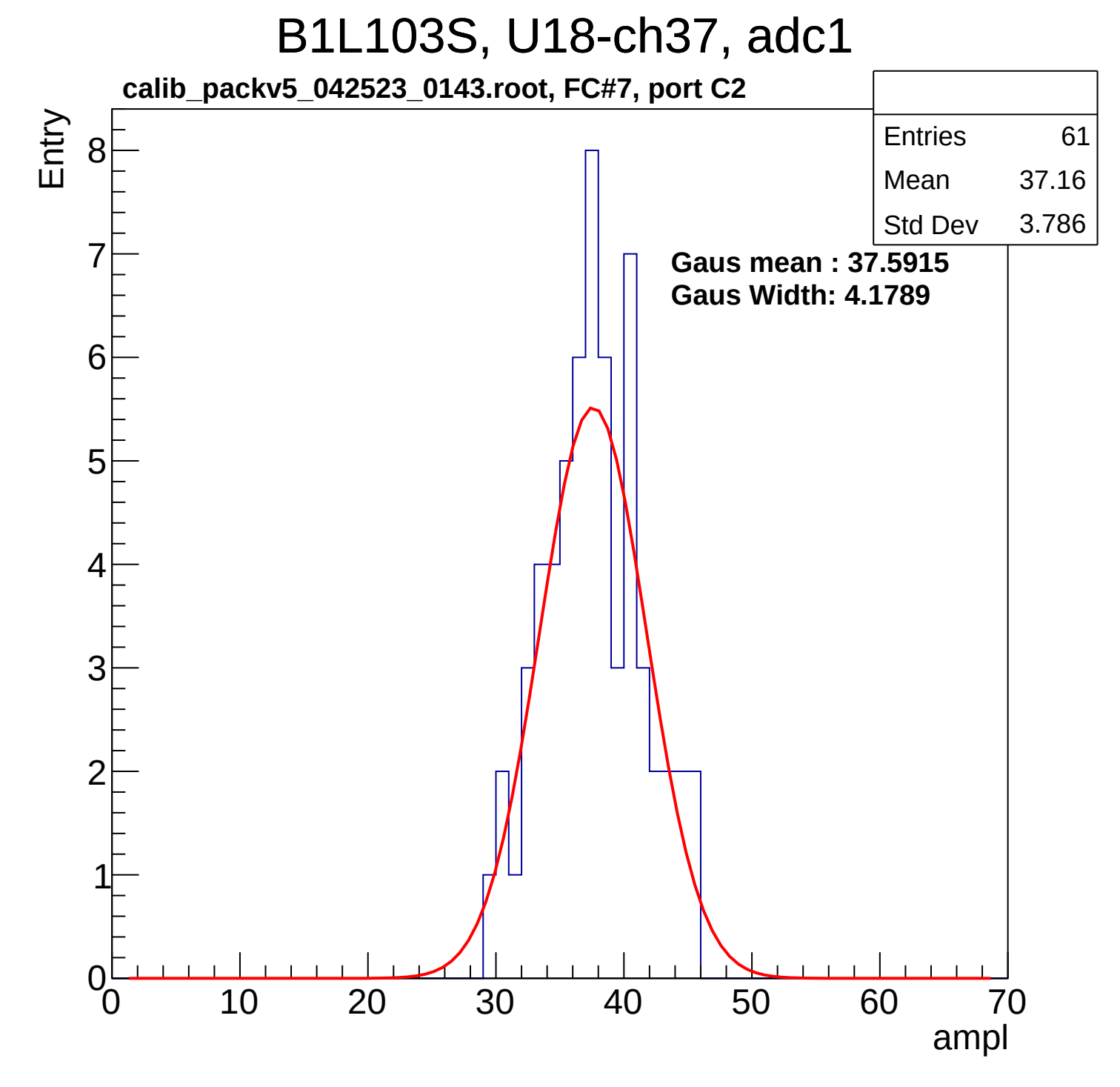
B1L103S, U18-ch37, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 61
Mean 37.16
Std Dev 3.786
Gaus mean : 37.5915
Gaus Width: 4.1789
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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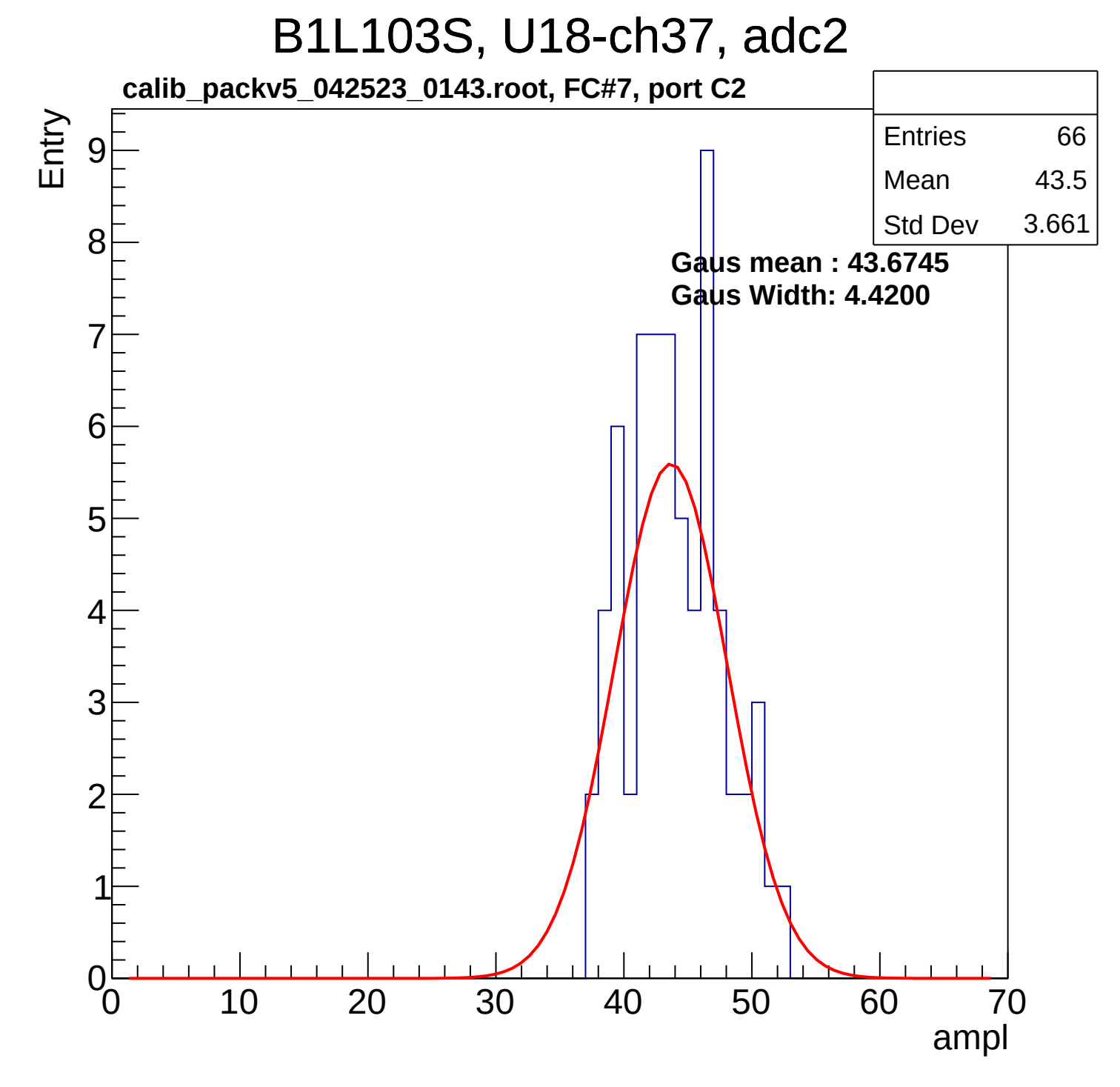
B1L103S, U18-ch37, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 43.5
Std Dev 3.661
Gaus mean : 43.6745
Gaus Width: 4.4200
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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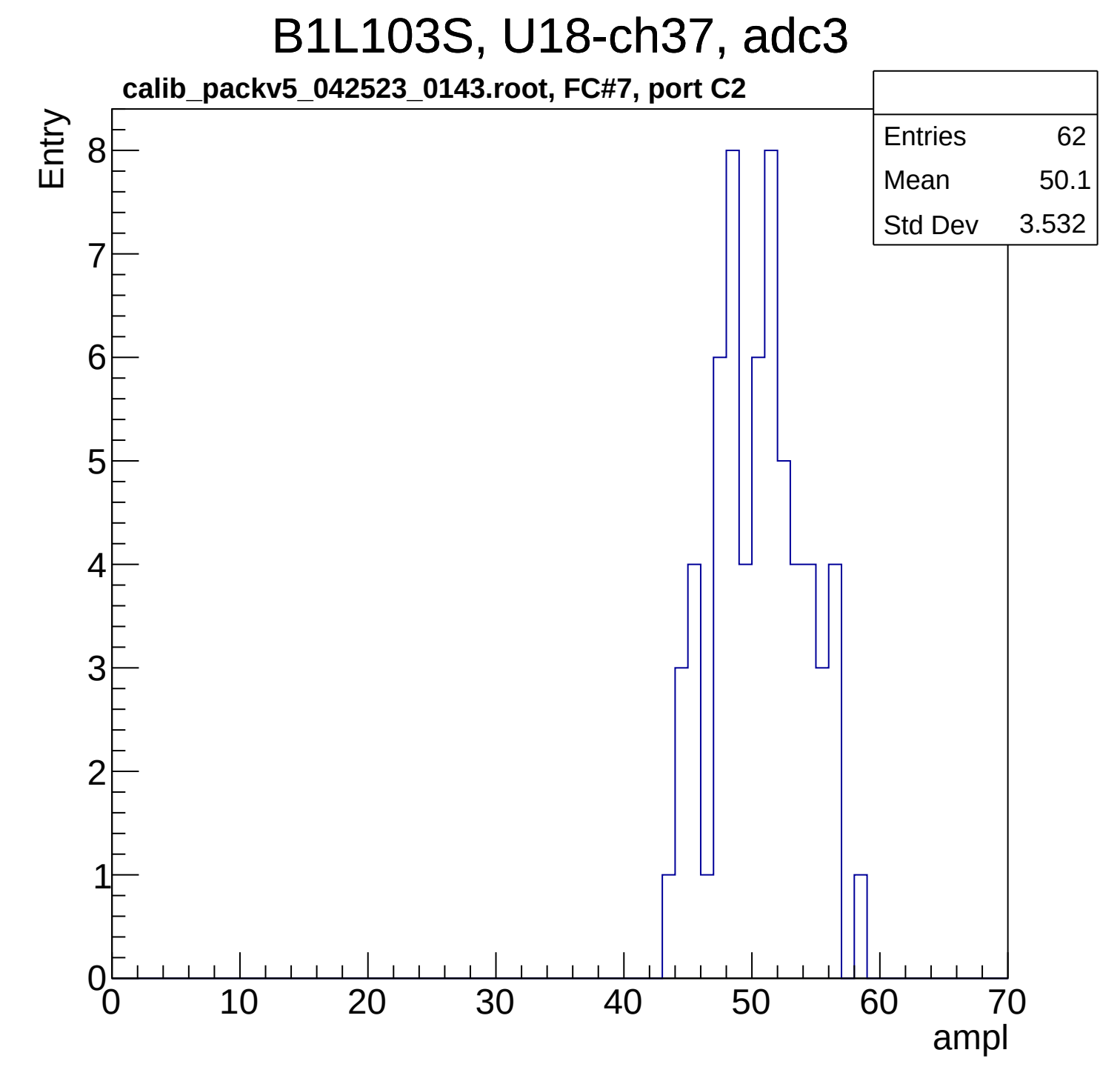
B1L103S, U18-ch37, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 62
Mean 50.1
Std Dev 3.532
Entry
ampl
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5
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7
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0
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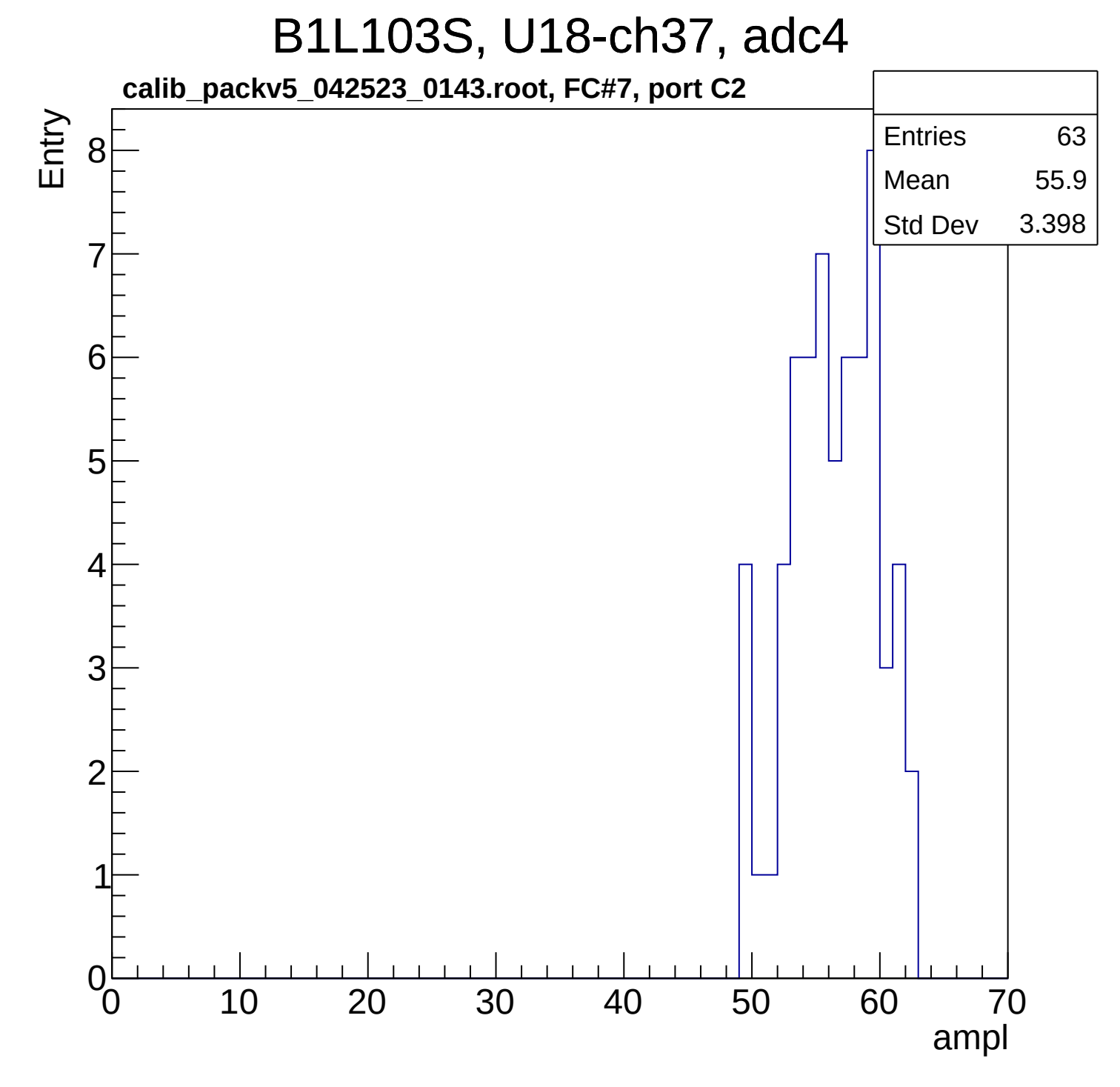
B1L103S, U18-ch37, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 55.9
Std Dev 3.398
Entry
ampl
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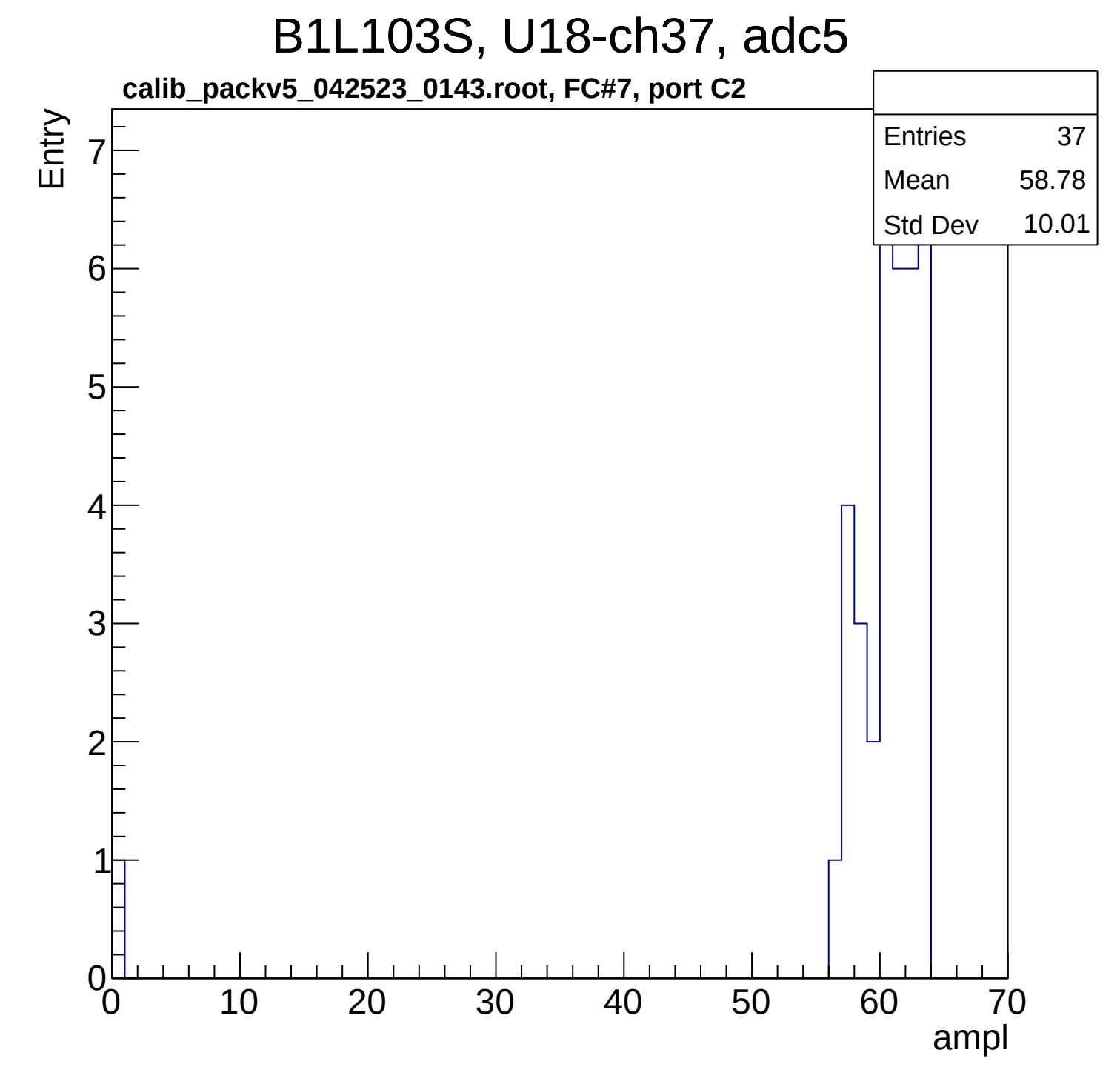
B1L103S, U18-ch37, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 37
Mean 58.78
Std Dev 10.01
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
50
60
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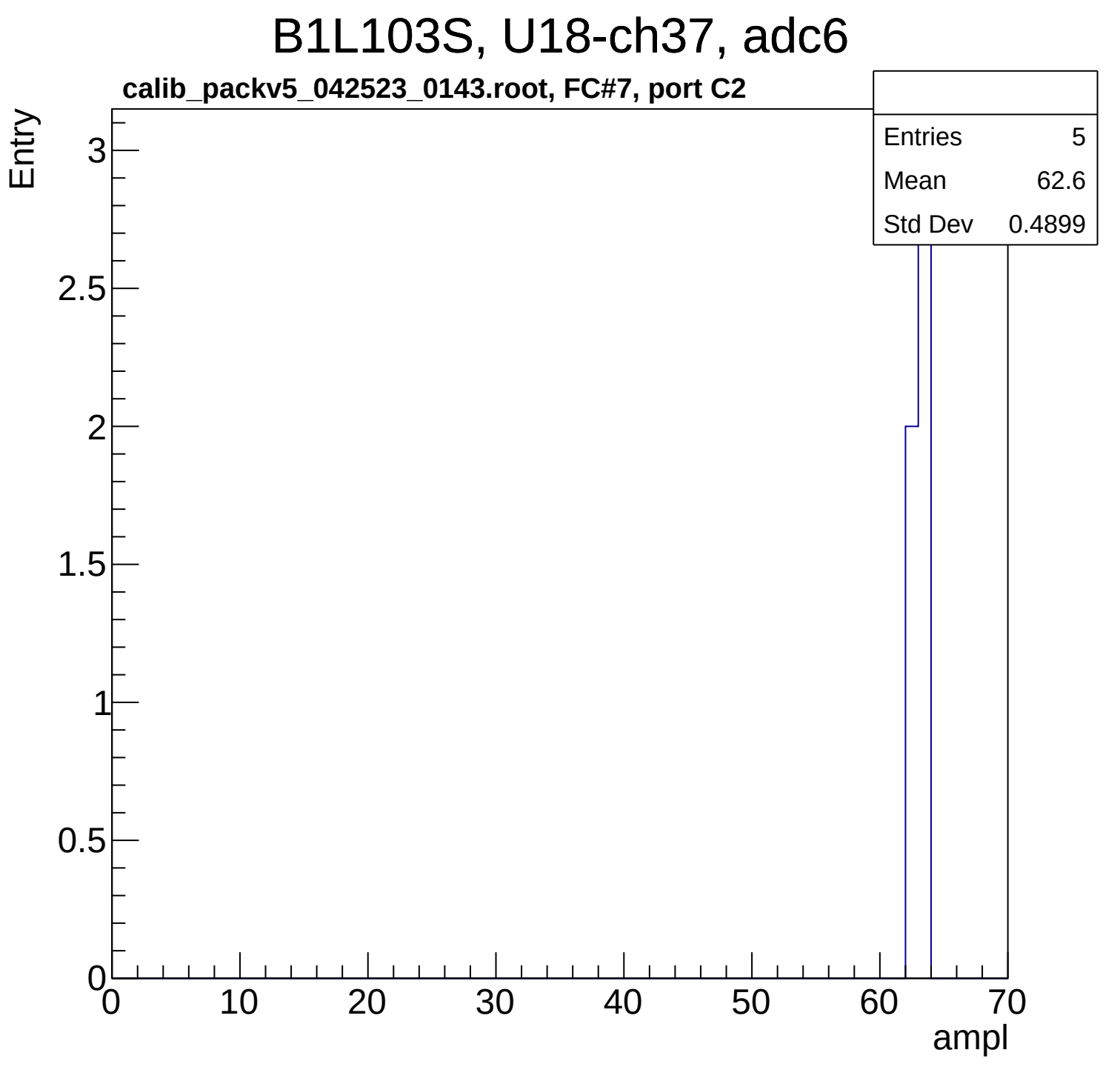
B1L103S, U18-ch37, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 5
Mean 62.6
Std Dev 0.4899
Entry
ampl
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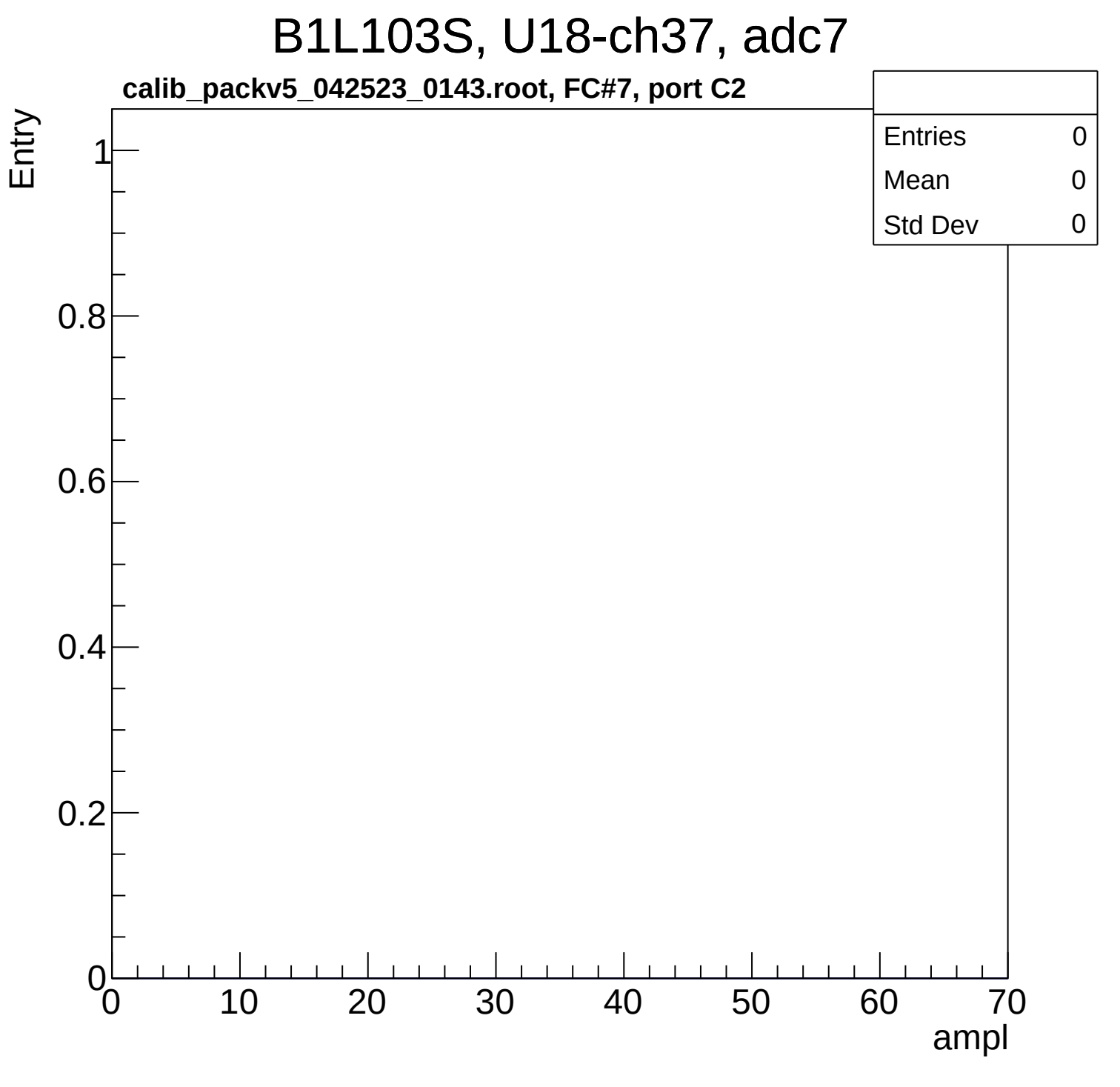
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U18-ch37, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
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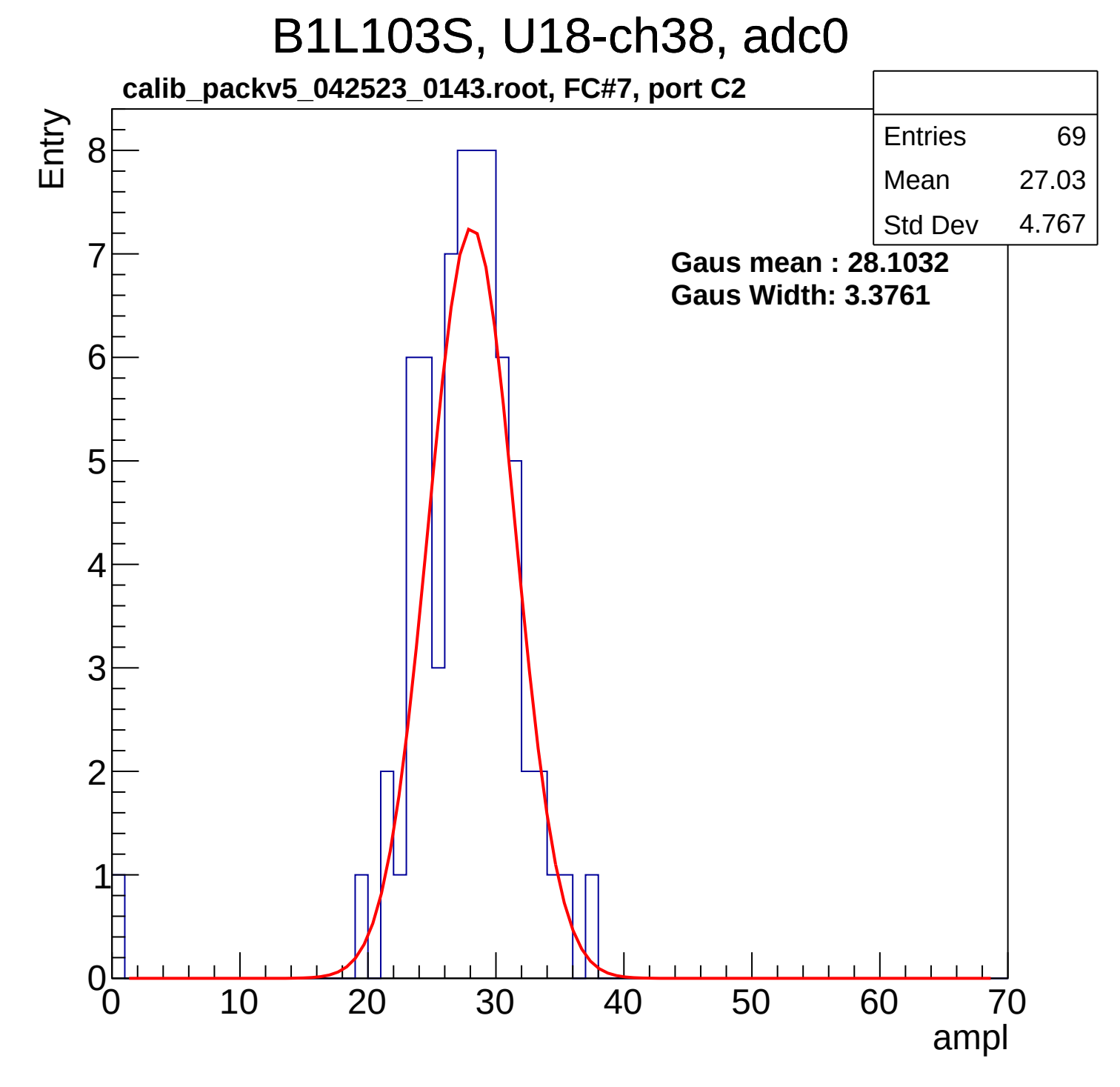
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch38, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 27.03
Std Dev 4.767
Gaus mean : 28.1032
Gaus Width: 3.3761
Entry
ampl
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1
2
3
4
5
6
7
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0
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20
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40
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60
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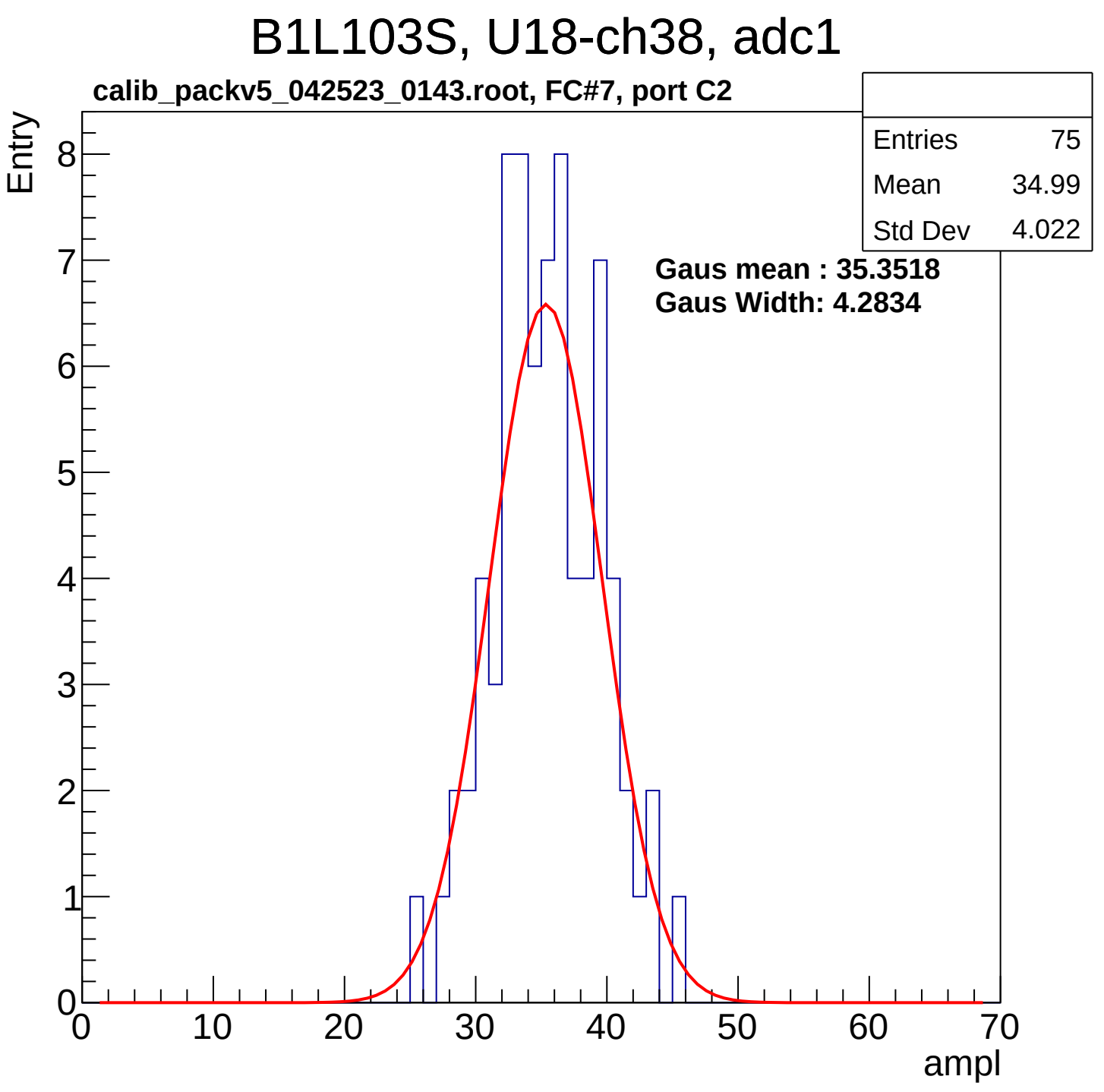
B1L103S, U18-ch38, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 75
Mean 34.99
Std Dev 4.022
Gaus mean : 35.3518
Gaus Width: 4.2834
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
50
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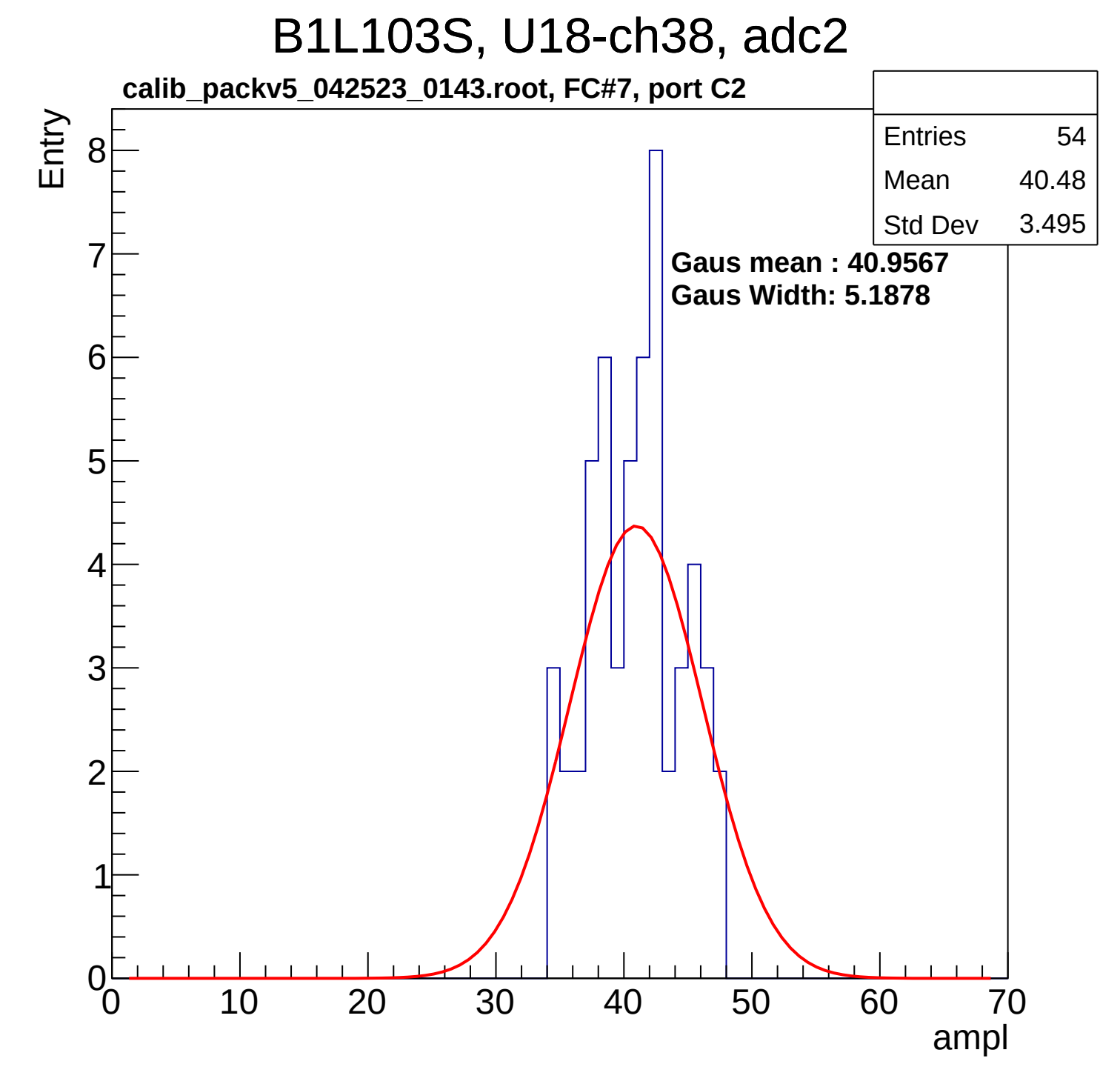
B1L103S, U18-ch38, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 54
Mean 40.48
Std Dev 3.495
Gaus mean : 40.9567
Gaus Width: 5.1878
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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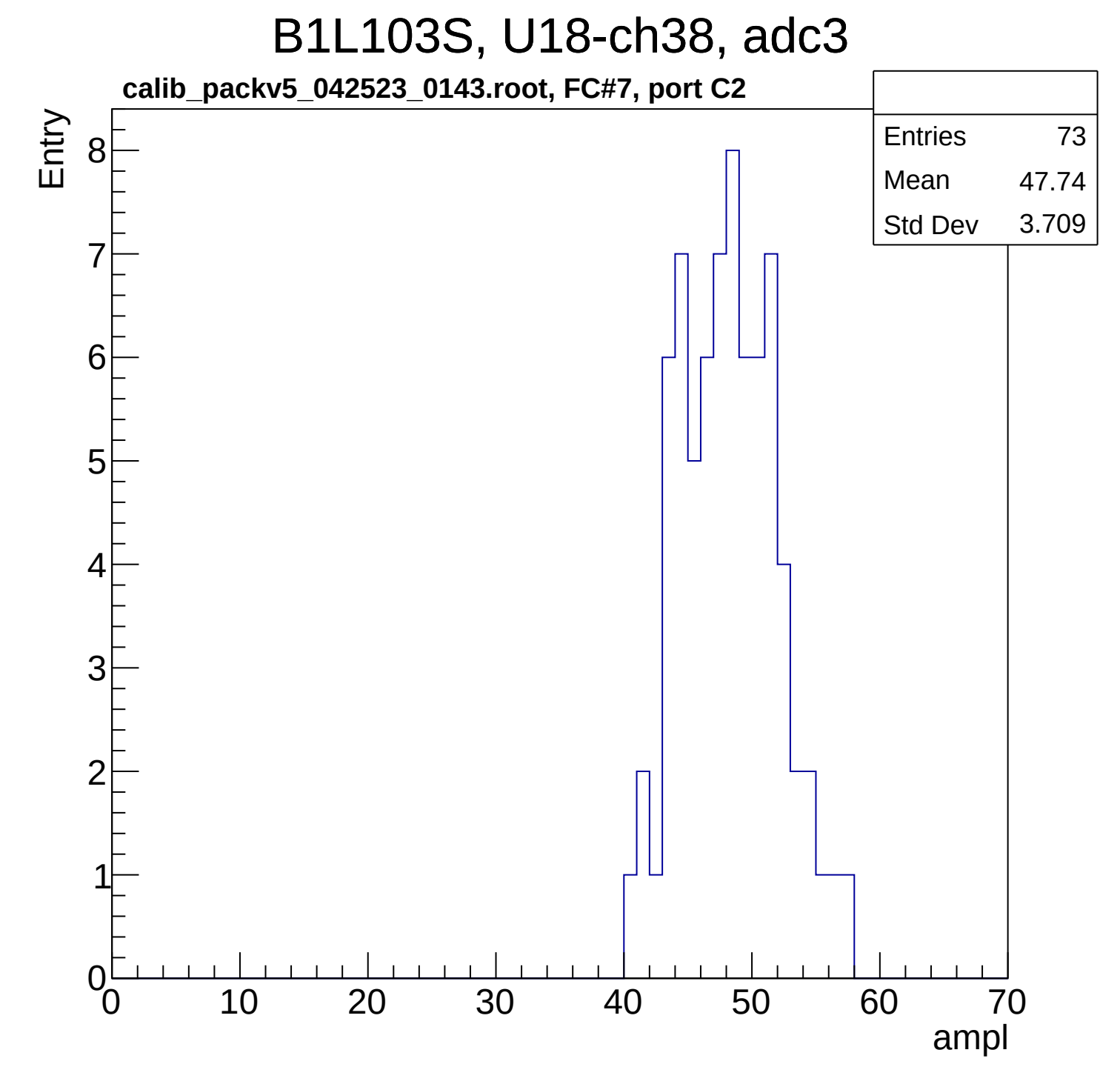
B1L103S, U18-ch38, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 73
Mean 47.74
Std Dev 3.709
Entry
ampl
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3
4
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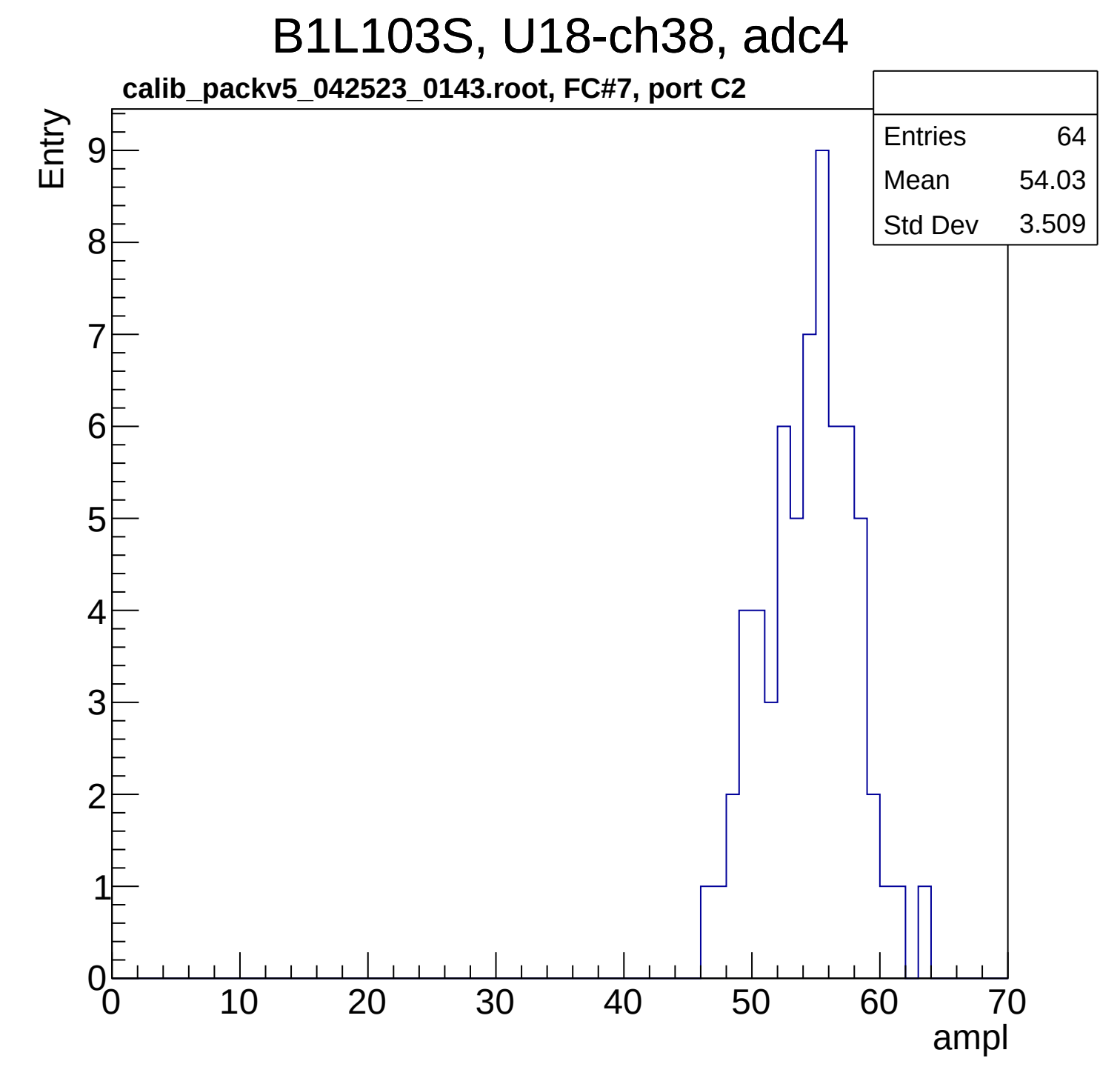
B1L103S, U18-ch38, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 54.03
Std Dev 3.509
Entry
ampl
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2
3
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6
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0
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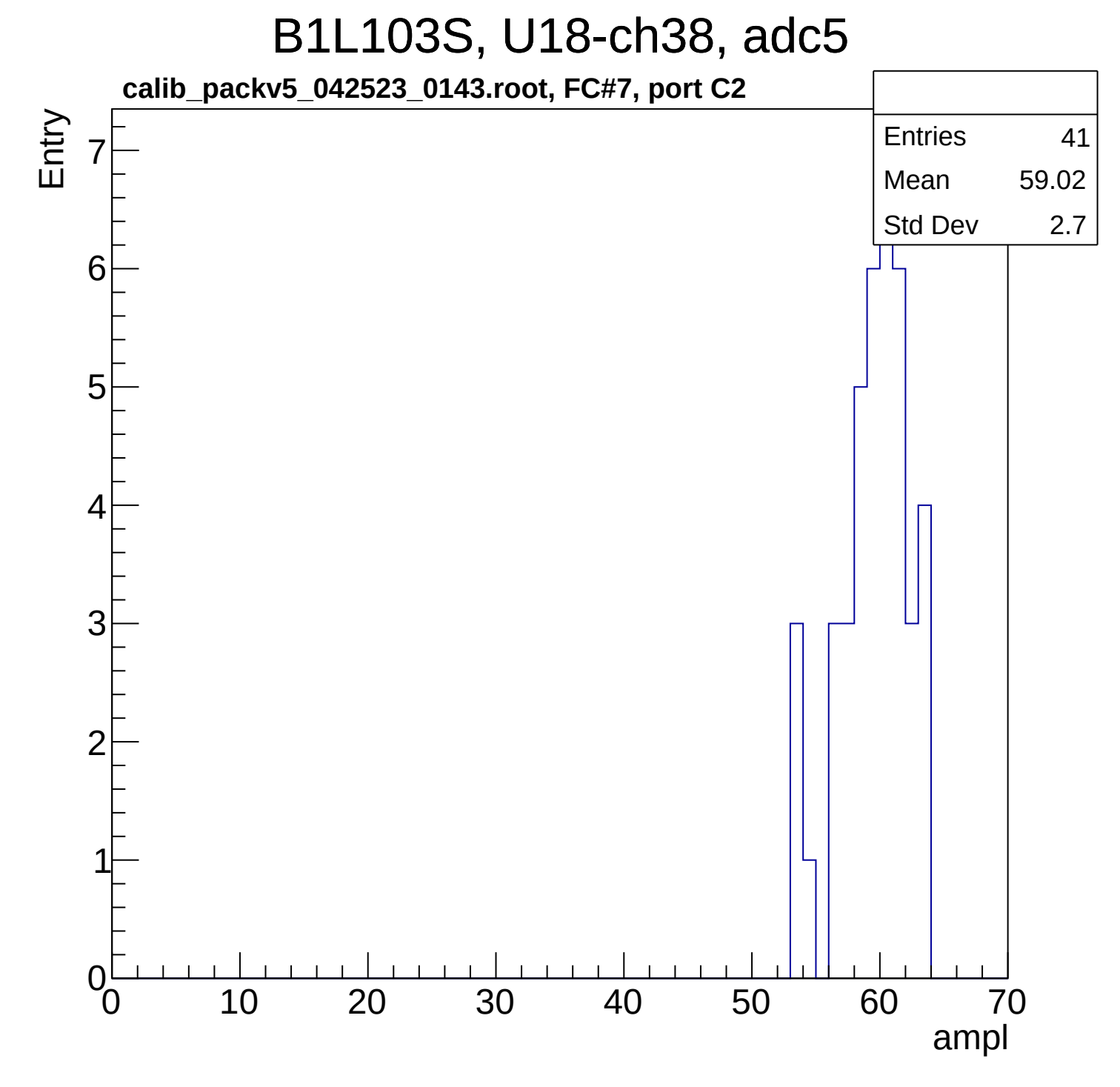
B1L103S, U18-ch38, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 41
Mean 59.02
Std Dev 2.7
Entry
ampl
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1
2
3
4
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6
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0
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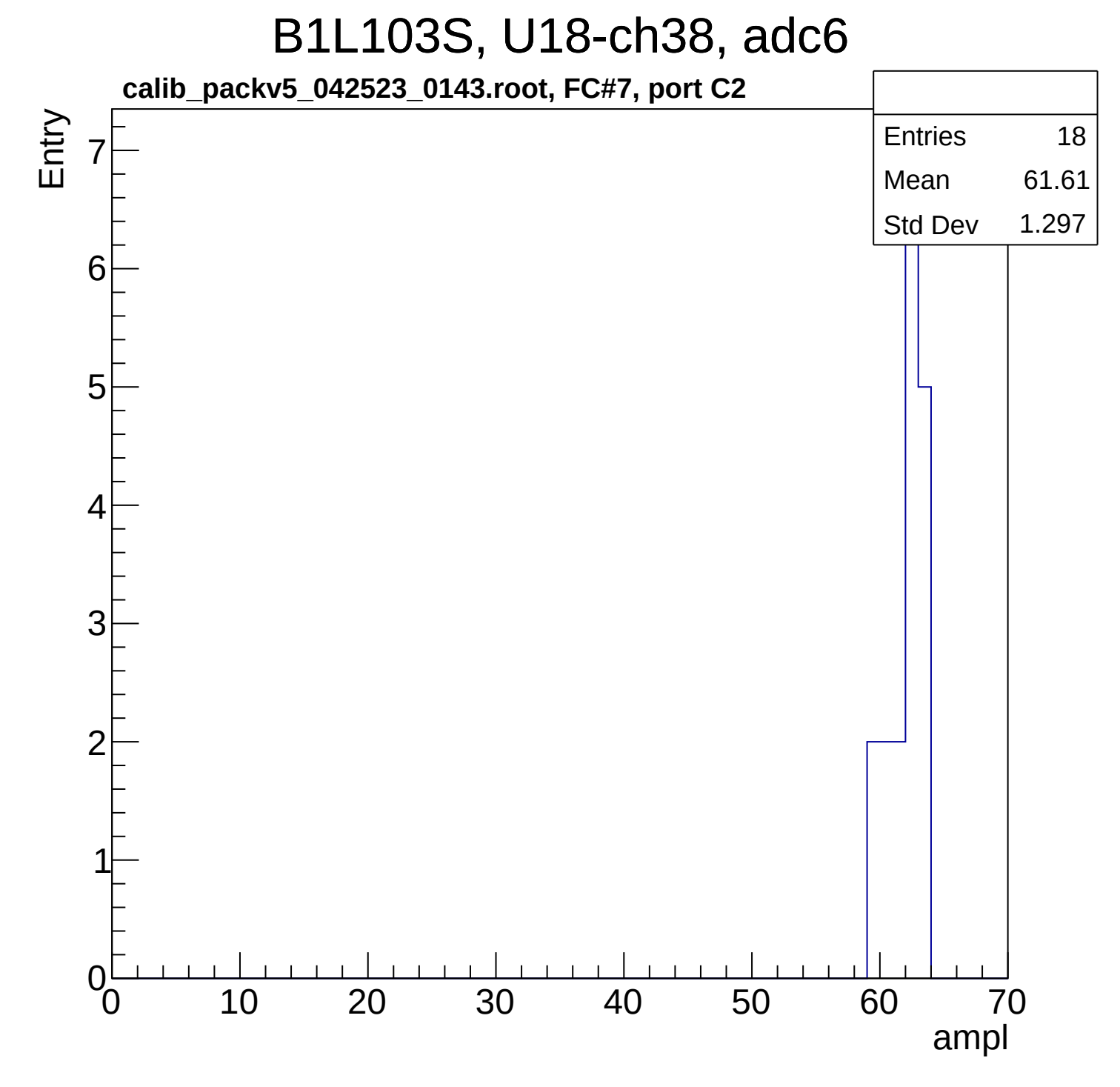
B1L103S, U18-ch38, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 18
Mean 61.61
Std Dev 1.297
Entry
ampl
0
1
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3
4
5
6
7
0
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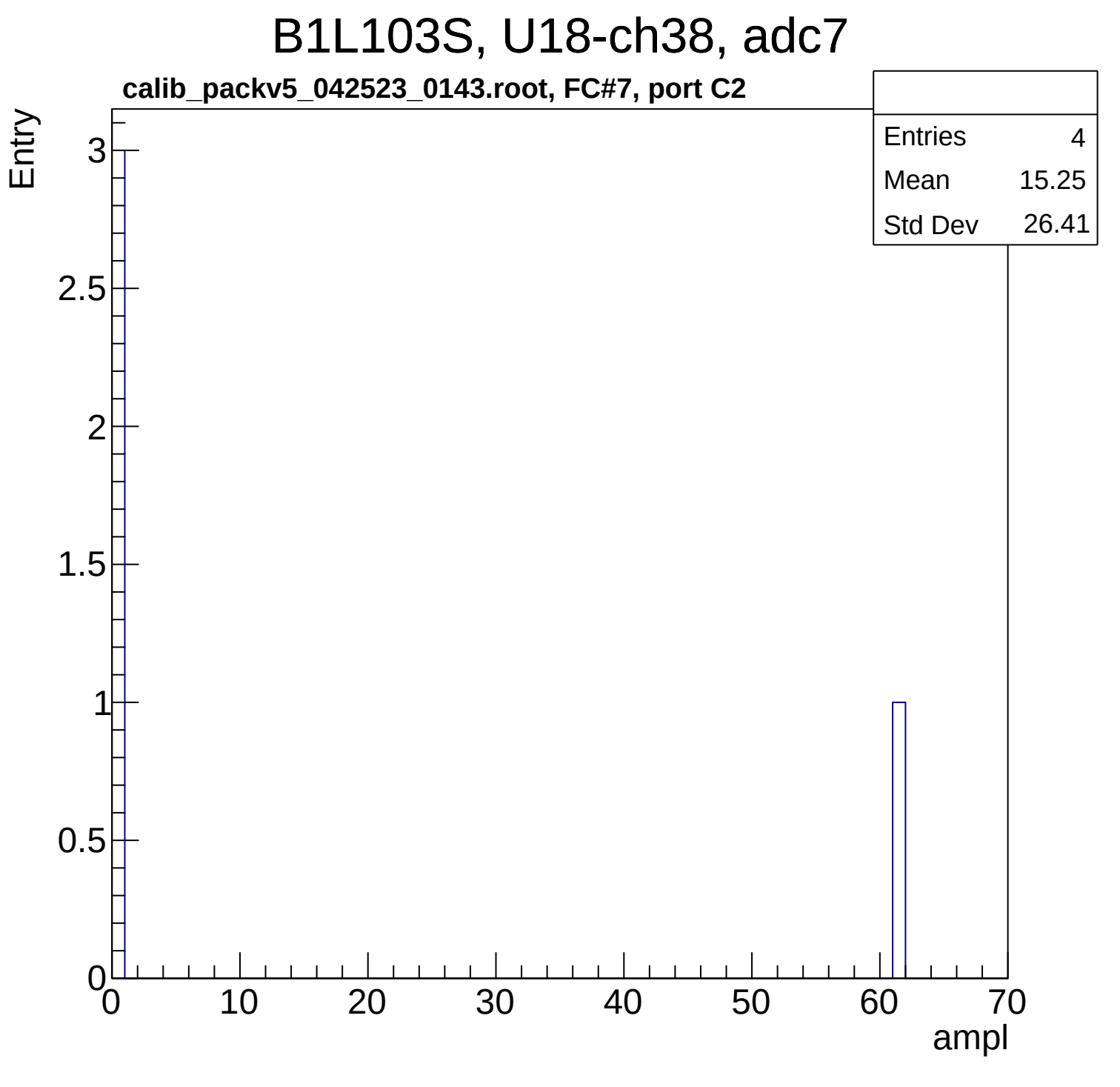
B1L103S, U18-ch38, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 4
Mean 15.25
Std Dev 26.41
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
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40
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60
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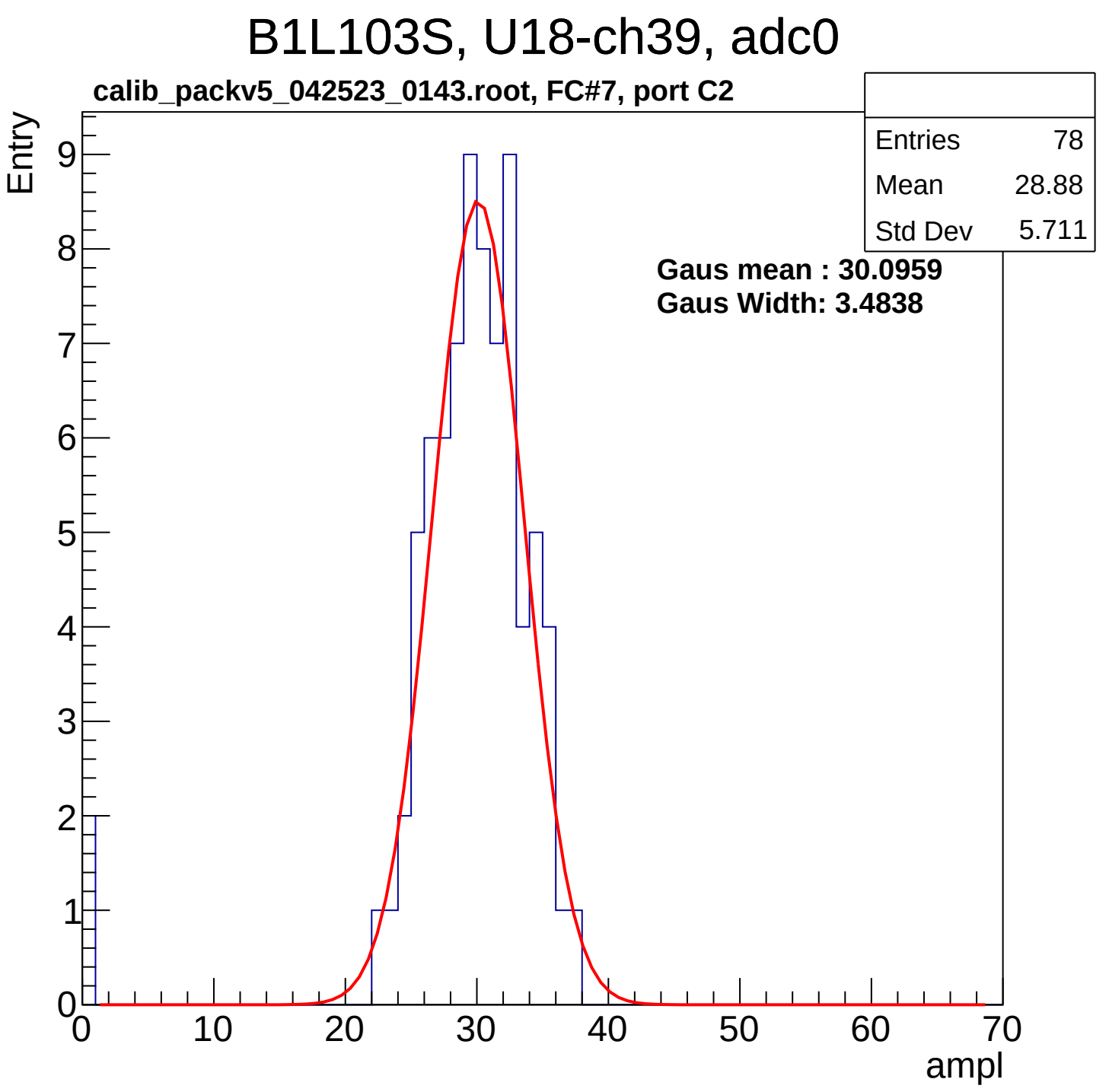
B1L103S, U18-ch39, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 78
Mean 28.88
Std Dev 5.711
Gaus mean : 30.0959
Gaus Width: 3.4838
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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40
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60
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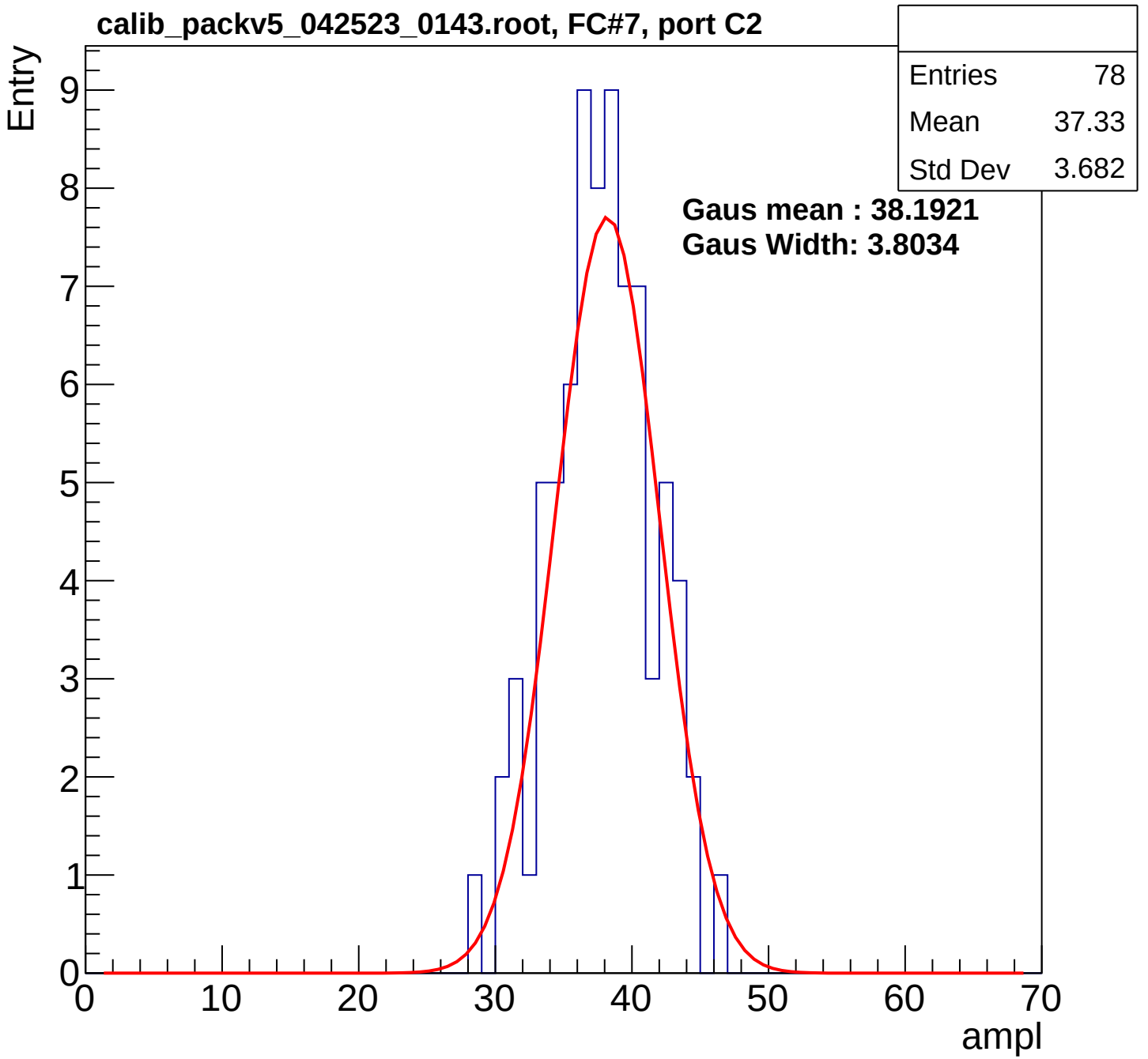
B1L103S, U18-ch39, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 78
Mean 37.33
Std Dev 3.682
Gaus mean : 38.1921
Gaus Width: 3.8034
Entry
ampl
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2
3
4
5
6
7
8
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0
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60
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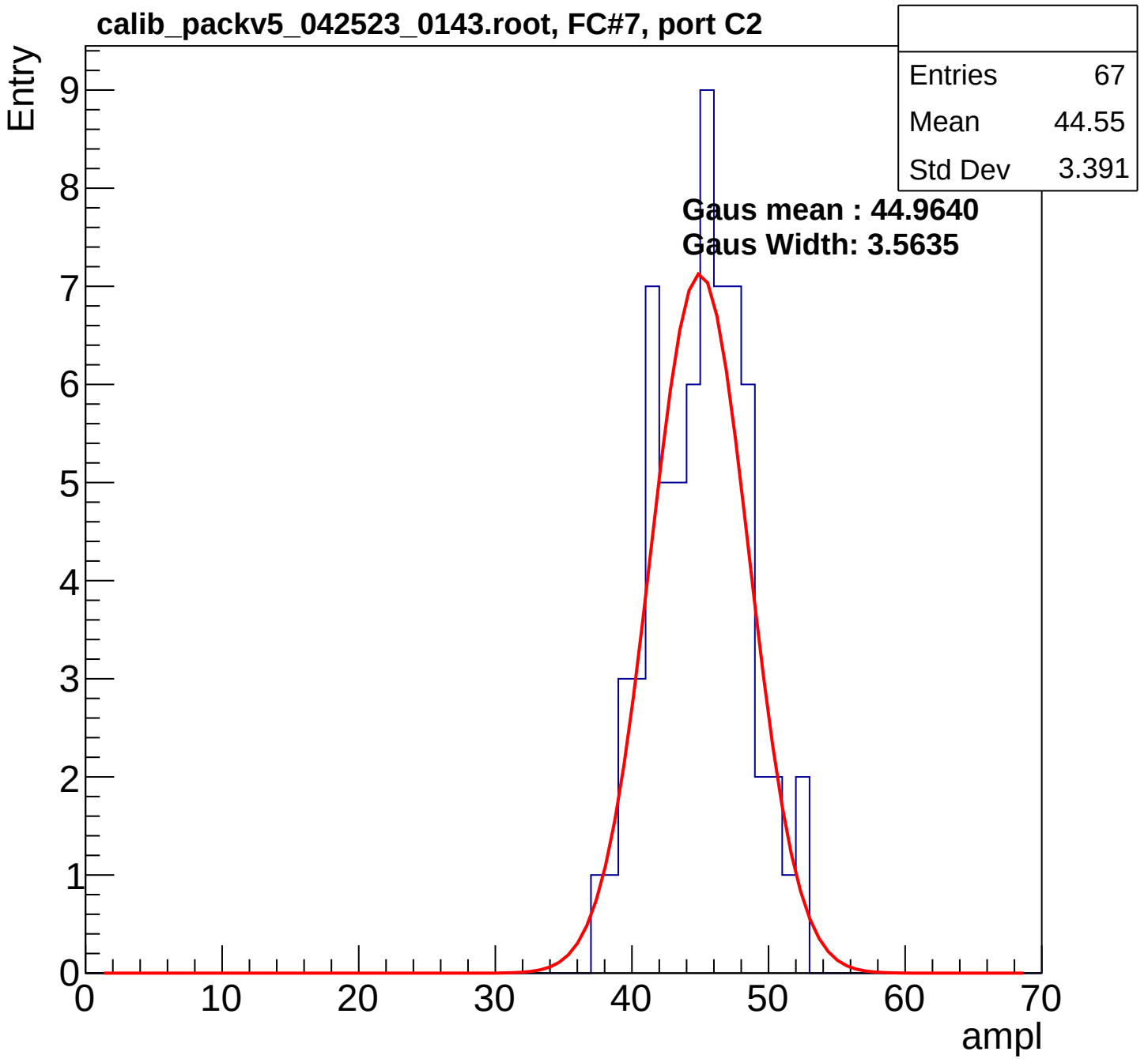
B1L103S, U18-ch39, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 44.55
Std Dev 3.391
Gaus mean : 44.9640
Gaus Width: 3.5635
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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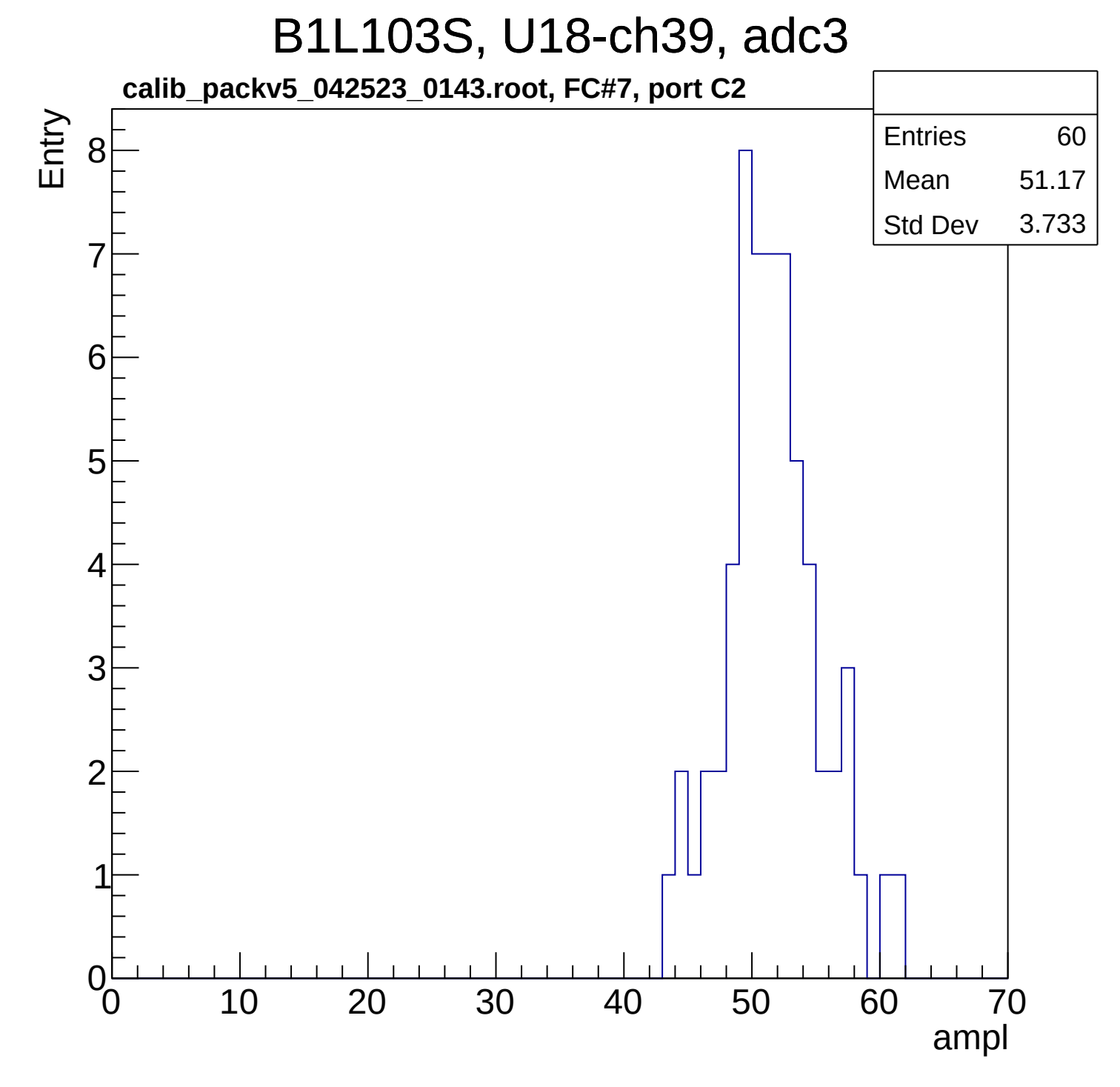
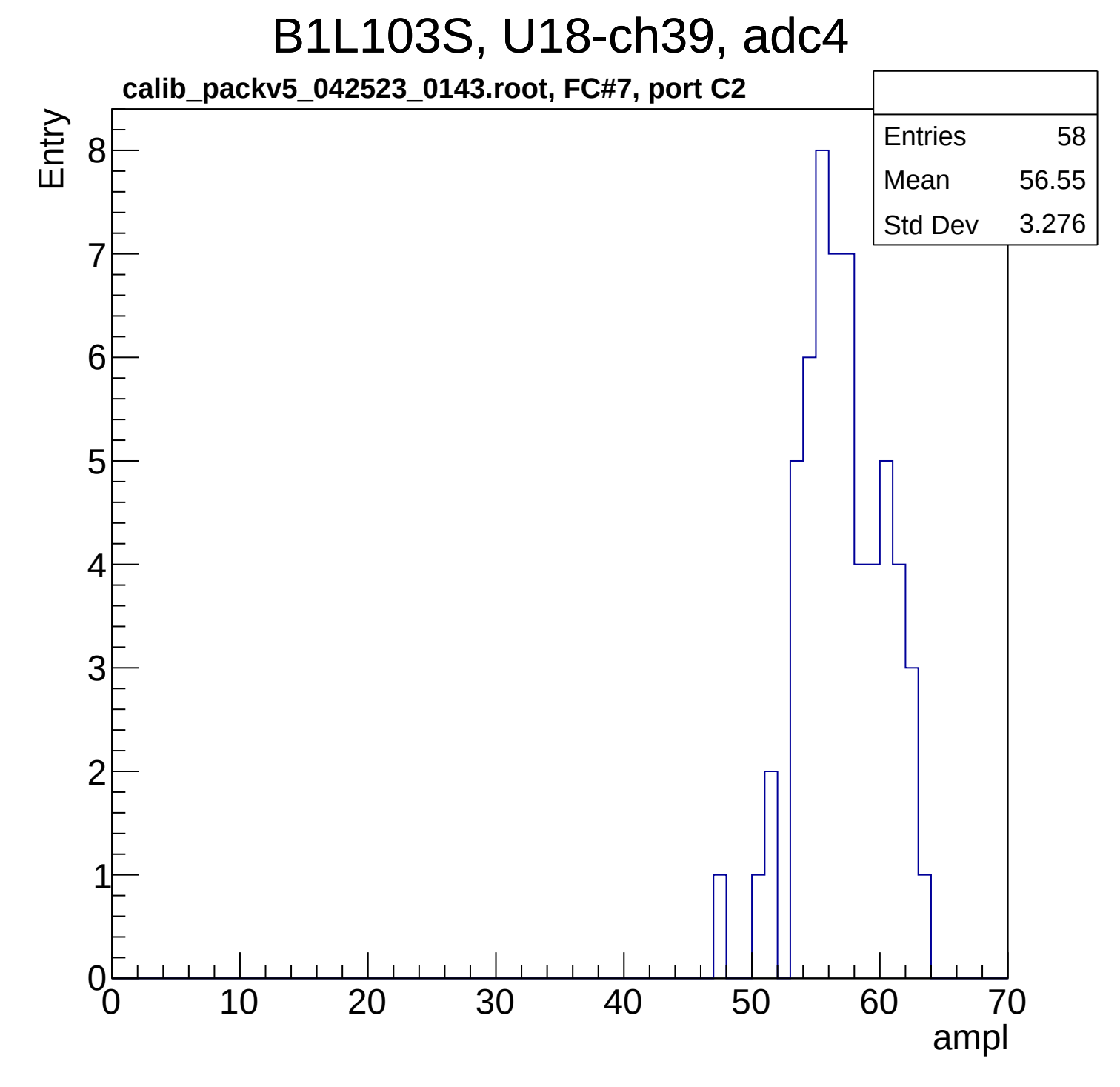

B1L103S, U18-ch39, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 60
Mean 51.17
Std Dev 3.733
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch39, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 58
Mean 56.55
Std Dev 3.276
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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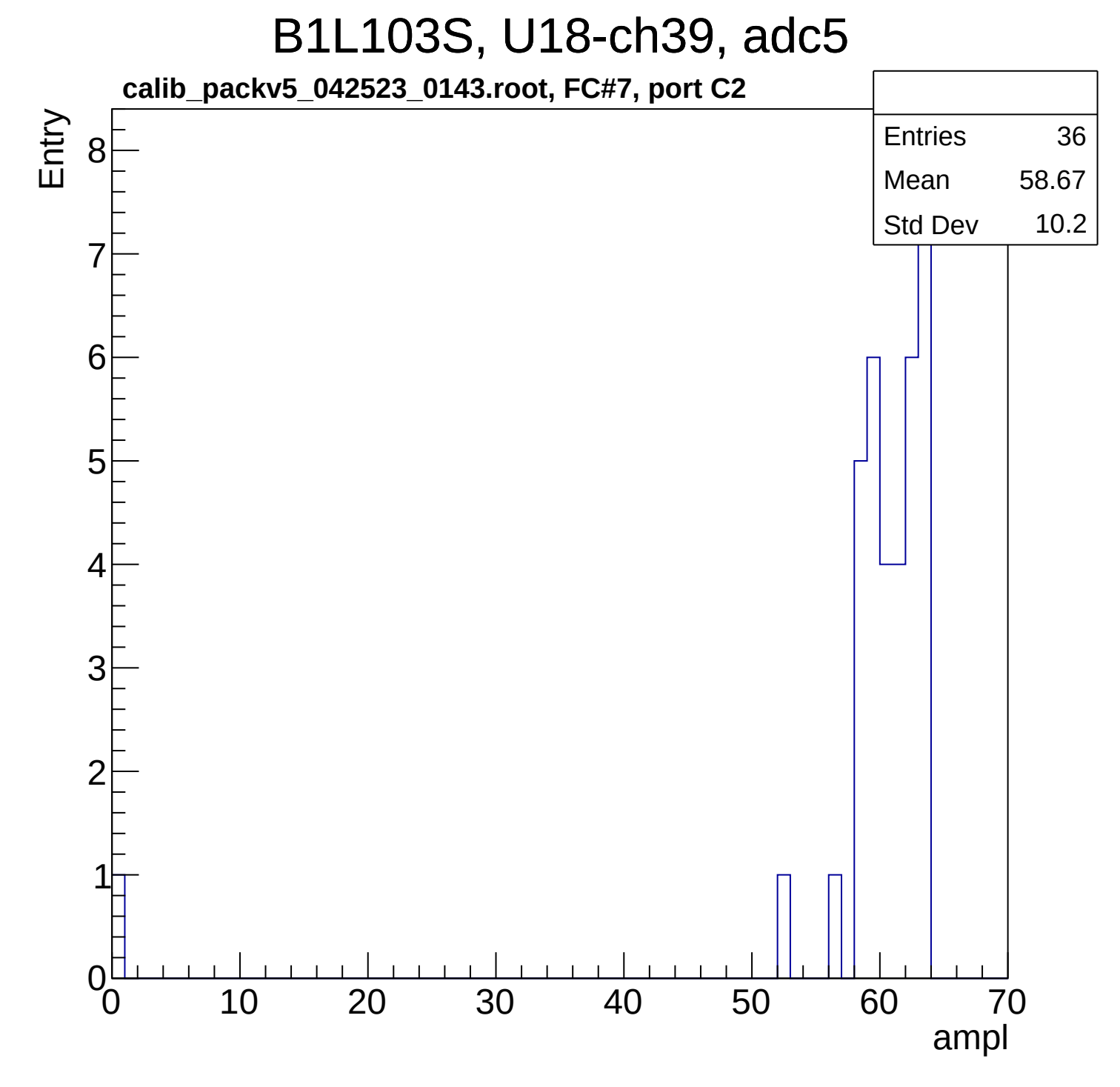
B1L103S, U18-ch39, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 36
Mean 58.67
Std Dev 10.2
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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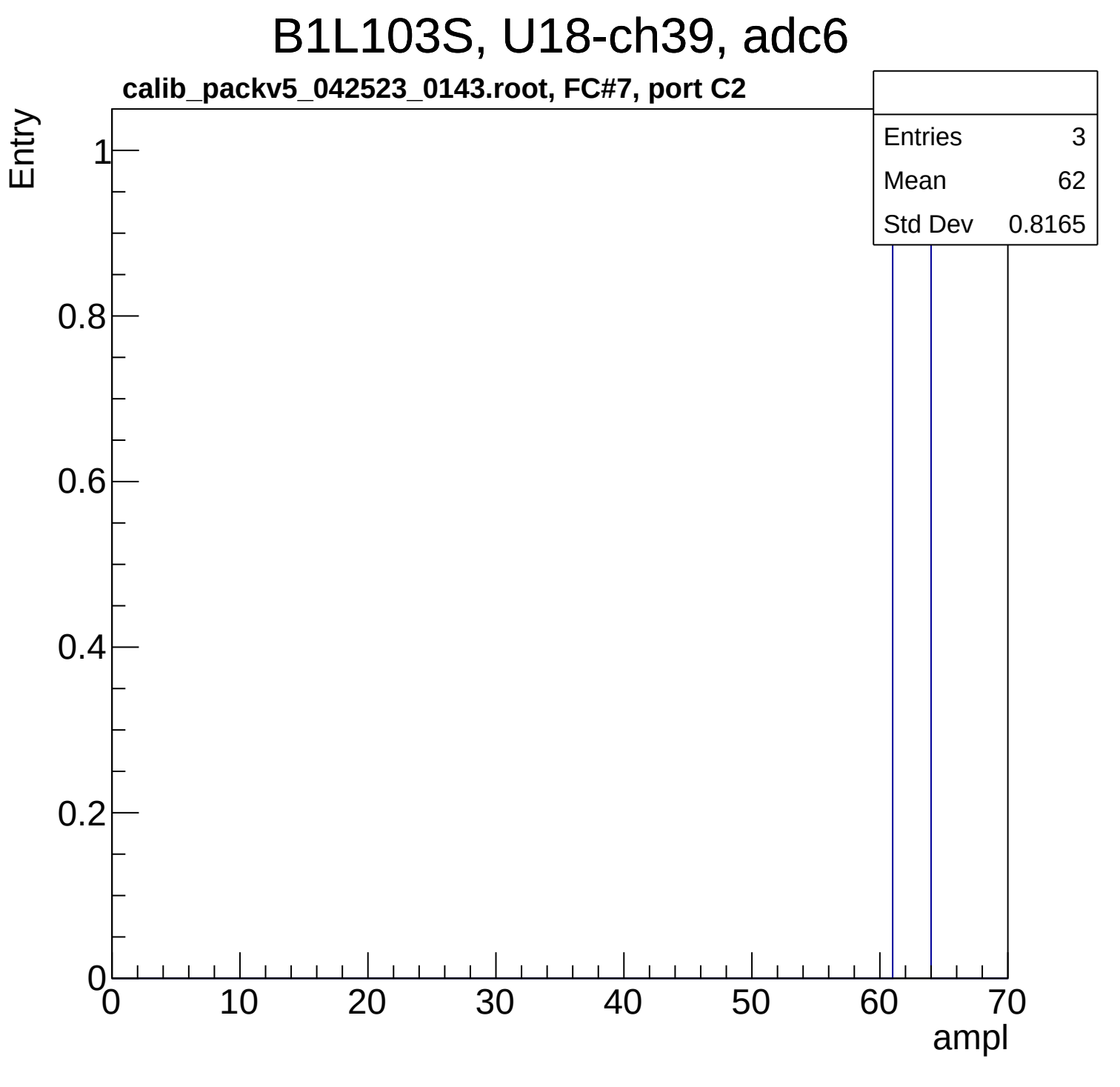
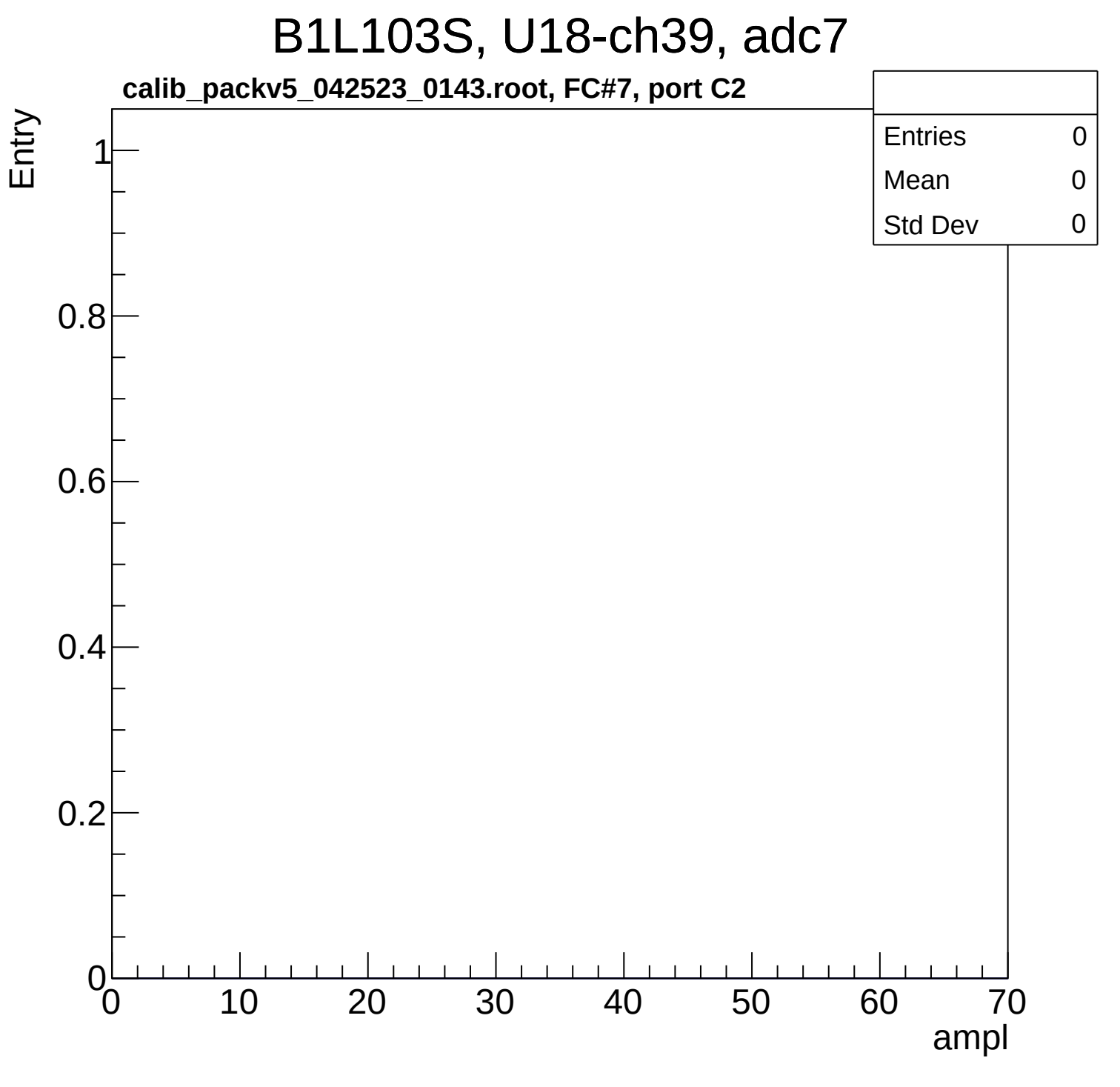
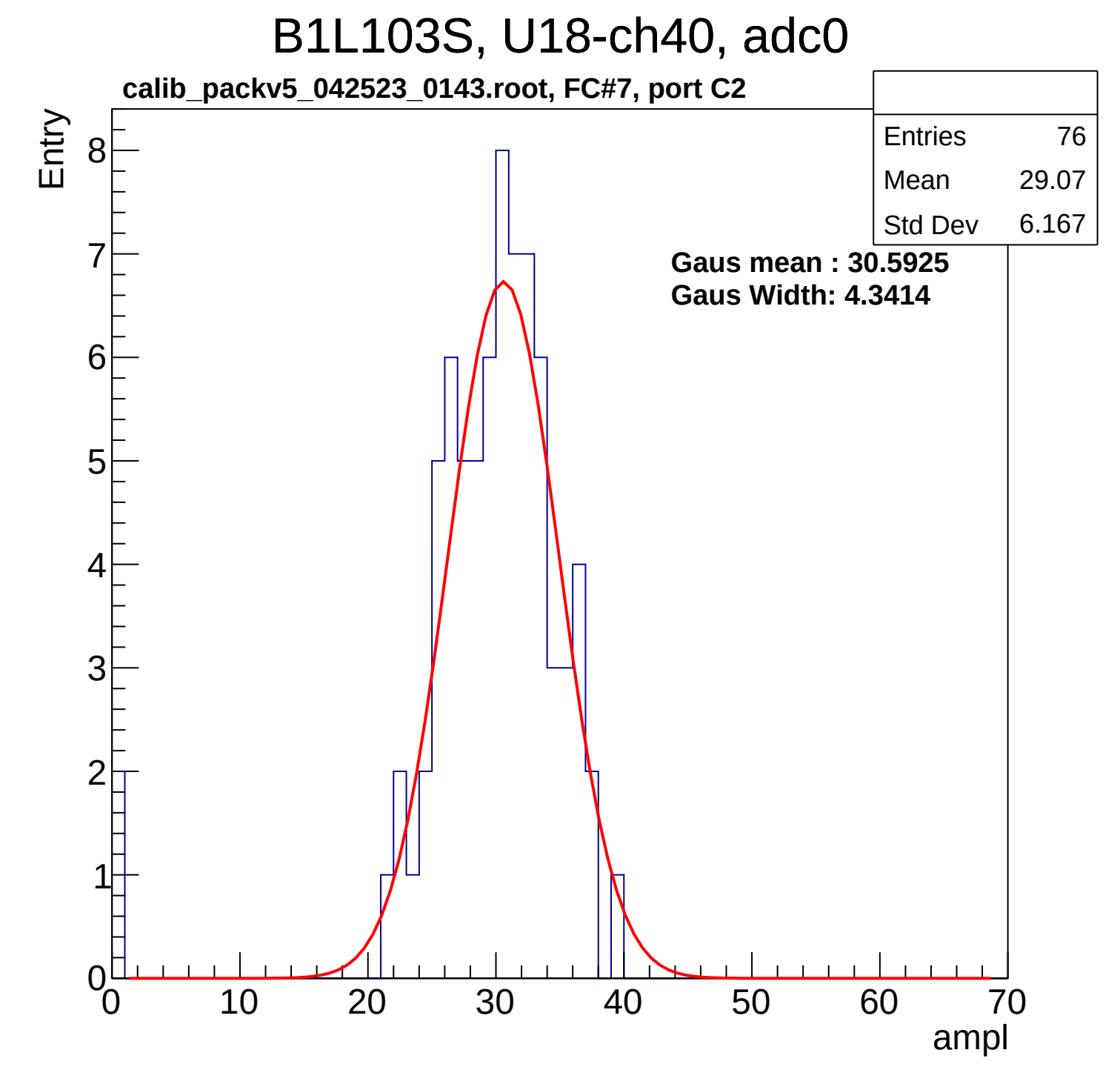
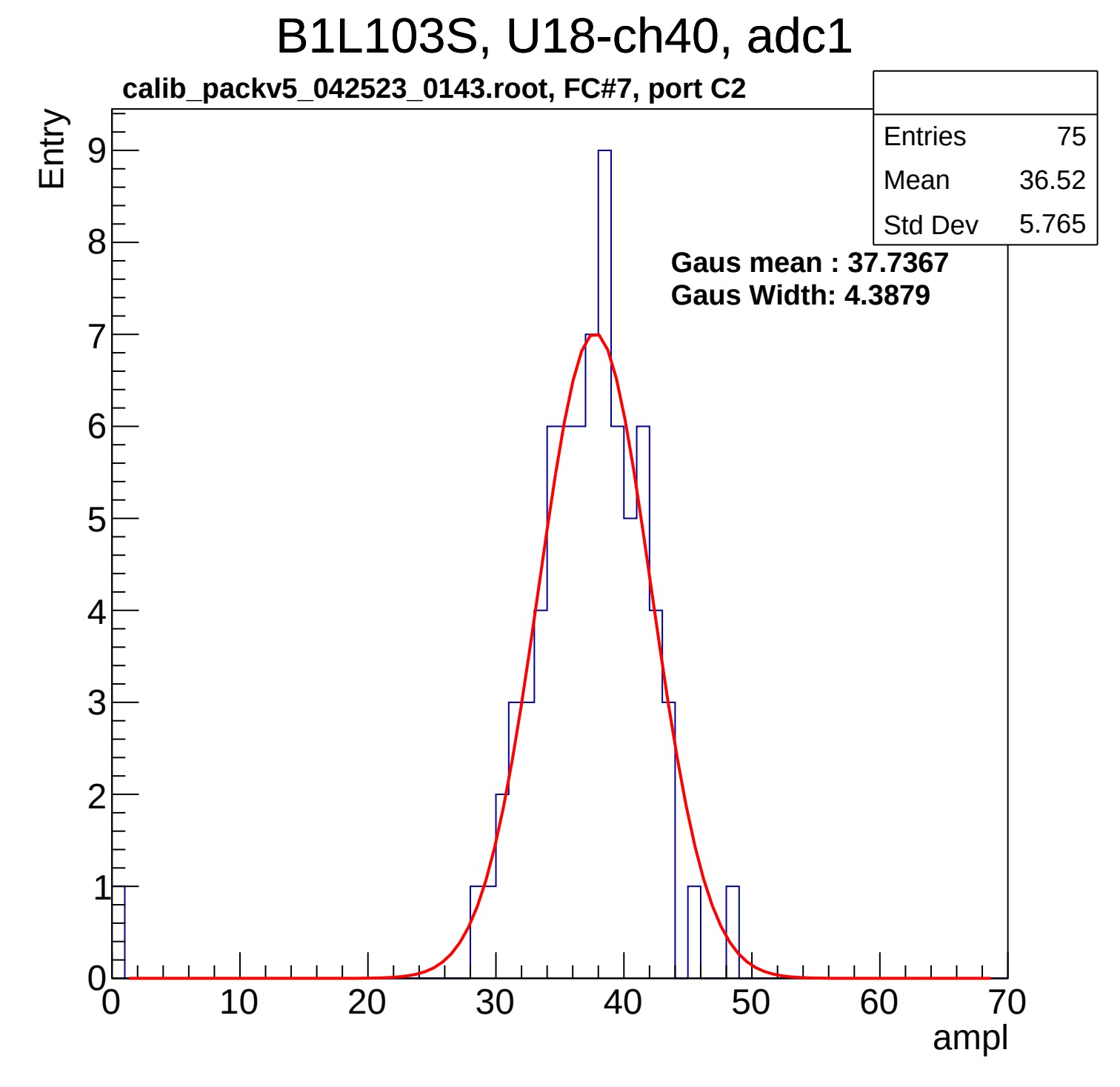

B1L103S, U18-ch39, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 62
Std Dev 0.8165
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch39, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch40, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 76
Mean 29.07
Std Dev 6.167
Gaus mean : 30.5925
Gaus Width: 4.3414
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch40, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 75
Mean 36.52
Std Dev 5.765
Gaus mean : 37.7367
Gaus Width: 4.3879
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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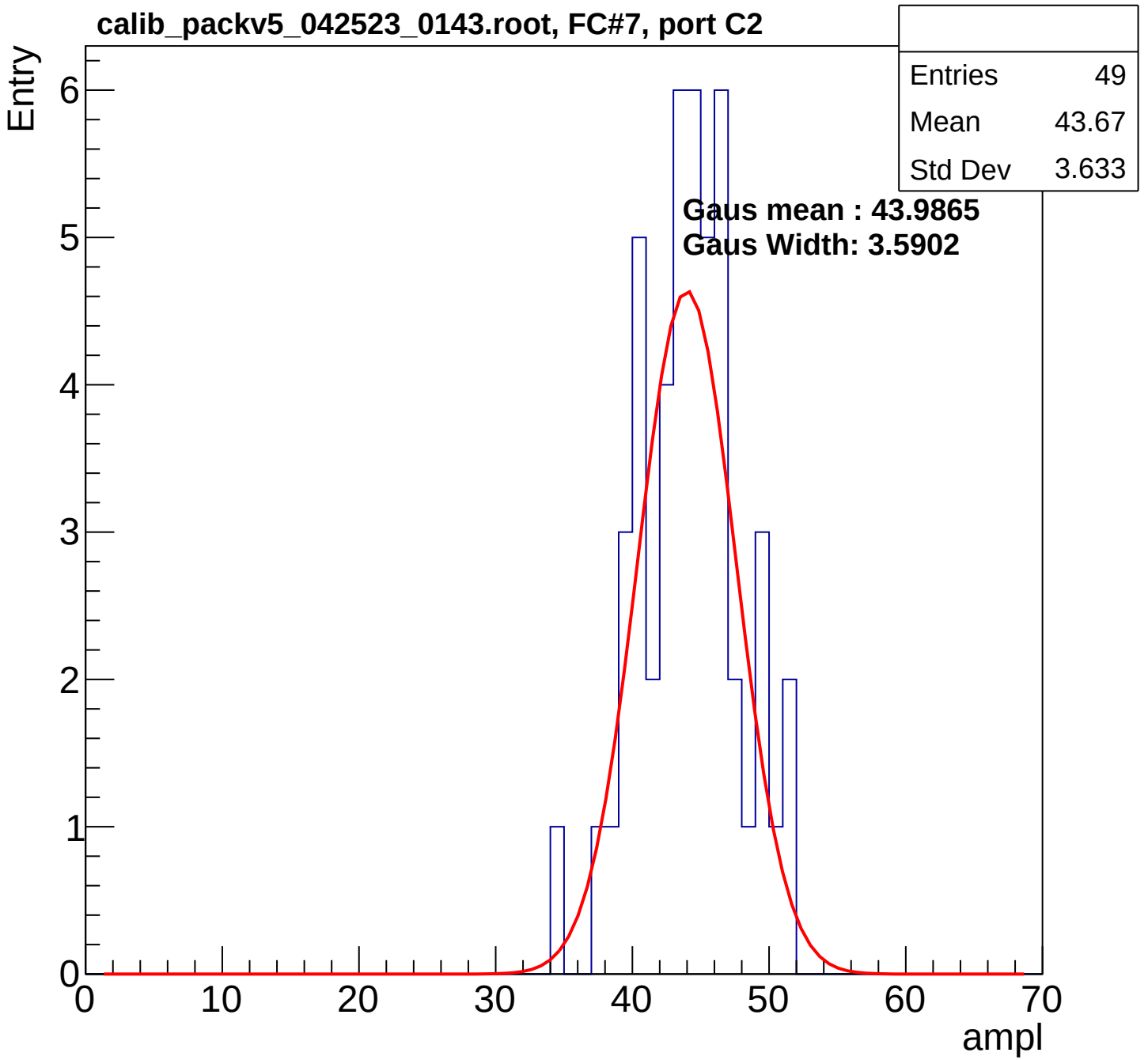
B1L103S, U18-ch40, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 49
Mean 43.67
Std Dev 3.633
Gaus mean : 43.9865
Gaus Width: 3.5902
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
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60
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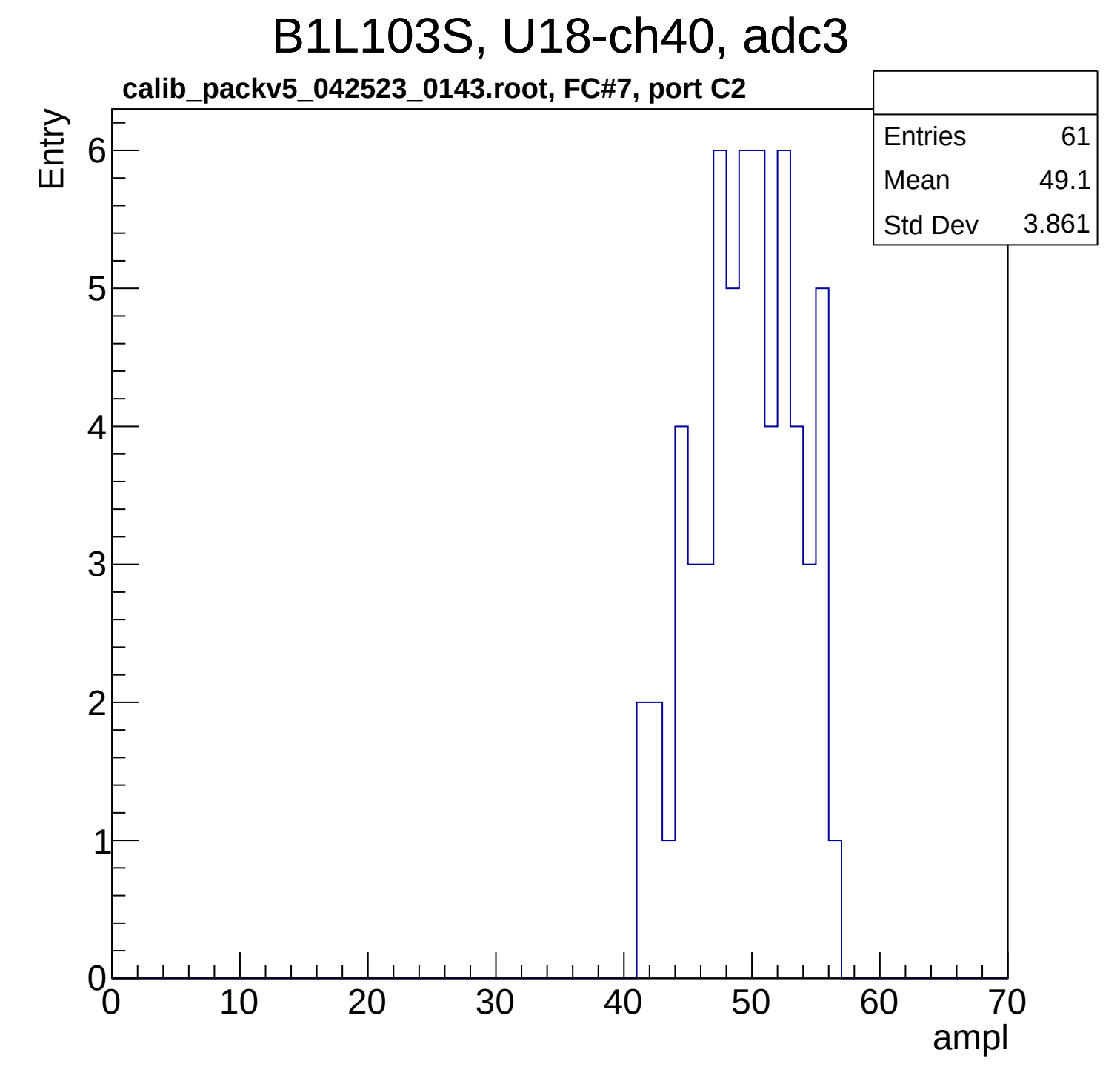
B1L103S, U18-ch40, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 61
Mean 49.1
Std Dev 3.861
Entry
ampl
0
1
2
3
4
5
6
0
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20
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40
50
60
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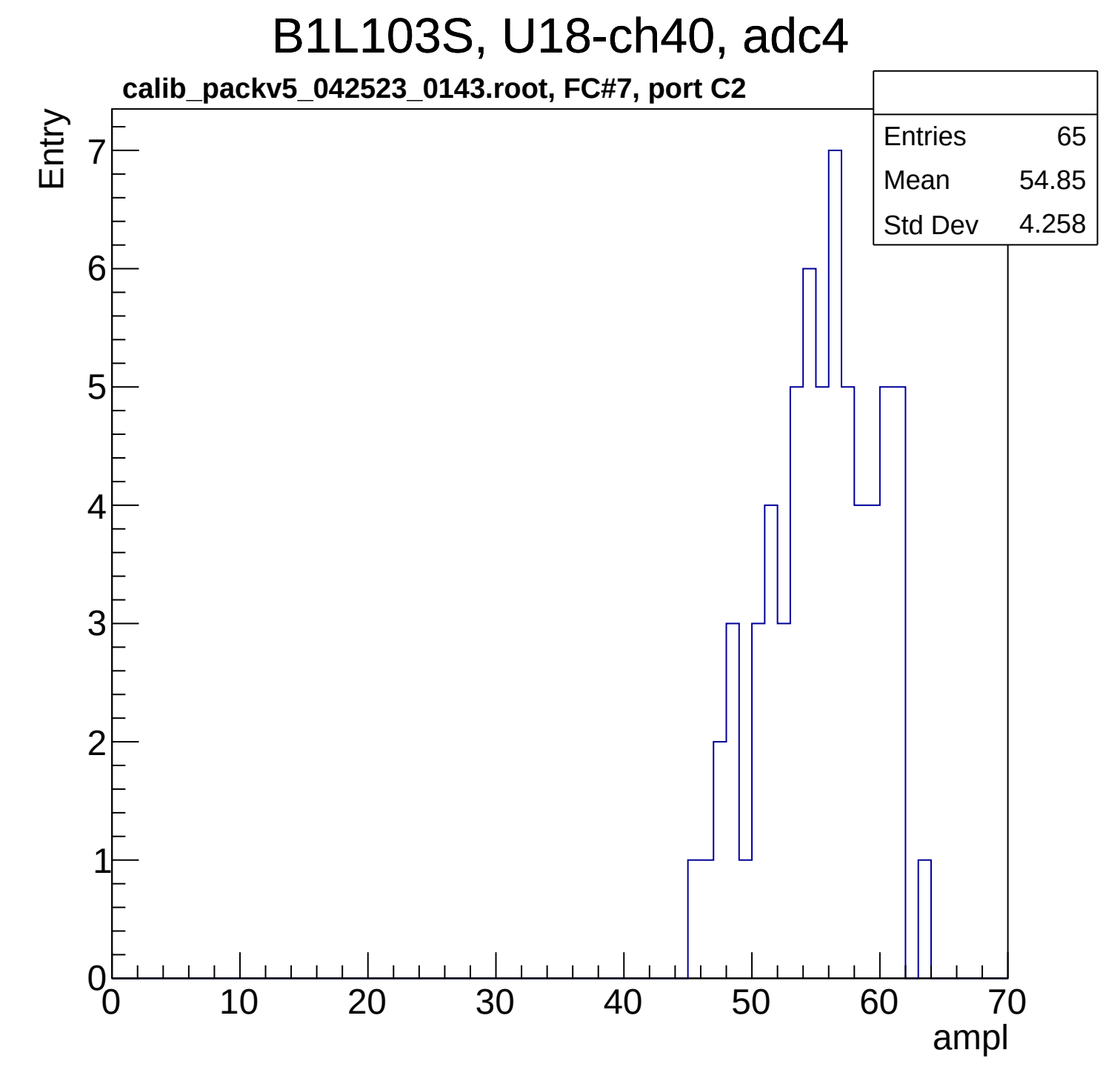
B1L103S, U18-ch40, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 54.85
Std Dev 4.258
Entry
ampl
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1
2
3
4
5
6
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0
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20
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40
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60
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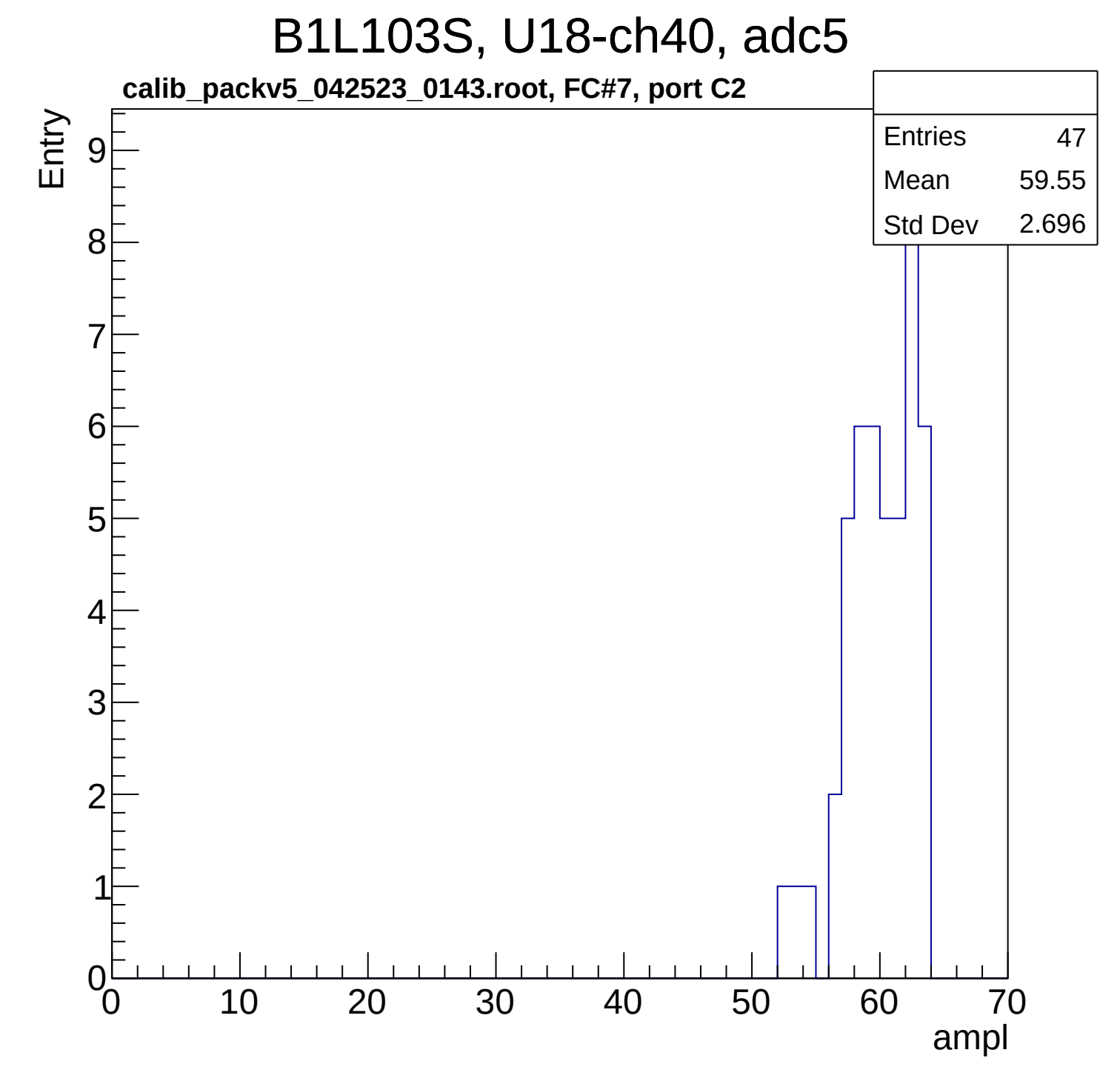
B1L103S, U18-ch40, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 47
Mean 59.55
Std Dev 2.696
Entry
ampl
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2
3
4
5
6
7
8
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0
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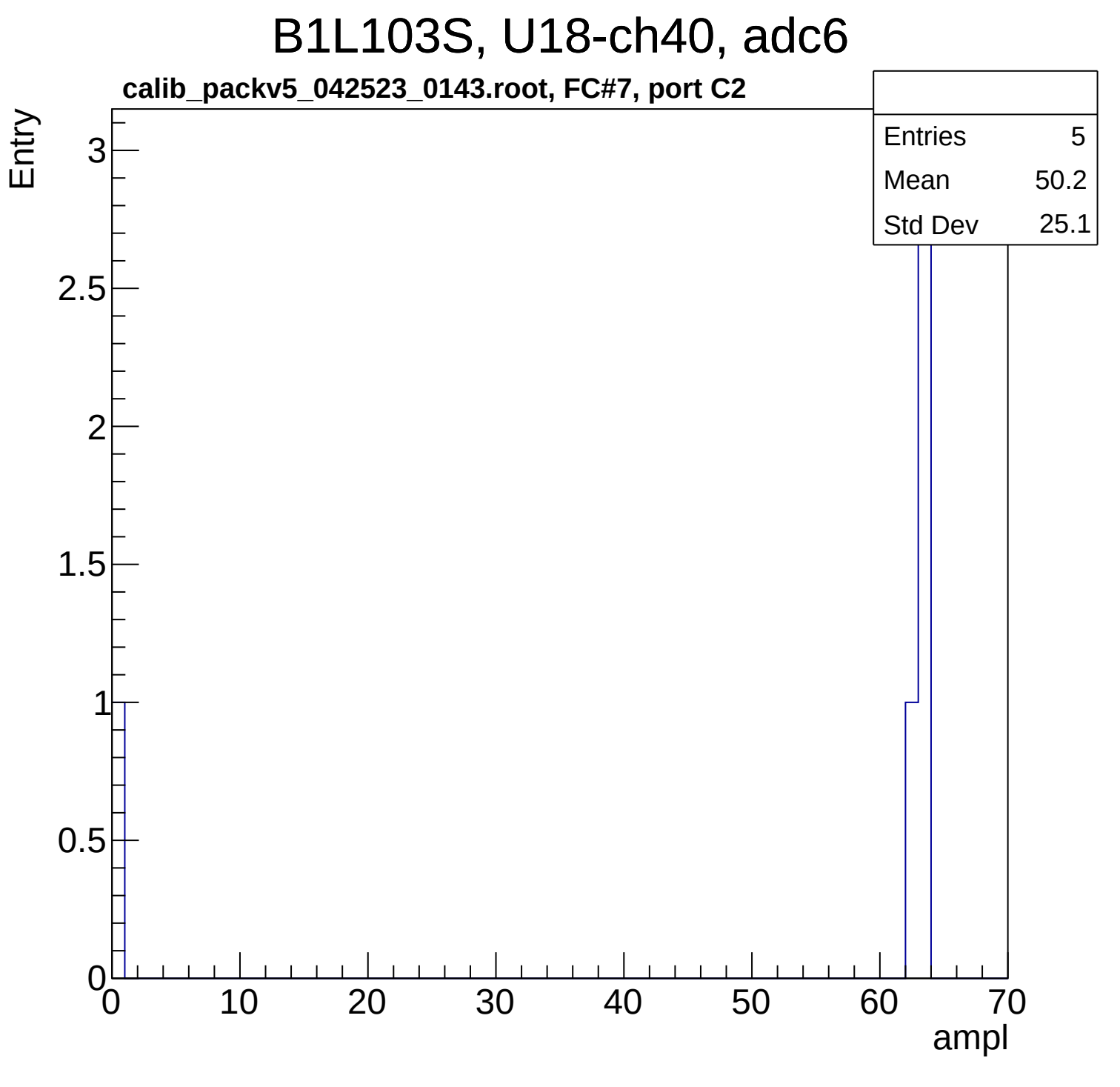
B1L103S, U18-ch40, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 5
Mean 50.2
Std Dev 25.1
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
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20
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40
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60
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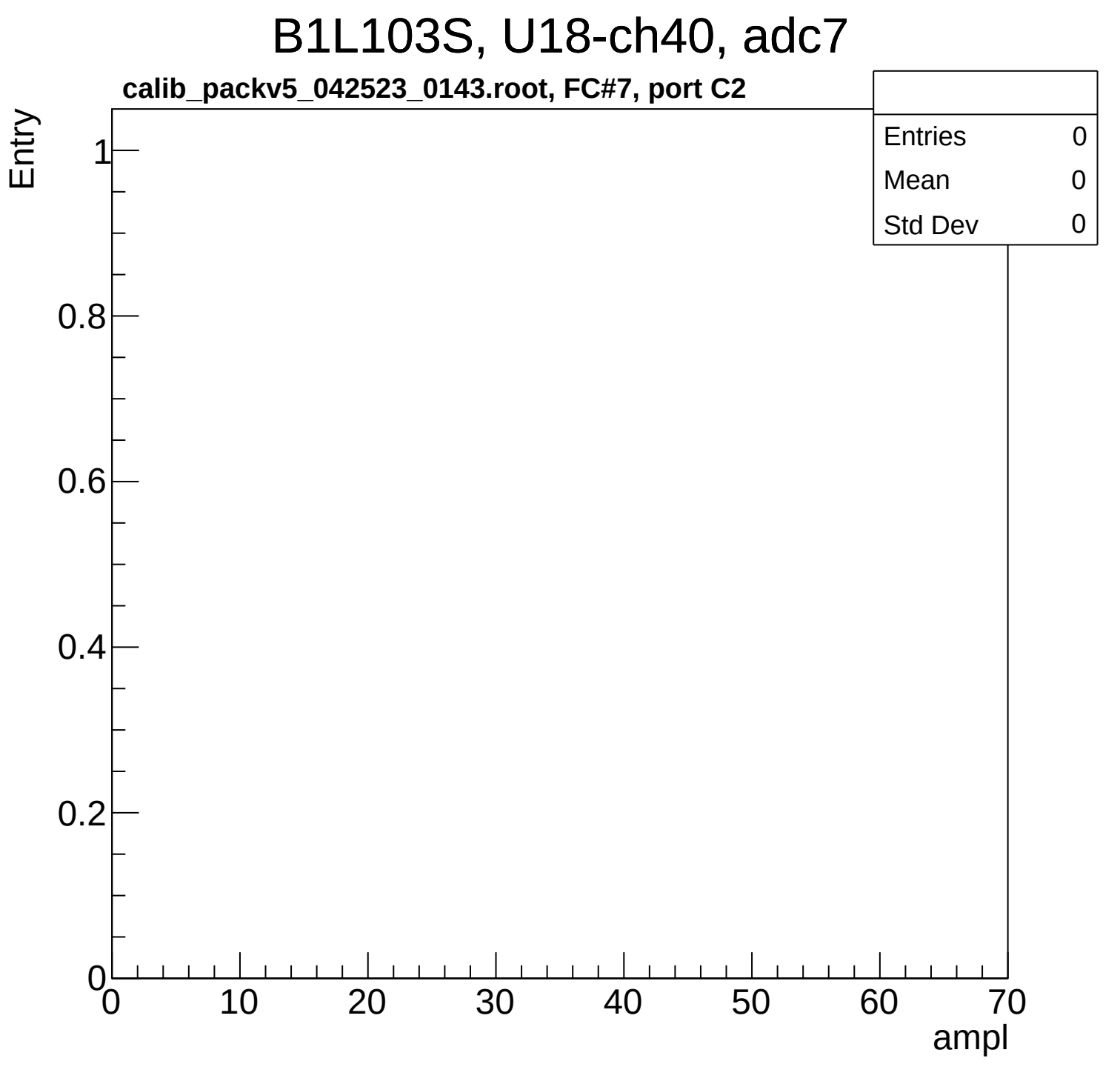
B1L103S, U18-ch40, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
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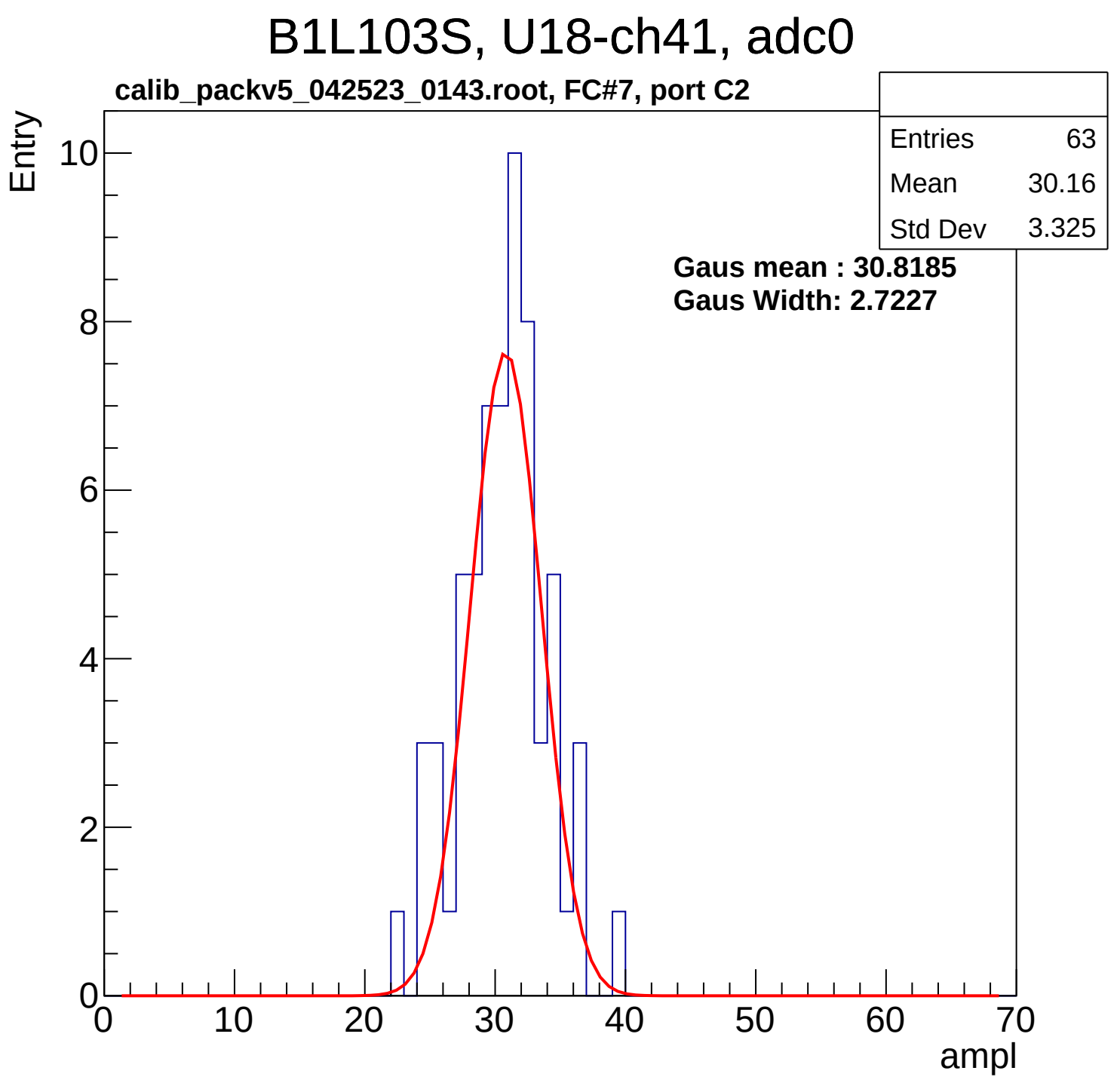
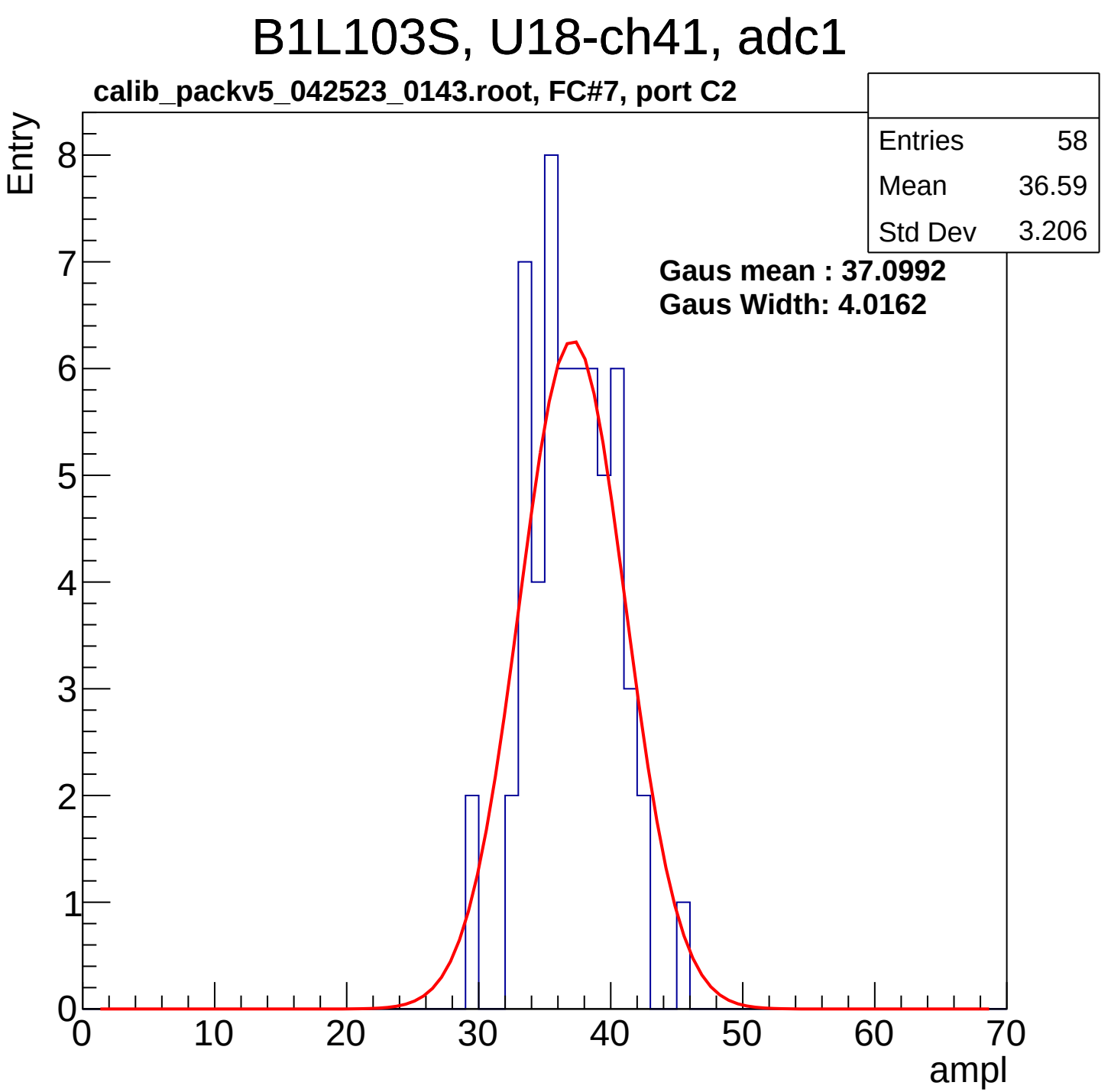
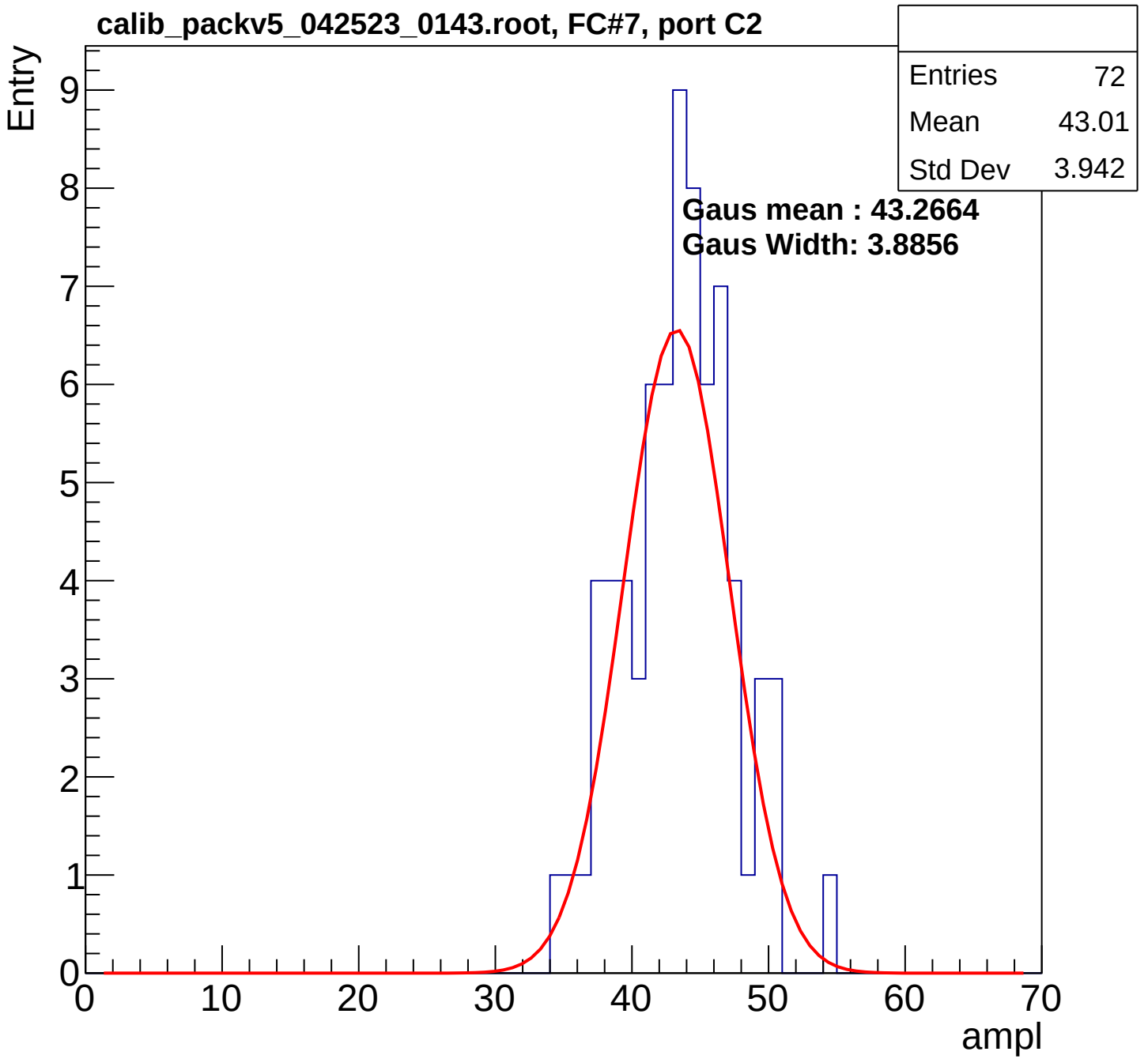
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch41, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 30.16
Std Dev 3.325
Gaus mean : 30.8185
Gaus Width: 2.7227
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch41, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 58
Mean 36.59
Std Dev 3.206
Gaus mean : 37.0992
Gaus Width: 4.0162
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch41, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 72
Mean 43.01
Std Dev 3.942
Gaus mean : 43.2664
Gaus Width: 3.8856
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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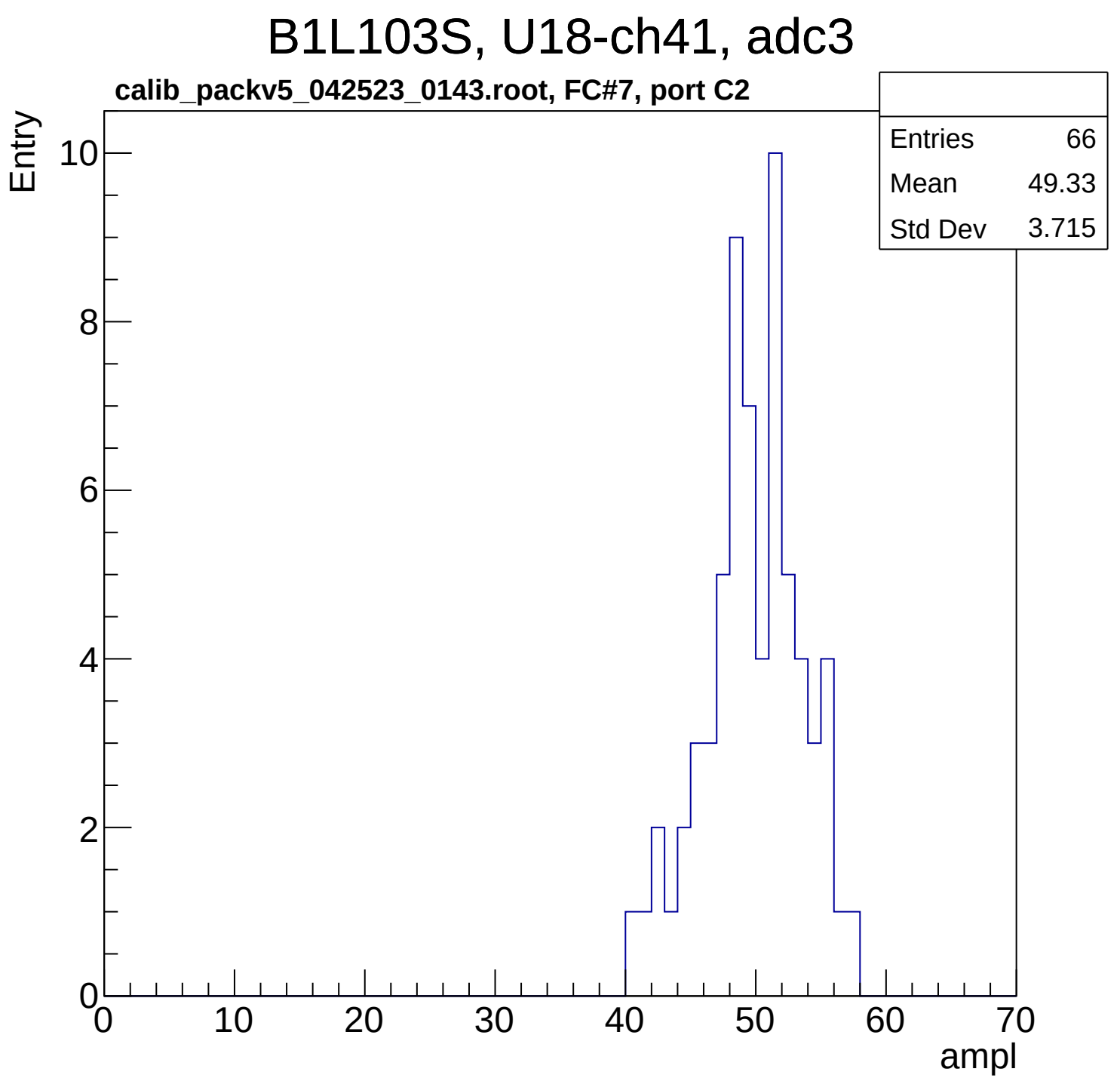
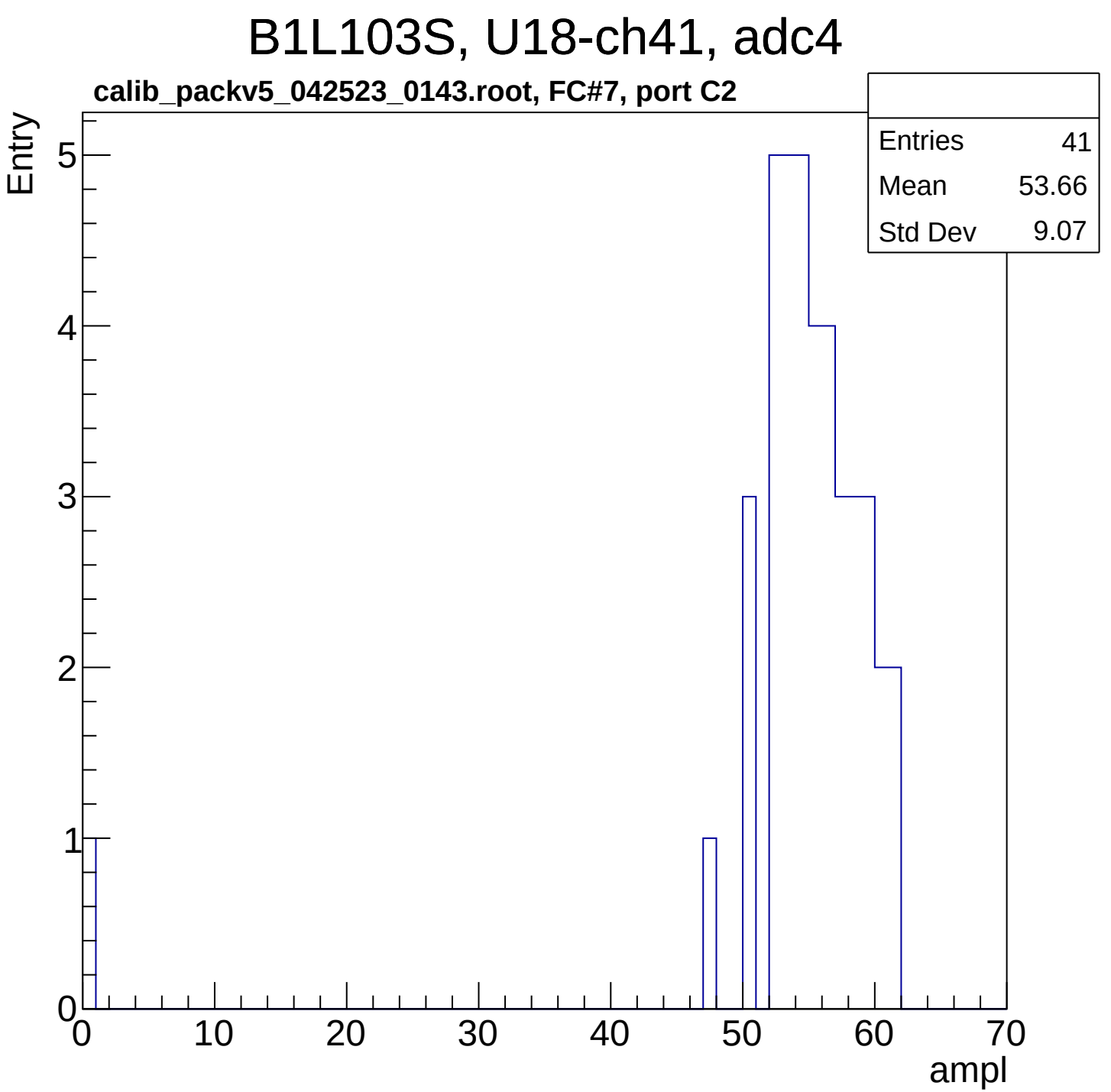
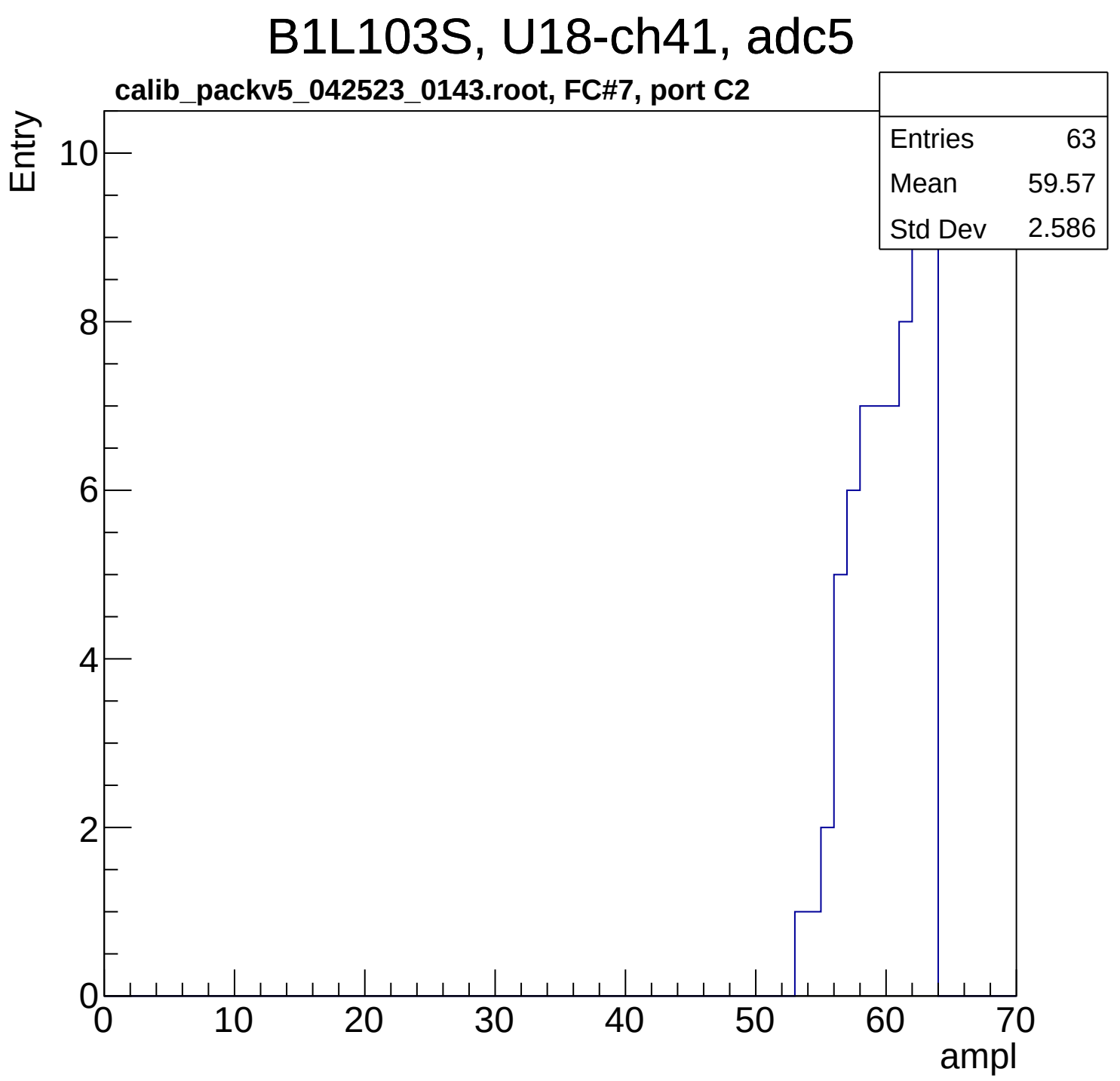
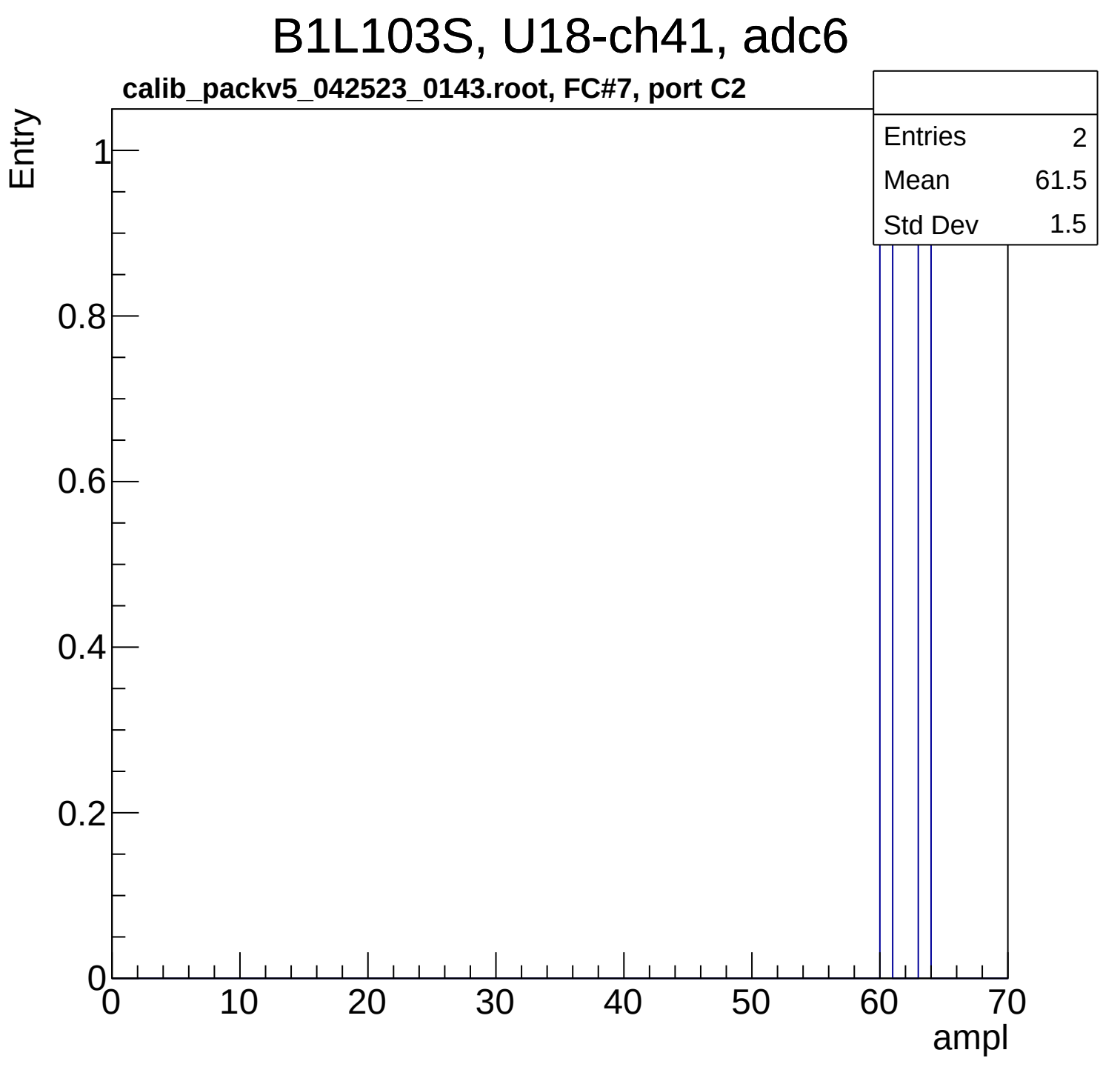
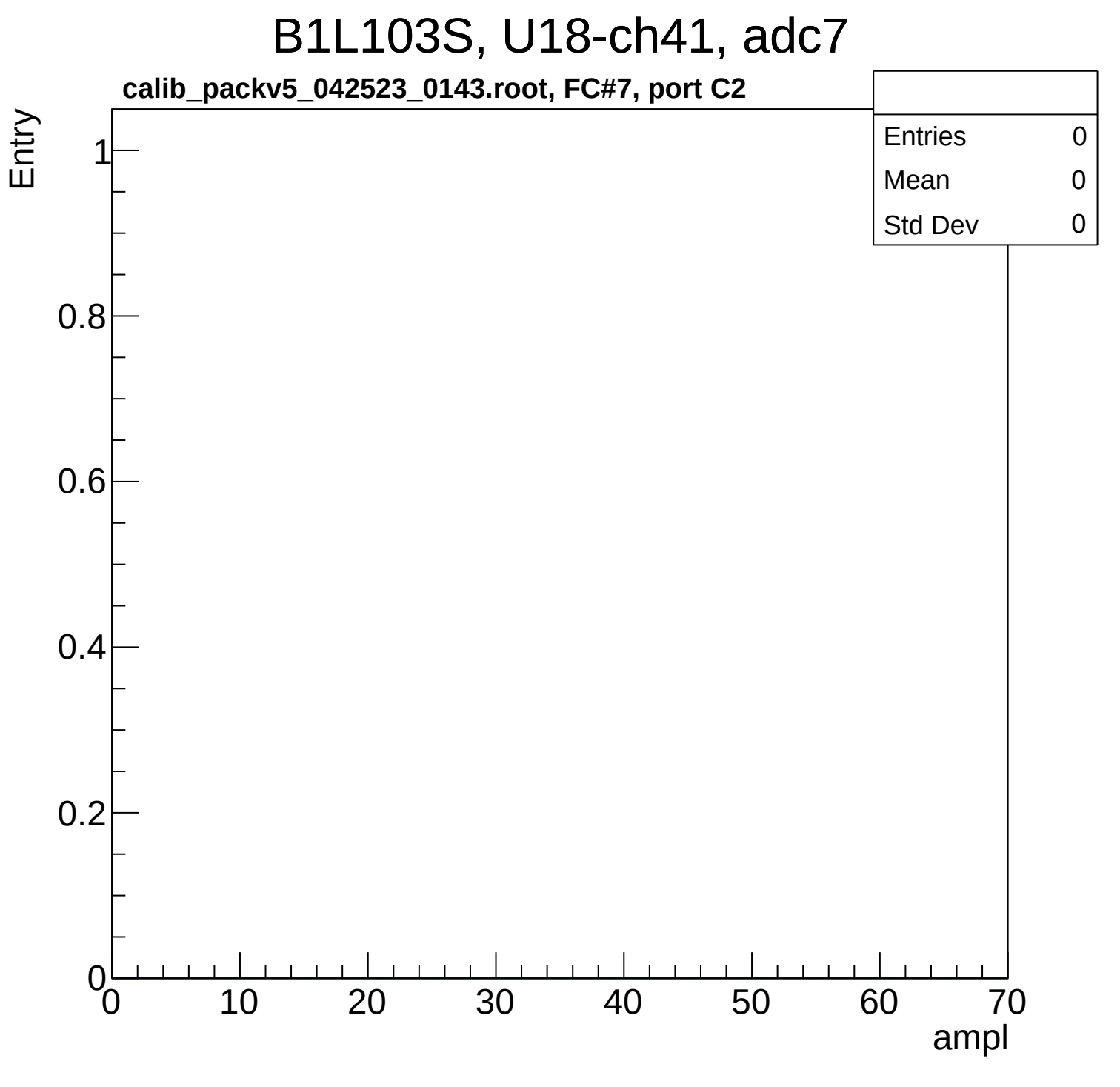

B1L103S, U18-ch41, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 49.33
Std Dev 3.715
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch41, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 41
Mean 53.66
Std Dev 9.07
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch41, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 59.57
Std Dev 2.586
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch41, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 61.5
Std Dev 1.5
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B1L103S, U18-ch41, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
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0.8
0.6
0.4
0.2
0
0
10
20
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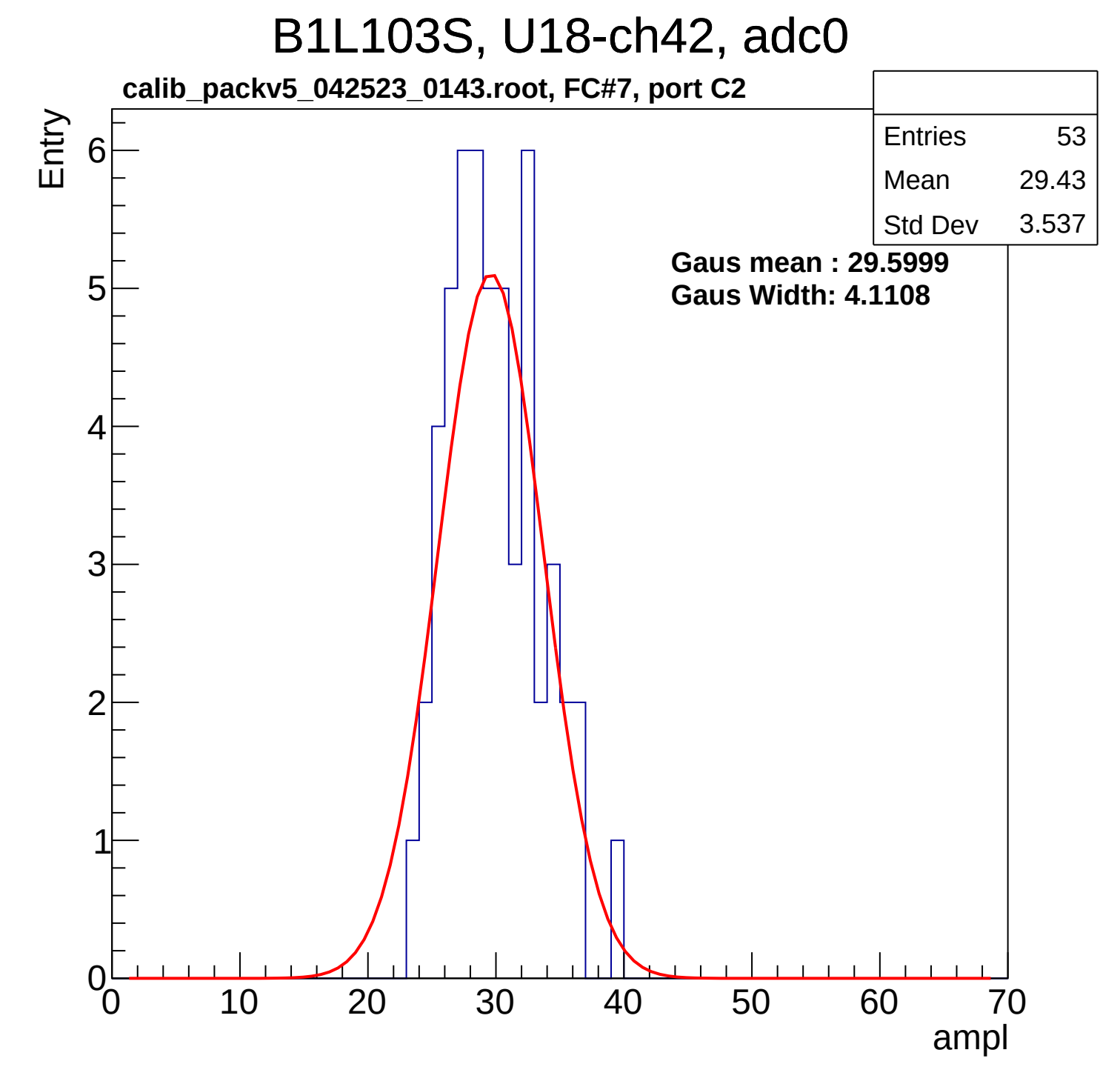
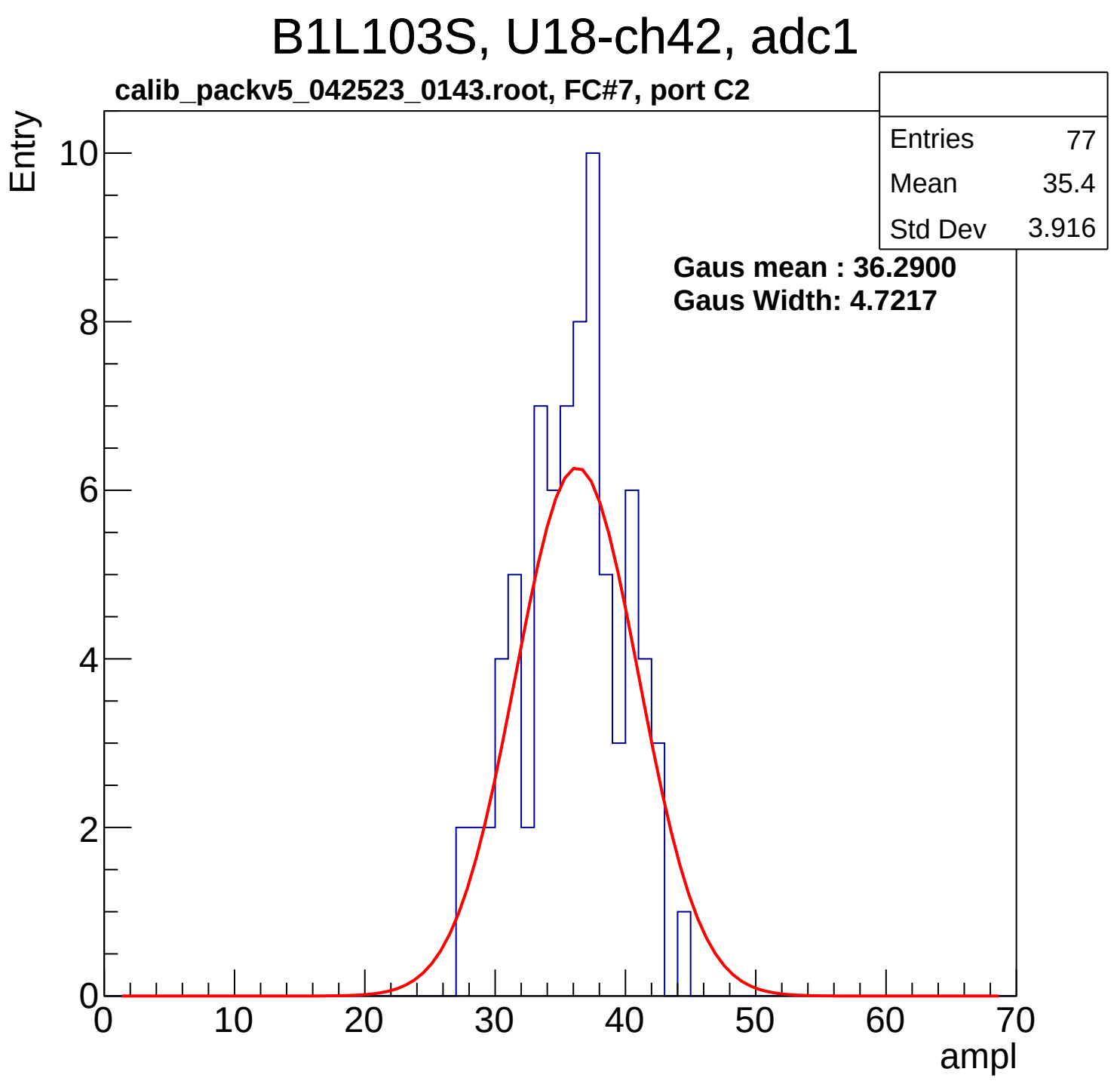
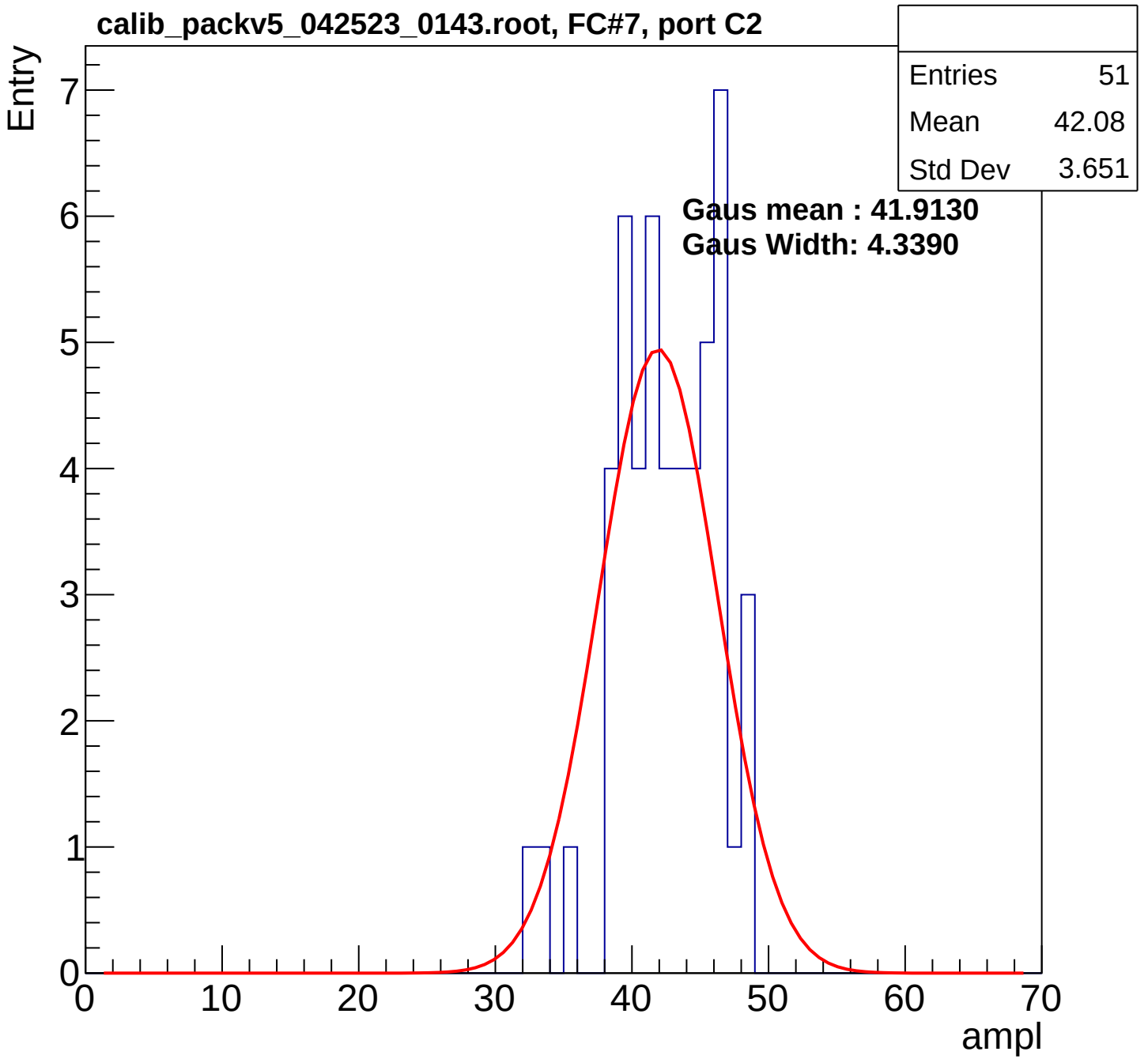
60
70
ampl


B1L103S, U18-ch42, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 29.43
Std Dev 3.537
Gaus mean : 29.5999
Gaus Width: 4.1108
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U18-ch42, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 77
Mean 35.4
Std Dev 3.916
Gaus mean : 36.2900
Gaus Width: 4.7217
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch42, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 51
Mean 42.08
Std Dev 3.651
Gaus mean : 41.9130
Gaus Width: 4.3390
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
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40
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60
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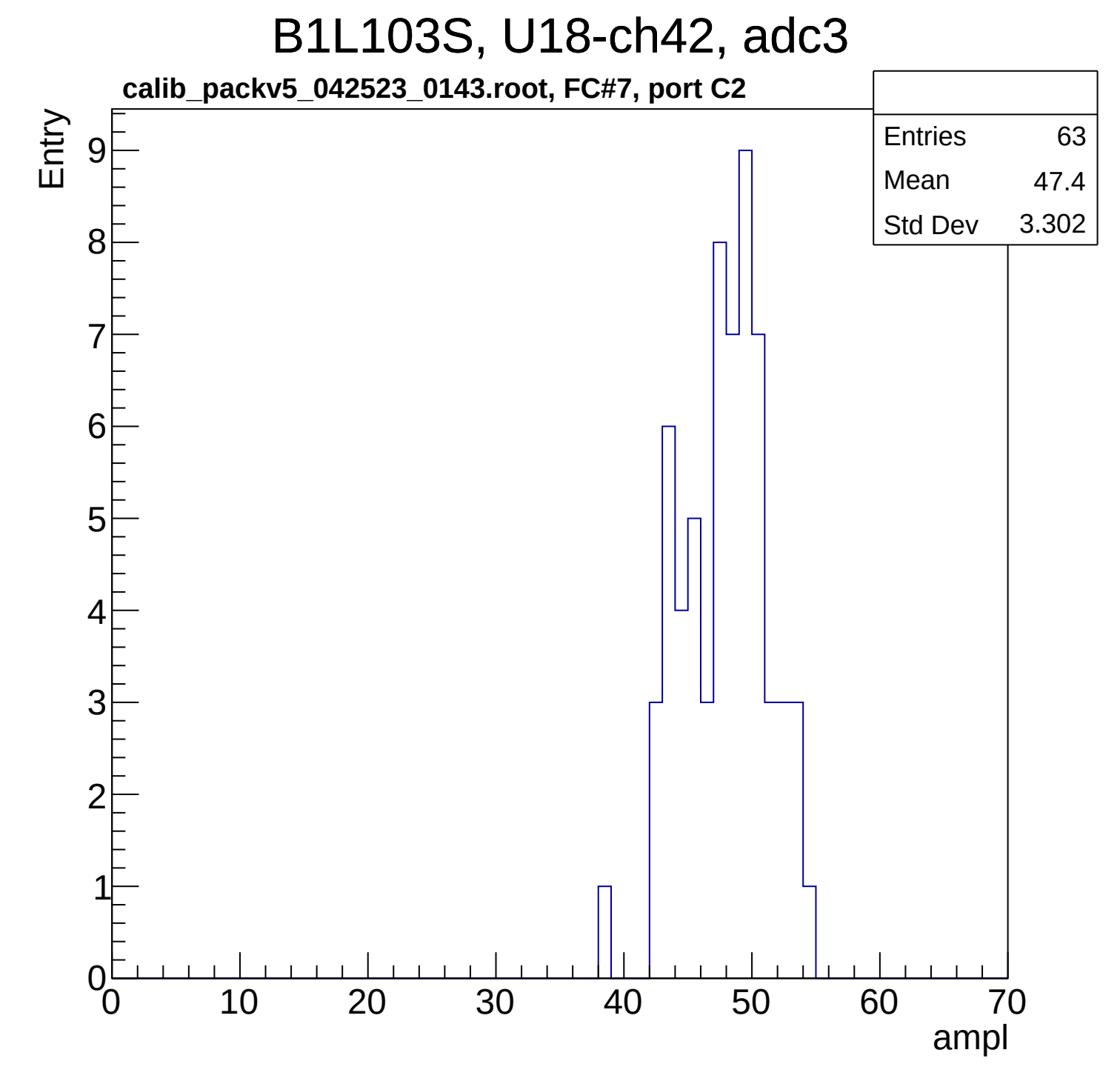
B1L103S, U18-ch42, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 47.4
Std Dev 3.302
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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20
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40
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60
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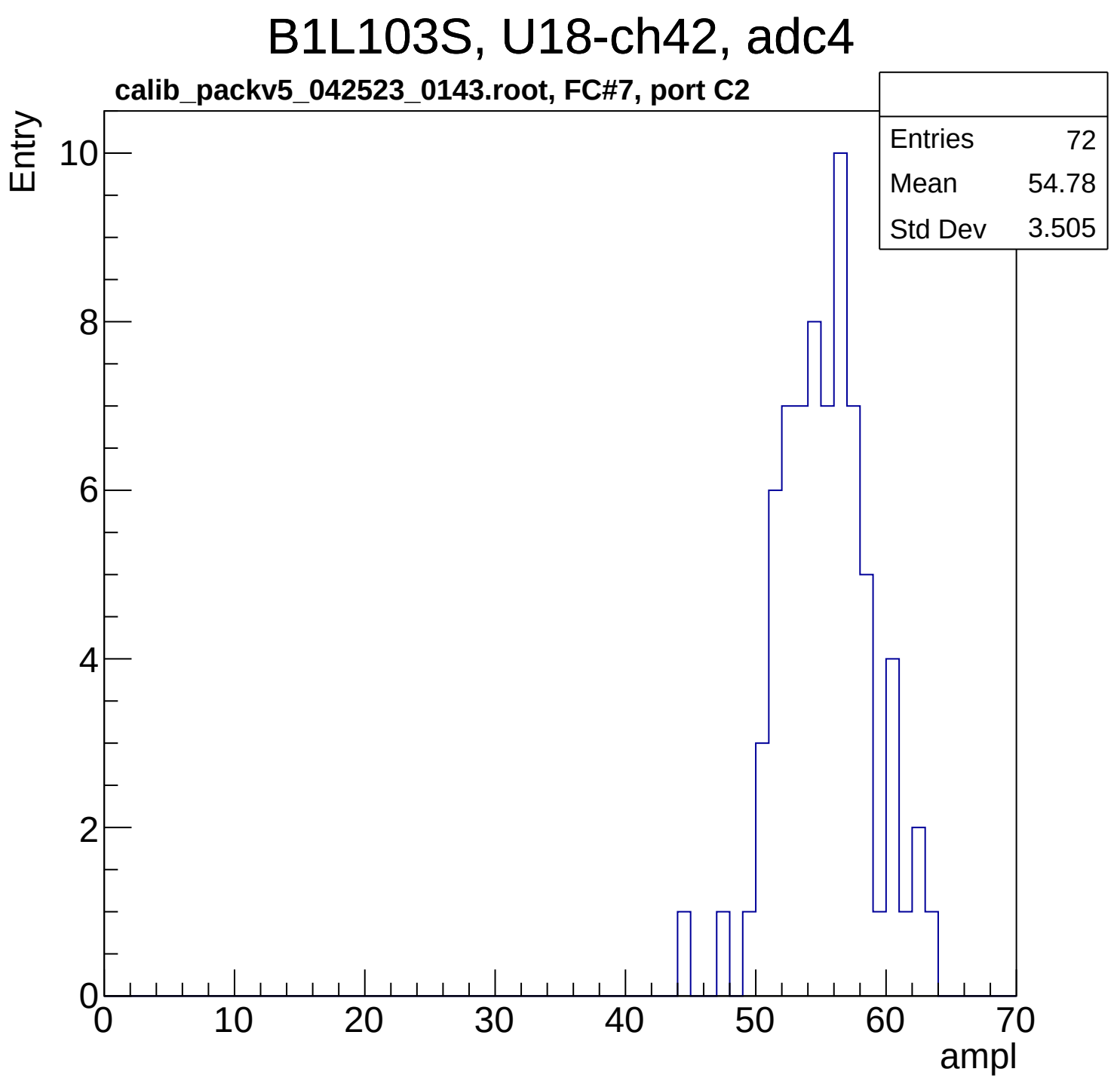
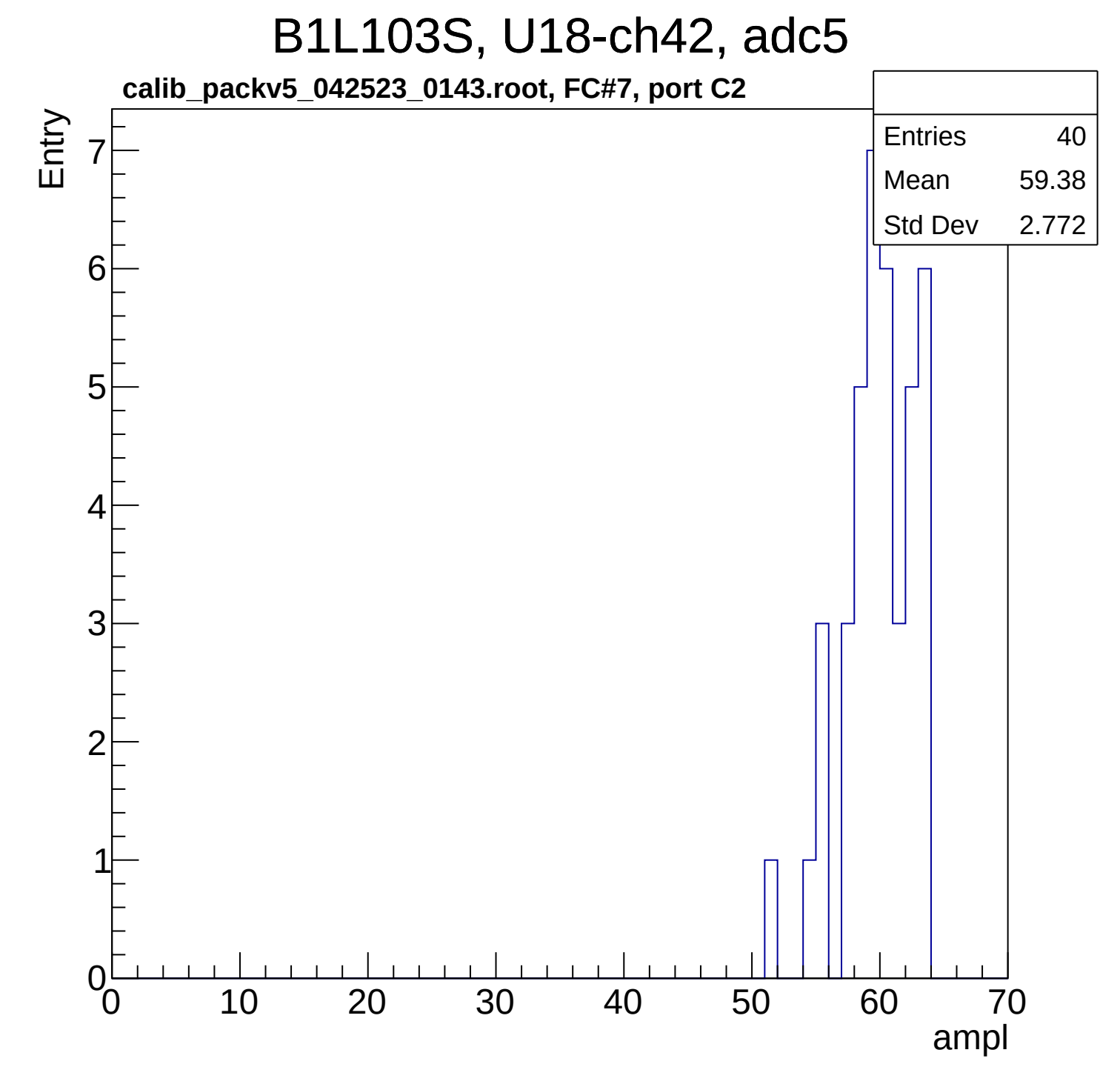

B1L103S, U18-ch42, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 72
Mean 54.78
Std Dev 3.505
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch42, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 40
Mean 59.38
Std Dev 2.772
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
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60
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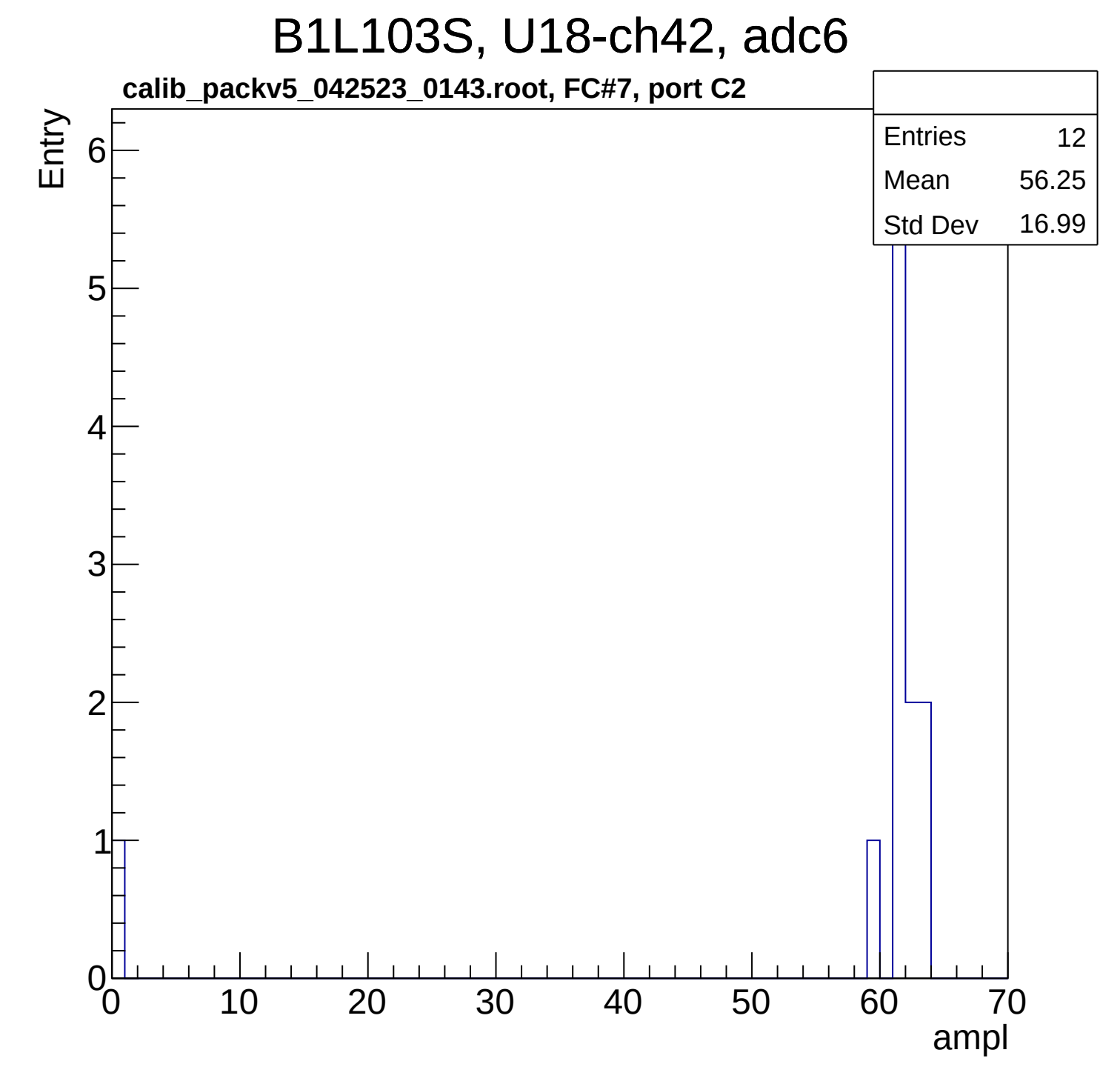
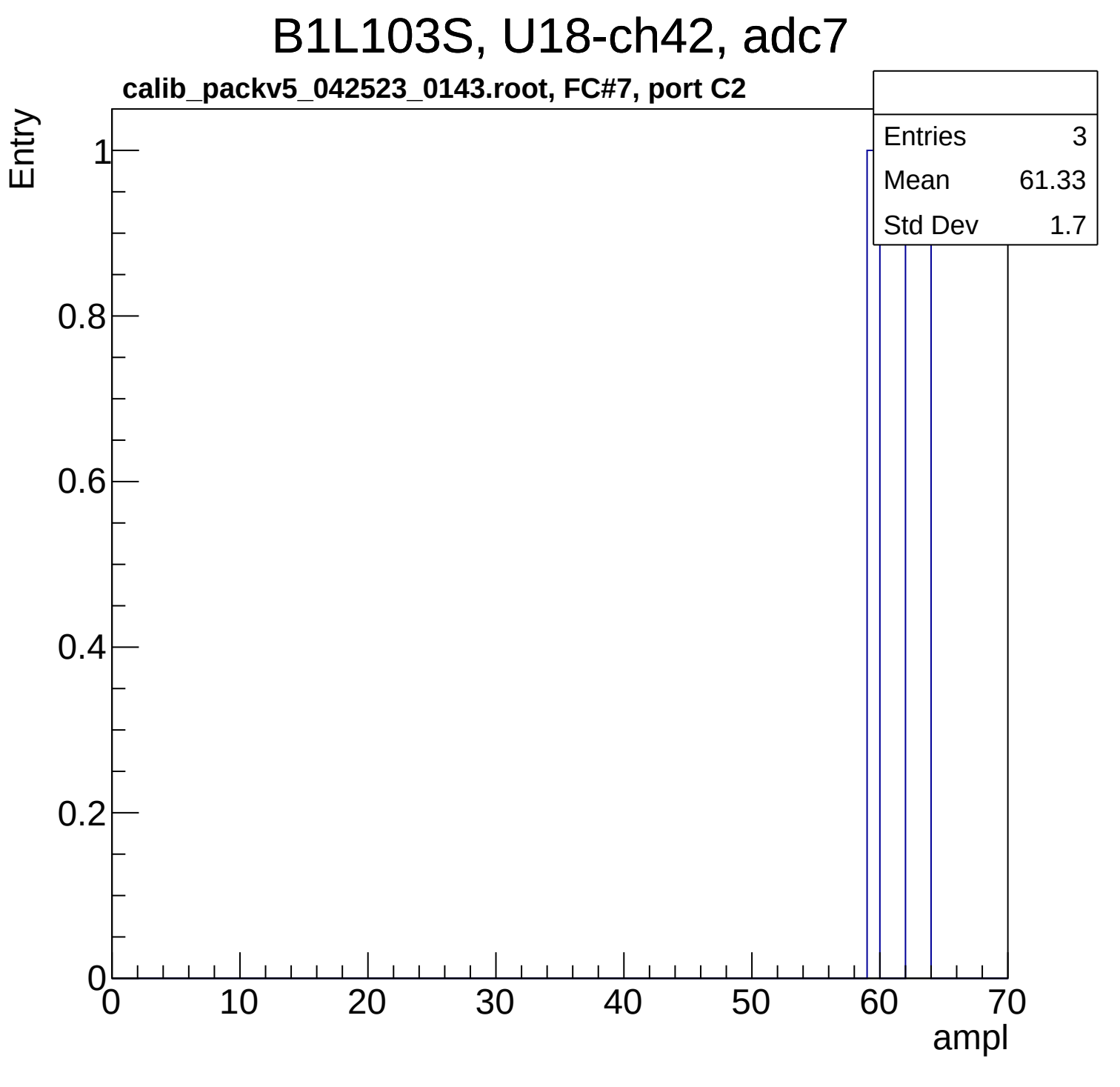
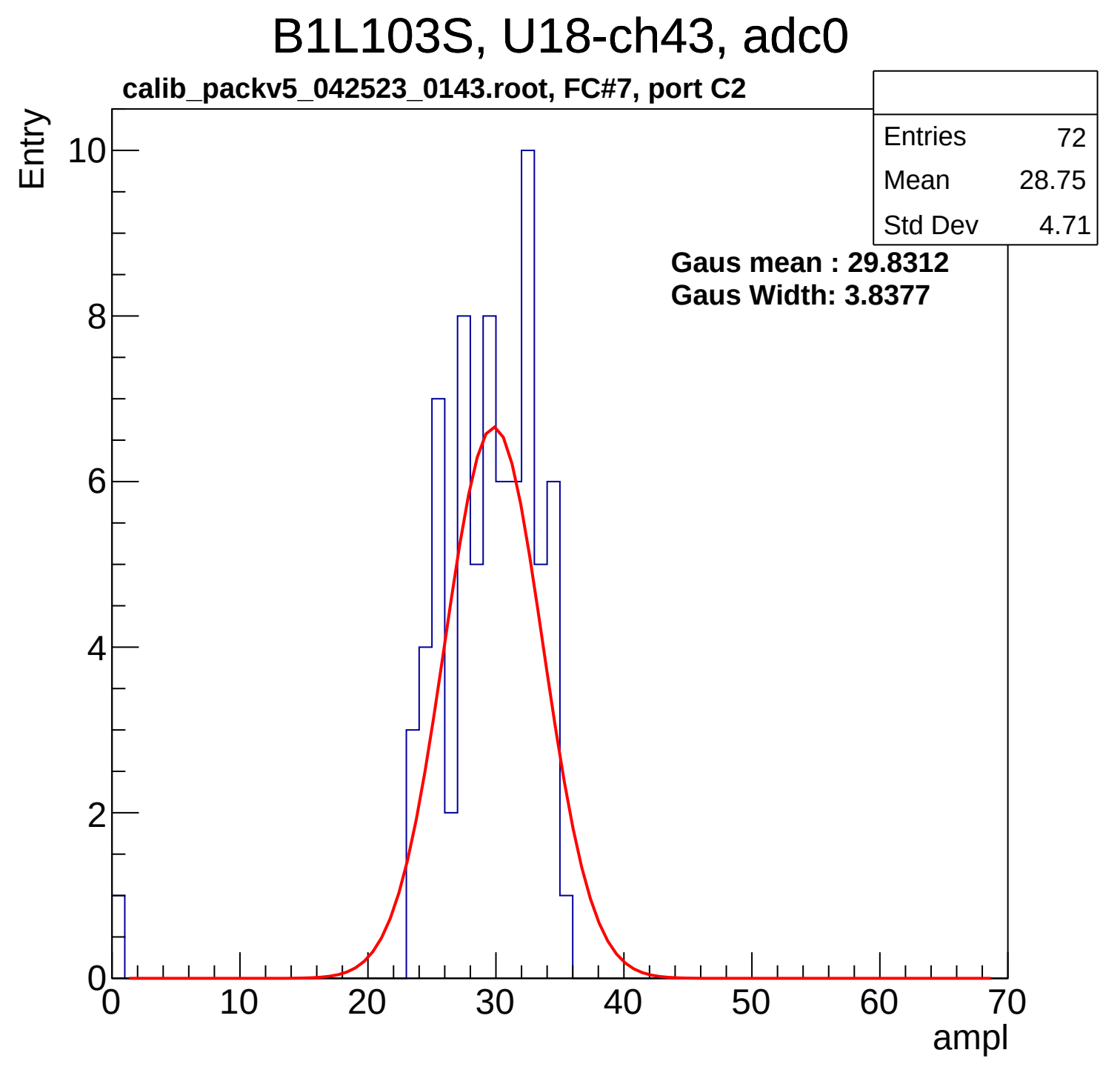
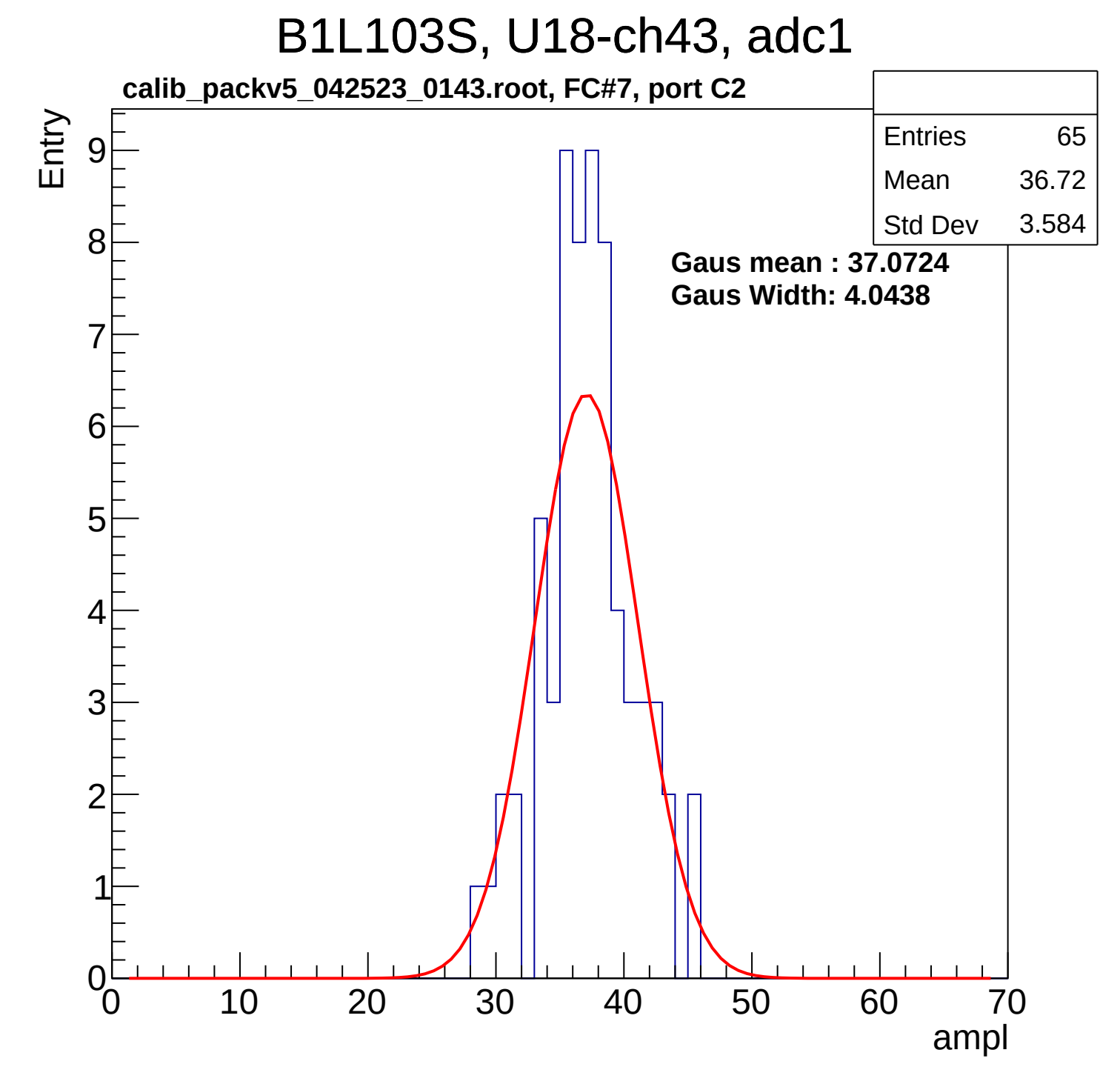

B1L103S, U18-ch42, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 12
Mean 56.25
Std Dev 16.99
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch42, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 61.33
Std Dev 1.7
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B1L103S, U18-ch43, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 72
Mean 28.75
Std Dev 4.71
Gaus mean : 29.8312
Gaus Width: 3.8377
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch43, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 36.72
Std Dev 3.584
Gaus mean : 37.0724
Gaus Width: 4.0438
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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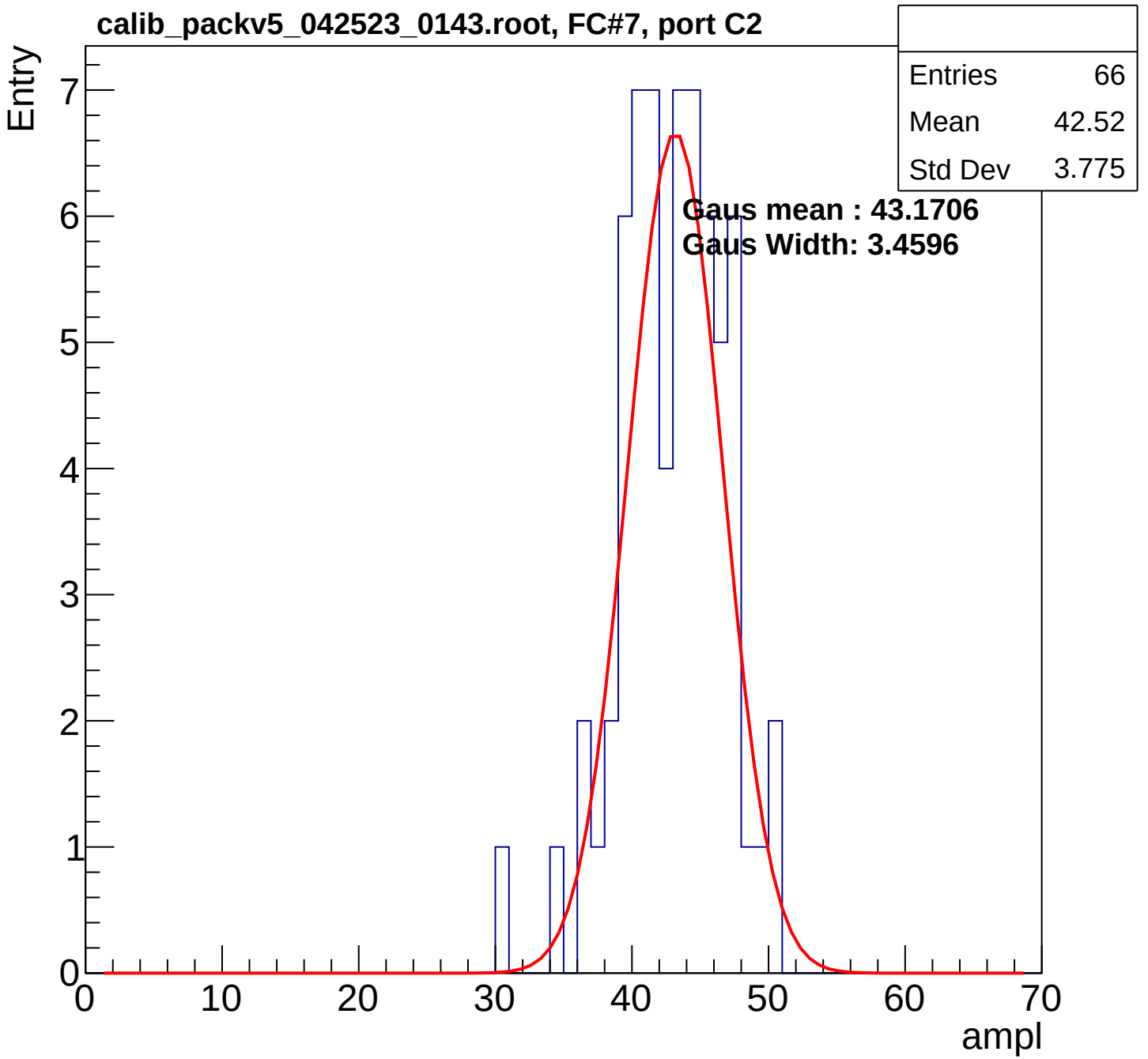
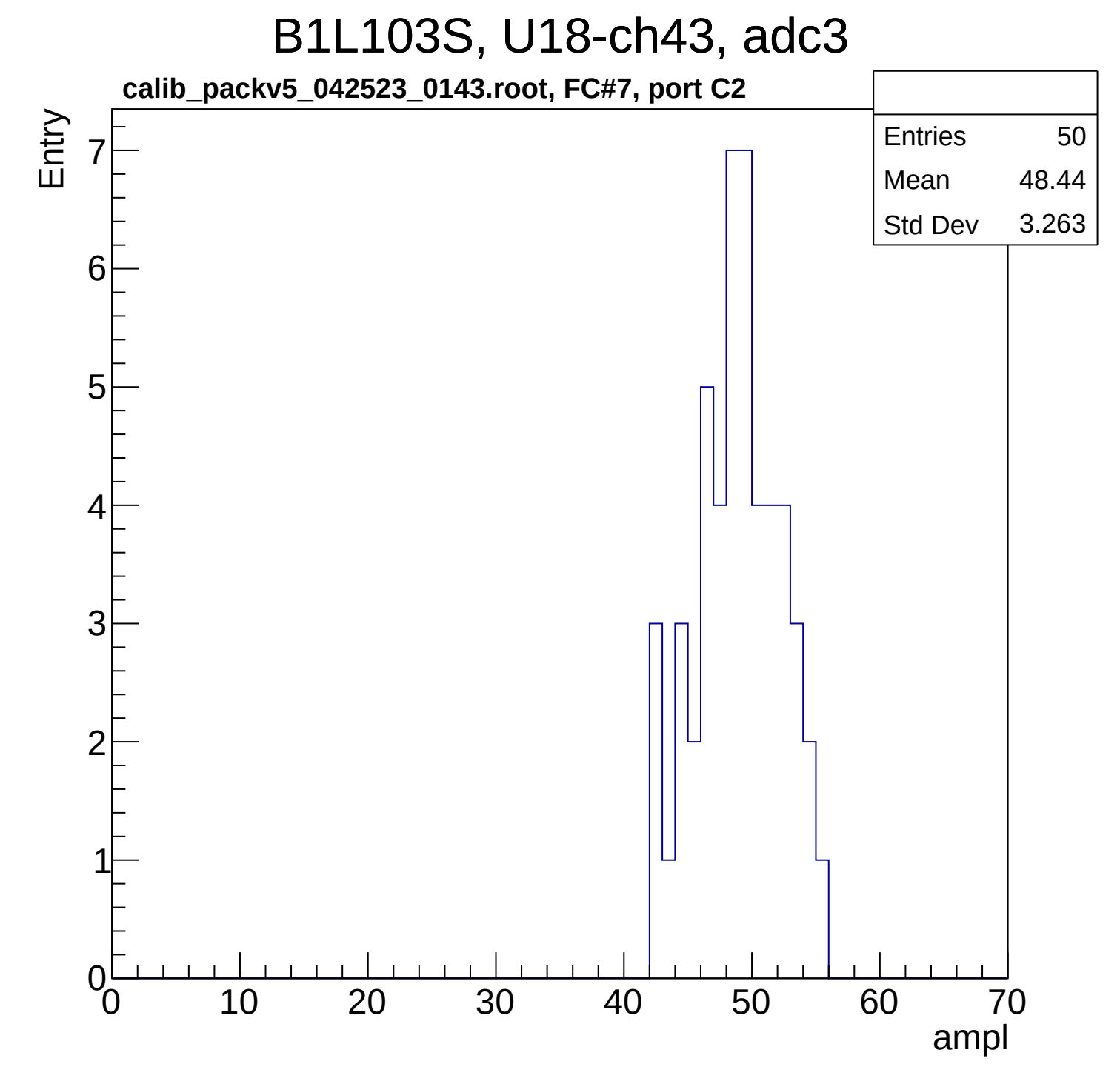
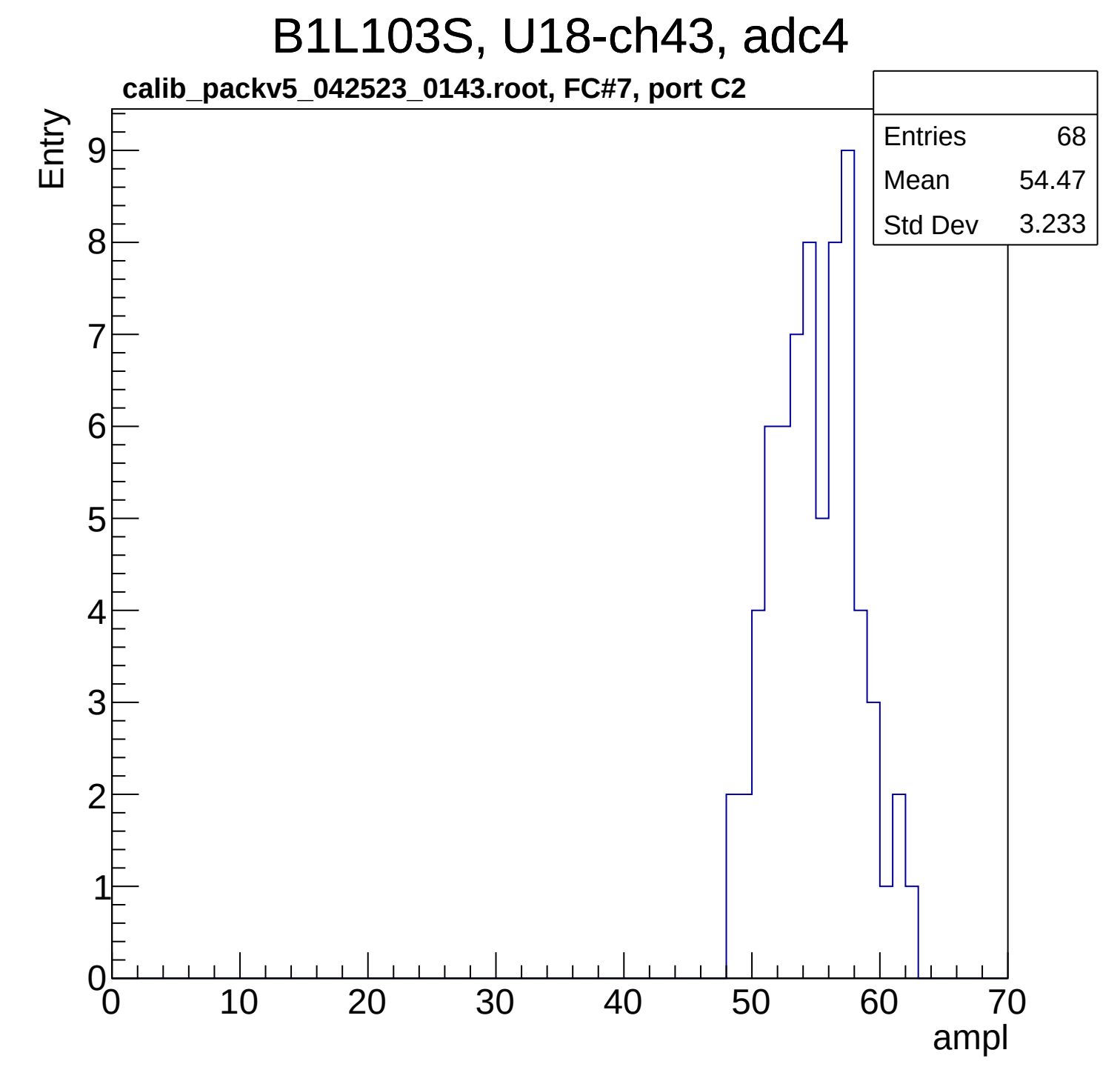
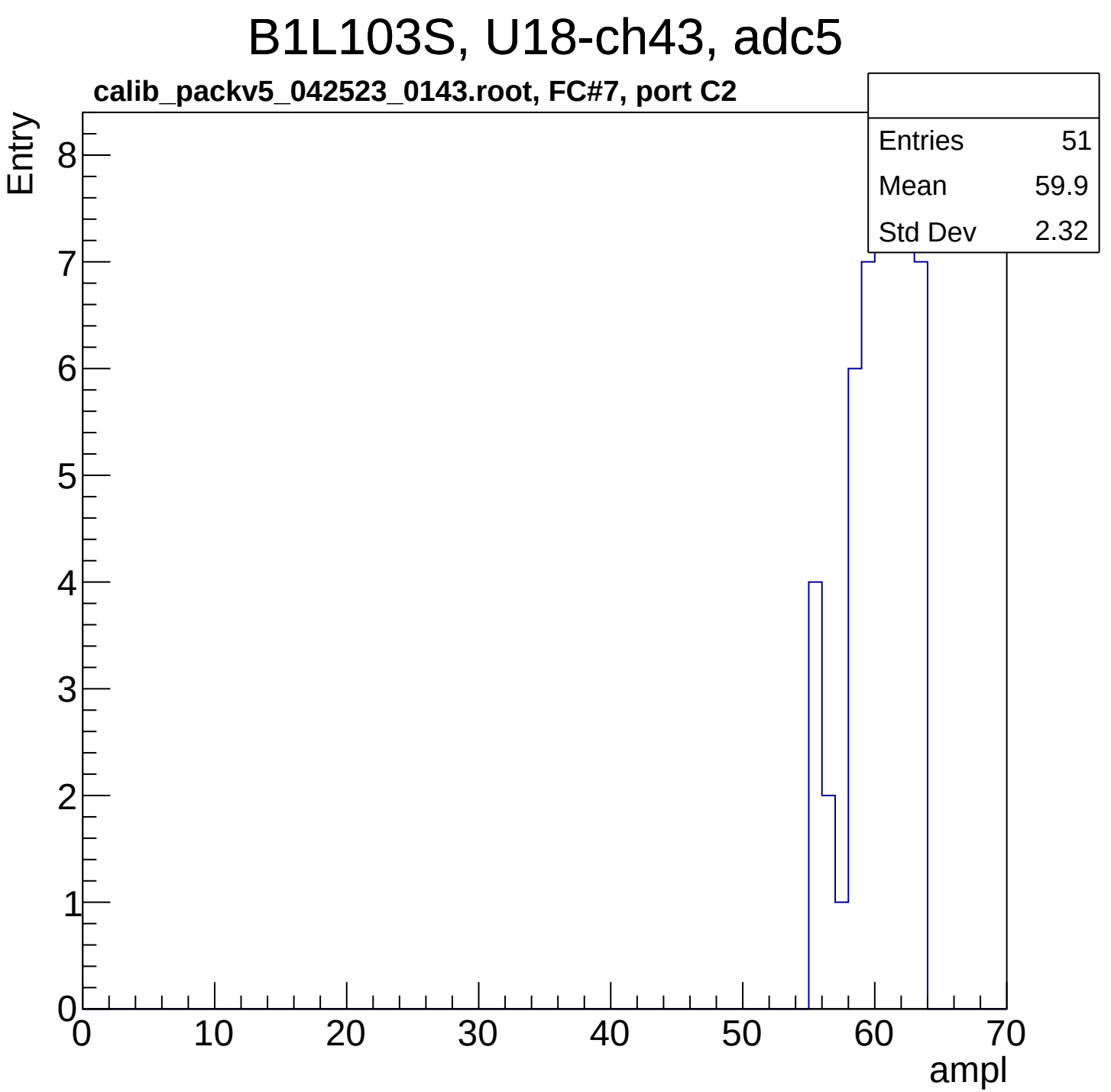

B1L103S, U18-ch43, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 42.52
Std Dev 3.775
Gaus mean : 43.1706
Gaus Width: 3.4596
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch43, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 50
Mean 48.44
Std Dev 3.263
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch43, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 54.47
Std Dev 3.233
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch43, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 51
Mean 59.9
Std Dev 2.32
Entry
ampl
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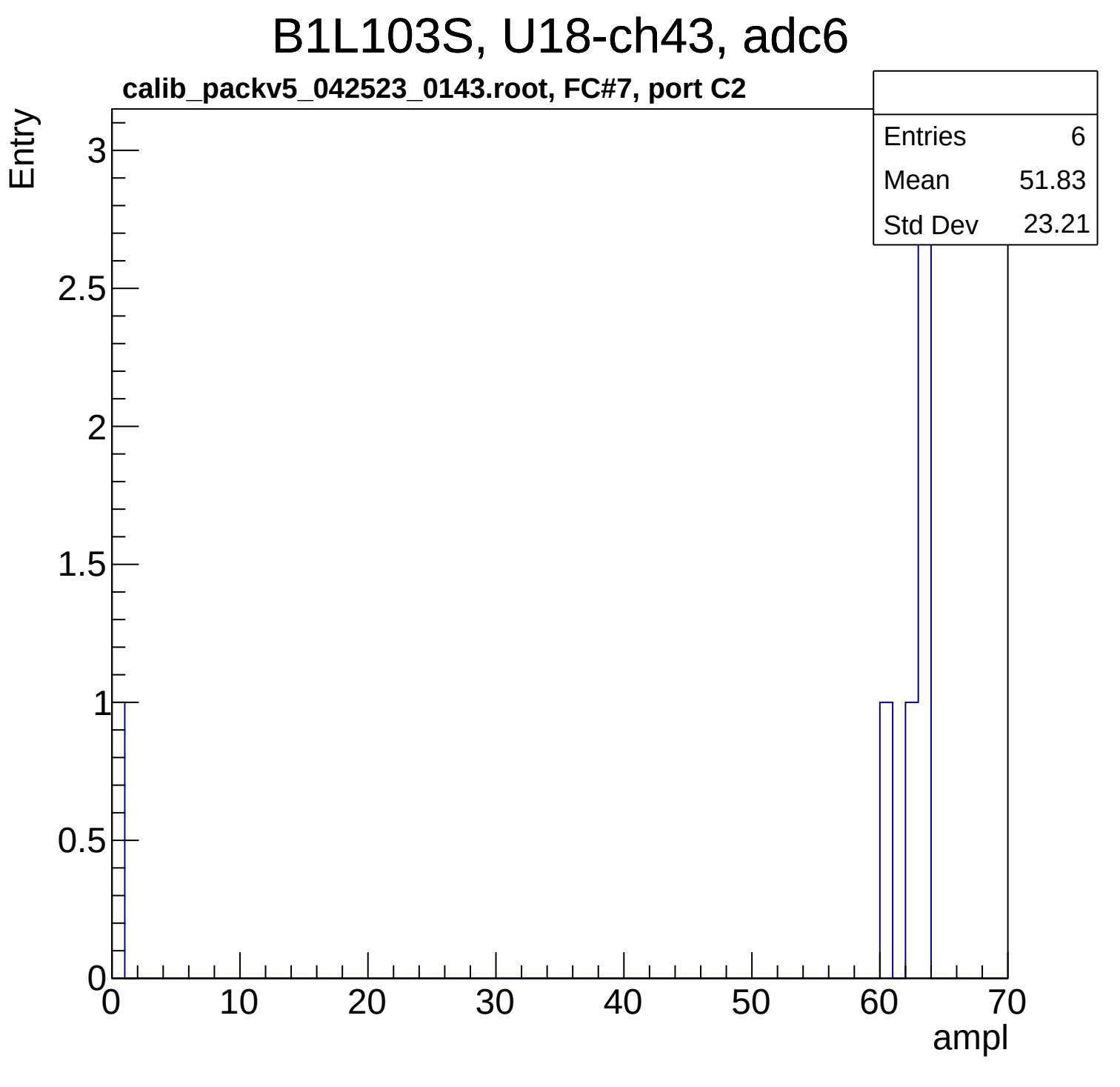
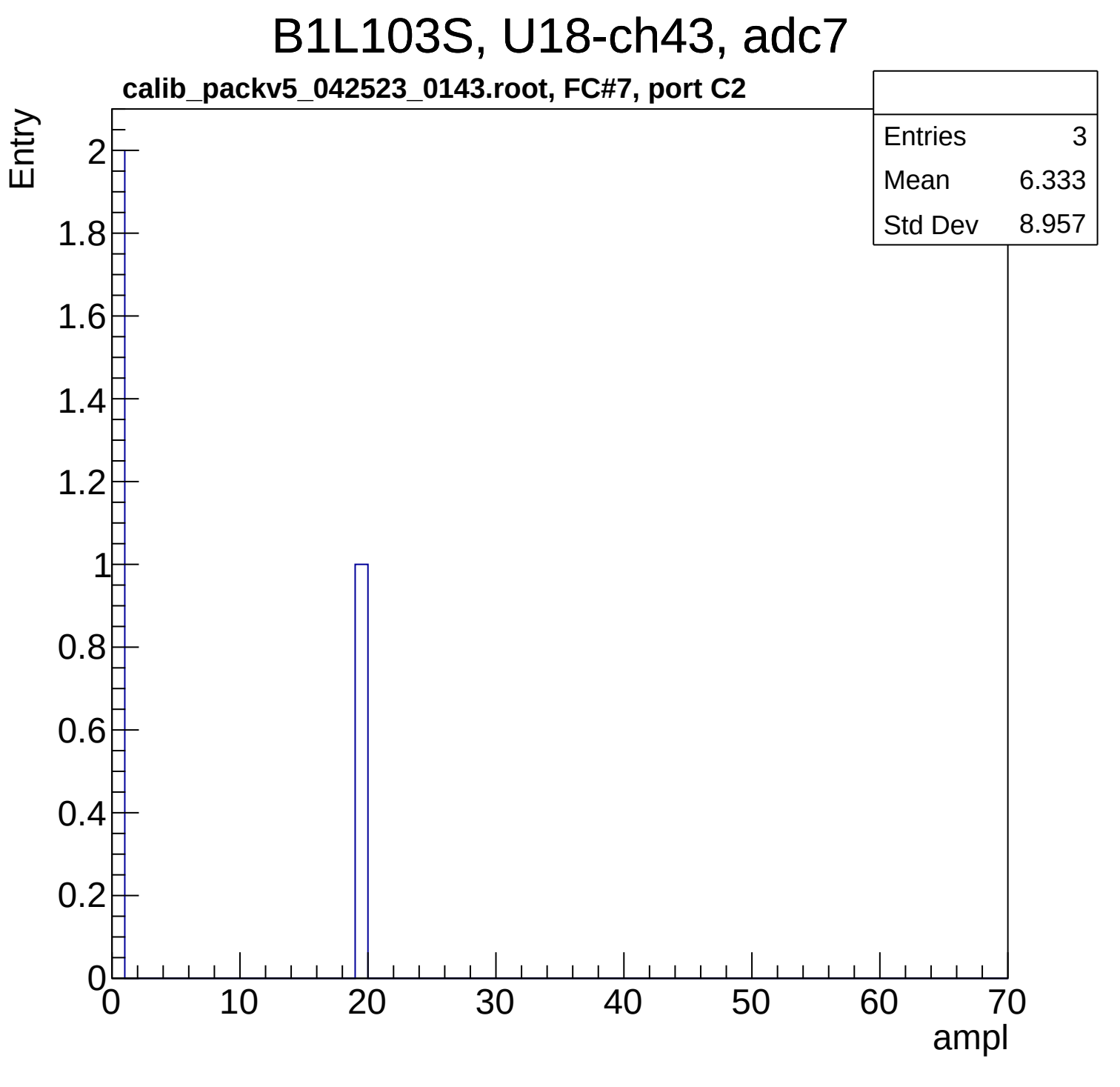
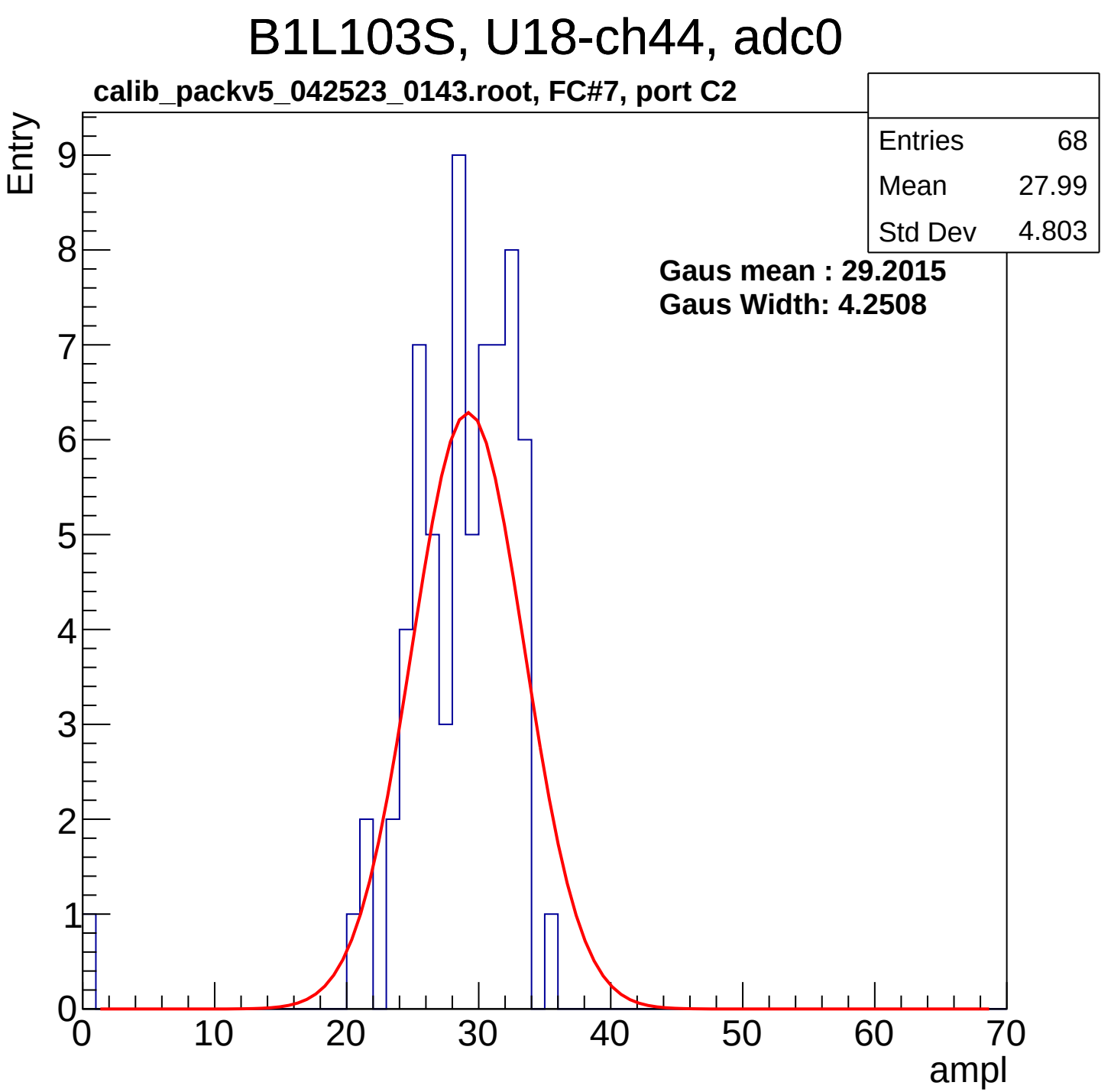
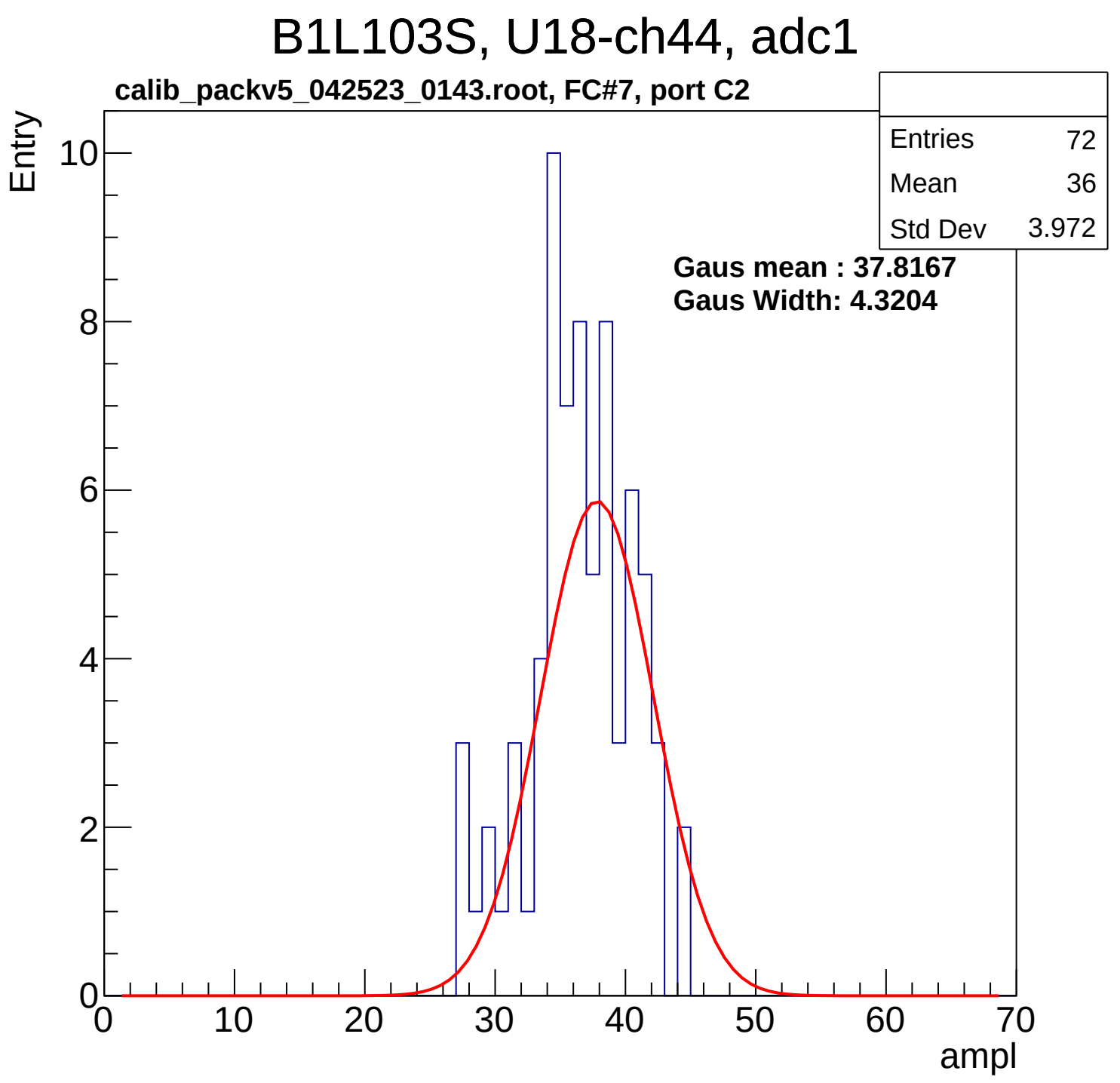
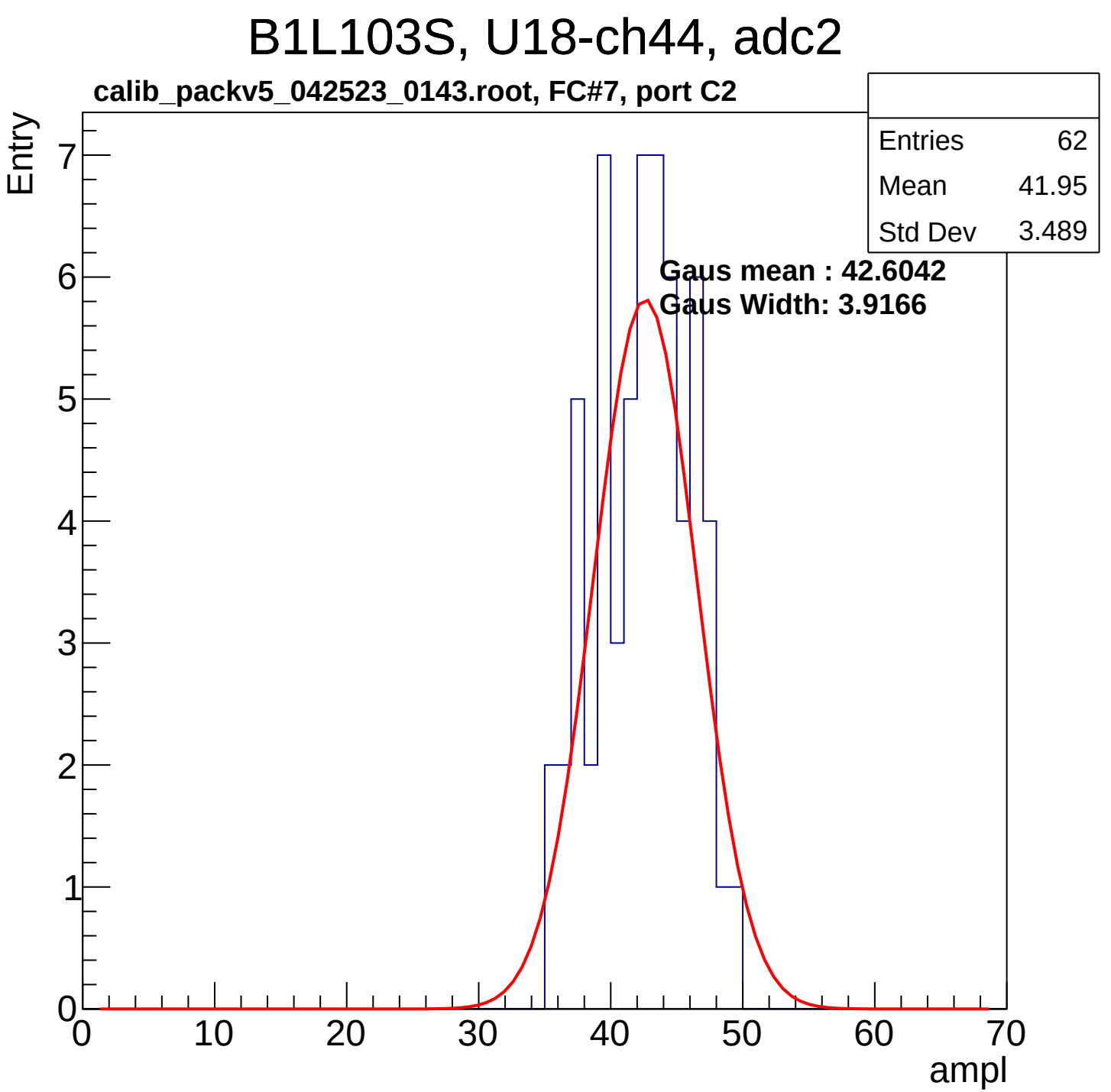
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

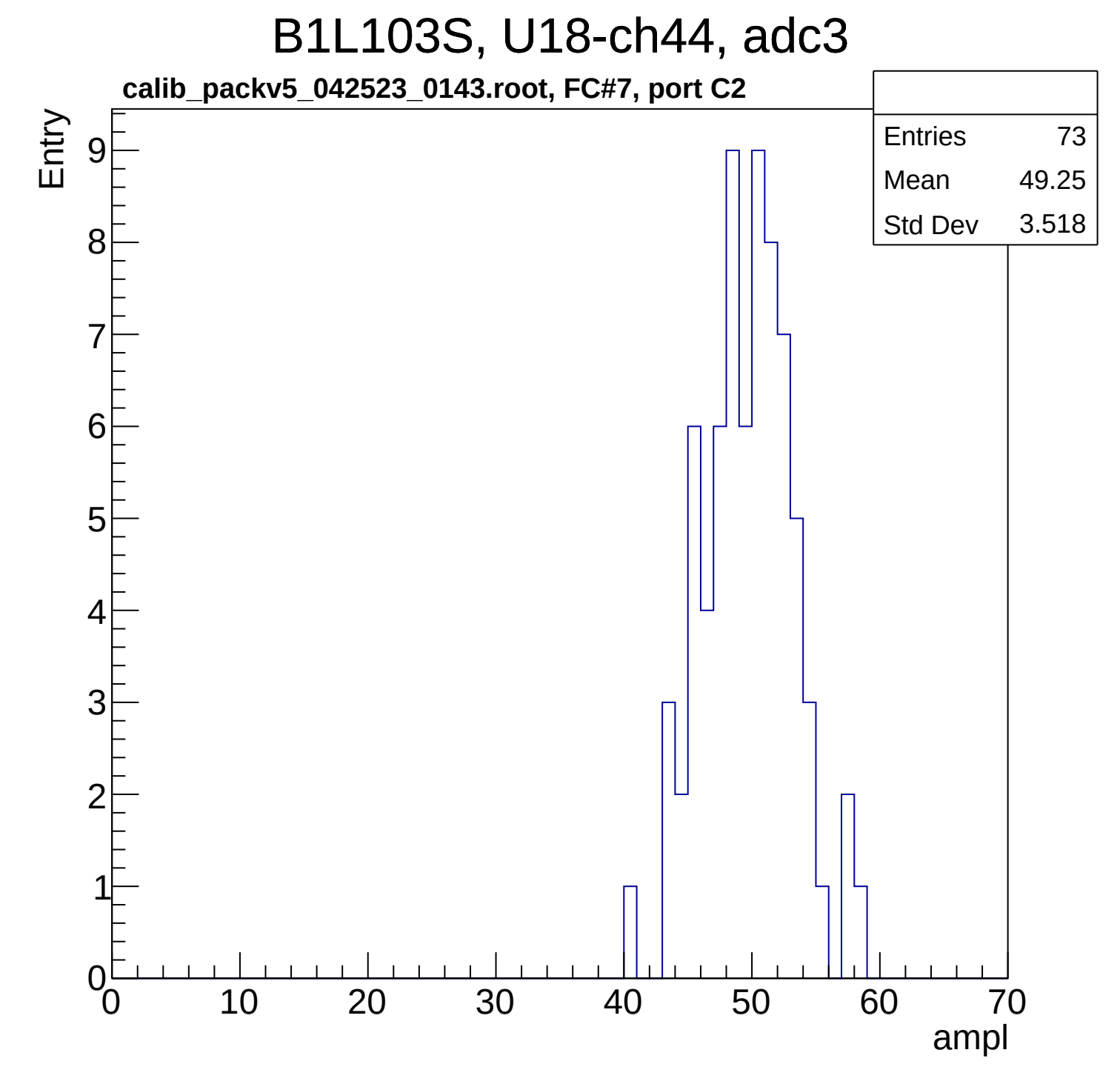

B1L103S, U18-ch43, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 6
Mean 51.83
Std Dev 23.21
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

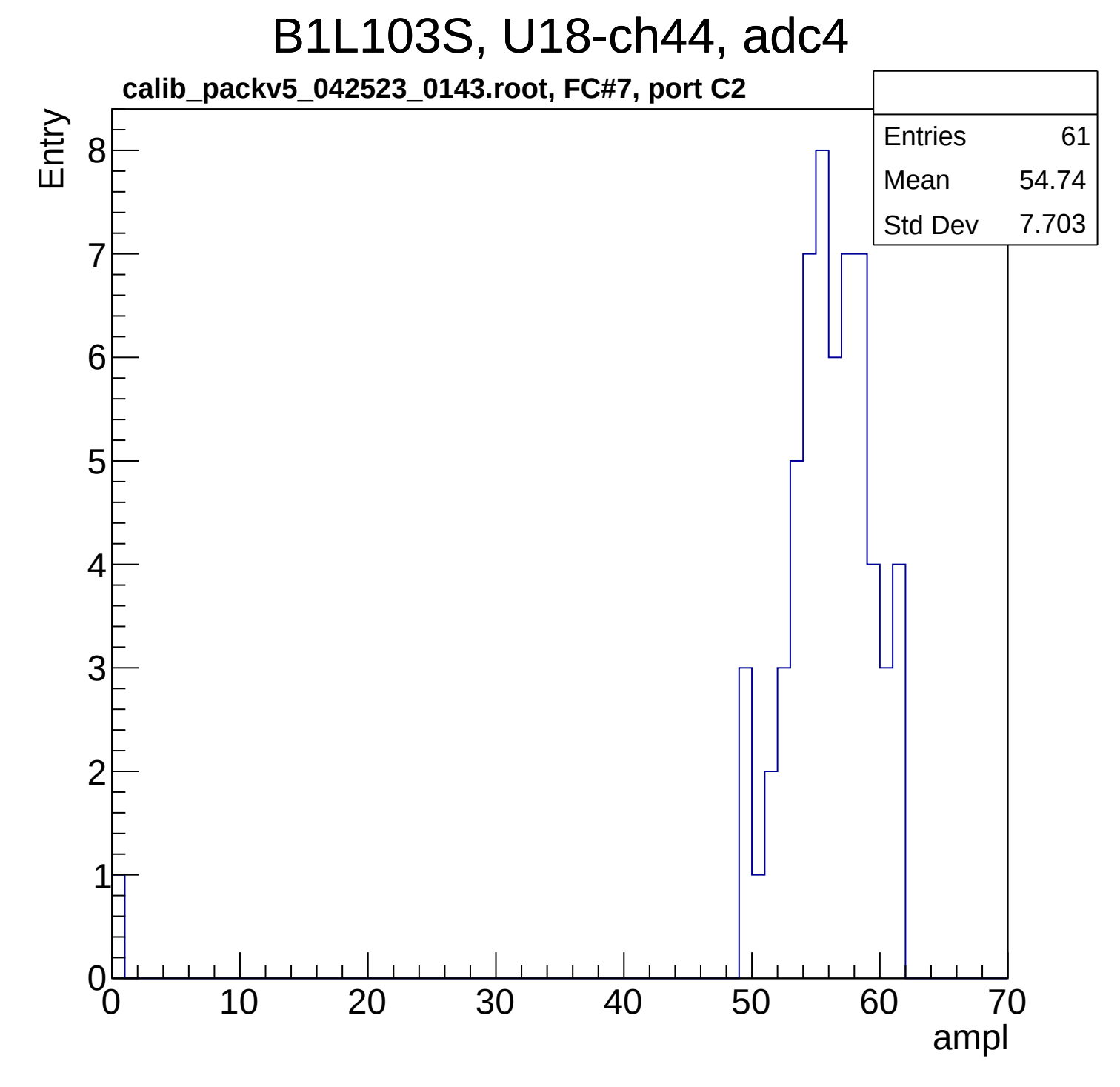

B1L103S, U18-ch43, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 6.333
Std Dev 8.957
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U18-ch44, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 27.99
Std Dev 4.803
Gaus mean : 29.2015
Gaus Width: 4.2508
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch44, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 72
Mean 36
Std Dev 3.972
Gaus mean : 37.8167
Gaus Width: 4.3204
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch44, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 62
Mean 41.95
Std Dev 3.489
Gaus mean : 42.6042
Gaus Width: 3.9166
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch44, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 73
Mean 49.25
Std Dev 3.518
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch44, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 61
Mean 54.74
Std Dev 7.703
Entry
ampl
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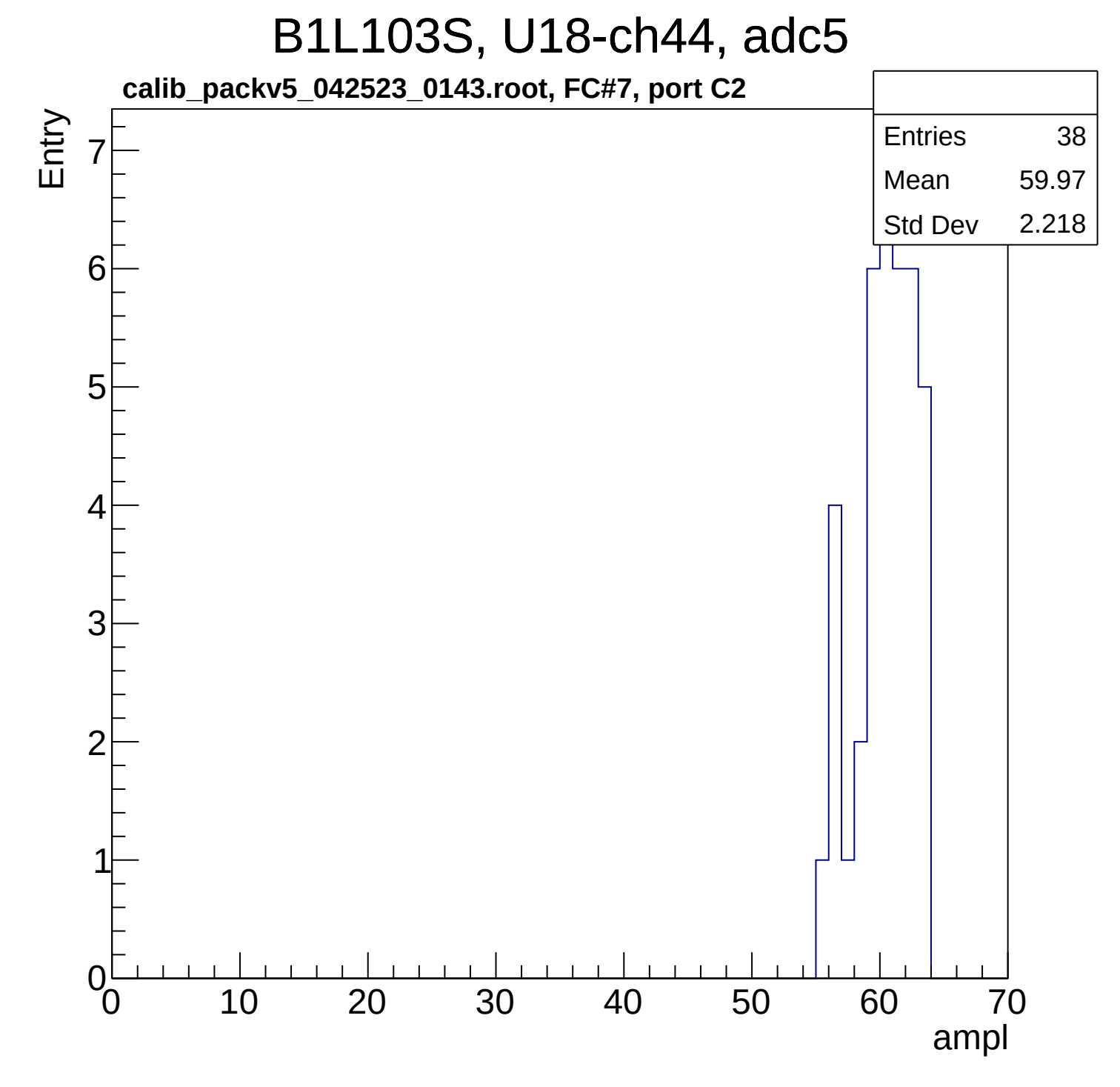
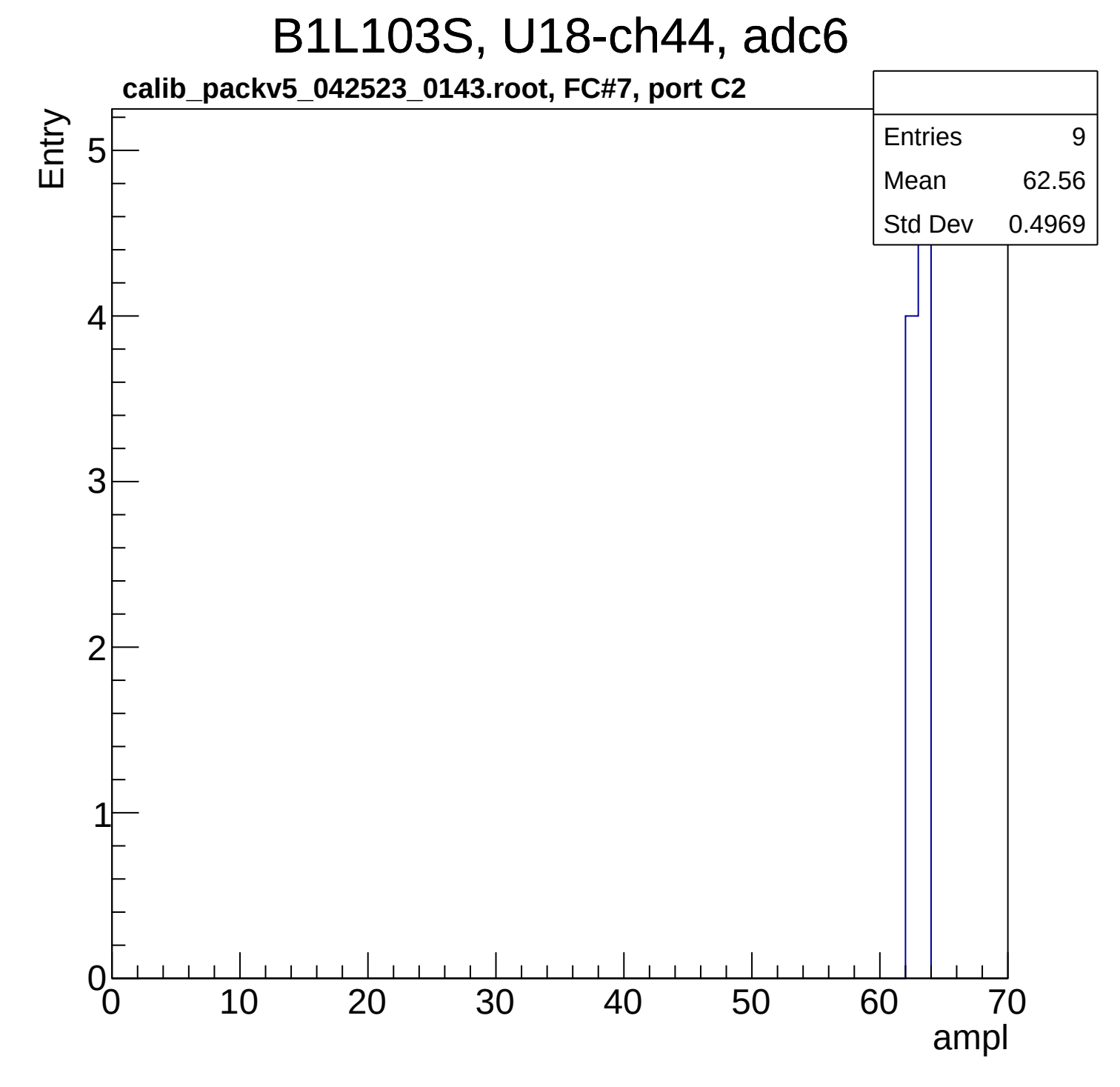
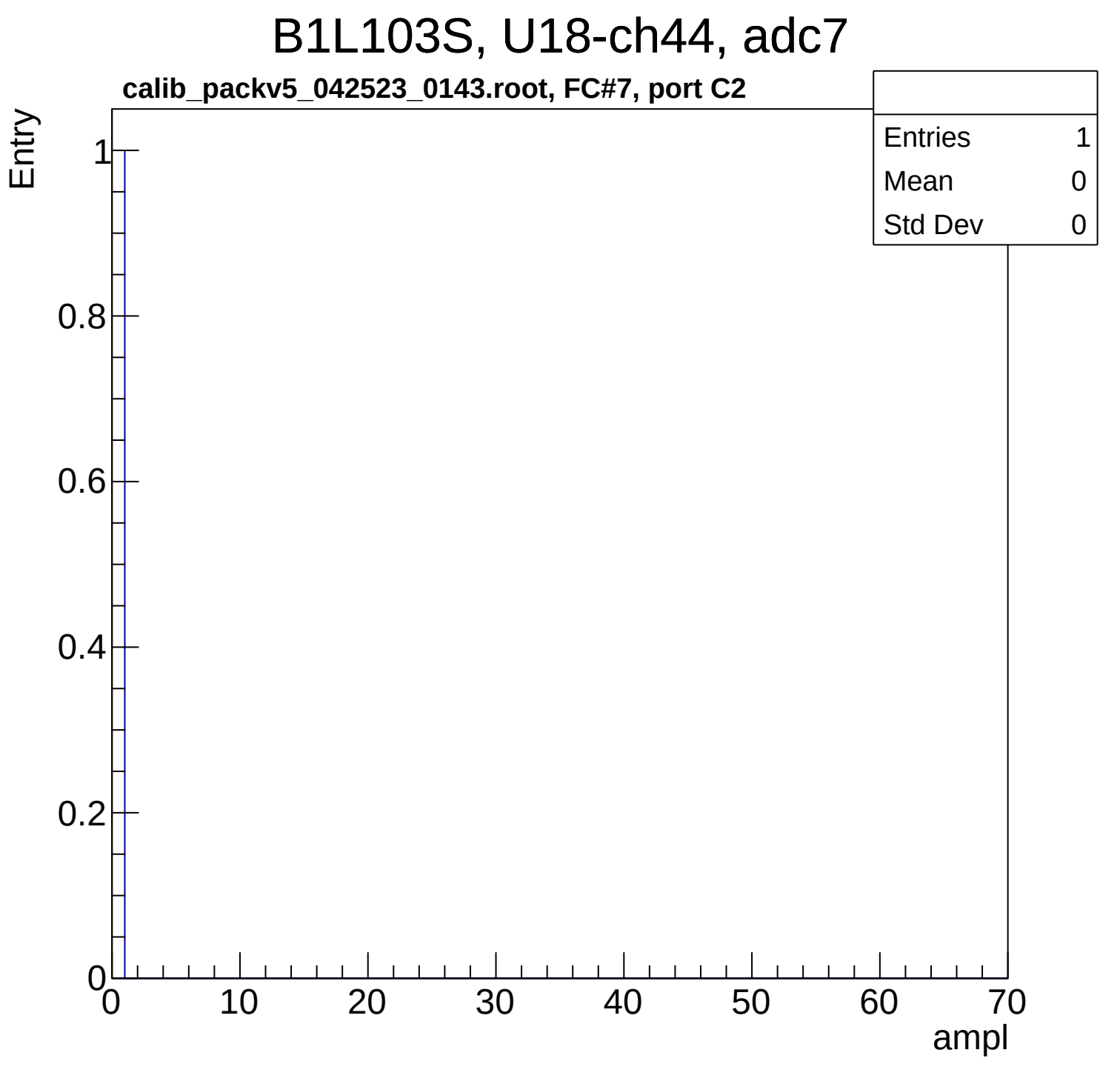
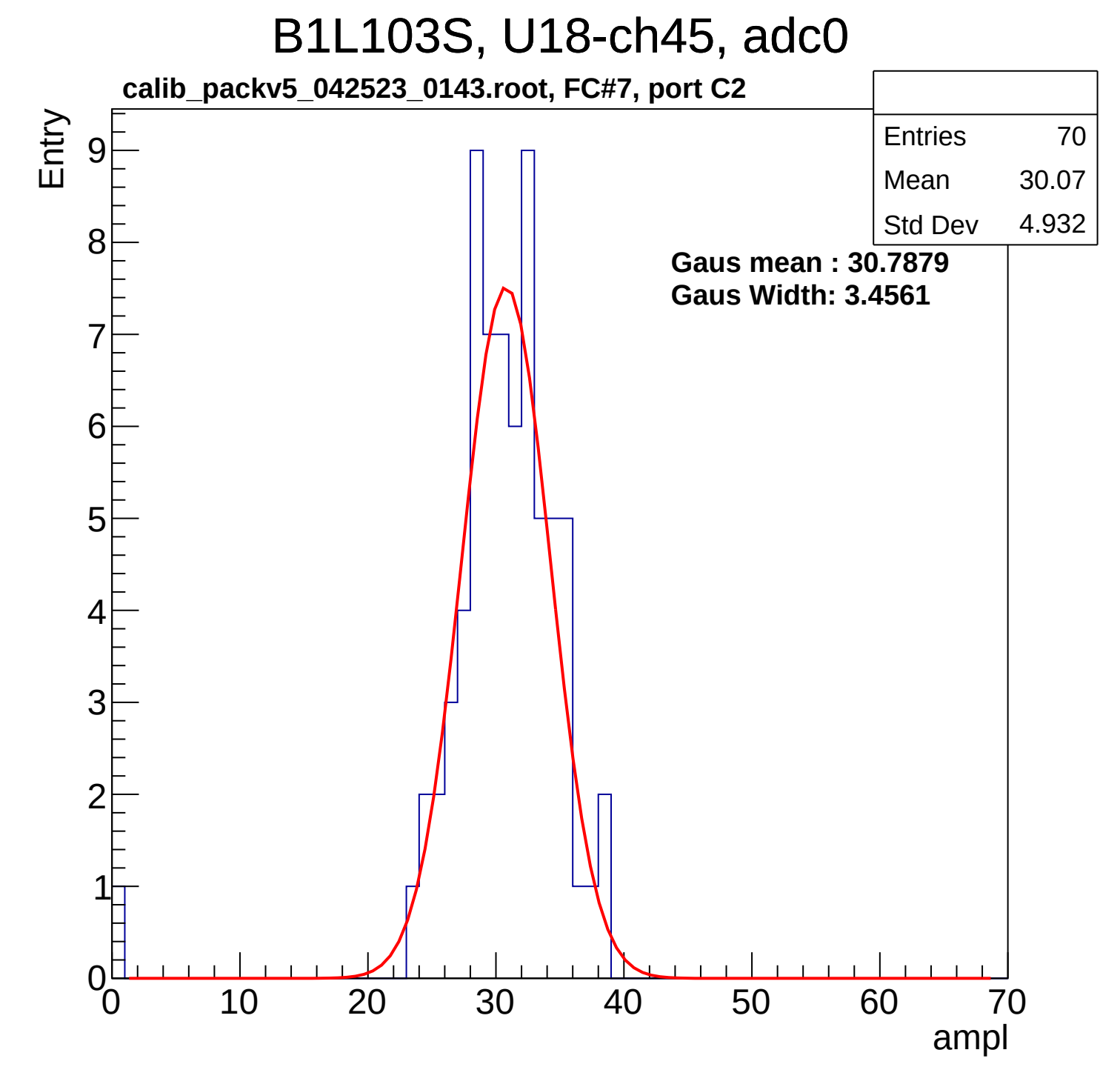
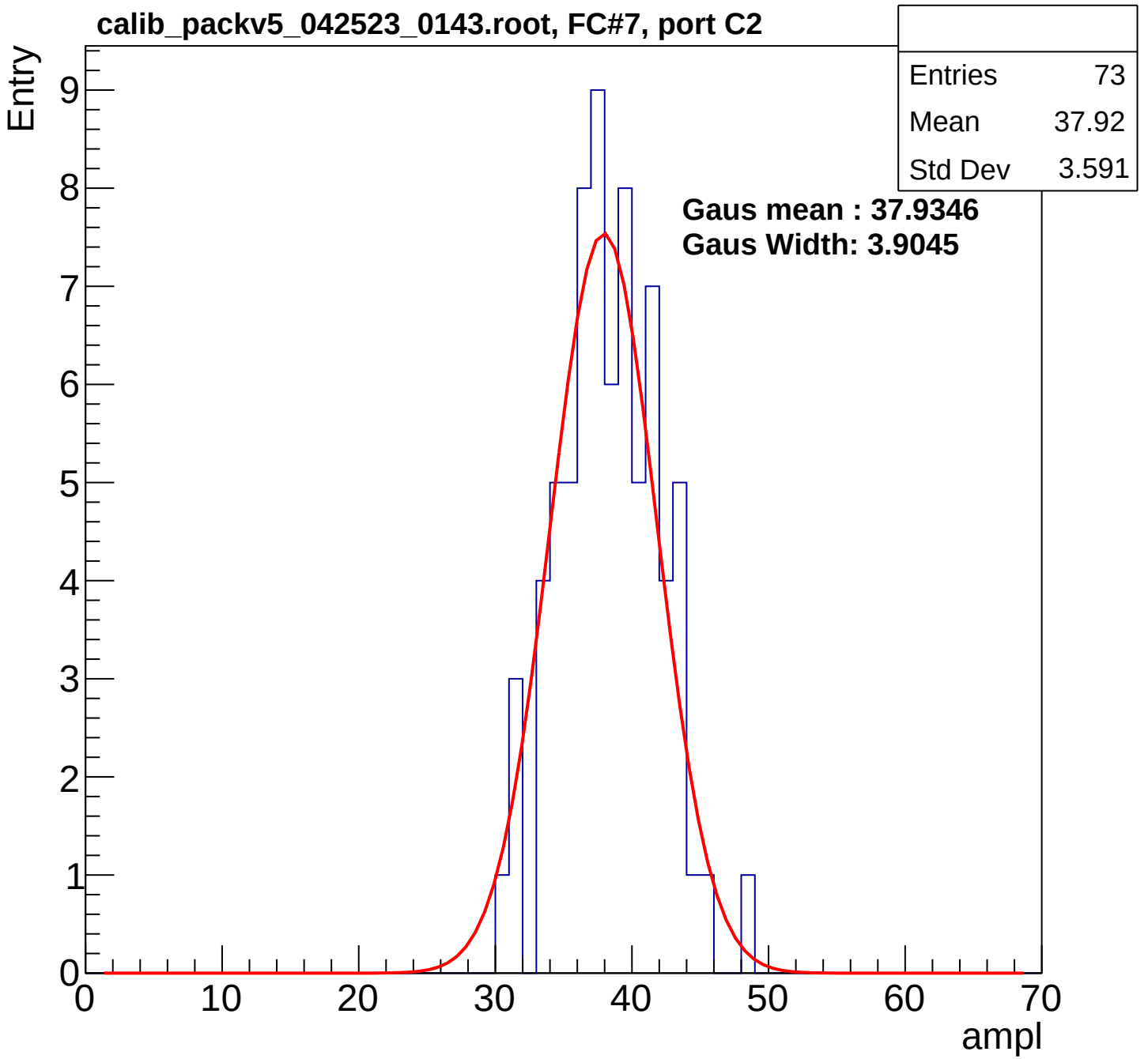
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch44, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 38
Mean 59.97
Std Dev 2.218
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch44, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 9
Mean 62.56
Std Dev 0.4969
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U18-ch44, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch45, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 30.07
Std Dev 4.932
Gaus mean : 30.7879
Gaus Width: 3.4561
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch45, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 73
Mean 37.92
Std Dev 3.591
Gaus mean : 37.9346
Gaus Width: 3.9045
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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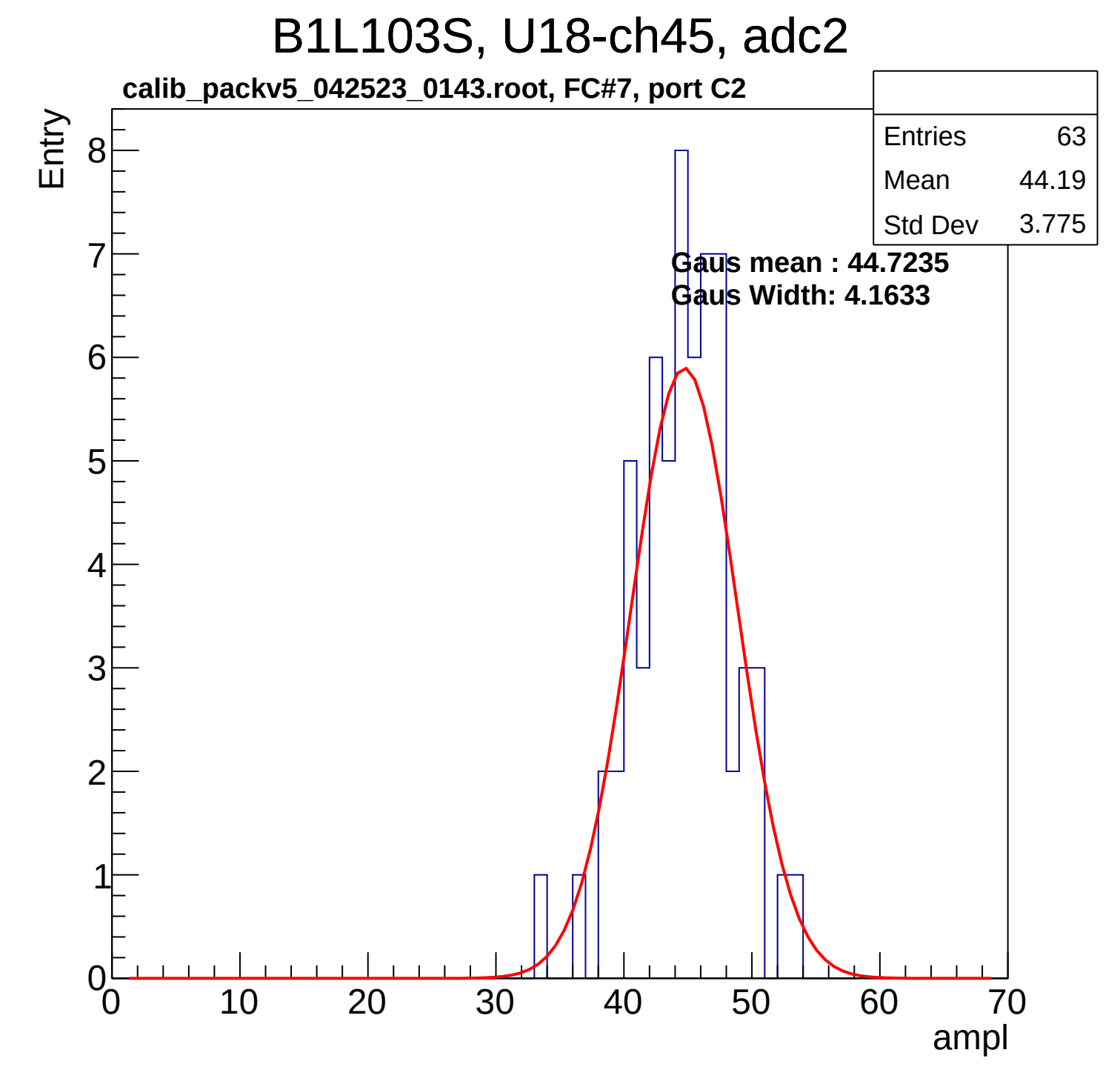
B1L103S, U18-ch45, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 44.19
Std Dev 3.775
Gaus mean : 44.7235
Gaus Width: 4.1633
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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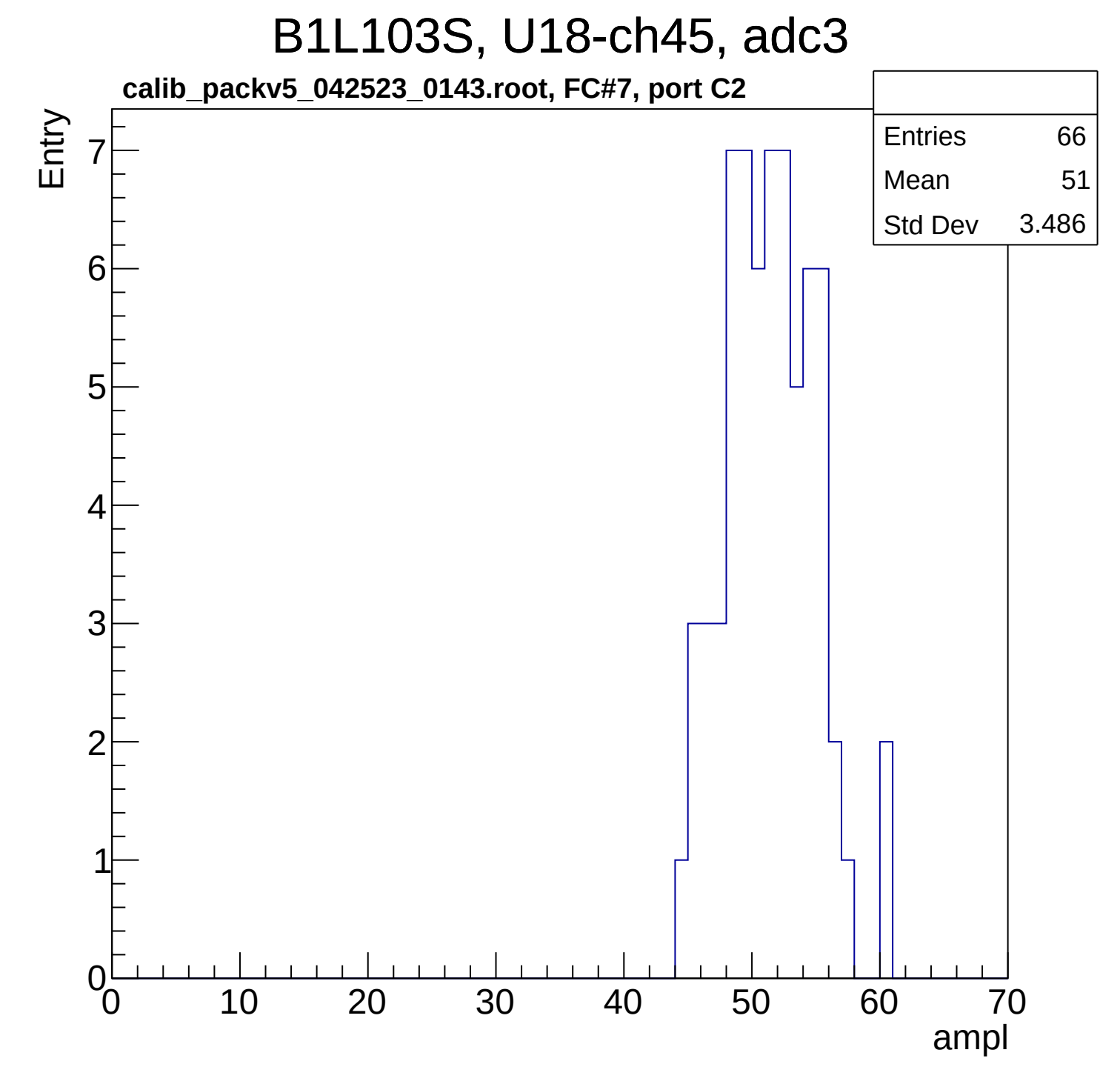
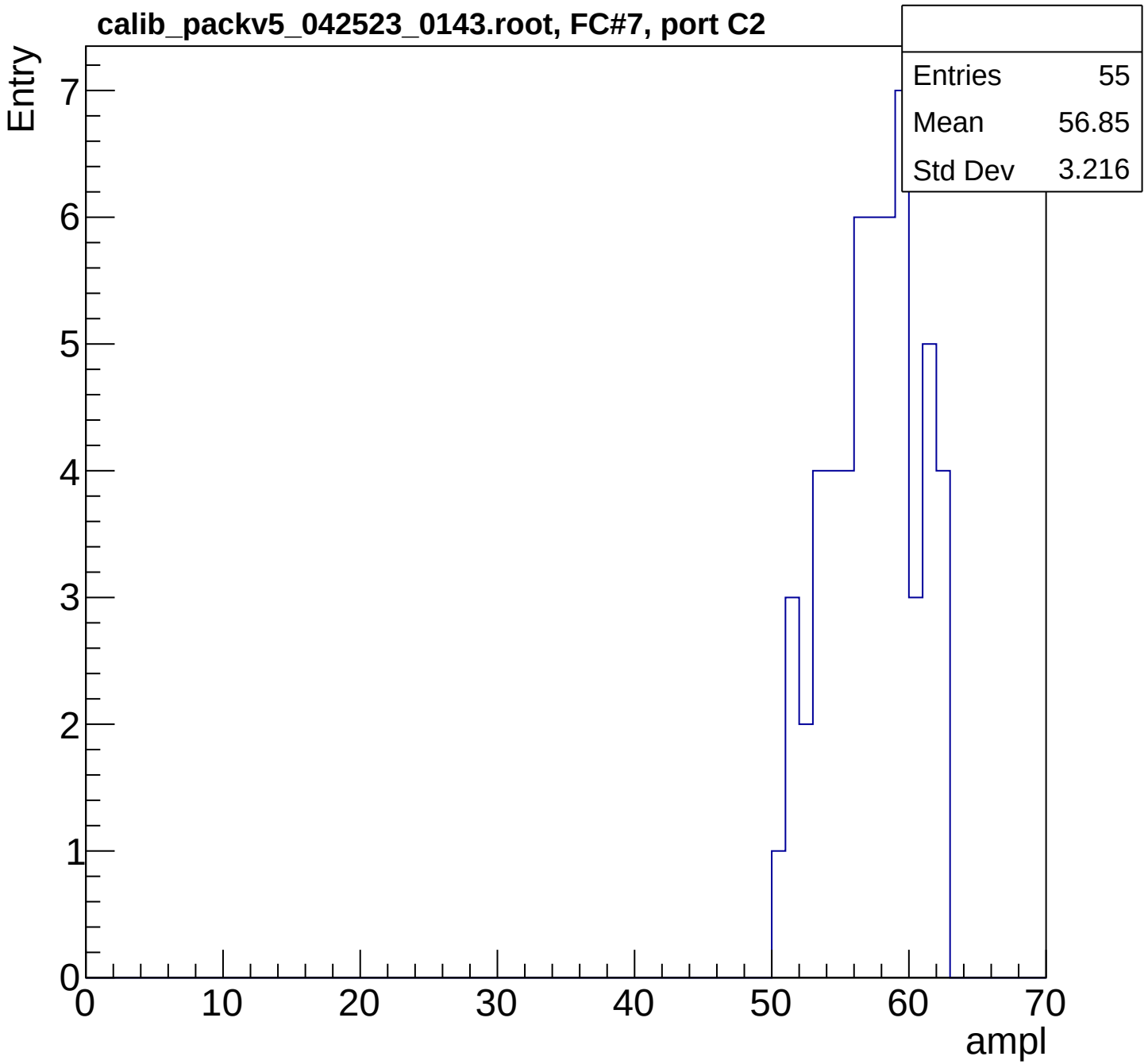
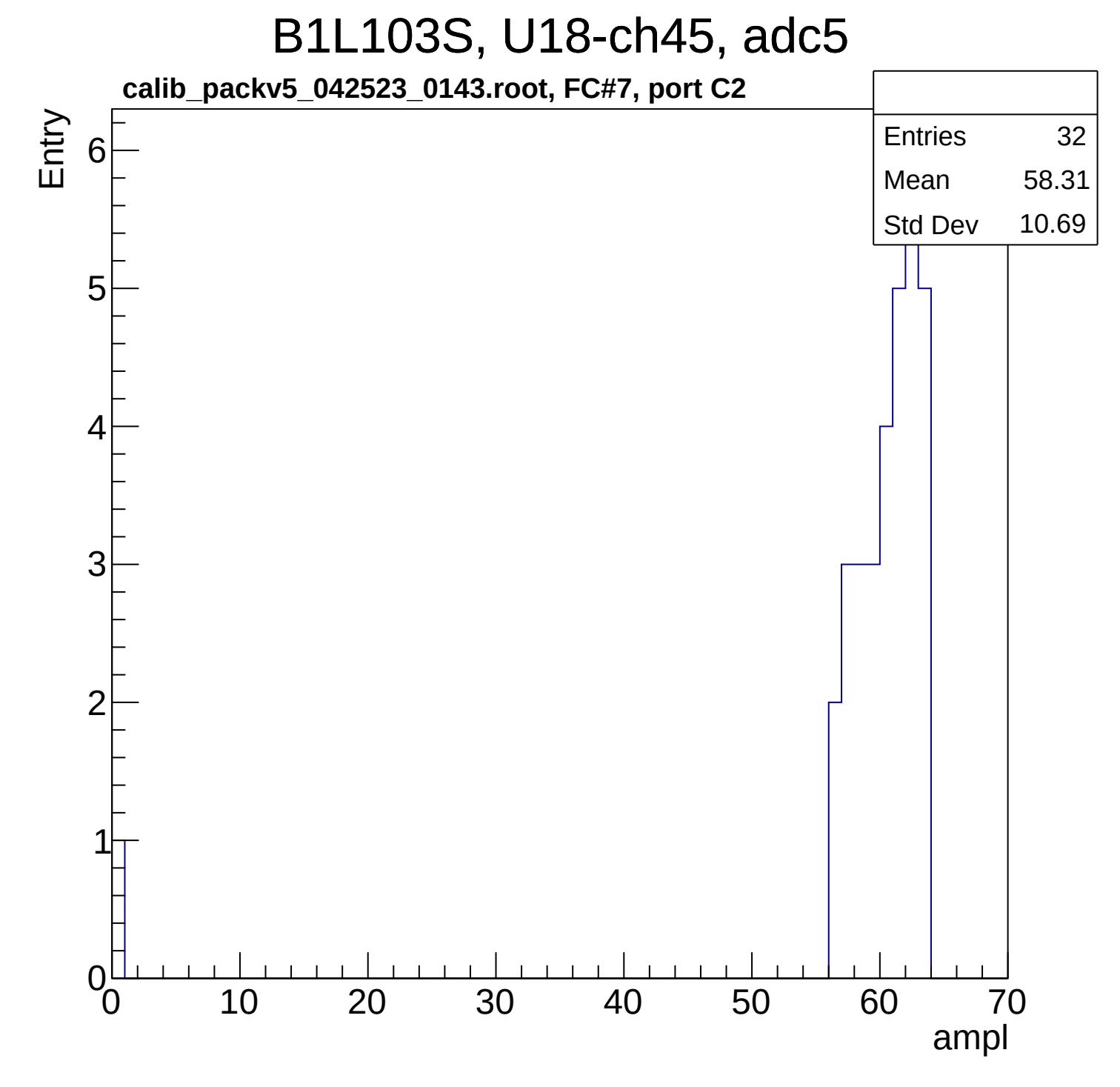
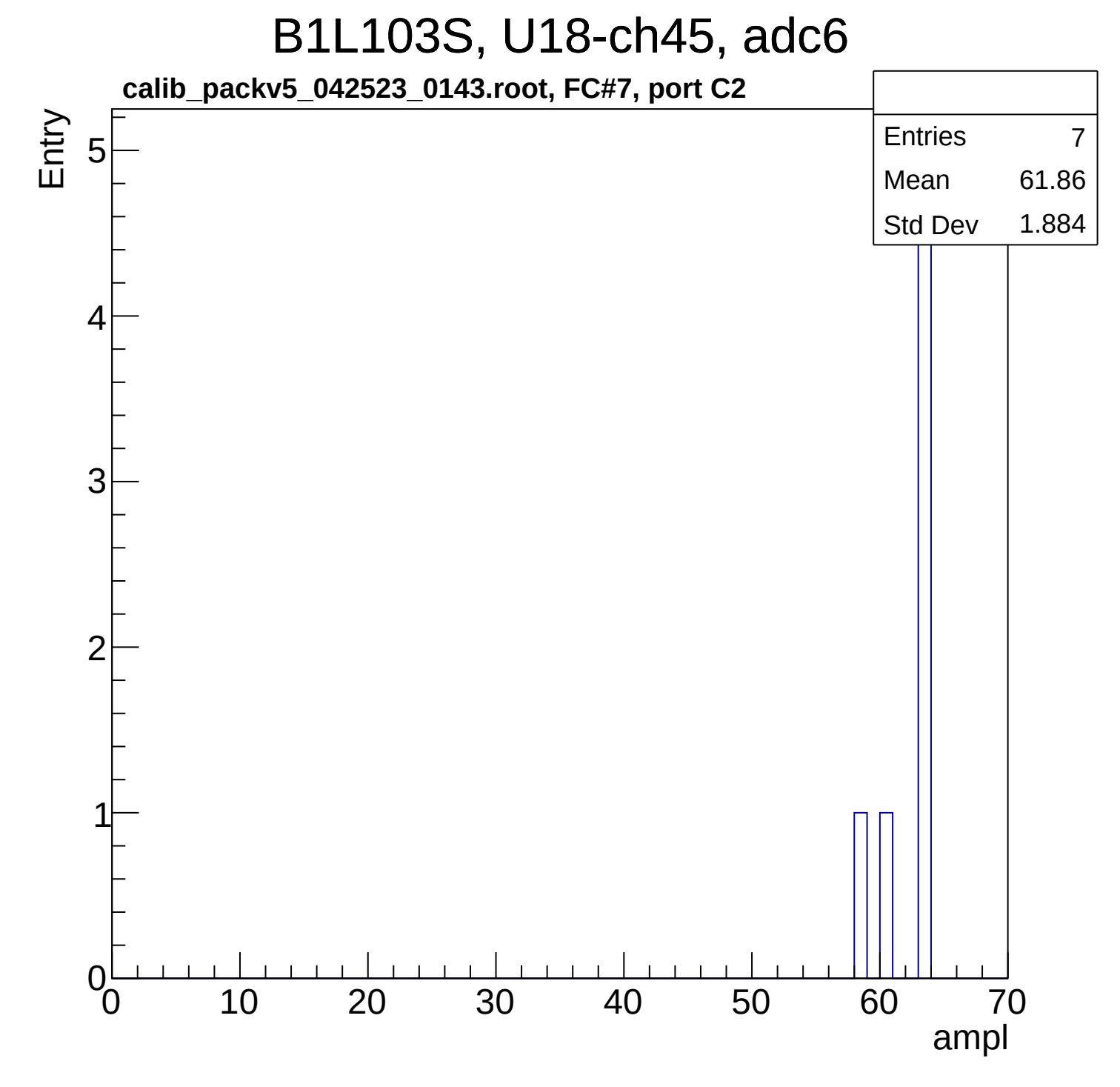
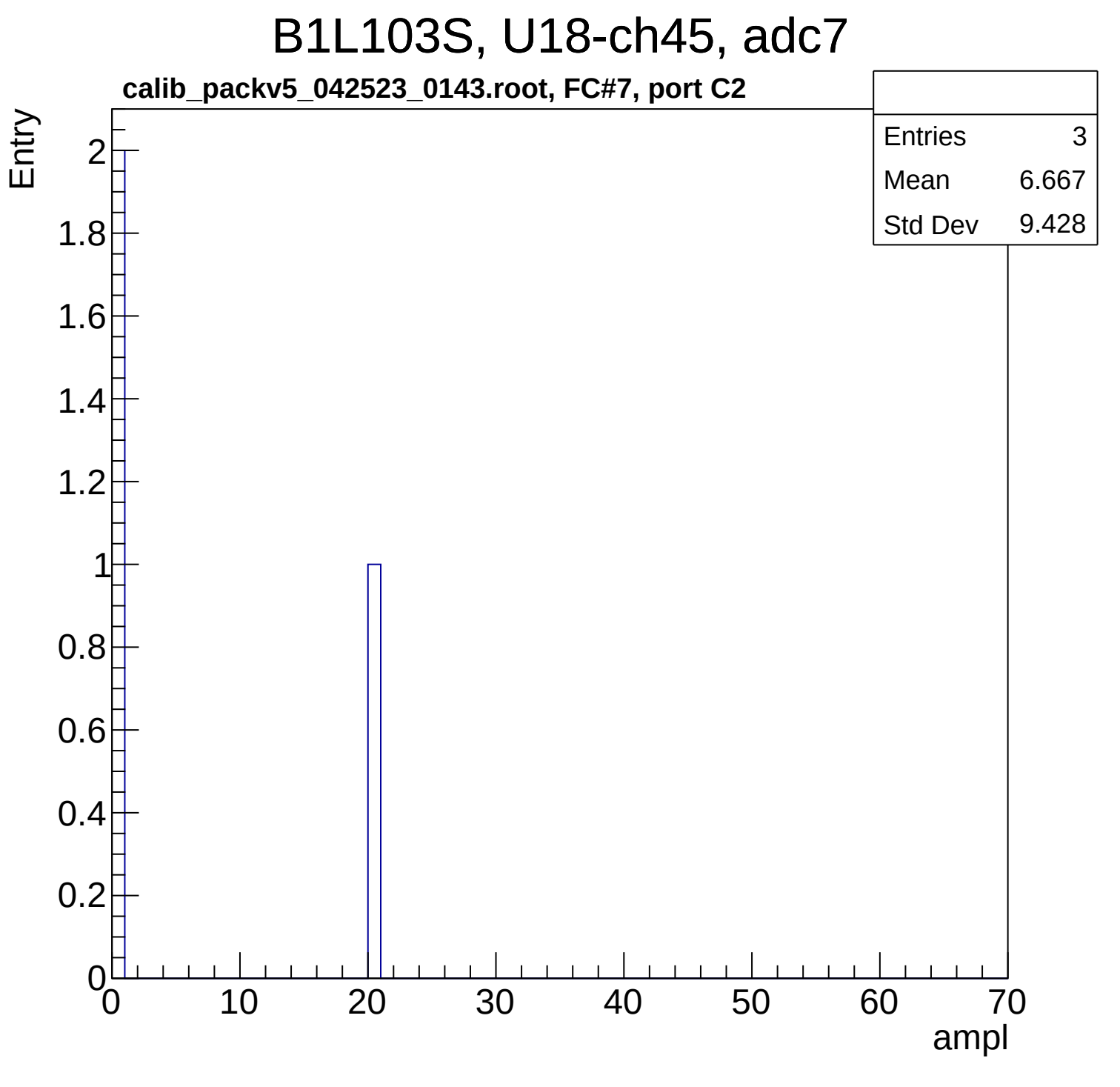
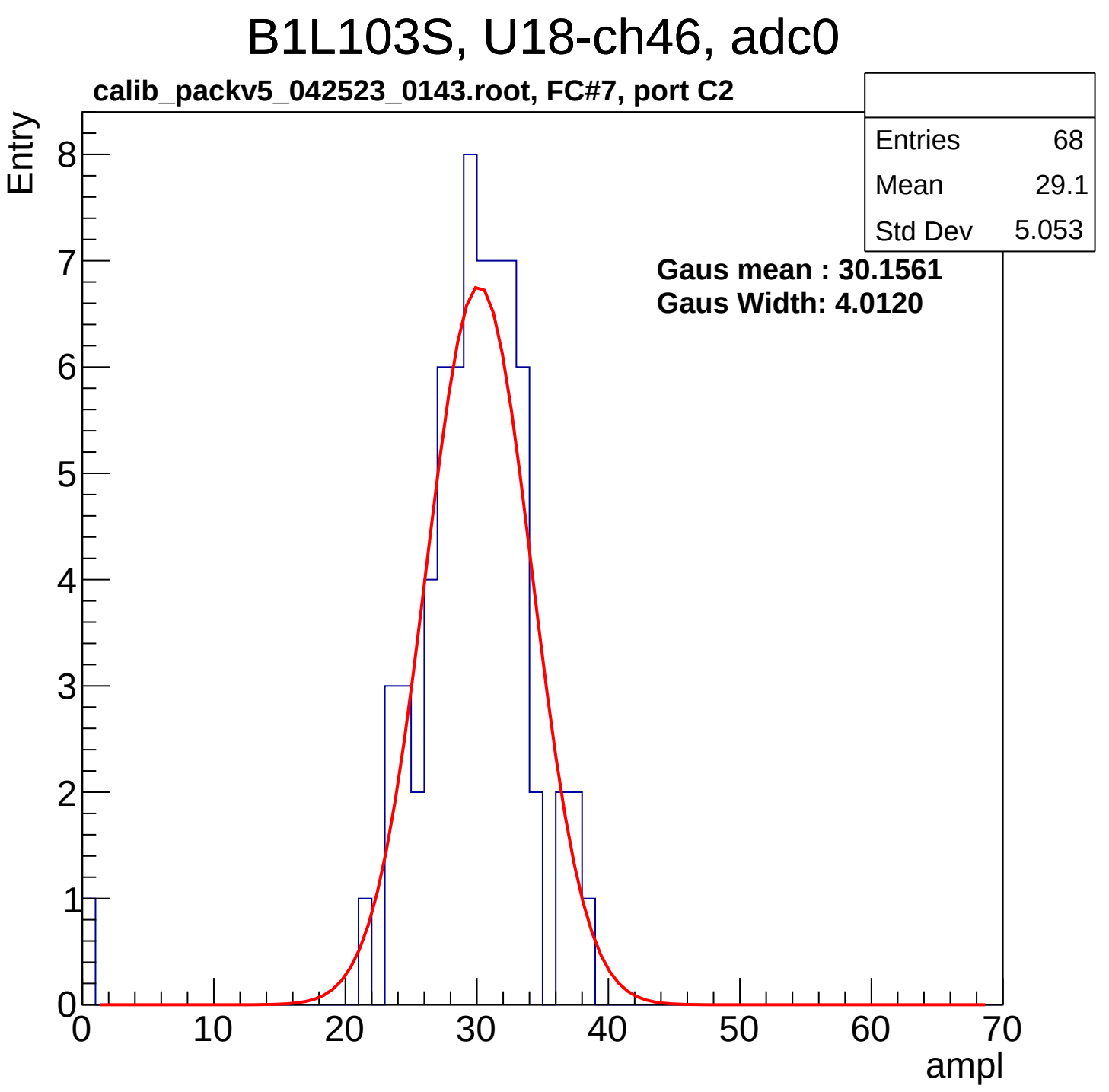

B1L103S, U18-ch45, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 51
Std Dev 3.486
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

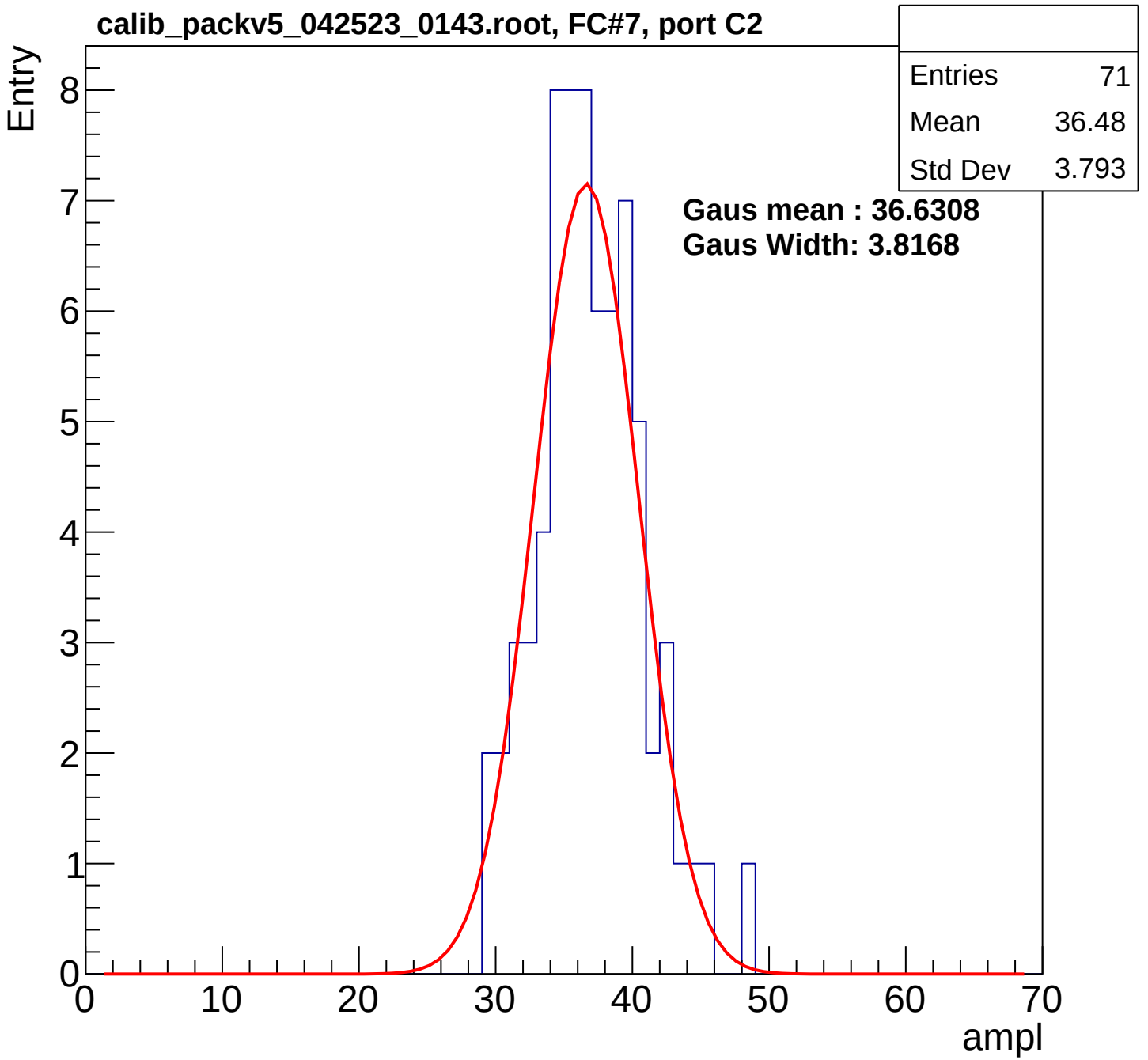

B1L103S, U18-ch45, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 56.85
Std Dev 3.216
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch45, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 32
Mean 58.31
Std Dev 10.69
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch45, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 7
Mean 61.86
Std Dev 1.884
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch45, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 6.667
Std Dev 9.428
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U18-ch46, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 29.1
Std Dev 5.053
Gaus mean : 30.1561
Gaus Width: 4.0120
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch46, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 71
Mean 36.48
Std Dev 3.793
Gaus mean : 36.6308
Gaus Width: 3.8168
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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20
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40
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60
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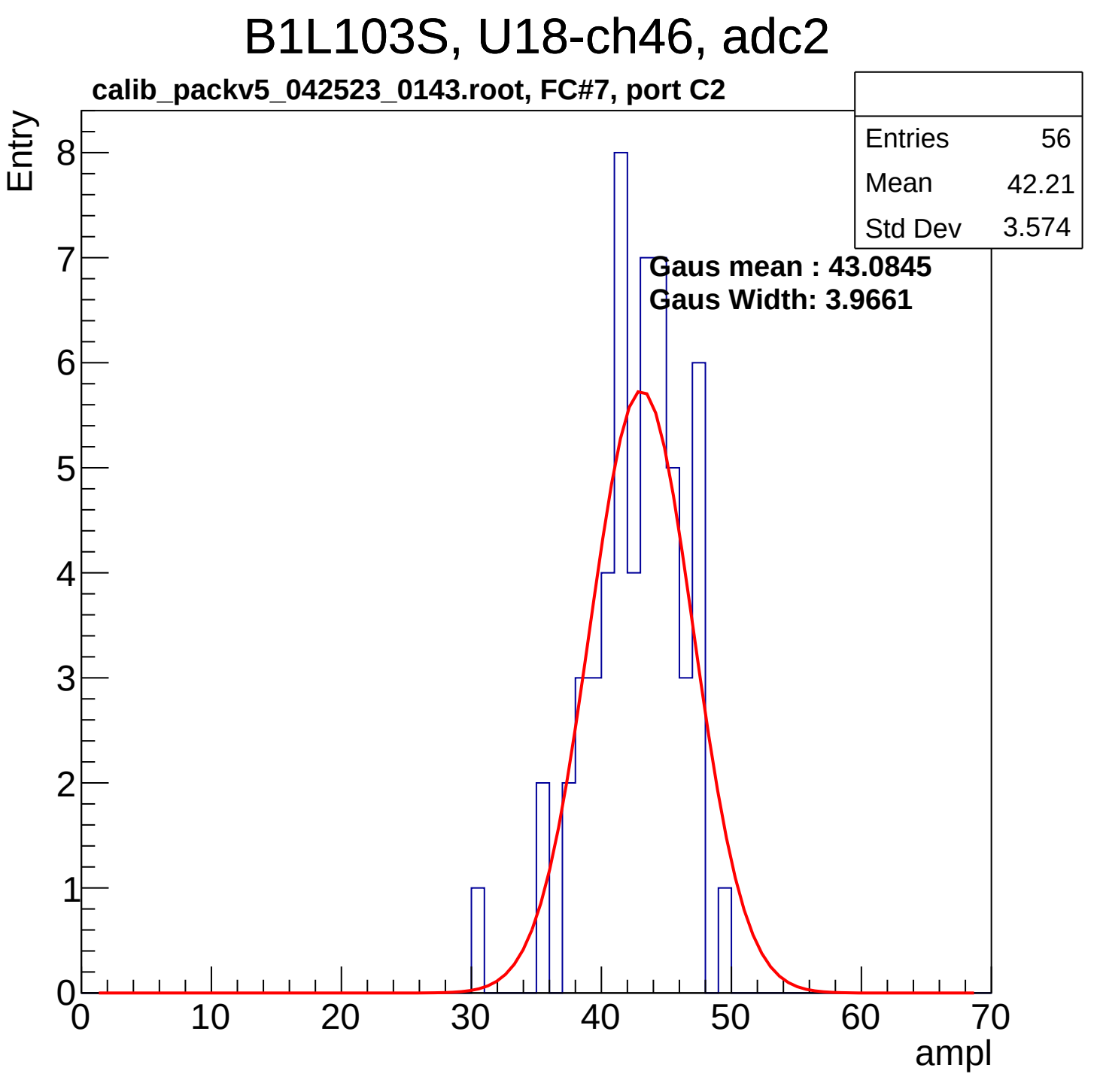
B1L103S, U18-ch46, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 42.21
Std Dev 3.574
Gaus mean : 43.0845
Gaus Width: 3.9661
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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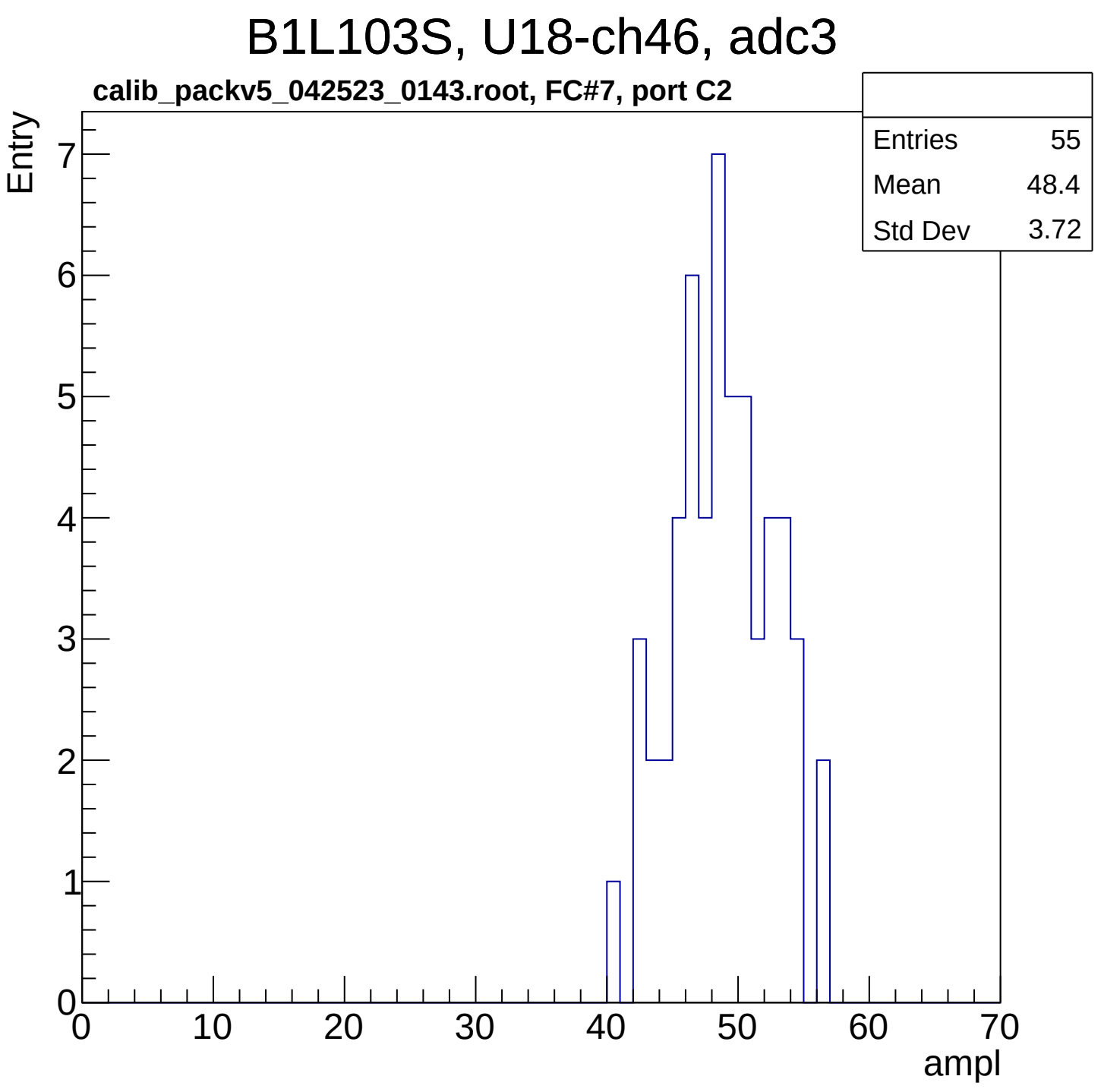
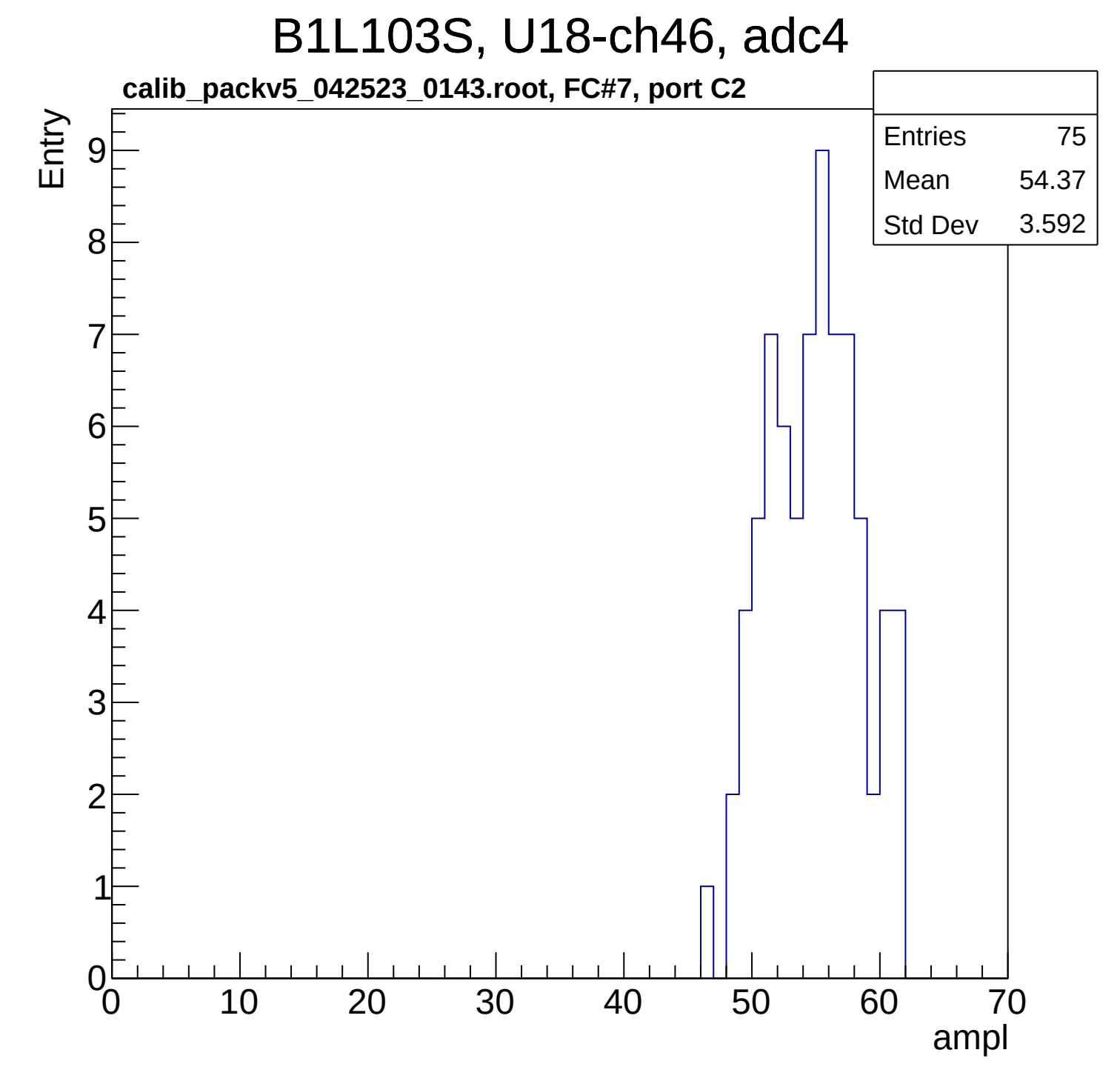

B1L103S, U18-ch46, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 48.4
Std Dev 3.72
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch46, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 75
Mean 54.37
Std Dev 3.592
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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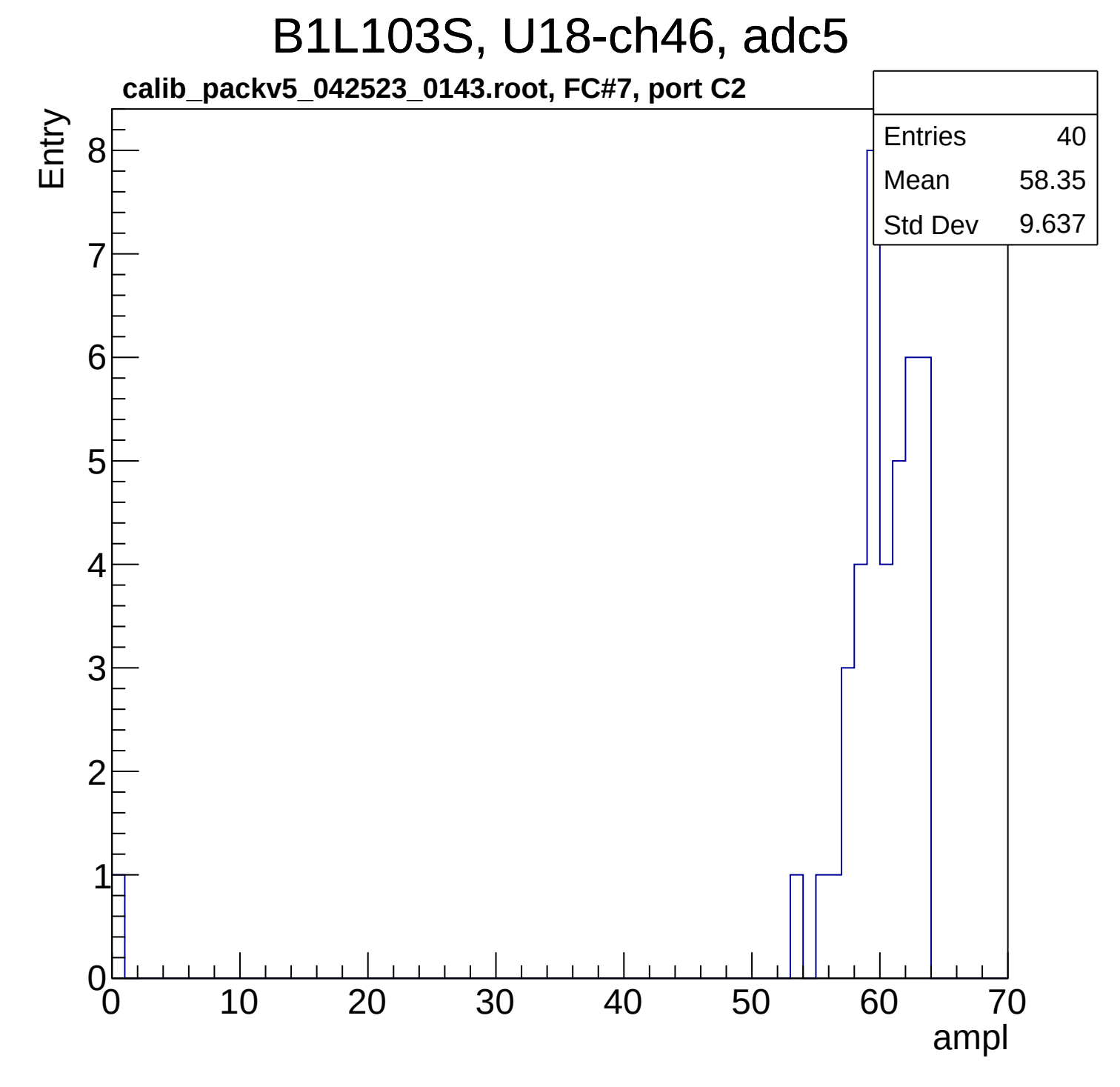
B1L103S, U18-ch46, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 40
Mean 58.35
Std Dev 9.637
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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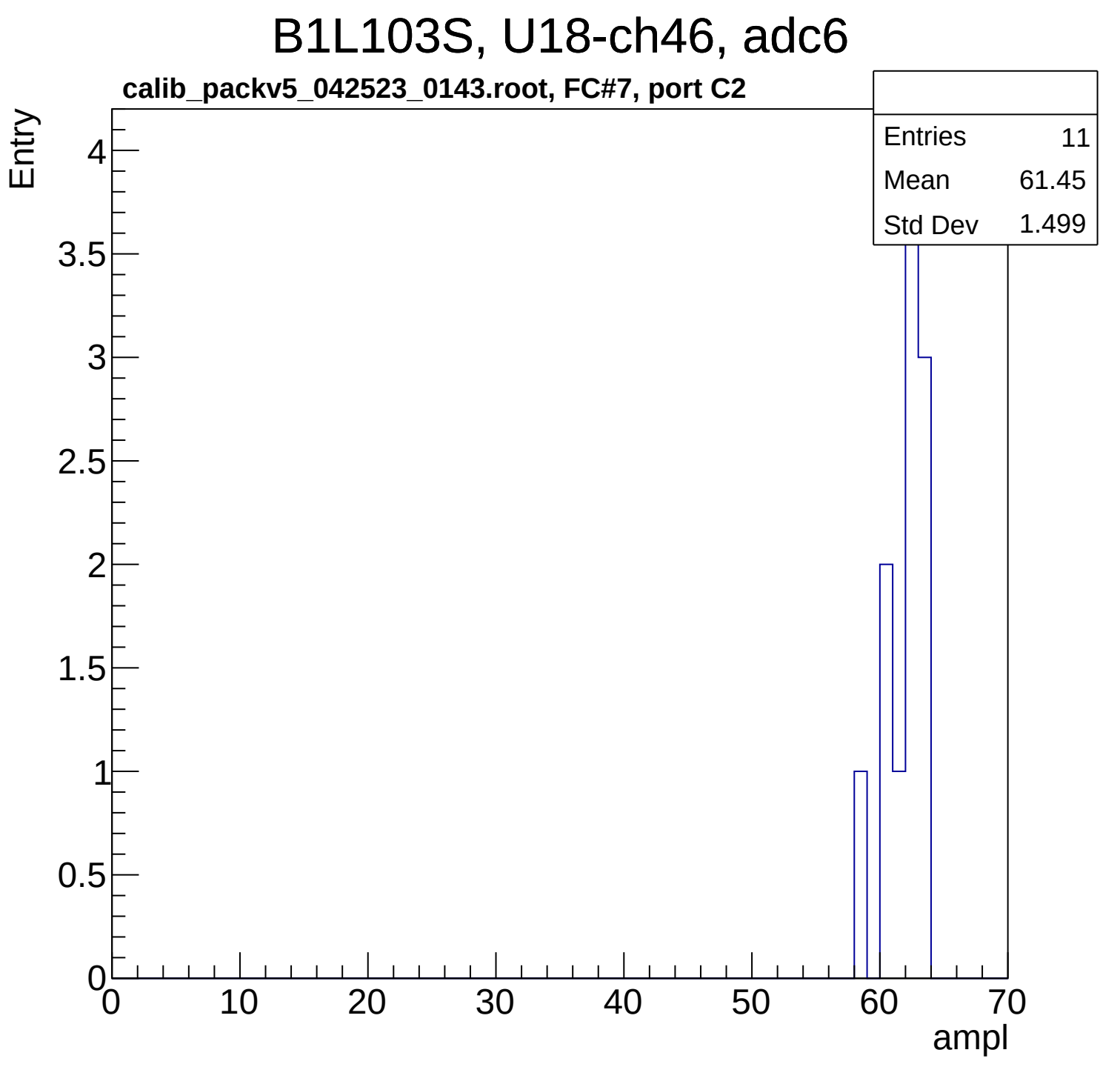
B1L103S, U18-ch46, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 11
Mean 61.45
Std Dev 1.499
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
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60
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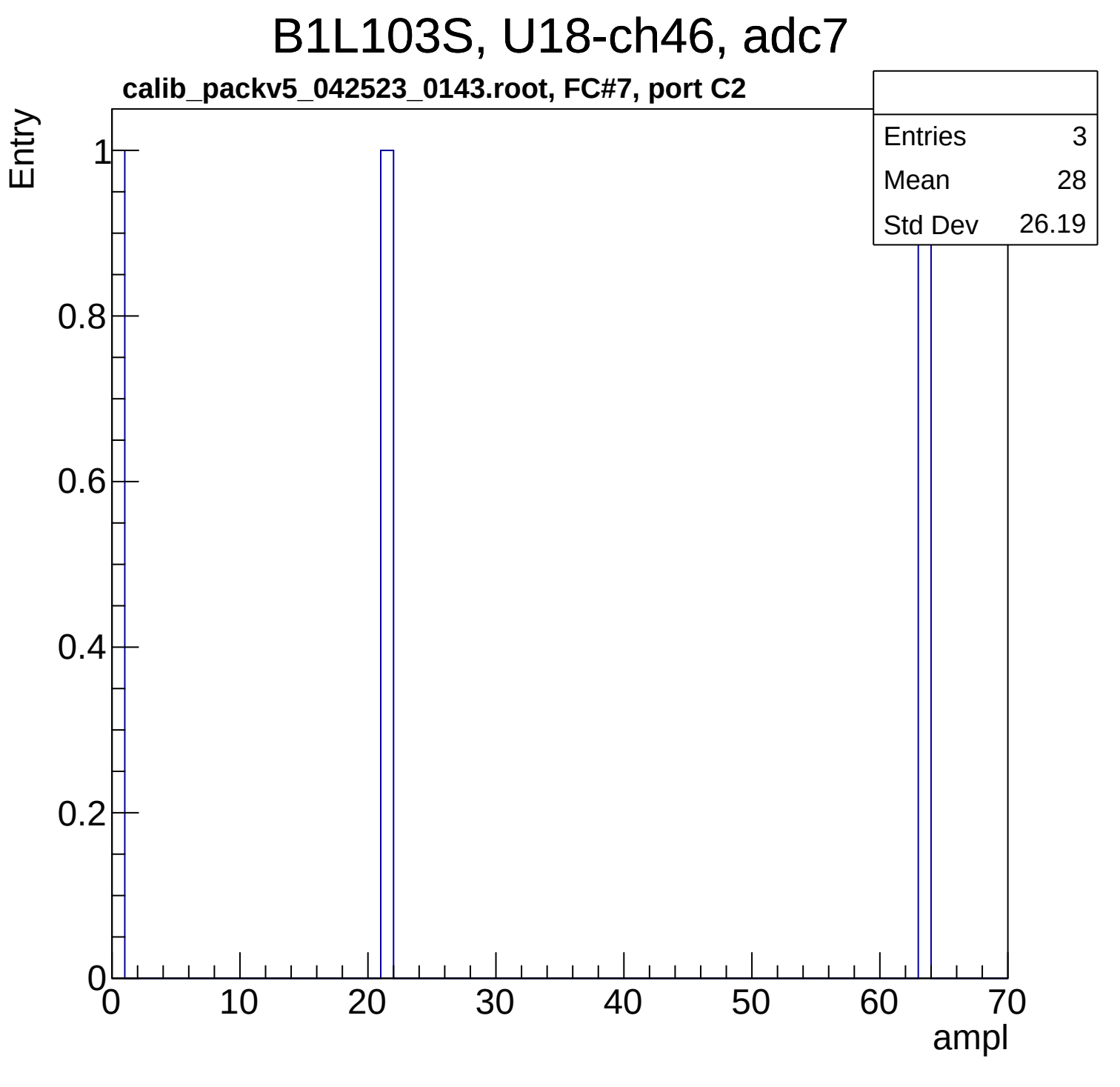
B1L103S, U18-ch46, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 28
Std Dev 26.19
Entry
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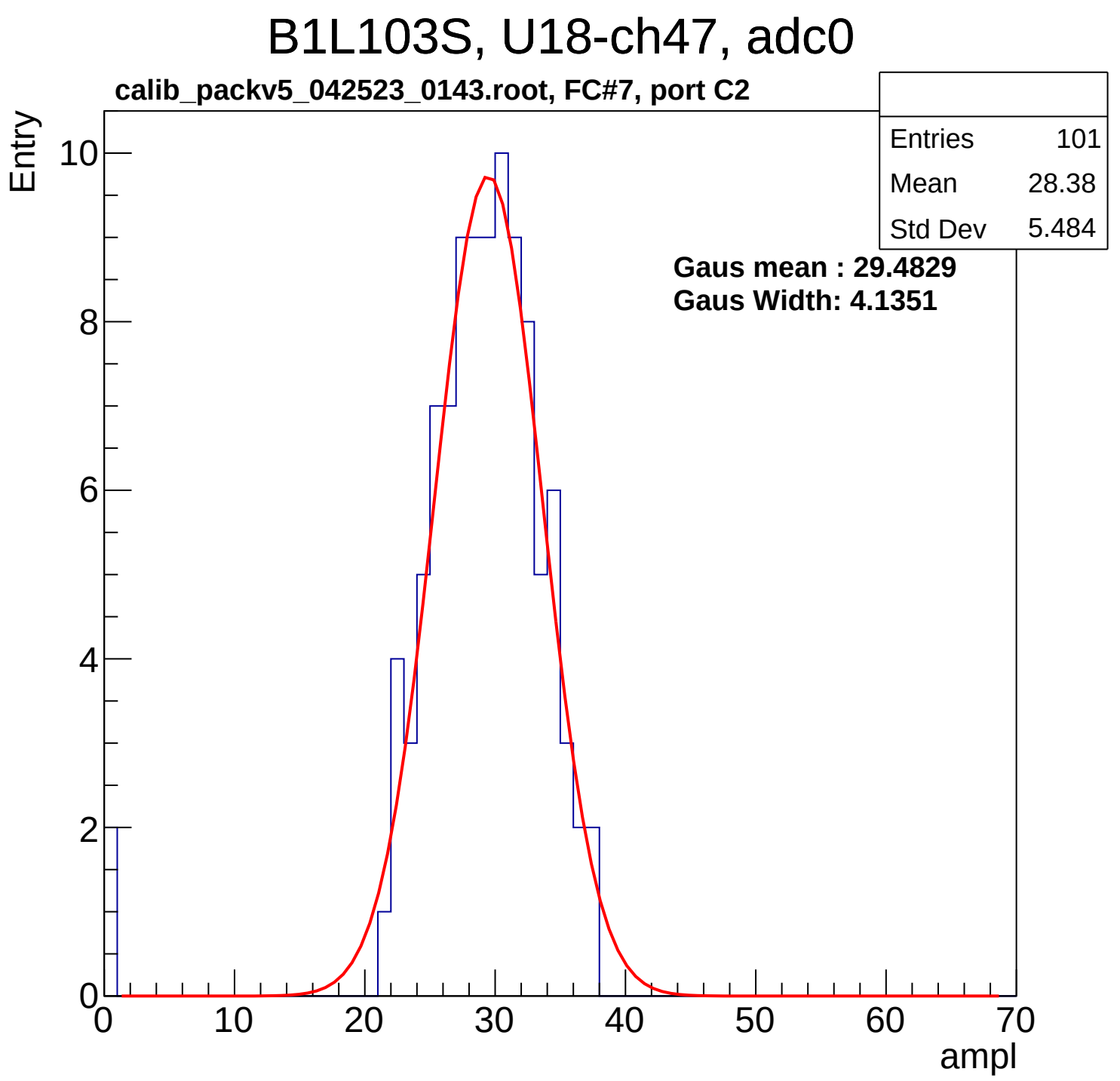
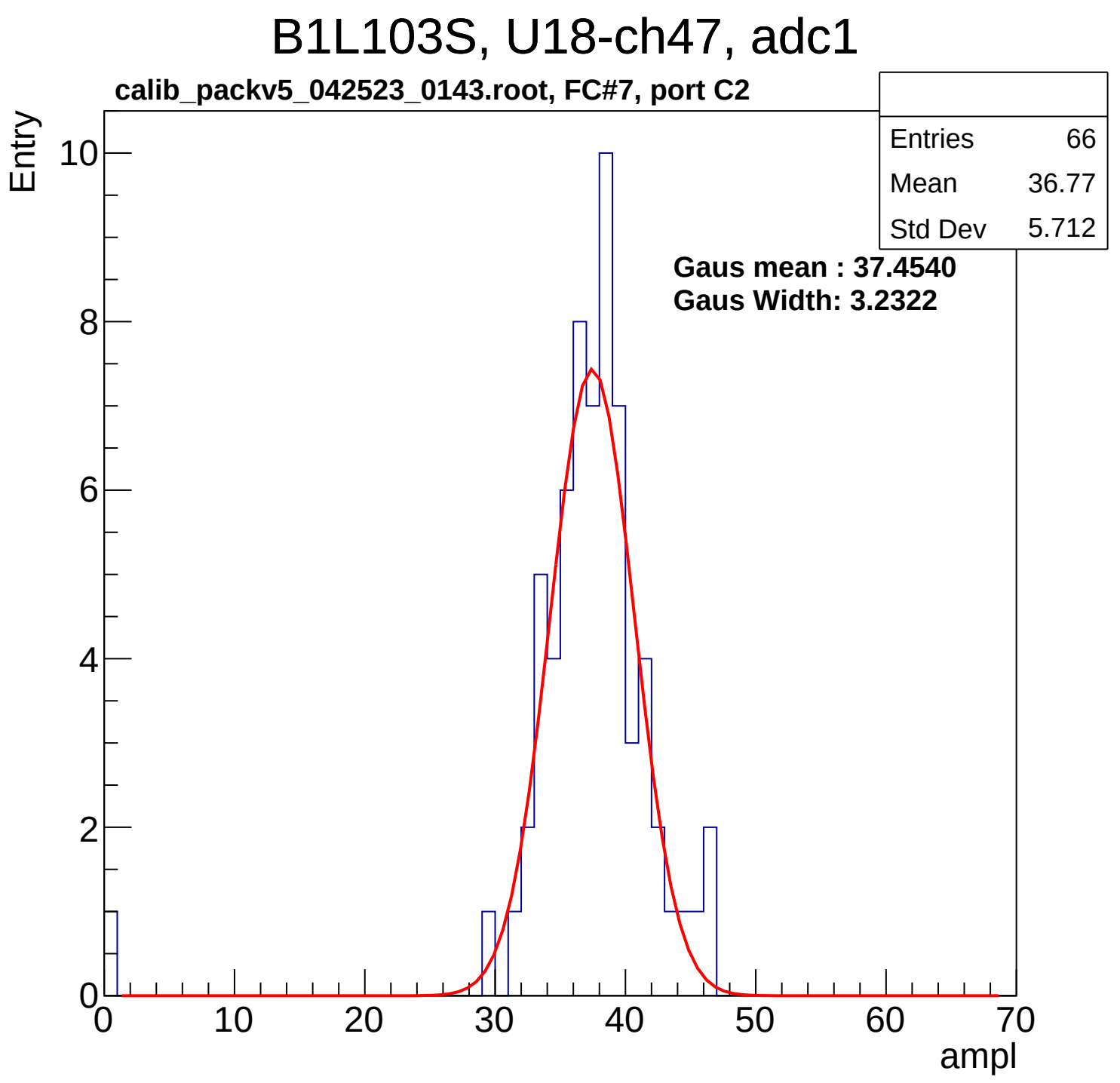
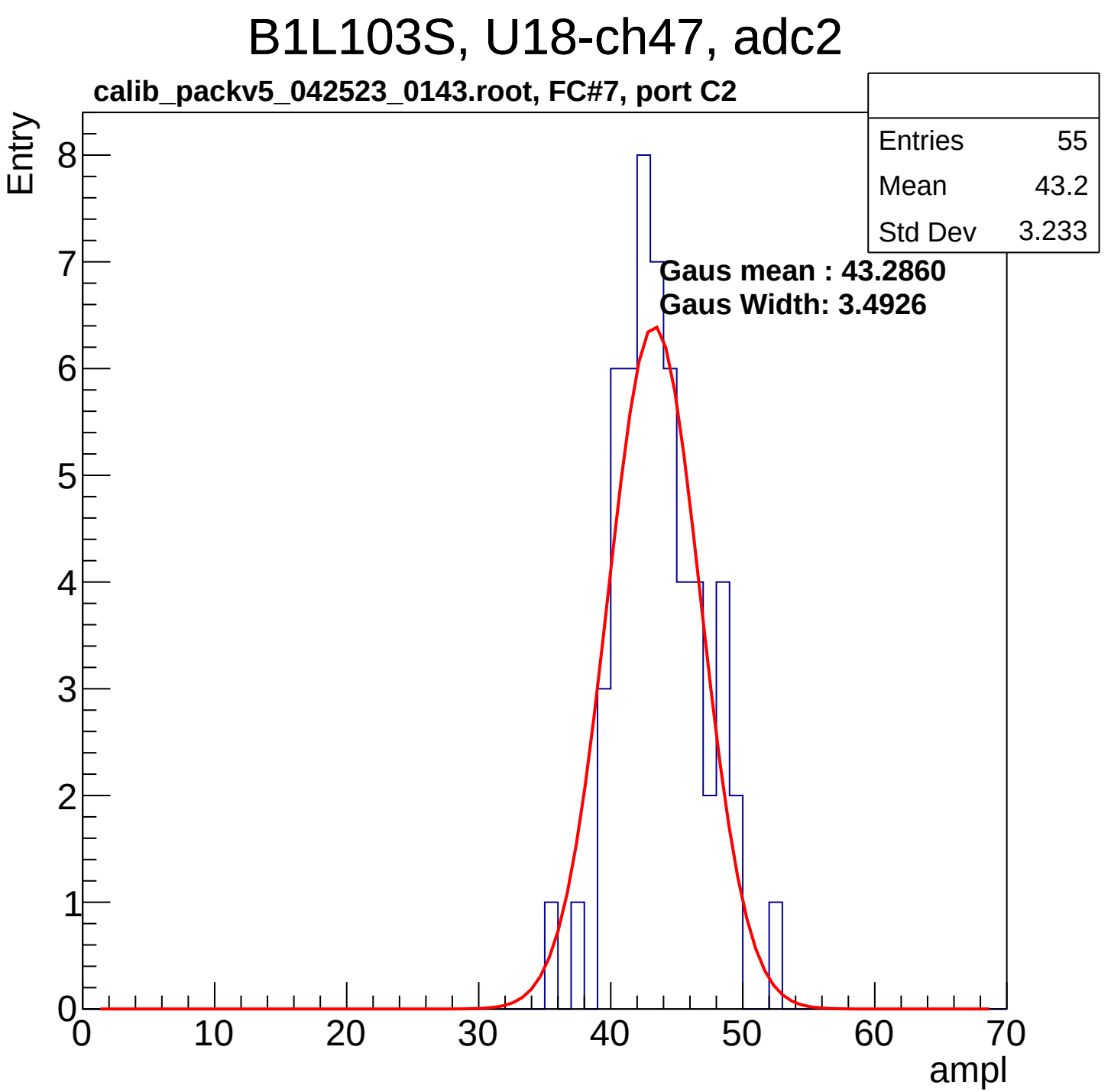
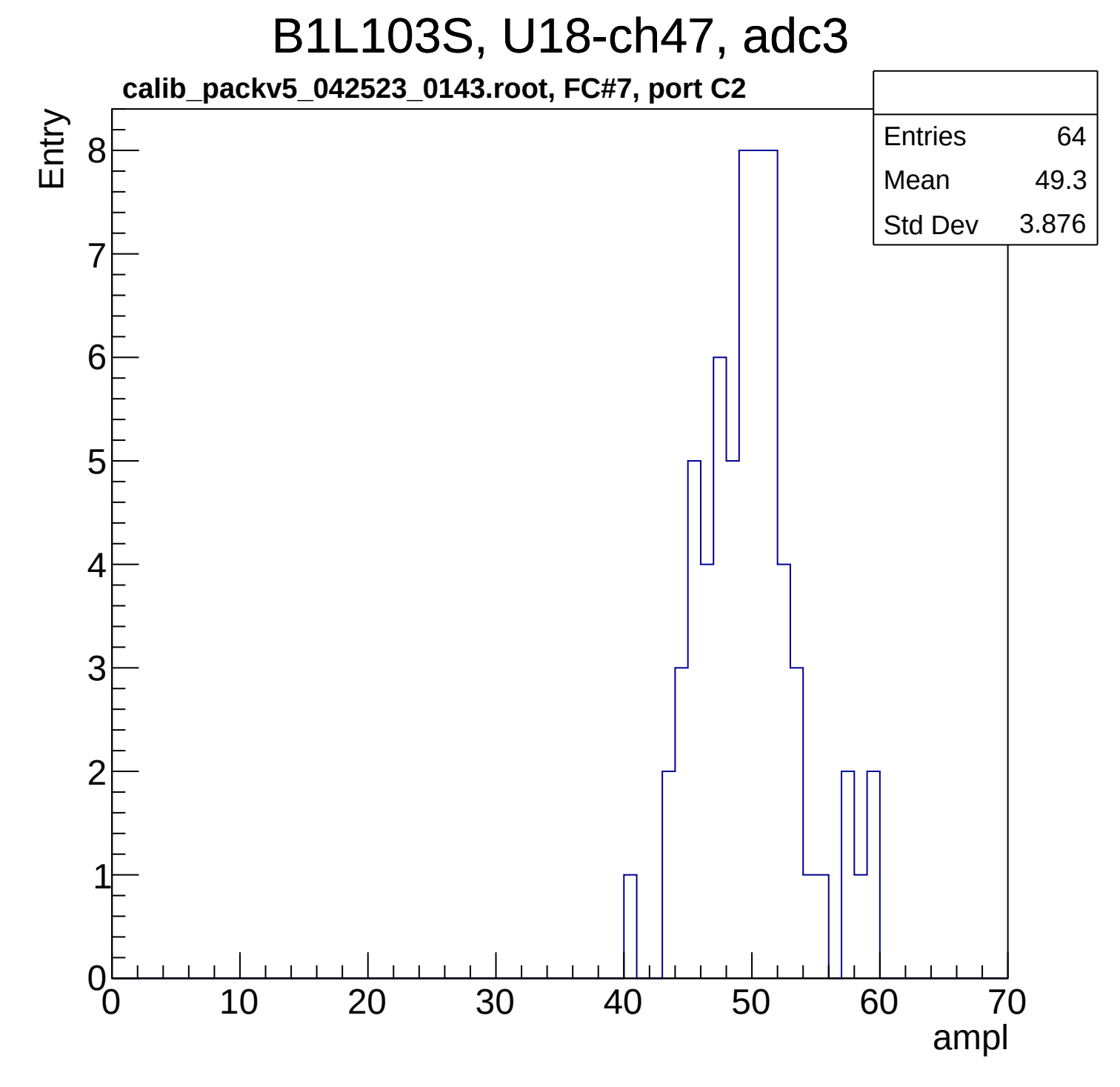
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch47, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 101
Mean 28.38
Std Dev 5.484
Gaus mean : 29.4829
Gaus Width: 4.1351
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch47, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 36.77
Std Dev 5.712
Gaus mean : 37.4540
Gaus Width: 3.2322
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch47, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 43.2
Std Dev 3.233
Gaus mean : 43.2860
Gaus Width: 3.4926
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch47, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 49.3
Std Dev 3.876
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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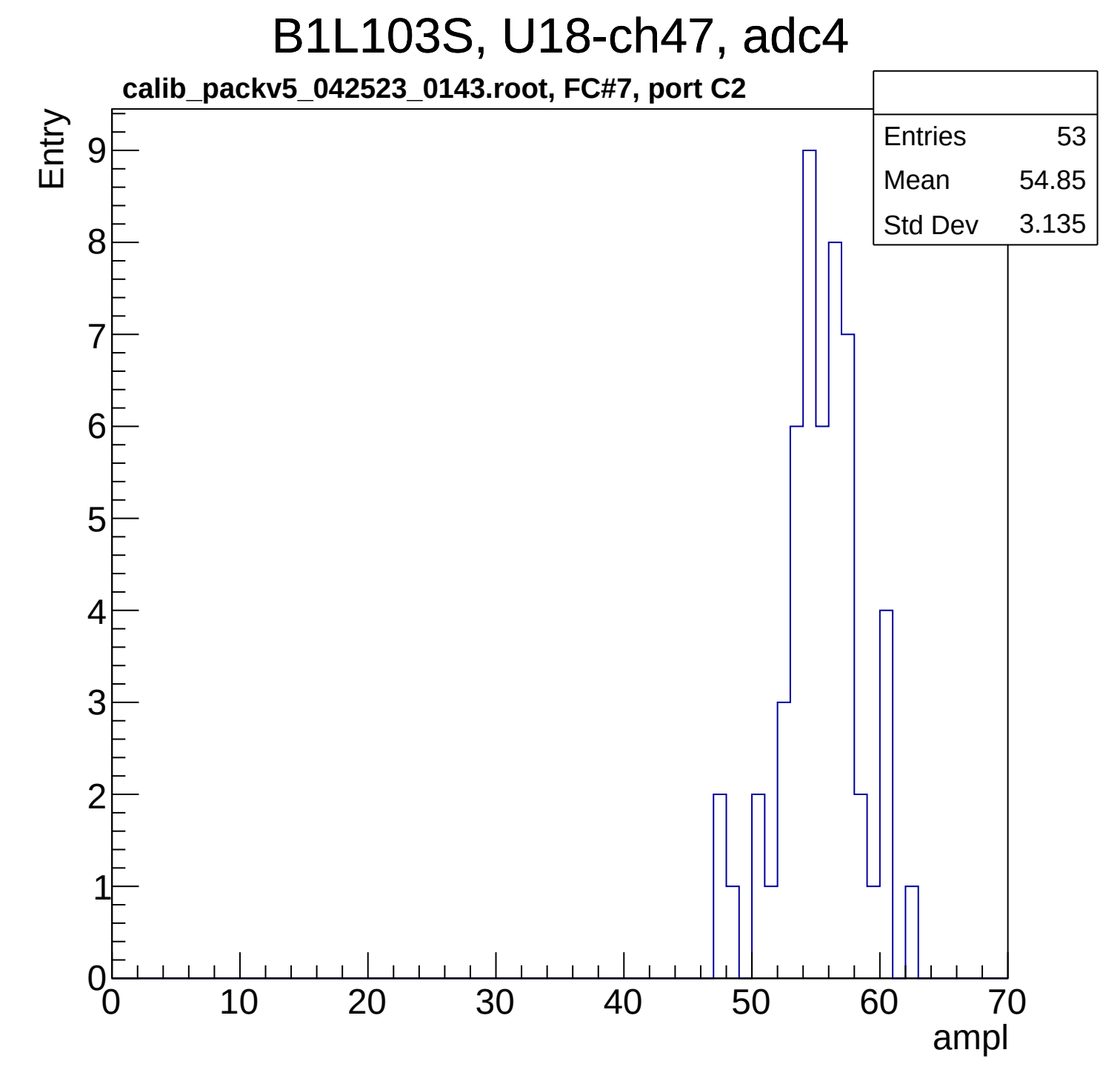
B1L103S, U18-ch47, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 54.85
Std Dev 3.135
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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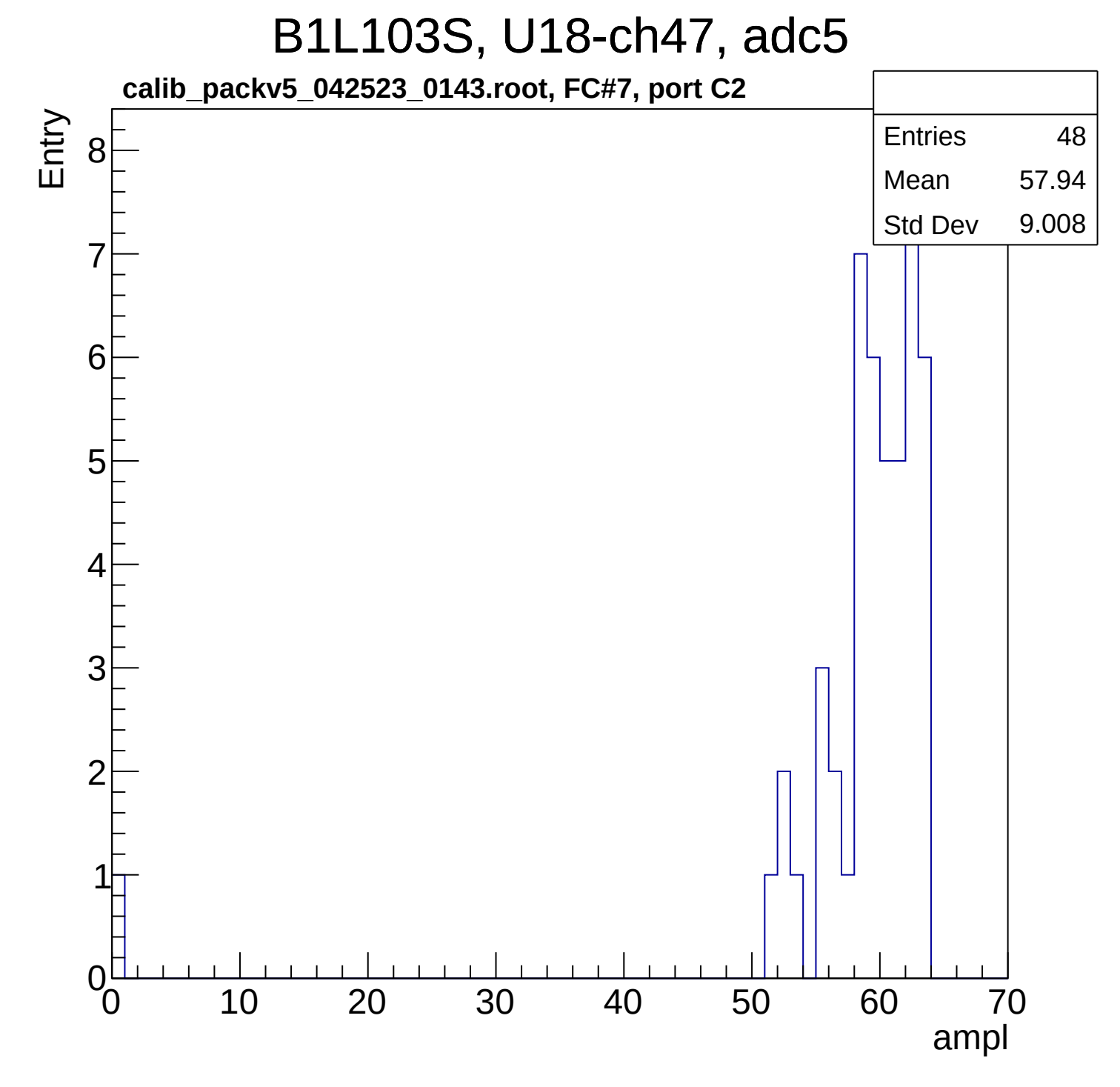
B1L103S, U18-ch47, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 48
Mean 57.94
Std Dev 9.008
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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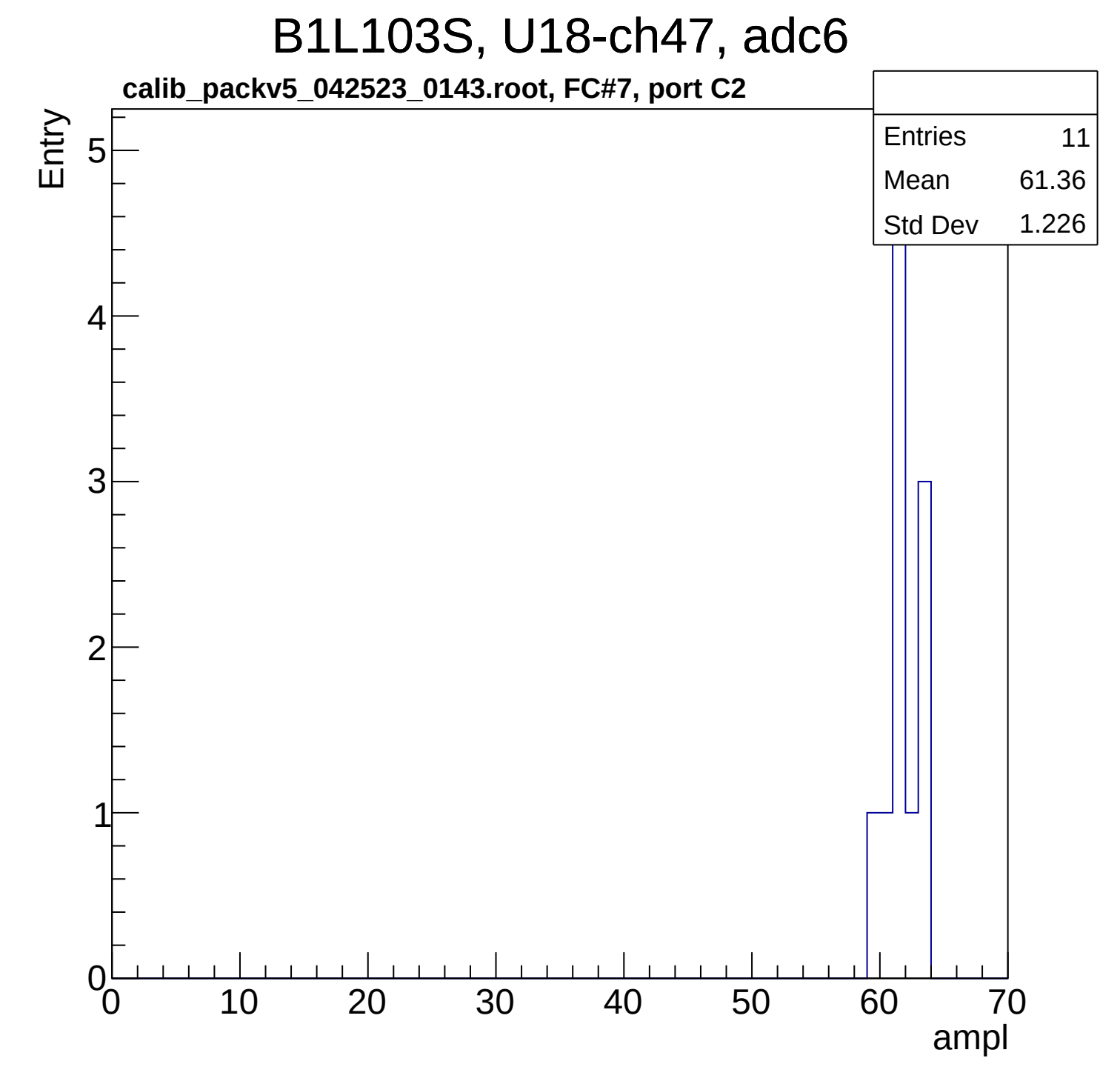
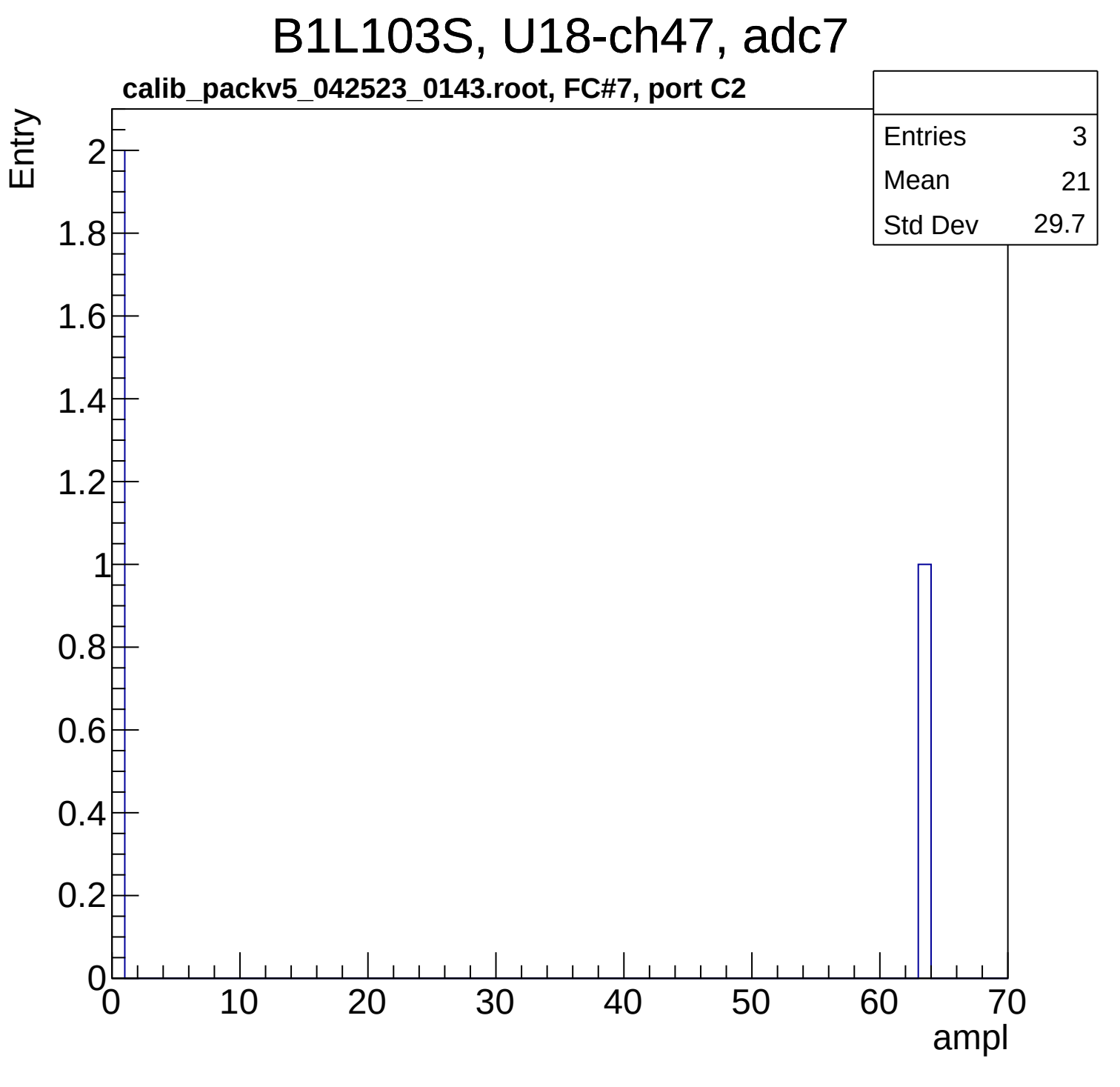

B1L103S, U18-ch47, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 11
Mean 61.36
Std Dev 1.226
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch47, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 21
Std Dev 29.7
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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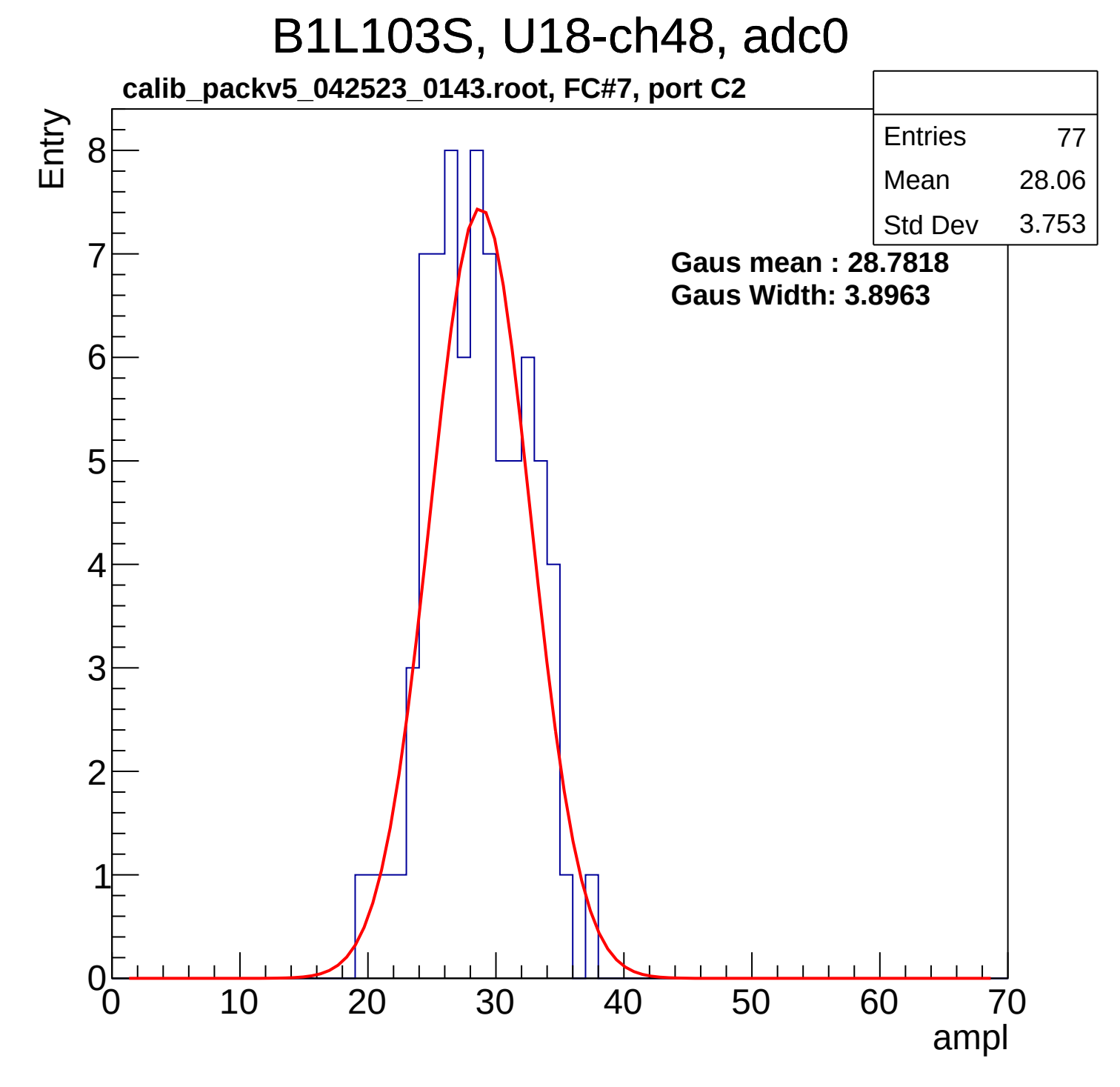
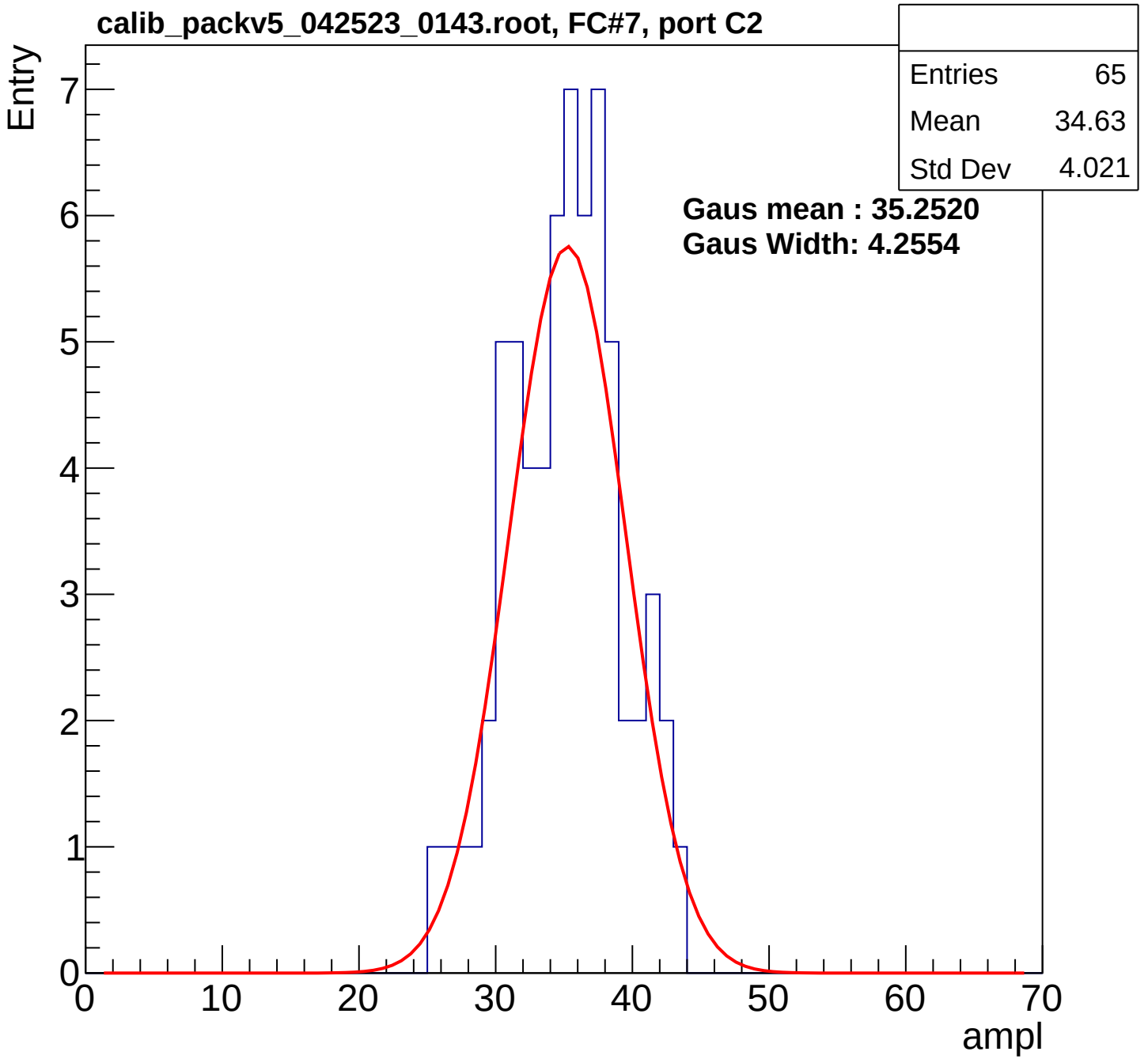
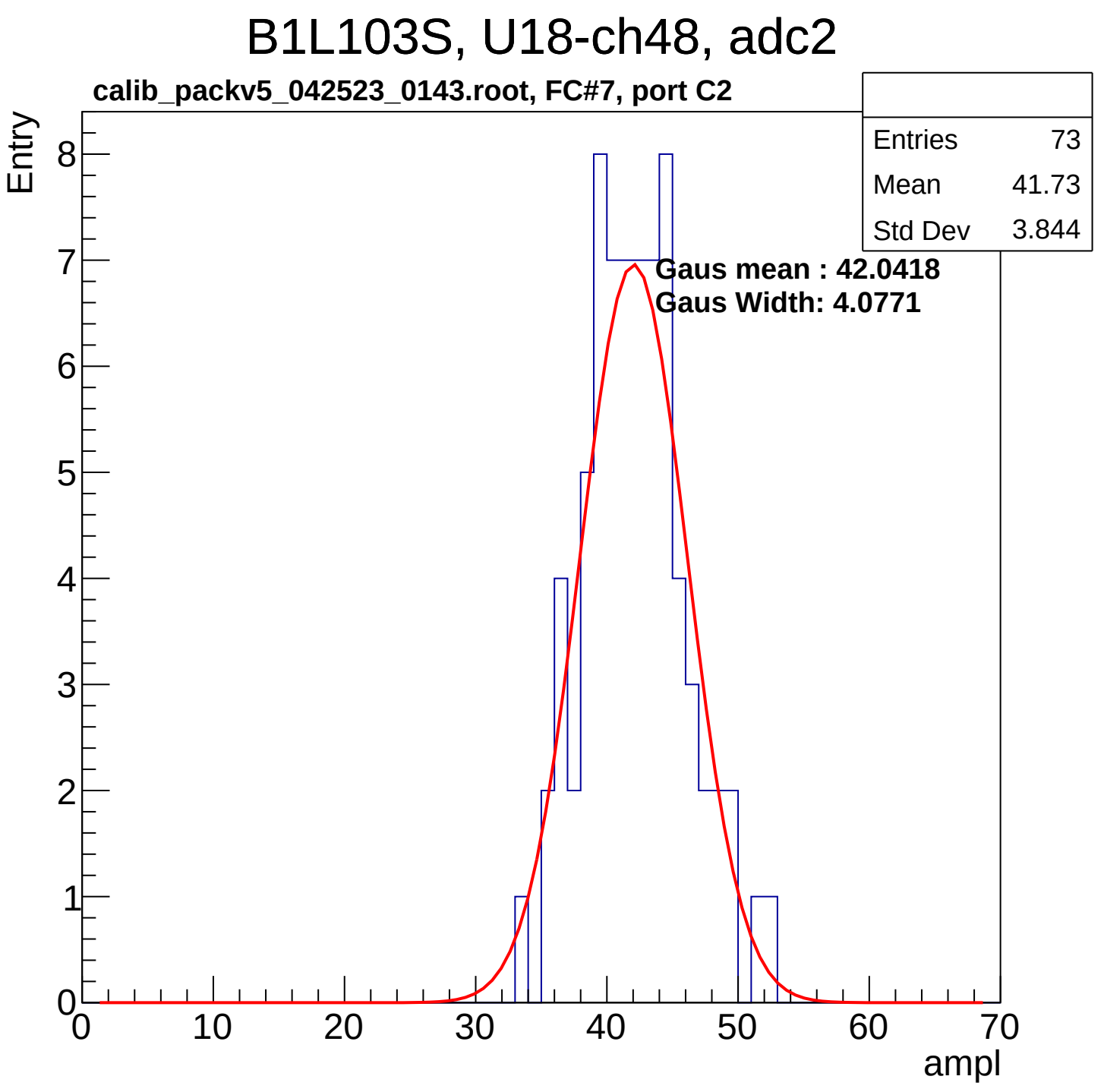

B1L103S, U18-ch48, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 77
Mean 28.06
Std Dev 3.753
Gaus mean : 28.7818
Gaus Width: 3.8963
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch48, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 34.63
Std Dev 4.021
Gaus mean : 35.2520
Gaus Width: 4.2554
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch48, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 73
Mean 41.73
Std Dev 3.844
Gaus mean : 42.0418
Gaus Width: 4.0771
Entry
ampl
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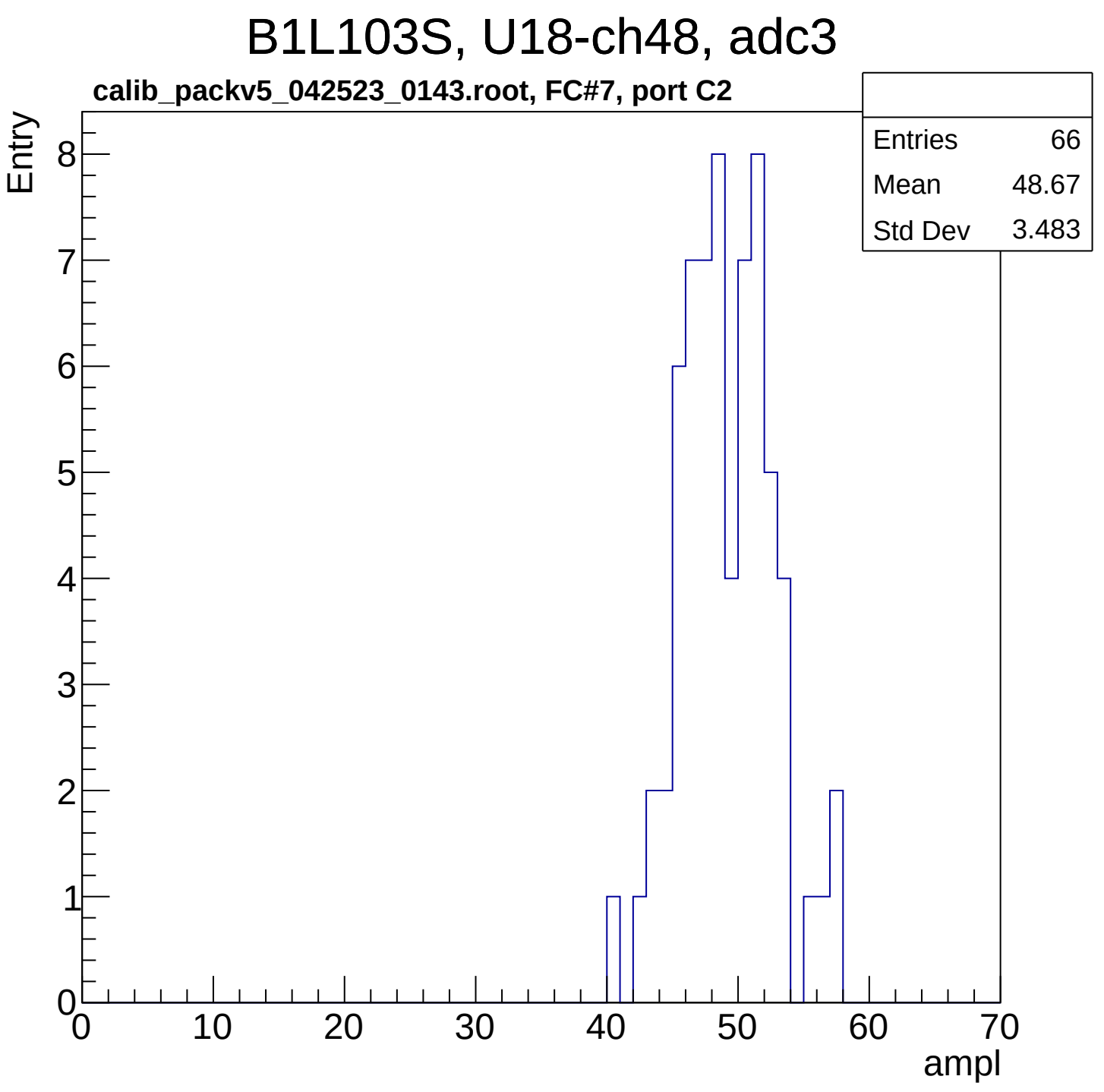
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch48, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 48.67
Std Dev 3.483
Entry
ampl
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1
2
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4
5
6
7
8
0
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40
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60
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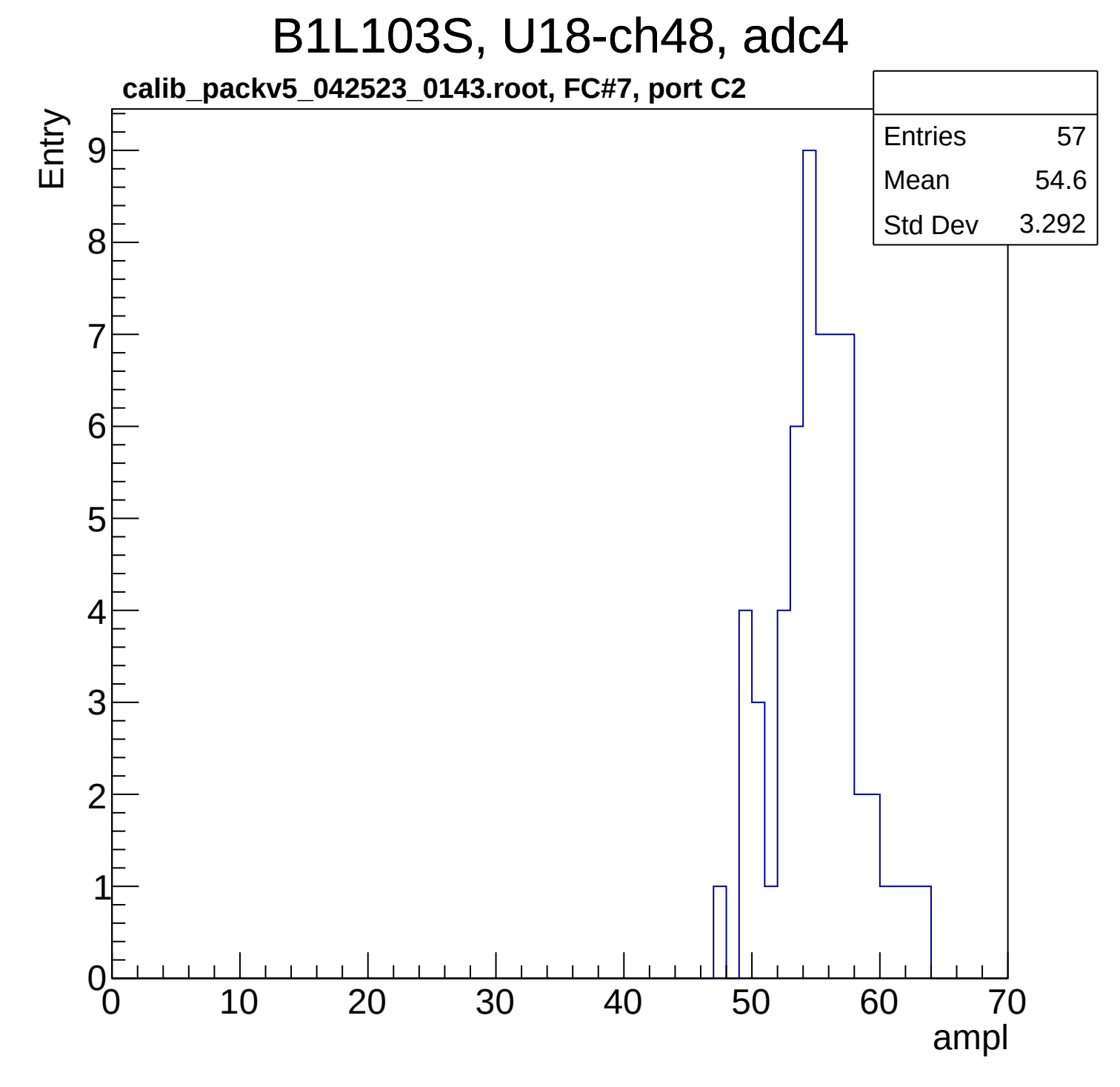
B1L103S, U18-ch48, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 54.6
Std Dev 3.292
Entry
ampl
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2
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6
7
8
9
0
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40
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60
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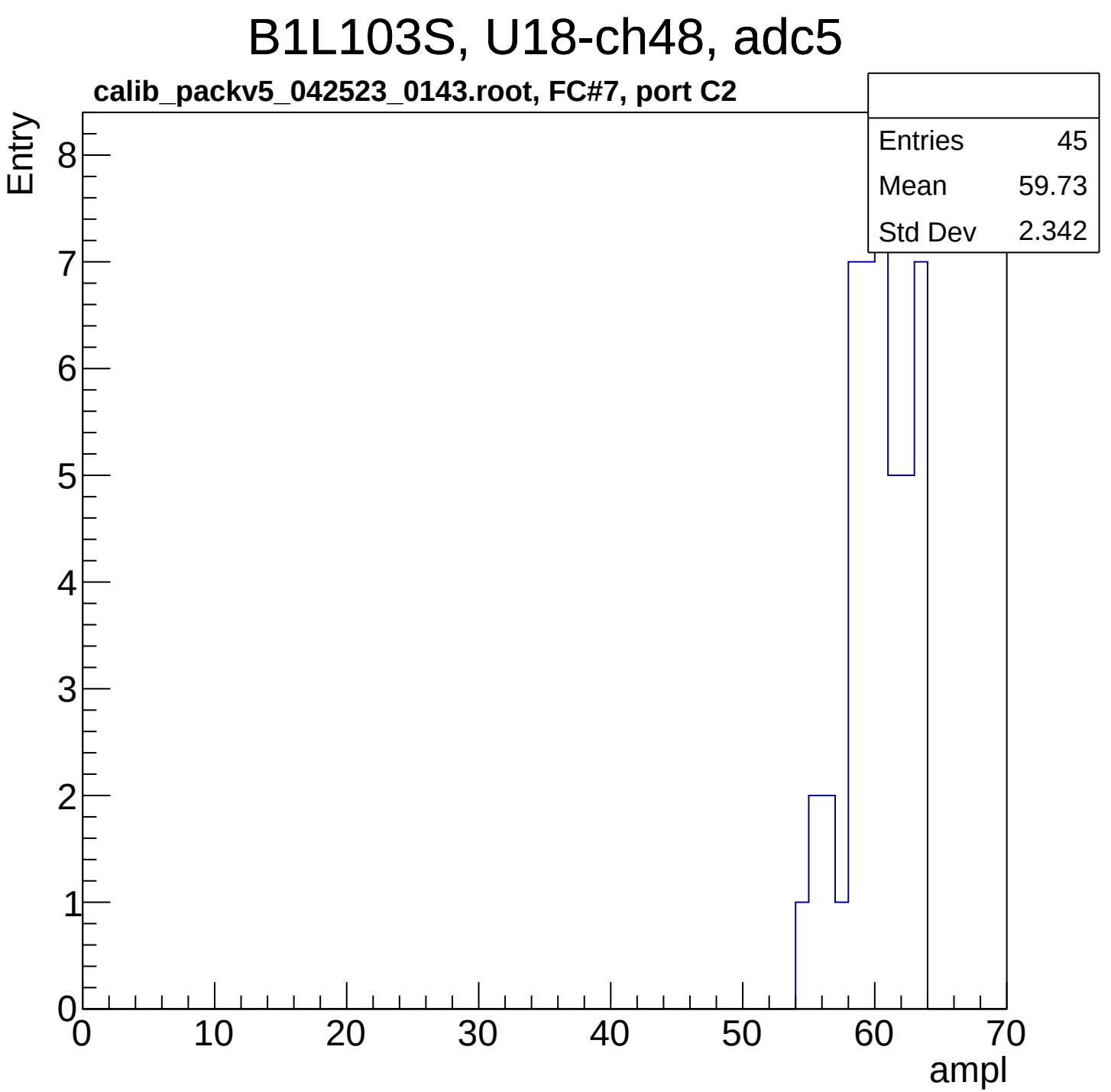
B1L103S, U18-ch48, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 45
Mean 59.73
Std Dev 2.342
Entry
ampl
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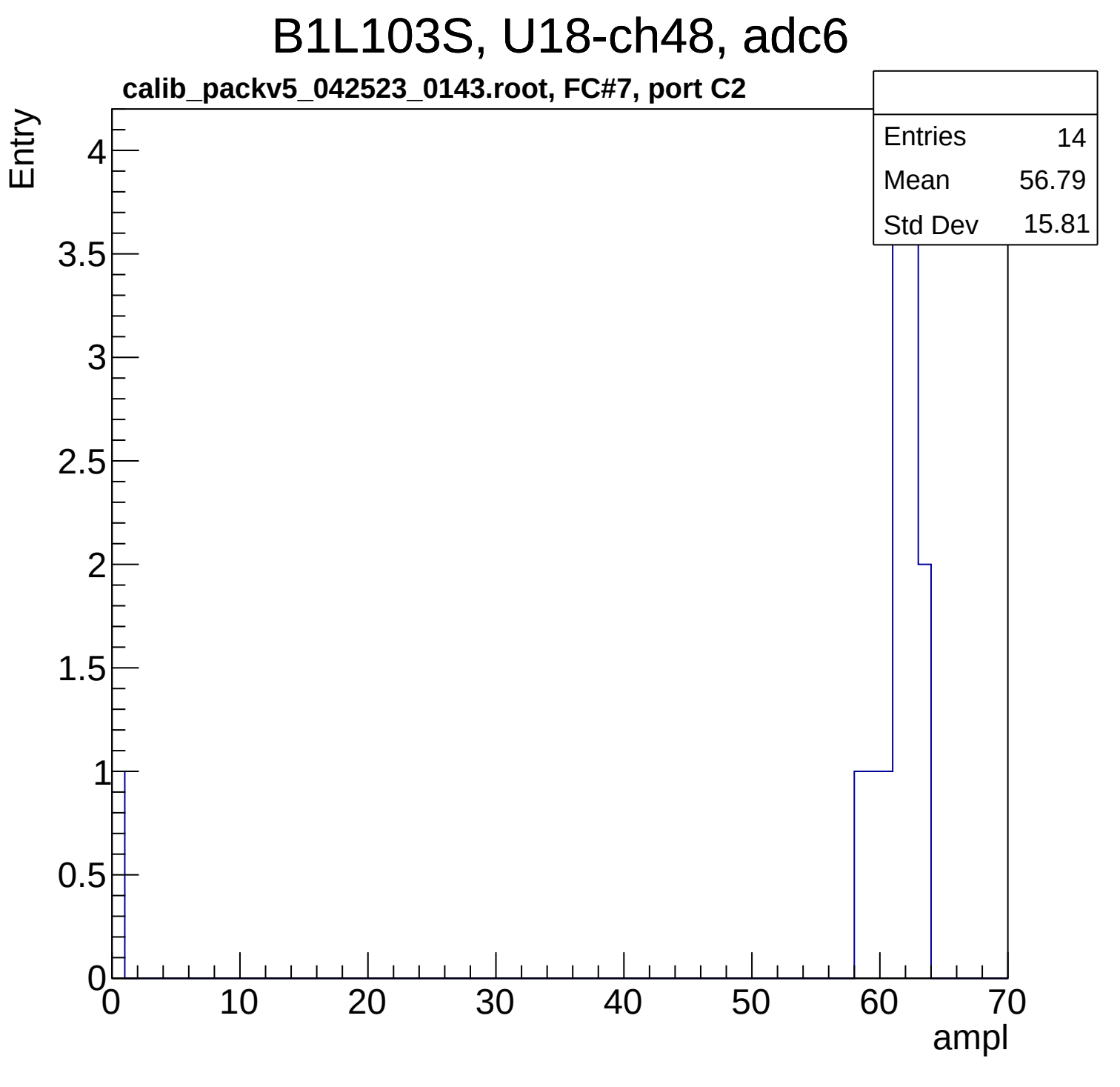
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch48, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 14
Mean 56.79
Std Dev 15.81
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
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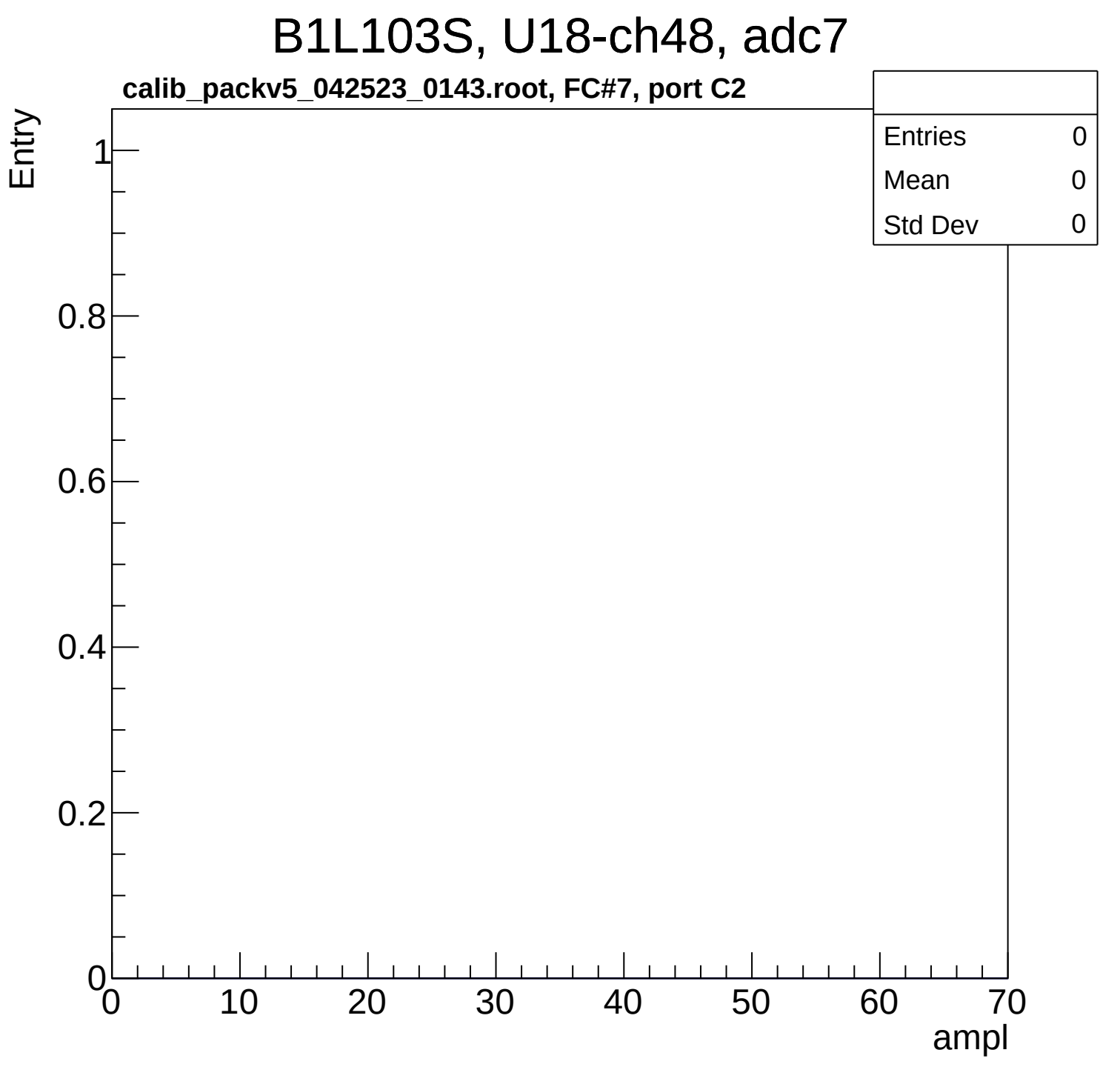
20
30
40
50
60
70


B1L103S, U18-ch48, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
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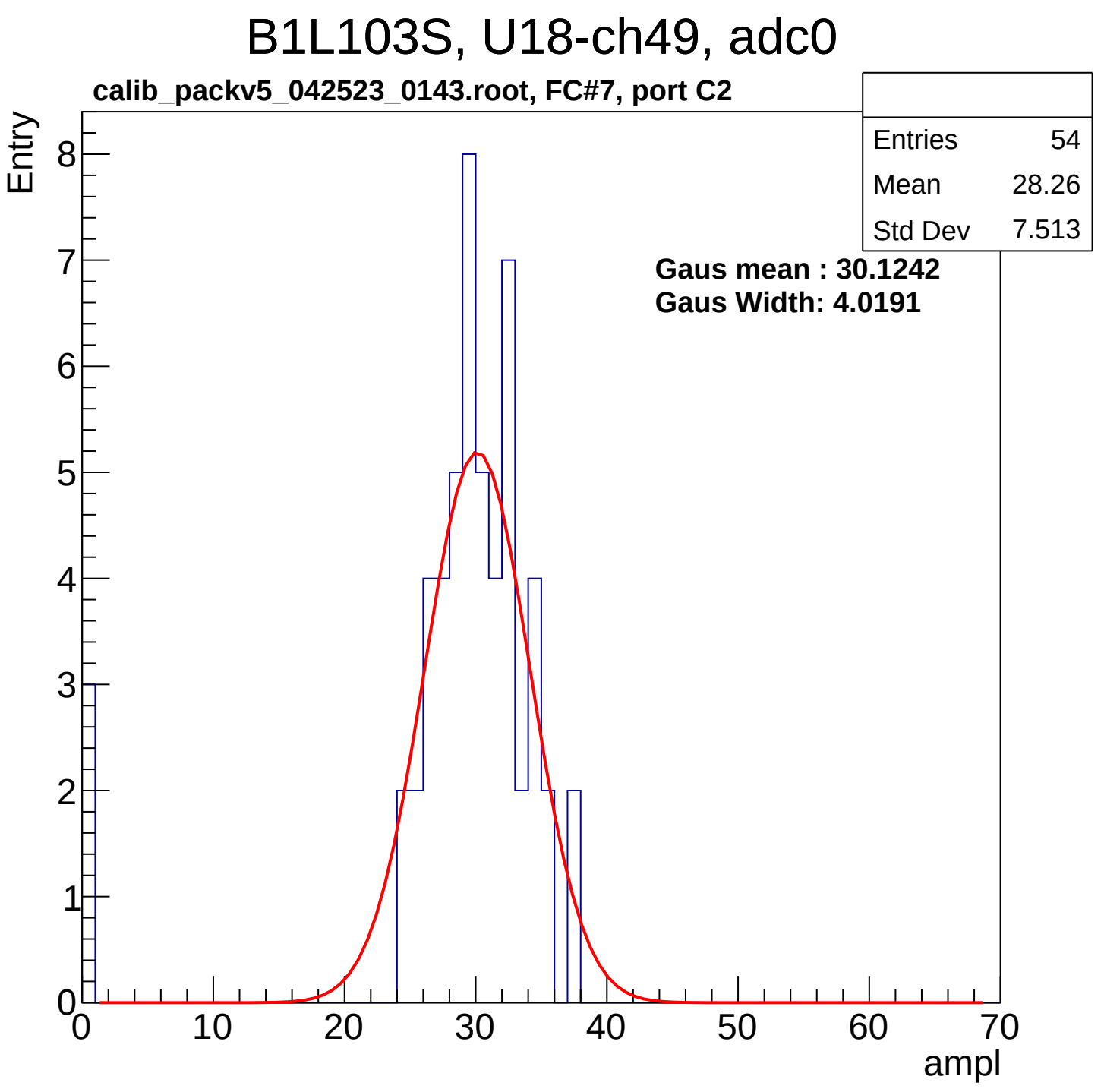
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch49, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 54
Mean 28.26
Std Dev 7.513
Gaus mean : 30.1242
Gaus Width: 4.0191
Entry
ampl
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1
2
3
4
5
6
7
8
0
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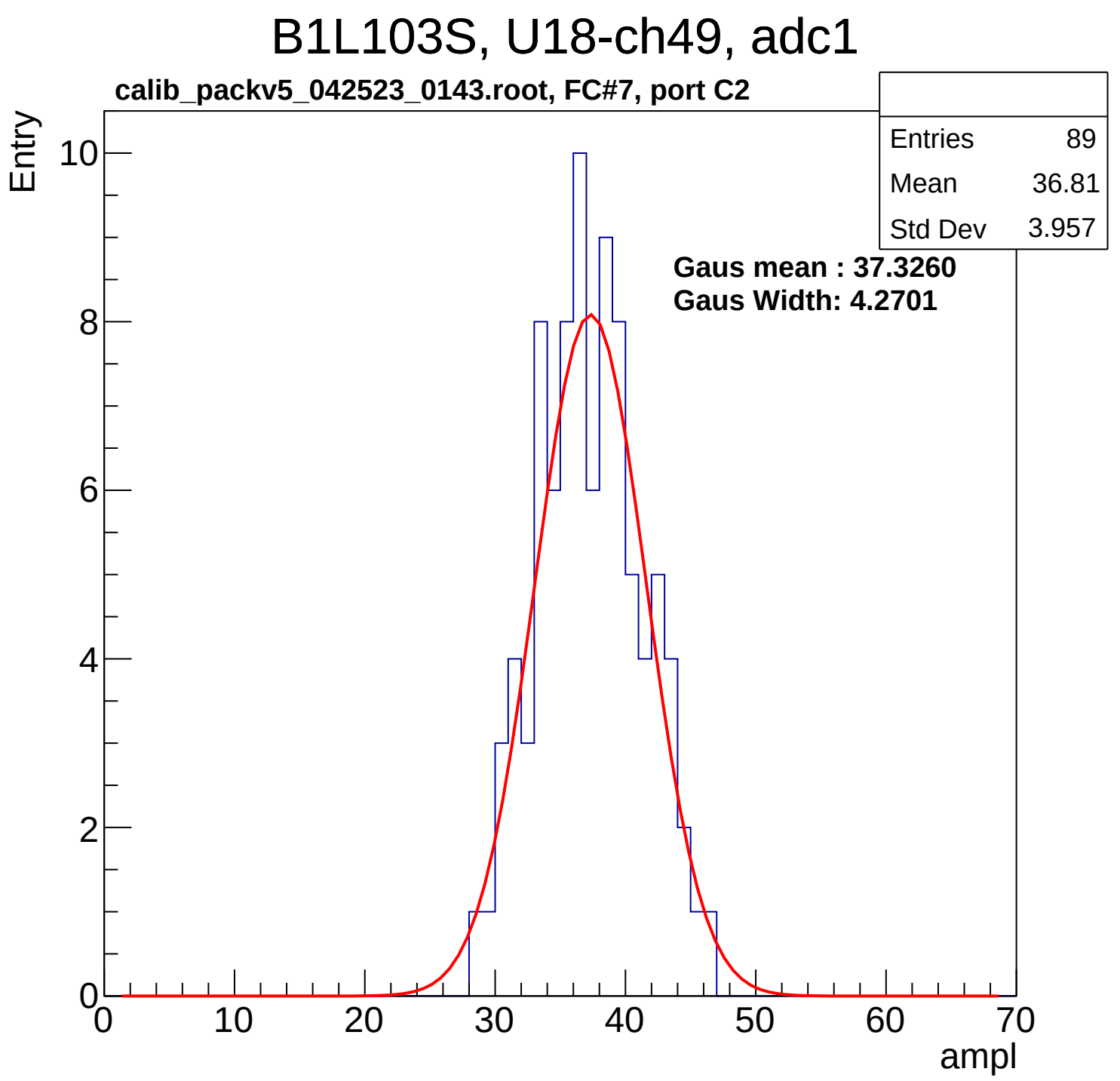
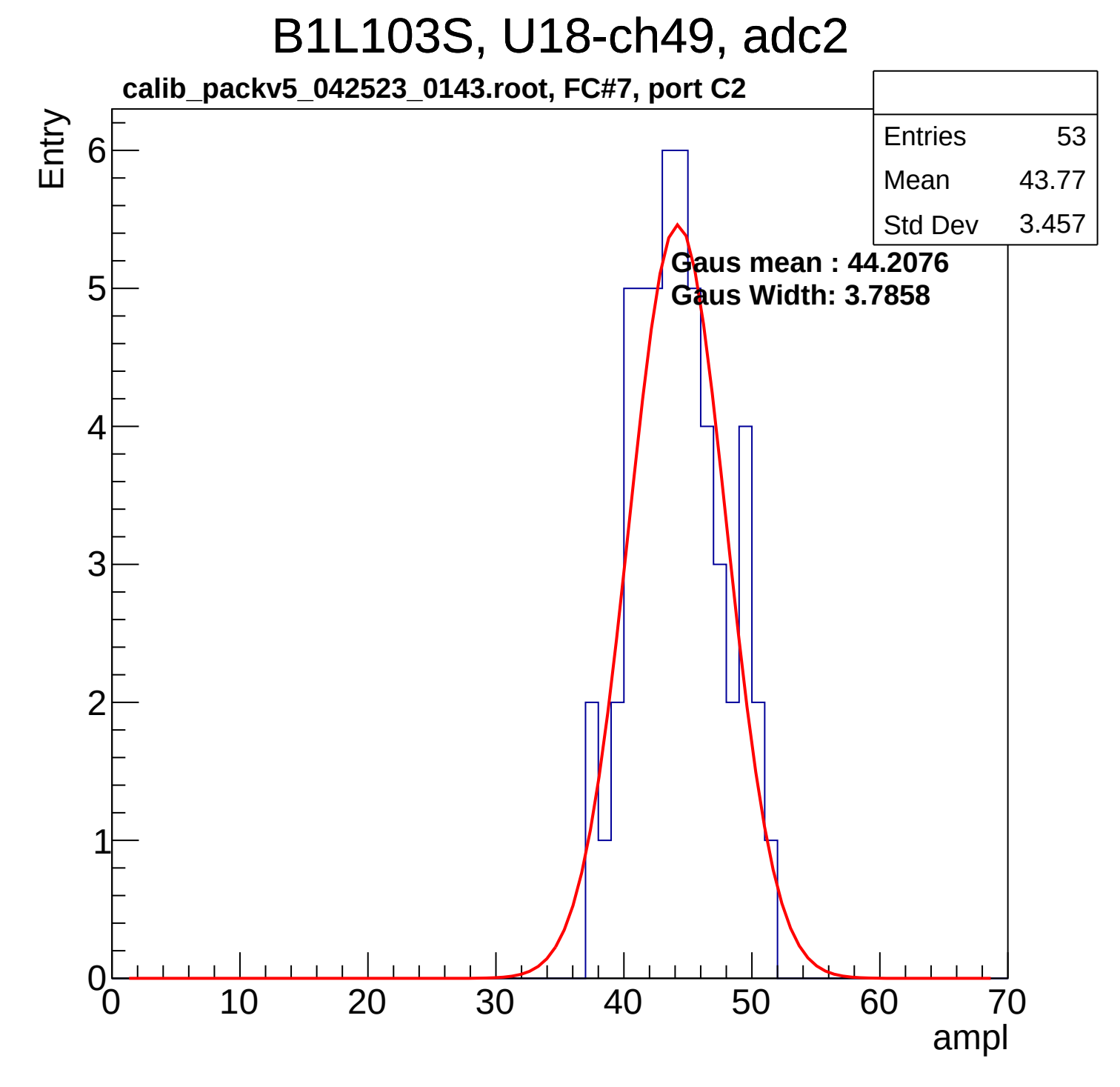
20
30
40
50
60
70


B1L103S, U18-ch49, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 89
Mean 36.81
Std Dev 3.957
Gaus mean : 37.3260
Gaus Width: 4.2701
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch49, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 43.77
Std Dev 3.457
Gaus mean : 44.2076
Gaus Width: 3.7858
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
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60
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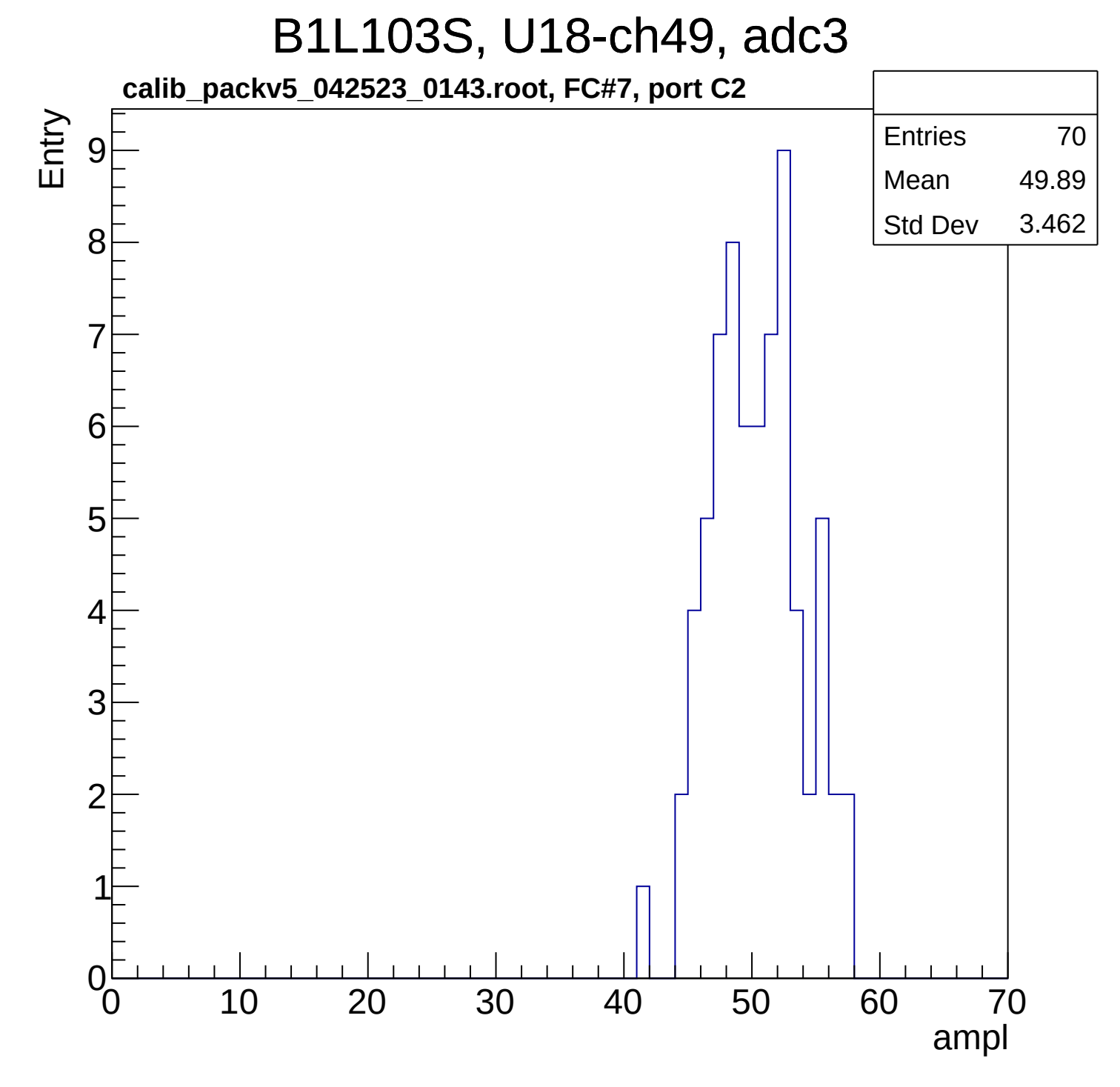
B1L103S, U18-ch49, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 49.89
Std Dev 3.462
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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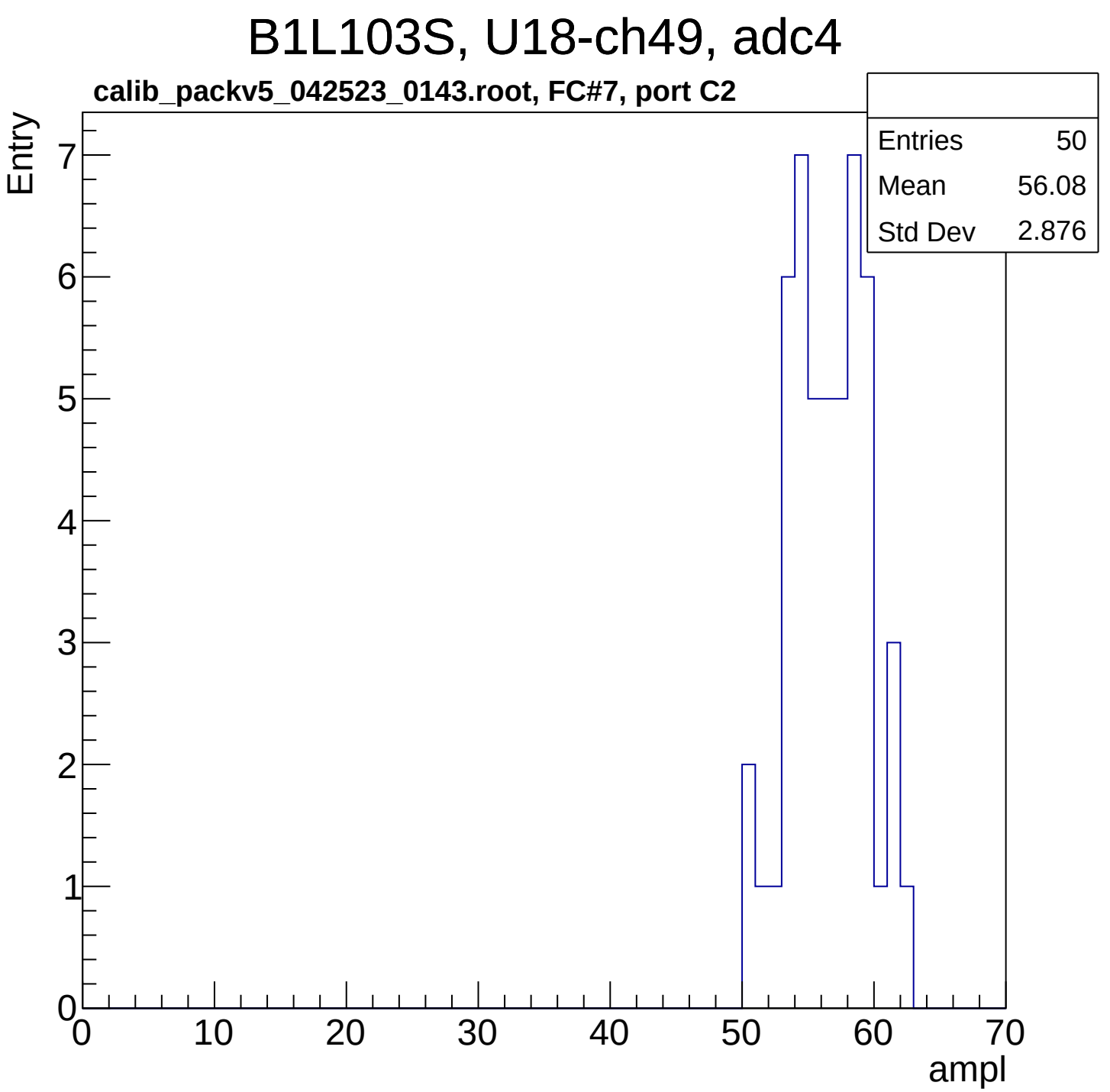
B1L103S, U18-ch49, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 50
Mean 56.08
Std Dev 2.876
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
30
40
50
60
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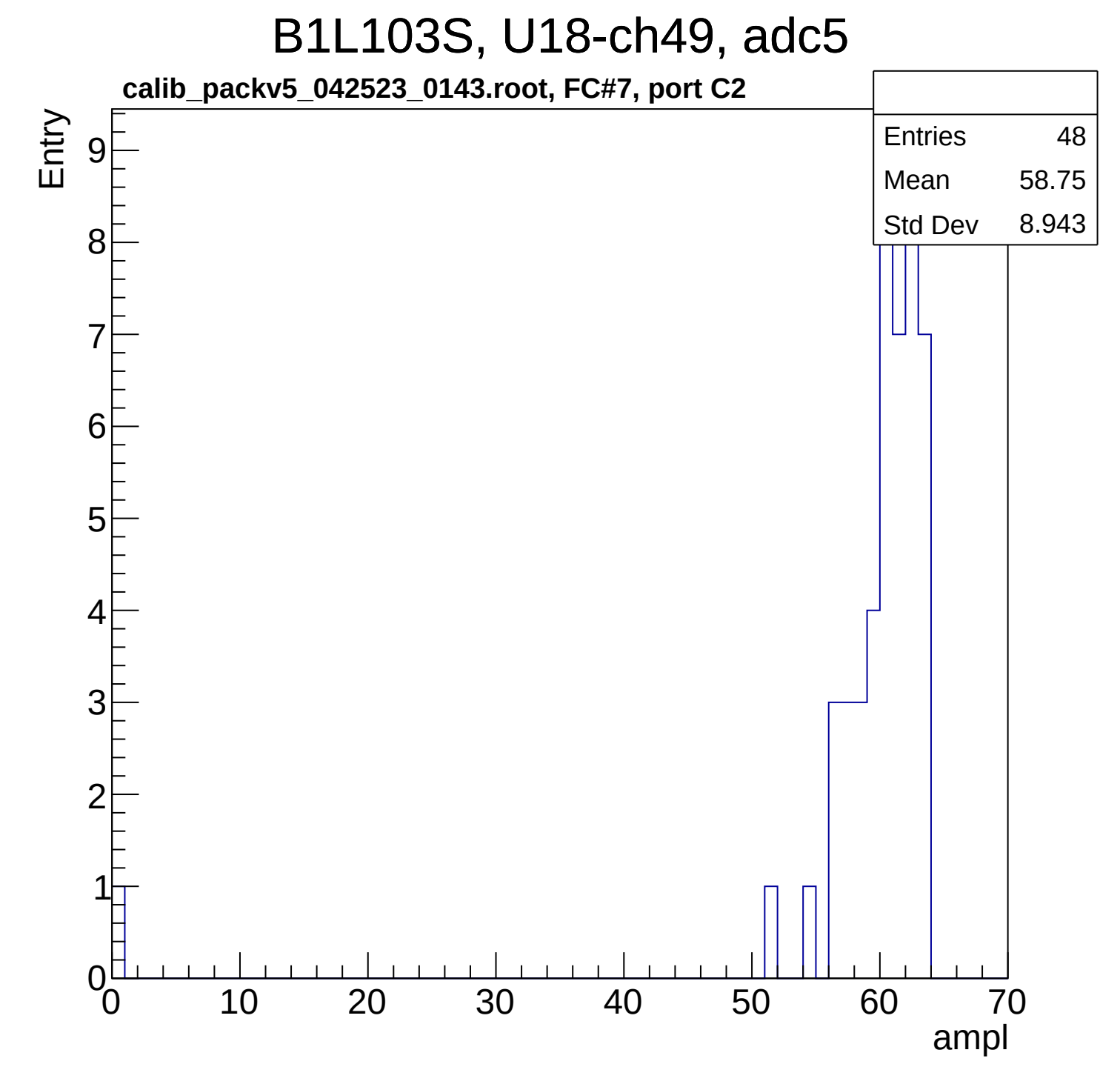
B1L103S, U18-ch49, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 48
Mean 58.75
Std Dev 8.943
Entry
ampl
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2
3
4
5
6
7
8
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0
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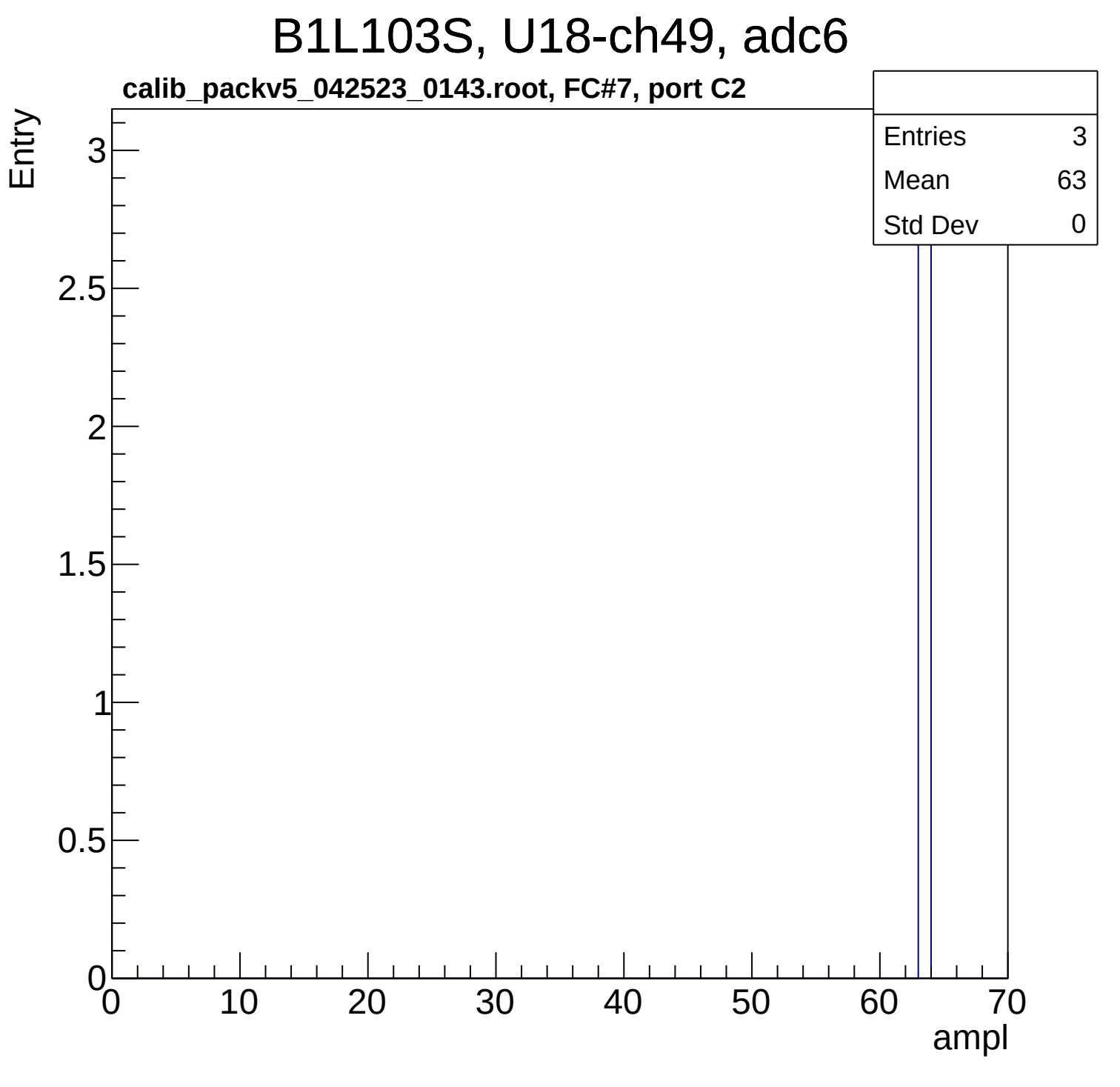
B1L103S, U18-ch49, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 63
Std Dev 0
Entry
ampl
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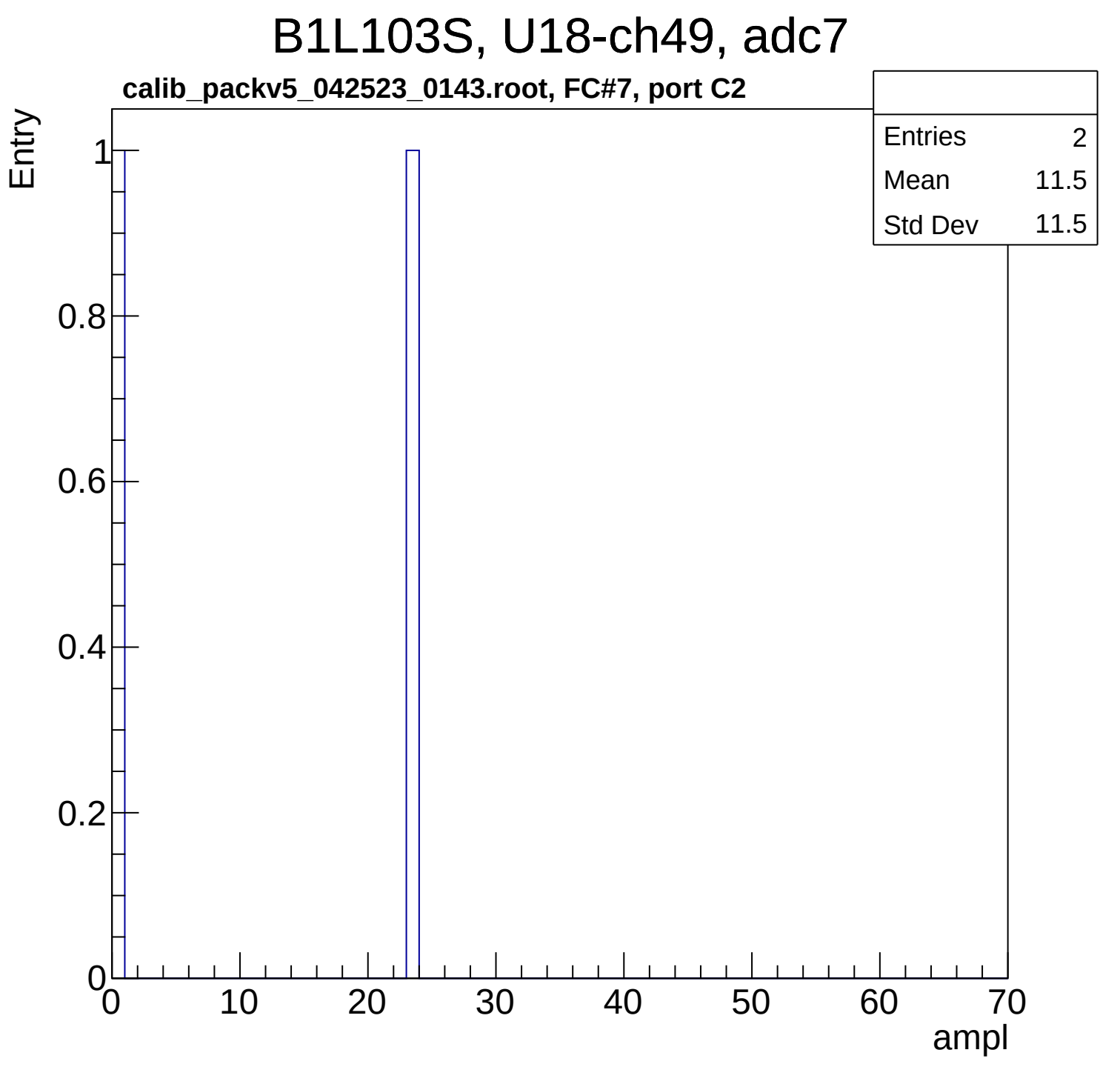
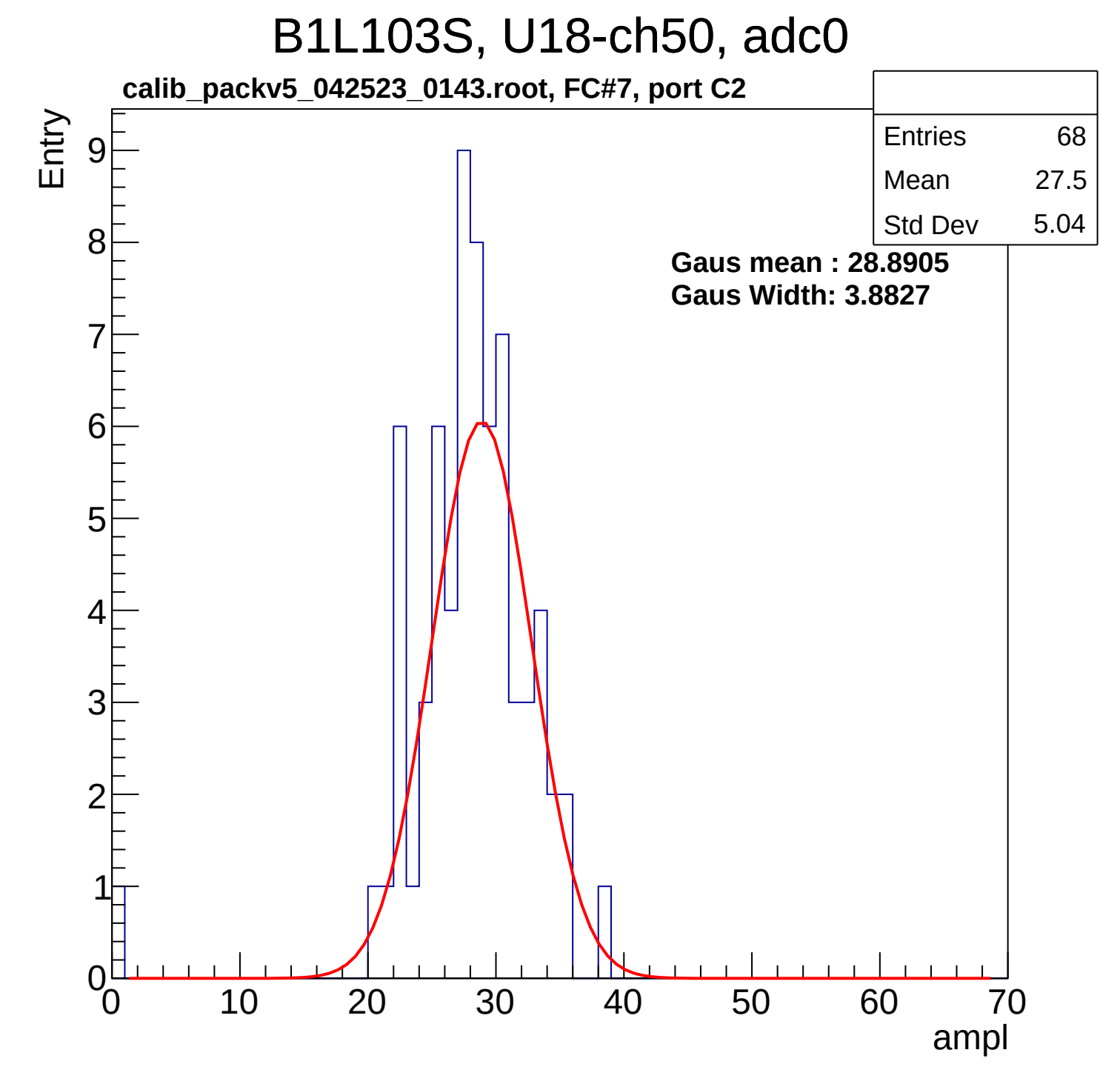
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U18-ch49, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 11.5
Std Dev 11.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch50, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 27.5
Std Dev 5.04
Gaus mean : 28.8905
Gaus Width: 3.8827
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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40
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60
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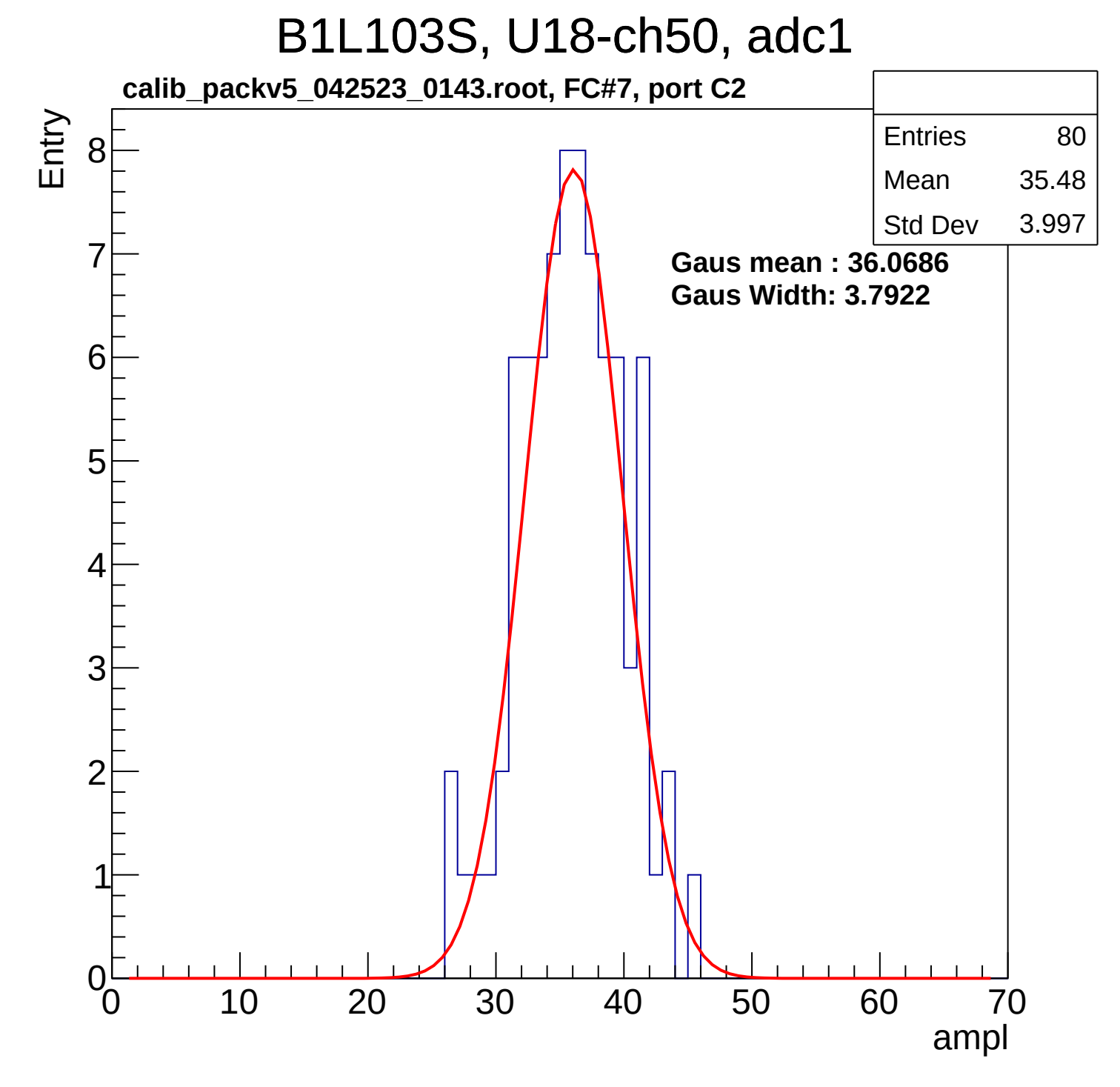
B1L103S, U18-ch50, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 80
Mean 35.48
Std Dev 3.997
Gaus mean : 36.0686
Gaus Width: 3.7922
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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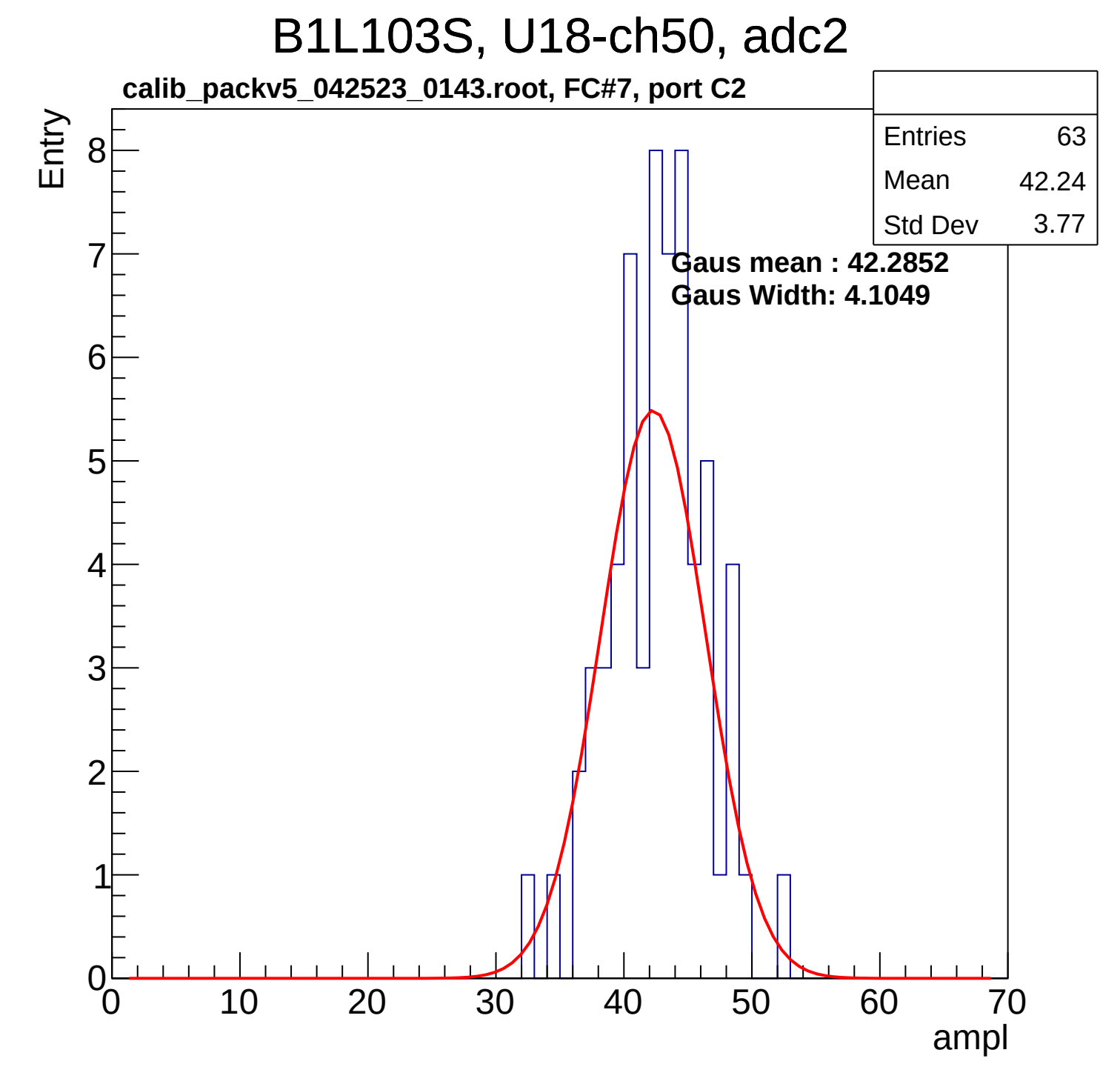
B1L103S, U18-ch50, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 42.24
Std Dev 3.77
Gaus mean : 42.2852
Gaus Width: 4.1049
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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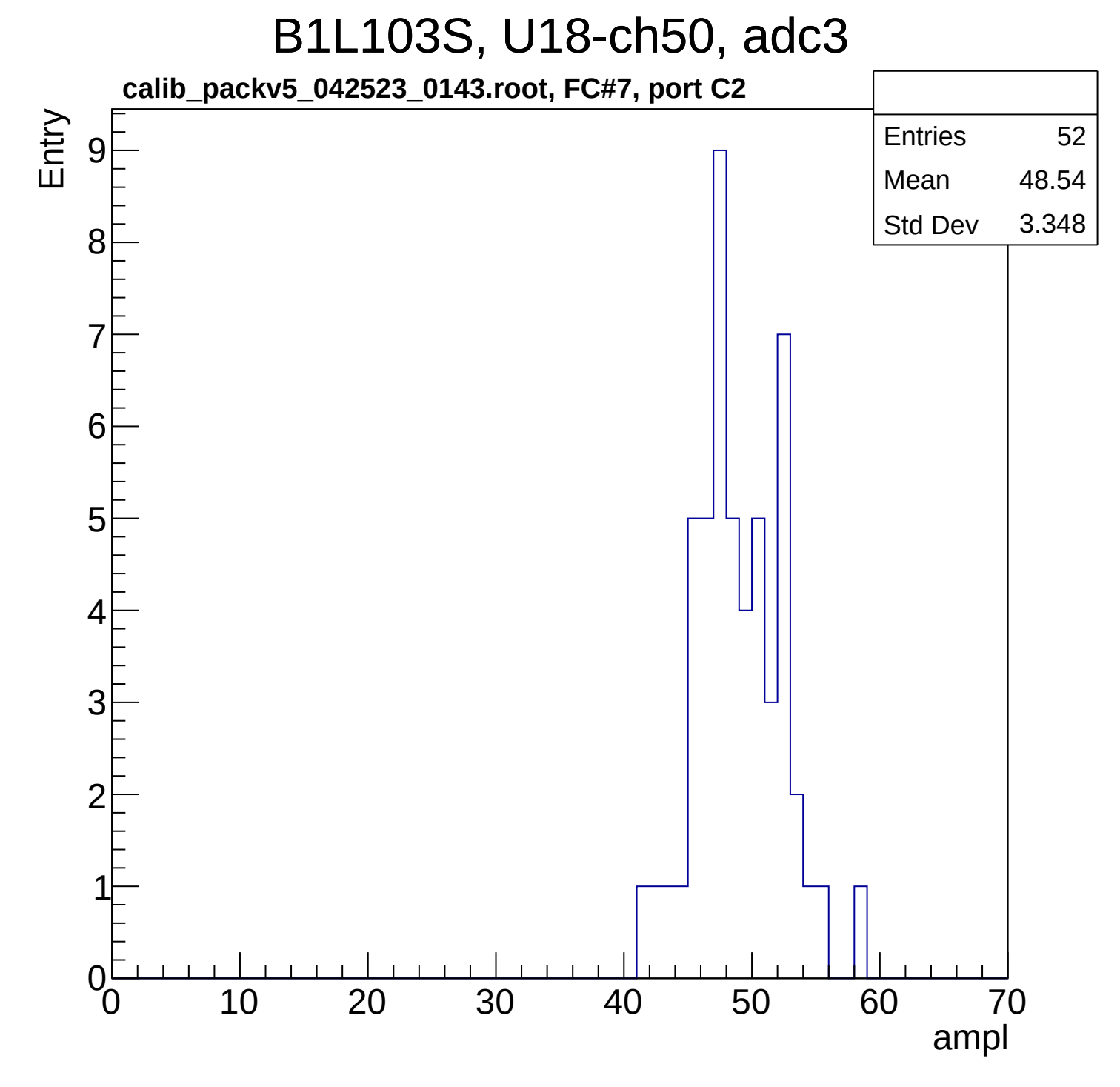
B1L103S, U18-ch50, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 52
Mean 48.54
Std Dev 3.348
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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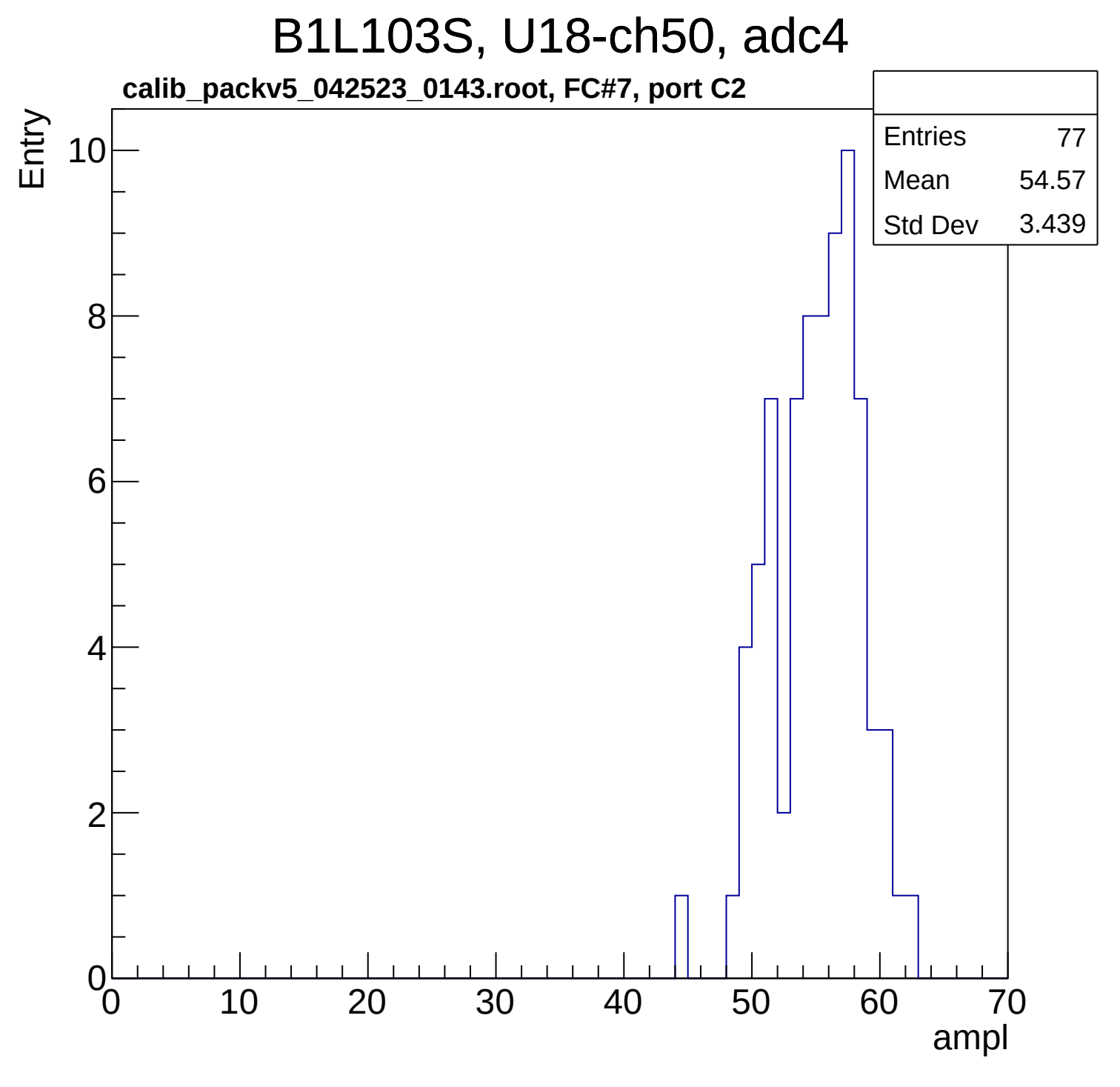
B1L103S, U18-ch50, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 77
Mean 54.57
Std Dev 3.439
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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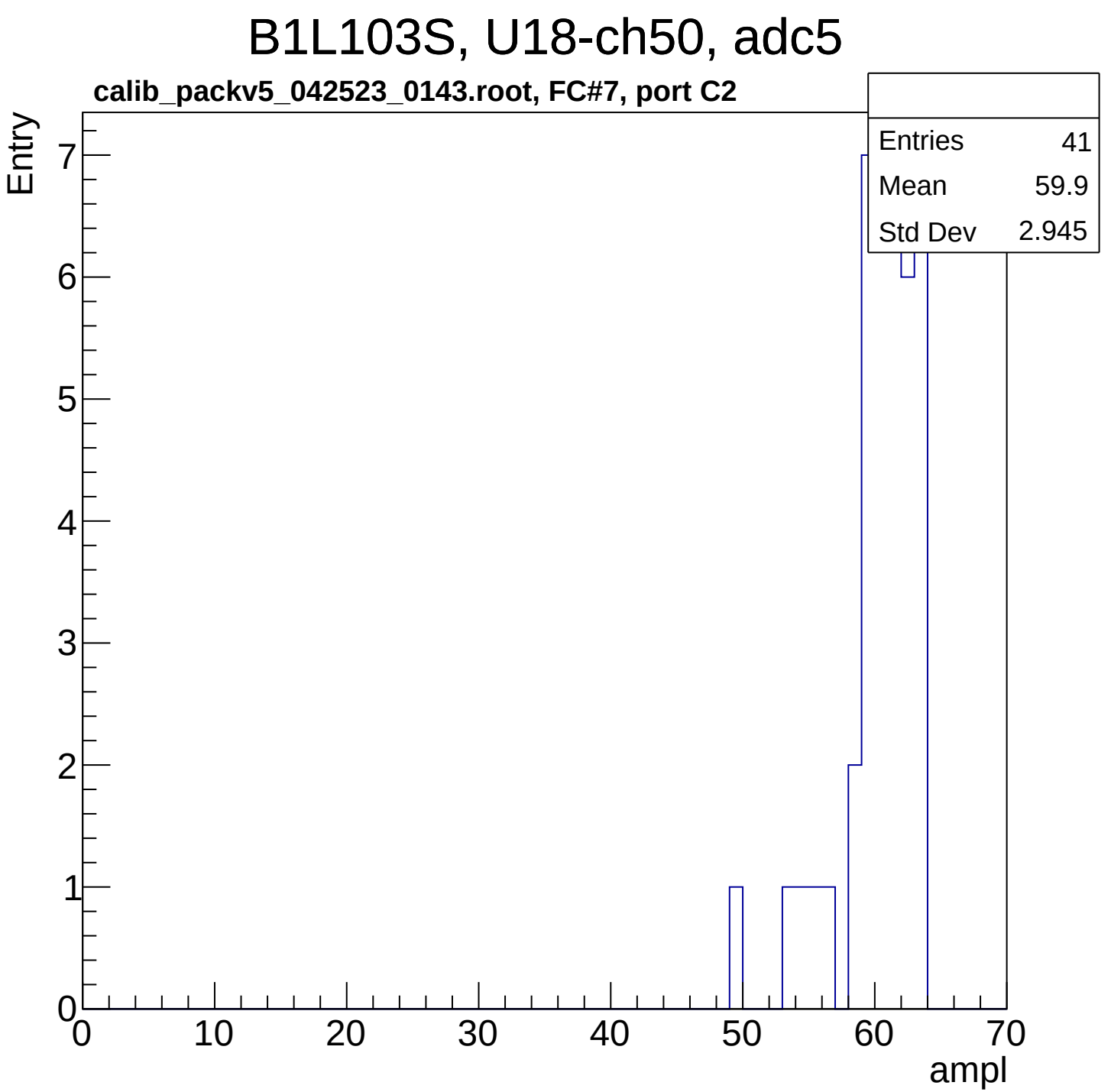
B1L103S, U18-ch50, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 41
Mean 59.9
Std Dev 2.945
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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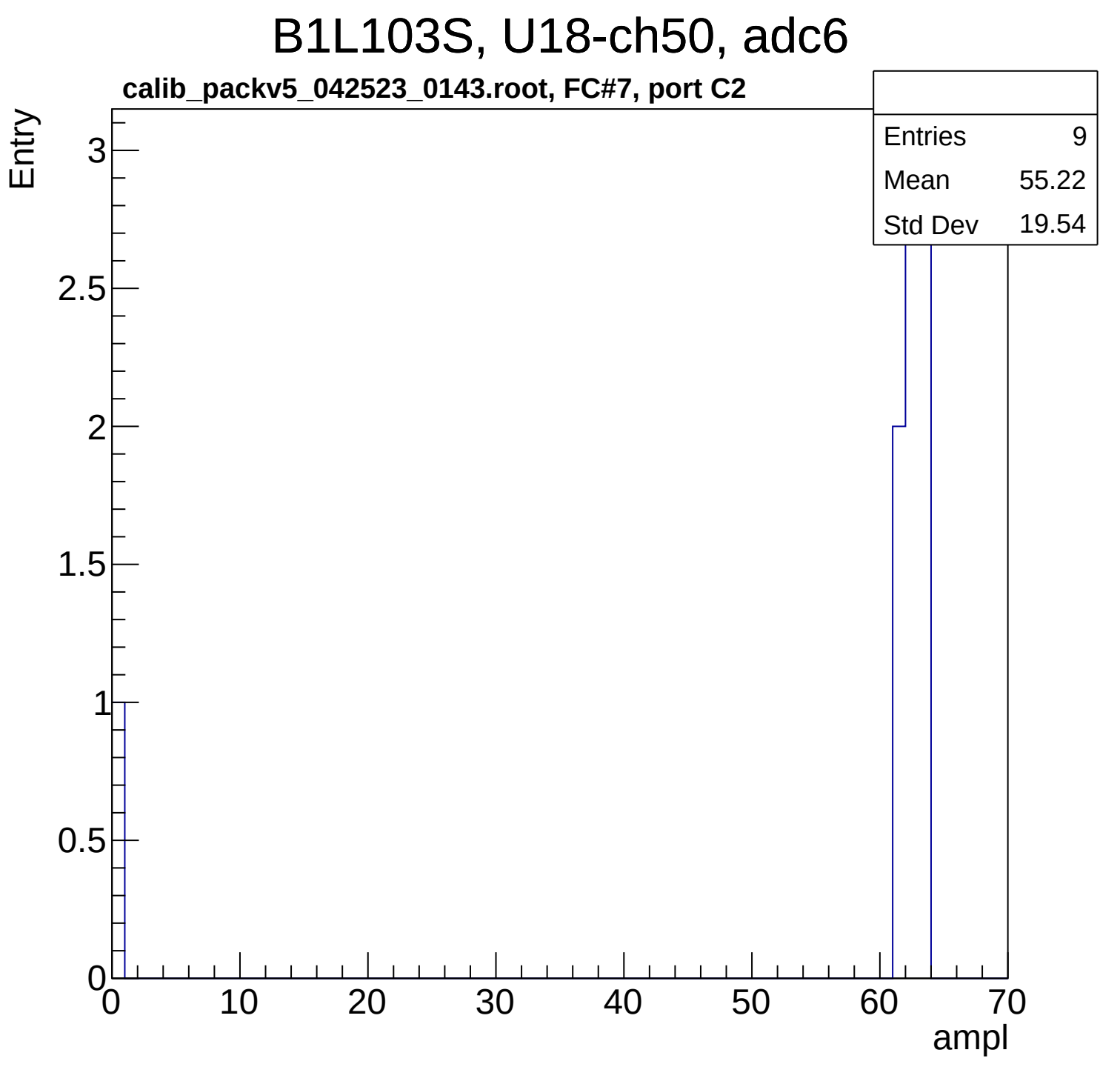
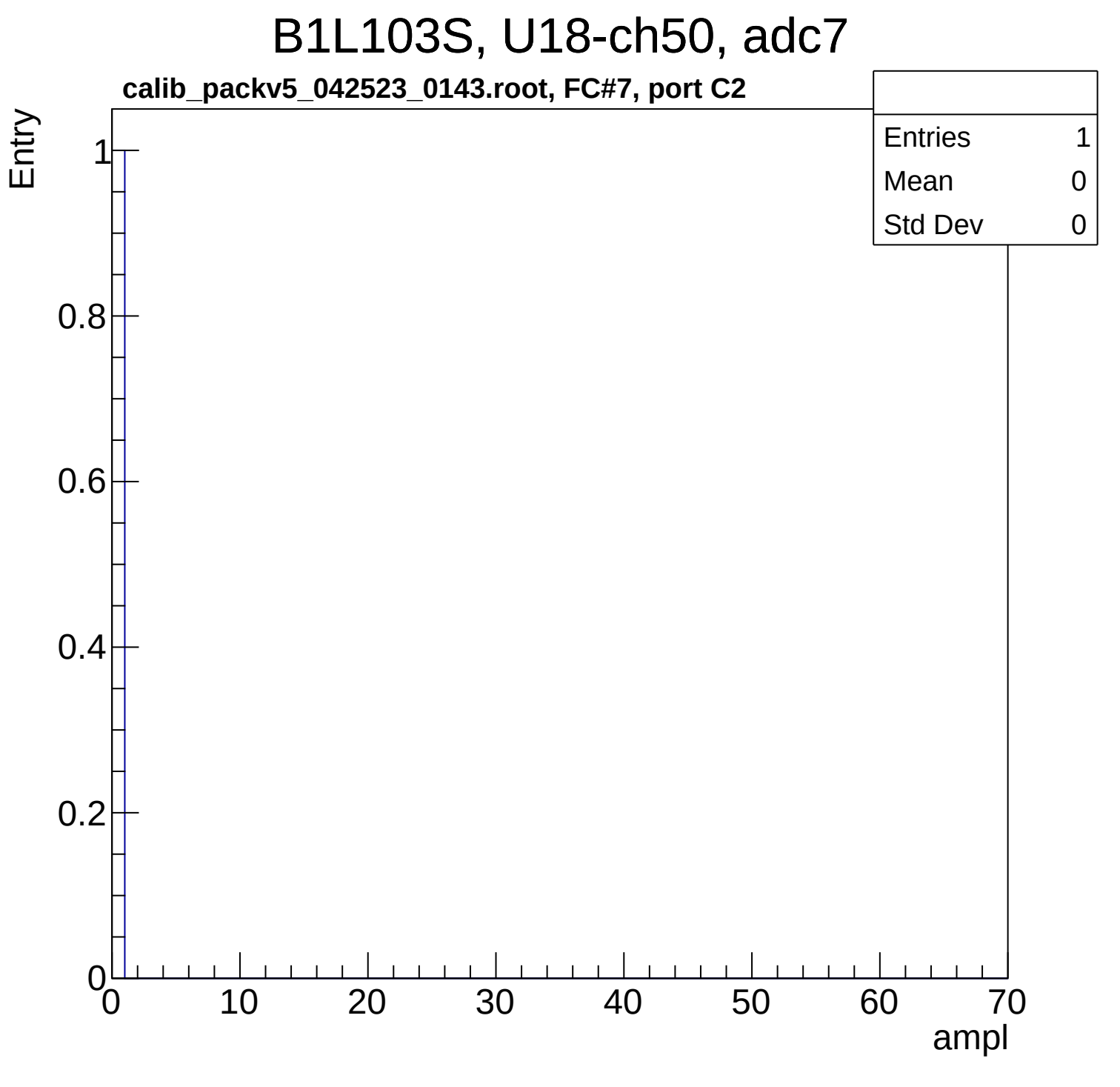
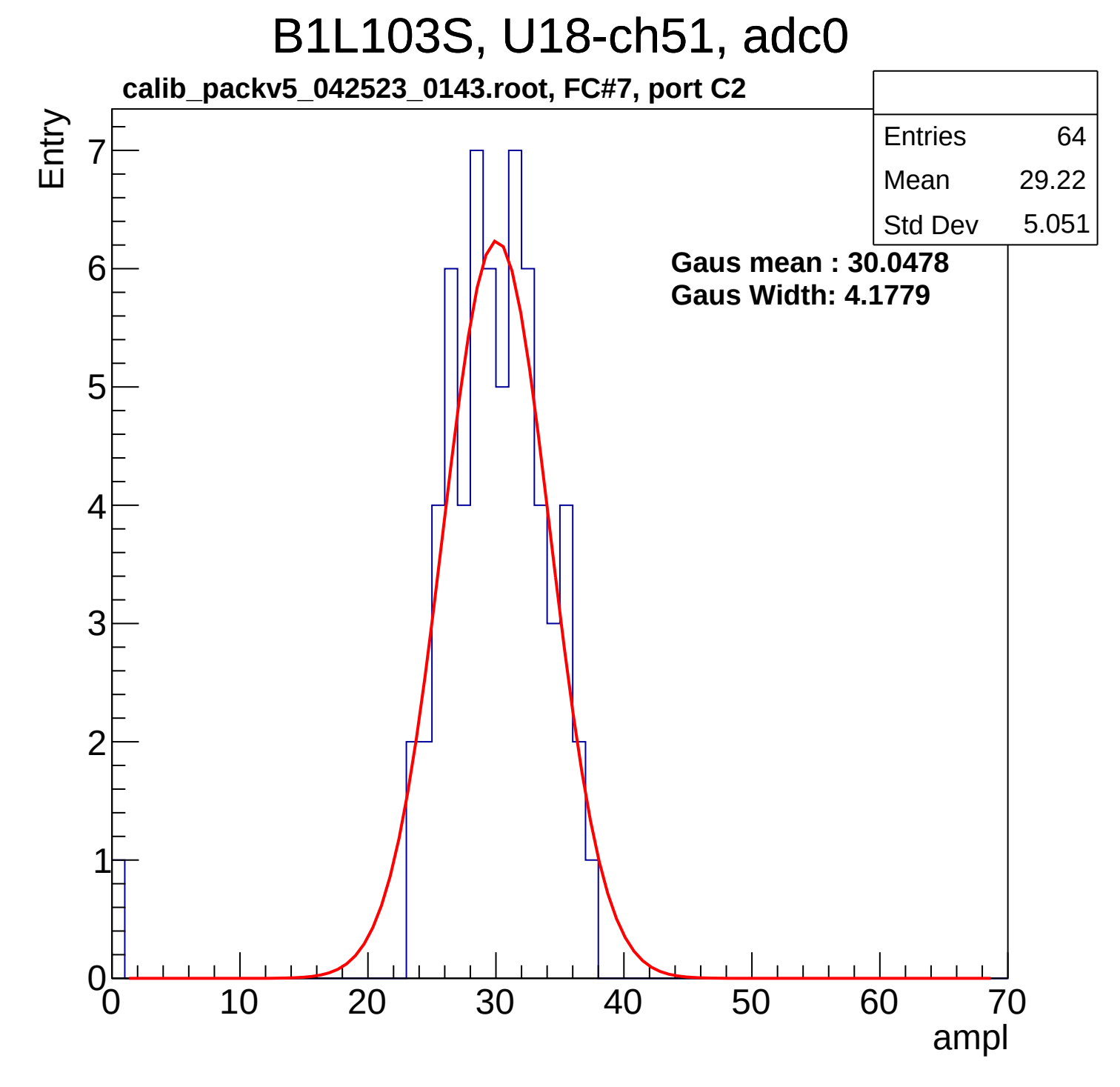
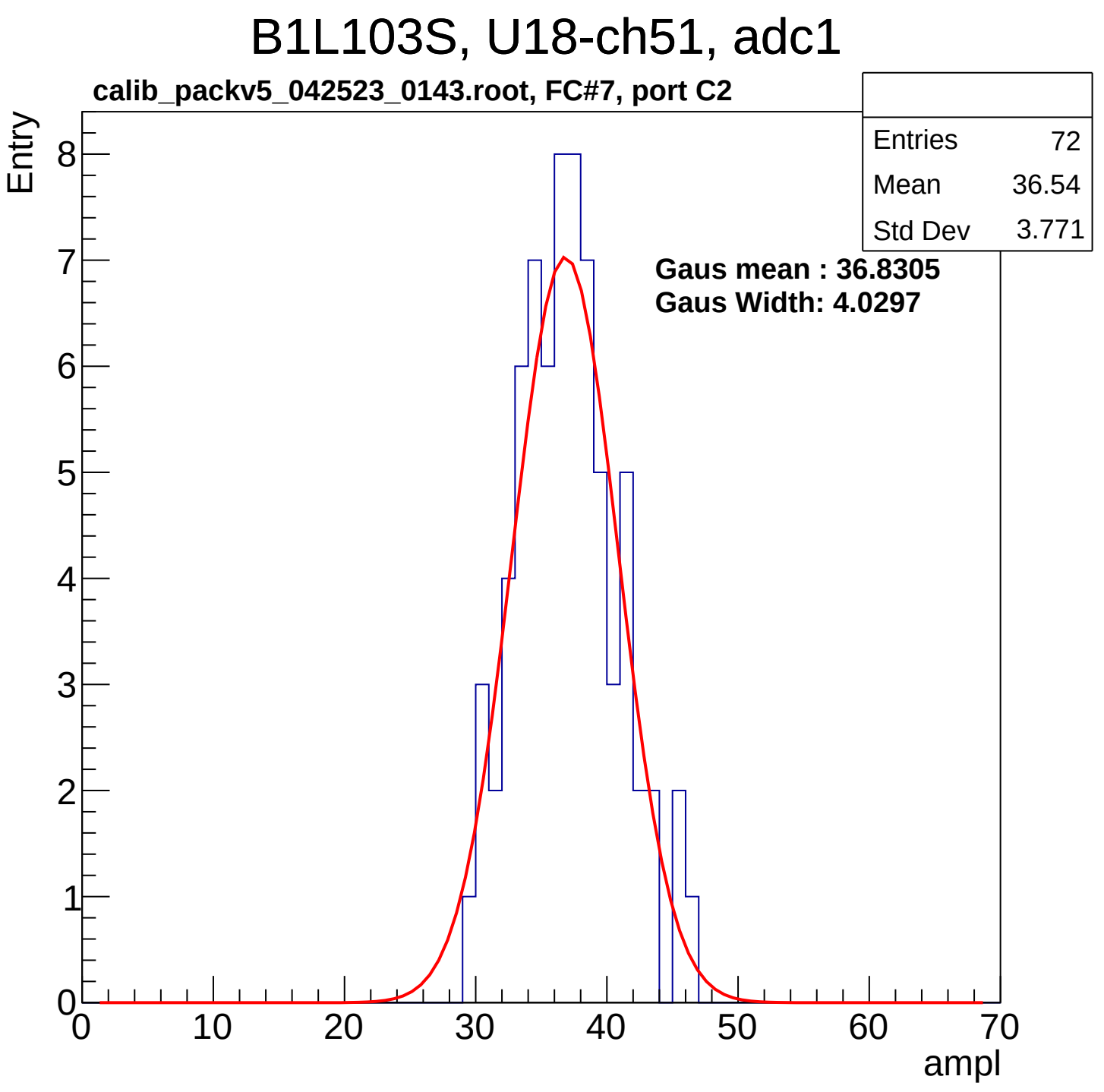
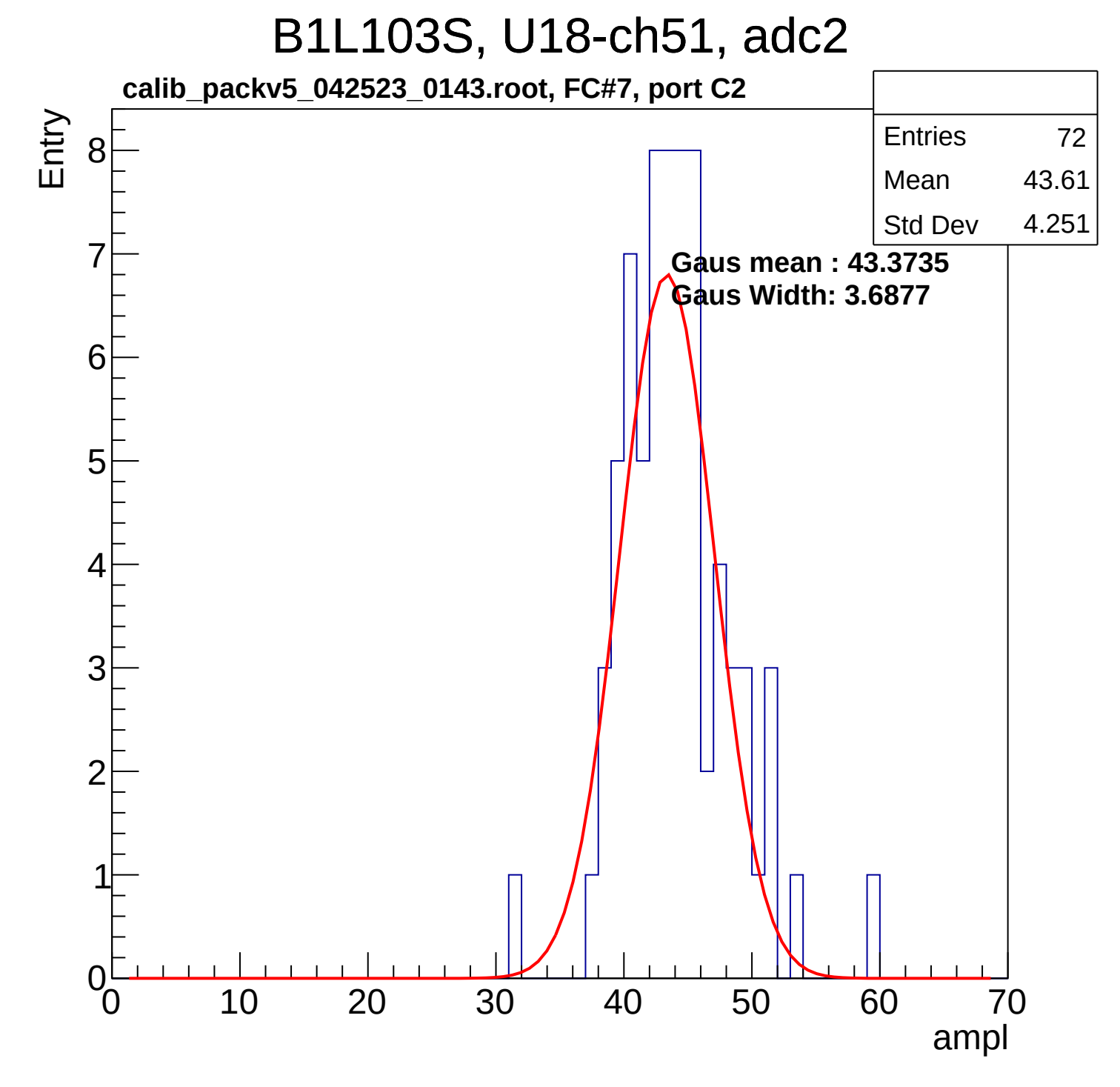
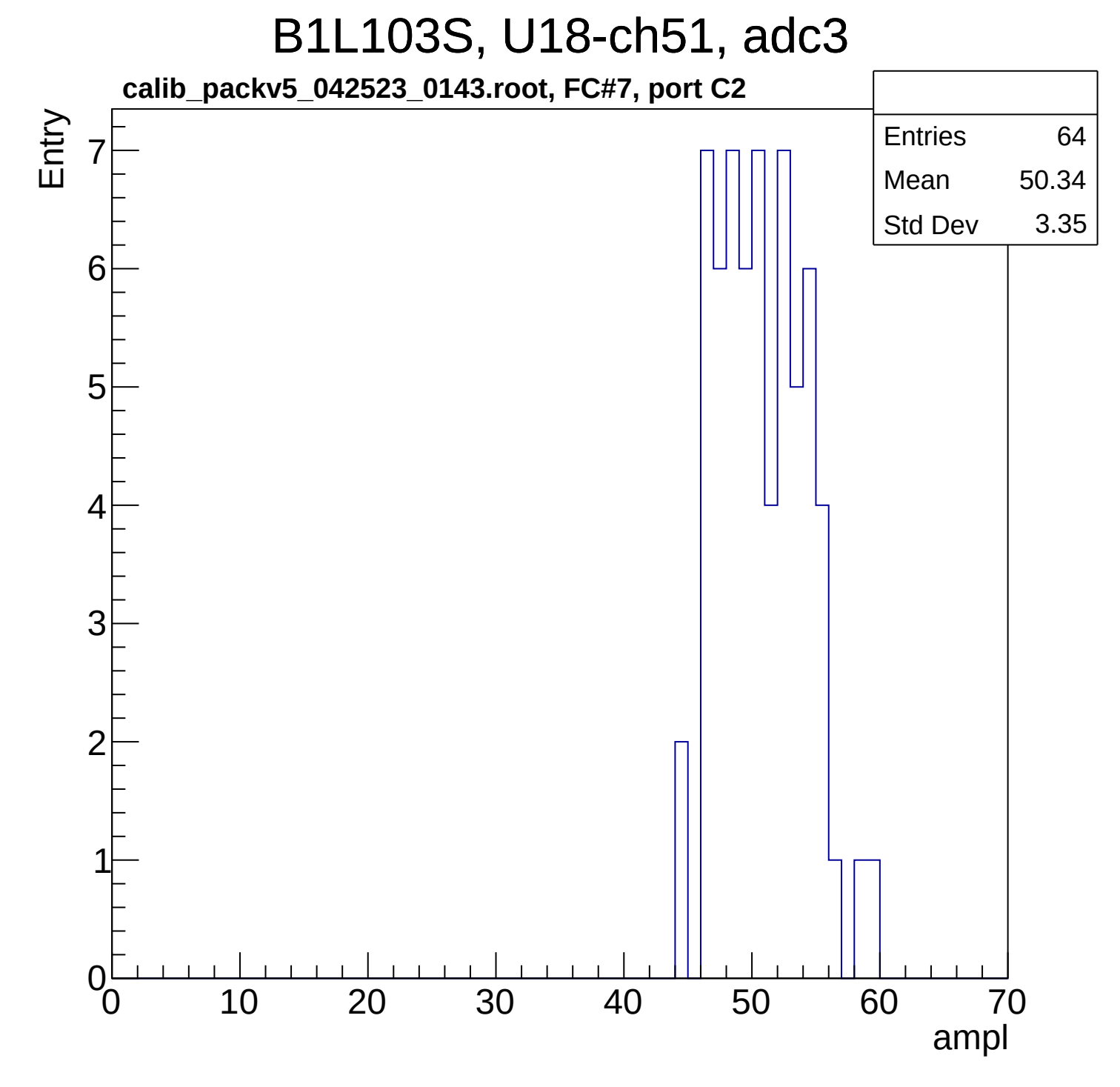

B1L103S, U18-ch50, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 9
Mean 55.22
Std Dev 19.54
Entry
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl

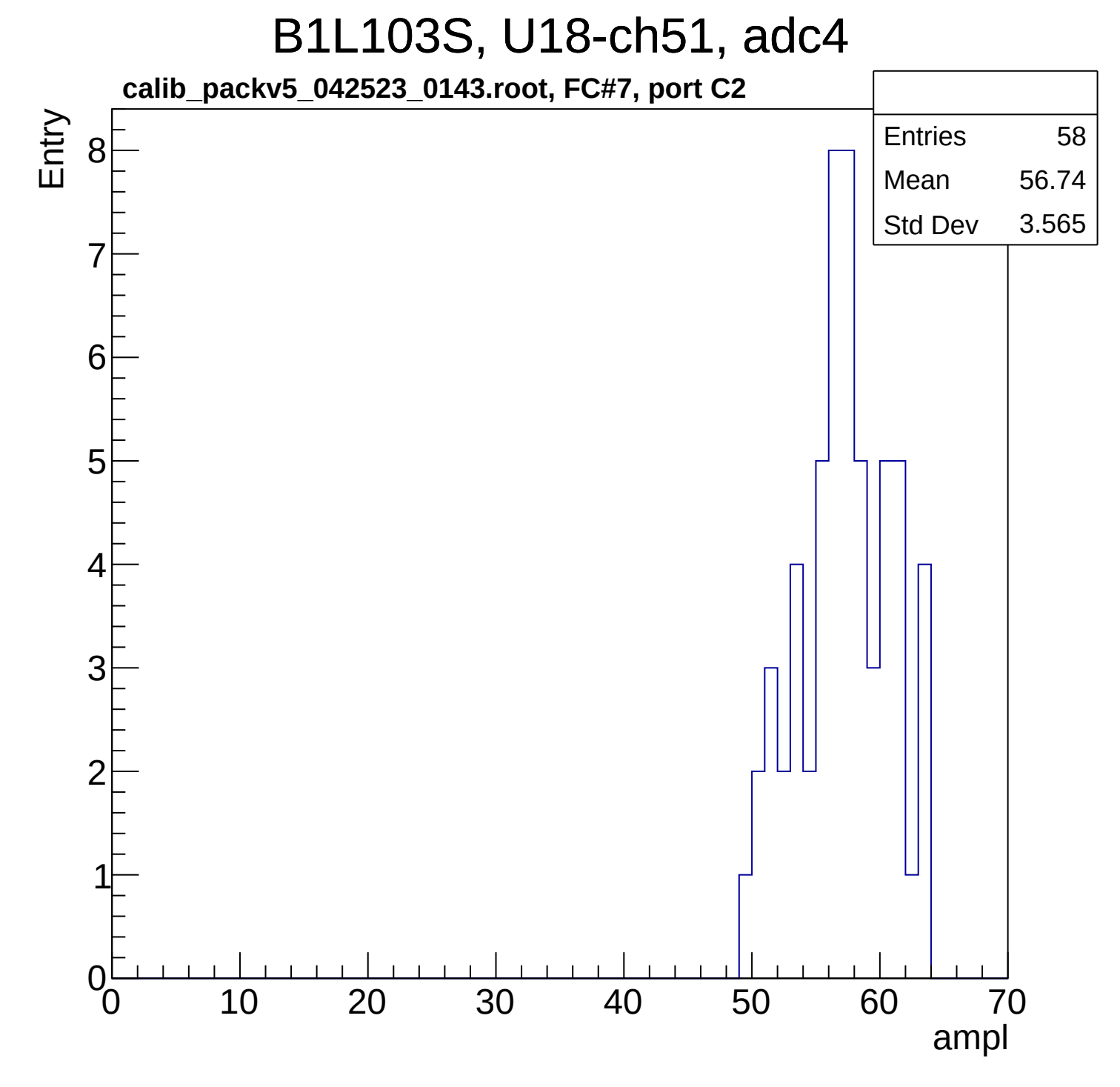

B1L103S, U18-ch50, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

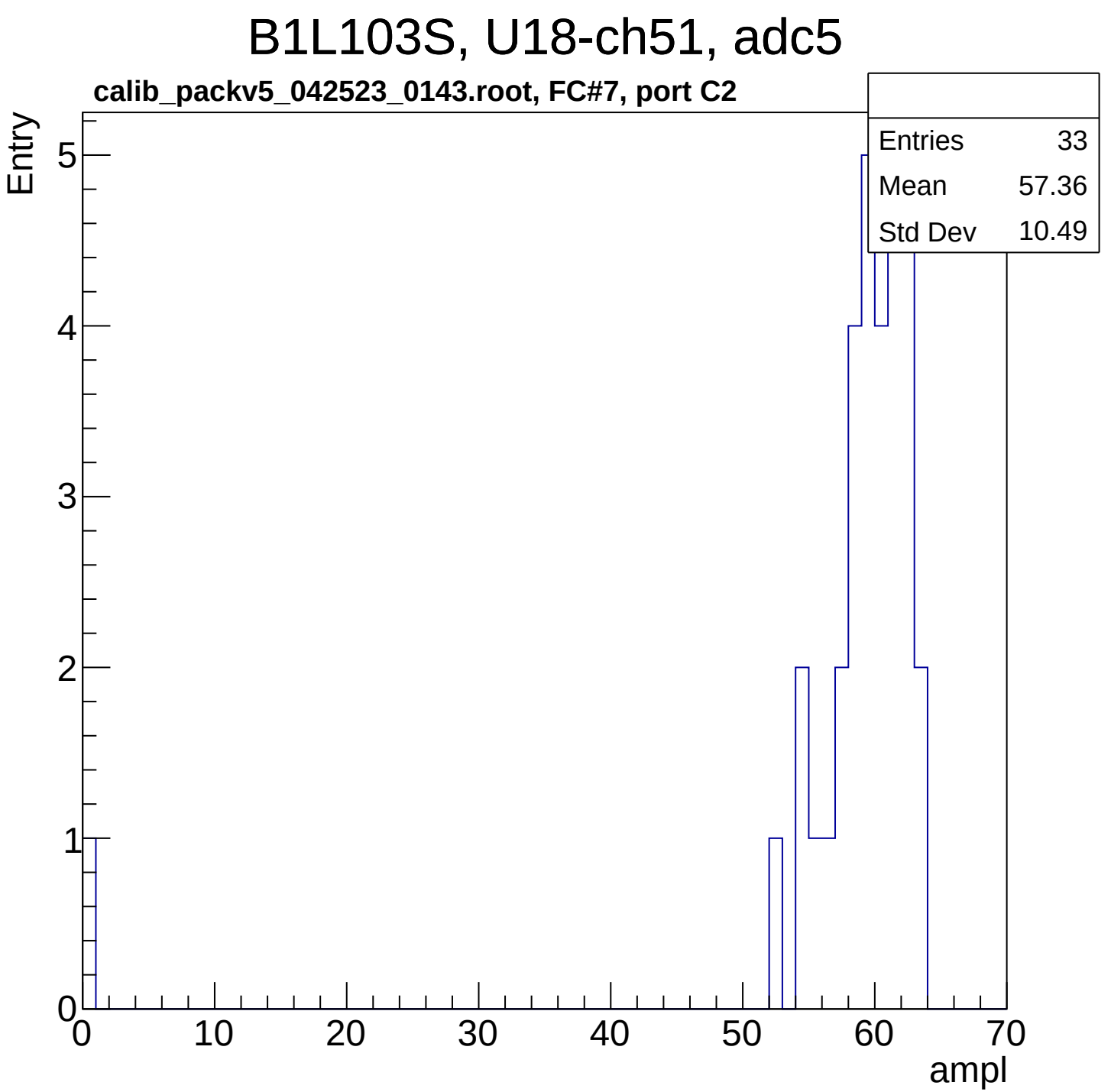

B1L103S, U18-ch51, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 29.22
Std Dev 5.051
Gaus mean : 30.0478
Gaus Width: 4.1779
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

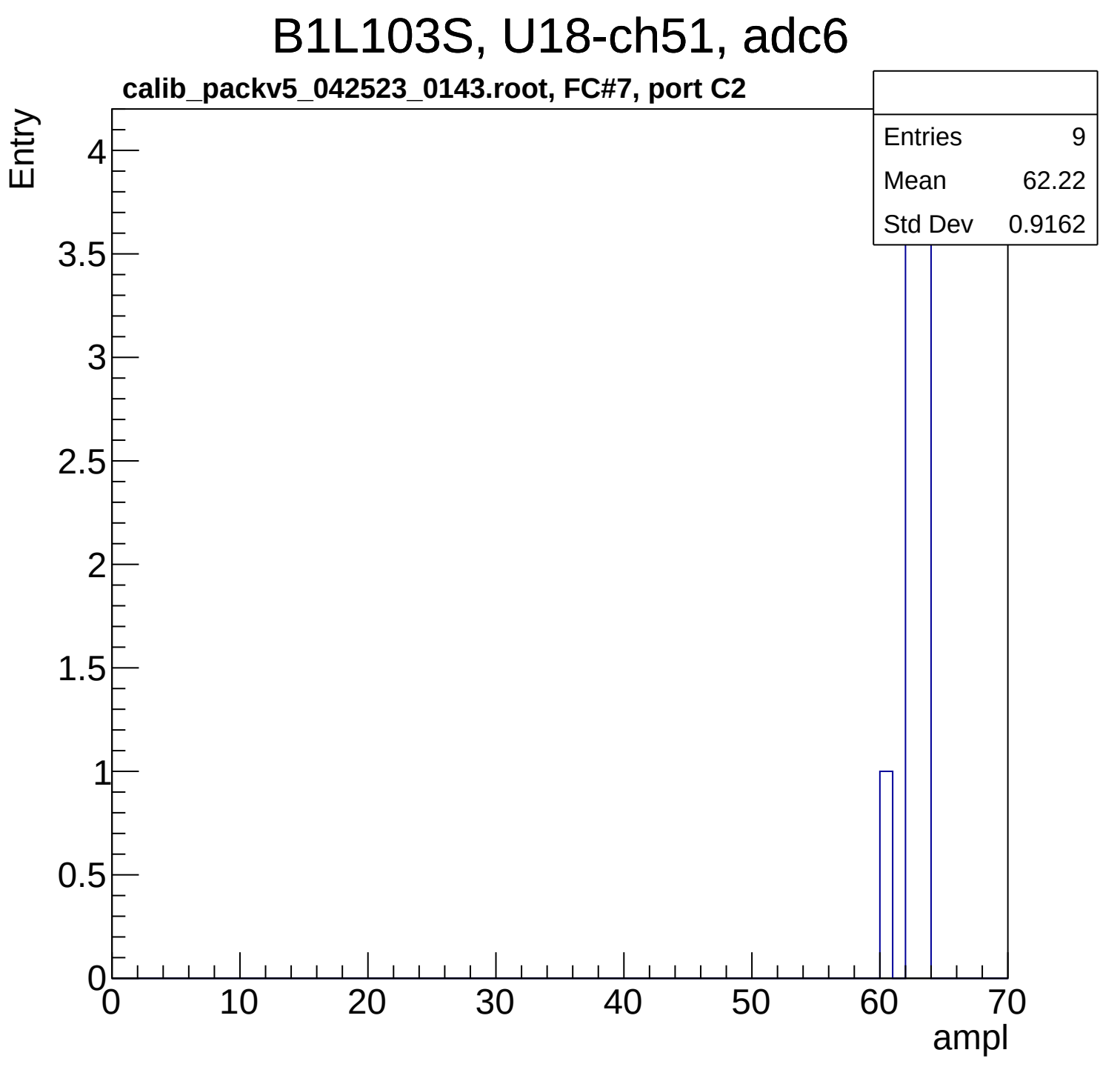

B1L103S, U18-ch51, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 72
Mean 36.54
Std Dev 3.771
Gaus mean : 36.8305
Gaus Width: 4.0297
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

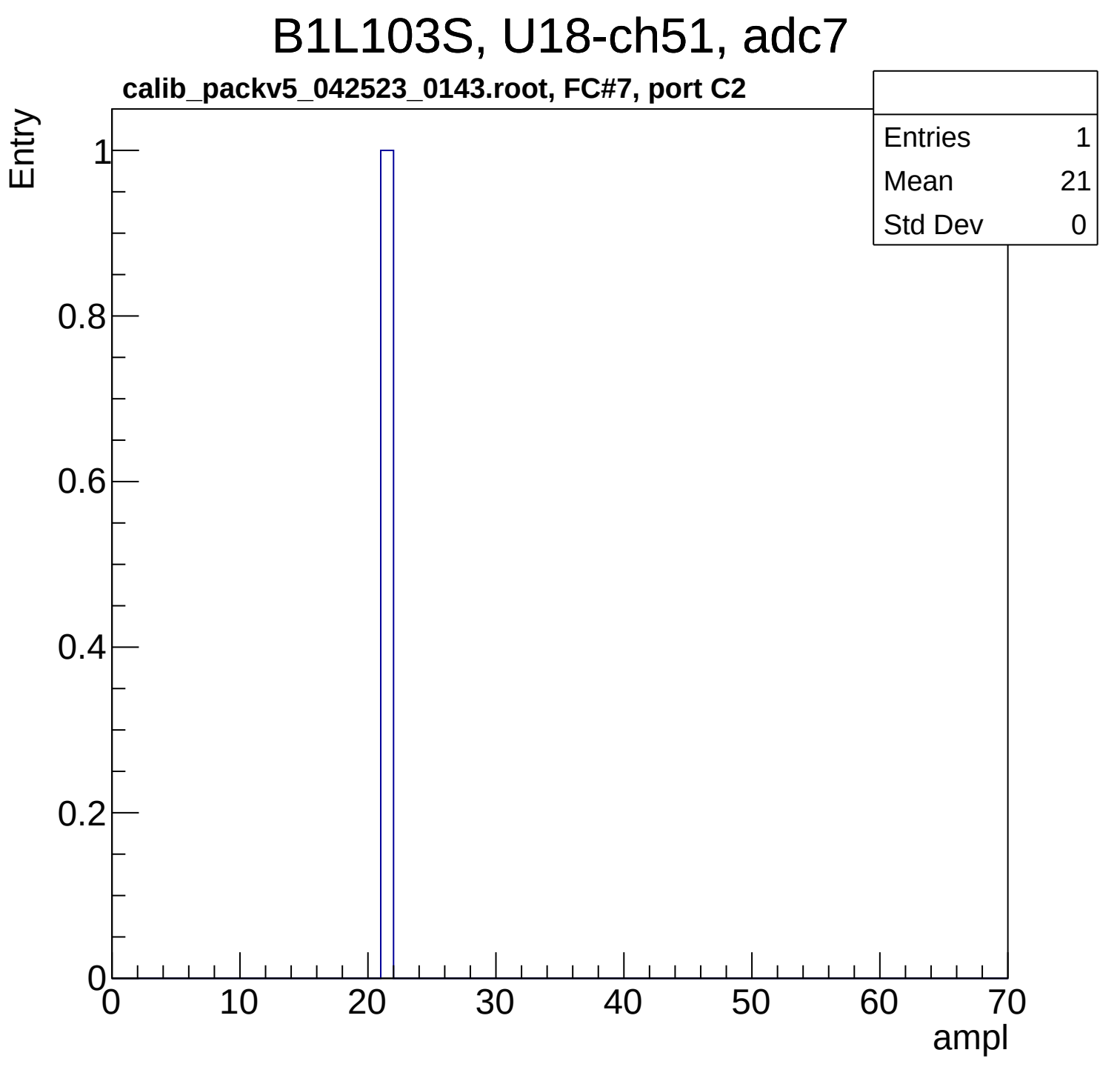

B1L103S, U18-ch51, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 72
Mean 43.61
Std Dev 4.251
Gaus mean : 43.3735
Gaus Width: 3.6877
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch51, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 50.34
Std Dev 3.35
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch51, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 58
Mean 56.74
Std Dev 3.565
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch51, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 33
Mean 57.36
Std Dev 10.49
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch51, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 9
Mean 62.22
Std Dev 0.9162
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U18-ch51, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 21
Std Dev 0
Entry
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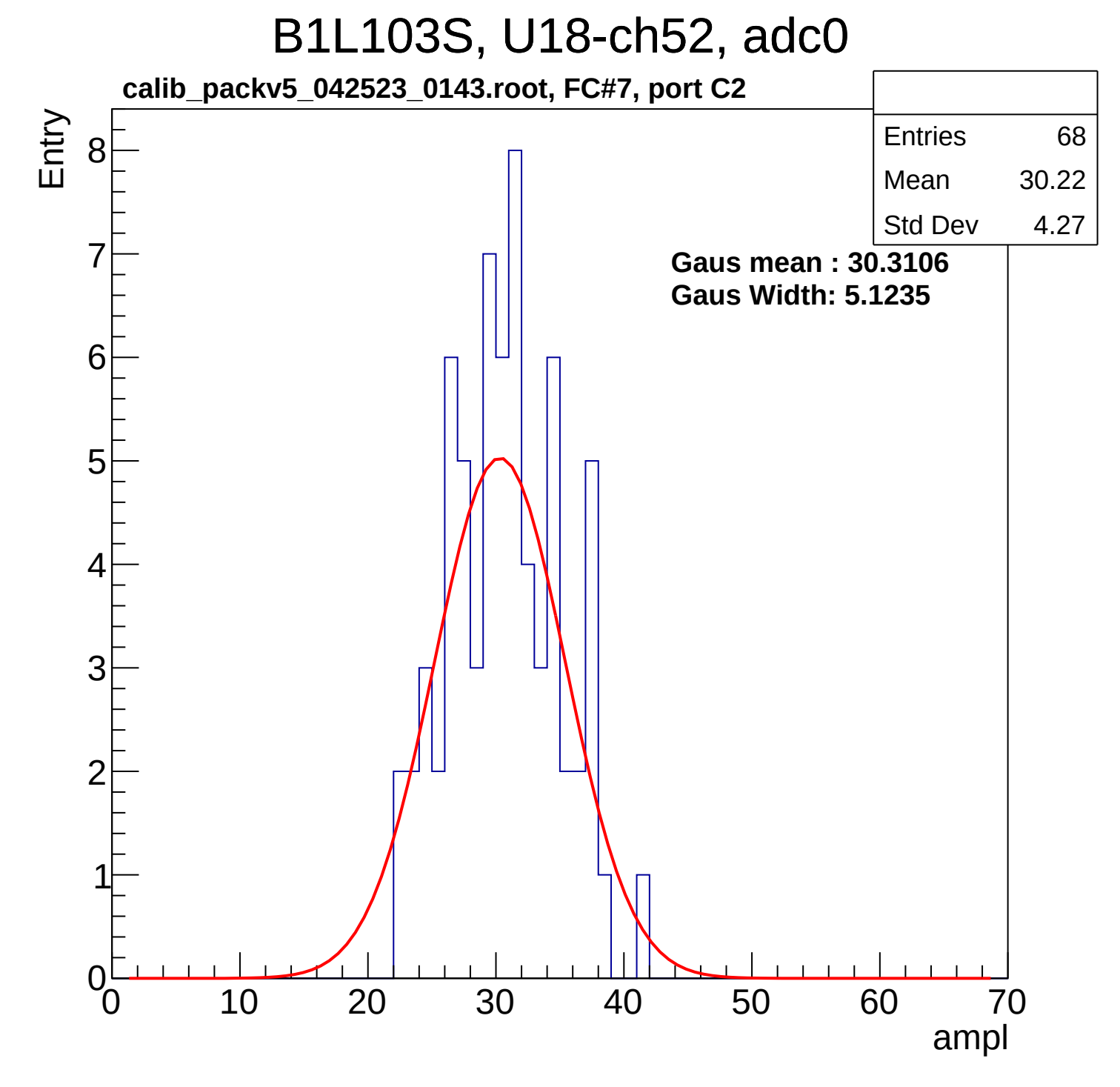
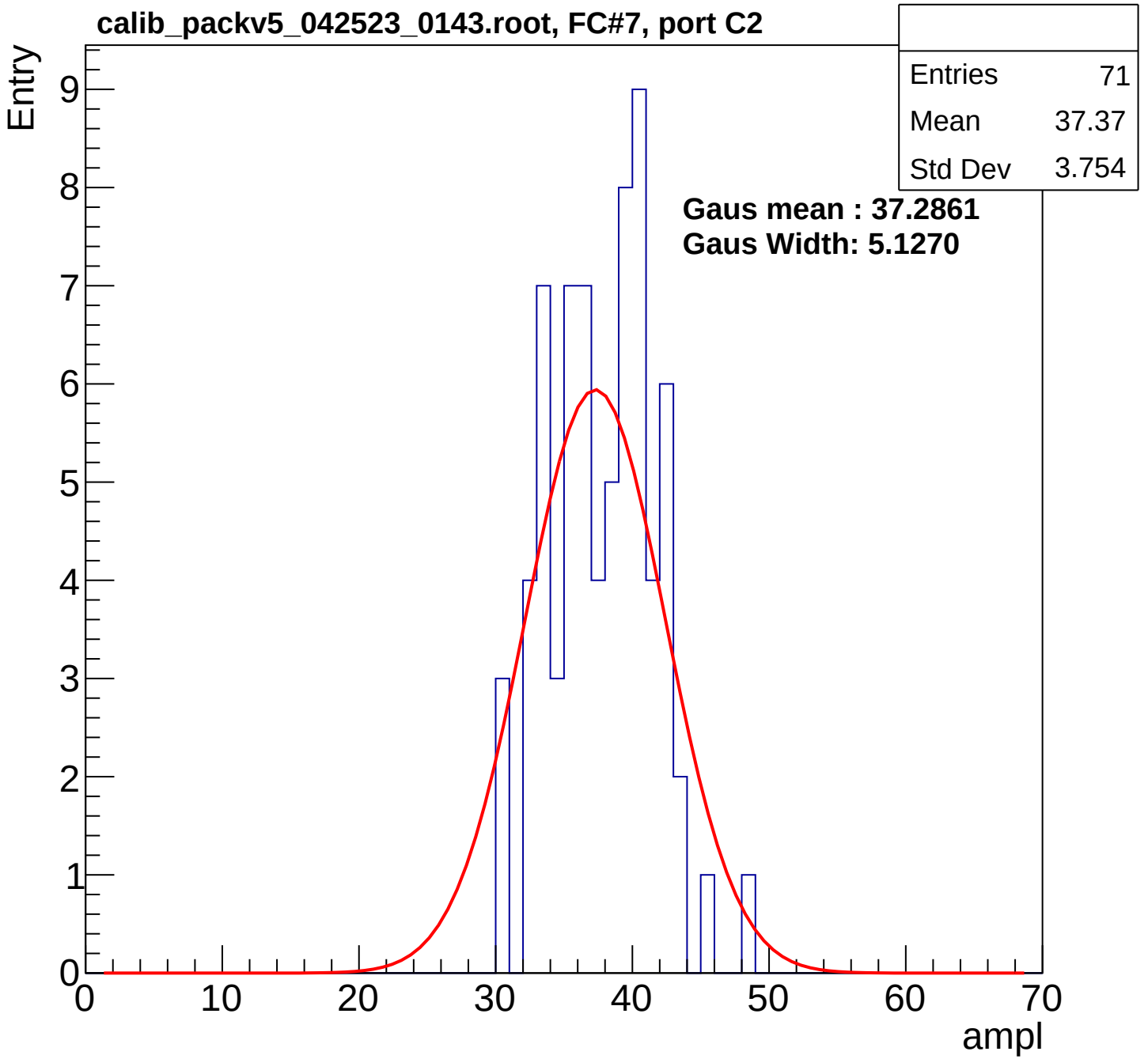
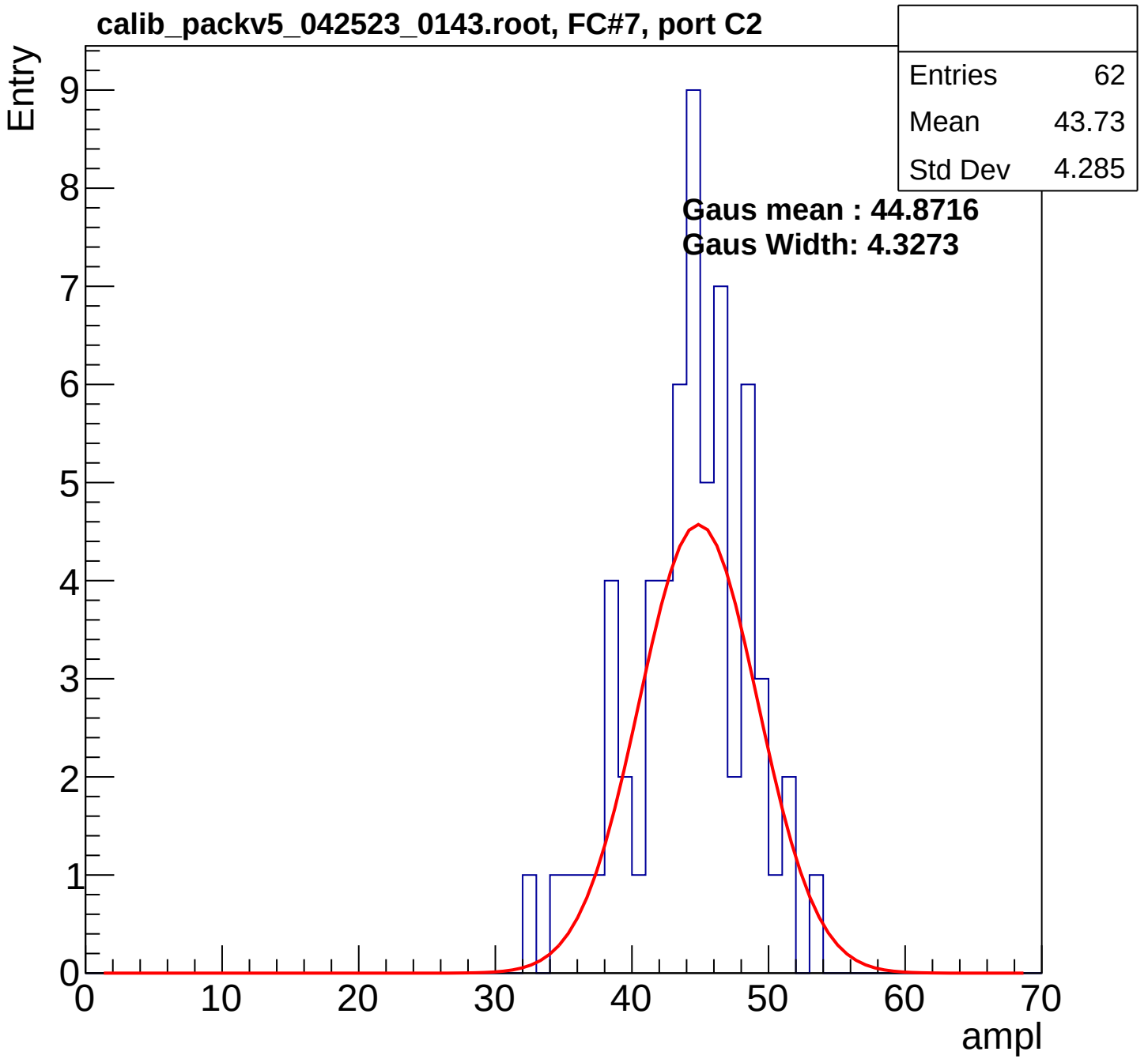
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch52, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 30.22
Std Dev 4.27
Gaus mean : 30.3106
Gaus Width: 5.1235
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch52, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 71
Mean 37.37
Std Dev 3.754
Gaus mean : 37.2861
Gaus Width: 5.1270
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch52, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 62
Mean 43.73
Std Dev 4.285
Gaus mean : 44.8716
Gaus Width: 4.3273
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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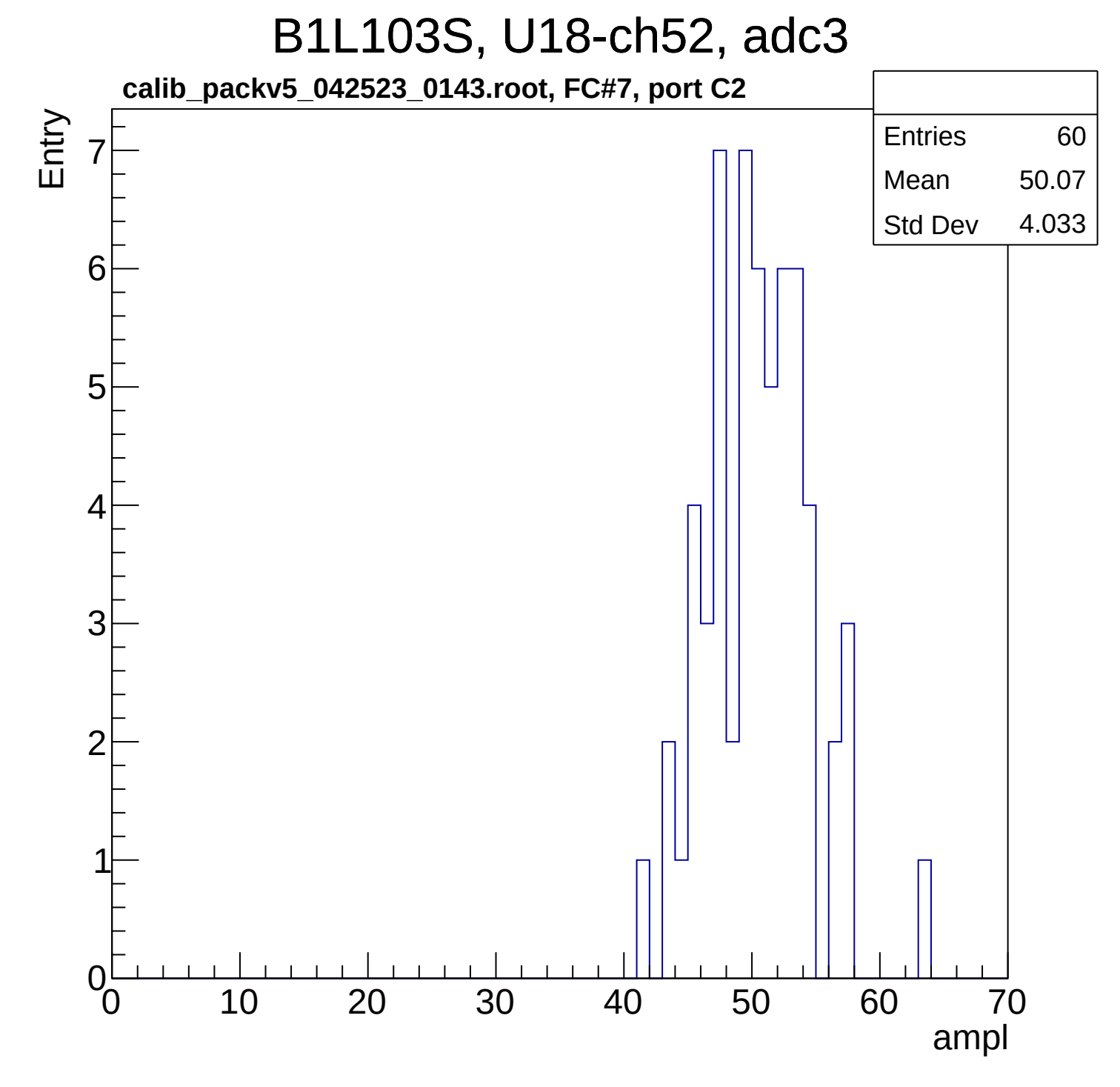
B1L103S, U18-ch52, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 60
Mean 50.07
Std Dev 4.033
Entry
ampl
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1
2
3
4
5
6
7
0
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20
30
40
50
60
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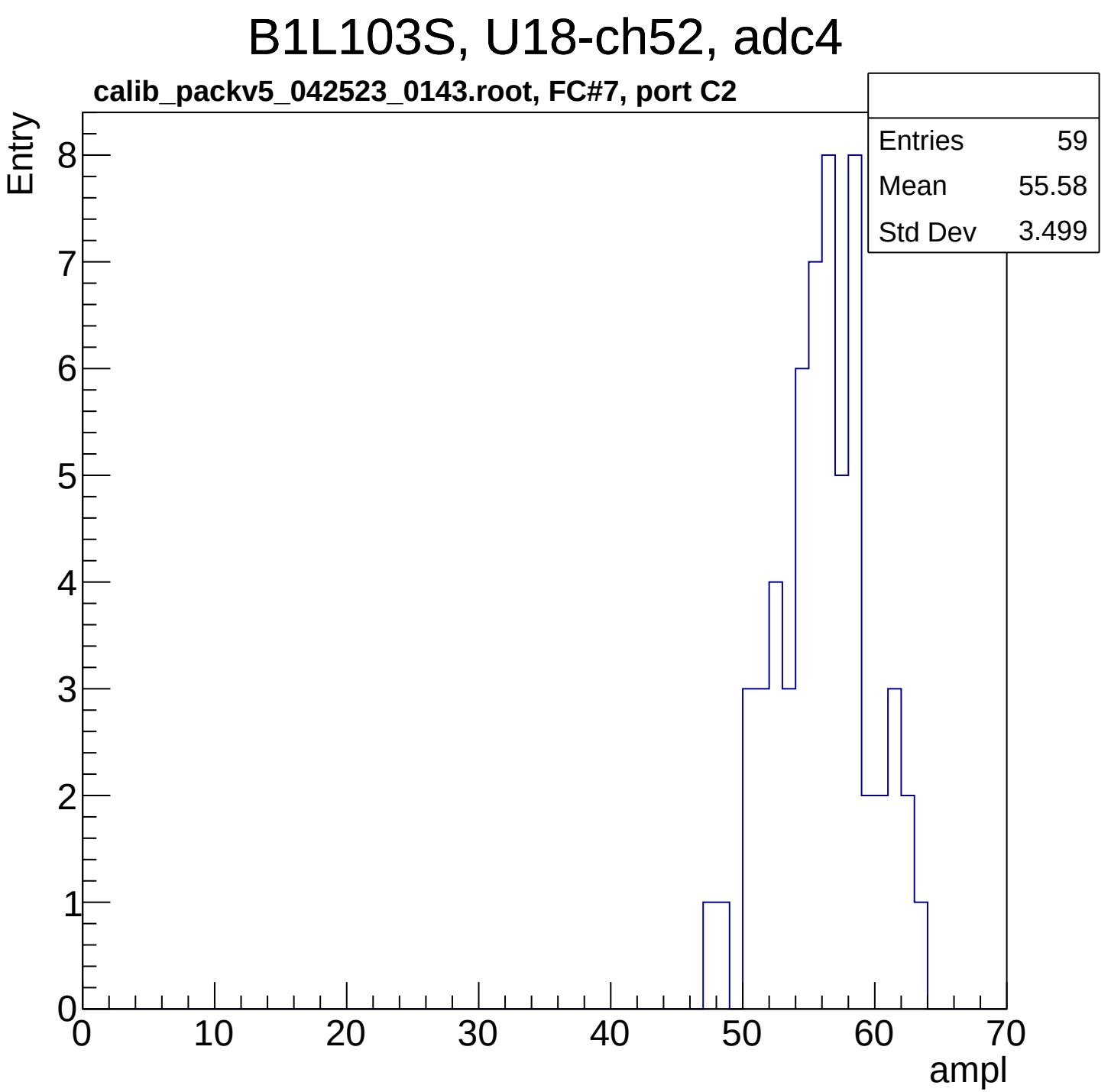
B1L103S, U18-ch52, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 55.58
Std Dev 3.499
Entry
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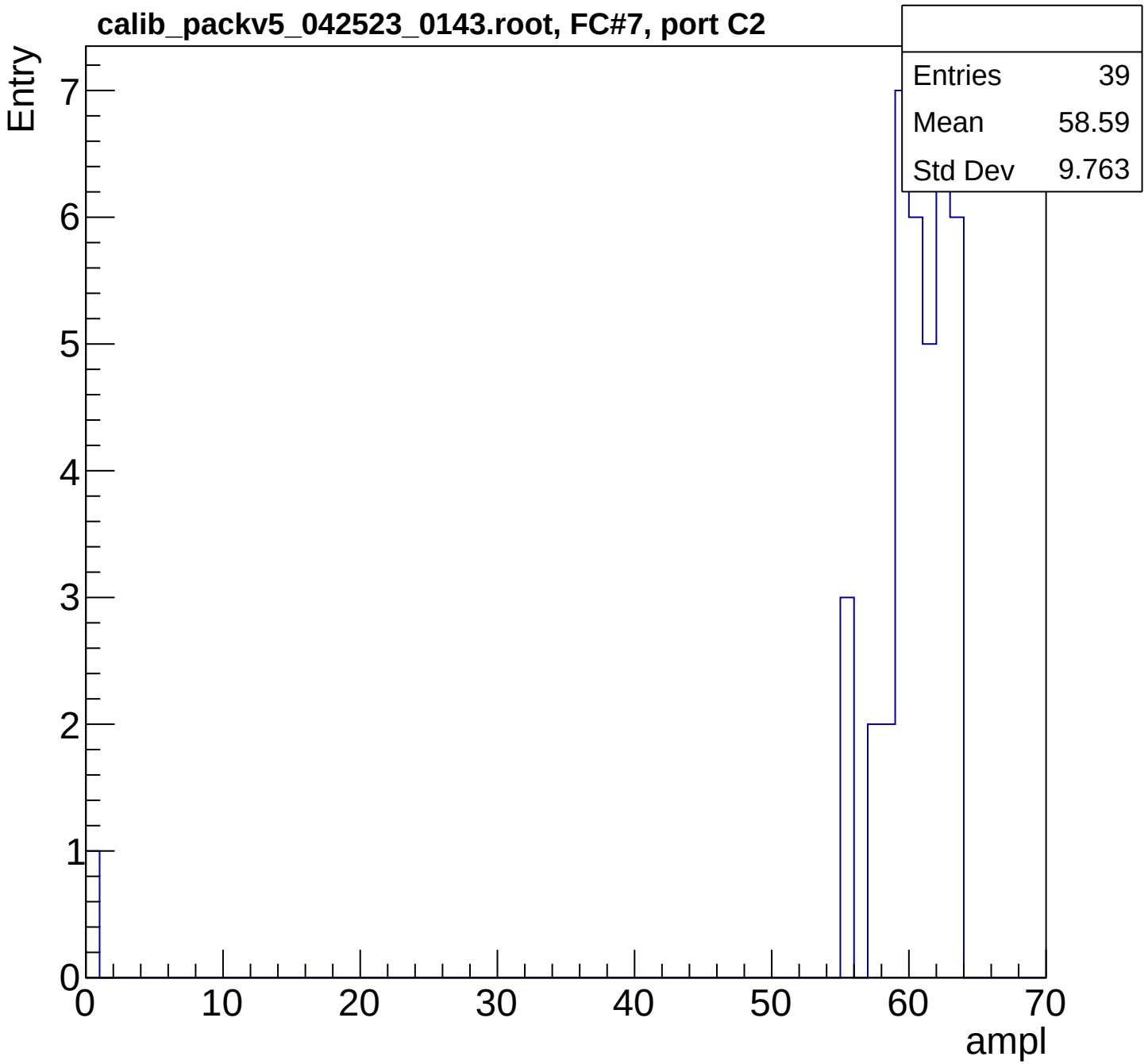
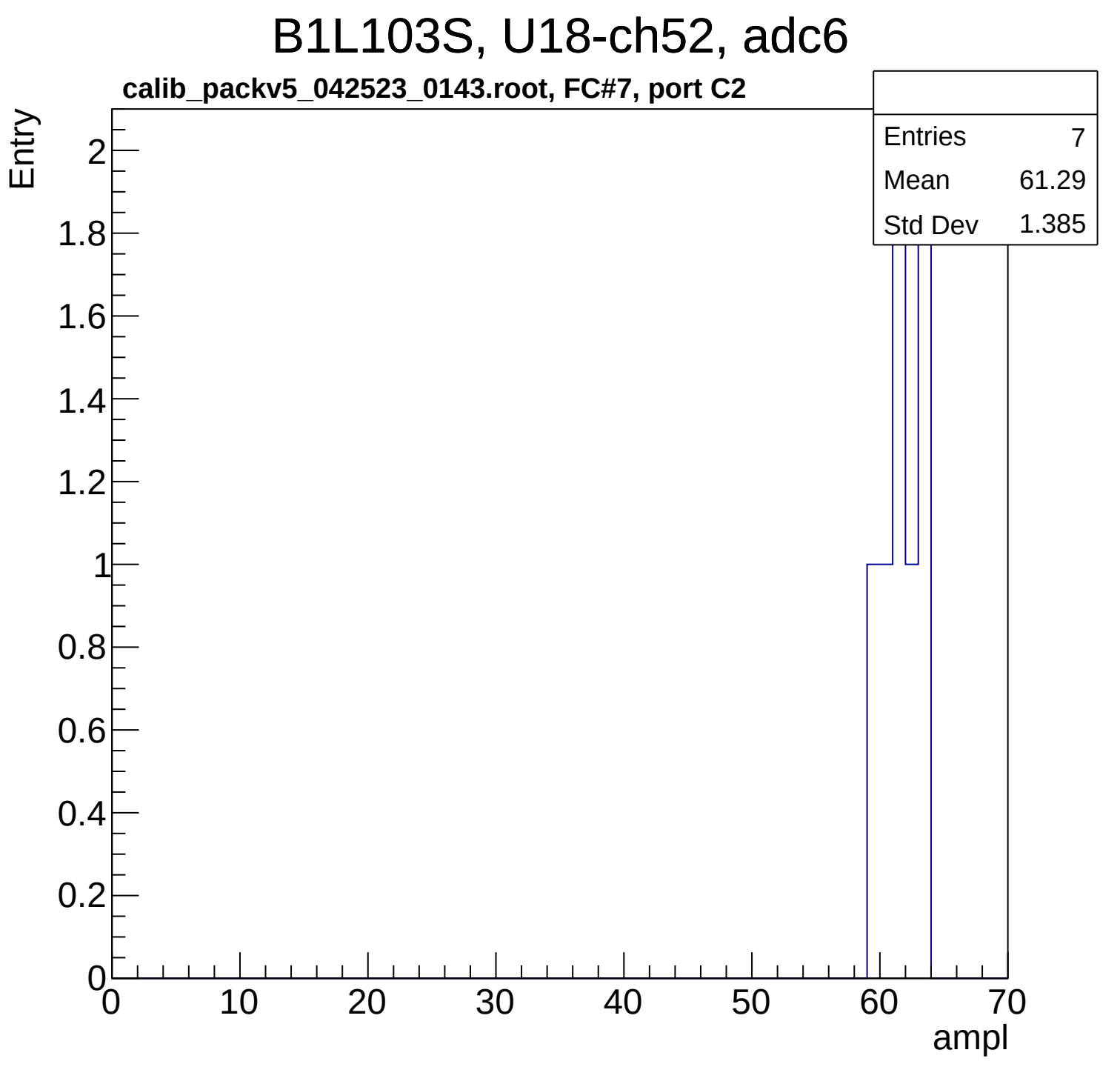
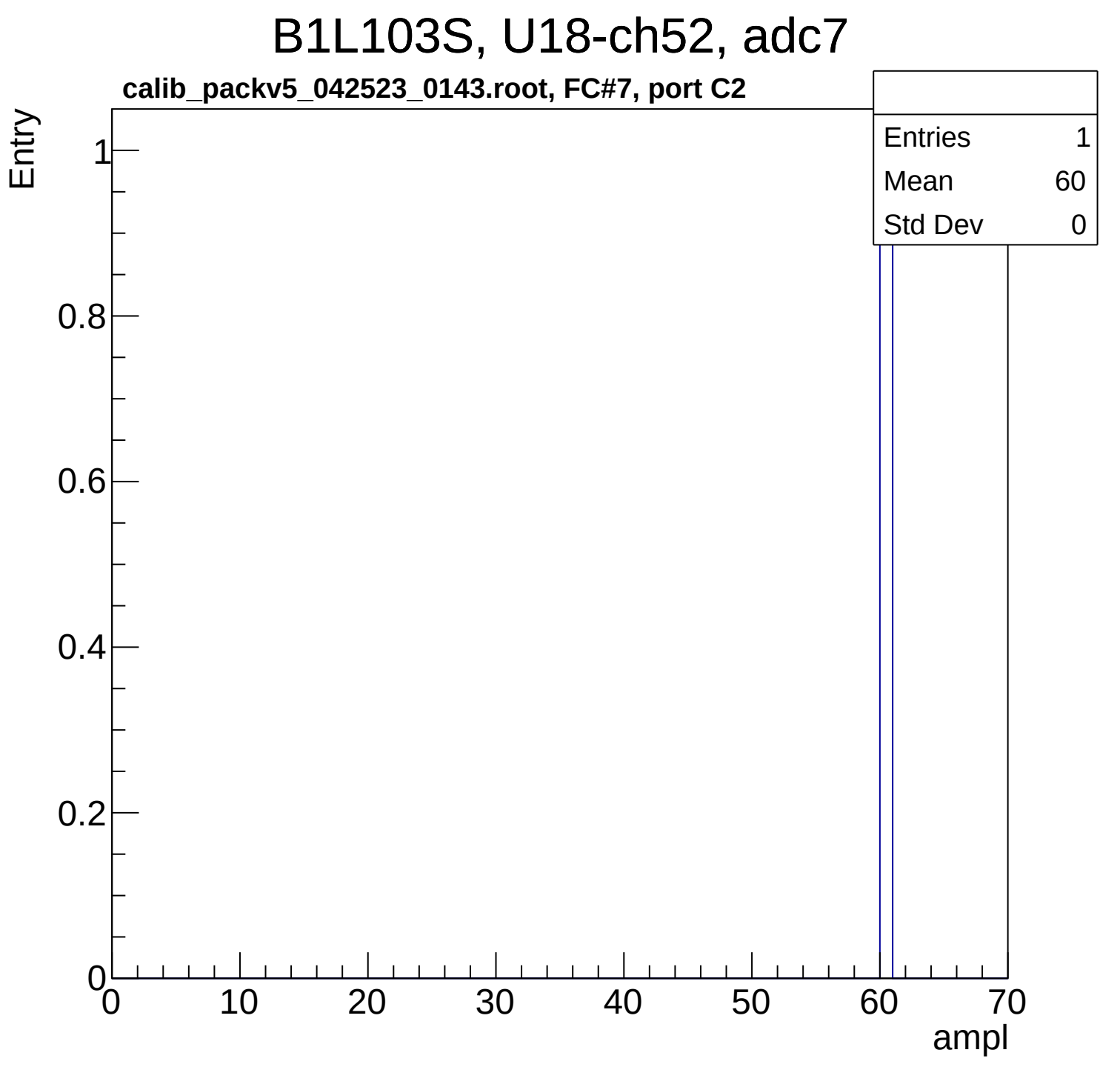
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch52, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 39
Mean 58.59
Std Dev 9.763
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch52, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 7
Mean 61.29
Std Dev 1.385
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U18-ch52, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 60
Std Dev 0
Entry
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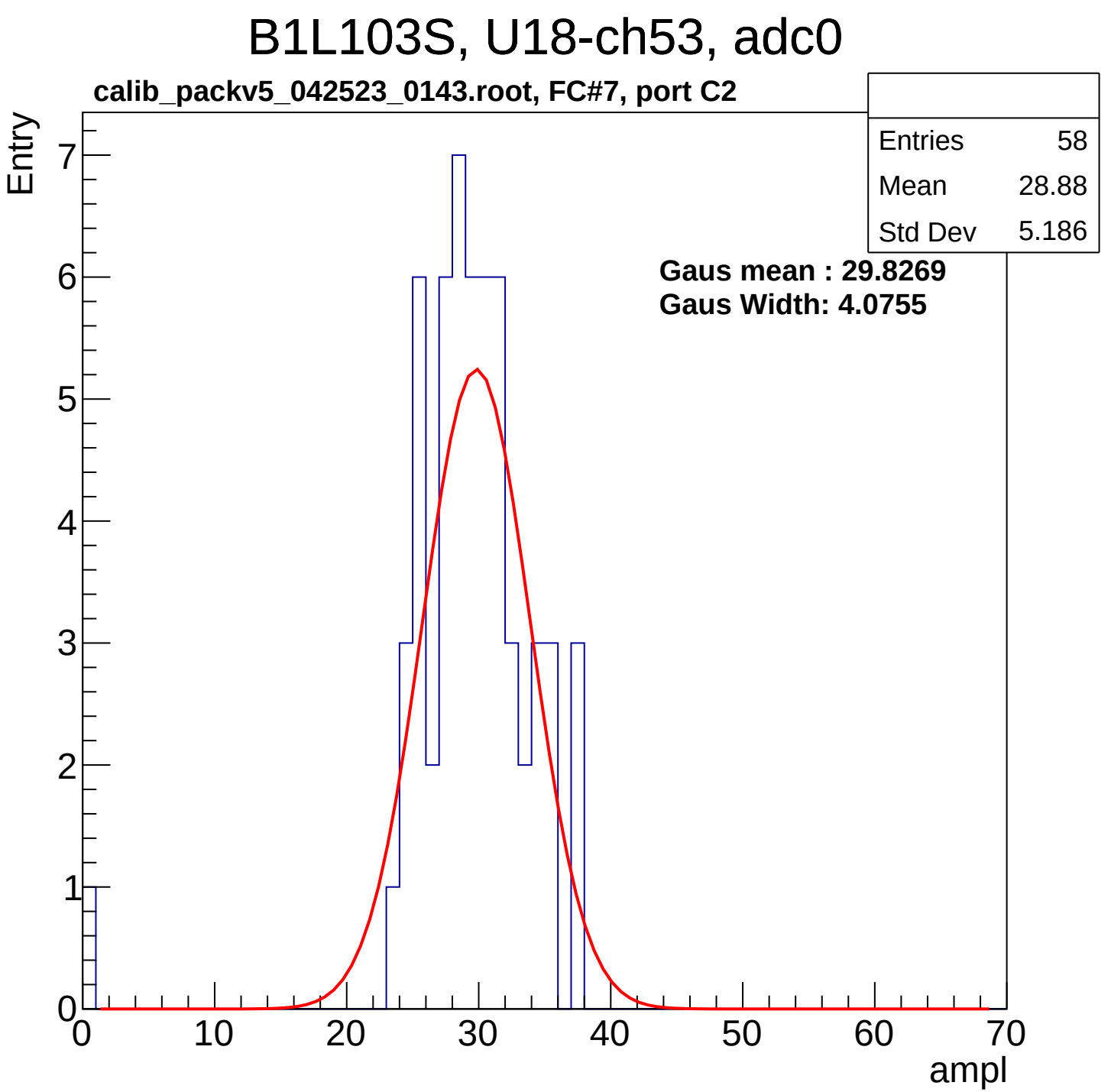
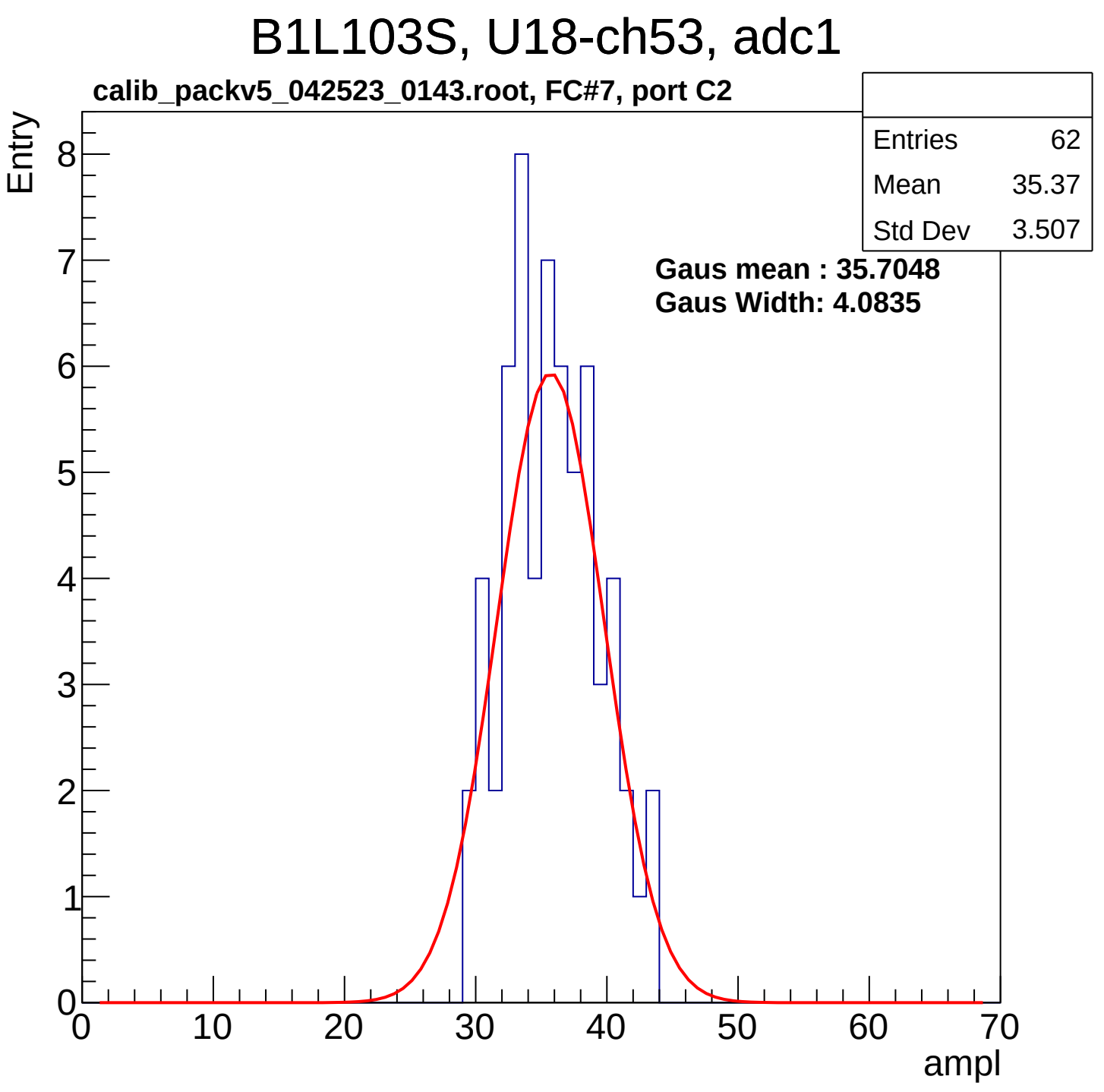
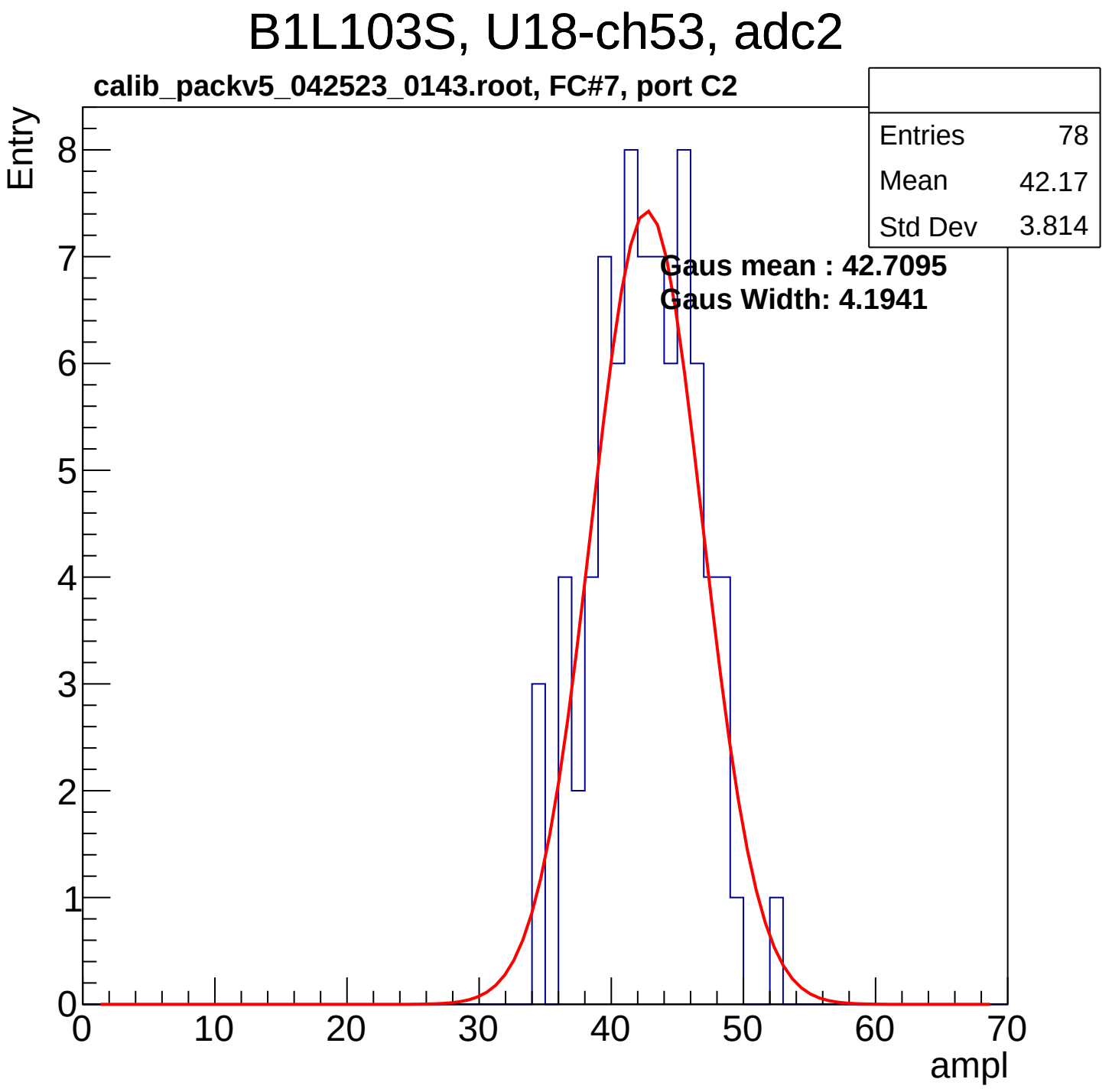
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch53, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 58
Mean 28.88
Std Dev 5.186
Gaus mean : 29.8269
Gaus Width: 4.0755
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch53, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 62
Mean 35.37
Std Dev 3.507
Gaus mean : 35.7048
Gaus Width: 4.0835
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch53, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 78
Mean 42.17
Std Dev 3.814
Gaus mean : 42.7095
Gaus Width: 4.1941
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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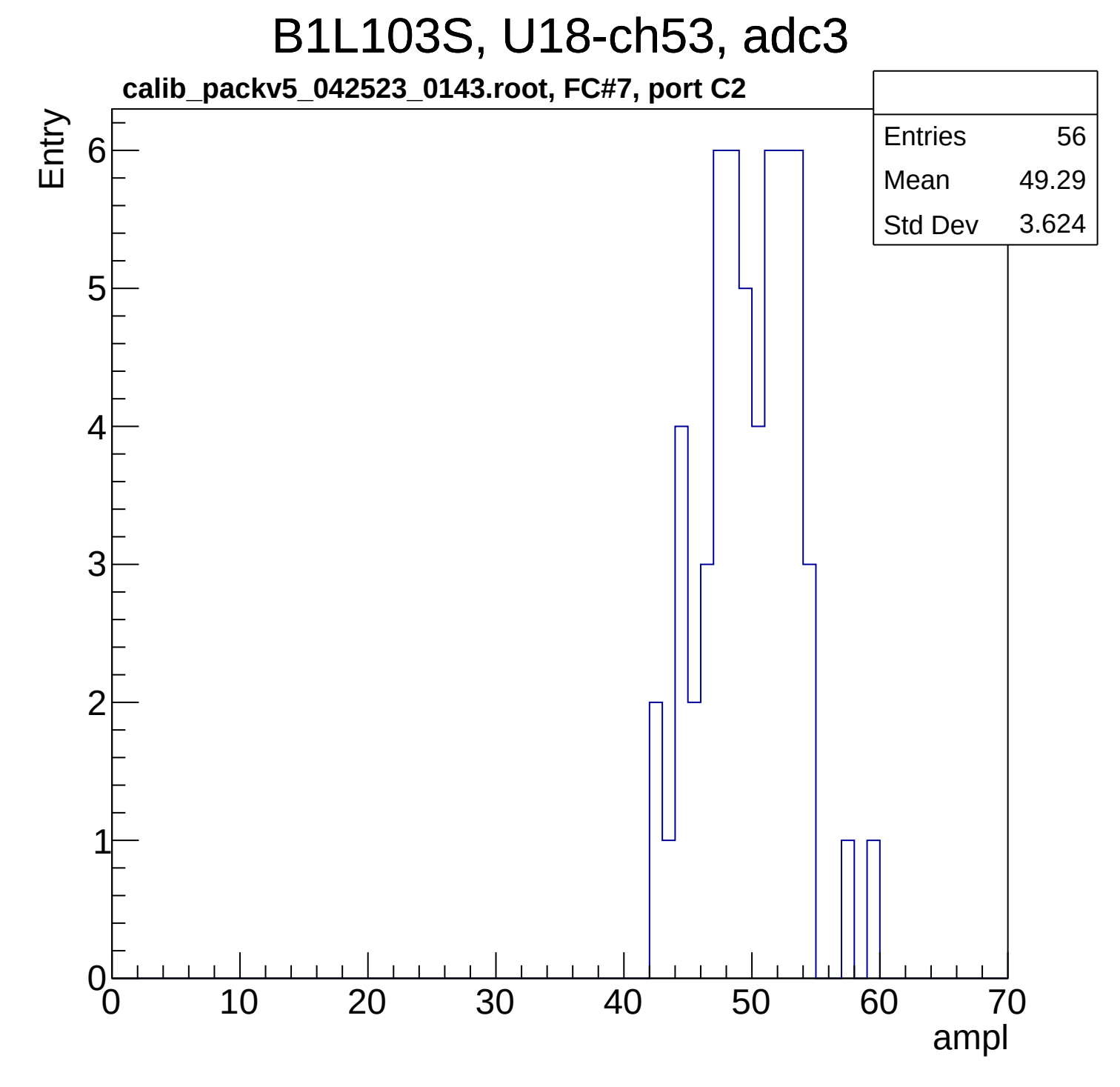
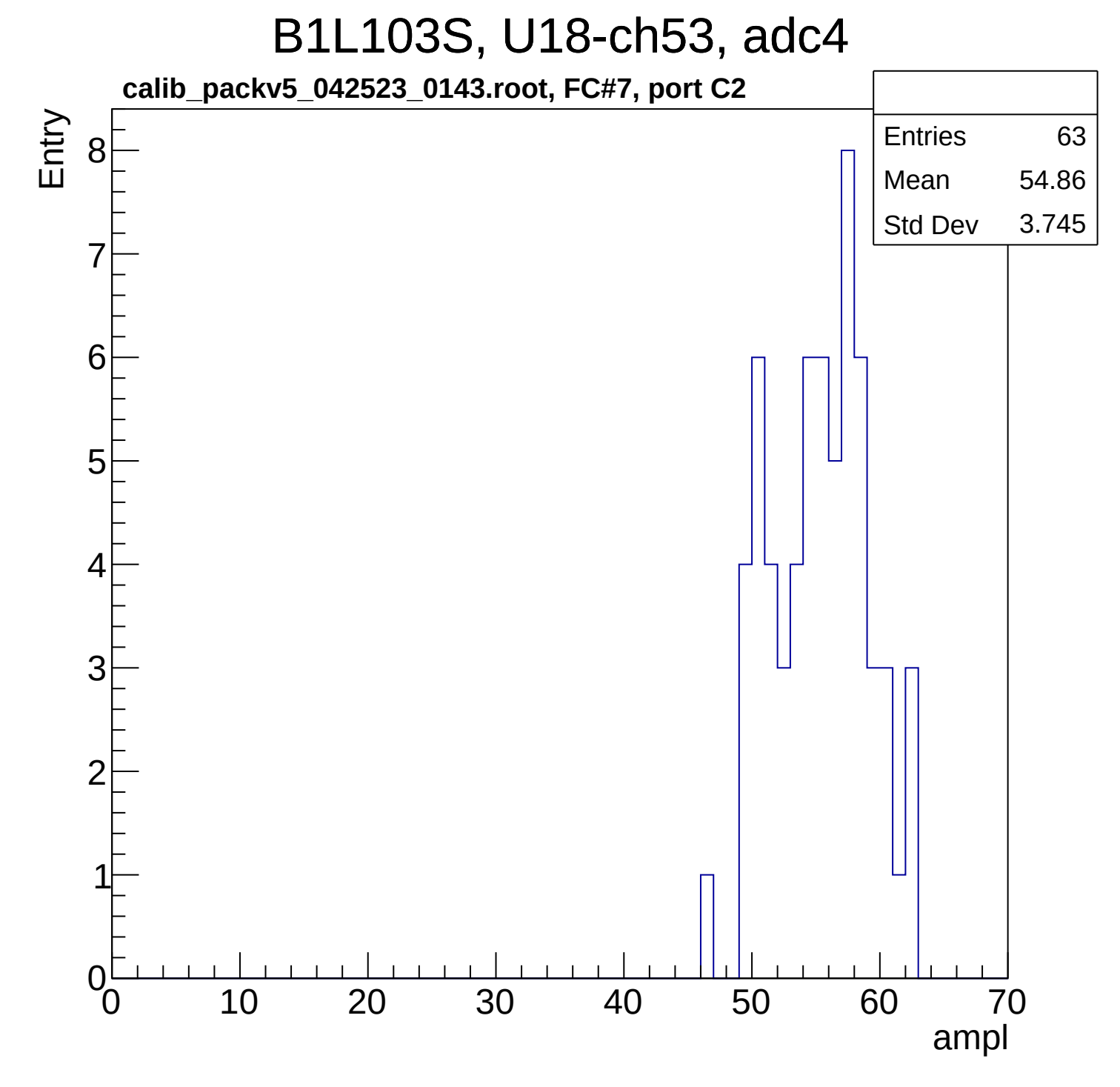

B1L103S, U18-ch53, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 49.29
Std Dev 3.624
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U18-ch53, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 54.86
Std Dev 3.745
Entry
ampl
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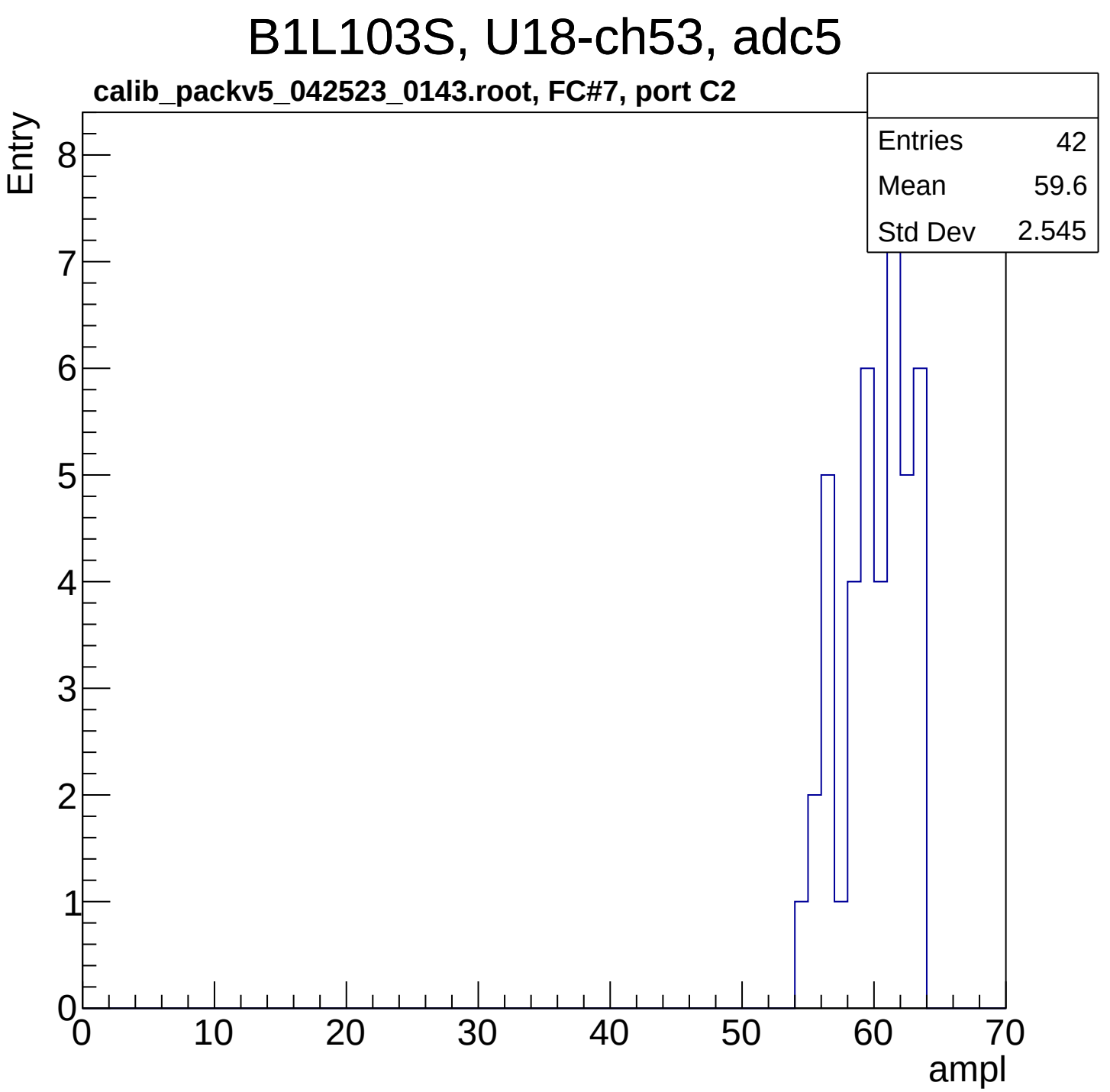
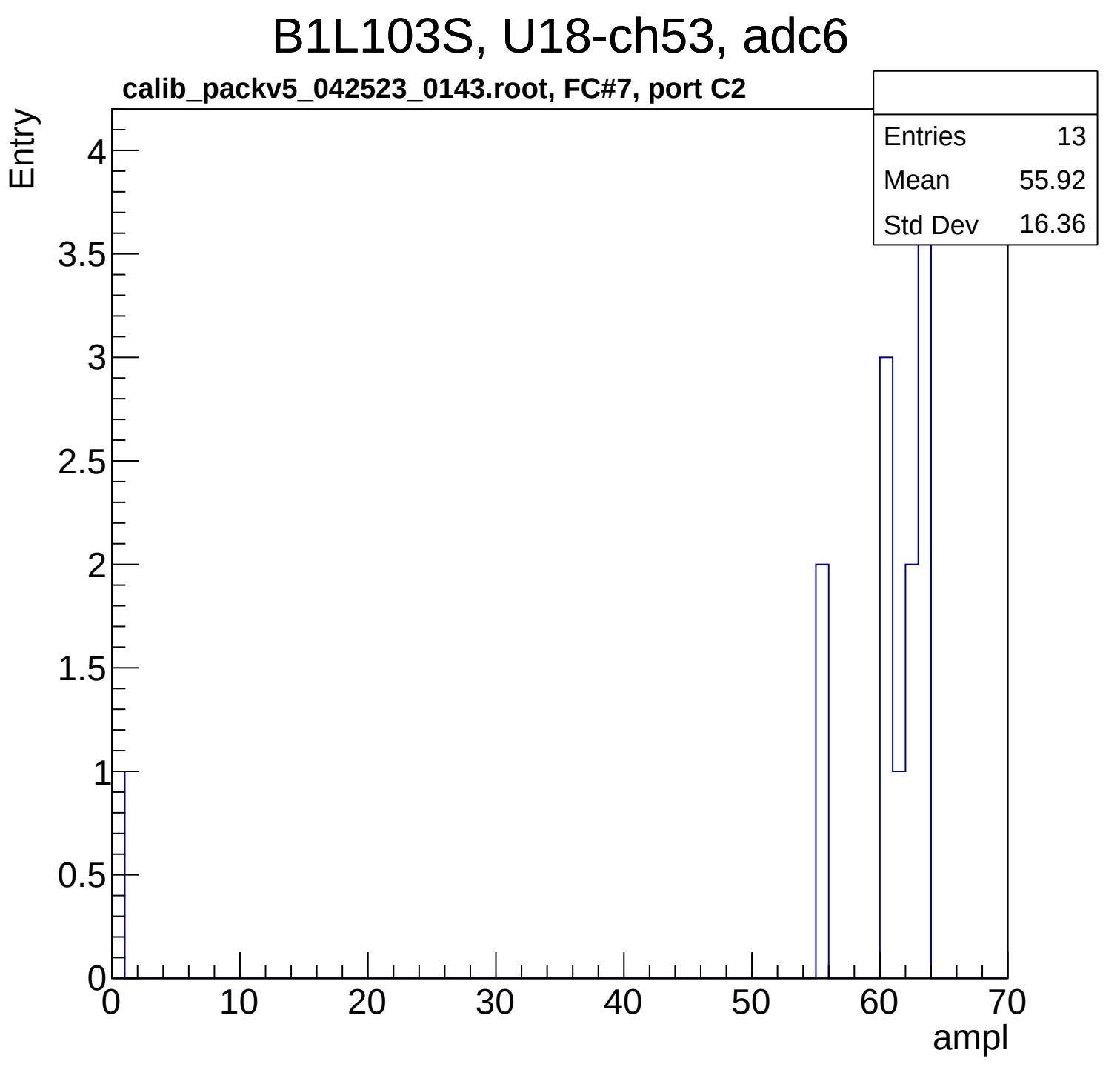
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch53, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 42
Mean 59.6
Std Dev 2.545
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch53, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 13
Mean 55.92
Std Dev 16.36
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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40
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60
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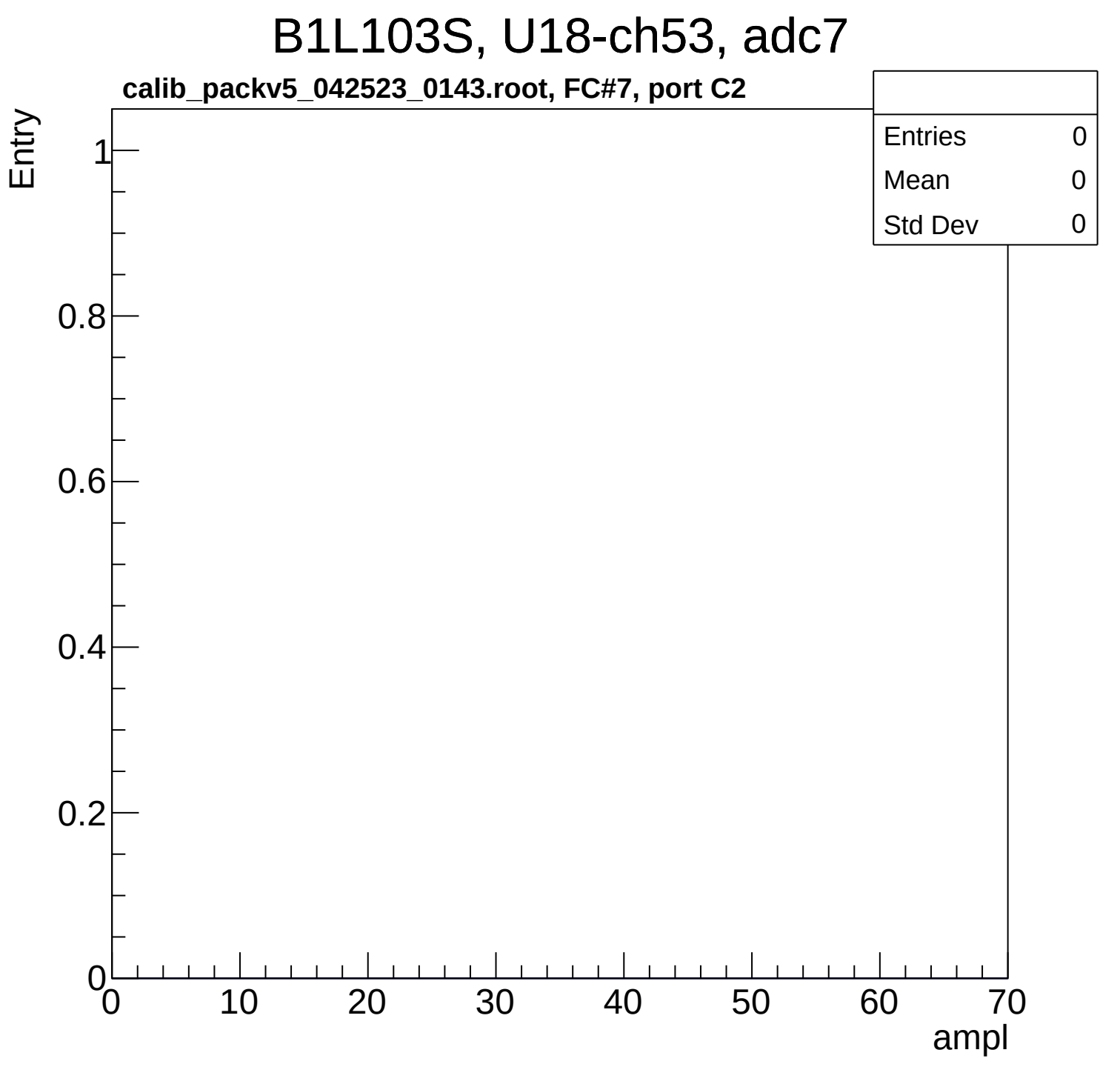
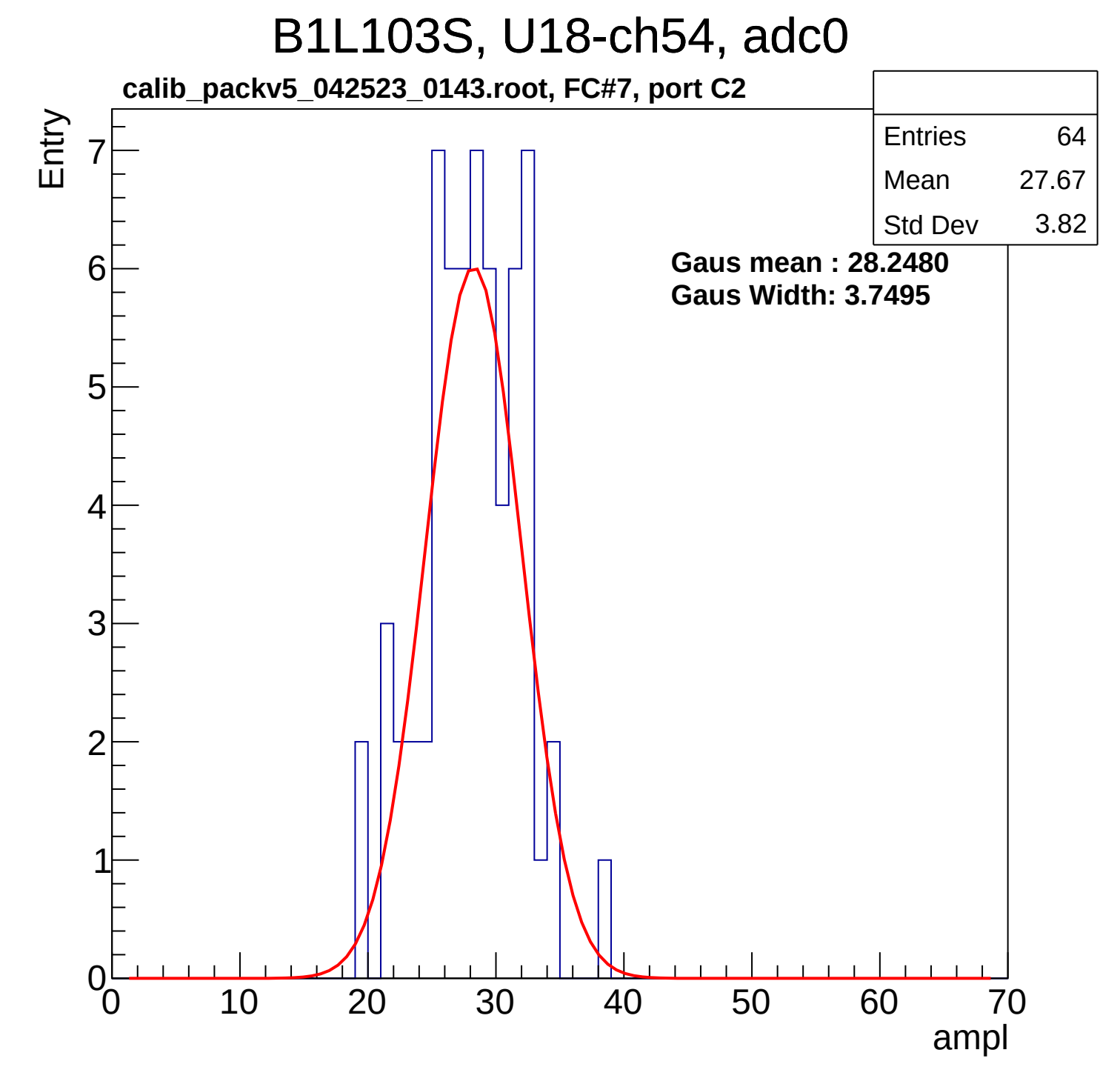
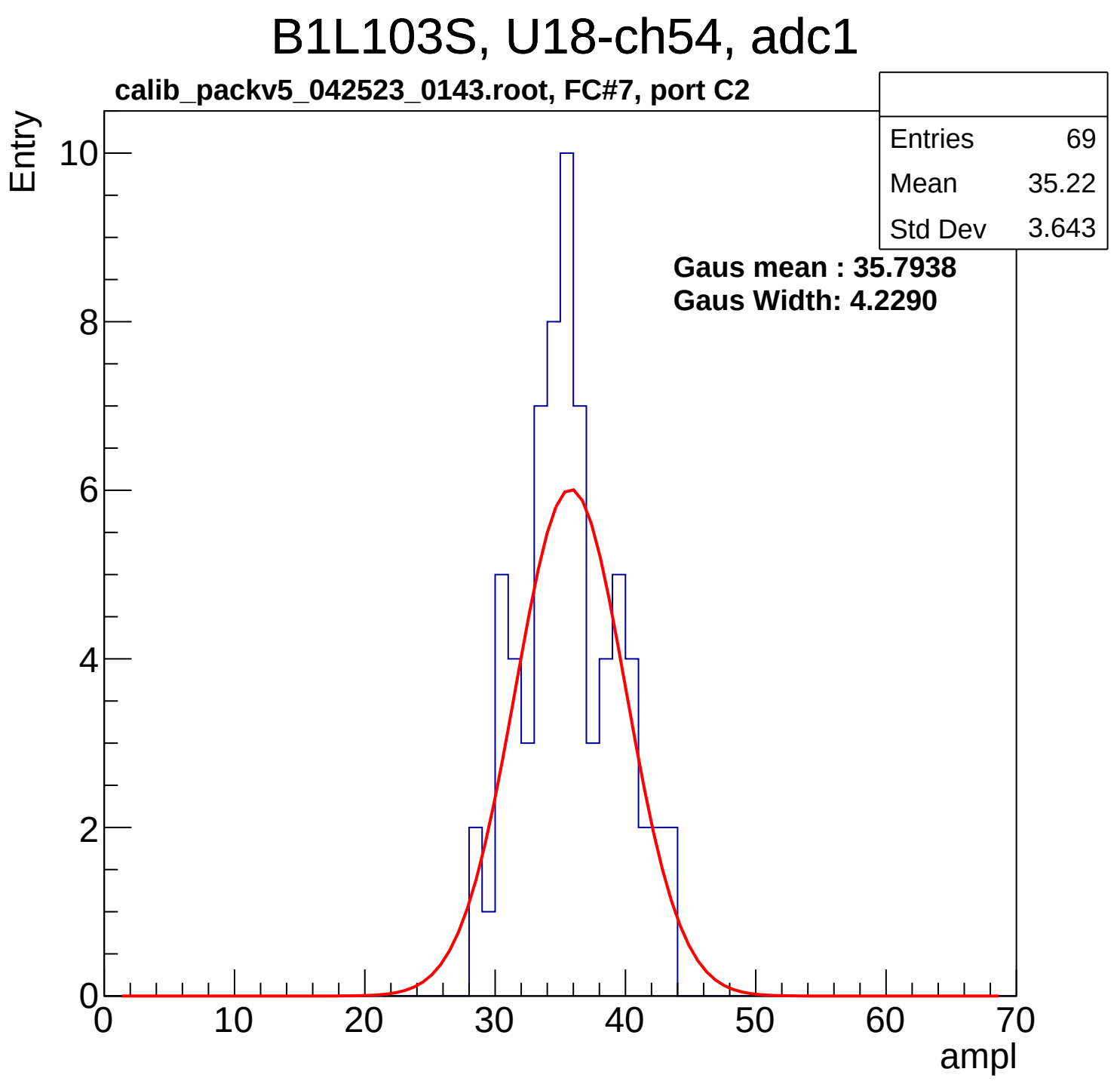

B1L103S, U18-ch53, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch54, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 27.67
Std Dev 3.82
Gaus mean : 28.2480
Gaus Width: 3.7495
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch54, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 35.22
Std Dev 3.643
Gaus mean : 35.7938
Gaus Width: 4.2290
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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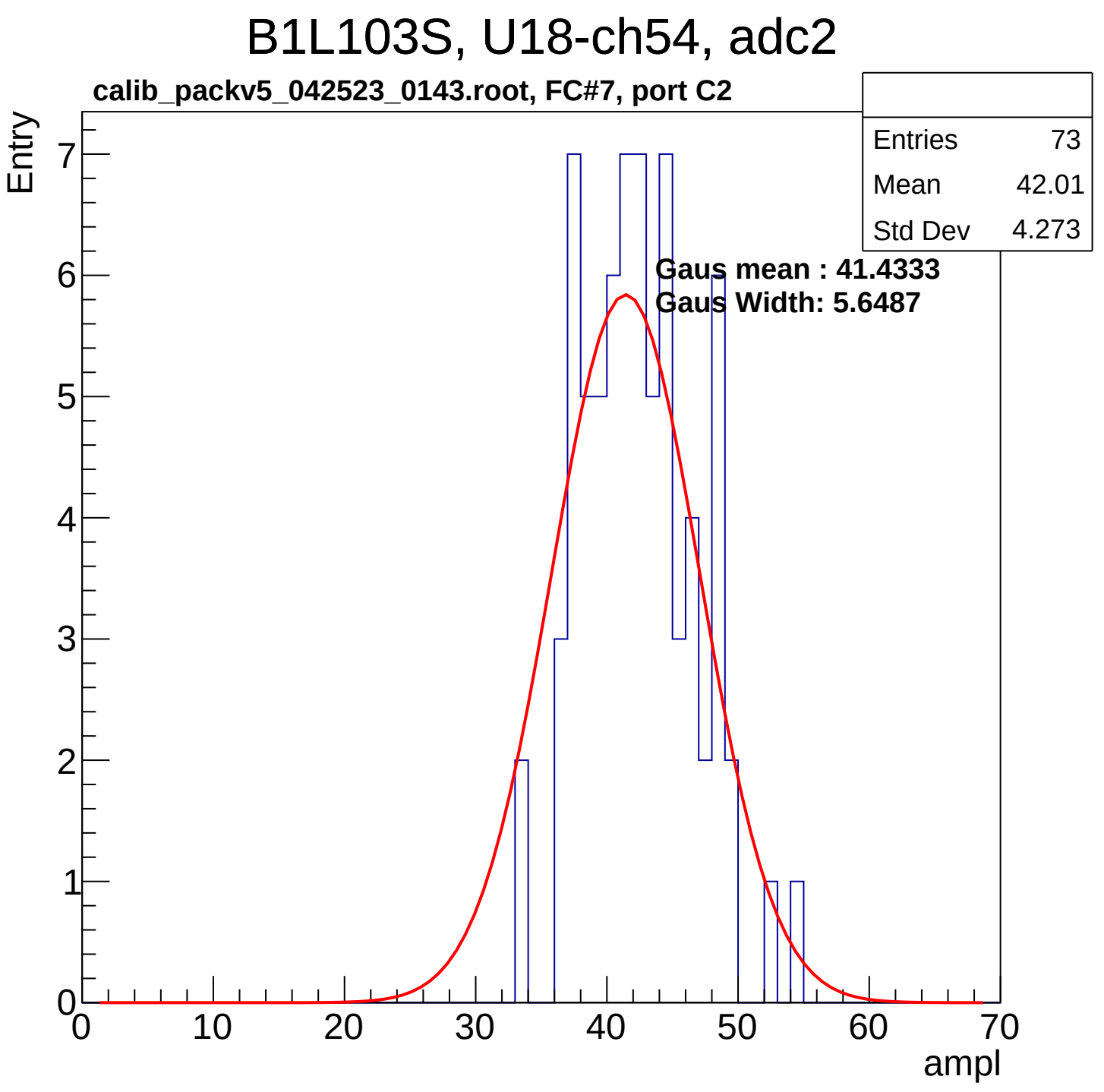
B1L103S, U18-ch54, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 73
Mean 42.01
Std Dev 4.273
Gaus mean : 41.4333
Gaus Width: 5.6487
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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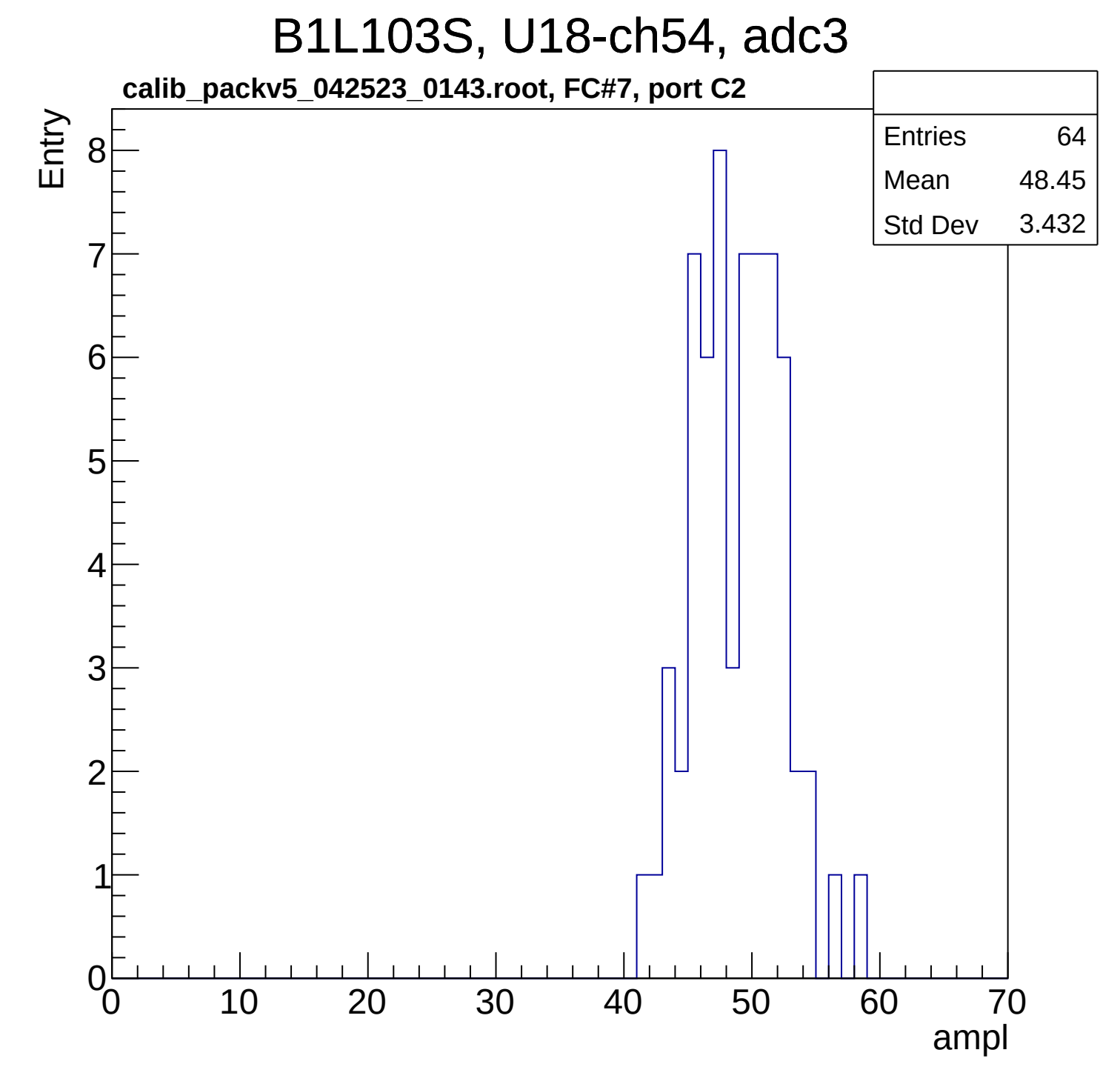
B1L103S, U18-ch54, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 48.45
Std Dev 3.432
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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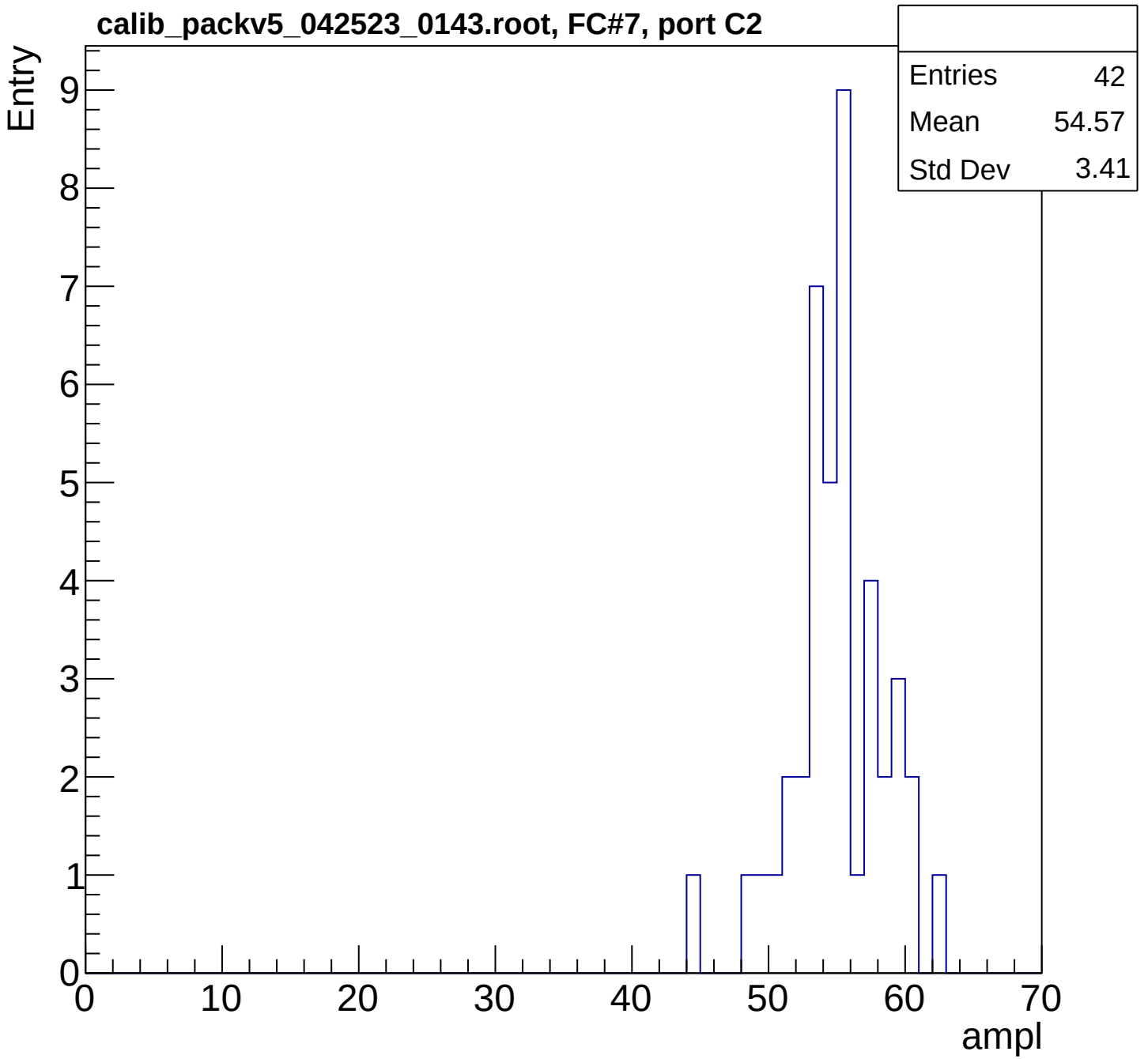
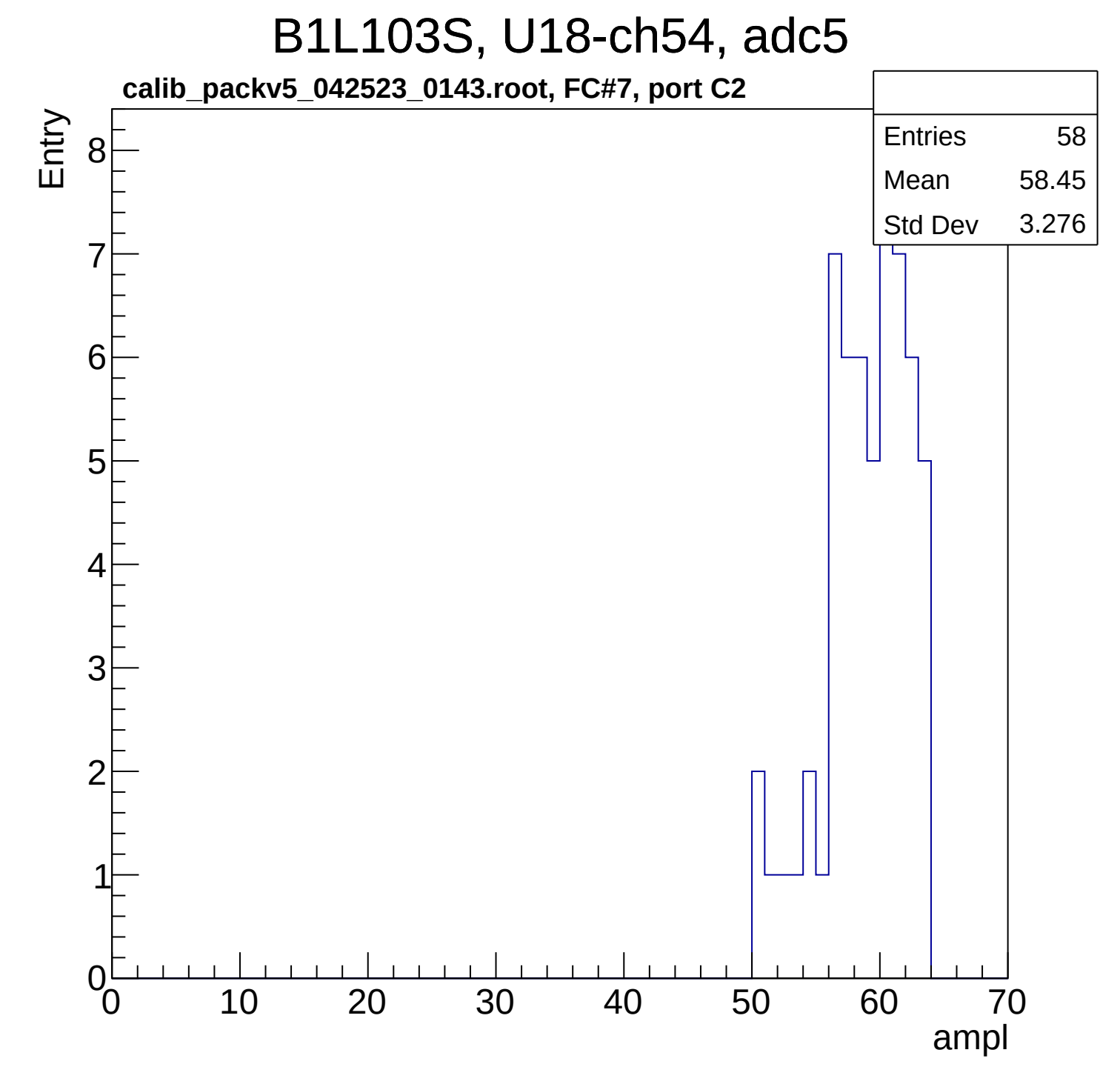

B1L103S, U18-ch54, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 42
Mean 54.57
Std Dev 3.41
Entry
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch54, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 58
Mean 58.45
Std Dev 3.276
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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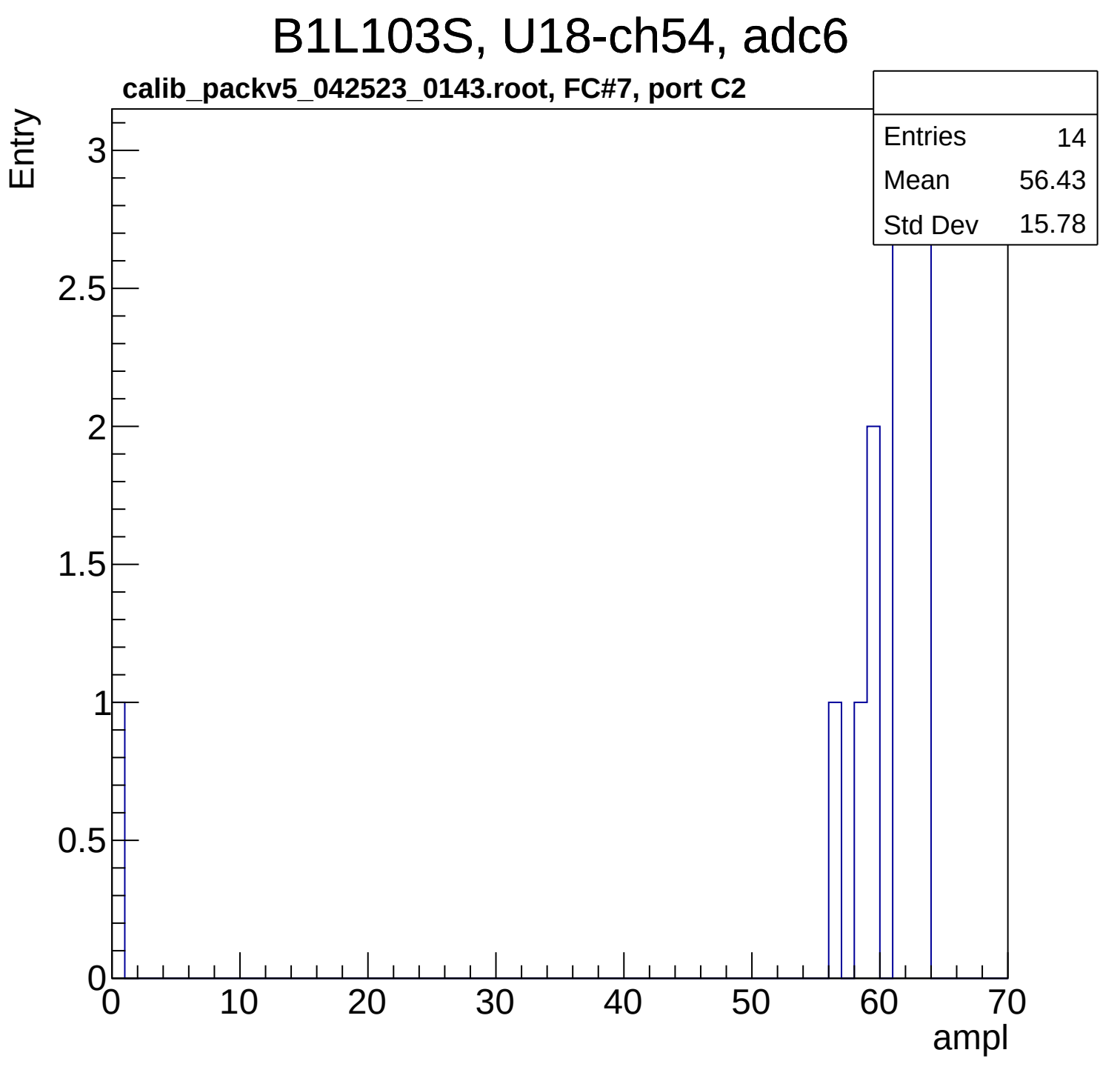
40
50
60
70


B1L103S, U18-ch54, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 14
Mean 56.43
Std Dev 15.78
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
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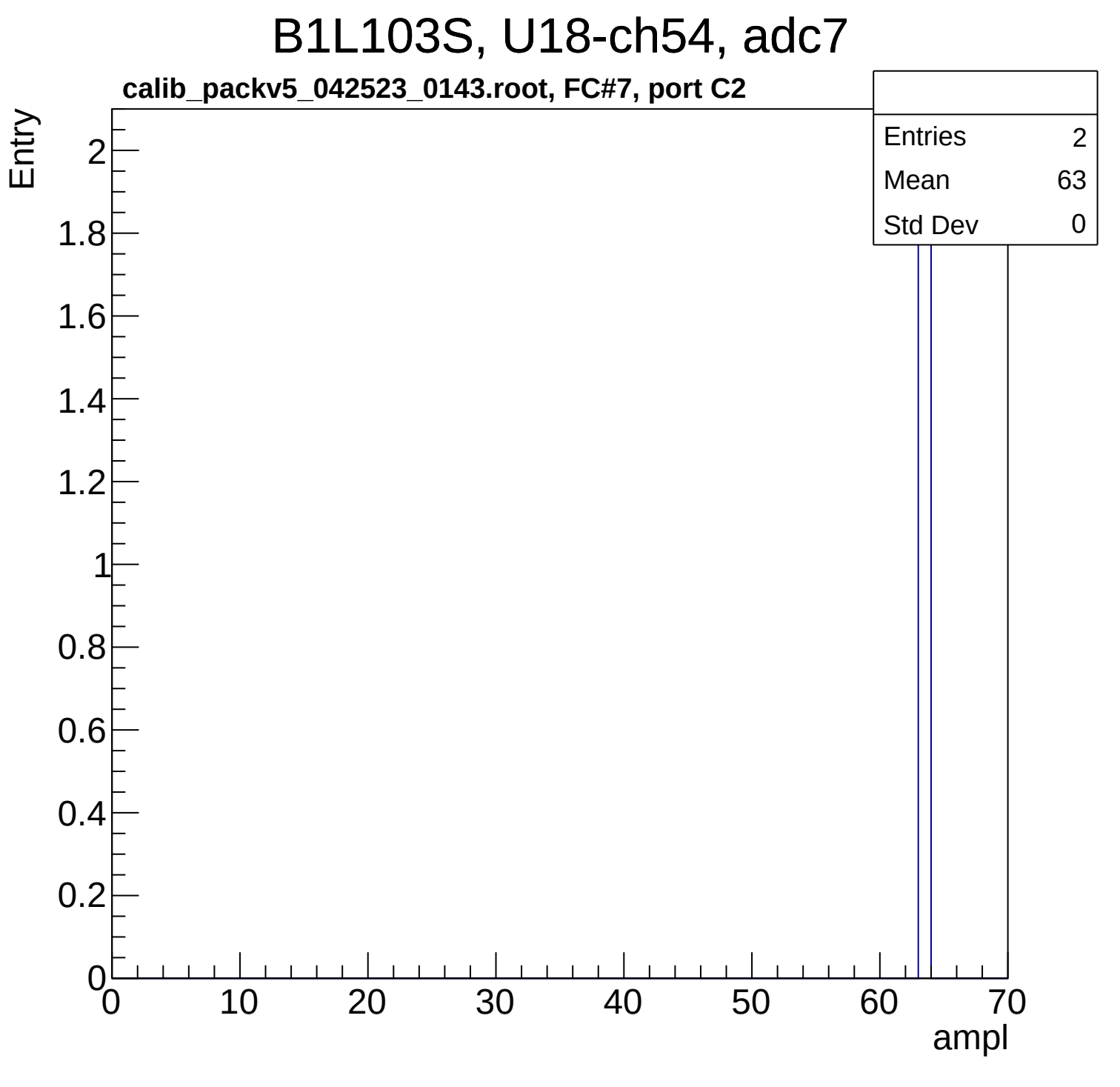
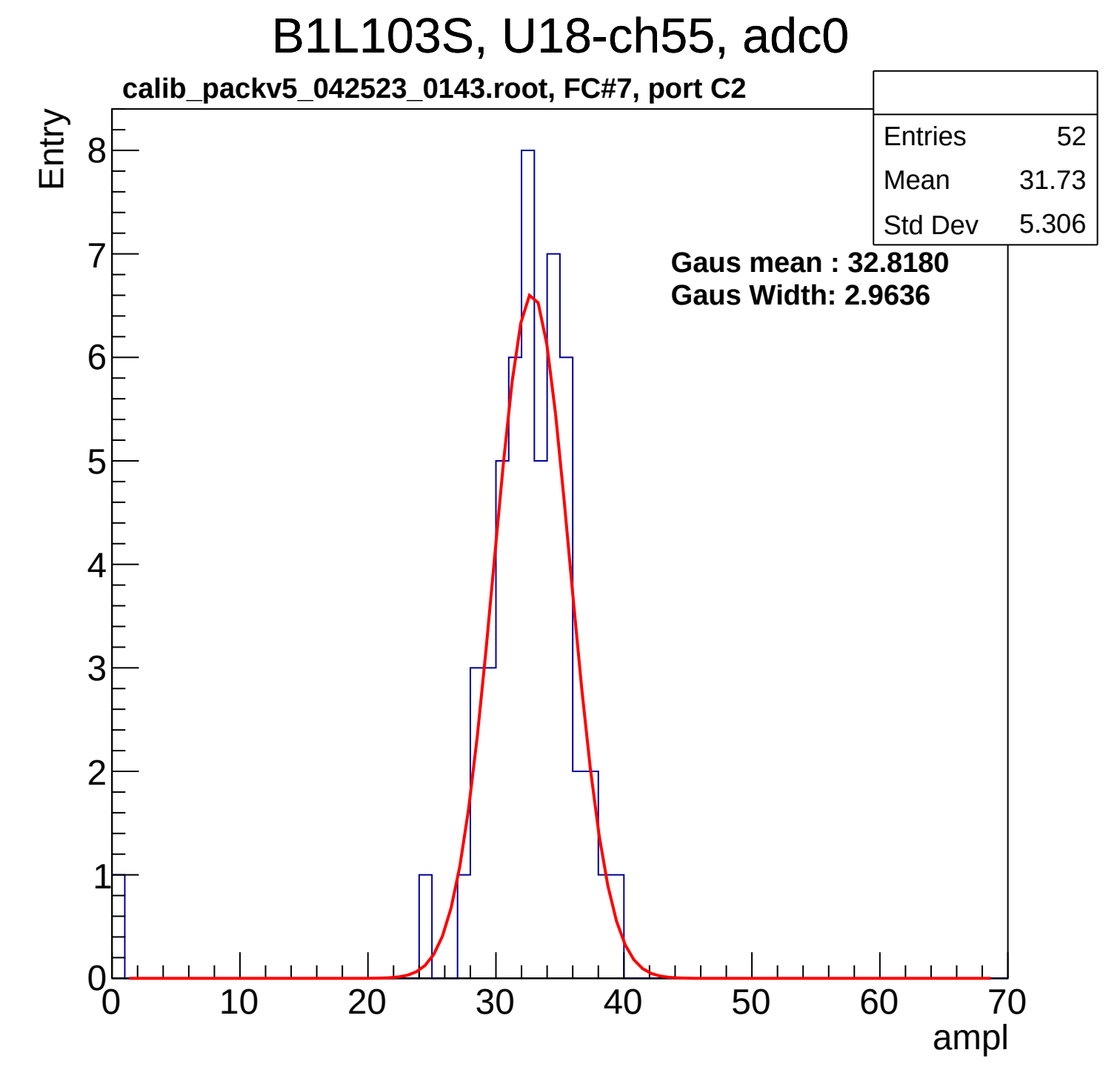
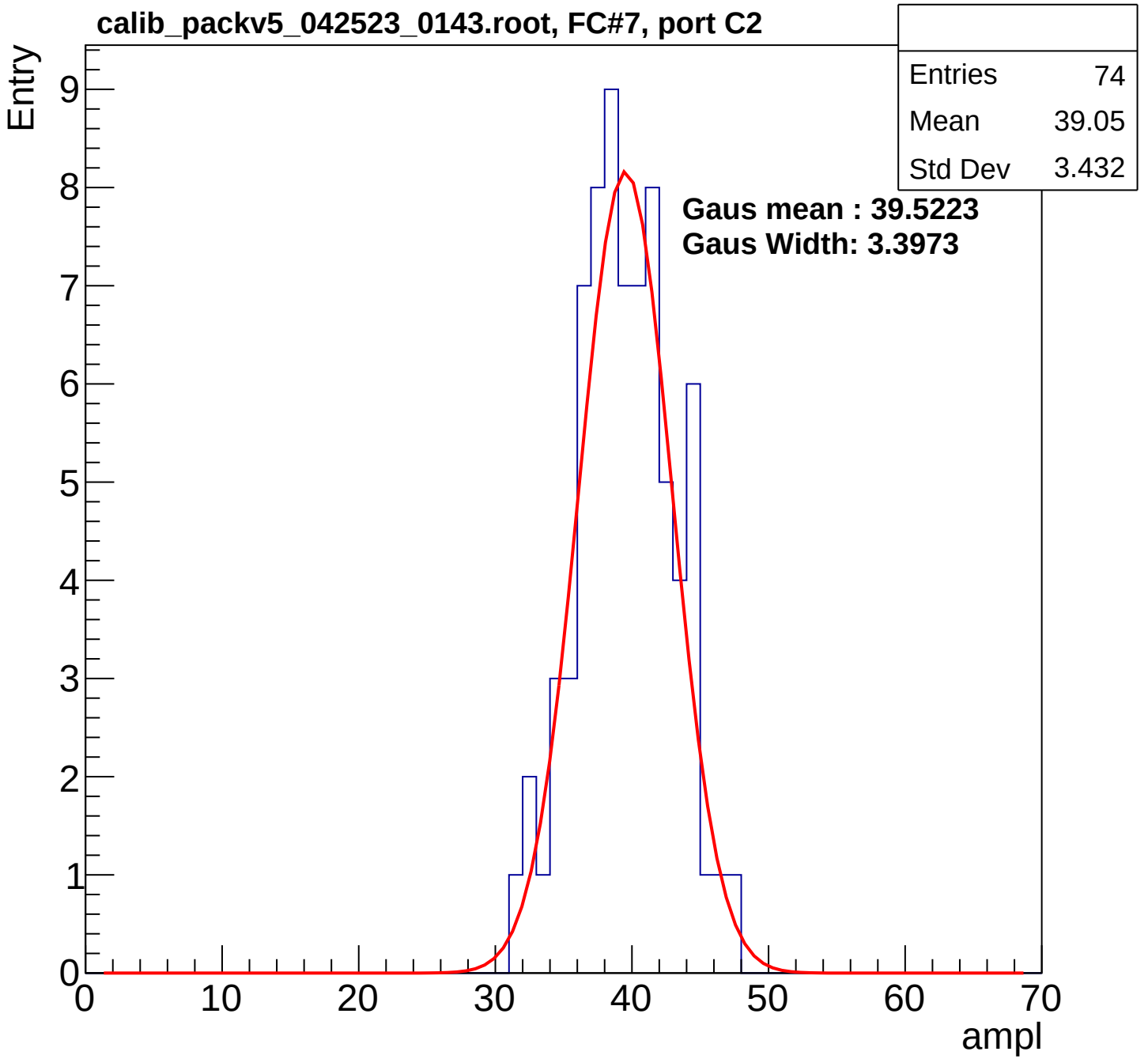

B1L103S, U18-ch54, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 63
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U18-ch55, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 52
Mean 31.73
Std Dev 5.306
Gaus mean : 32.8180
Gaus Width: 2.9636
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch55, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 74
Mean 39.05
Std Dev 3.432
Gaus mean : 39.5223
Gaus Width: 3.3973
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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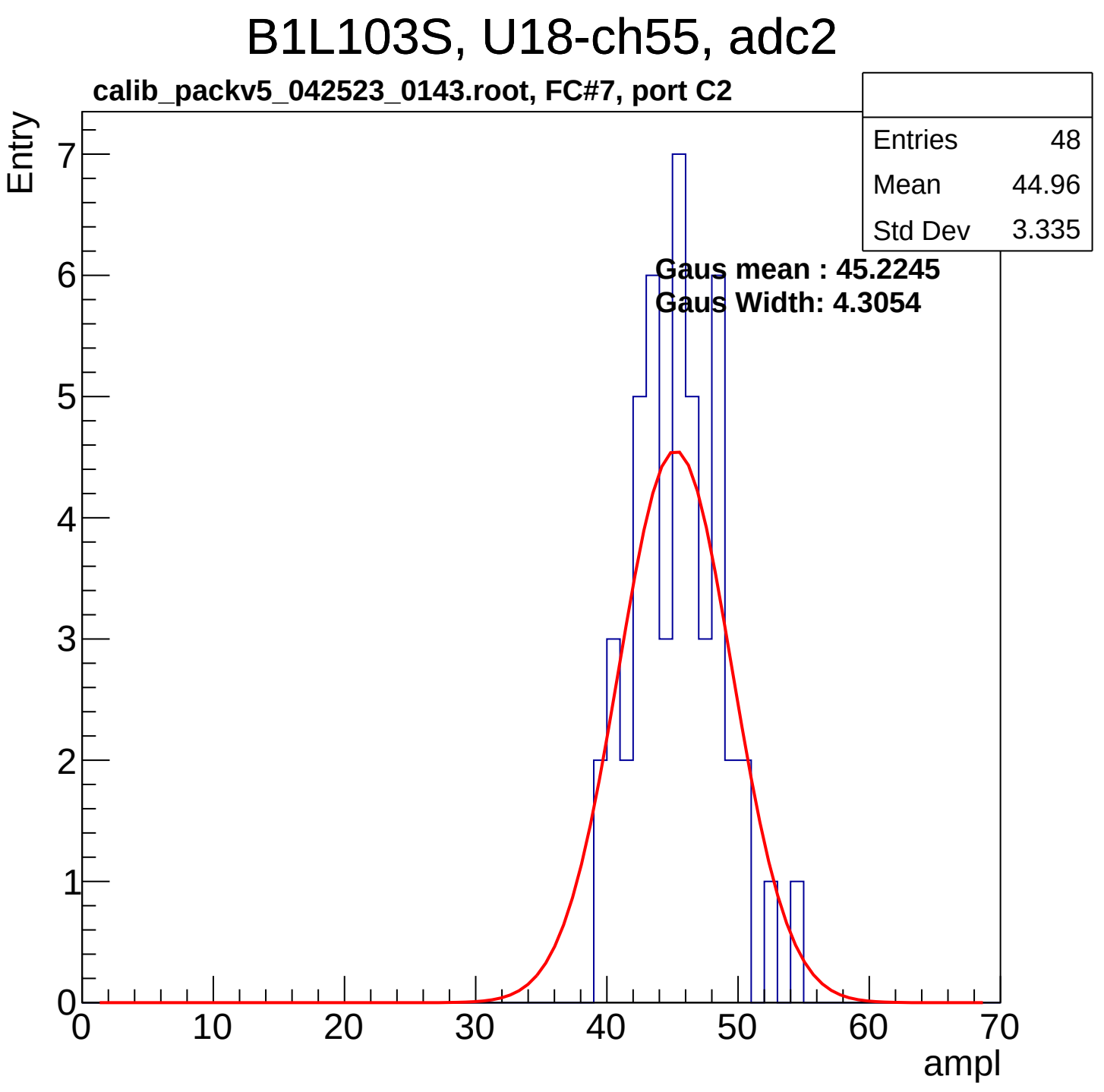
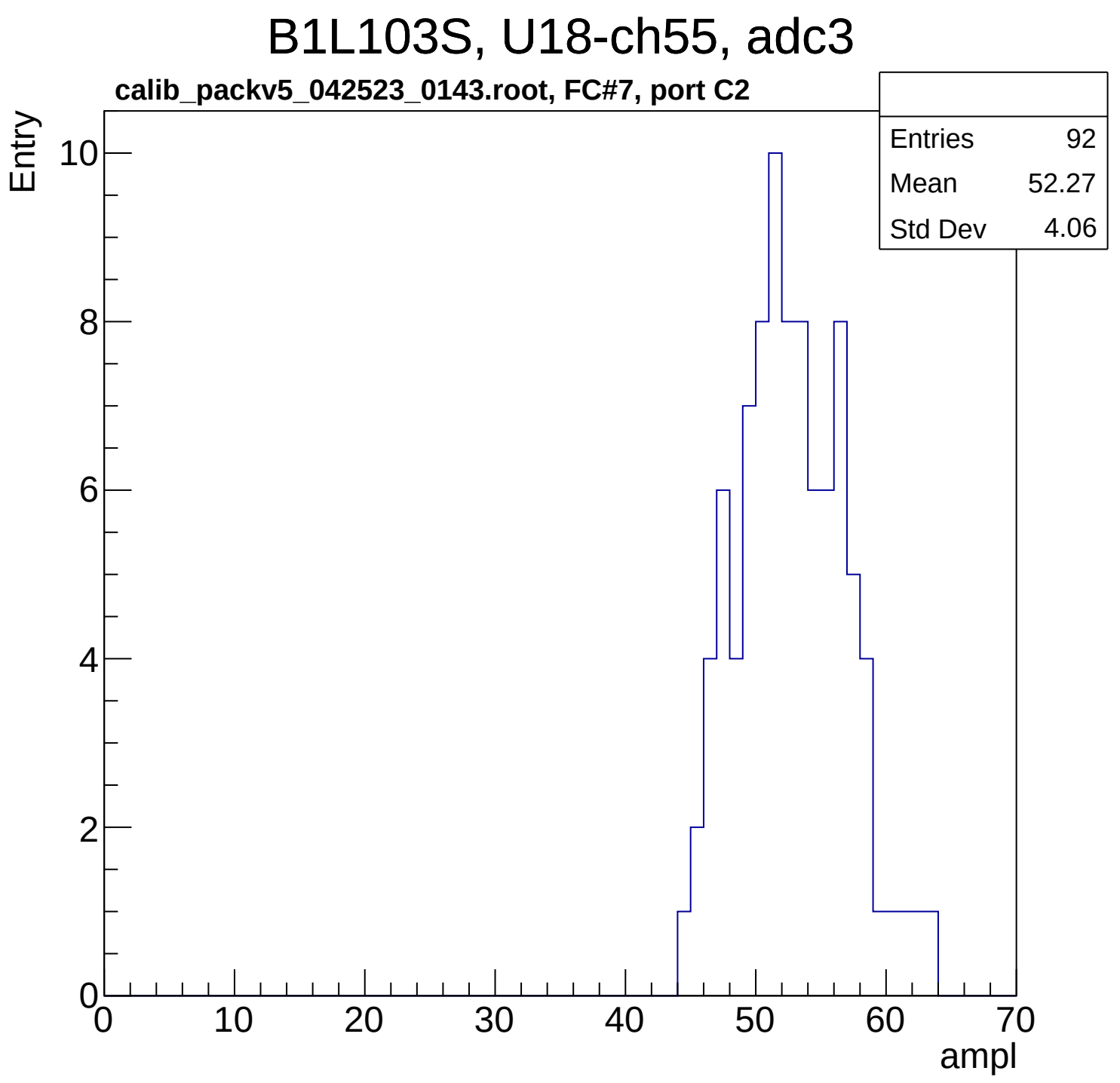
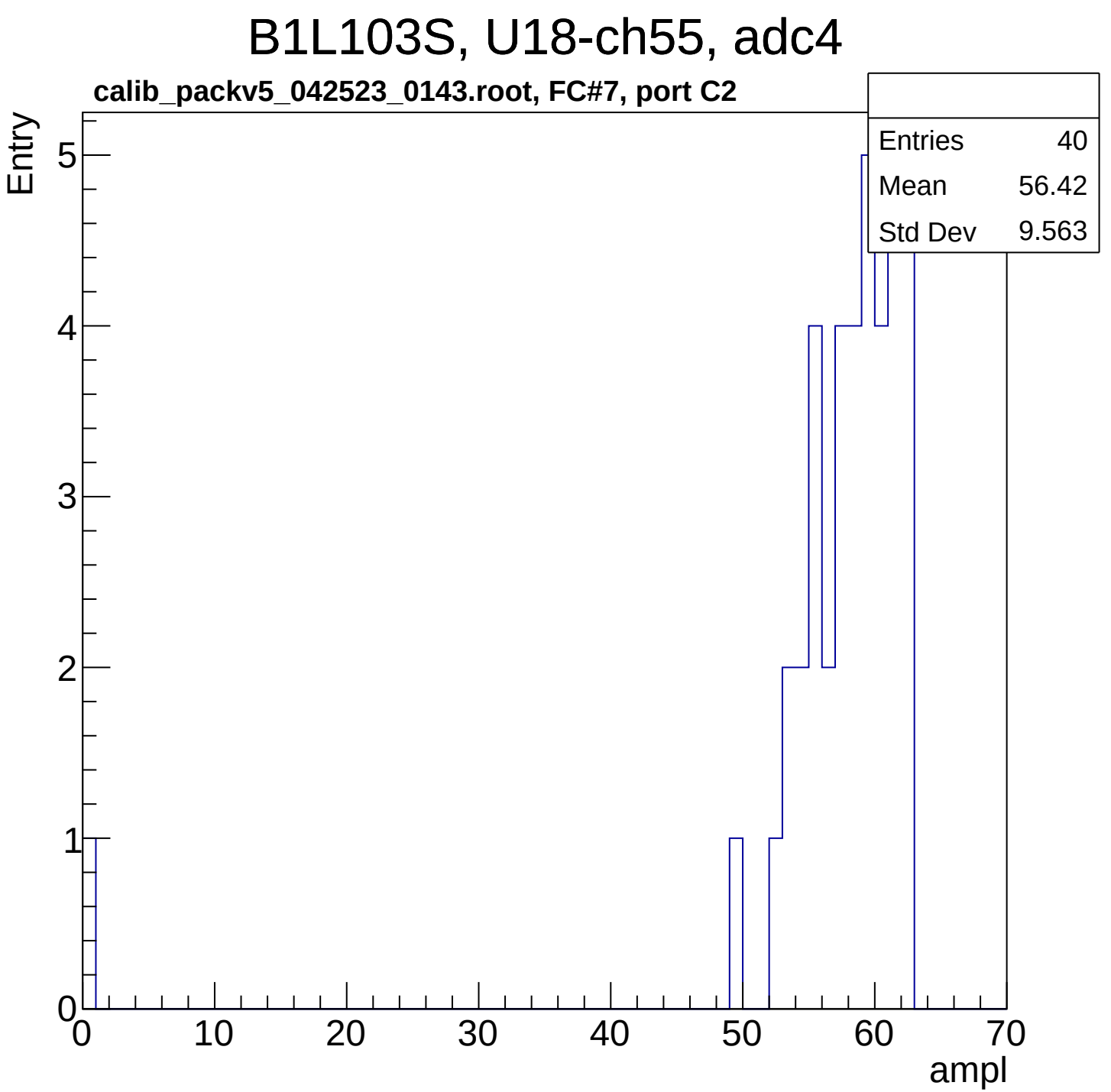
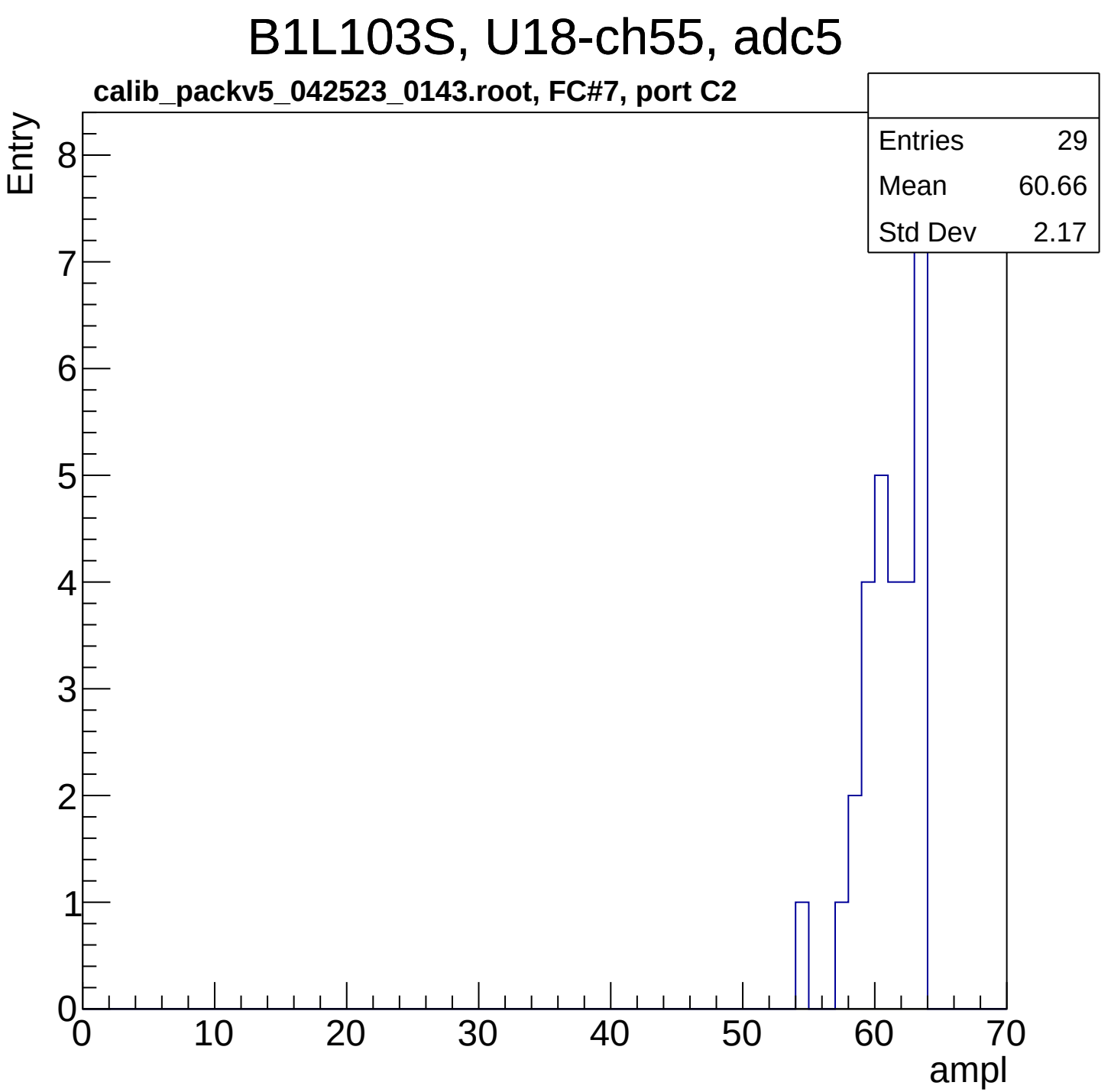
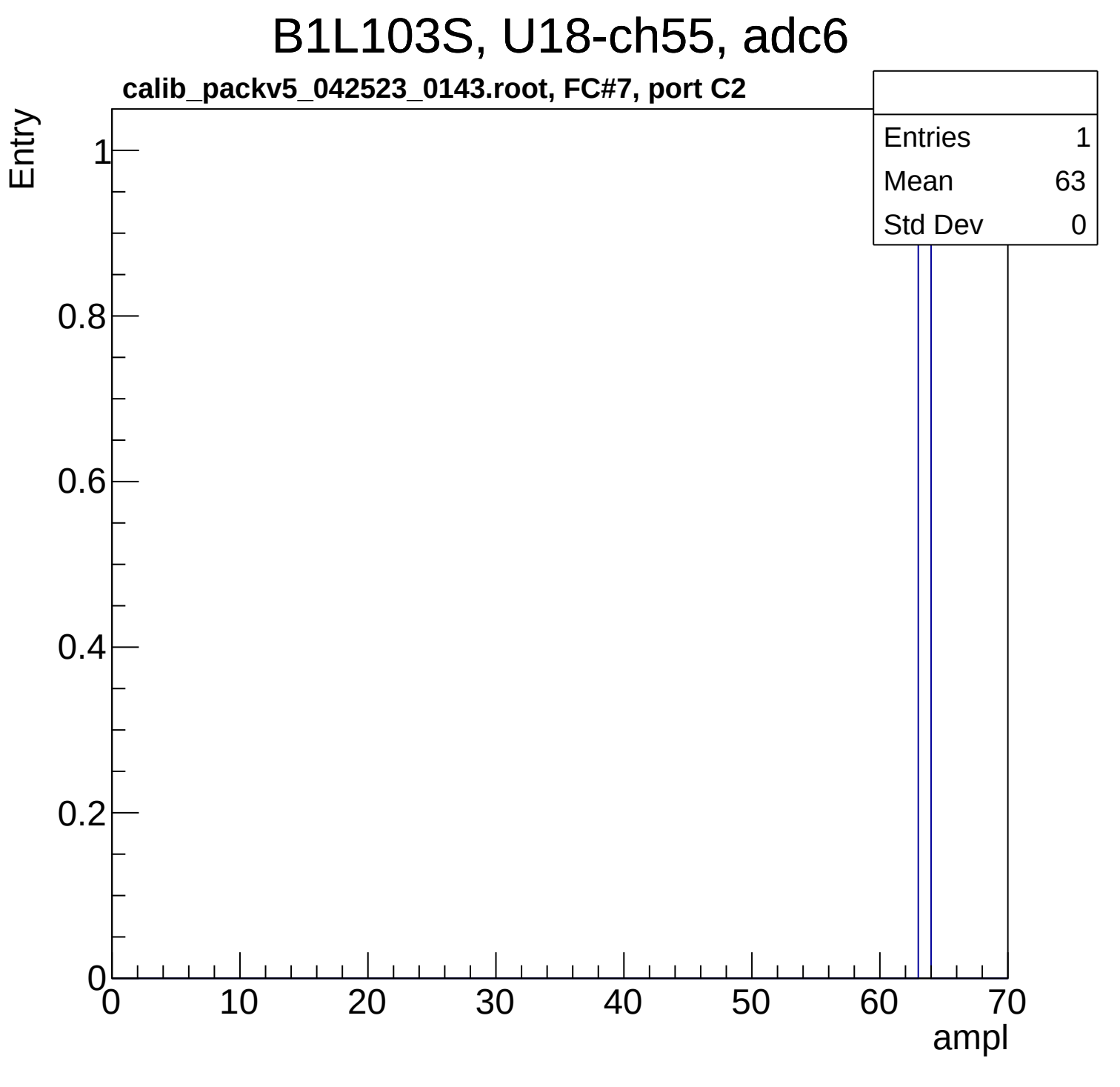
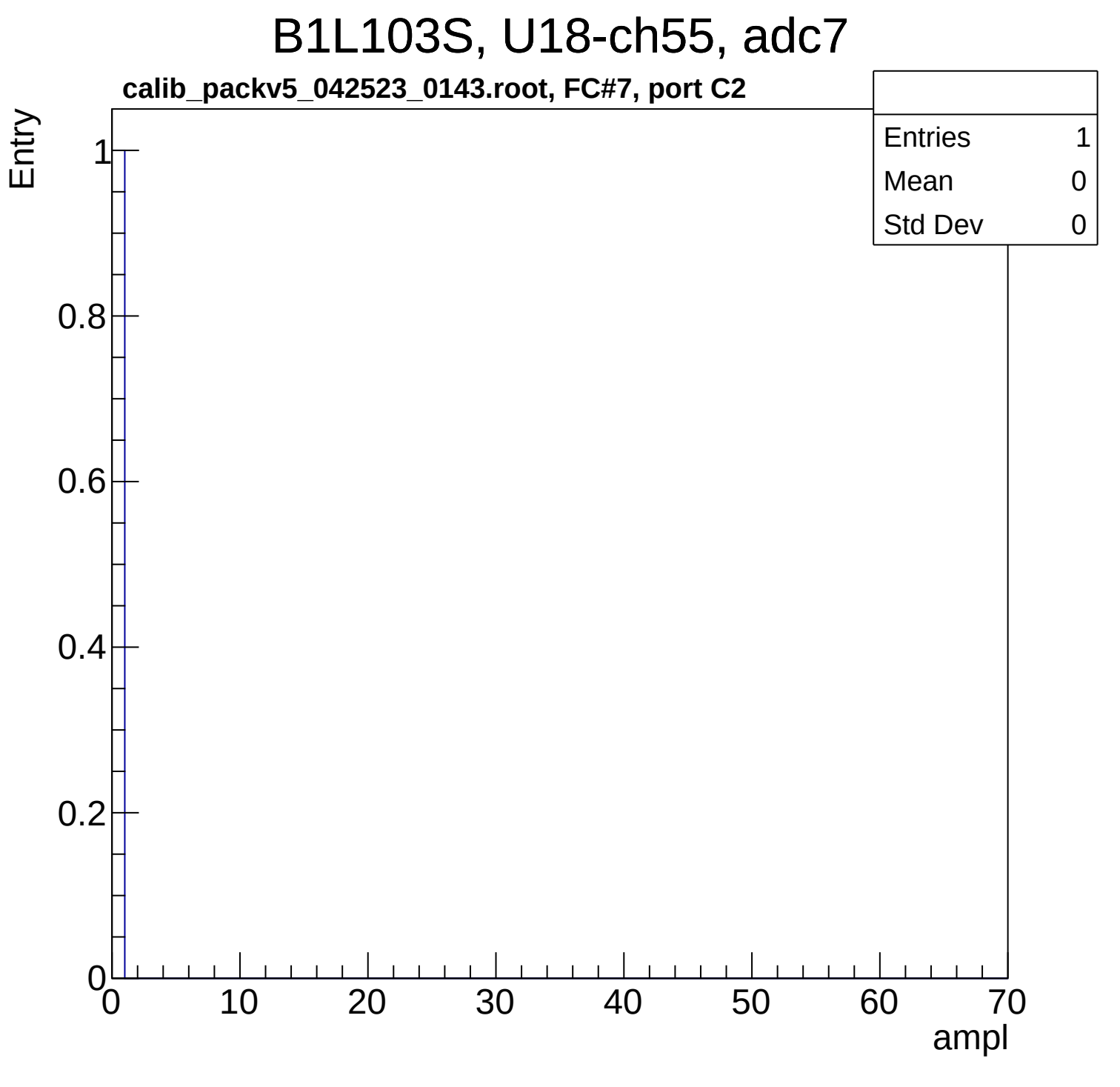

B1L103S, U18-ch55, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 48
Mean 44.96
Std Dev 3.335
Gaus mean : 45.2245
Gaus Width: 4.3054
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

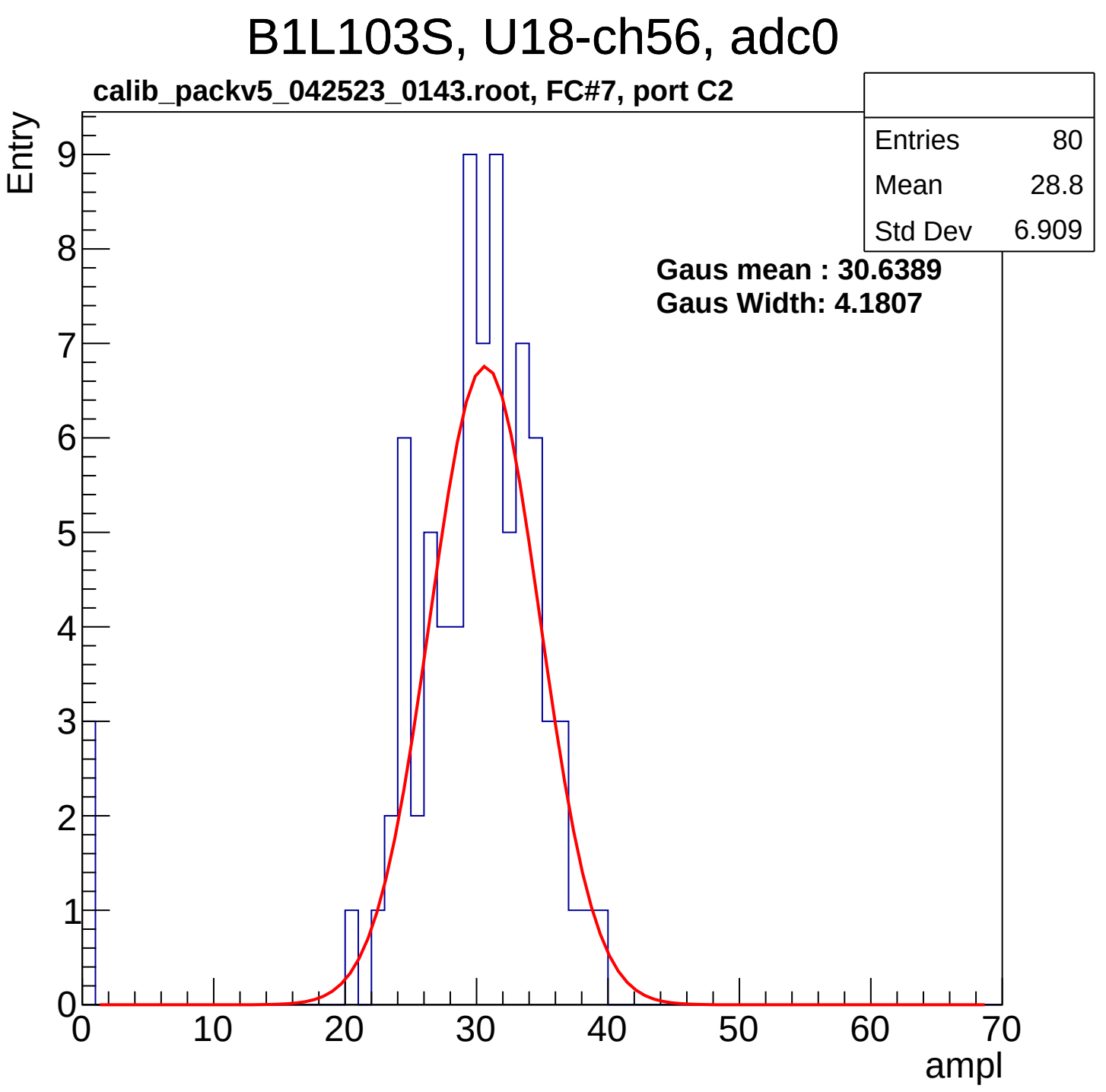

B1L103S, U18-ch55, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 92
Mean 52.27
Std Dev 4.06
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

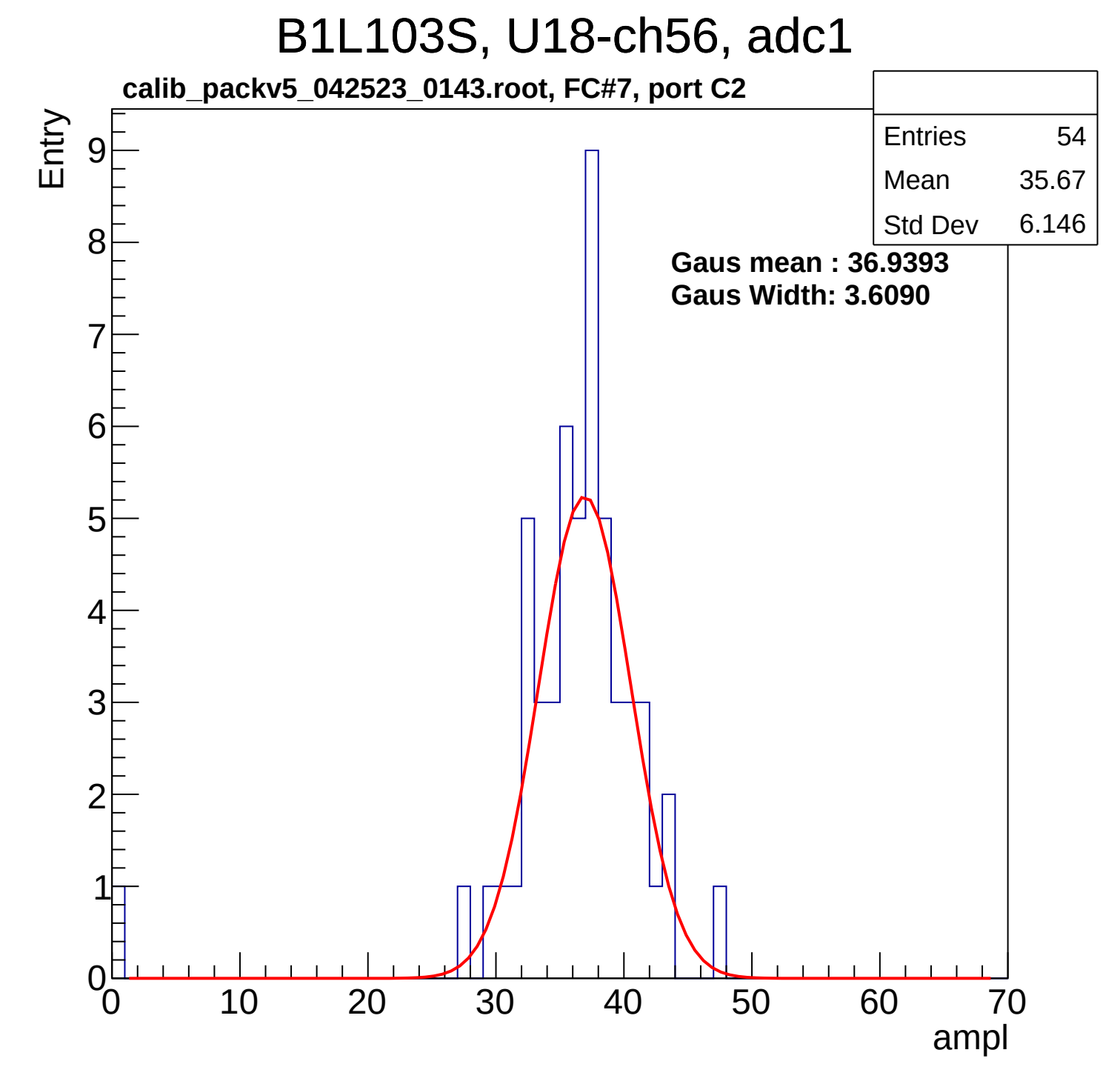

B1L103S, U18-ch55, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 40
Mean 56.42
Std Dev 9.563
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

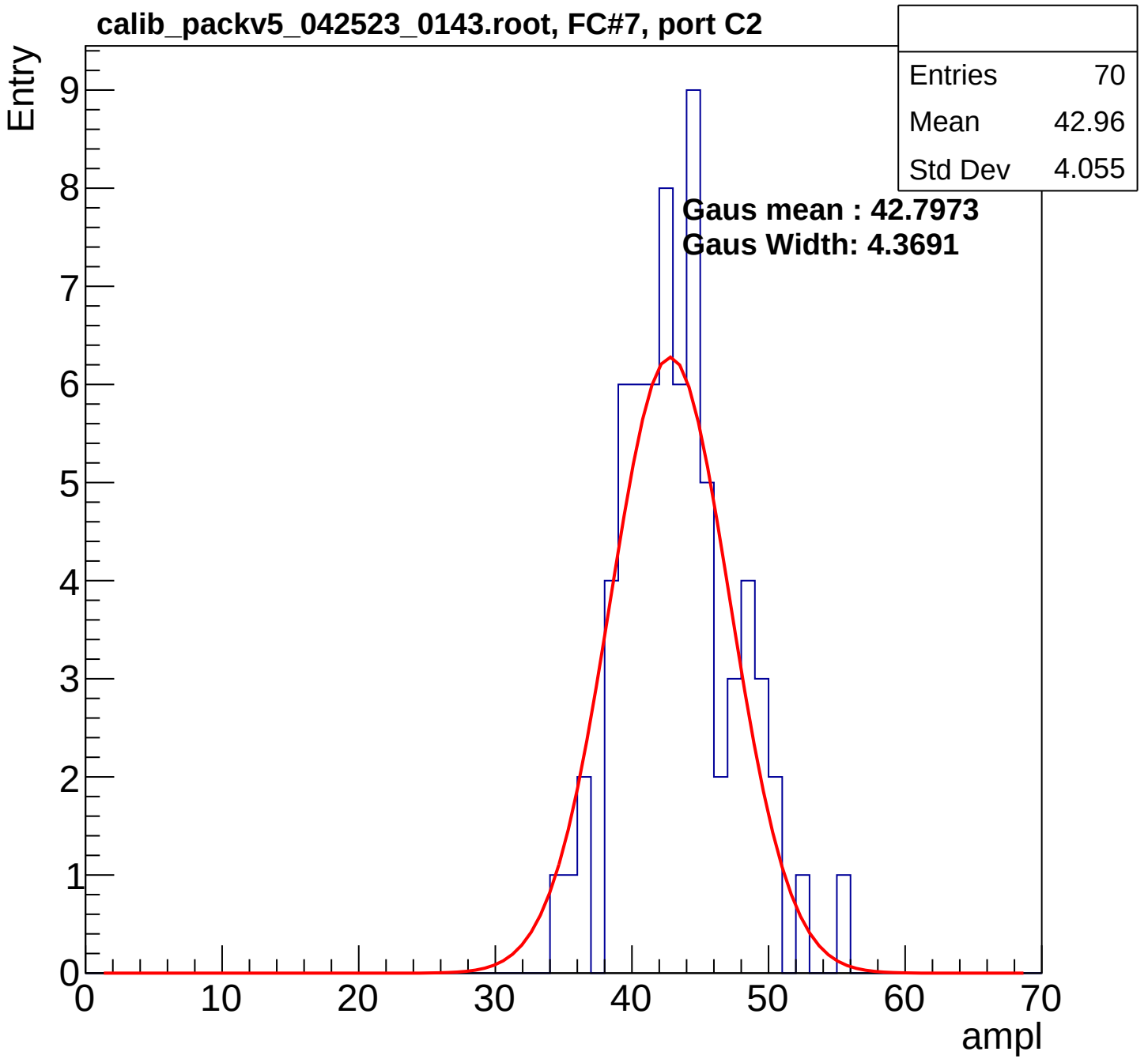

B1L103S, U18-ch55, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 29
Mean 60.66
Std Dev 2.17
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch55, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch55, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch56, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 80
Mean 28.8
Std Dev 6.909
Gaus mean : 30.6389
Gaus Width: 4.1807
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch56, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 54
Mean 35.67
Std Dev 6.146
Gaus mean : 36.9393
Gaus Width: 3.6090
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch56, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 42.96
Std Dev 4.055
Gaus mean : 42.7973
Gaus Width: 4.3691
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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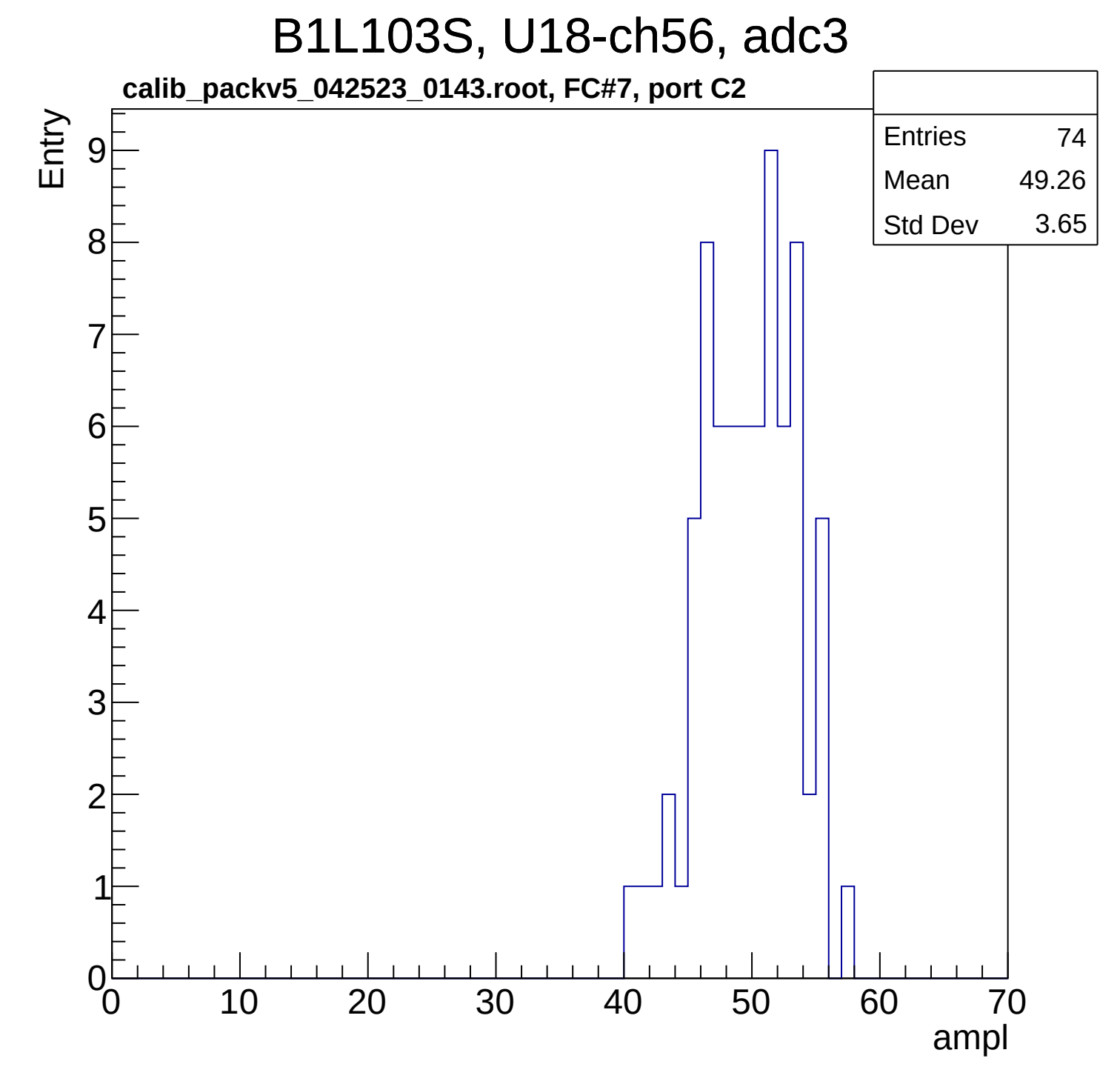
B1L103S, U18-ch56, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 74
Mean 49.26
Std Dev 3.65
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
10
20
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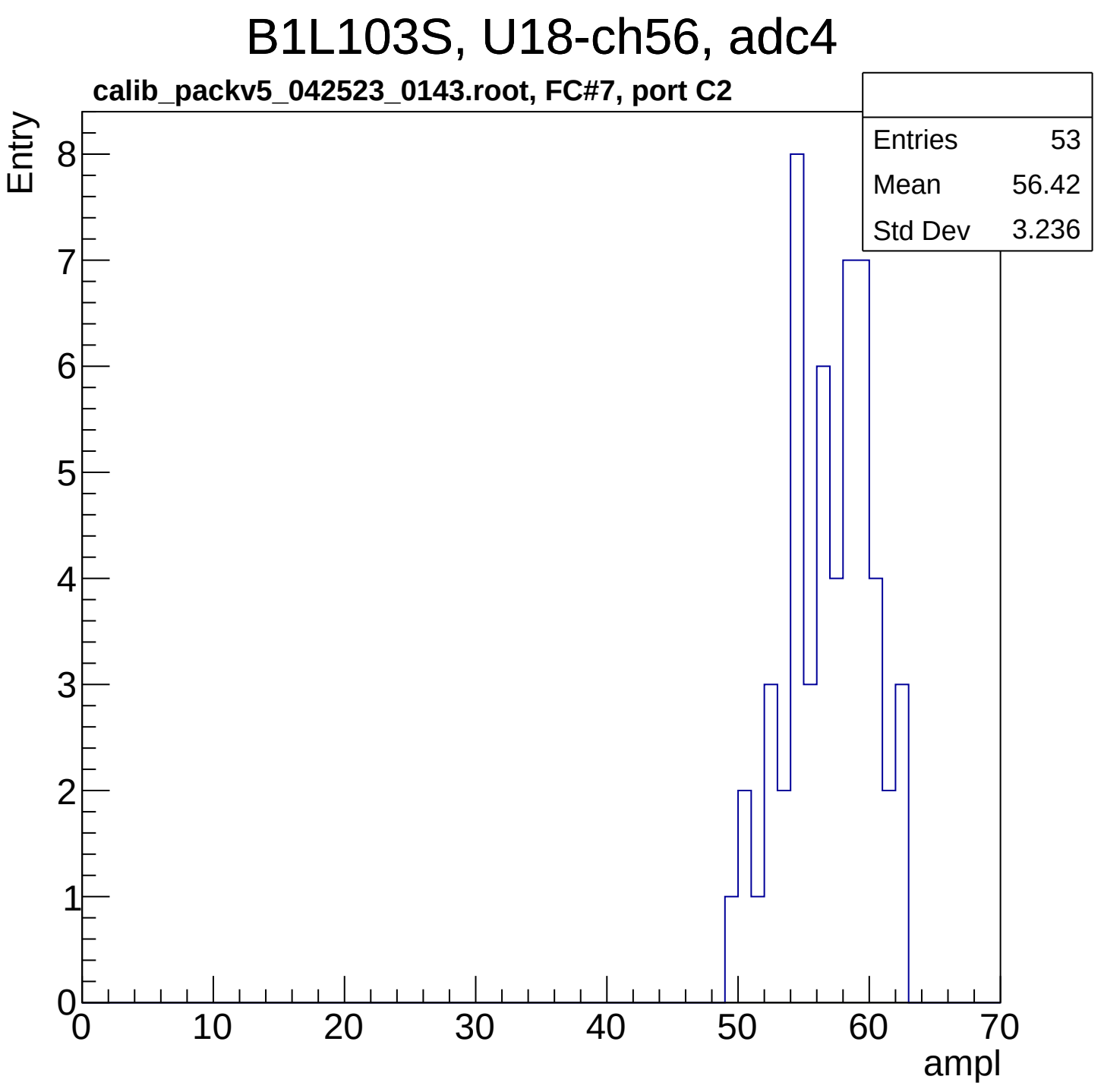
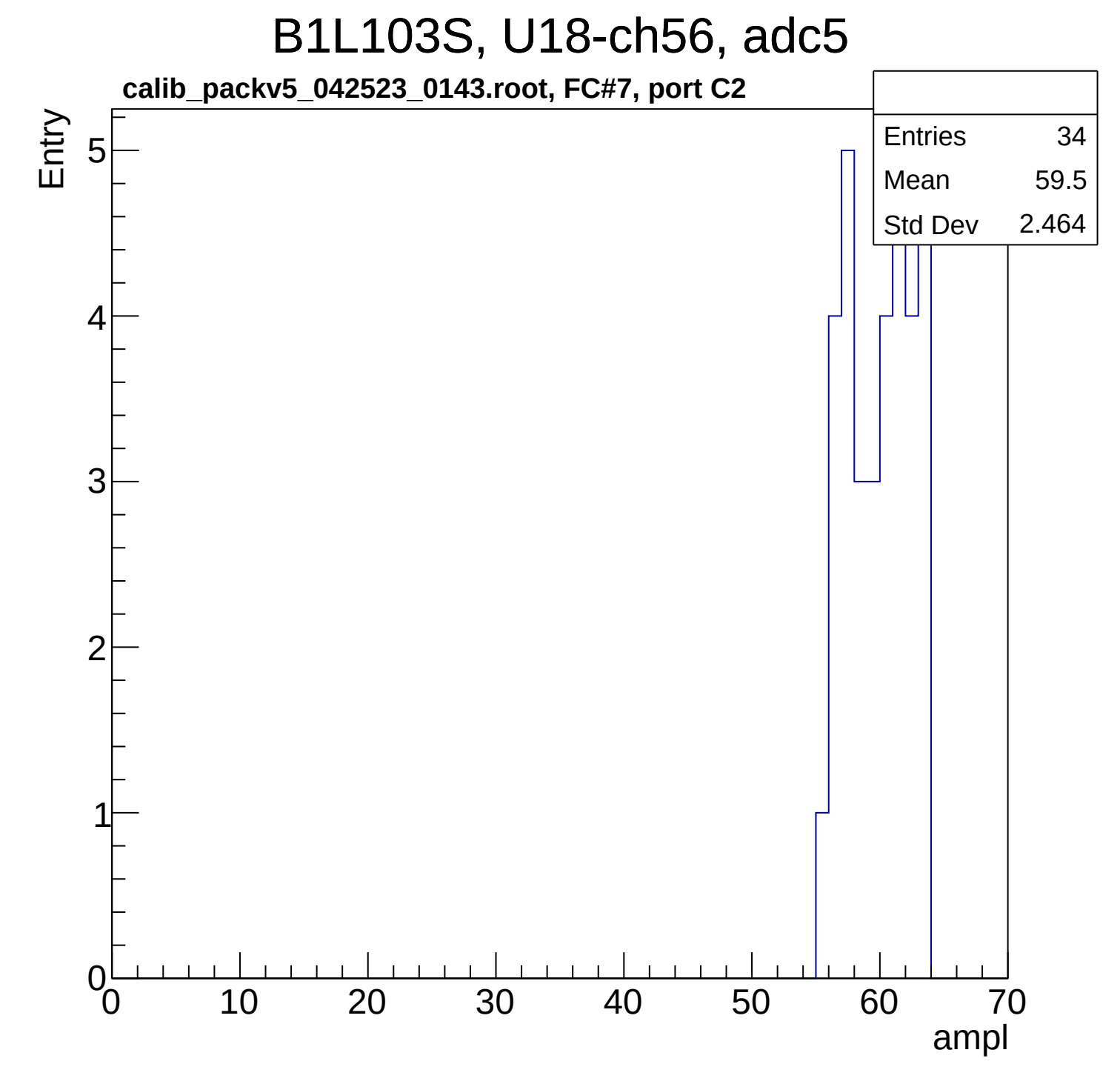
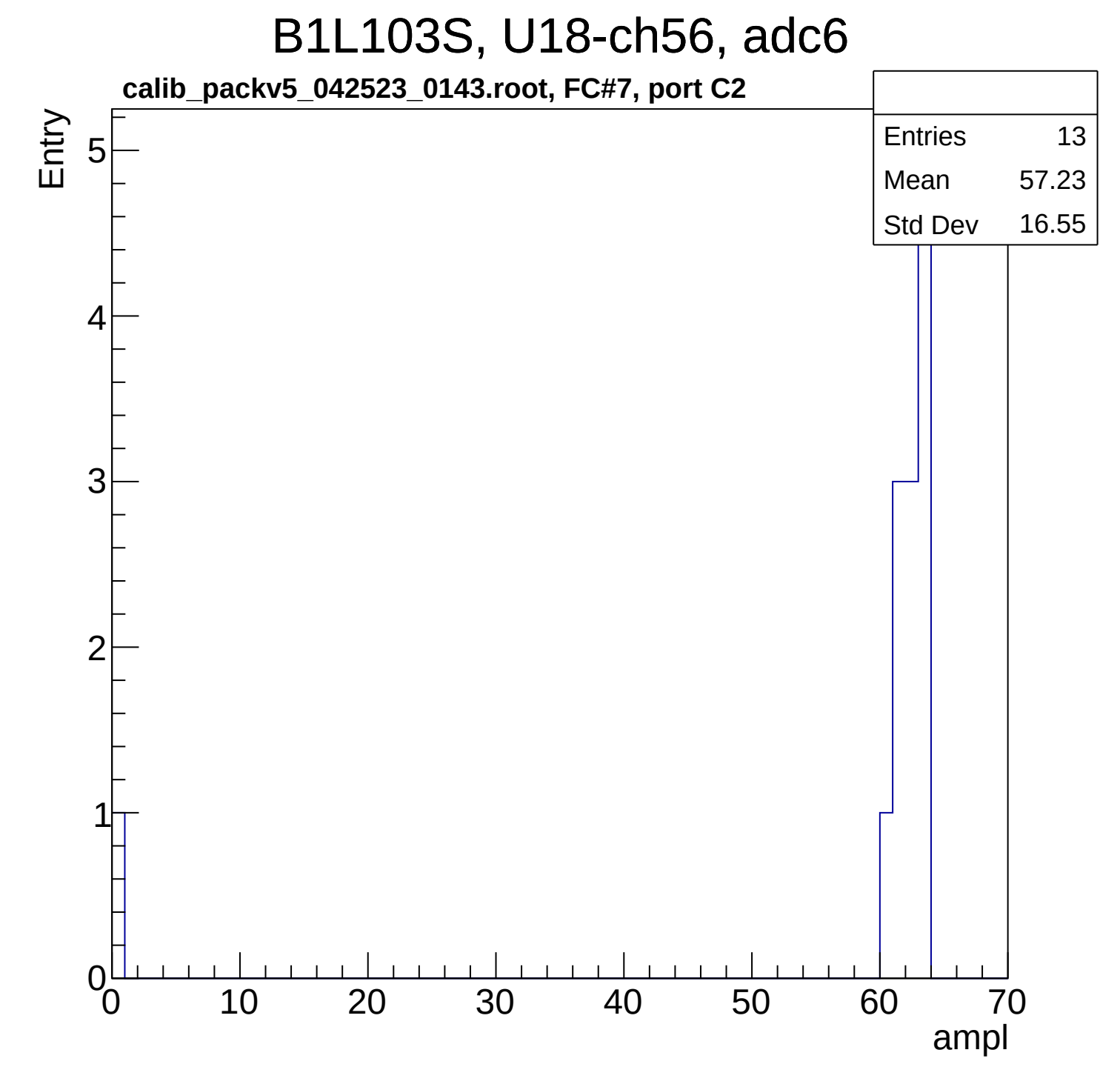
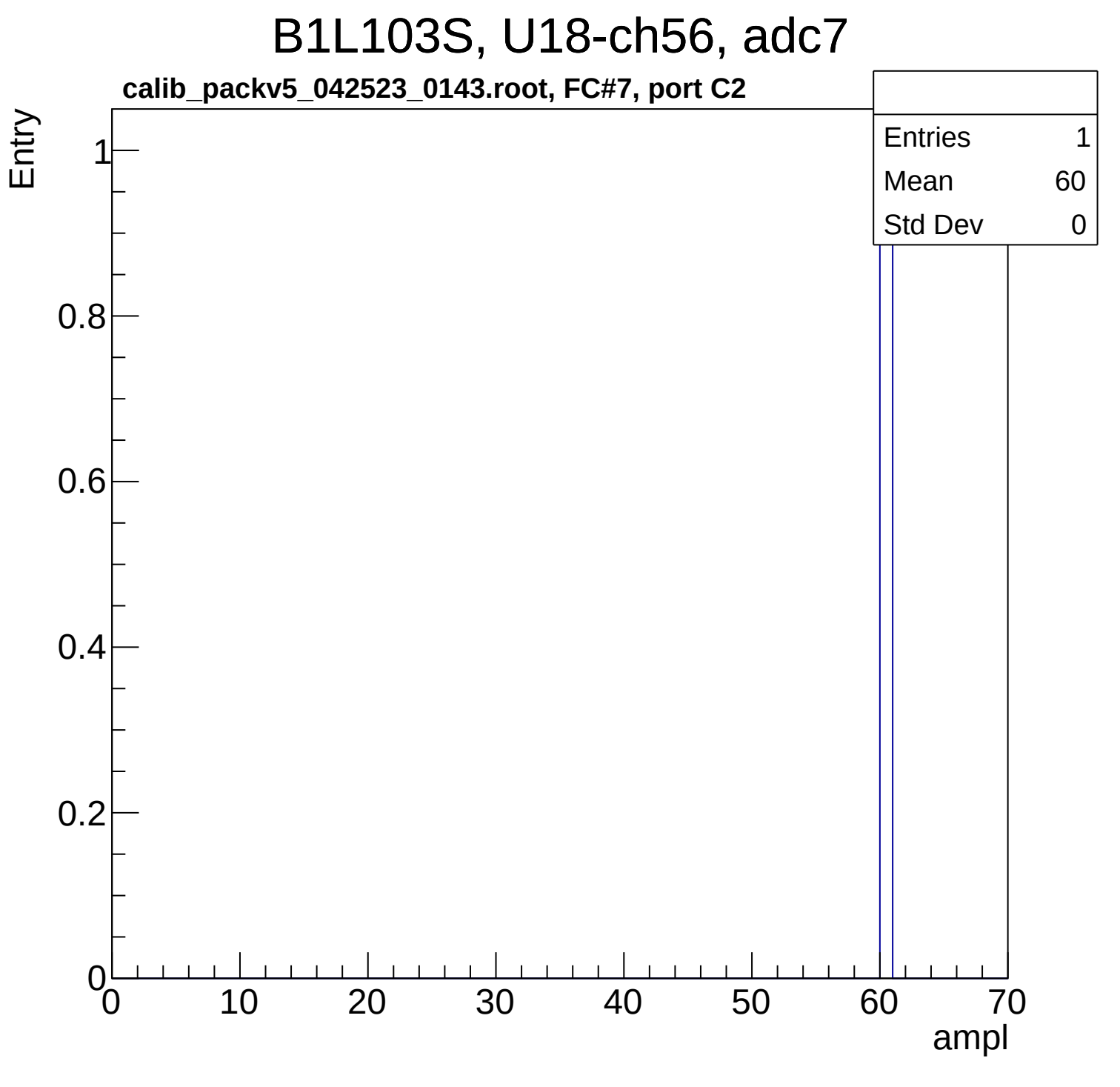
40
50
60
70


B1L103S, U18-ch56, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 56.42
Std Dev 3.236
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch56, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 34
Mean 59.5
Std Dev 2.464
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch56, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 13
Mean 57.23
Std Dev 16.55
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch56, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 60
Std Dev 0
Entry
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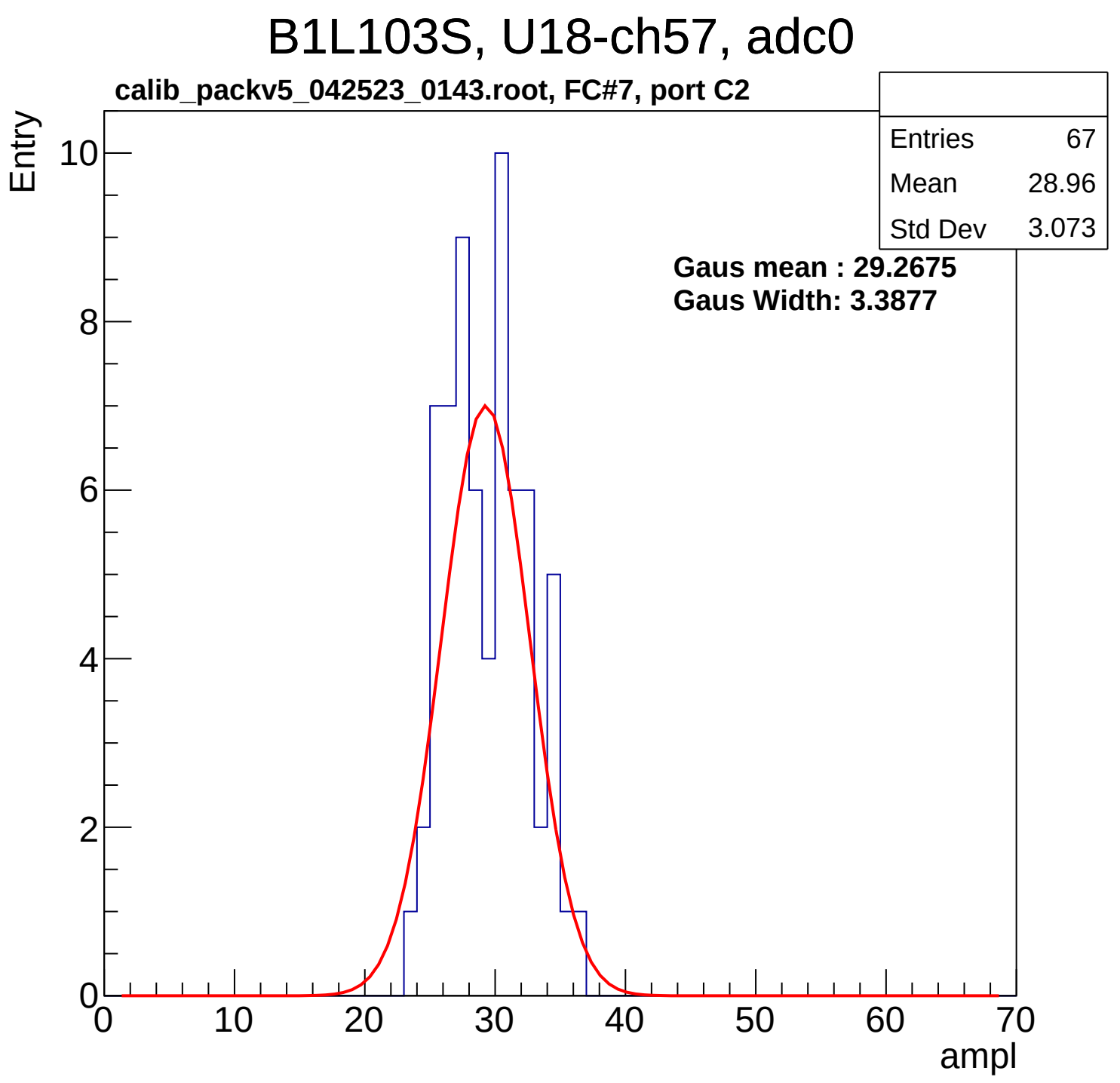
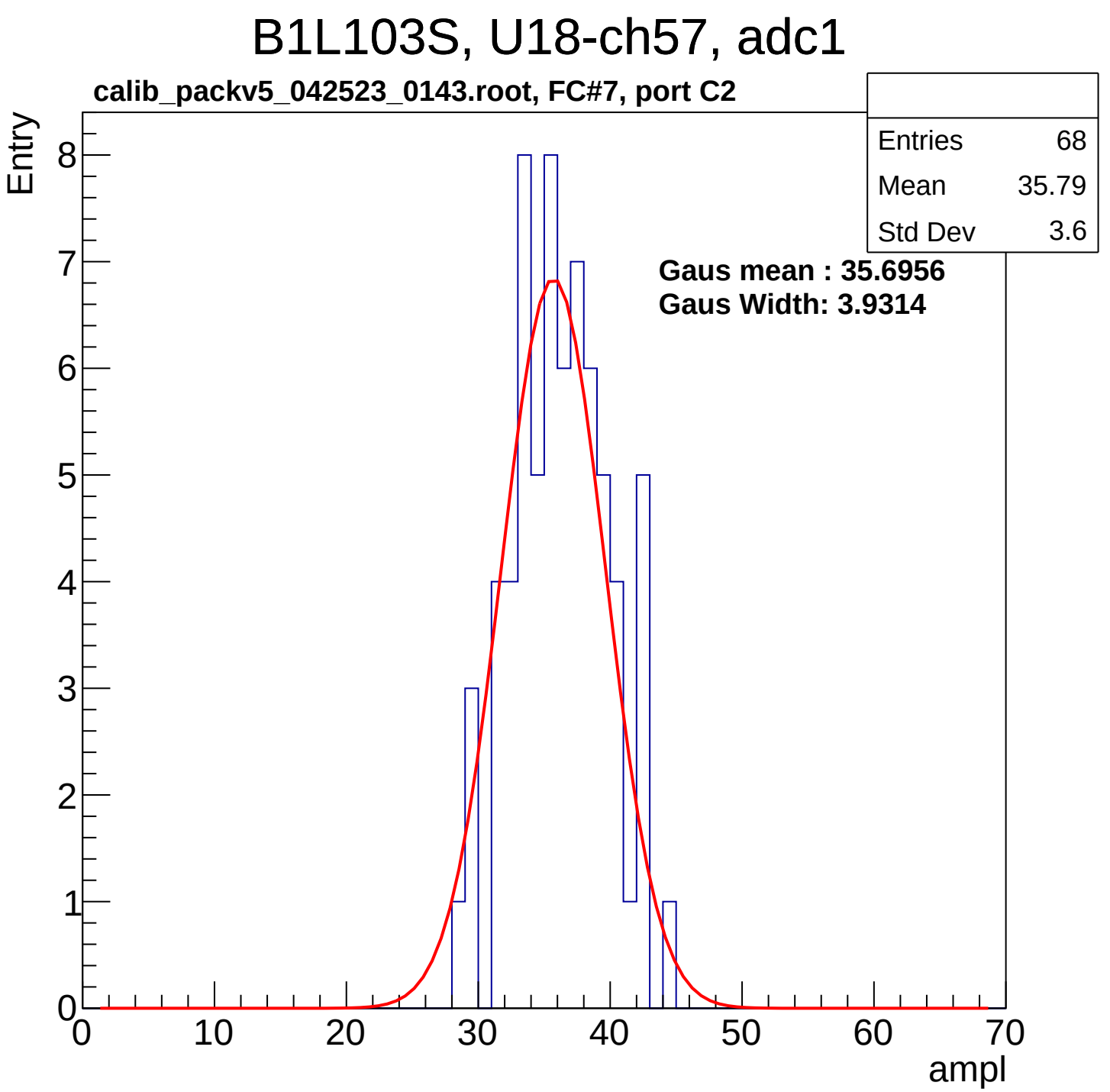
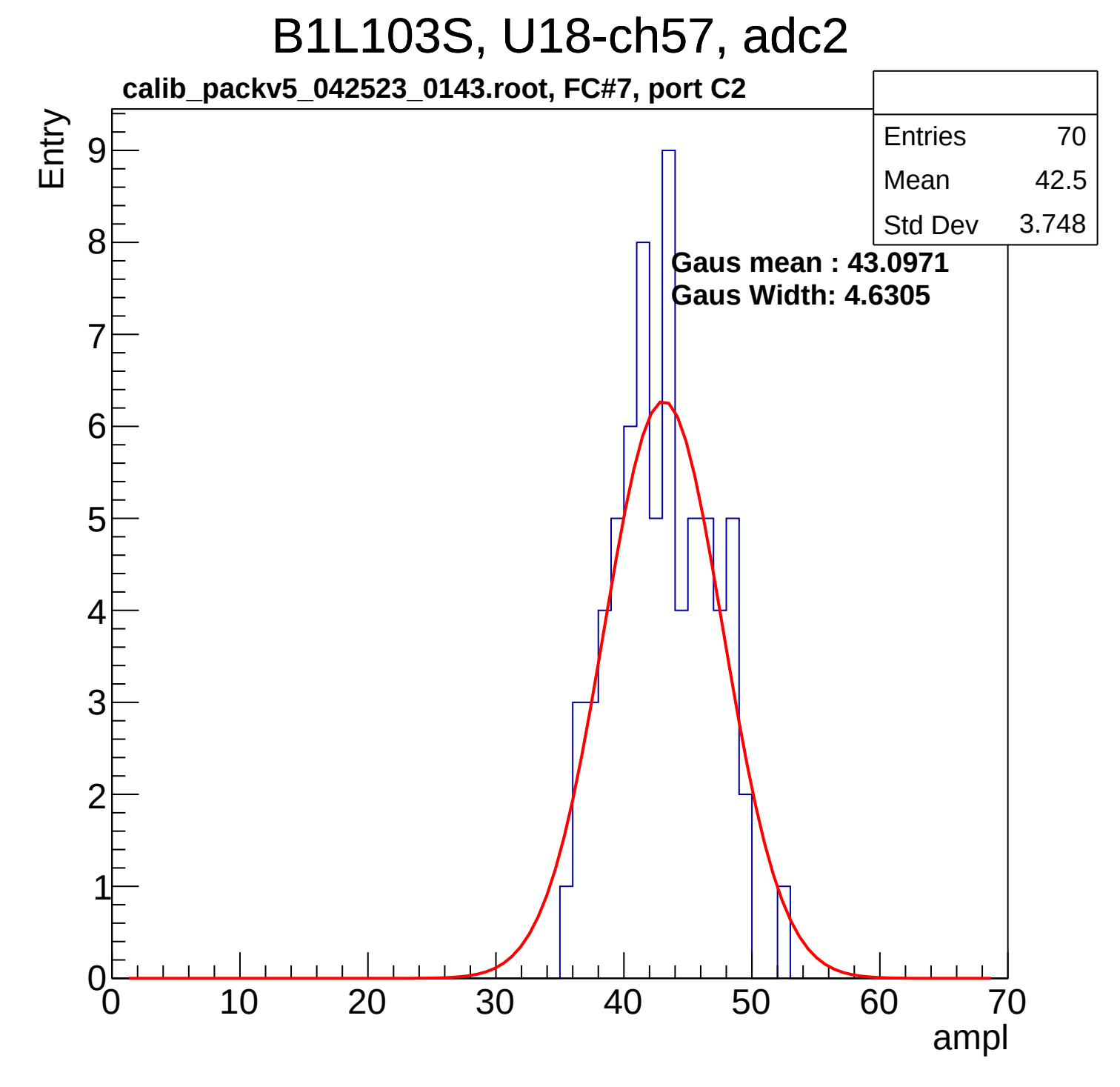
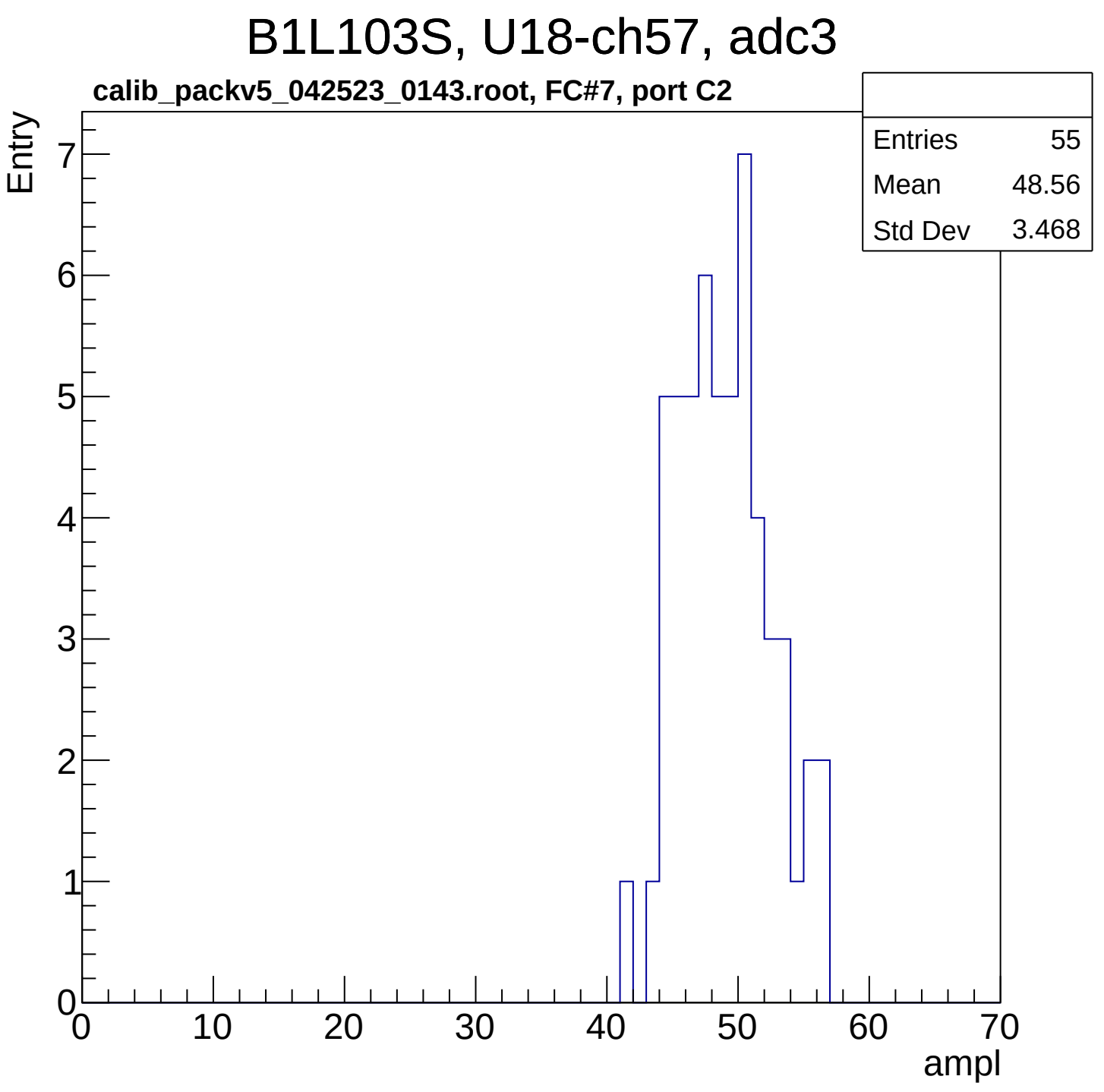
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch57, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 28.96
Std Dev 3.073
Gaus mean : 29.2675
Gaus Width: 3.3877
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch57, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 35.79
Std Dev 3.6
Gaus mean : 35.6956
Gaus Width: 3.9314
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch57, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 42.5
Std Dev 3.748
Gaus mean : 43.0971
Gaus Width: 4.6305
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch57, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 48.56
Std Dev 3.468
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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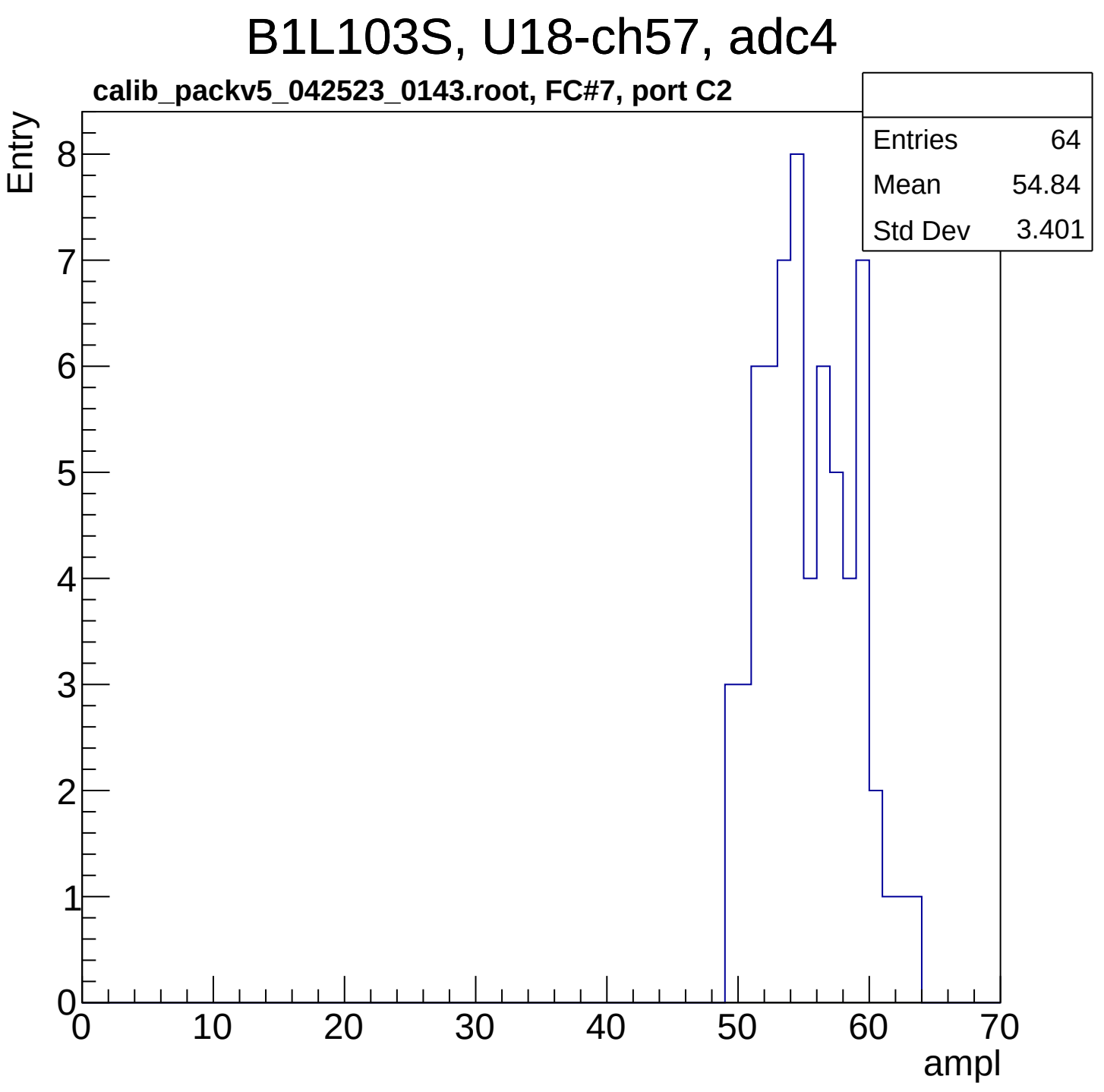
B1L103S, U18-ch57, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 54.84
Std Dev 3.401
Entry
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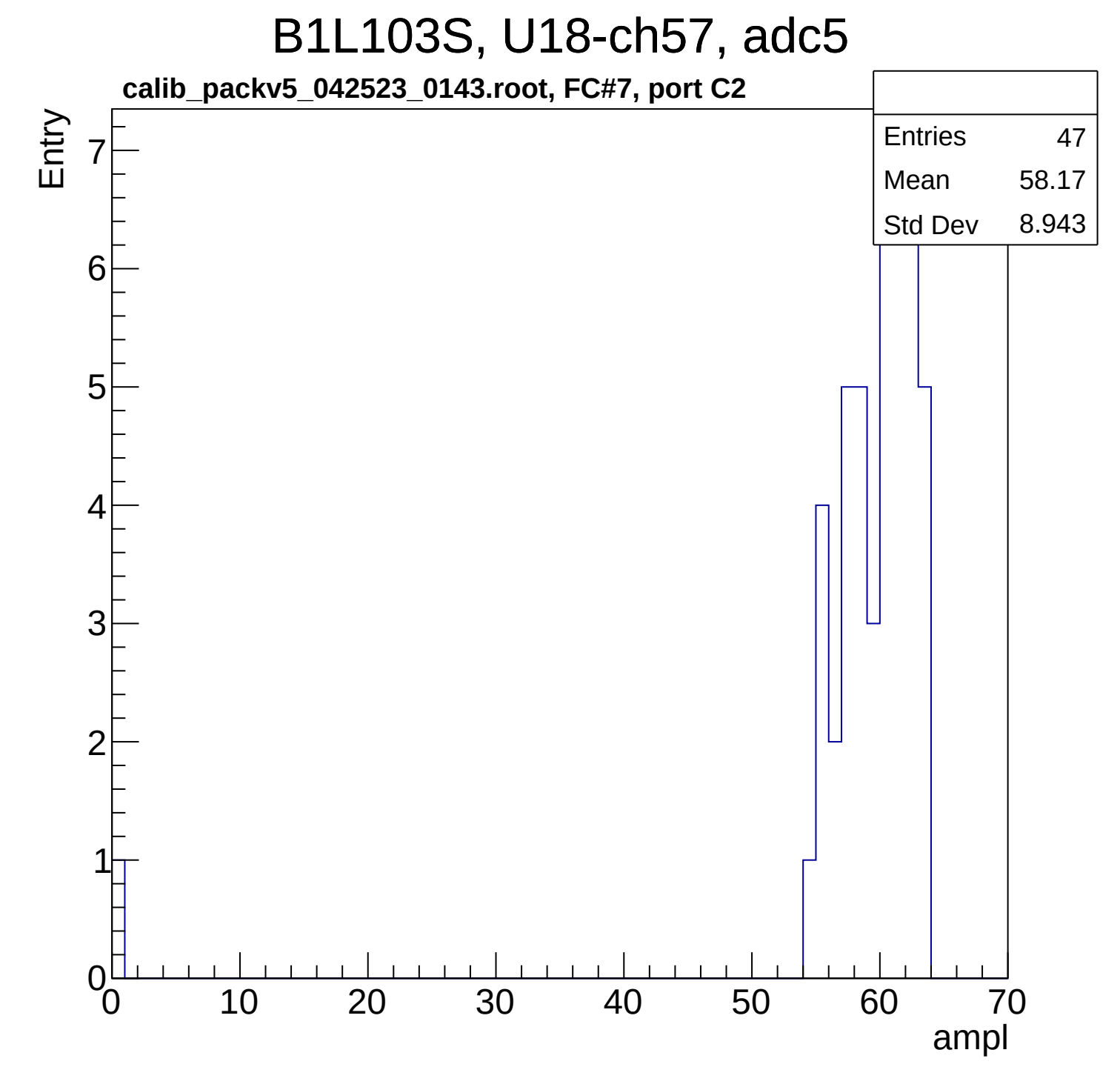
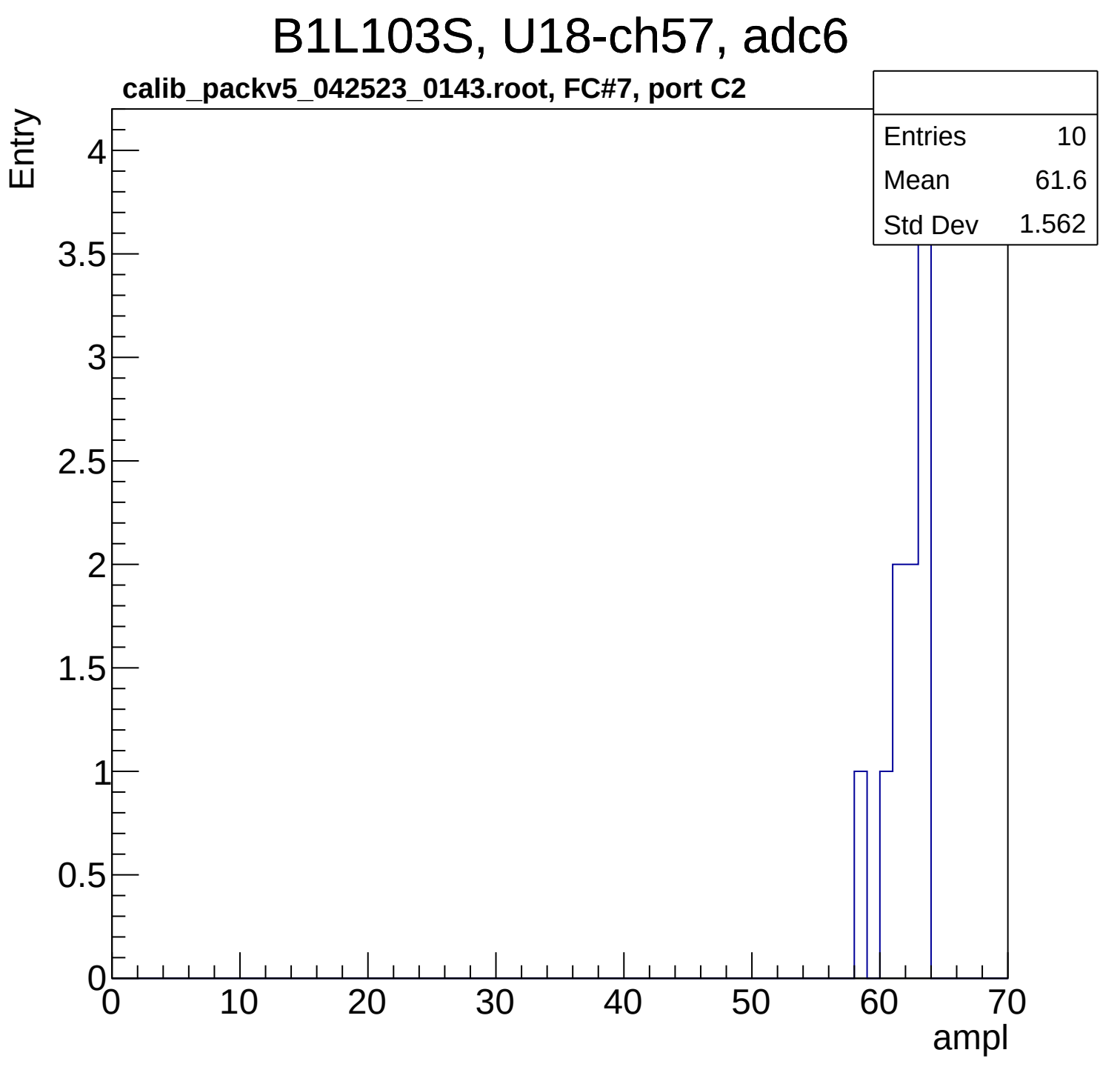
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch57, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 47
Mean 58.17
Std Dev 8.943
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch57, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 10
Mean 61.6
Std Dev 1.562
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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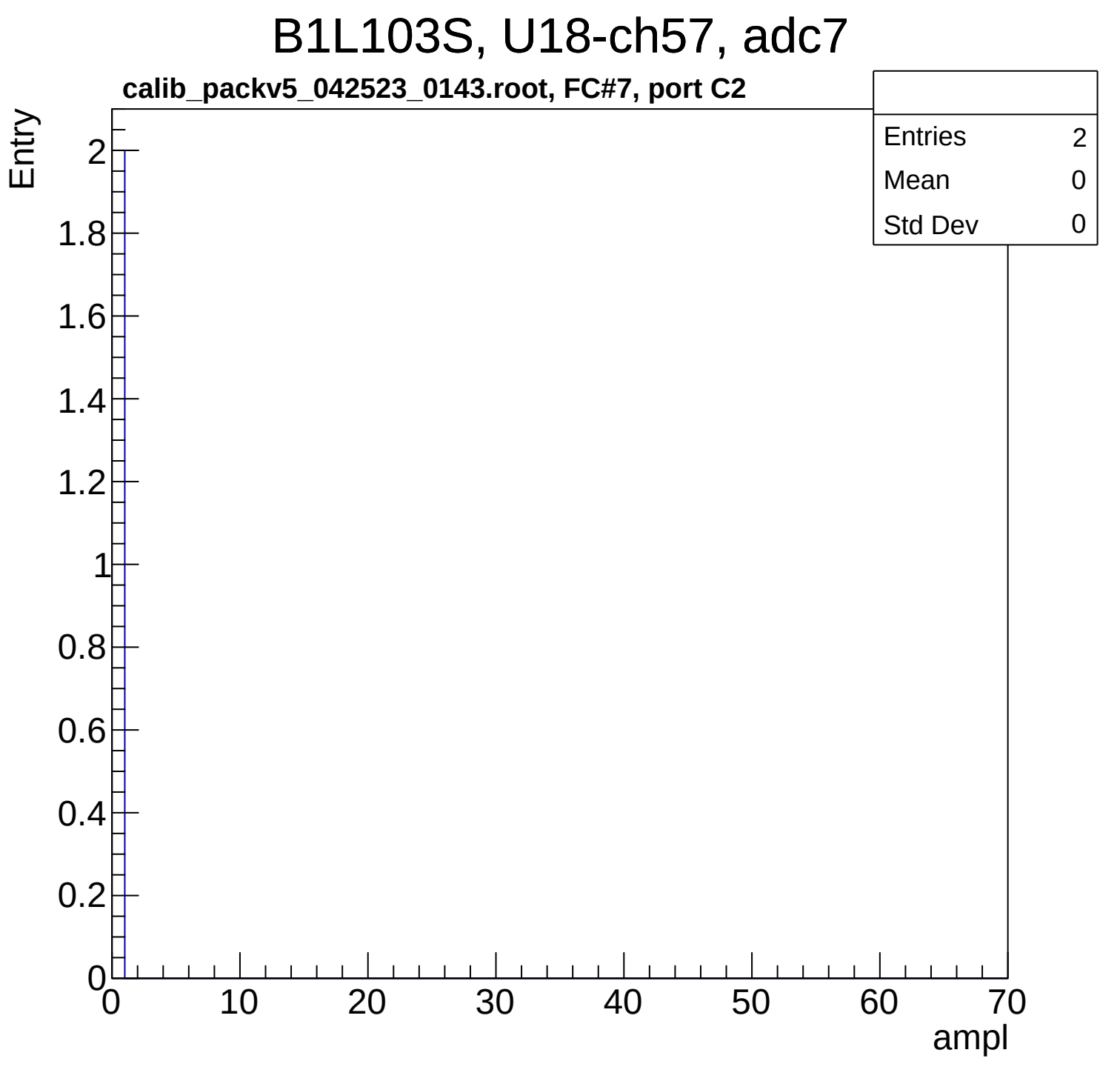
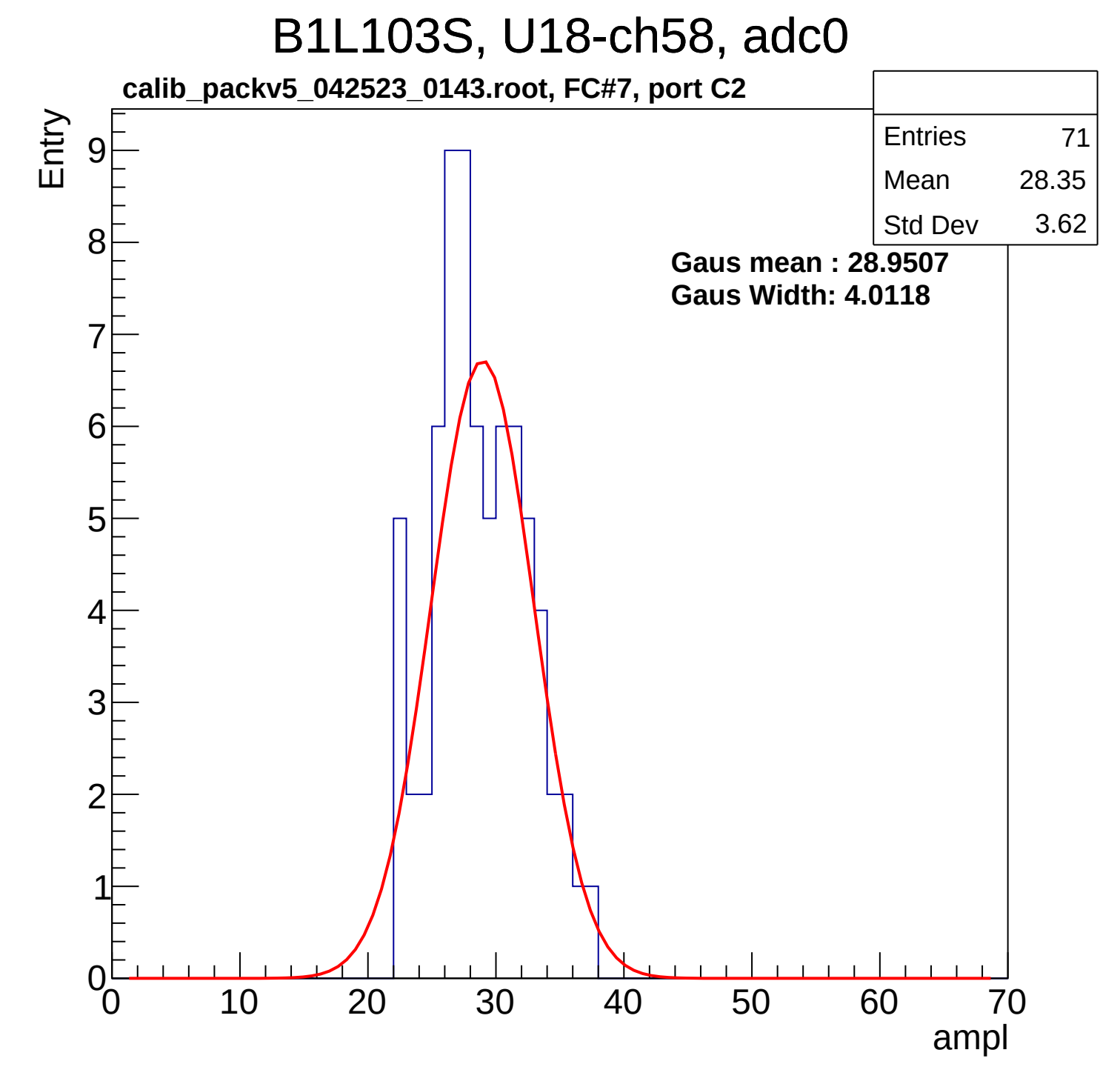
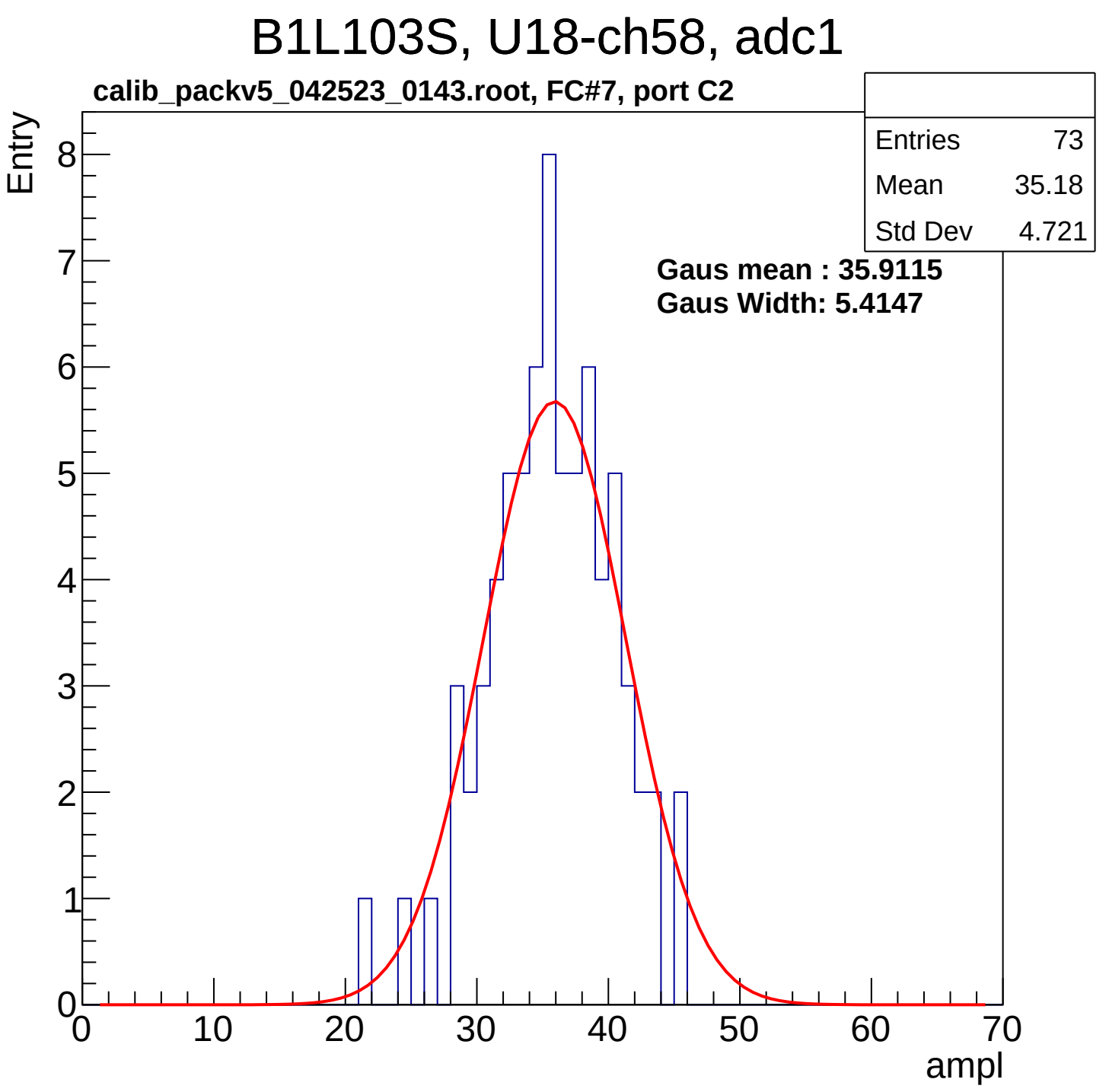
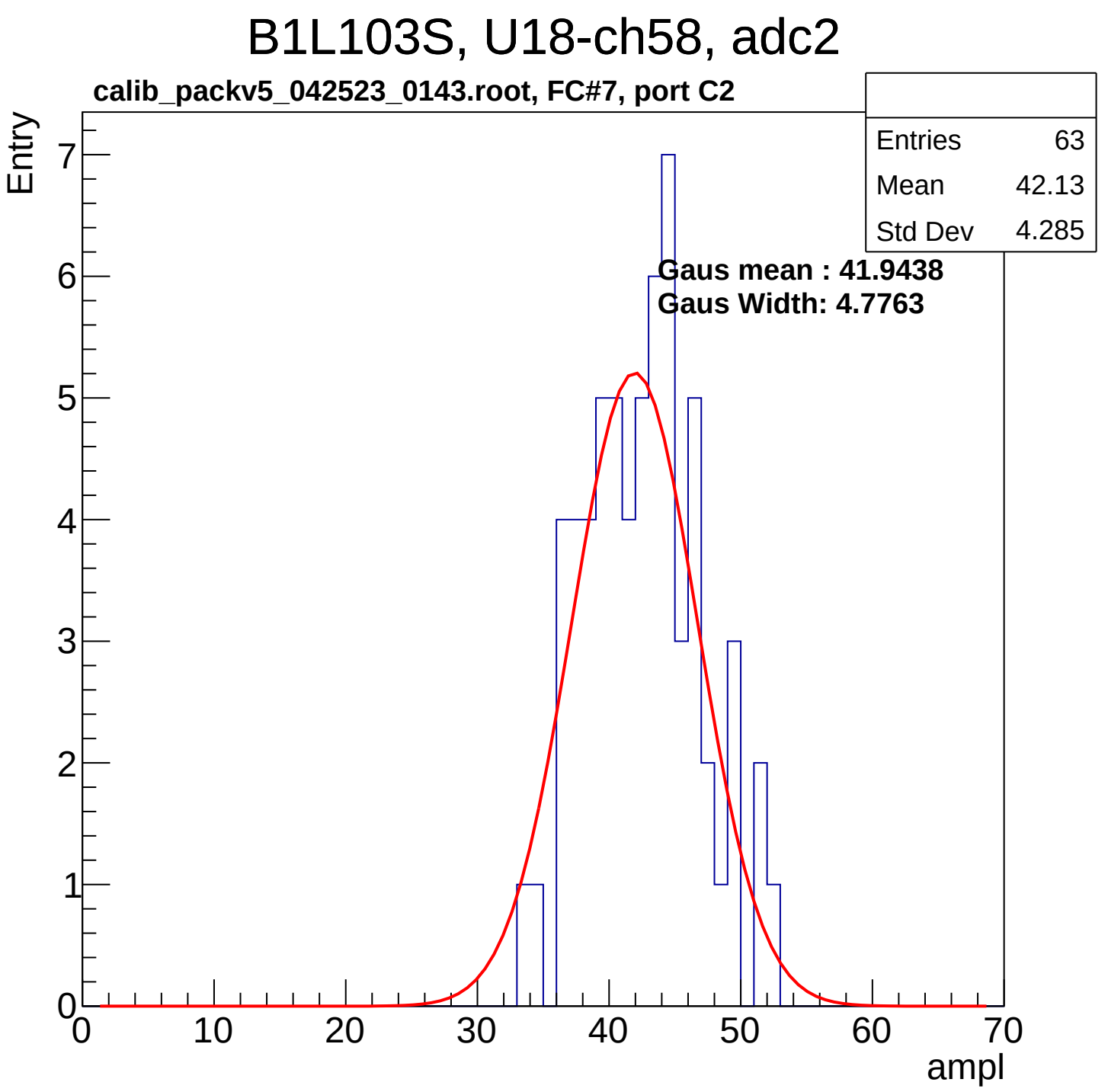
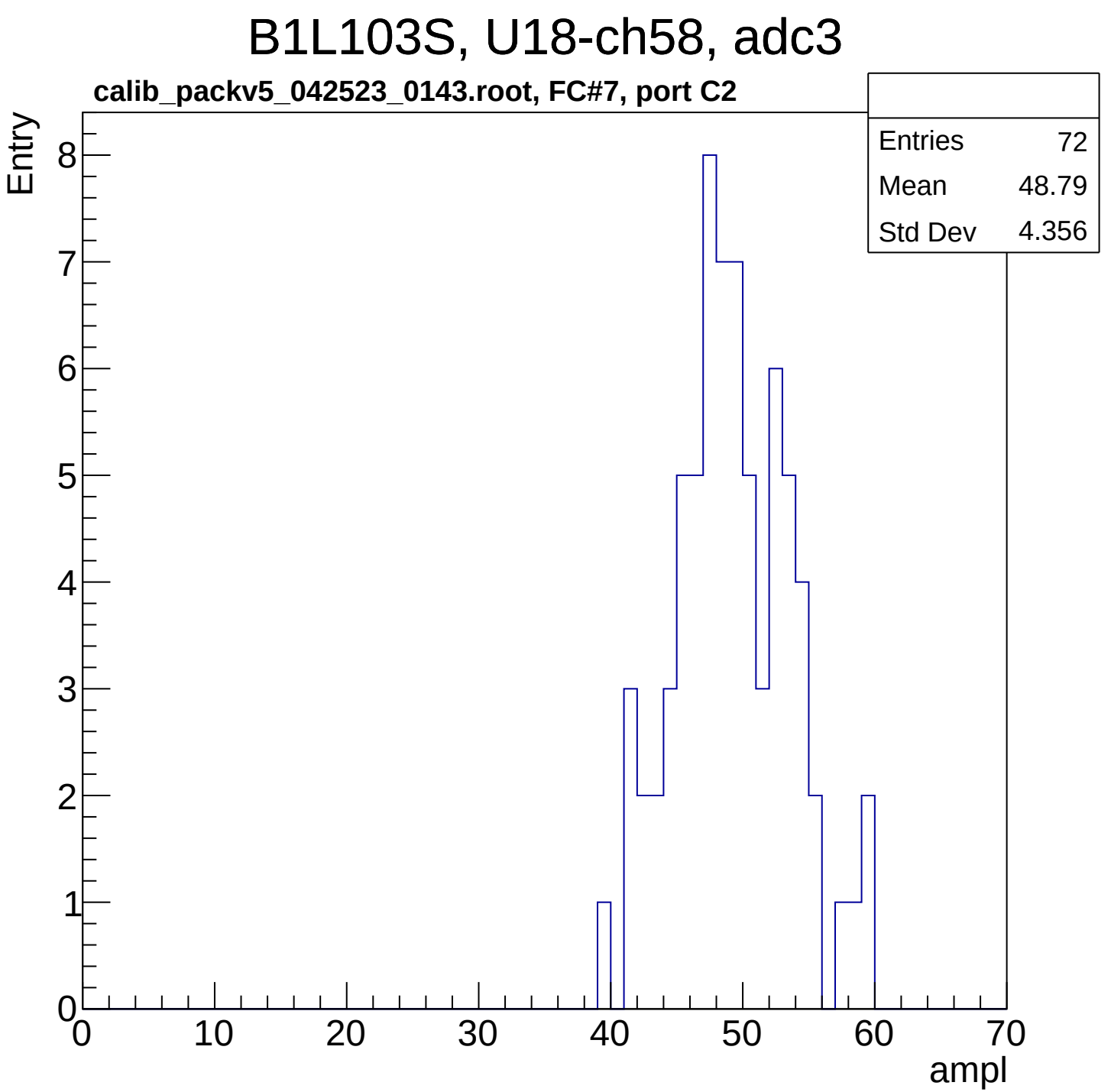
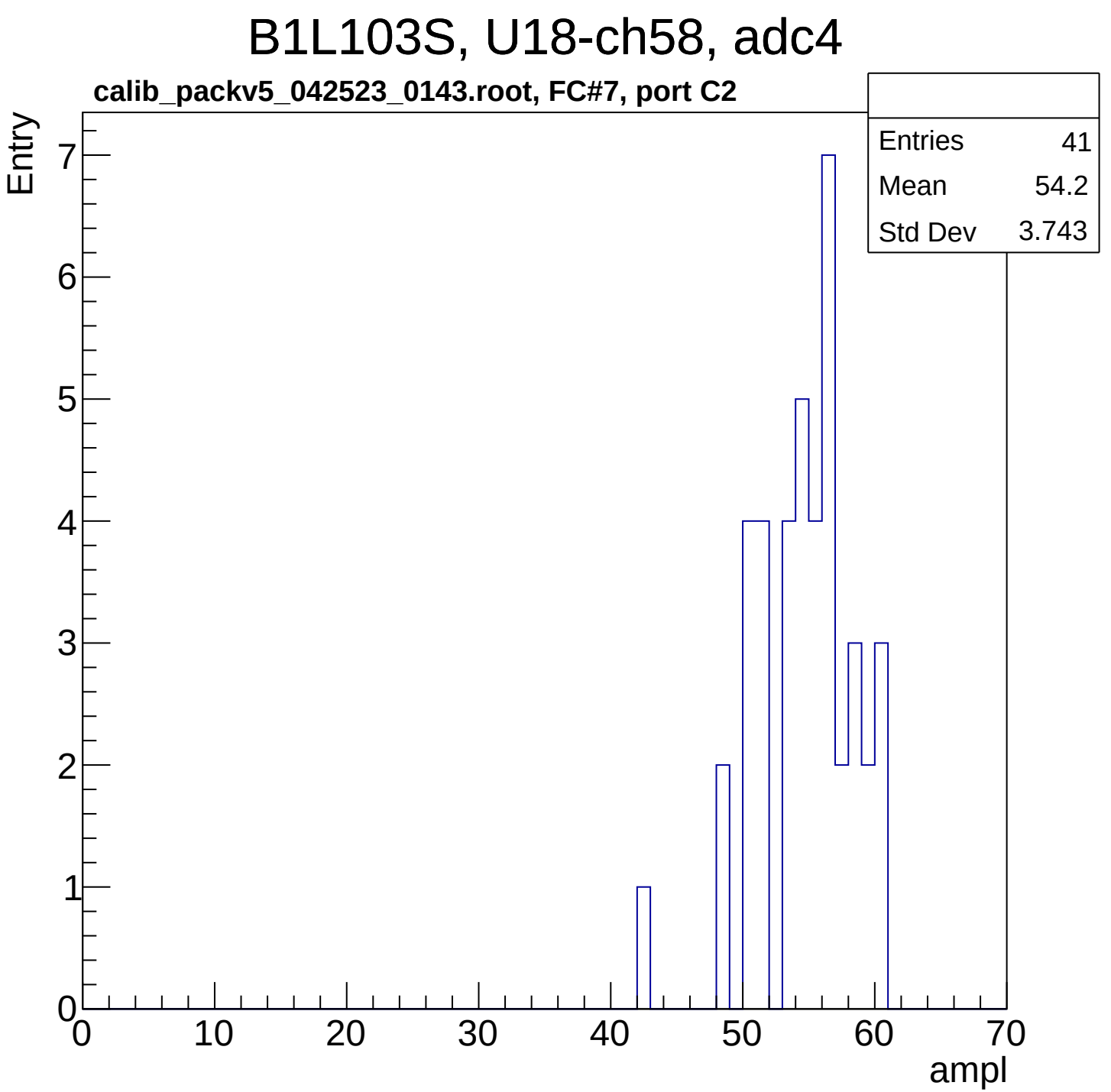

B1L103S, U18-ch57, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 0
Std Dev 0
Entry
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70
ampl

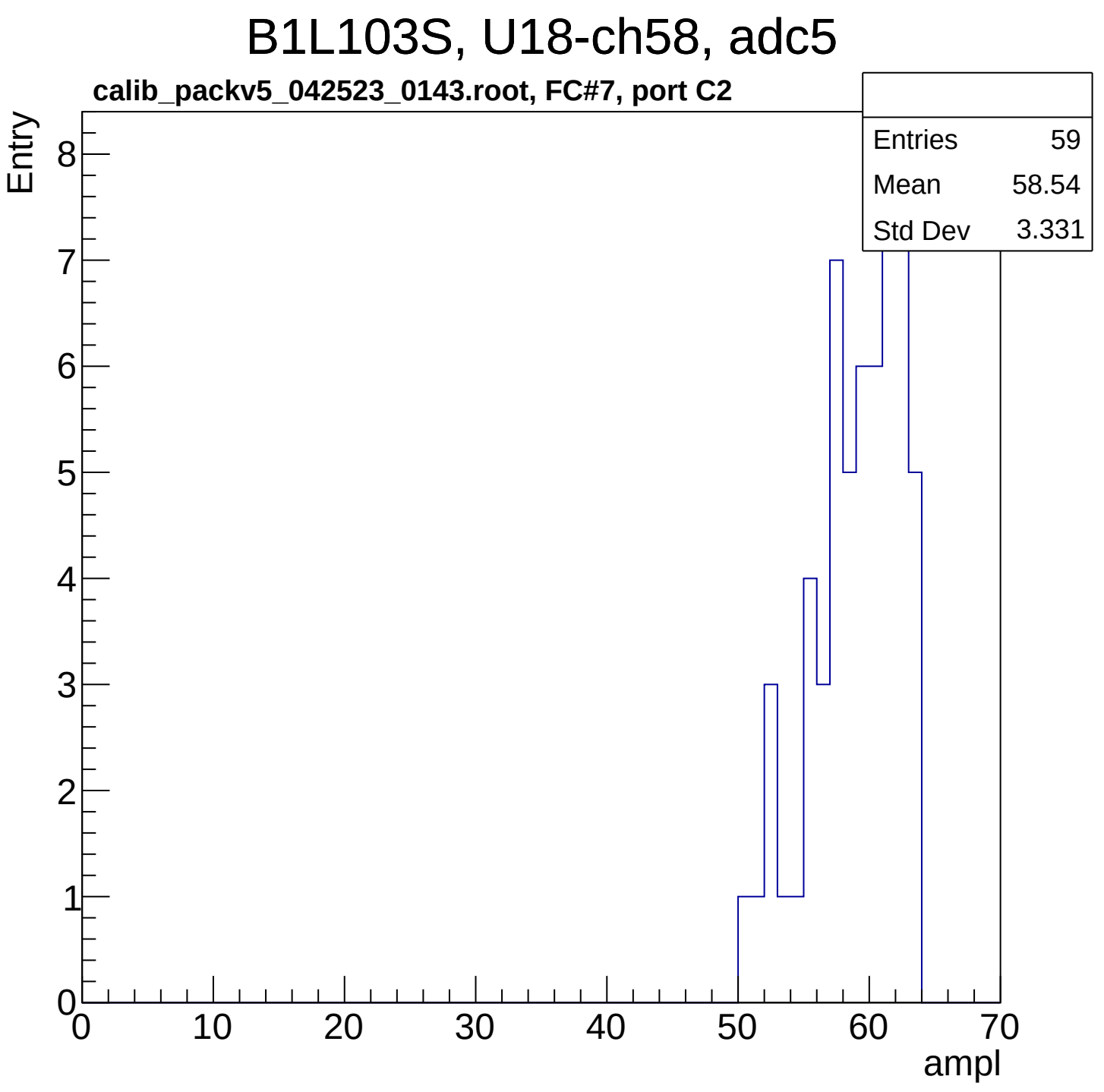

B1L103S, U18-ch58, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 71
Mean 28.35
Std Dev 3.62
Gaus mean : 28.9507
Gaus Width: 4.0118
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch58, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 73
Mean 35.18
Std Dev 4.721
Gaus mean : 35.9115
Gaus Width: 5.4147
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch58, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 42.13
Std Dev 4.285
Gaus mean : 41.9438
Gaus Width: 4.7763
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch58, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 72
Mean 48.79
Std Dev 4.356
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch58, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 41
Mean 54.2
Std Dev 3.743
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch58, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 58.54
Std Dev 3.331
Entry
ampl
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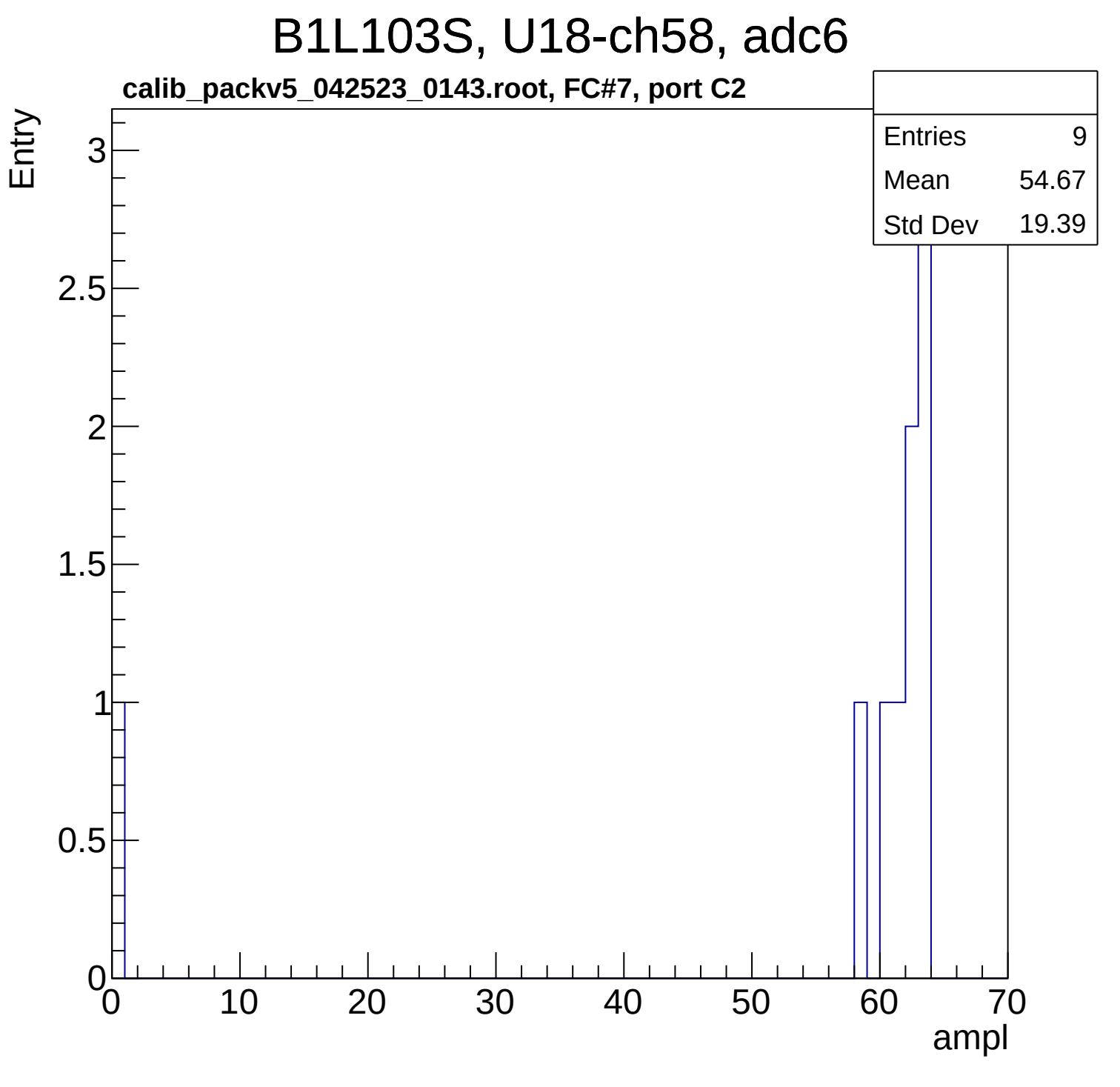
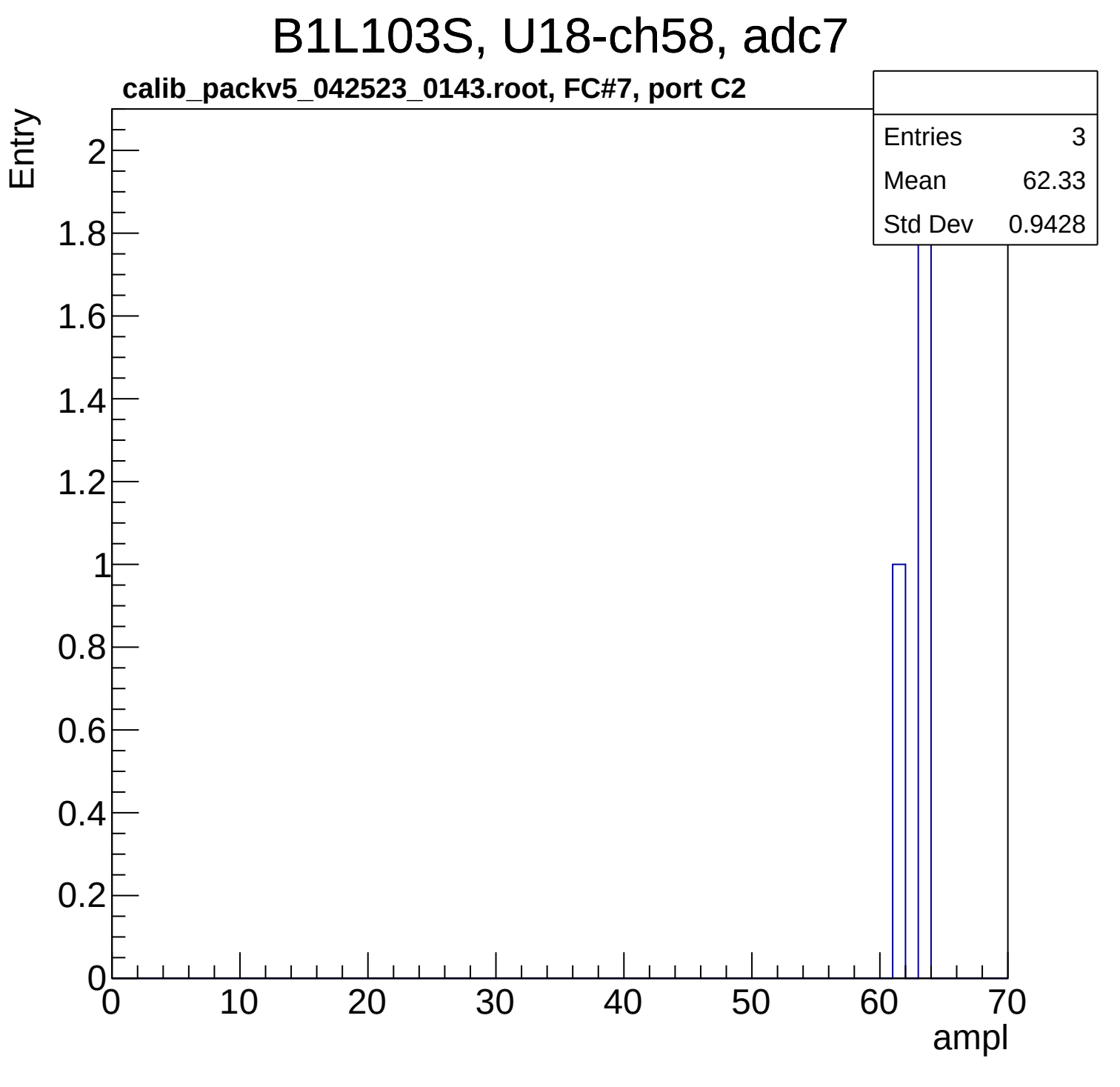
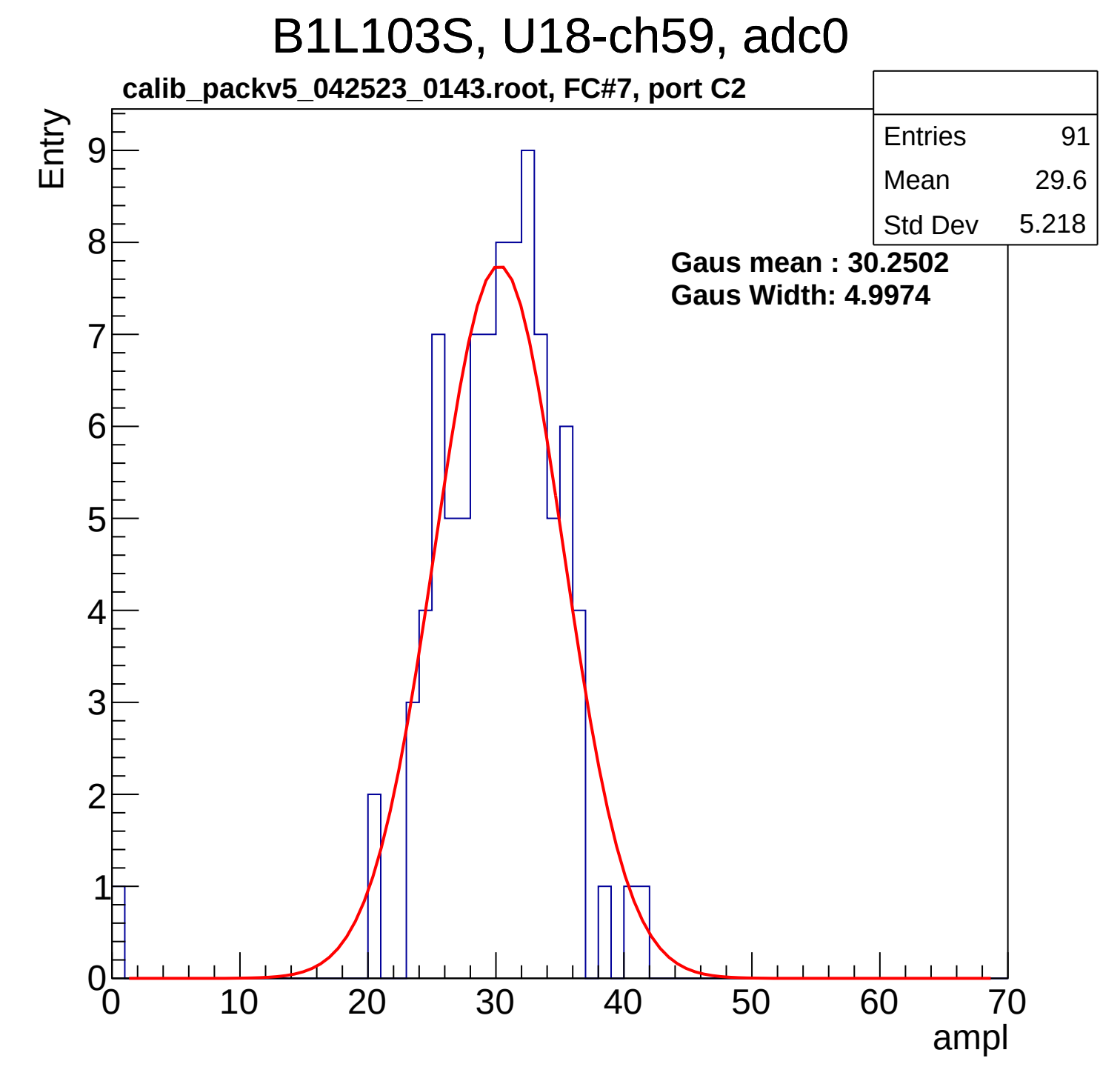
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch58, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 9
Mean 54.67
Std Dev 19.39
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U18-ch58, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 62.33
Std Dev 0.9428
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U18-ch59, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 91
Mean 29.6
Std Dev 5.218
Gaus mean : 30.2502
Gaus Width: 4.9974
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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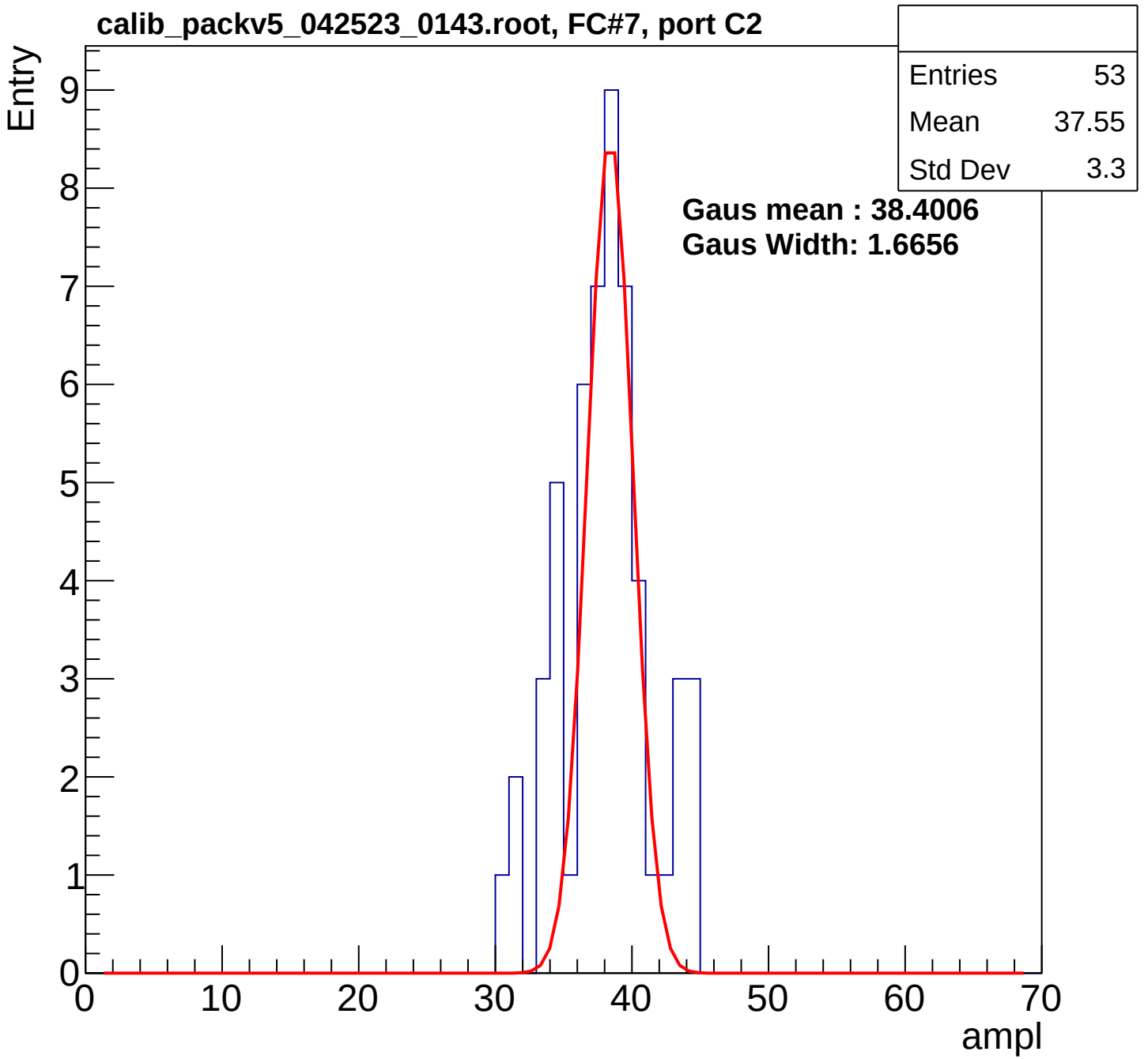
B1L103S, U18-ch59, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 37.55
Std Dev 3.3
Gaus mean : 38.4006
Gaus Width: 1.6656
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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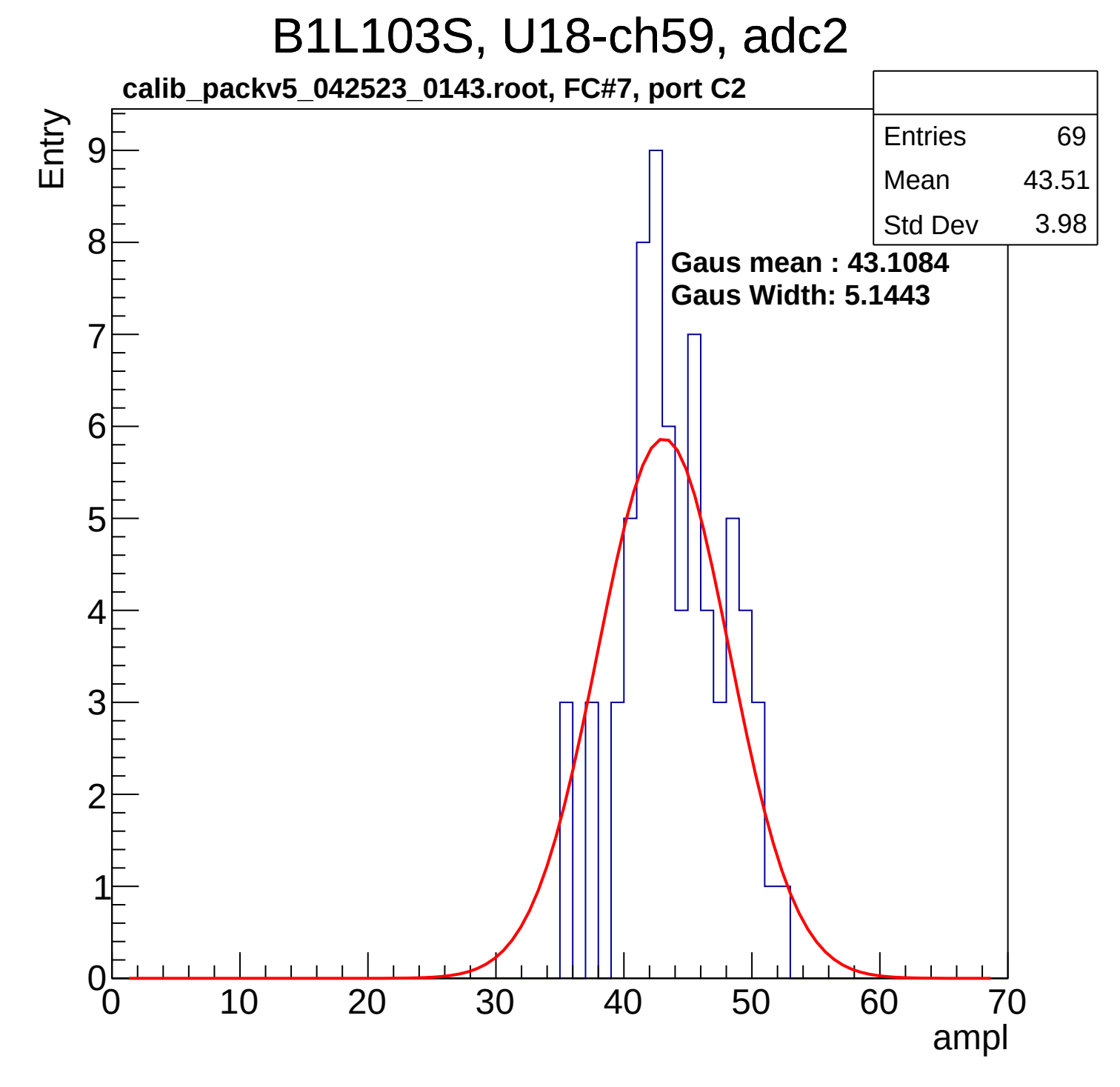
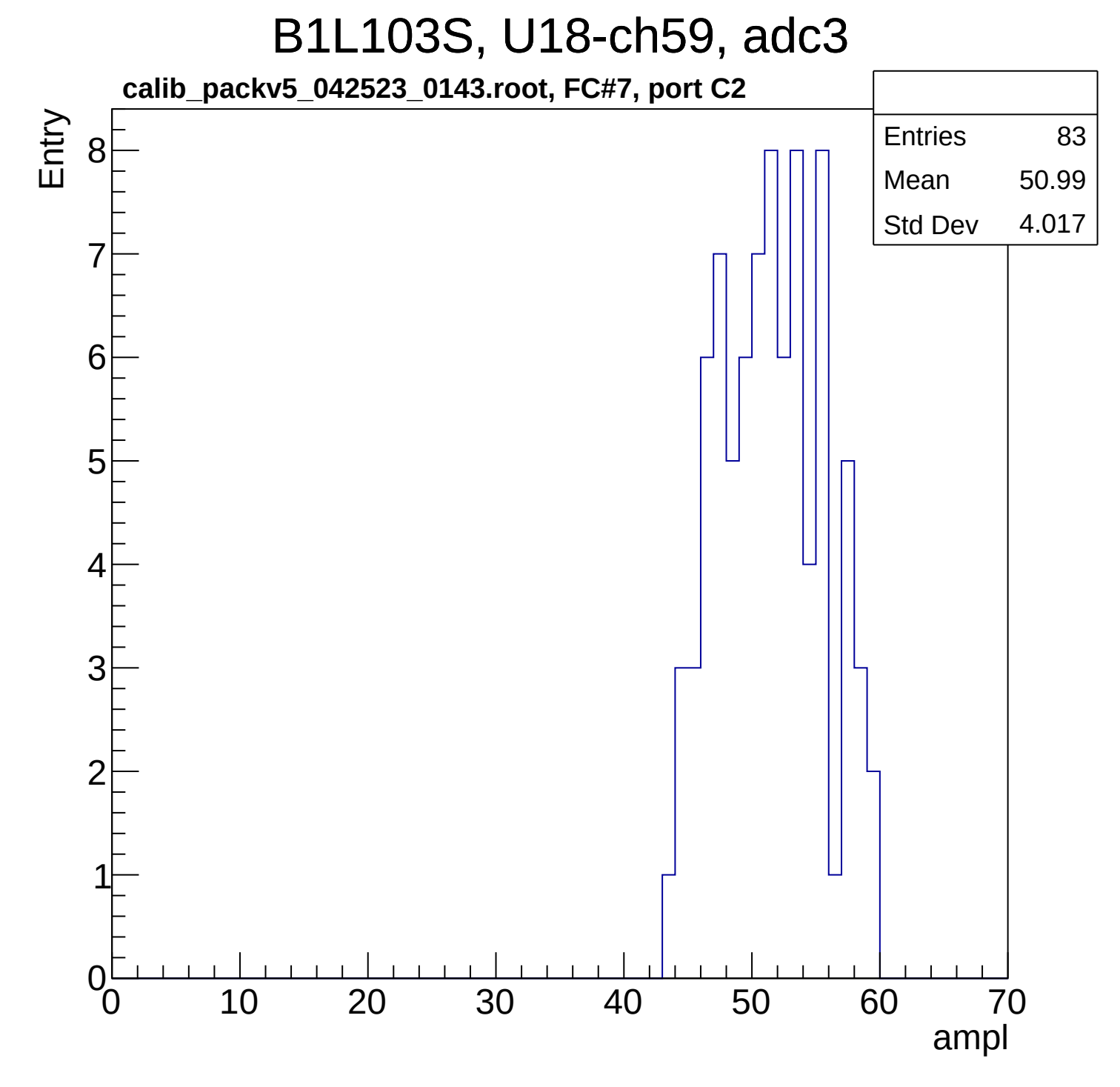
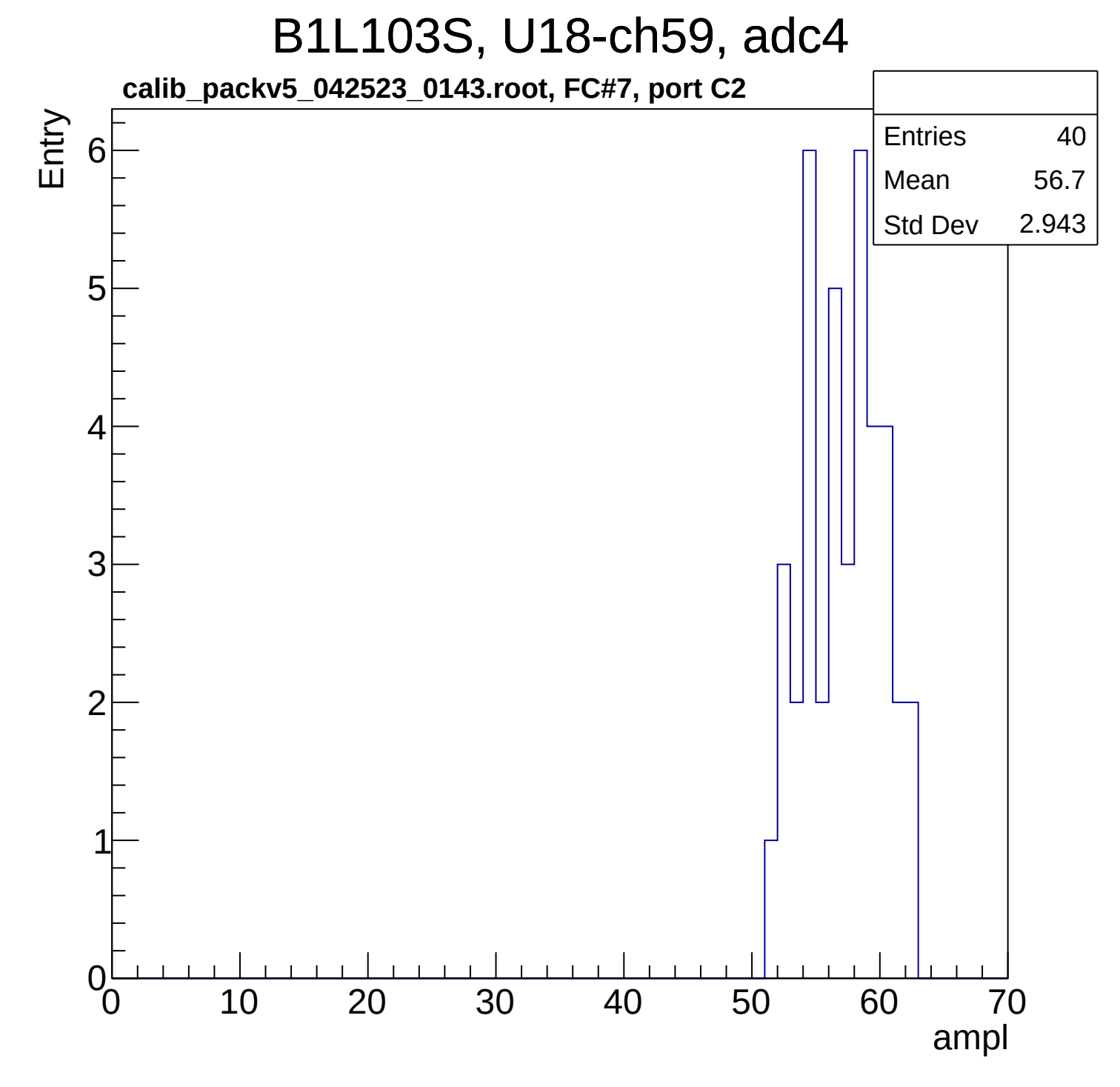
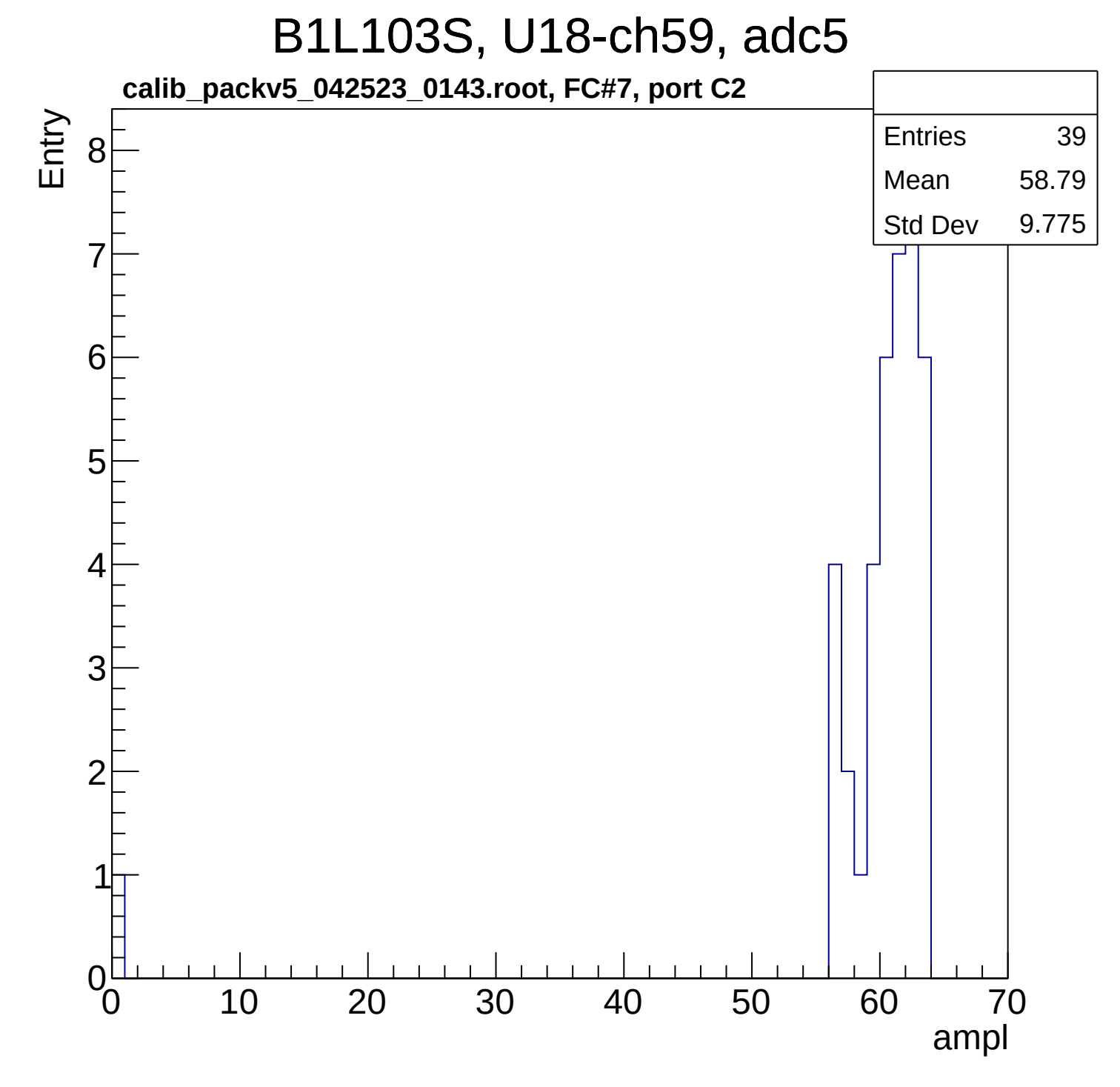

B1L103S, U18-ch59, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 43.51
Std Dev 3.98
Gaus mean : 43.1084
Gaus Width: 5.1443
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch59, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 83
Mean 50.99
Std Dev 4.017
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch59, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 40
Mean 56.7
Std Dev 2.943
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch59, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 39
Mean 58.79
Std Dev 9.775
Entry
ampl
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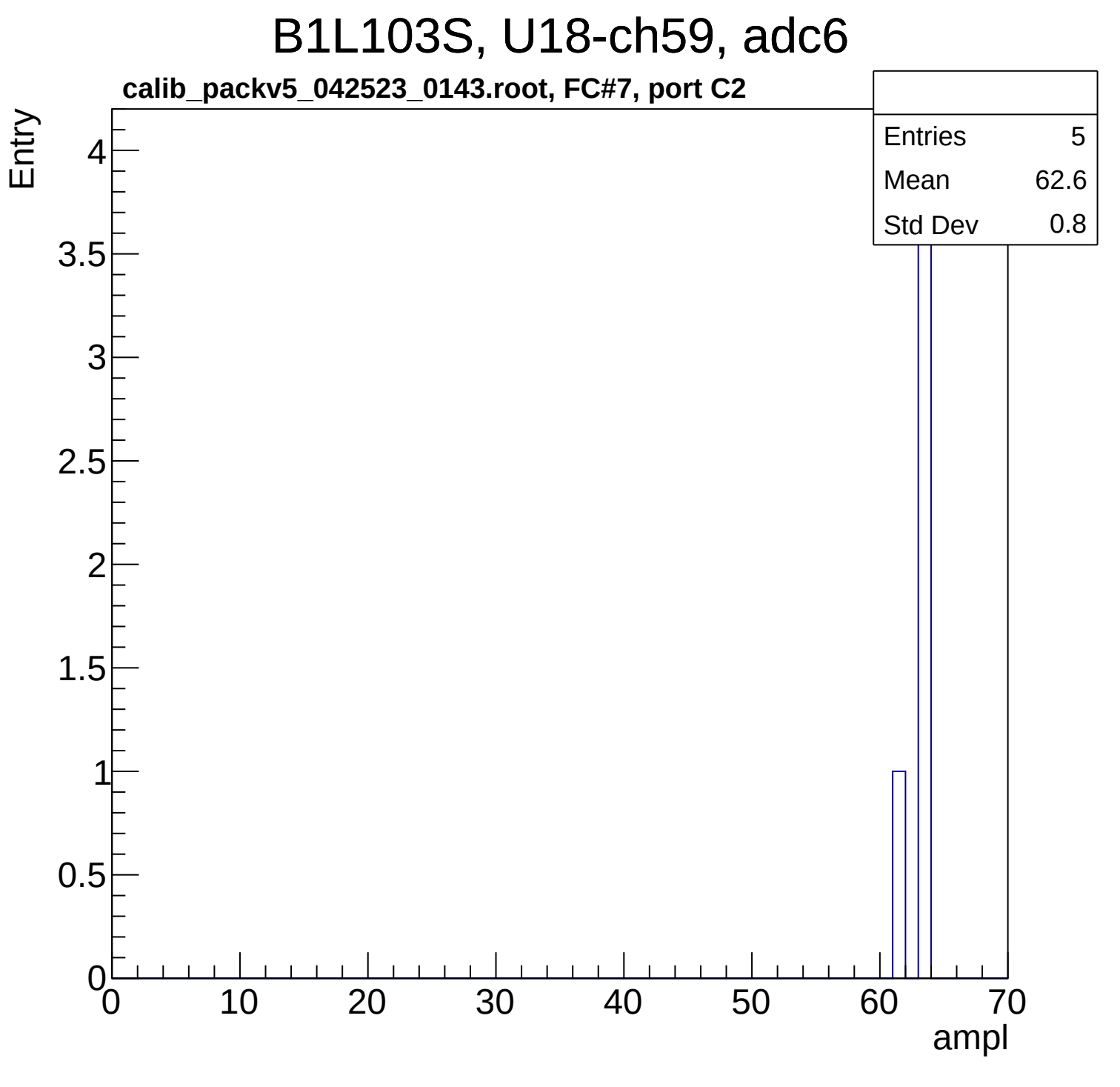
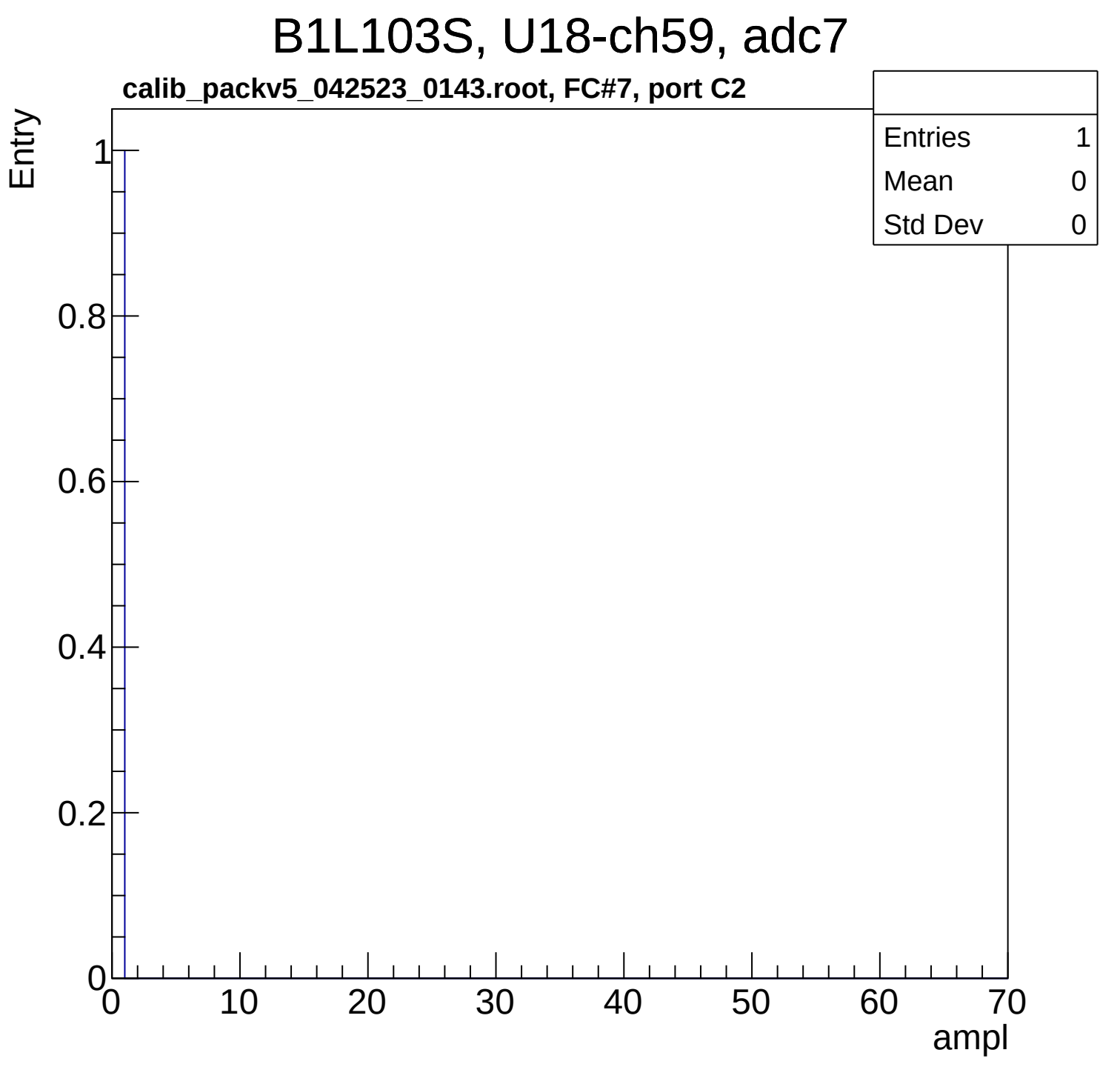
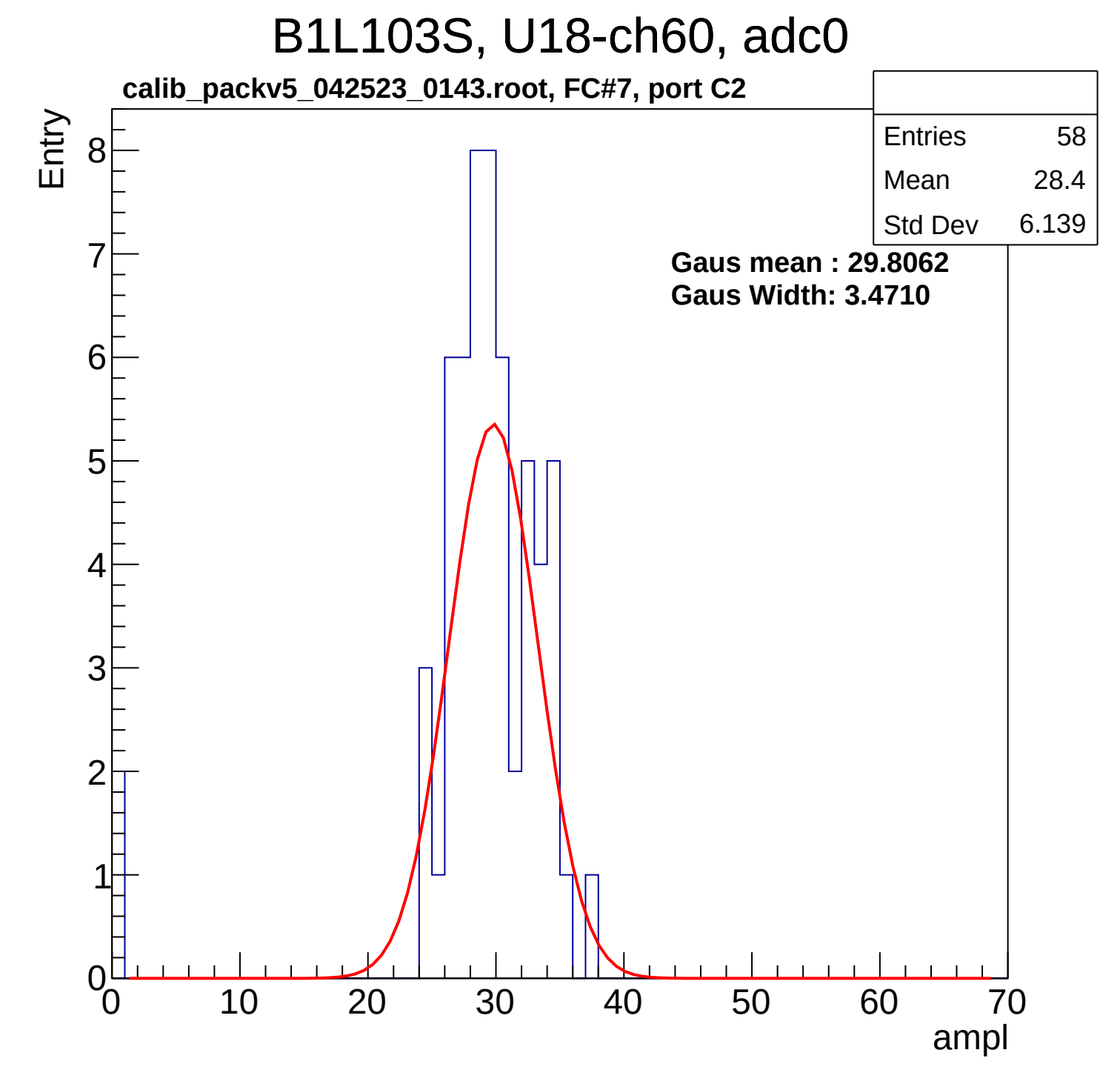
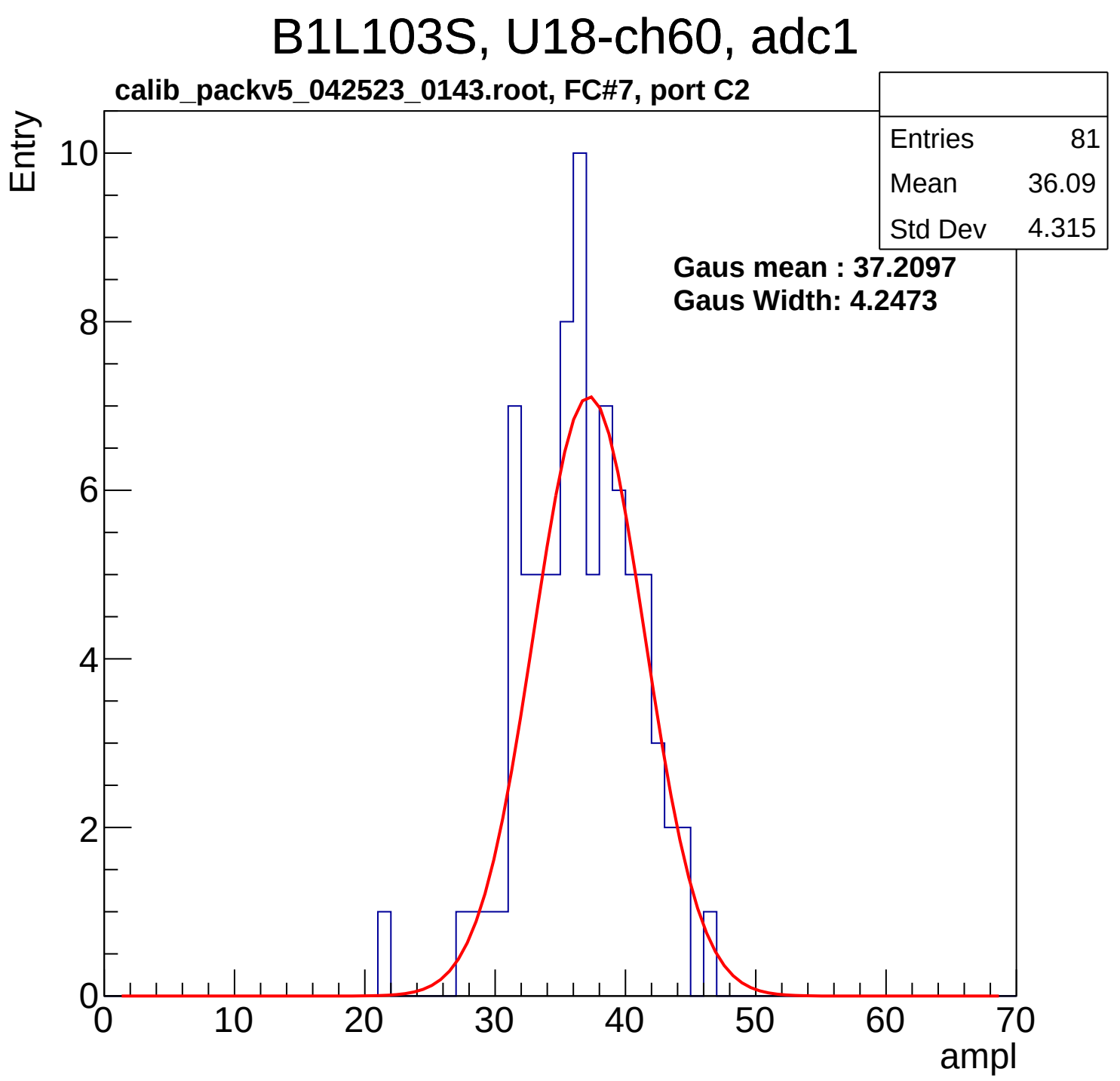
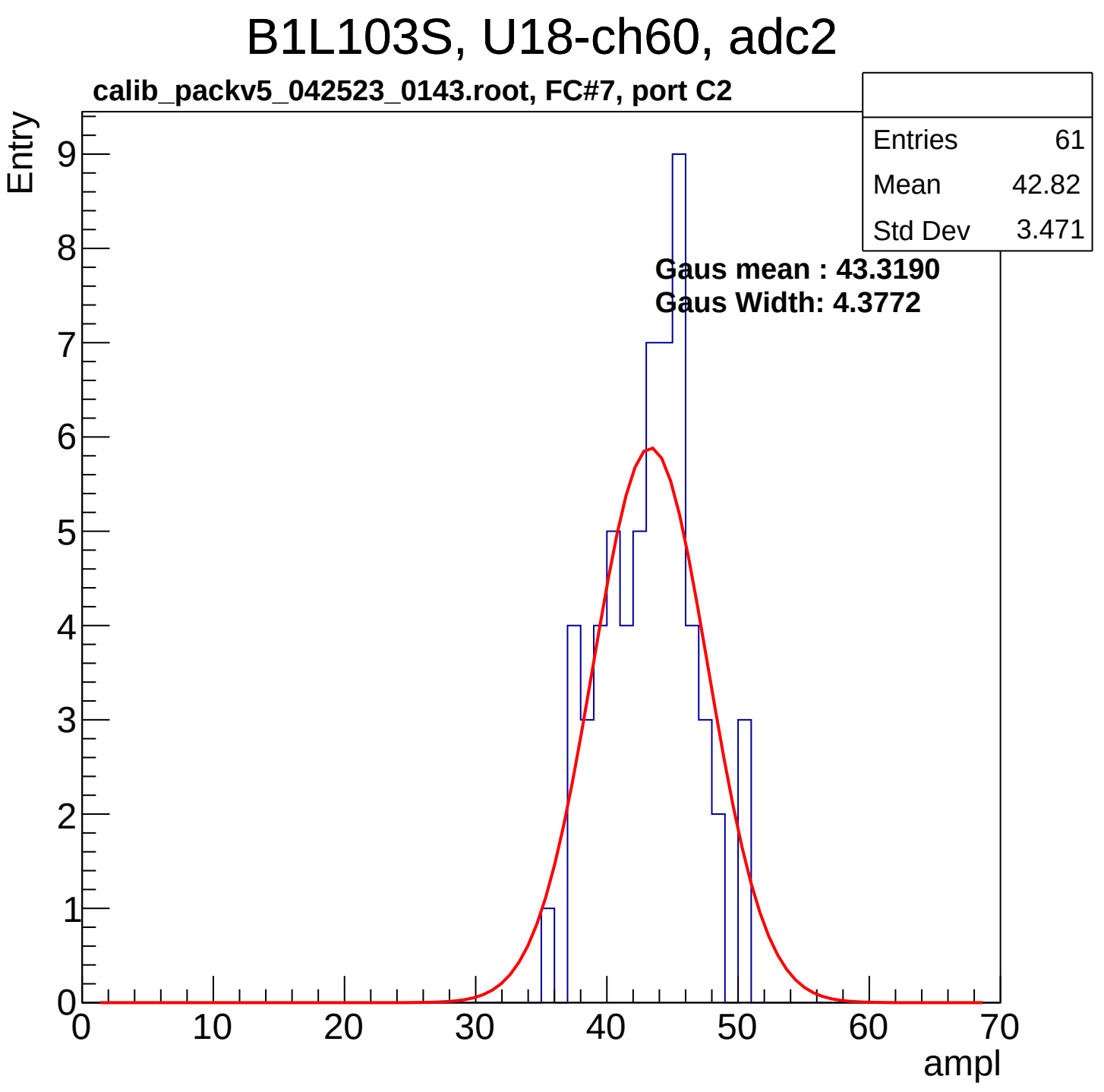
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch59, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 5
Mean 62.6
Std Dev 0.8
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U18-ch59, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch60, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 58
Mean 28.4
Std Dev 6.139
Gaus mean : 29.8062
Gaus Width: 3.4710
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch60, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 81
Mean 36.09
Std Dev 4.315
Gaus mean : 37.2097
Gaus Width: 4.2473
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch60, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 61
Mean 42.82
Std Dev 3.471
Gaus mean : 43.3190
Gaus Width: 4.3772
Entry
ampl
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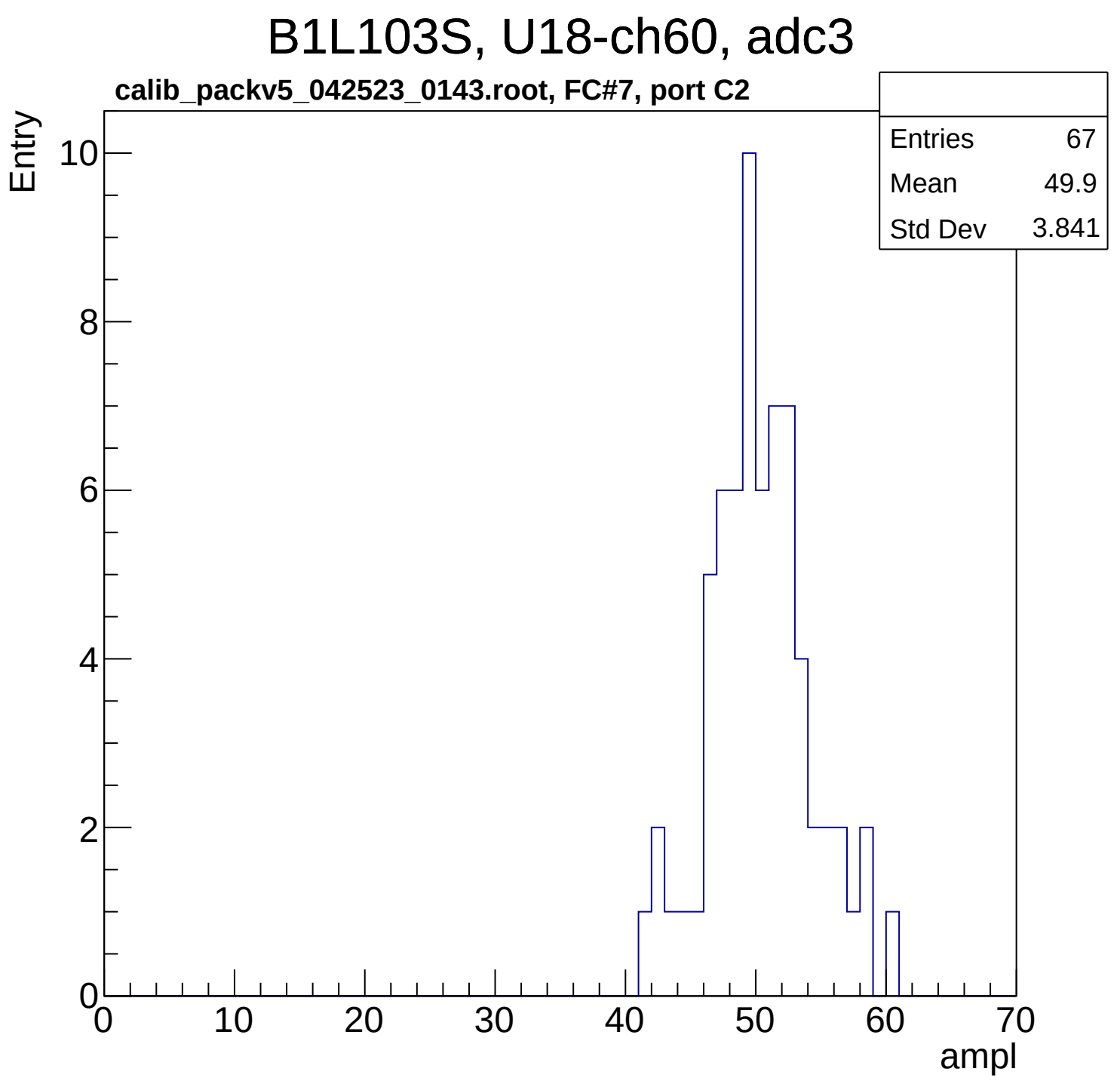
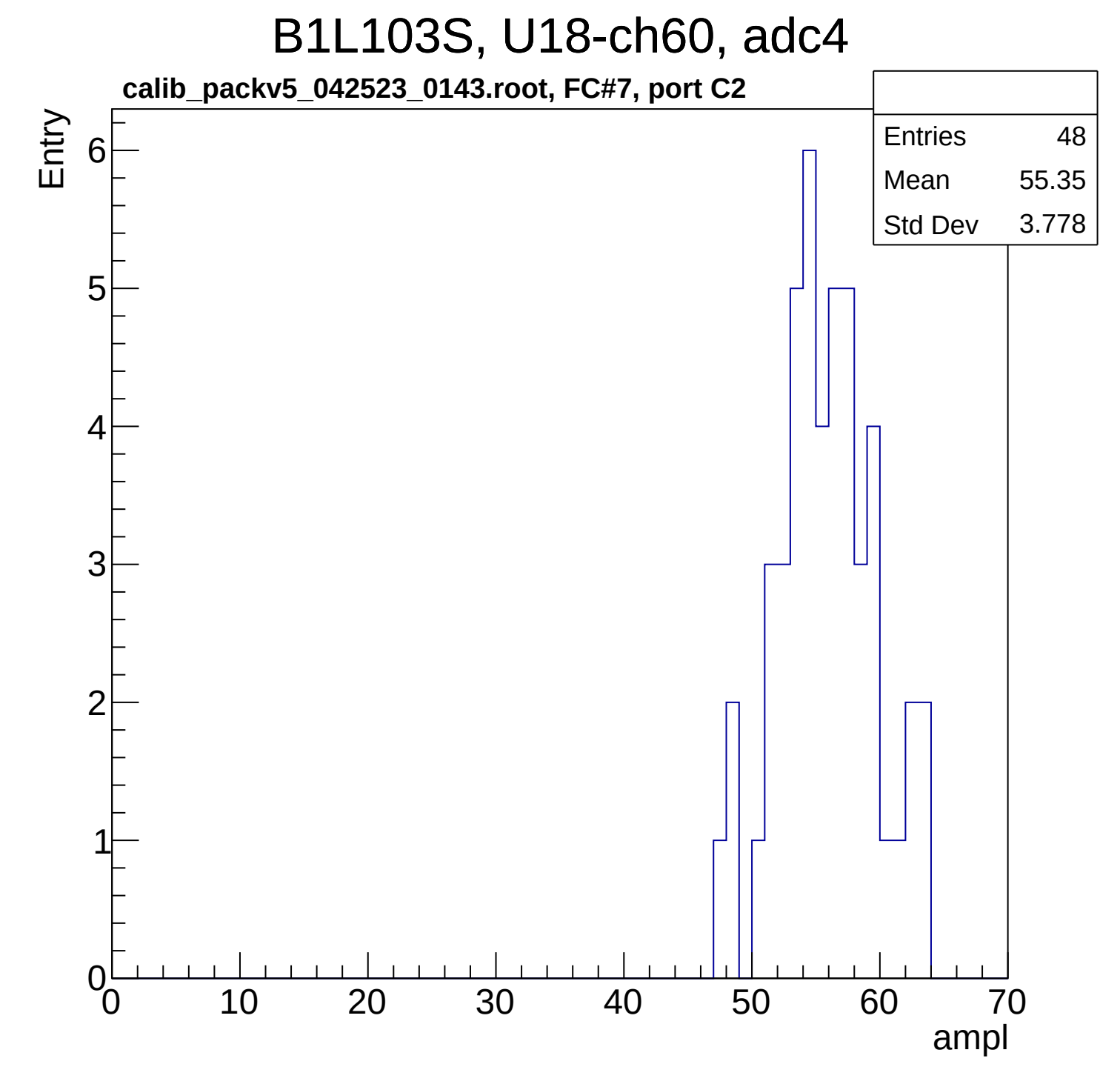
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch60, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 49.9
Std Dev 3.841
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch60, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 48
Mean 55.35
Std Dev 3.778
Entry
0
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2
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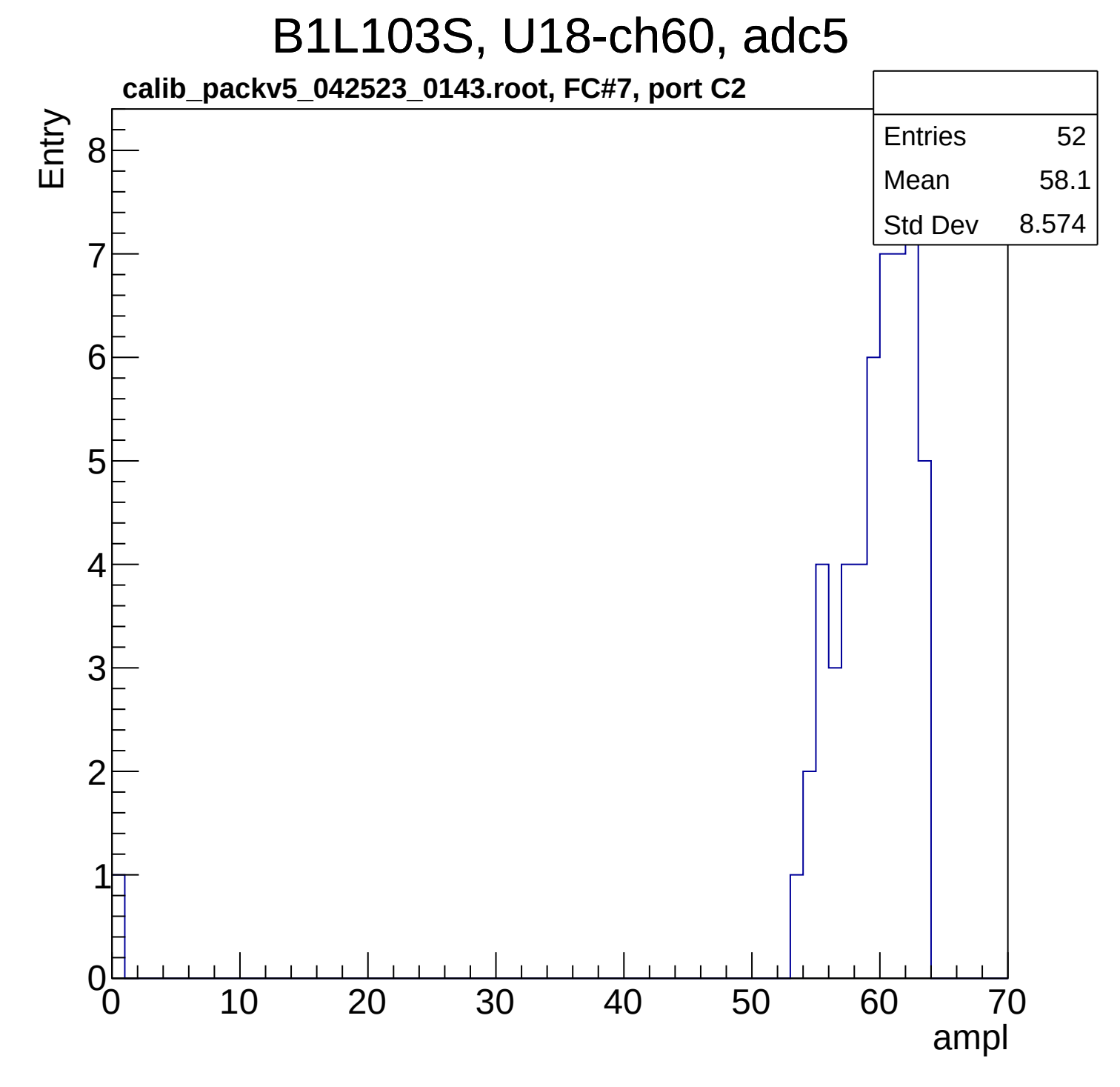
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch60, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 52
Mean 58.1
Std Dev 8.574
Entry
ampl
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1
2
3
4
5
6
7
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0
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60
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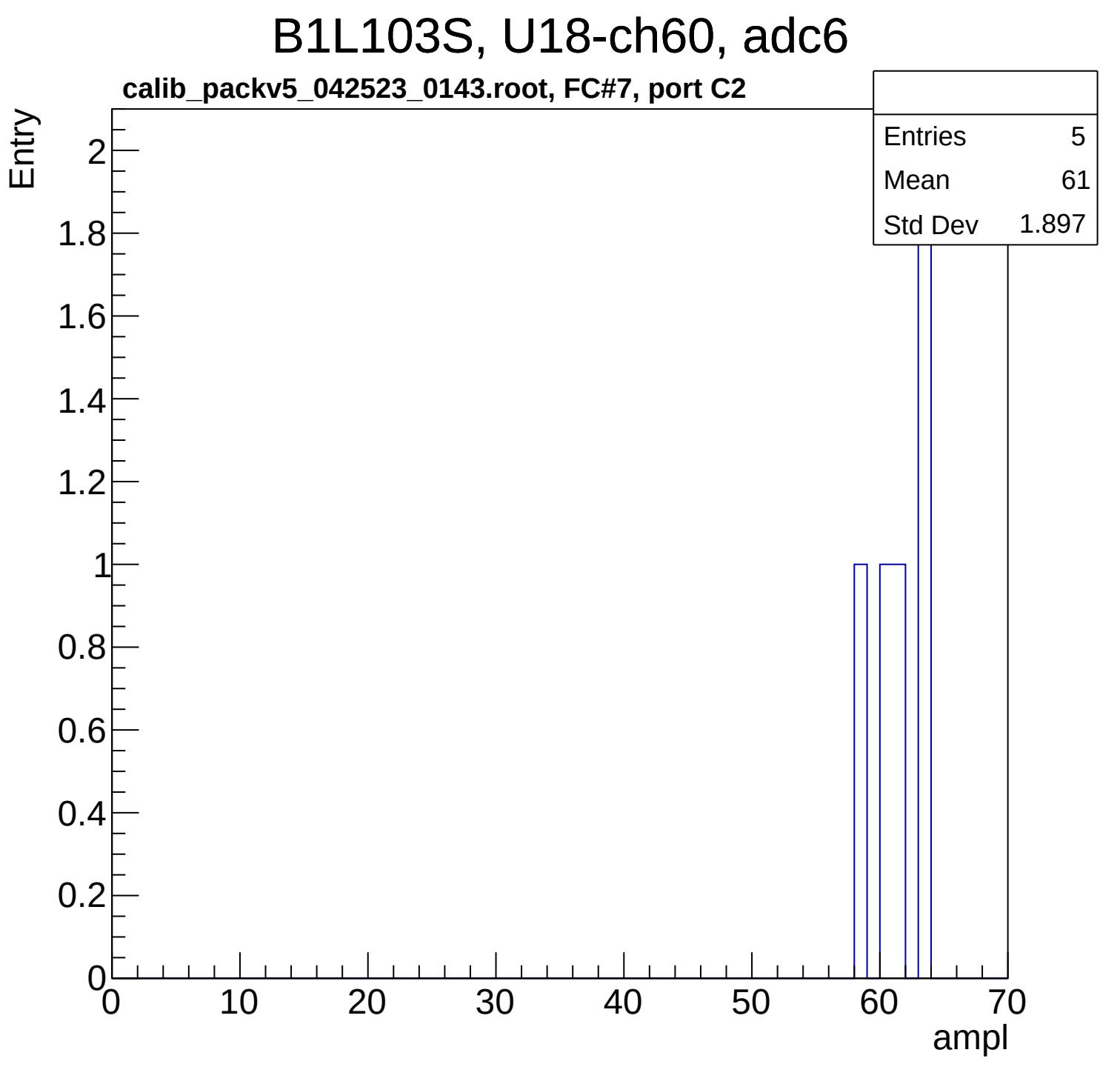
B1L103S, U18-ch60, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 5
Mean 61
Std Dev 1.897
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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20
30
40
50
60
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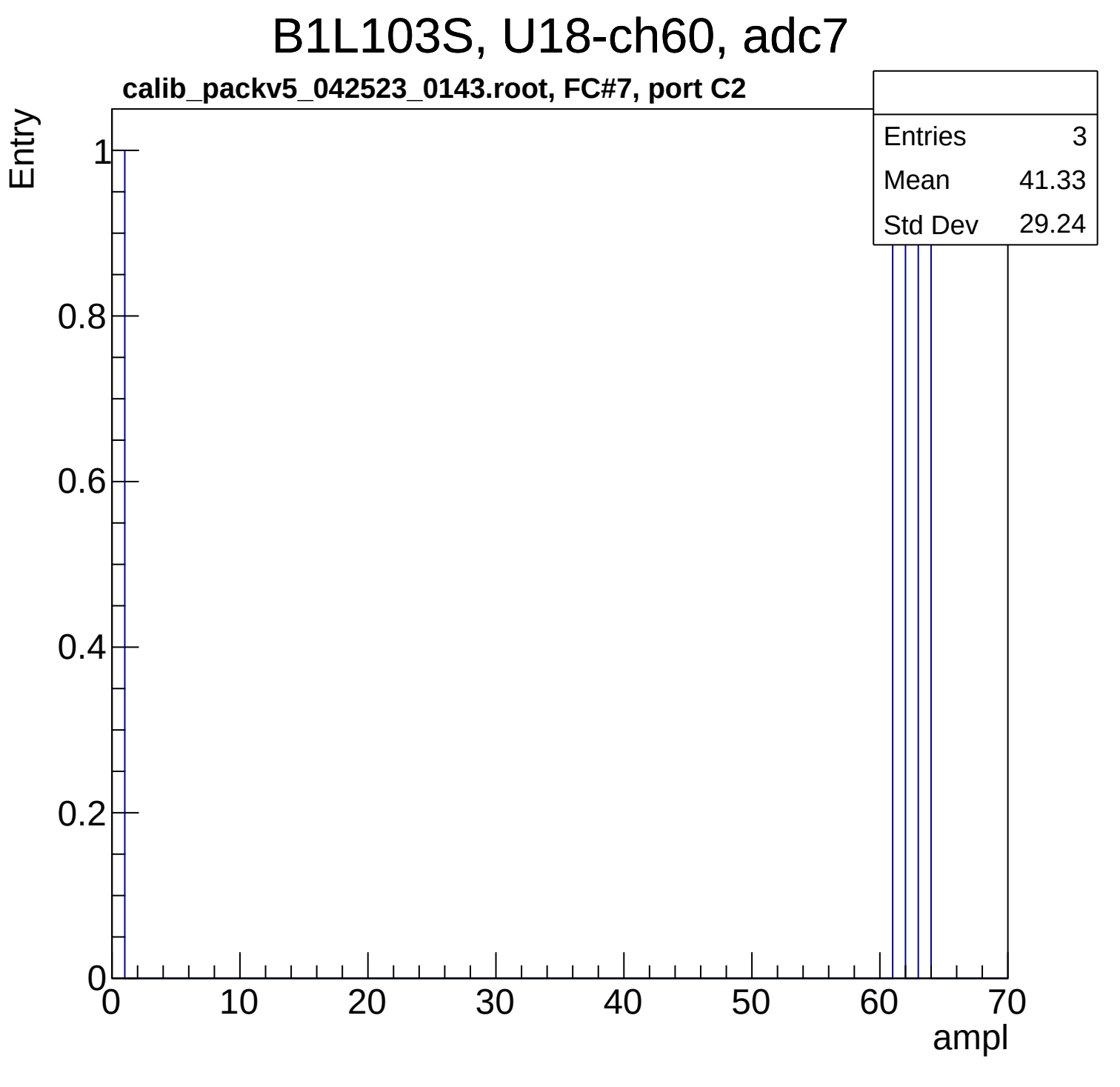
B1L103S, U18-ch60, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 41.33
Std Dev 29.24
Entry
ampl
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0.2
0.4
0.6
0.8
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0
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20
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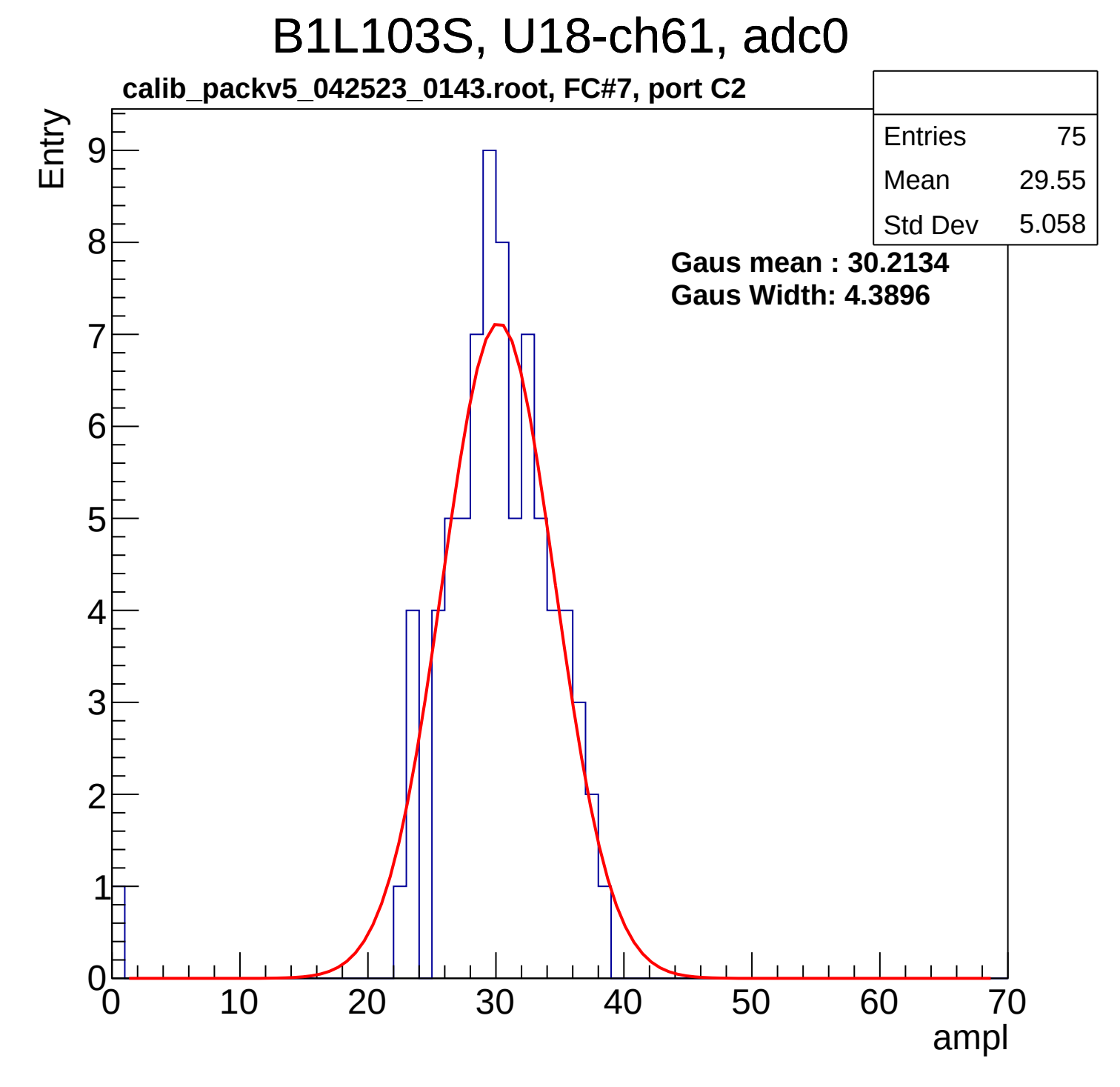
40
50
60
70


B1L103S, U18-ch61, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 75
Mean 29.55
Std Dev 5.058
Gaus mean : 30.2134
Gaus Width: 4.3896
Entry
ampl
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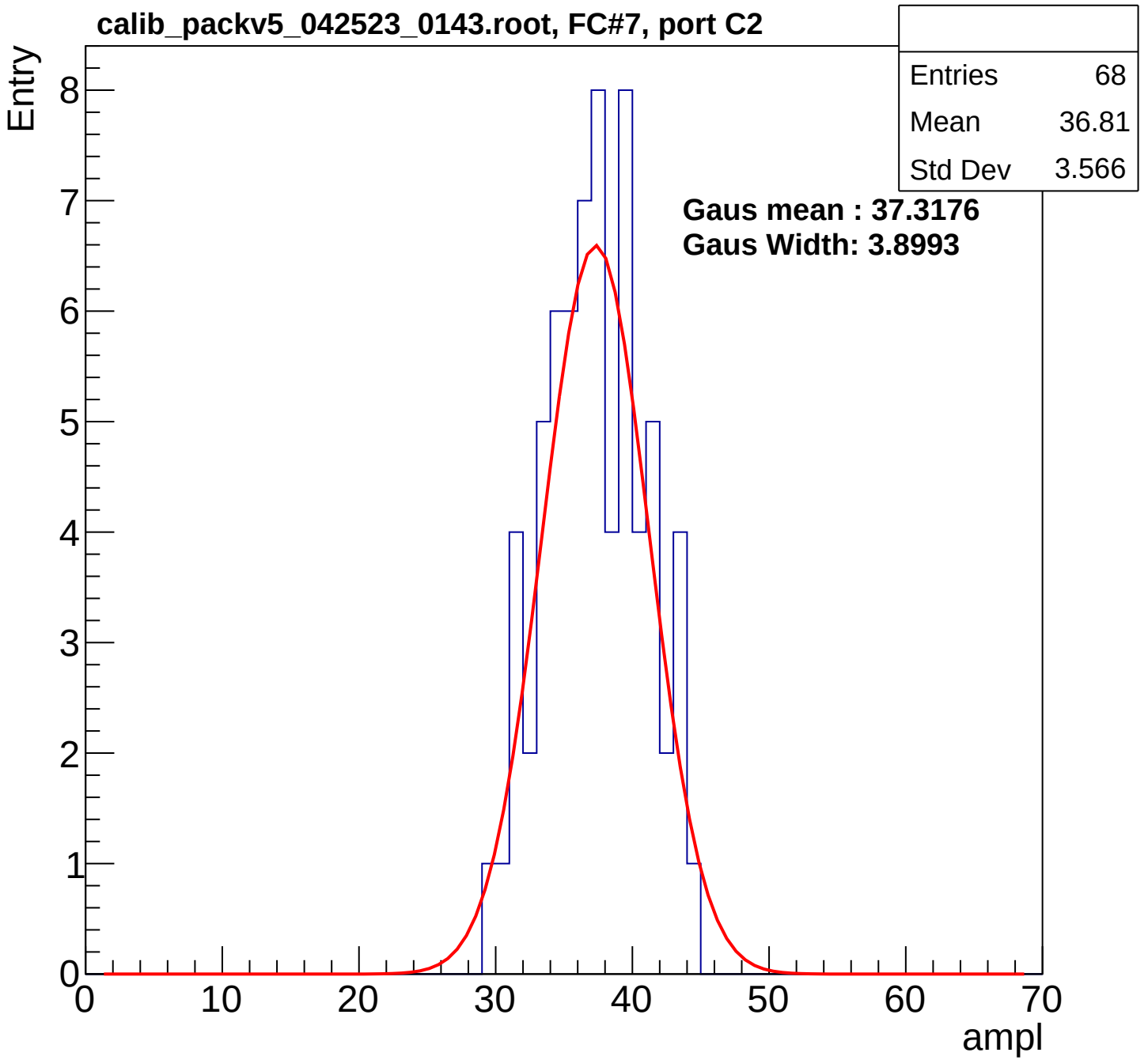
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch61, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 36.81
Std Dev 3.566
Gaus mean : 37.3176
Gaus Width: 3.8993
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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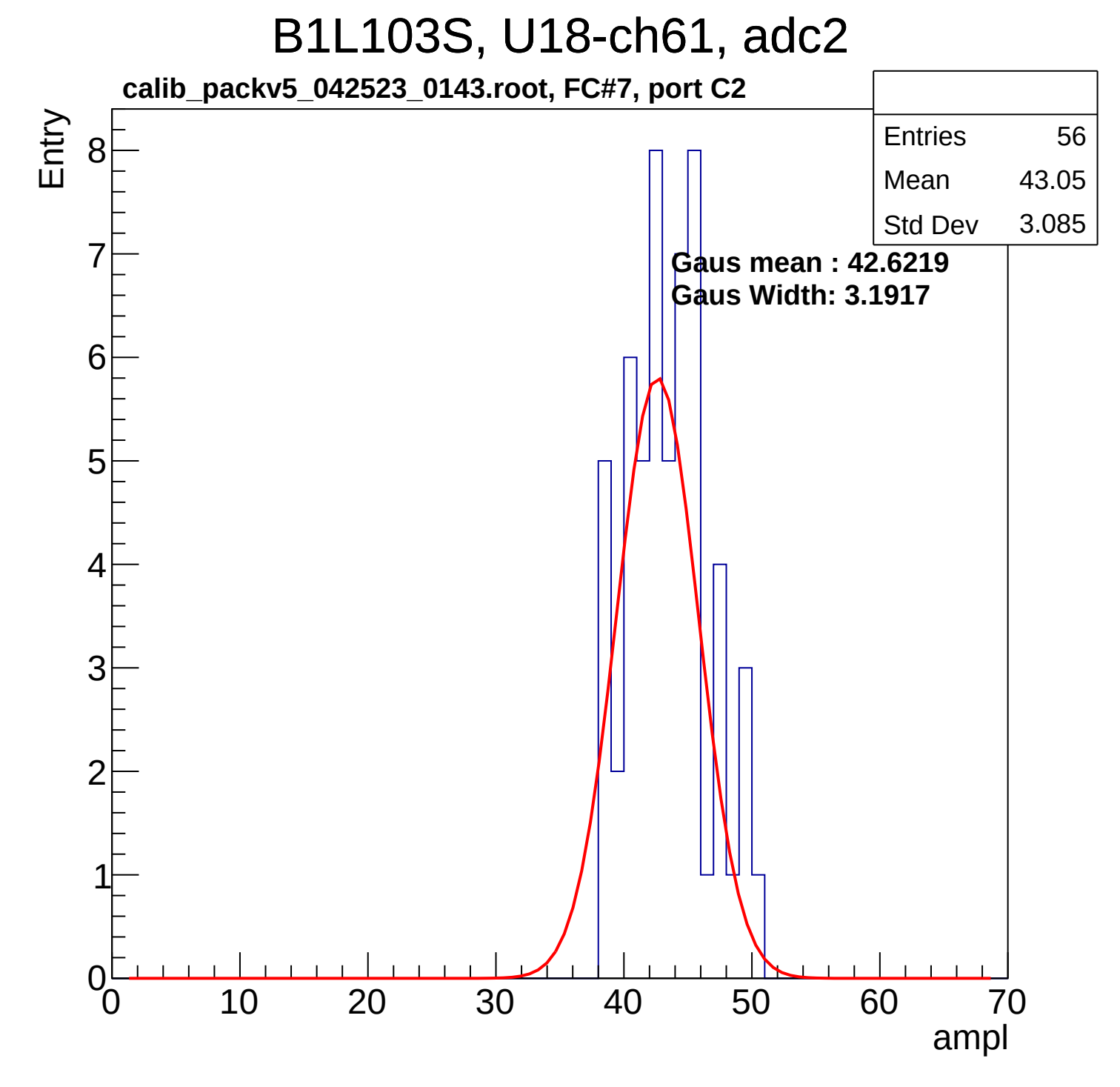
B1L103S, U18-ch61, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 43.05
Std Dev 3.085
Gaus mean : 42.6219
Gaus Width: 3.1917
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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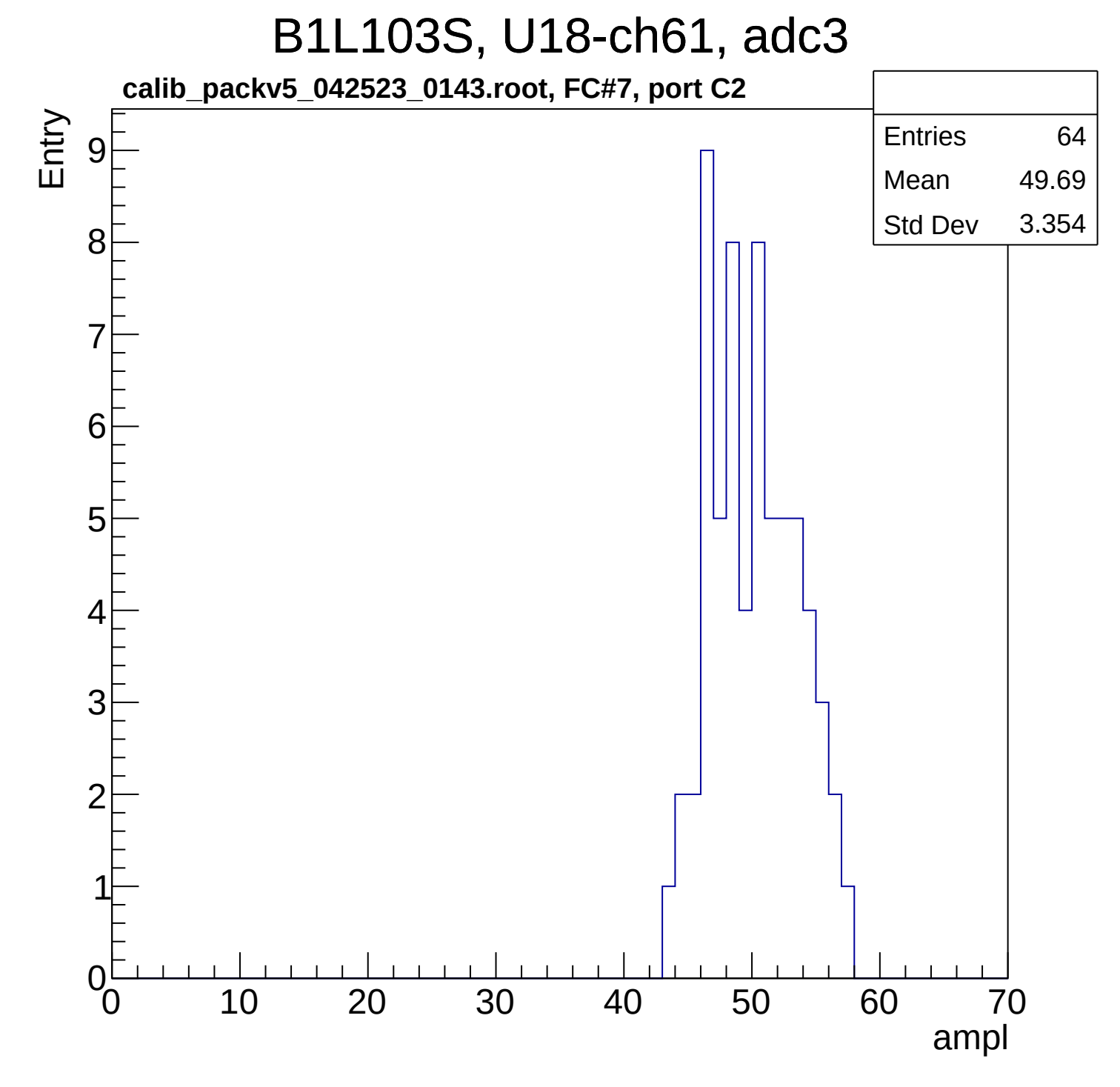
B1L103S, U18-ch61, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 49.69
Std Dev 3.354
Entry
ampl
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3
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6
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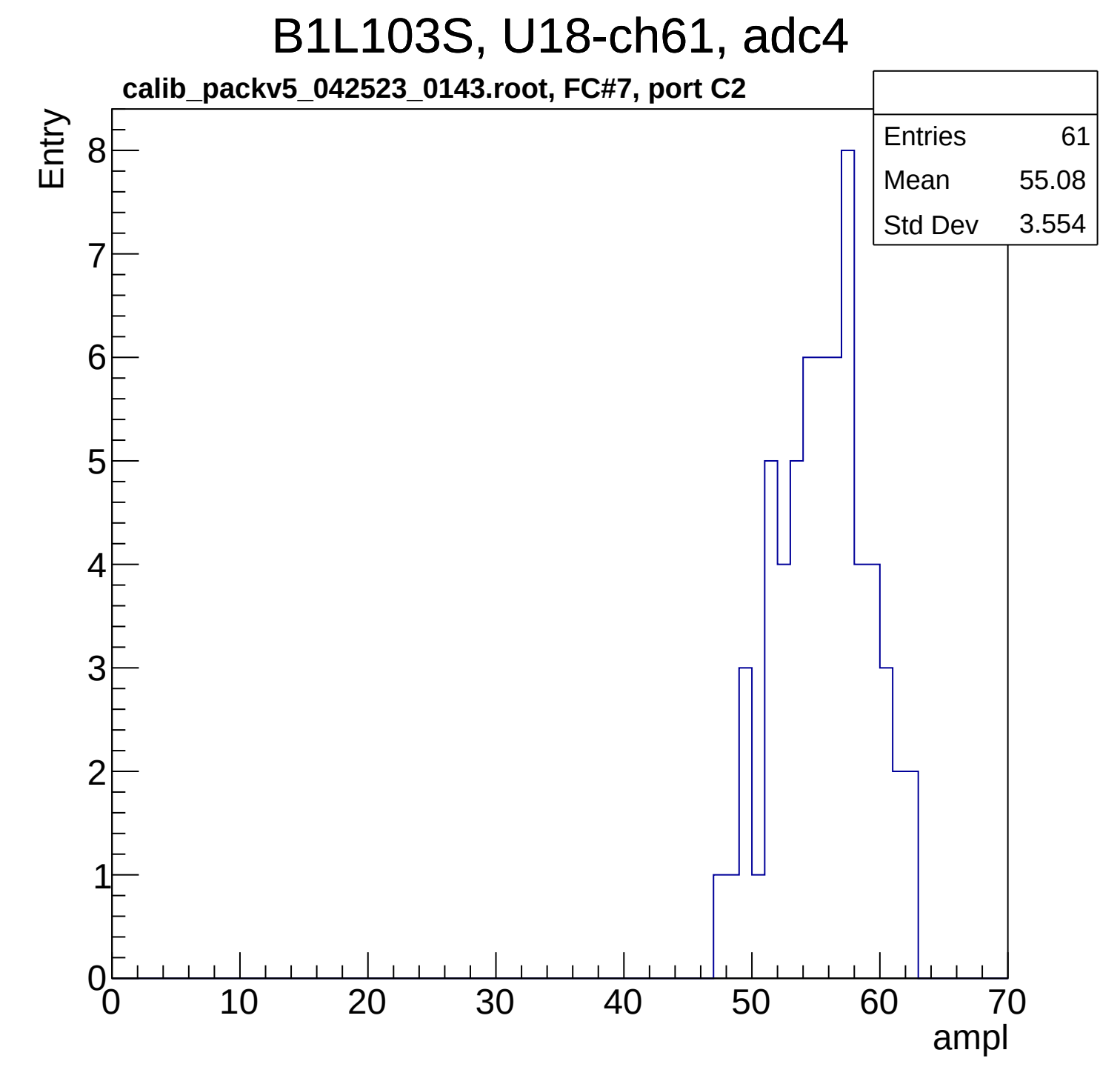
B1L103S, U18-ch61, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 61
Mean 55.08
Std Dev 3.554
Entry
ampl
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1
2
3
4
5
6
7
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0
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60
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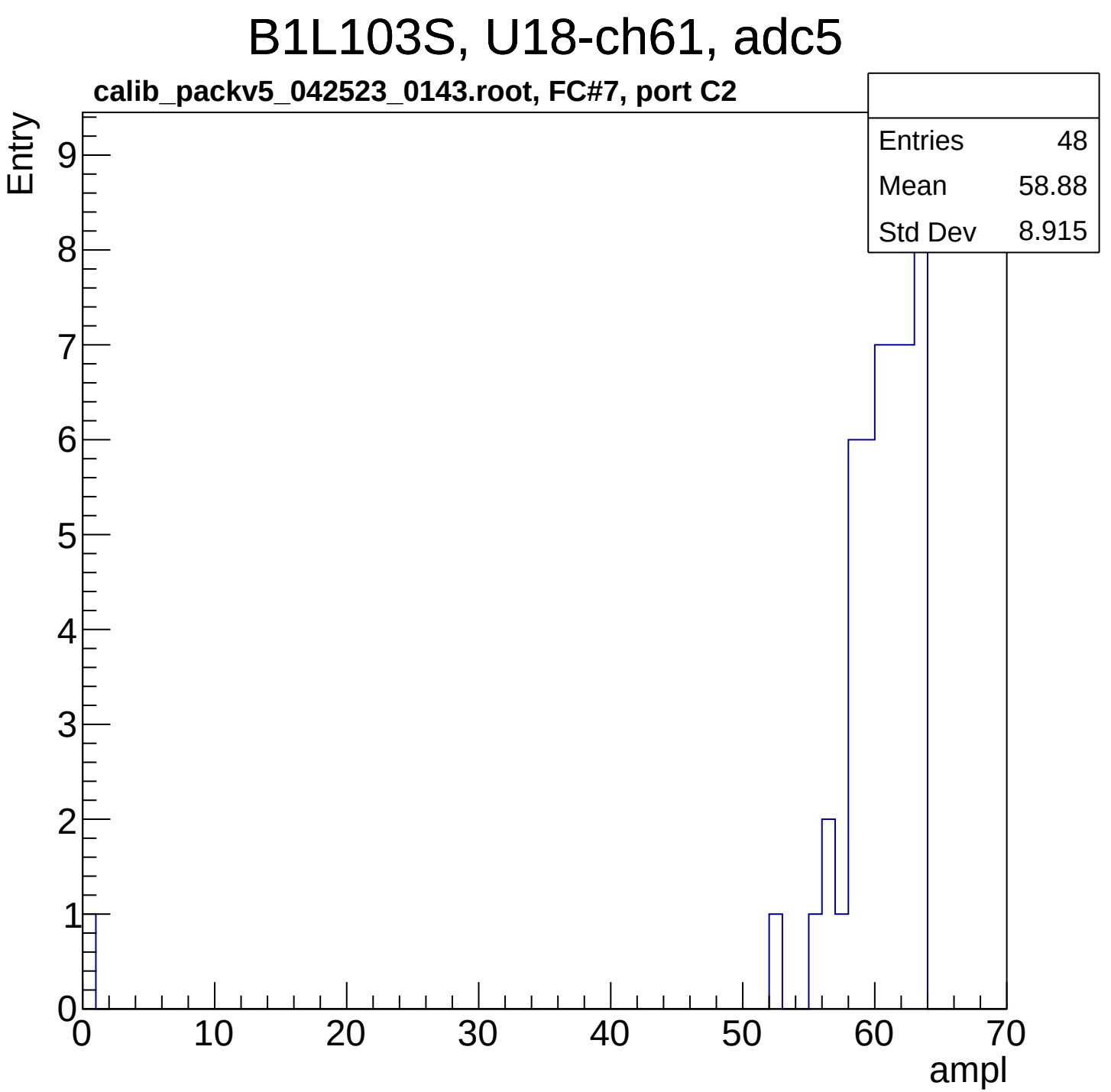
B1L103S, U18-ch61, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 48
Mean 58.88
Std Dev 8.915
Entry
ampl
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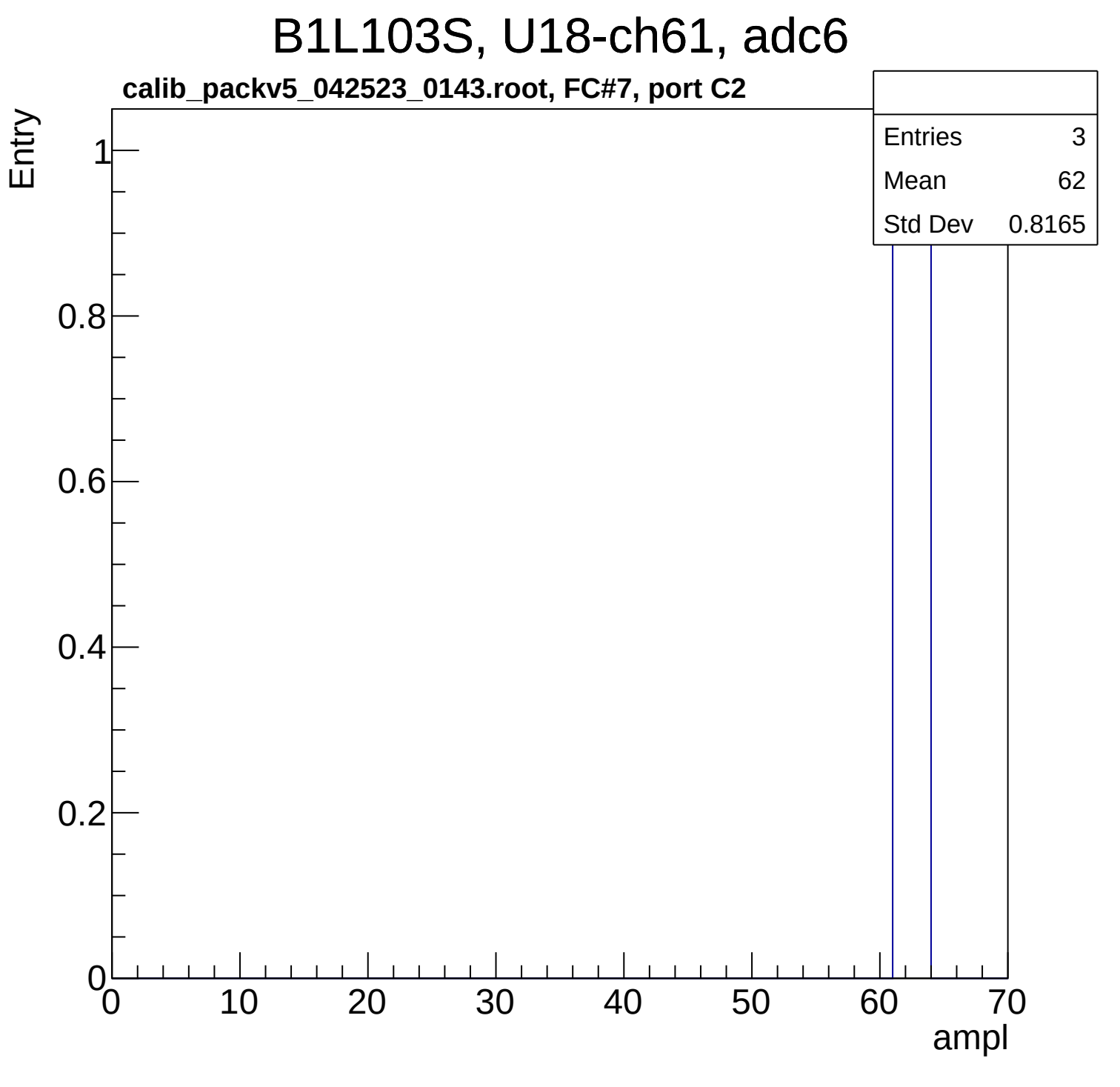
B1L103S, U18-ch61, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 62
Std Dev 0.8165
Entry
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0.8
0.6
0.4
0.2
0
0
10
20
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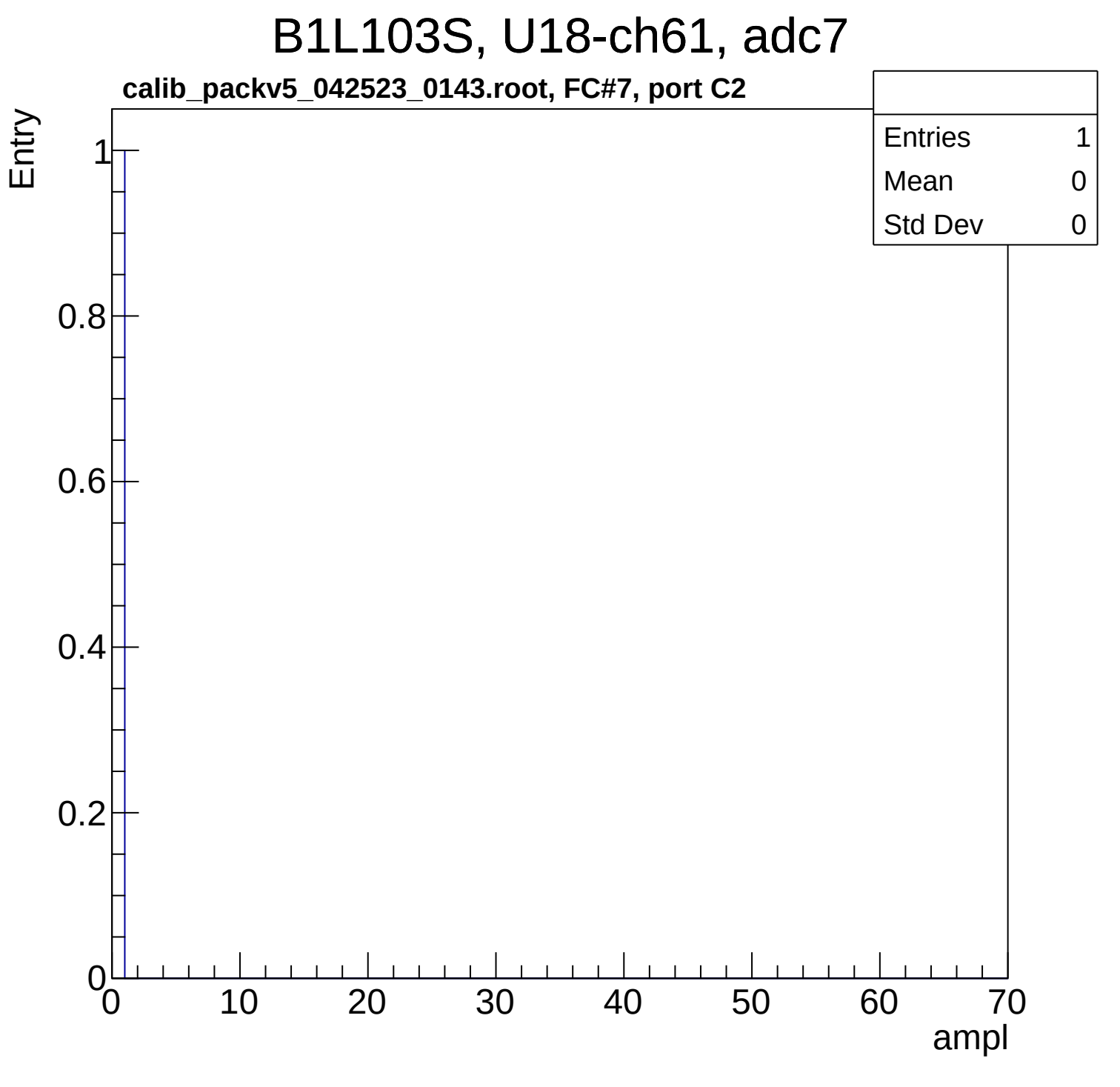
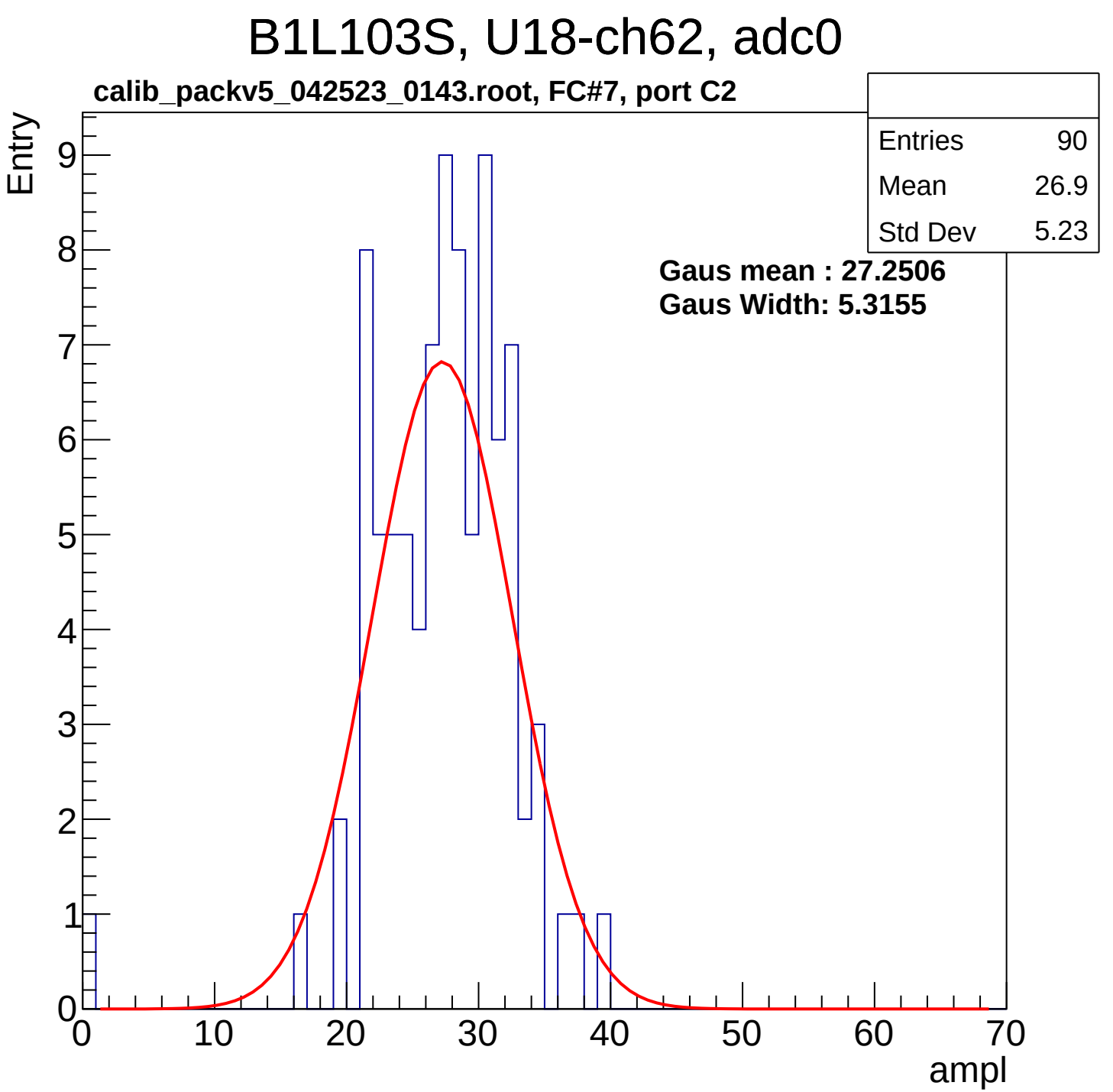
50
60
70
ampl


B1L103S, U18-ch61, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch62, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 90
Mean 26.9
Std Dev 5.23
Gaus mean : 27.2506
Gaus Width: 5.3155
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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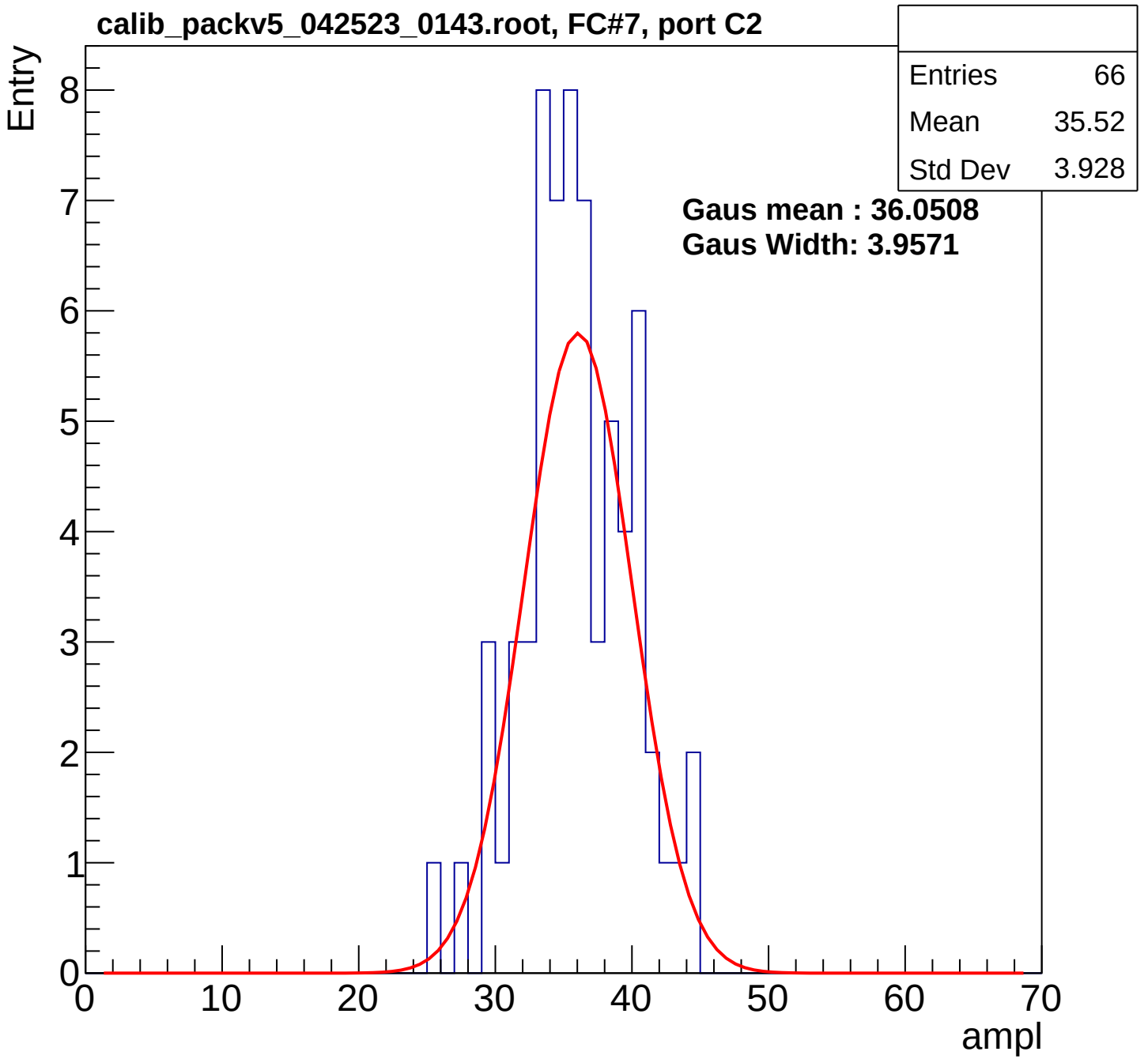
B1L103S, U18-ch62, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 35.52
Std Dev 3.928
Gaus mean : 36.0508
Gaus Width: 3.9571
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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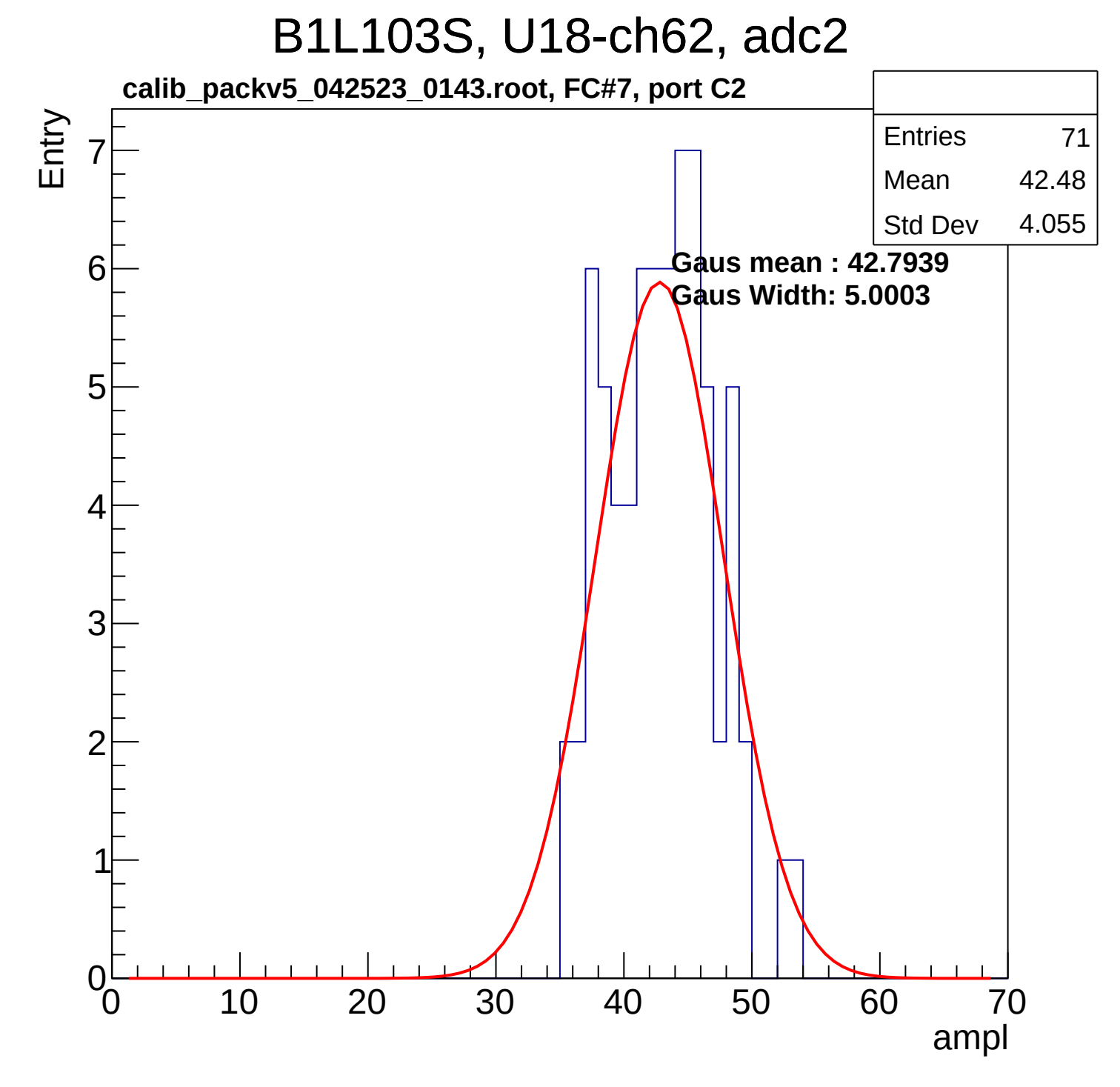
B1L103S, U18-ch62, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 71
Mean 42.48
Std Dev 4.055
Gaus mean : 42.7939
Gaus Width: 5.0003
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
50
60
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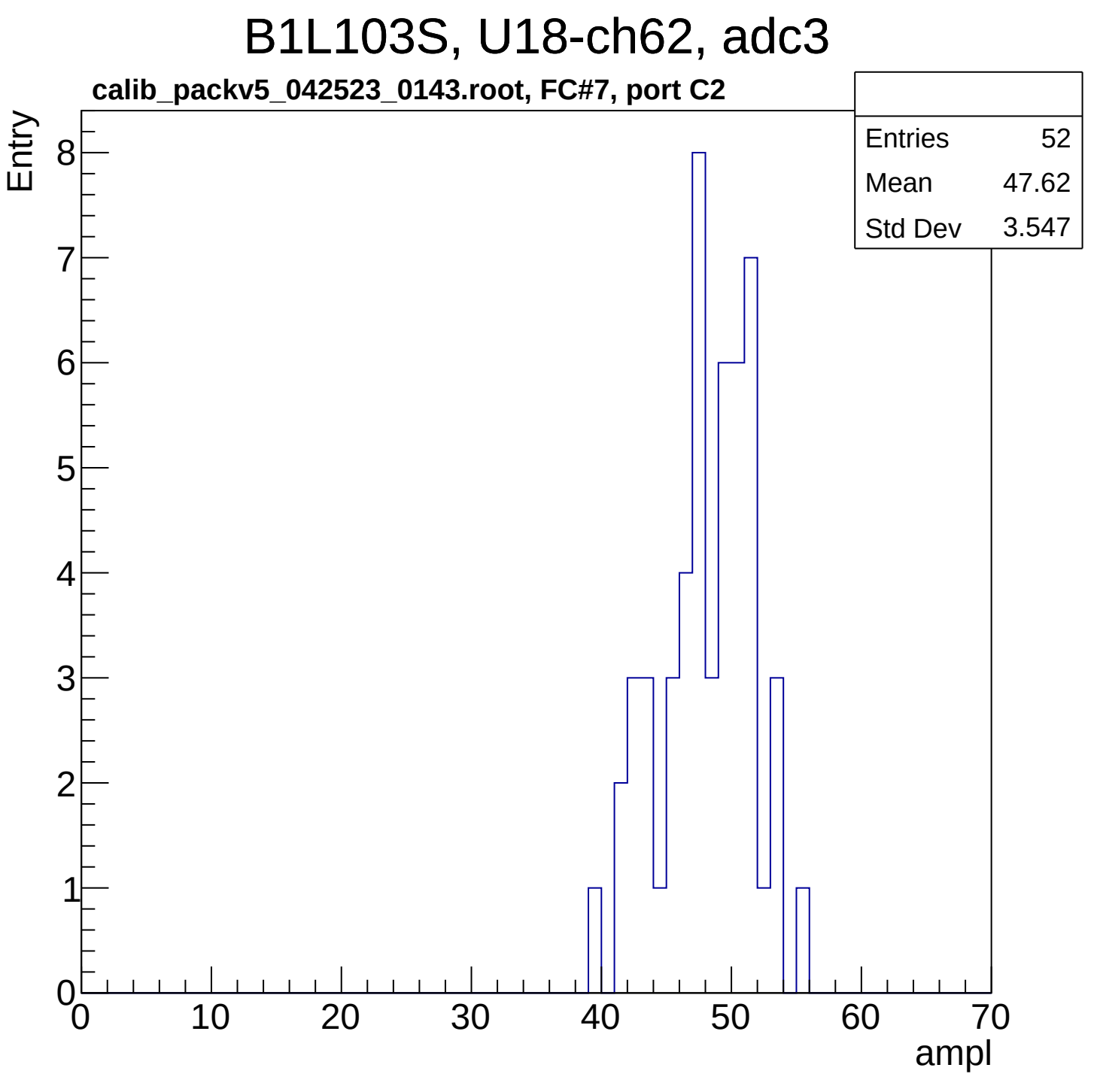
B1L103S, U18-ch62, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 52
Mean 47.62
Std Dev 3.547
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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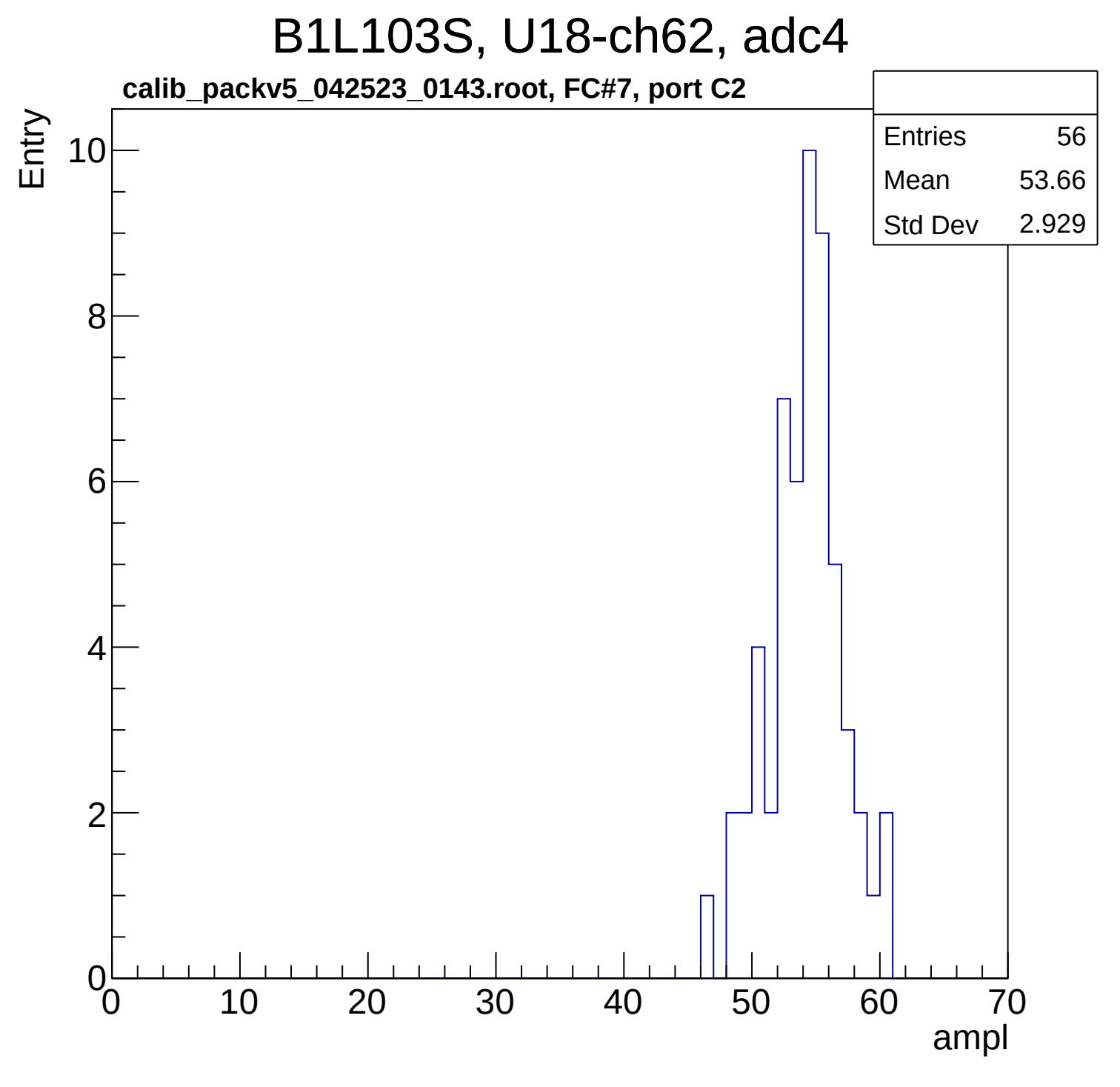
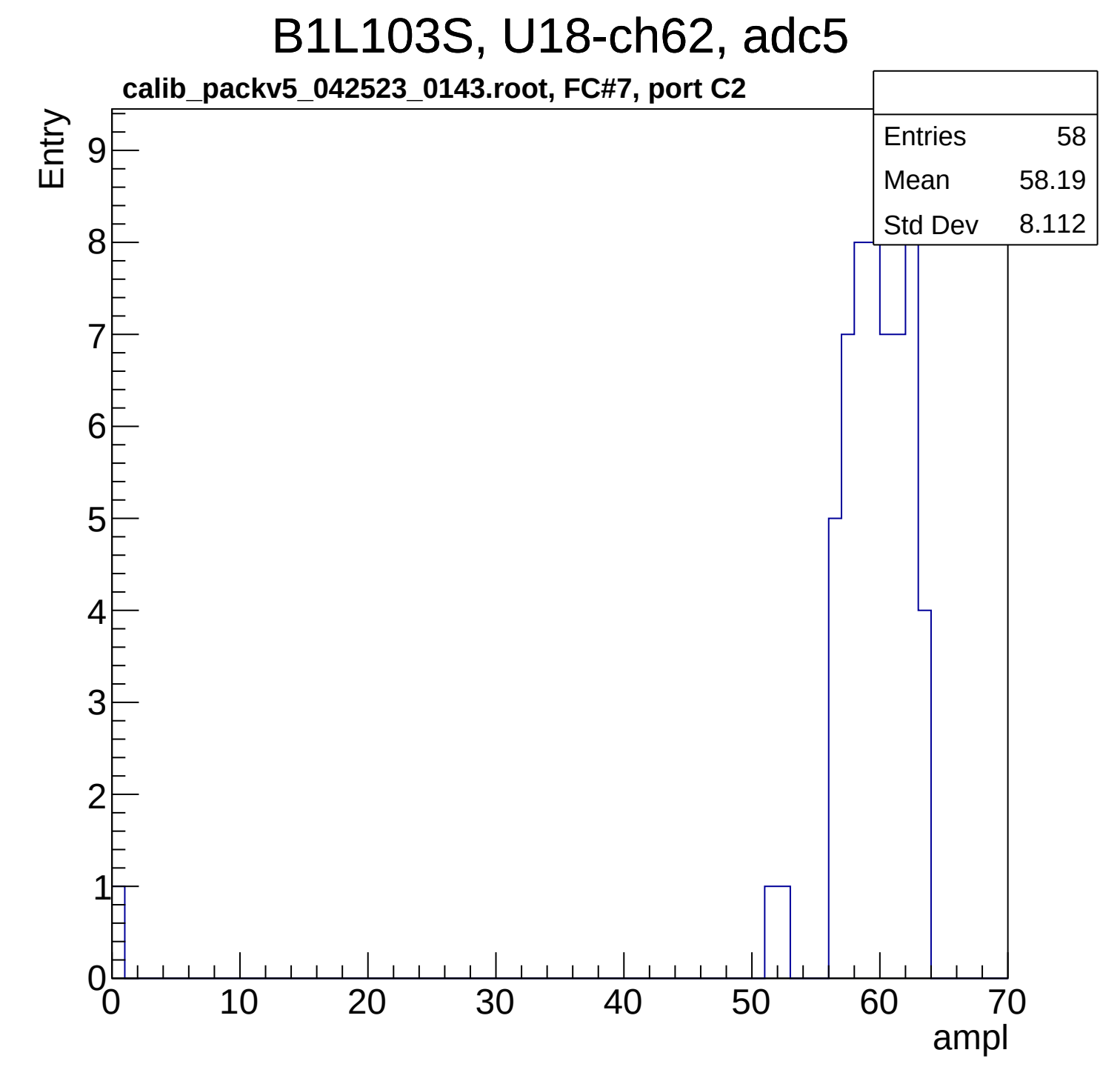

B1L103S, U18-ch62, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 53.66
Std Dev 2.929
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch62, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 58
Mean 58.19
Std Dev 8.112
Entry
ampl
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2
3
4
5
6
7
8
9
0
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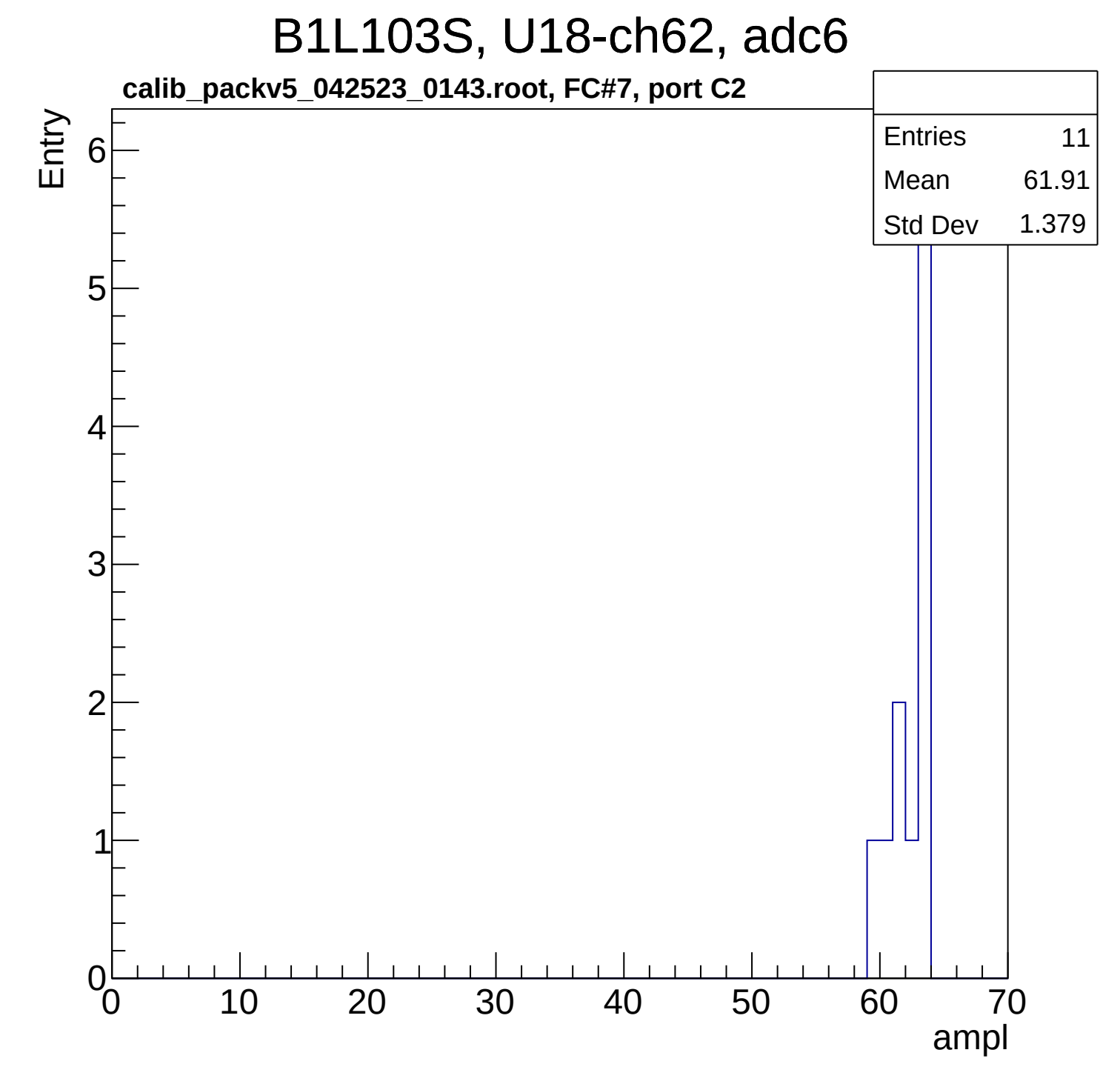
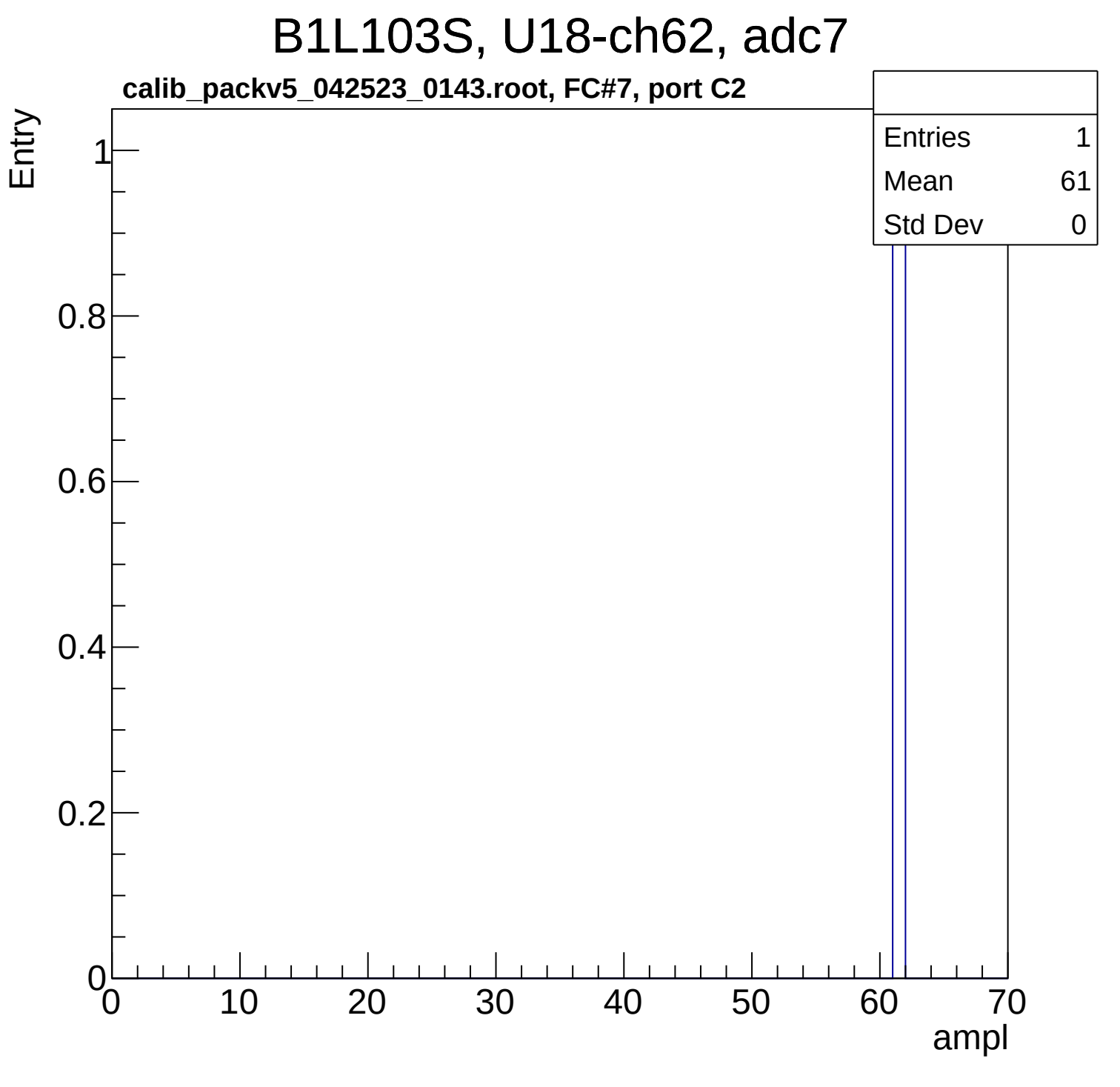
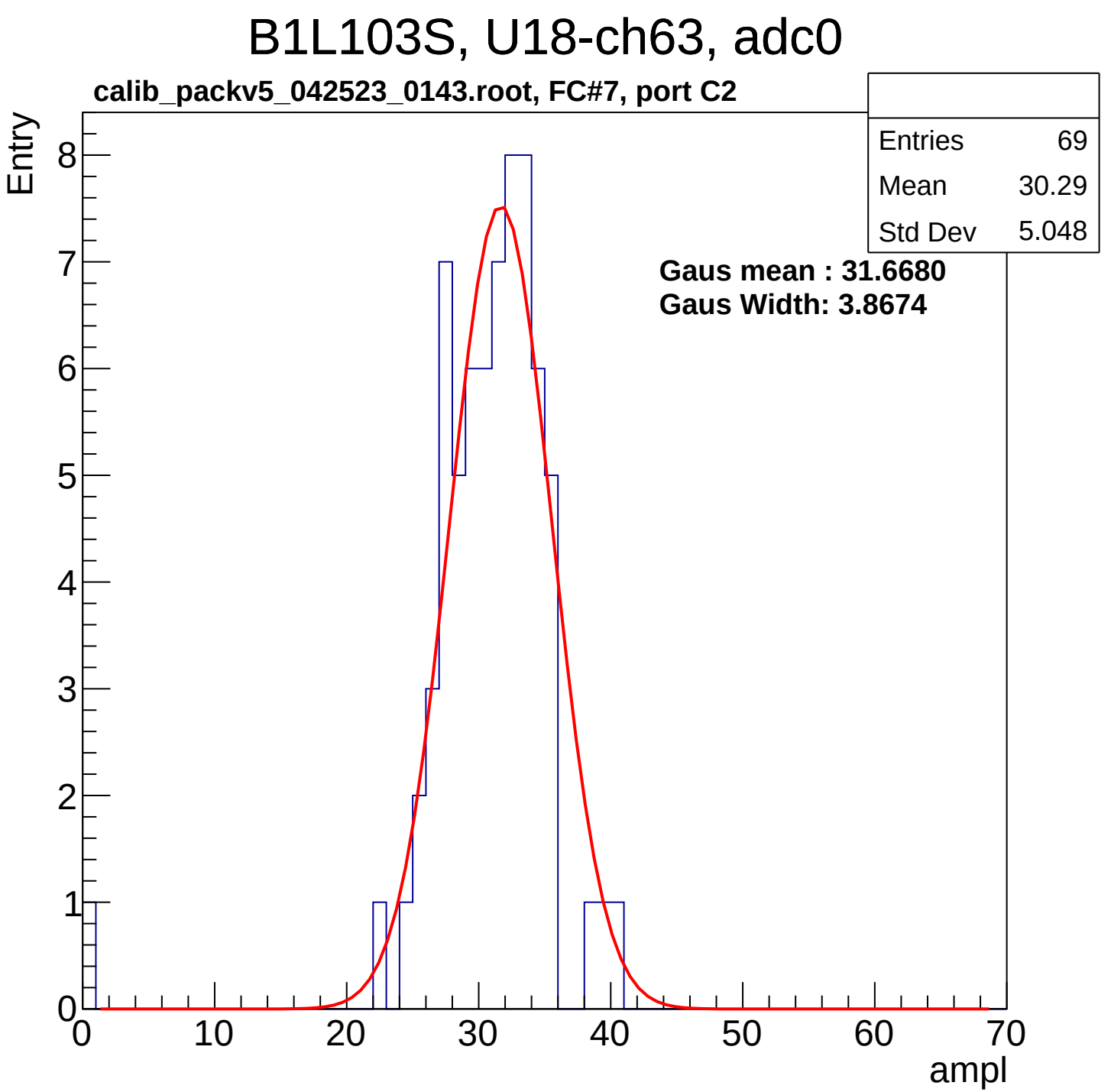

B1L103S, U18-ch62, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 11
Mean 61.91
Std Dev 1.379
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch62, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 61
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch63, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 30.29
Std Dev 5.048
Gaus mean : 31.6680
Gaus Width: 3.8674
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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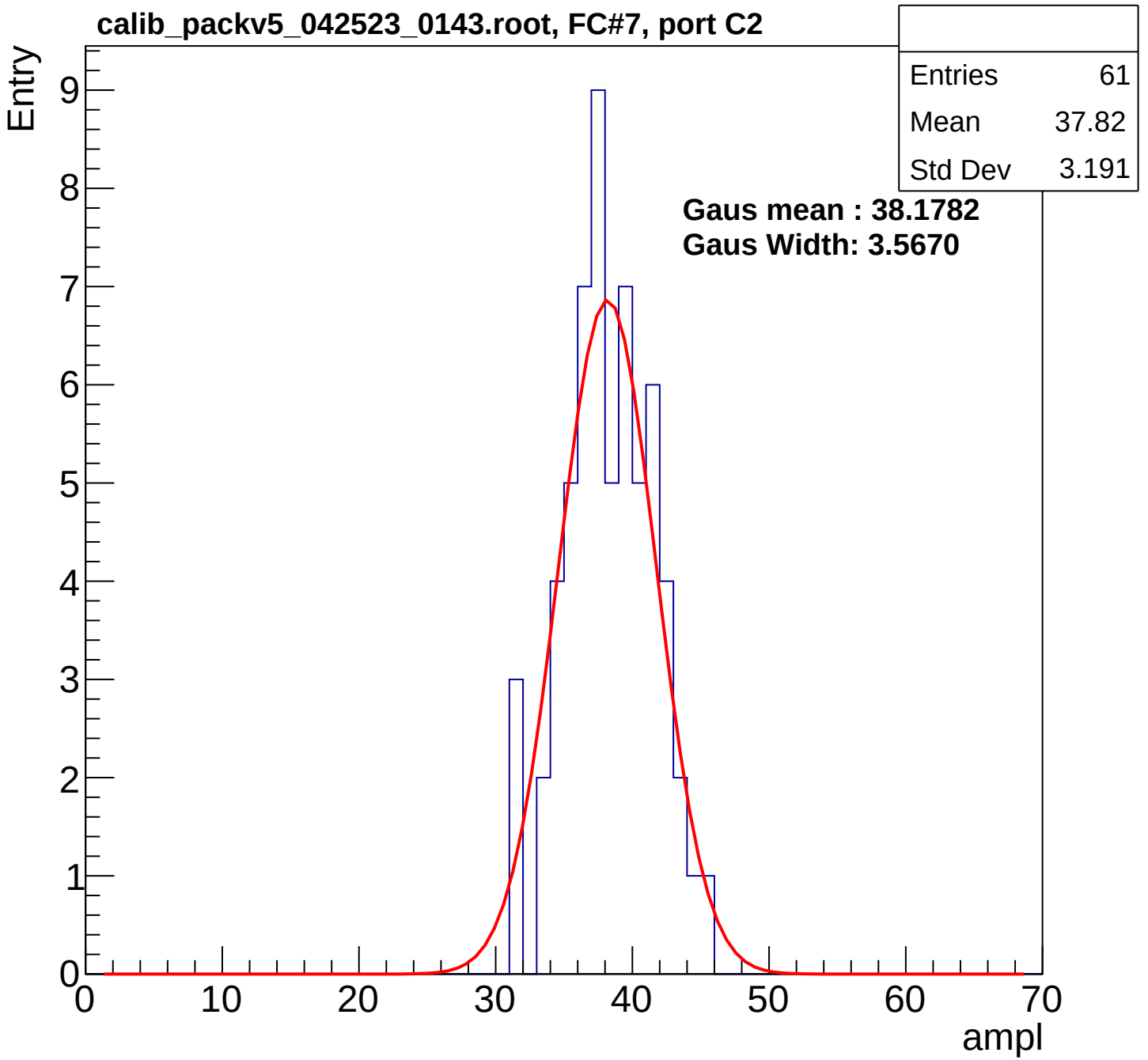
B1L103S, U18-ch63, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 61
Mean 37.82
Std Dev 3.191
Gaus mean : 38.1782
Gaus Width: 3.5670
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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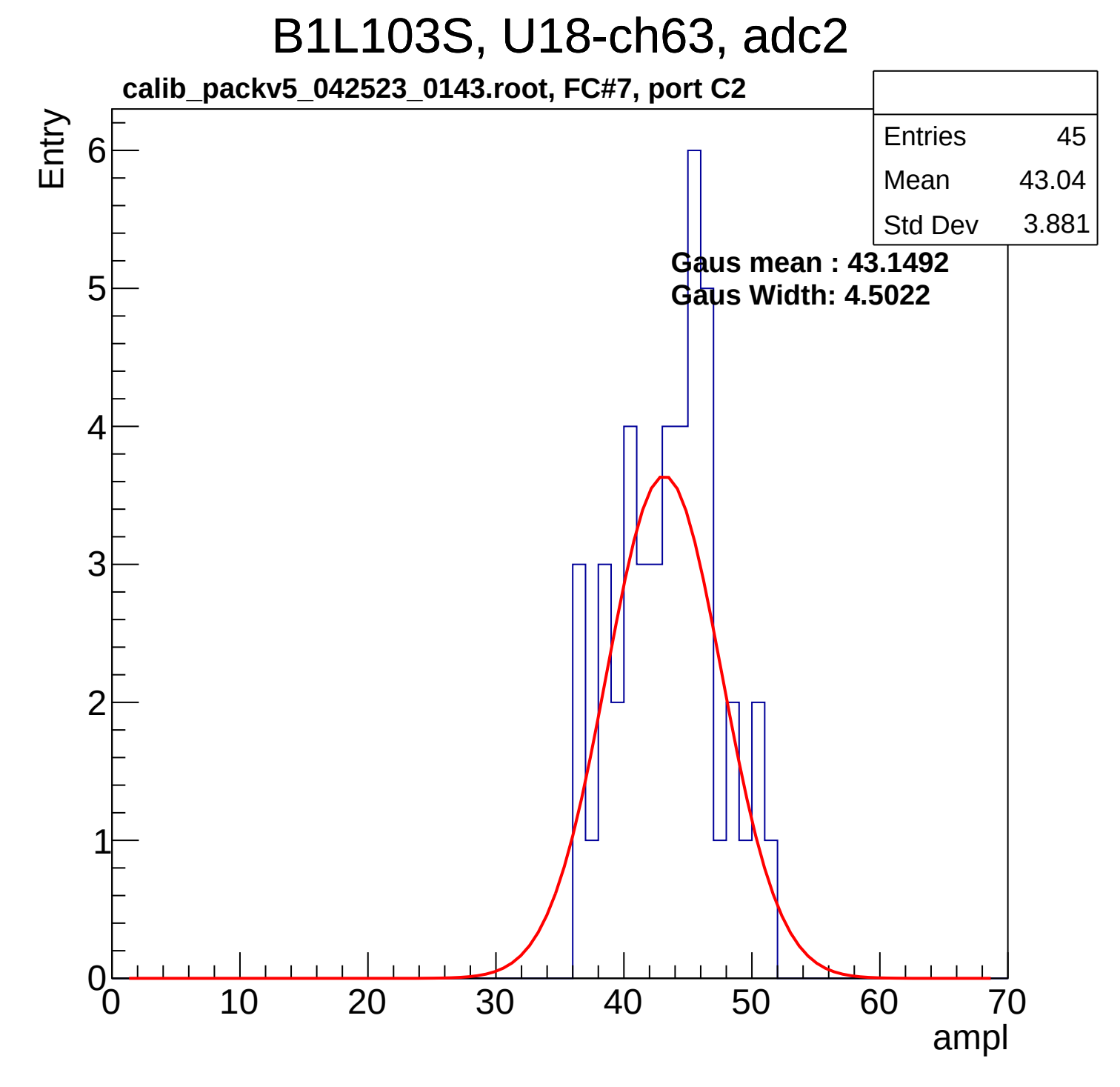
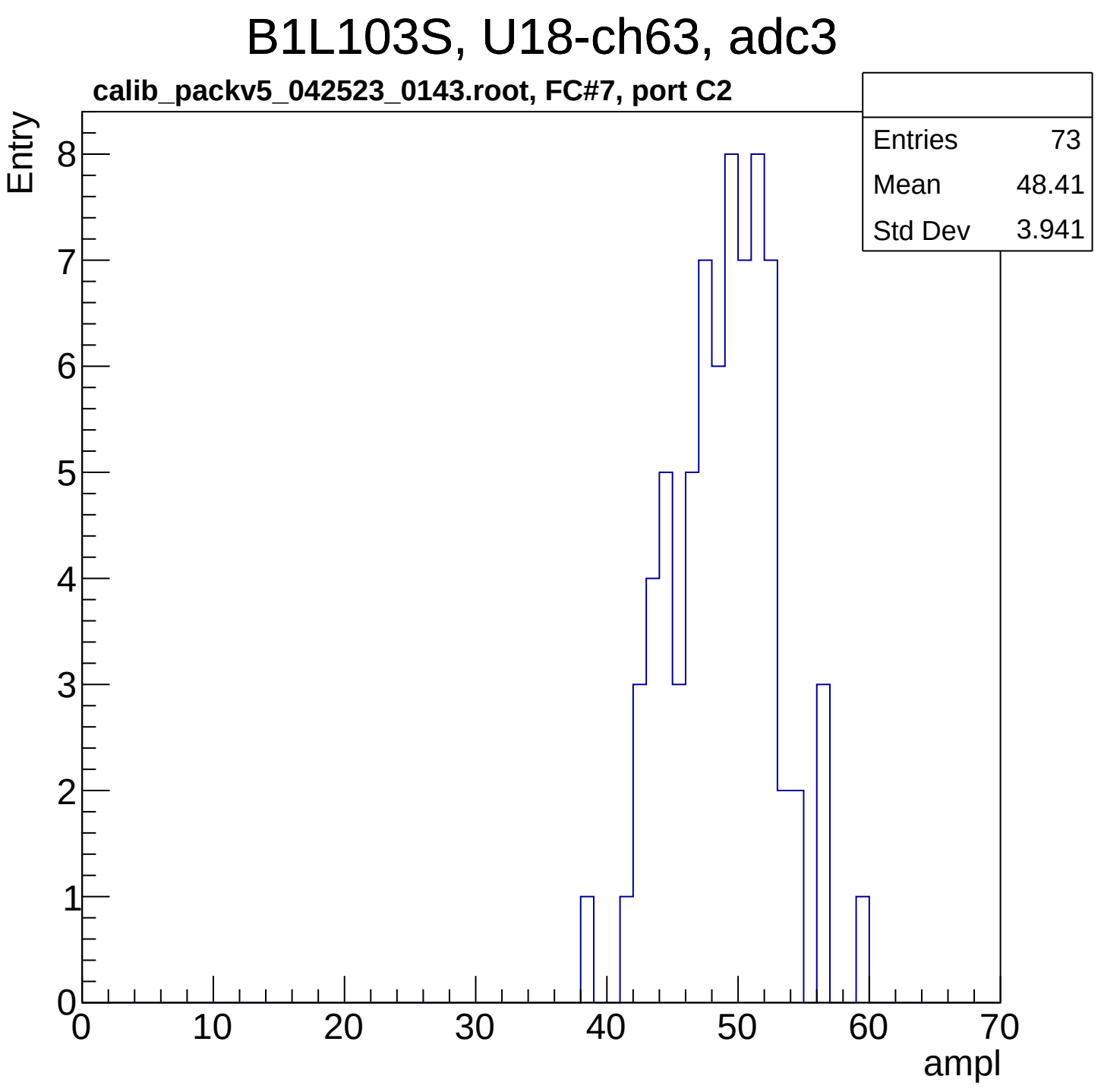

B1L103S, U18-ch63, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 45
Mean 43.04
Std Dev 3.881
Gaus mean : 43.1492
Gaus Width: 4.5022
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U18-ch63, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 73
Mean 48.41
Std Dev 3.941
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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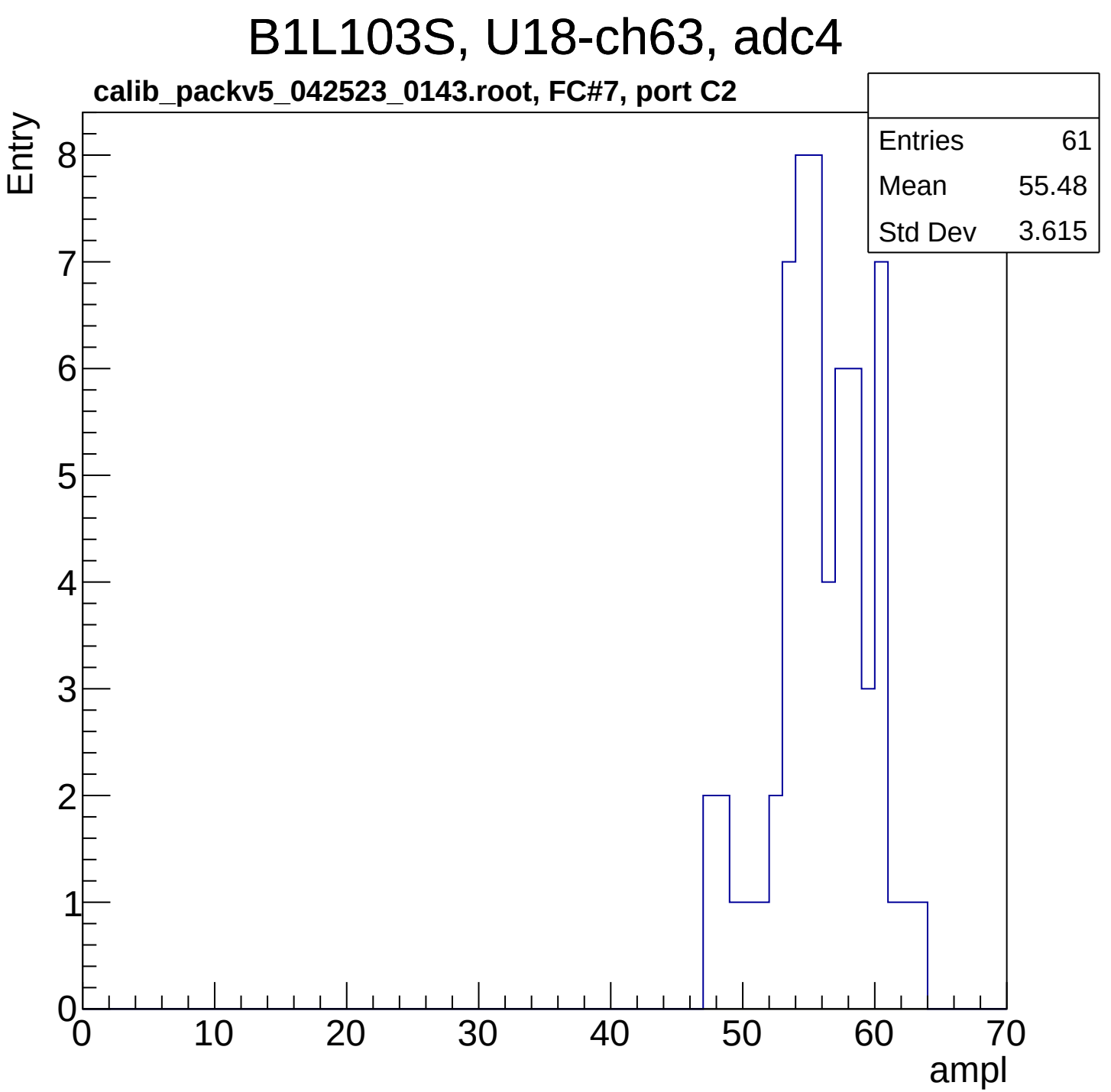
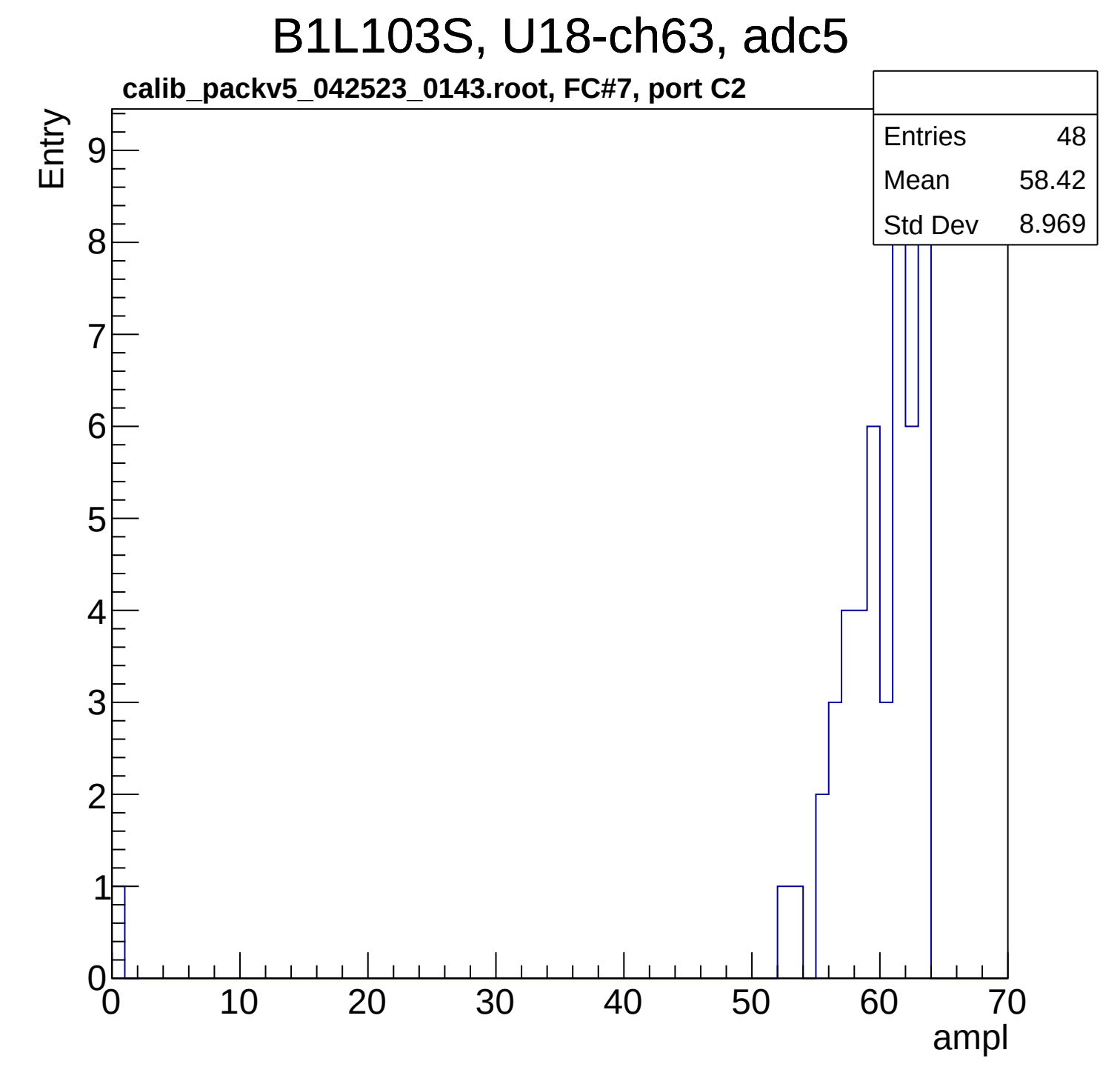

B1L103S, U18-ch63, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 61
Mean 55.48
Std Dev 3.615
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch63, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 48
Mean 58.42
Std Dev 8.969
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
30
40
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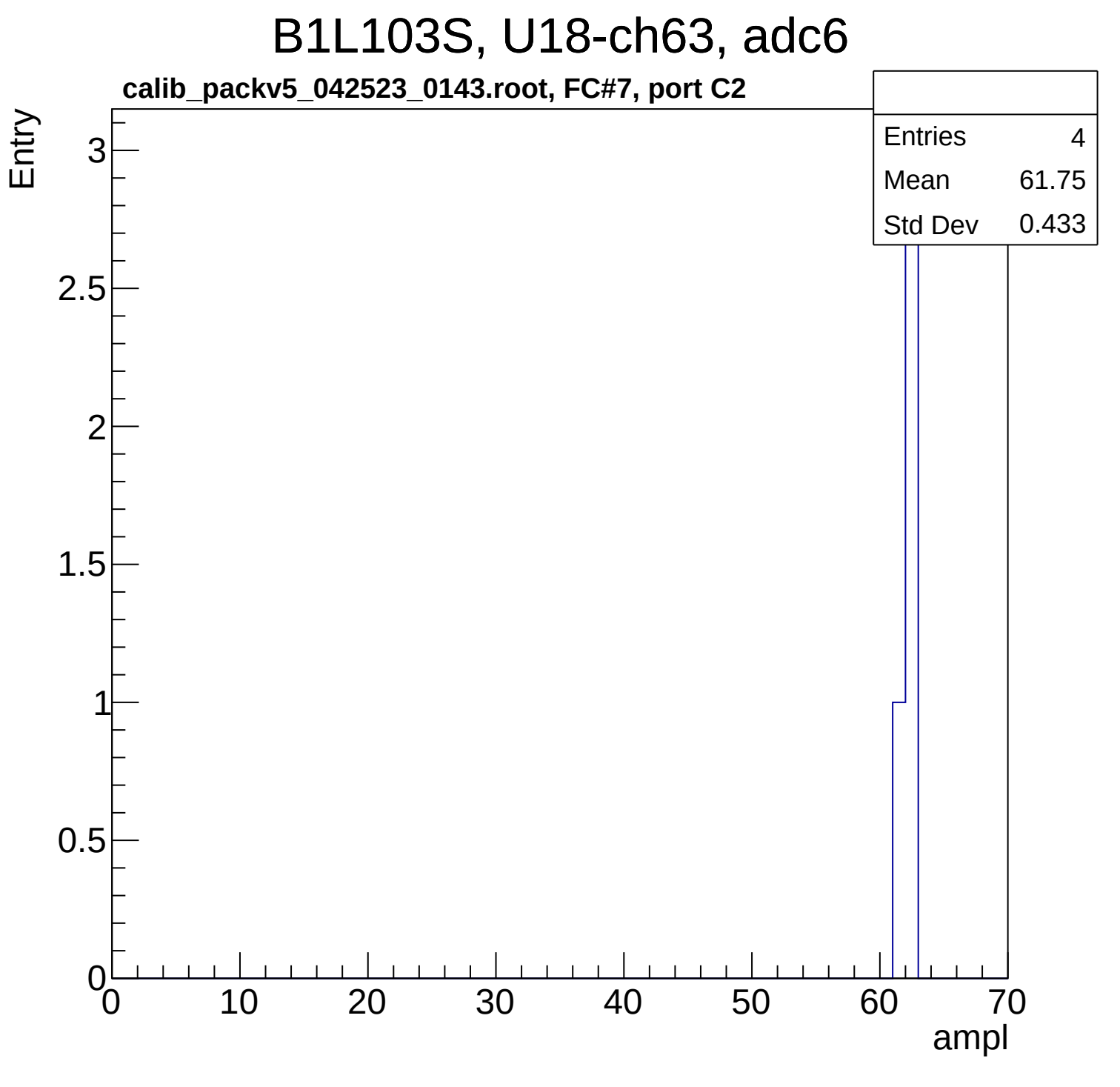
60
70


B1L103S, U18-ch63, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 4
Mean 61.75
Std Dev 0.433
Entry
ampl
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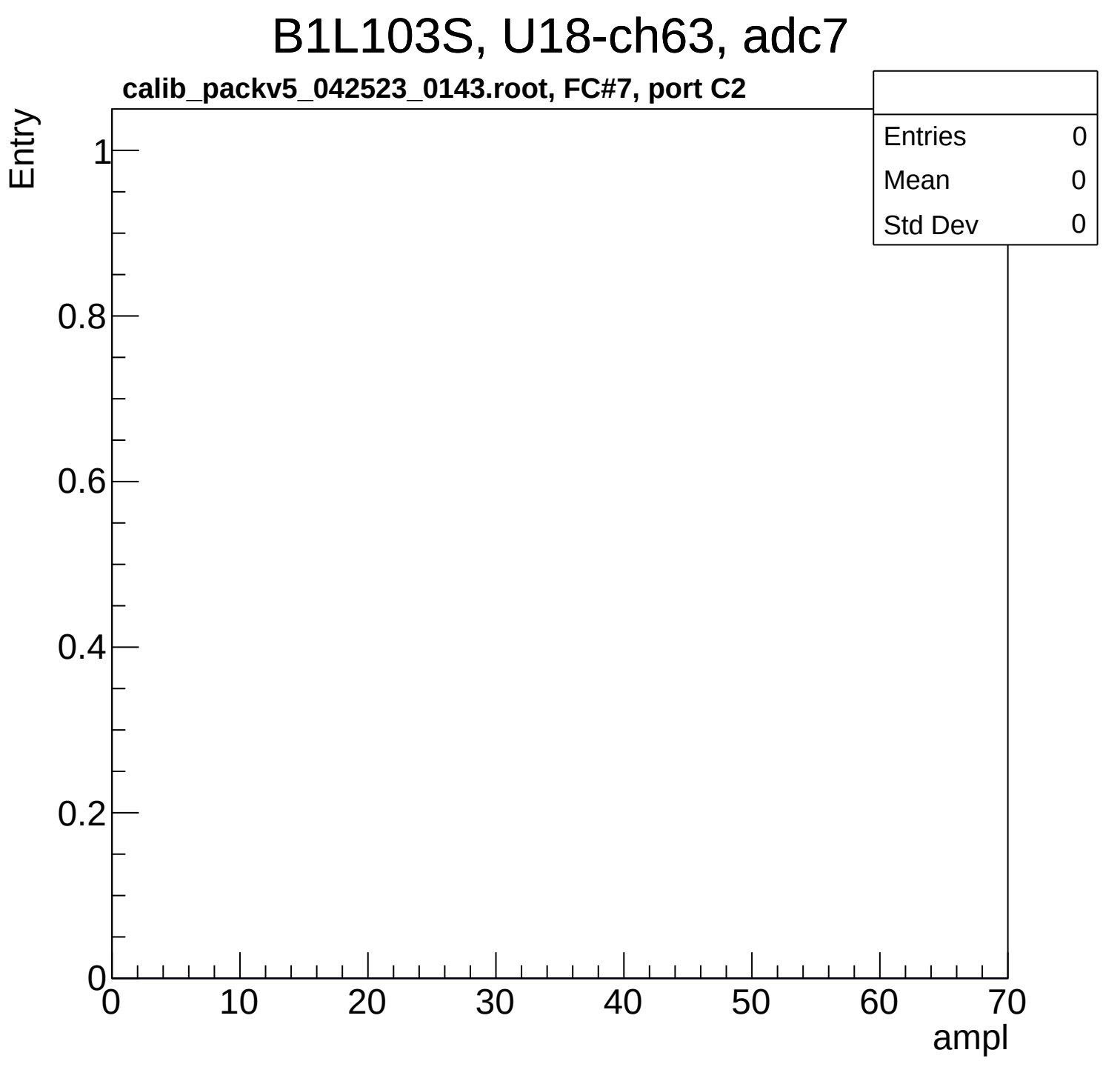
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U18-ch63, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
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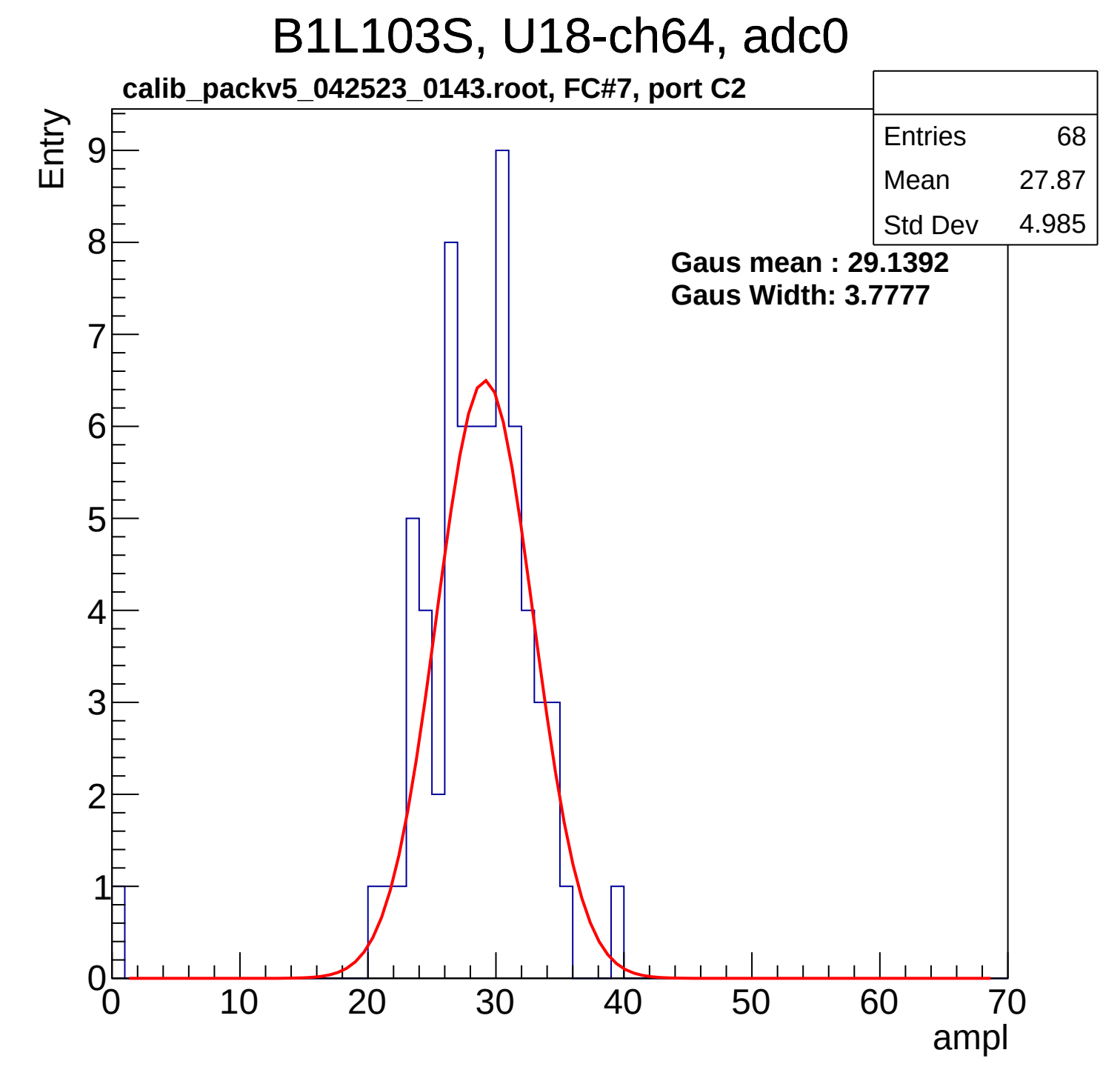
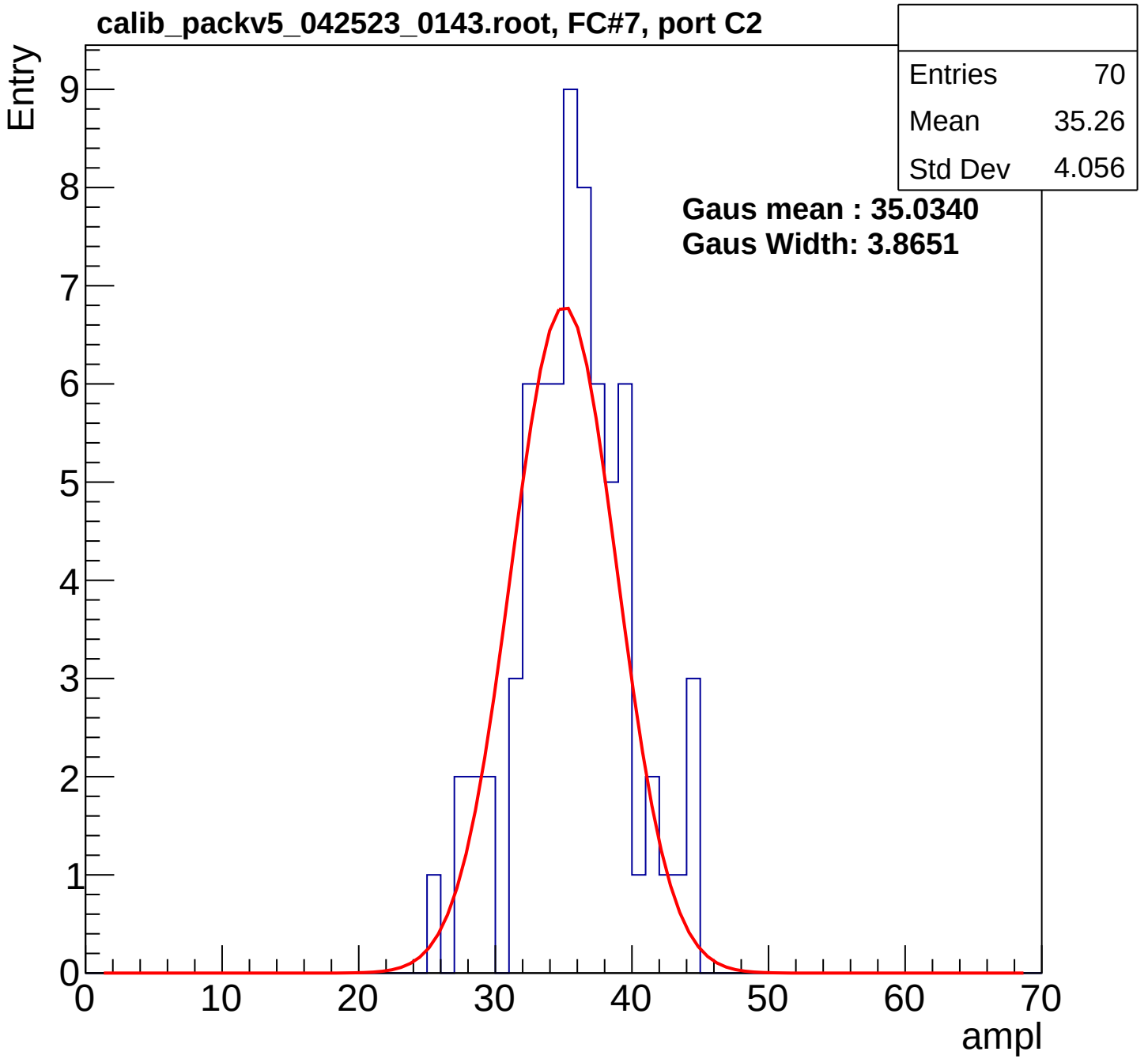
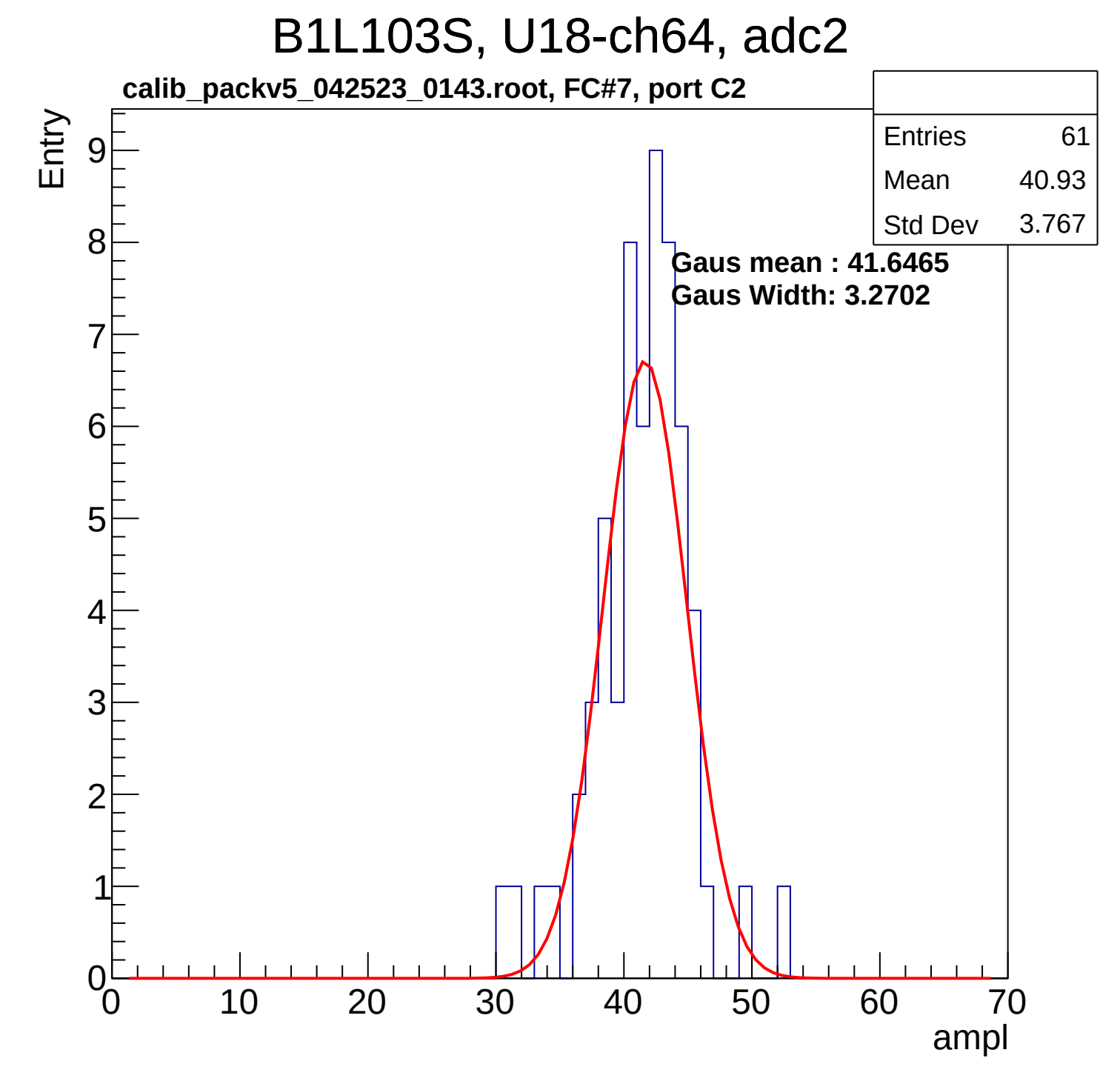
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch64, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 27.87
Std Dev 4.985
Gaus mean : 29.1392
Gaus Width: 3.7777
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch64, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 35.26
Std Dev 4.056
Gaus mean : 35.0340
Gaus Width: 3.8651
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch64, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 61
Mean 40.93
Std Dev 3.767
Gaus mean : 41.6465
Gaus Width: 3.2702
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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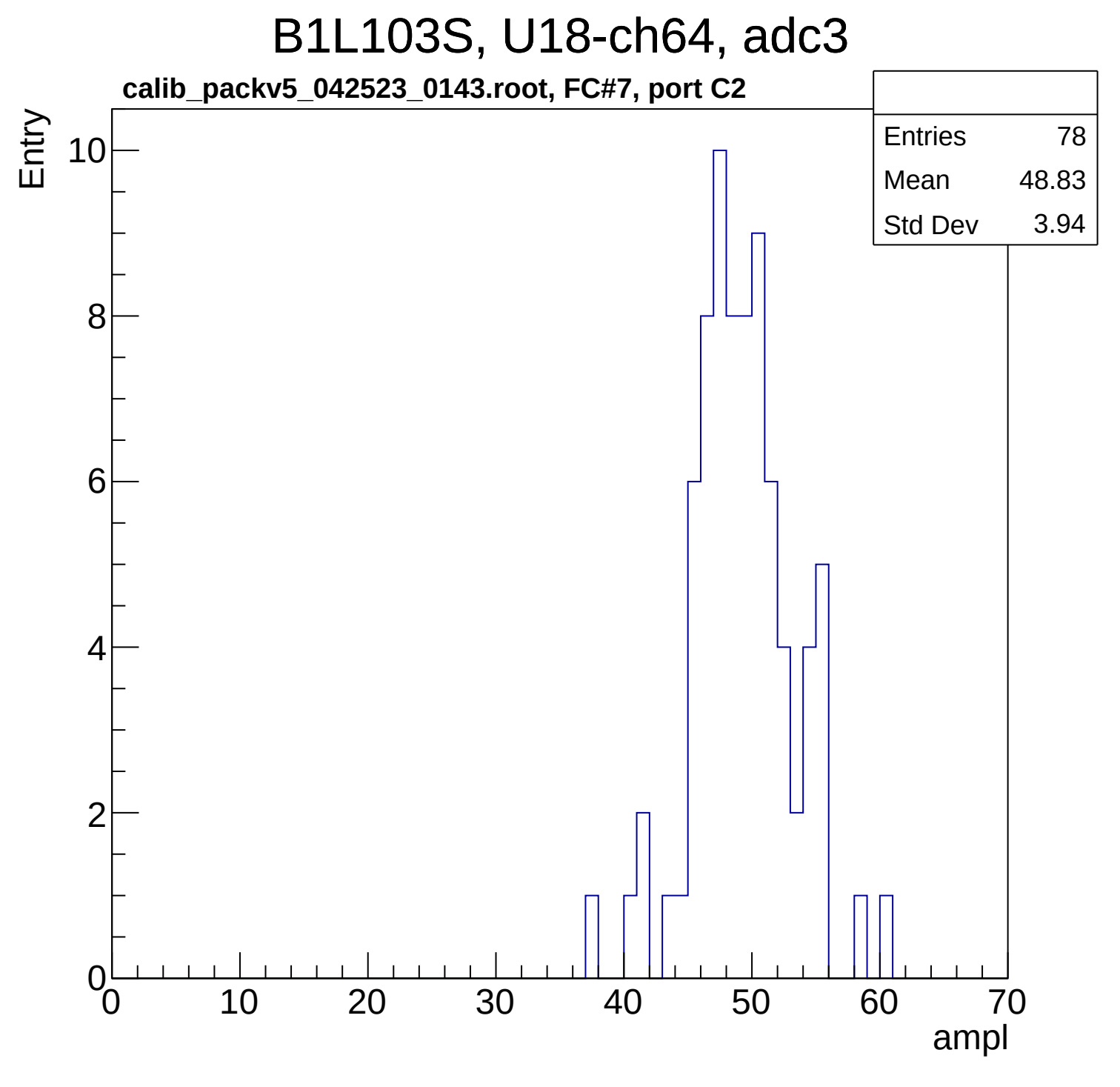
B1L103S, U18-ch64, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 78
Mean 48.83
Std Dev 3.94
Entry
ampl
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4
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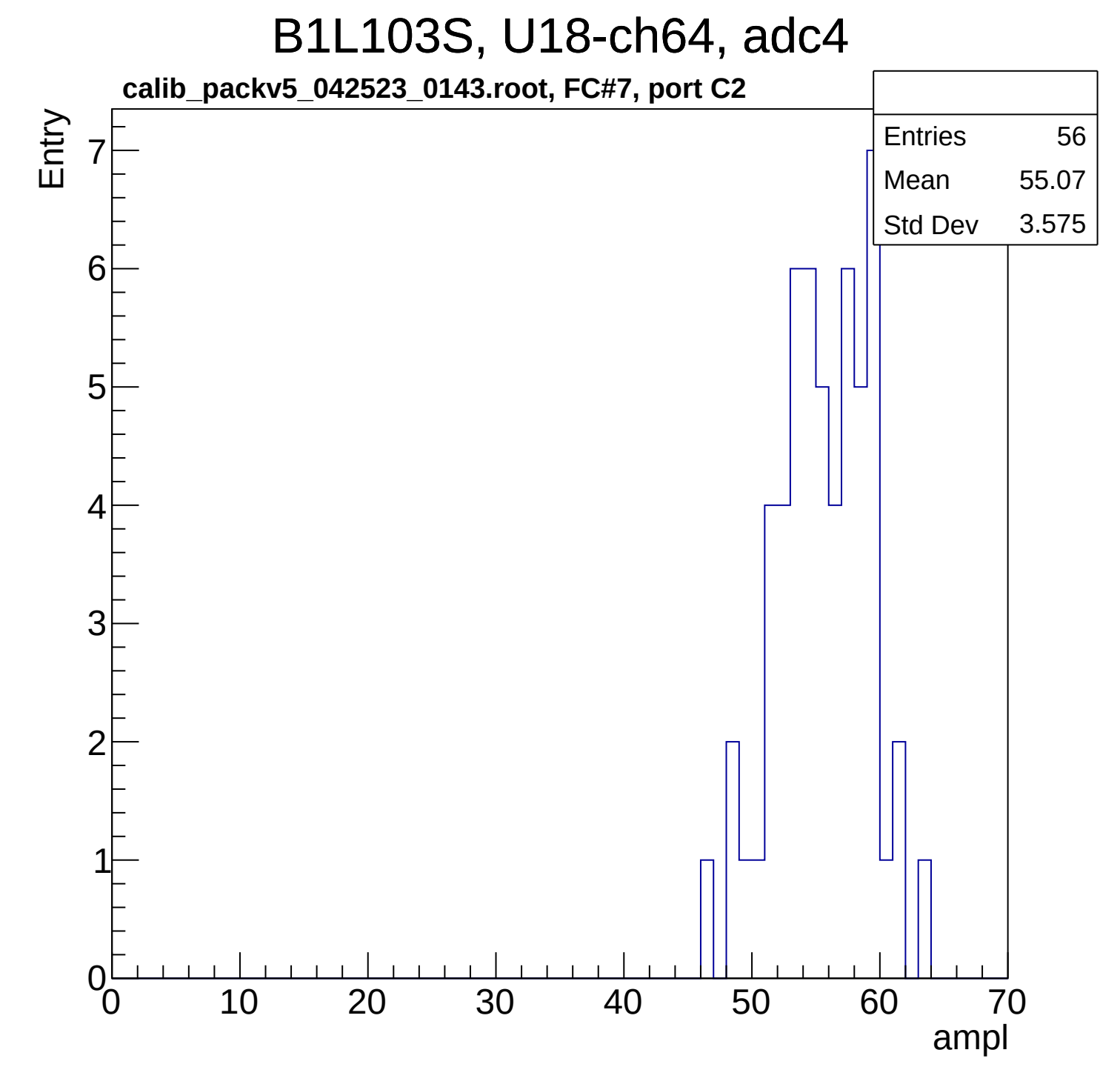
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch64, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 55.07
Std Dev 3.575
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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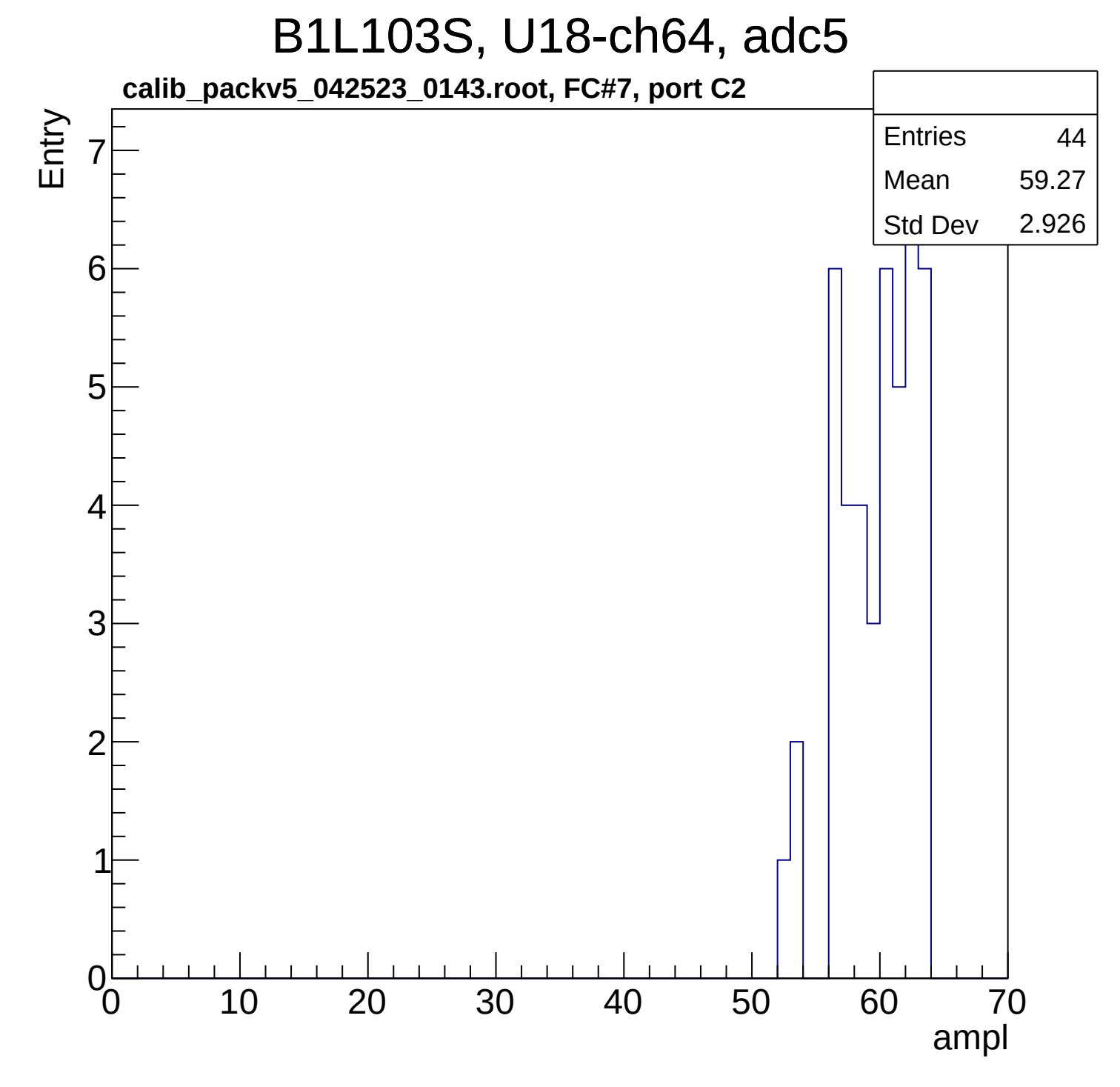
B1L103S, U18-ch64, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 44
Mean 59.27
Std Dev 2.926
Entry
ampl
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2
3
4
5
6
7
0
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20
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40
50
60
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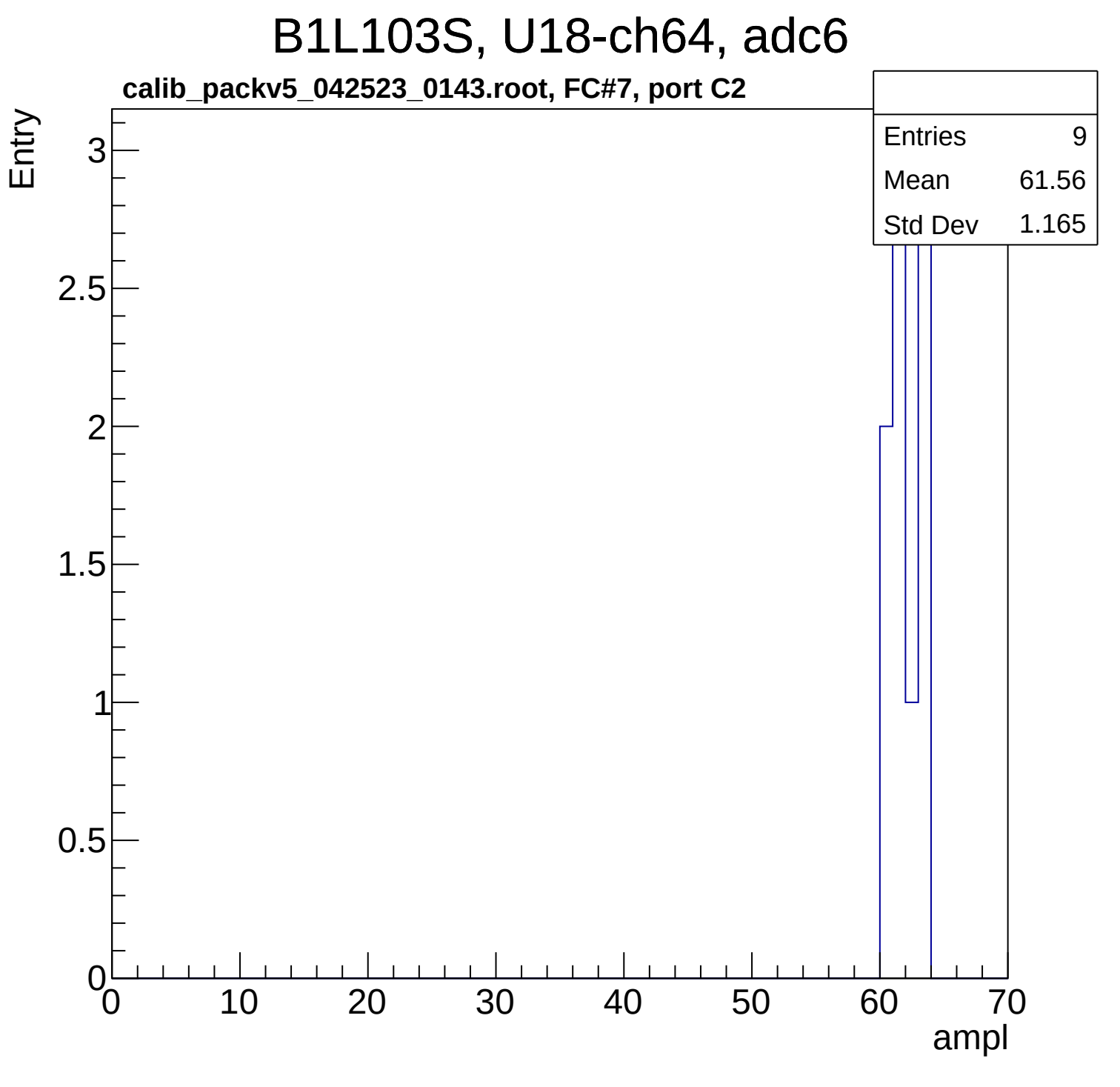
B1L103S, U18-ch64, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 9
Mean 61.56
Std Dev 1.165
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
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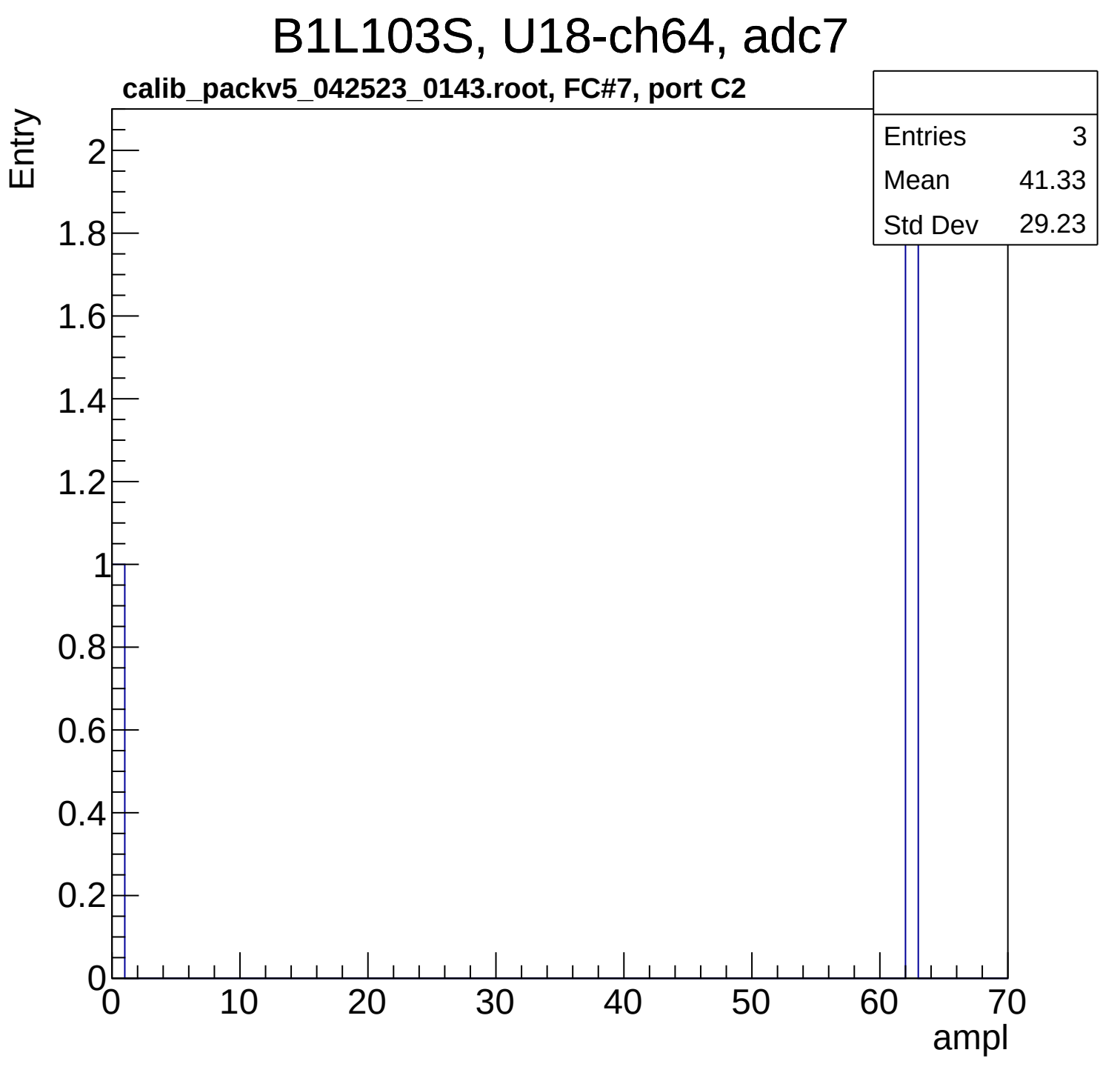
20
30
40
50
60
70


B1L103S, U18-ch64, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 41.33
Std Dev 29.23
Entry
ampl
0
0.2
0.4
0.6
0.8
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1.2
1.4
1.6
1.8
2
0
10
20
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40
50
60
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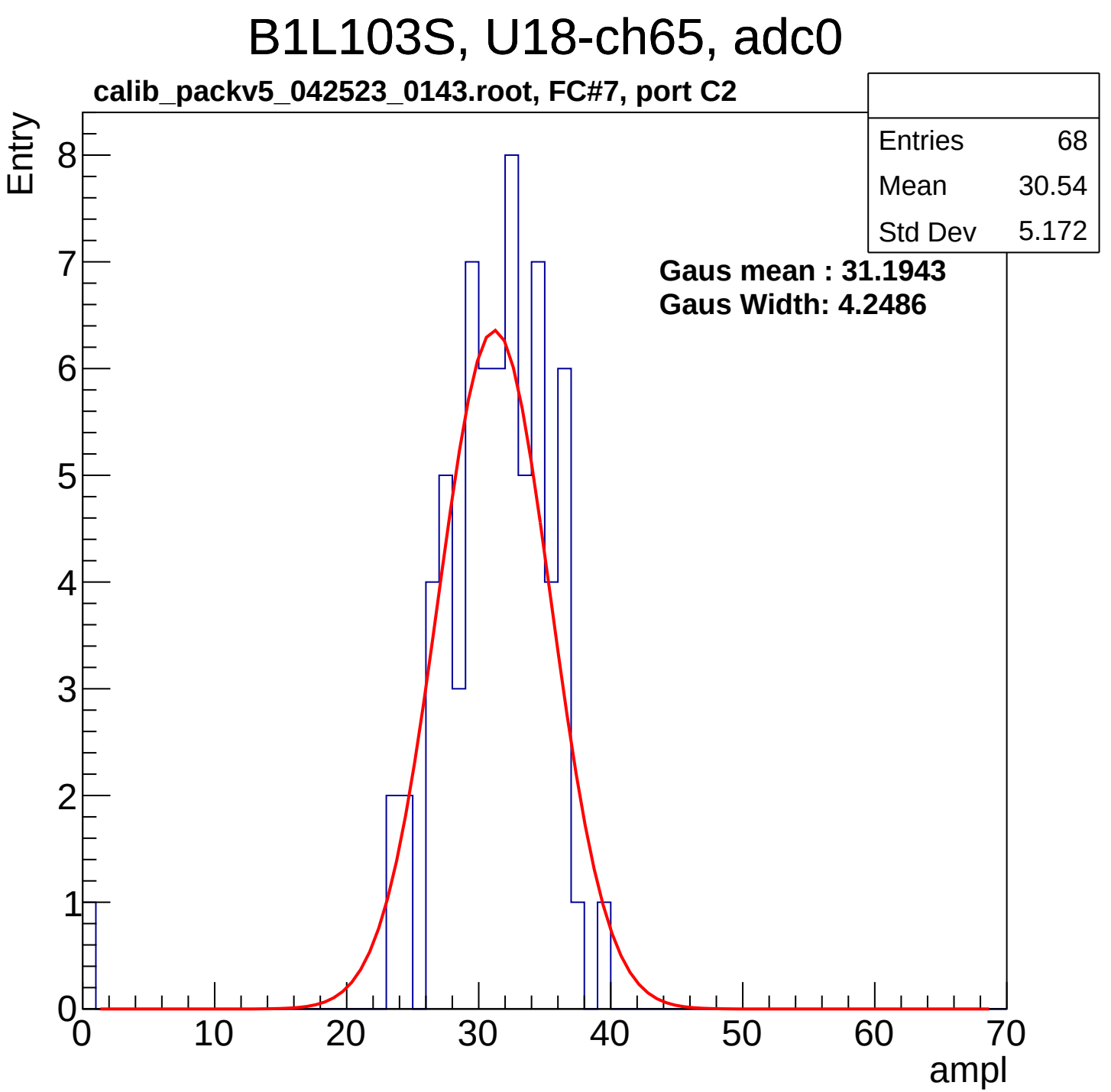
B1L103S, U18-ch65, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 30.54
Std Dev 5.172
Gaus mean : 31.1943
Gaus Width: 4.2486
Entry
ampl
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1
2
3
4
5
6
7
8
0
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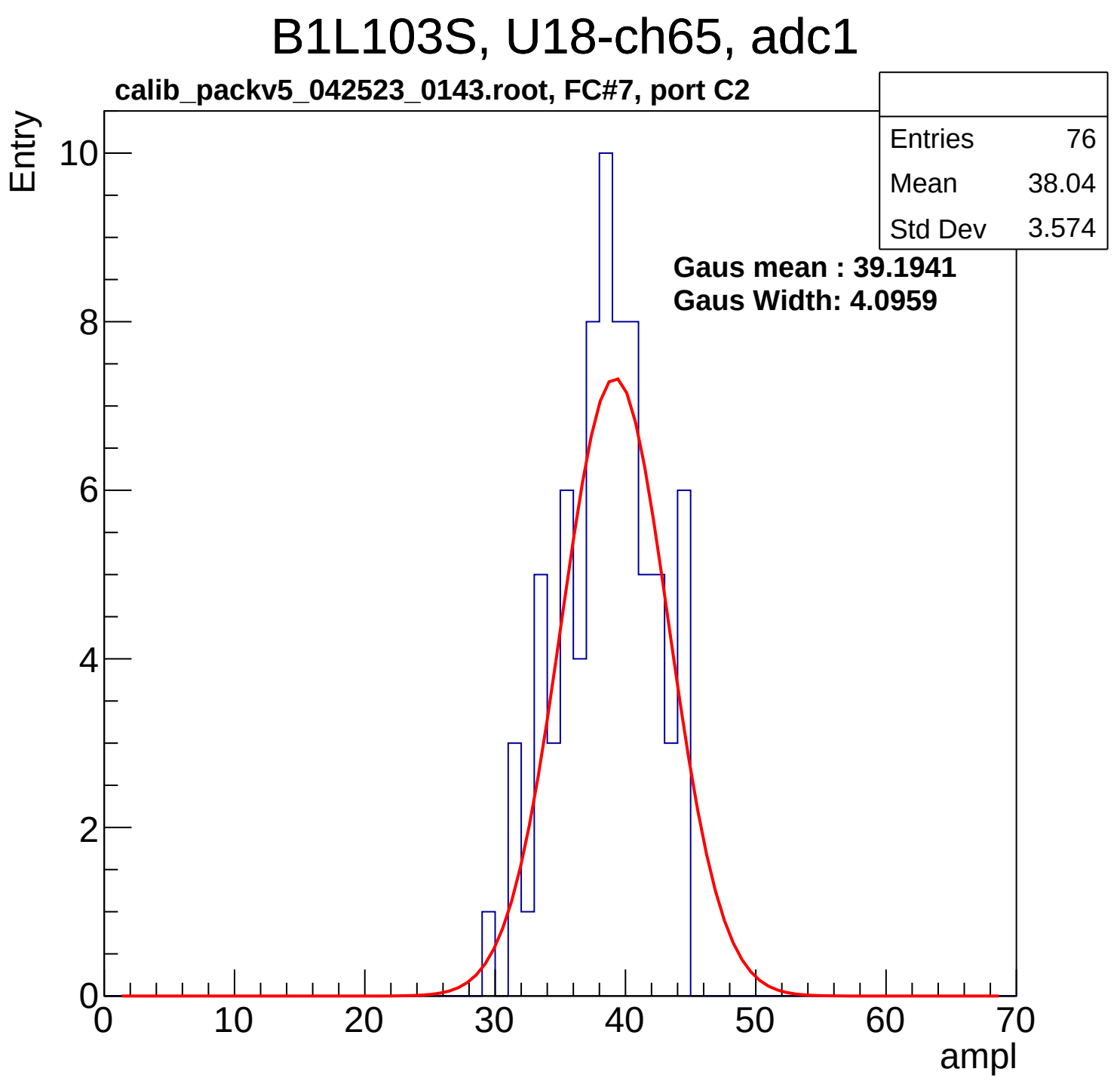
B1L103S, U18-ch65, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 76
Mean 38.04
Std Dev 3.574
Gaus mean : 39.1941
Gaus Width: 4.0959
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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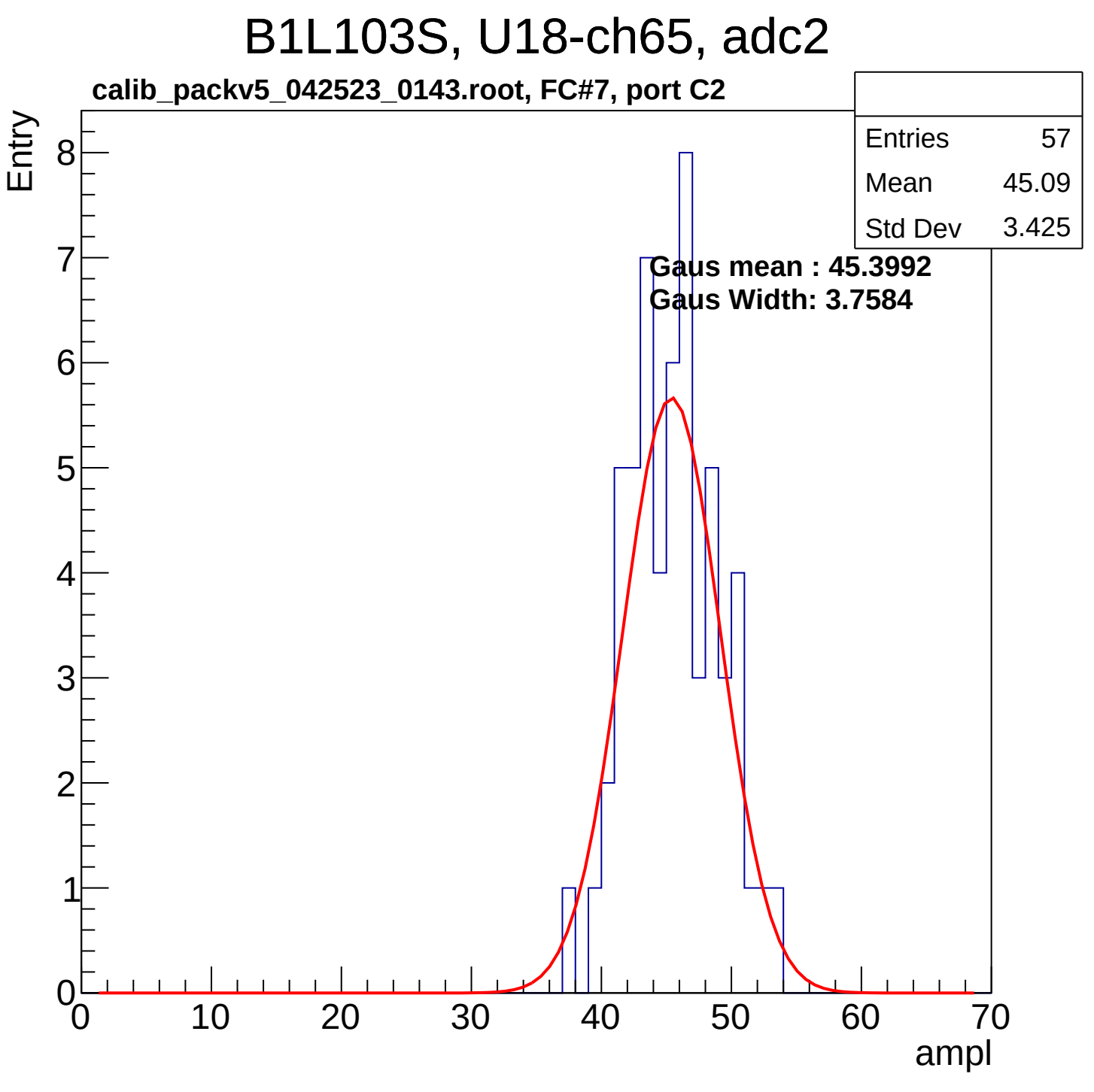
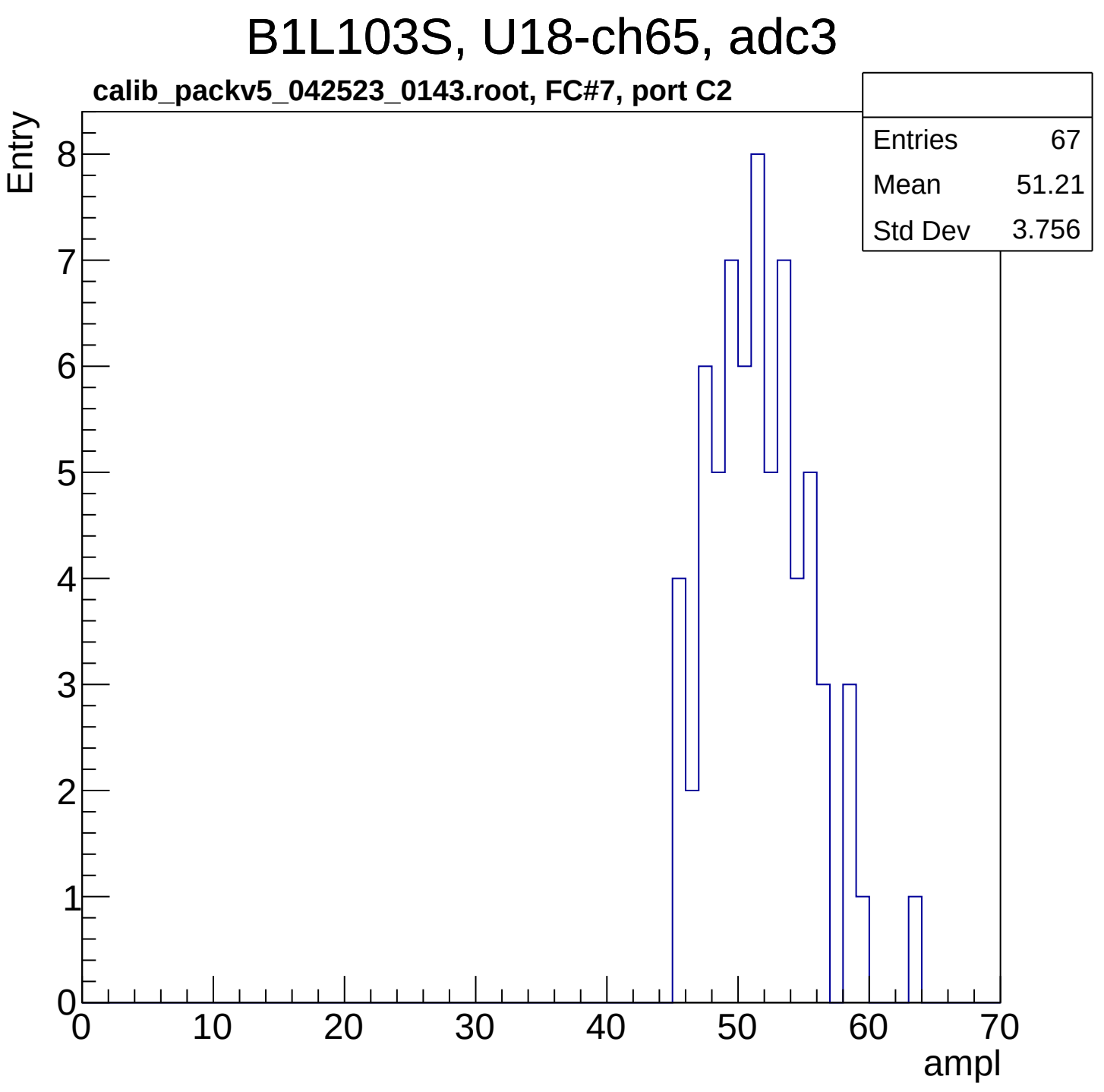

B1L103S, U18-ch65, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 45.09
Std Dev 3.425
Gaus mean : 45.3992
Gaus Width: 3.7584
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch65, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 51.21
Std Dev 3.756
Entry
ampl
0
1
2
3
4
5
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7
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0
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40
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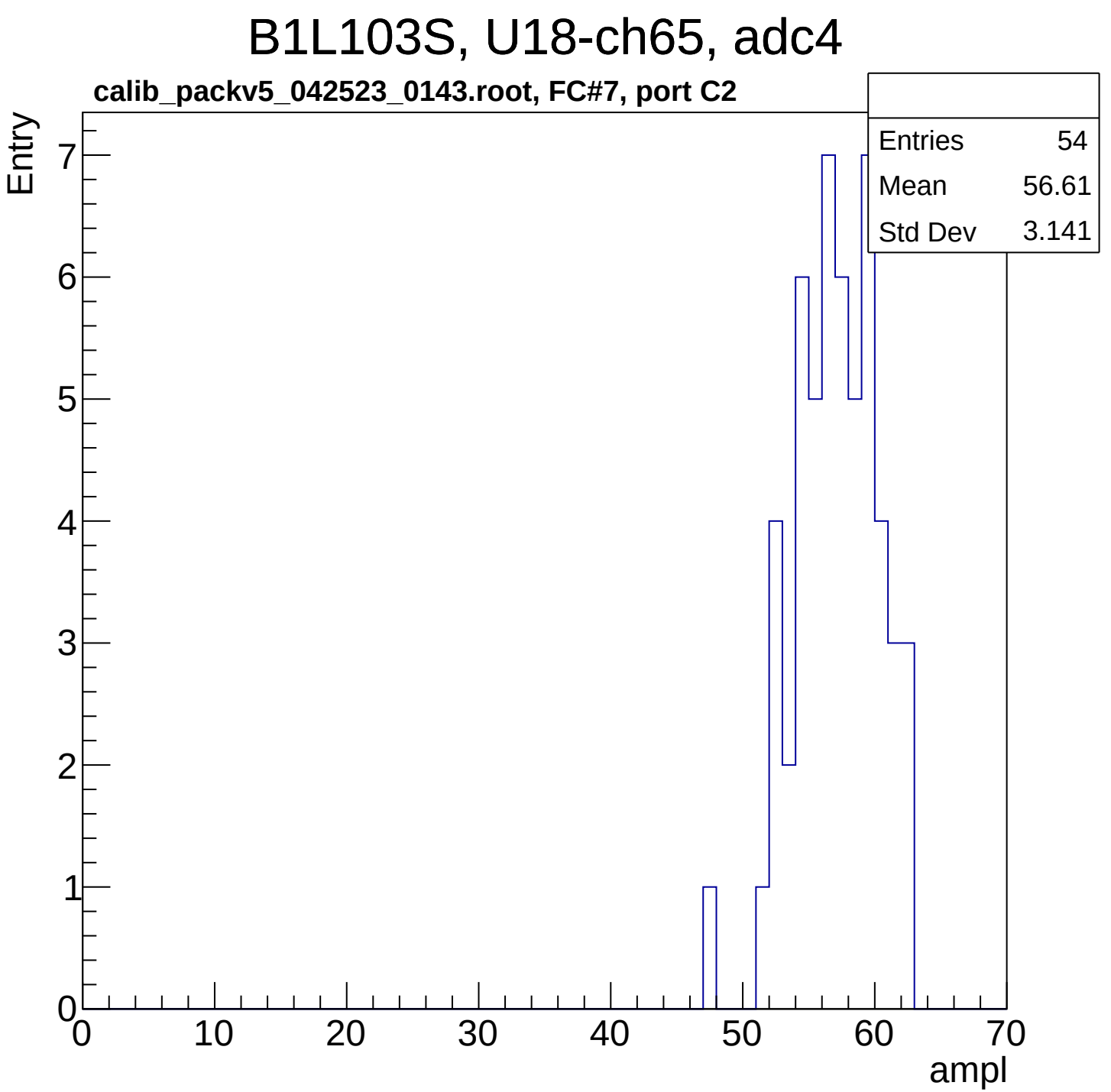
B1L103S, U18-ch65, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 54
Mean 56.61
Std Dev 3.141
Entry
ampl
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1
2
3
4
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0
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40
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60
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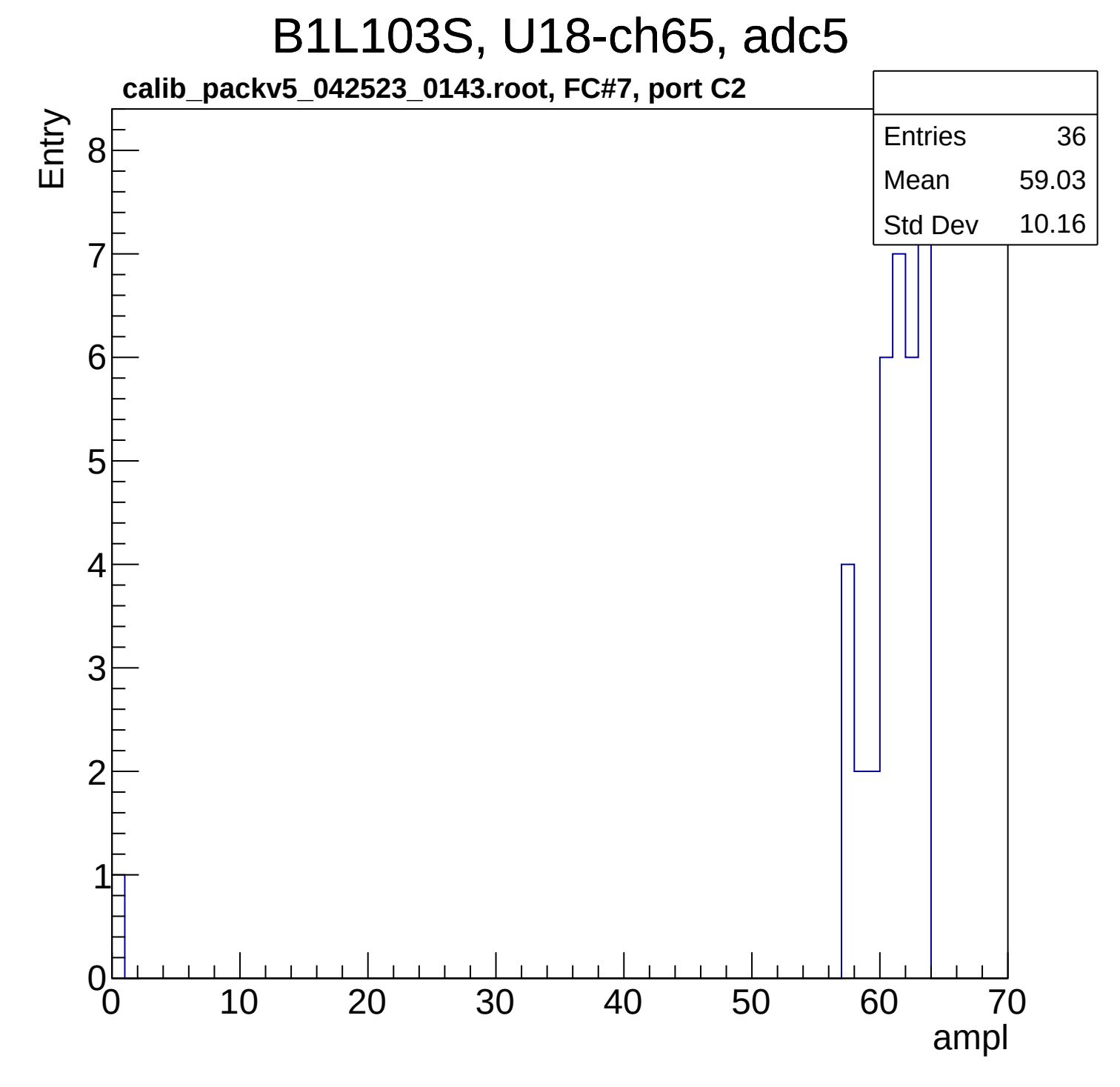
B1L103S, U18-ch65, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 36
Mean 59.03
Std Dev 10.16
Entry
ampl
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1
2
3
4
5
6
7
8
0
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30
40
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60
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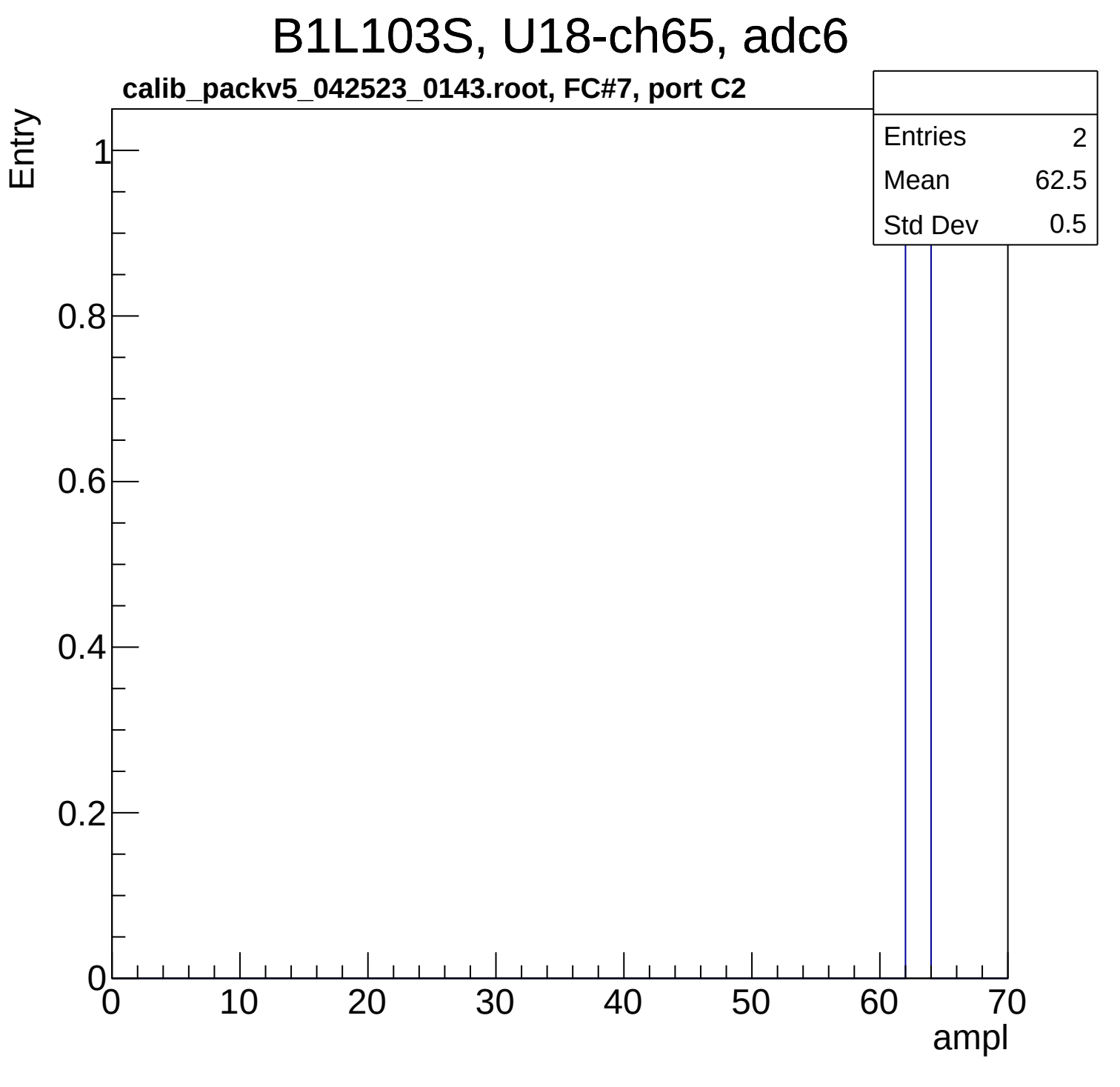
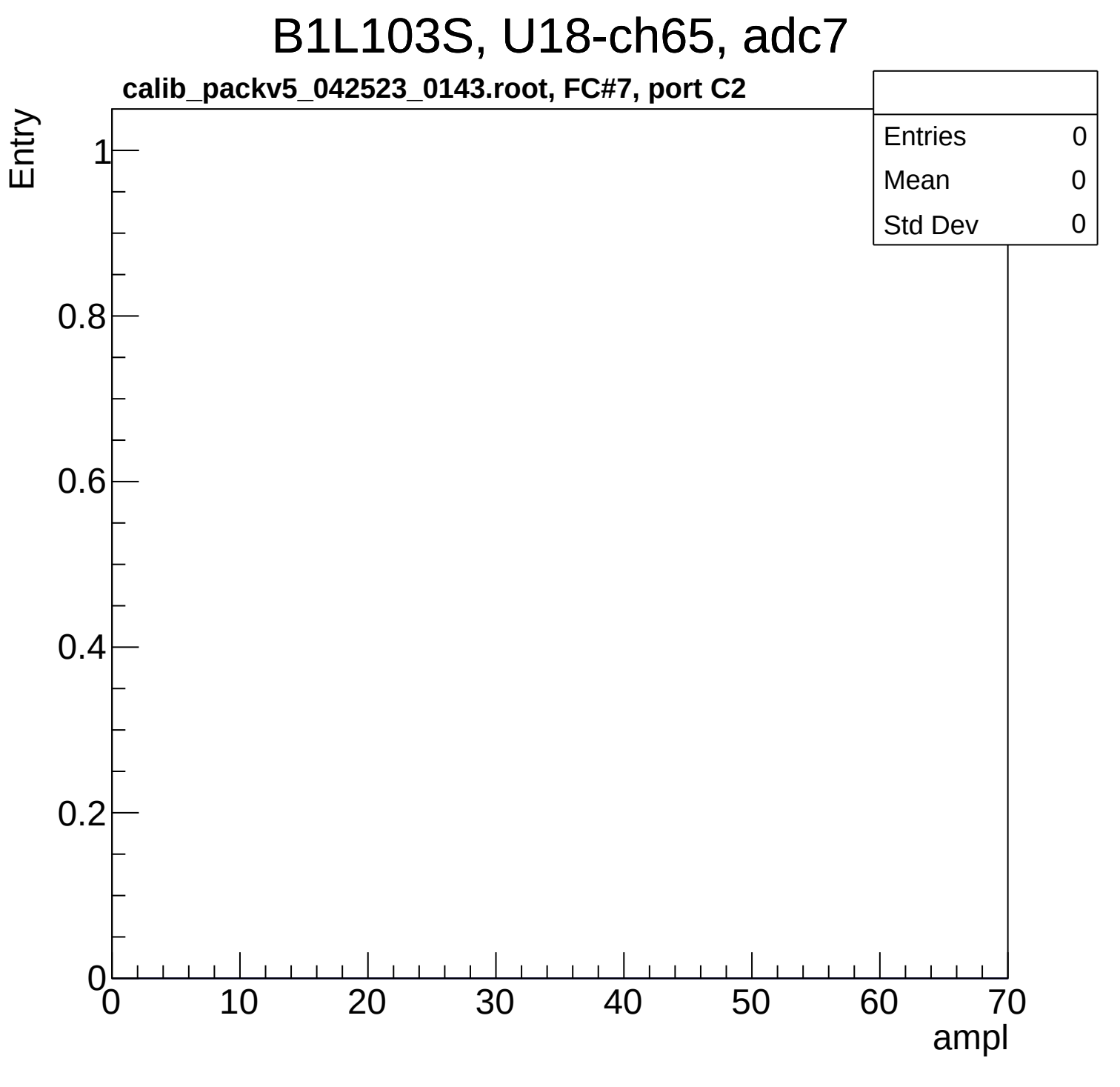
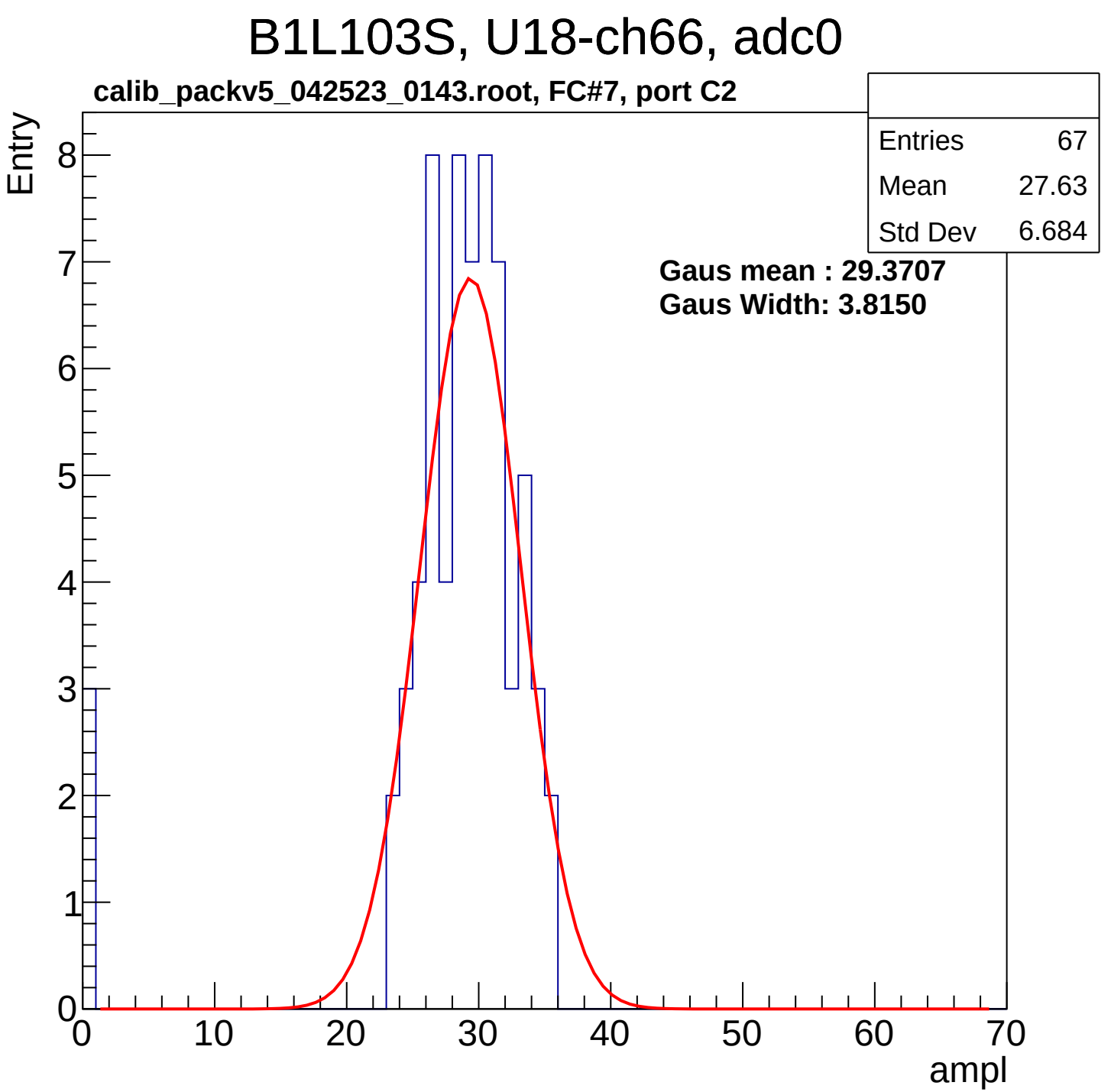

B1L103S, U18-ch65, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch65, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch66, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 27.63
Std Dev 6.684
Gaus mean : 29.3707
Gaus Width: 3.8150
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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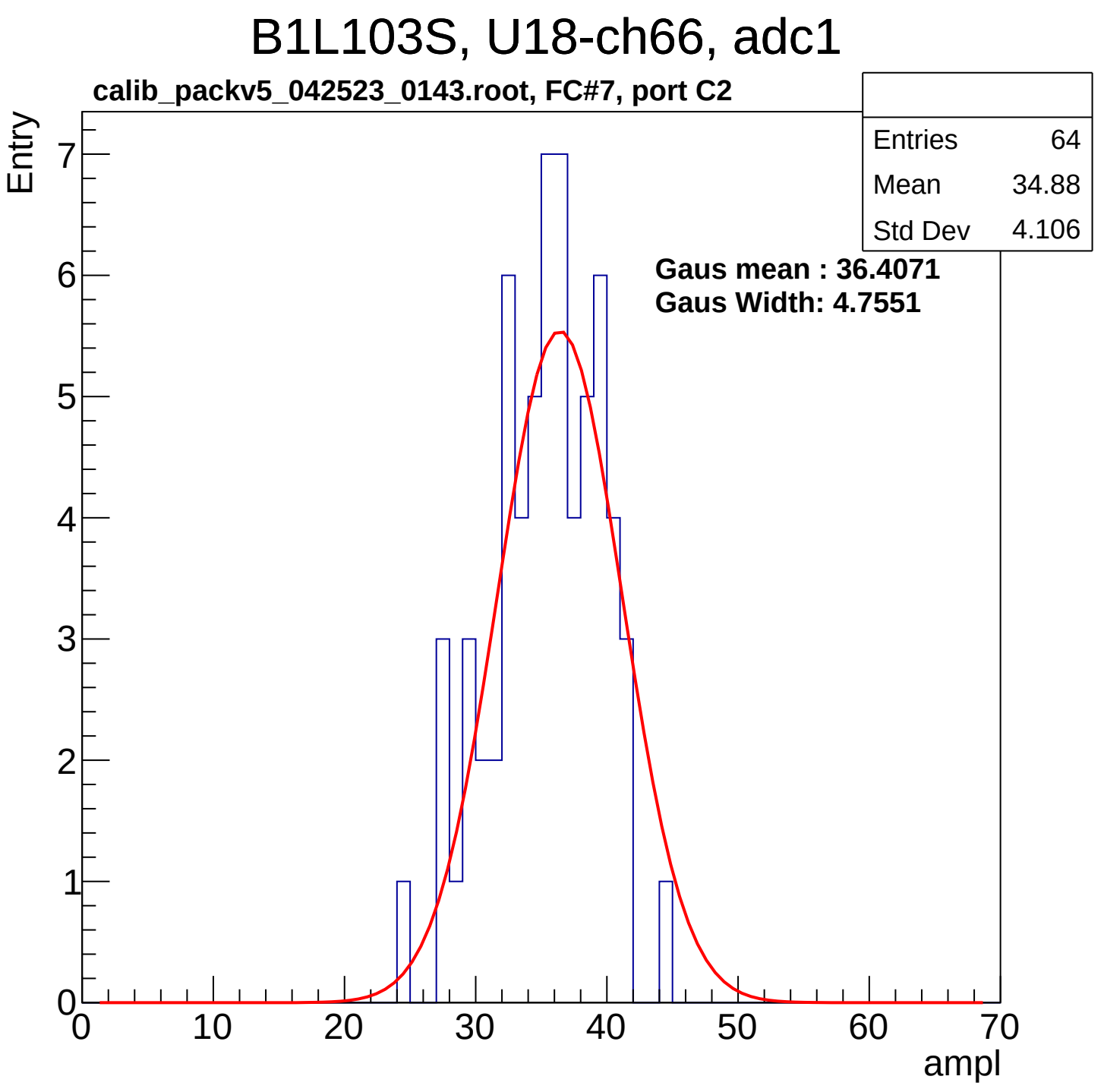
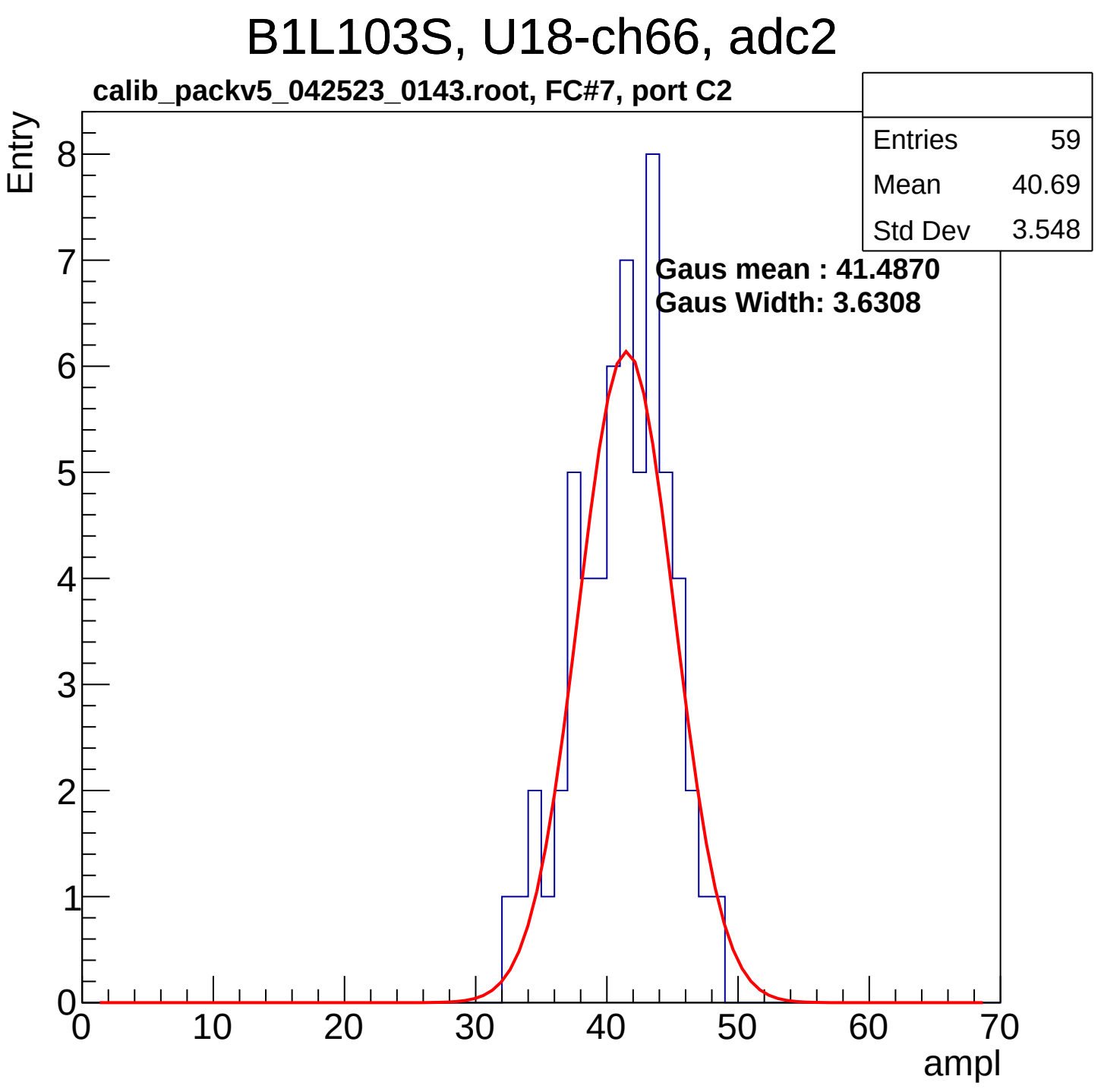

B1L103S, U18-ch66, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 34.88
Std Dev 4.106
Gaus mean : 36.4071
Gaus Width: 4.7551
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch66, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 40.69
Std Dev 3.548
Gaus mean : 41.4870
Gaus Width: 3.6308
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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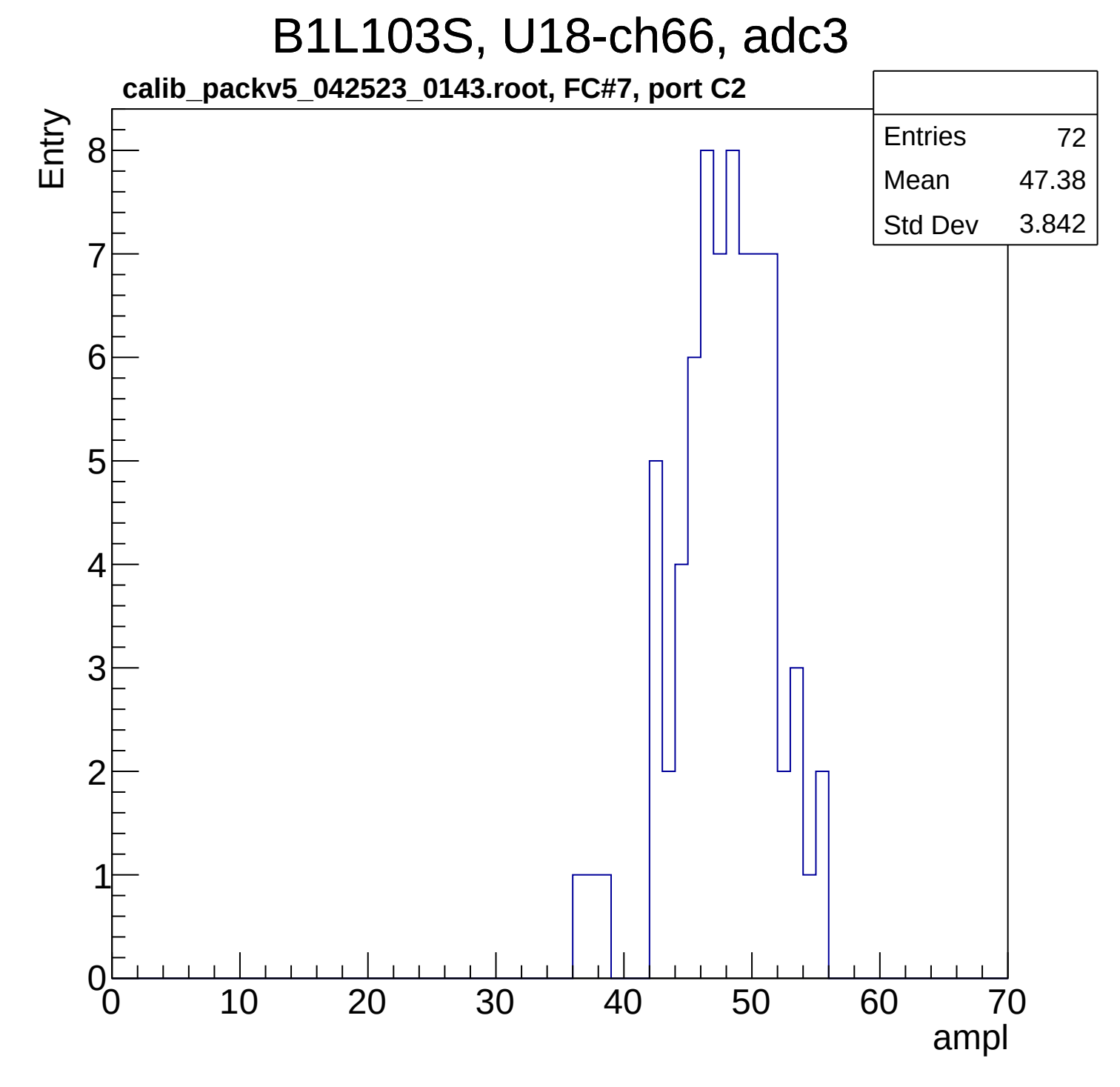
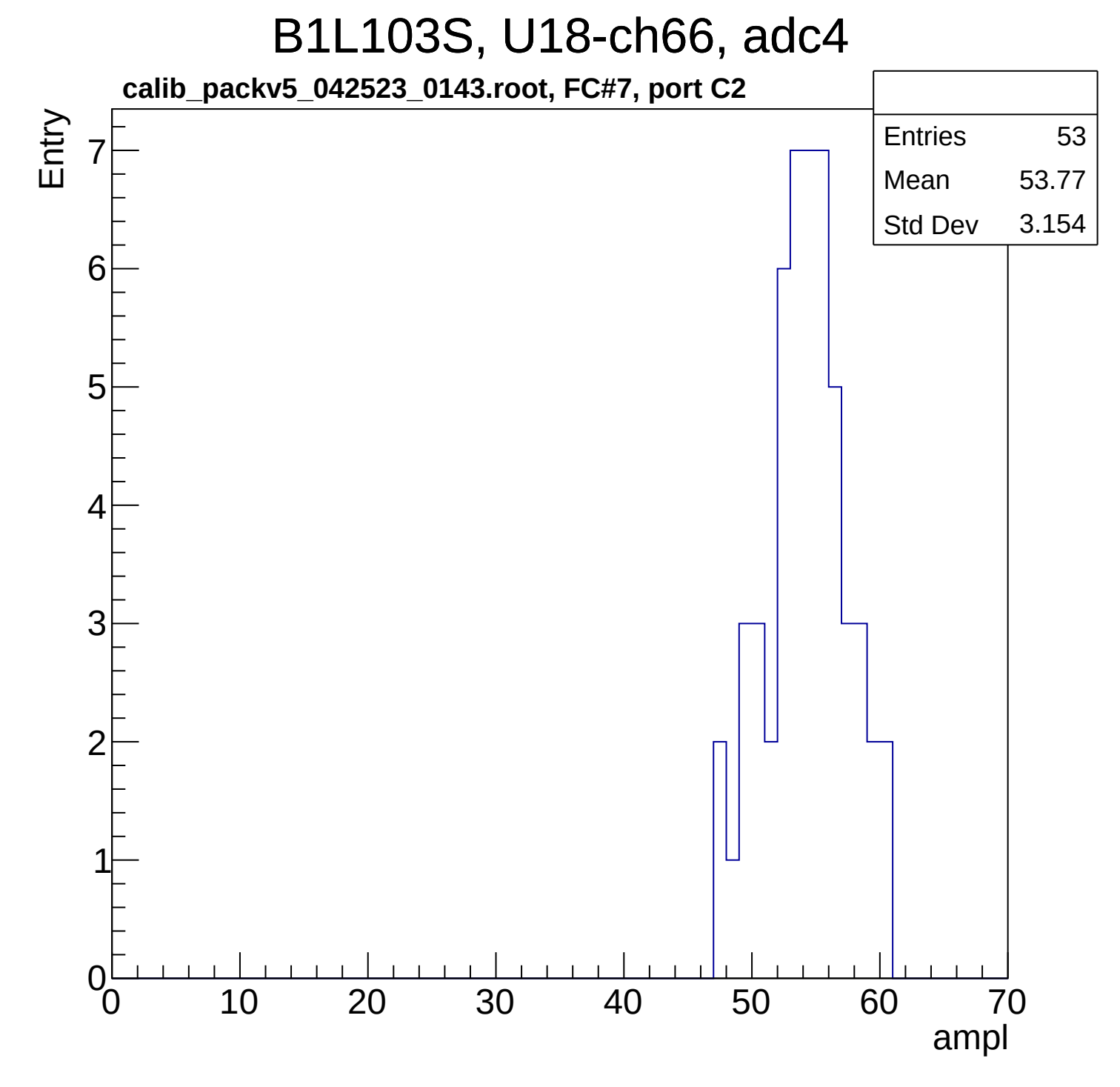
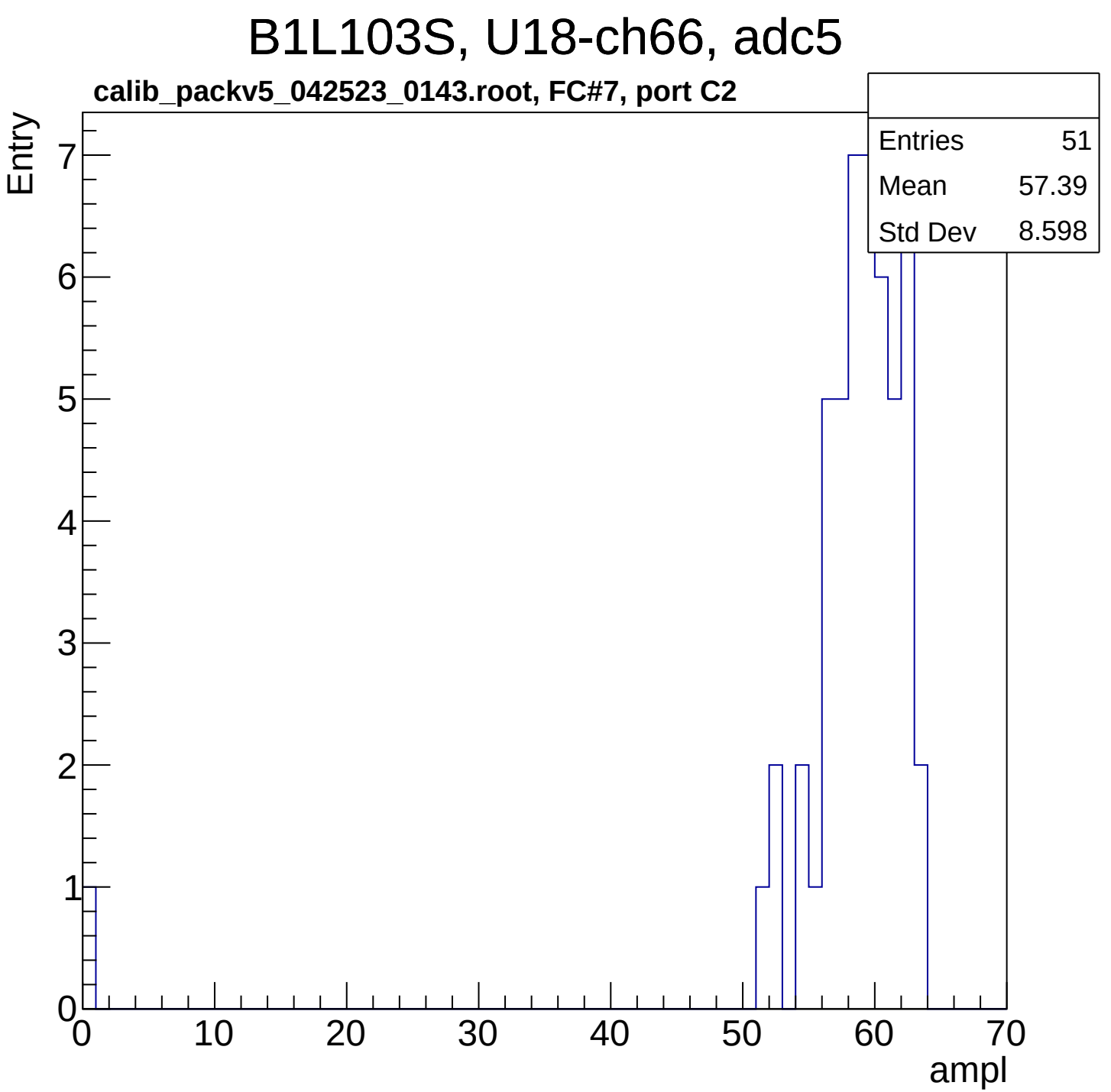
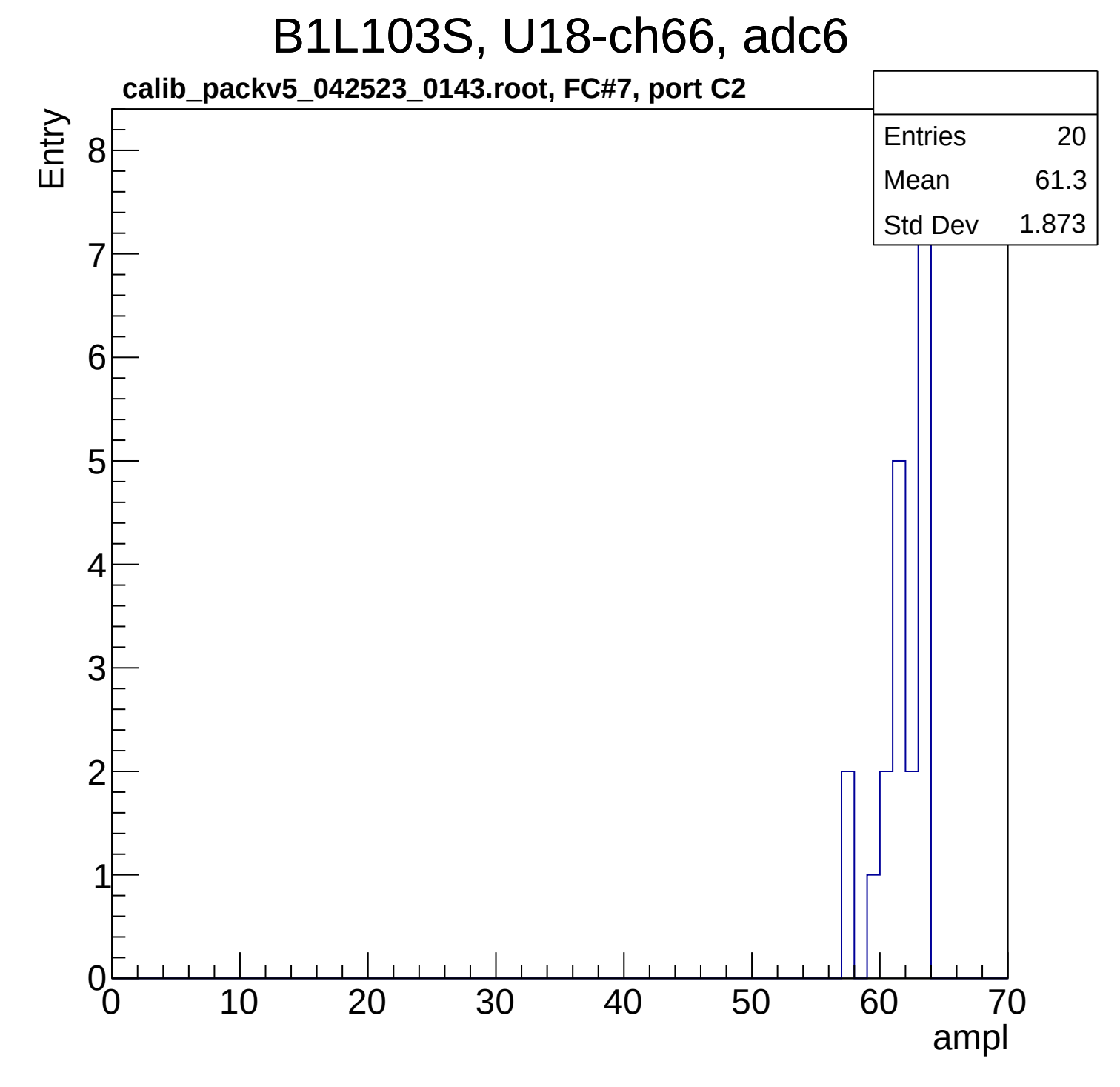
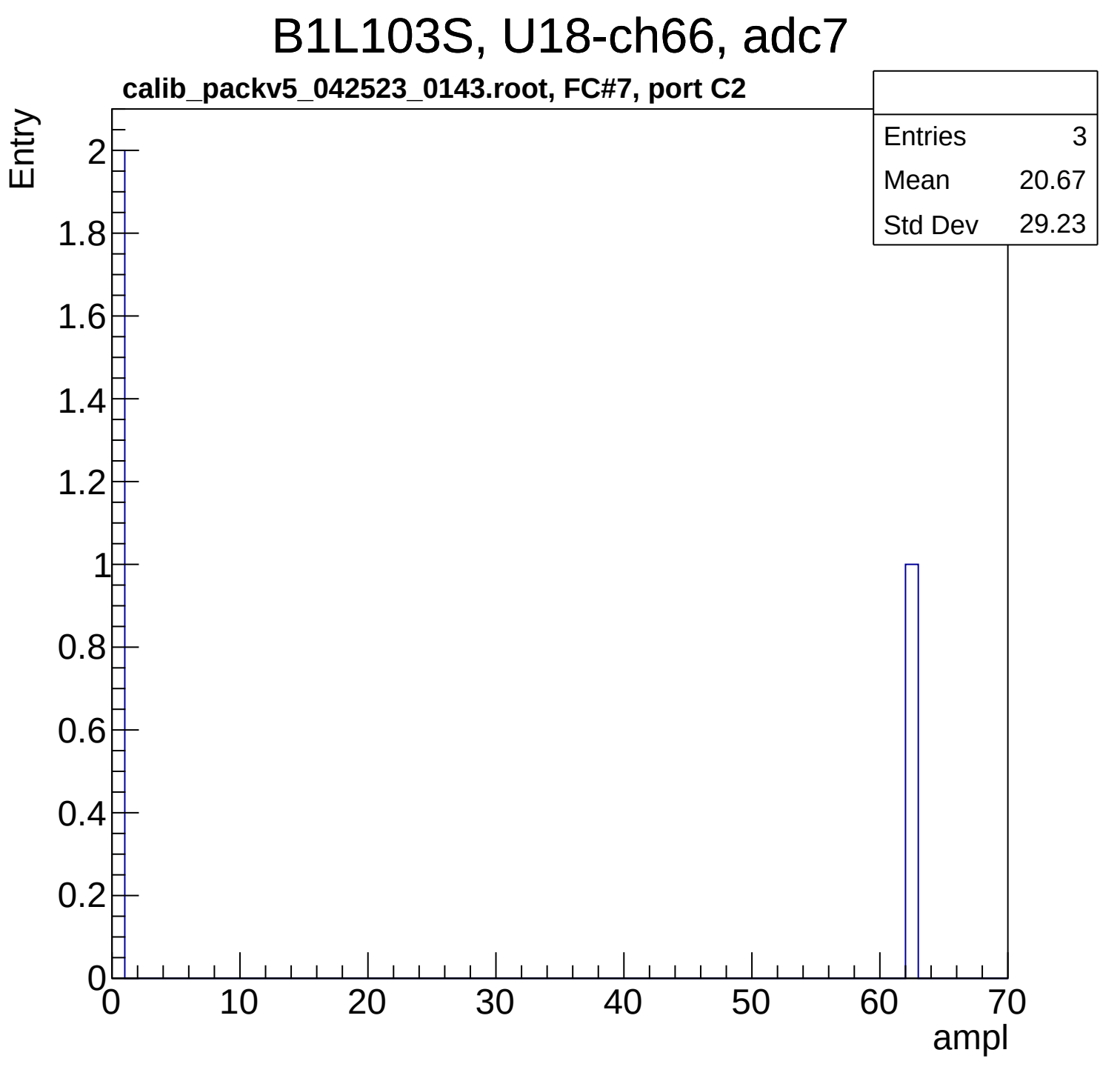
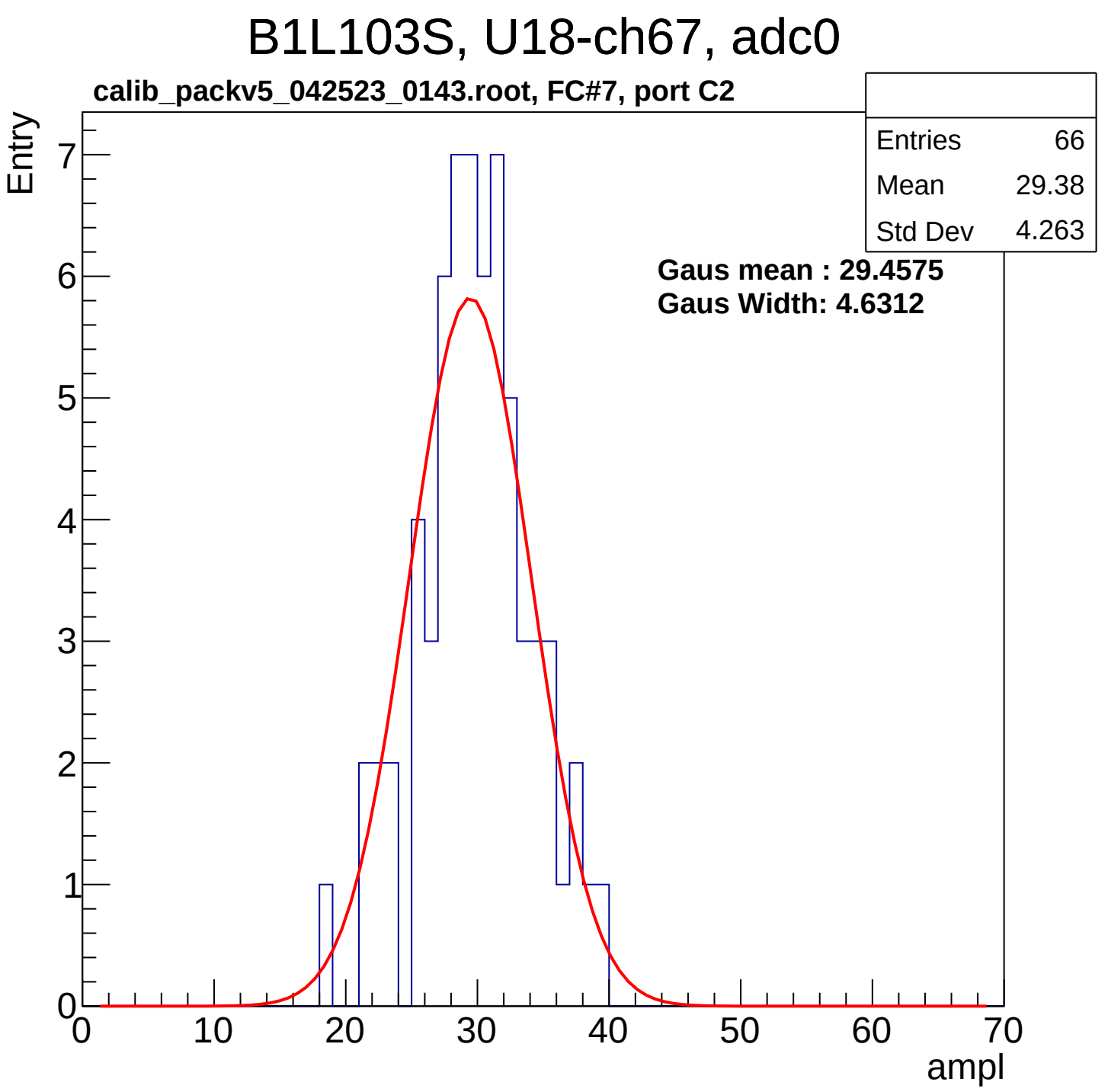

B1L103S, U18-ch66, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 72
Mean 47.38
Std Dev 3.842
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

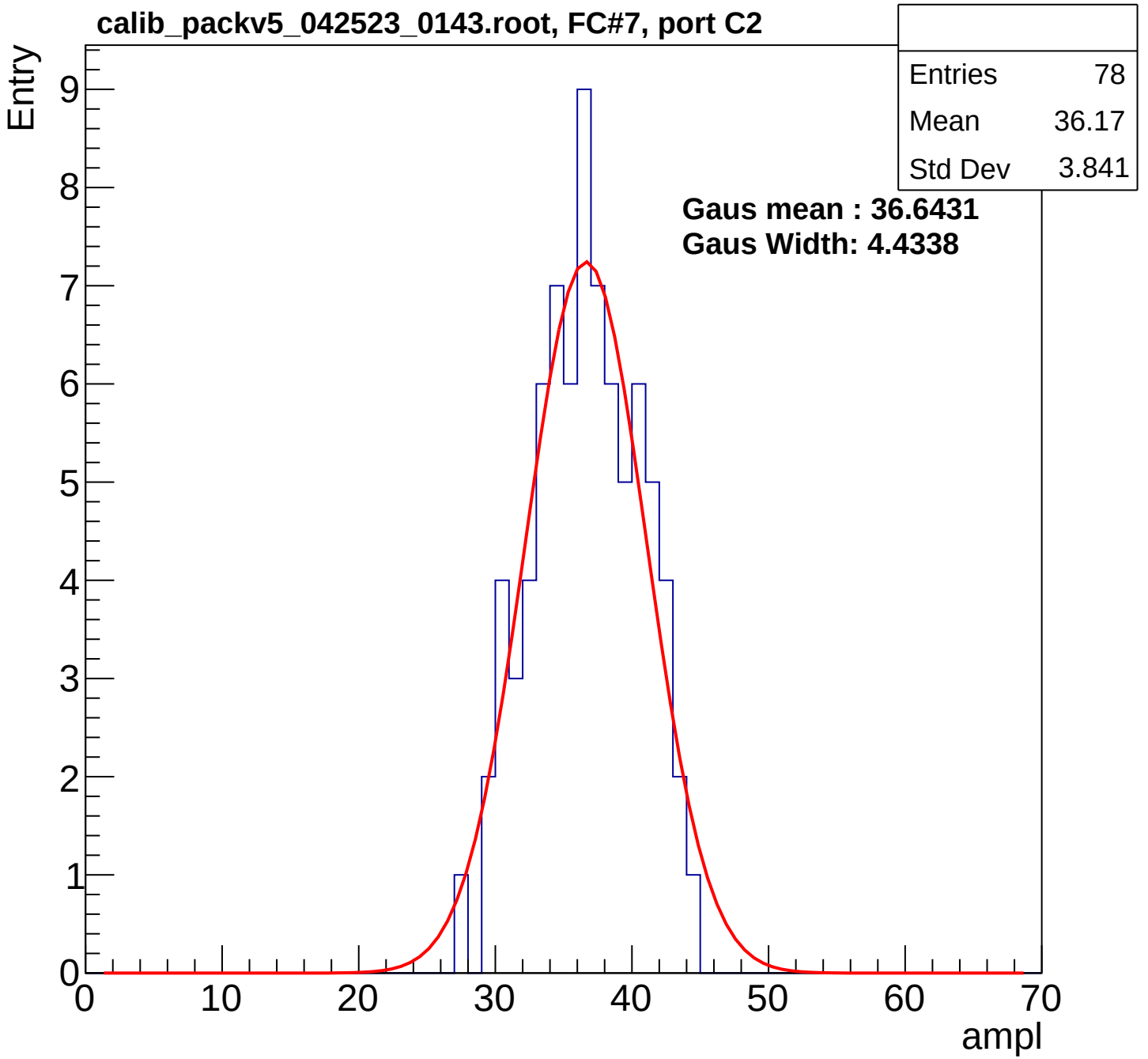

B1L103S, U18-ch66, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 53.77
Std Dev 3.154
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch66, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 51
Mean 57.39
Std Dev 8.598
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch66, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 20
Mean 61.3
Std Dev 1.873
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch66, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 20.67
Std Dev 29.23
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U18-ch67, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 29.38
Std Dev 4.263
Gaus mean : 29.4575
Gaus Width: 4.6312
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch67, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 78
Mean 36.17
Std Dev 3.841
Gaus mean : 36.6431
Gaus Width: 4.4338
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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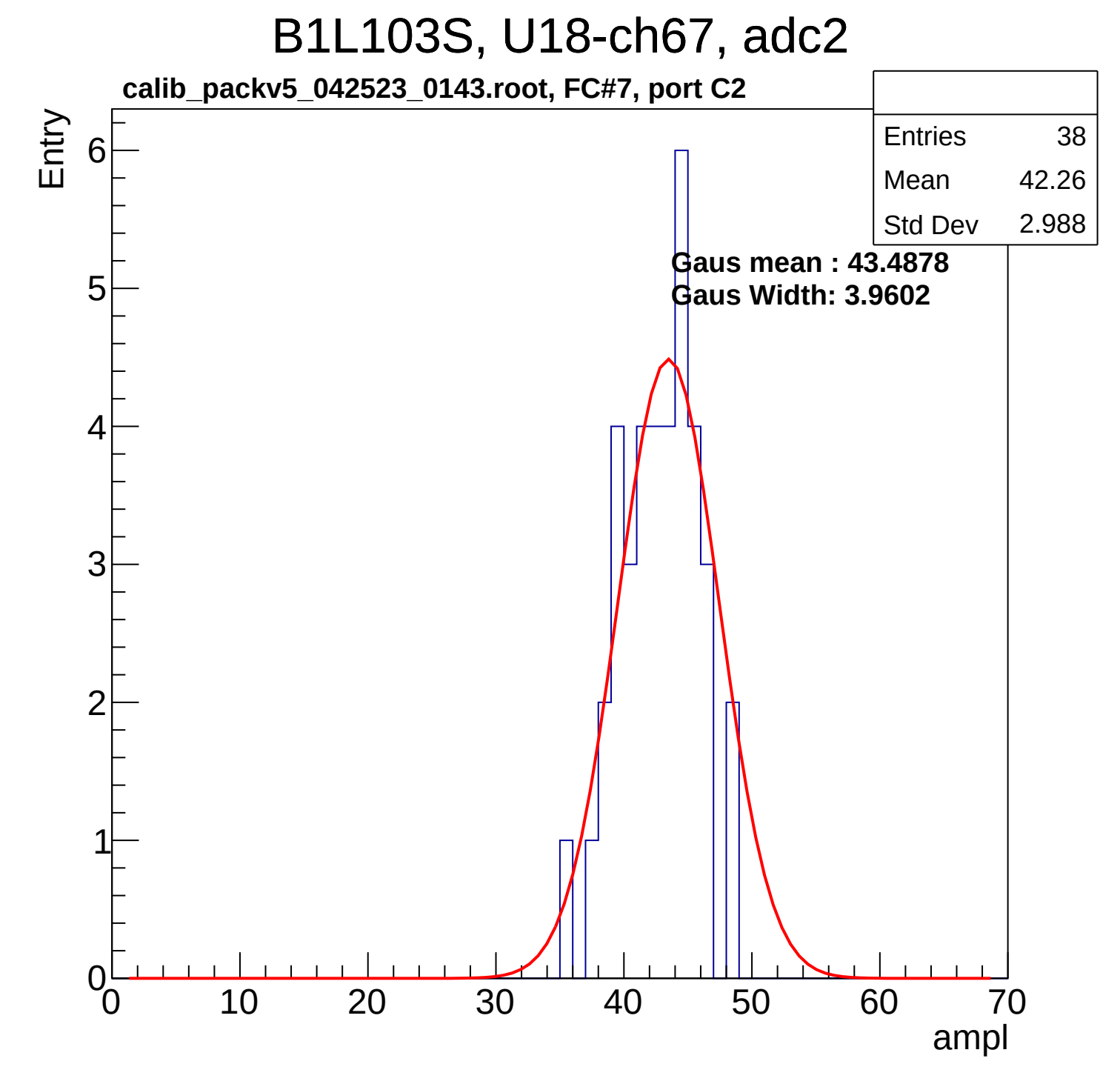
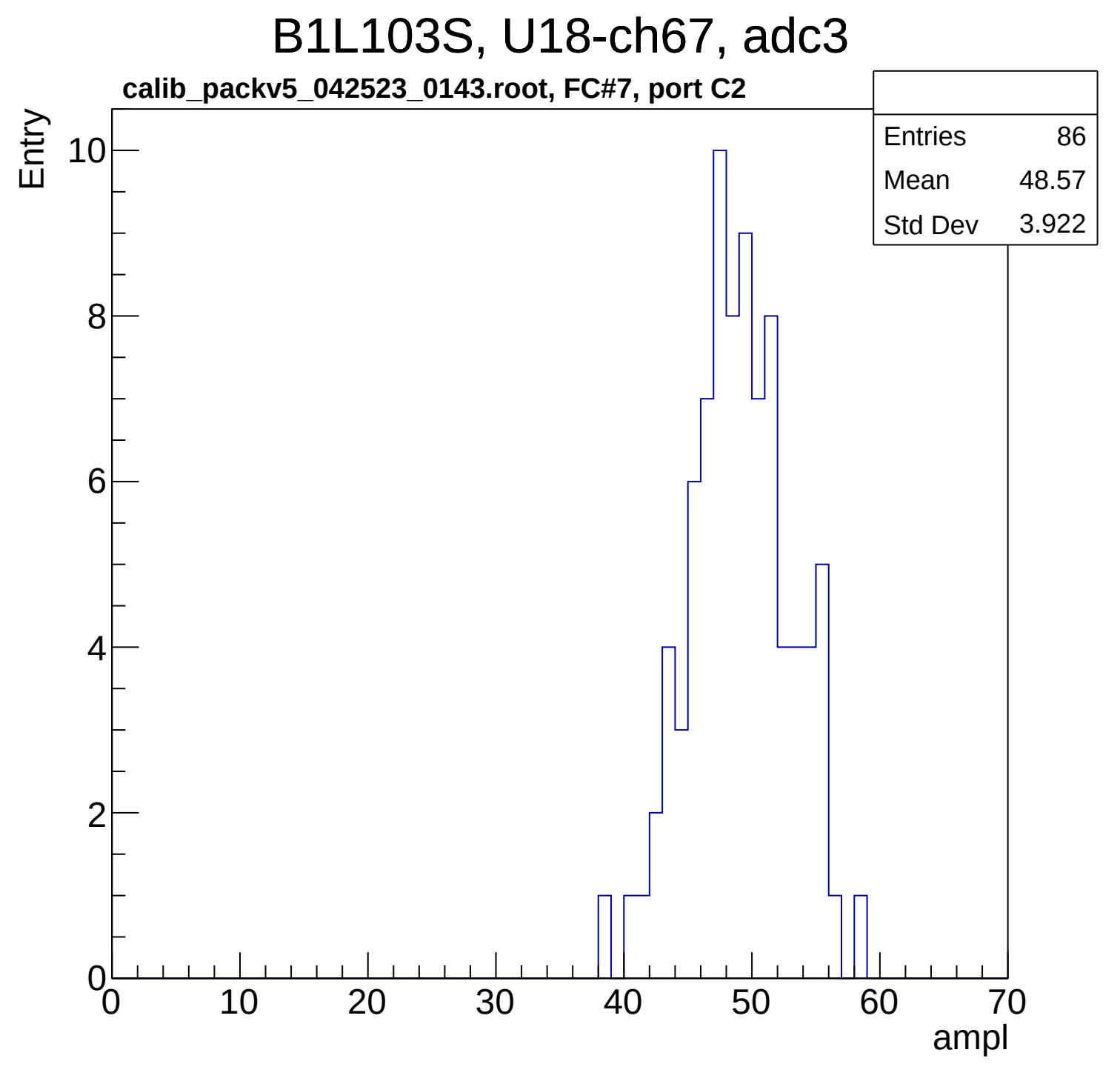
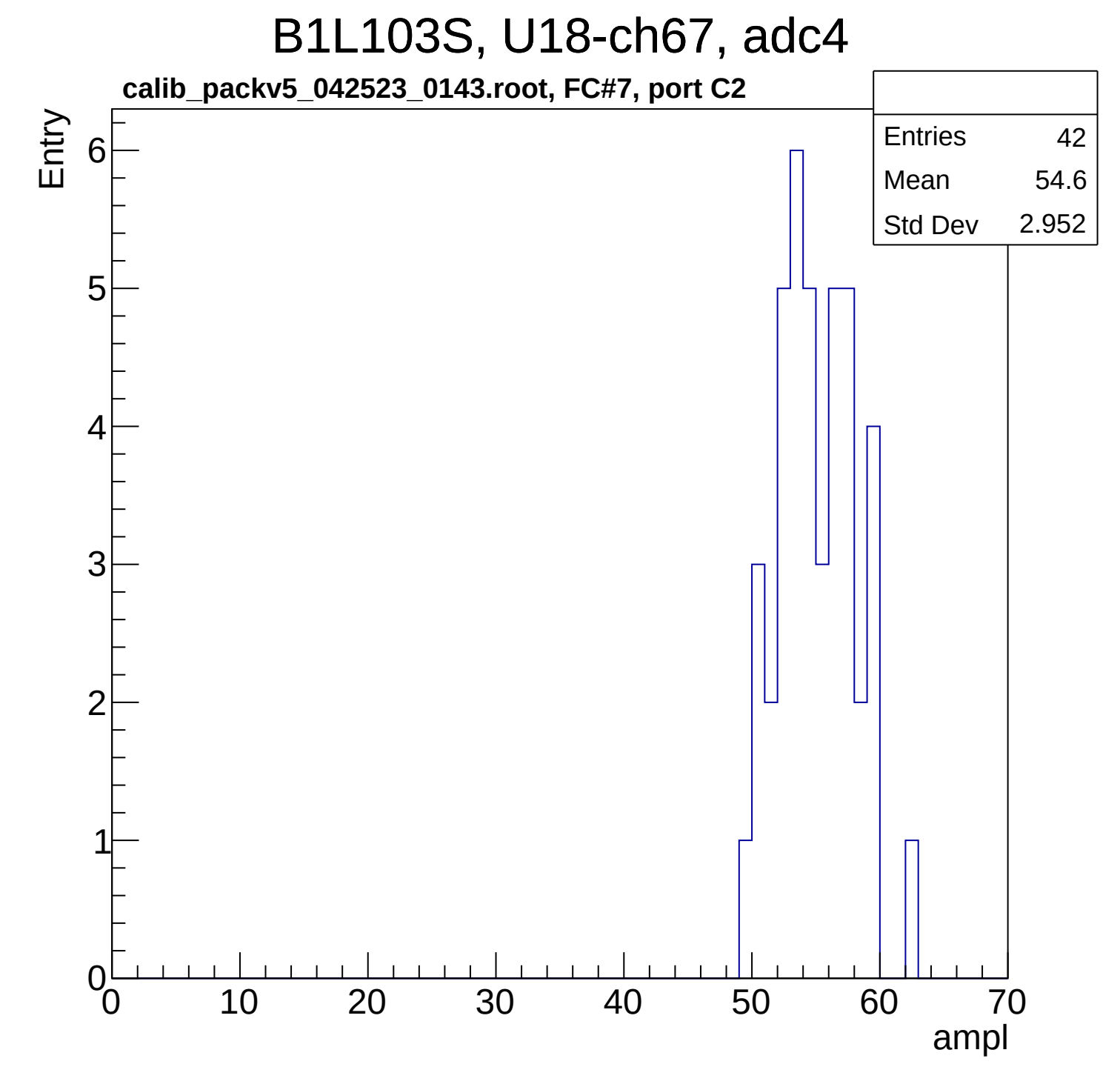
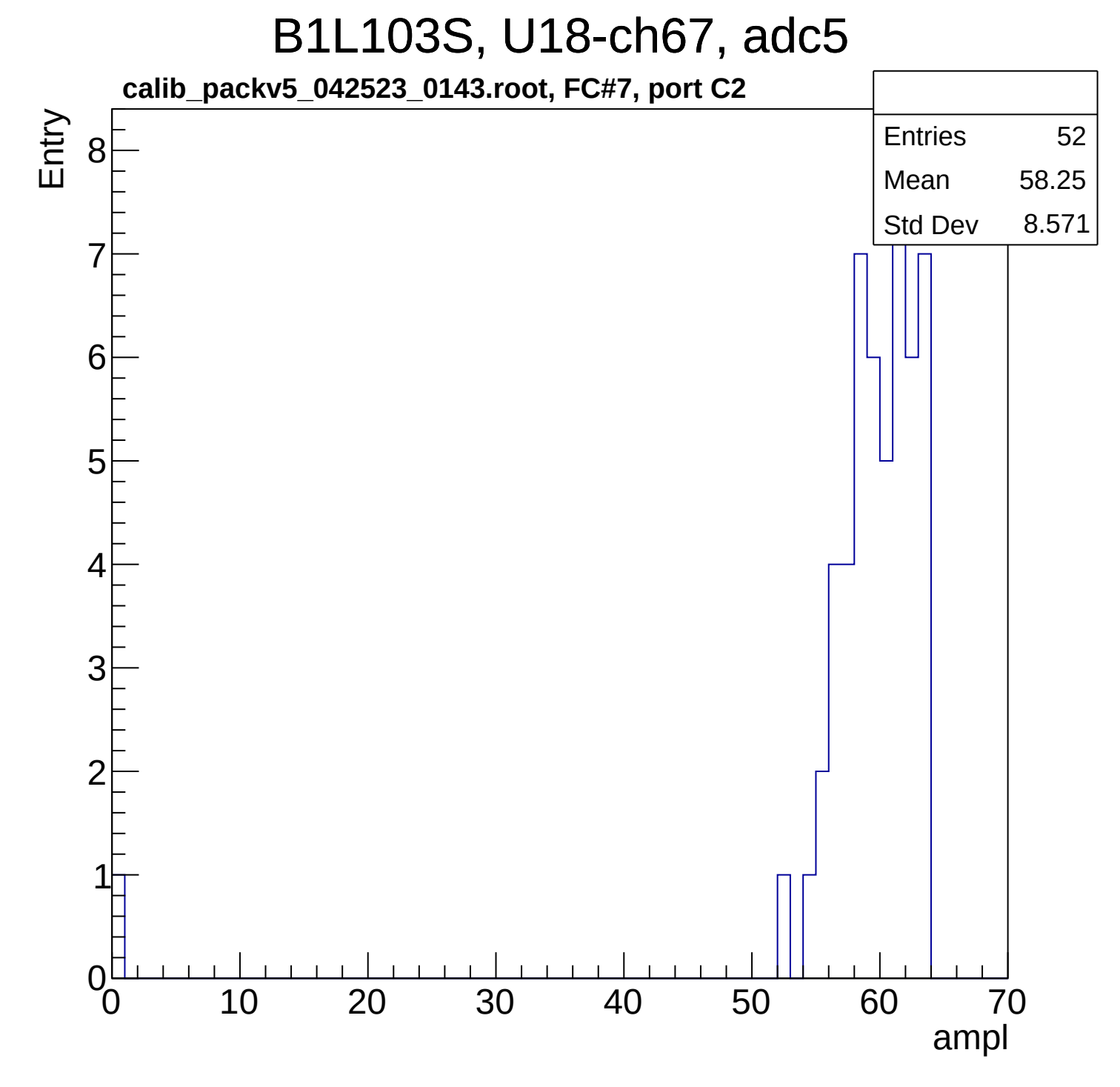

B1L103S, U18-ch67, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 38
Mean 42.26
Std Dev 2.988
Gaus mean : 43.4878
Gaus Width: 3.9602
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U18-ch67, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 86
Mean 48.57
Std Dev 3.922
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch67, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 42
Mean 54.6
Std Dev 2.952
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U18-ch67, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 52
Mean 58.25
Std Dev 8.571
Entry
ampl
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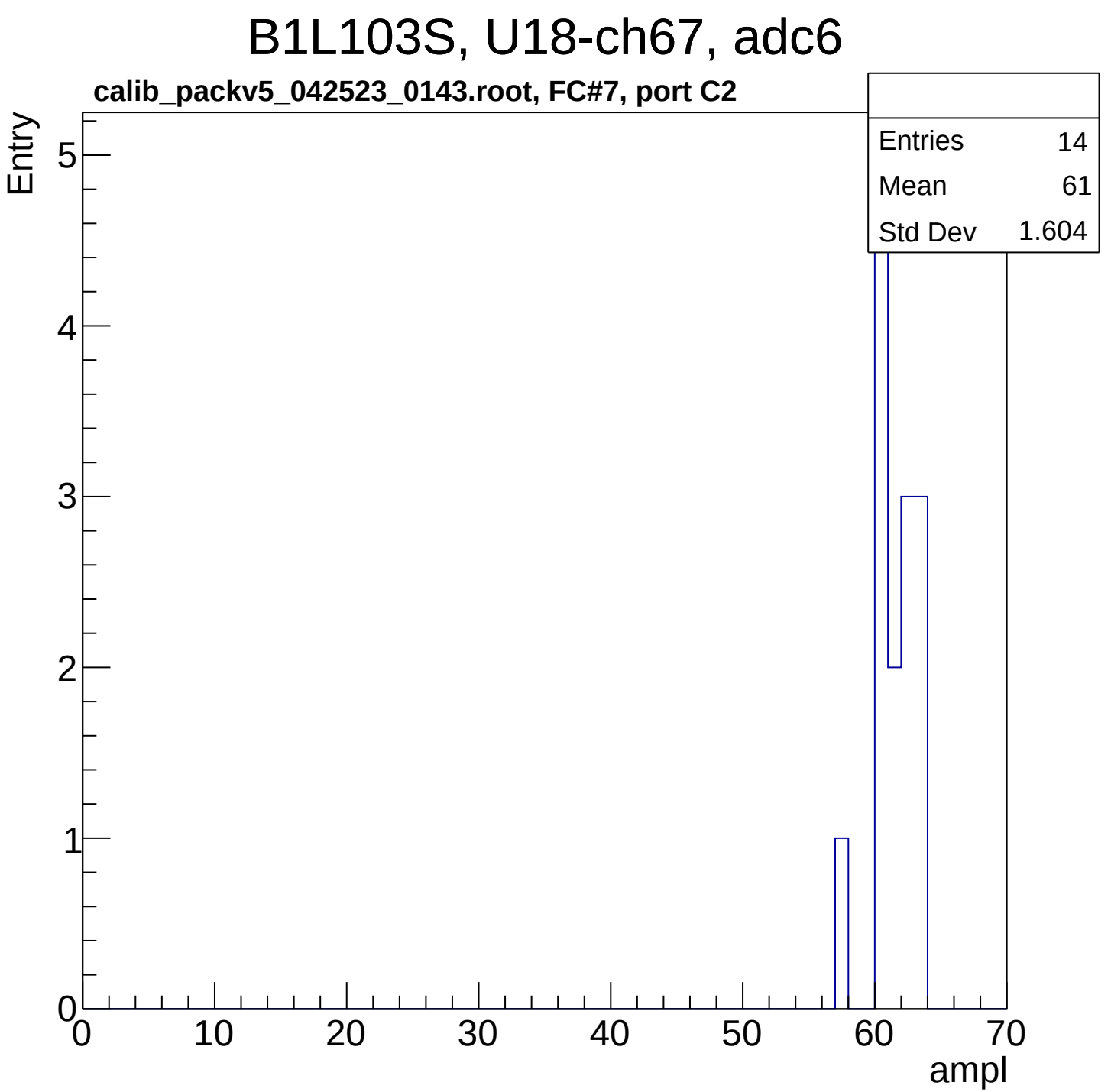
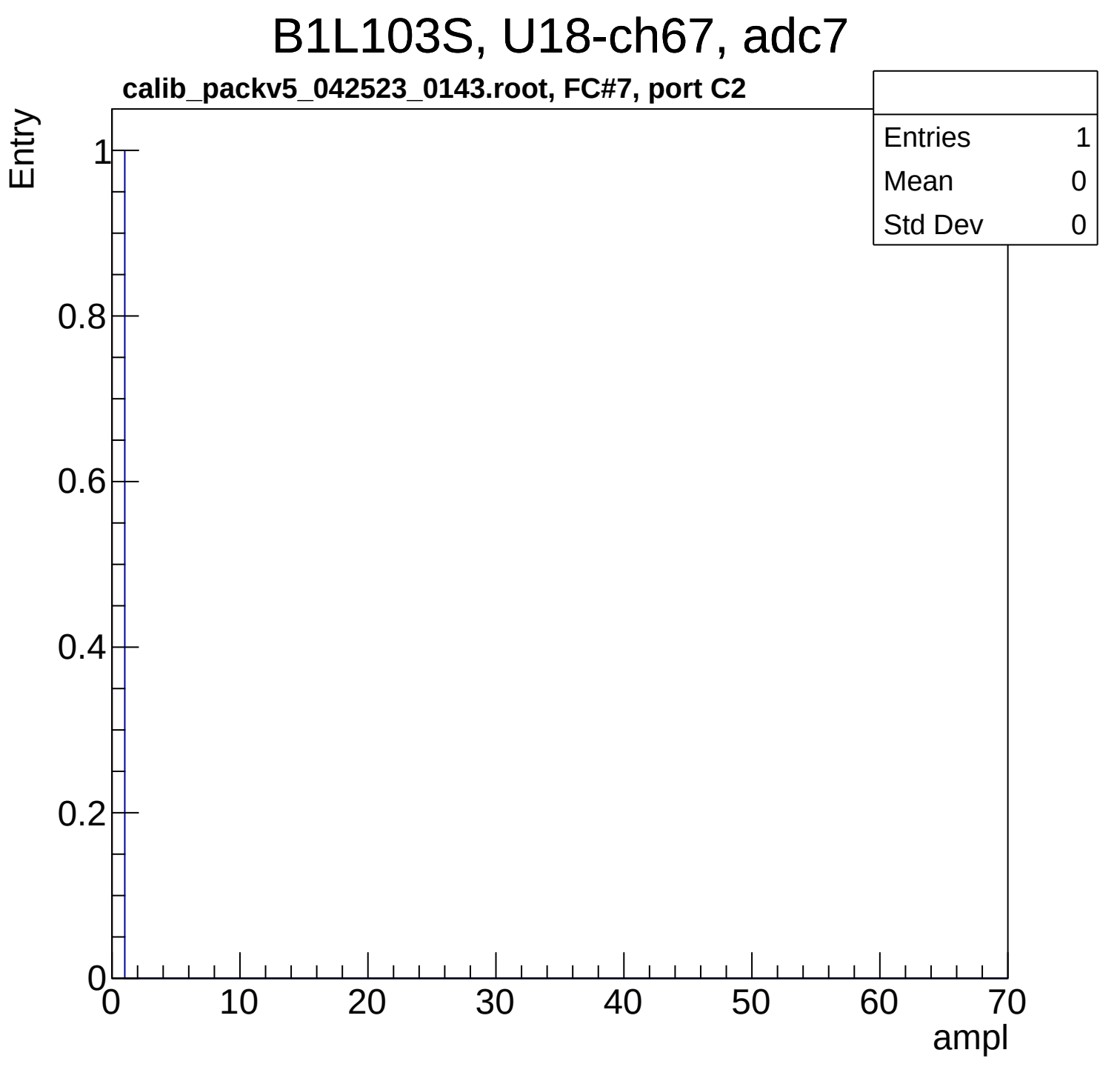
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch67, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 14
Mean 61
Std Dev 1.604
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch67, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
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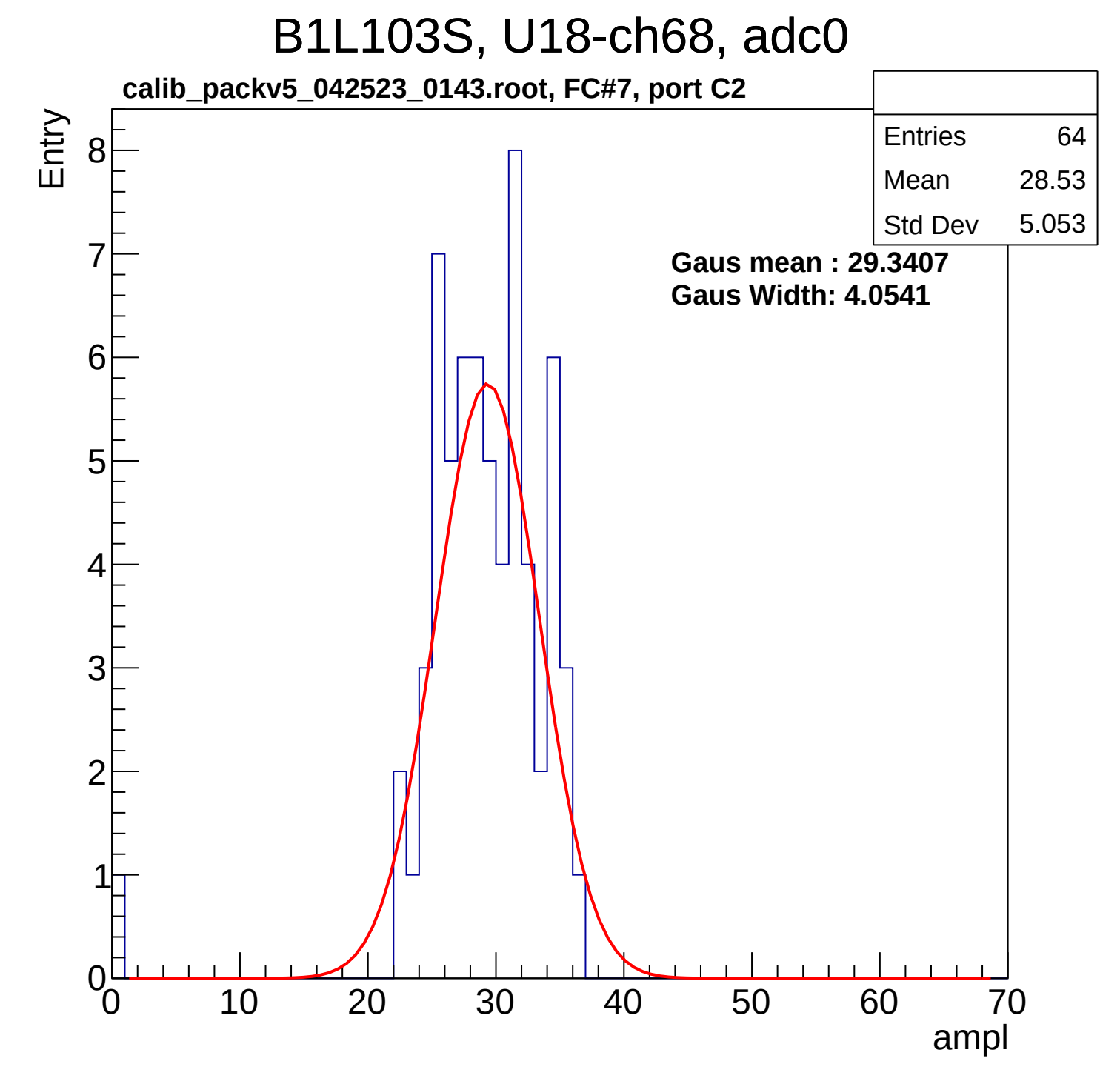
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch68, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 28.53
Std Dev 5.053
Gaus mean : 29.3407
Gaus Width: 4.0541
Entry
ampl
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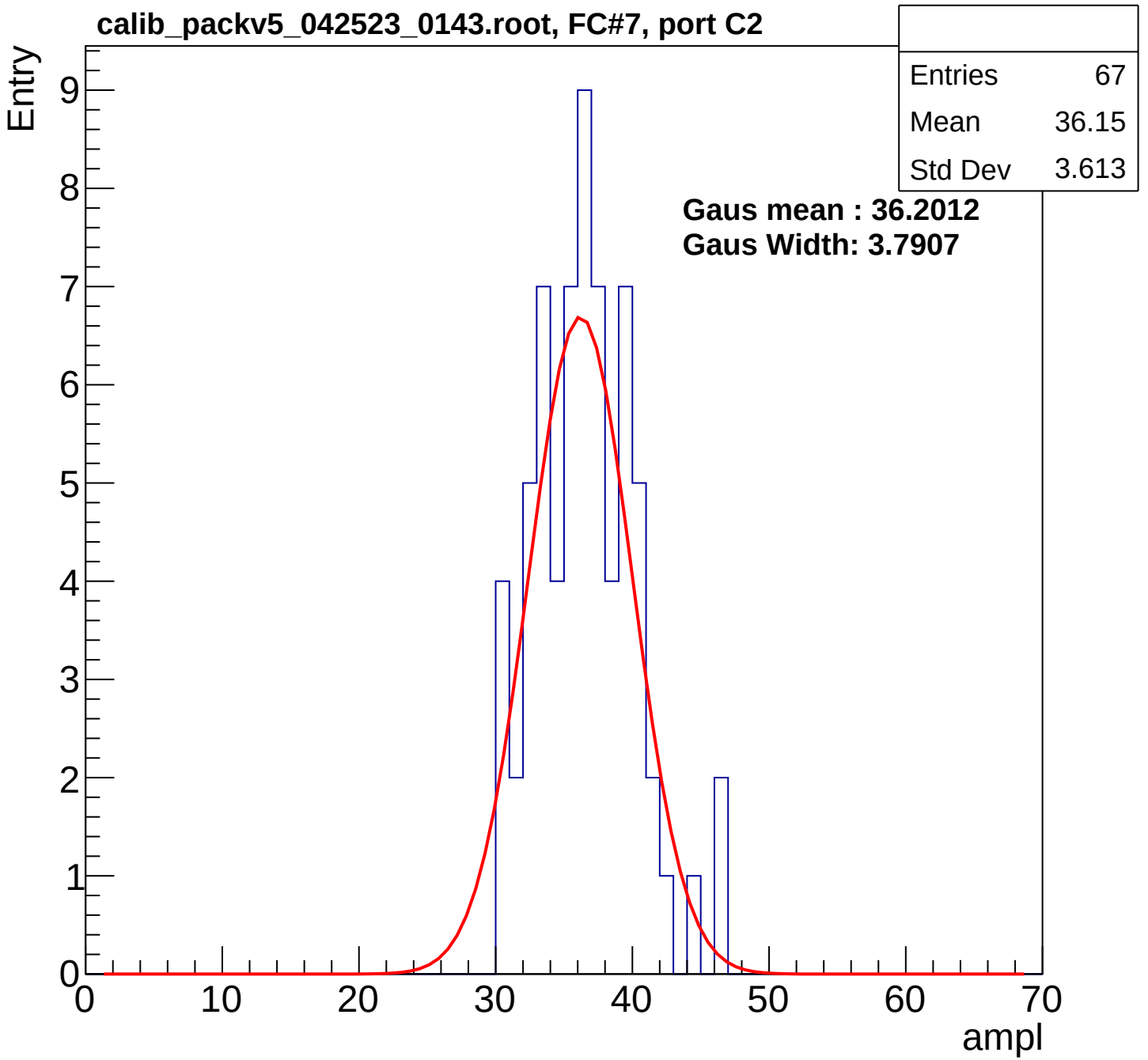
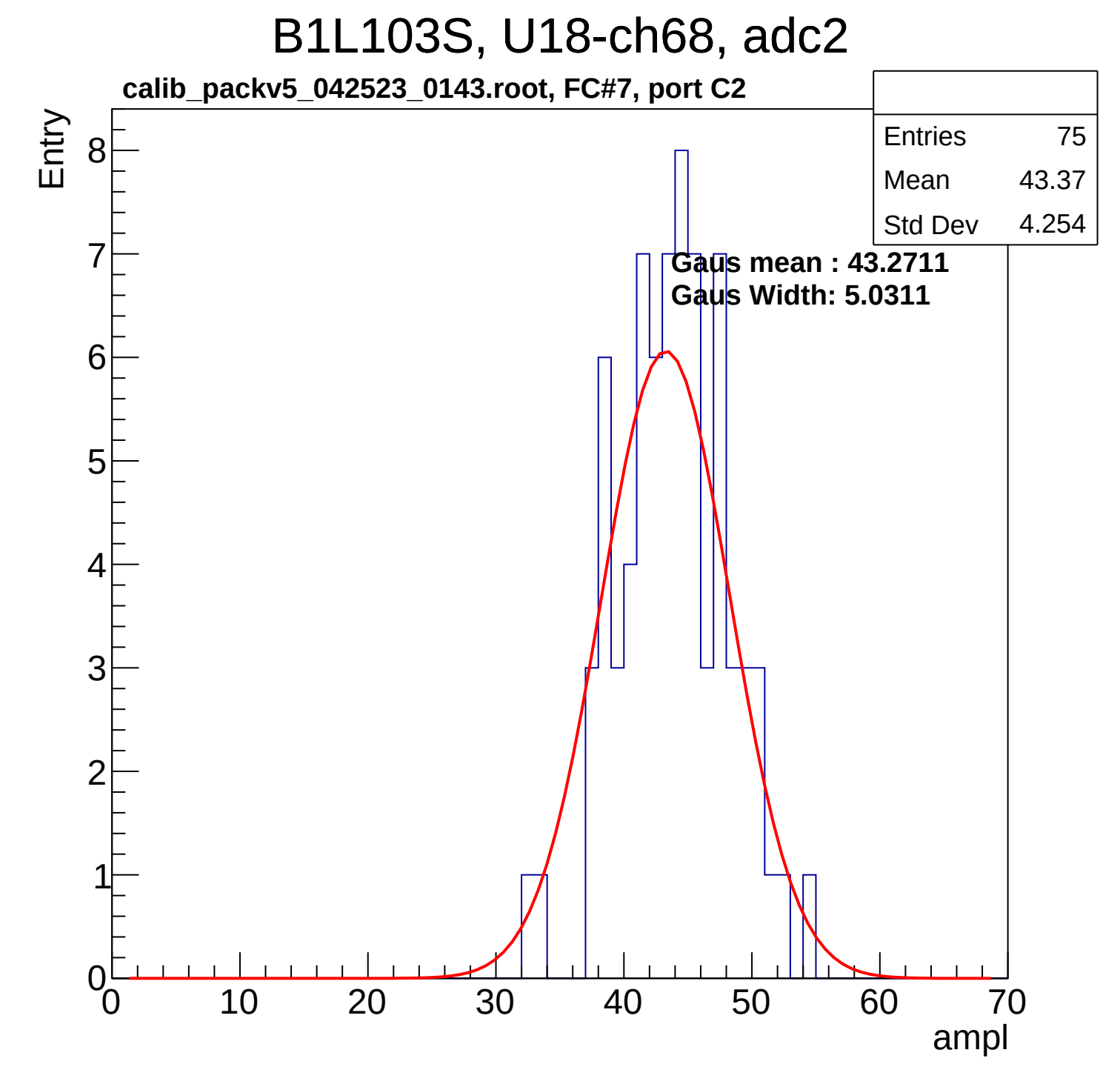
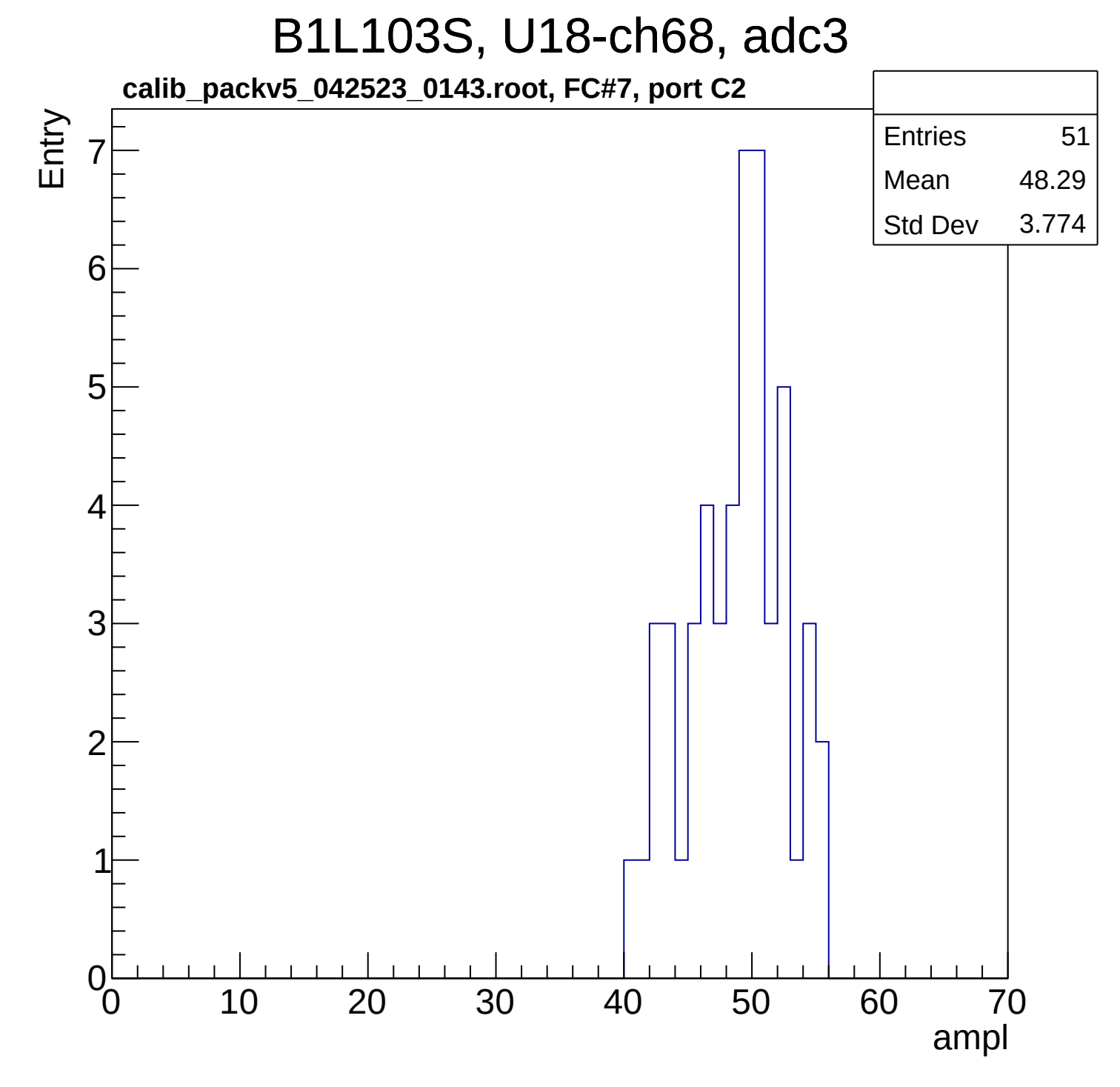
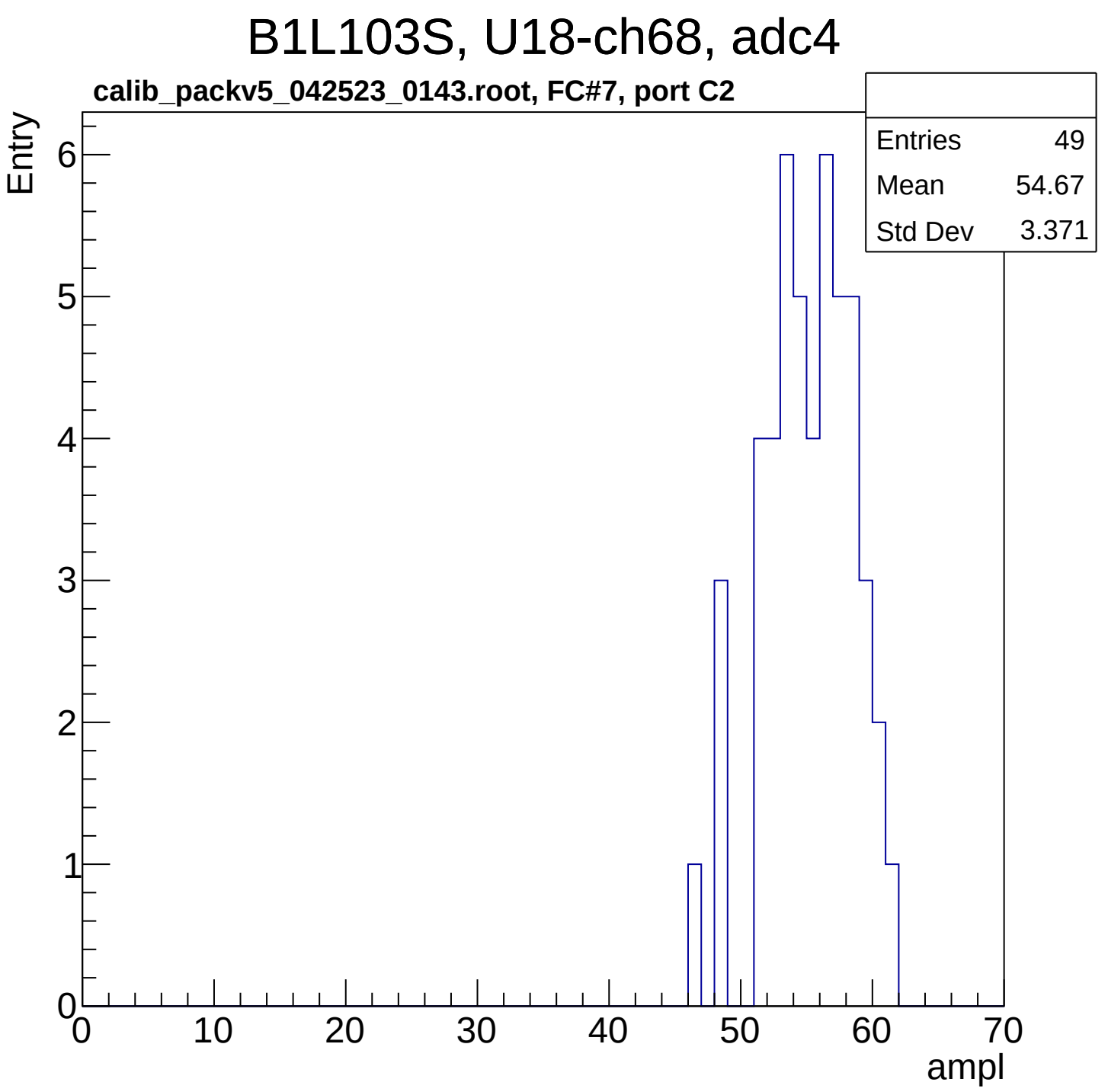
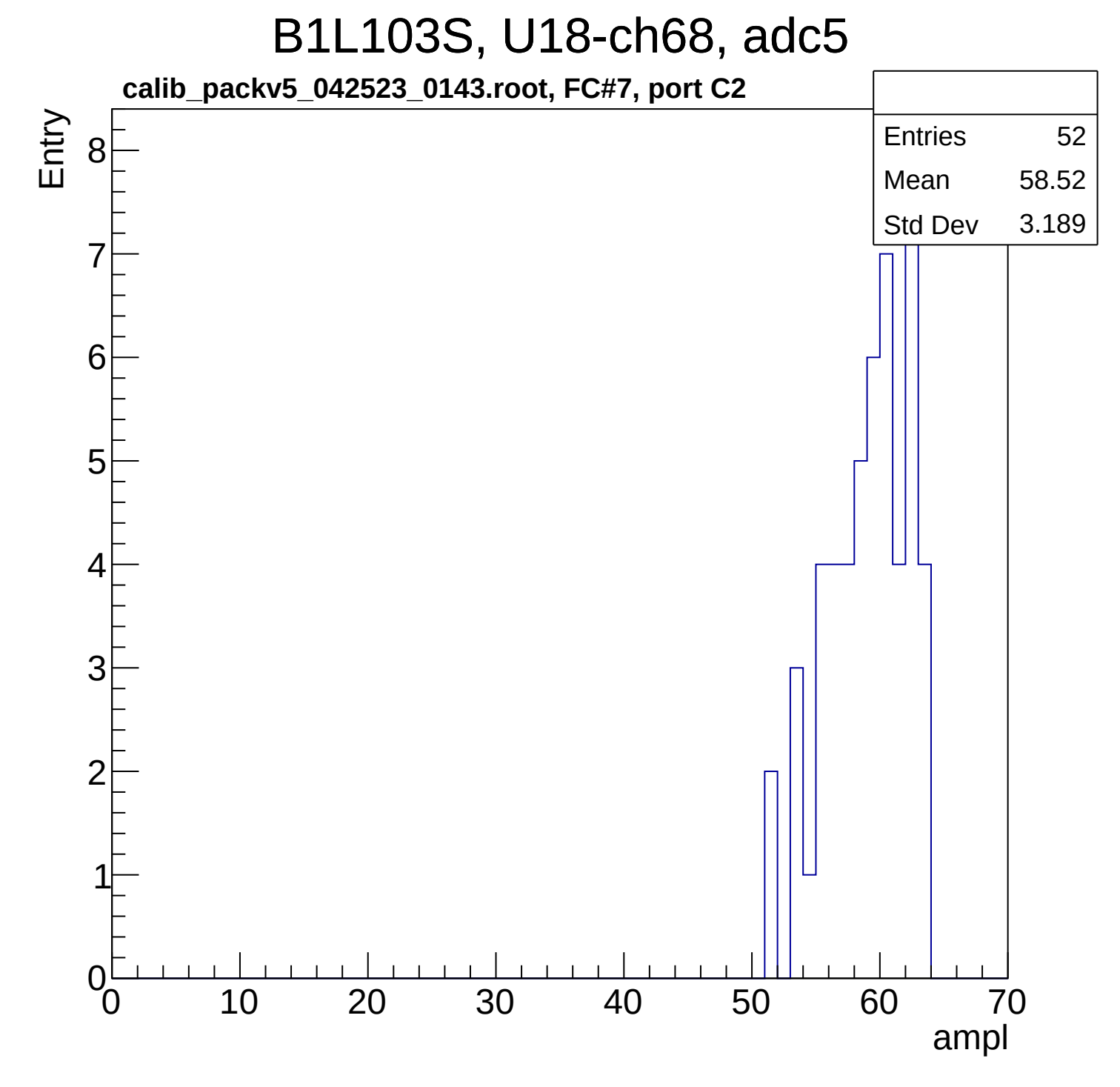
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

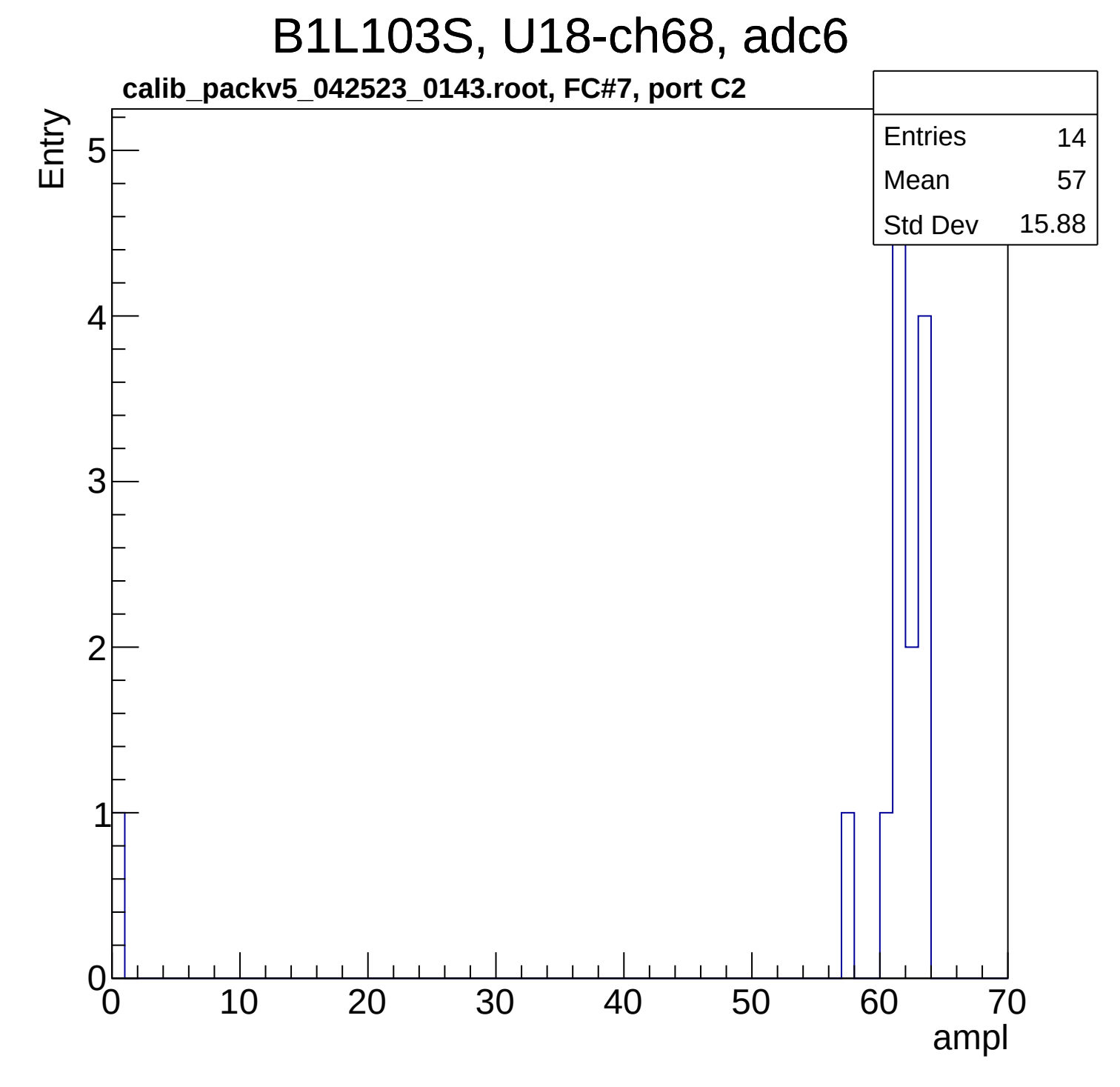

B1L103S, U18-ch68, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 36.15
Std Dev 3.613
Gaus mean : 36.2012
Gaus Width: 3.7907
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

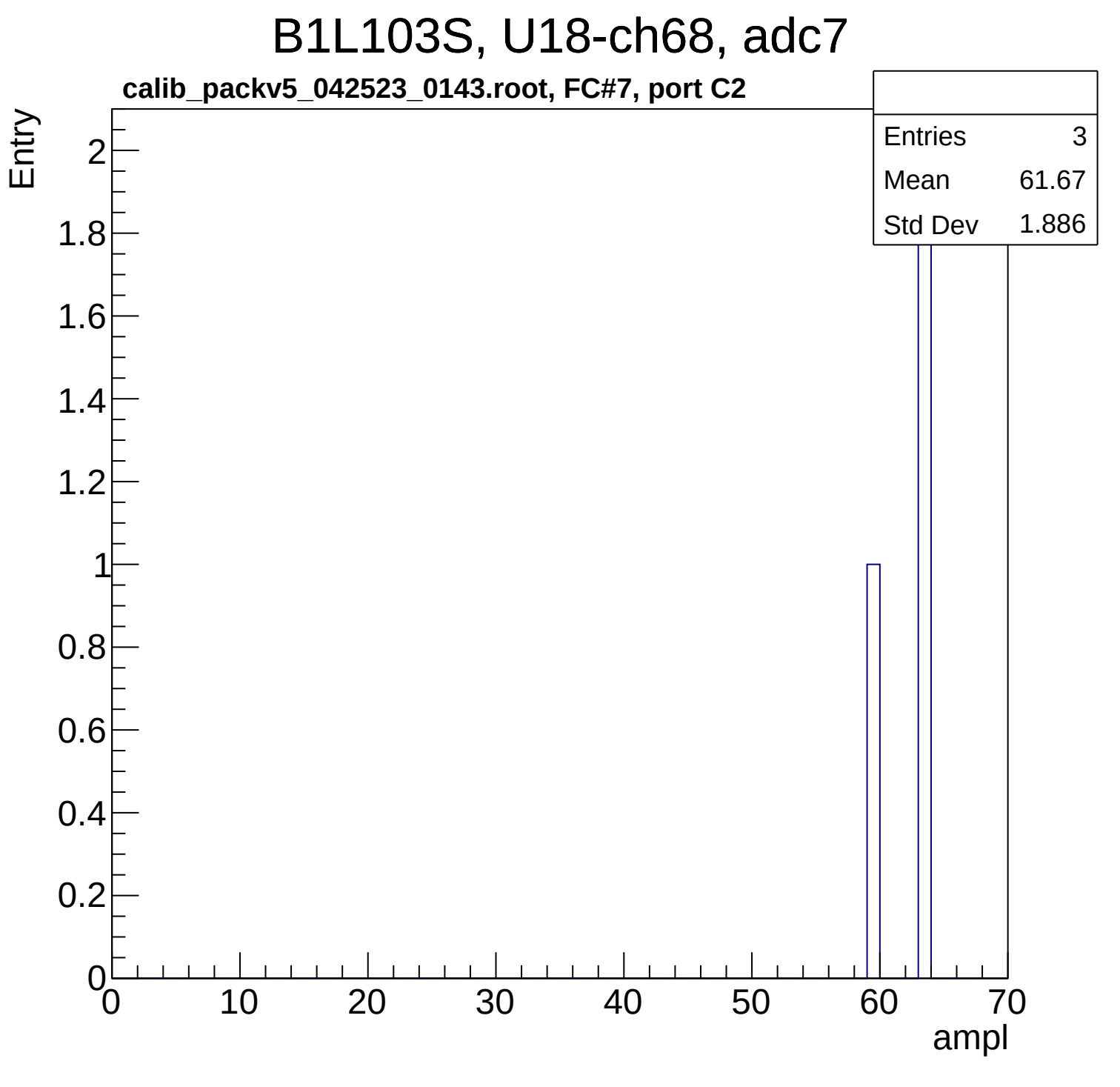

B1L103S, U18-ch68, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 75
Mean 43.37
Std Dev 4.254
Gaus mean : 43.2711
Gaus Width: 5.0311
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch68, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 51
Mean 48.29
Std Dev 3.774
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch68, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 49
Mean 54.67
Std Dev 3.371
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch68, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 52
Mean 58.52
Std Dev 3.189
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch68, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 14
Mean 57
Std Dev 15.88
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch68, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 61.67
Std Dev 1.886
Entry
ampl
0
0.2
0.4
0.6
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1
1.2
1.4
1.6
1.8
2
0
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40
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60
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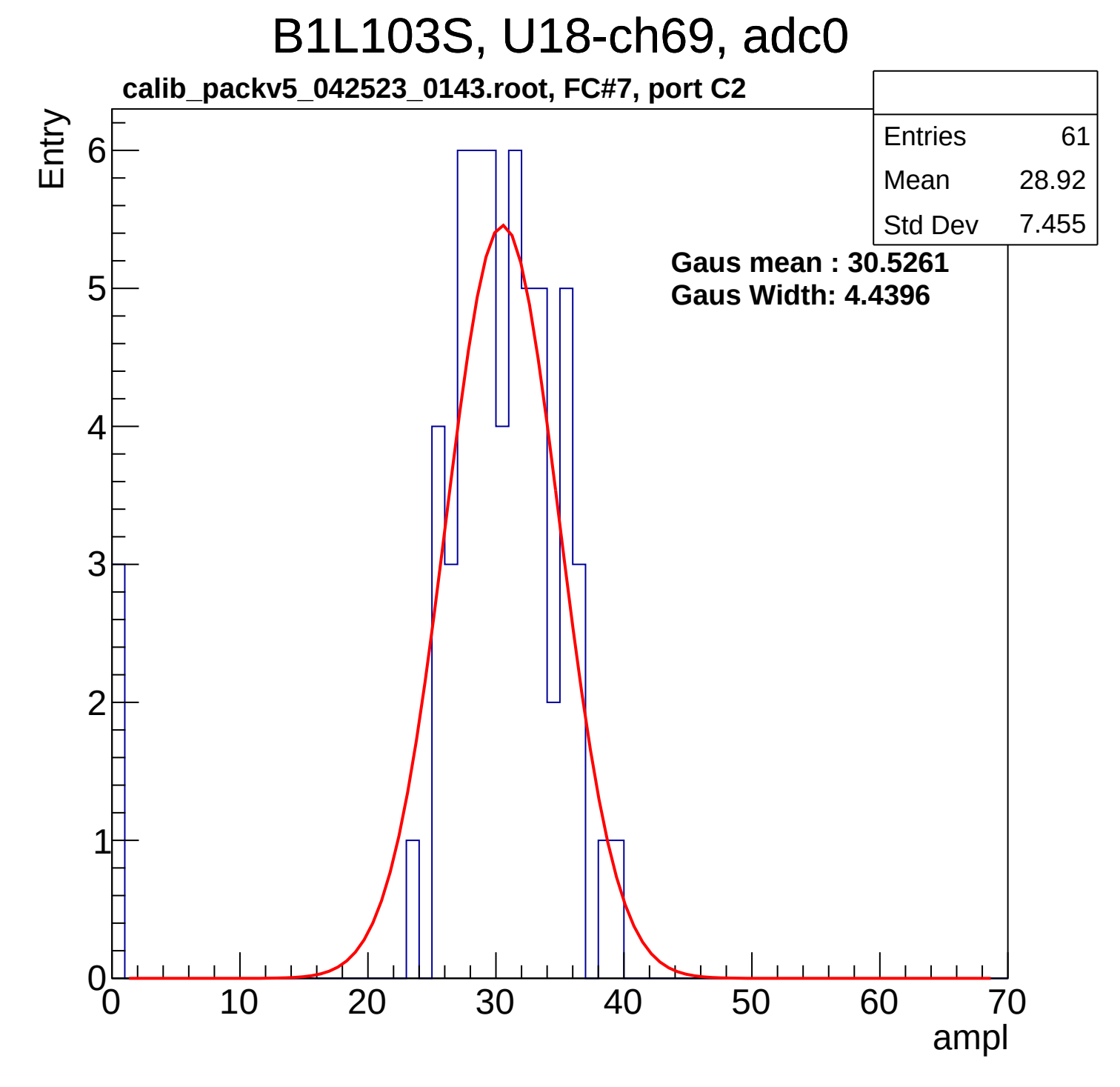
B1L103S, U18-ch69, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 61
Mean 28.92
Std Dev 7.455
Gaus mean : 30.5261
Gaus Width: 4.4396
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
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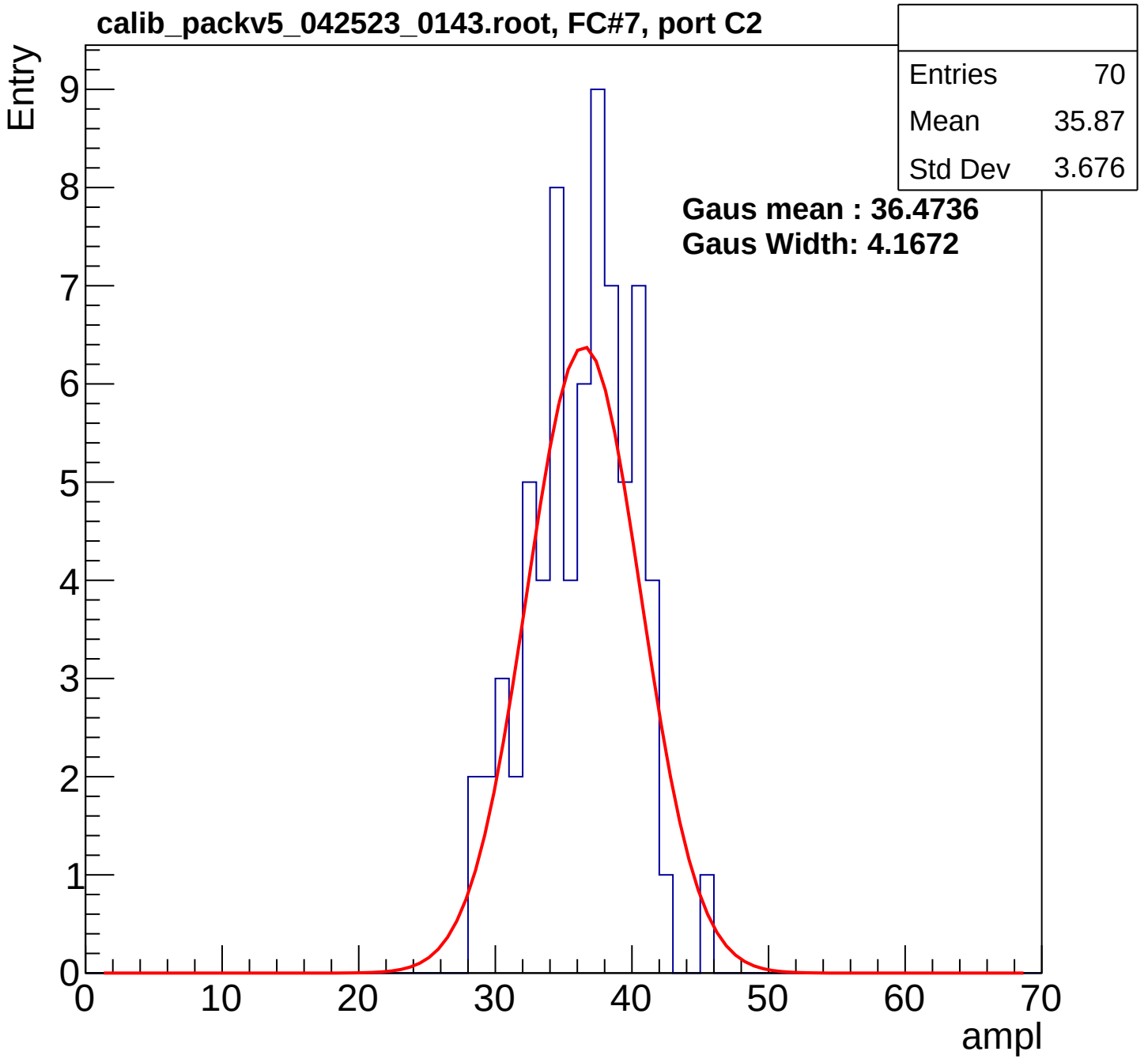
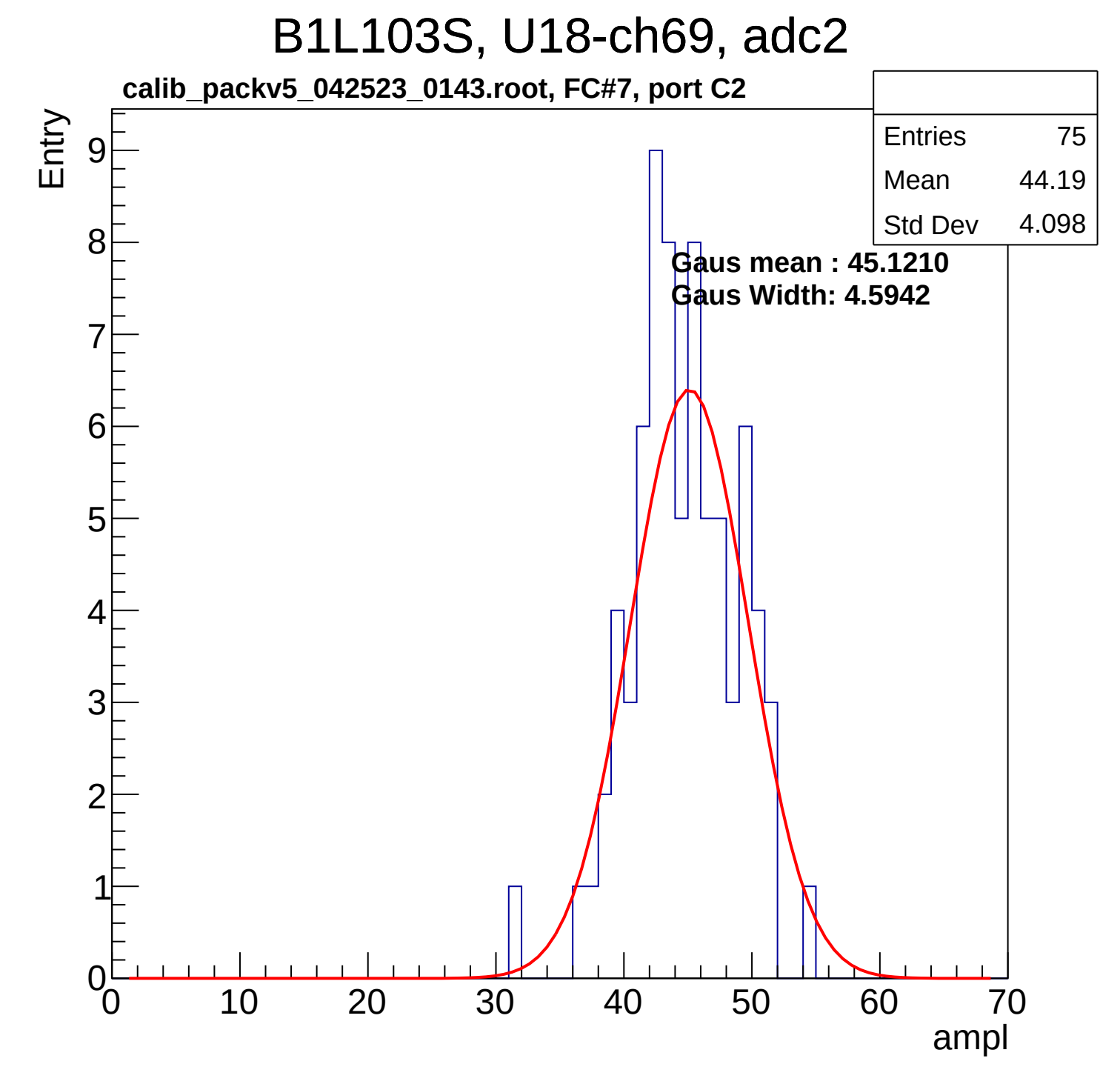

B1L103S, U18-ch69, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 35.87
Std Dev 3.676
Gaus mean : 36.4736
Gaus Width: 4.1672
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch69, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 75
Mean 44.19
Std Dev 4.098
Gaus mean : 45.1210
Gaus Width: 4.5942
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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20
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40
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60
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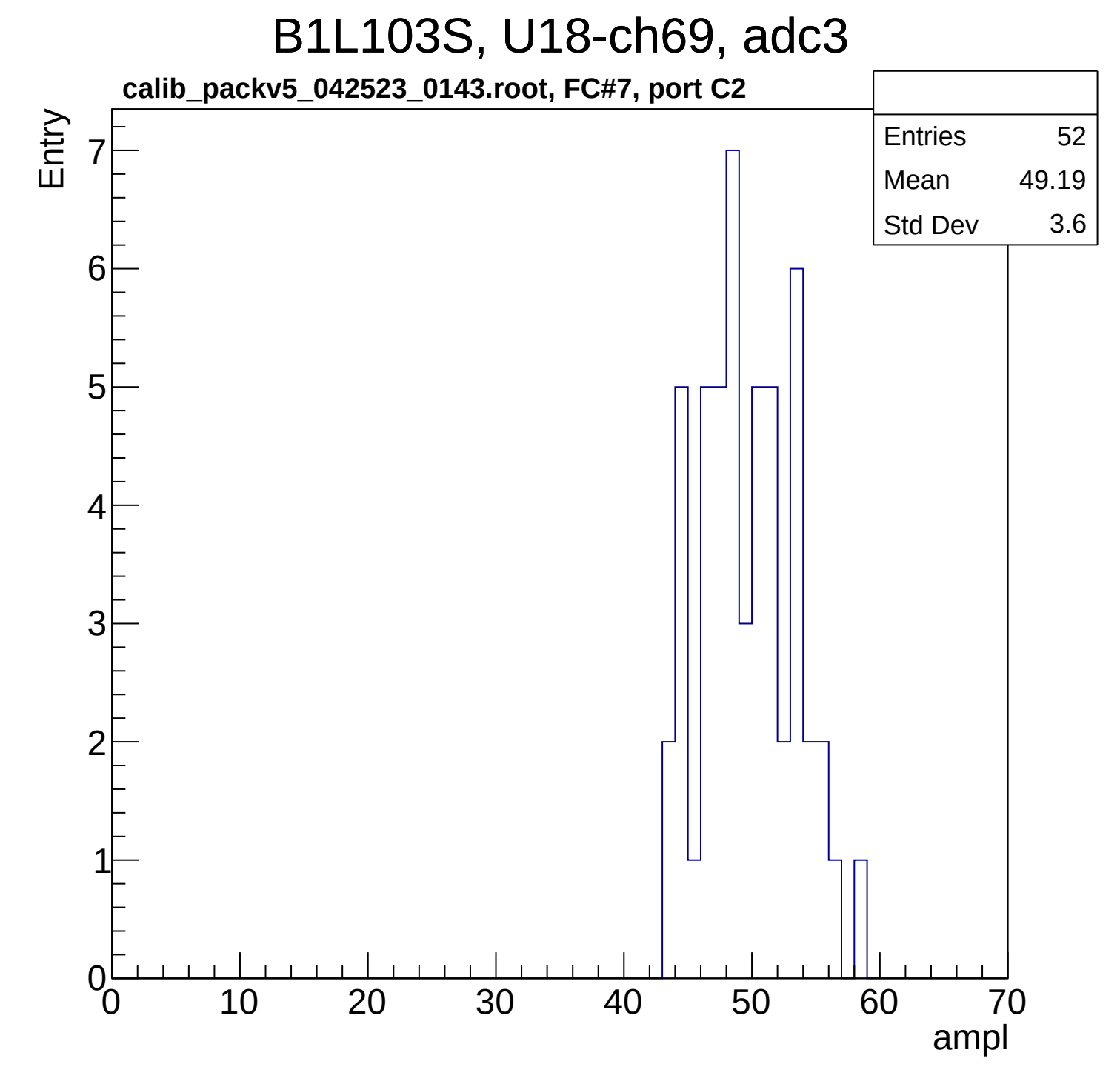
B1L103S, U18-ch69, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 52
Mean 49.19
Std Dev 3.6
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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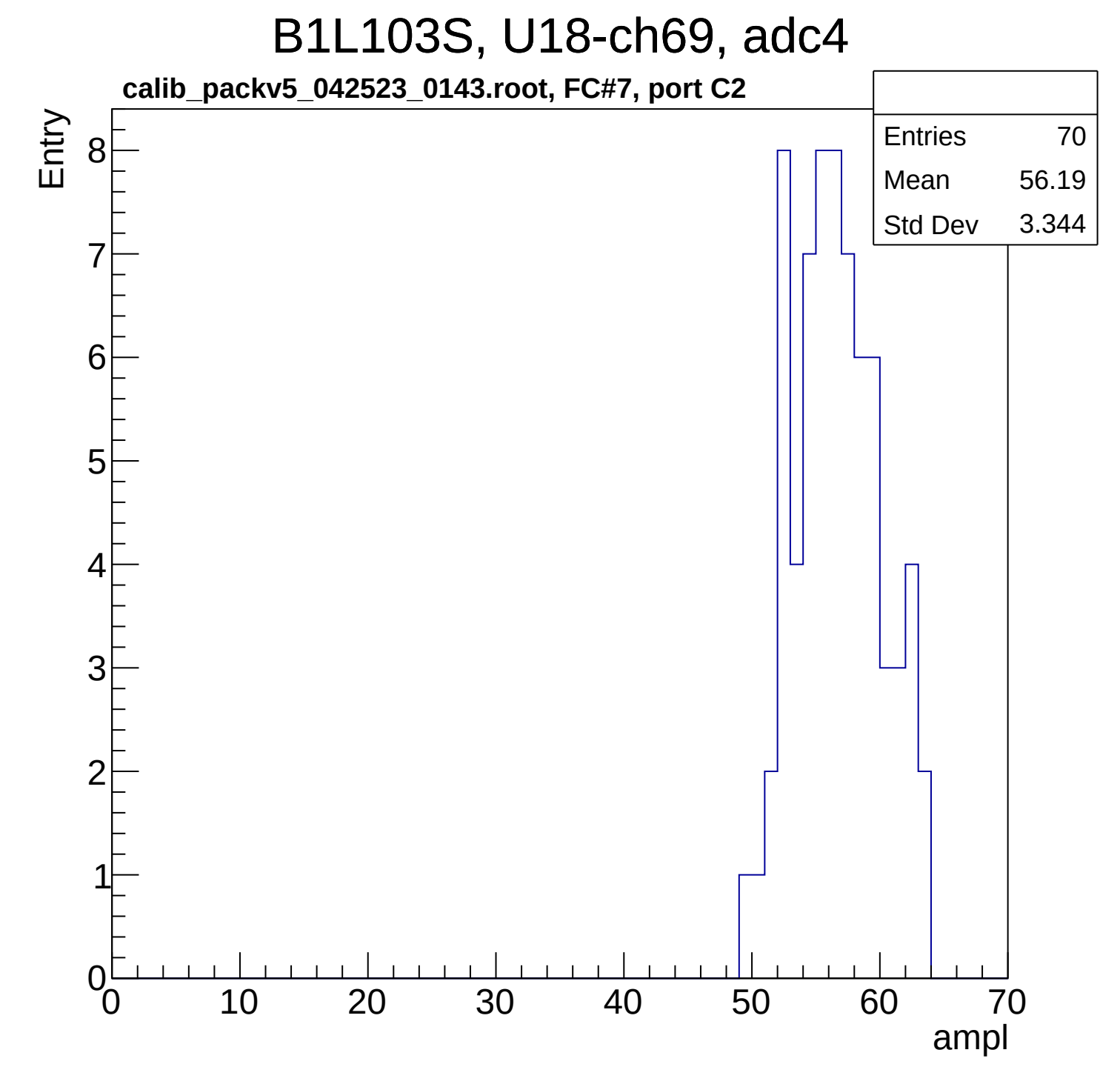
B1L103S, U18-ch69, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 56.19
Std Dev 3.344
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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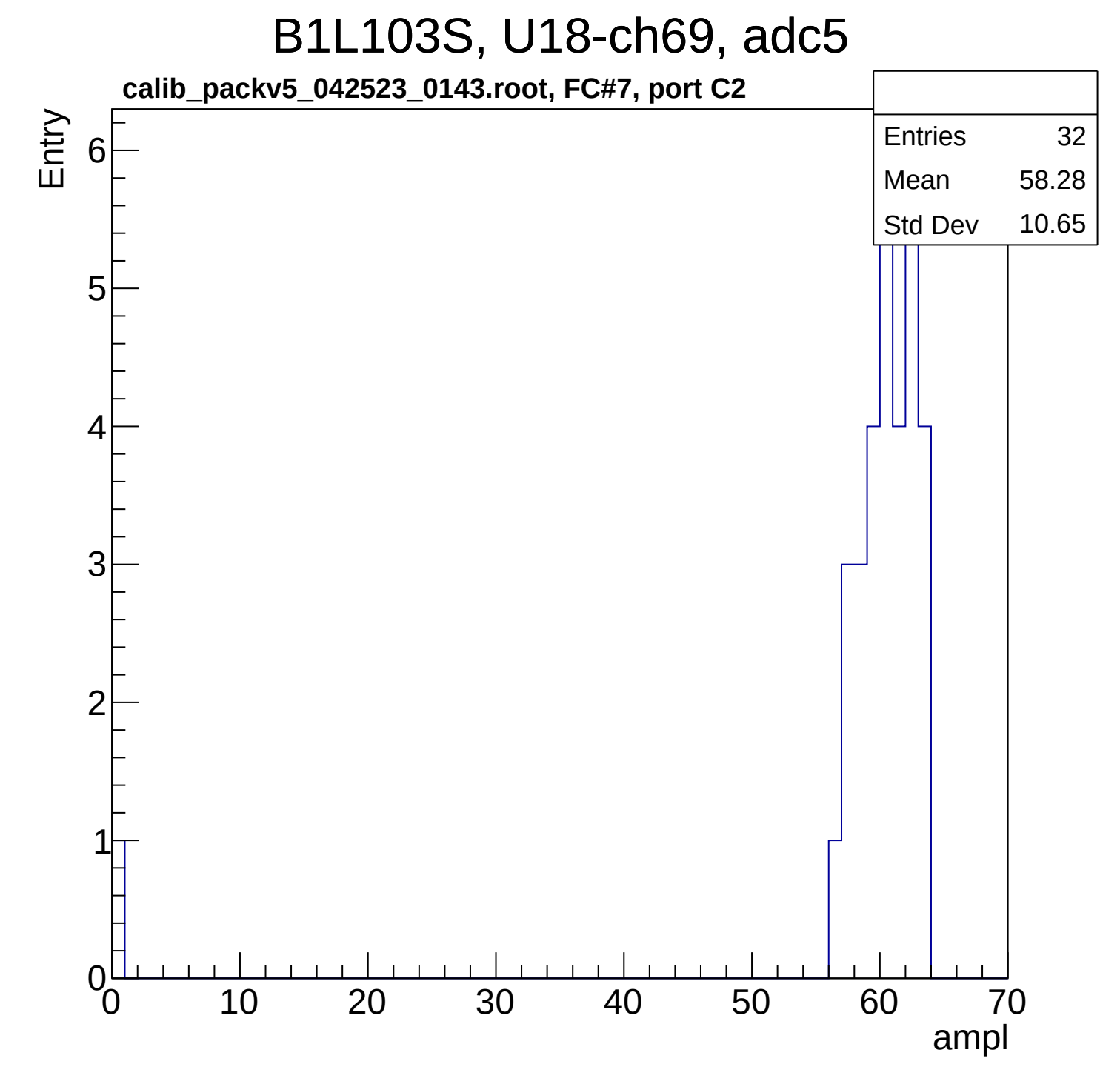
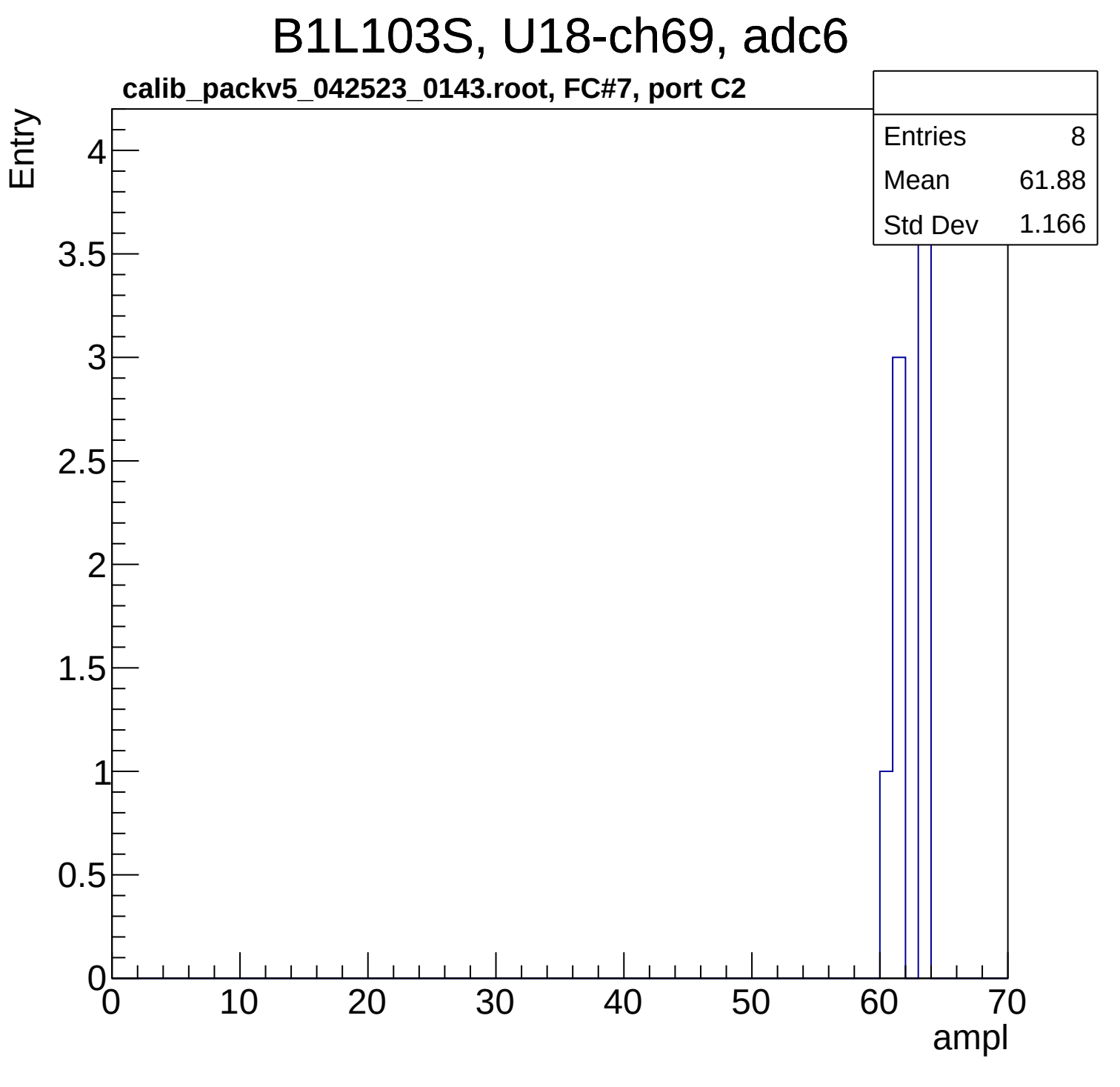

B1L103S, U18-ch69, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 32
Mean 58.28
Std Dev 10.65
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch69, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 8
Mean 61.88
Std Dev 1.166
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
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60
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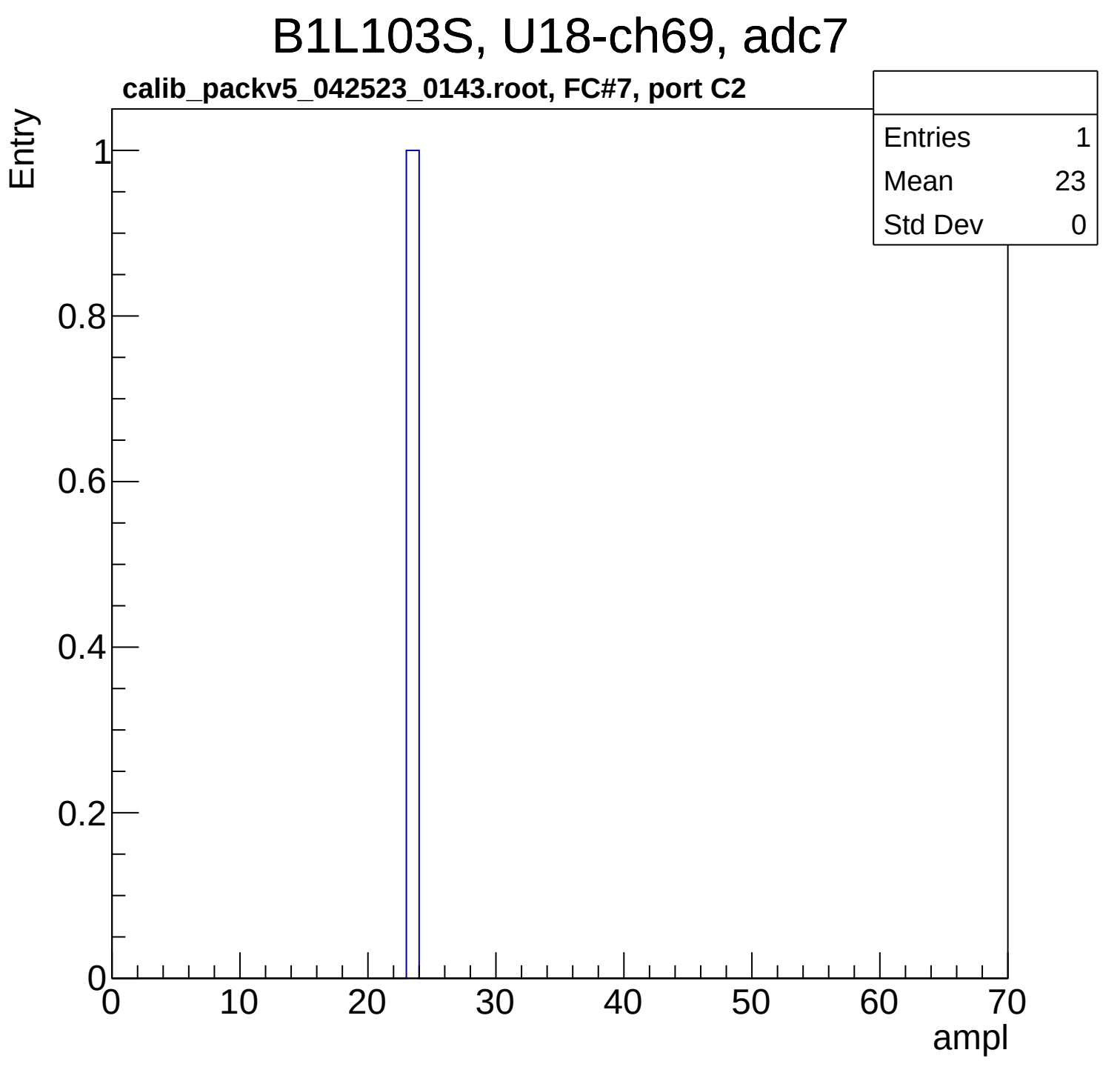
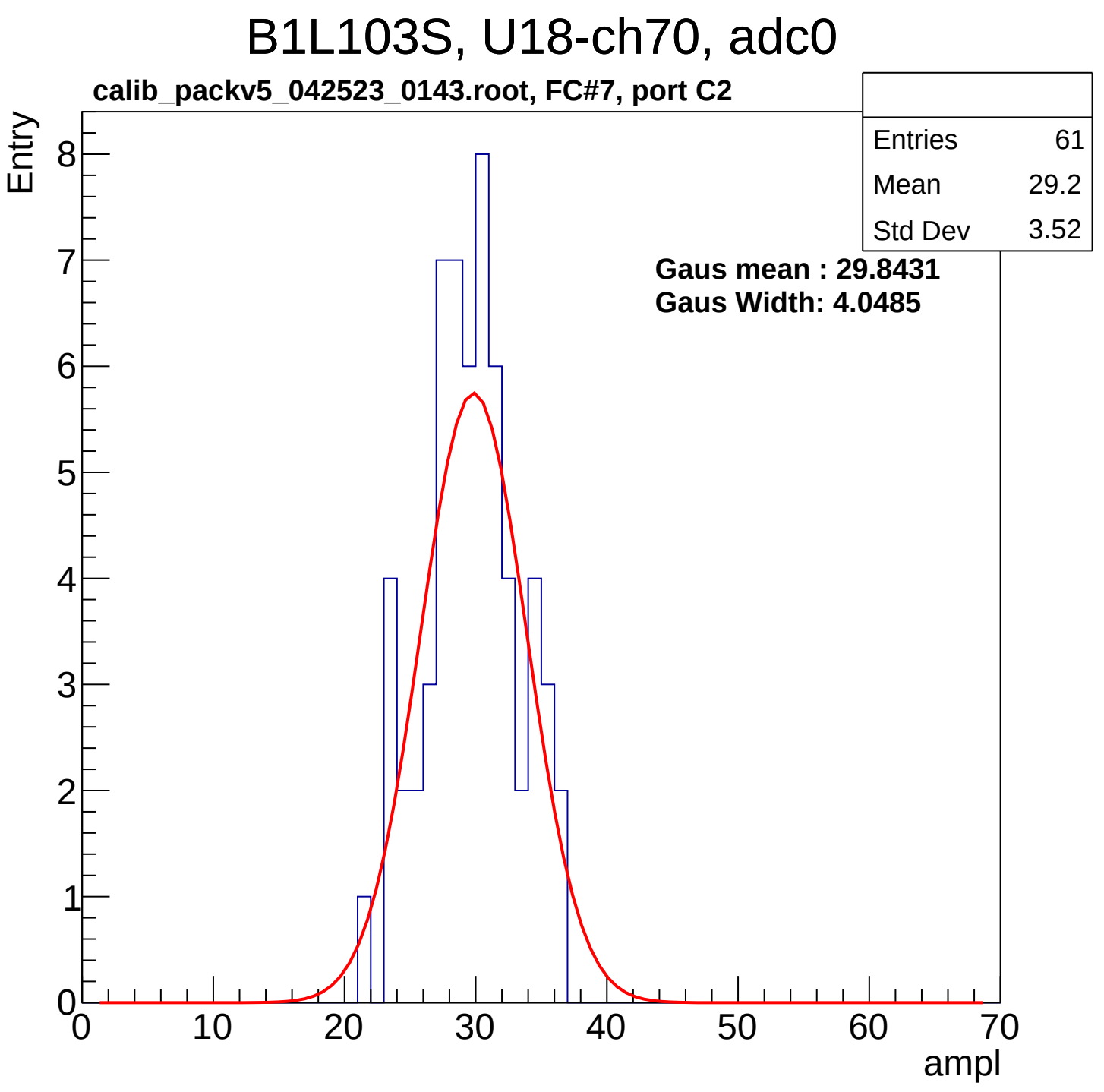
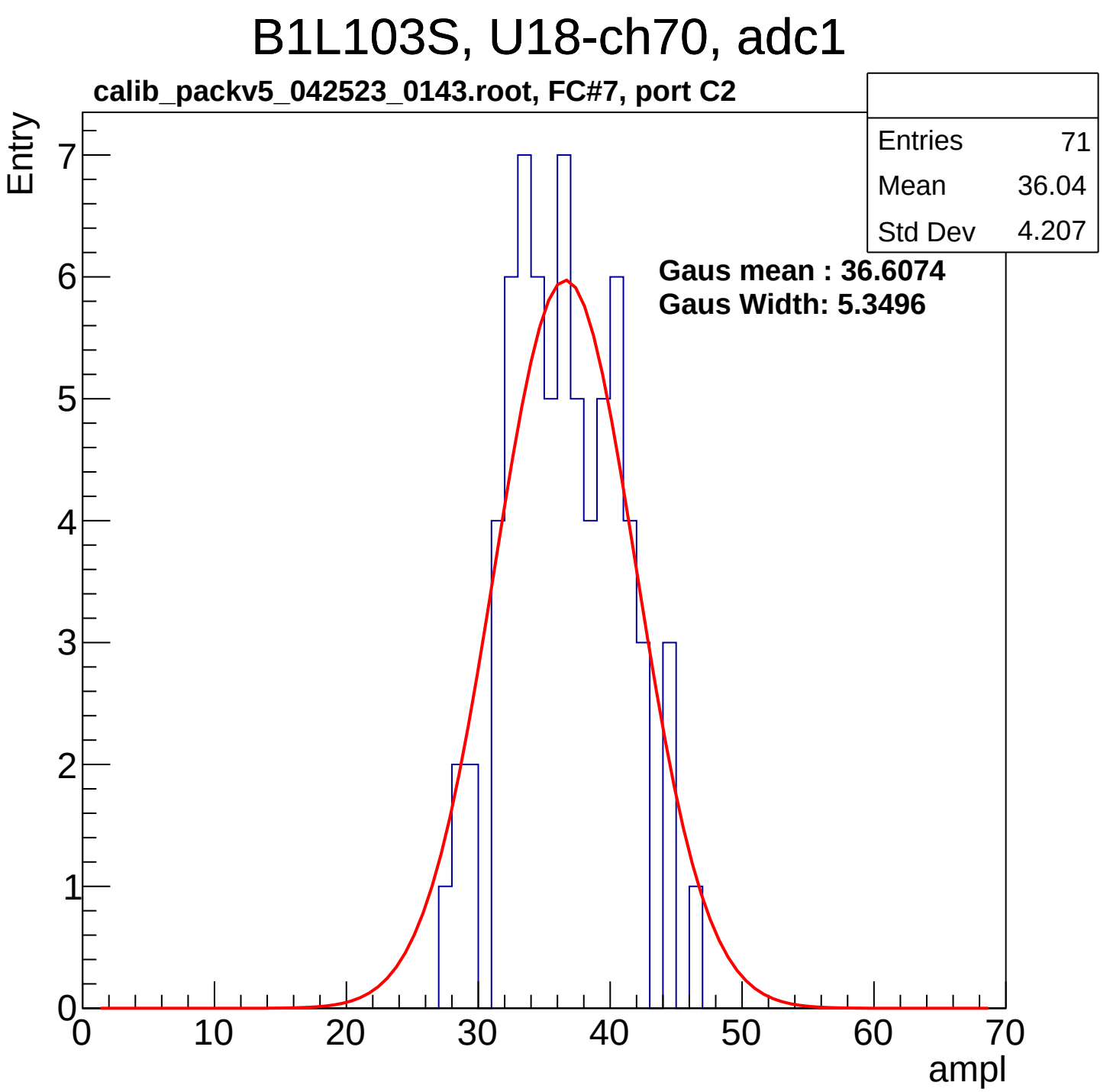

B1L103S, U18-ch69, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 23
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch70, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 61
Mean 29.2
Std Dev 3.52
Gaus mean : 29.8431
Gaus Width: 4.0485
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch70, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 71
Mean 36.04
Std Dev 4.207
Gaus mean : 36.6074
Gaus Width: 5.3496
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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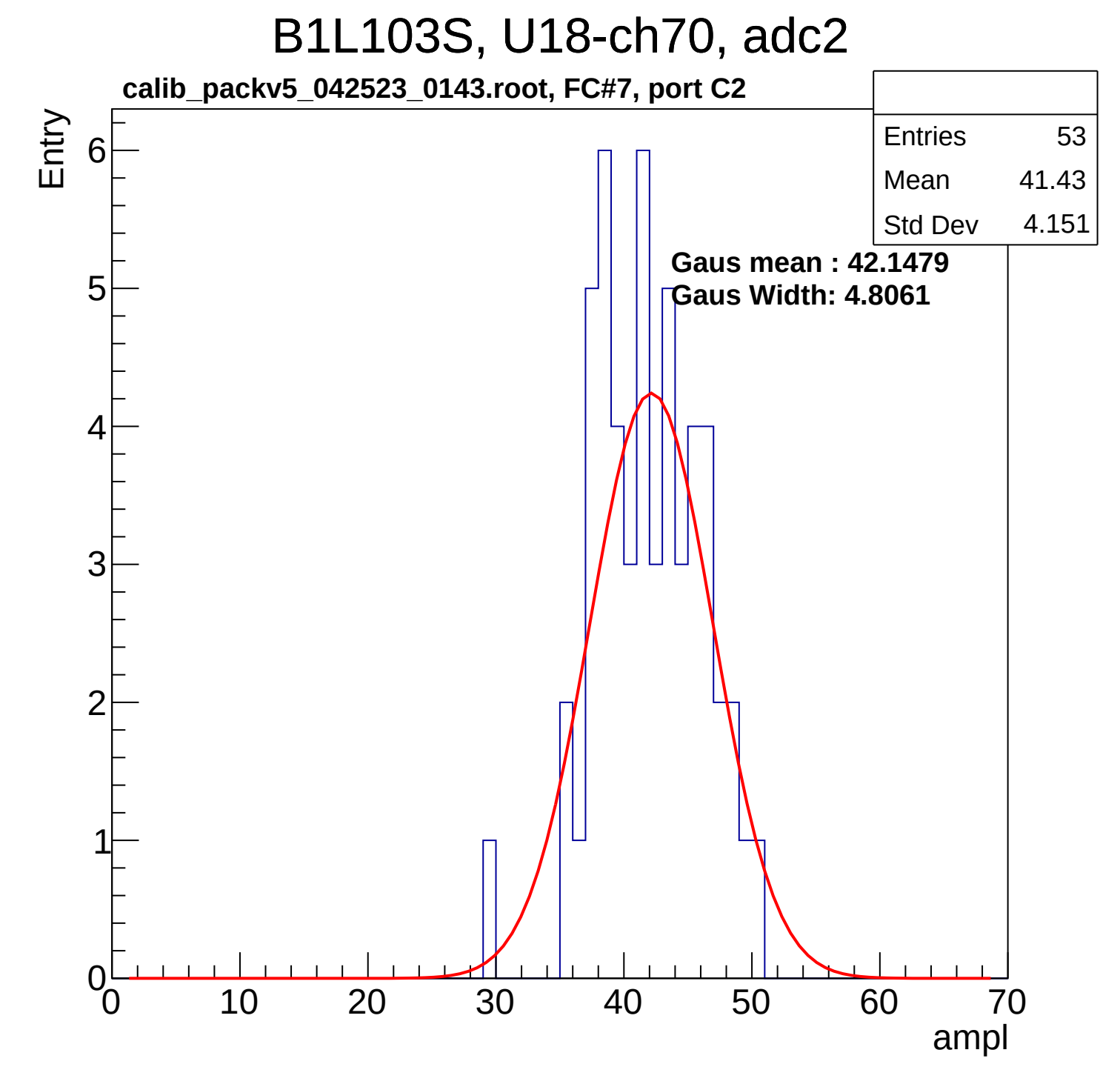
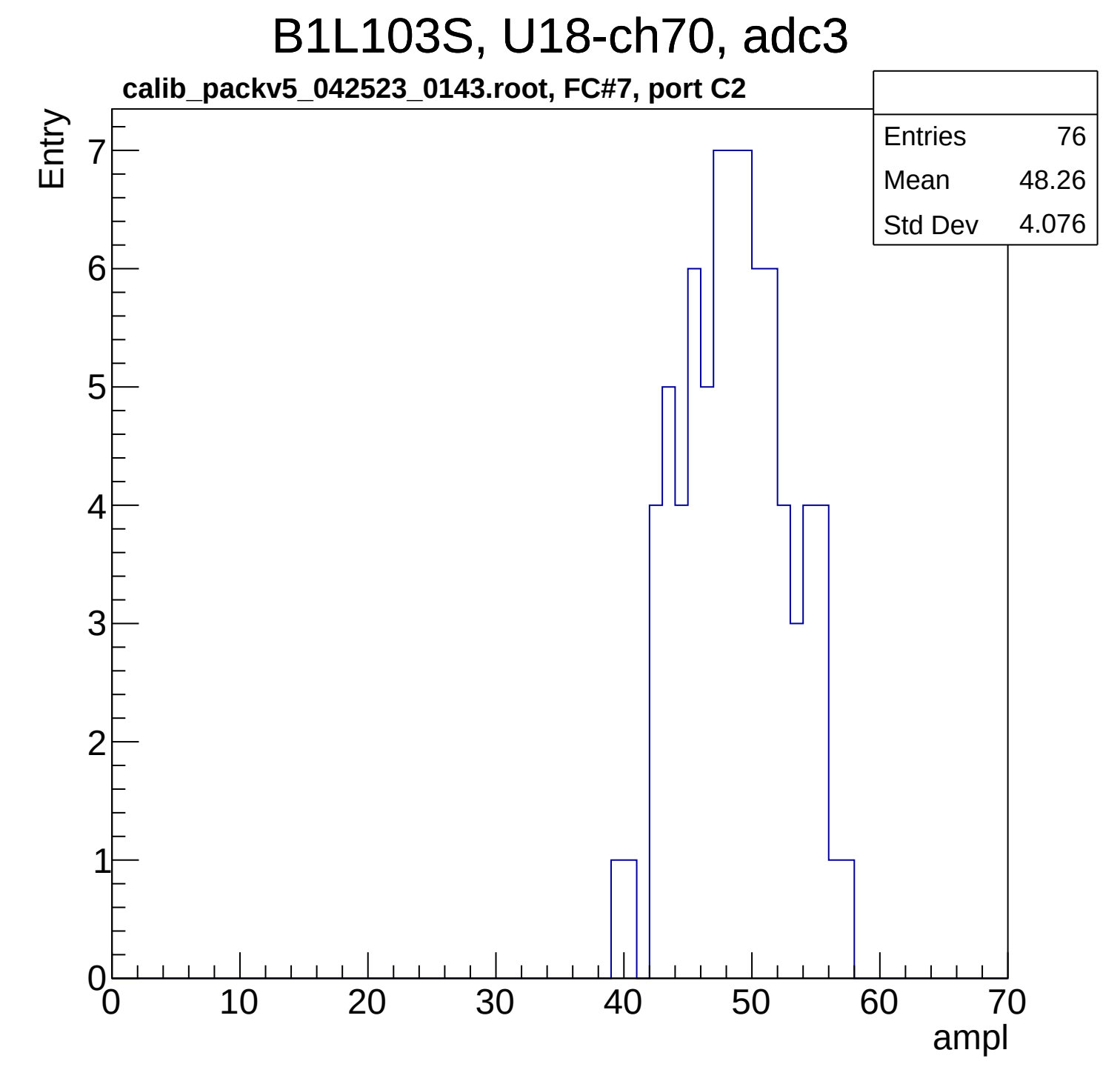
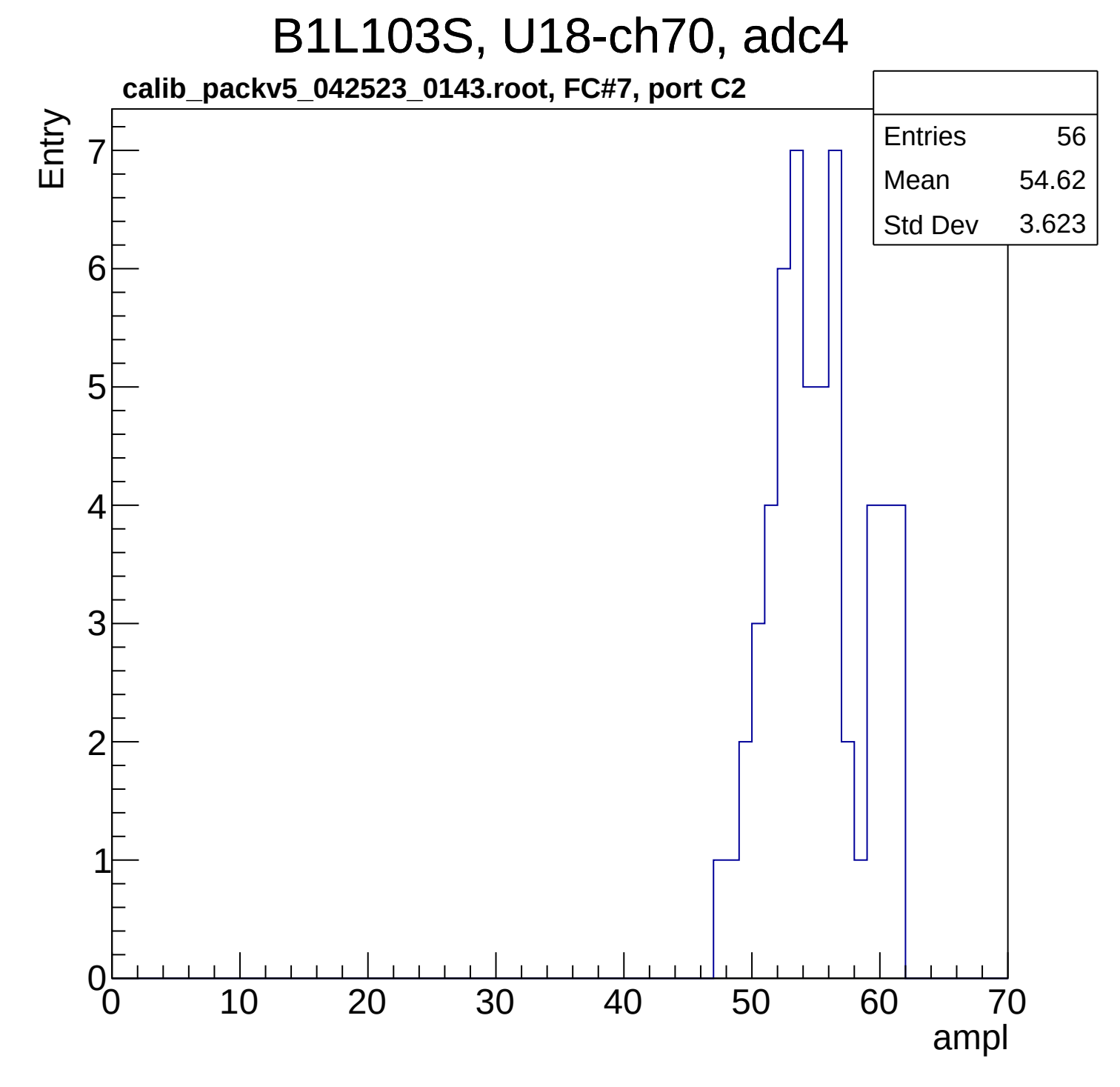

B1L103S, U18-ch70, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 41.43
Std Dev 4.151
Gaus mean : 42.1479
Gaus Width: 4.8061
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U18-ch70, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 76
Mean 48.26
Std Dev 4.076
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch70, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 54.62
Std Dev 3.623
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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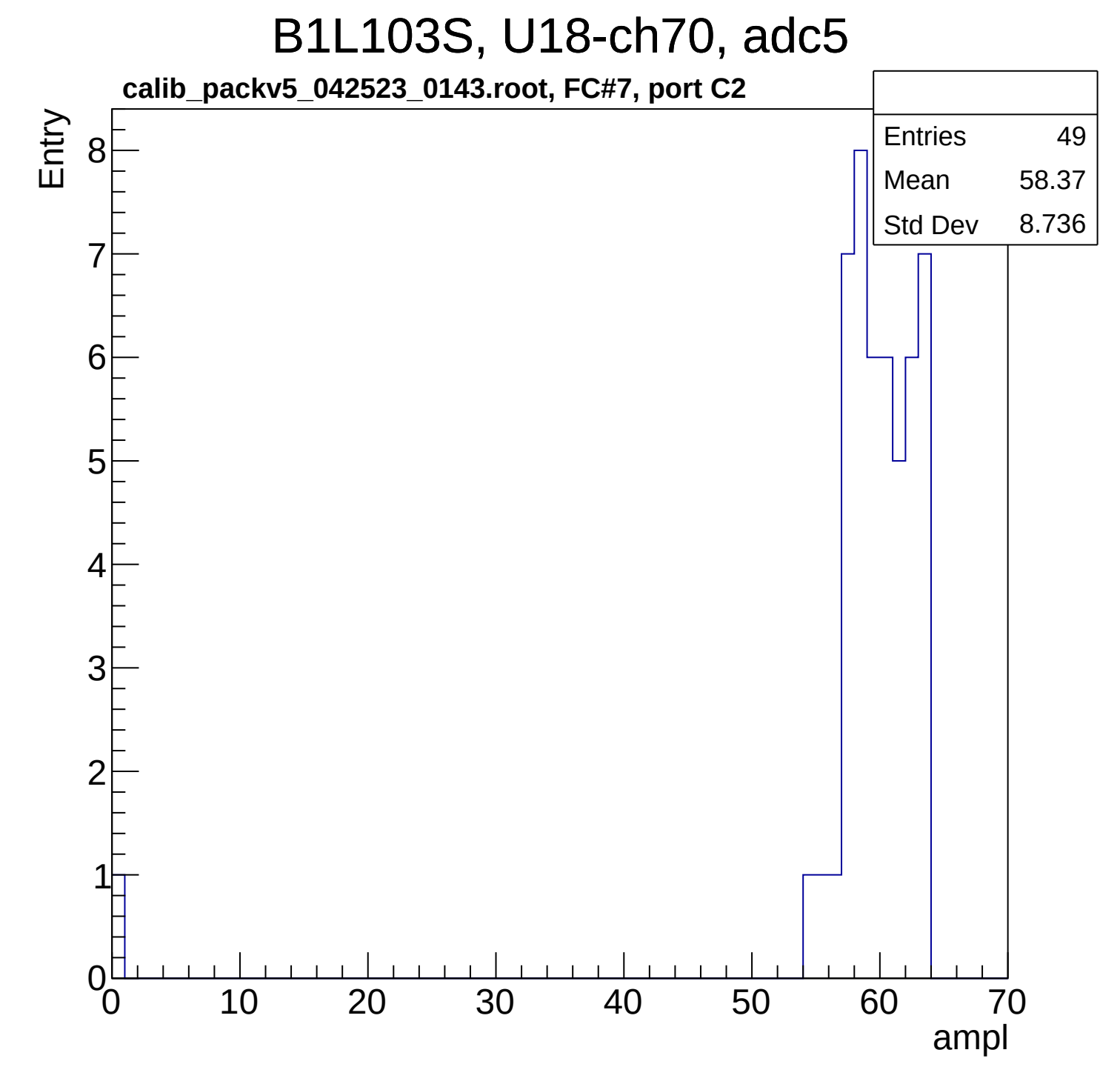
B1L103S, U18-ch70, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 49
Mean 58.37
Std Dev 8.736
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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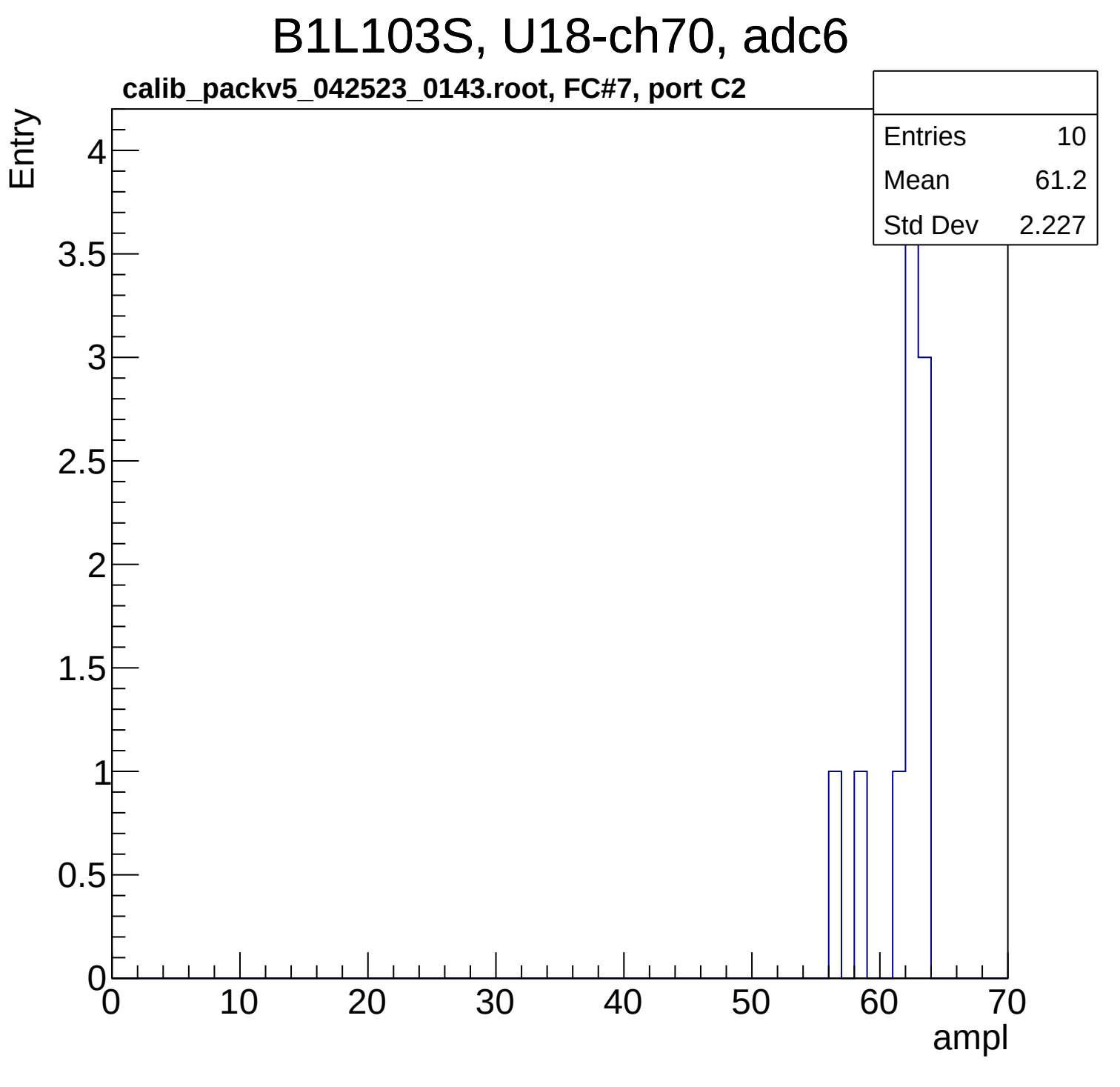
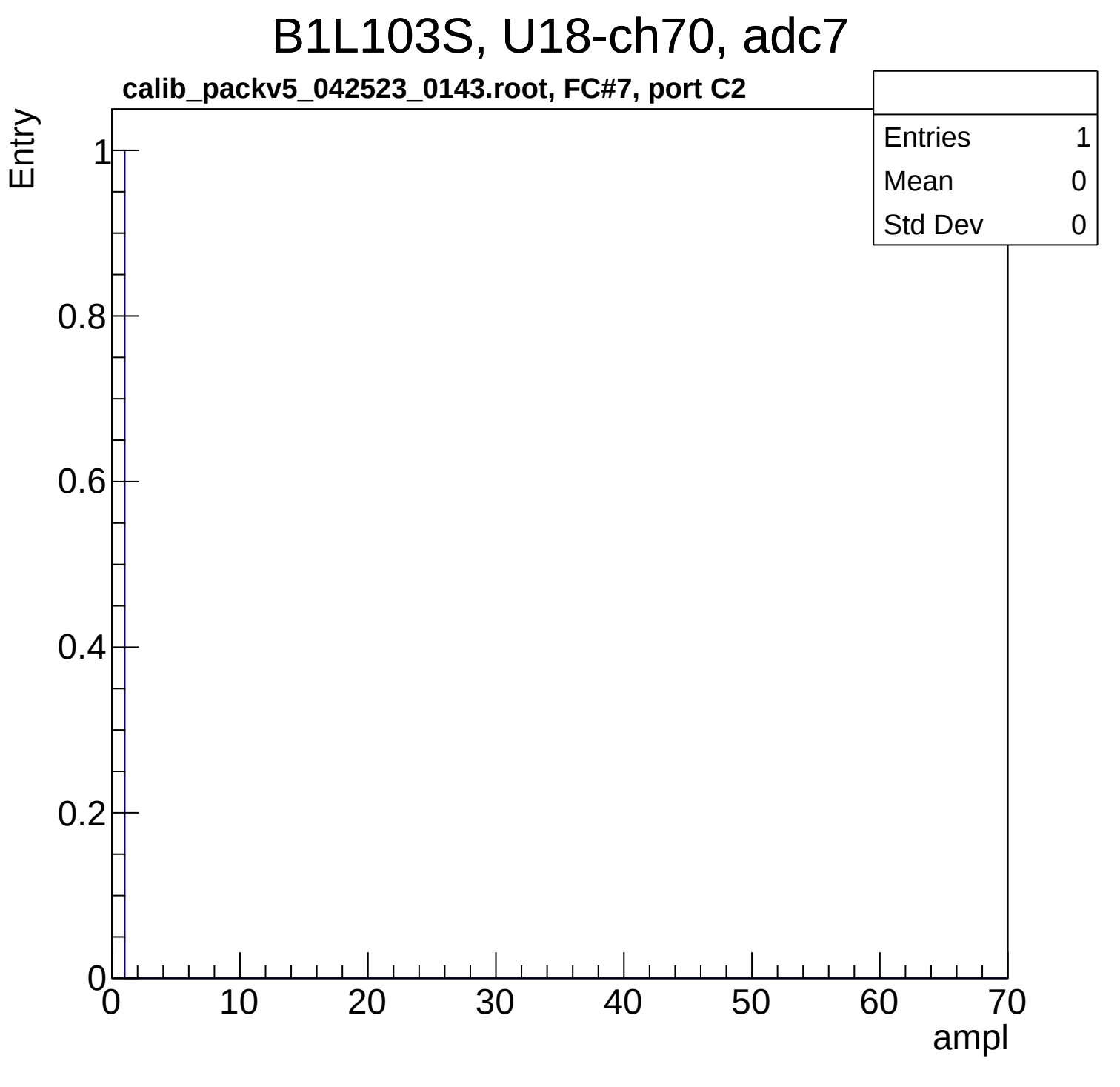
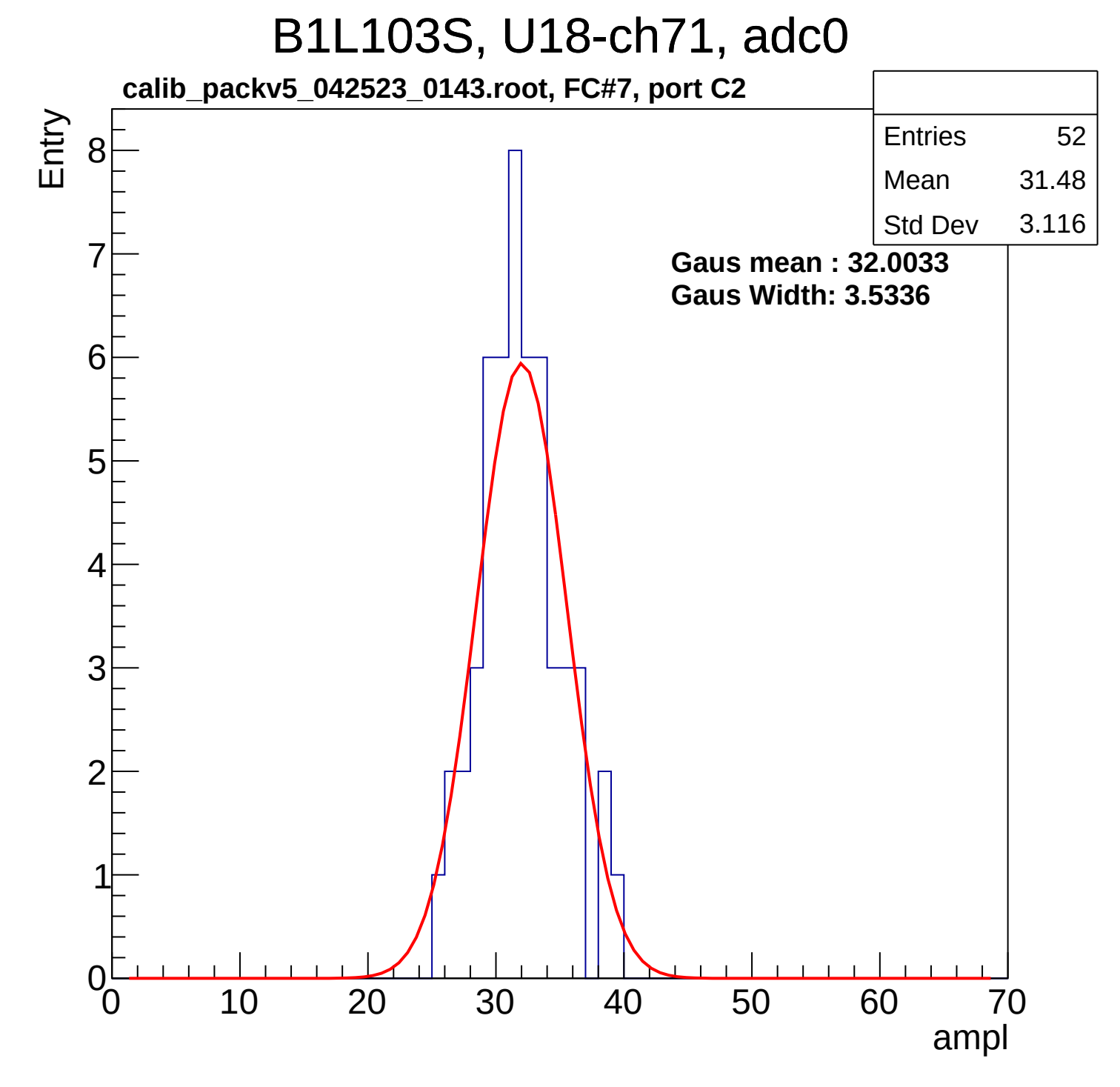
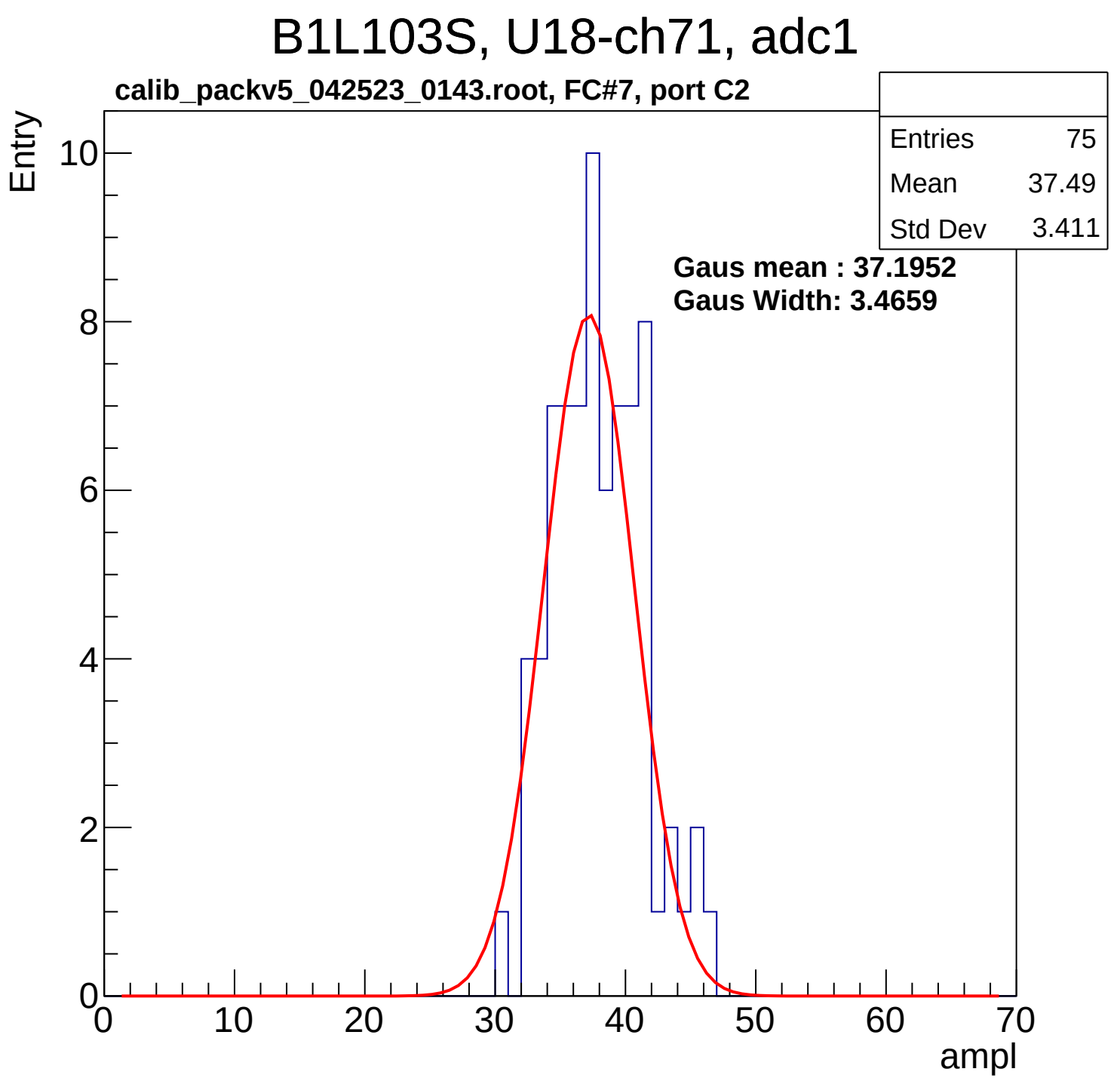
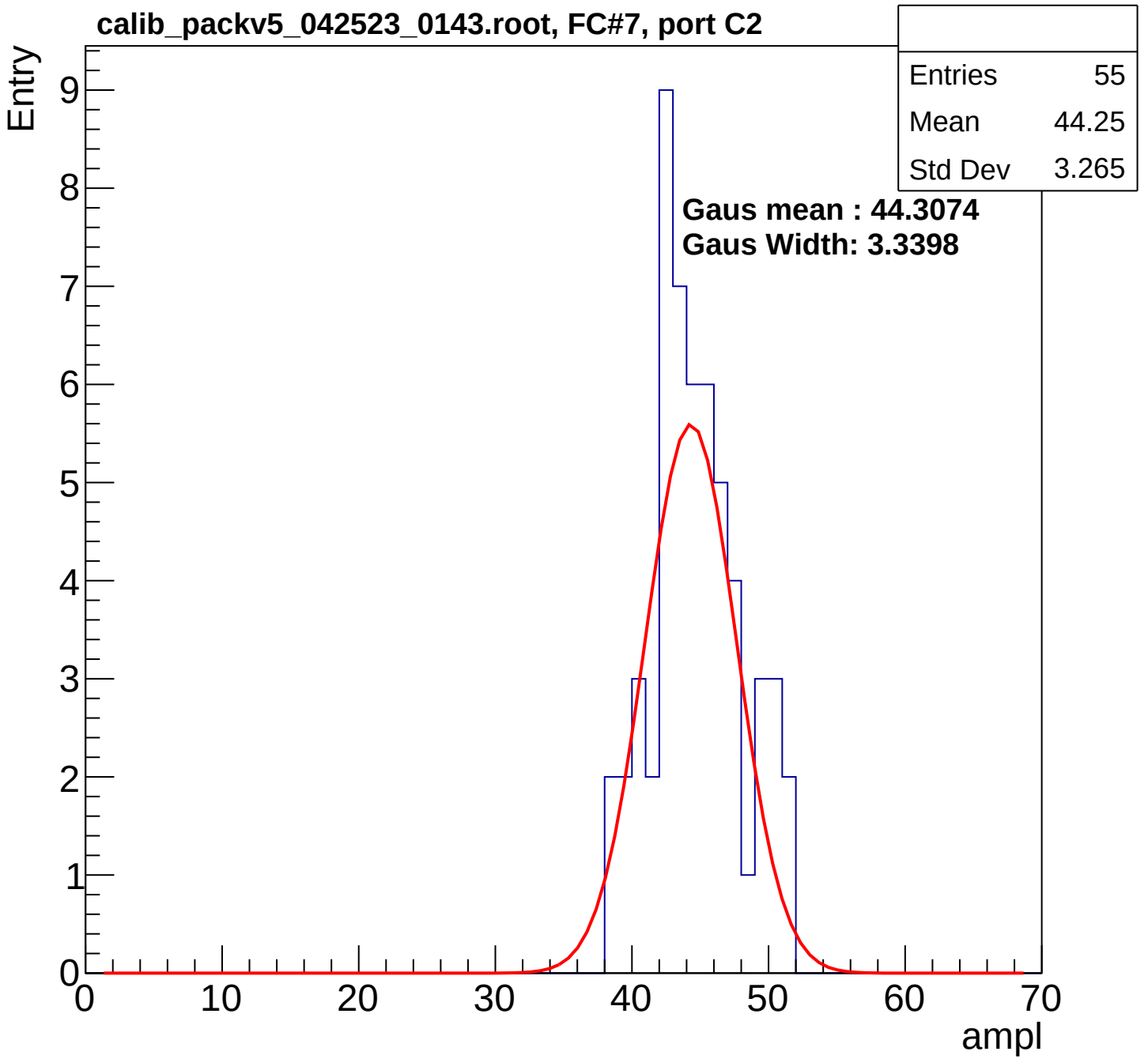
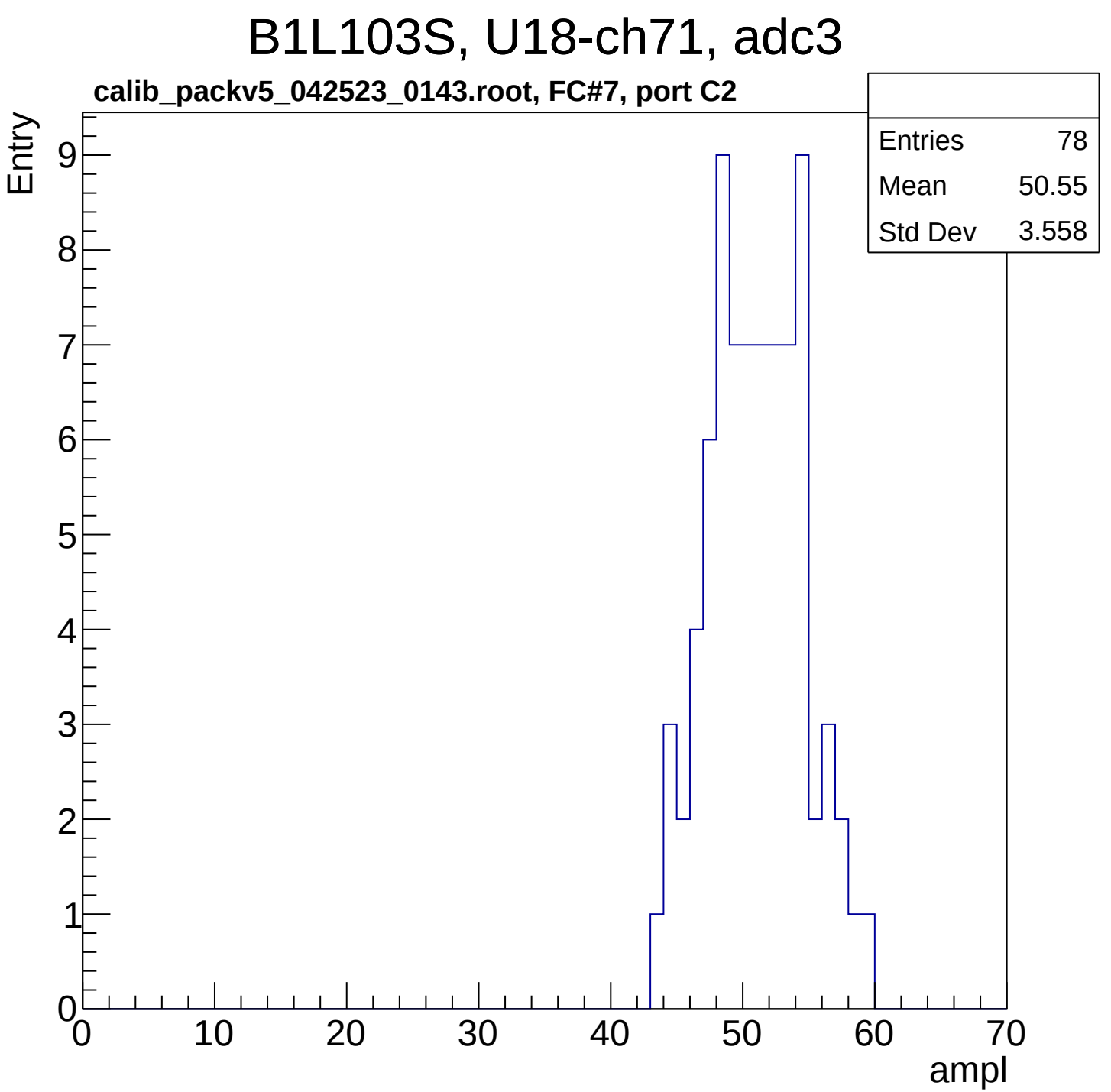

B1L103S, U18-ch70, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 10
Mean 61.2
Std Dev 2.227
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U18-ch70, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch71, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 52
Mean 31.48
Std Dev 3.116
Gaus mean : 32.0033
Gaus Width: 3.5336
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch71, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 75
Mean 37.49
Std Dev 3.411
Gaus mean : 37.1952
Gaus Width: 3.4659
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch71, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 44.25
Std Dev 3.265
Gaus mean : 44.3074
Gaus Width: 3.3398
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch71, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 78
Mean 50.55
Std Dev 3.558
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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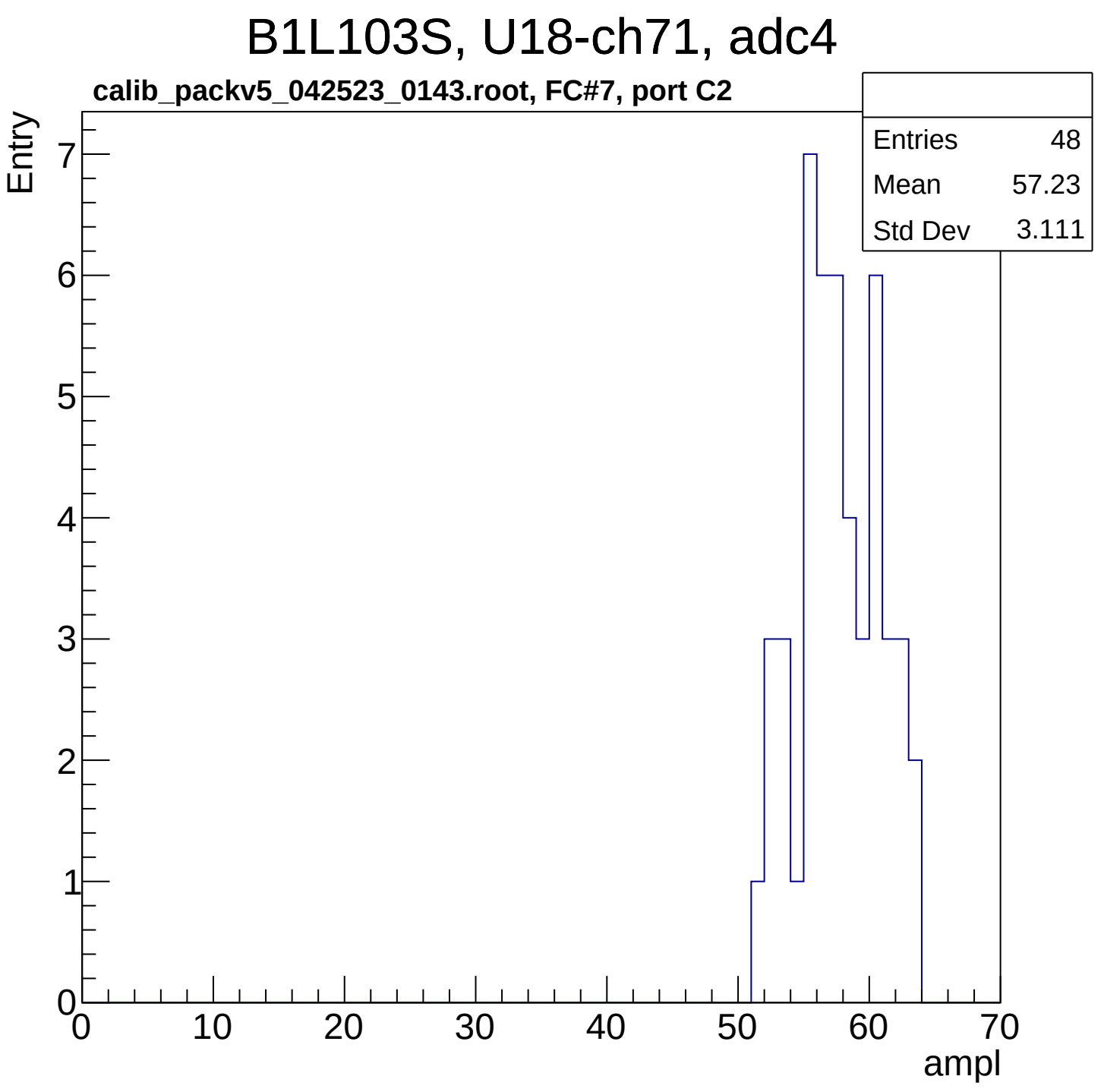
40
50
60
70


B1L103S, U18-ch71, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 48
Mean 57.23
Std Dev 3.111
Entry
ampl
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1
2
3
4
5
6
7
0
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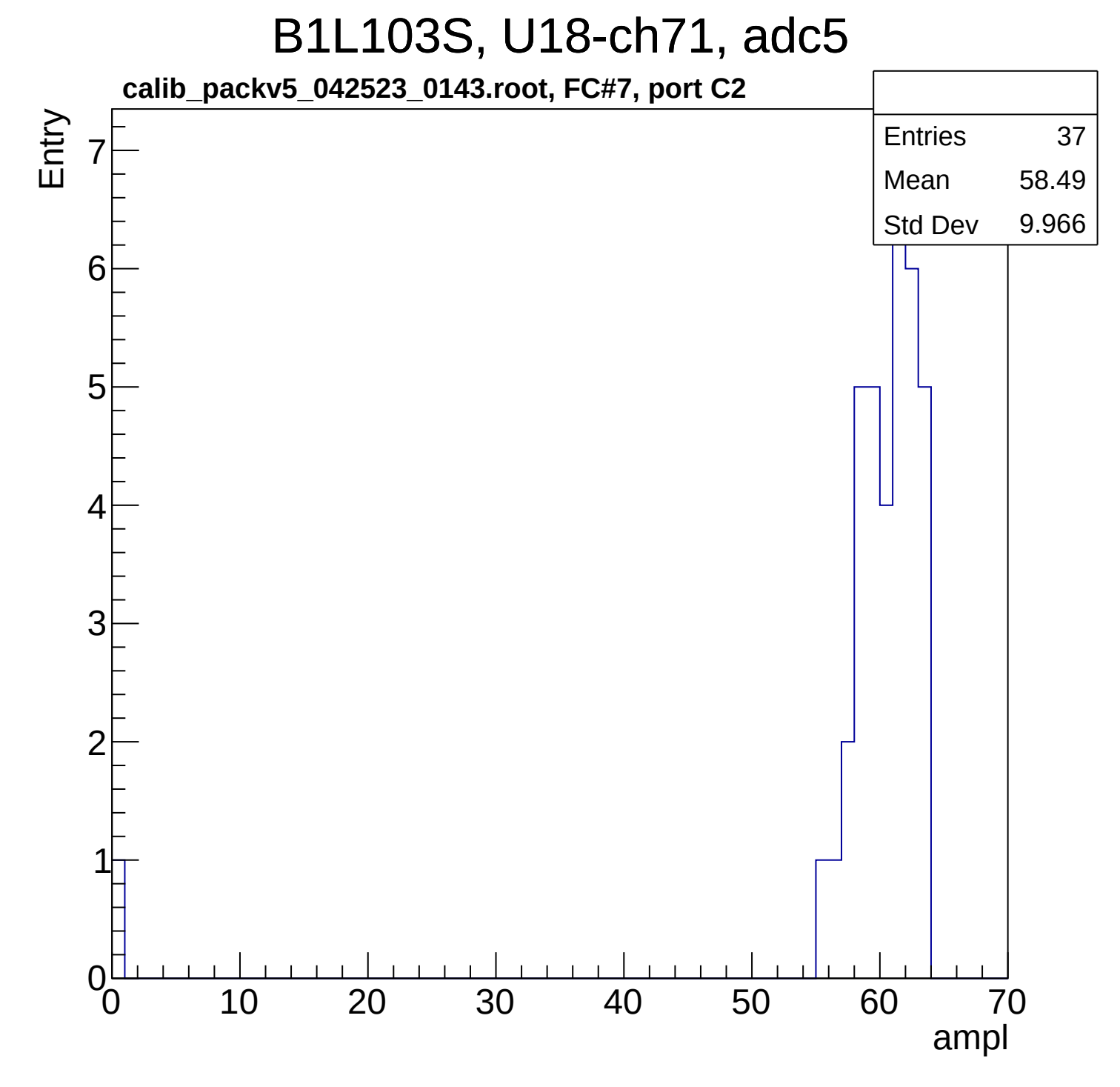
20
30
40
50
60
70


B1L103S, U18-ch71, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 37
Mean 58.49
Std Dev 9.966
Entry
ampl
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1
2
3
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60
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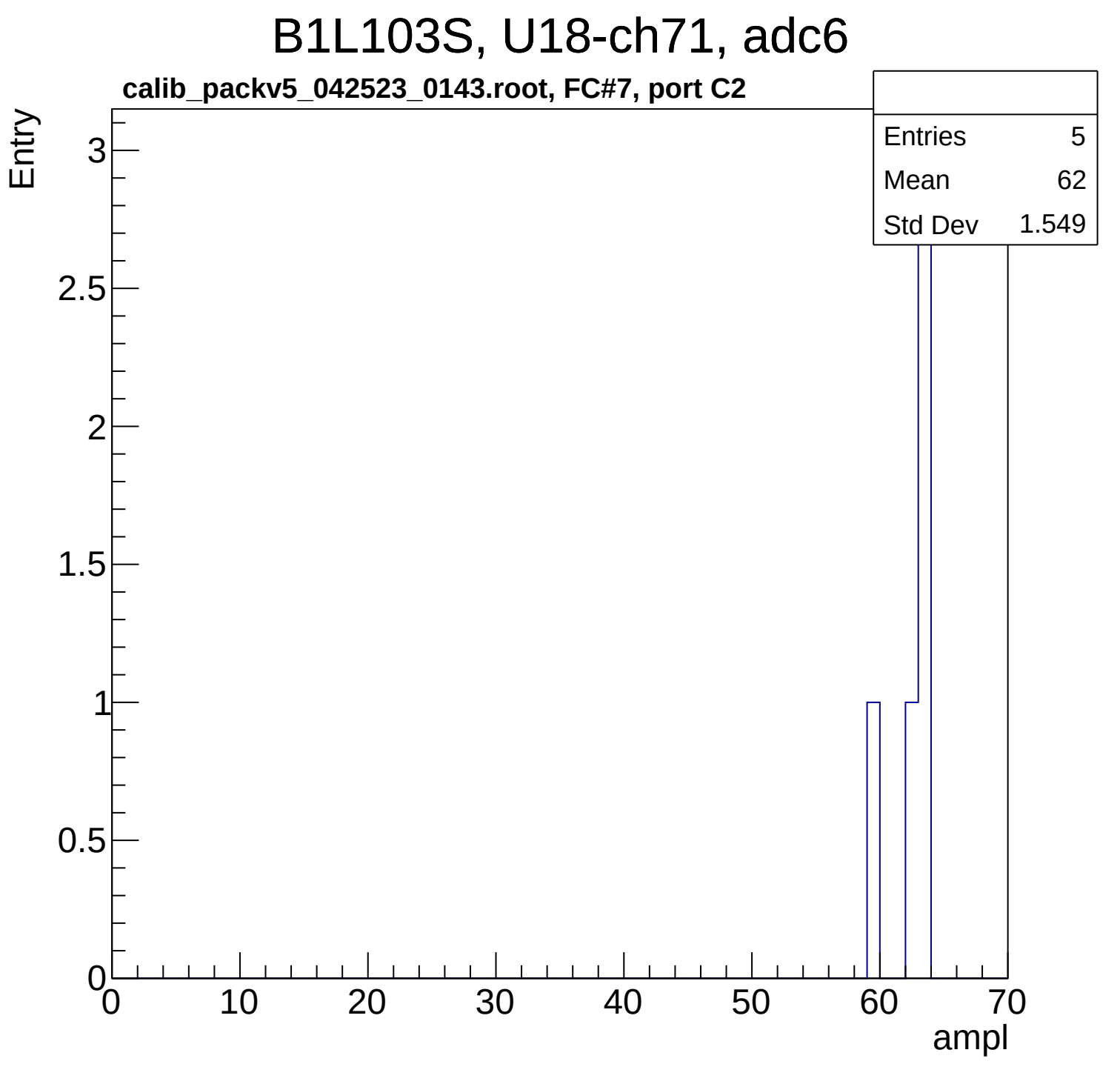
B1L103S, U18-ch71, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 5
Mean 62
Std Dev 1.549
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
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20
30
40
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60
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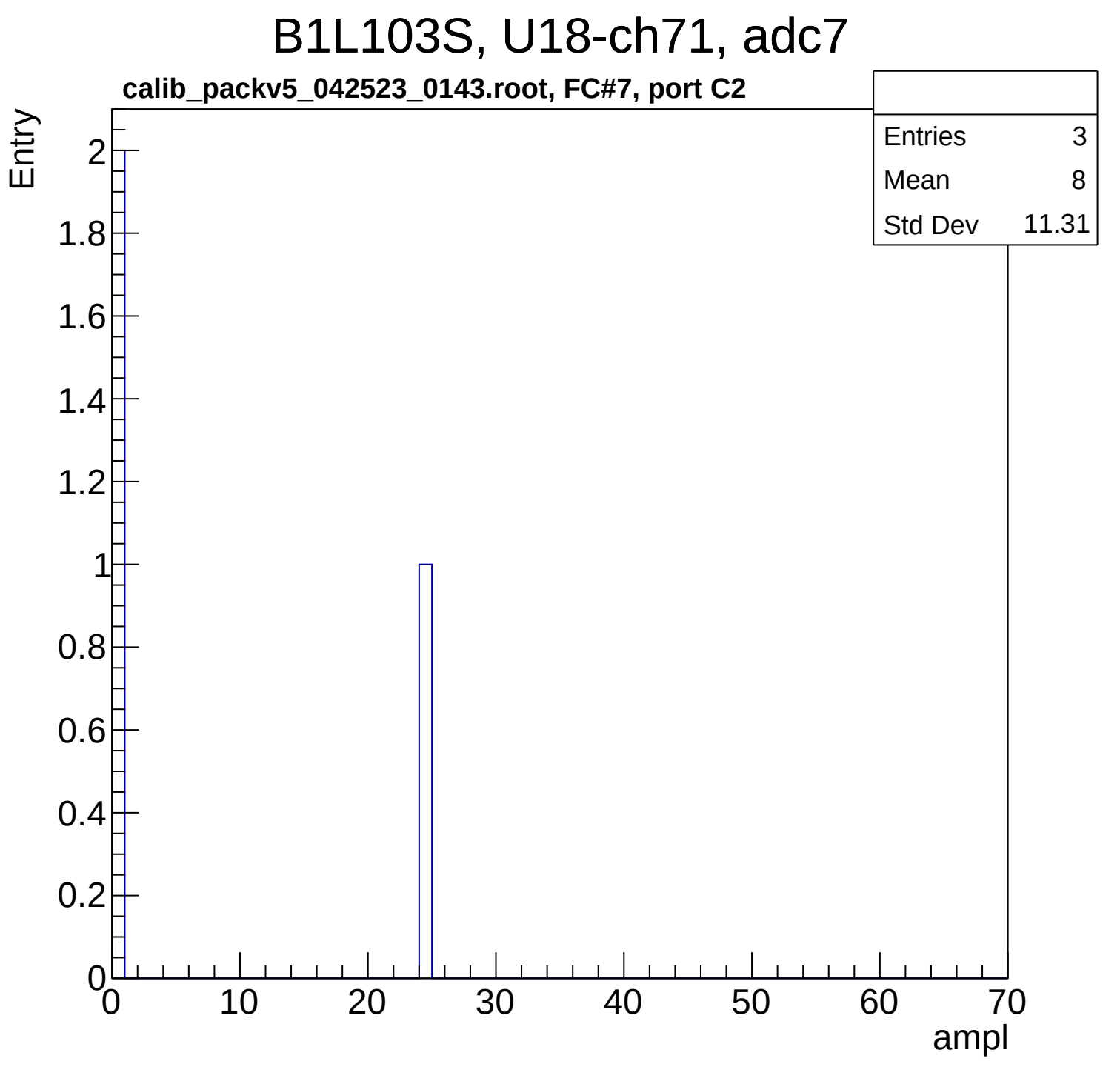
B1L103S, U18-ch71, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 8
Std Dev 11.31
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
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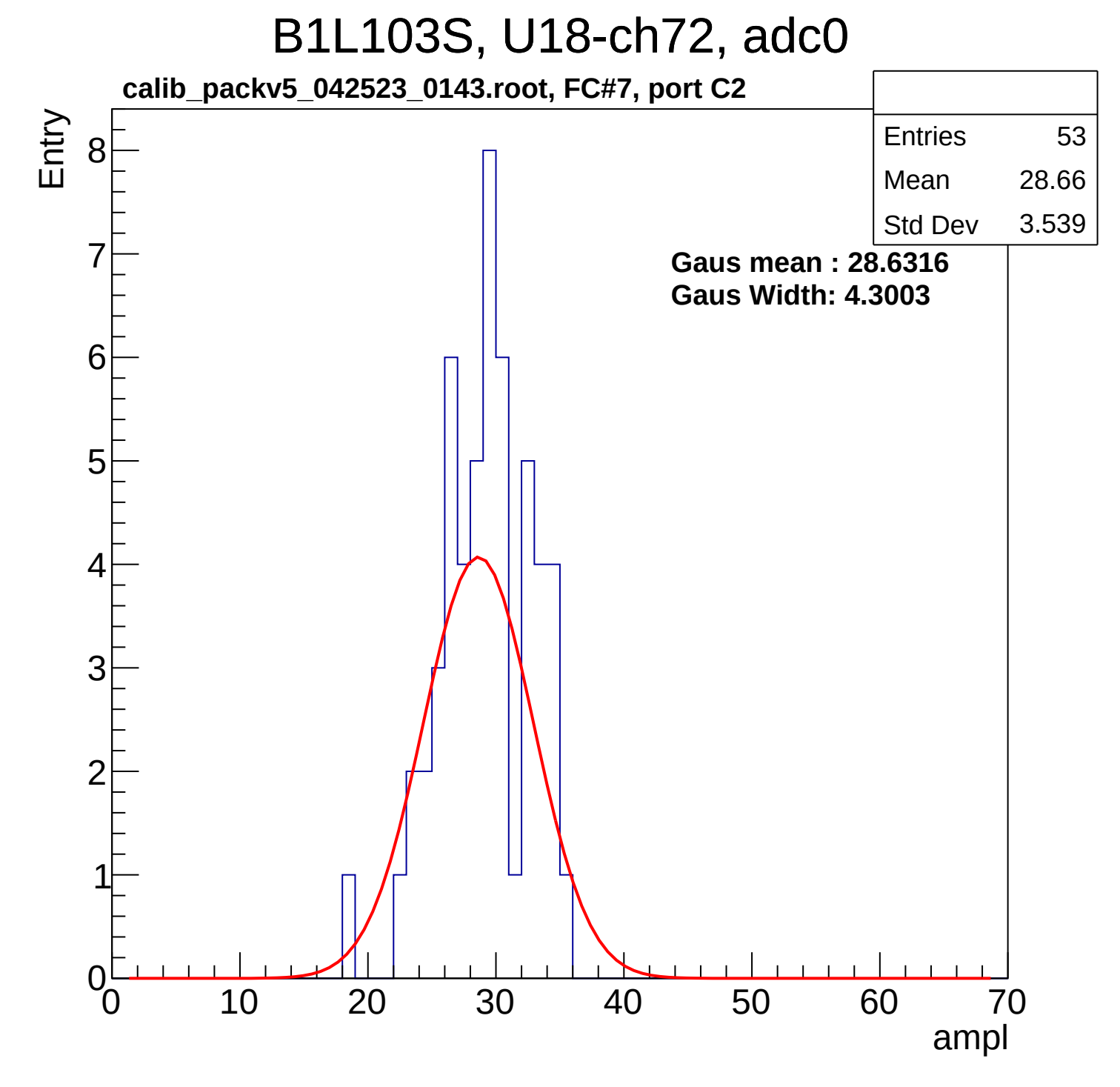
60
70


B1L103S, U18-ch72, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 28.66
Std Dev 3.539
Gaus mean : 28.6316
Gaus Width: 4.3003
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
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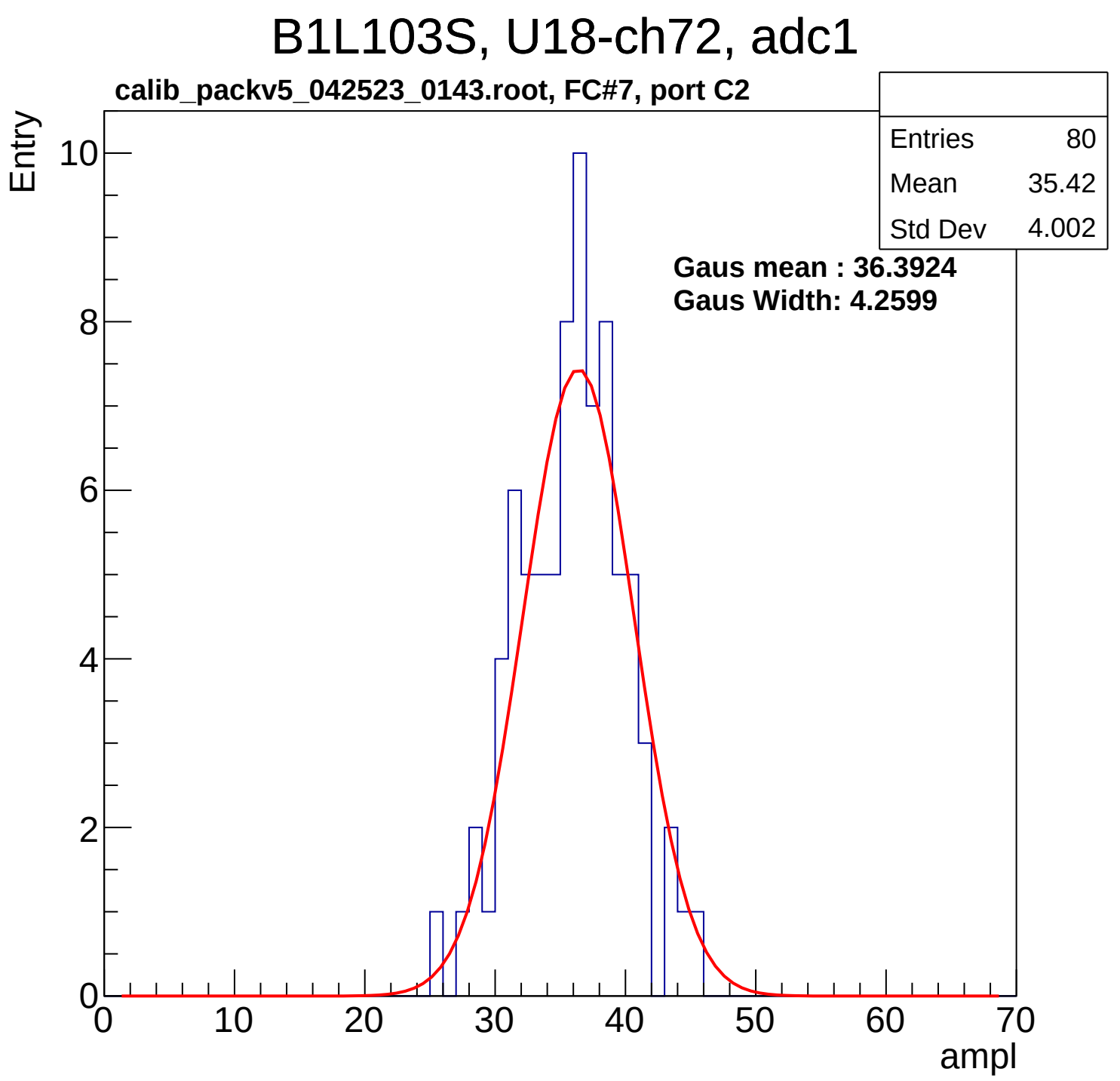
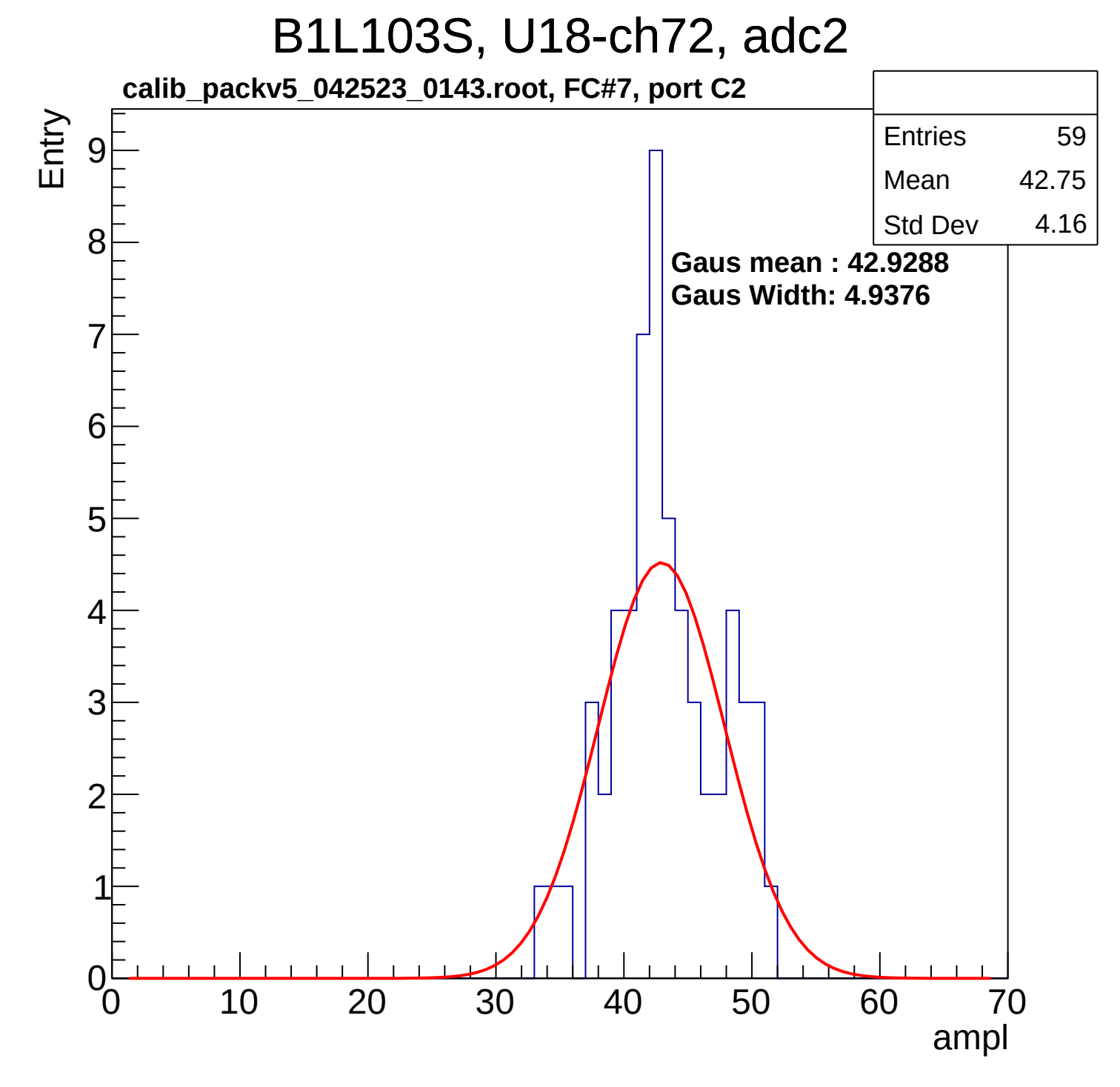
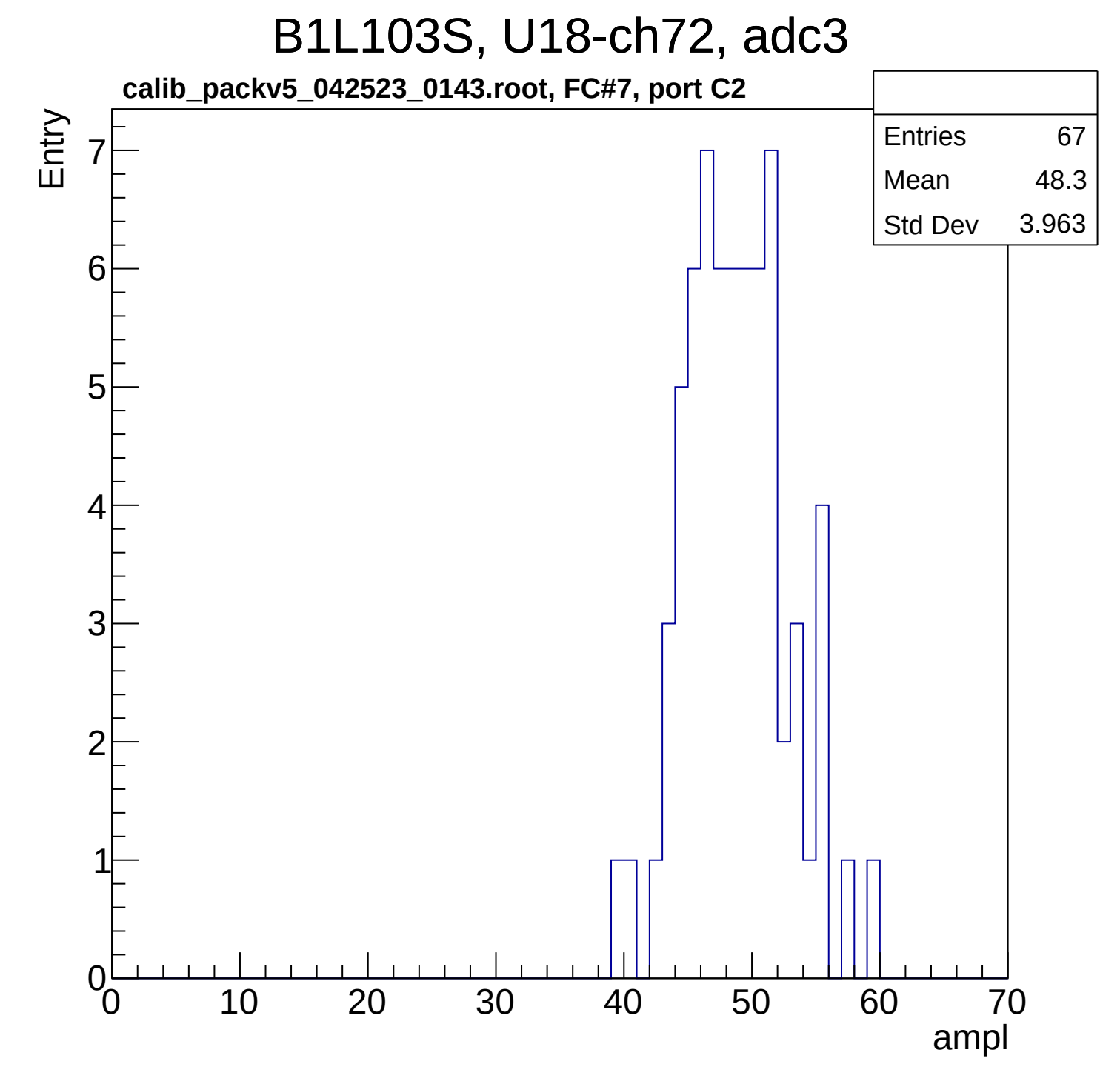
60
70


B1L103S, U18-ch72, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 80
Mean 35.42
Std Dev 4.002
Gaus mean : 36.3924
Gaus Width: 4.2599
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch72, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 42.75
Std Dev 4.16
Gaus mean : 42.9288
Gaus Width: 4.9376
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L103S, U18-ch72, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 48.3
Std Dev 3.963
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
30
40
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60
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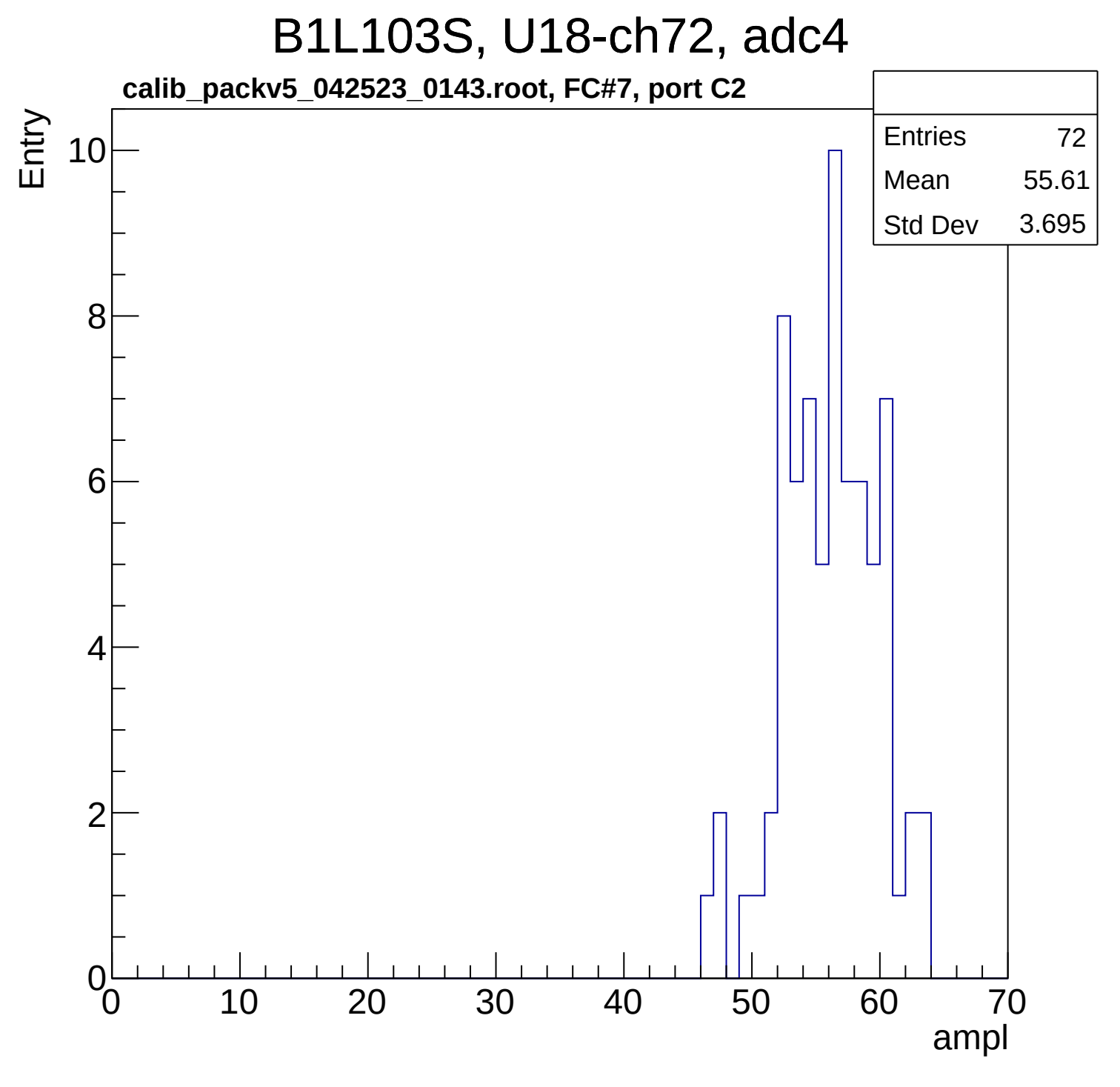
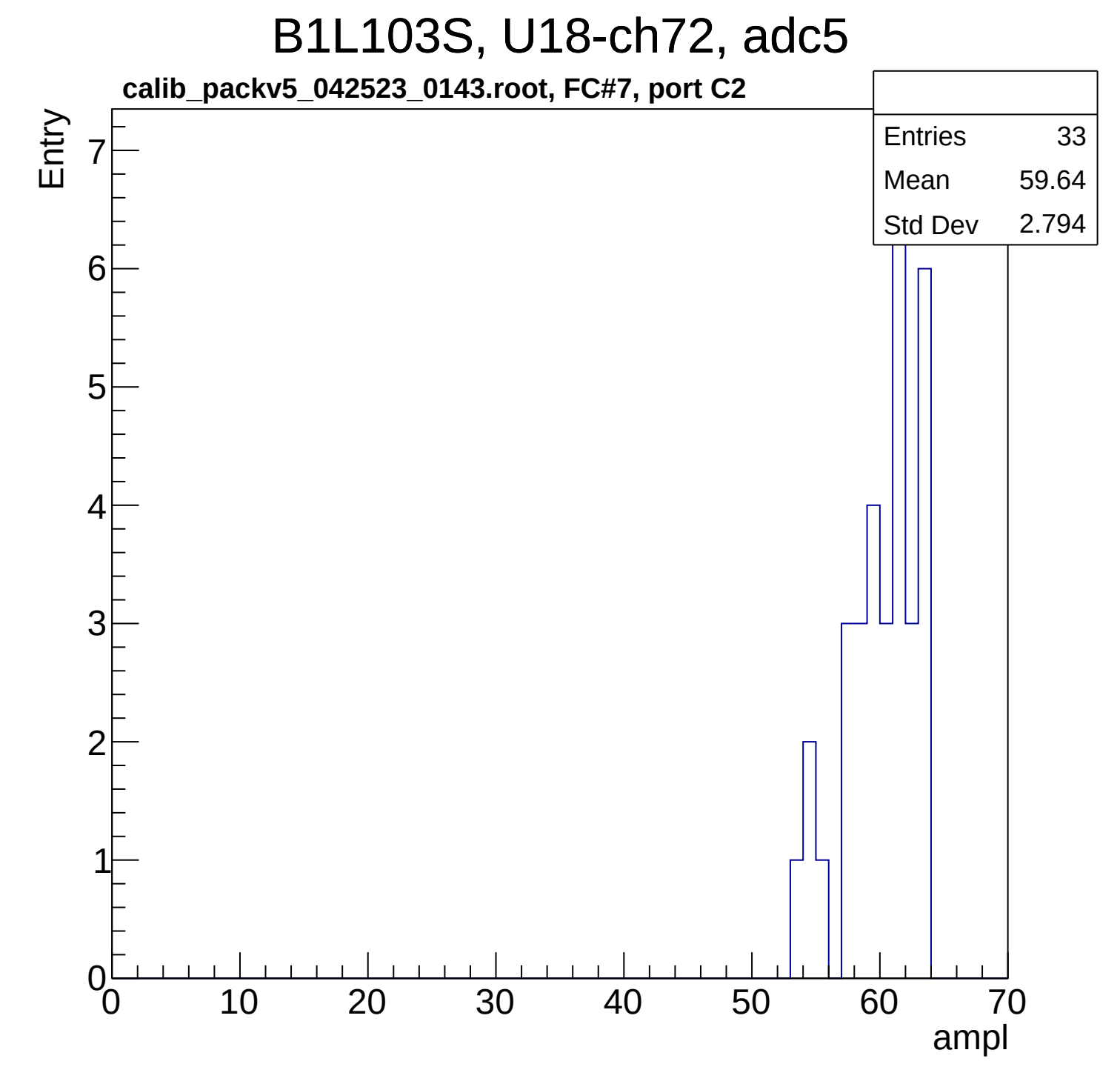
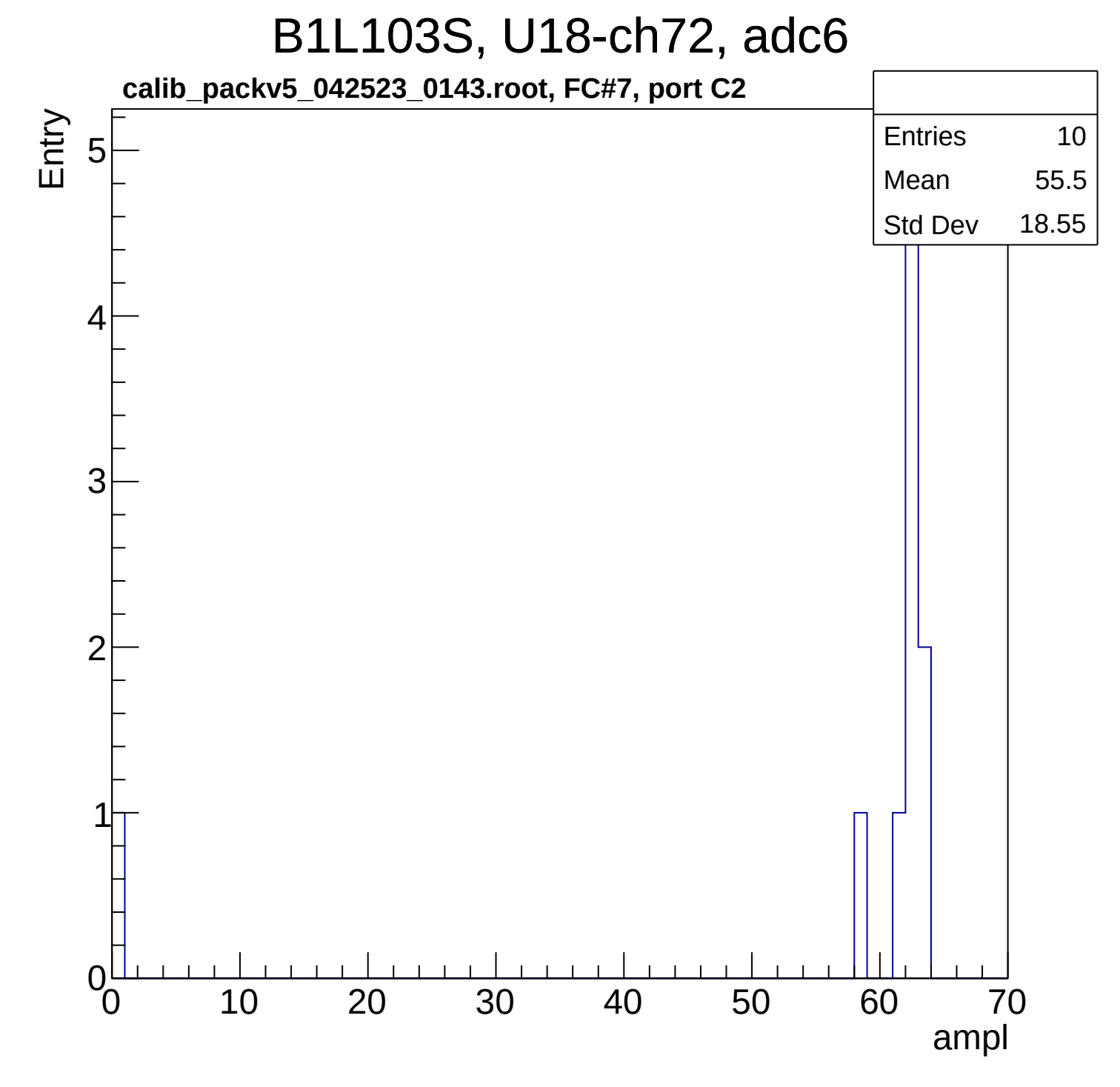
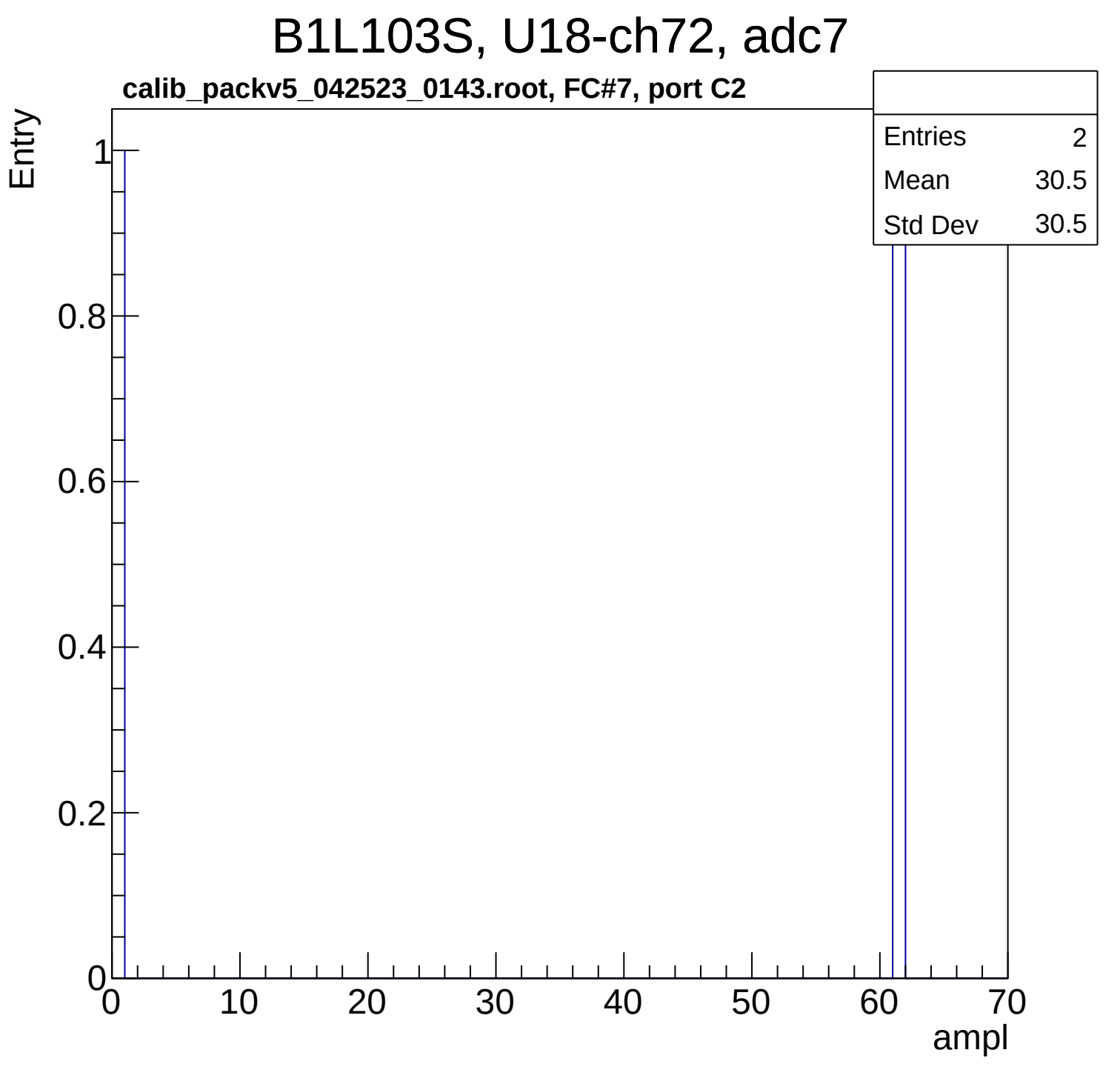
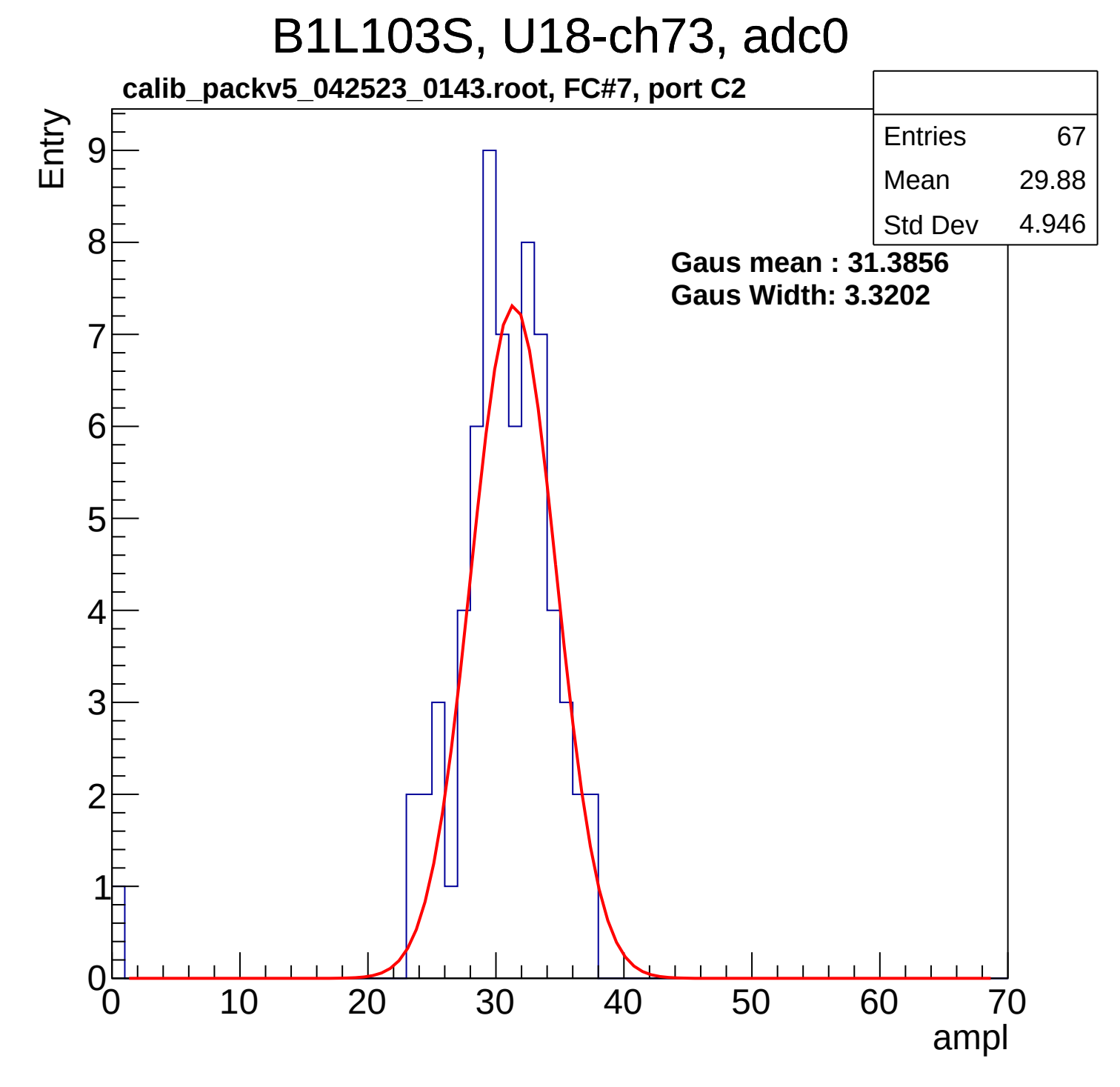
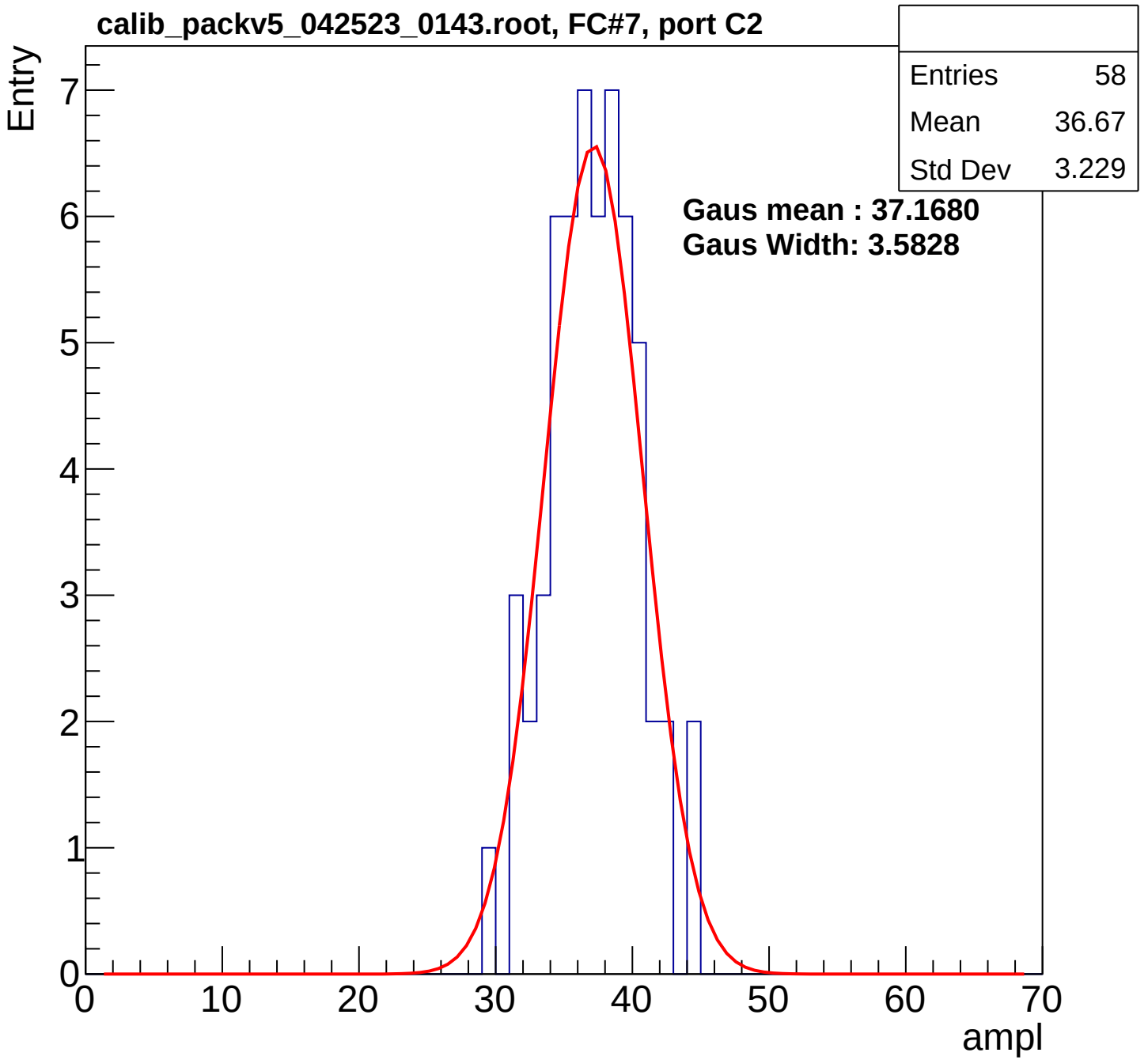

B1L103S, U18-ch72, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 72
Mean 55.61
Std Dev 3.695
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch72, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 33
Mean 59.64
Std Dev 2.794
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch72, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 10
Mean 55.5
Std Dev 18.55
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch72, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 30.5
Std Dev 30.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch73, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 29.88
Std Dev 4.946
Gaus mean : 31.3856
Gaus Width: 3.3202
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch73, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 58
Mean 36.67
Std Dev 3.229
Gaus mean : 37.1680
Gaus Width: 3.5828
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
50
60
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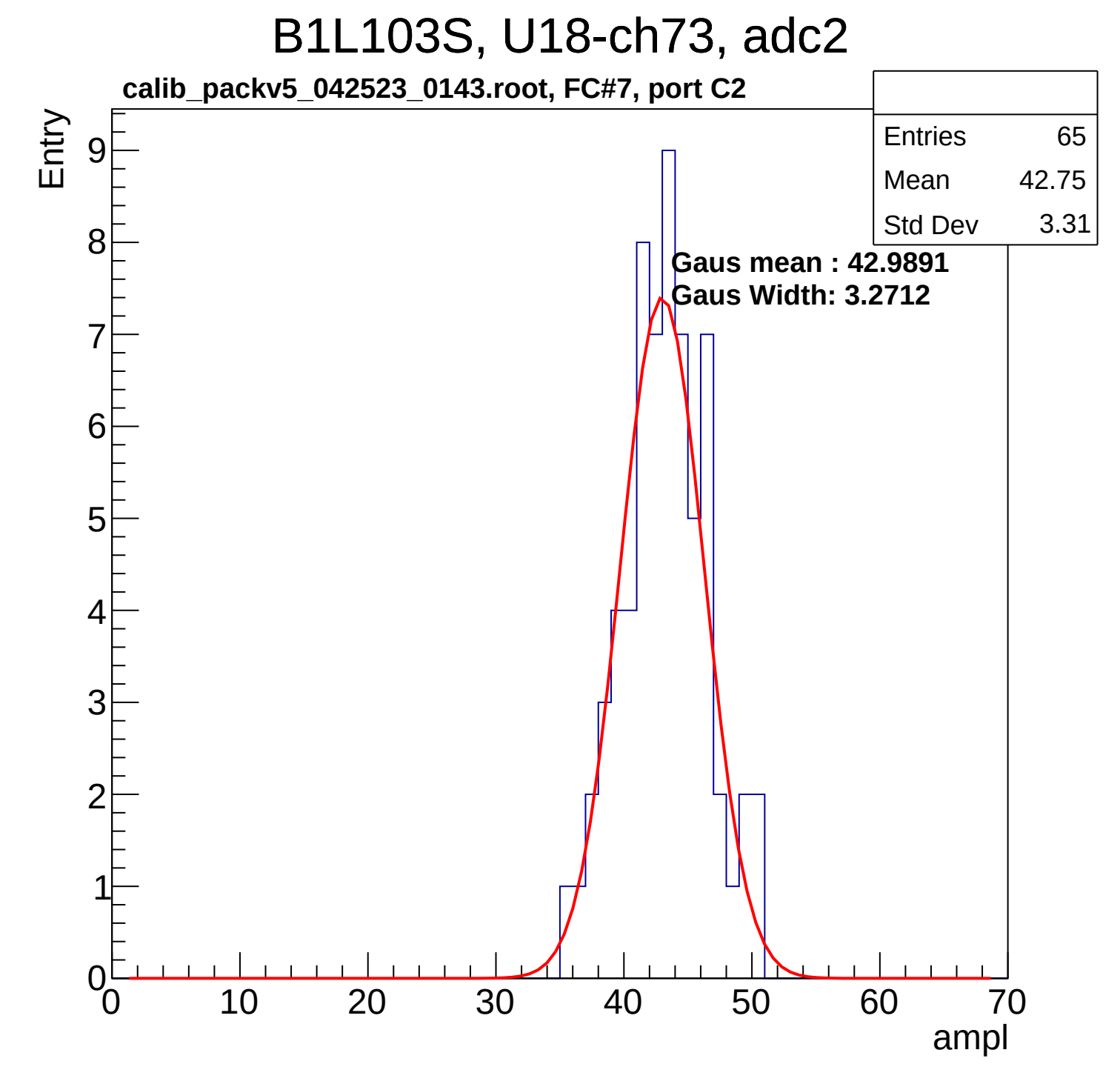
B1L103S, U18-ch73, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 42.75
Std Dev 3.31
Gaus mean : 42.9891
Gaus Width: 3.2712
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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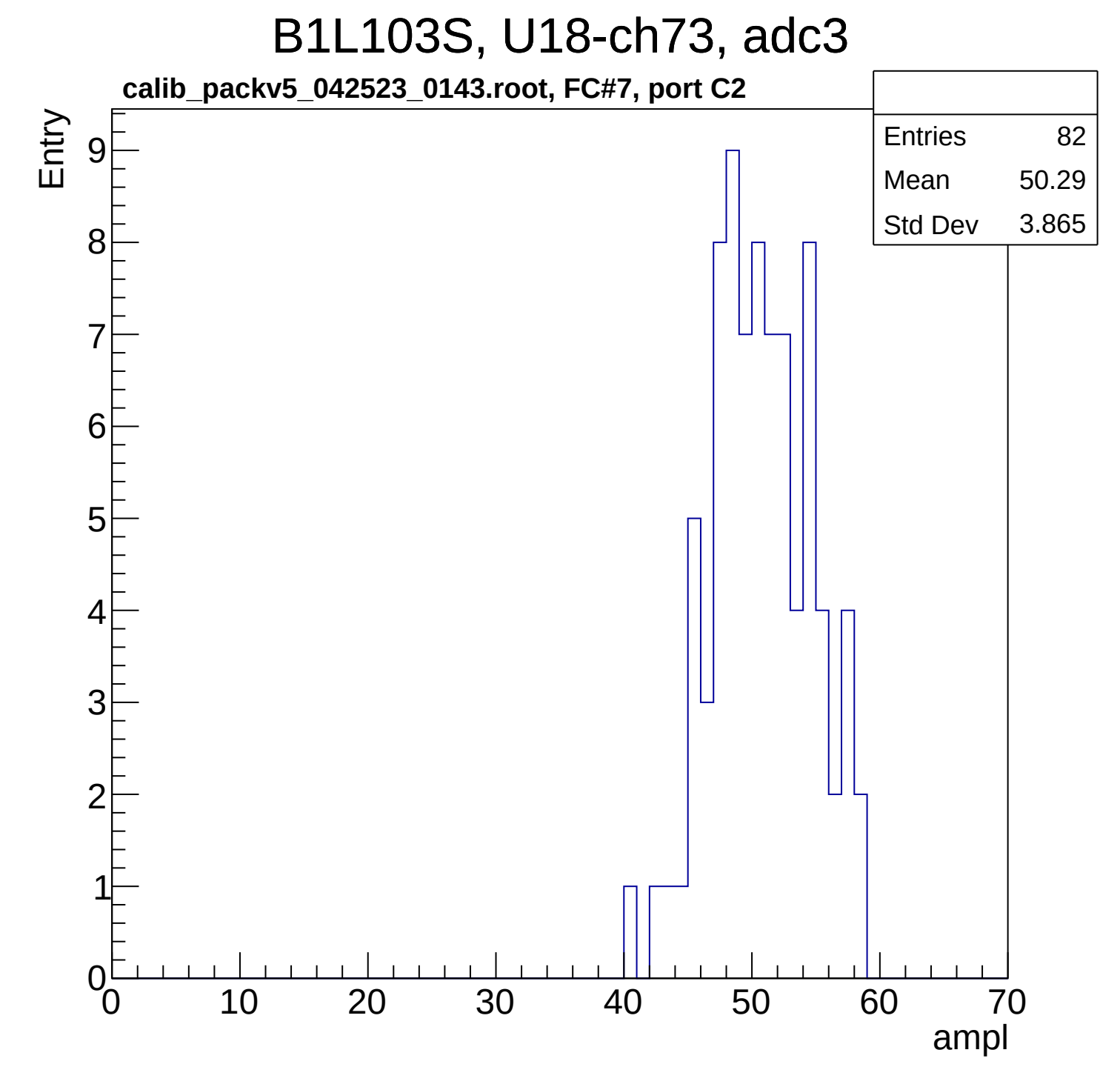
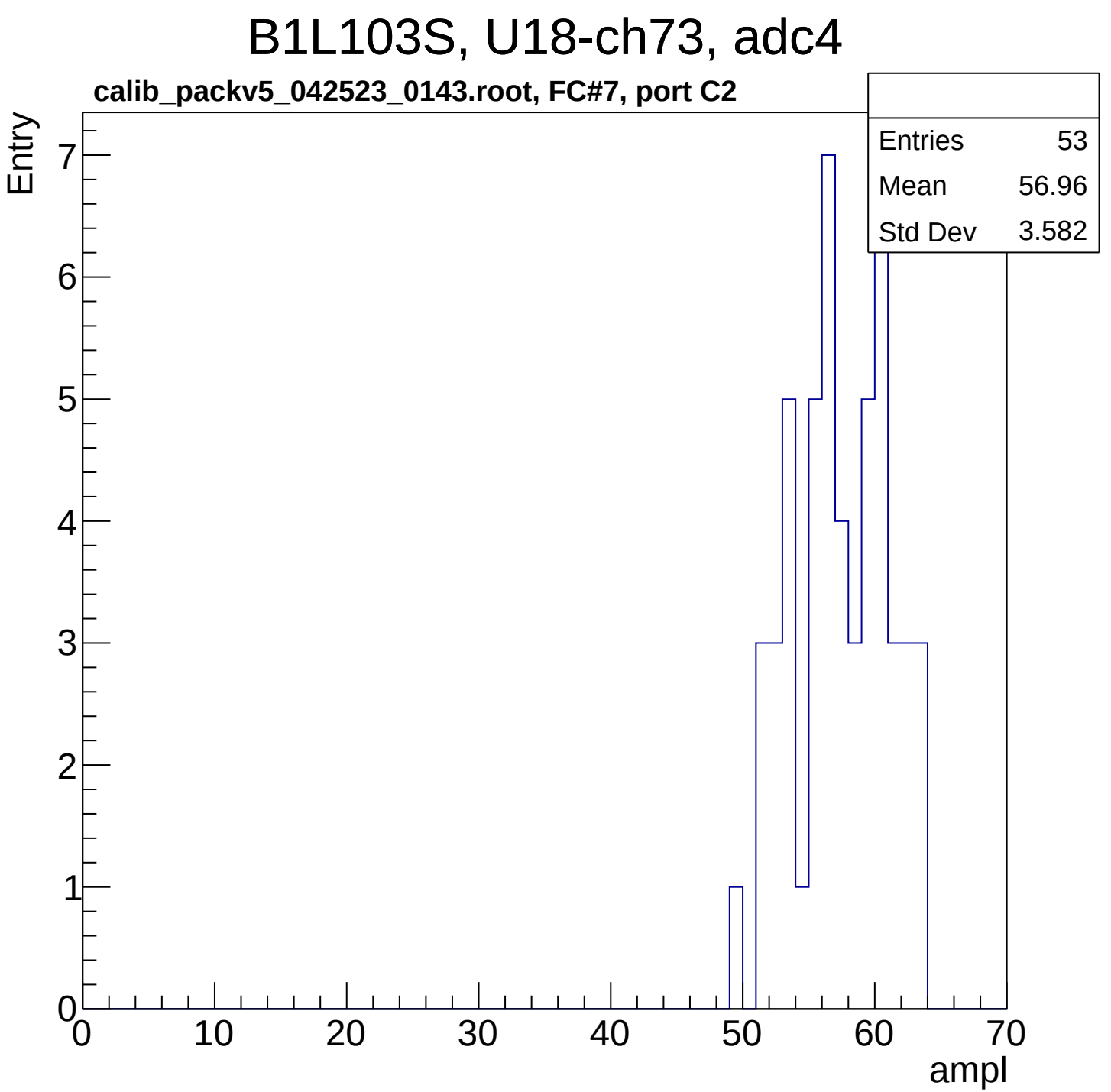
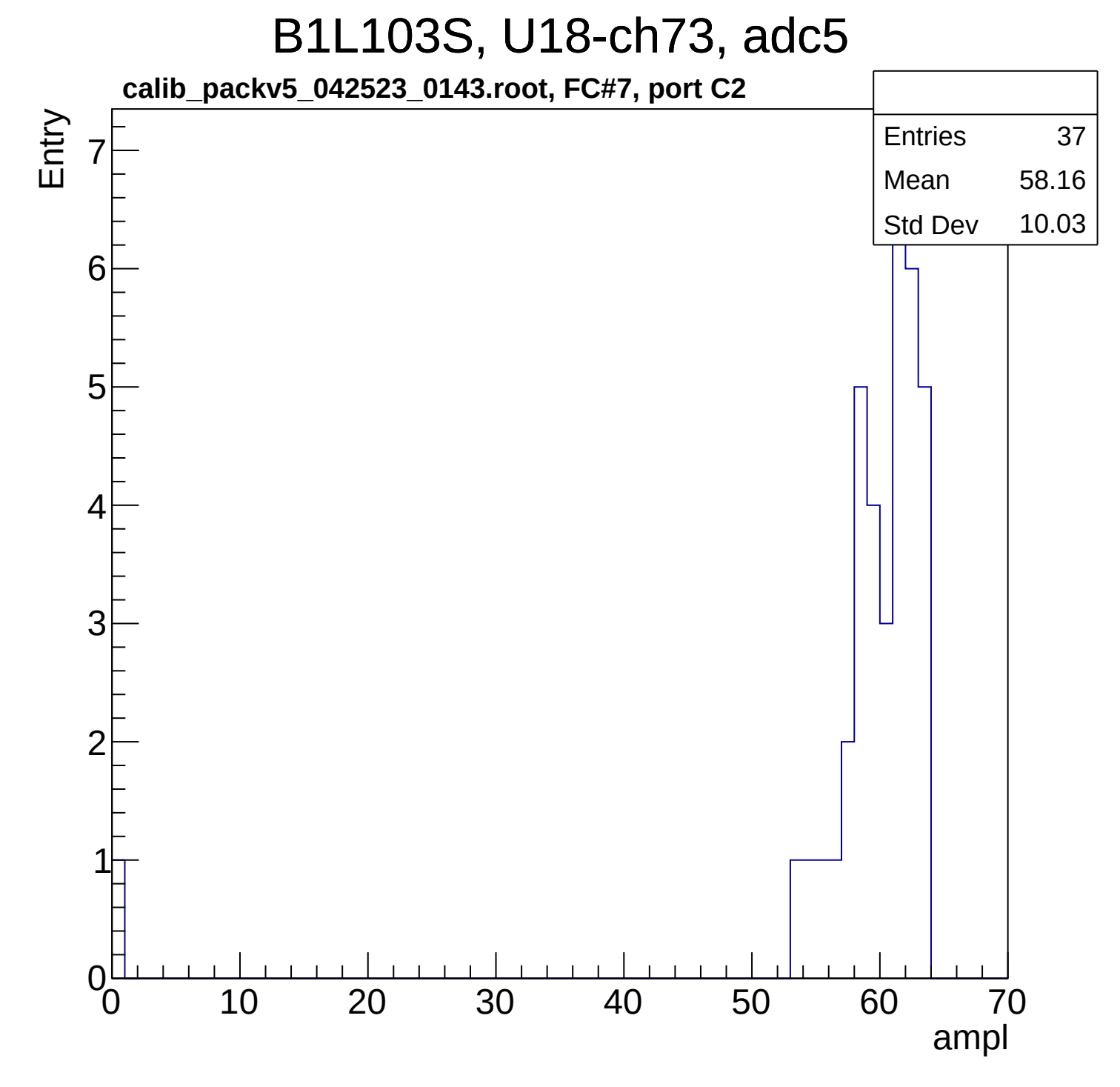
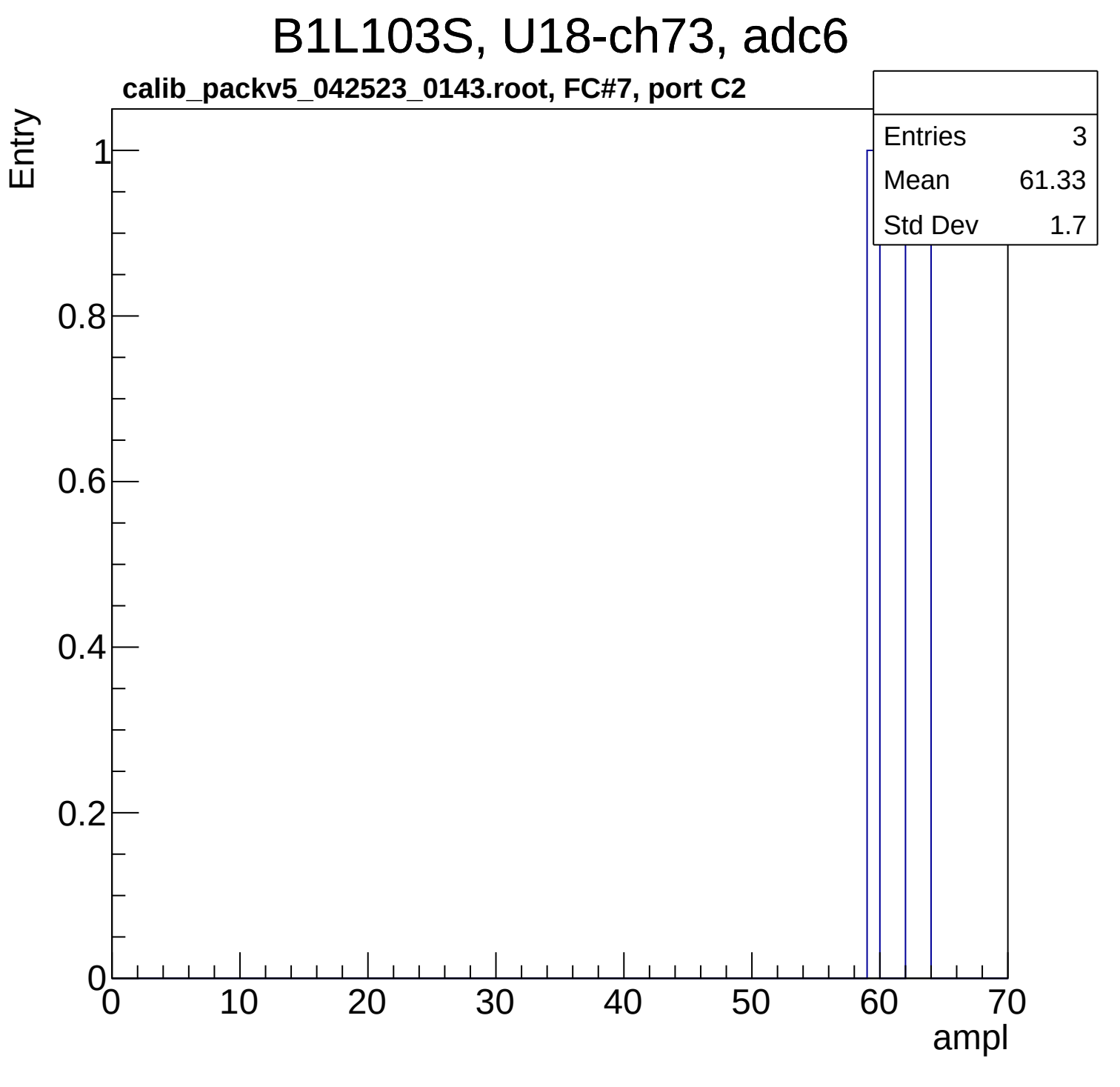
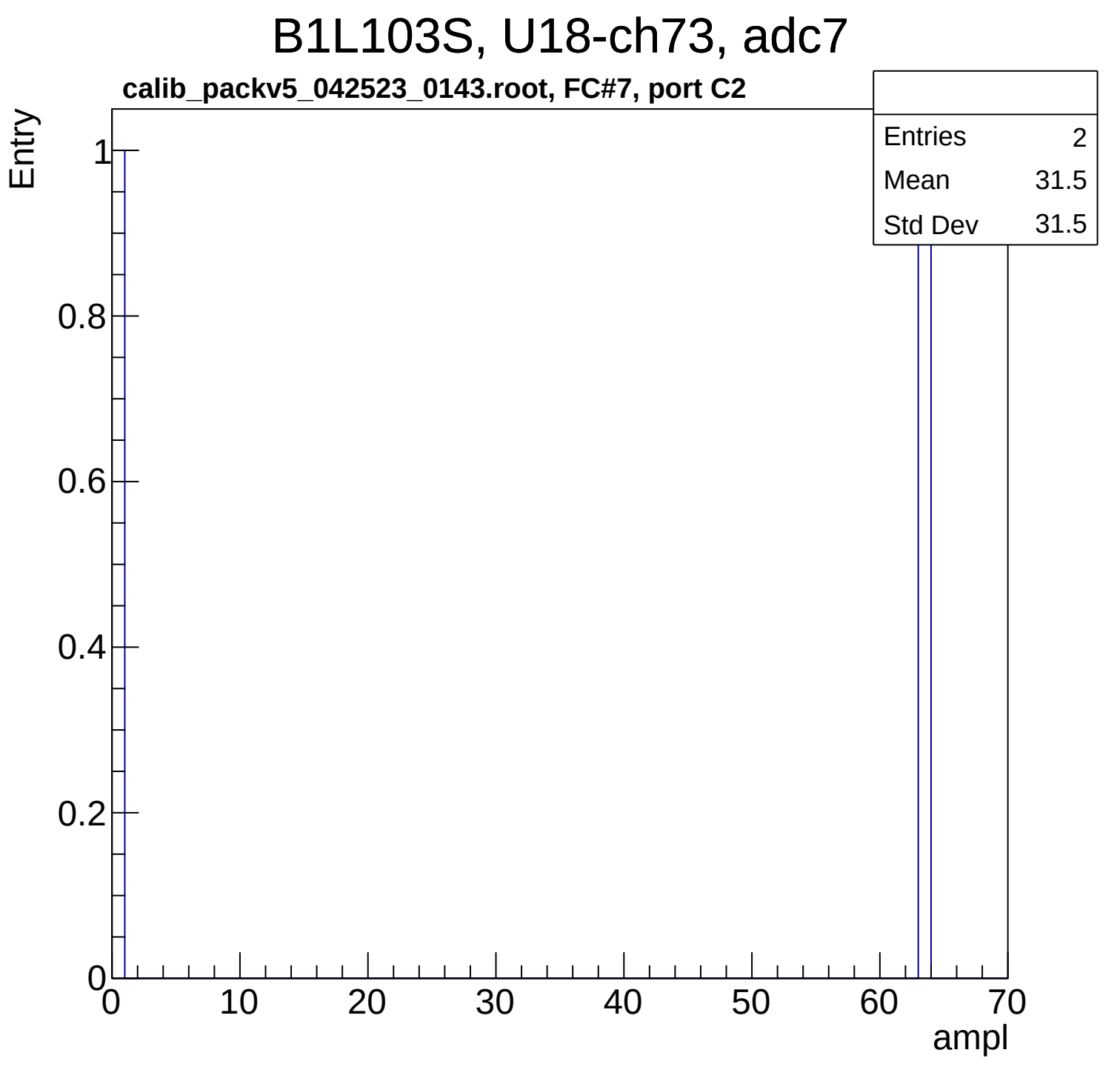
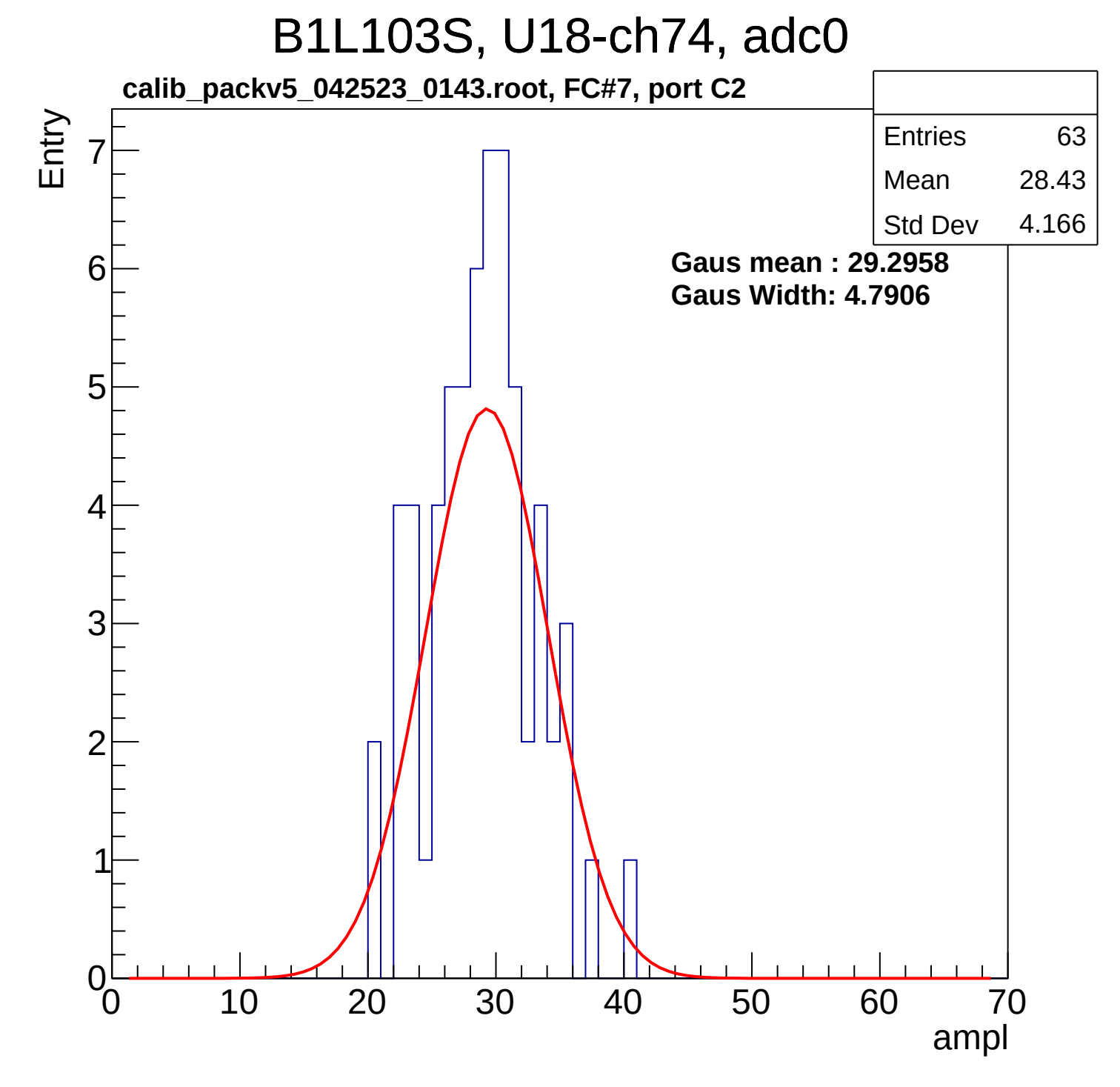

B1L103S, U18-ch73, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 82
Mean 50.29
Std Dev 3.865
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

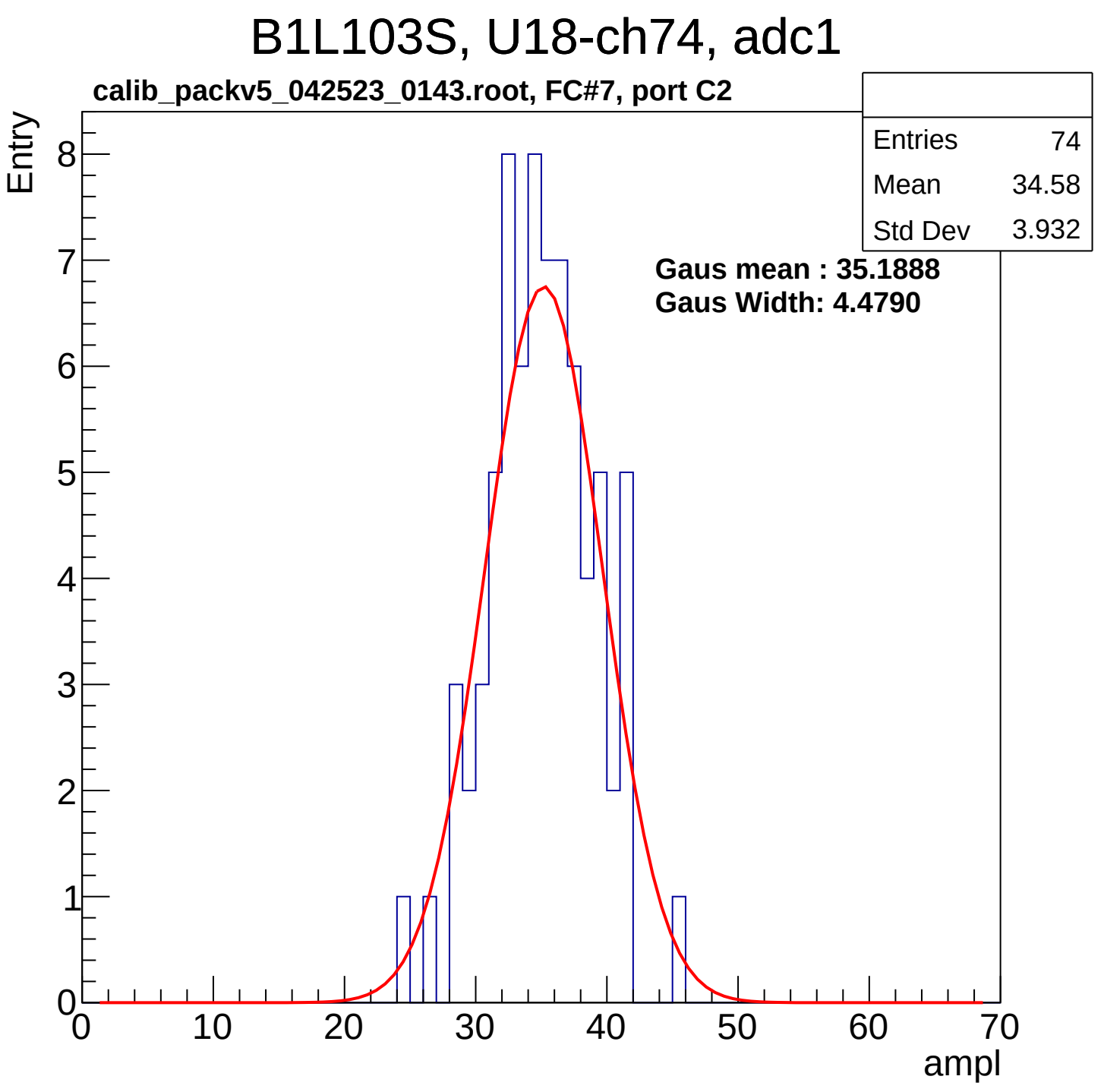

B1L103S, U18-ch73, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 56.96
Std Dev 3.582
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

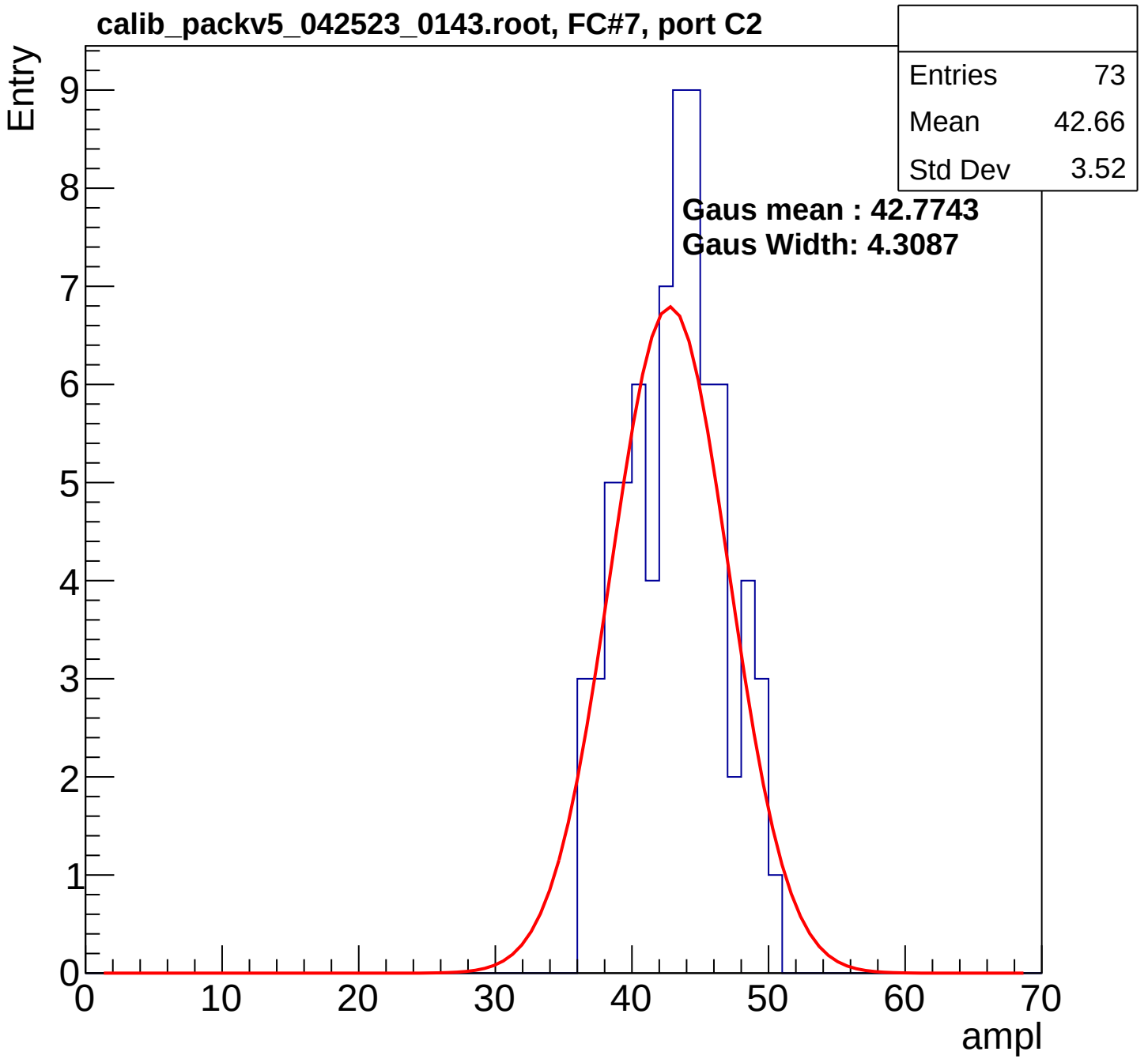

B1L103S, U18-ch73, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 37
Mean 58.16
Std Dev 10.03
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

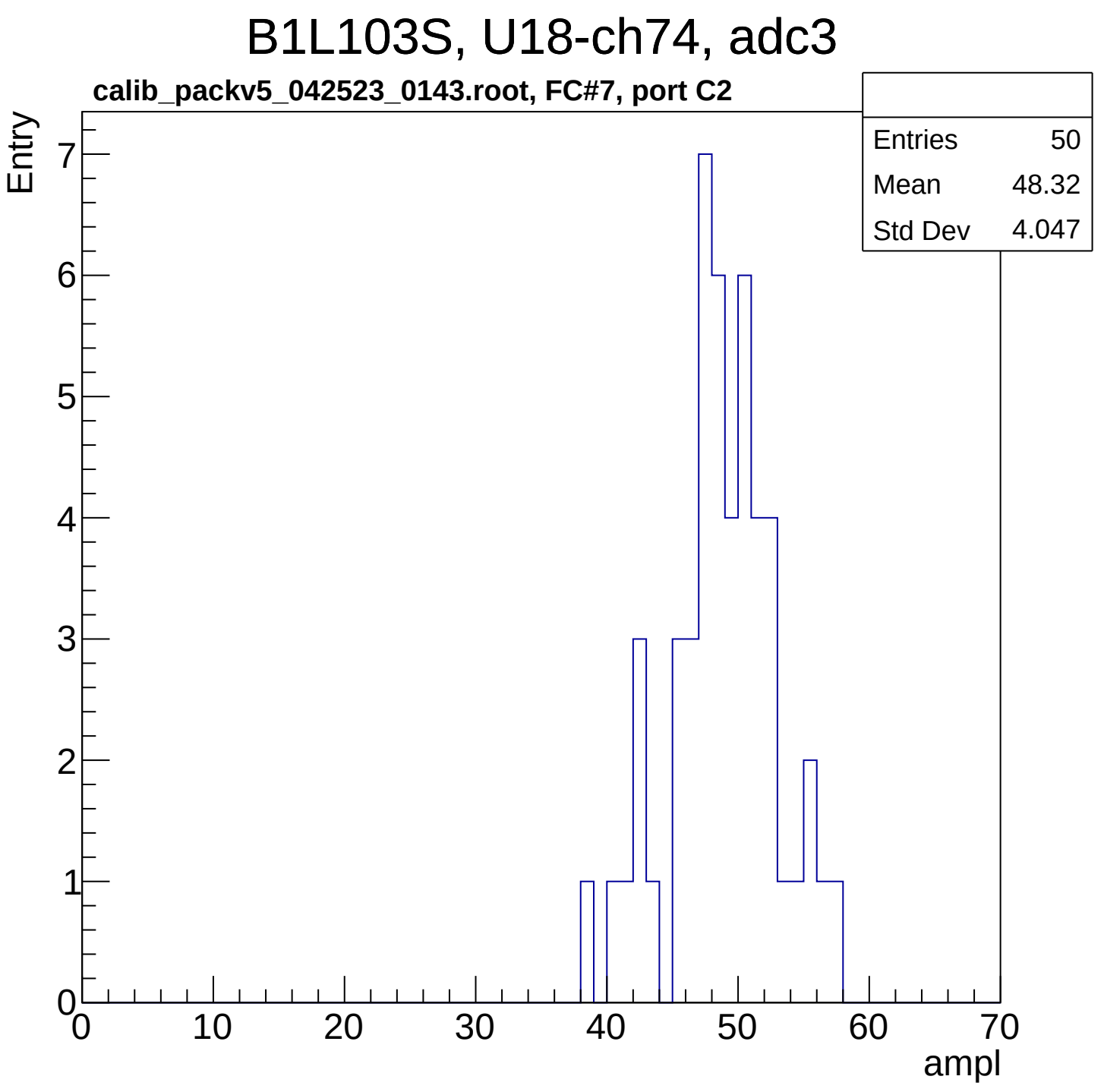

B1L103S, U18-ch73, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 61.33
Std Dev 1.7
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

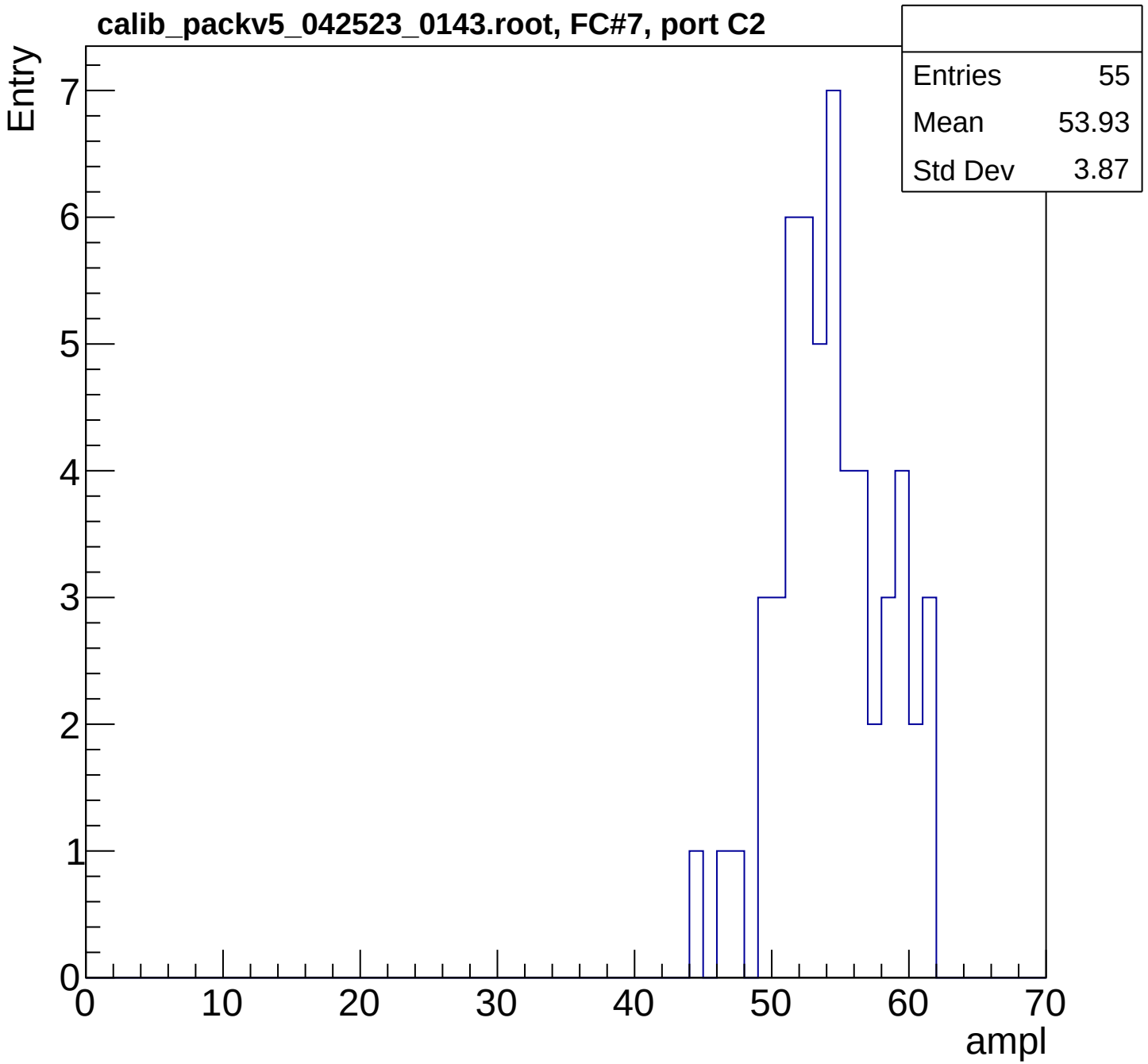

B1L103S, U18-ch73, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 31.5
Std Dev 31.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

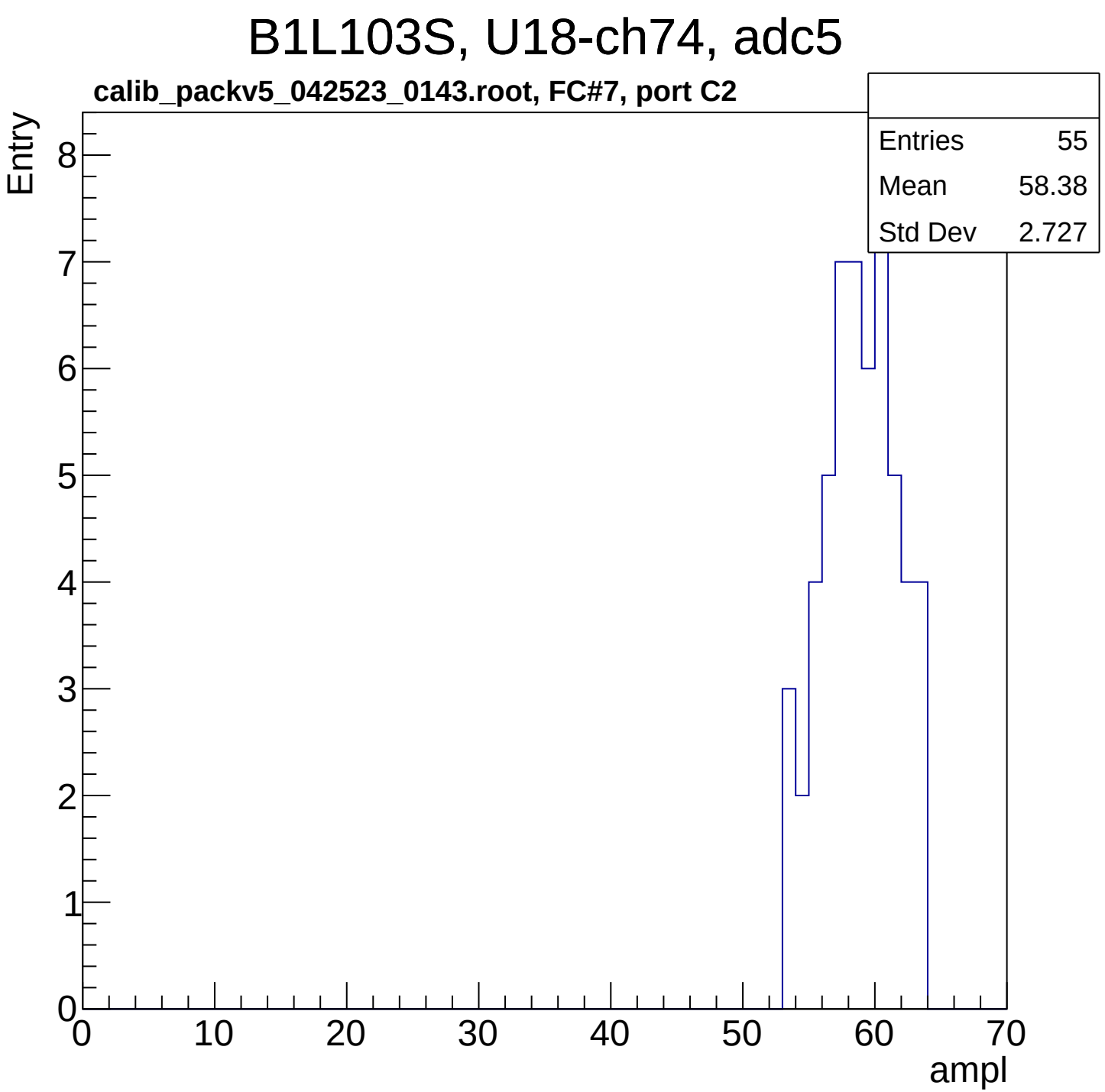

B1L103S, U18-ch74, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 28.43
Std Dev 4.166
Gaus mean : 29.2958
Gaus Width: 4.7906
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

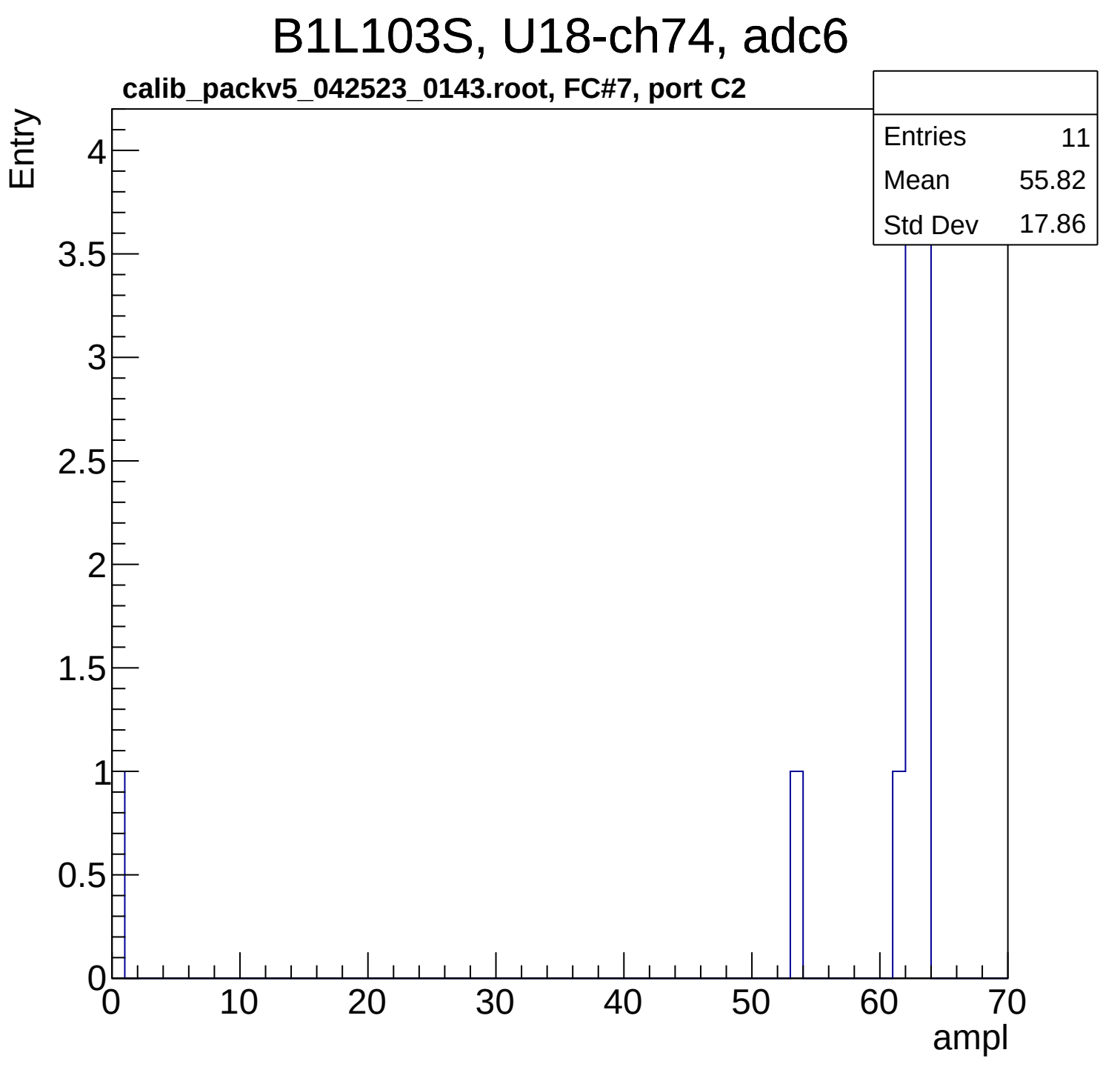

B1L103S, U18-ch74, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 74
Mean 34.58
Std Dev 3.932
Gaus mean : 35.1888
Gaus Width: 4.4790
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

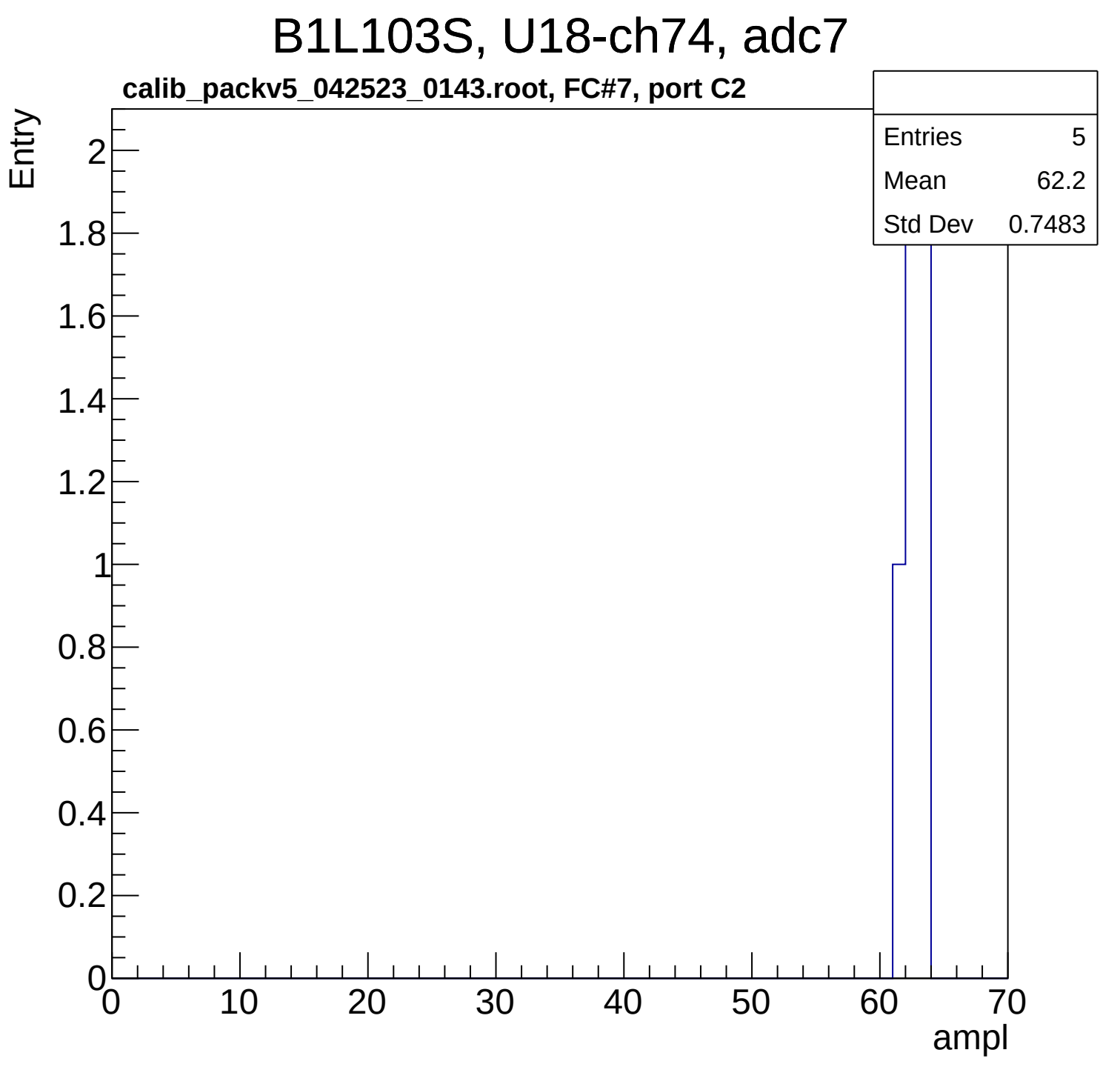

B1L103S, U18-ch74, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 73
Mean 42.66
Std Dev 3.52
Gaus mean : 42.7743
Gaus Width: 4.3087
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch74, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 50
Mean 48.32
Std Dev 4.047
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch74, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 53.93
Std Dev 3.87
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch74, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 58.38
Std Dev 2.727
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch74, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 11
Mean 55.82
Std Dev 17.86
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U18-ch74, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 5
Mean 62.2
Std Dev 0.7483
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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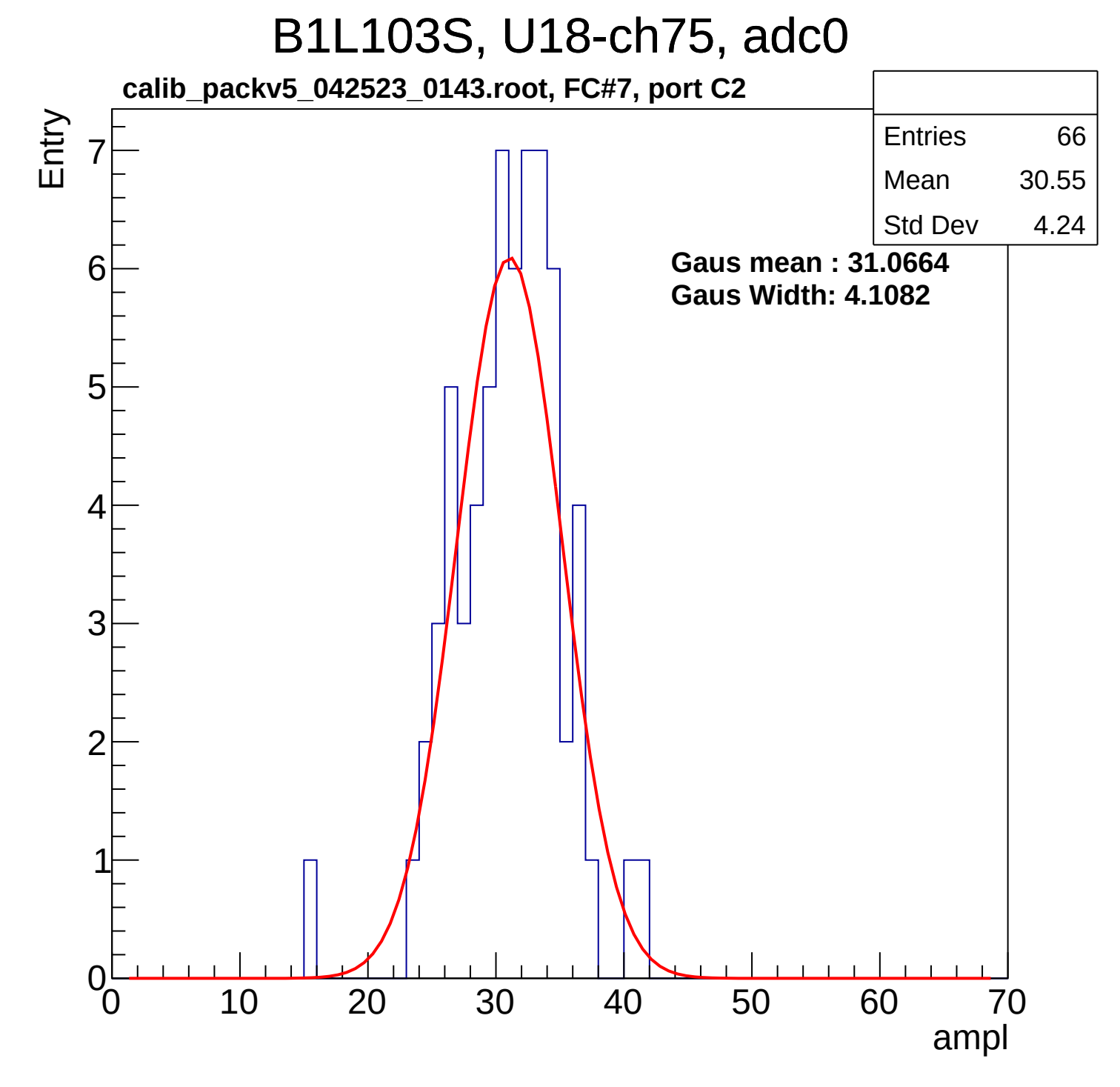
B1L103S, U18-ch75, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 30.55
Std Dev 4.24
Gaus mean : 31.0664
Gaus Width: 4.1082
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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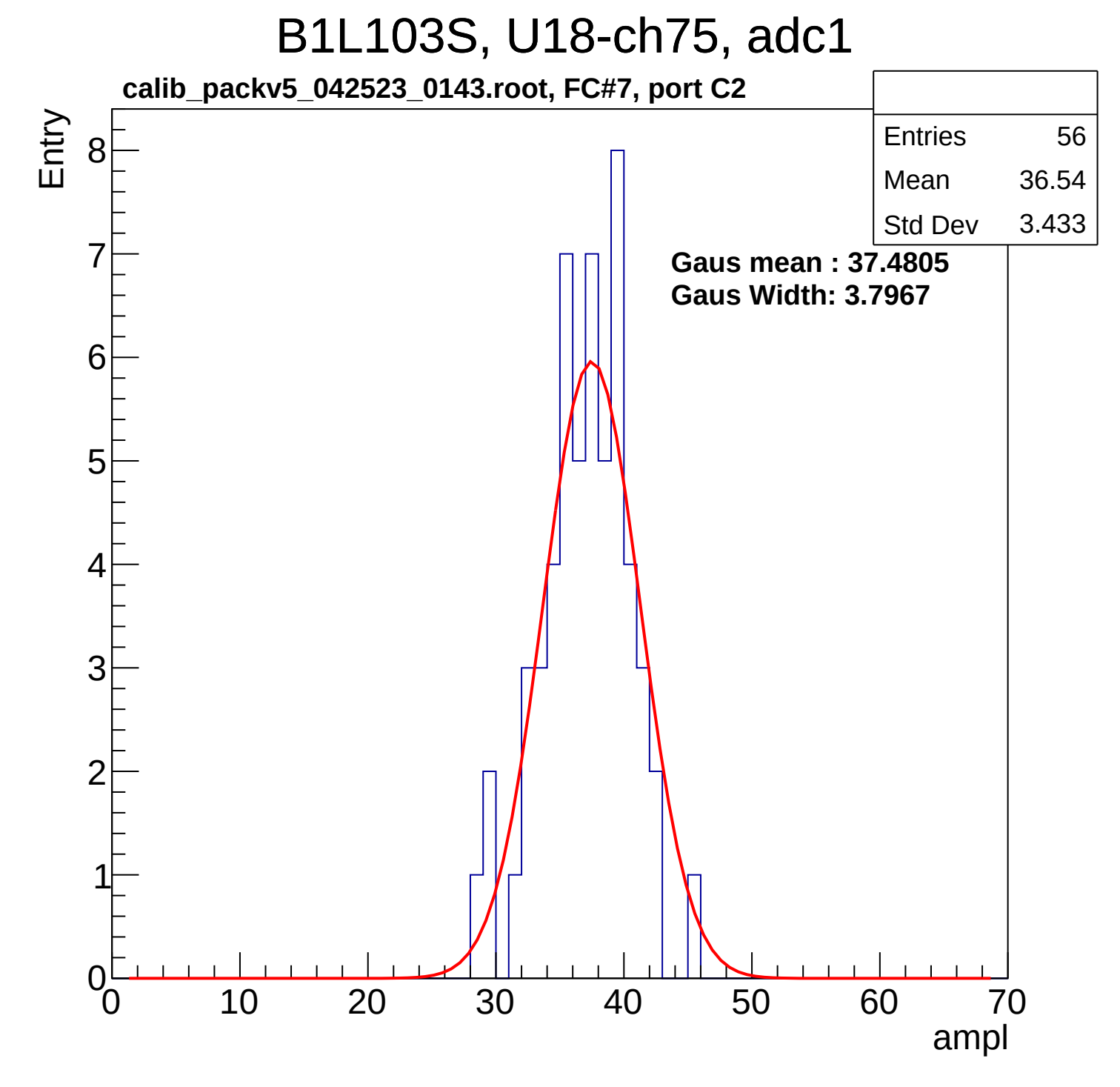
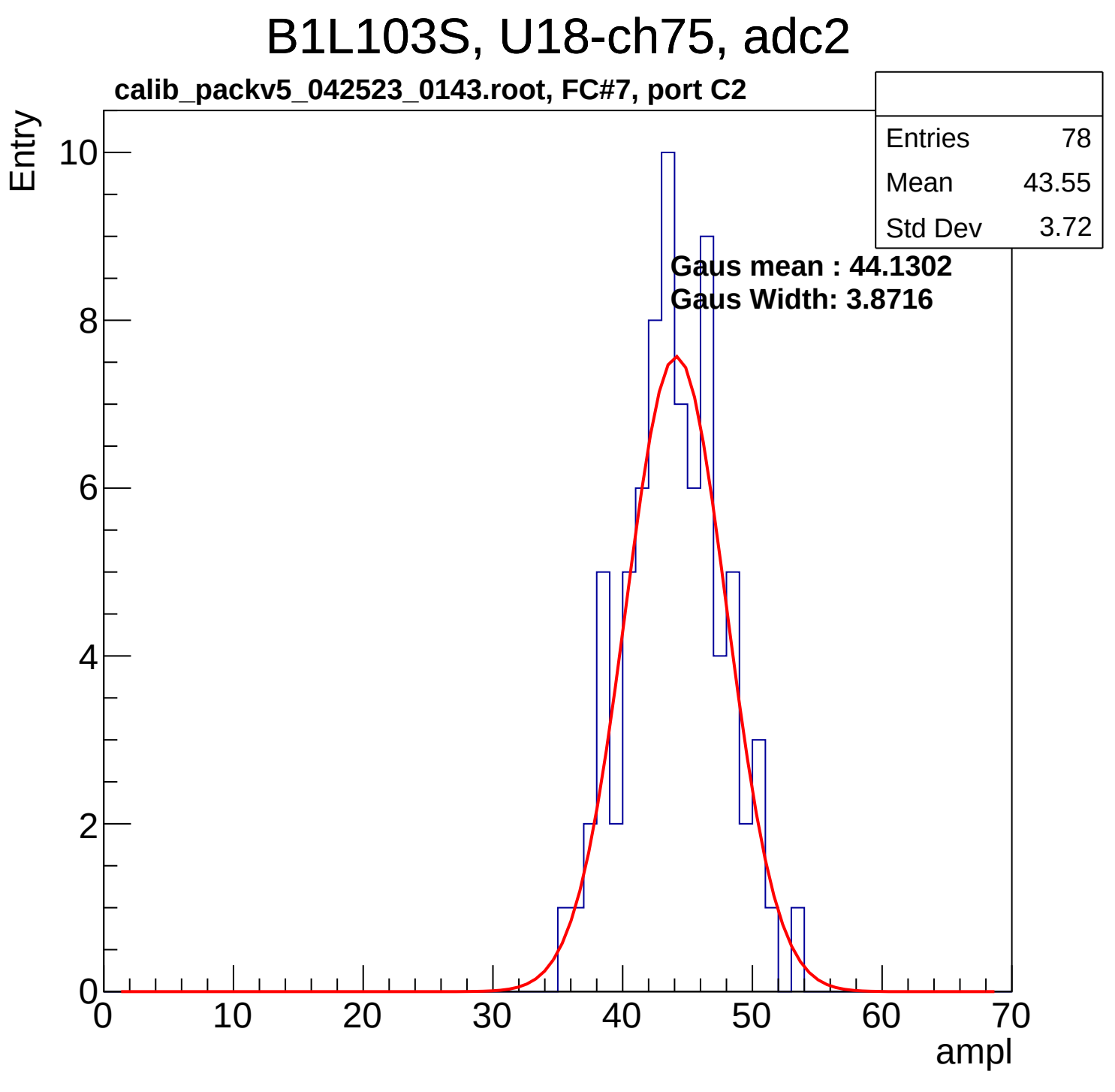
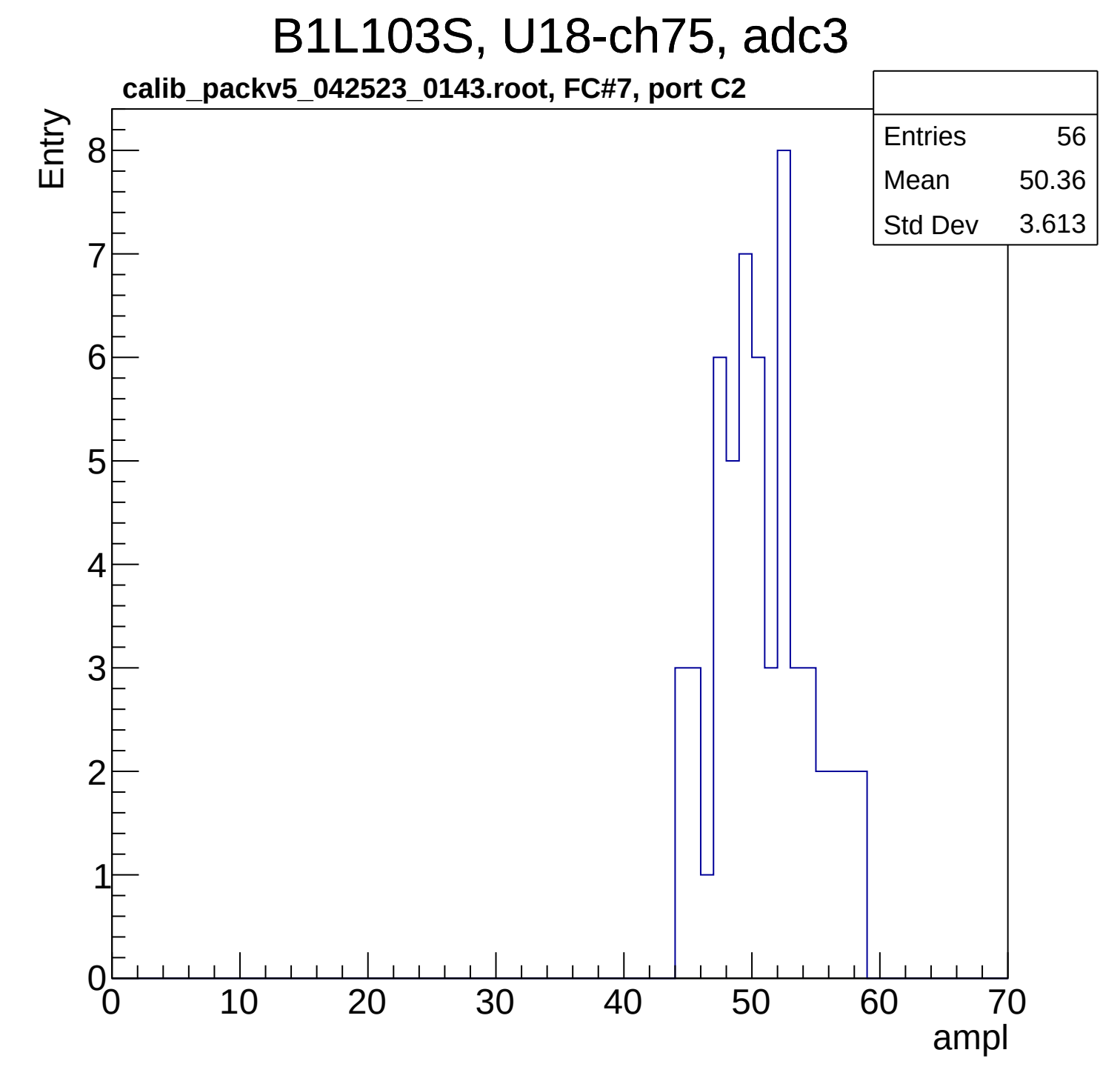

B1L103S, U18-ch75, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 36.54
Std Dev 3.433
Gaus mean : 37.4805
Gaus Width: 3.7967
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch75, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 78
Mean 43.55
Std Dev 3.72
Gaus mean : 44.1302
Gaus Width: 3.8716
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch75, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 50.36
Std Dev 3.613
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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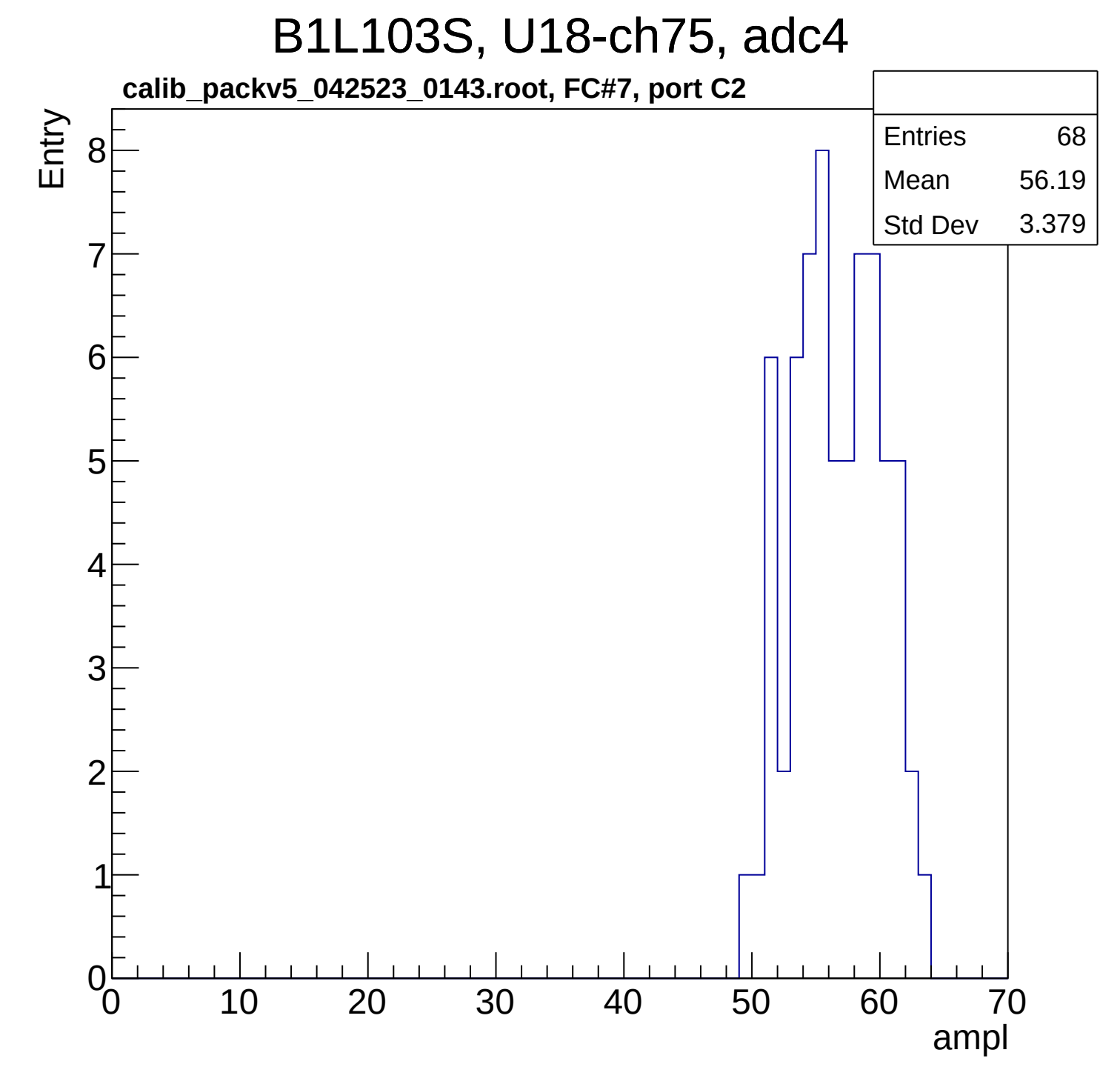
B1L103S, U18-ch75, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 56.19
Std Dev 3.379
Entry
ampl
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1
2
3
4
5
6
7
8
0
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40
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60
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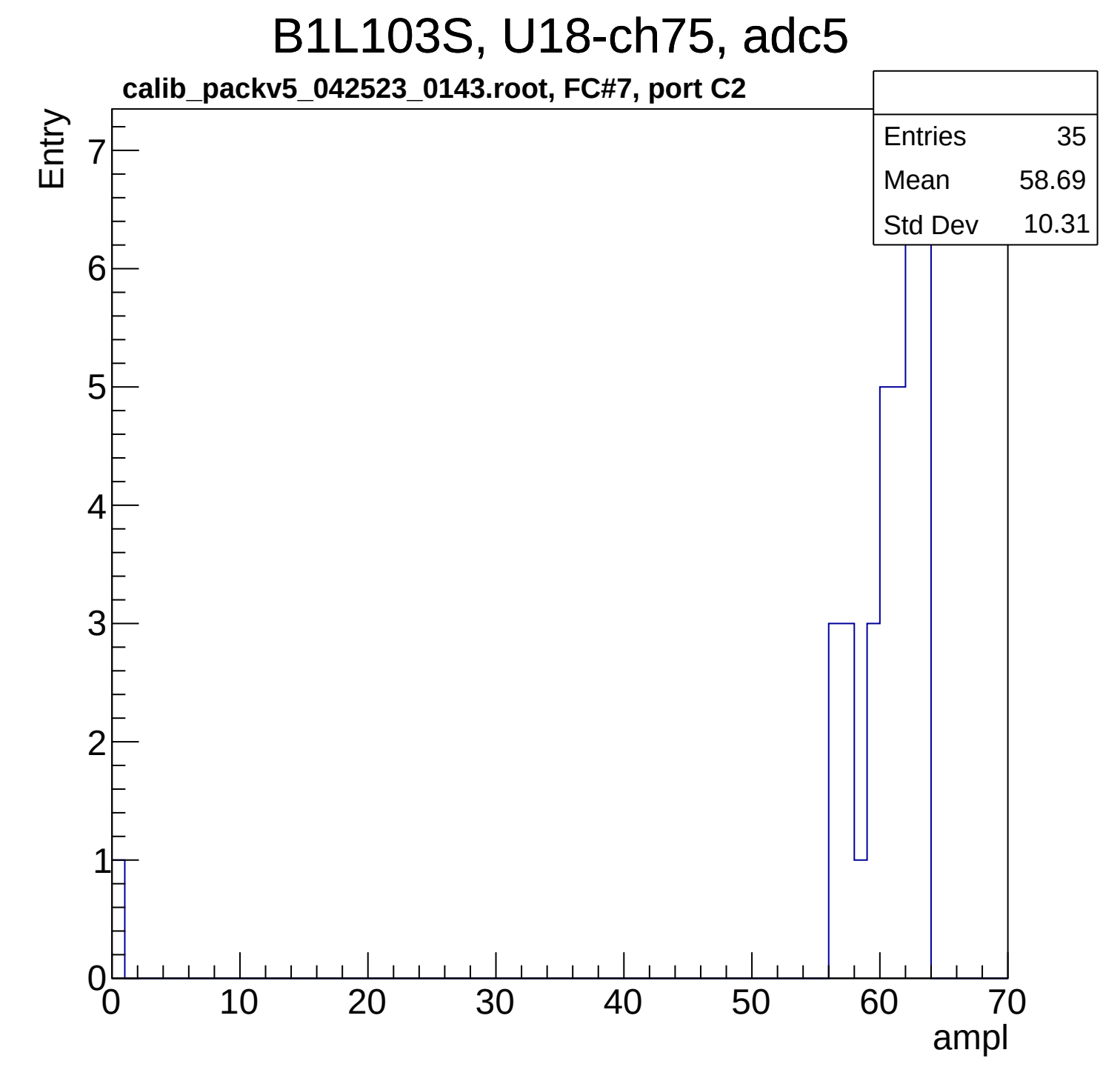
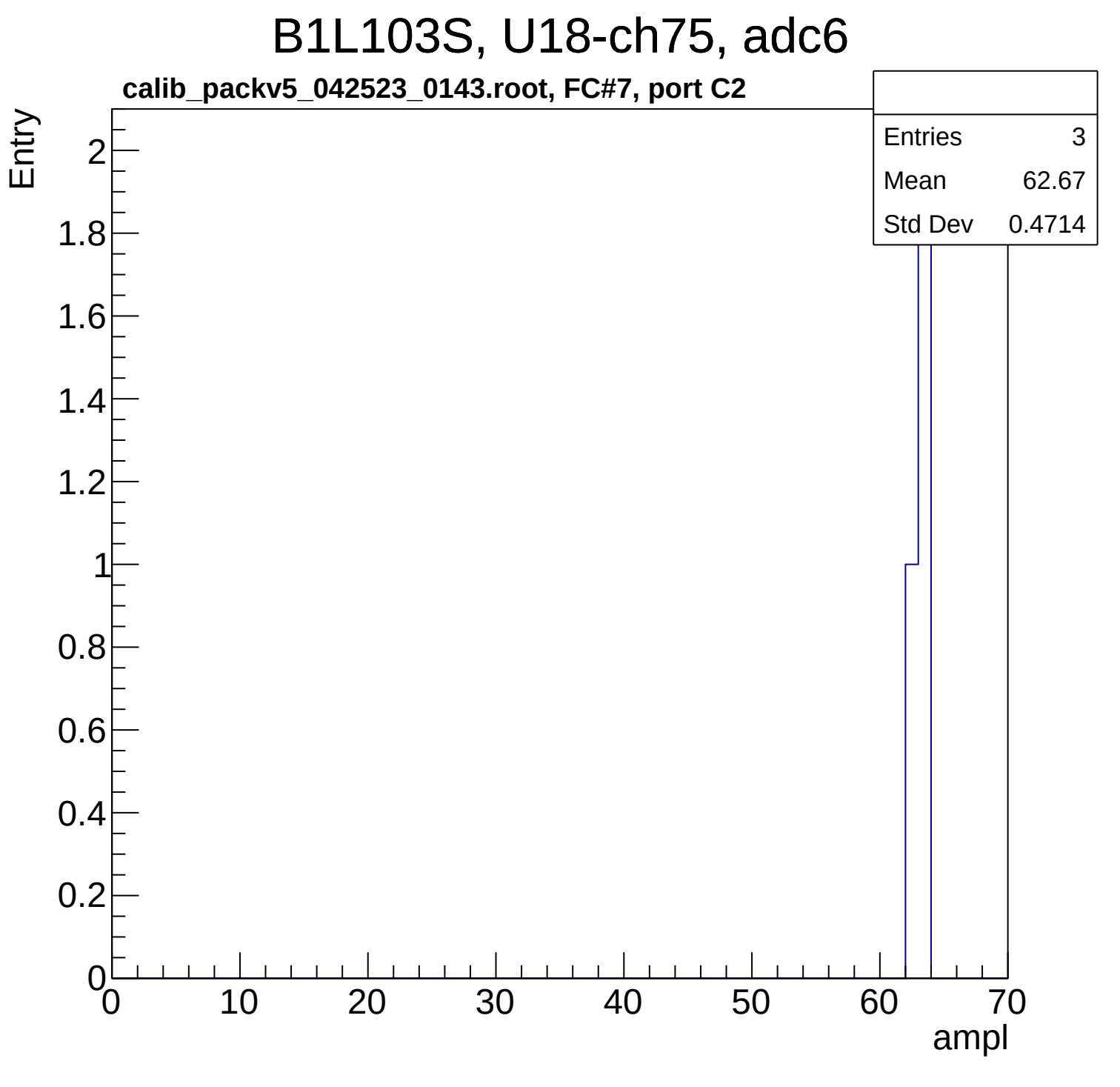
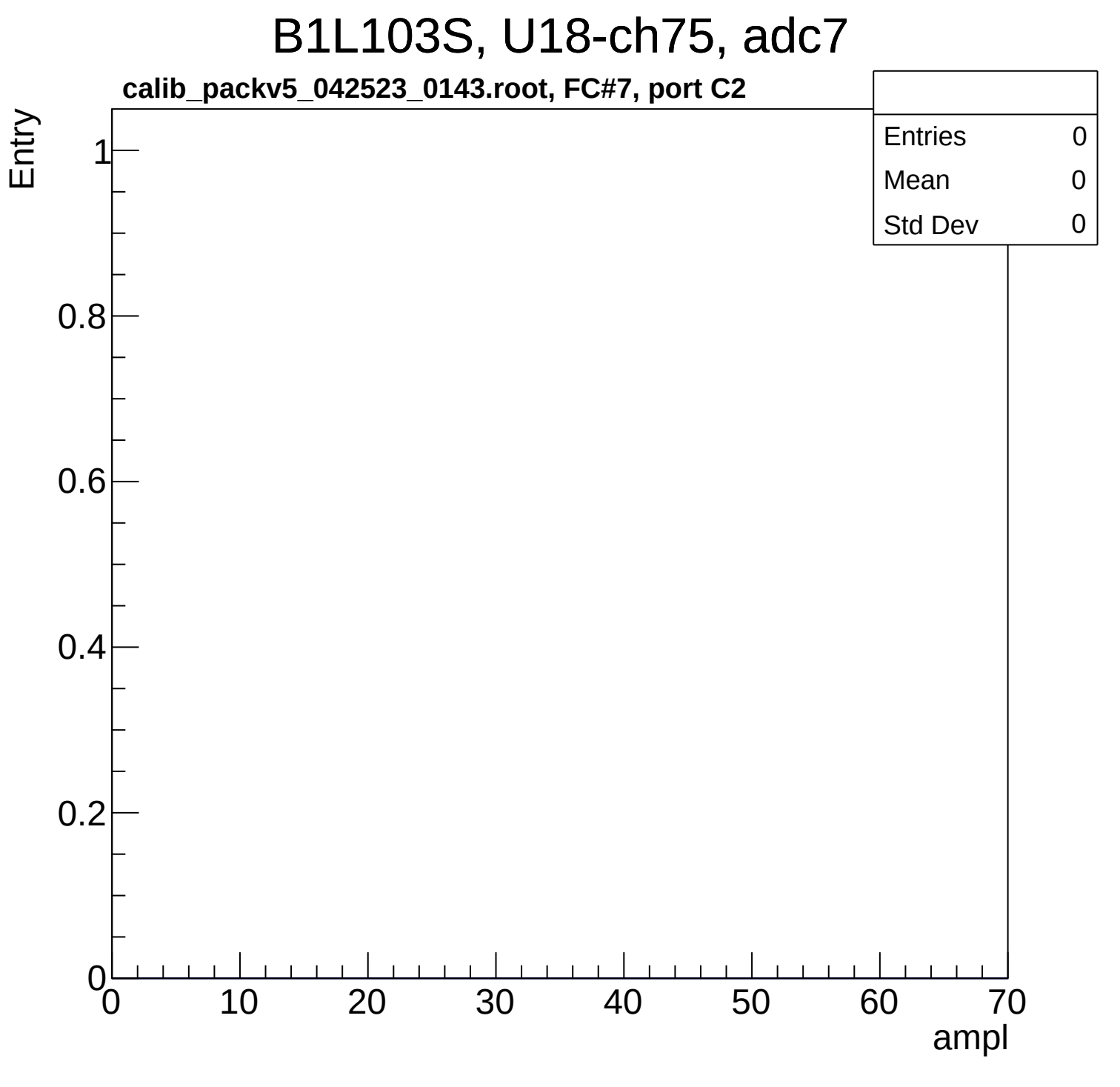
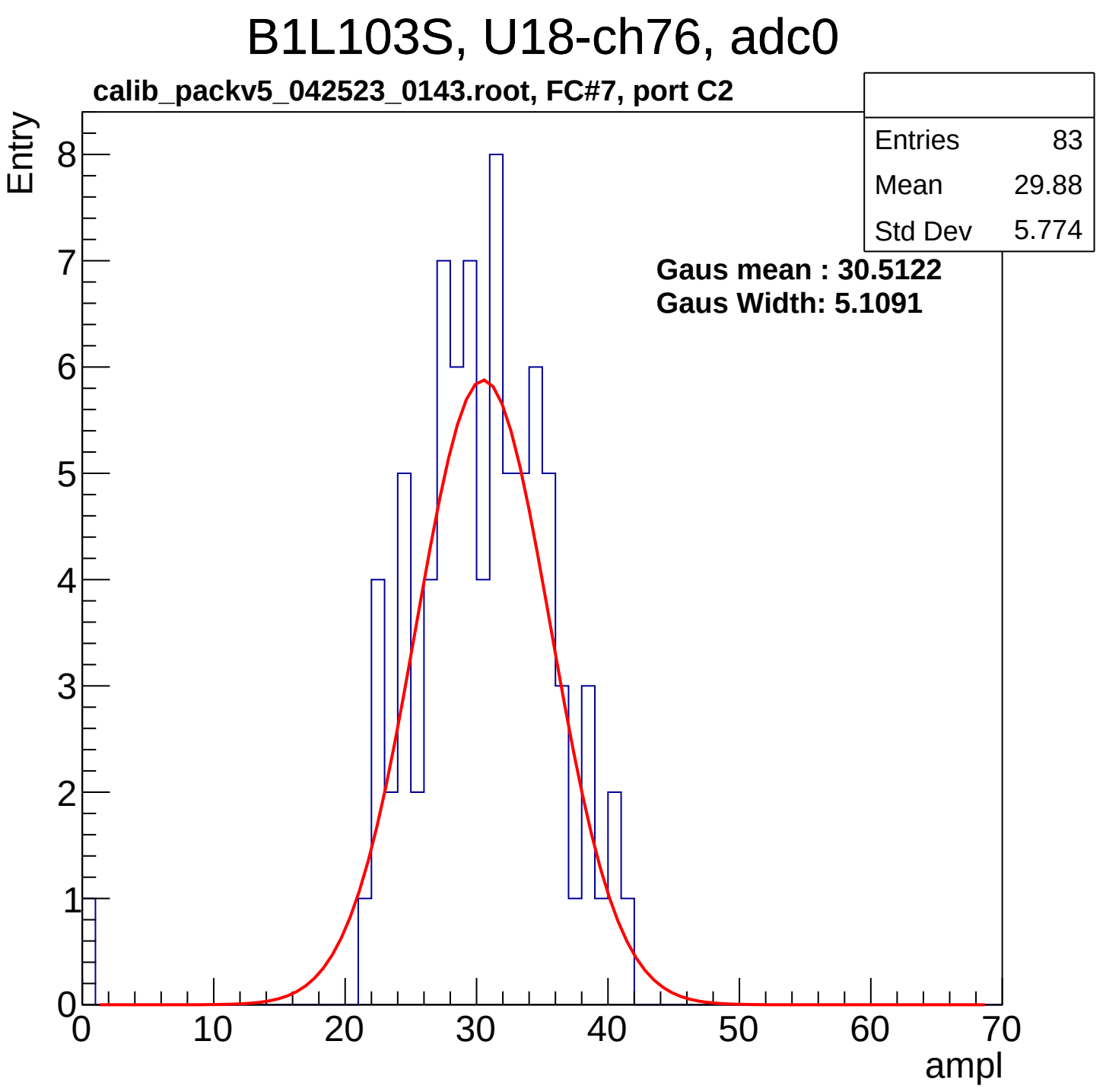

B1L103S, U18-ch75, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 35
Mean 58.69
Std Dev 10.31
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch75, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 62.67
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U18-ch75, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch76, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 83
Mean 29.88
Std Dev 5.774
Gaus mean : 30.5122
Gaus Width: 5.1091
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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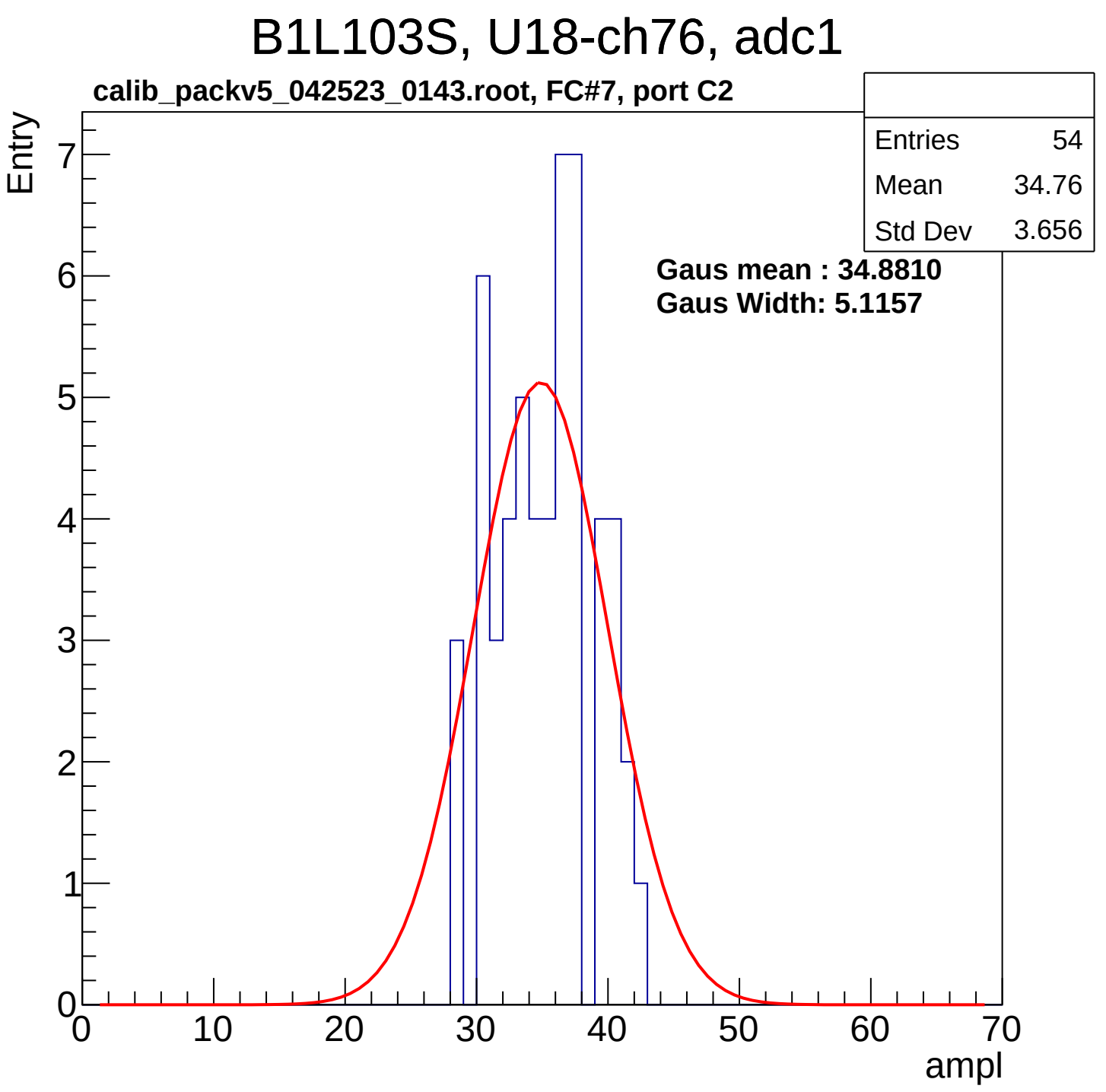
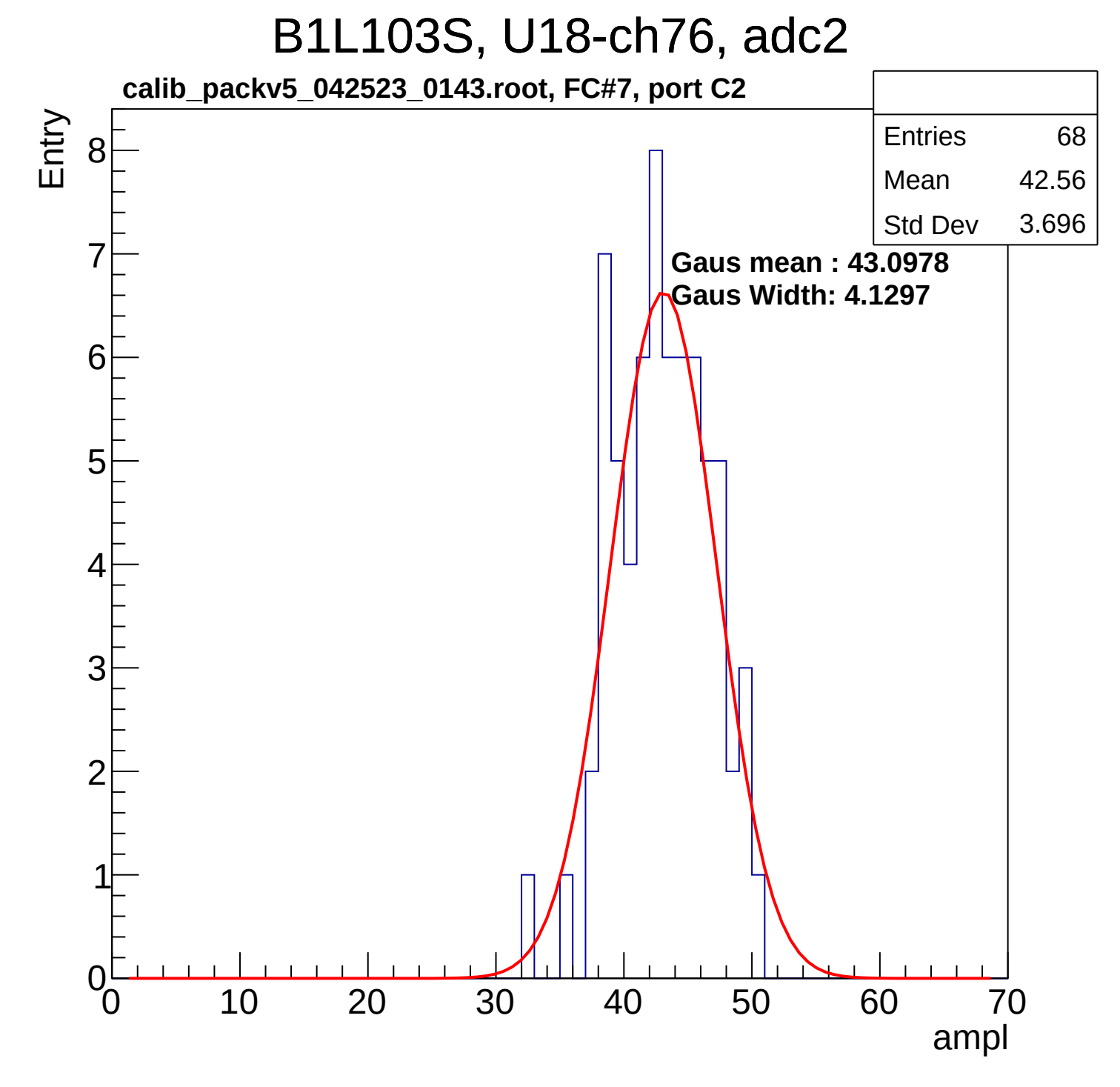
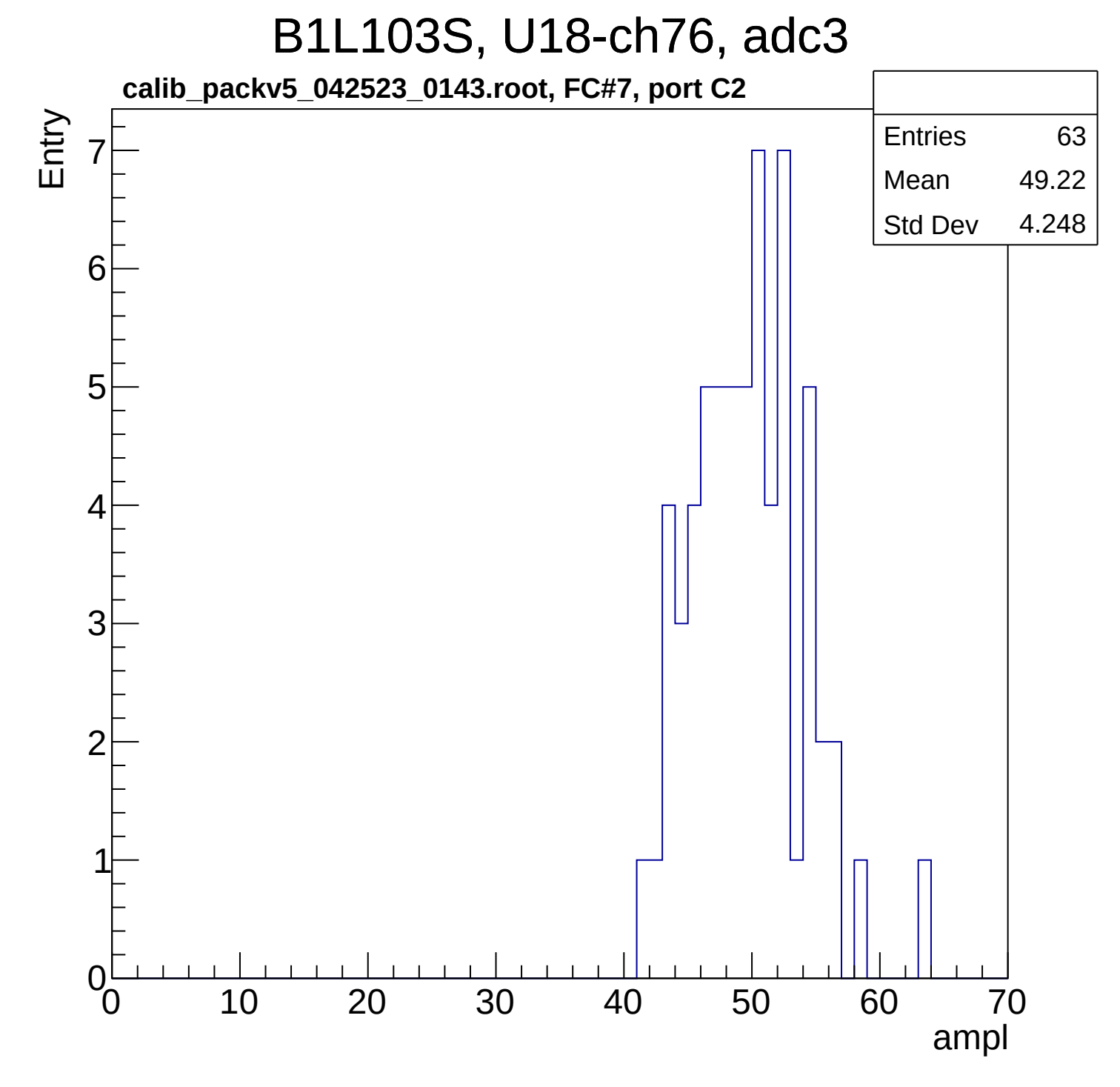

B1L103S, U18-ch76, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 54
Mean 34.76
Std Dev 3.656
Gaus mean : 34.8810
Gaus Width: 5.1157
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch76, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 42.56
Std Dev 3.696
Gaus mean : 43.0978
Gaus Width: 4.1297
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch76, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 49.22
Std Dev 4.248
Entry
ampl
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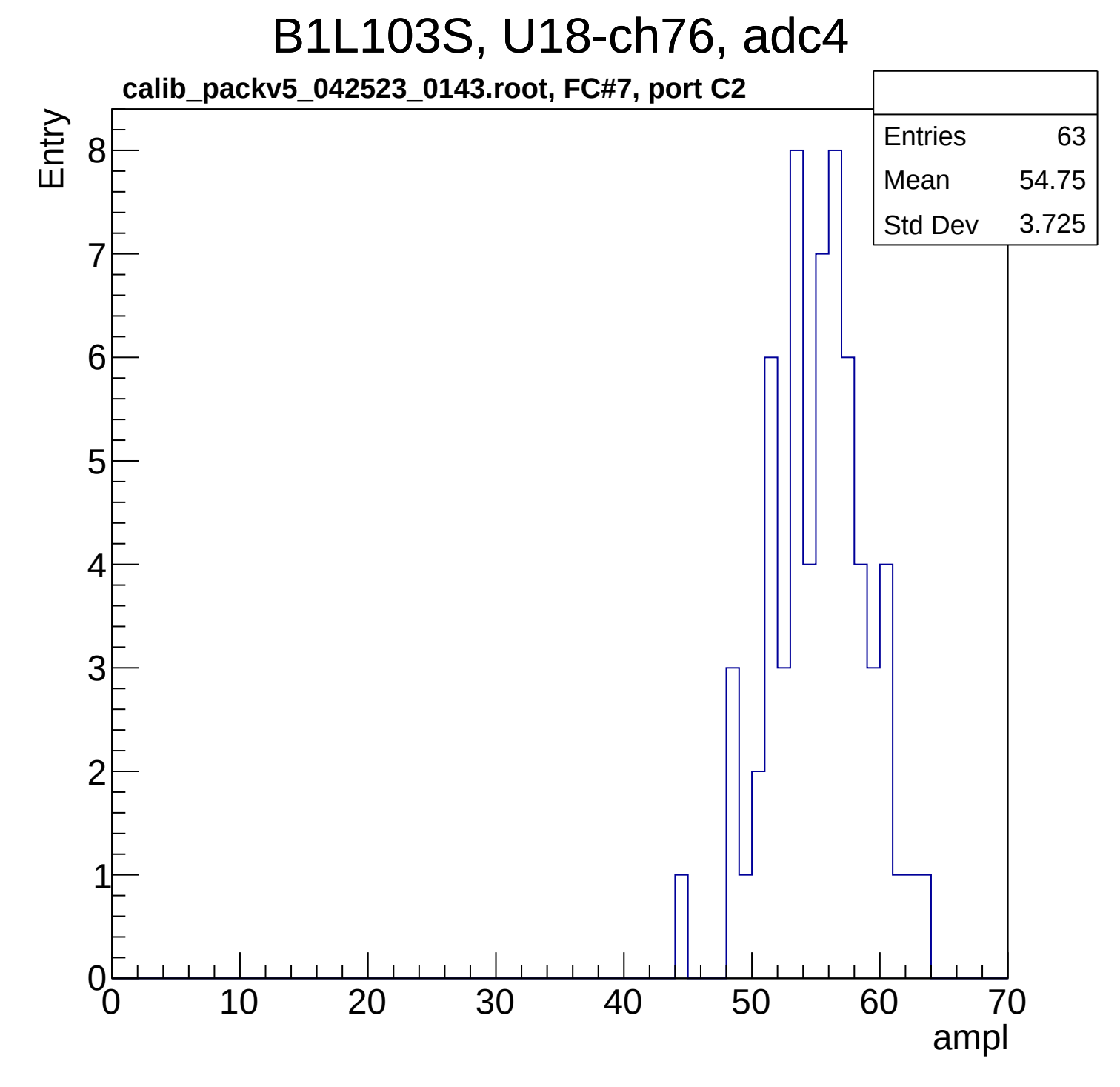
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch76, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 54.75
Std Dev 3.725
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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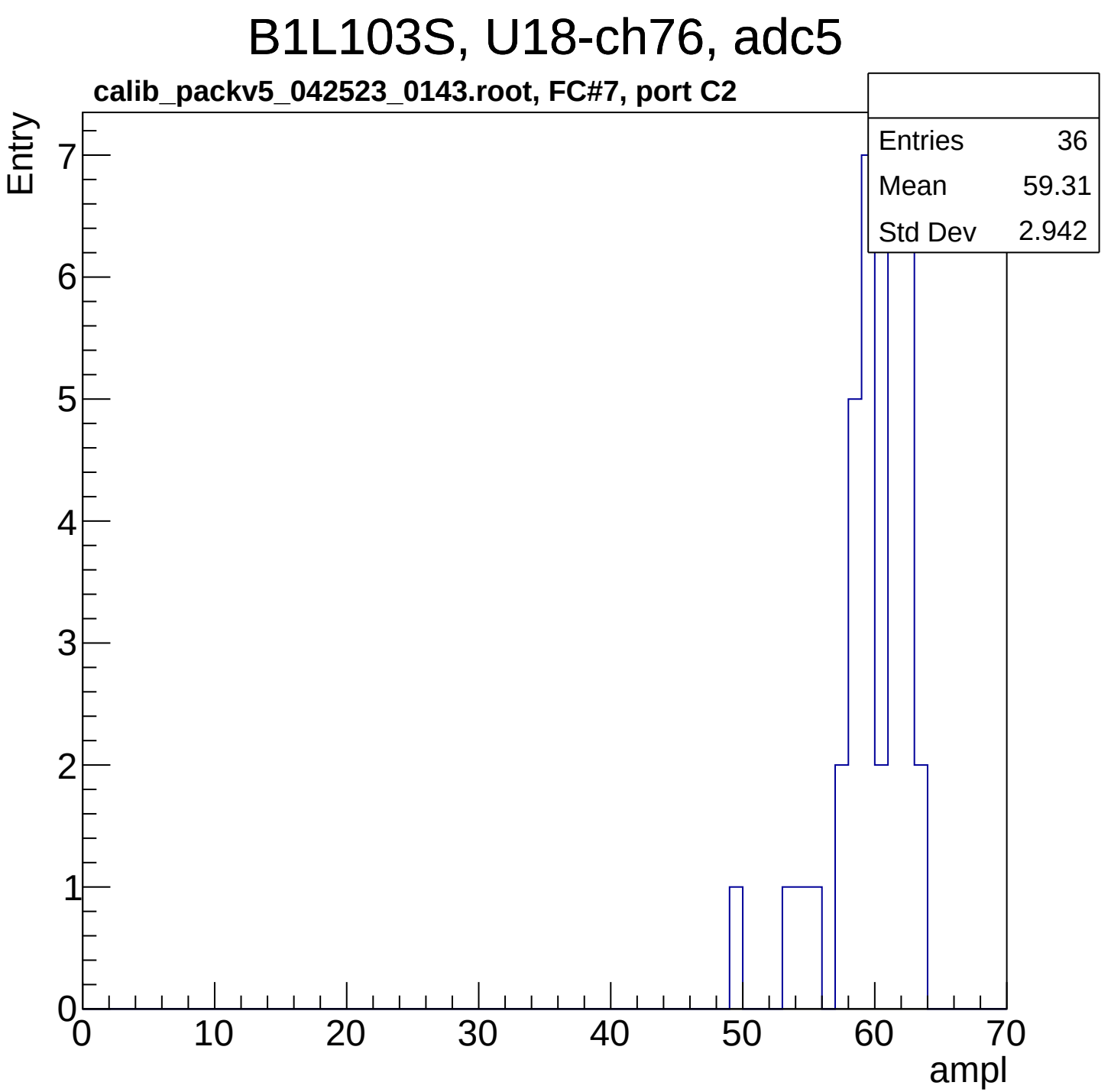
B1L103S, U18-ch76, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 36
Mean 59.31
Std Dev 2.942
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
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60
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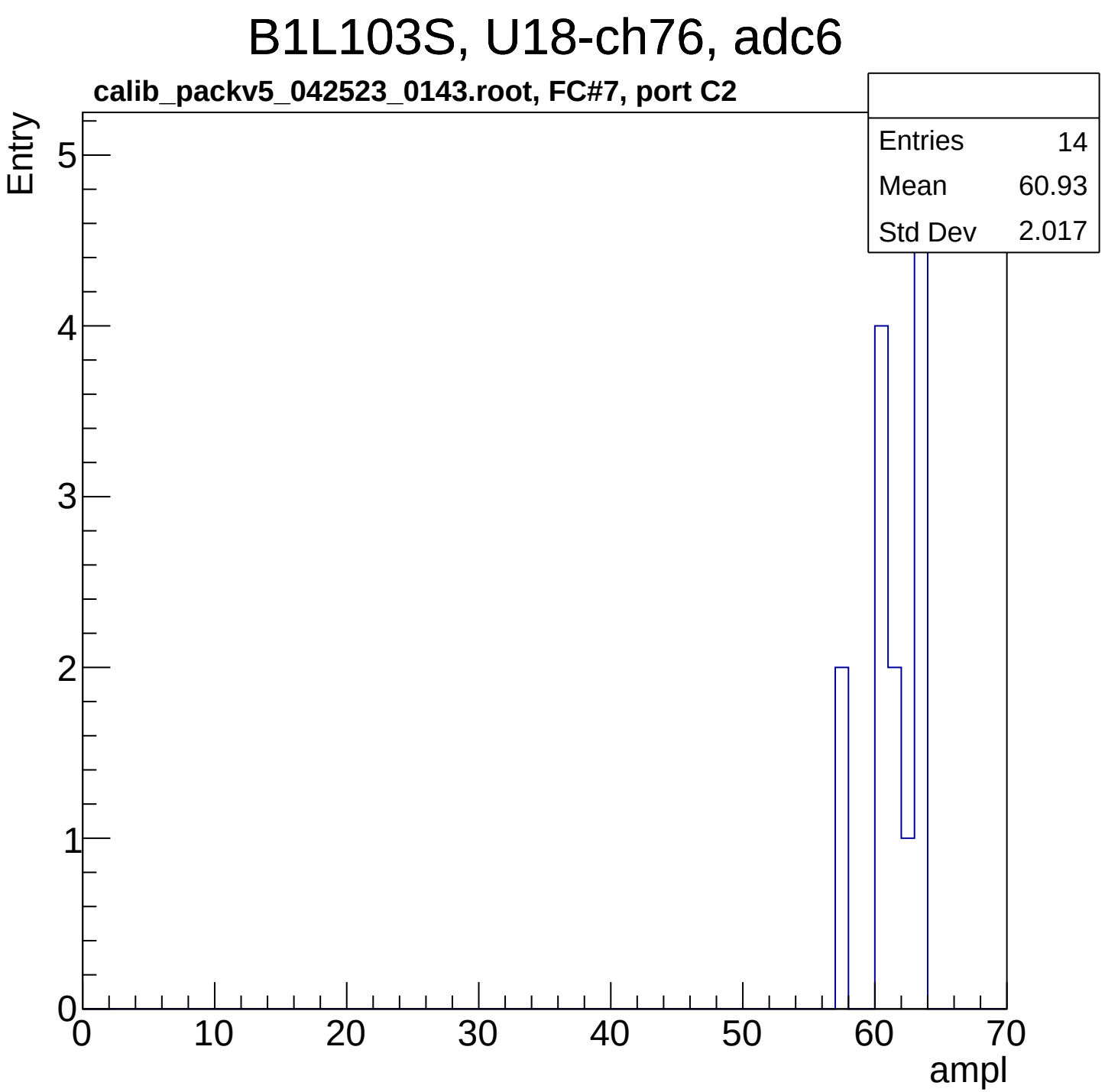
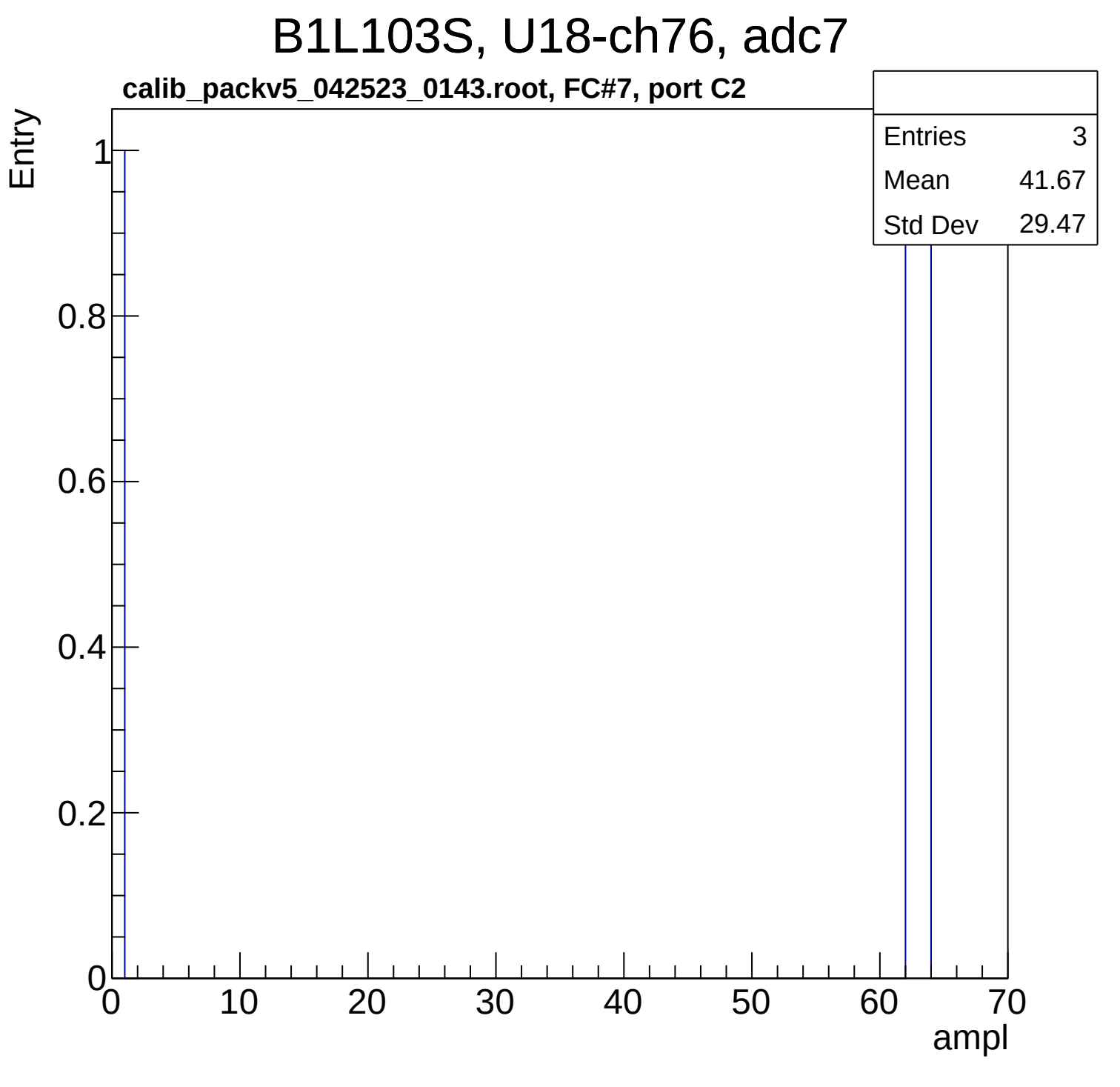
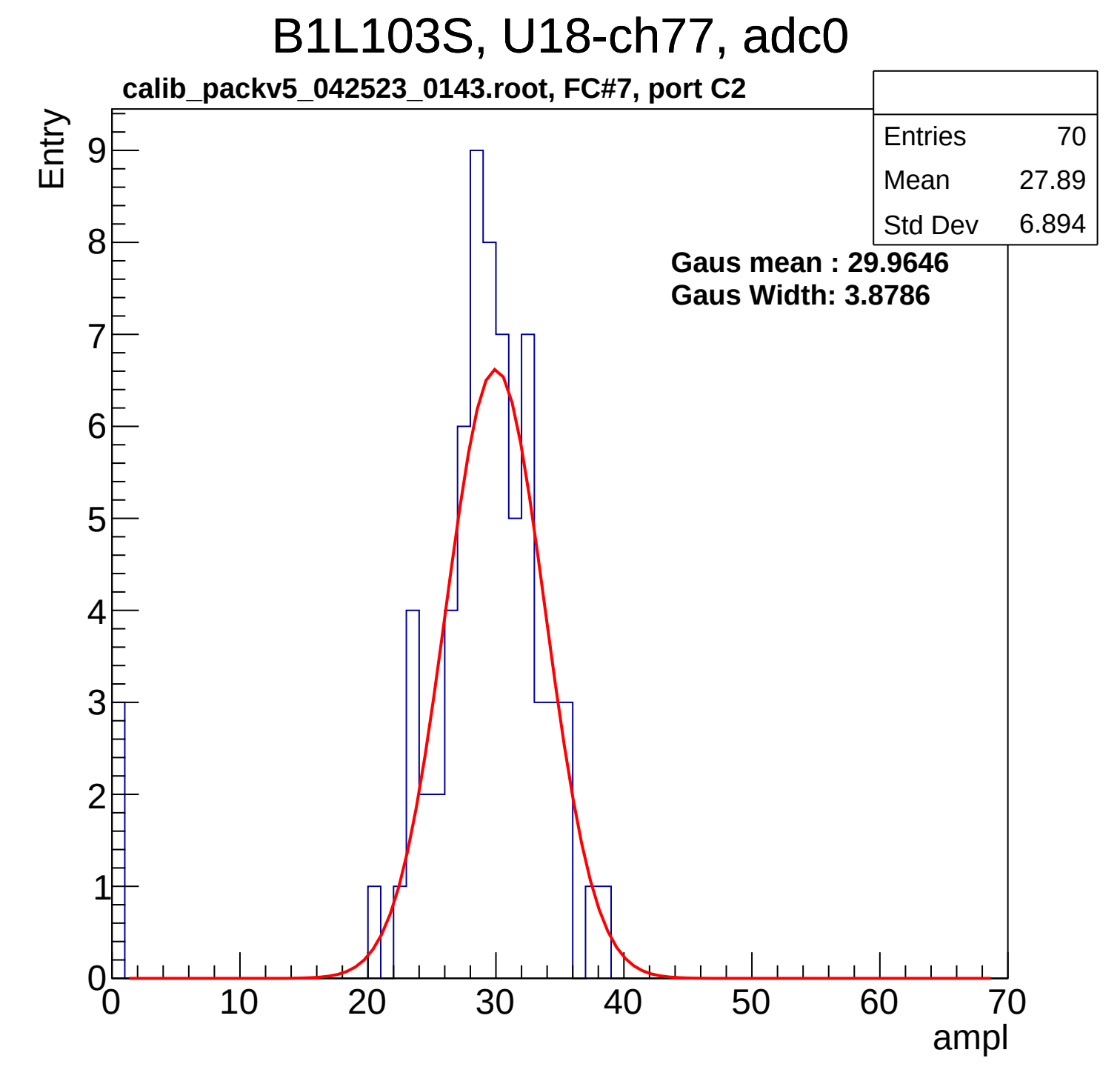

B1L103S, U18-ch76, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 14
Mean 60.93
Std Dev 2.017
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch76, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 41.67
Std Dev 29.47
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch77, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 27.89
Std Dev 6.894
Gaus mean : 29.9646
Gaus Width: 3.8786
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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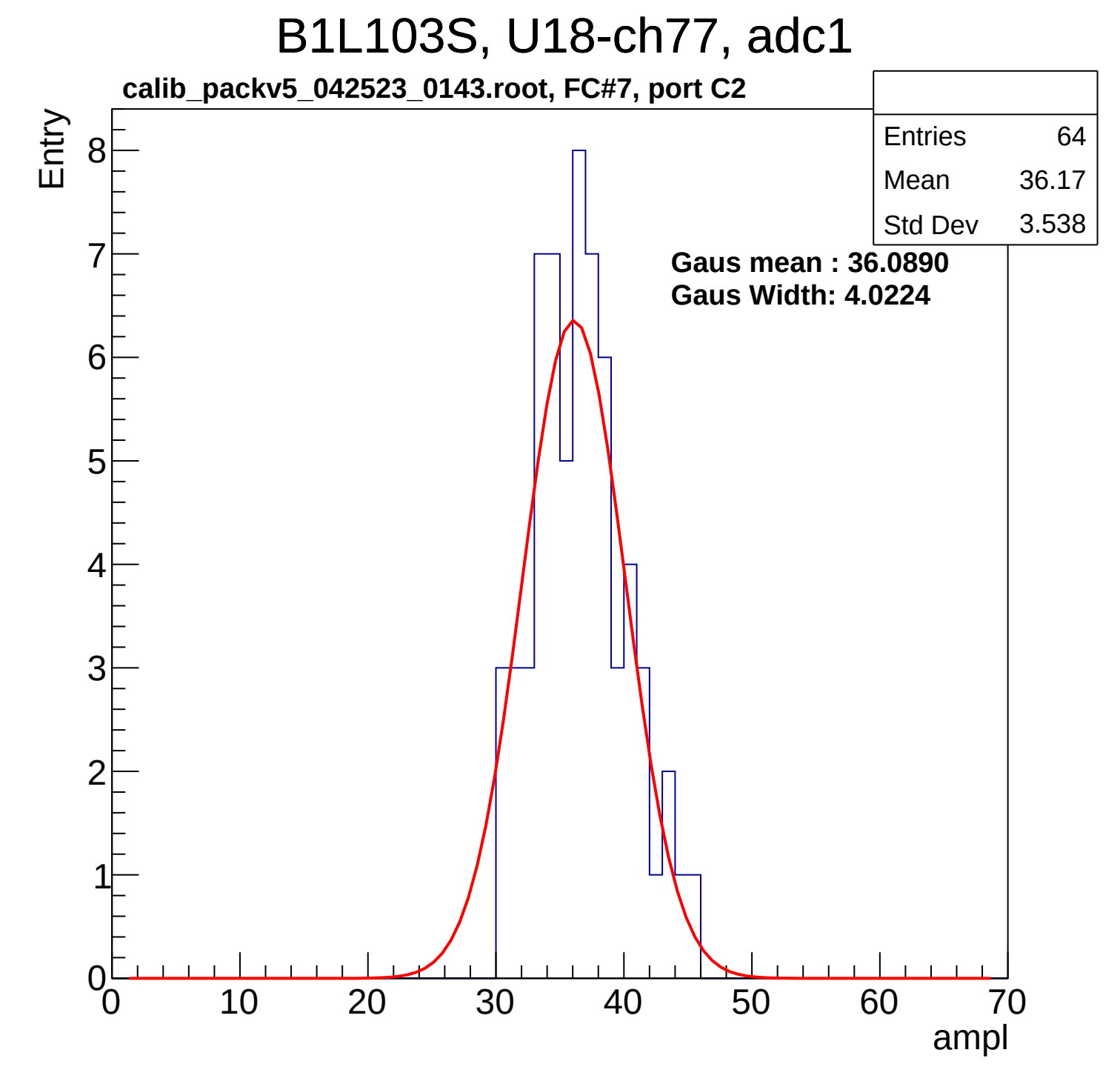
B1L103S, U18-ch77, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 36.17
Std Dev 3.538
Gaus mean : 36.0890
Gaus Width: 4.0224
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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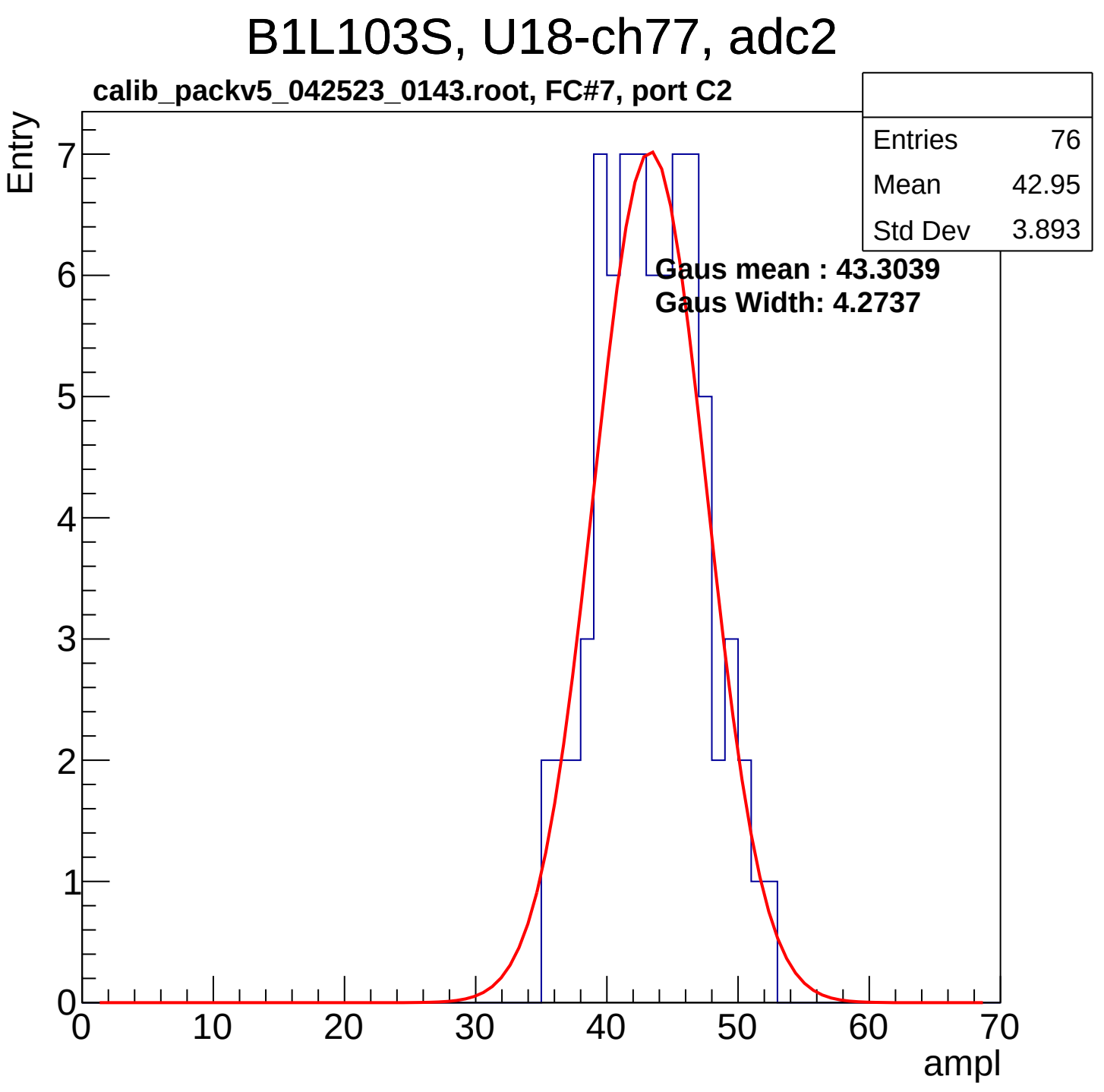
B1L103S, U18-ch77, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 76
Mean 42.95
Std Dev 3.893
Gaus mean : 43.3039
Gaus Width: 4.2737
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
50
60
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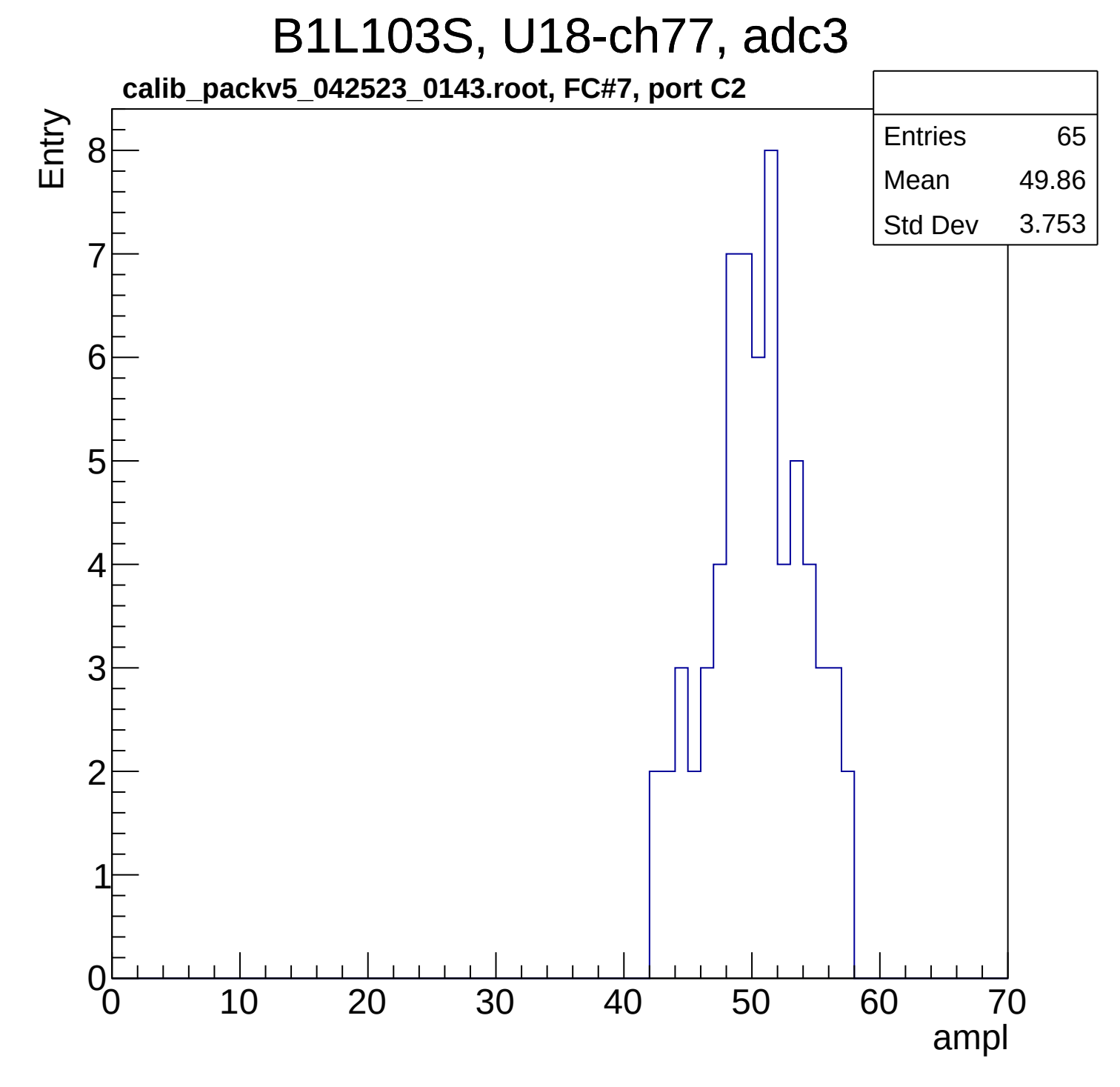
B1L103S, U18-ch77, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 49.86
Std Dev 3.753
Entry
ampl
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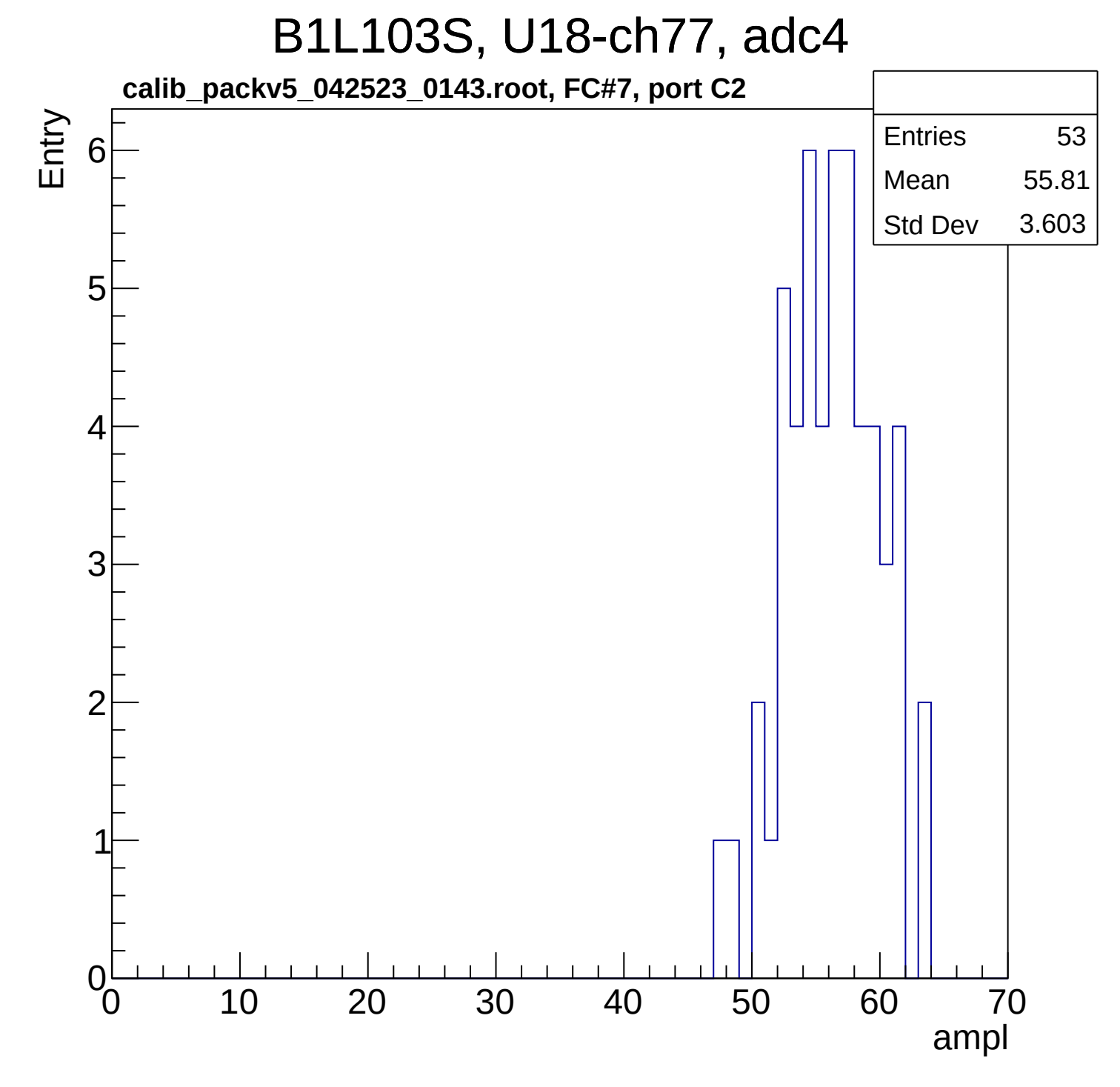
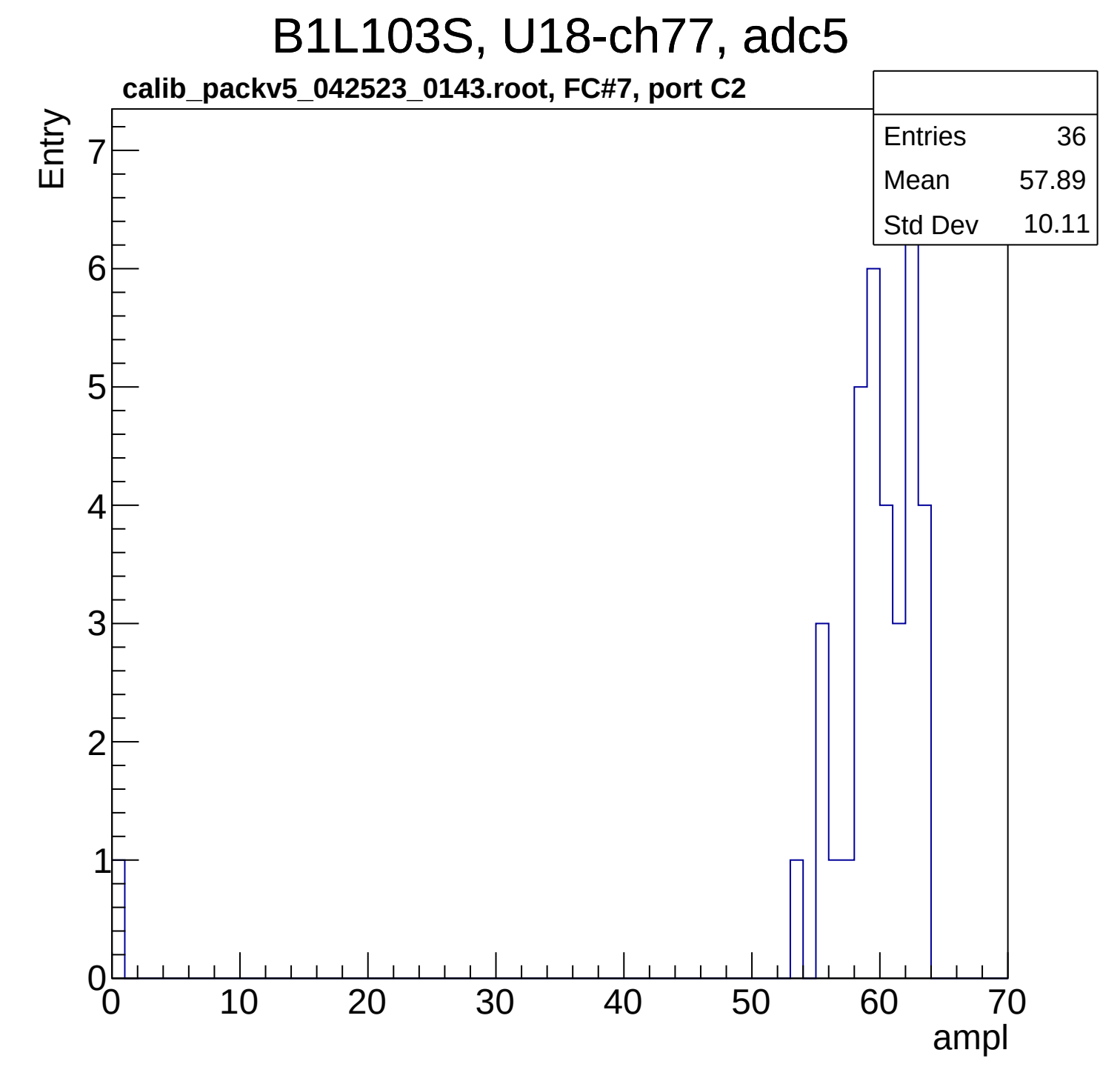
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch77, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 55.81
Std Dev 3.603
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U18-ch77, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 36
Mean 57.89
Std Dev 10.11
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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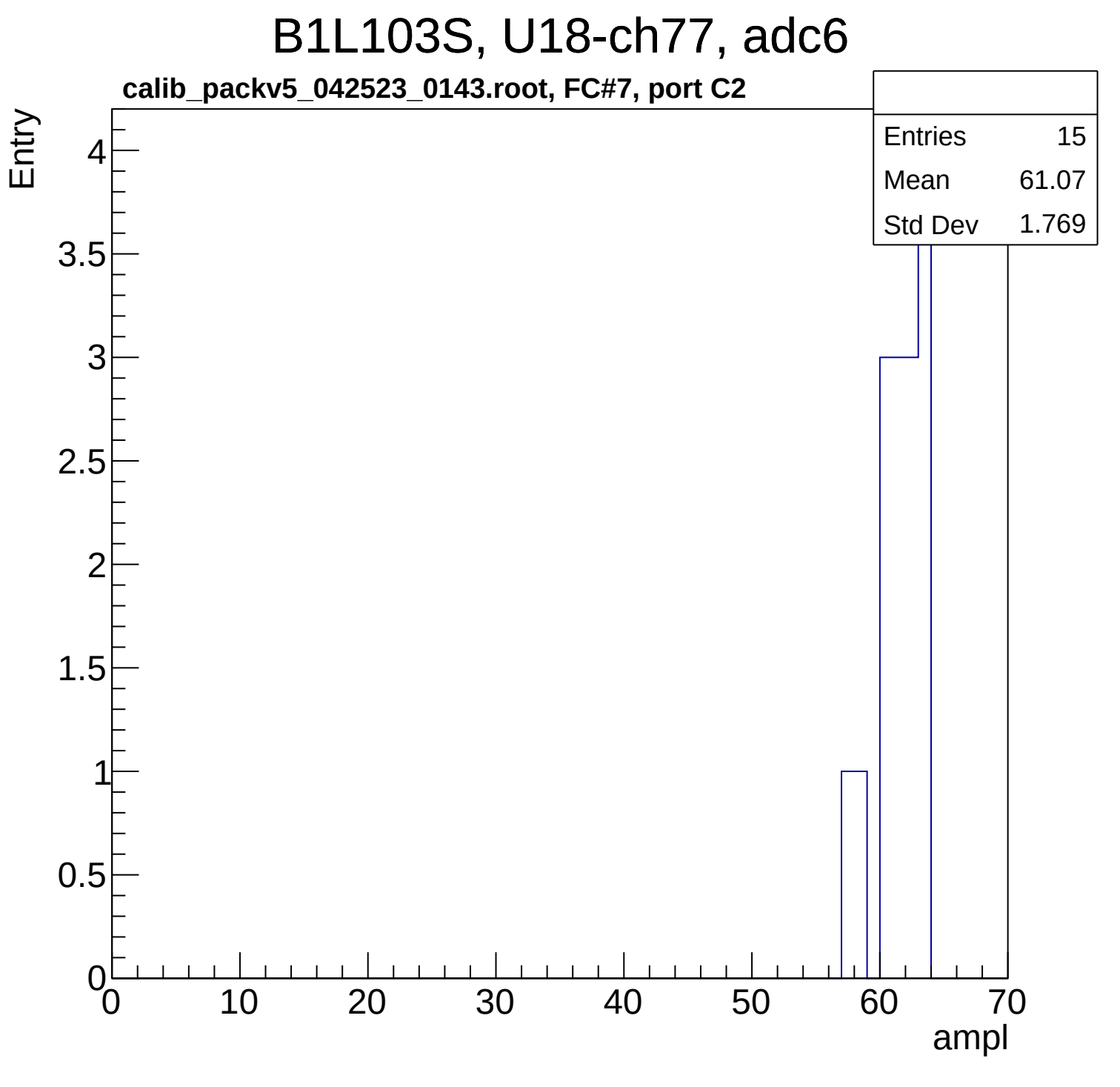
B1L103S, U18-ch77, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 15
Mean 61.07
Std Dev 1.769
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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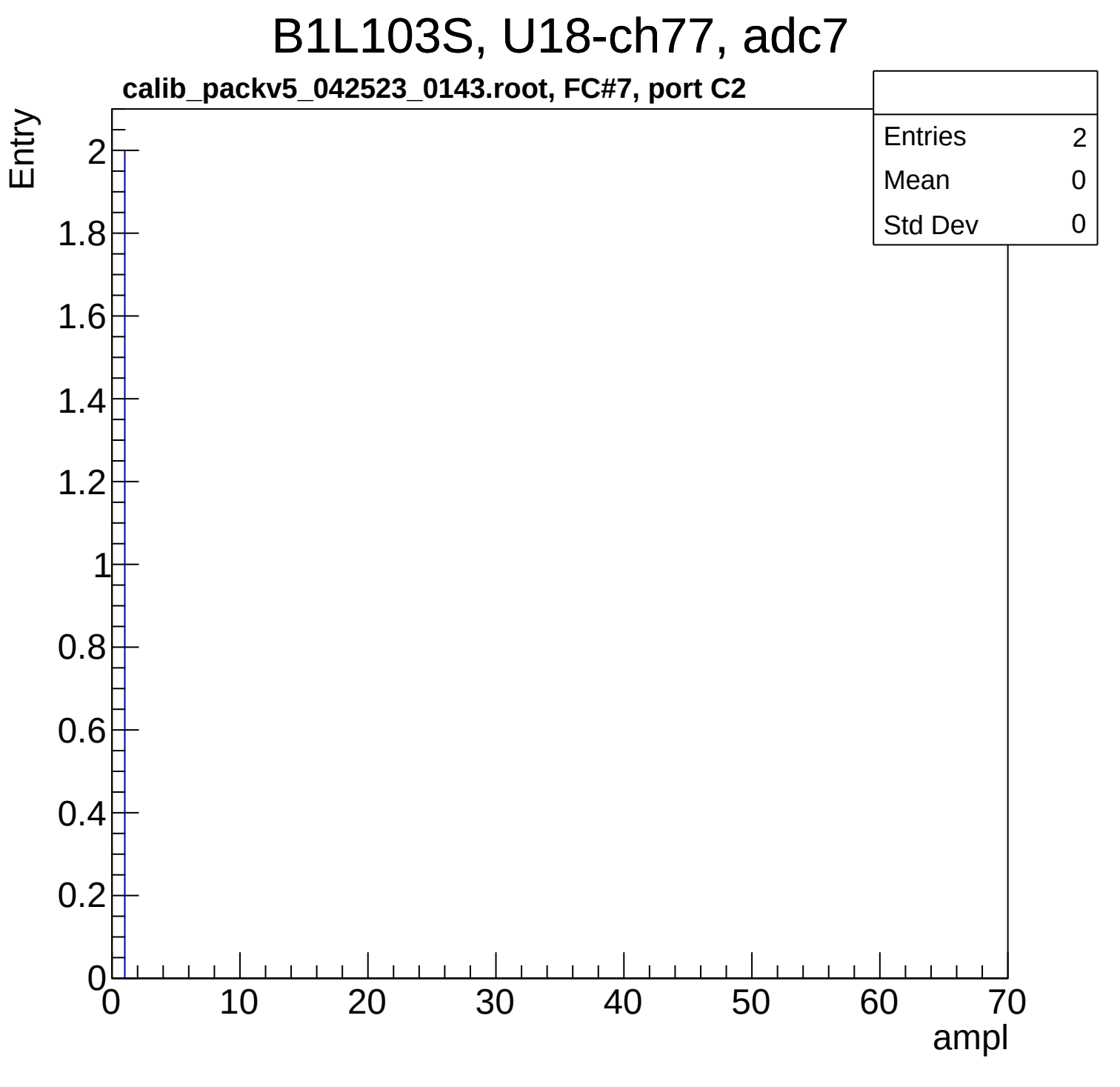
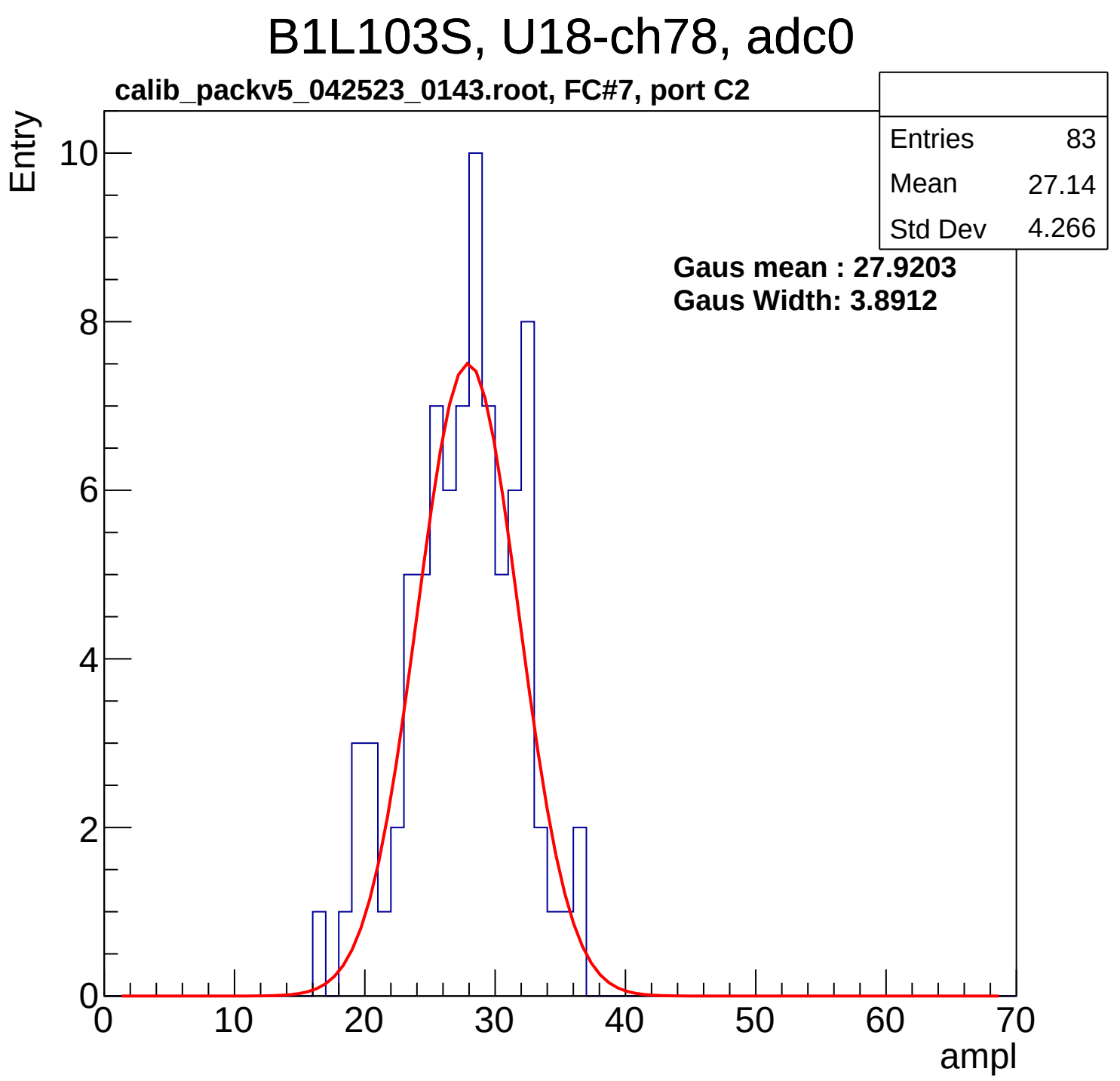
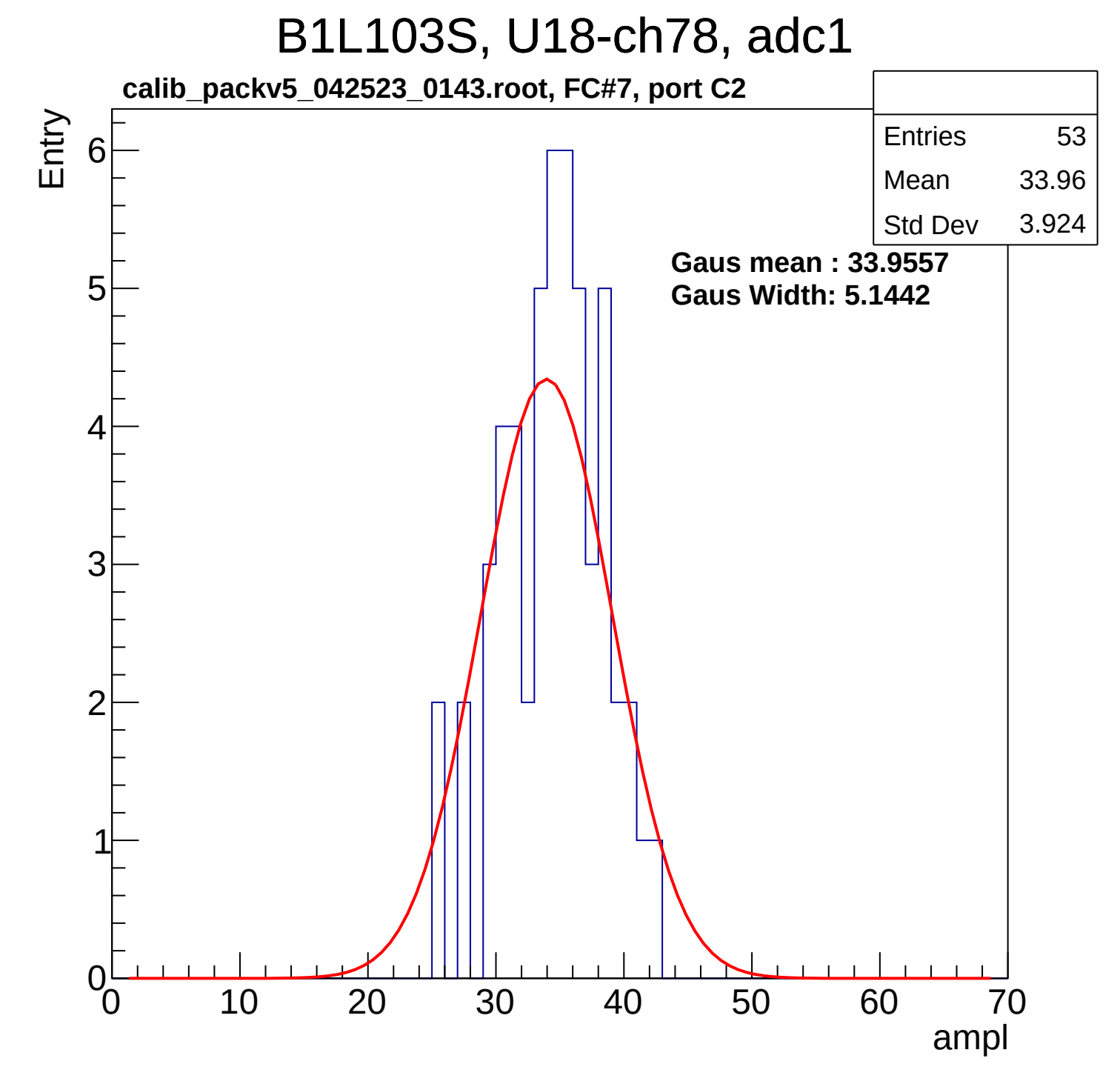
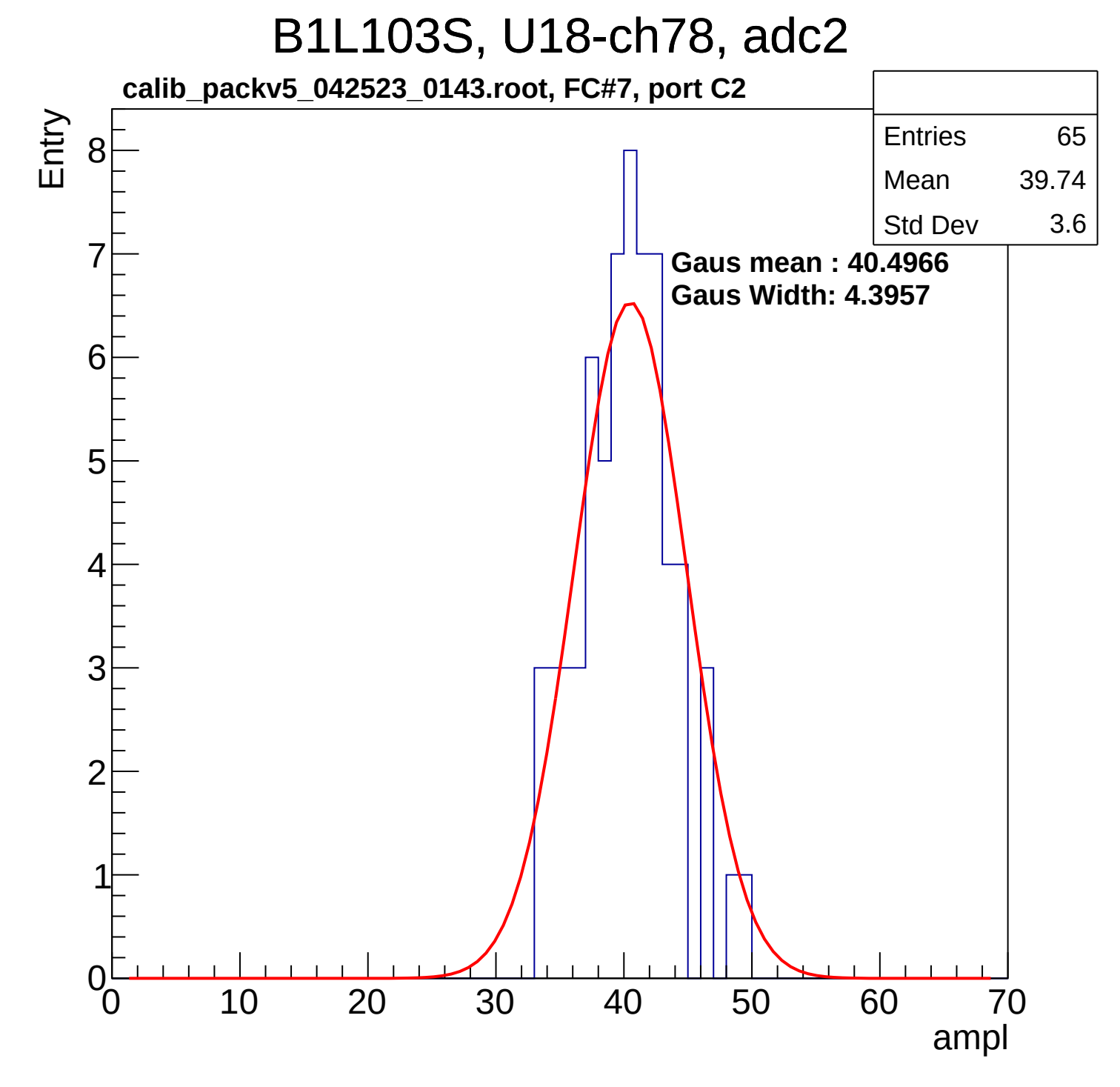
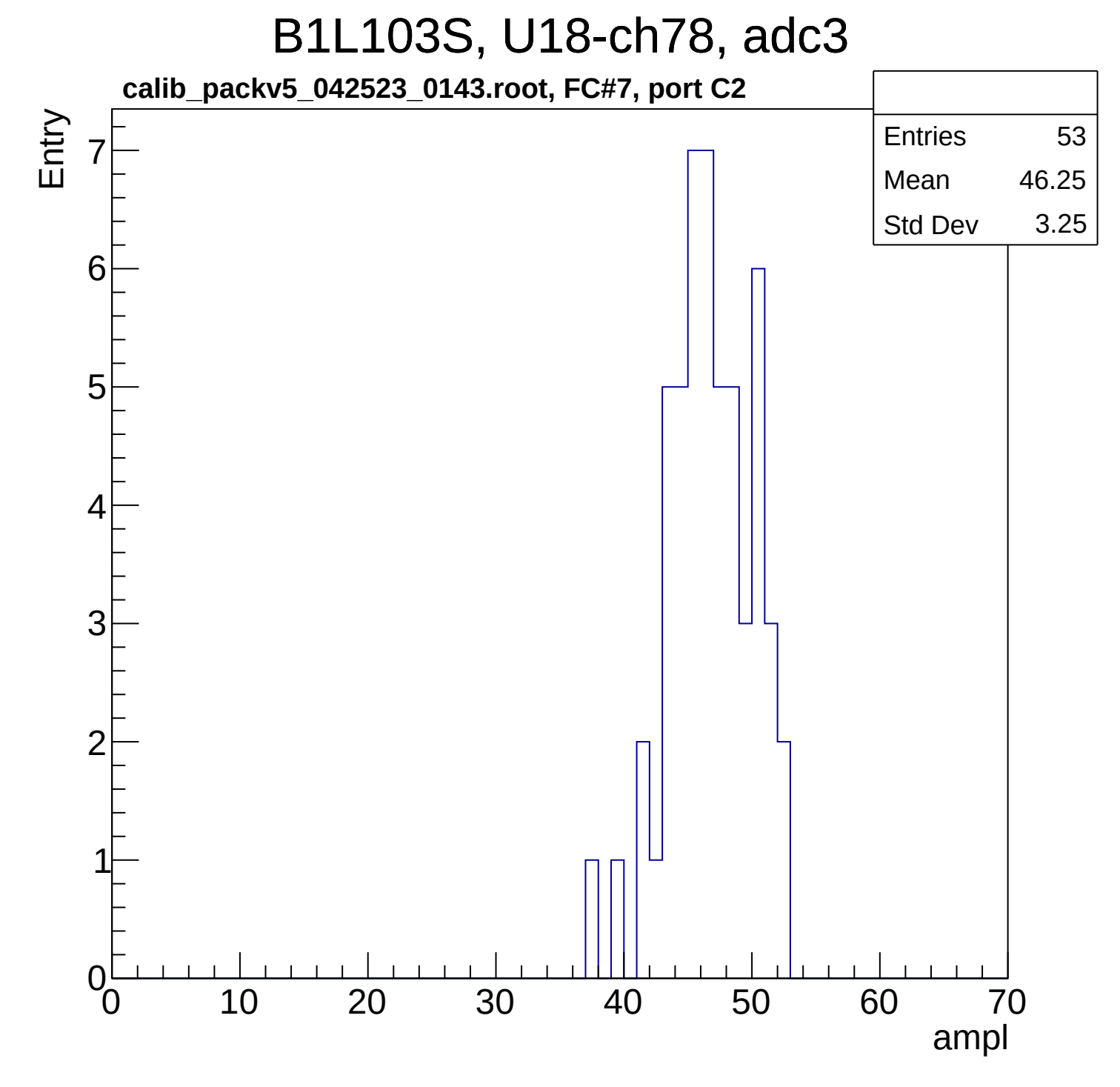
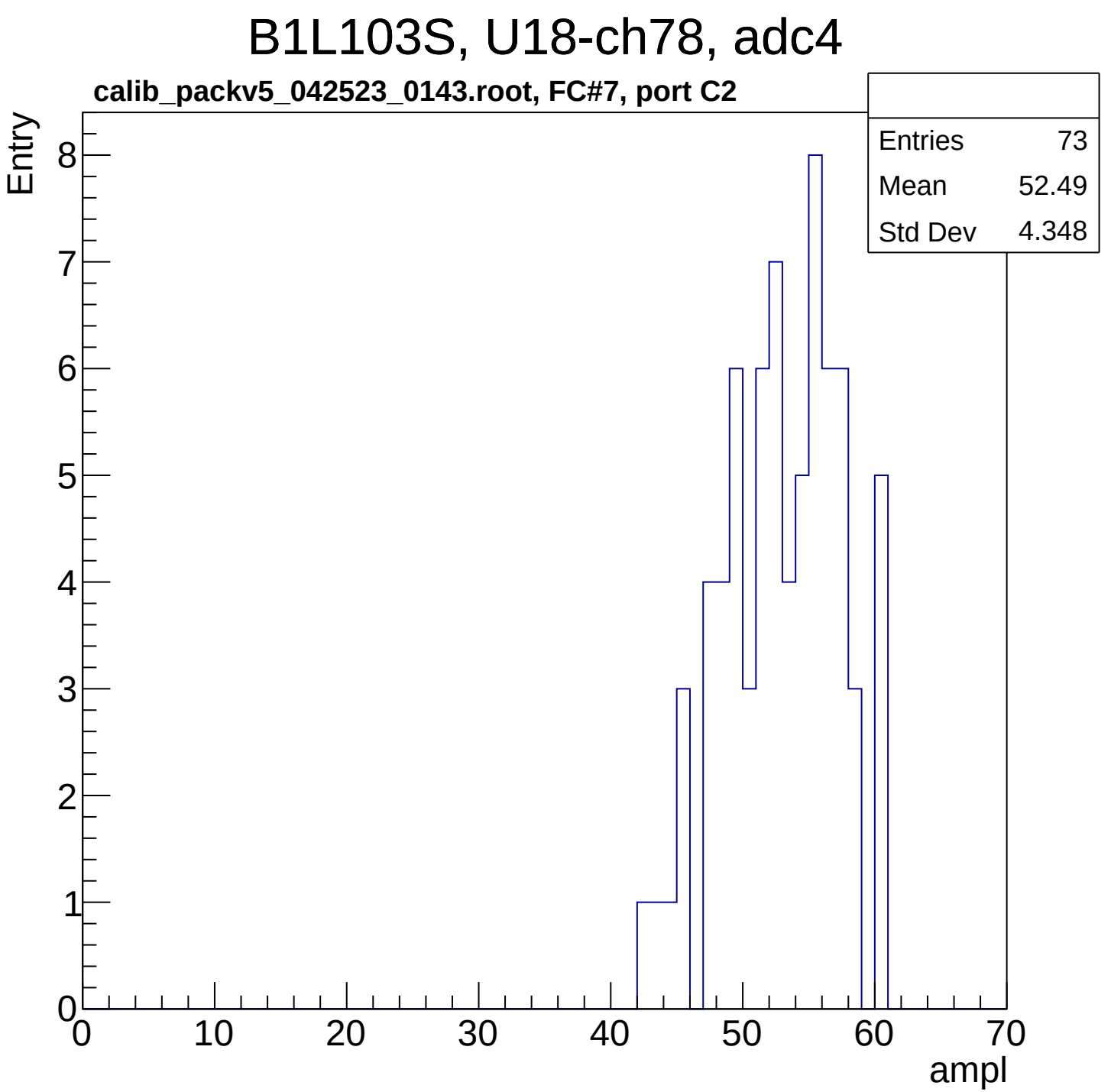

B1L103S, U18-ch77, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

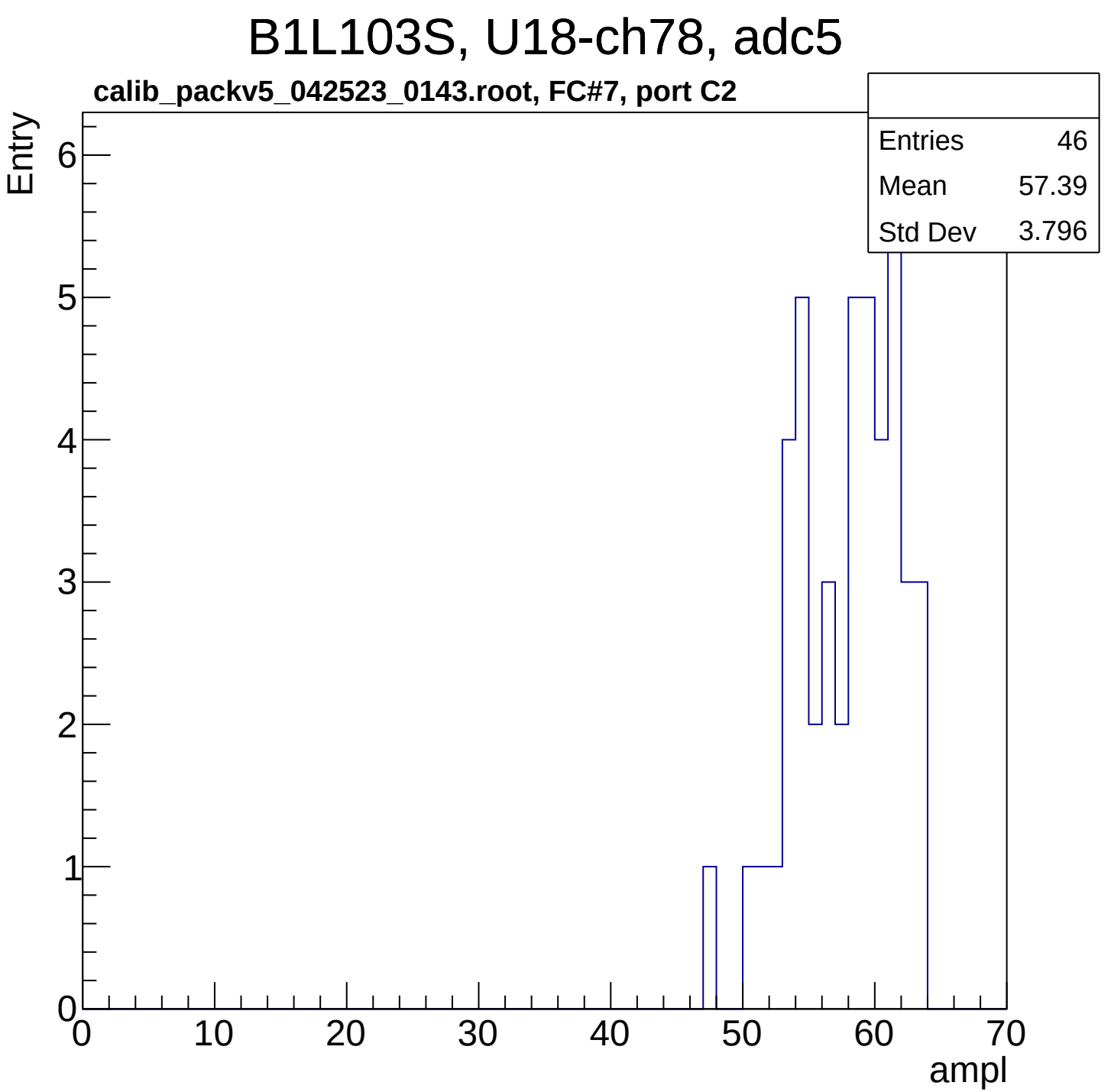

B1L103S, U18-ch78, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 83
Mean 27.14
Std Dev 4.266
Gaus mean : 27.9203
Gaus Width: 3.8912
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

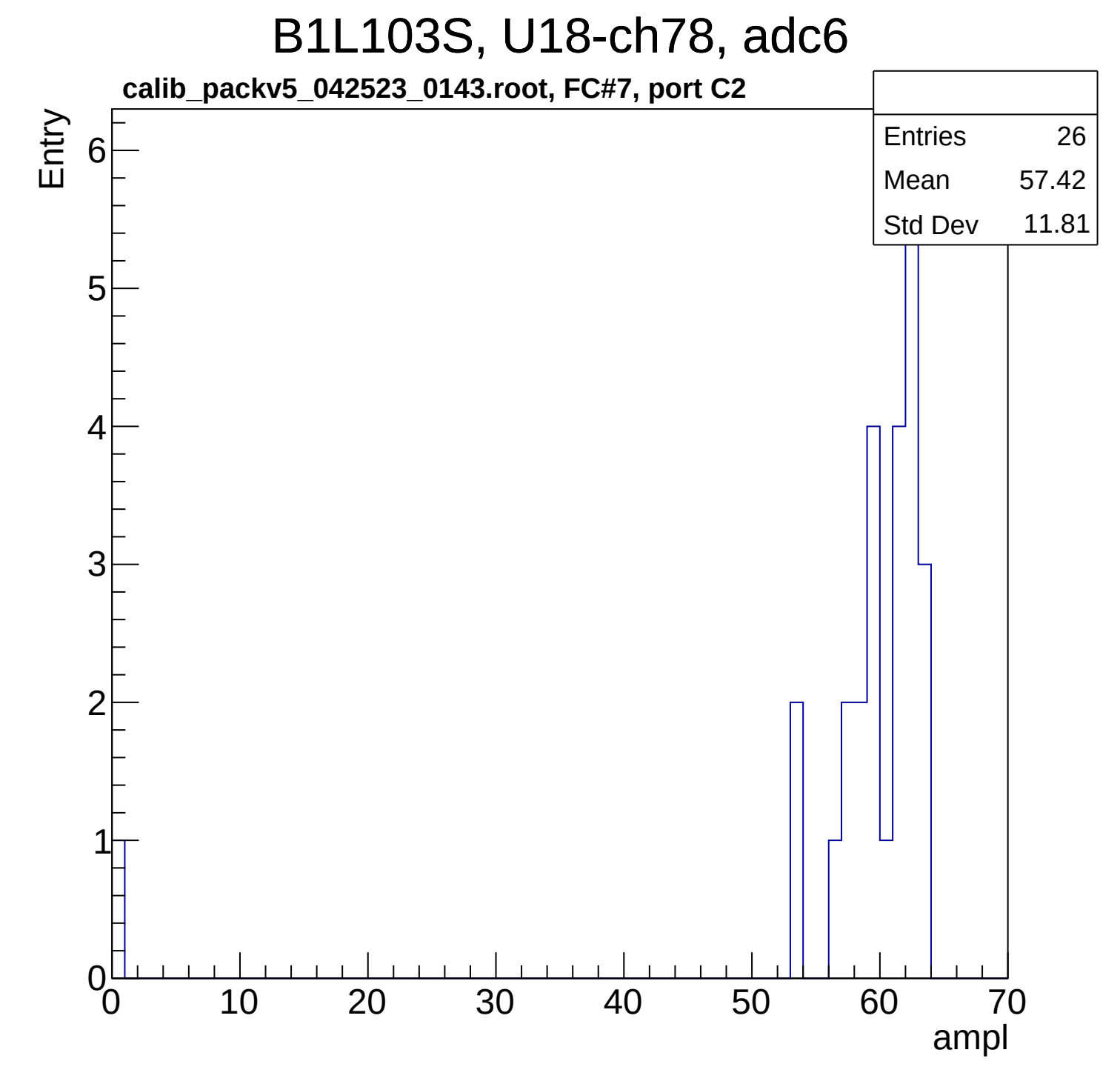

B1L103S, U18-ch78, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 33.96
Std Dev 3.924
Gaus mean : 33.9557
Gaus Width: 5.1442
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

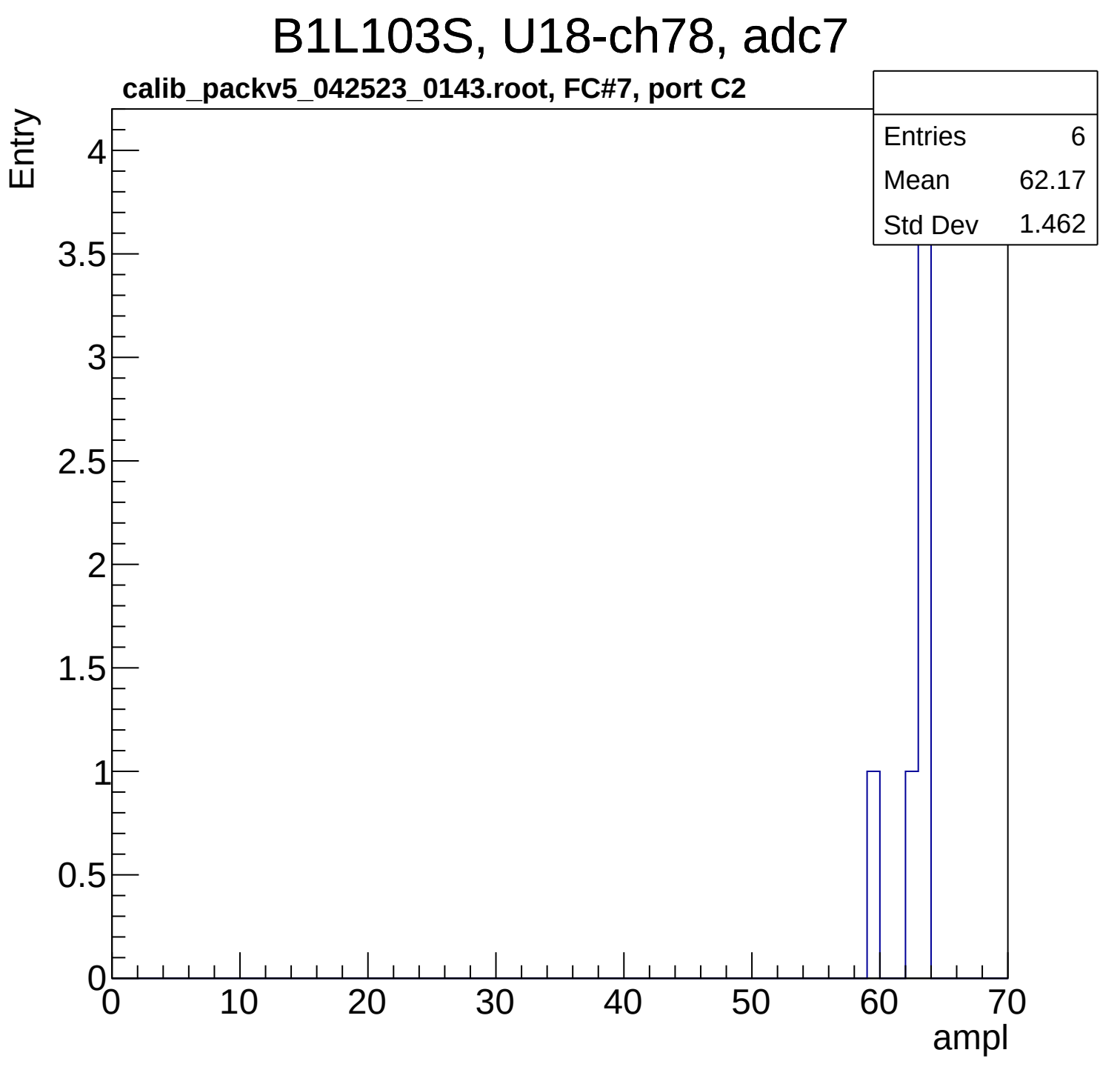

B1L103S, U18-ch78, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 39.74
Std Dev 3.6
Gaus mean : 40.4966
Gaus Width: 4.3957
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch78, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 46.25
Std Dev 3.25
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch78, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 73
Mean 52.49
Std Dev 4.348
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch78, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 46
Mean 57.39
Std Dev 3.796
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch78, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 26
Mean 57.42
Std Dev 11.81
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch78, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 6
Mean 62.17
Std Dev 1.462
Entry
ampl
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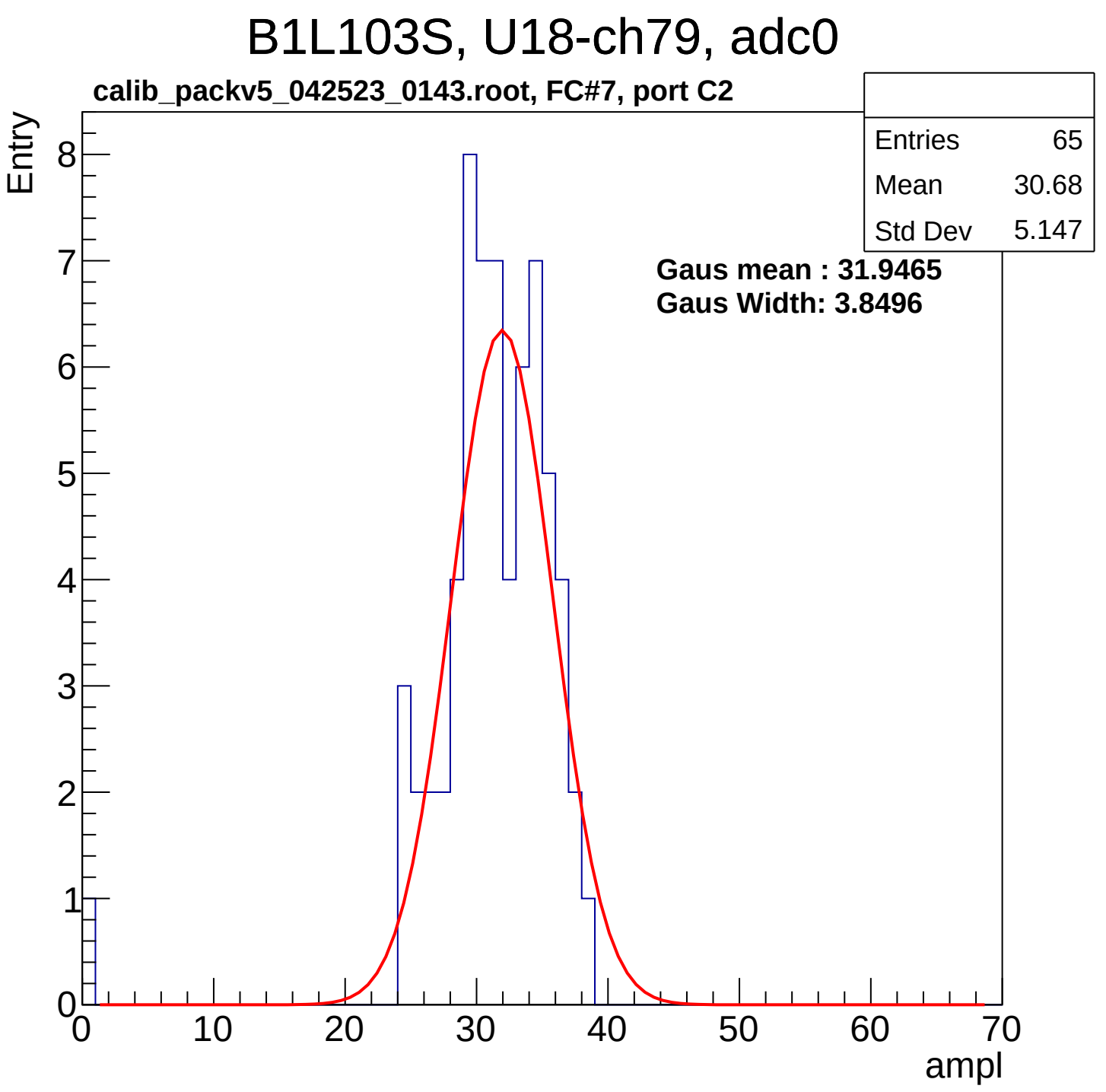
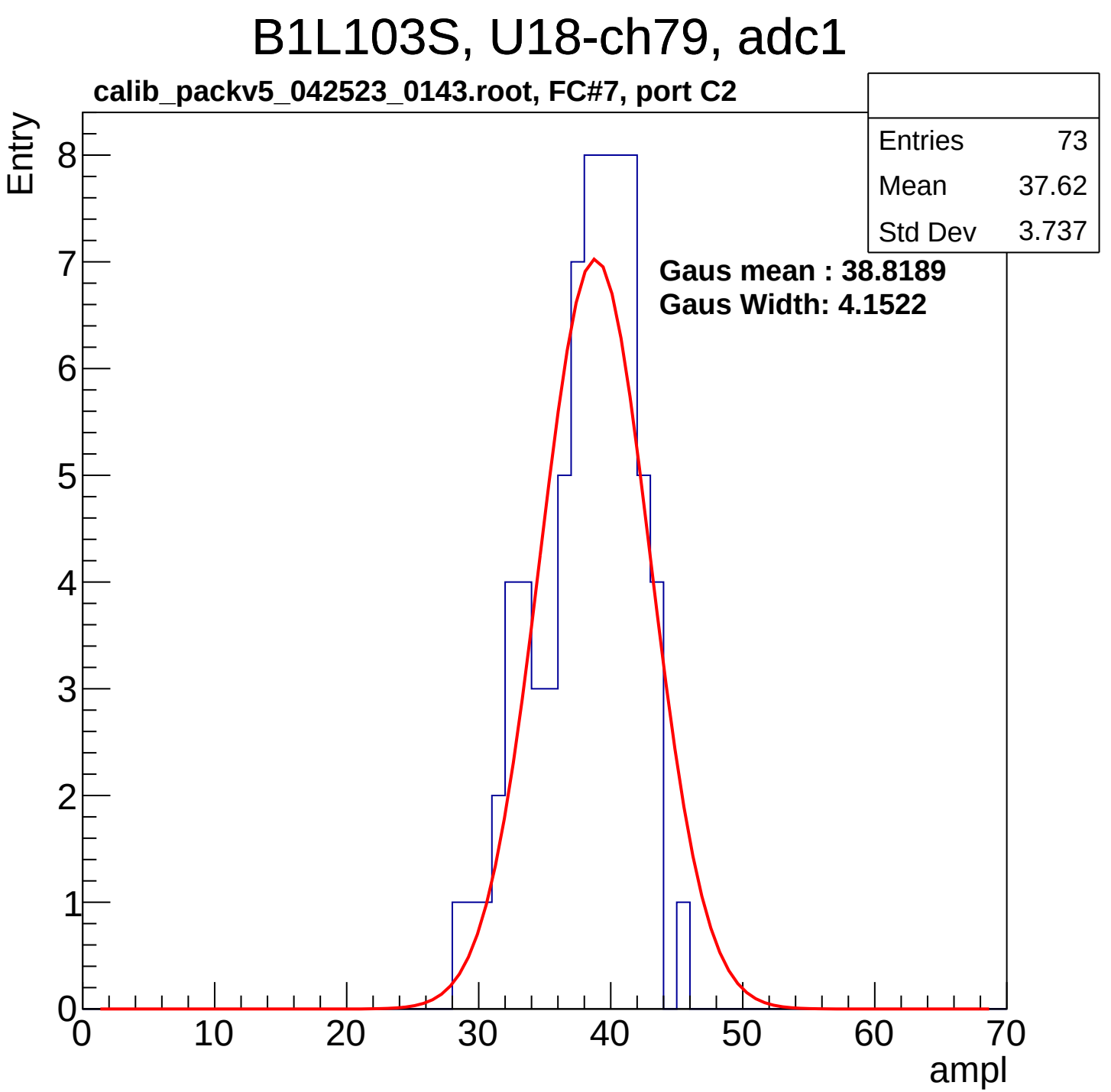
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U18-ch79, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 30.68
Std Dev 5.147
Gaus mean : 31.9465
Gaus Width: 3.8496
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch79, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 73
Mean 37.62
Std Dev 3.737
Gaus mean : 38.8189
Gaus Width: 4.1522
Entry
ampl
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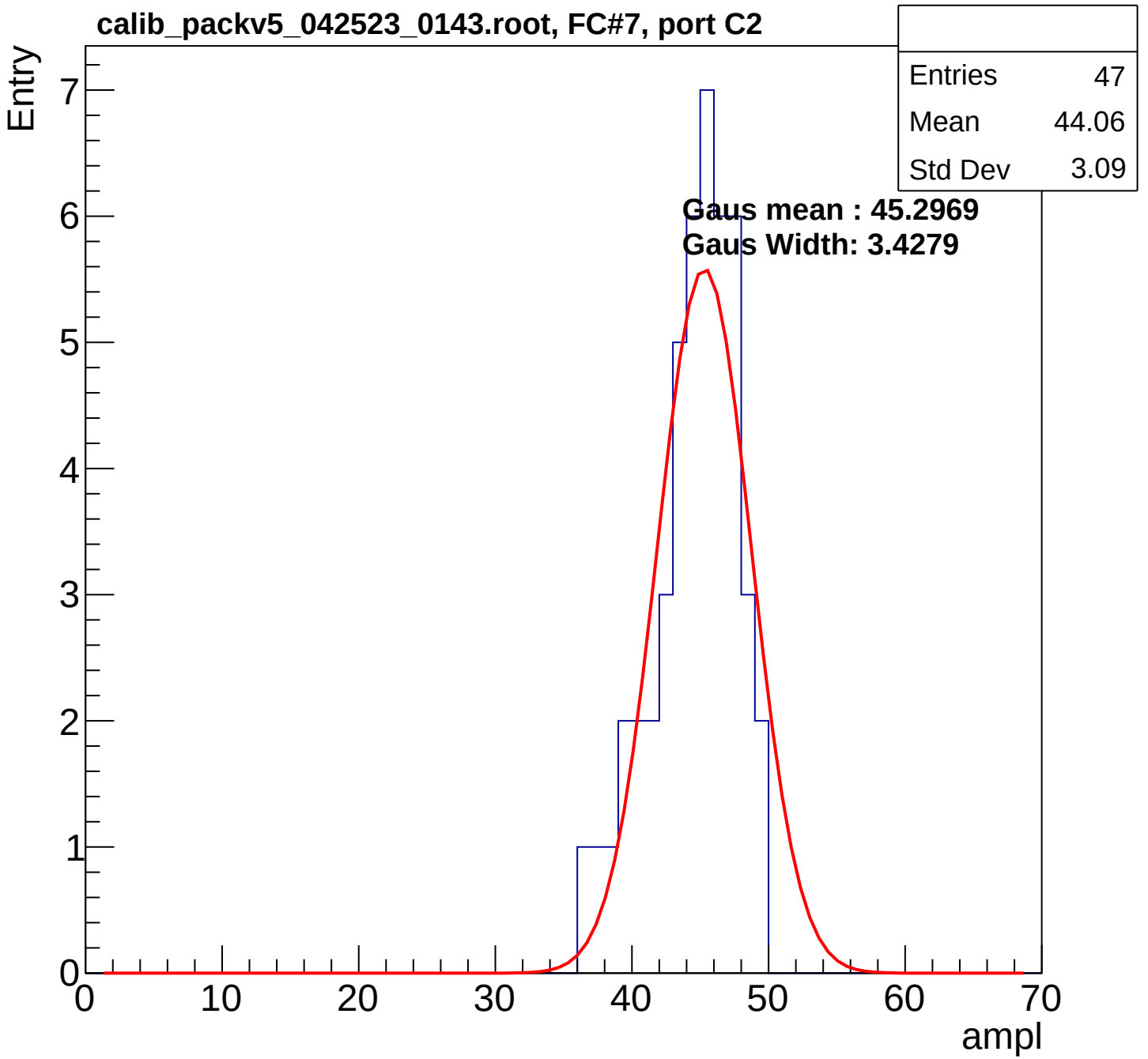
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch79, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 47
Mean 44.06
Std Dev 3.09
Gaus mean : 45.2969
Gaus Width: 3.4279
Entry
ampl
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1
2
3
4
5
6
7
0
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20
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40
50
60
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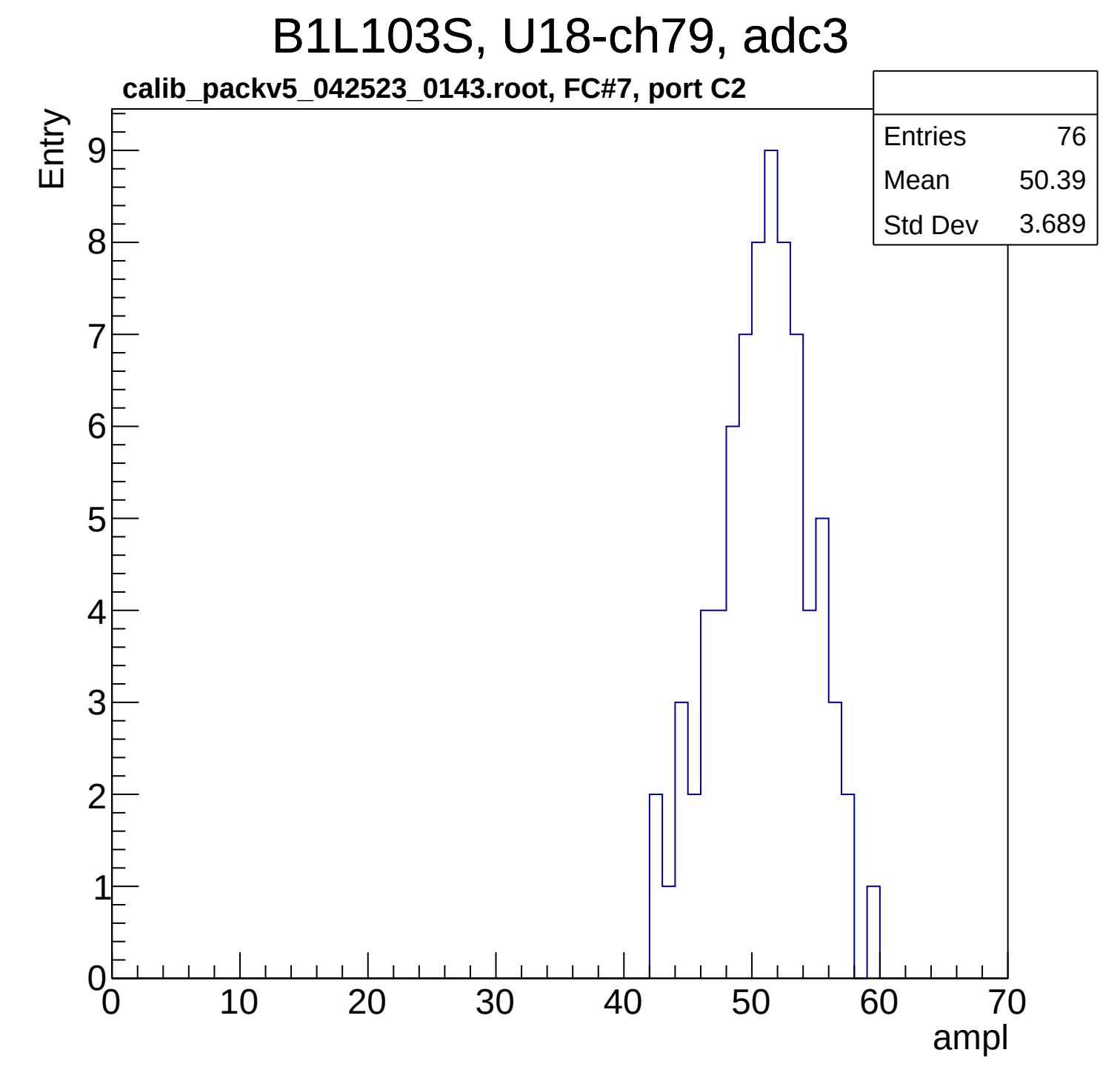
B1L103S, U18-ch79, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 76
Mean 50.39
Std Dev 3.689
Entry
ampl
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3
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5
6
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0
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20
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60
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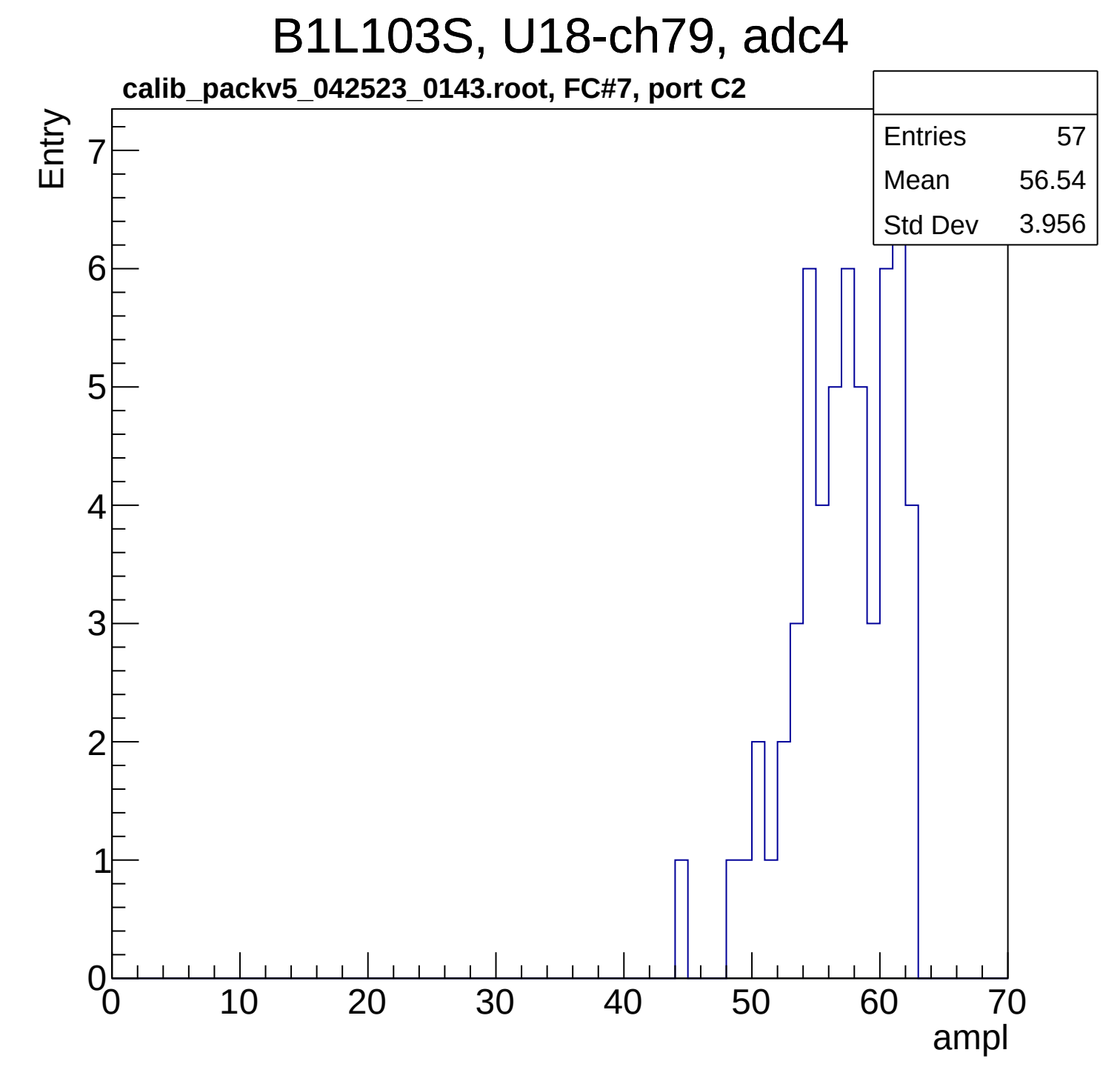
B1L103S, U18-ch79, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 56.54
Std Dev 3.956
Entry
ampl
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0
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60
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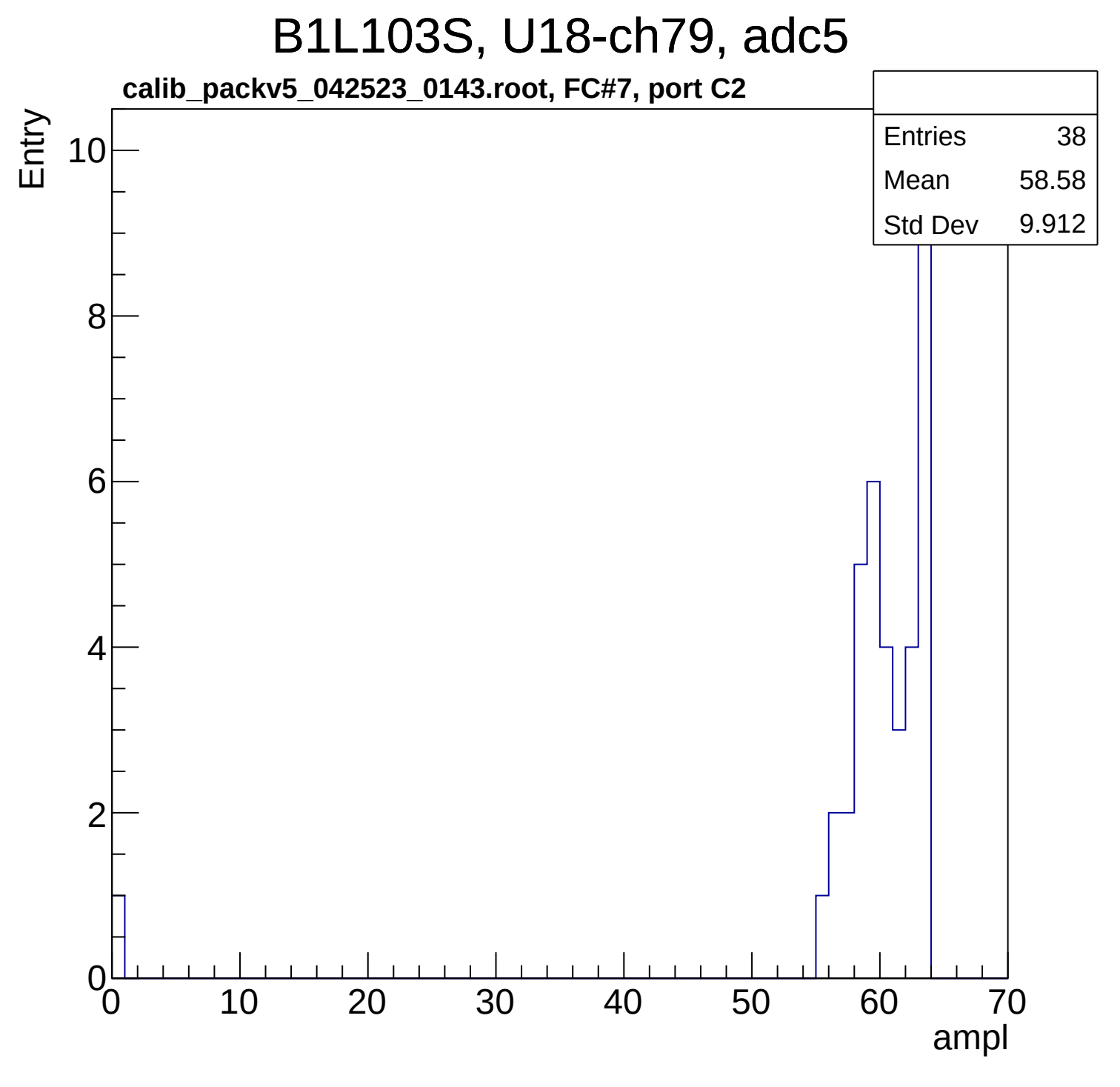
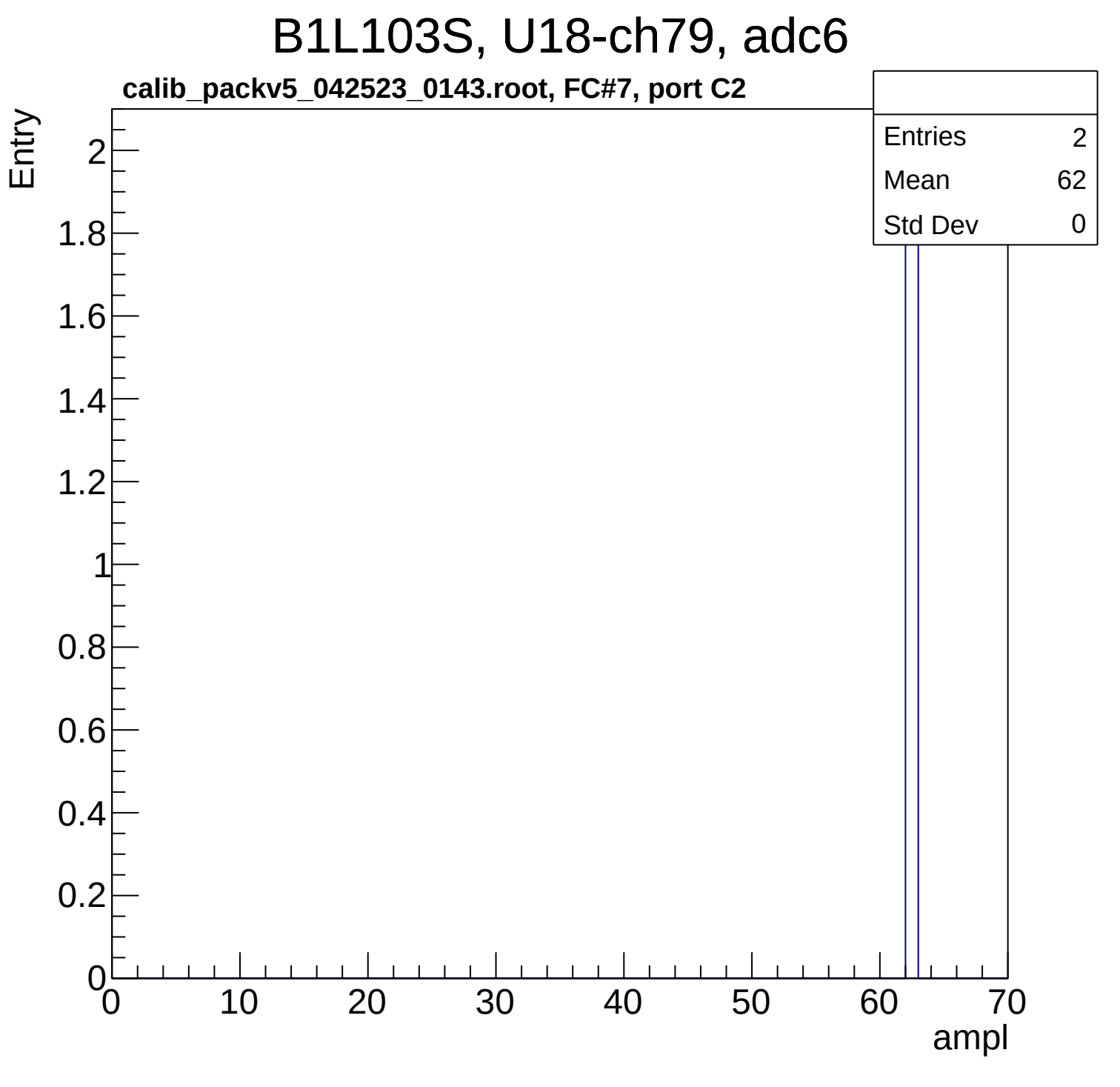

B1L103S, U18-ch79, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 38
Mean 58.58
Std Dev 9.912
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch79, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 62
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
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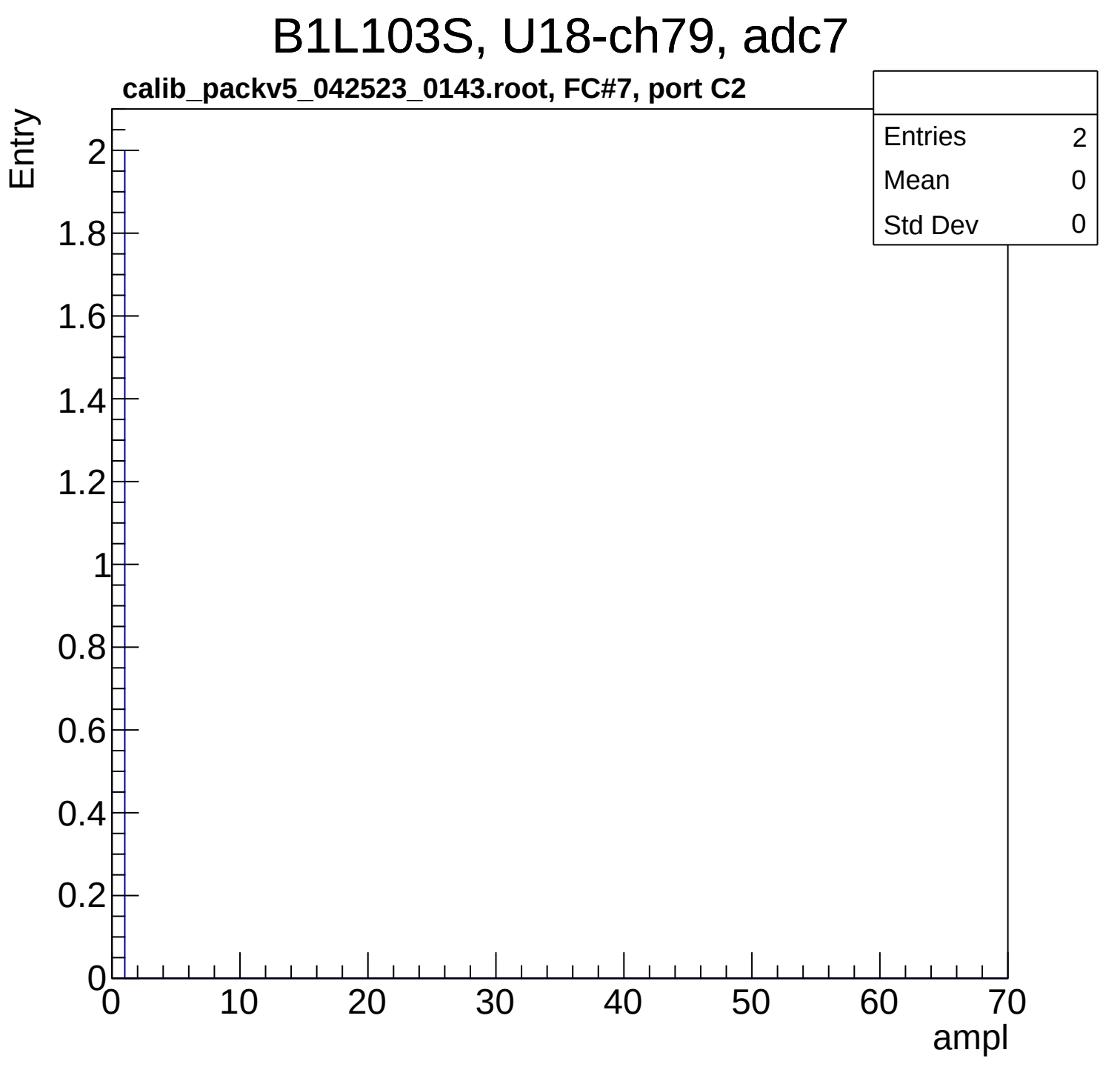
10
20
30
40
50
60
70


B1L103S, U18-ch79, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
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0.6
0.4
0.2
0
0
10
20
30
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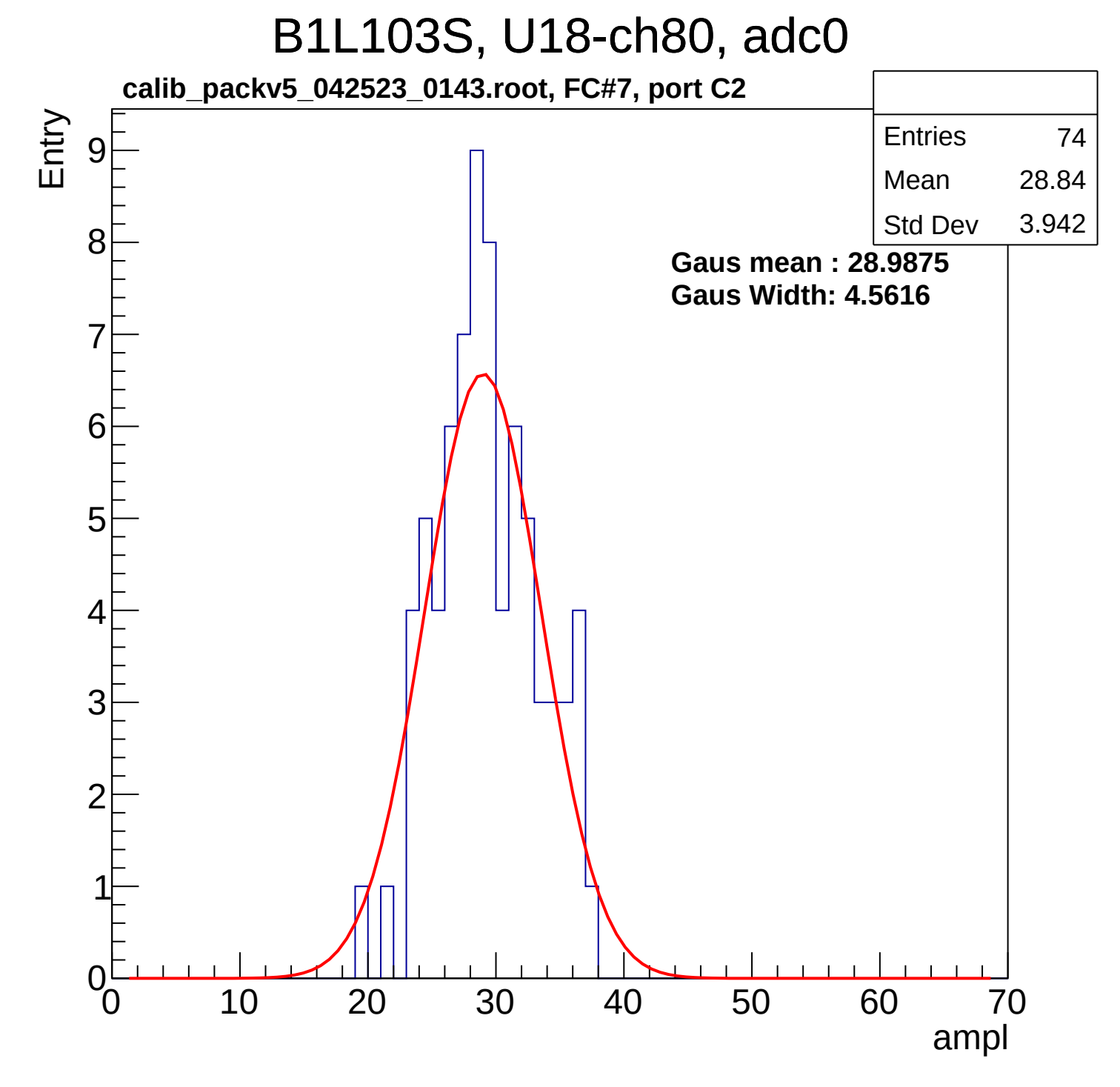
50
60
70
ampl


B1L103S, U18-ch80, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 74
Mean 28.84
Std Dev 3.942
Gaus mean : 28.9875
Gaus Width: 4.5616
Entry
ampl
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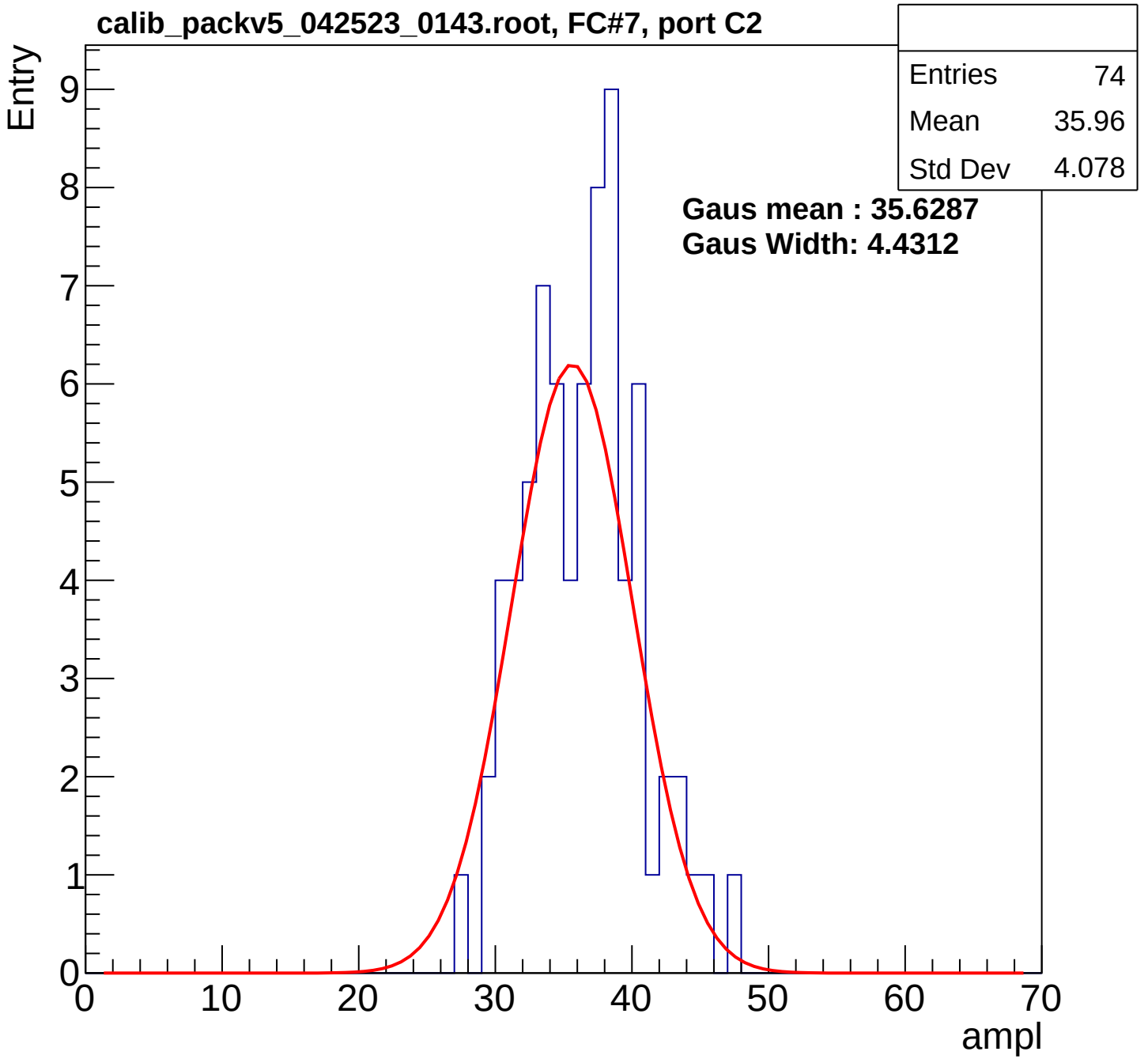
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch80, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 74
Mean 35.96
Std Dev 4.078
Gaus mean : 35.6287
Gaus Width: 4.4312
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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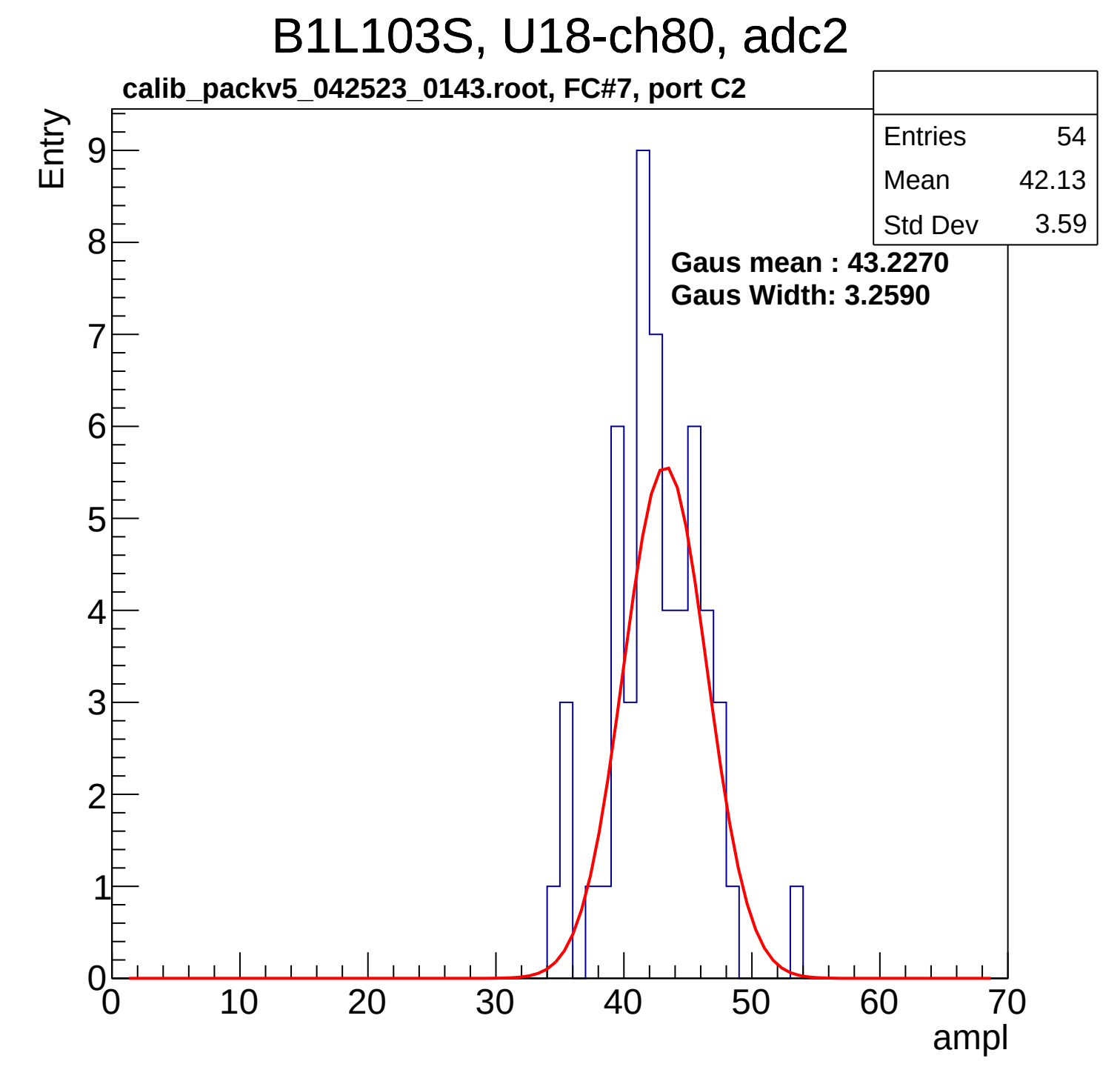
40
50
60
70


B1L103S, U18-ch80, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 54
Mean 42.13
Std Dev 3.59
Gaus mean : 43.2270
Gaus Width: 3.2590
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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40
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60
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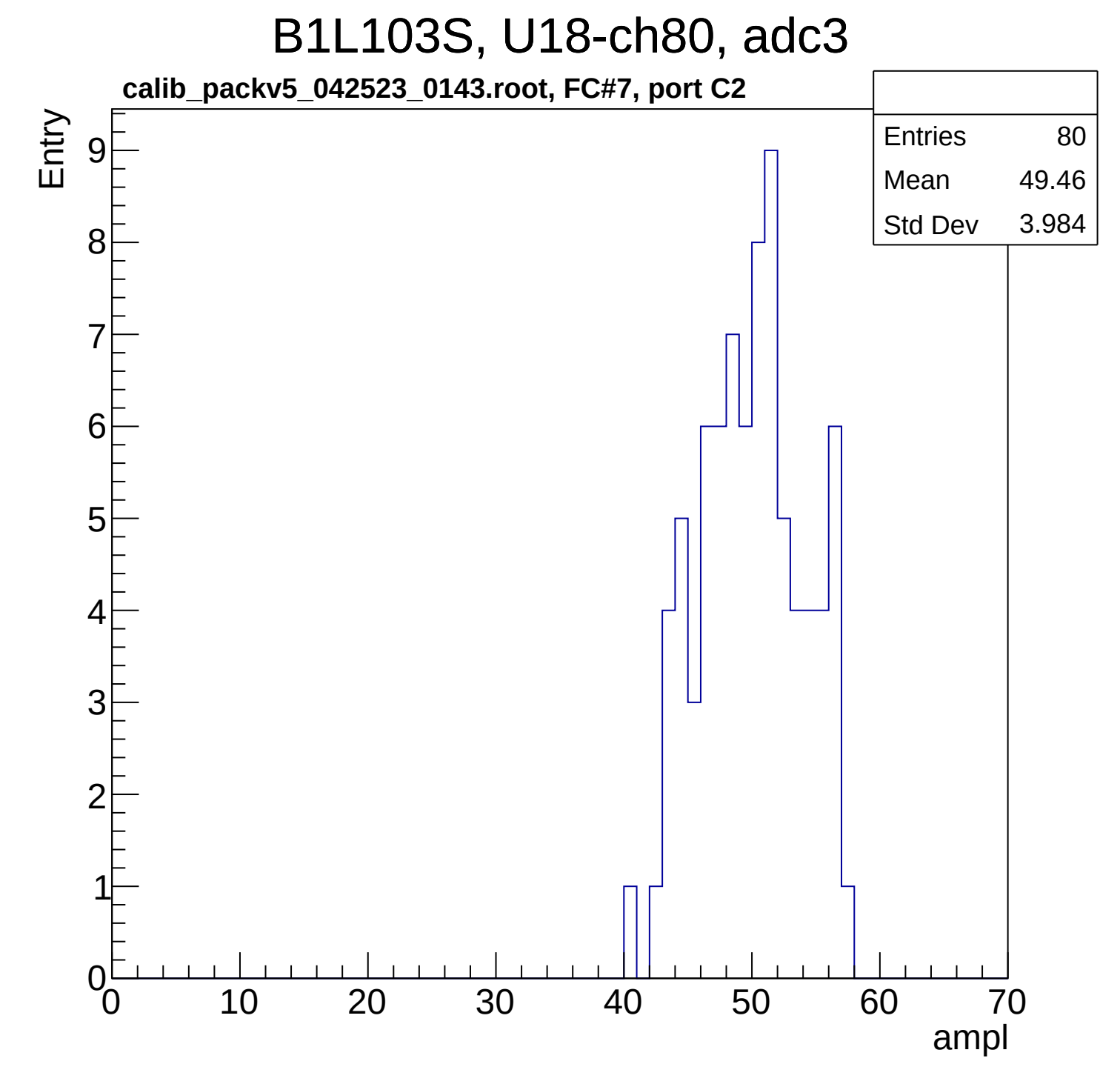
B1L103S, U18-ch80, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 80
Mean 49.46
Std Dev 3.984
Entry
ampl
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3
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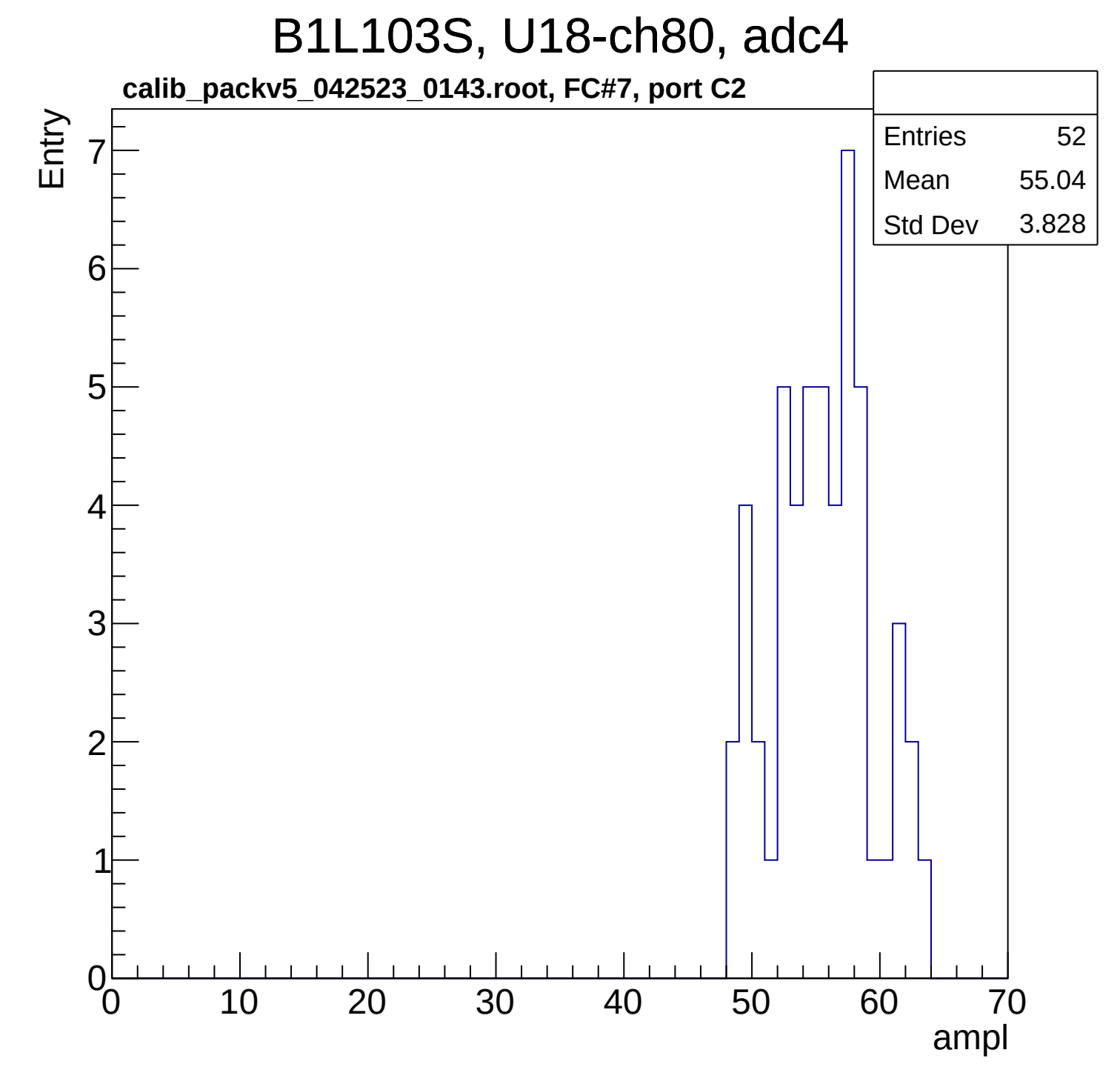
B1L103S, U18-ch80, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 52
Mean 55.04
Std Dev 3.828
Entry
ampl
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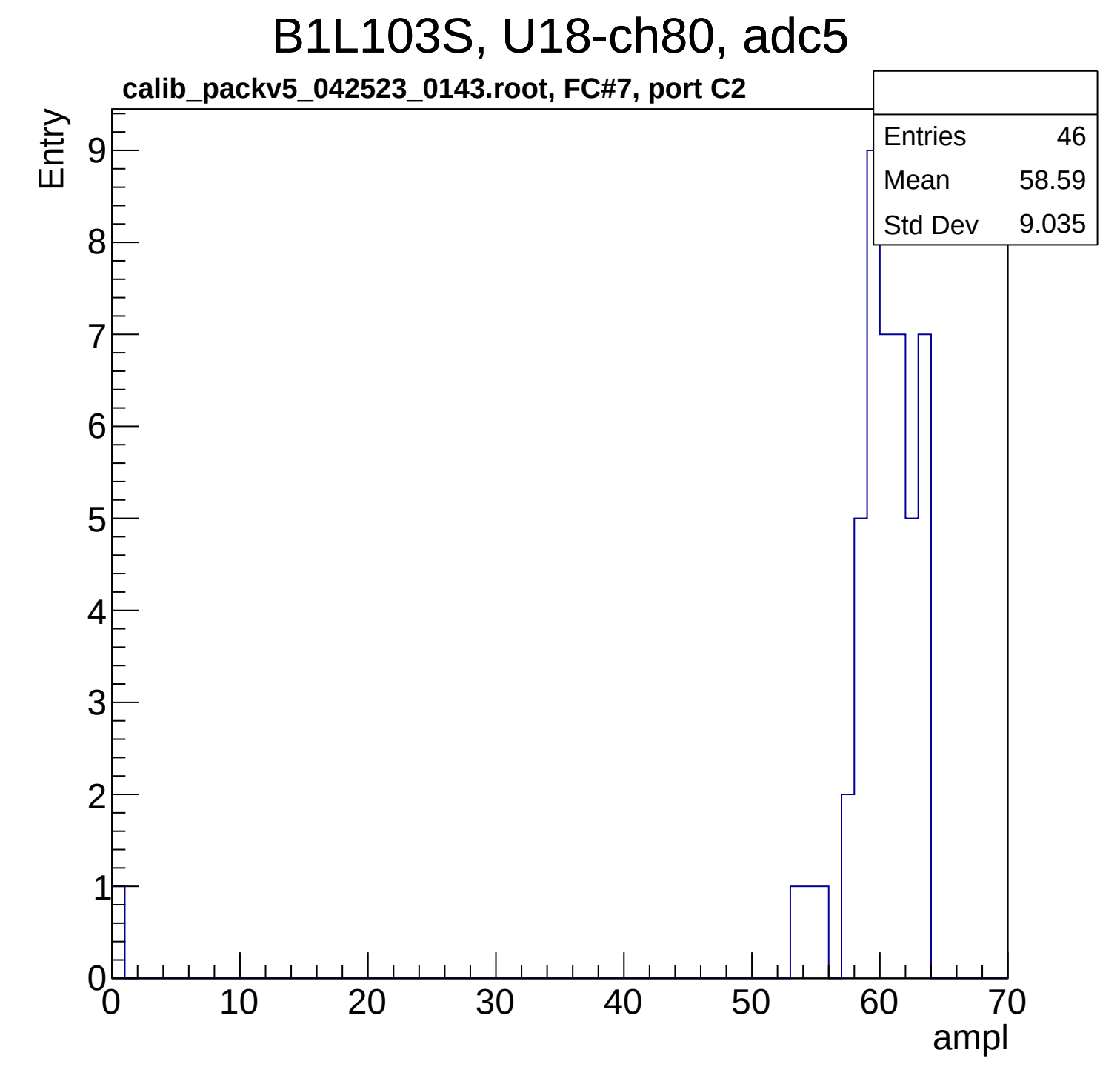
B1L103S, U18-ch80, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 46
Mean 58.59
Std Dev 9.035
Entry
ampl
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2
3
4
5
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9
0
10
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60
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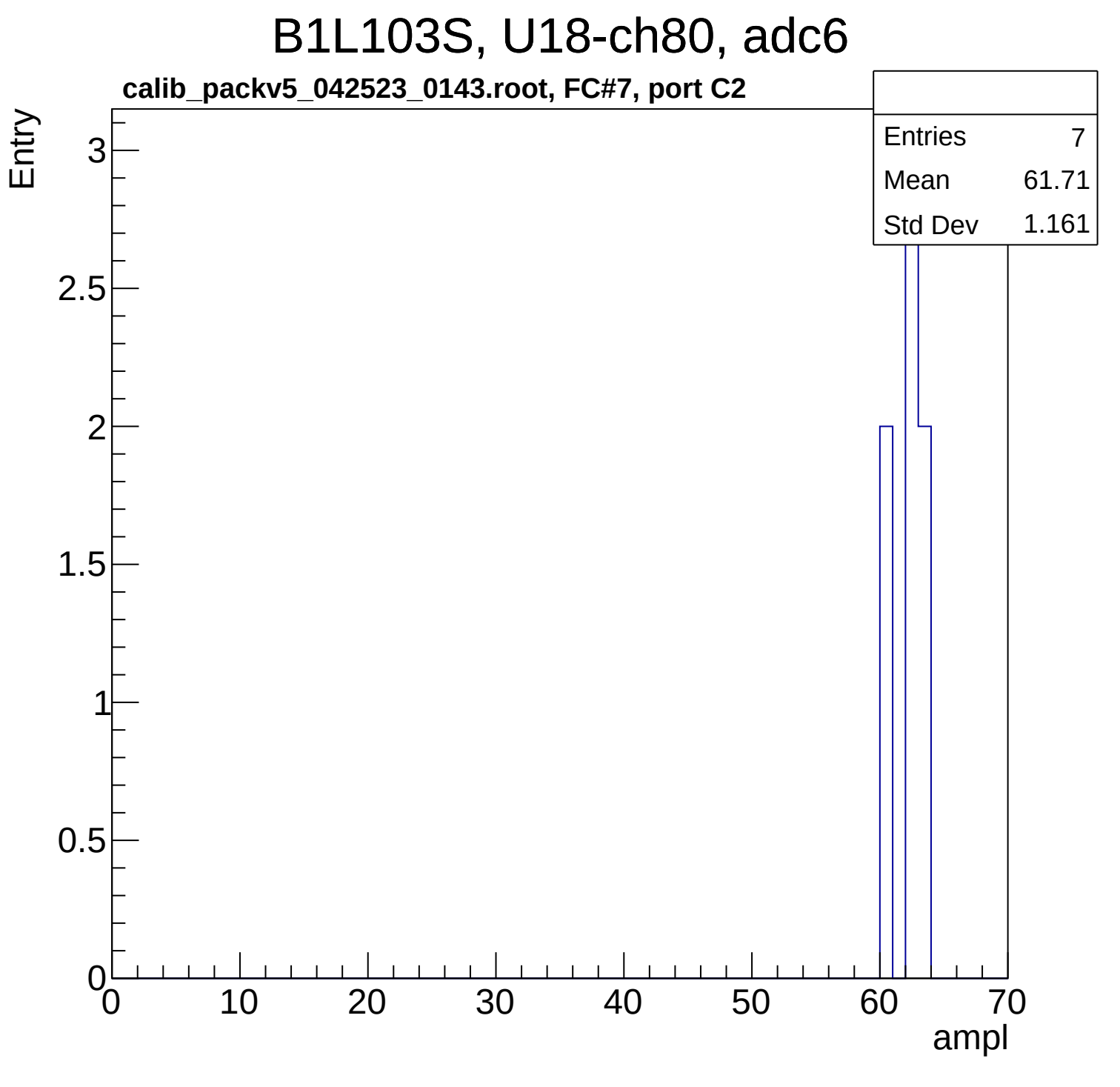
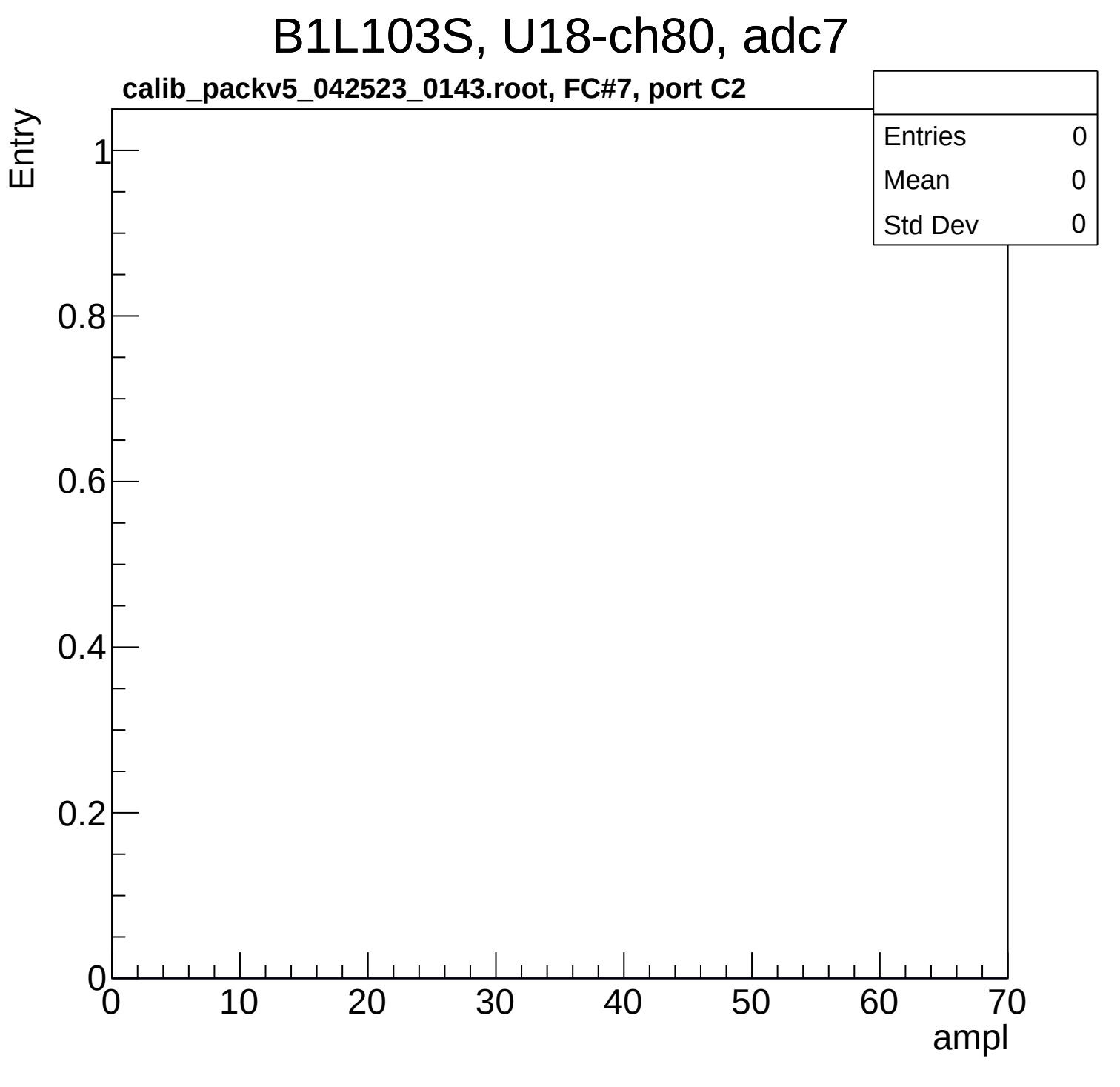
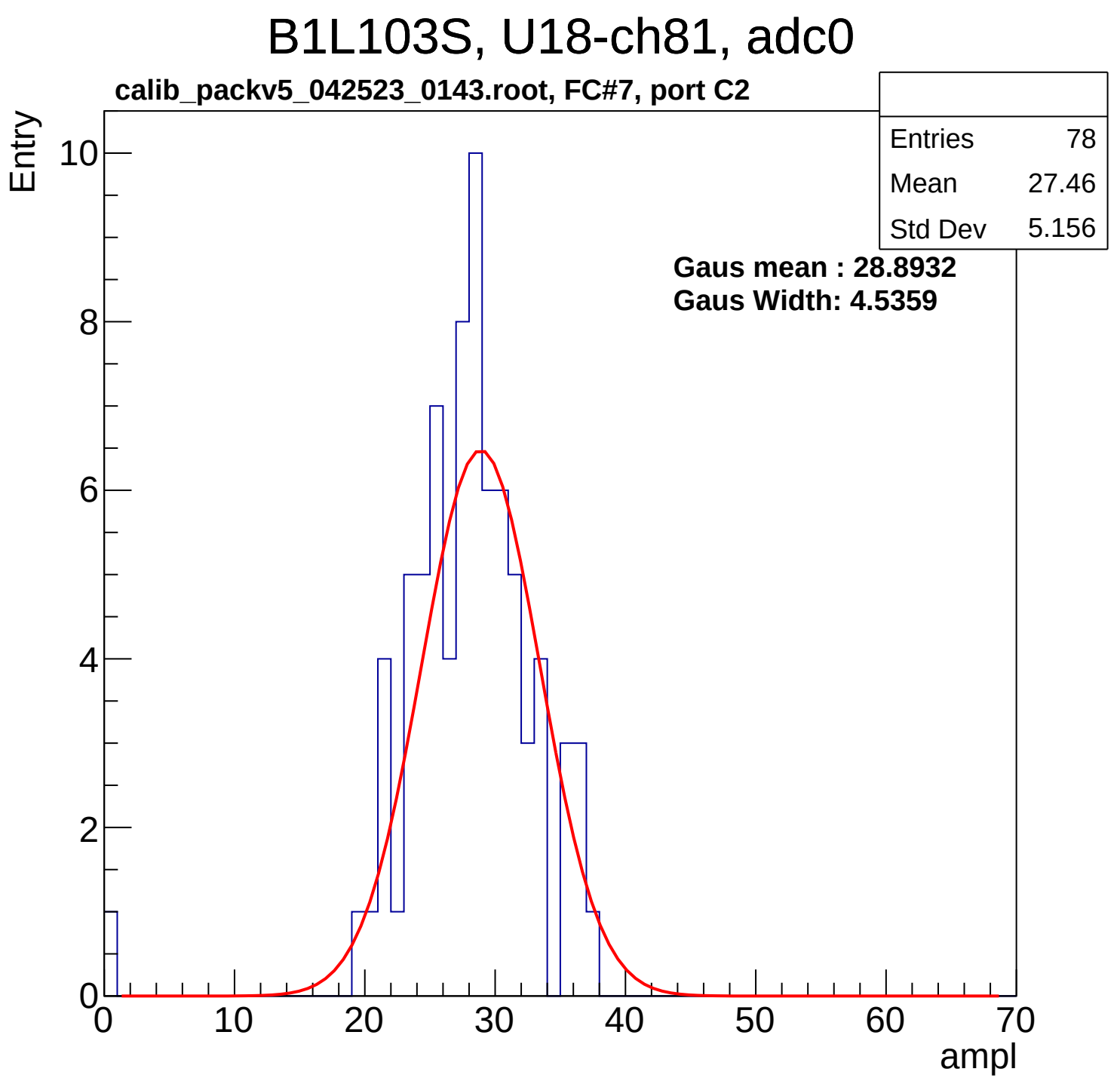
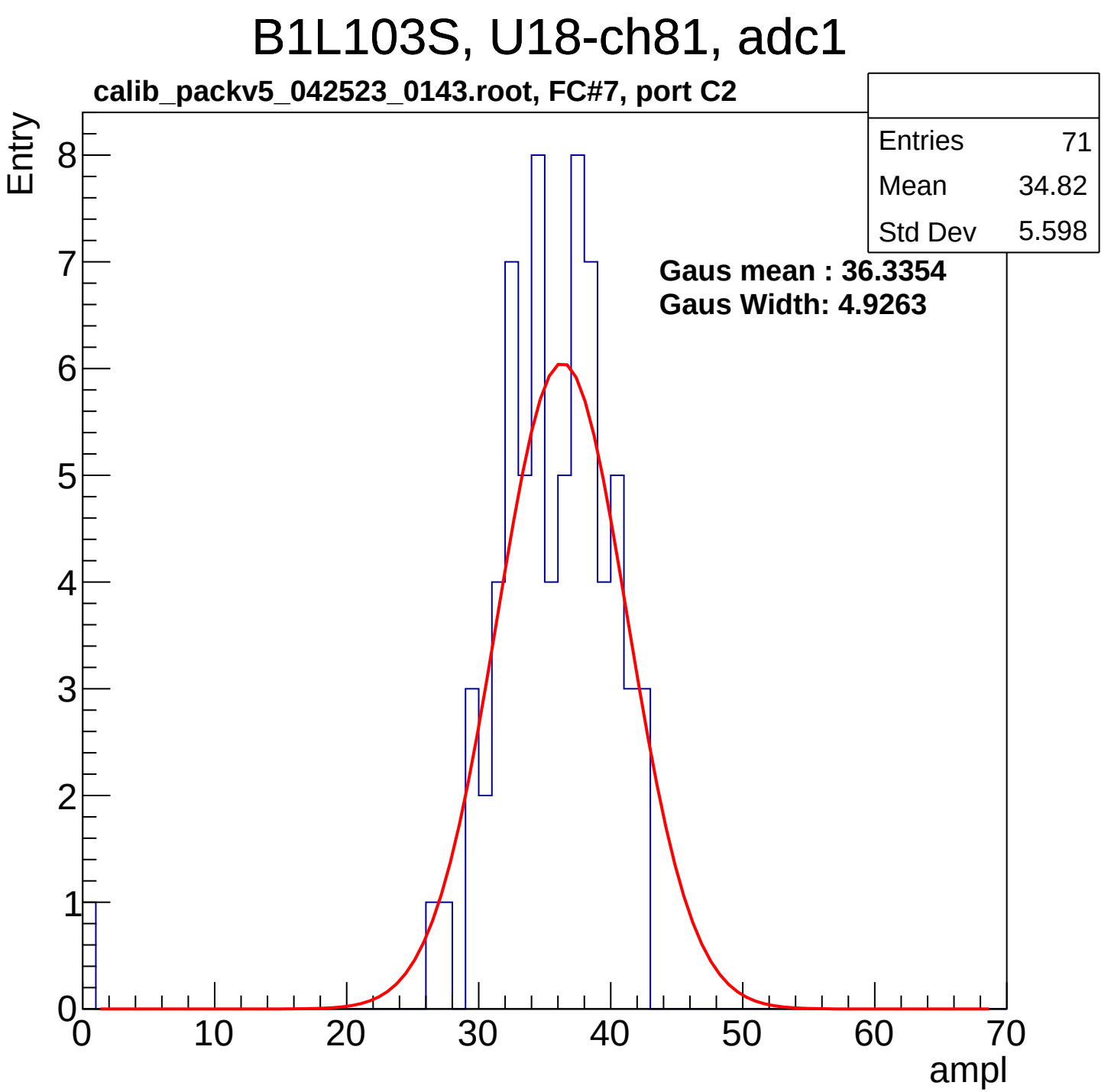

B1L103S, U18-ch80, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 7
Mean 61.71
Std Dev 1.161
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U18-ch80, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch81, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 78
Mean 27.46
Std Dev 5.156
Gaus mean : 28.8932
Gaus Width: 4.5359
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch81, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 71
Mean 34.82
Std Dev 5.598
Gaus mean : 36.3354
Gaus Width: 4.9263
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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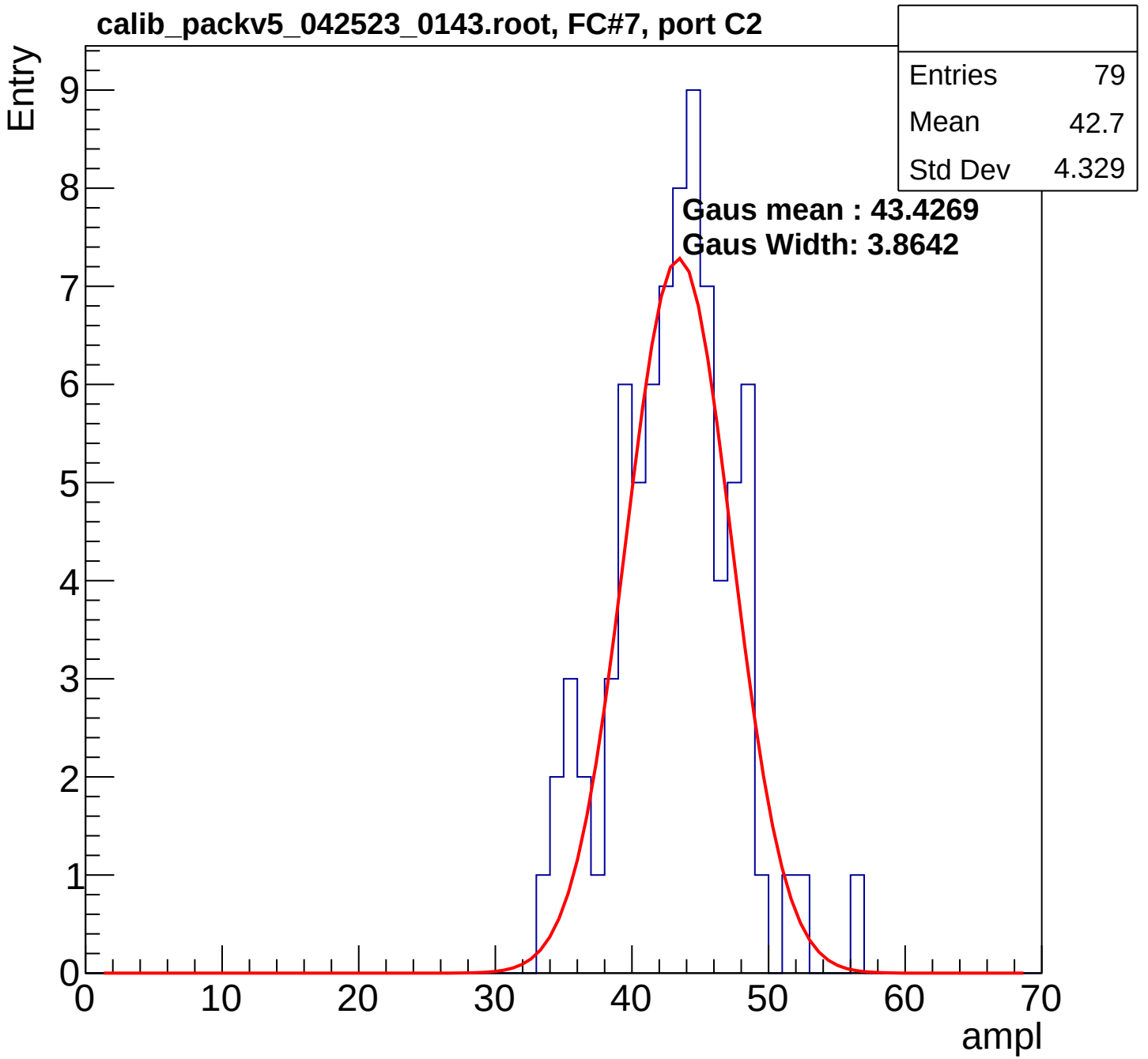
B1L103S, U18-ch81, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 79
Mean 42.7
Std Dev 4.329
Gaus mean : 43.4269
Gaus Width: 3.8642
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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60
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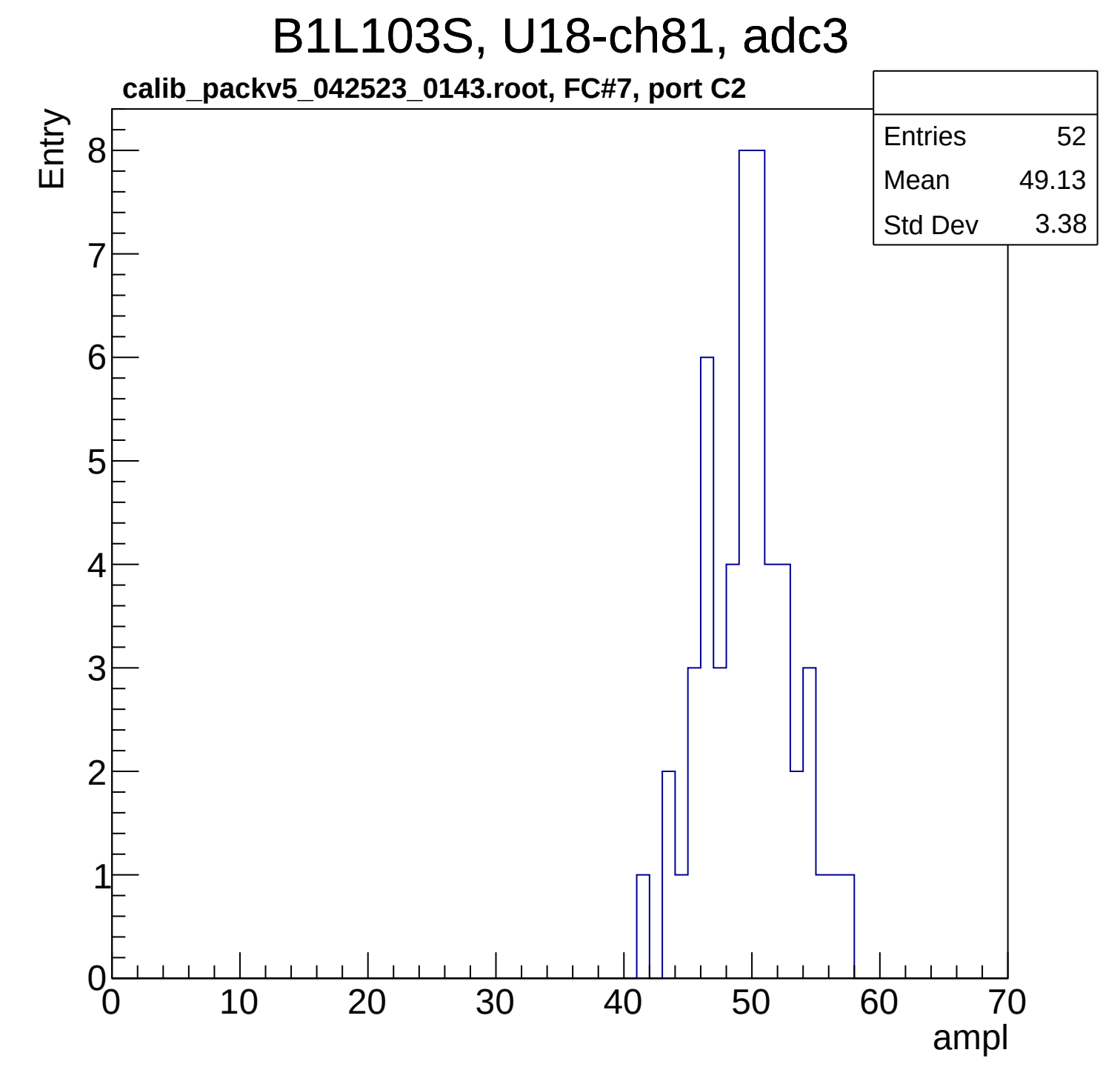
B1L103S, U18-ch81, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 52
Mean 49.13
Std Dev 3.38
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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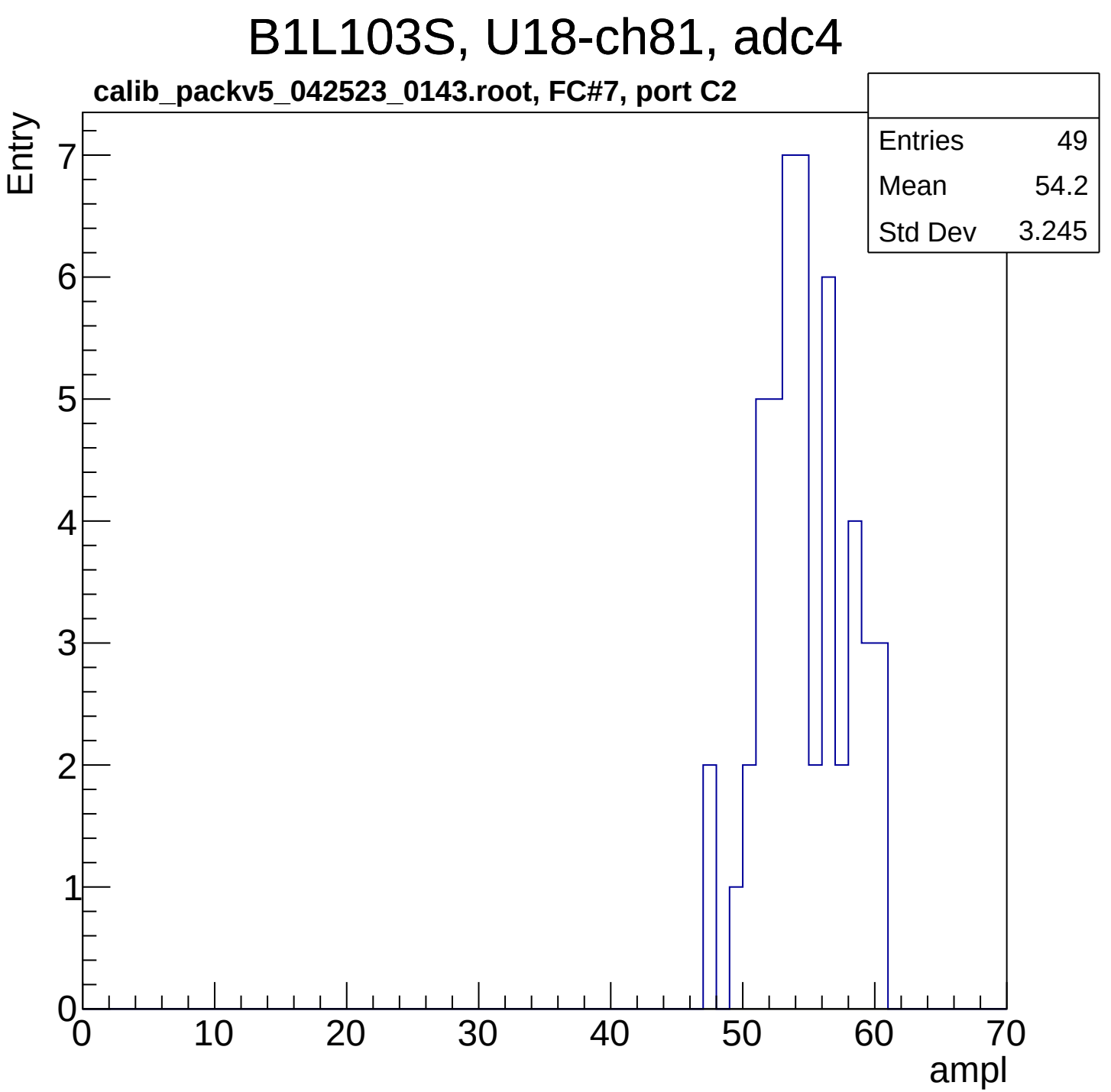
B1L103S, U18-ch81, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 49
Mean 54.2
Std Dev 3.245
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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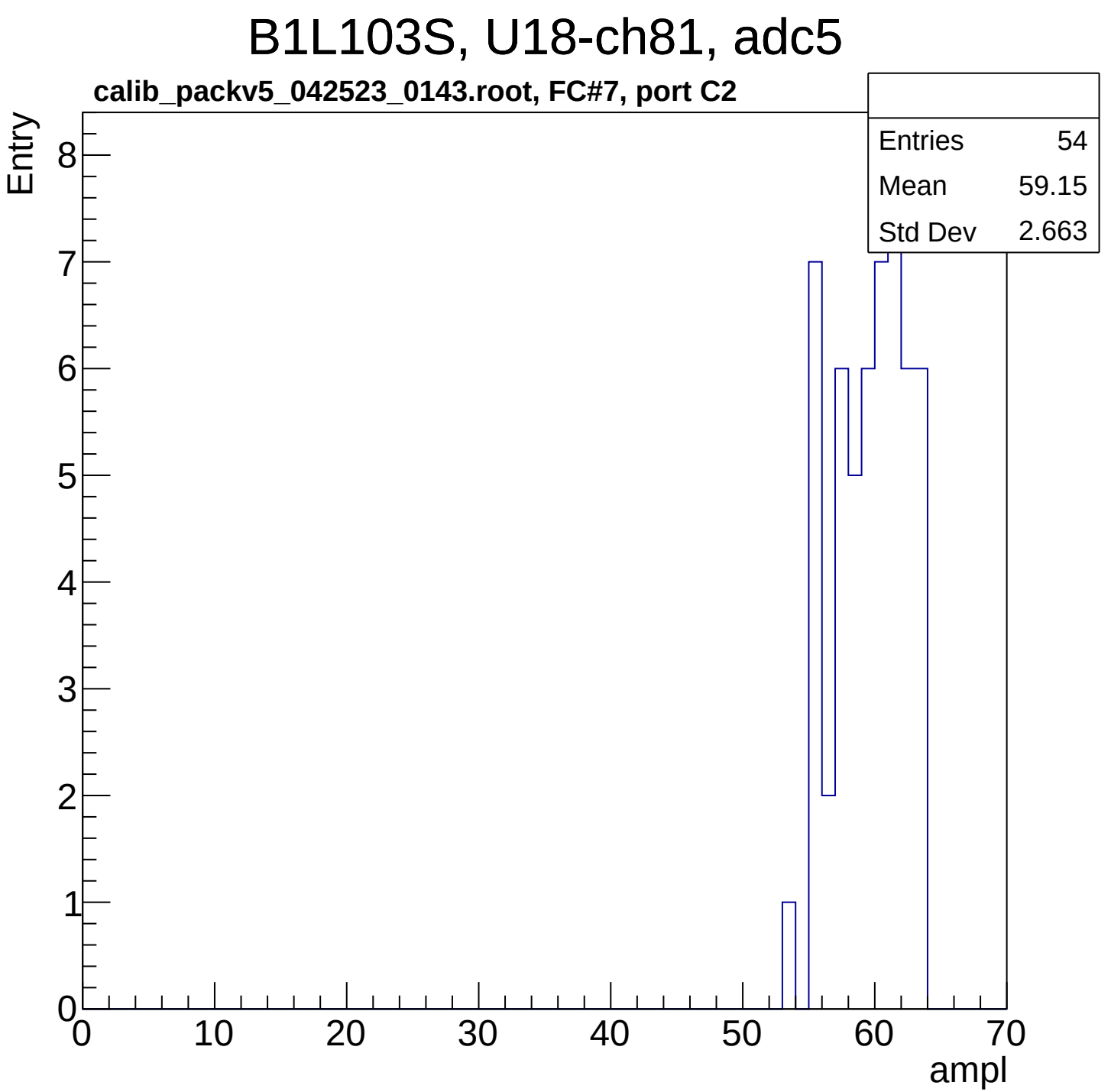
B1L103S, U18-ch81, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 54
Mean 59.15
Std Dev 2.663
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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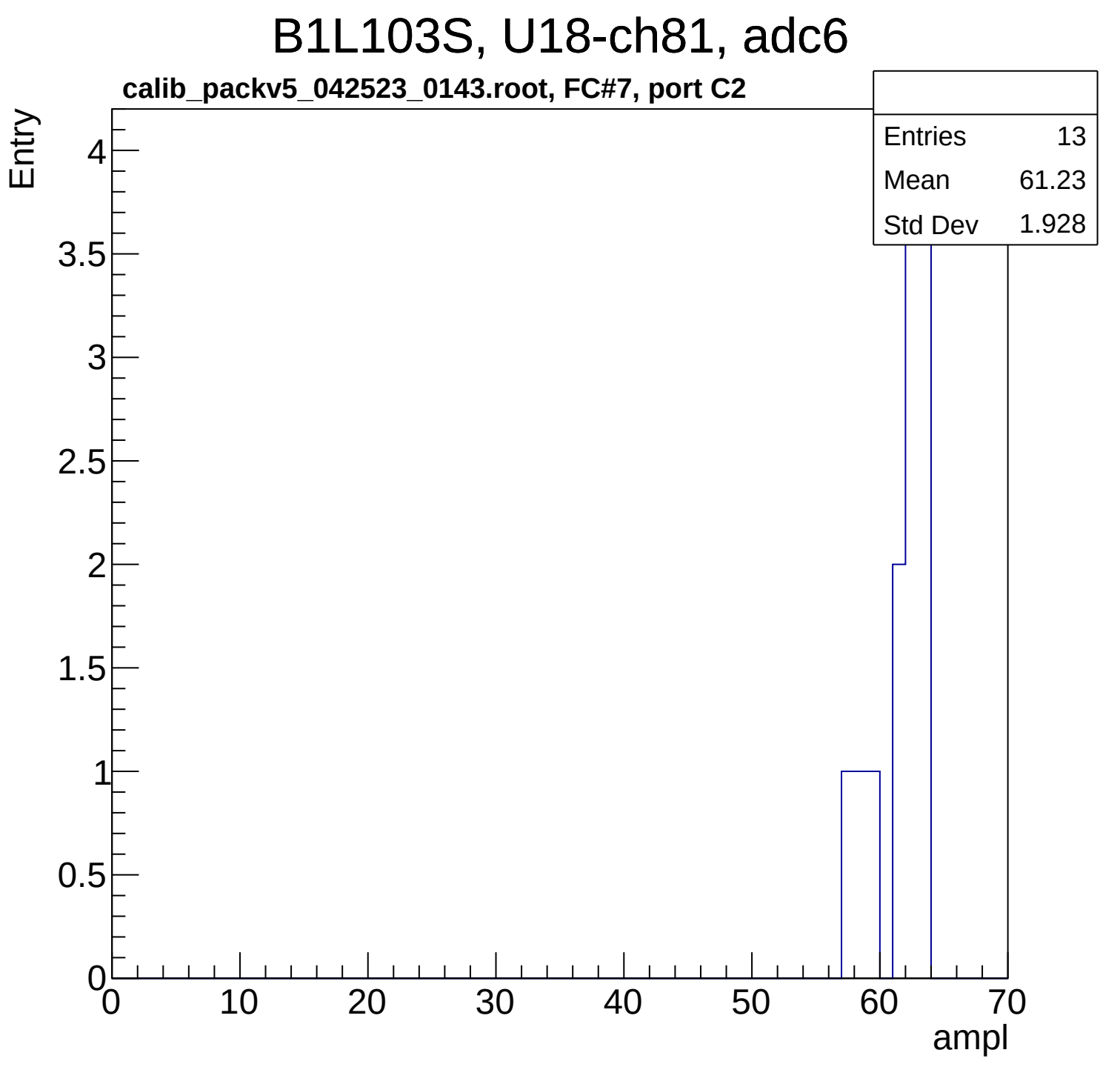
B1L103S, U18-ch81, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 13
Mean 61.23
Std Dev 1.928
Entry
ampl
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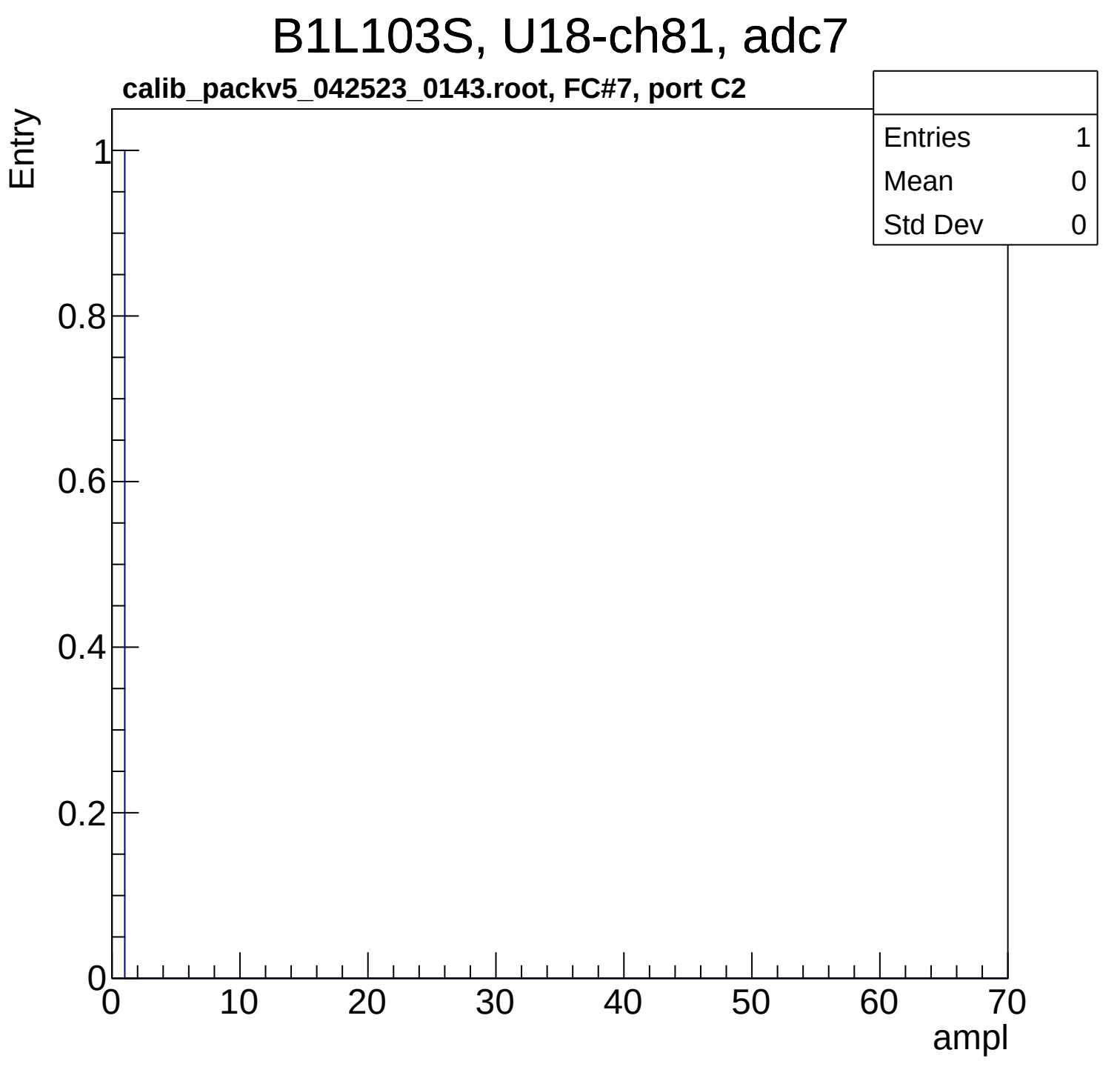
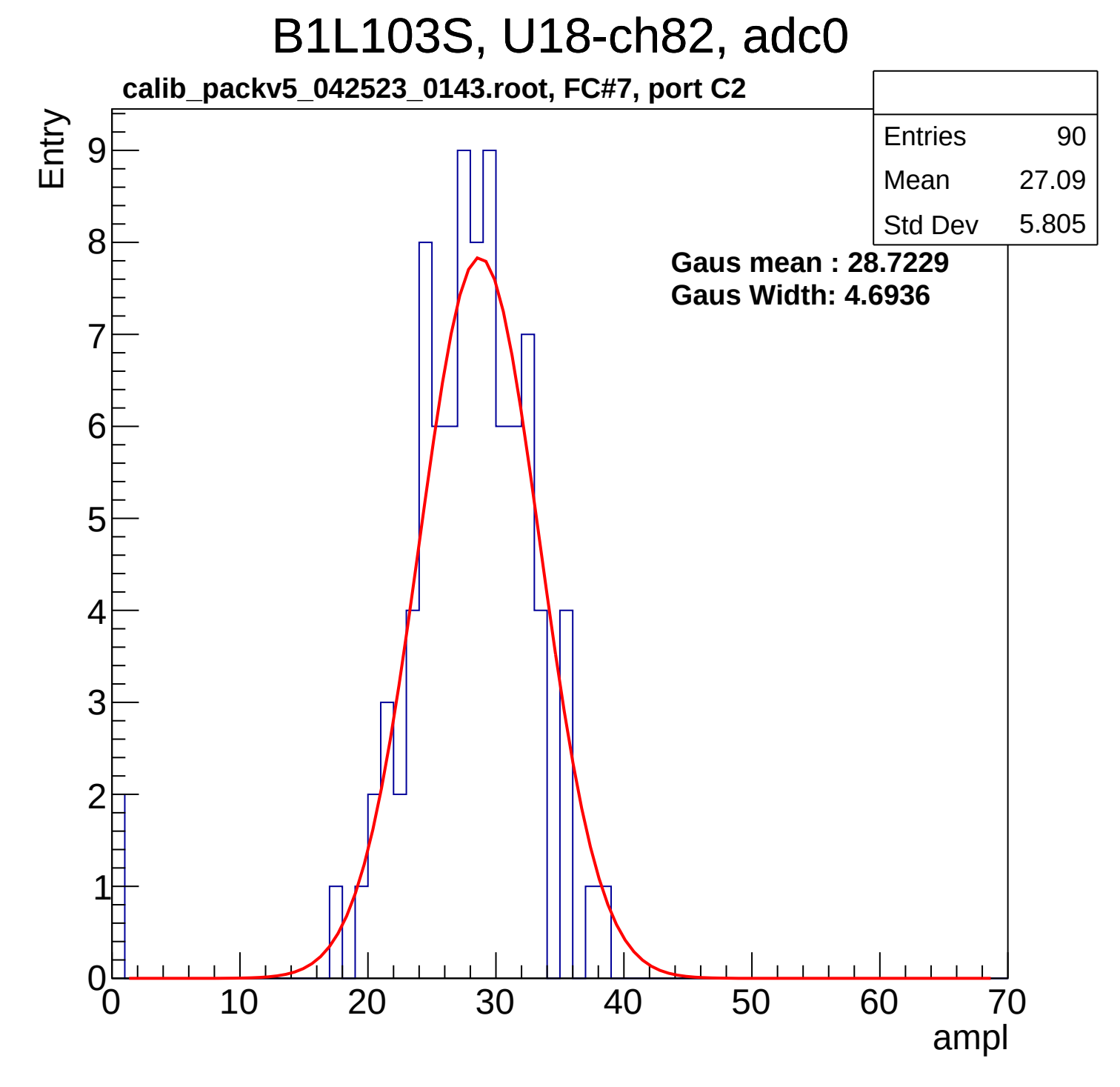
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U18-ch81, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch82, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 90
Mean 27.09
Std Dev 5.805
Gaus mean : 28.7229
Gaus Width: 4.6936
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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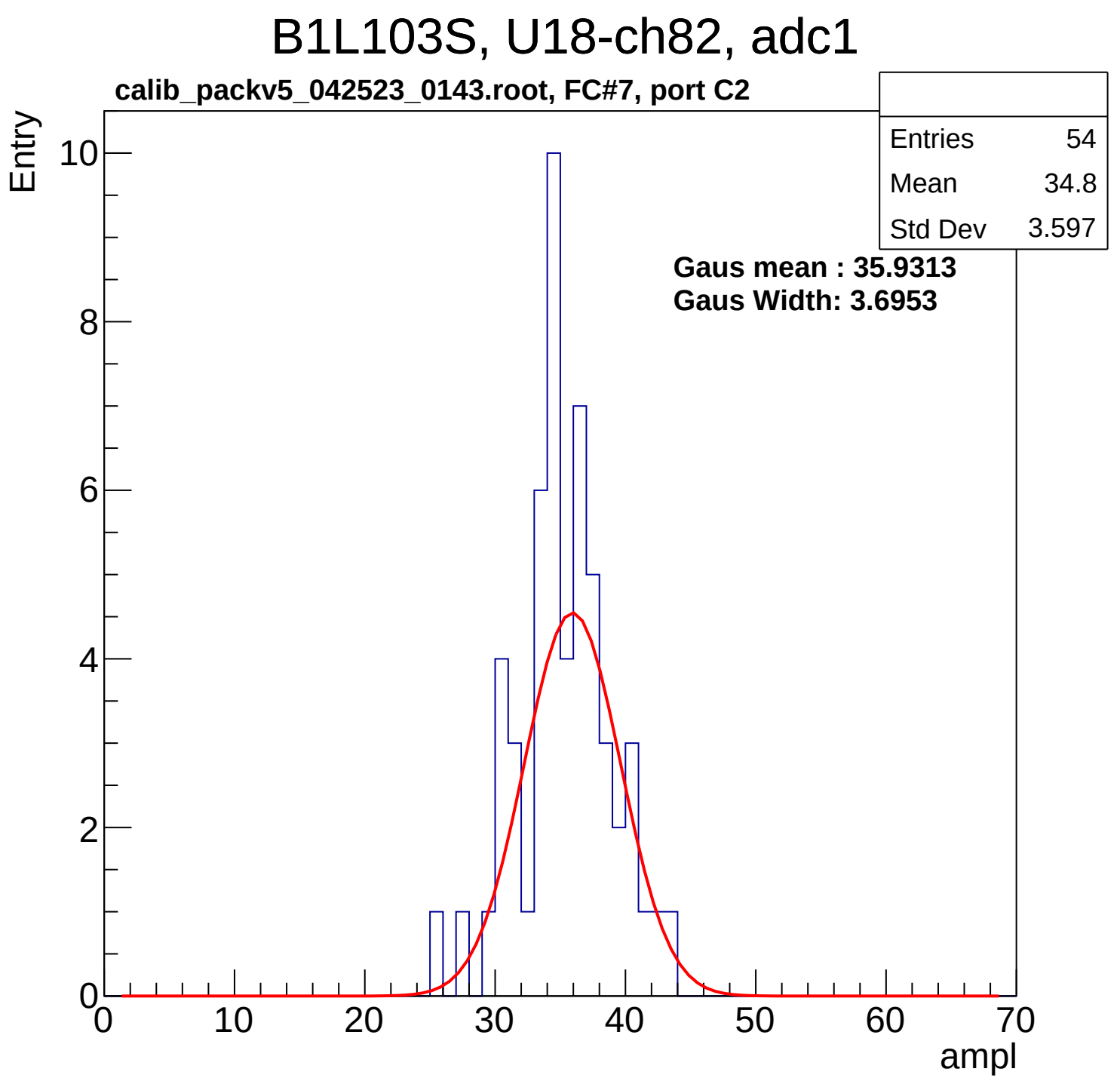
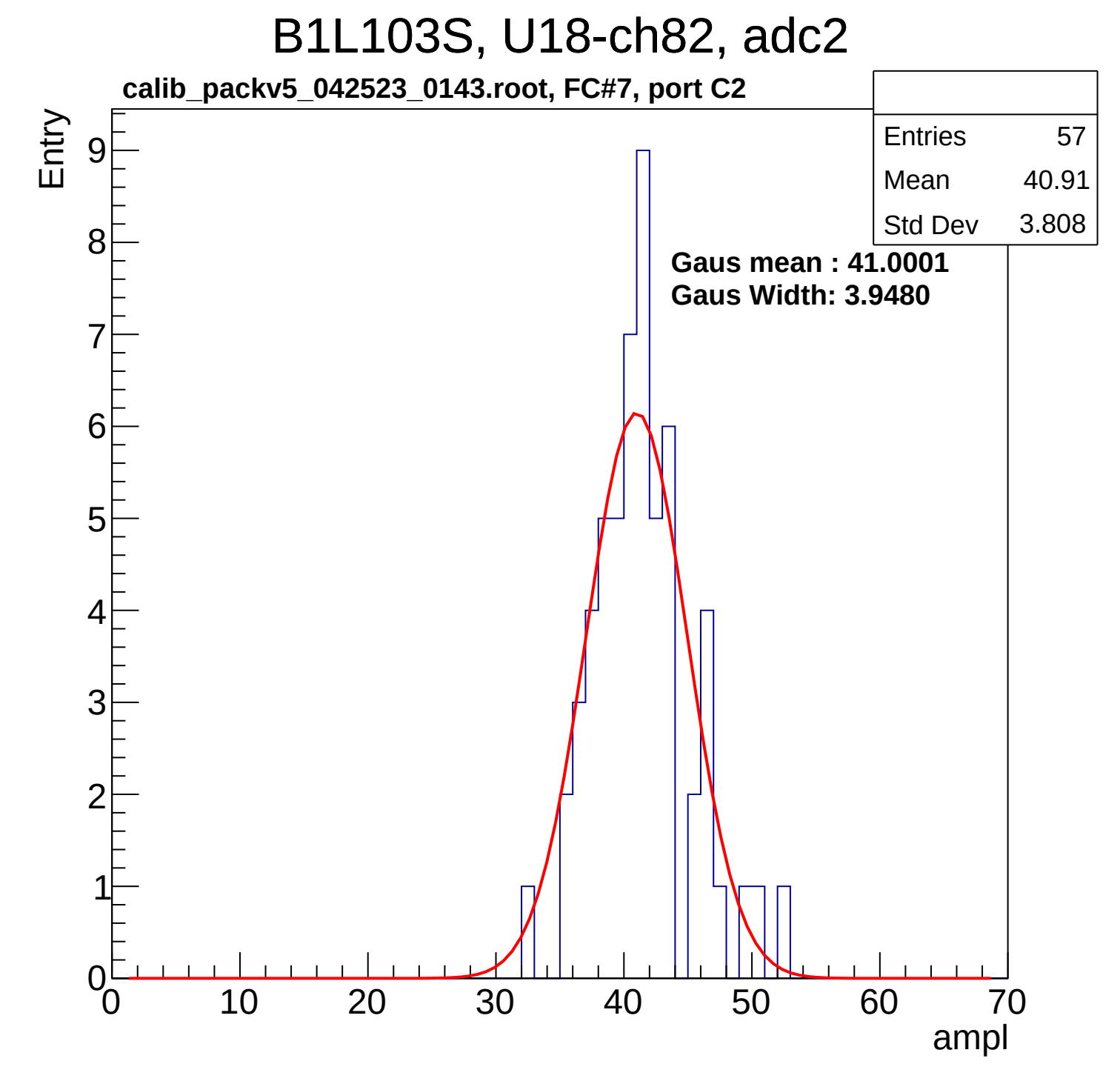

B1L103S, U18-ch82, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 54
Mean 34.8
Std Dev 3.597
Gaus mean : 35.9313
Gaus Width: 3.6953
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch82, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 40.91
Std Dev 3.808
Gaus mean : 41.0001
Gaus Width: 3.9480
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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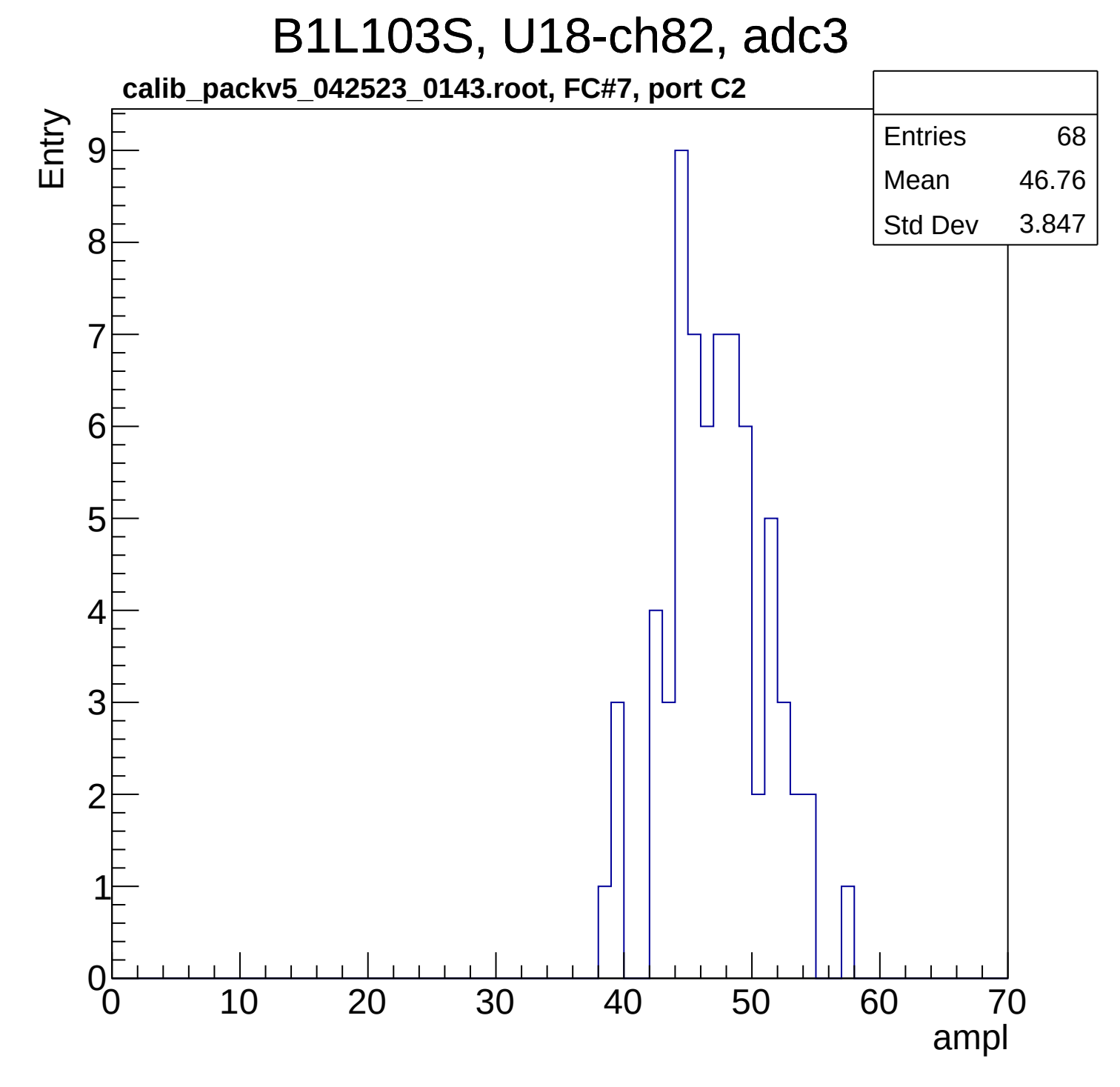
B1L103S, U18-ch82, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 46.76
Std Dev 3.847
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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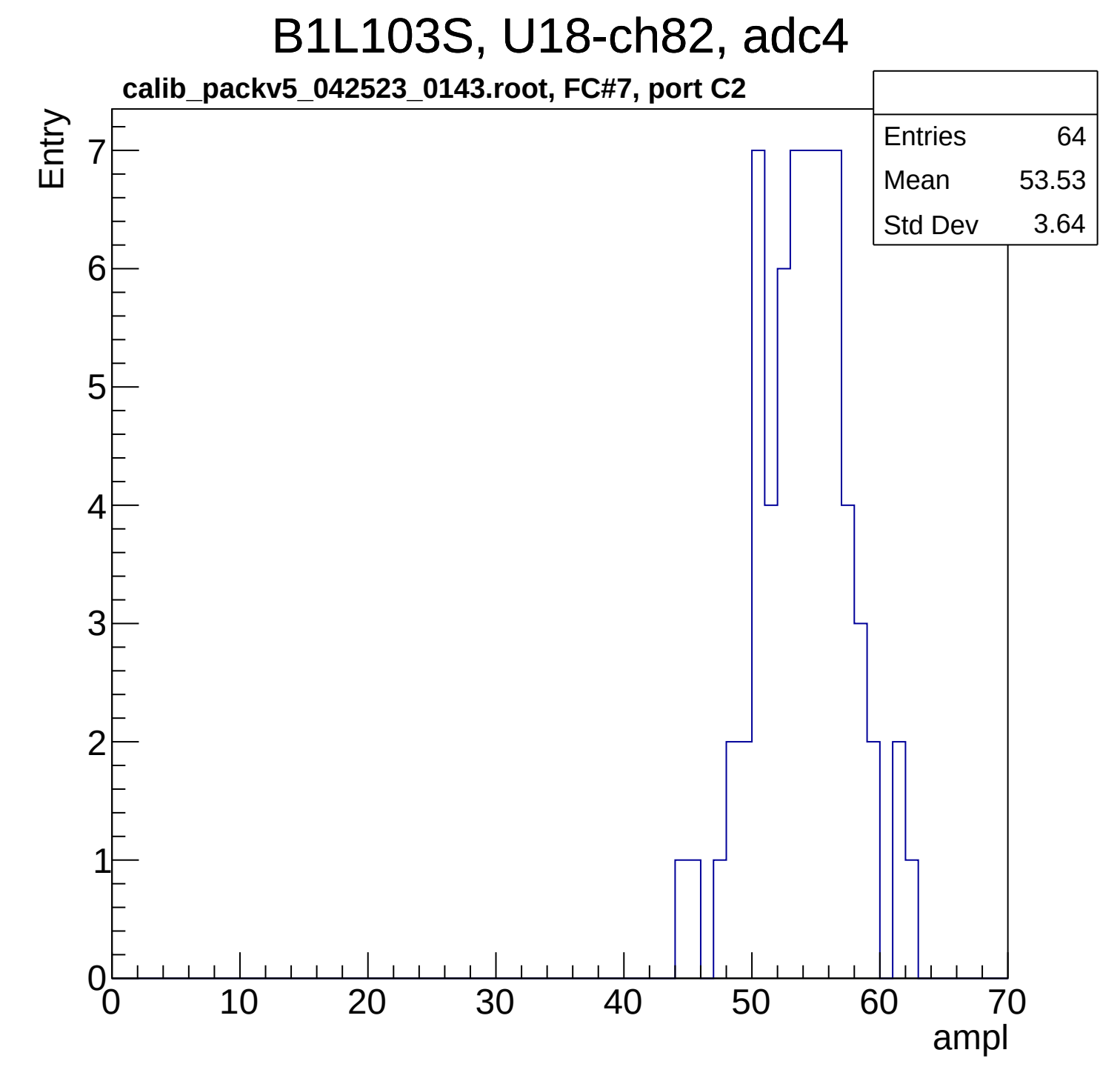
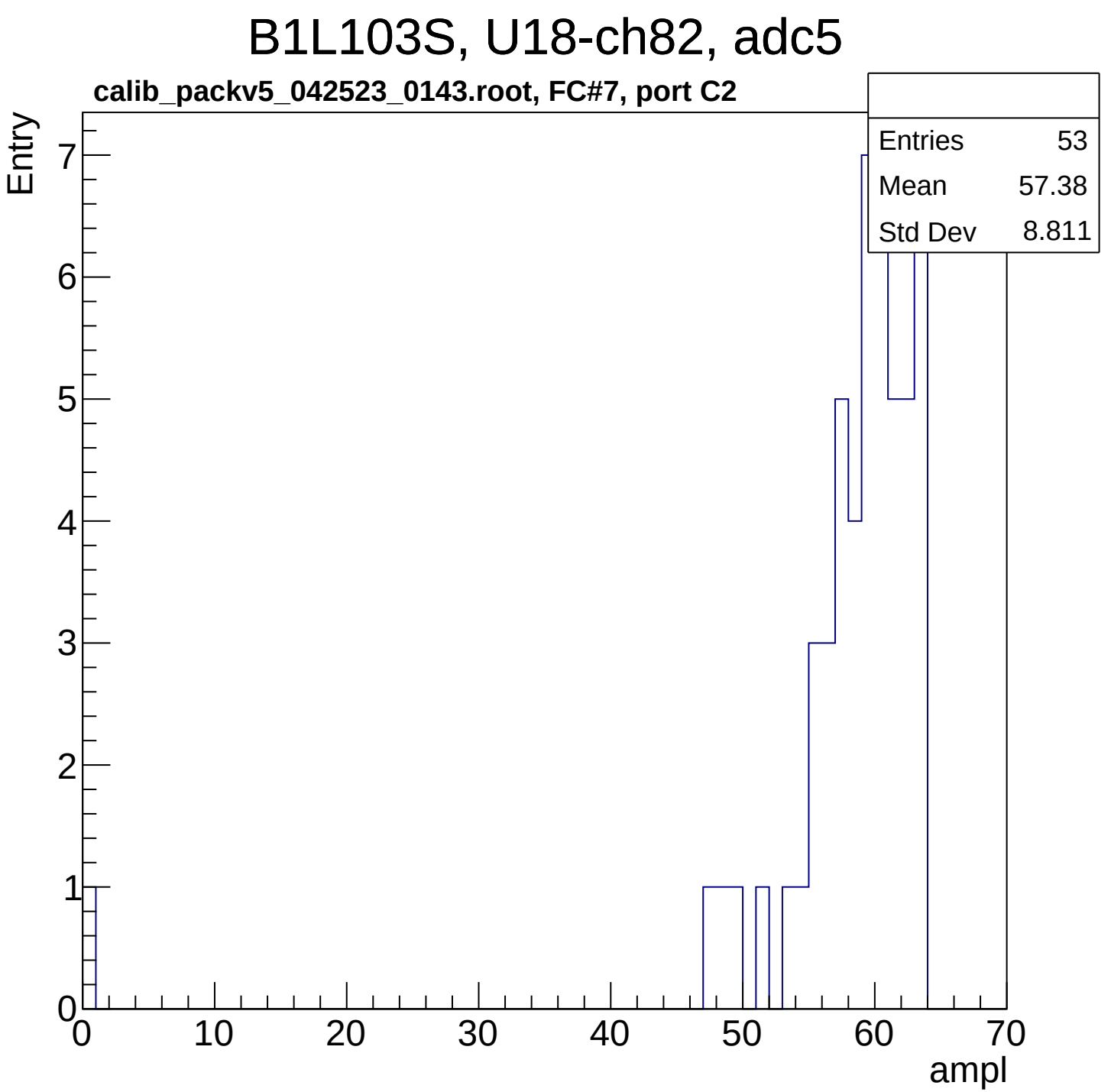

B1L103S, U18-ch82, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 53.53
Std Dev 3.64
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch82, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 57.38
Std Dev 8.811
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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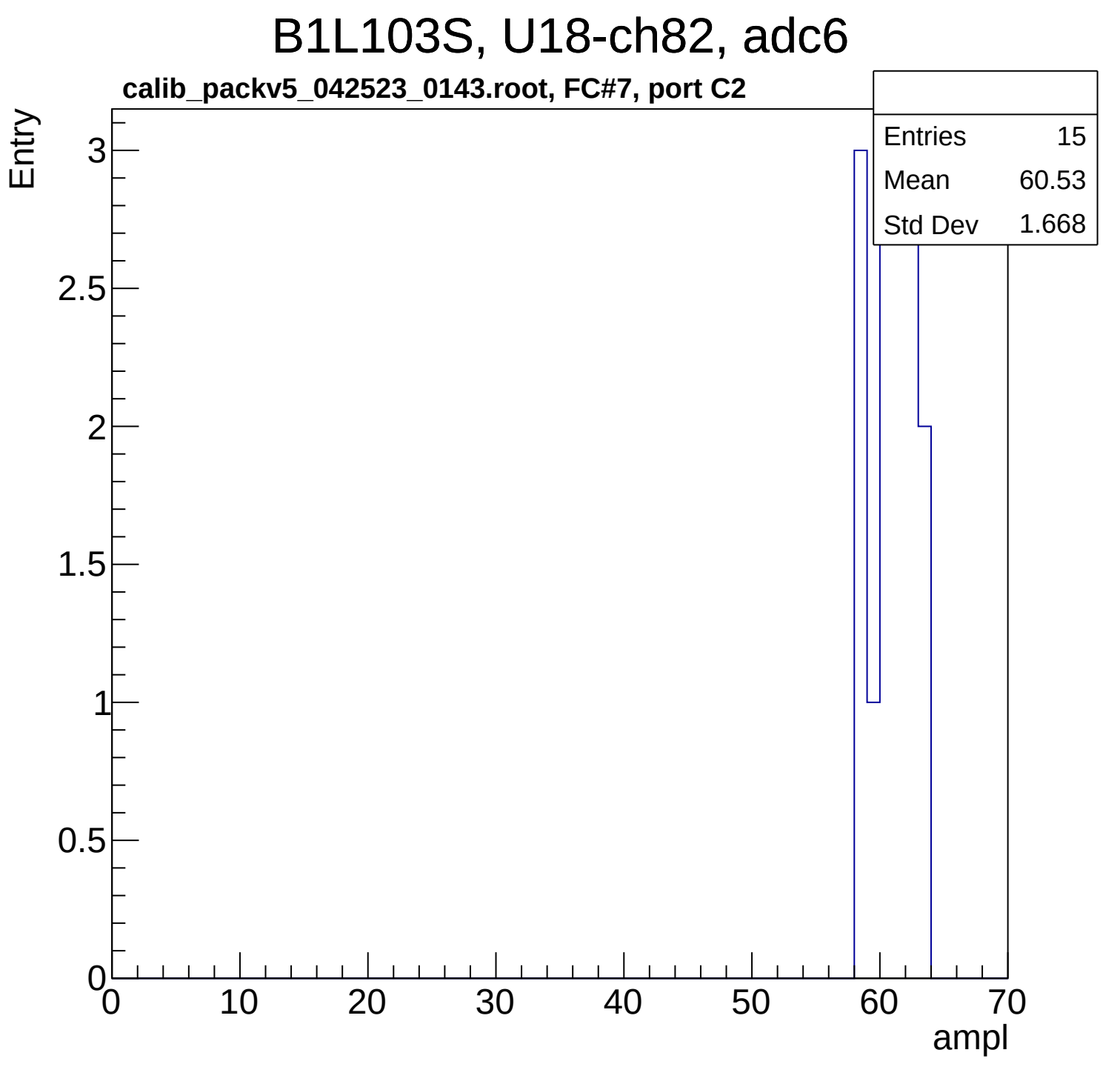
B1L103S, U18-ch82, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 15
Mean 60.53
Std Dev 1.668
Entry
ampl
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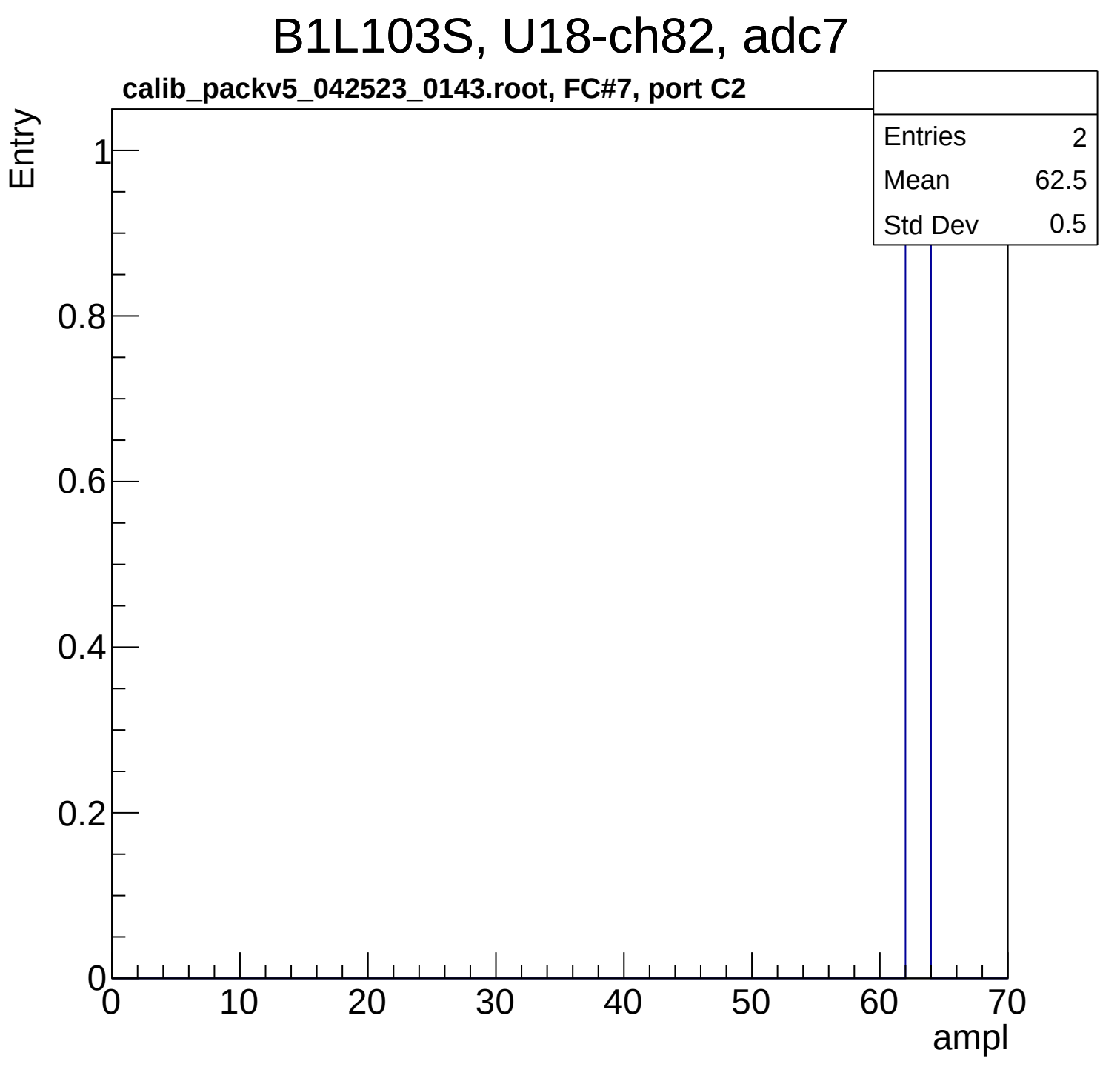
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U18-ch82, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
1
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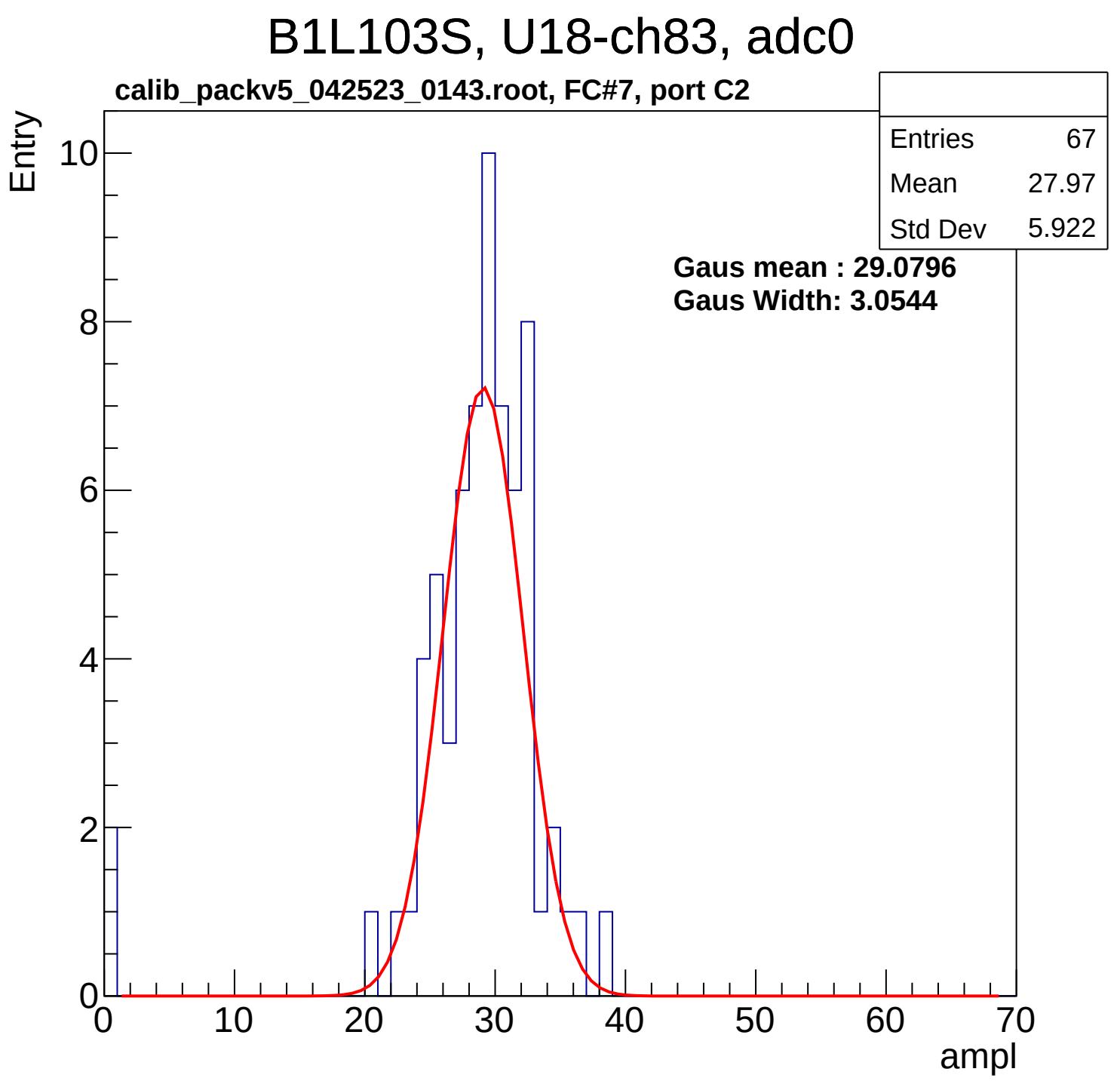
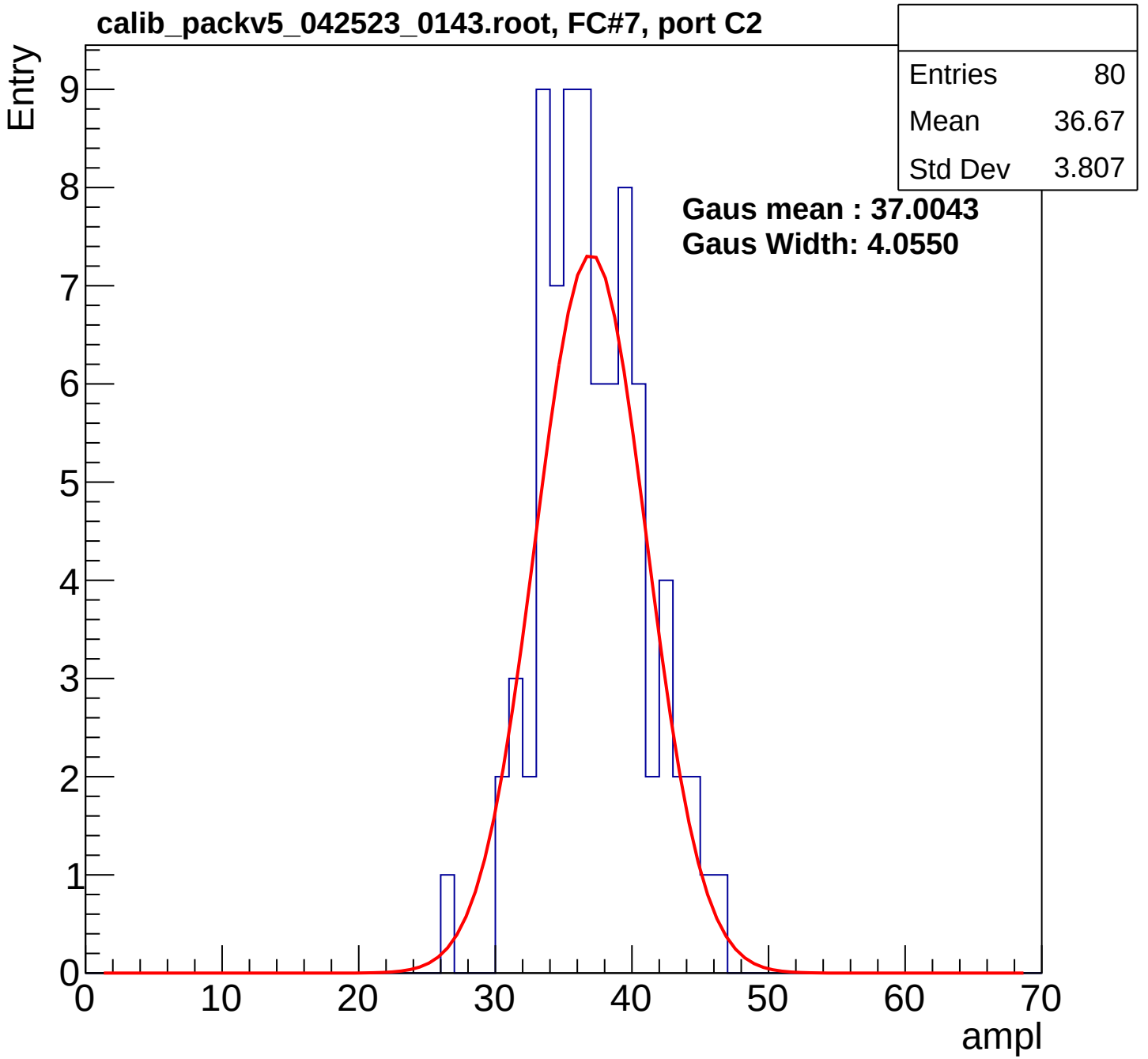
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch83, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 27.97
Std Dev 5.922
Gaus mean : 29.0796
Gaus Width: 3.0544
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch83, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 80
Mean 36.67
Std Dev 3.807
Gaus mean : 37.0043
Gaus Width: 4.0550
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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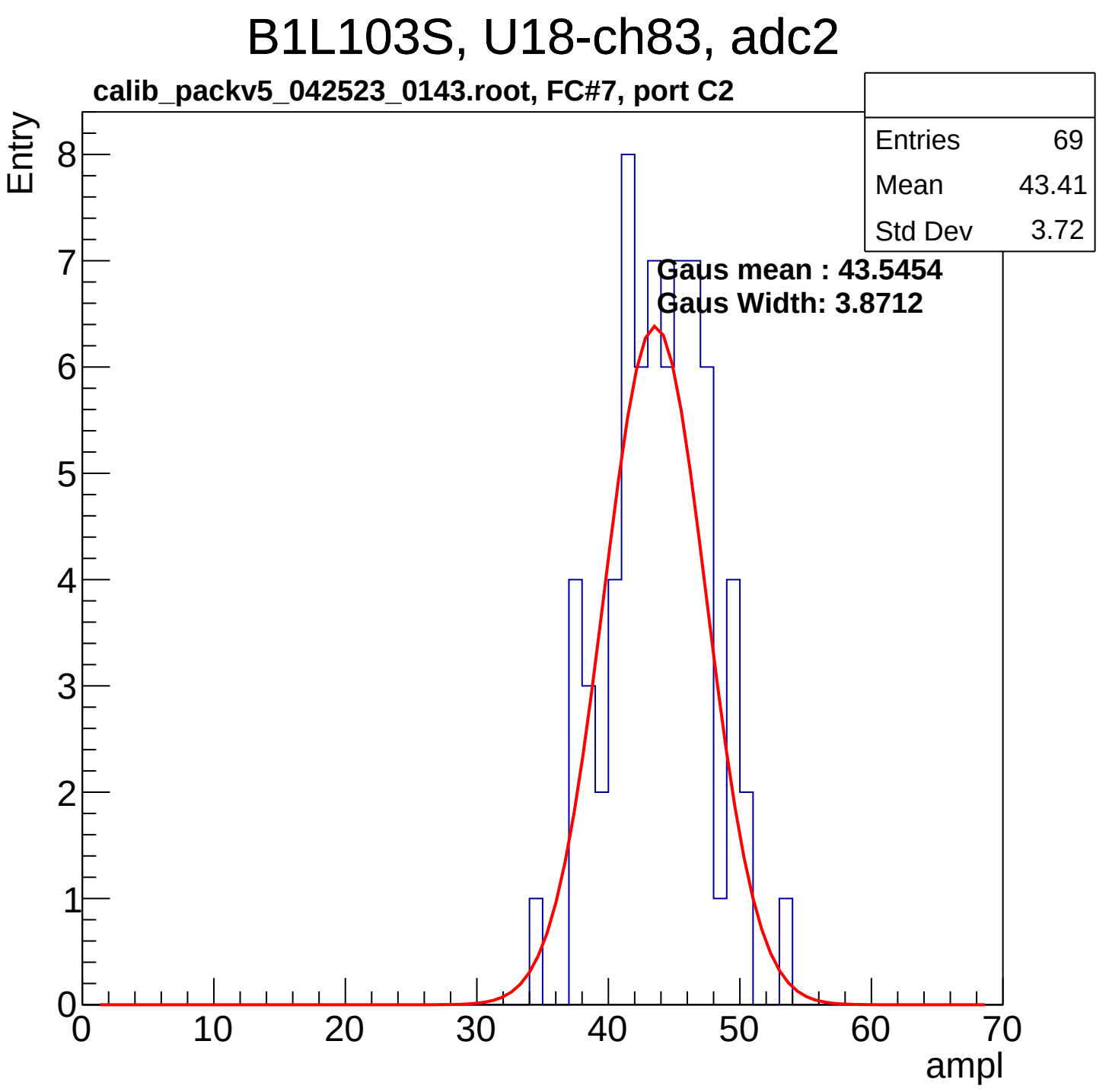
B1L103S, U18-ch83, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 43.41
Std Dev 3.72
Gaus mean : 43.5454
Gaus Width: 3.8712
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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20
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40
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60
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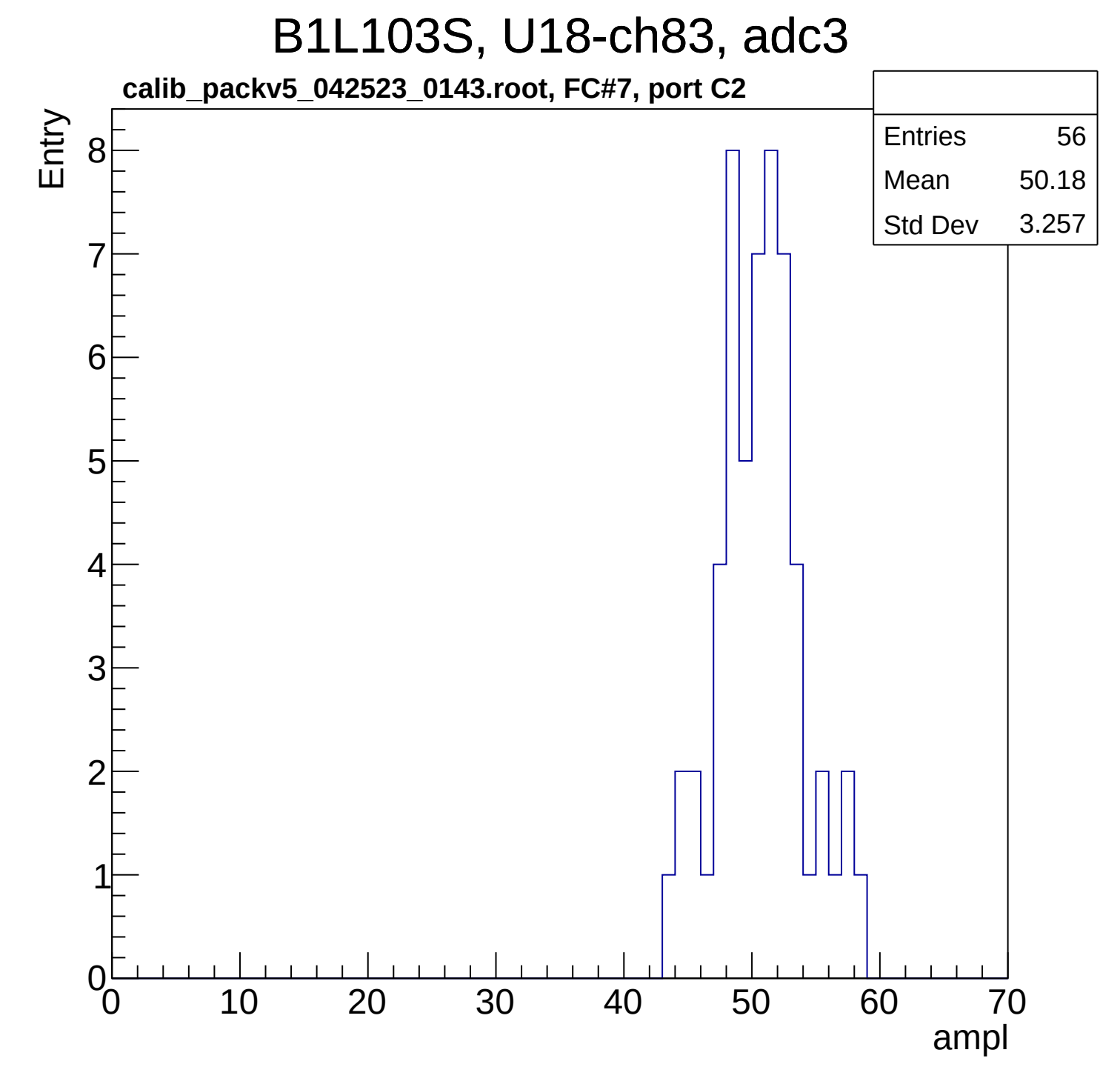
B1L103S, U18-ch83, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 50.18
Std Dev 3.257
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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60
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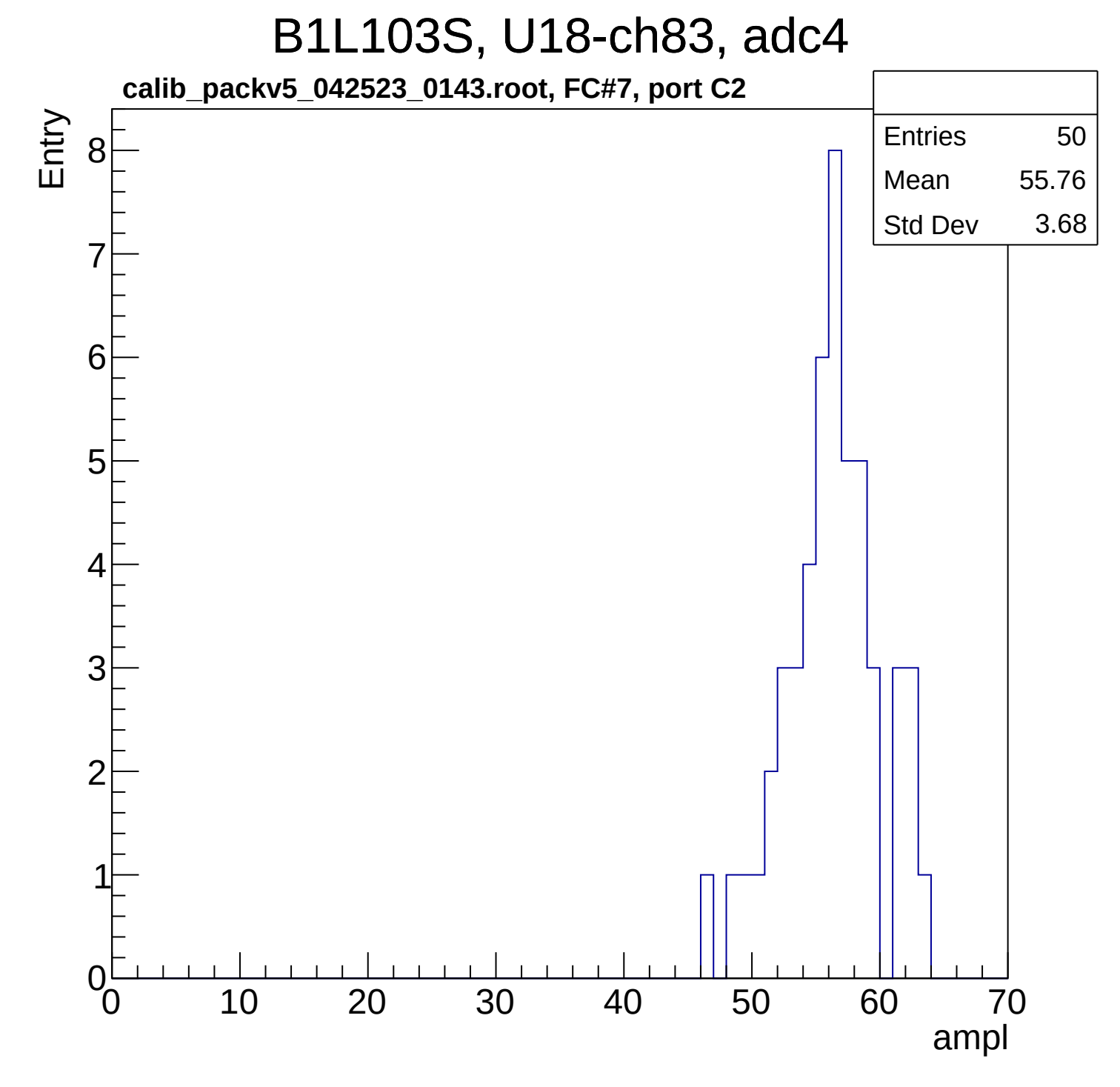
B1L103S, U18-ch83, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 50
Mean 55.76
Std Dev 3.68
Entry
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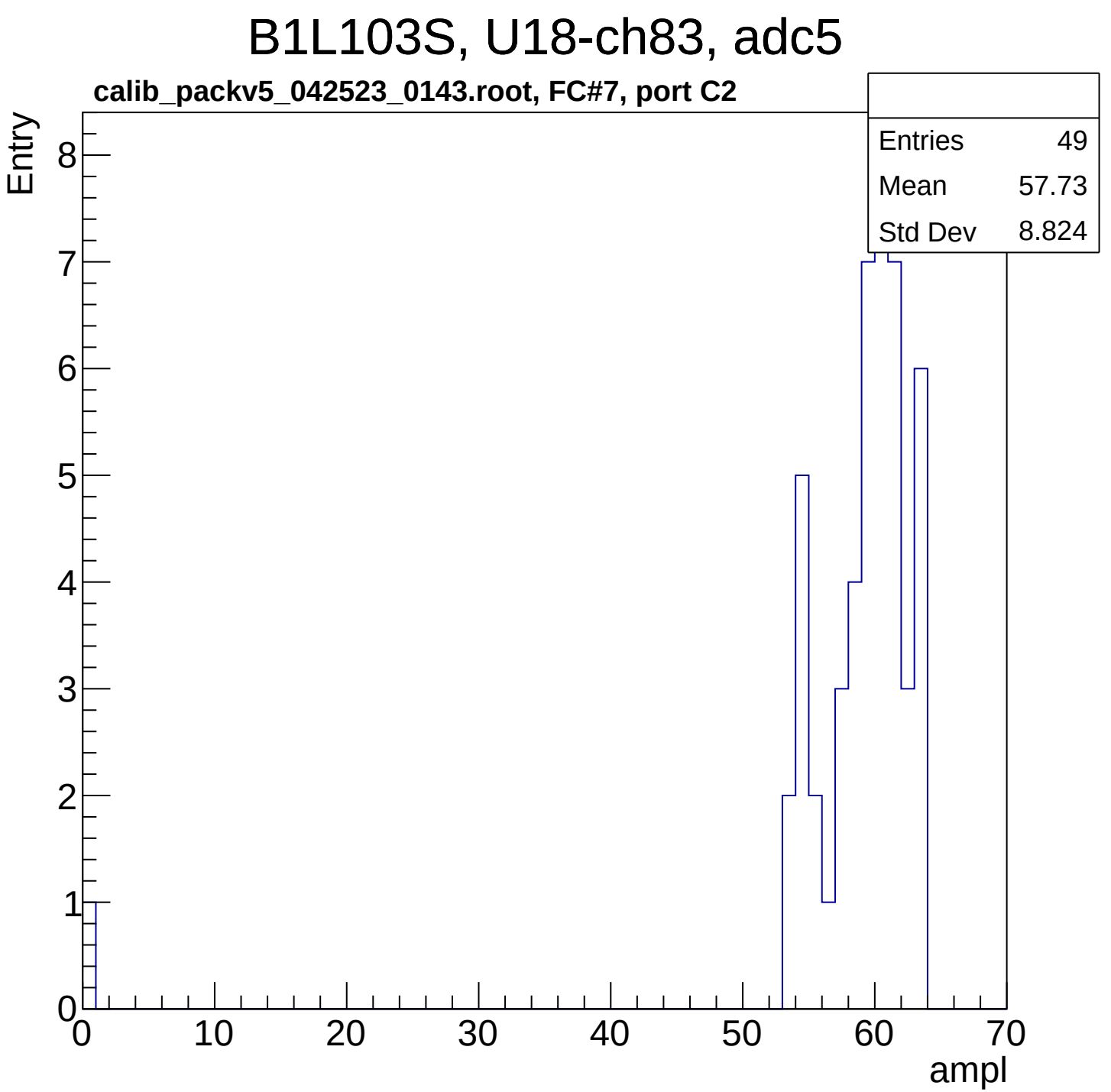
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch83, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 49
Mean 57.73
Std Dev 8.824
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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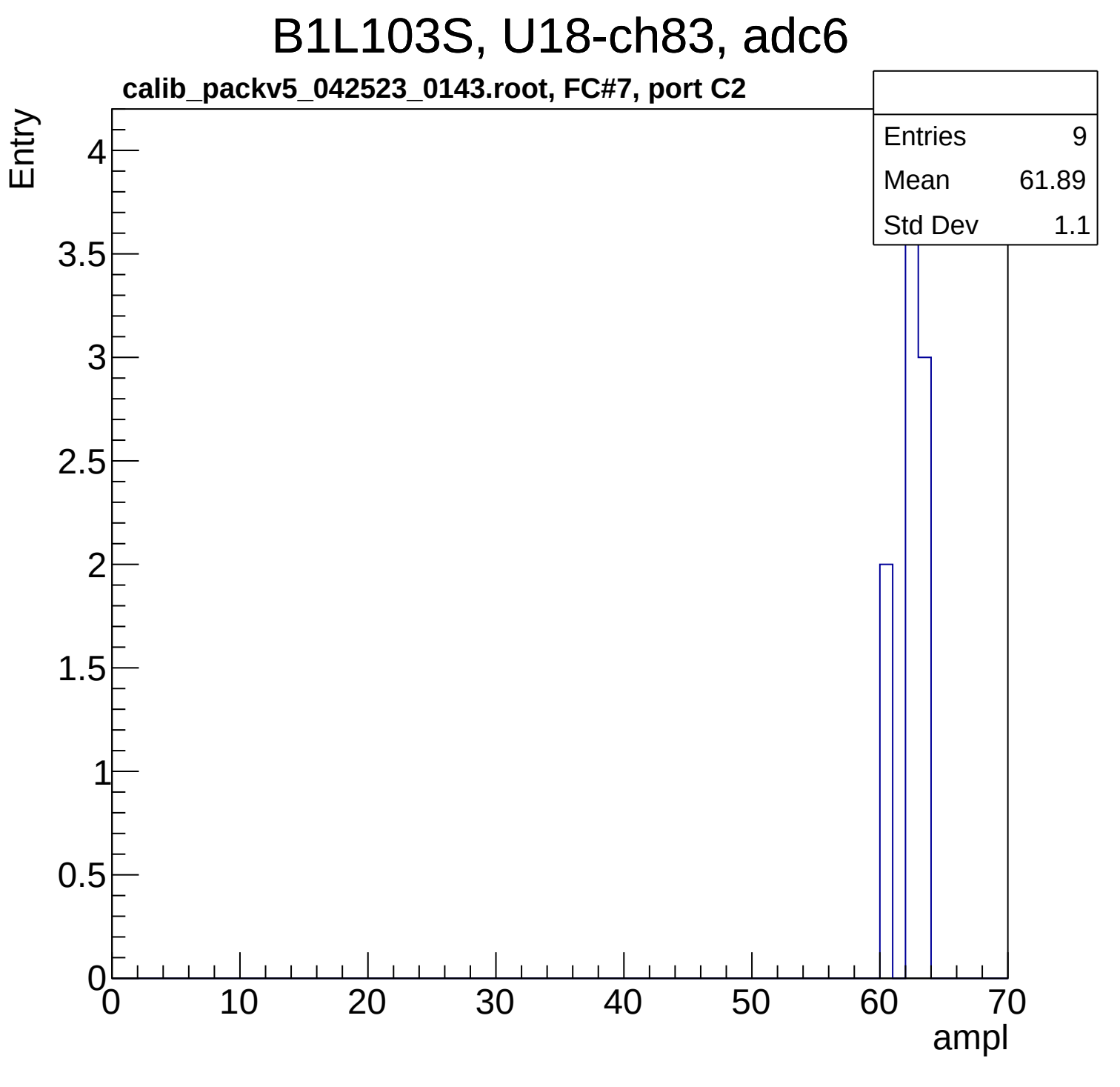
B1L103S, U18-ch83, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 9
Mean 61.89
Std Dev 1.1
Entry
ampl
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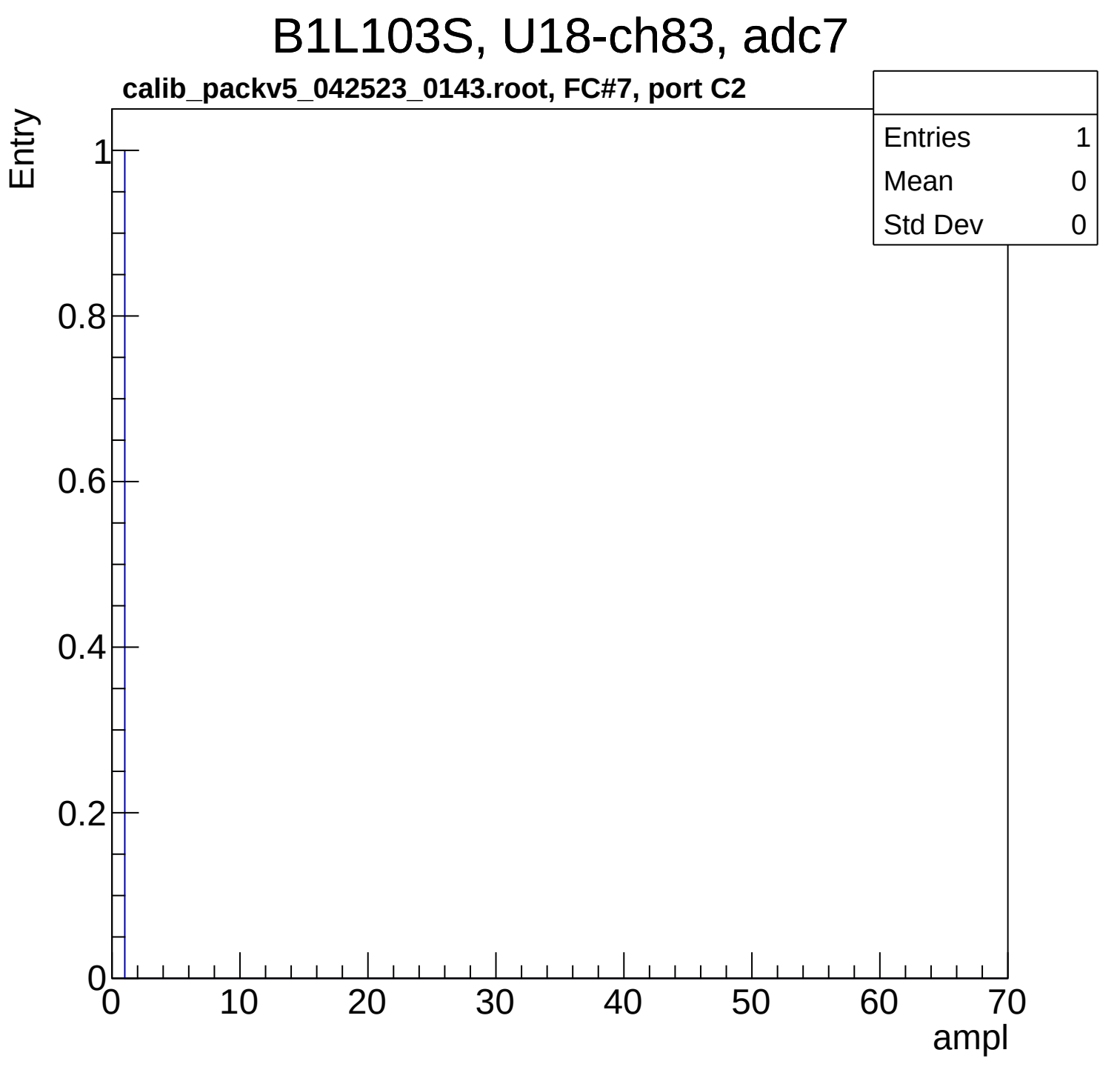
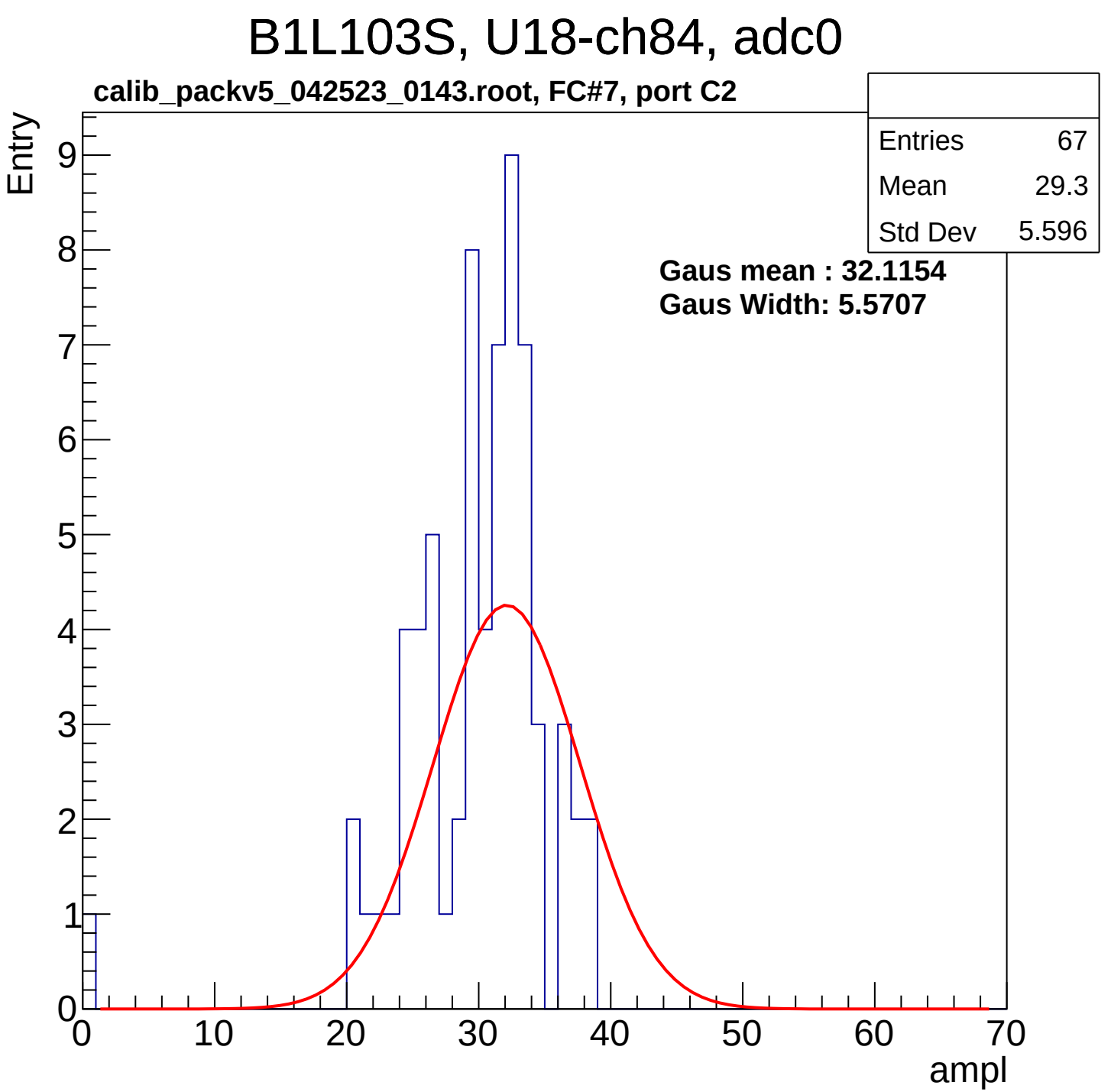
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U18-ch83, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch84, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 29.3
Std Dev 5.596
Gaus mean : 32.1154
Gaus Width: 5.5707
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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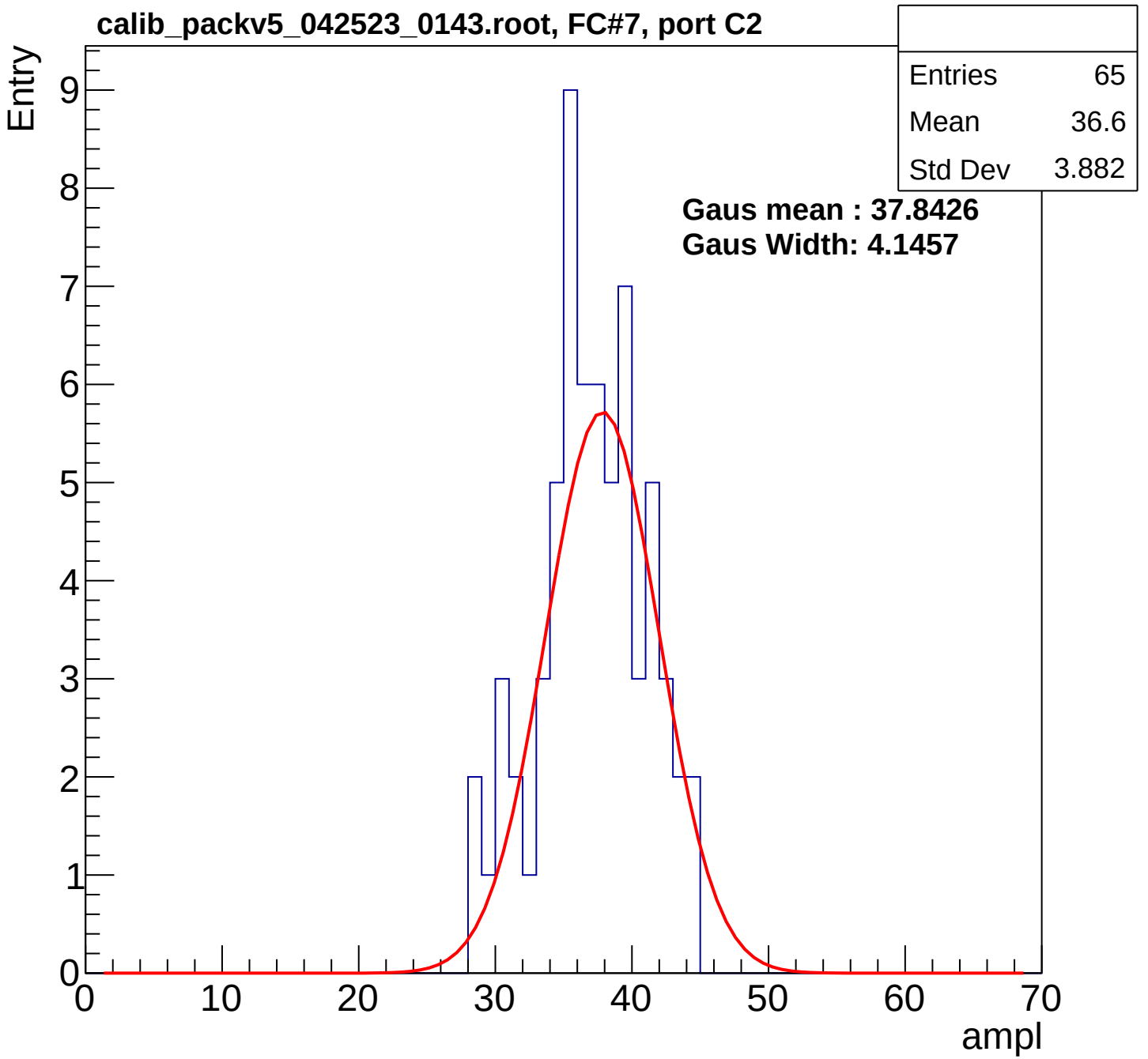
B1L103S, U18-ch84, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 36.6
Std Dev 3.882
Gaus mean : 37.8426
Gaus Width: 4.1457
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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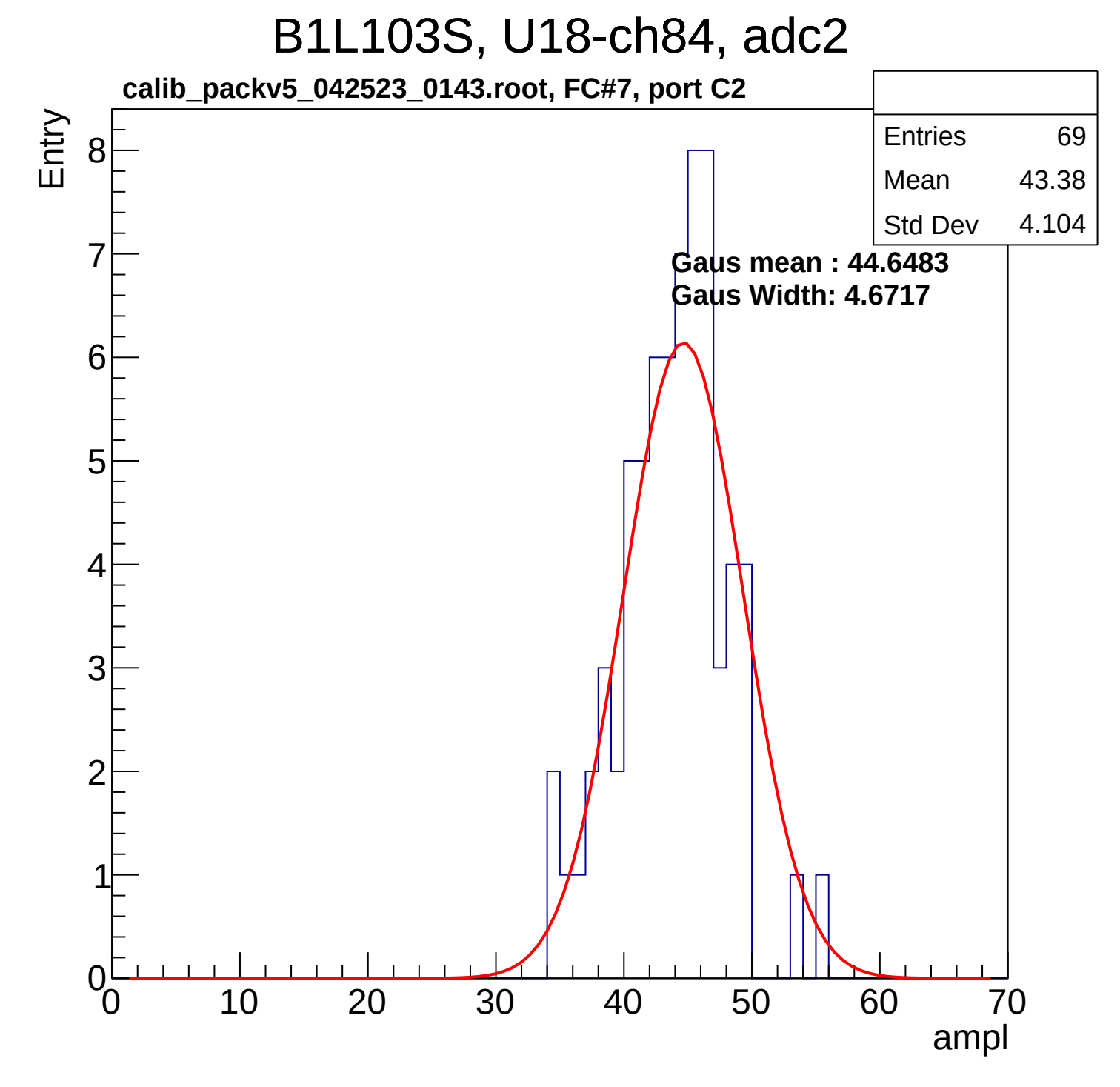
B1L103S, U18-ch84, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 43.38
Std Dev 4.104
Gaus mean : 44.6483
Gaus Width: 4.6717
Entry
ampl
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1
2
3
4
5
6
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0
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60
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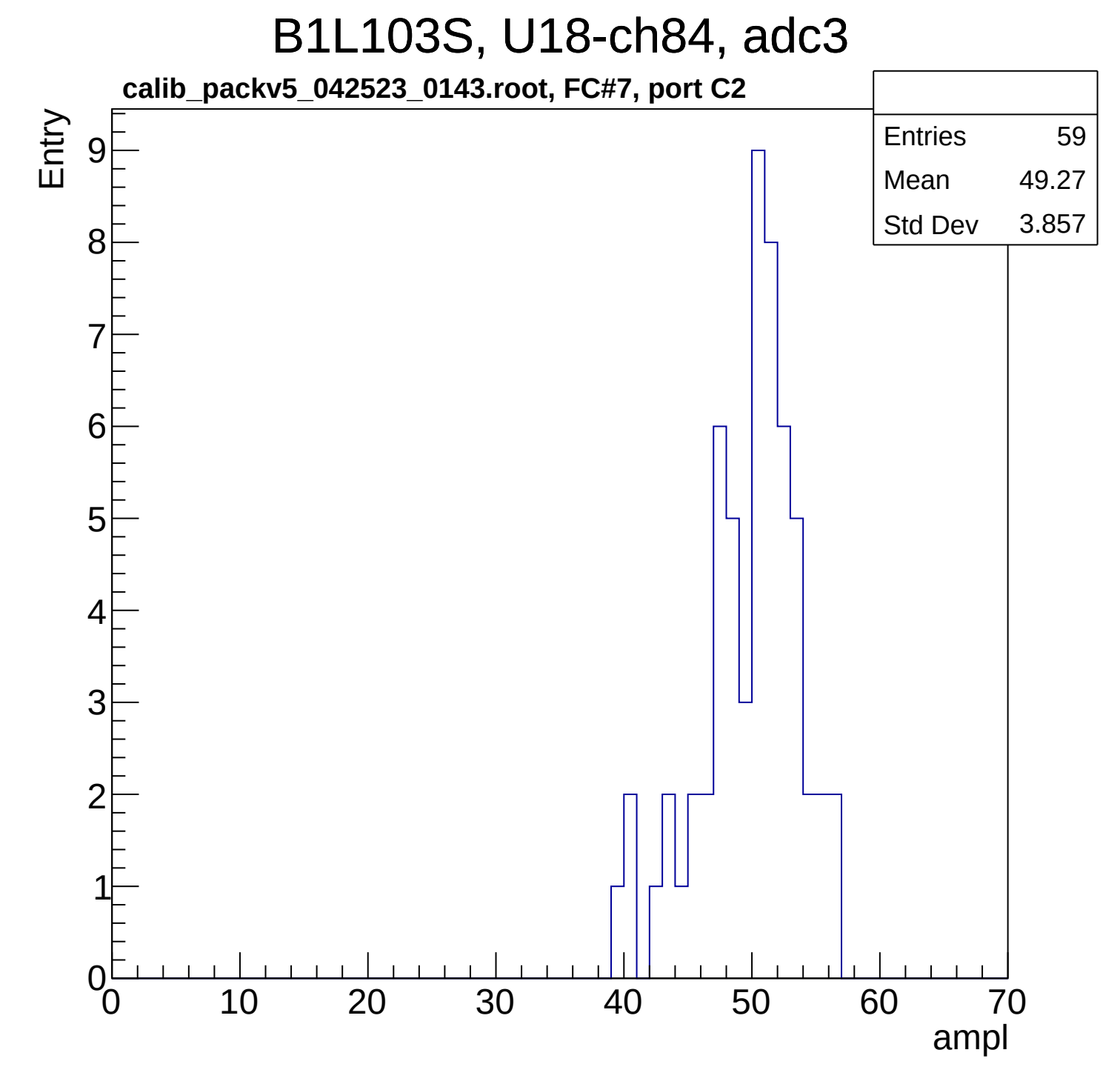
B1L103S, U18-ch84, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 49.27
Std Dev 3.857
Entry
ampl
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3
4
5
6
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9
0
10
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40
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60
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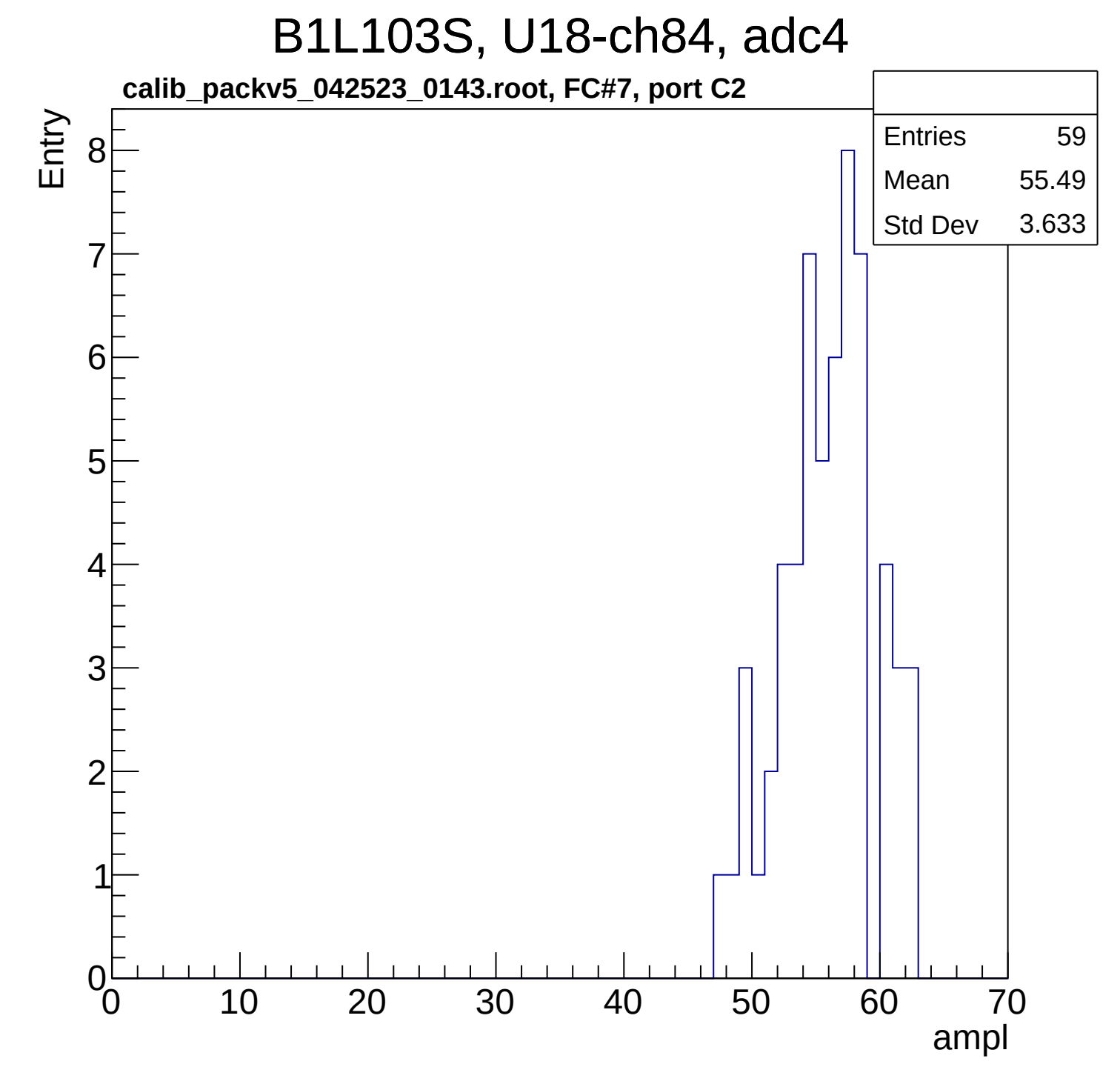
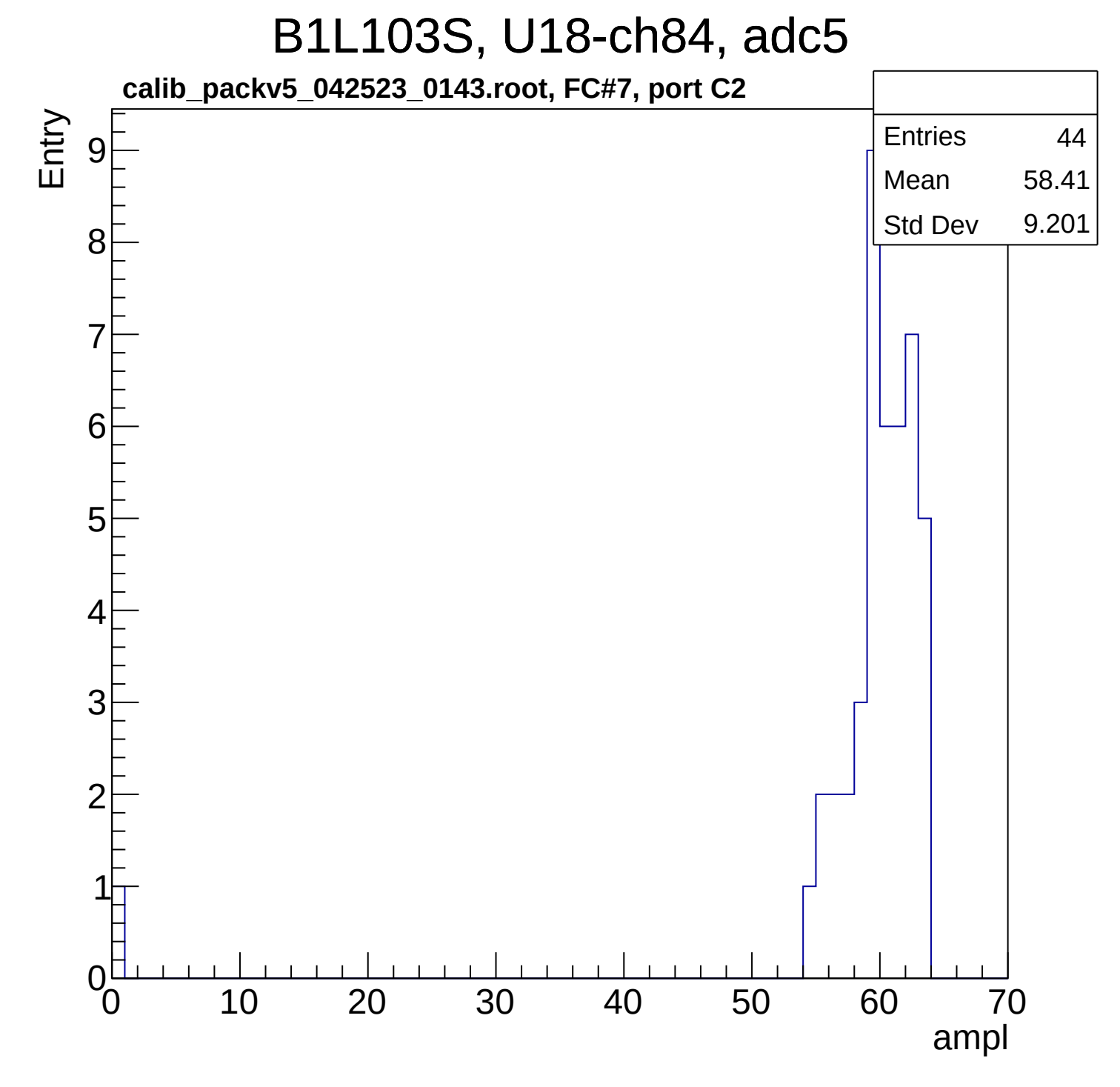

B1L103S, U18-ch84, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 55.49
Std Dev 3.633
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch84, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 44
Mean 58.41
Std Dev 9.201
Entry
ampl
0
1
2
3
4
5
6
7
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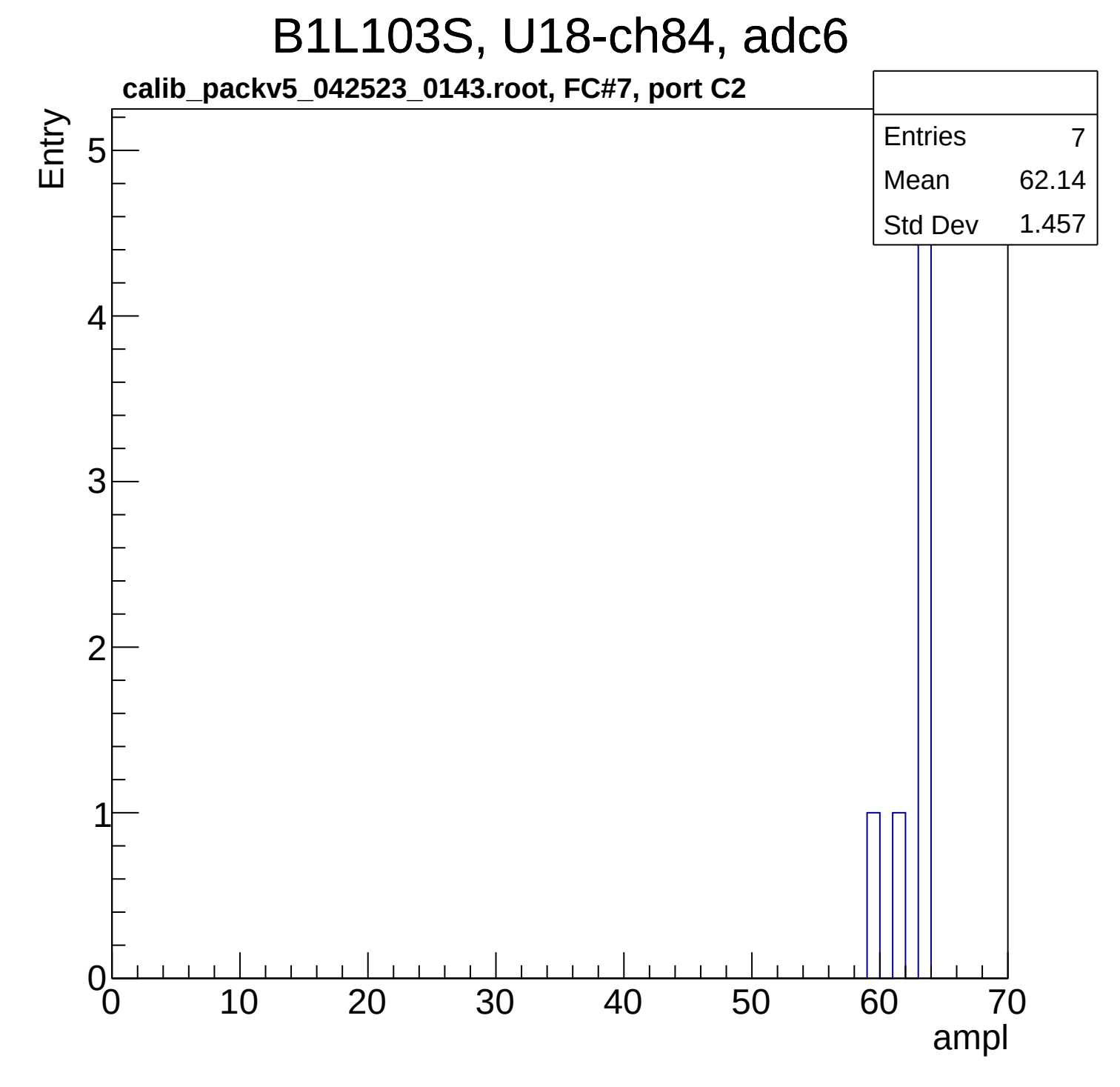
B1L103S, U18-ch84, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 7
Mean 62.14
Std Dev 1.457
Entry
ampl
0
1
2
3
4
5
0
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40
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60
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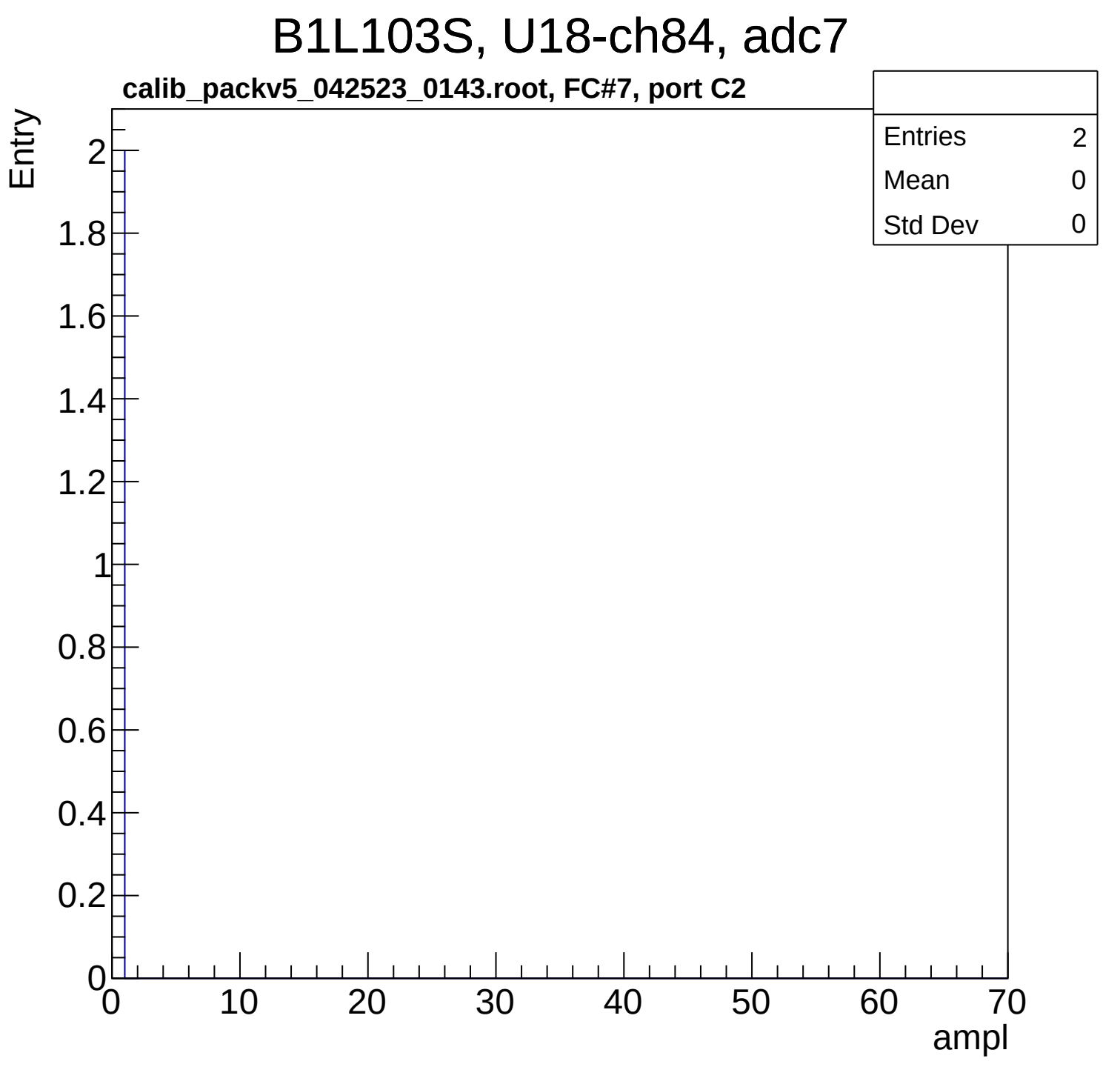
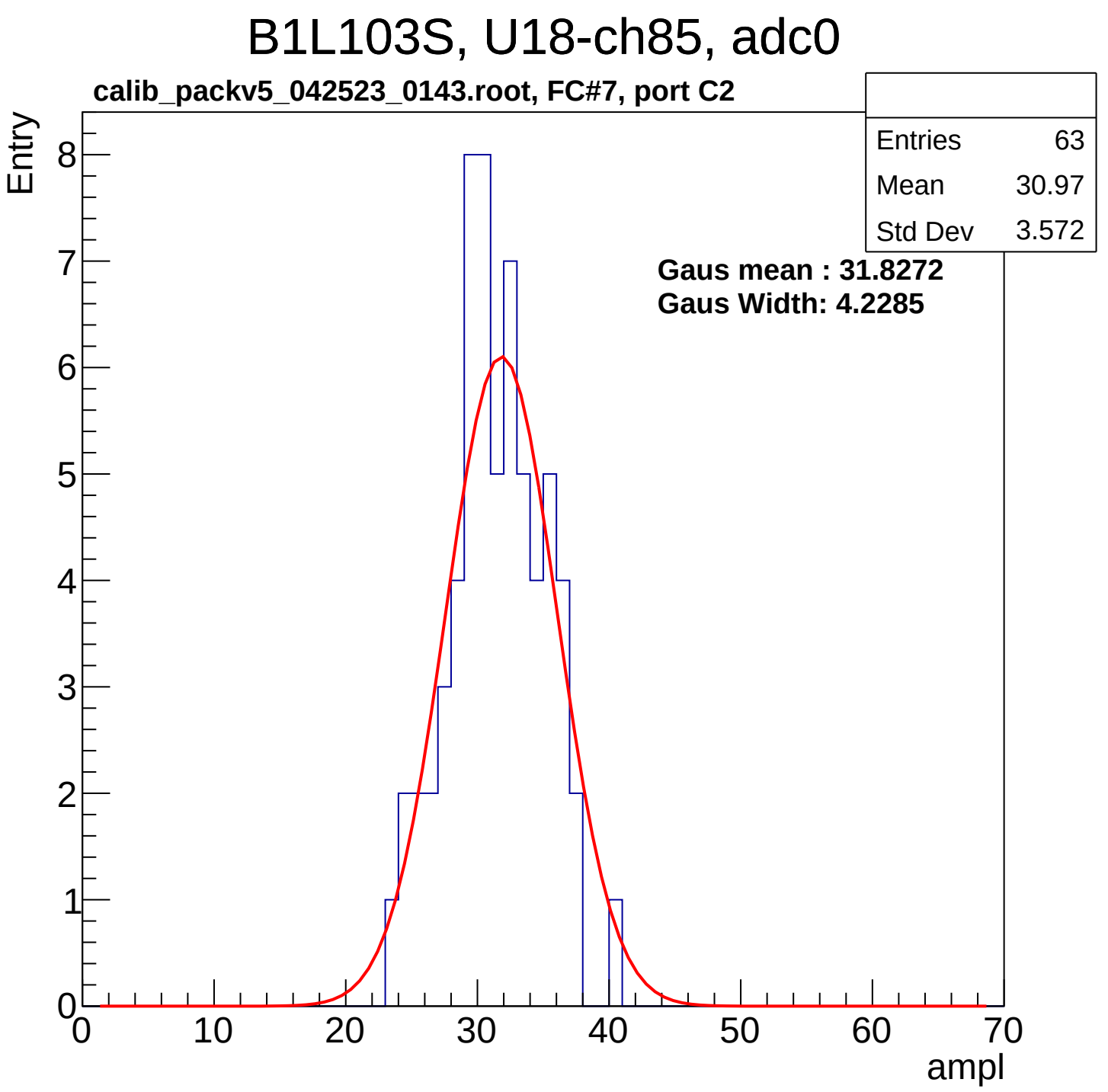
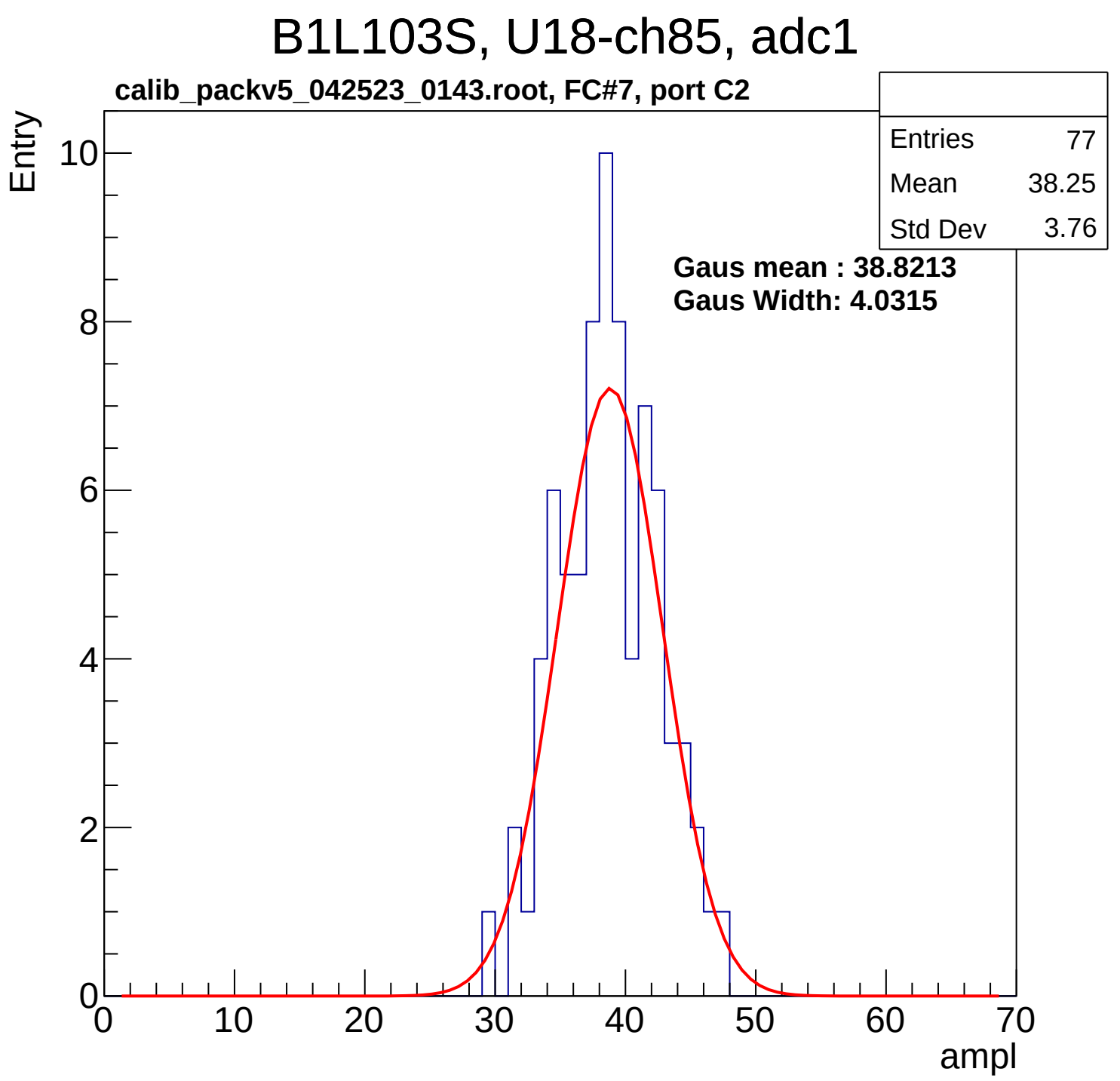
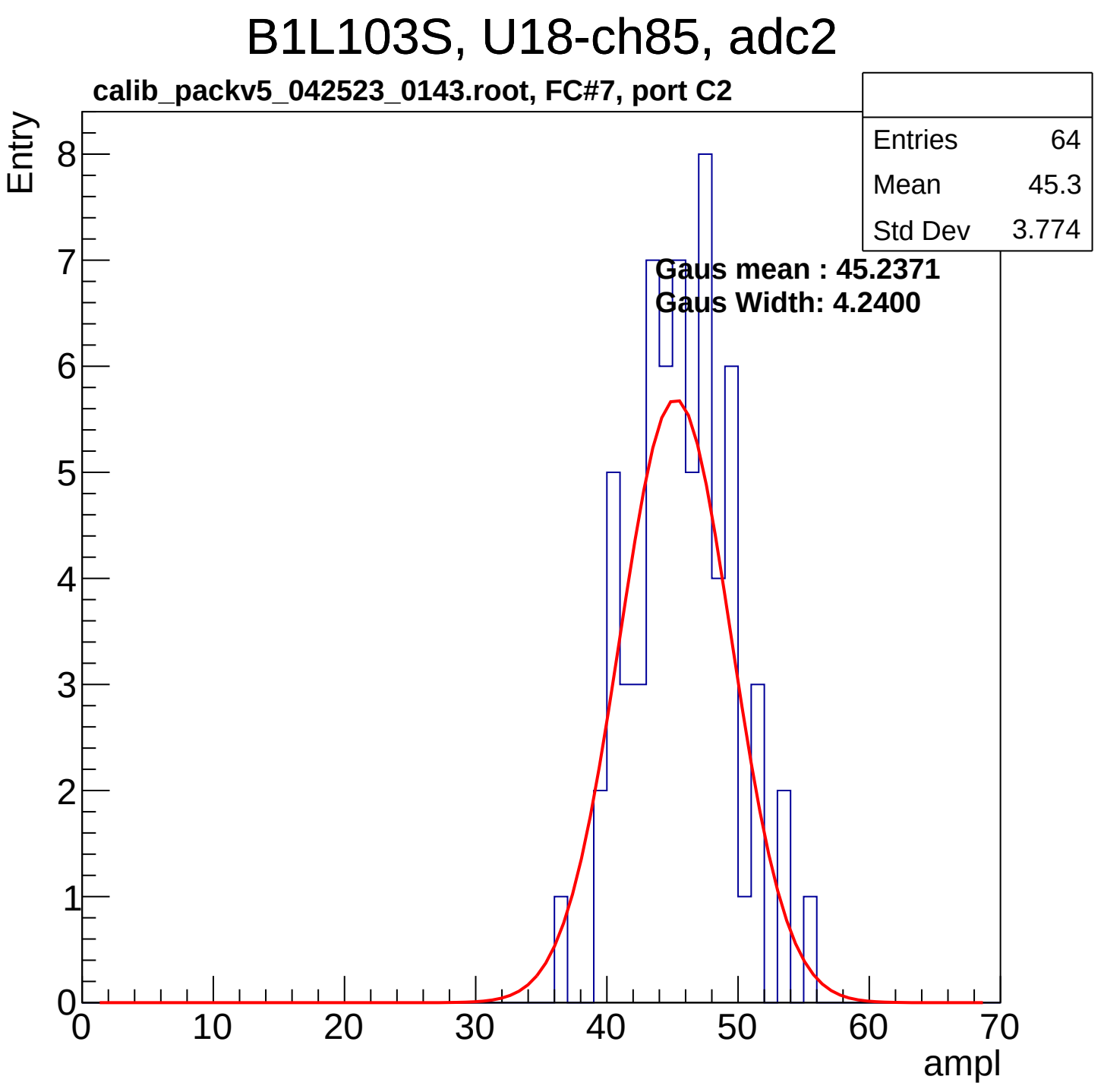

B1L103S, U18-ch84, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch85, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 30.97
Std Dev 3.572
Gaus mean : 31.8272
Gaus Width: 4.2285
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch85, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 77
Mean 38.25
Std Dev 3.76
Gaus mean : 38.8213
Gaus Width: 4.0315
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch85, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 45.3
Std Dev 3.774
Gaus mean : 45.2371
Gaus Width: 4.2400
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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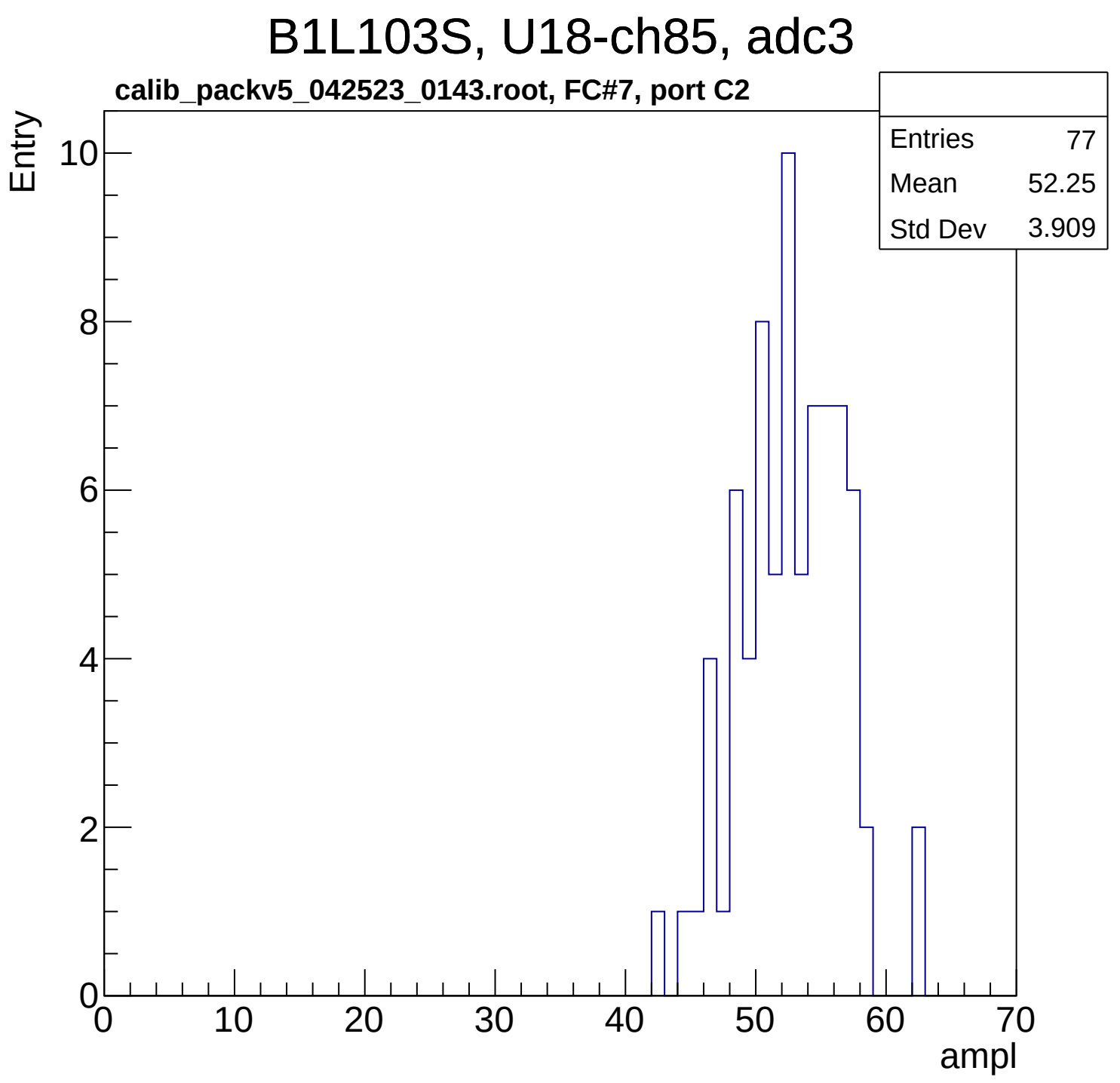
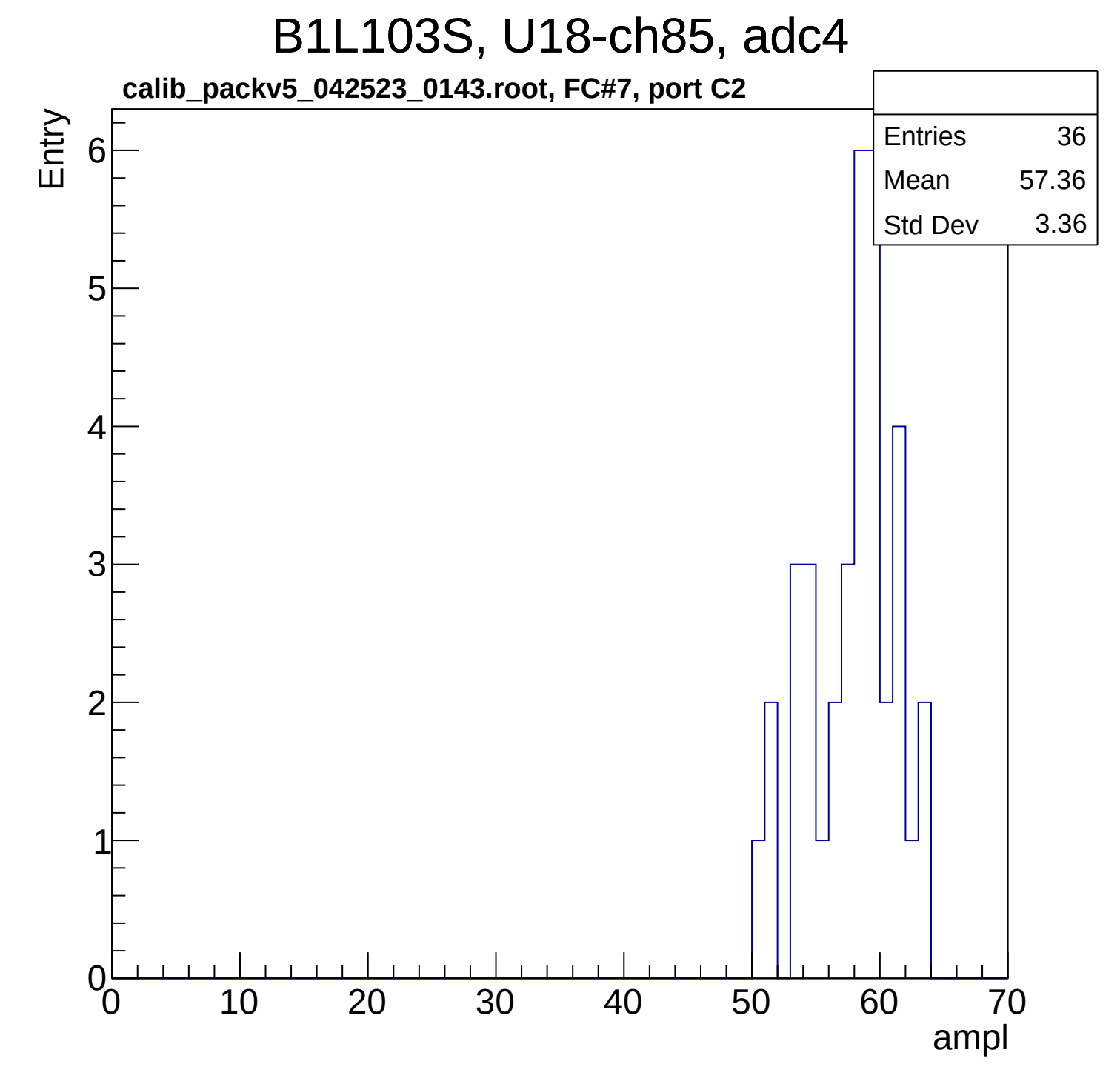
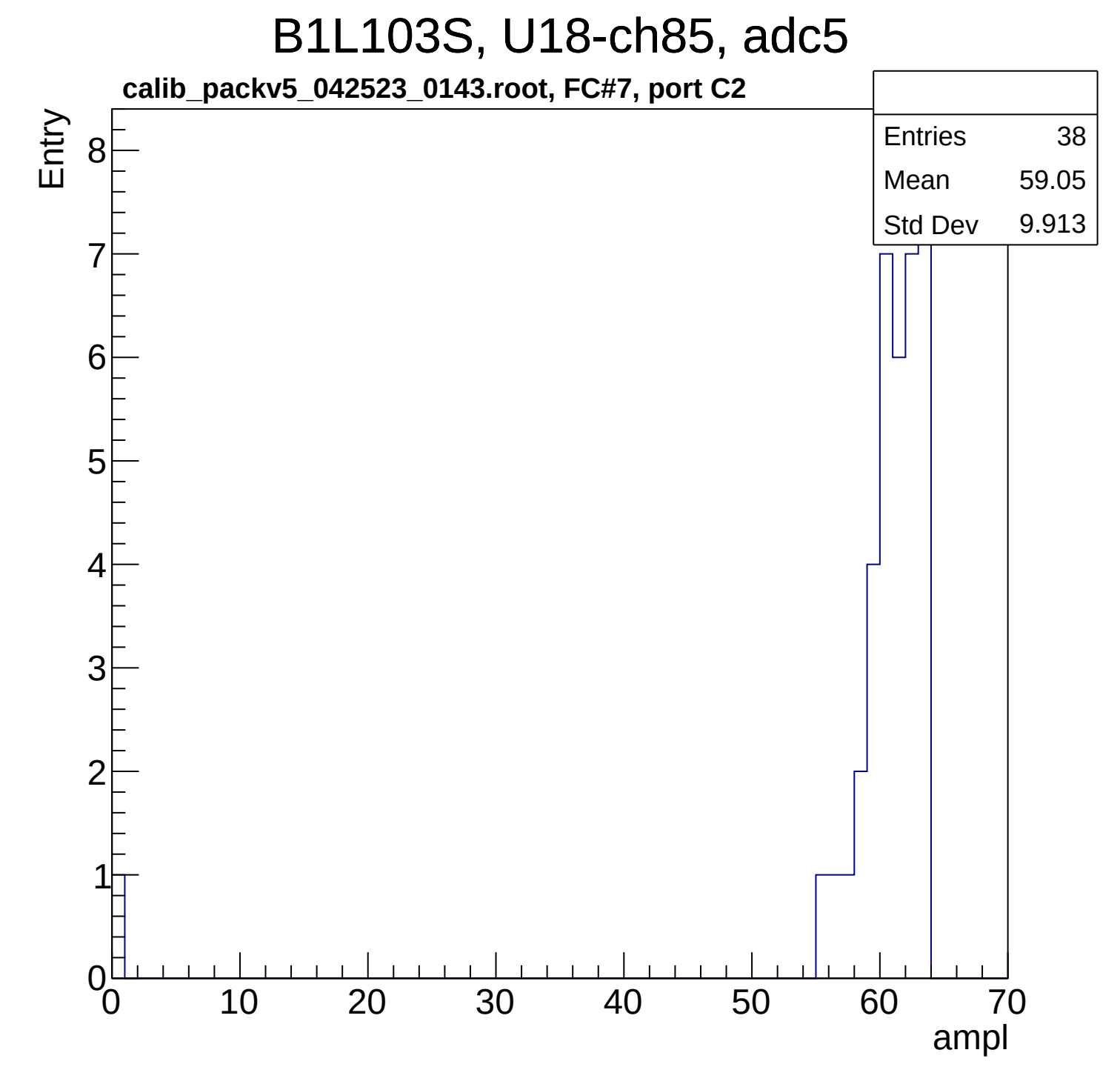
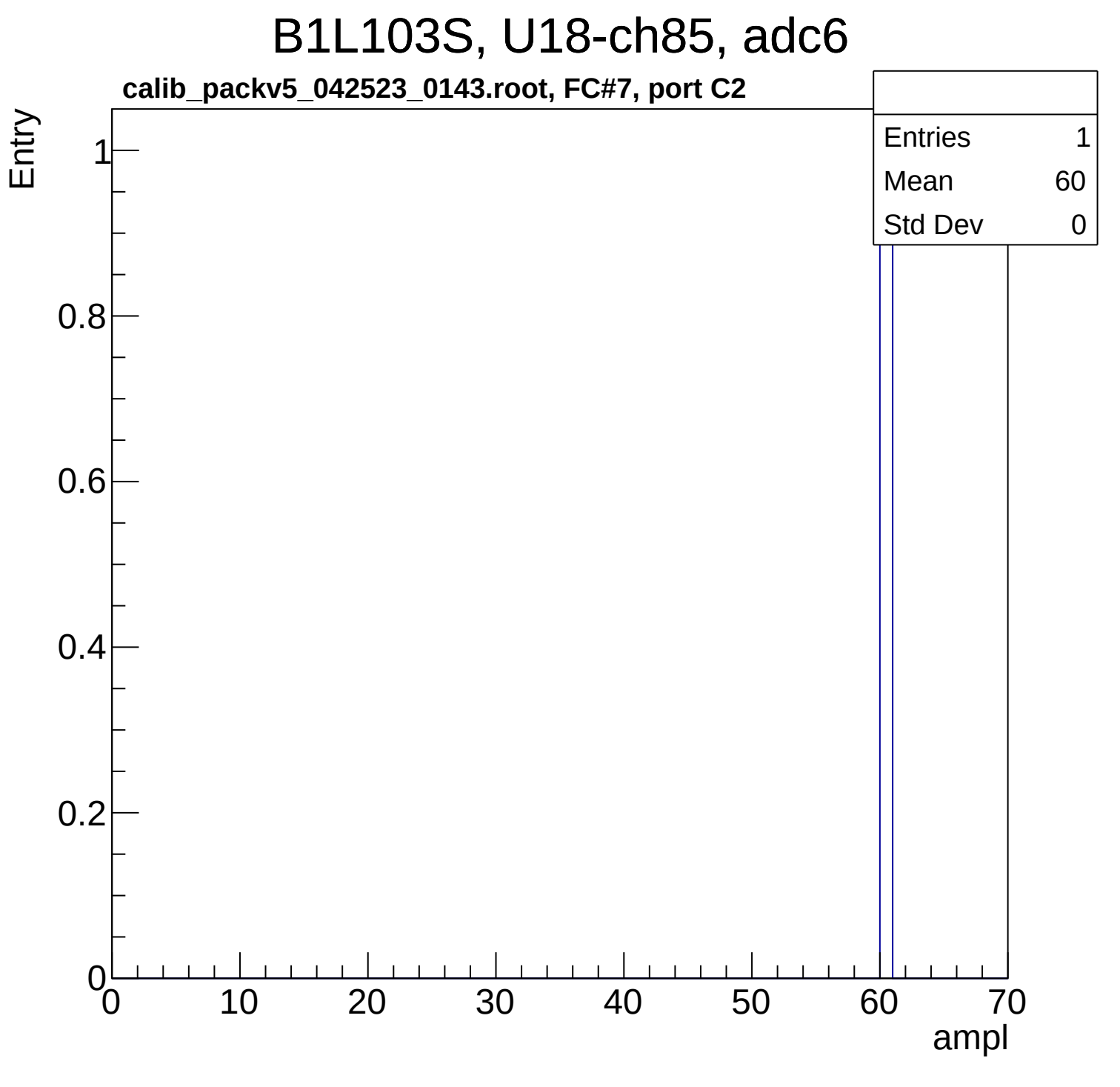
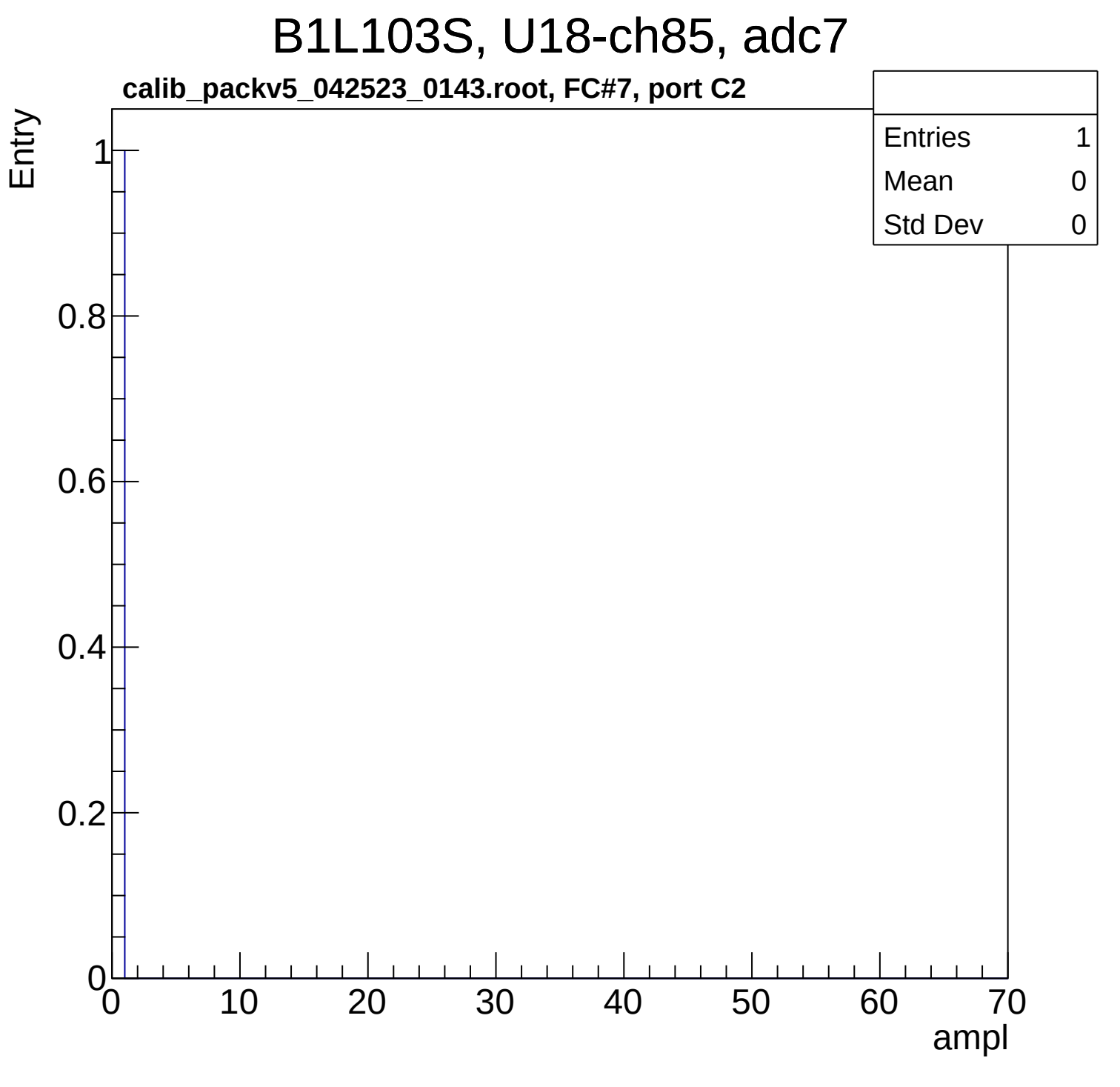
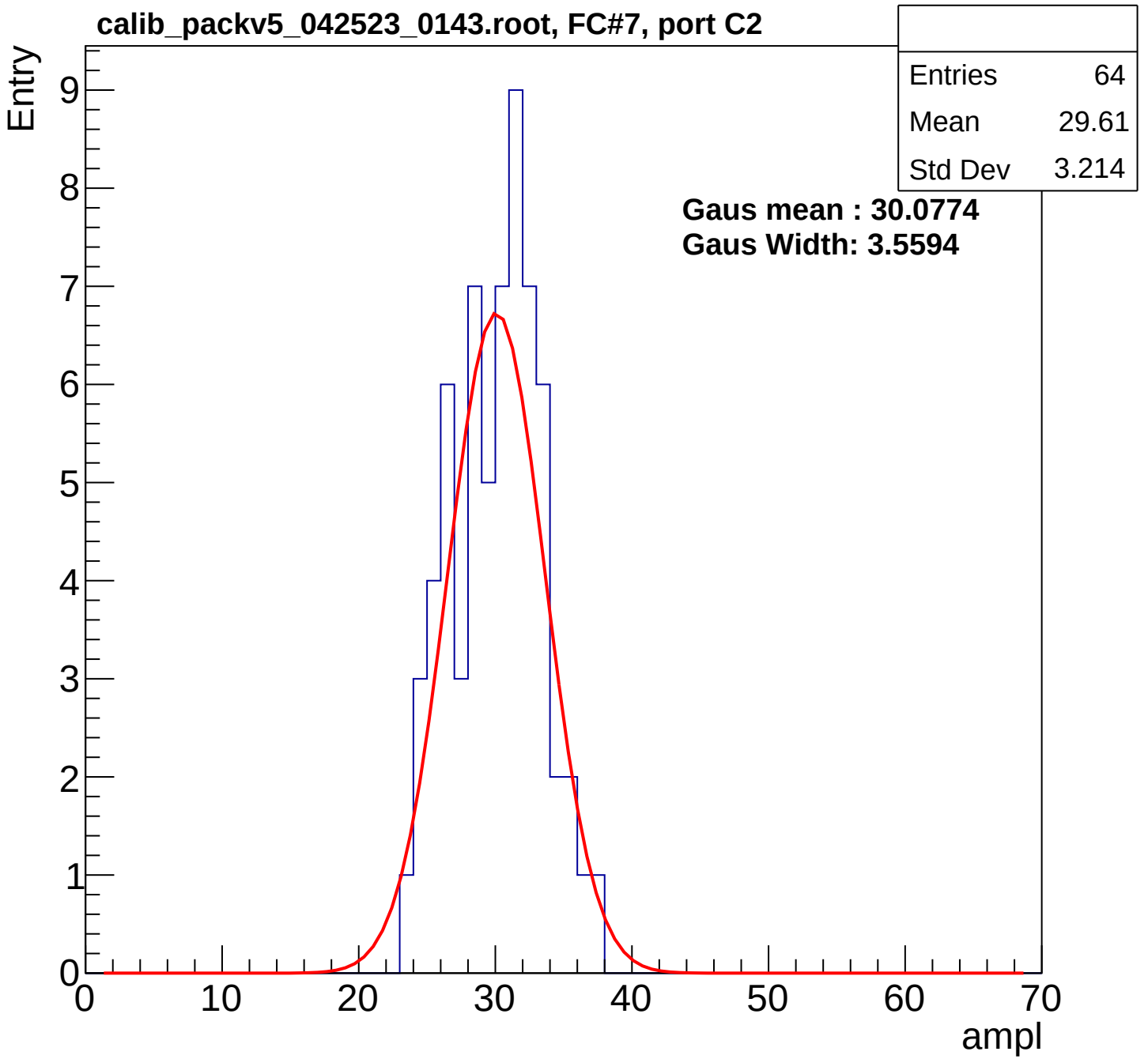

B1L103S, U18-ch85, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 77
Mean 52.25
Std Dev 3.909
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

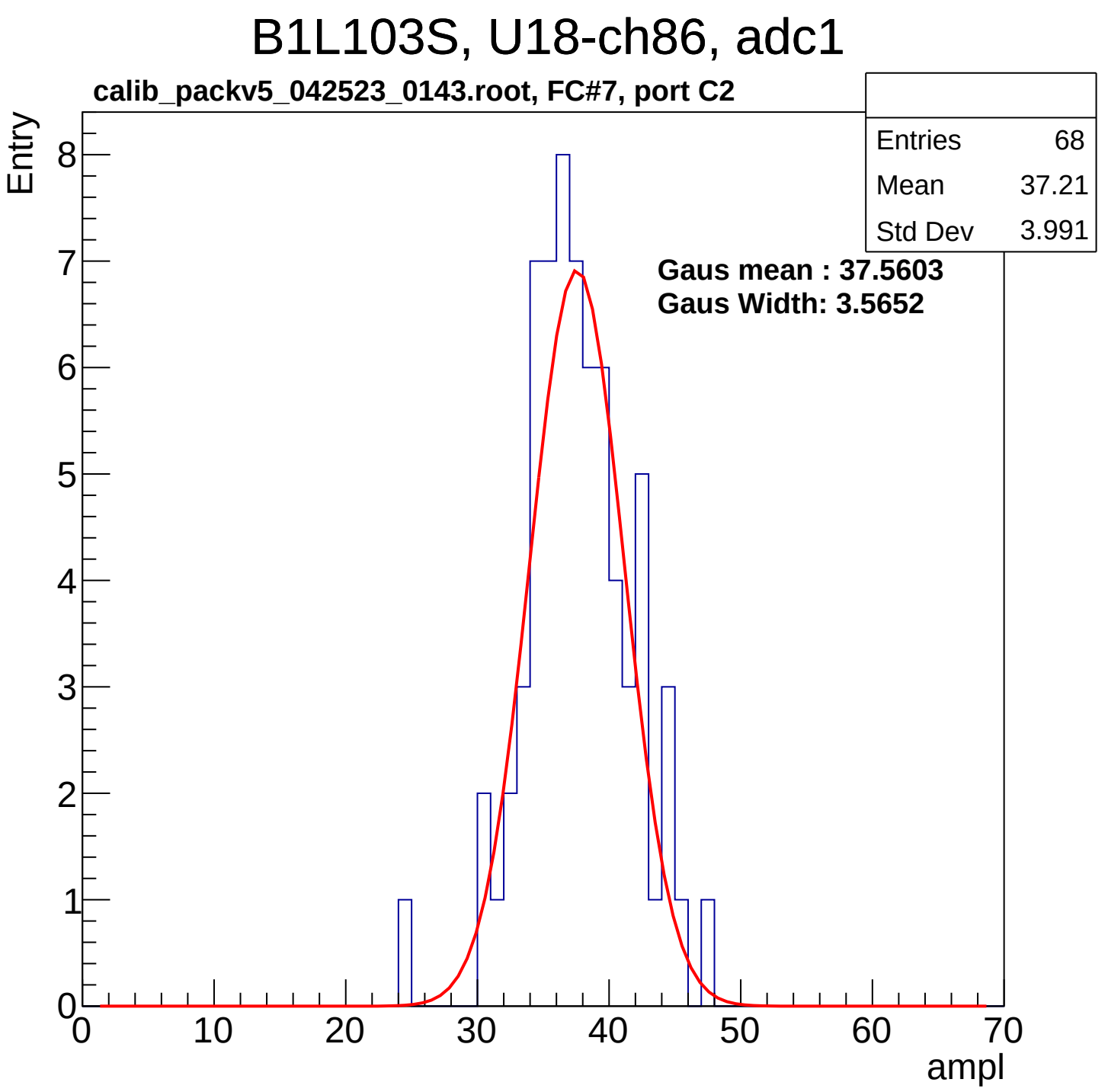

B1L103S, U18-ch85, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 36
Mean 57.36
Std Dev 3.36
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

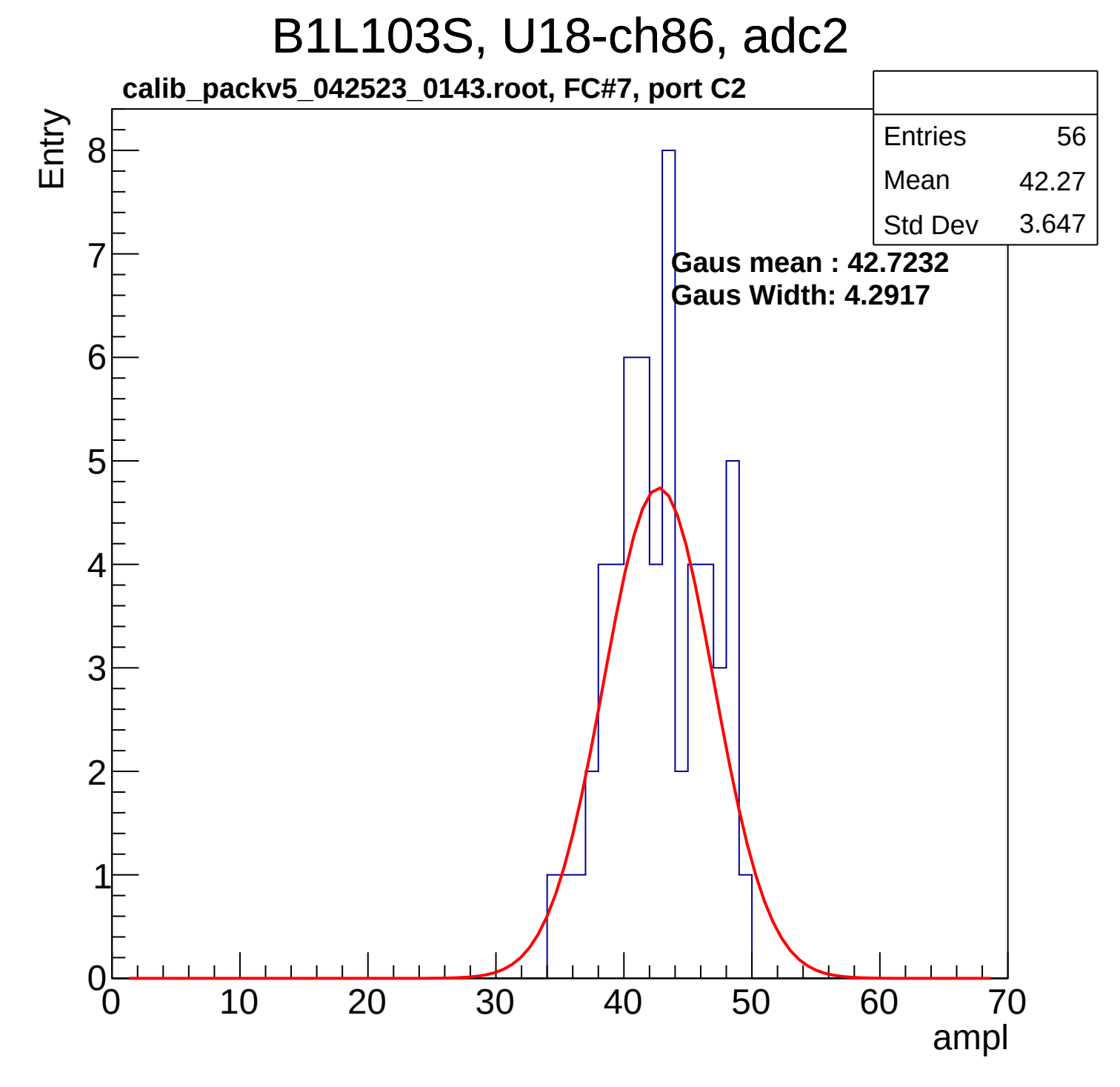

B1L103S, U18-ch85, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 38
Mean 59.05
Std Dev 9.913
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

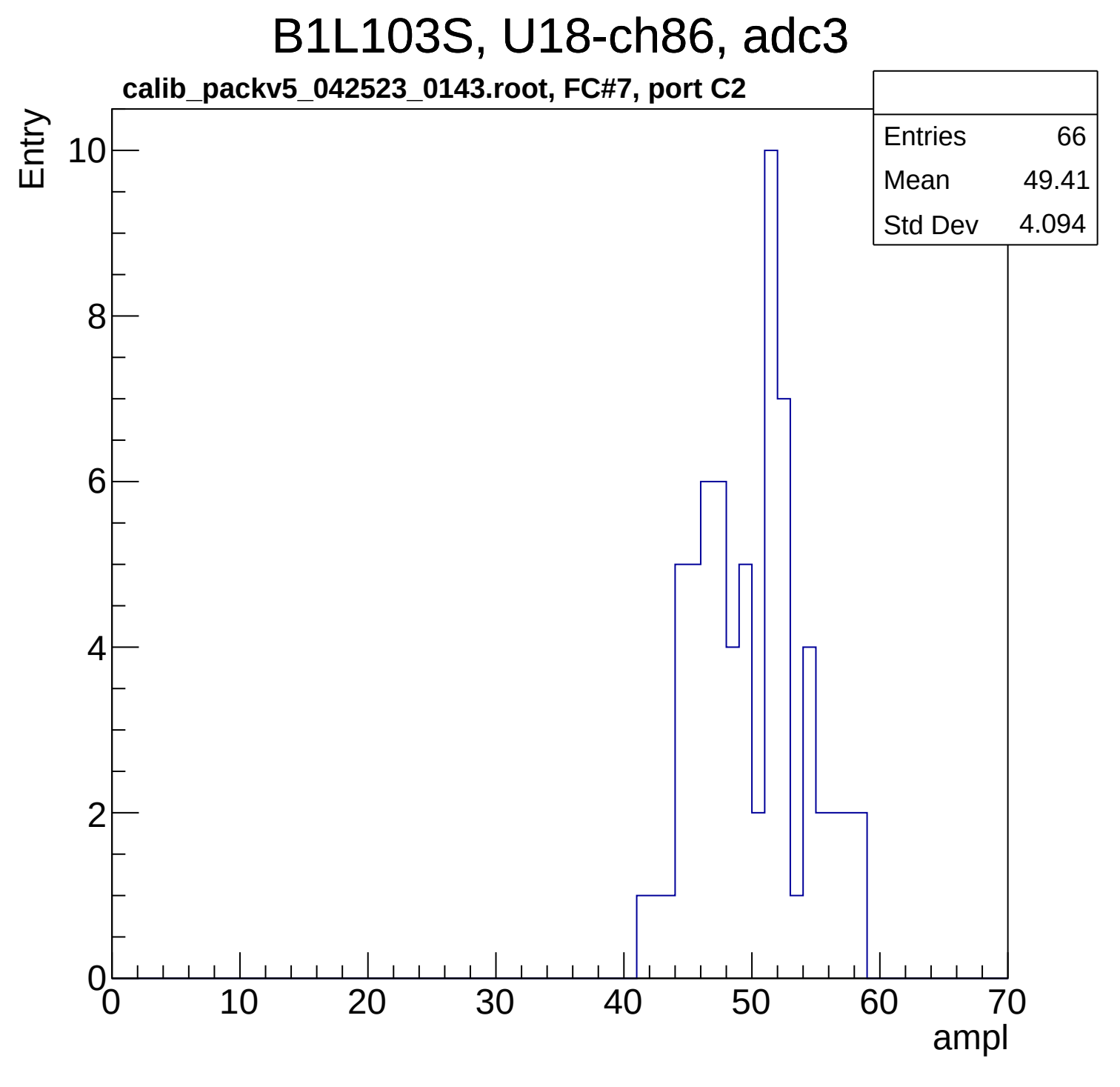

B1L103S, U18-ch85, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 60
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

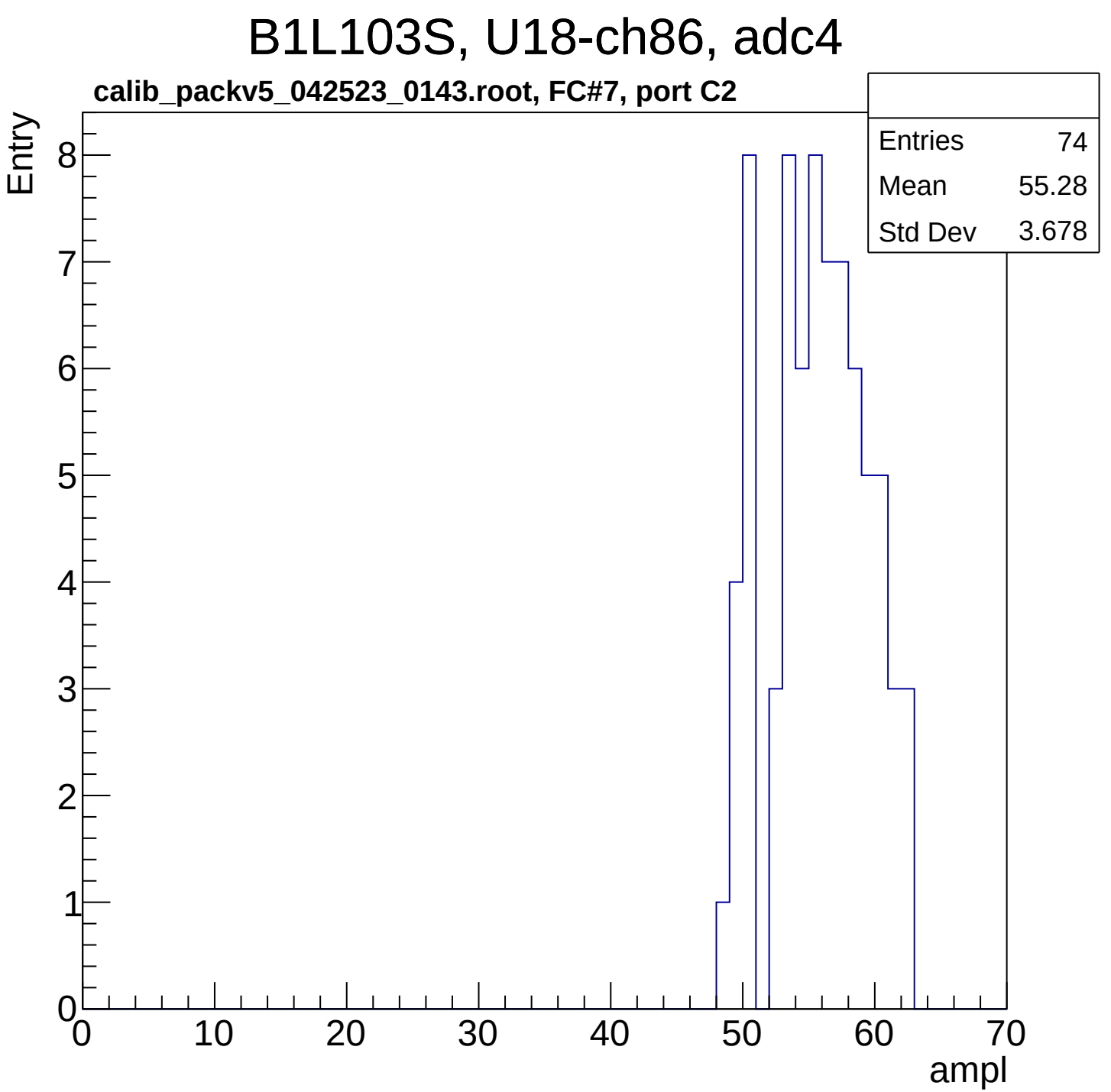

B1L103S, U18-ch85, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

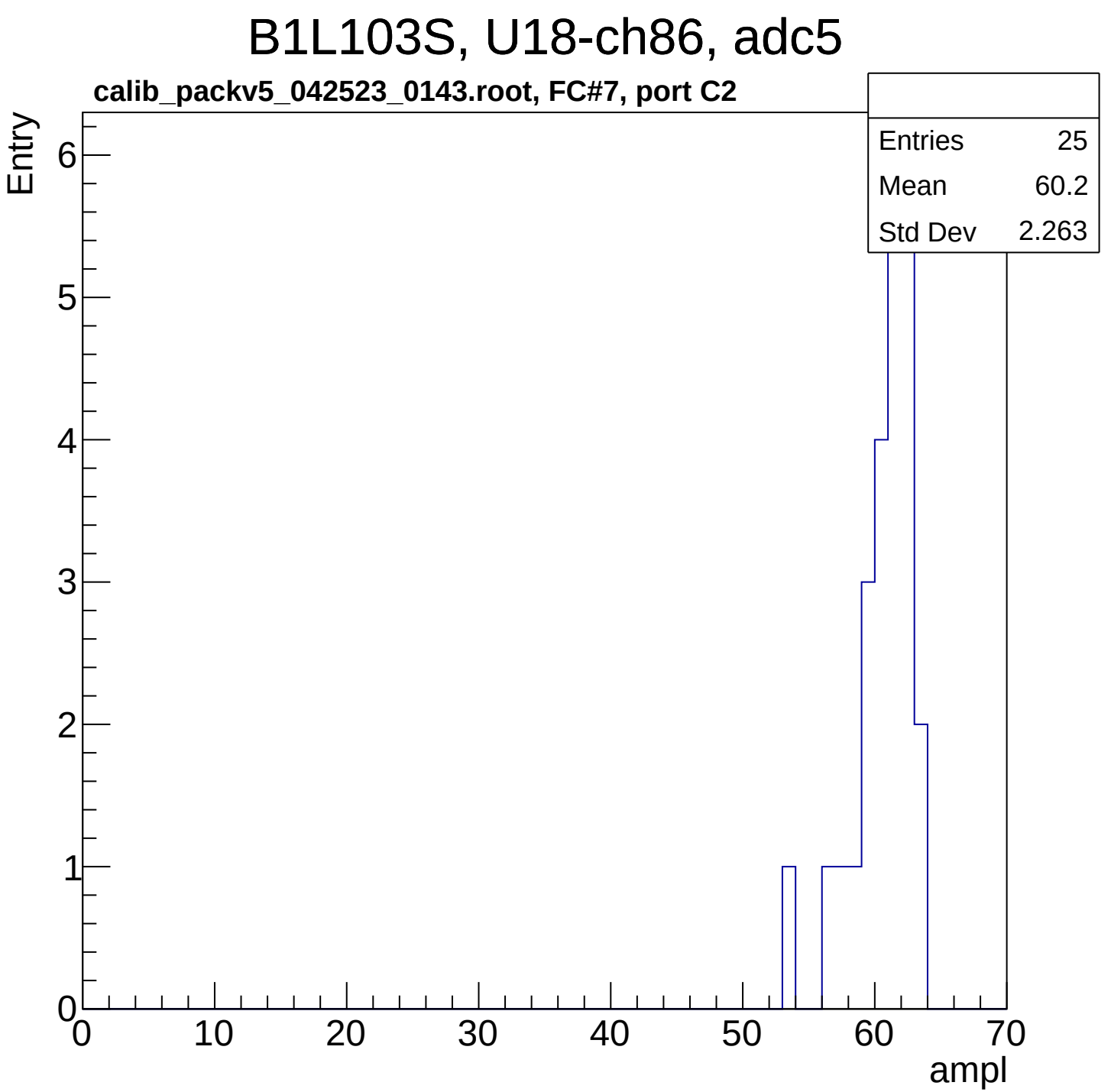

B1L103S, U18-ch86, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 29.61
Std Dev 3.214
Gaus mean : 30.0774
Gaus Width: 3.5594
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

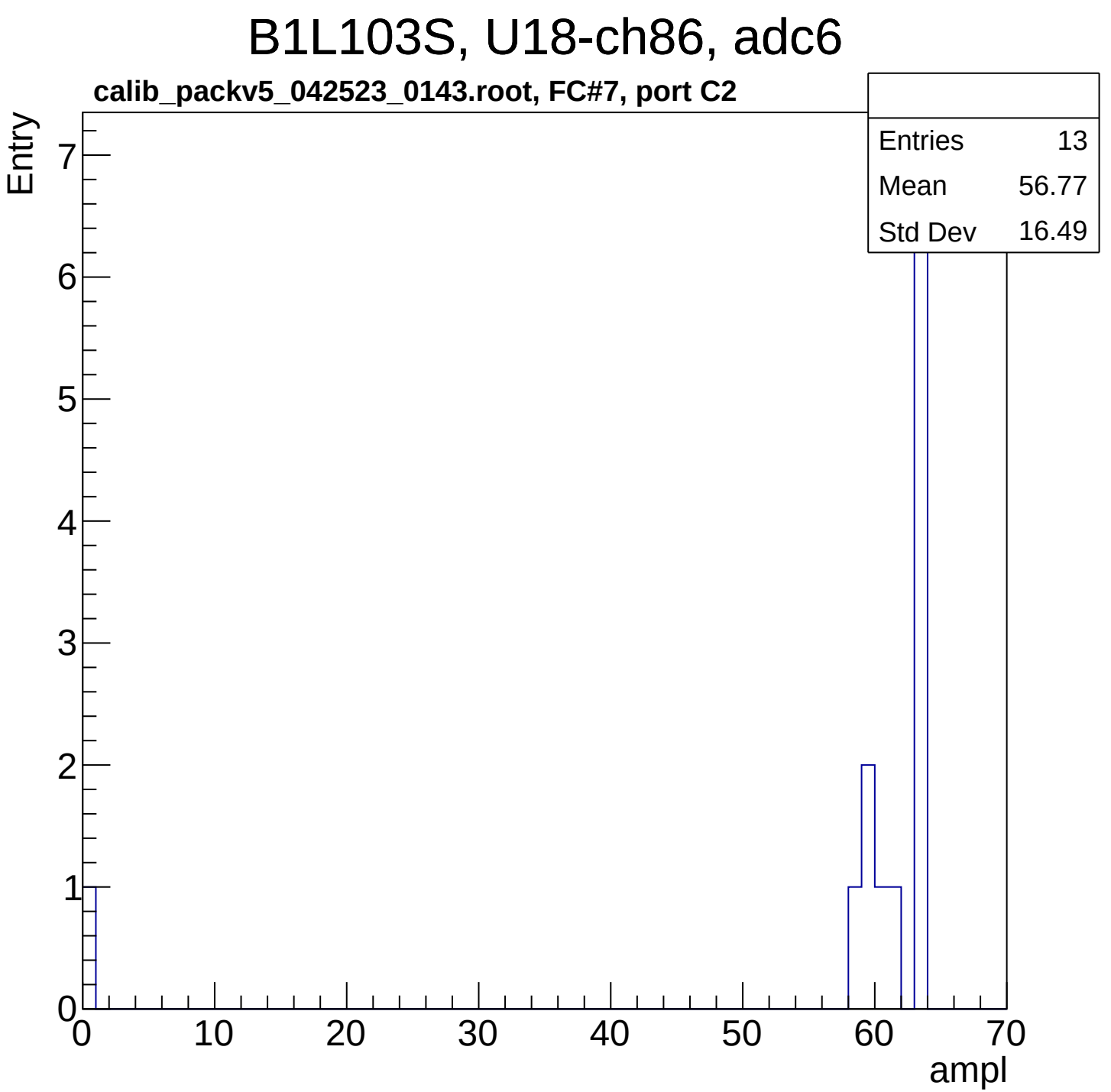

B1L103S, U18-ch86, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 37.21
Std Dev 3.991
Gaus mean : 37.5603
Gaus Width: 3.5652
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

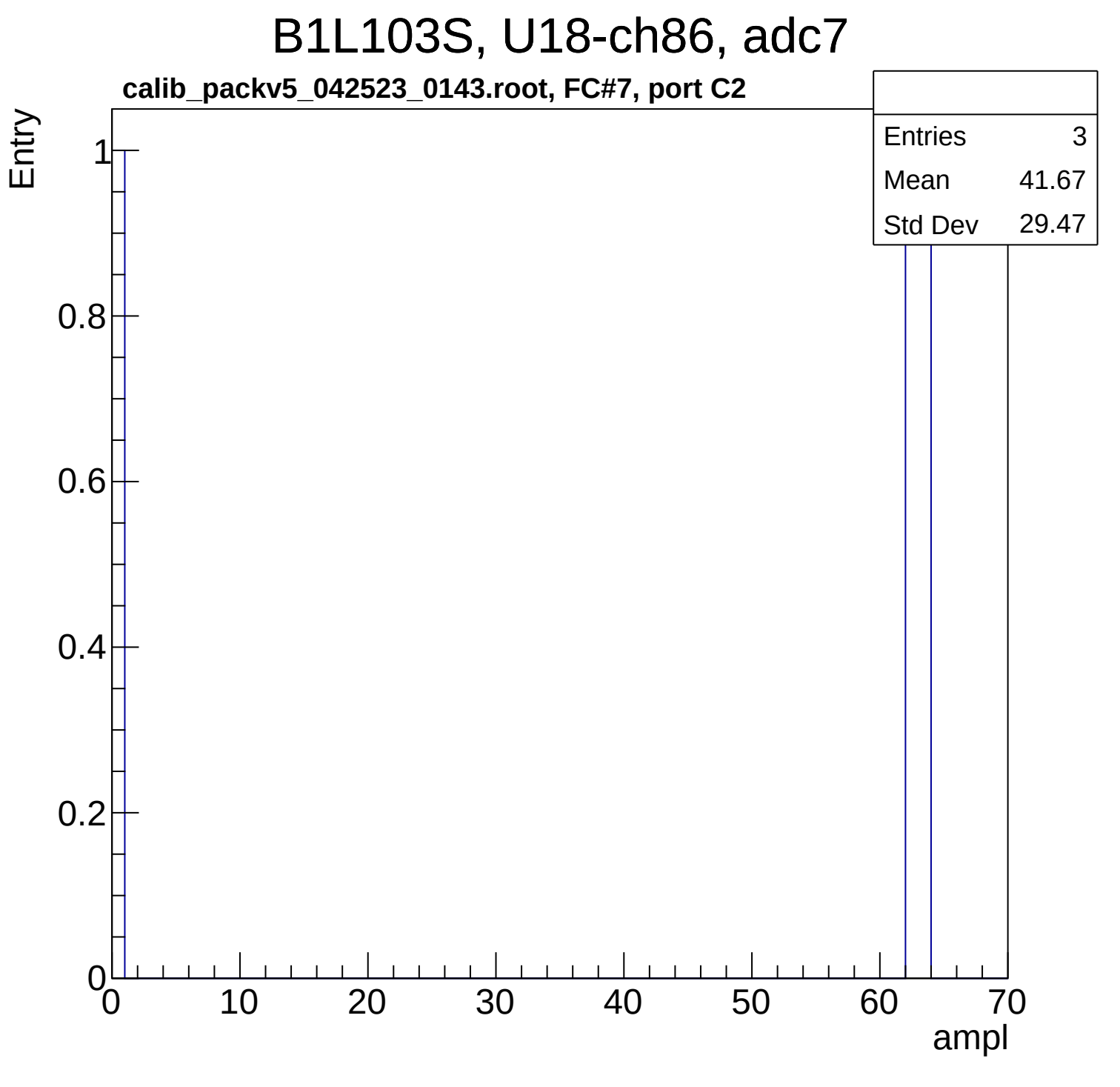

B1L103S, U18-ch86, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 42.27
Std Dev 3.647
Gaus mean : 42.7232
Gaus Width: 4.2917
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

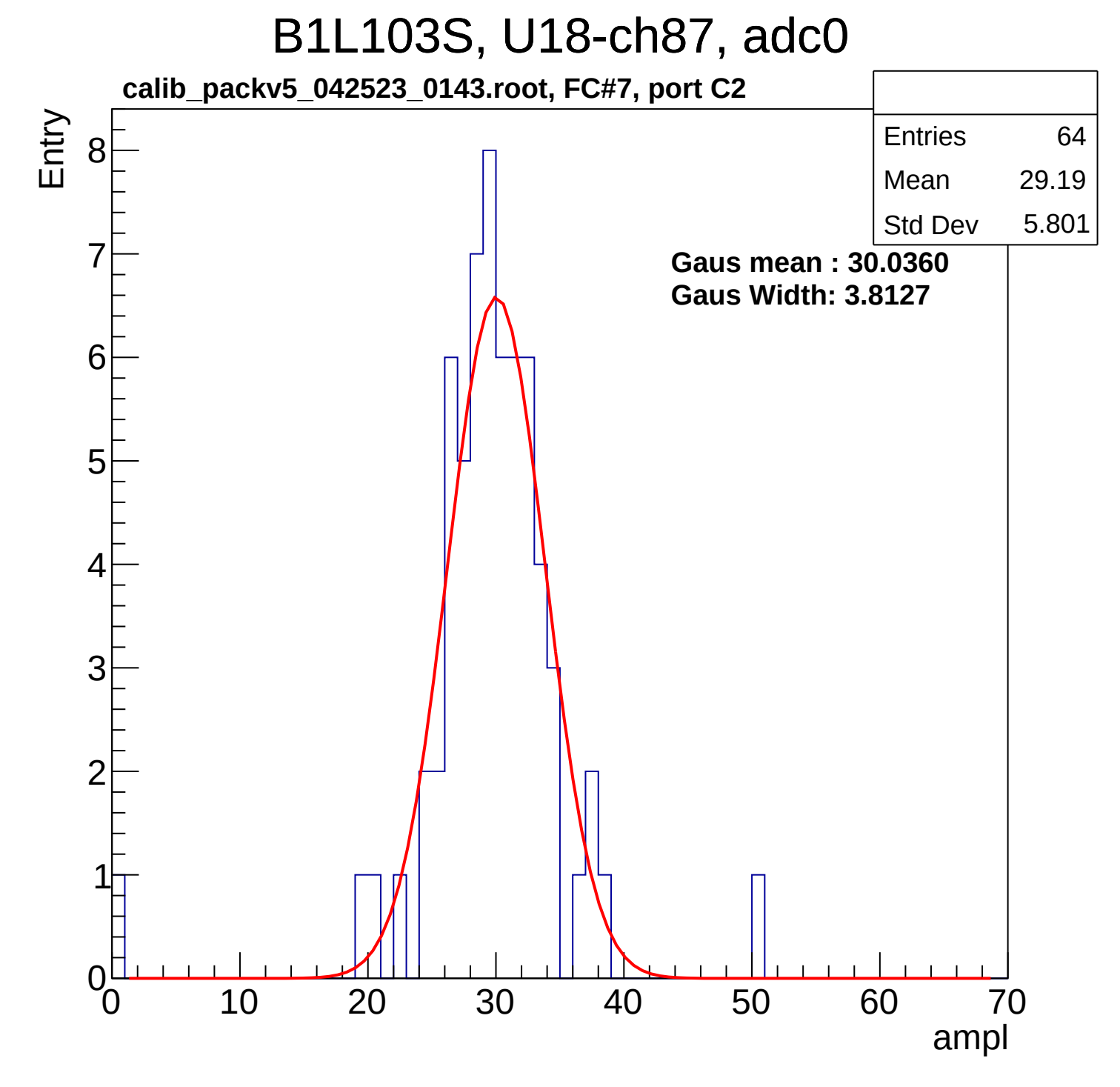

B1L103S, U18-ch86, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 49.41
Std Dev 4.094
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch86, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 74
Mean 55.28
Std Dev 3.678
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch86, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 25
Mean 60.2
Std Dev 2.263
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch86, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 13
Mean 56.77
Std Dev 16.49
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch86, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 41.67
Std Dev 29.47
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch87, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 29.19
Std Dev 5.801
Gaus mean : 30.0360
Gaus Width: 3.8127
Entry
ampl
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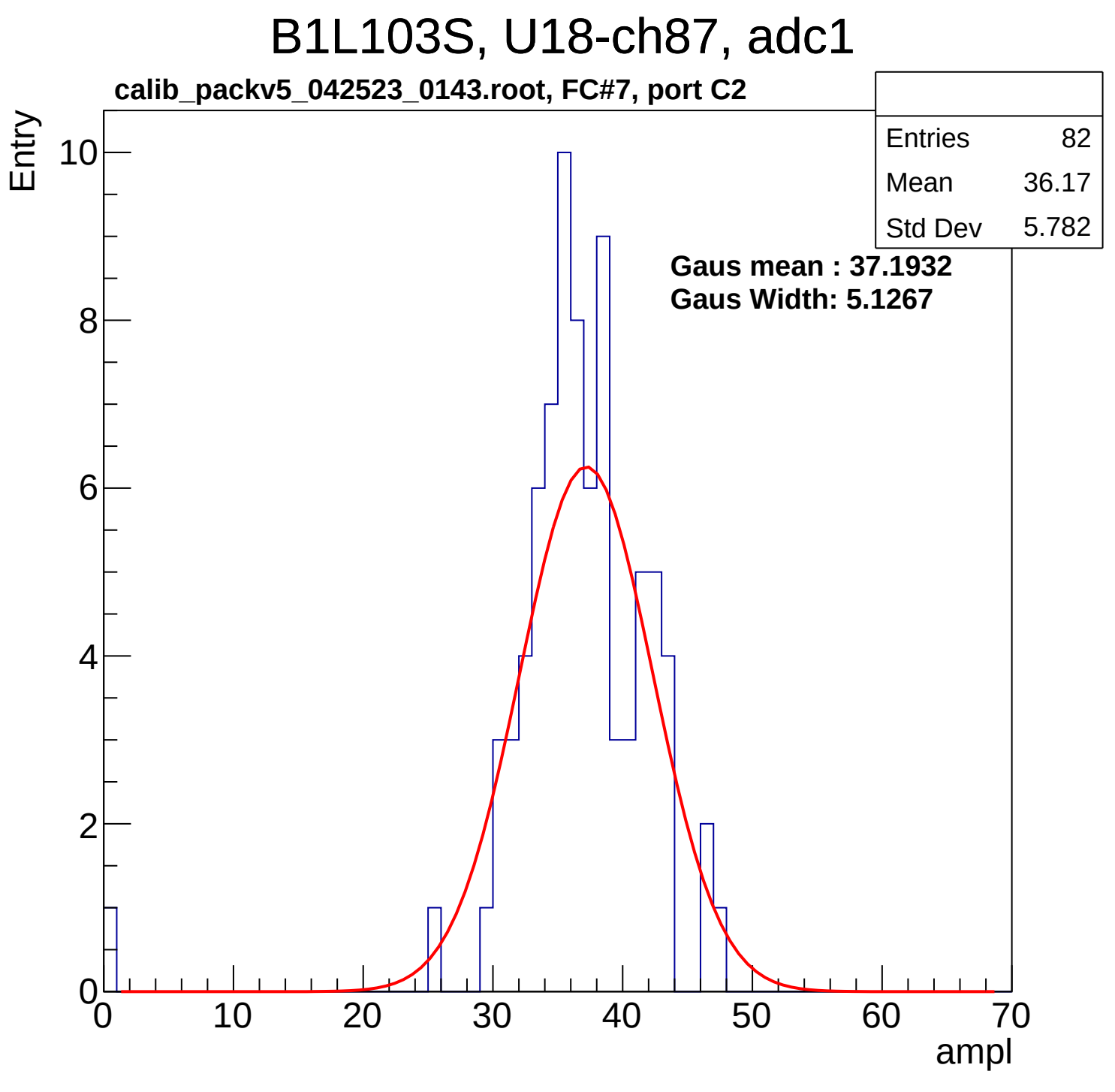
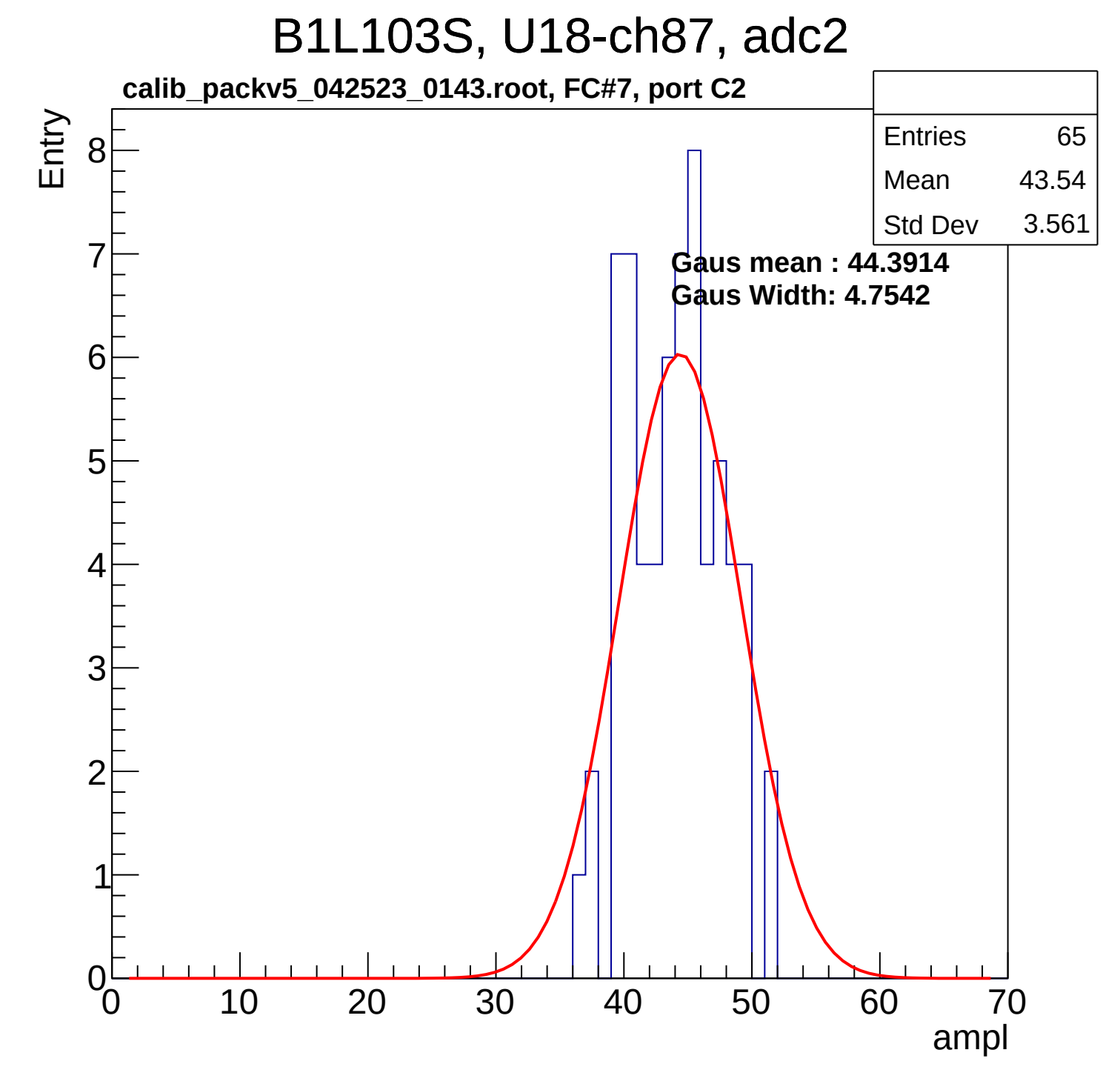
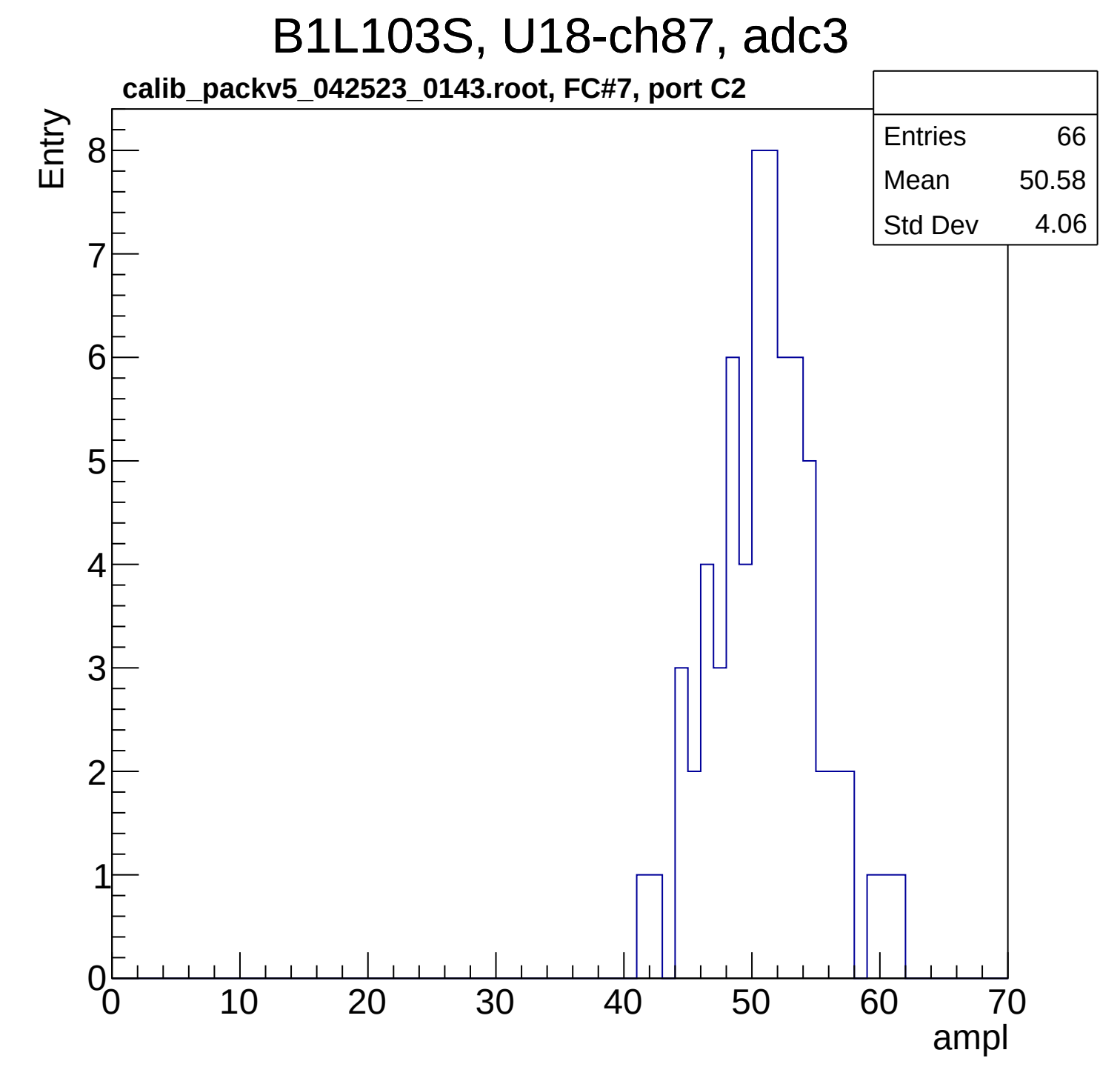
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch87, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 82
Mean 36.17
Std Dev 5.782
Gaus mean : 37.1932
Gaus Width: 5.1267
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch87, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 43.54
Std Dev 3.561
Gaus mean : 44.3914
Gaus Width: 4.7542
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch87, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 50.58
Std Dev 4.06
Entry
ampl
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1
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3
4
5
6
7
8
0
10
20
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40
50
60
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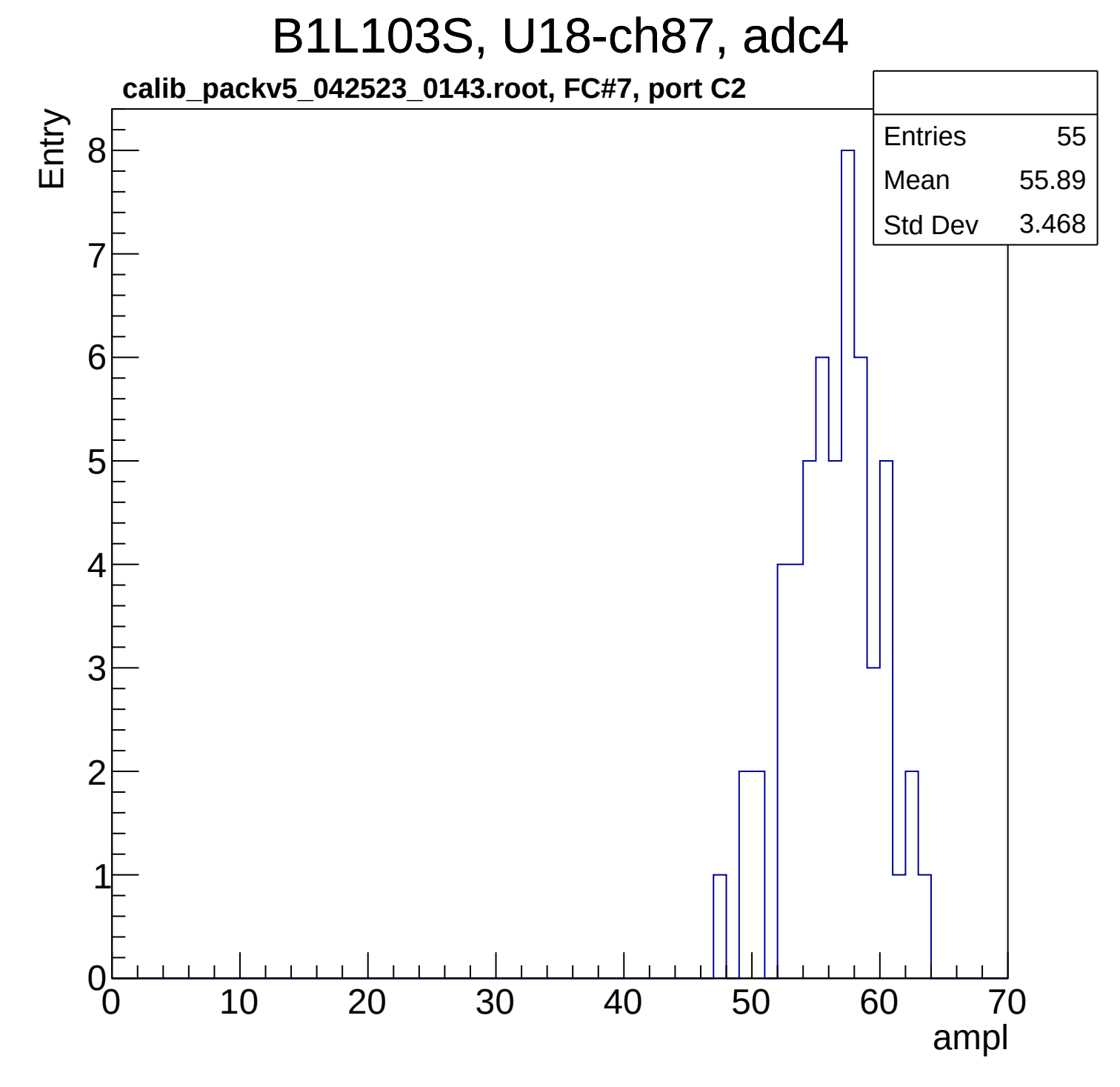
B1L103S, U18-ch87, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 55.89
Std Dev 3.468
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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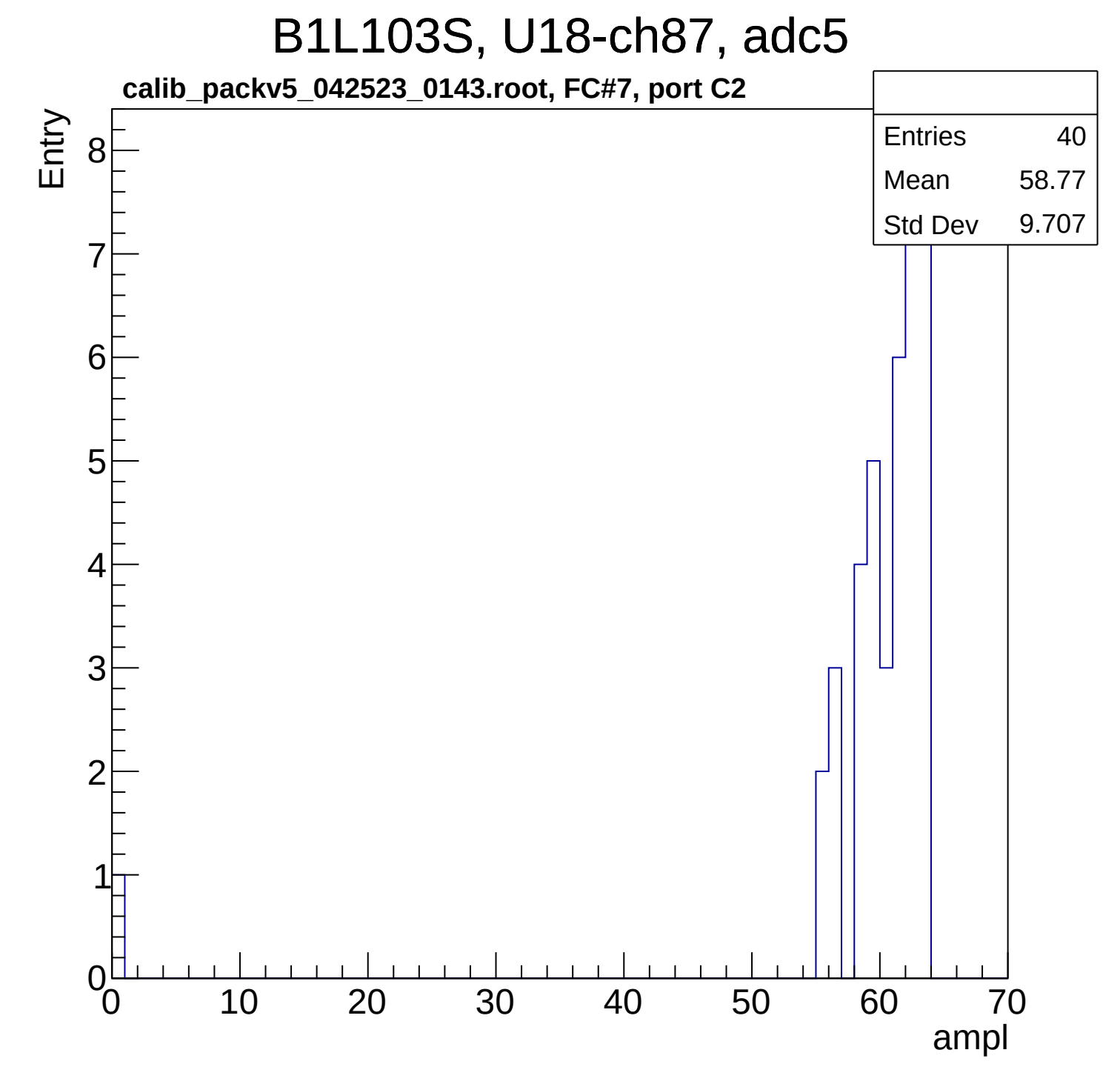
B1L103S, U18-ch87, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 40
Mean 58.77
Std Dev 9.707
Entry
ampl
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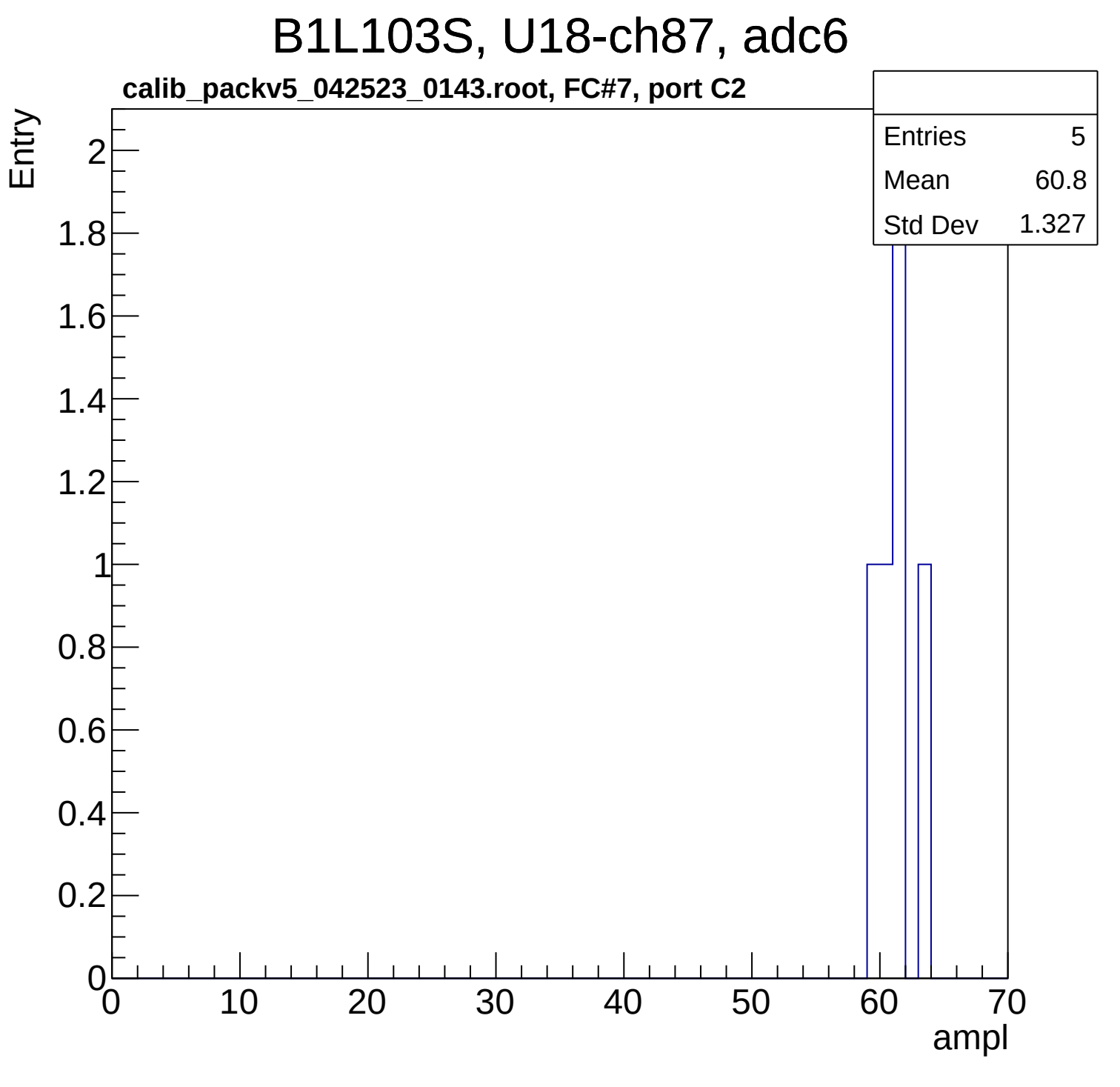
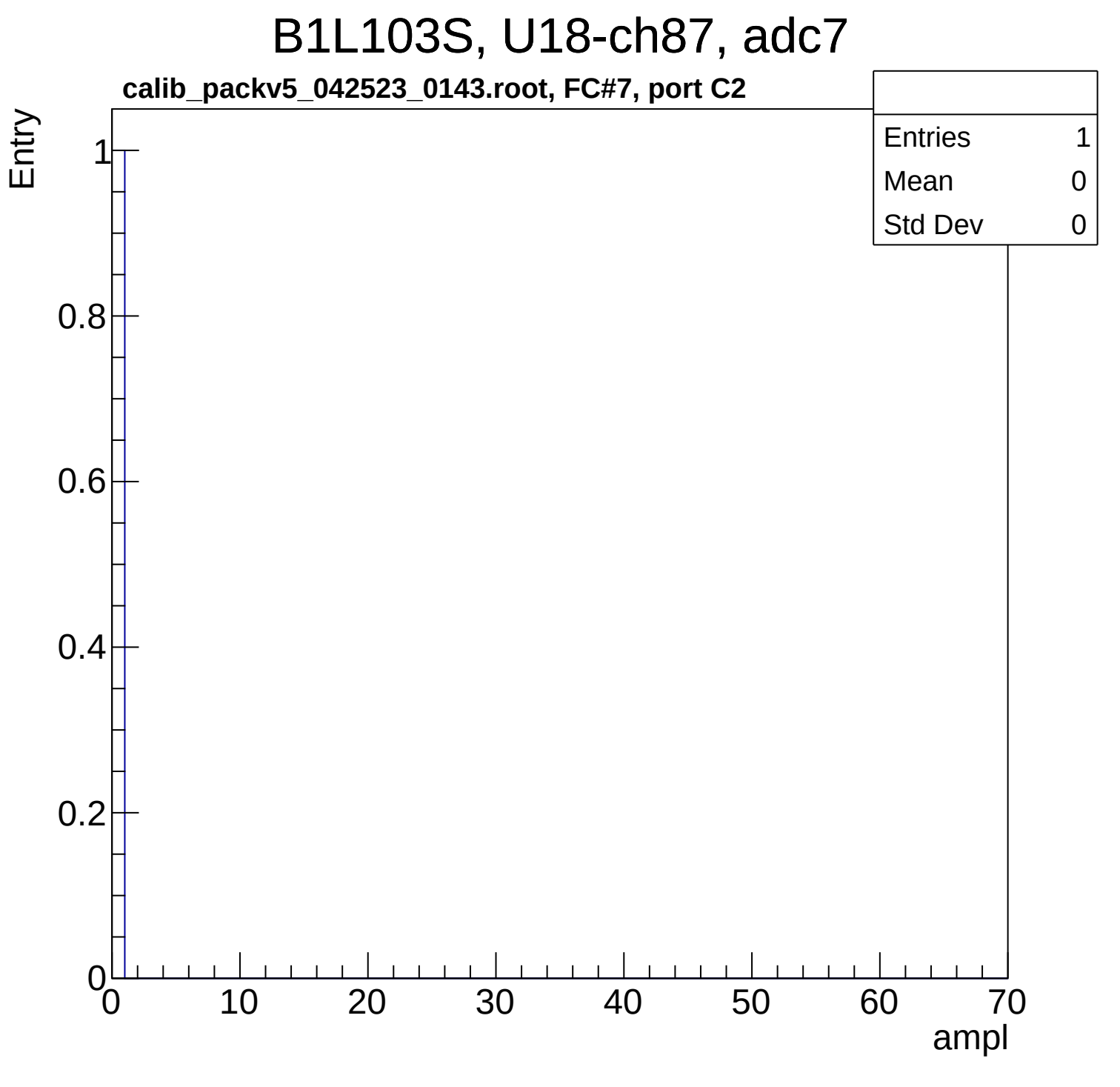
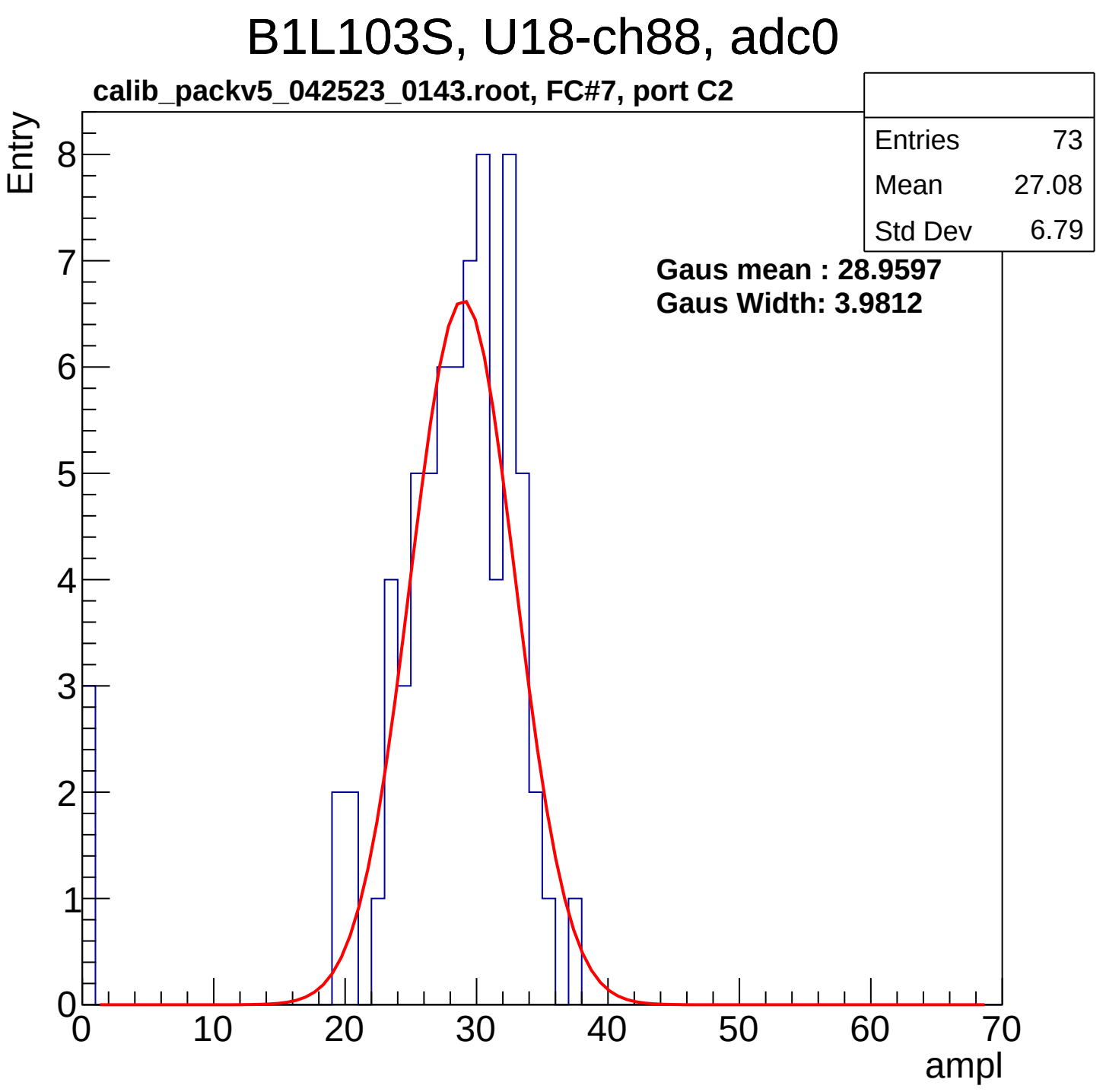
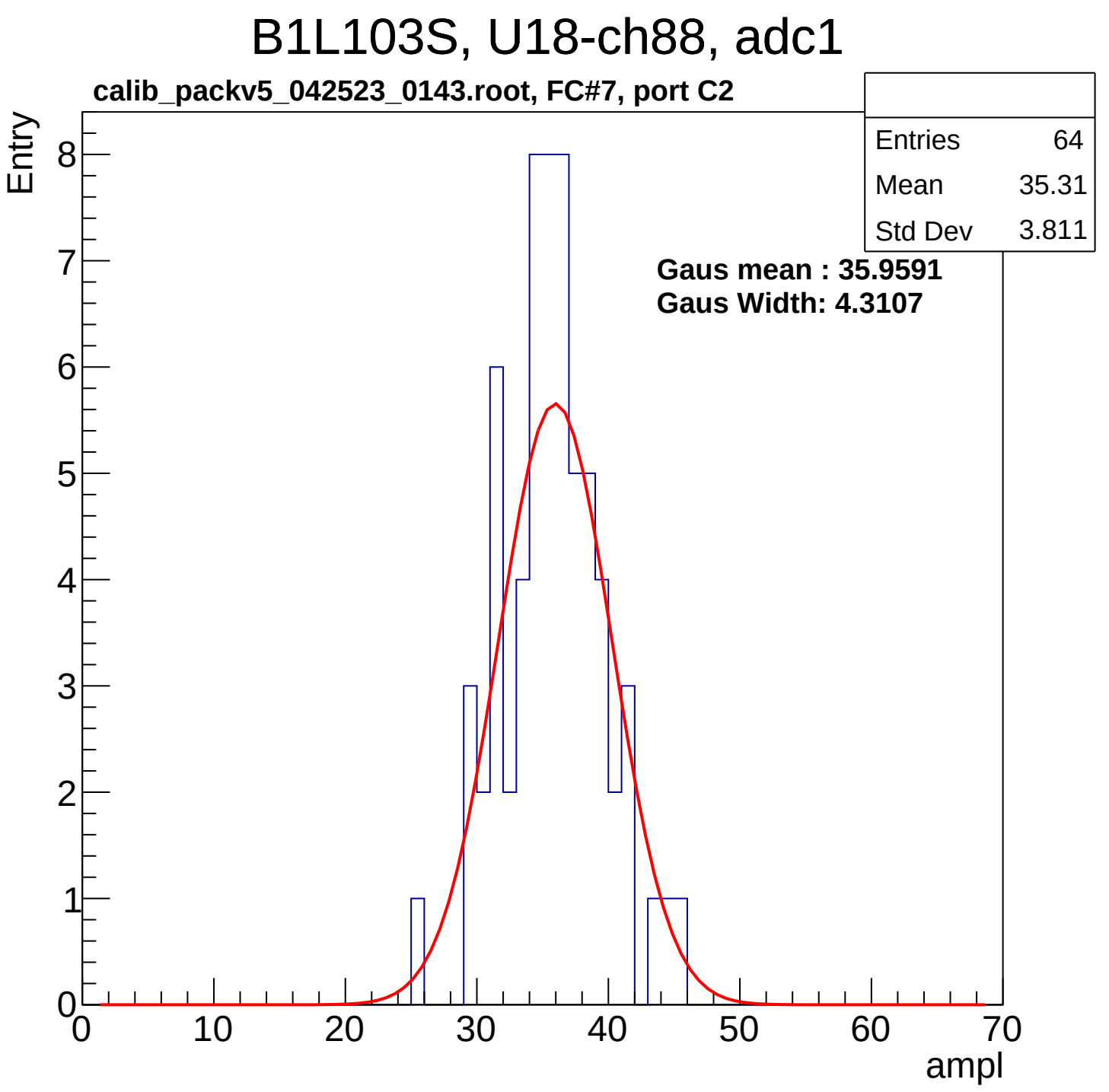
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch87, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 5
Mean 60.8
Std Dev 1.327
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U18-ch87, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch88, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 73
Mean 27.08
Std Dev 6.79
Gaus mean : 28.9597
Gaus Width: 3.9812
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch88, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 35.31
Std Dev 3.811
Gaus mean : 35.9591
Gaus Width: 4.3107
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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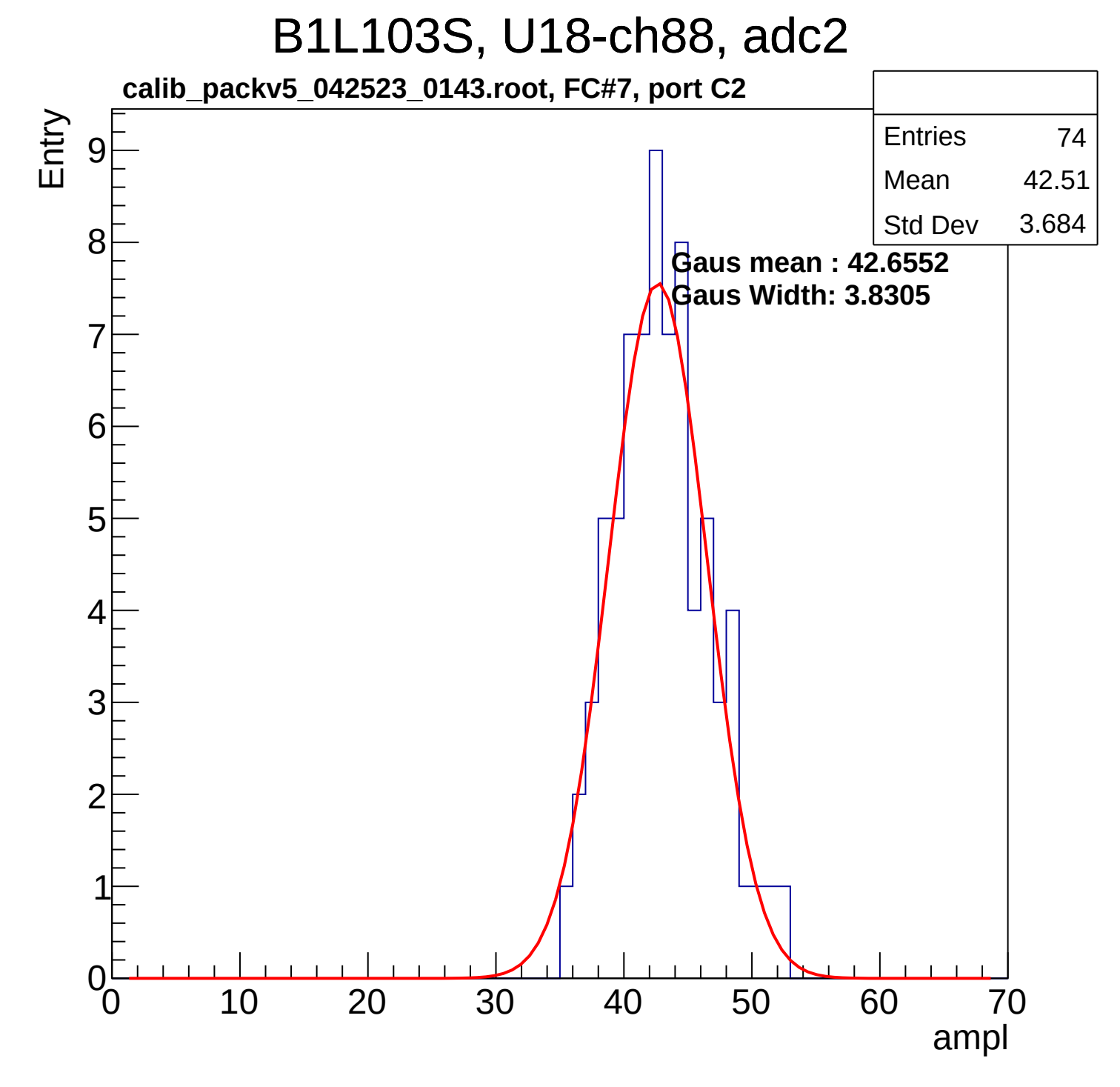
B1L103S, U18-ch88, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 74
Mean 42.51
Std Dev 3.684
Gaus mean : 42.6552
Gaus Width: 3.8305
Entry
ampl
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2
3
4
5
6
7
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0
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40
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60
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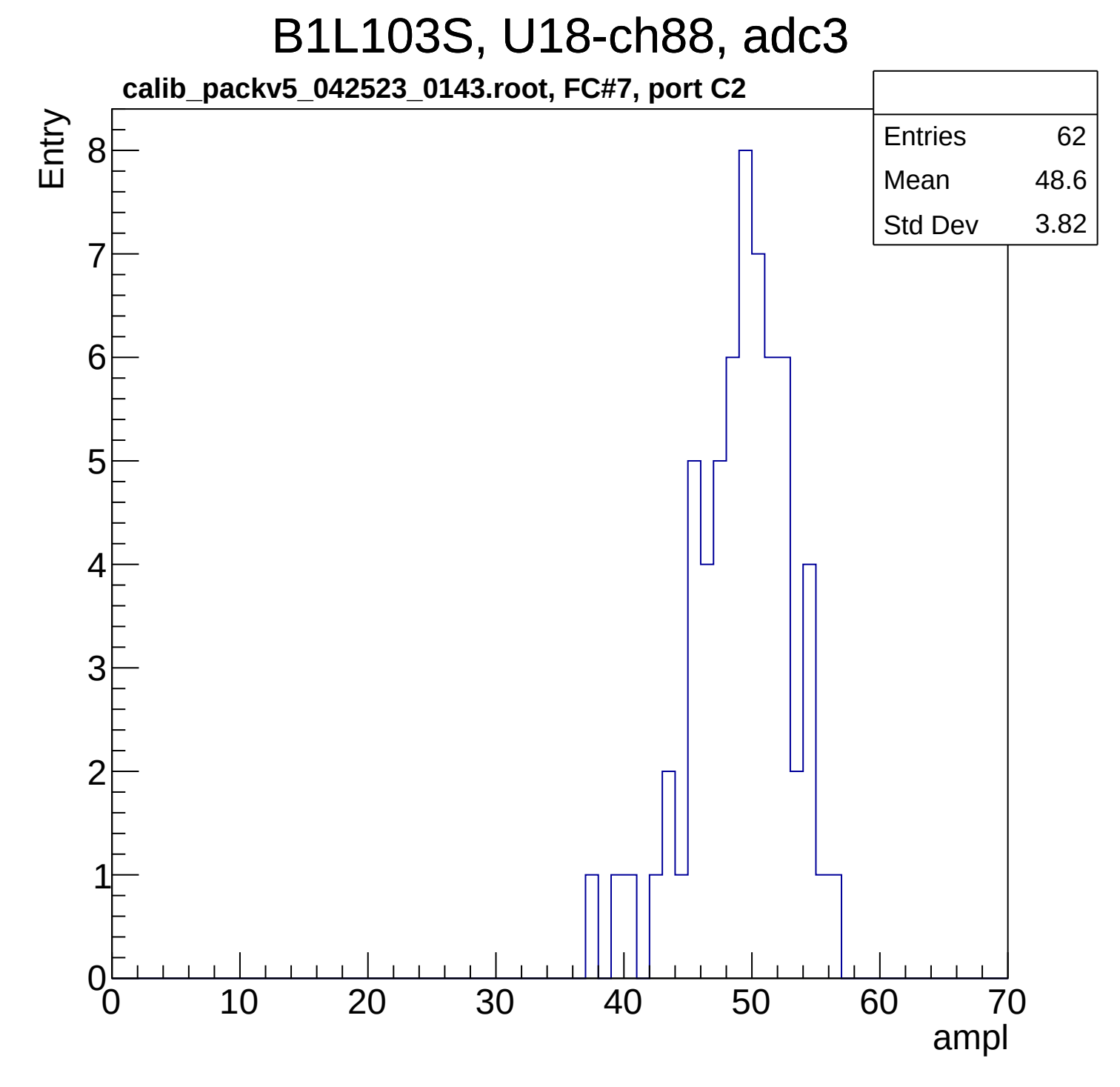
B1L103S, U18-ch88, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 62
Mean 48.6
Std Dev 3.82
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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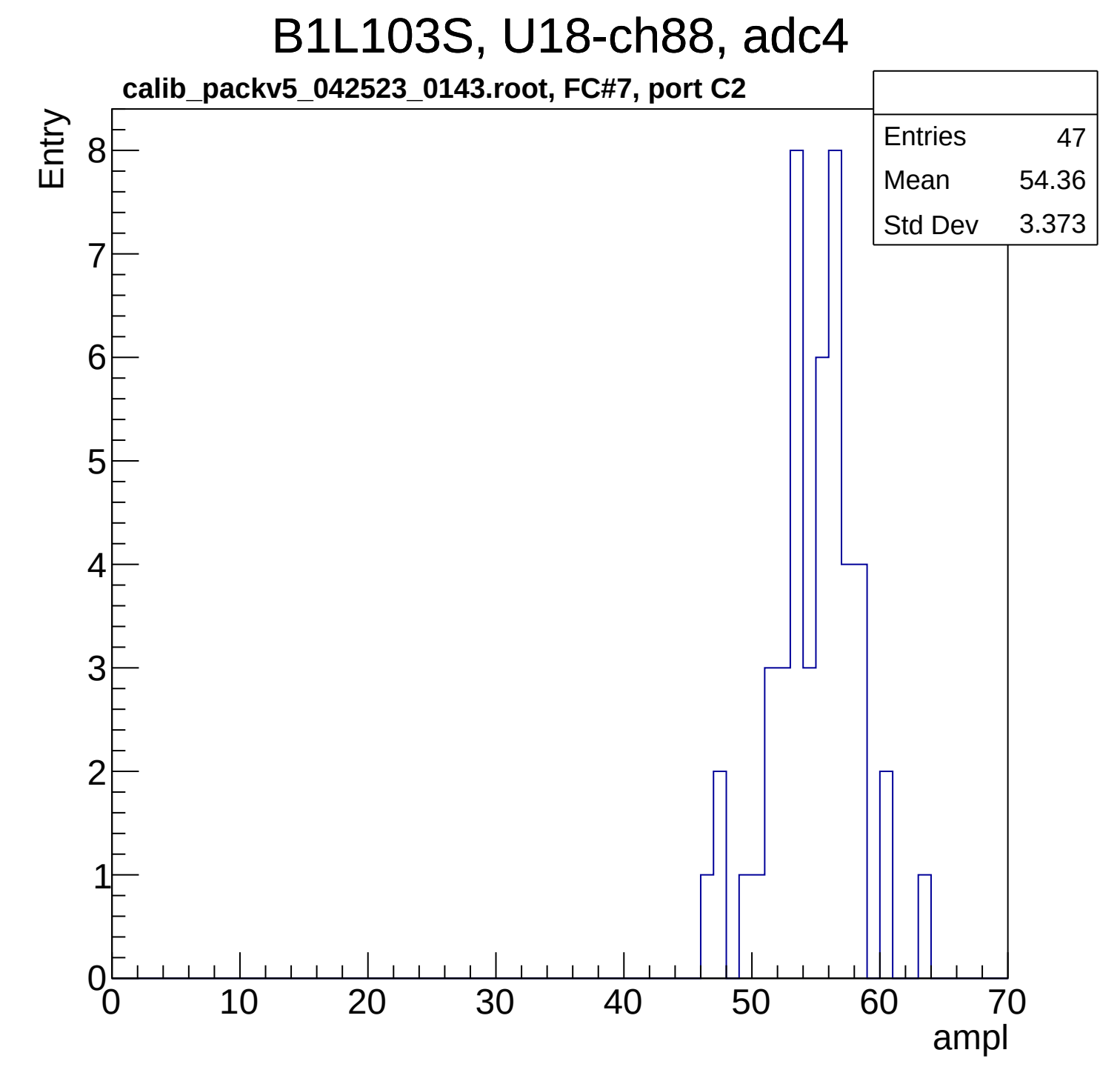
B1L103S, U18-ch88, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 47
Mean 54.36
Std Dev 3.373
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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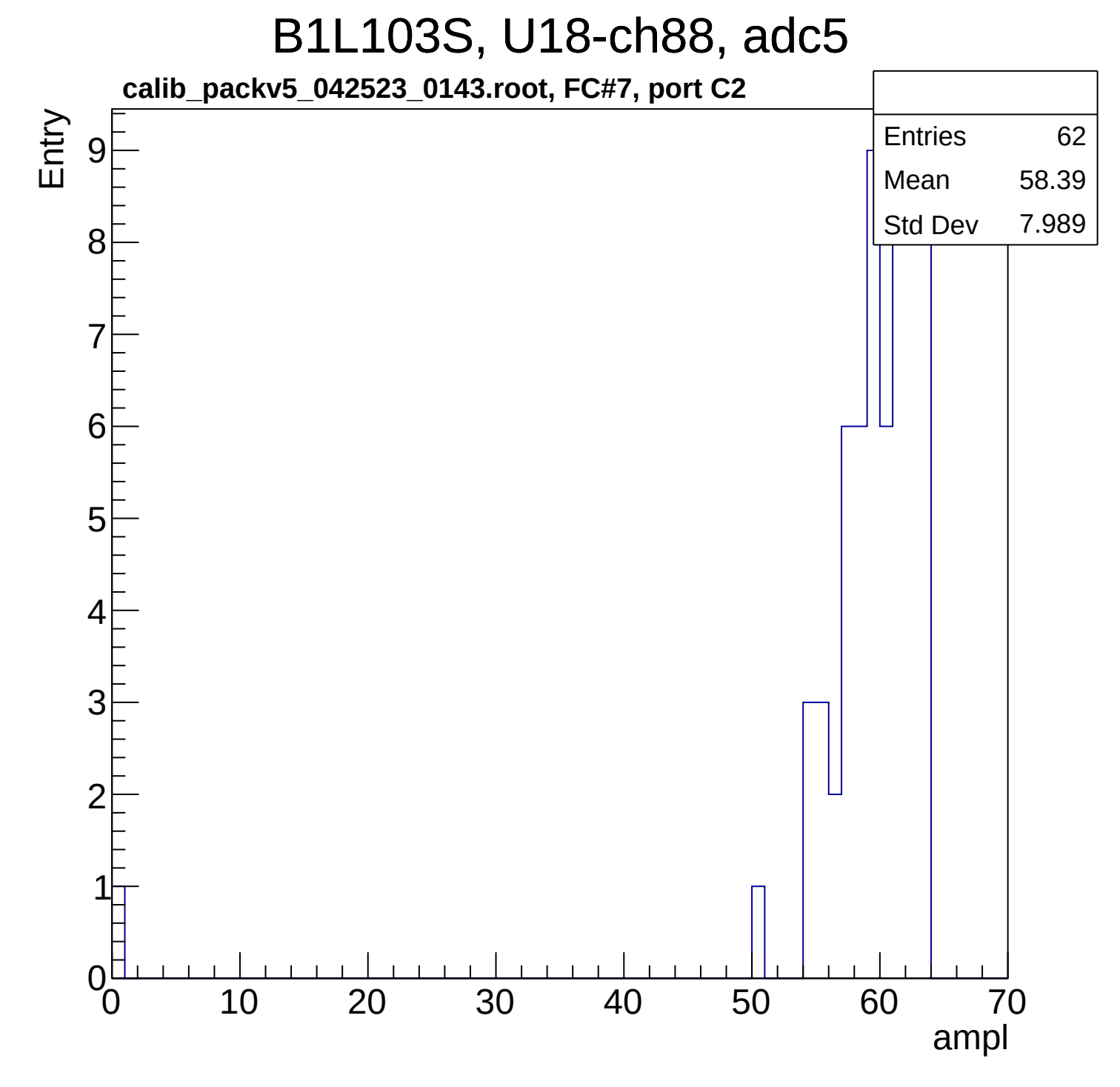
B1L103S, U18-ch88, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 62
Mean 58.39
Std Dev 7.989
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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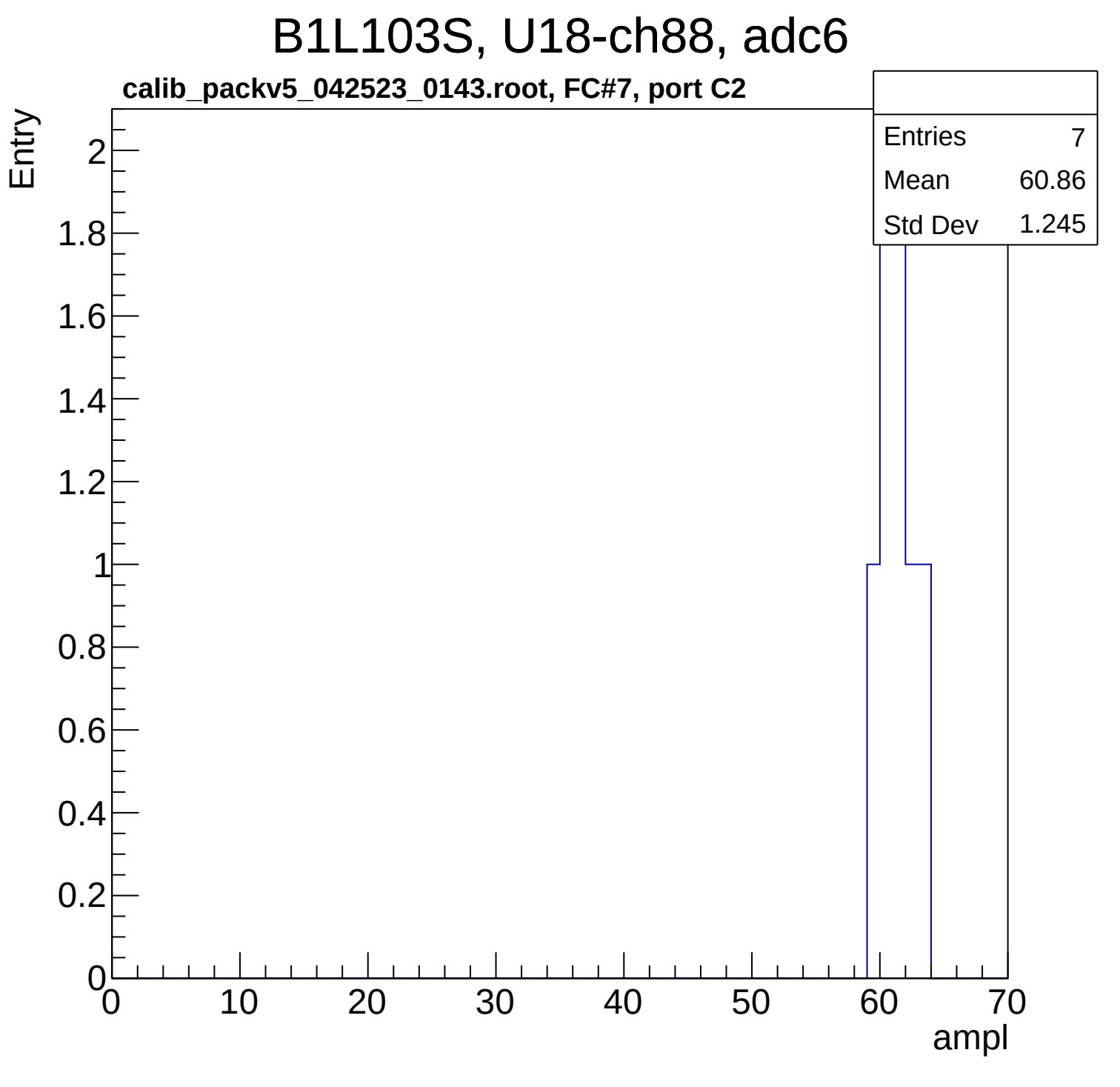
B1L103S, U18-ch88, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 7
Mean 60.86
Std Dev 1.245
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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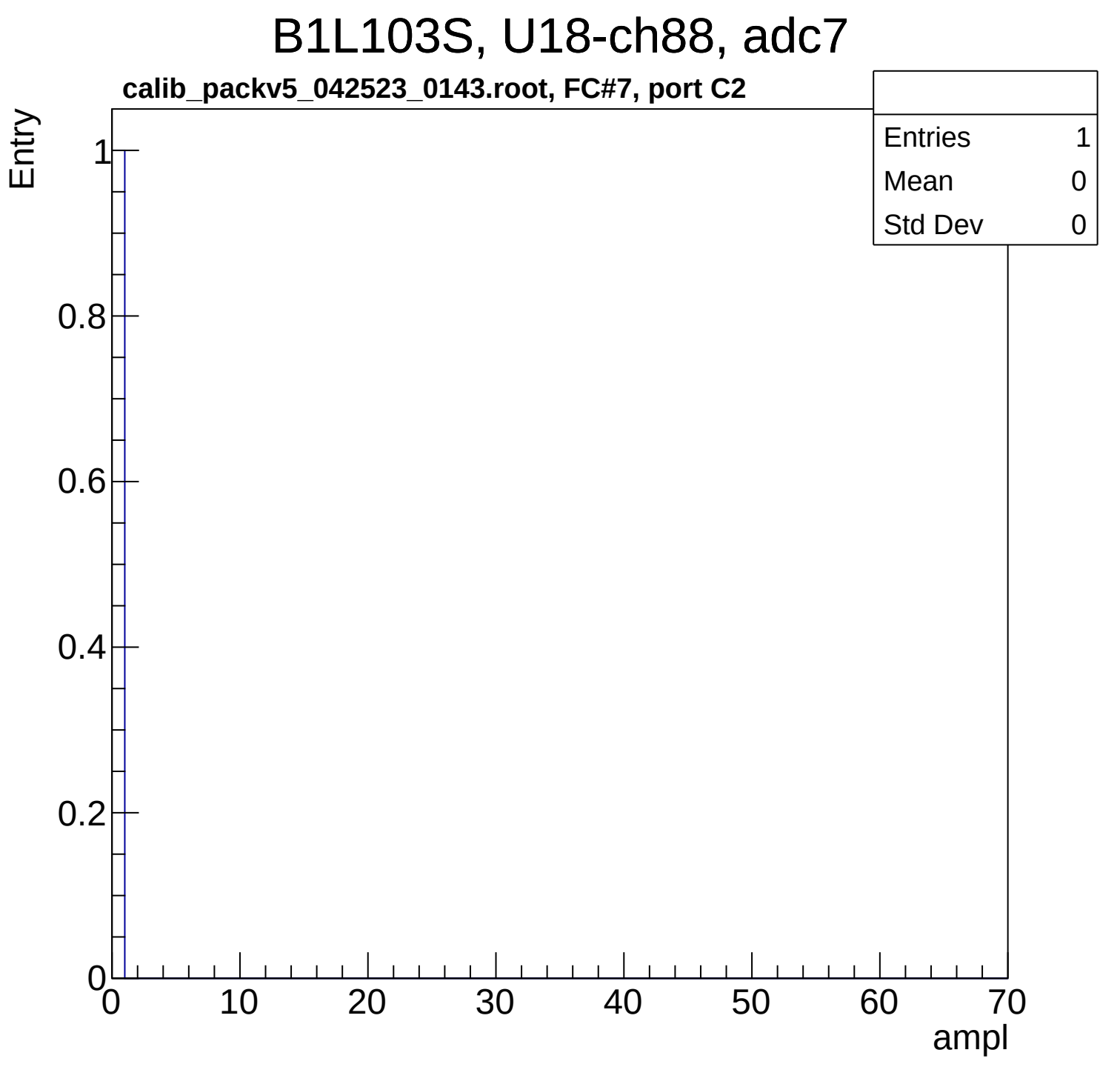
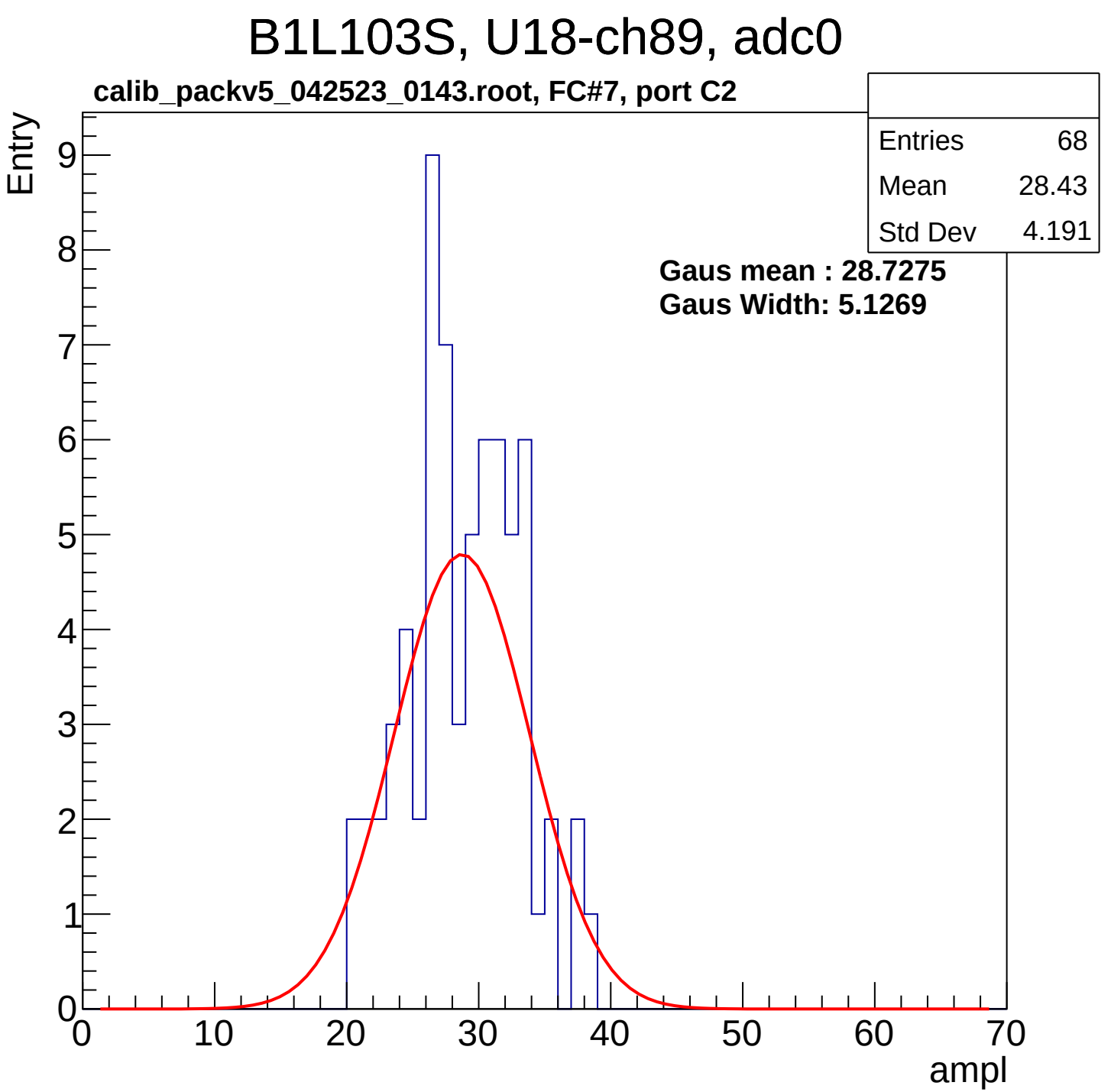

B1L103S, U18-ch88, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch89, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 28.43
Std Dev 4.191
Gaus mean : 28.7275
Gaus Width: 5.1269
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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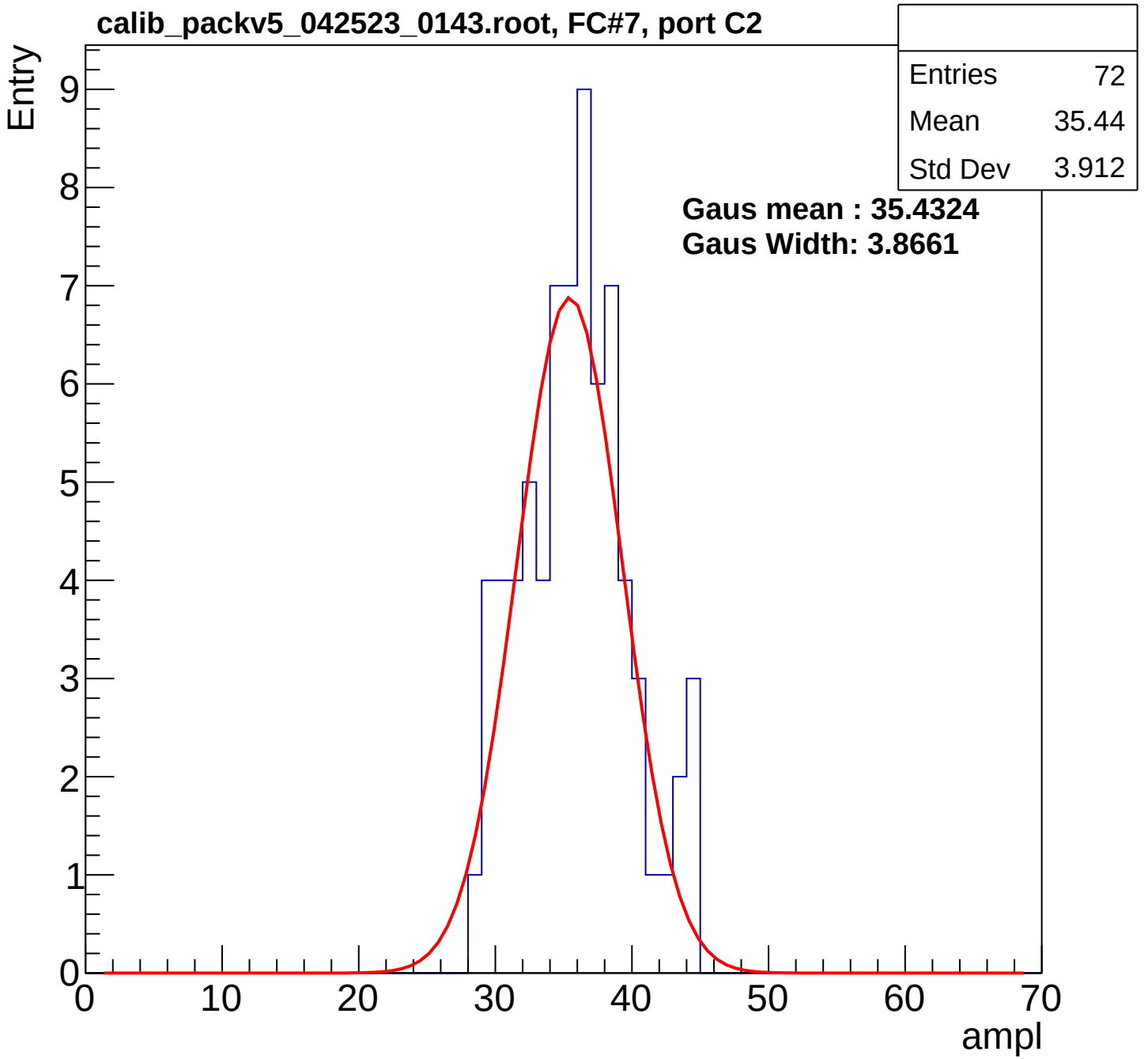
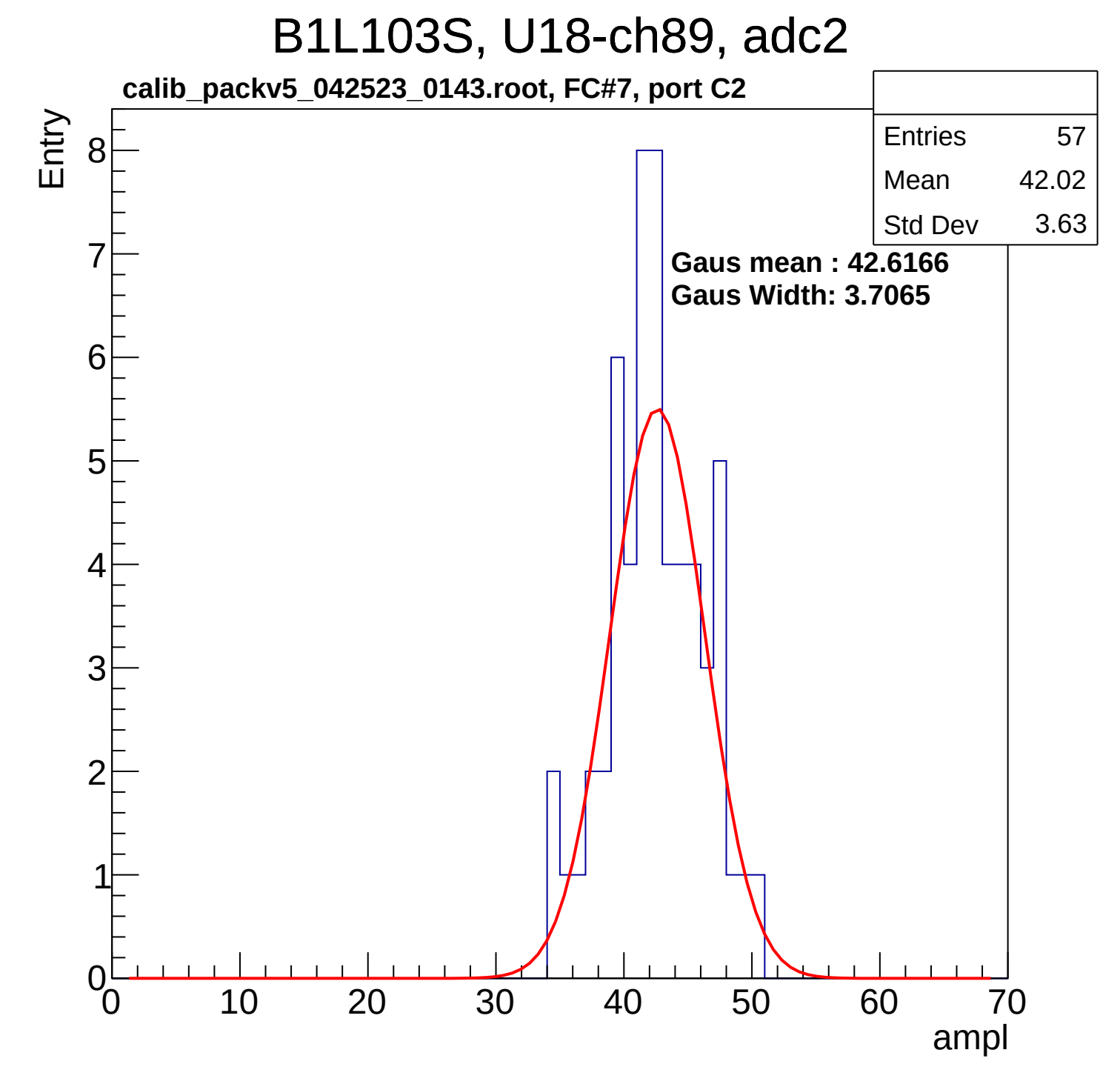

B1L103S, U18-ch89, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 72
Mean 35.44
Std Dev 3.912
Gaus mean : 35.4324
Gaus Width: 3.8661
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch89, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 42.02
Std Dev 3.63
Gaus mean : 42.6166
Gaus Width: 3.7065
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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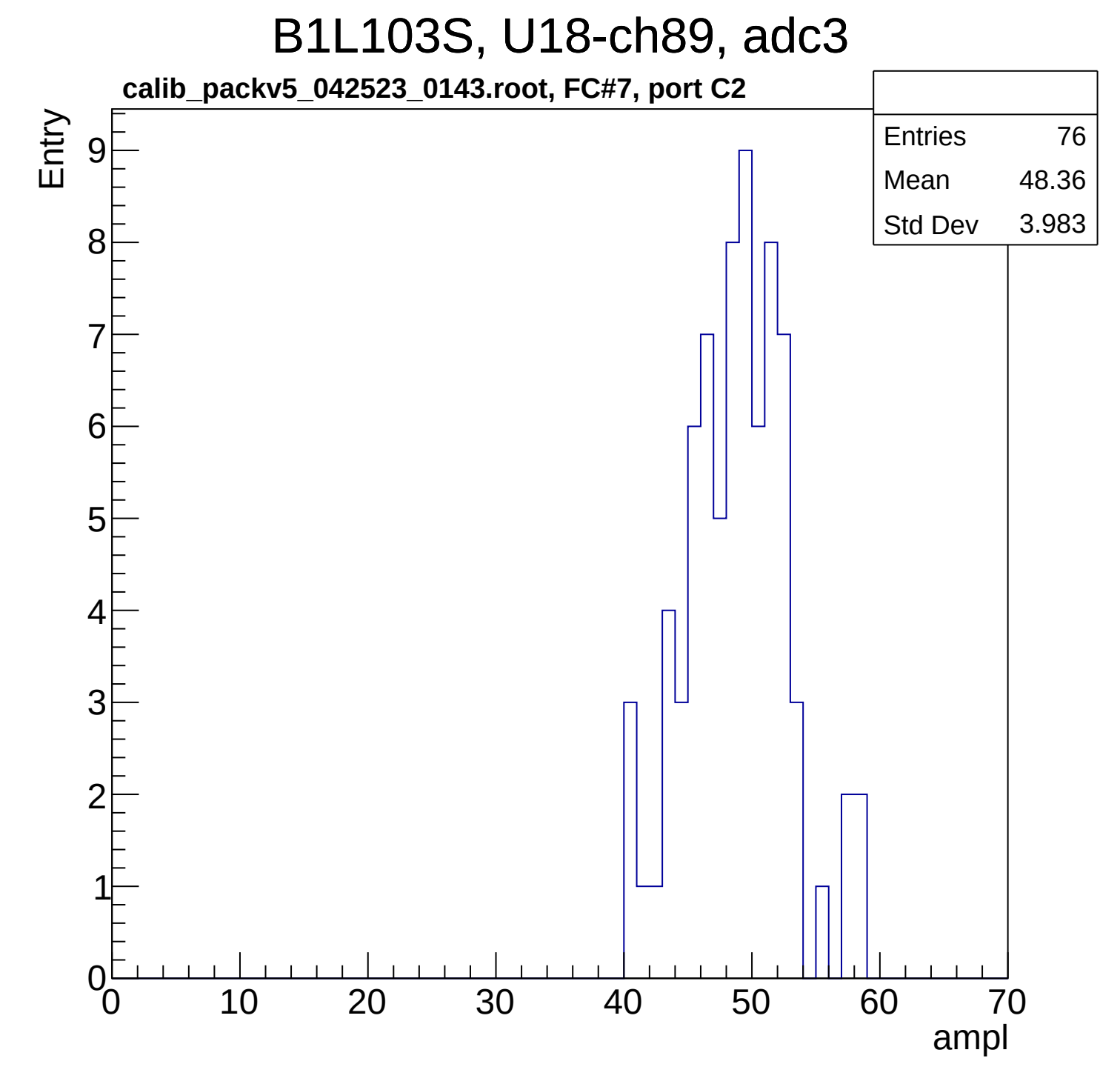
B1L103S, U18-ch89, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 76
Mean 48.36
Std Dev 3.983
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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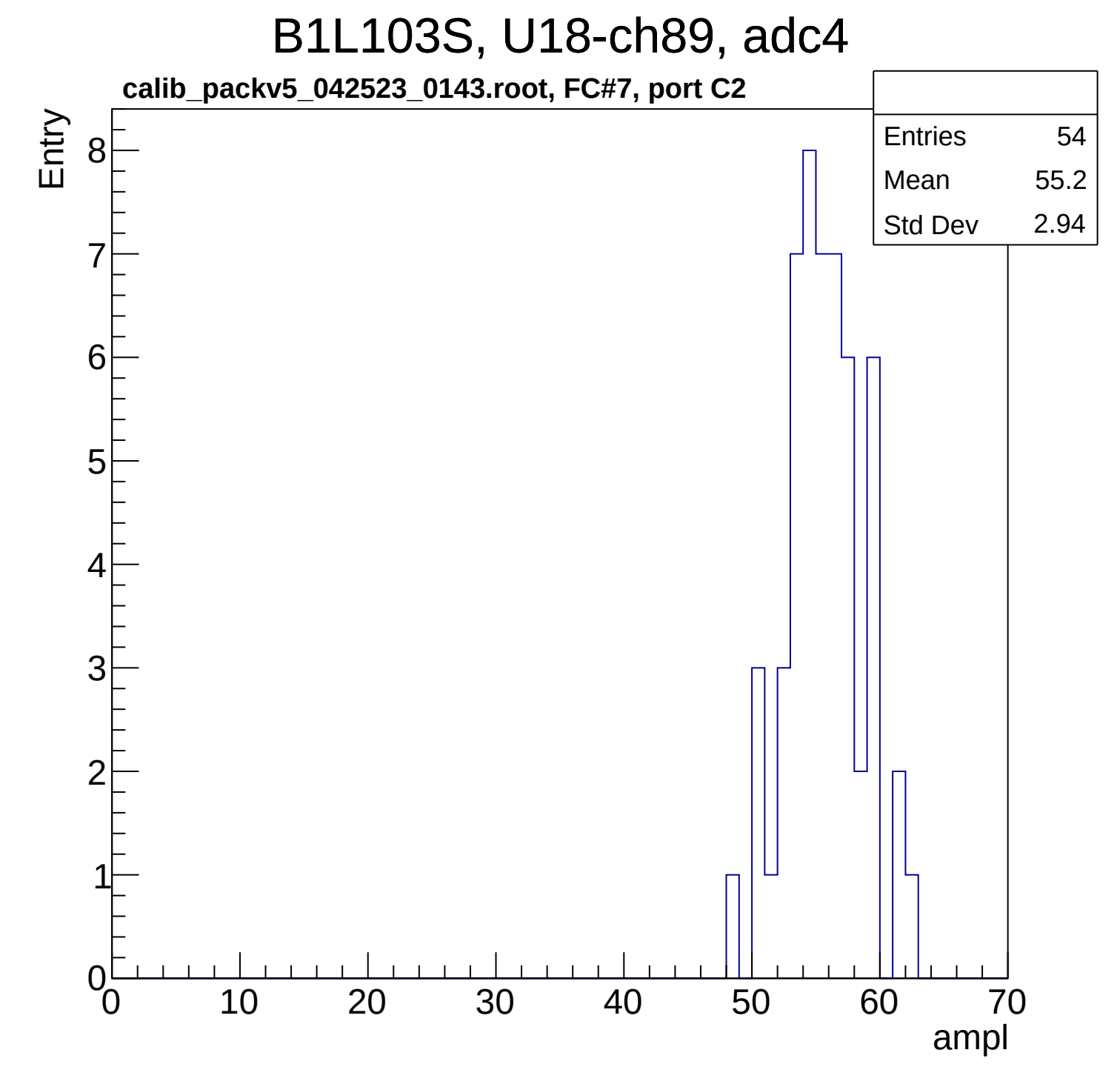
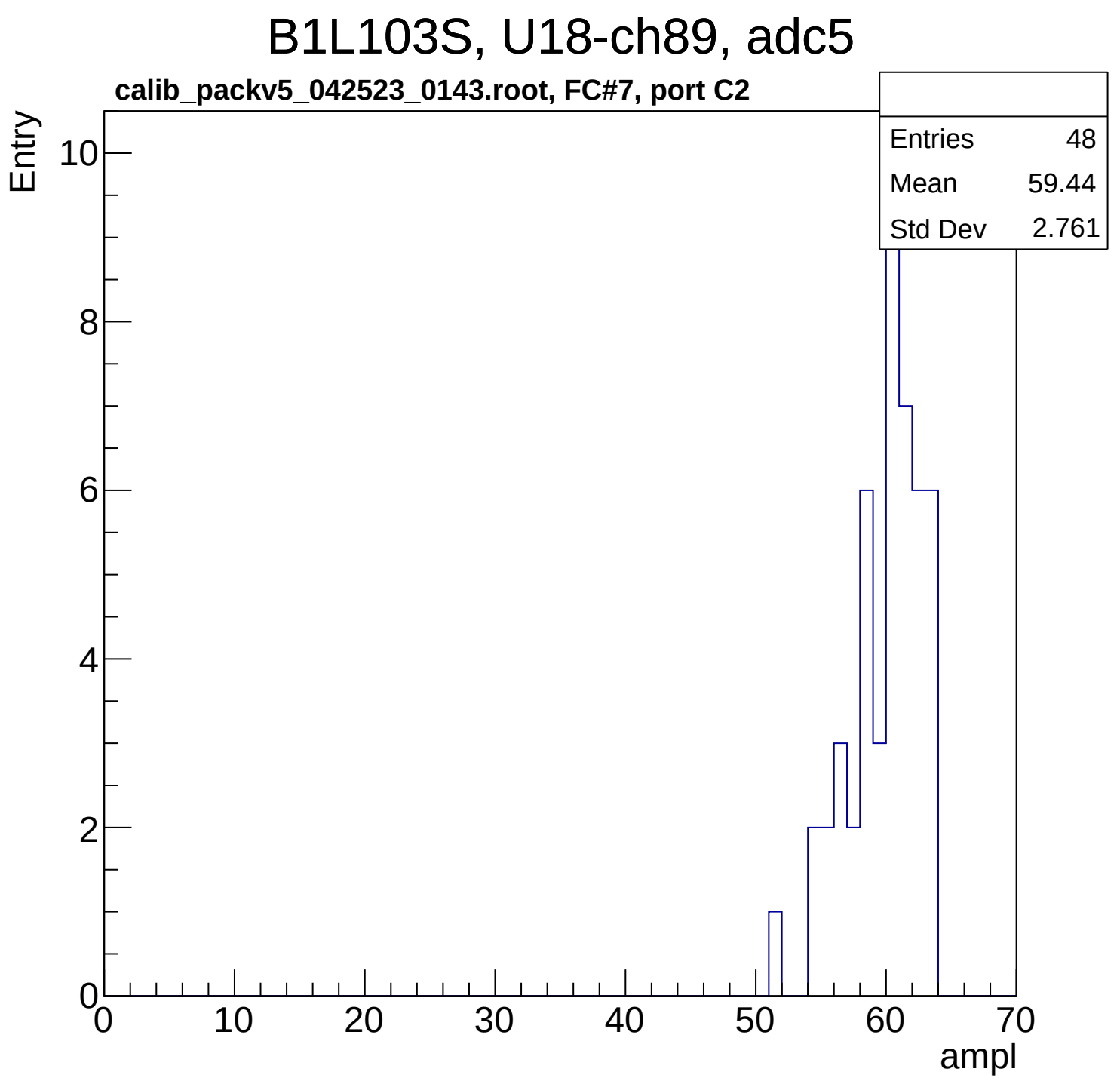
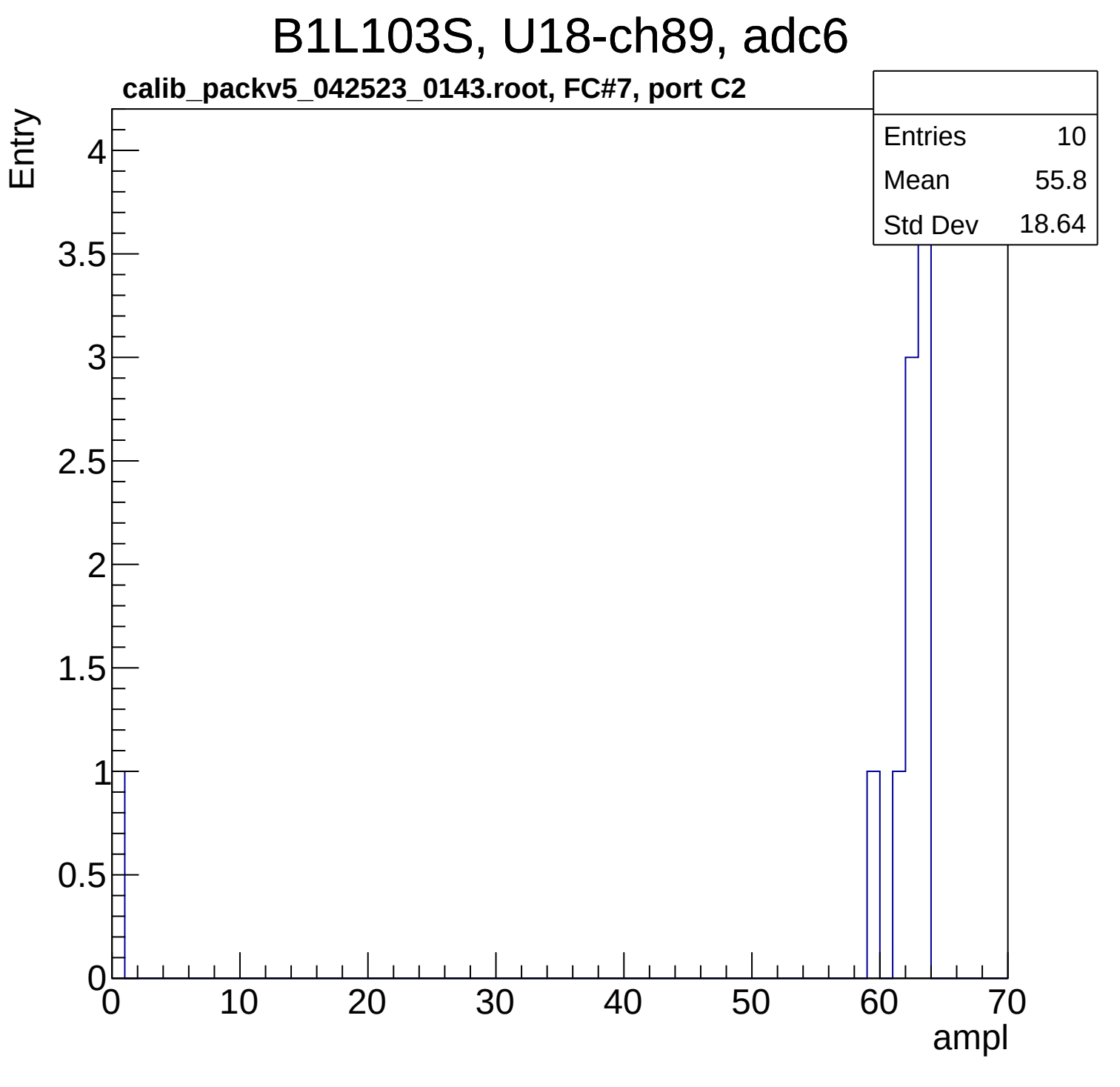
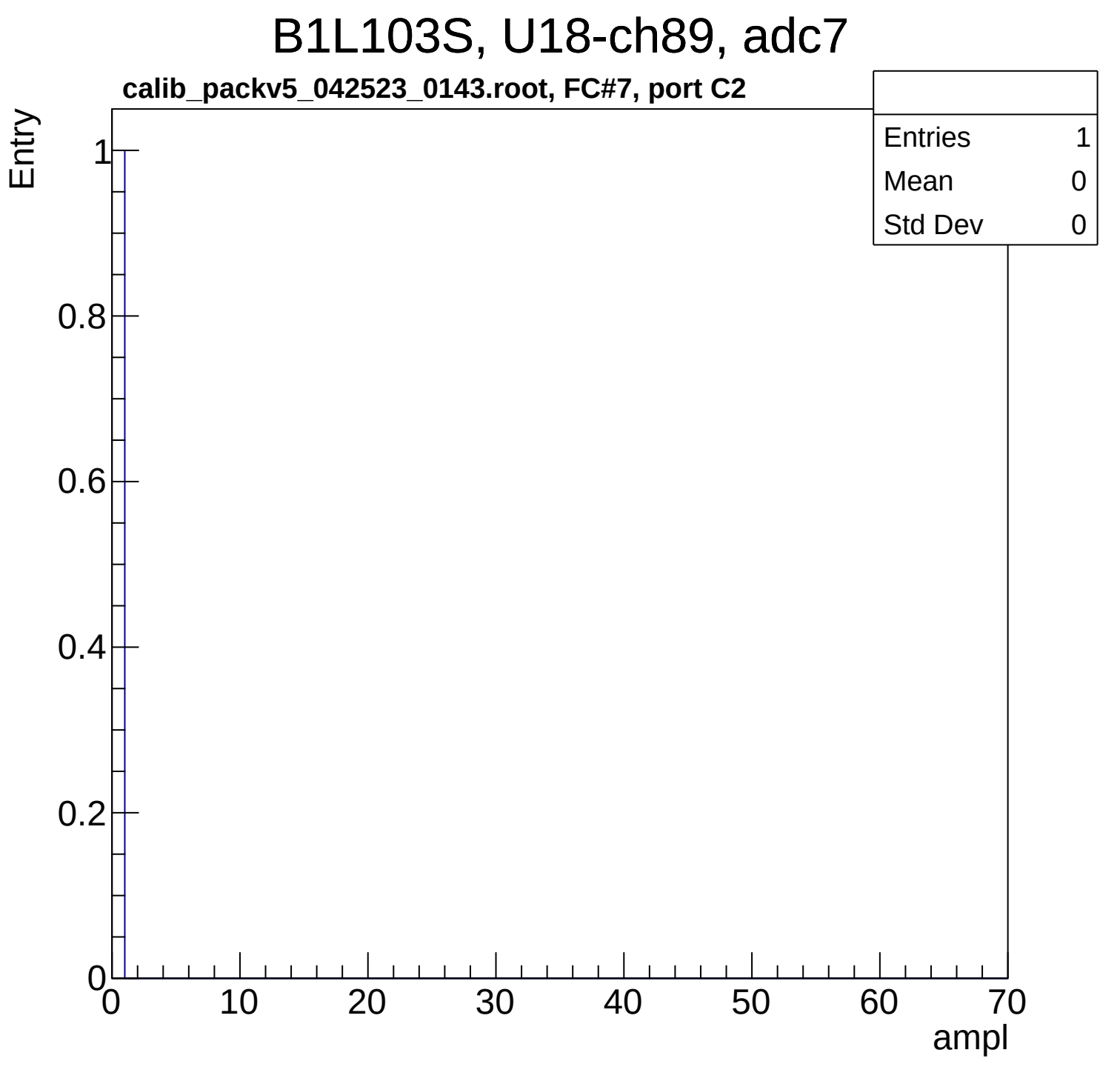
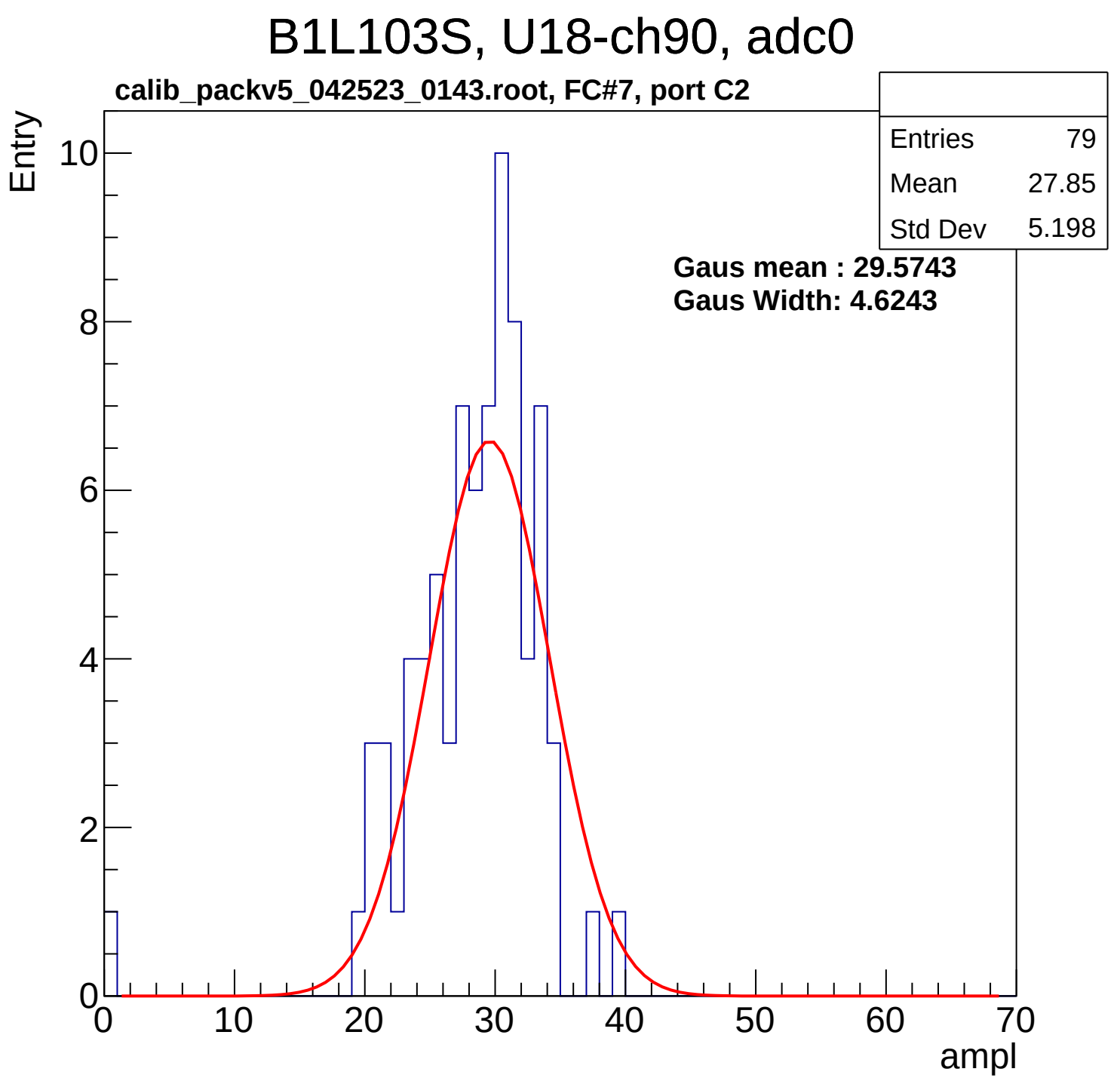
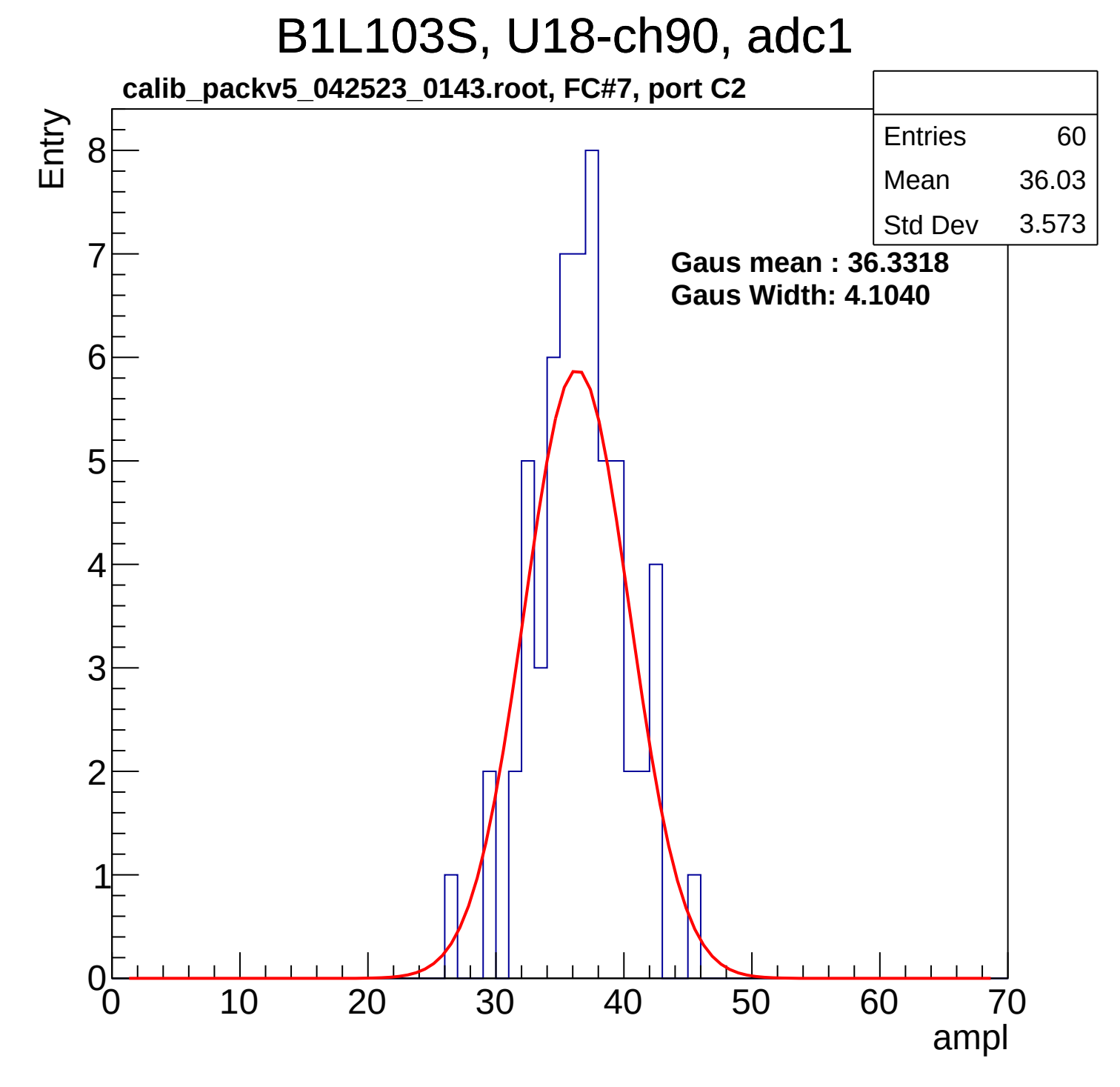

B1L103S, U18-ch89, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 54
Mean 55.2
Std Dev 2.94
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch89, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 48
Mean 59.44
Std Dev 2.761
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch89, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 10
Mean 55.8
Std Dev 18.64
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U18-ch89, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch90, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 79
Mean 27.85
Std Dev 5.198
Gaus mean : 29.5743
Gaus Width: 4.6243
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch90, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 60
Mean 36.03
Std Dev 3.573
Gaus mean : 36.3318
Gaus Width: 4.1040
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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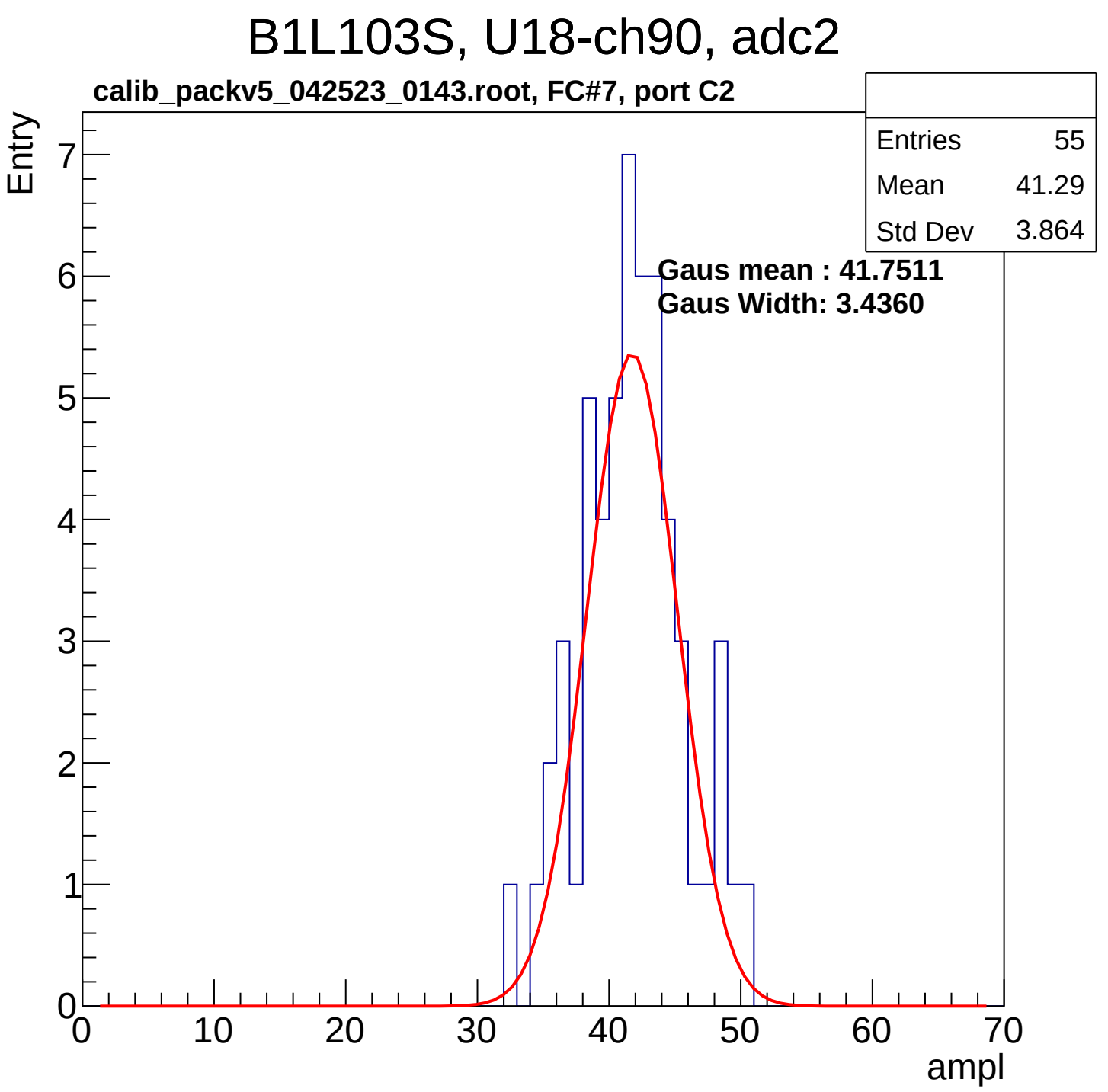
B1L103S, U18-ch90, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 41.29
Std Dev 3.864
Gaus mean : 41.7511
Gaus Width: 3.4360
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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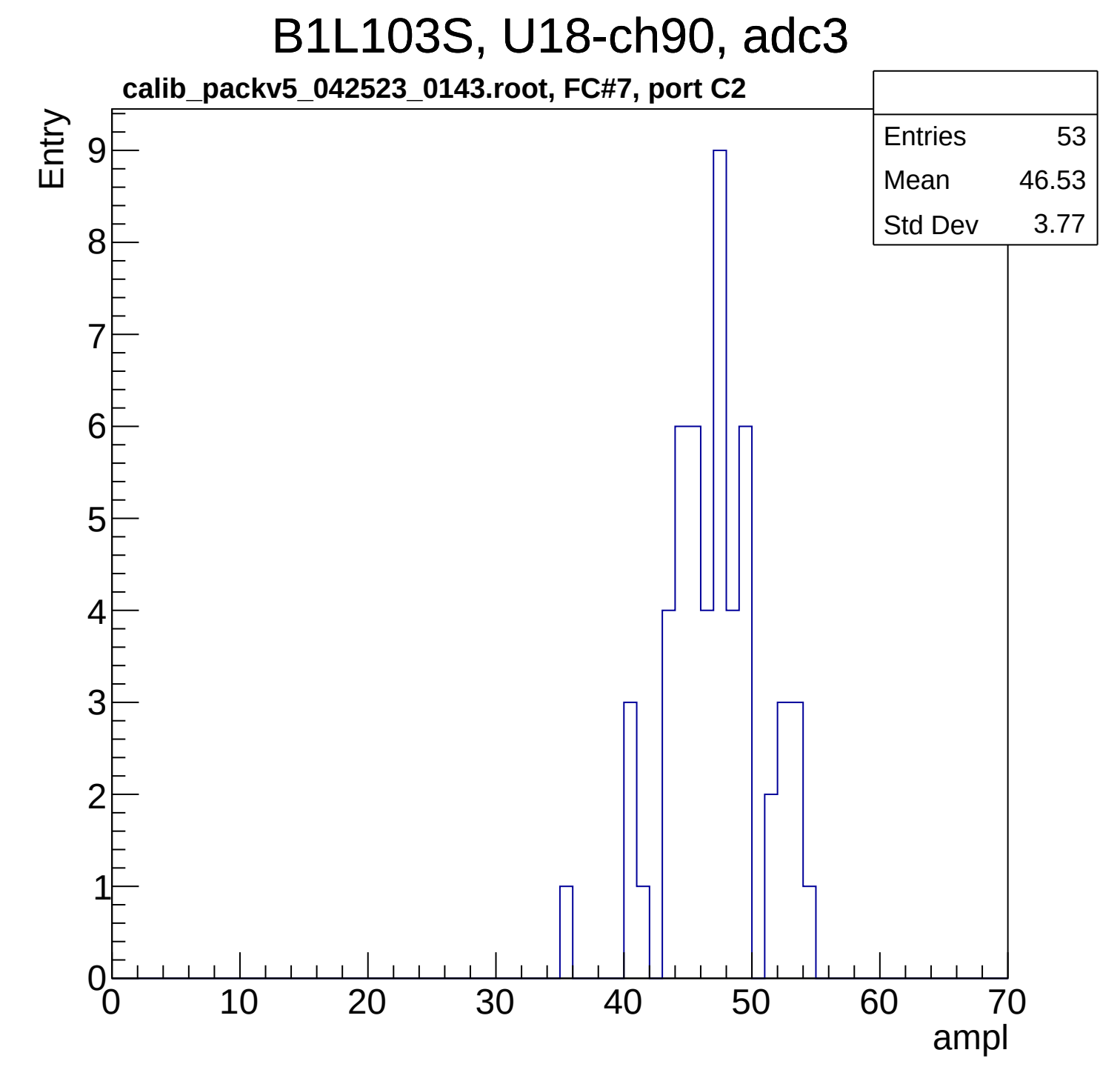
B1L103S, U18-ch90, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 46.53
Std Dev 3.77
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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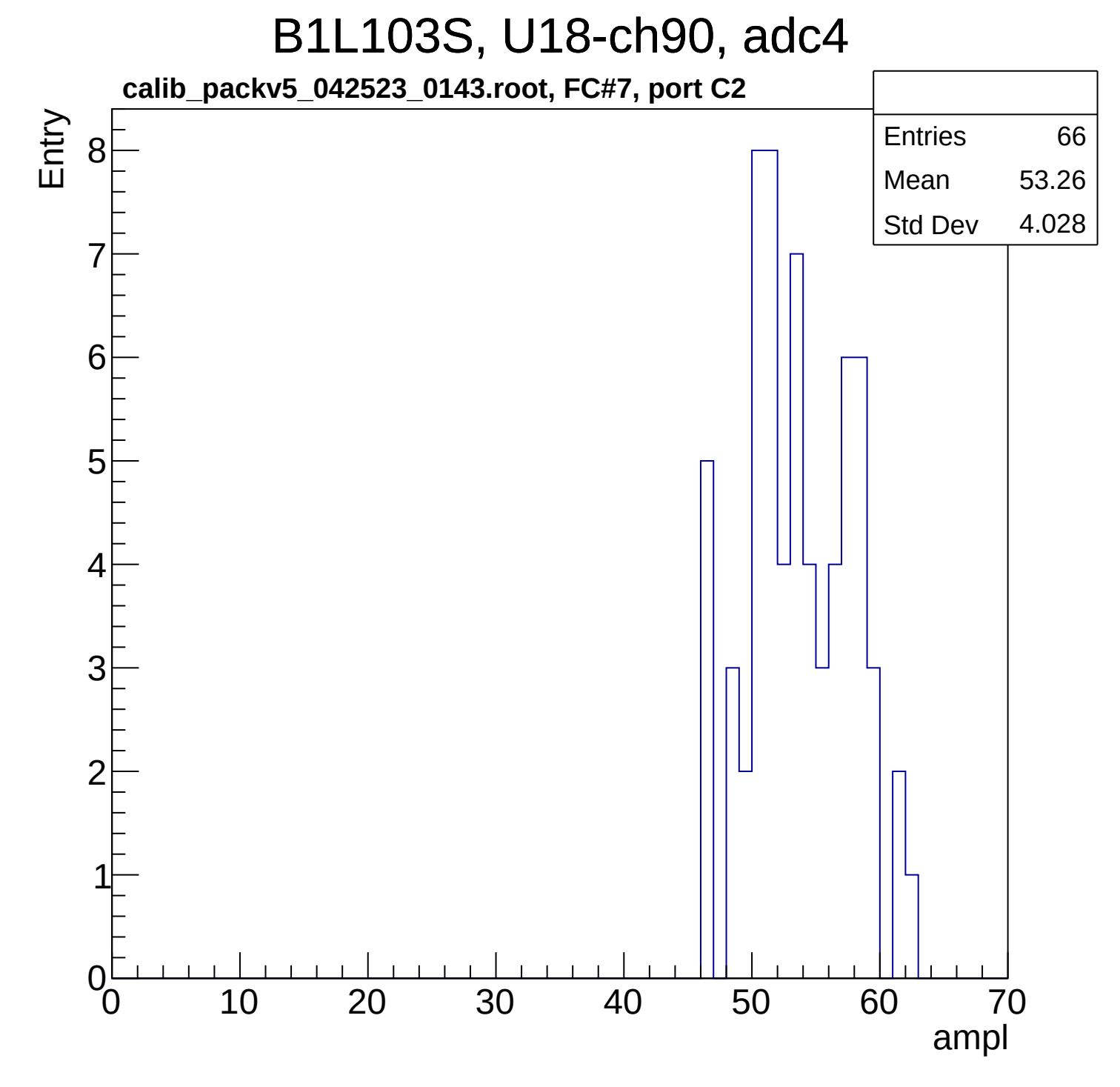
B1L103S, U18-ch90, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 53.26
Std Dev 4.028
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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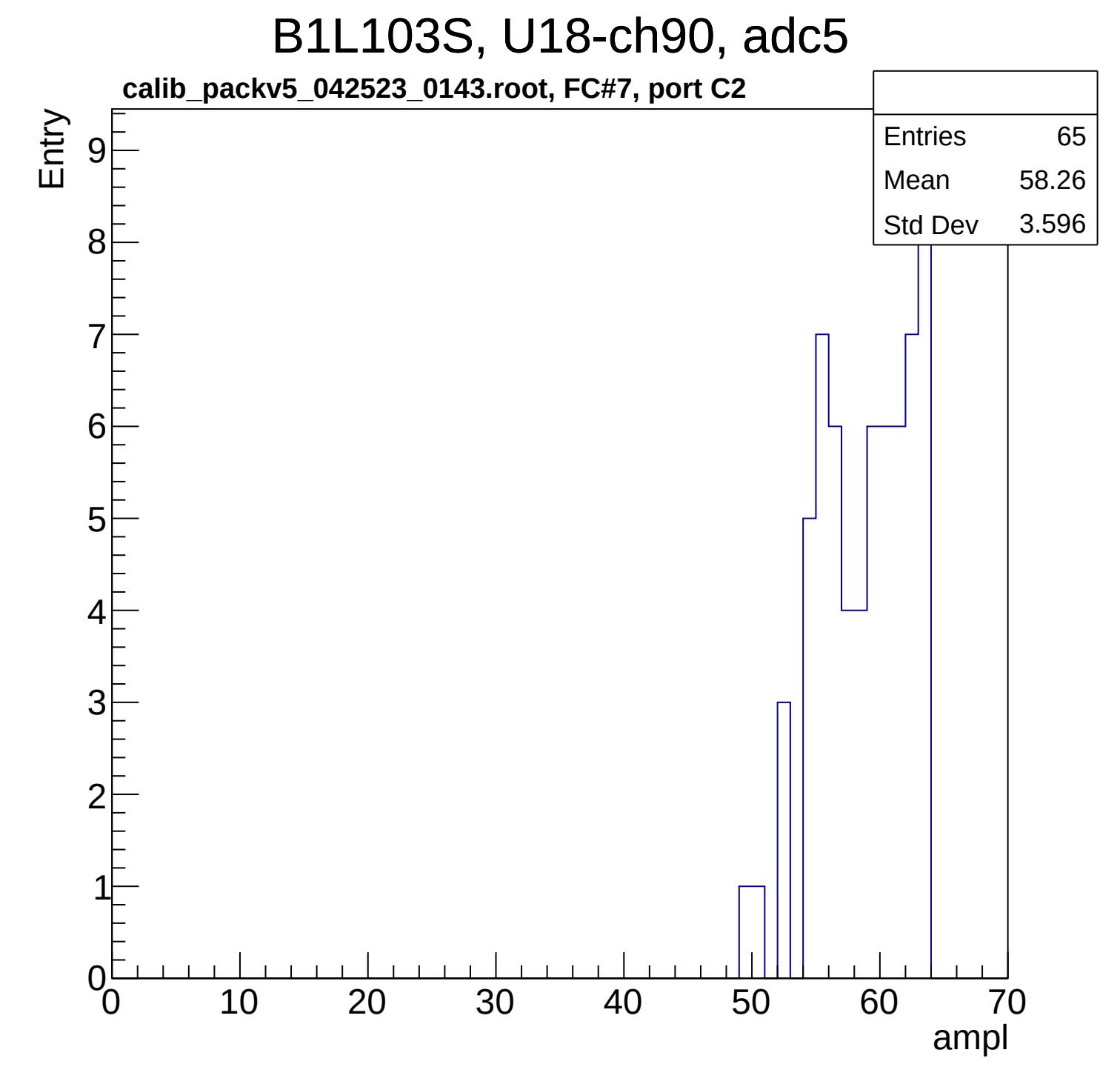
B1L103S, U18-ch90, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 58.26
Std Dev 3.596
Entry
ampl
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3
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5
6
7
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0
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60
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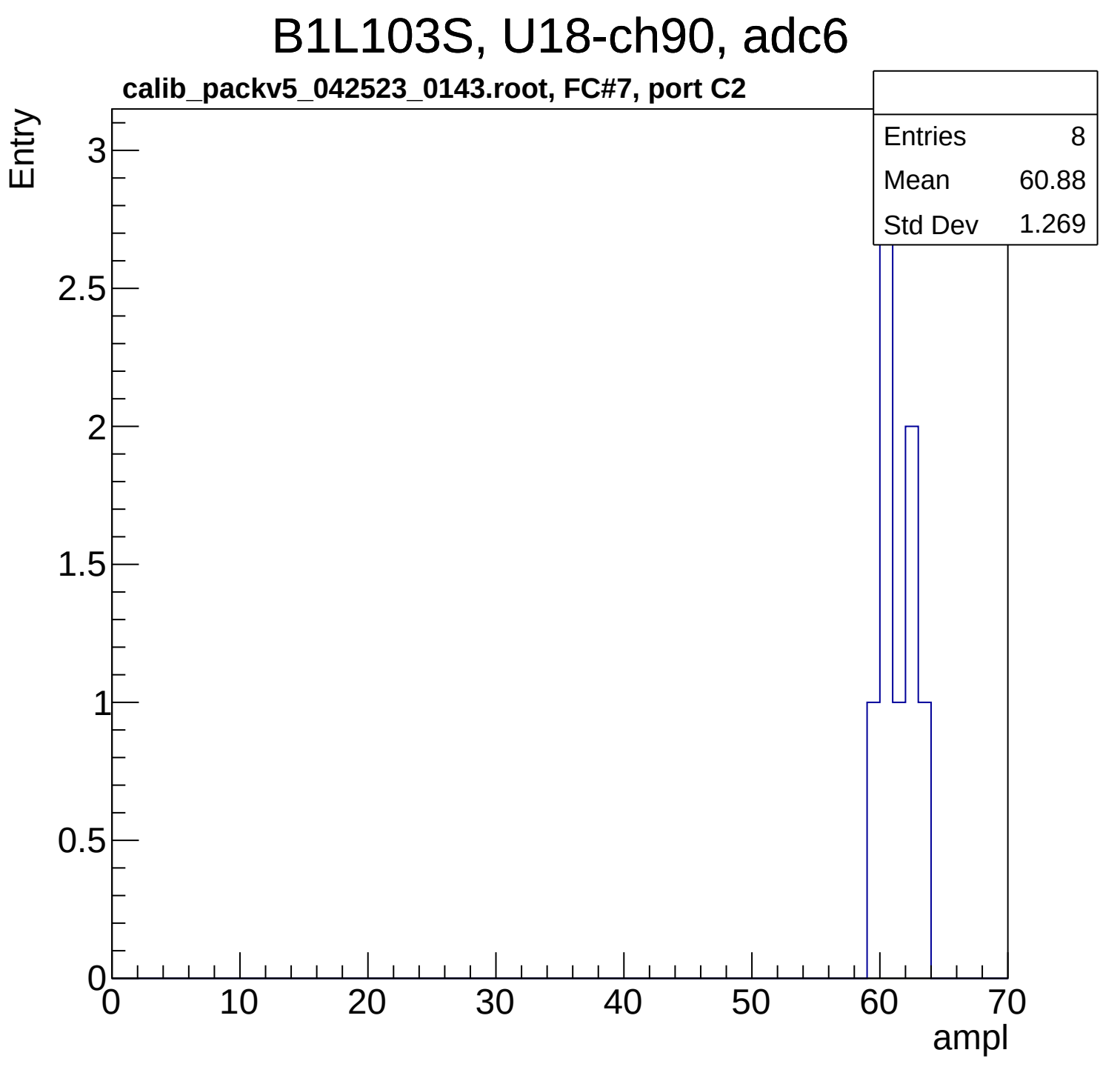
B1L103S, U18-ch90, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 8
Mean 60.88
Std Dev 1.269
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
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20
30
40
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60
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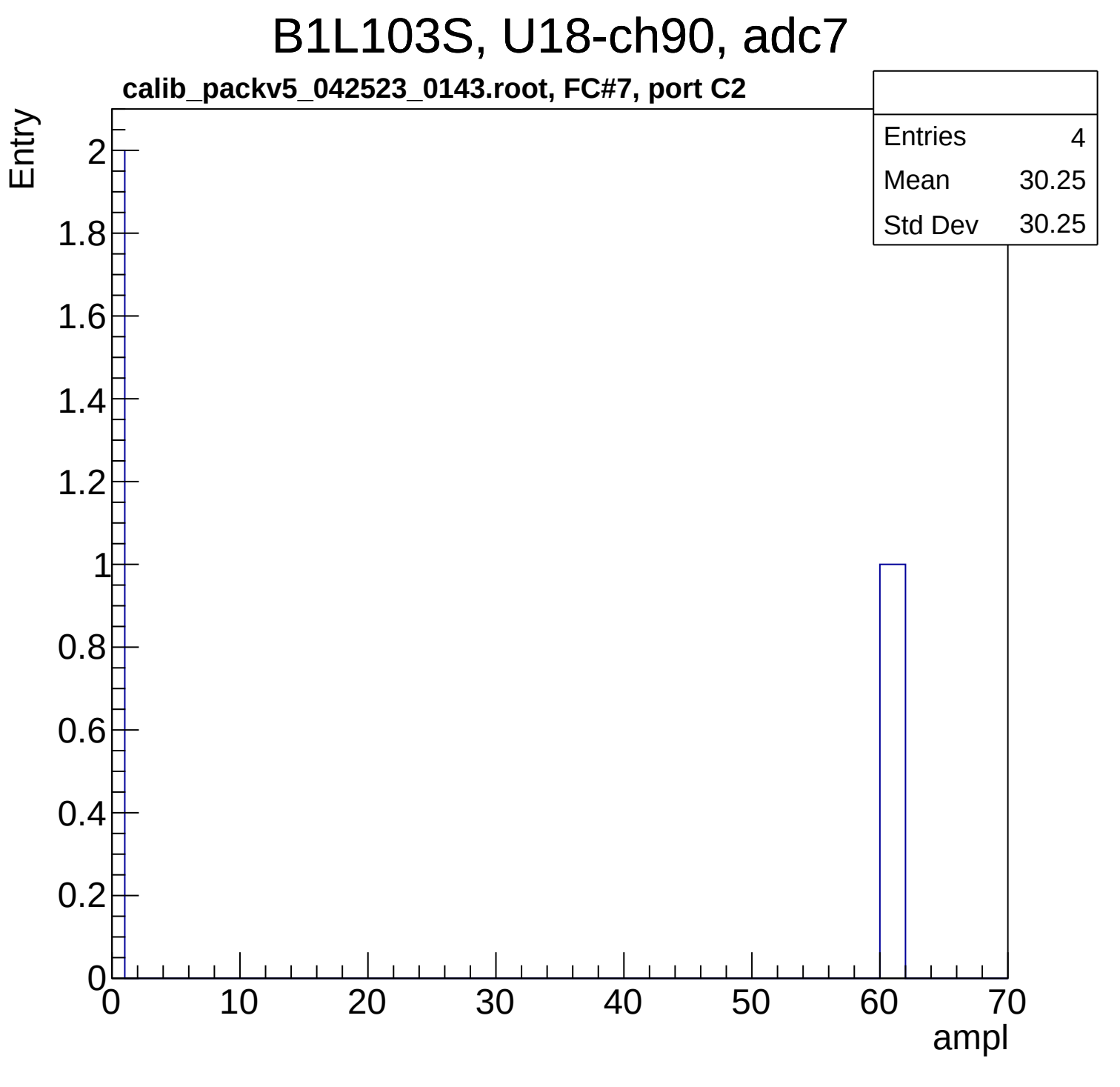
B1L103S, U18-ch90, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 4
Mean 30.25
Std Dev 30.25
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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40
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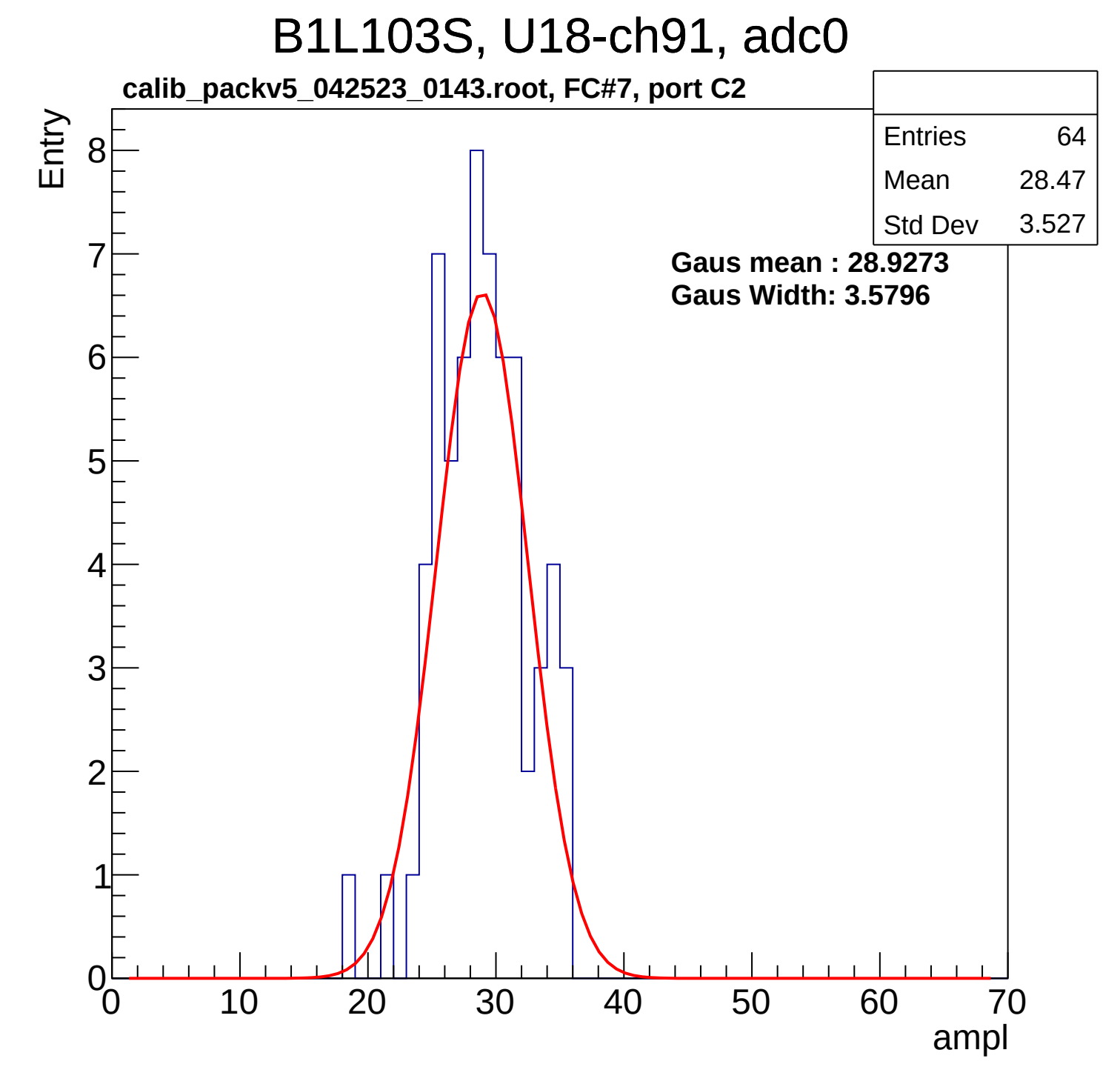
60
70


B1L103S, U18-ch91, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 28.47
Std Dev 3.527
Gaus mean : 28.9273
Gaus Width: 3.5796
Entry
ampl
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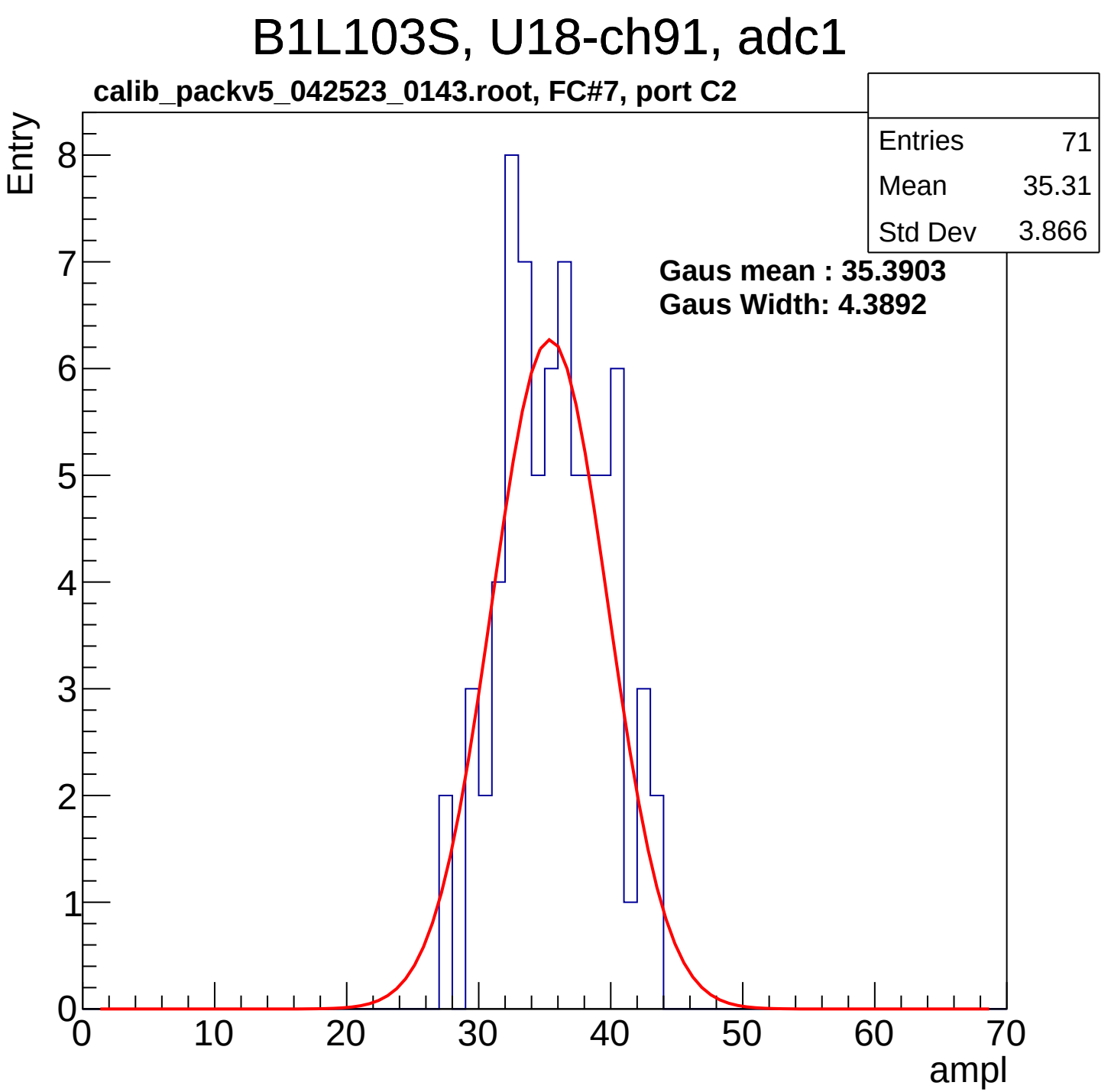
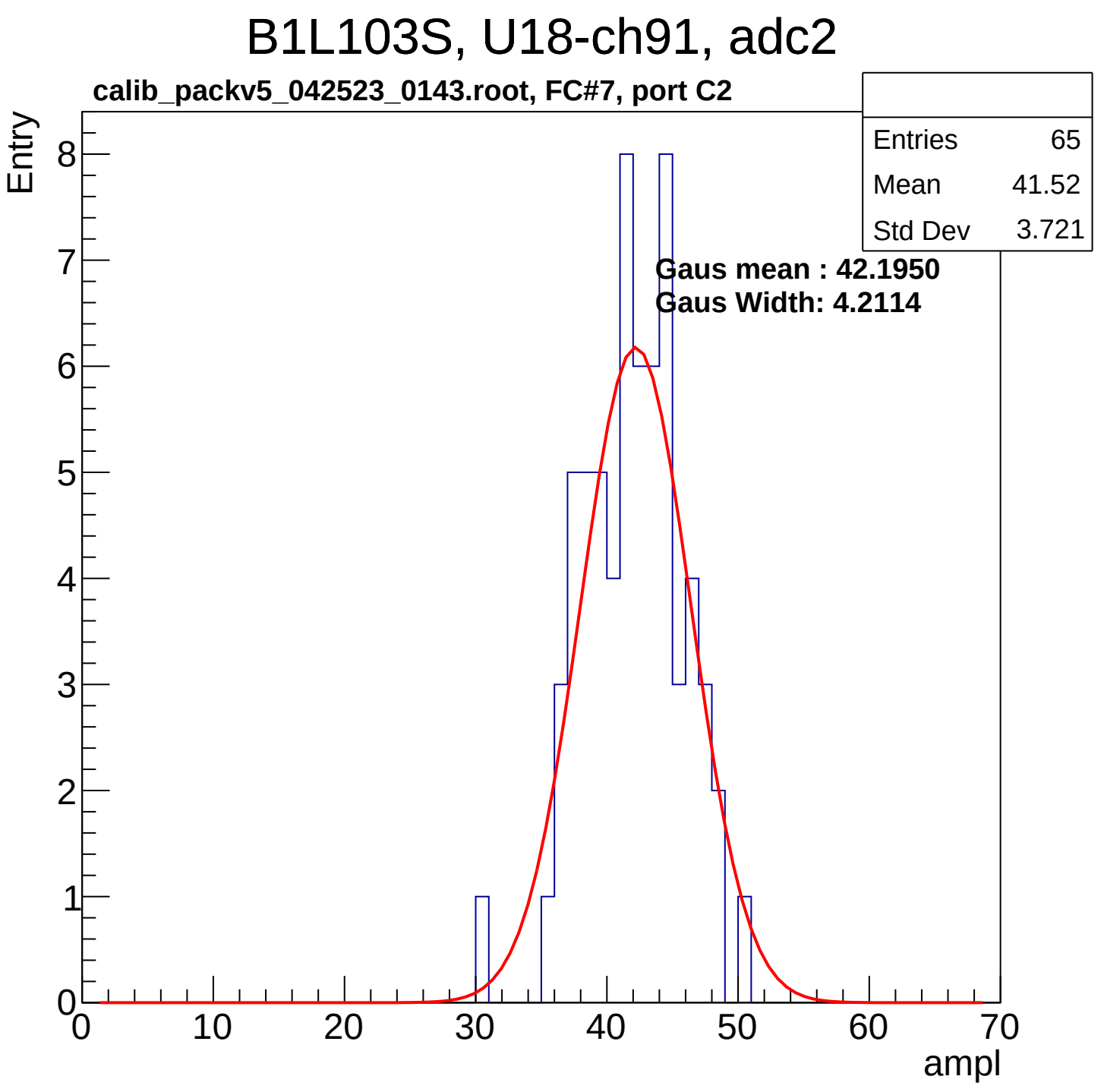
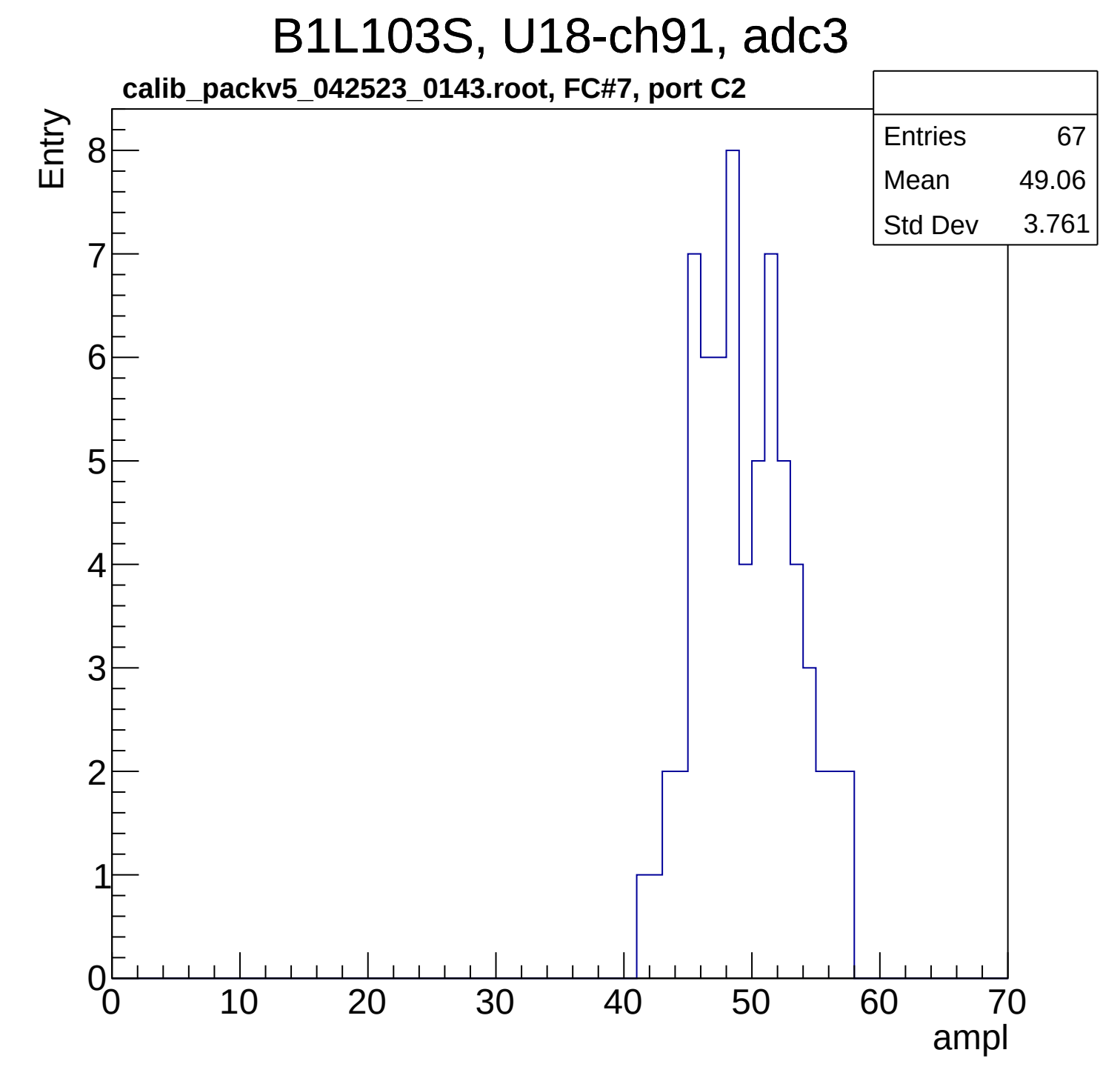
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch91, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 71
Mean 35.31
Std Dev 3.866
Gaus mean : 35.3903
Gaus Width: 4.3892
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch91, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 41.52
Std Dev 3.721
Gaus mean : 42.1950
Gaus Width: 4.2114
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch91, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 49.06
Std Dev 3.761
Entry
ampl
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3
4
5
6
7
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0
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20
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60
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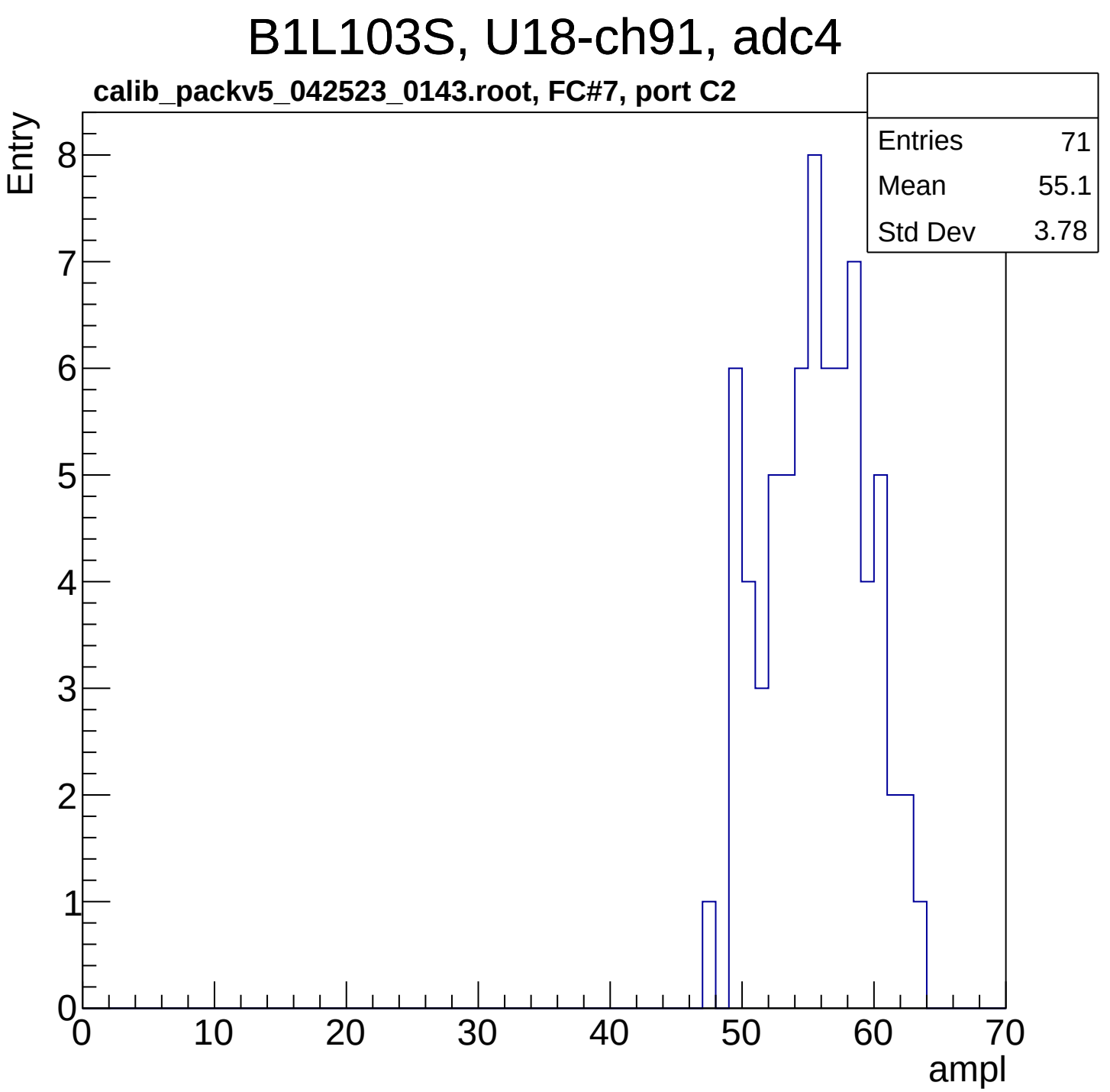
B1L103S, U18-ch91, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 71
Mean 55.1
Std Dev 3.78
Entry
ampl
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1
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3
4
5
6
7
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0
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20
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40
50
60
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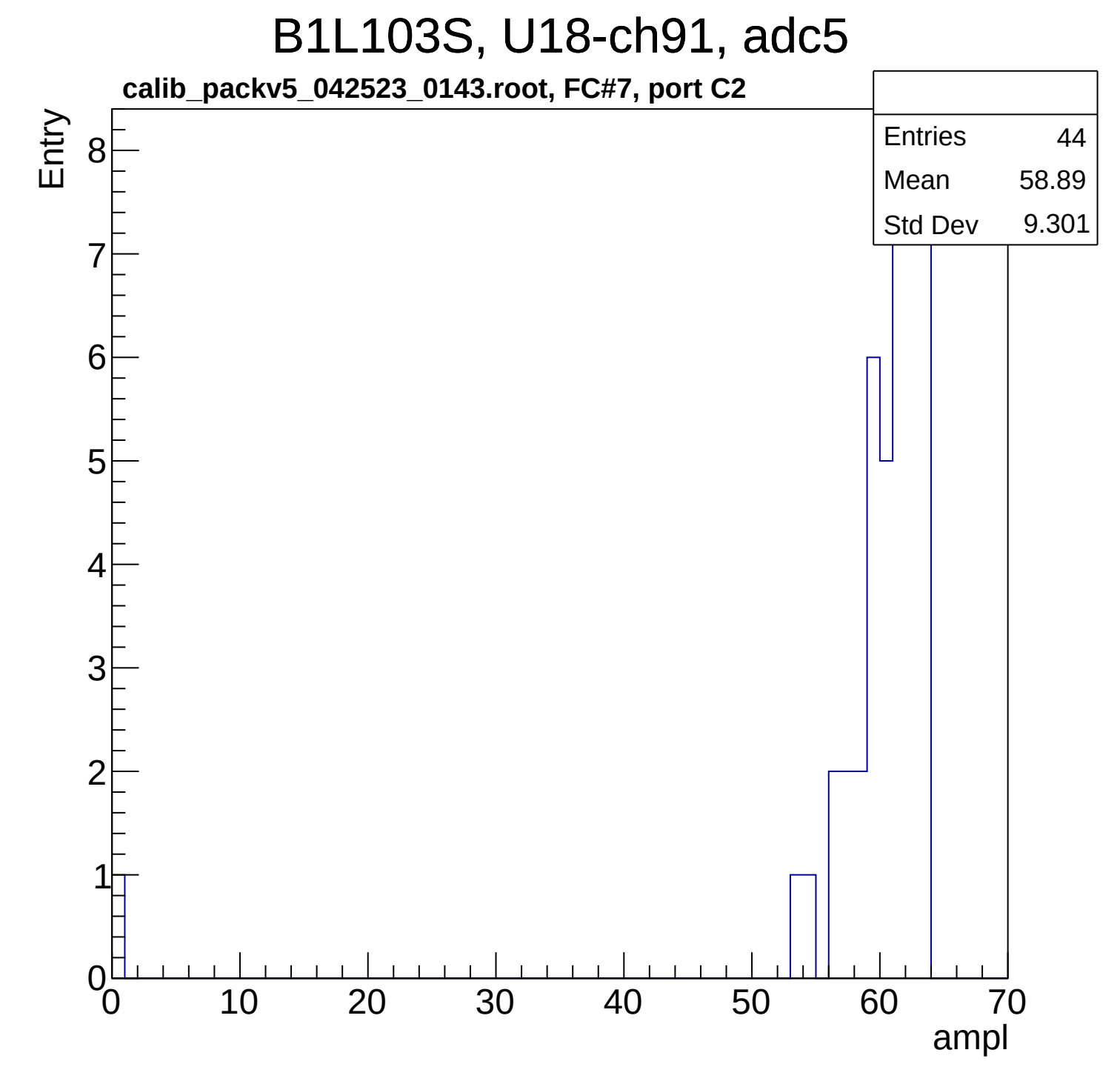
B1L103S, U18-ch91, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 44
Mean 58.89
Std Dev 9.301
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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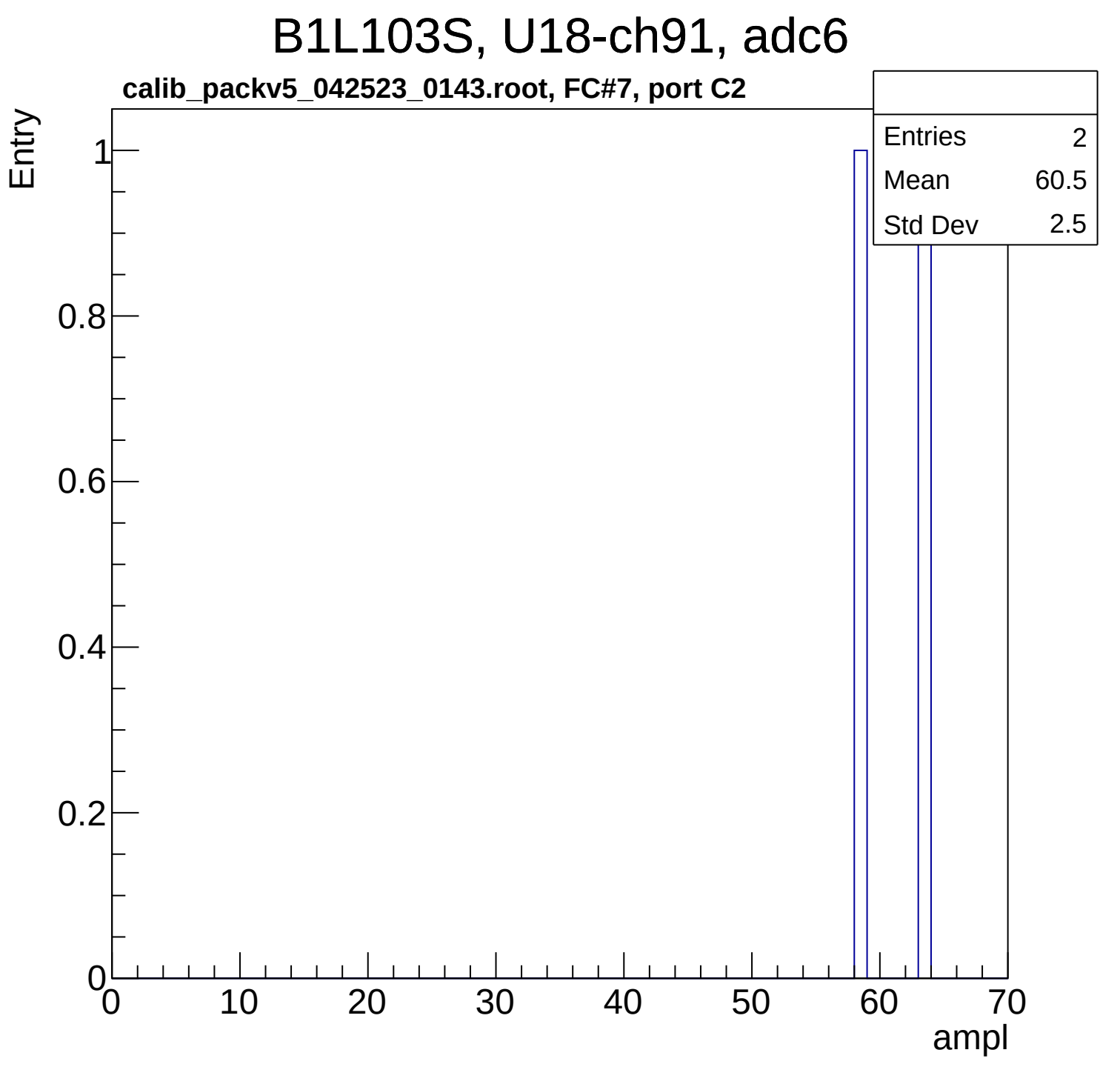
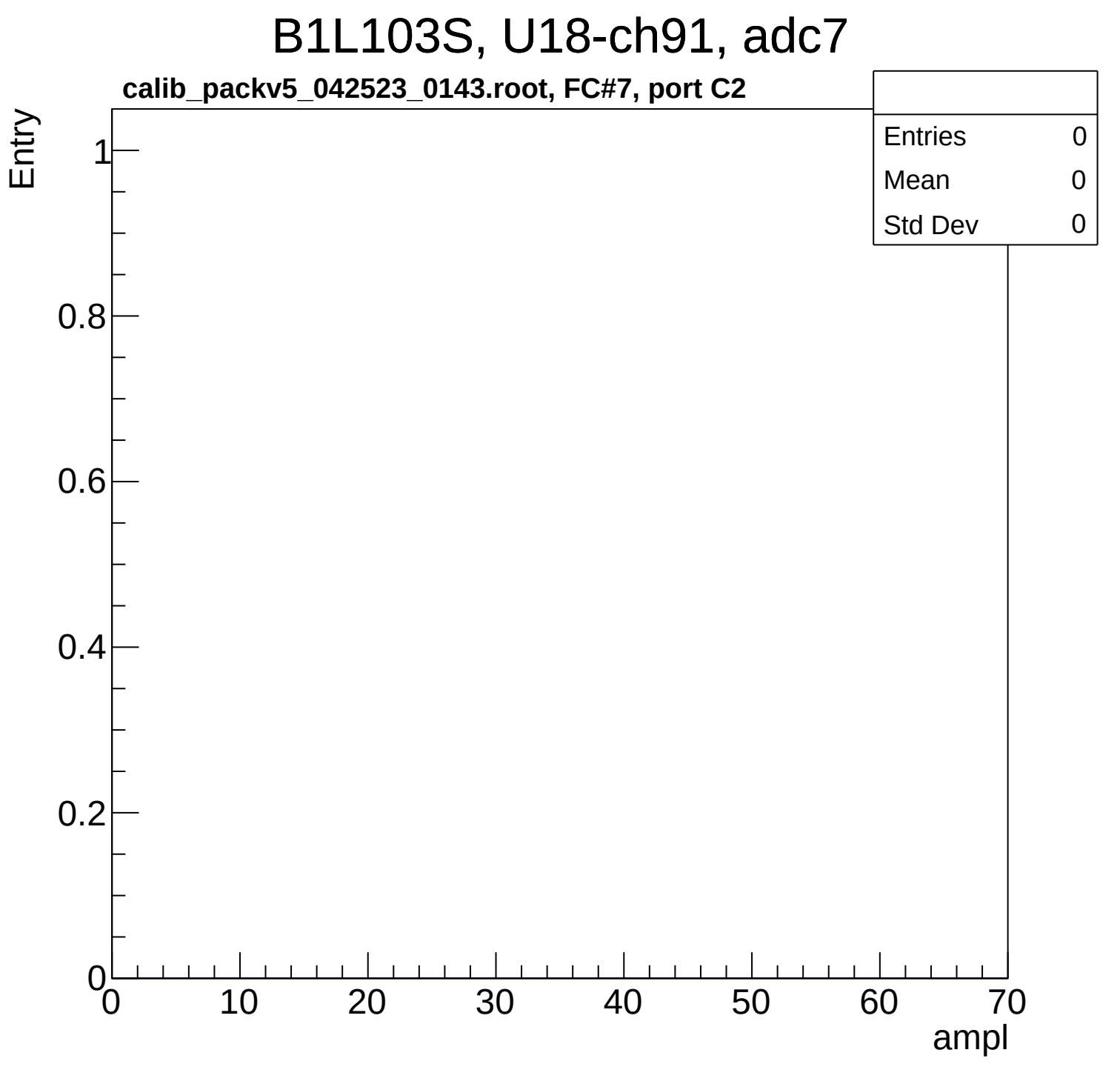
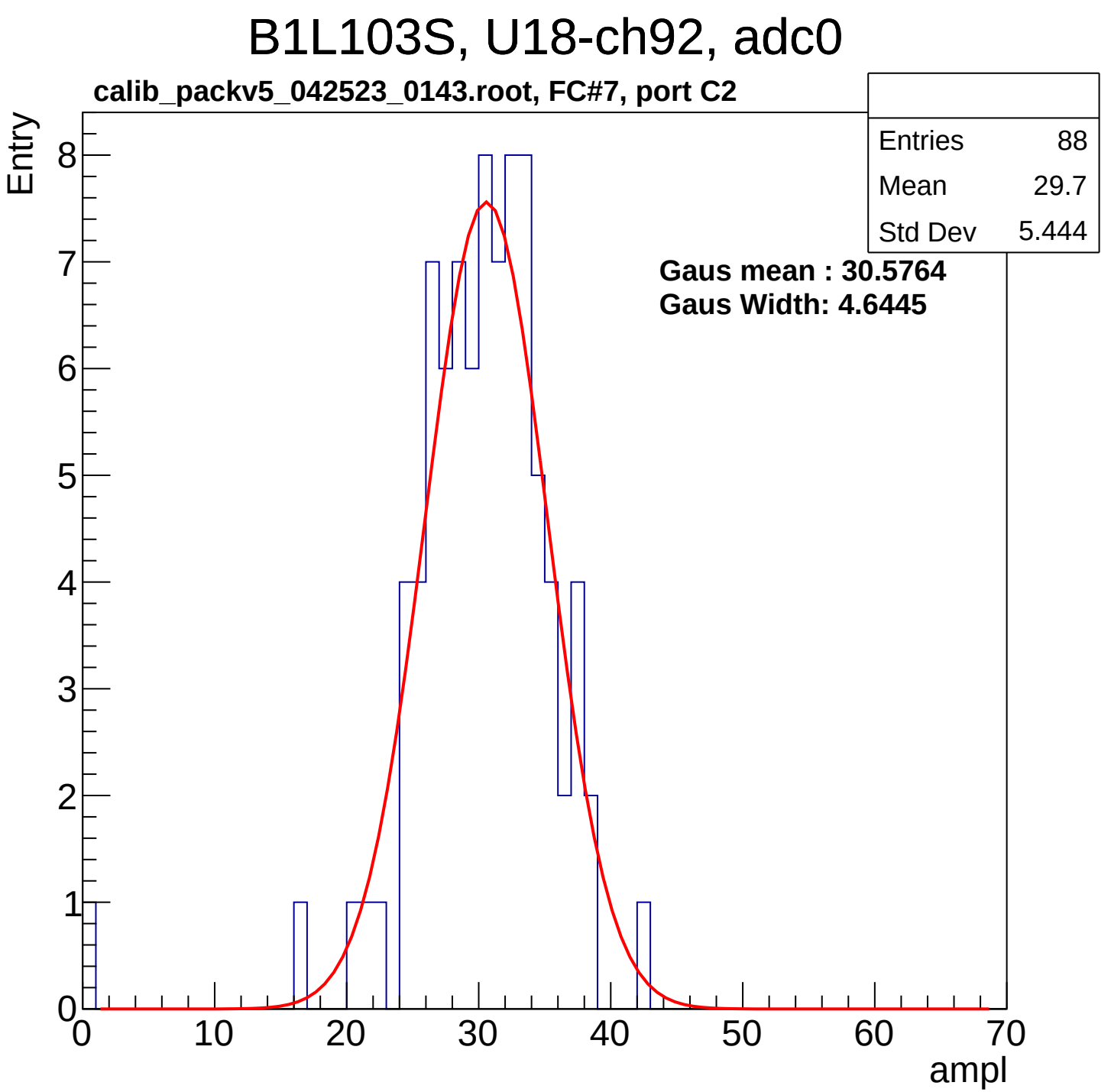

B1L103S, U18-ch91, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 60.5
Std Dev 2.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch91, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch92, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 88
Mean 29.7
Std Dev 5.444
Gaus mean : 30.5764
Gaus Width: 4.6445
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
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40
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60
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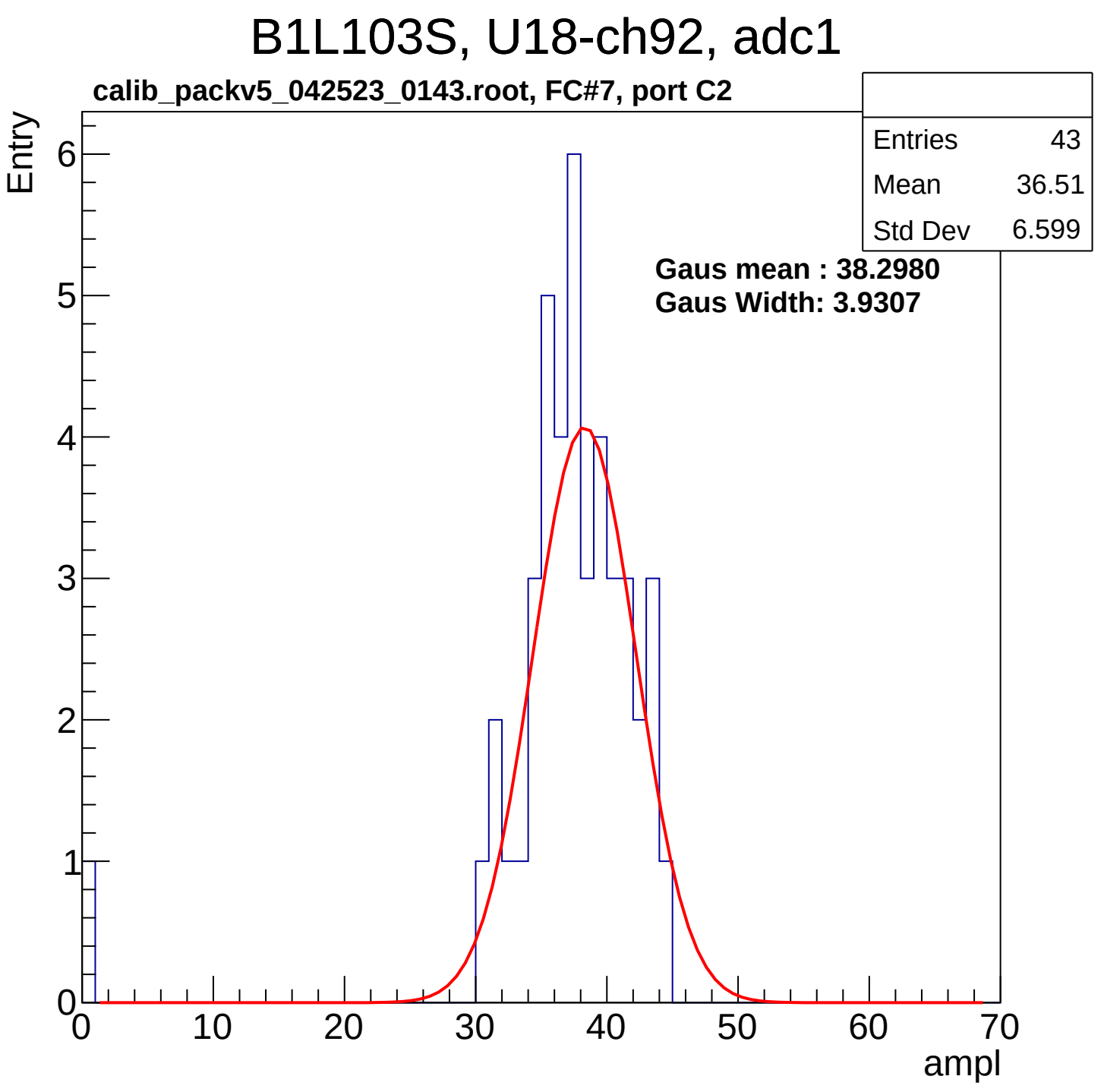
B1L103S, U18-ch92, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 43
Mean 36.51
Std Dev 6.599
Gaus mean : 38.2980
Gaus Width: 3.9307
Entry
ampl
0
1
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3
4
5
6
0
10
20
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40
50
60
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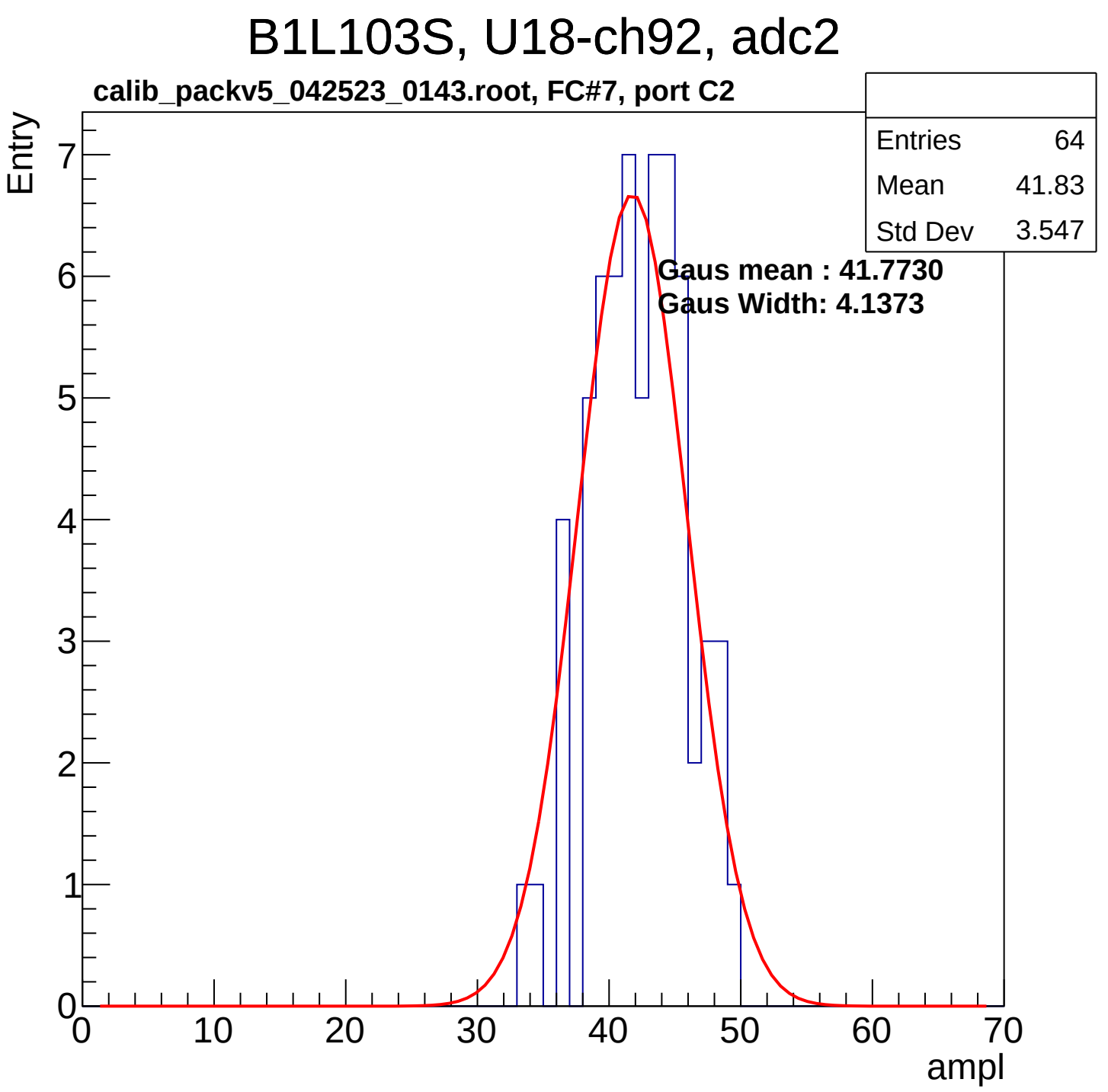
B1L103S, U18-ch92, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 41.83
Std Dev 3.547
Gaus mean : 41.7730
Gaus Width: 4.1373
Entry
ampl
0
1
2
3
4
5
6
7
0
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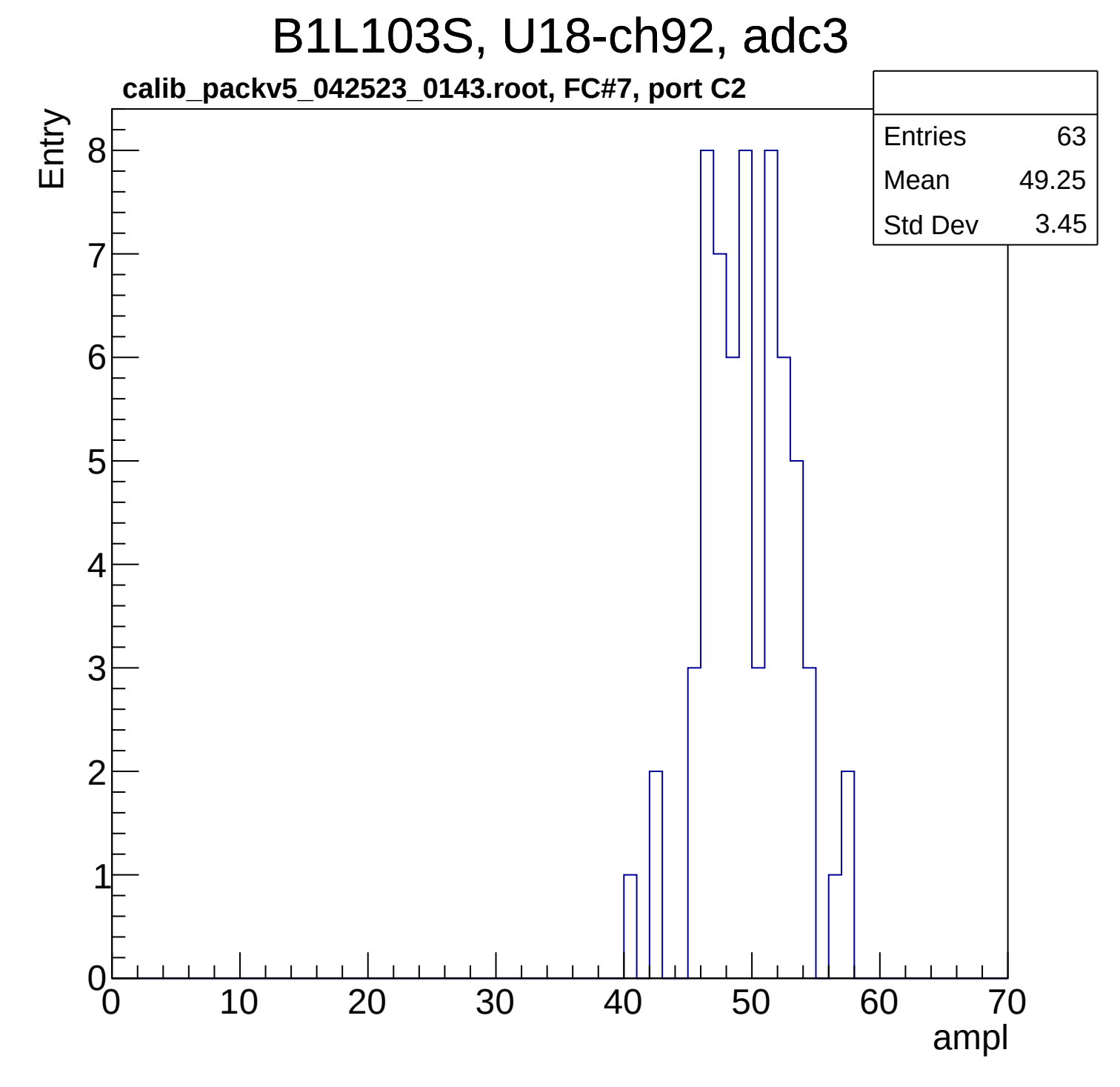
60
70


B1L103S, U18-ch92, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 49.25
Std Dev 3.45
Entry
ampl
0
1
2
3
4
5
6
7
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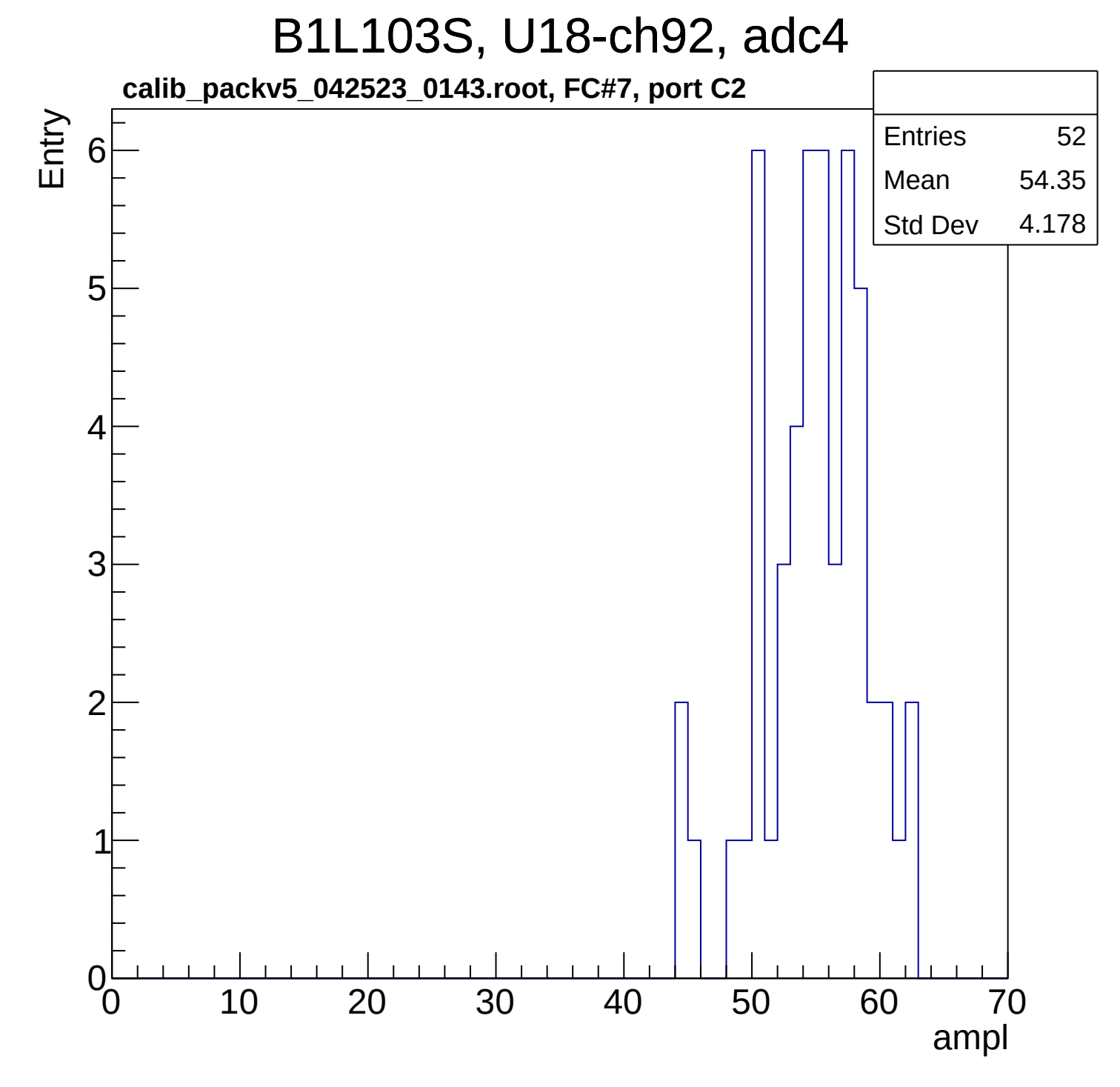
B1L103S, U18-ch92, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 52
Mean 54.35
Std Dev 4.178
Entry
ampl
0
1
2
3
4
5
6
0
10
20
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60
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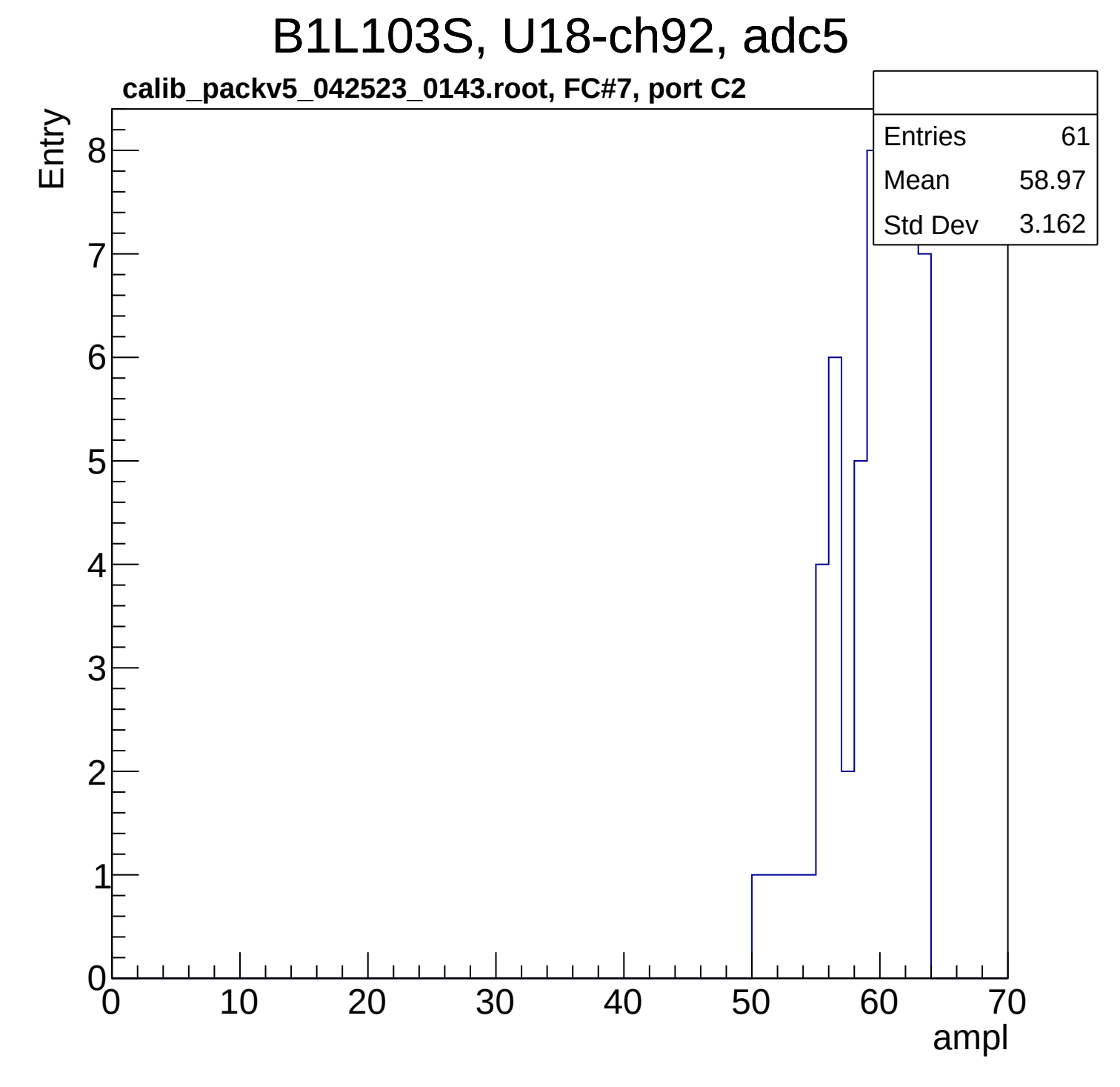
B1L103S, U18-ch92, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 61
Mean 58.97
Std Dev 3.162
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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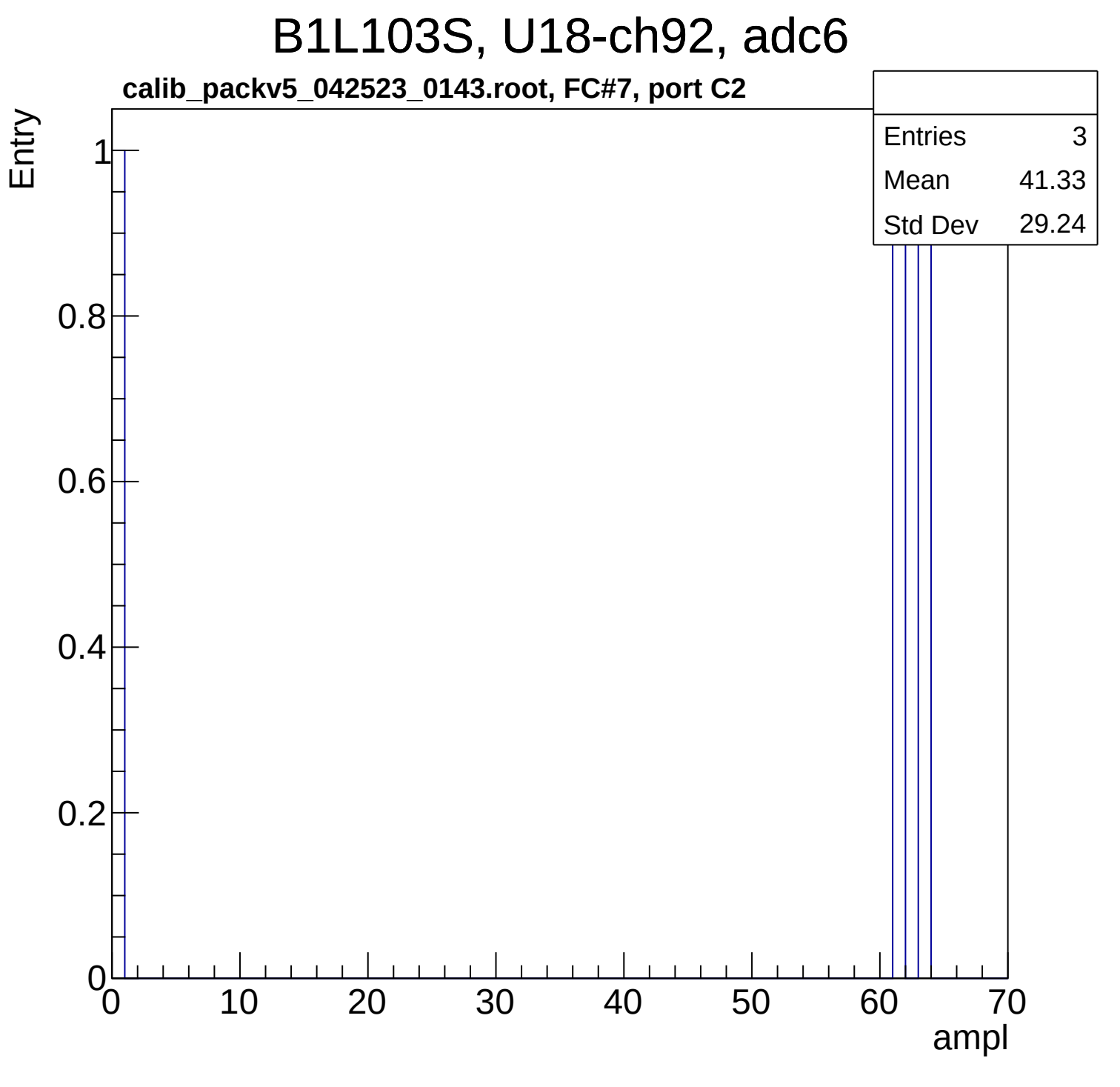
B1L103S, U18-ch92, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 41.33
Std Dev 29.24
Entry
ampl
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0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
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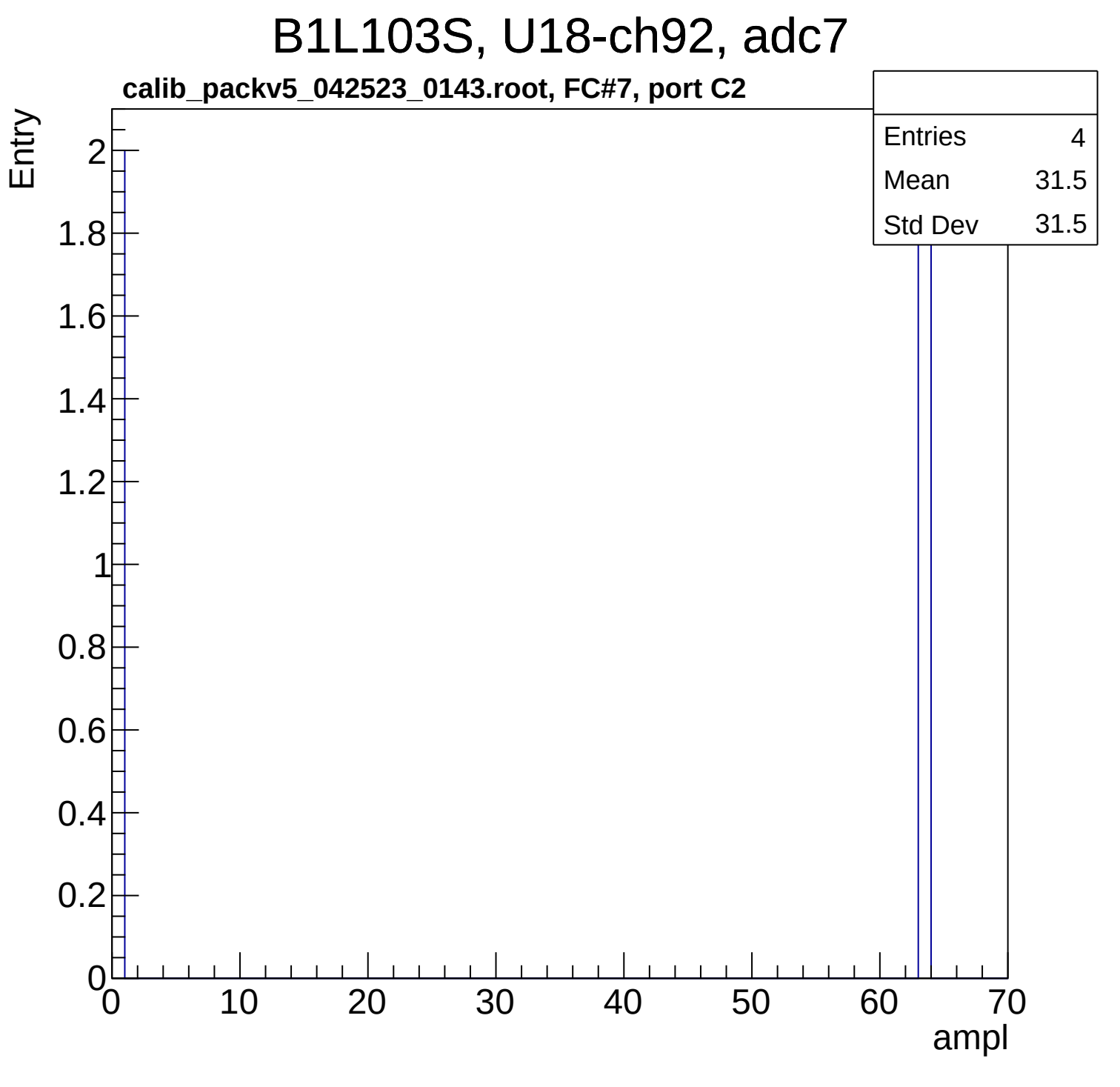
B1L103S, U18-ch92, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 4
Mean 31.5
Std Dev 31.5
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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40
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60
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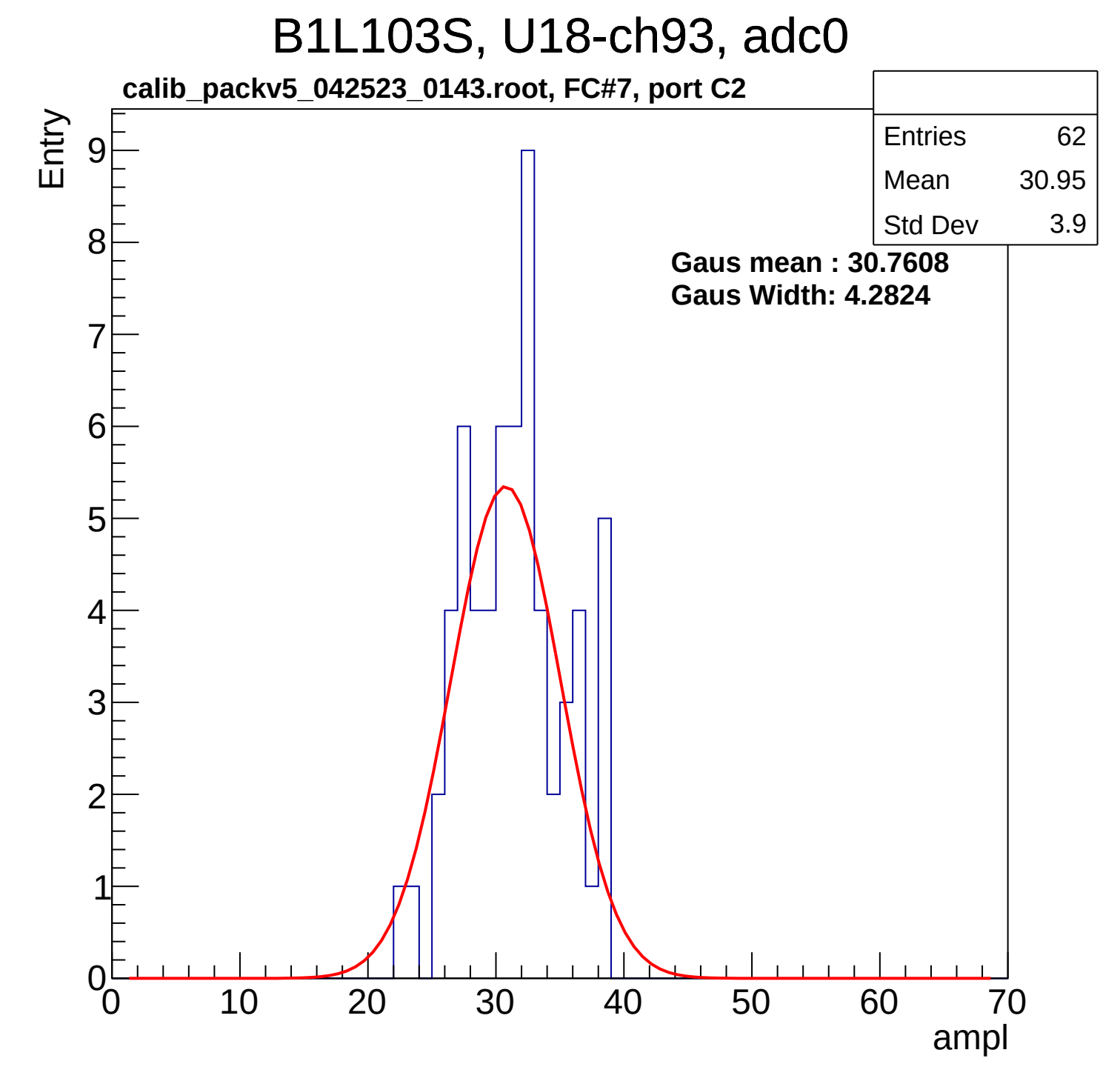
B1L103S, U18-ch93, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 62
Mean 30.95
Std Dev 3.9
Gaus mean : 30.7608
Gaus Width: 4.2824
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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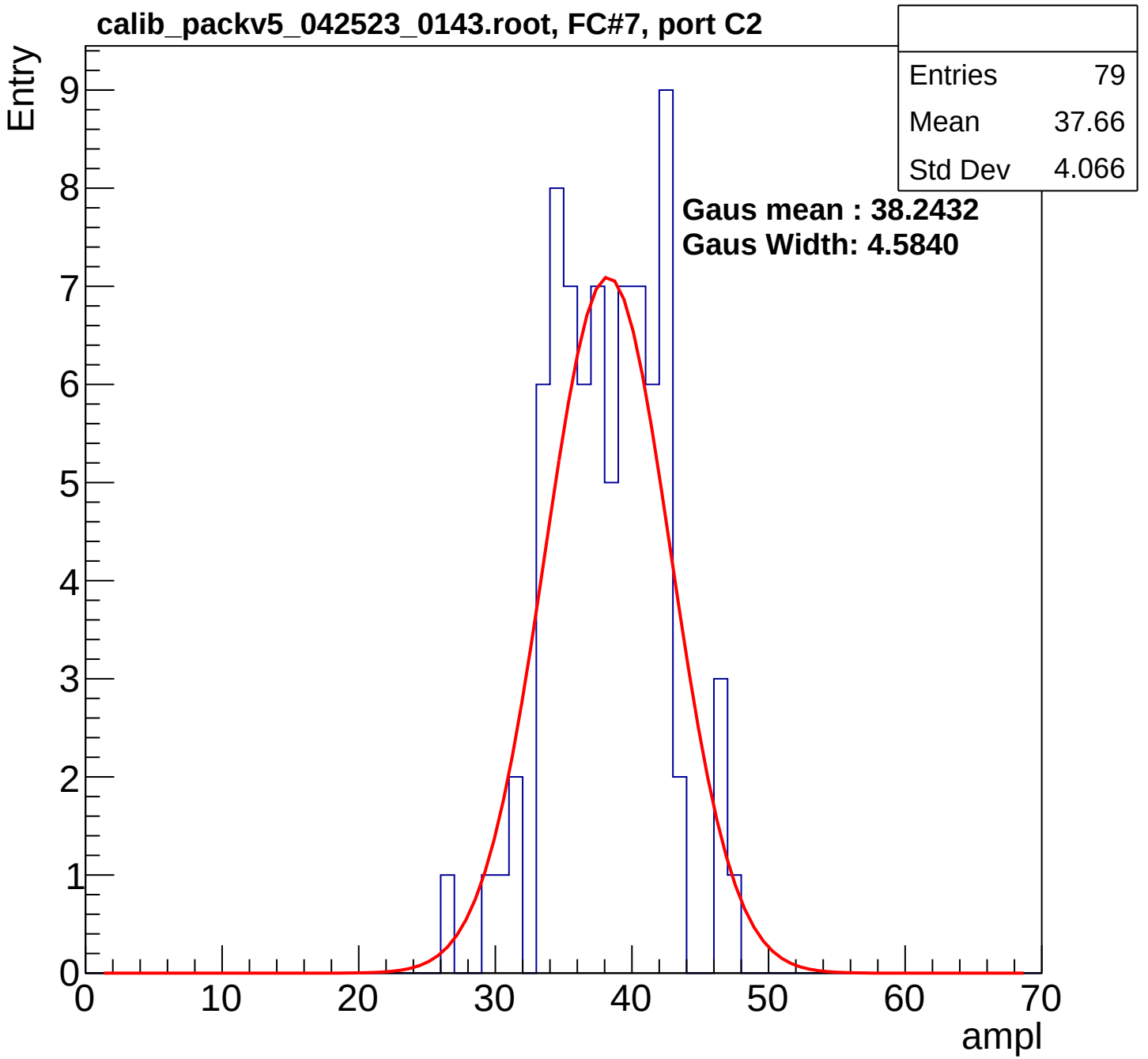
B1L103S, U18-ch93, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 79
Mean 37.66
Std Dev 4.066
Gaus mean : 38.2432
Gaus Width: 4.5840
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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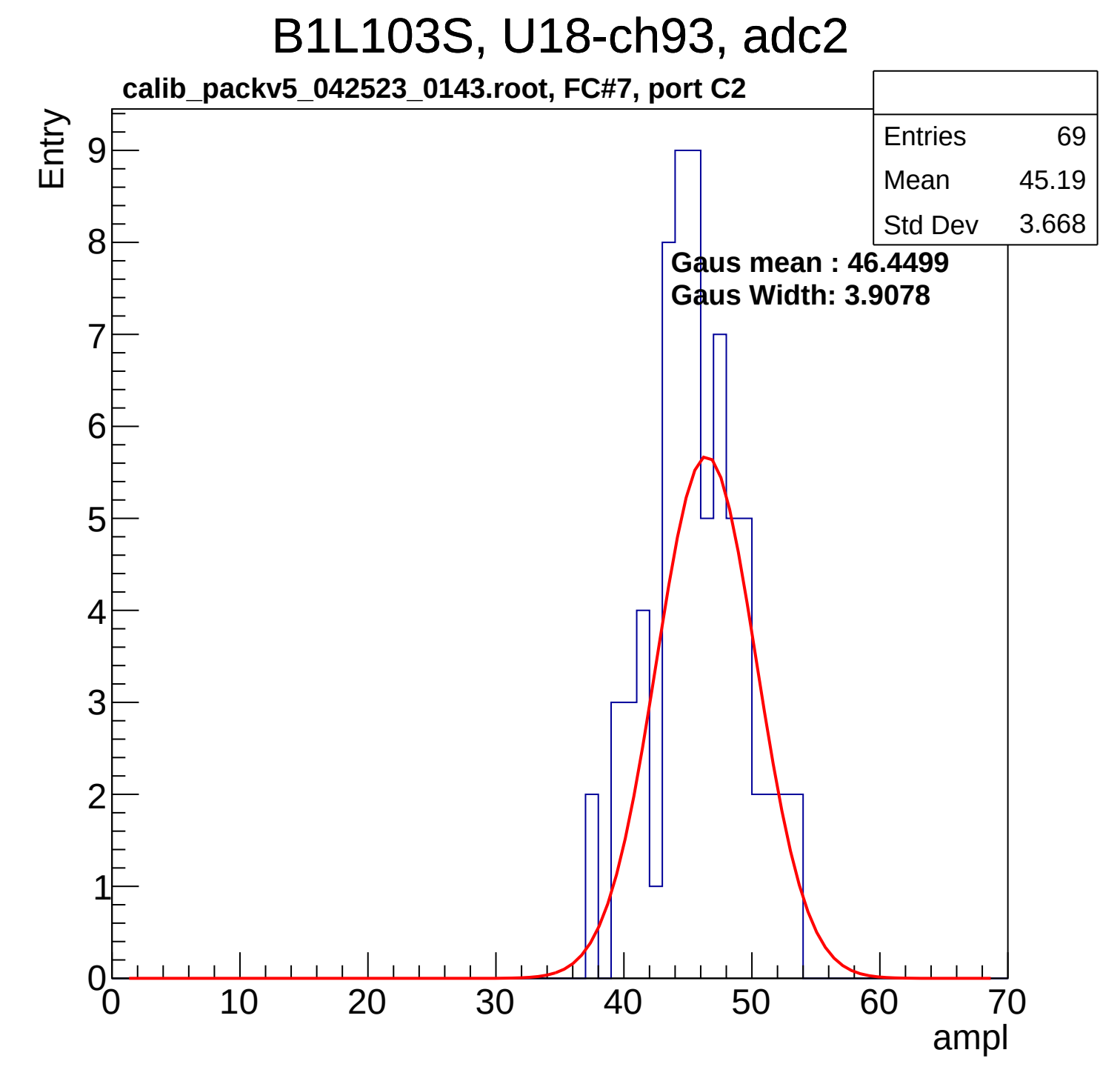
B1L103S, U18-ch93, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 45.19
Std Dev 3.668
Gaus mean : 46.4499
Gaus Width: 3.9078
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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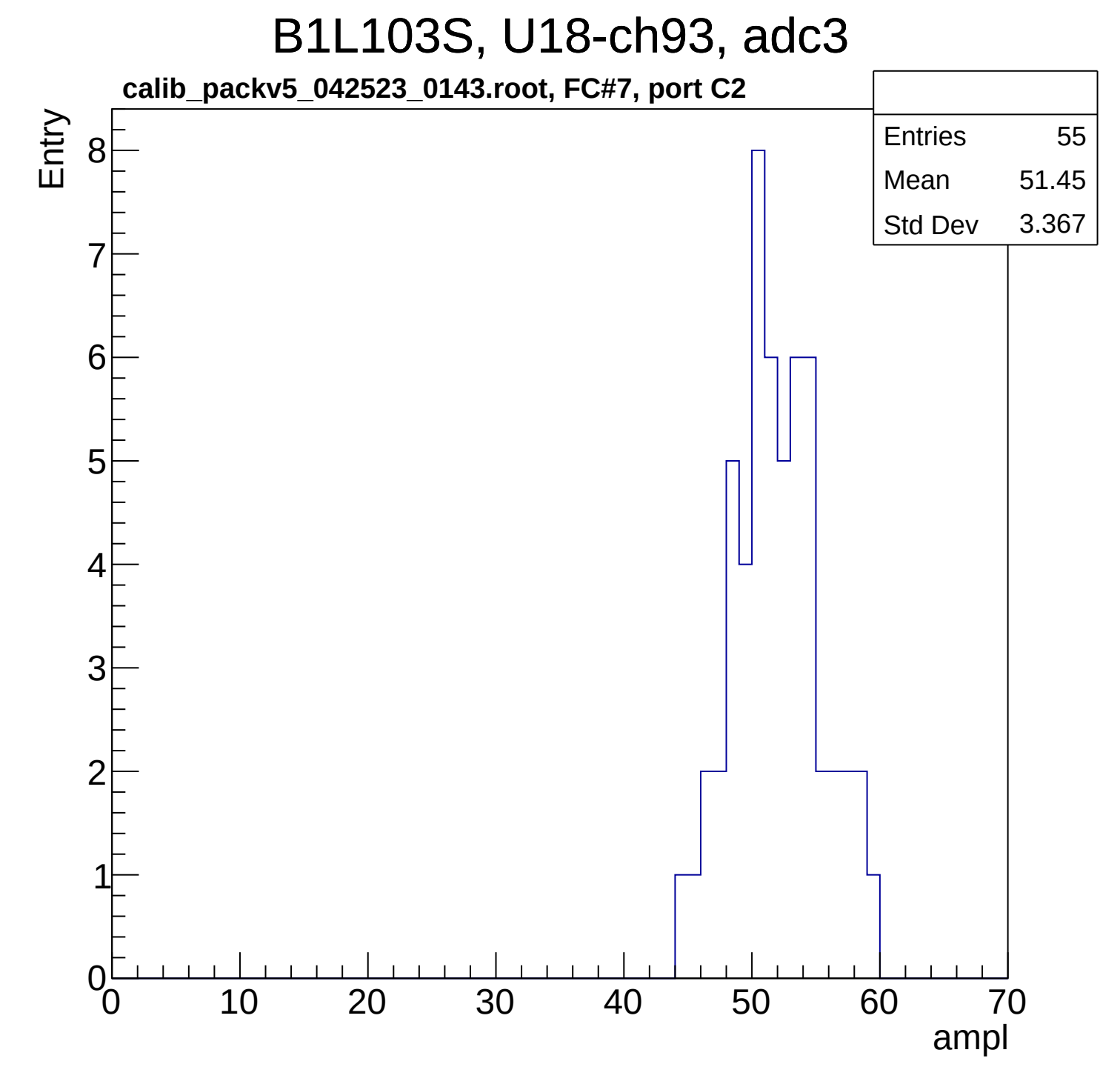
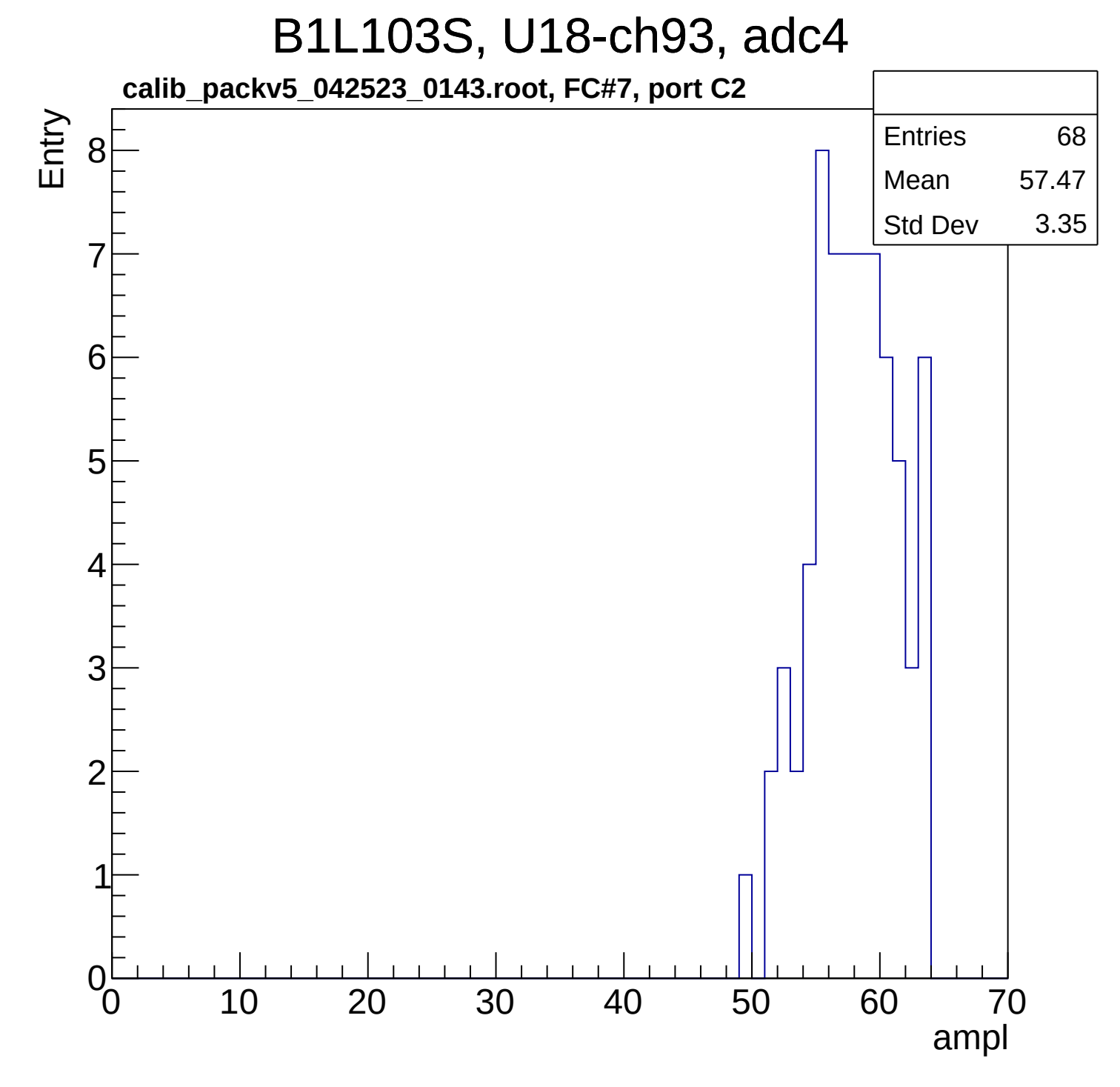

B1L103S, U18-ch93, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 51.45
Std Dev 3.367
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch93, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 57.47
Std Dev 3.35
Entry
ampl
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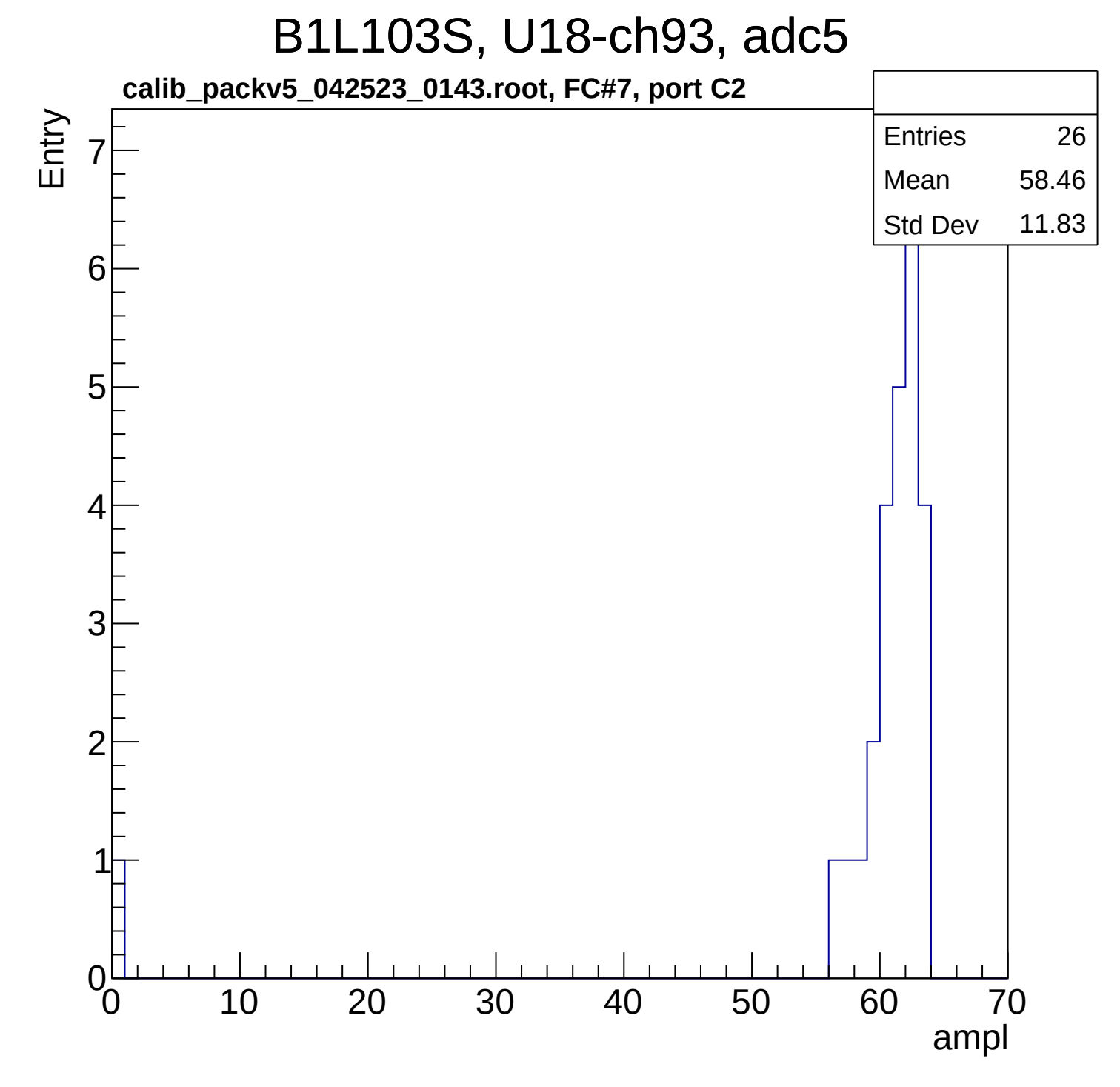
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch93, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 26
Mean 58.46
Std Dev 11.83
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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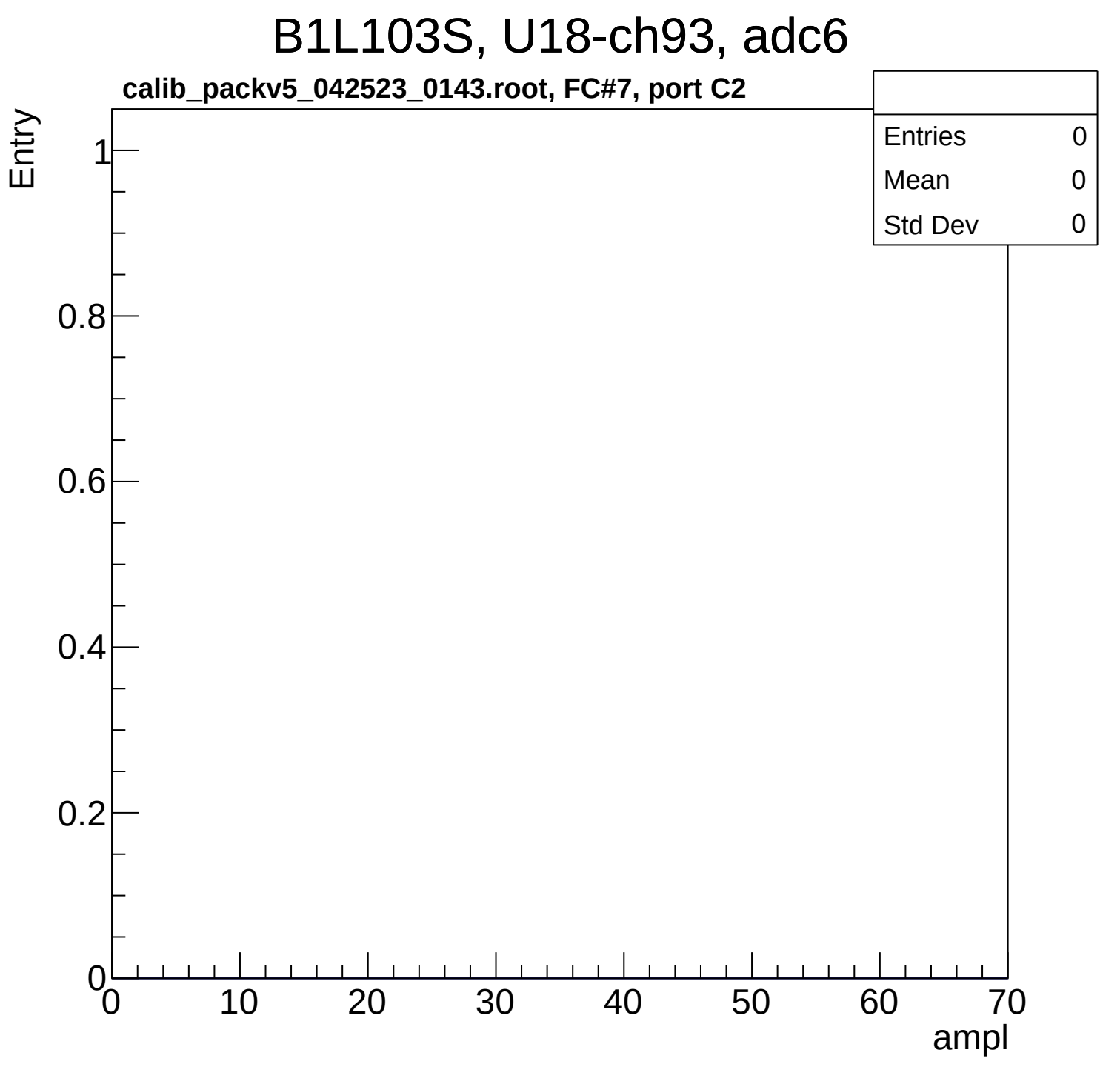
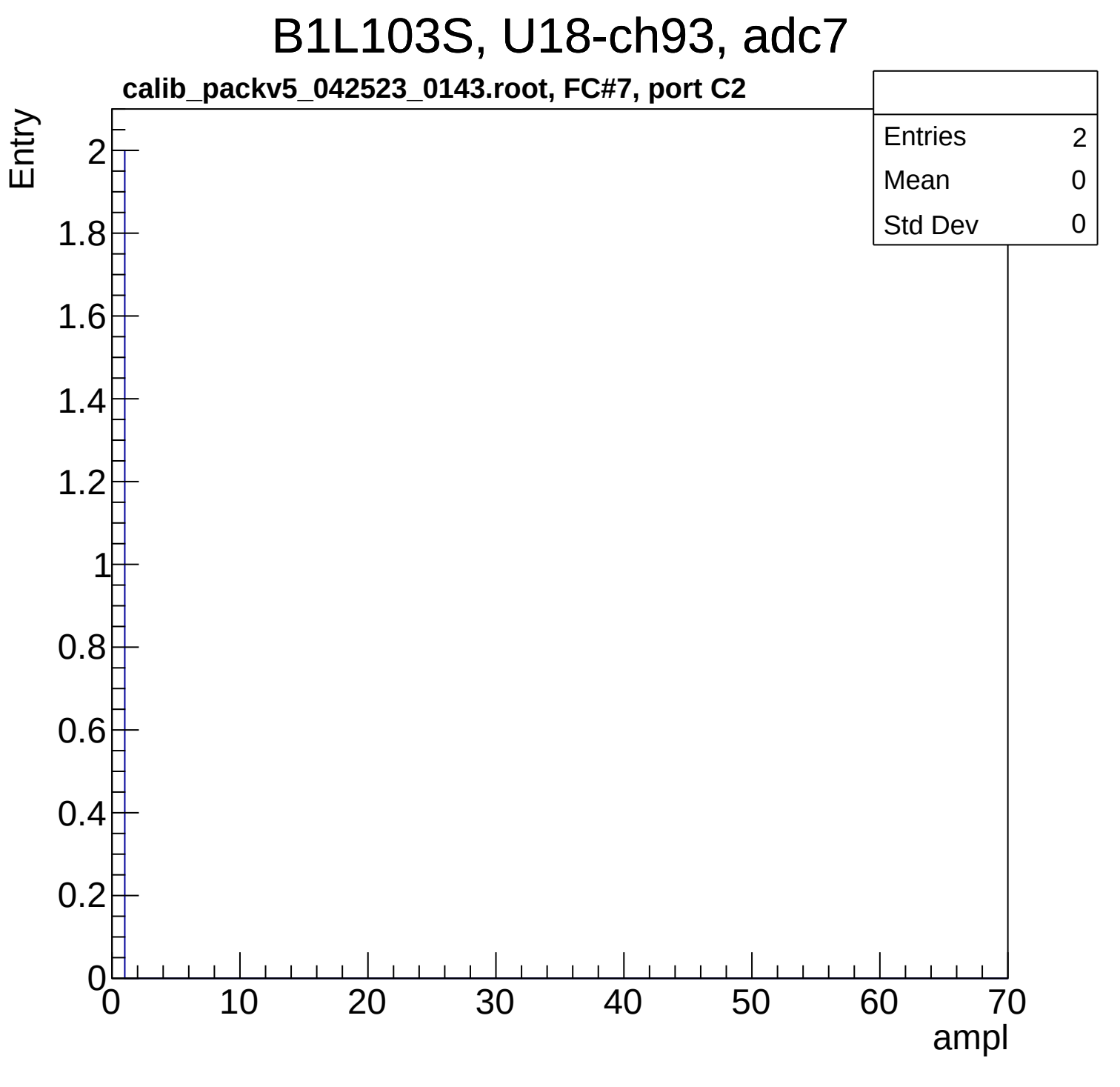
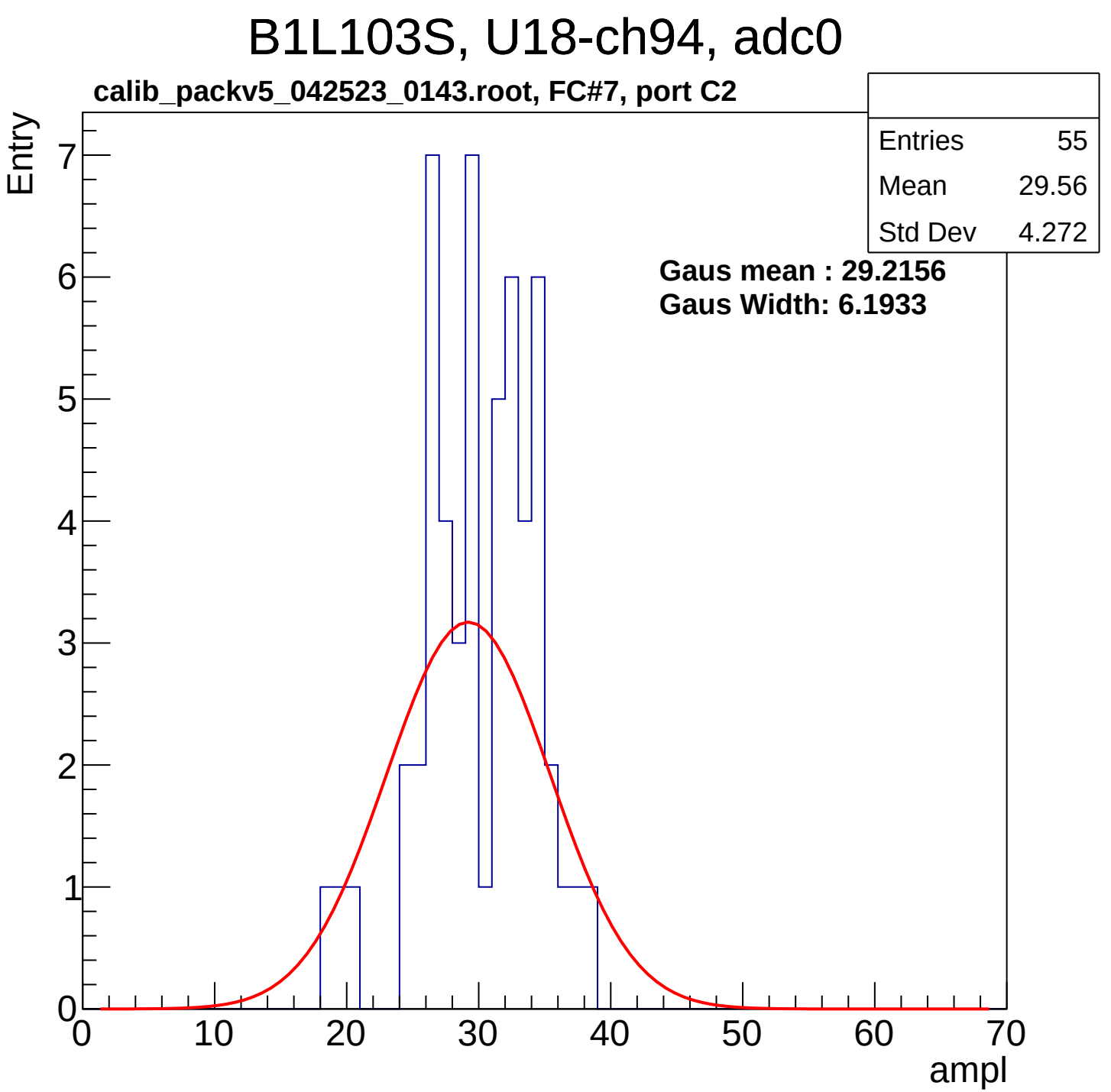
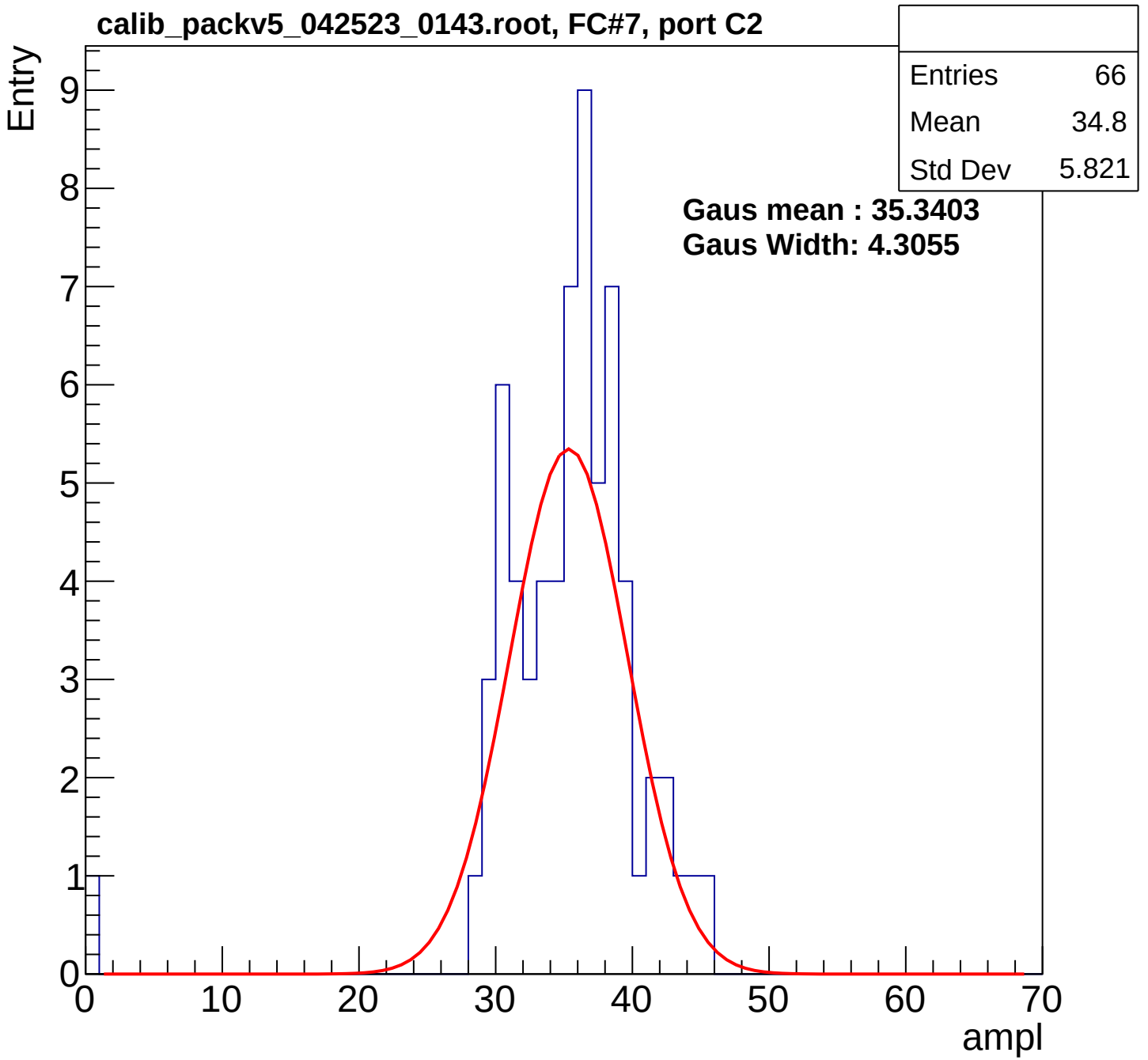

B1L103S, U18-ch93, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch93, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch94, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 29.56
Std Dev 4.272
Gaus mean : 29.2156
Gaus Width: 6.1933
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch94, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 34.8
Std Dev 5.821
Gaus mean : 35.3403
Gaus Width: 4.3055
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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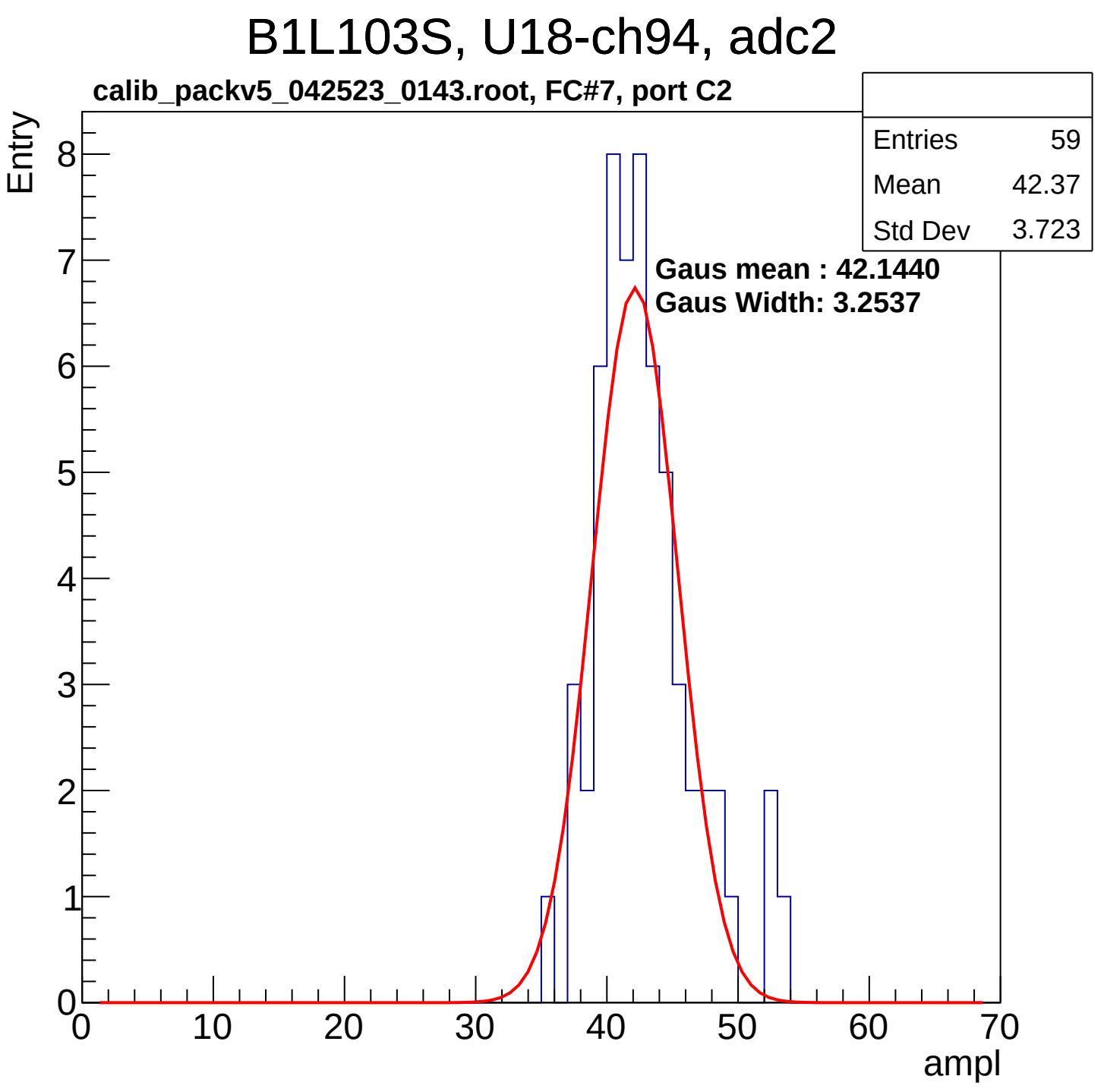
B1L103S, U18-ch94, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 42.37
Std Dev 3.723
Gaus mean : 42.1440
Gaus Width: 3.2537
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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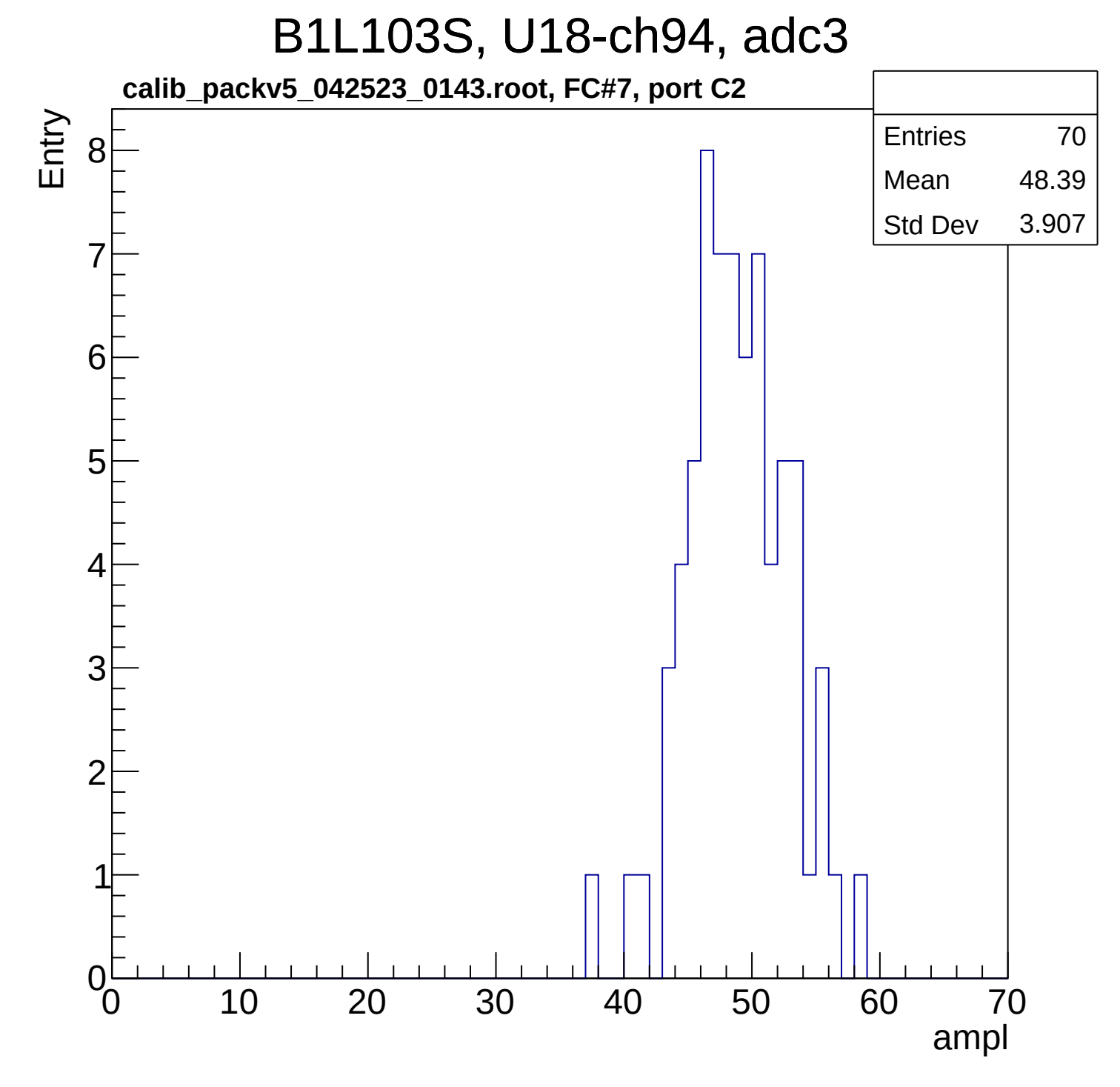
B1L103S, U18-ch94, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 48.39
Std Dev 3.907
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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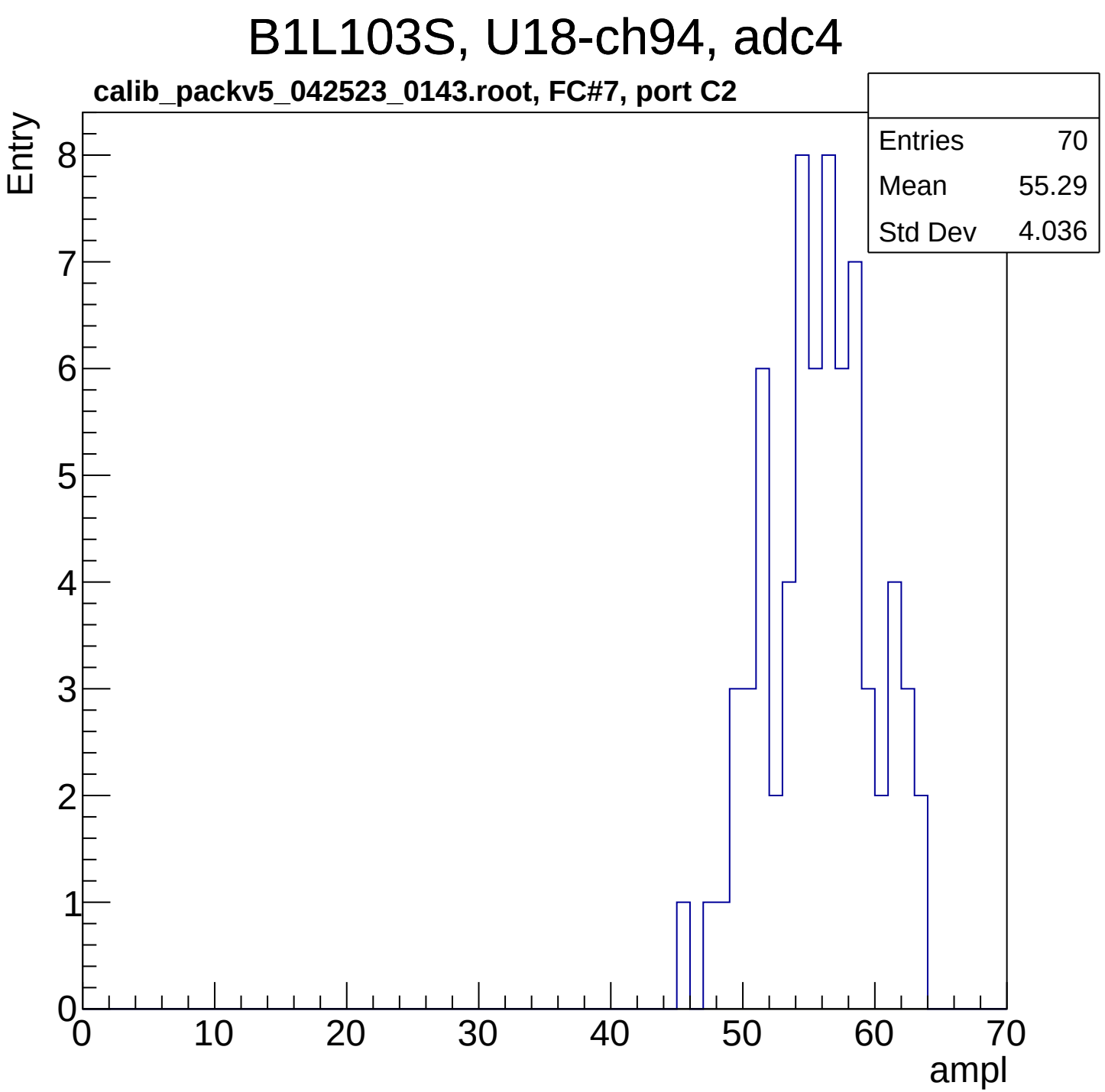
B1L103S, U18-ch94, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 55.29
Std Dev 4.036
Entry
ampl
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1
2
3
4
5
6
7
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0
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20
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40
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60
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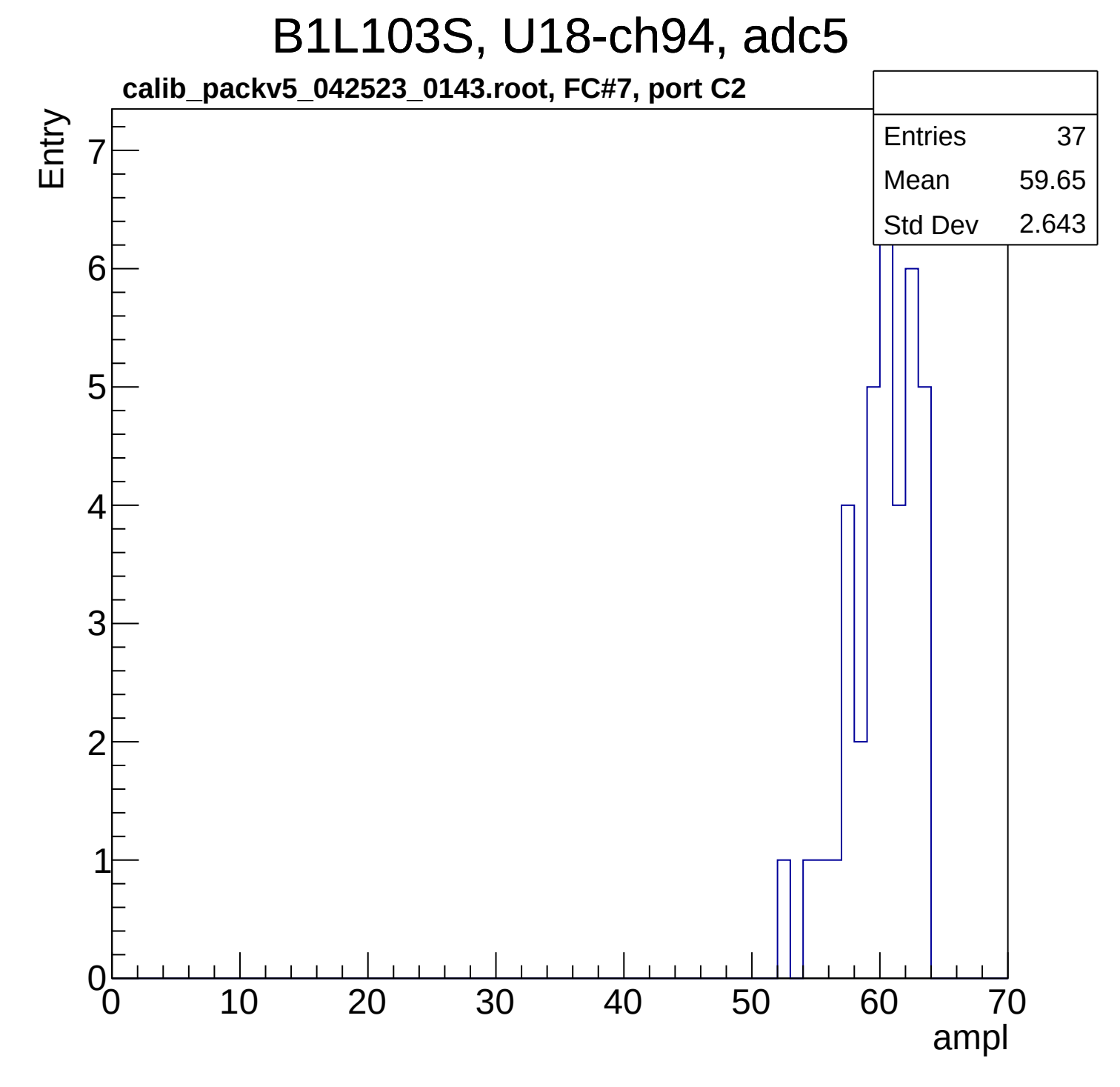
B1L103S, U18-ch94, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 37
Mean 59.65
Std Dev 2.643
Entry
ampl
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1
2
3
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0
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60
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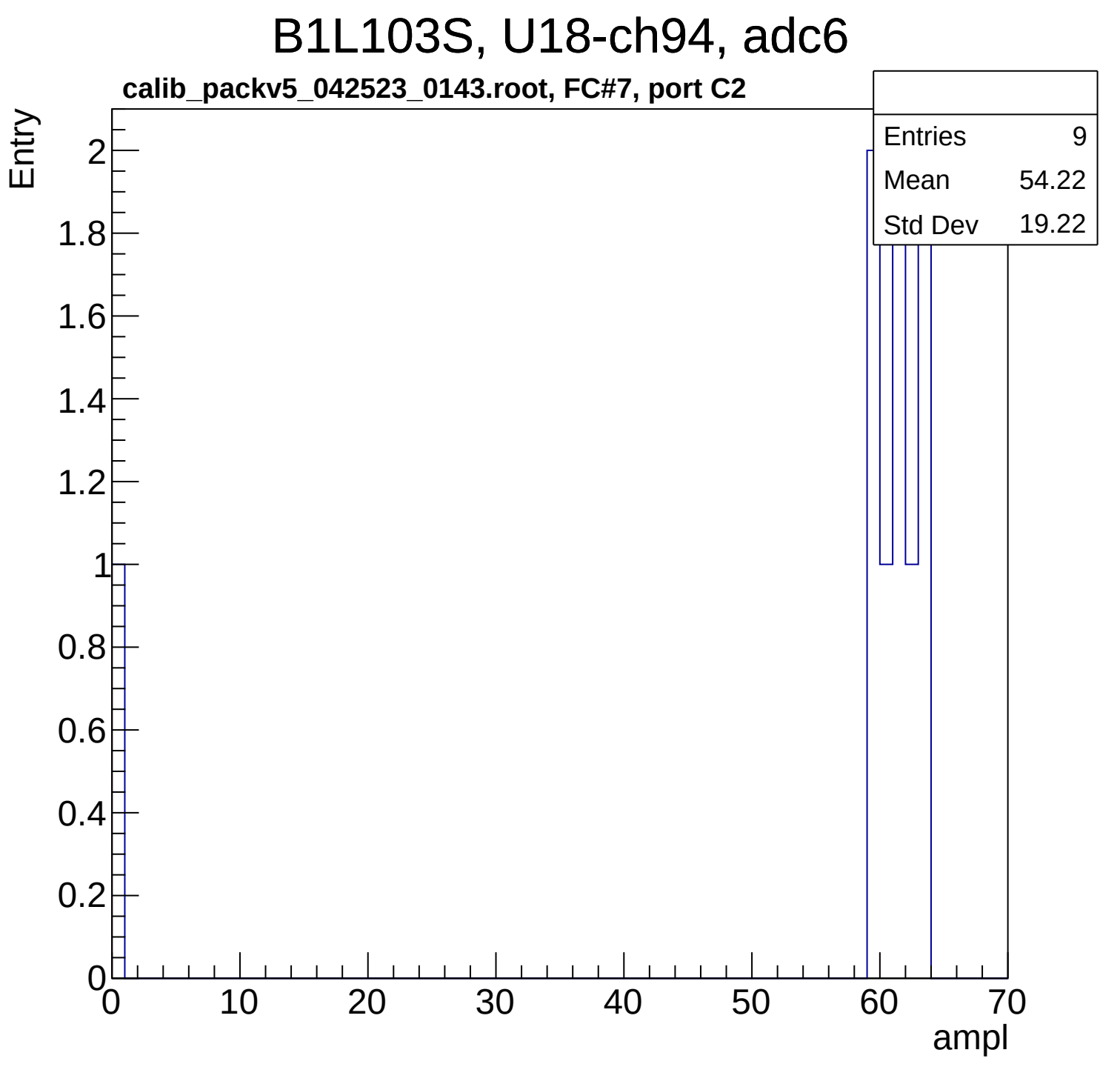
B1L103S, U18-ch94, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 9
Mean 54.22
Std Dev 19.22
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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40
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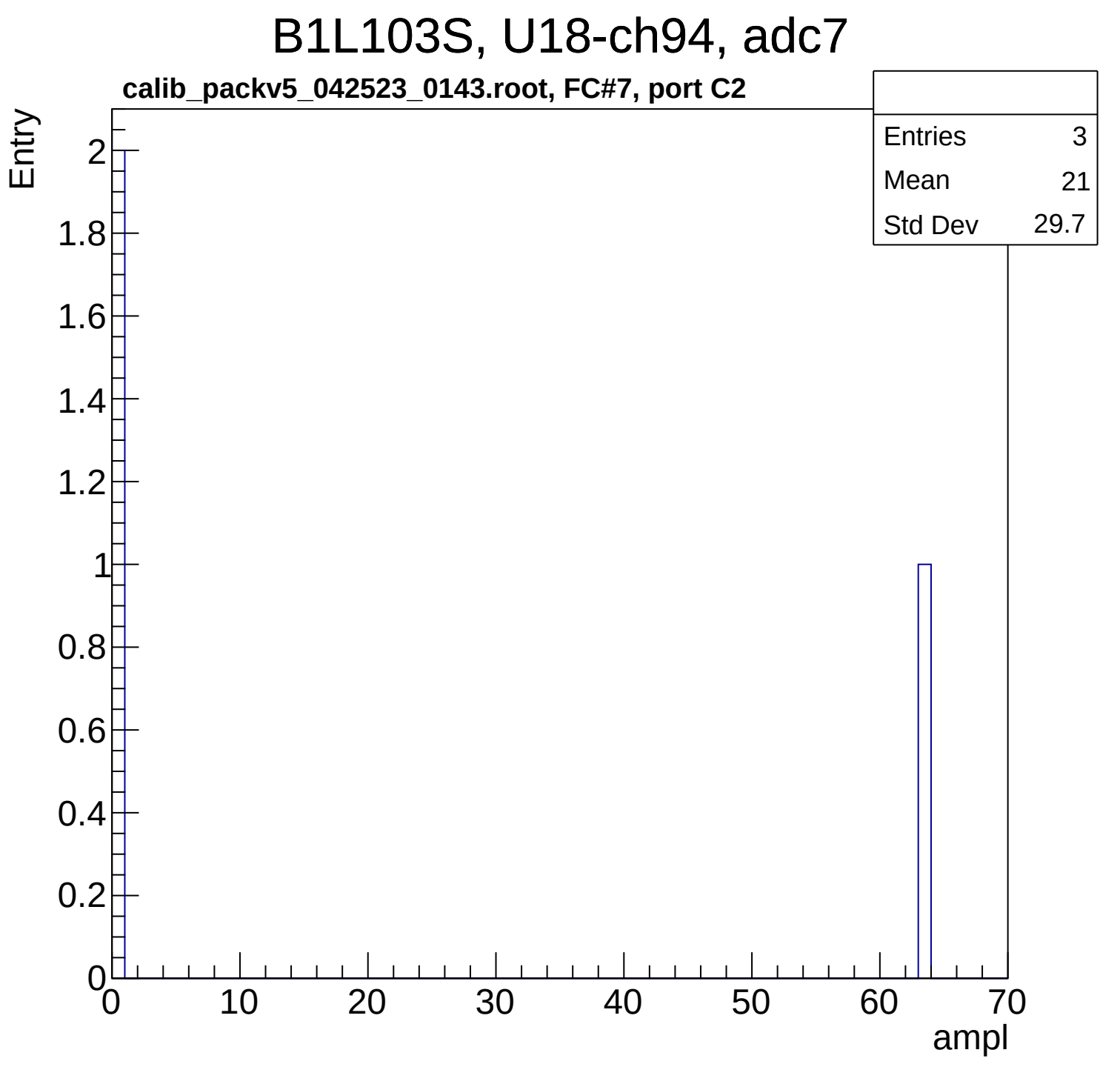
60
70


B1L103S, U18-ch94, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 21
Std Dev 29.7
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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20
30
40
50
60
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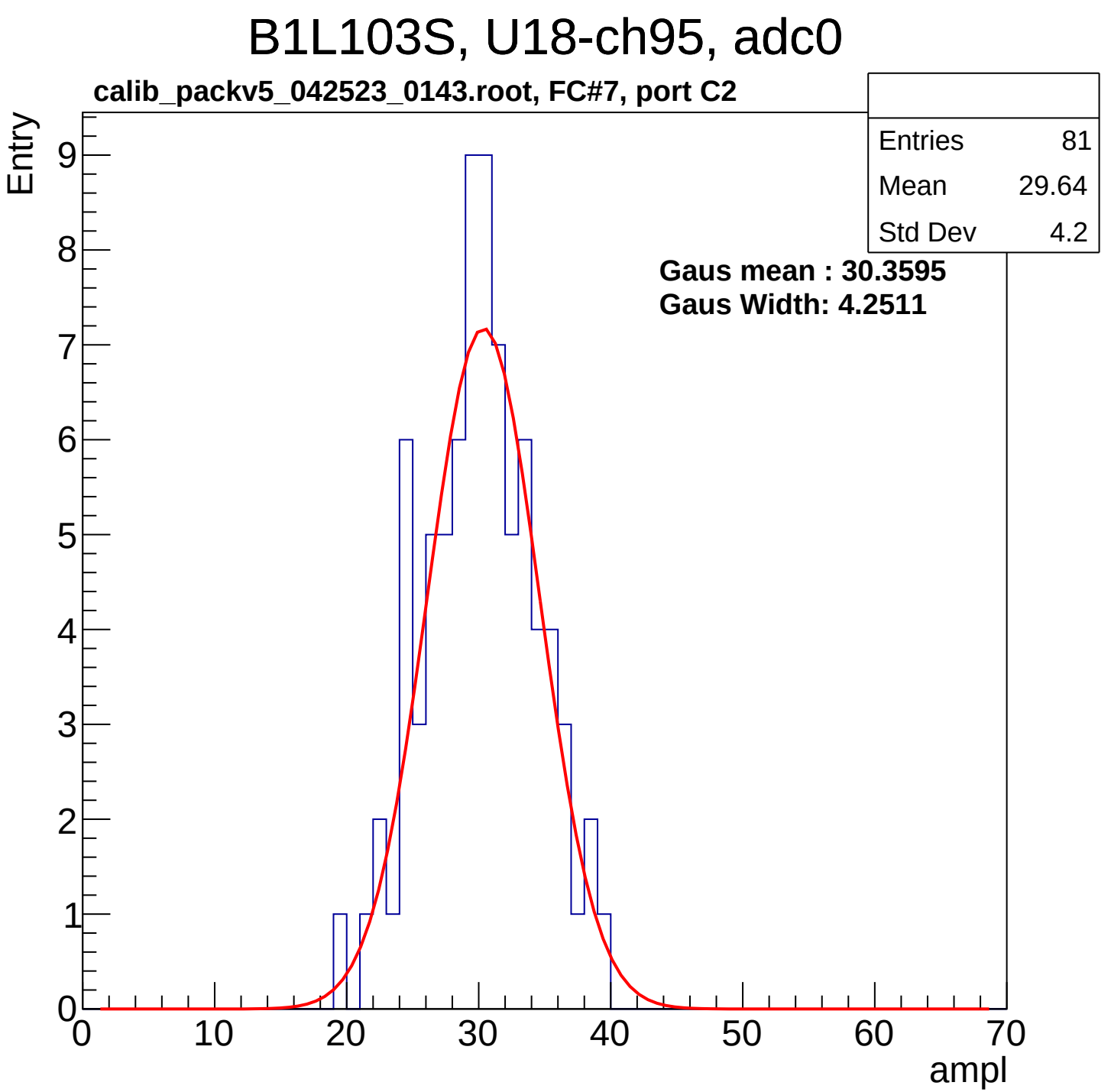
B1L103S, U18-ch95, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 81
Mean 29.64
Std Dev 4.2
Gaus mean : 30.3595
Gaus Width: 4.2511
Entry
ampl
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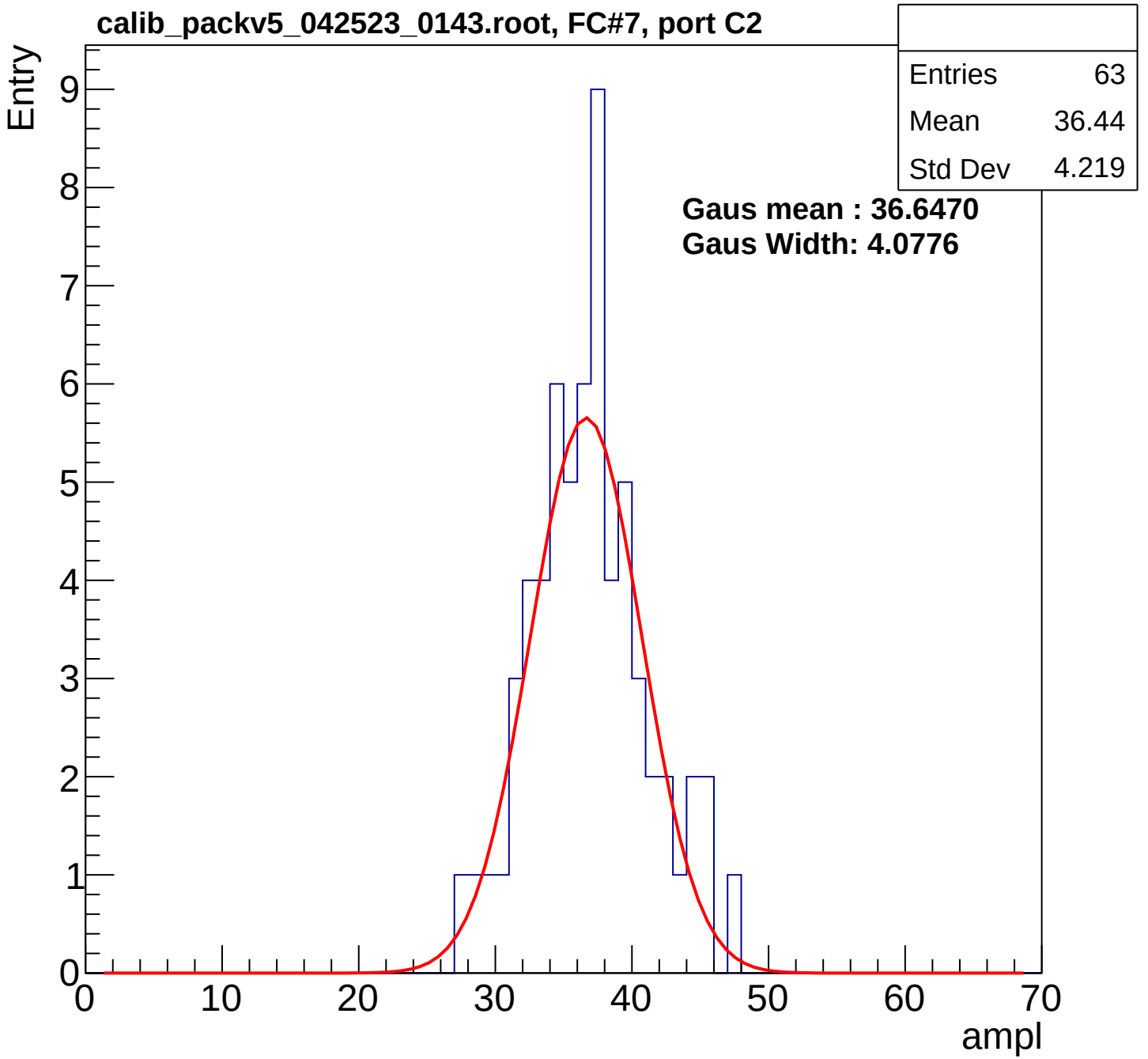
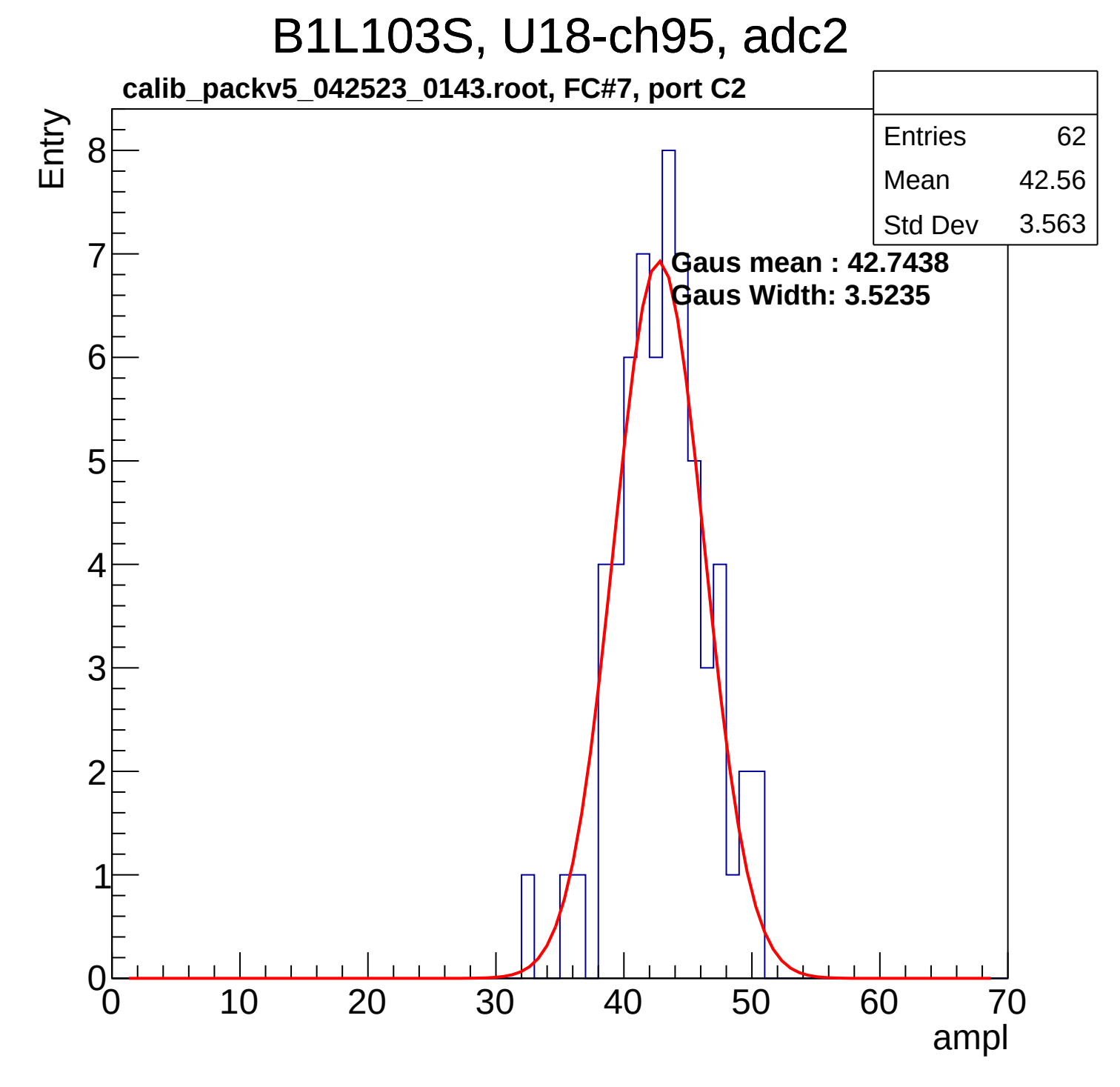
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch95, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 36.44
Std Dev 4.219
Gaus mean : 36.6470
Gaus Width: 4.0776
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch95, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 62
Mean 42.56
Std Dev 3.563
Gaus mean : 42.7438
Gaus Width: 3.5235
Entry
ampl
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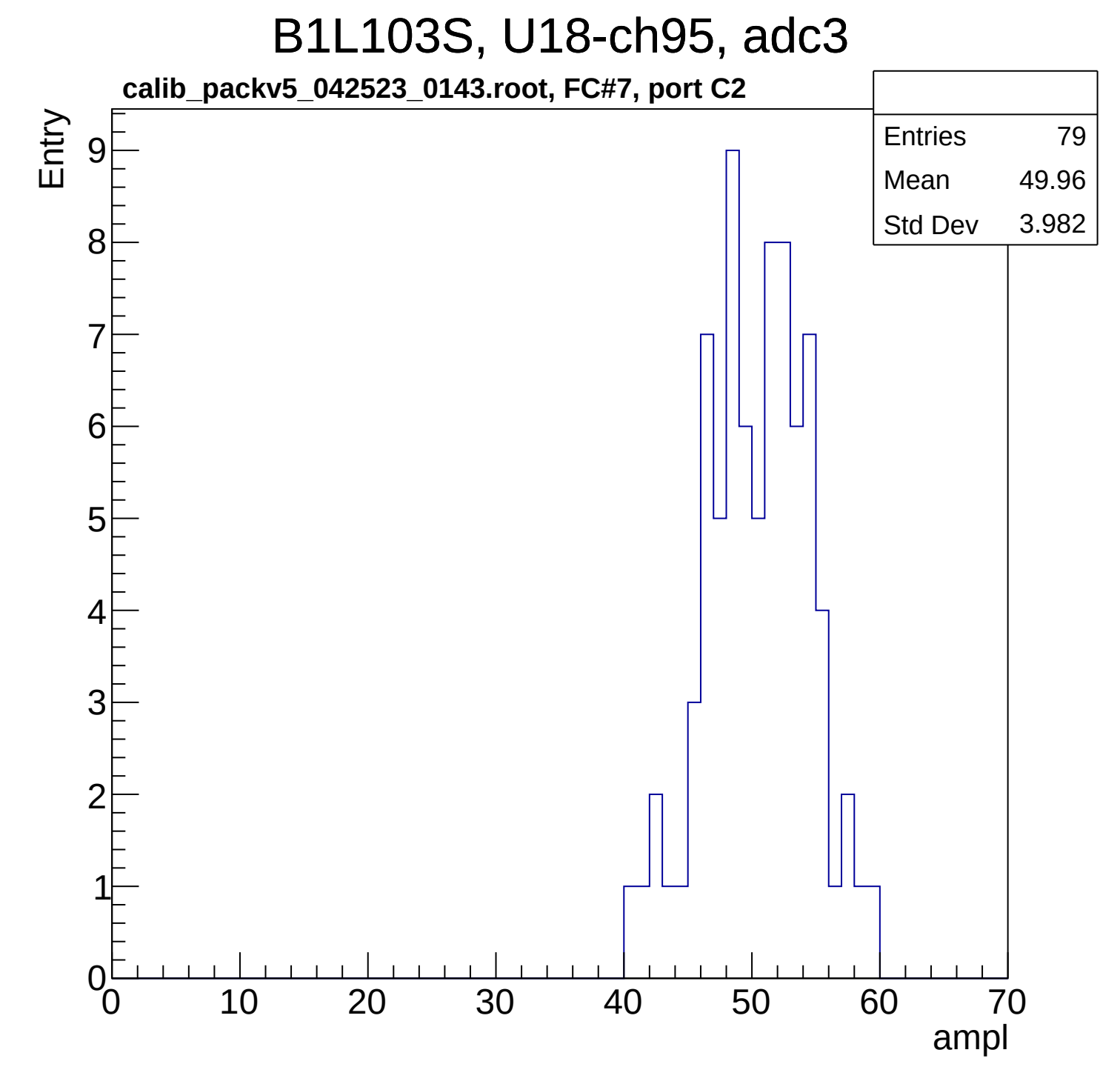
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch95, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 79
Mean 49.96
Std Dev 3.982
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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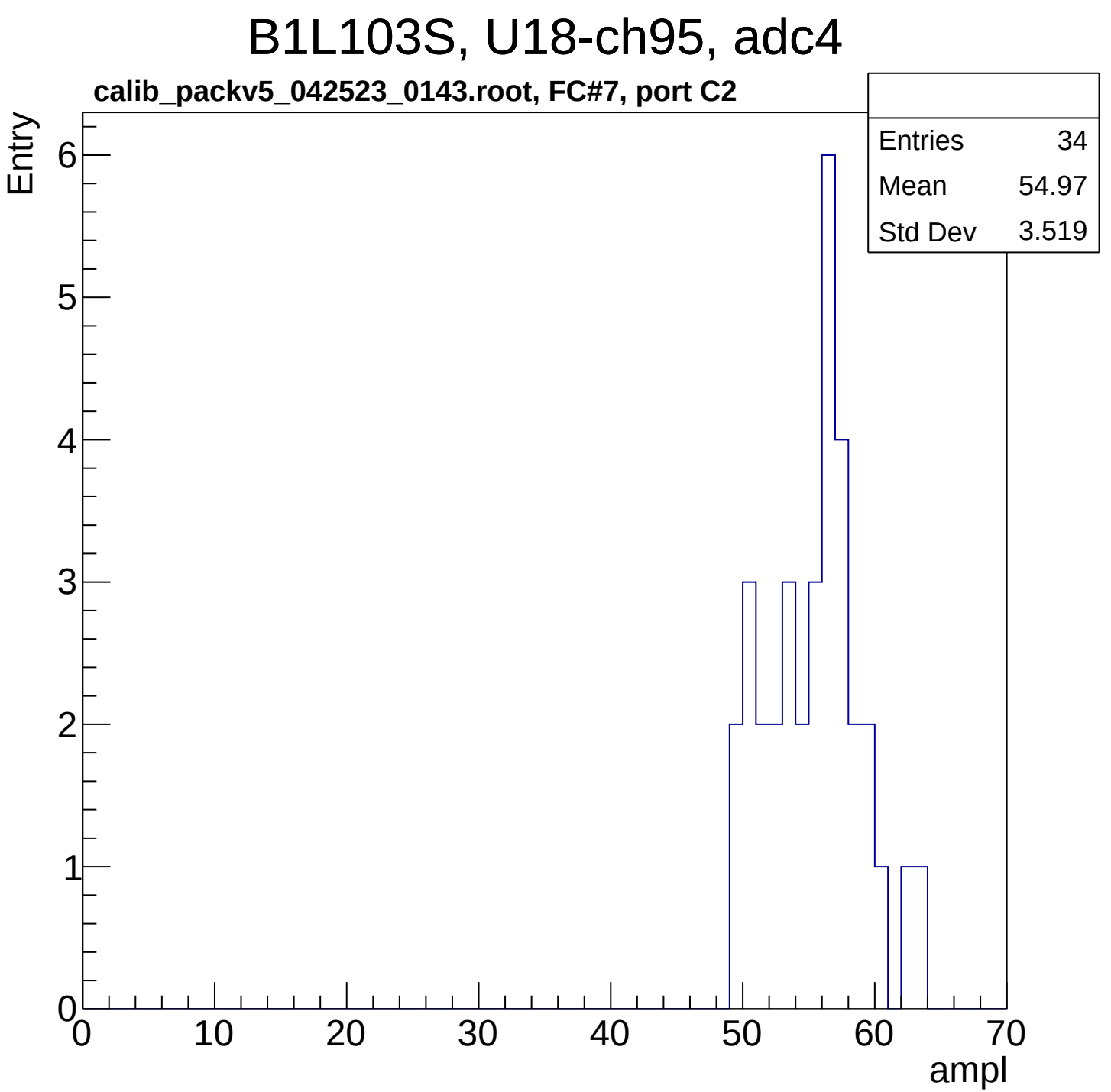
B1L103S, U18-ch95, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 34
Mean 54.97
Std Dev 3.519
Entry
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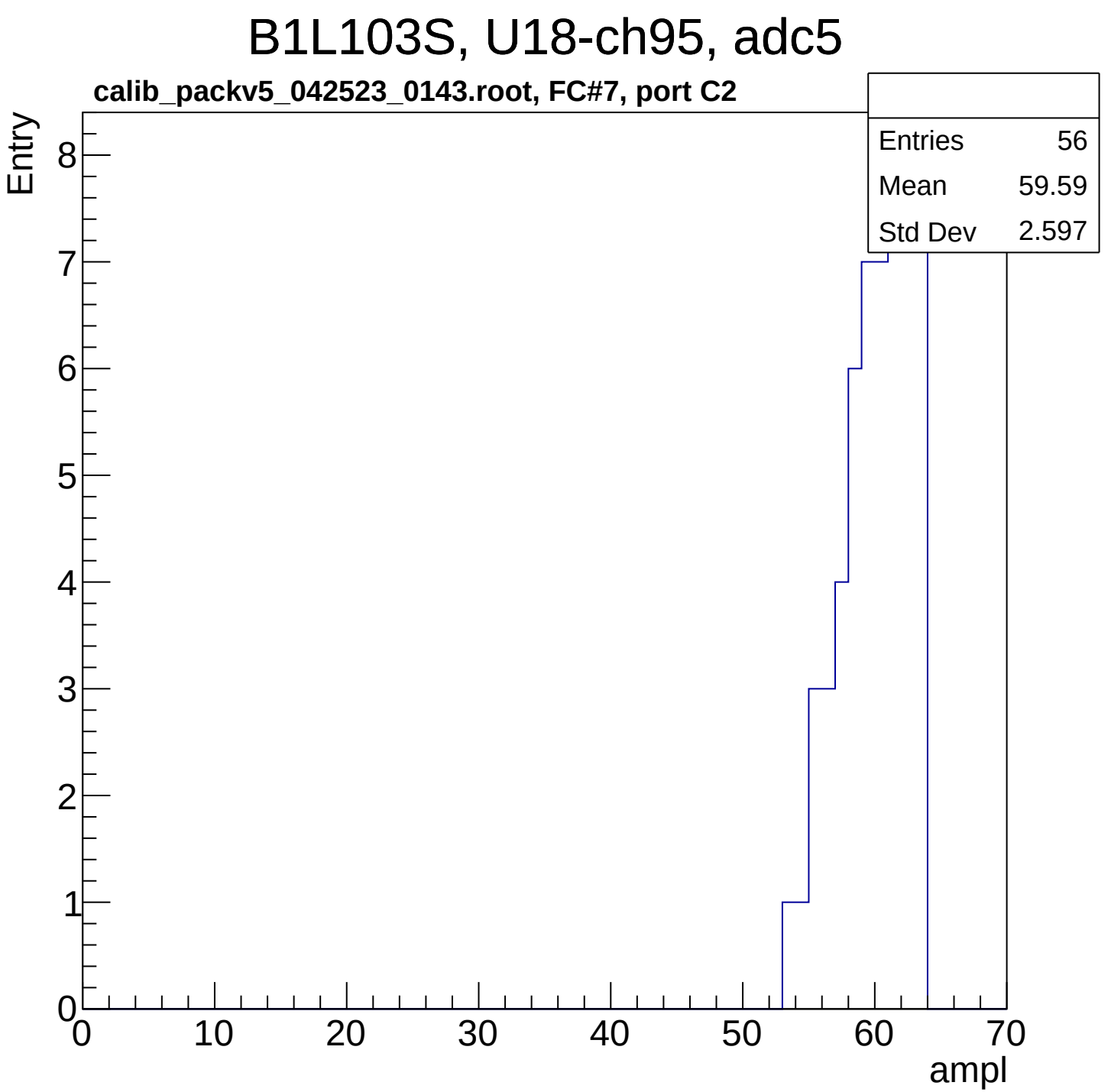
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch95, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 59.59
Std Dev 2.597
Entry
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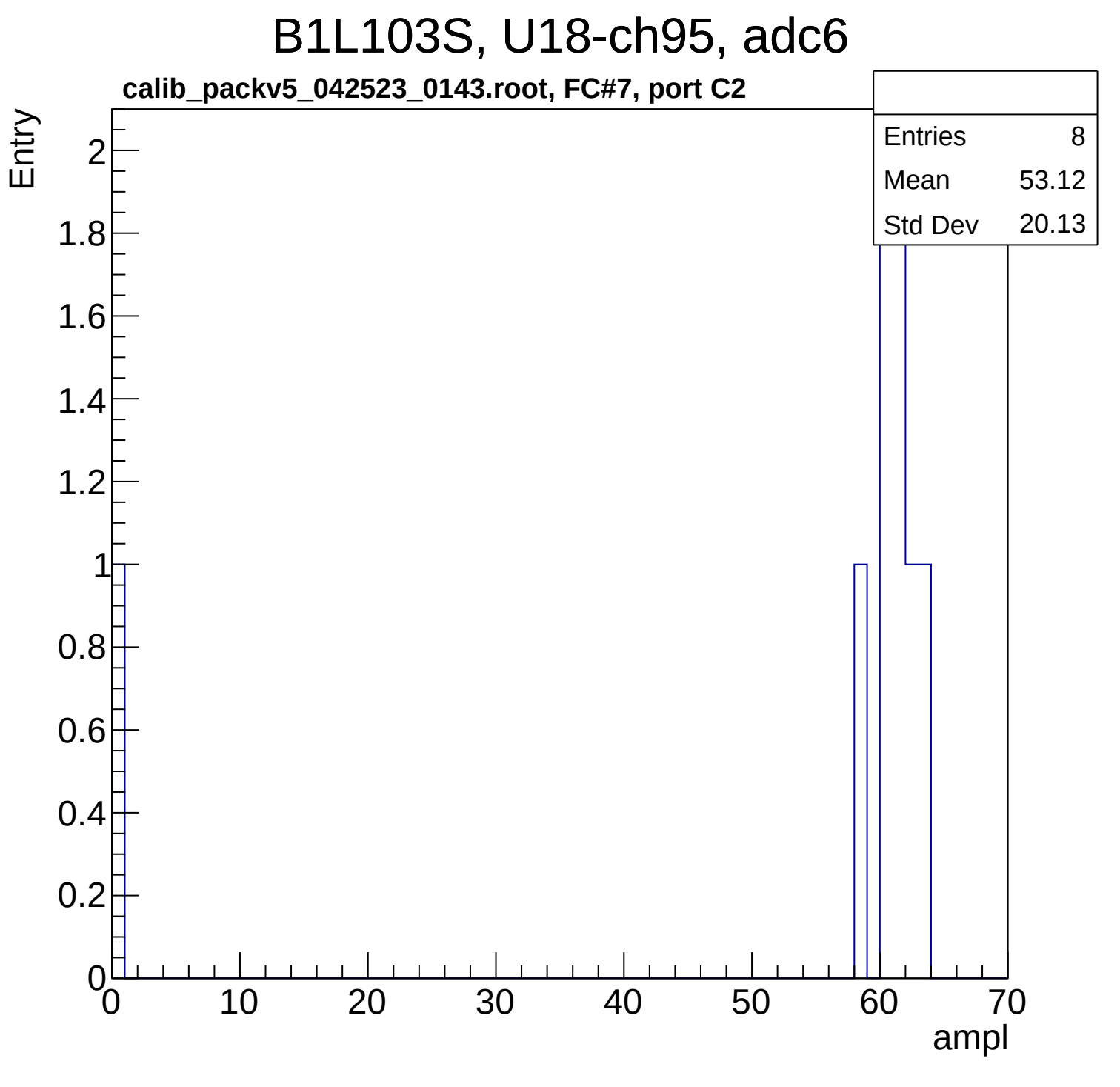
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch95, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 8
Mean 53.12
Std Dev 20.13
Entry
ampl
0
0.2
0.4
0.6
0.8
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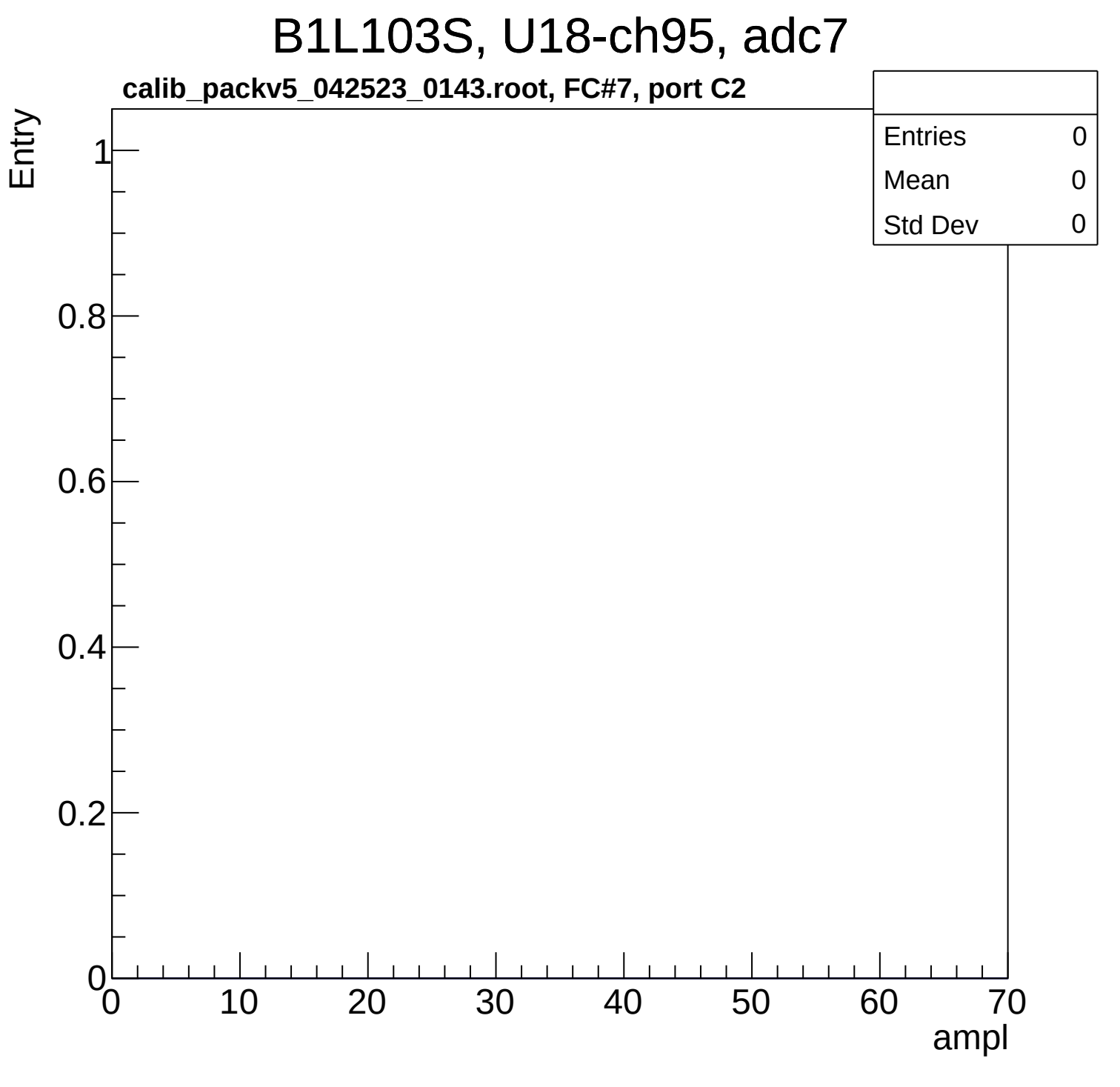
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U18-ch95, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
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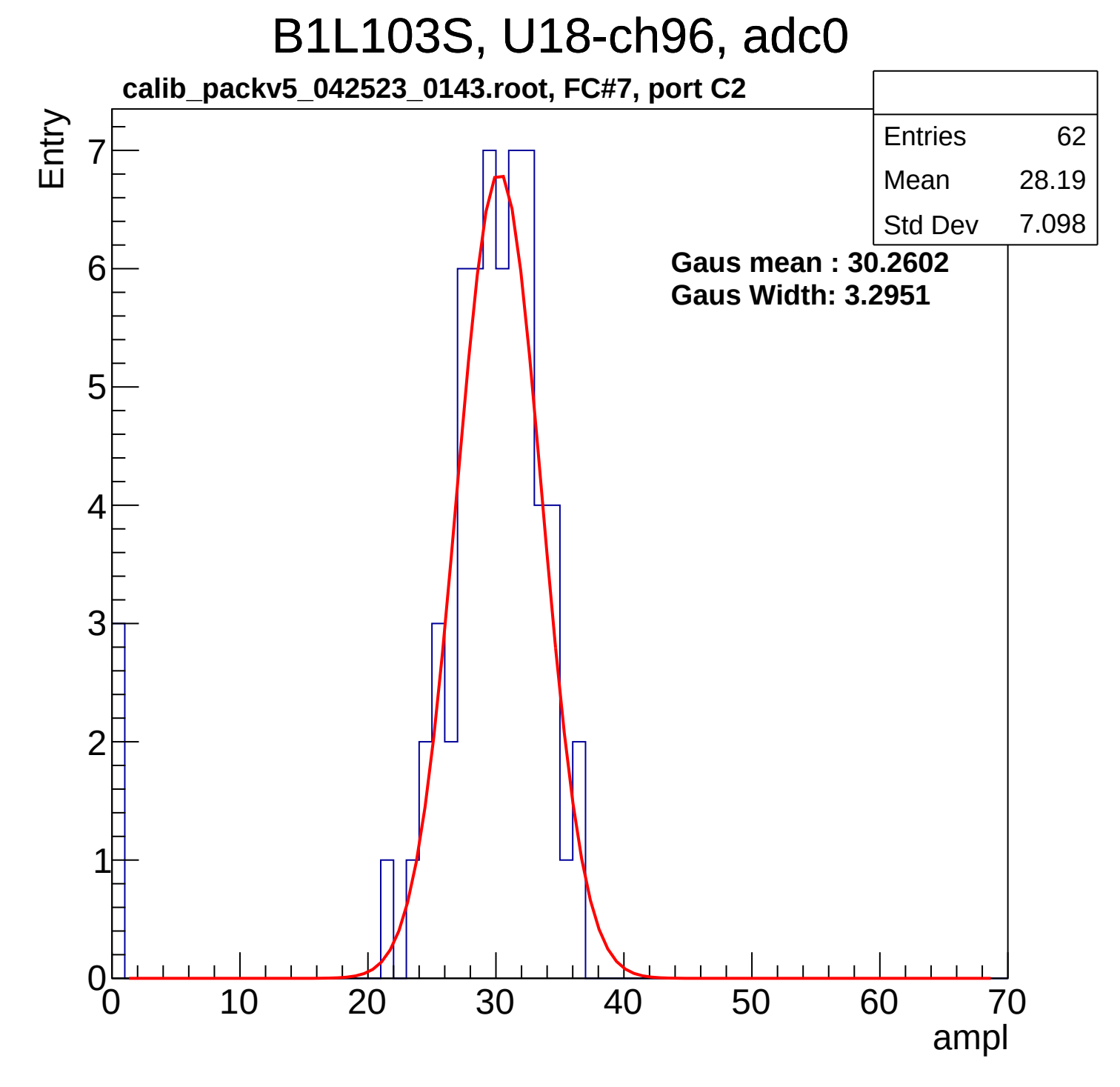
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch96, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 62
Mean 28.19
Std Dev 7.098
Gaus mean : 30.2602
Gaus Width: 3.2951
Entry
ampl
0
1
2
3
4
5
6
7
0
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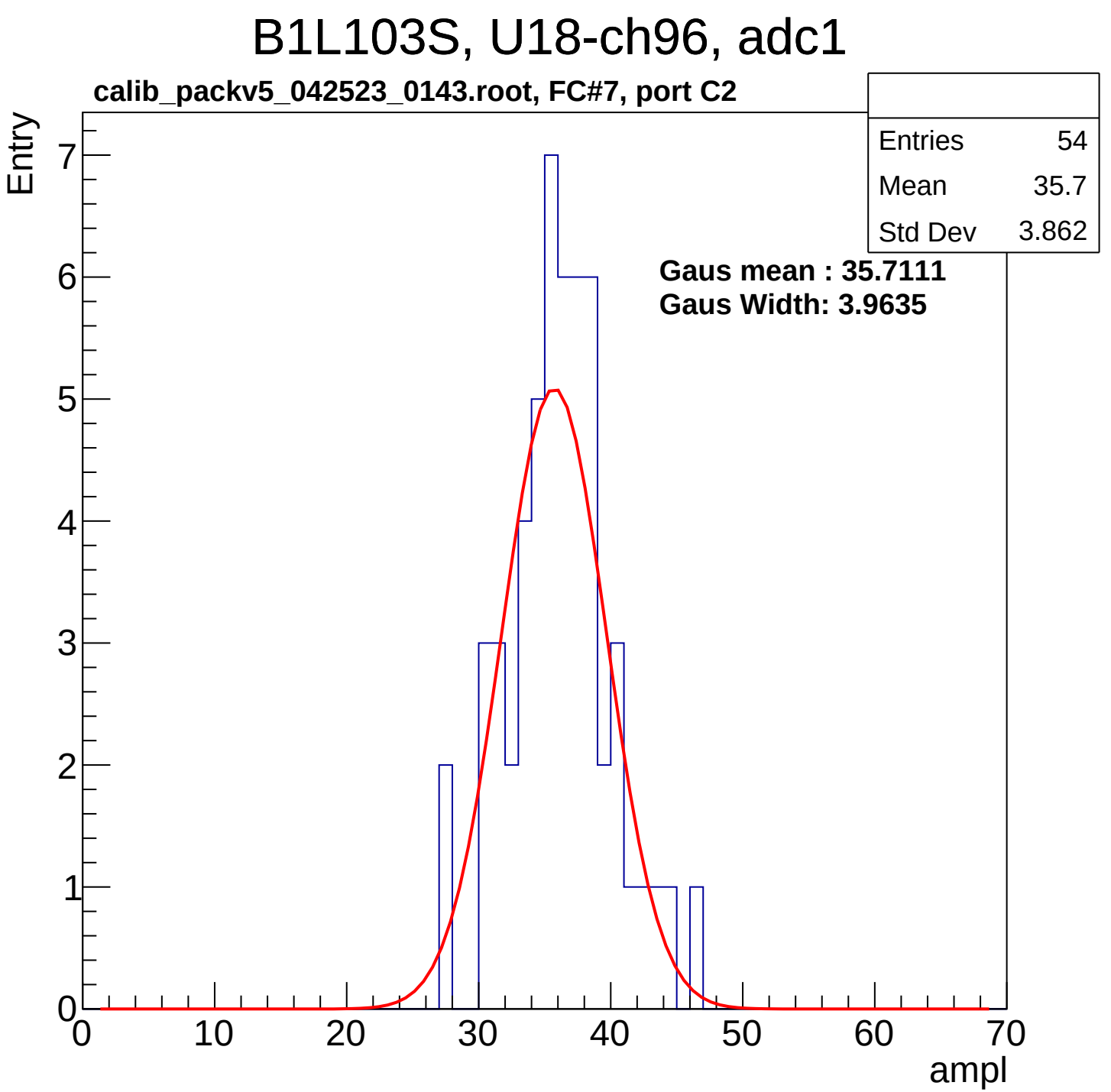
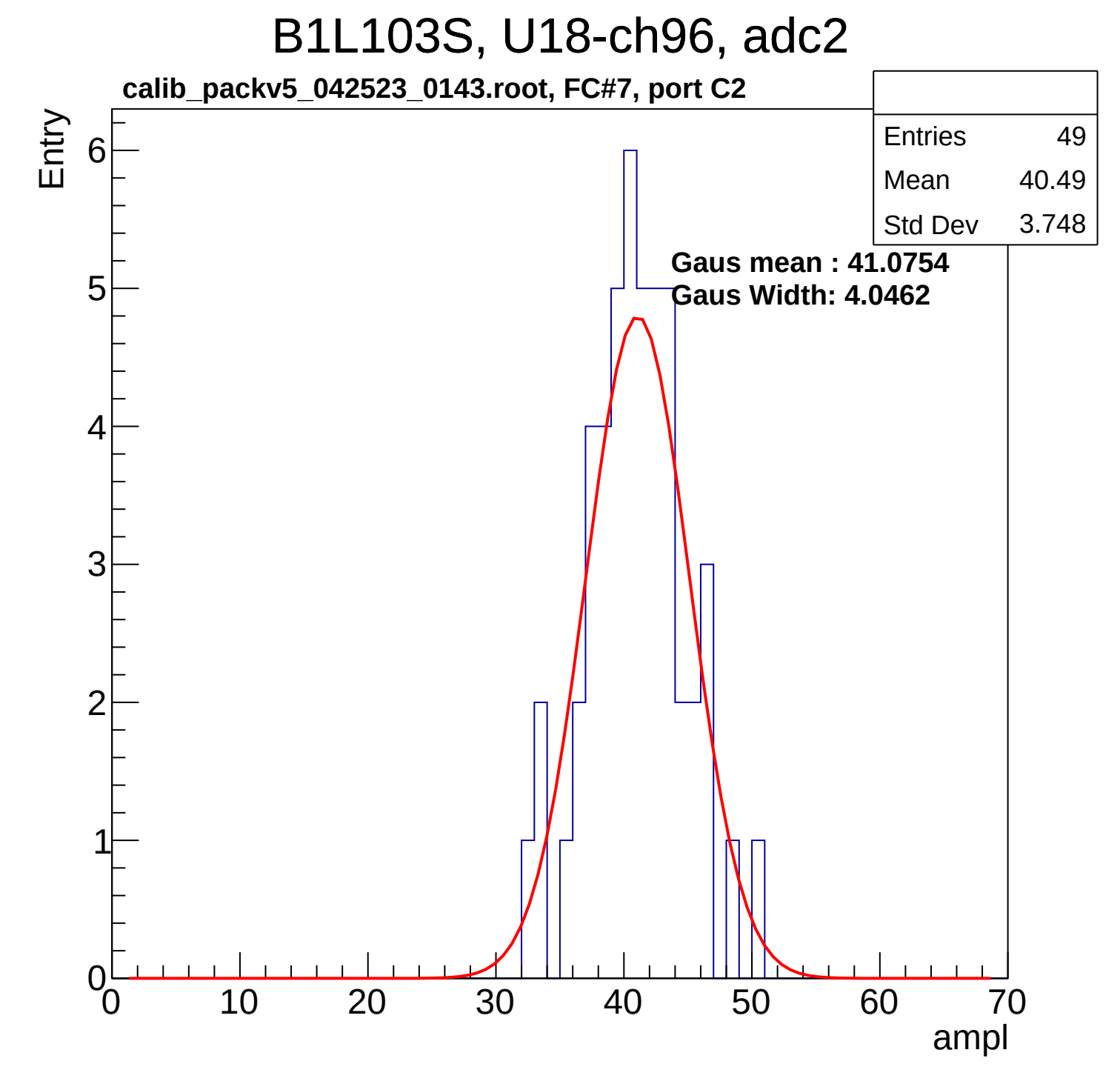

B1L103S, U18-ch96, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 54
Mean 35.7
Std Dev 3.862
Gaus mean : 35.7111
Gaus Width: 3.9635
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch96, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 49
Mean 40.49
Std Dev 3.748
Gaus mean : 41.0754
Gaus Width: 4.0462
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
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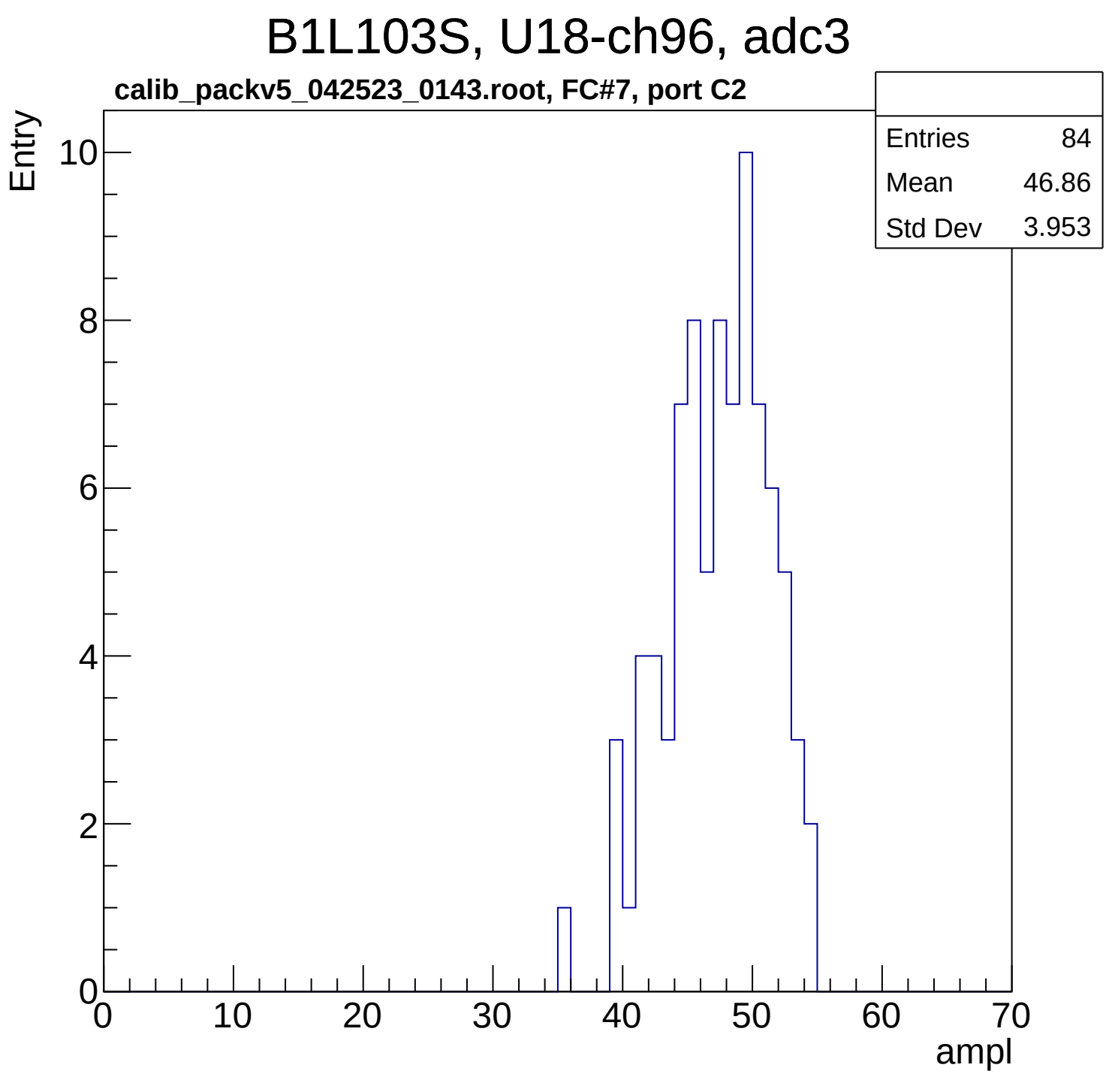
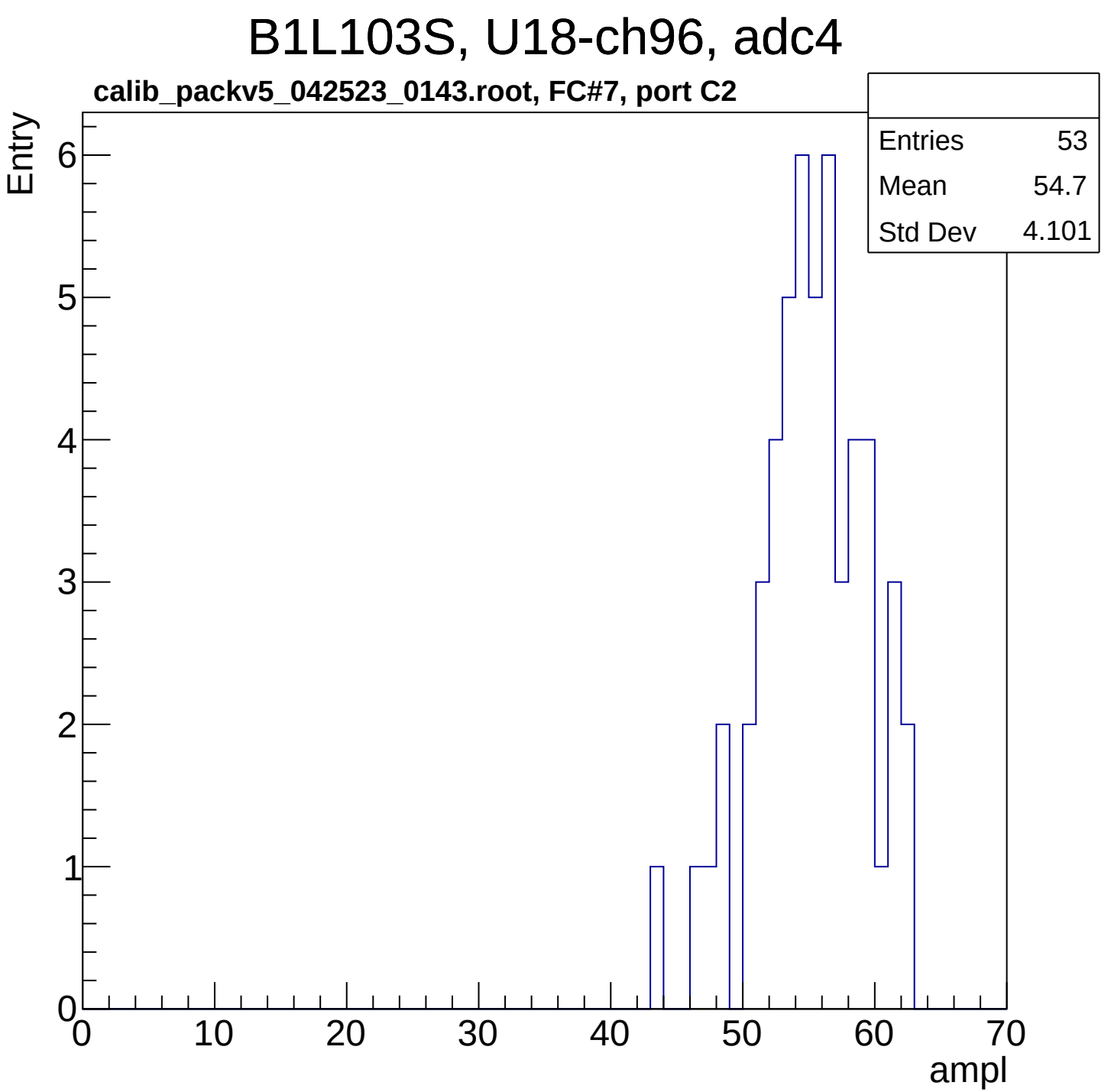
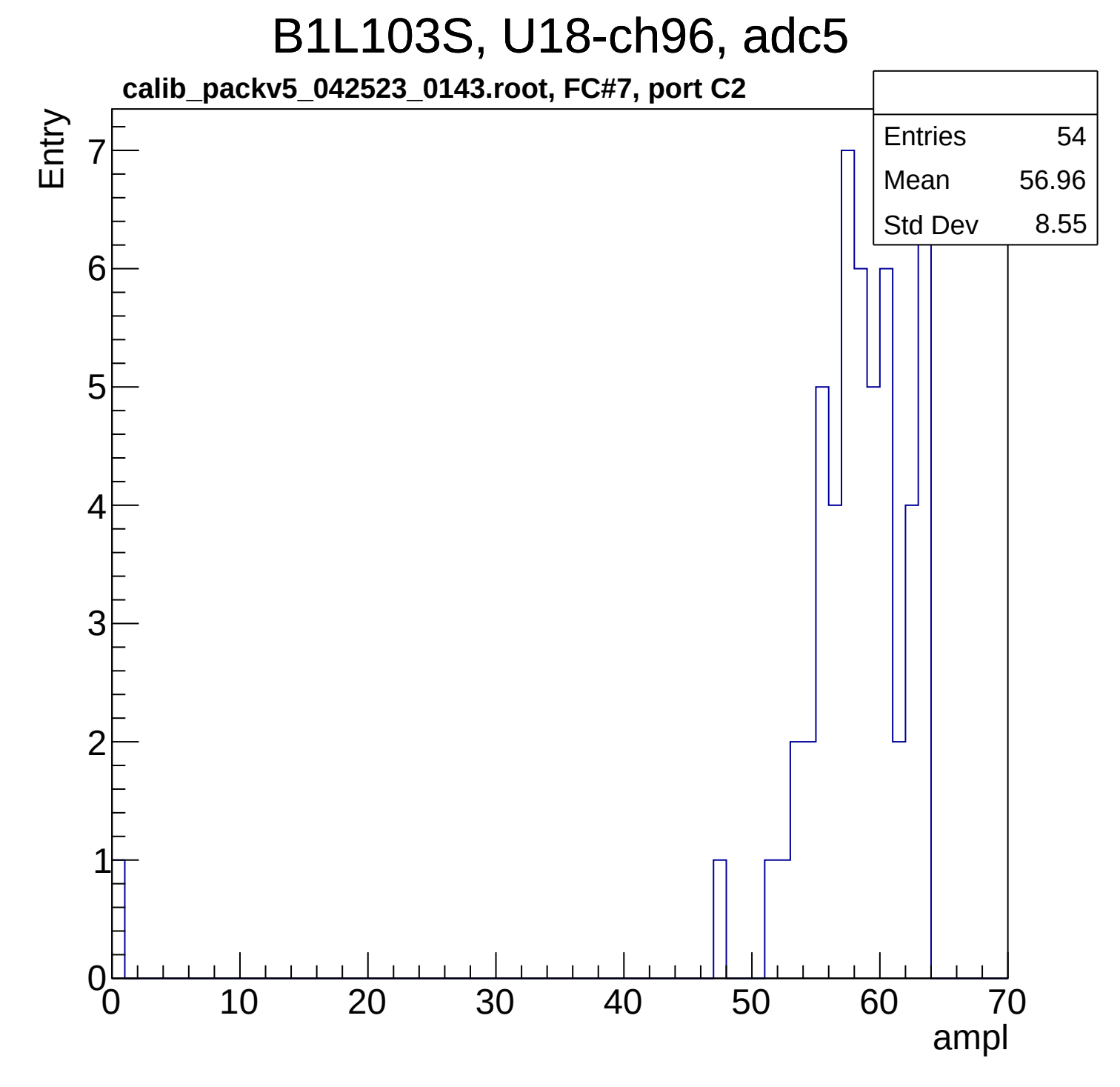

B1L103S, U18-ch96, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 84
Mean 46.86
Std Dev 3.953
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch96, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 54.7
Std Dev 4.101
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U18-ch96, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 54
Mean 56.96
Std Dev 8.55
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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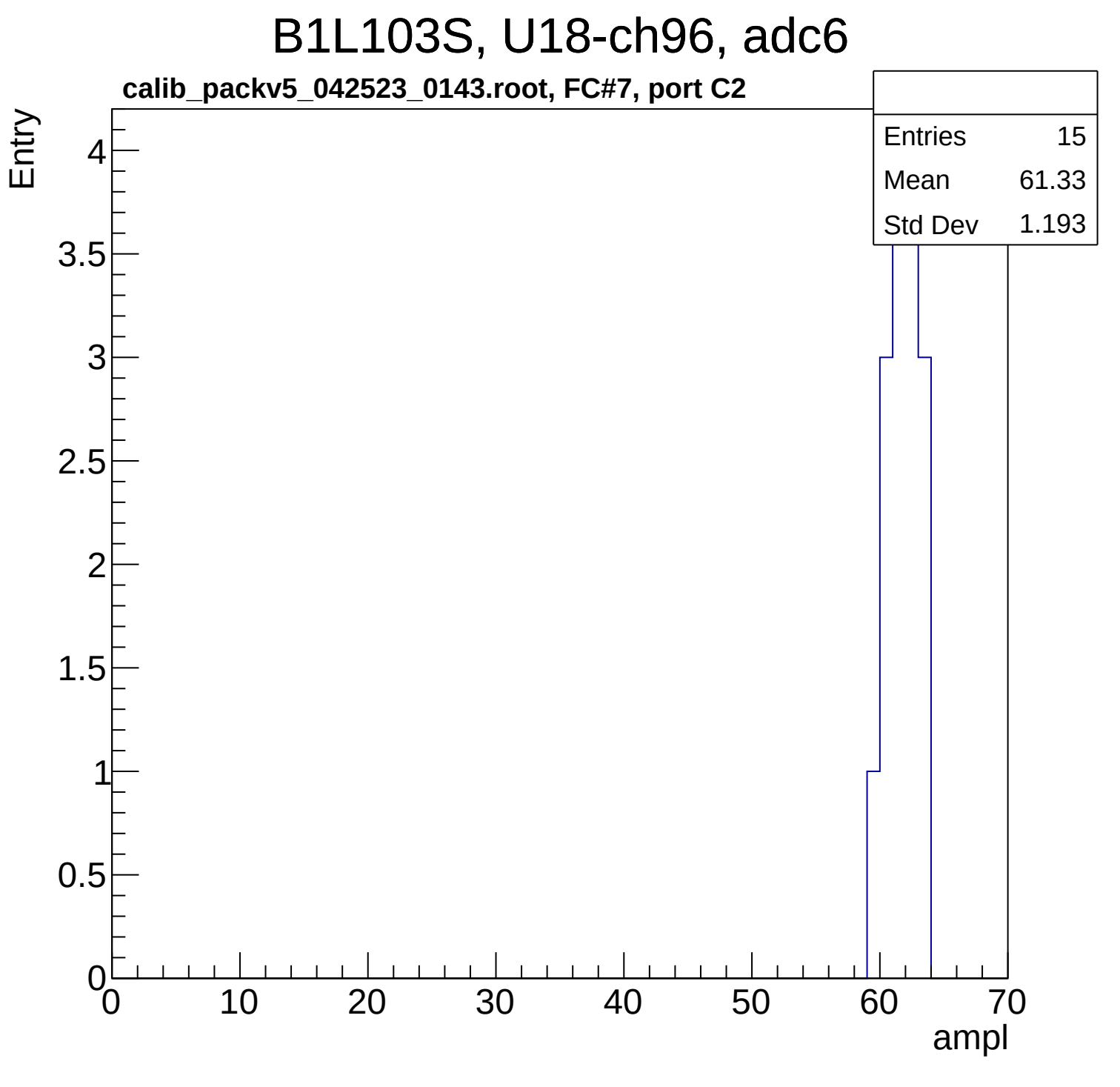
B1L103S, U18-ch96, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 15
Mean 61.33
Std Dev 1.193
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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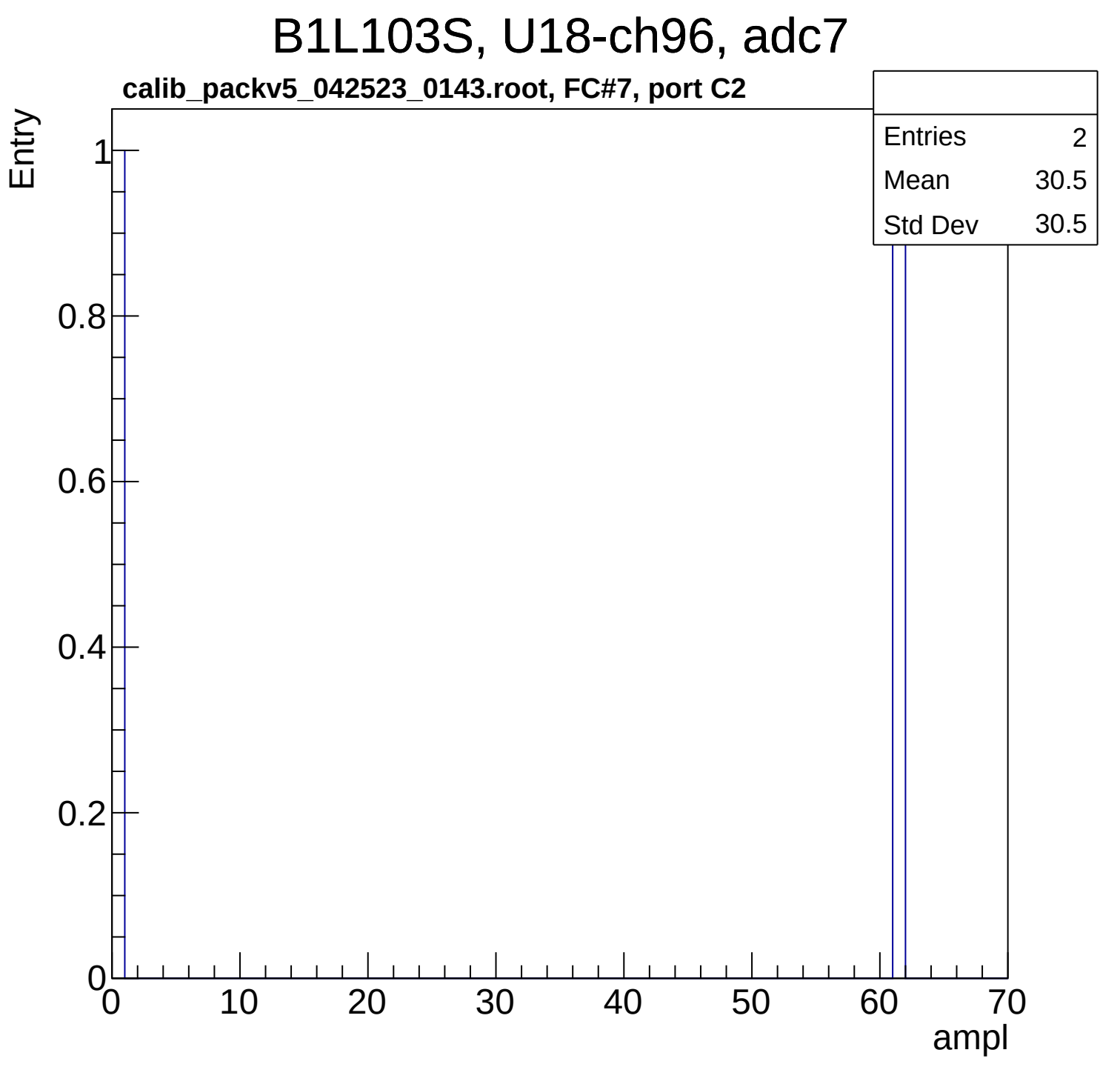
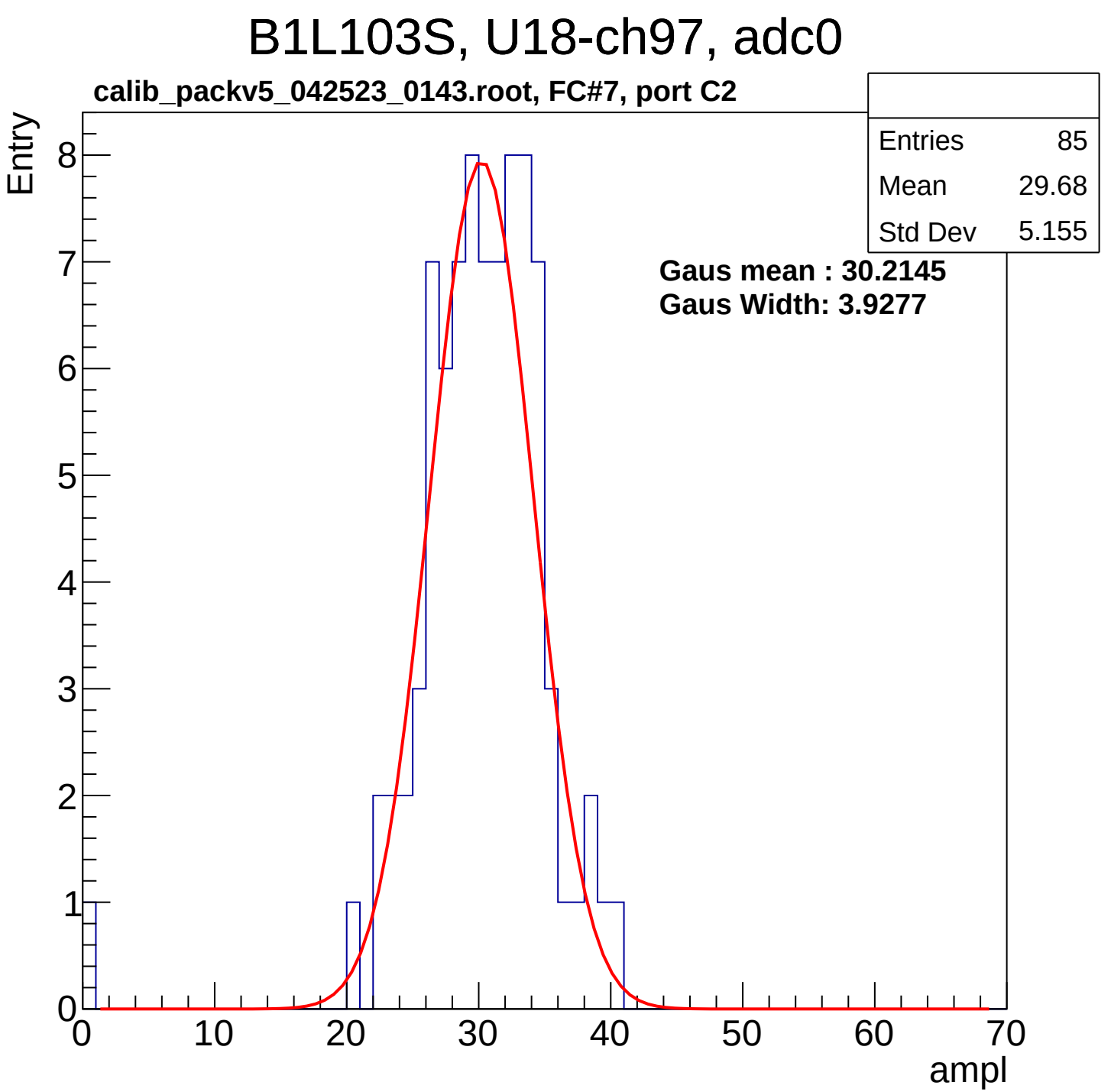

B1L103S, U18-ch96, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 30.5
Std Dev 30.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch97, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 85
Mean 29.68
Std Dev 5.155
Gaus mean : 30.2145
Gaus Width: 3.9277
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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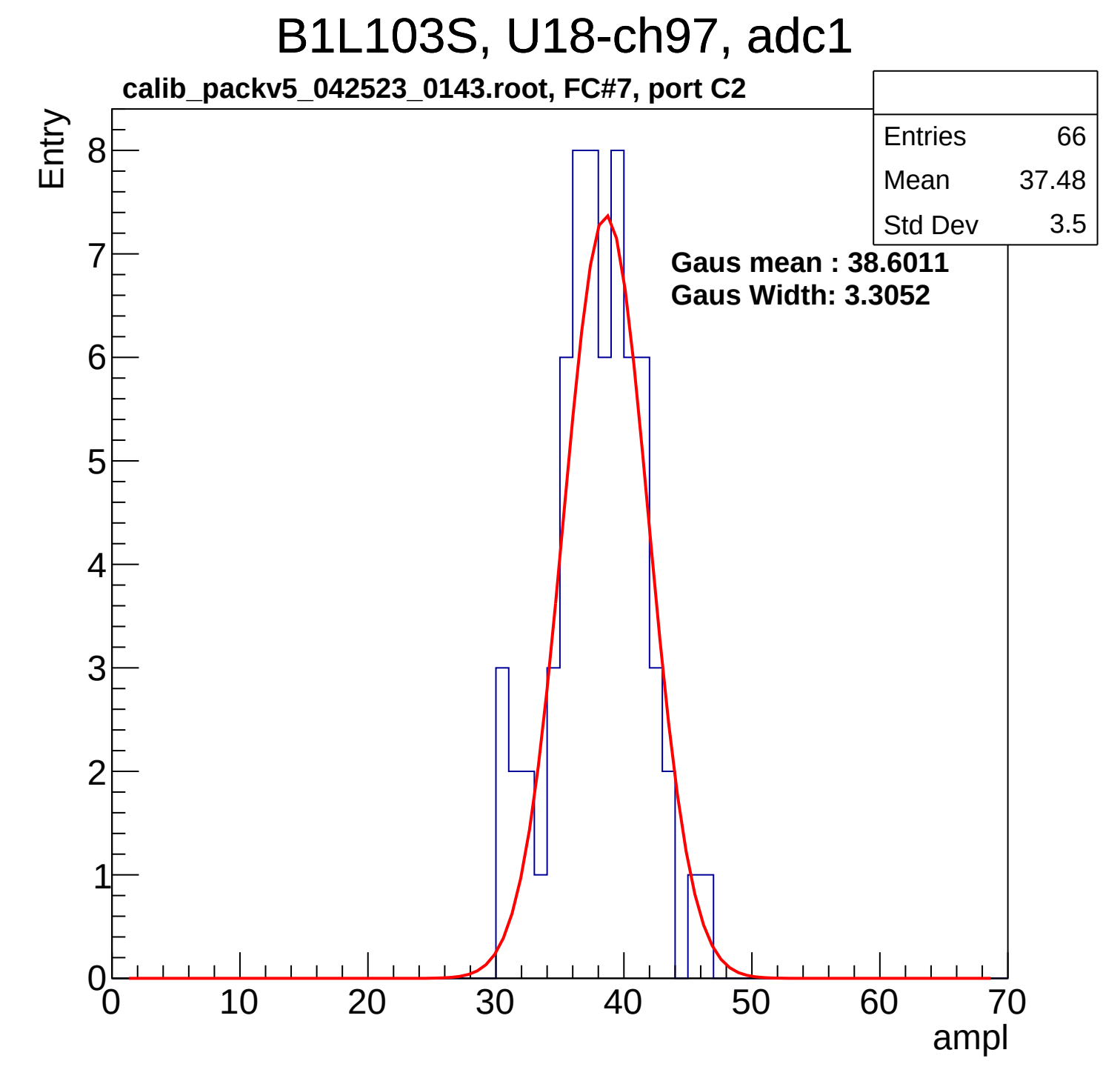
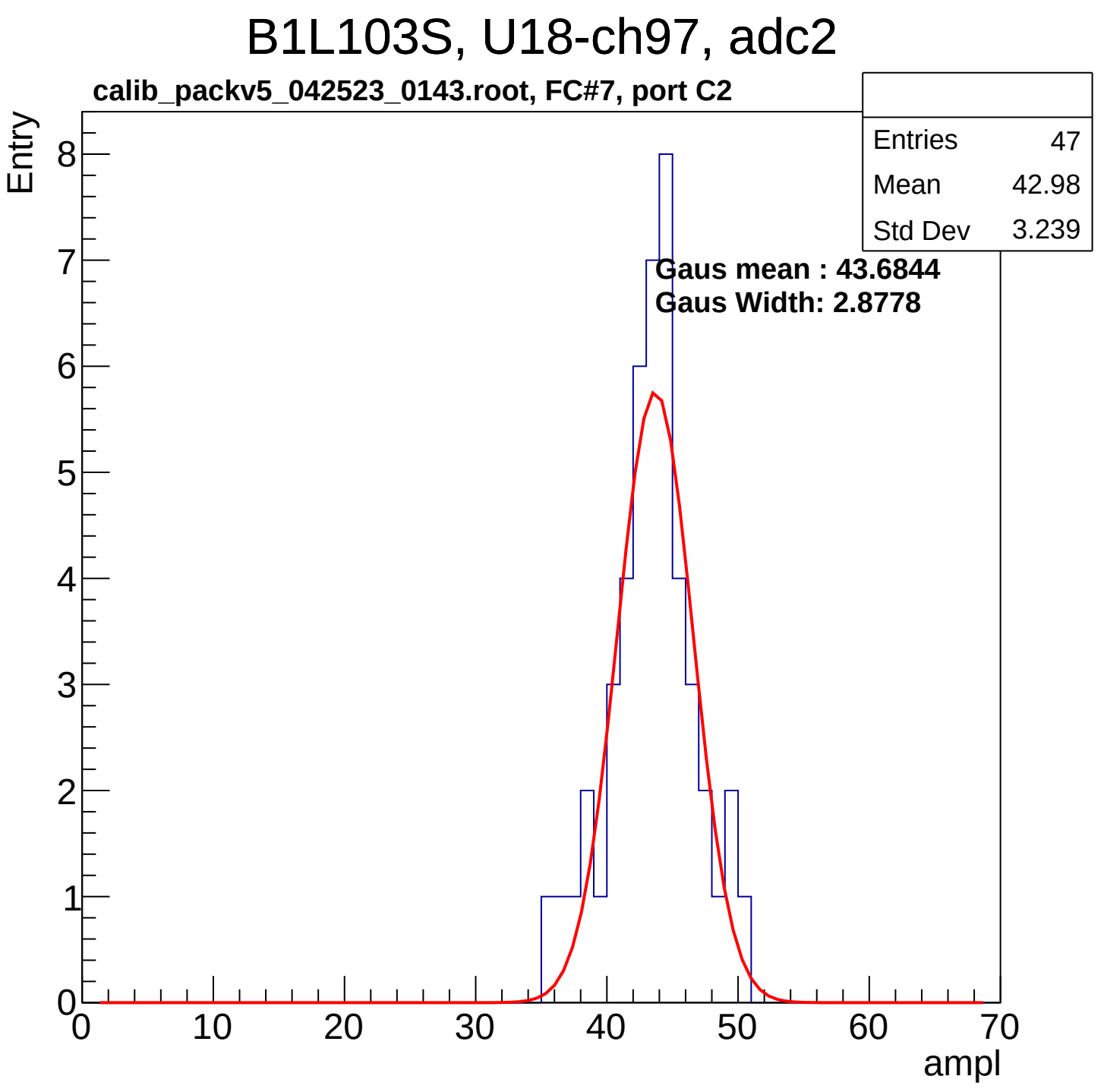
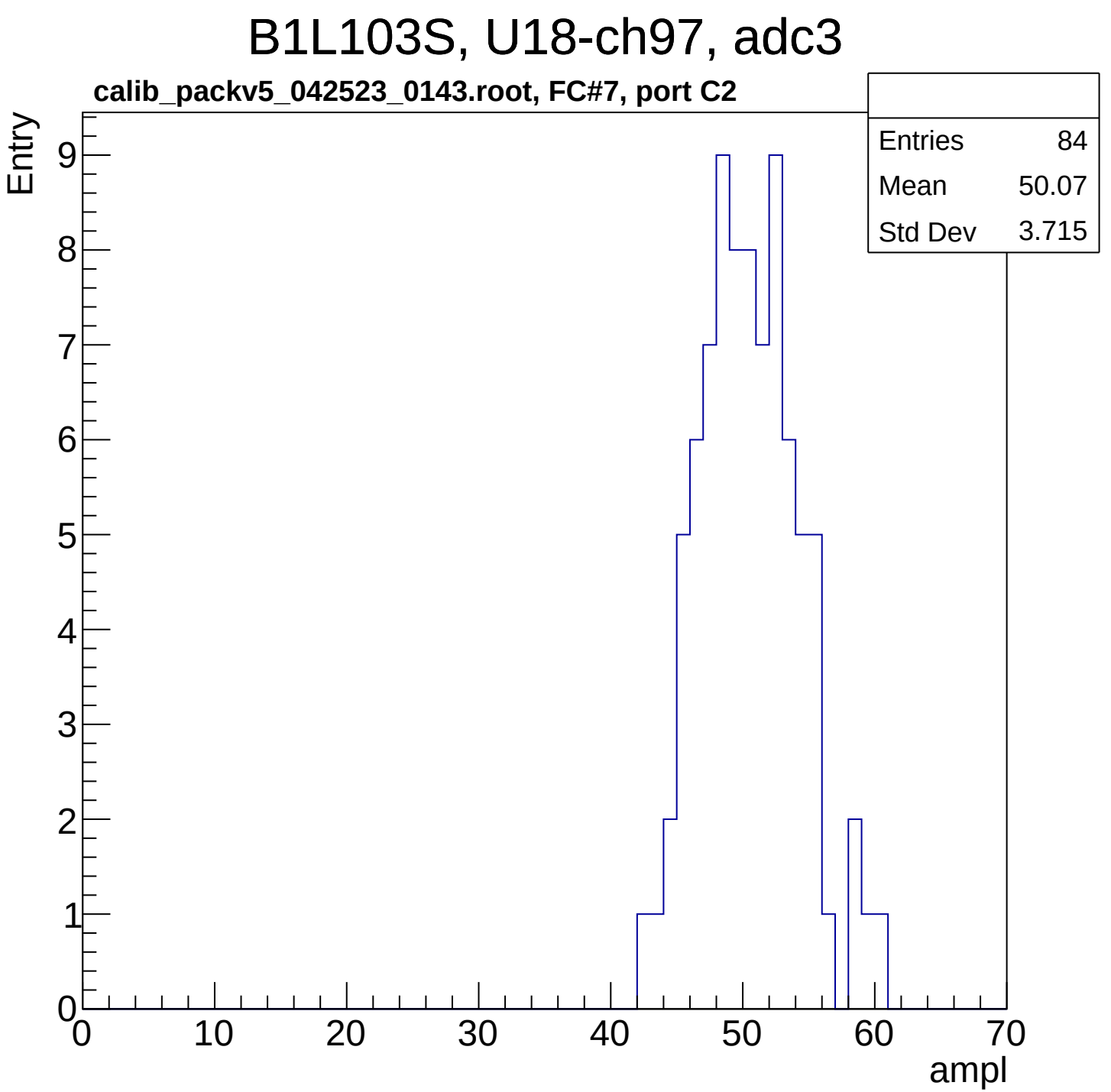

B1L103S, U18-ch97, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 37.48
Std Dev 3.5
Gaus mean : 38.6011
Gaus Width: 3.3052
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch97, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 47
Mean 42.98
Std Dev 3.239
Gaus mean : 43.6844
Gaus Width: 2.8778
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch97, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 84
Mean 50.07
Std Dev 3.715
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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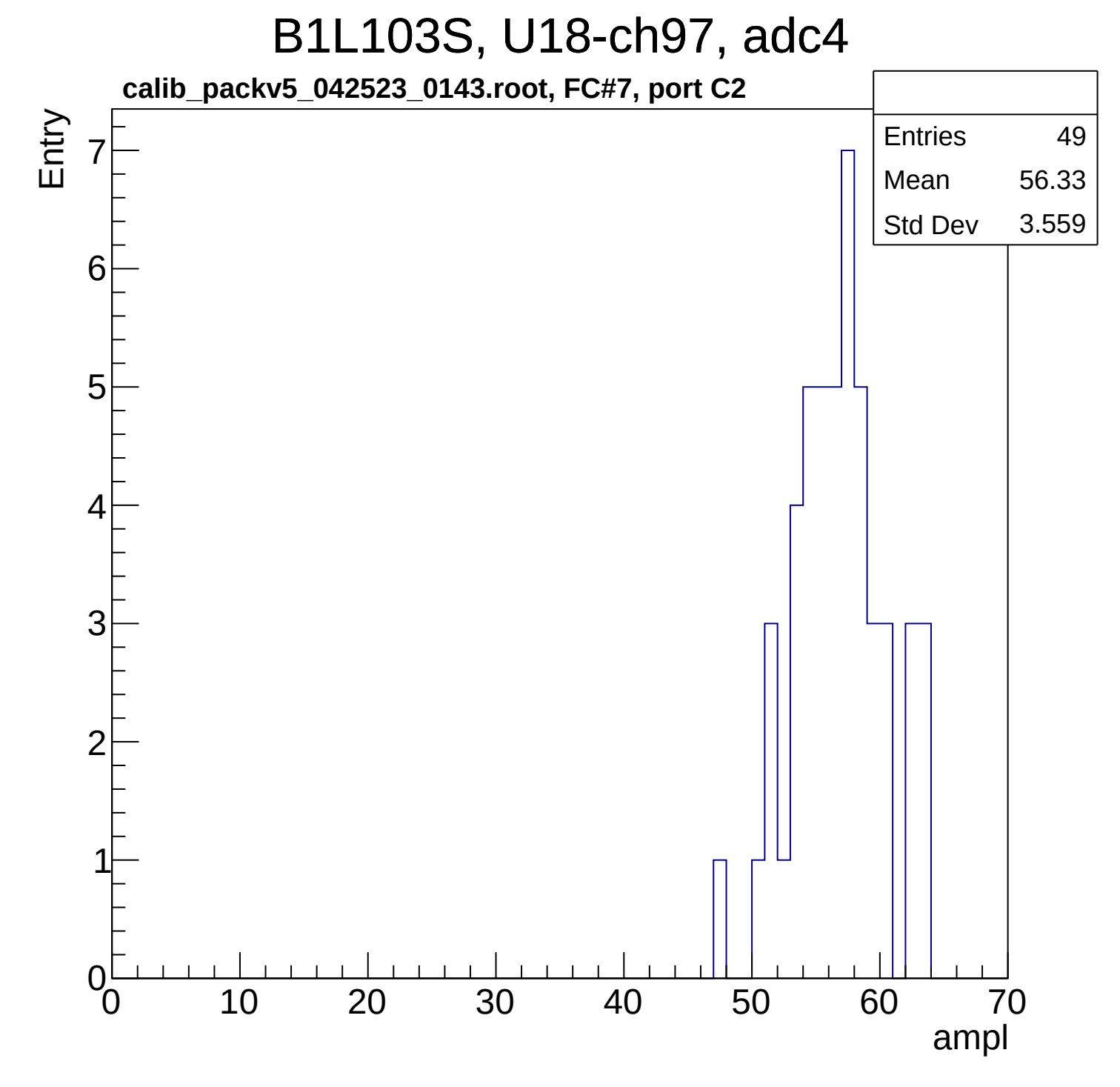
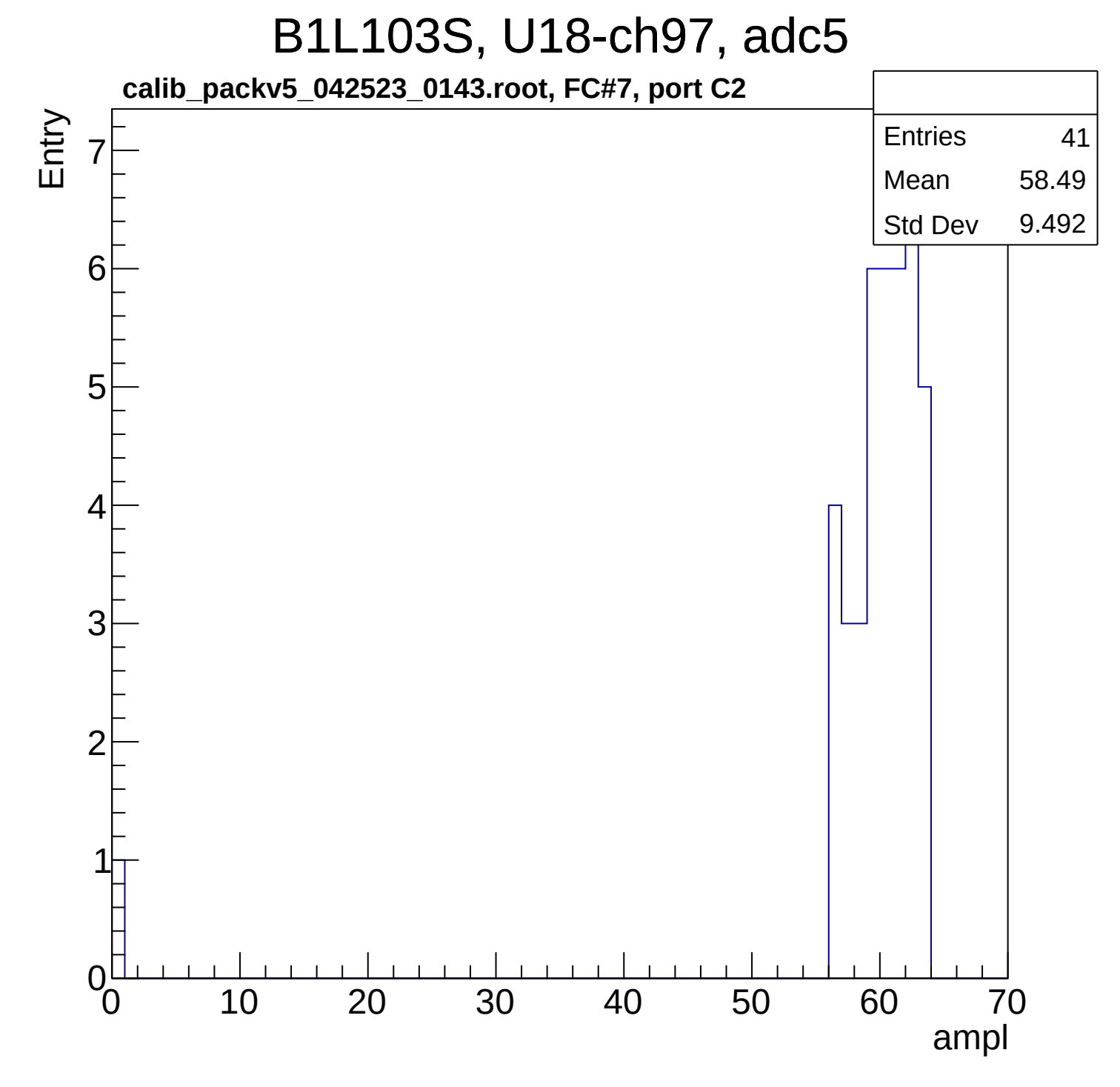

B1L103S, U18-ch97, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 49
Mean 56.33
Std Dev 3.559
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch97, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 41
Mean 58.49
Std Dev 9.492
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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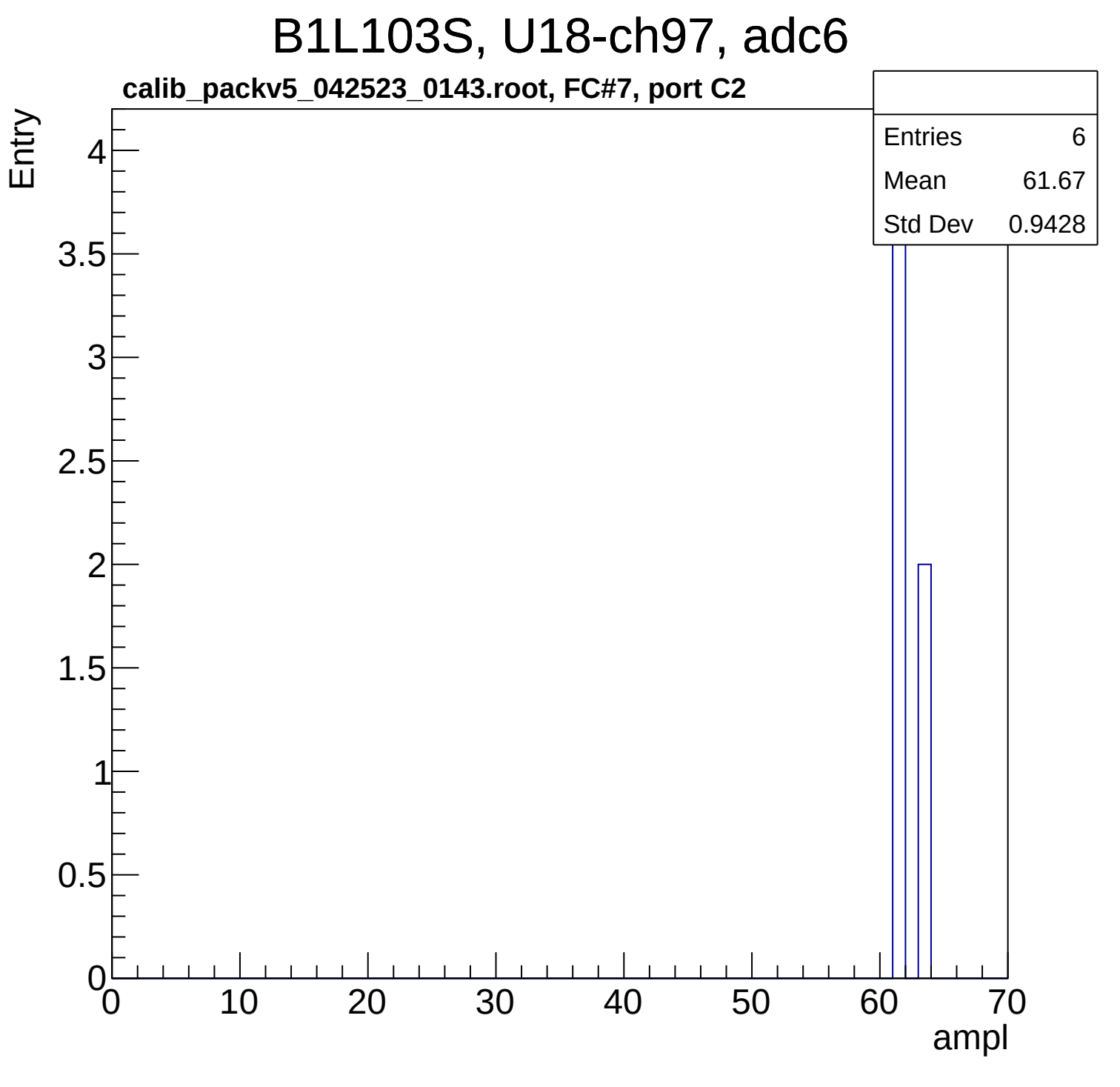
40
50
60
70


B1L103S, U18-ch97, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 6
Mean 61.67
Std Dev 0.9428
Entry
ampl
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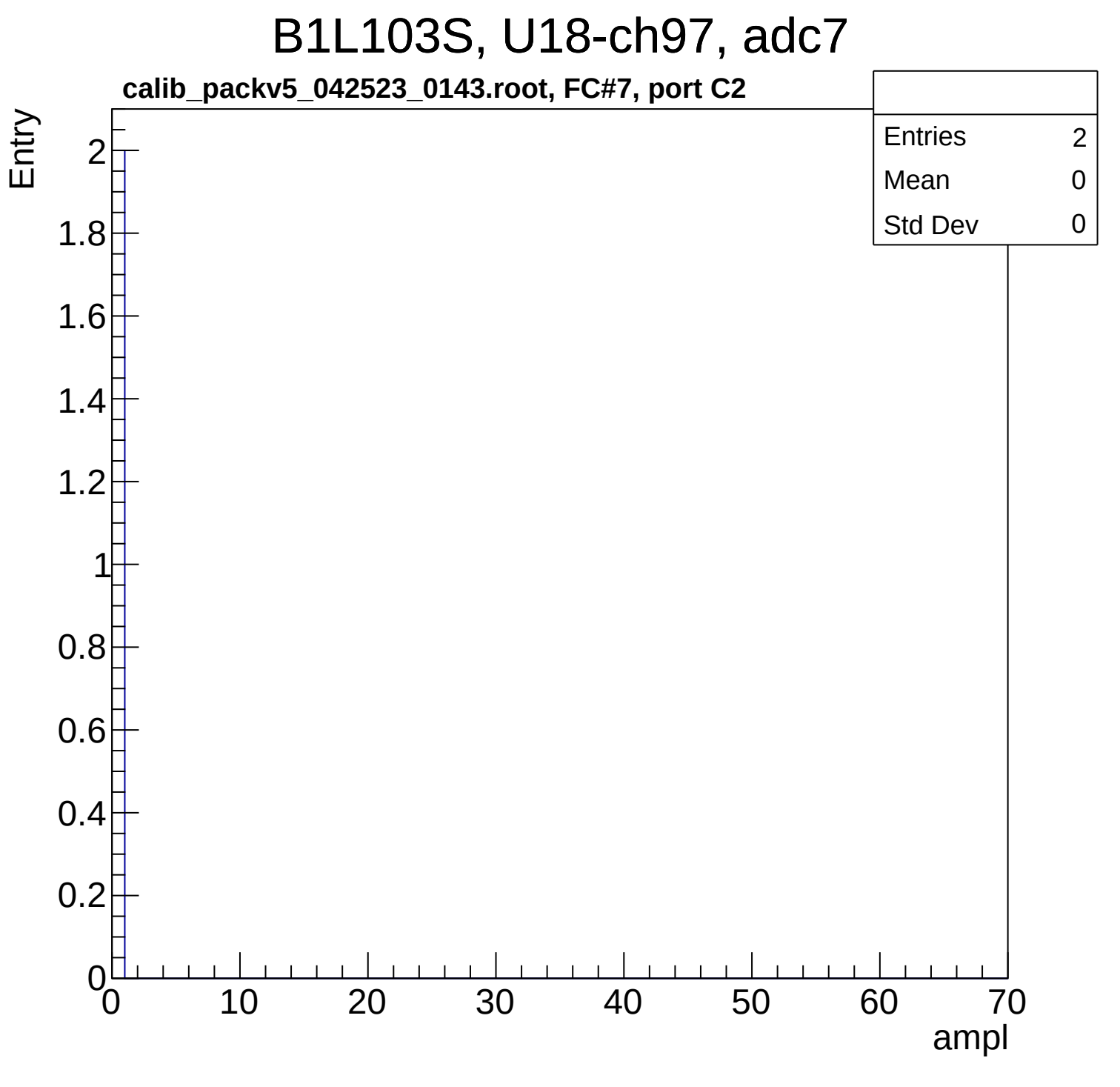
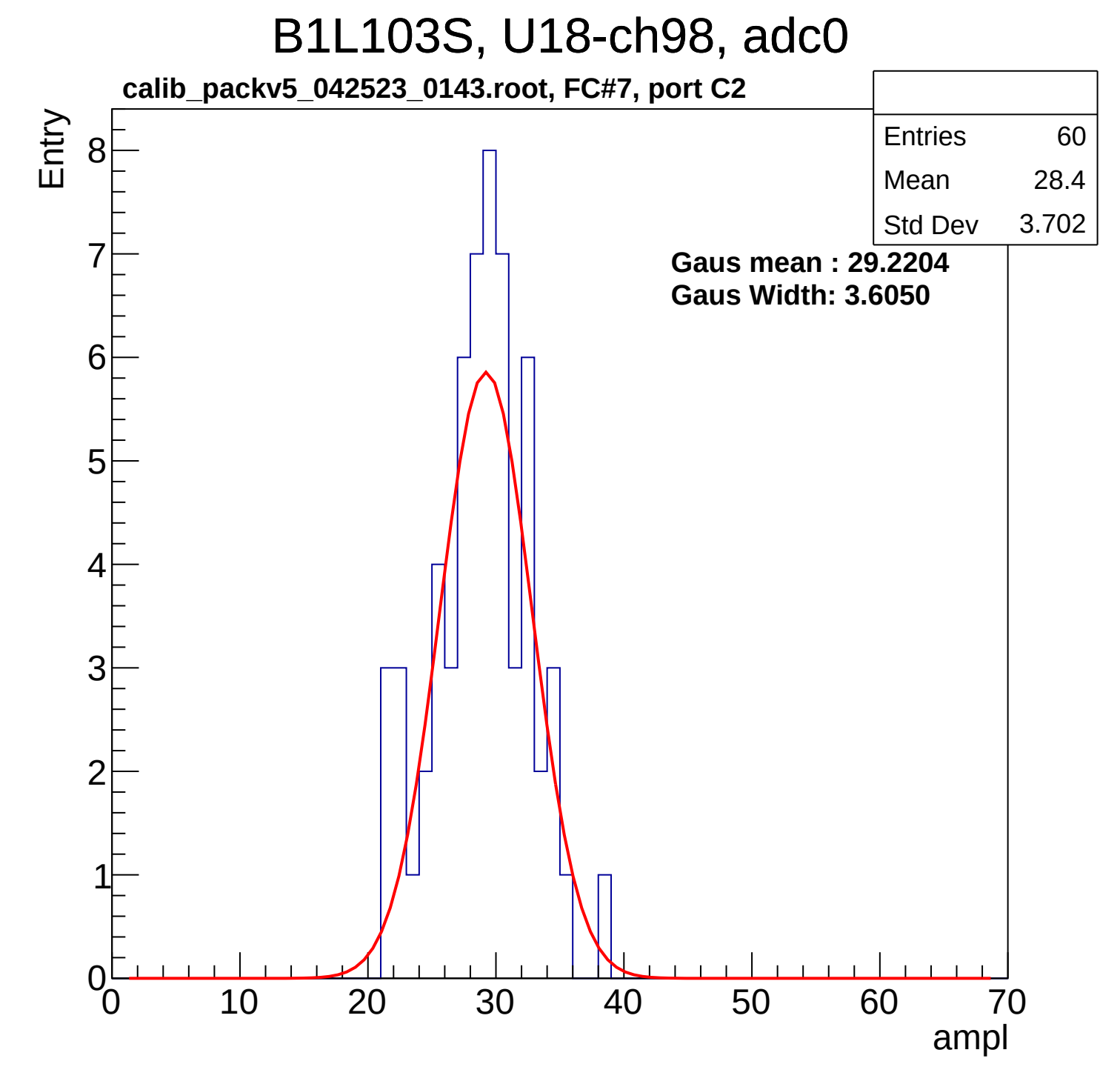
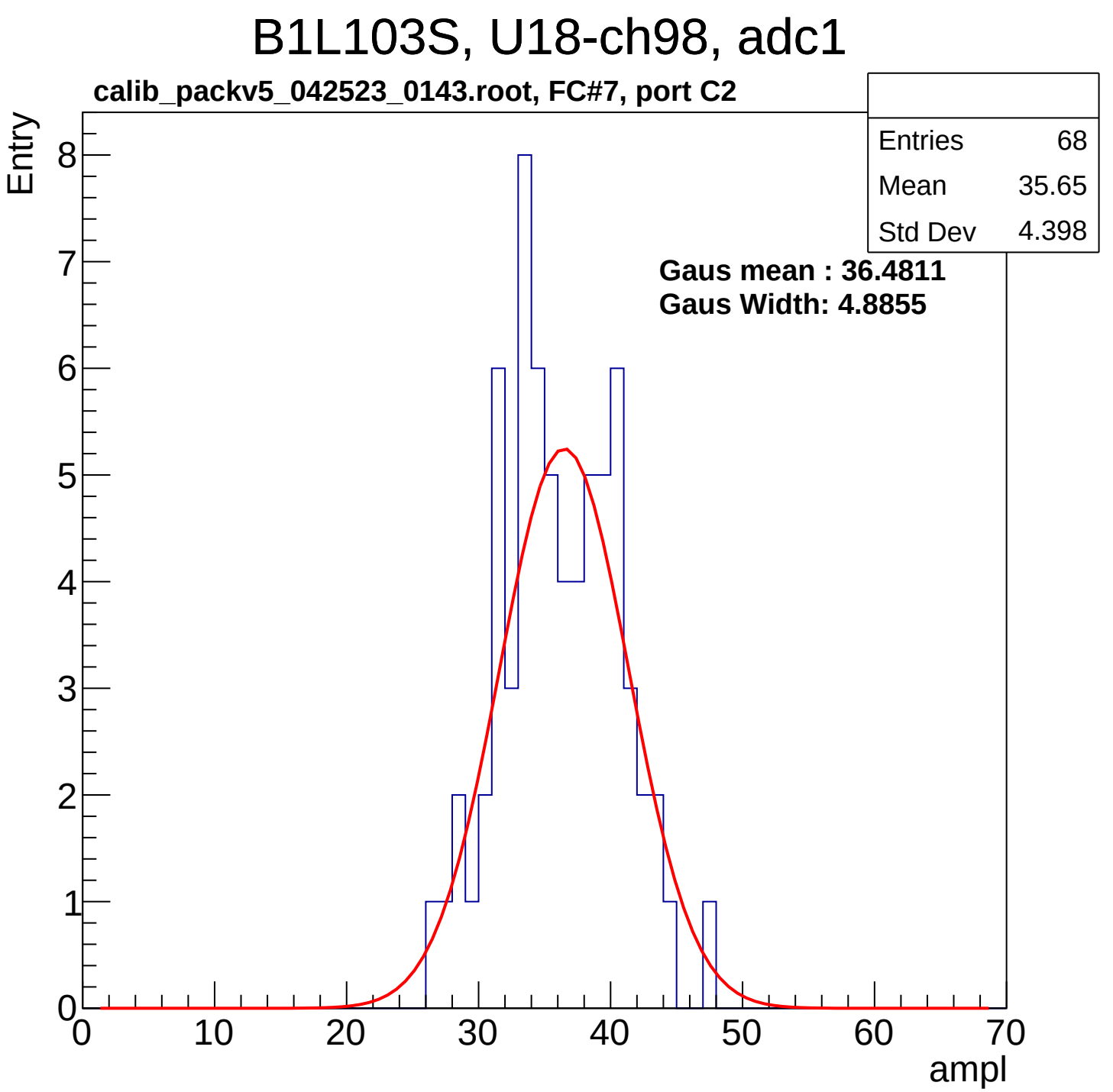
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U18-ch97, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch98, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 60
Mean 28.4
Std Dev 3.702
Gaus mean : 29.2204
Gaus Width: 3.6050
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch98, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 35.65
Std Dev 4.398
Gaus mean : 36.4811
Gaus Width: 4.8855
Entry
ampl
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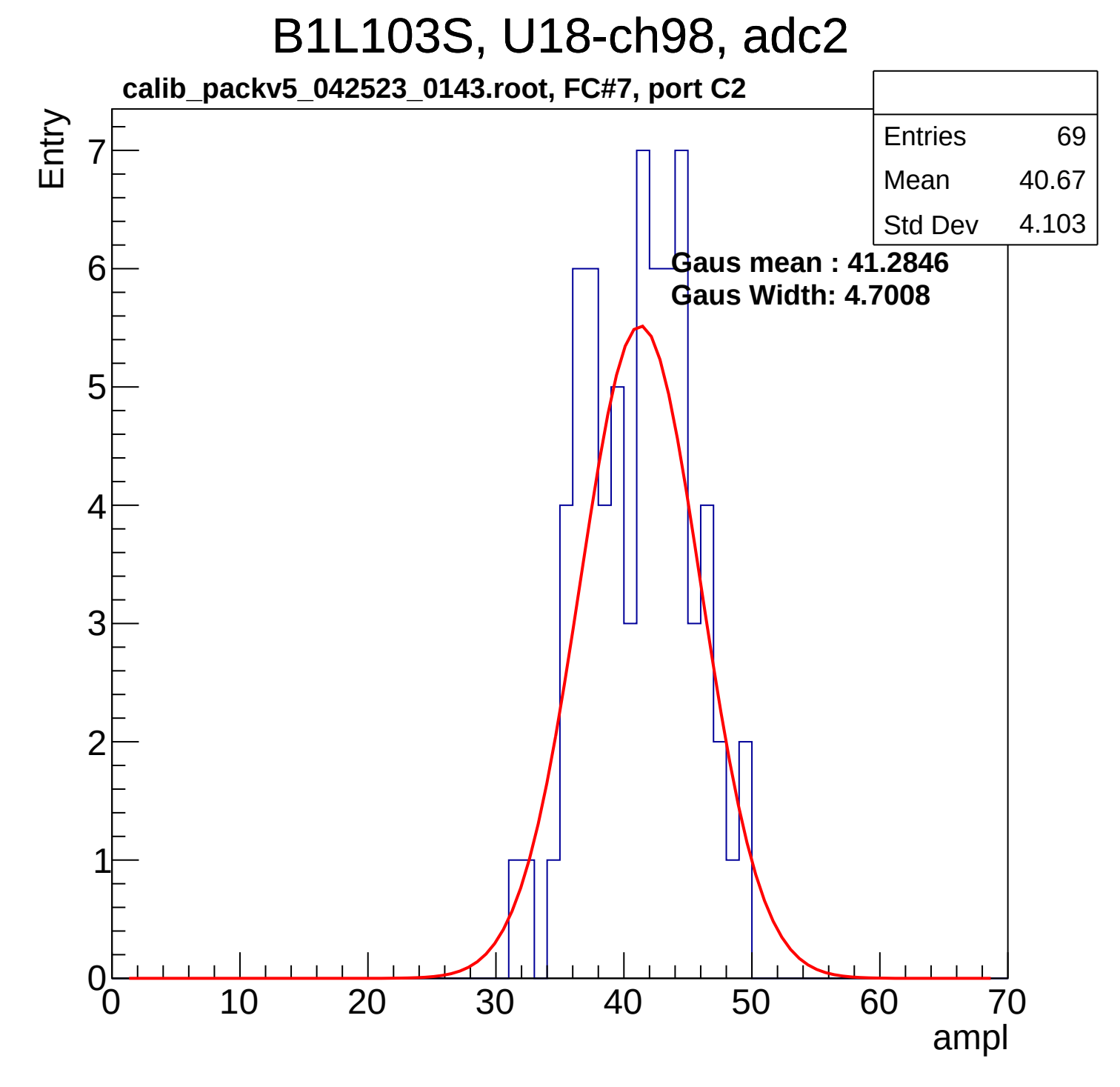
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch98, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 40.67
Std Dev 4.103
Gaus mean : 41.2846
Gaus Width: 4.7008
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
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60
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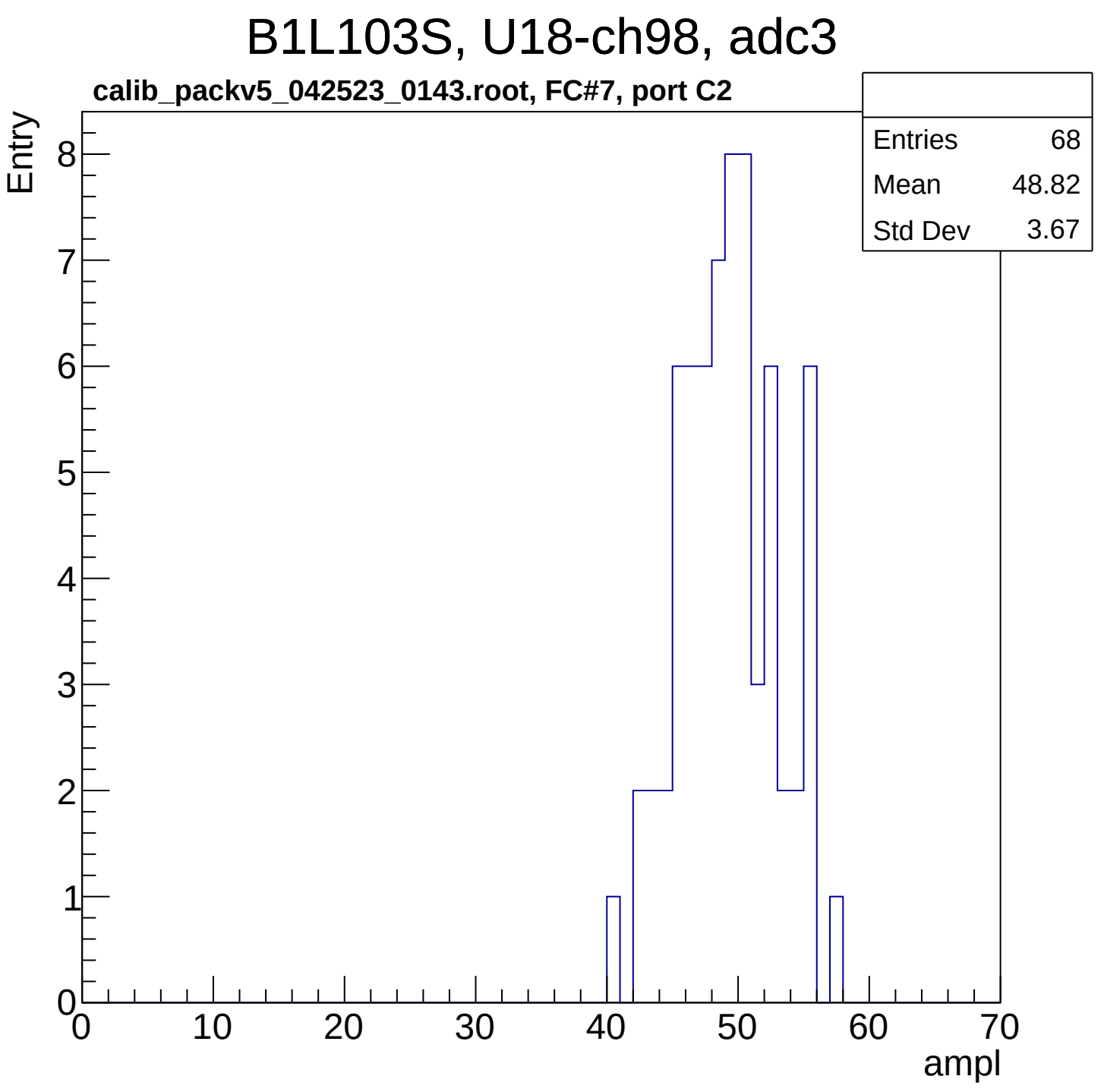
B1L103S, U18-ch98, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 48.82
Std Dev 3.67
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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40
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60
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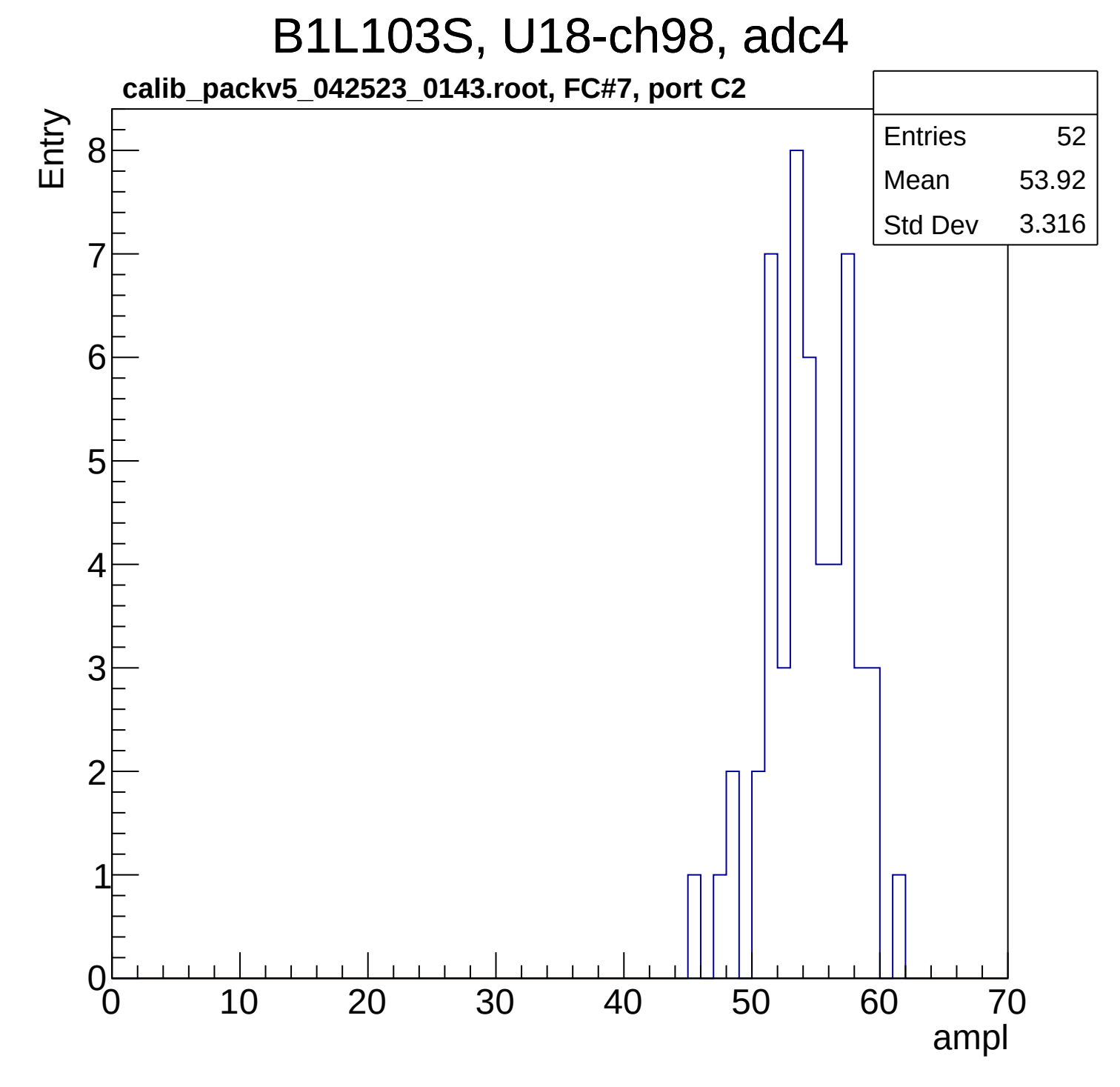
B1L103S, U18-ch98, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 52
Mean 53.92
Std Dev 3.316
Entry
ampl
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2
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0
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20
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60
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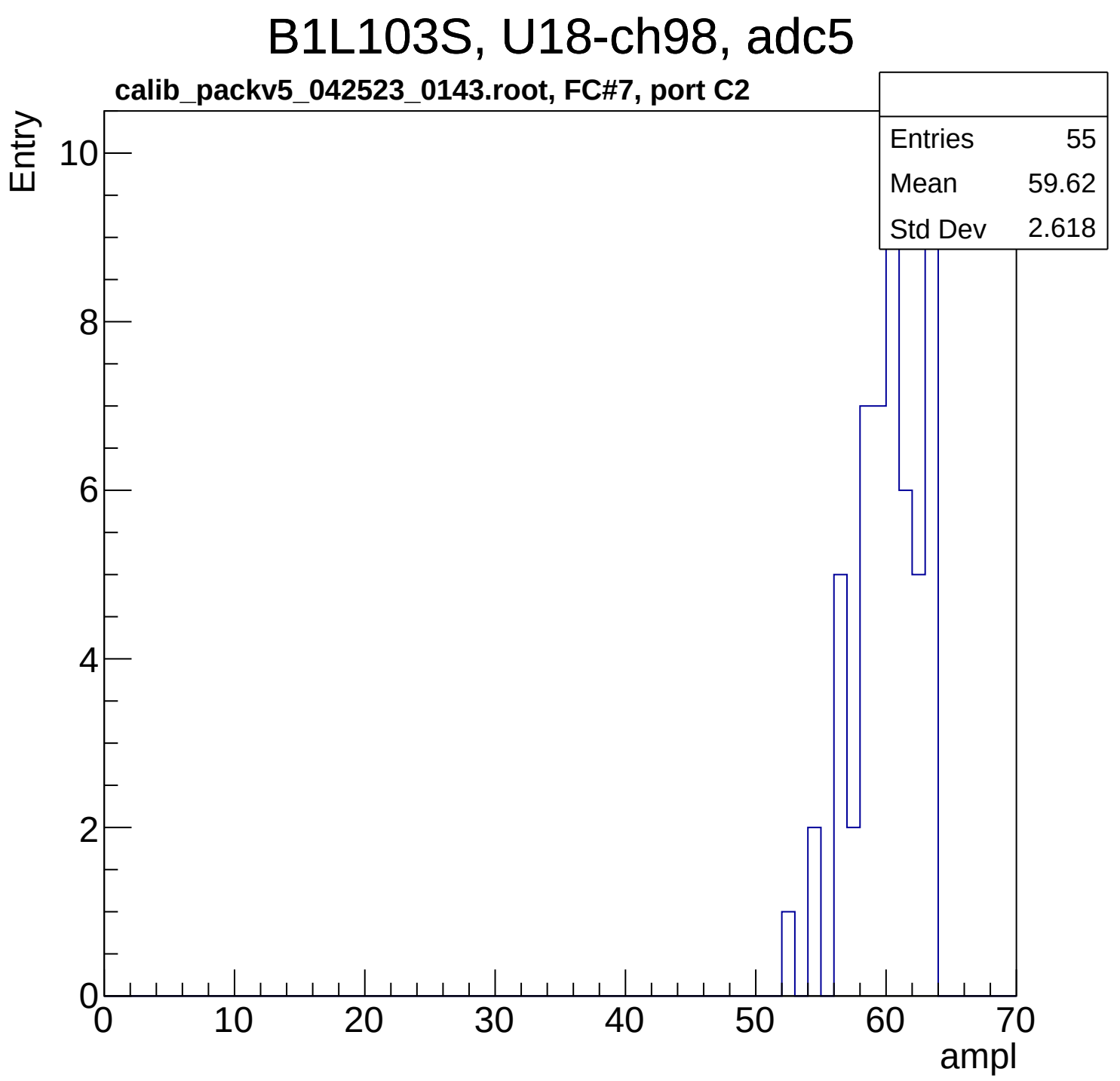
B1L103S, U18-ch98, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 59.62
Std Dev 2.618
Entry
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4
6
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10
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20
30
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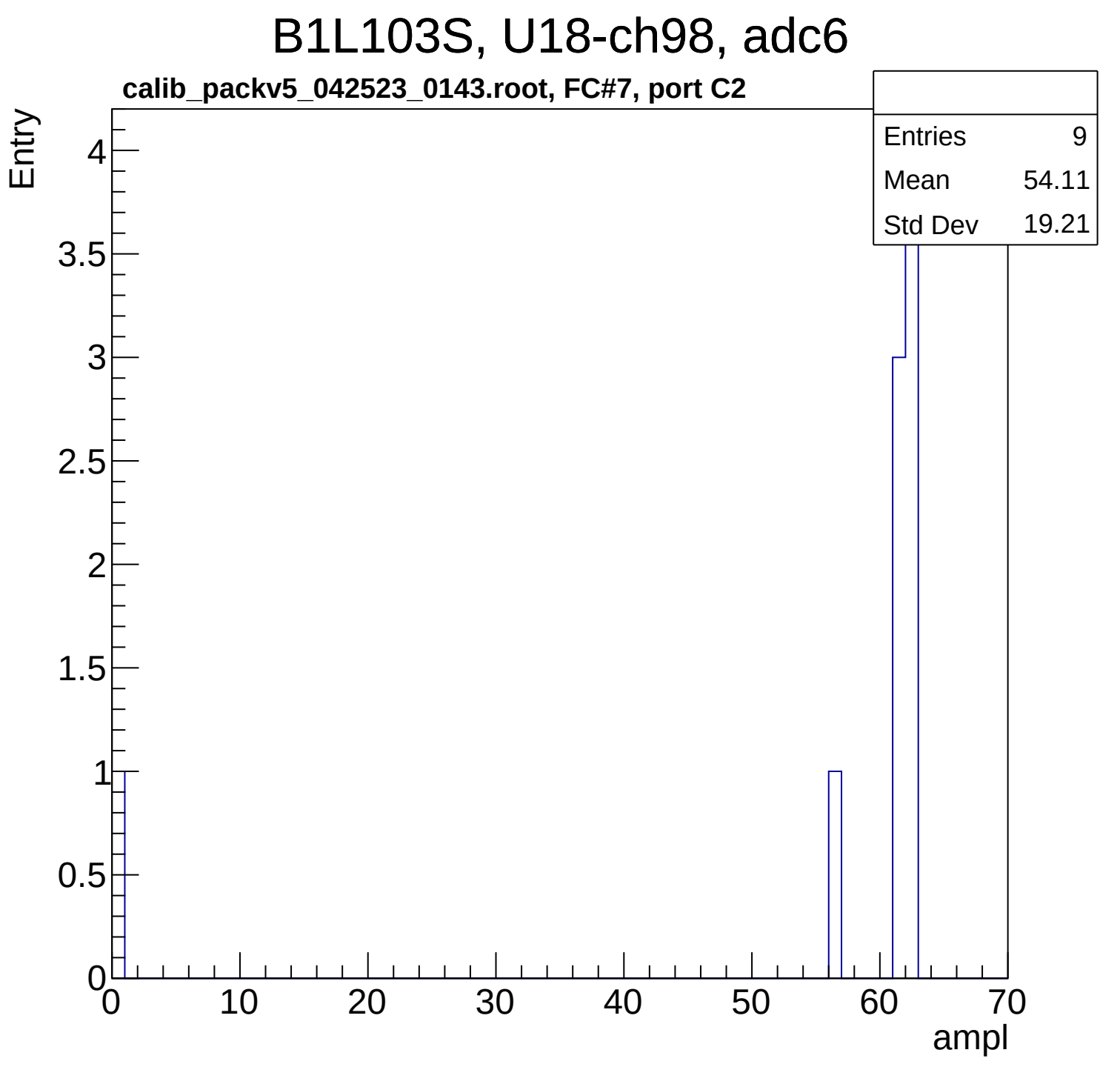
50
60
70
ampl


B1L103S, U18-ch98, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 9
Mean 54.11
Std Dev 19.21
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
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20
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40
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60
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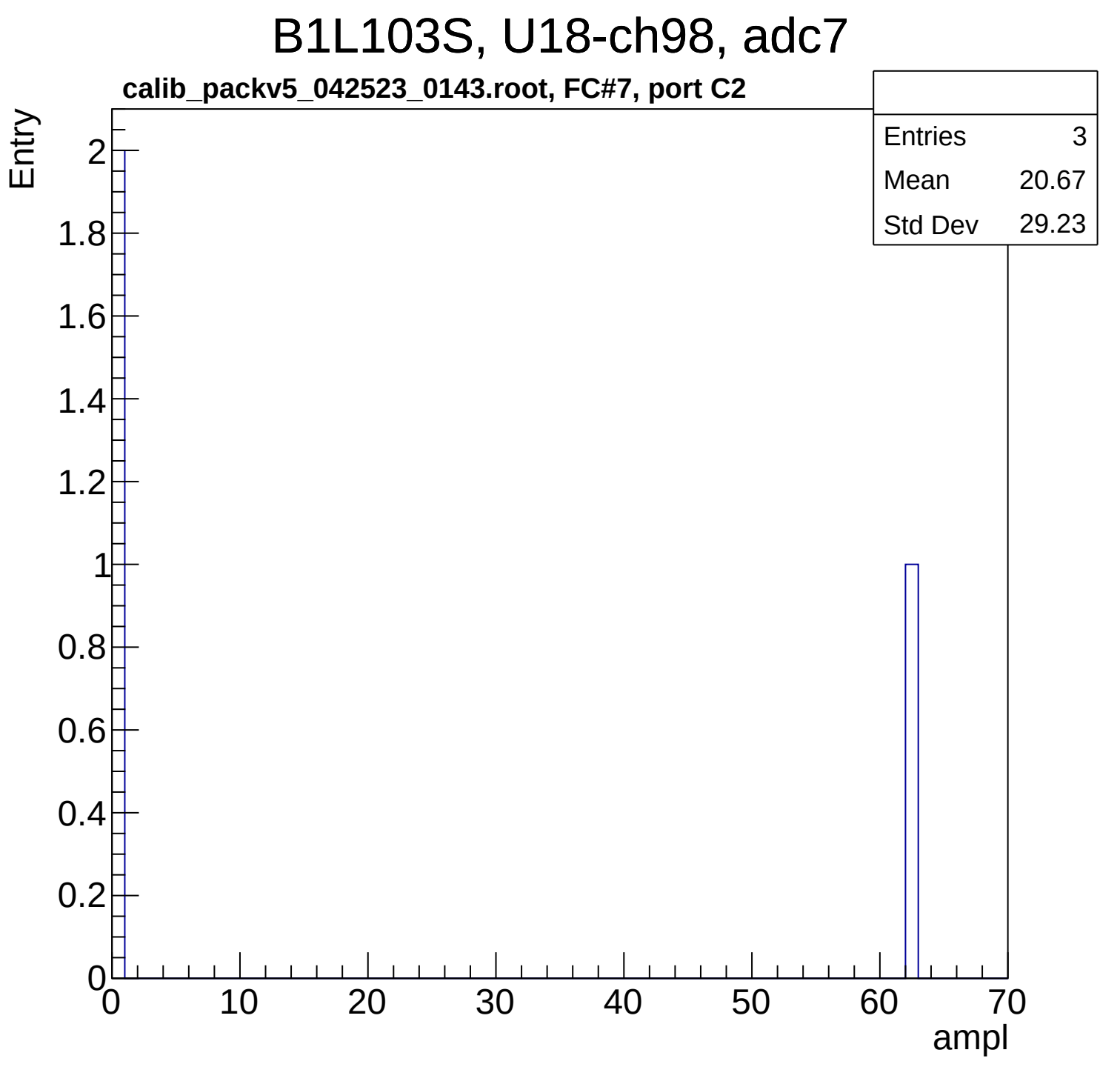
B1L103S, U18-ch98, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 20.67
Std Dev 29.23
Entry
ampl
0
0.2
0.4
0.6
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1
1.2
1.4
1.6
1.8
2
0
10
20
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40
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60
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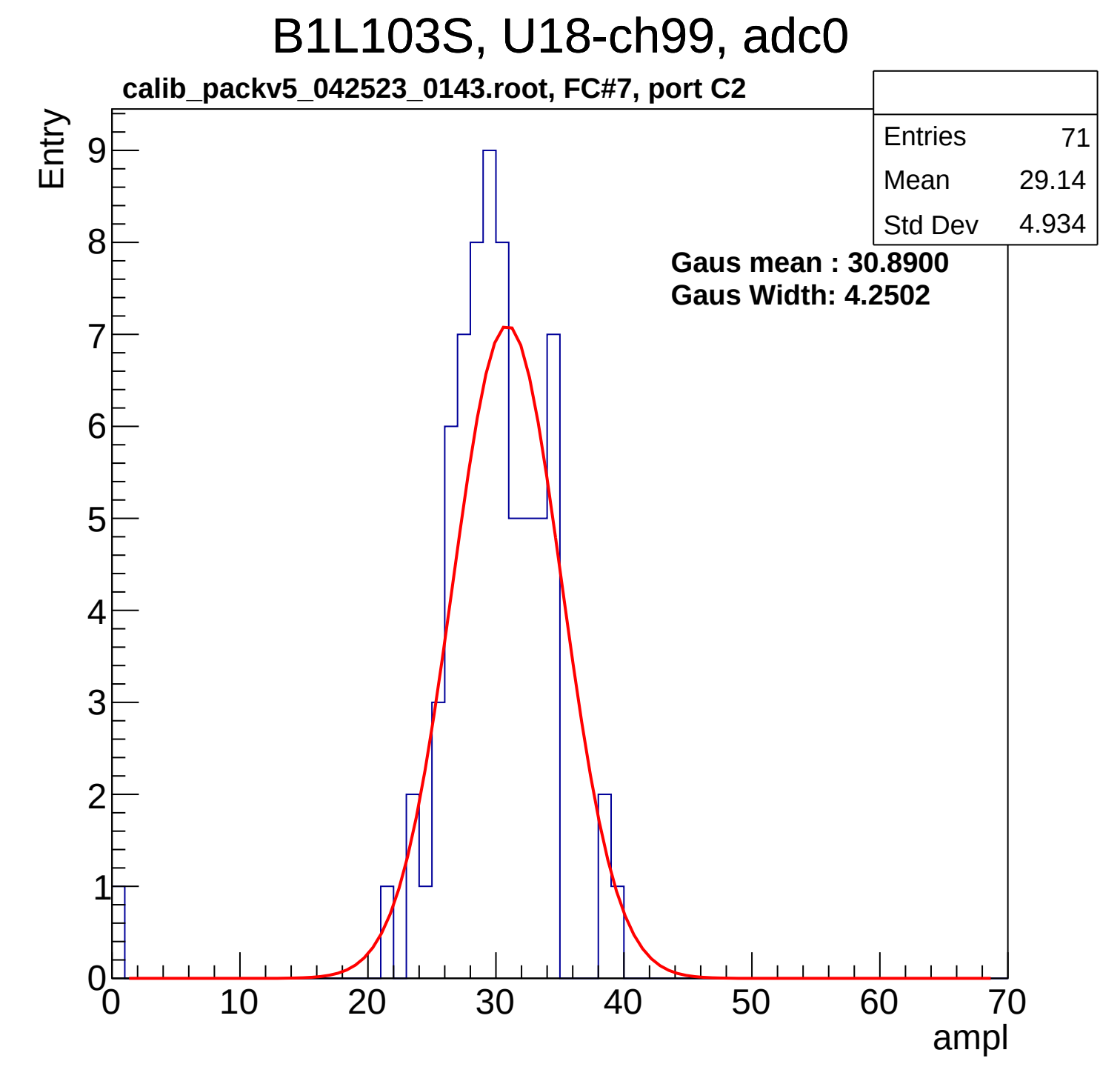
B1L103S, U18-ch99, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 71
Mean 29.14
Std Dev 4.934
Gaus mean : 30.8900
Gaus Width: 4.2502
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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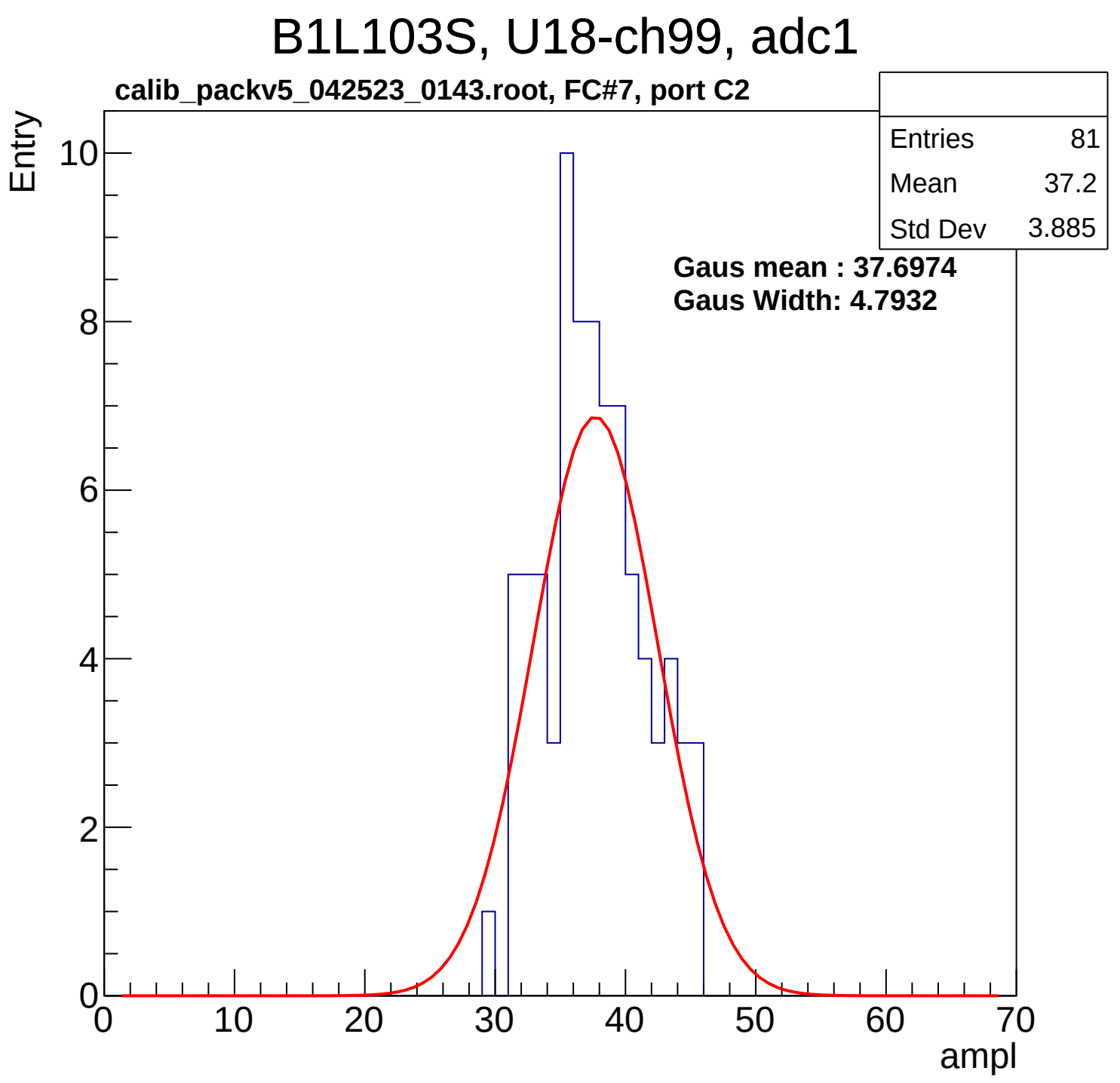
B1L103S, U18-ch99, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 81
Mean 37.2
Std Dev 3.885
Gaus mean : 37.6974
Gaus Width: 4.7932
Entry
ampl
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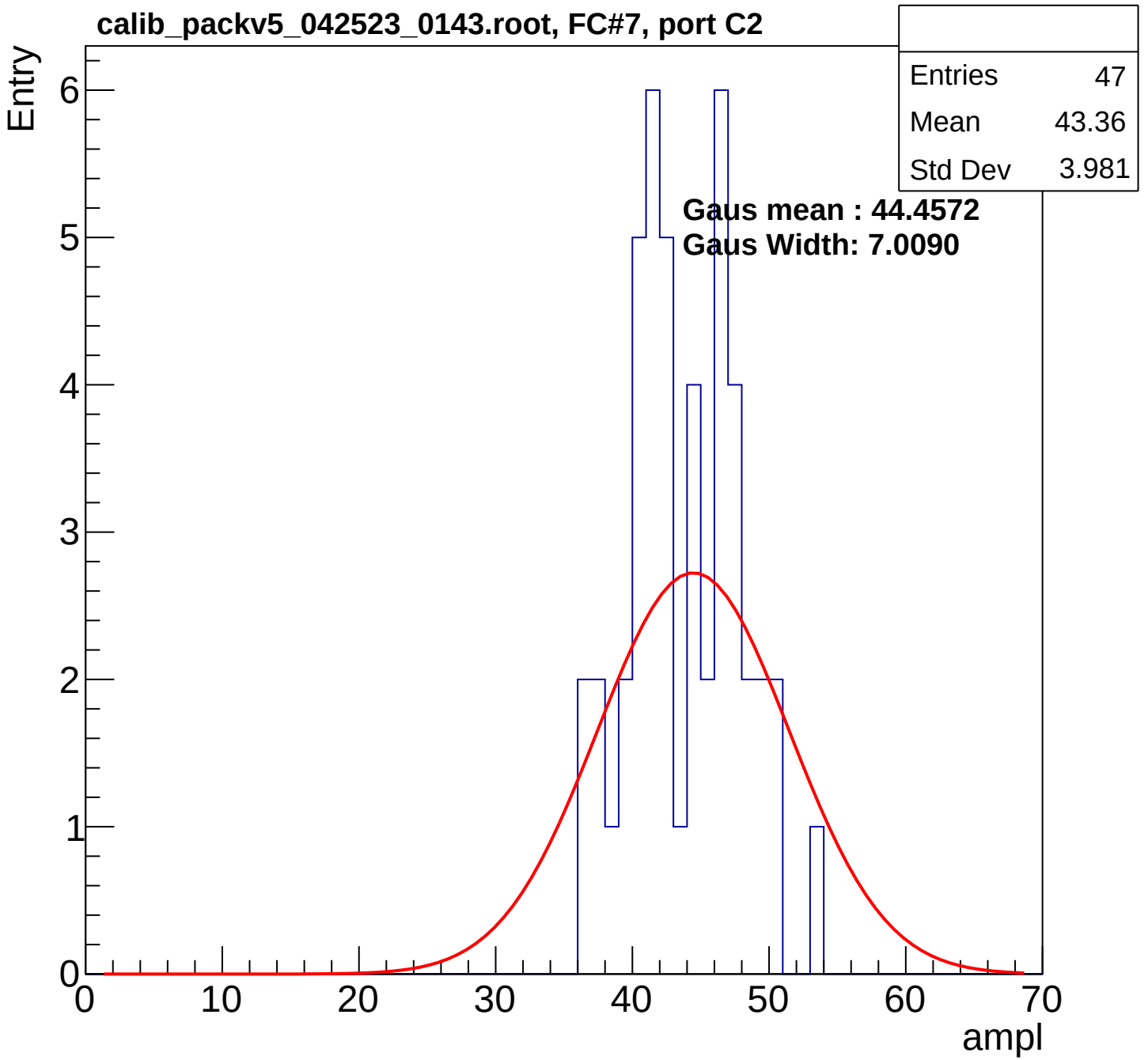
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch99, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 47
Mean 43.36
Std Dev 3.981
Gaus mean : 44.4572
Gaus Width: 7.0090
Entry
ampl
0
1
2
3
4
5
6
0
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20
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40
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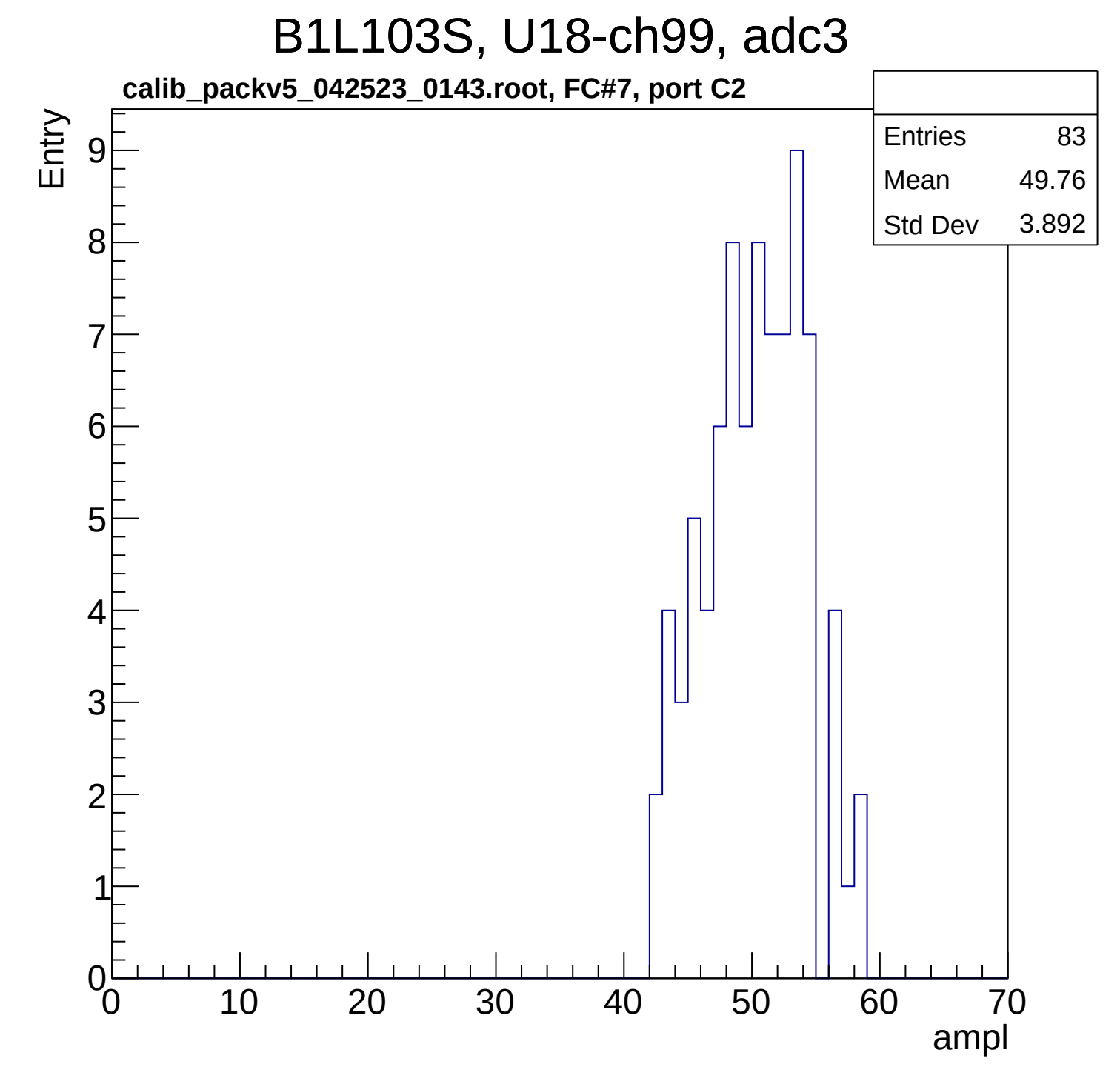
60
70


B1L103S, U18-ch99, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 83
Mean 49.76
Std Dev 3.892
Entry
ampl
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3
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5
6
7
8
9
0
10
20
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40
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60
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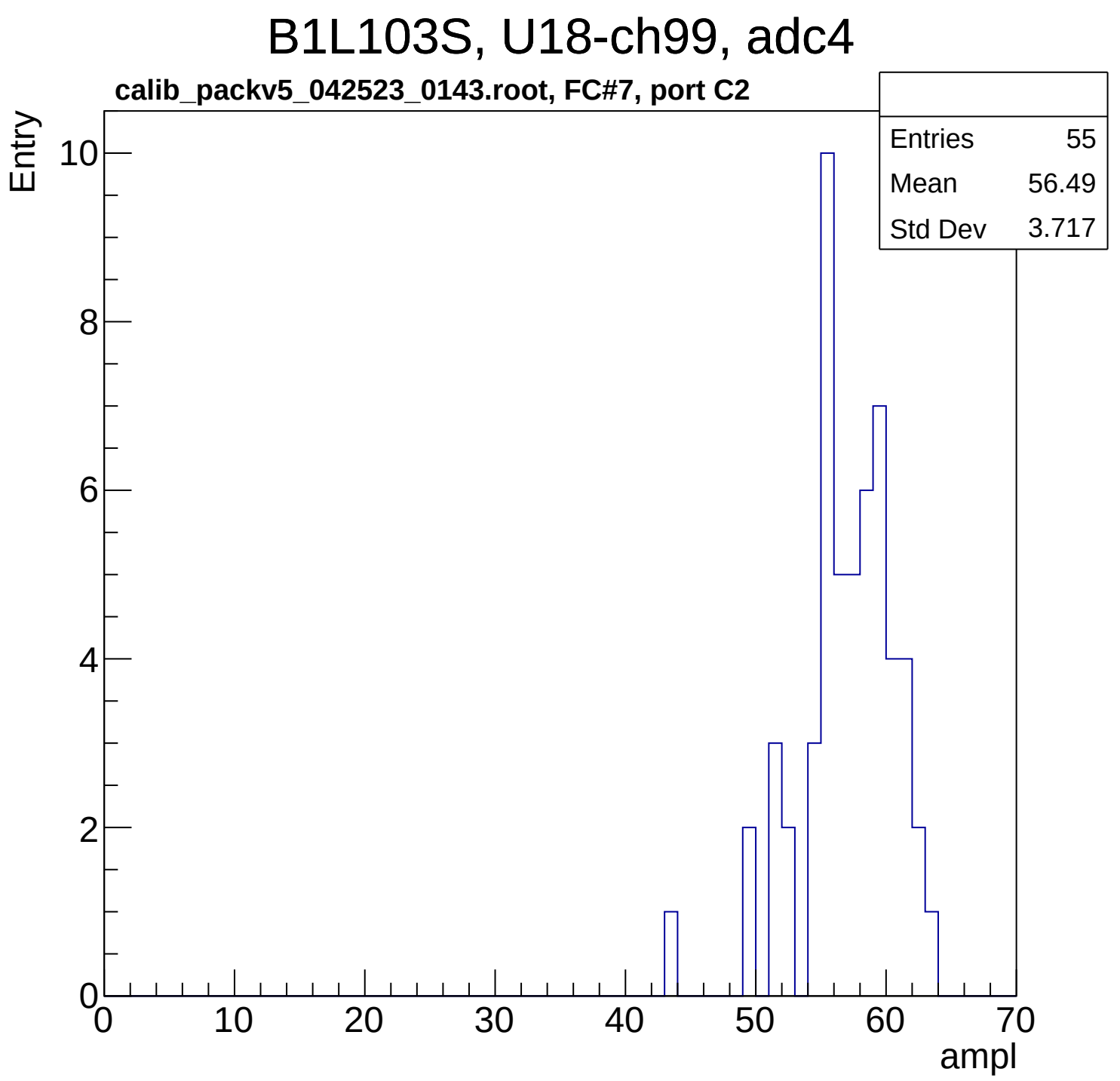
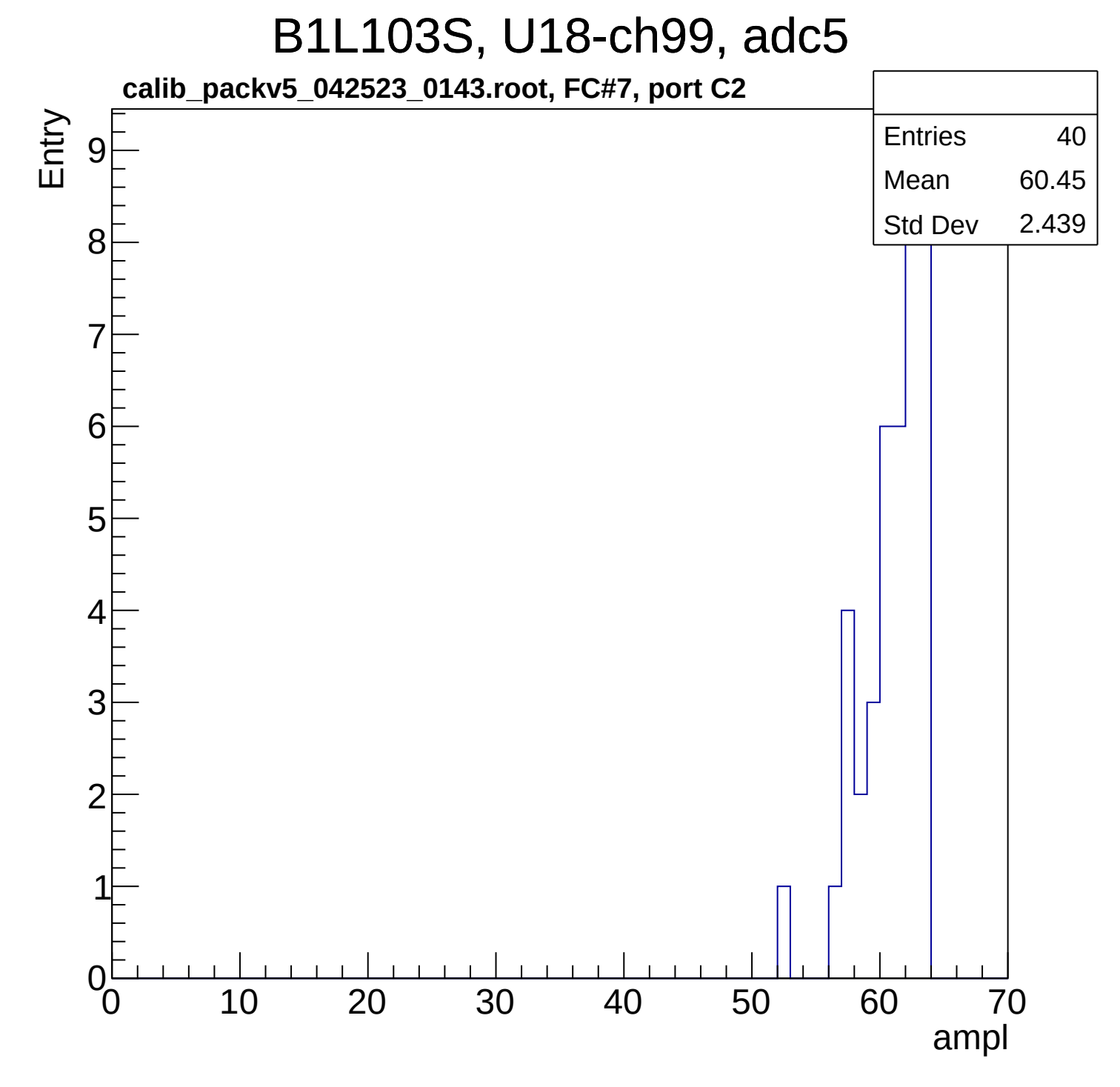

B1L103S, U18-ch99, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 56.49
Std Dev 3.717
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch99, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 40
Mean 60.45
Std Dev 2.439
Entry
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3
4
5
6
7
8
9
0
10
20
30
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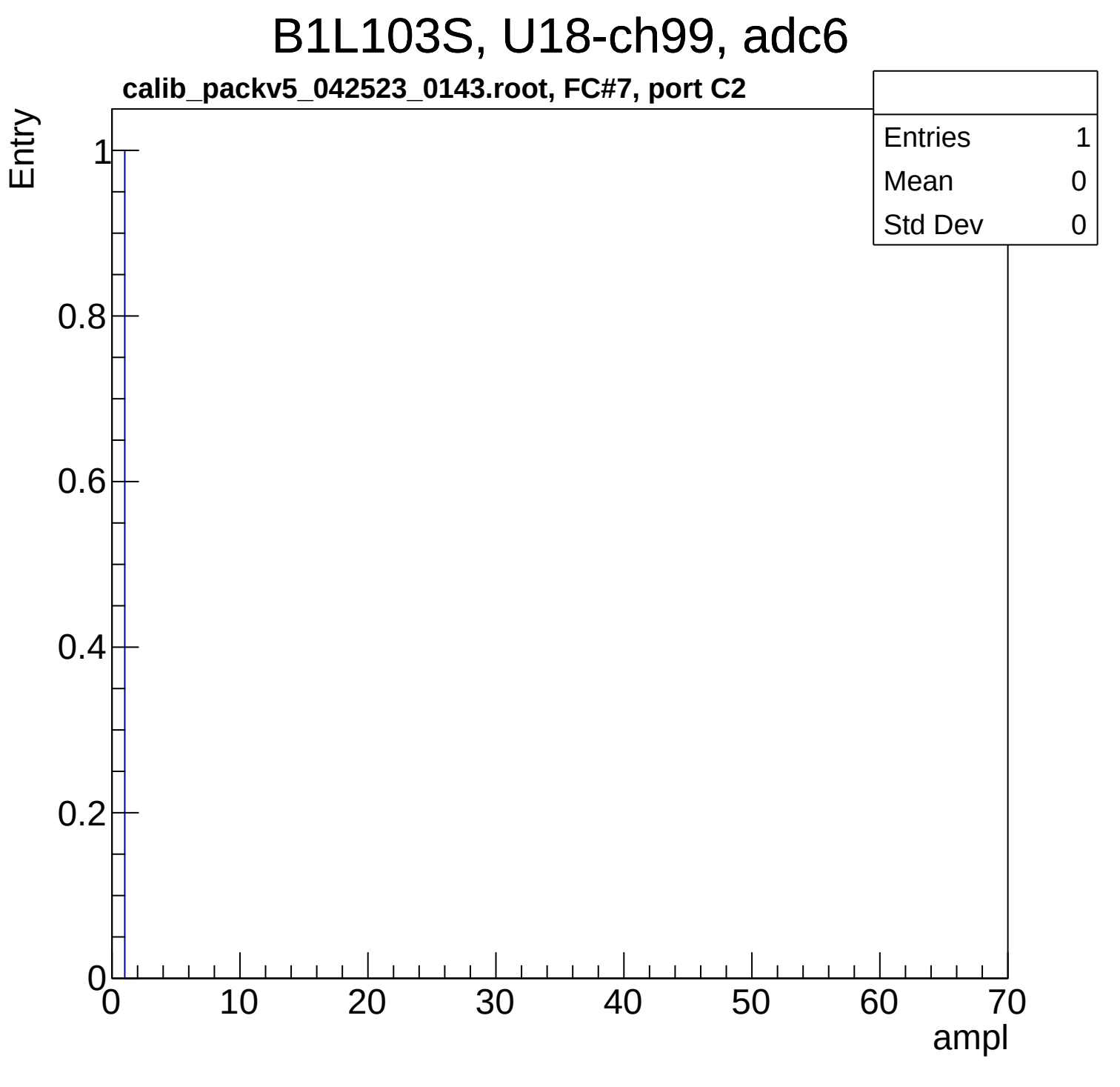
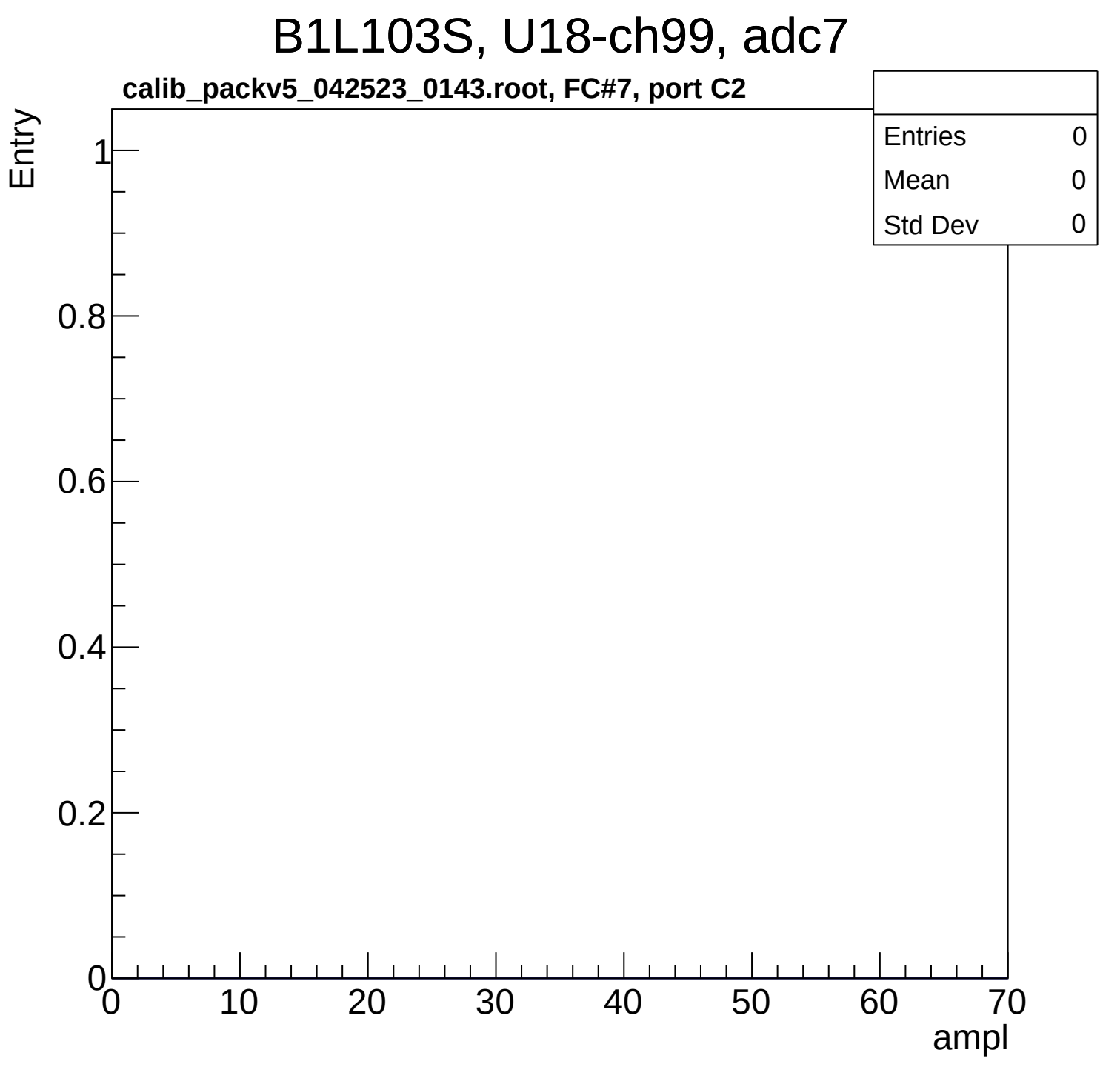
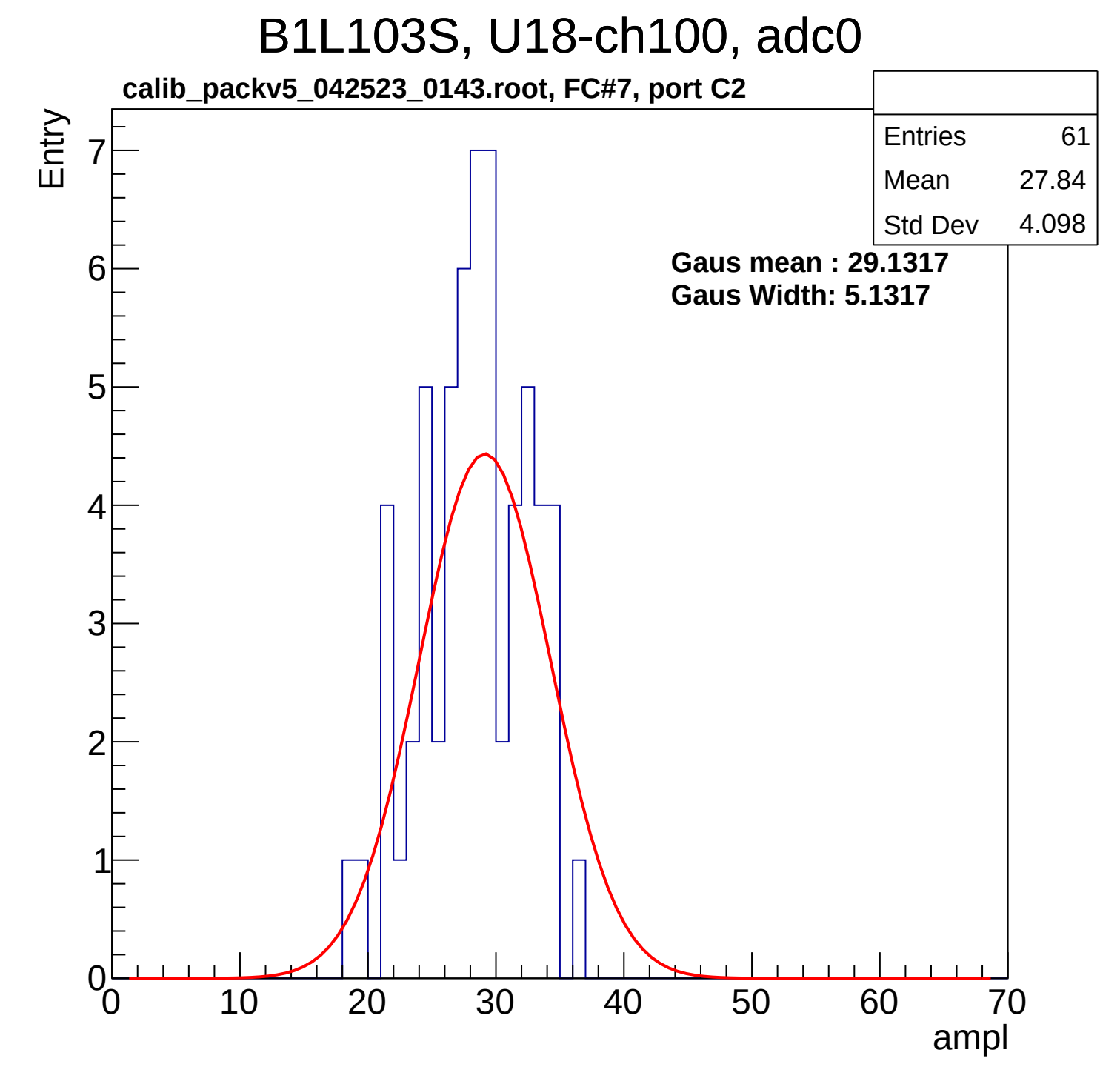
50
60
70
ampl


B1L103S, U18-ch99, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch99, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch100, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 61
Mean 27.84
Std Dev 4.098
Gaus mean : 29.1317
Gaus Width: 5.1317
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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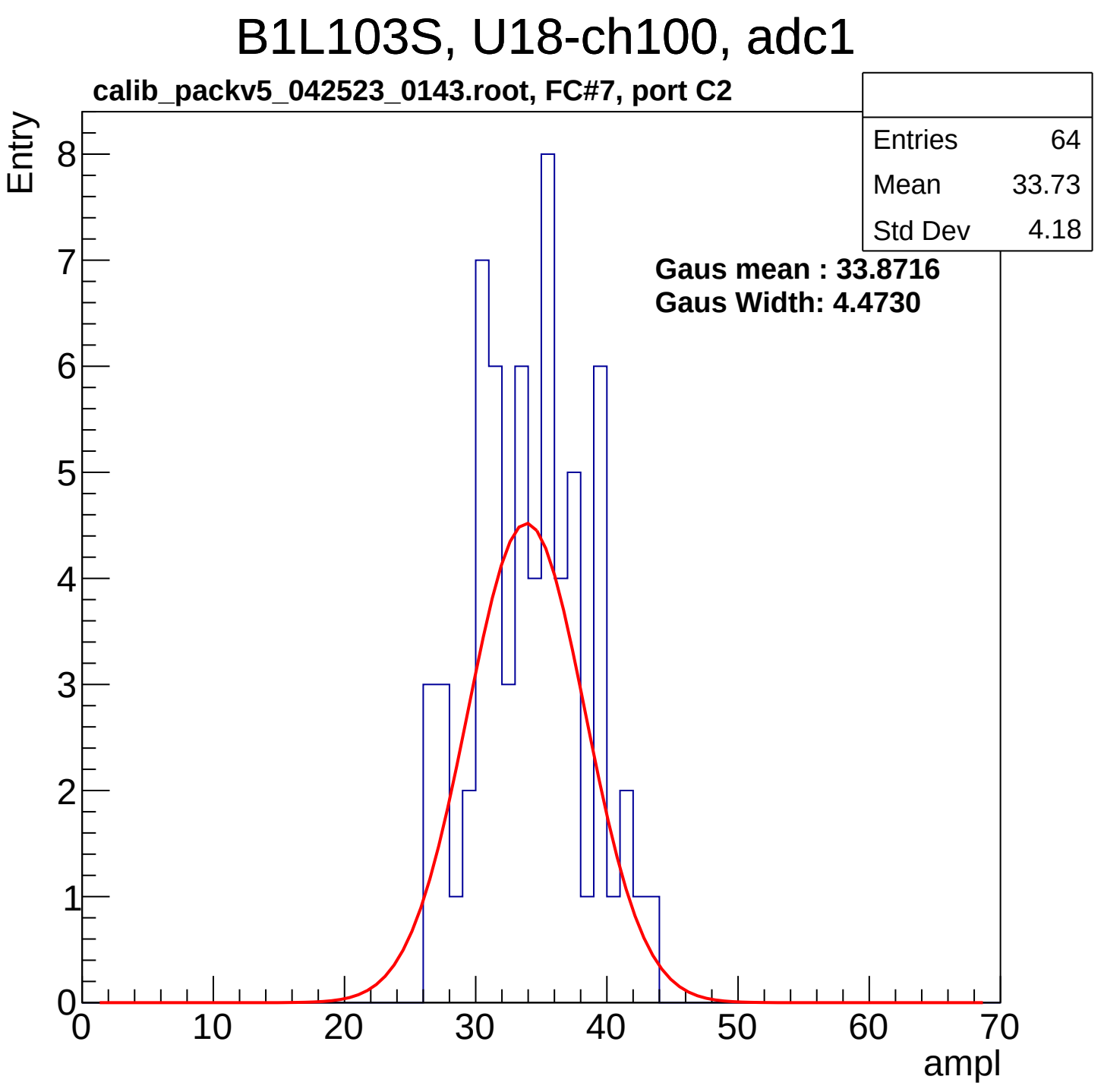
B1L103S, U18-ch100, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 33.73
Std Dev 4.18
Gaus mean : 33.8716
Gaus Width: 4.4730
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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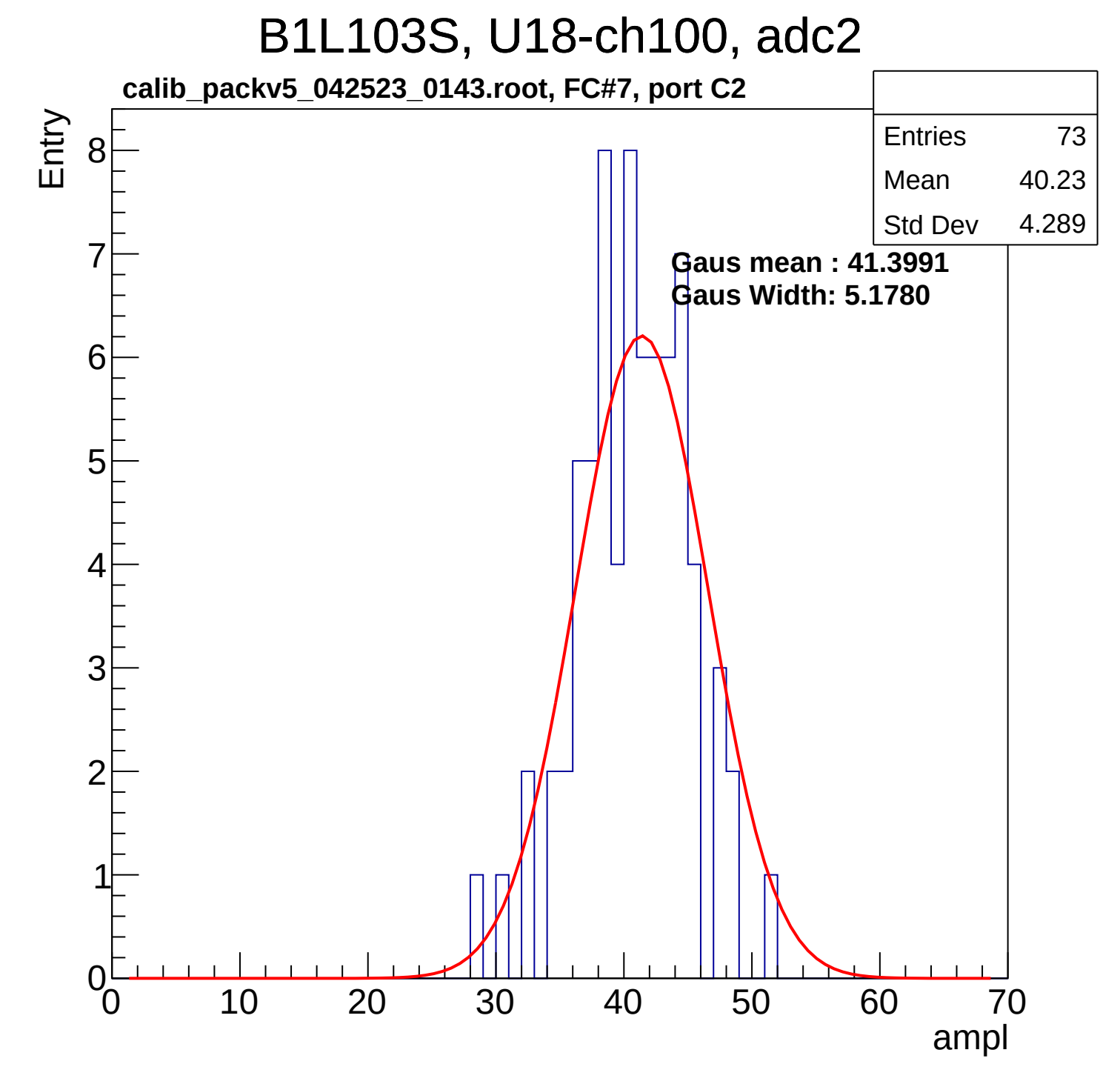
B1L103S, U18-ch100, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 73
Mean 40.23
Std Dev 4.289
Gaus mean : 41.3991
Gaus Width: 5.1780
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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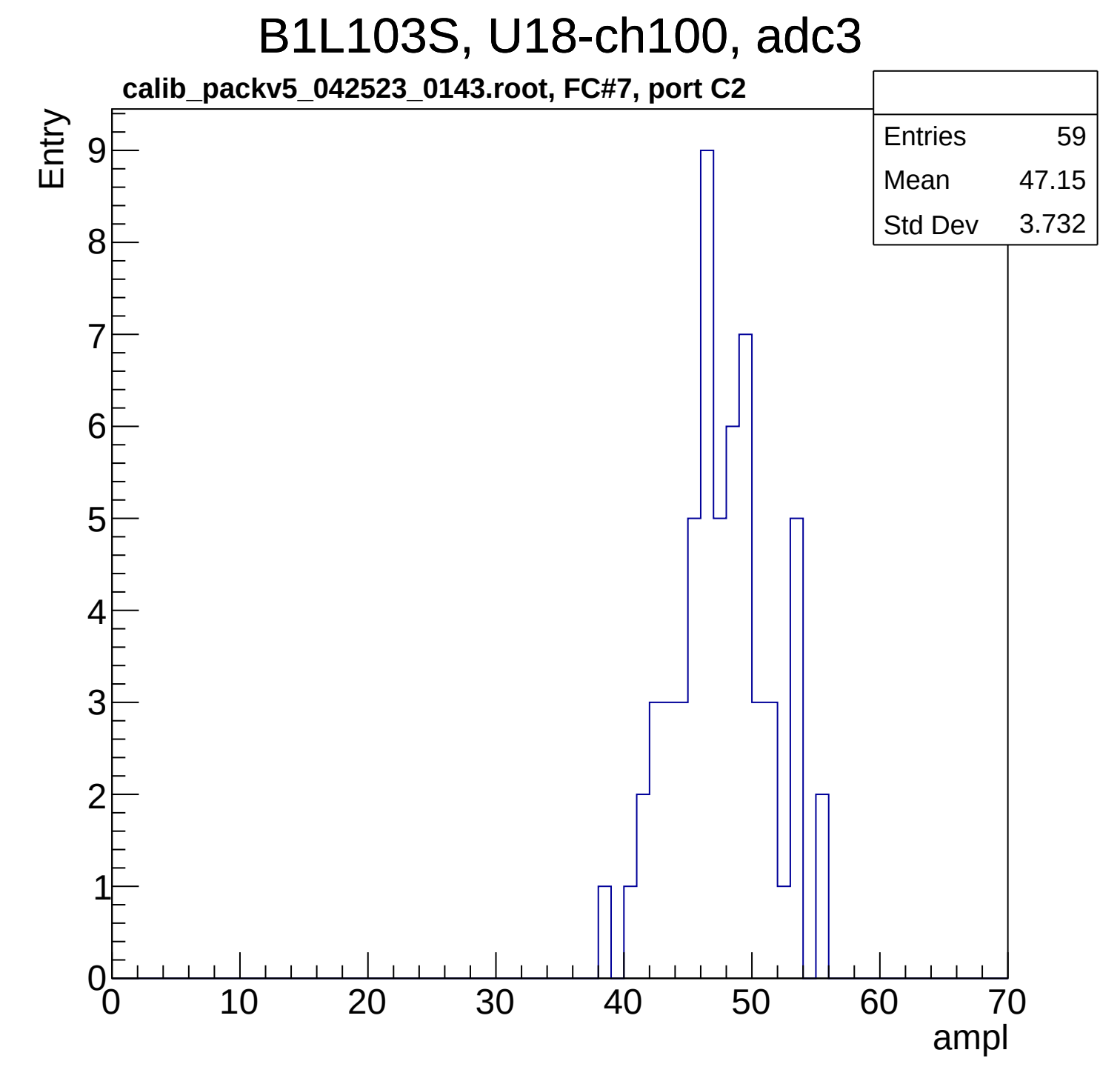
B1L103S, U18-ch100, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 47.15
Std Dev 3.732
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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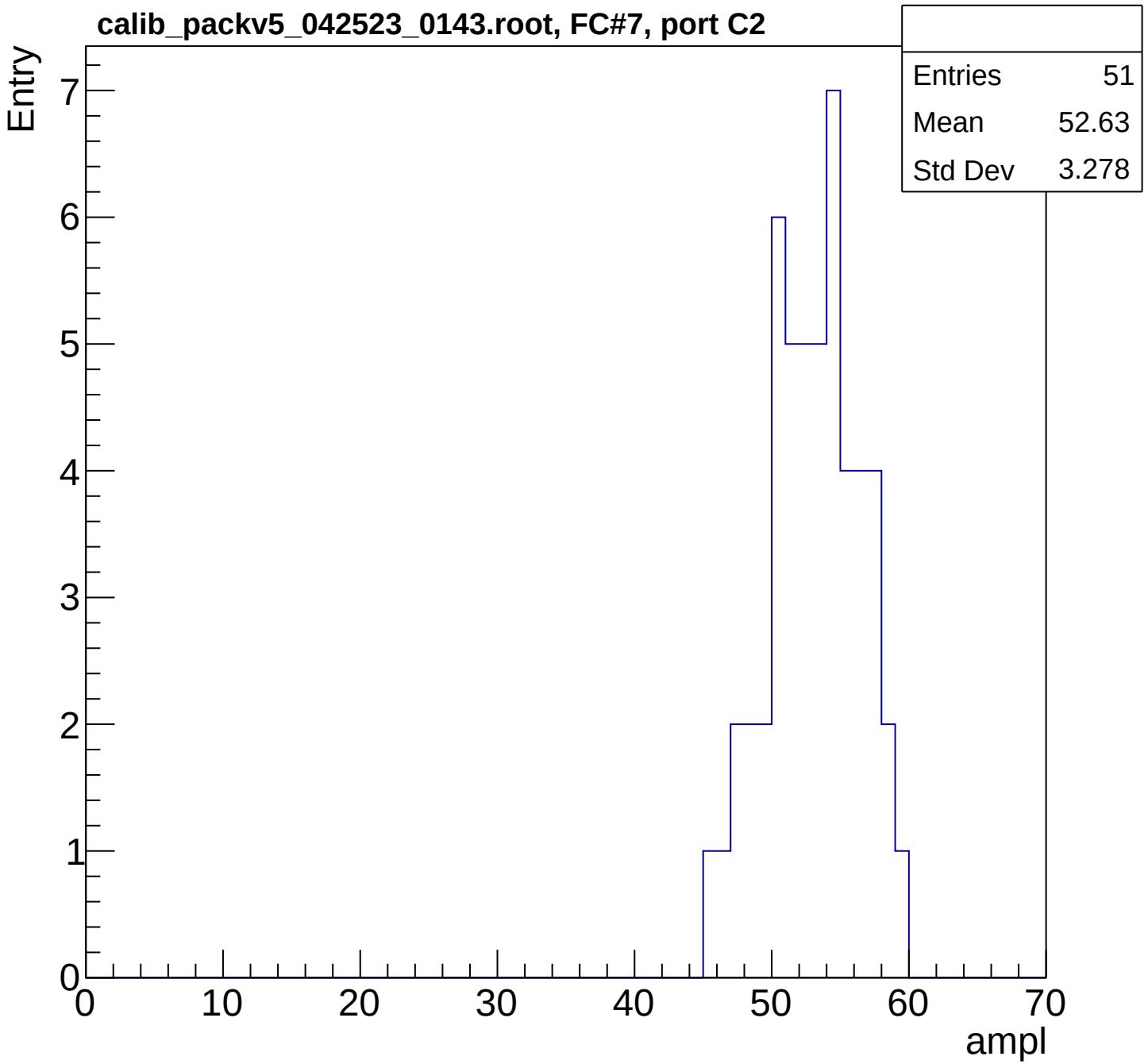
B1L103S, U18-ch100, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 51
Mean 52.63
Std Dev 3.278
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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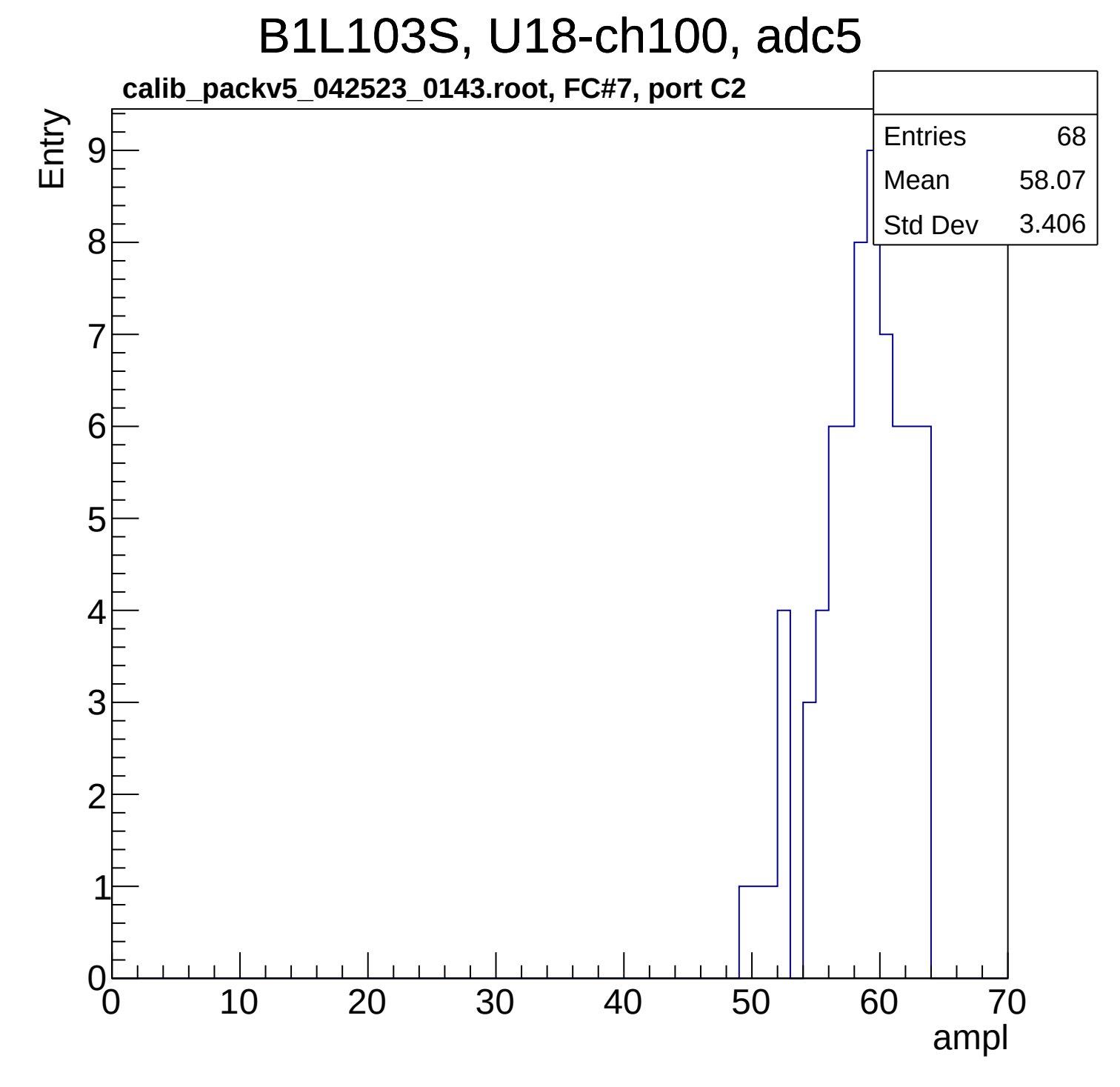
B1L103S, U18-ch100, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 58.07
Std Dev 3.406
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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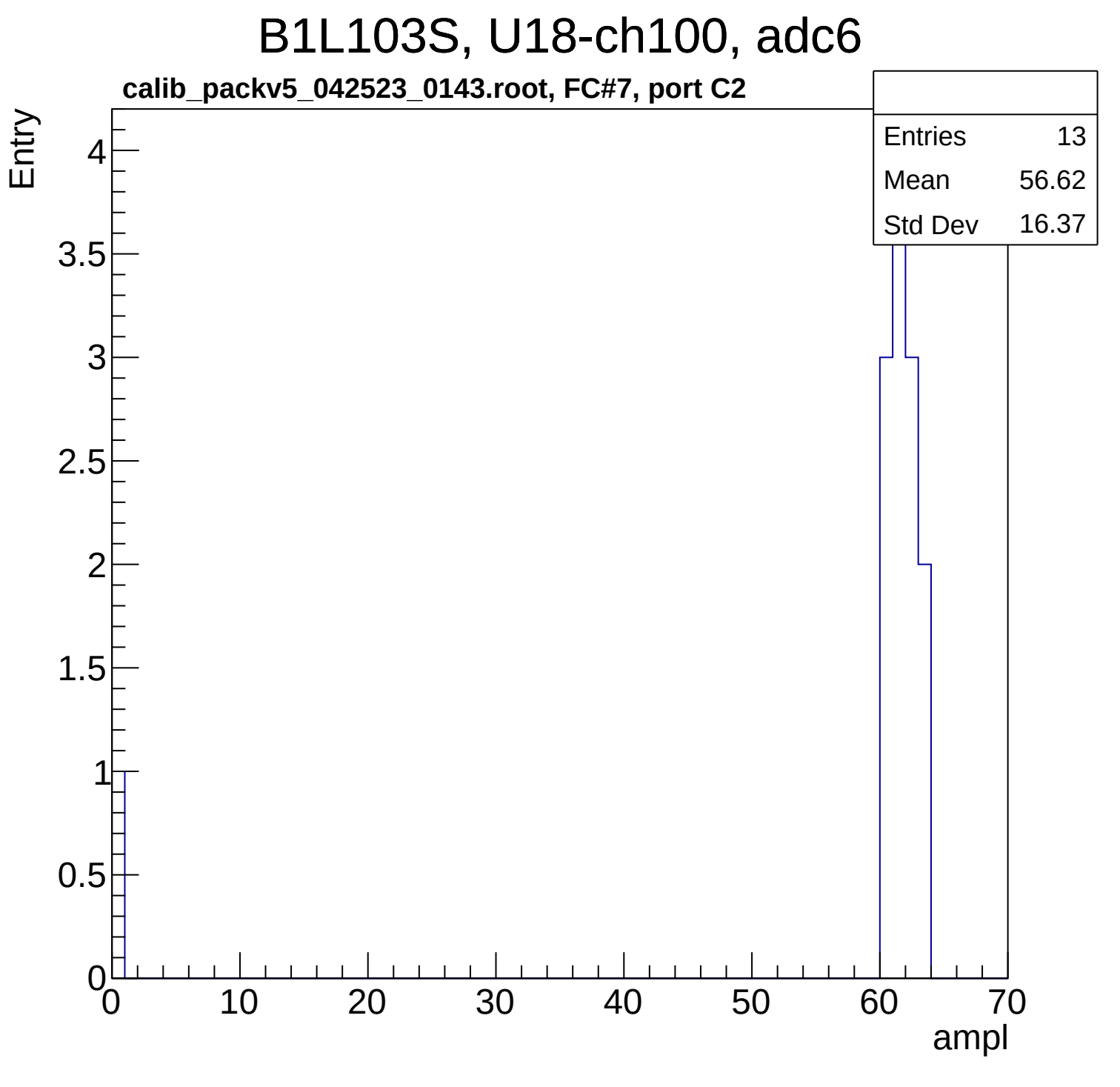
B1L103S, U18-ch100, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 13
Mean 56.62
Std Dev 16.37
Entry
ampl
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0.5
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1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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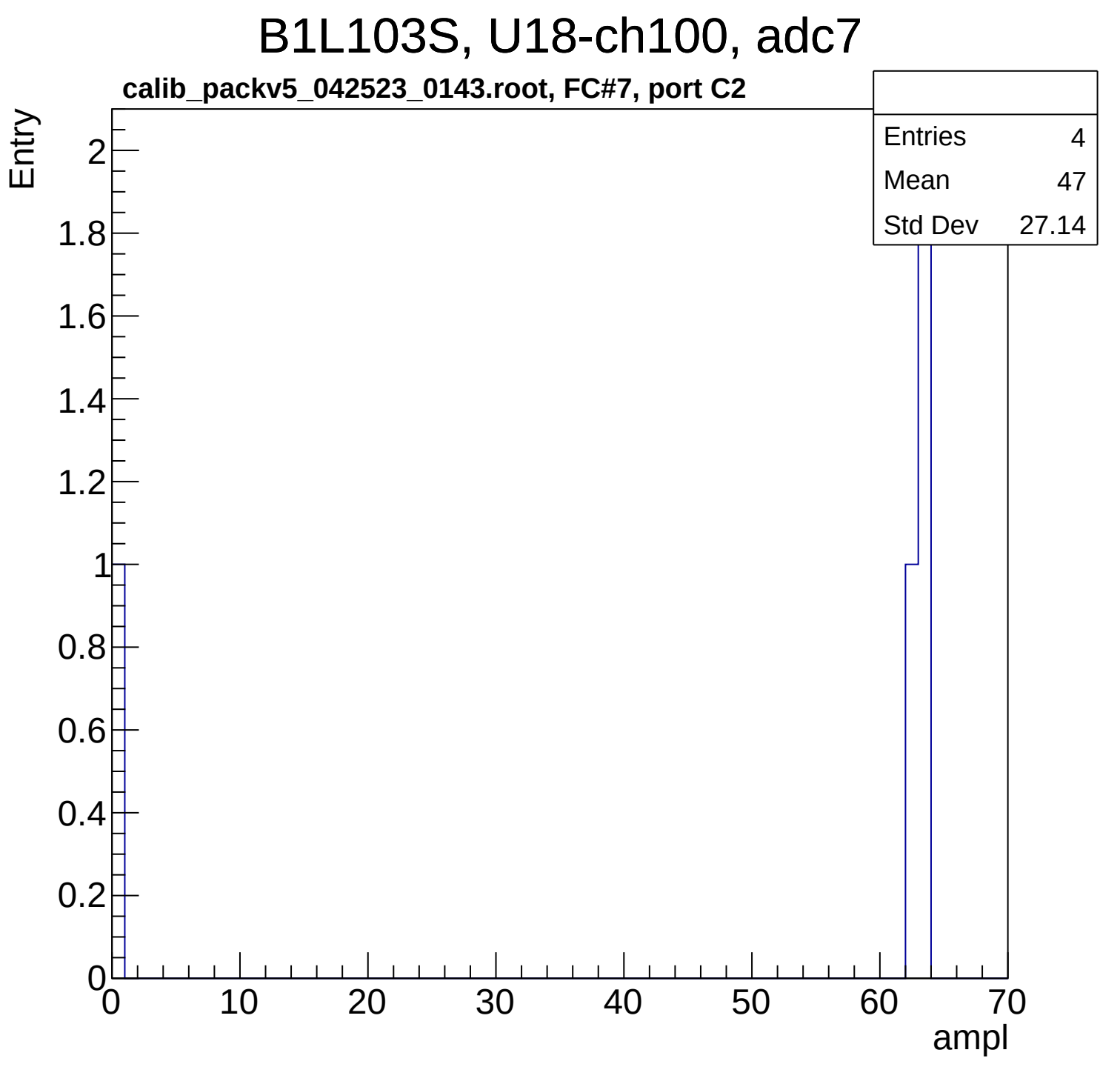
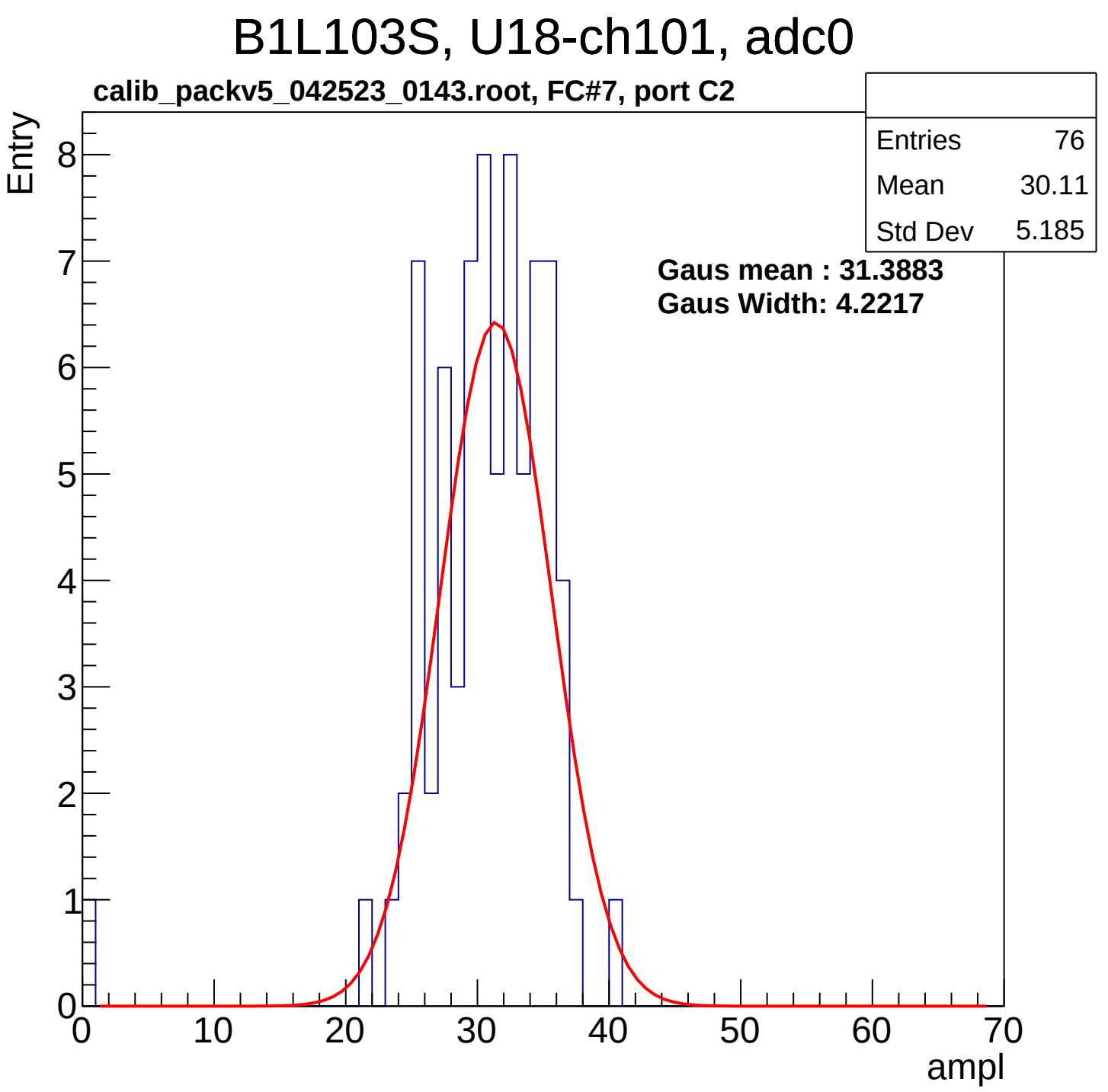
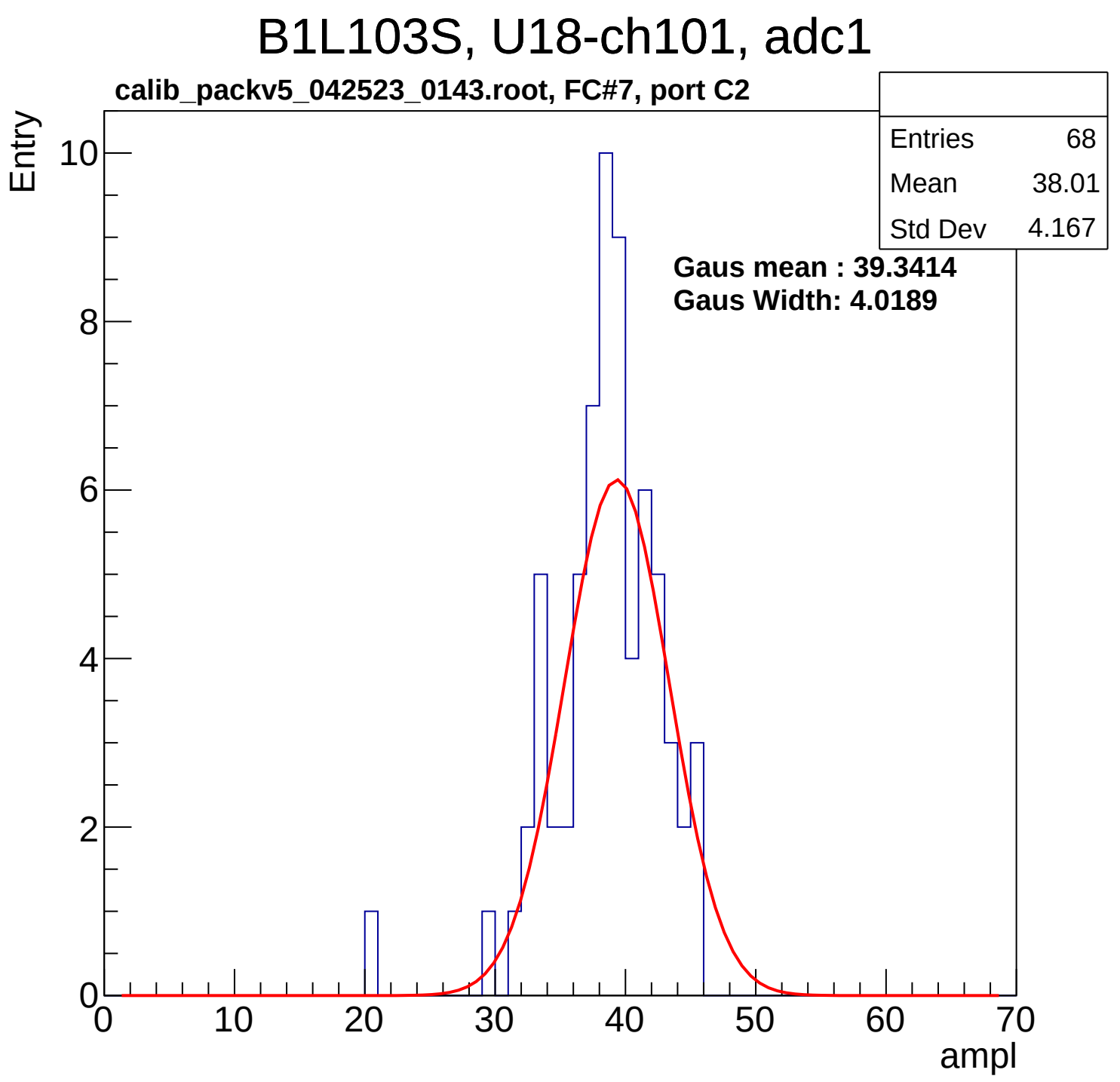
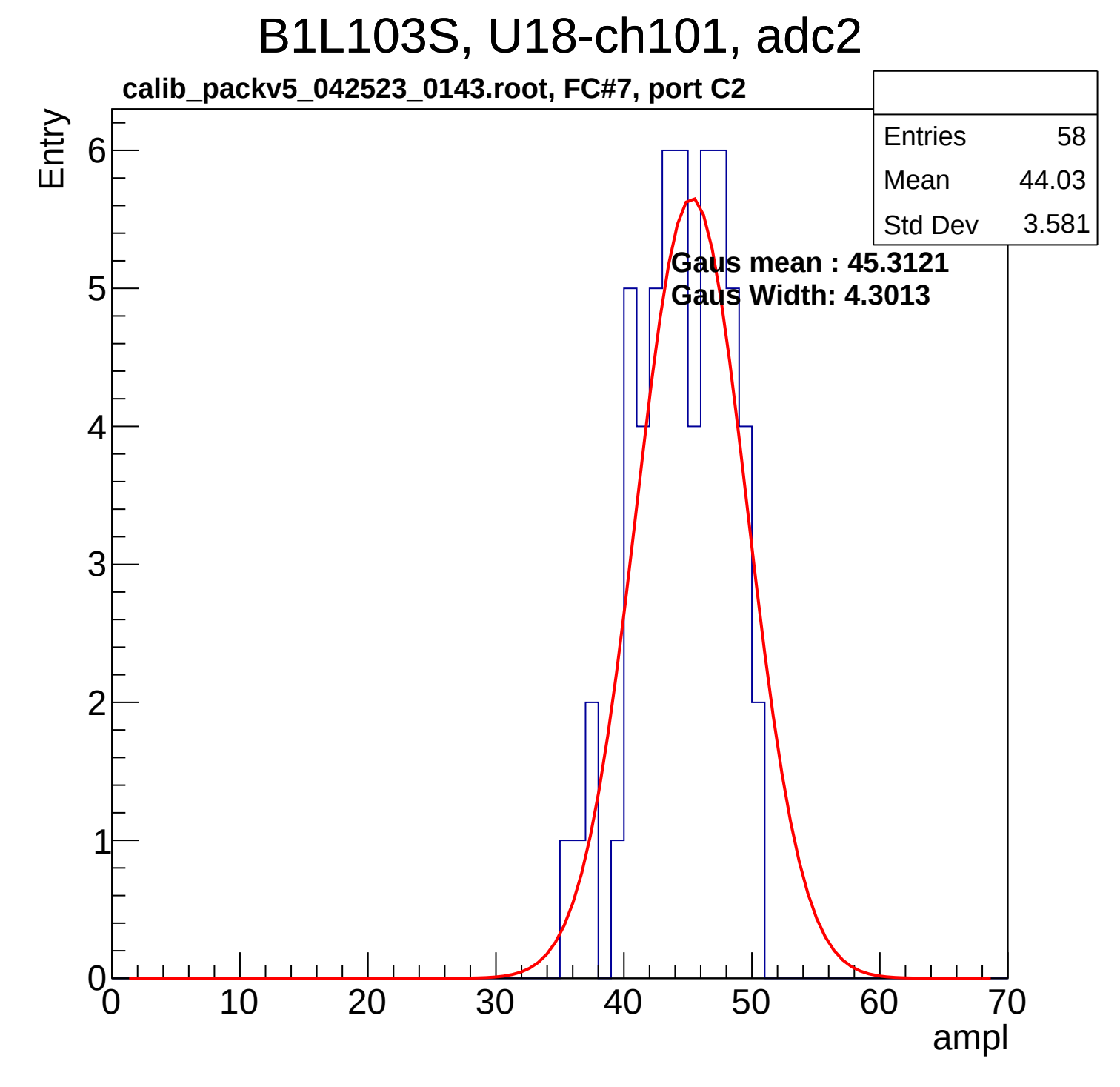

B1L103S, U18-ch100, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 4
Mean 47
Std Dev 27.14
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U18-ch101, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 76
Mean 30.11
Std Dev 5.185
Gaus mean : 31.3883
Gaus Width: 4.2217
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch101, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 38.01
Std Dev 4.167
Gaus mean : 39.3414
Gaus Width: 4.0189
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch101, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 58
Mean 44.03
Std Dev 3.581
Gaus mean : 45.3121
Gaus Width: 4.3013
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
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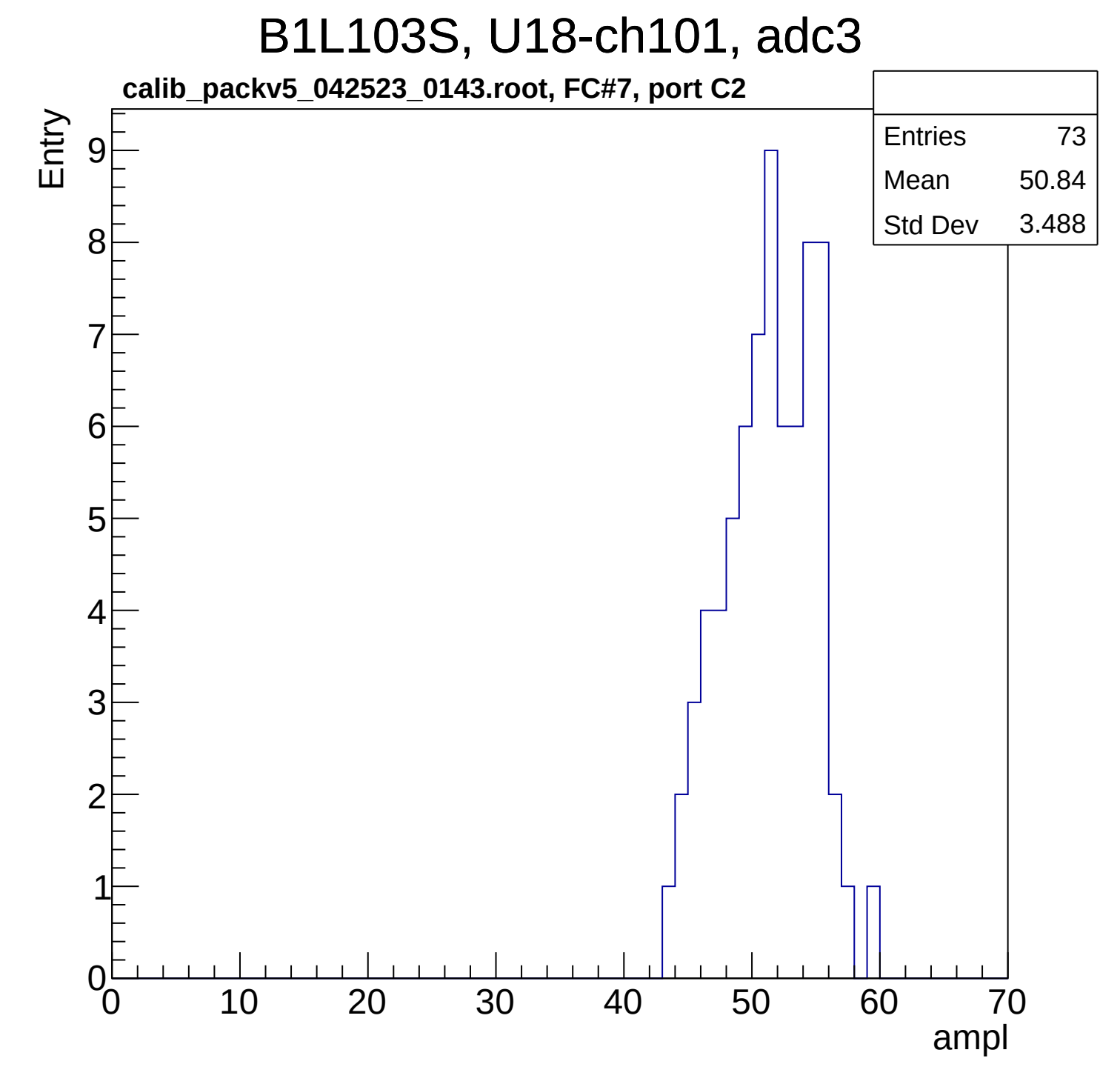
B1L103S, U18-ch101, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 73
Mean 50.84
Std Dev 3.488
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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20
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40
50
60
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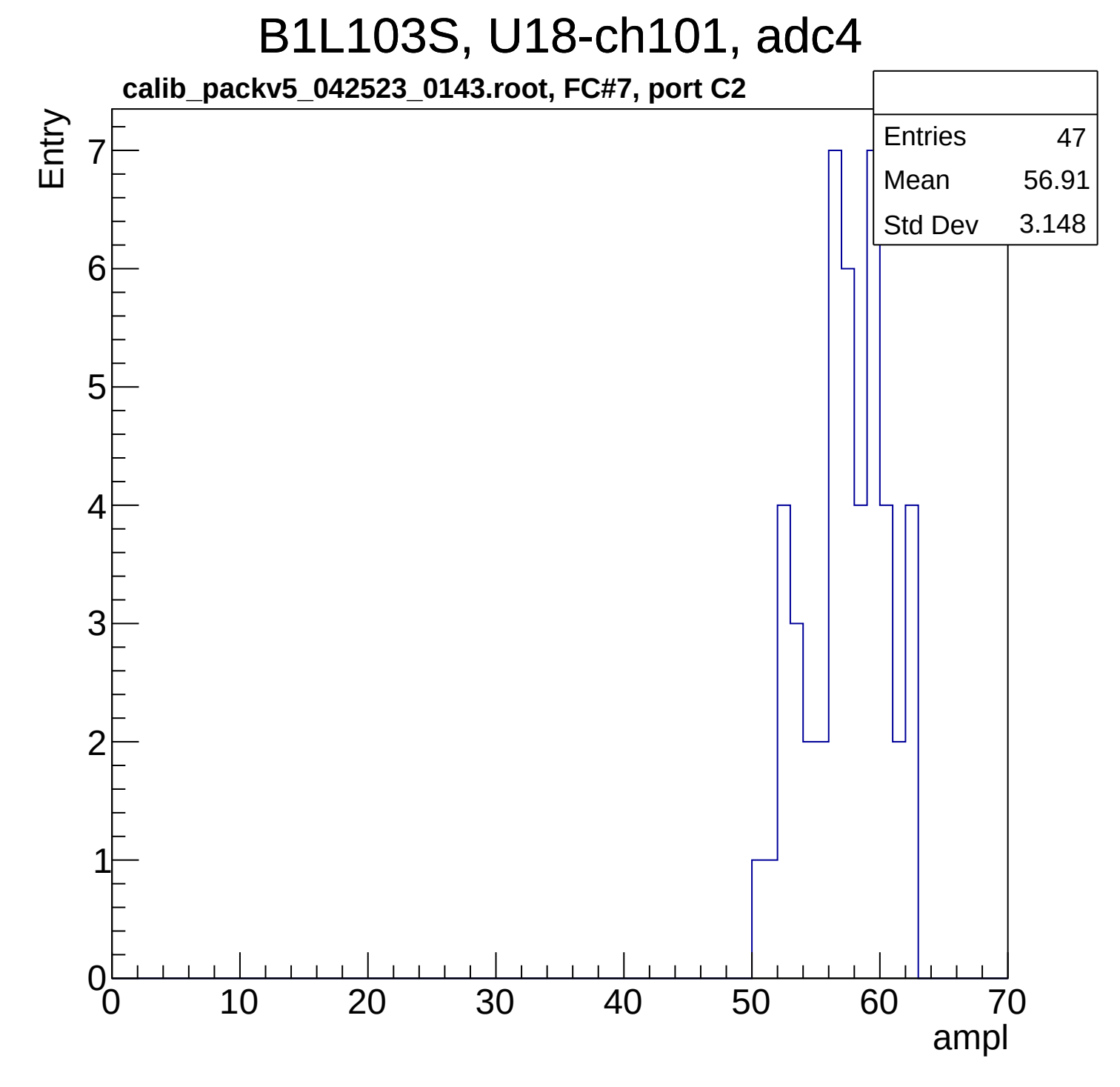
B1L103S, U18-ch101, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 47
Mean 56.91
Std Dev 3.148
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
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60
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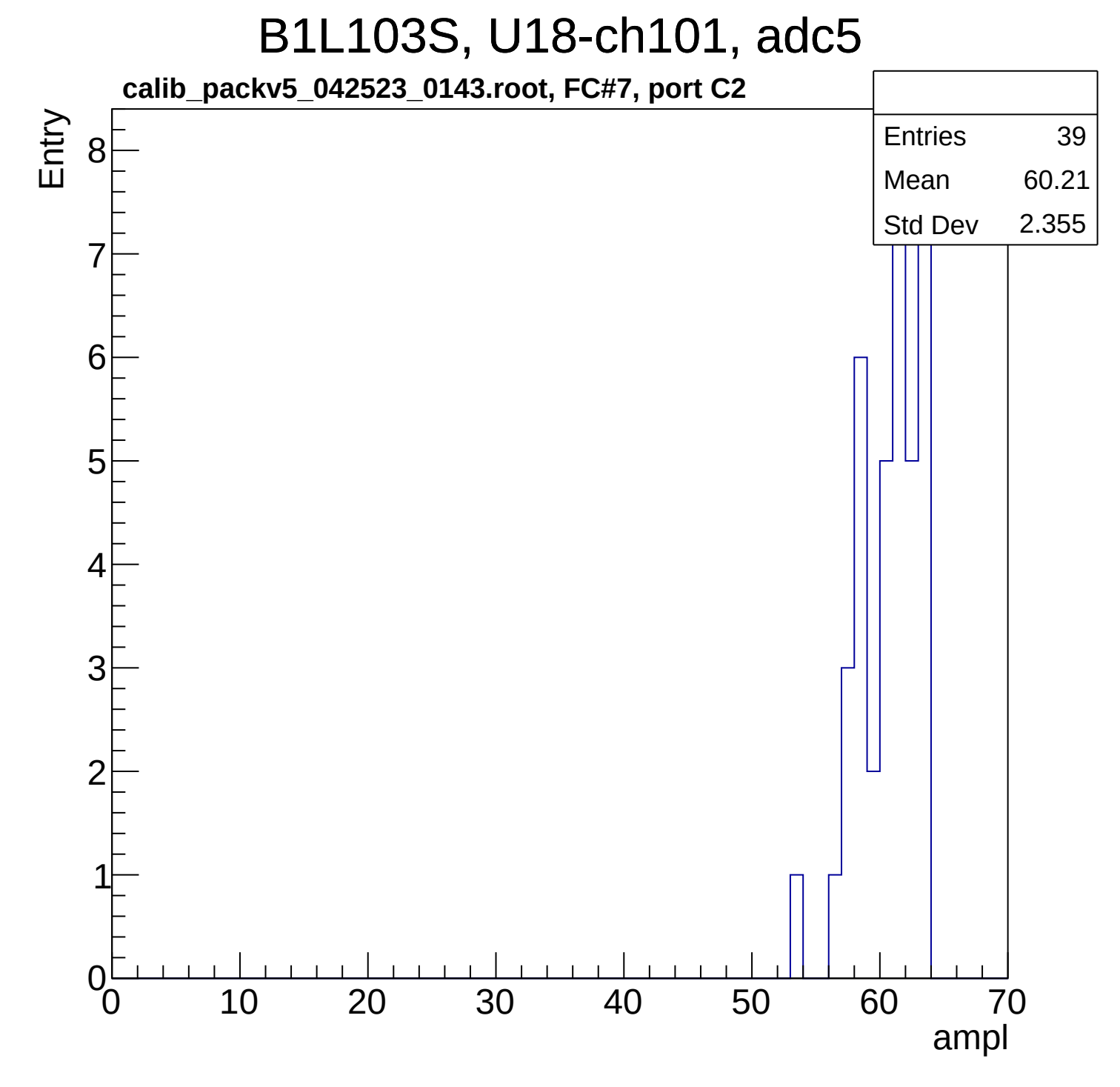
B1L103S, U18-ch101, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 39
Mean 60.21
Std Dev 2.355
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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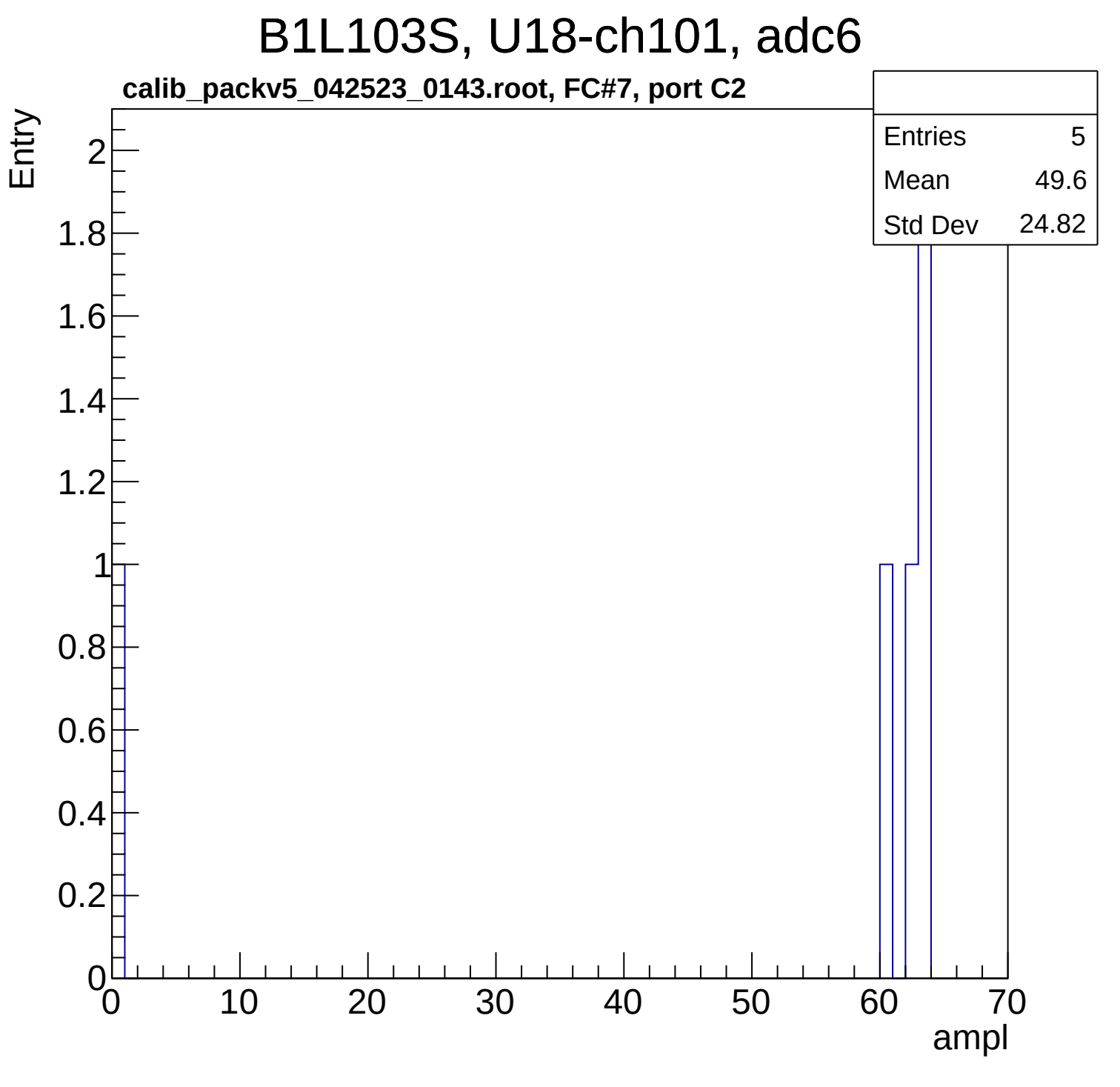
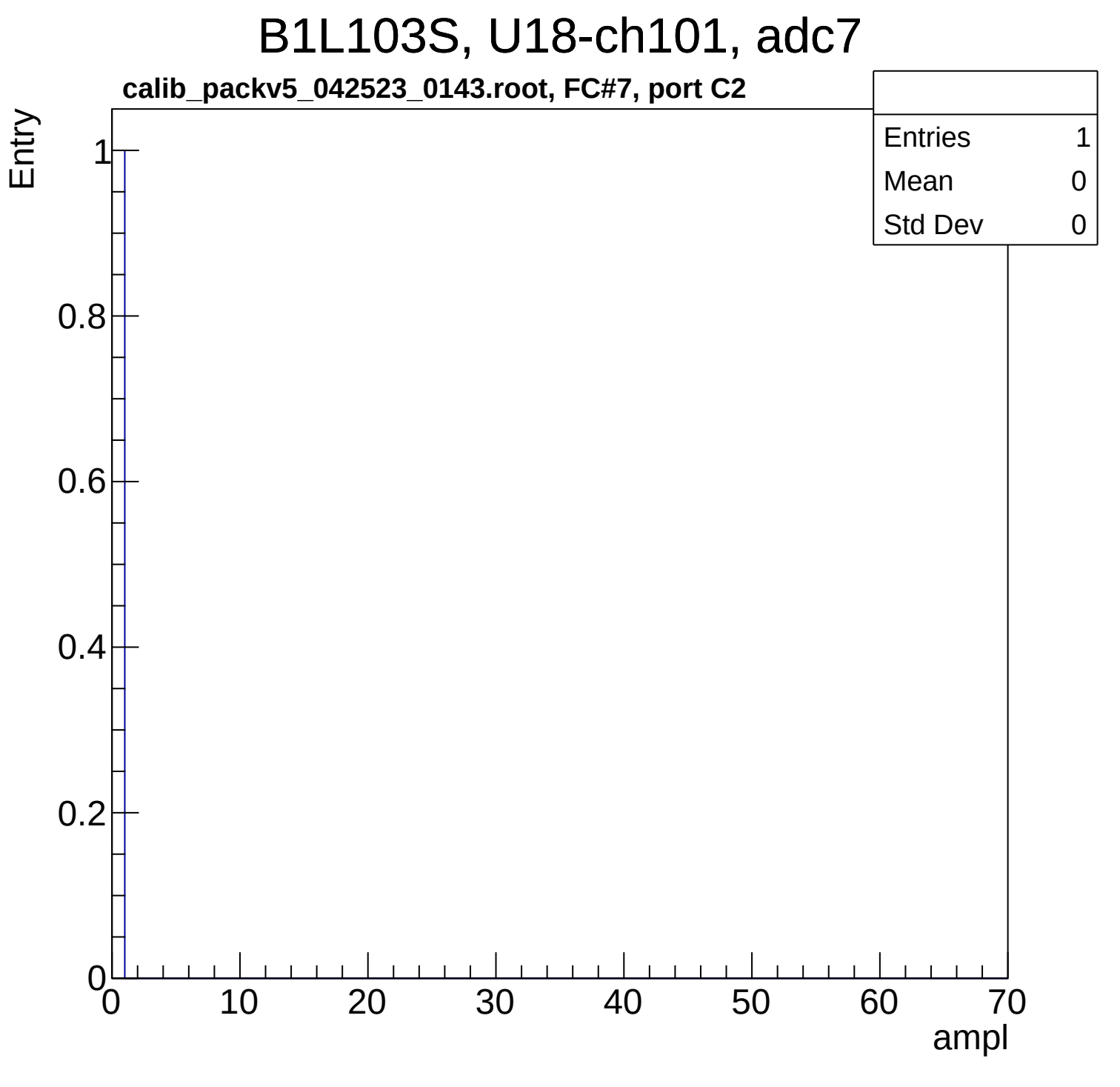
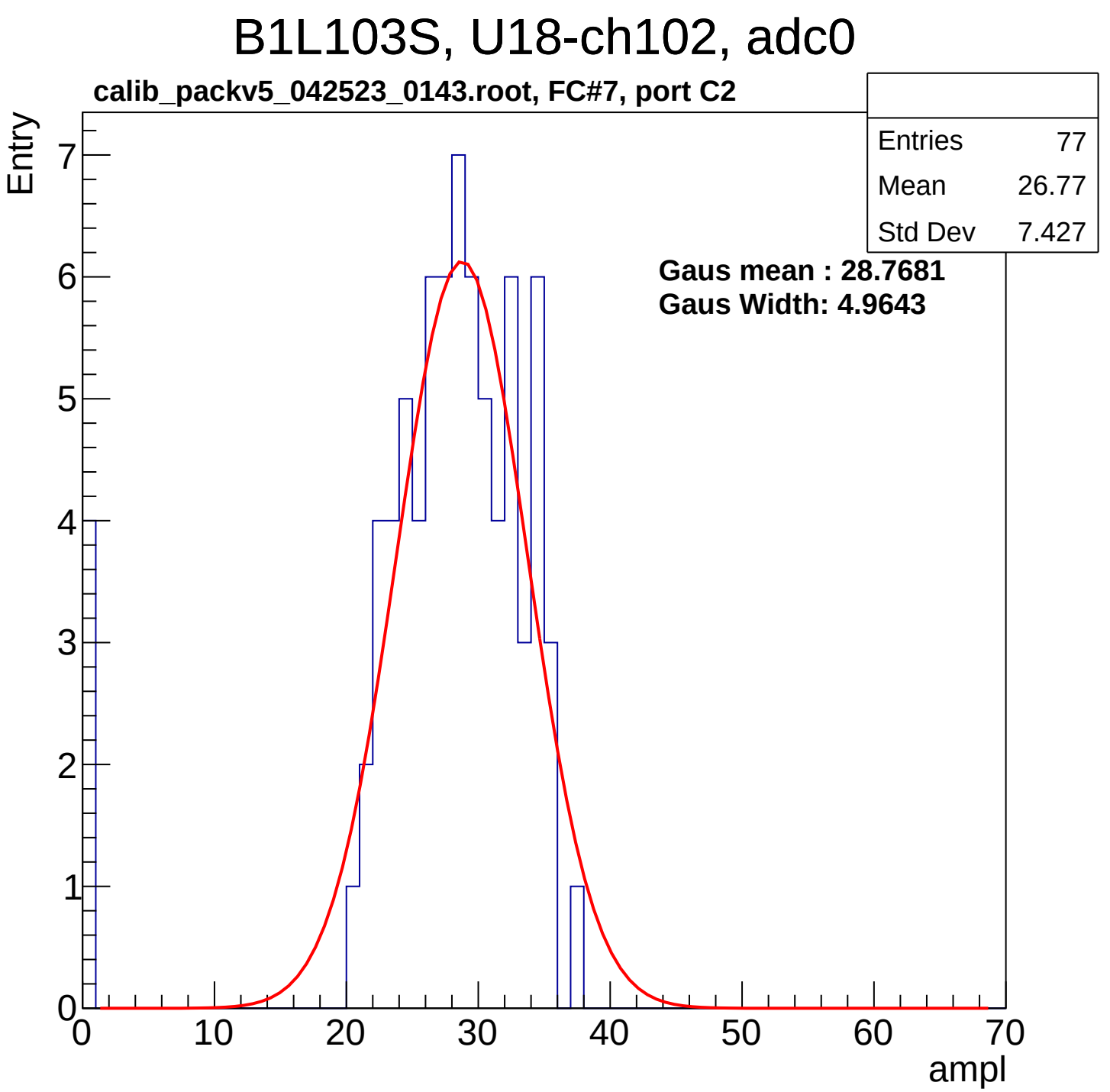
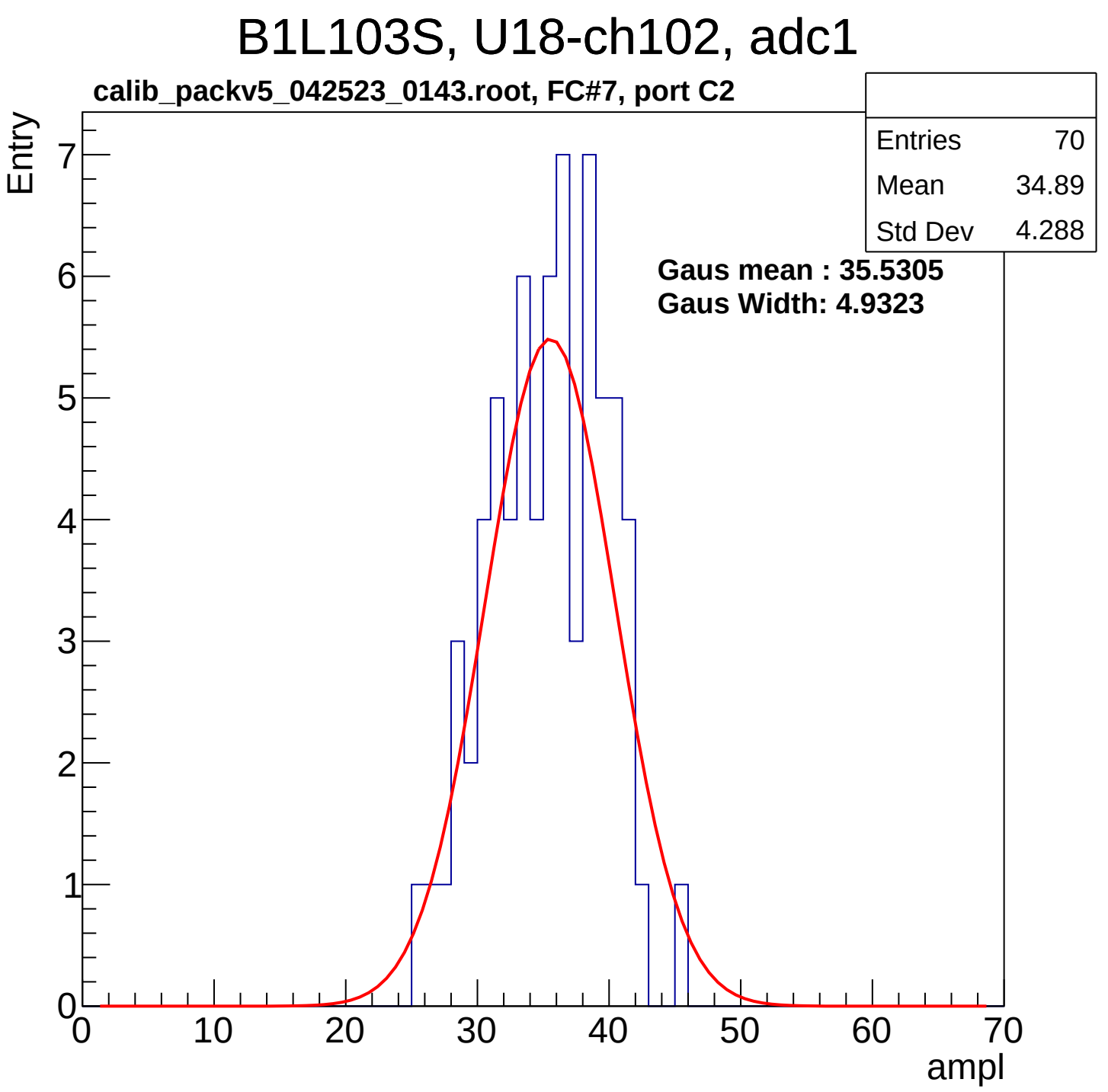

B1L103S, U18-ch101, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 5
Mean 49.6
Std Dev 24.82
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U18-ch101, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch102, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 77
Mean 26.77
Std Dev 7.427
Gaus mean : 28.7681
Gaus Width: 4.9643
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch102, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 34.89
Std Dev 4.288
Gaus mean : 35.5305
Gaus Width: 4.9323
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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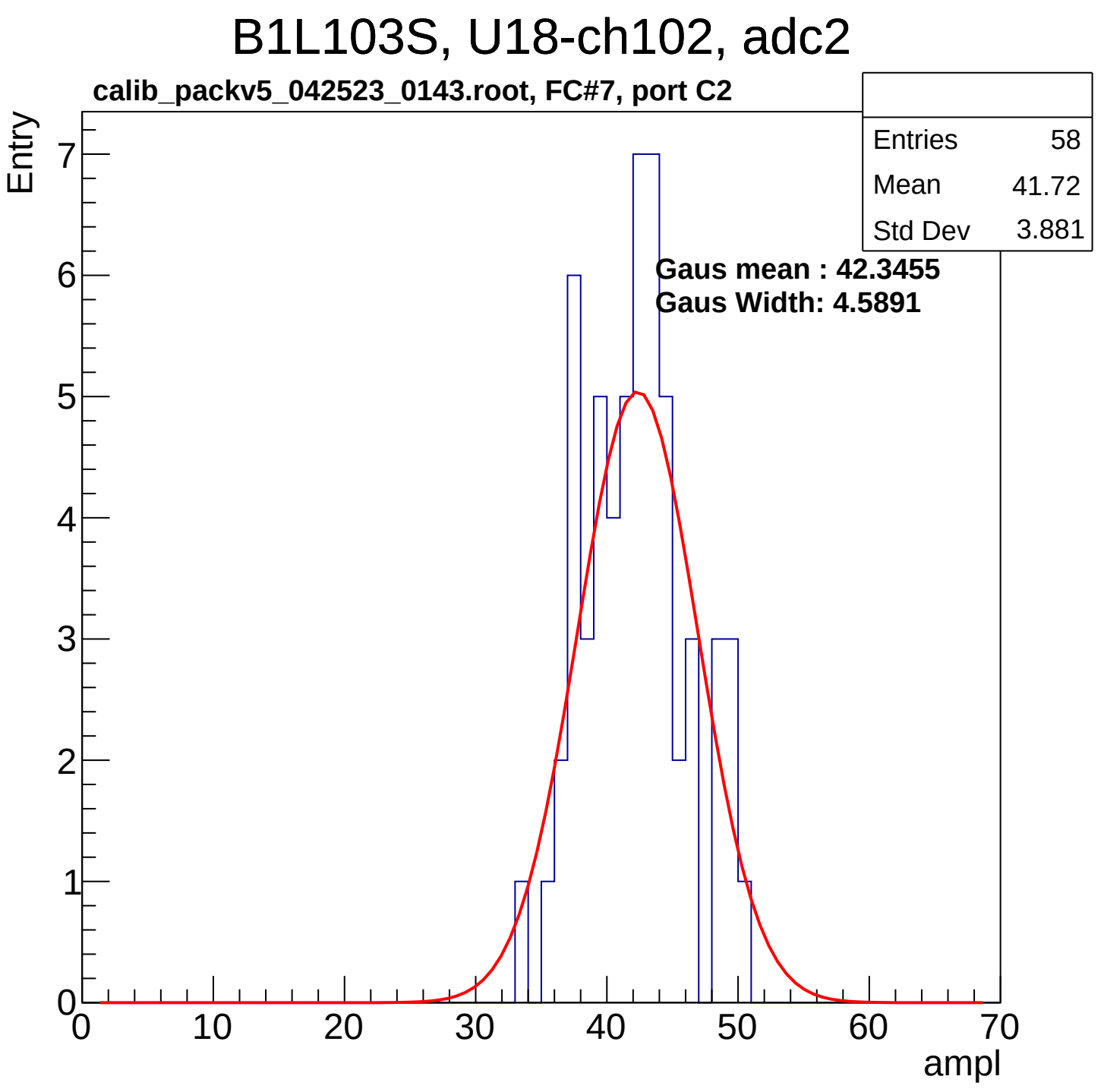
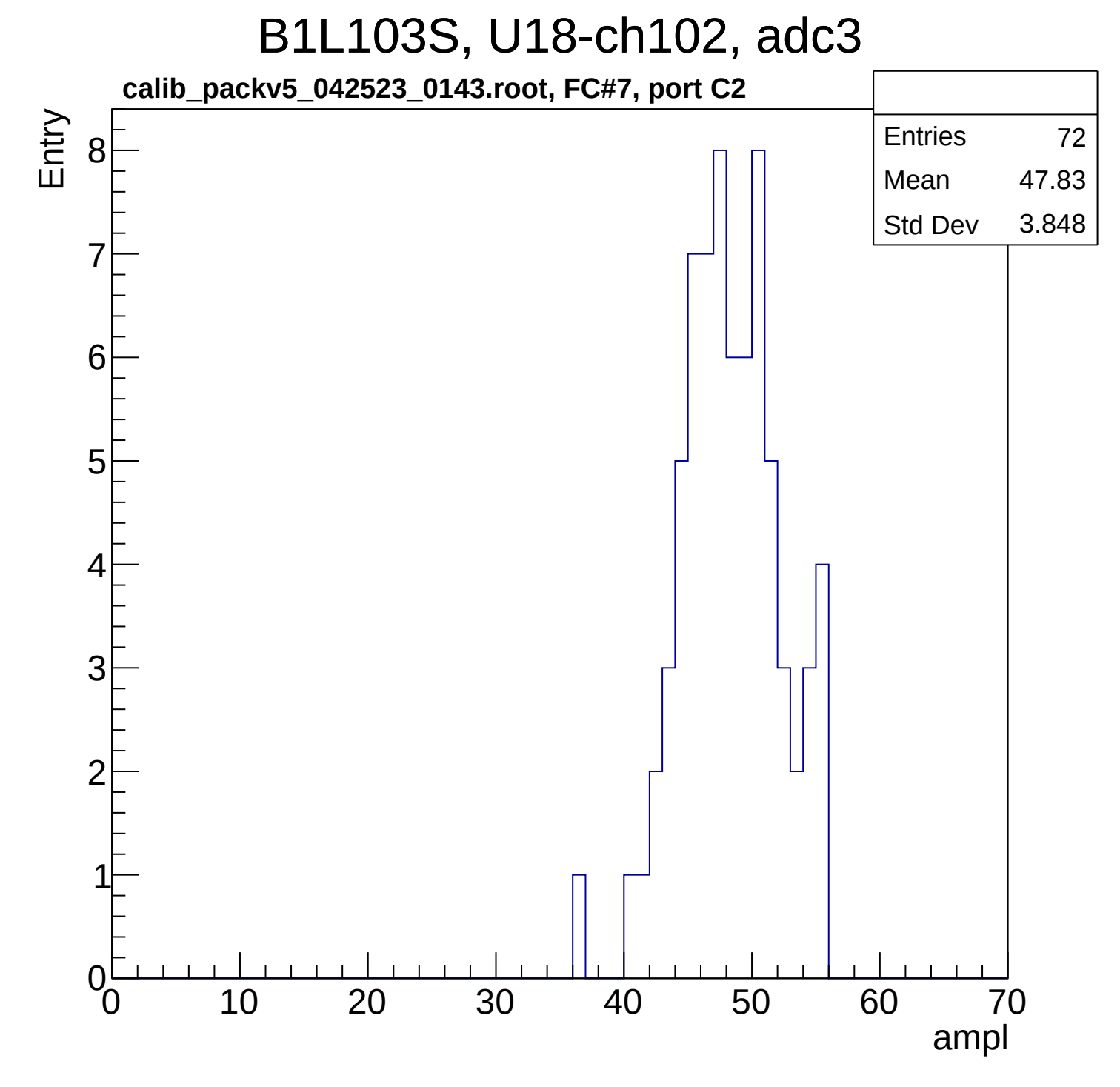

B1L103S, U18-ch102, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 58
Mean 41.72
Std Dev 3.881
Gaus mean : 42.3455
Gaus Width: 4.5891
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch102, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 72
Mean 47.83
Std Dev 3.848
Entry
ampl
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2
3
4
5
6
7
8
0
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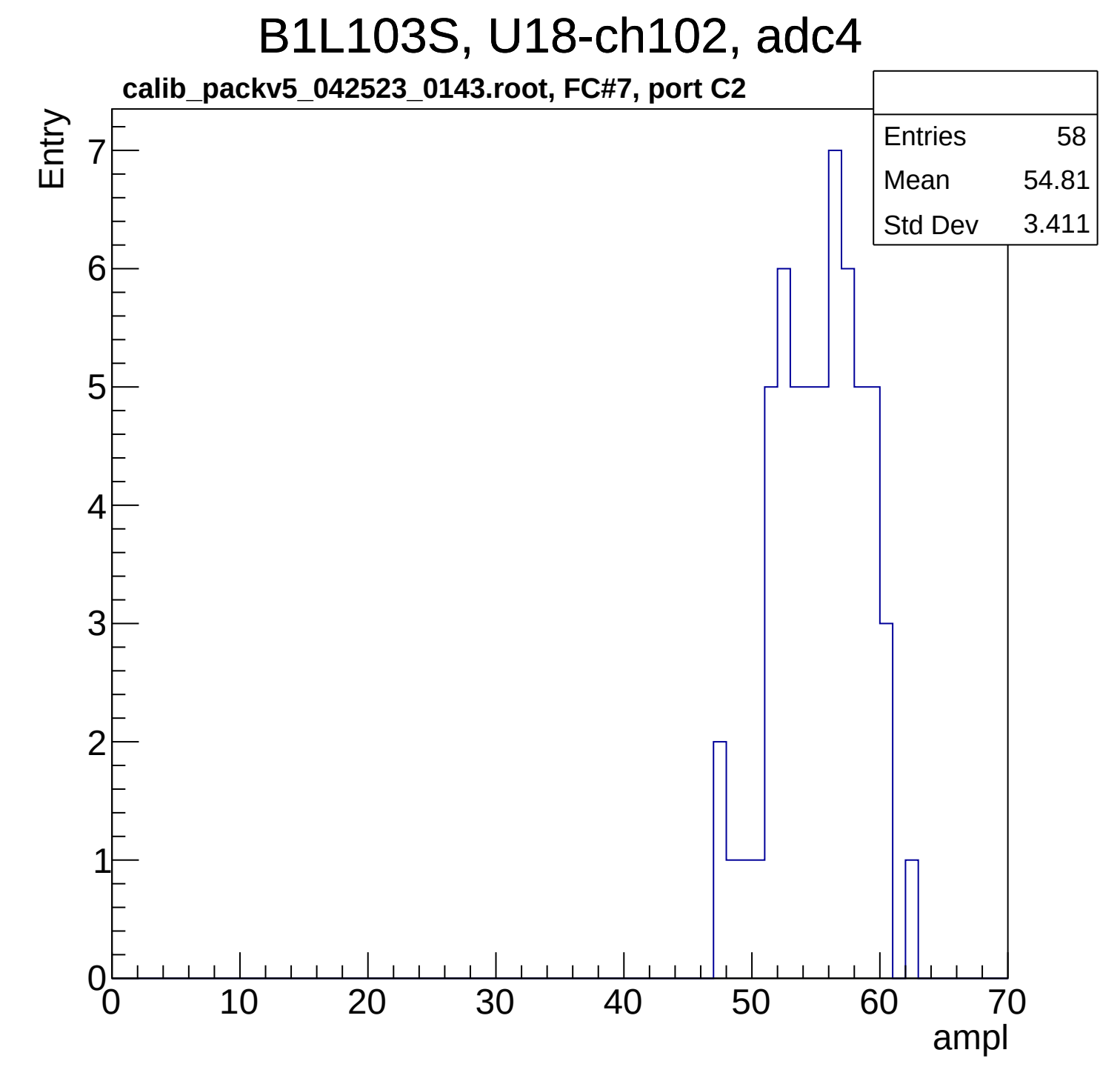
20
30
40
50
60
70


B1L103S, U18-ch102, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 58
Mean 54.81
Std Dev 3.411
Entry
ampl
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1
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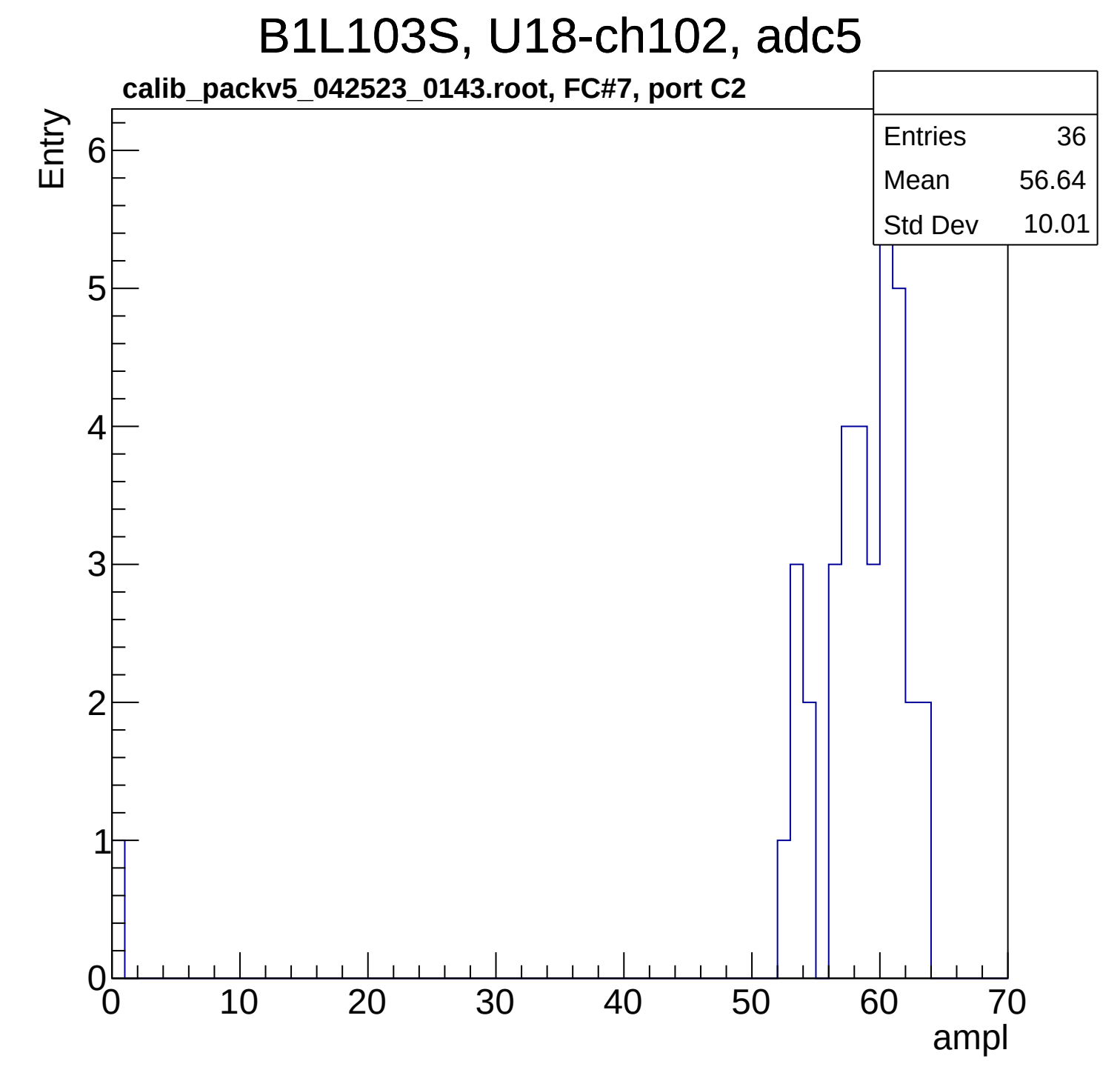
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch102, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 36
Mean 56.64
Std Dev 10.01
Entry
0
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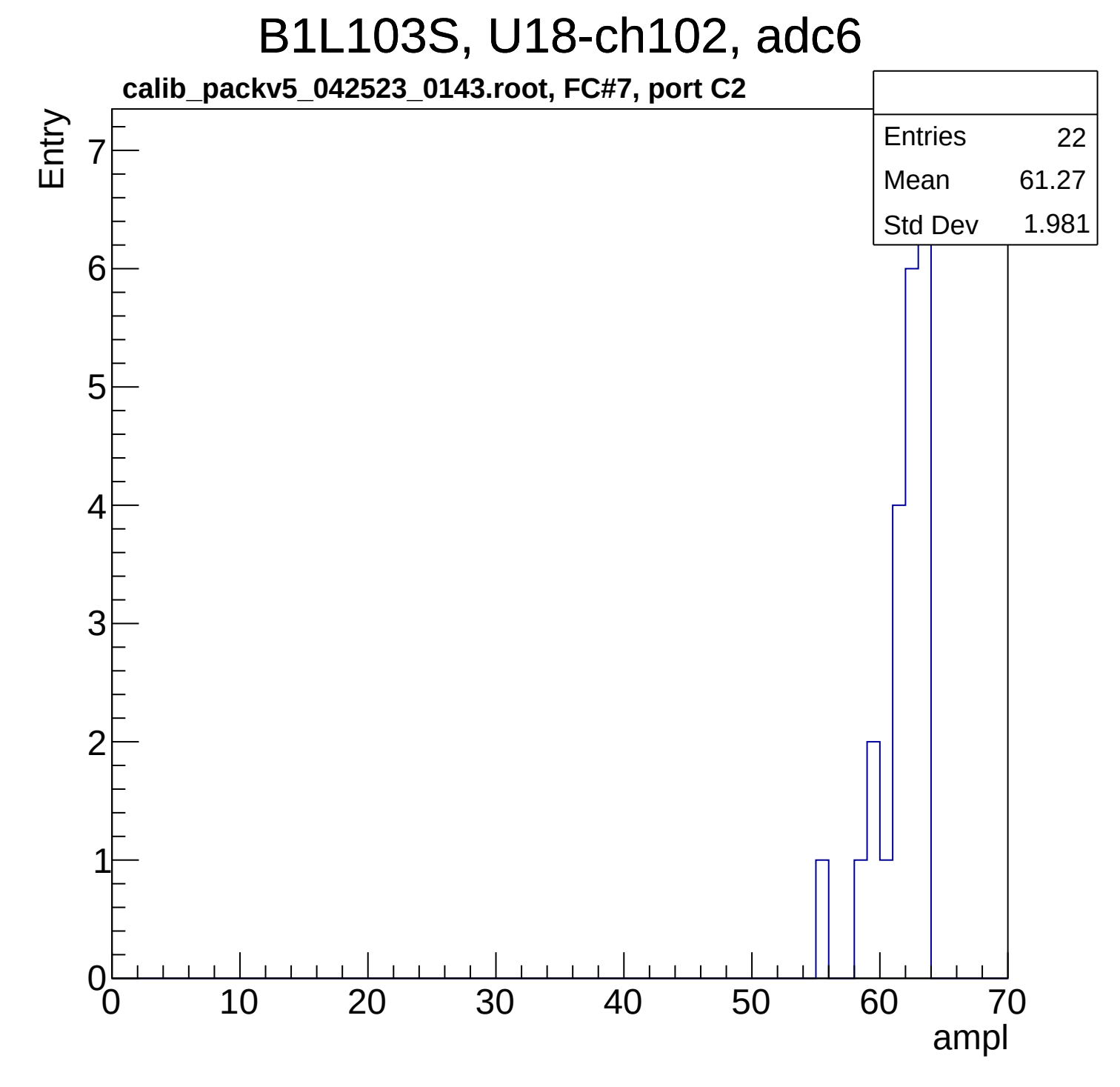
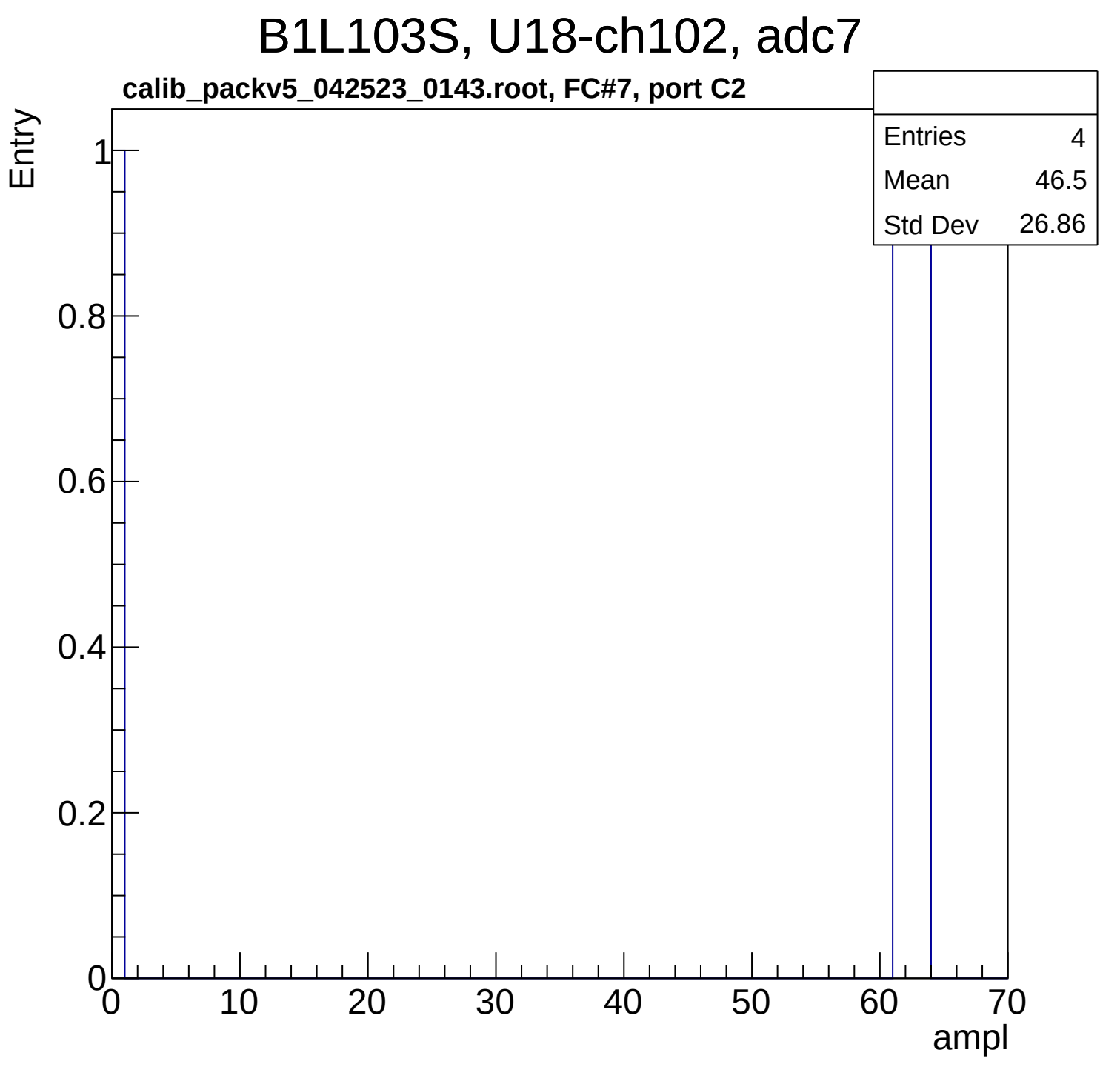
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch102, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 22
Mean 61.27
Std Dev 1.981
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch102, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 4
Mean 46.5
Std Dev 26.86
Entry
ampl
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0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
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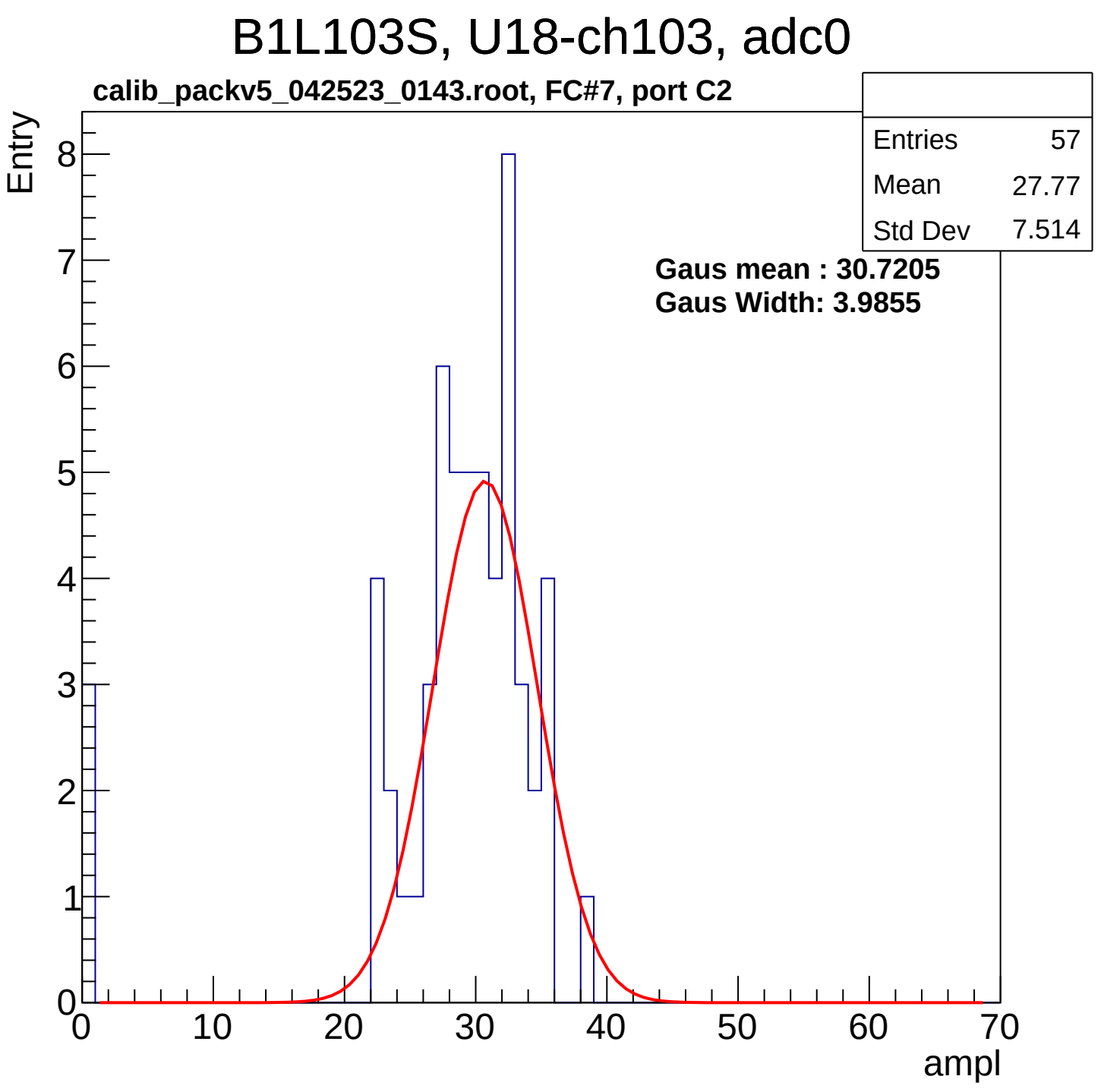
B1L103S, U18-ch103, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 27.77
Std Dev 7.514
Gaus mean : 30.7205
Gaus Width: 3.9855
Entry
ampl
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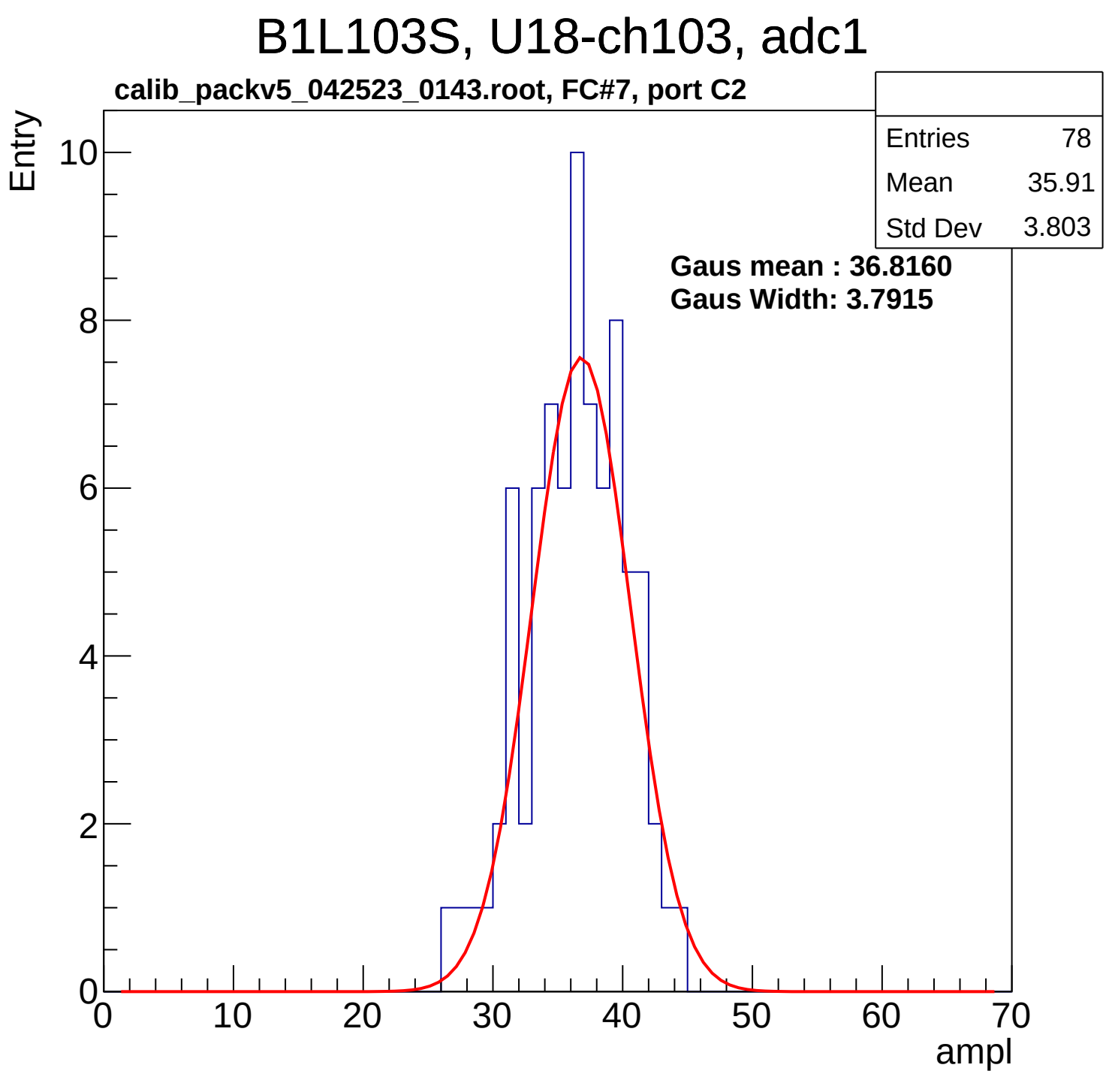
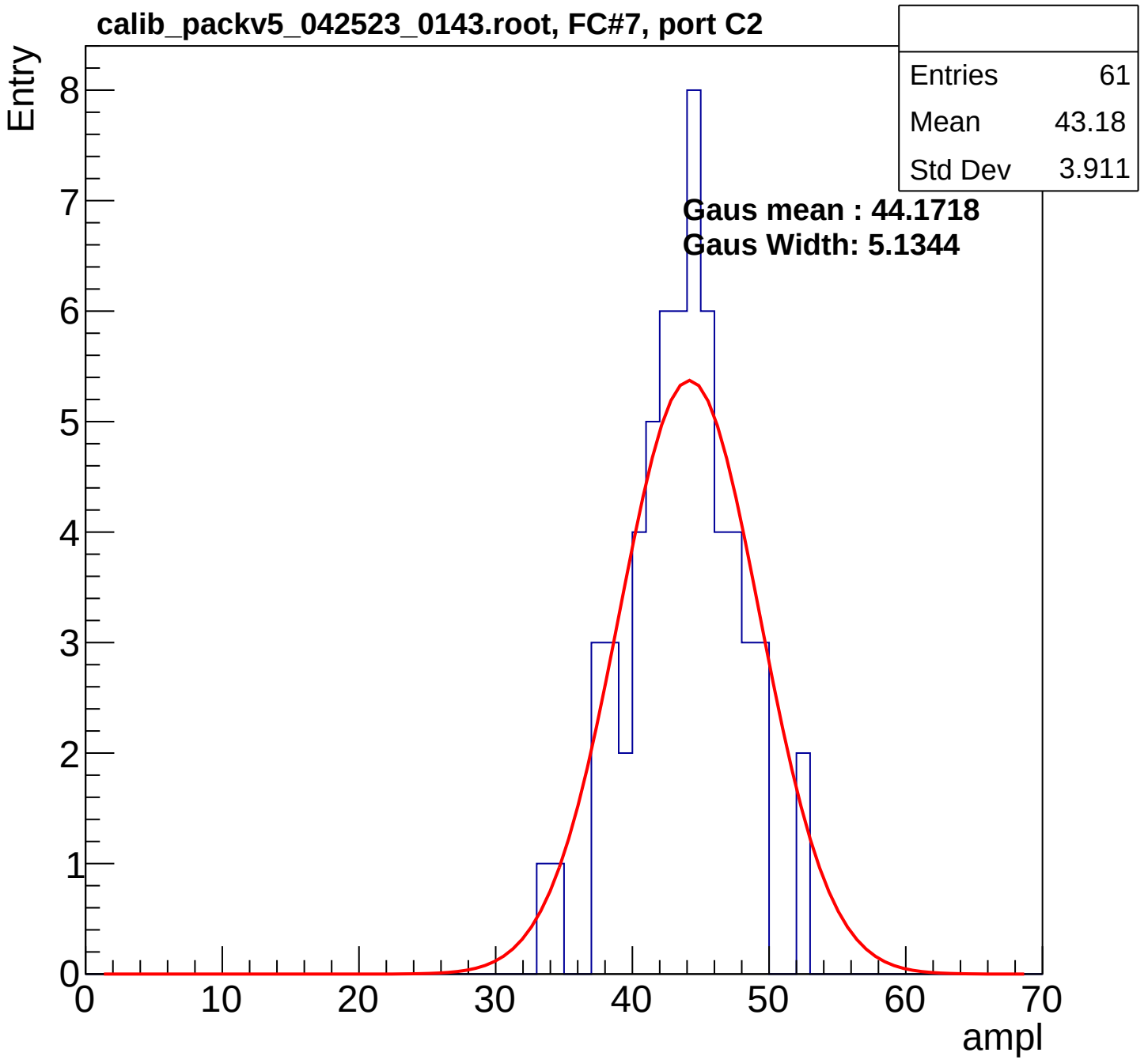
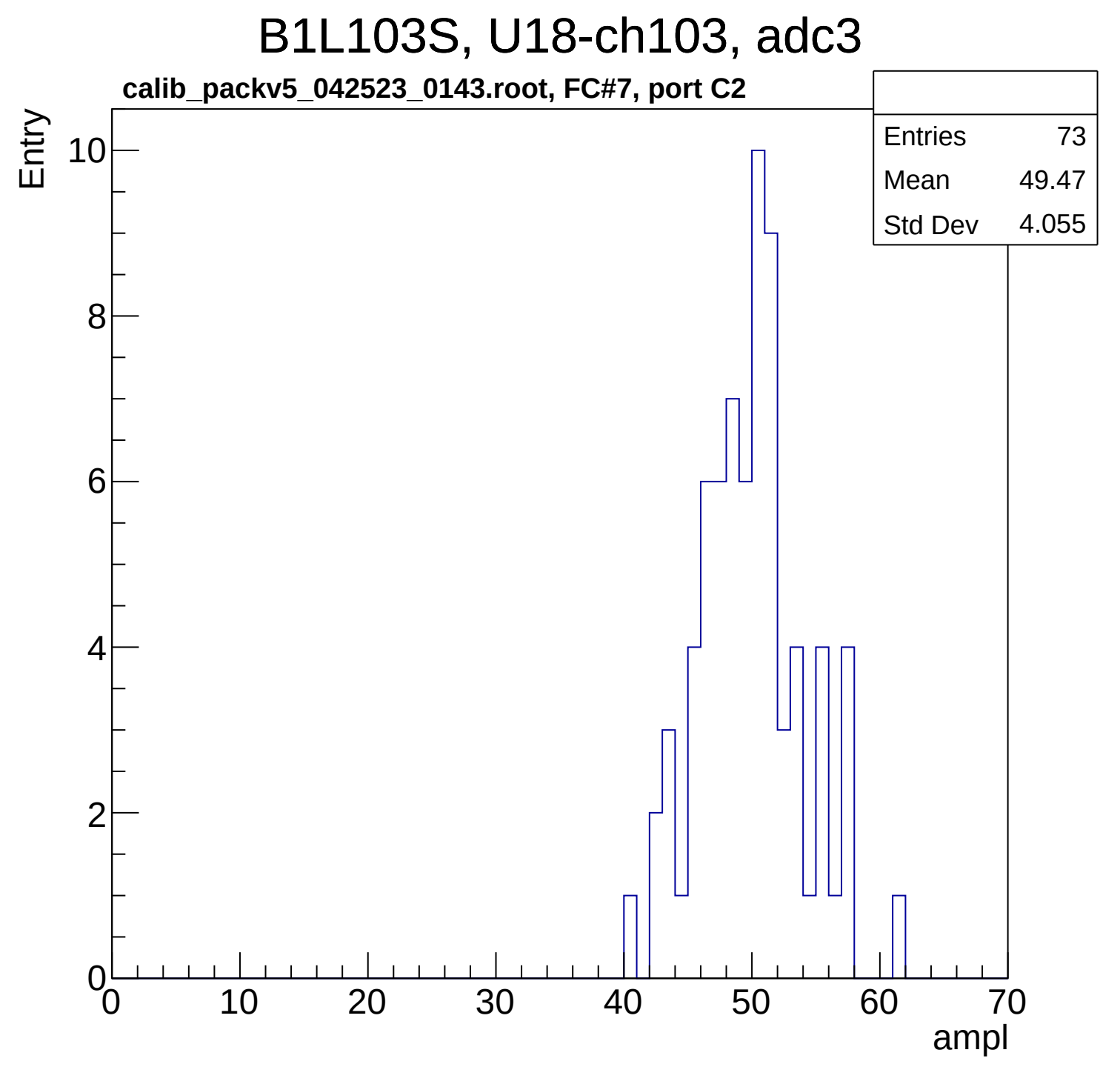
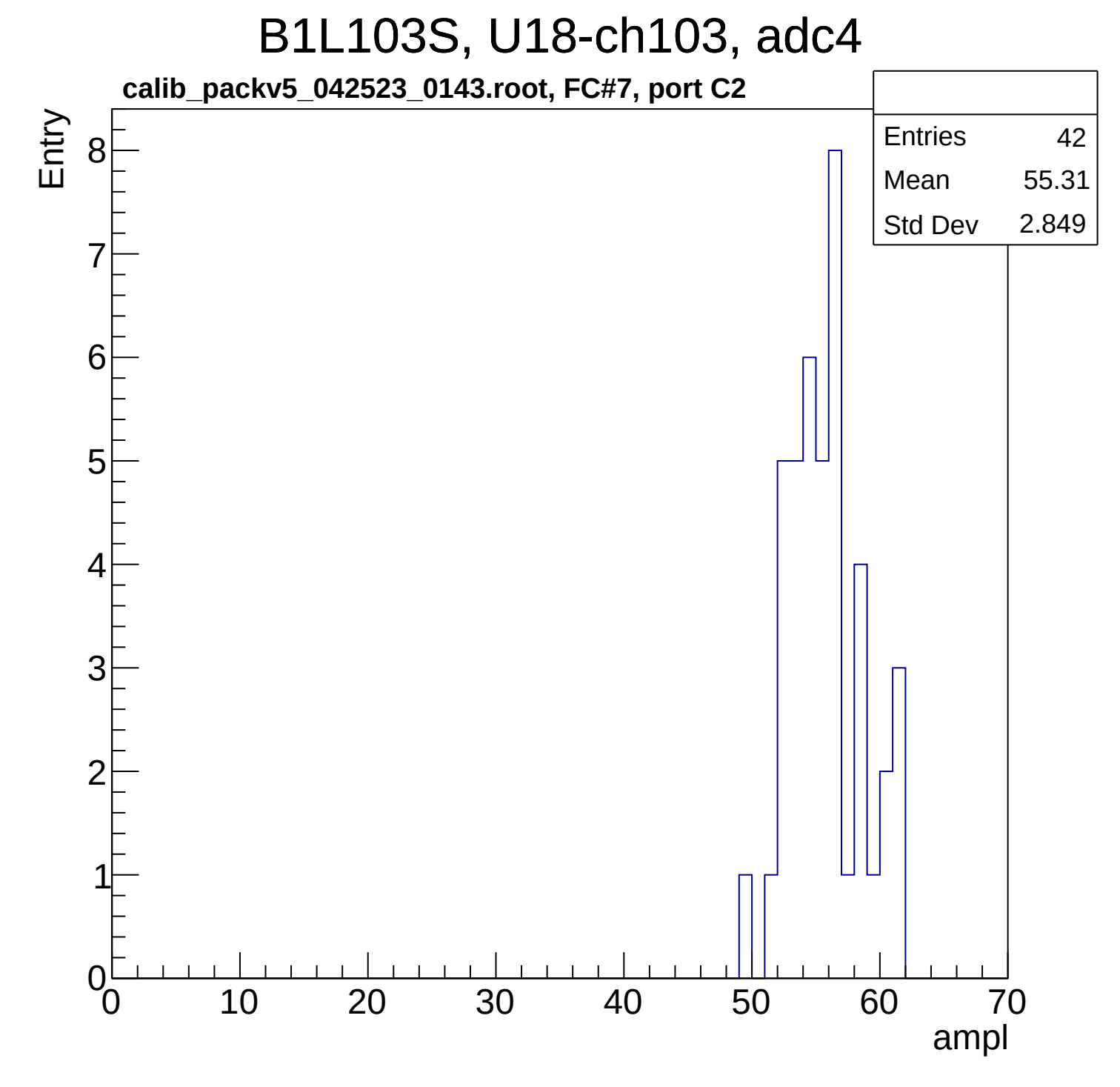
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch103, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 78
Mean 35.91
Std Dev 3.803
Gaus mean : 36.8160
Gaus Width: 3.7915
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch103, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 61
Mean 43.18
Std Dev 3.911
Gaus mean : 44.1718
Gaus Width: 5.1344
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch103, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 73
Mean 49.47
Std Dev 4.055
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch103, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 42
Mean 55.31
Std Dev 2.849
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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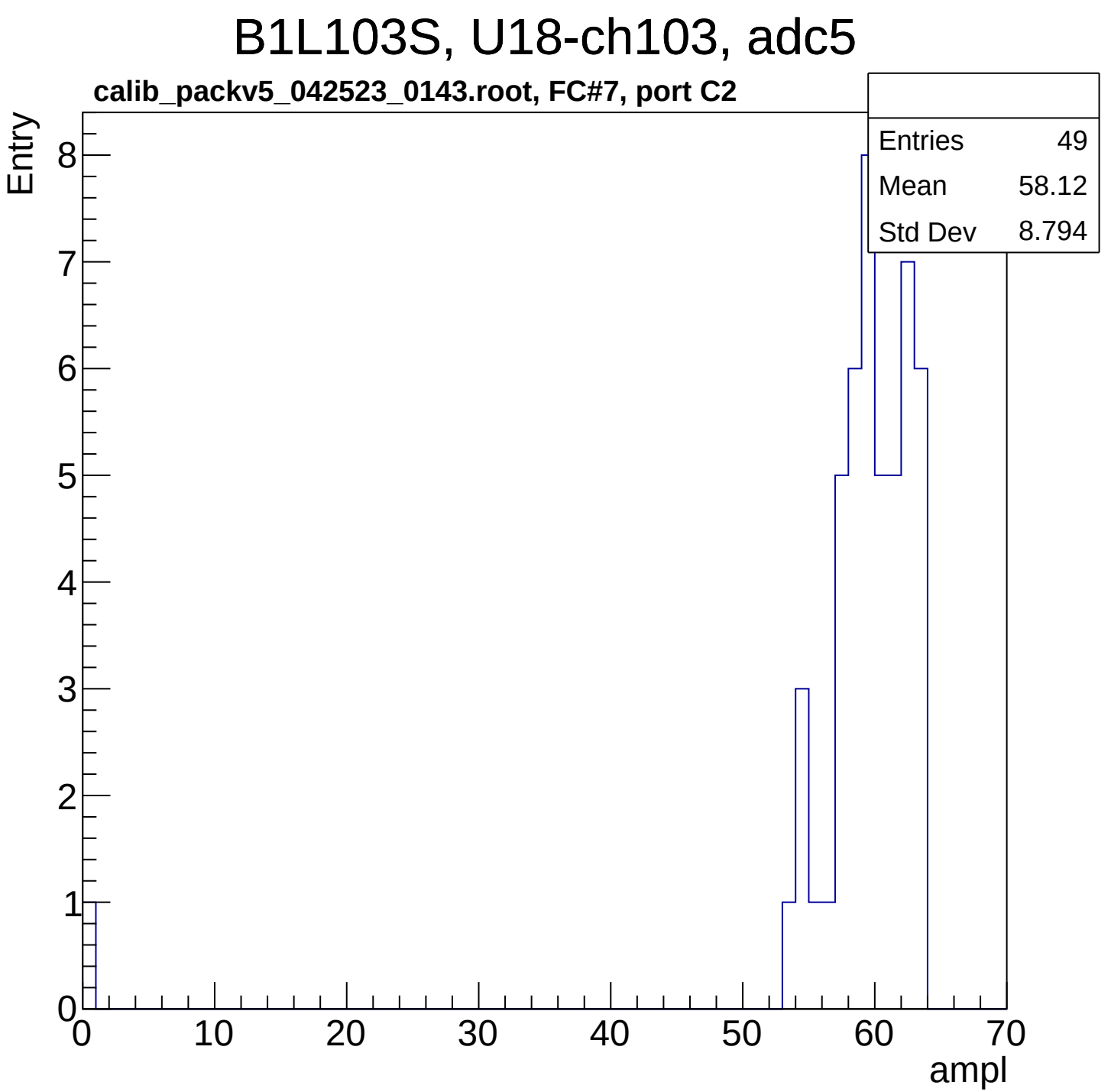
B1L103S, U18-ch103, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 49
Mean 58.12
Std Dev 8.794
Entry
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8
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10
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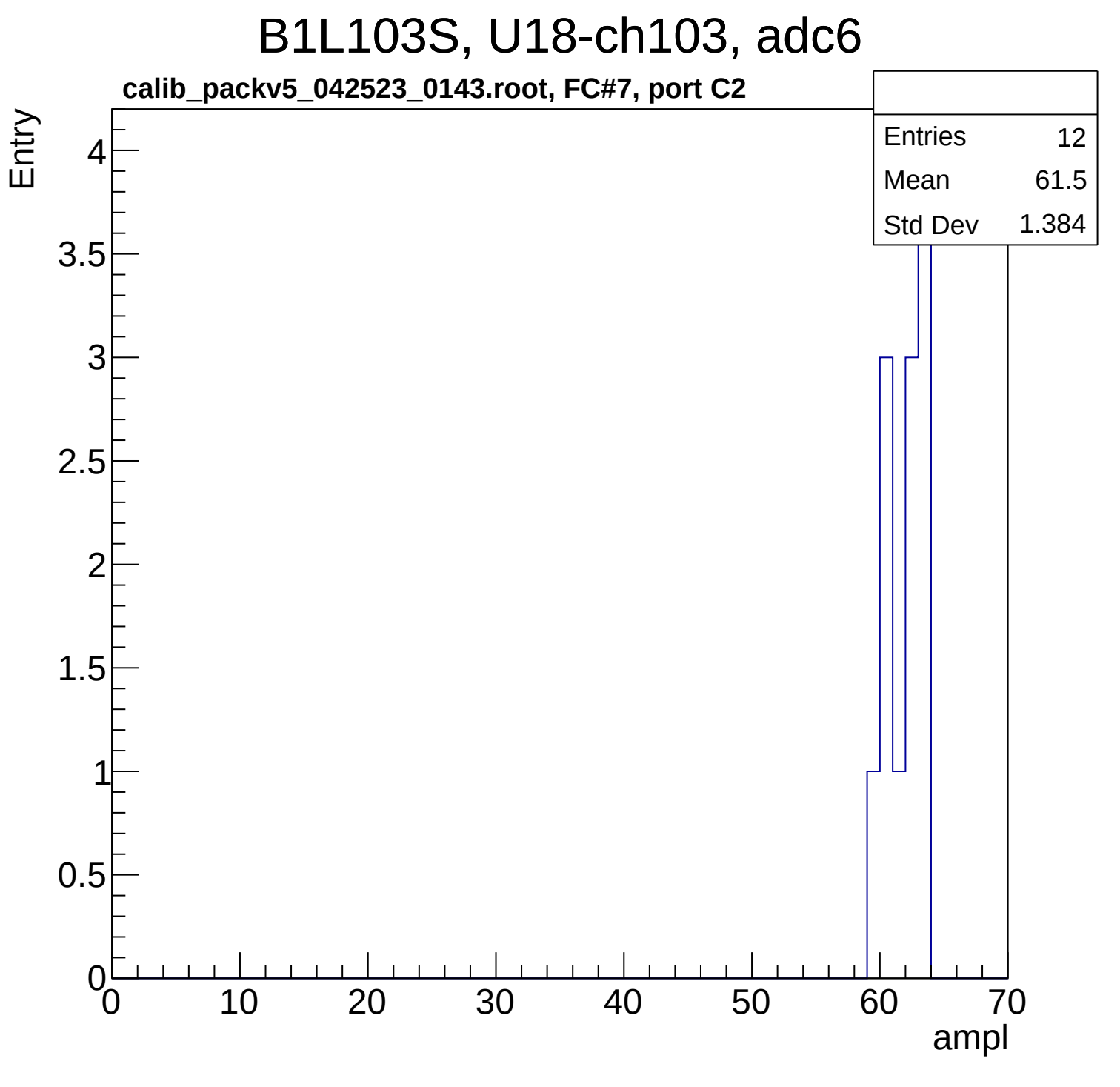
60
70
ampl


B1L103S, U18-ch103, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 12
Mean 61.5
Std Dev 1.384
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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40
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60
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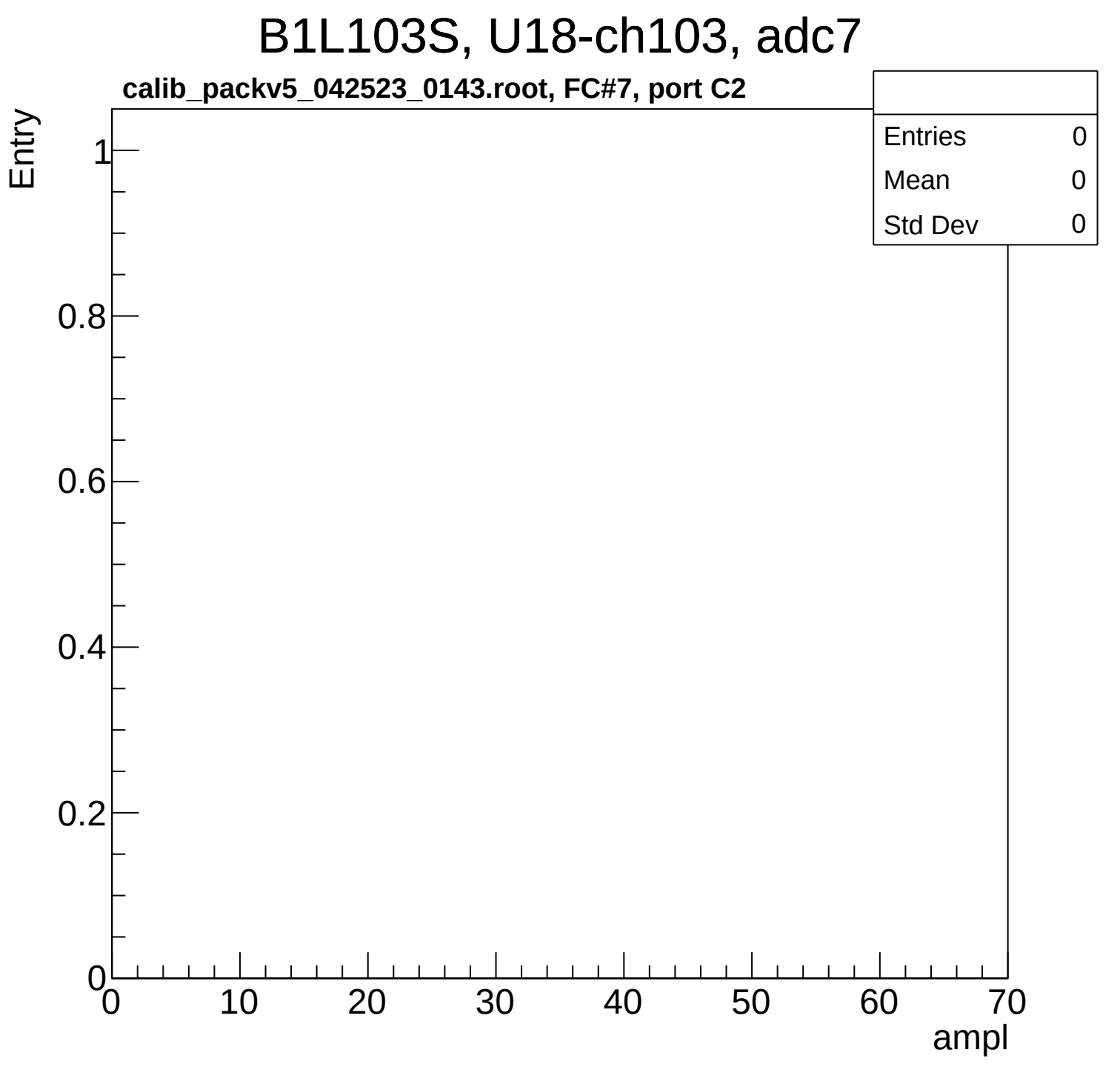
B1L103S, U18-ch103, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
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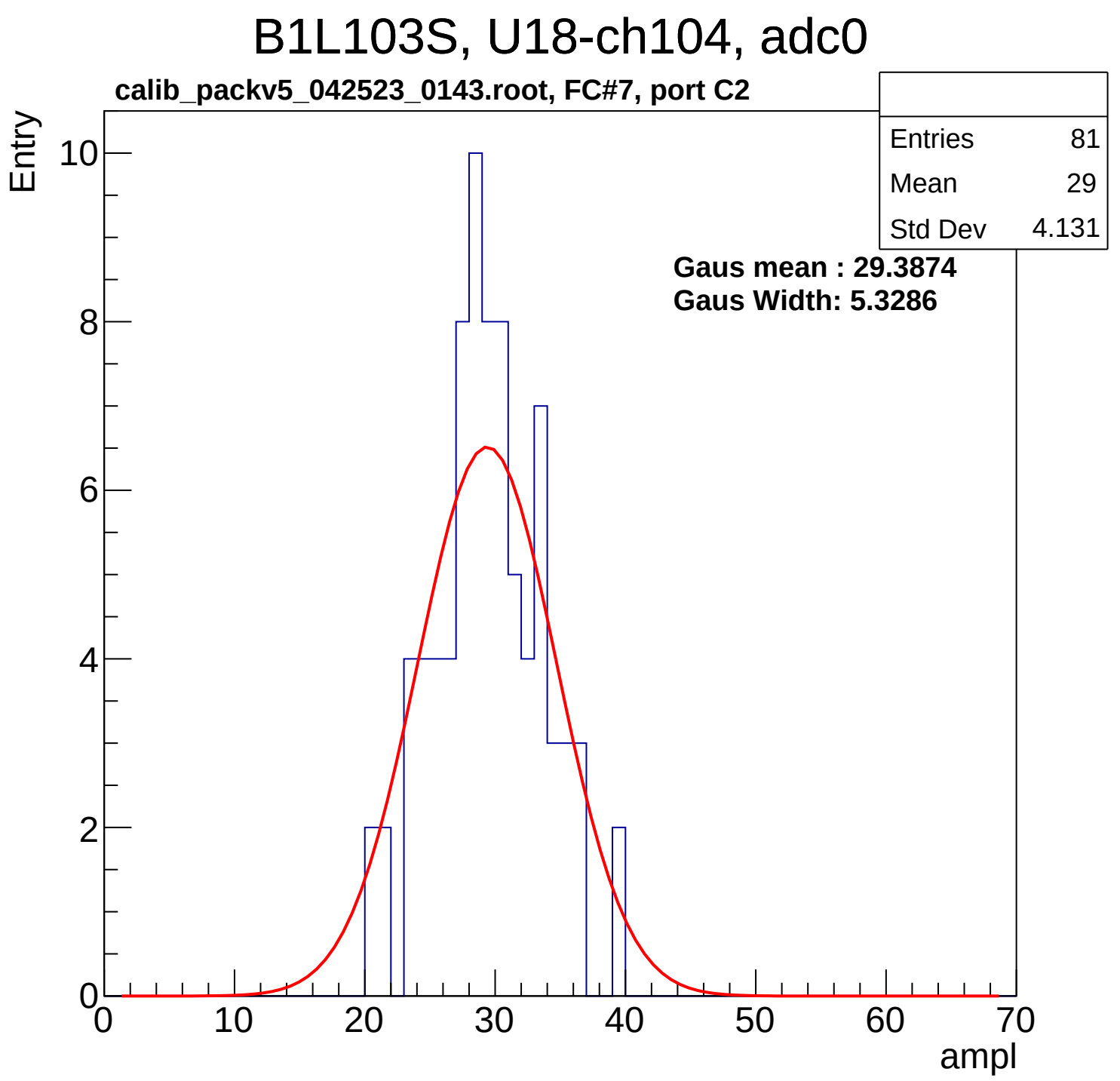
30
40
50
60
70
ampl


B1L103S, U18-ch104, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 81
Mean 29
Std Dev 4.131
Gaus mean : 29.3874
Gaus Width: 5.3286
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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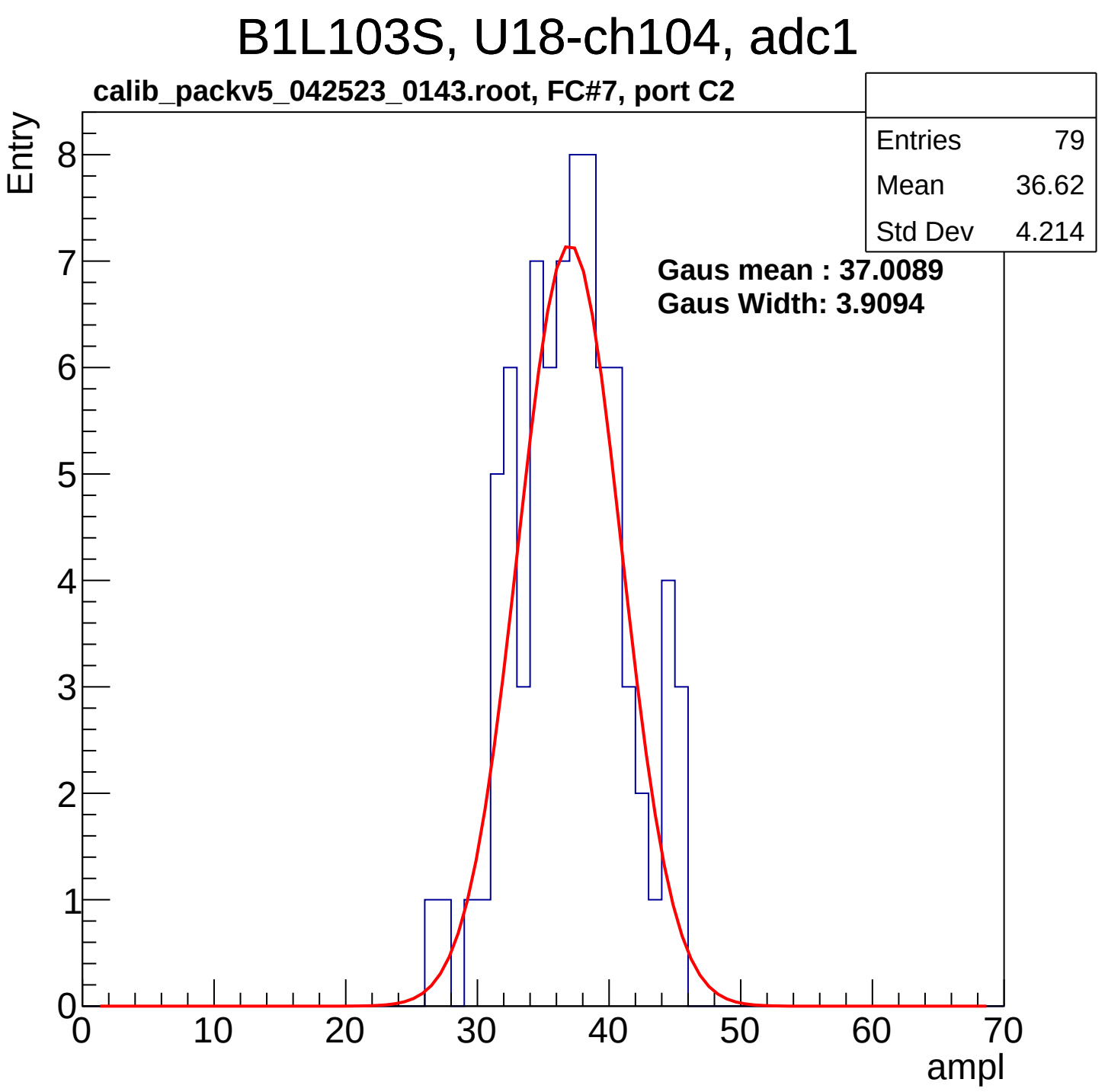
B1L103S, U18-ch104, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 79
Mean 36.62
Std Dev 4.214
Gaus mean : 37.0089
Gaus Width: 3.9094
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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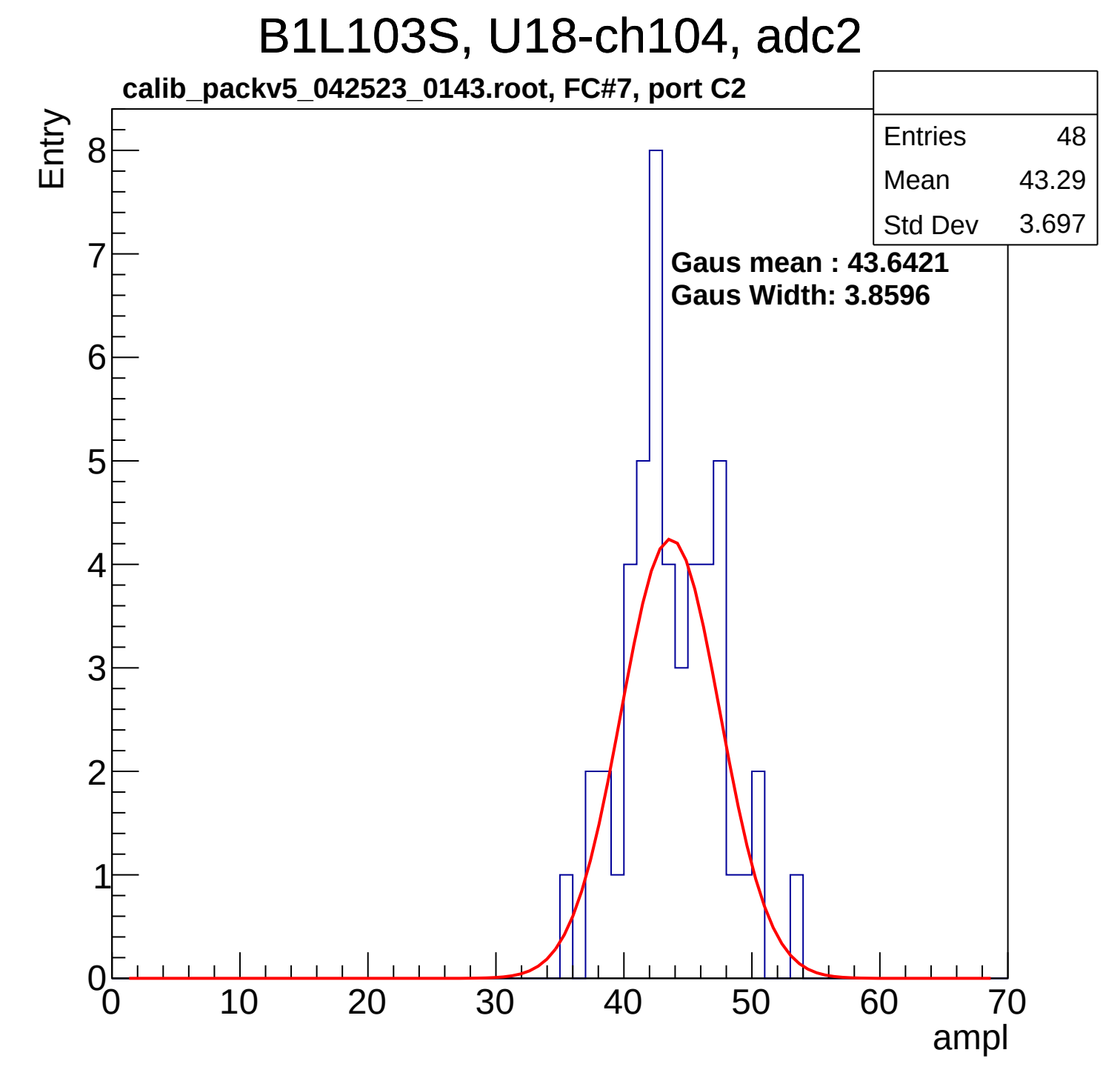
B1L103S, U18-ch104, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 48
Mean 43.29
Std Dev 3.697
Gaus mean : 43.6421
Gaus Width: 3.8596
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
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60
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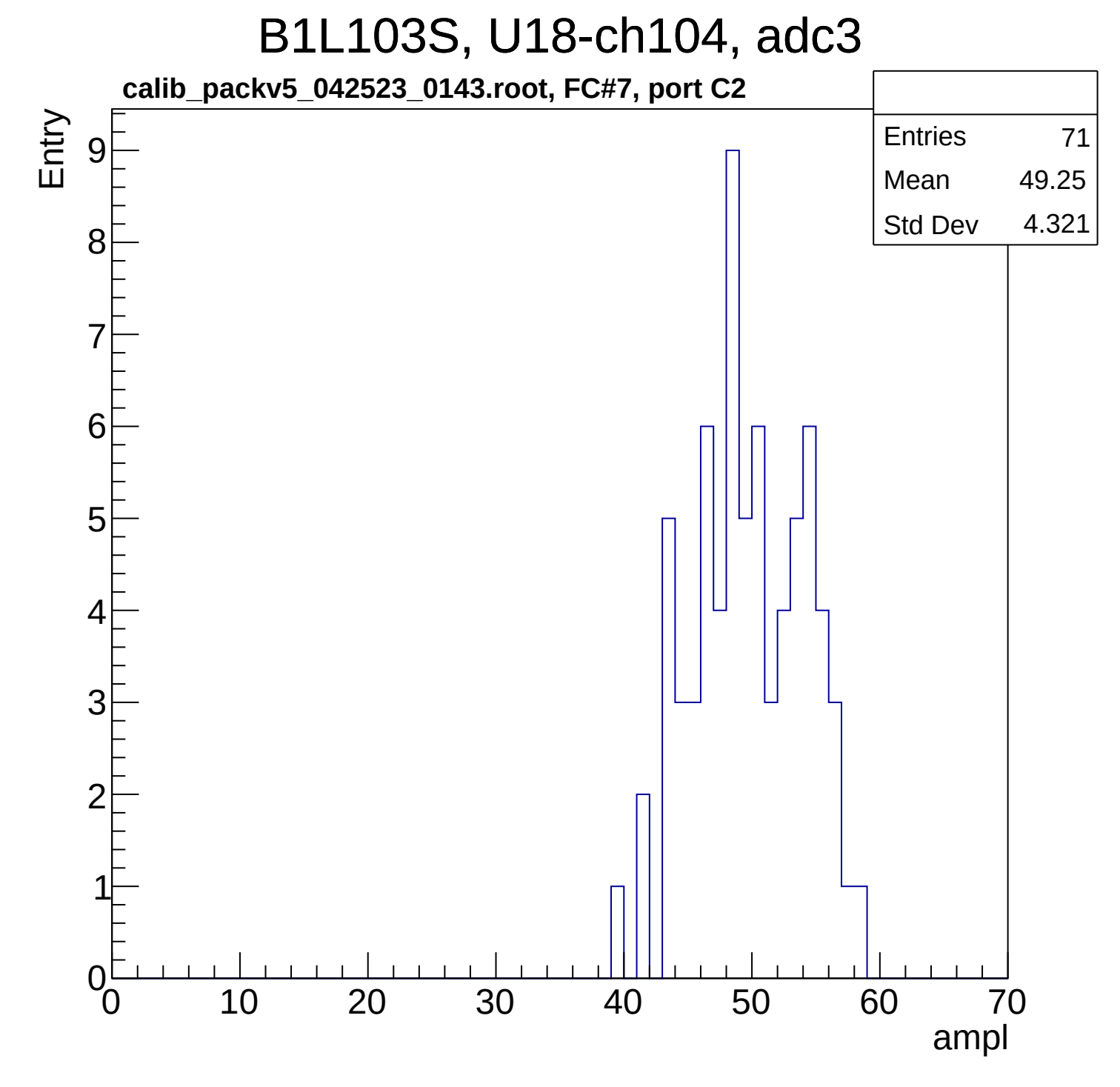
B1L103S, U18-ch104, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 71
Mean 49.25
Std Dev 4.321
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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20
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40
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60
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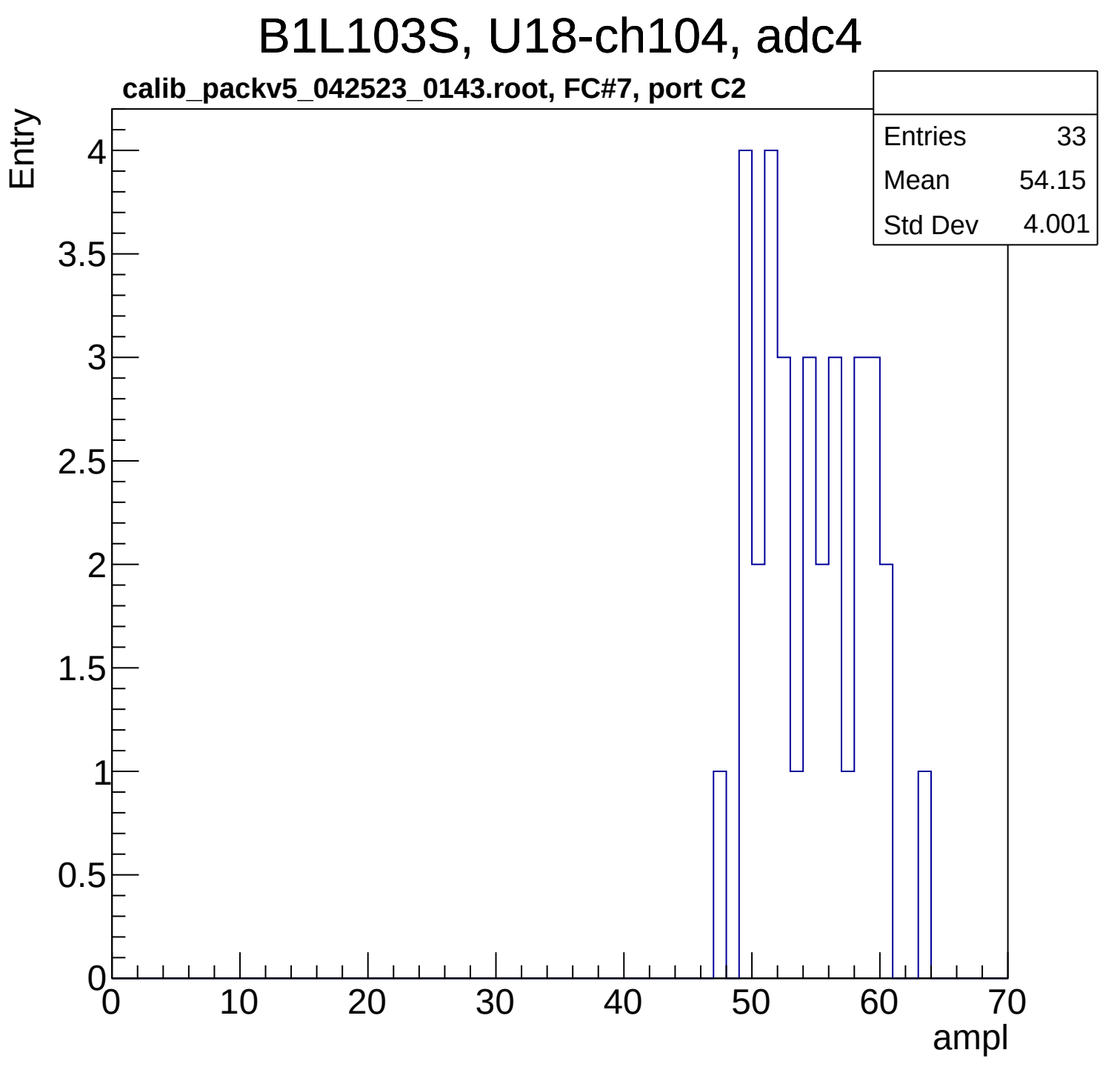
B1L103S, U18-ch104, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 33
Mean 54.15
Std Dev 4.001
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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40
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60
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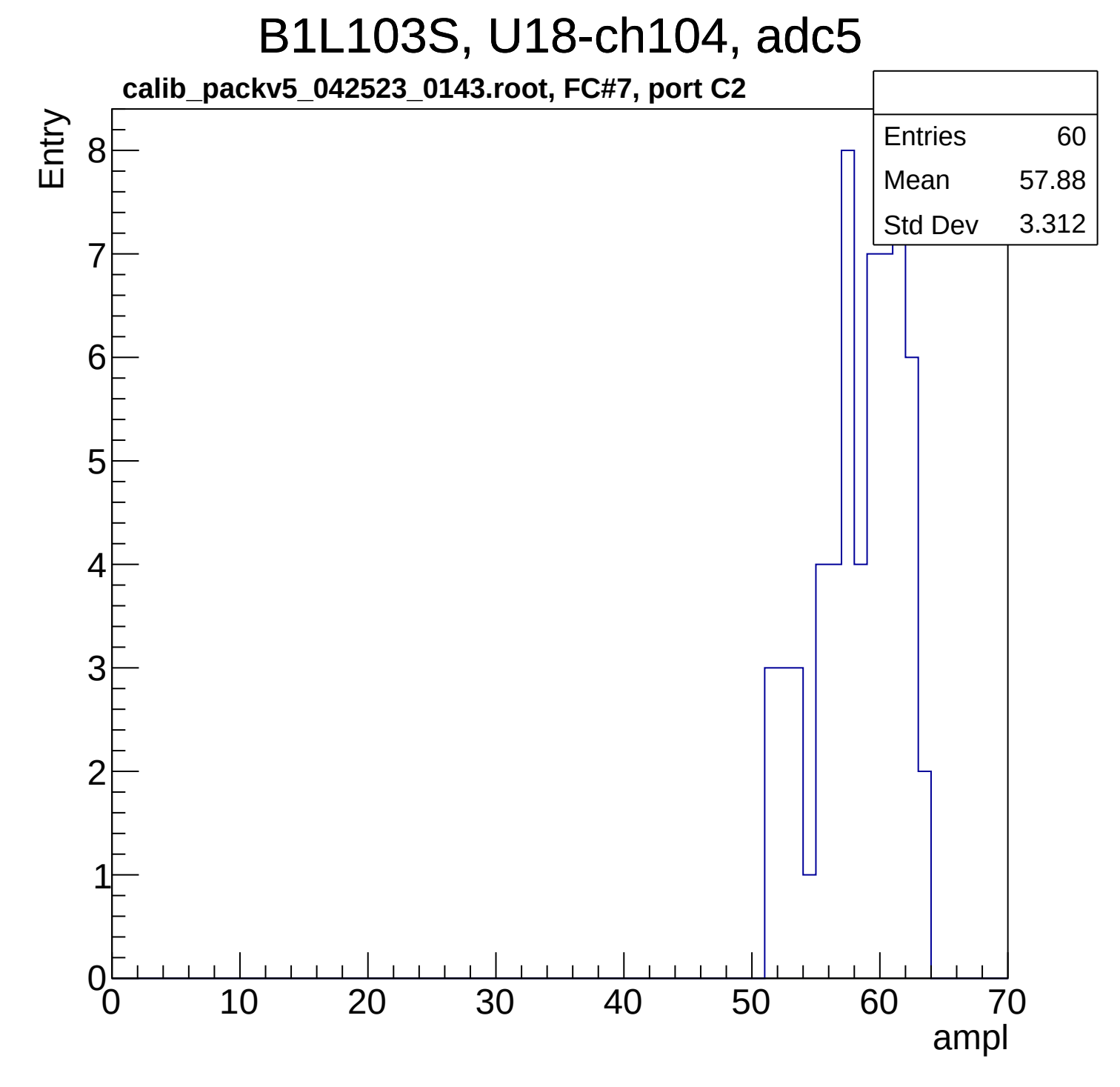
B1L103S, U18-ch104, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 60
Mean 57.88
Std Dev 3.312
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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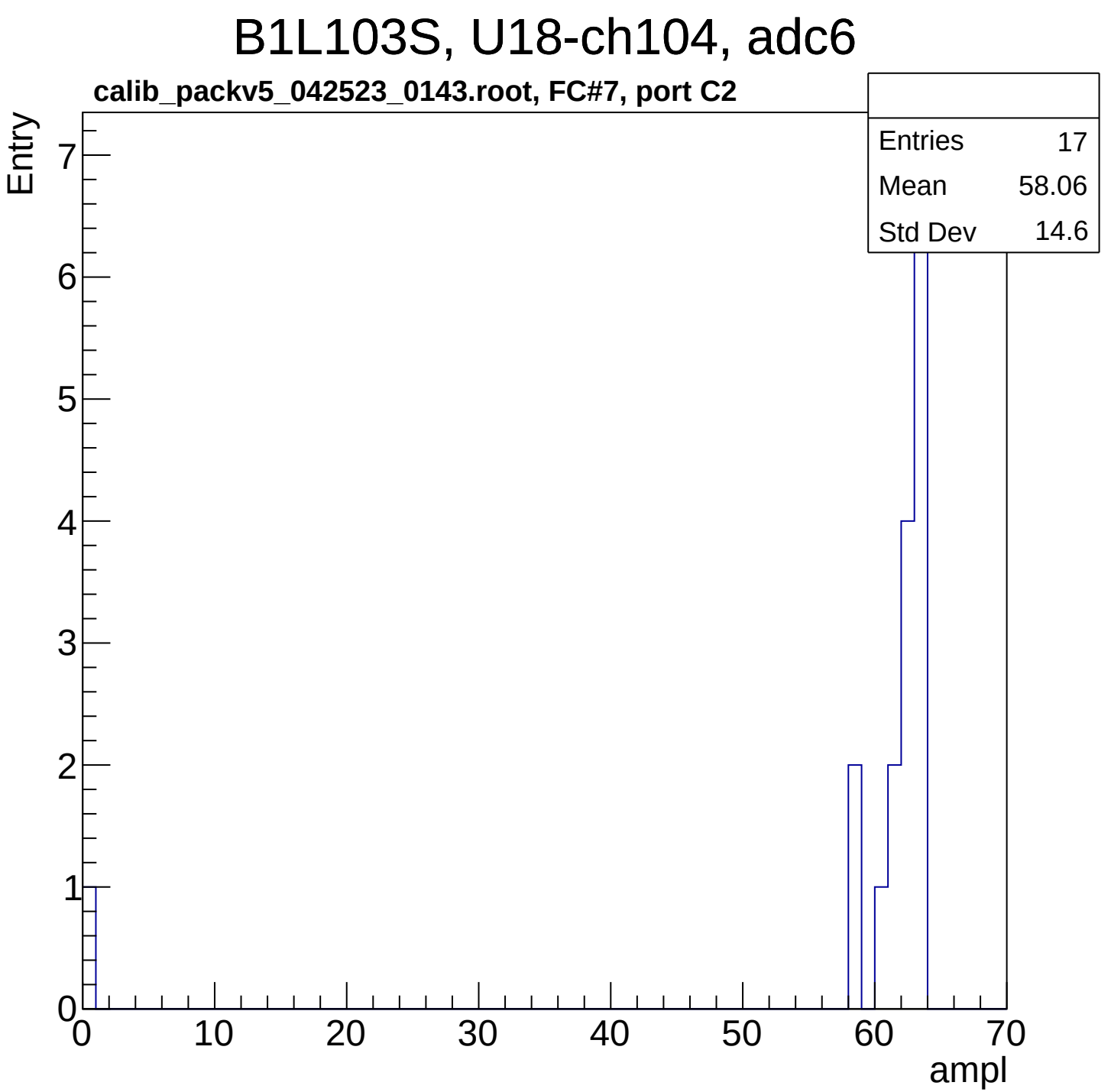
B1L103S, U18-ch104, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 17
Mean 58.06
Std Dev 14.6
Entry
ampl
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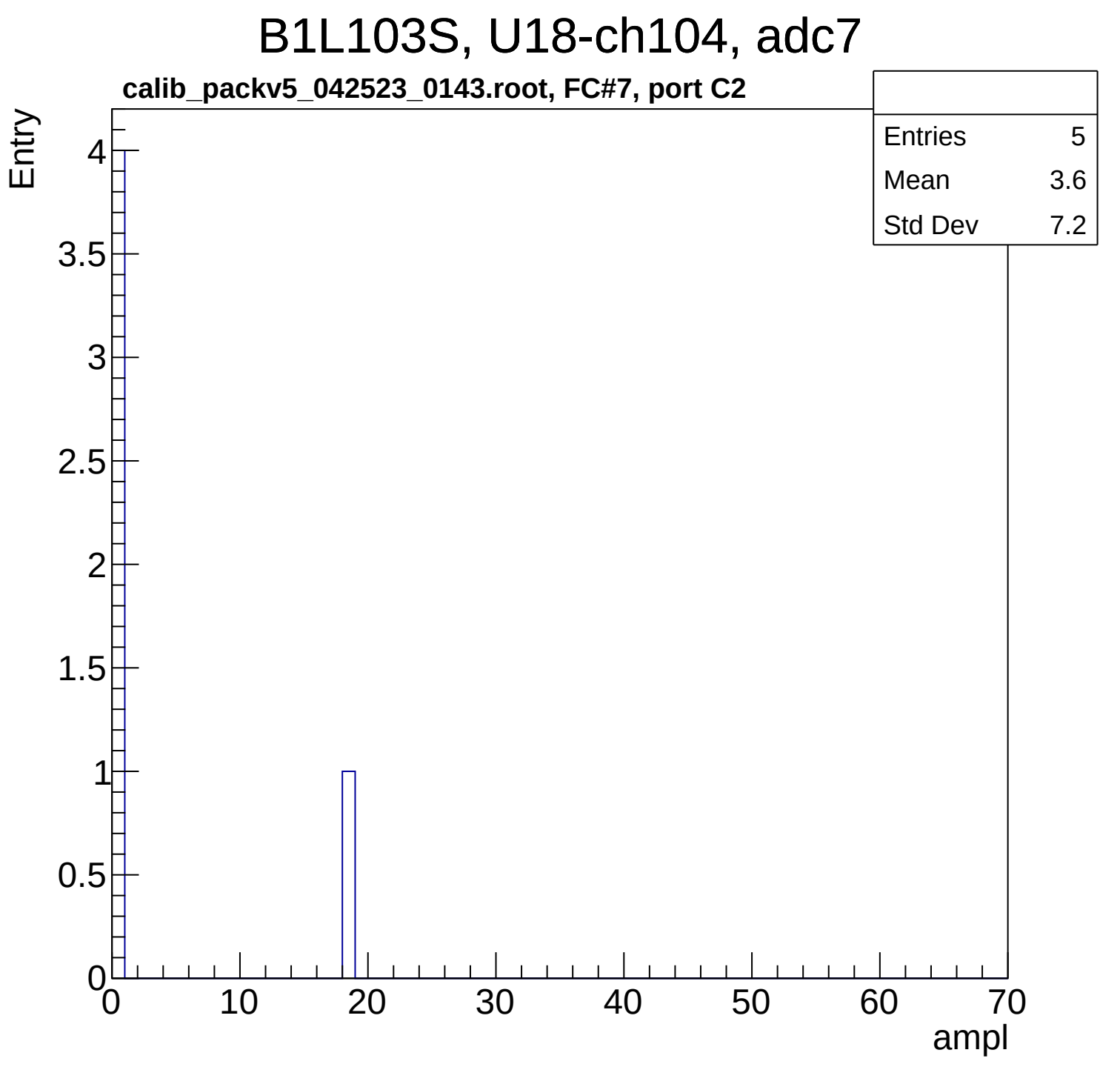
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch104, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 5
Mean 3.6
Std Dev 7.2
Entry
ampl
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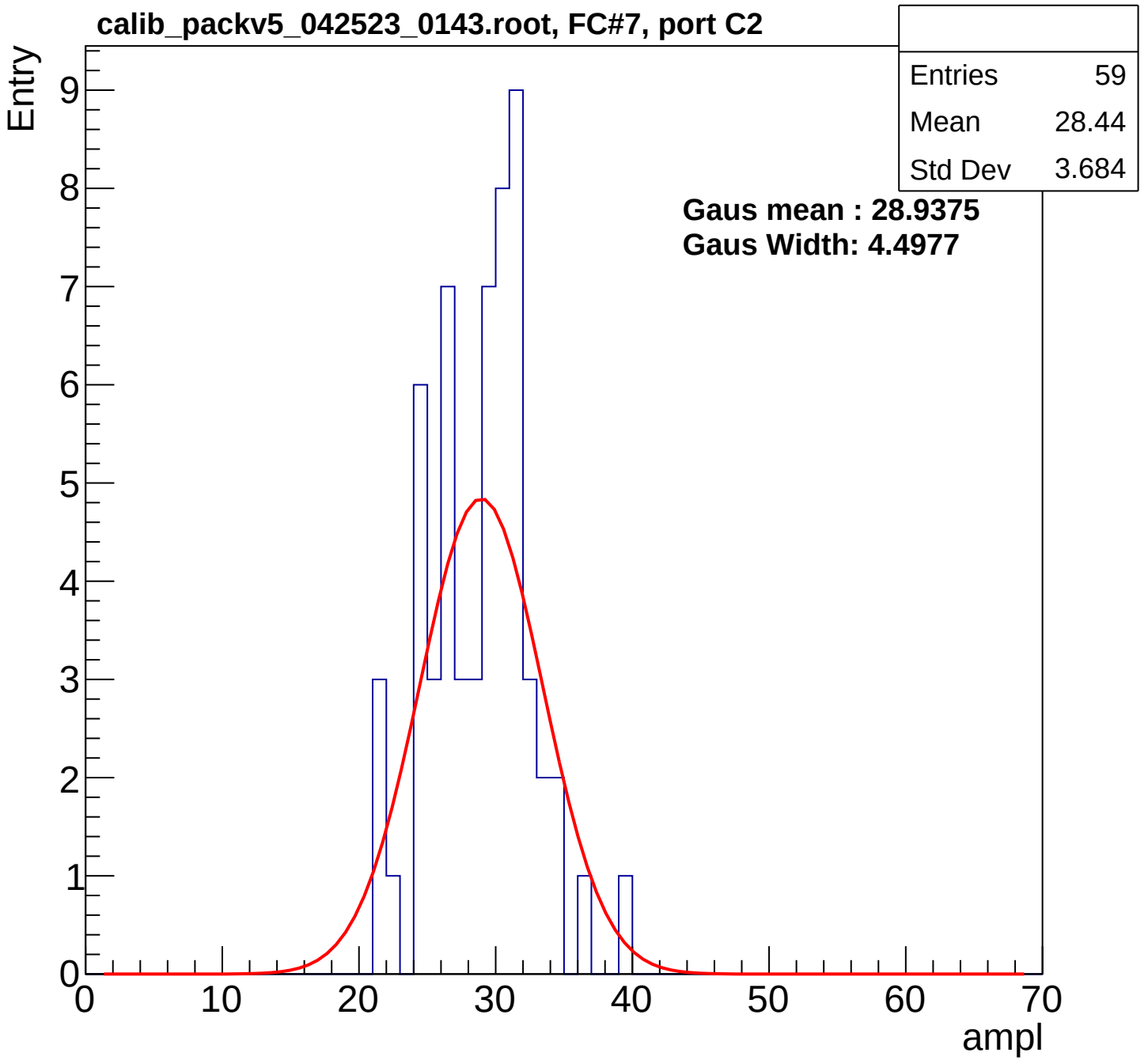
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U18-ch105, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 28.44
Std Dev 3.684
Gaus mean : 28.9375
Gaus Width: 4.4977
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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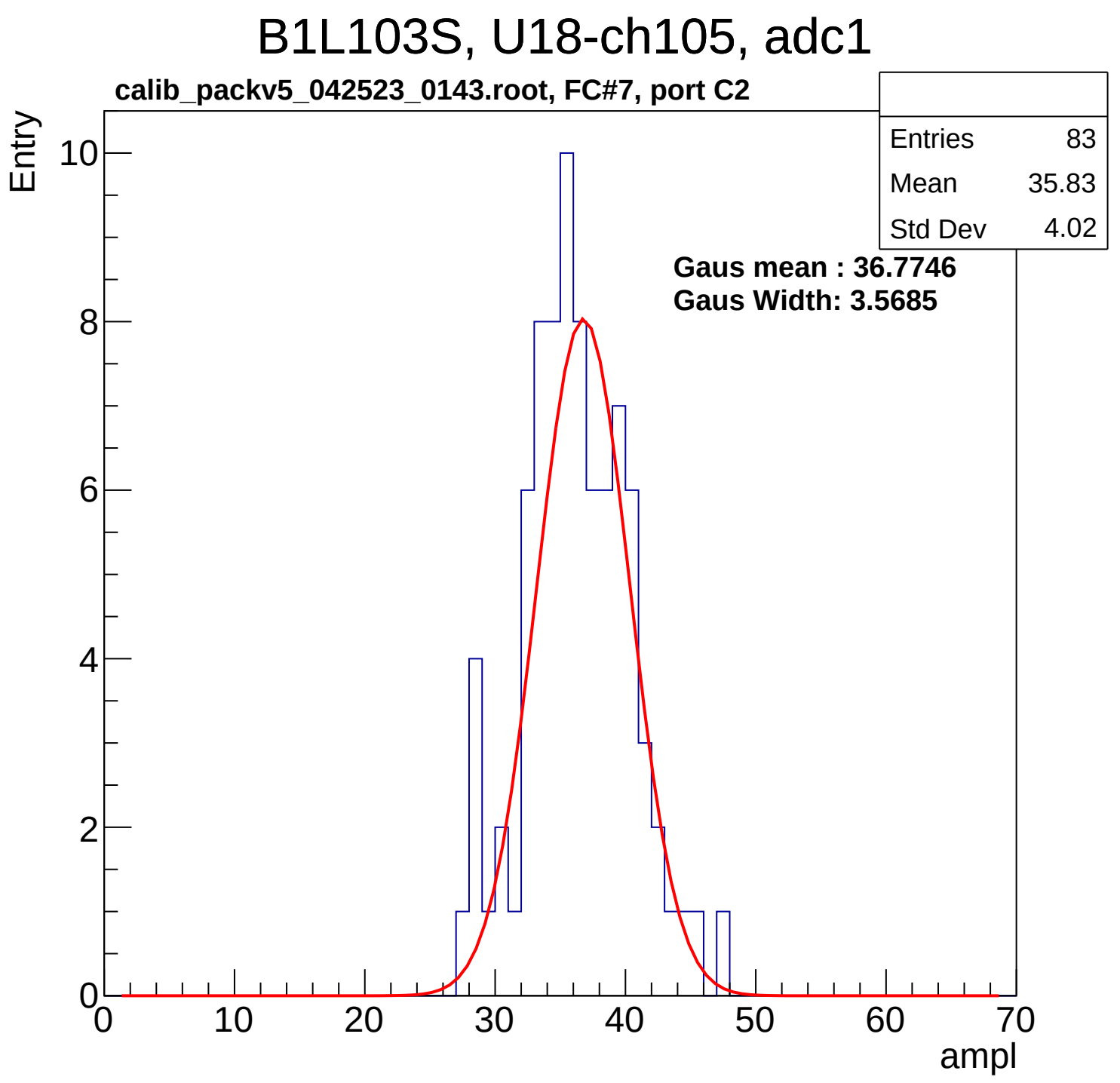
B1L103S, U18-ch105, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 83
Mean 35.83
Std Dev 4.02
Gaus mean : 36.7746
Gaus Width: 3.5685
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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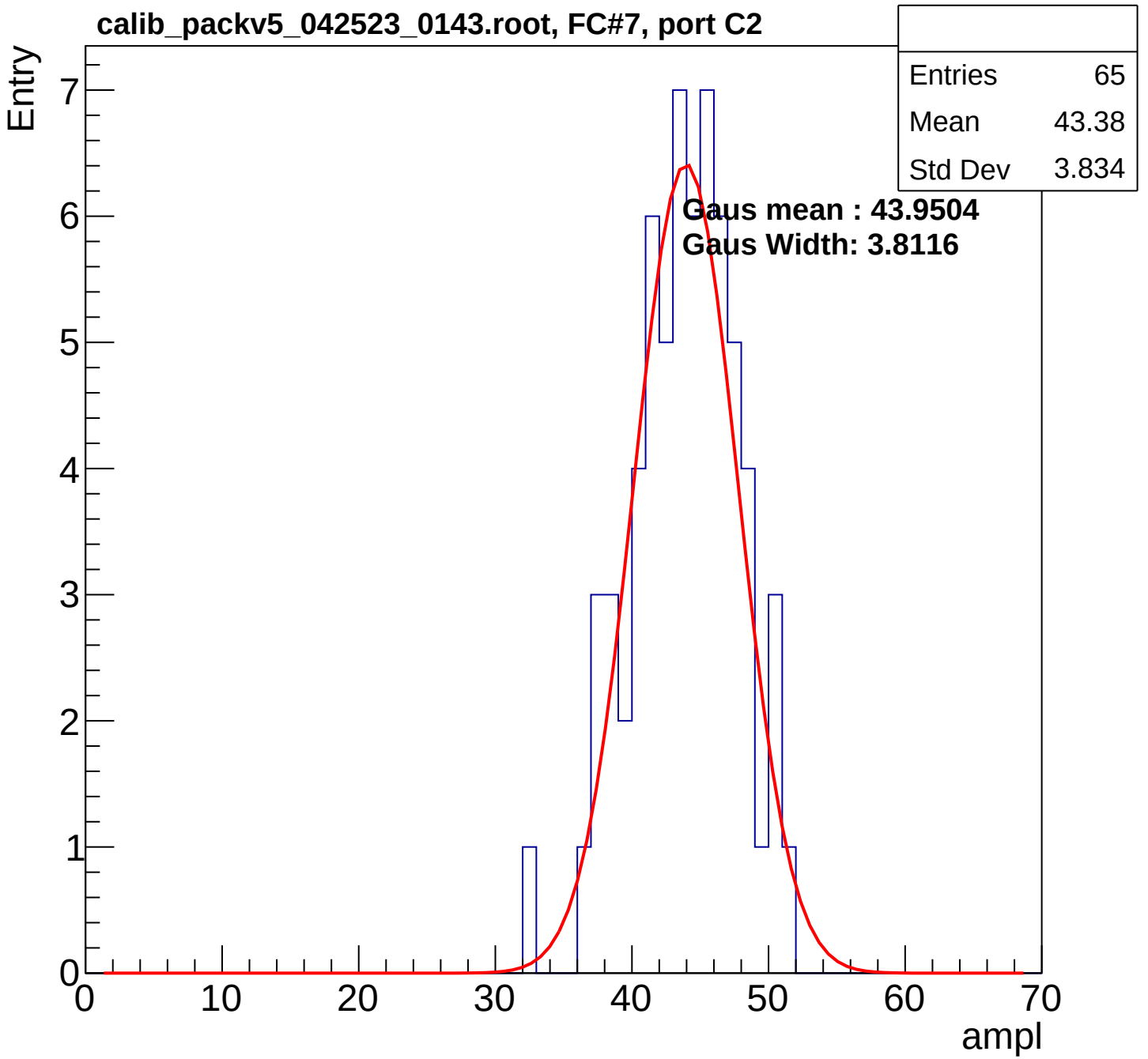
B1L103S, U18-ch105, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 43.38
Std Dev 3.834
Gaus mean : 43.9504
Gaus Width: 3.8116
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
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60
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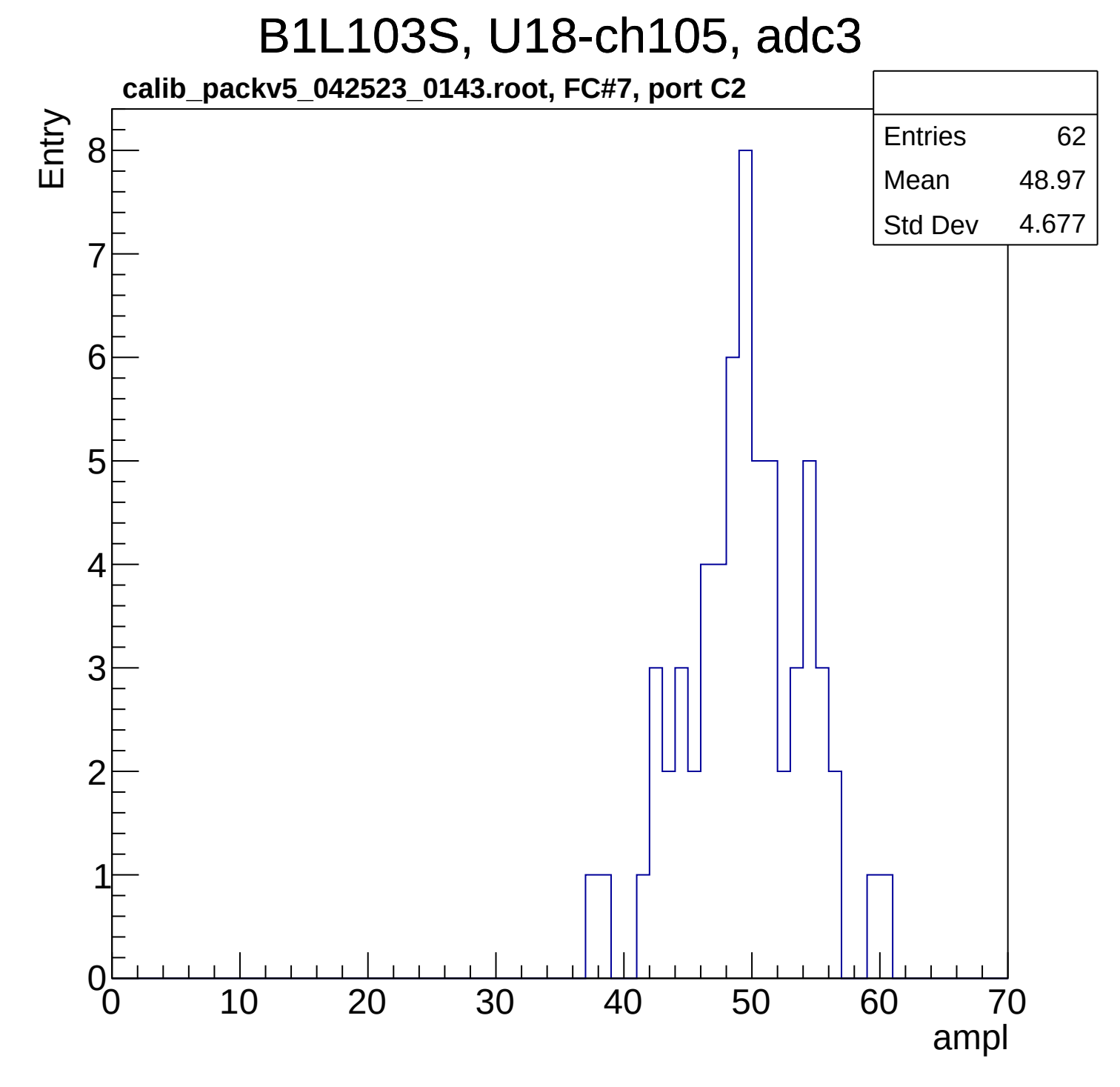
B1L103S, U18-ch105, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 62
Mean 48.97
Std Dev 4.677
Entry
ampl
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1
2
3
4
5
6
7
8
0
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60
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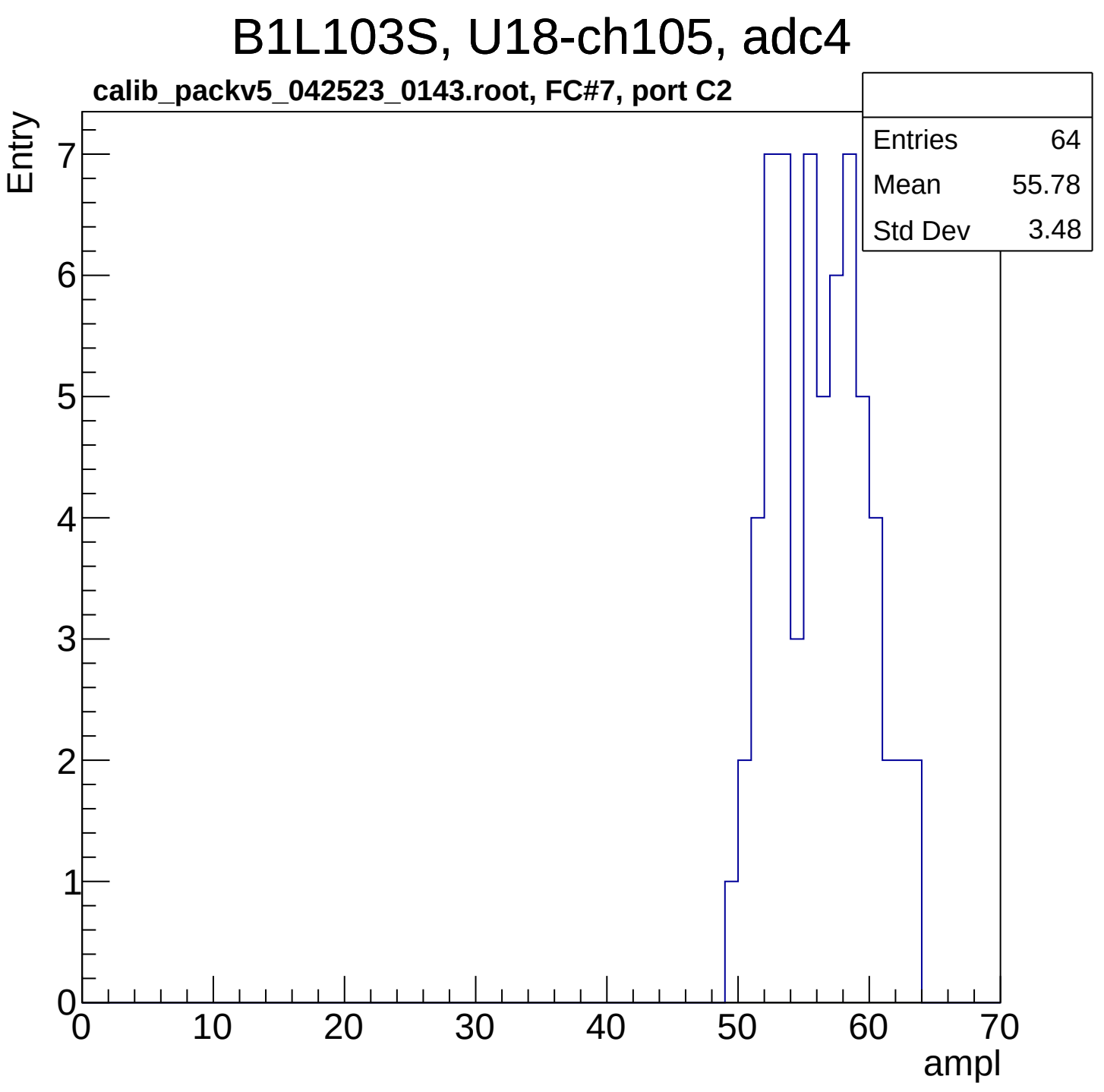
B1L103S, U18-ch105, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 55.78
Std Dev 3.48
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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40
50
60
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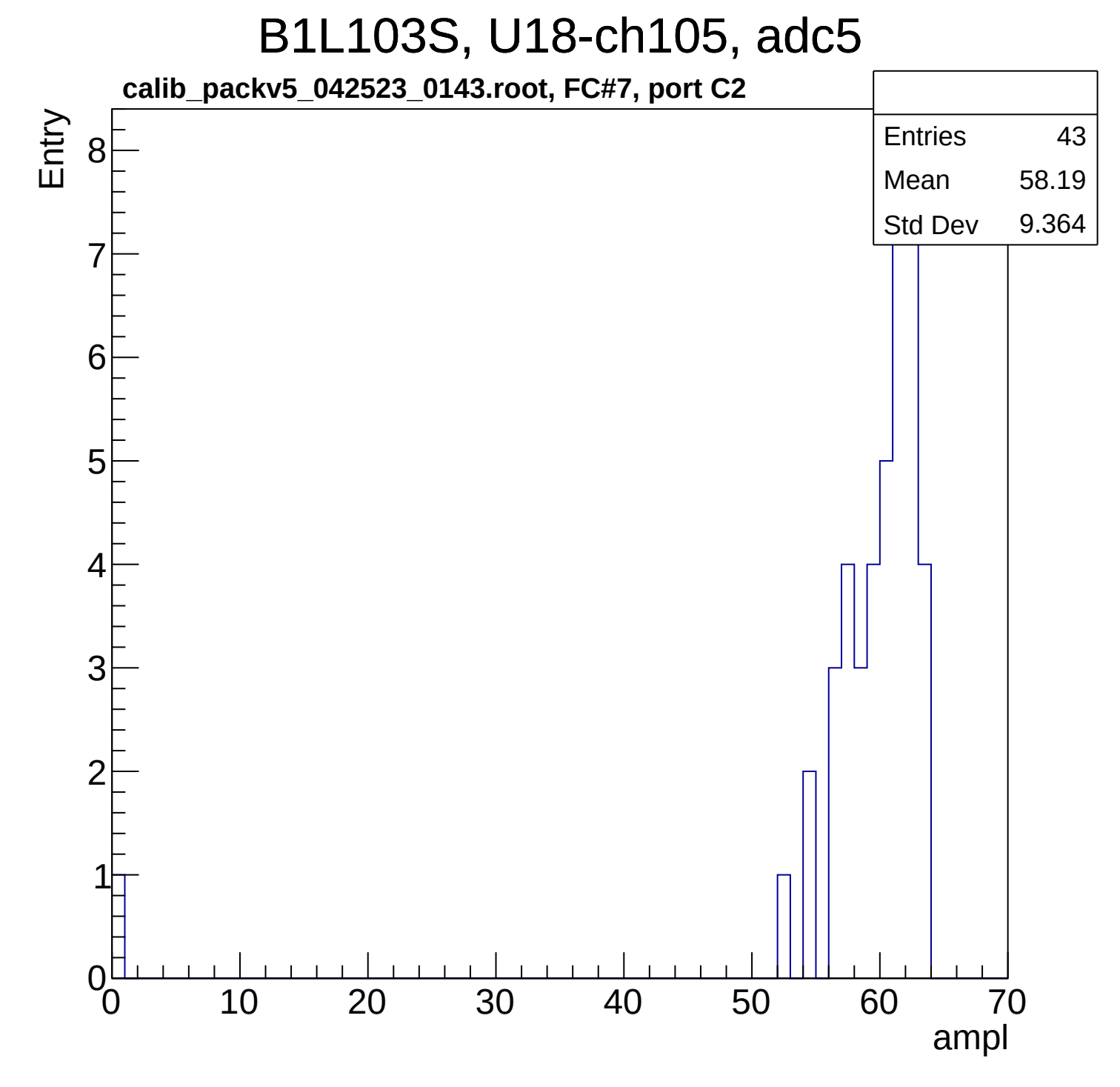
B1L103S, U18-ch105, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 43
Mean 58.19
Std Dev 9.364
Entry
ampl
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1
2
3
4
5
6
7
8
0
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60
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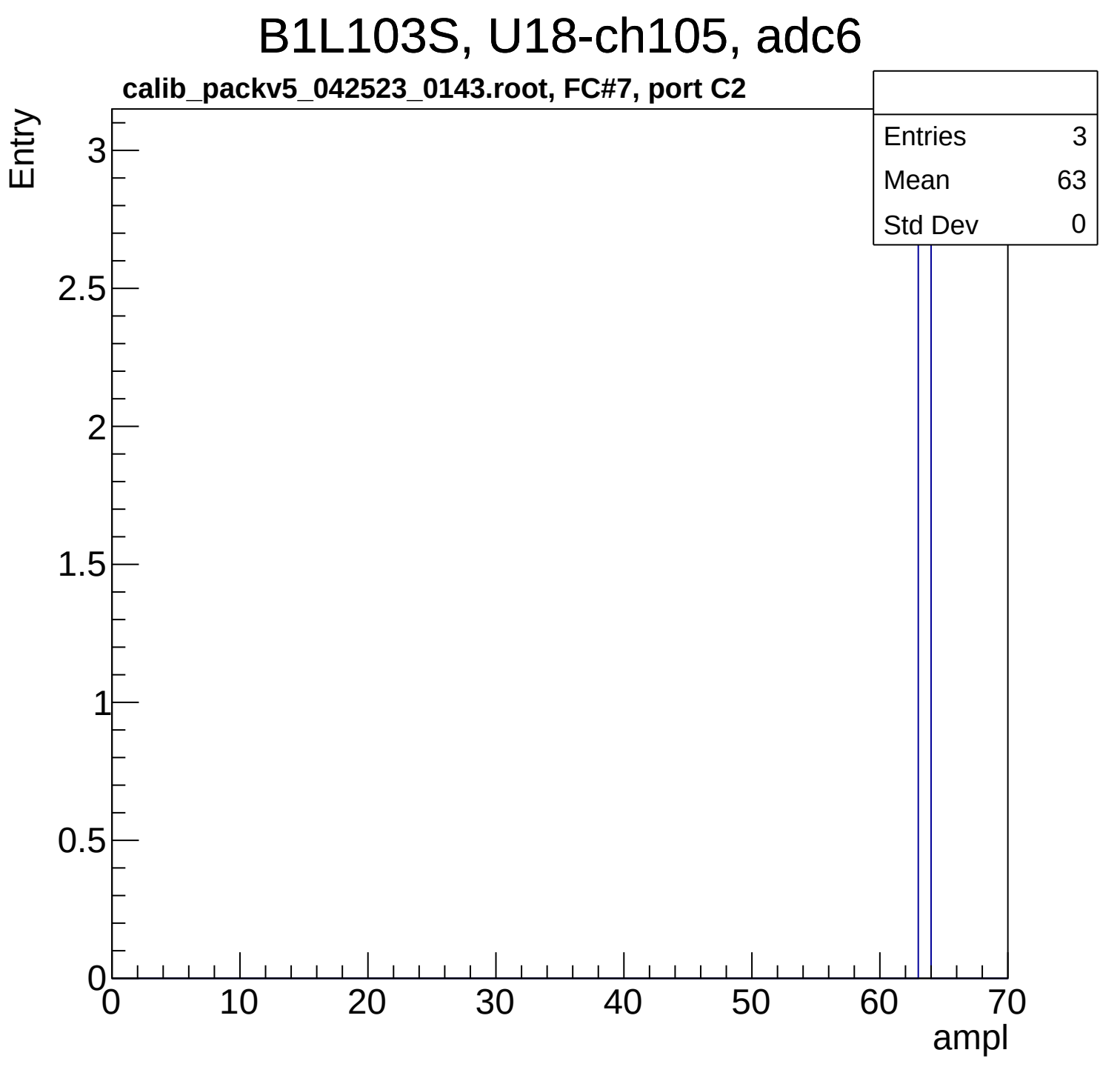
B1L103S, U18-ch105, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 63
Std Dev 0
Entry
ampl
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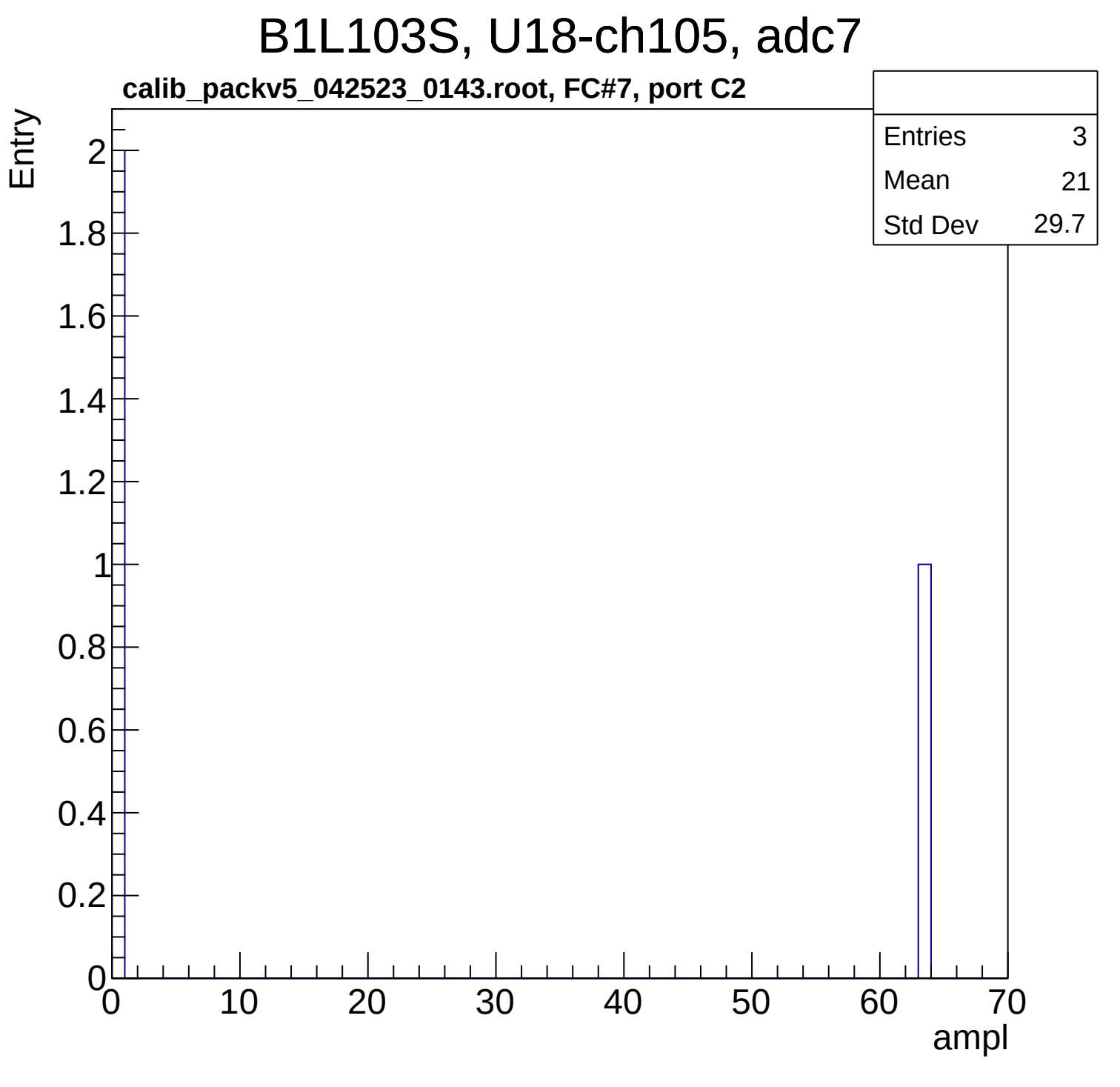
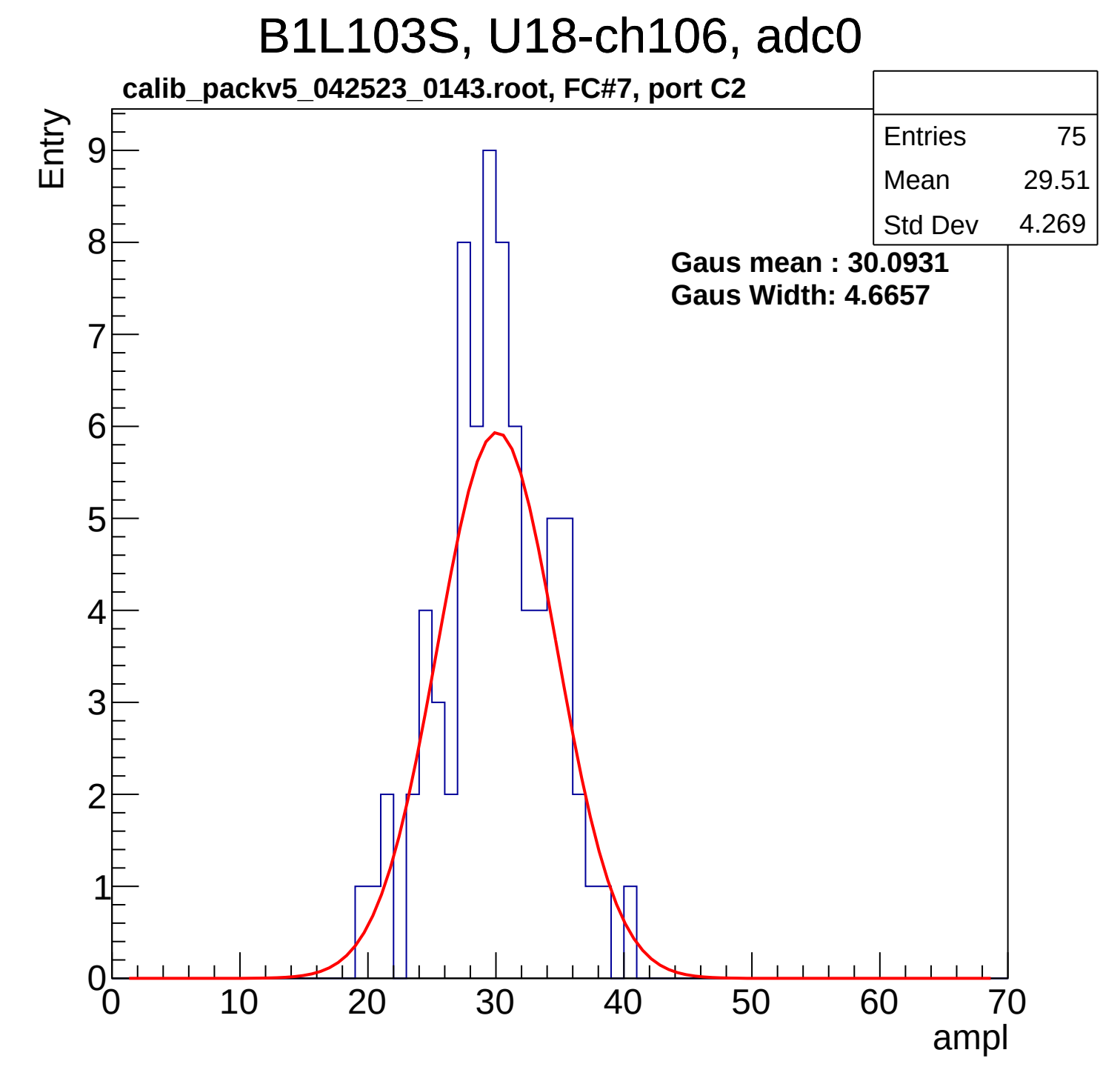
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U18-ch105, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 21
Std Dev 29.7
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U18-ch106, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 75
Mean 29.51
Std Dev 4.269
Gaus mean : 30.0931
Gaus Width: 4.6657
Entry
ampl
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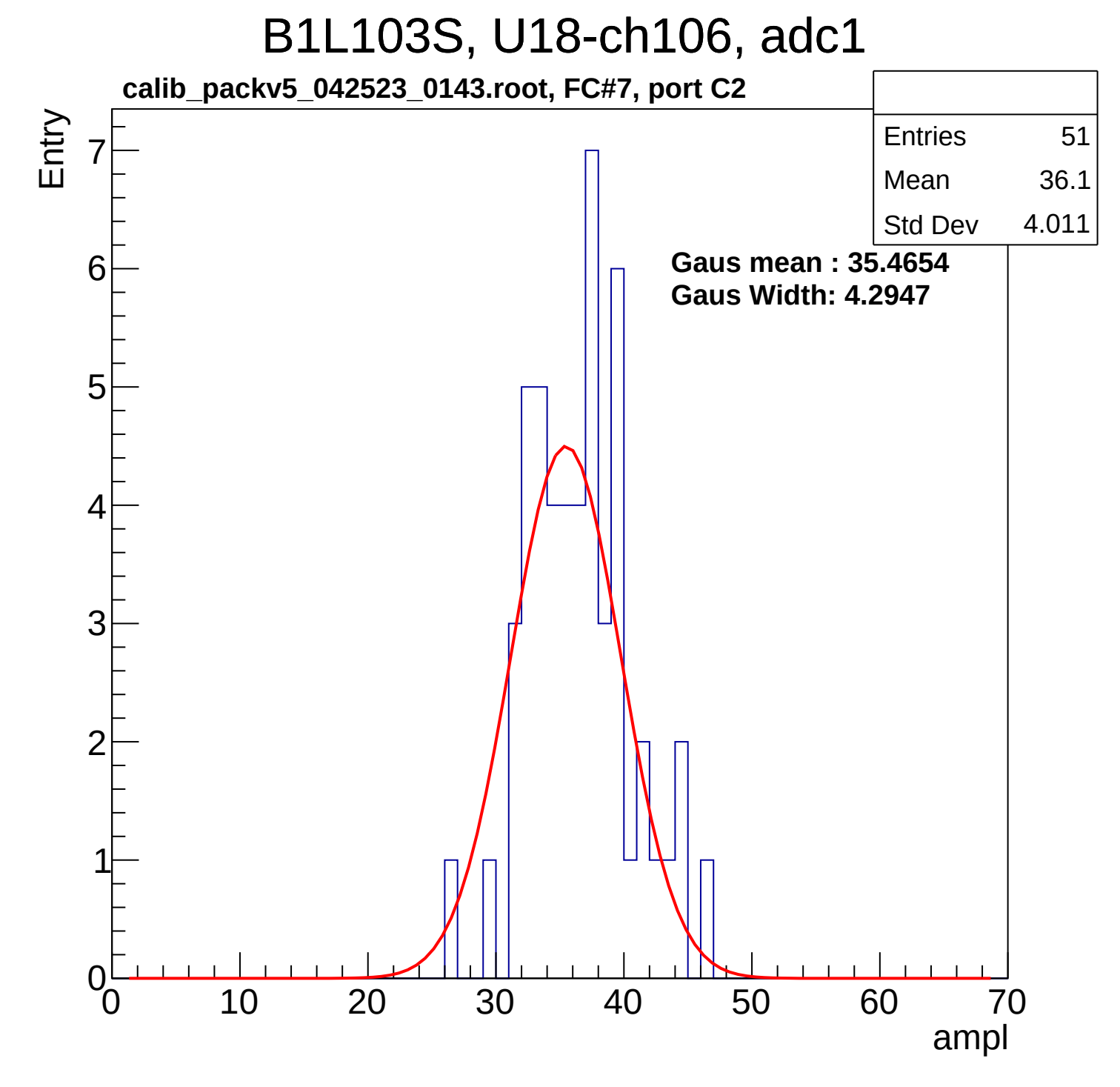
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch106, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 51
Mean 36.1
Std Dev 4.011
Gaus mean : 35.4654
Gaus Width: 4.2947
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
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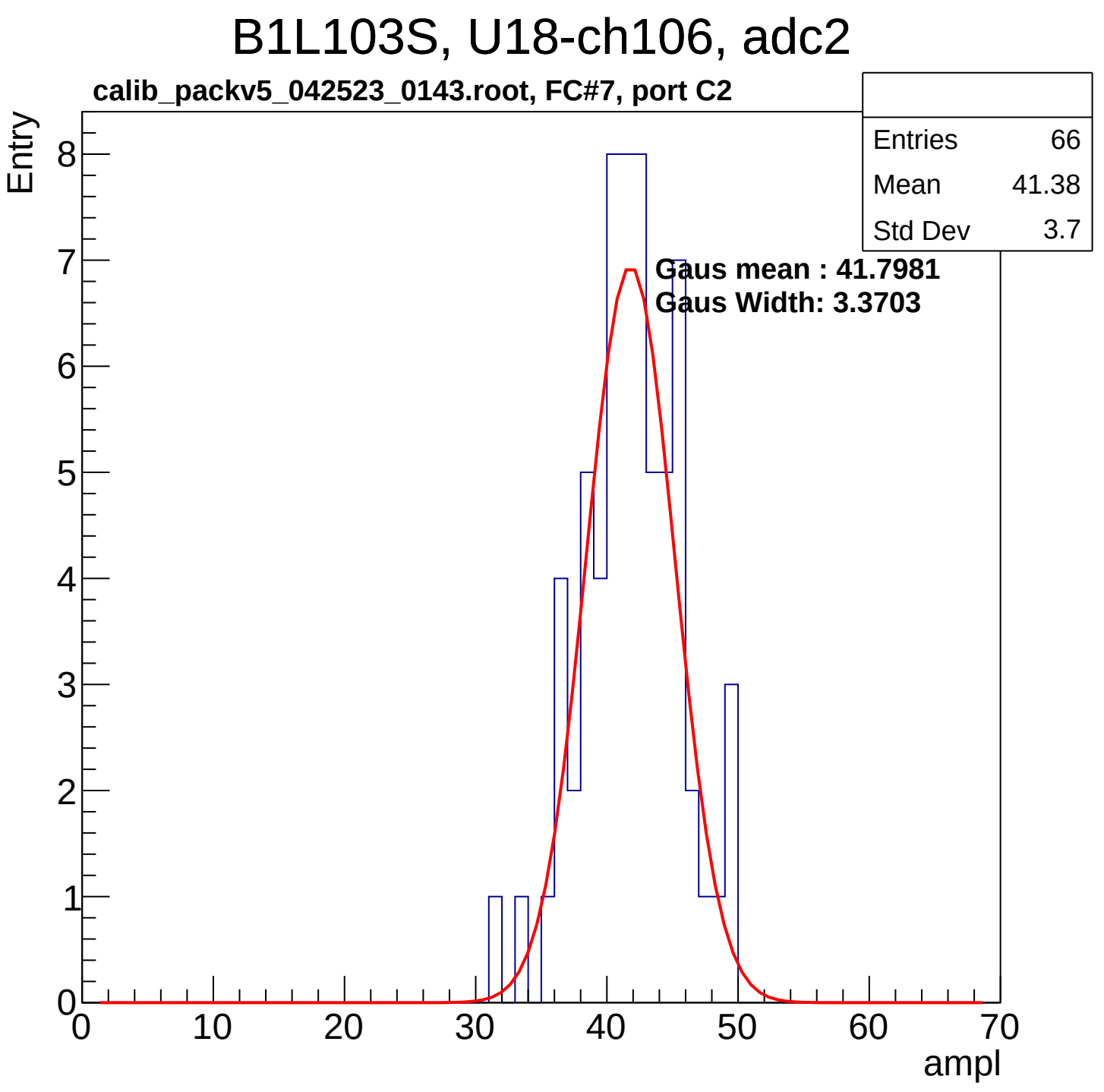
40
50
60
70


B1L103S, U18-ch106, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 41.38
Std Dev 3.7
Gaus mean : 41.7981
Gaus Width: 3.3703
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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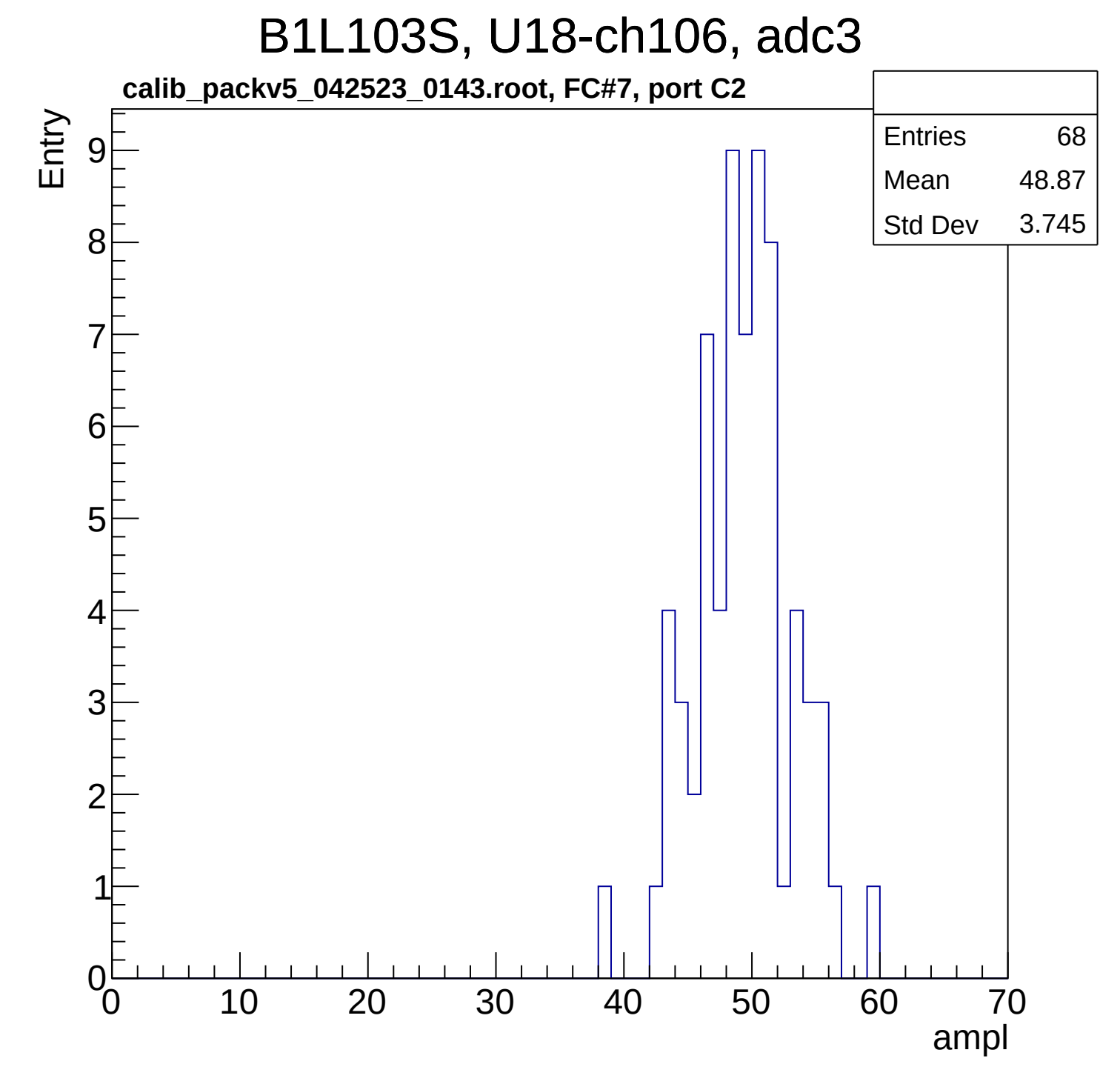
B1L103S, U18-ch106, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 48.87
Std Dev 3.745
Entry
ampl
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0
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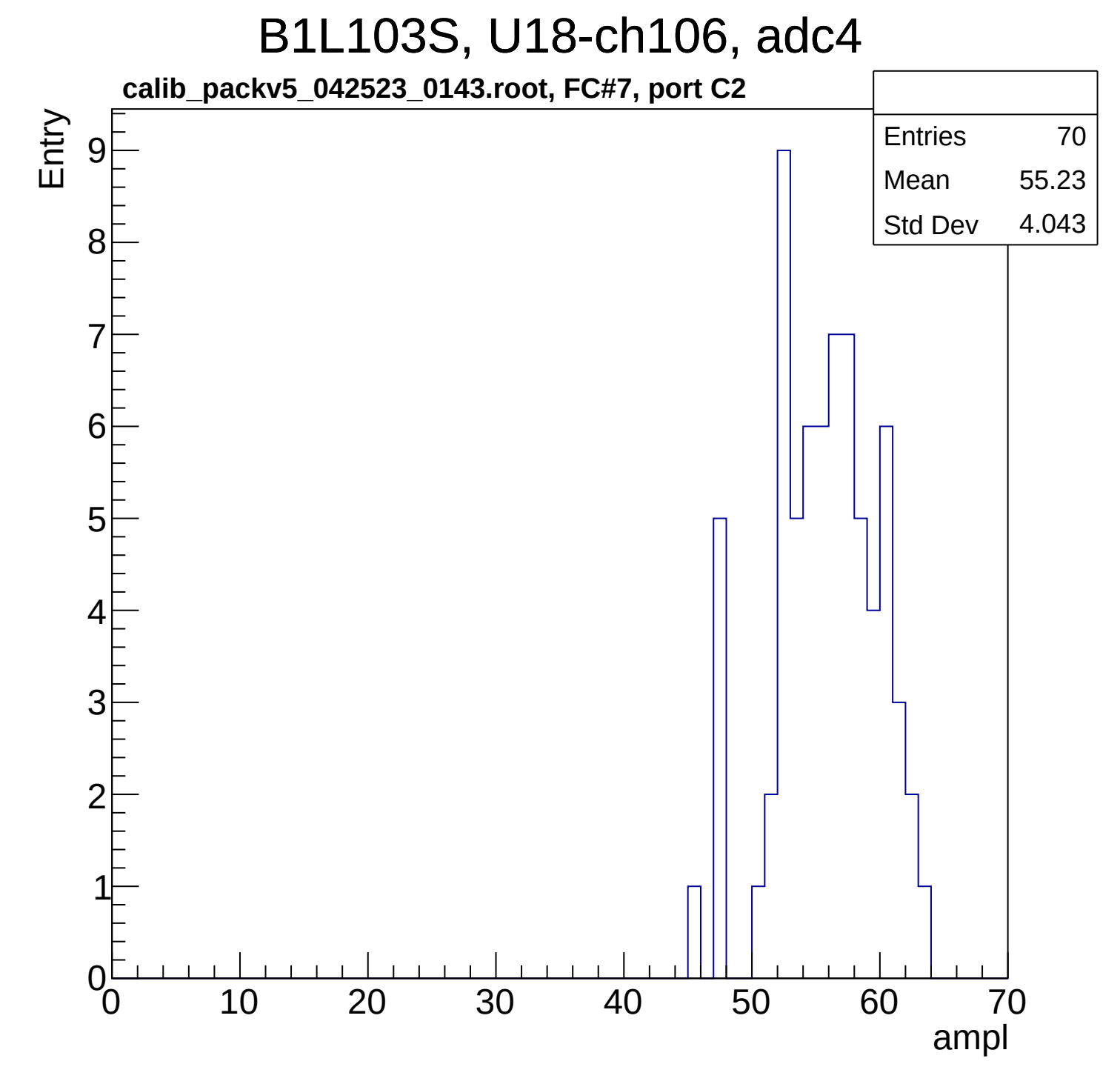
60
70


B1L103S, U18-ch106, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 55.23
Std Dev 4.043
Entry
ampl
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3
4
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7
8
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0
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40
50
60
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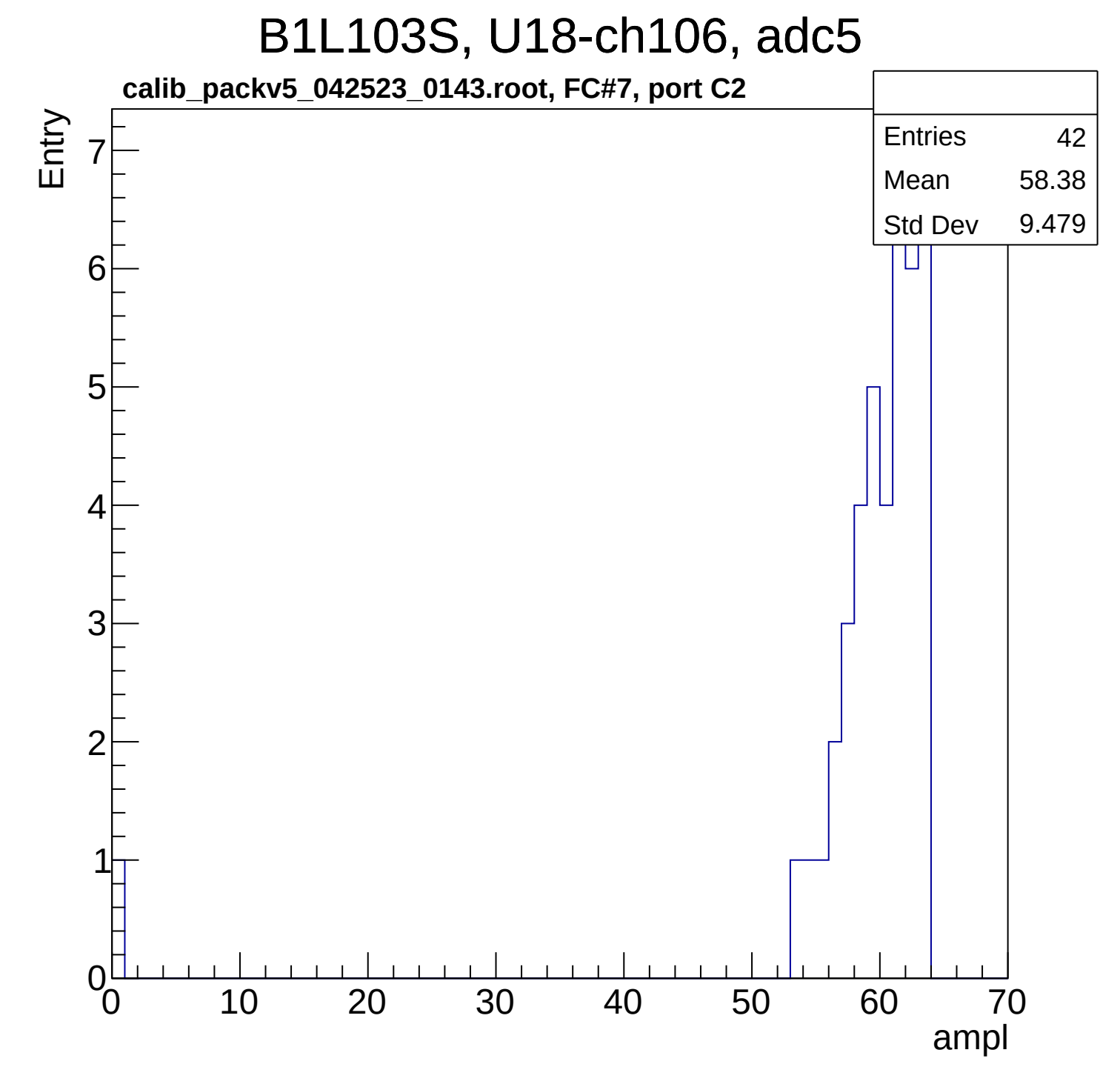
B1L103S, U18-ch106, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 42
Mean 58.38
Std Dev 9.479
Entry
ampl
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0
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60
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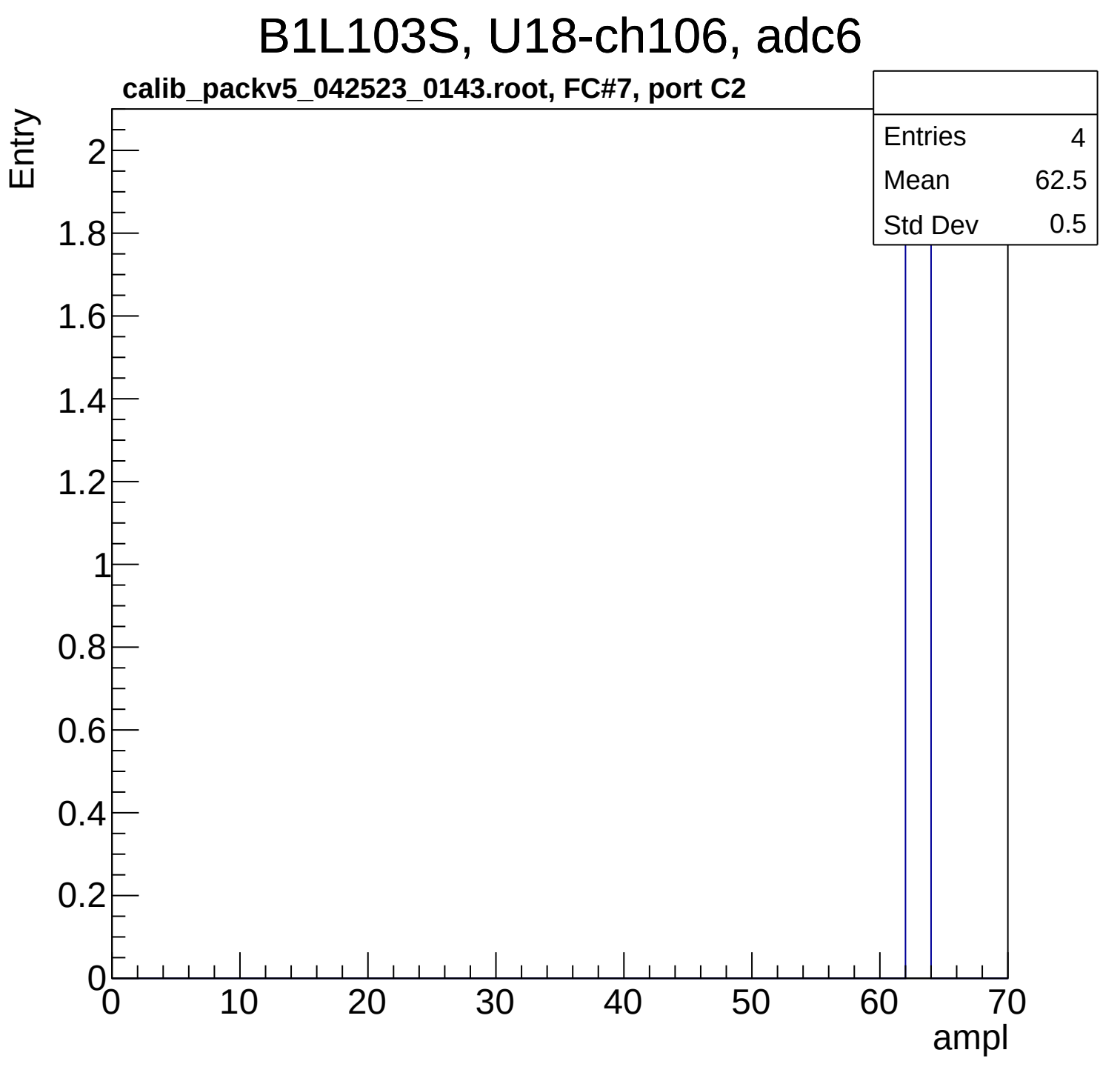
B1L103S, U18-ch106, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 4
Mean 62.5
Std Dev 0.5
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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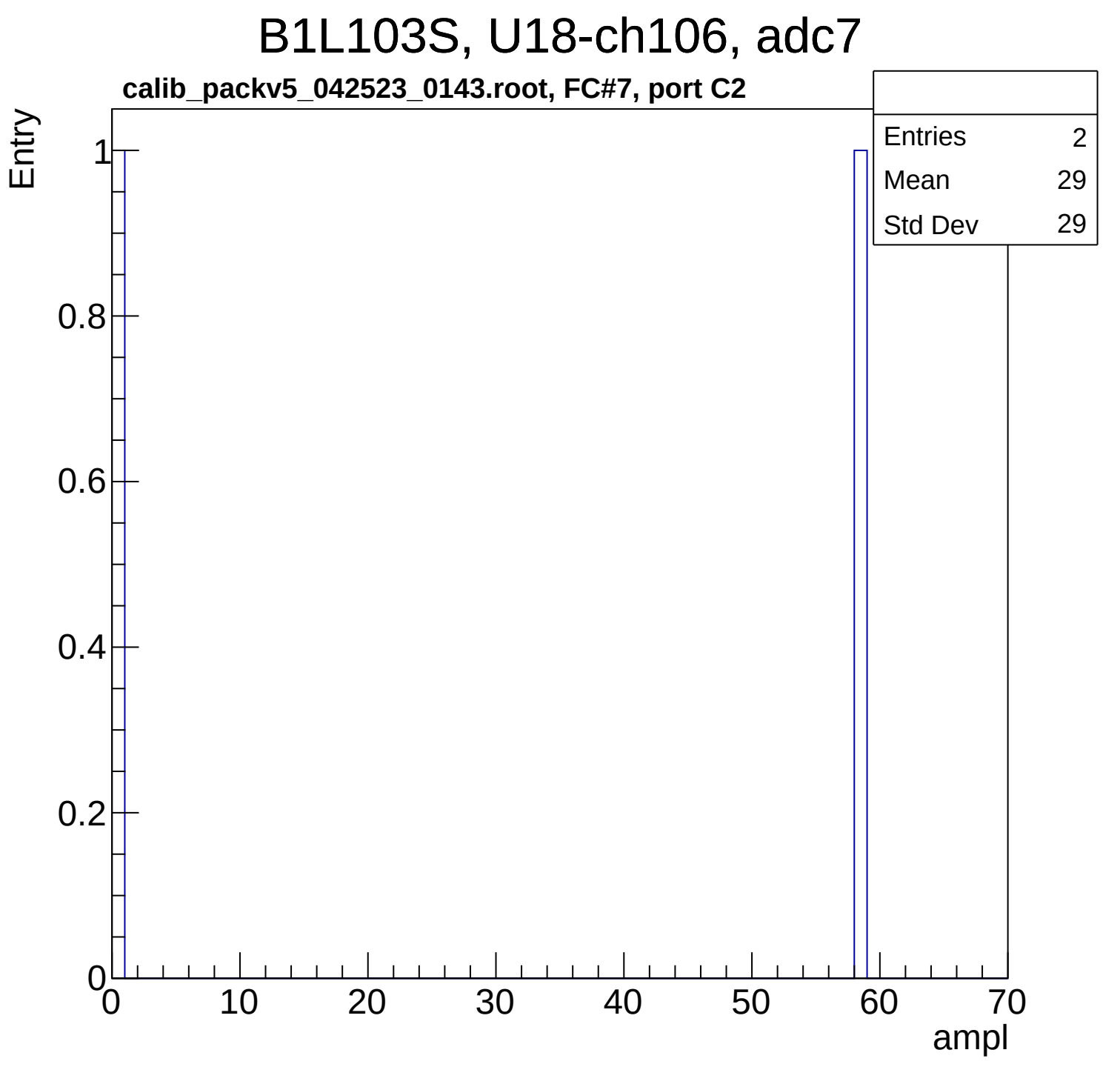
40
50
60
70


B1L103S, U18-ch106, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 29
Std Dev 29
Entry
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0.6
0.4
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10
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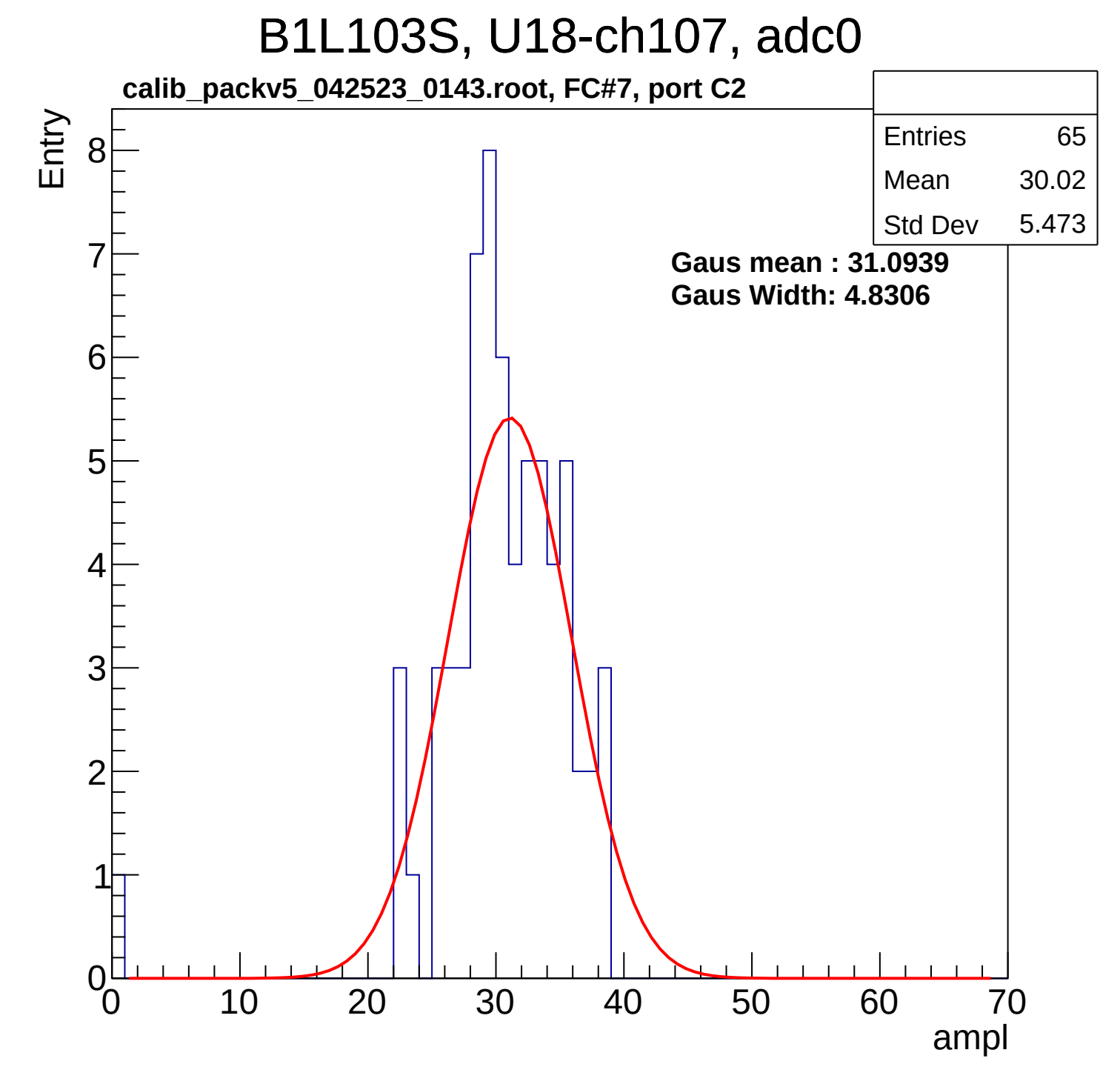
50
60
70
ampl


B1L103S, U18-ch107, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 30.02
Std Dev 5.473
Gaus mean : 31.0939
Gaus Width: 4.8306
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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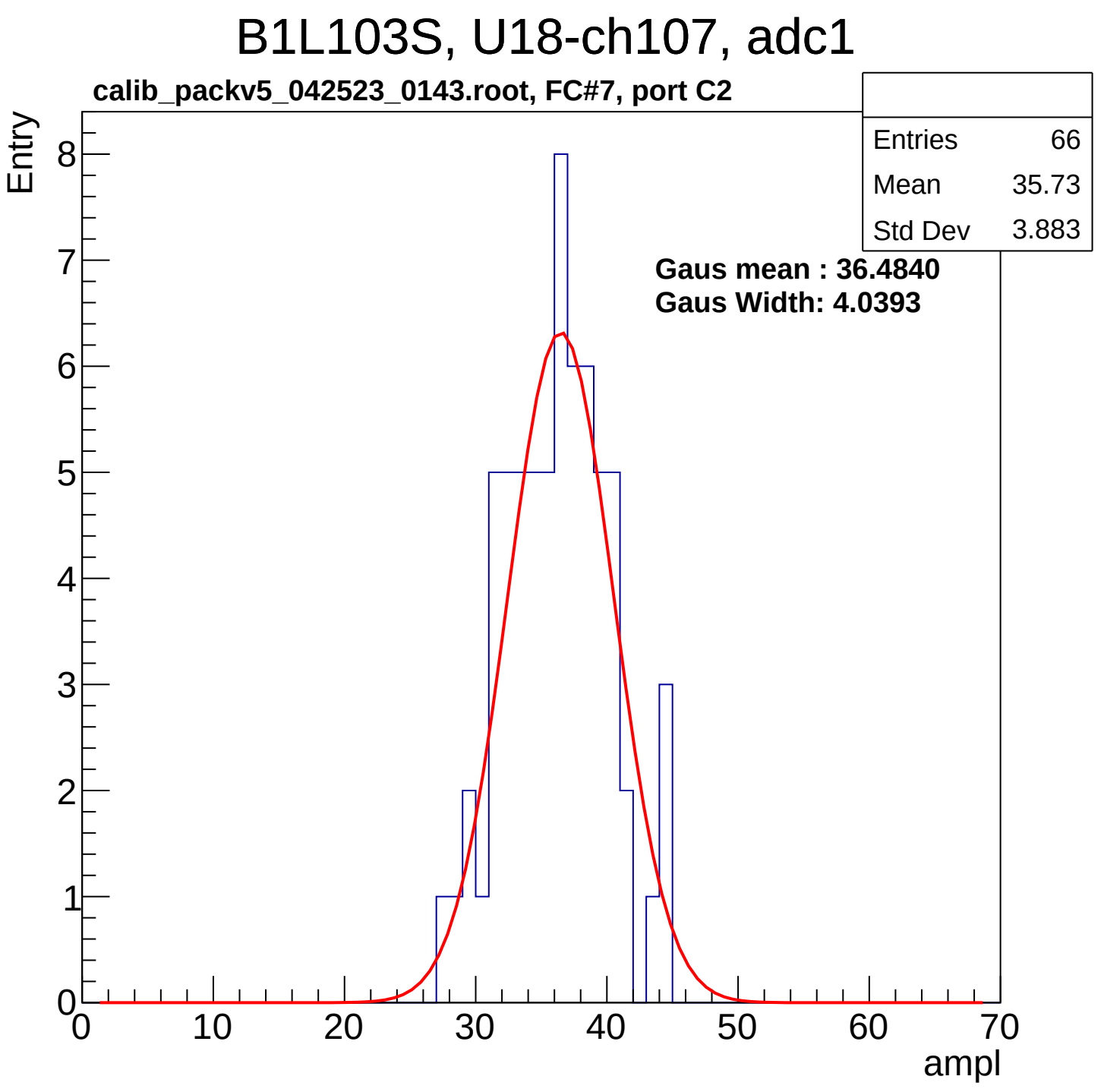
B1L103S, U18-ch107, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 35.73
Std Dev 3.883
Gaus mean : 36.4840
Gaus Width: 4.0393
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
50
60
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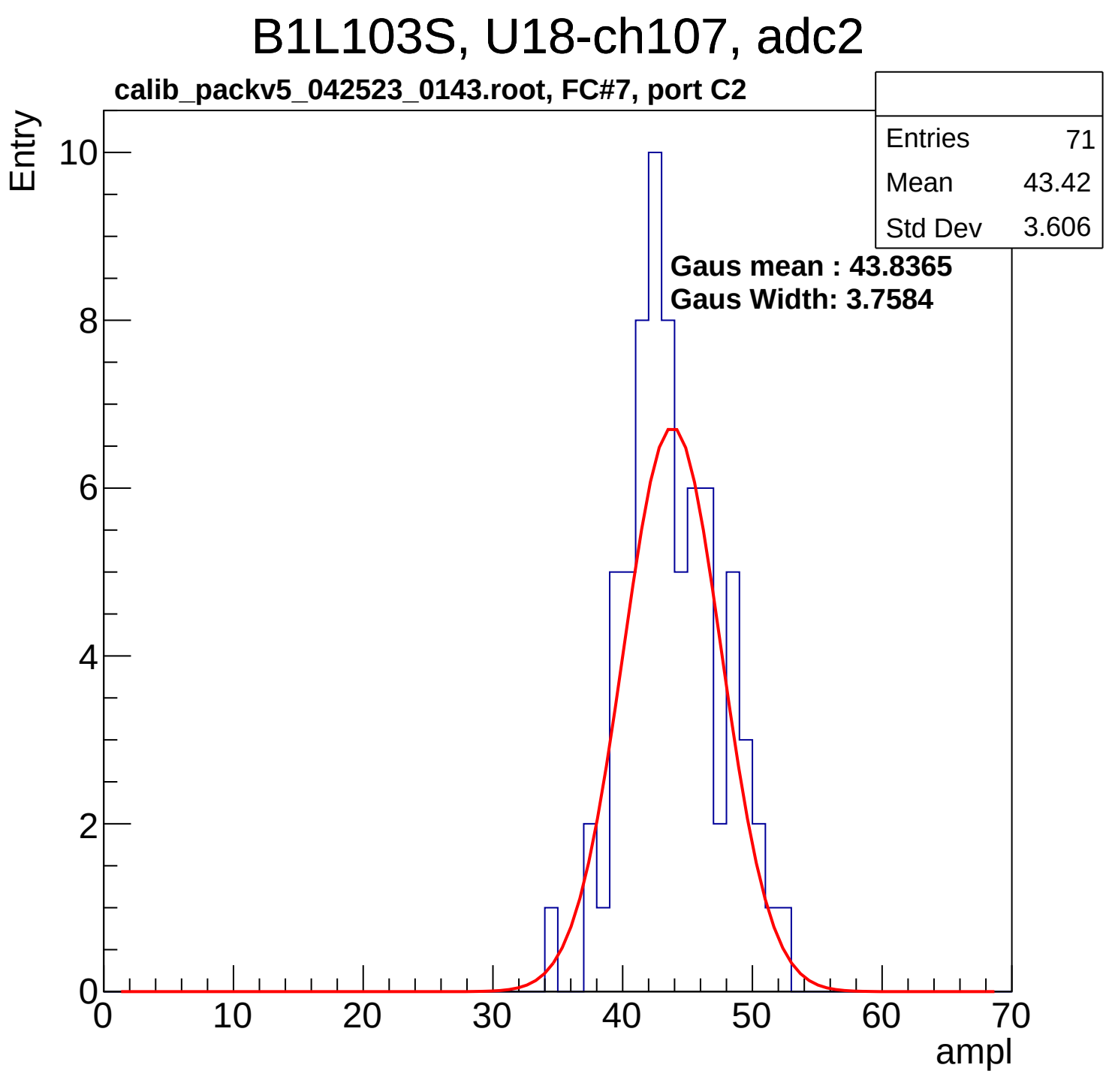
B1L103S, U18-ch107, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 71
Mean 43.42
Std Dev 3.606
Gaus mean : 43.8365
Gaus Width: 3.7584
Entry
ampl
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60
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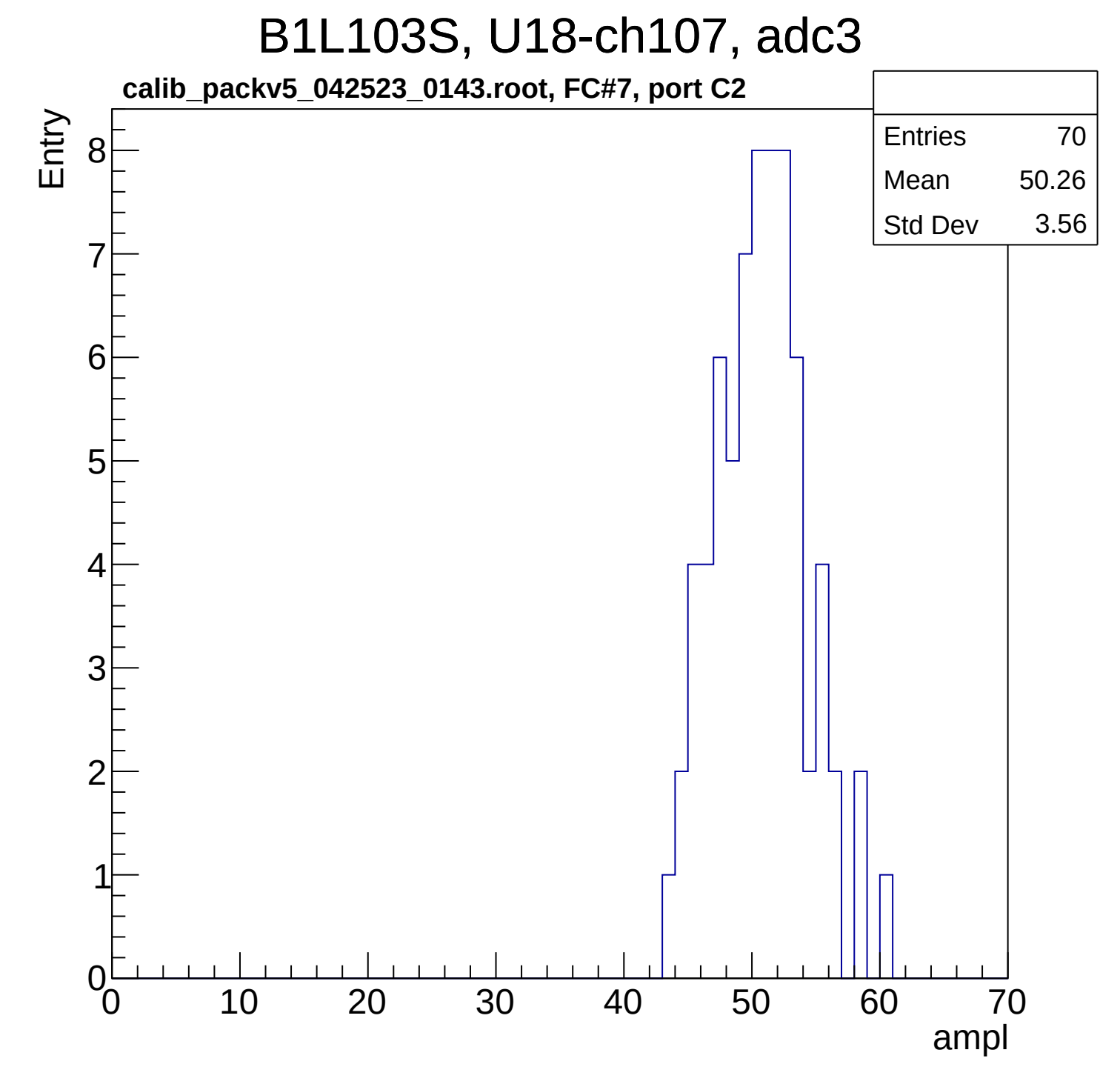
B1L103S, U18-ch107, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 50.26
Std Dev 3.56
Entry
ampl
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2
3
4
5
6
7
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60
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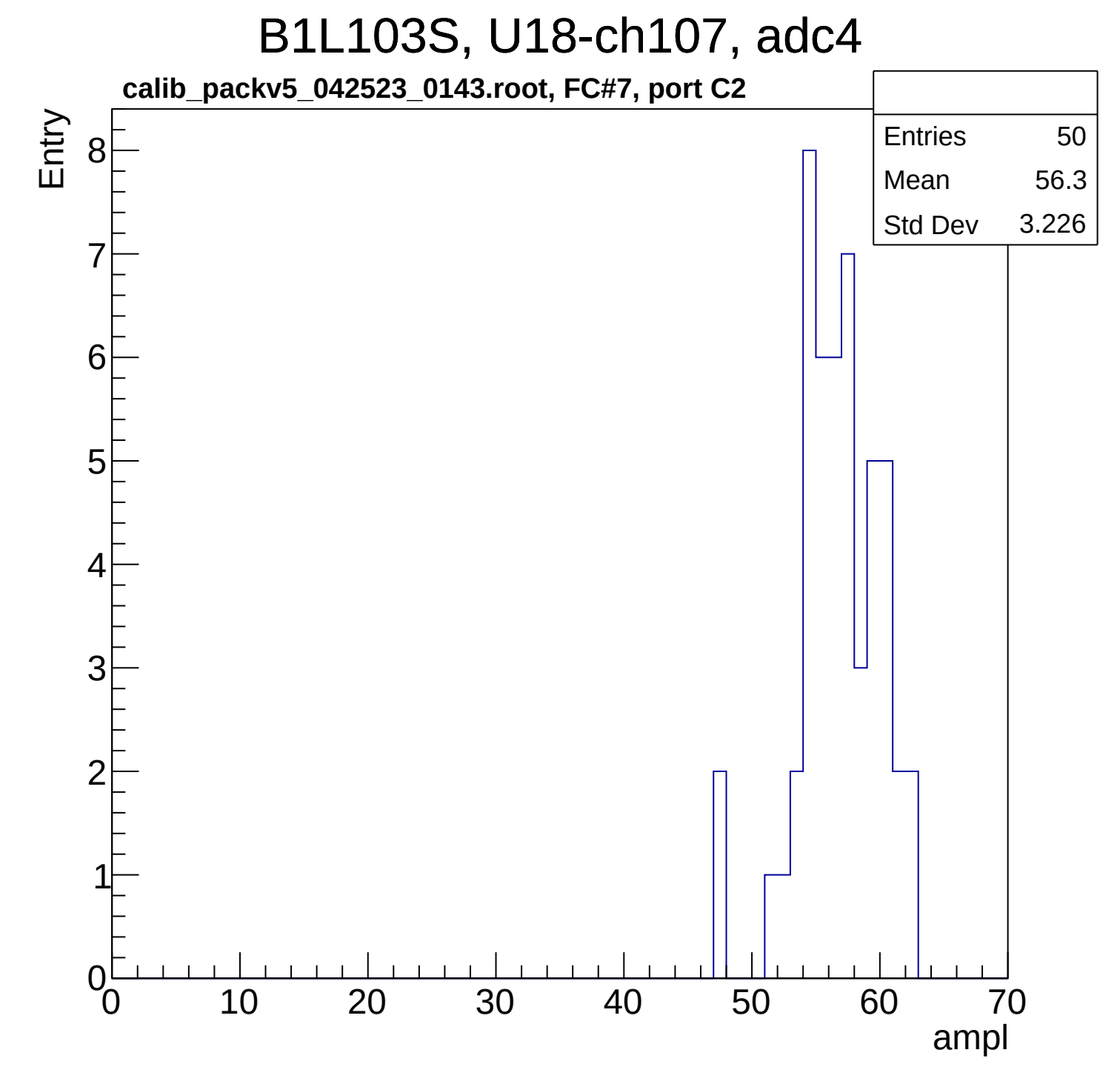
B1L103S, U18-ch107, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 50
Mean 56.3
Std Dev 3.226
Entry
ampl
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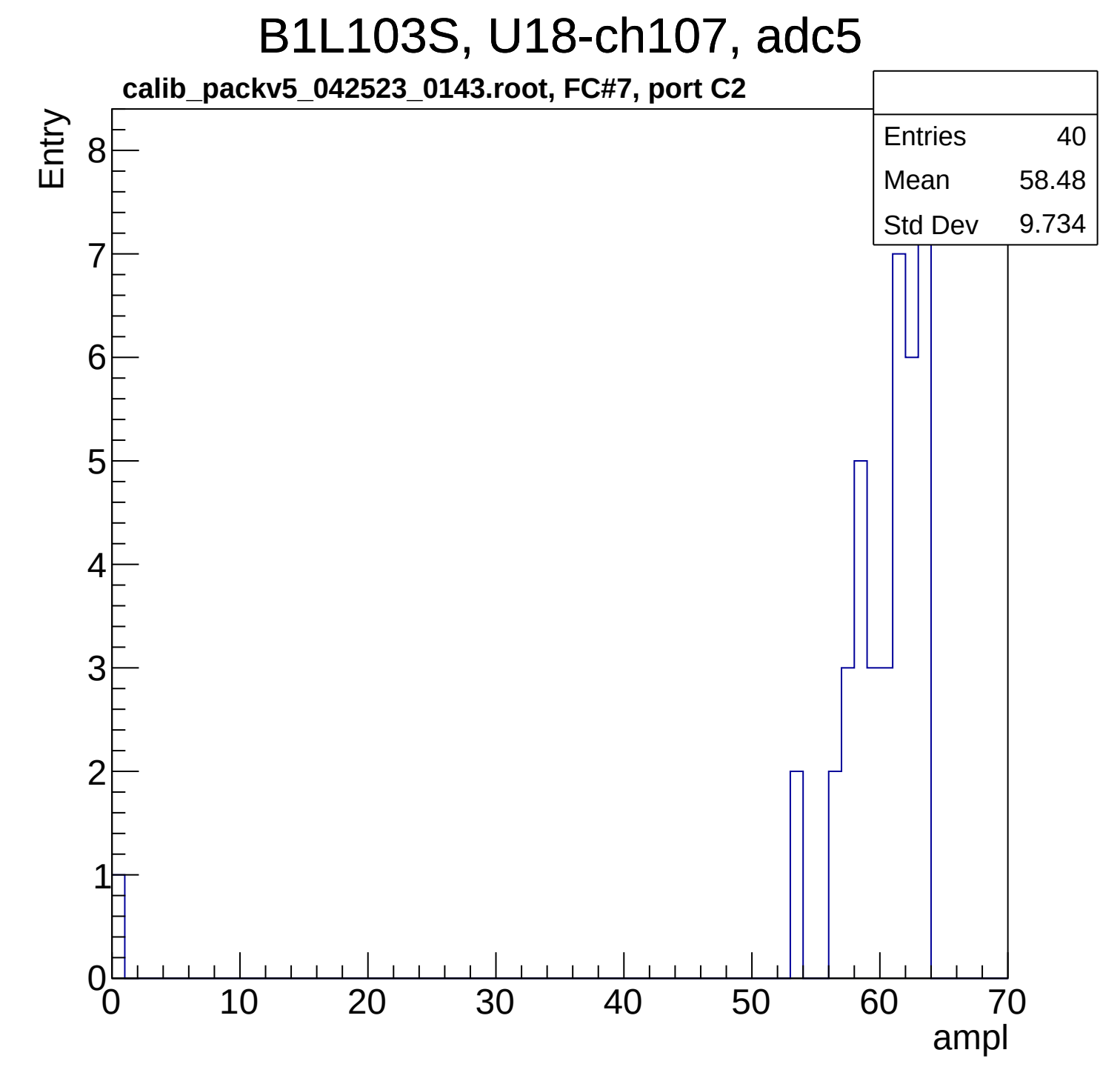
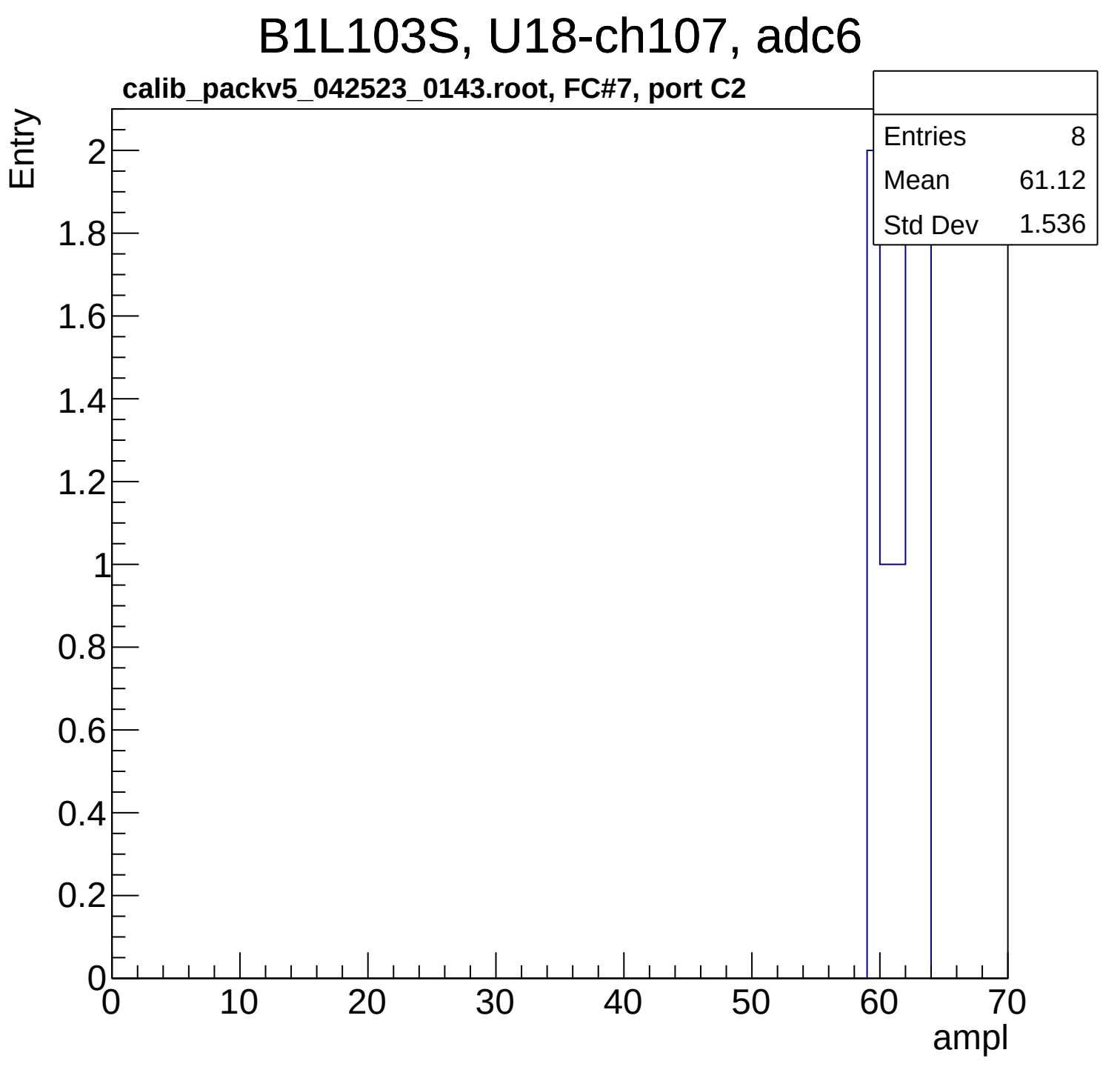

B1L103S, U18-ch107, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 40
Mean 58.48
Std Dev 9.734
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch107, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 8
Mean 61.12
Std Dev 1.536
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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40
50
60
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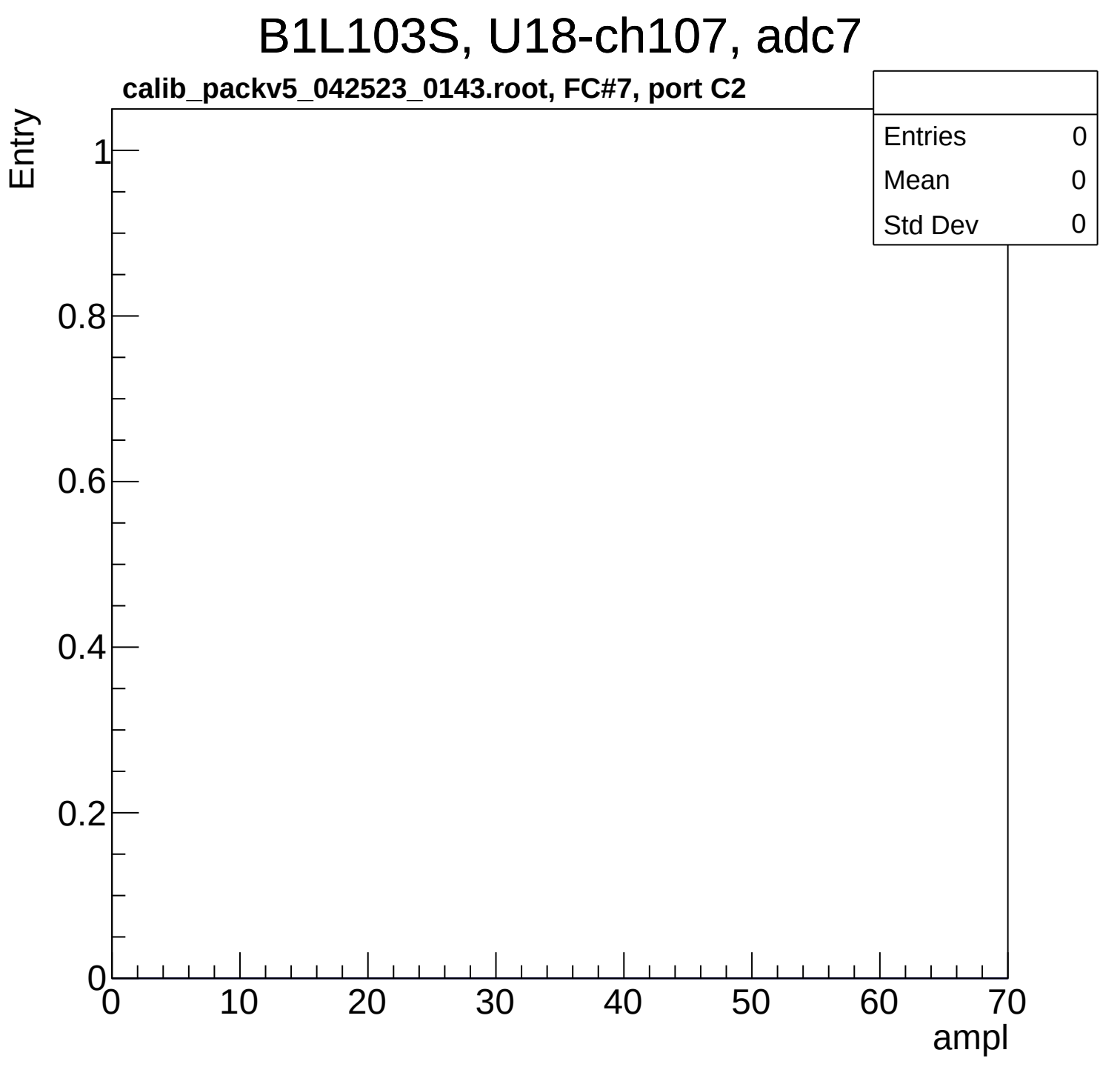
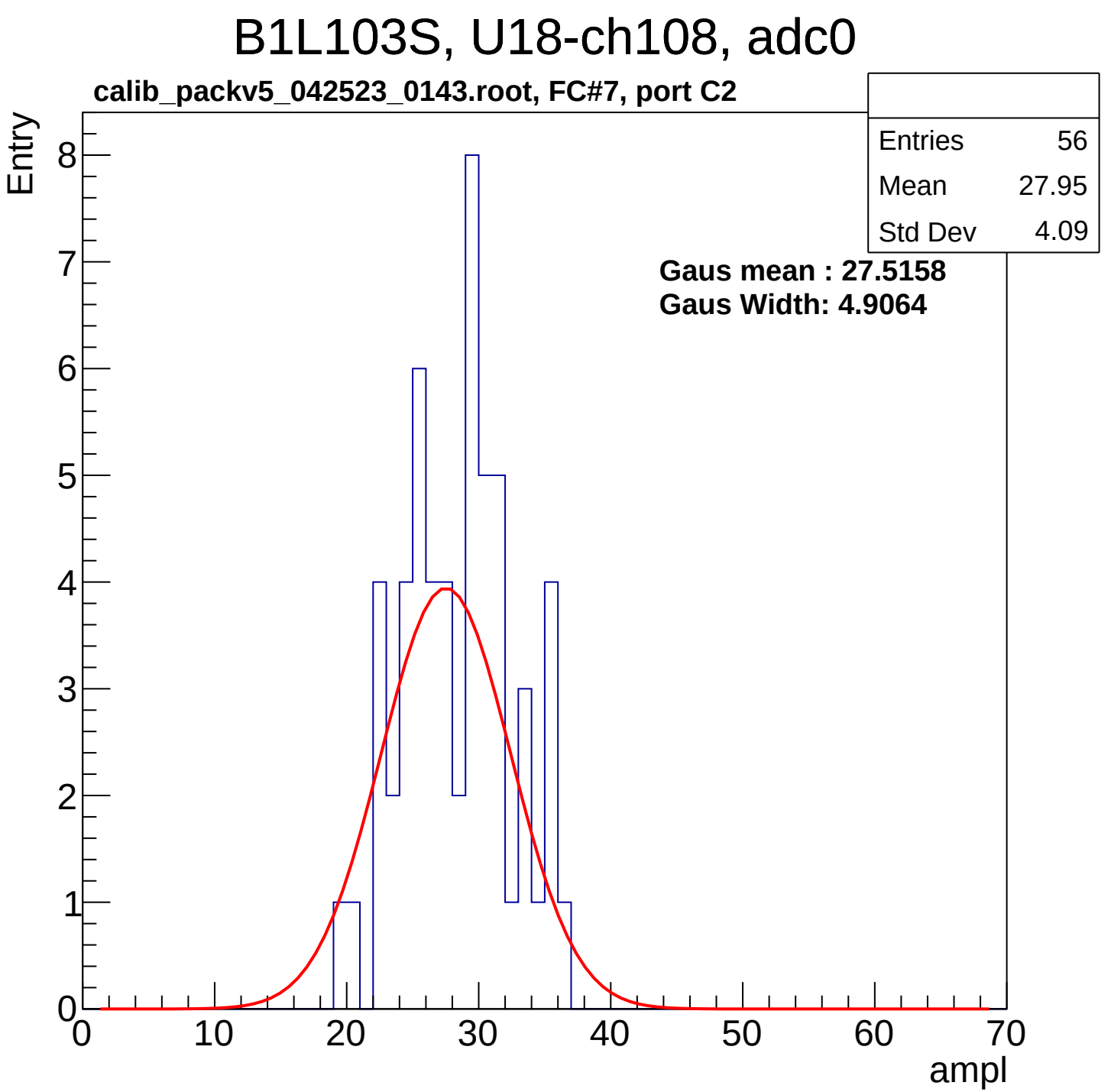

B1L103S, U18-ch107, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch108, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 27.95
Std Dev 4.09
Gaus mean : 27.5158
Gaus Width: 4.9064
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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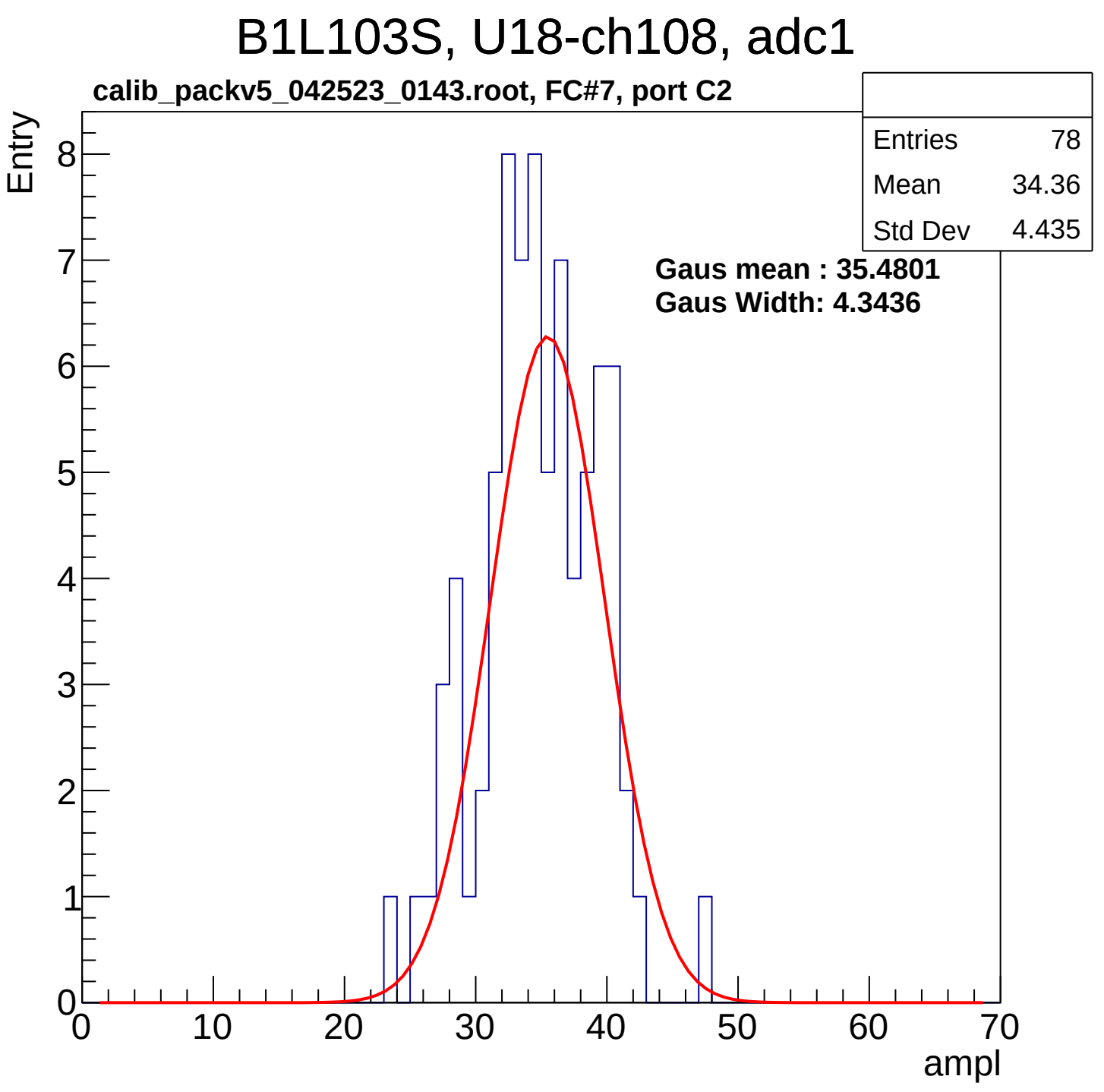
B1L103S, U18-ch108, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 78
Mean 34.36
Std Dev 4.435
Gaus mean : 35.4801
Gaus Width: 4.3436
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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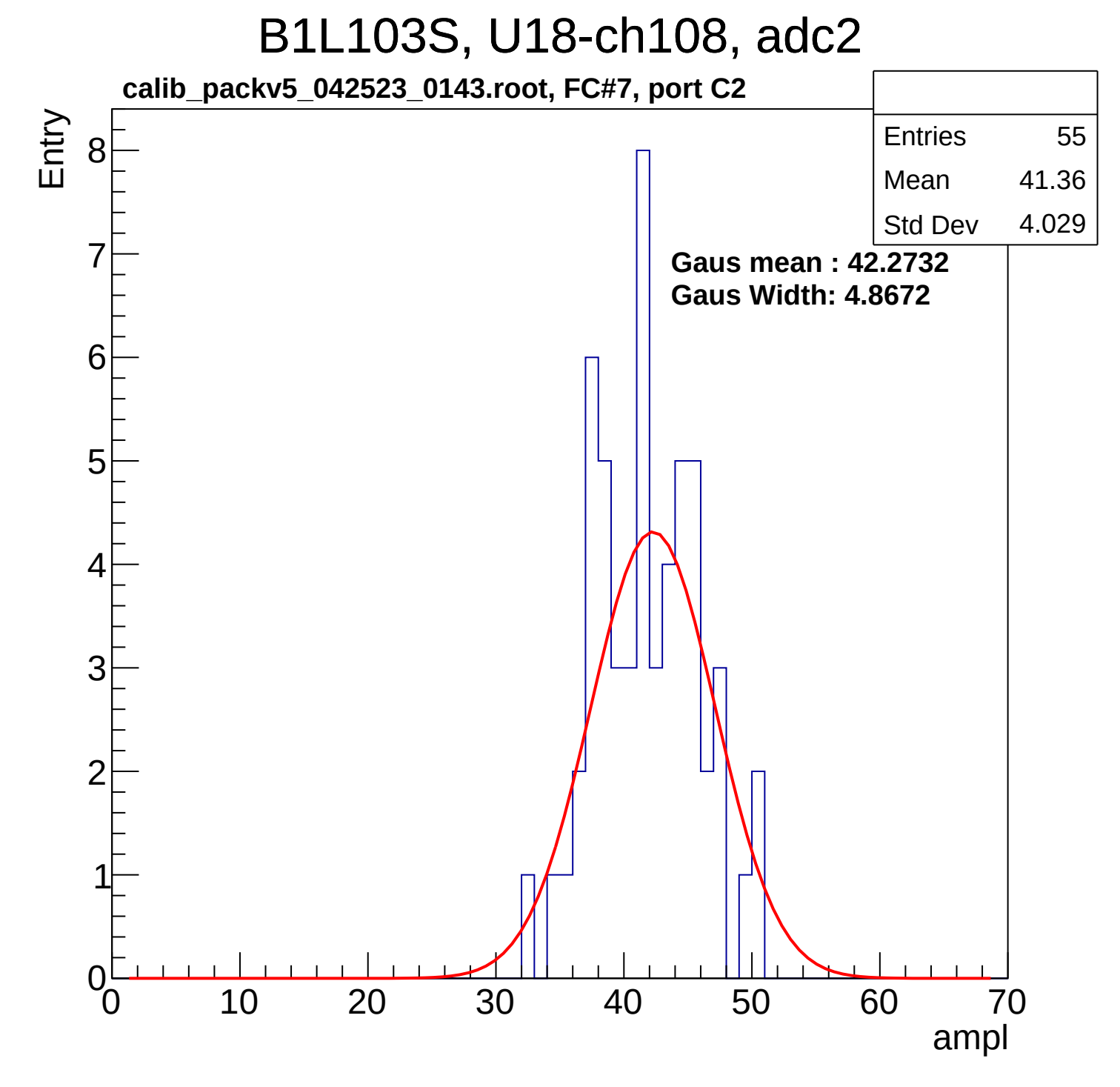
B1L103S, U18-ch108, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 41.36
Std Dev 4.029
Gaus mean : 42.2732
Gaus Width: 4.8672
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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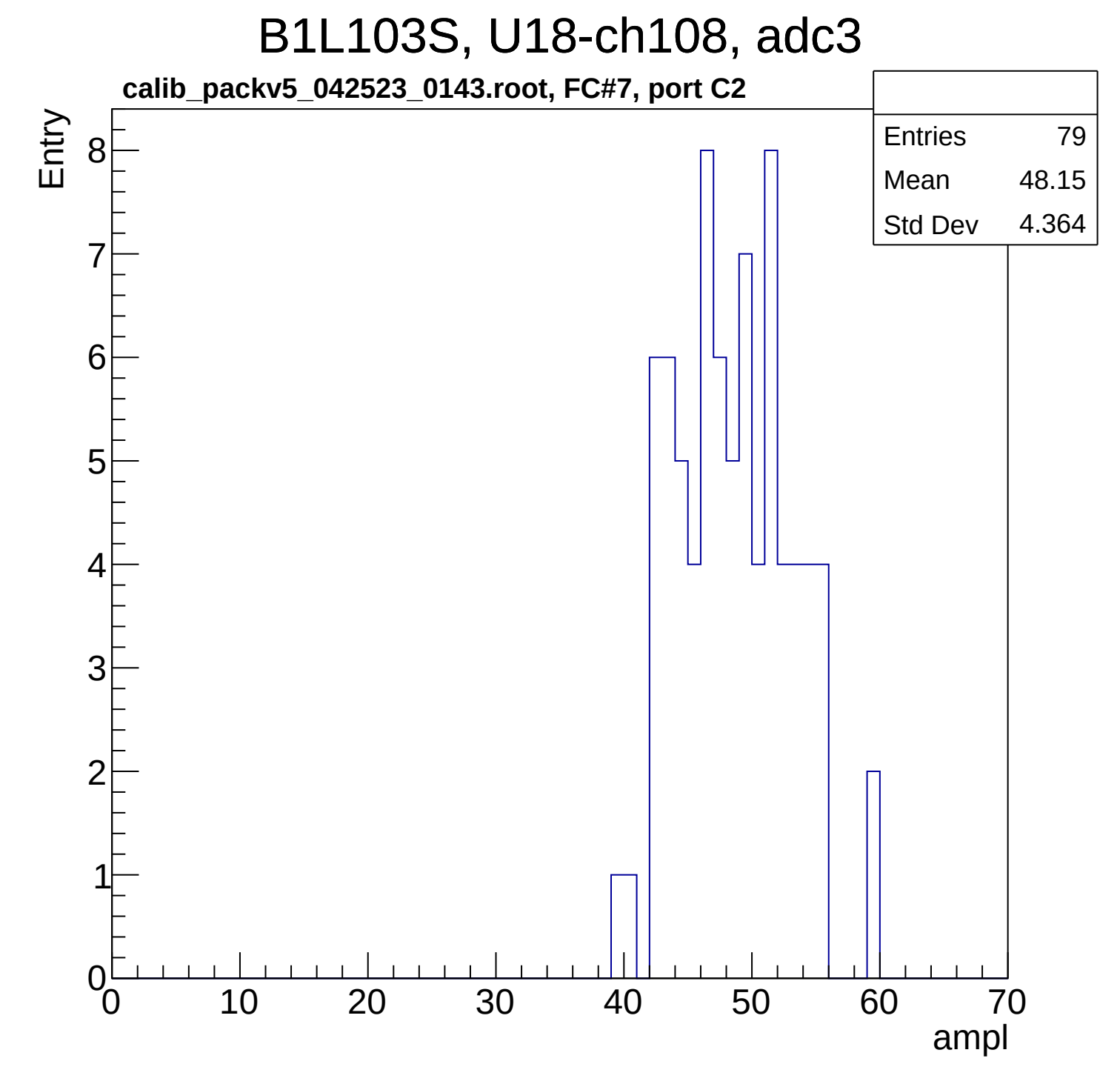
B1L103S, U18-ch108, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 79
Mean 48.15
Std Dev 4.364
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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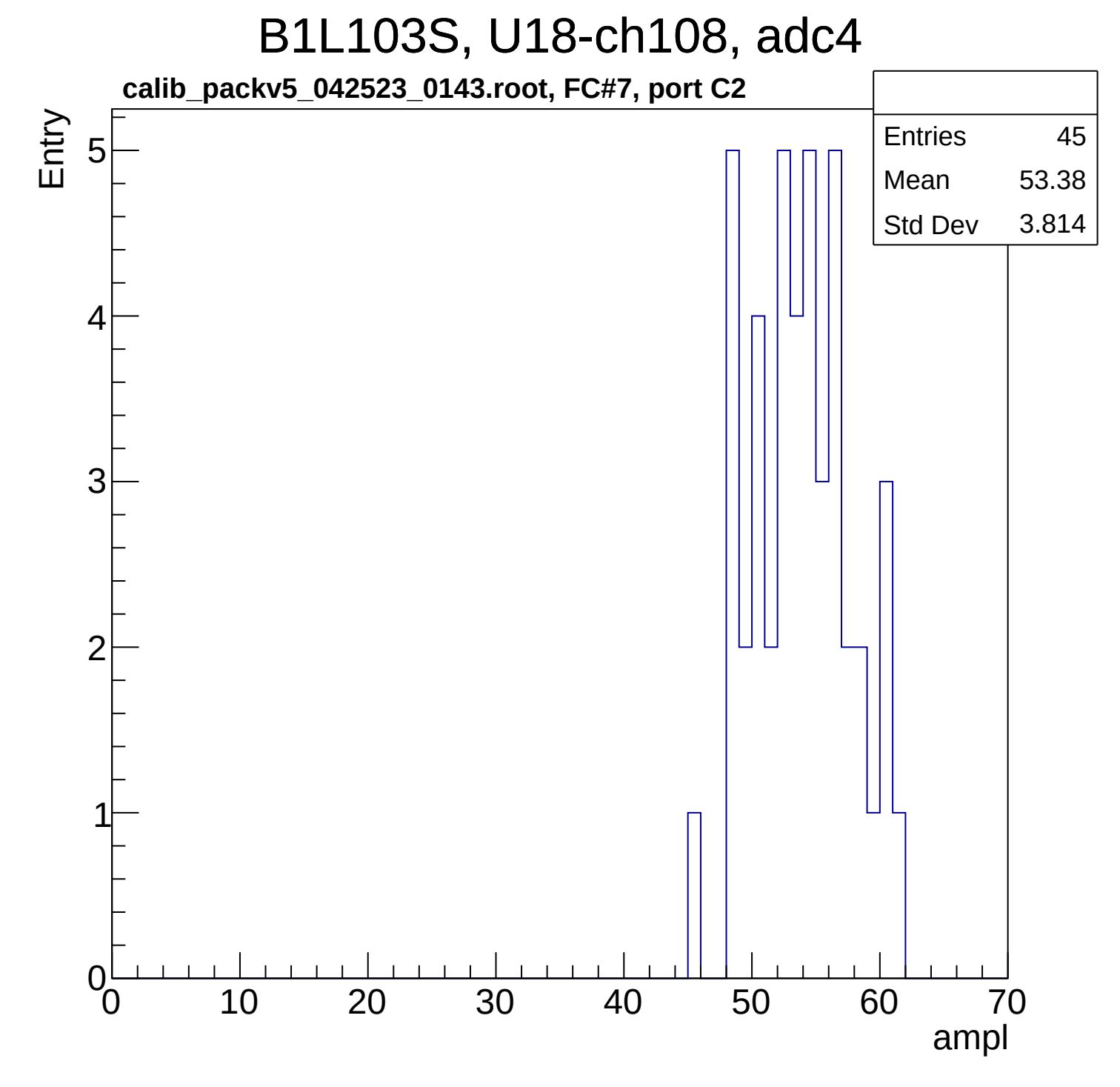
B1L103S, U18-ch108, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 45
Mean 53.38
Std Dev 3.814
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
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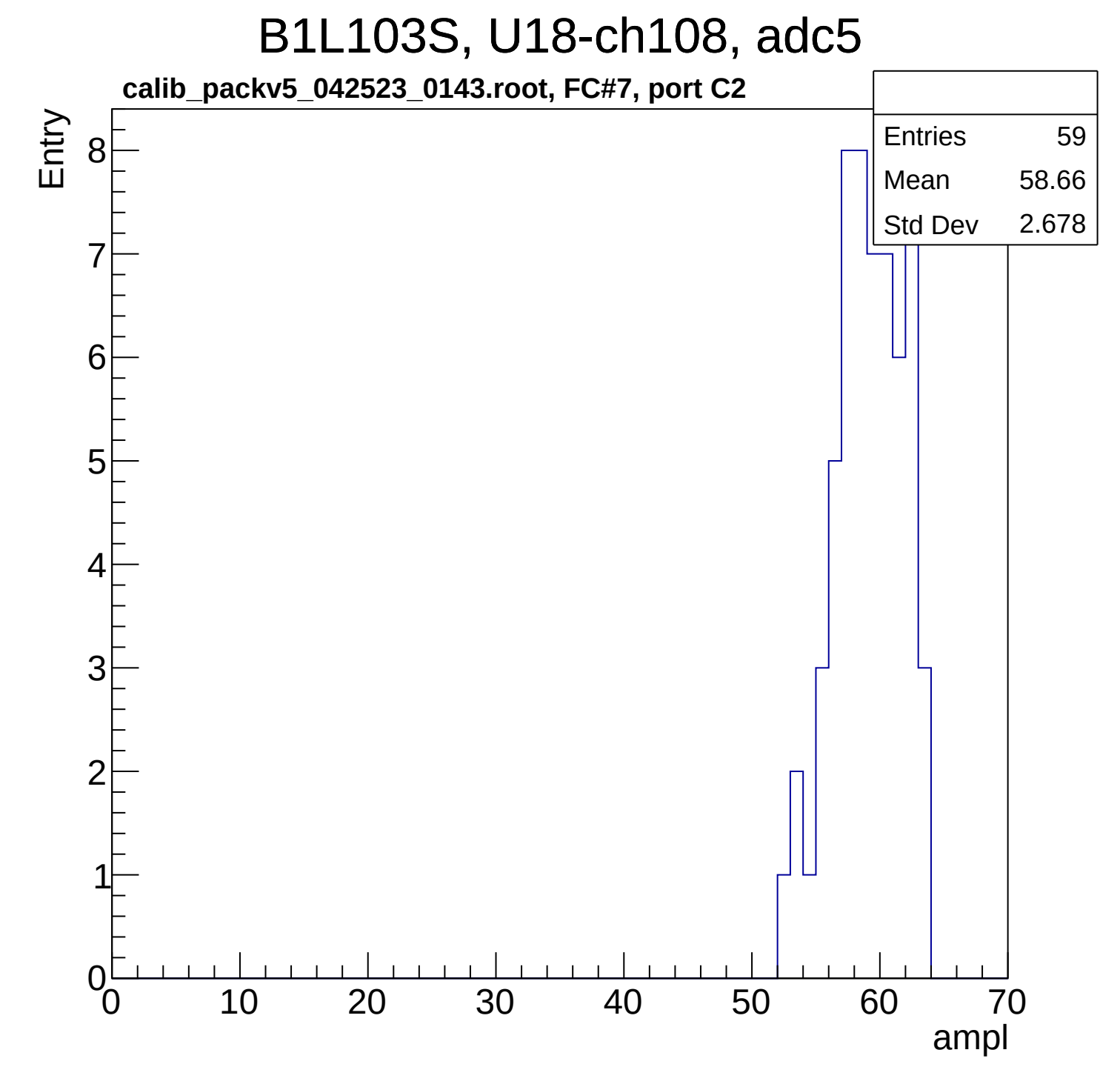
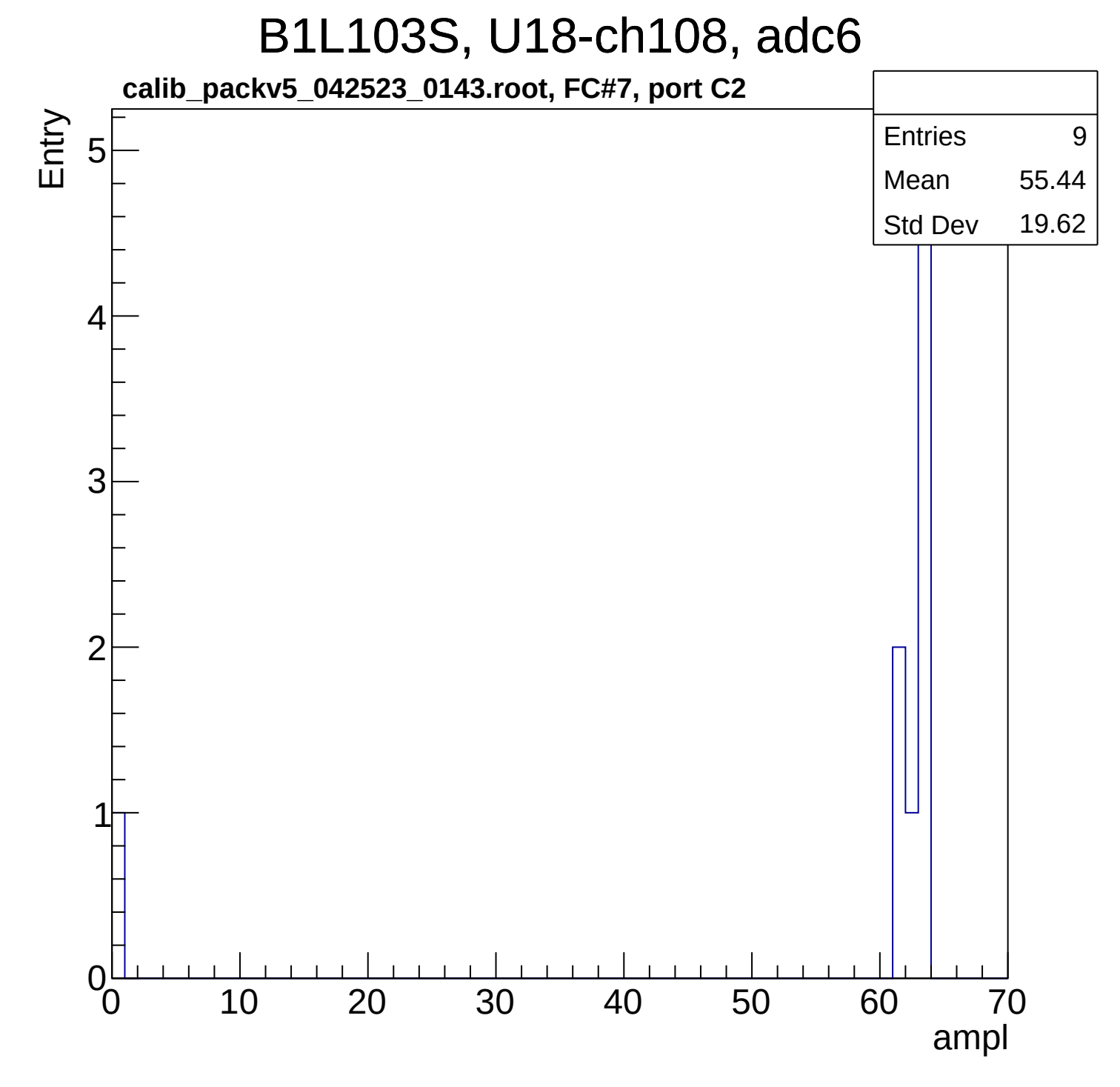
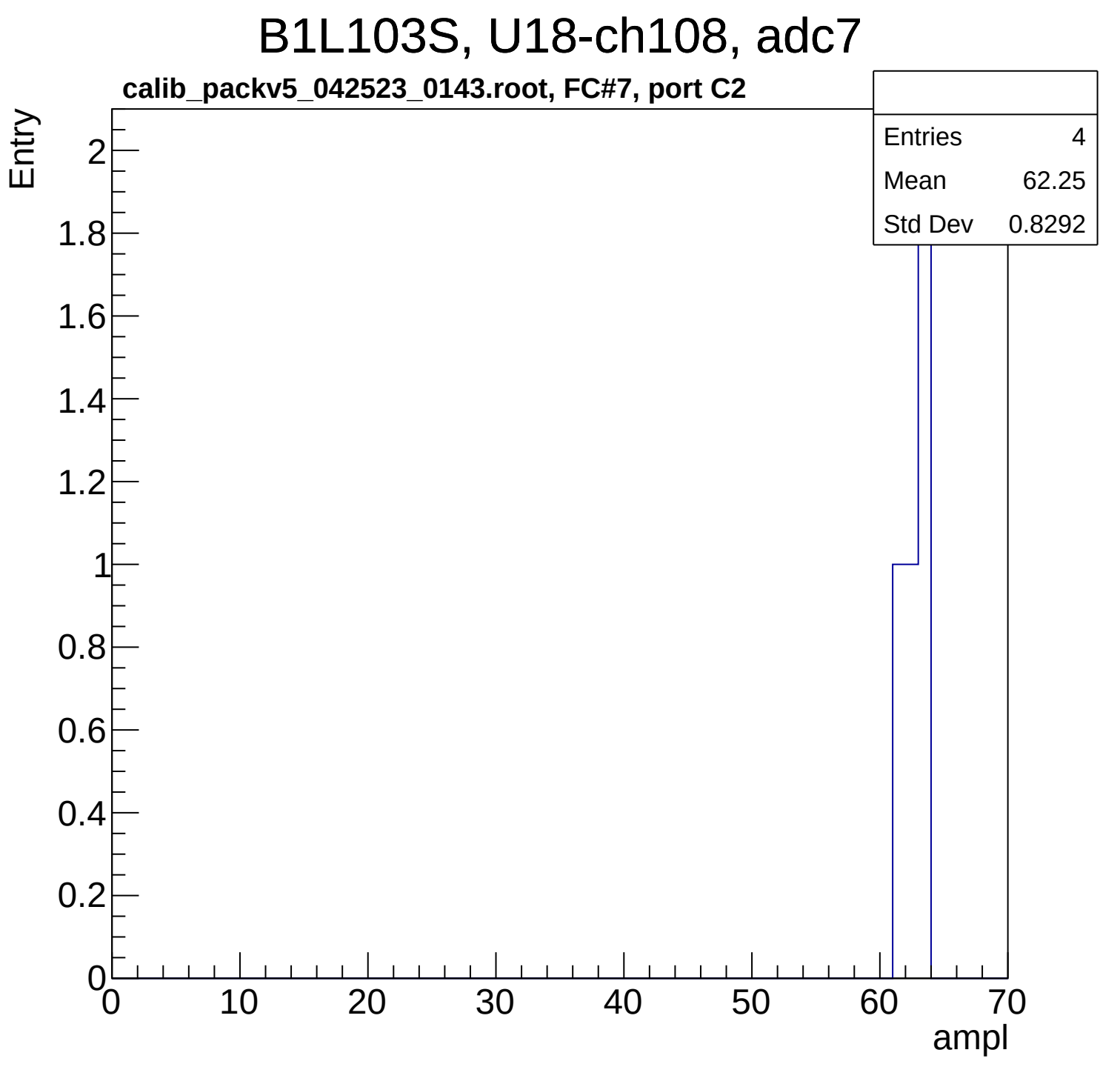
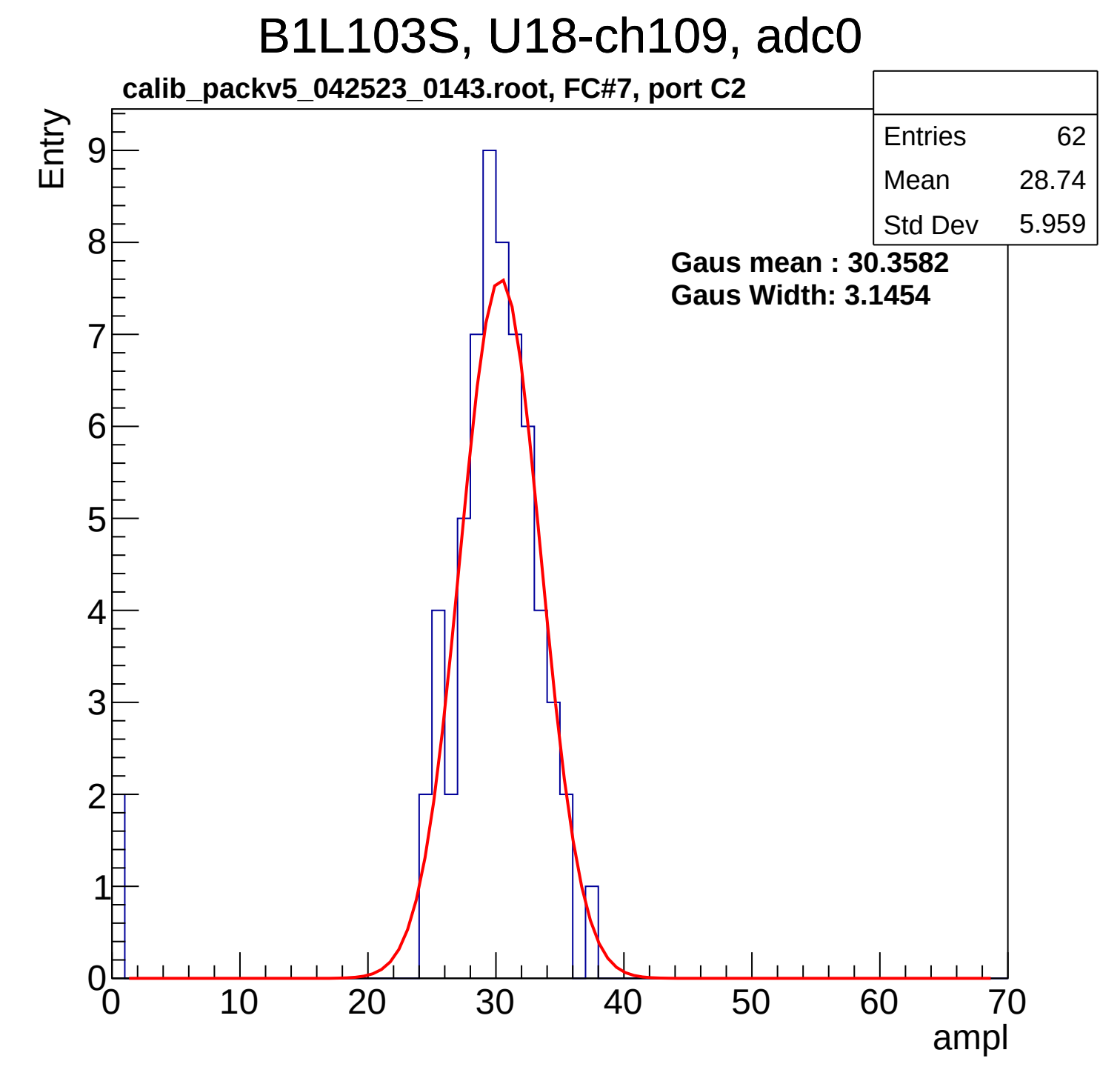

B1L103S, U18-ch108, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 58.66
Std Dev 2.678
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch108, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 9
Mean 55.44
Std Dev 19.62
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U18-ch108, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 4
Mean 62.25
Std Dev 0.8292
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U18-ch109, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 62
Mean 28.74
Std Dev 5.959
Gaus mean : 30.3582
Gaus Width: 3.1454
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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20
30
40
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60
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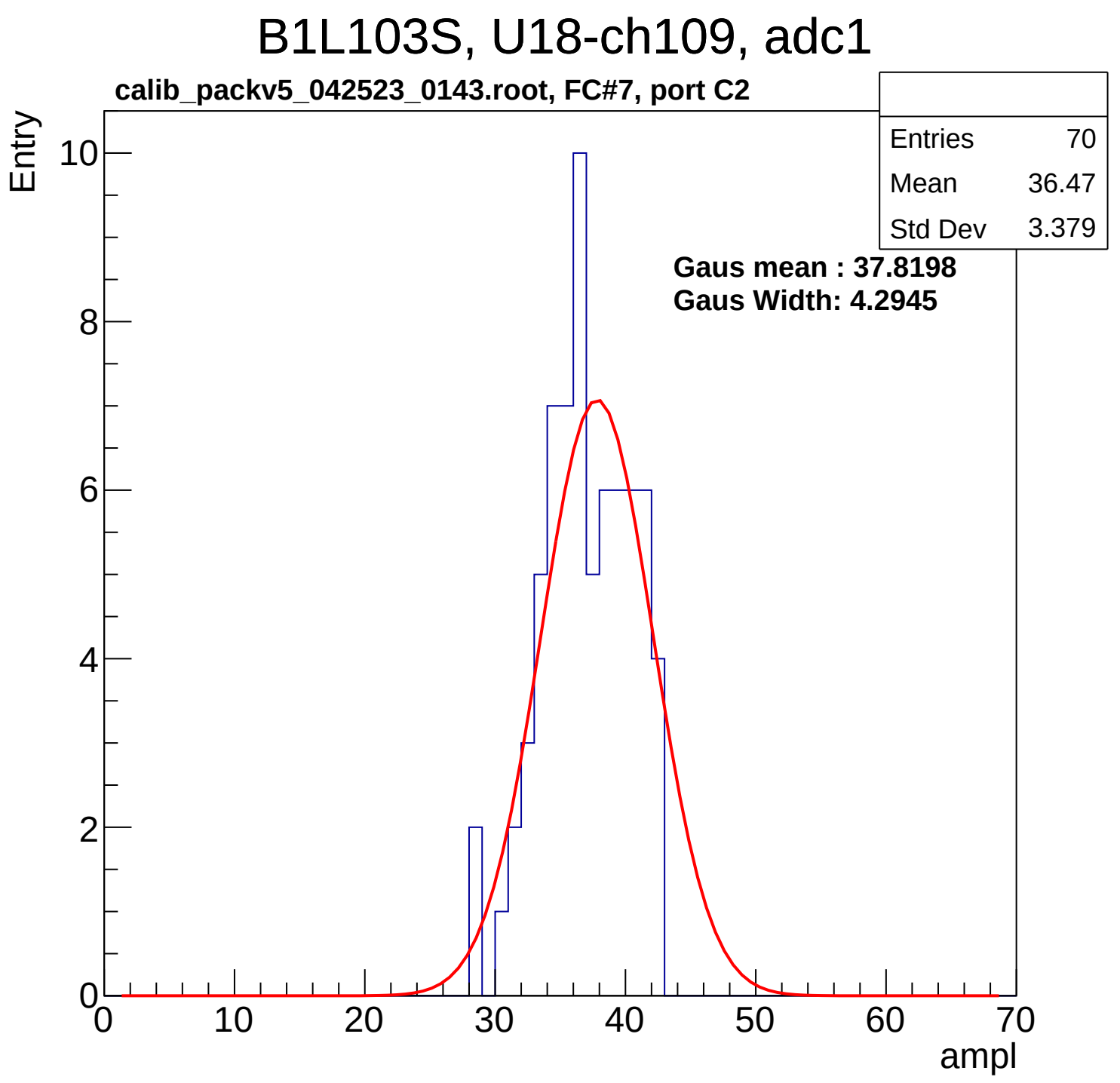
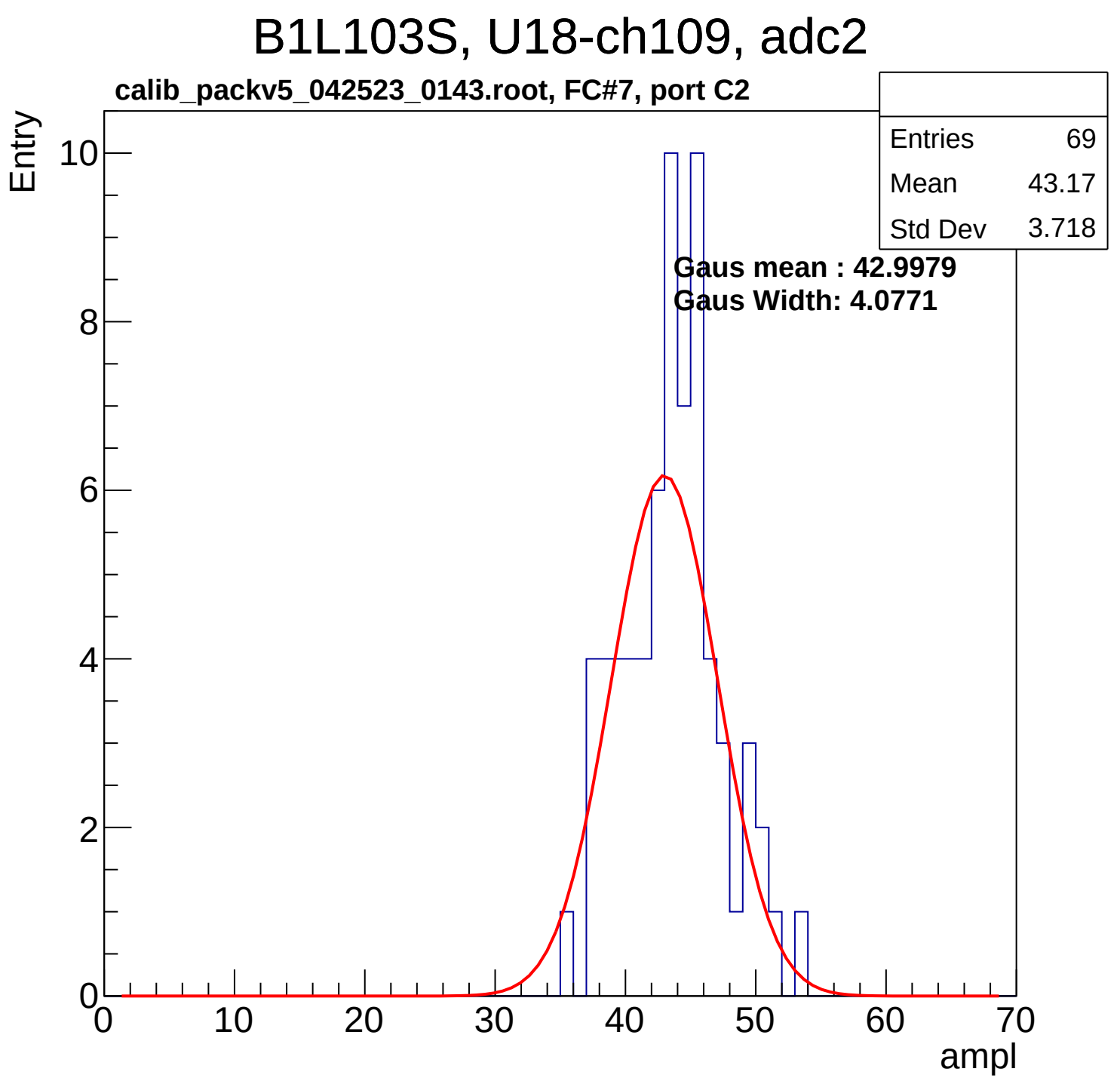

B1L103S, U18-ch109, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 36.47
Std Dev 3.379
Gaus mean : 37.8198
Gaus Width: 4.2945
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch109, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 43.17
Std Dev 3.718
Gaus mean : 42.9979
Gaus Width: 4.0771
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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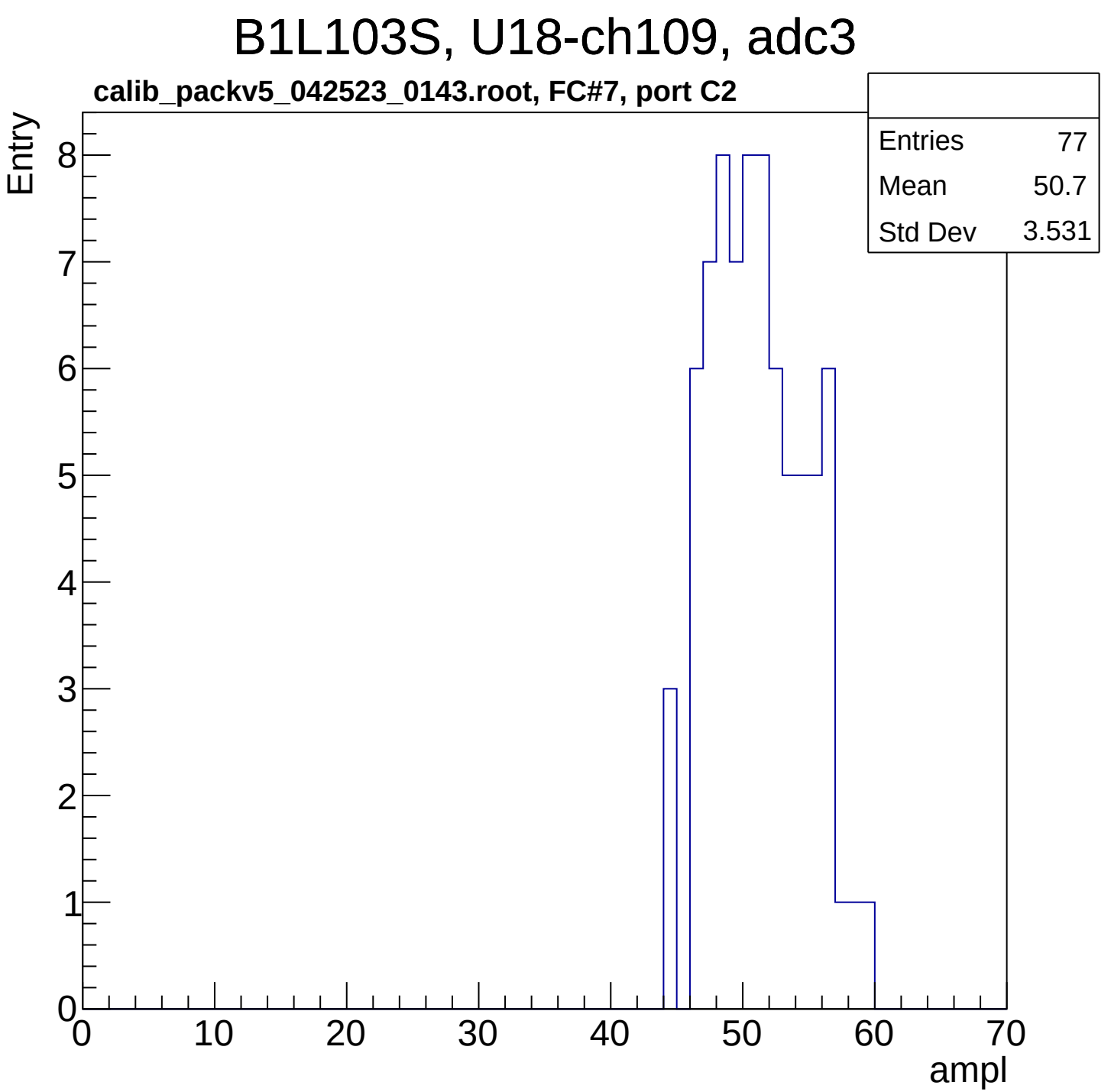
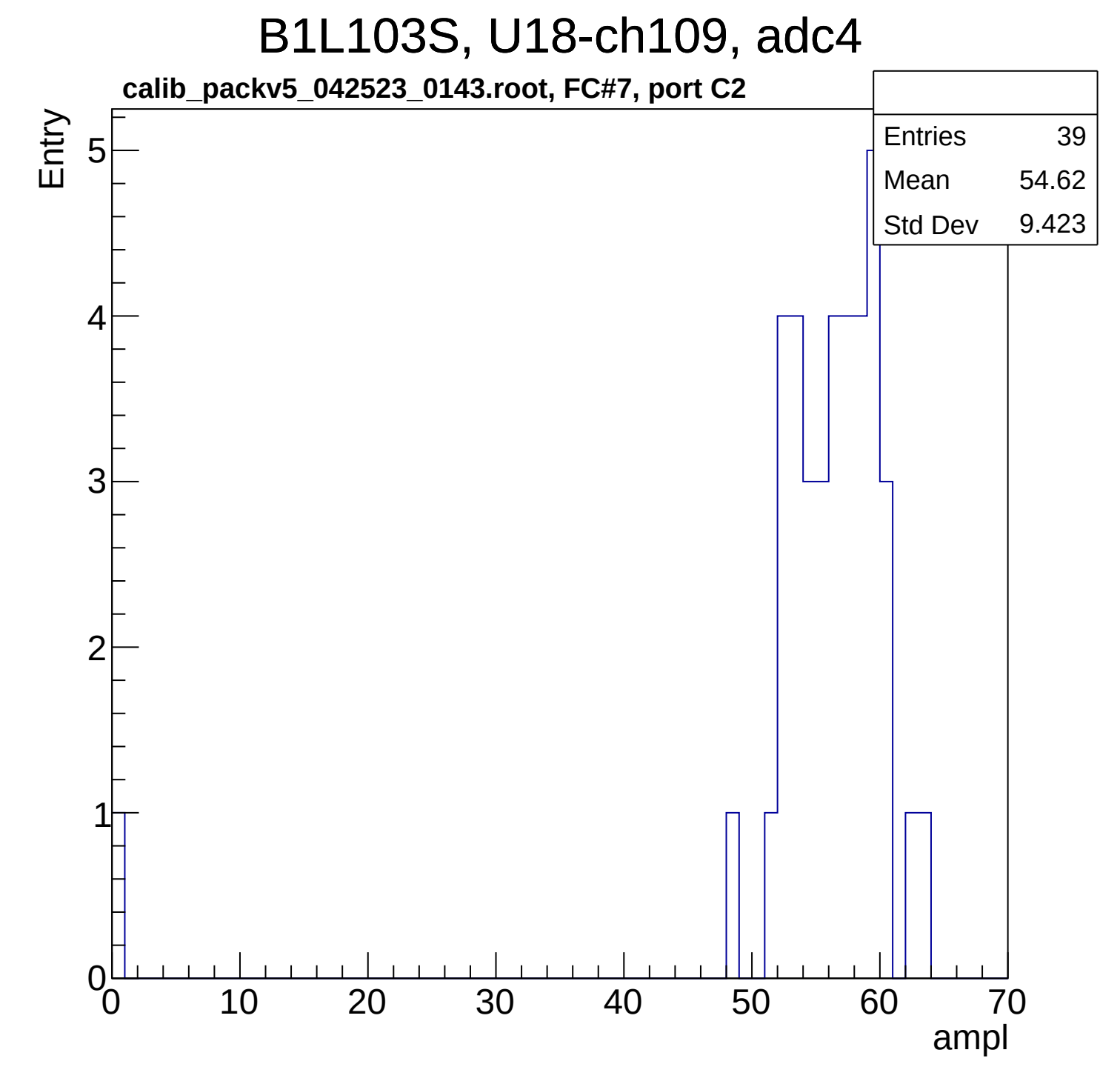
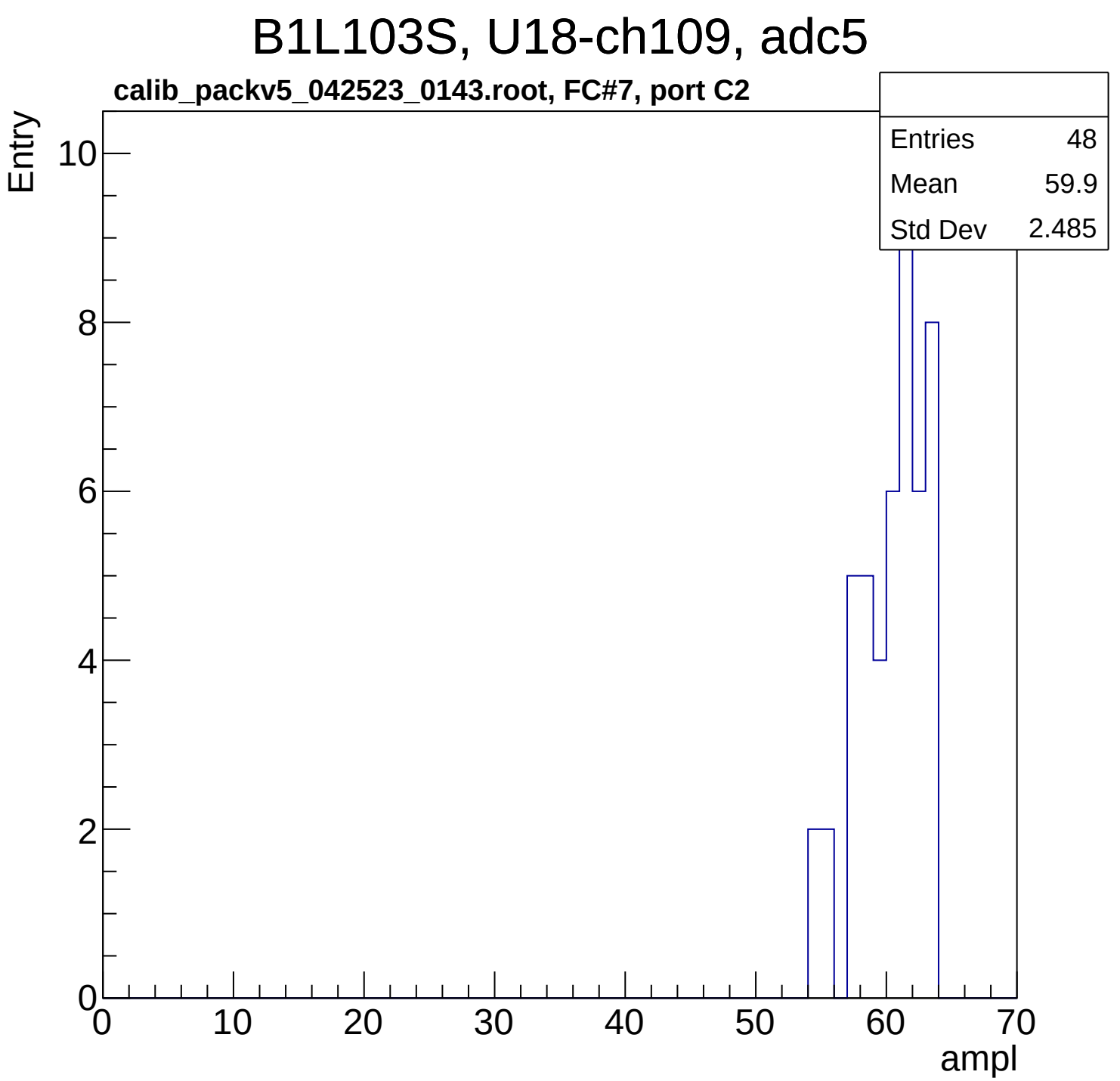

B1L103S, U18-ch109, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 77
Mean 50.7
Std Dev 3.531
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch109, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 39
Mean 54.62
Std Dev 9.423
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U18-ch109, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 48
Mean 59.9
Std Dev 2.485
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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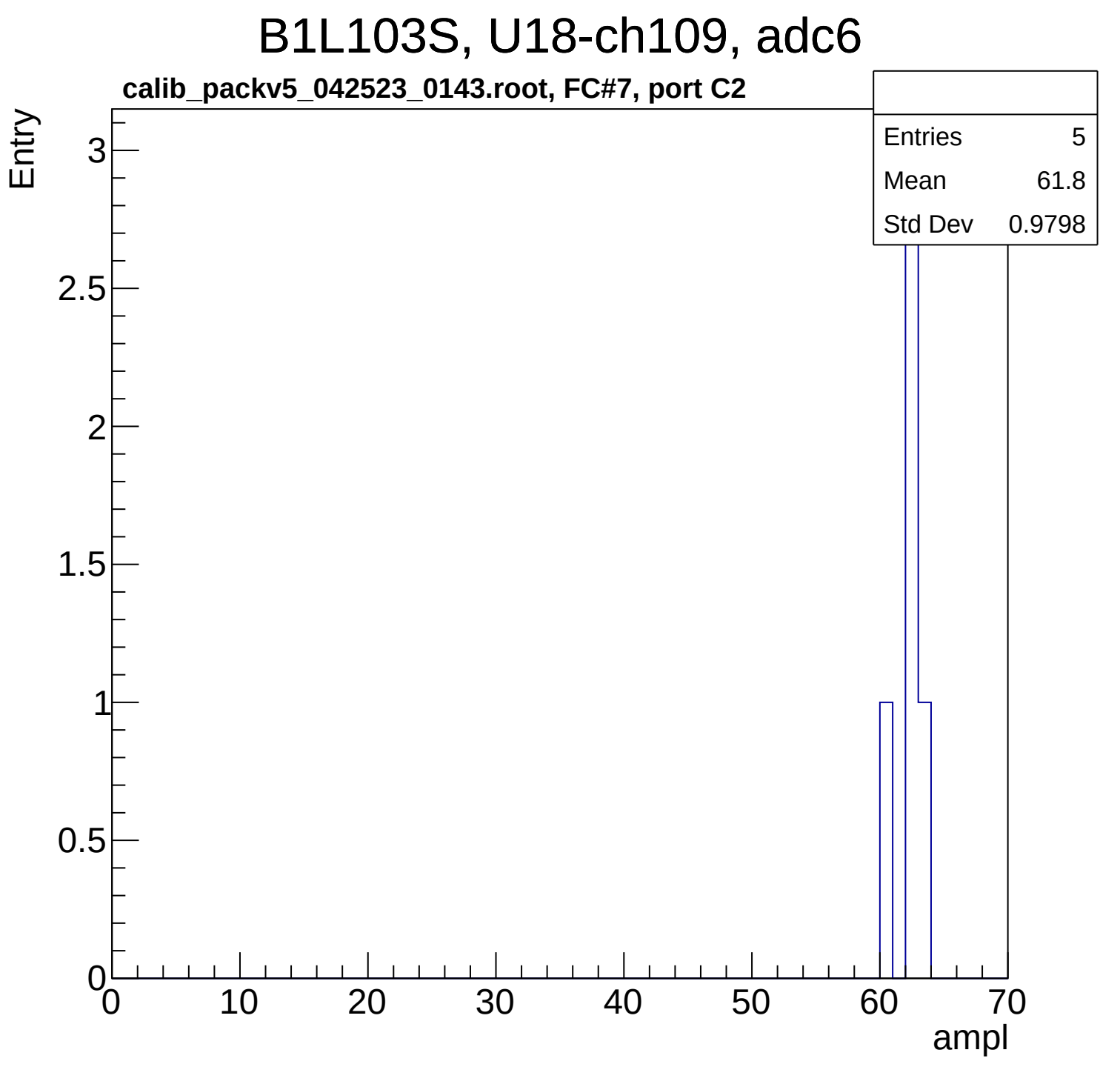
B1L103S, U18-ch109, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 5
Mean 61.8
Std Dev 0.9798
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
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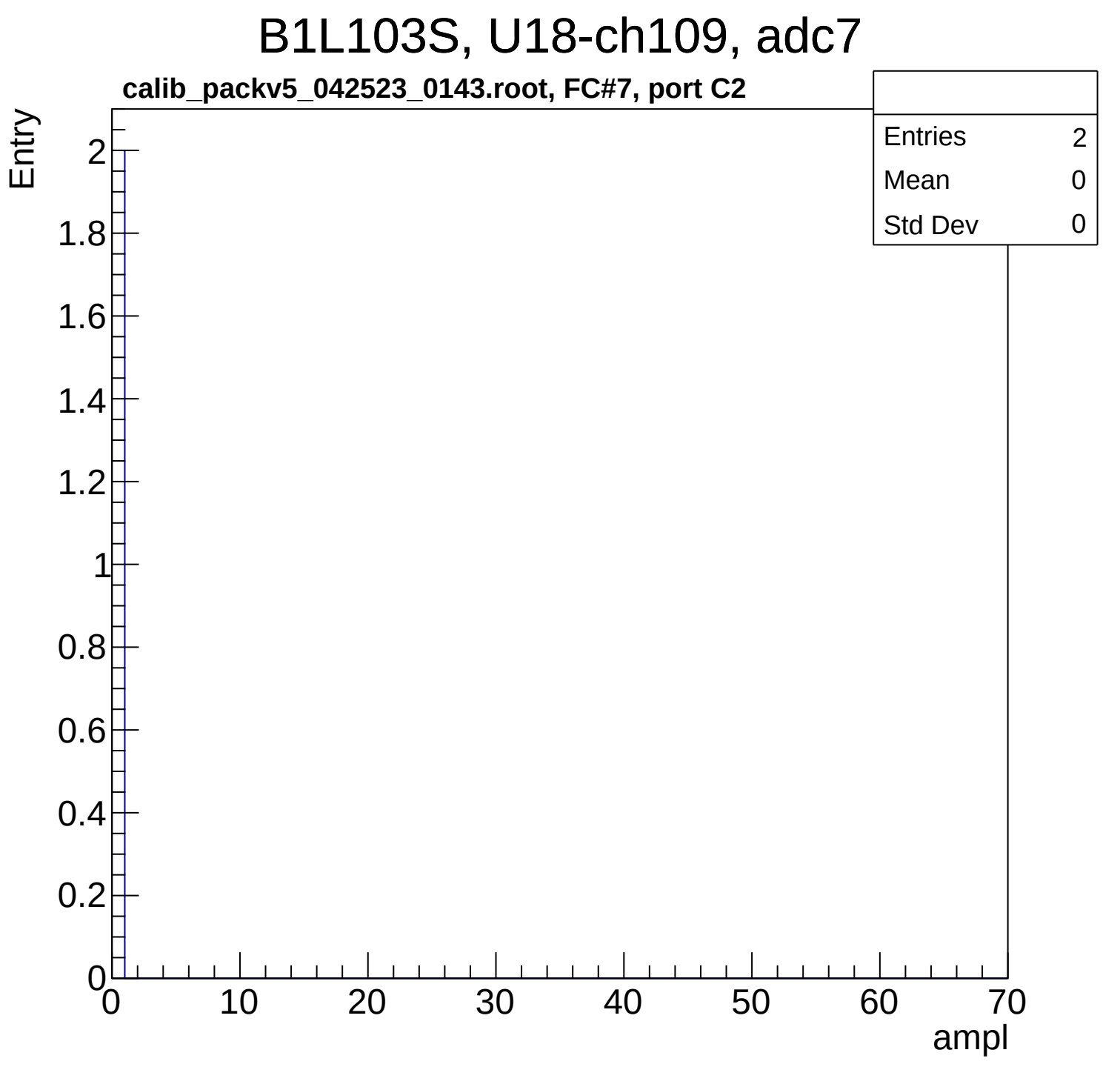
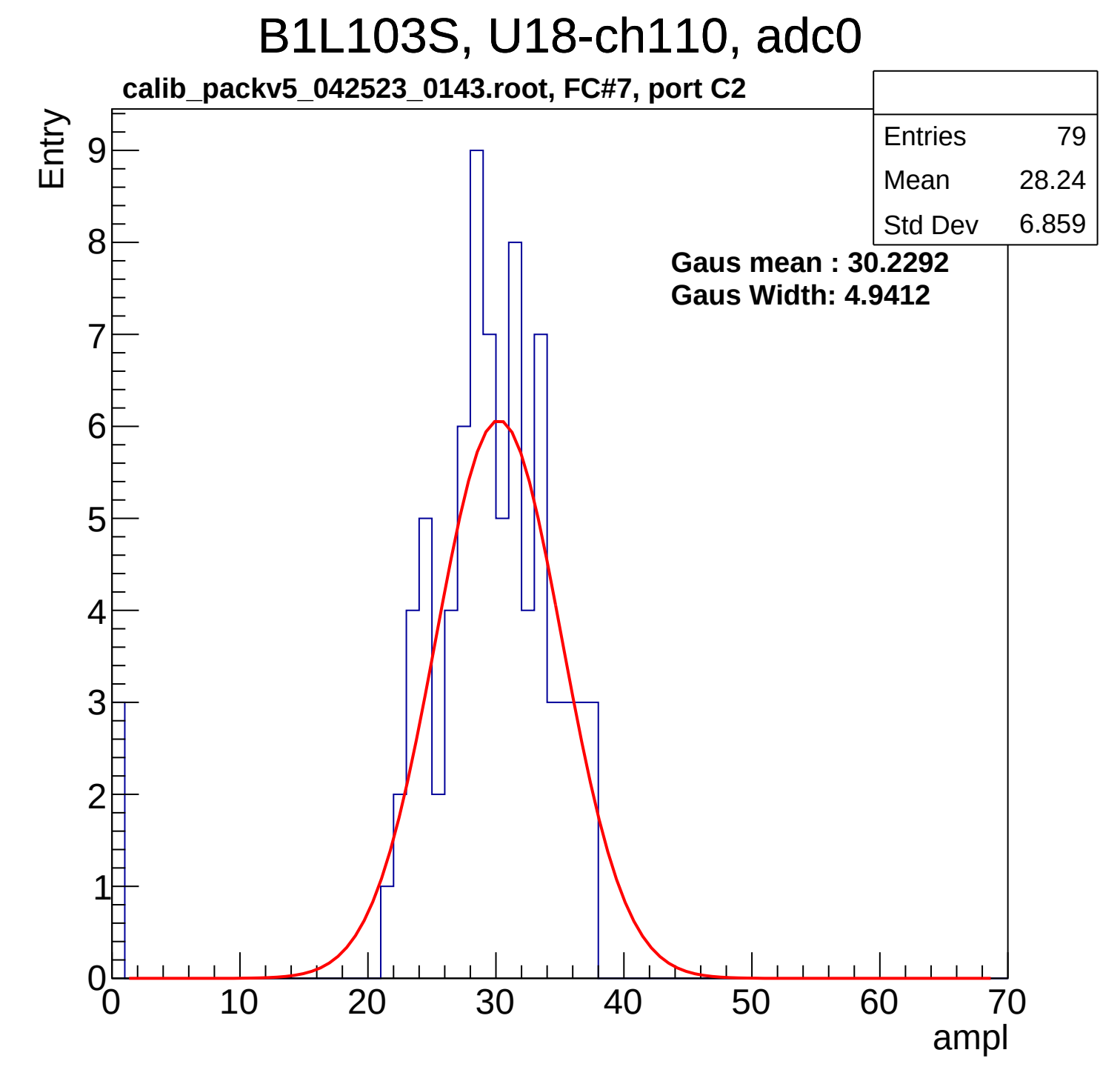

B1L103S, U18-ch109, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch110, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 79
Mean 28.24
Std Dev 6.859
Gaus mean : 30.2292
Gaus Width: 4.9412
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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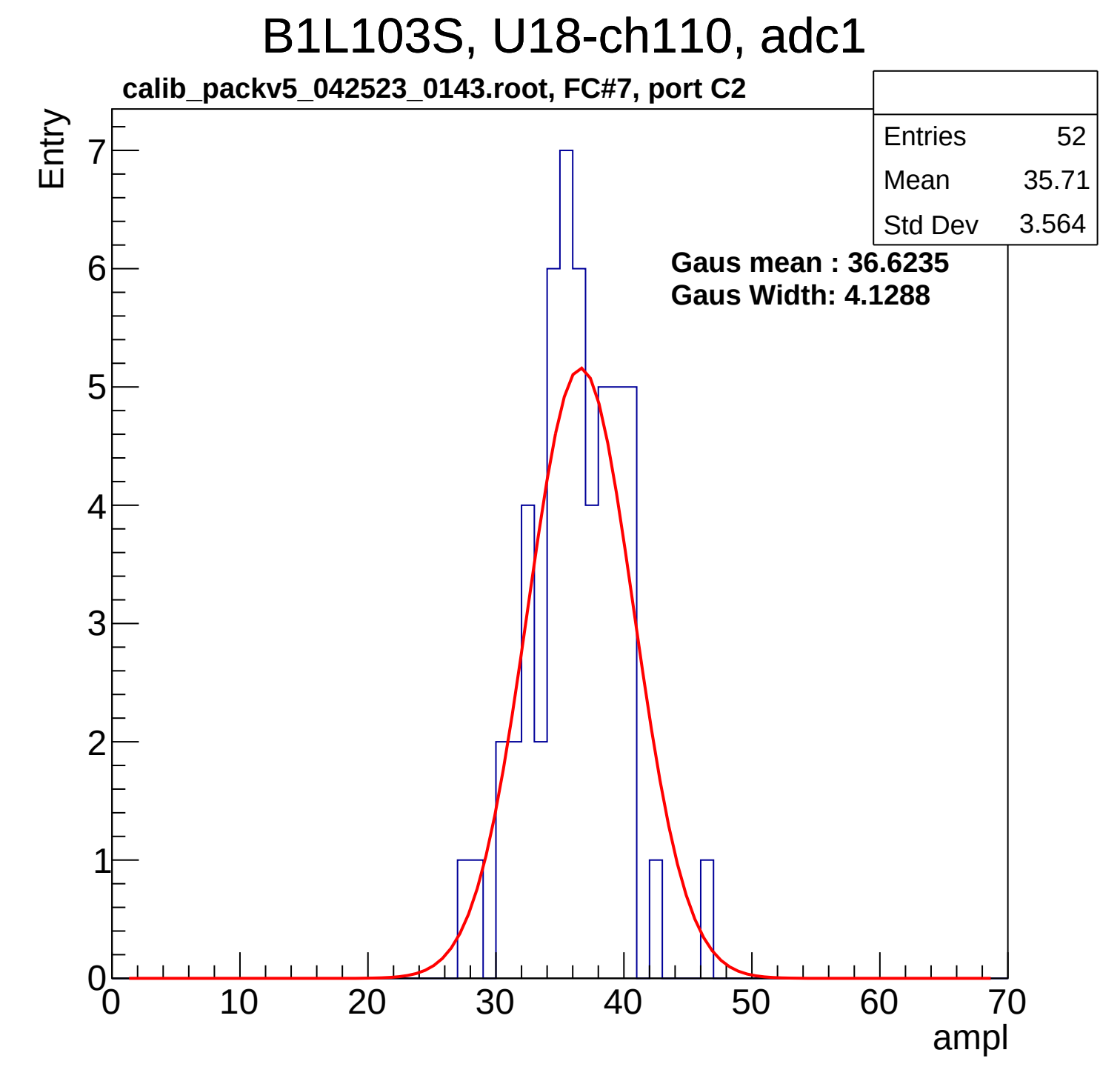
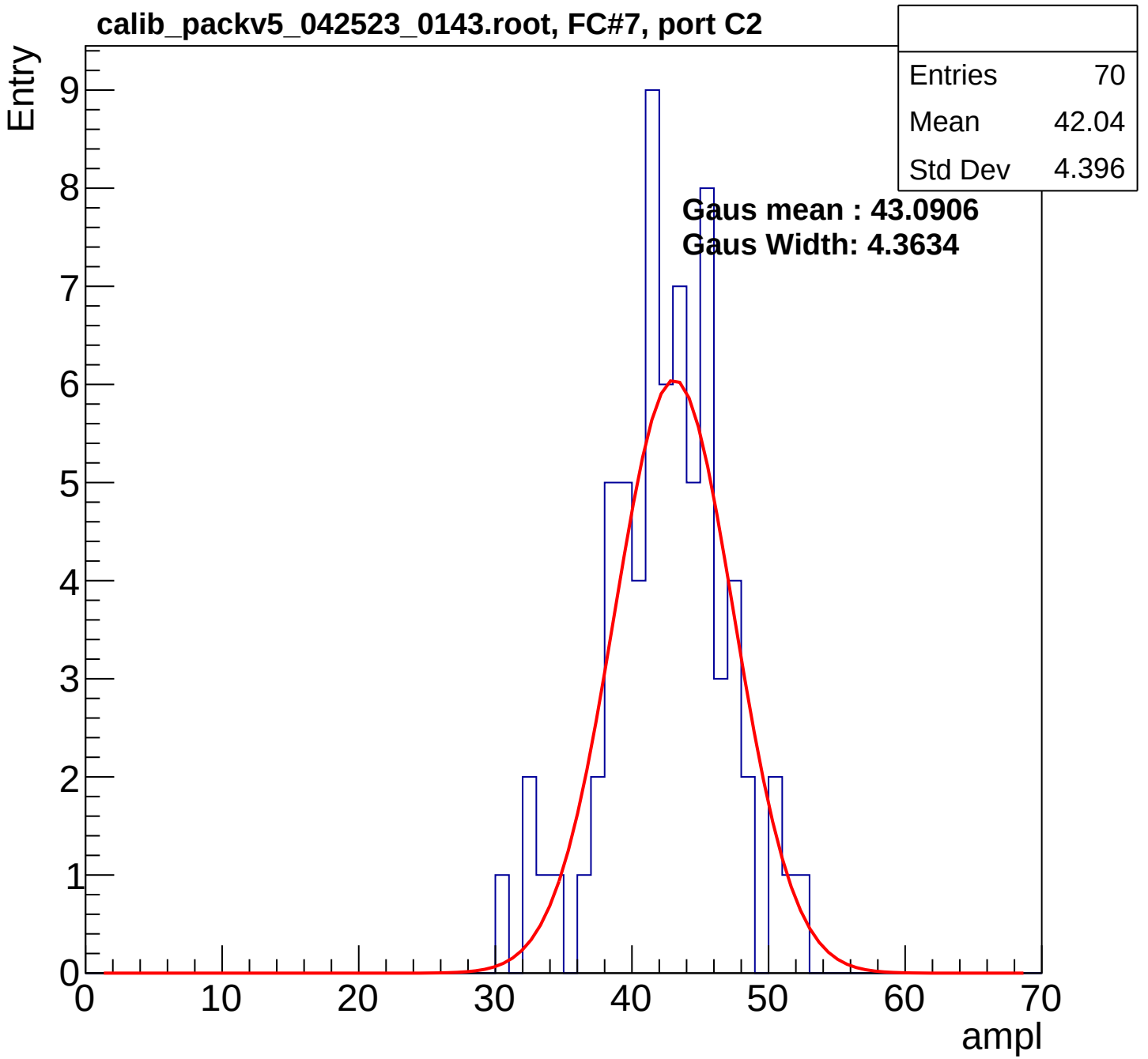

B1L103S, U18-ch110, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 52
Mean 35.71
Std Dev 3.564
Gaus mean : 36.6235
Gaus Width: 4.1288
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch110, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 42.04
Std Dev 4.396
Gaus mean : 43.0906
Gaus Width: 4.3634
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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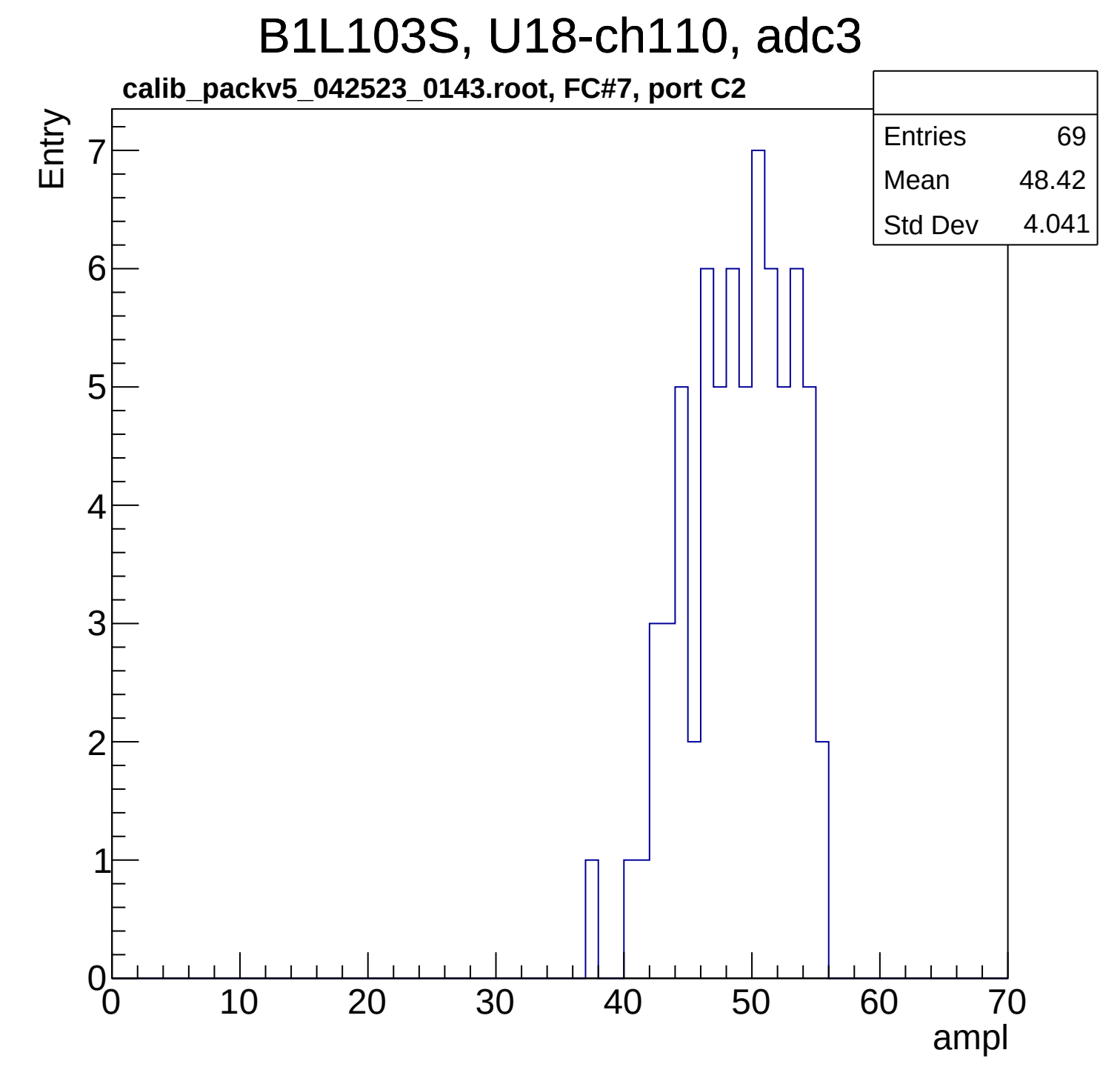
B1L103S, U18-ch110, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 48.42
Std Dev 4.041
Entry
ampl
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4
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0
10
20
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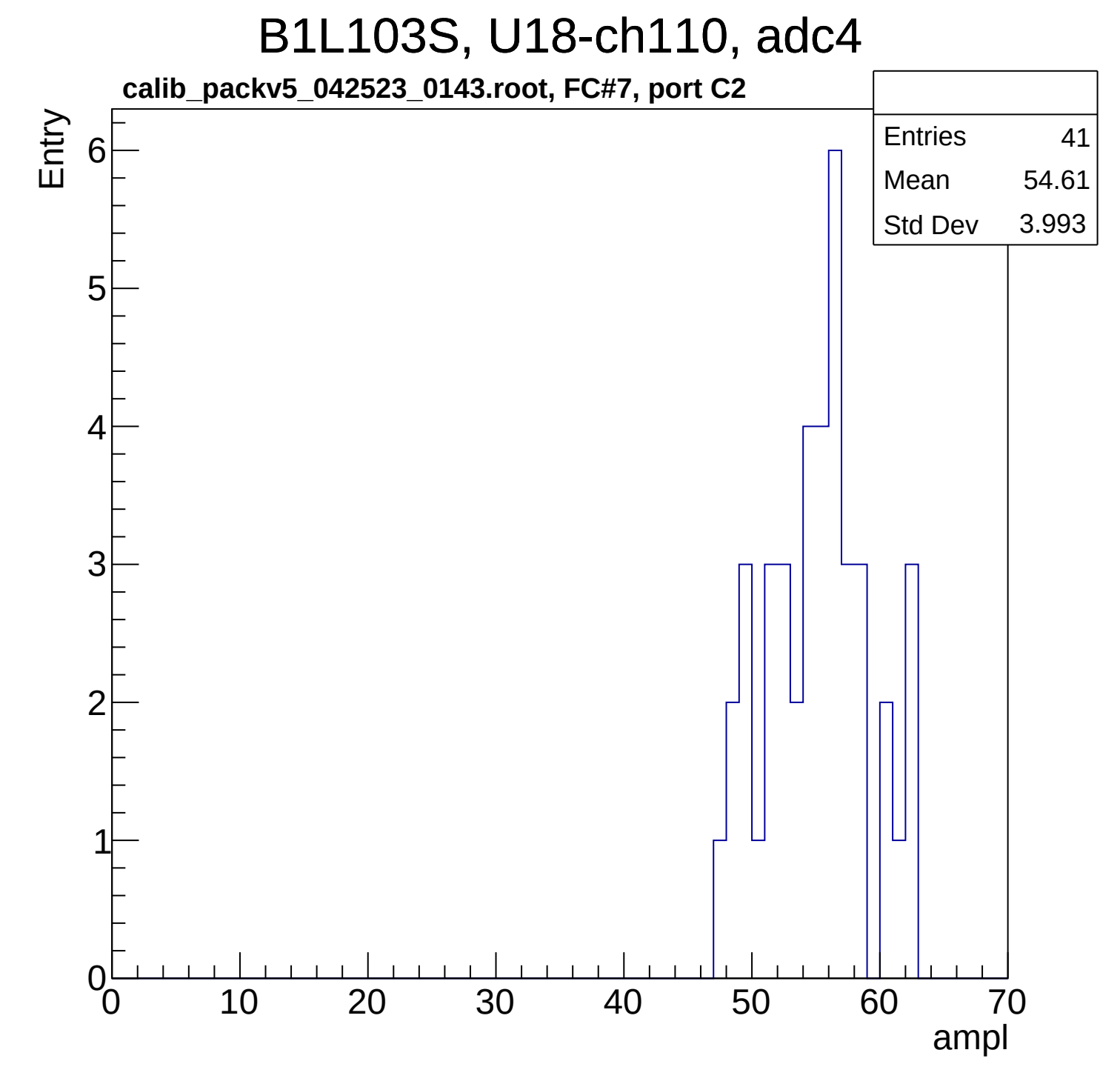
40
50
60
70


B1L103S, U18-ch110, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 41
Mean 54.61
Std Dev 3.993
Entry
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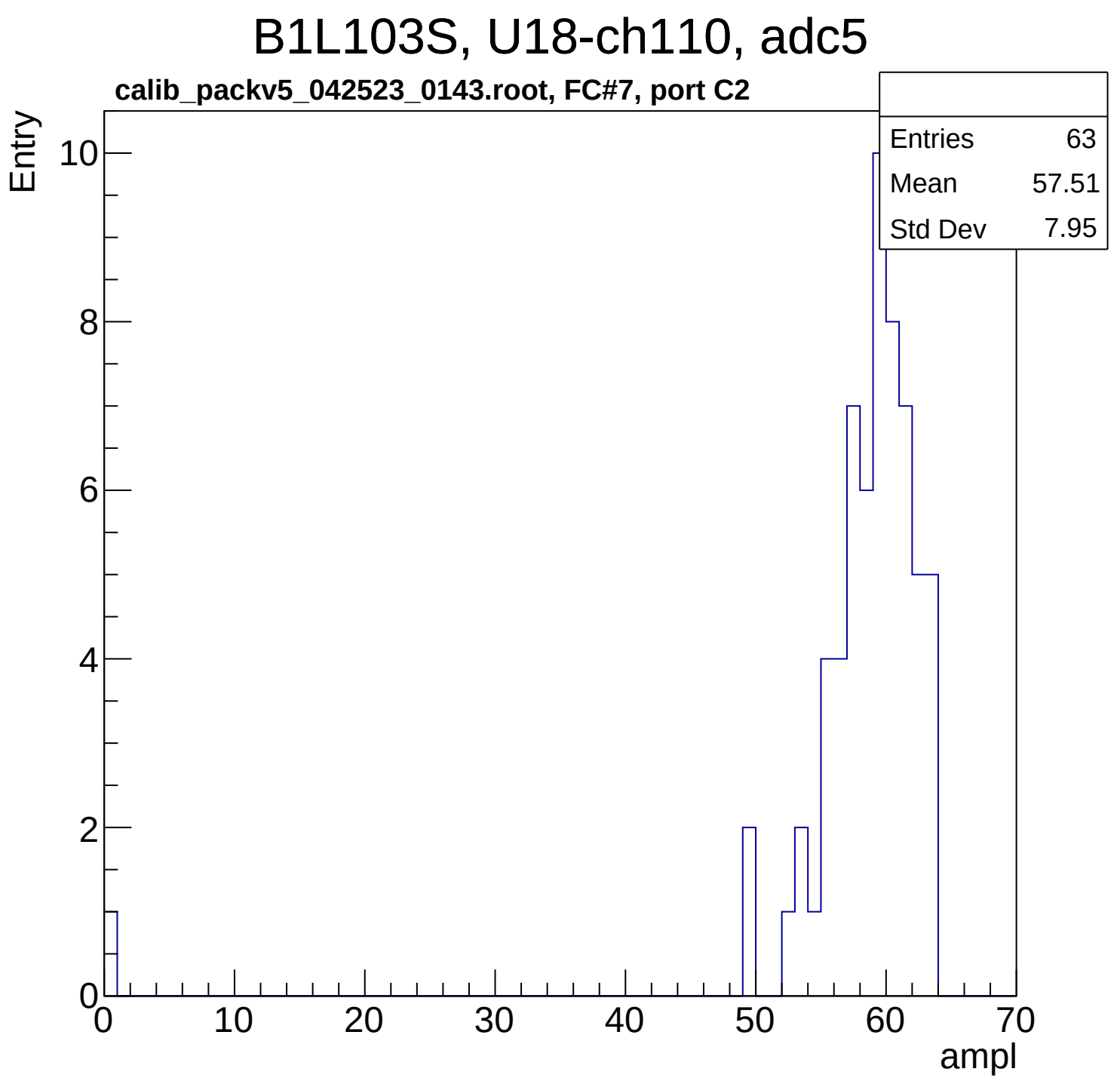
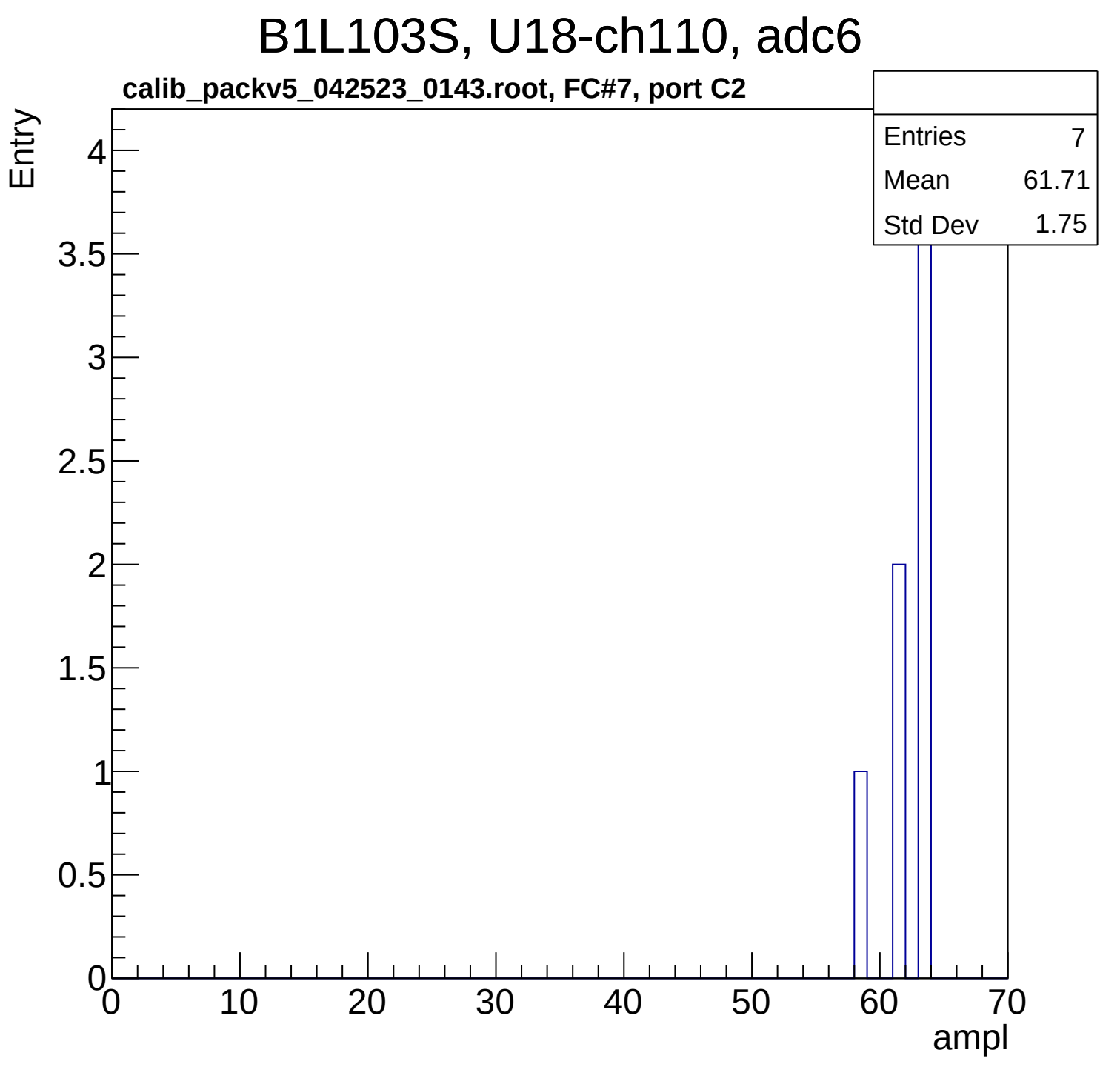
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch110, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 57.51
Std Dev 7.95
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch110, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 7
Mean 61.71
Std Dev 1.75
Entry
ampl
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0.5
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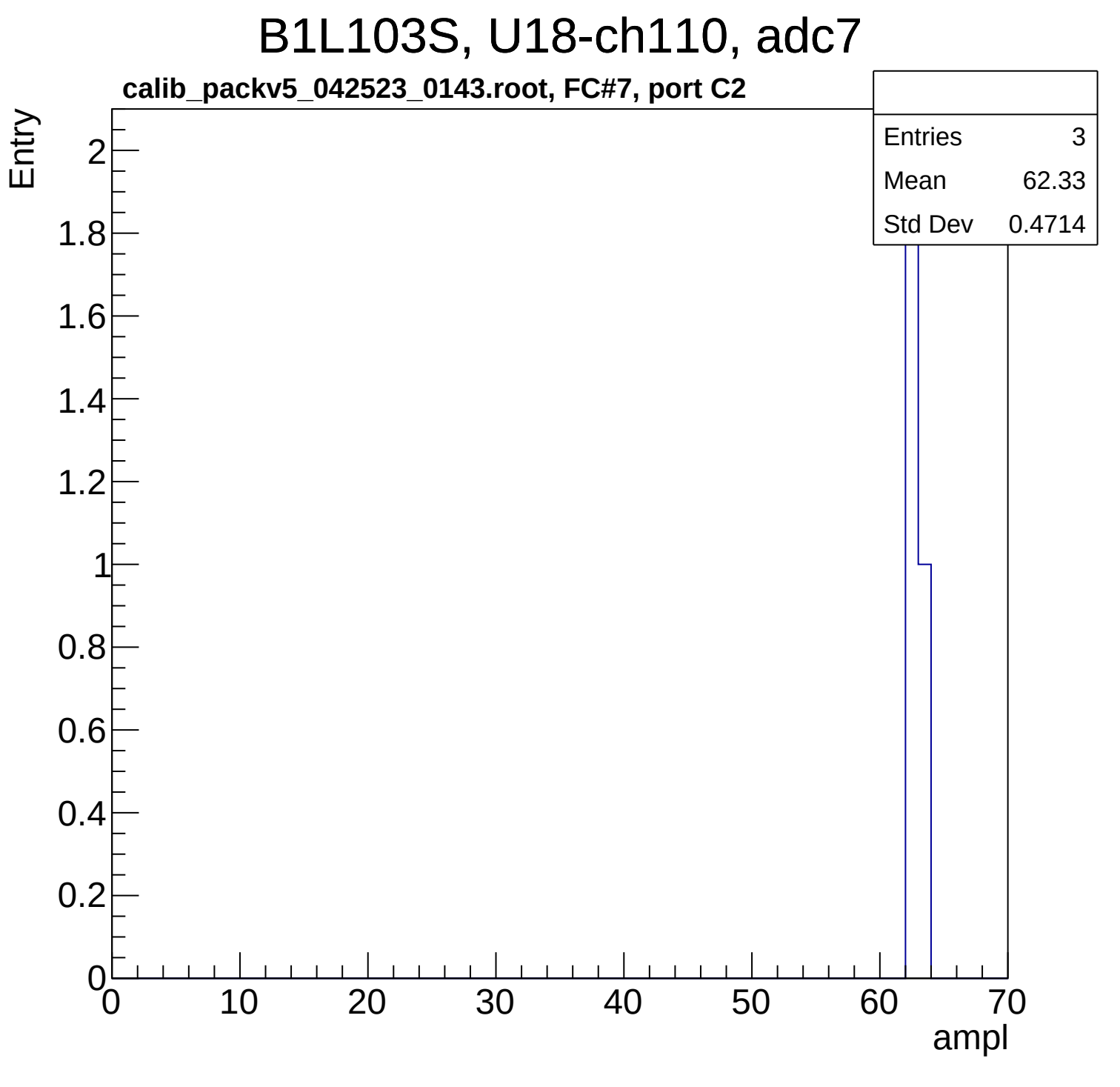
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U18-ch110, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 62.33
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
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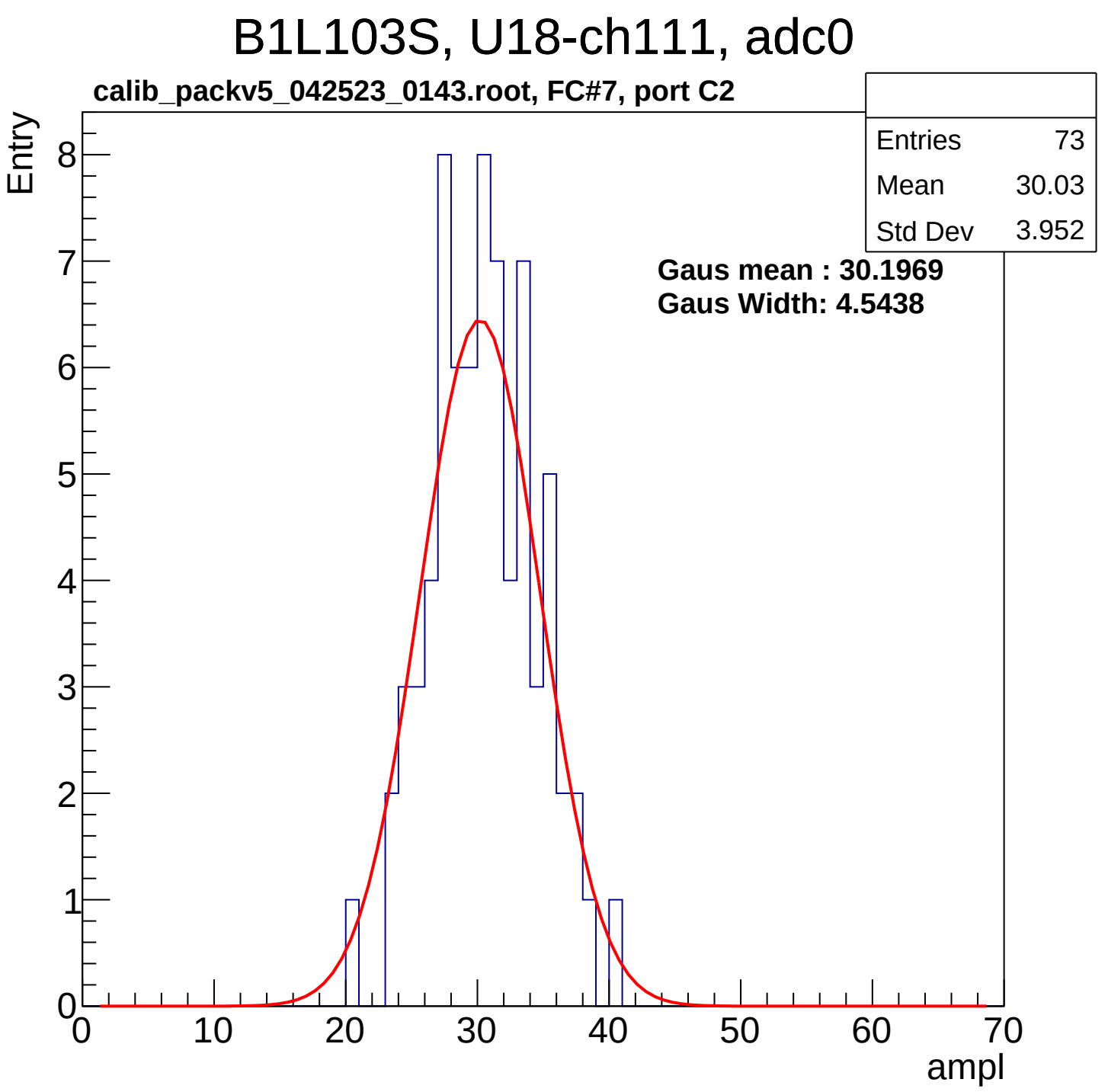
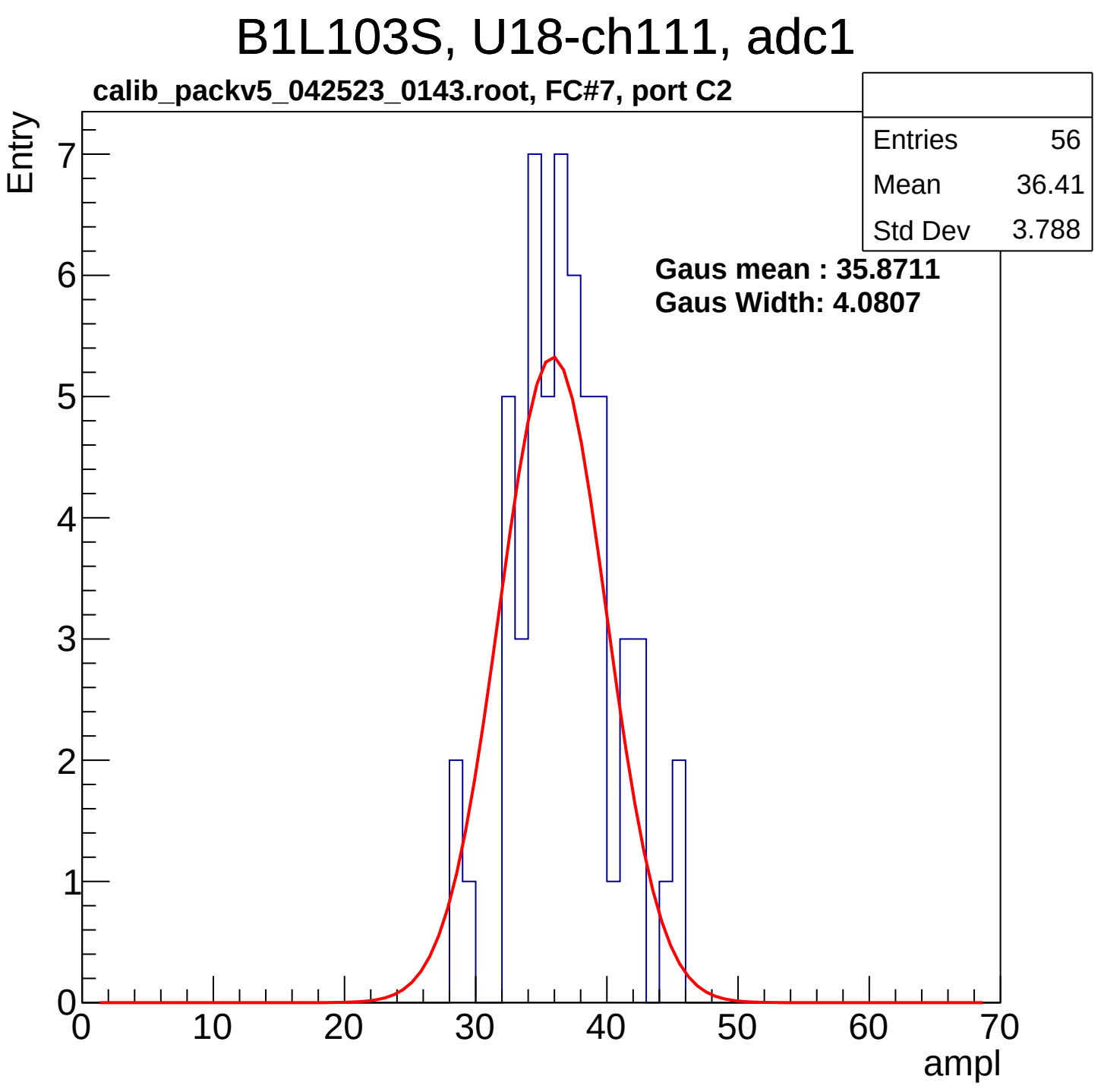
40
50
60
70


B1L103S, U18-ch111, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 73
Mean 30.03
Std Dev 3.952
Gaus mean : 30.1969
Gaus Width: 4.5438
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch111, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 36.41
Std Dev 3.788
Gaus mean : 35.8711
Gaus Width: 4.0807
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
50
60
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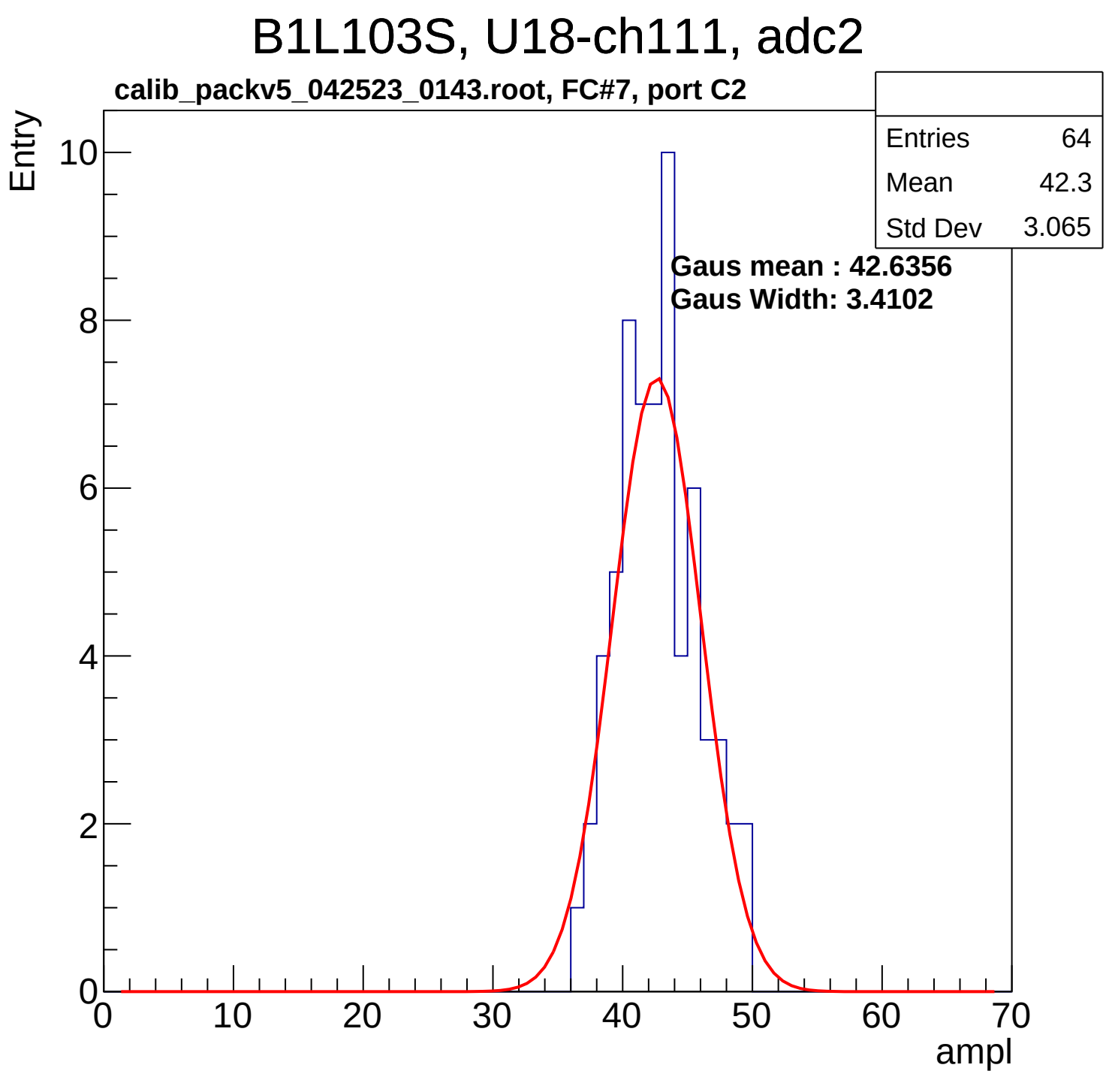
B1L103S, U18-ch111, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 42.3
Std Dev 3.065
Gaus mean : 42.6356
Gaus Width: 3.4102
Entry
ampl
0
2
4
6
8
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0
10
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40
50
60
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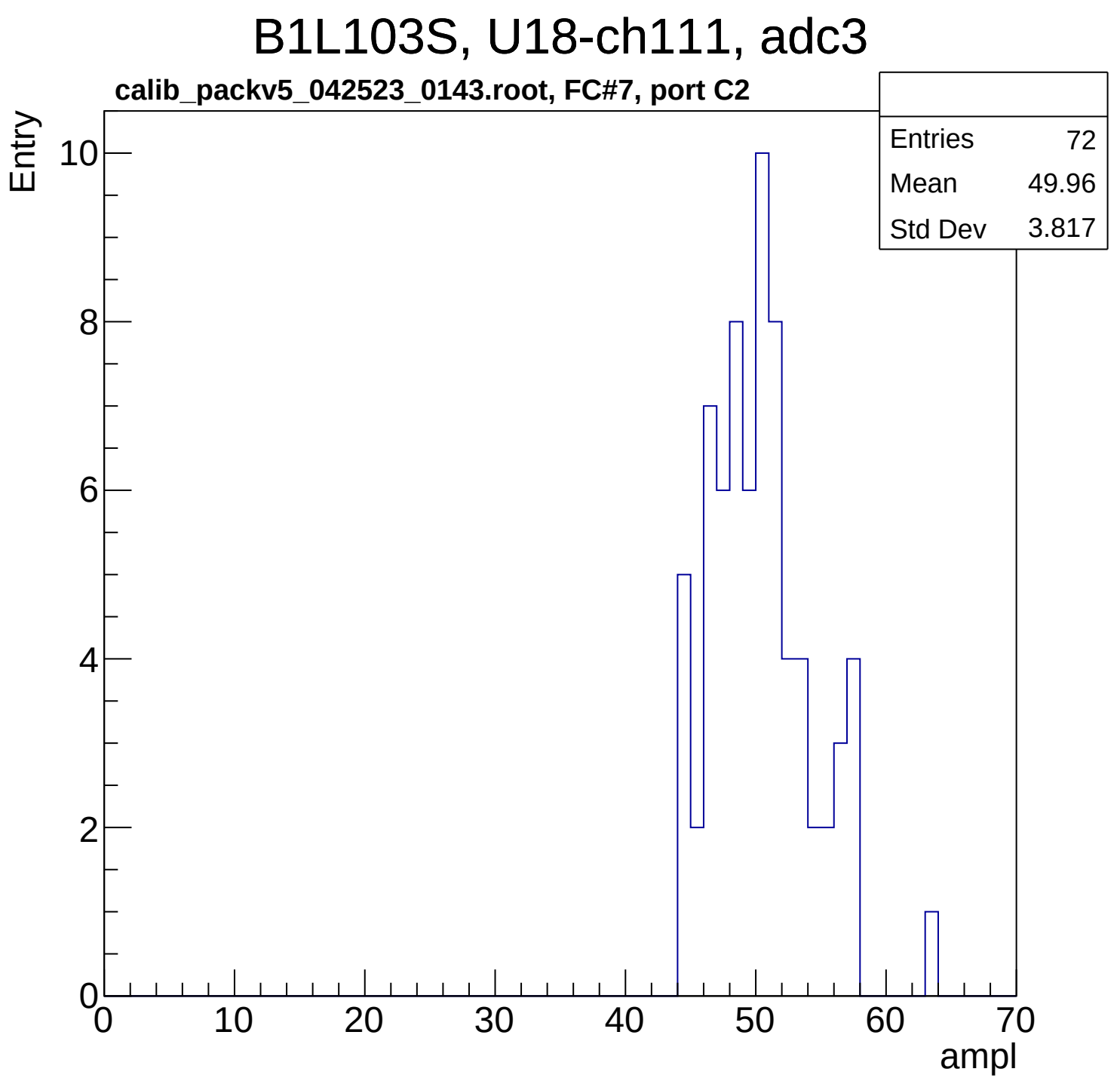
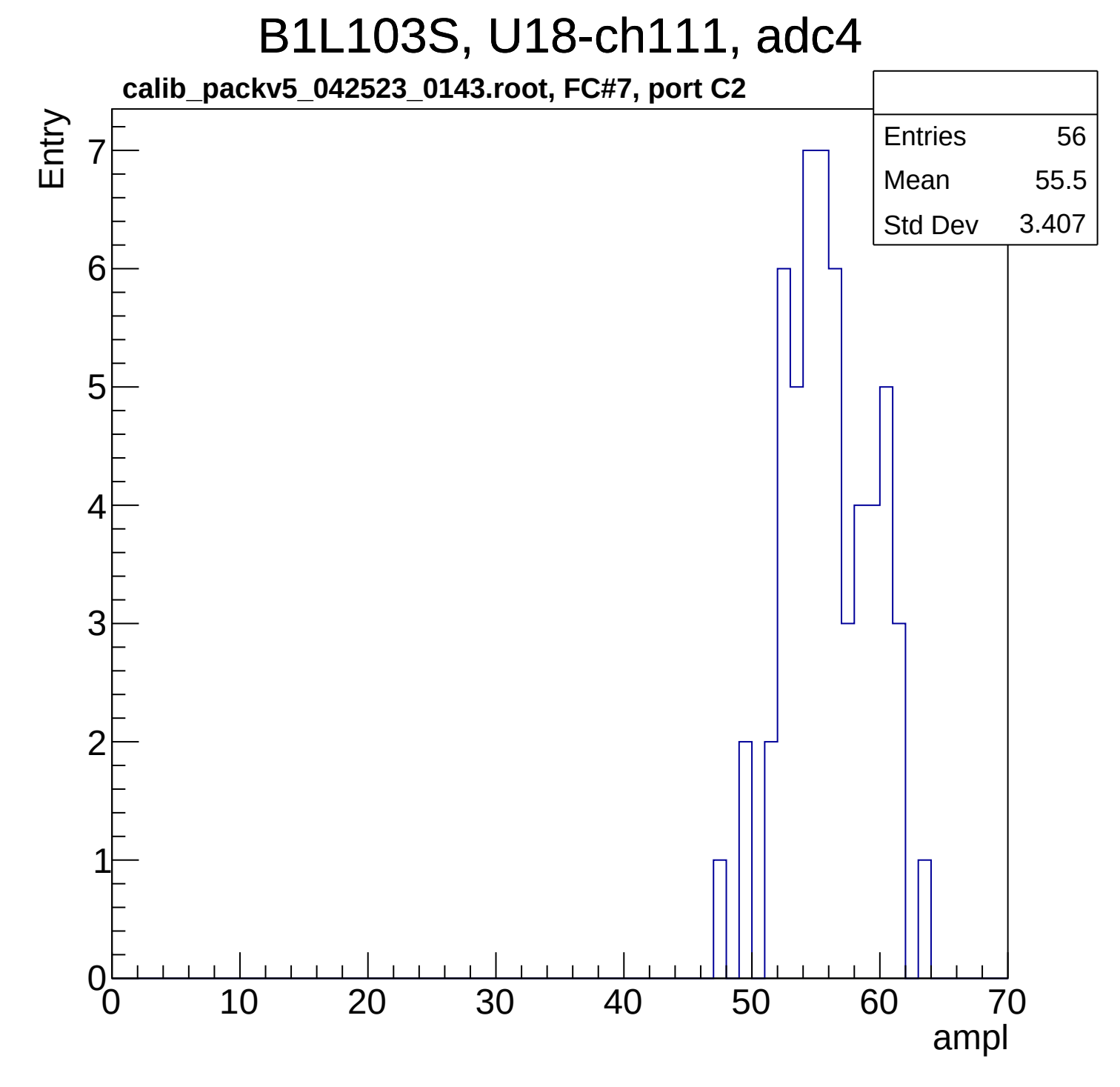
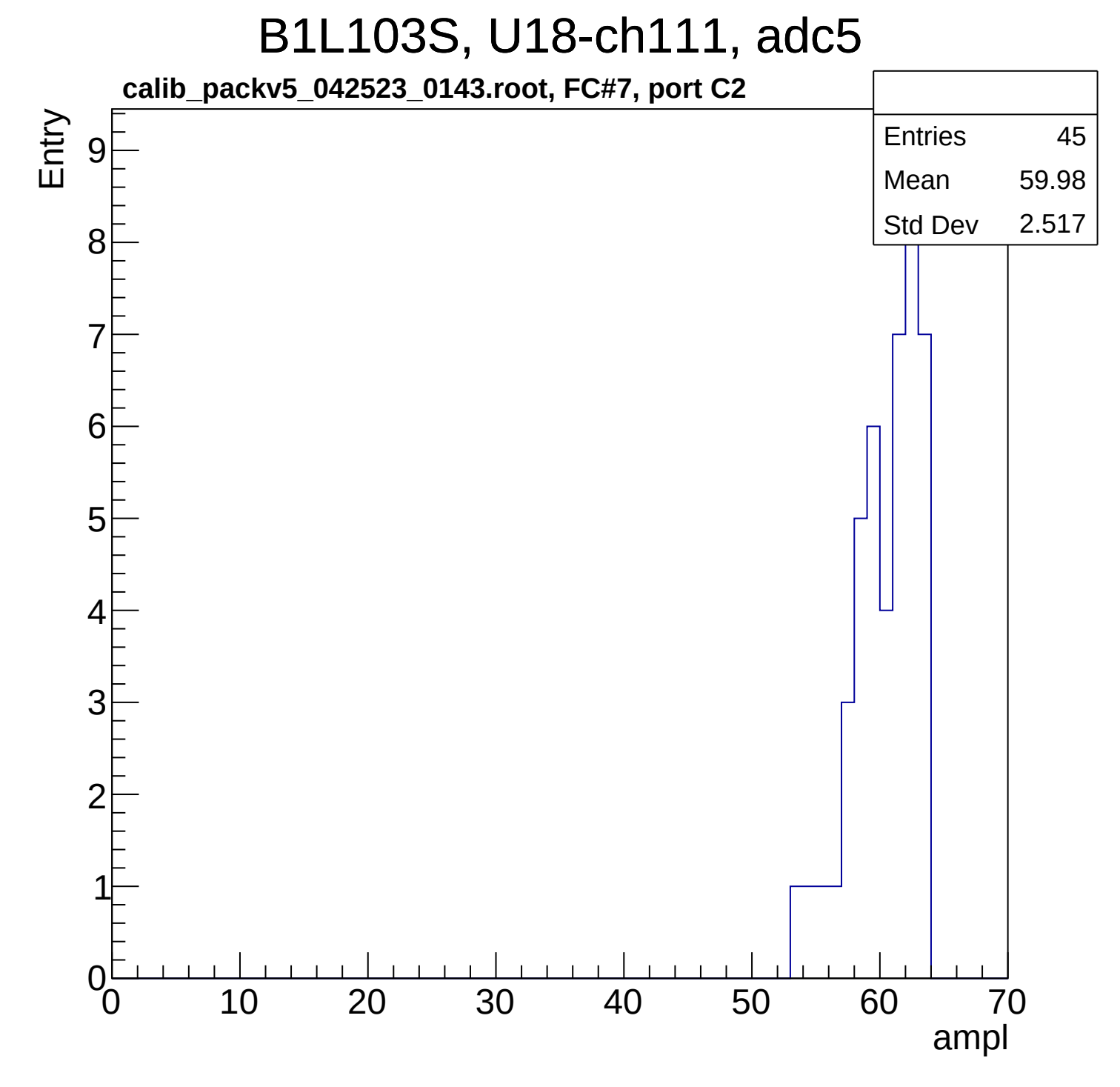

B1L103S, U18-ch111, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 72
Mean 49.96
Std Dev 3.817
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch111, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 55.5
Std Dev 3.407
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch111, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 45
Mean 59.98
Std Dev 2.517
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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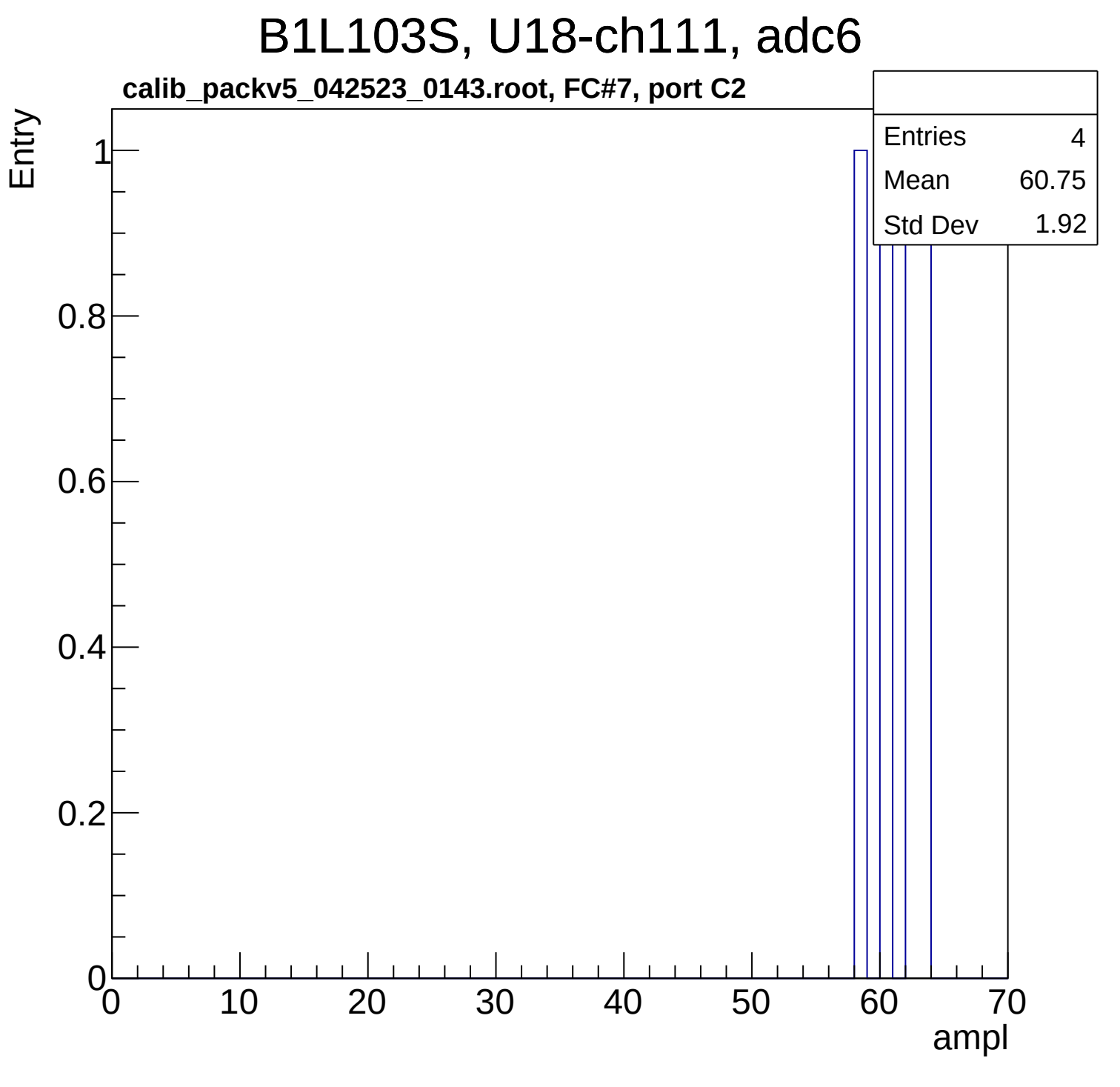
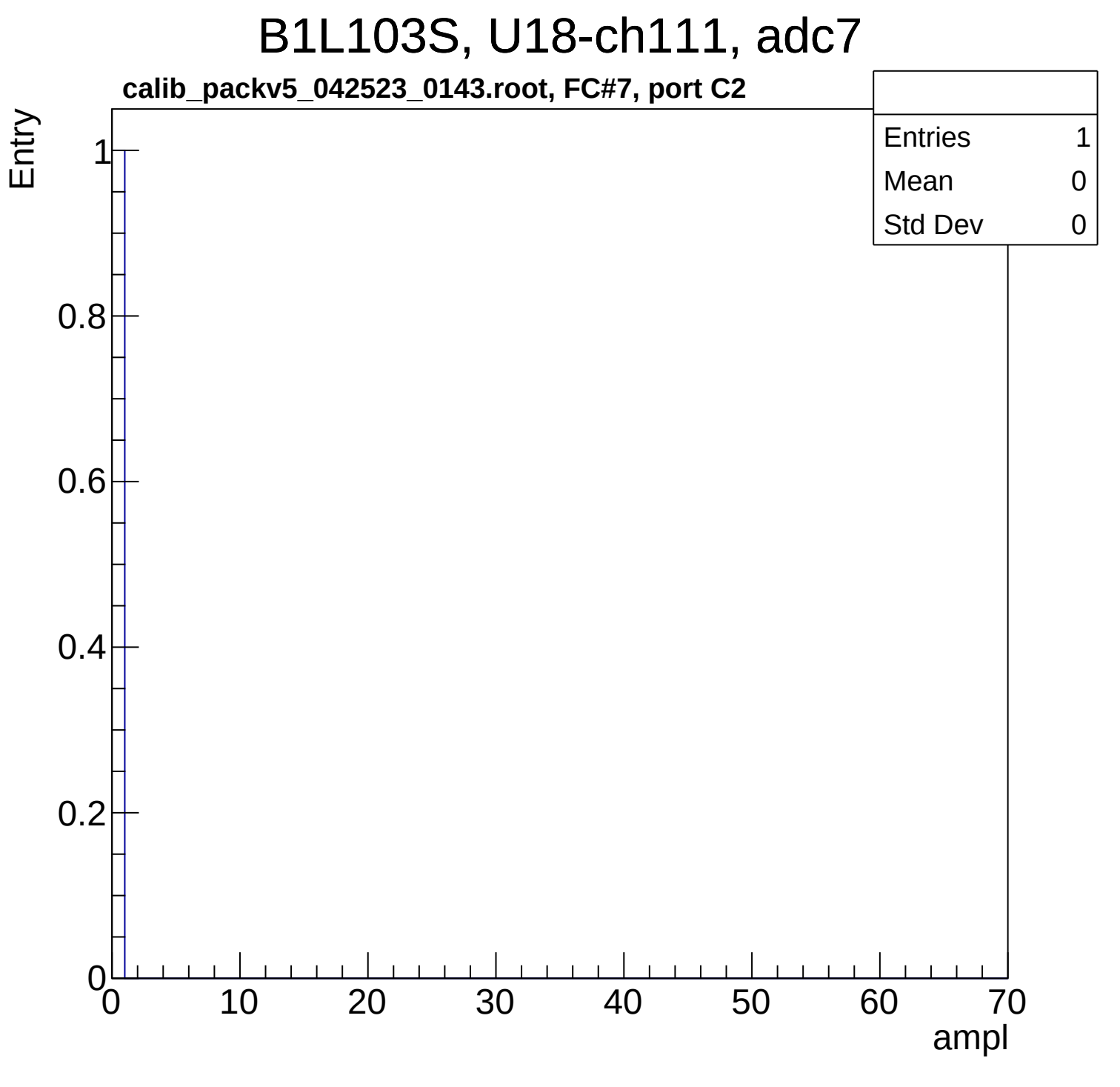
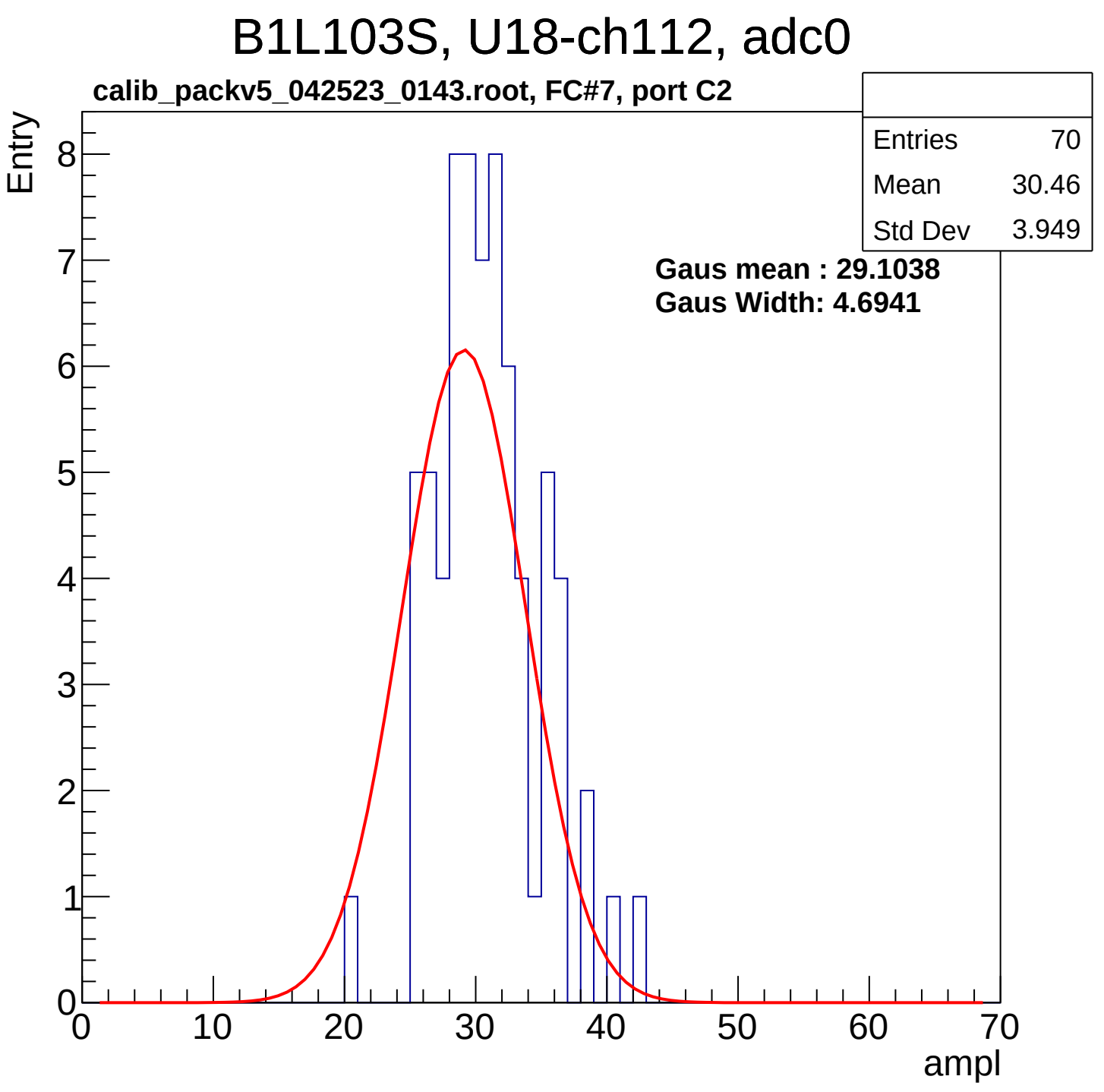
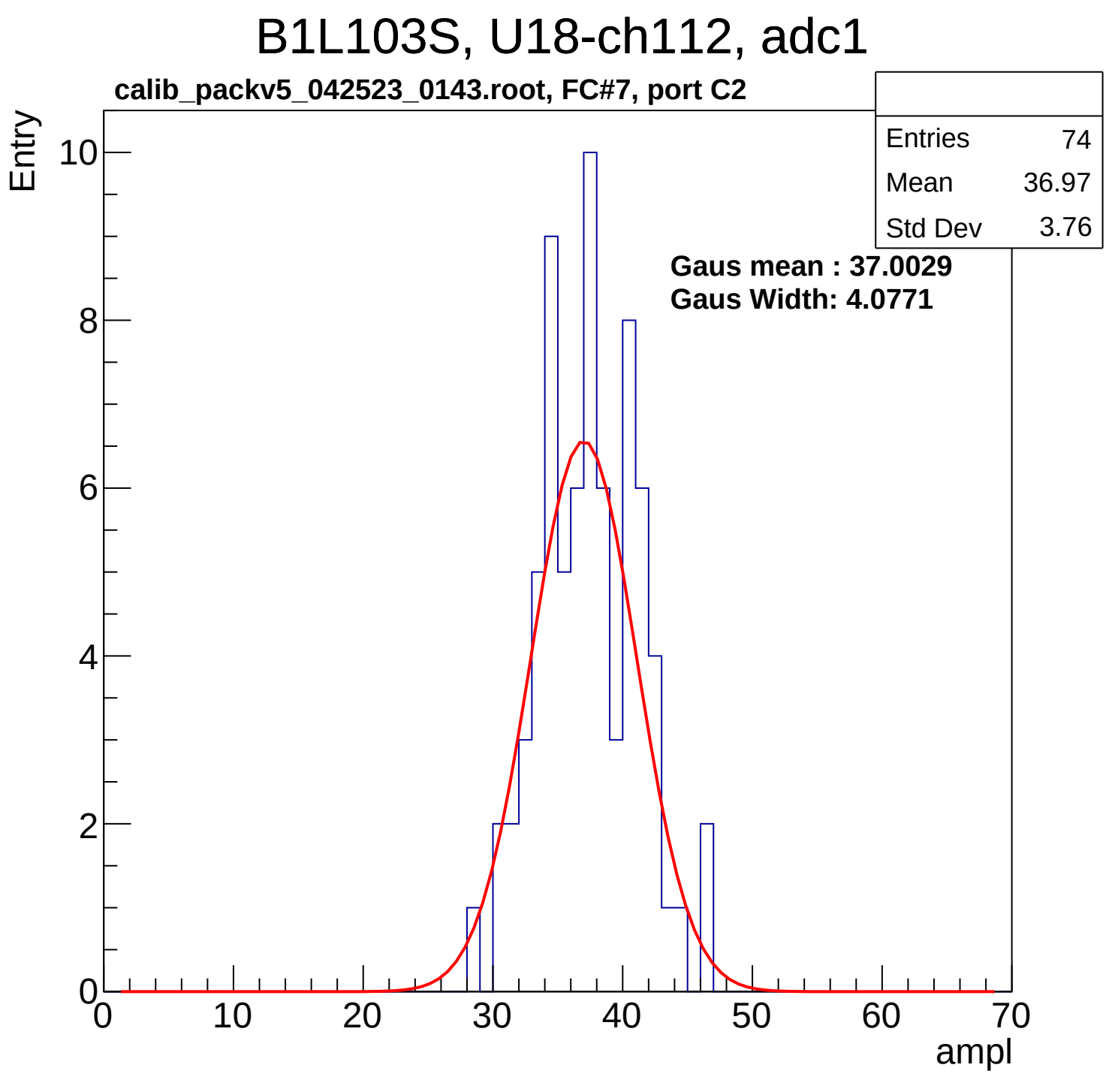
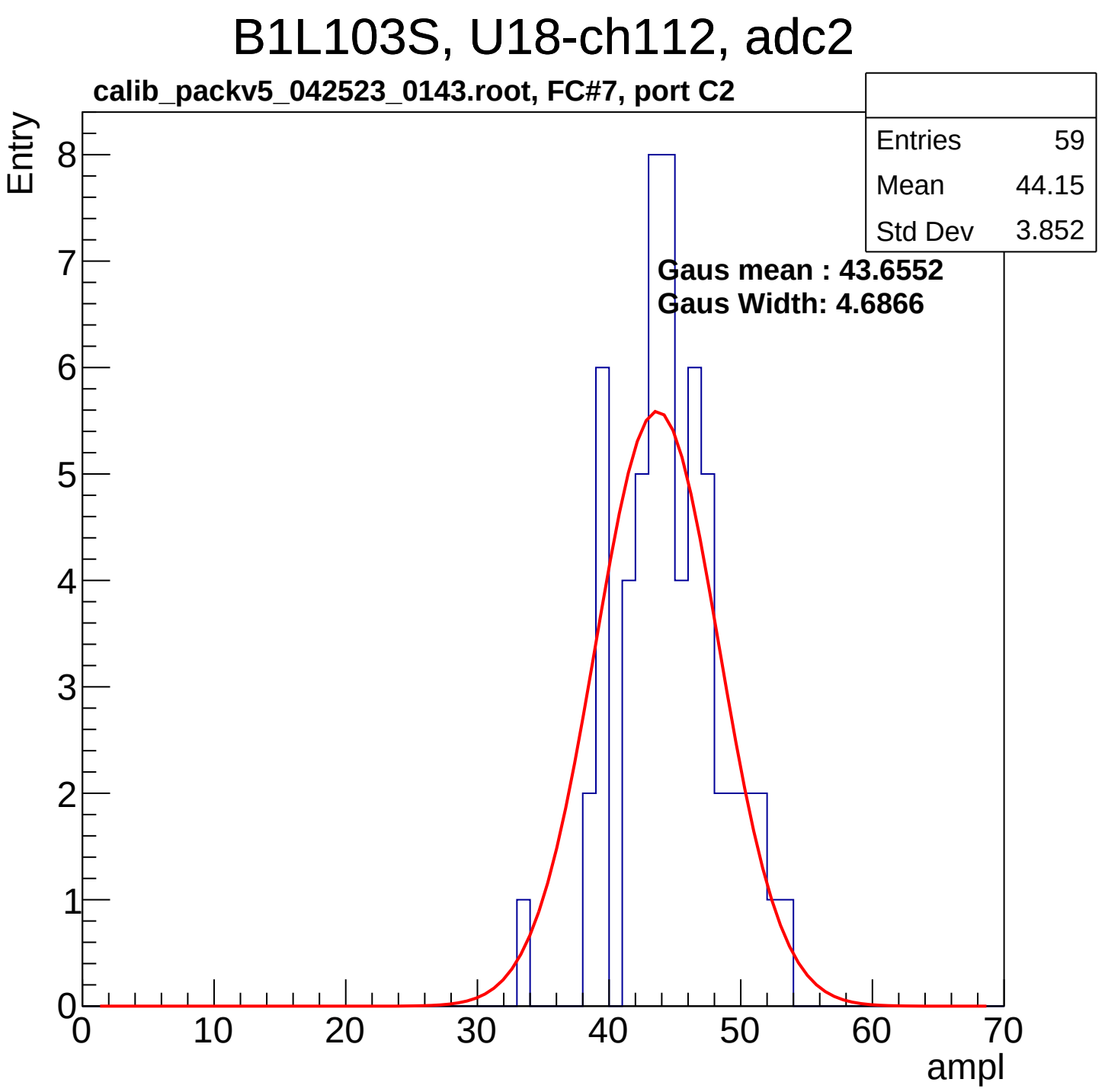
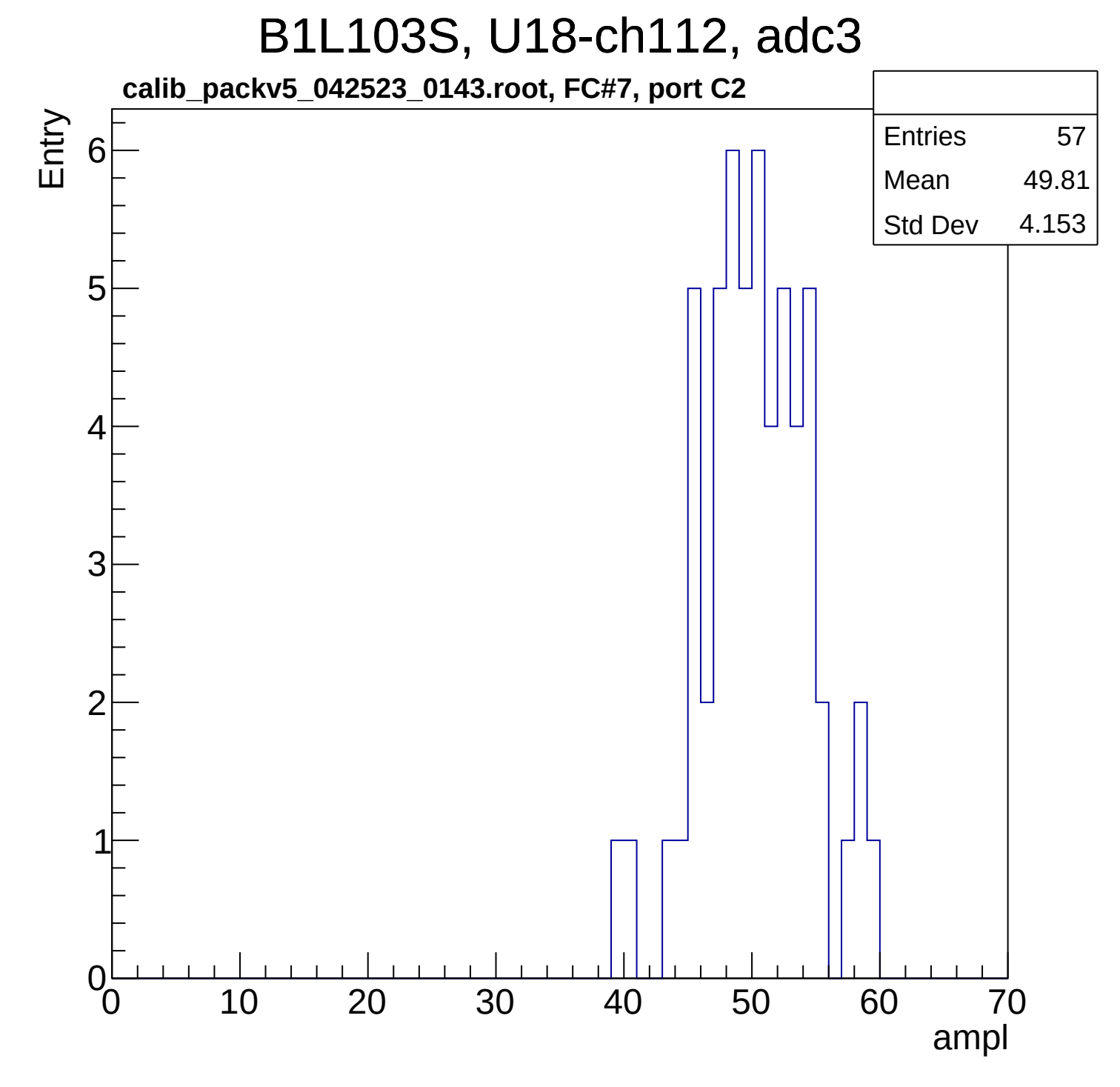

B1L103S, U18-ch111, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 4
Mean 60.75
Std Dev 1.92
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

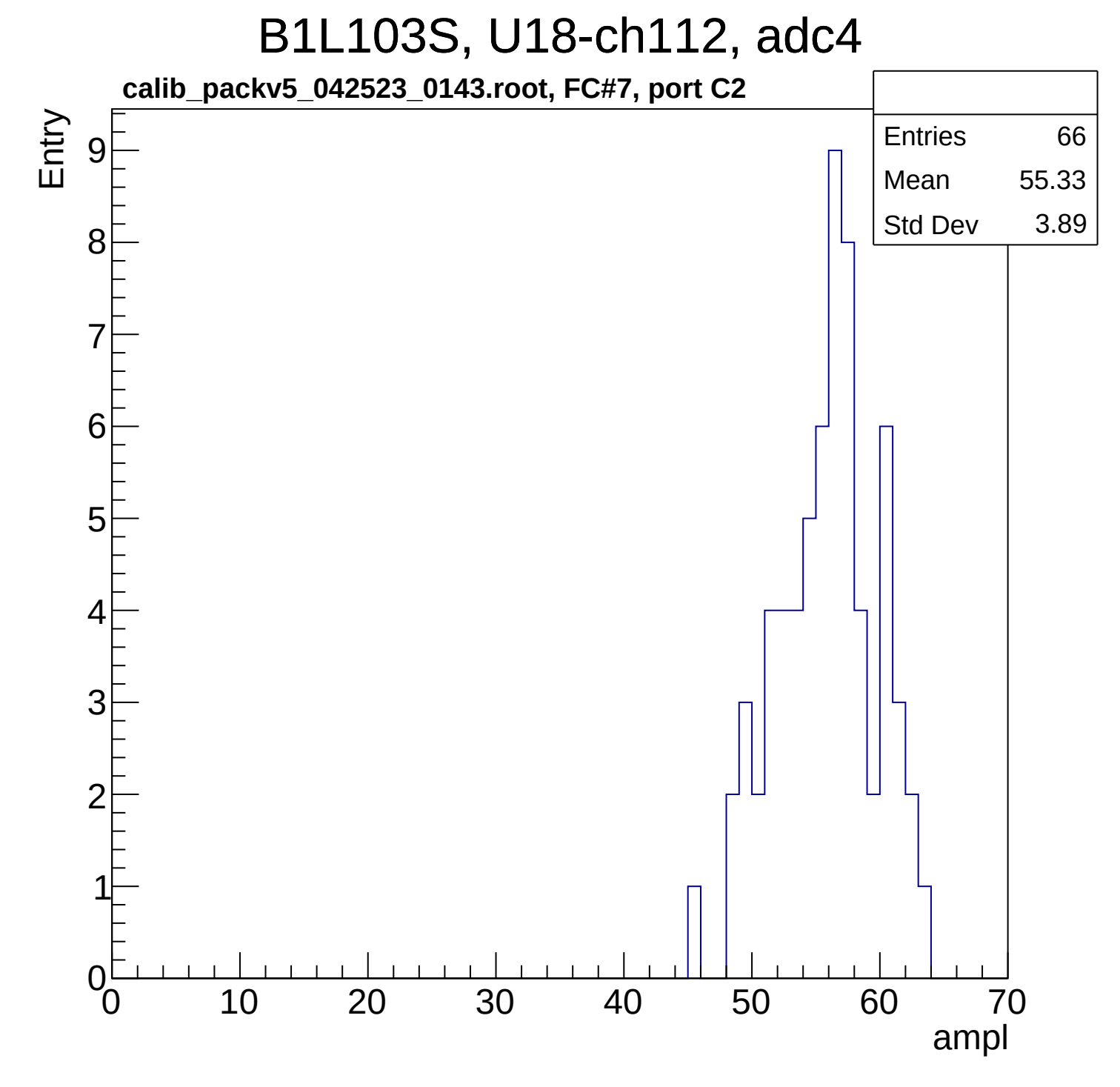

B1L103S, U18-ch111, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch112, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 30.46
Std Dev 3.949
Gaus mean : 29.1038
Gaus Width: 4.6941
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch112, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 74
Mean 36.97
Std Dev 3.76
Gaus mean : 37.0029
Gaus Width: 4.0771
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch112, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 44.15
Std Dev 3.852
Gaus mean : 43.6552
Gaus Width: 4.6866
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch112, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 49.81
Std Dev 4.153
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U18-ch112, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 55.33
Std Dev 3.89
Entry
ampl
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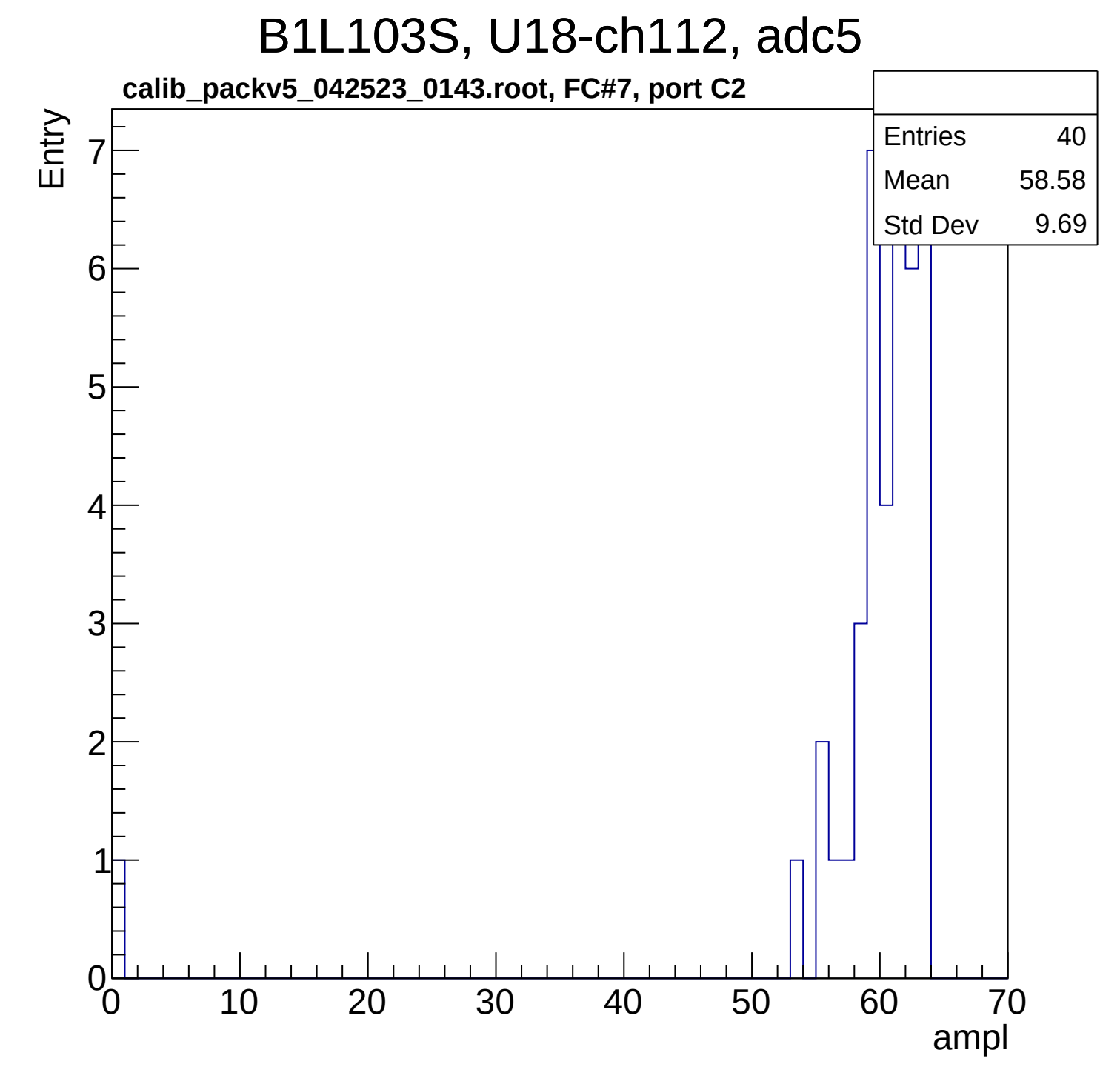
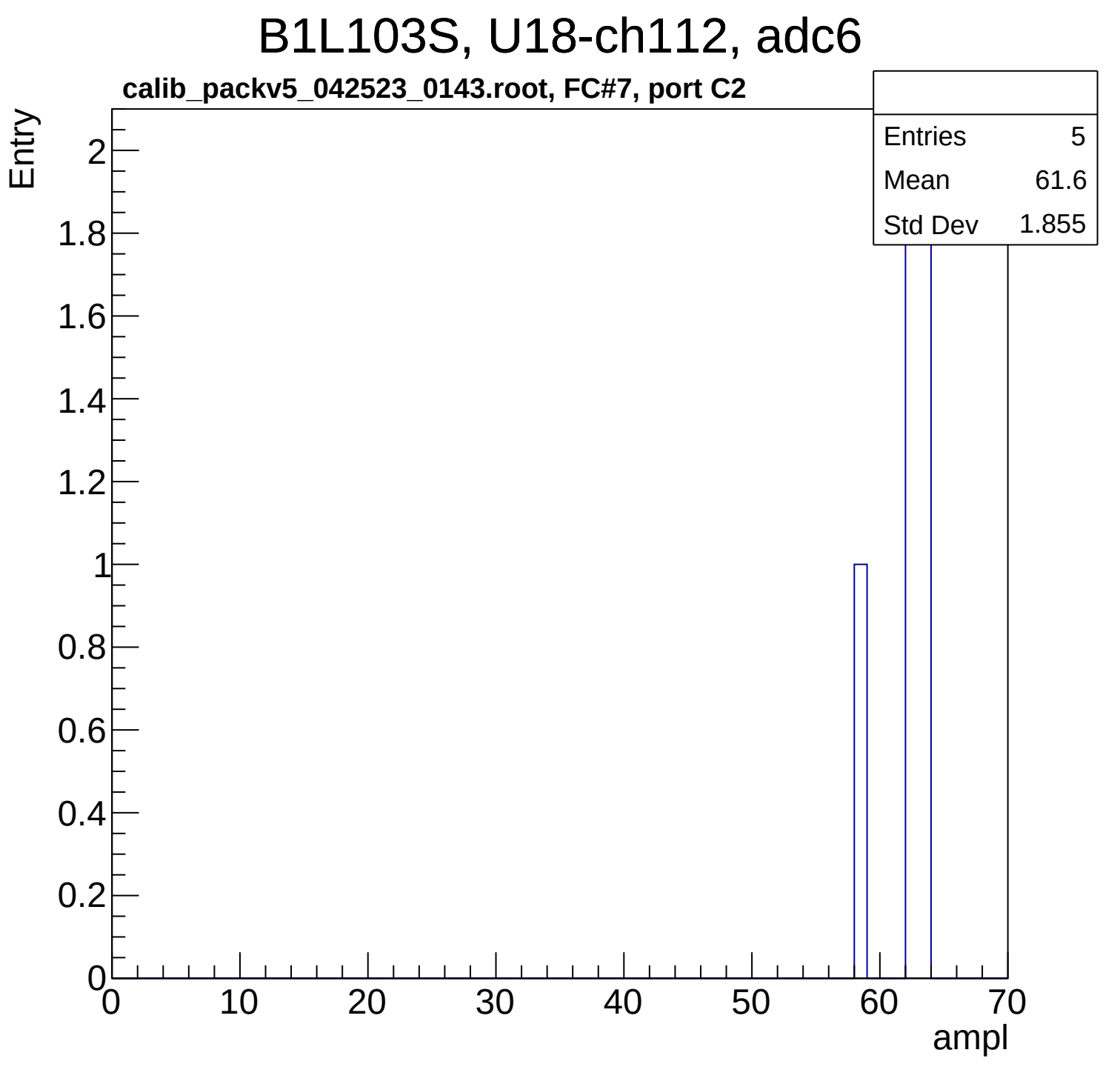
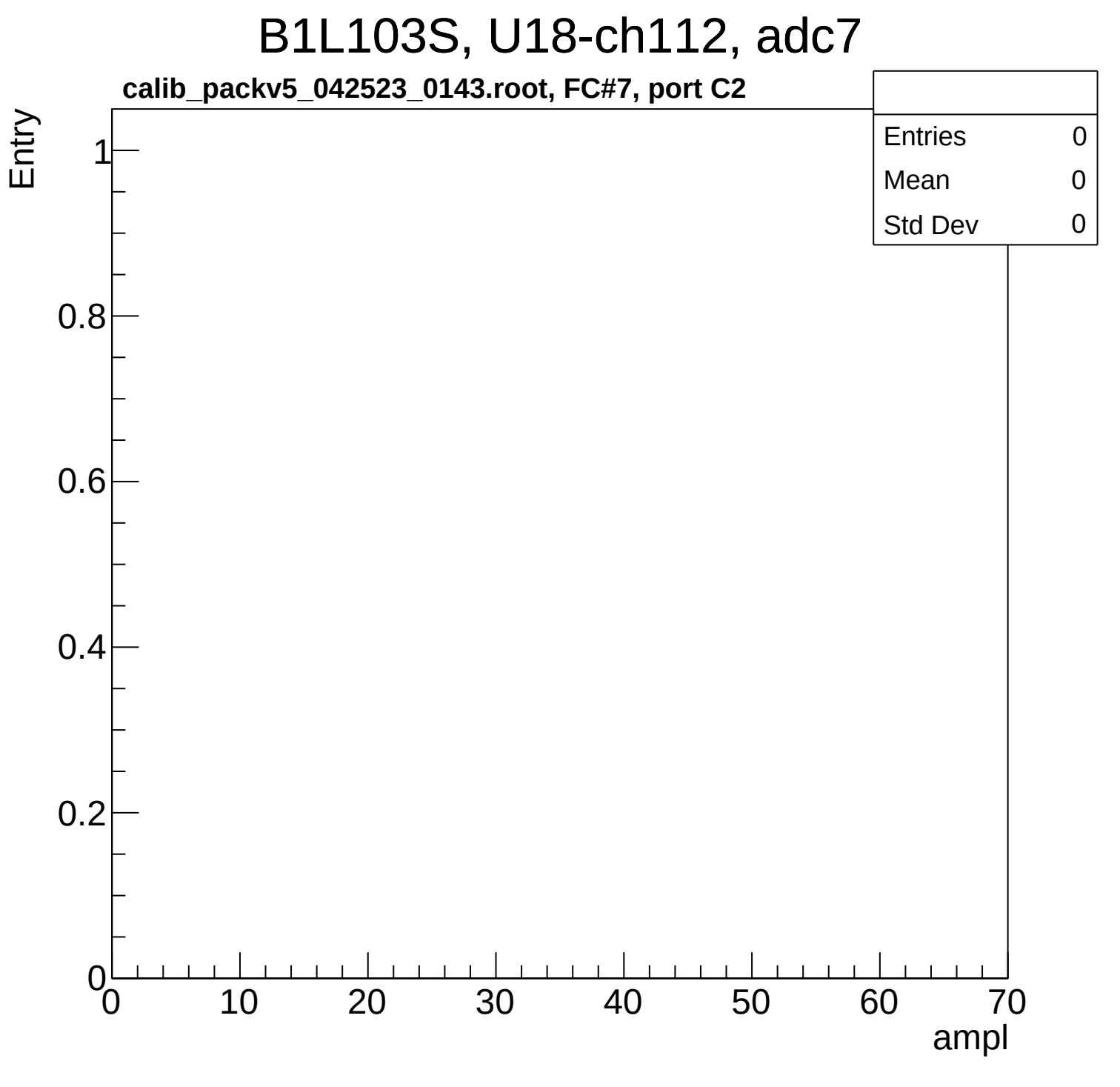
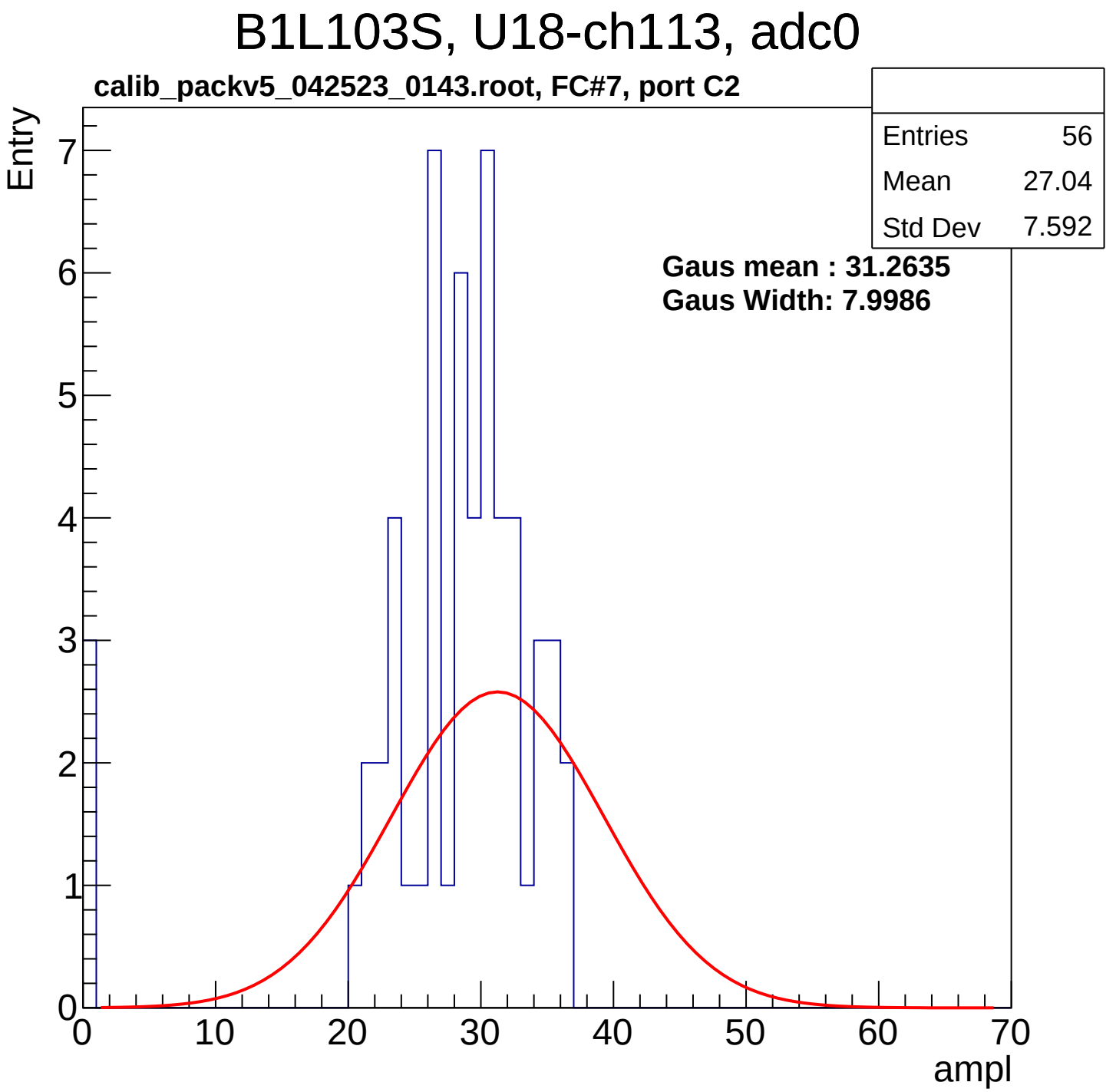
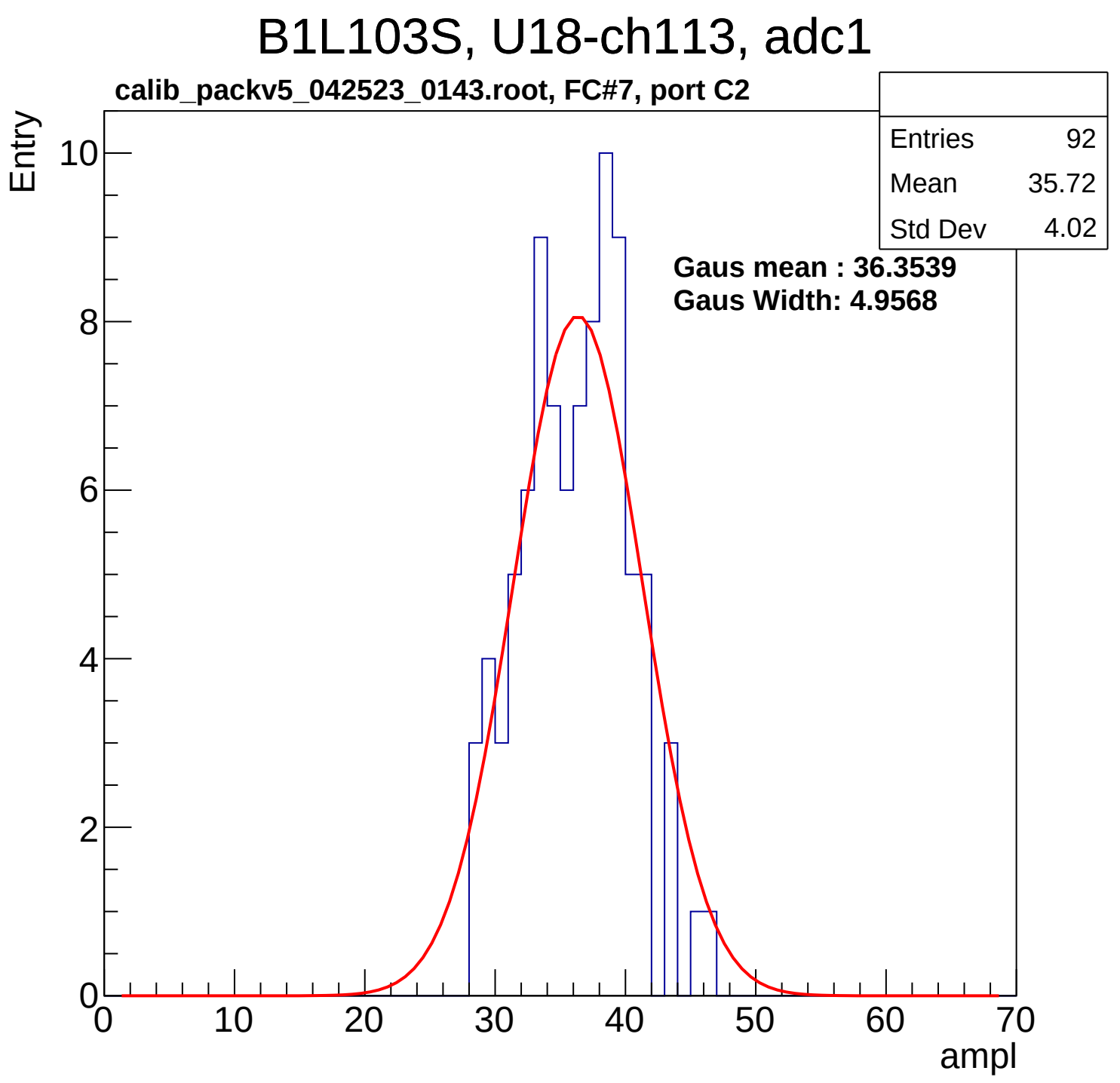
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

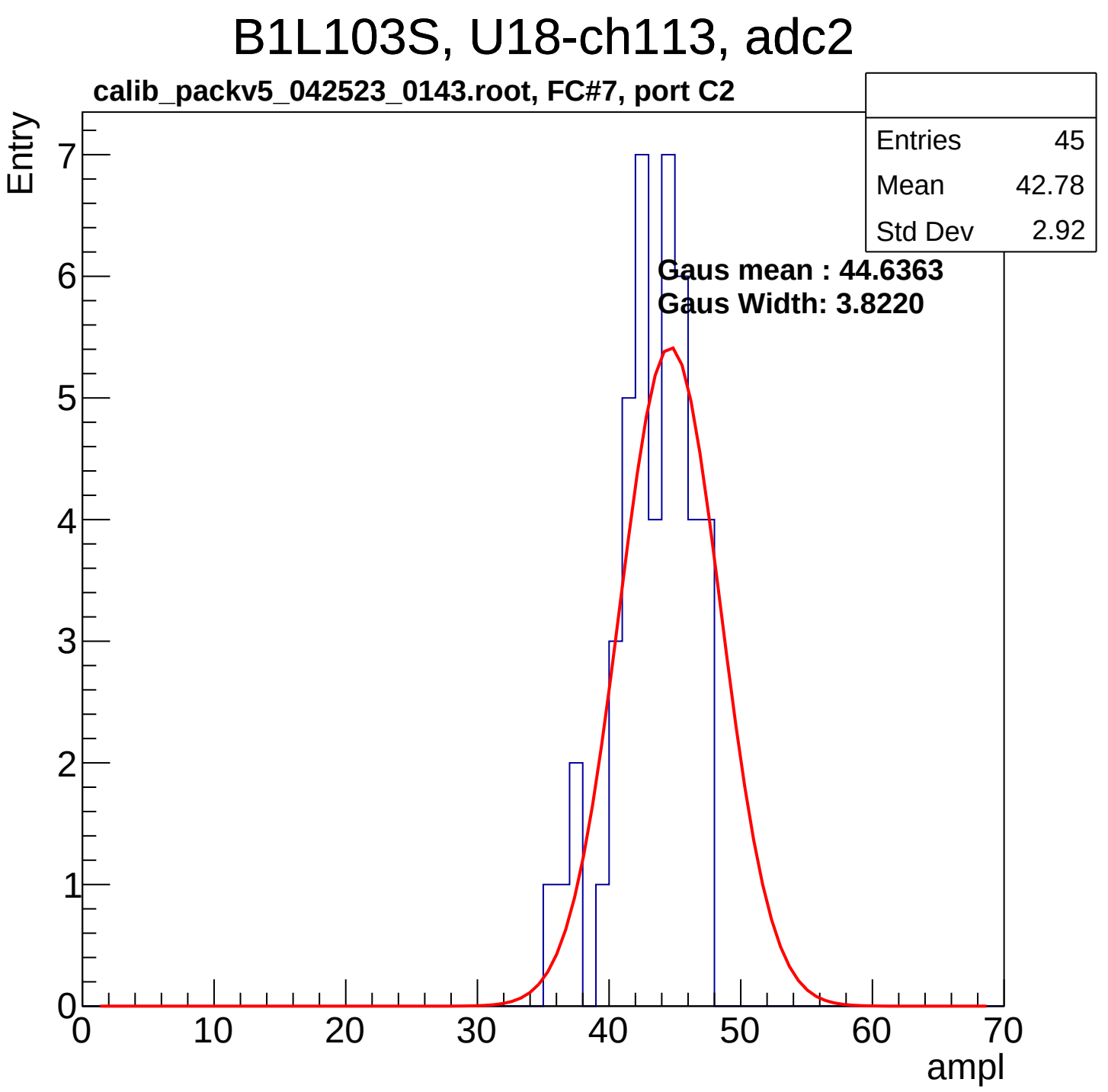

B1L103S, U18-ch112, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 40
Mean 58.58
Std Dev 9.69
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch112, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 5
Mean 61.6
Std Dev 1.855
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U18-ch112, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch113, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 27.04
Std Dev 7.592
Gaus mean : 31.2635
Gaus Width: 7.9986
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch113, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 92
Mean 35.72
Std Dev 4.02
Gaus mean : 36.3539
Gaus Width: 4.9568
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch113, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 45
Mean 42.78
Std Dev 2.92
Gaus mean : 44.6363
Gaus Width: 3.8220
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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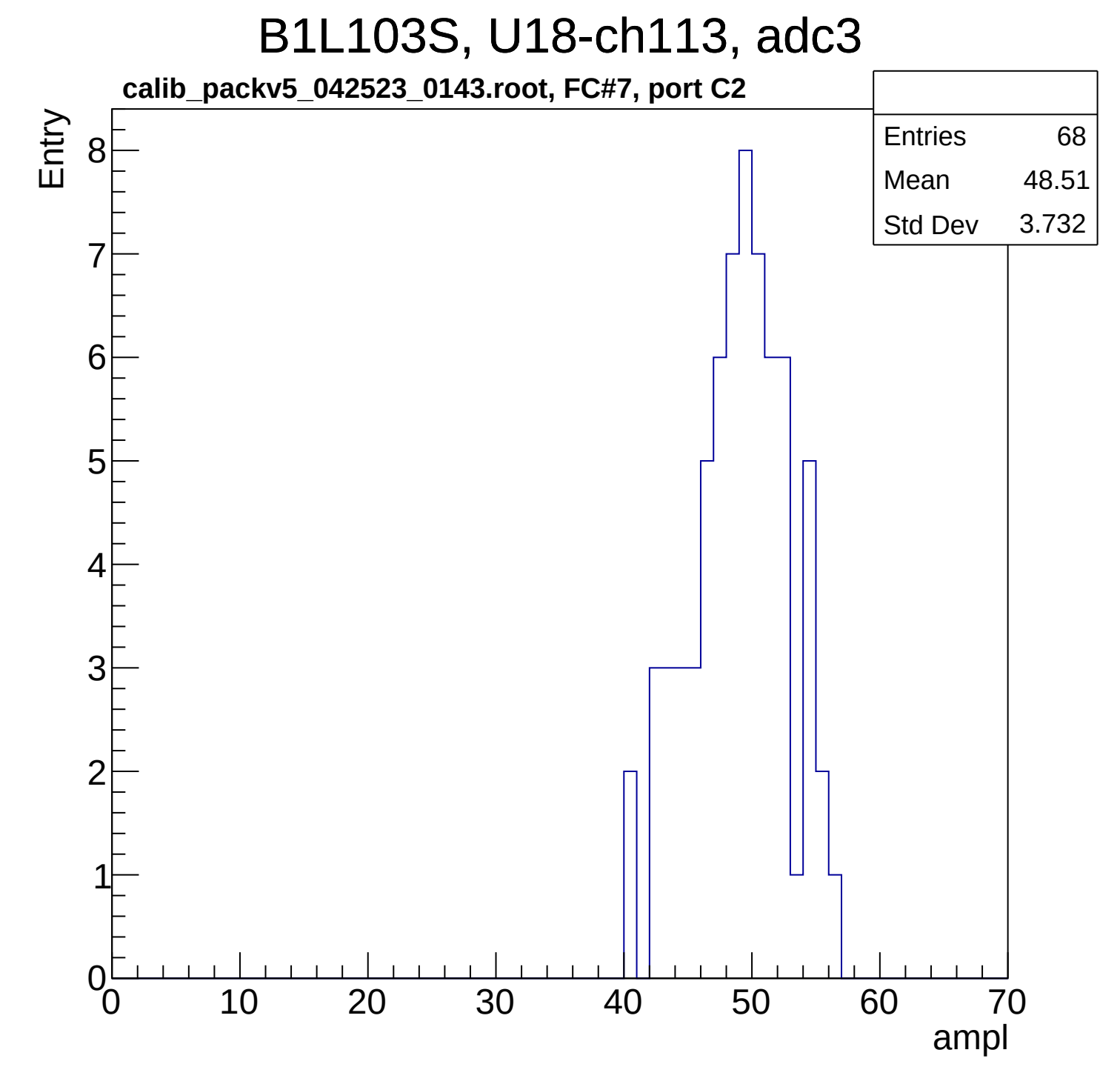
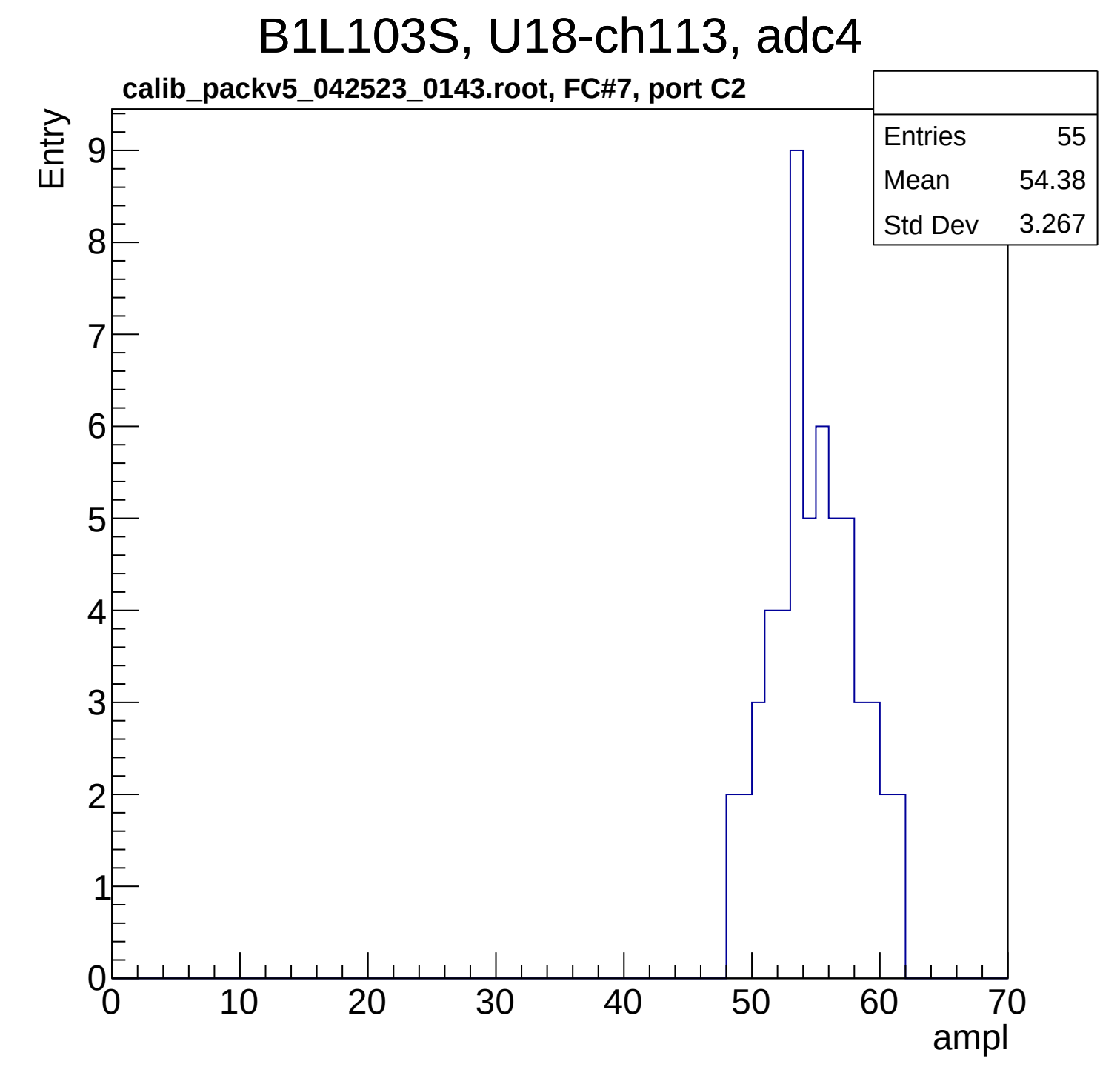

B1L103S, U18-ch113, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 48.51
Std Dev 3.732
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch113, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 54.38
Std Dev 3.267
Entry
ampl
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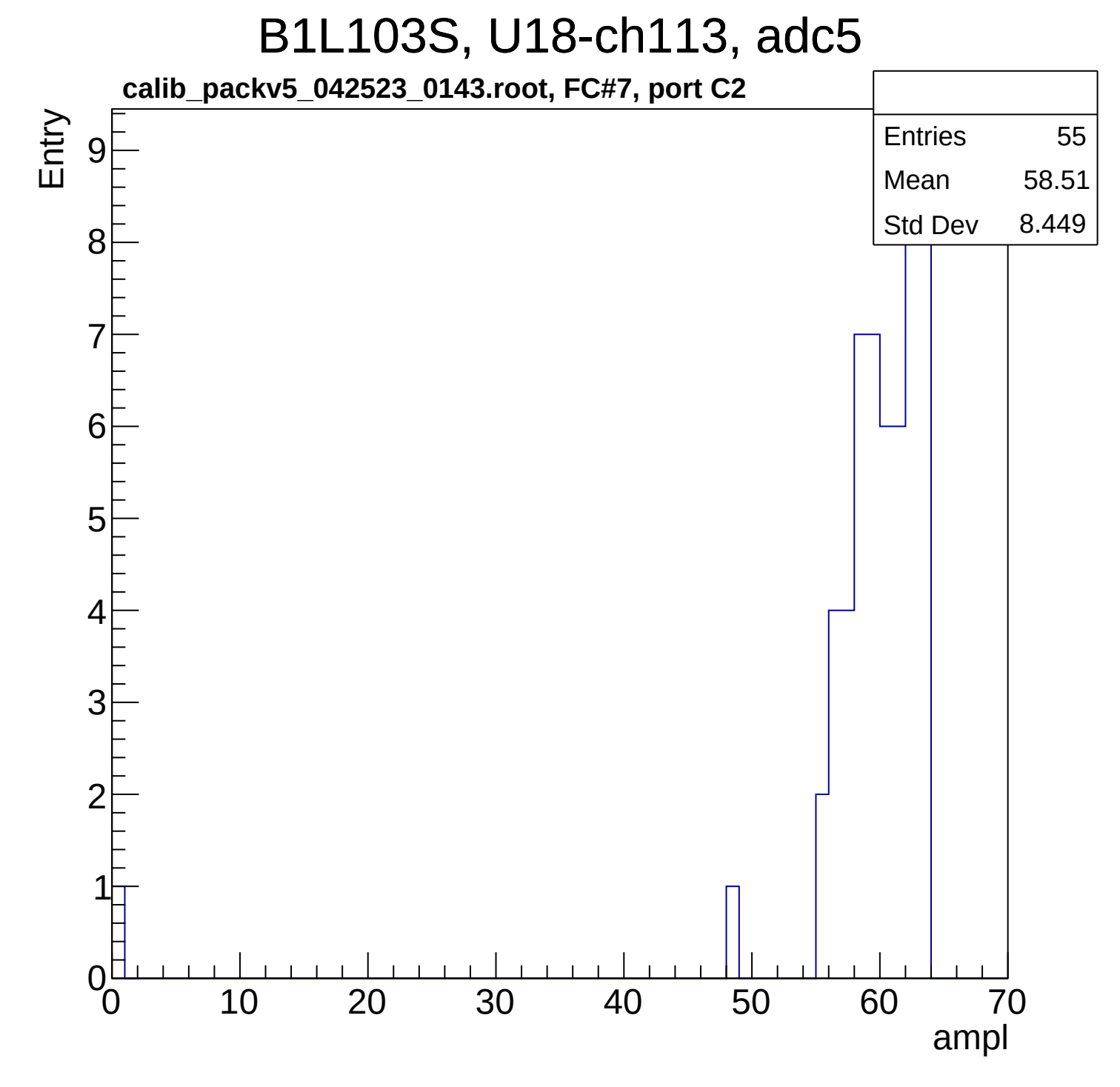
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch113, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 58.51
Std Dev 8.449
Entry
ampl
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2
3
4
5
6
7
8
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0
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60
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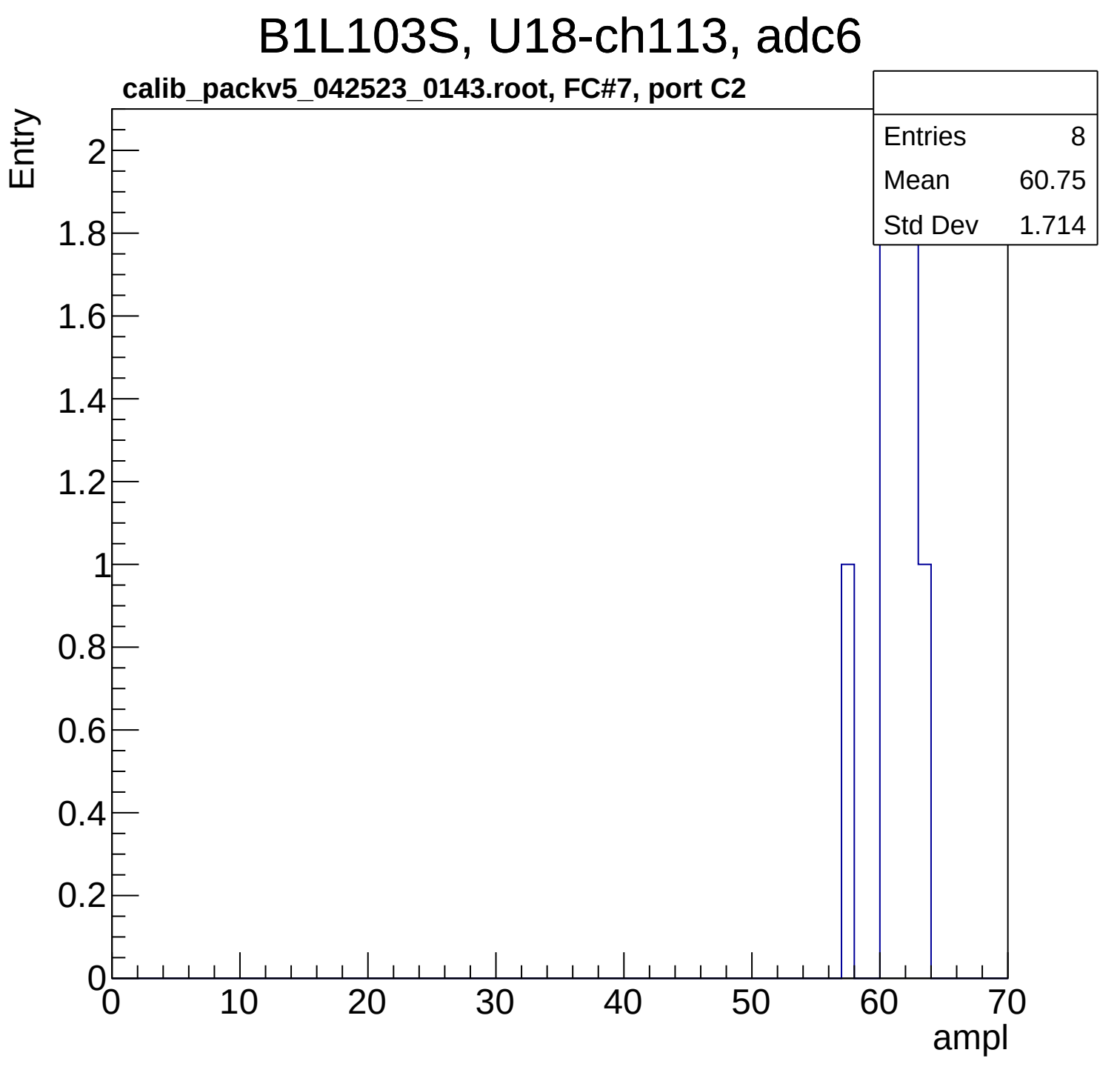
B1L103S, U18-ch113, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 8
Mean 60.75
Std Dev 1.714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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60
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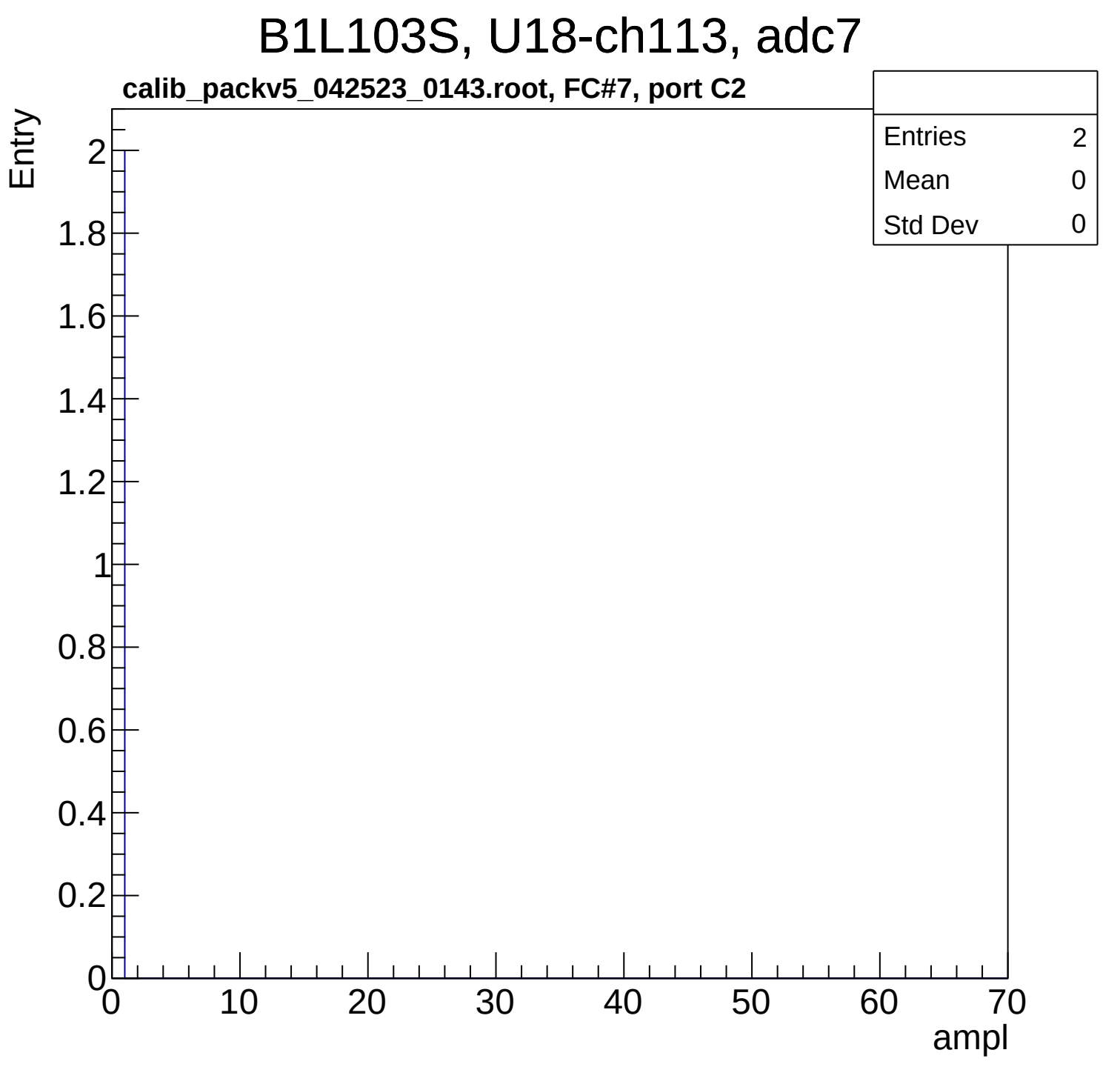
B1L103S, U18-ch113, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
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1.2
1.4
1.6
1.8
2
0
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60
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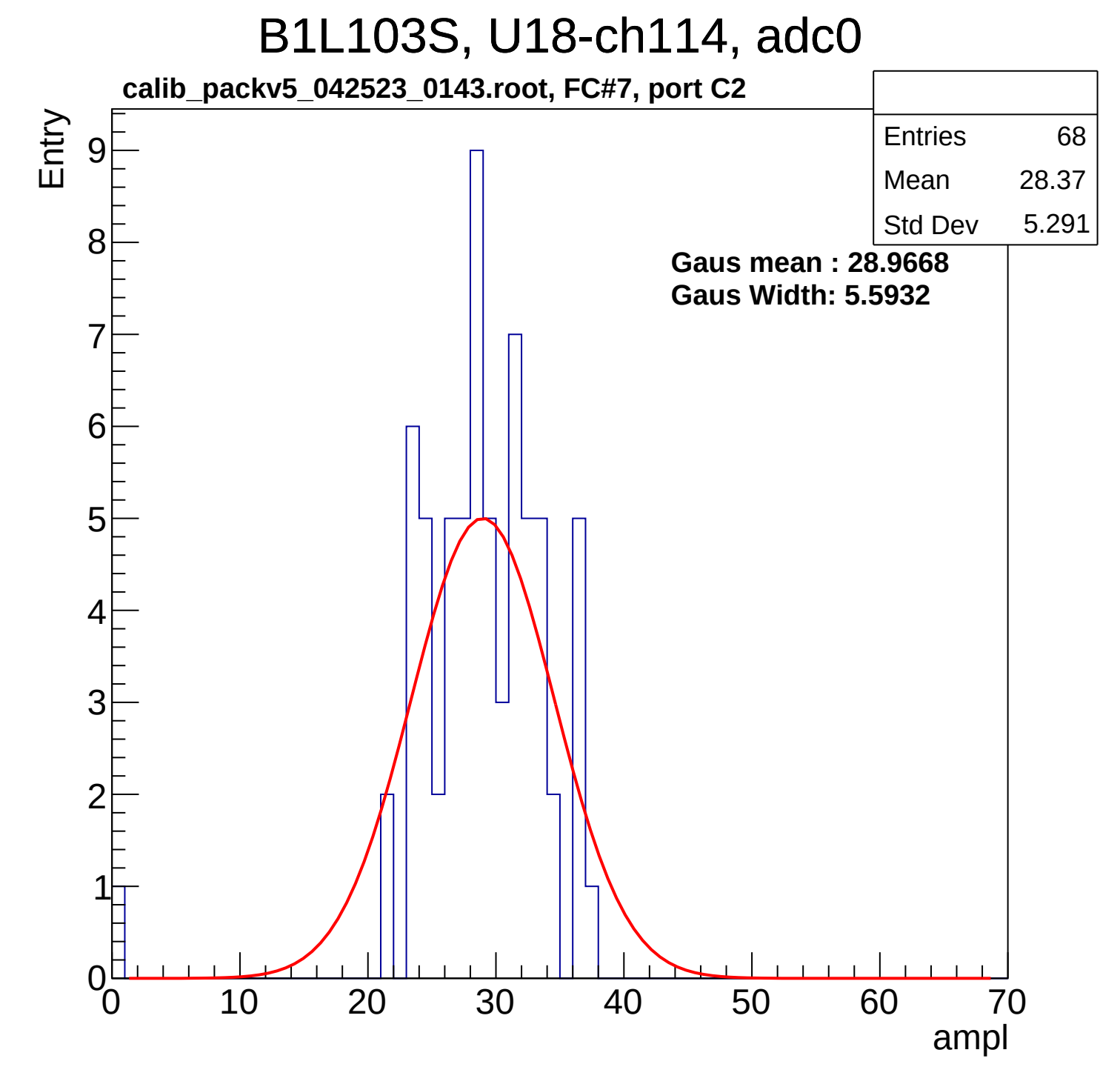
B1L103S, U18-ch114, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 28.37
Std Dev 5.291
Gaus mean : 28.9668
Gaus Width: 5.5932
Entry
ampl
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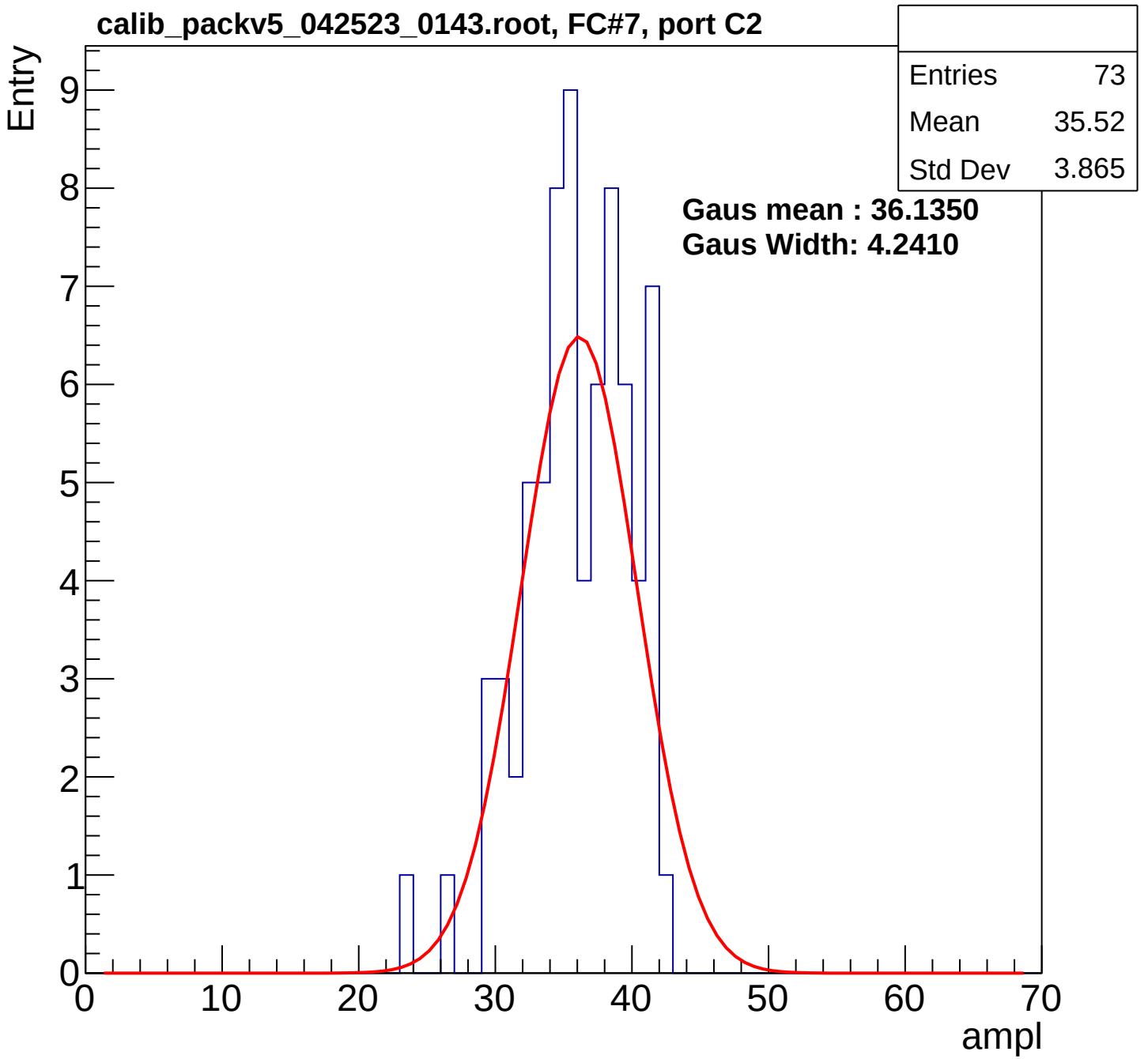
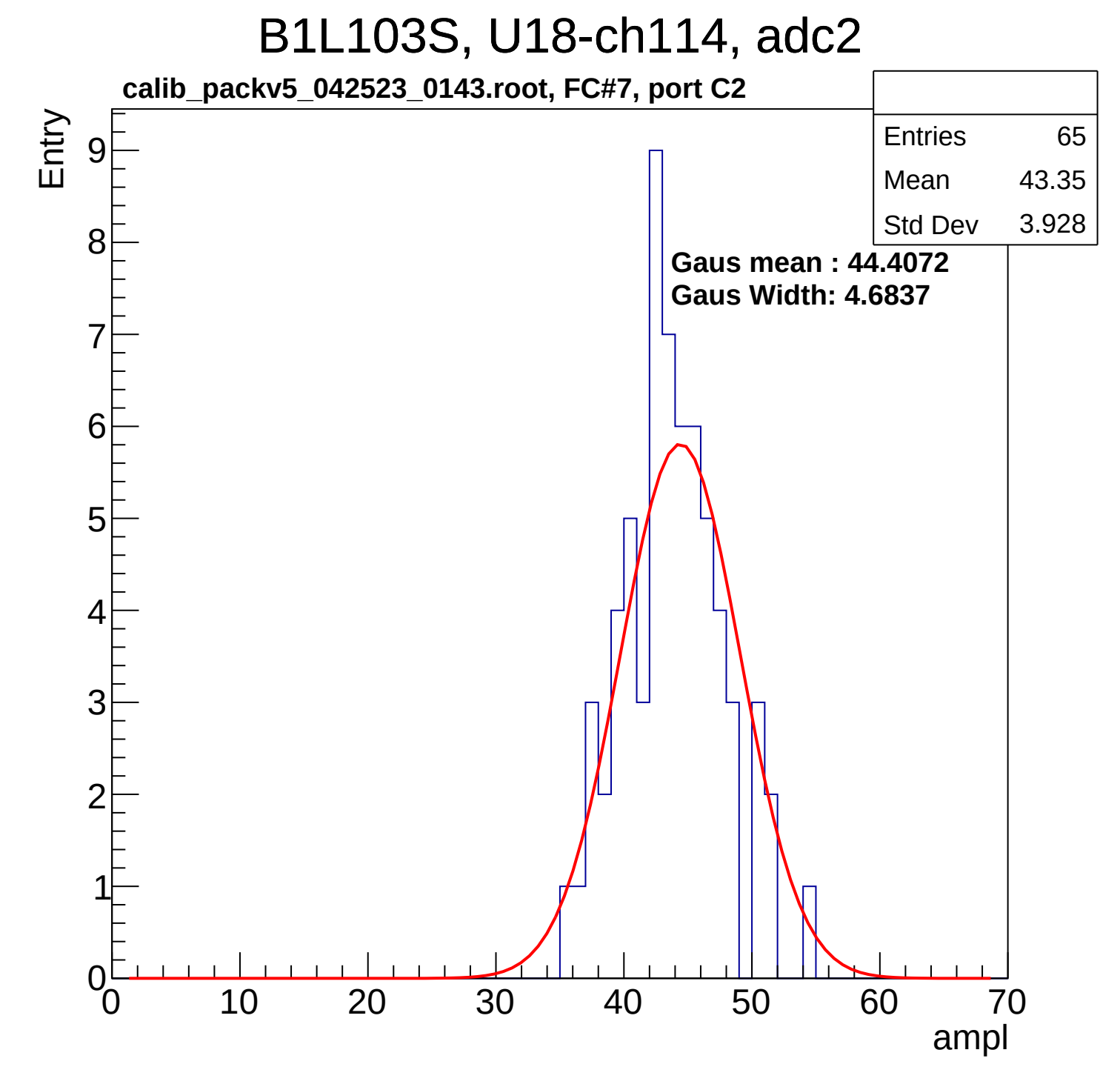
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch114, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 73
Mean 35.52
Std Dev 3.865
Gaus mean : 36.1350
Gaus Width: 4.2410
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch114, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 43.35
Std Dev 3.928
Gaus mean : 44.4072
Gaus Width: 4.6837
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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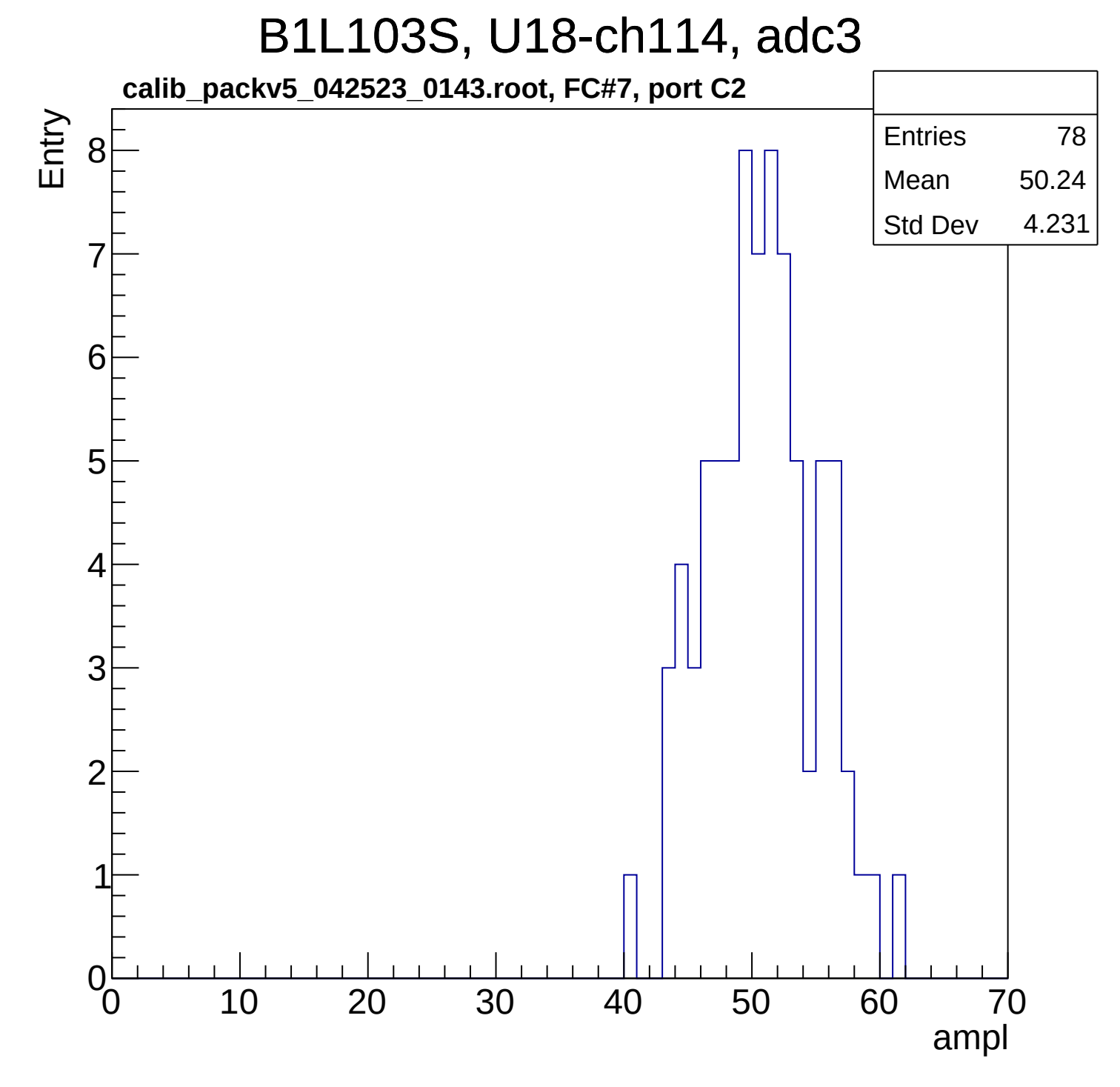
B1L103S, U18-ch114, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 78
Mean 50.24
Std Dev 4.231
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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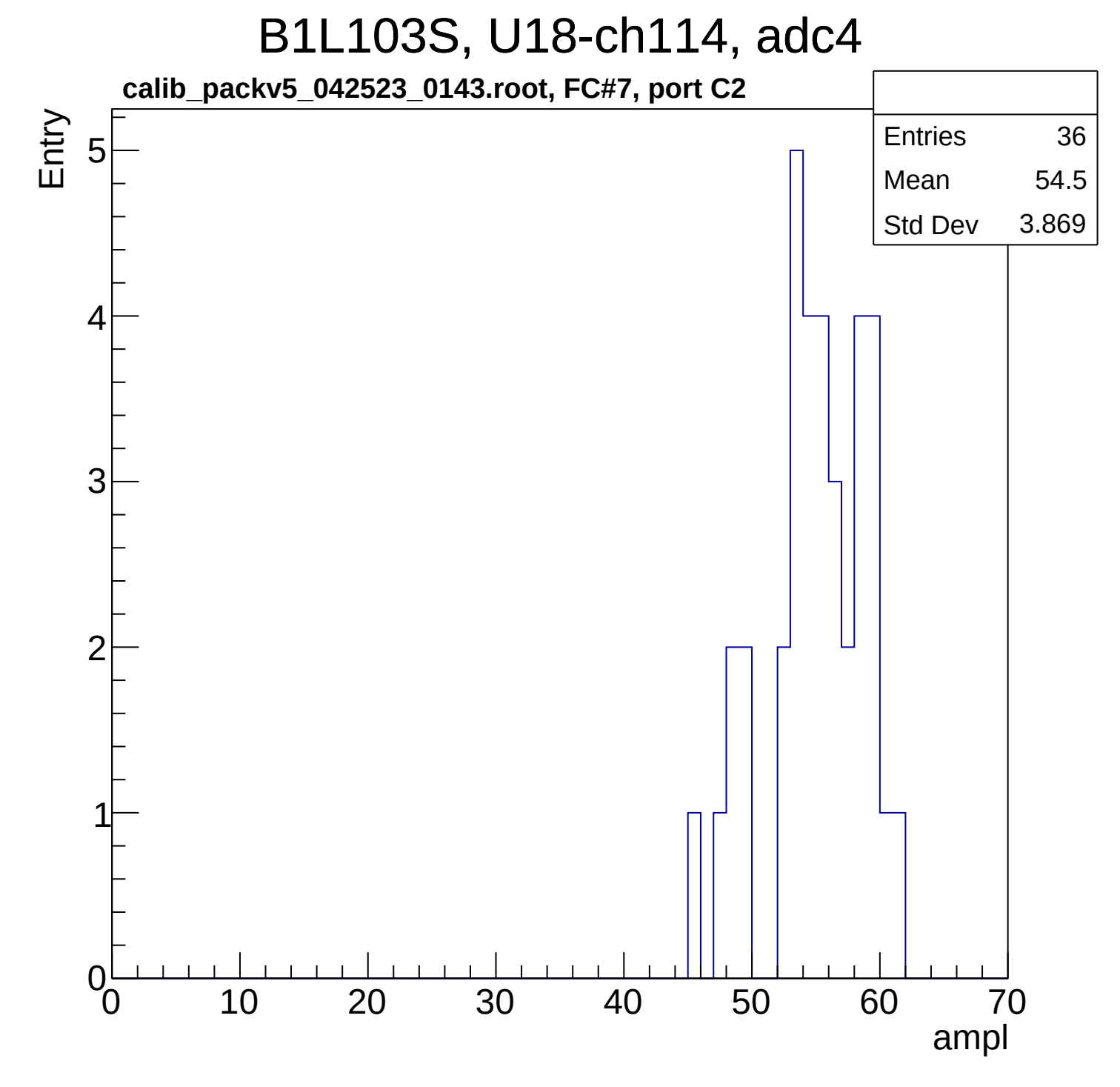
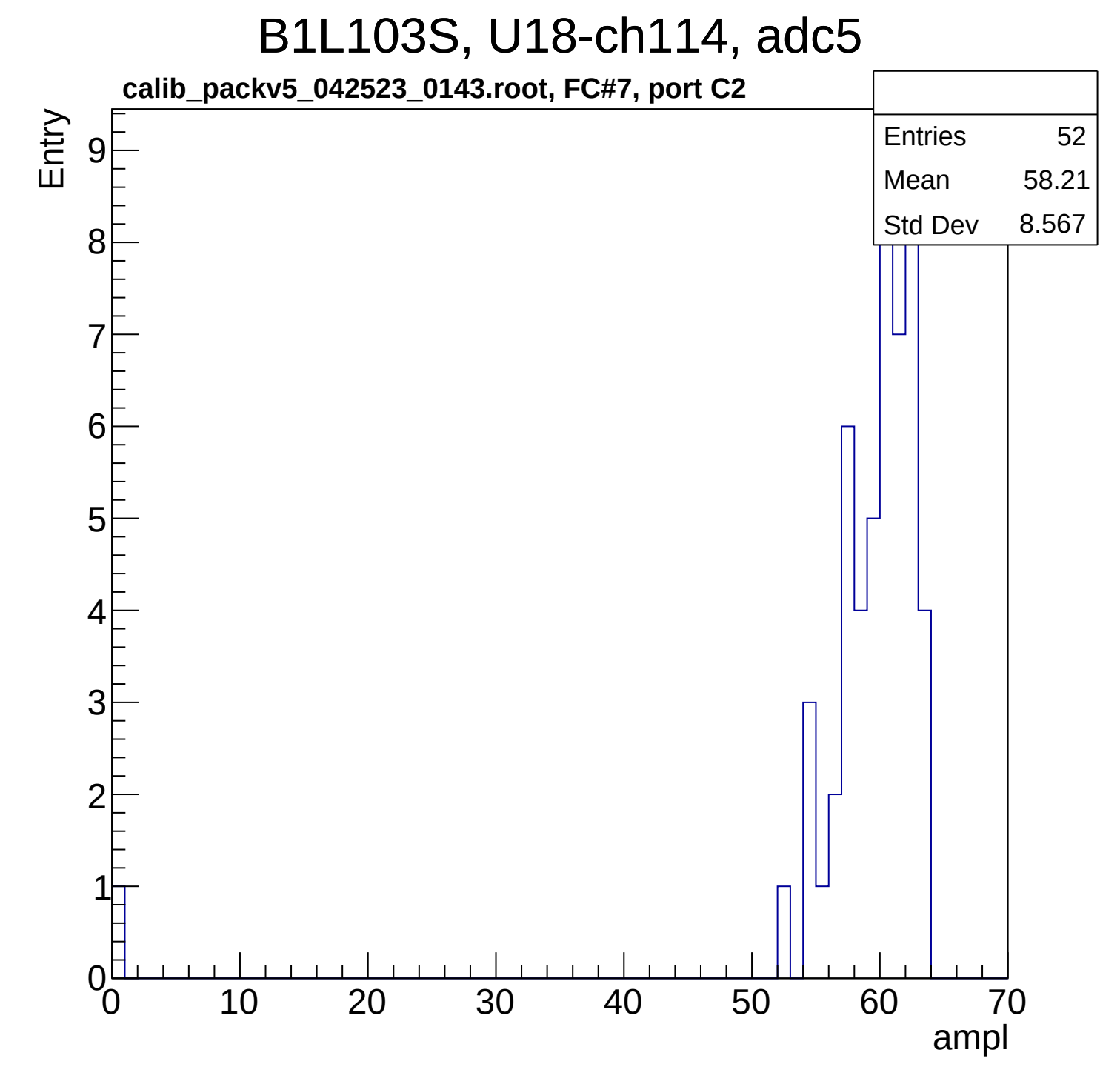
40
50
60
70


B1L103S, U18-ch114, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 36
Mean 54.5
Std Dev 3.869
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch114, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 52
Mean 58.21
Std Dev 8.567
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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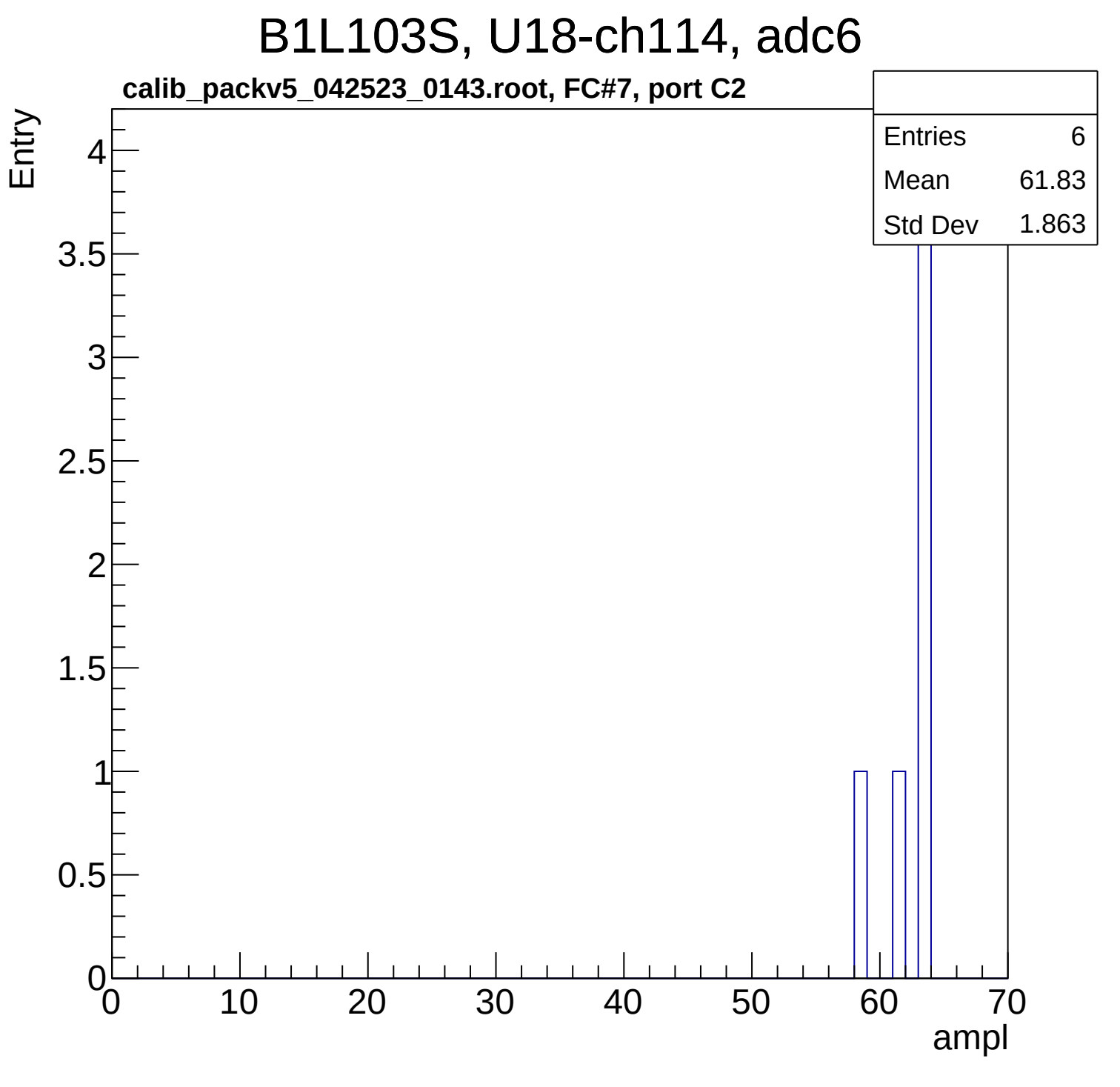
40
50
60
70


B1L103S, U18-ch114, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 6
Mean 61.83
Std Dev 1.863
Entry
ampl
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0.5
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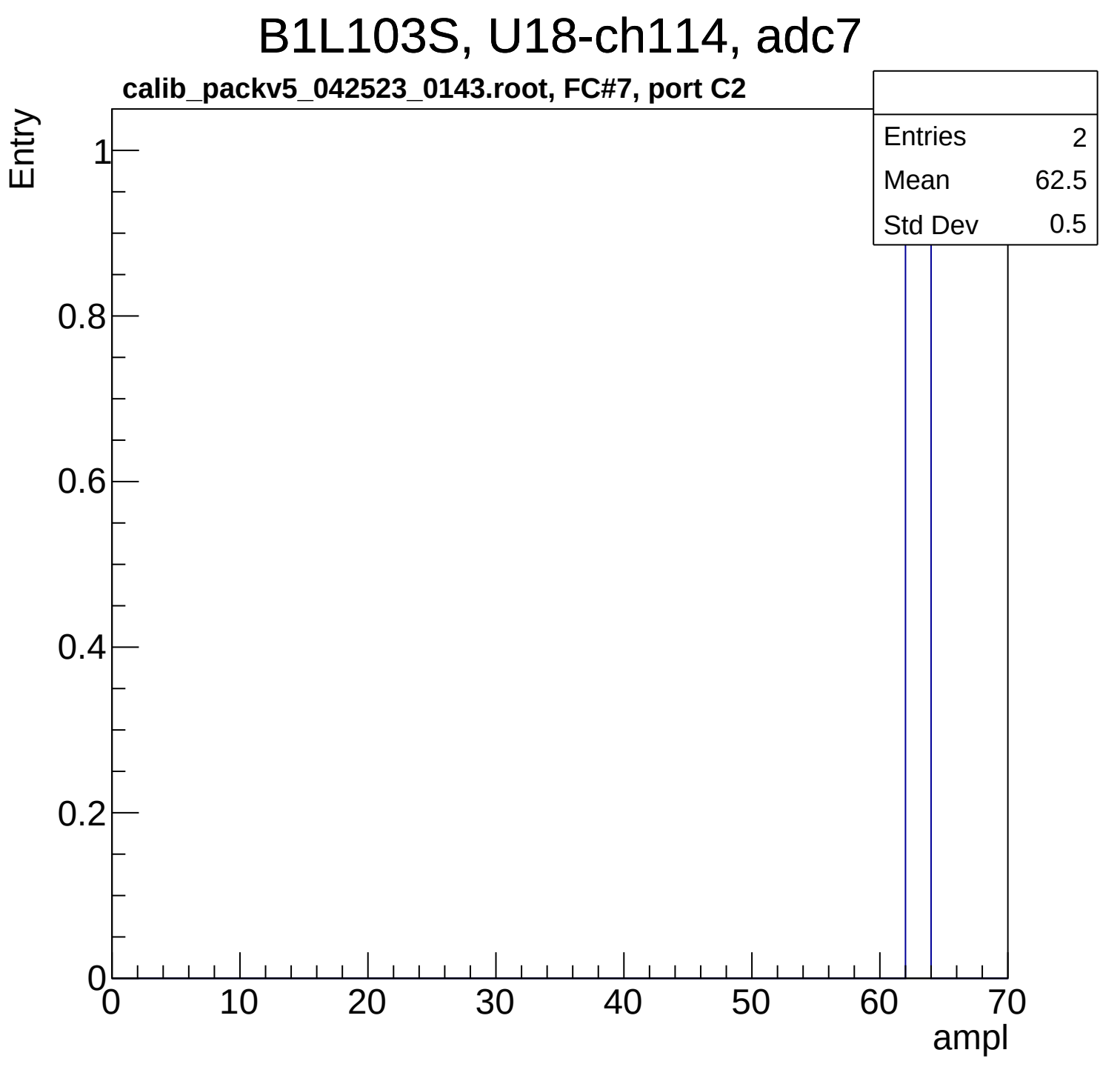
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U18-ch114, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
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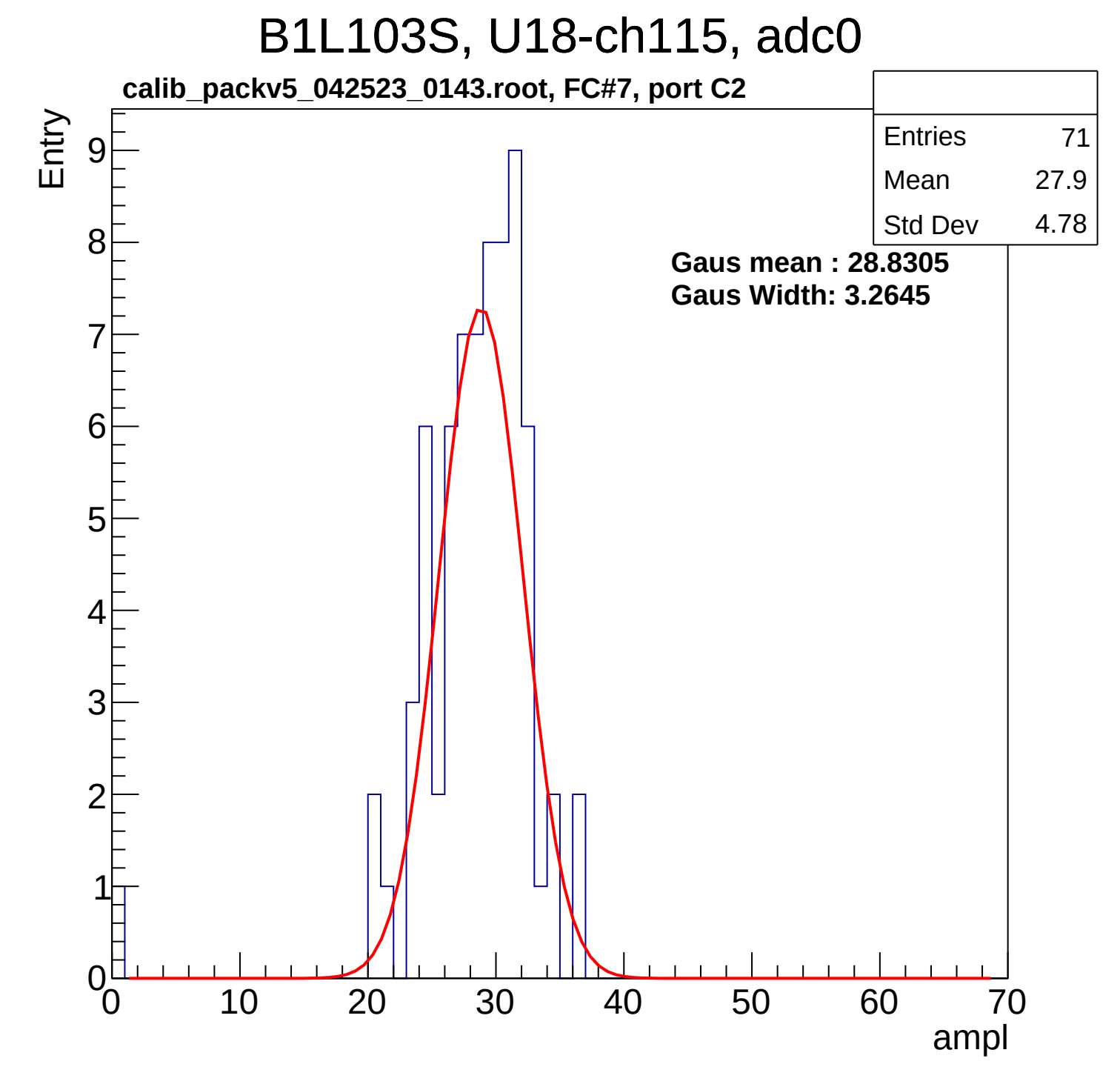
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch115, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 71
Mean 27.9
Std Dev 4.78
Gaus mean : 28.8305
Gaus Width: 3.2645
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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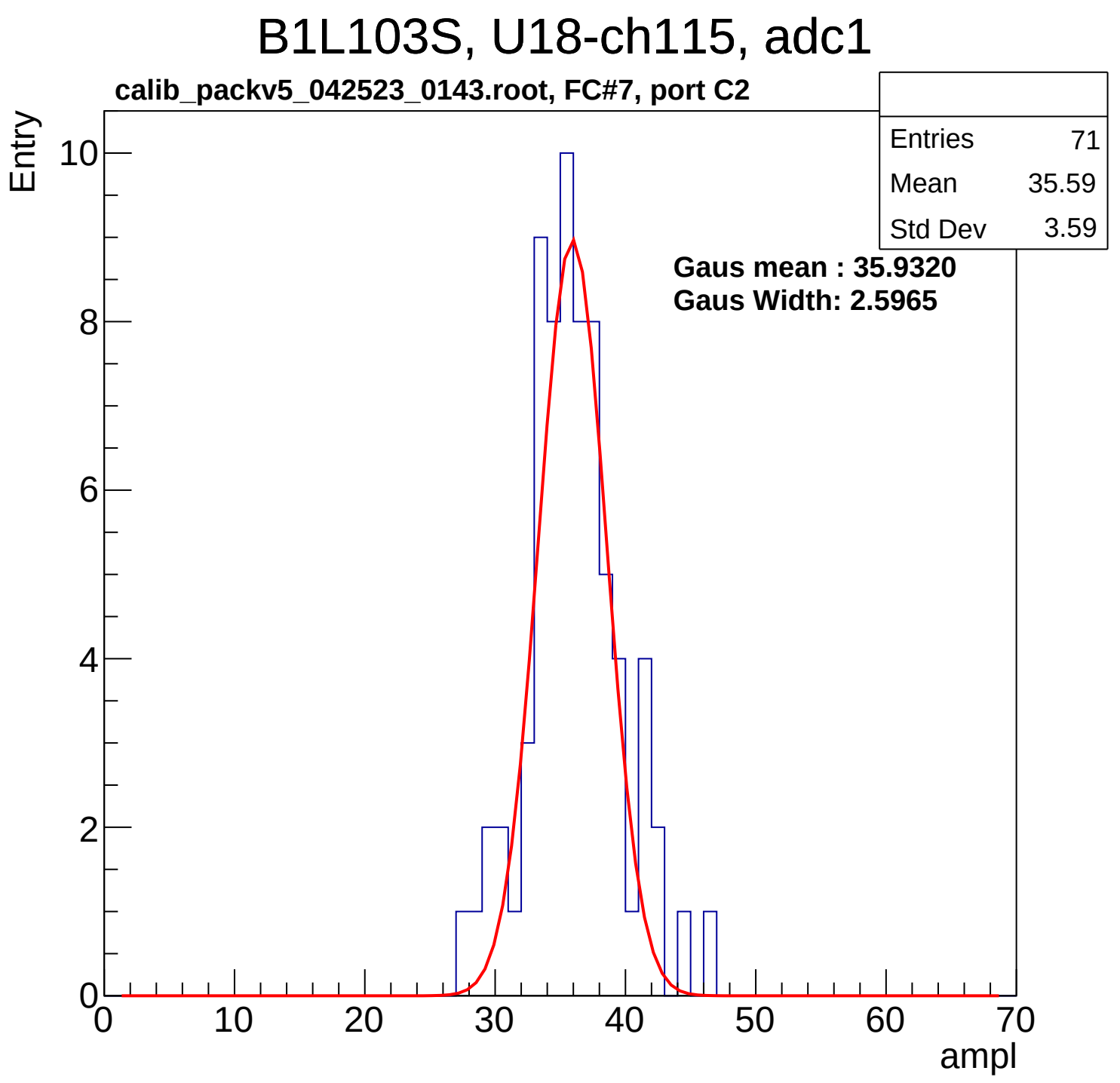
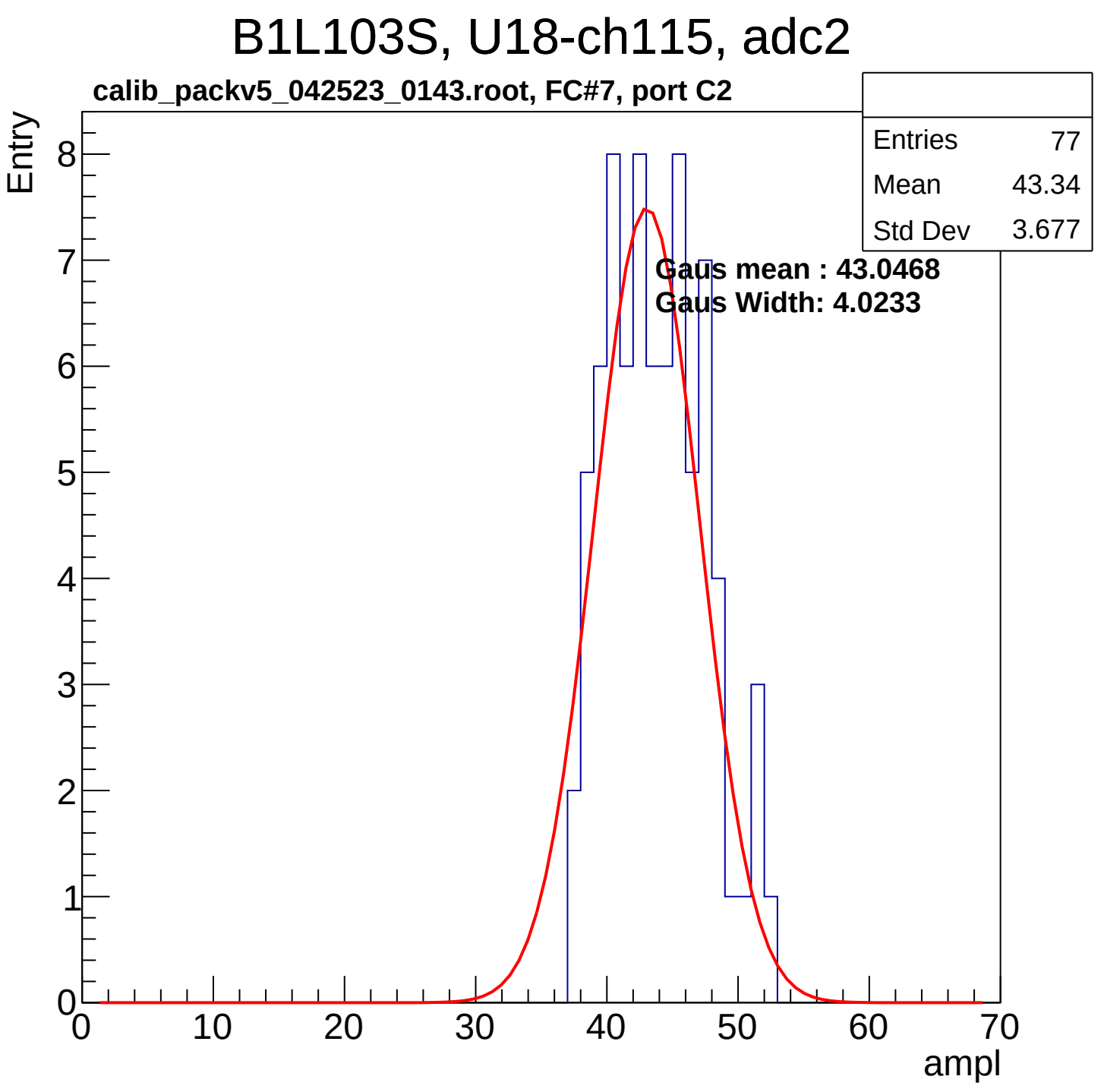
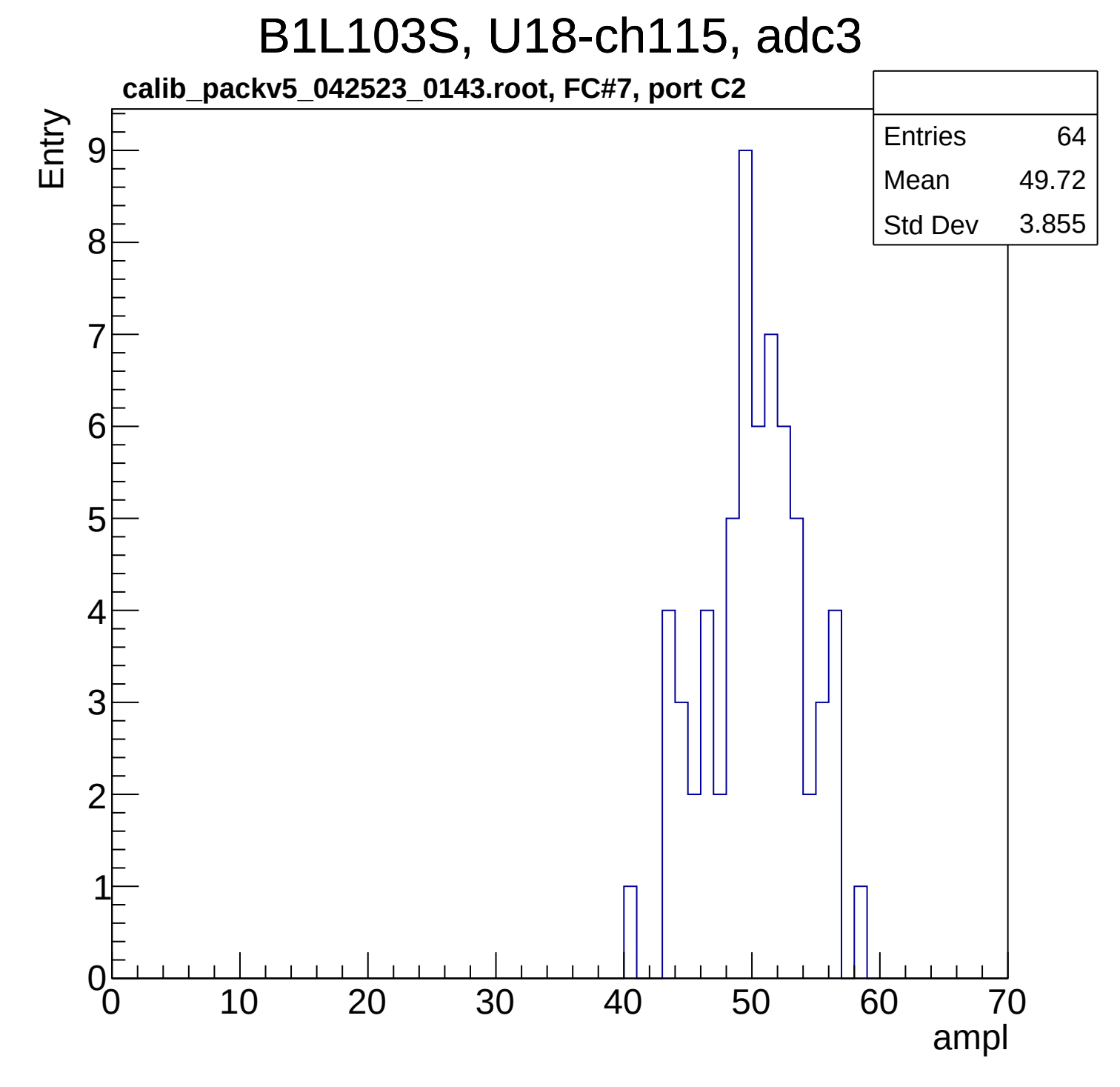

B1L103S, U18-ch115, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 71
Mean 35.59
Std Dev 3.59
Gaus mean : 35.9320
Gaus Width: 2.5965
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch115, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 77
Mean 43.34
Std Dev 3.677
Gaus mean : 43.0468
Gaus Width: 4.0233
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch115, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 49.72
Std Dev 3.855
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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40
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60
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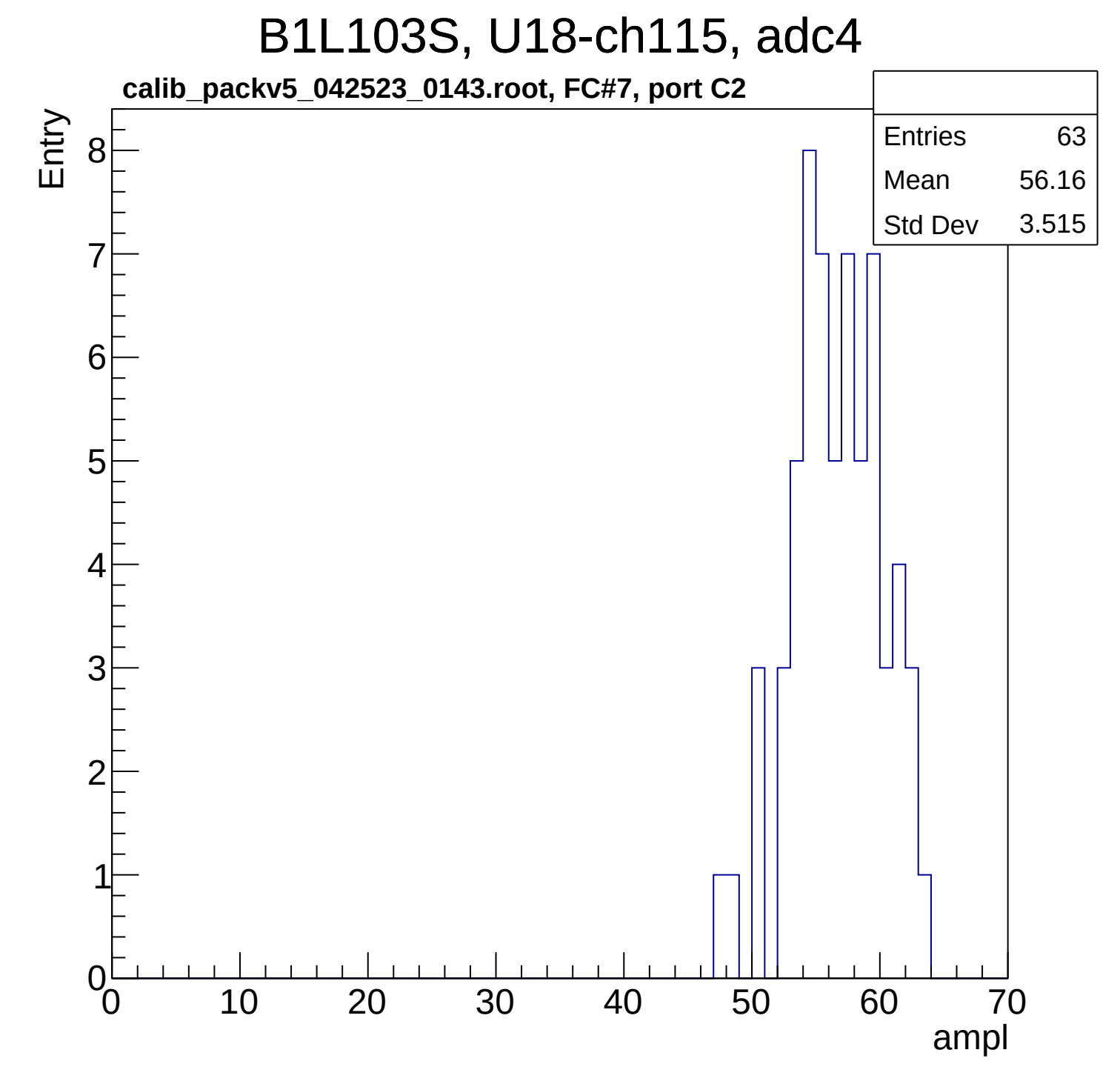
B1L103S, U18-ch115, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 56.16
Std Dev 3.515
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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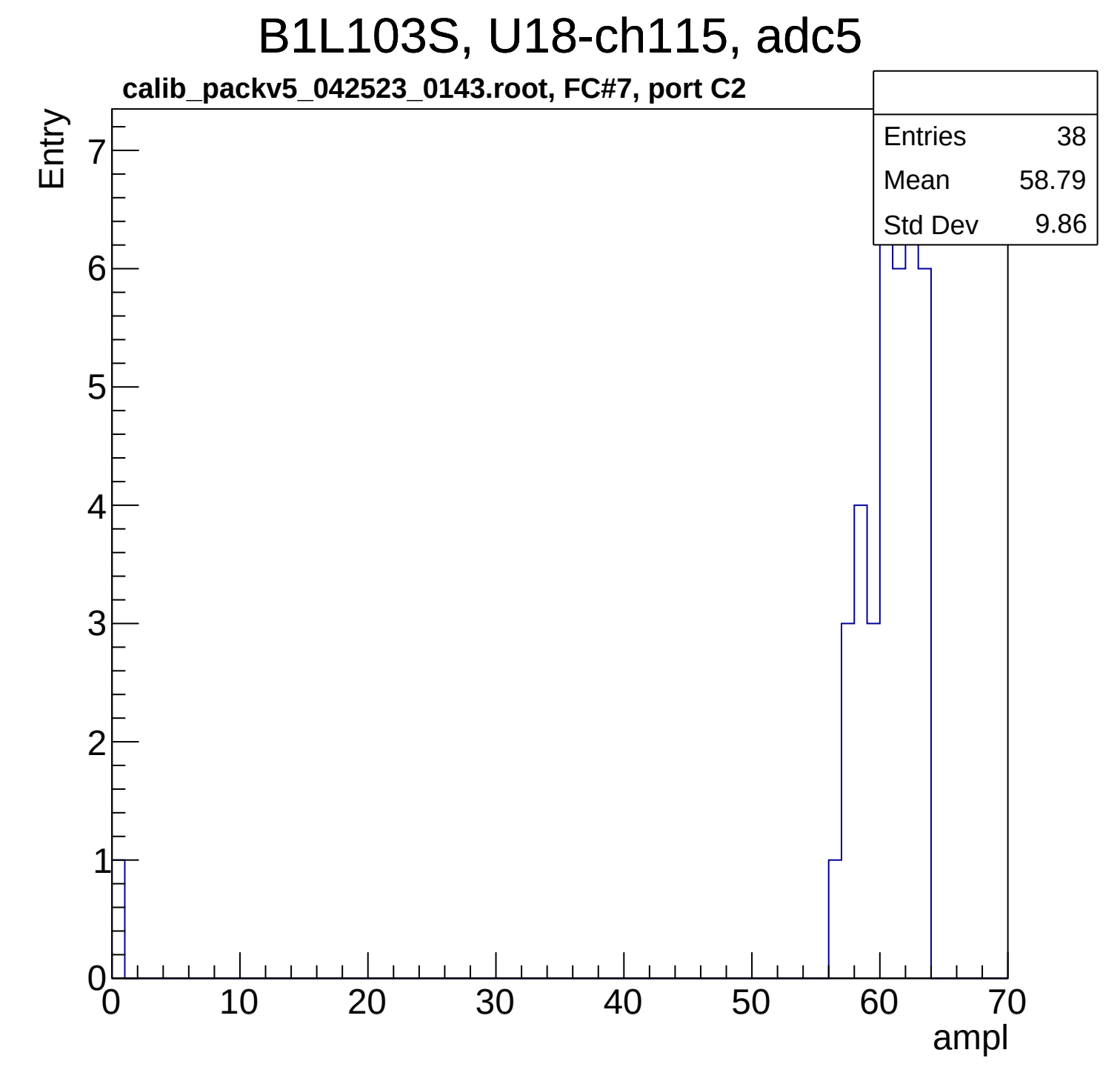
B1L103S, U18-ch115, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 38
Mean 58.79
Std Dev 9.86
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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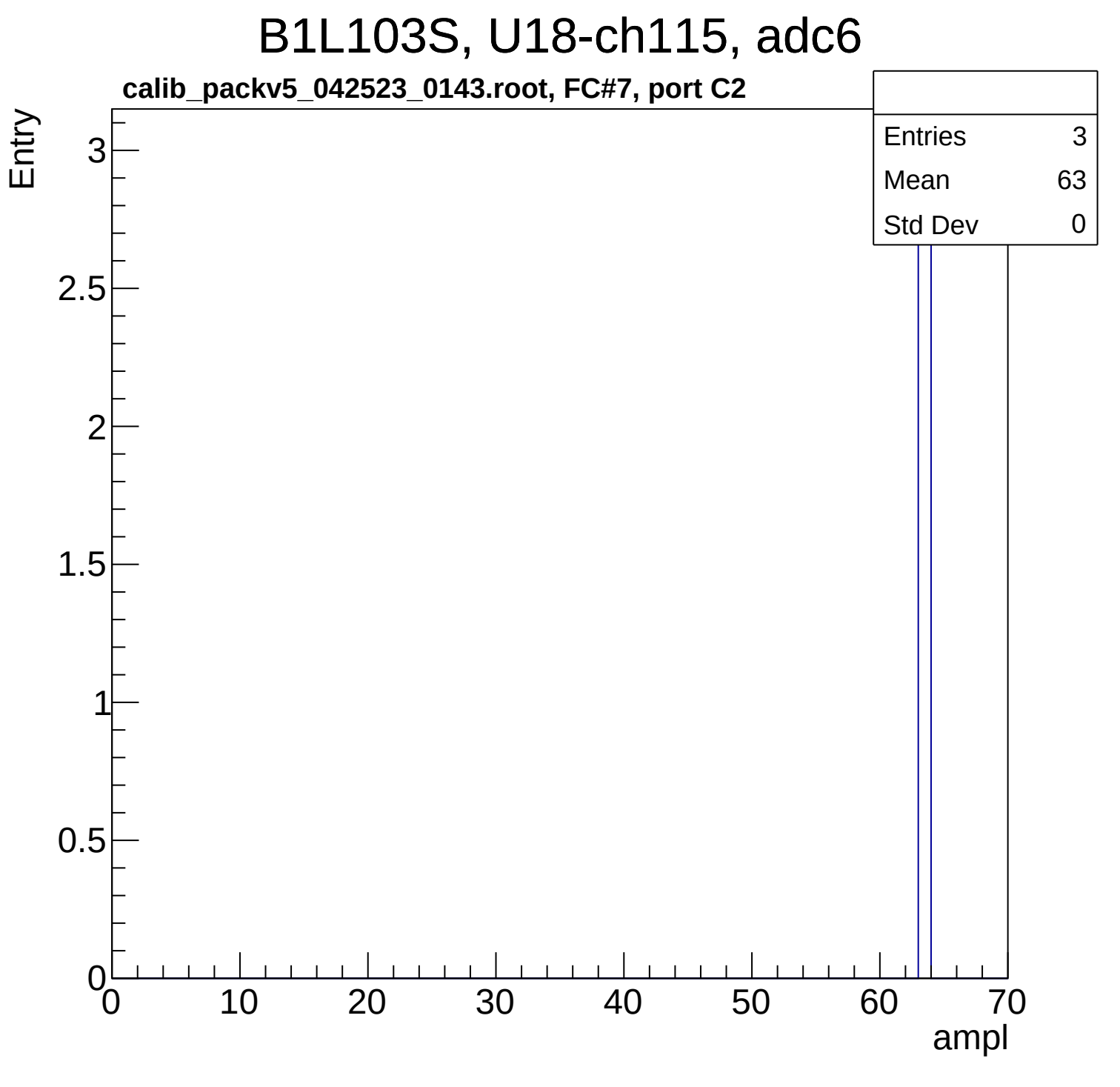
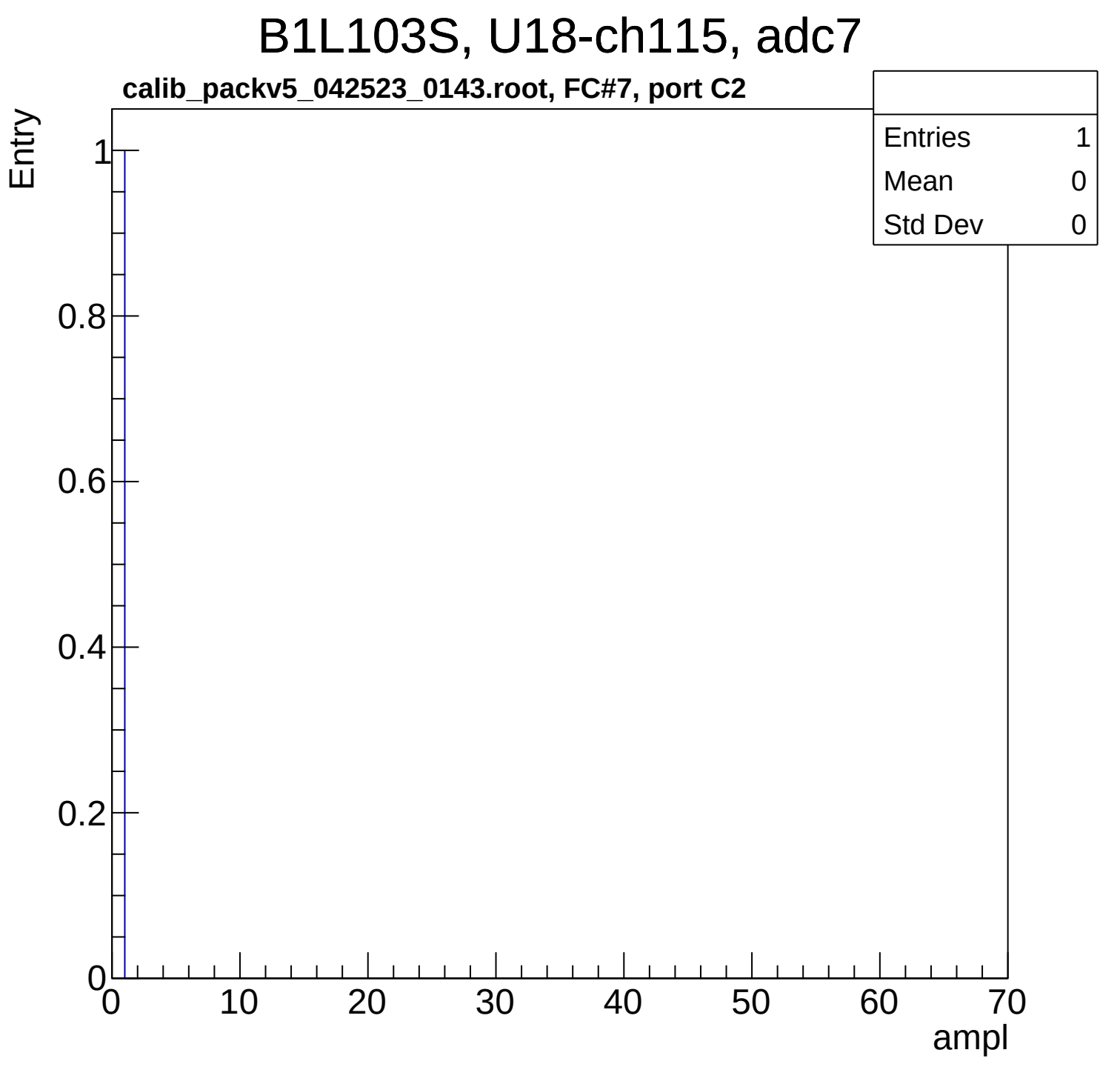
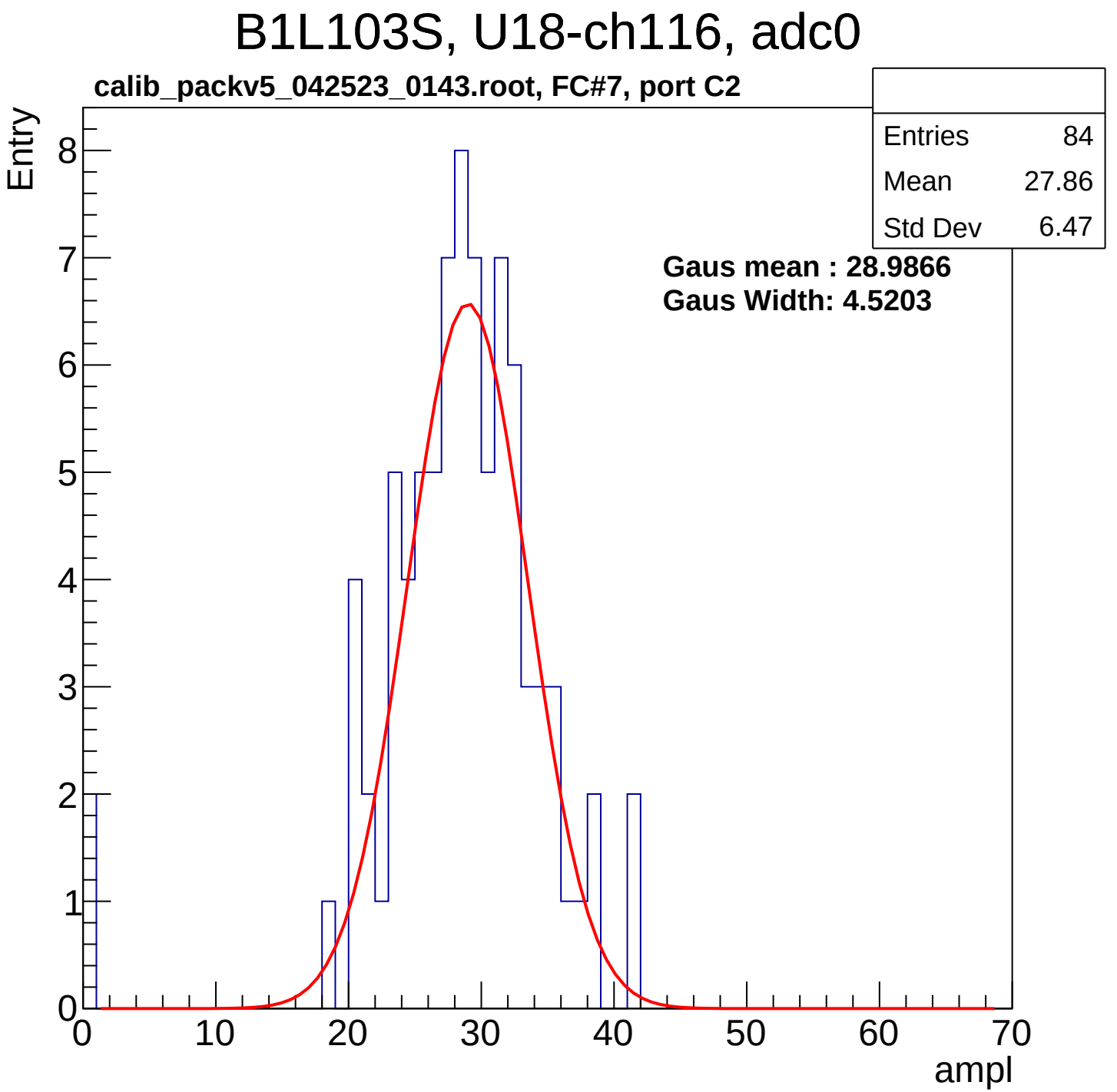
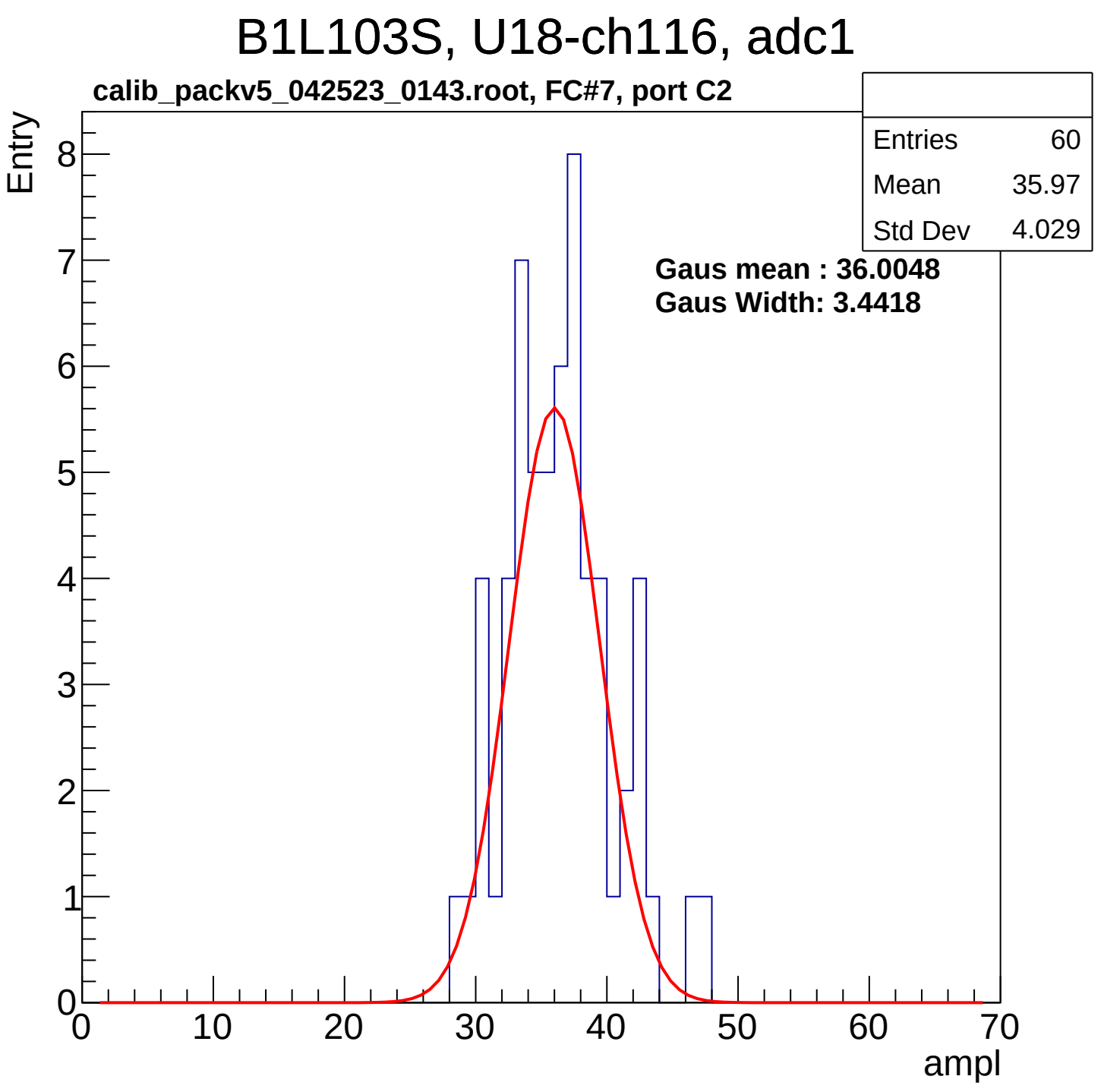

B1L103S, U18-ch115, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 63
Std Dev 0
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U18-ch115, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch116, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 84
Mean 27.86
Std Dev 6.47
Gaus mean : 28.9866
Gaus Width: 4.5203
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch116, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 60
Mean 35.97
Std Dev 4.029
Gaus mean : 36.0048
Gaus Width: 3.4418
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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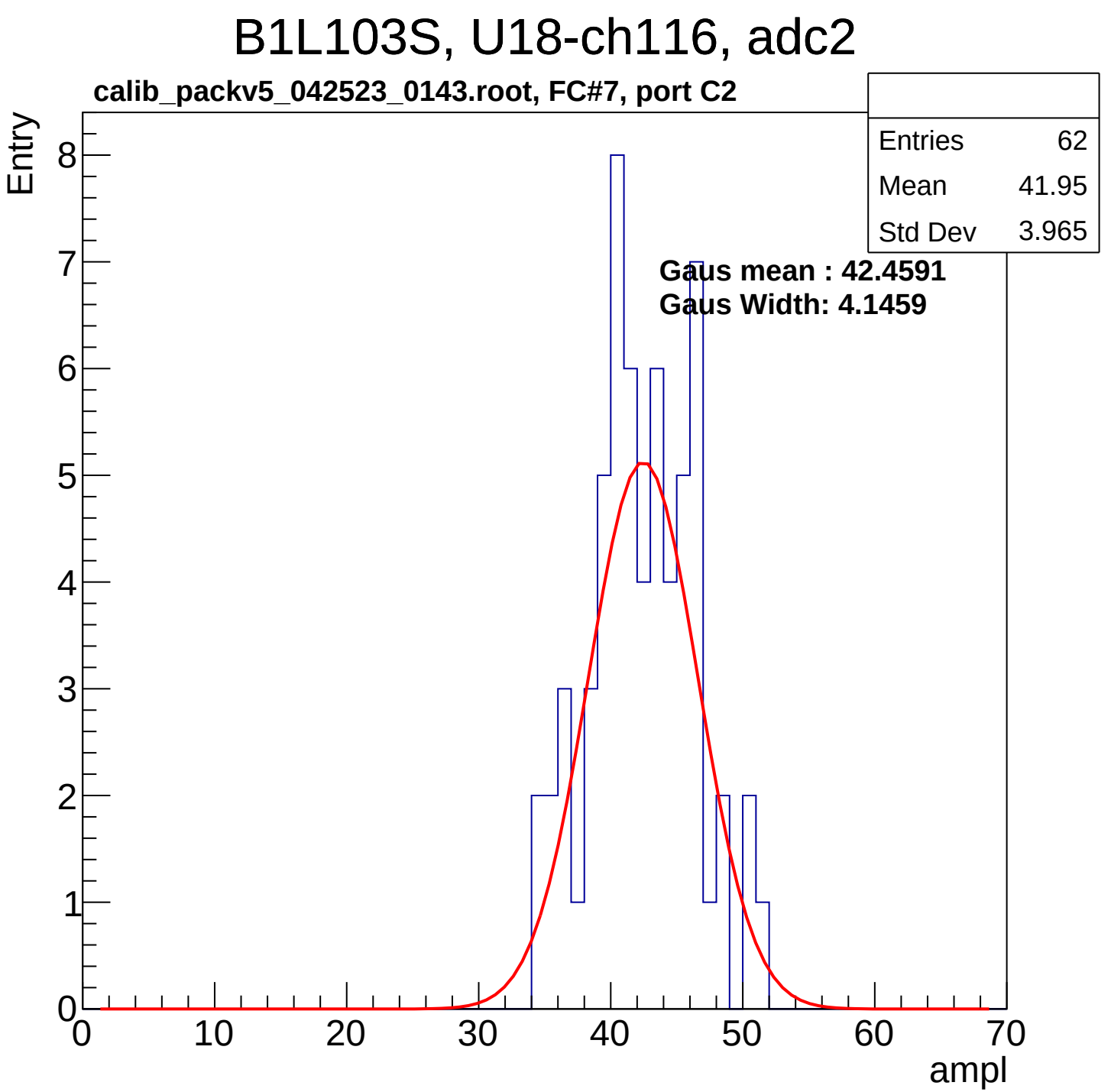
B1L103S, U18-ch116, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 62
Mean 41.95
Std Dev 3.965
Gaus mean : 42.4591
Gaus Width: 4.1459
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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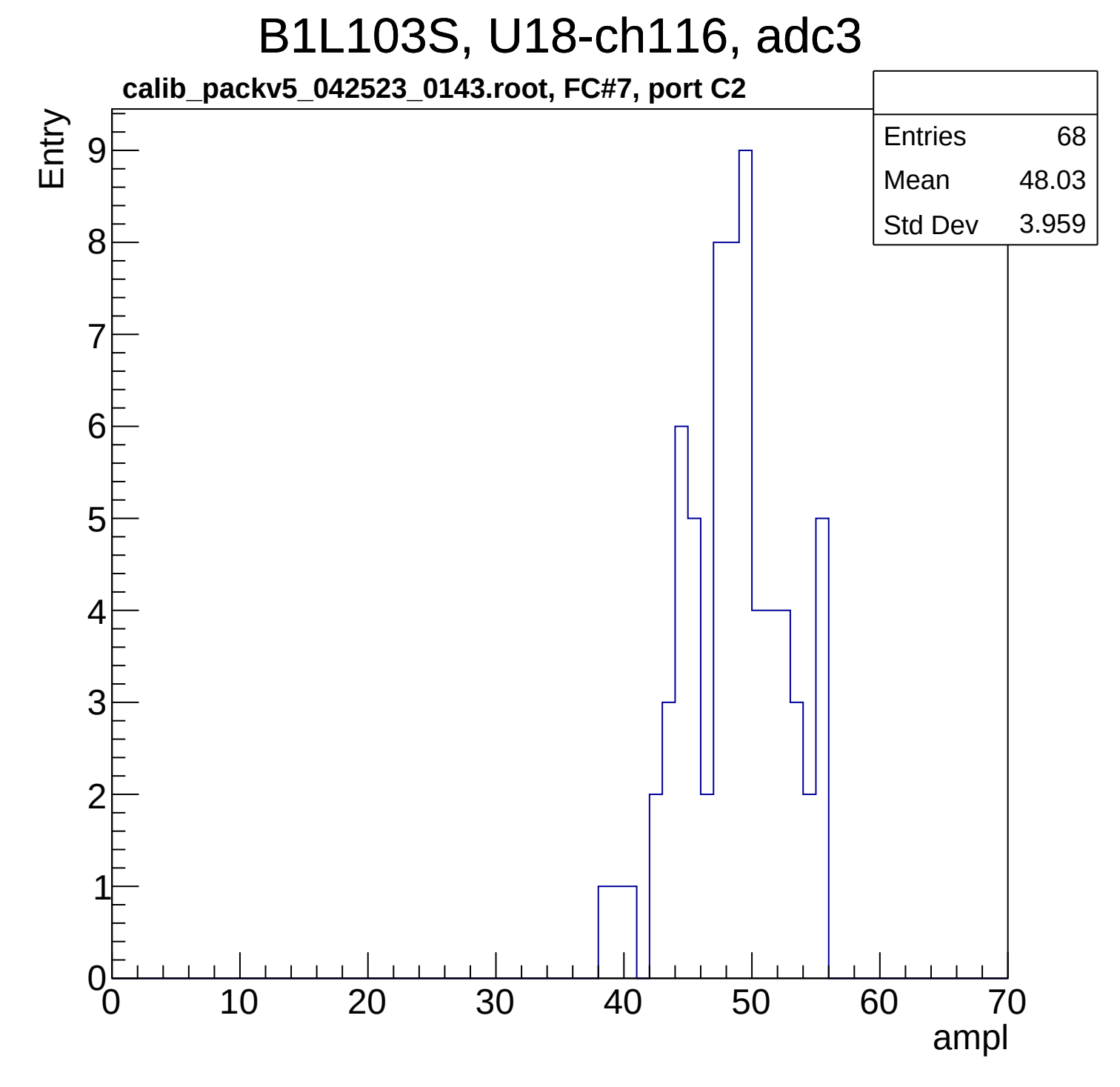
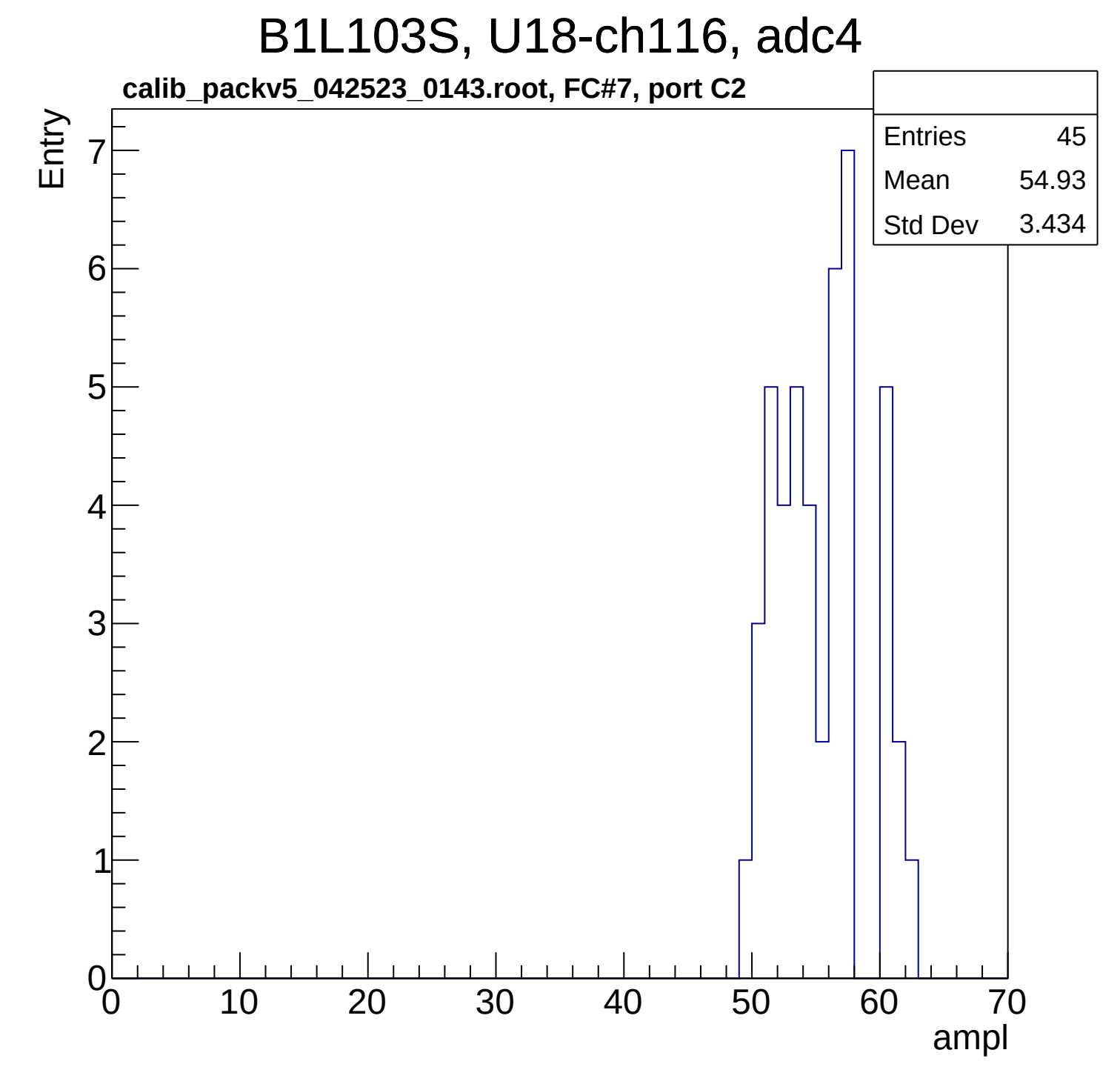
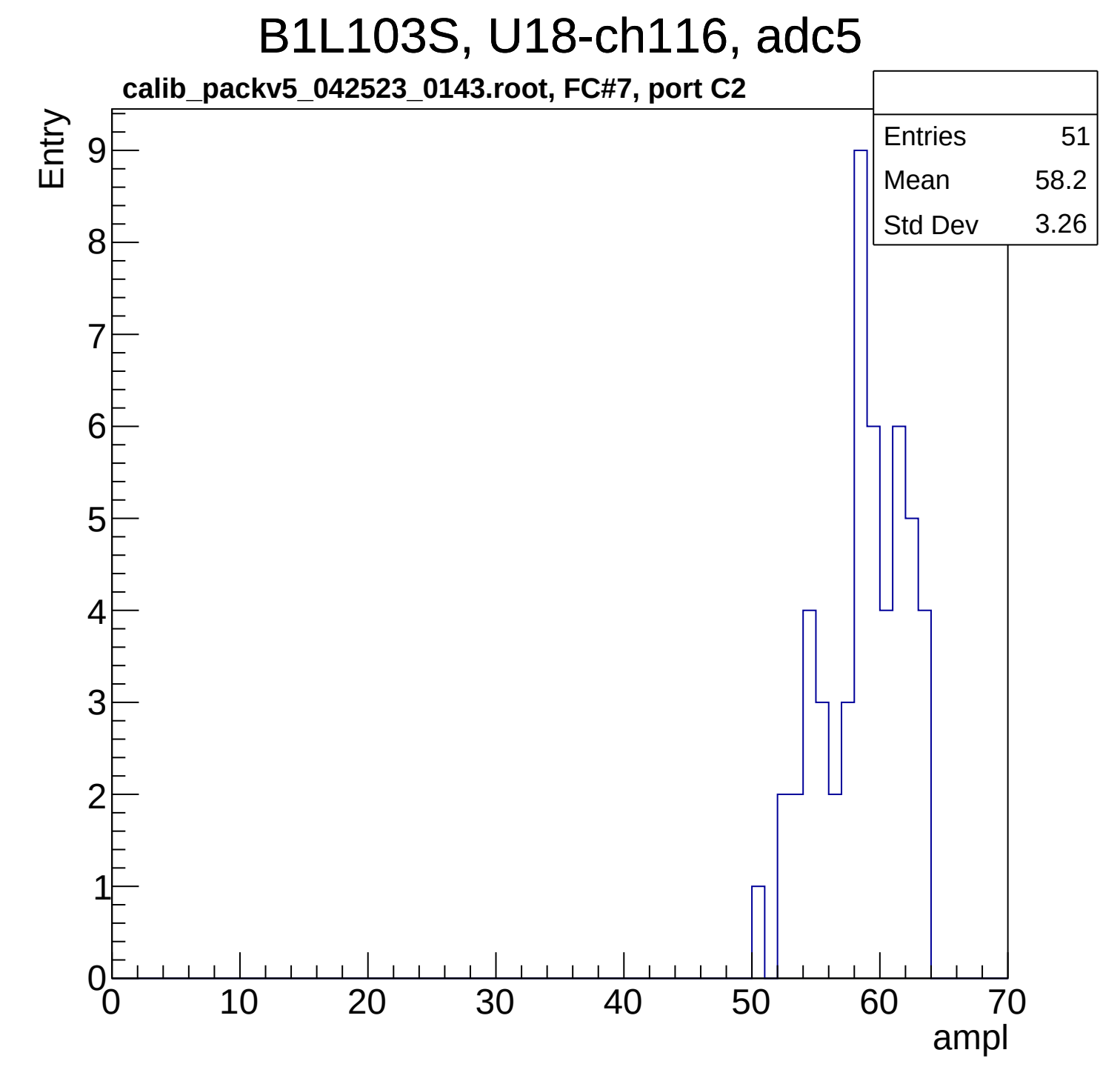

B1L103S, U18-ch116, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 48.03
Std Dev 3.959
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch116, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 45
Mean 54.93
Std Dev 3.434
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch116, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 51
Mean 58.2
Std Dev 3.26
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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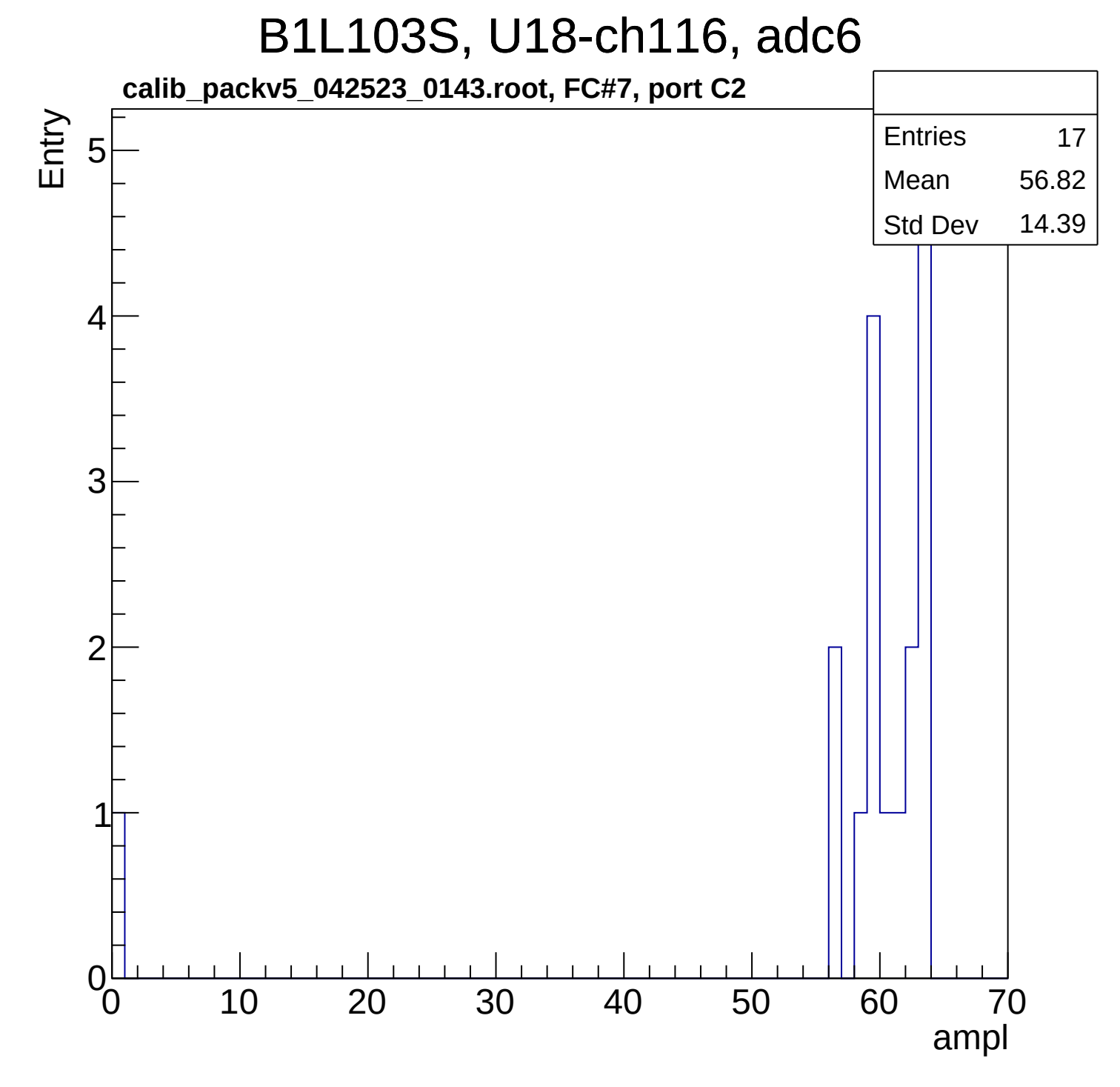
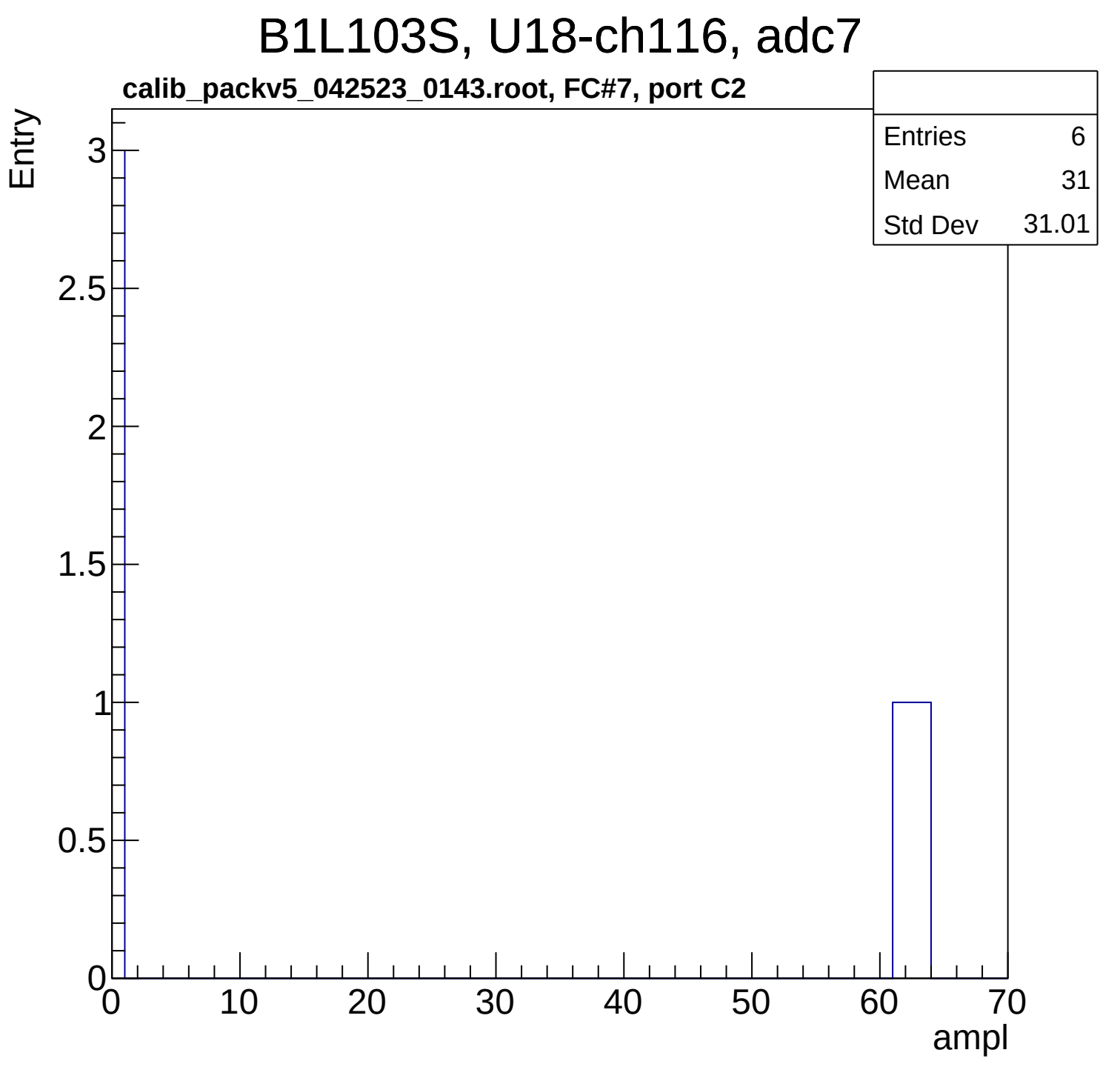
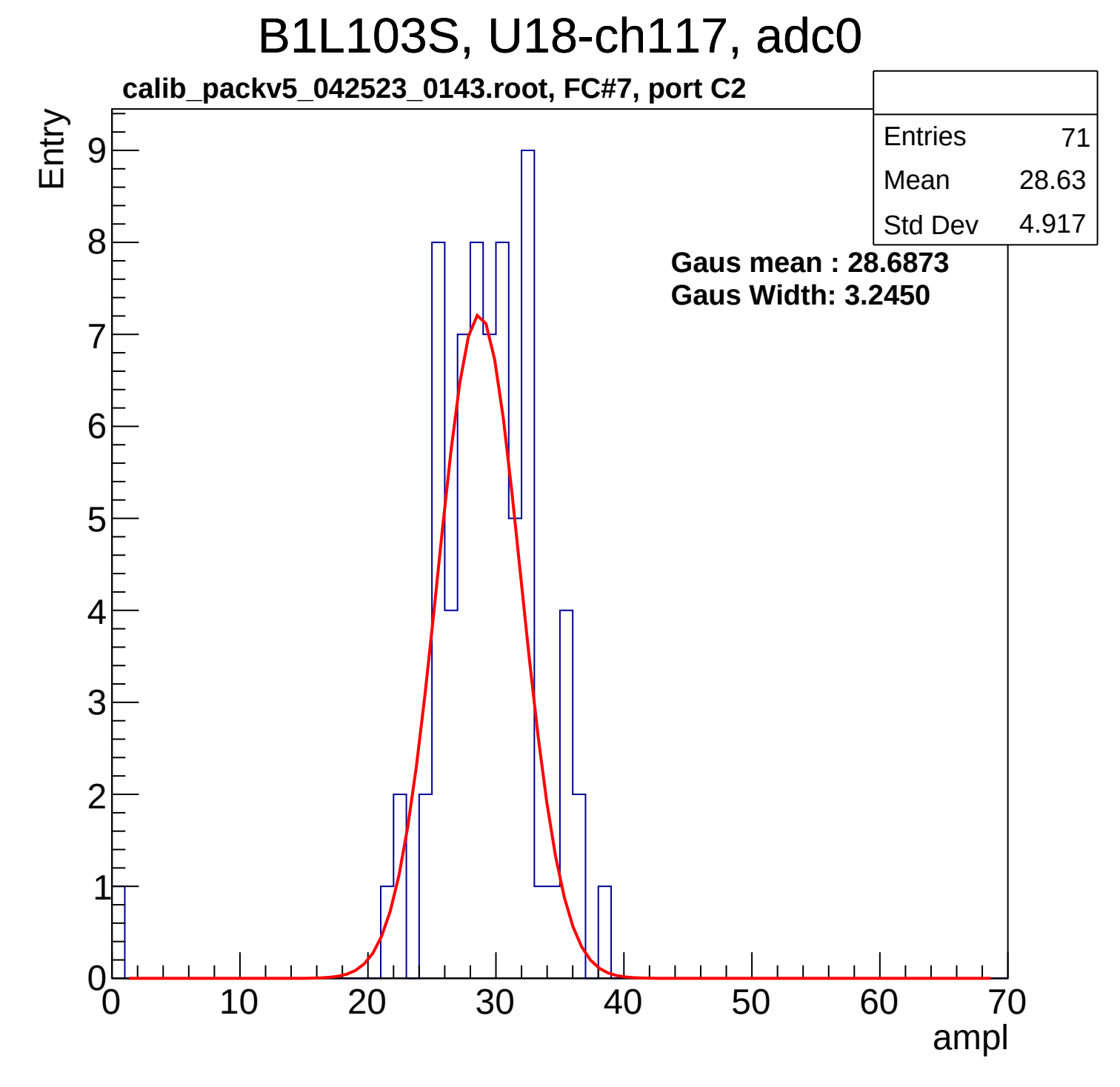
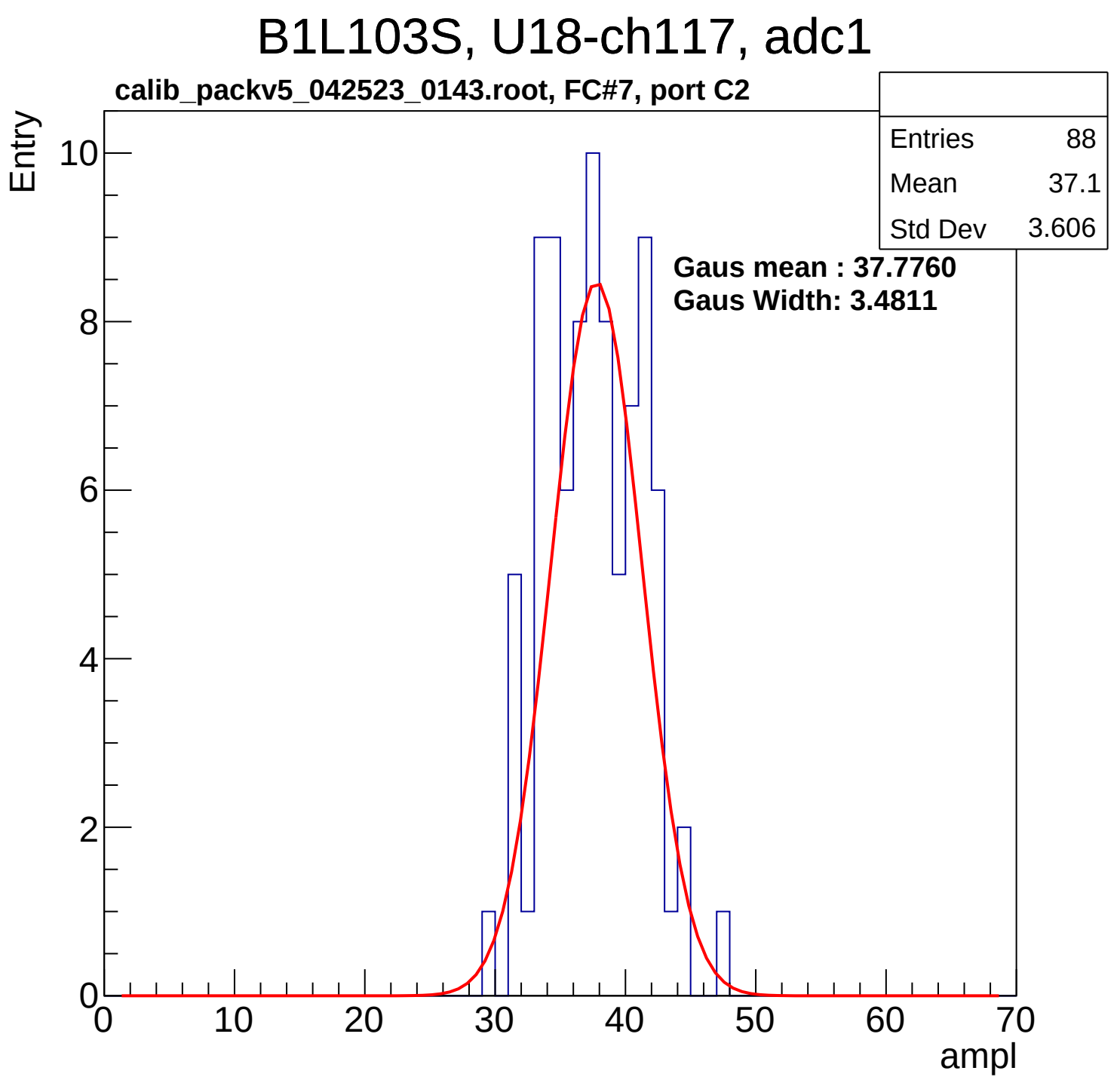
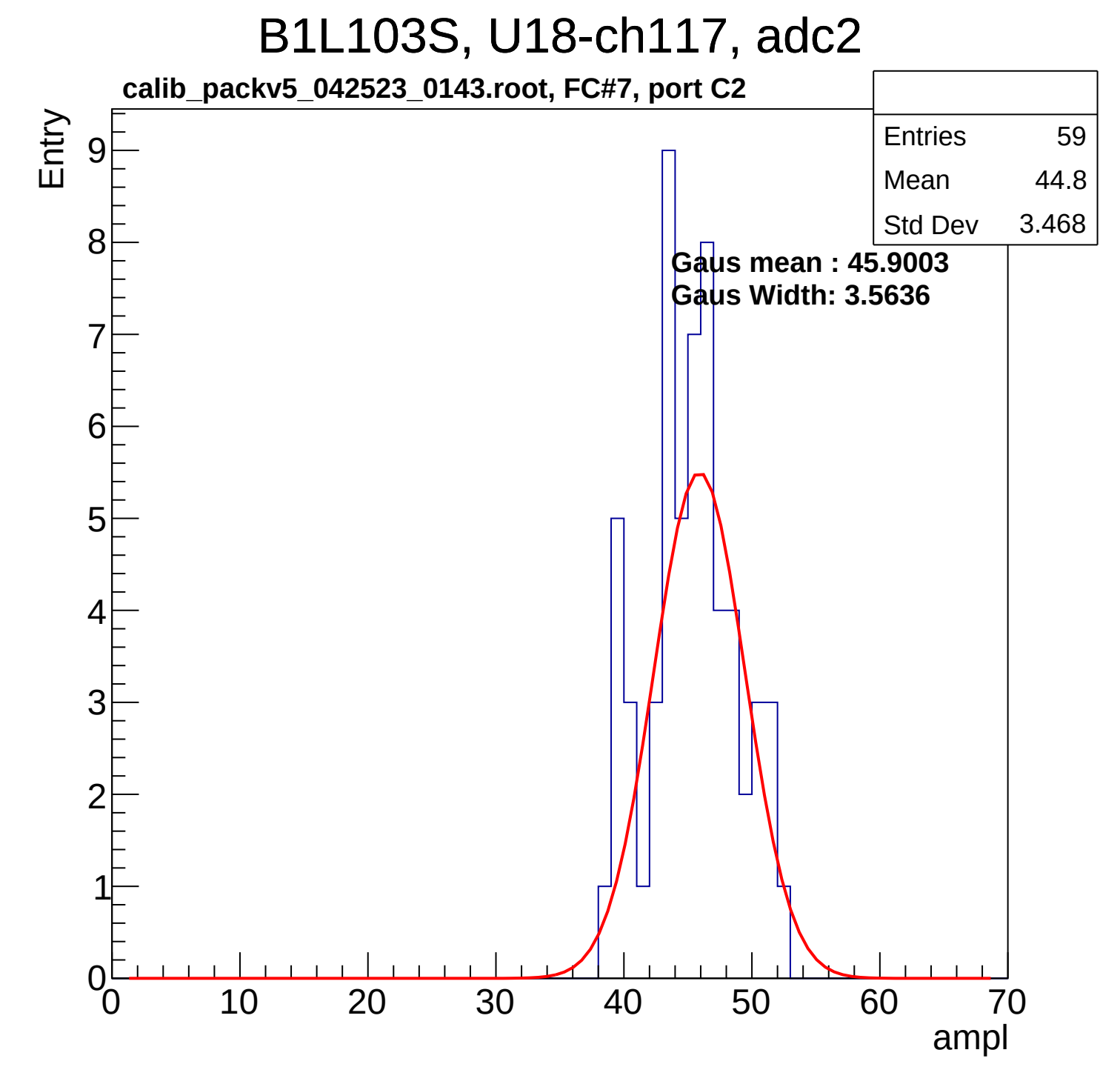
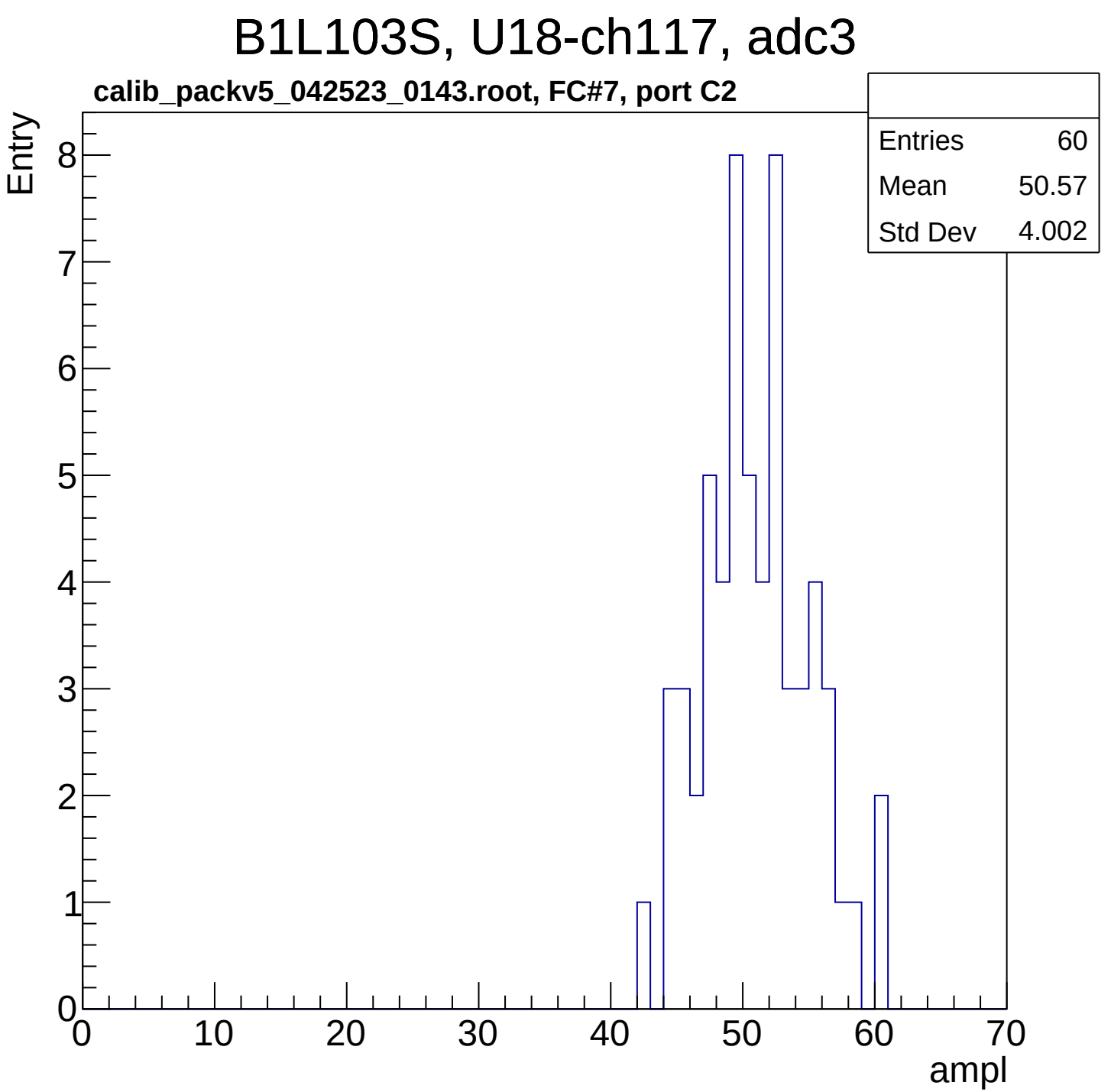

B1L103S, U18-ch116, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 17
Mean 56.82
Std Dev 14.39
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

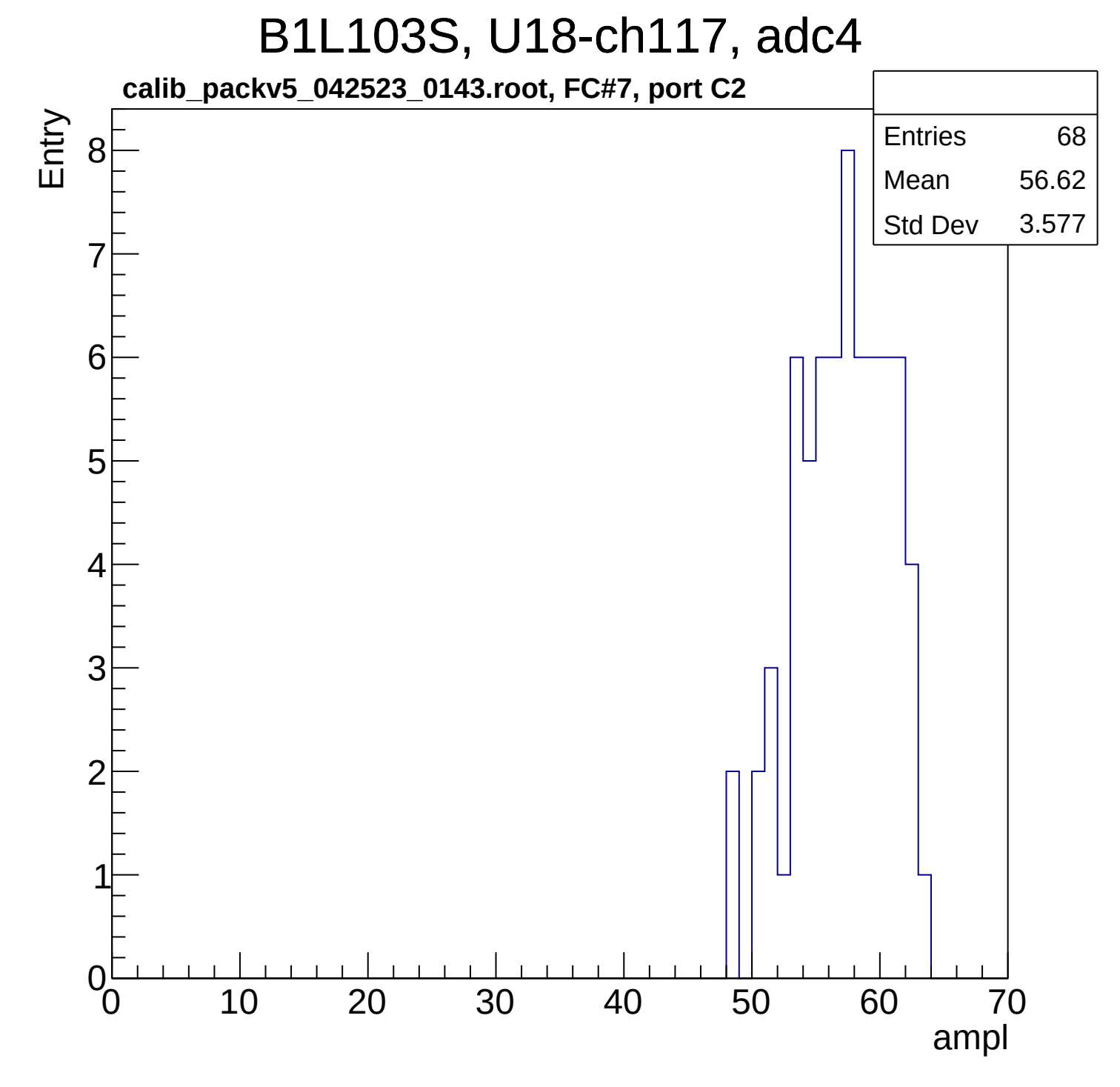

B1L103S, U18-ch116, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 6
Mean 31
Std Dev 31.01
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

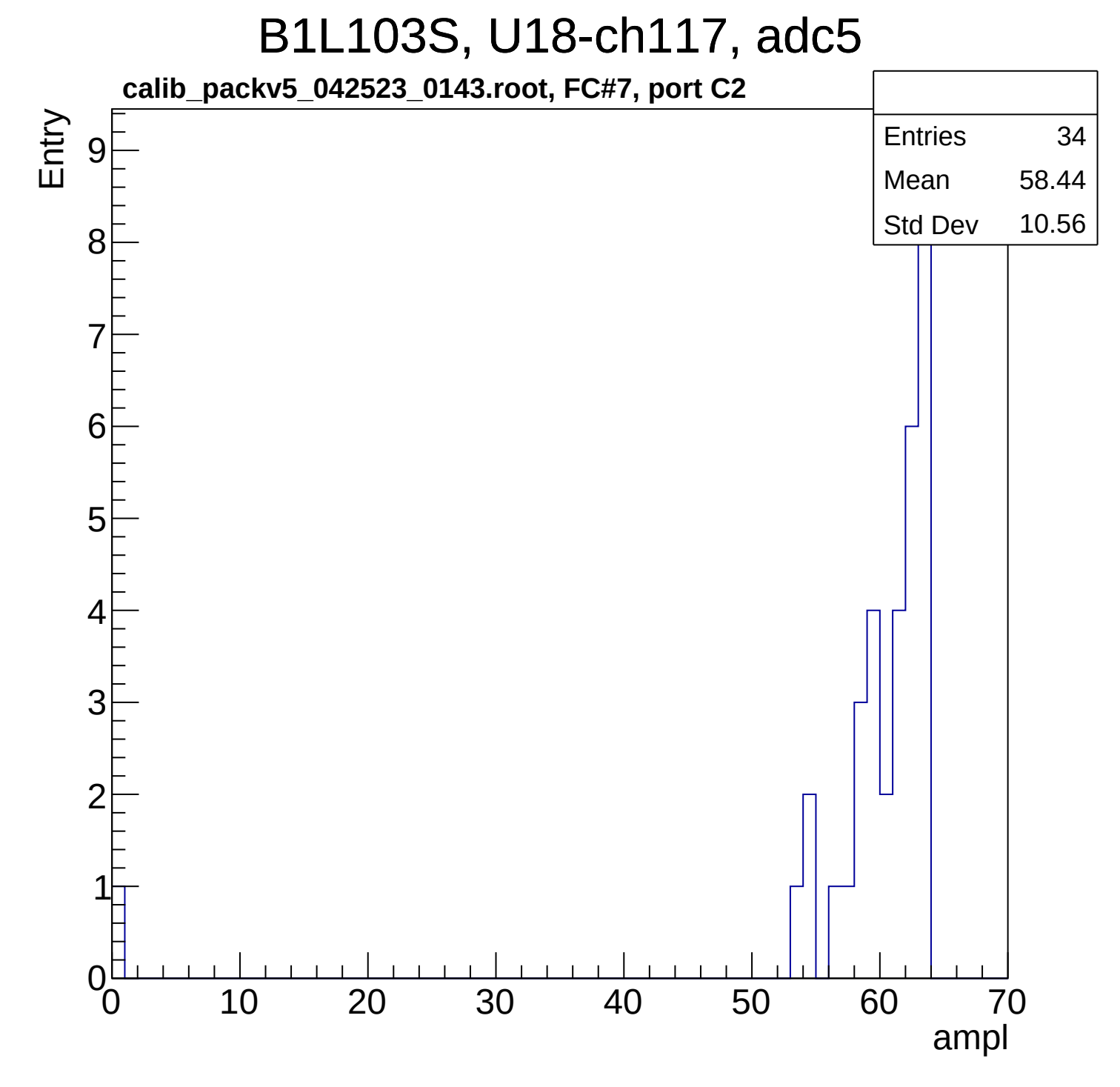

B1L103S, U18-ch117, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 71
Mean 28.63
Std Dev 4.917
Gaus mean : 28.6873
Gaus Width: 3.2450
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

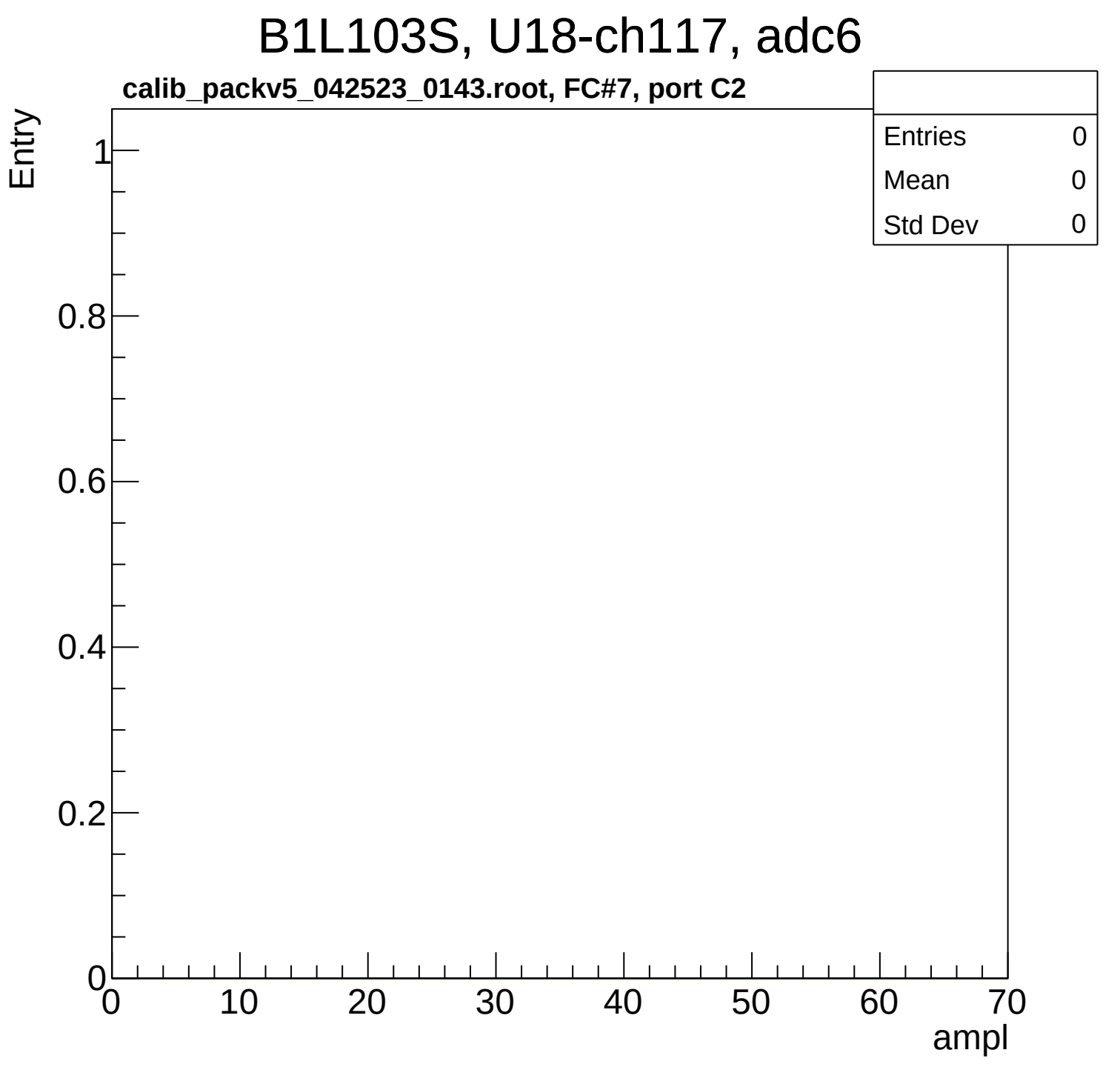

B1L103S, U18-ch117, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 88
Mean 37.1
Std Dev 3.606
Gaus mean : 37.7760
Gaus Width: 3.4811
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

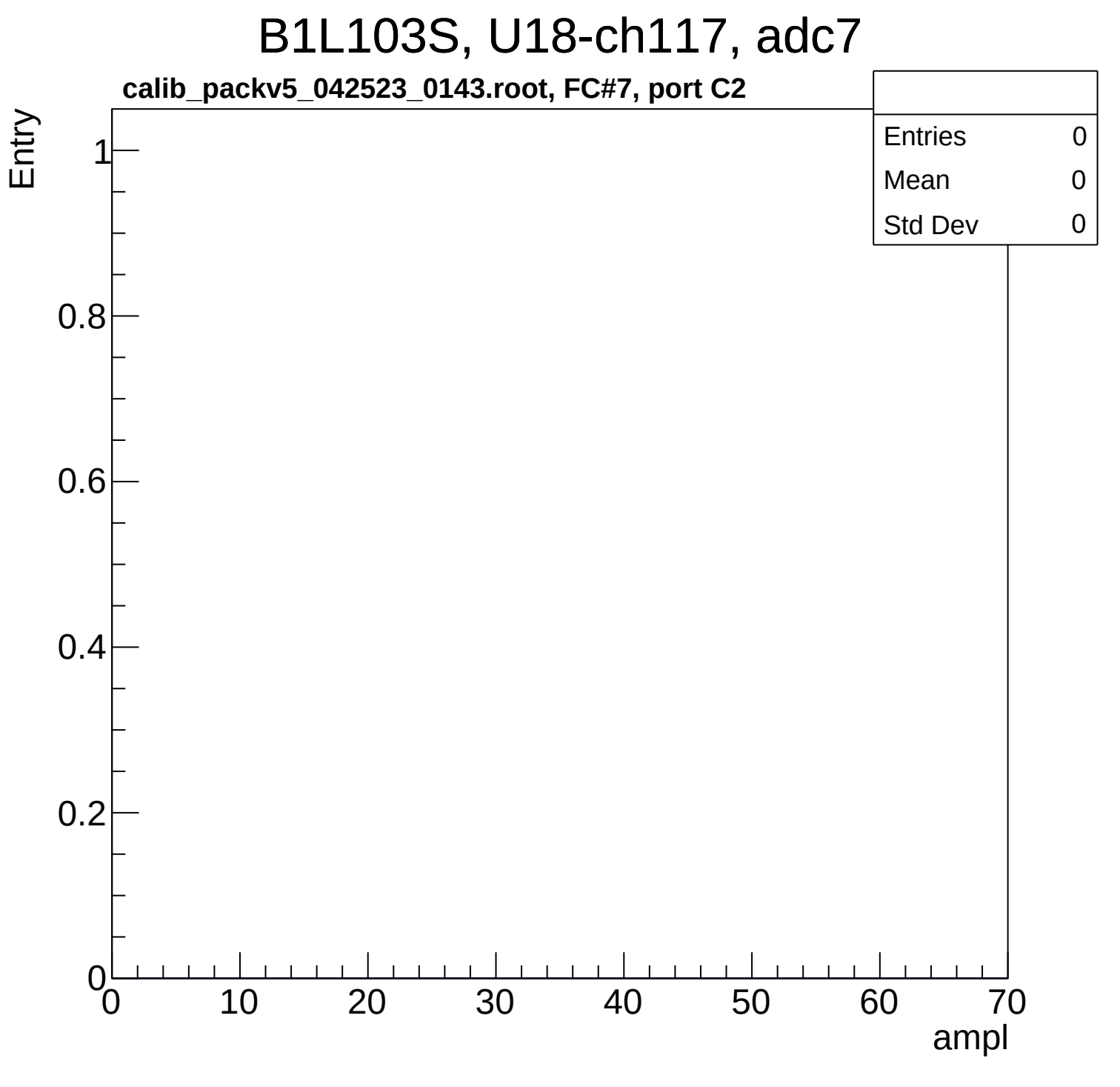

B1L103S, U18-ch117, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 44.8
Std Dev 3.468
Gaus mean : 45.9003
Gaus Width: 3.5636
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

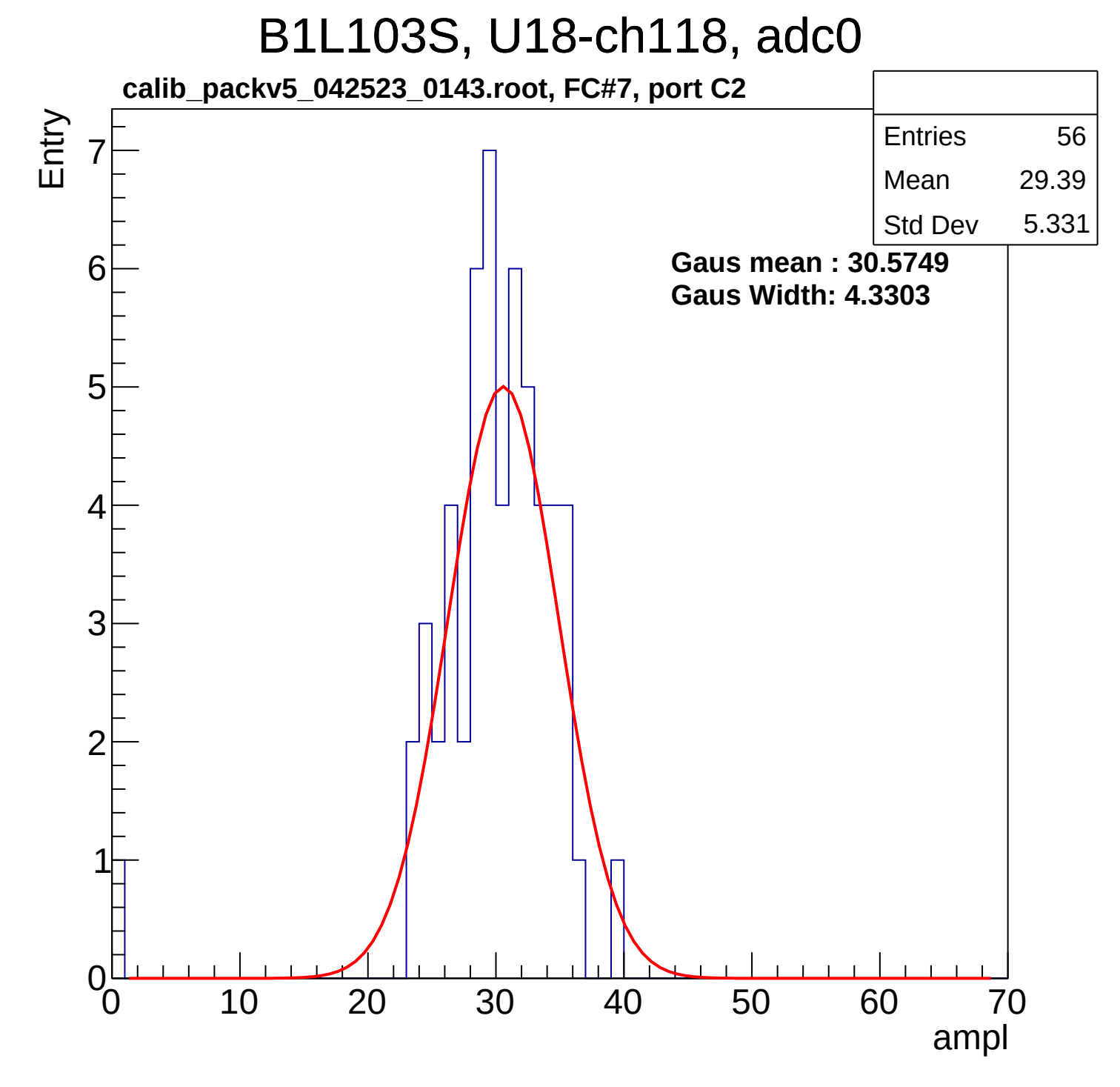

B1L103S, U18-ch117, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 60
Mean 50.57
Std Dev 4.002
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

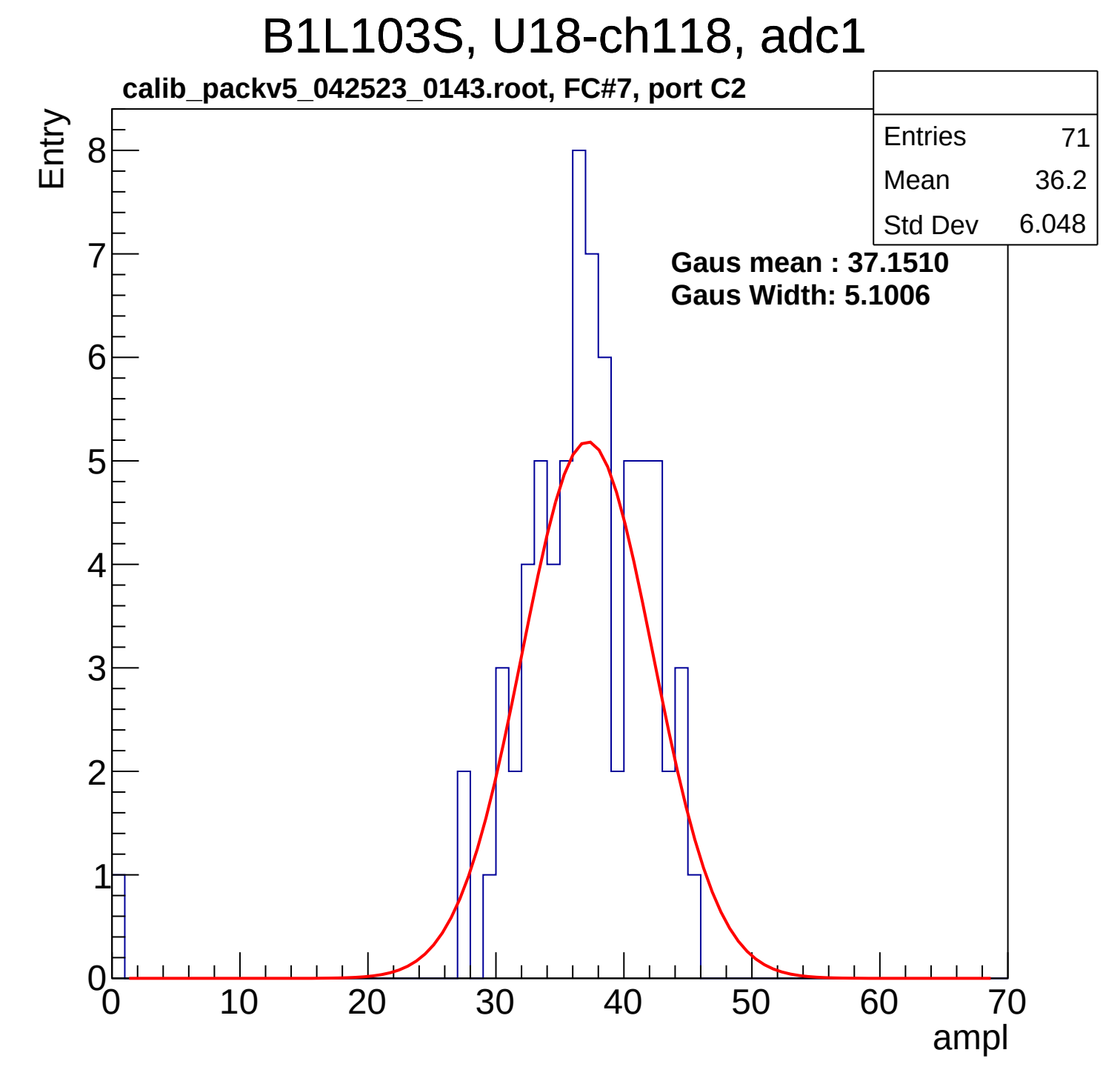

B1L103S, U18-ch117, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 56.62
Std Dev 3.577
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

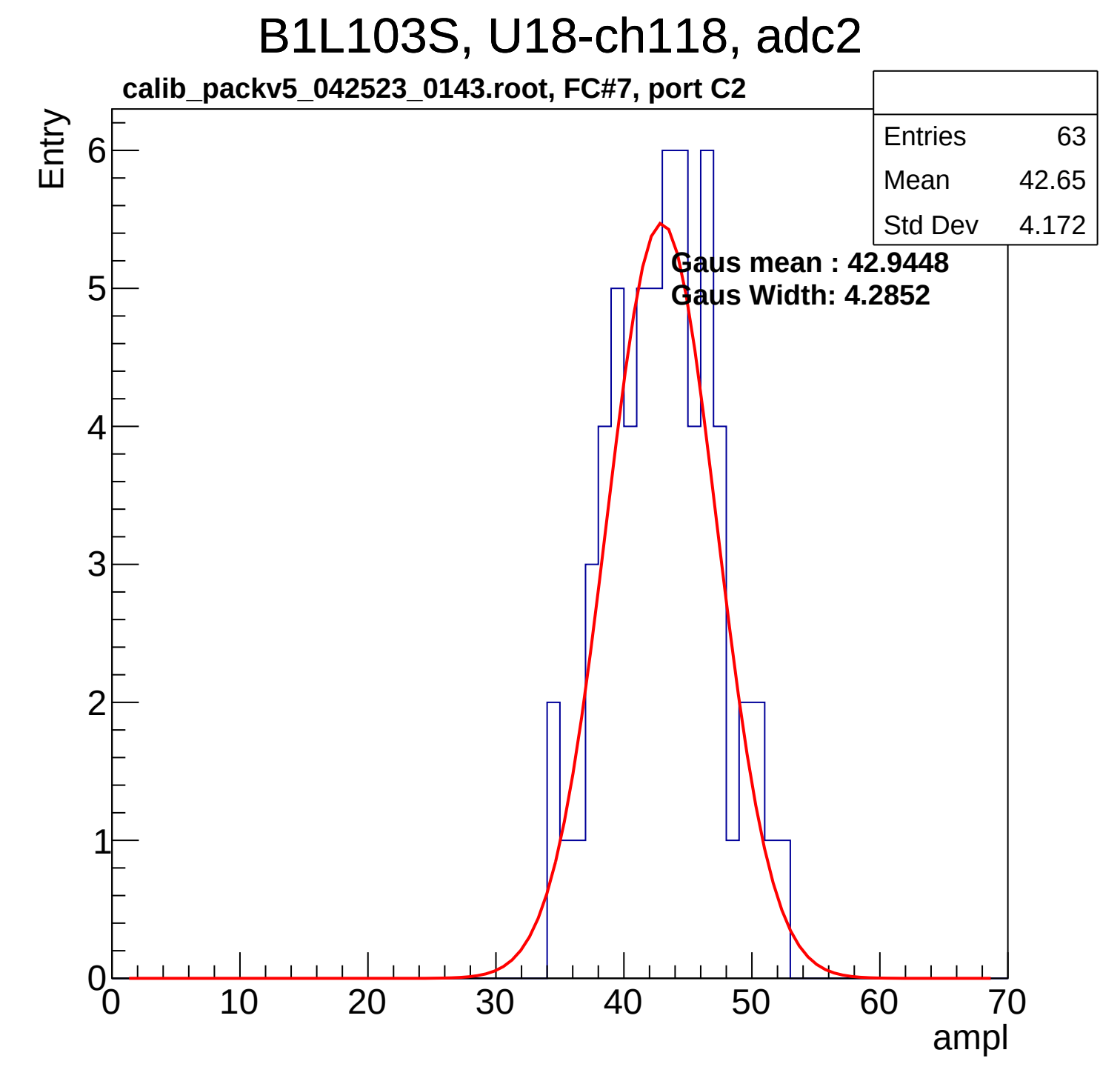

B1L103S, U18-ch117, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 34
Mean 58.44
Std Dev 10.56
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

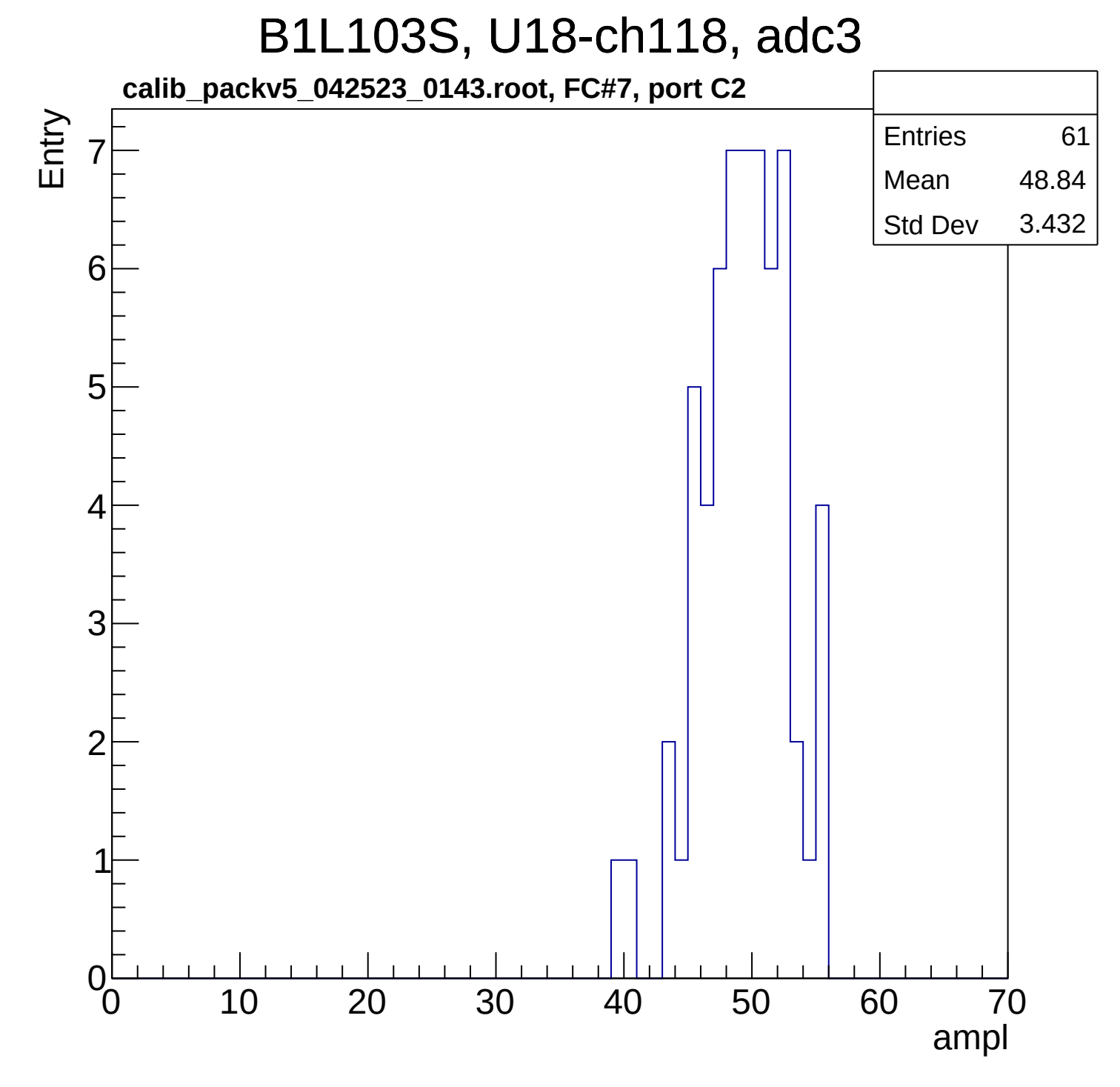

B1L103S, U18-ch117, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

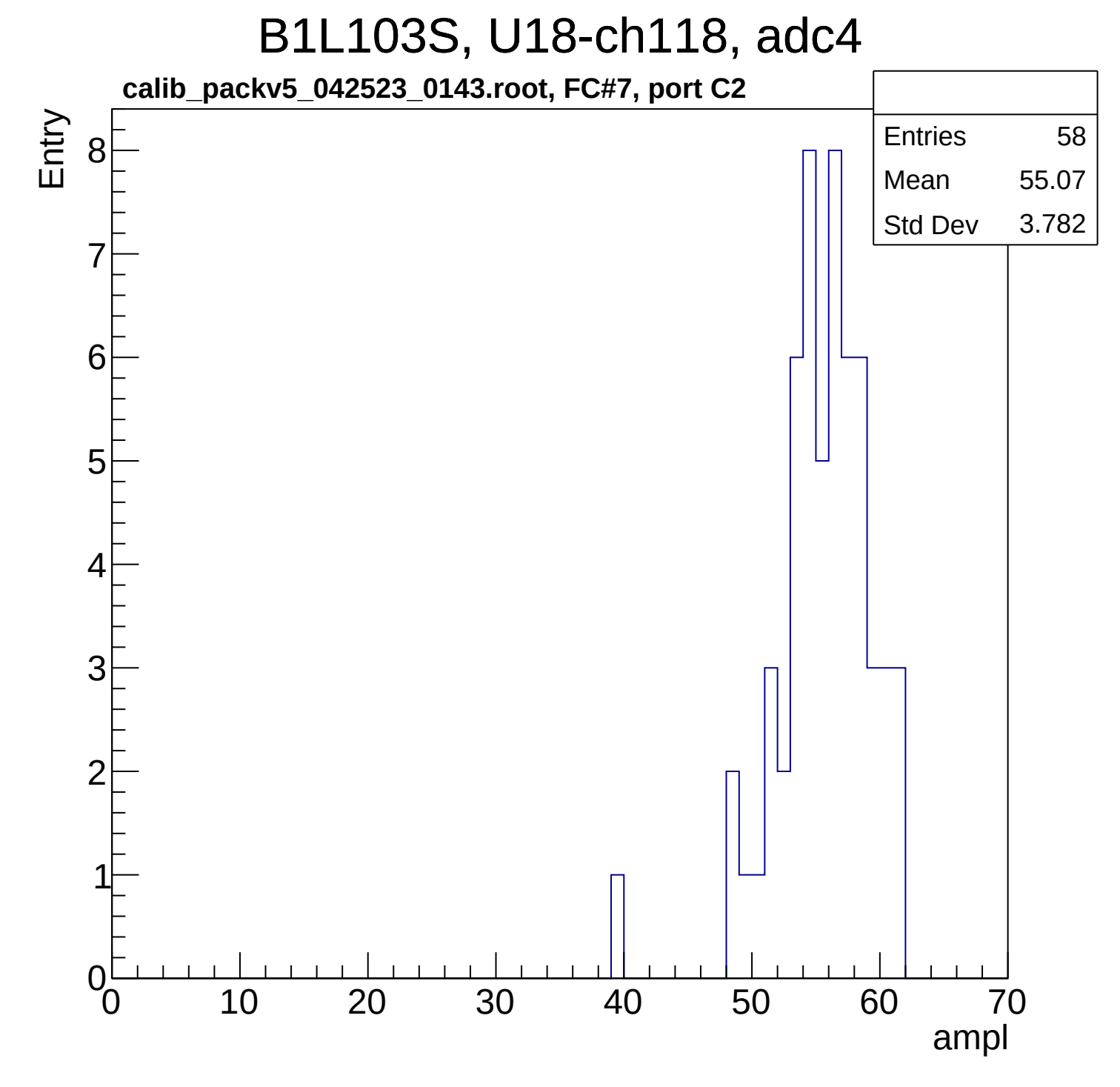

B1L103S, U18-ch117, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch118, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 29.39
Std Dev 5.331
Gaus mean : 30.5749
Gaus Width: 4.3303
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch118, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 71
Mean 36.2
Std Dev 6.048
Gaus mean : 37.1510
Gaus Width: 5.1006
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch118, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 42.65
Std Dev 4.172
Gaus mean : 42.9448
Gaus Width: 4.2852
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U18-ch118, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 61
Mean 48.84
Std Dev 3.432
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch118, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 58
Mean 55.07
Std Dev 3.782
Entry
ampl
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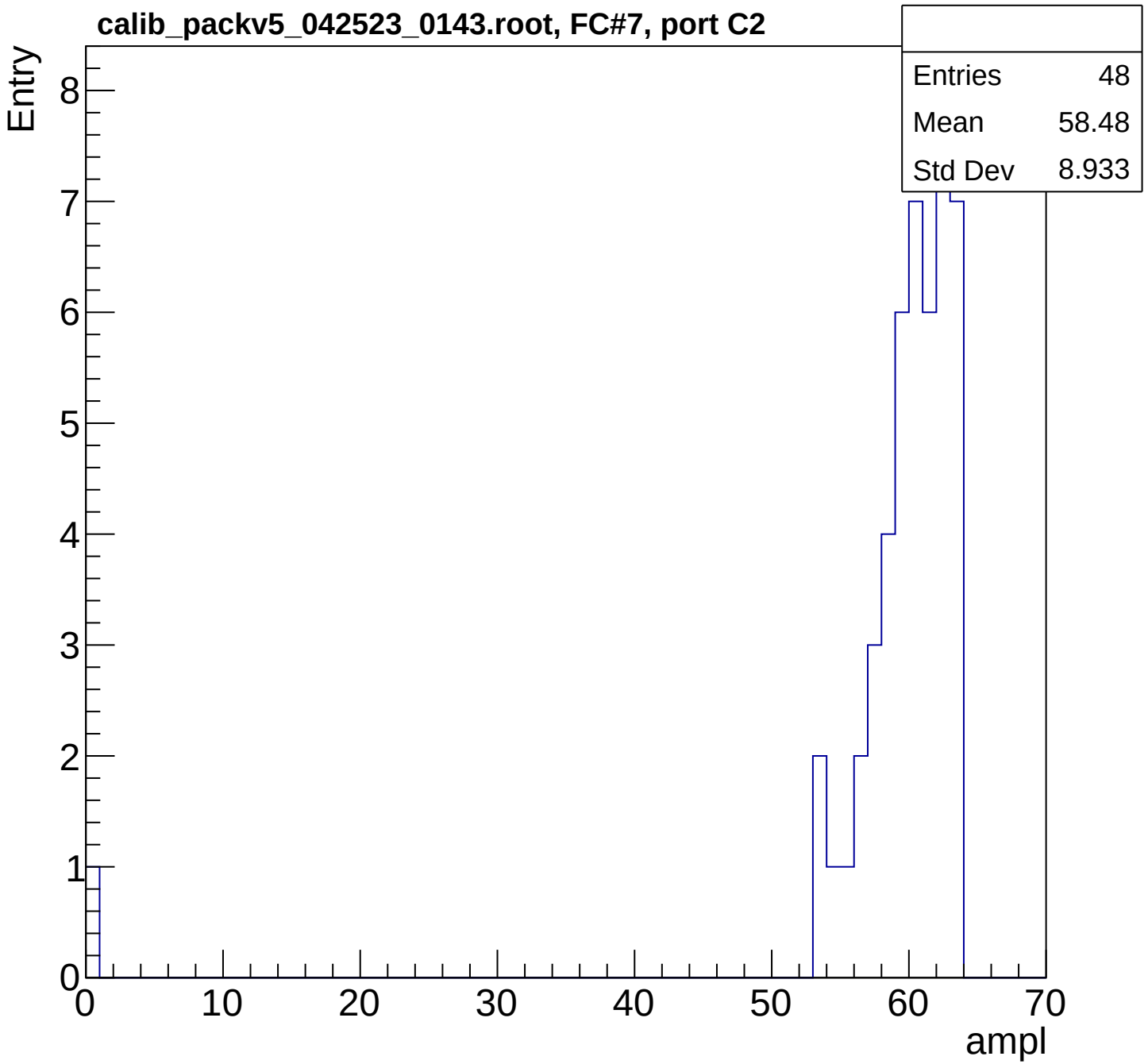
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch118, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 48
Mean 58.48
Std Dev 8.933
Entry
ampl
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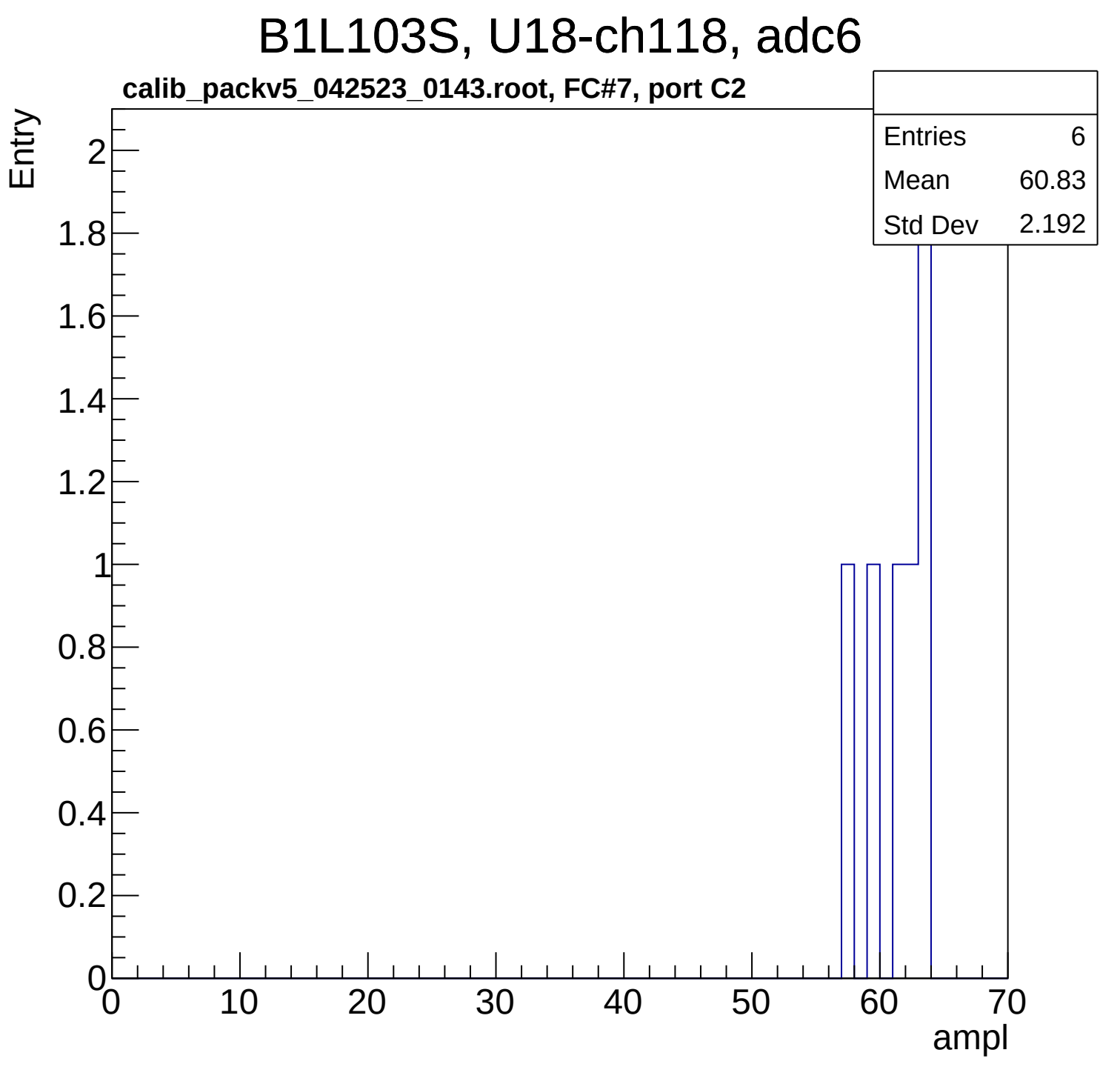
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch118, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 6
Mean 60.83
Std Dev 2.192
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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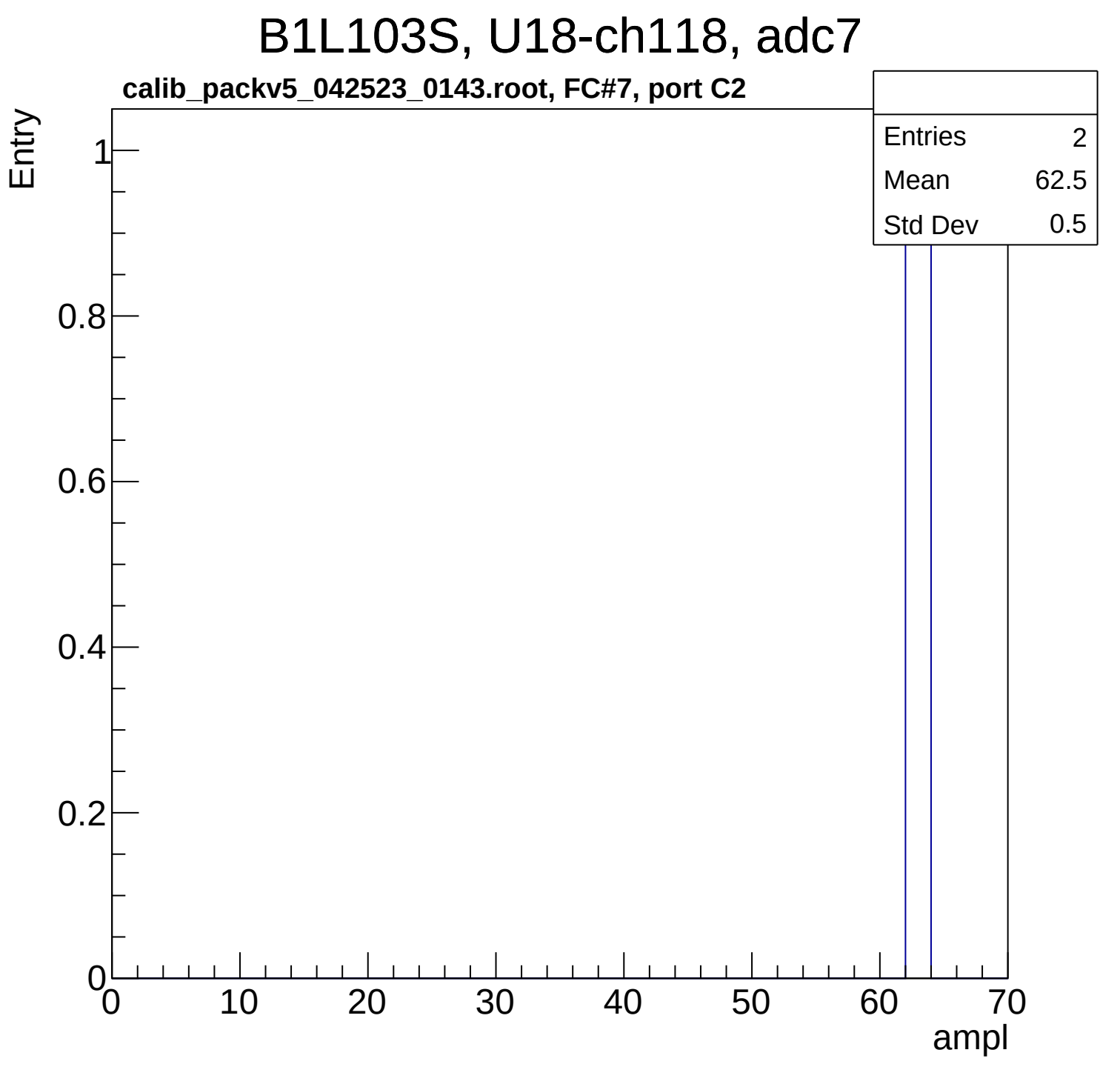
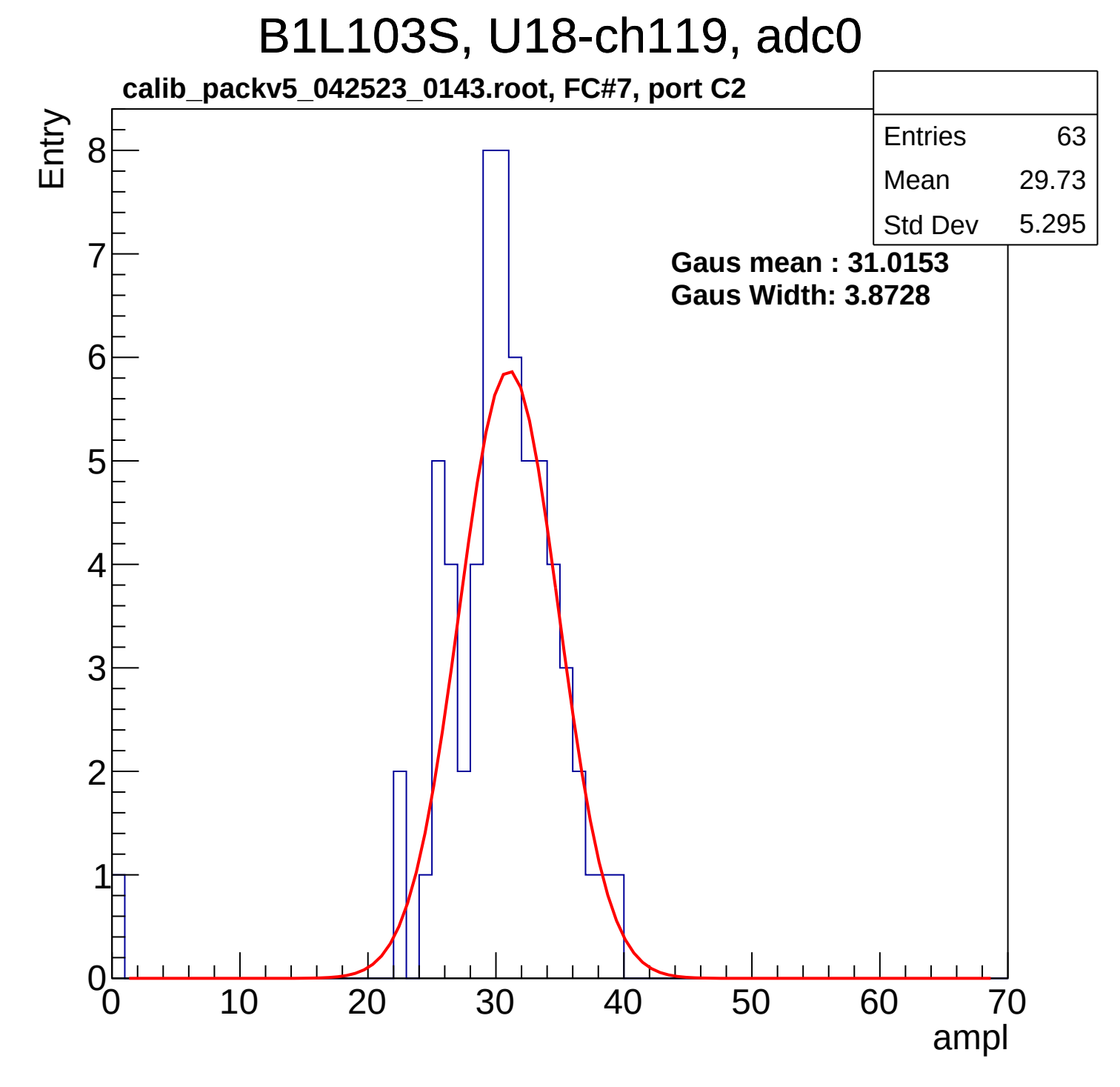

B1L103S, U18-ch118, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch119, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 29.73
Std Dev 5.295
Gaus mean : 31.0153
Gaus Width: 3.8728
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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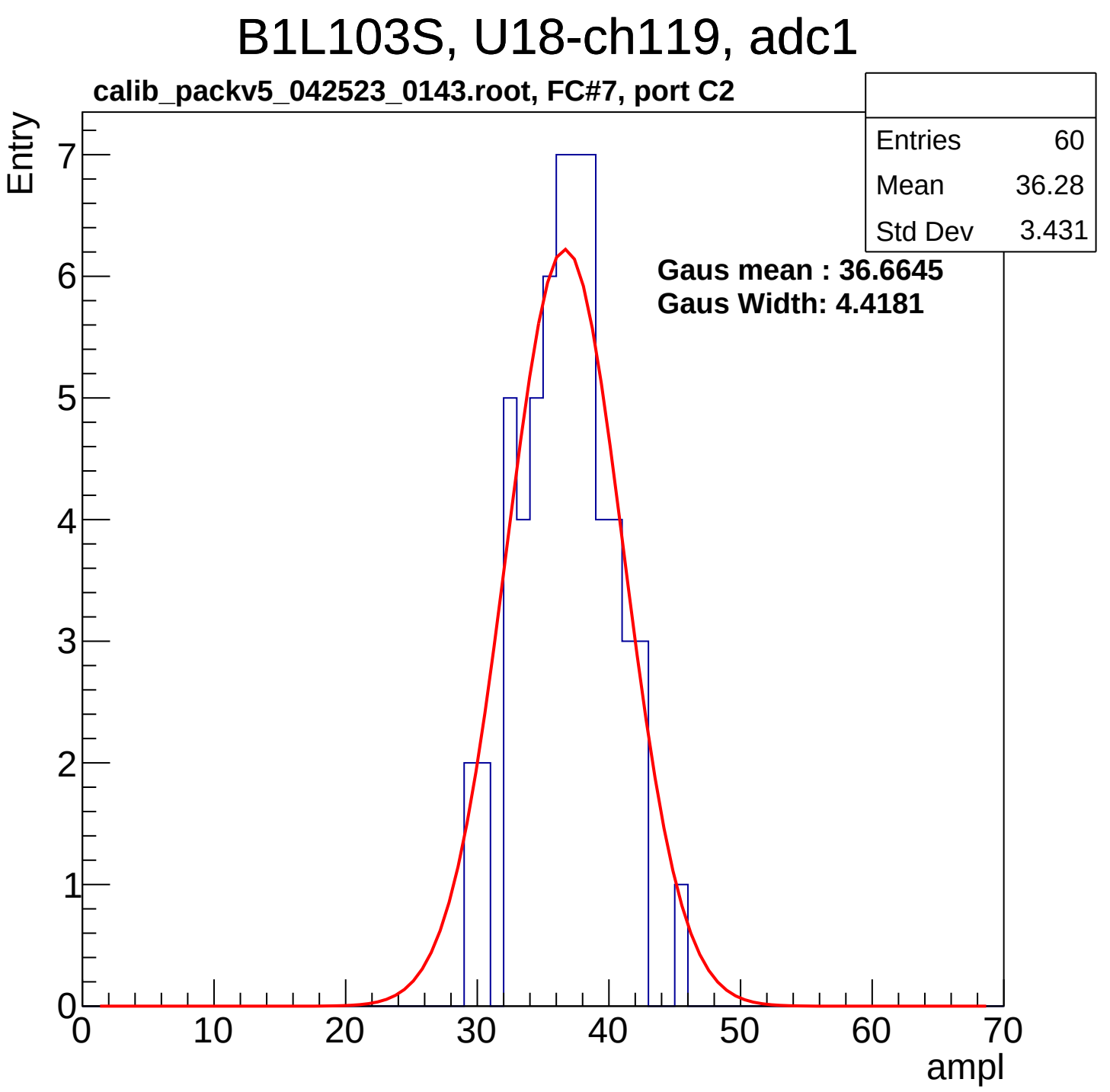
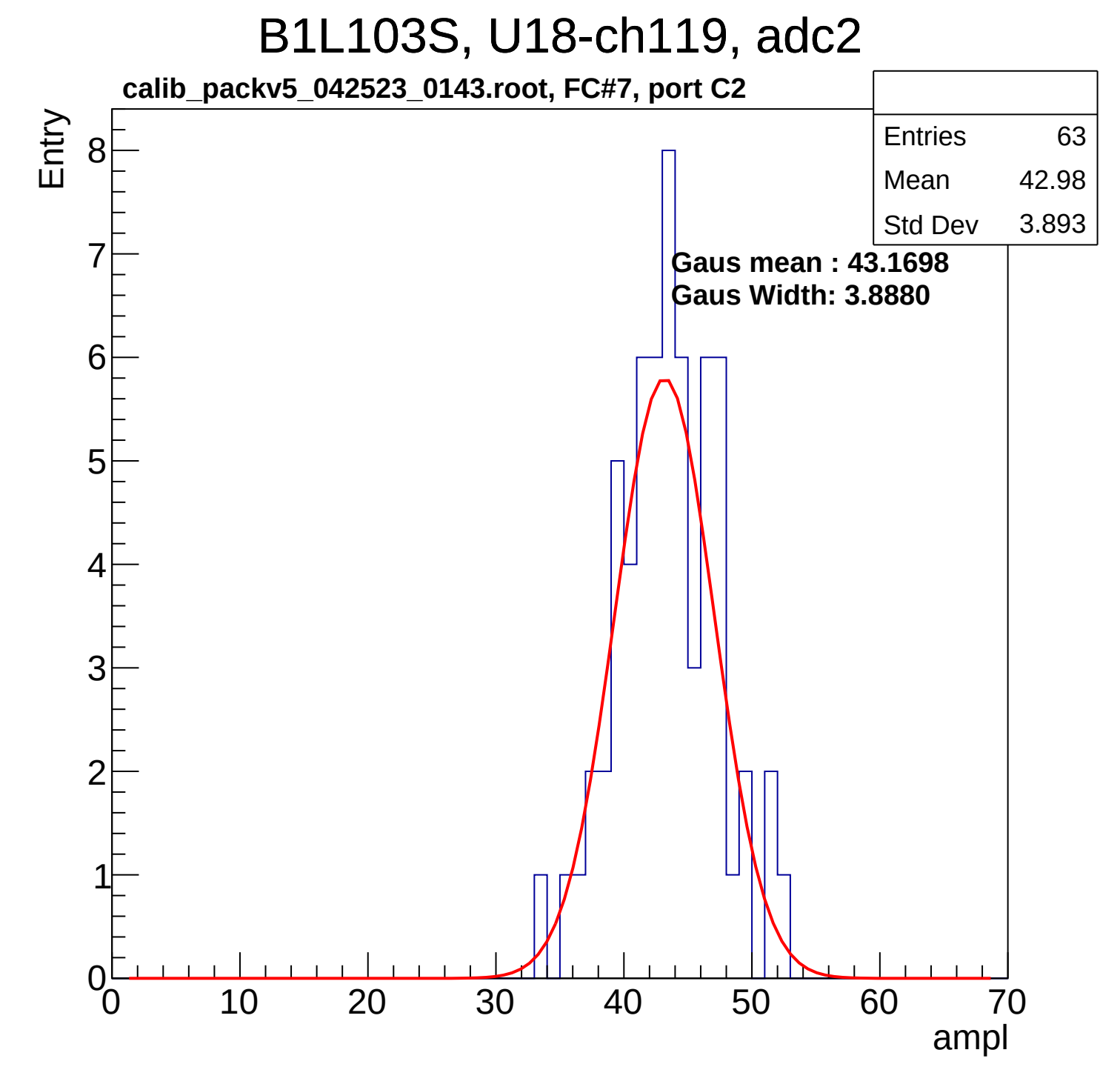

B1L103S, U18-ch119, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 60
Mean 36.28
Std Dev 3.431
Gaus mean : 36.6645
Gaus Width: 4.4181
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch119, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 42.98
Std Dev 3.893
Gaus mean : 43.1698
Gaus Width: 3.8880
Entry
ampl
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1
2
3
4
5
6
7
8
0
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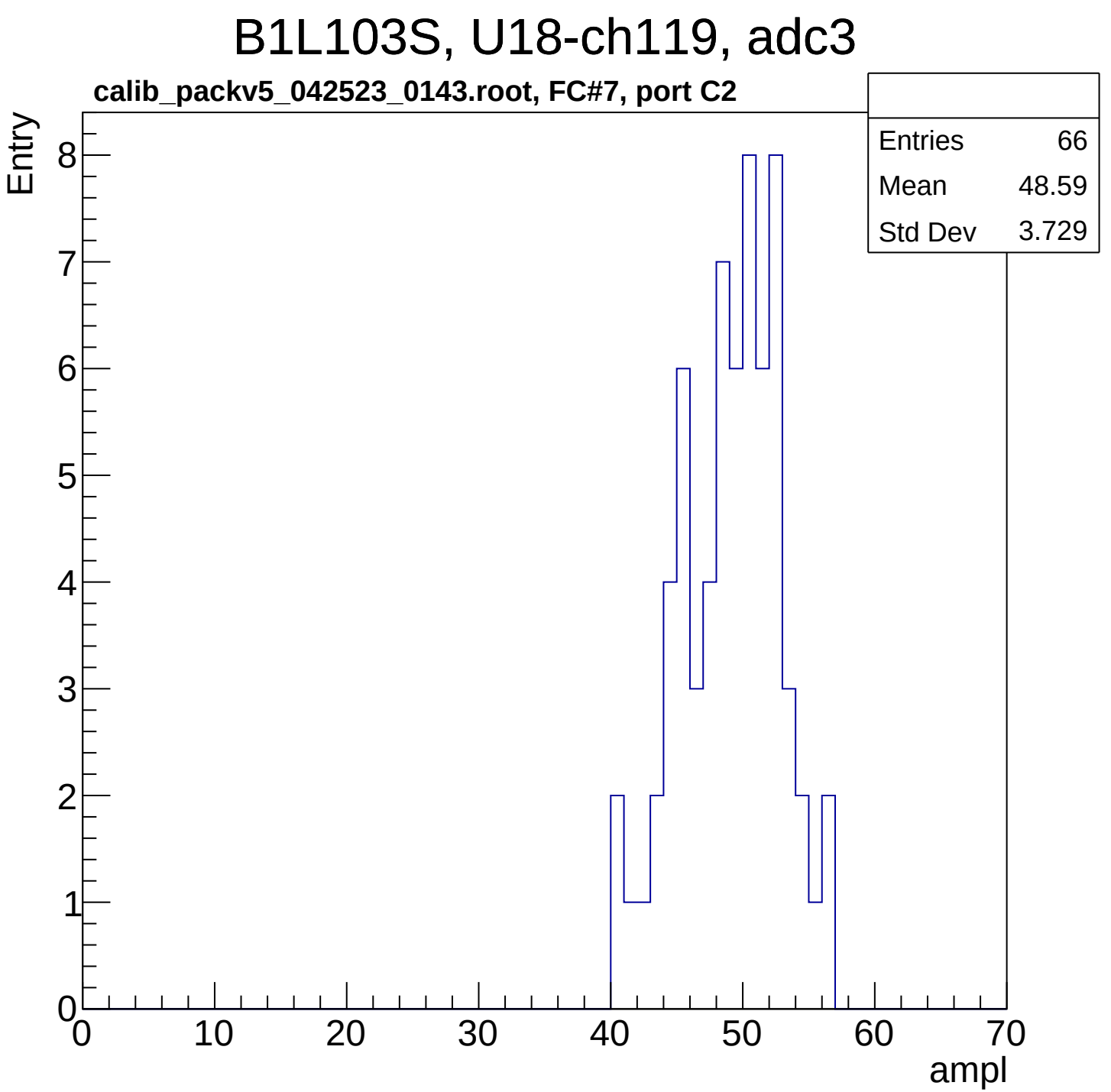
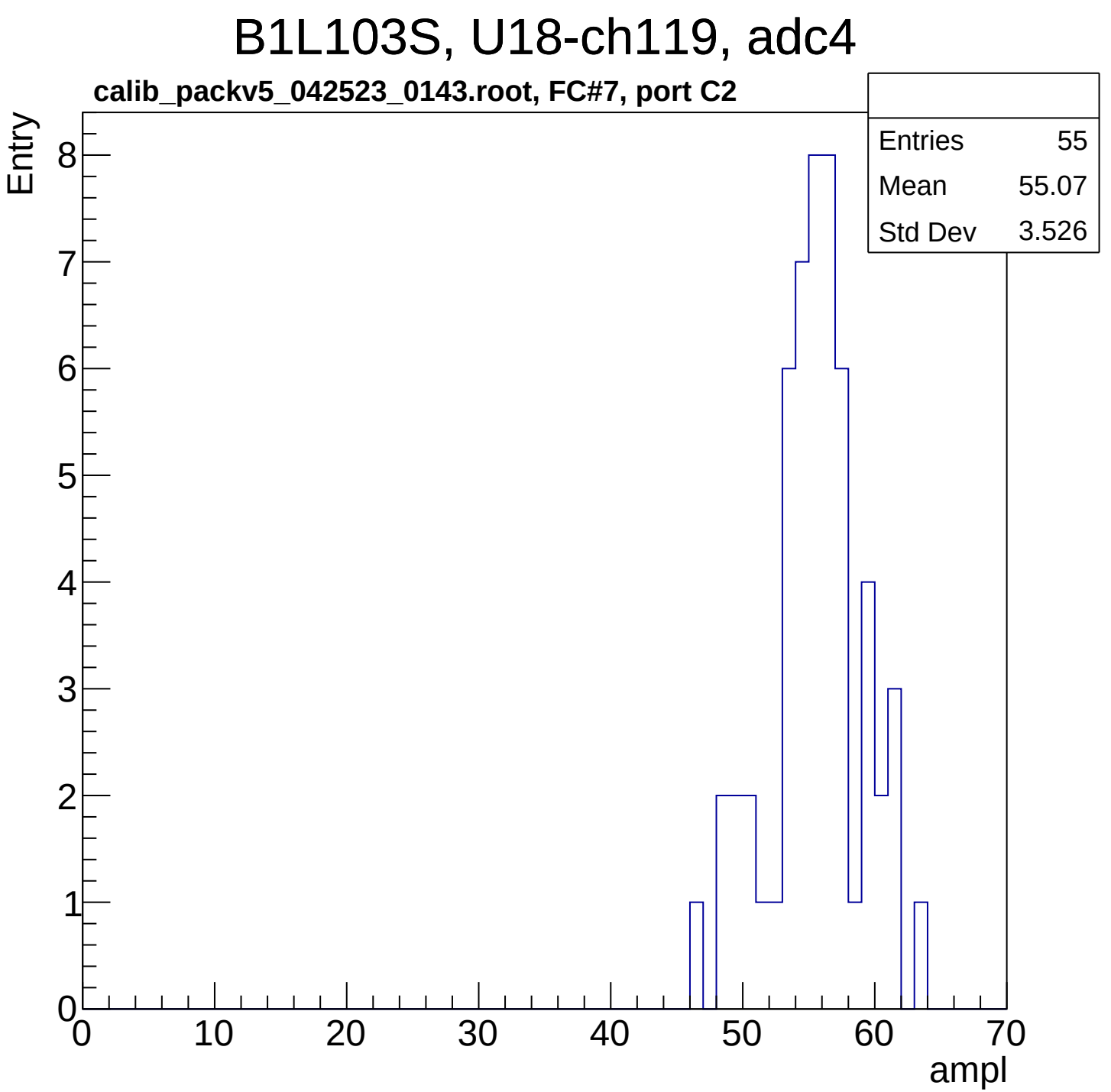

B1L103S, U18-ch119, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 48.59
Std Dev 3.729
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch119, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 55.07
Std Dev 3.526
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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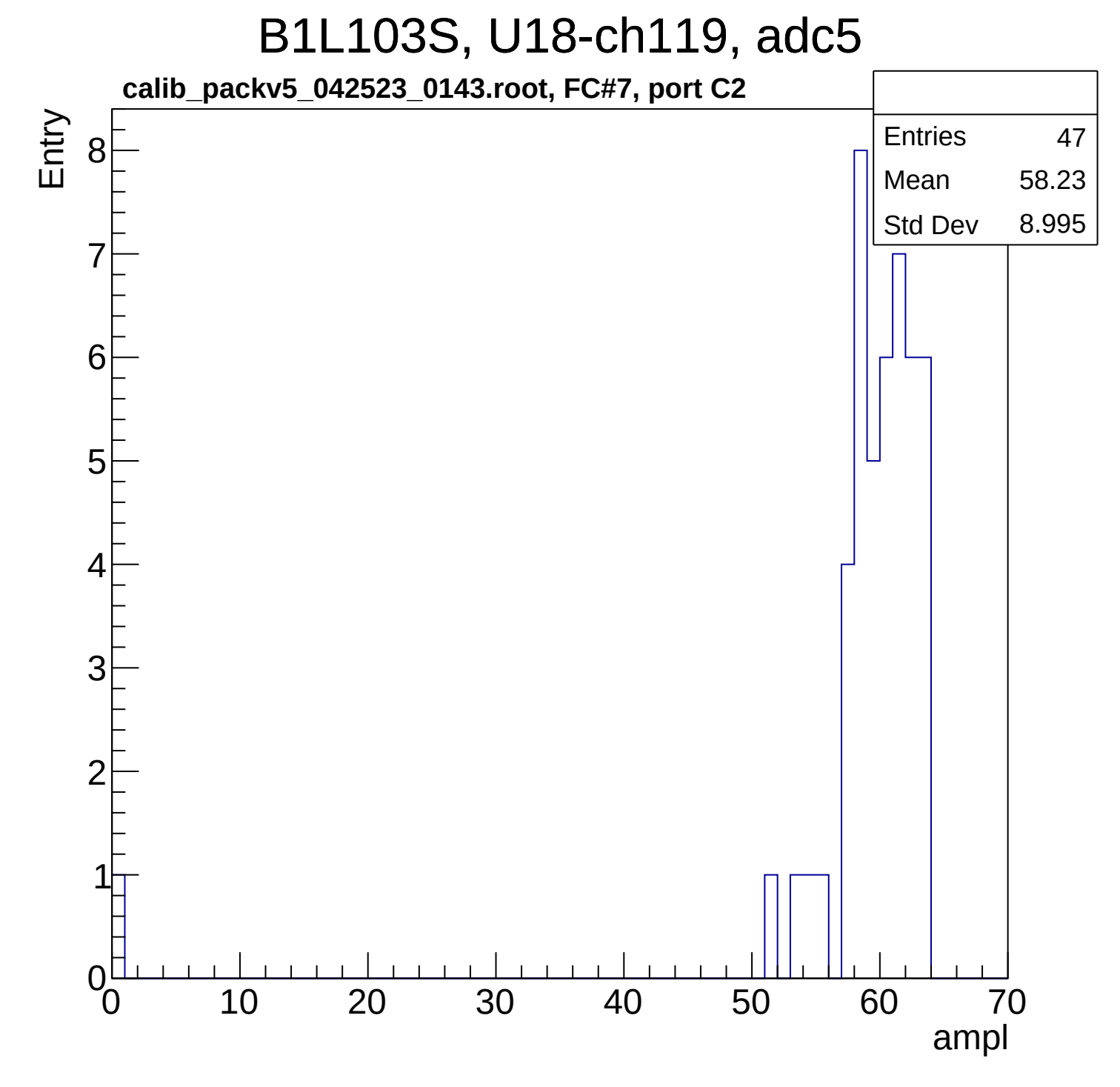
B1L103S, U18-ch119, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 47
Mean 58.23
Std Dev 8.995
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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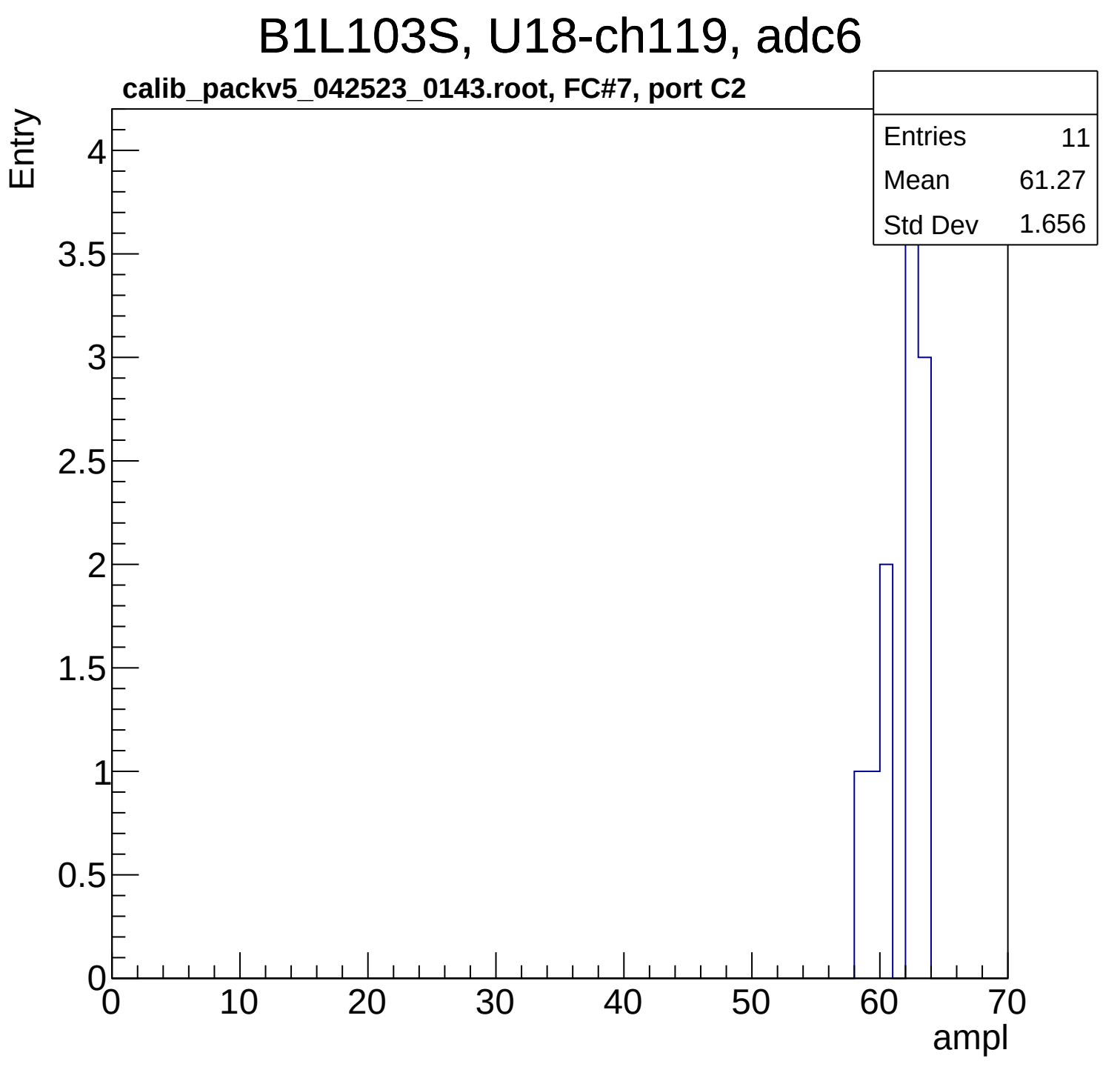
B1L103S, U18-ch119, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 11
Mean 61.27
Std Dev 1.656
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
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20
30
40
50
60
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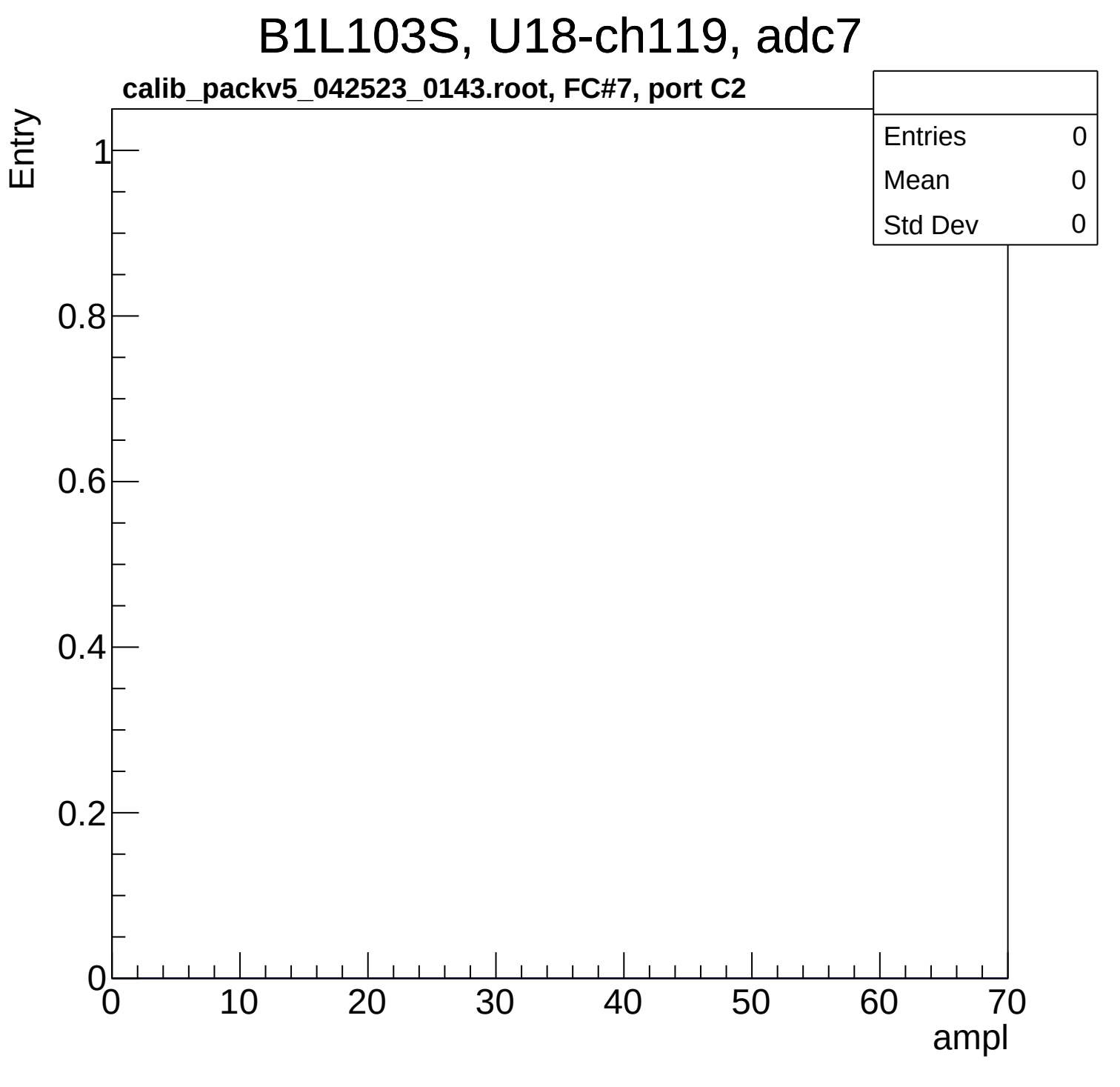
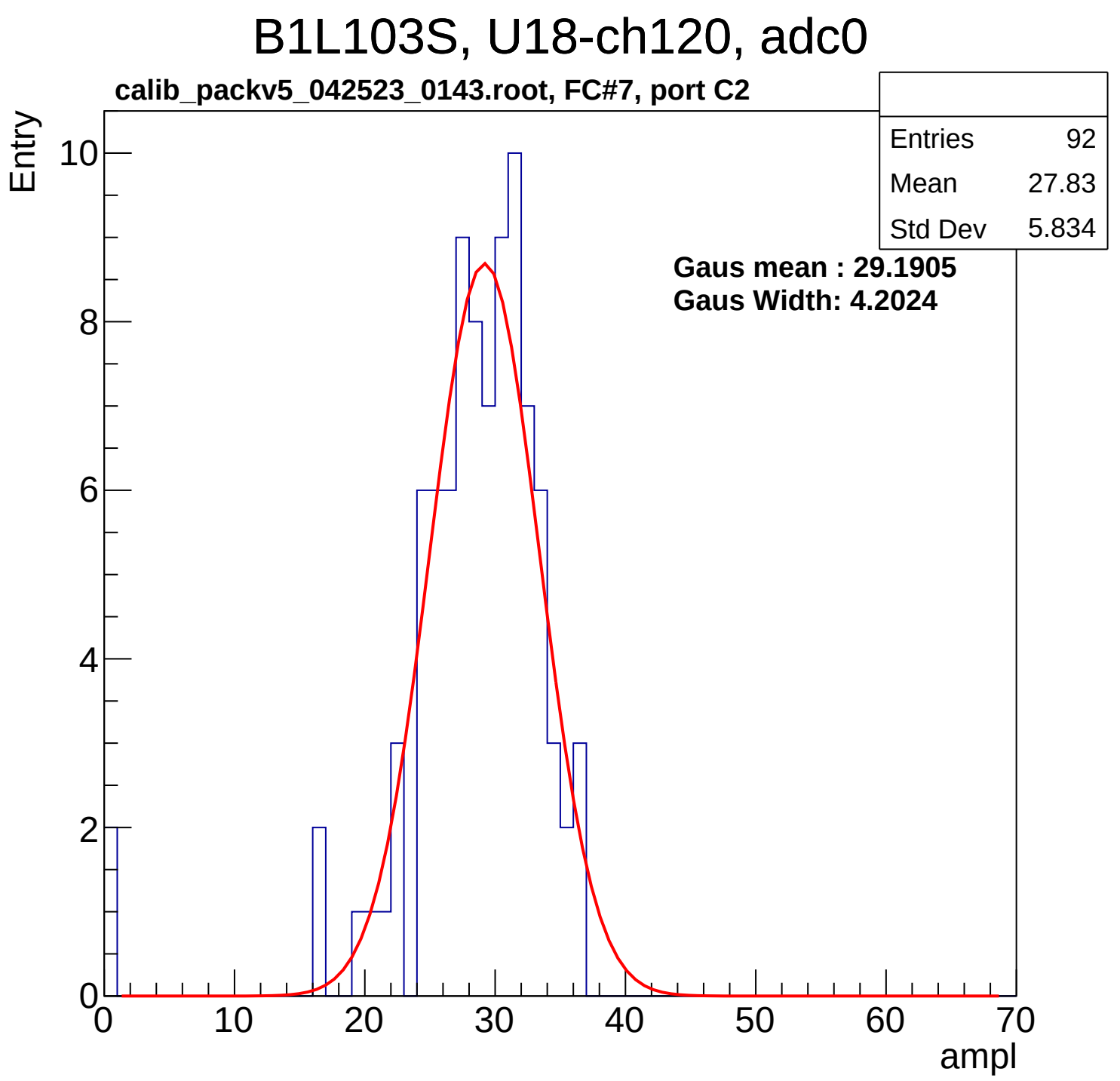
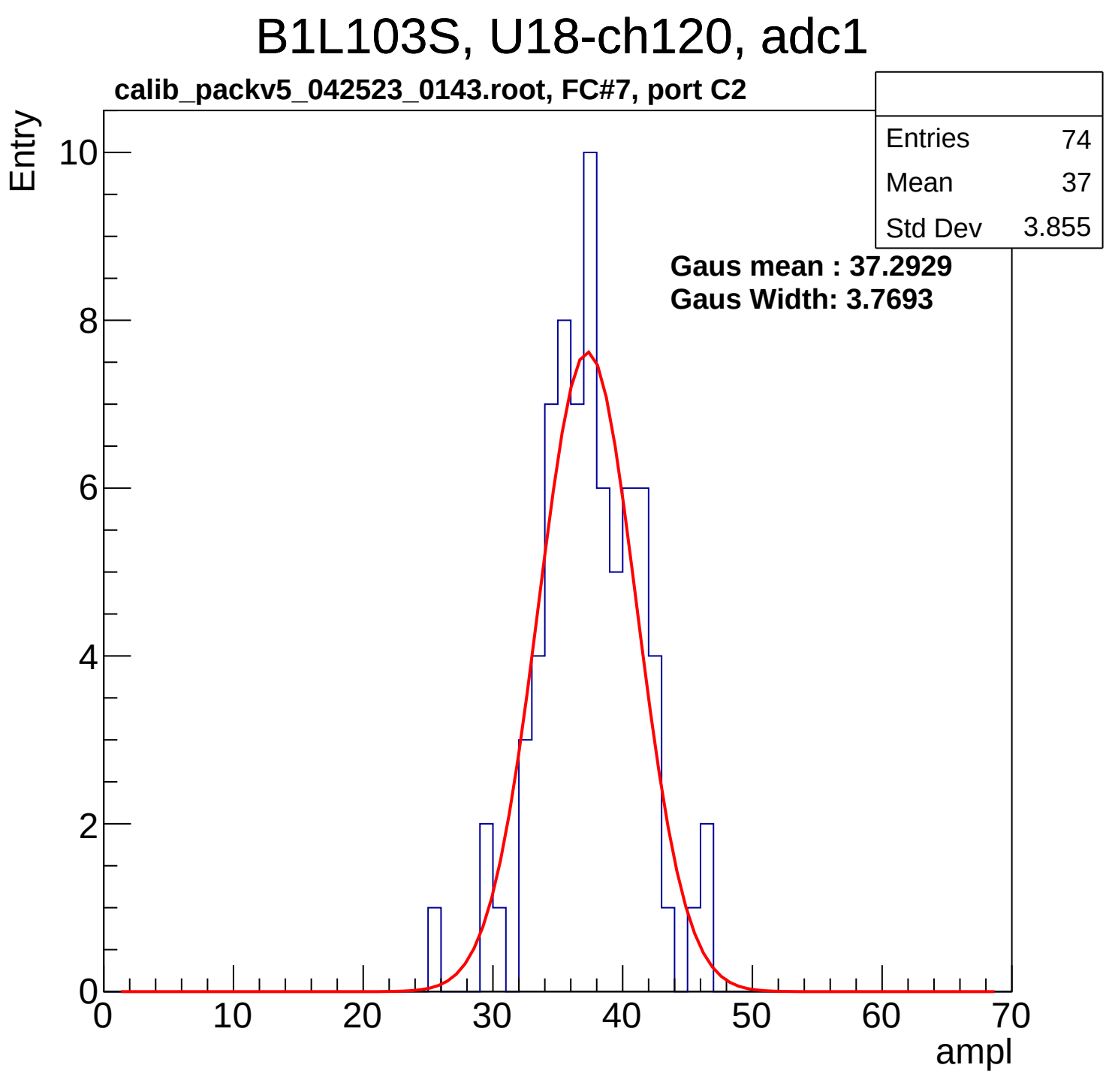

B1L103S, U18-ch119, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch120, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 92
Mean 27.83
Std Dev 5.834
Gaus mean : 29.1905
Gaus Width: 4.2024
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch120, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 74
Mean 37
Std Dev 3.855
Gaus mean : 37.2929
Gaus Width: 3.7693
Entry
ampl
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2
4
6
8
10
0
10
20
30
40
50
60
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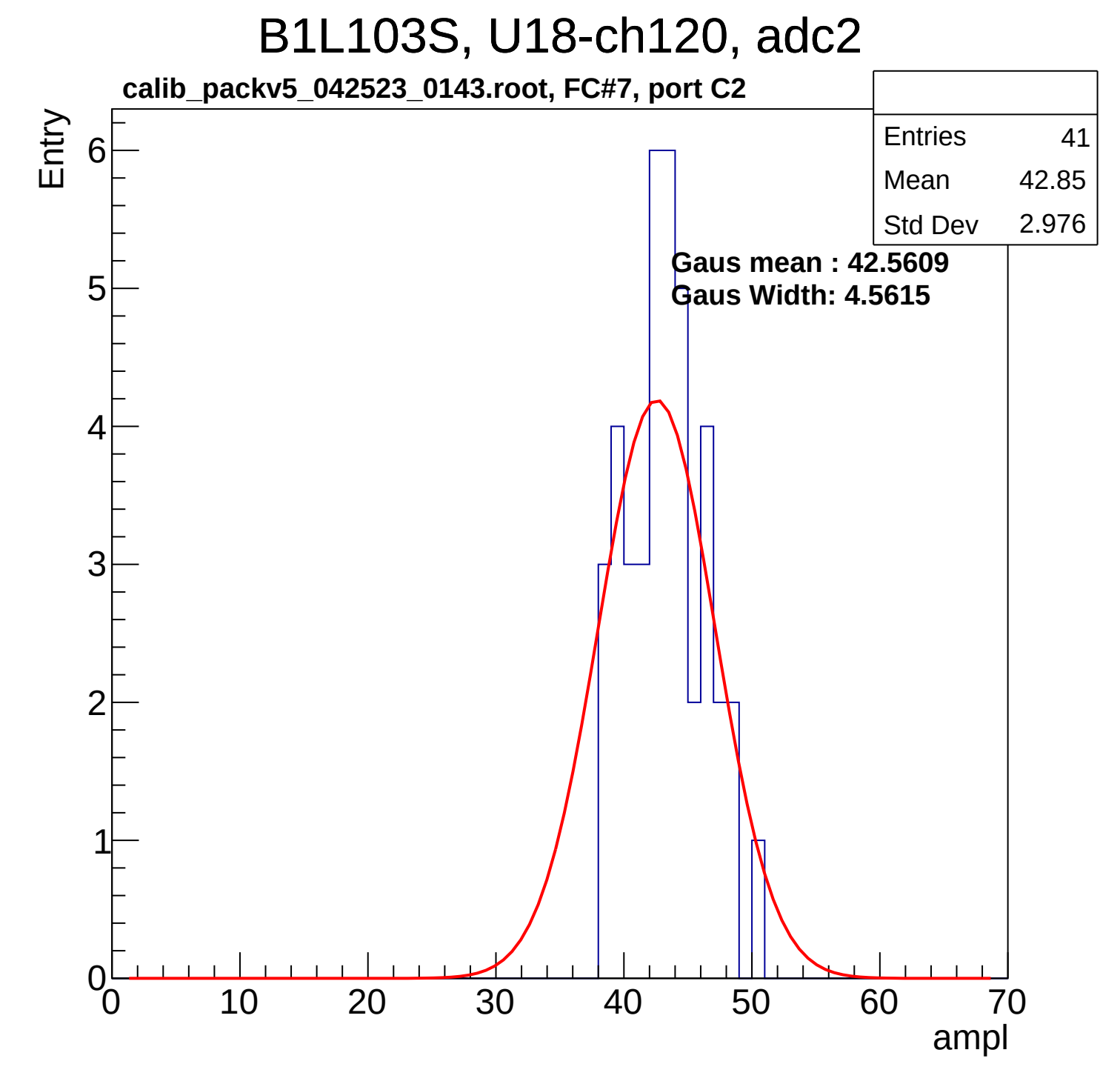
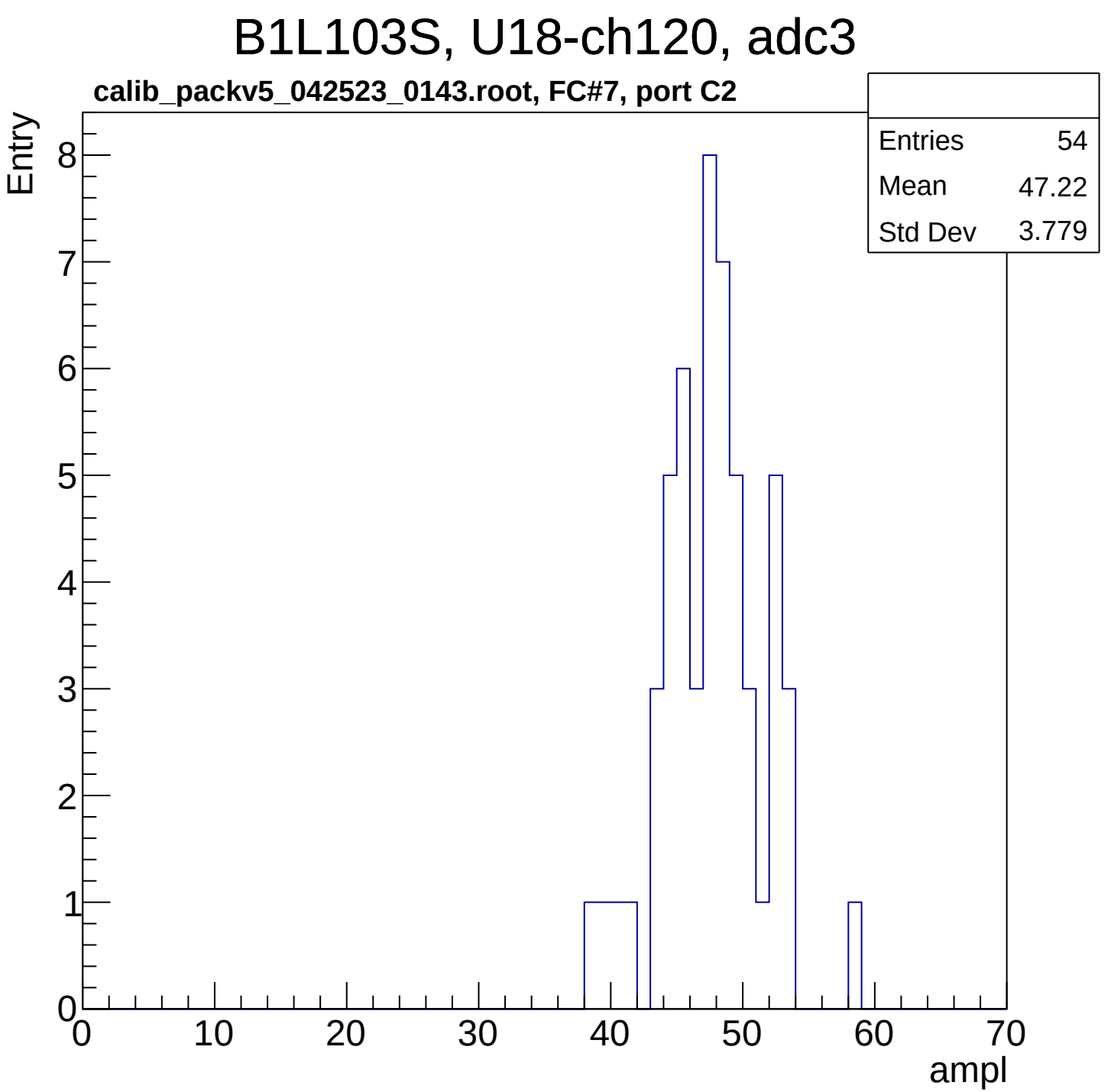

B1L103S, U18-ch120, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 41
Mean 42.85
Std Dev 2.976
Gaus mean : 42.5609
Gaus Width: 4.5615
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U18-ch120, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 54
Mean 47.22
Std Dev 3.779
Entry
ampl
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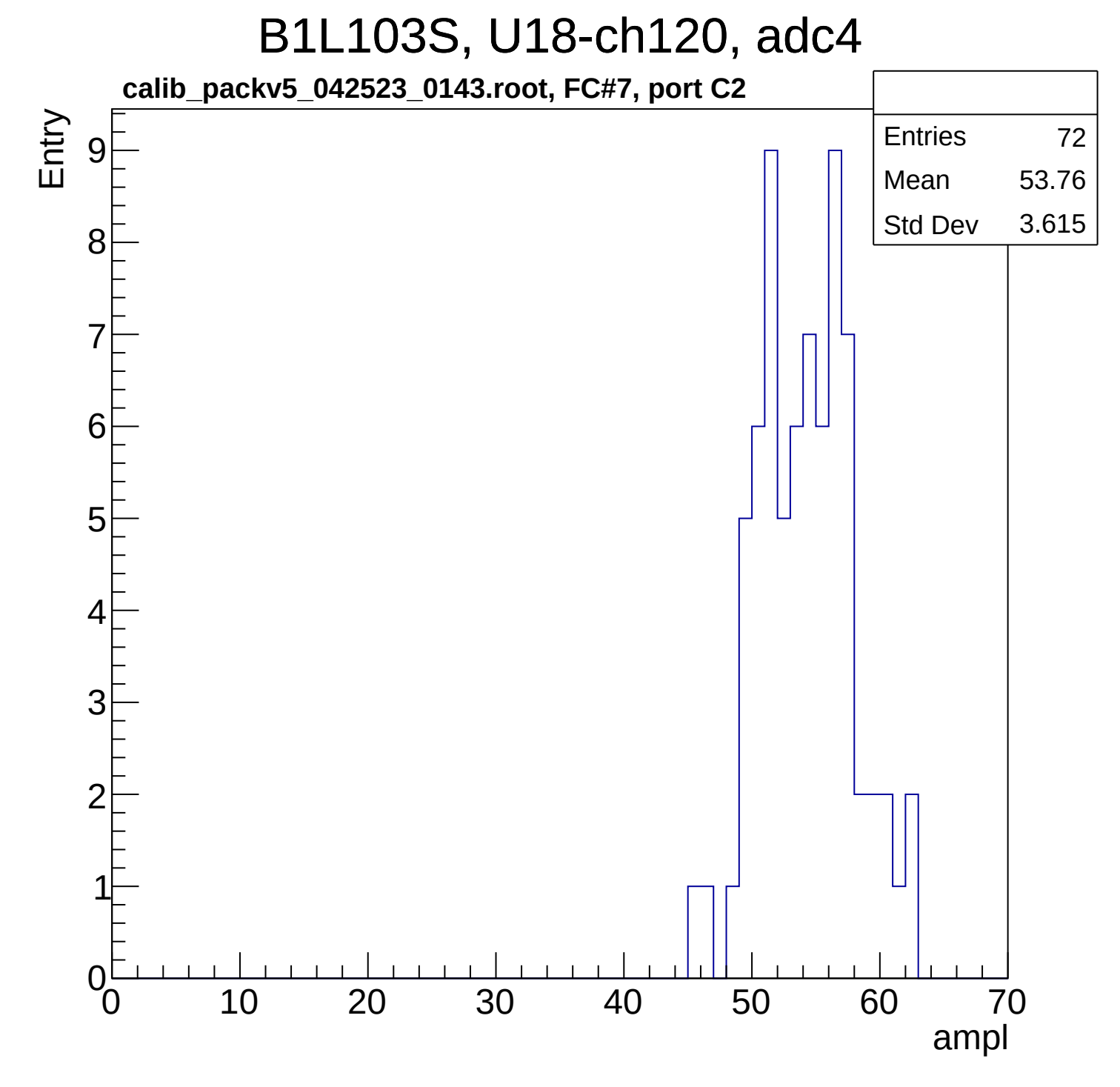
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch120, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 72
Mean 53.76
Std Dev 3.615
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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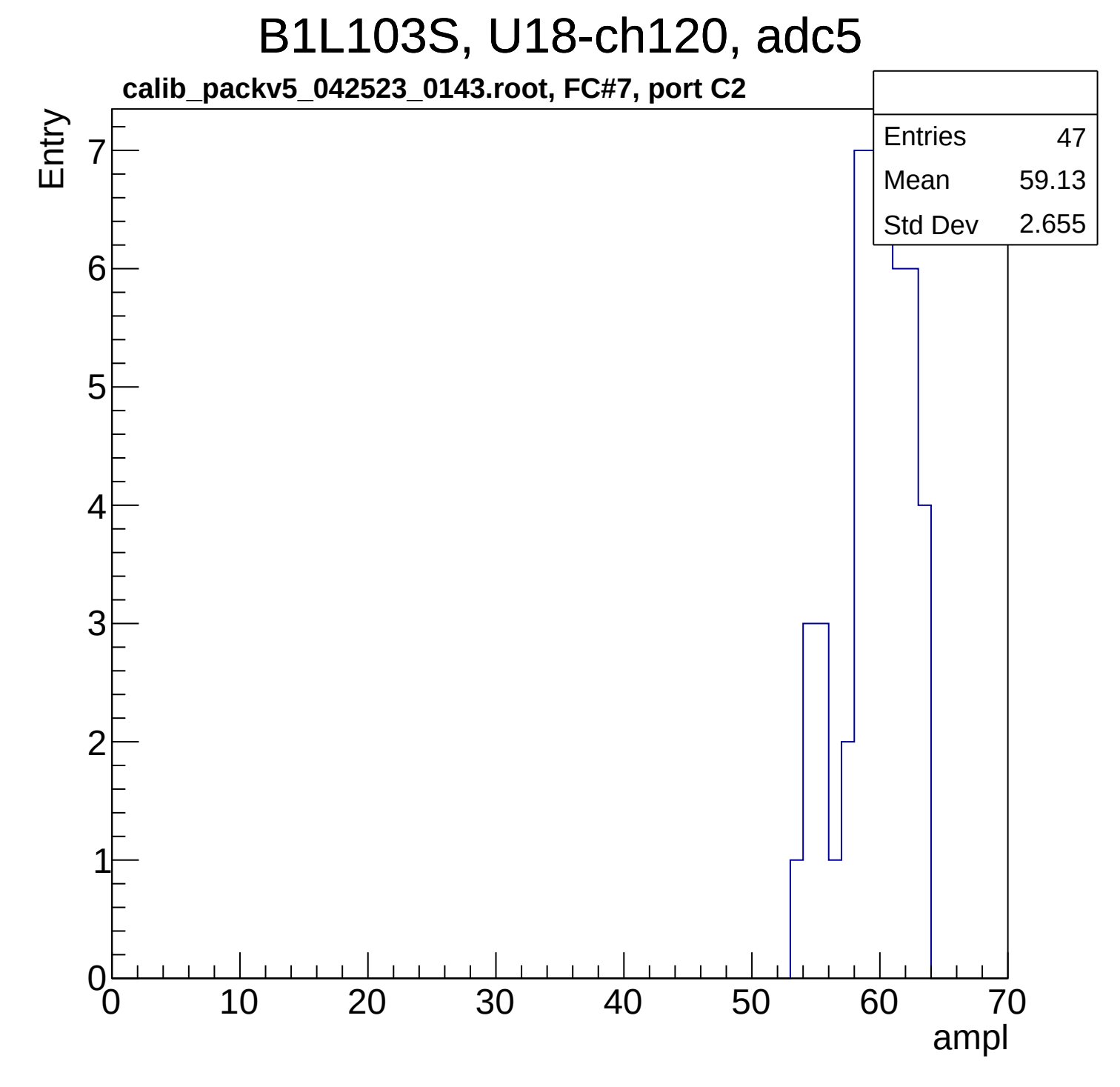
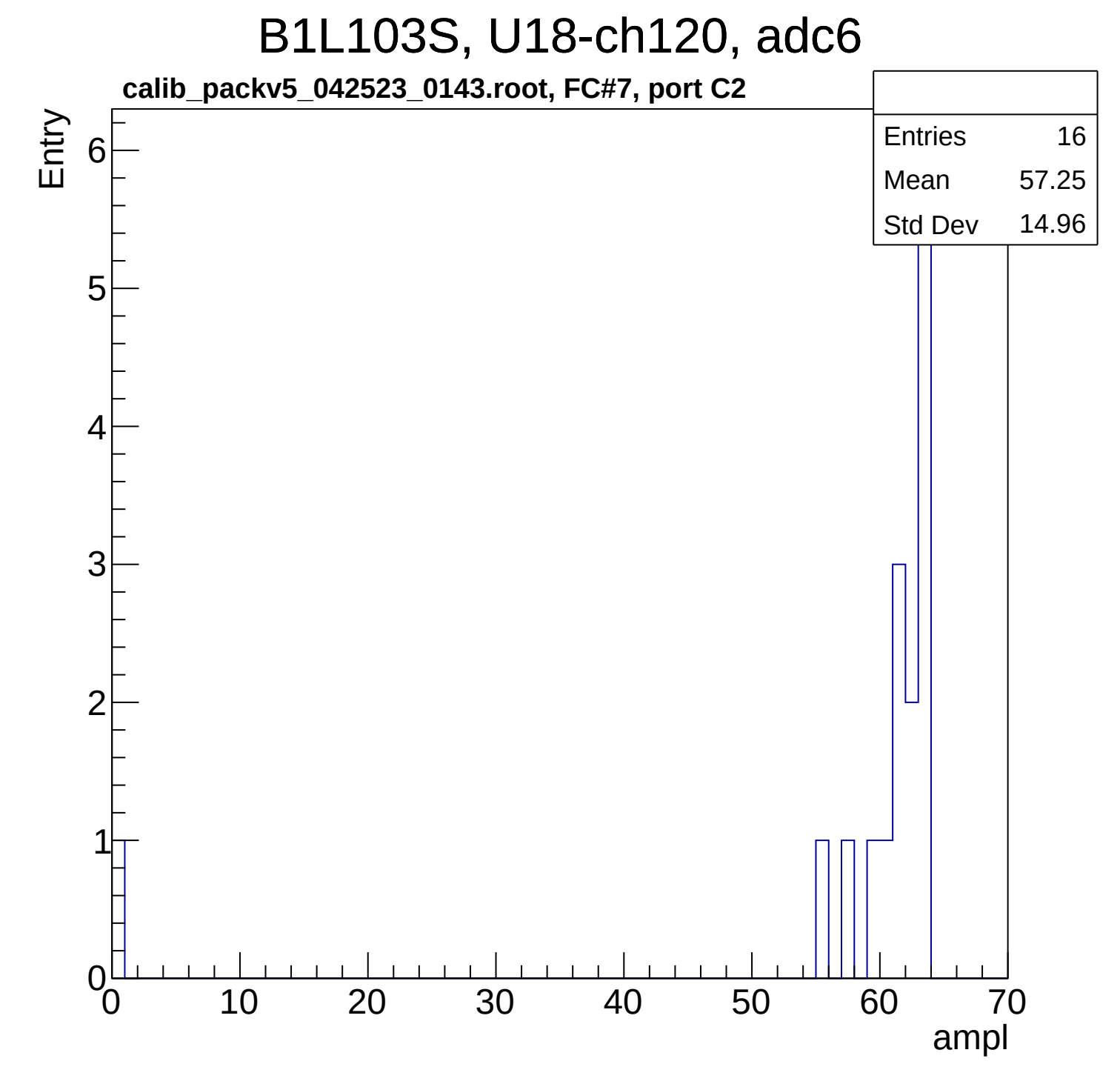
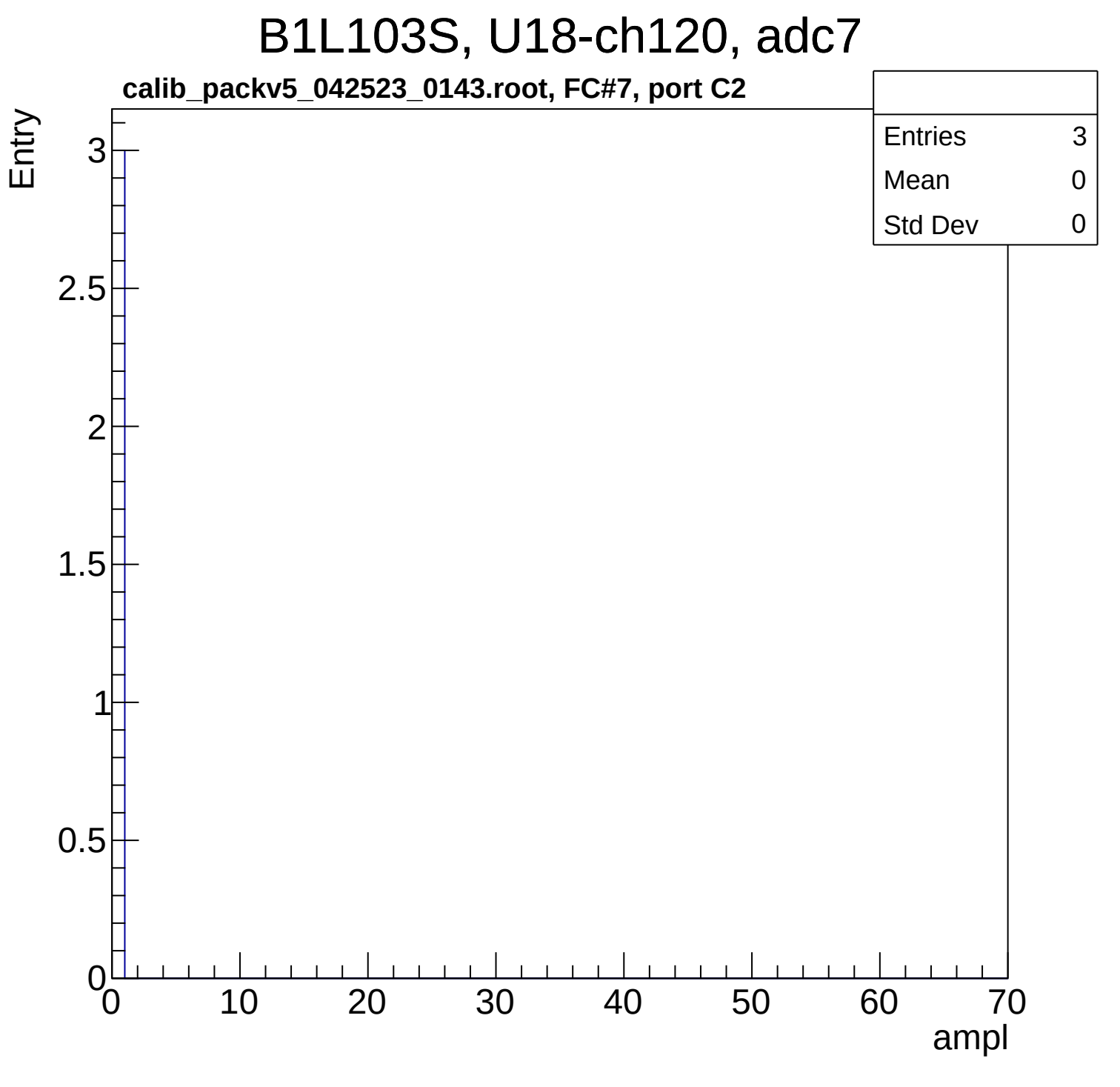
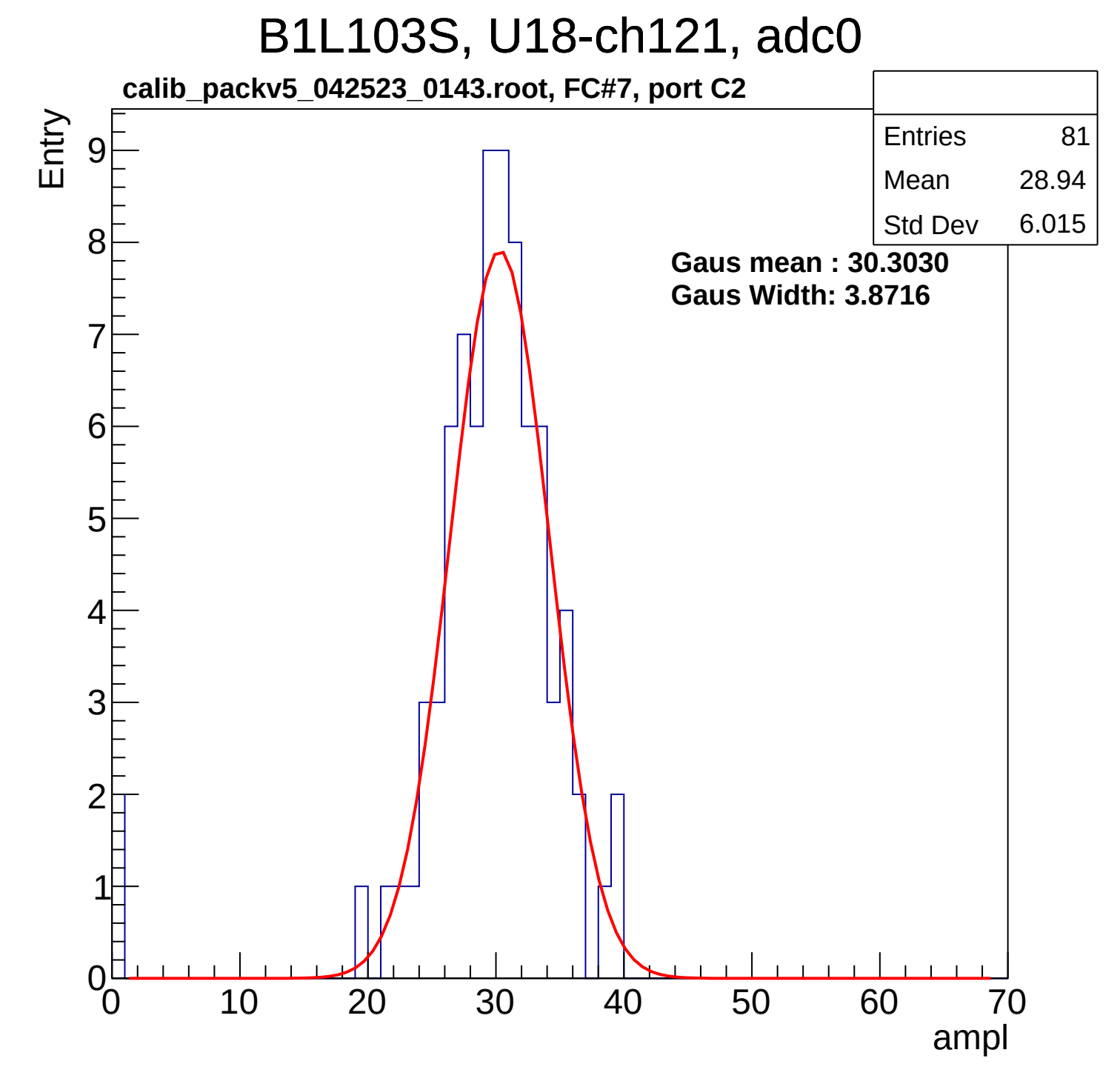
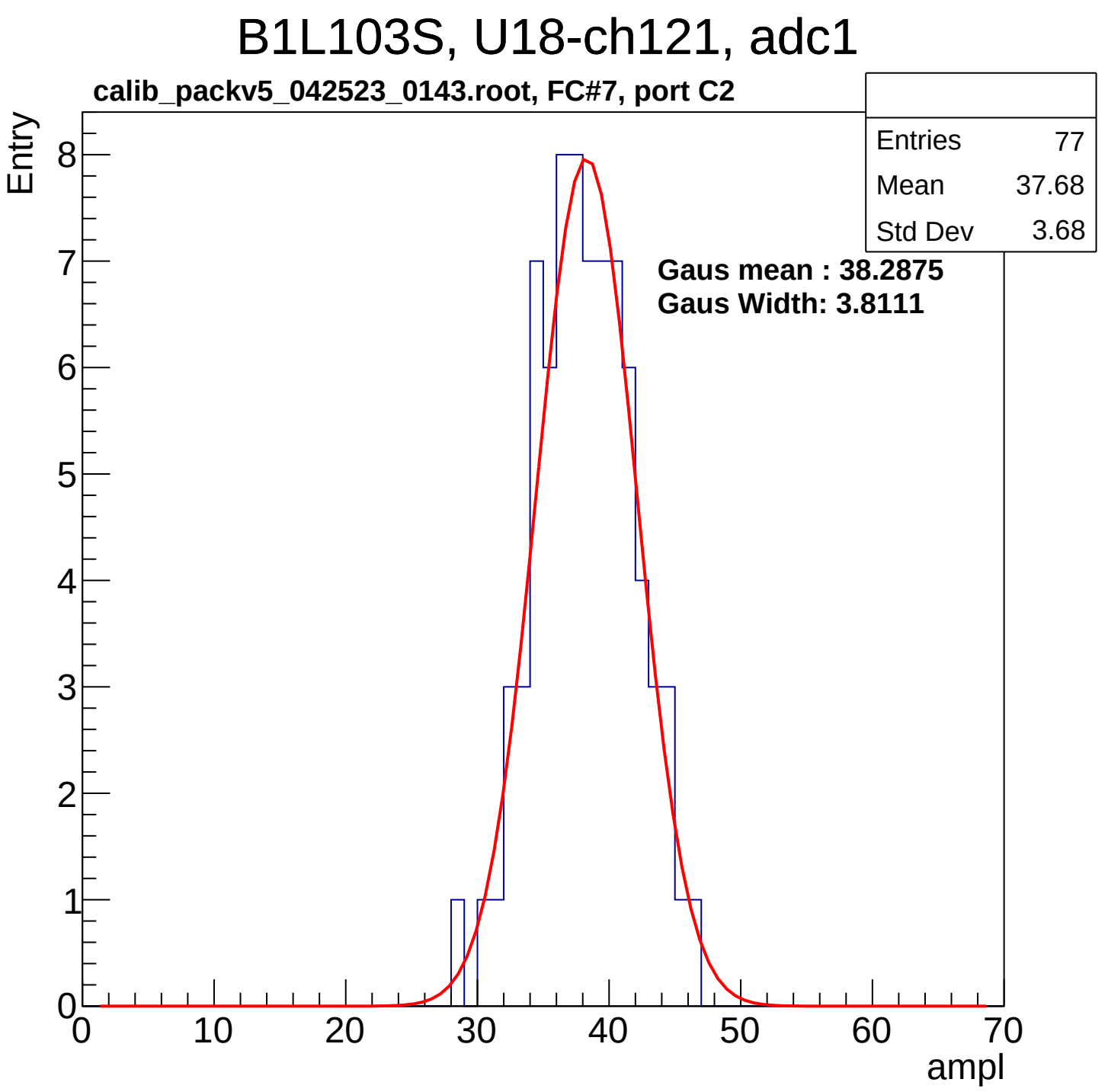
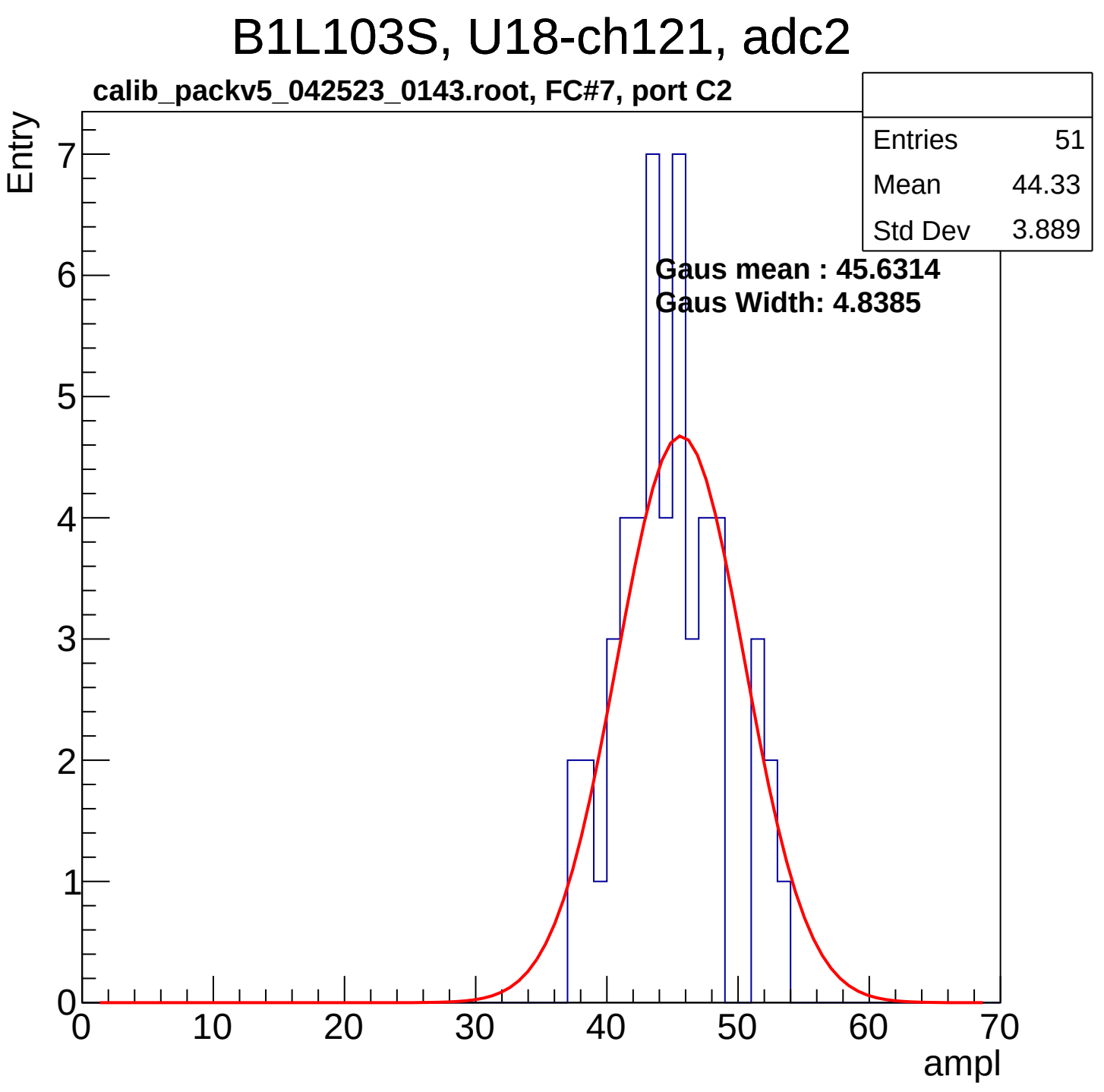

B1L103S, U18-ch120, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 47
Mean 59.13
Std Dev 2.655
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch120, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 16
Mean 57.25
Std Dev 14.96
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch120, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 0
Std Dev 0
Entry
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch121, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 81
Mean 28.94
Std Dev 6.015
Gaus mean : 30.3030
Gaus Width: 3.8716
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch121, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 77
Mean 37.68
Std Dev 3.68
Gaus mean : 38.2875
Gaus Width: 3.8111
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch121, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 51
Mean 44.33
Std Dev 3.889
Gaus mean : 45.6314
Gaus Width: 4.8385
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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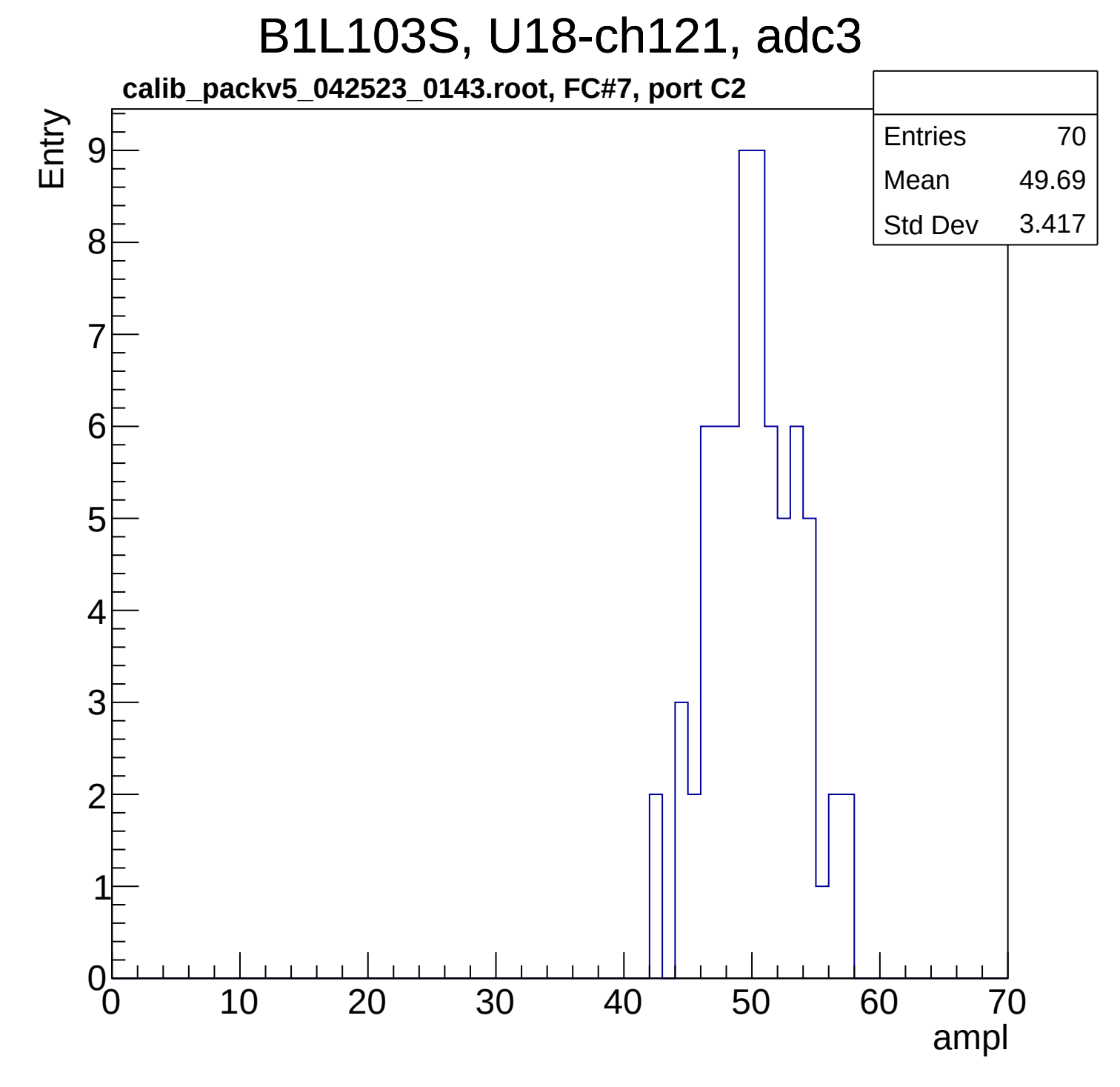
B1L103S, U18-ch121, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 49.69
Std Dev 3.417
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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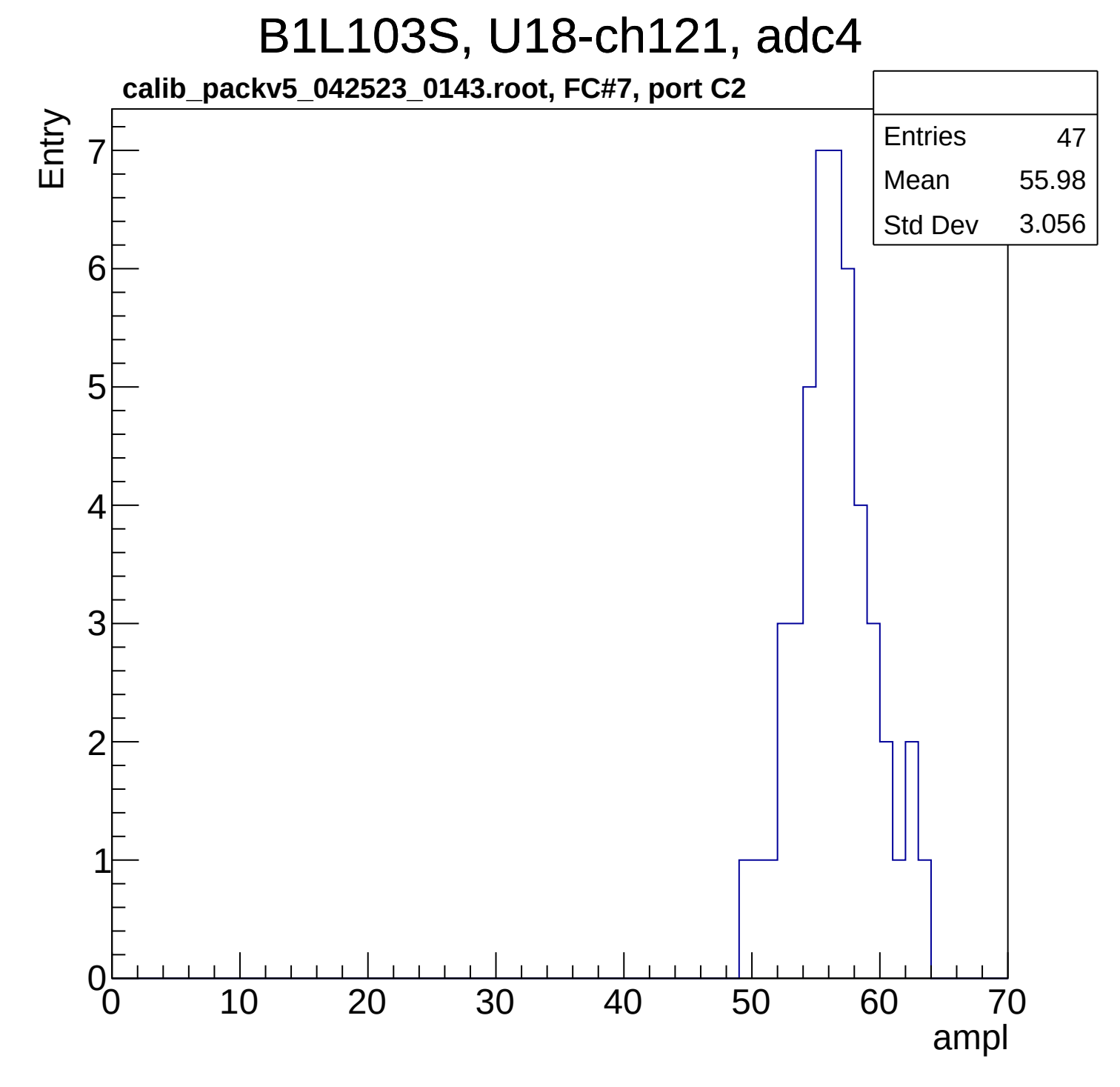
B1L103S, U18-ch121, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 47
Mean 55.98
Std Dev 3.056
Entry
ampl
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1
2
3
4
5
6
7
0
10
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30
40
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60
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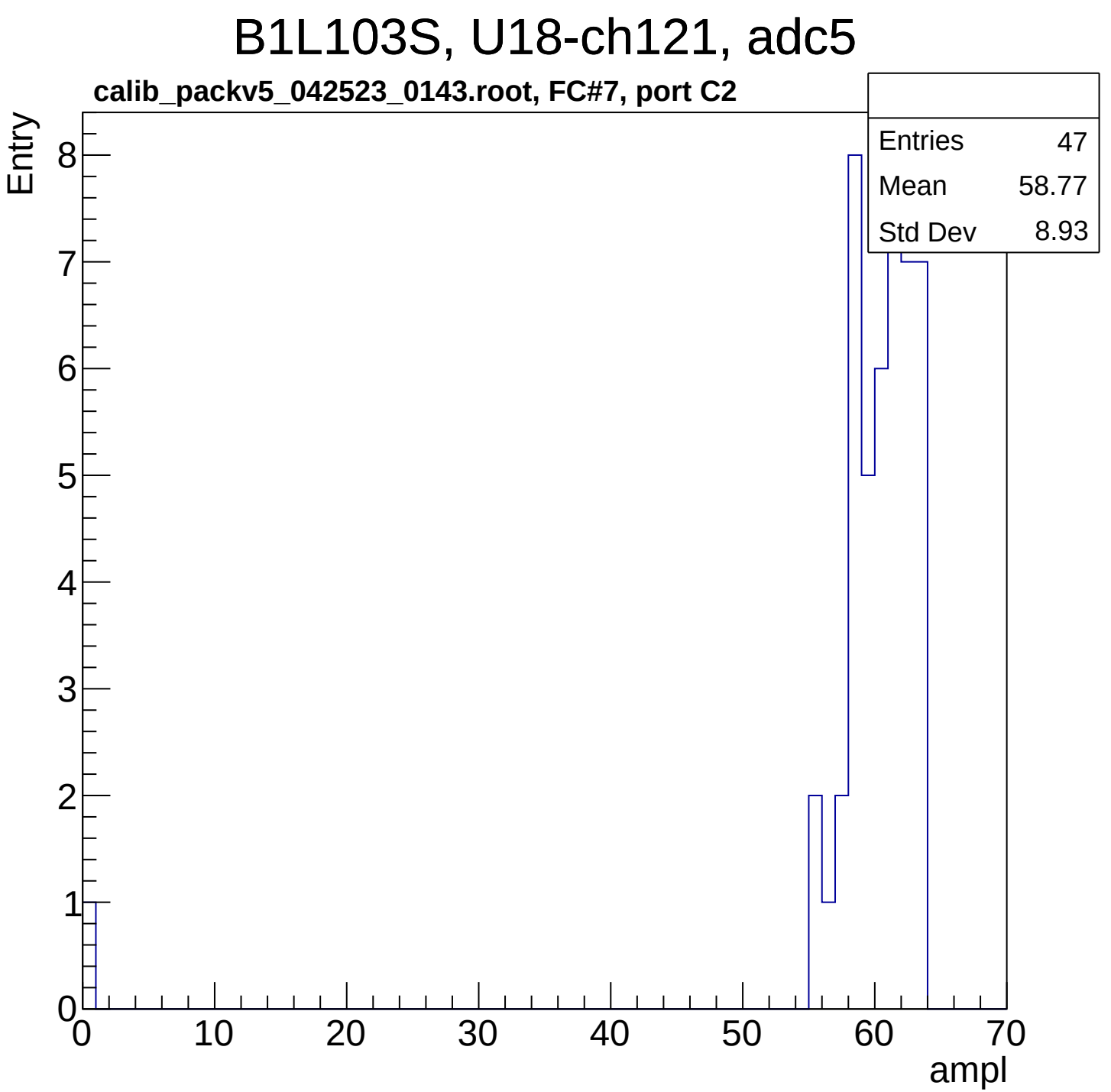
B1L103S, U18-ch121, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 47
Mean 58.77
Std Dev 8.93
Entry
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8
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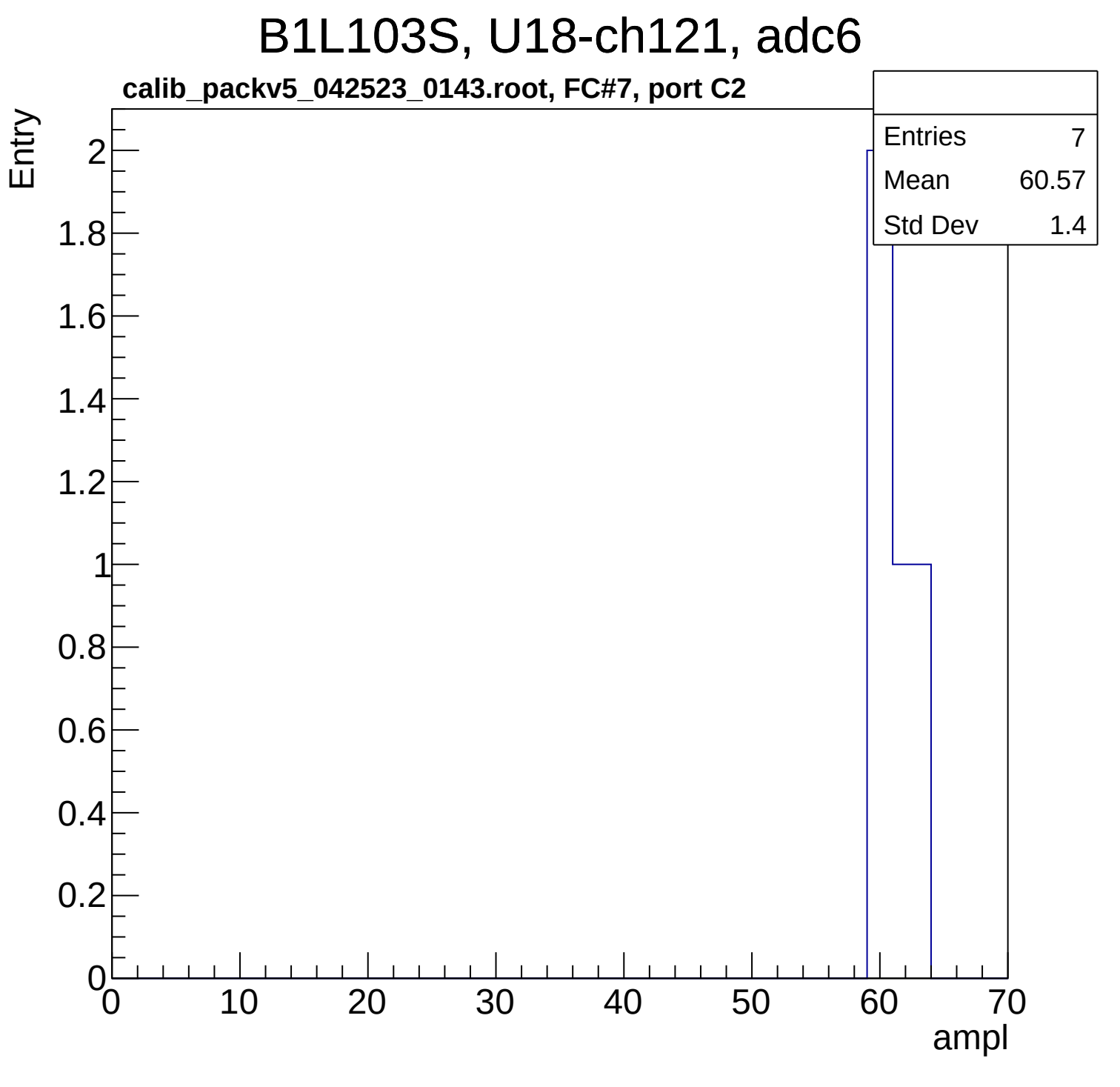
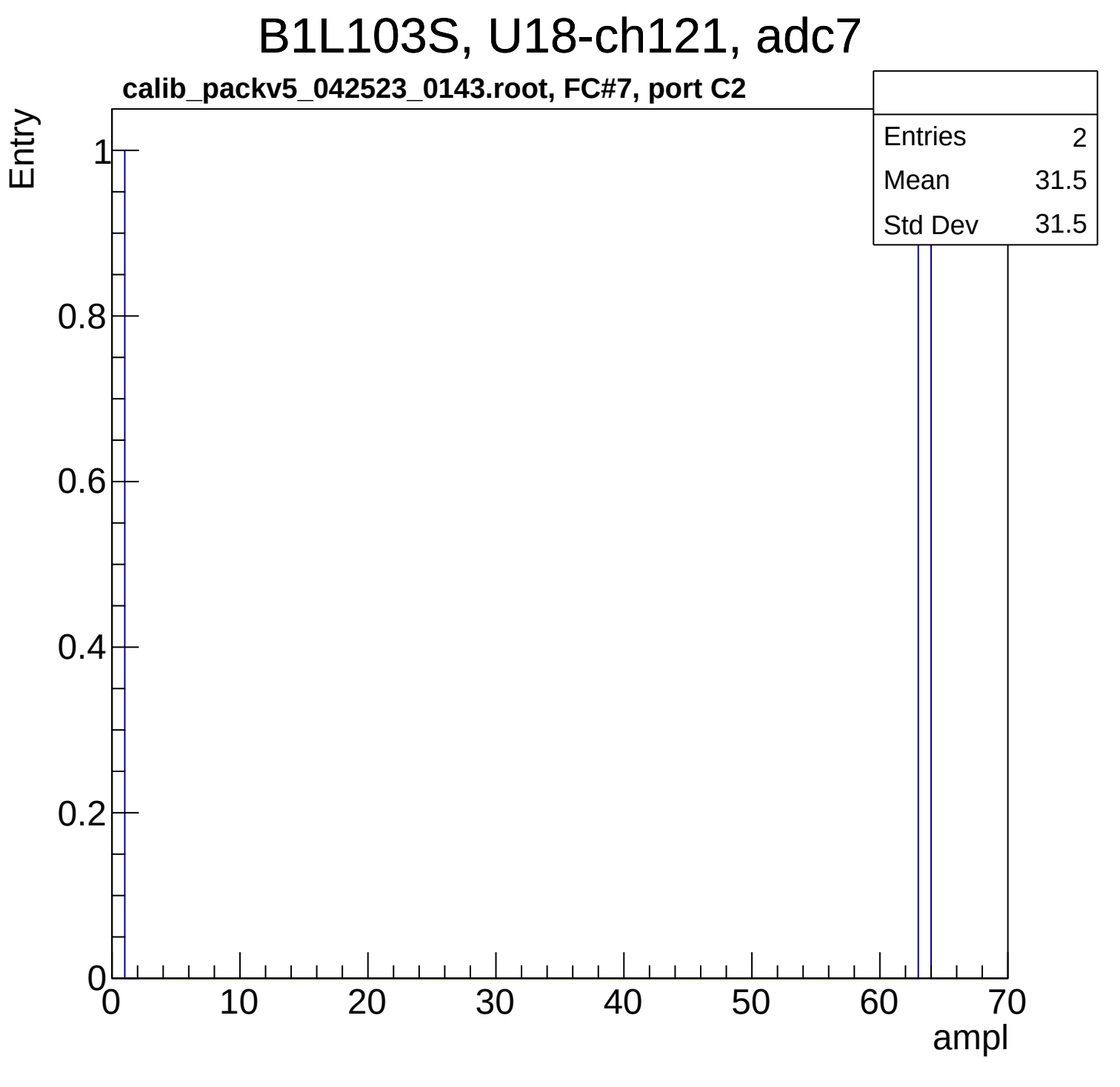
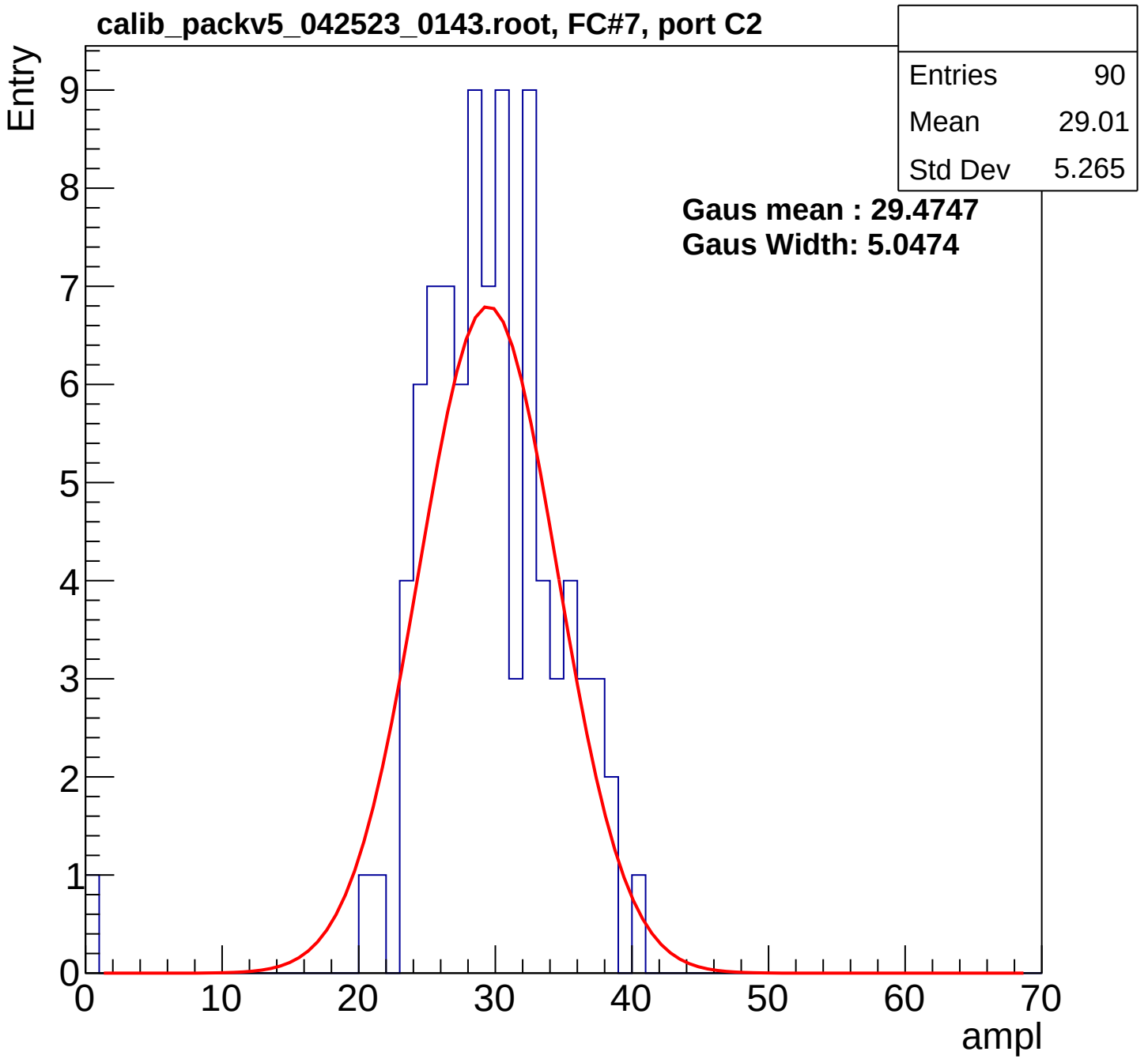
20
30
40
50
60
70
ampl


B1L103S, U18-ch121, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 7
Mean 60.57
Std Dev 1.4
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U18-ch121, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 31.5
Std Dev 31.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch122, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 90
Mean 29.01
Std Dev 5.265
Gaus mean : 29.4747
Gaus Width: 5.0474
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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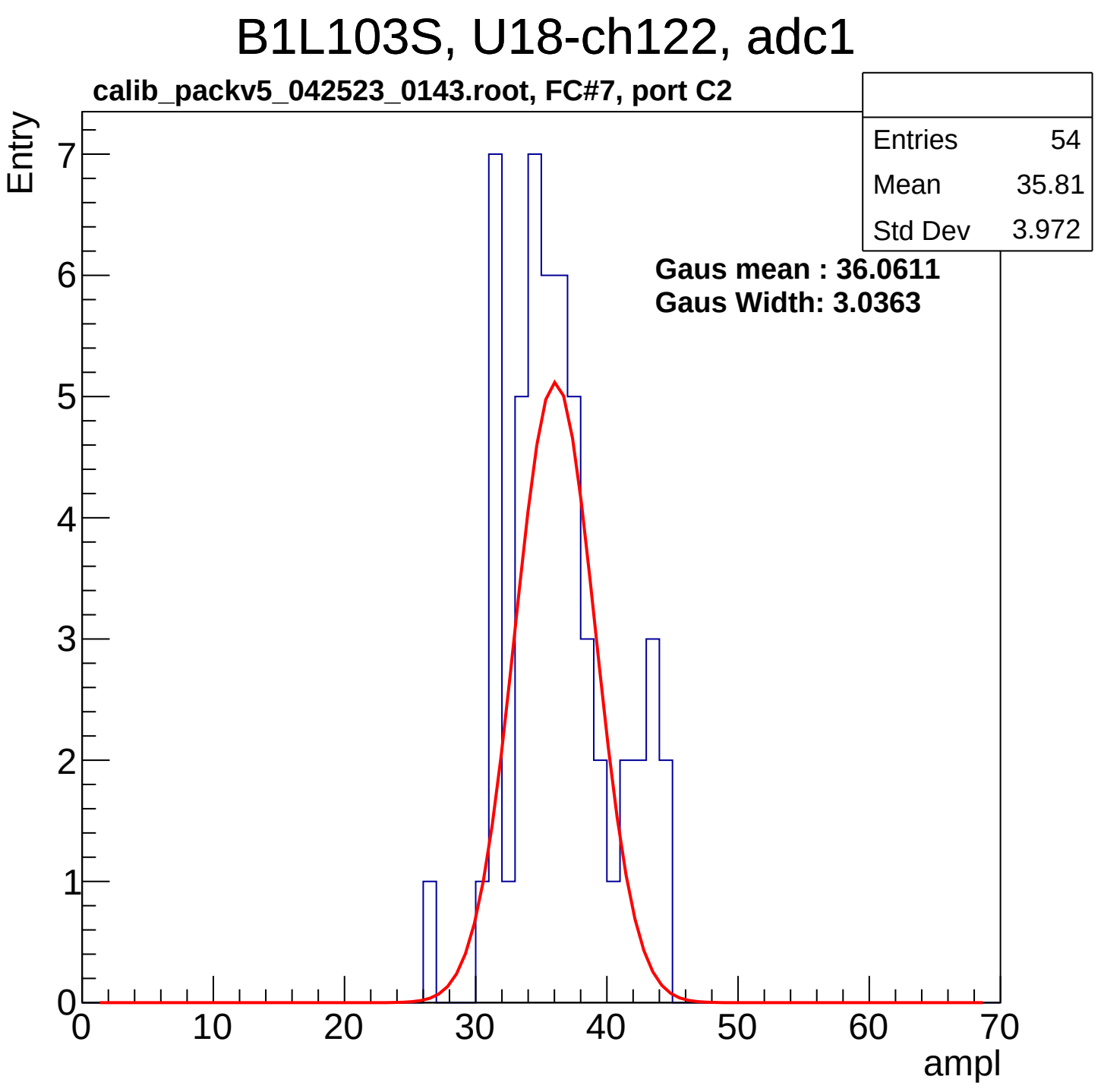
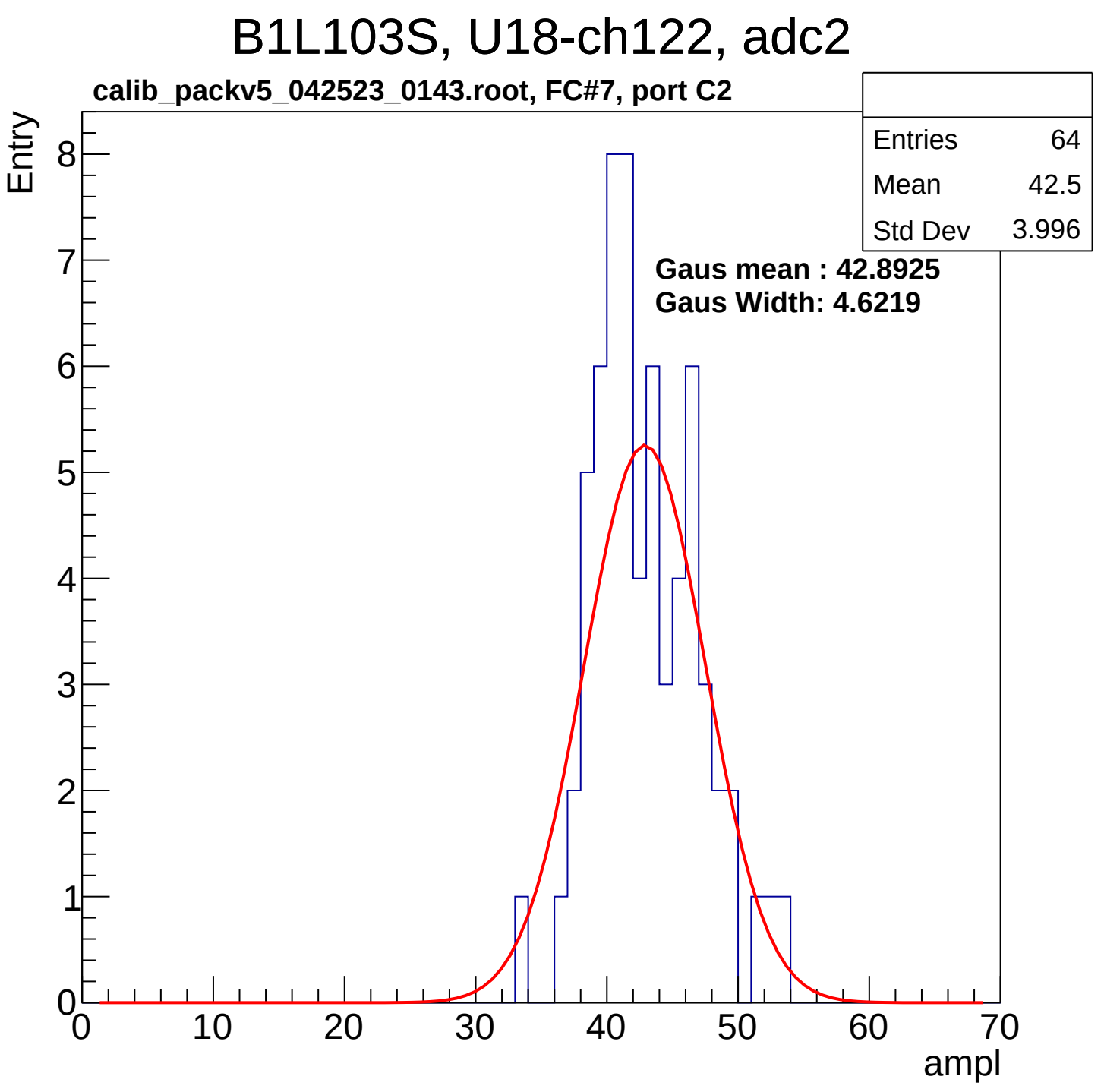

B1L103S, U18-ch122, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 54
Mean 35.81
Std Dev 3.972
Gaus mean : 36.0611
Gaus Width: 3.0363
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch122, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 42.5
Std Dev 3.996
Gaus mean : 42.8925
Gaus Width: 4.6219
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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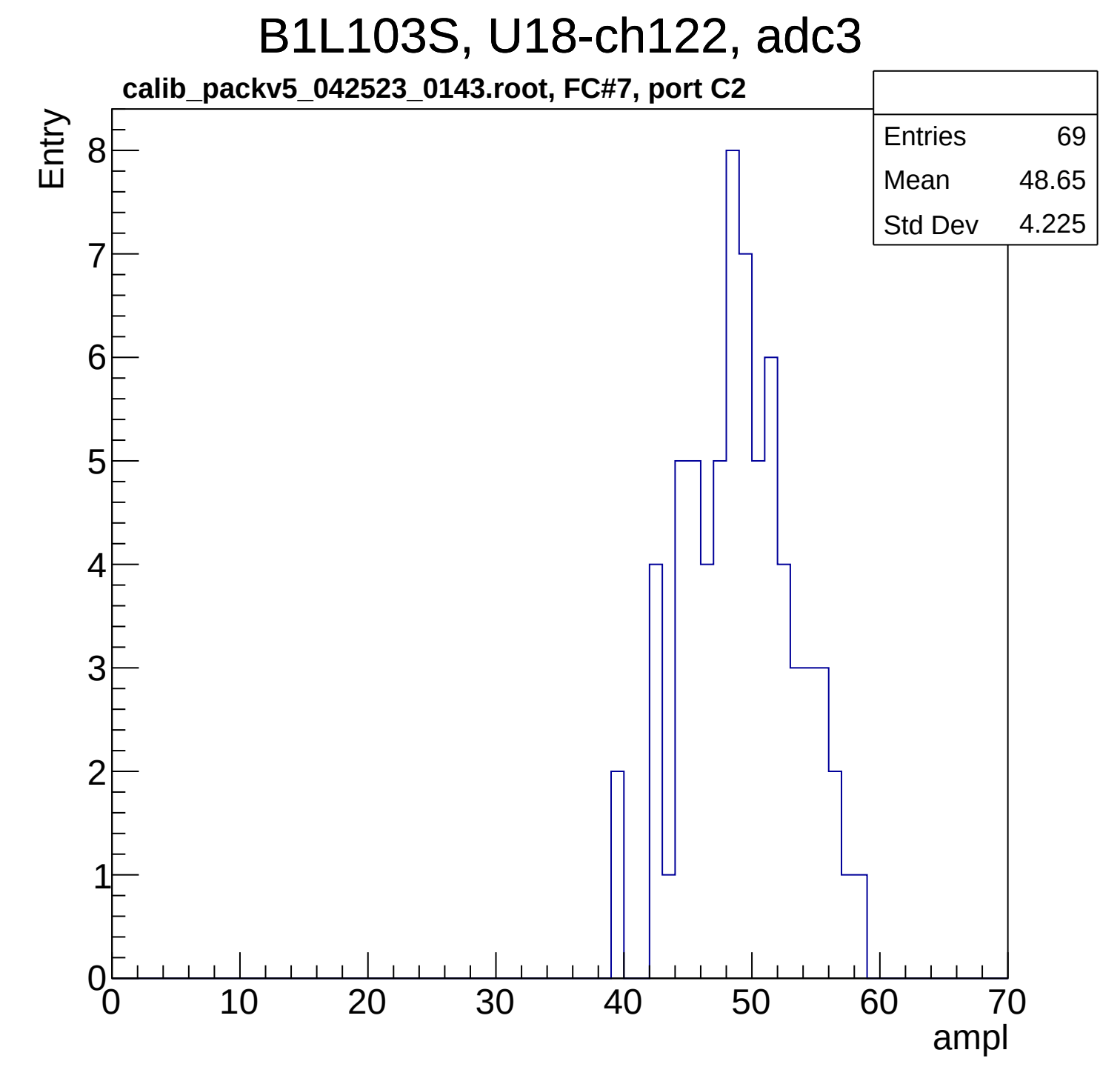
B1L103S, U18-ch122, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 48.65
Std Dev 4.225
Entry
ampl
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1
2
3
4
5
6
7
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0
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60
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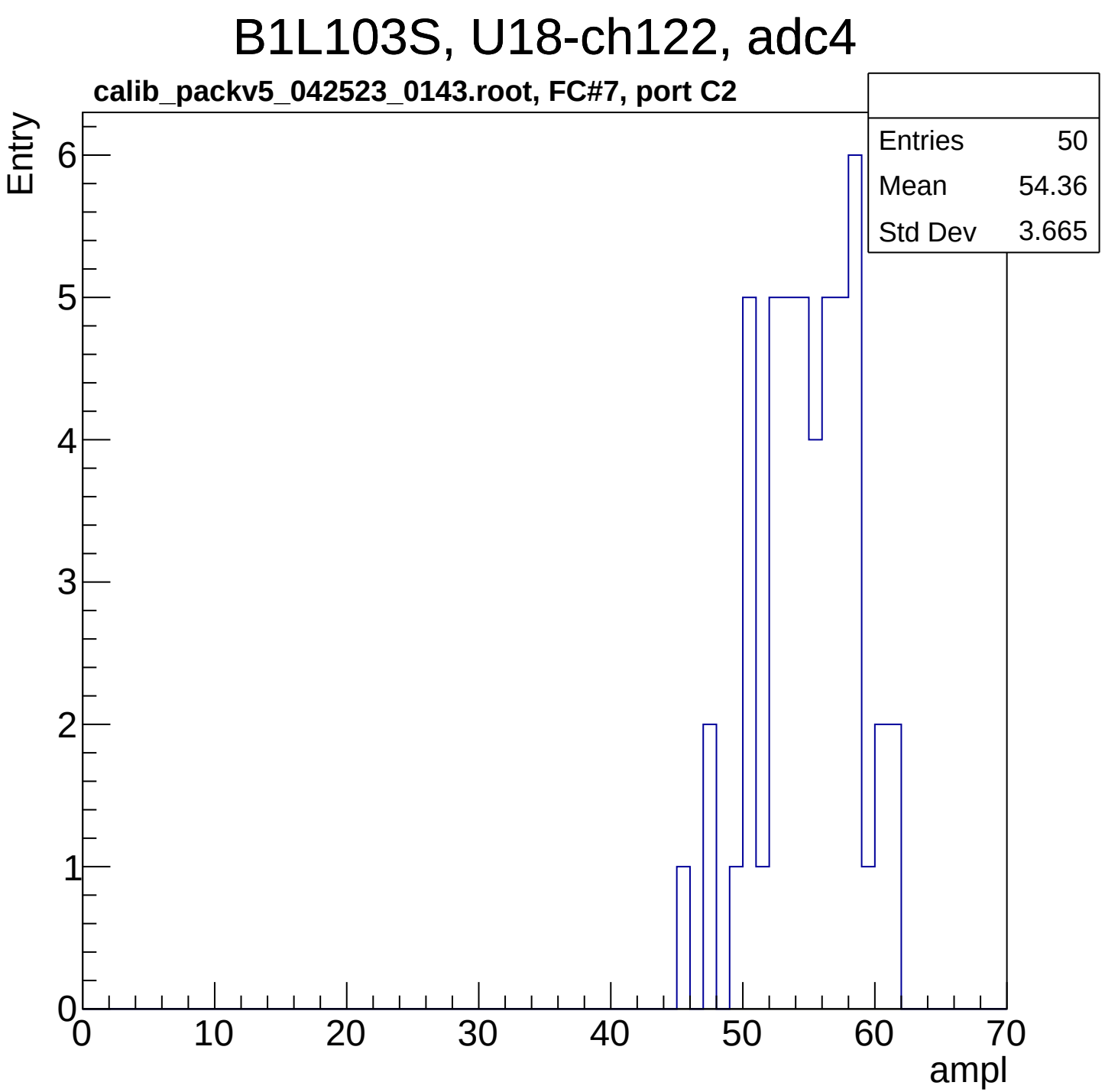
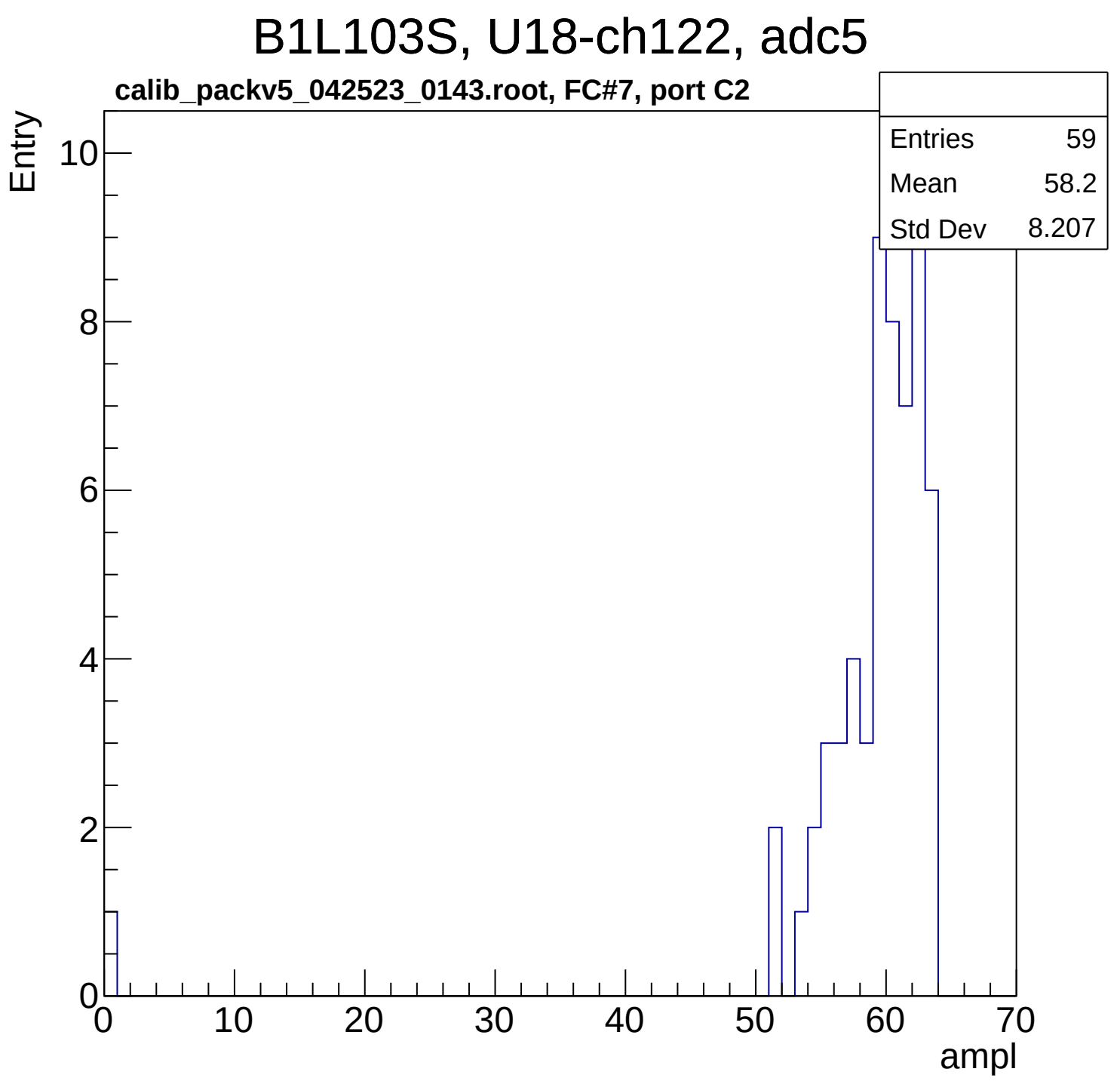
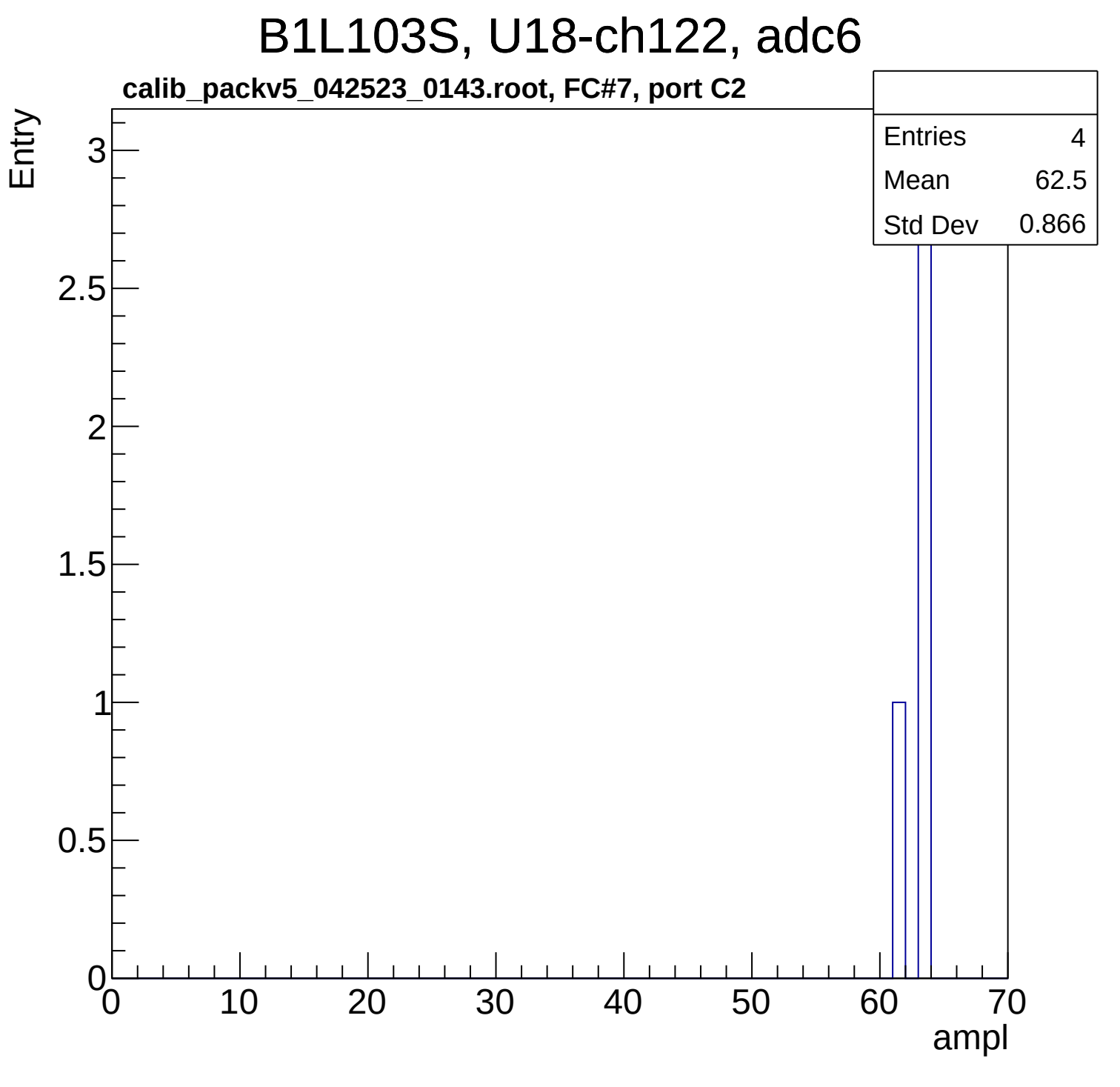

B1L103S, U18-ch122, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 50
Mean 54.36
Std Dev 3.665
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U18-ch122, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 58.2
Std Dev 8.207
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch122, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 4
Mean 62.5
Std Dev 0.866
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
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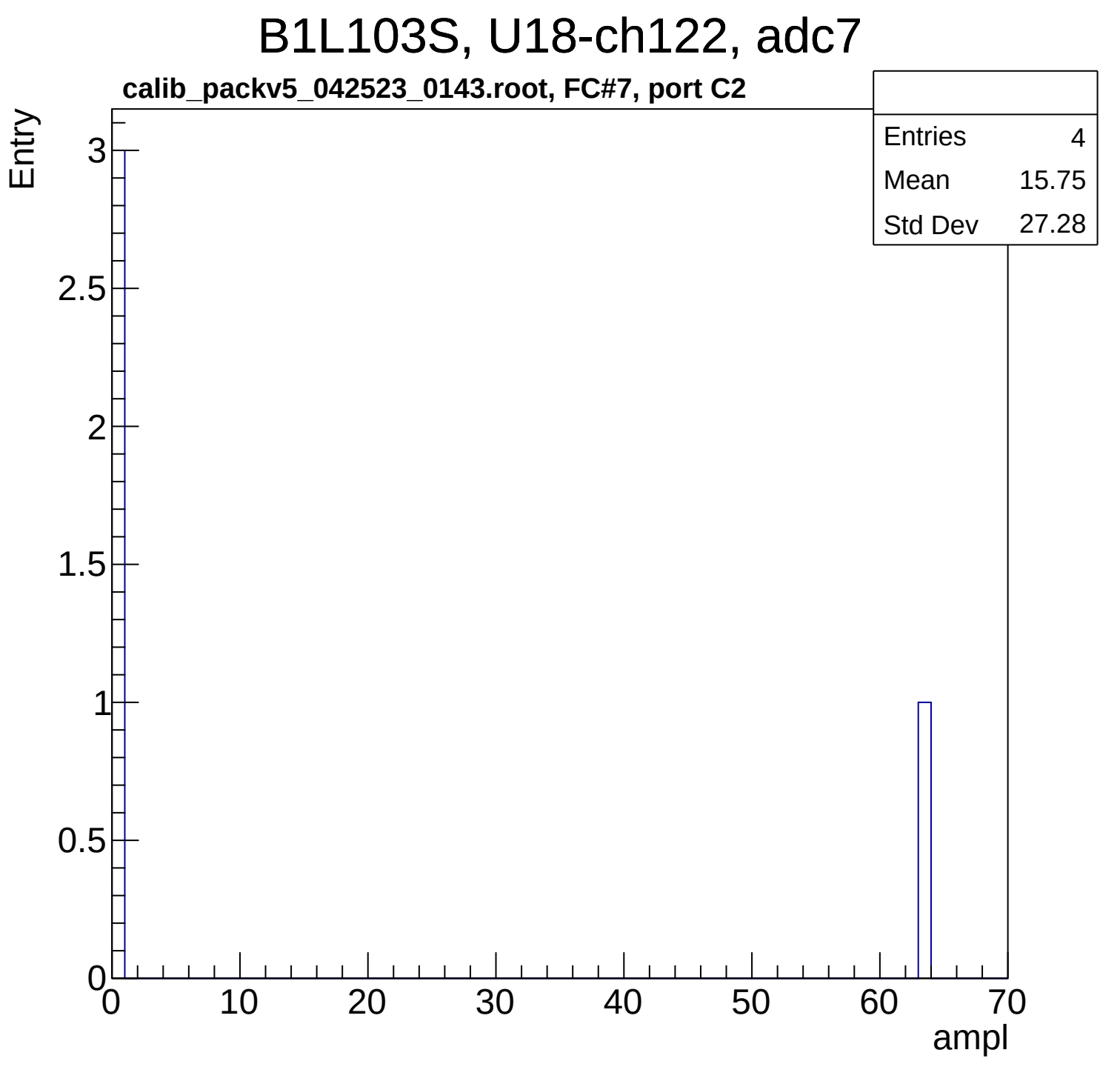
B1L103S, U18-ch122, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 4
Mean 15.75
Std Dev 27.28
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
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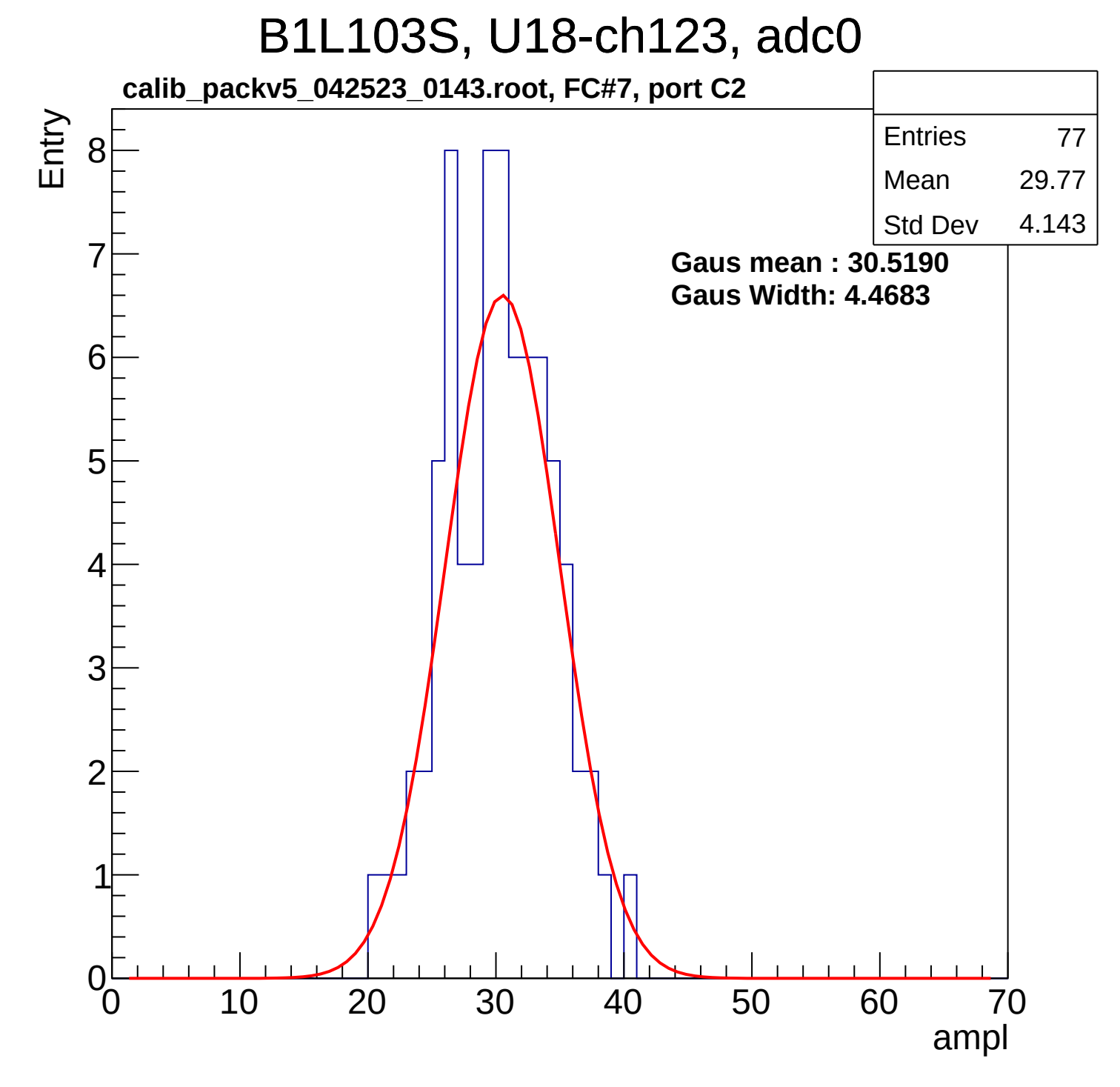
40
50
60
70


B1L103S, U18-ch123, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 77
Mean 29.77
Std Dev 4.143
Gaus mean : 30.5190
Gaus Width: 4.4683
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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20
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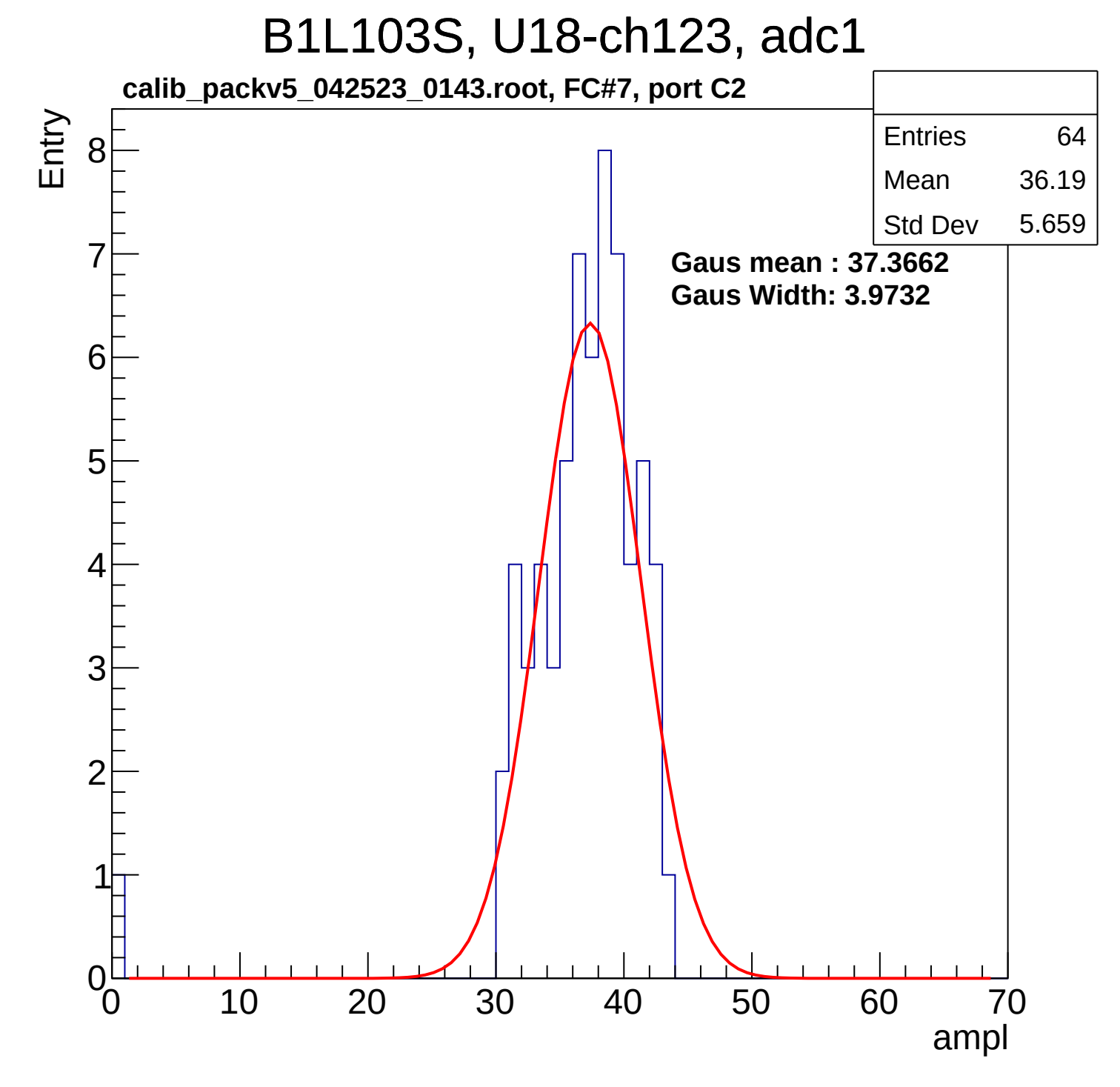
40
50
60
70


B1L103S, U18-ch123, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 36.19
Std Dev 5.659
Gaus mean : 37.3662
Gaus Width: 3.9732
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
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40
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60
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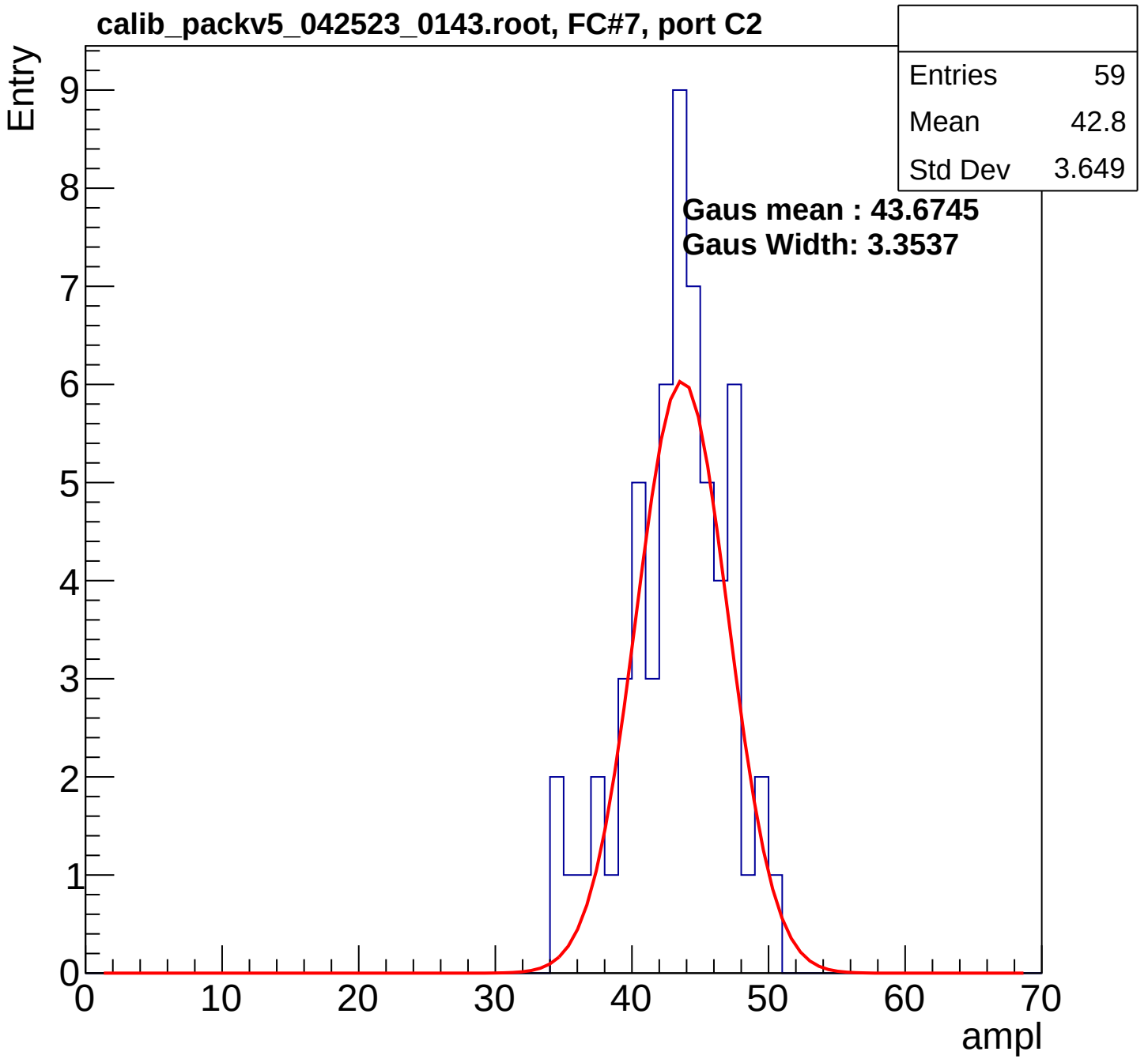
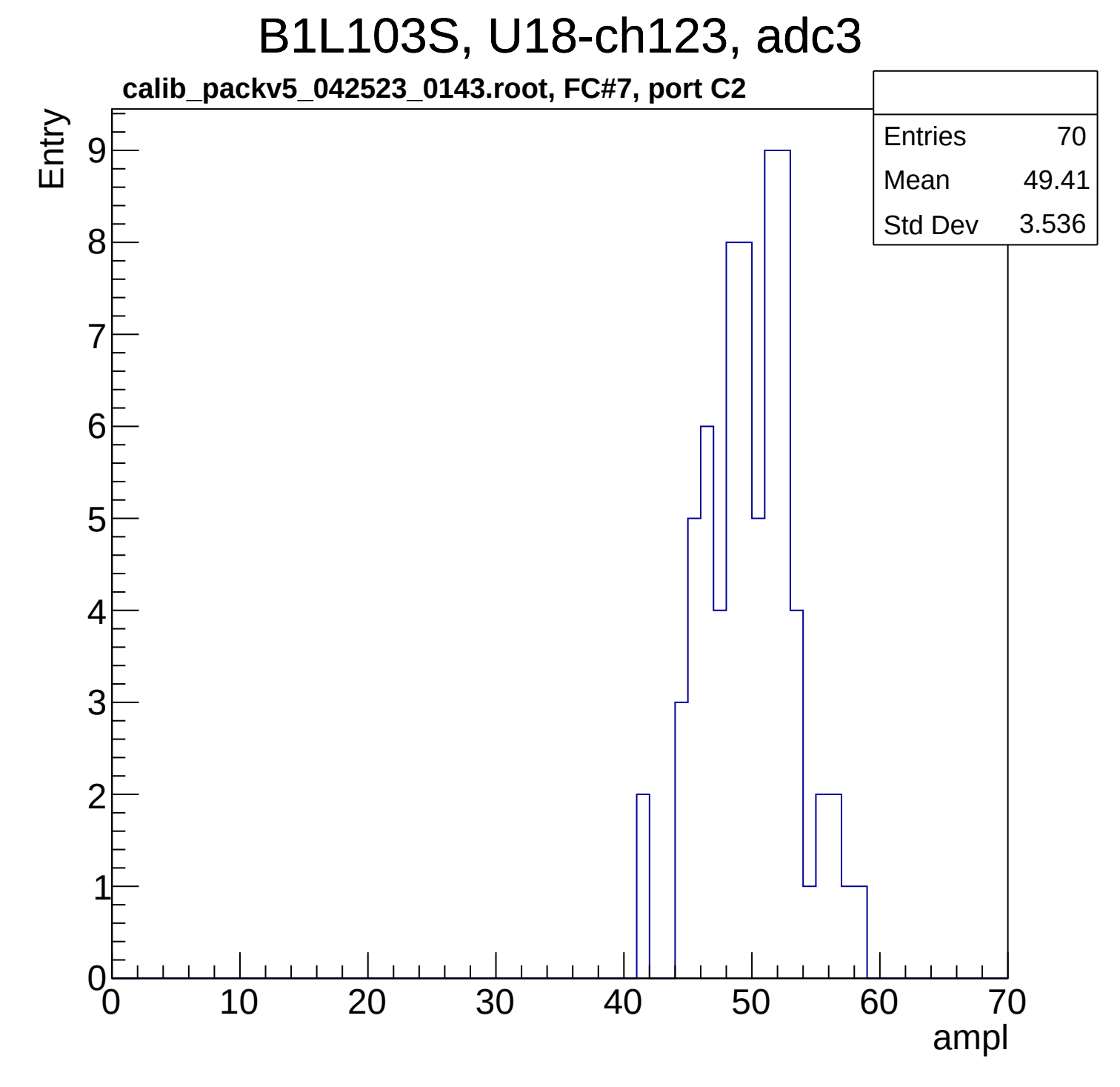

B1L103S, U18-ch123, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 42.8
Std Dev 3.649
Gaus mean : 43.6745
Gaus Width: 3.3537
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L103S, U18-ch123, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 49.41
Std Dev 3.536
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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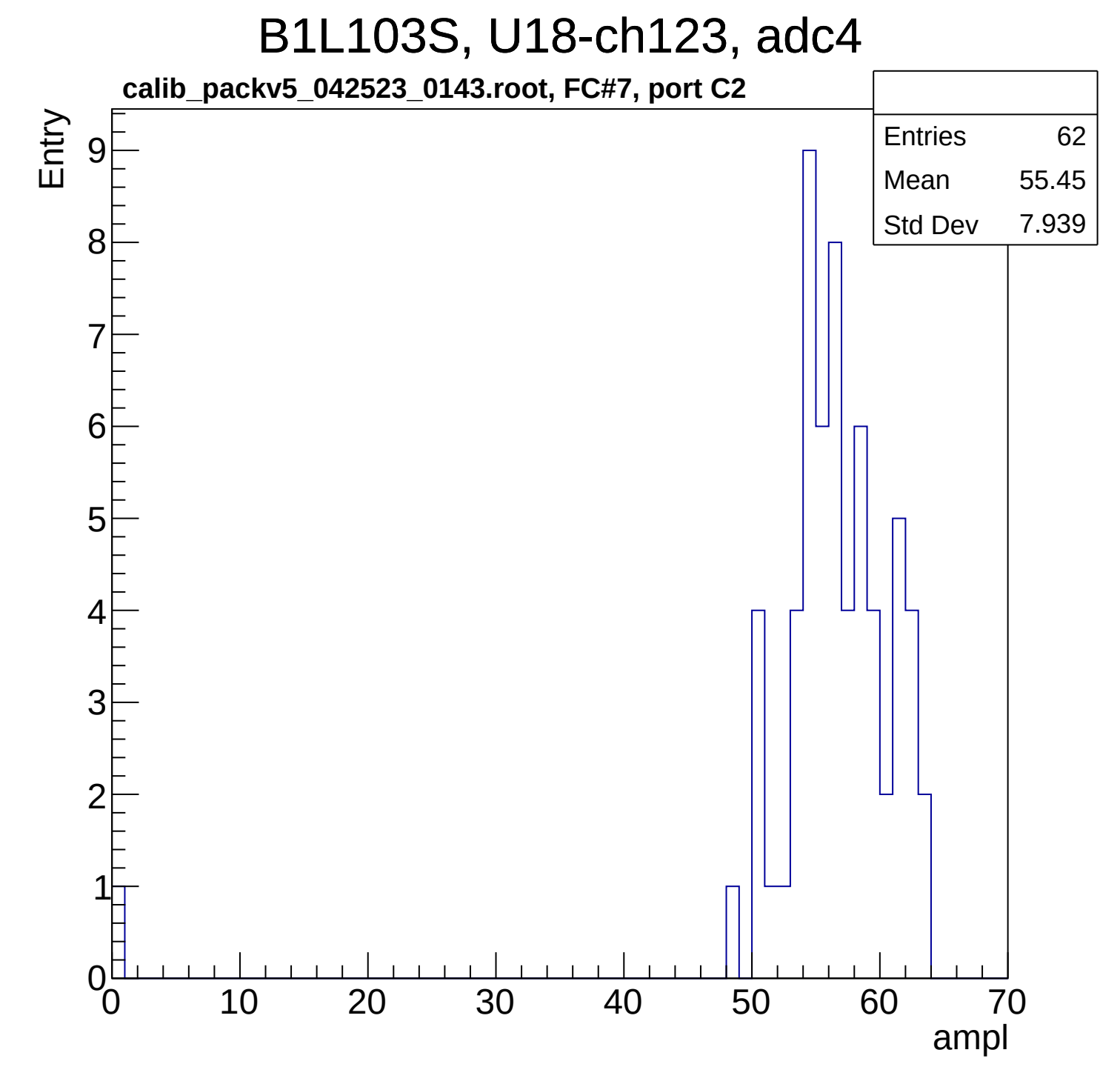
B1L103S, U18-ch123, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 62
Mean 55.45
Std Dev 7.939
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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20
30
40
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60
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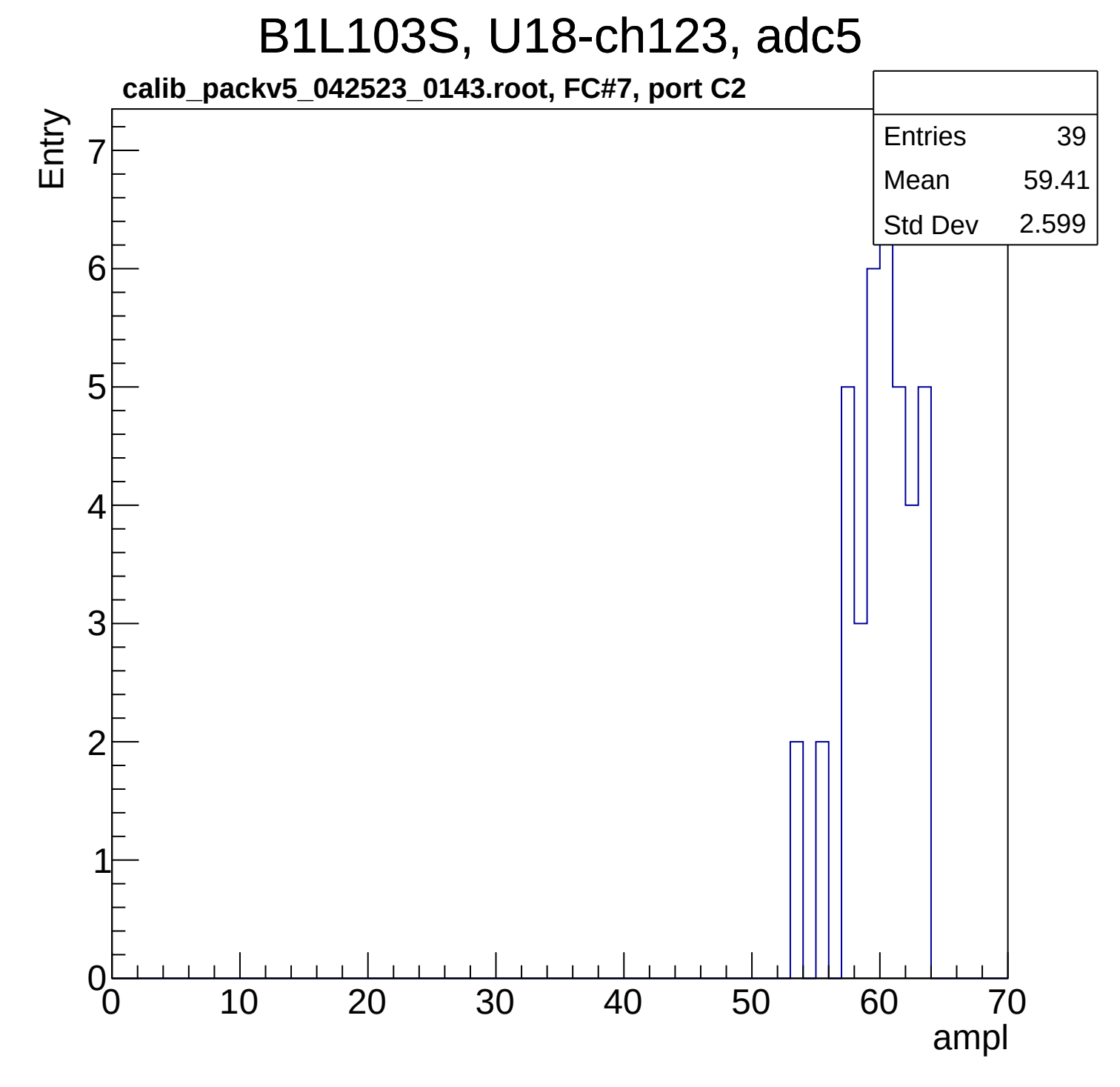
B1L103S, U18-ch123, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 39
Mean 59.41
Std Dev 2.599
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
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60
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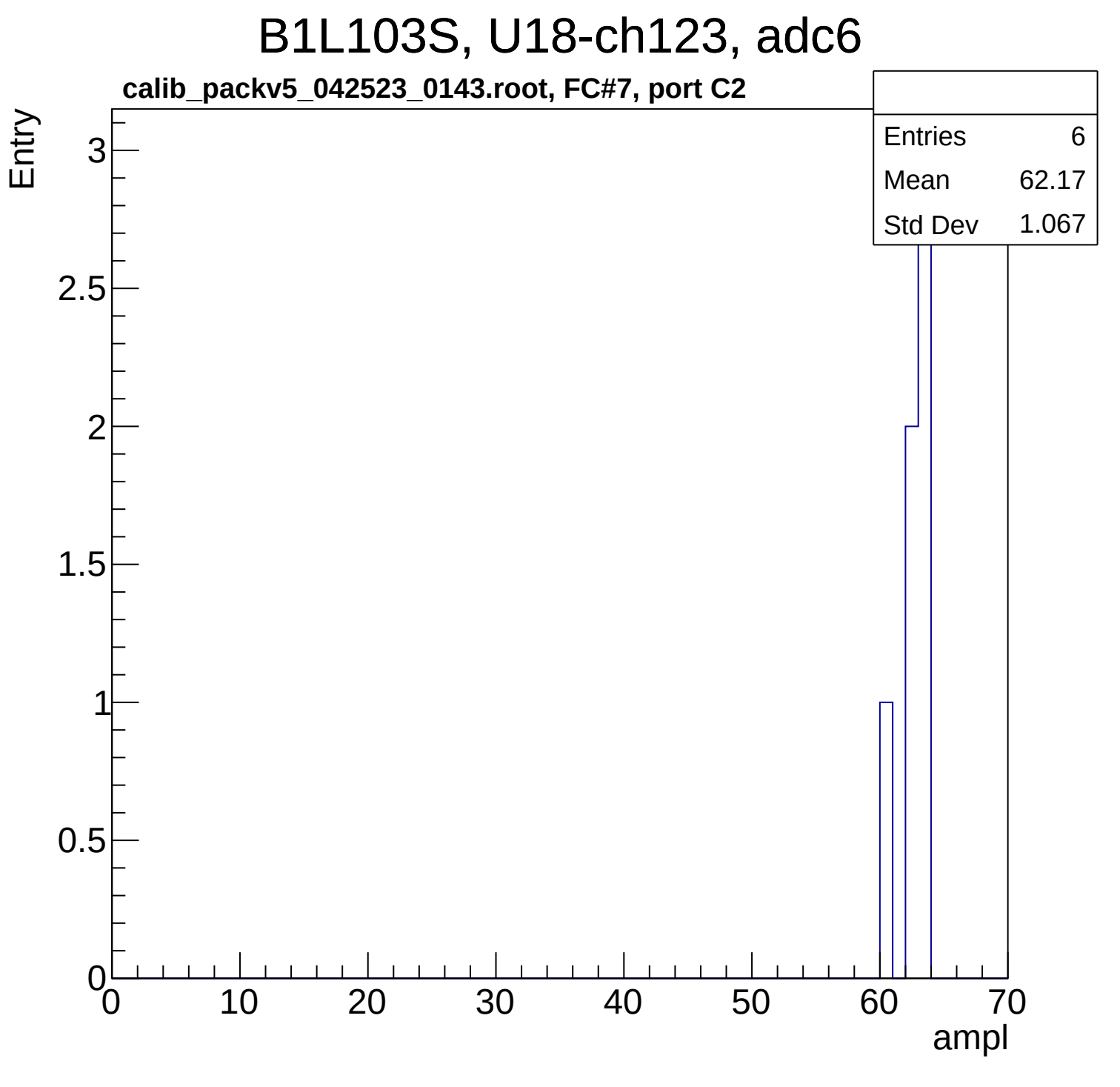
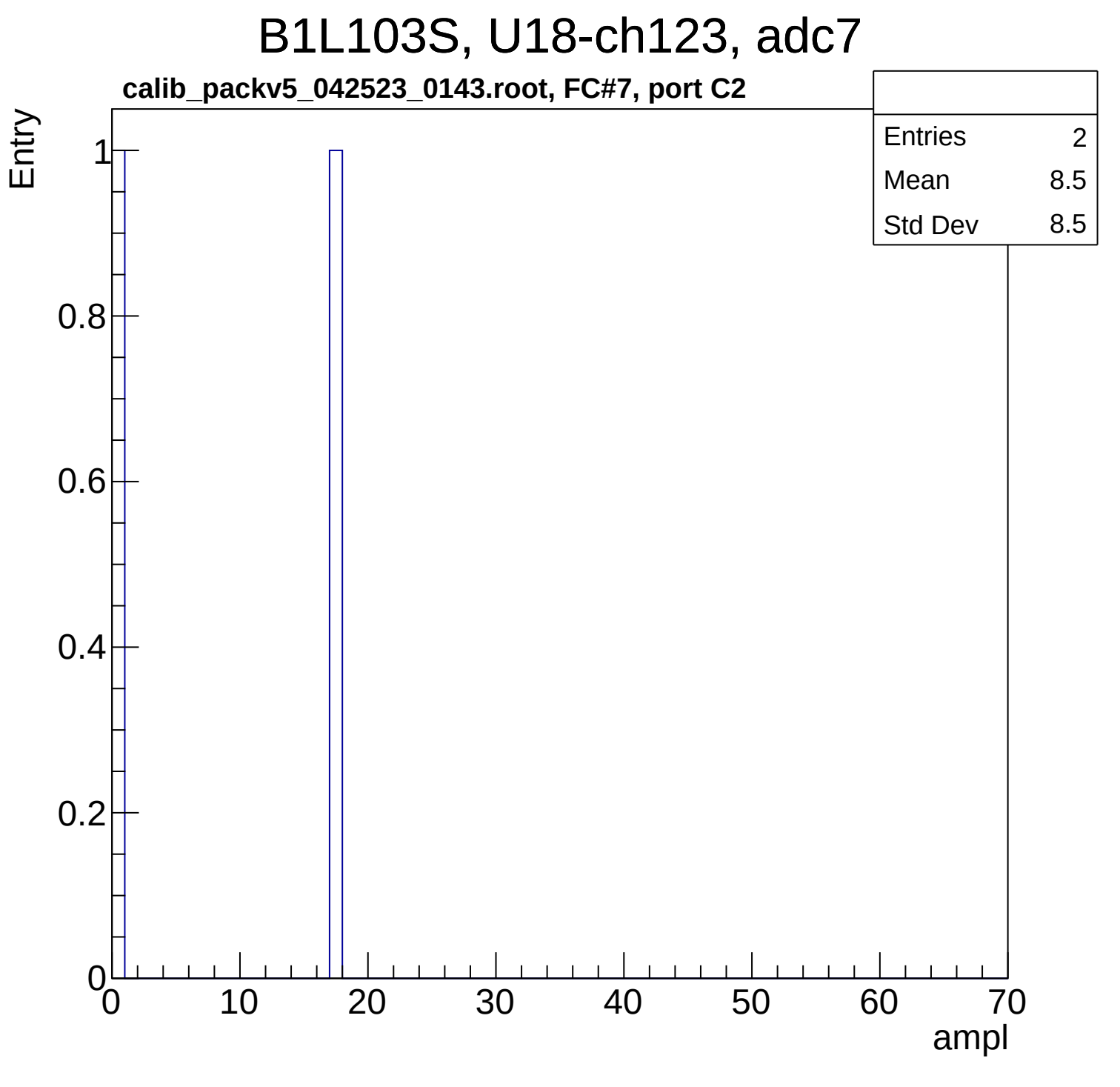
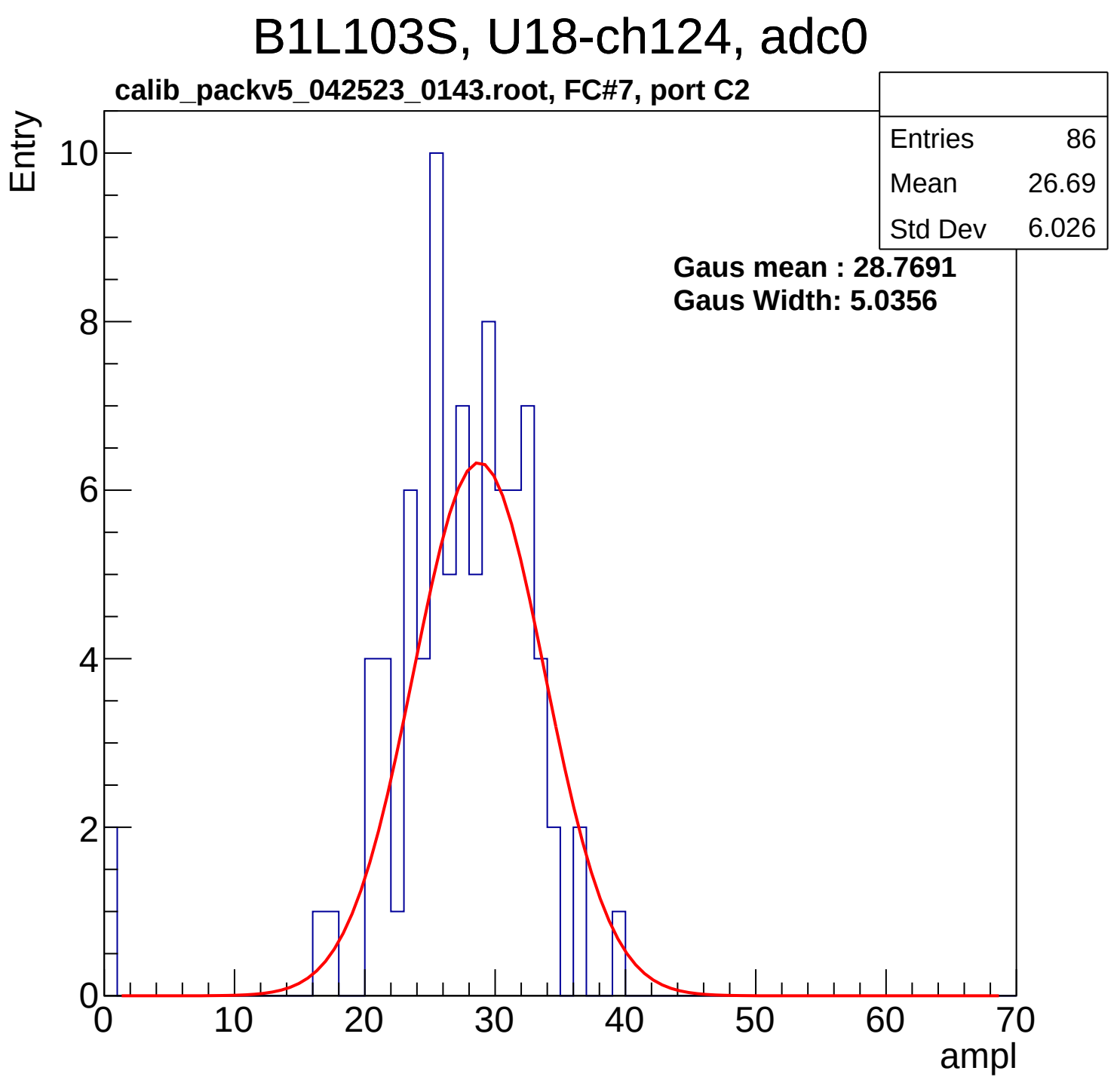
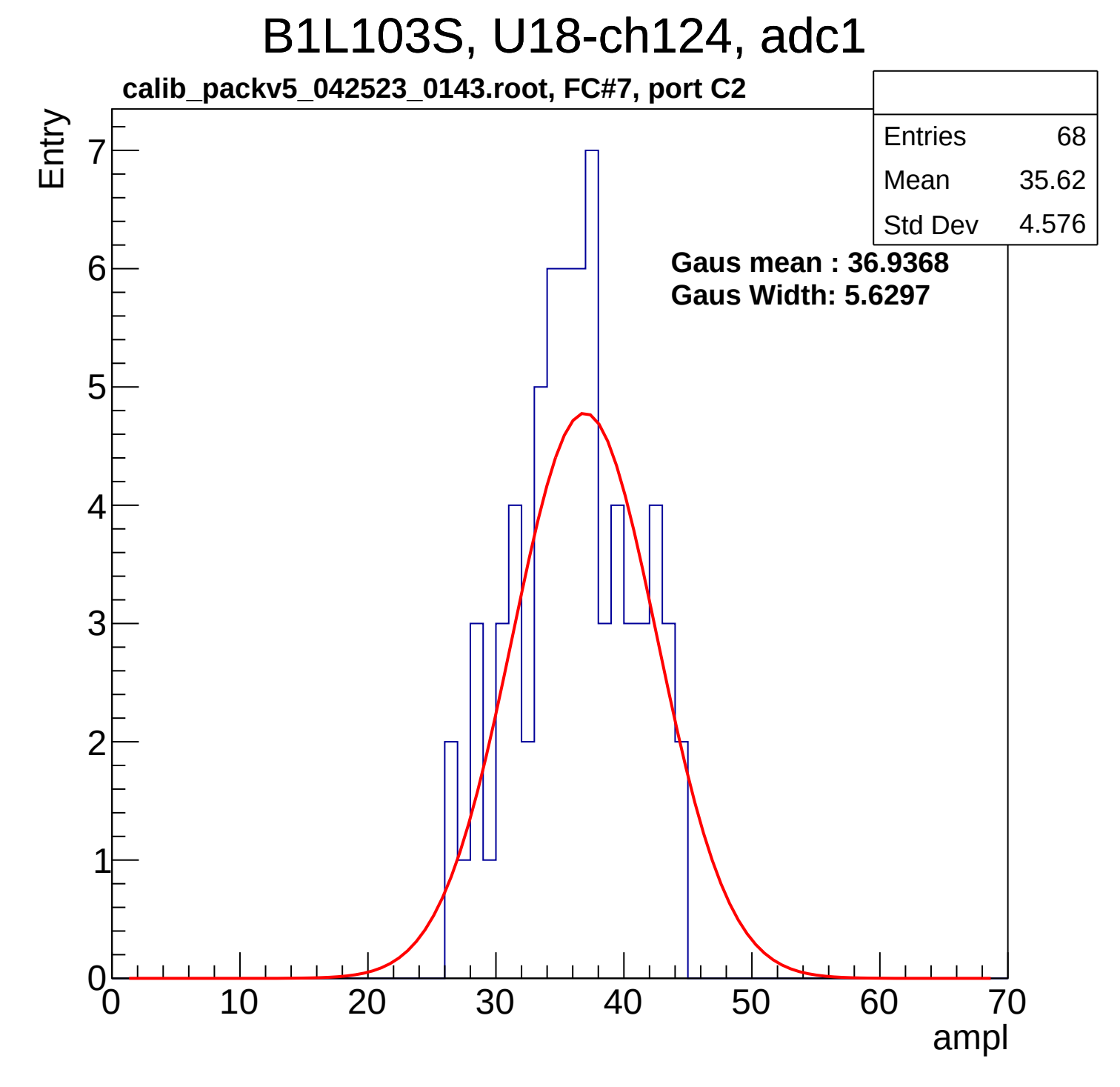
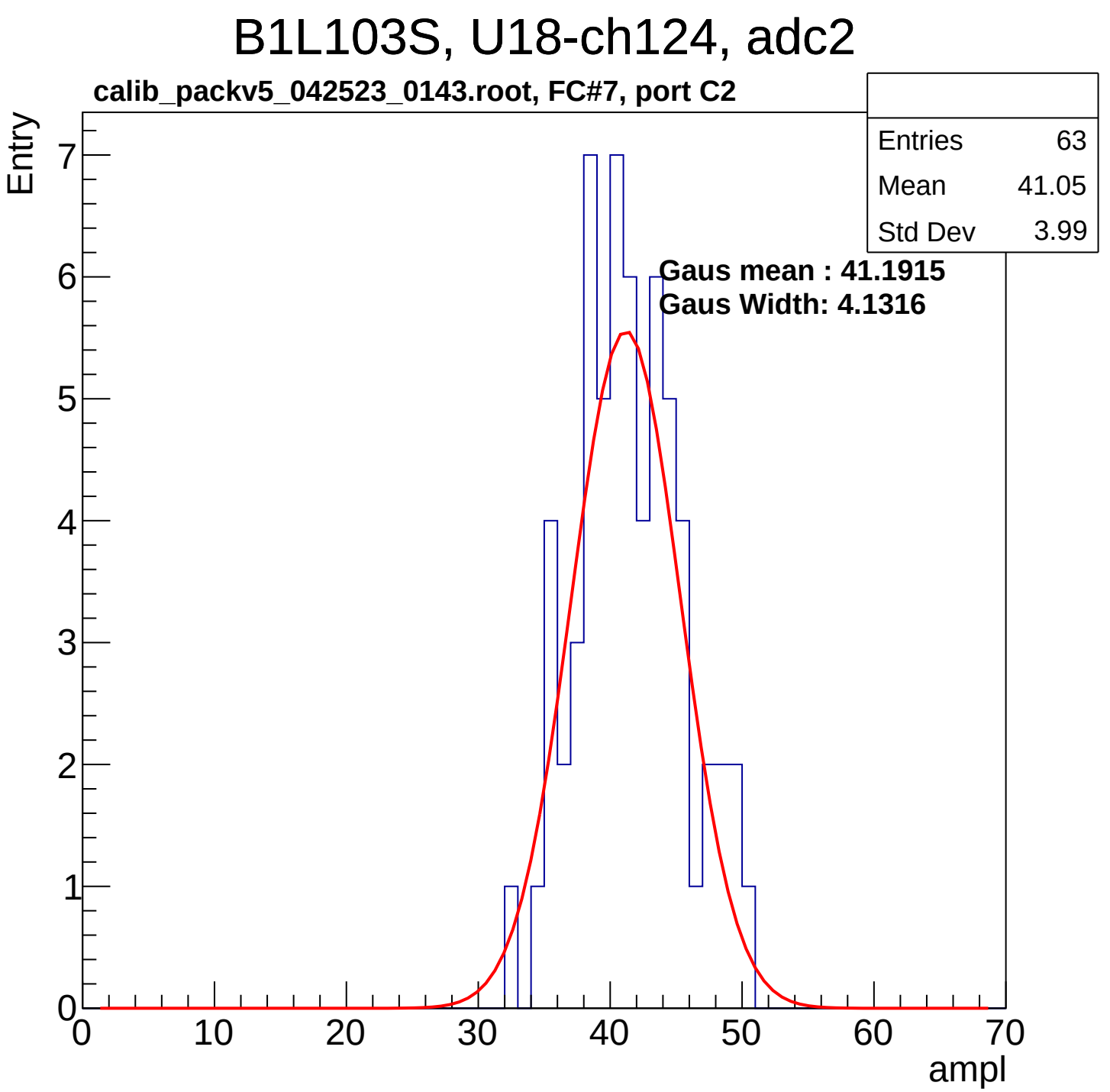
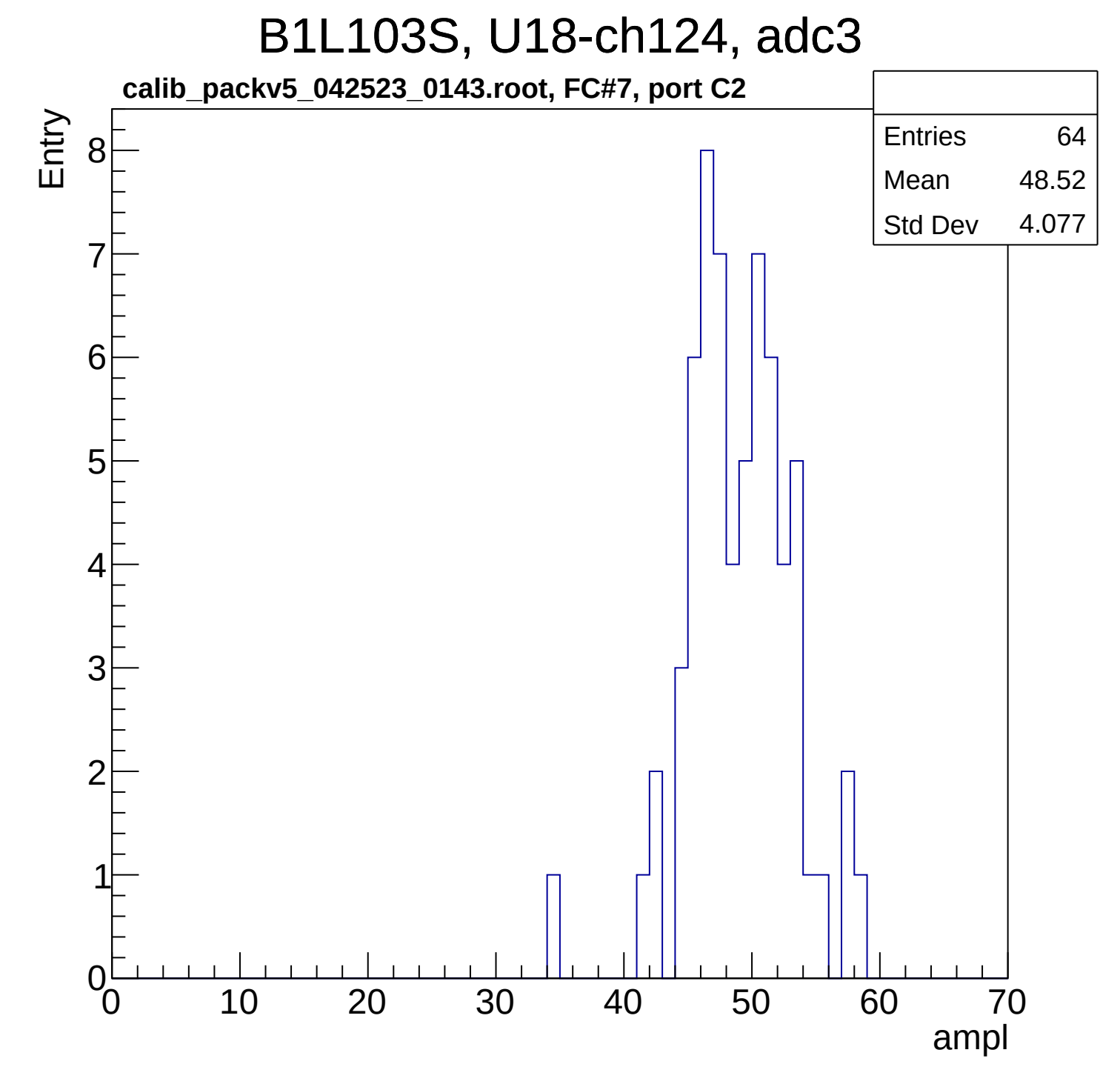

B1L103S, U18-ch123, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 6
Mean 62.17
Std Dev 1.067
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U18-ch123, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 8.5
Std Dev 8.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch124, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 86
Mean 26.69
Std Dev 6.026
Gaus mean : 28.7691
Gaus Width: 5.0356
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch124, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 35.62
Std Dev 4.576
Gaus mean : 36.9368
Gaus Width: 5.6297
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch124, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 41.05
Std Dev 3.99
Gaus mean : 41.1915
Gaus Width: 4.1316
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch124, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 48.52
Std Dev 4.077
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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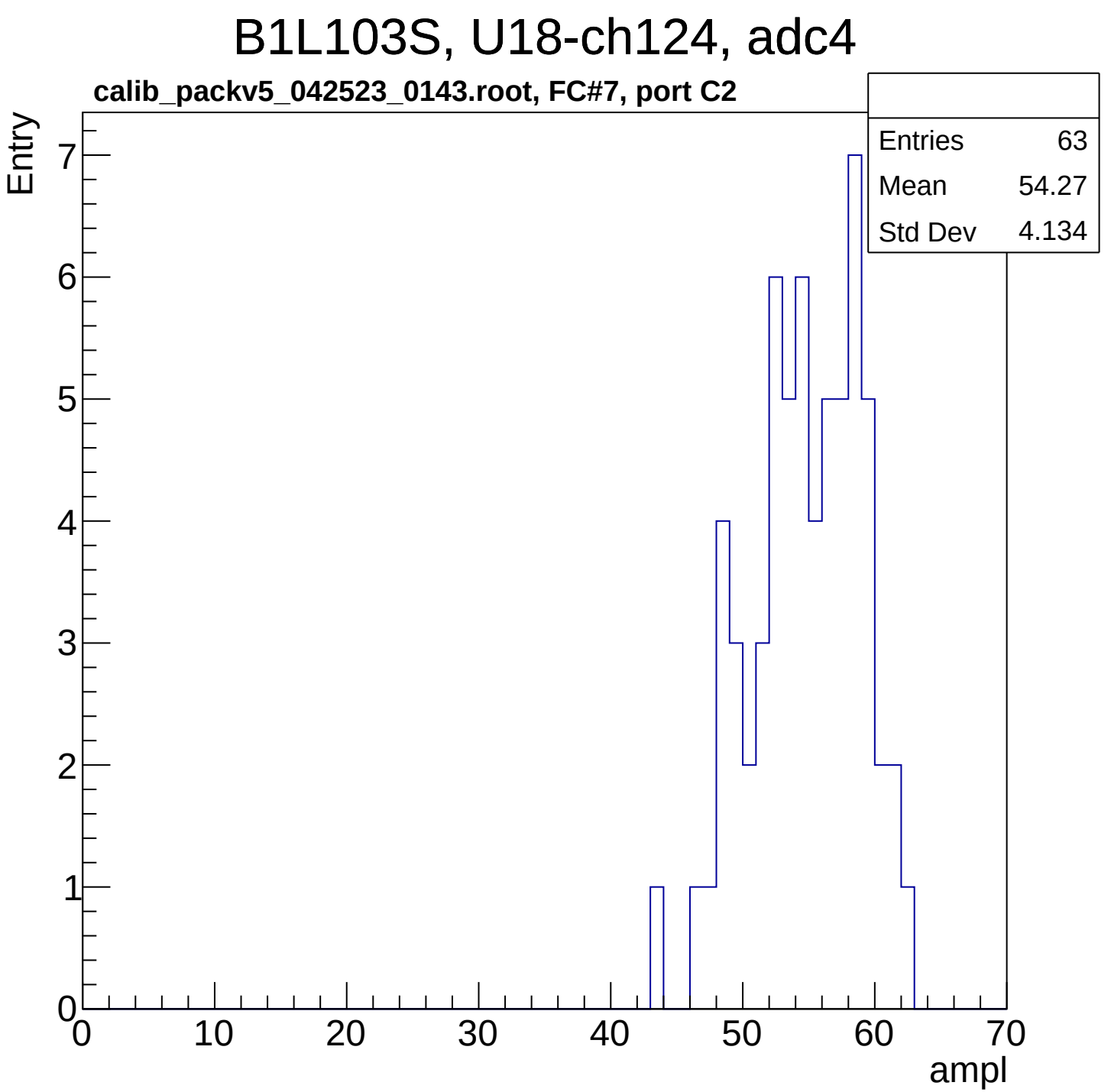
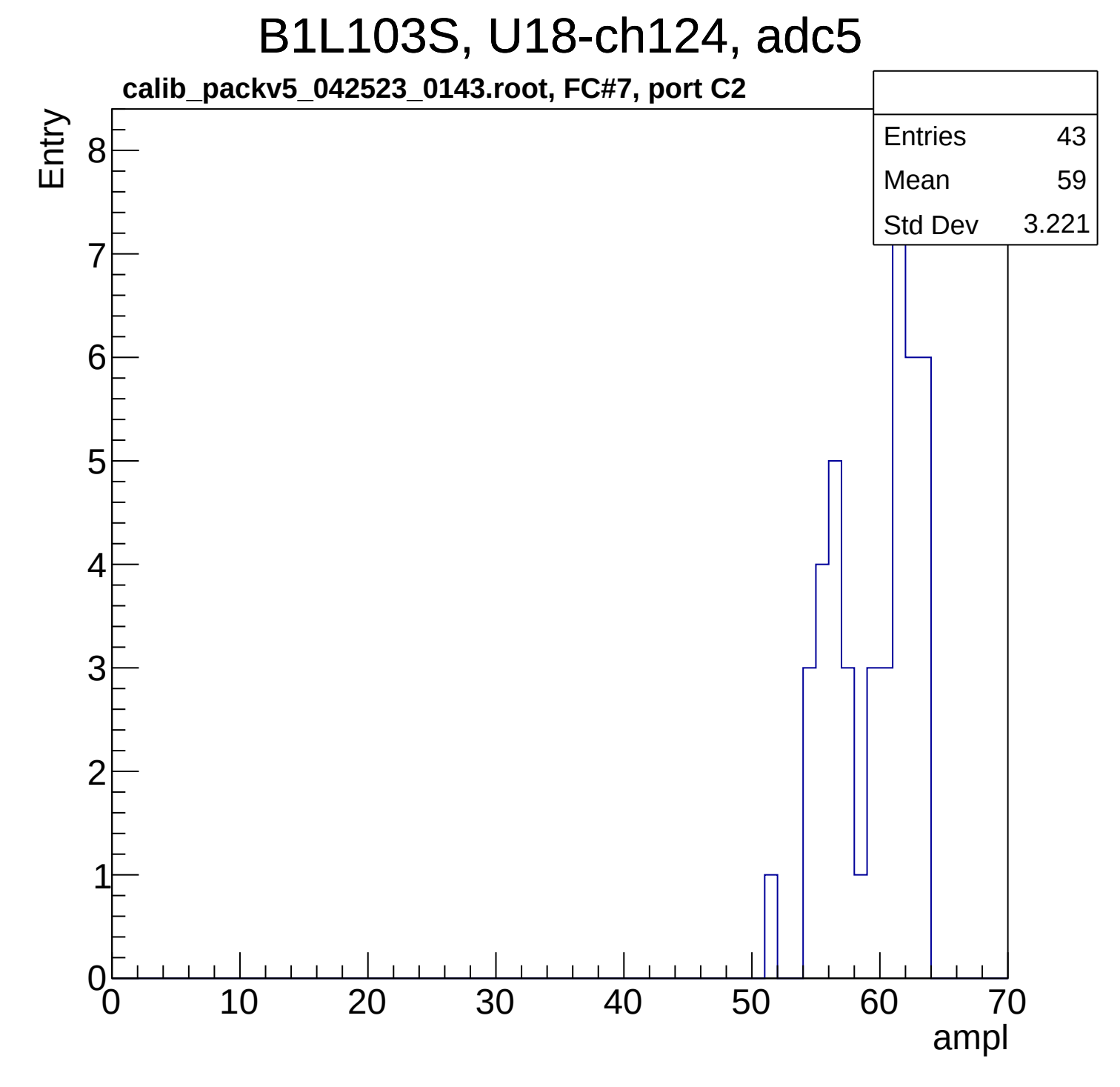
40
50
60
70


B1L103S, U18-ch124, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 54.27
Std Dev 4.134
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch124, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 43
Mean 59
Std Dev 3.221
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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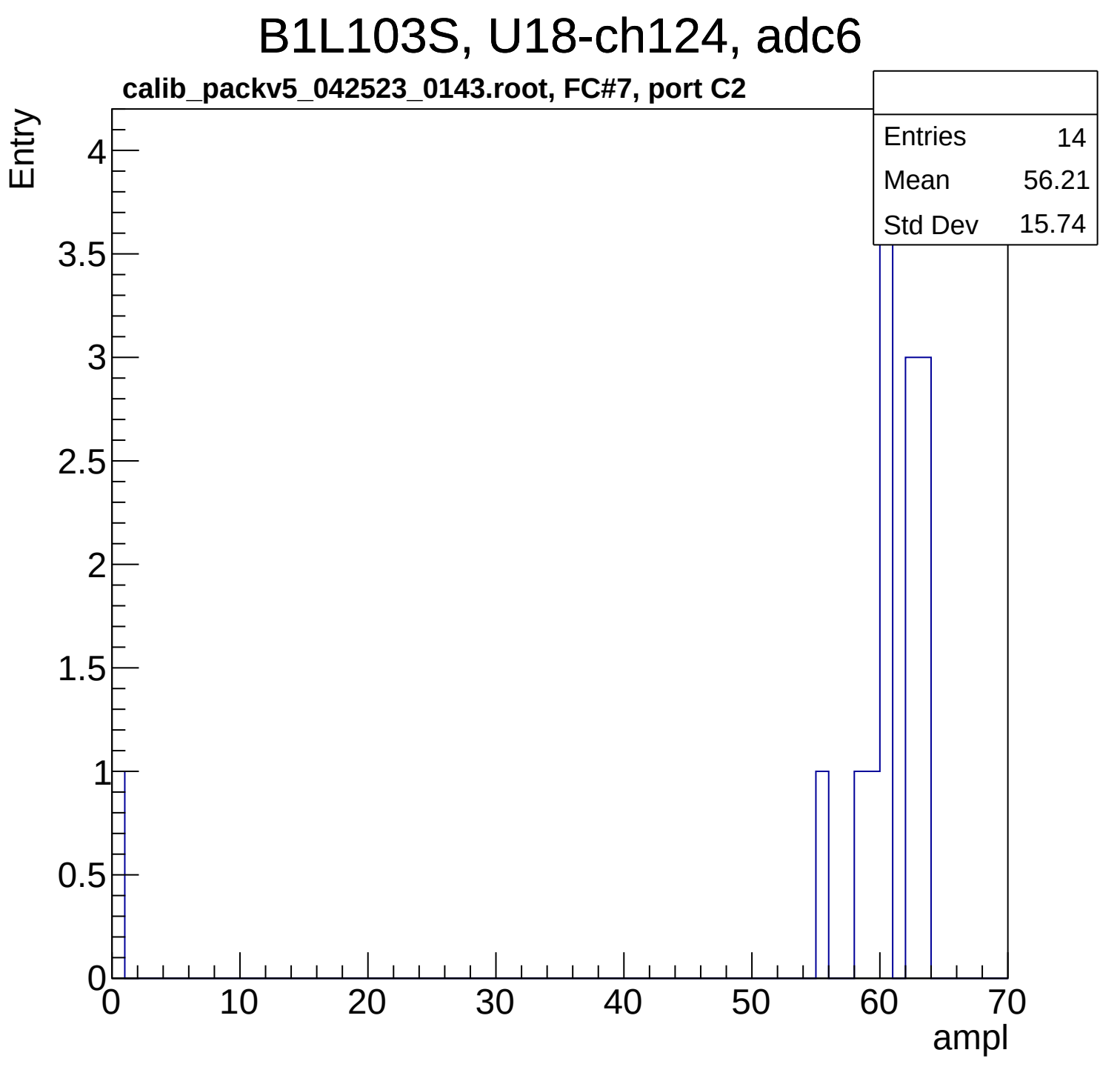
B1L103S, U18-ch124, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 14
Mean 56.21
Std Dev 15.74
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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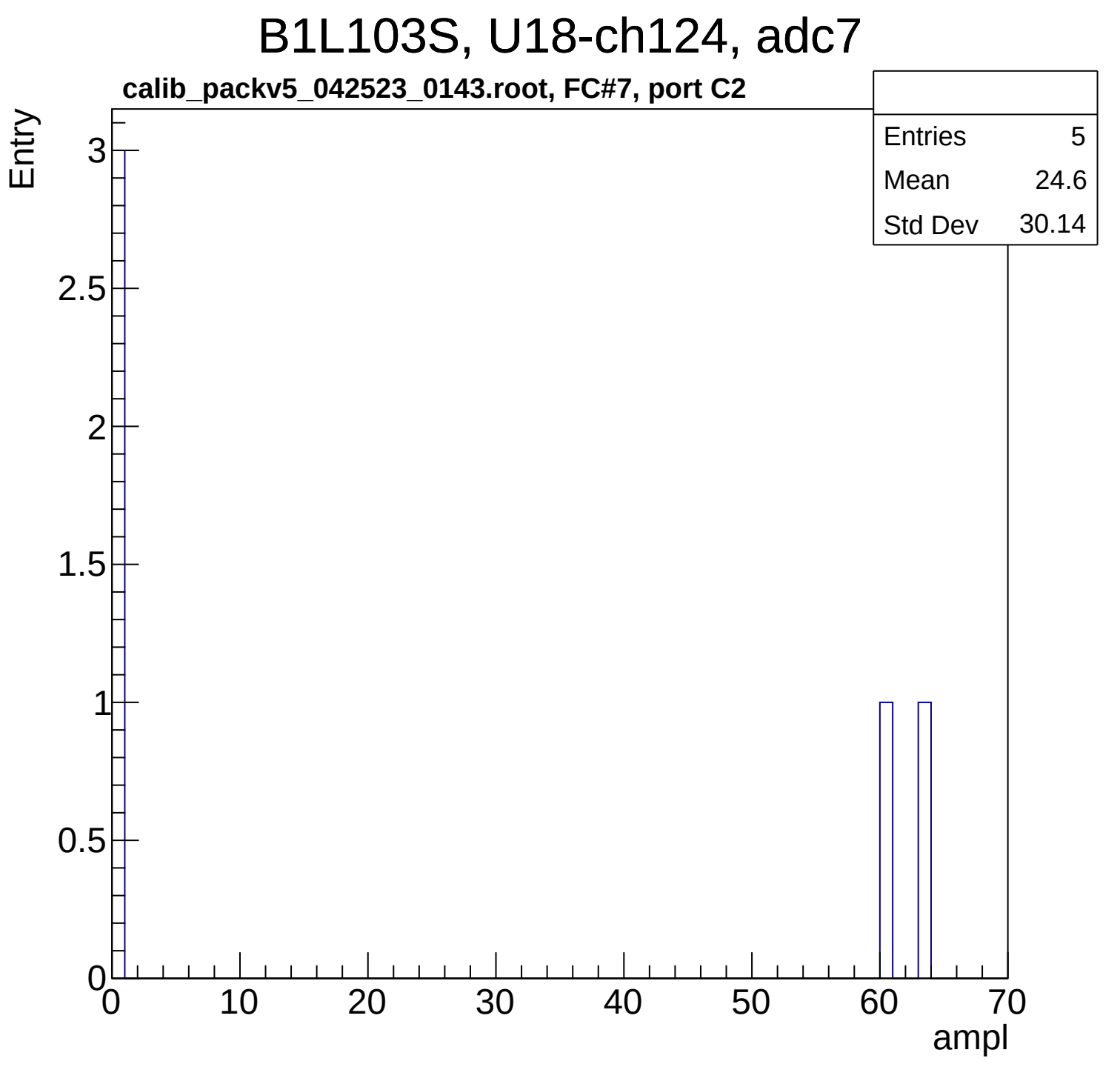
40
50
60
70


B1L103S, U18-ch124, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 5
Mean 24.6
Std Dev 30.14
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
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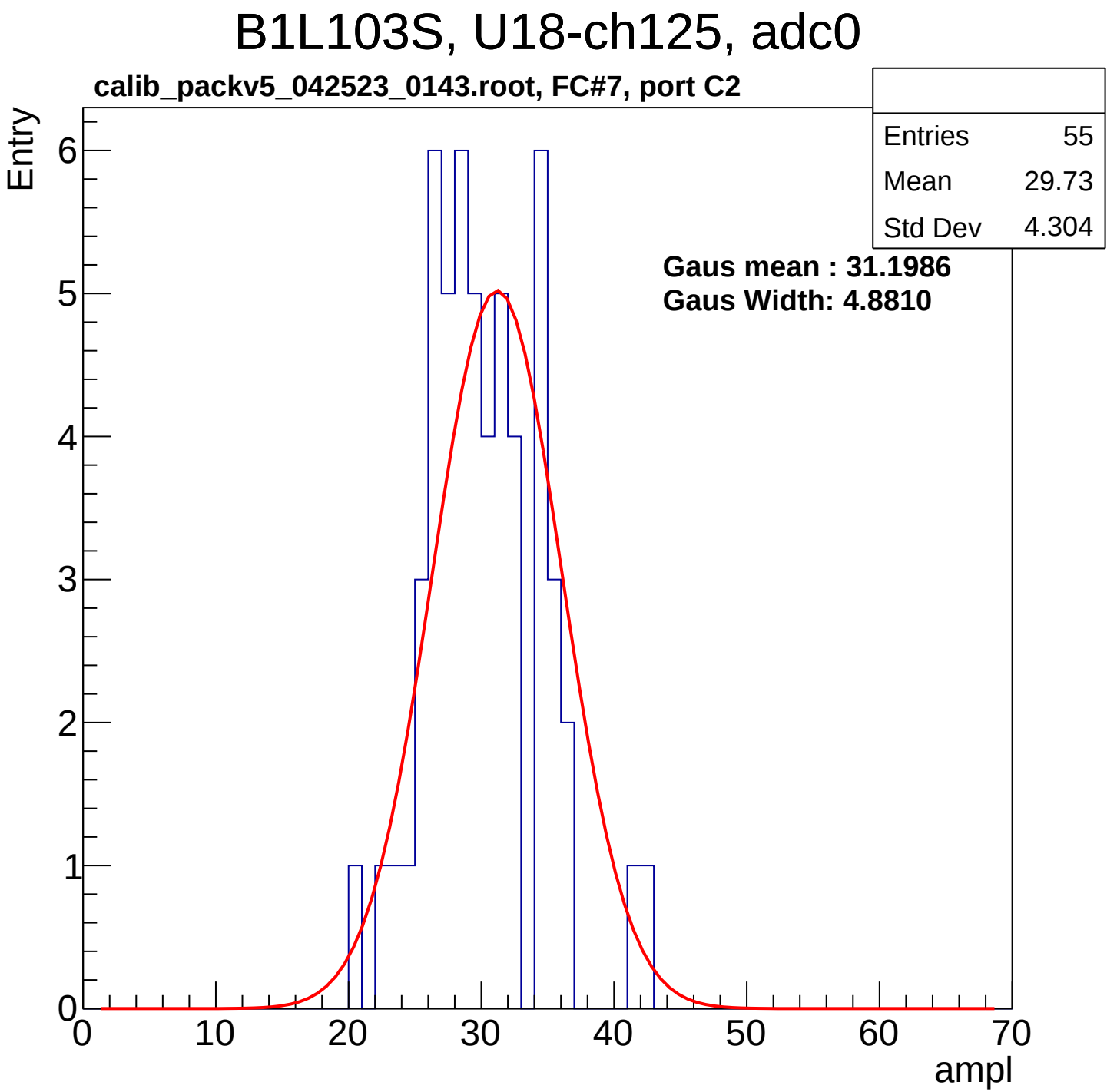
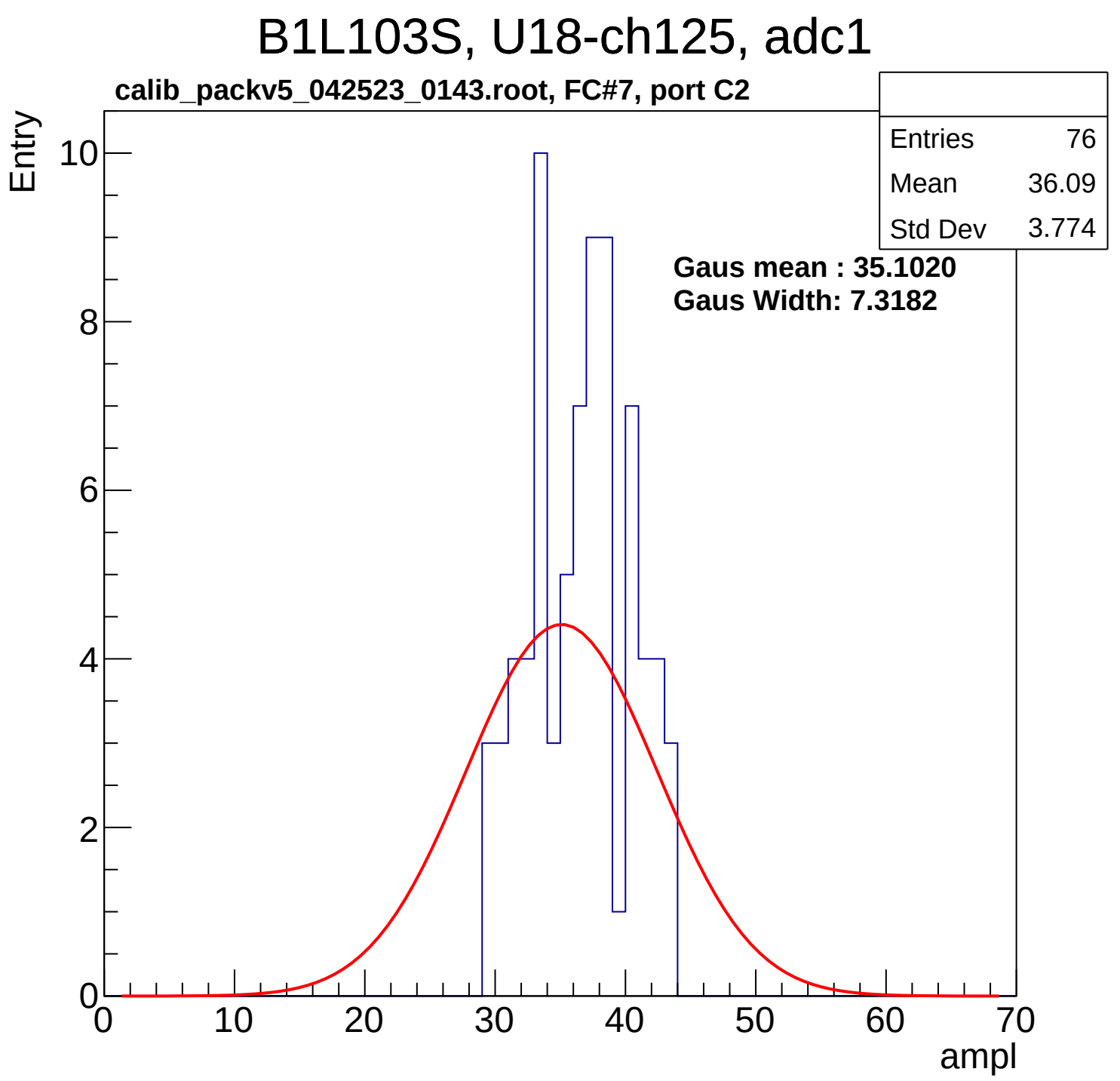
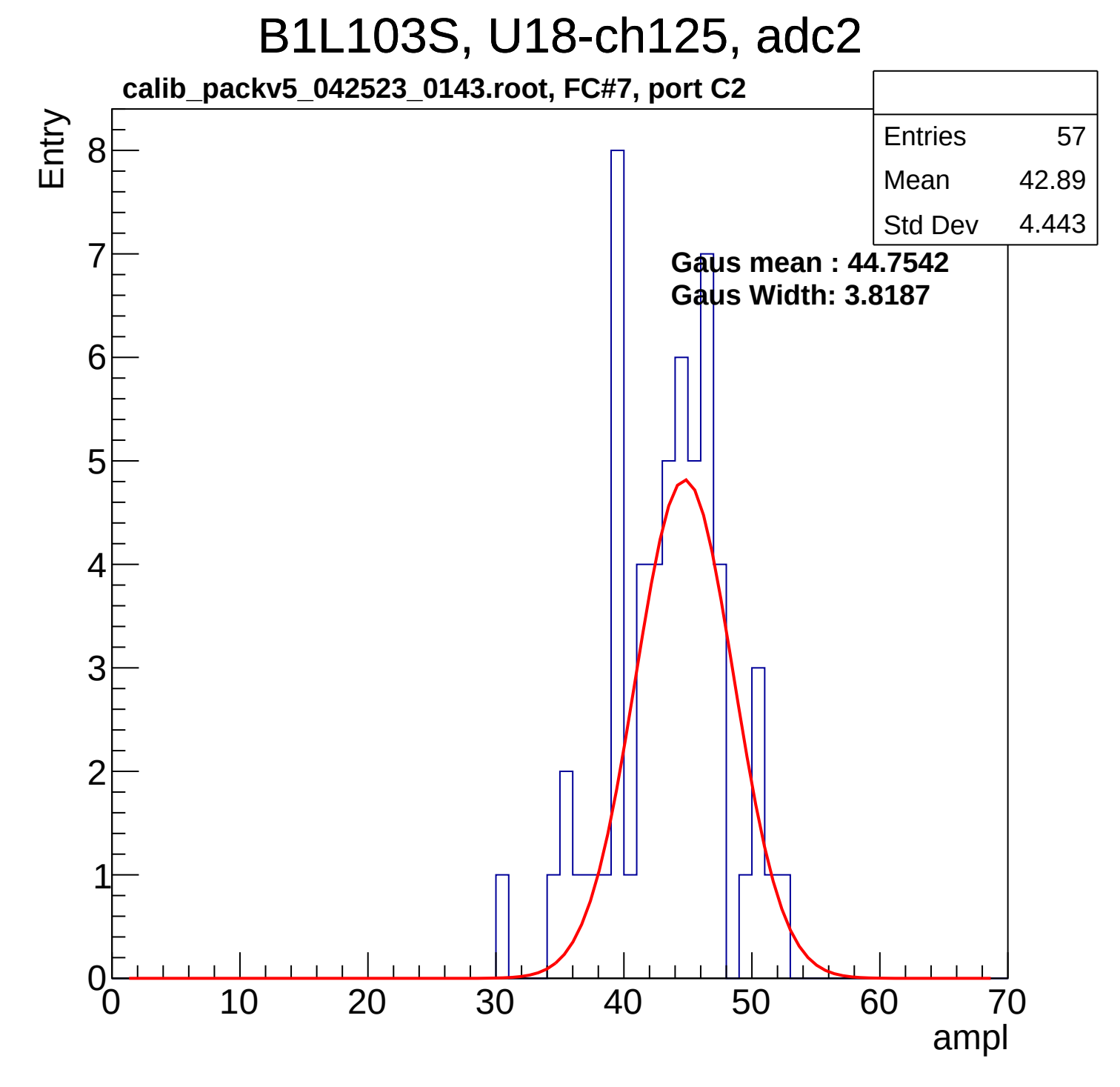

B1L103S, U18-ch125, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 29.73
Std Dev 4.304
Gaus mean : 31.1986
Gaus Width: 4.8810
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U18-ch125, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 76
Mean 36.09
Std Dev 3.774
Gaus mean : 35.1020
Gaus Width: 7.3182
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch125, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 42.89
Std Dev 4.443
Gaus mean : 44.7542
Gaus Width: 3.8187
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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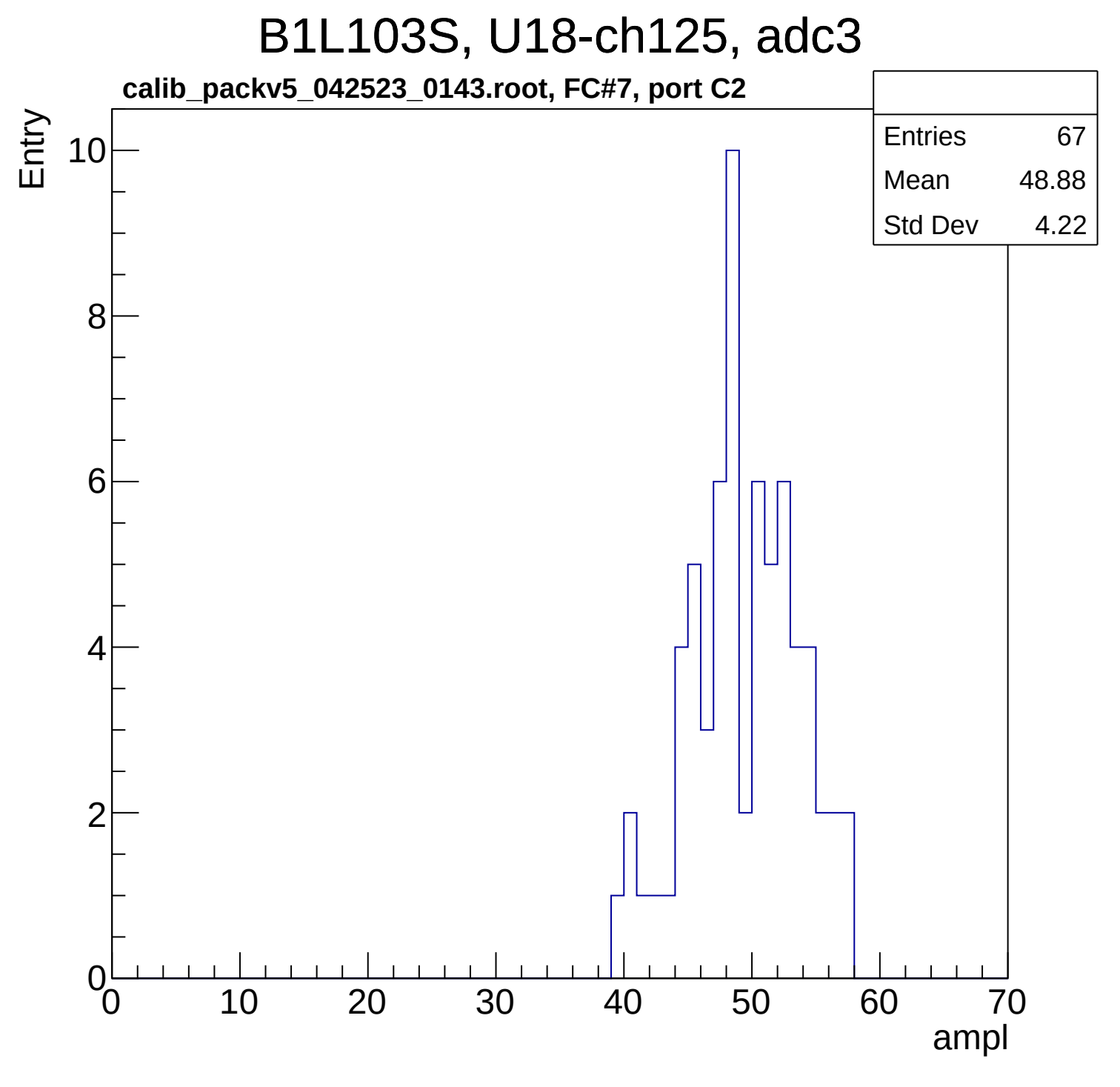
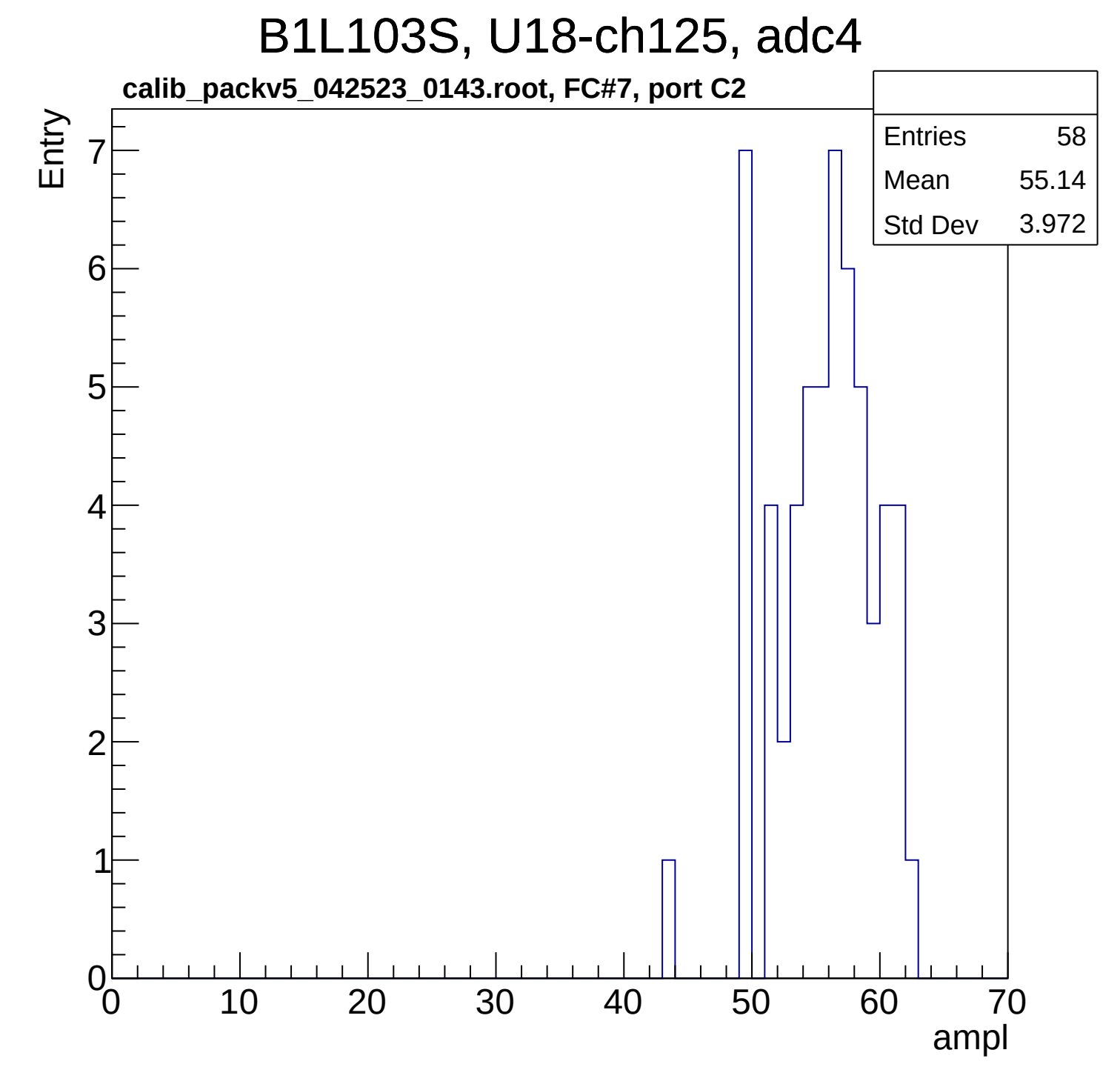
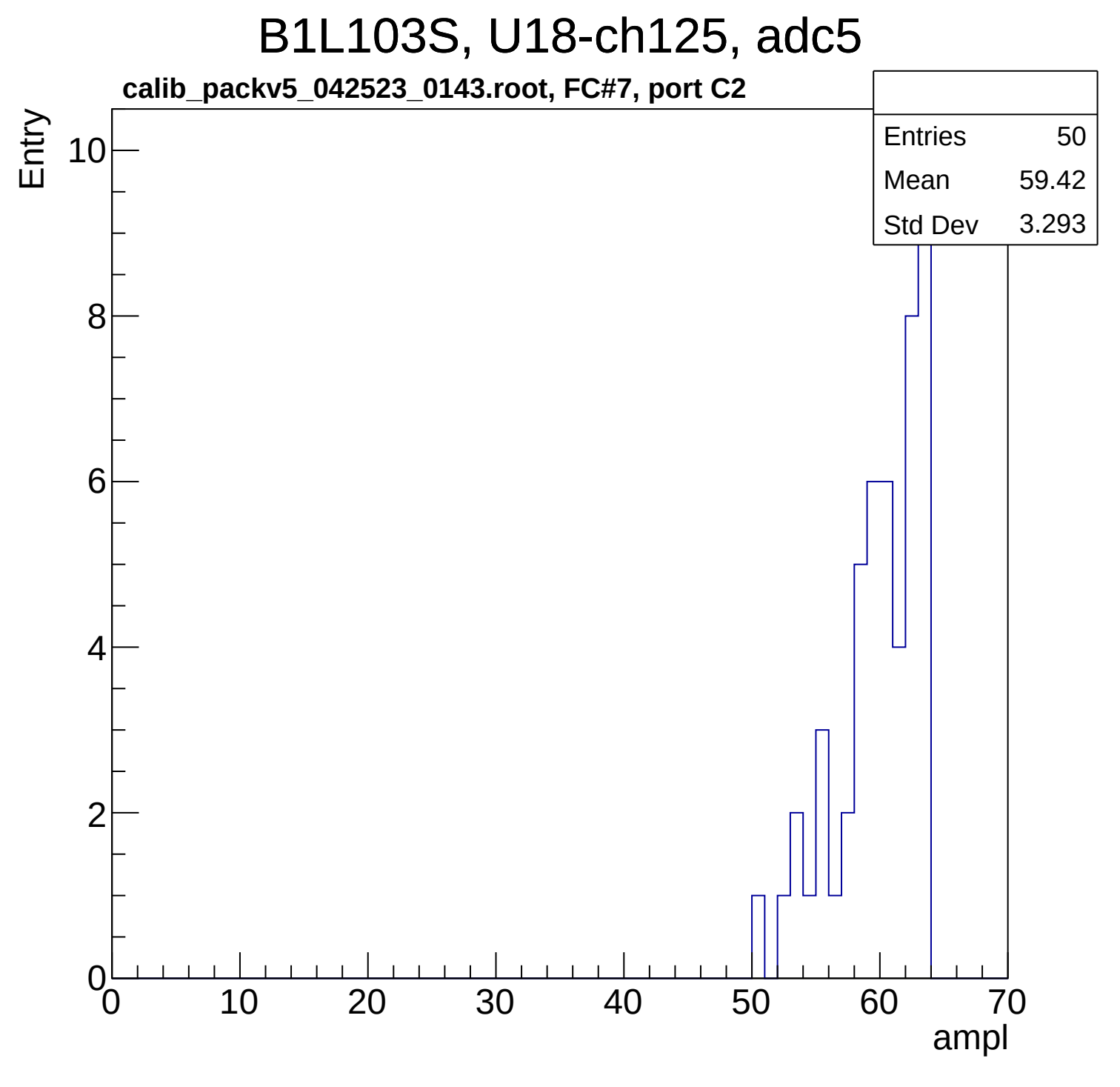
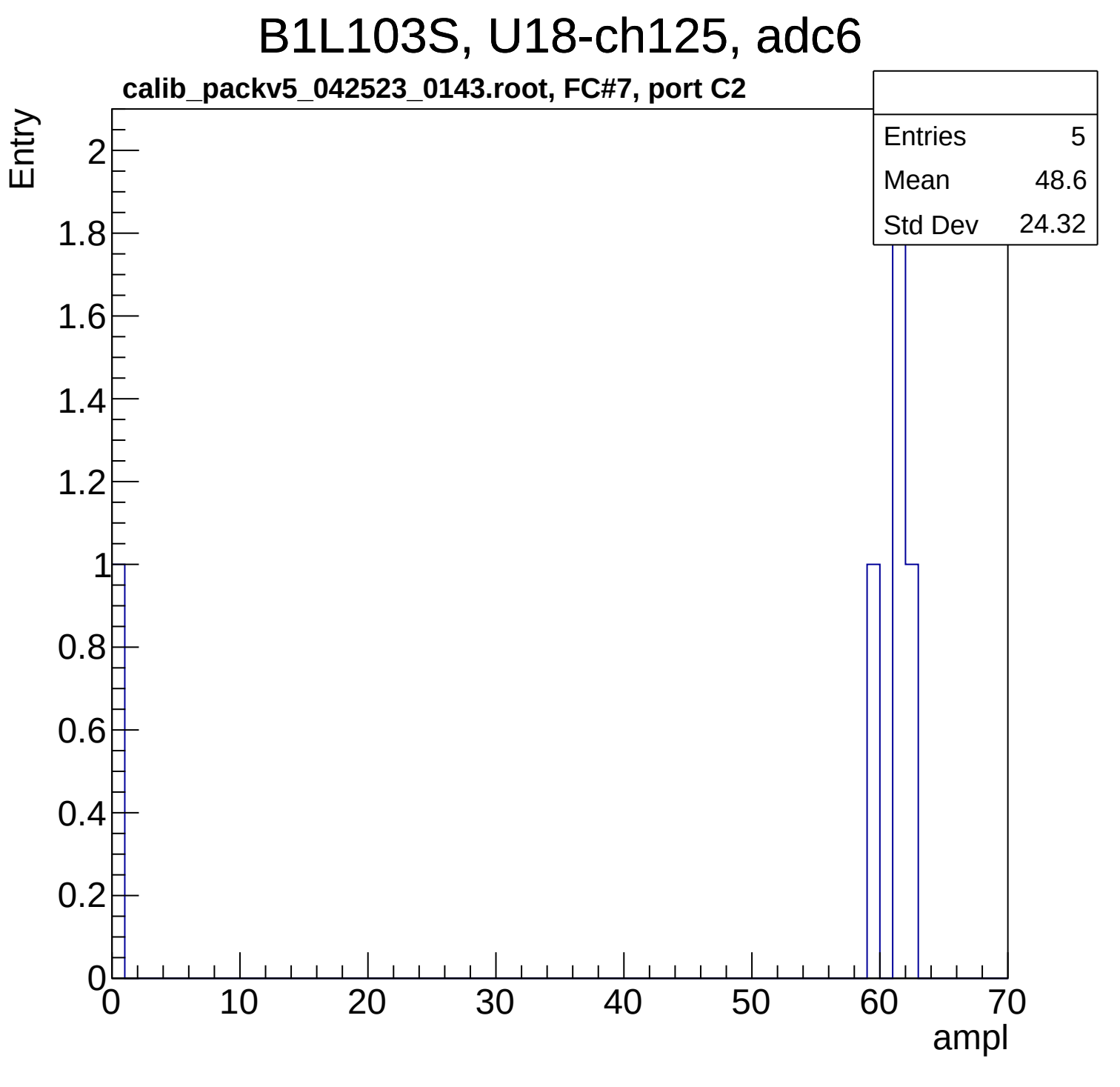

B1L103S, U18-ch125, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 48.88
Std Dev 4.22
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch125, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 58
Mean 55.14
Std Dev 3.972
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch125, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 50
Mean 59.42
Std Dev 3.293
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch125, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 5
Mean 48.6
Std Dev 24.32
Entry
ampl
0
0.2
0.4
0.6
0.8
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1.2
1.4
1.6
1.8
2
0
10
20
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40
50
60
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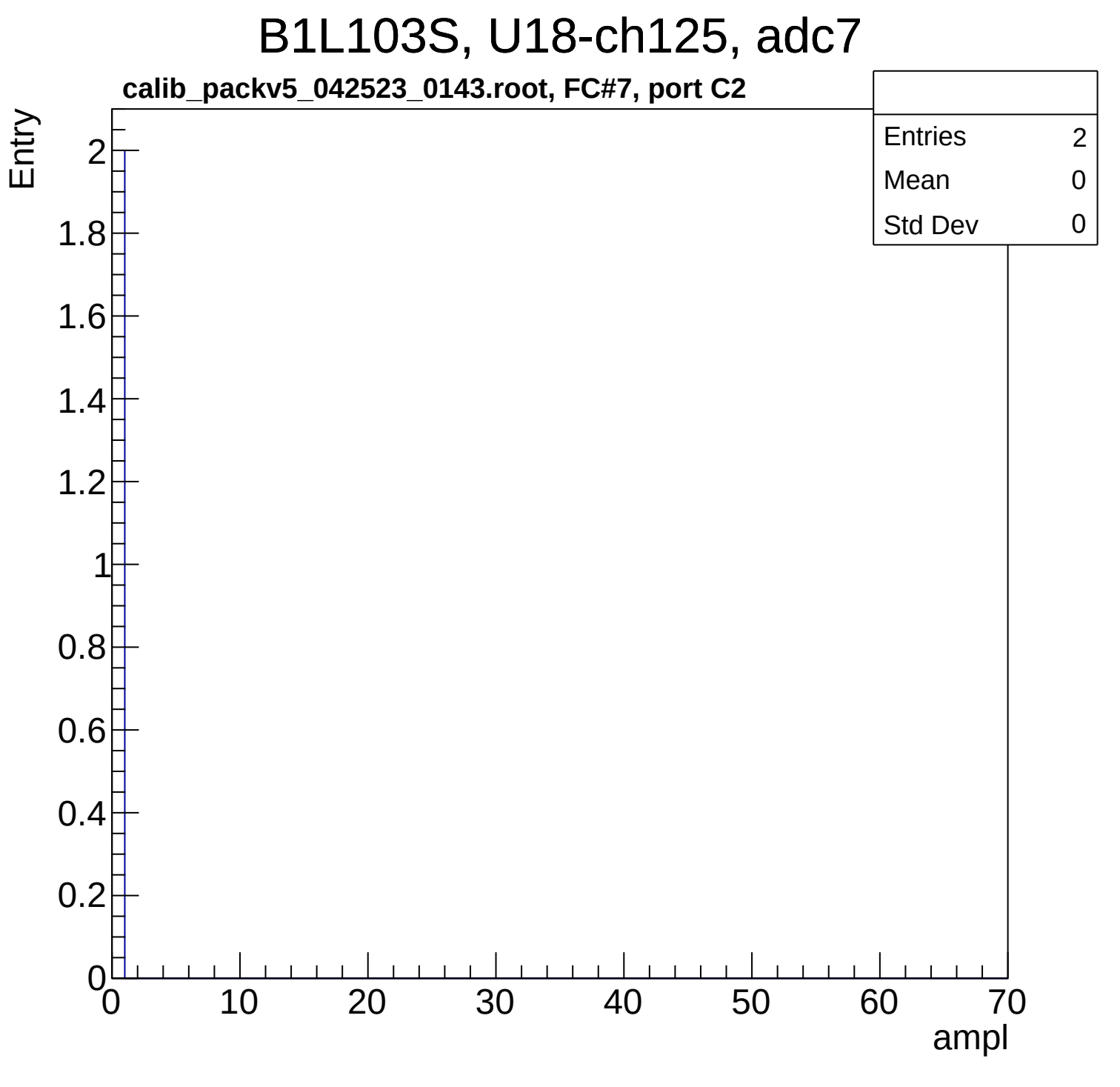
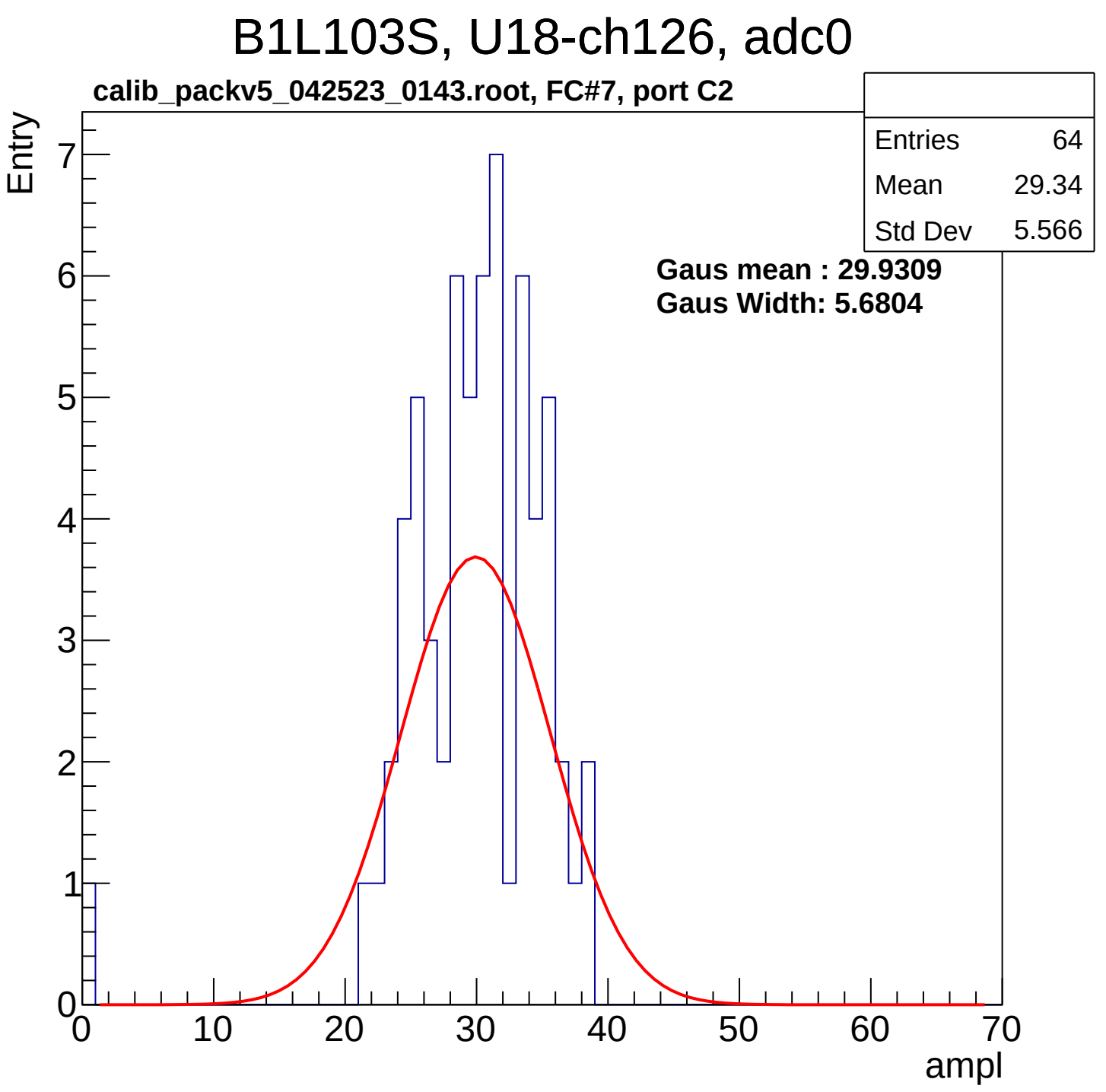
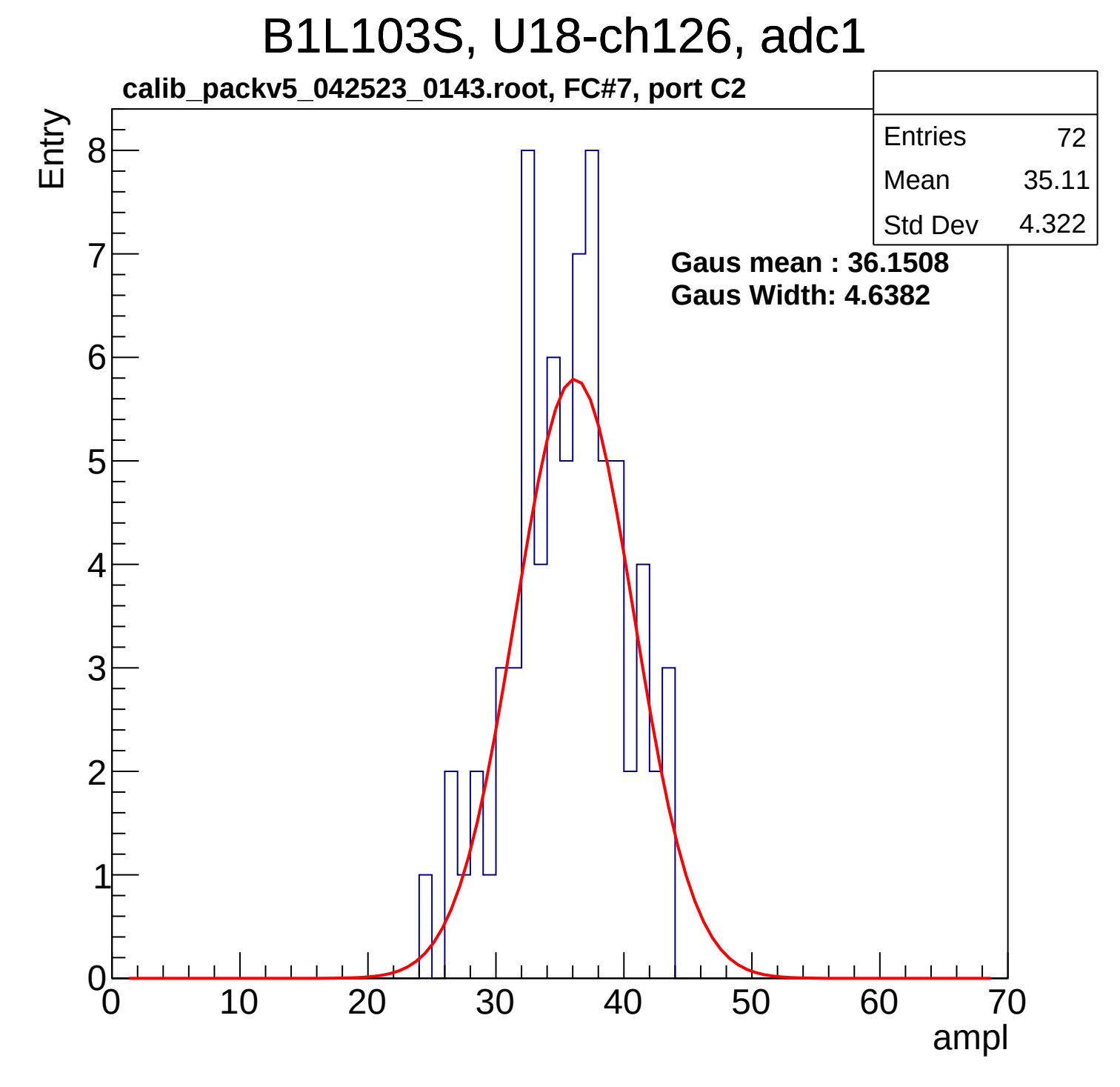

B1L103S, U18-ch125, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch126, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 29.34
Std Dev 5.566
Gaus mean : 29.9309
Gaus Width: 5.6804
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch126, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 72
Mean 35.11
Std Dev 4.322
Gaus mean : 36.1508
Gaus Width: 4.6382
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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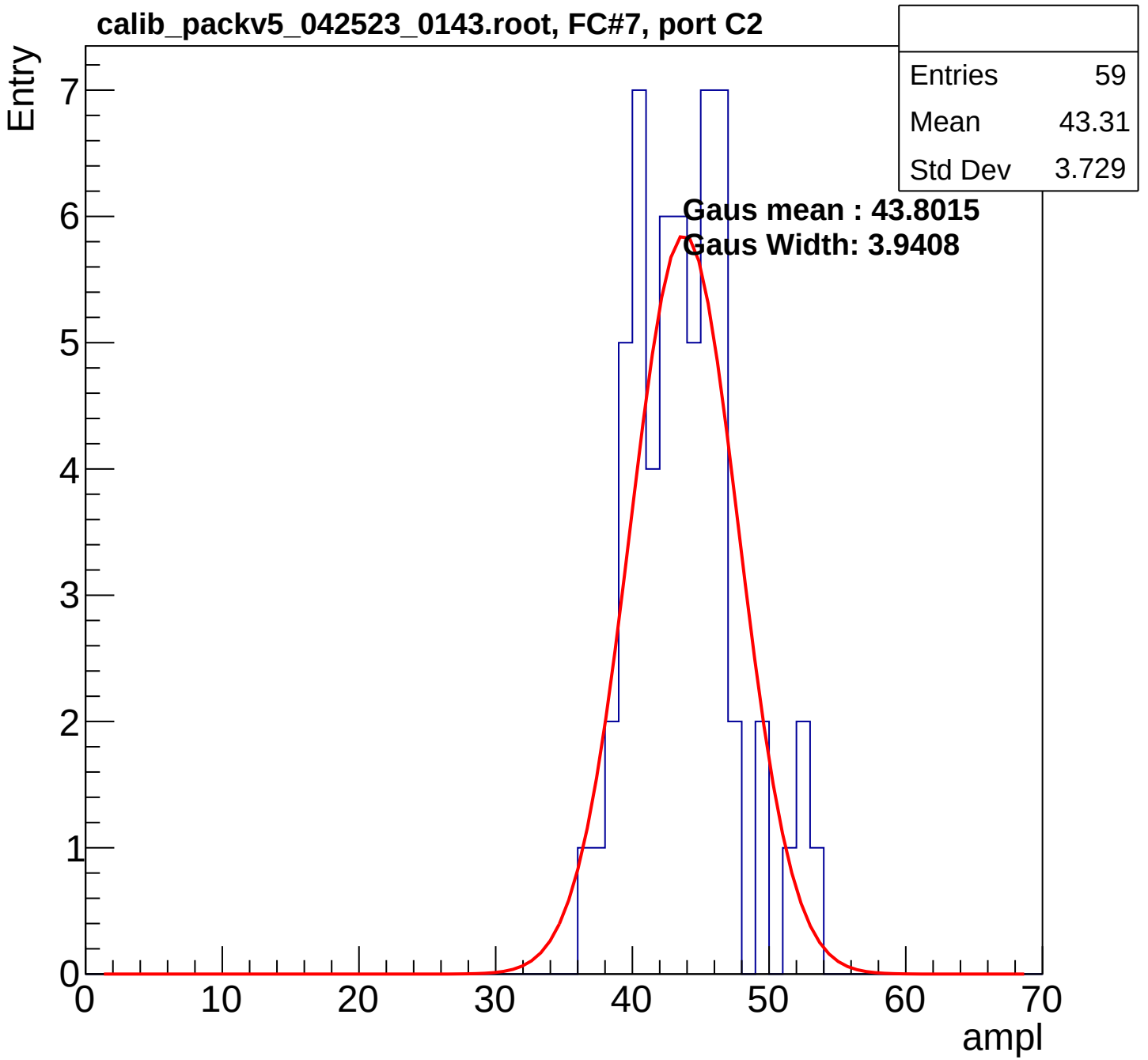
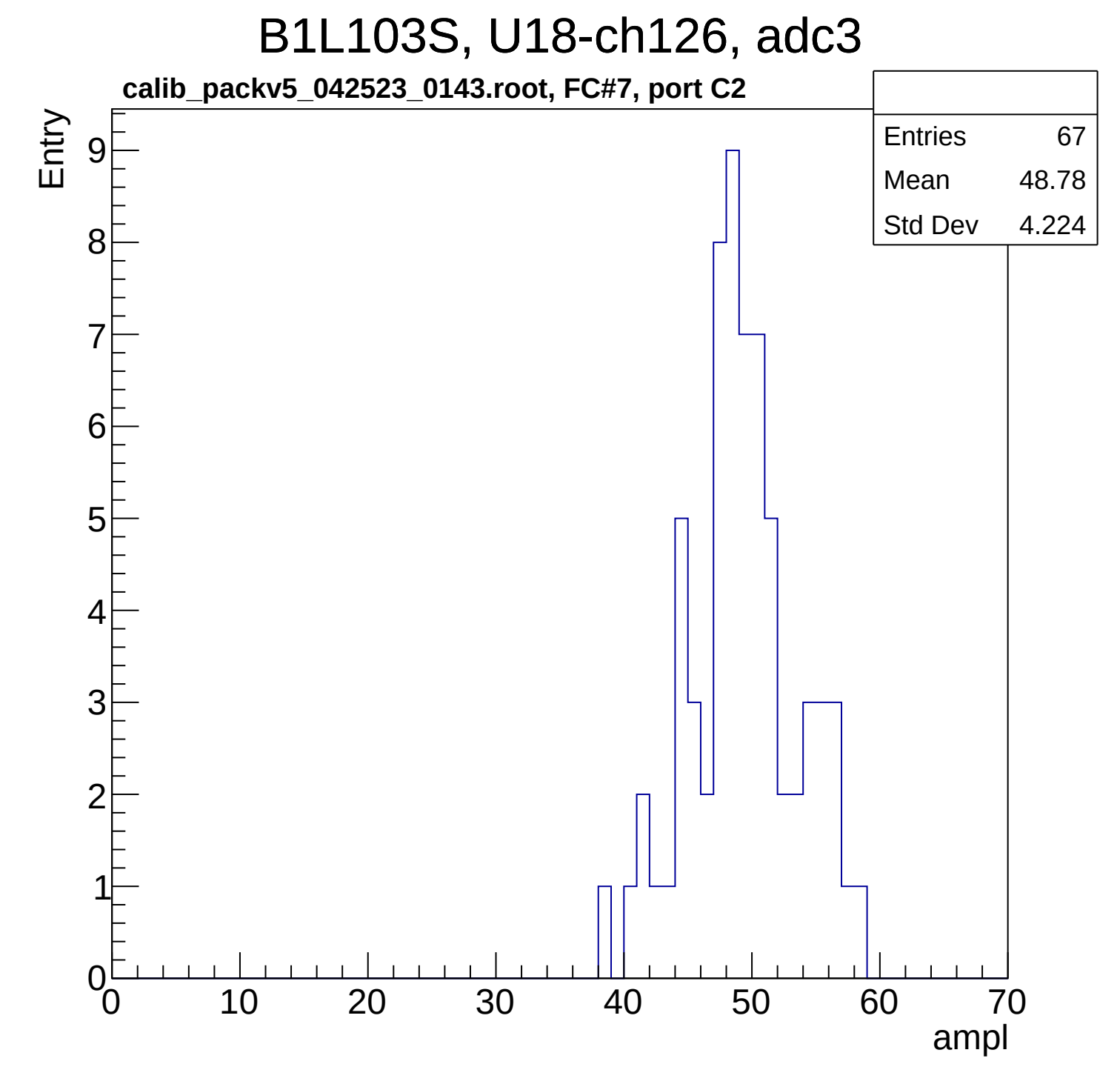
40
50
60
70


B1L103S, U18-ch126, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 43.31
Std Dev 3.729
Gaus mean : 43.8015
Gaus Width: 3.9408
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch126, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 48.78
Std Dev 4.224
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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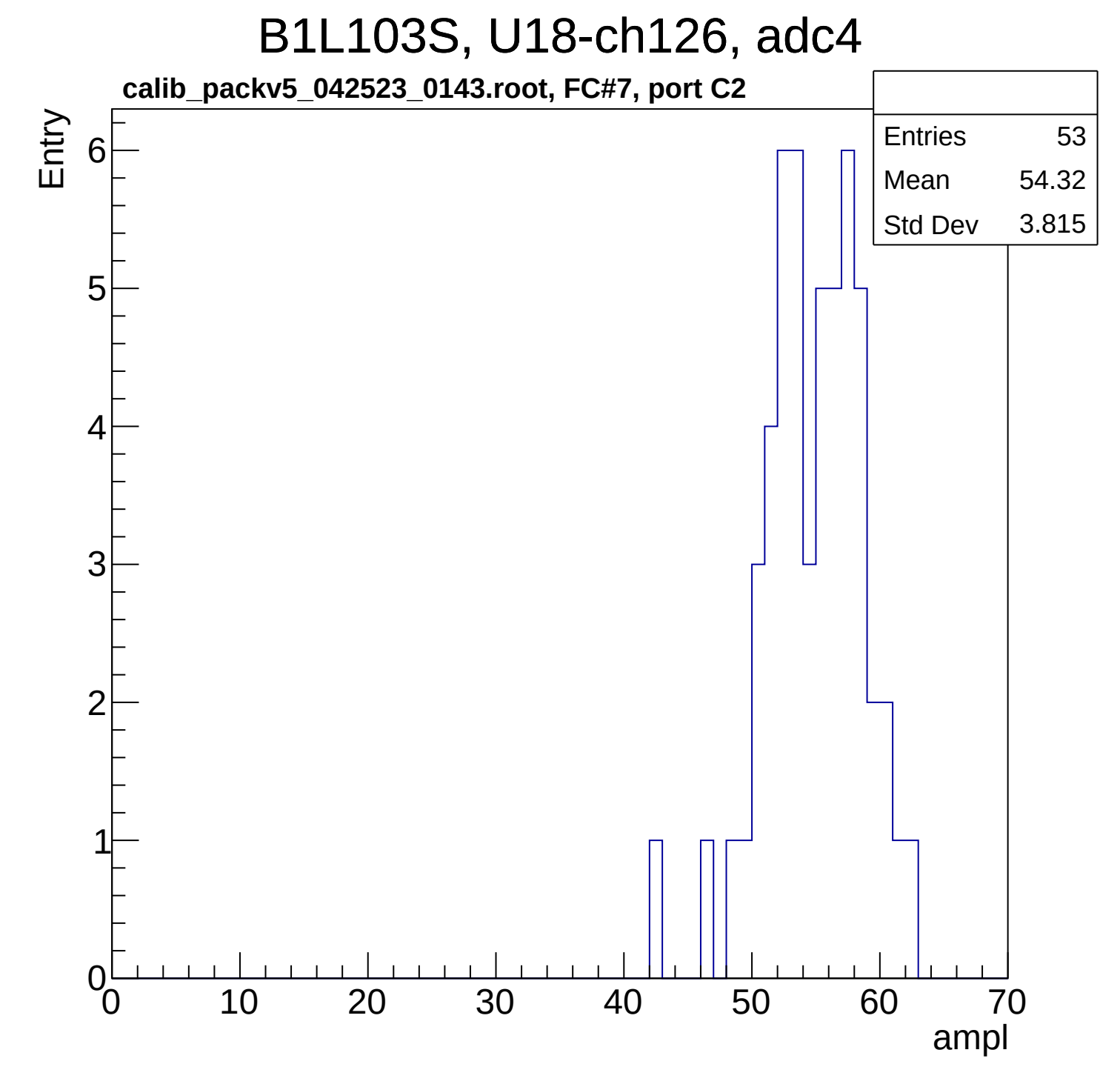
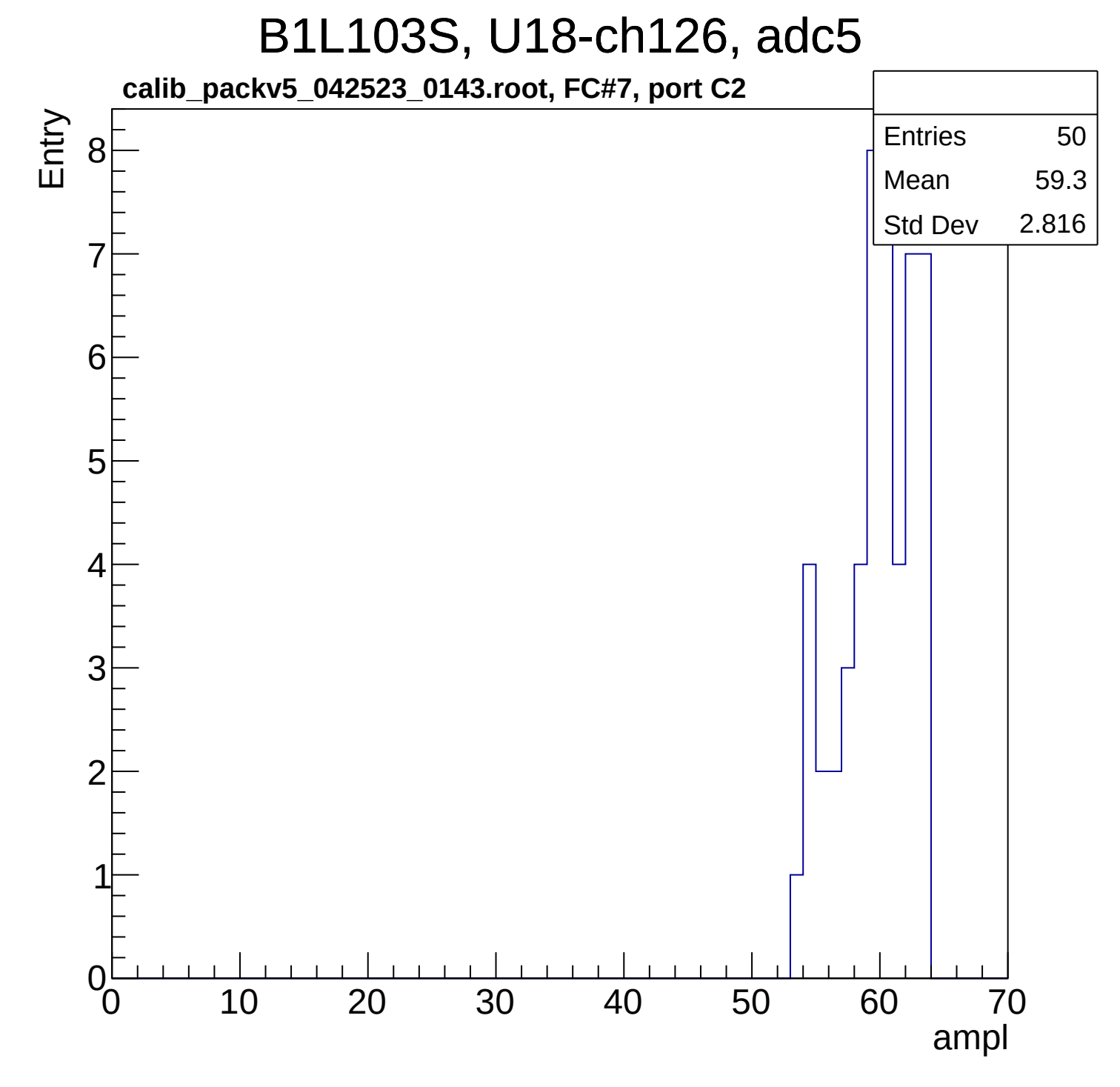

B1L103S, U18-ch126, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 54.32
Std Dev 3.815
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U18-ch126, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 50
Mean 59.3
Std Dev 2.816
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
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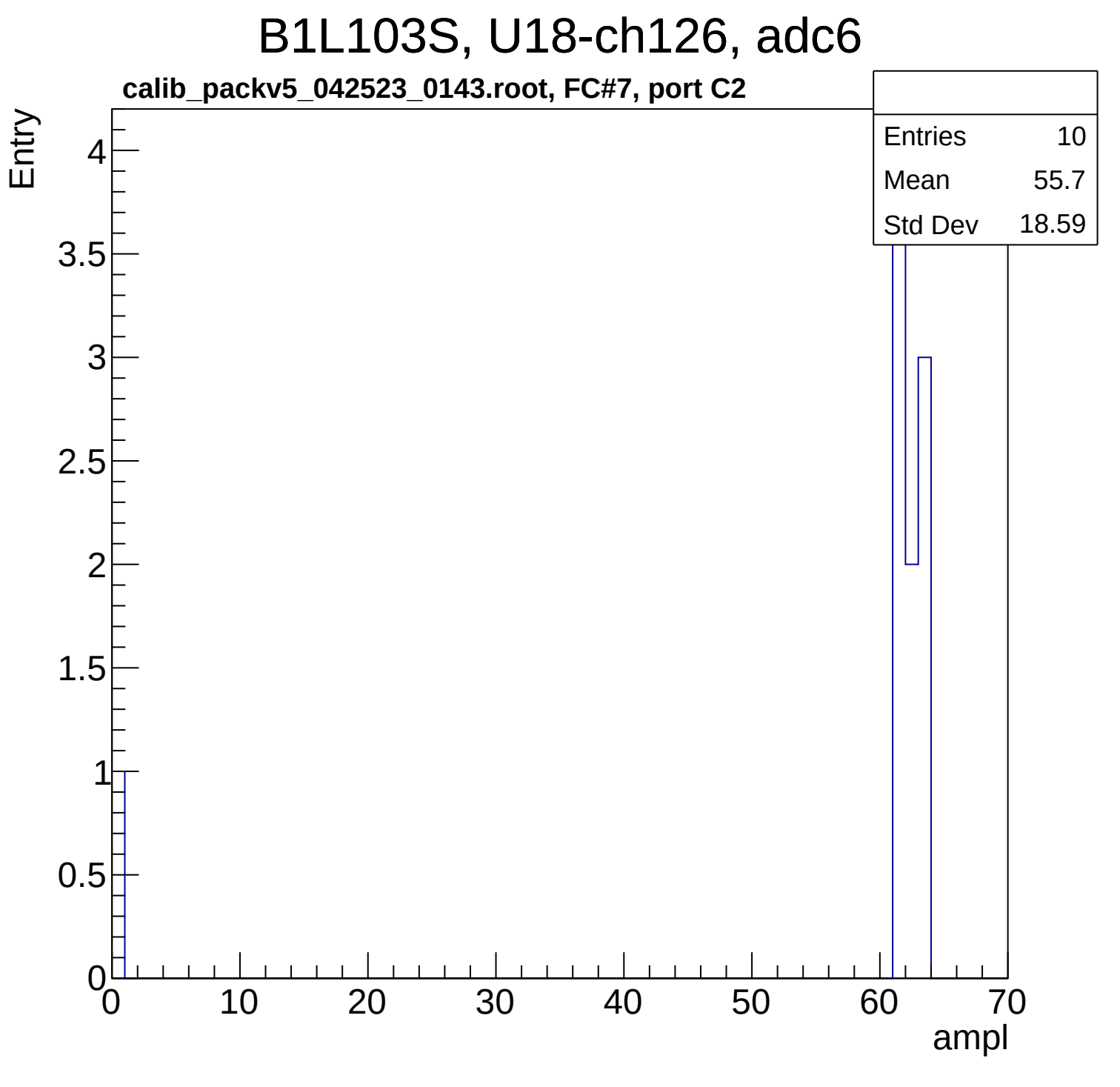
60
70


B1L103S, U18-ch126, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 10
Mean 55.7
Std Dev 18.59
Entry
ampl
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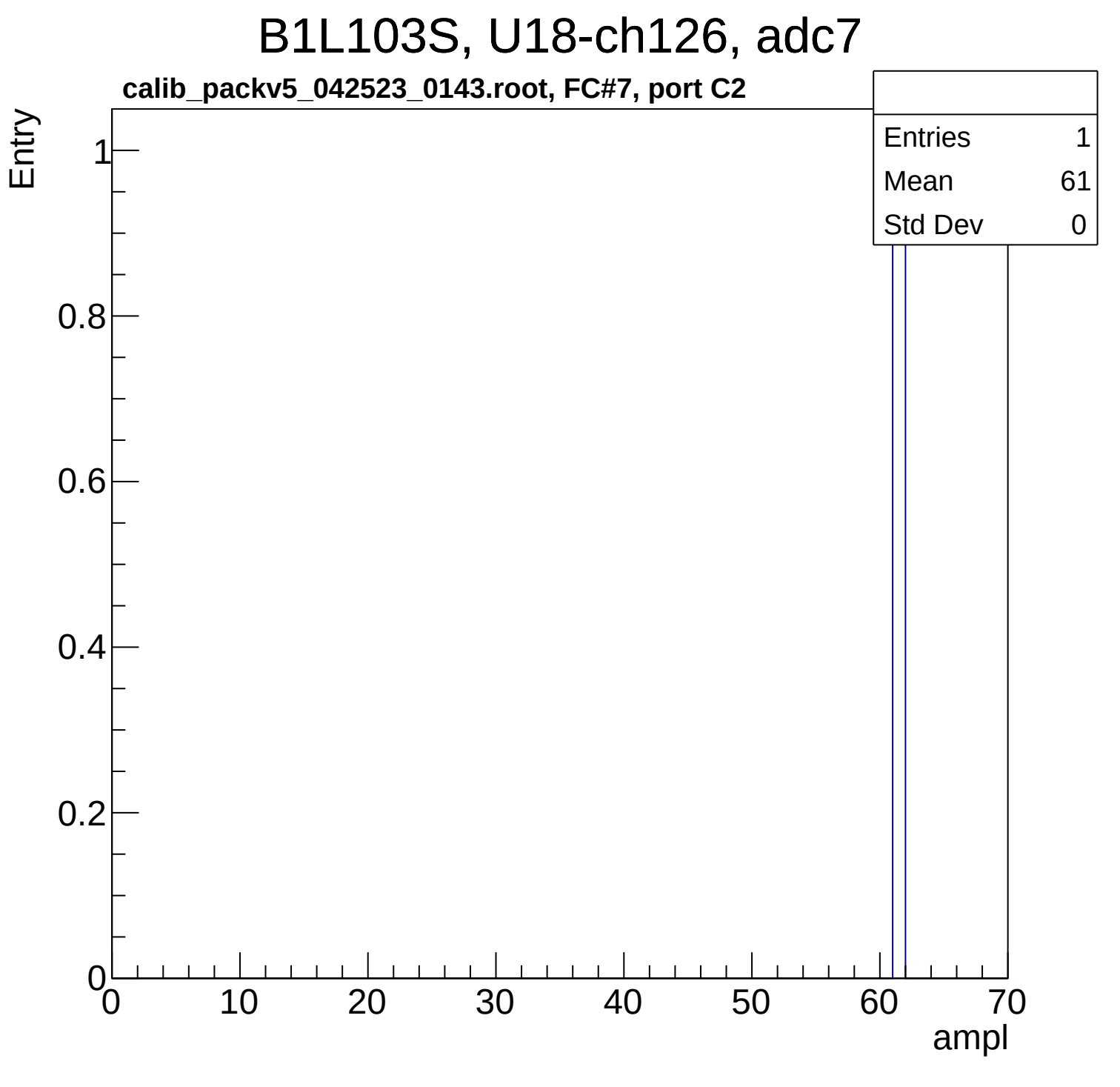
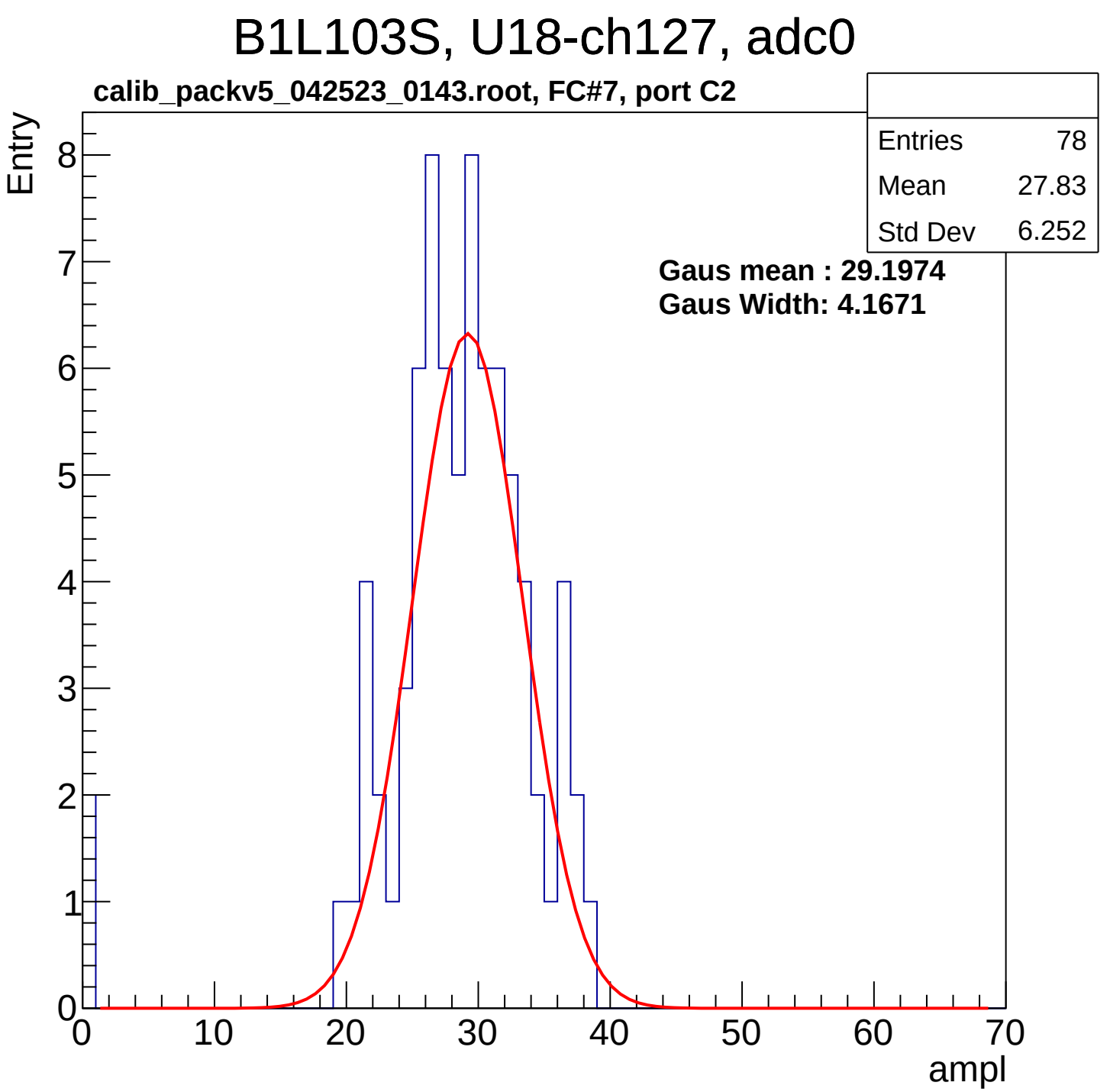
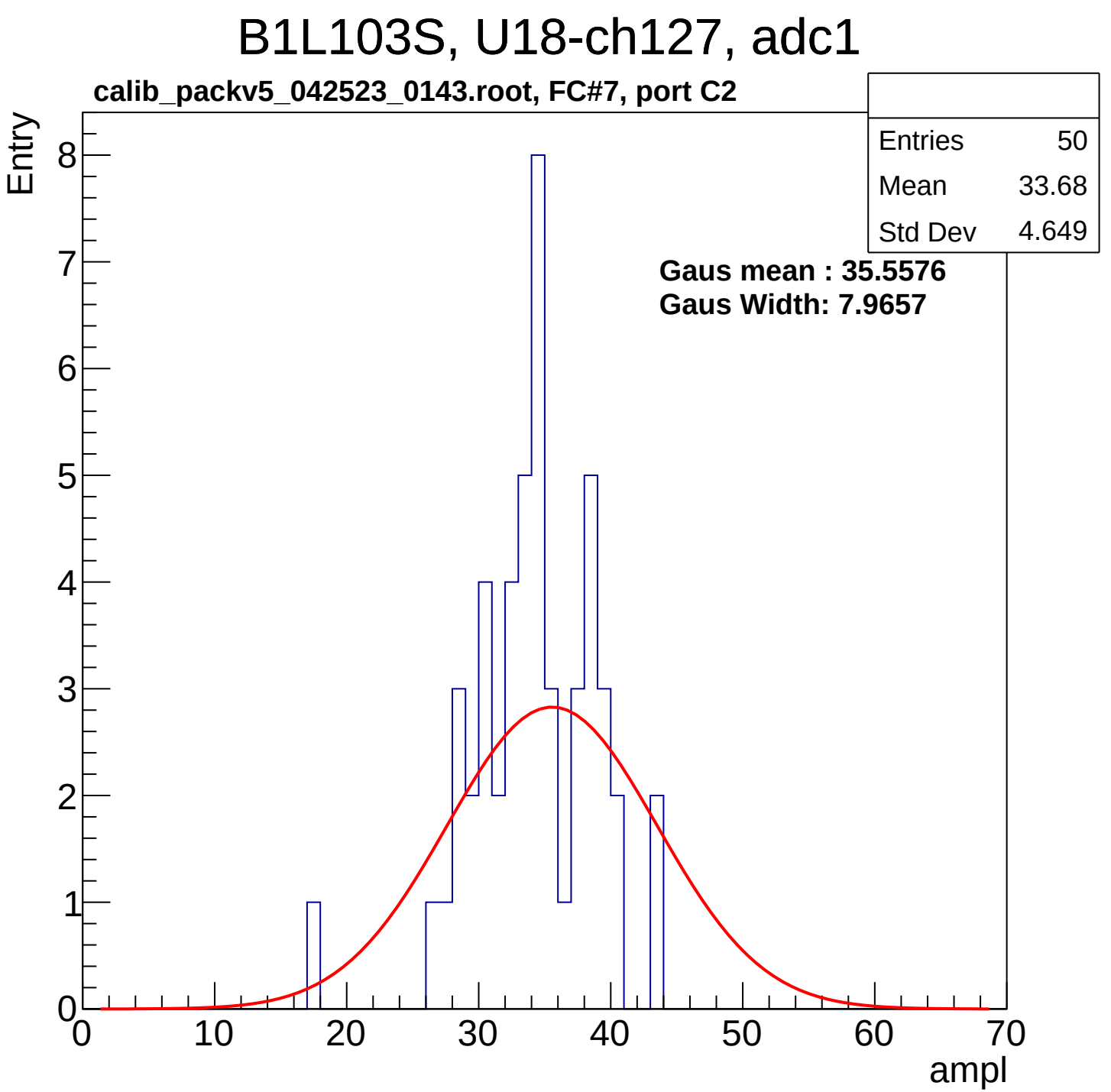
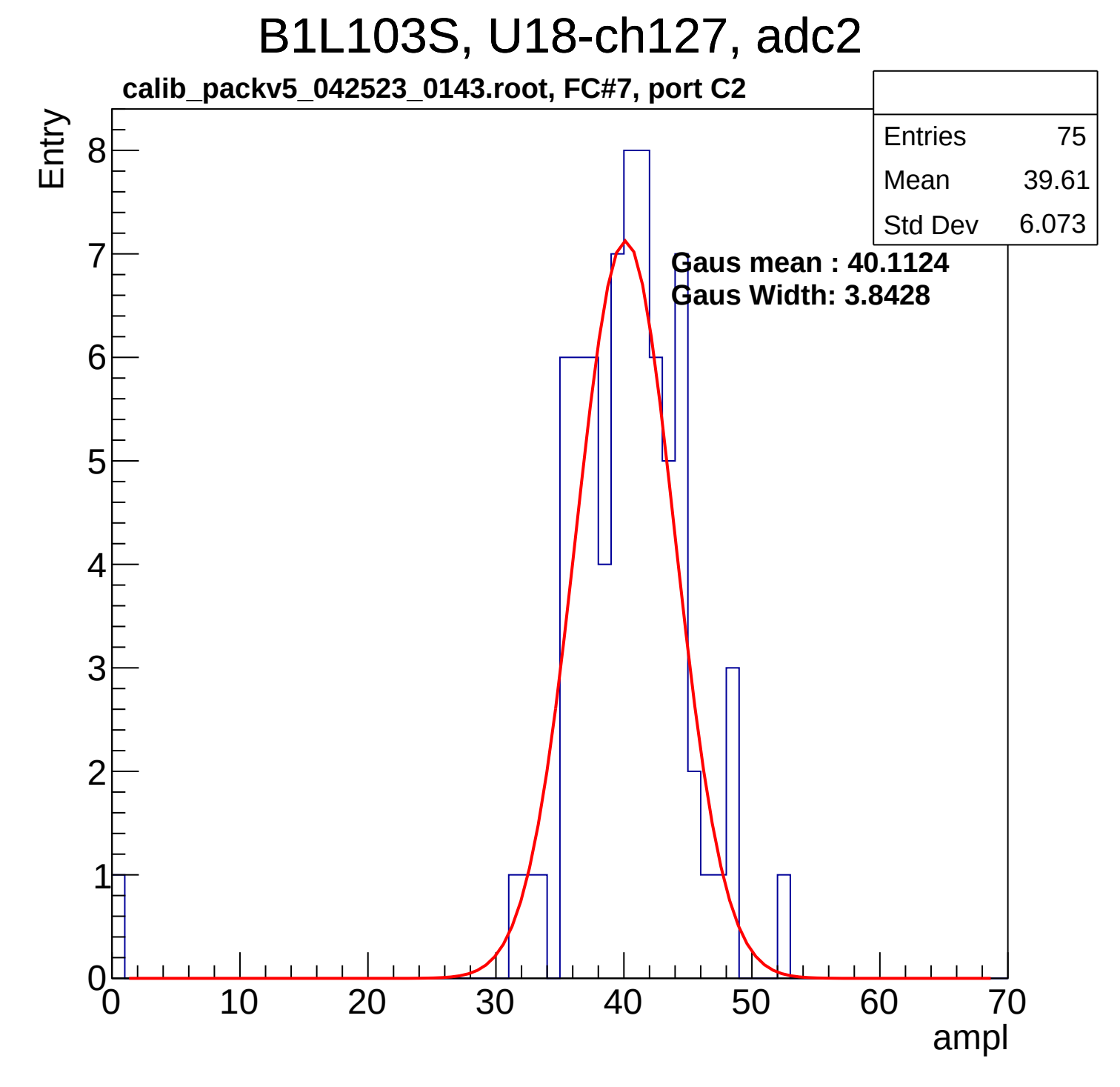
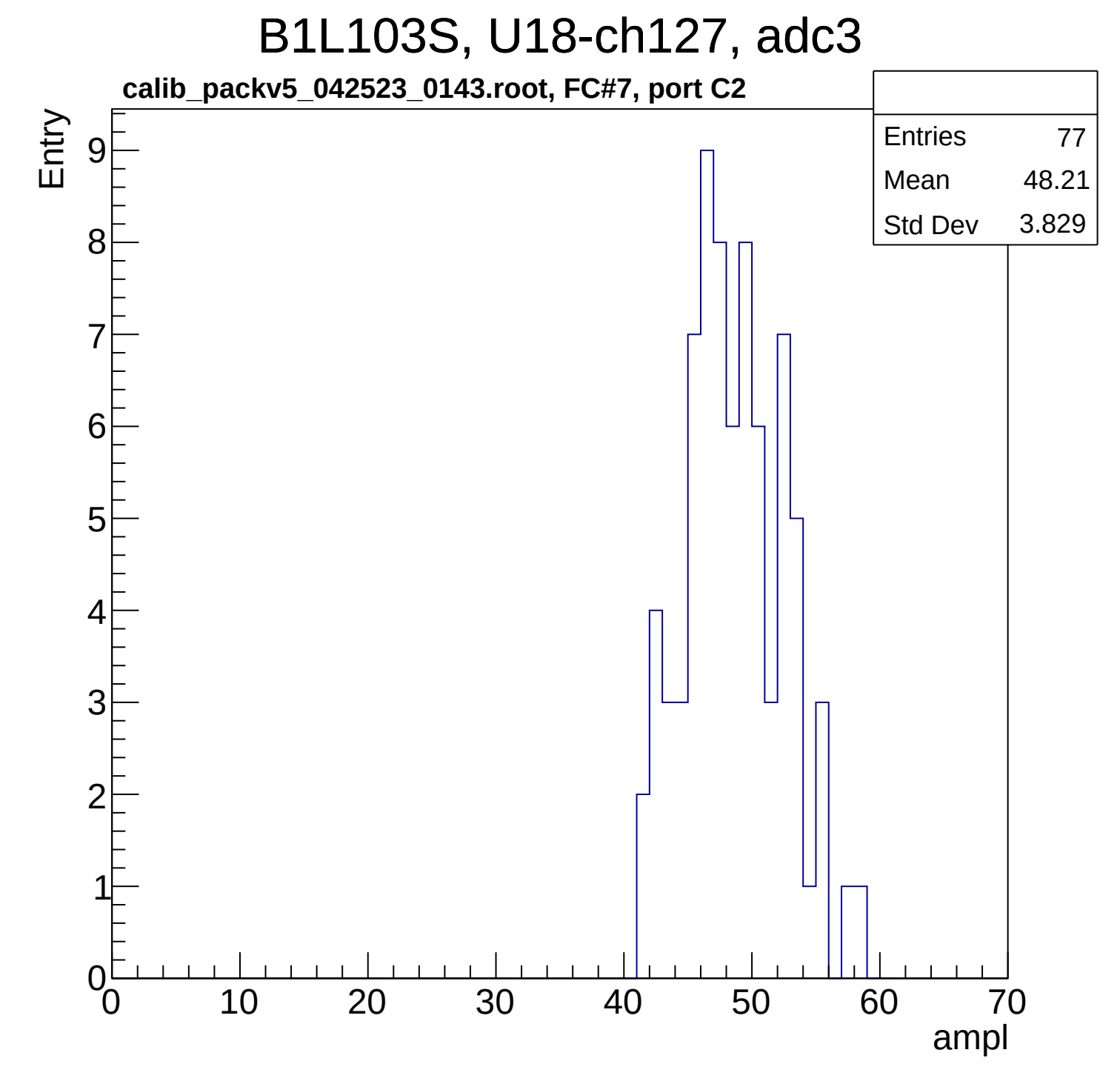
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

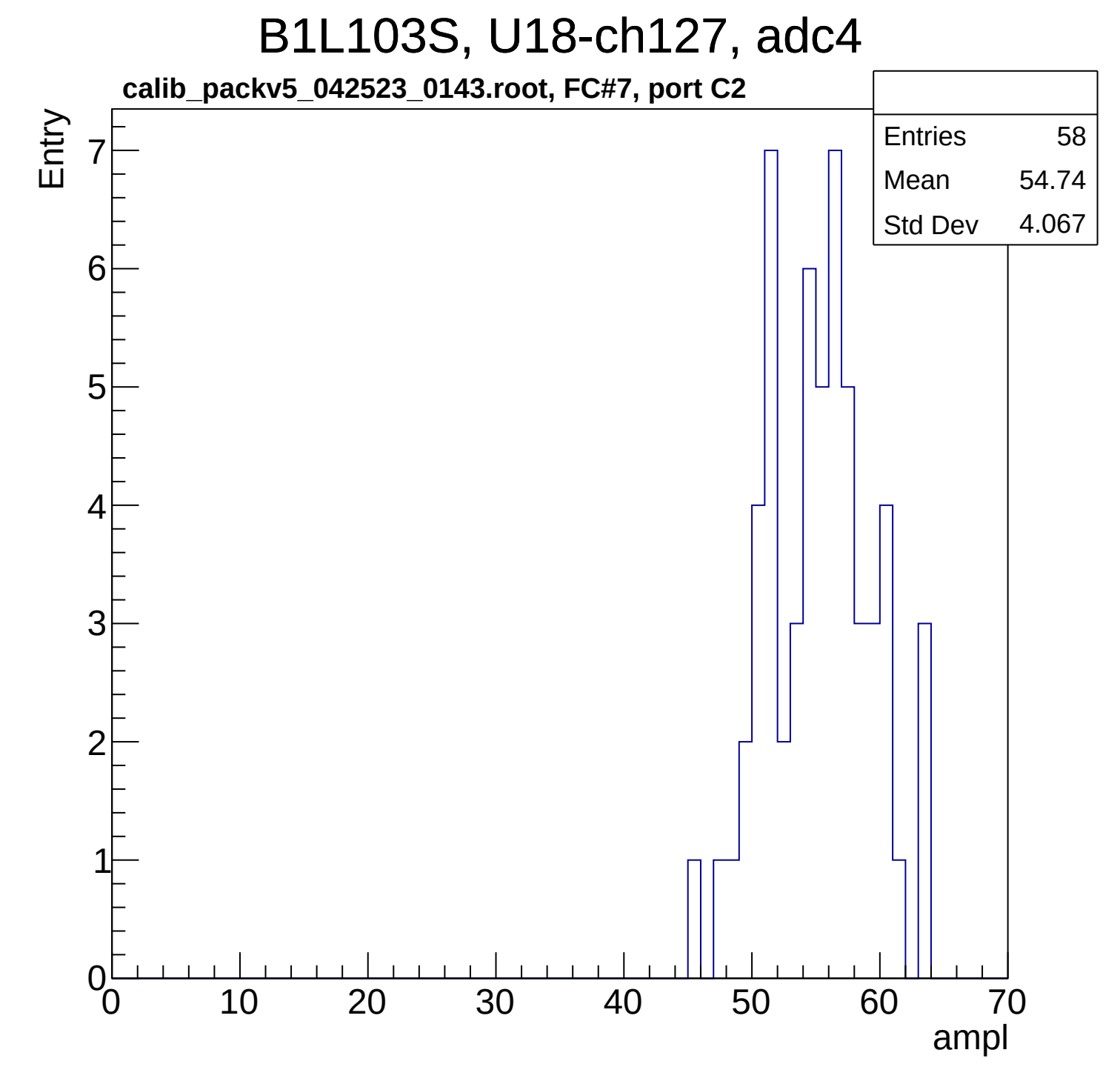

B1L103S, U18-ch126, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 61
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

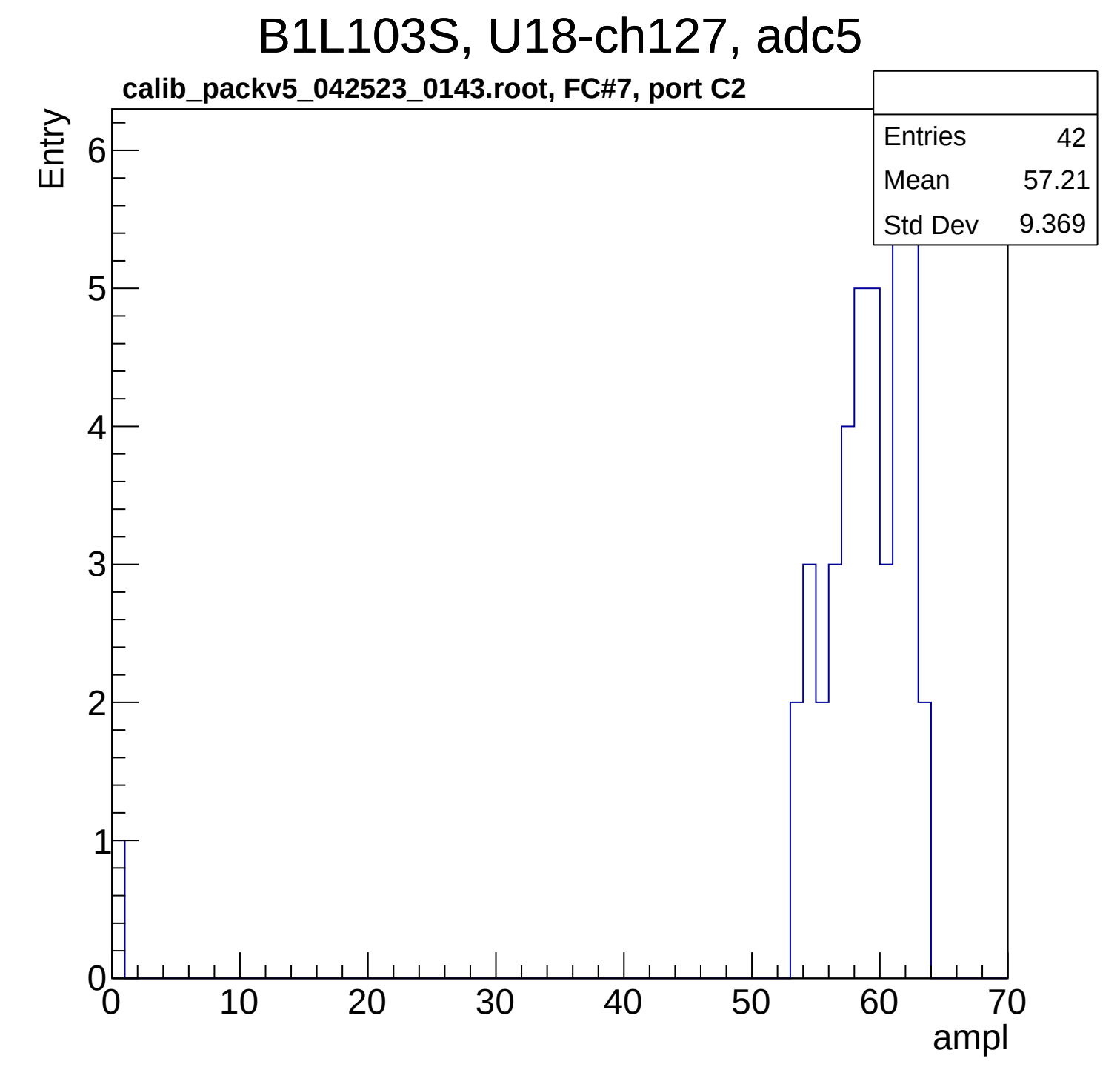

B1L103S, U18-ch127, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 78
Mean 27.83
Std Dev 6.252
Gaus mean : 29.1974
Gaus Width: 4.1671
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

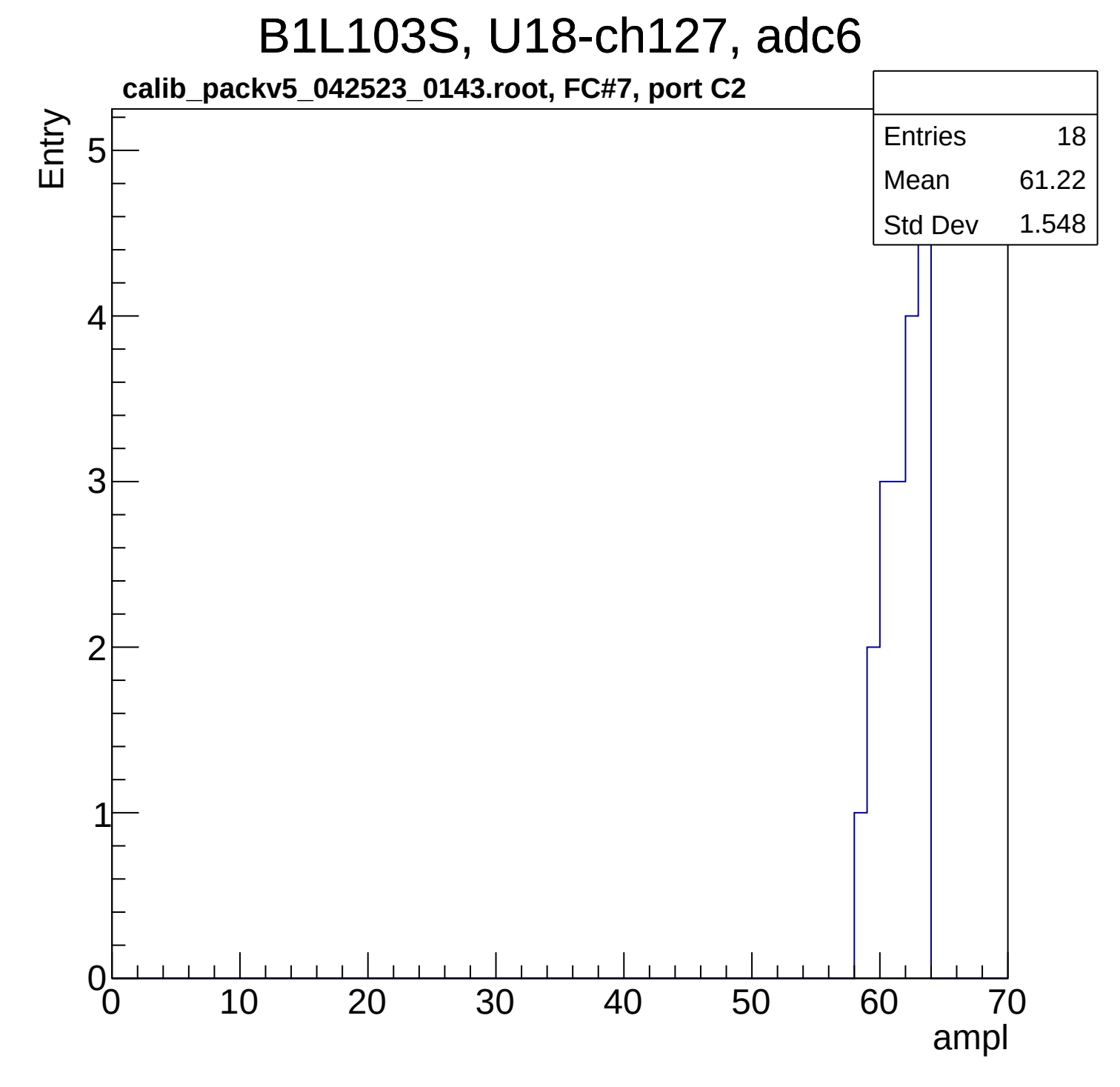

B1L103S, U18-ch127, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 50
Mean 33.68
Std Dev 4.649
Gaus mean : 35.5576
Gaus Width: 7.9657
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

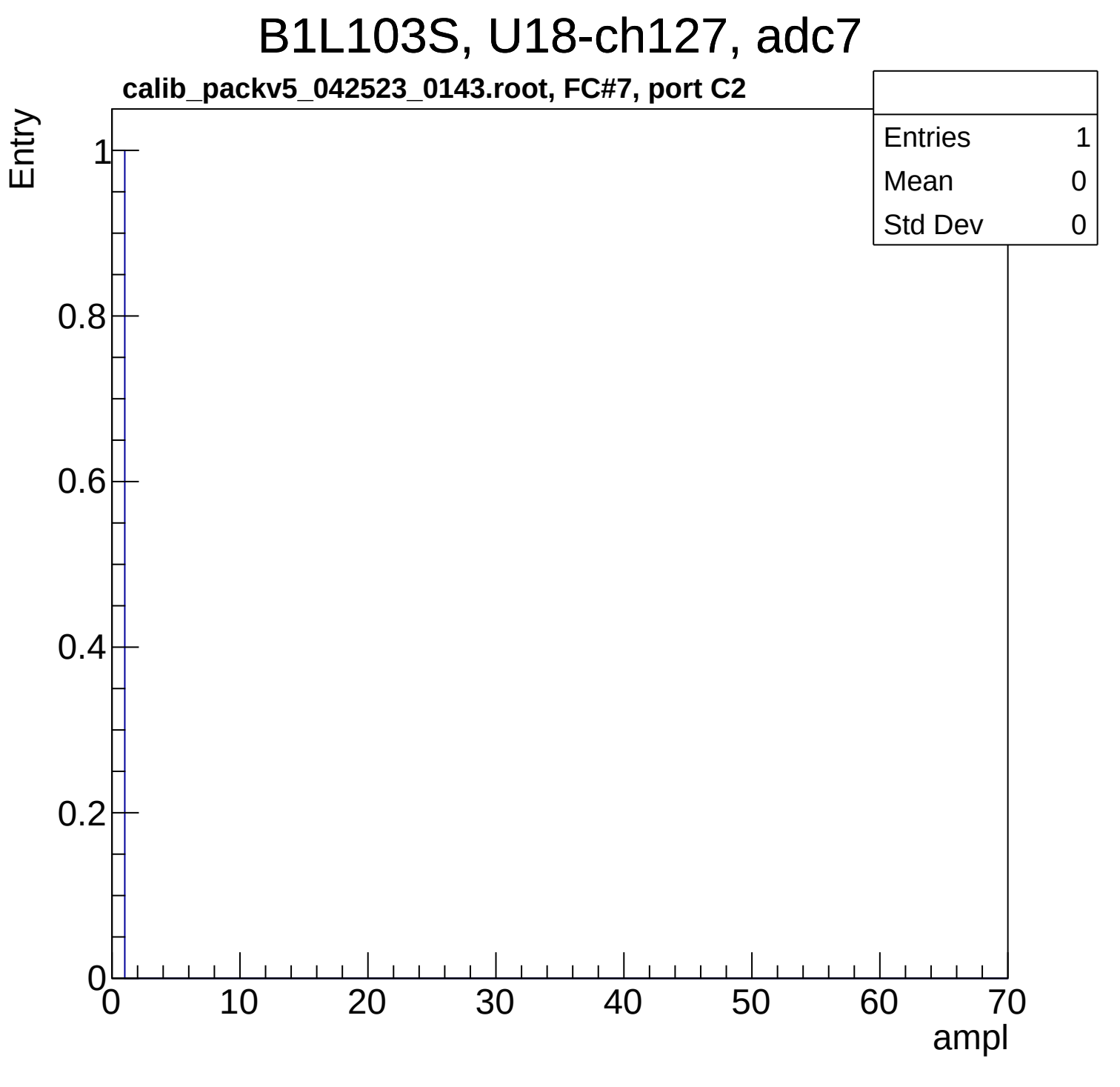

B1L103S, U18-ch127, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 75
Mean 39.61
Std Dev 6.073
Gaus mean : 40.1124
Gaus Width: 3.8428
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

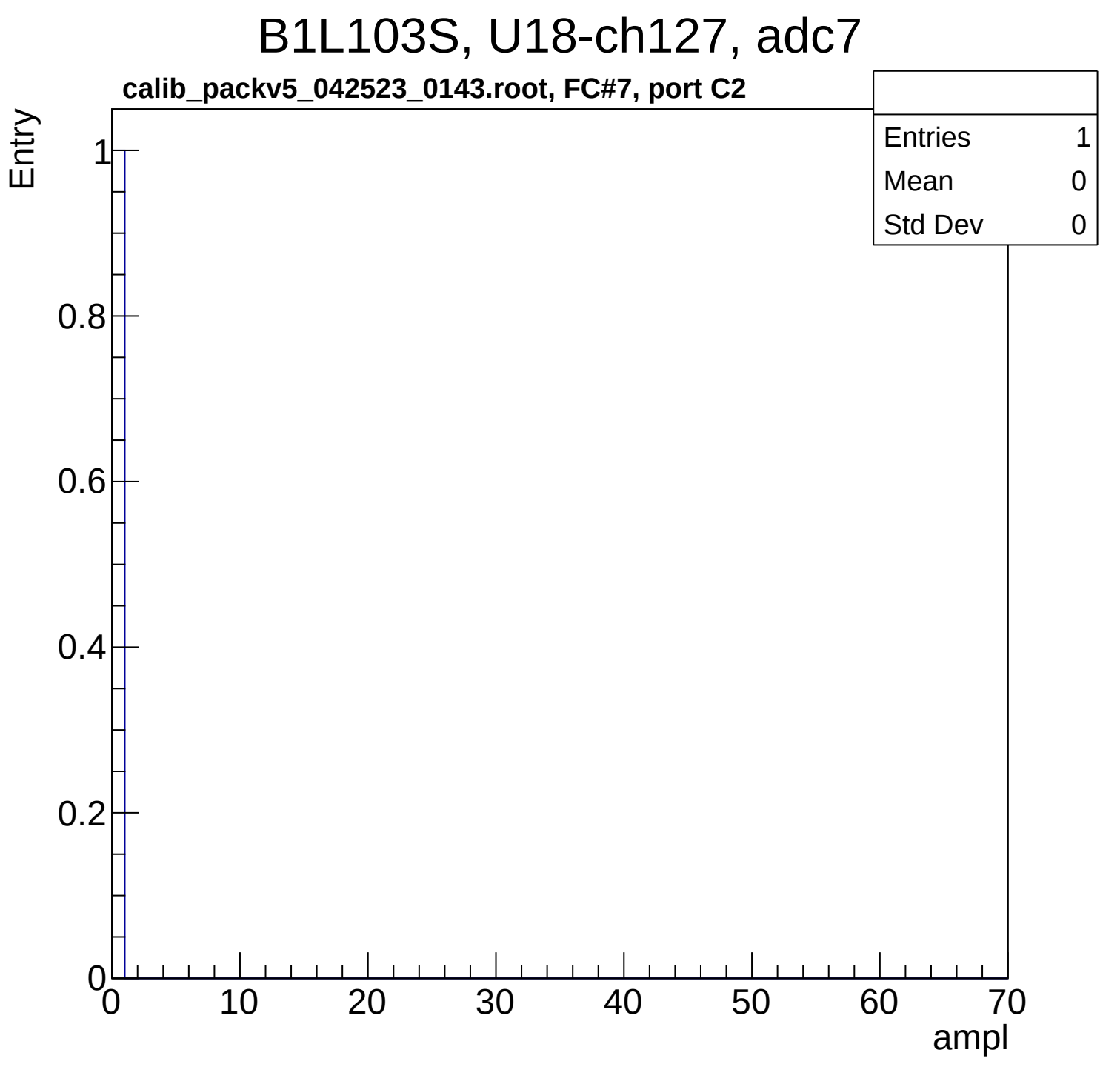

B1L103S, U18-ch127, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 77
Mean 48.21
Std Dev 3.829
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch127, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 58
Mean 54.74
Std Dev 4.067
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch127, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 42
Mean 57.21
Std Dev 9.369
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U18-ch127, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 18
Mean 61.22
Std Dev 1.548
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U18-ch127, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch127, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl