

B1L101S, U8-ch0

calib_packv5_042523_0143.root, FC#0, port D2

Entries	400
Mean	43.12
Std Dev	12.4

Turn on : 24.5136

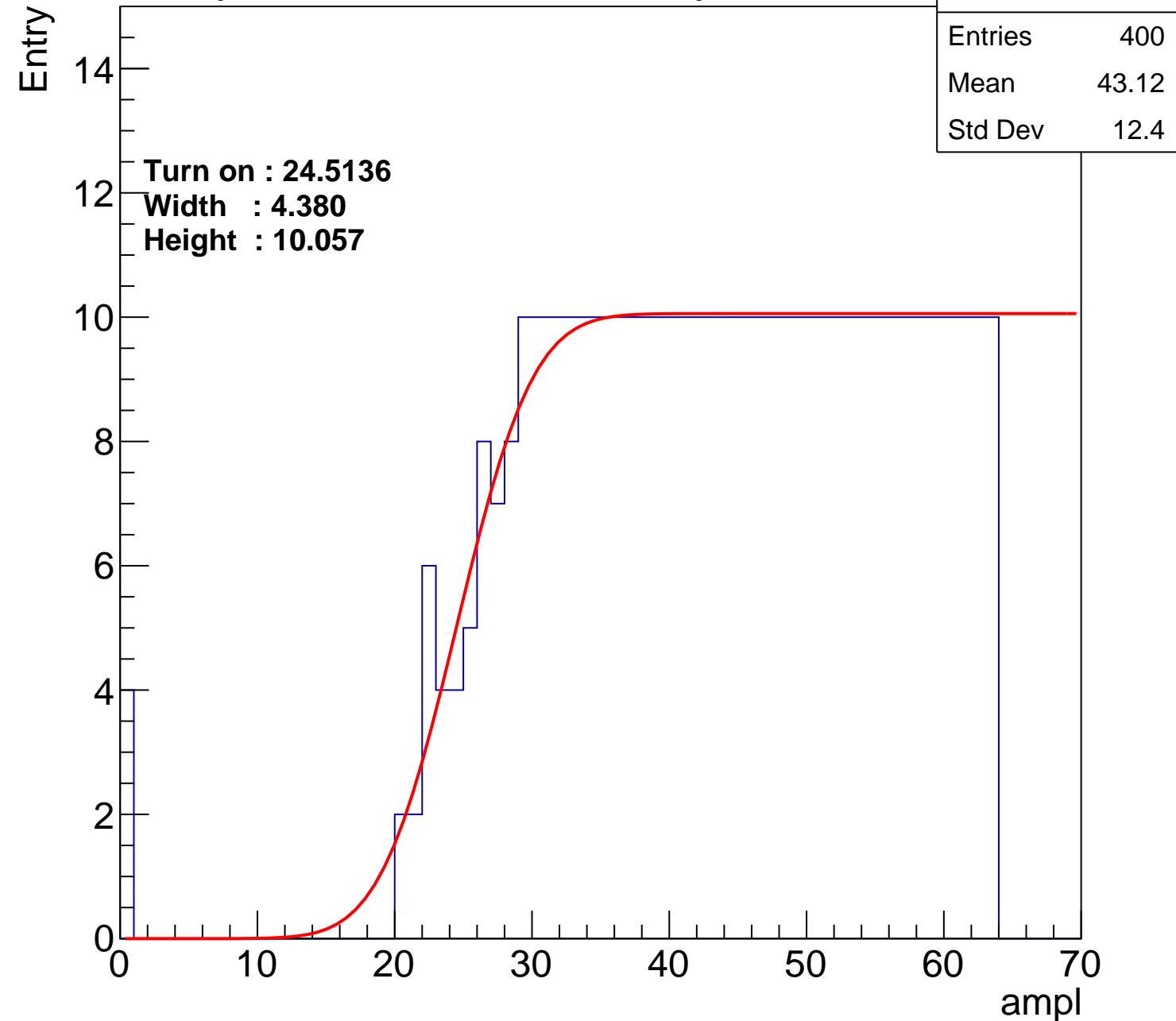
Width : 4.380

Height : 10.057

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch1

calib_packv5_042523_0143.root, FC#0, port D2

Entries	378
Mean	44.33
Std Dev	11.52

Turn on : 26.4120

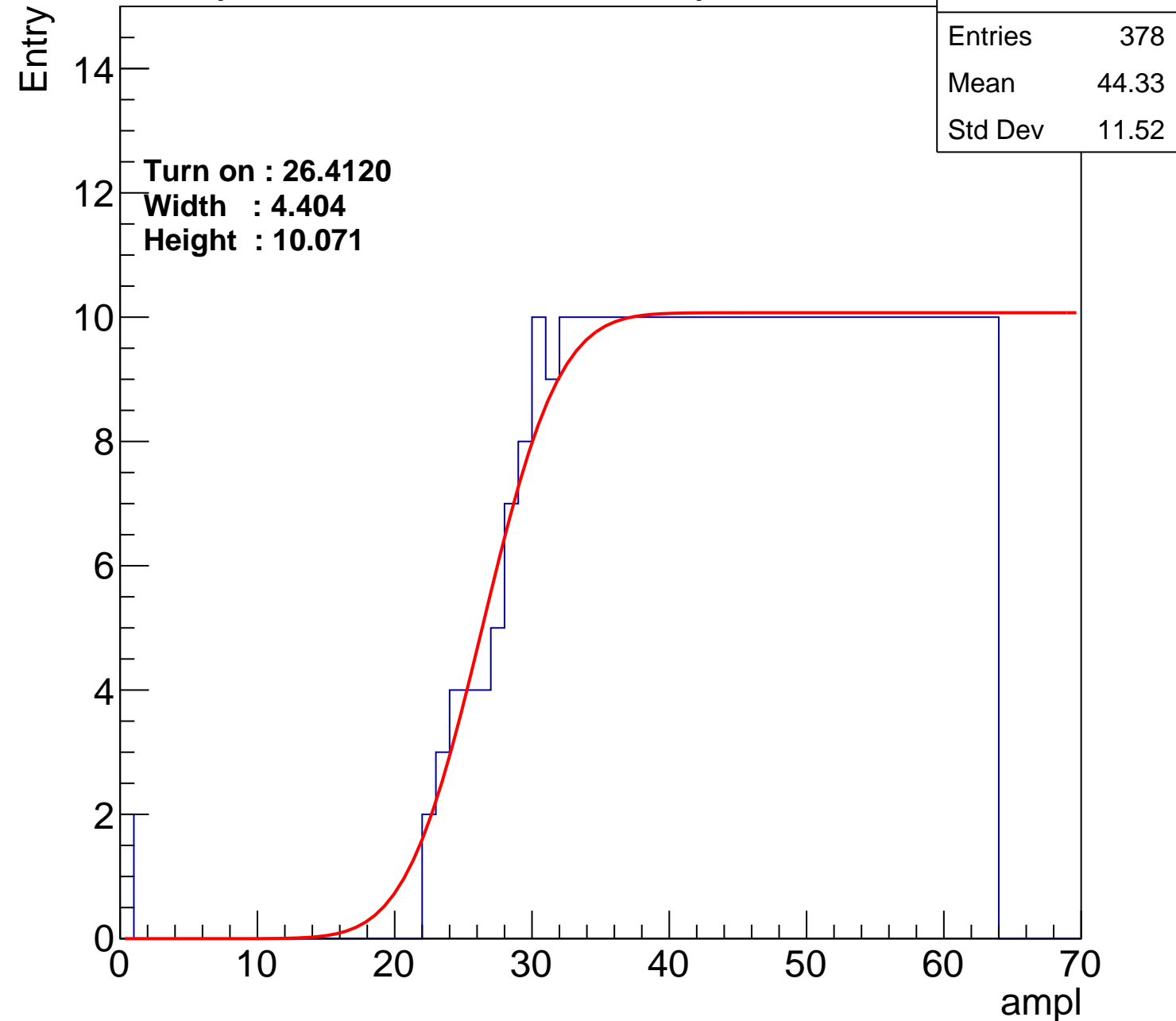
Width : 4.404

Height : 10.071

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch2

calib_packv5_042523_0143.root, FC#0, port D2

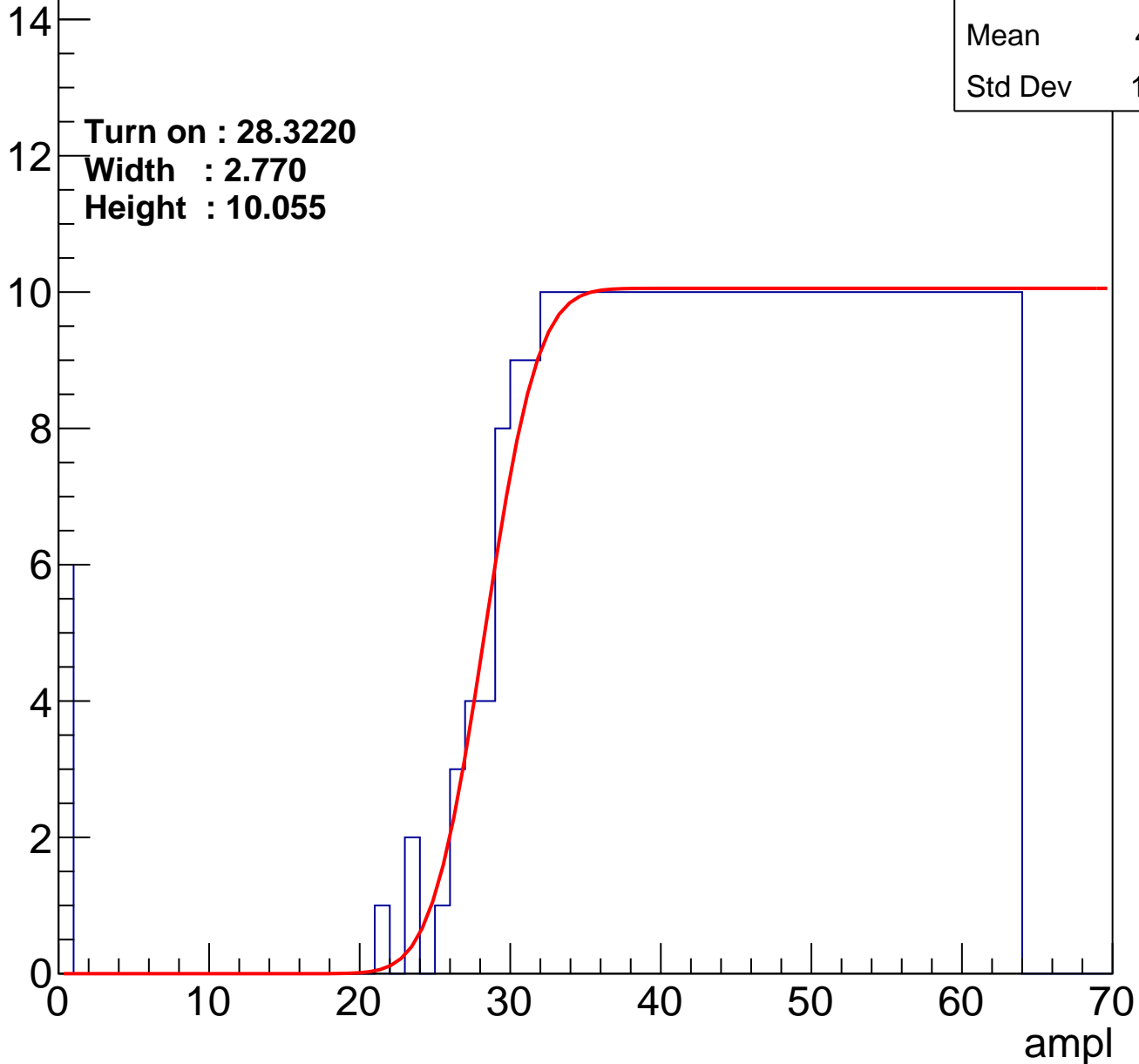
Entries	367
Mean	44.61
Std Dev	11.98

Turn on : 28.3220

Width : 2.770

Height : 10.055

Entry



B1L101S, U8-ch3

calib_packv5_042523_0143.root, FC#0, port D2

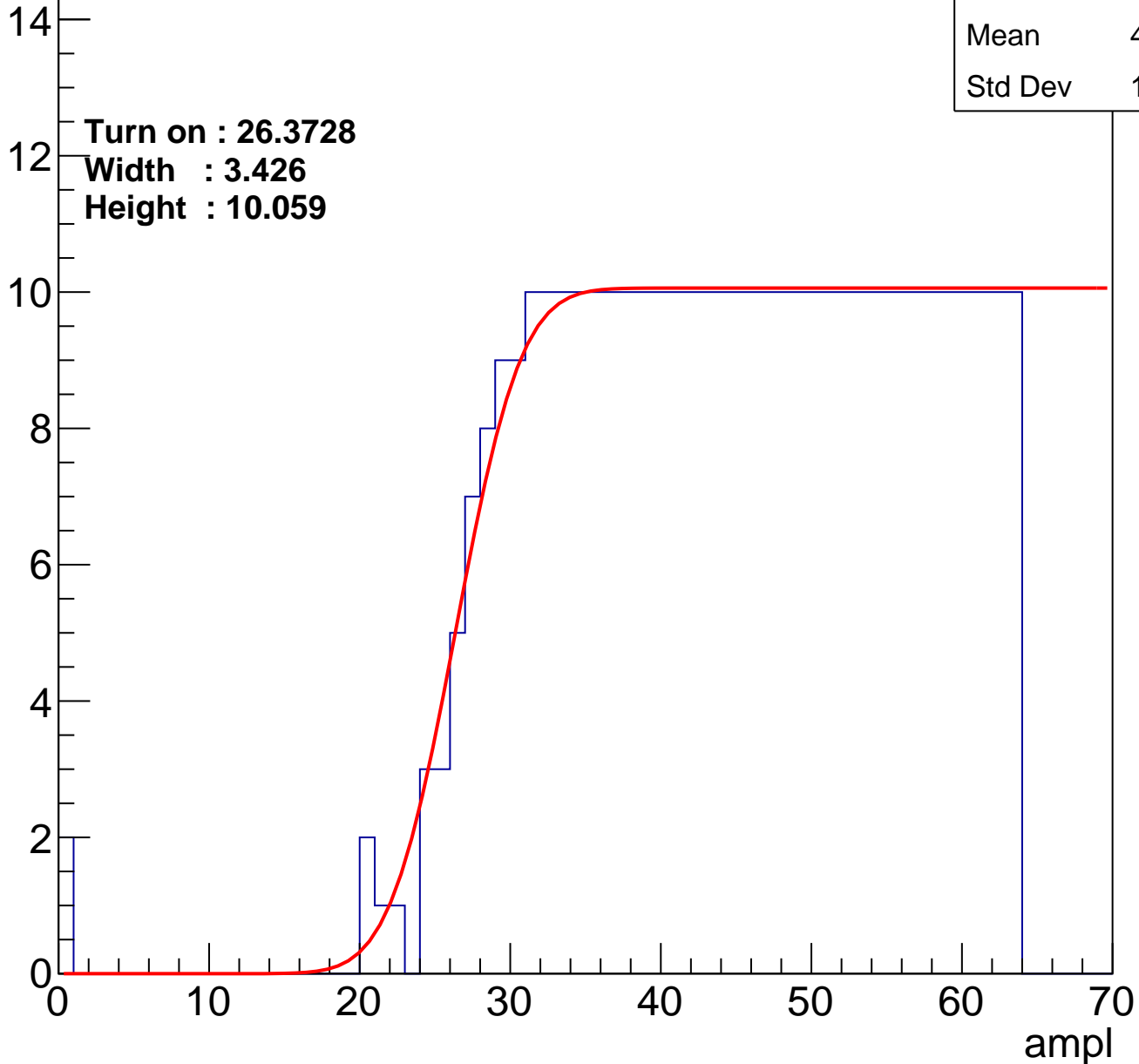
Entries	380
Mean	44.25
Std Dev	11.55

Turn on : 26.3728

Width : 3.426

Height : 10.059

Entry



B1L101S, U8-ch4

calib_packv5_042523_0143.root, FC#0, port D2

Entries	369
Mean	44.66
Std Dev	11.63

Turn on : 27.4338

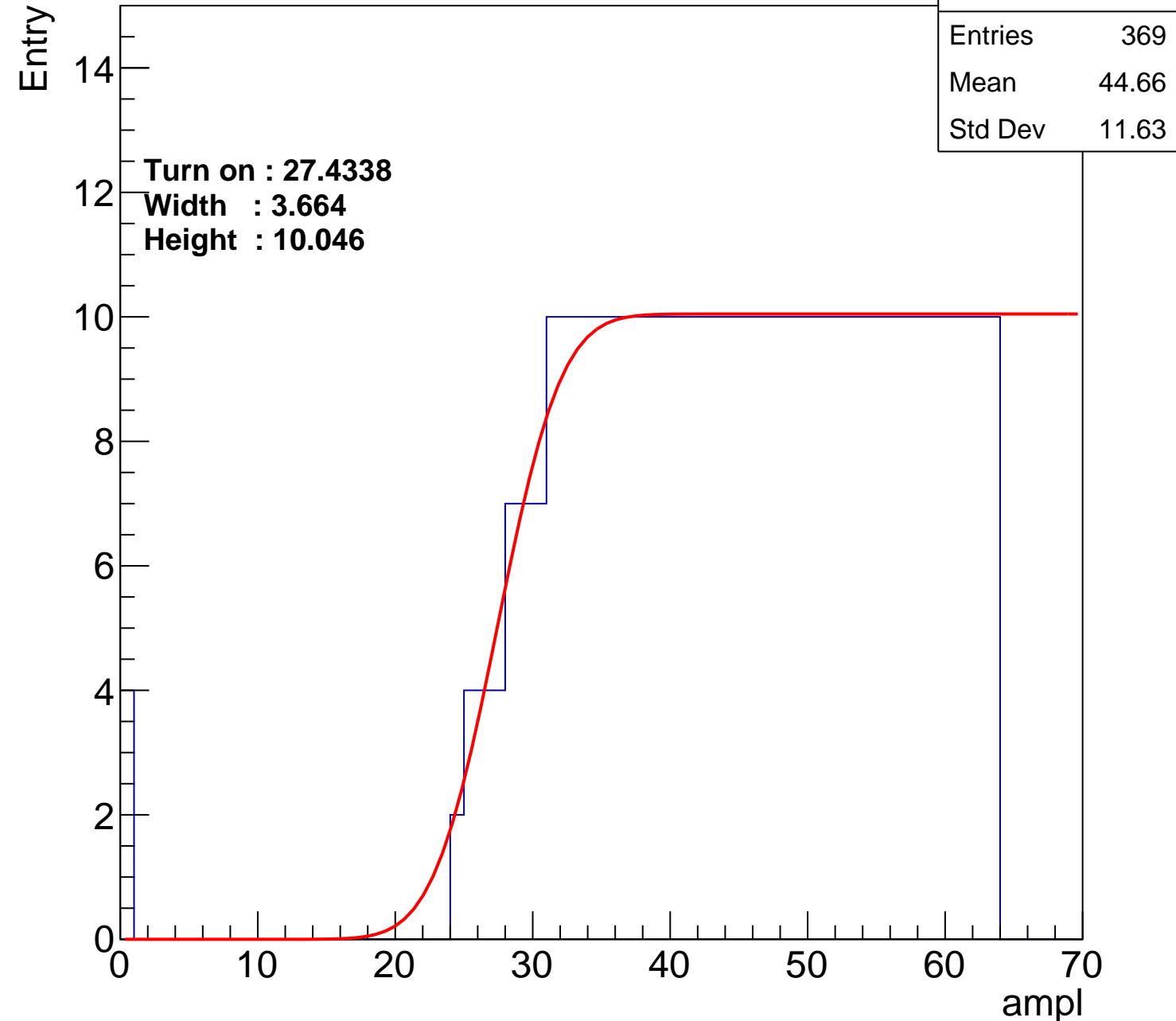
Width : 3.664

Height : 10.046

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch5

calib_packv5_042523_0143.root, FC#0, port D2

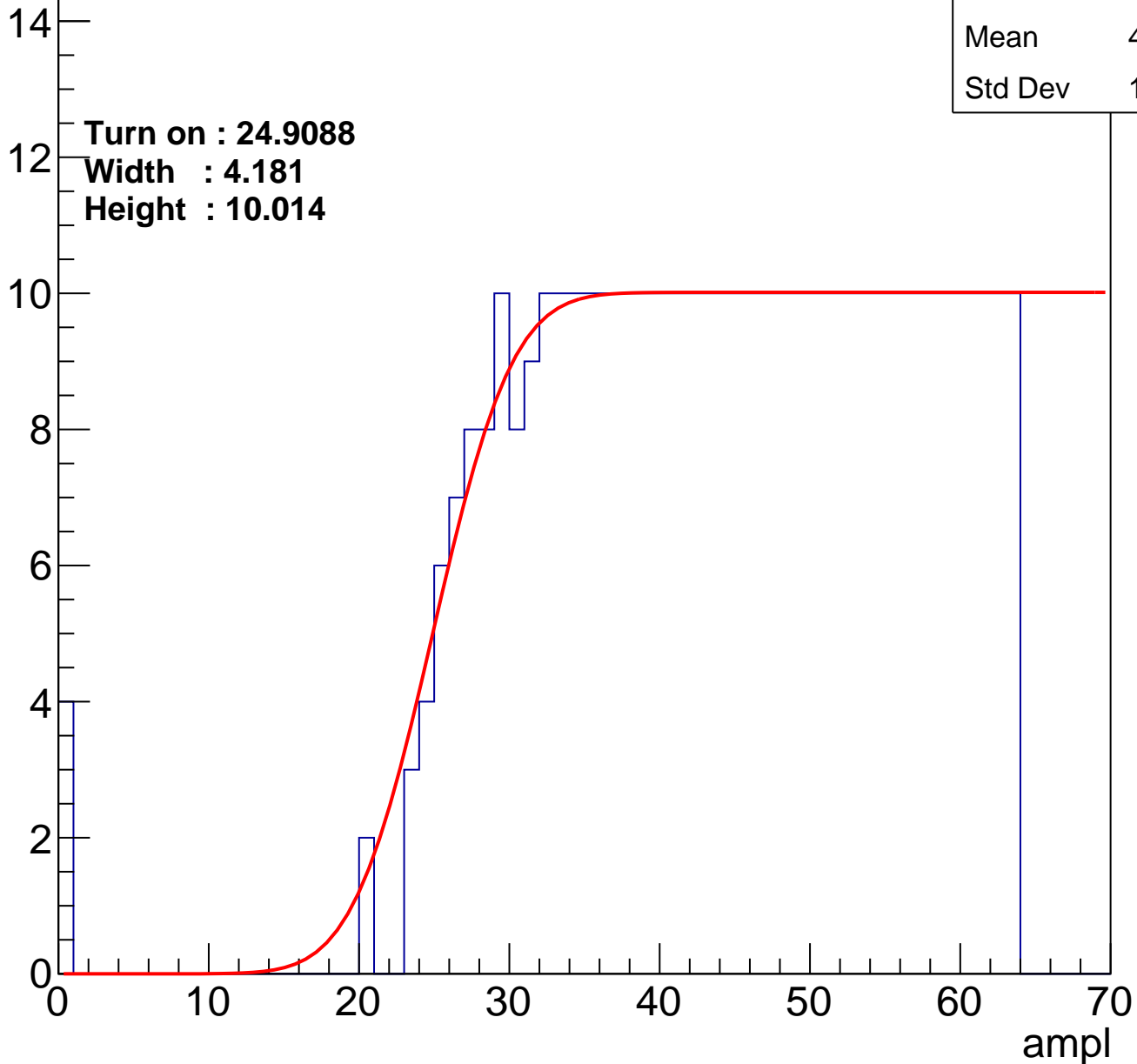
Entries	389
Mean	43.67
Std Dev	12.12

Turn on : 24.9088

Width : 4.181

Height : 10.014

Entry



B1L101S, U8-ch6

calib_packv5_042523_0143.root, FC#0, port D2

Entries	383
Mean	43.83
Std Dev	12.32

Turn on : 26.2524

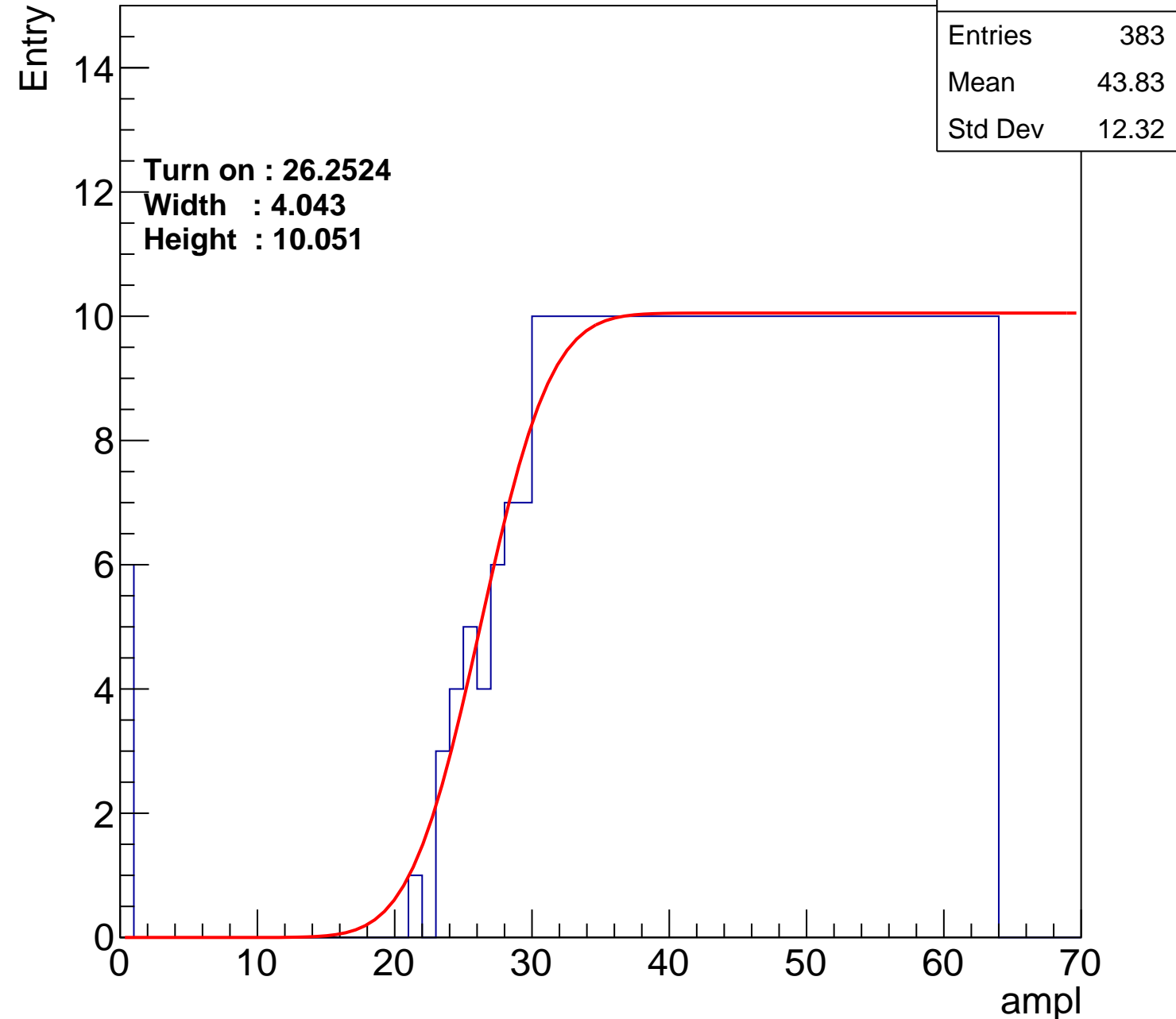
Width : 4.043

Height : 10.051

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch7

calib_packv5_042523_0143.root, FC#0, port D2

Entries	367
Mean	44.9
Std Dev	11.19

Turn on : 27.7587

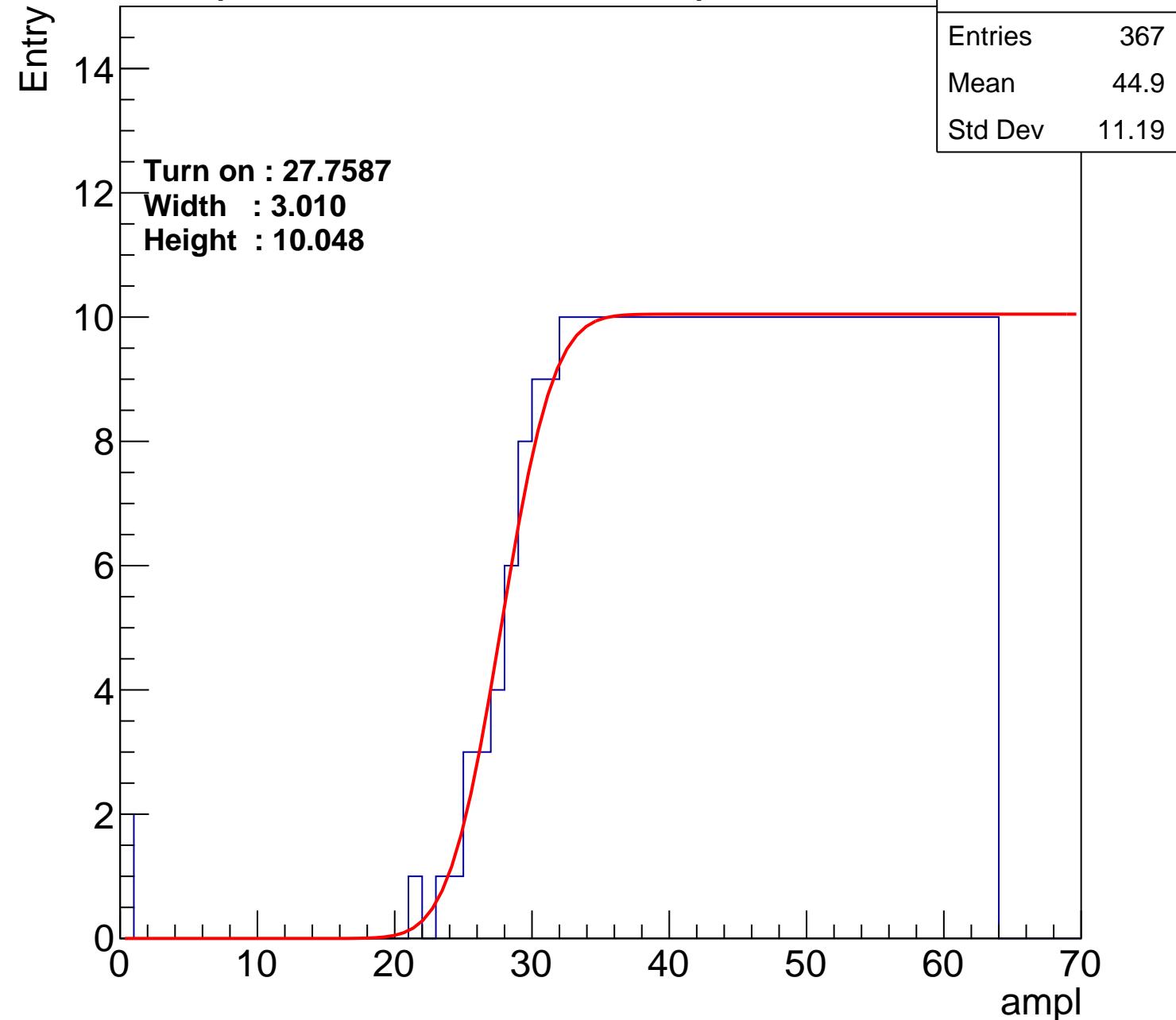
Width : 3.010

Height : 10.048

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch8

calib_packv5_042523_0143.root, FC#0, port D2

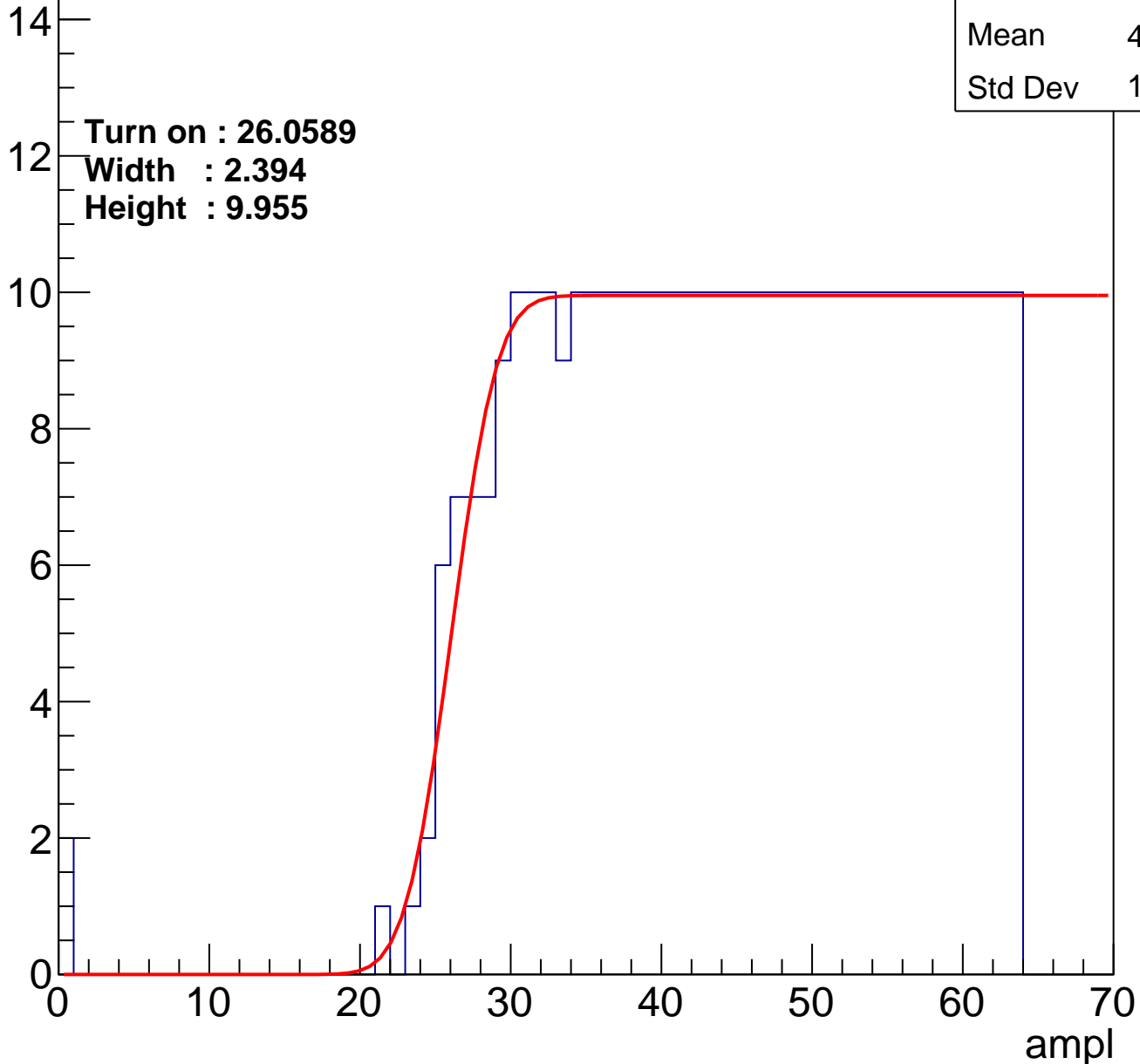
Entry

Entries	381
Mean	44.22
Std Dev	11.53

Turn on : 26.0589

Width : 2.394

Height : 9.955



B1L101S, U8-ch9

calib_packv5_042523_0143.root, FC#0, port D2

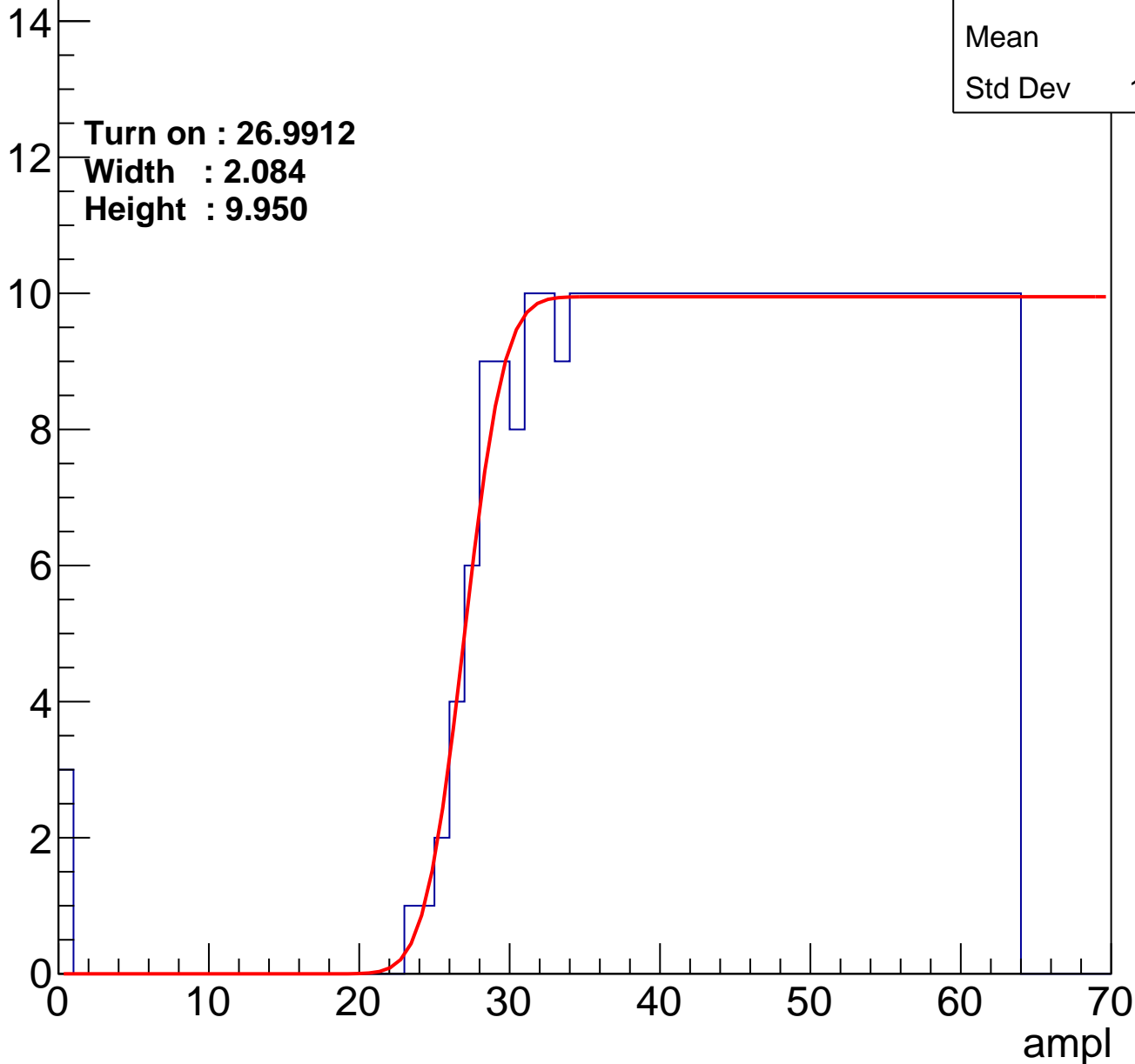
Entry

Entries	372
Mean	44.6
Std Dev	11.47

Turn on : 26.9912

Width : 2.084

Height : 9.950



B1L101S, U8-ch10

calib_packv5_042523_0143.root, FC#0, port D2

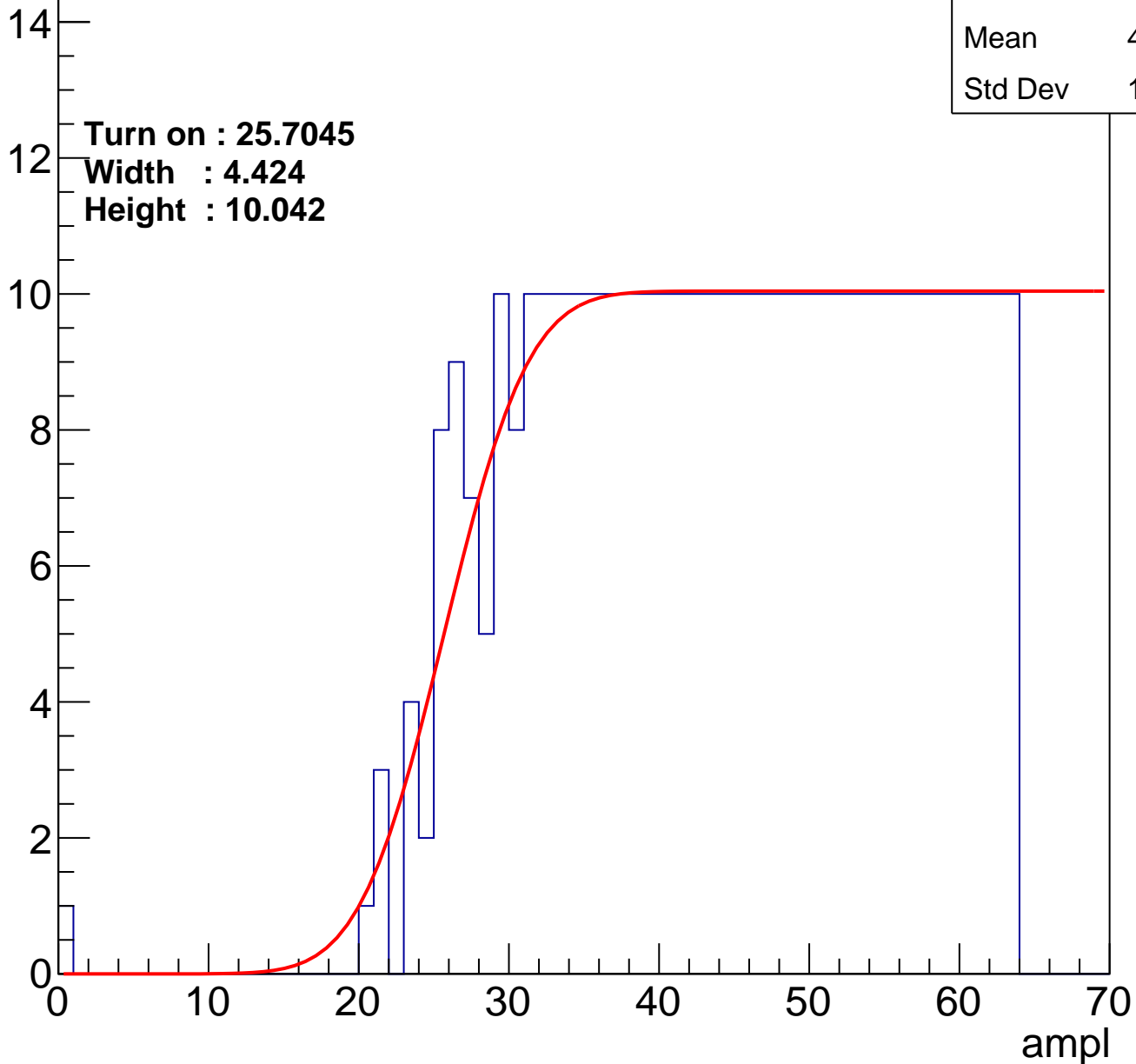
Entries	388
Mean	43.88
Std Dev	11.63

Turn on : 25.7045

Width : 4.424

Height : 10.042

Entry



B1L101S, U8-ch11

calib_packv5_042523_0143.root, FC#0, port D2

Entries	352
Mean	45.56
Std Dev	11.04

Turn on : 29.2242

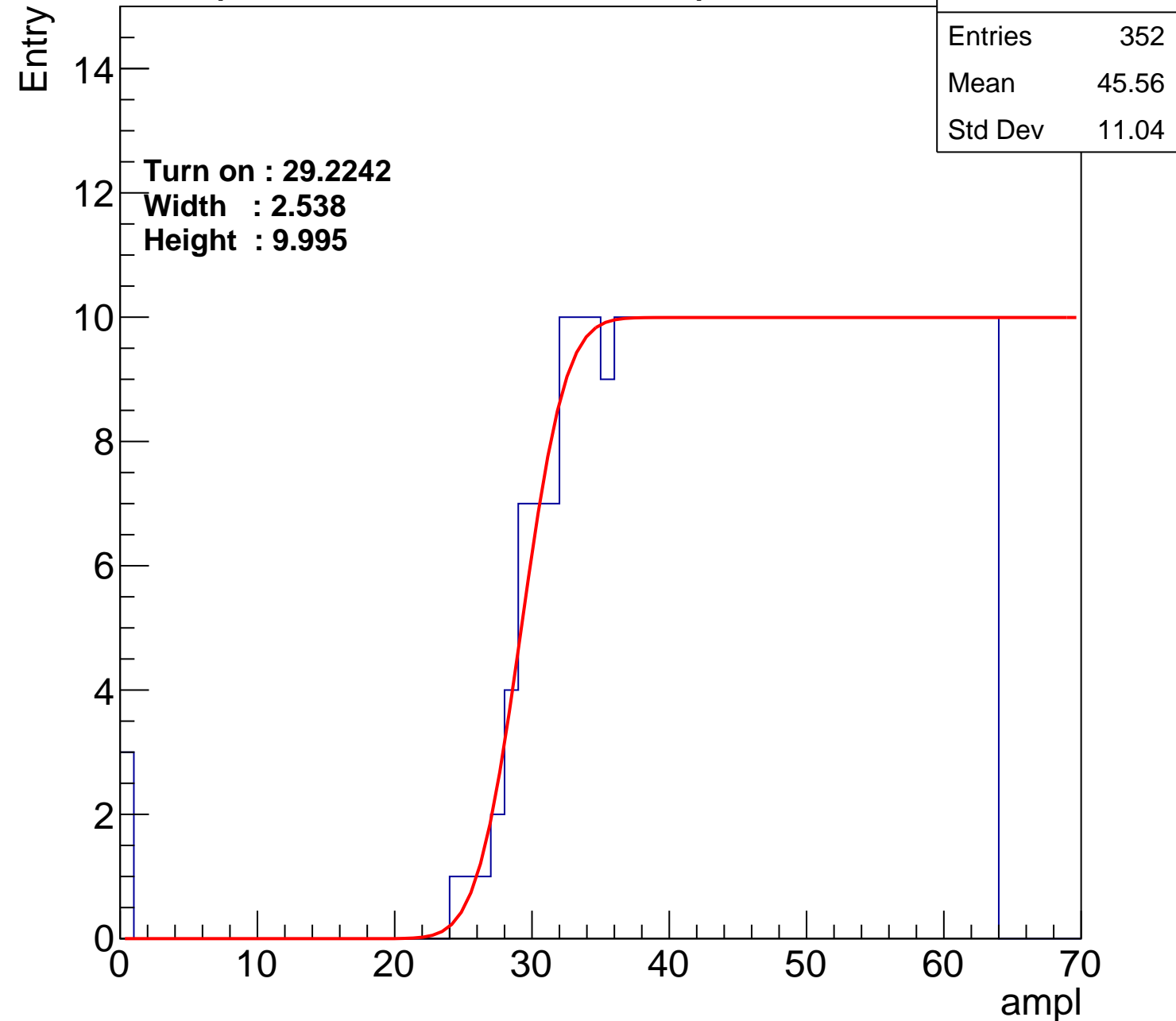
Width : 2.538

Height : 9.995

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch12

calib_packv5_042523_0143.root, FC#0, port D2

Entries	383
Mean	44.12
Std Dev	11.59

Turn on : 26.1932

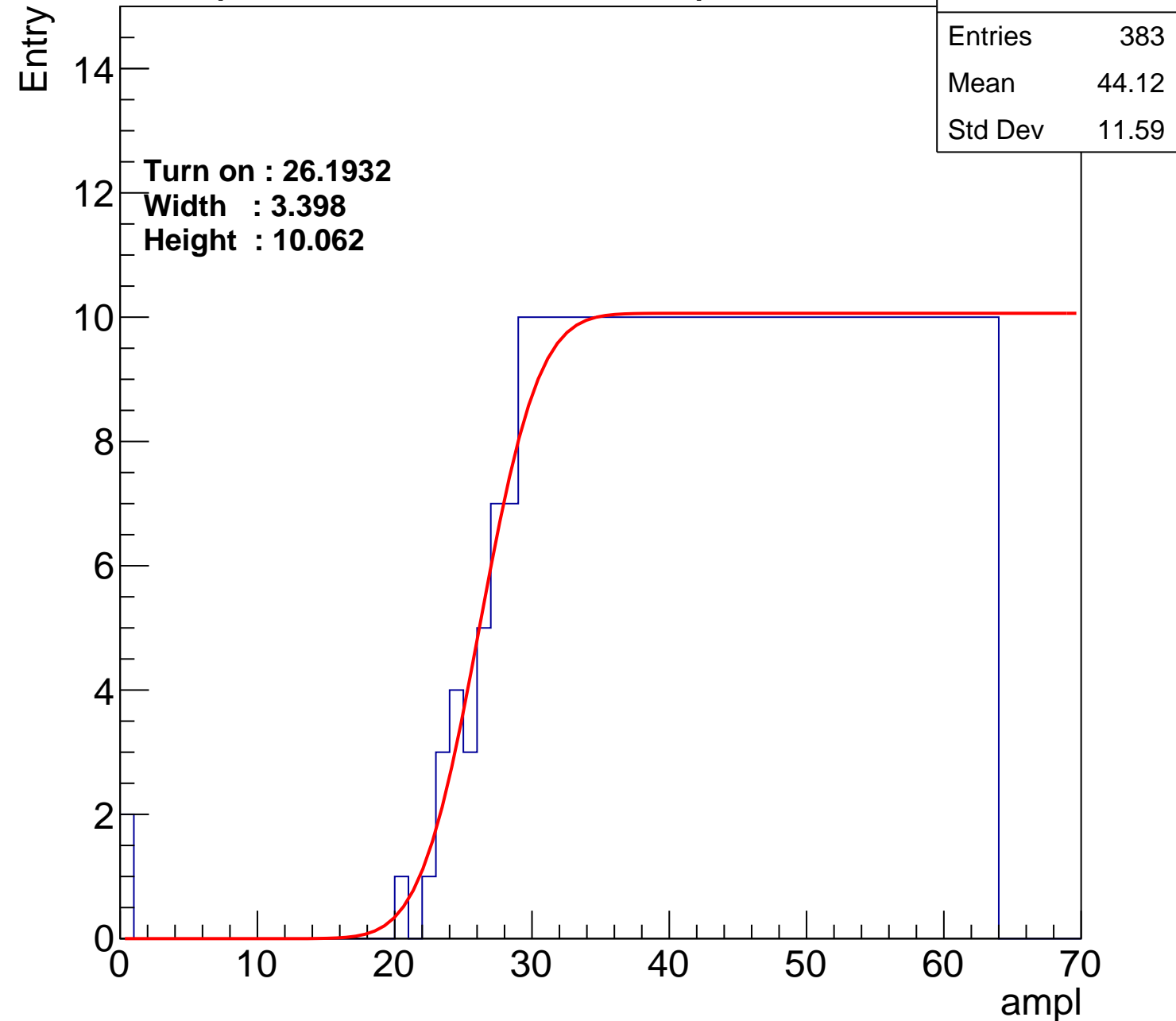
Width : 3.398

Height : 10.062

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch13

calib_packv5_042523_0143.root, FC#0, port D2

Entries	381
Mean	44.04
Std Dev	12.03

Turn on : 26.6343

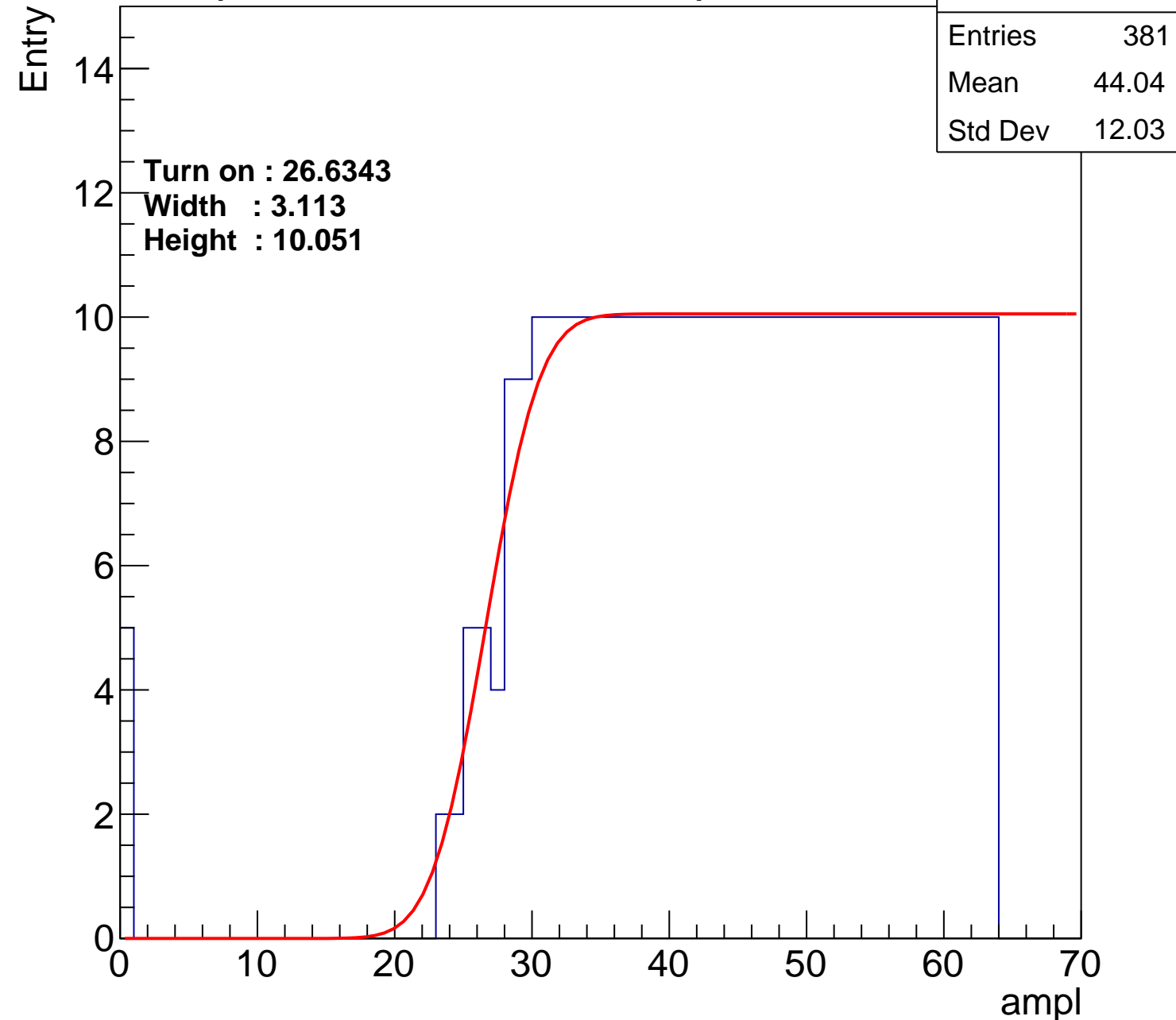
Width : 3.113

Height : 10.051

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch14

calib_packv5_042523_0143.root, FC#0, port D2

Entries	388
Mean	43.85
Std Dev	11.75

Turn on : 26.1690

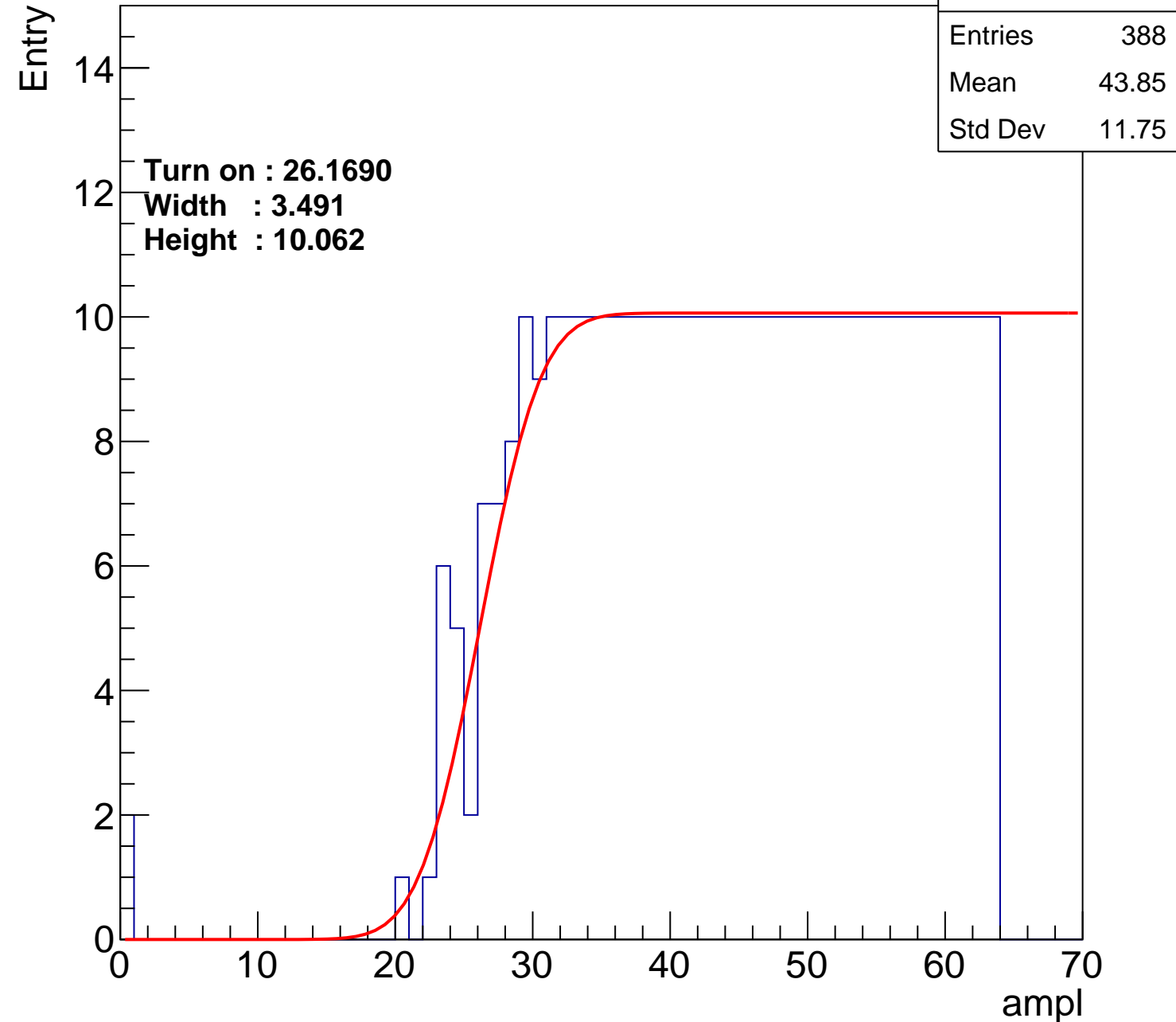
Width : 3.491

Height : 10.062

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch15

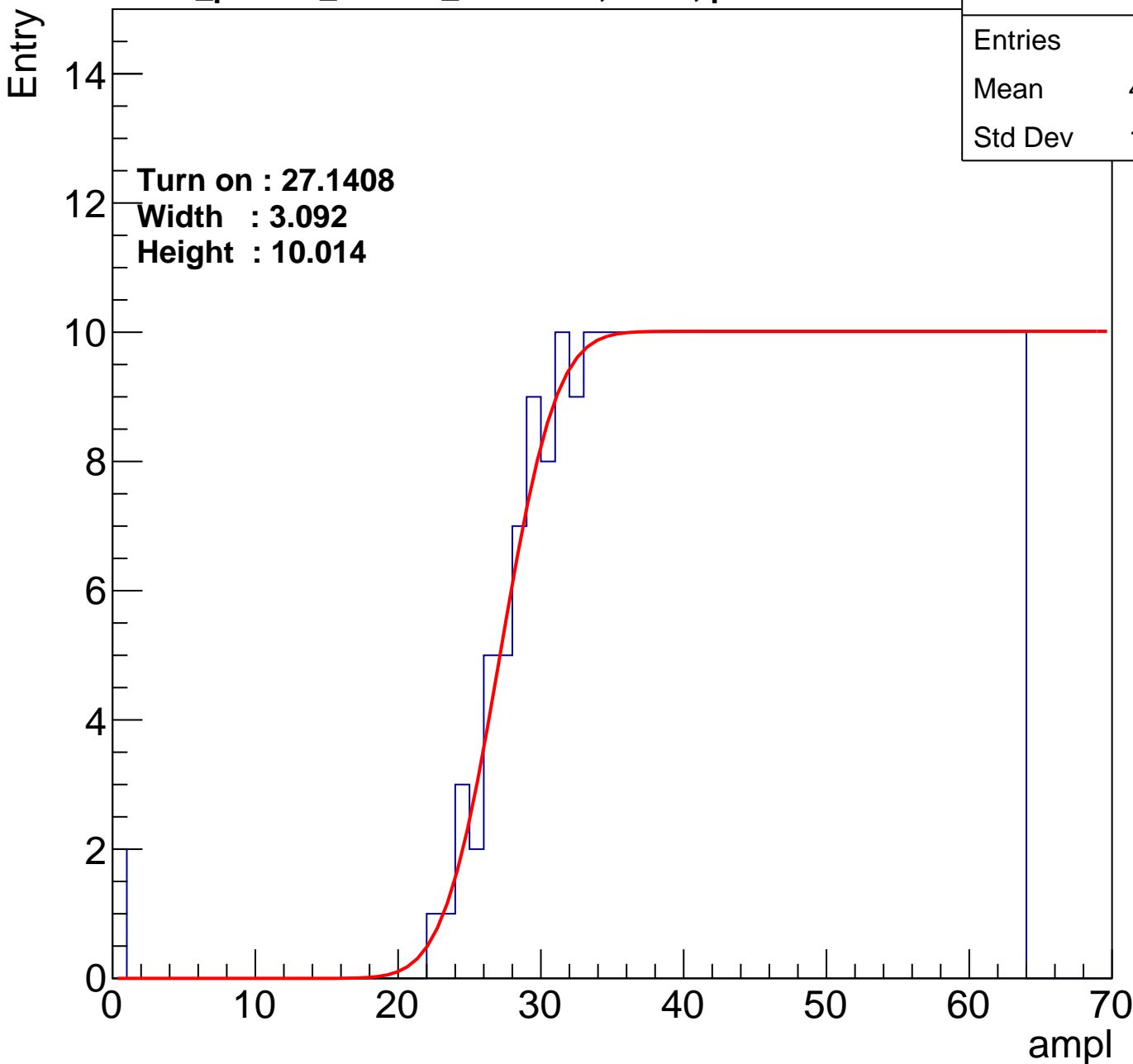
calib_packv5_042523_0143.root, FC#0, port D2

Entries	372
Mean	44.64
Std Dev	11.33

Turn on : 27.1408

Width : 3.092

Height : 10.014



B1L101S, U8-ch16

calib_packv5_042523_0143.root, FC#0, port D2

Entries	374
Mean	44.48
Std Dev	11.56

Turn on : 27.6749

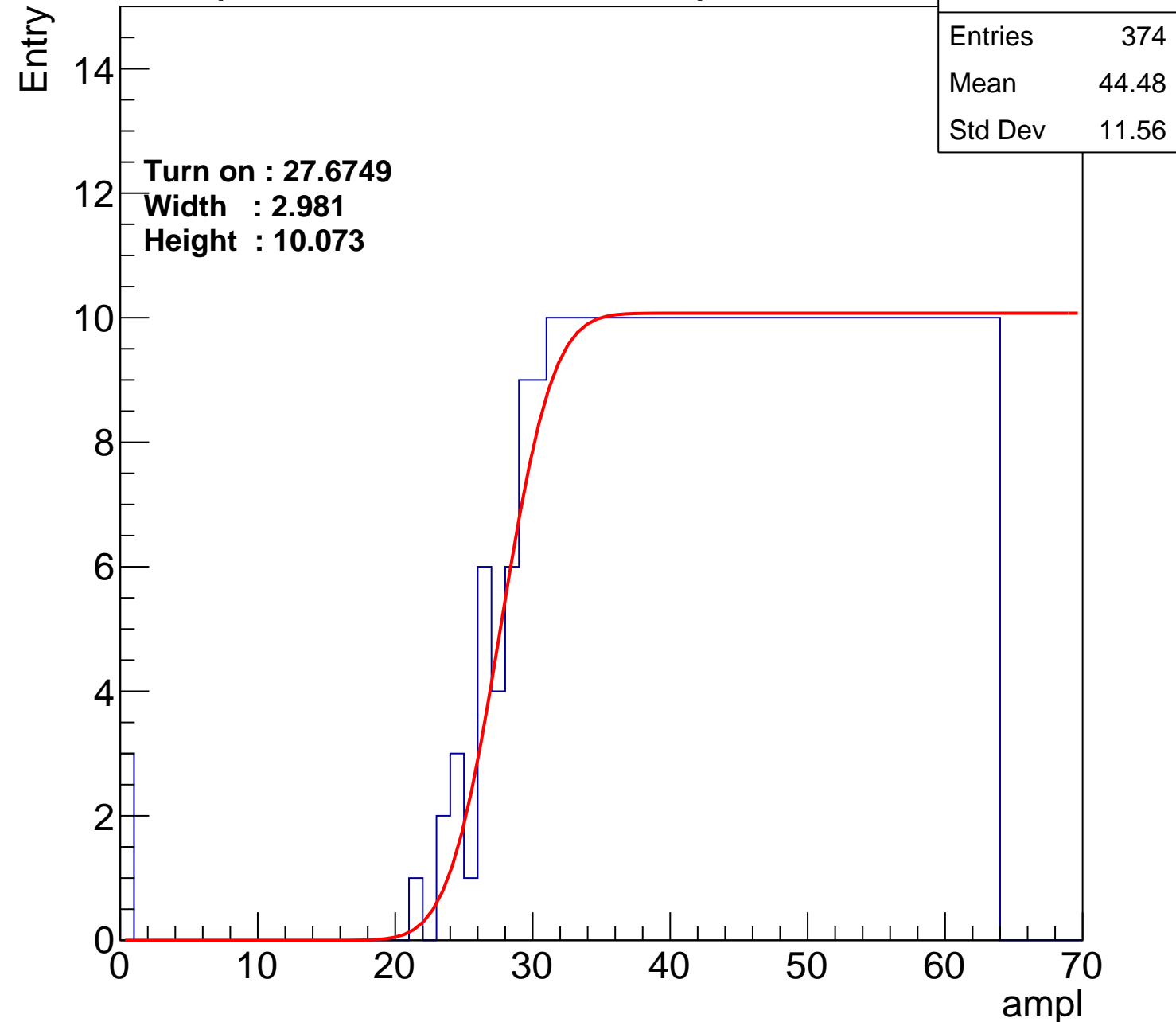
Width : 2.981

Height : 10.073

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch17

calib_packv5_042523_0143.root, FC#0, port D2

Entries	363
Mean	45.06
Std Dev	11.24

Turn on : 28.0823

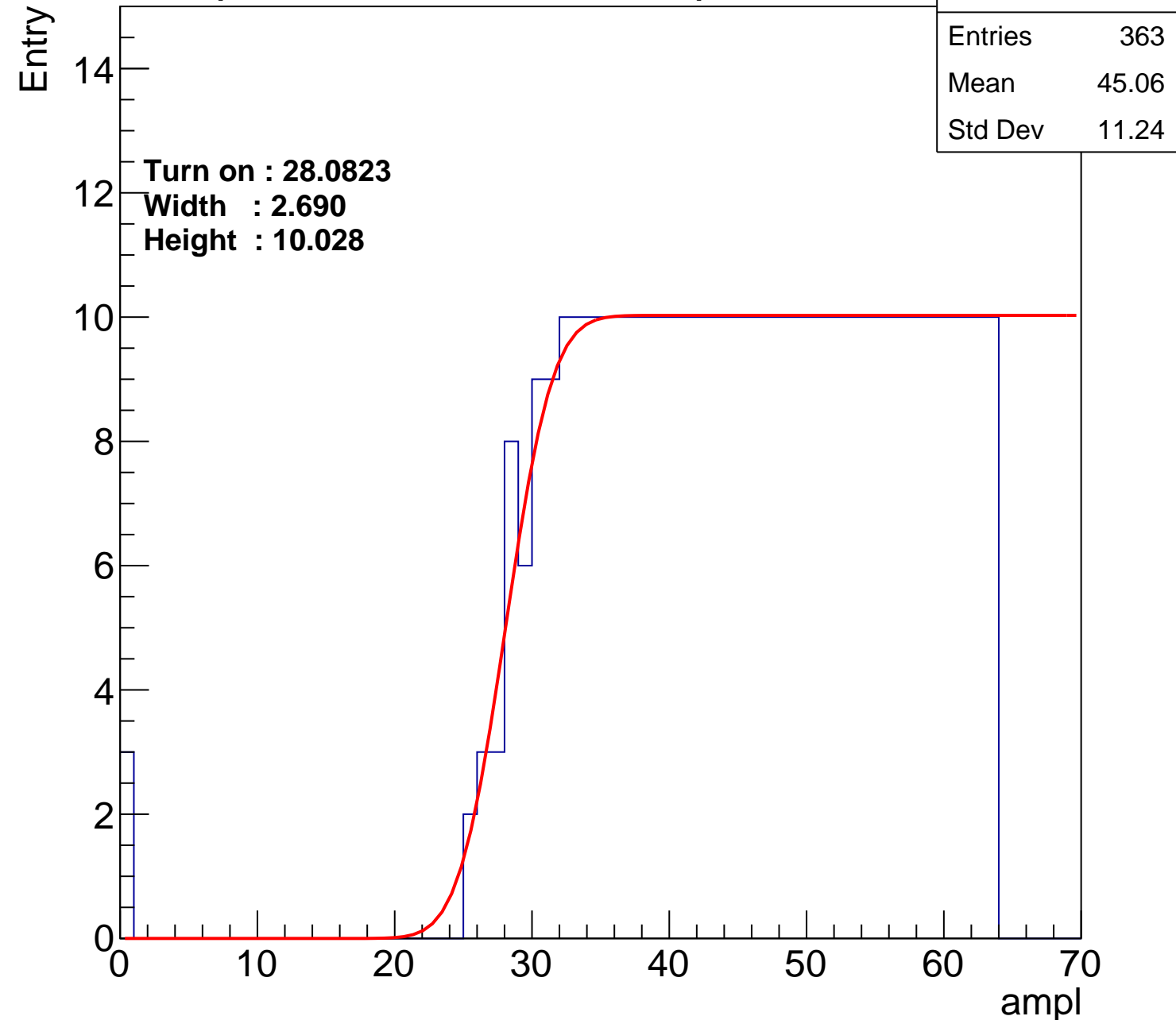
Width : 2.690

Height : 10.028

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch18

calib_packv5_042523_0143.root, FC#0, port D2

Entries	389
Mean	43.71
Std Dev	12.05

Turn on : 25.8435

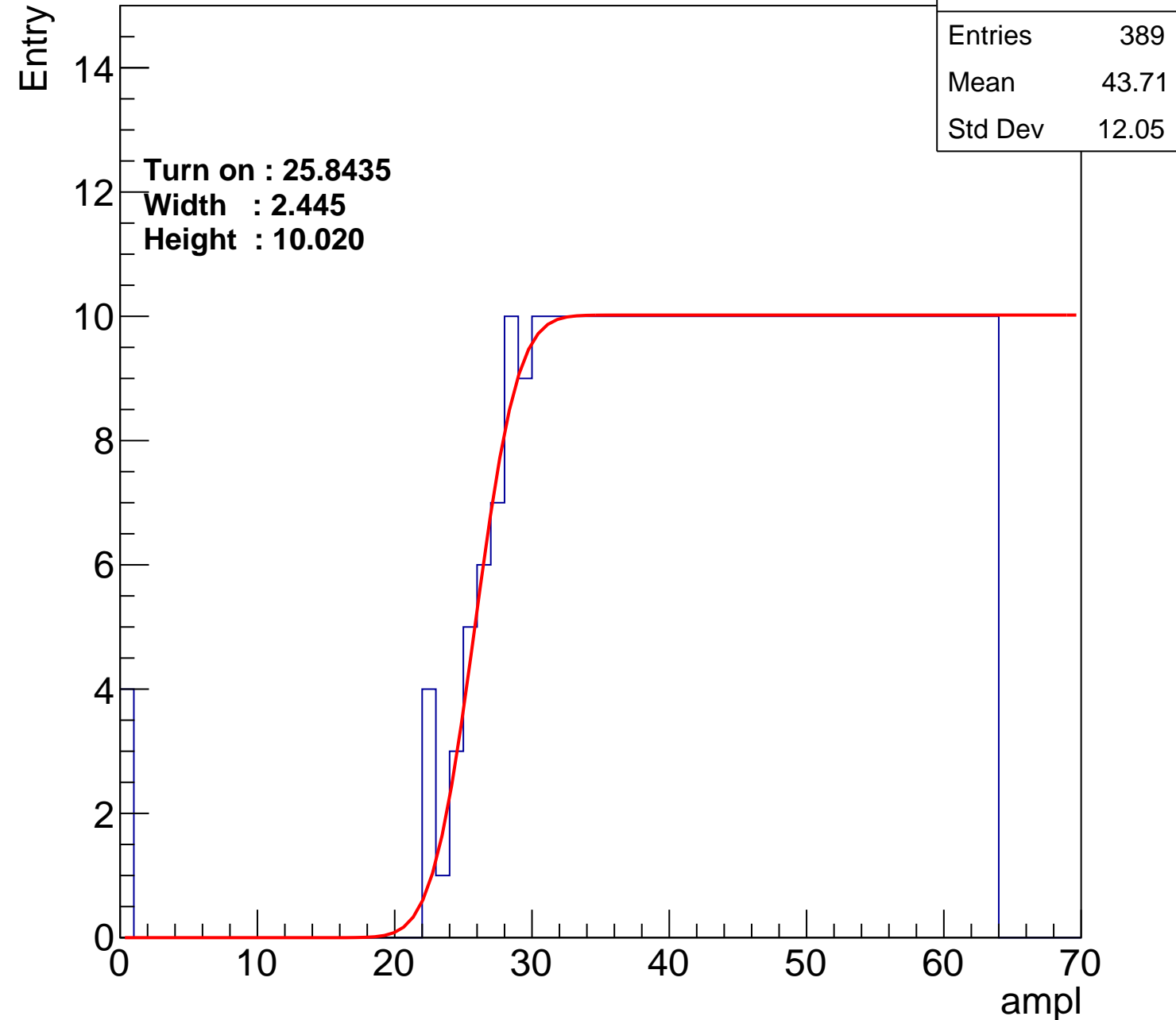
Width : 2.445

Height : 10.020

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch19

calib_packv5_042523_0143.root, FC#0, port D2

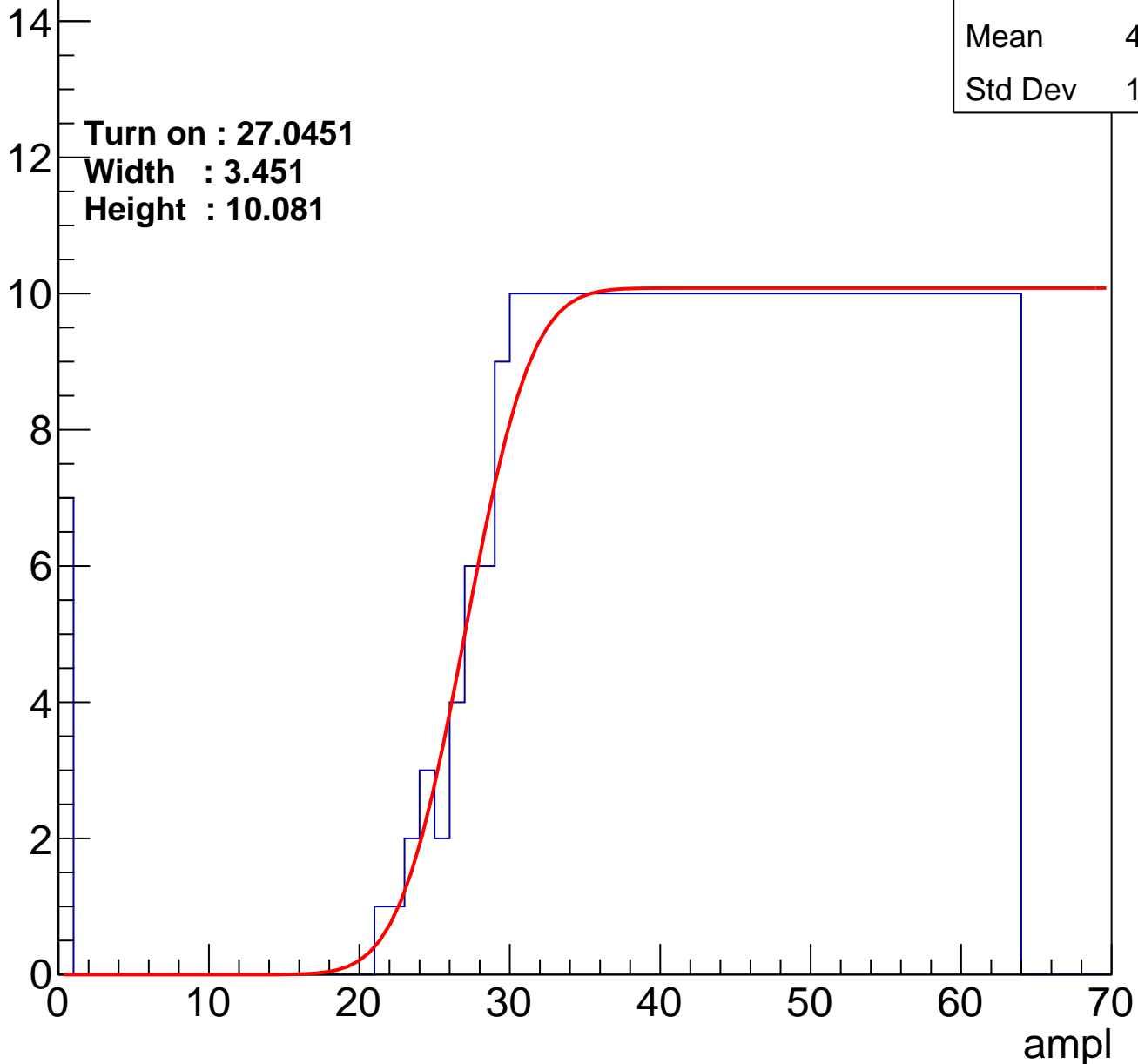
Entries	381
Mean	43.87
Std Dev	12.42

Turn on : 27.0451

Width : 3.451

Height : 10.081

Entry



B1L101S, U8-ch20

calib_packv5_042523_0143.root, FC#0, port D2

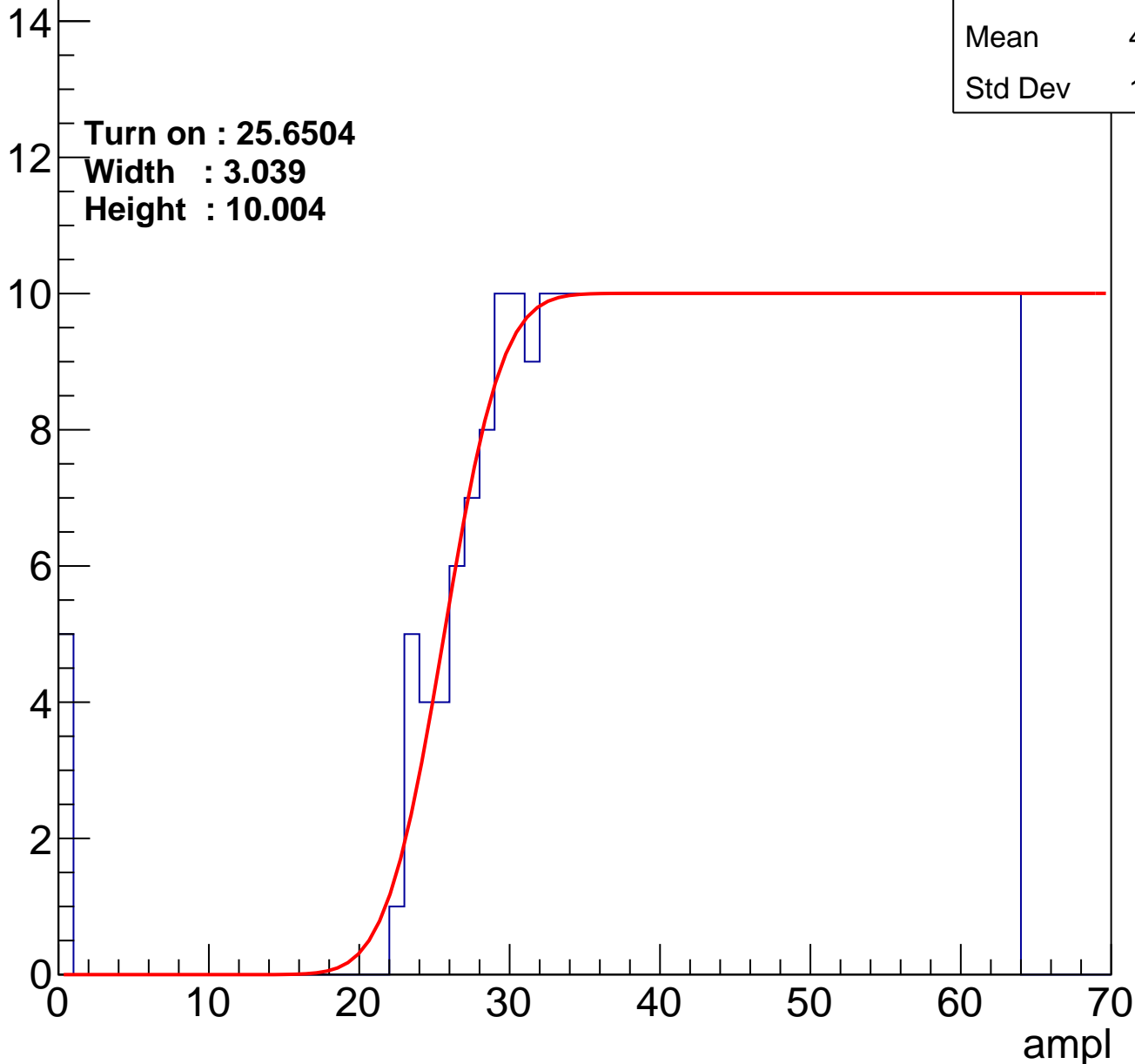
Entries	389
Mean	43.63
Std Dev	12.24

Turn on : 25.6504

Width : 3.039

Height : 10.004

Entry



B1L101S, U8-ch21

calib_packv5_042523_0143.root, FC#0, port D2

Entries	368
Mean	44.83
Std Dev	11.24

Turn on : 28.1874

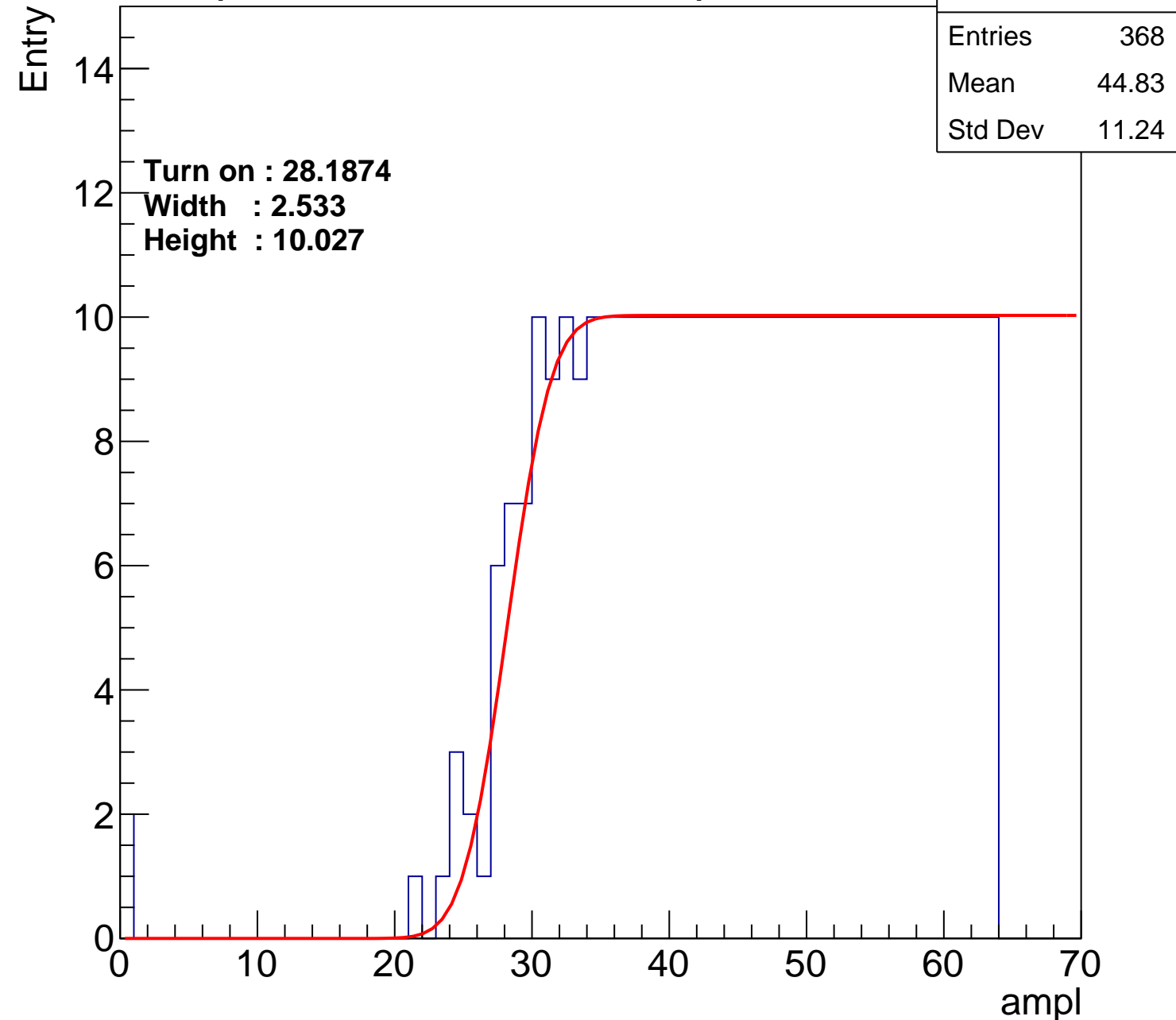
Width : 2.533

Height : 10.027

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch22

calib_packv5_042523_0143.root, FC#0, port D2

Entries	365
Mean	45.01
Std Dev	11.12

Turn on : 27.9998

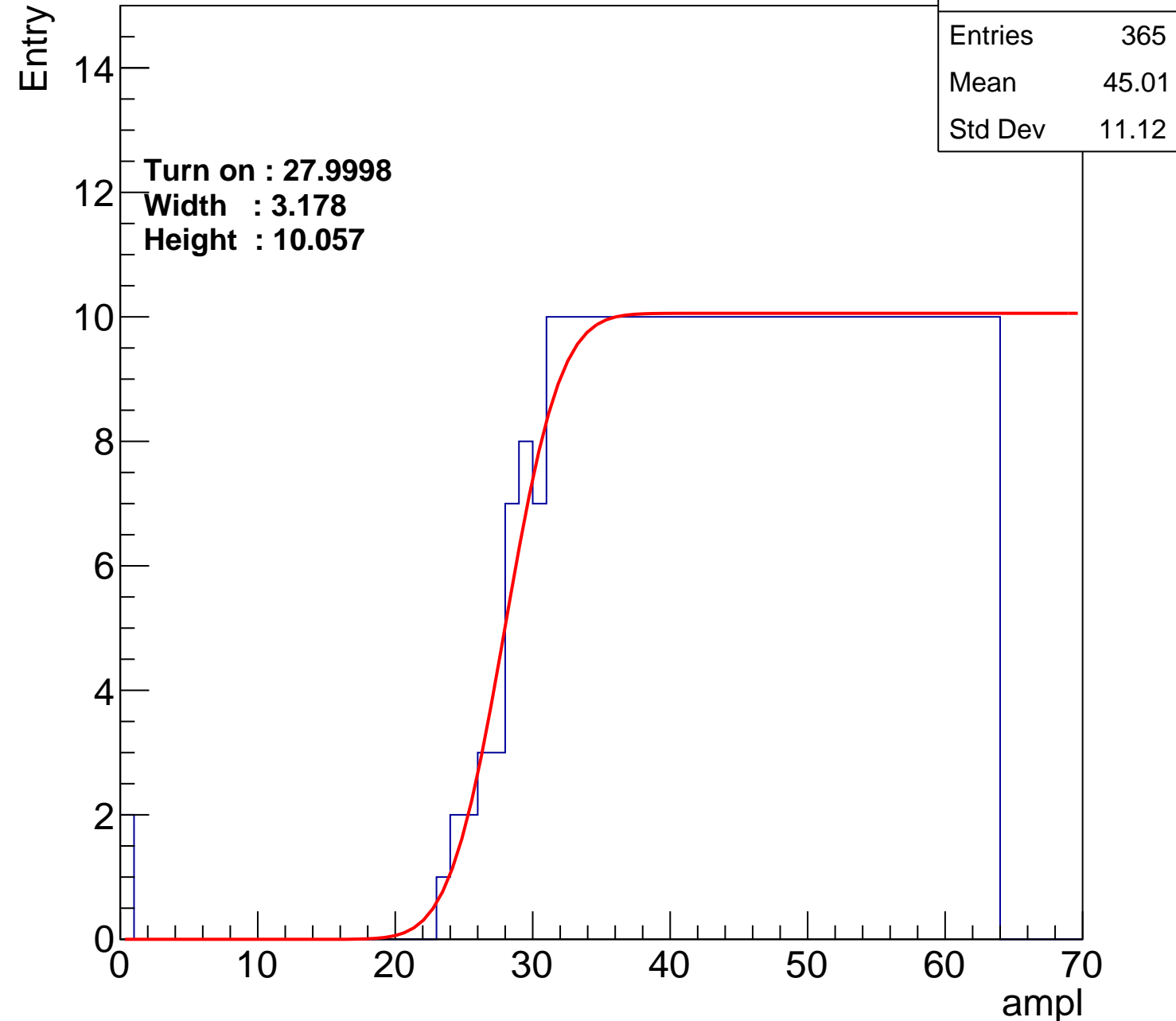
Width : 3.178

Height : 10.057

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch23

calib_packv5_042523_0143.root, FC#0, port D2

Entries	380
Mean	44.08
Std Dev	12.02

Turn on : 26.6098

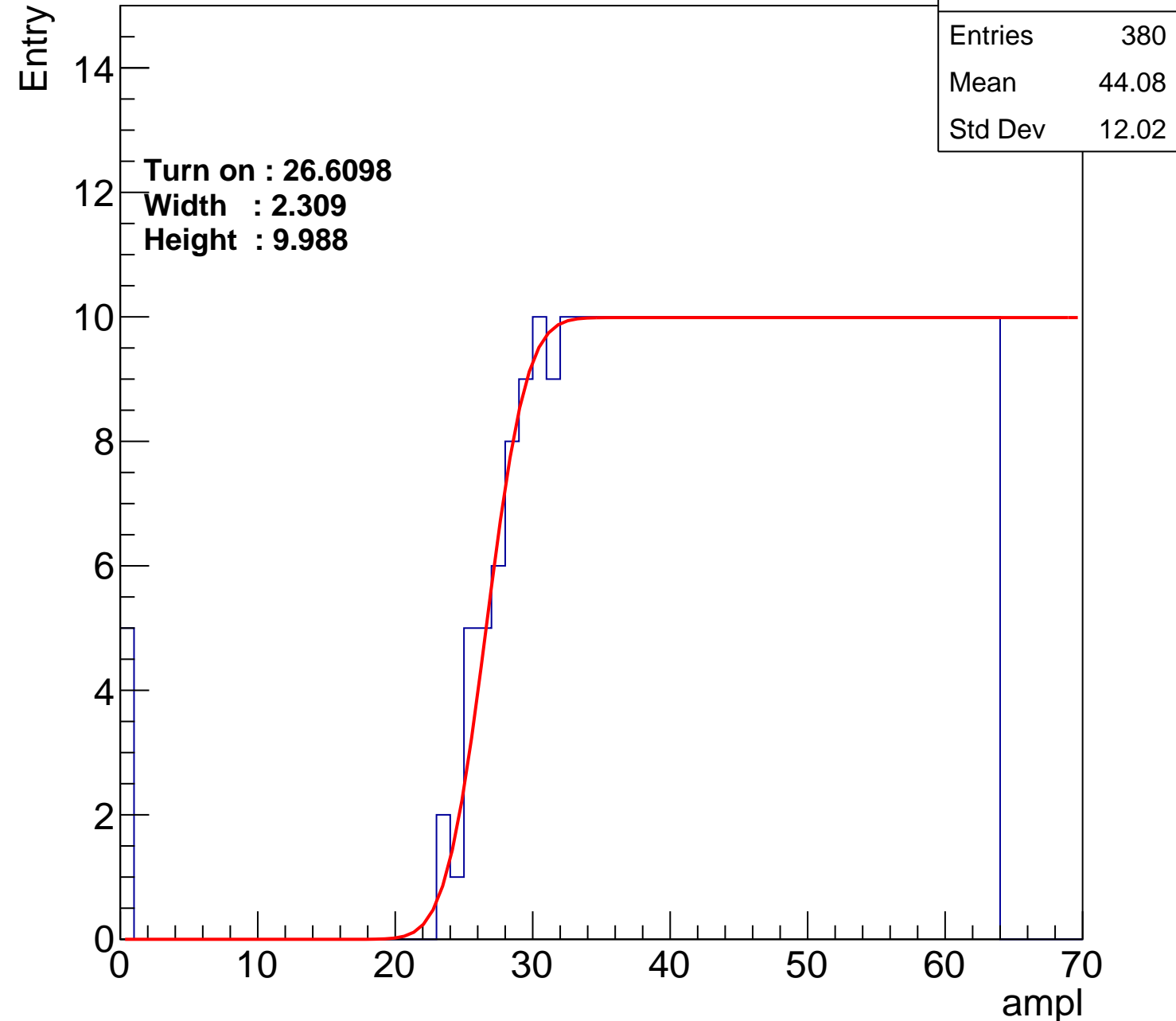
Width : 2.309

Height : 9.988

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch24

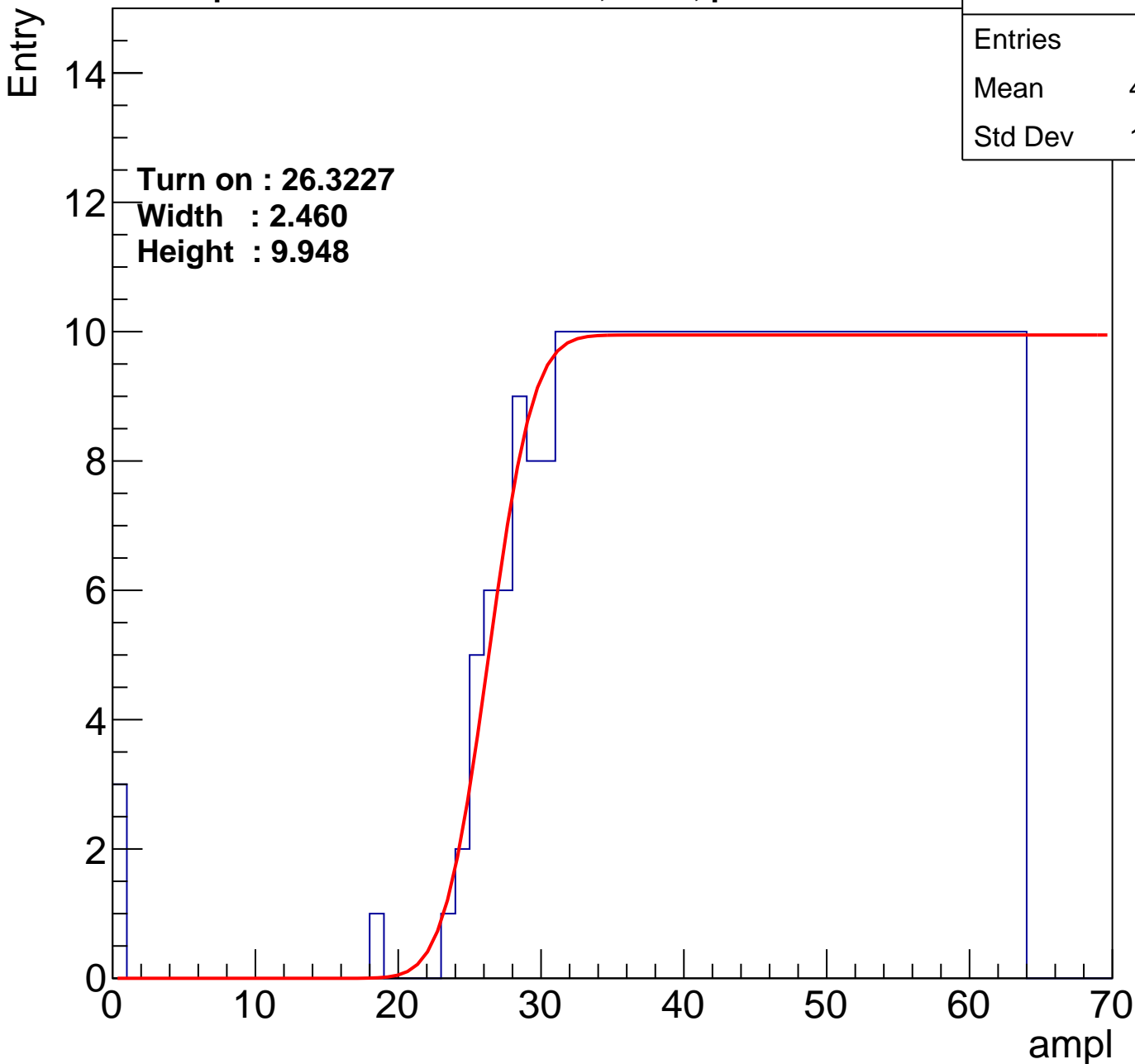
calib_packv5_042523_0143.root, FC#0, port D2

Entries	379
Mean	44.24
Std Dev	11.69

Turn on : 26.3227

Width : 2.460

Height : 9.948



B1L101S, U8-ch25

calib_packv5_042523_0143.root, FC#0, port D2

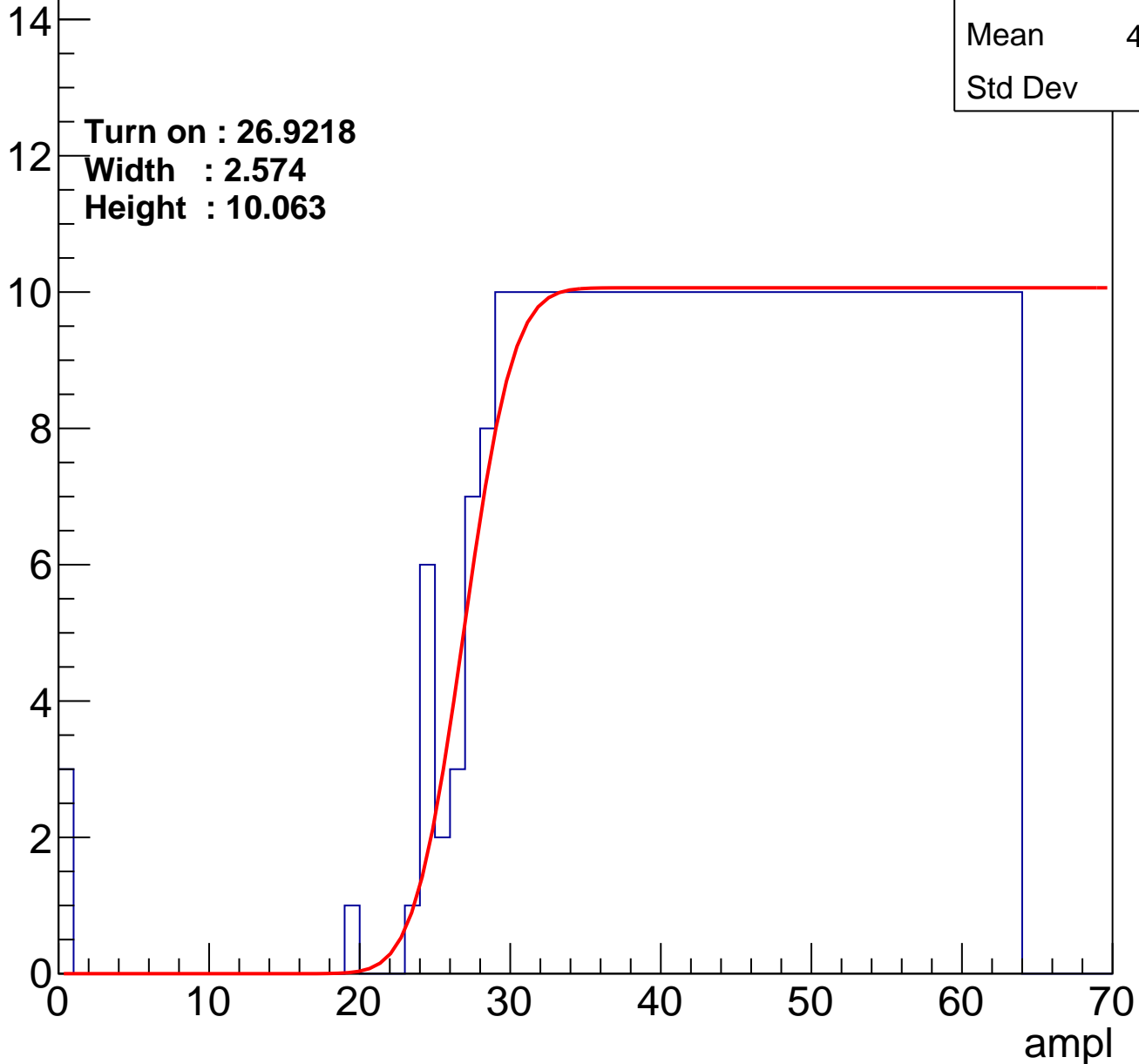
Entries	381
Mean	44.17
Std Dev	11.7

Turn on : 26.9218

Width : 2.574

Height : 10.063

Entry



B1L101S, U8-ch26

calib_packv5_042523_0143.root, FC#0, port D2

Entries	397
Mean	43.36
Std Dev	12.13

Turn on : 24.2252

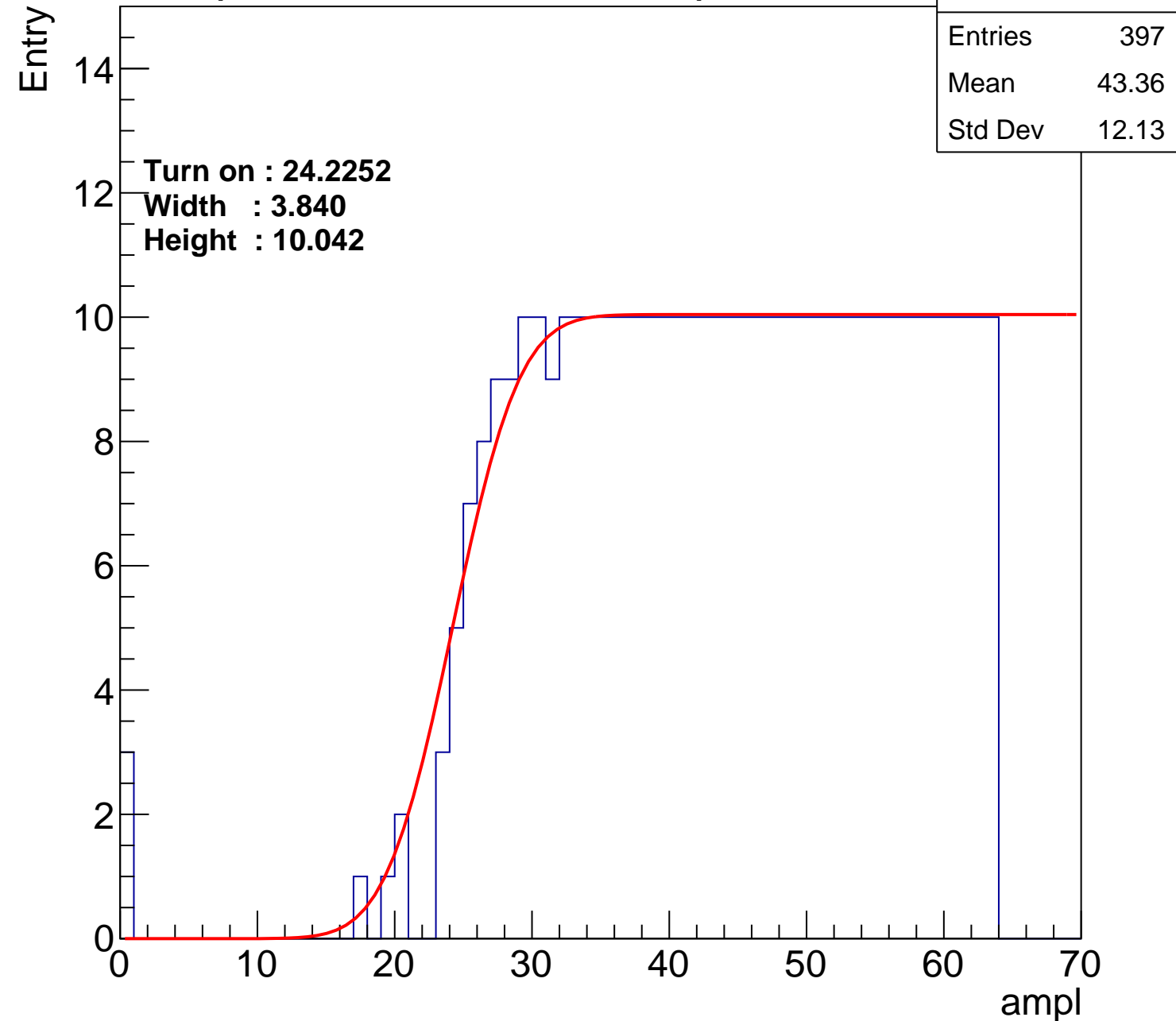
Width : 3.840

Height : 10.042

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch27

calib_packv5_042523_0143.root, FC#0, port D2

Entries	372
Mean	44.45
Std Dev	11.87

Turn on : 28.2015

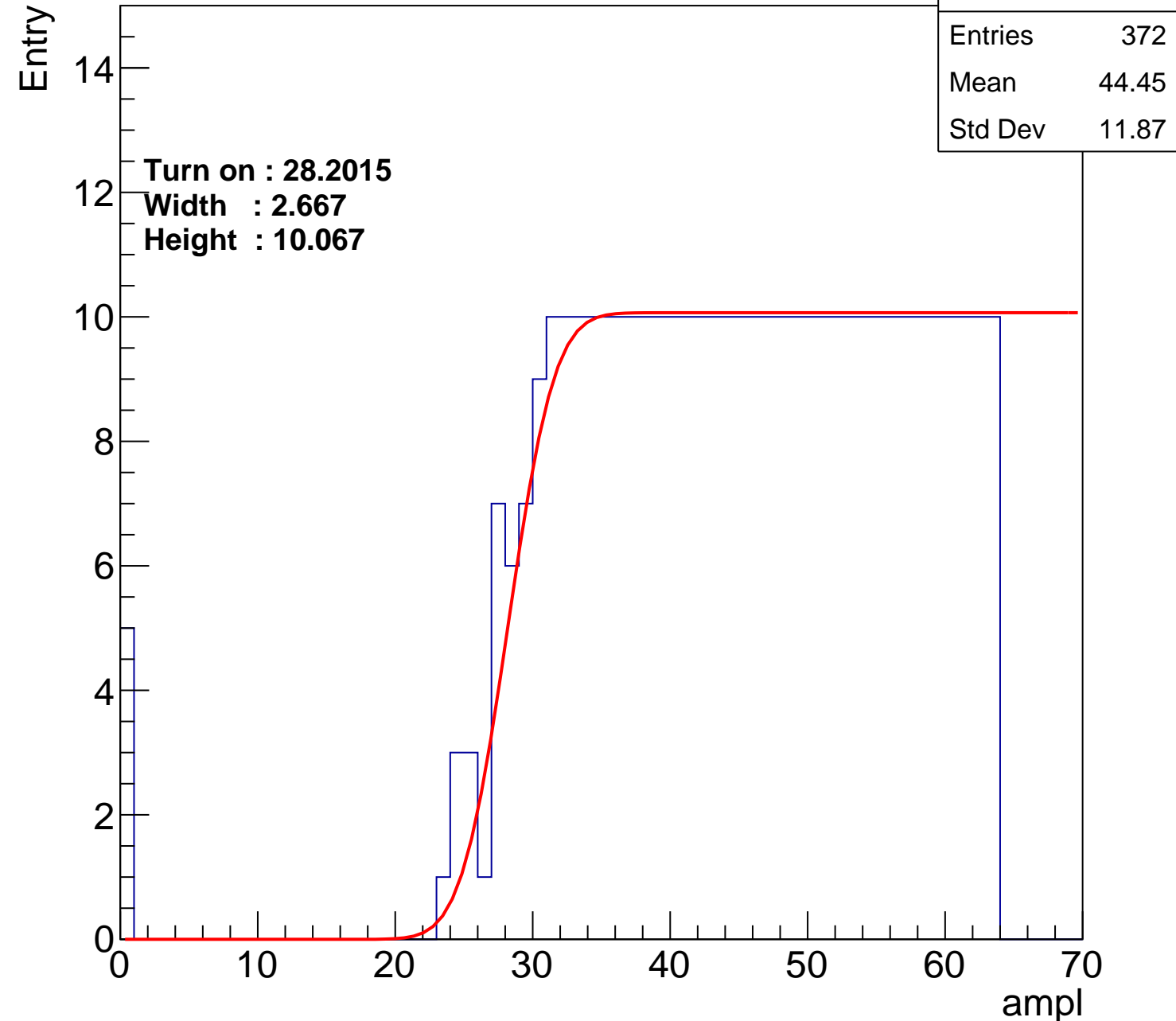
Width : 2.667

Height : 10.067

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch28

calib_packv5_042523_0143.root, FC#0, port D2

Entries	375
Mean	44.58
Std Dev	11.18

Turn on : 26.4348

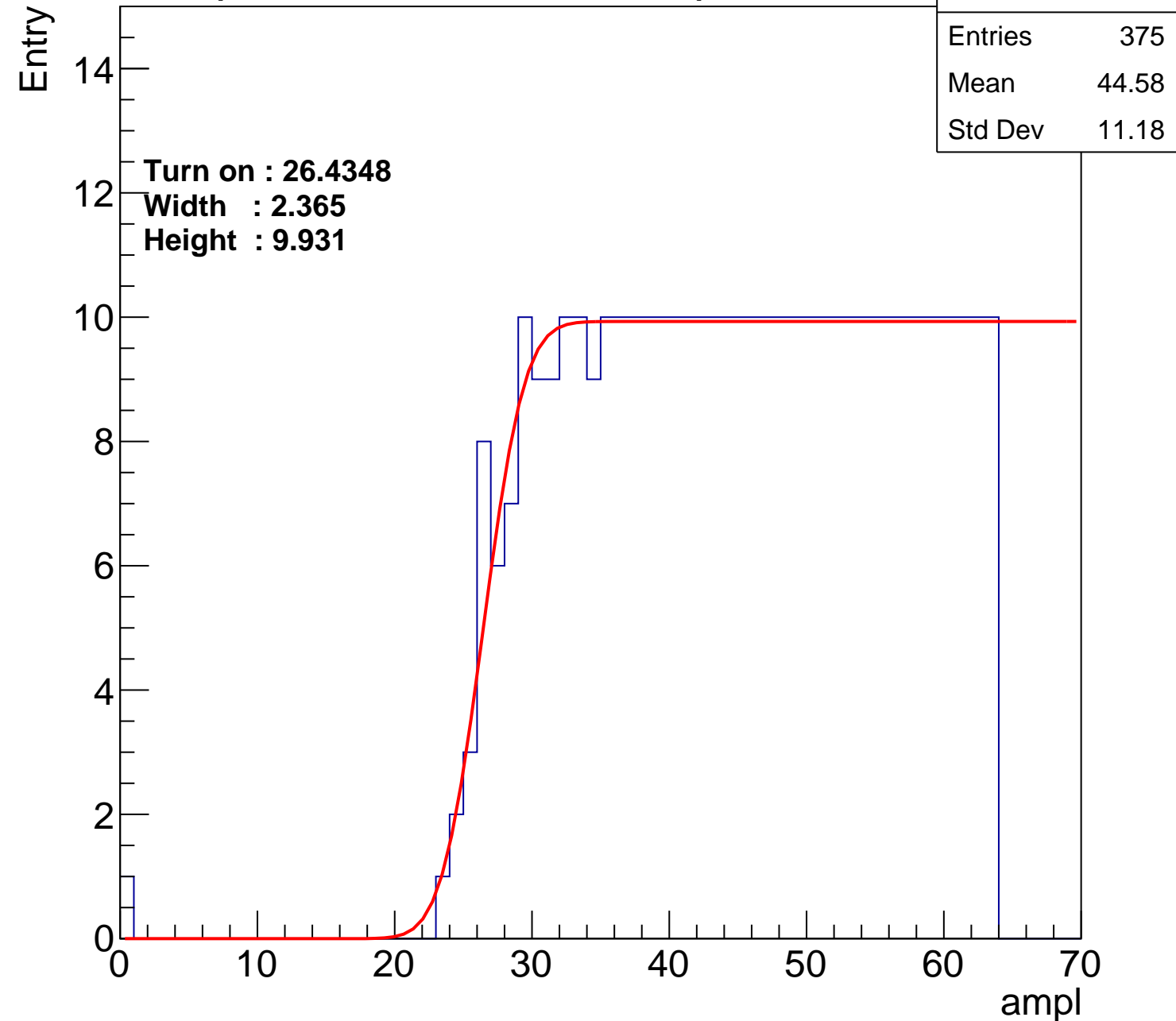
Width : 2.365

Height : 9.931

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch29

calib_packv5_042523_0143.root, FC#0, port D2

Entries	391
Mean	43.79
Std Dev	11.62

Turn on : 24.9293

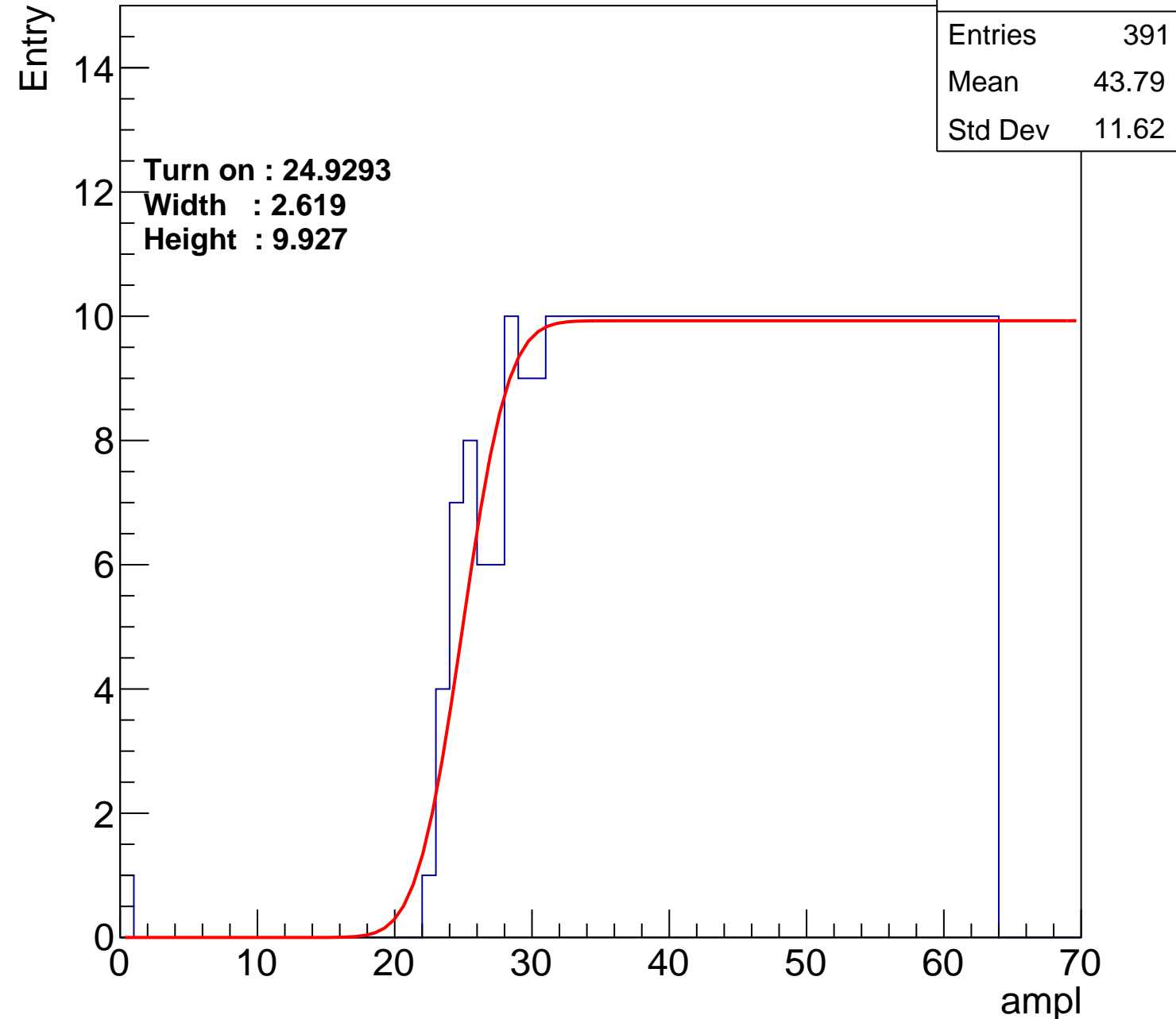
Width : 2.619

Height : 9.927

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch30

calib_packv5_042523_0143.root, FC#0, port D2

Entries	376
Mean	44.4
Std Dev	11.58

Turn on : 26.3414

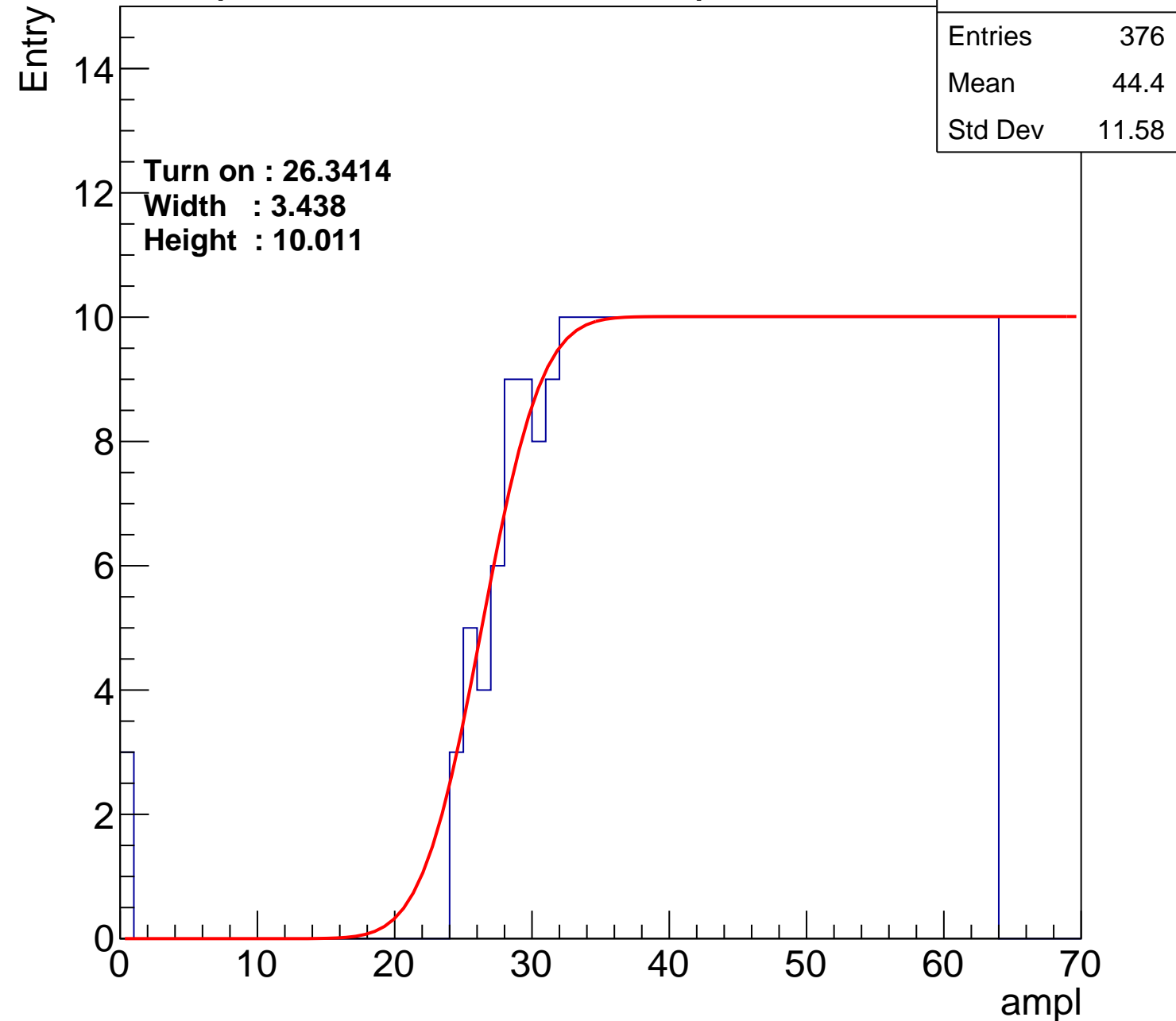
Width : 3.438

Height : 10.011

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch31

calib_packv5_042523_0143.root, FC#0, port D2

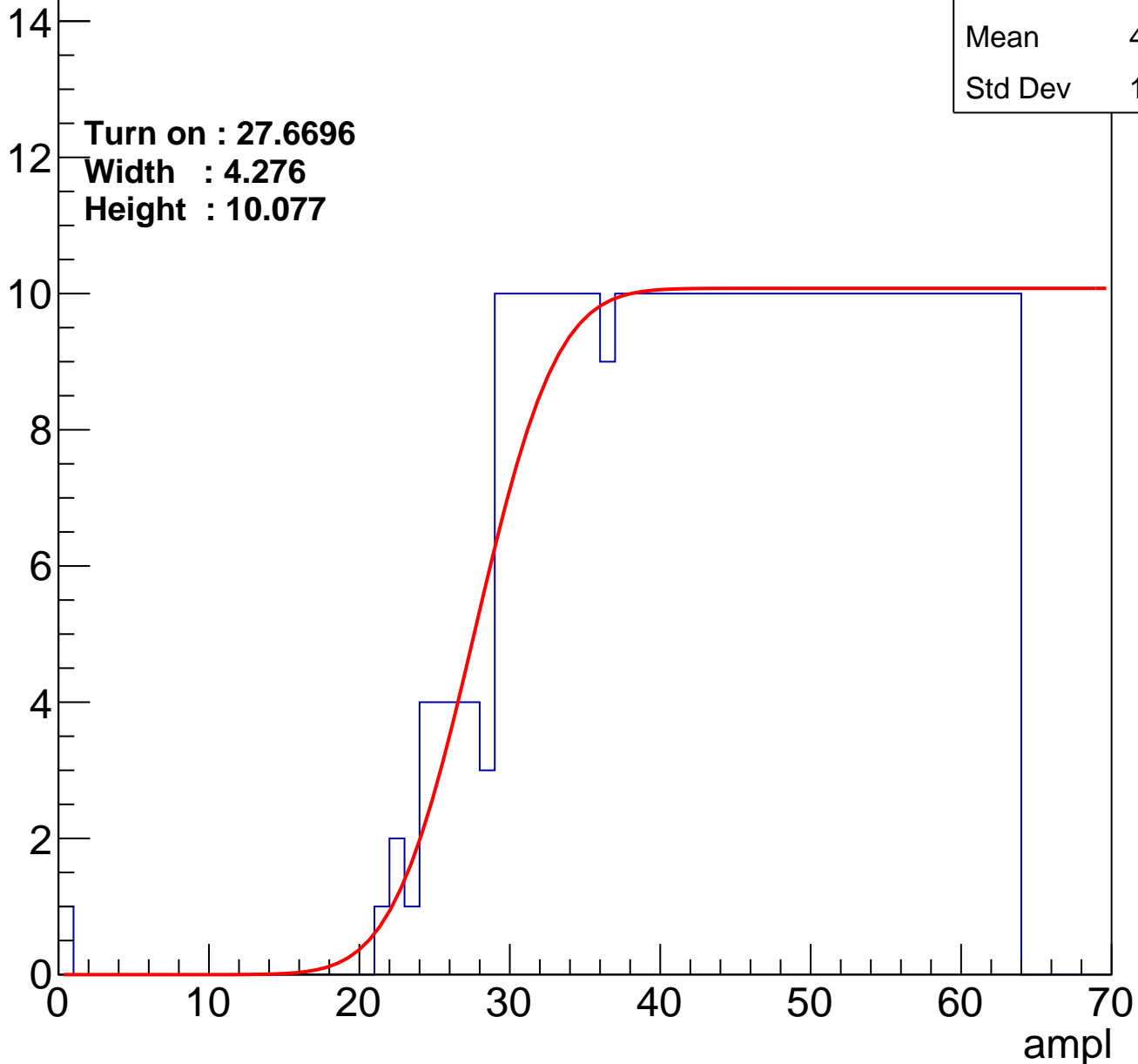
Entries	373
Mean	44.62
Std Dev	11.23

Turn on : 27.6696

Width : 4.276

Height : 10.077

Entry



B1L101S, U8-ch32

calib_packv5_042523_0143.root, FC#0, port D2

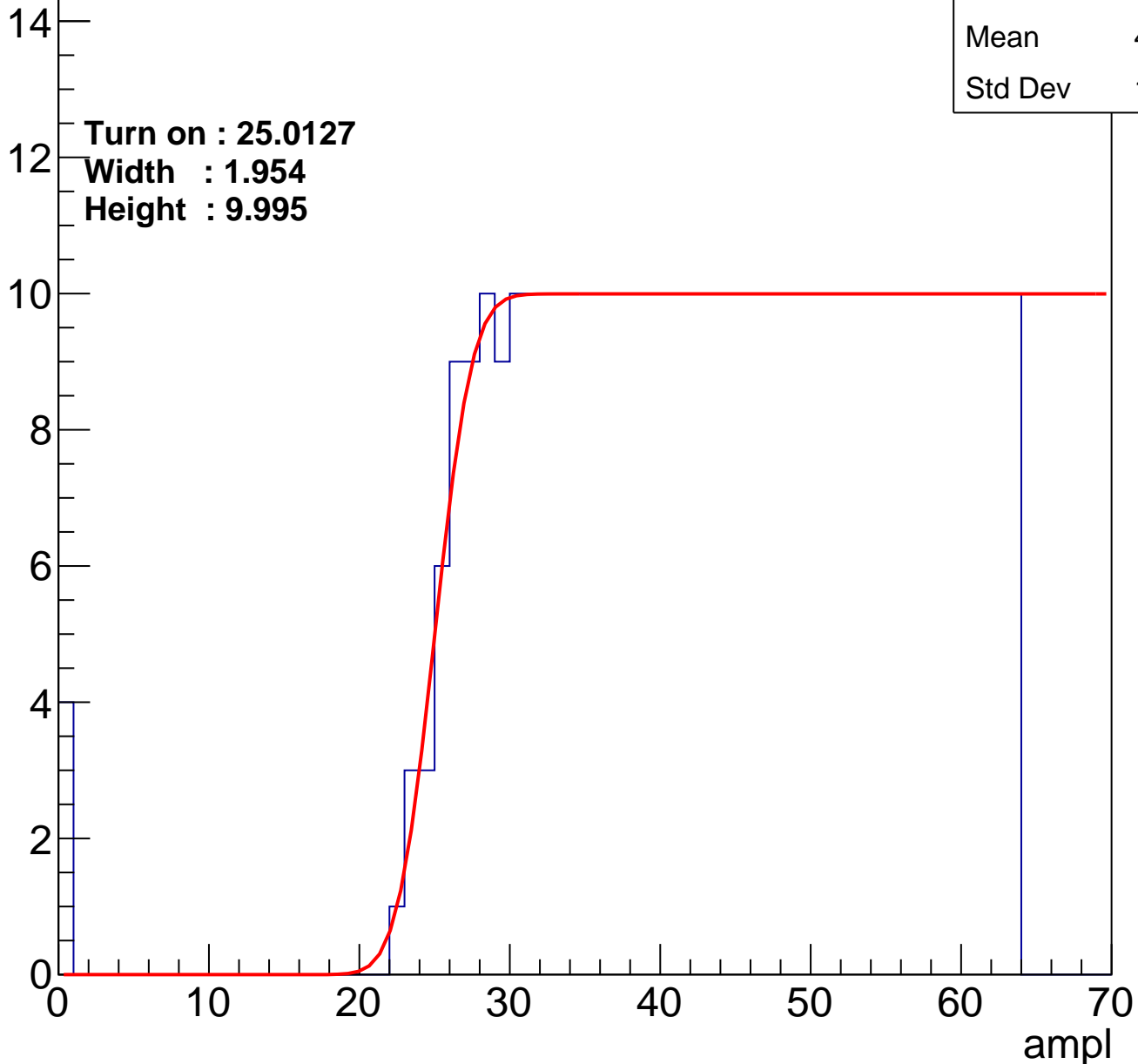
Entries	394
Mean	43.51
Std Dev	12.11

Turn on : 25.0127

Width : 1.954

Height : 9.995

Entry



B1L101S, U8-ch33

calib_packv5_042523_0143.root, FC#0, port D2

Entries	356
Mean	45.35
Std Dev	11.16

Turn on : 28.6248

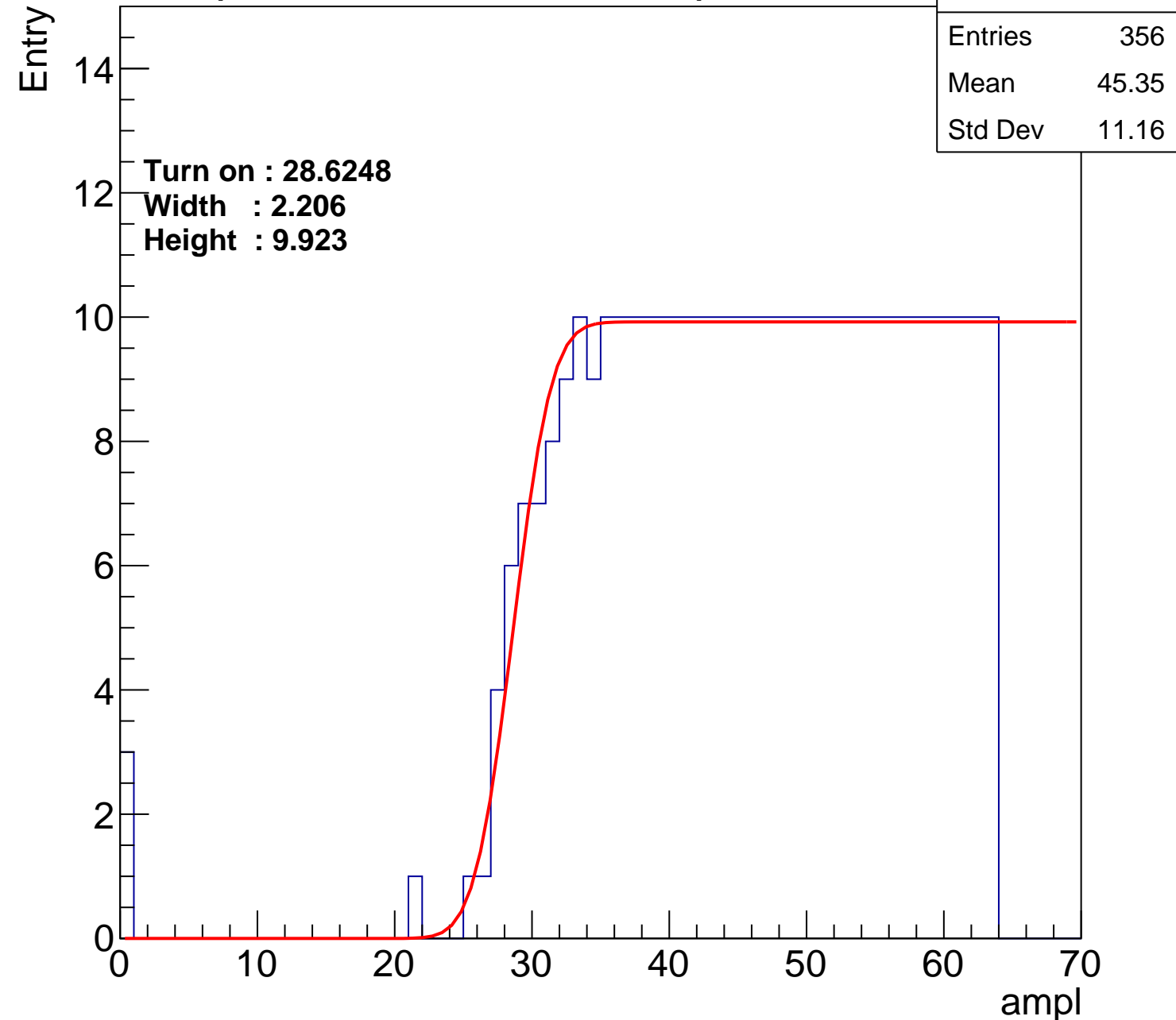
Width : 2.206

Height : 9.923

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch34

calib_packv5_042523_0143.root, FC#0, port D2

Entries	378
Mean	44.41
Std Dev	11.38

Turn on : 26.5937

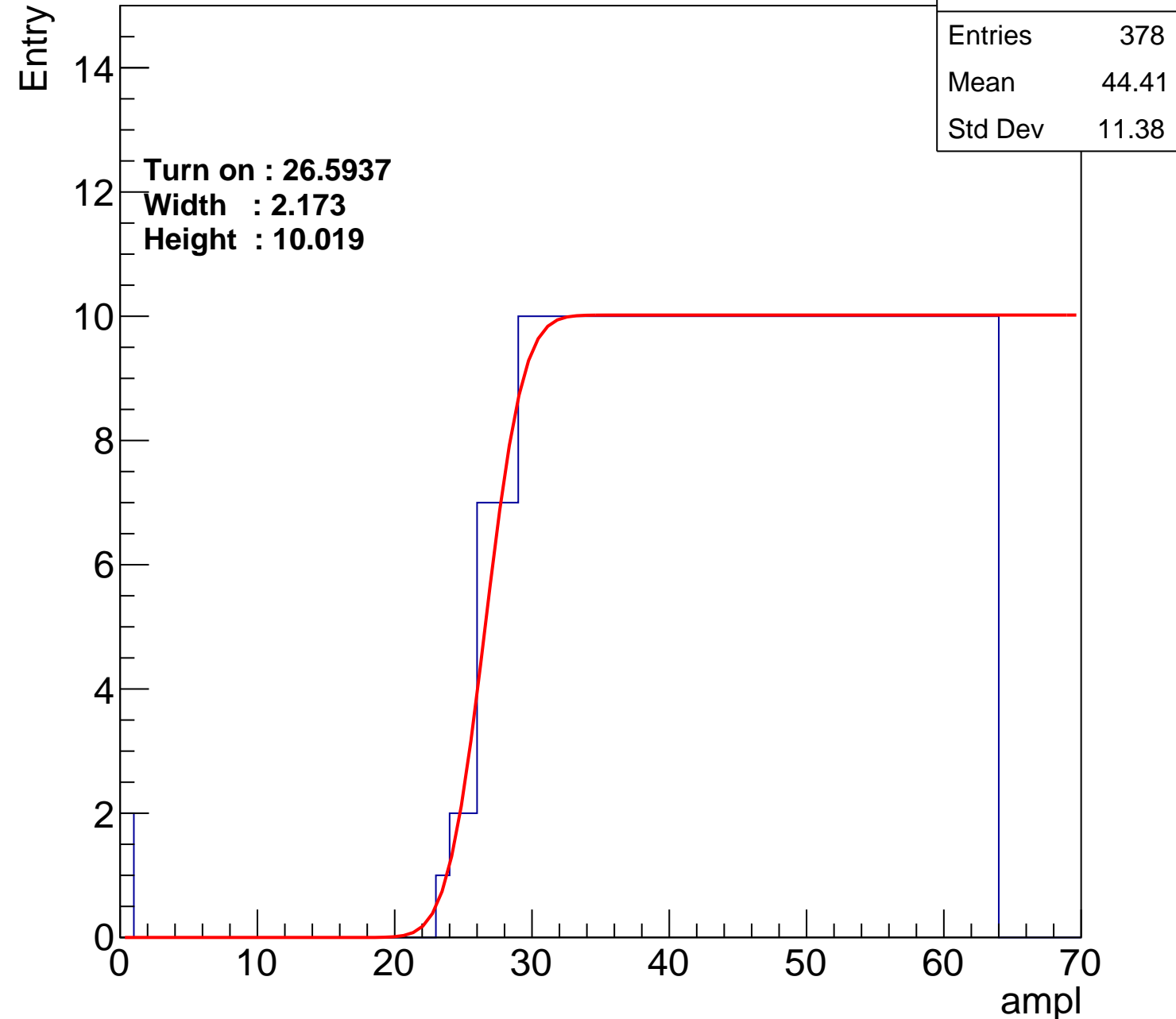
Width : 2.173

Height : 10.019

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch35

calib_packv5_042523_0143.root, FC#0, port D2

Entries	367
Mean	44.87
Std Dev	11.41

Turn on : 28.0297

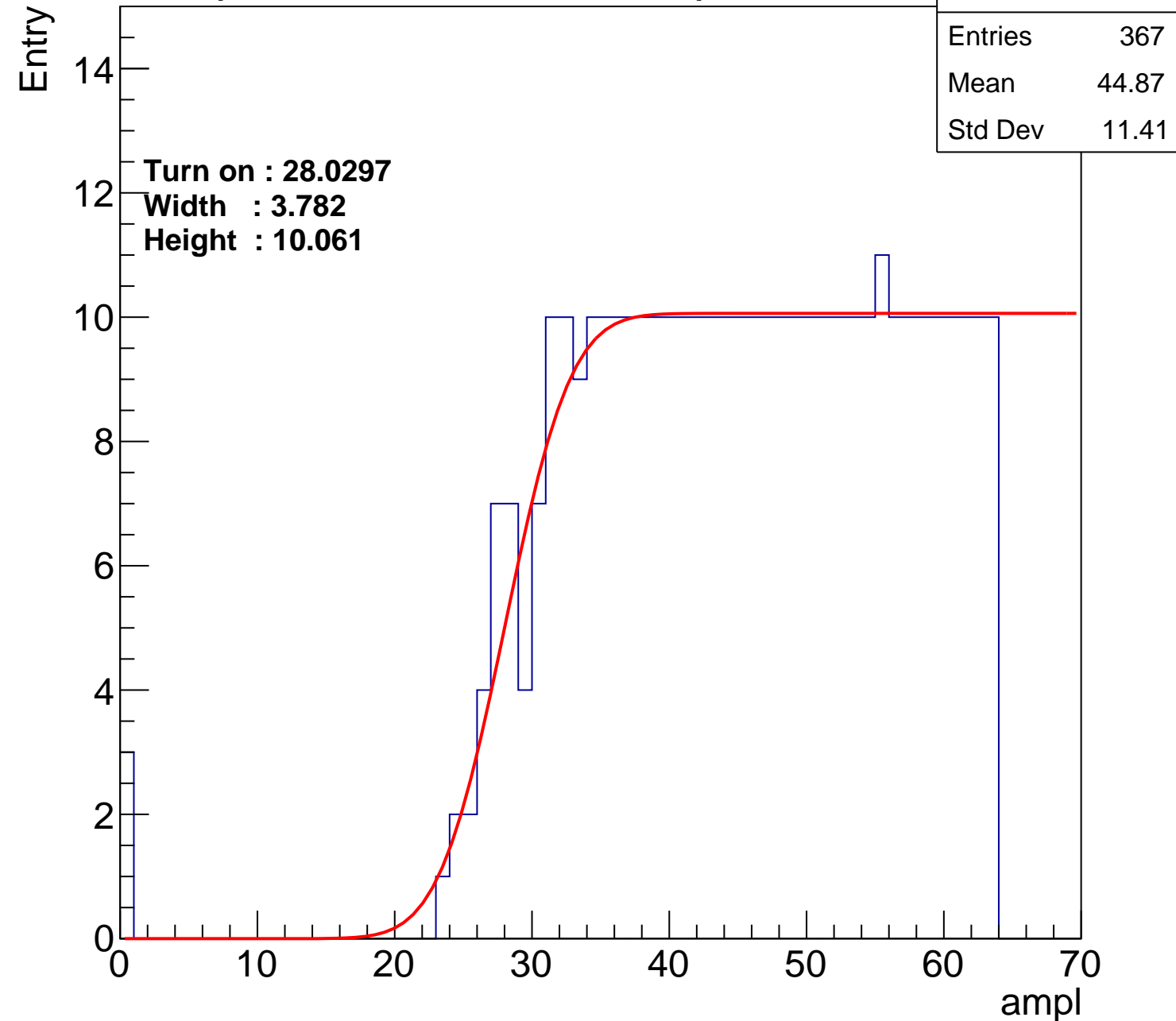
Width : 3.782

Height : 10.061

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch36

calib_packv5_042523_0143.root, FC#0, port D2

Entries	378
Mean	44.35
Std Dev	11.48

Turn on : 26.6396

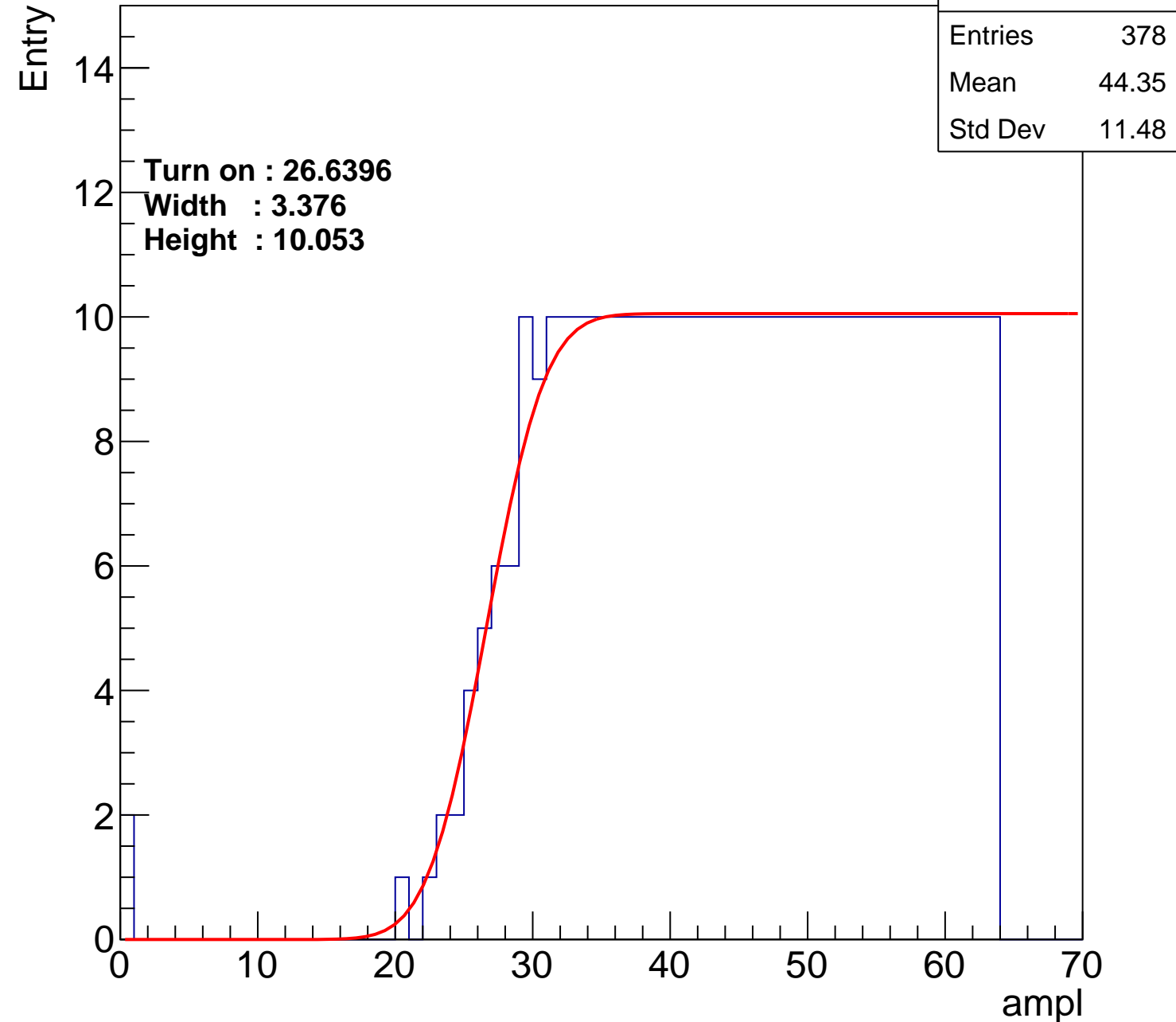
Width : 3.376

Height : 10.053

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch37

calib_packv5_042523_0143.root, FC#0, port D2

Entries	367
Mean	44.97
Std Dev	10.98

Turn on : 27.3893

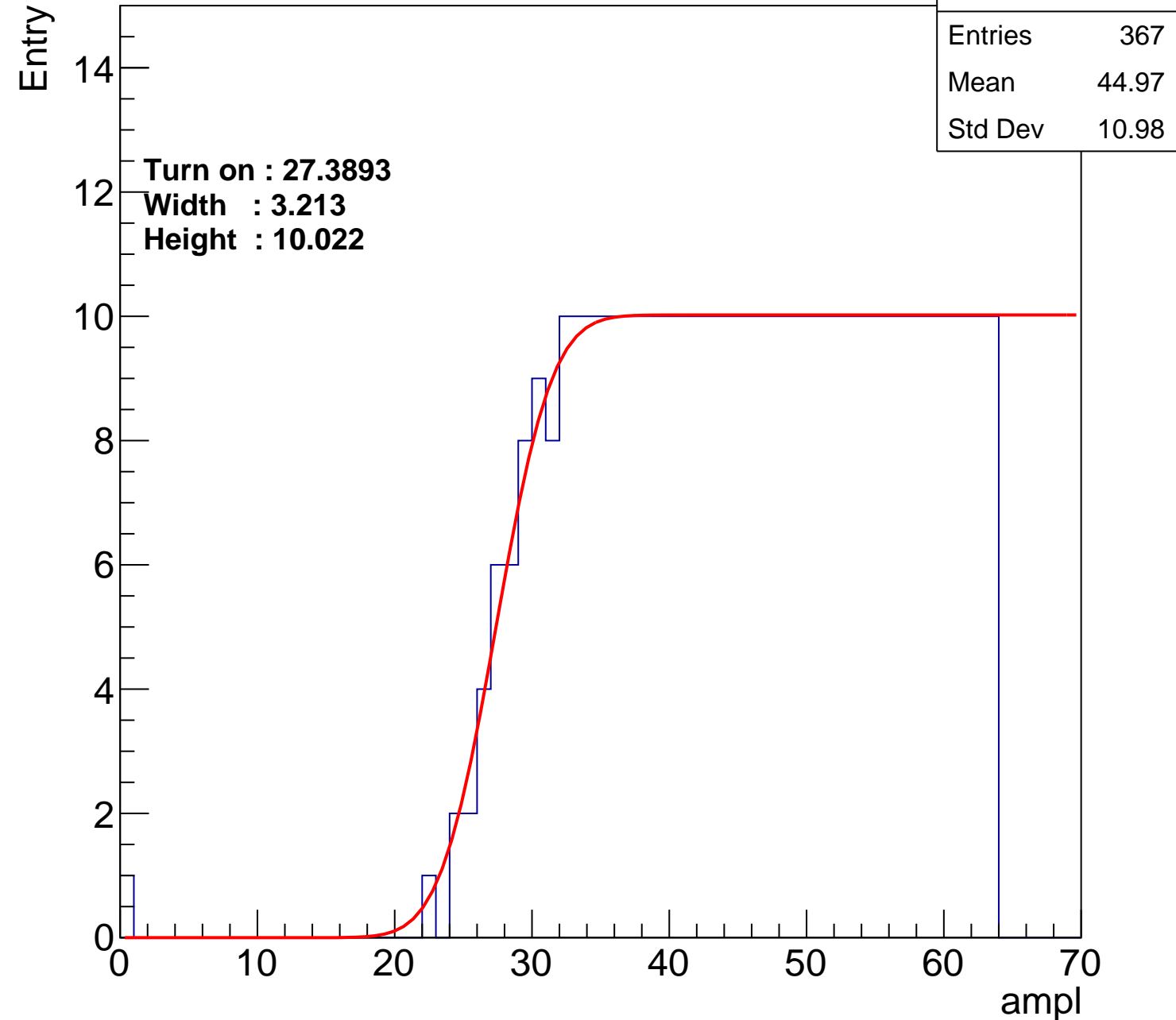
Width : 3.213

Height : 10.022

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch38

calib_packv5_042523_0143.root, FC#0, port D2

Entries	411
Mean	42.62
Std Dev	12.66

Turn on : 23.2064

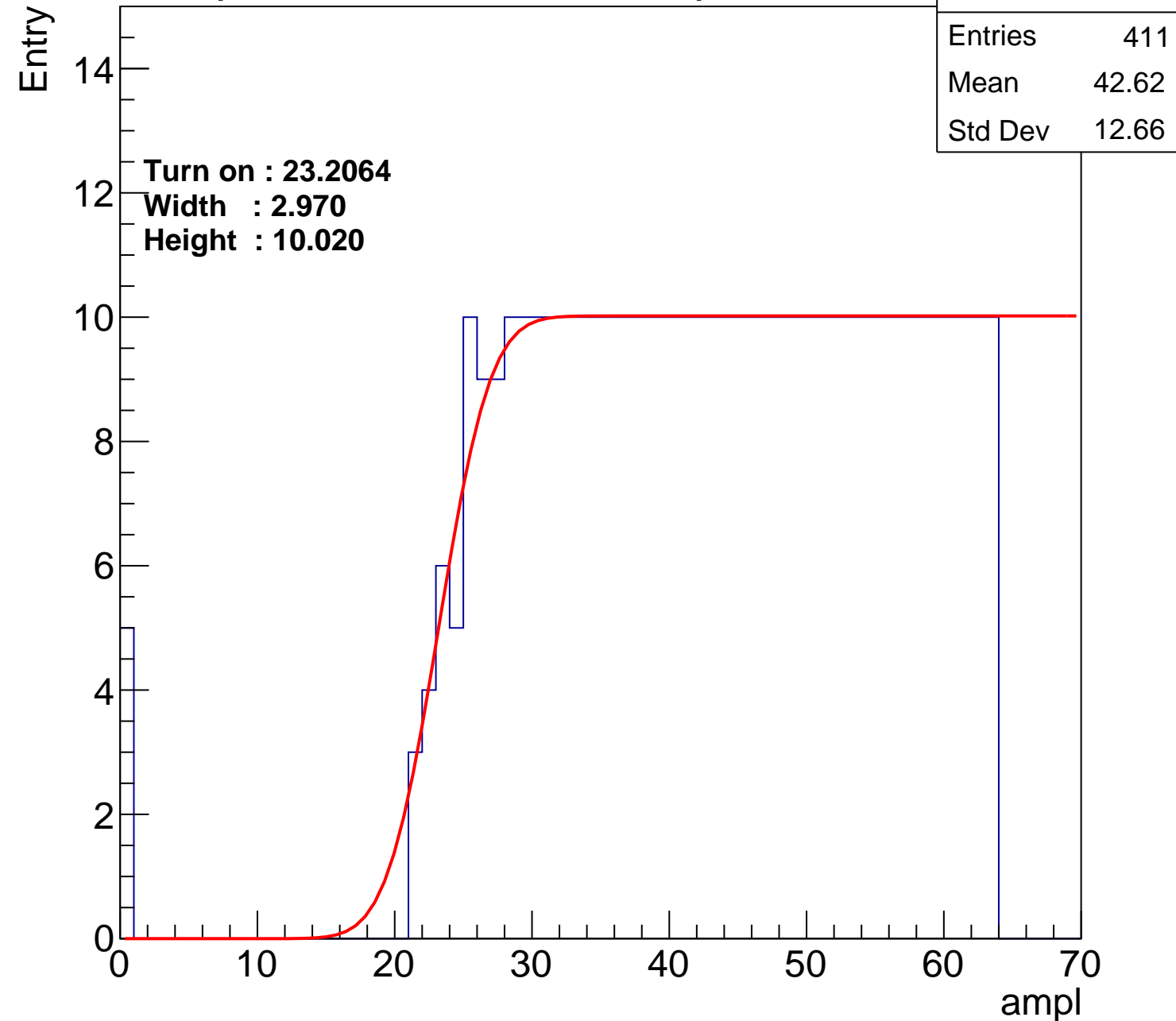
Width : 2.970

Height : 10.020

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch39

calib_packv5_042523_0143.root, FC#0, port D2

Entries	380
Mean	44.07
Std Dev	11.97

Turn on : 26.9324

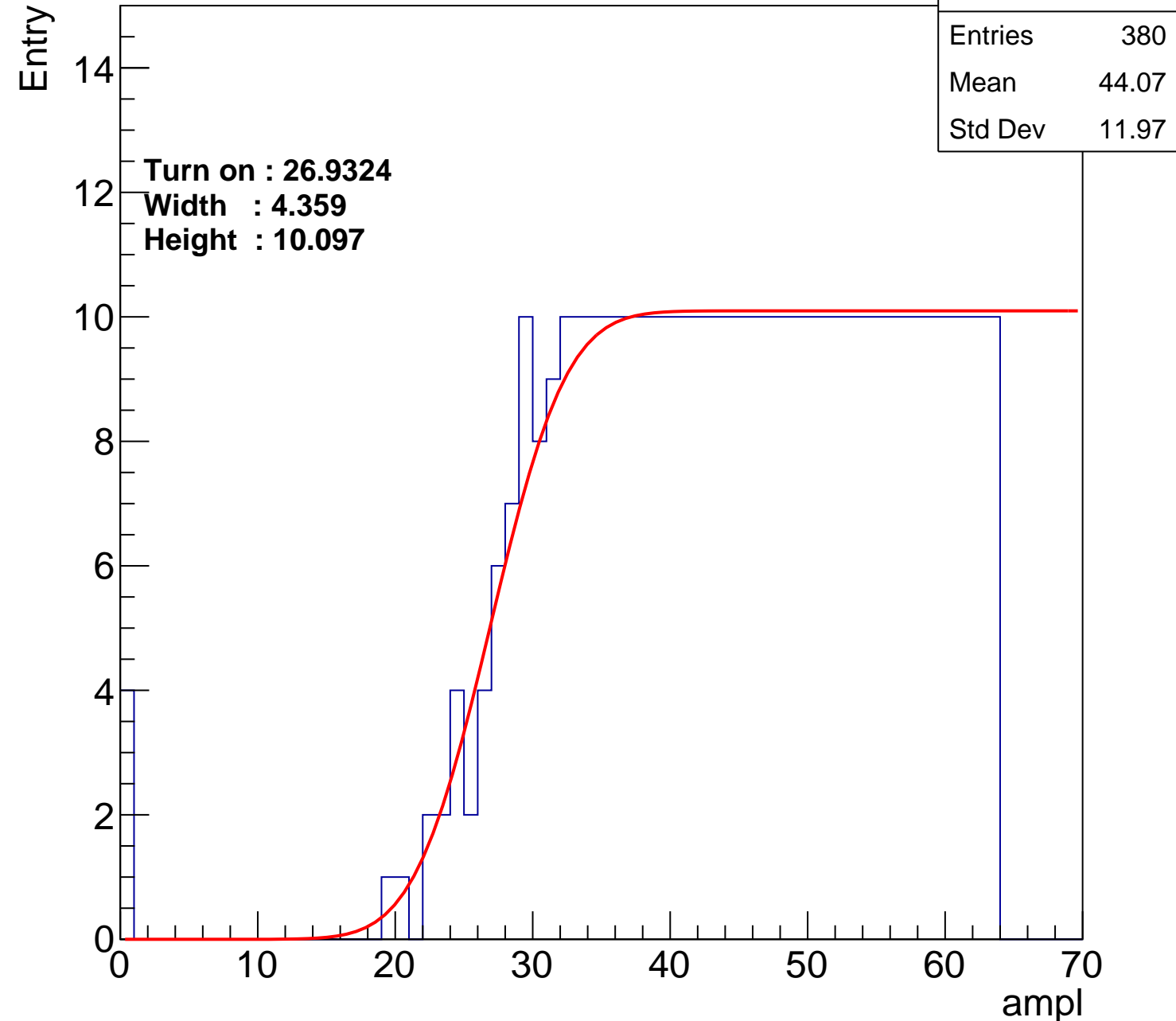
Width : 4.359

Height : 10.097

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch40

calib_packv5_042523_0143.root, FC#0, port D2

Entries	376
Mean	44.45
Std Dev	11.44

Turn on : 27.0681

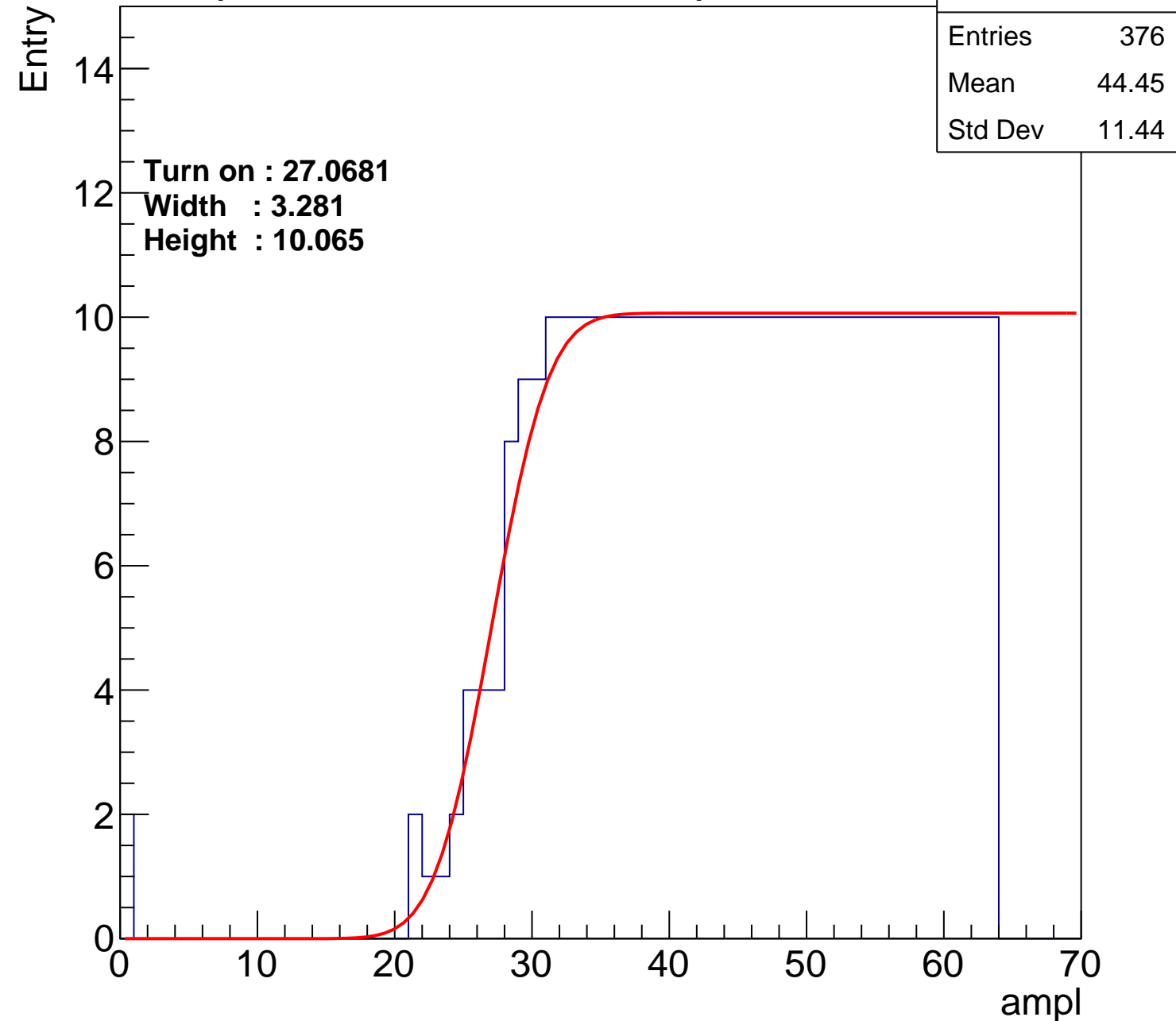
Width : 3.281

Height : 10.065

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch41

calib_packv5_042523_0143.root, FC#0, port D2

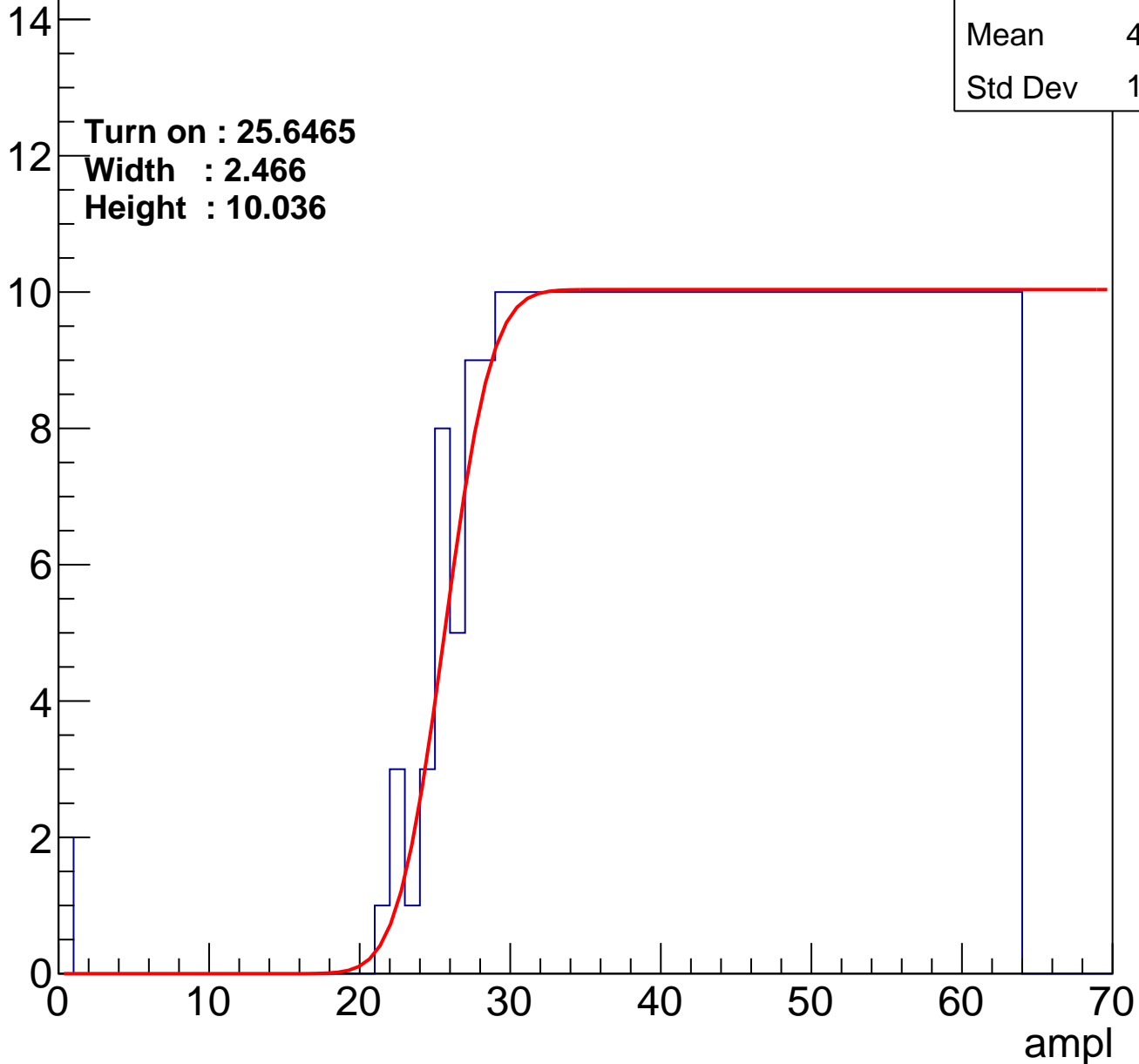
Entries	391
Mean	43.75
Std Dev	11.75

Turn on : 25.6465

Width : 2.466

Height : 10.036

Entry



B1L101S, U8-ch42

calib_packv5_042523_0143.root, FC#0, port D2

Entries	403
Mean	43.08
Std Dev	12.18

Turn on : 23.9905

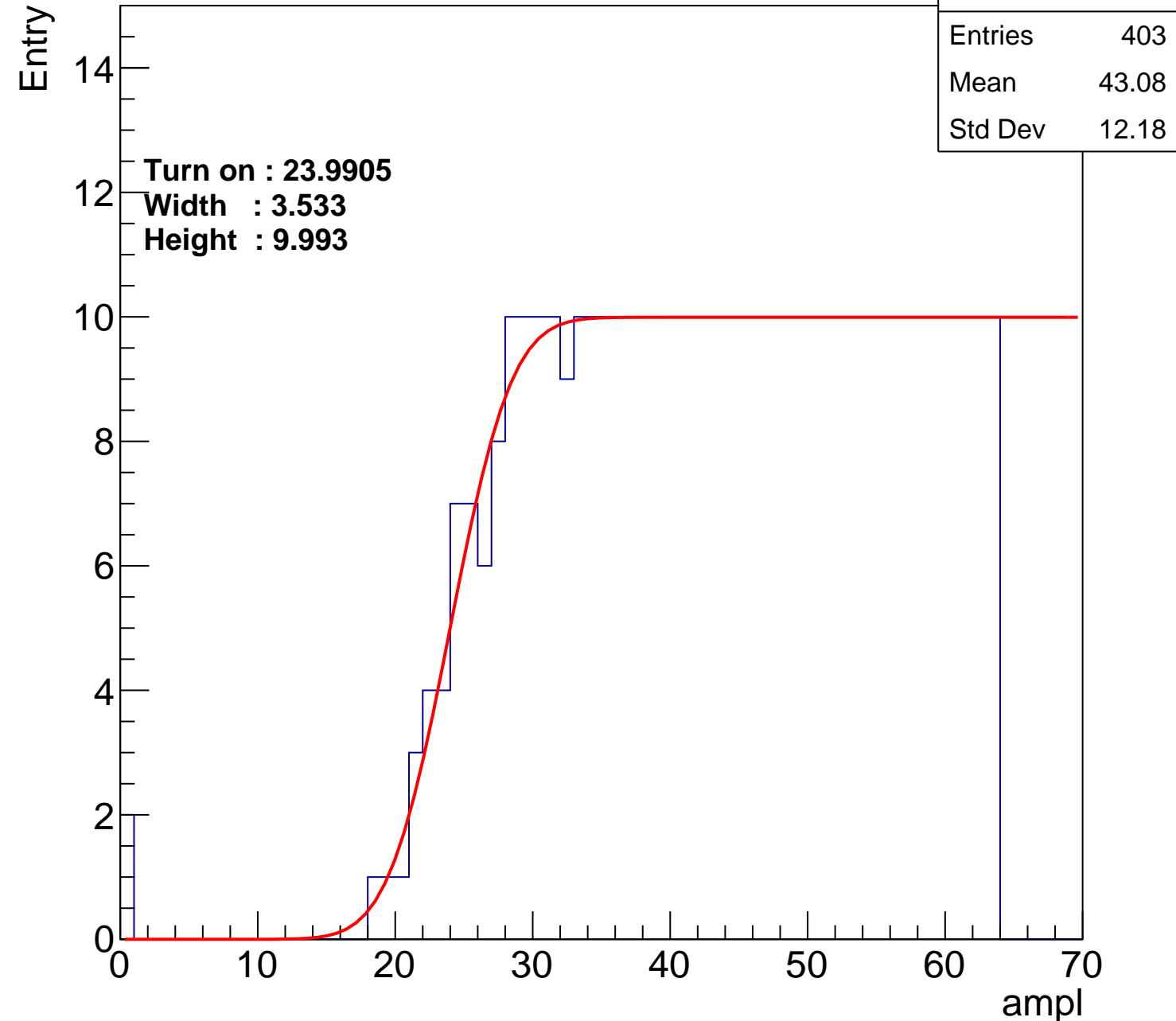
Width : 3.533

Height : 9.993

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch43

calib_packv5_042523_0143.root, FC#0, port D2

Entries	388
Mean	43.85
Std Dev	11.82

Turn on : 25.2646

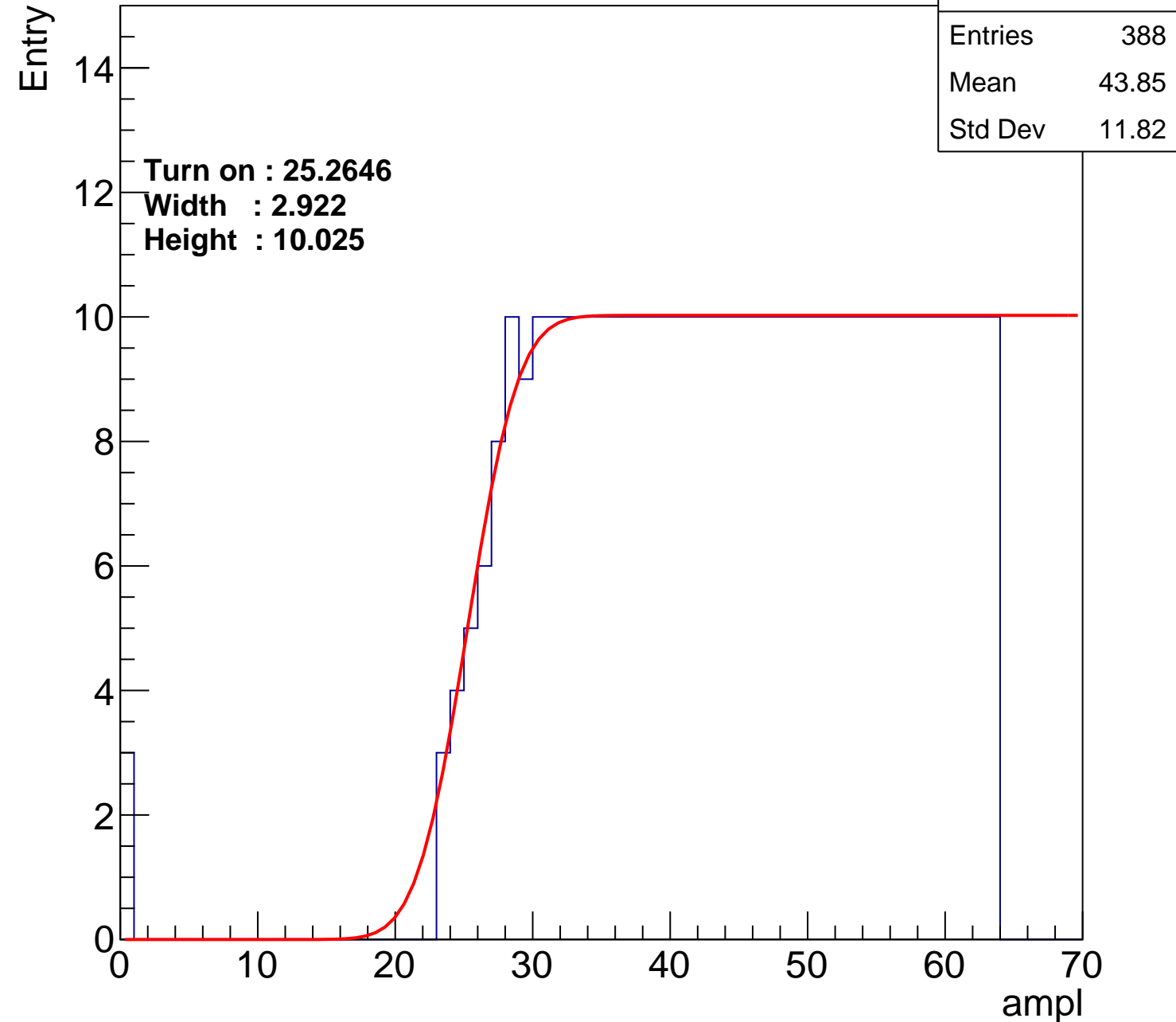
Width : 2.922

Height : 10.025

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch44

calib_packv5_042523_0143.root, FC#0, port D2

Entries	382
Mean	43.97
Std Dev	12.09

Turn on : 26.4951

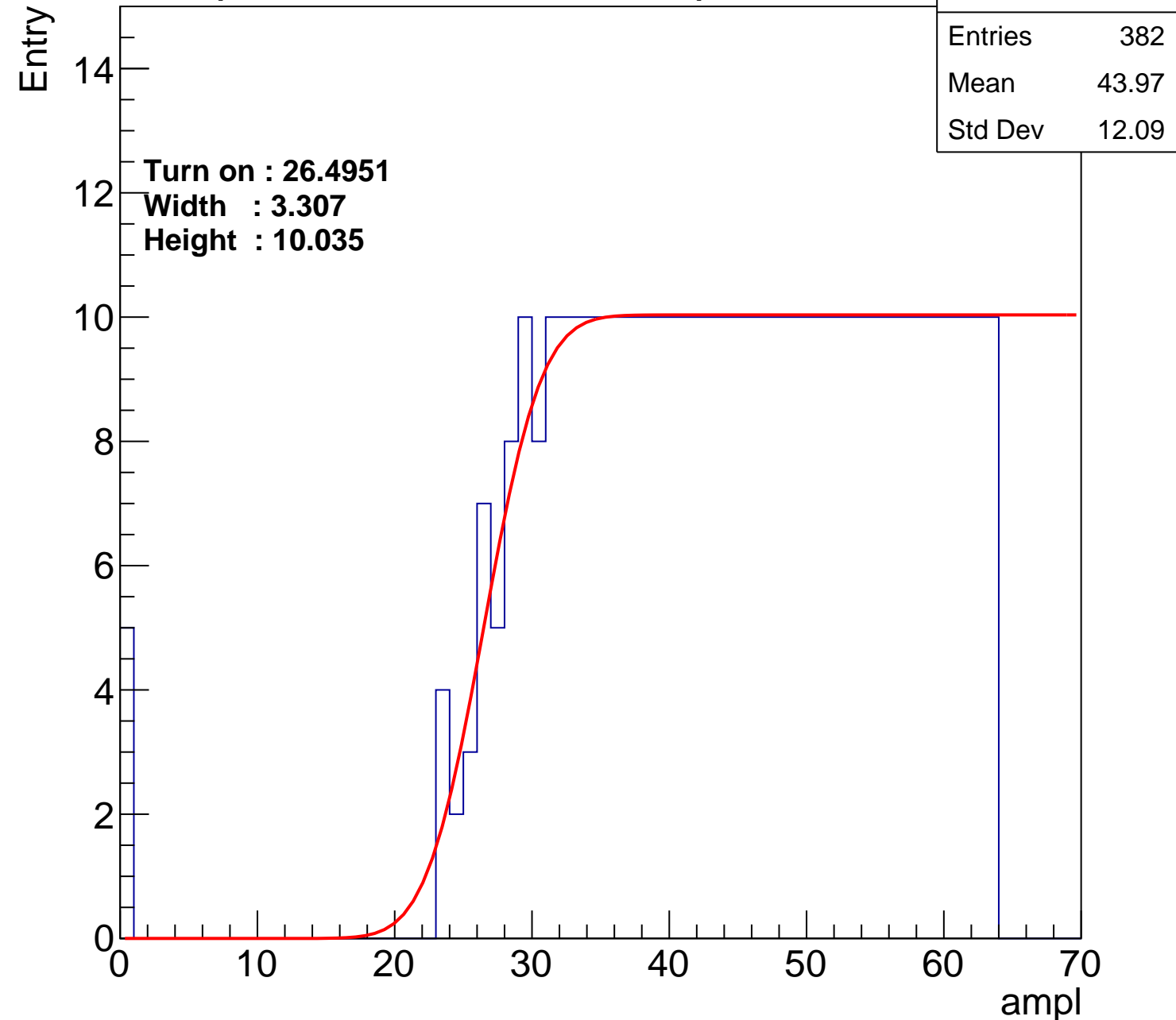
Width : 3.307

Height : 10.035

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch45

calib_packv5_042523_0143.root, FC#0, port D2

Entries	390
Mean	43.79
Std Dev	11.67

Turn on : 25.4482

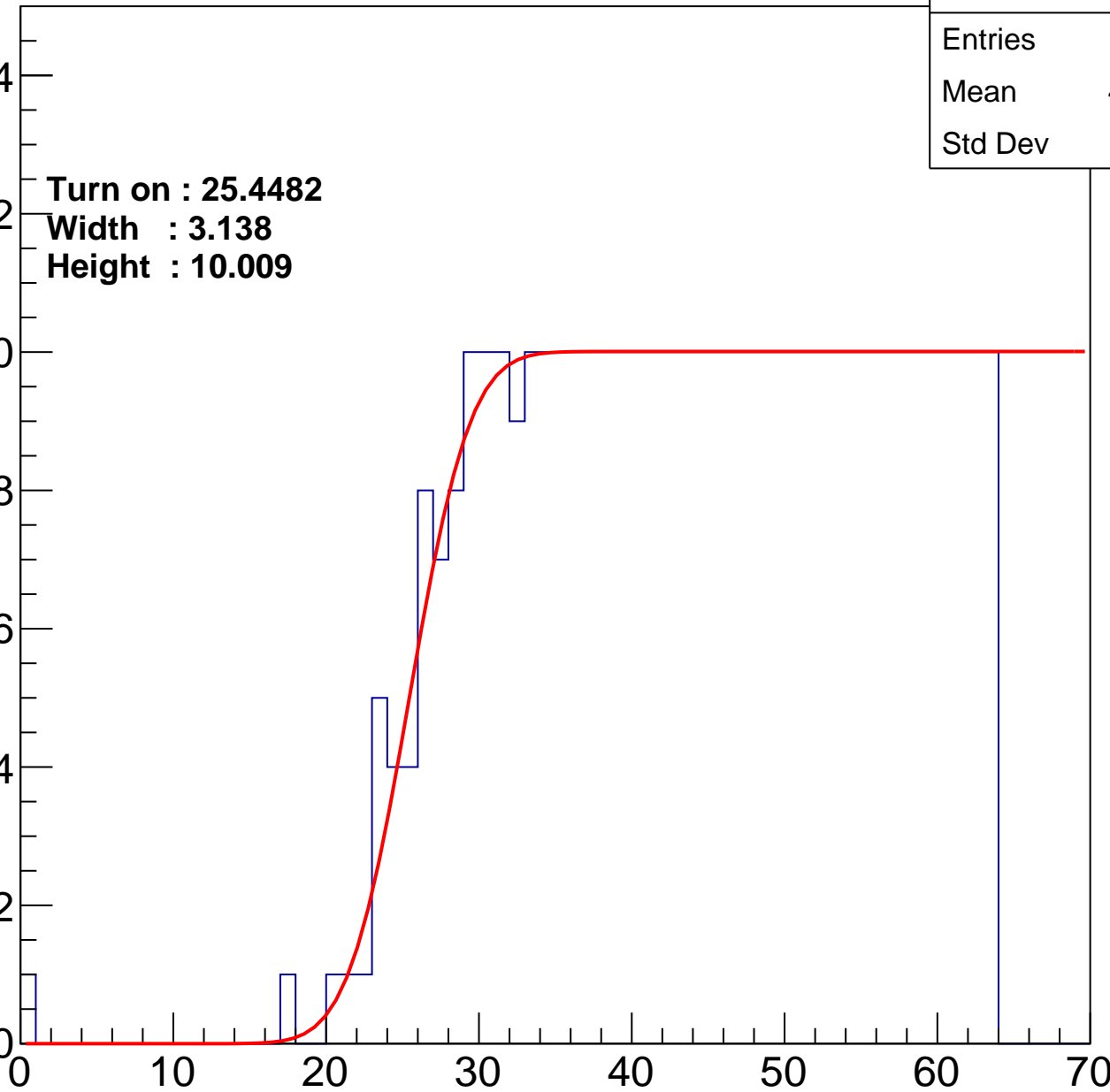
Width : 3.138

Height : 10.009

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch46

calib_packv5_042523_0143.root, FC#0, port D2

Entries	366
Mean	44.86
Std Dev	11.39

Turn on : 28.6779

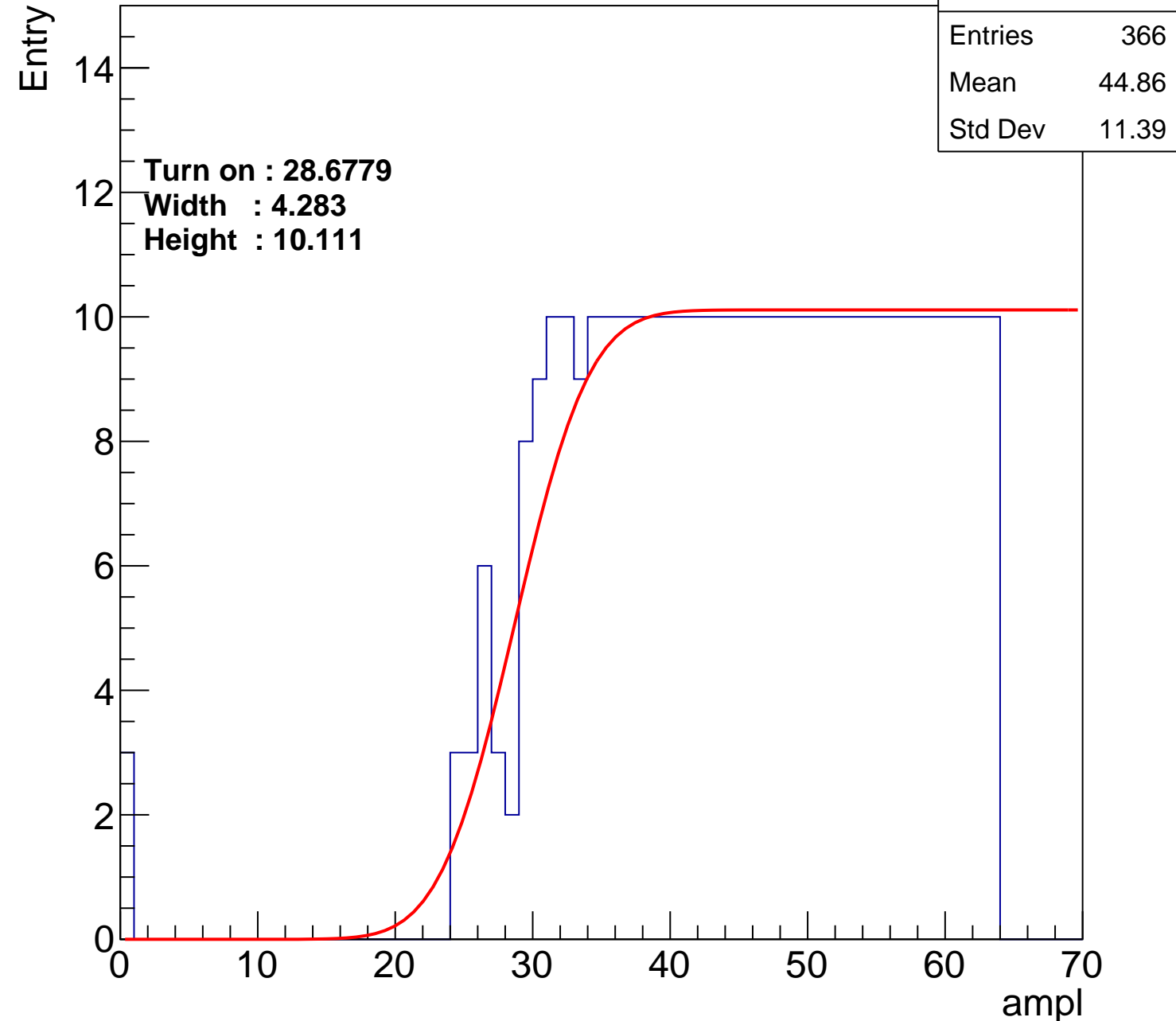
Width : 4.283

Height : 10.111

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch47

calib_packv5_042523_0143.root, FC#0, port D2

Entries	375
Mean	44.37
Std Dev	11.76

Turn on : 27.7731

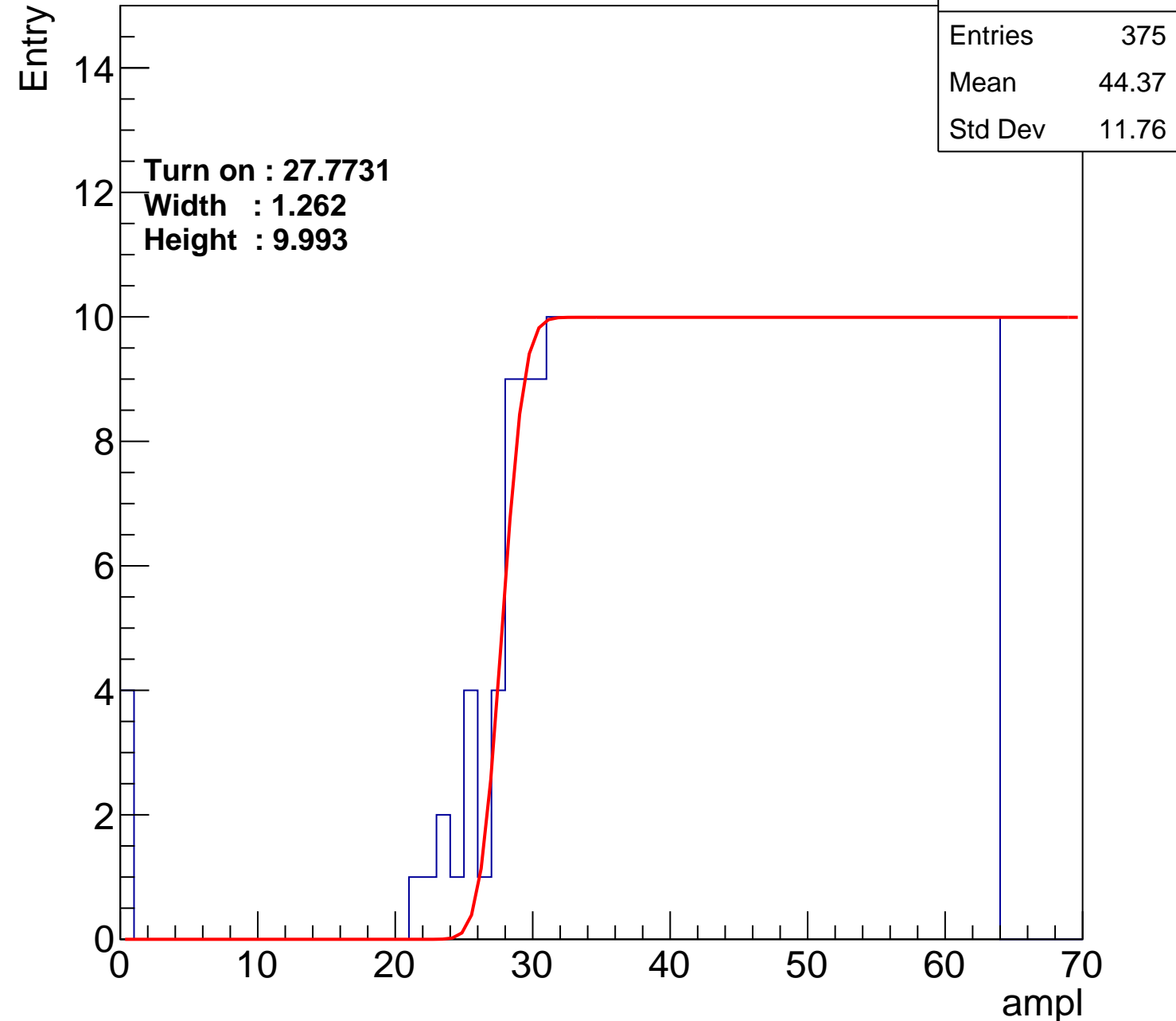
Width : 1.262

Height : 9.993

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch48

calib_packv5_042523_0143.root, FC#0, port D2

Entries	374
Mean	44.6
Std Dev	11.21

Turn on : 26.9282

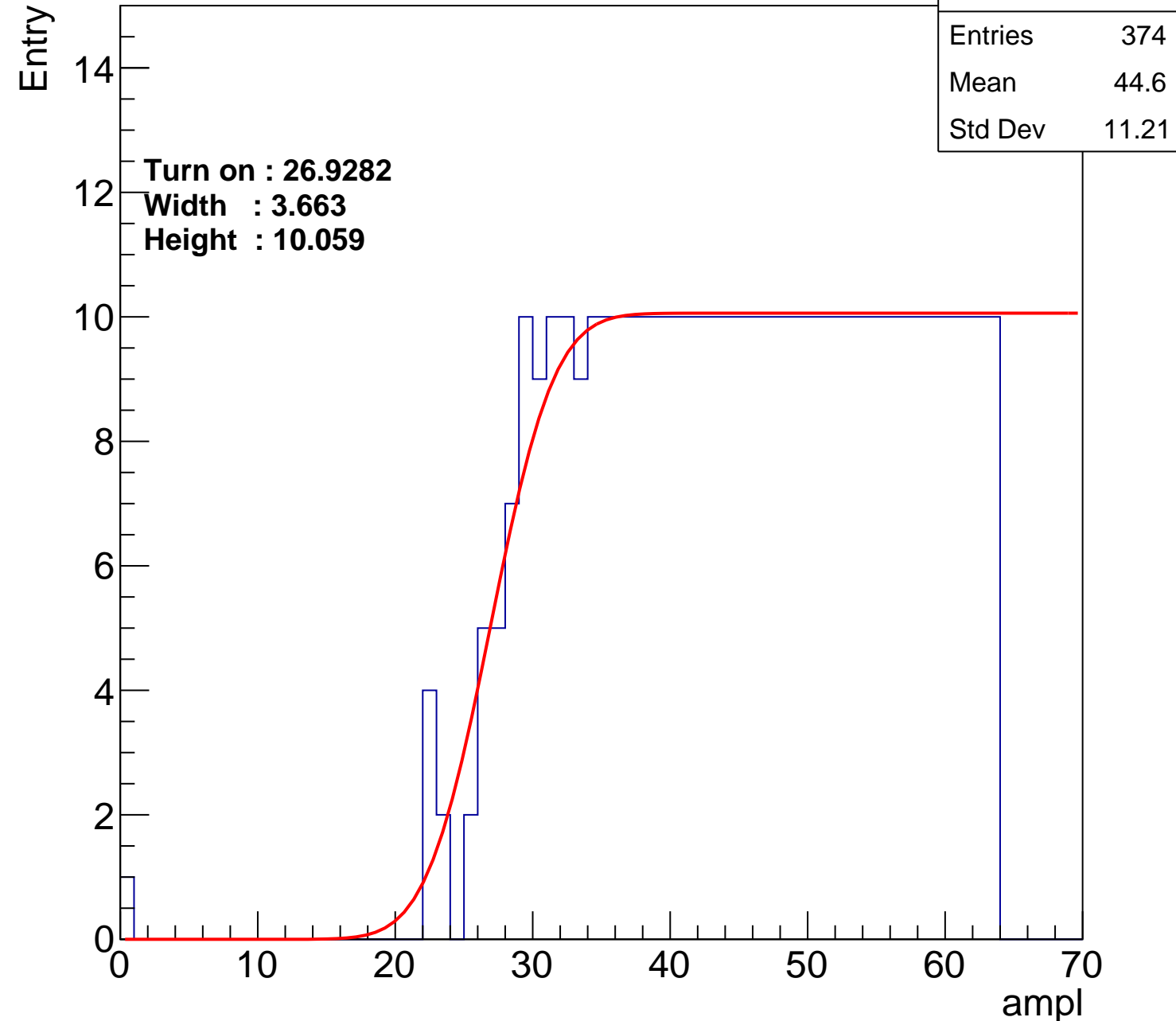
Width : 3.663

Height : 10.059

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch49

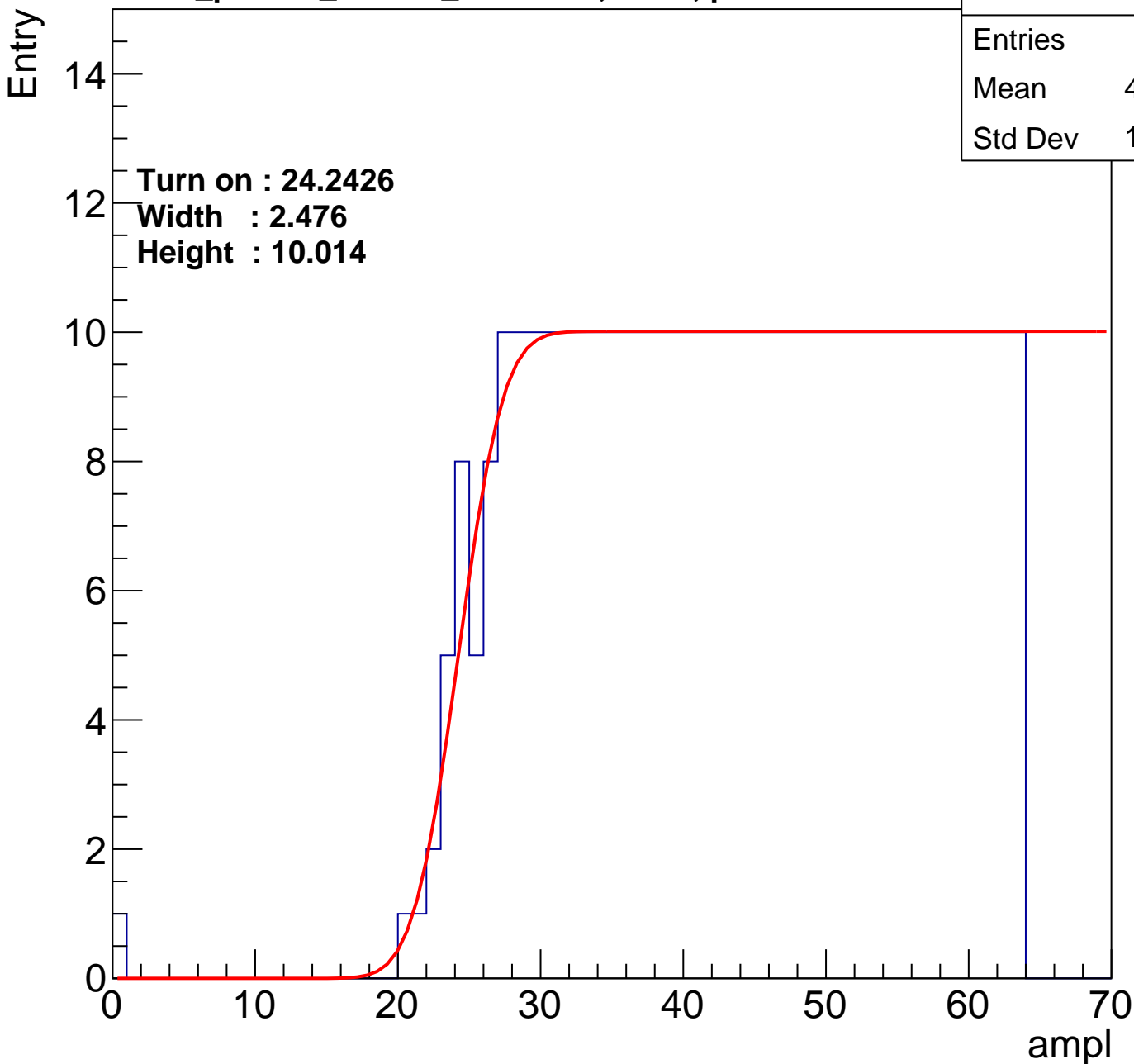
calib_packv5_042523_0143.root, FC#0, port D2

Entries	401
Mean	43.33
Std Dev	11.84

Turn on : 24.2426

Width : 2.476

Height : 10.014



B1L101S, U8-ch50

calib_packv5_042523_0143.root, FC#0, port D2

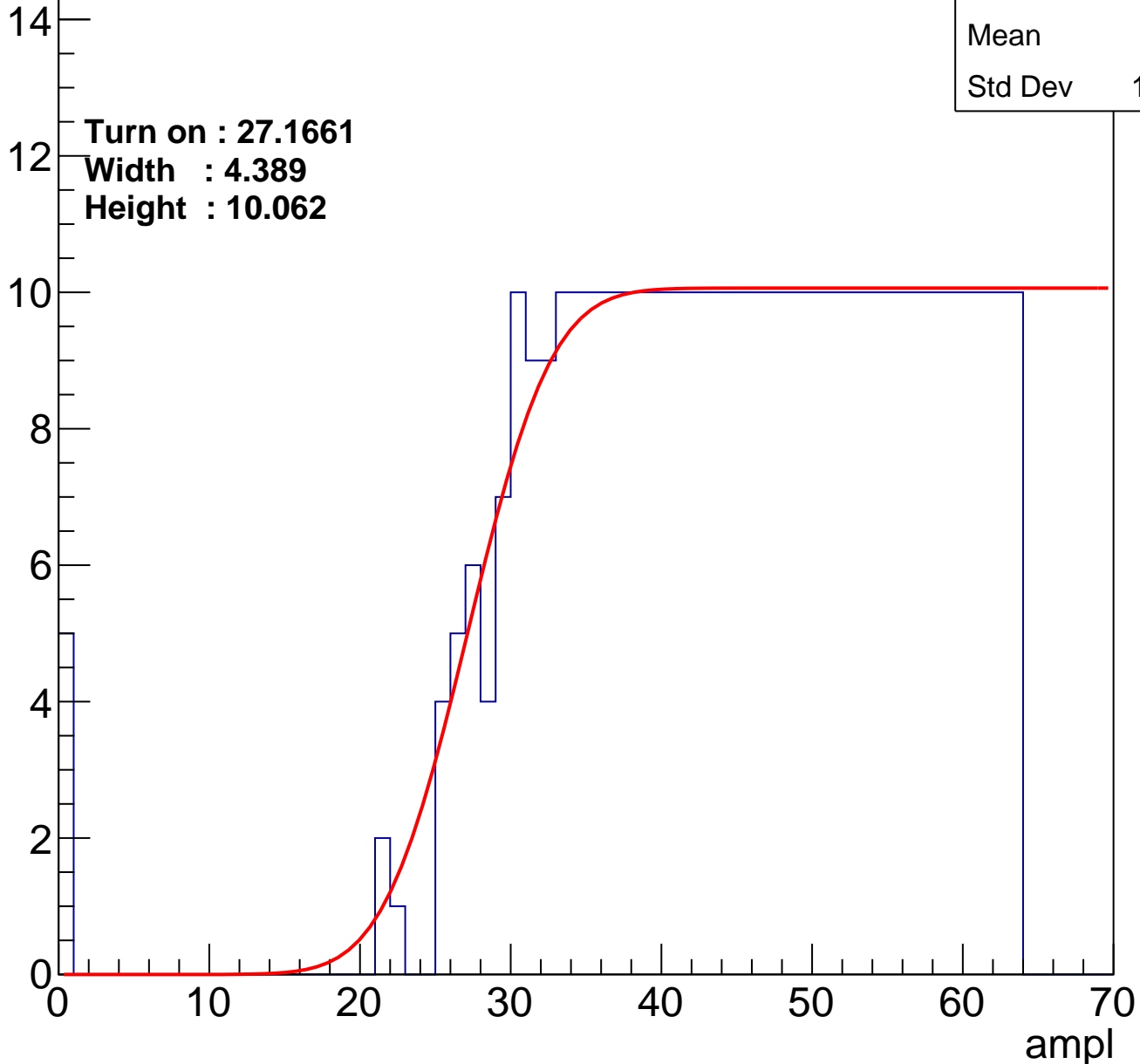
Entries	372
Mean	44.4
Std Dev	11.95

Turn on : 27.1661

Width : 4.389

Height : 10.062

Entry



B1L101S, U8-ch51

calib_packv5_042523_0143.root, FC#0, port D2

Entries	348
Mean	45.66
Std Dev	11.19

Turn on : 29.7949

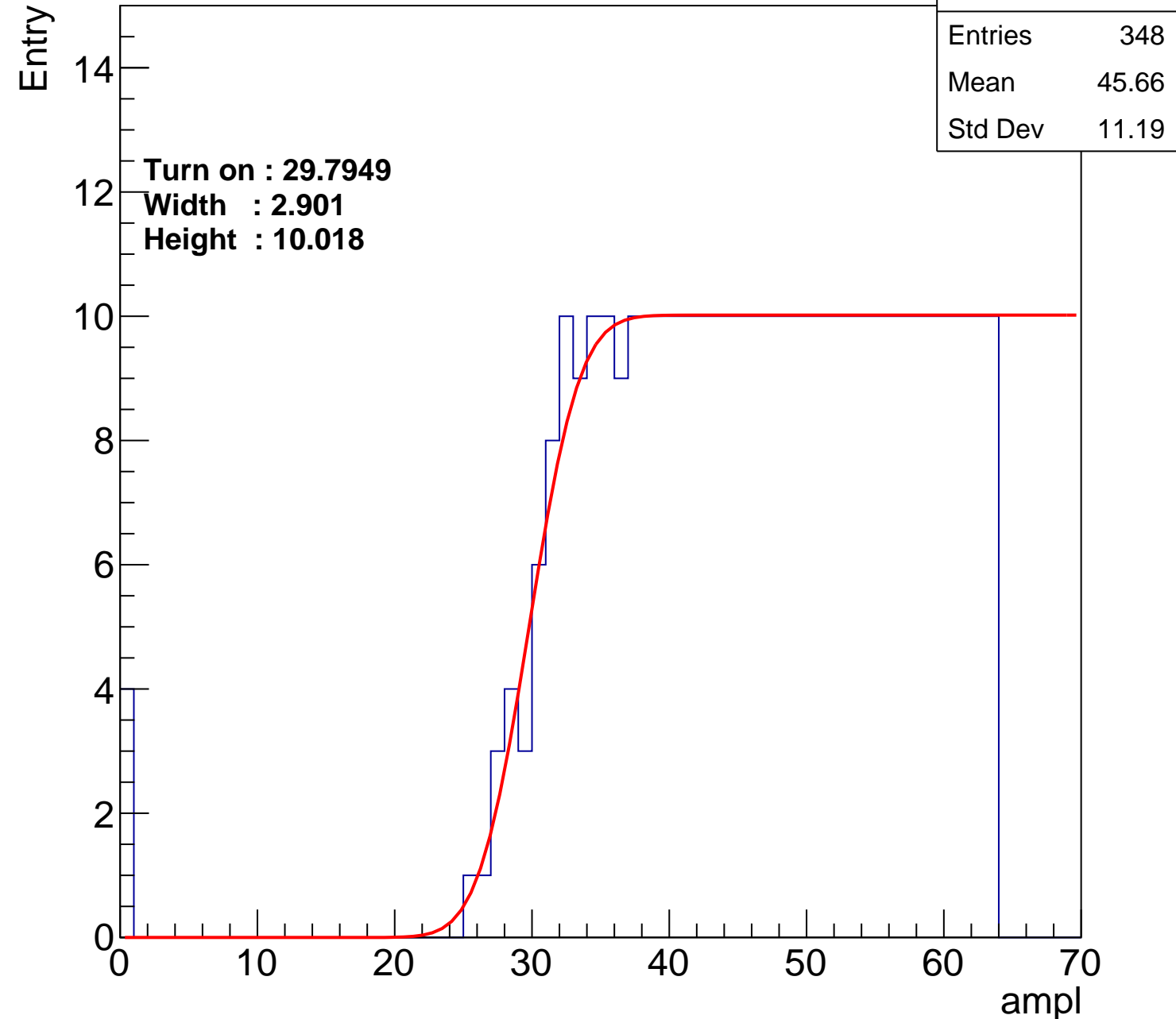
Width : 2.901

Height : 10.018

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch52

calib_packv5_042523_0143.root, FC#0, port D2

Entries	375
Mean	44.22
Std Dev	12.06

Turn on : 27.2126

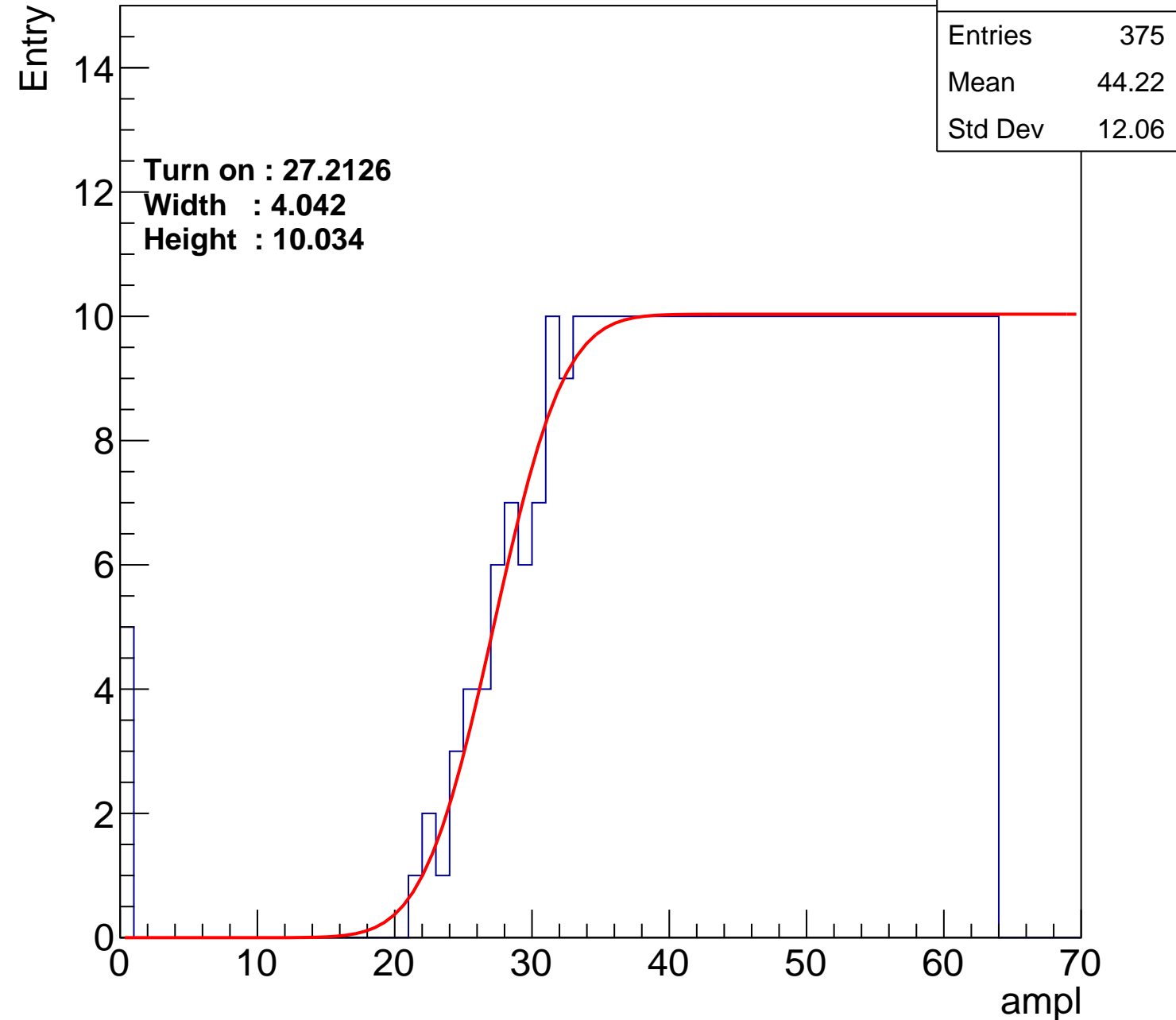
Width : 4.042

Height : 10.034

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch53

calib_packv5_042523_0143.root, FC#0, port D2

Entries	374
Mean	44.62
Std Dev	11.18

Turn on : 26.7705

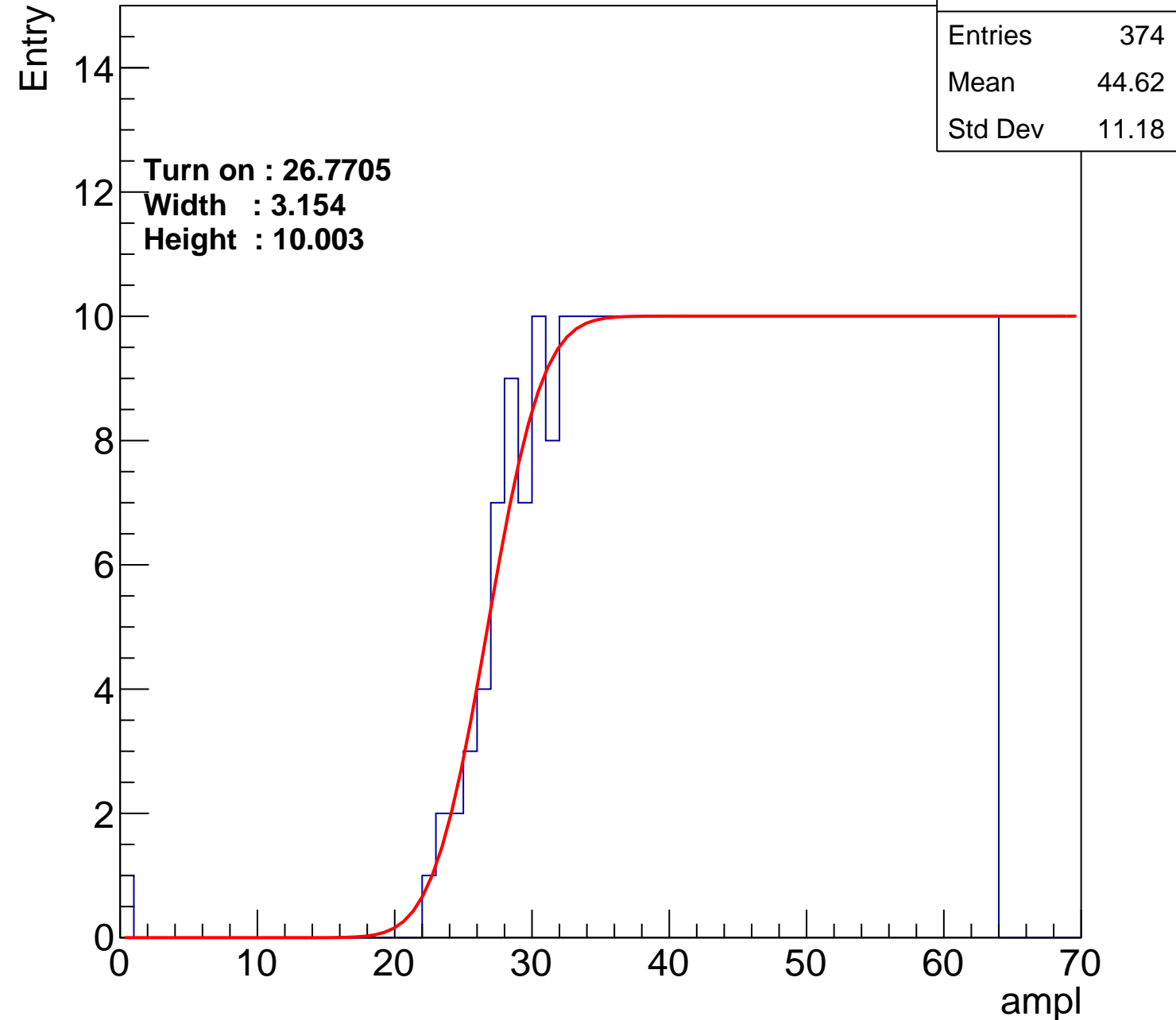
Width : 3.154

Height : 10.003

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch54

calib_packv5_042523_0143.root, FC#0, port D2

Entries	377
Mean	43.92
Std Dev	12.69

Turn on : 27.4174

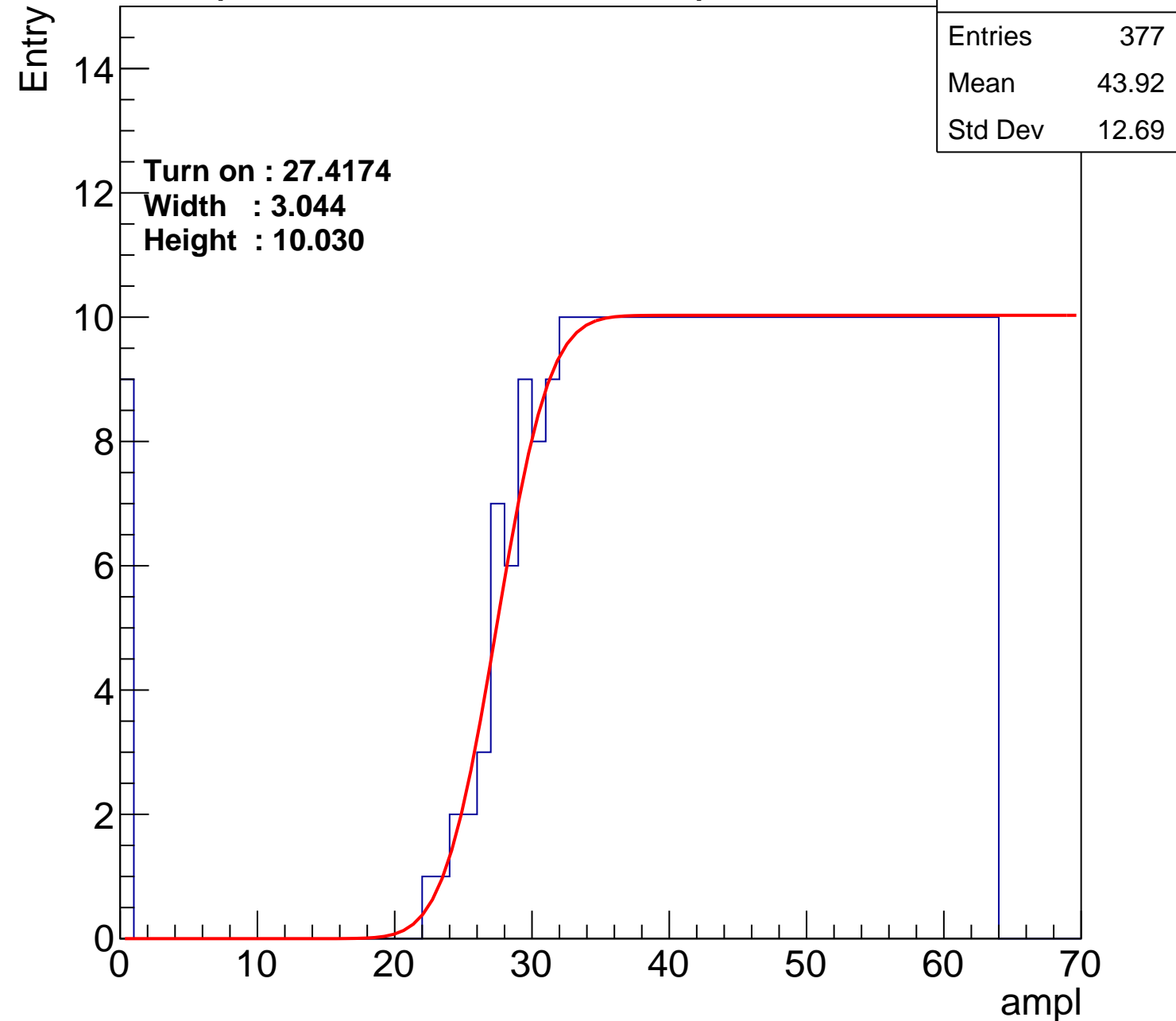
Width : 3.044

Height : 10.030

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch55

calib_packv5_042523_0143.root, FC#0, port D2

Entries	361
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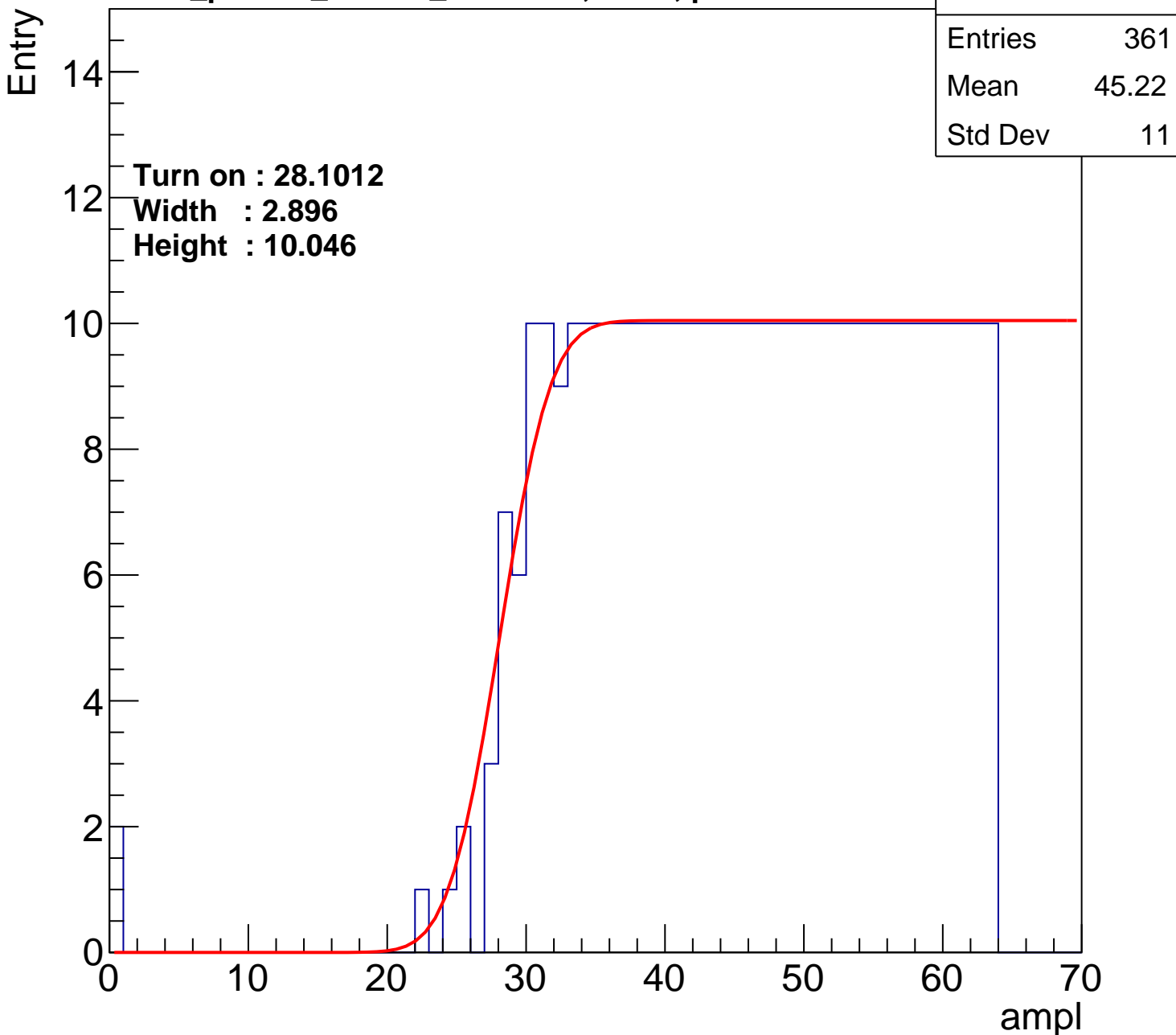
Mean	45.22
------	-------

Std Dev	11
---------	----

Turn on : 28.1012

Width : 2.896

Height : 10.046



B1L101S, U8-ch56

calib_packv5_042523_0143.root, FC#0, port D2

Entries	387
Mean	43.74
Std Dev	12.18

Turn on : 26.3319

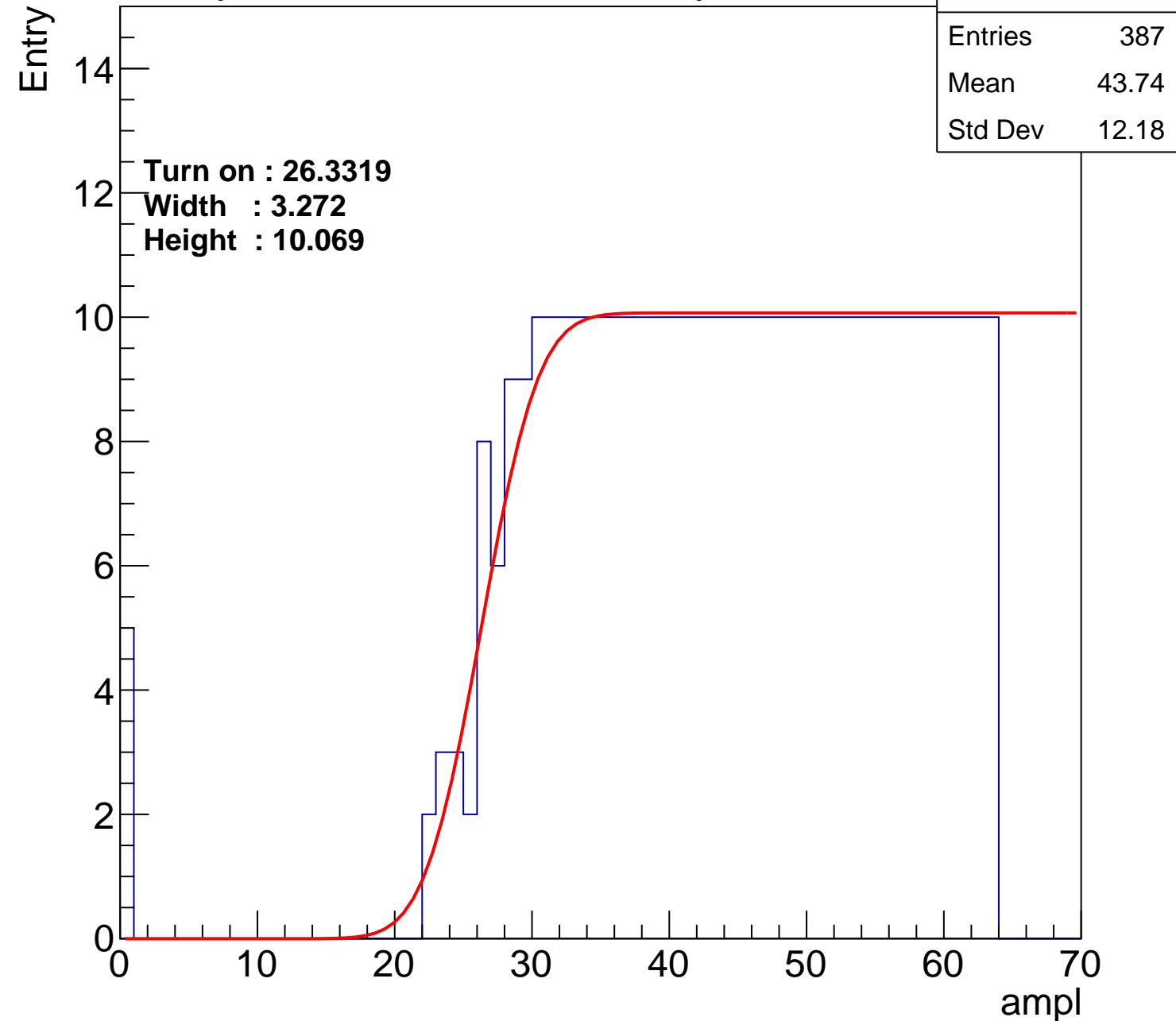
Width : 3.272

Height : 10.069

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch57

calib_packv5_042523_0143.root, FC#0, port D2

Entries	360
Mean	45.19
Std Dev	11.18

Turn on : 28.1825

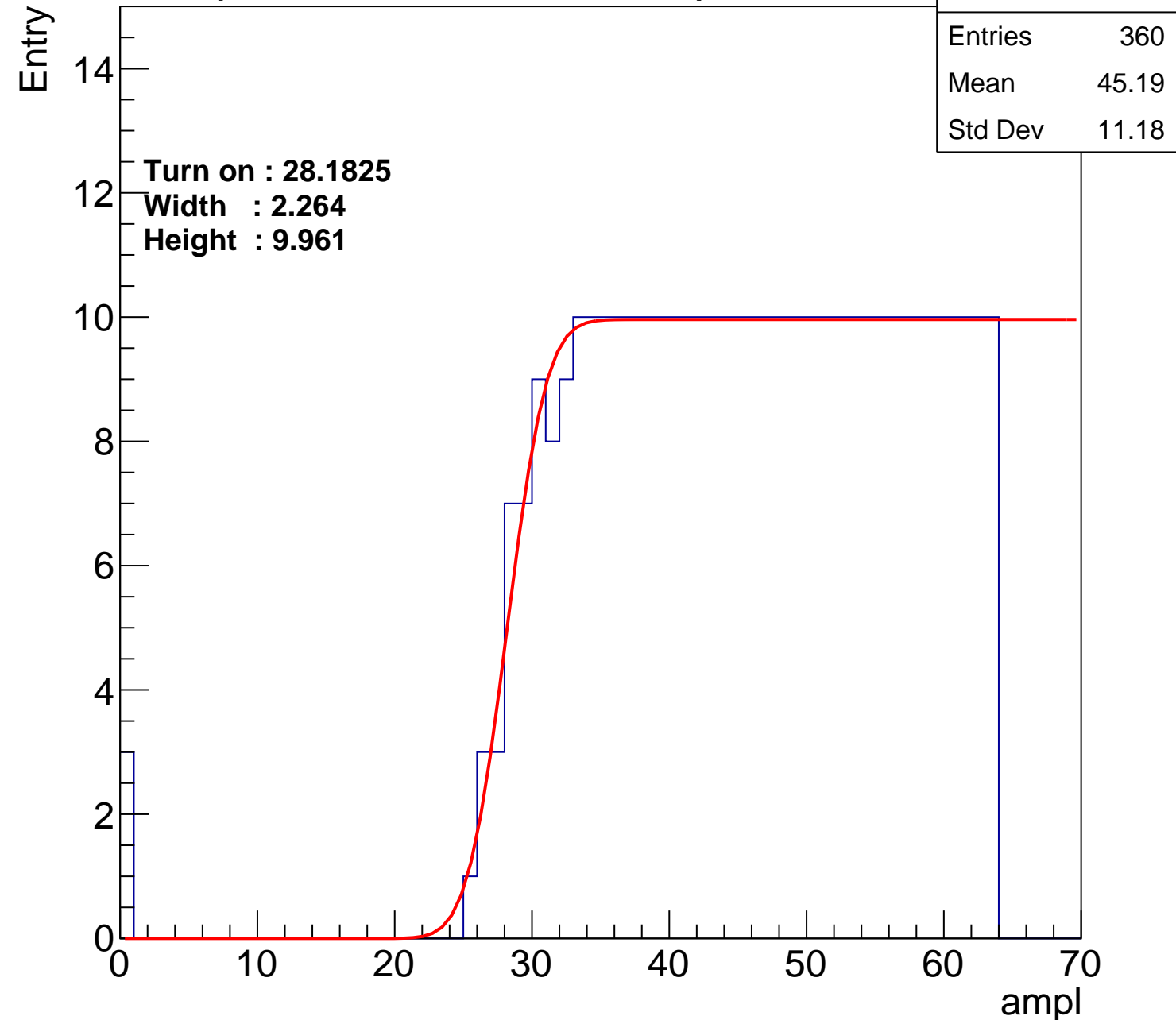
Width : 2.264

Height : 9.961

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch58

calib_packv5_042523_0143.root, FC#0, port D2

Entries	388
Mean	43.73
Std Dev	12.07

Turn on : 25.7943

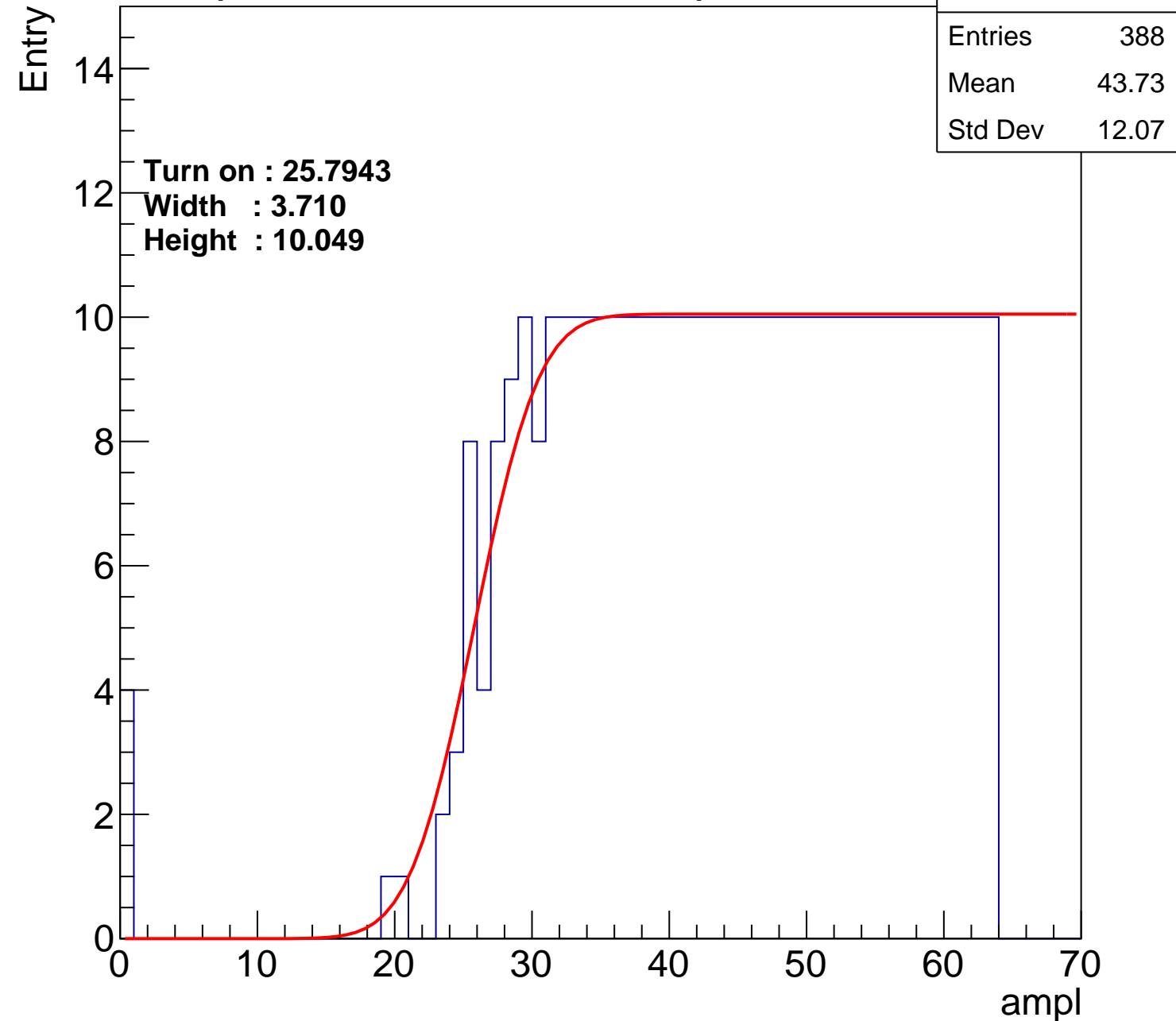
Width : 3.710

Height : 10.049

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch59

calib_packv5_042523_0143.root, FC#0, port D2

Entries	372
Mean	44.64
Std Dev	11.34

Turn on : 27.1033

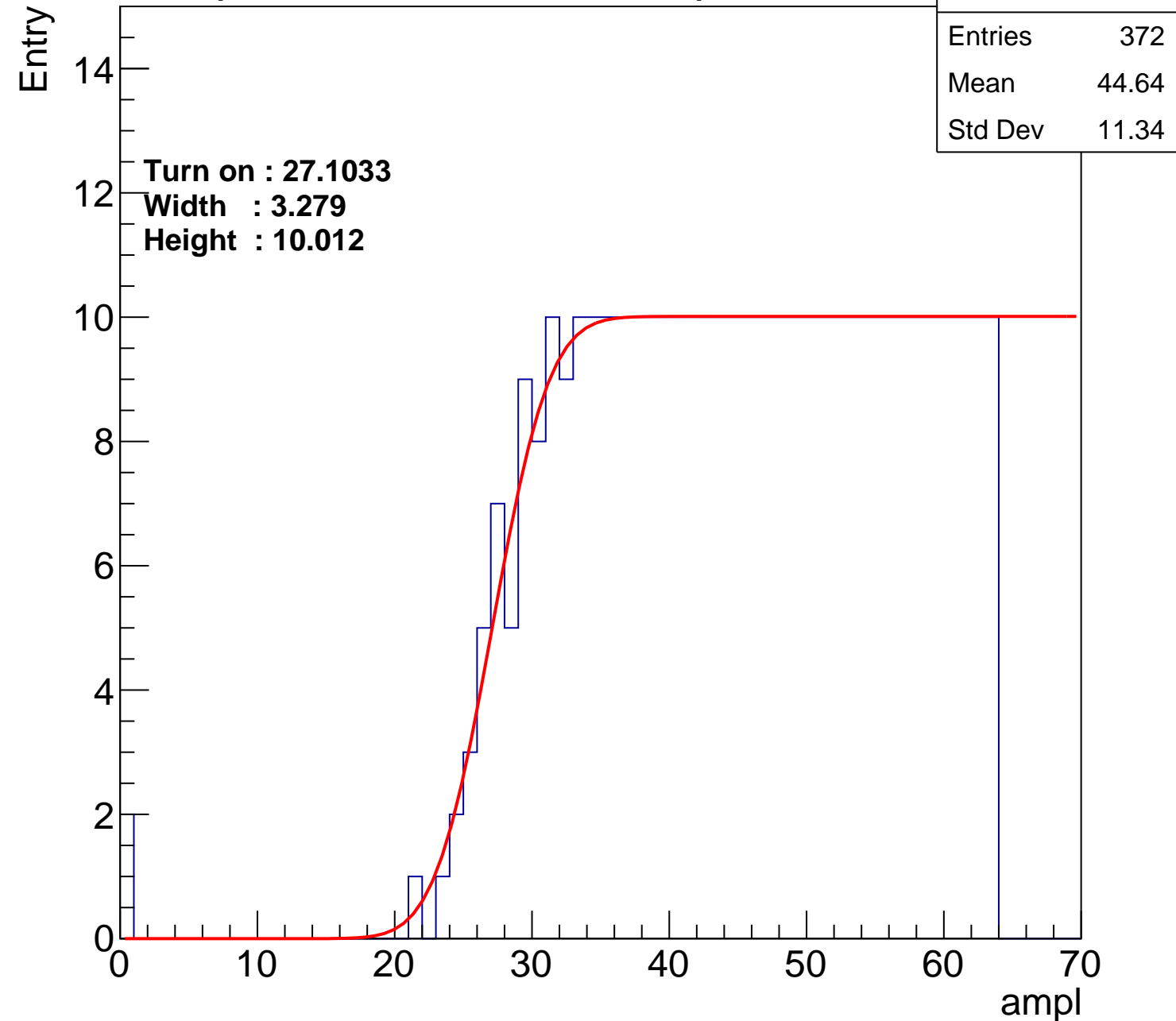
Width : 3.279

Height : 10.012

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch60

calib_packv5_042523_0143.root, FC#0, port D2

Entries	387
Mean	43.83
Std Dev	11.98

Turn on : 25.6960

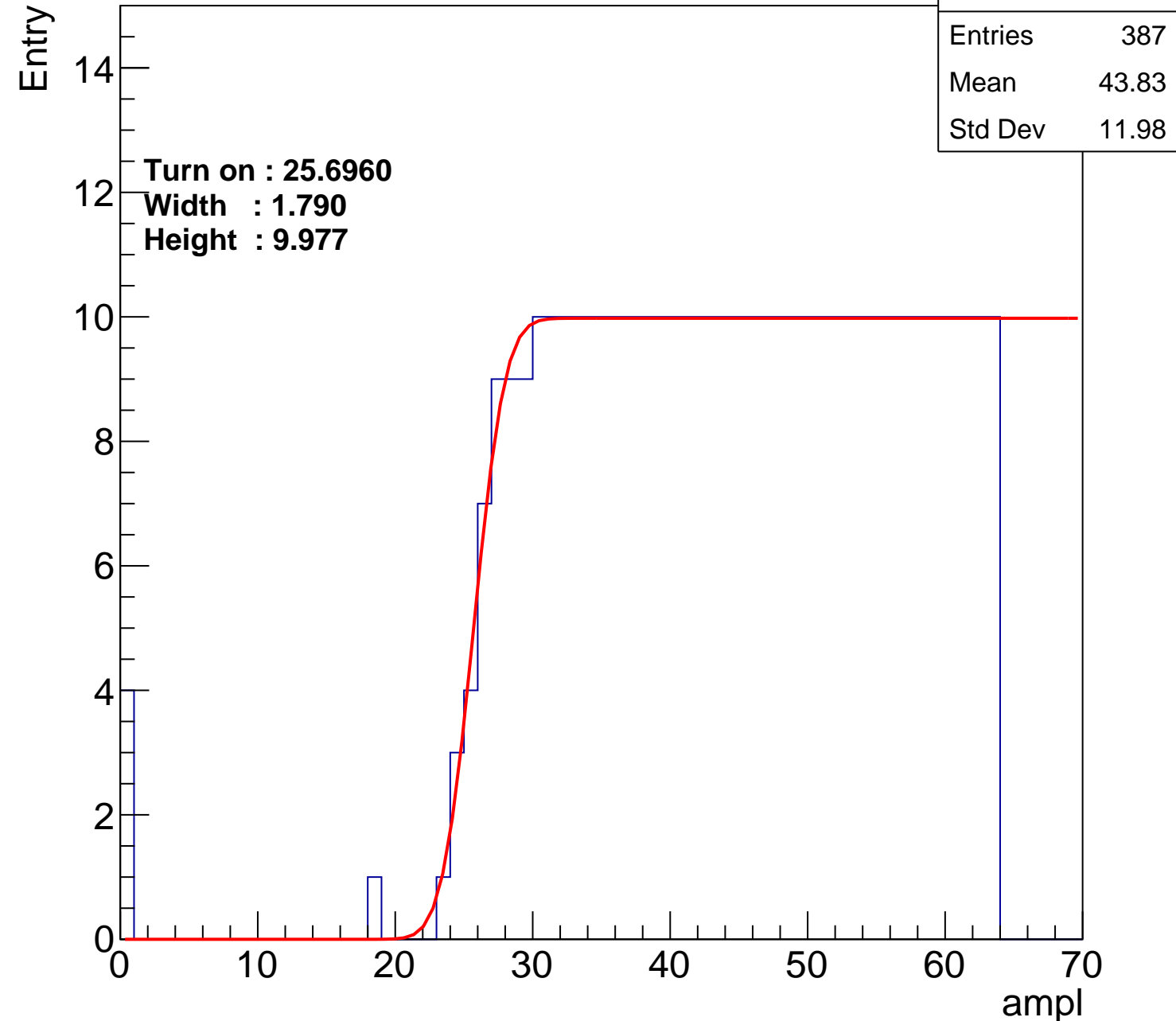
Width : 1.790

Height : 9.977

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch61

calib_packv5_042523_0143.root, FC#0, port D2

Entries	381
Mean	44.26
Std Dev	11.47

Turn on : 26.4189

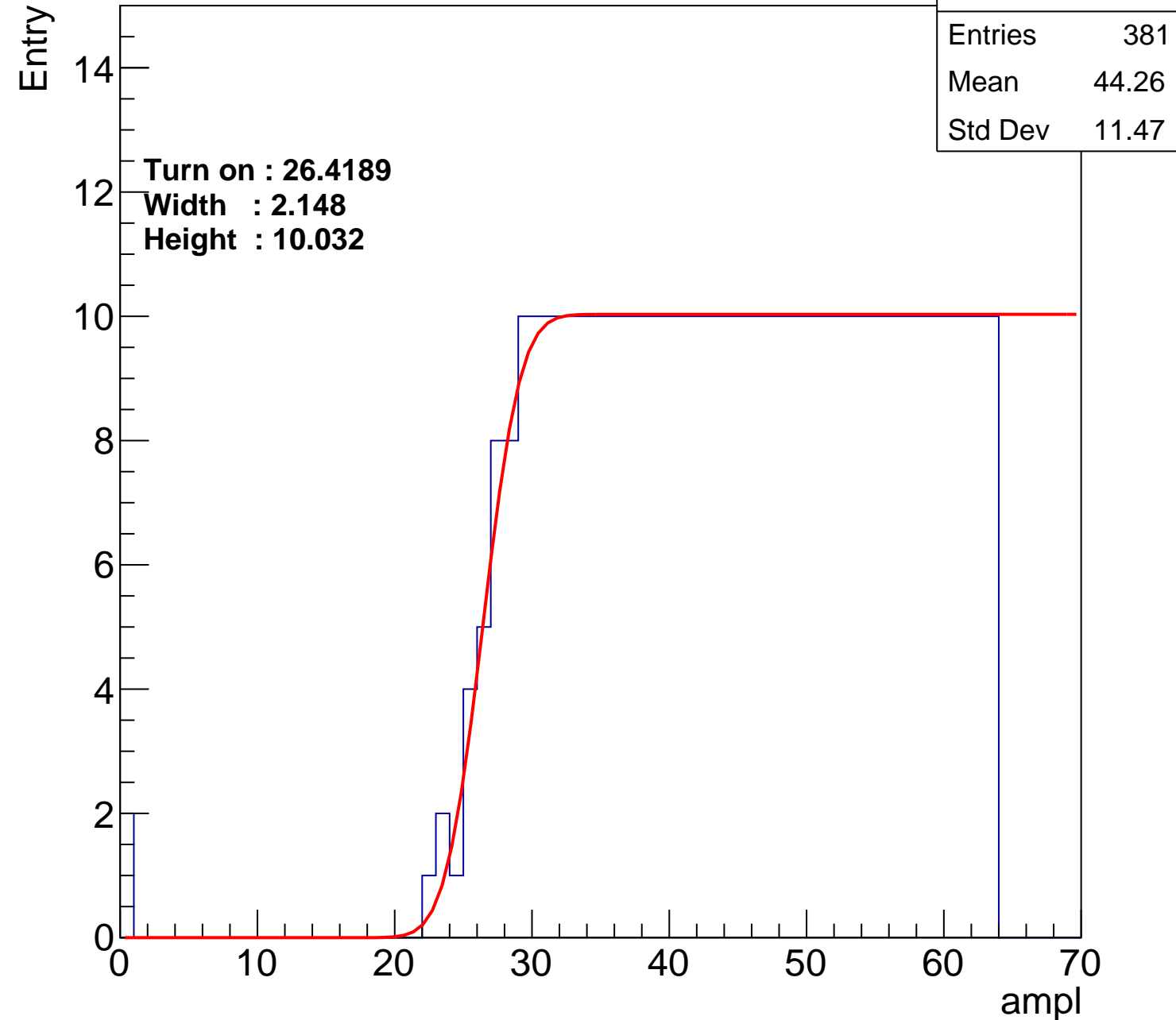
Width : 2.148

Height : 10.032

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch62

calib_packv5_042523_0143.root, FC#0, port D2

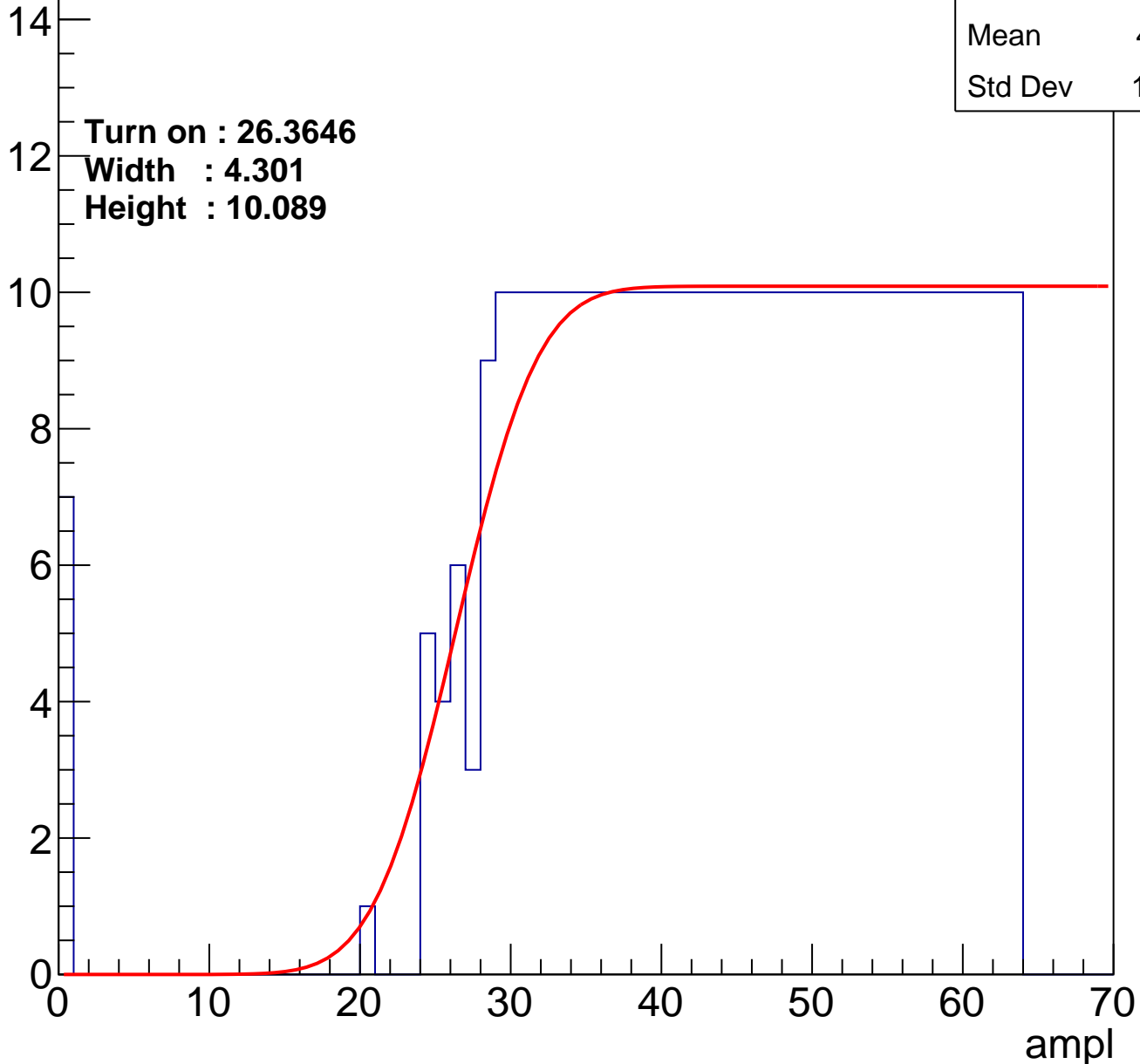
Entries	385
Mean	43.71
Std Dev	12.46

Turn on : 26.3646

Width : 4.301

Height : 10.089

Entry



B1L101S, U8-ch63

calib_packv5_042523_0143.root, FC#0, port D2

Entries	392
Mean	43.65
Std Dev	11.87

Turn on : 26.0191

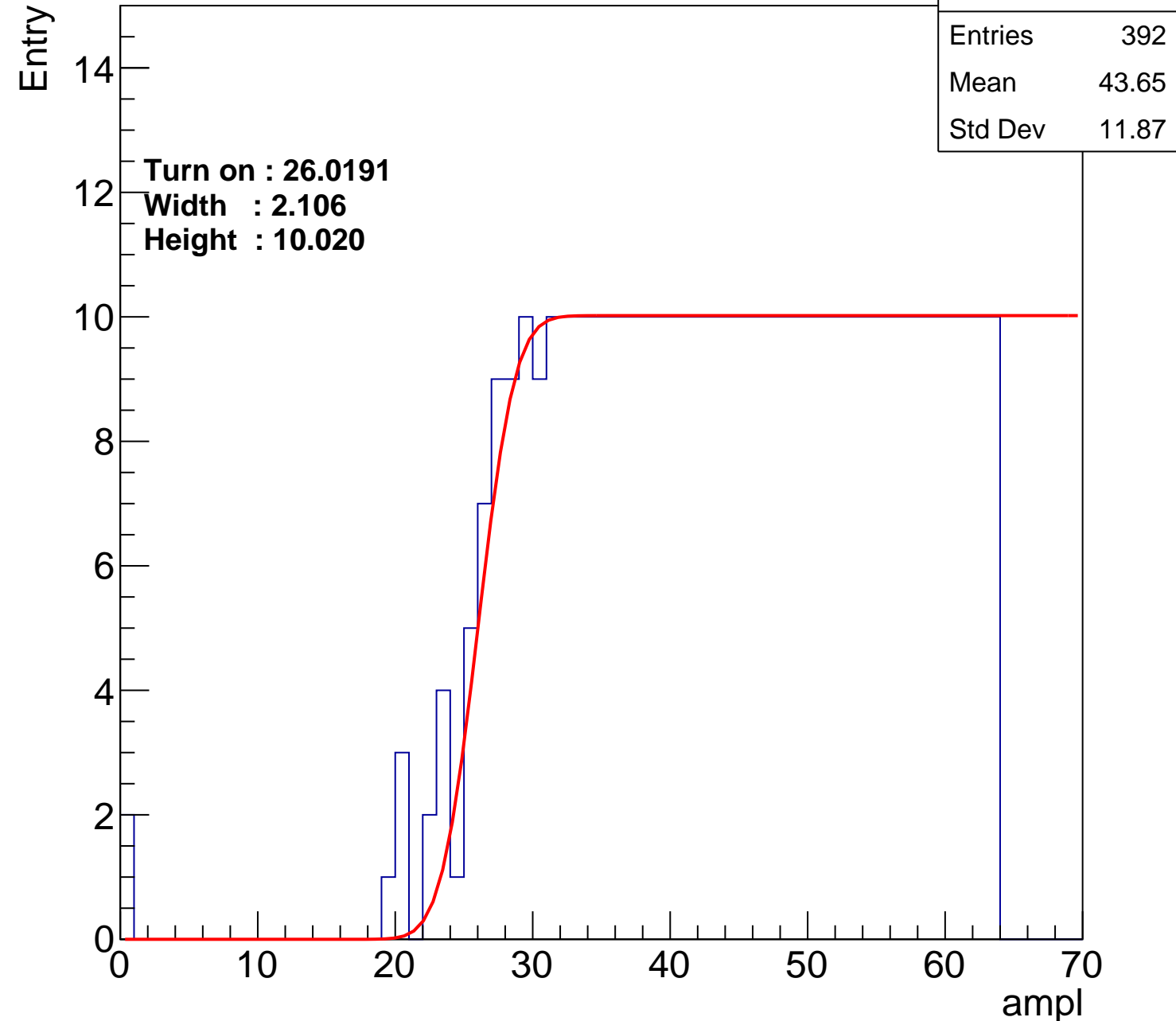
Width : 2.106

Height : 10.020

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch64

calib_packv5_042523_0143.root, FC#0, port D2

Entries	376
Mean	44.58
Std Dev	11.14

Turn on : 26.4425

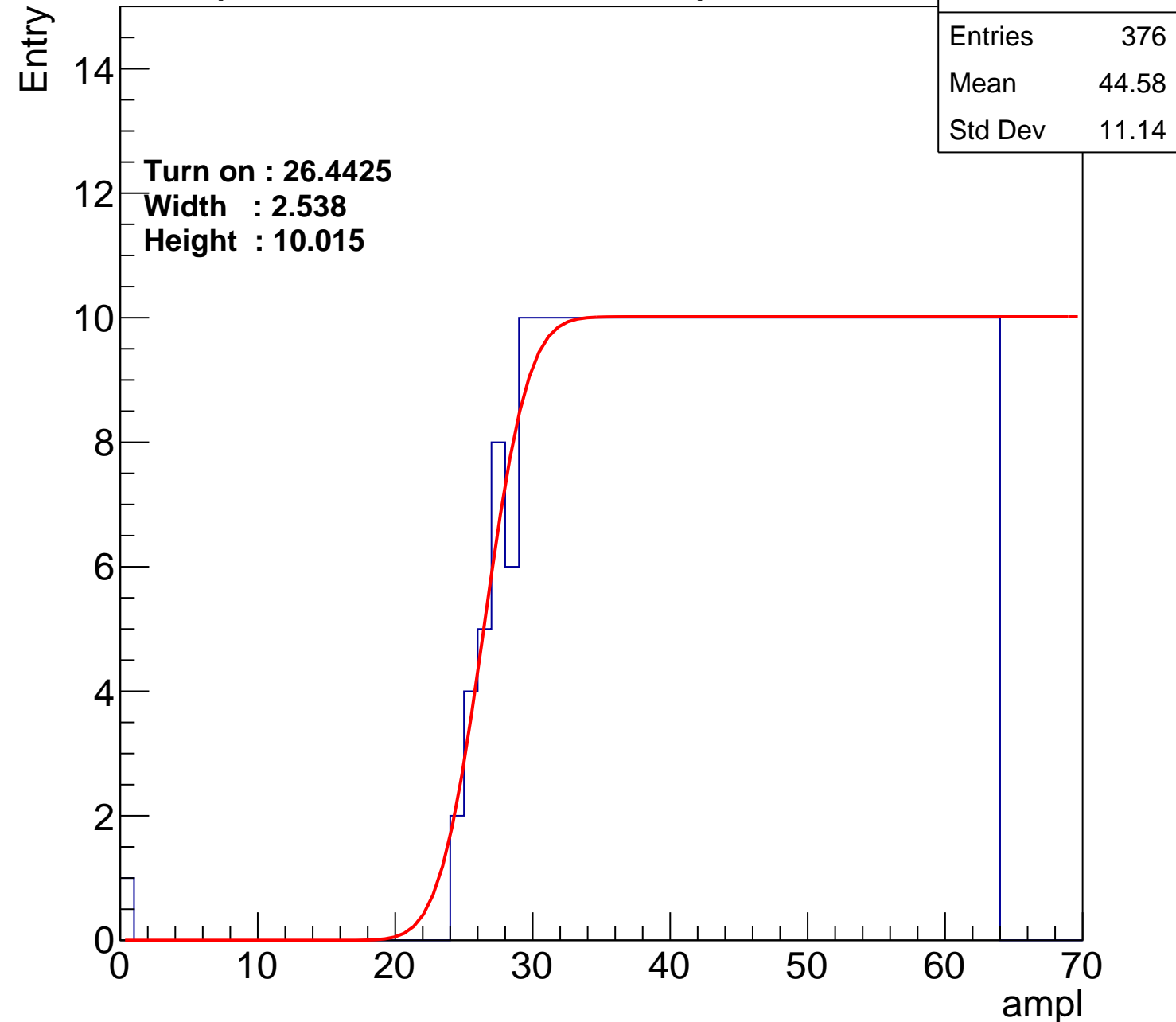
Width : 2.538

Height : 10.015

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch65

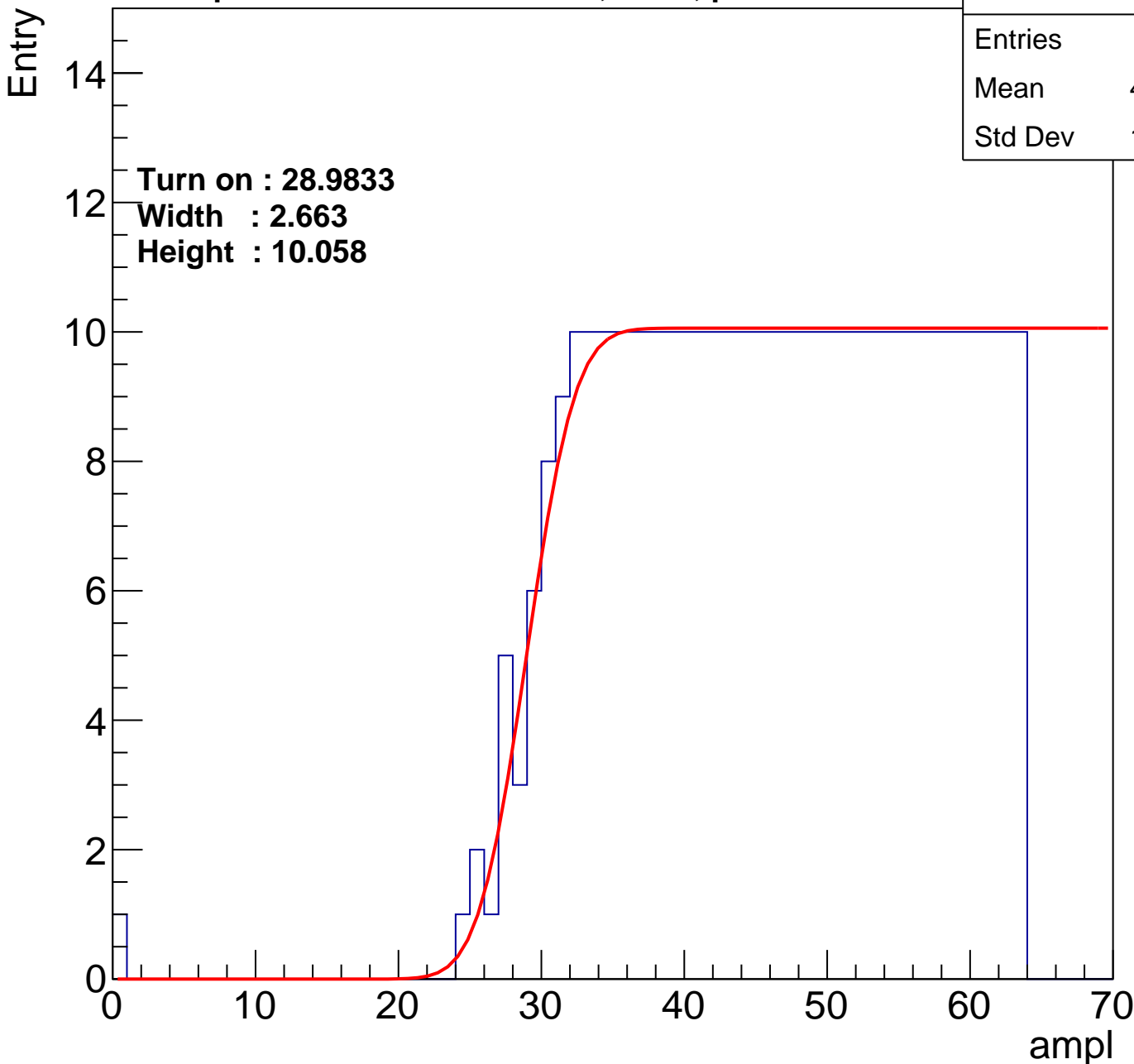
calib_packv5_042523_0143.root, FC#0, port D2

Entries	356
Mean	45.54
Std Dev	10.65

Turn on : 28.9833

Width : 2.663

Height : 10.058



B1L101S, U8-ch66

calib_packv5_042523_0143.root, FC#0, port D2

Entries	385
Mean	44.09
Std Dev	11.45

Turn on : 25.6515

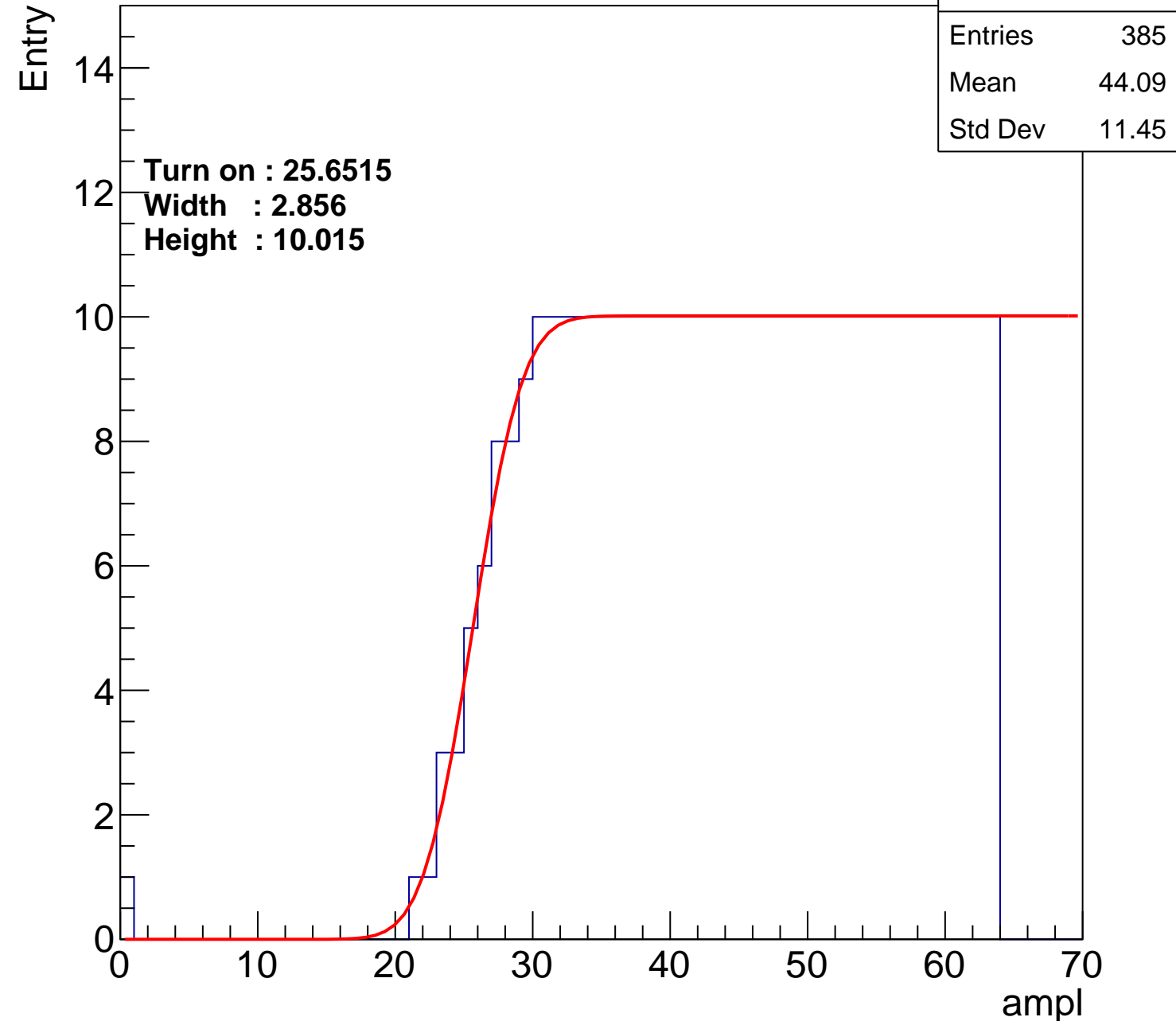
Width : 2.856

Height : 10.015

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch67

calib_packv5_042523_0143.root, FC#0, port D2

Entries	365
Mean	44.92
Std Dev	11.35

Turn on : 28.3658

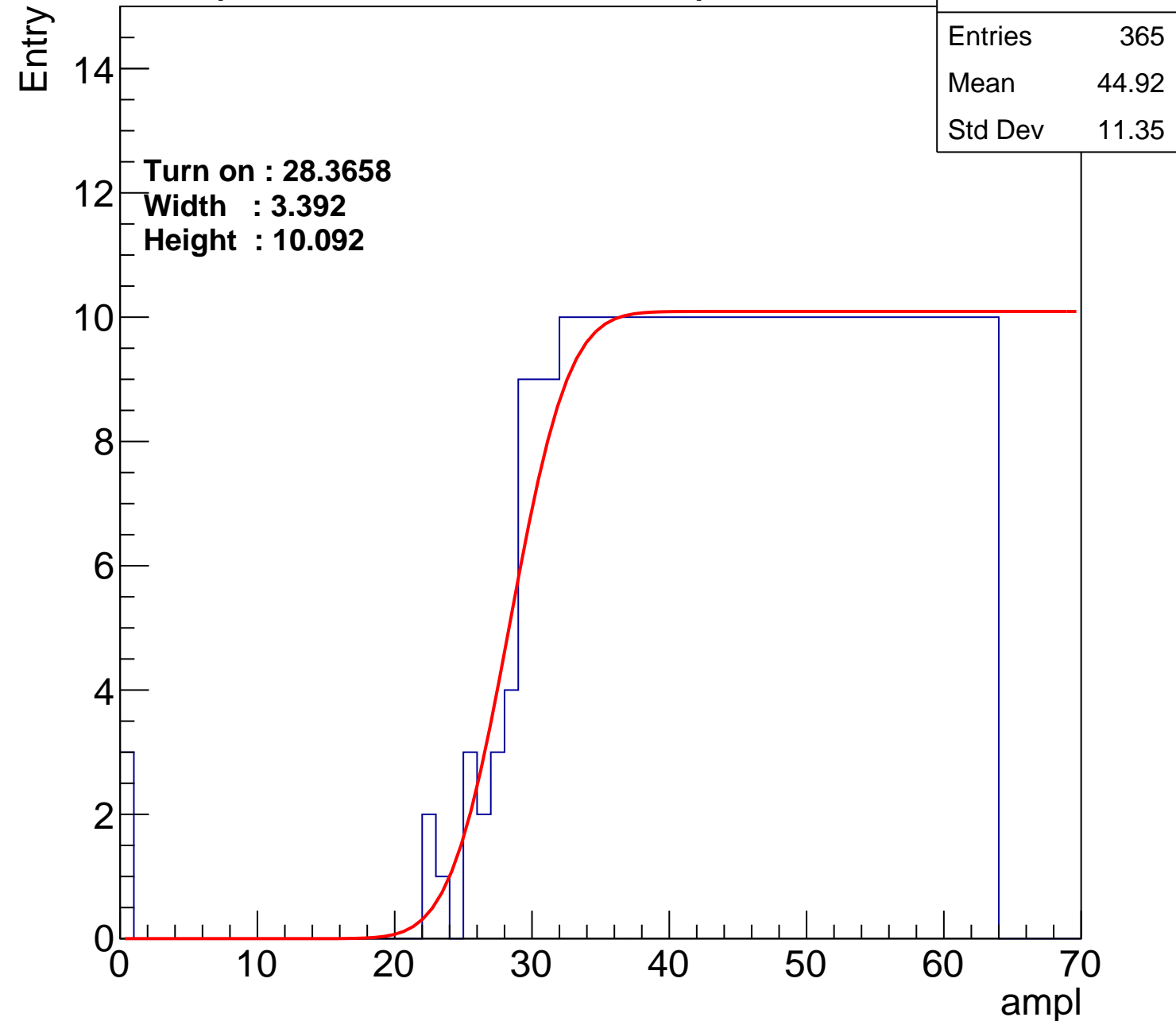
Width : 3.392

Height : 10.092

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch68

calib_packv5_042523_0143.root, FC#0, port D2

Entries	367
Mean	44.84
Std Dev	11.27

Turn on : 27.7329

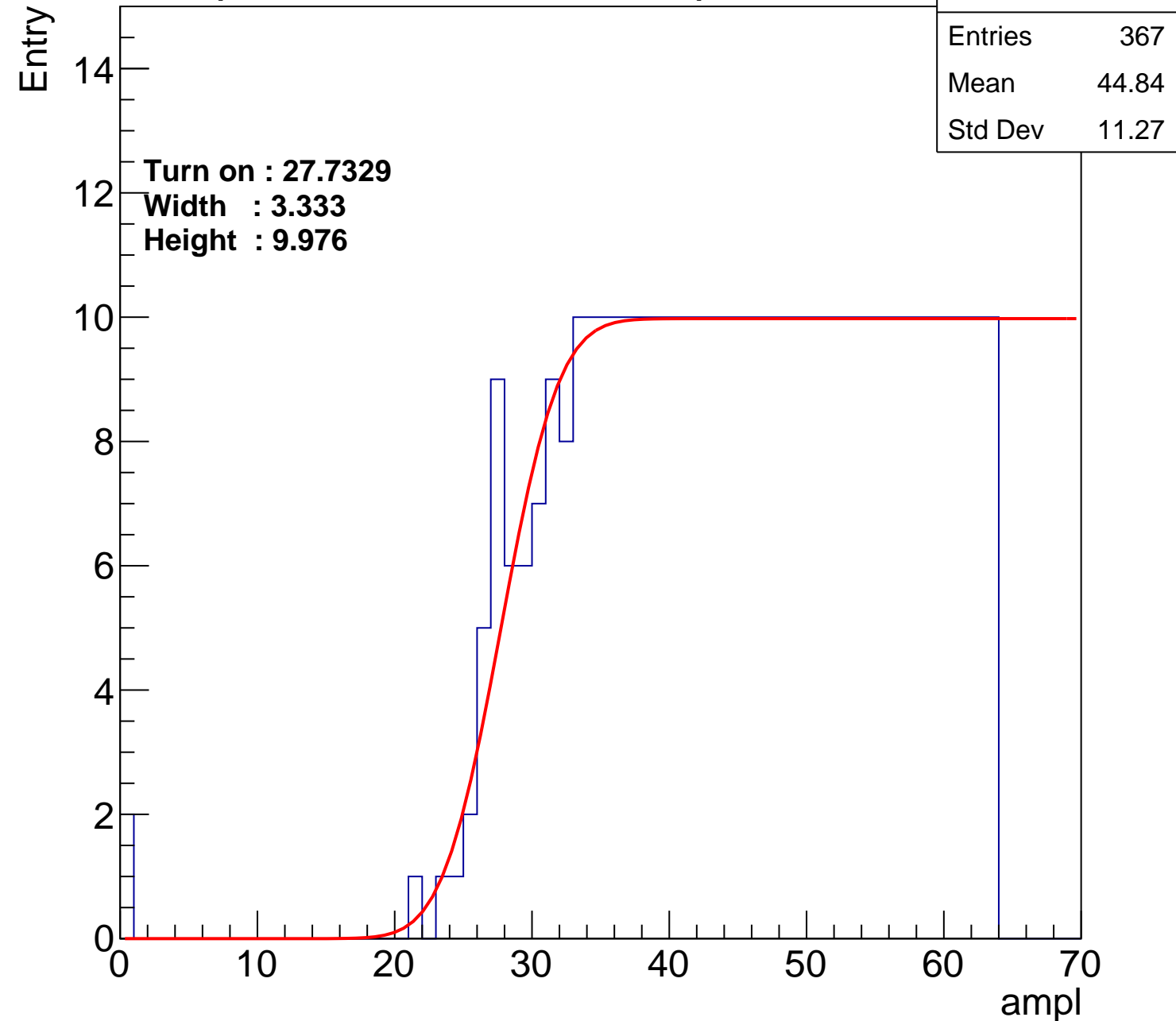
Width : 3.333

Height : 9.976

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch69

calib_packv5_042523_0143.root, FC#0, port D2

Entries	371
Mean	44.69
Std Dev	11.32

Turn on : 27.6375

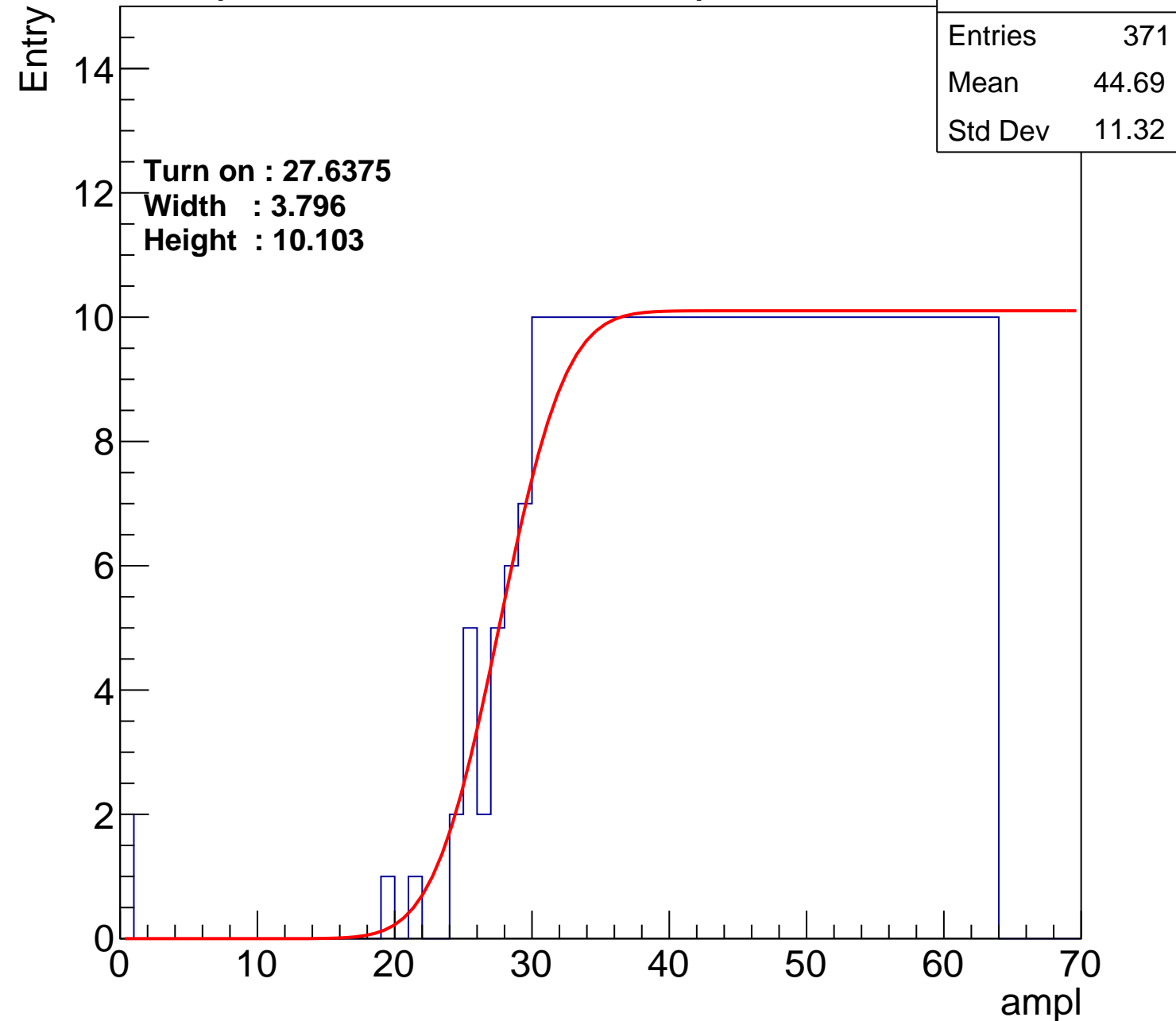
Width : 3.796

Height : 10.103

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch70

calib_packv5_042523_0143.root, FC#0, port D2

Entries	385
Mean	43.72
Std Dev	12.31

Turn on : 26.4627

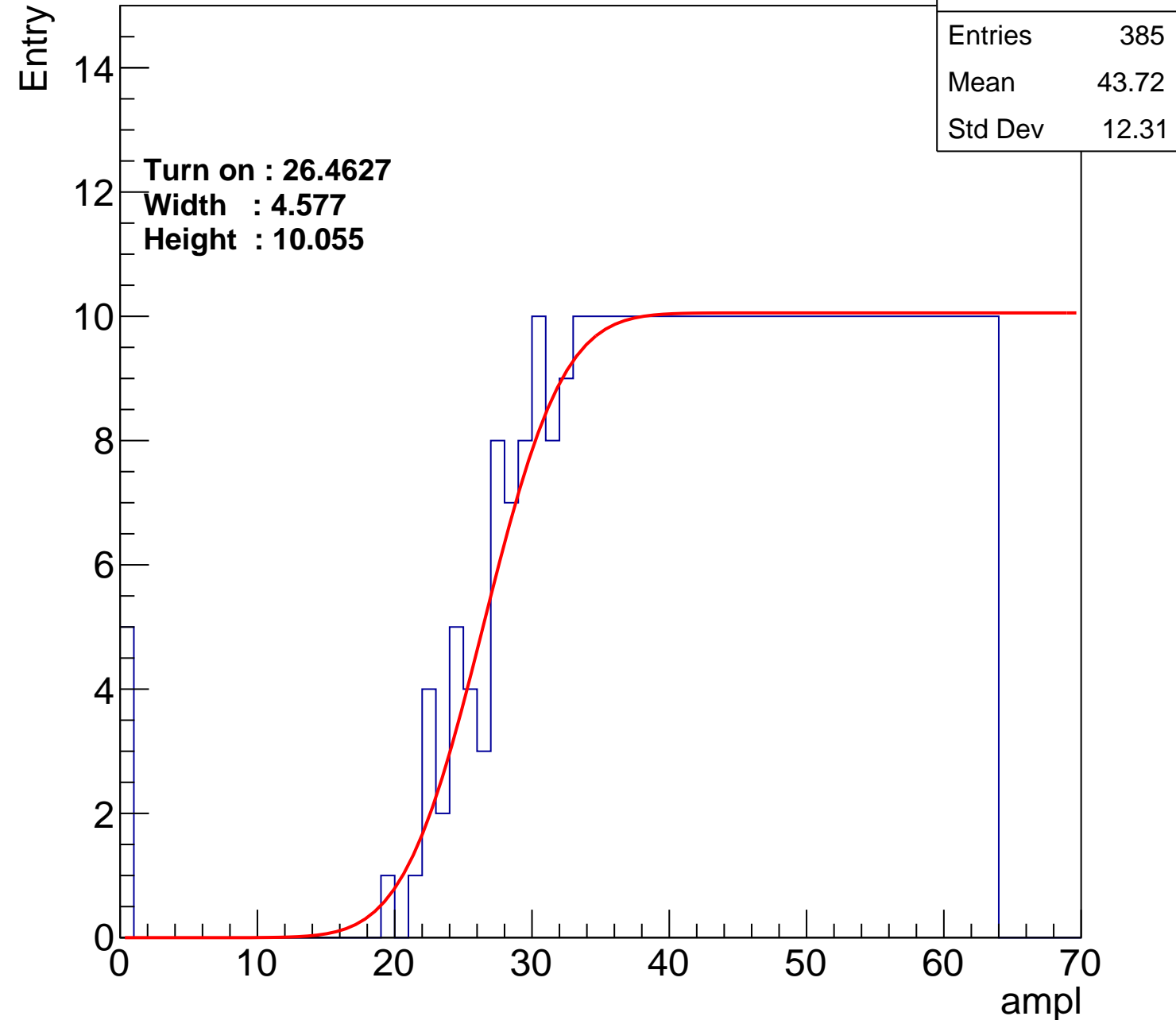
Width : 4.577

Height : 10.055

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch71

calib_packv5_042523_0143.root, FC#0, port D2

Entries	376
Mean	44.39
Std Dev	11.6

Turn on : 26.6205

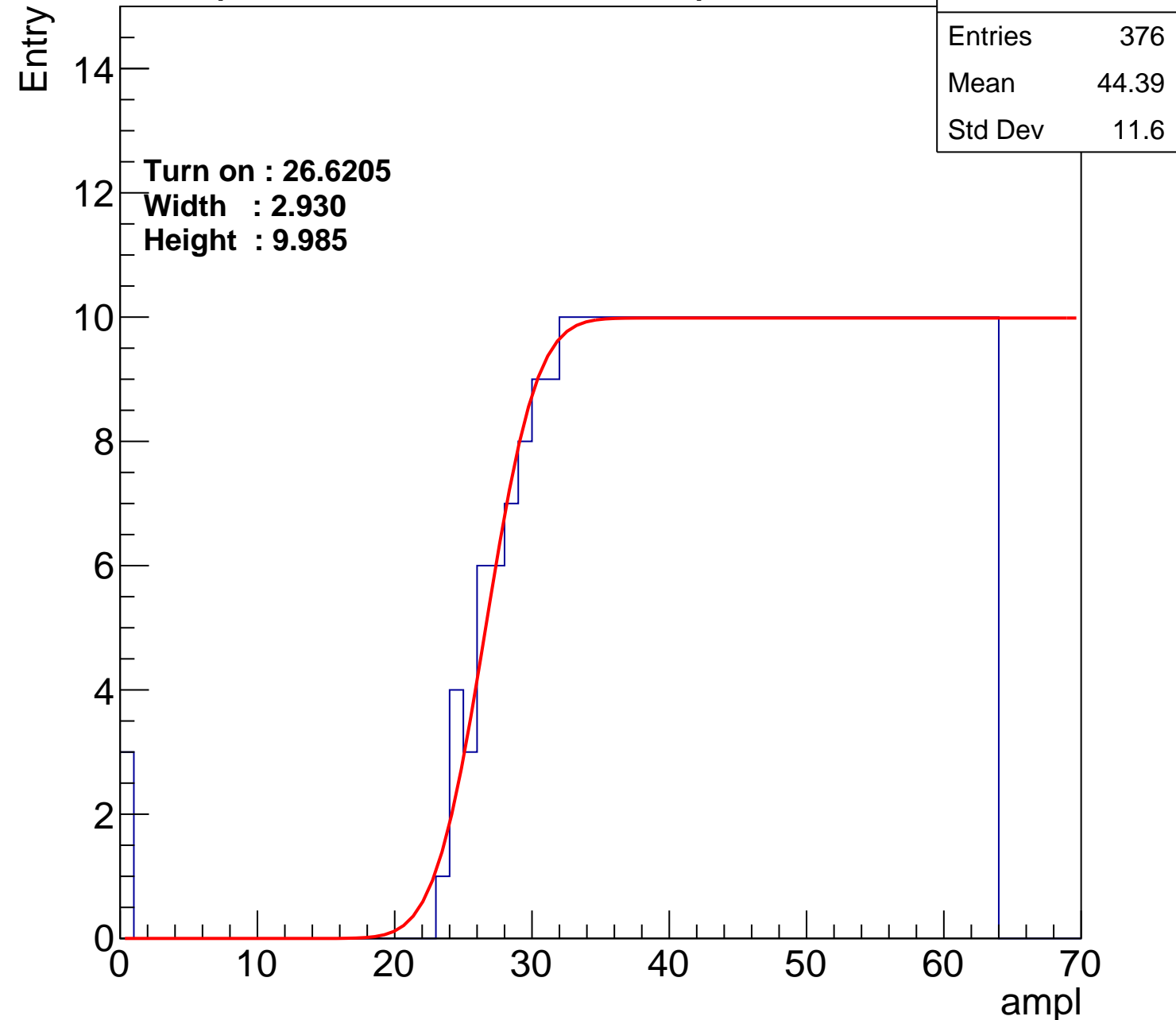
Width : 2.930

Height : 9.985

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch72

calib_packv5_042523_0143.root, FC#0, port D2

Entries	389
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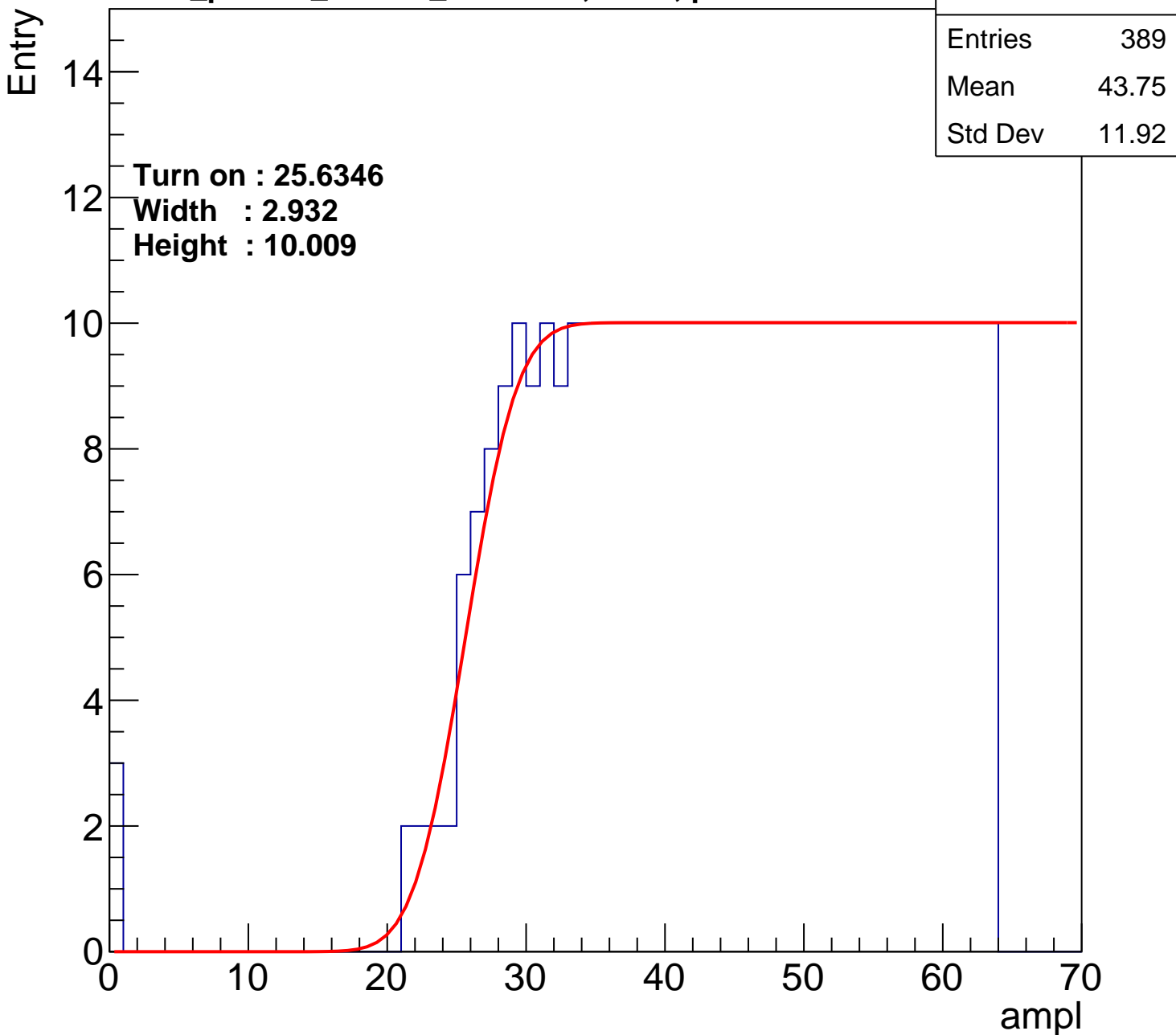
Mean	43.75
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Std Dev	11.92
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Turn on : 25.6346

Width : 2.932

Height : 10.009



B1L101S, U8-ch73

calib_packv5_042523_0143.root, FC#0, port D2

Entries	360
Mean	45.22
Std Dev	11.05

Turn on : 28.4934

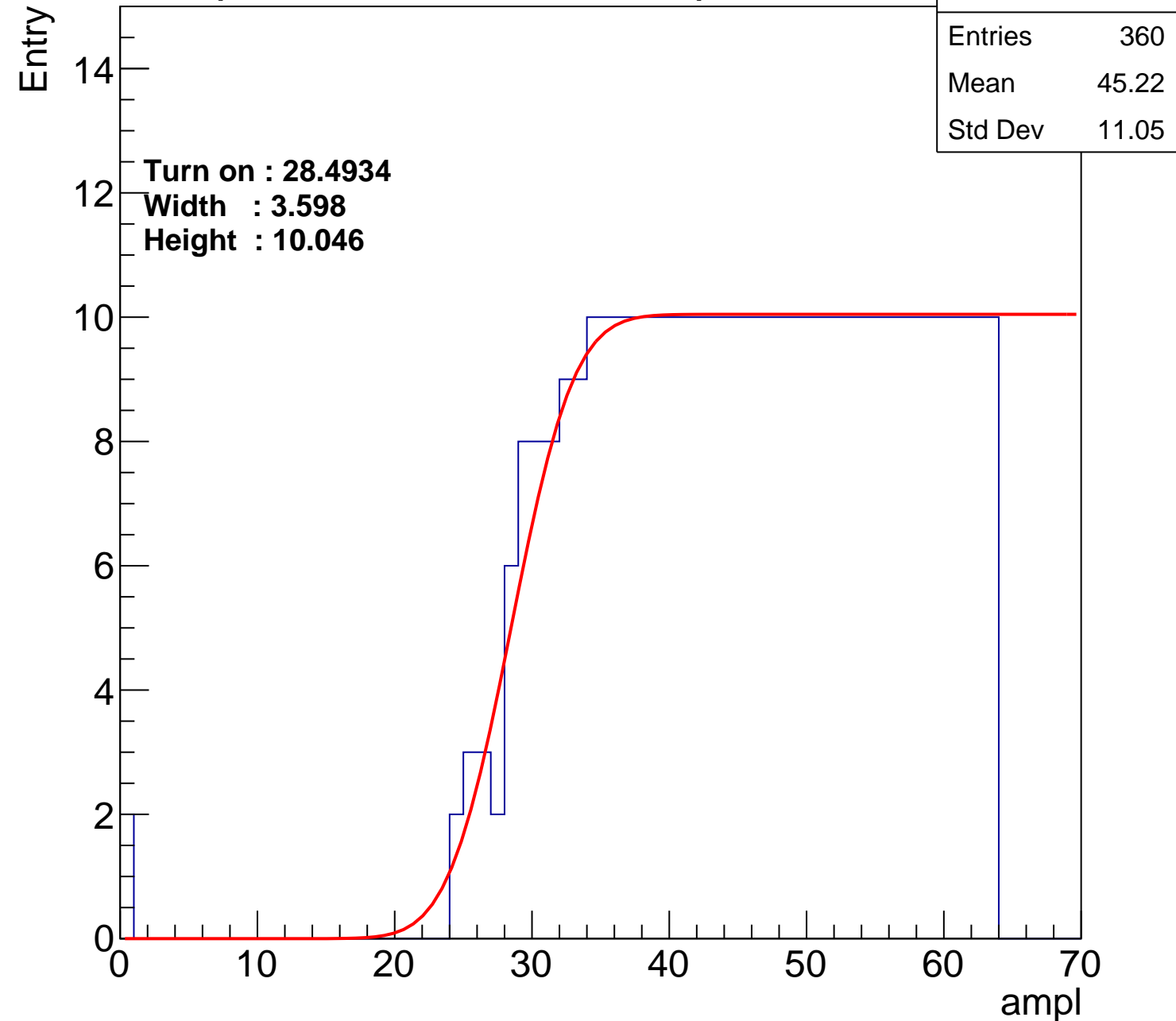
Width : 3.598

Height : 10.046

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch74

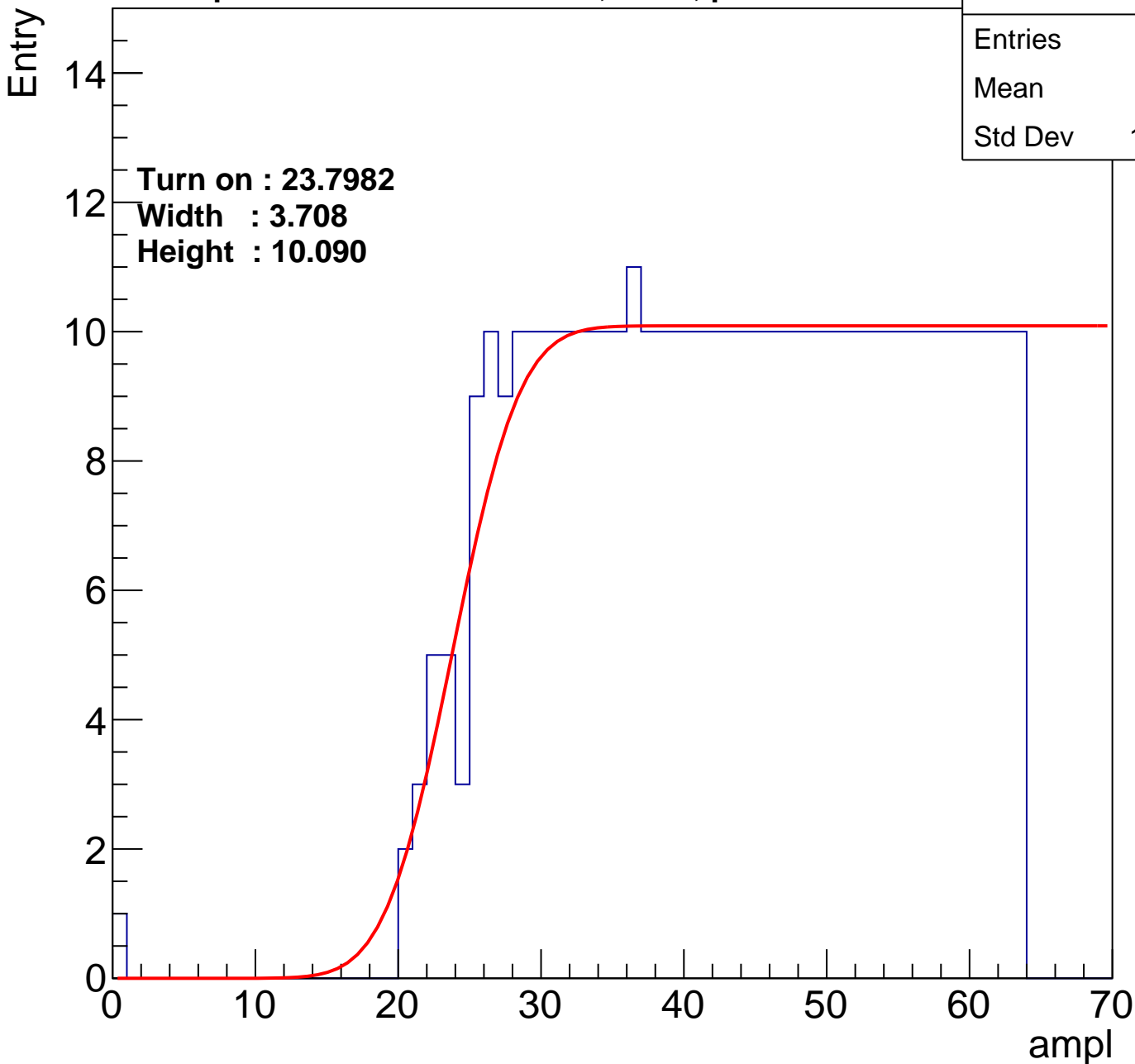
calib_packv5_042523_0143.root, FC#0, port D2

Entries	408
Mean	43
Std Dev	12.02

Turn on : 23.7982

Width : 3.708

Height : 10.090



B1L101S, U8-ch75

calib_packv5_042523_0143.root, FC#0, port D2

Entries	401
Mean	43.19
Std Dev	12.18

Turn on : 24.3793

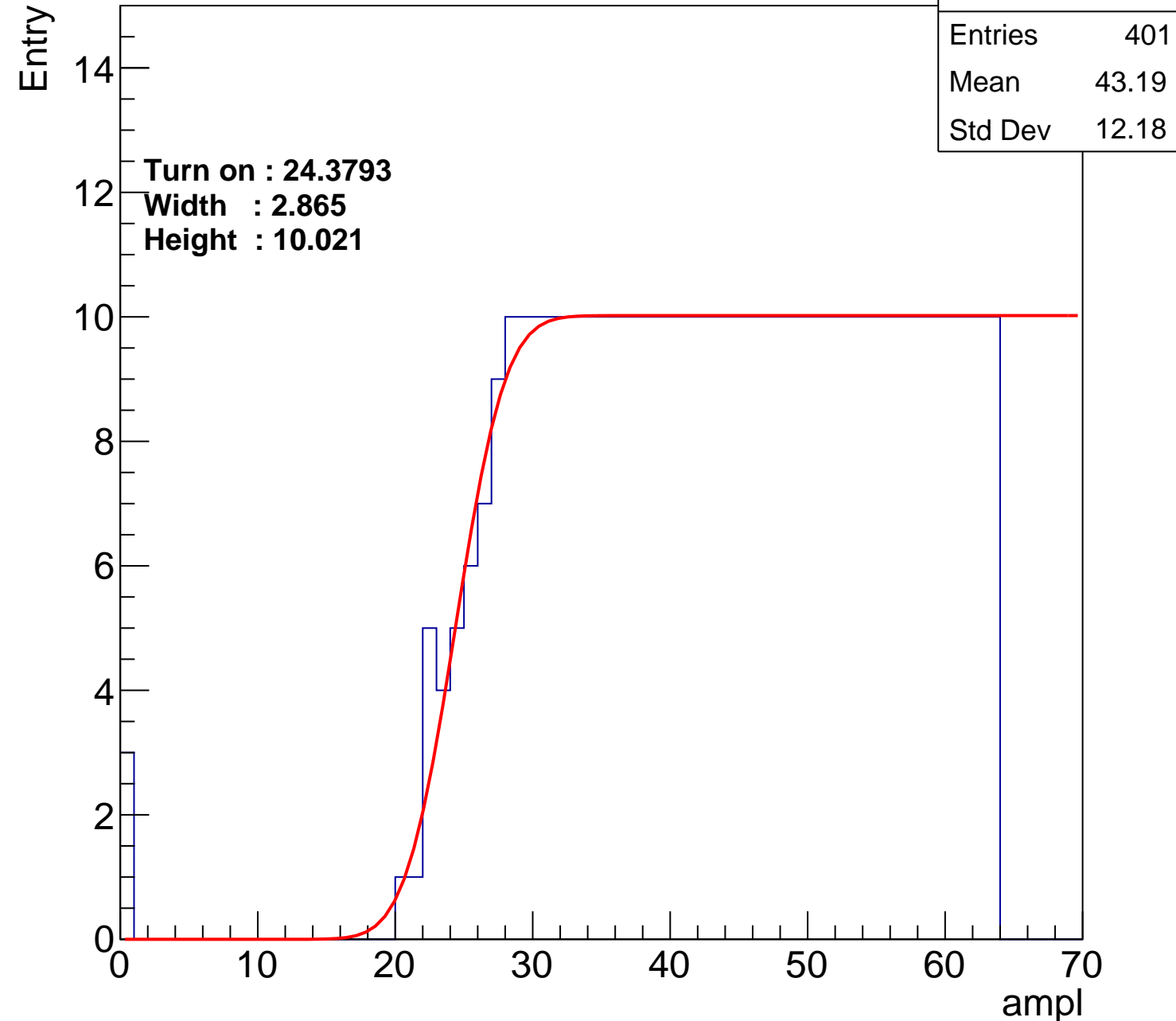
Width : 2.865

Height : 10.021

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch76

calib_packv5_042523_0143.root, FC#0, port D2

Entries	371
Mean	44.76
Std Dev	11.2

Turn on : 27.0624

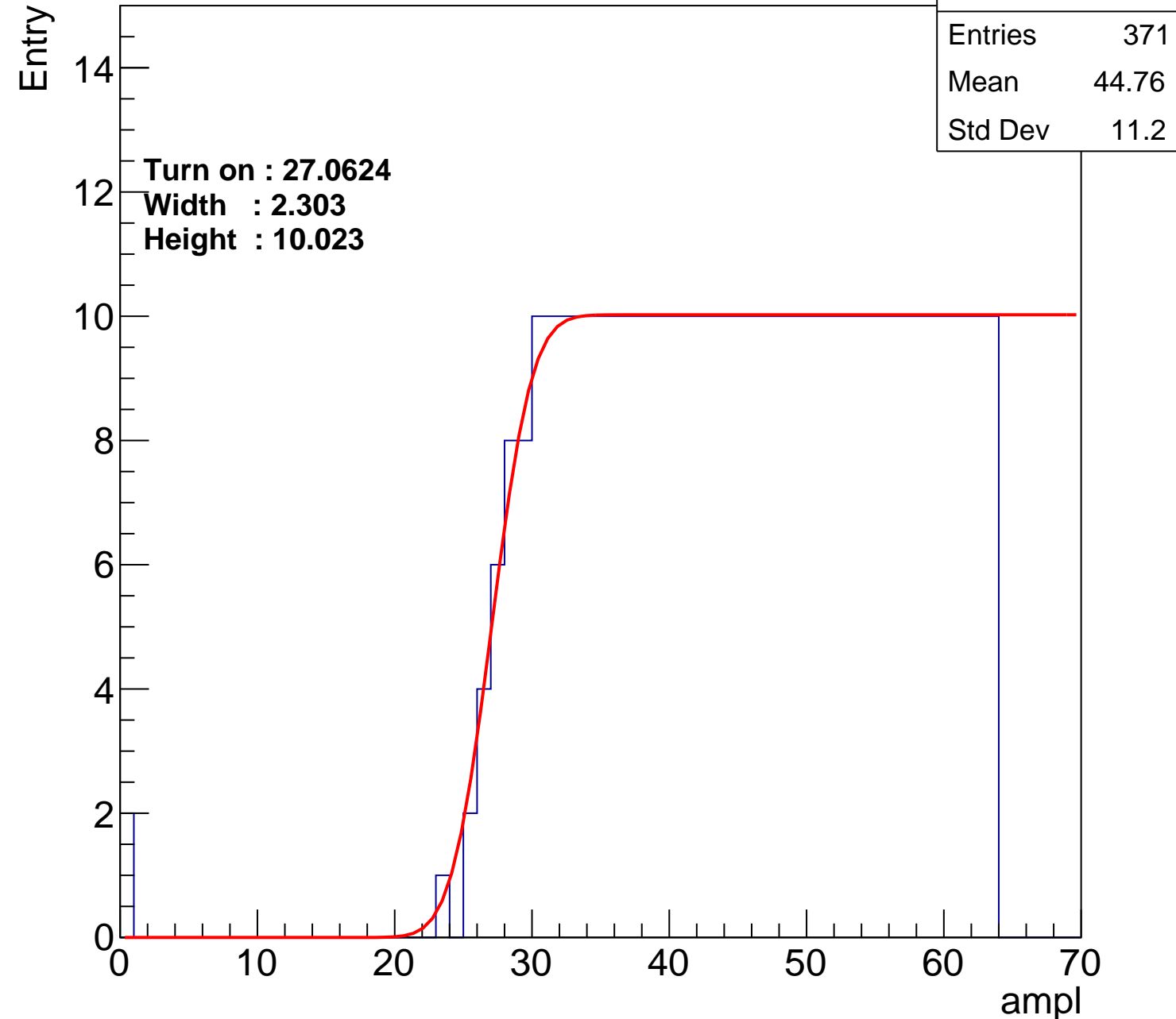
Width : 2.303

Height : 10.023

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch77

calib_packv5_042523_0143.root, FC#0, port D2

Entries	386
Mean	43.65
Std Dev	12.49

Turn on : 26.2054

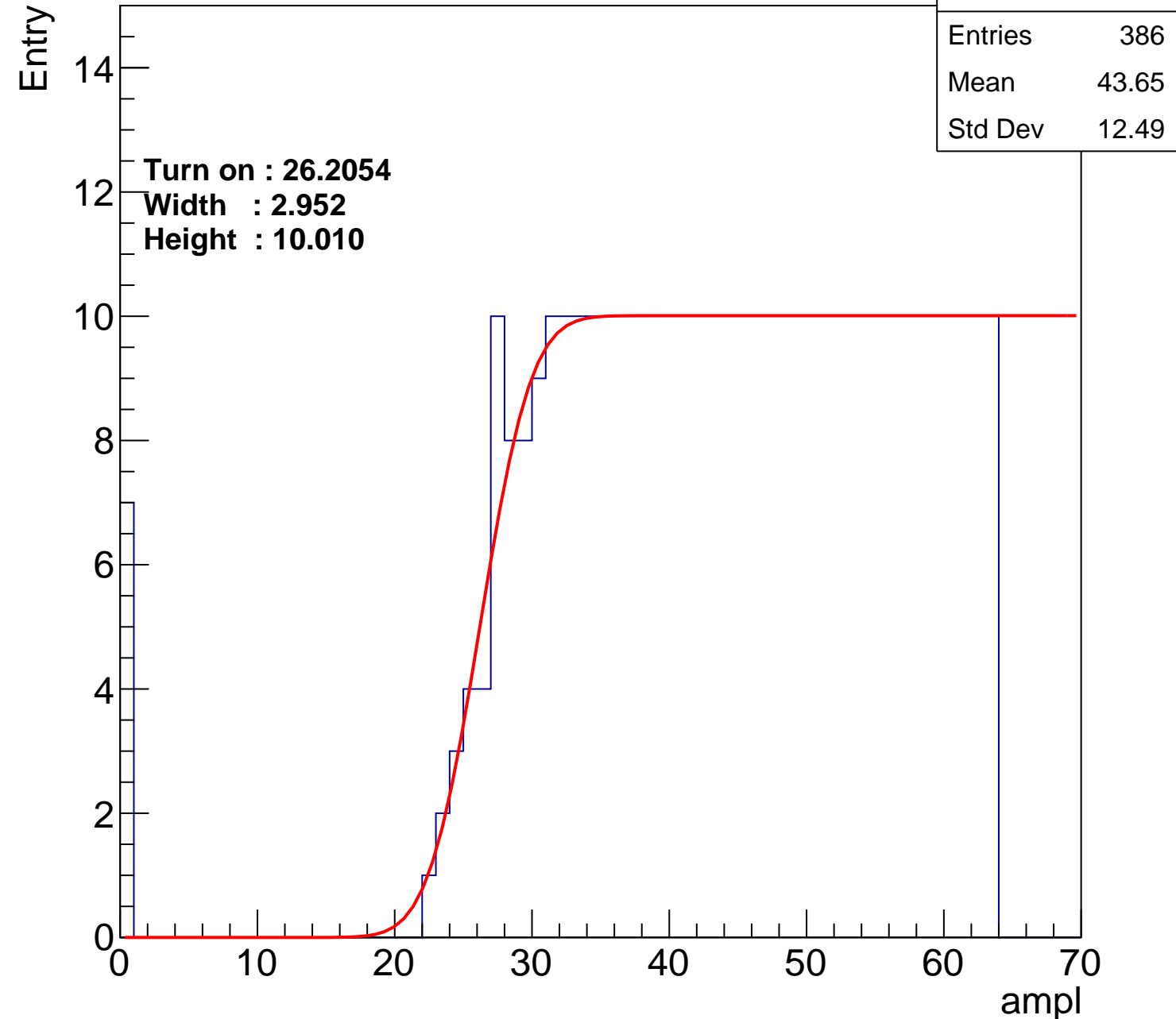
Width : 2.952

Height : 10.010

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch78

calib_packv5_042523_0143.root, FC#0, port D2

Entries	379
Mean	44.19
Std Dev	11.83

Turn on : 26.6155

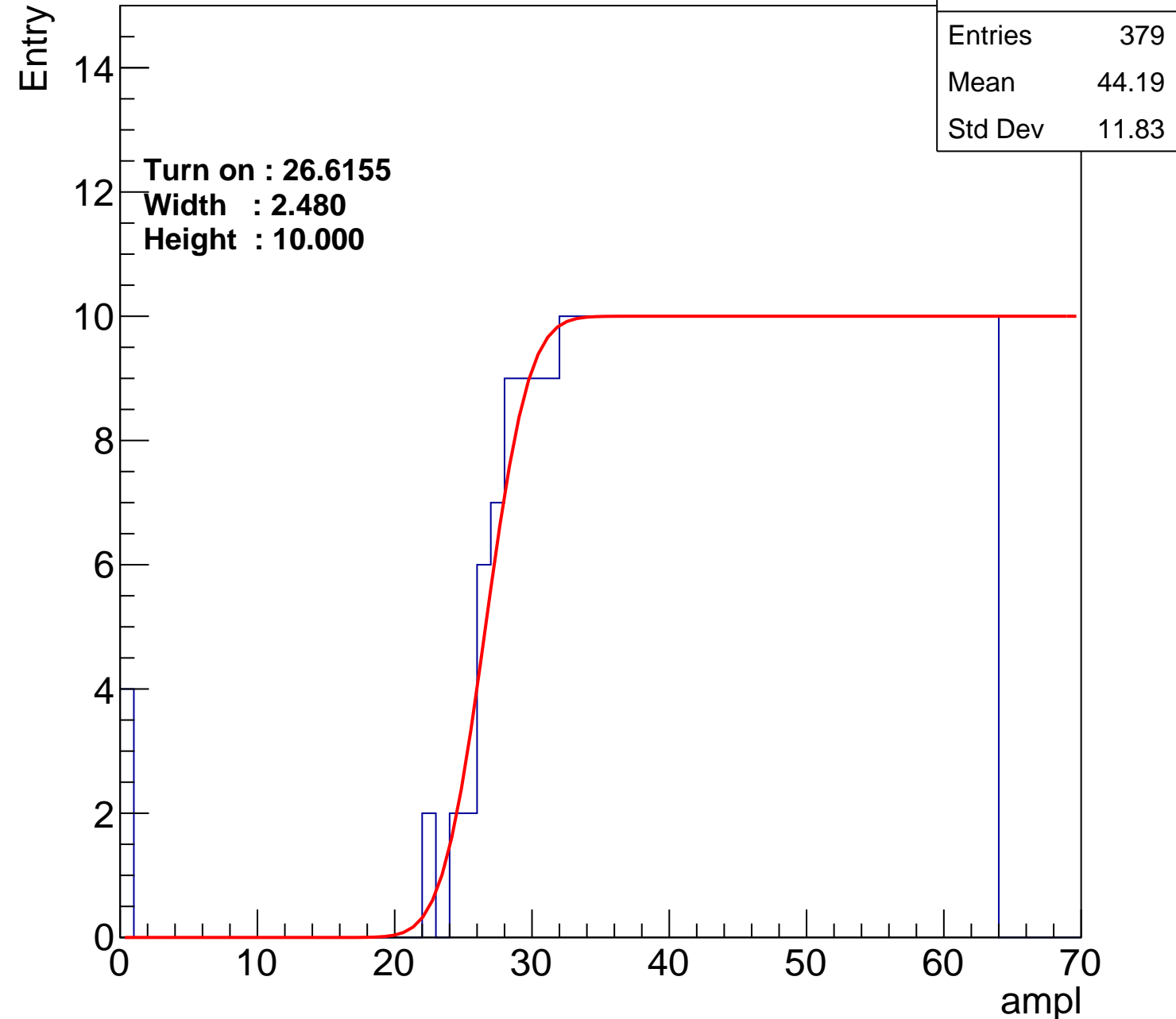
Width : 2.480

Height : 10.000

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch79

calib_packv5_042523_0143.root, FC#0, port D2

Entries	375
Mean	44.4
Std Dev	11.72

Turn on : 26.9933

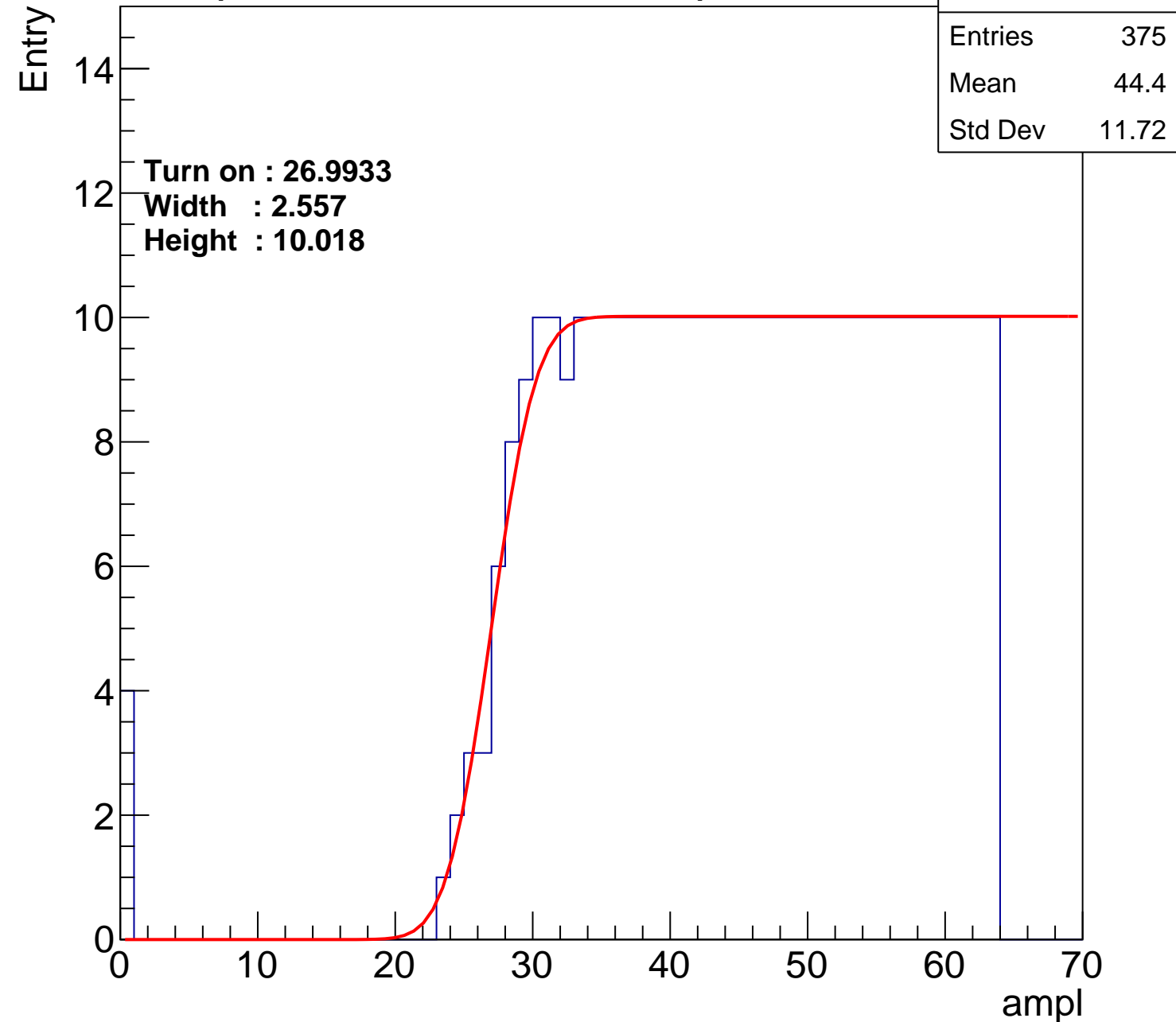
Width : 2.557

Height : 10.018

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch80

calib_packv5_042523_0143.root, FC#0, port D2

Entries	381
Mean	44.1
Std Dev	11.86

Turn on : 26.5478

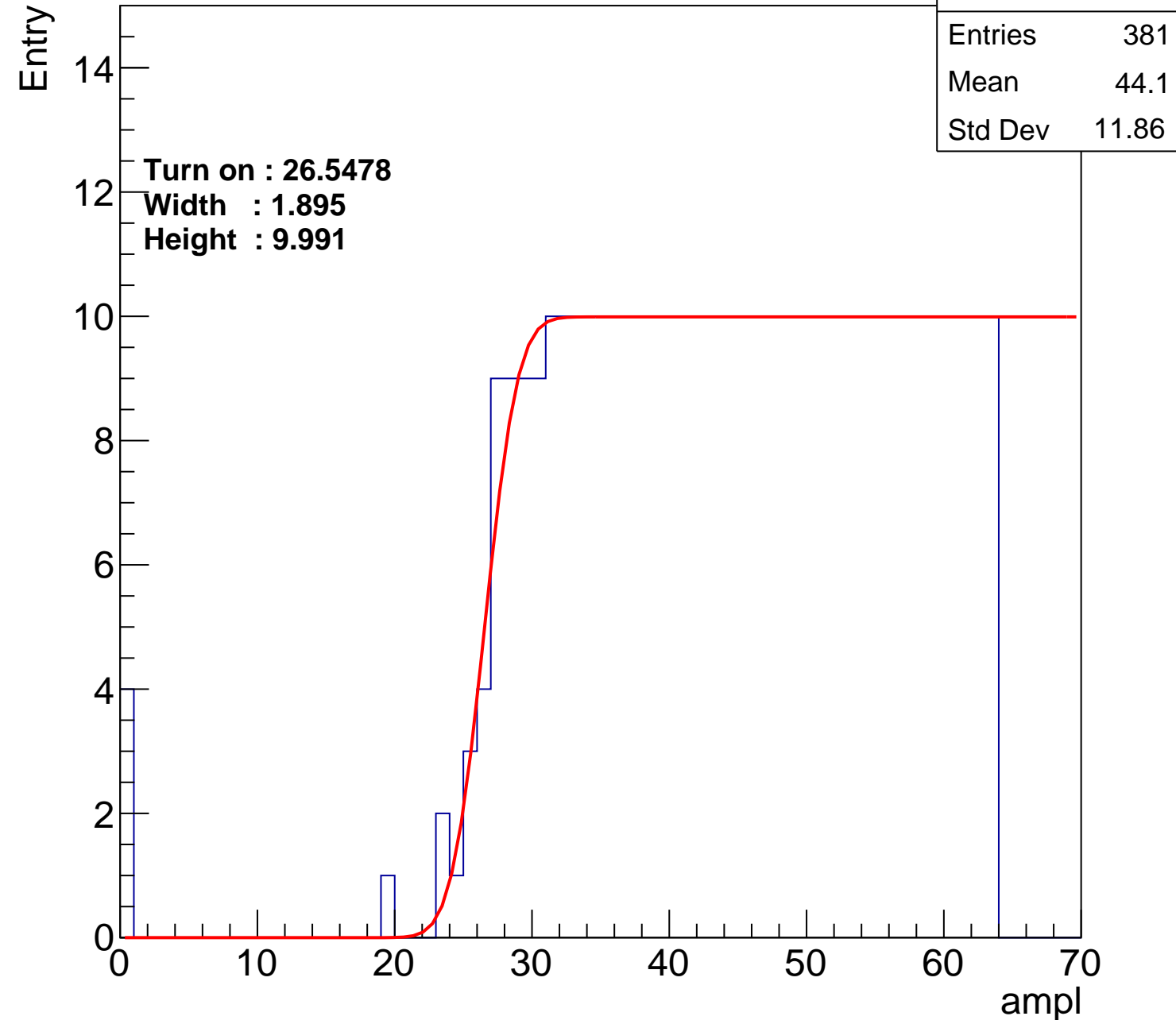
Width : 1.895

Height : 9.991

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch81

calib_packv5_042523_0143.root, FC#0, port D2

Entries	393
Mean	43.64
Std Dev	11.82

Turn on : 25.1007

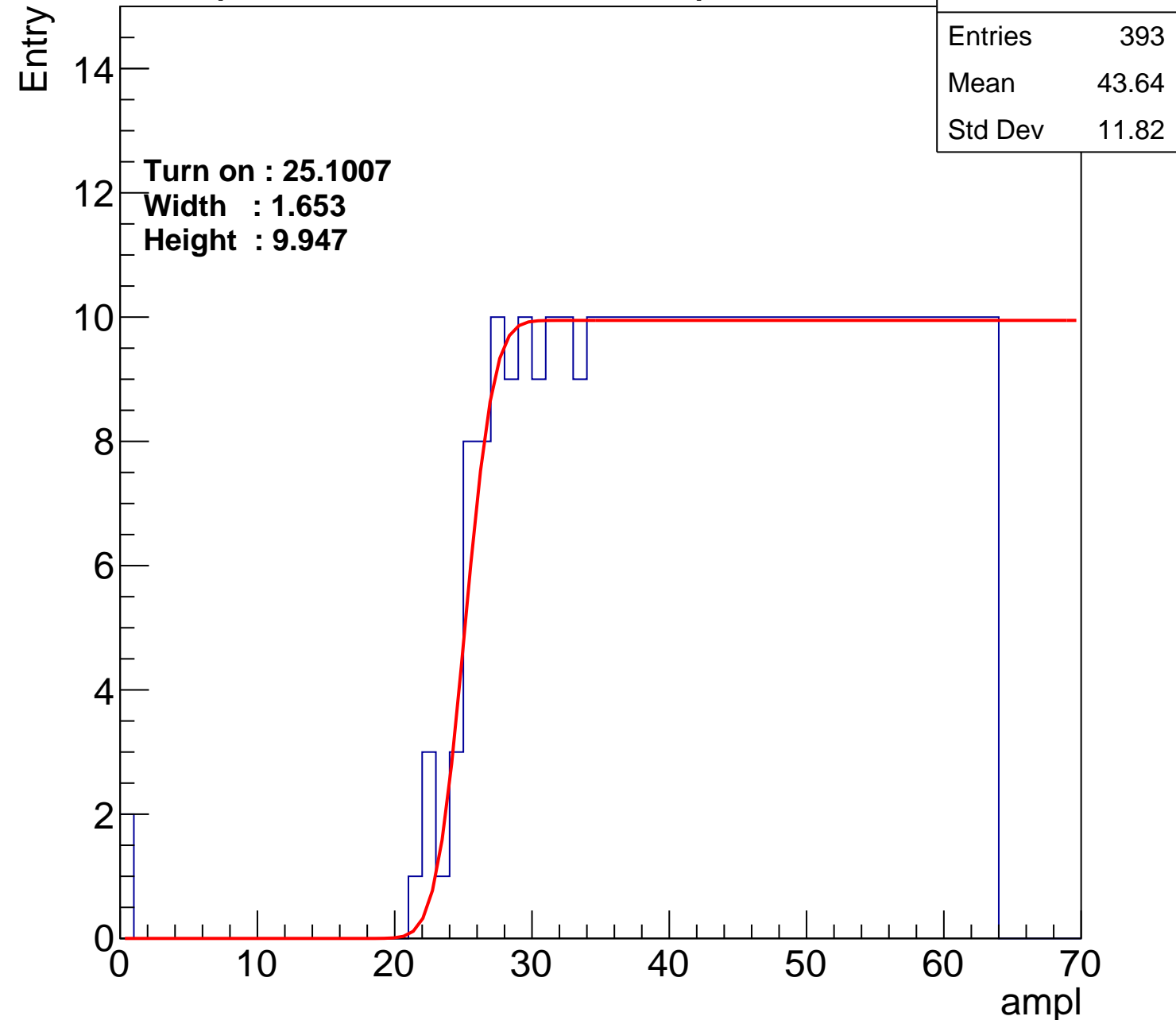
Width : 1.653

Height : 9.947

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch82

calib_packv5_042523_0143.root, FC#0, port D2

Entries 379

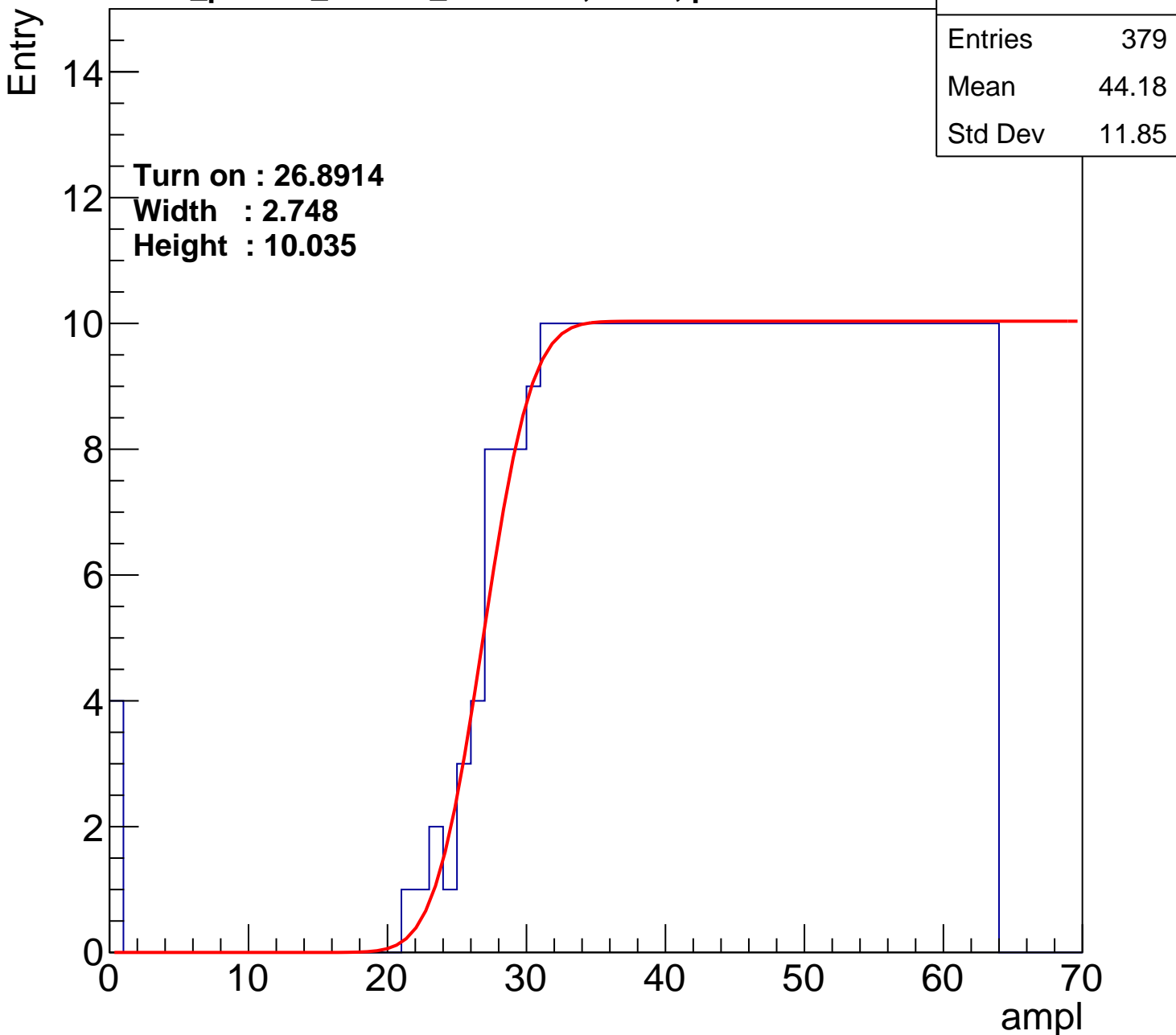
Mean 44.18

Std Dev 11.85

Turn on : 26.8914

Width : 2.748

Height : 10.035



B1L101S, U8-ch83

calib_packv5_042523_0143.root, FC#0, port D2

Entries	374
Mean	44.48
Std Dev	11.56

Turn on : 26.9505

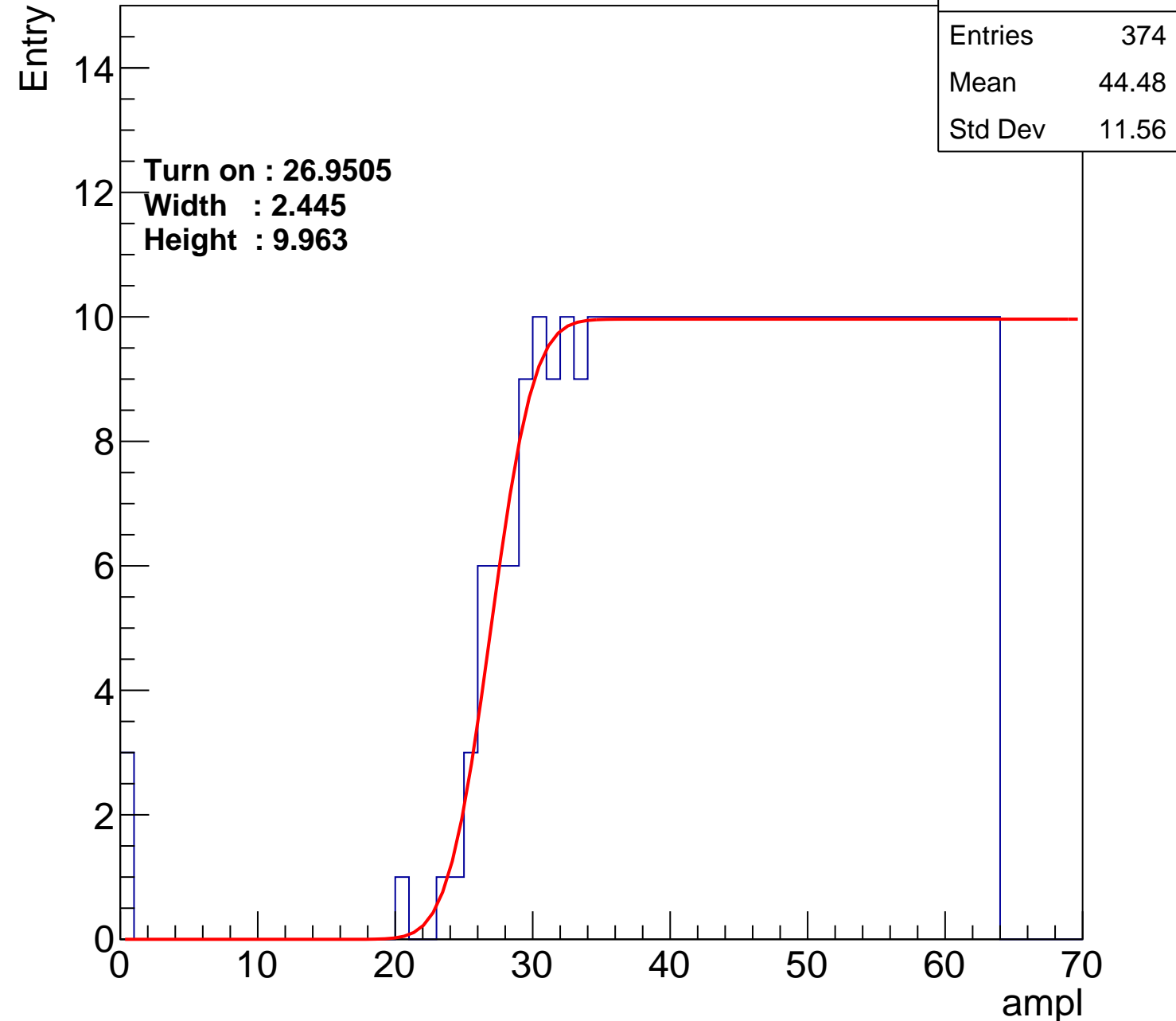
Width : 2.445

Height : 9.963

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch84

calib_packv5_042523_0143.root, FC#0, port D2

Entries	387
Mean	43.91
Std Dev	11.72

Turn on : 25.8931

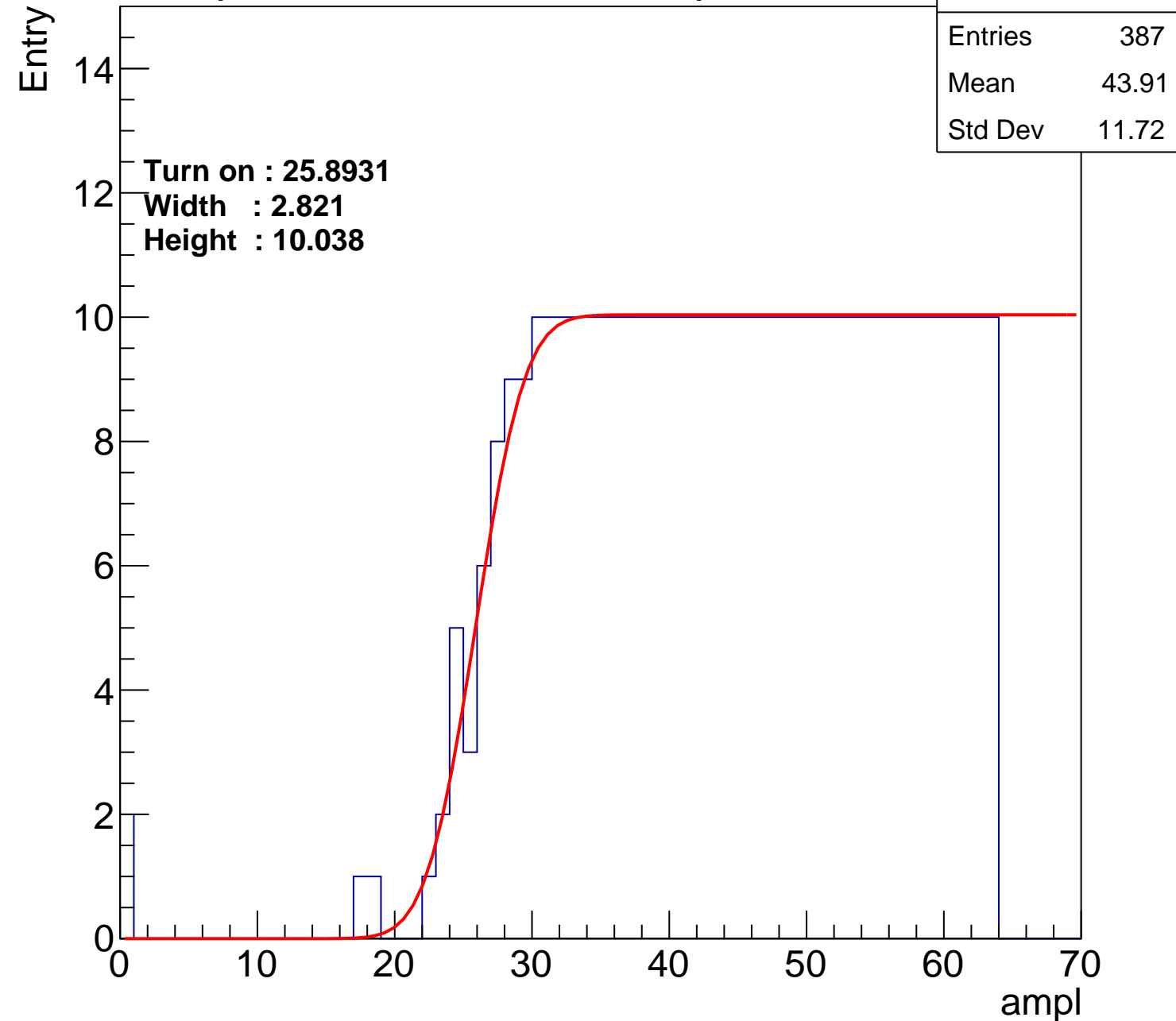
Width : 2.821

Height : 10.038

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch85

calib_packv5_042523_0143.root, FC#0, port D2

Entries	381
Mean	44.13
Std Dev	11.74

Turn on : 26.5724

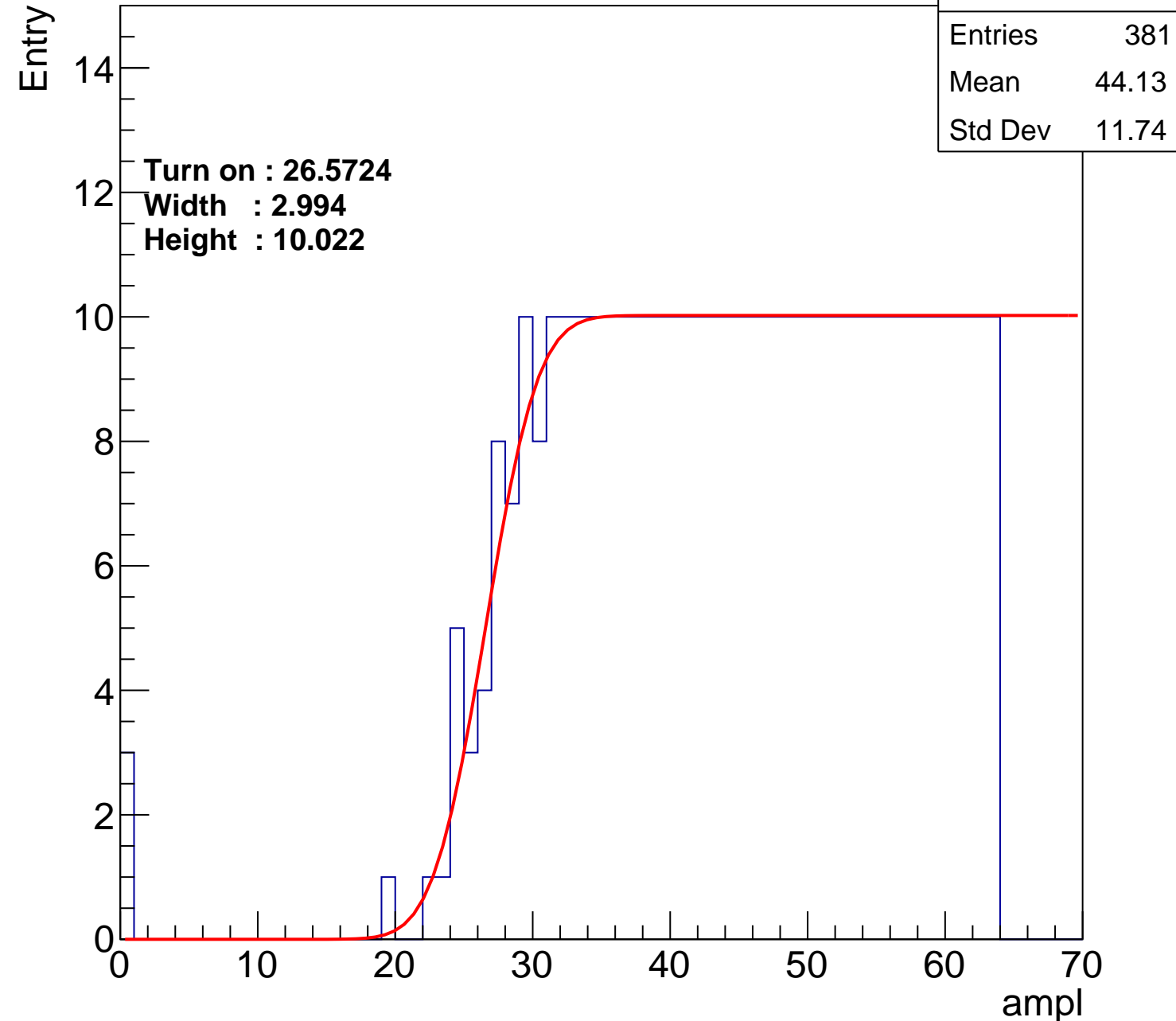
Width : 2.994

Height : 10.022

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch86

calib_packv5_042523_0143.root, FC#0, port D2

Entries	385
Mean	43.79
Std Dev	12.2

Turn on : 26.2544

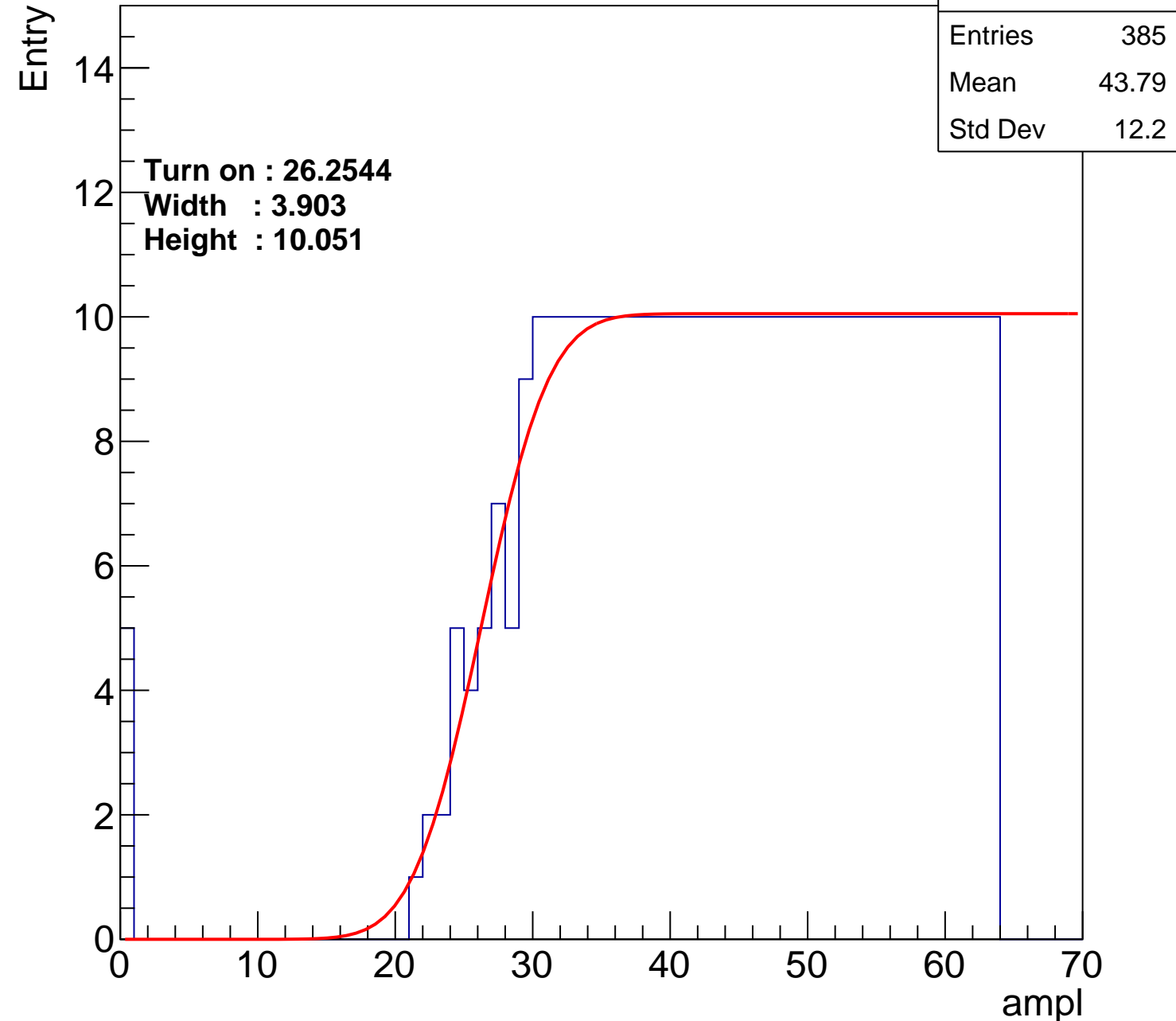
Width : 3.903

Height : 10.051

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch87

calib_packv5_042523_0143.root, FC#0, port D2

Entries	376
Mean	44.45
Std Dev	11.42

Turn on : 26.6949

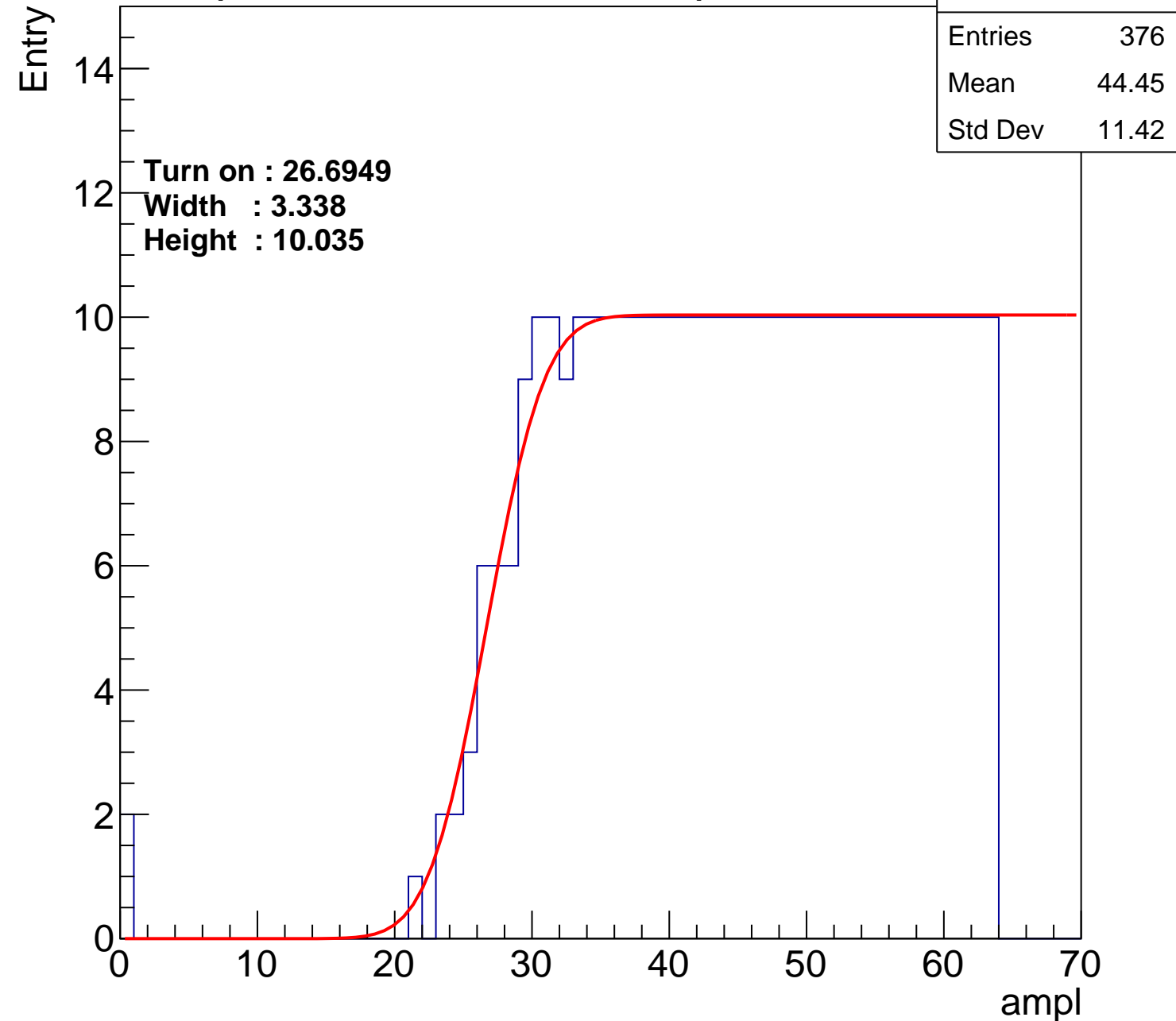
Width : 3.338

Height : 10.035

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch88

calib_packv5_042523_0143.root, FC#0, port D2

Entries	386
Mean	43.92
Std Dev	11.8

Turn on : 25.7877

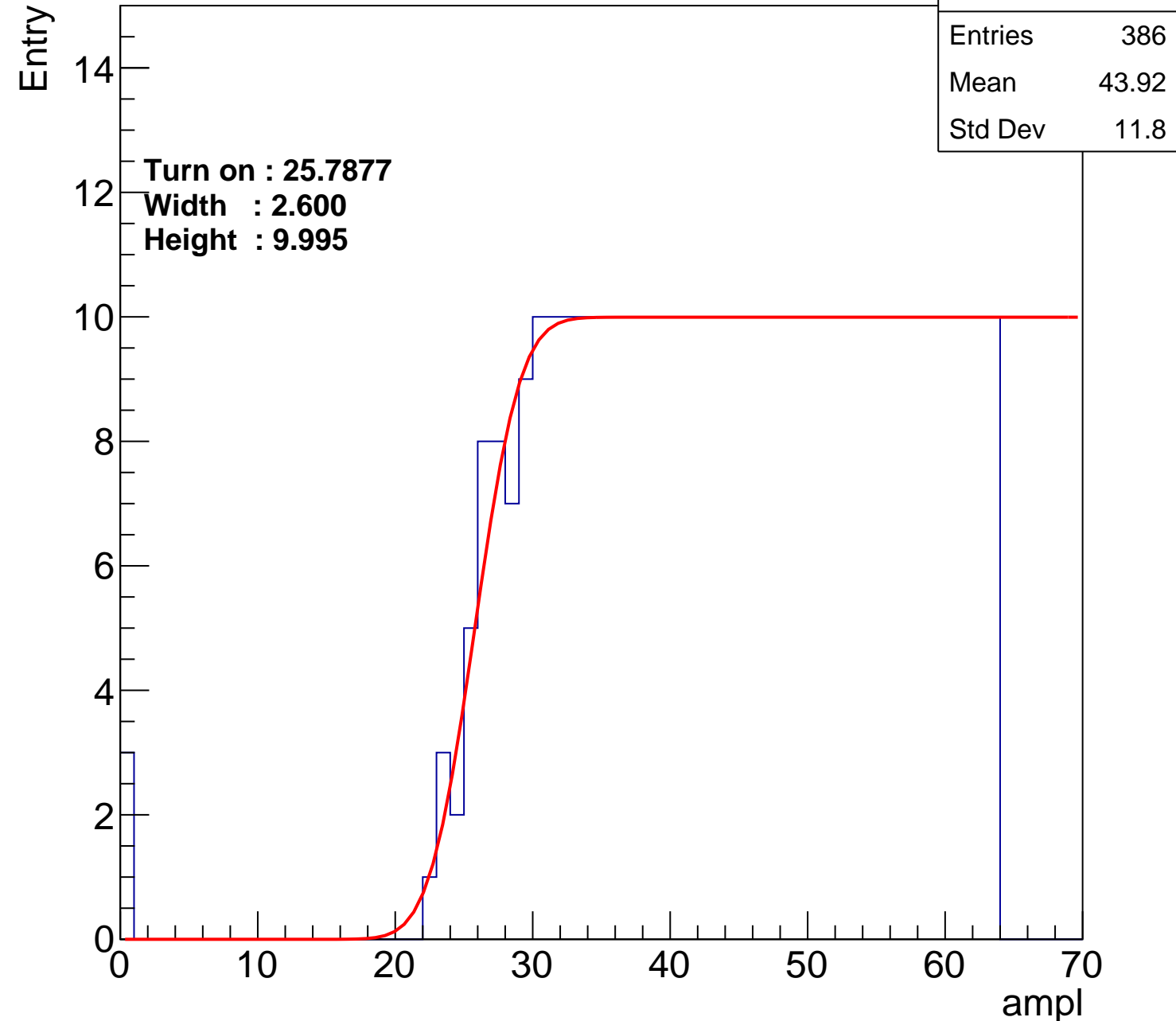
Width : 2.600

Height : 9.995

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch89

calib_packv5_042523_0143.root, FC#0, port D2

Entries	366
Mean	44.75
Std Dev	11.73

Turn on : 28.3791

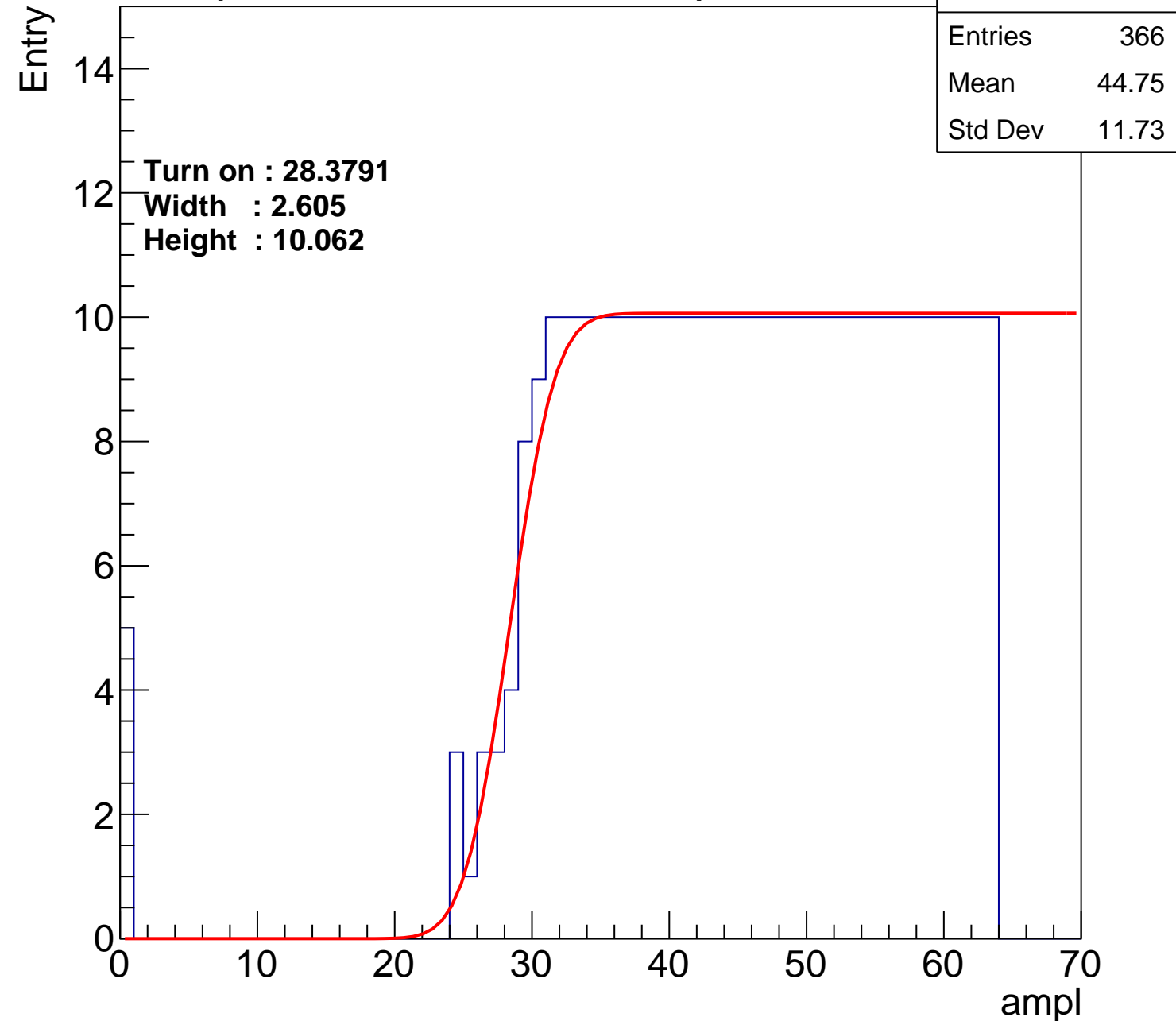
Width : 2.605

Height : 10.062

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch90

calib_packv5_042523_0143.root, FC#0, port D2

Entries	401
Mean	43.18
Std Dev	12.19

Turn on : 24.3316

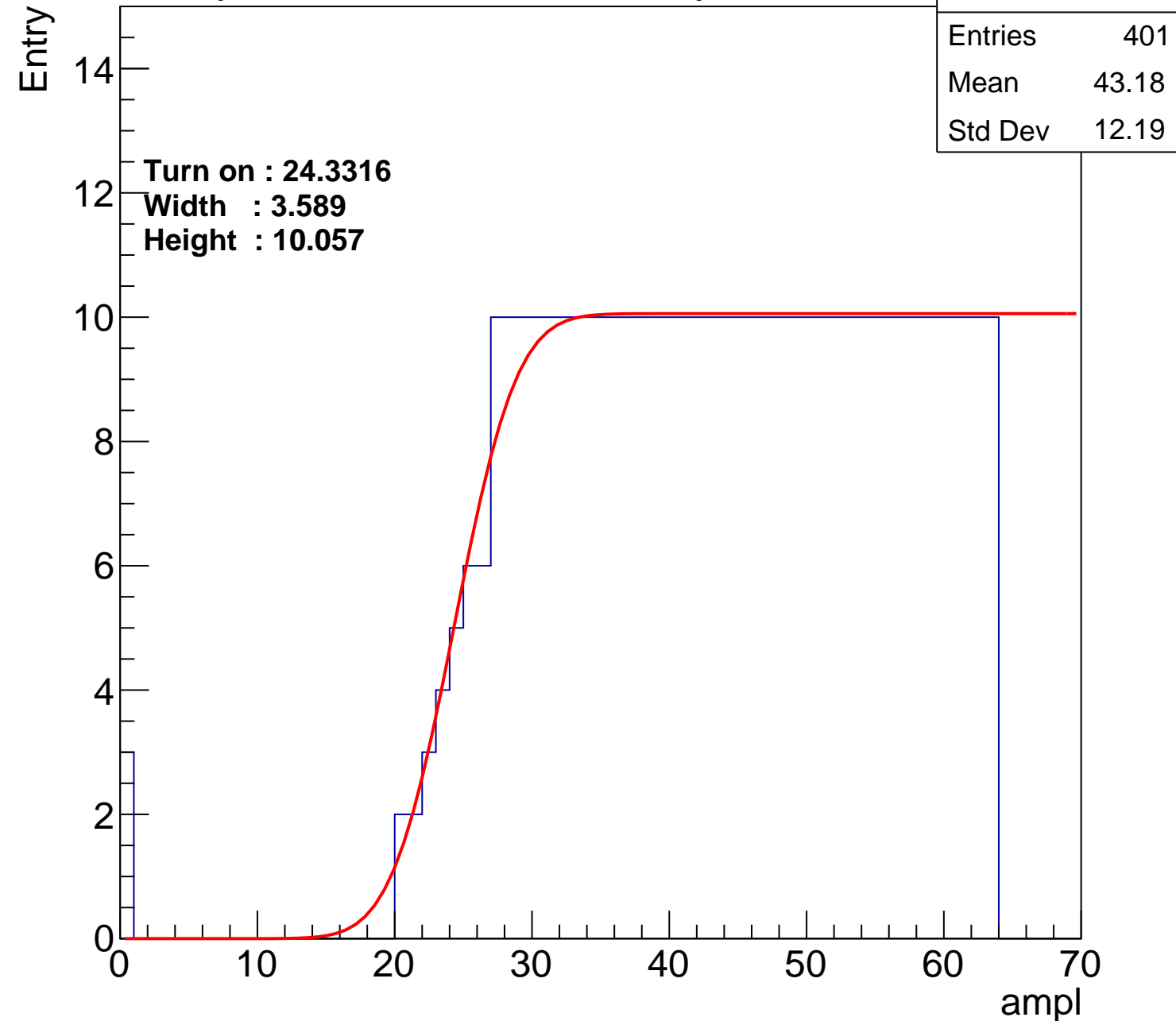
Width : 3.589

Height : 10.057

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch91

calib_packv5_042523_0143.root, FC#0, port D2

Entries	372
Mean	44.64
Std Dev	11.34

Turn on : 27.1206

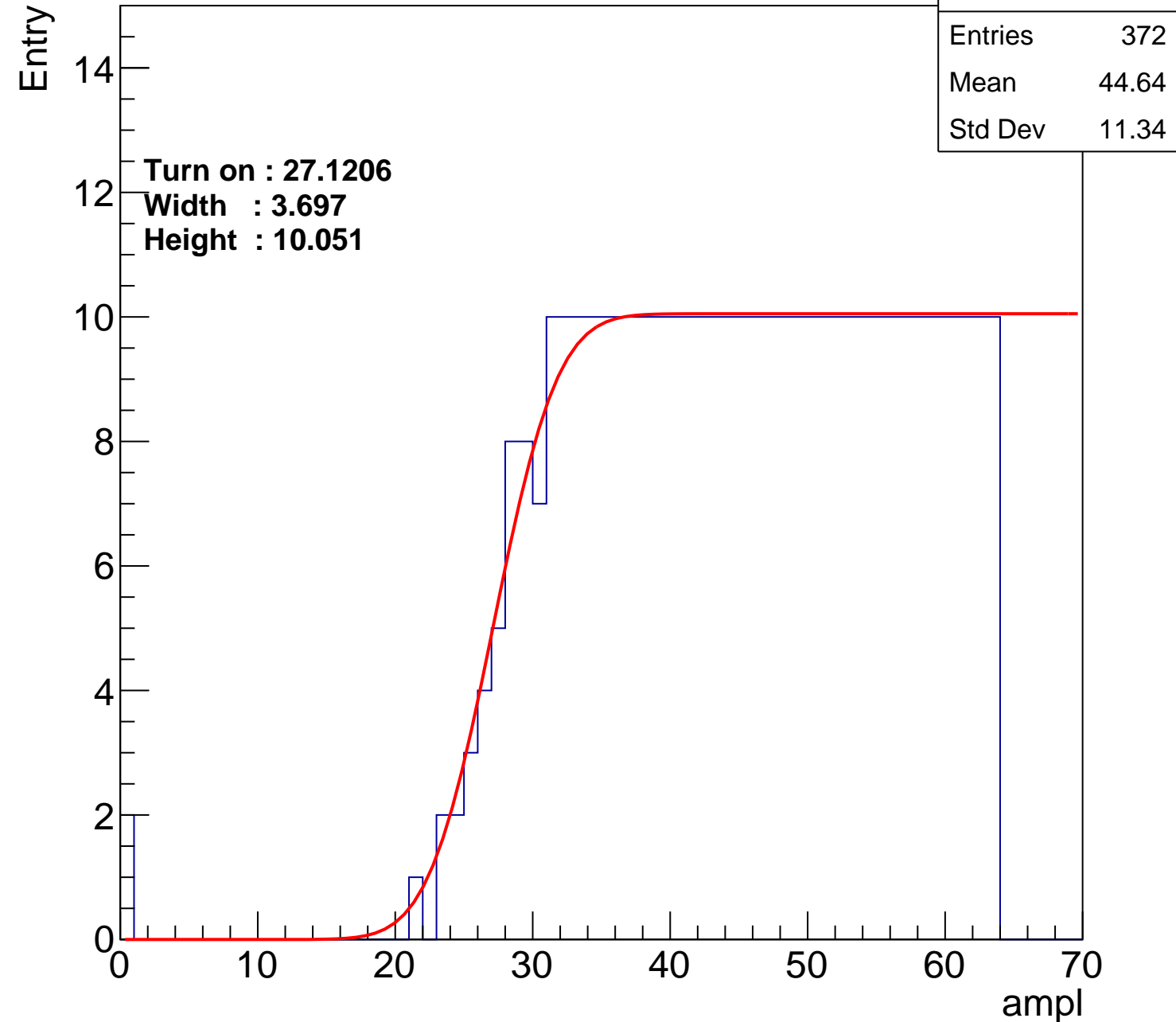
Width : 3.697

Height : 10.051

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch92

calib_packv5_042523_0143.root, FC#0, port D2

Entries	412
Mean	42.57
Std Dev	12.68

Turn on : 23.2564

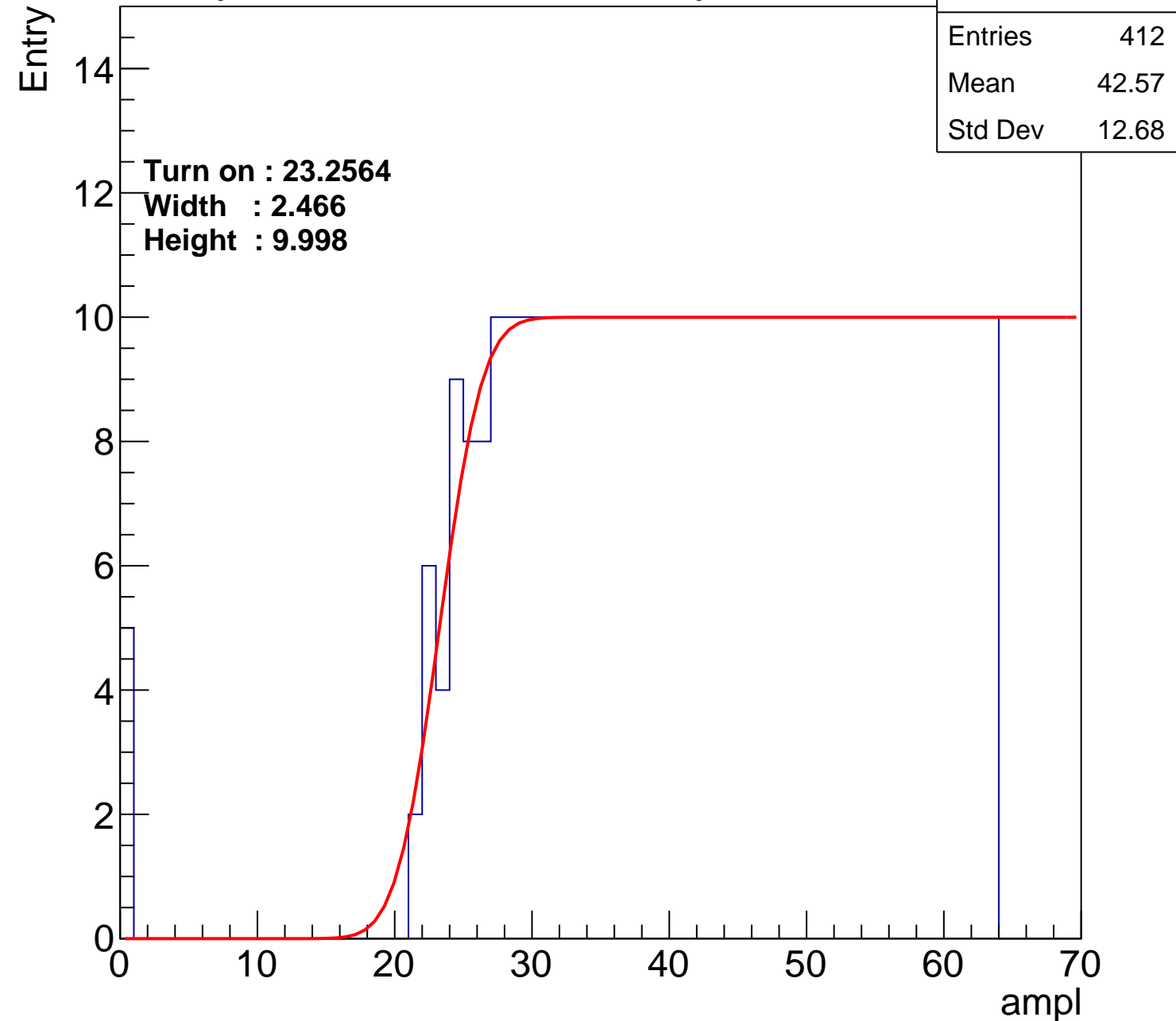
Width : 2.466

Height : 9.998

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch93

calib_packv5_042523_0143.root, FC#0, port D2

Entries	384
Mean	43.94
Std Dev	11.88

Turn on : 25.8945

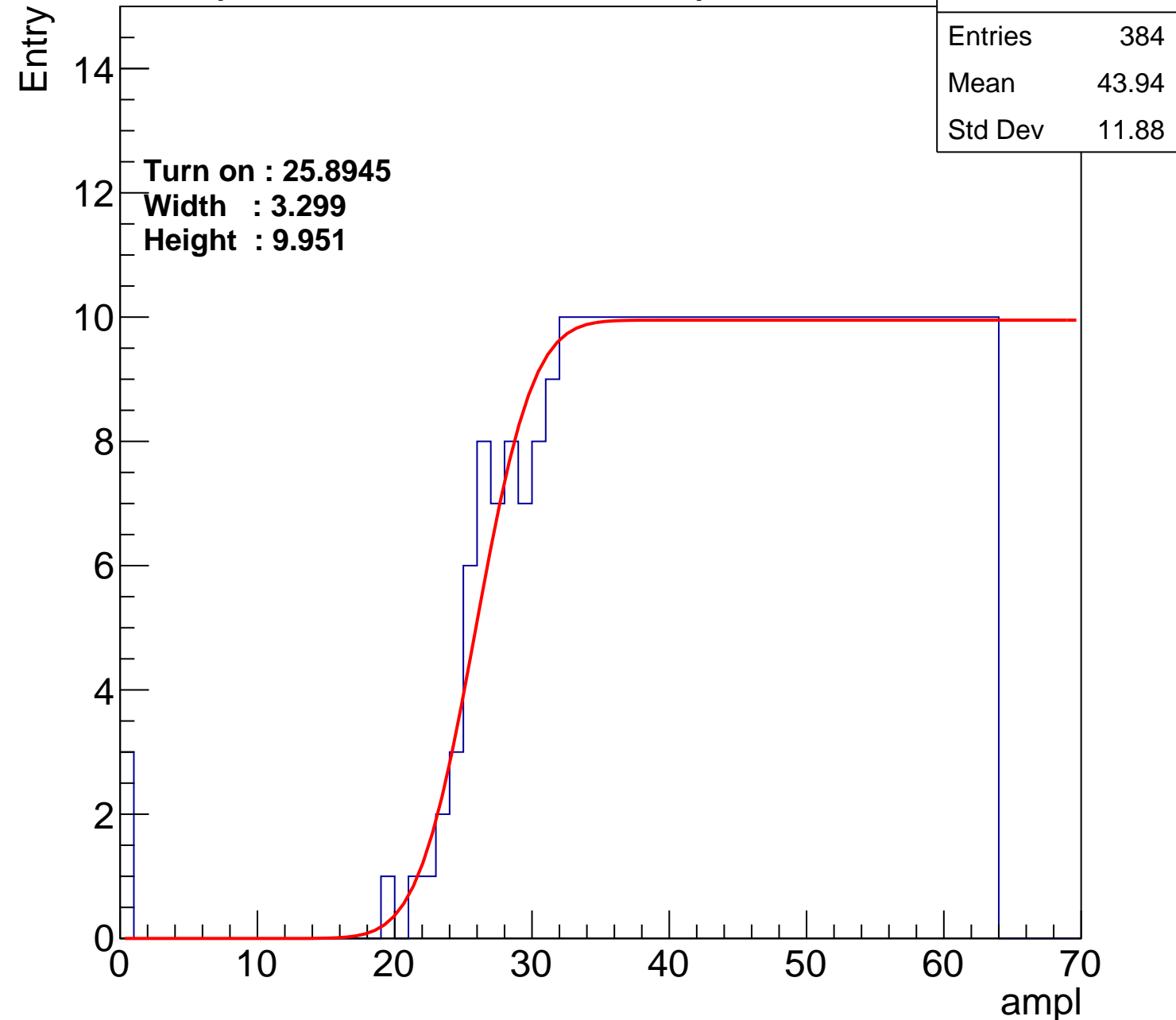
Width : 3.299

Height : 9.951

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch94

calib_packv5_042523_0143.root, FC#0, port D2

Entries	377
Mean	44.06
Std Dev	12.34

Turn on : 28.1790

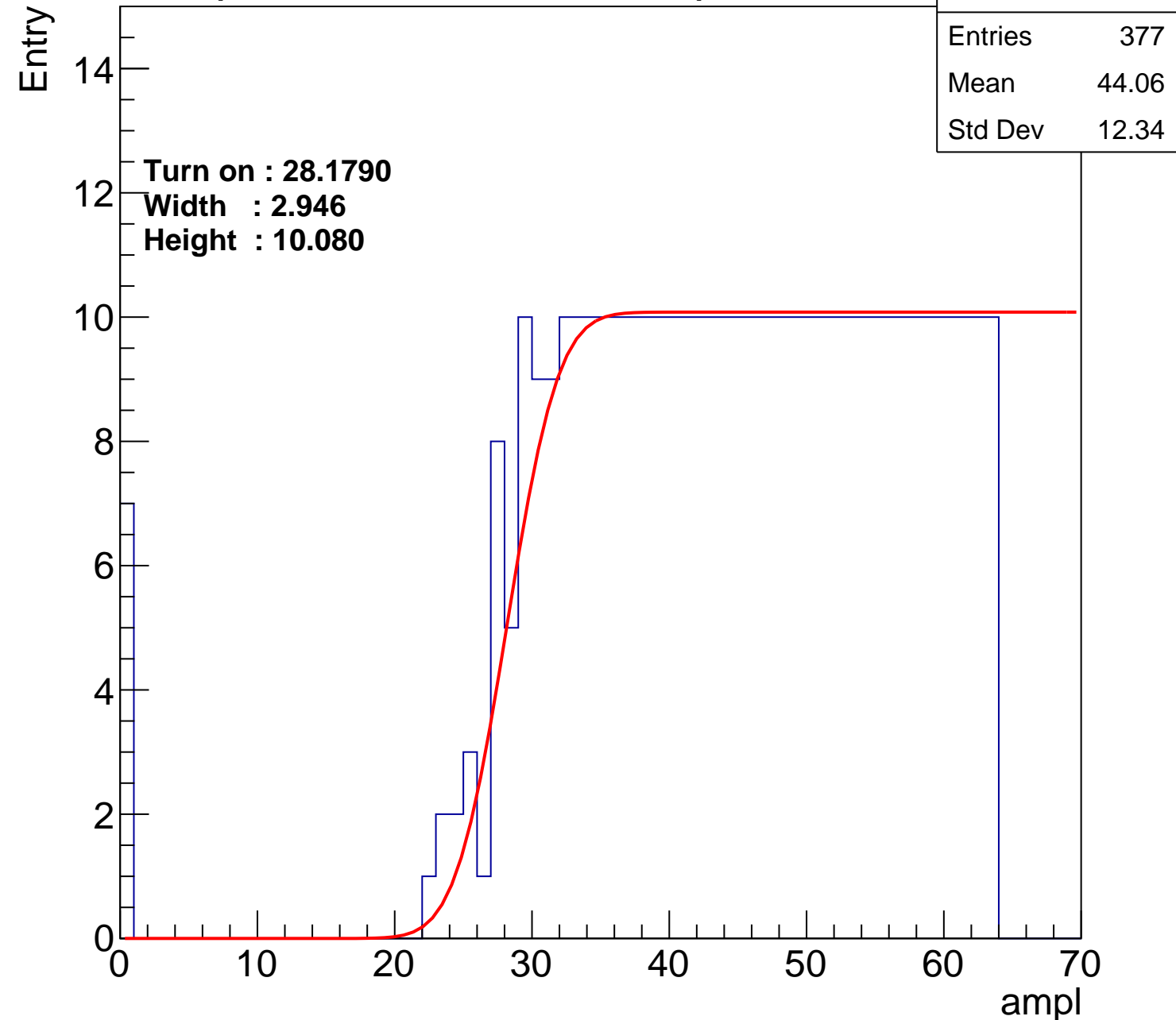
Width : 2.946

Height : 10.080

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch95

calib_packv5_042523_0143.root, FC#0, port D2

Entries	364
Mean	45.05
Std Dev	11.11

Turn on : 28.1909

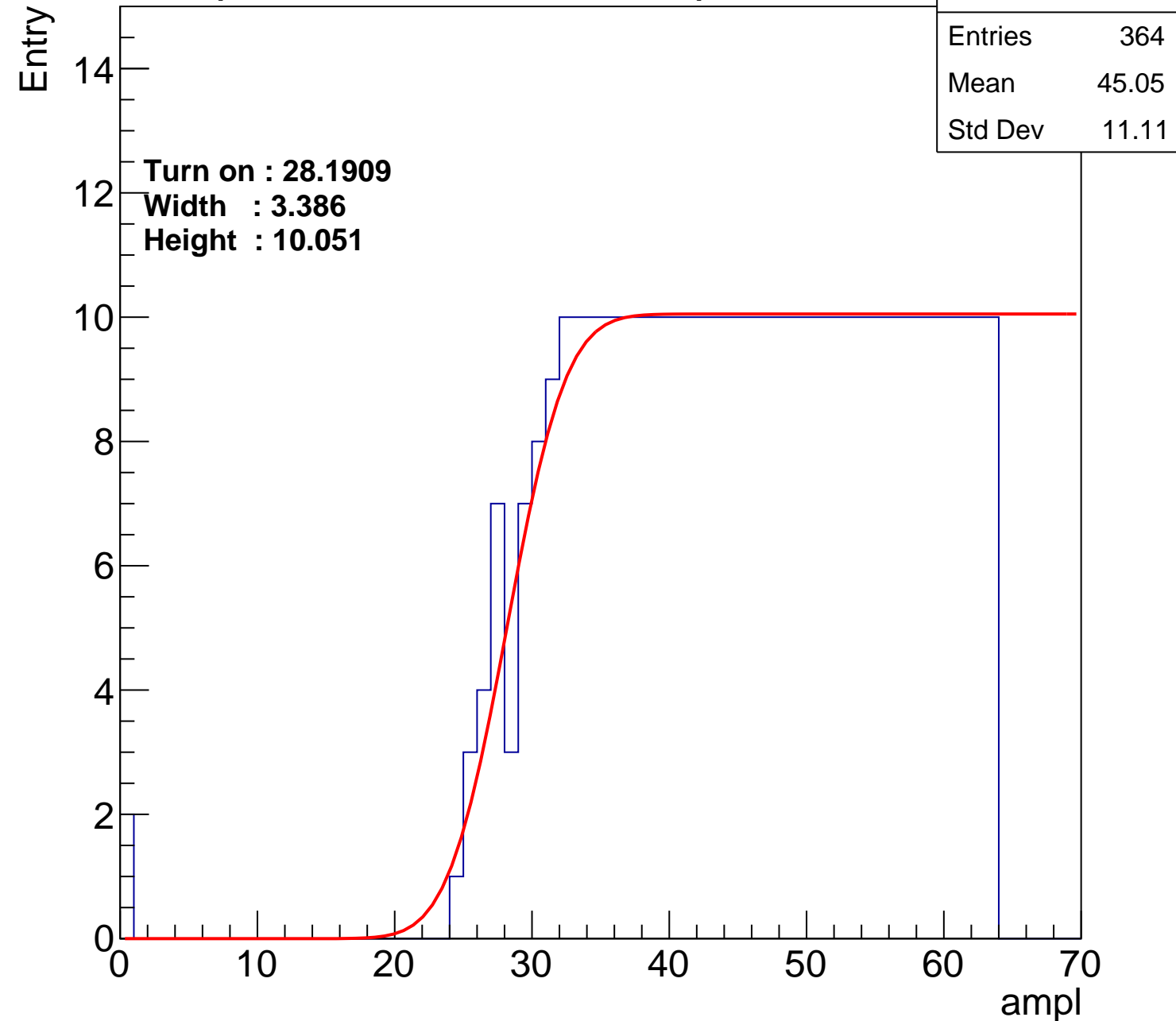
Width : 3.386

Height : 10.051

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch96

calib_packv5_042523_0143.root, FC#0, port D2

Entries	384
Mean	43.79
Std Dev	12.33

Turn on : 27.9646

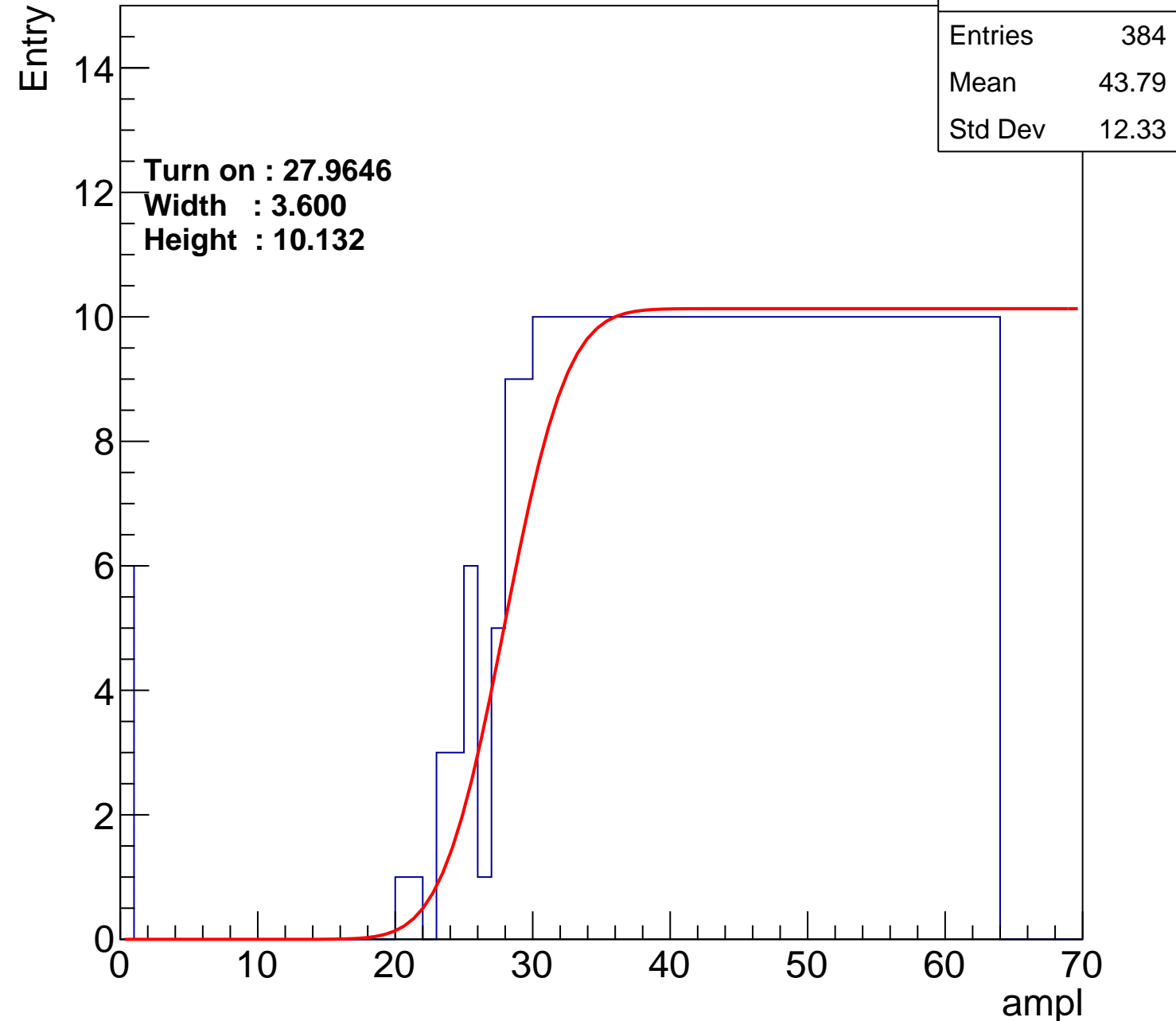
Width : 3.600

Height : 10.132

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch97

calib_packv5_042523_0143.root, FC#0, port D2

Entries	392
Mean	43.69
Std Dev	11.8

Turn on : 24.9617

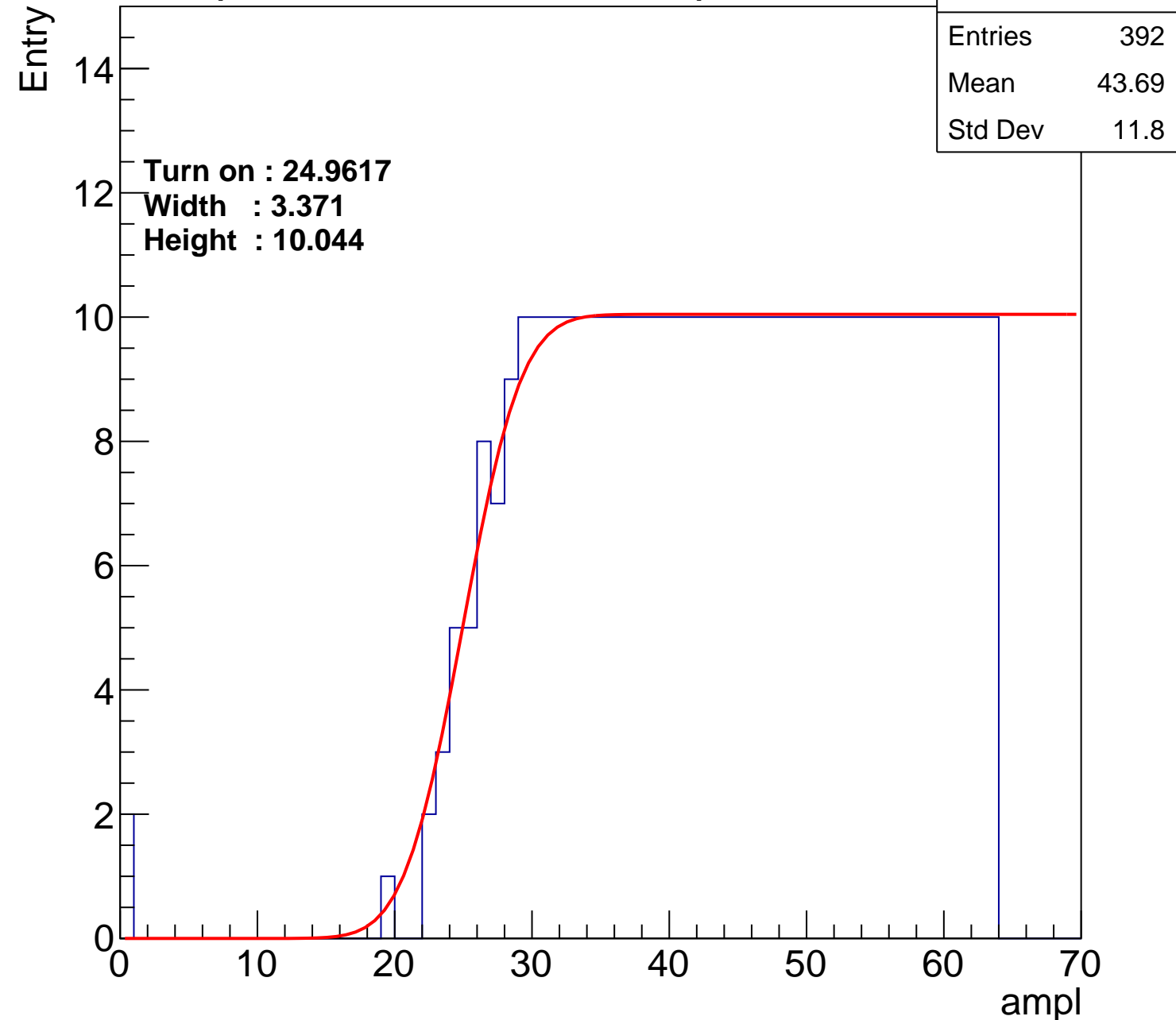
Width : 3.371

Height : 10.044

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch98

calib_packv5_042523_0143.root, FC#0, port D2

Entries	391
Mean	43.79
Std Dev	11.63

Turn on : 25.1187

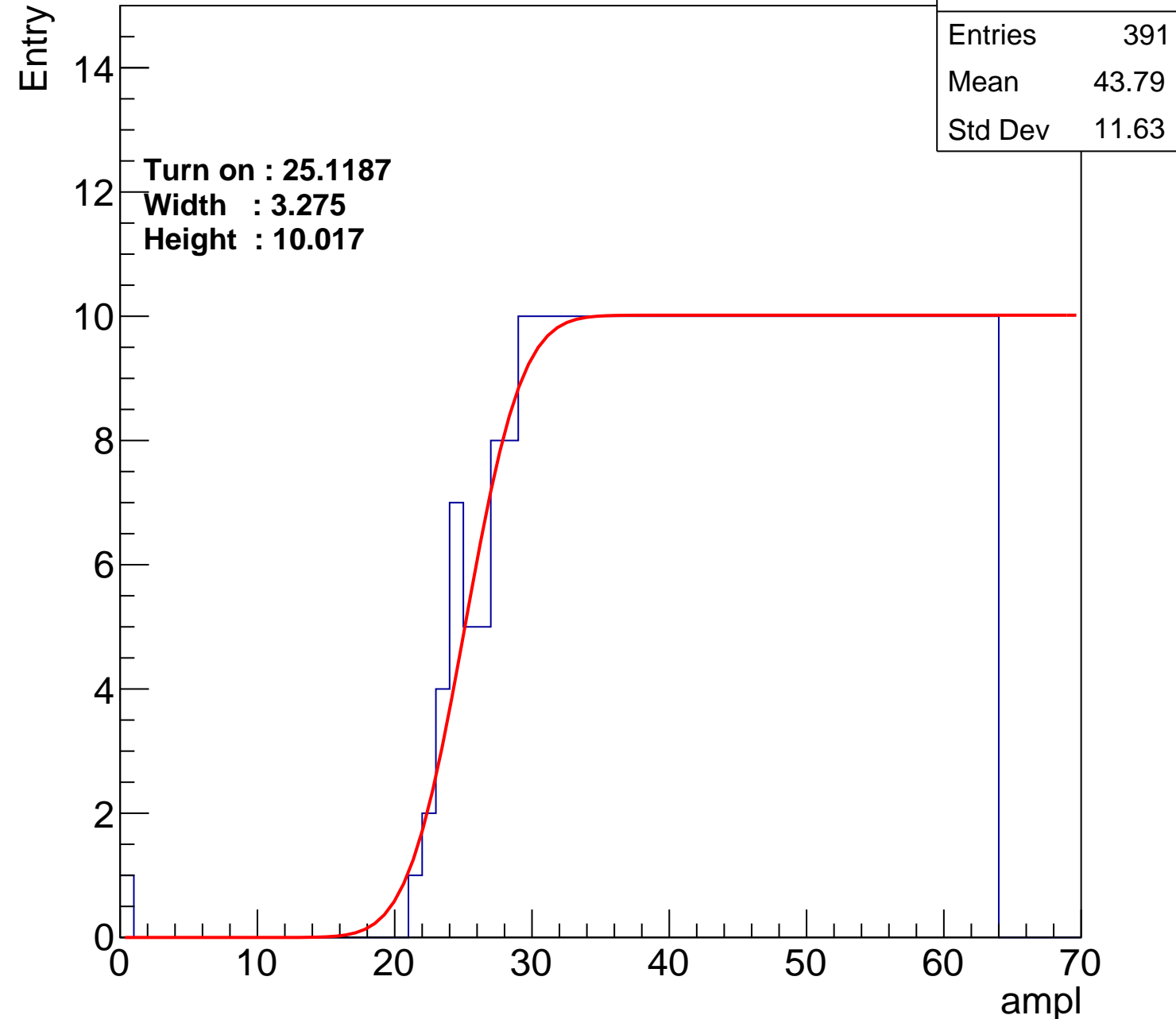
Width : 3.275

Height : 10.017

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch99

calib_packv5_042523_0143.root, FC#0, port D2

Entries	367
Mean	44.78
Std Dev	11.46

Turn on : 27.7165

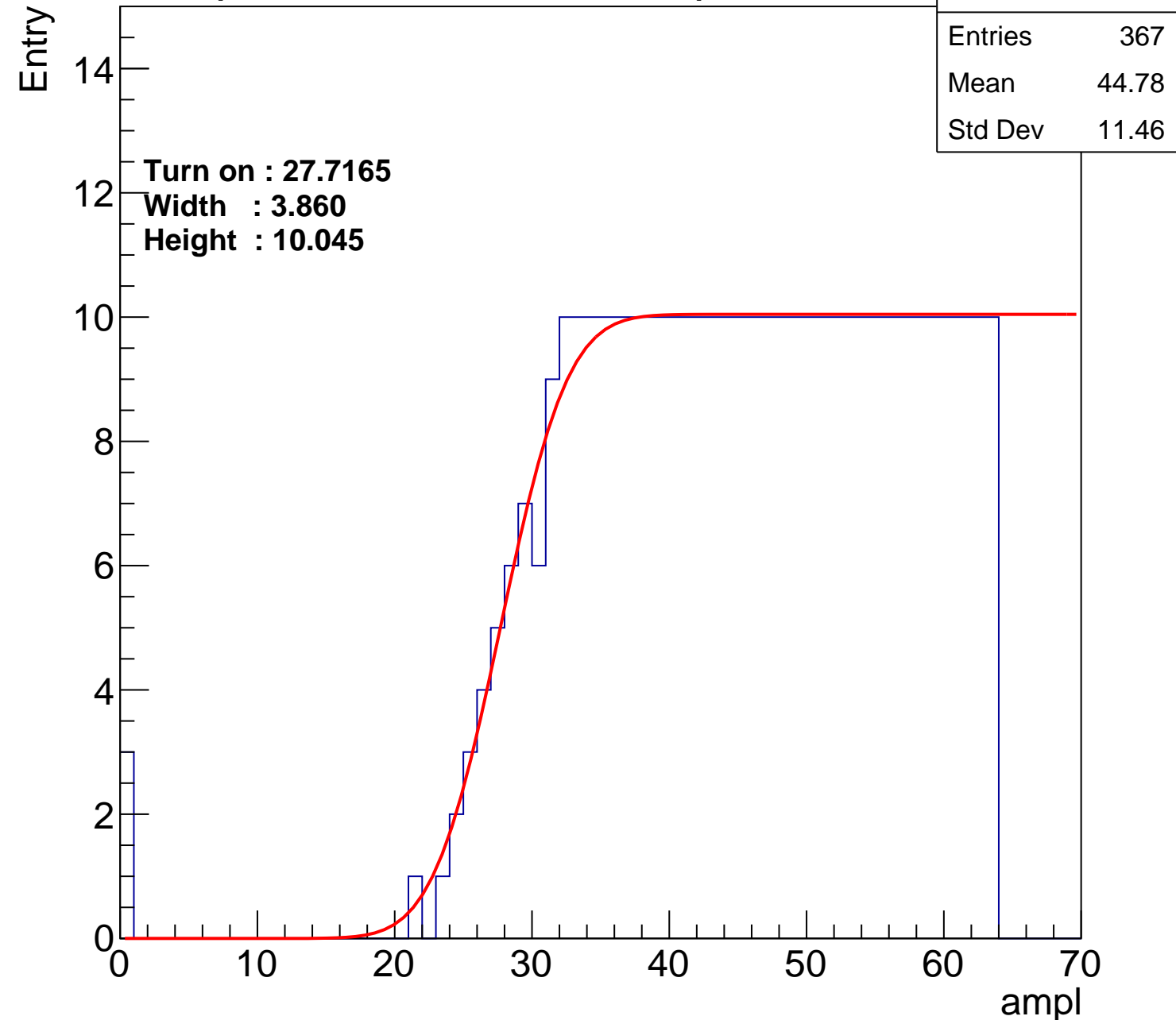
Width : 3.860

Height : 10.045

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch100

calib_packv5_042523_0143.root, FC#0, port D2

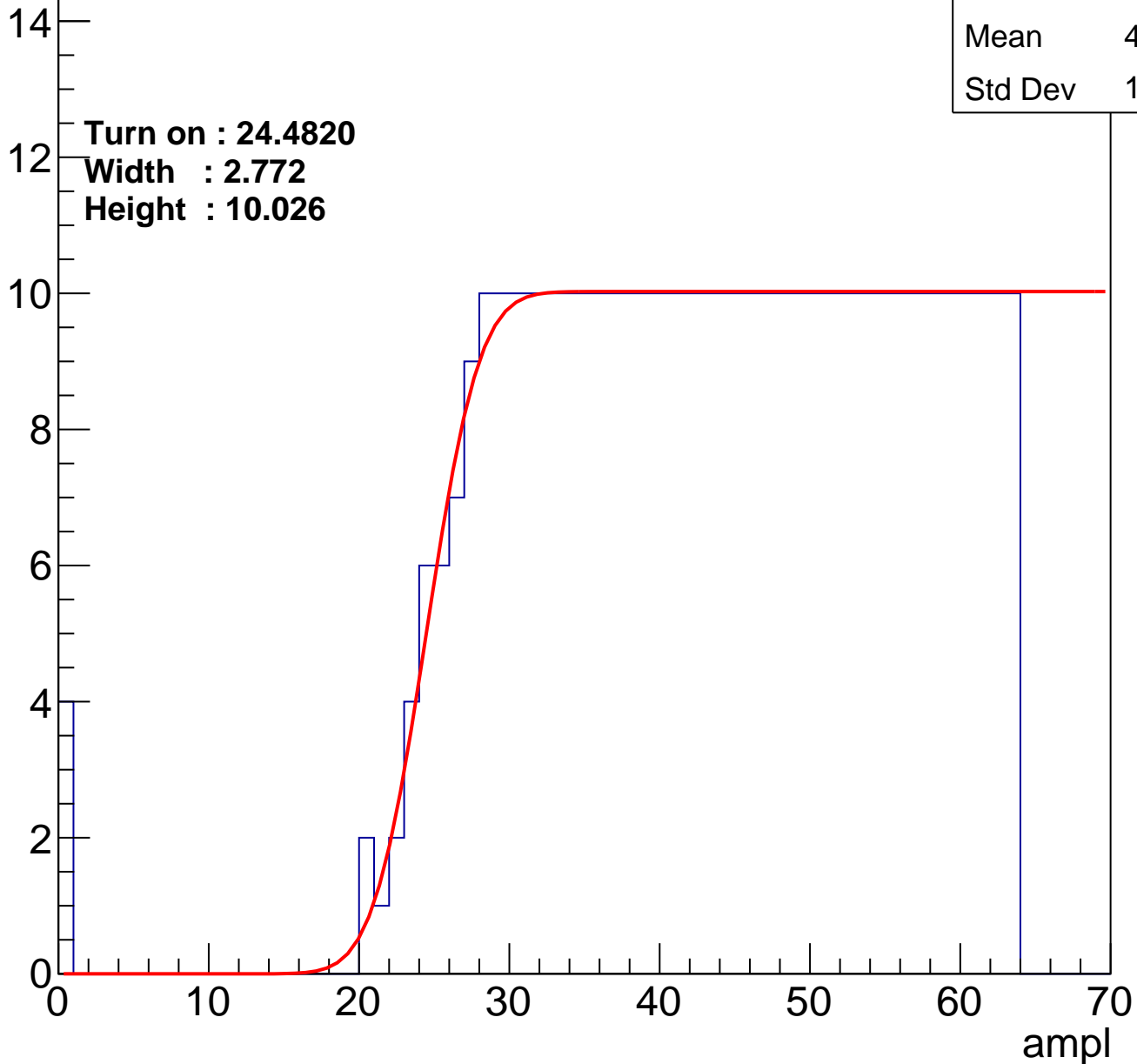
Entries	401
Mean	43.13
Std Dev	12.33

Turn on : 24.4820

Width : 2.772

Height : 10.026

Entry



B1L101S, U8-ch101

calib_packv5_042523_0143.root, FC#0, port D2

Entries	375
Mean	44.59
Std Dev	11.17

Turn on : 26.9467

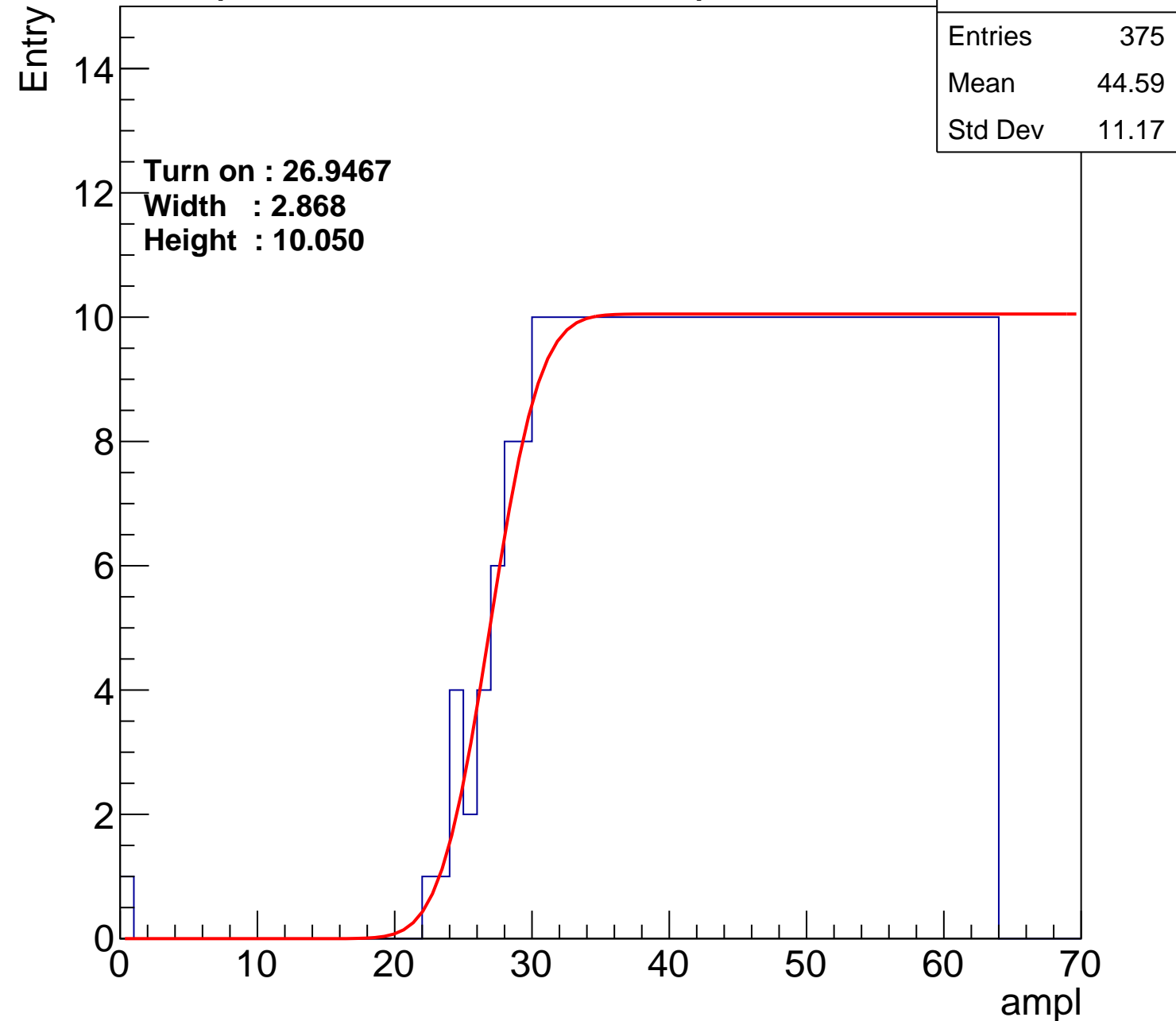
Width : 2.868

Height : 10.050

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch102

calib_packv5_042523_0143.root, FC#0, port D2

Entries	376
Mean	44.25
Std Dev	11.97

Turn on : 26.8407

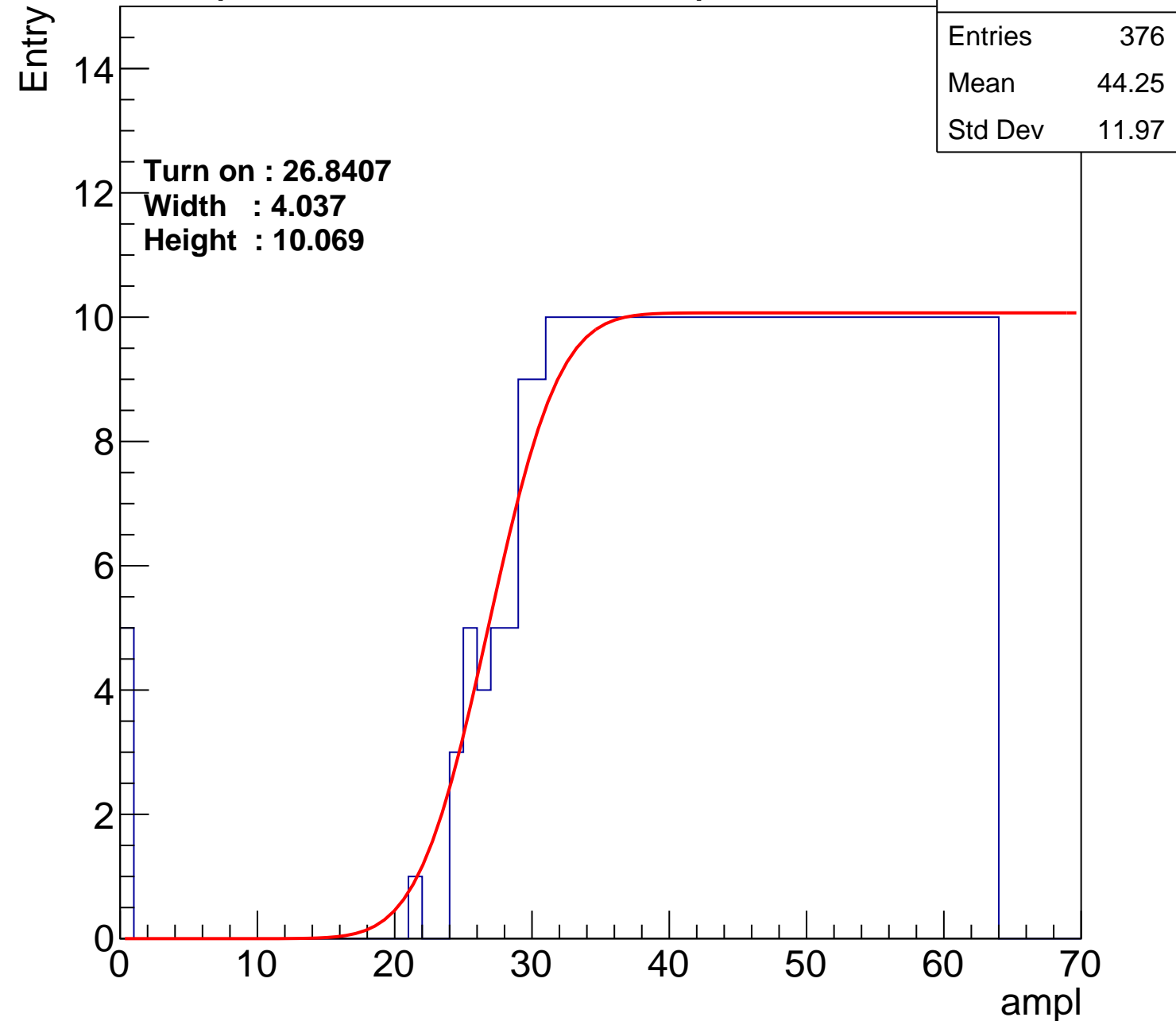
Width : 4.037

Height : 10.069

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch103

calib_packv5_042523_0143.root, FC#0, port D2

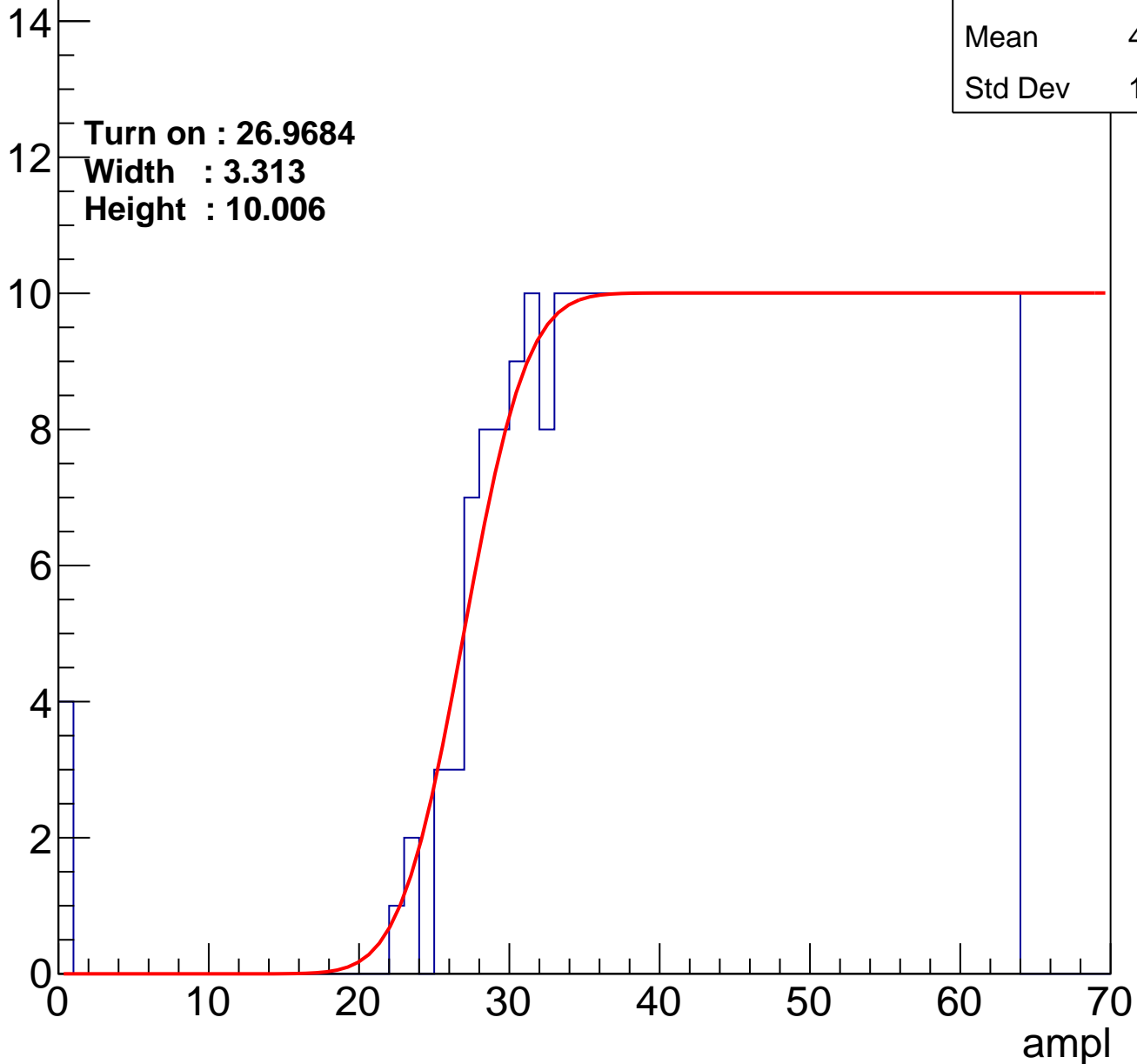
Entries	373
Mean	44.46
Std Dev	11.73

Turn on : 26.9684

Width : 3.313

Height : 10.006

Entry



B1L101S, U8-ch104

calib_packv5_042523_0143.root, FC#0, port D2

Entries	403
Mean	43.2
Std Dev	11.93

Turn on : 23.8330

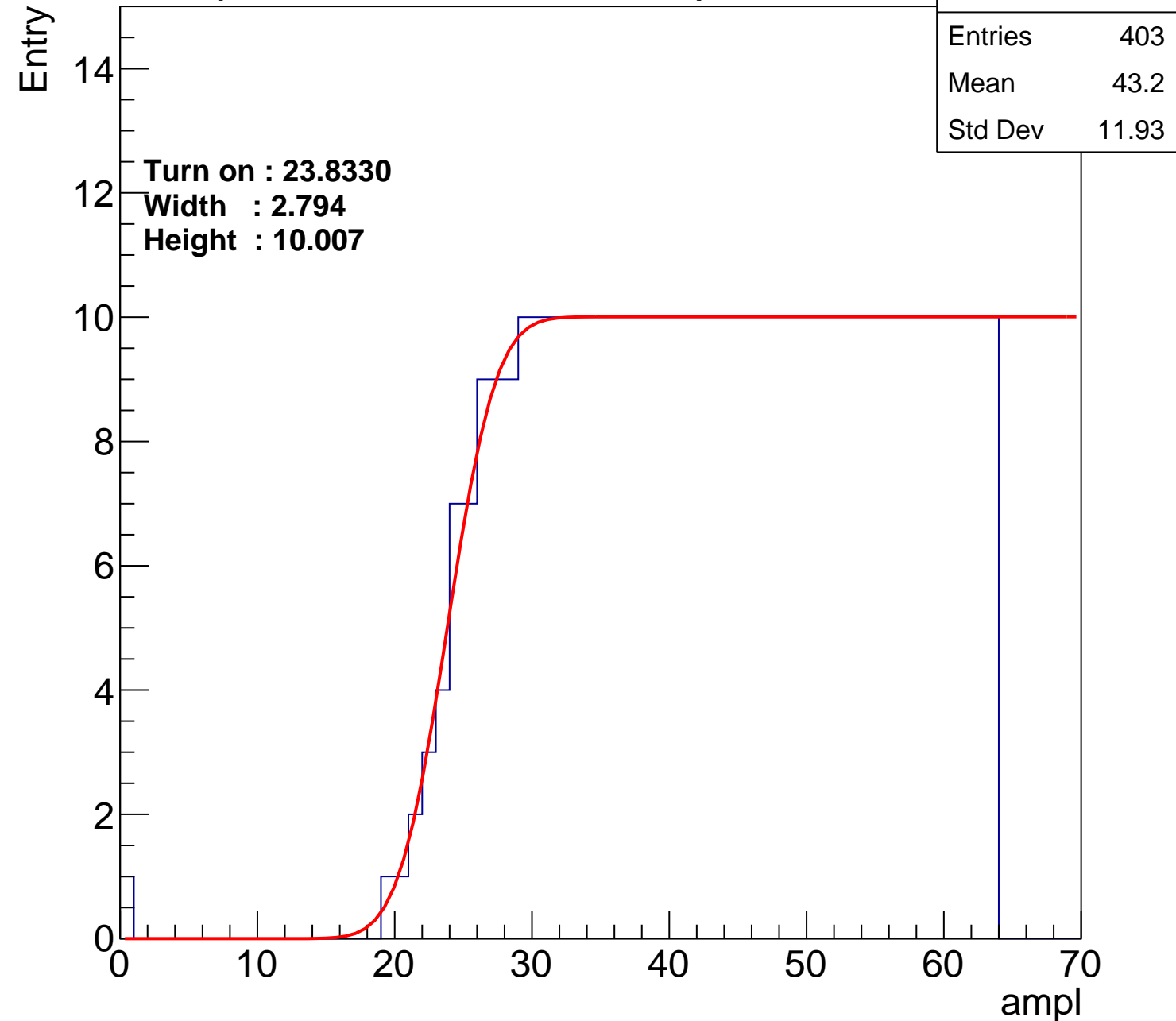
Width : 2.794

Height : 10.007

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch105

calib_packv5_042523_0143.root, FC#0, port D2

Entries	368
Mean	44.95
Std Dev	10.97

Turn on : 27.6585

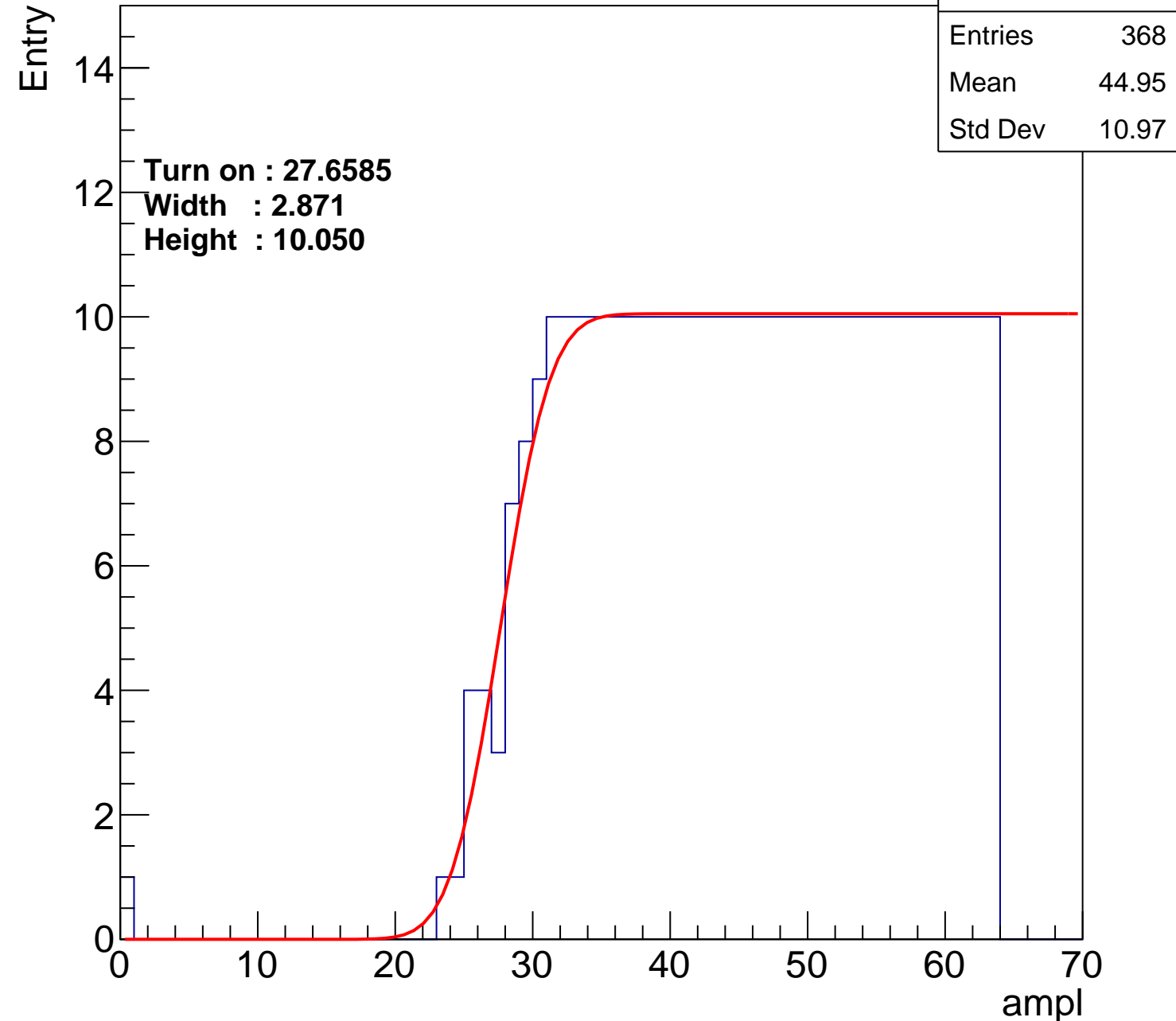
Width : 2.871

Height : 10.050

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch106

calib_packv5_042523_0143.root, FC#0, port D2

Entries	372
Mean	44.52
Std Dev	11.7

Turn on : 27.5181

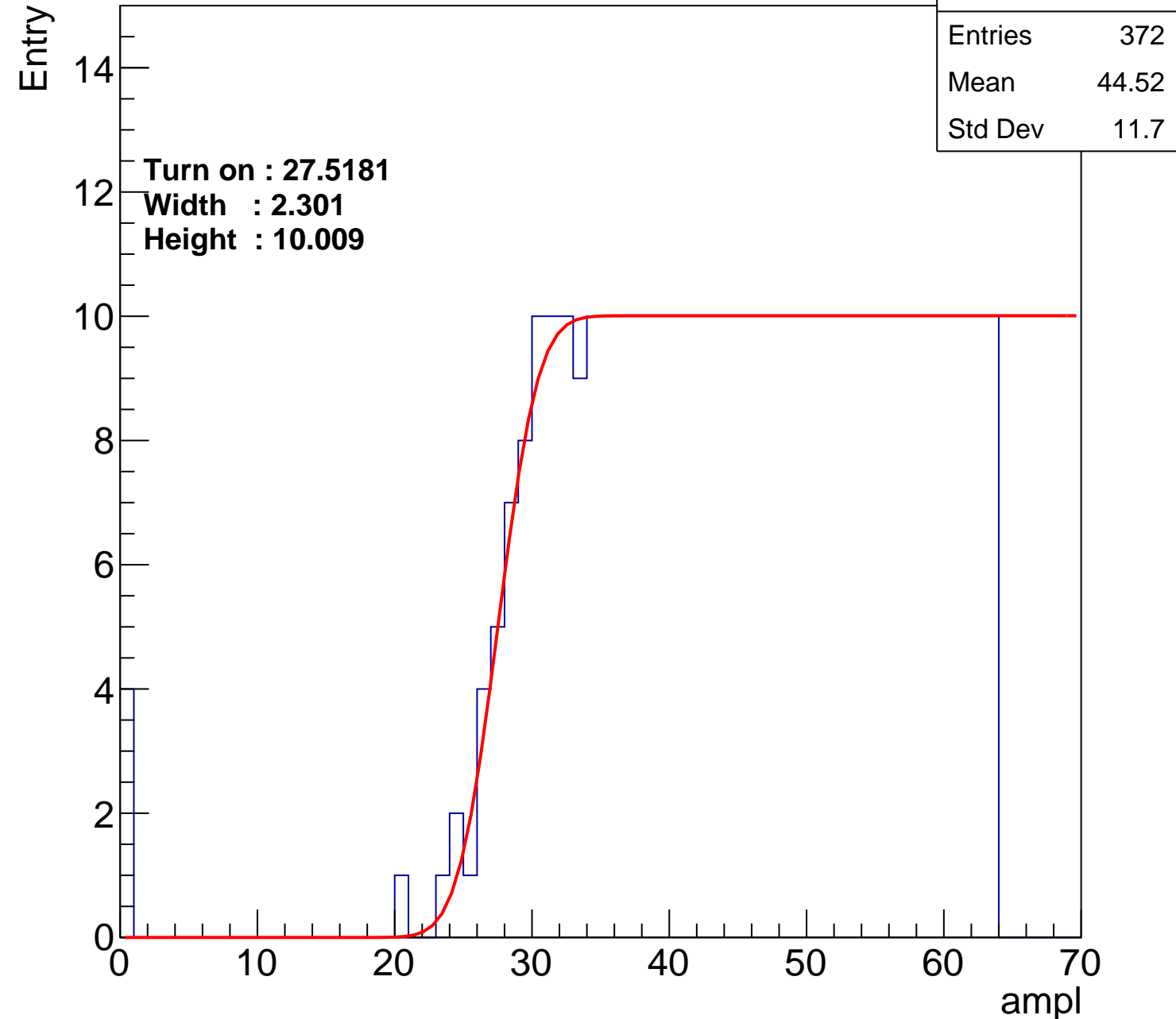
Width : 2.301

Height : 10.009

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch107

calib_packv5_042523_0143.root, FC#0, port D2

Entries	370
Mean	44.81
Std Dev	11.09

Turn on : 26.4410

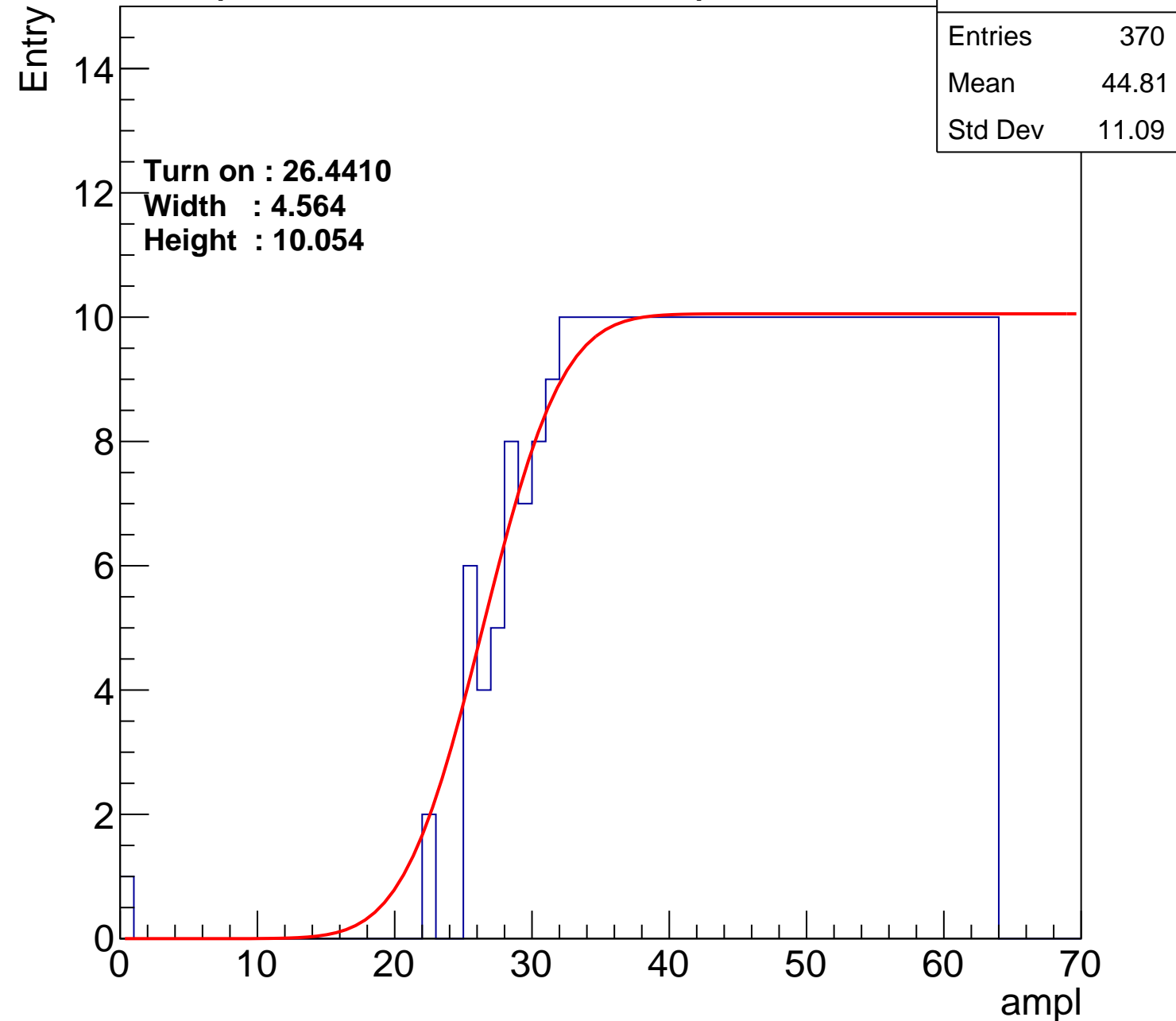
Width : 4.564

Height : 10.054

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch108

calib_packv5_042523_0143.root, FC#0, port D2

Entries	400
Mean	43.14
Std Dev	12.42

Turn on : 24.0095

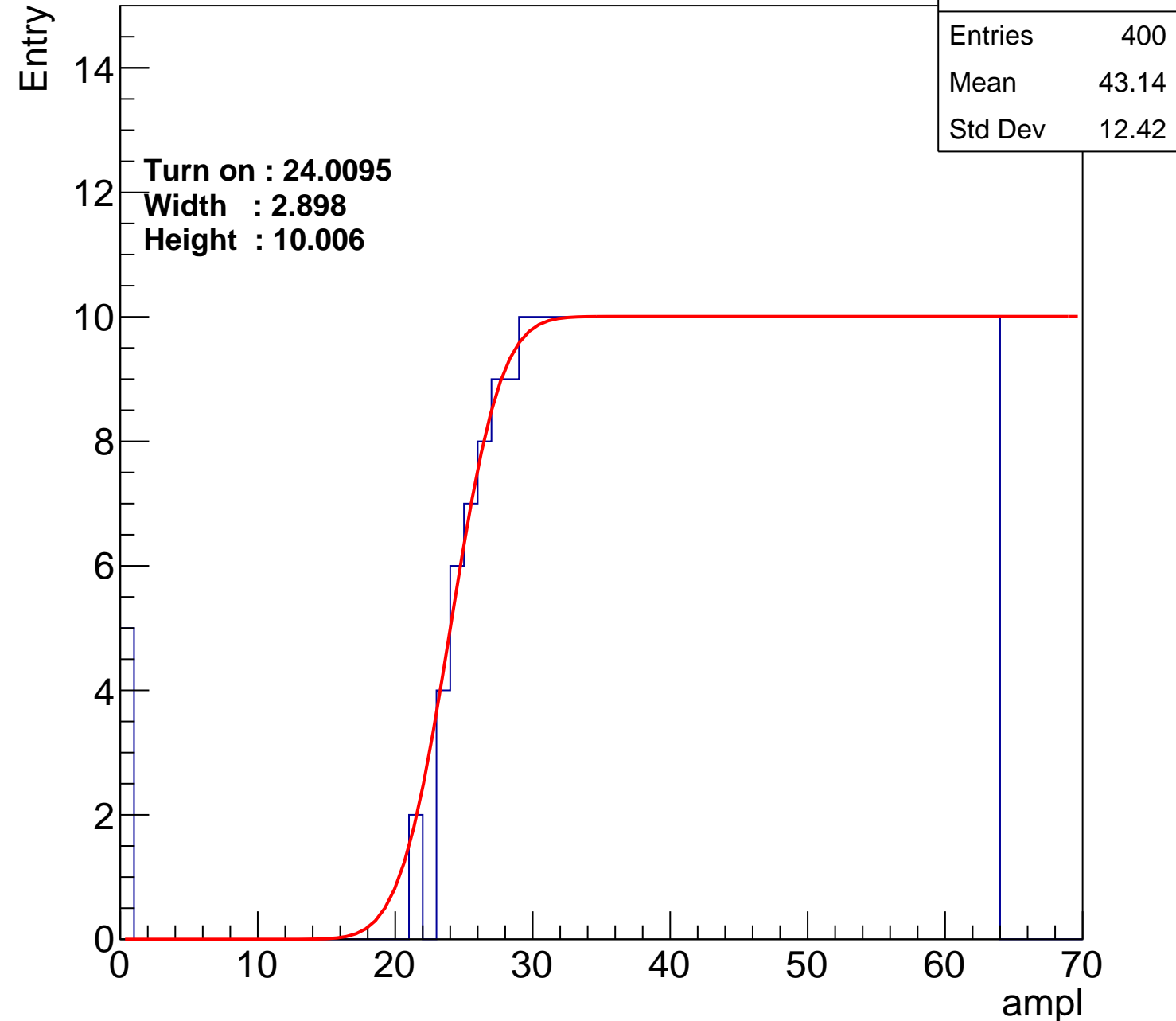
Width : 2.898

Height : 10.006

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch109

calib_packv5_042523_0143.root, FC#0, port D2

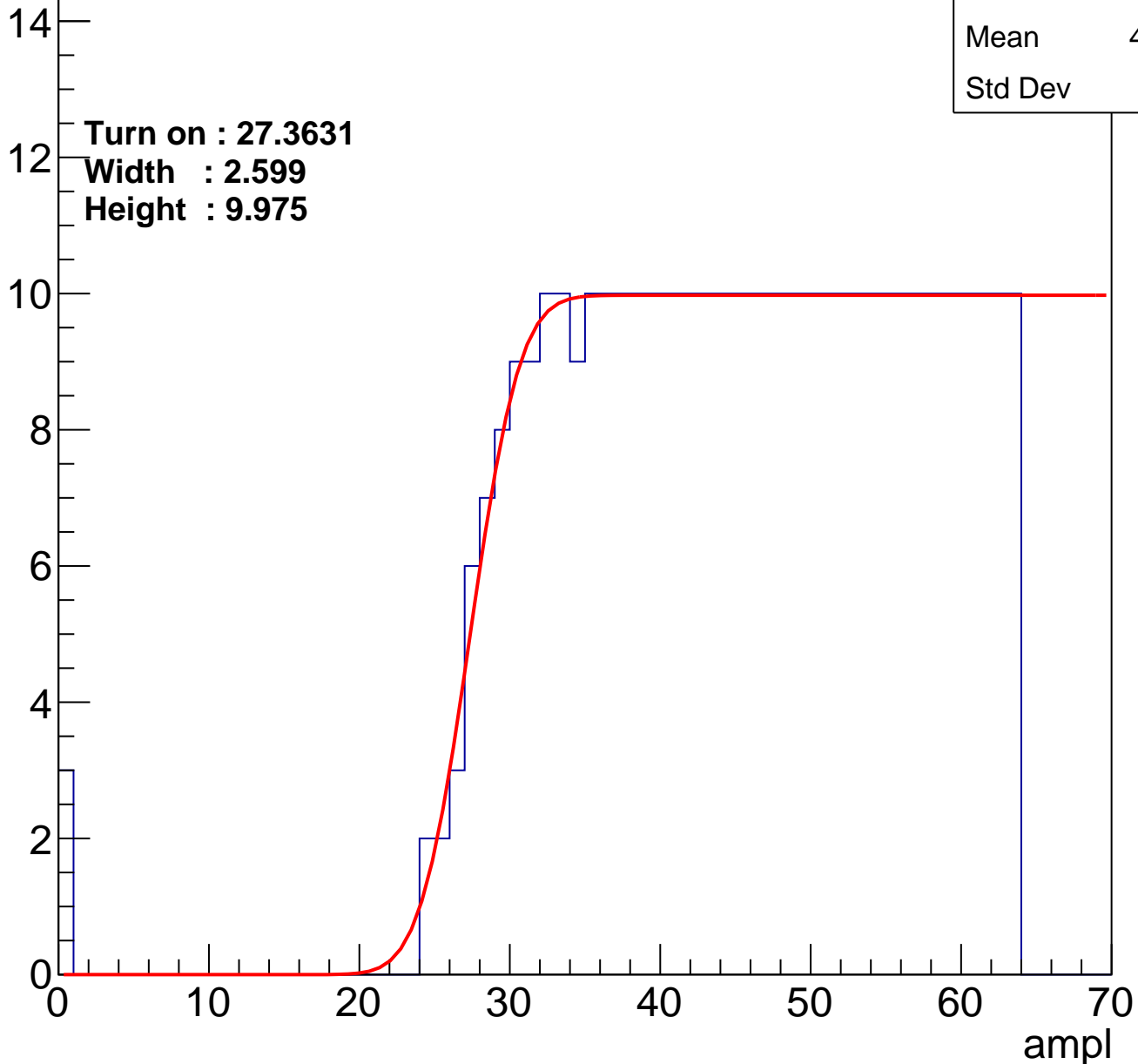
Entries	368
Mean	44.79
Std Dev	11.4

Turn on : 27.3631

Width : 2.599

Height : 9.975

Entry



B1L101S, U8-ch110

calib_packv5_042523_0143.root, FC#0, port D2

Entries	375
Mean	44.3
Std Dev	11.95

Turn on : 27.2309

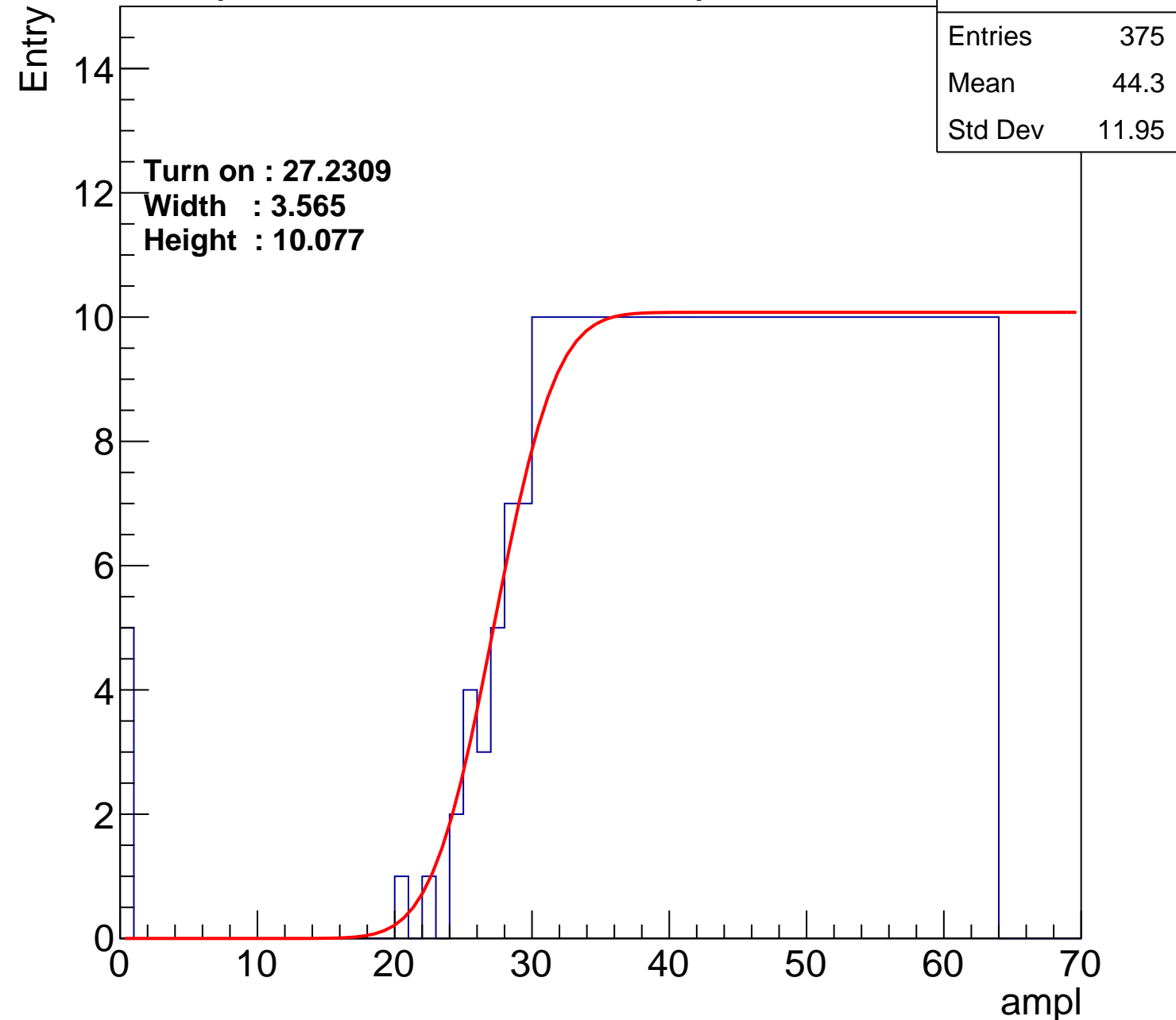
Width : 3.565

Height : 10.077

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch111

calib_packv5_042523_0143.root, FC#0, port D2

Entries	365
Mean	44.99
Std Dev	11.14

Turn on : 27.2760

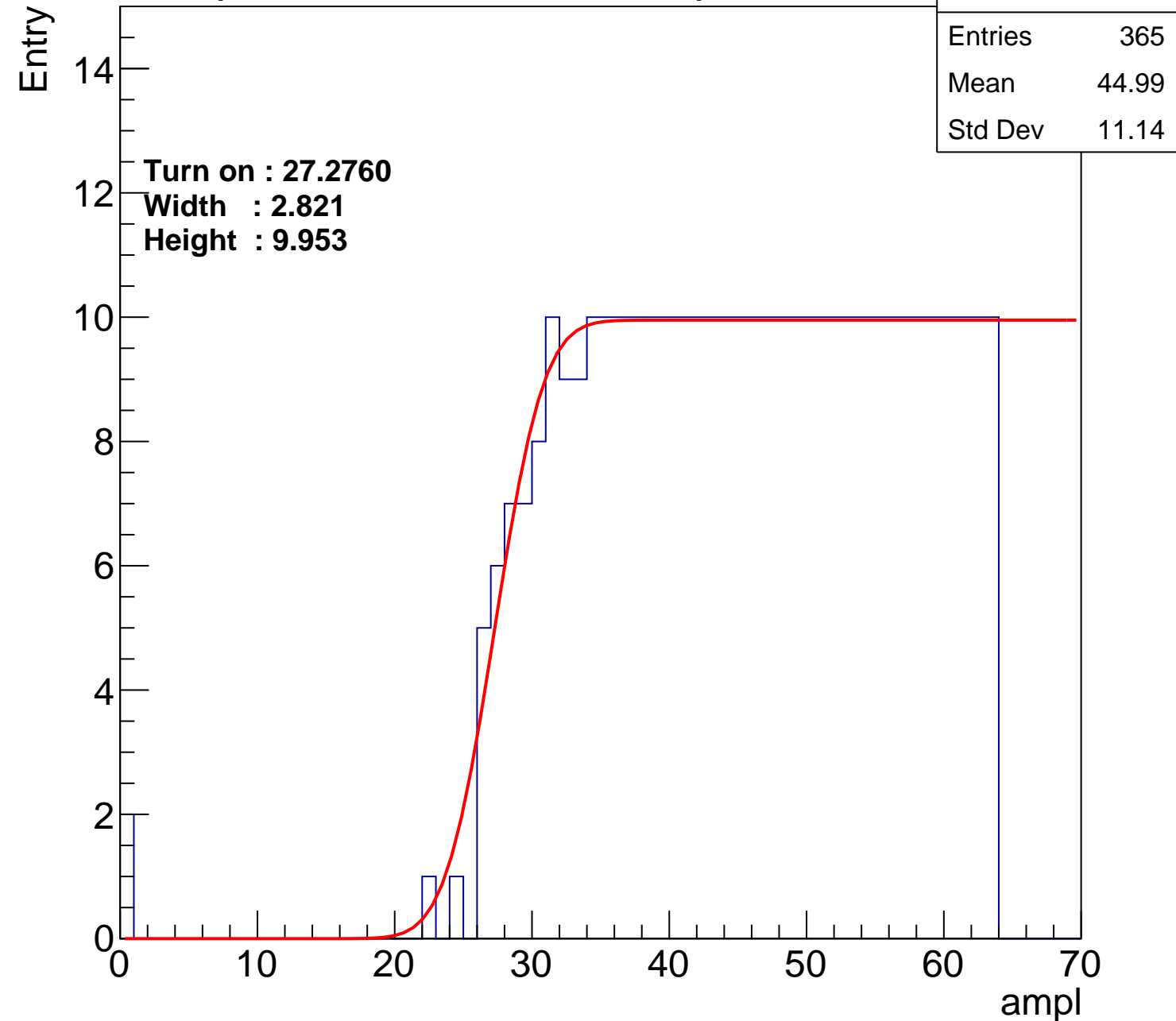
Width : 2.821

Height : 9.953

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch112

calib_packv5_042523_0143.root, FC#0, port D2

Entries	389
Mean	43.84
Std Dev	11.71

Turn on : 25.4847

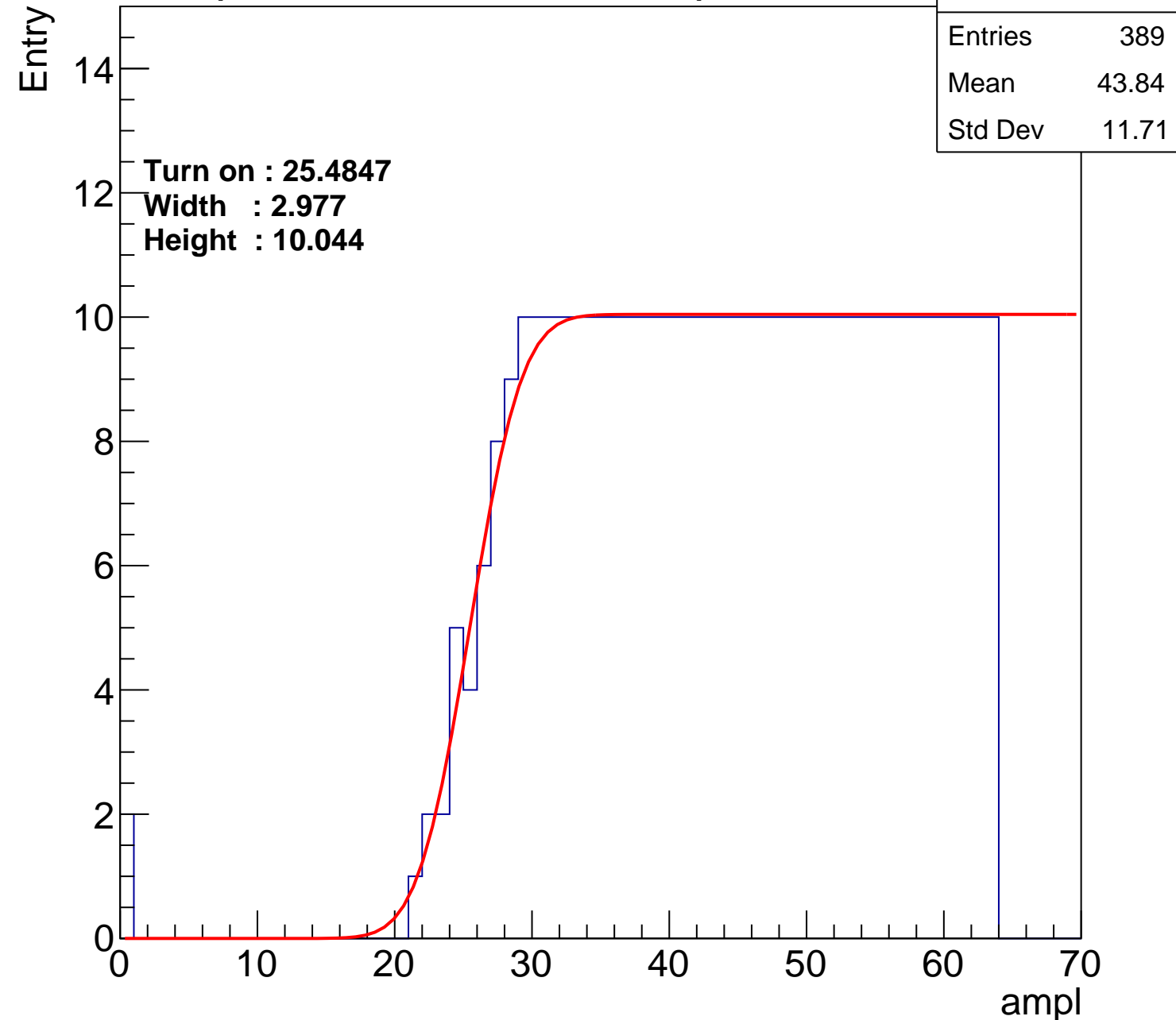
Width : 2.977

Height : 10.044

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch113

calib_packv5_042523_0143.root, FC#0, port D2

Entries	373
Mean	44.57
Std Dev	11.39

Turn on : 27.1147

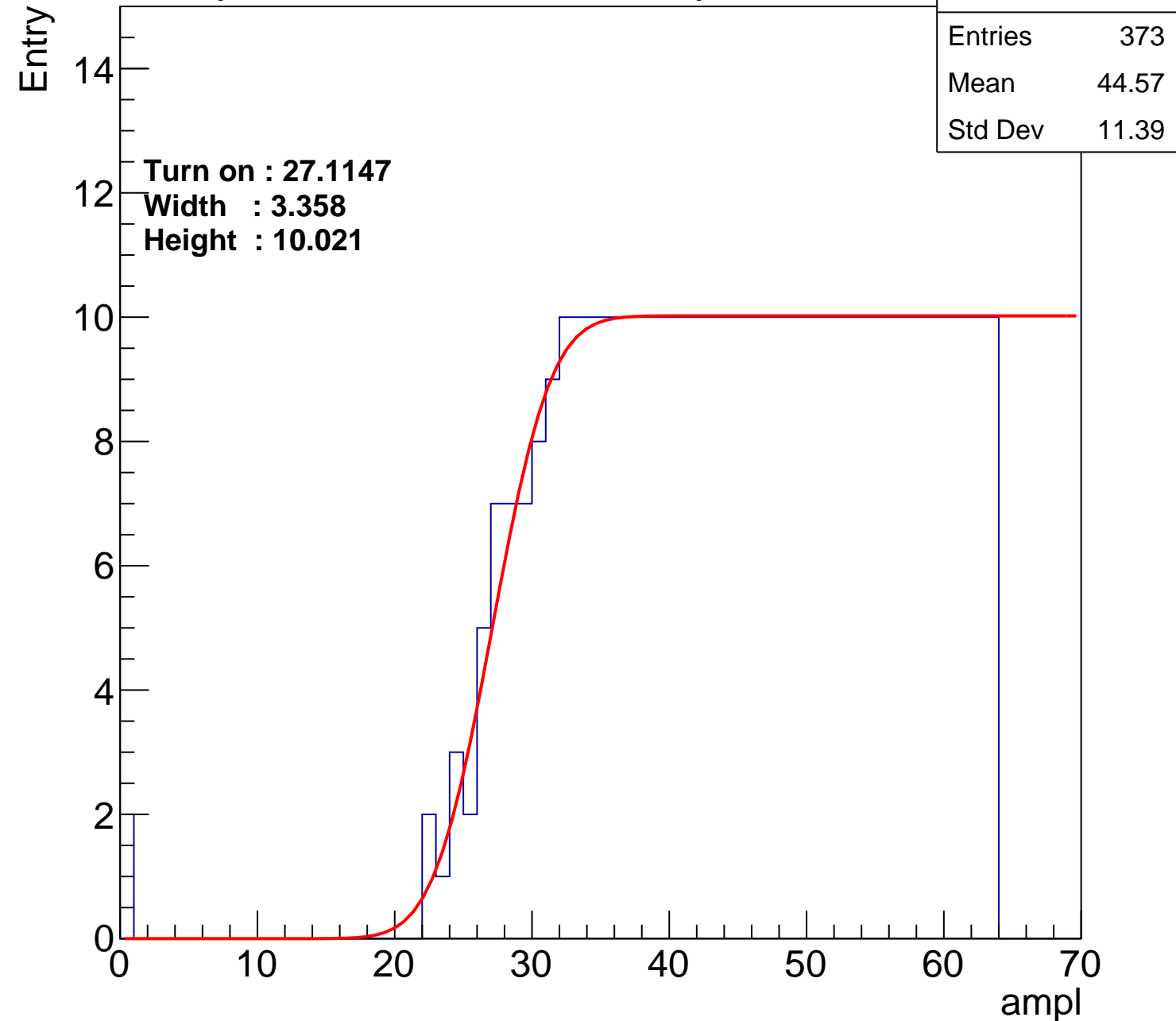
Width : 3.358

Height : 10.021

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch114

calib_packv5_042523_0143.root, FC#0, port D2

Entries	380
Mean	44.13
Std Dev	11.88

Turn on : 26.6299

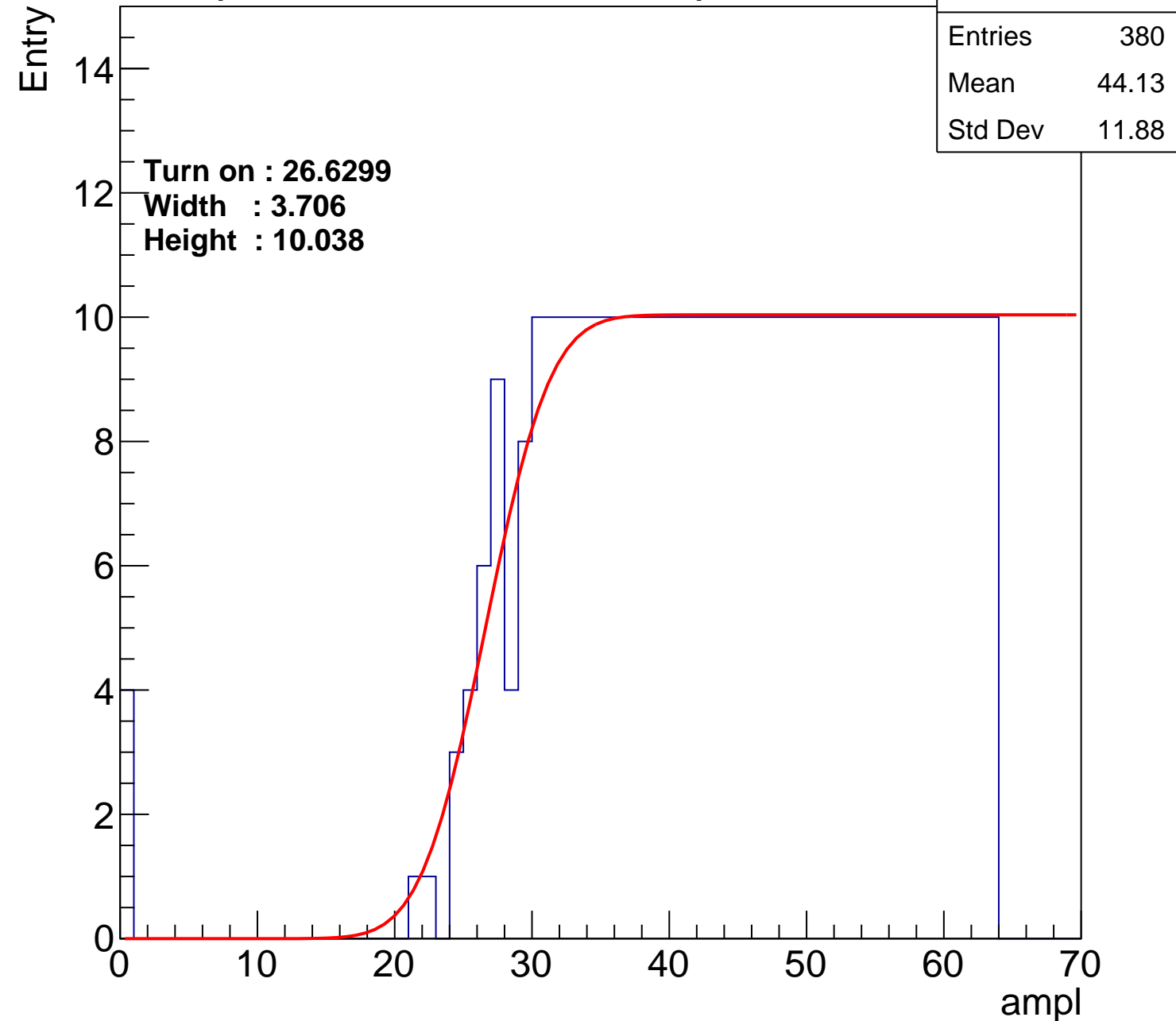
Width : 3.706

Height : 10.038

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch115

calib_packv5_042523_0143.root, FC#0, port D2

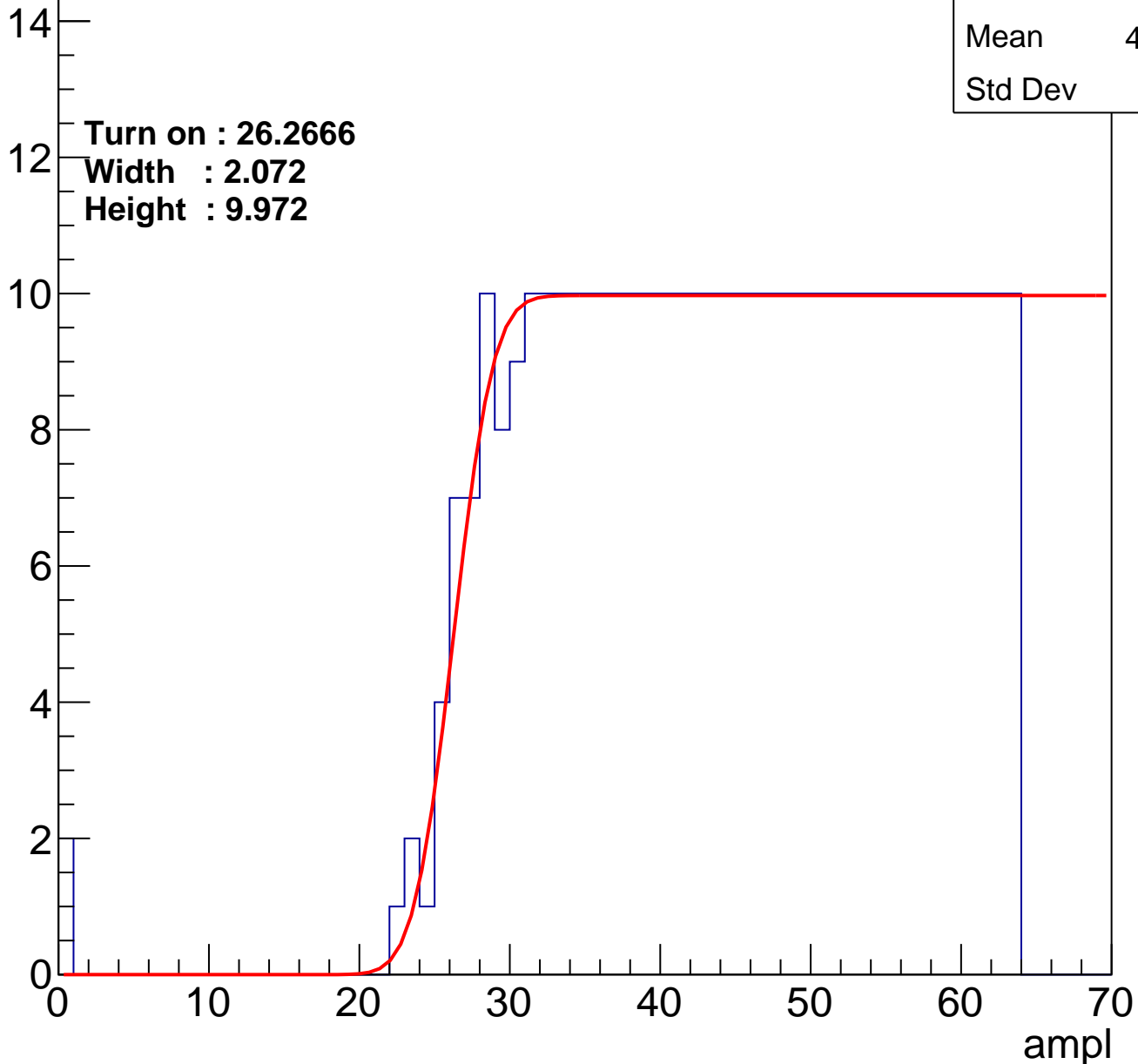
Entries	381
Mean	44.24
Std Dev	11.5

Turn on : 26.2666

Width : 2.072

Height : 9.972

Entry



B1L101S, U8-ch116

calib_packv5_042523_0143.root, FC#0, port D2

Entries	399
Mean	43.41
Std Dev	11.81

Turn on : 24.1948

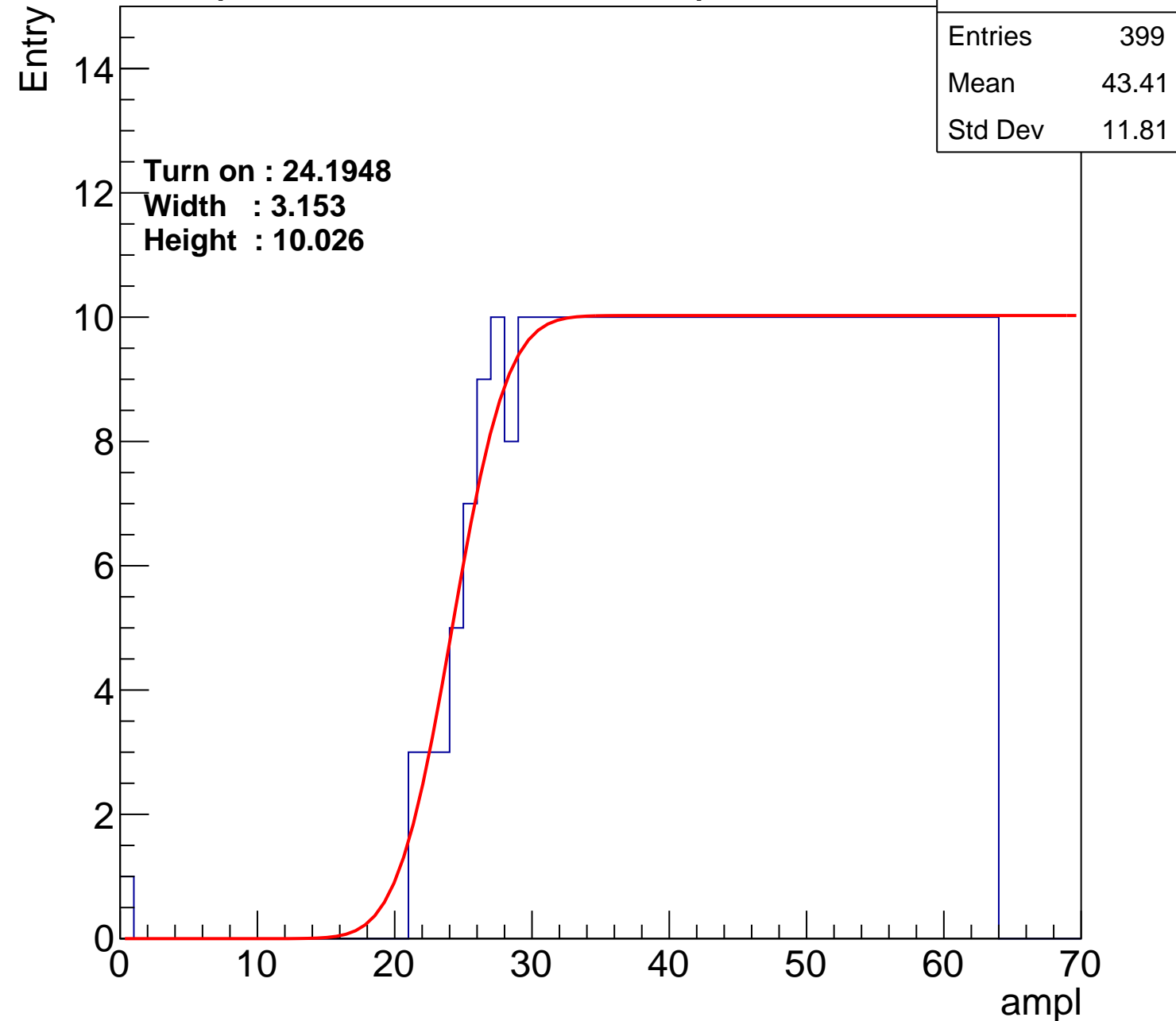
Width : 3.153

Height : 10.026

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch117

calib_packv5_042523_0143.root, FC#0, port D2

Entries	378
Mean	44.31
Std Dev	11.68

Turn on : 27.3836

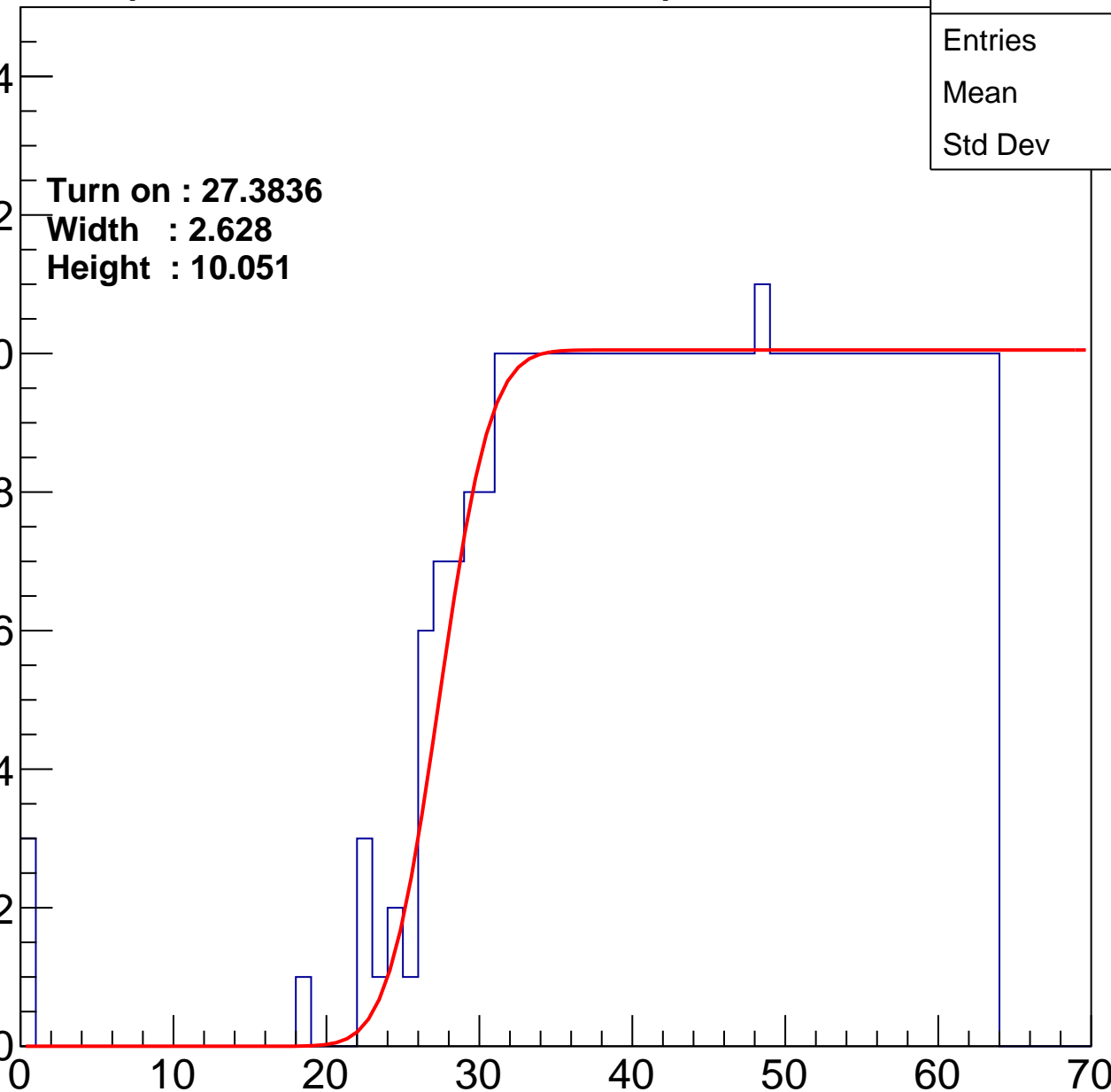
Width : 2.628

Height : 10.051

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch118

calib_packv5_042523_0143.root, FC#0, port D2

Entries	368
Mean	44.74
Std Dev	11.56

Turn on : 27.8578

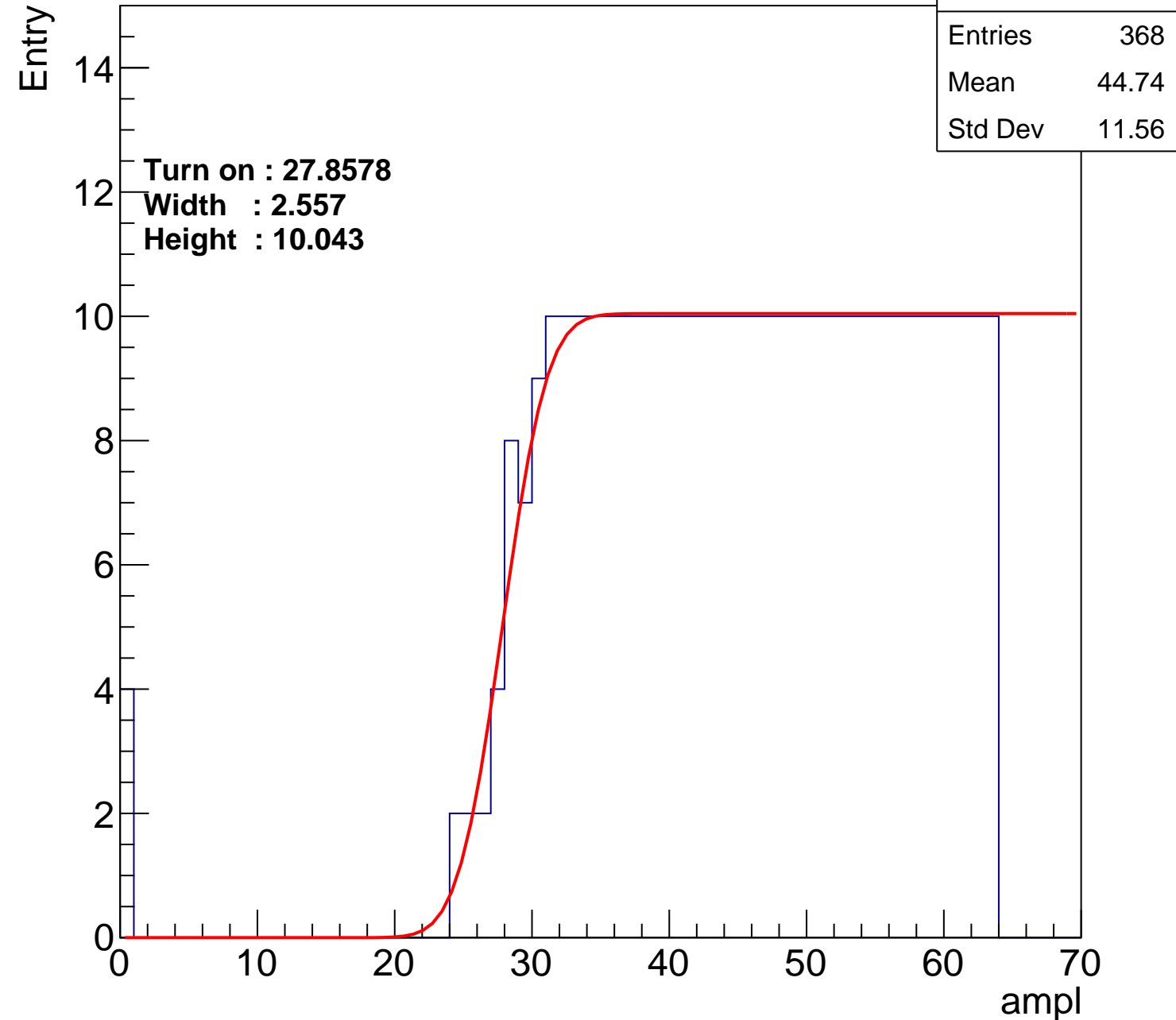
Width : 2.557

Height : 10.043

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch119

calib_packv5_042523_0143.root, FC#0, port D2

Entries	371
Mean	44.61
Std Dev	11.53

Turn on : 27.7195

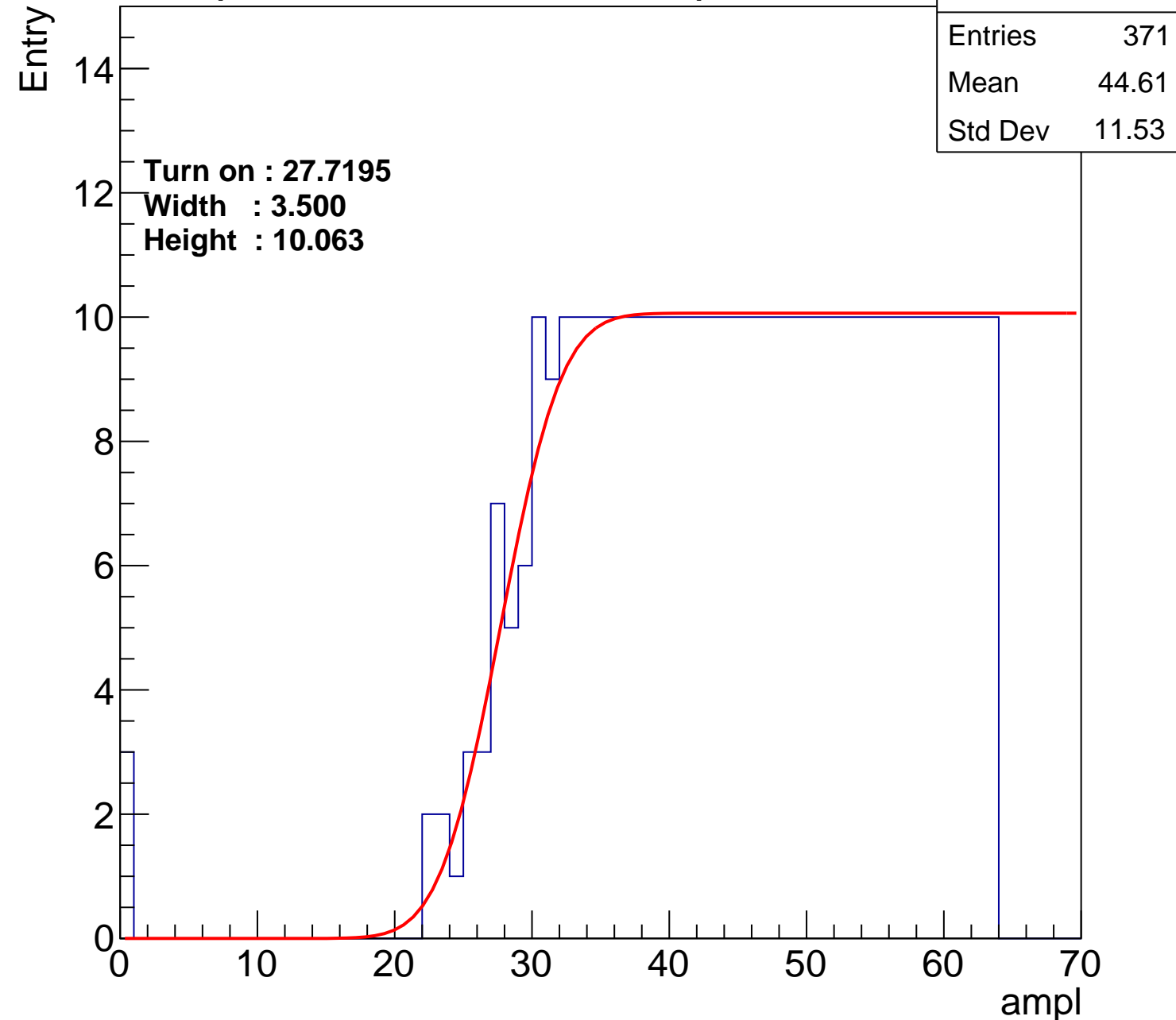
Width : 3.500

Height : 10.063

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch120

calib_packv5_042523_0143.root, FC#0, port D2

Entries	386
Mean	43.74
Std Dev	12.23

Turn on : 26.2796

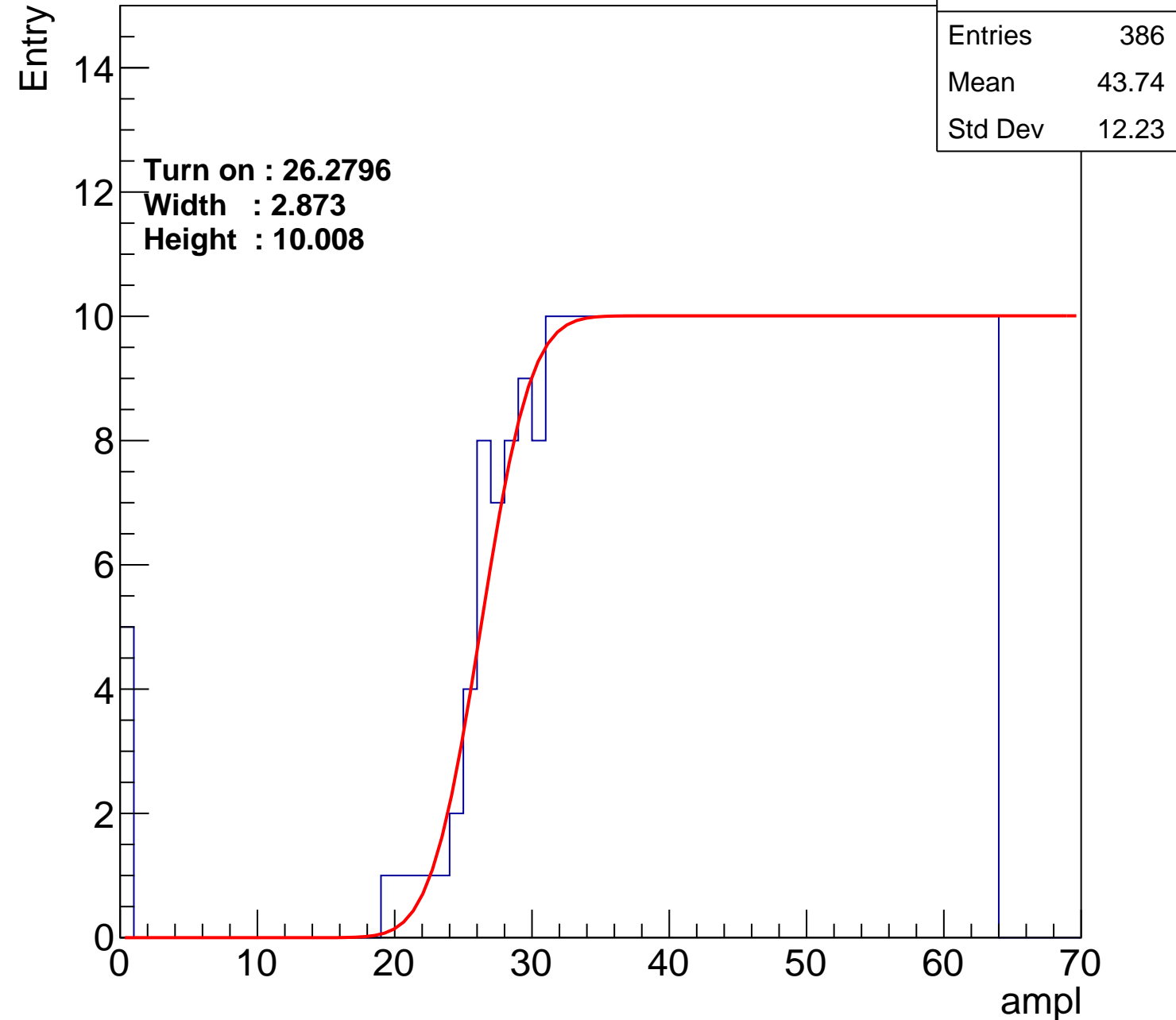
Width : 2.873

Height : 10.008

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch121

calib_packv5_042523_0143.root, FC#0, port D2

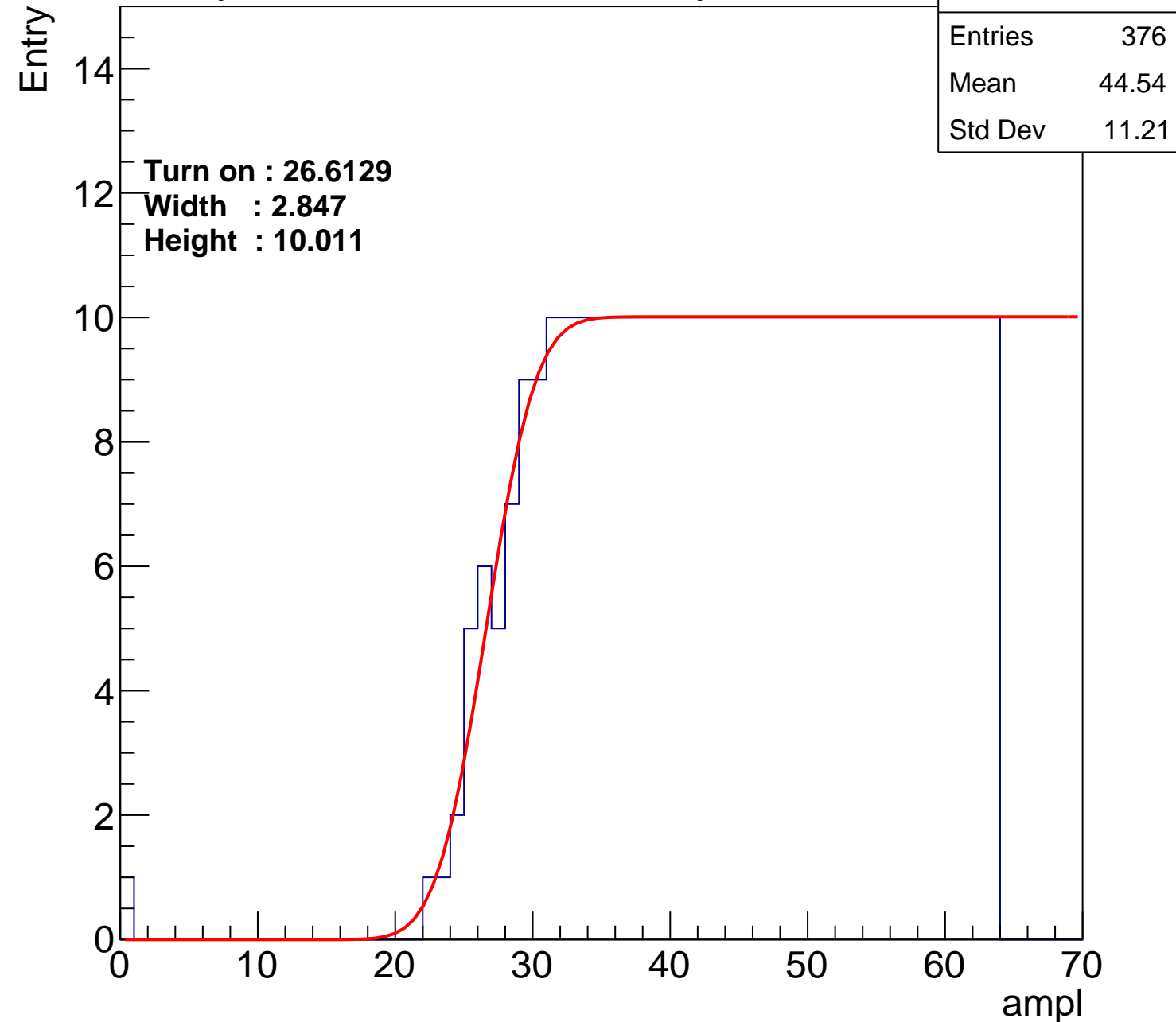
Entry

14
12
10
8
6
4
2
0

Turn on : 26.6129
Width : 2.847
Height : 10.011

Entries	376
Mean	44.54
Std Dev	11.21

ampl



B1L101S, U8-ch122

calib_packv5_042523_0143.root, FC#0, port D2

Entries	396
Mean	43.27
Std Dev	12.49

Turn on : 25.2494

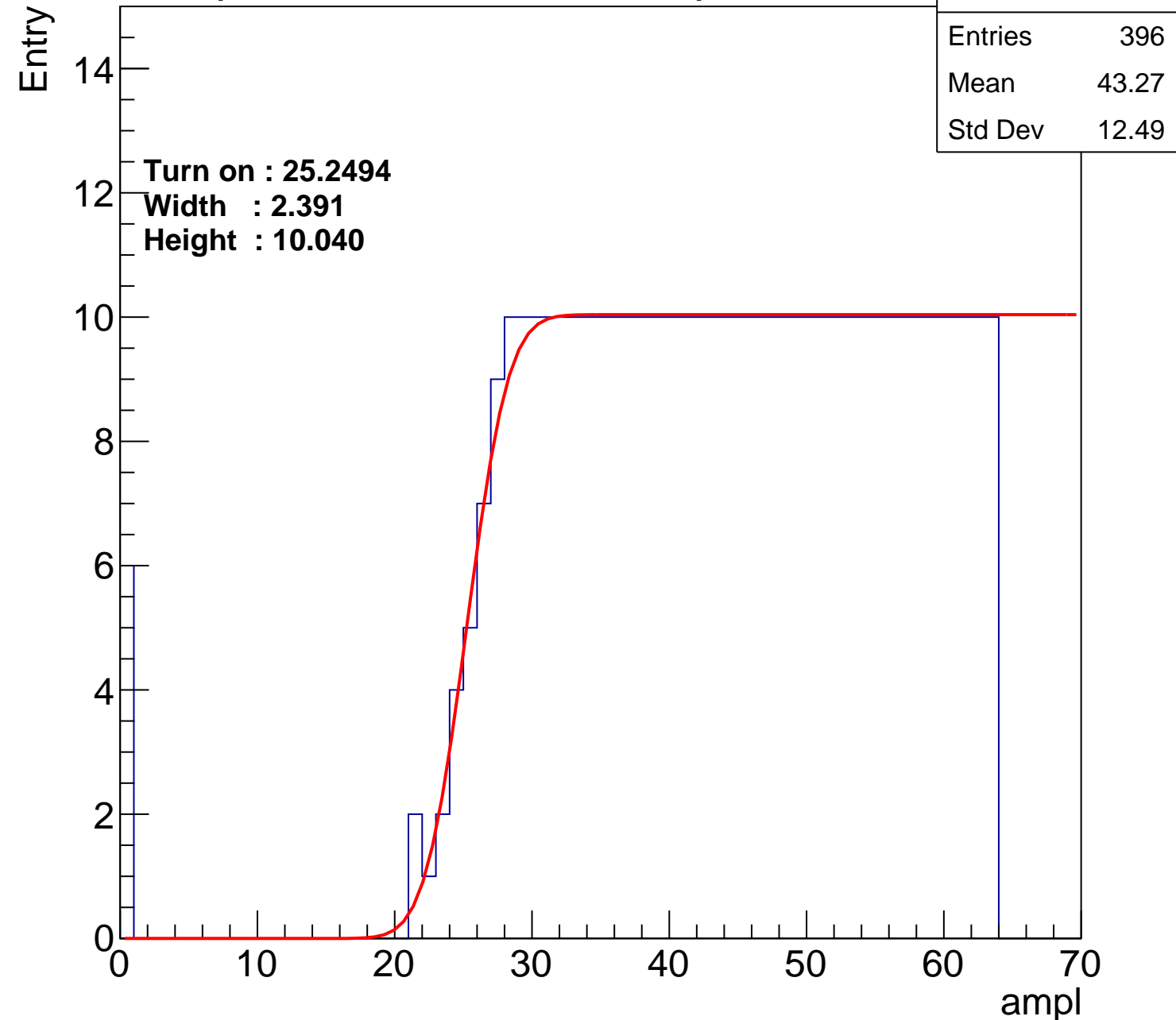
Width : 2.391

Height : 10.040

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch123

calib_packv5_042523_0143.root, FC#0, port D2

Entries	363
Mean	45.05
Std Dev	11.16

Turn on : 27.9107

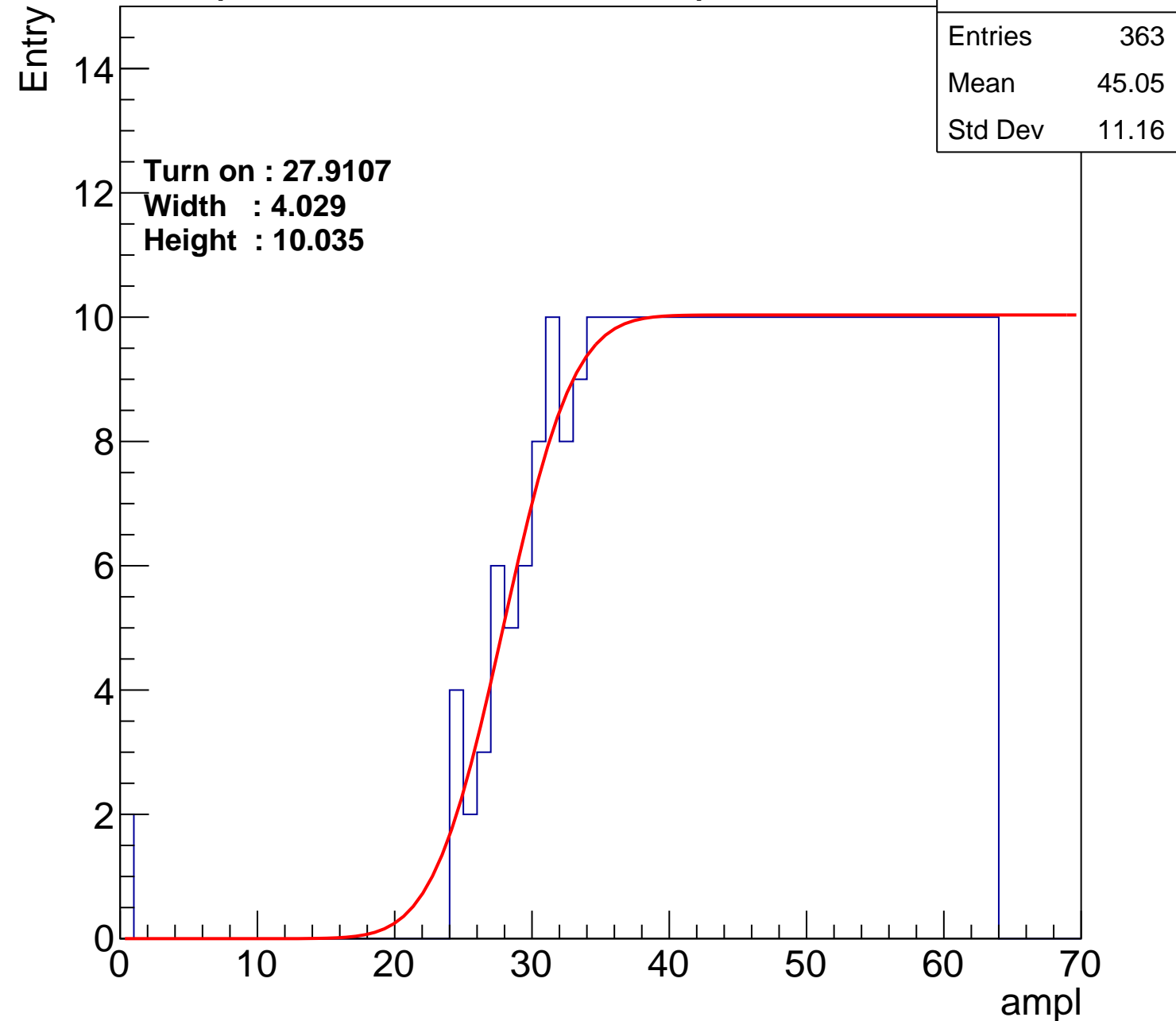
Width : 4.029

Height : 10.035

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch124

calib_packv5_042523_0143.root, FC#0, port D2

Entries	391
Mean	43.62
Std Dev	12.08

Turn on : 25.9263

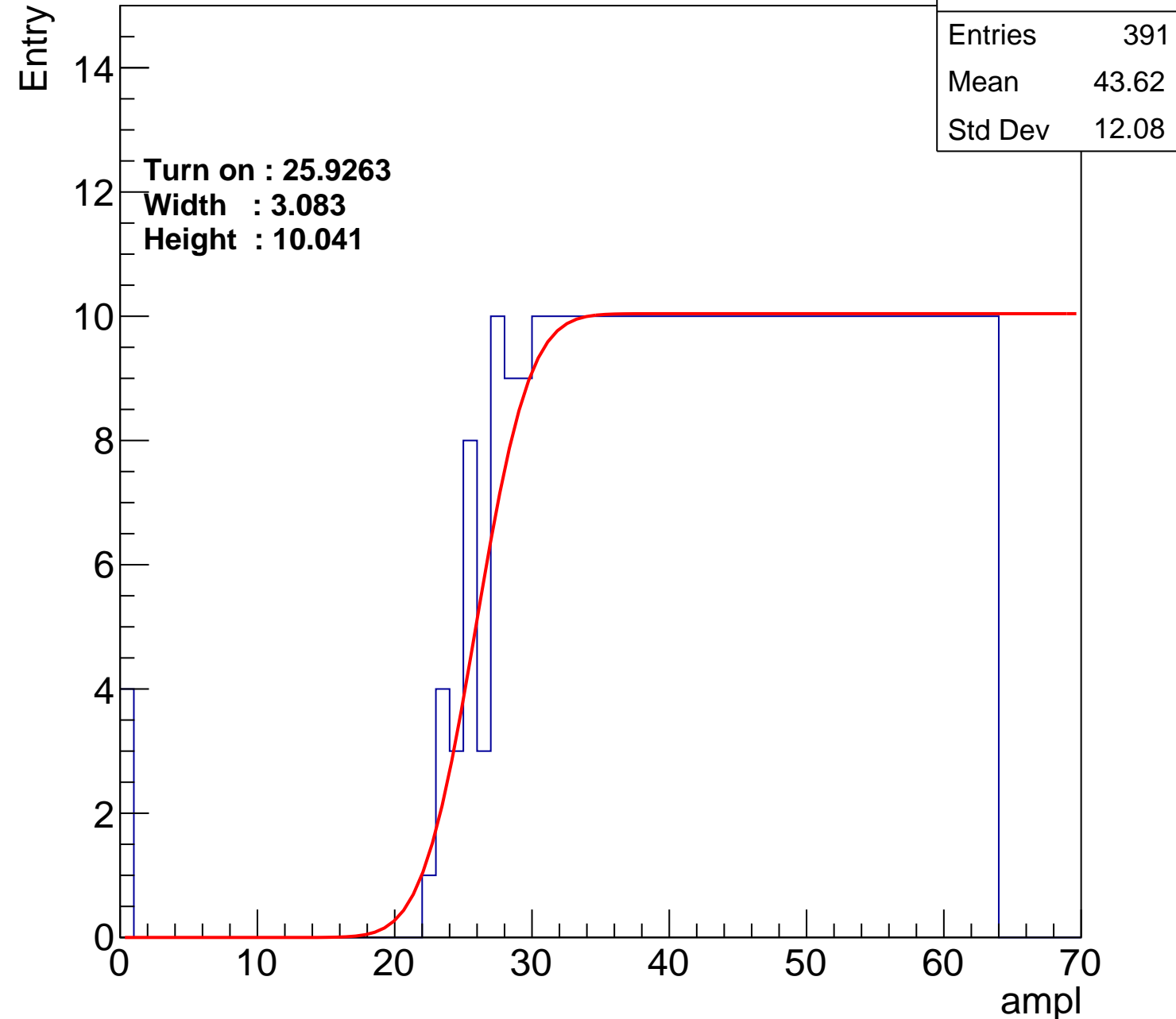
Width : 3.083

Height : 10.041

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch125

calib_packv5_042523_0143.root, FC#0, port D2

Entries	360
Mean	45.15
Std Dev	11.25

Turn on : 28.7755

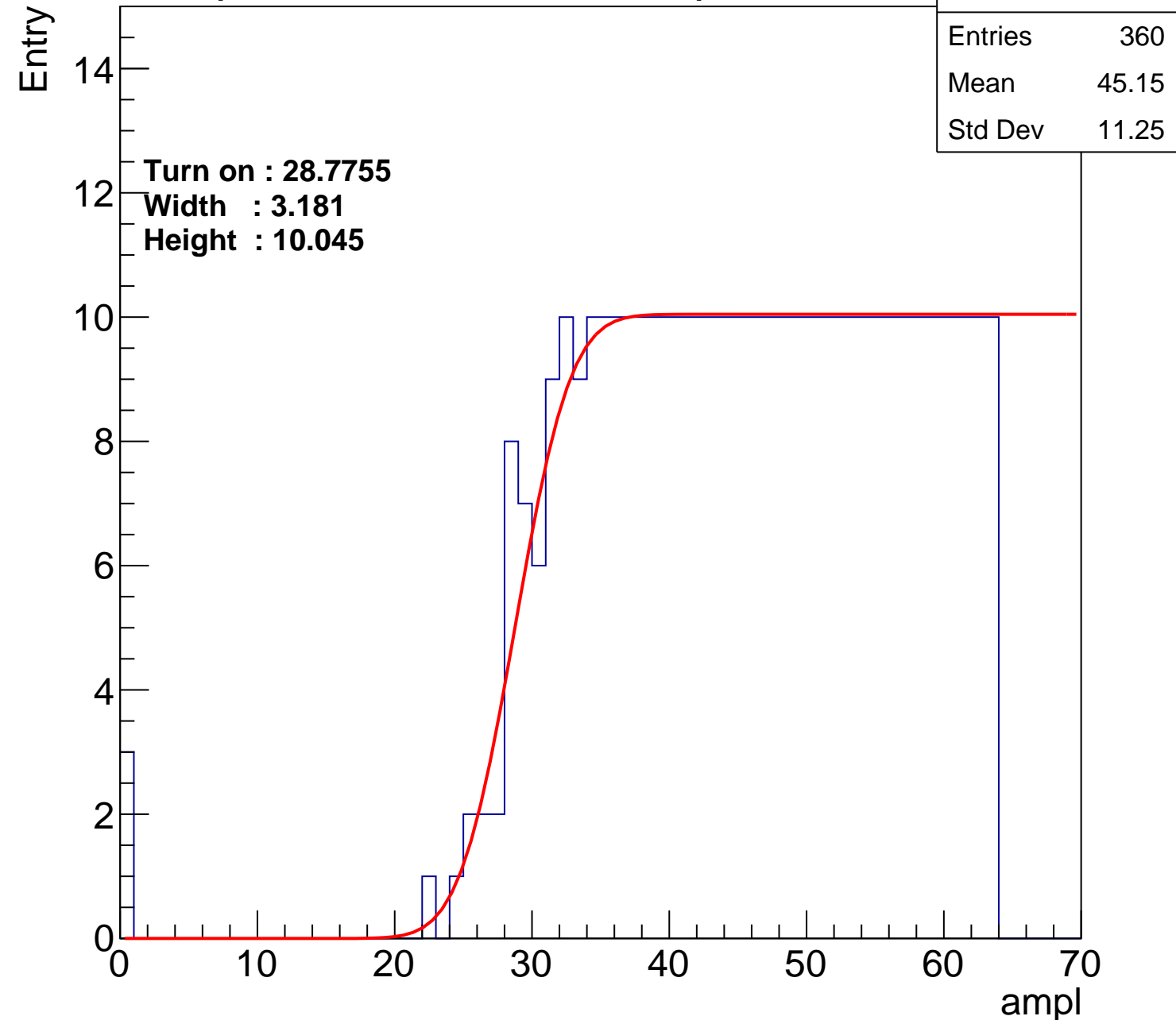
Width : 3.181

Height : 10.045

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch126

calib_packv5_042523_0143.root, FC#0, port D2

Entries	389
Mean	43.8
Std Dev	11.79

Turn on : 25.7043

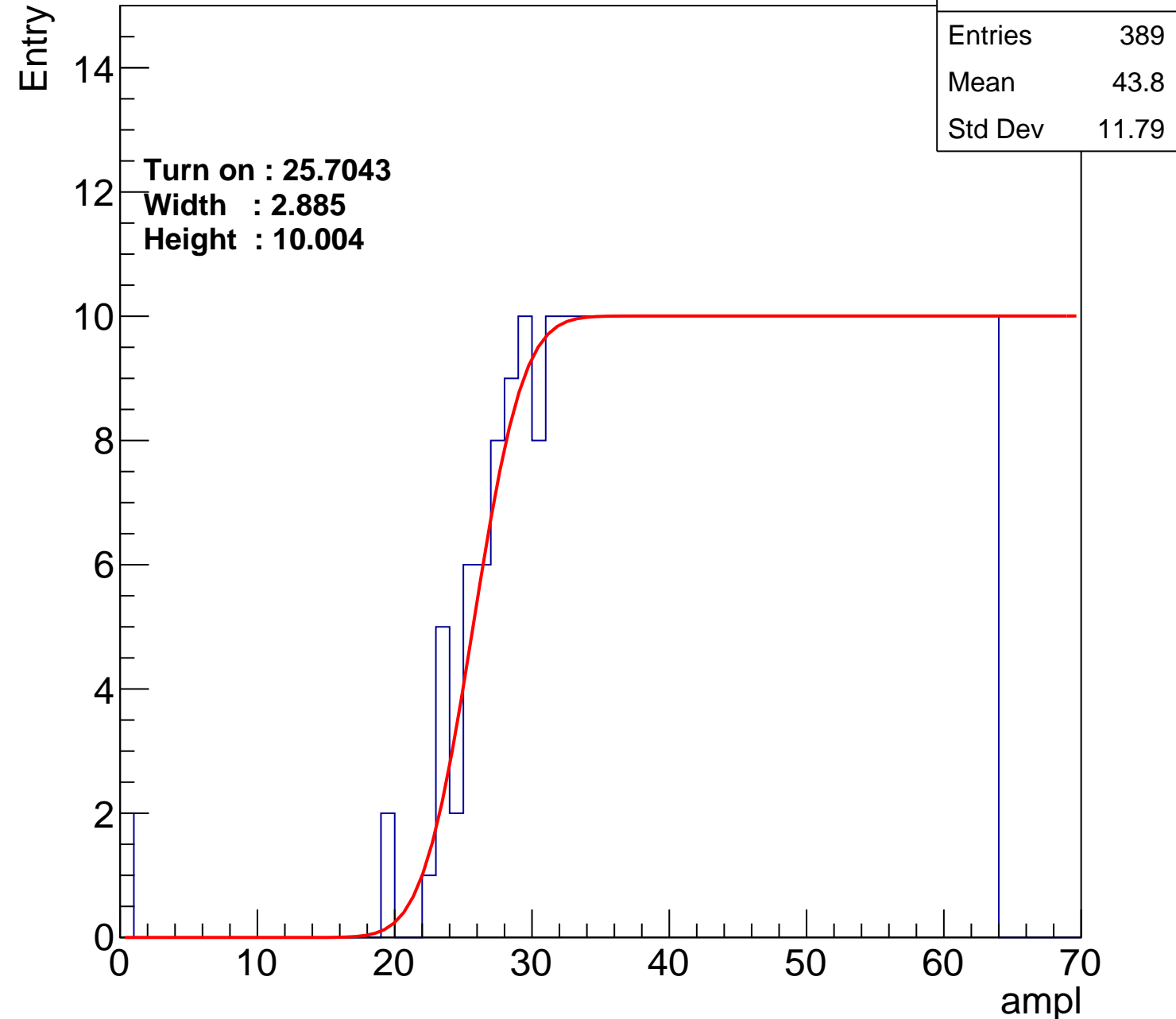
Width : 2.885

Height : 10.004

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch127

calib_packv5_042523_0143.root, FC#0, port D2

Entries	364
Mean	44.88
Std Dev	11.55

Turn on : 28.2485

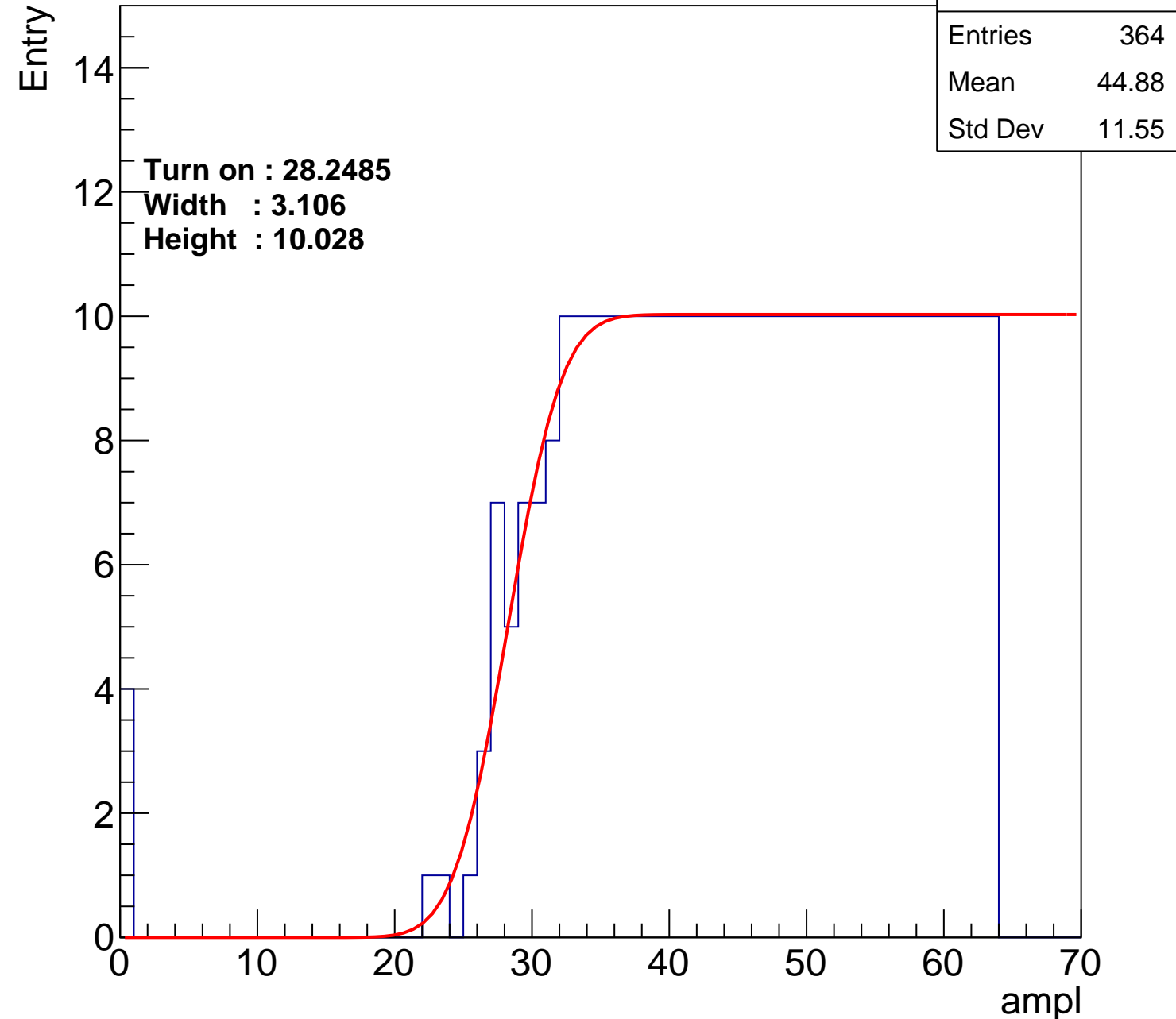
Width : 3.106

Height : 10.028

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U8-ch127

calib_packv5_042523_0143.root, FC#0, port D2

Entries	364
Mean	44.88
Std Dev	11.55

Turn on : 28.2485

Width : 3.106

Height : 10.028

Entry

14
12
10
8
6
4
2
0

ampl

