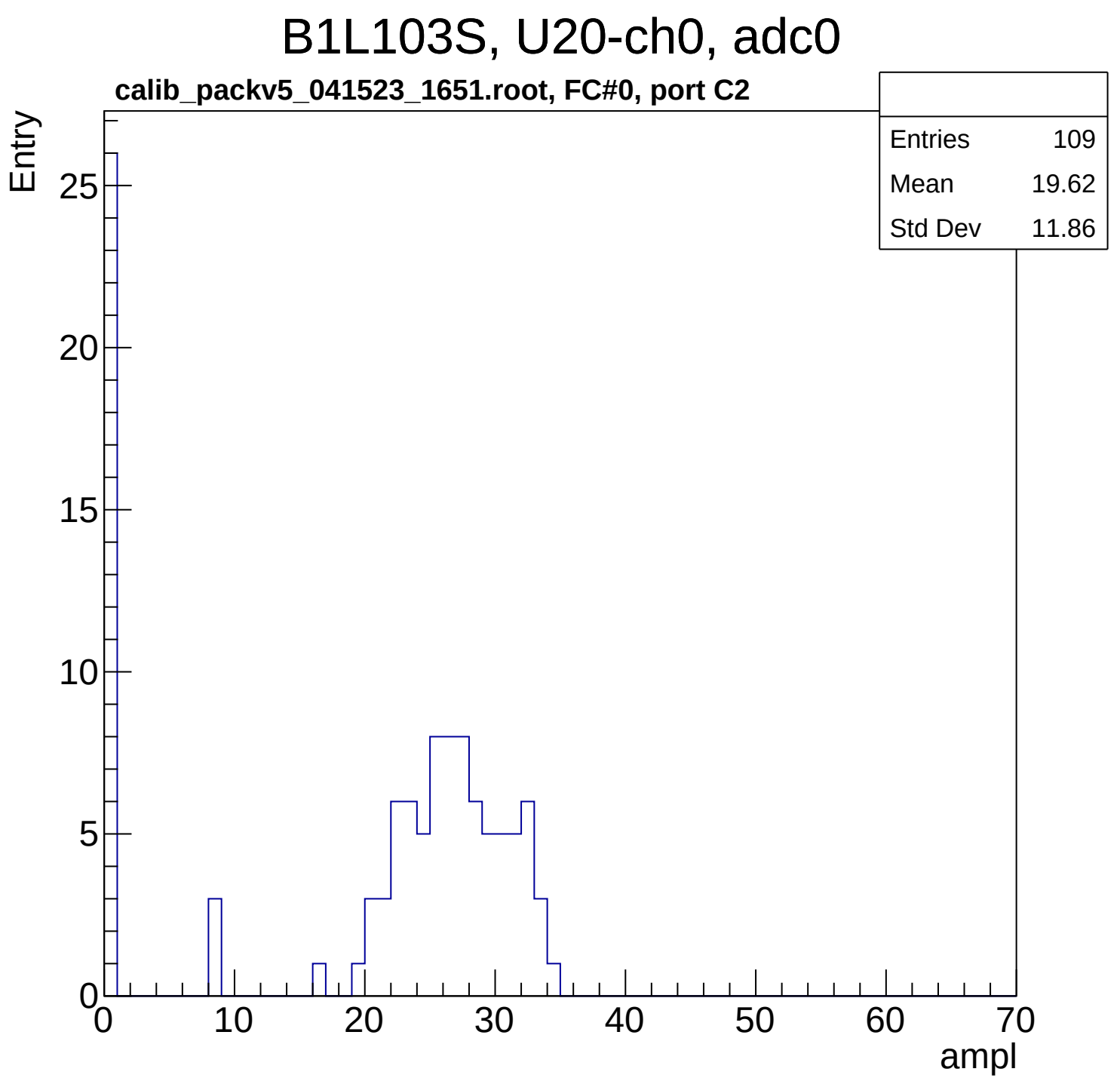
B1L103S, U20-ch0, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 109
Mean 19.62
Std Dev 11.86
Entry
0
5
10
15
20
25
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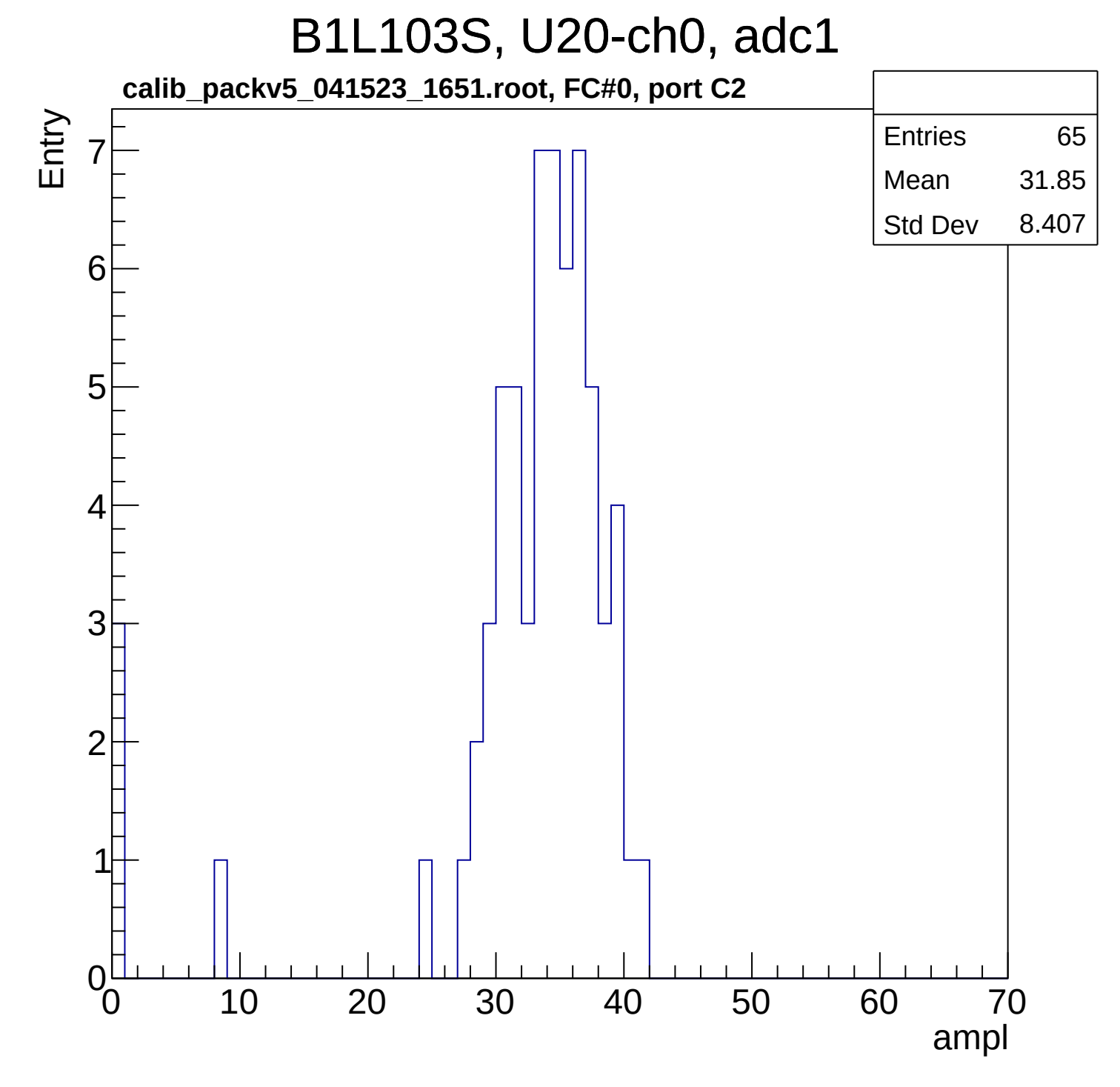
60
70
ampl


B1L103S, U20-ch0, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 31.85
Std Dev 8.407
Entry
ampl
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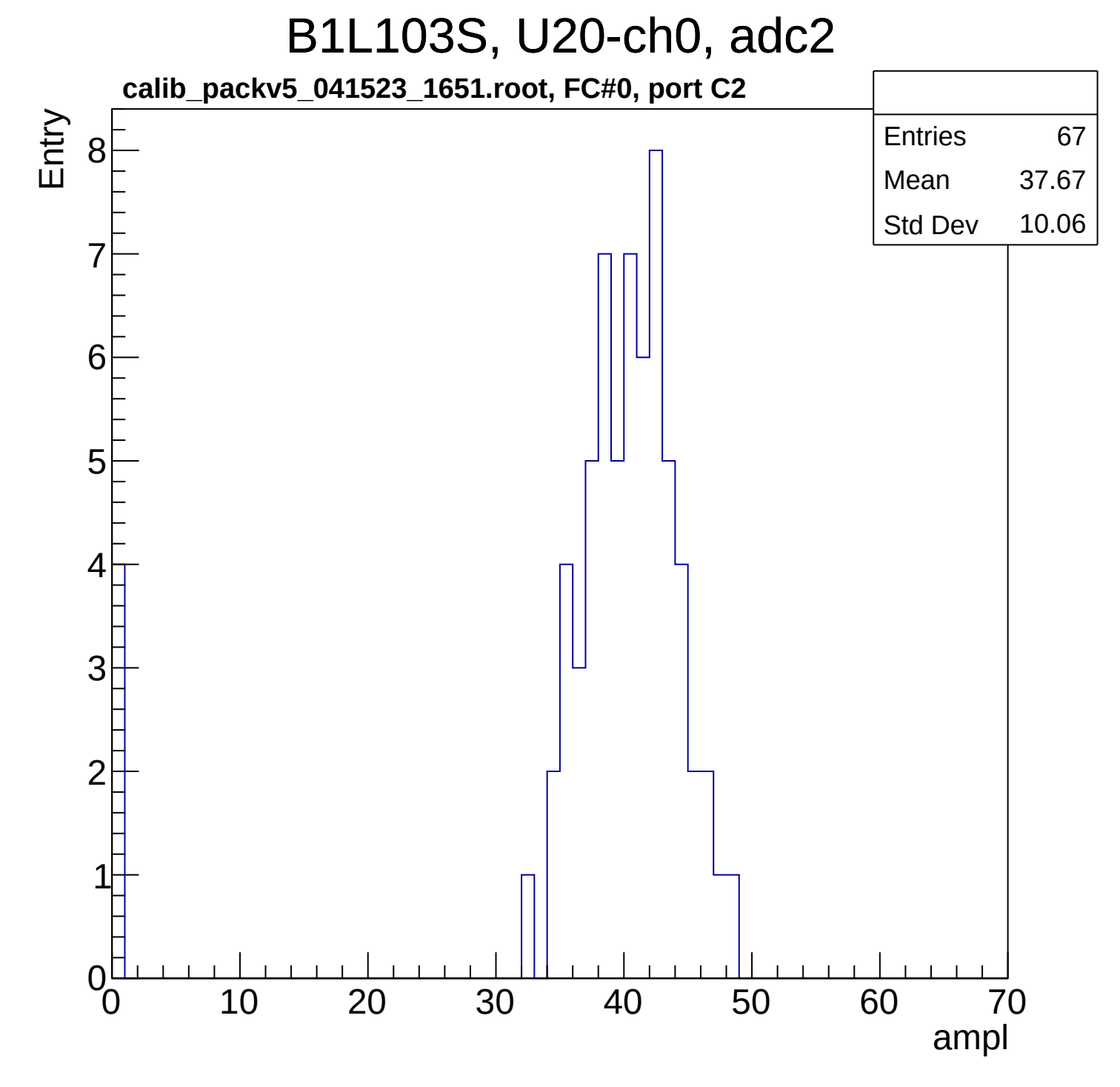
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U20-ch0, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 37.67
Std Dev 10.06
Entry
ampl
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1
2
3
4
5
6
7
8
0
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60
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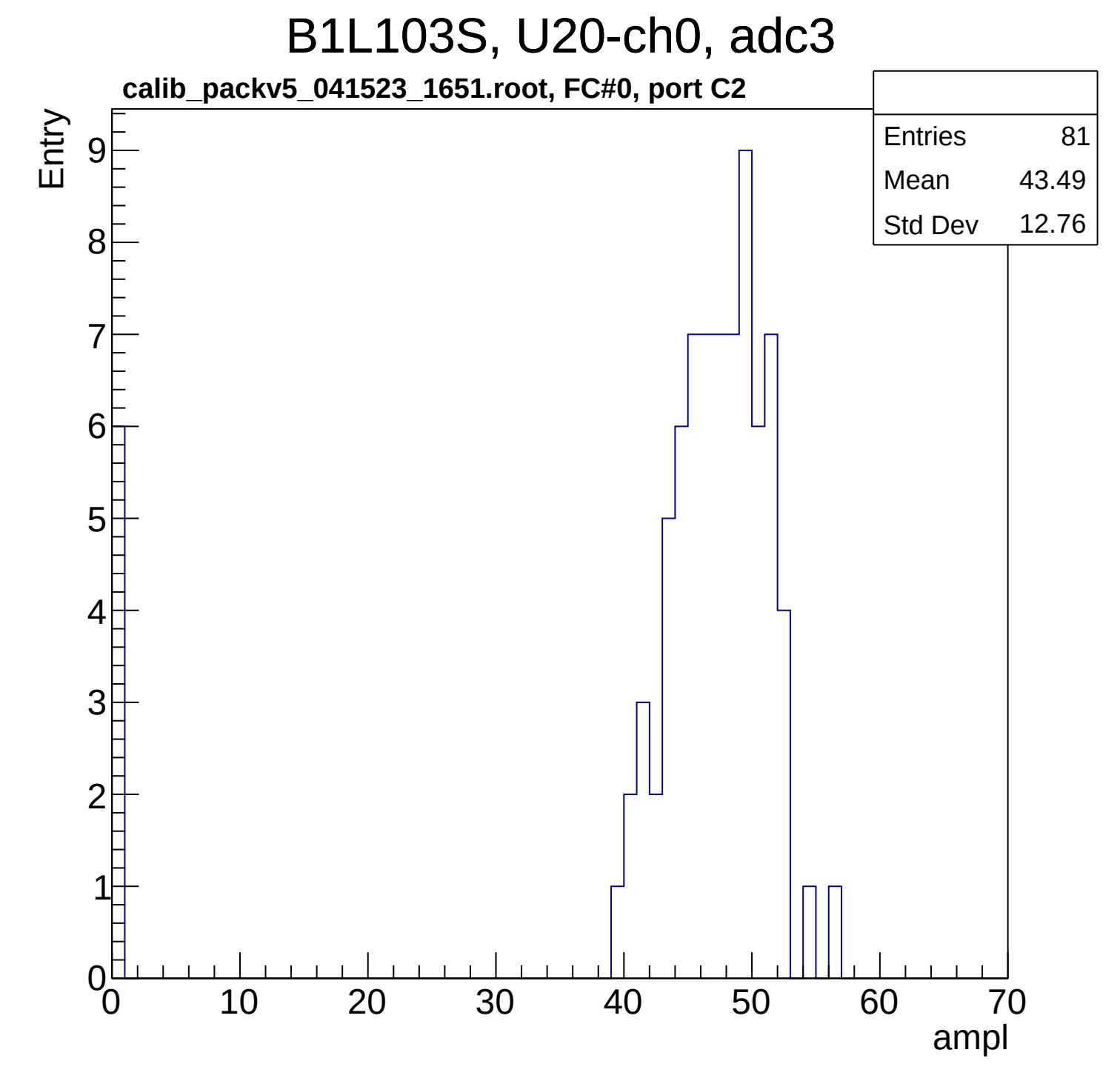
B1L103S, U20-ch0, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 43.49
Std Dev 12.76
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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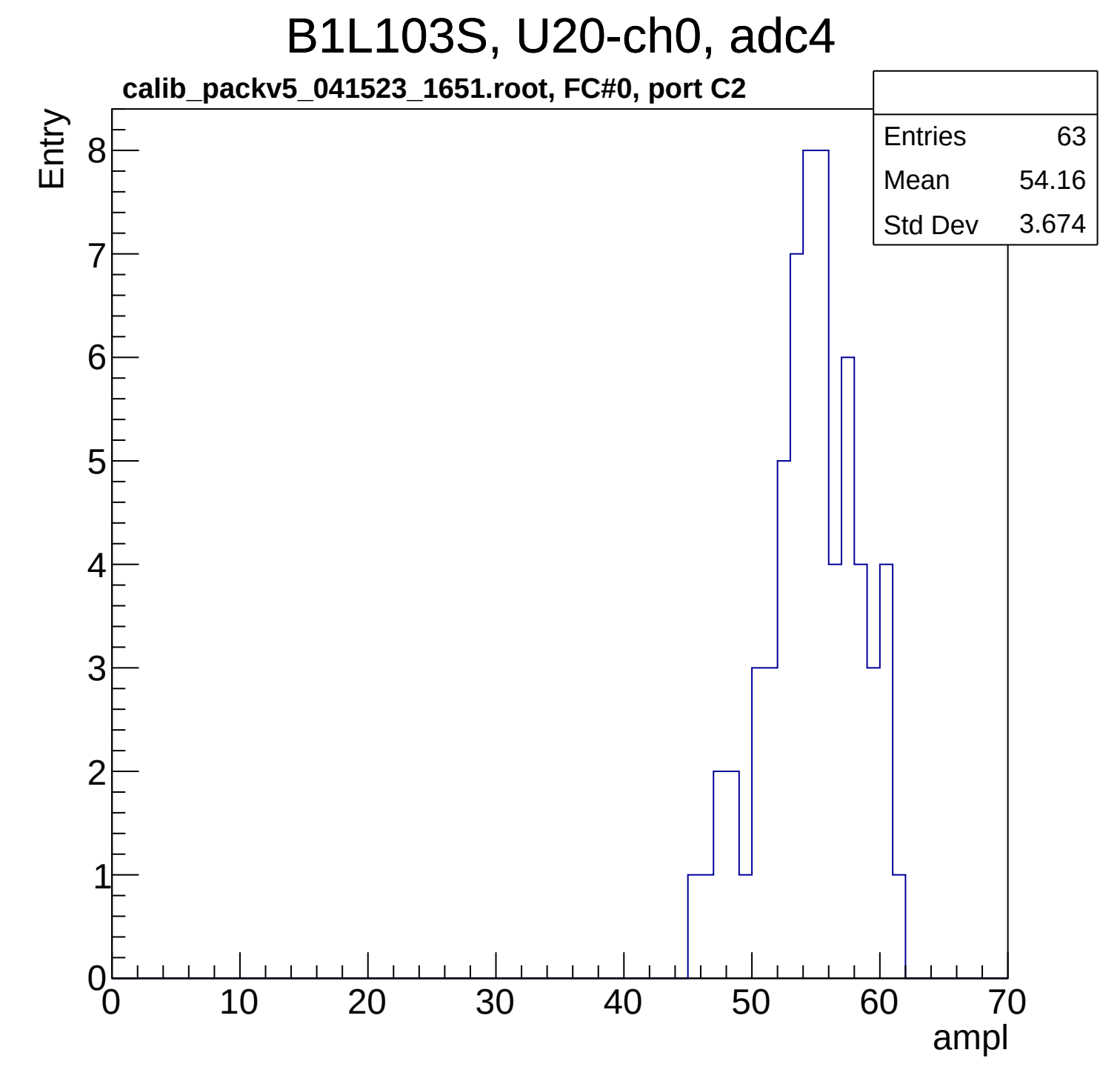
B1L103S, U20-ch0, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 54.16
Std Dev 3.674
Entry
ampl
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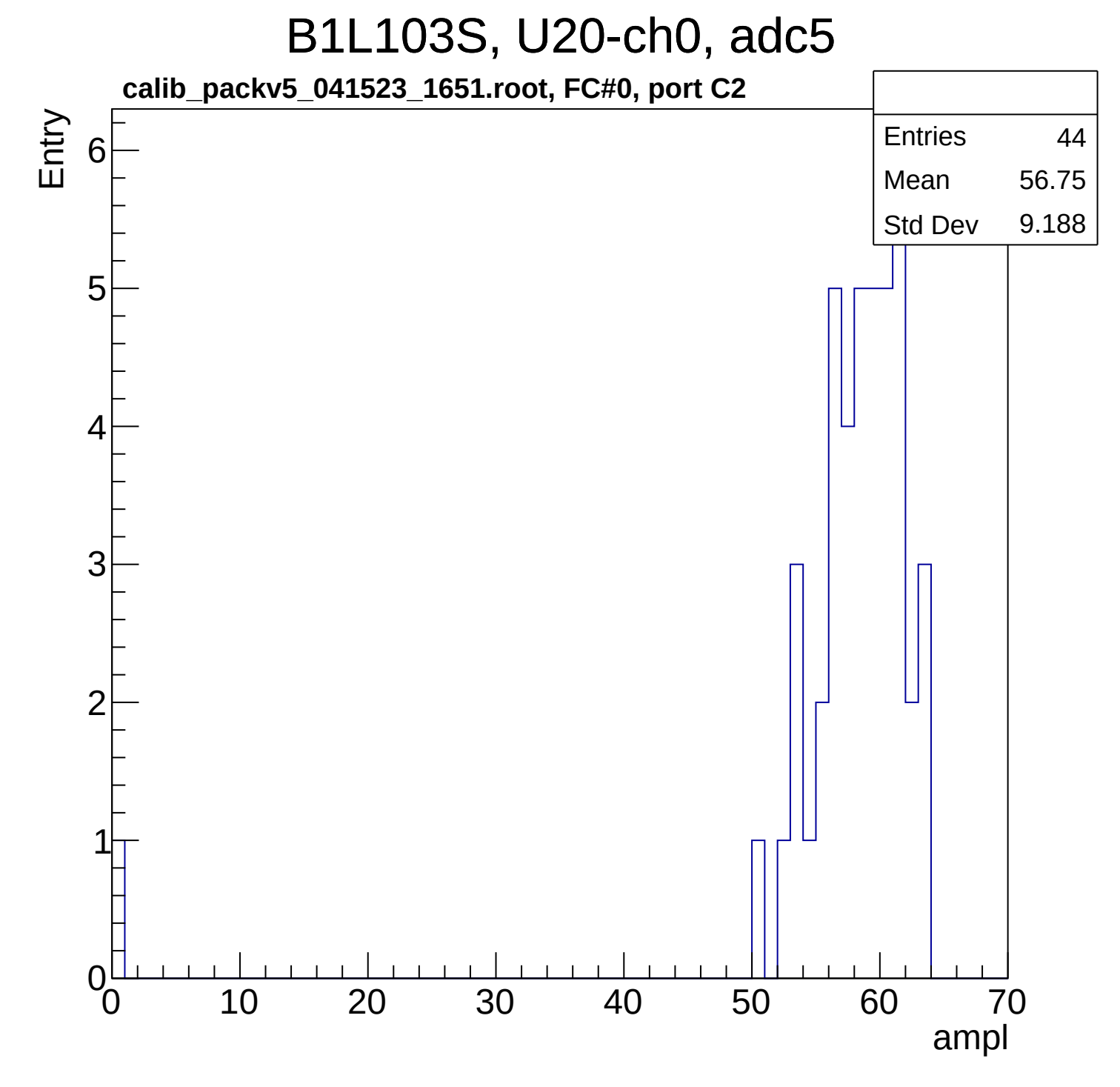
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch0, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 56.75
Std Dev 9.188
Entry
ampl
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2
3
4
5
6
0
10
20
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40
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60
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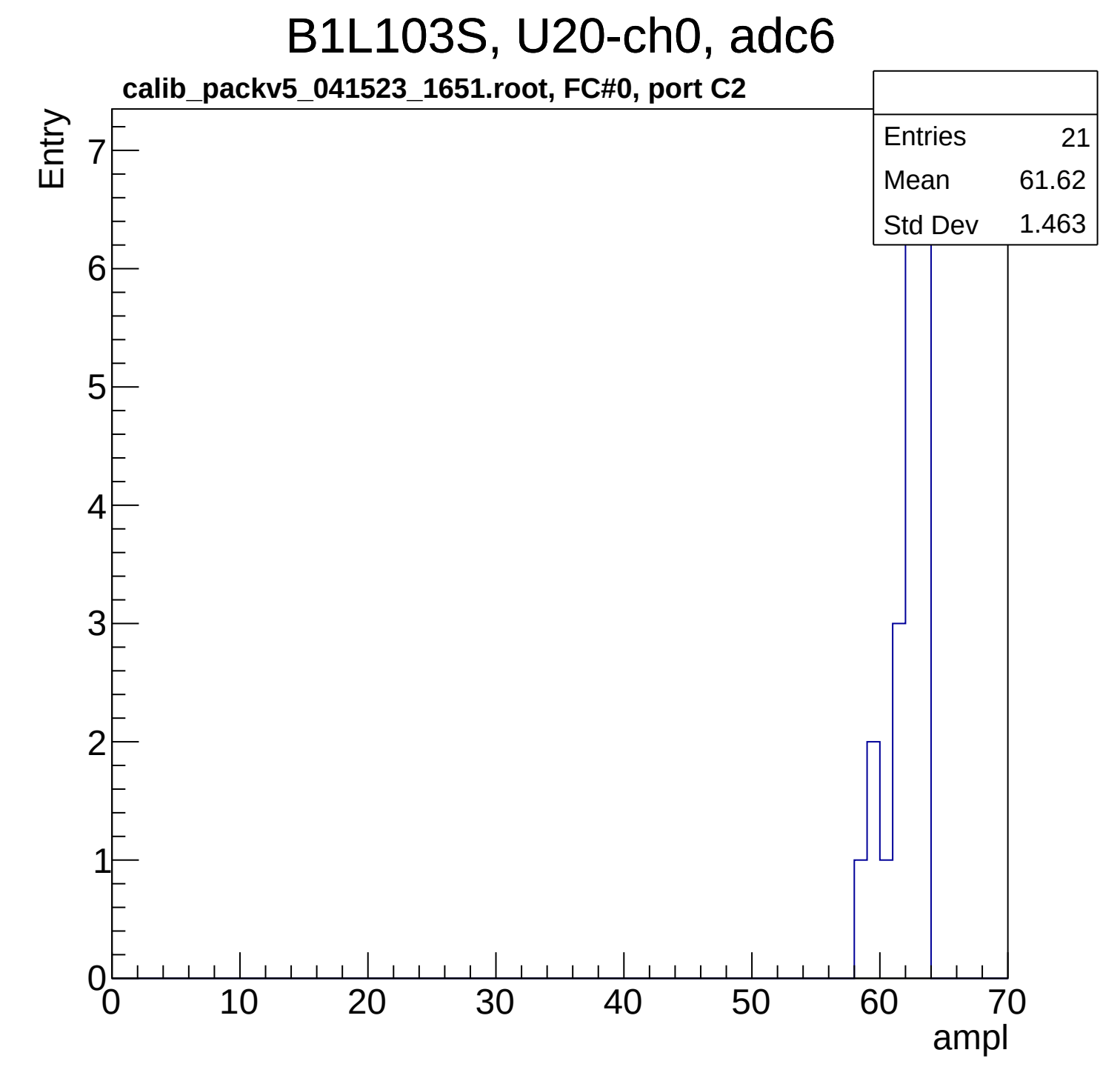
B1L103S, U20-ch0, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 61.62
Std Dev 1.463
Entry
ampl
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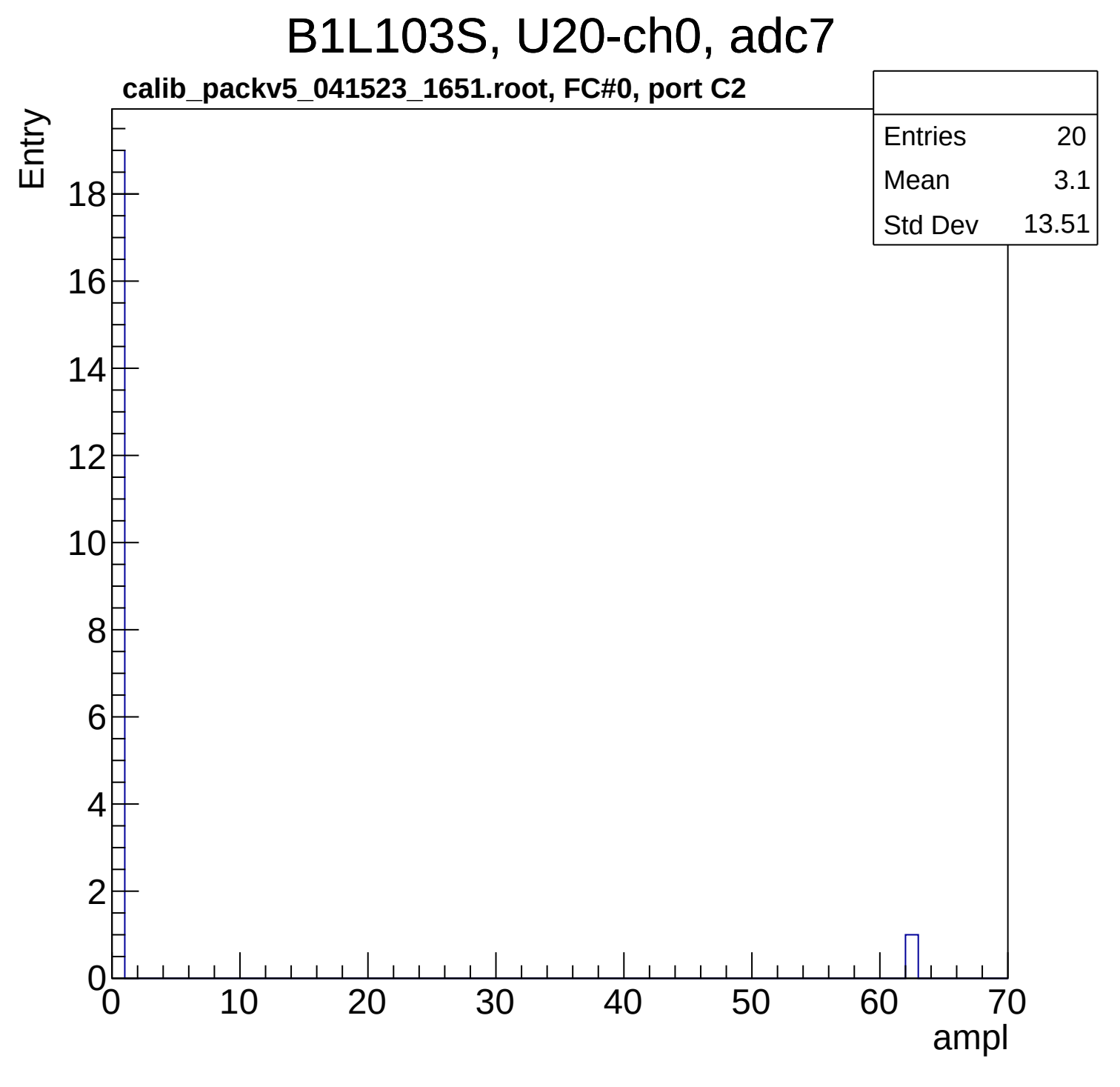
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U20-ch0, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
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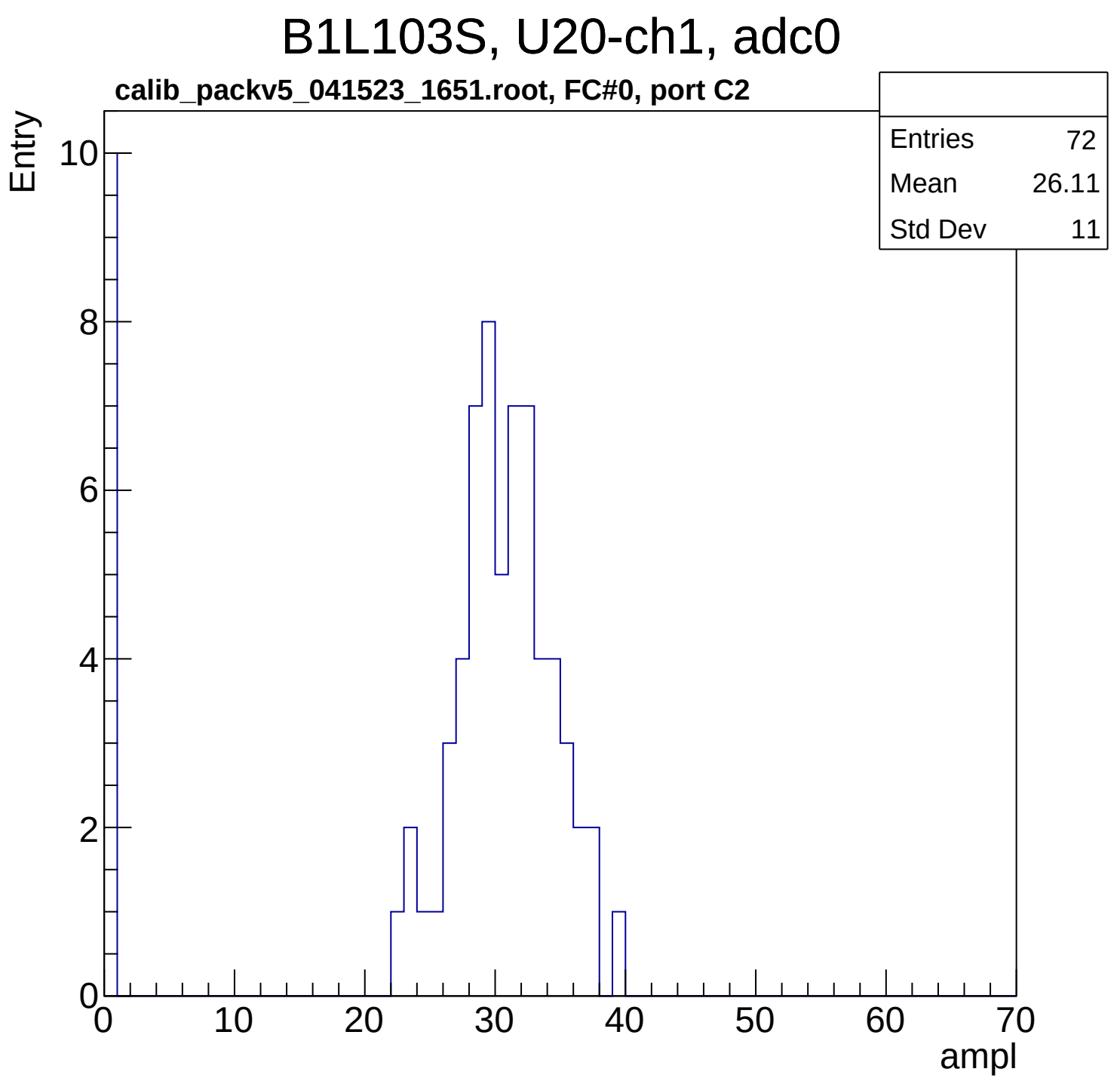
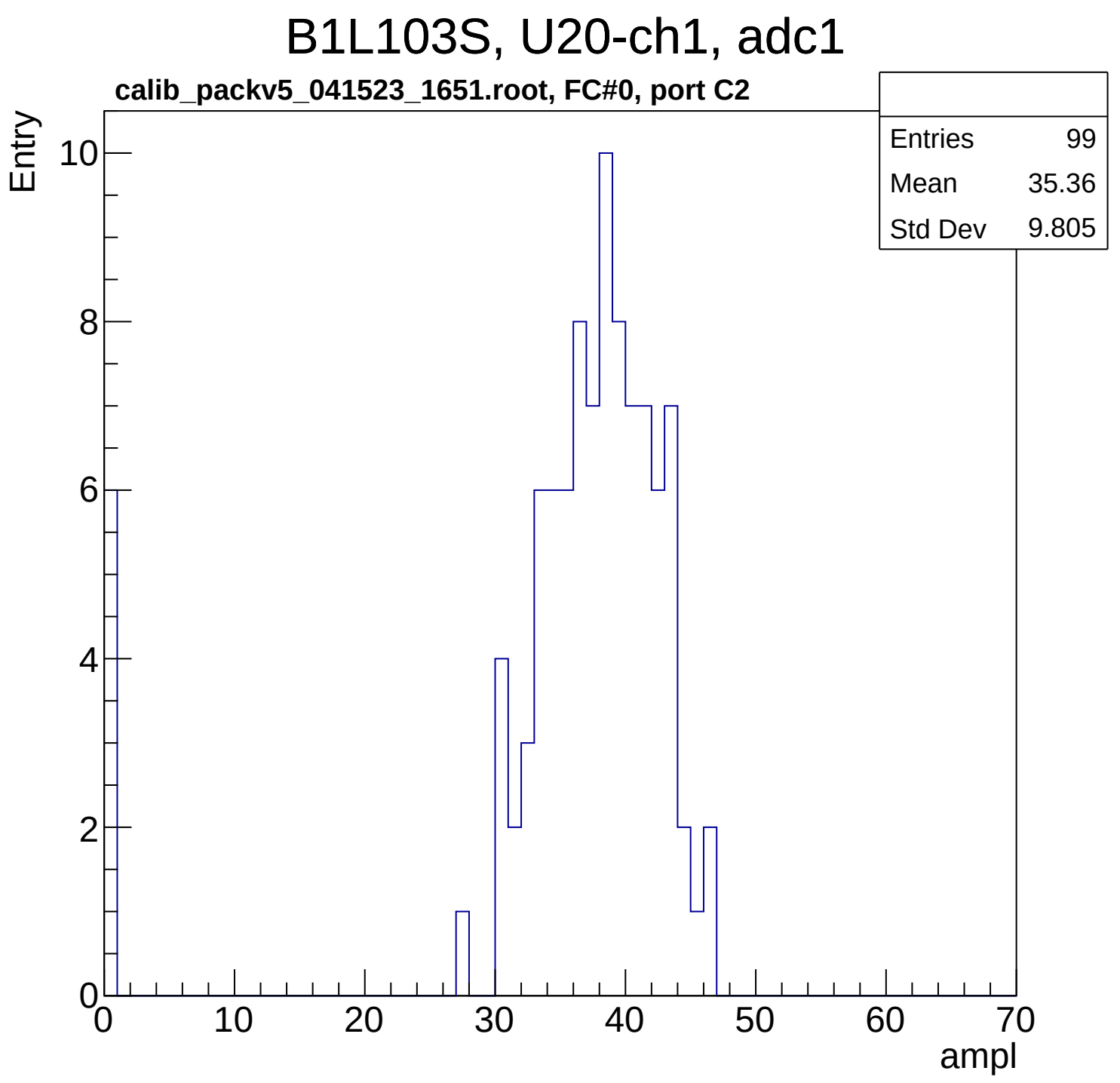
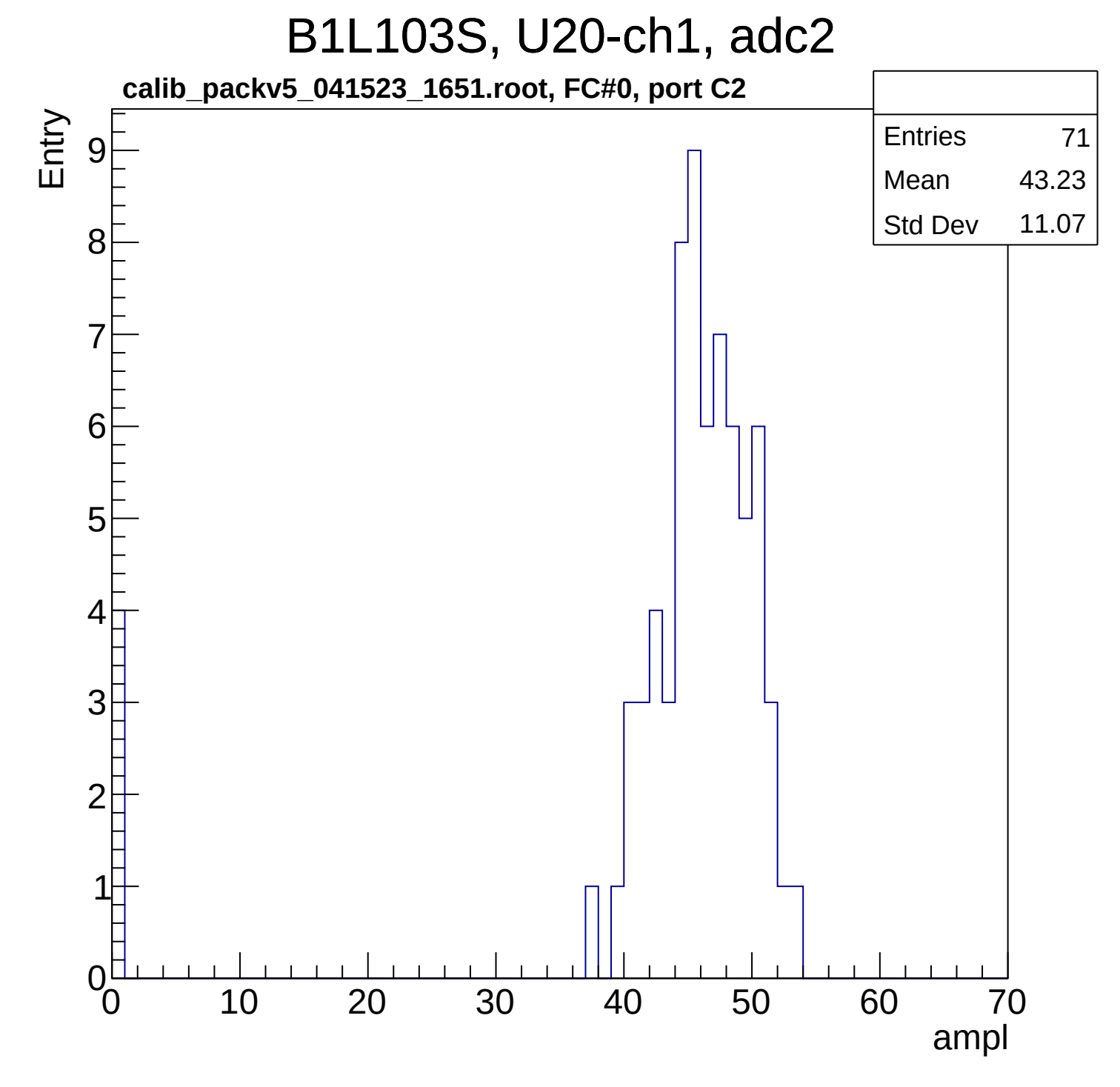
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch1, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 26.11
Std Dev 11
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U20-ch1, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 35.36
Std Dev 9.805
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U20-ch1, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 43.23
Std Dev 11.07
Entry
ampl
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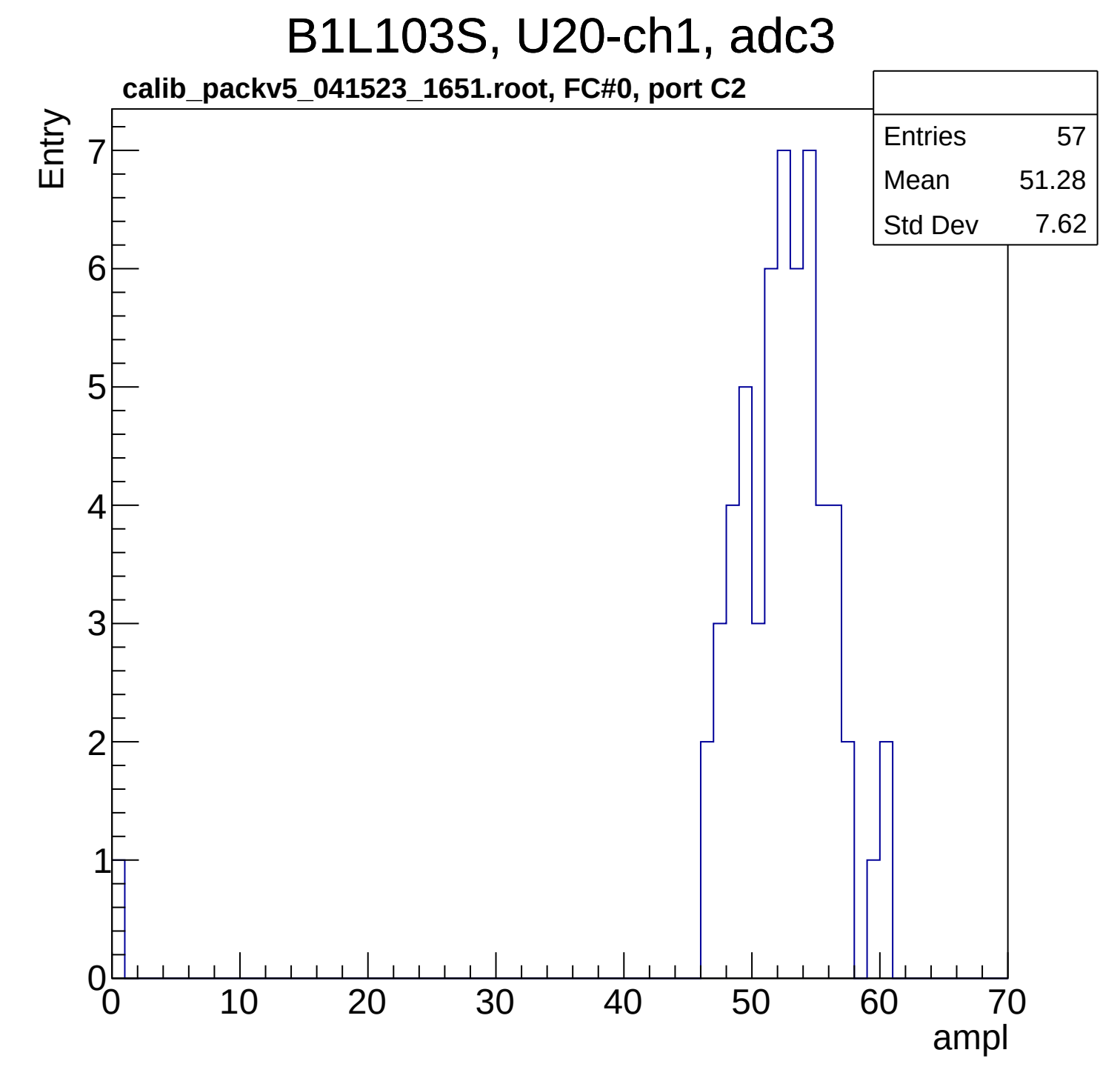
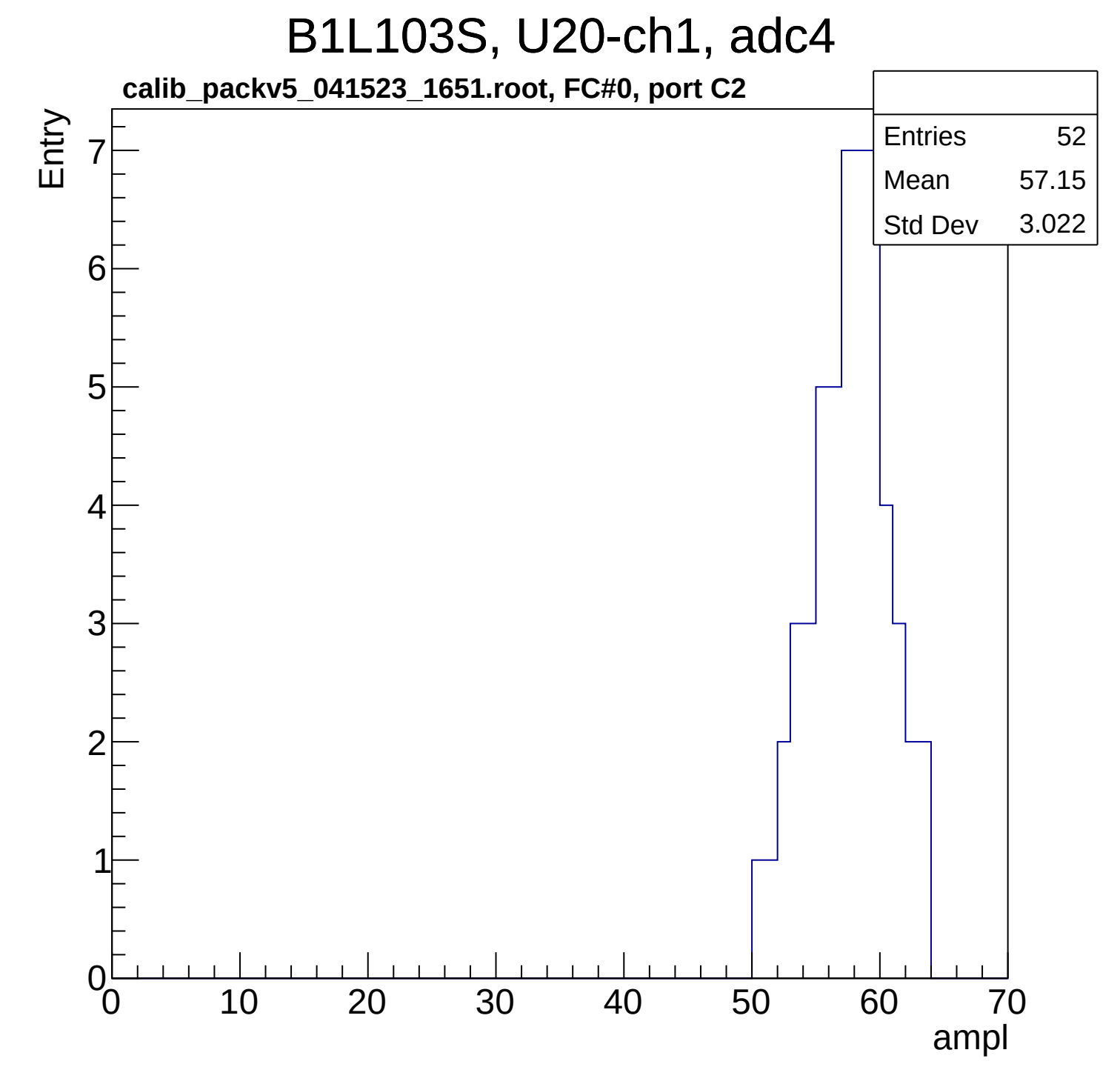
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch1, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 51.28
Std Dev 7.62
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U20-ch1, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 57.15
Std Dev 3.022
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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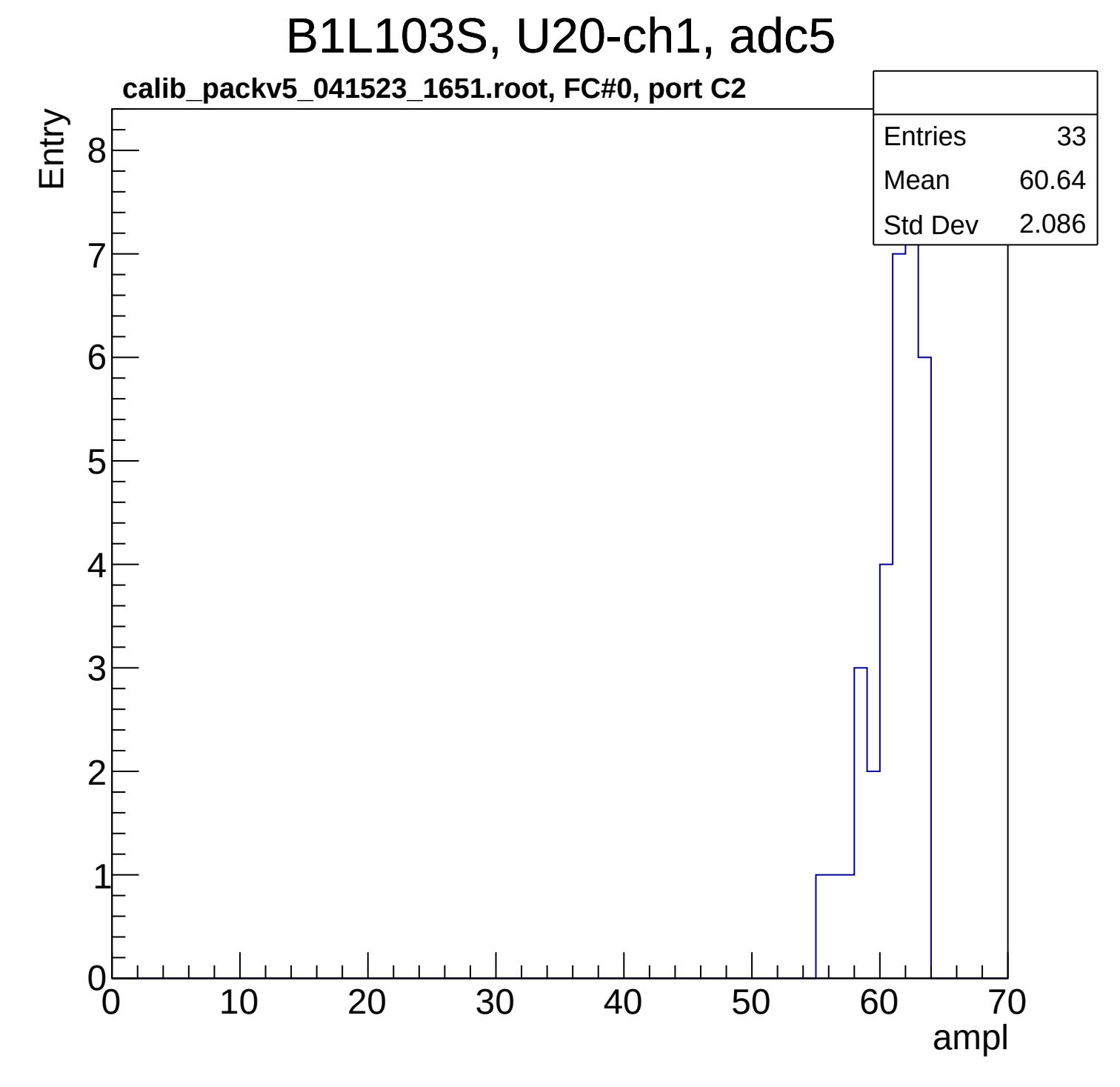
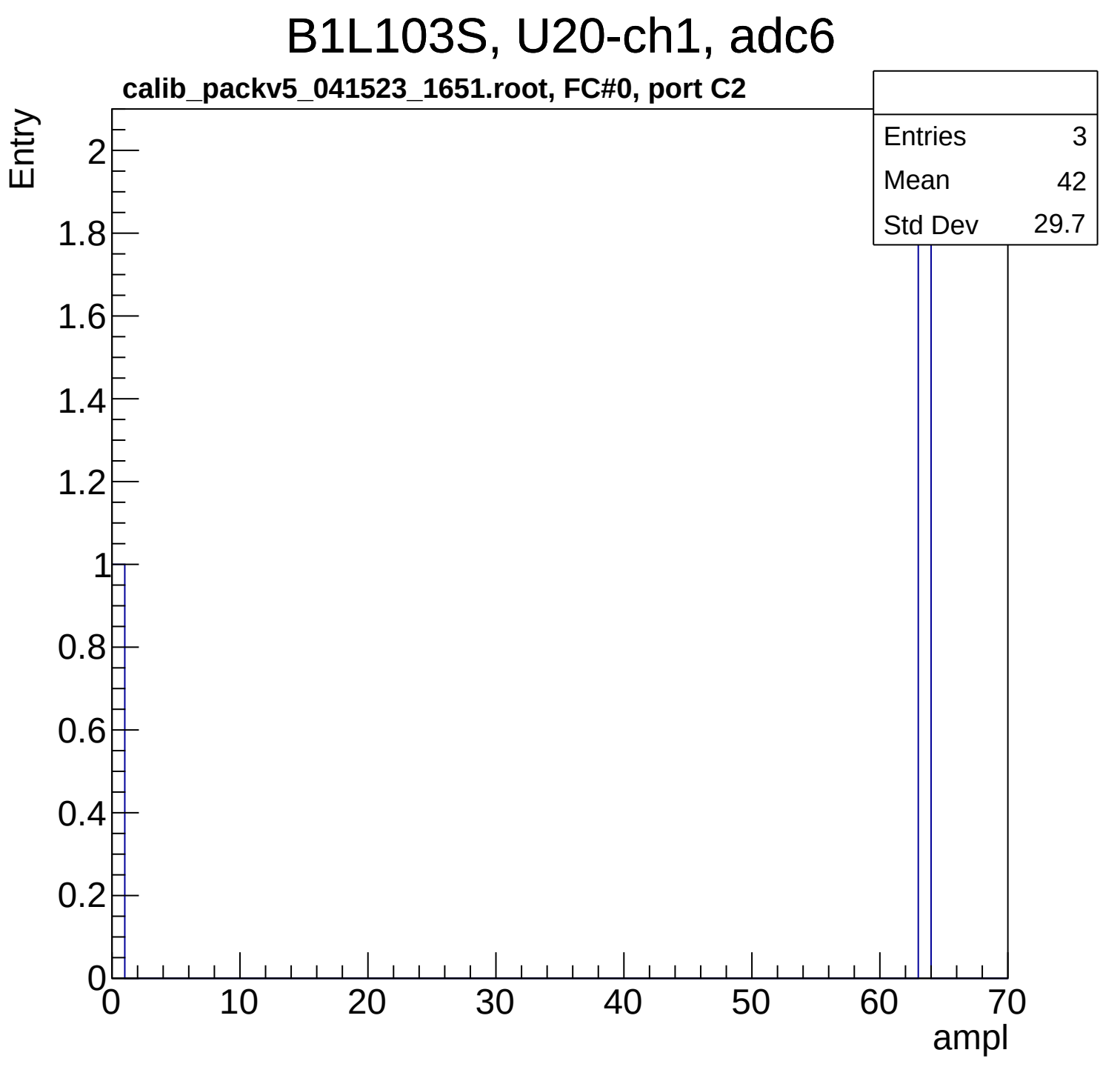
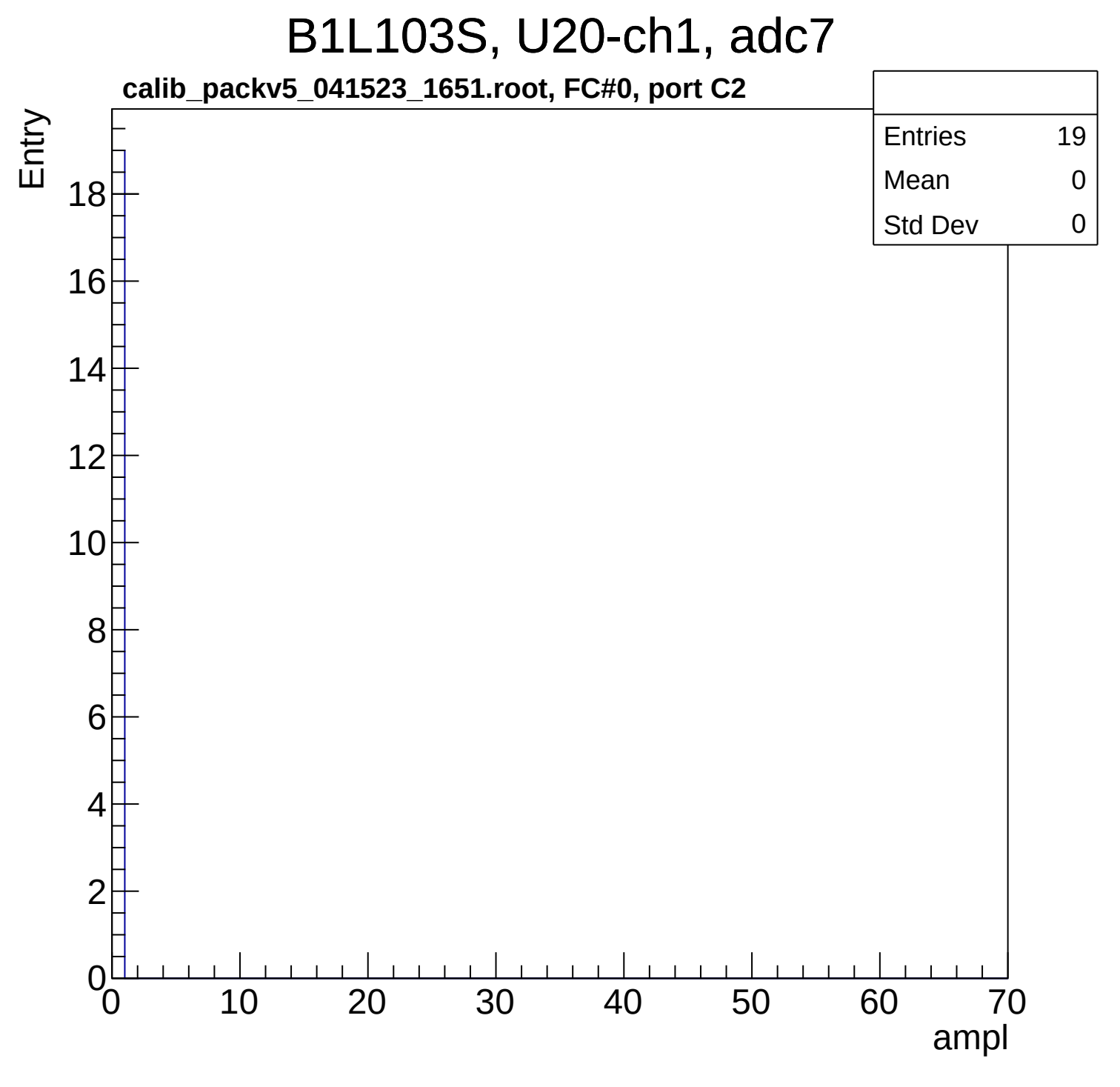
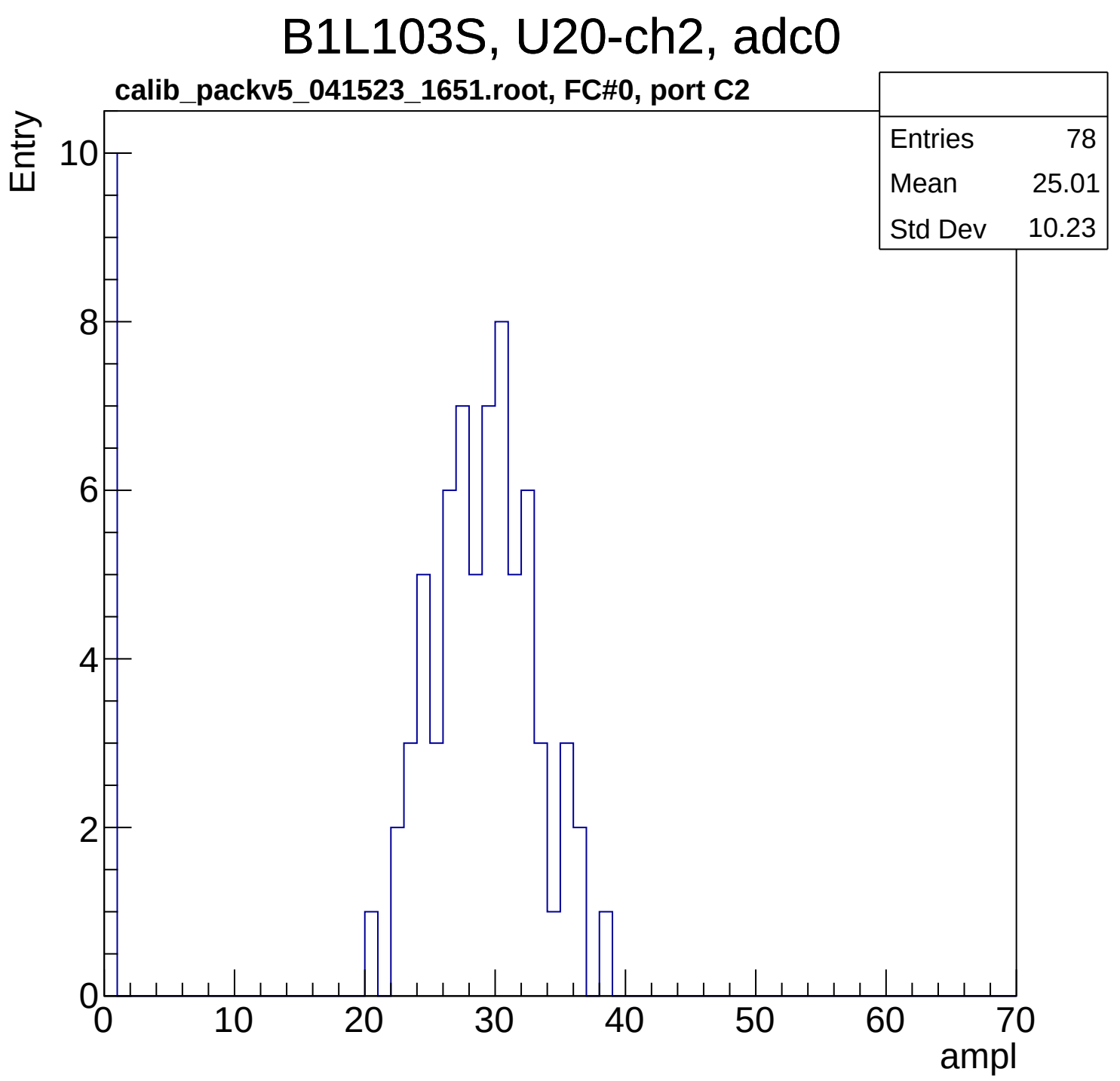

B1L103S, U20-ch1, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 60.64
Std Dev 2.086
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch1, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 42
Std Dev 29.7
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U20-ch1, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch2, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 25.01
Std Dev 10.23
Entry
ampl
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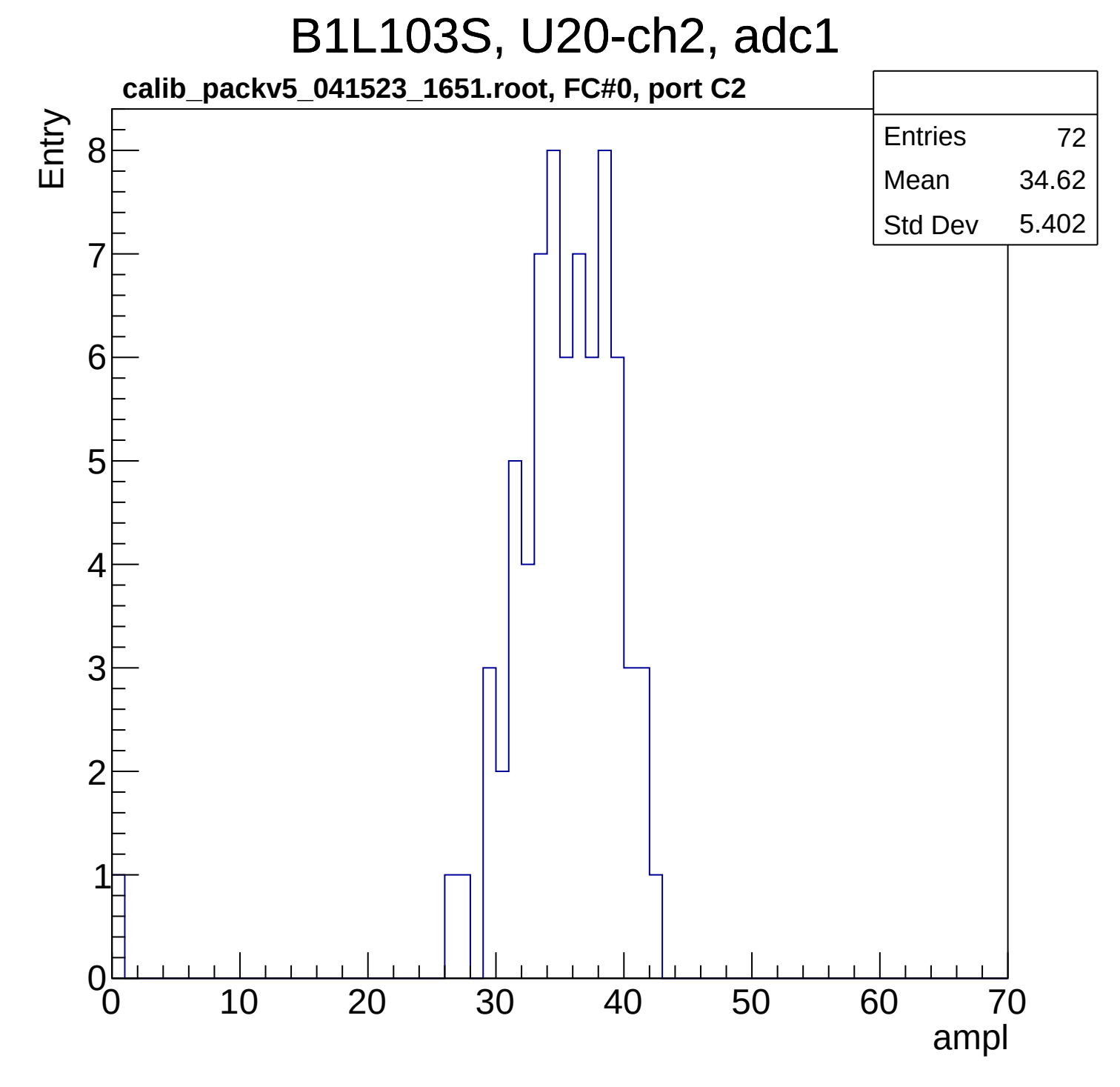
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U20-ch2, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 34.62
Std Dev 5.402
Entry
ampl
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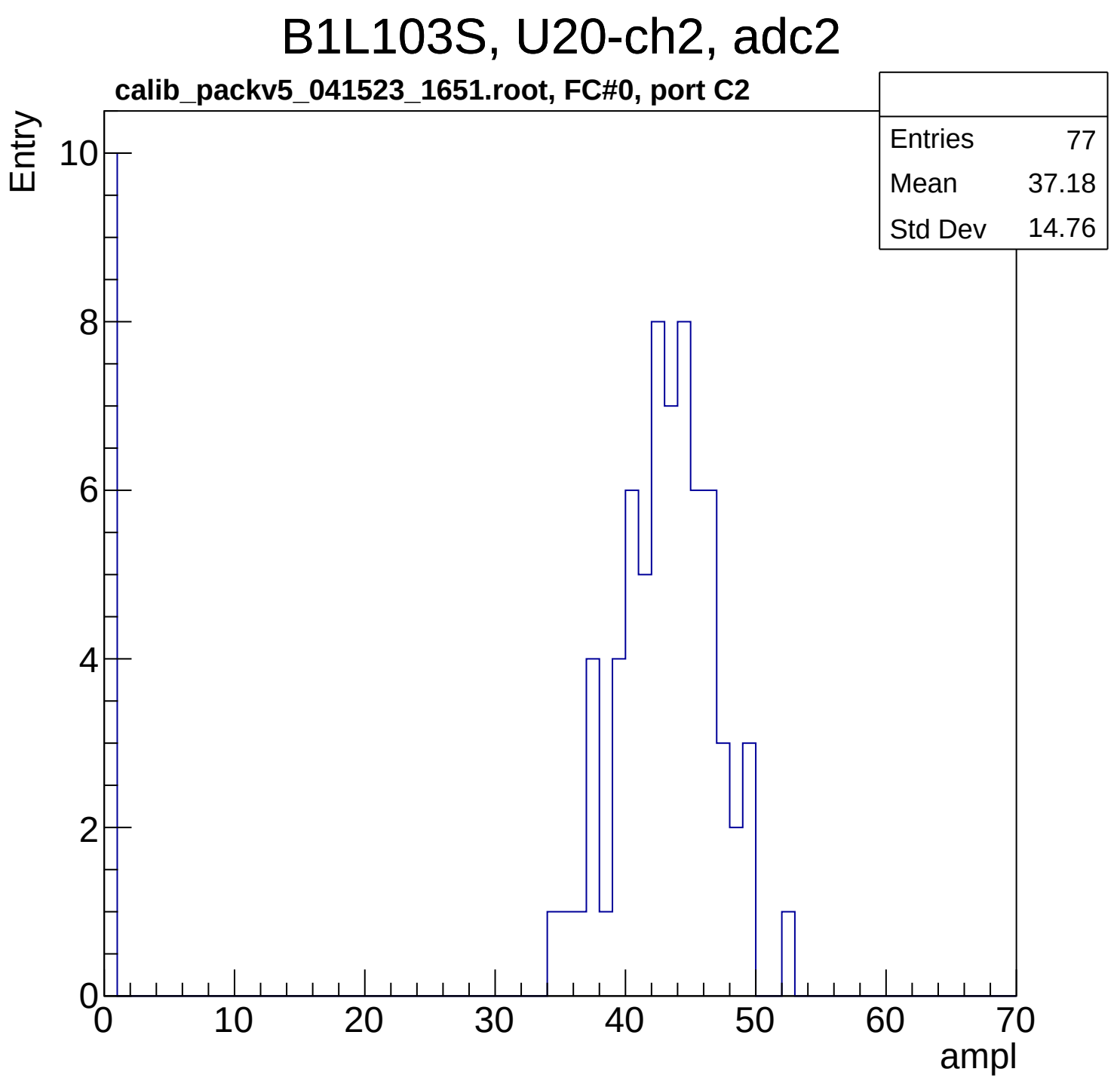
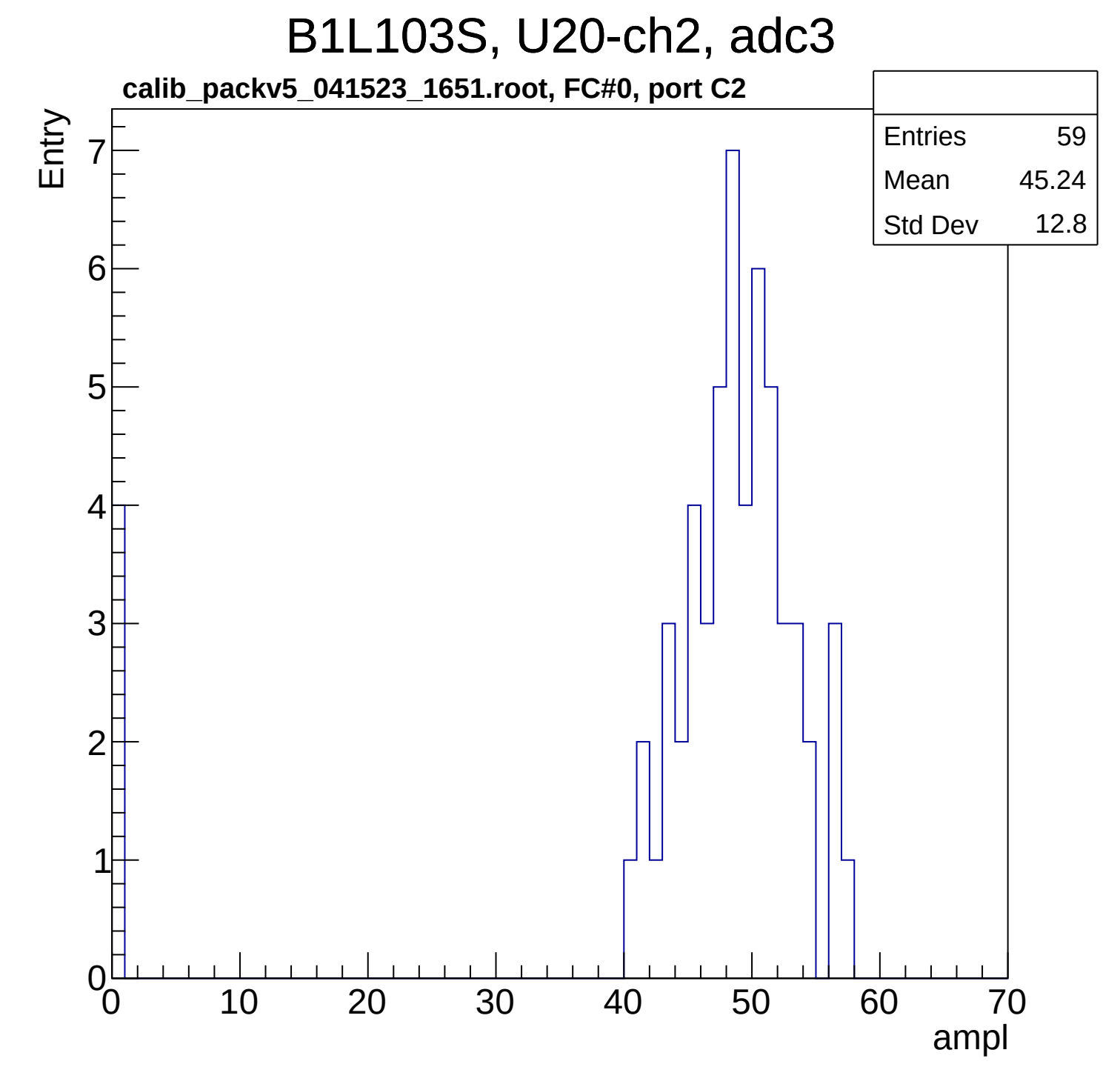
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch2, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 37.18
Std Dev 14.76
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch2, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 45.24
Std Dev 12.8
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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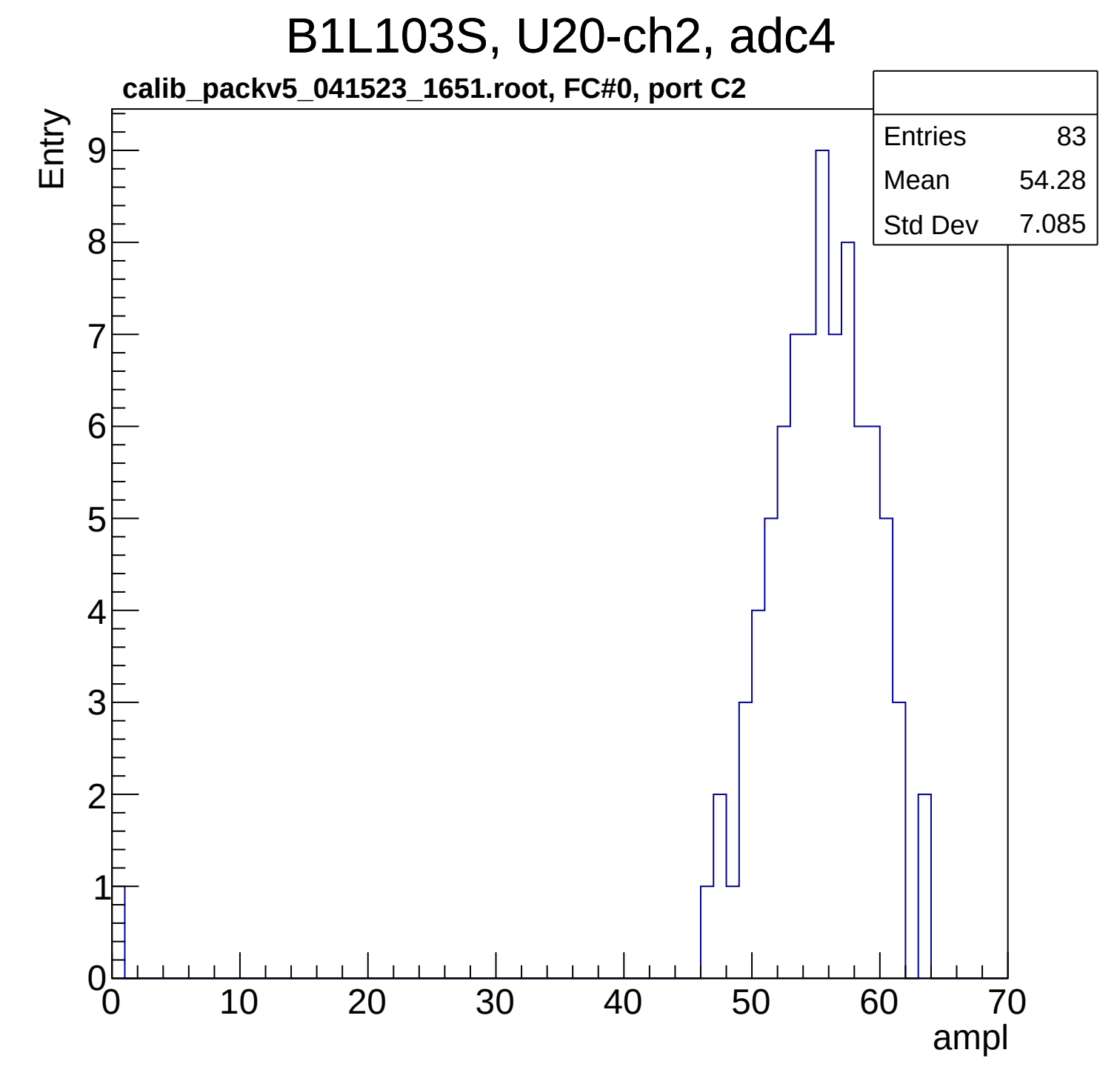
40
50
60
70


B1L103S, U20-ch2, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 54.28
Std Dev 7.085
Entry
ampl
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2
3
4
5
6
7
8
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0
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50
60
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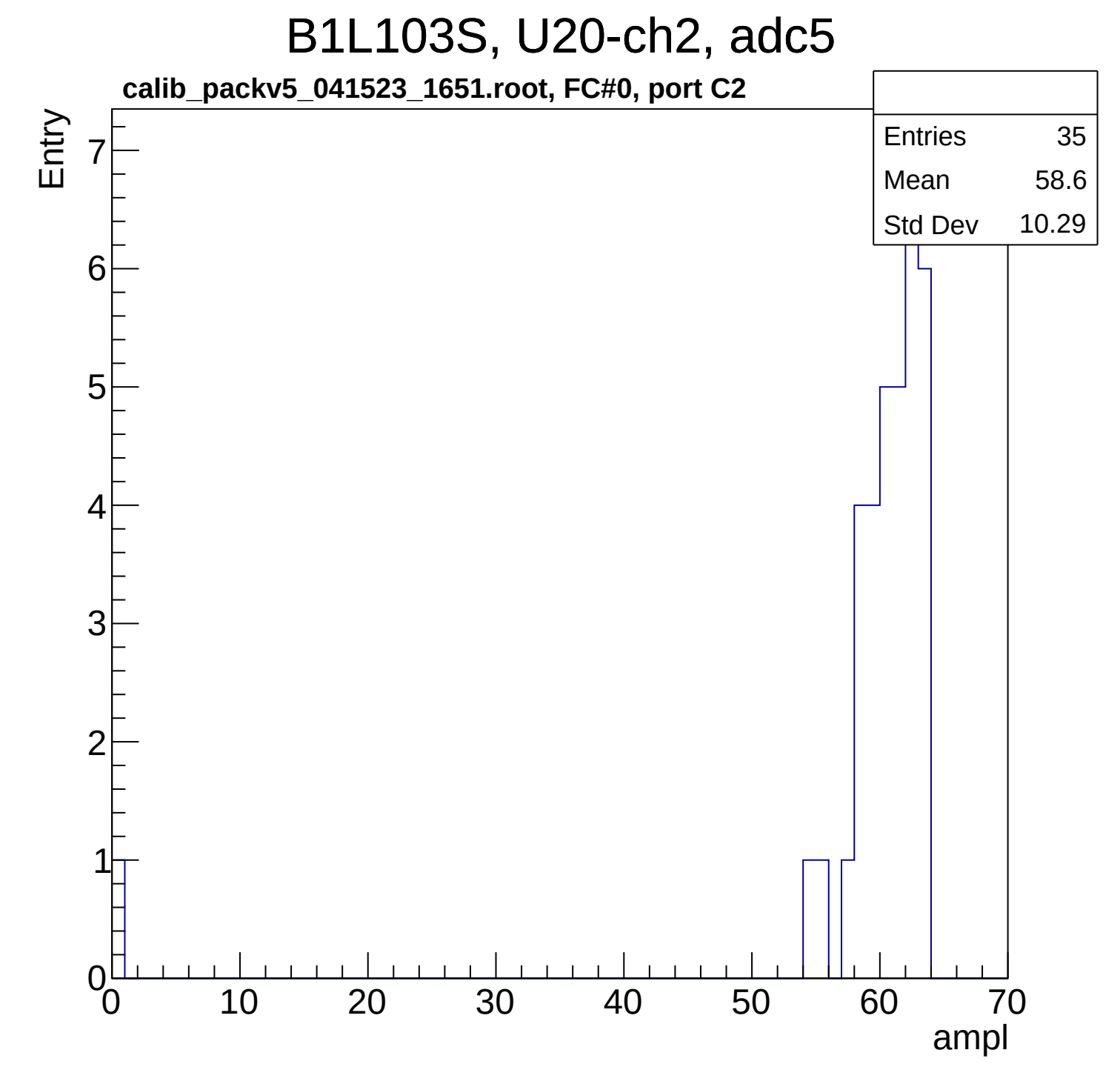
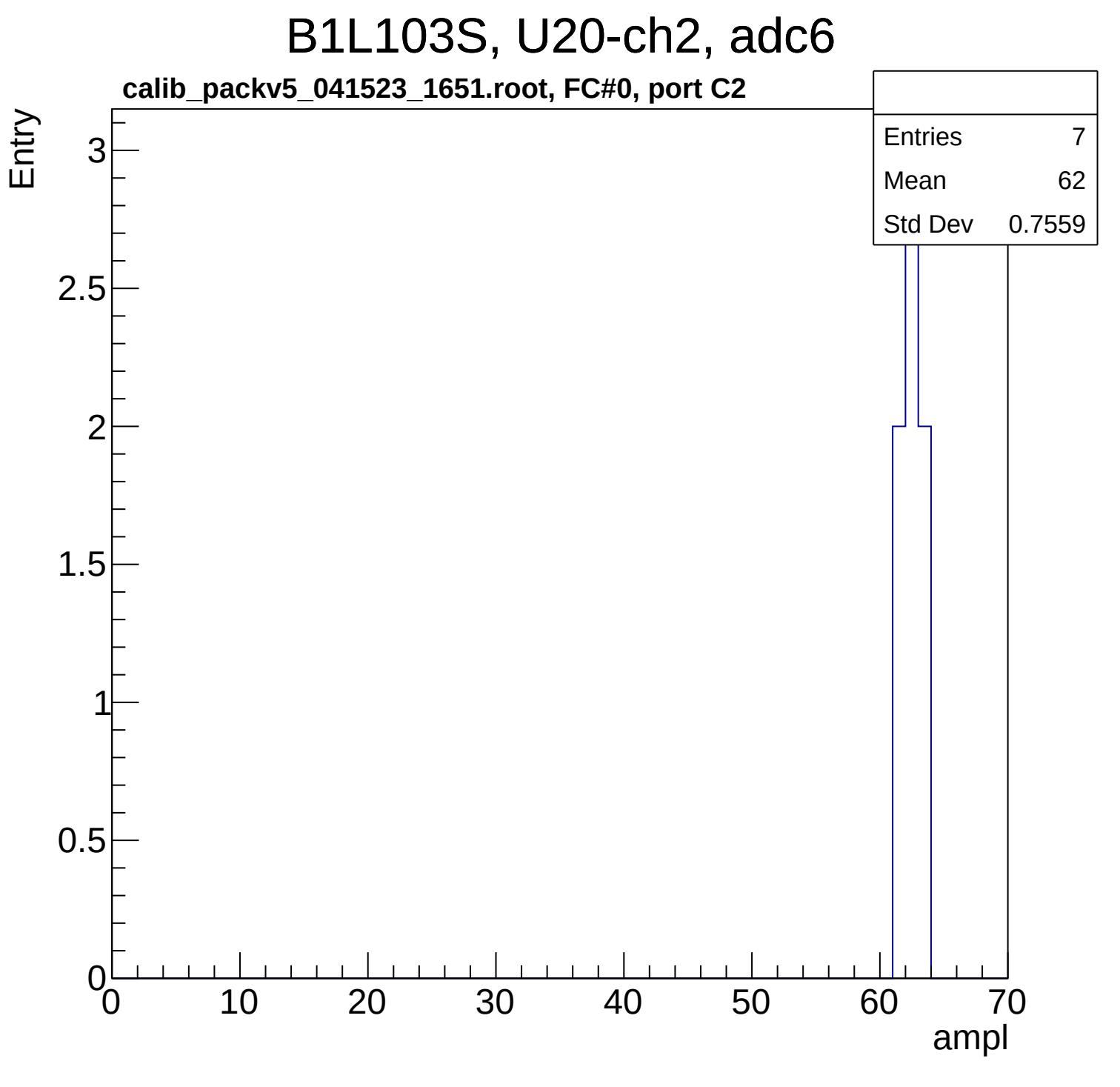

B1L103S, U20-ch2, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 58.6
Std Dev 10.29
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U20-ch2, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 62
Std Dev 0.7559
Entry
ampl
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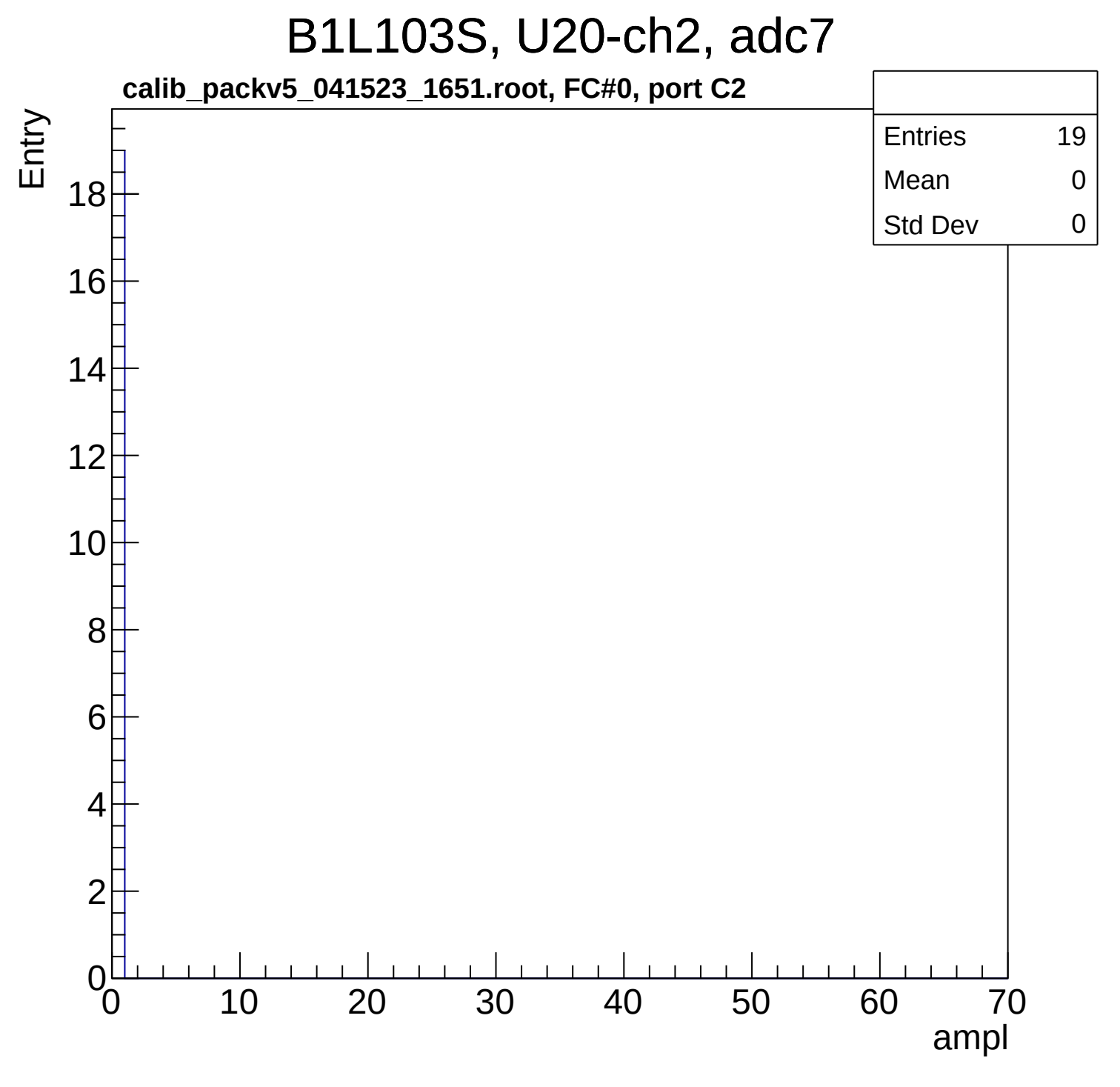
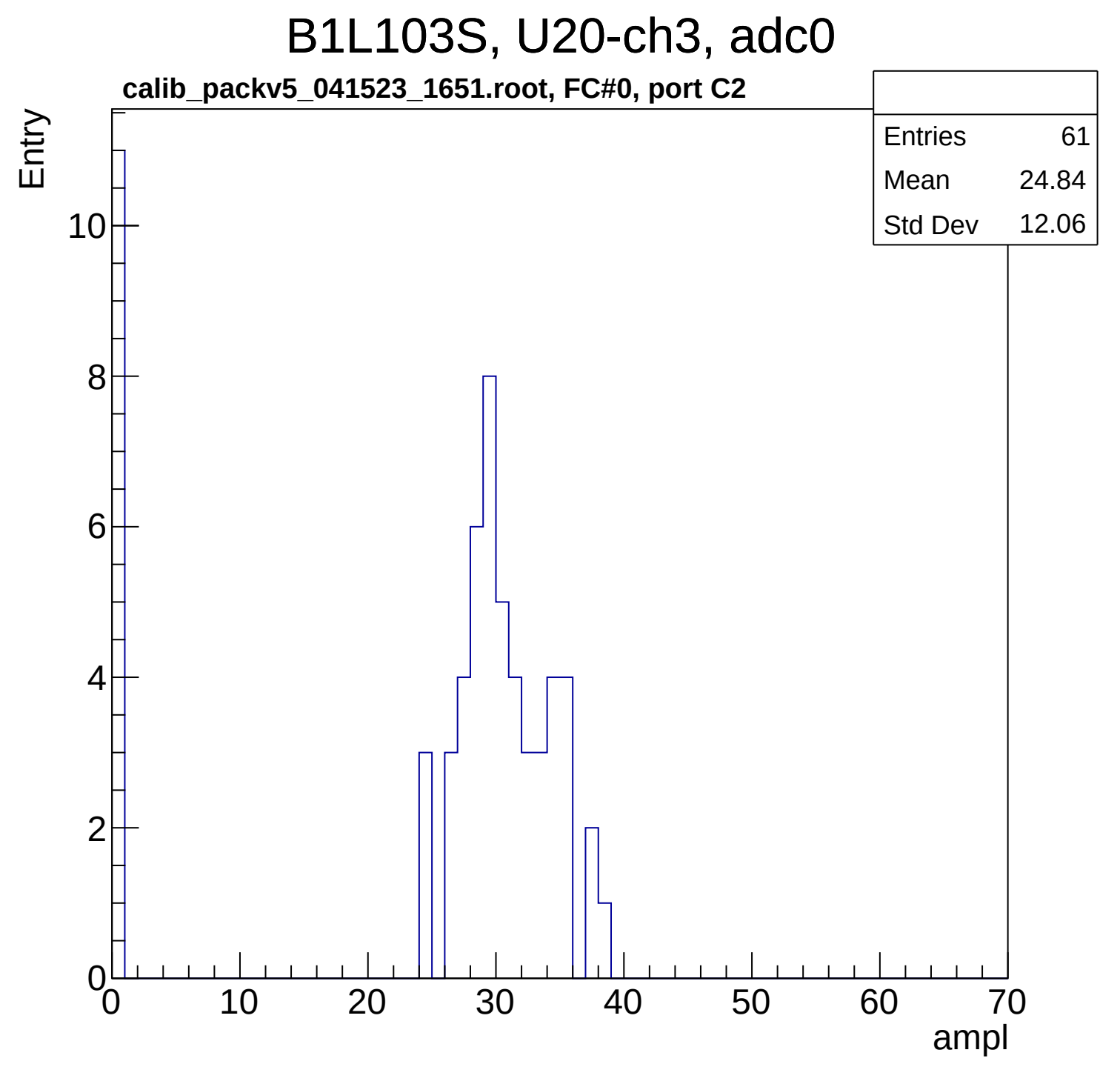
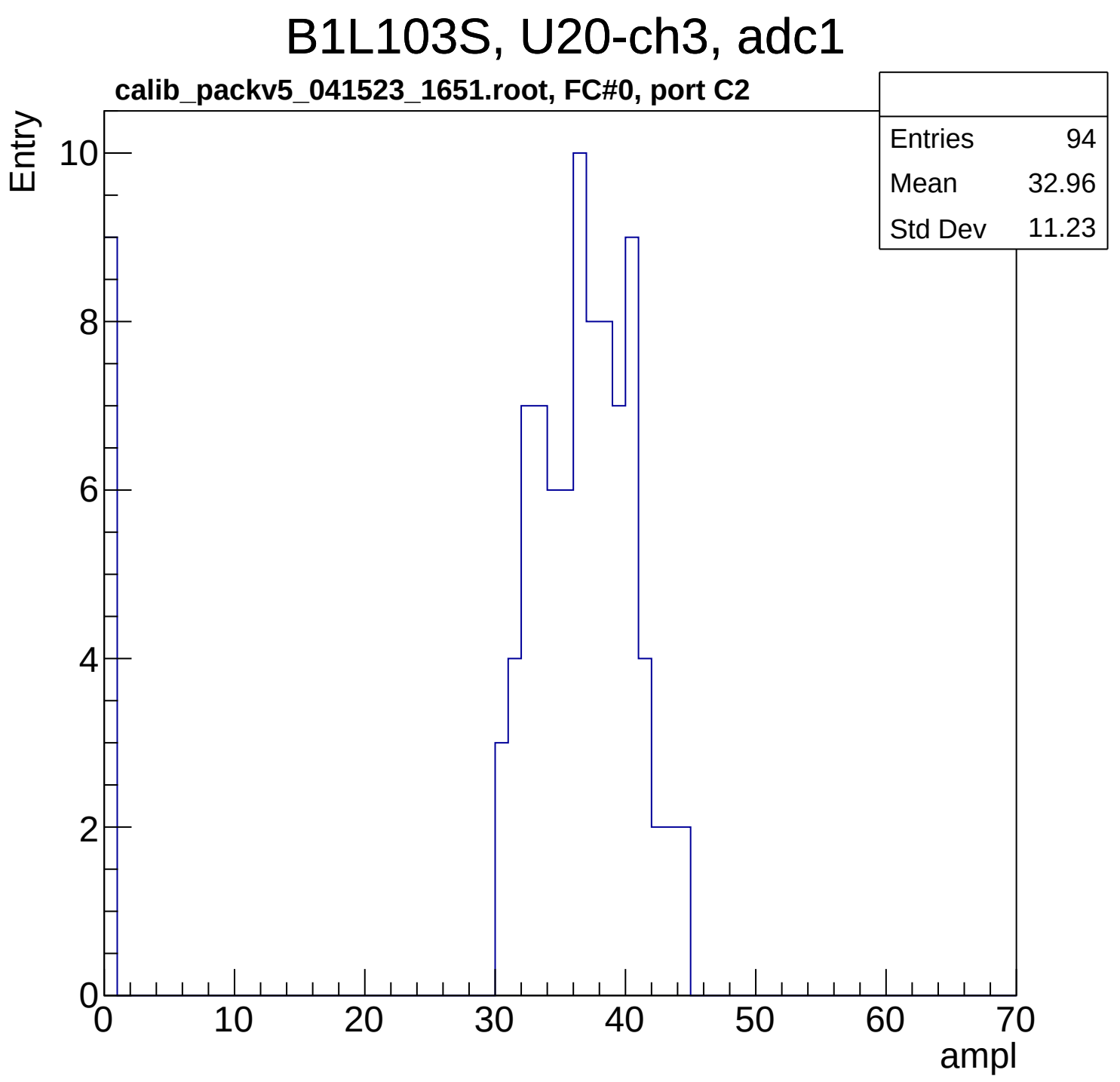
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U20-ch2, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch3, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 24.84
Std Dev 12.06
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch3, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 32.96
Std Dev 11.23
Entry
0
2
4
6
8
10
0
10
20
30
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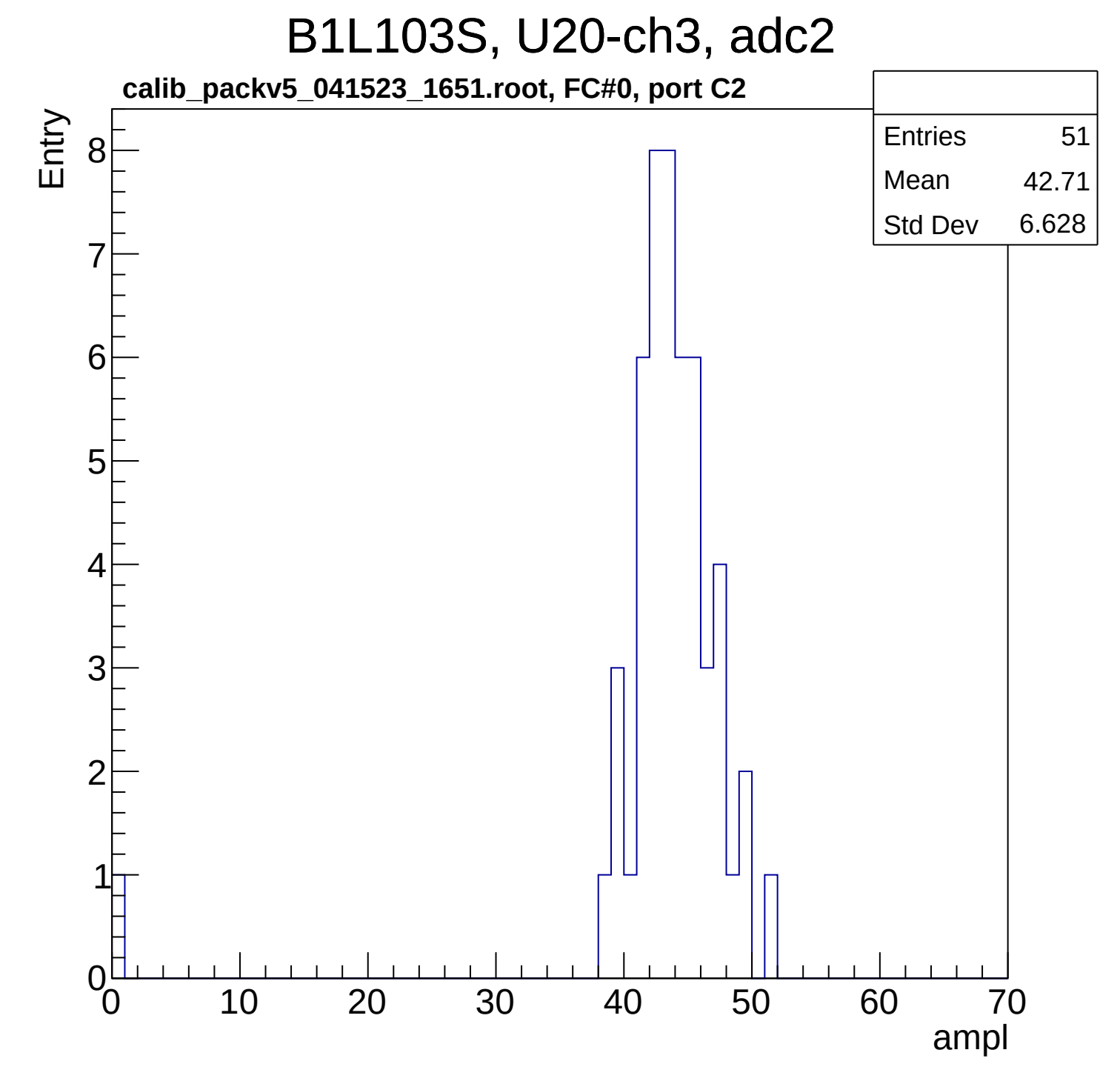
50
60
70
ampl


B1L103S, U20-ch3, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 42.71
Std Dev 6.628
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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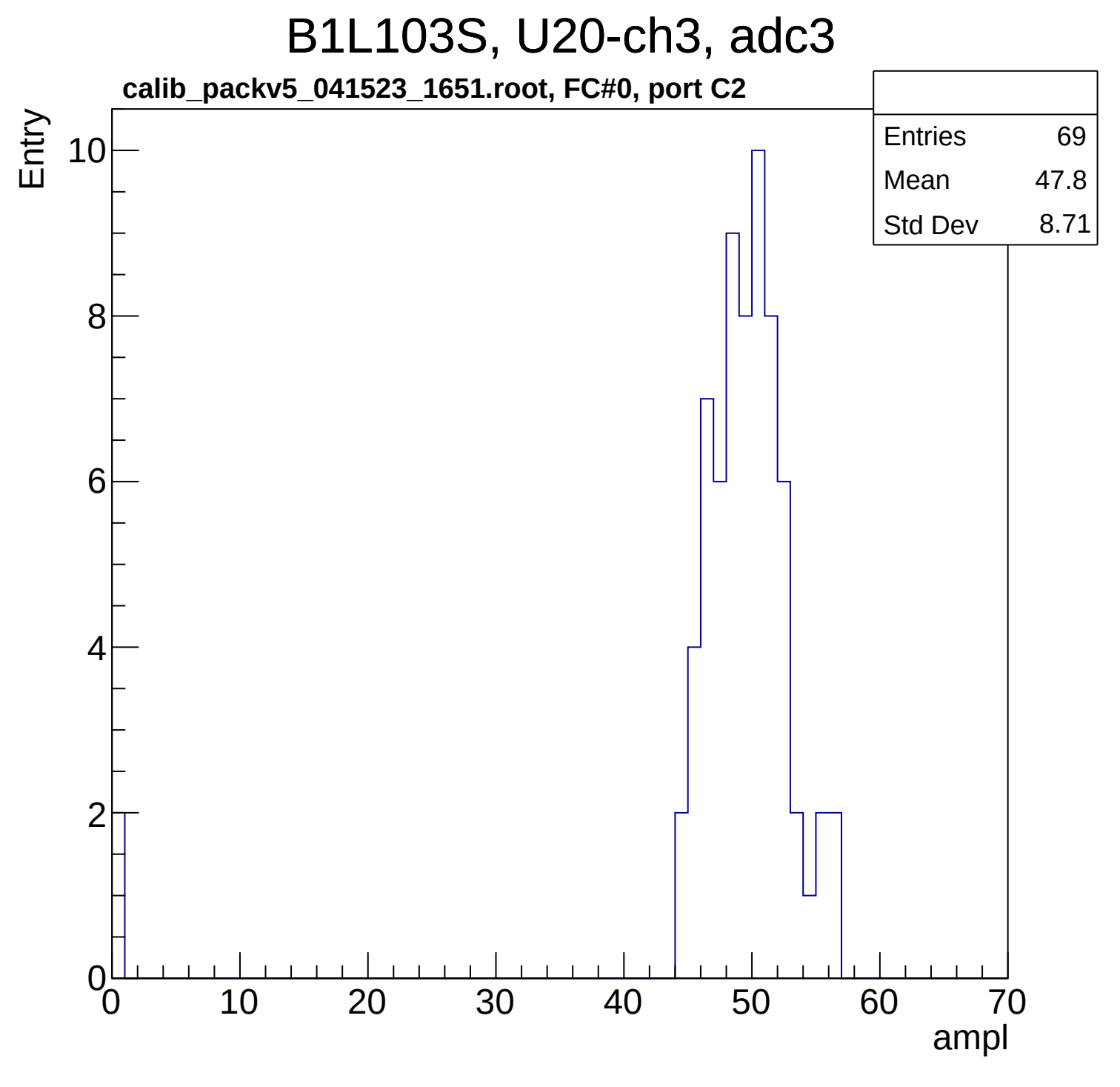
40
50
60
70


B1L103S, U20-ch3, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 47.8
Std Dev 8.71
Entry
ampl
0
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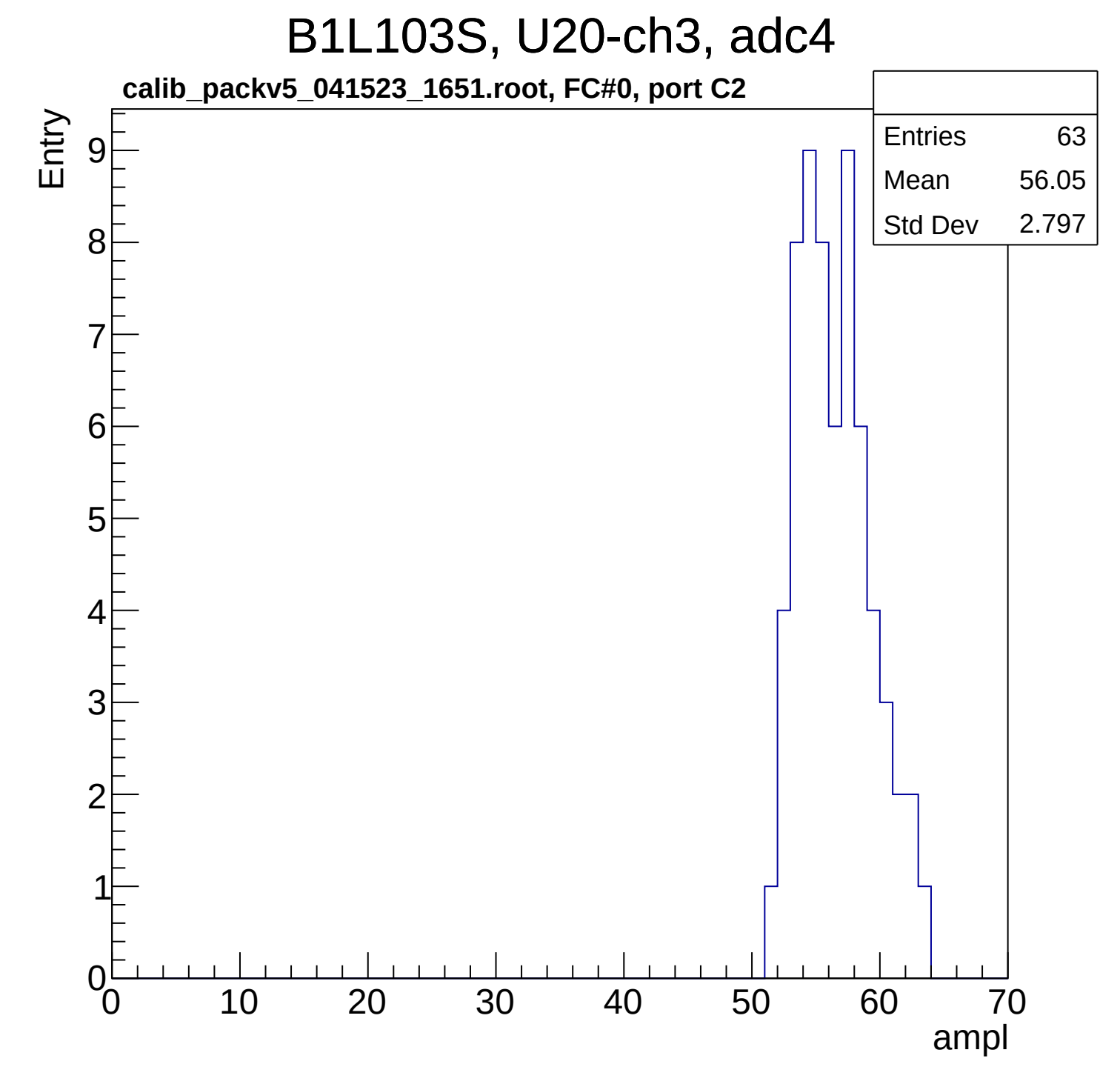
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U20-ch3, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 56.05
Std Dev 2.797
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
10
20
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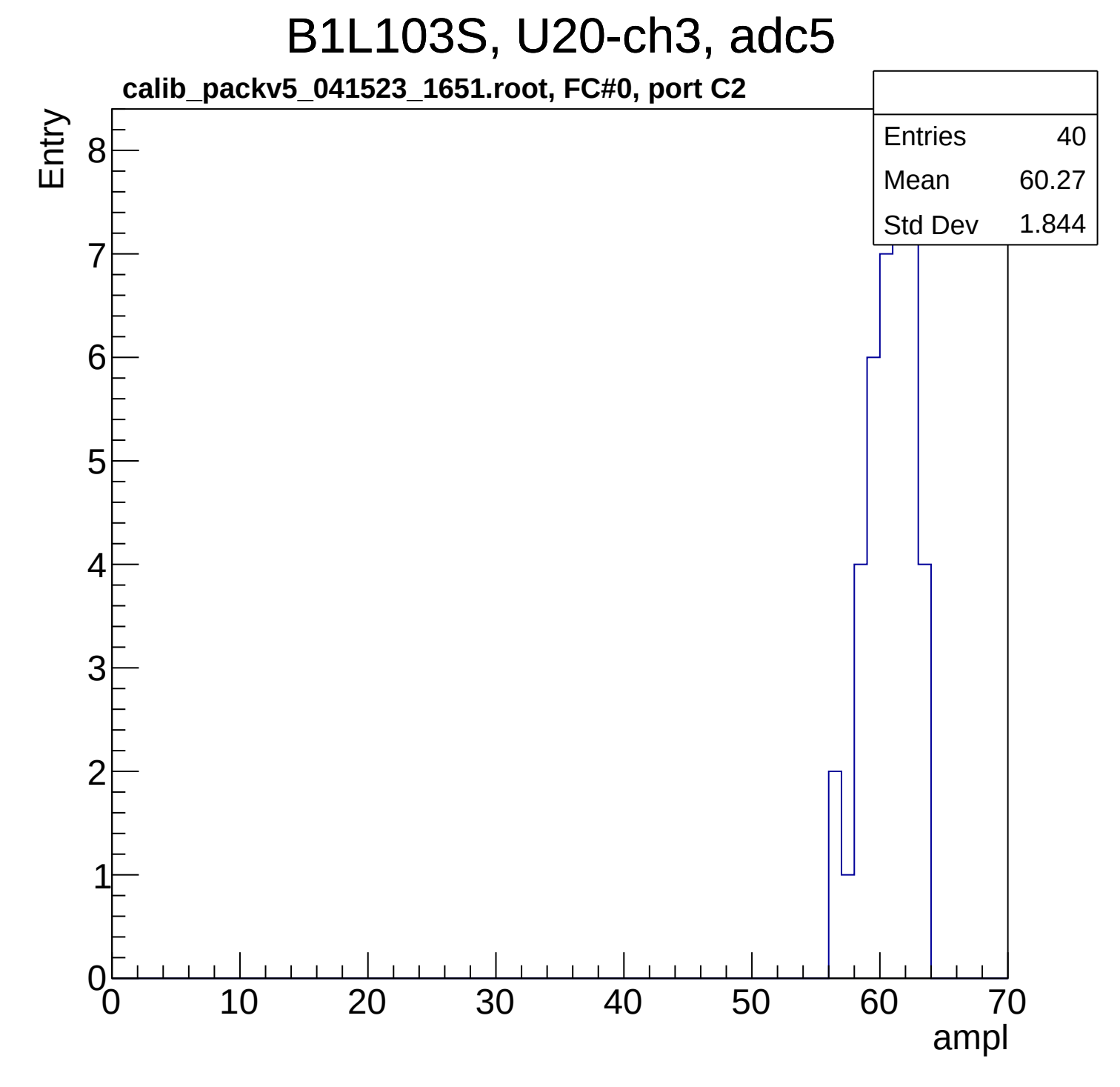
40
50
60
70


B1L103S, U20-ch3, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 60.27
Std Dev 1.844
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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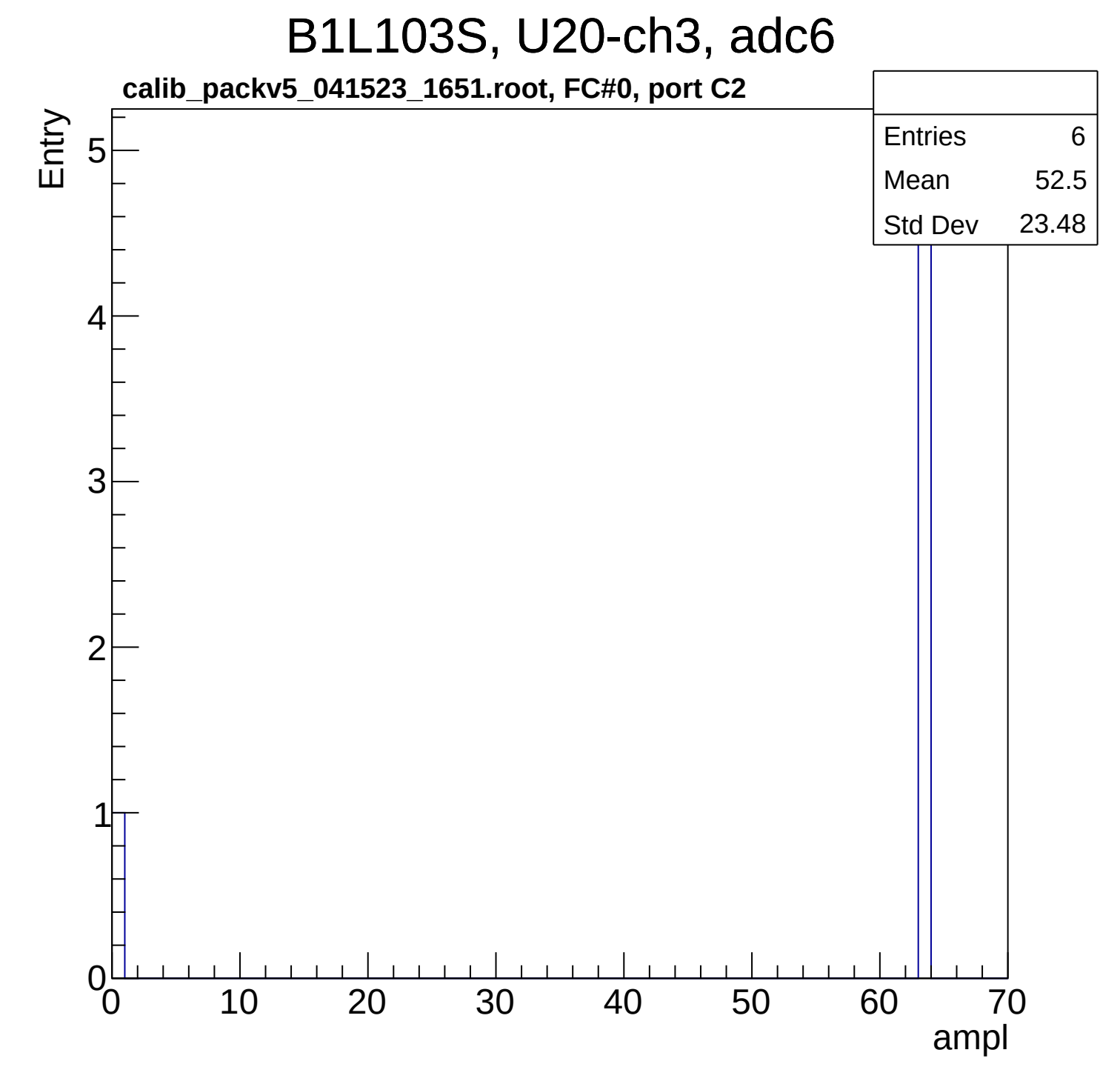
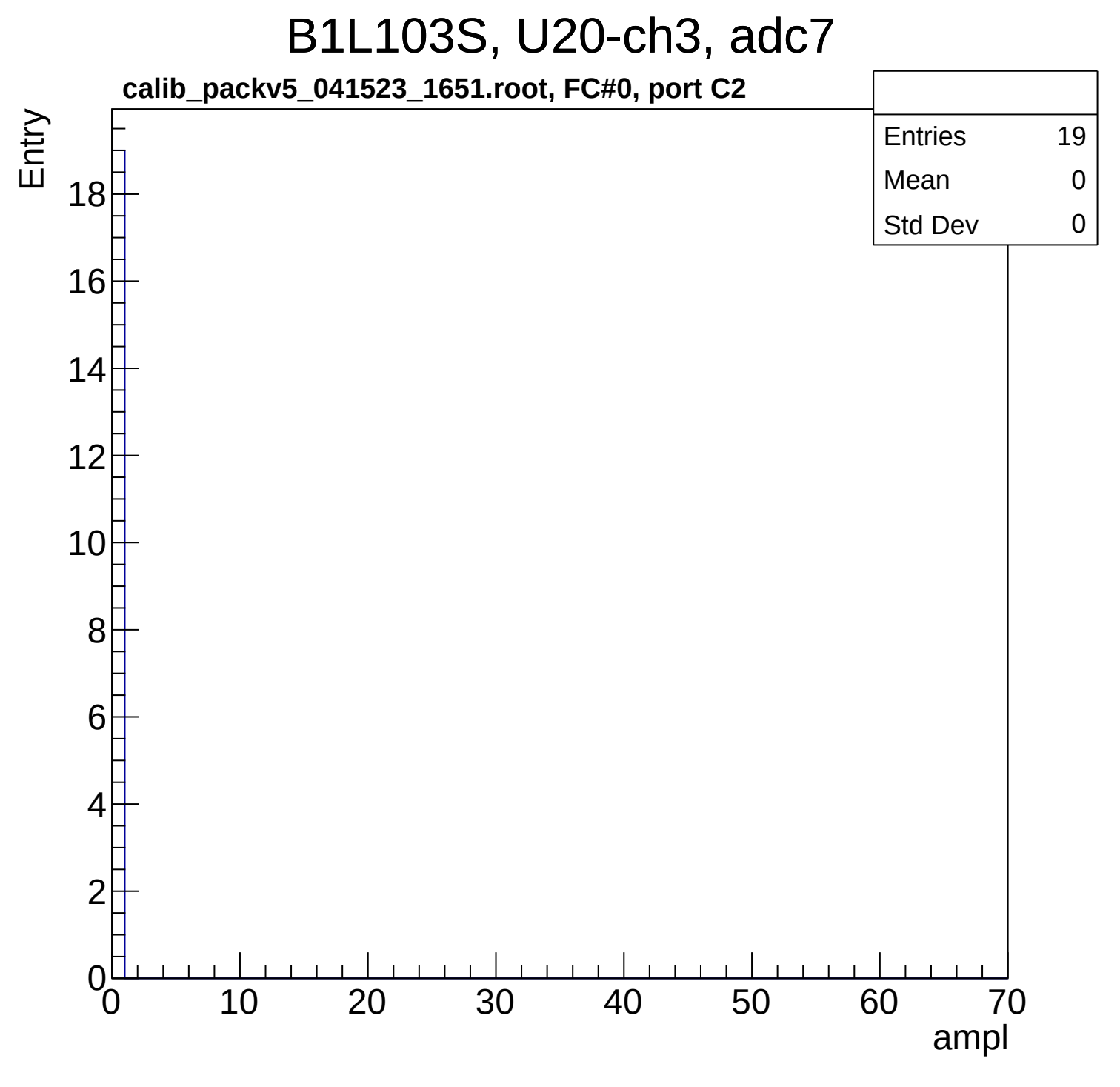
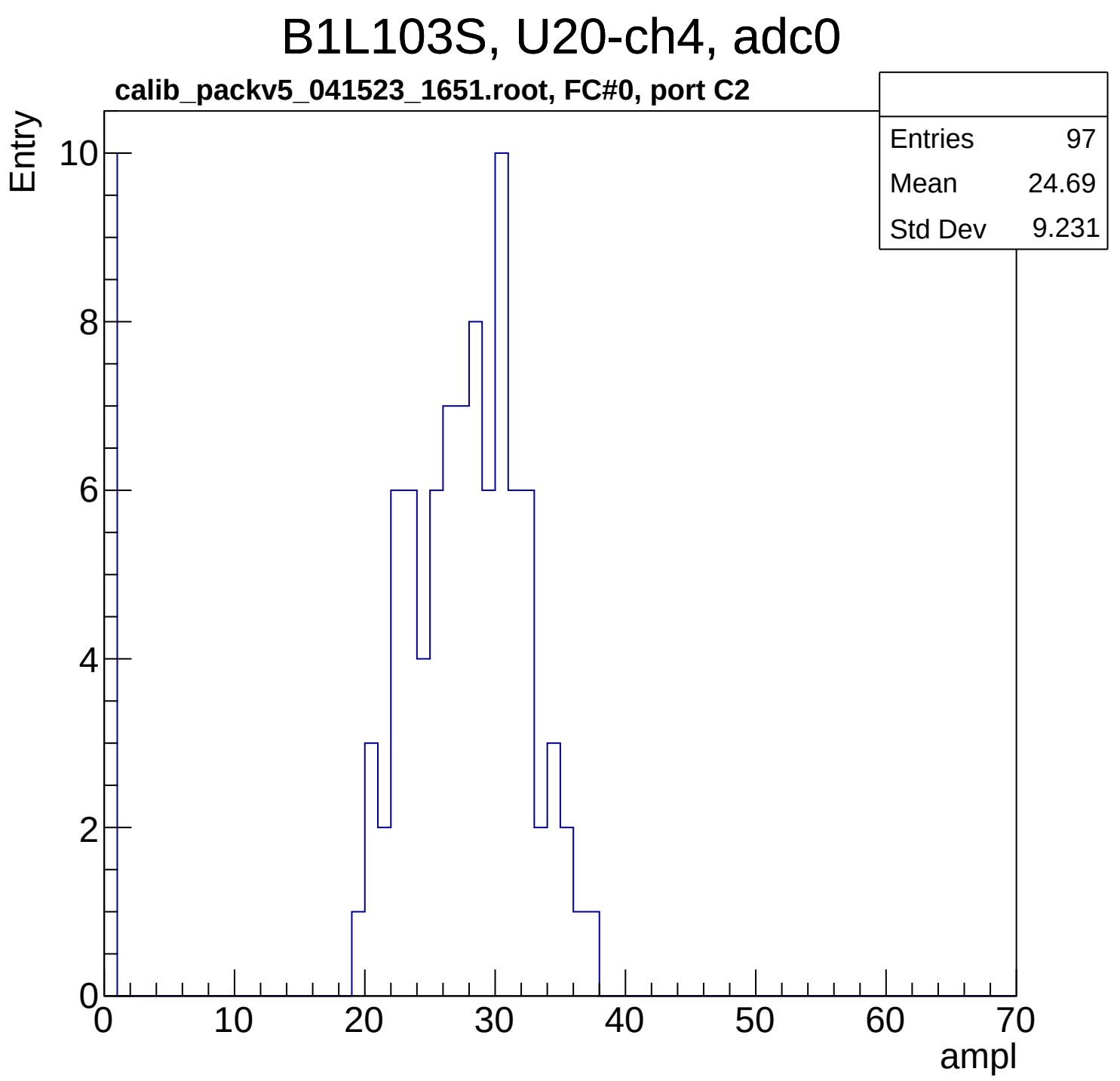
60
70


B1L103S, U20-ch3, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 52.5
Std Dev 23.48
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch3, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch4, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 24.69
Std Dev 9.231
Entry
ampl
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2
4
6
8
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0
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40
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60
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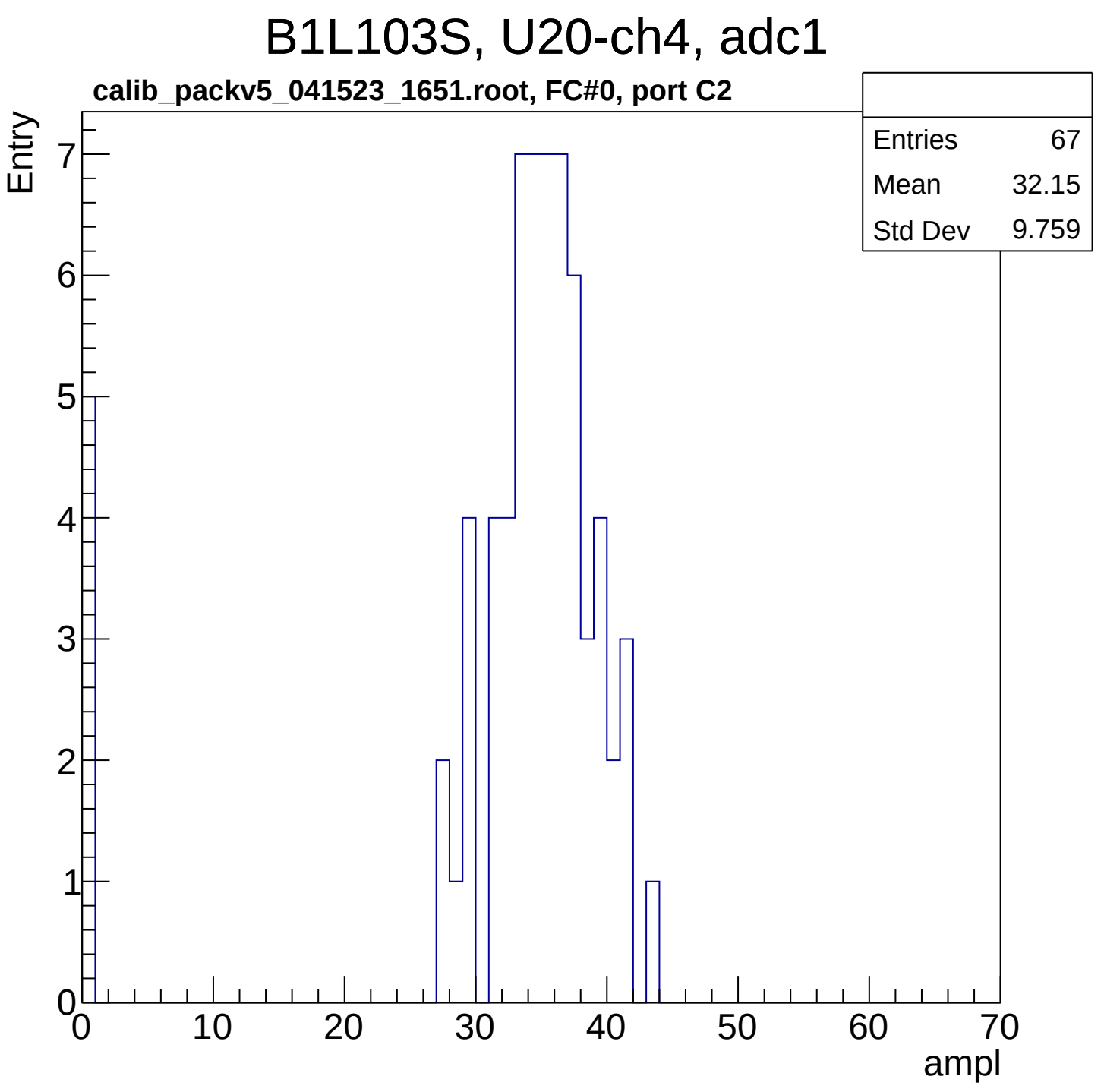
B1L103S, U20-ch4, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 32.15
Std Dev 9.759
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
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40
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60
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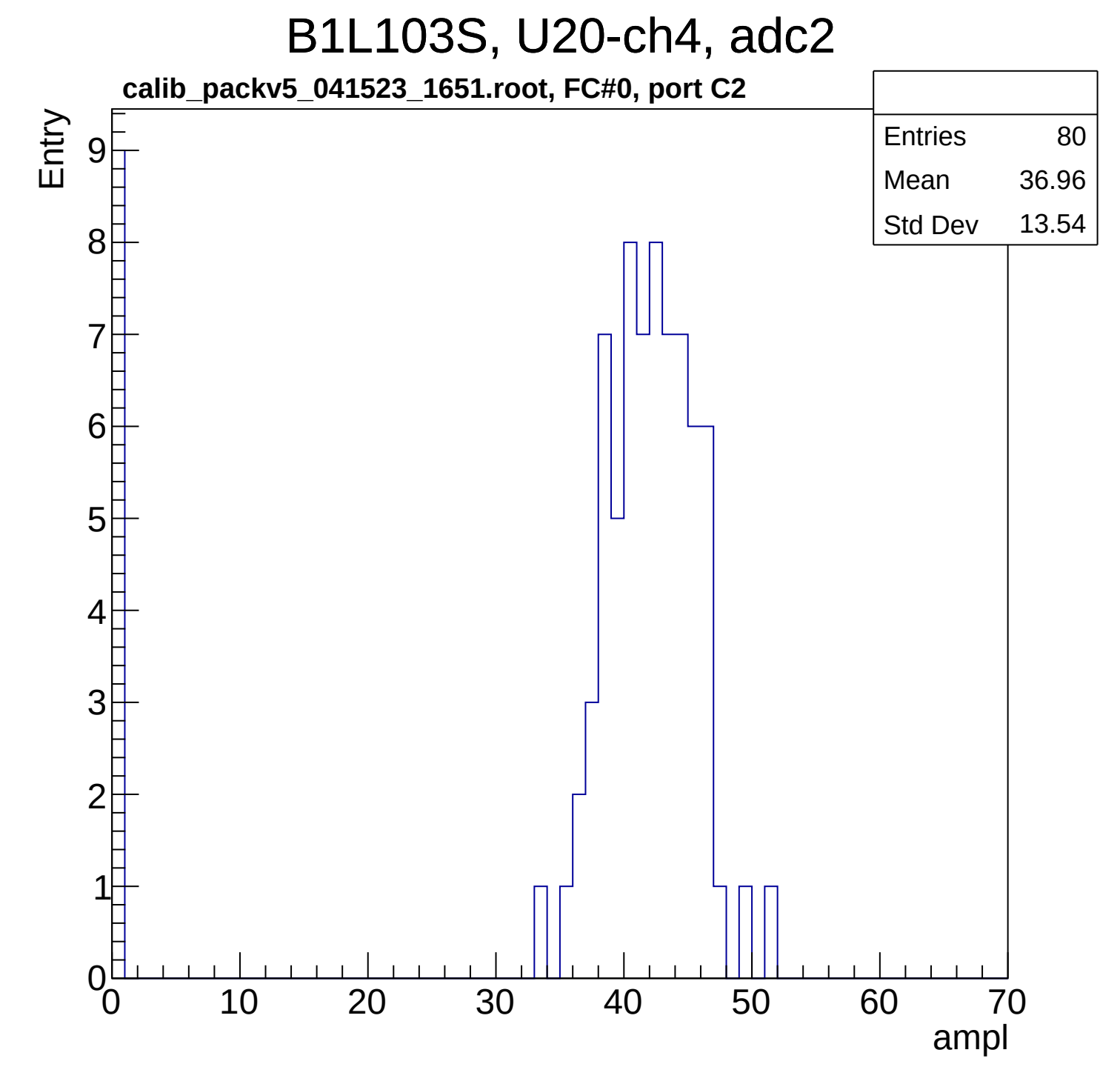
B1L103S, U20-ch4, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 36.96
Std Dev 13.54
Entry
ampl
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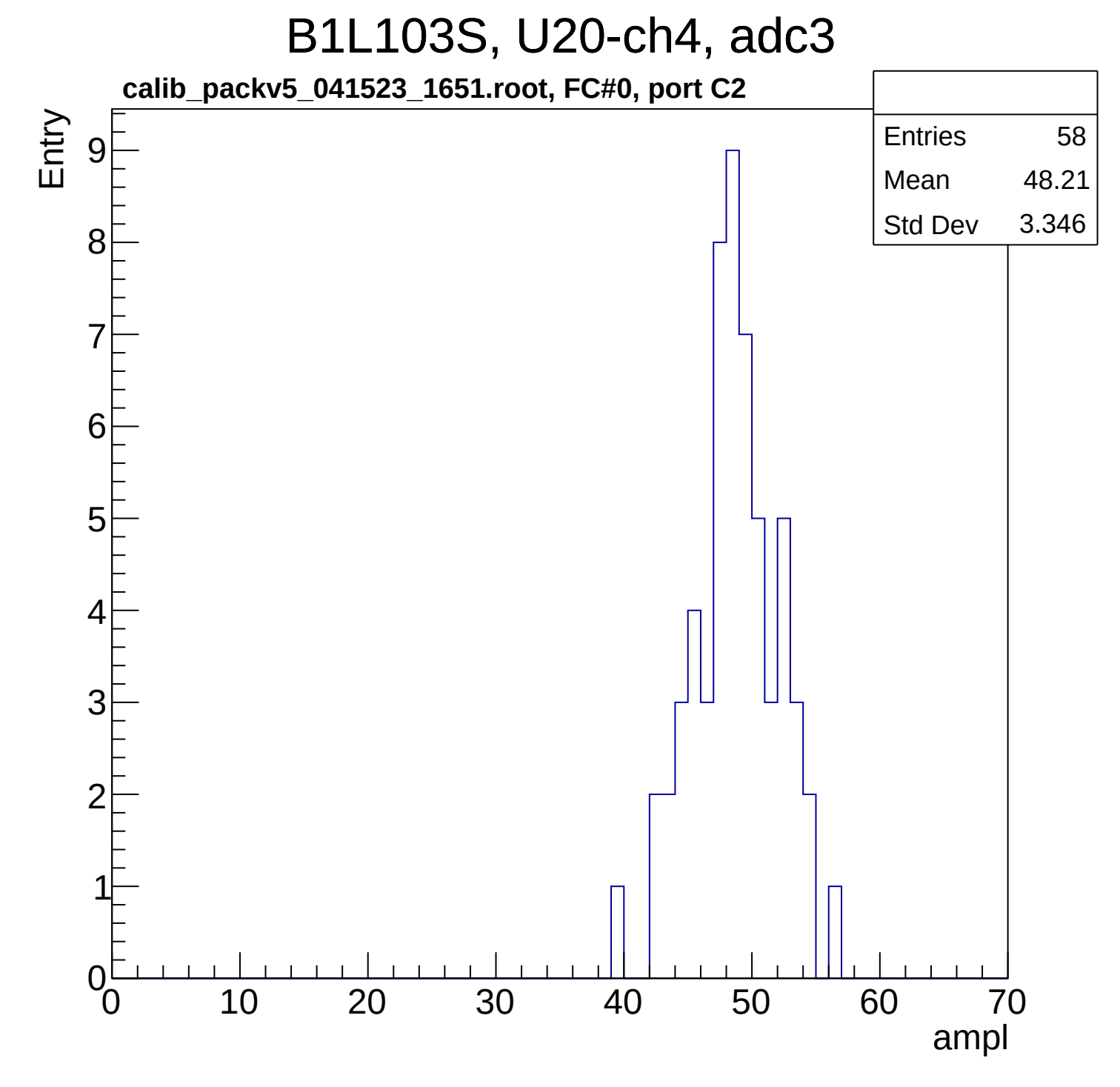
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch4, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 48.21
Std Dev 3.346
Entry
ampl
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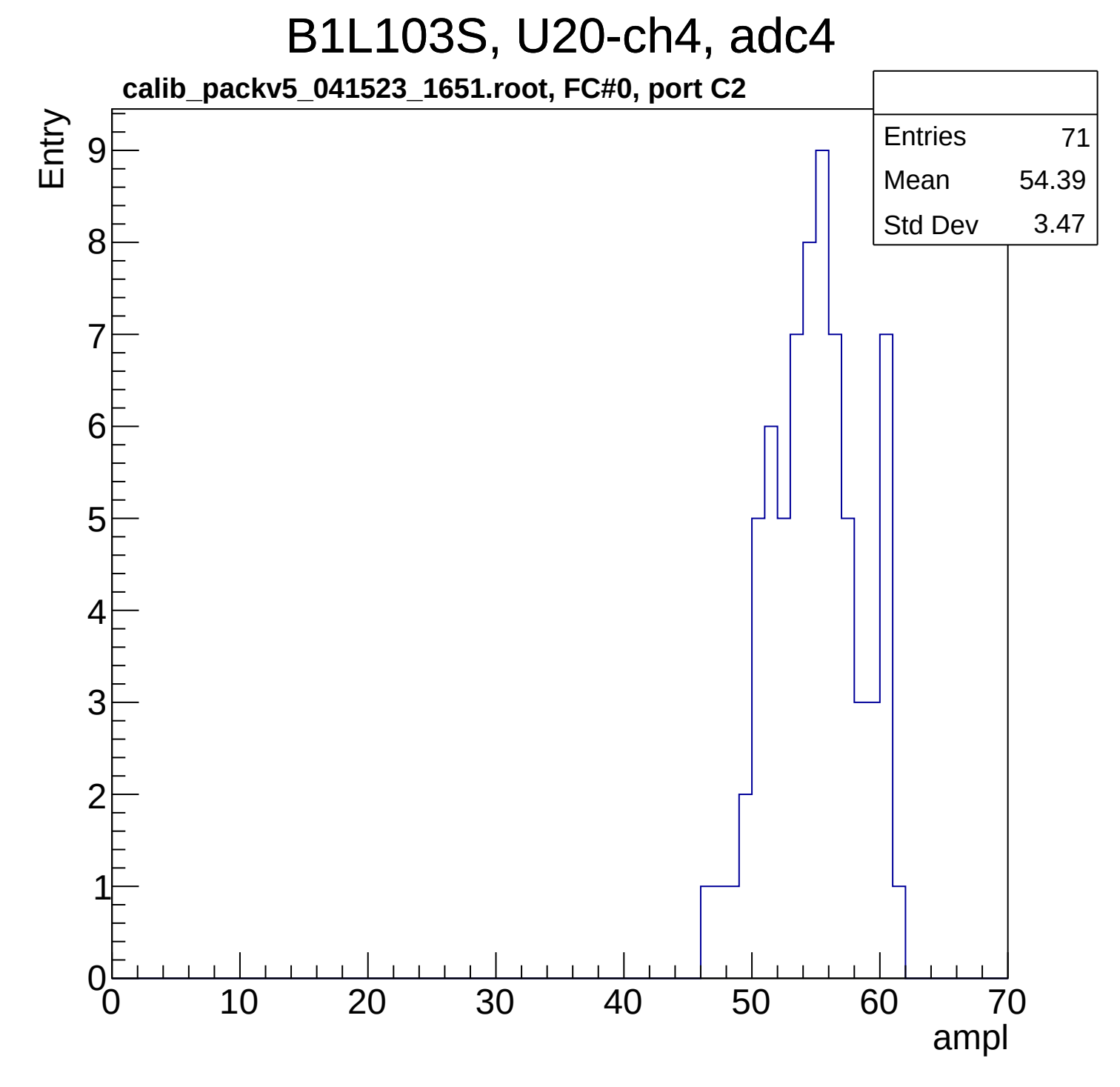
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch4, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 54.39
Std Dev 3.47
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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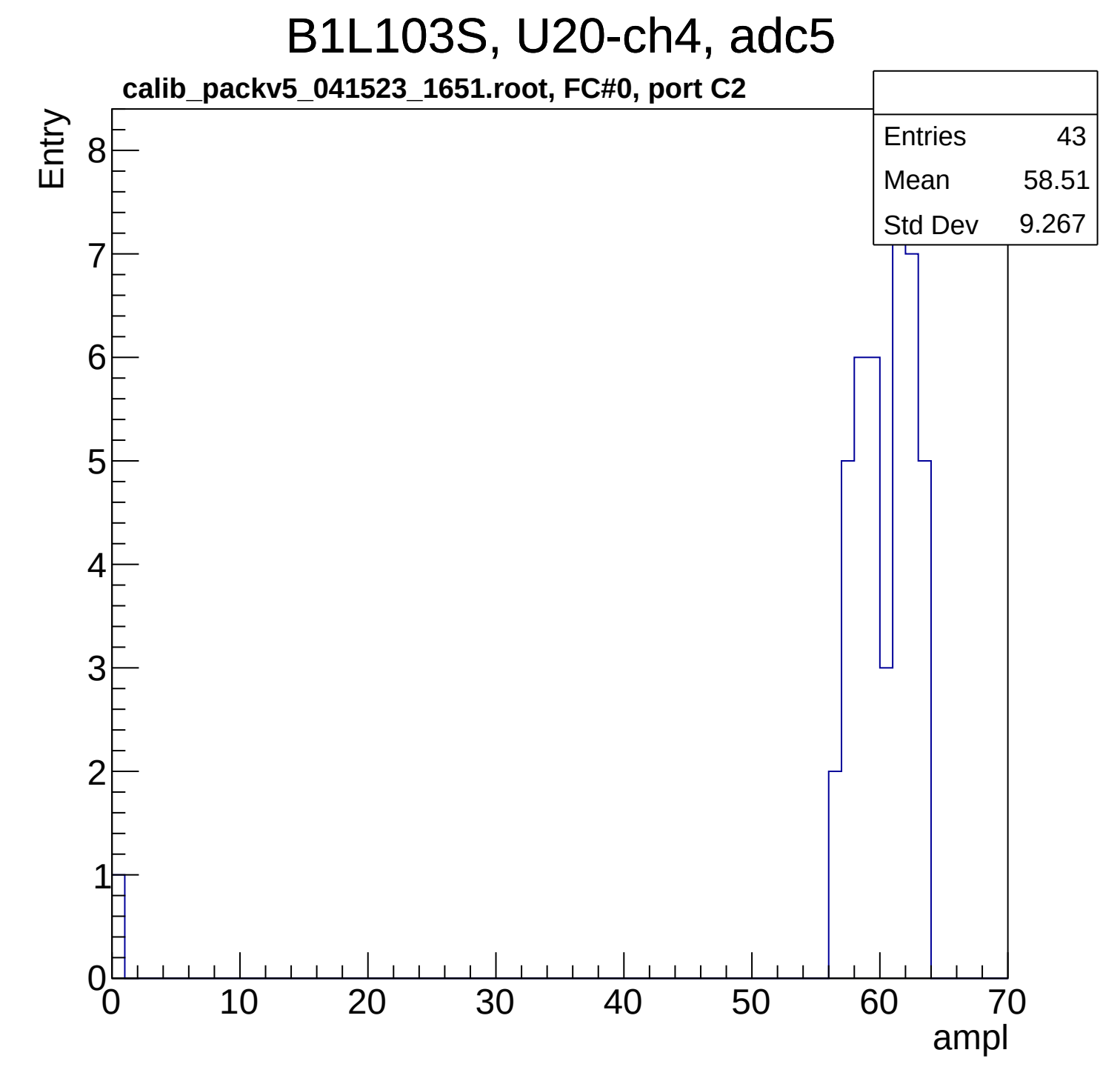
B1L103S, U20-ch4, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 58.51
Std Dev 9.267
Entry
ampl
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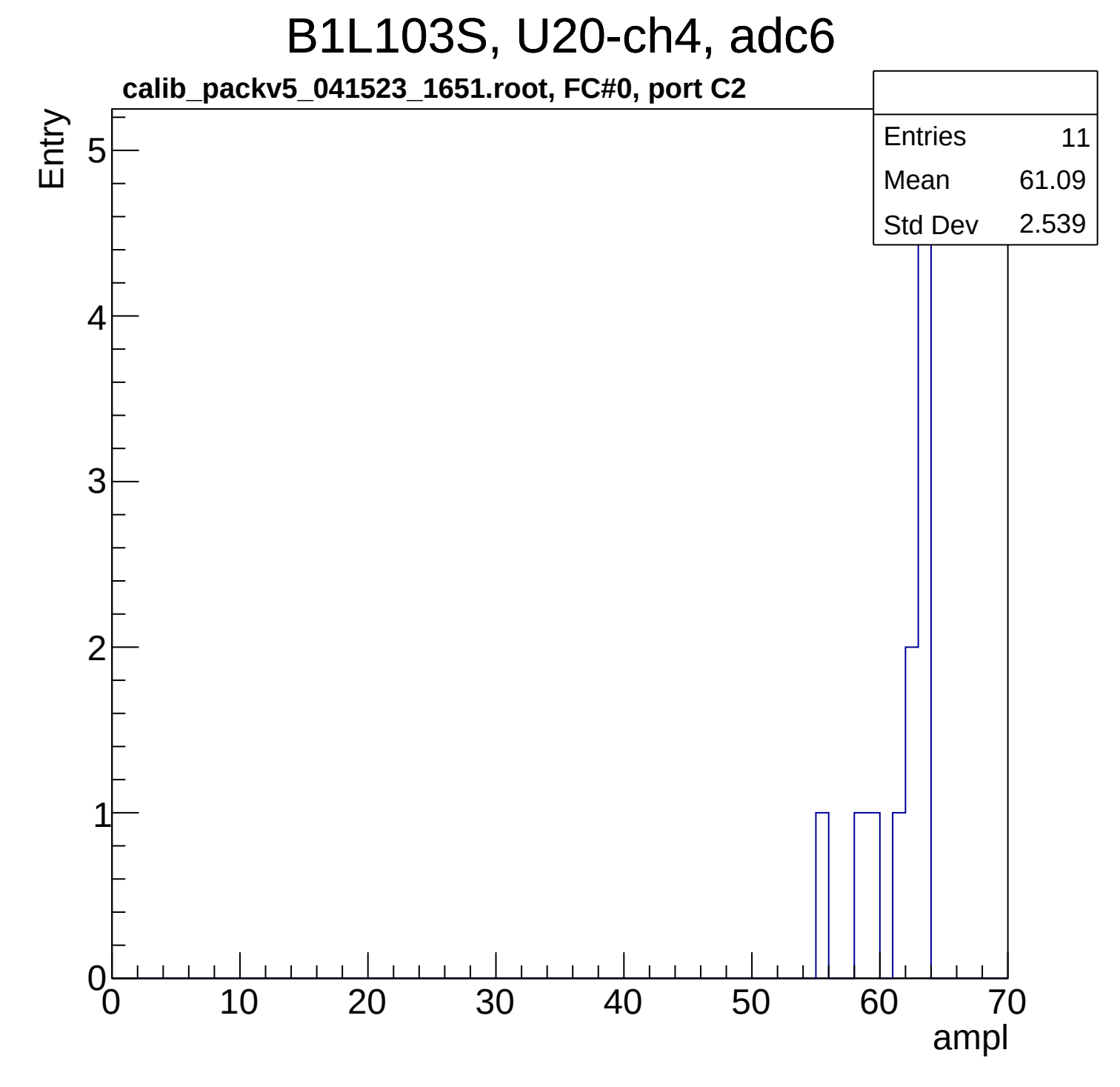
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch4, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 61.09
Std Dev 2.539
Entry
ampl
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2
3
4
5
0
10
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40
50
60
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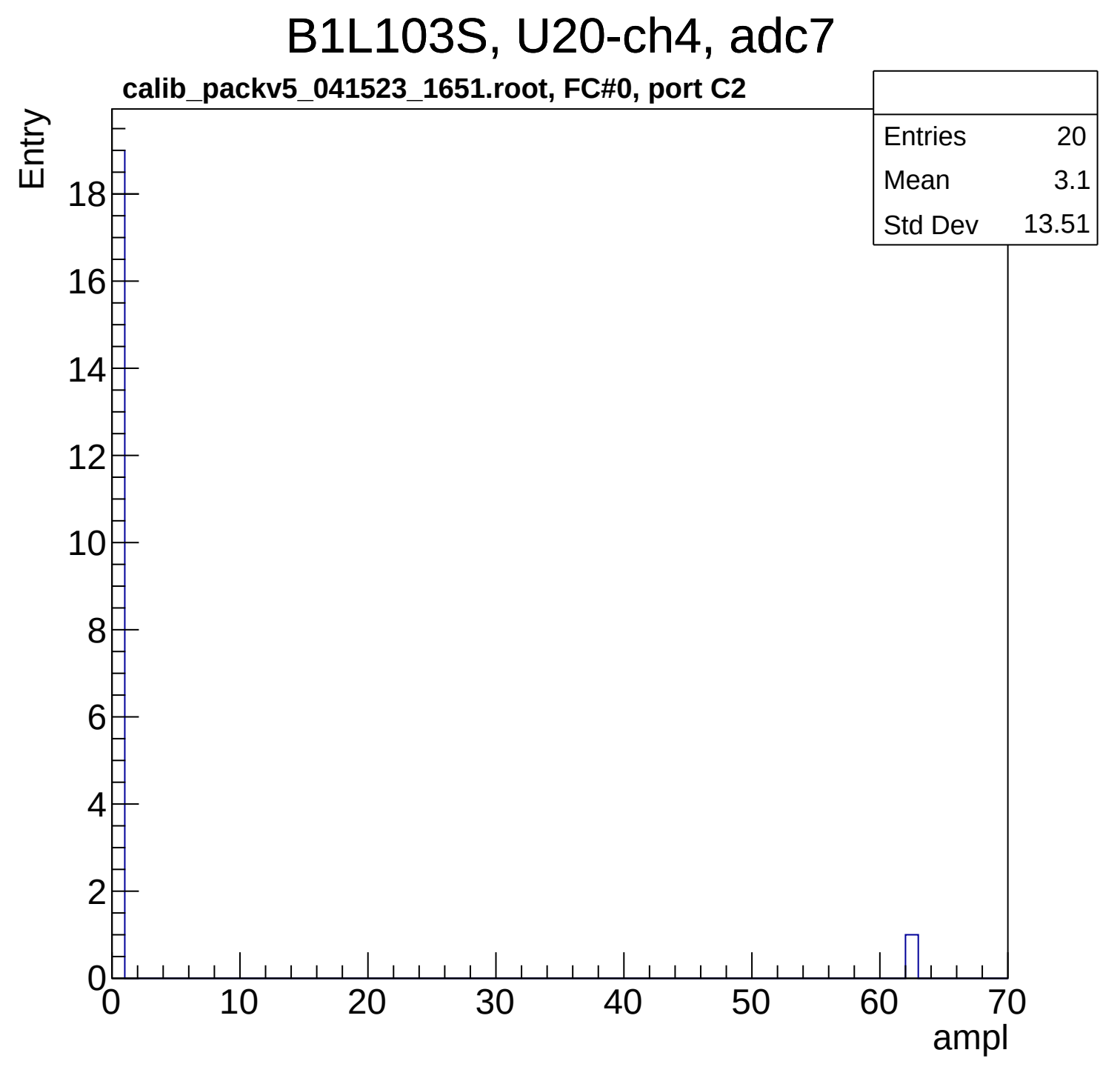
B1L103S, U20-ch4, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
ampl
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2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
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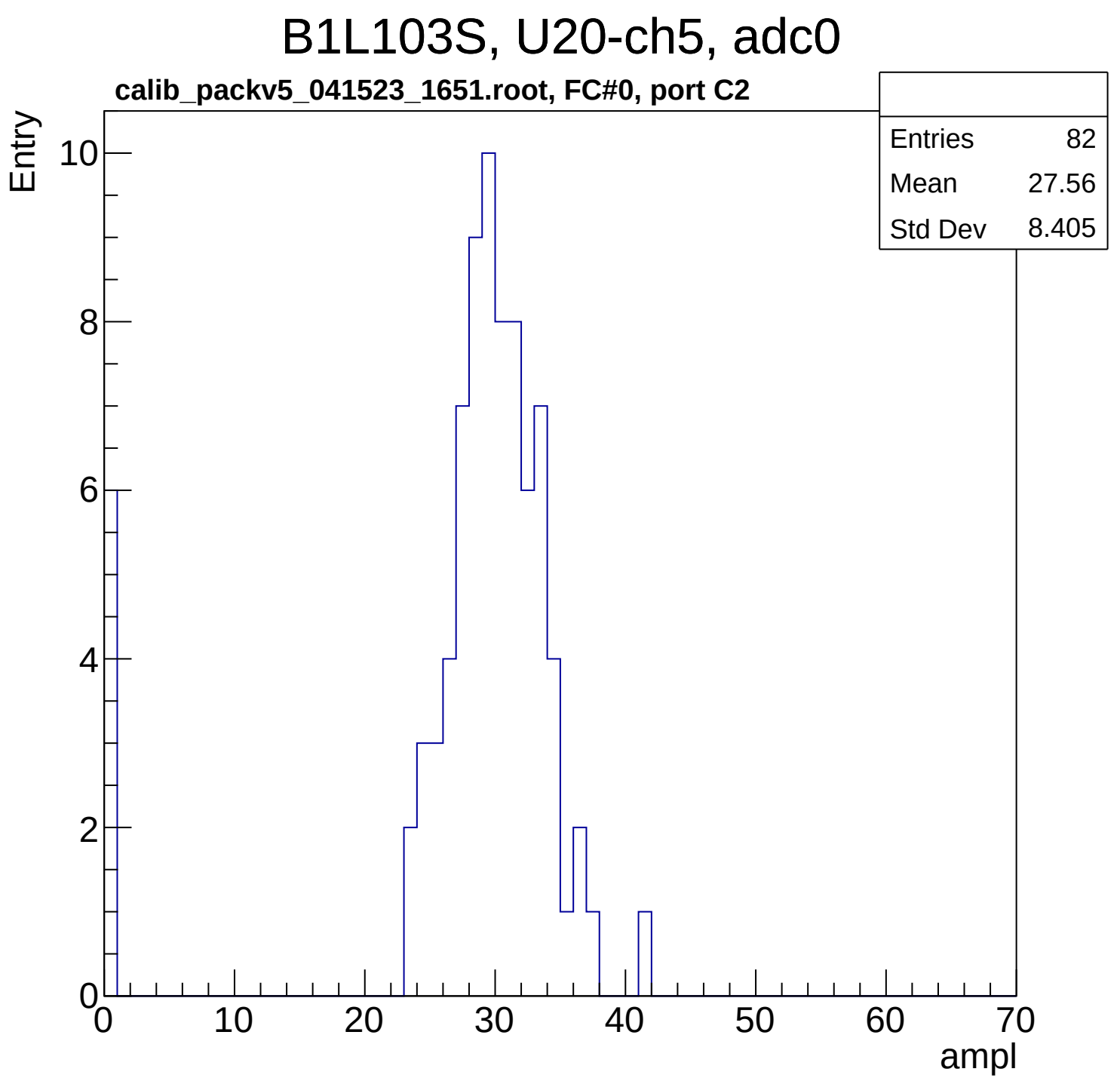
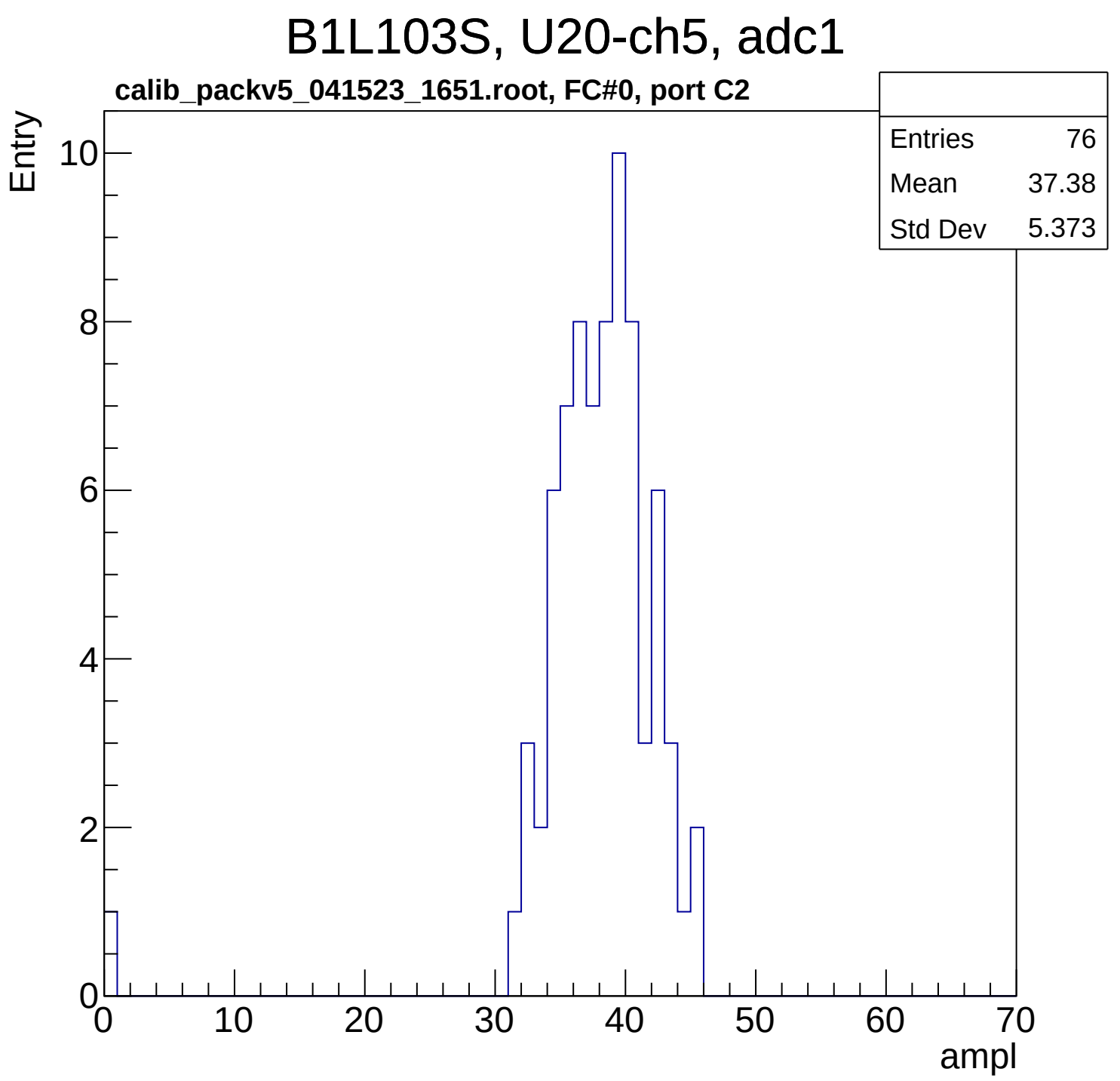
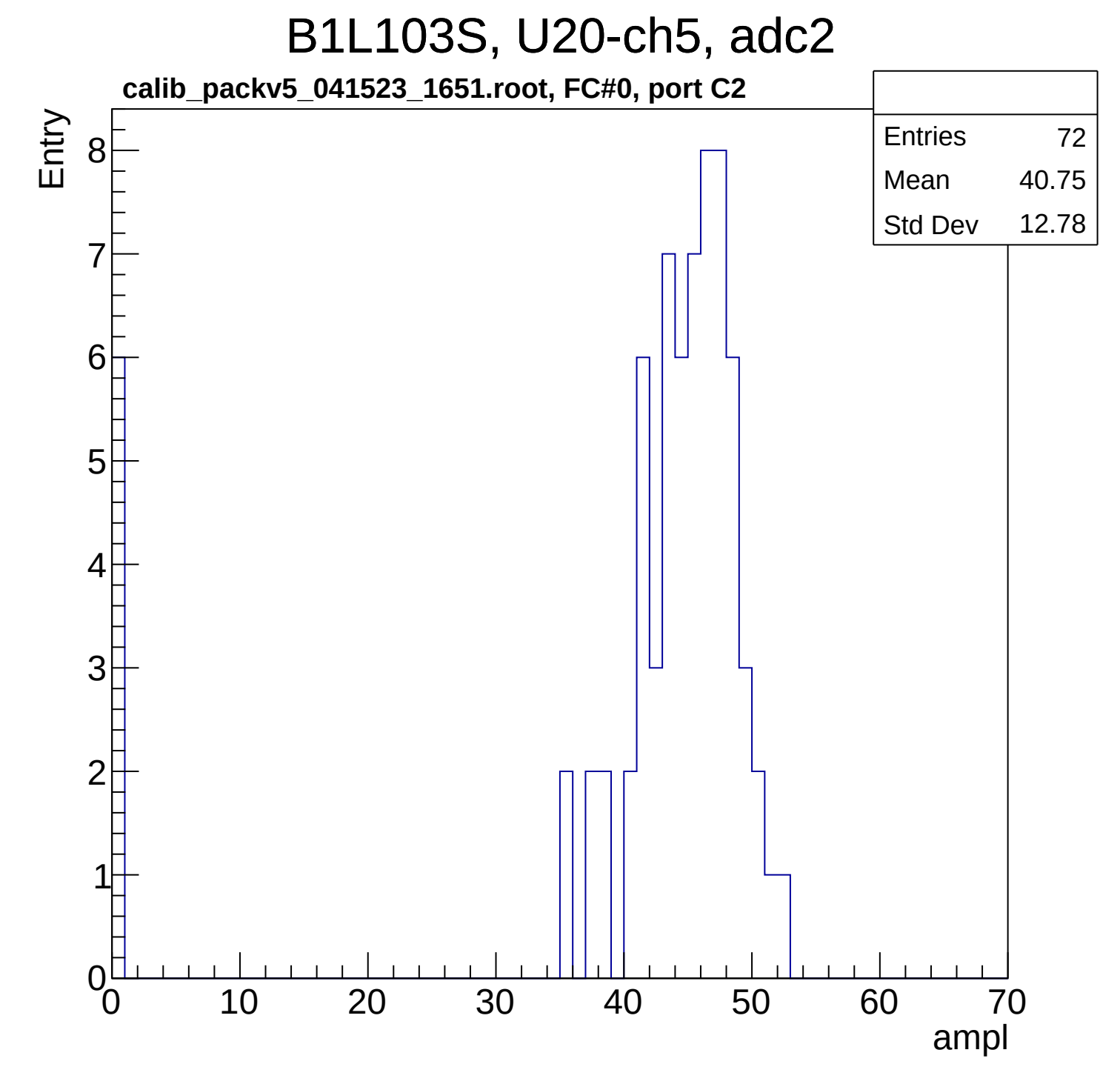

B1L103S, U20-ch5, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 27.56
Std Dev 8.405
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U20-ch5, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 37.38
Std Dev 5.373
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U20-ch5, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 40.75
Std Dev 12.78
Entry
ampl
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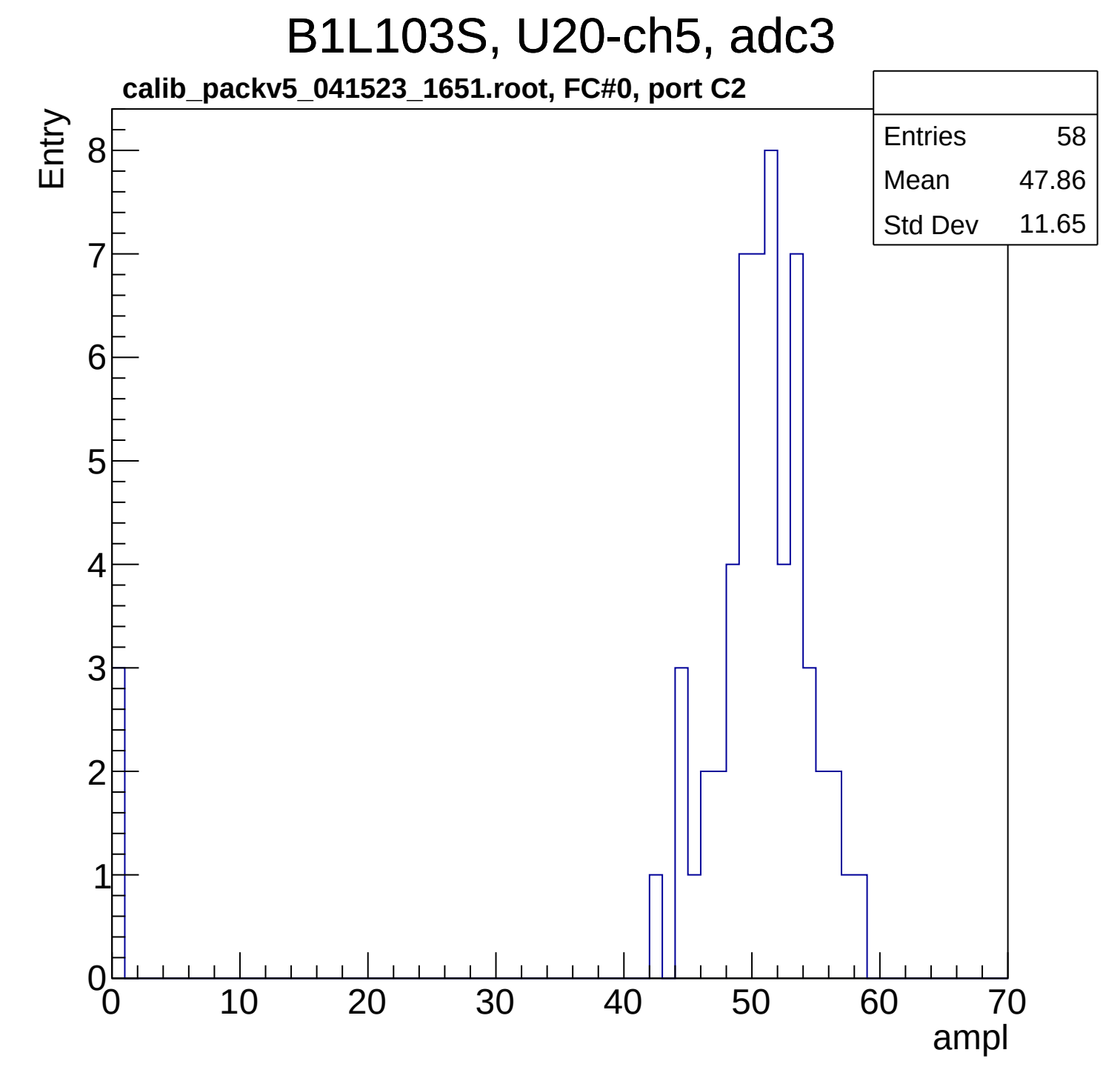
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch5, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 47.86
Std Dev 11.65
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
50
60
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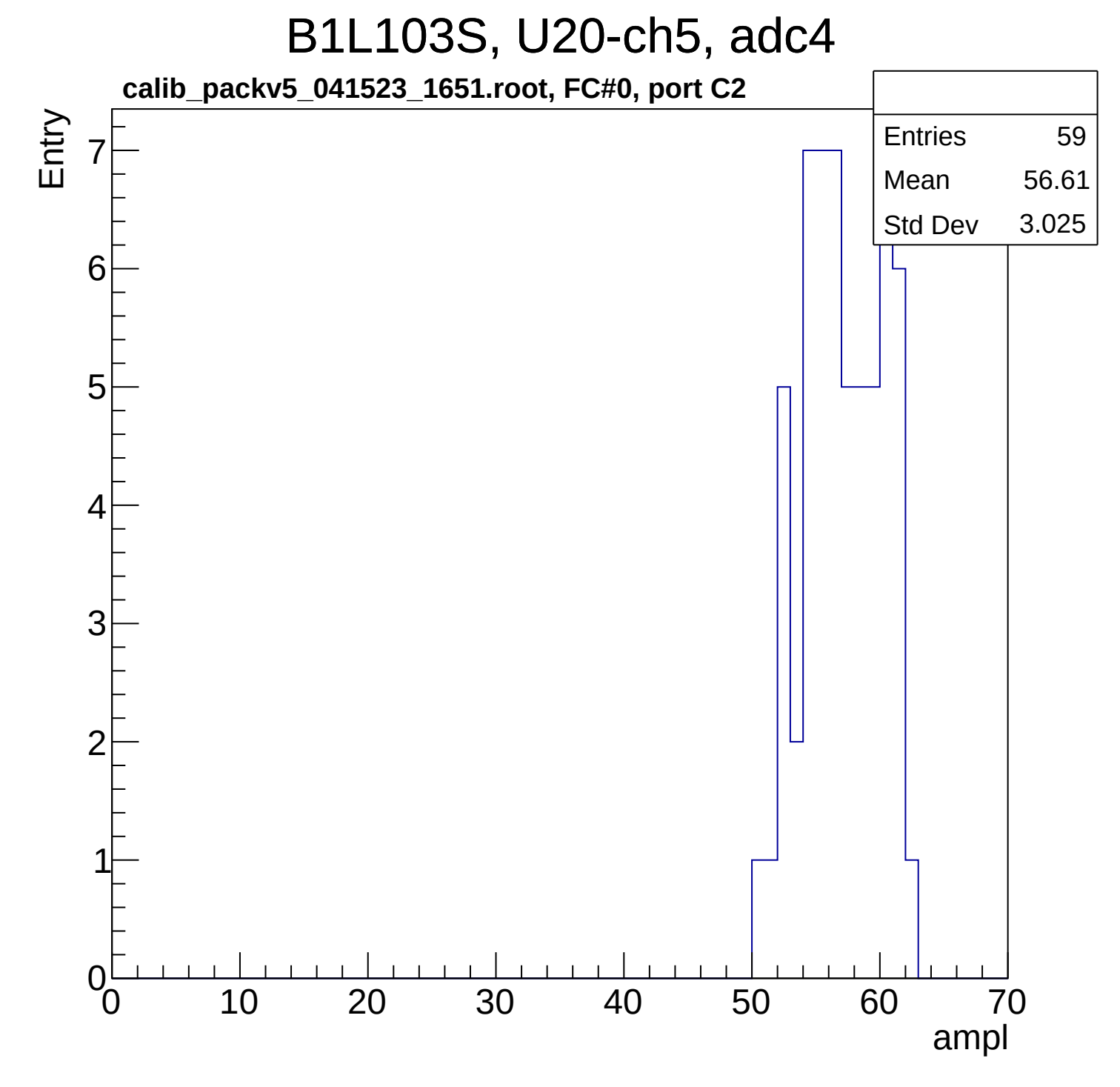
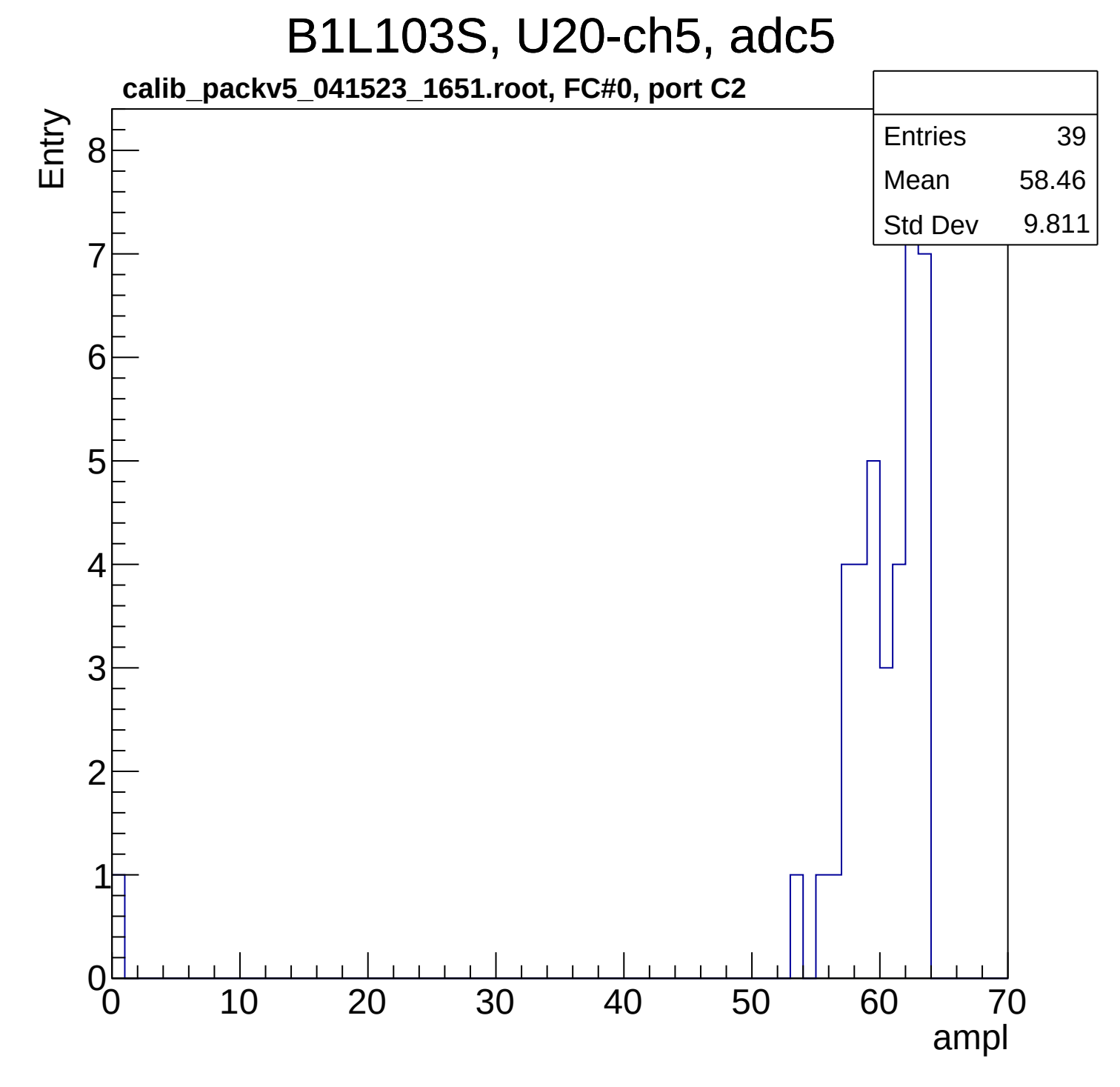

B1L103S, U20-ch5, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 56.61
Std Dev 3.025
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U20-ch5, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 58.46
Std Dev 9.811
Entry
ampl
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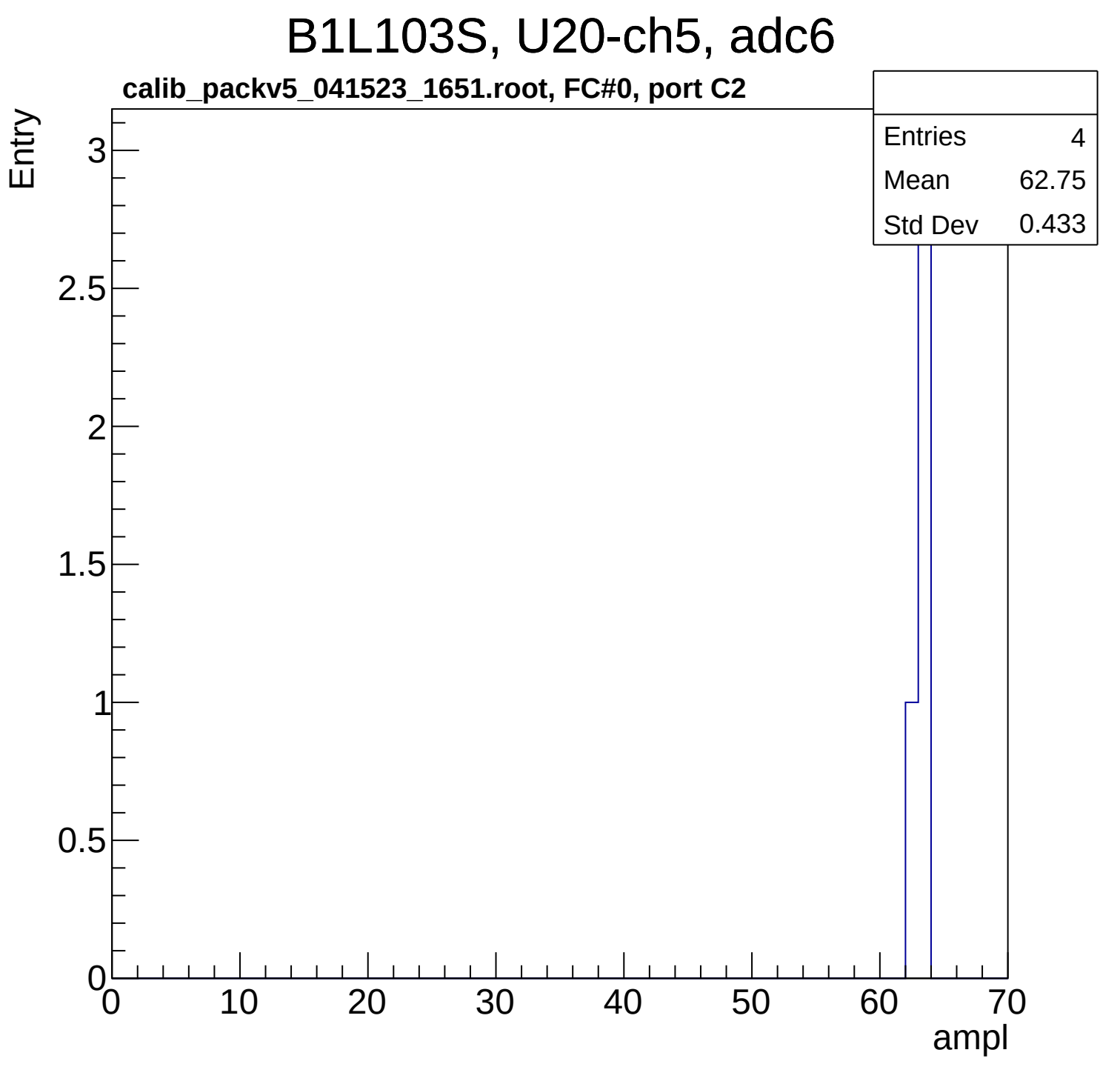
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch5, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 62.75
Std Dev 0.433
Entry
ampl
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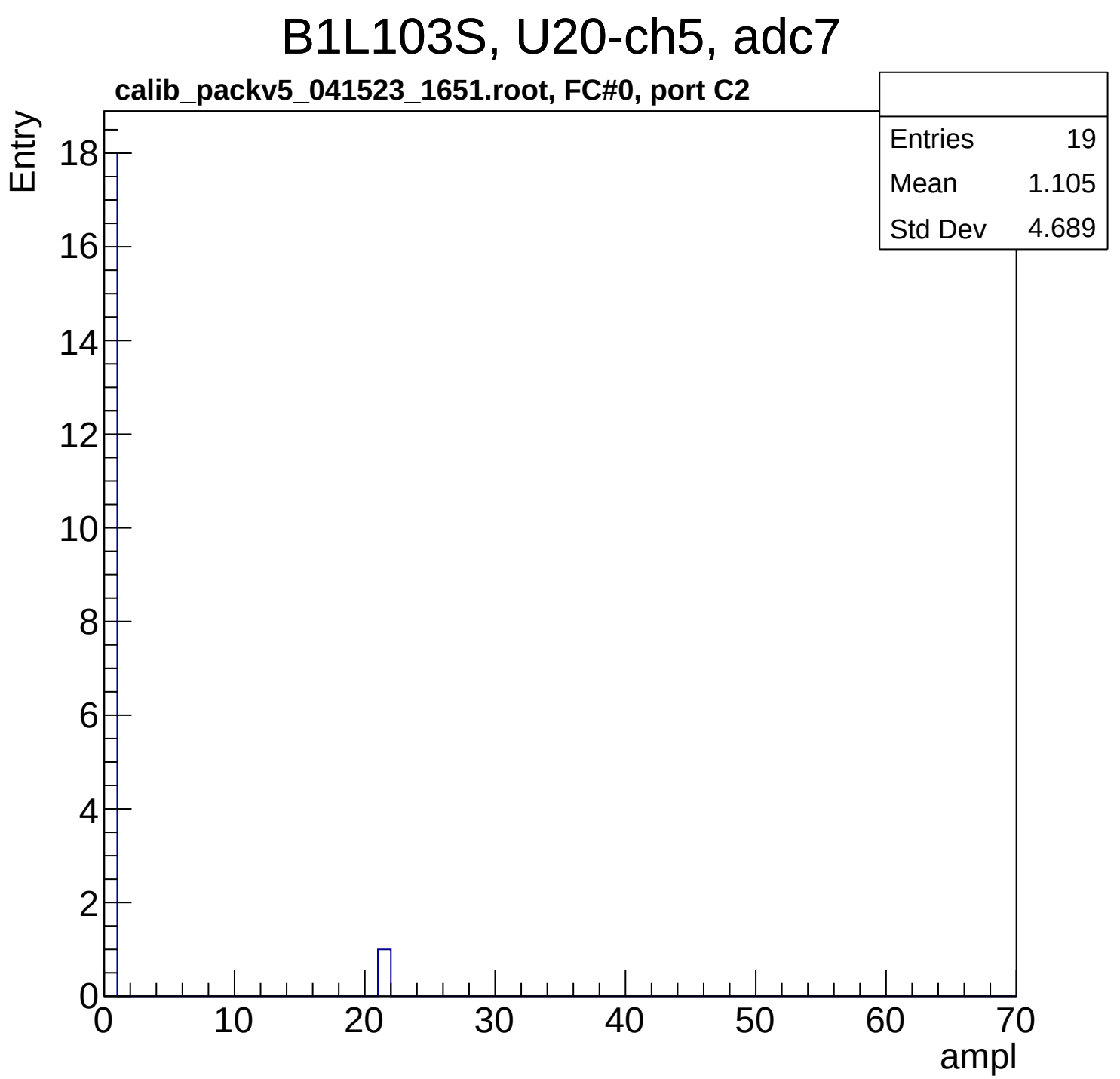
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U20-ch5, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.105
Std Dev 4.689
Entry
0
2
4
6
8
10
12
14
16
18
0
10
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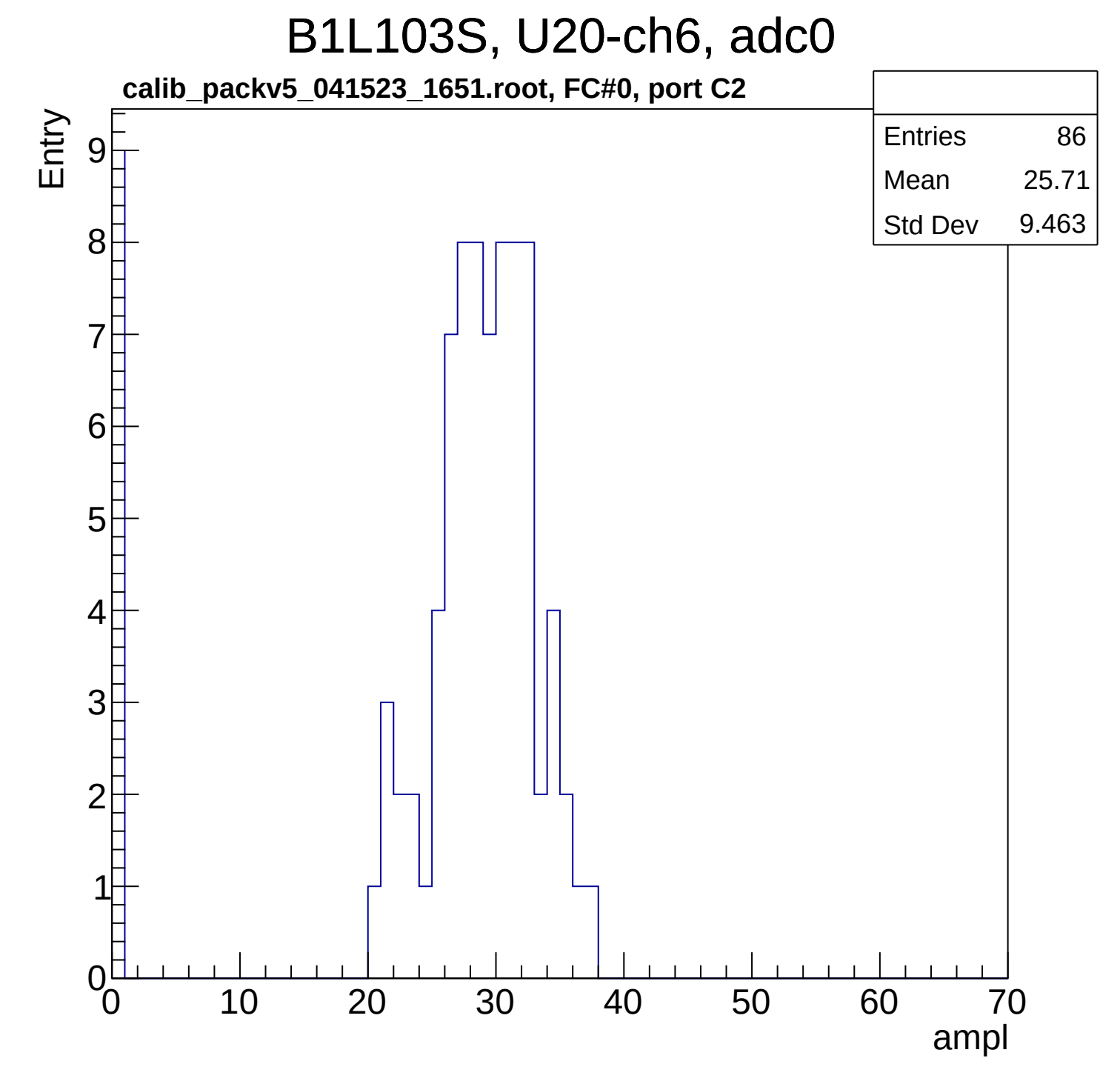
30
40
50
60
70
ampl


B1L103S, U20-ch6, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 25.71
Std Dev 9.463
Entry
ampl
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3
4
5
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7
8
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0
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60
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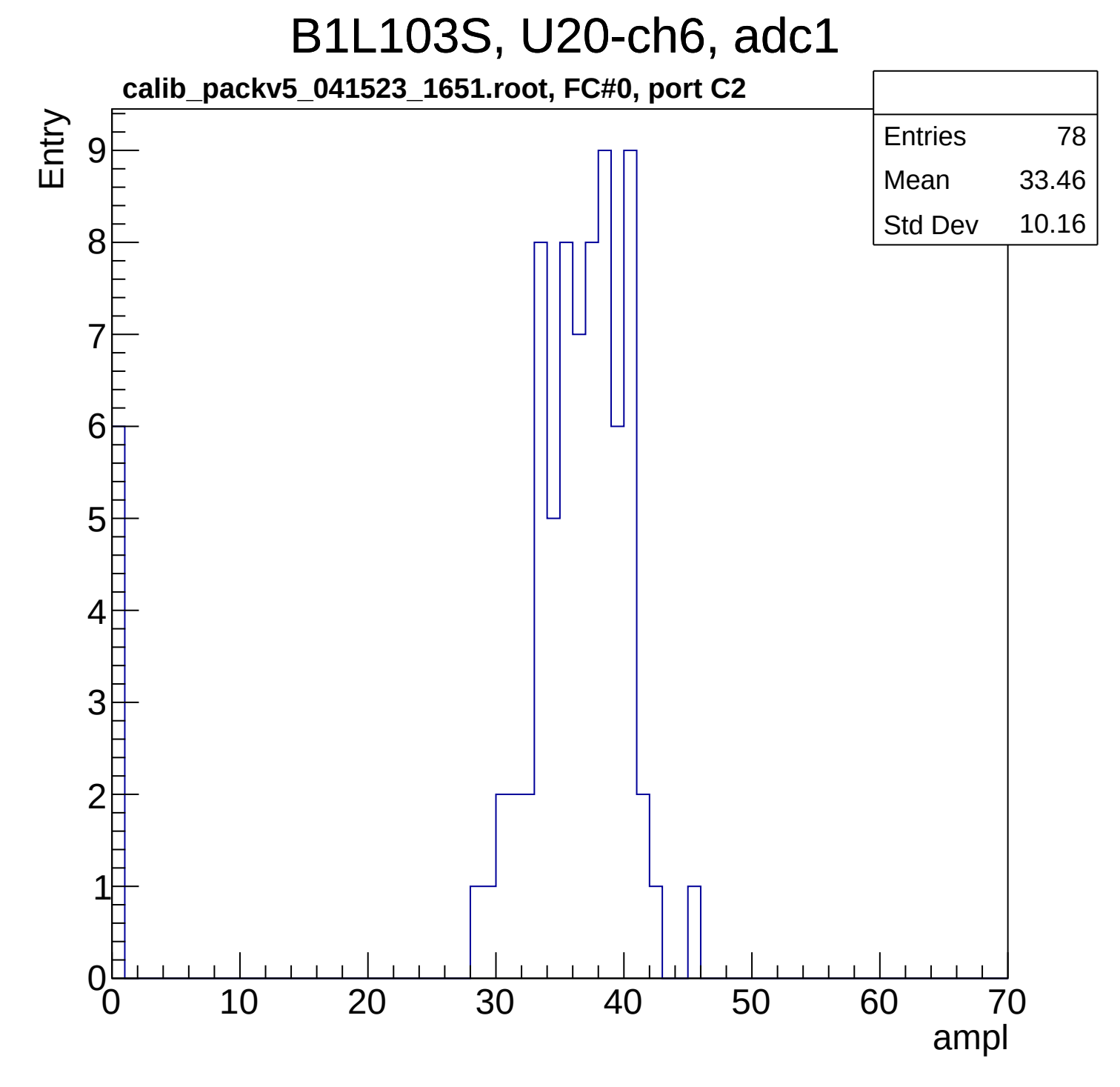
B1L103S, U20-ch6, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 33.46
Std Dev 10.16
Entry
ampl
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3
4
5
6
7
8
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0
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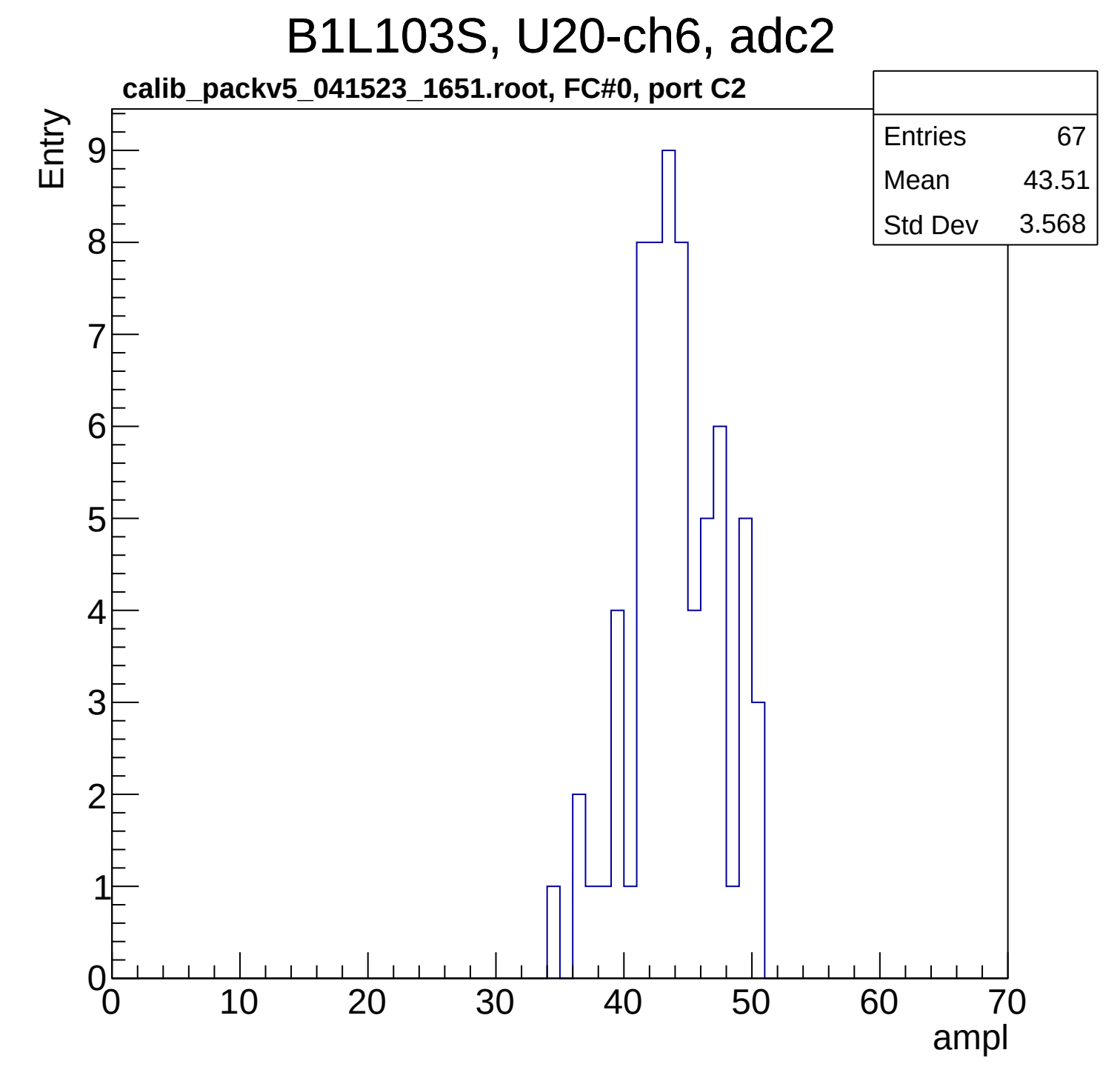
40
50
60
70


B1L103S, U20-ch6, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 43.51
Std Dev 3.568
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
30
40
50
60
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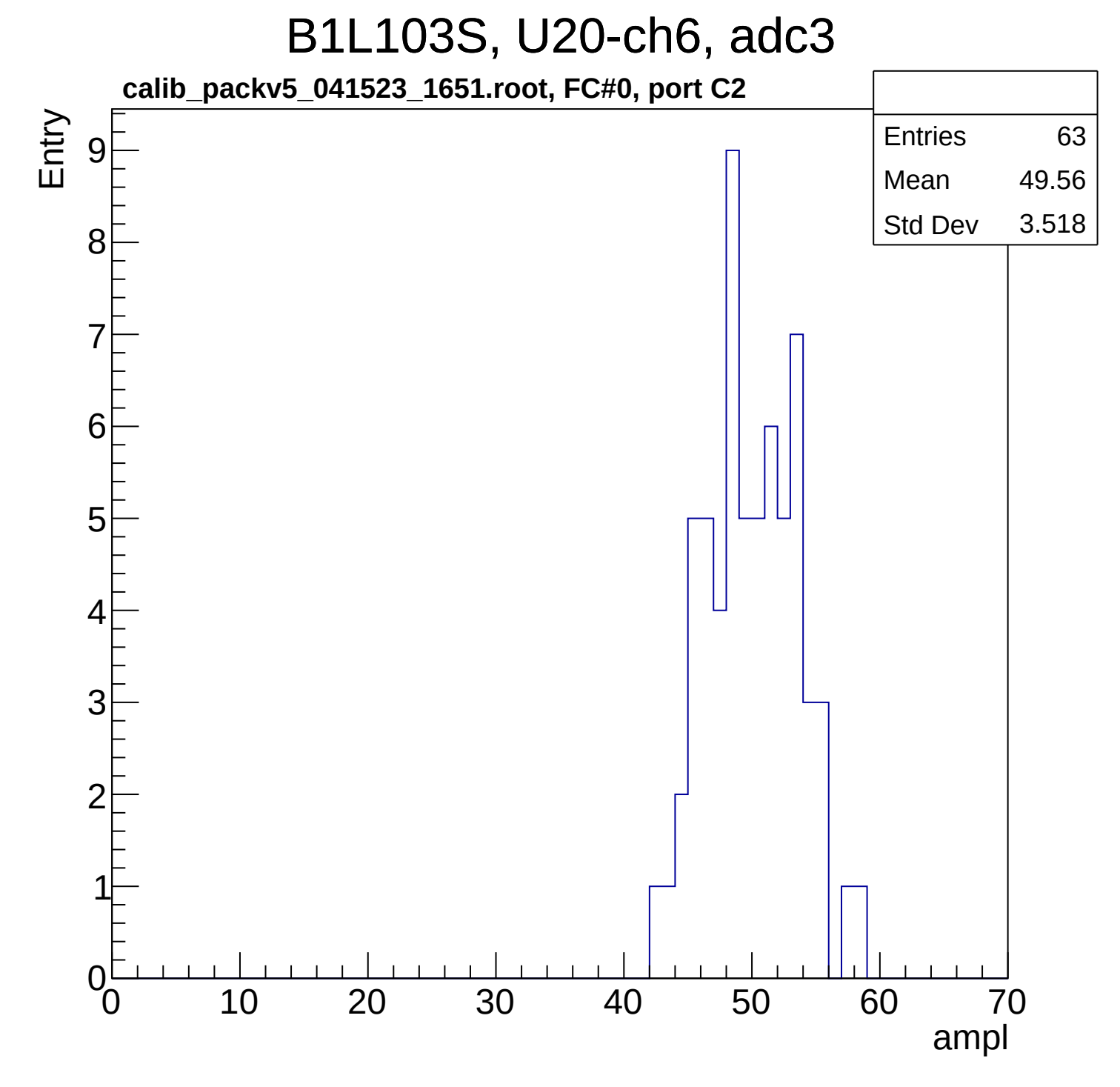
B1L103S, U20-ch6, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 49.56
Std Dev 3.518
Entry
ampl
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3
4
5
6
7
8
9
0
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20
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40
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60
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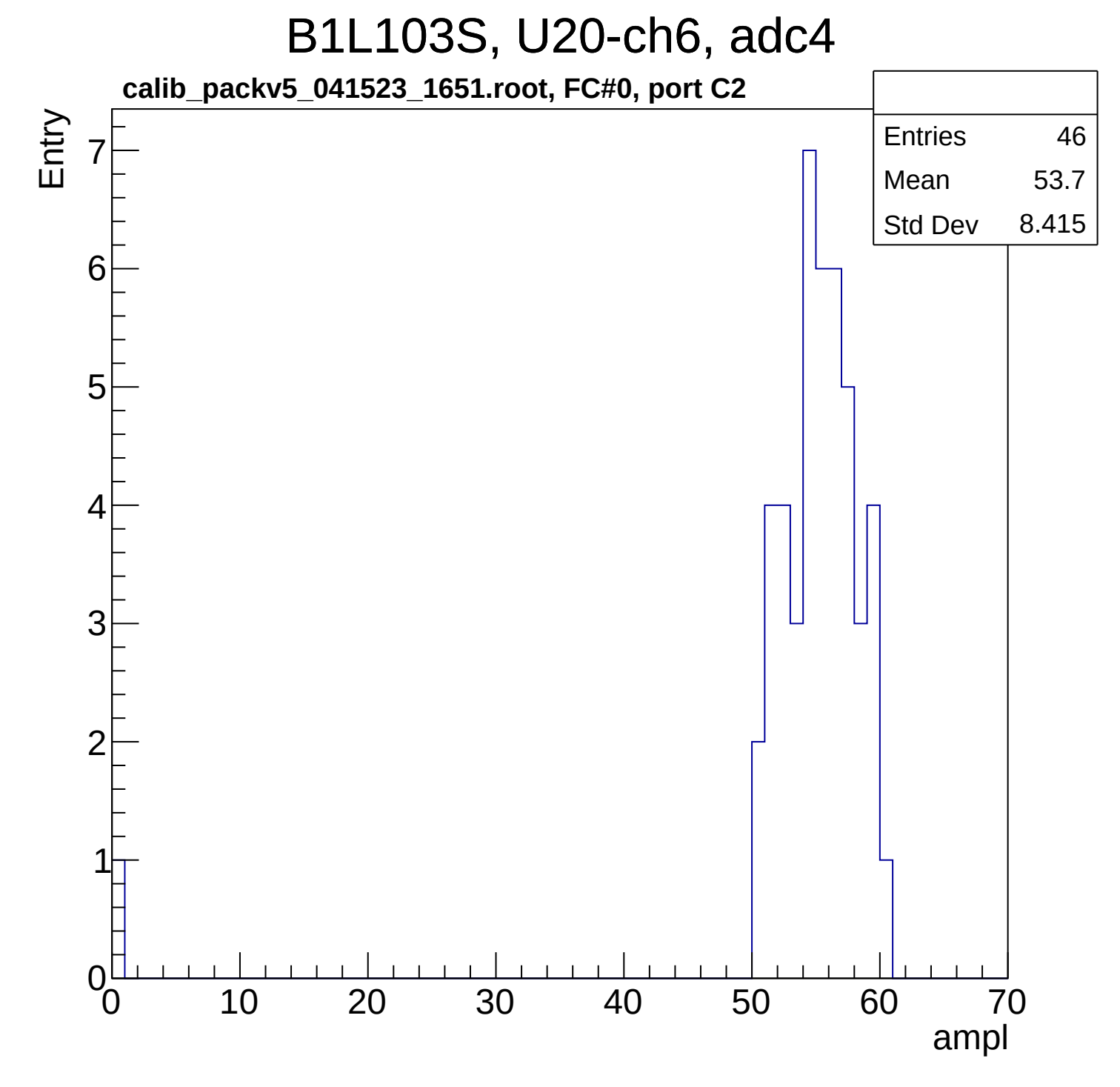
B1L103S, U20-ch6, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 53.7
Std Dev 8.415
Entry
ampl
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3
4
5
6
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0
10
20
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40
50
60
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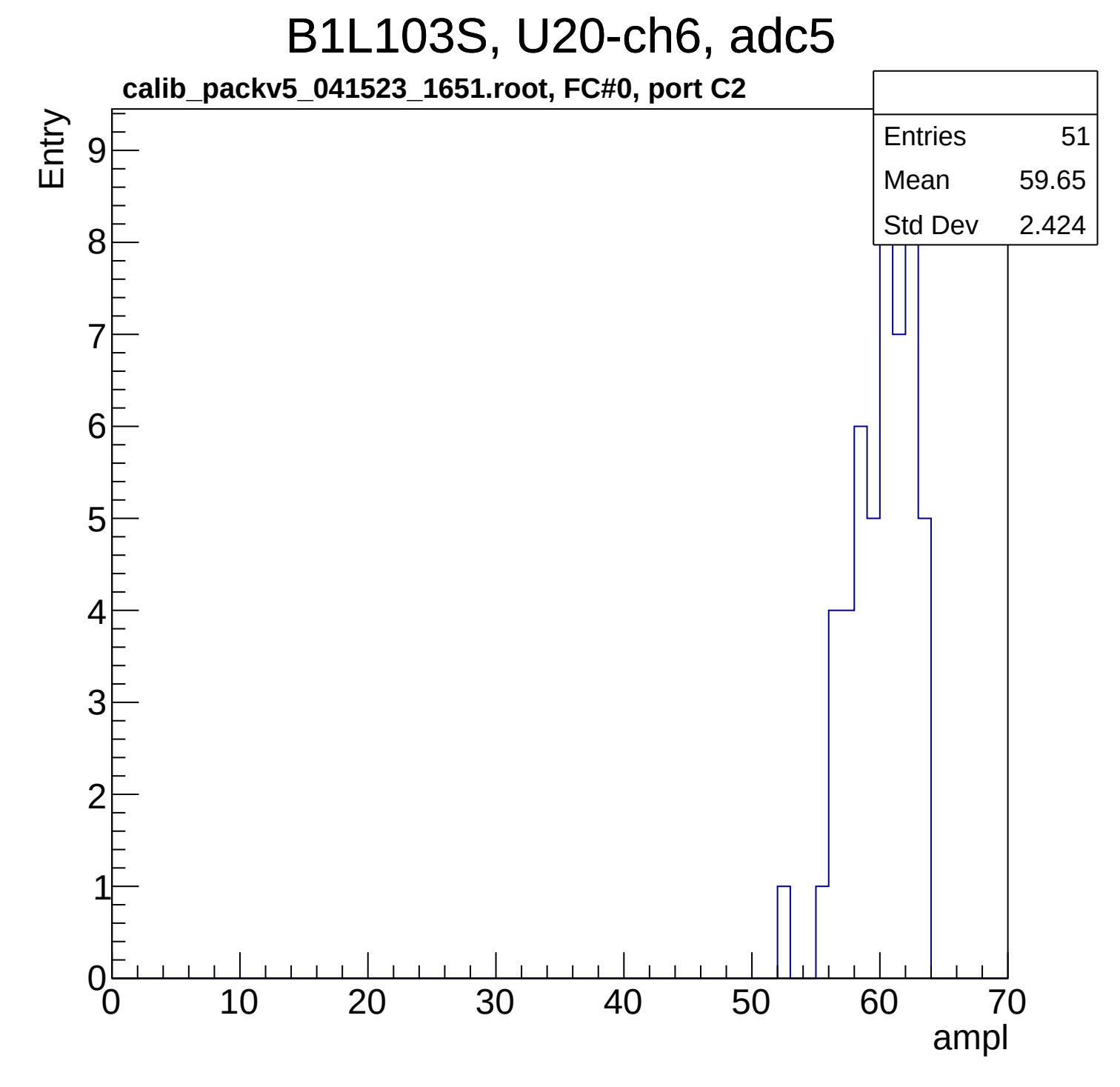
B1L103S, U20-ch6, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 59.65
Std Dev 2.424
Entry
ampl
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3
4
5
6
7
8
9
0
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20
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40
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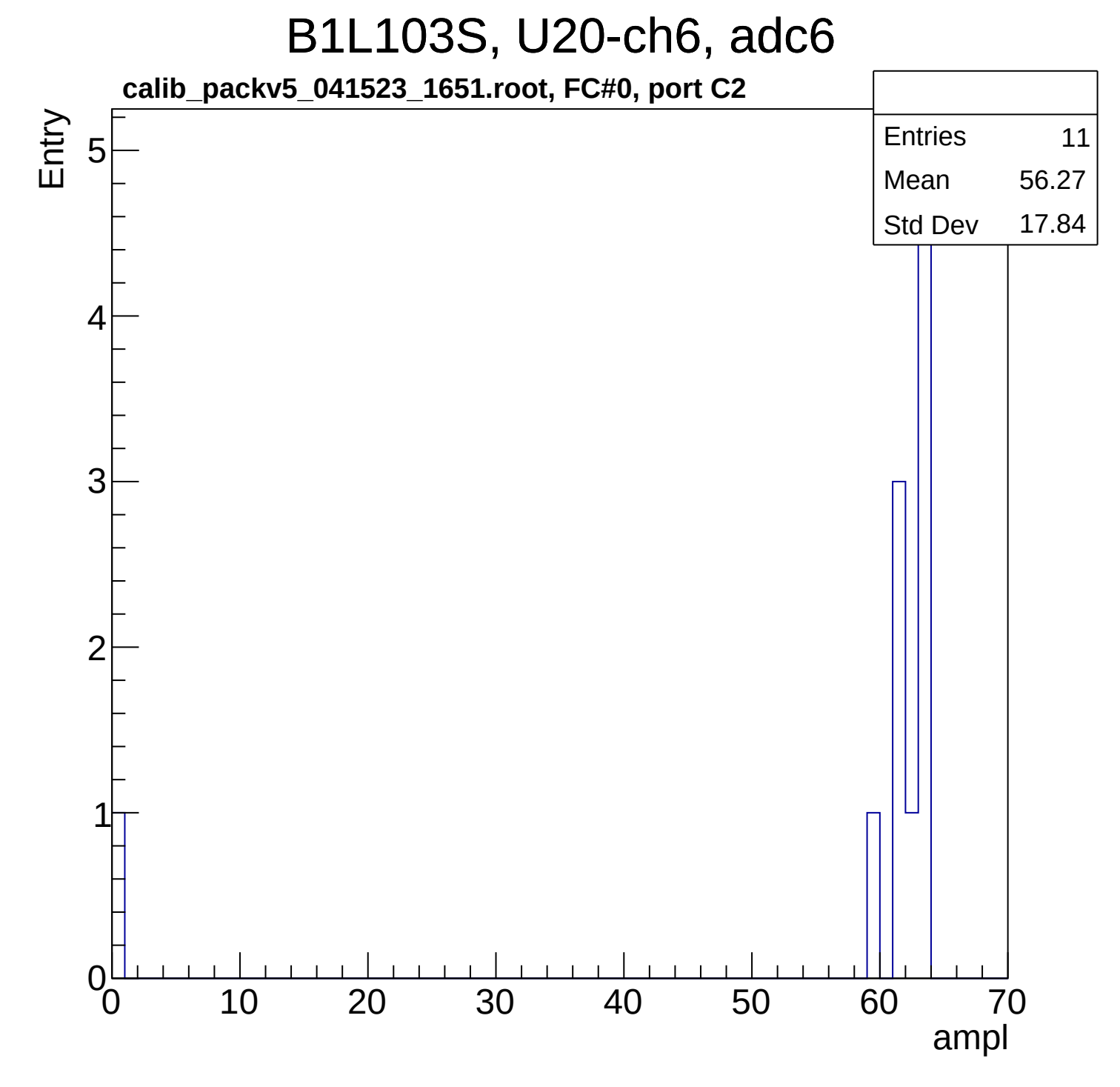
60
70


B1L103S, U20-ch6, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 56.27
Std Dev 17.84
Entry
ampl
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1
2
3
4
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0
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20
30
40
50
60
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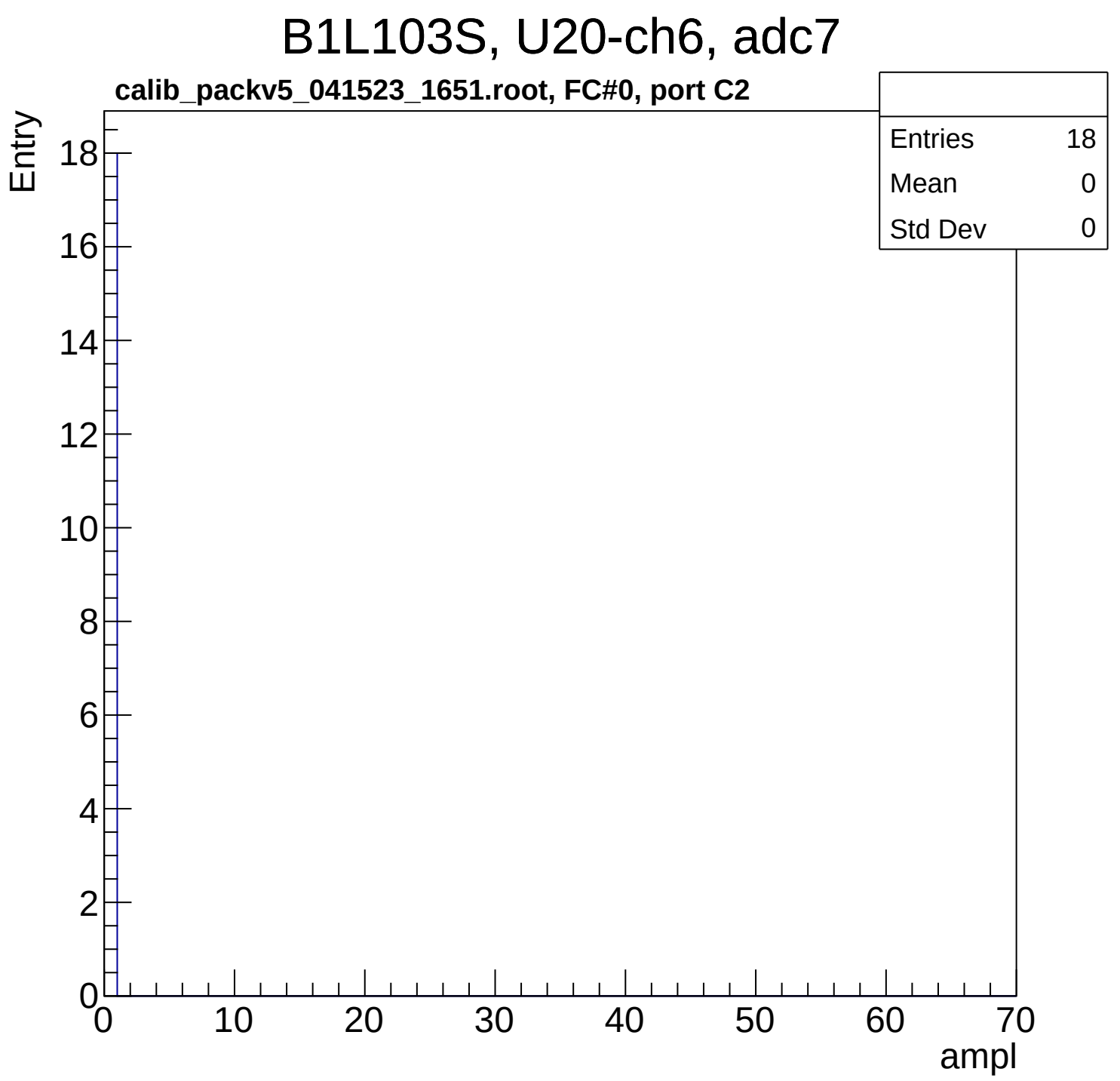
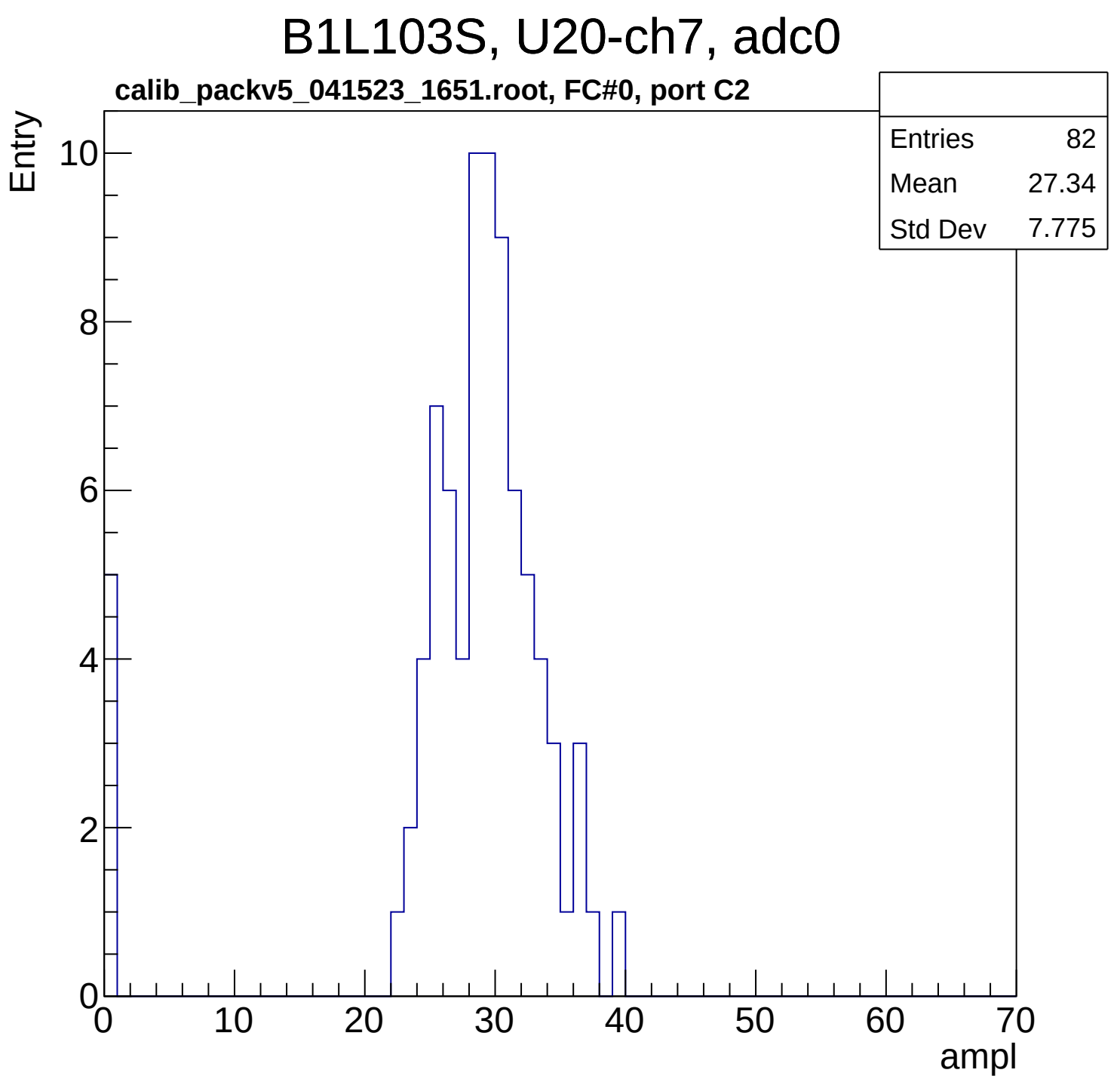

B1L103S, U20-ch6, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch7, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 27.34
Std Dev 7.775
Entry
ampl
0
2
4
6
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0
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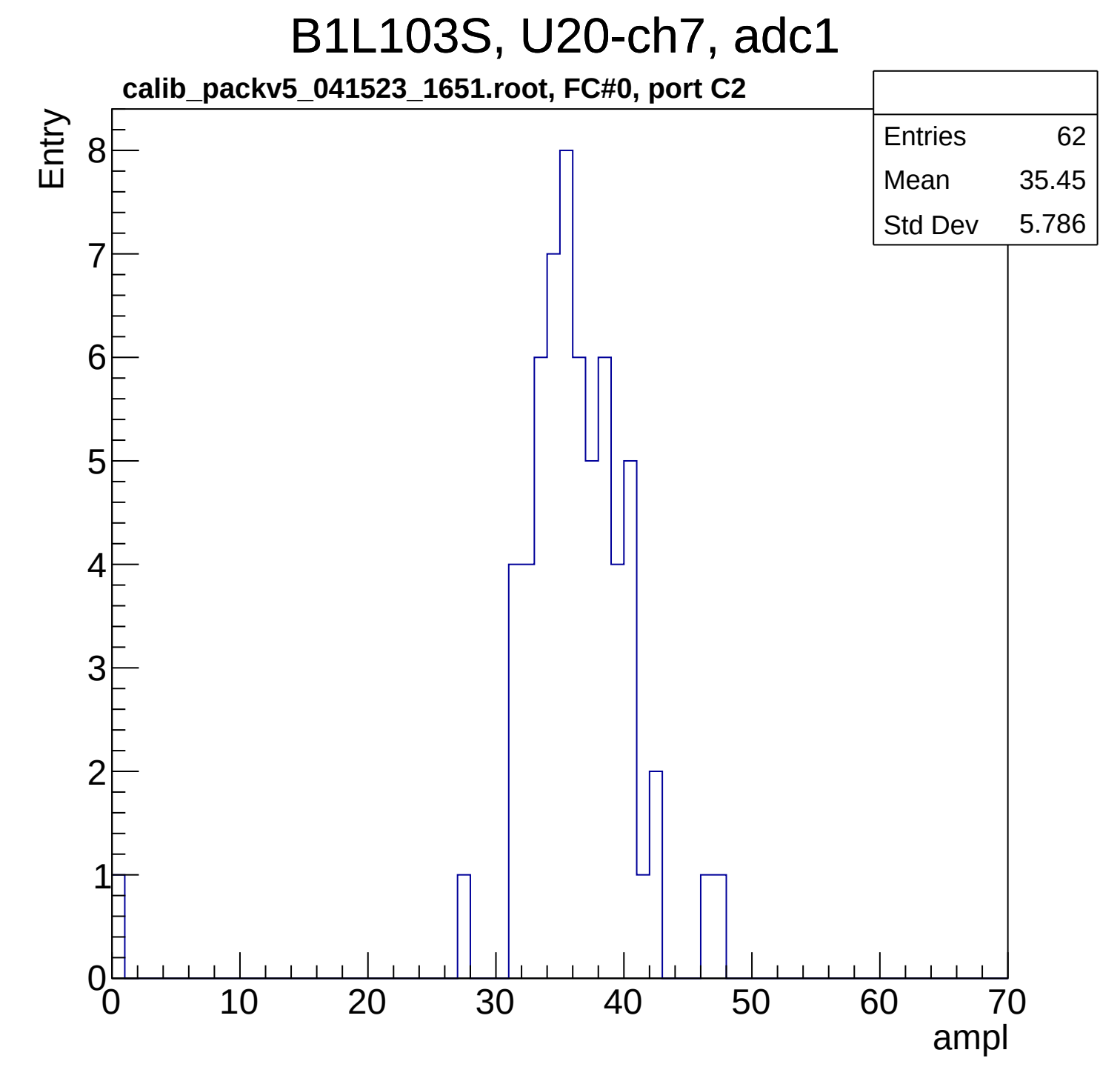
20
30
40
50
60
70


B1L103S, U20-ch7, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 35.45
Std Dev 5.786
Entry
ampl
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2
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5
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7
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0
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20
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40
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60
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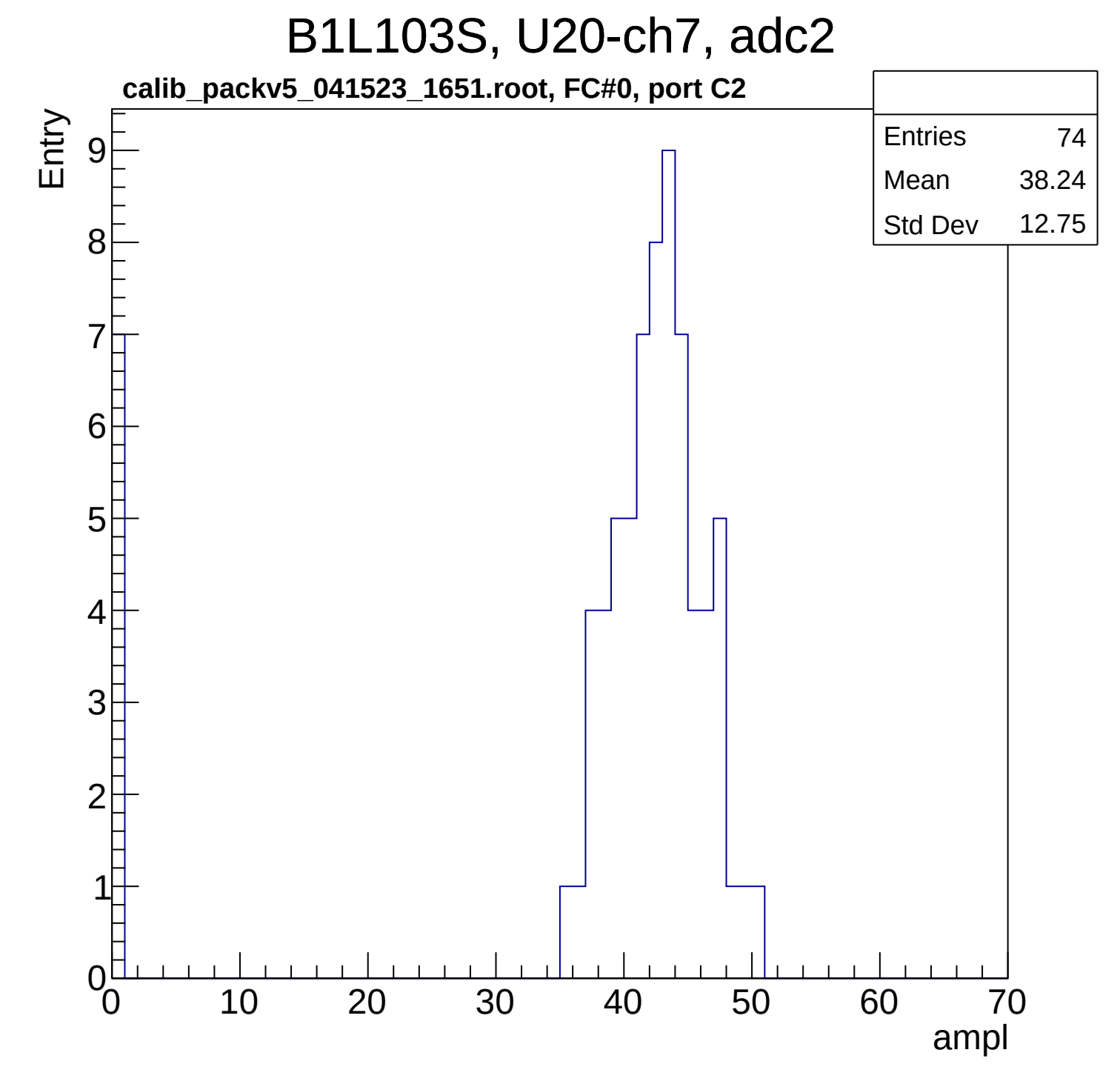
B1L103S, U20-ch7, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 38.24
Std Dev 12.75
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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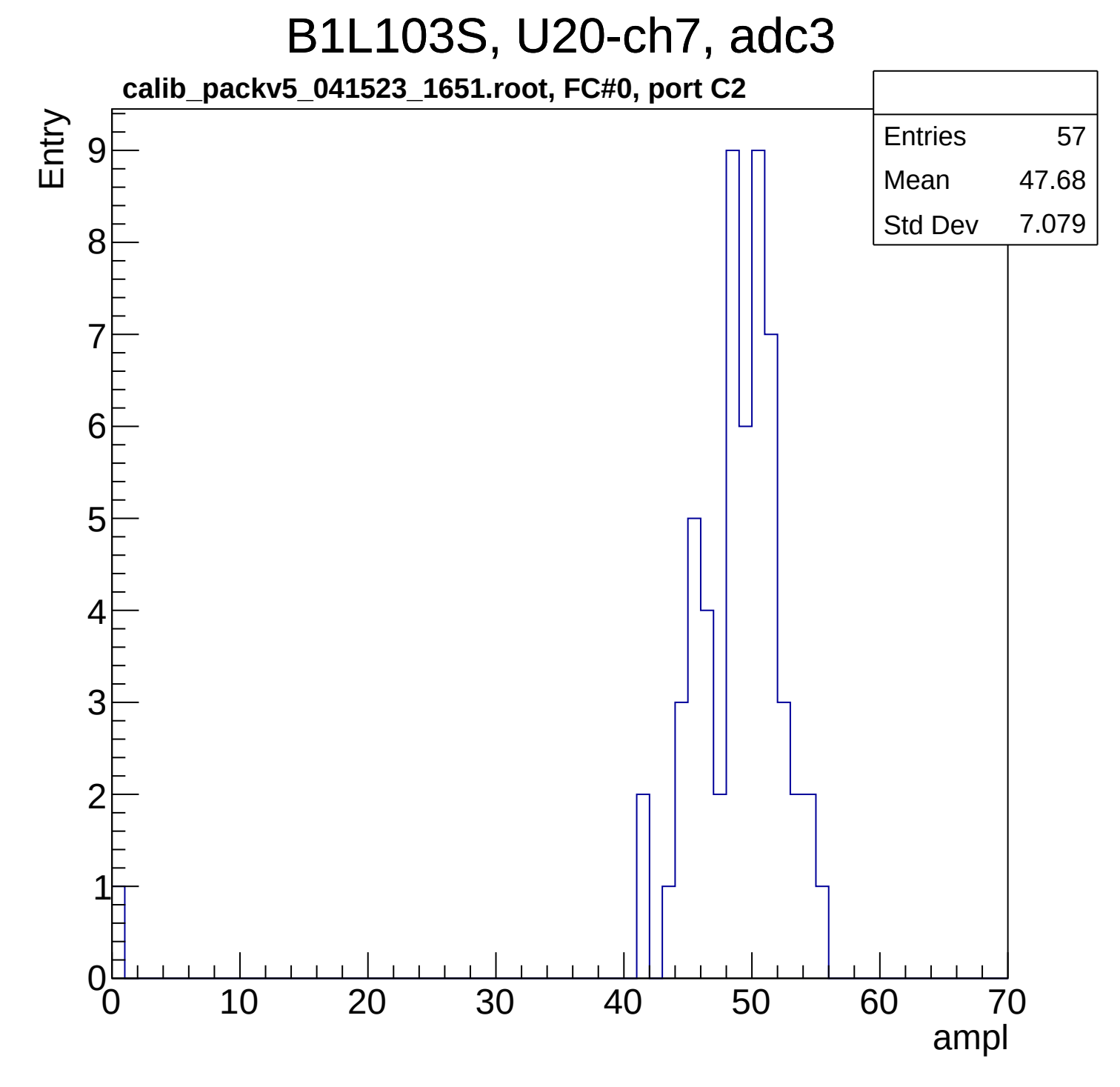
60
70


B1L103S, U20-ch7, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 47.68
Std Dev 7.079
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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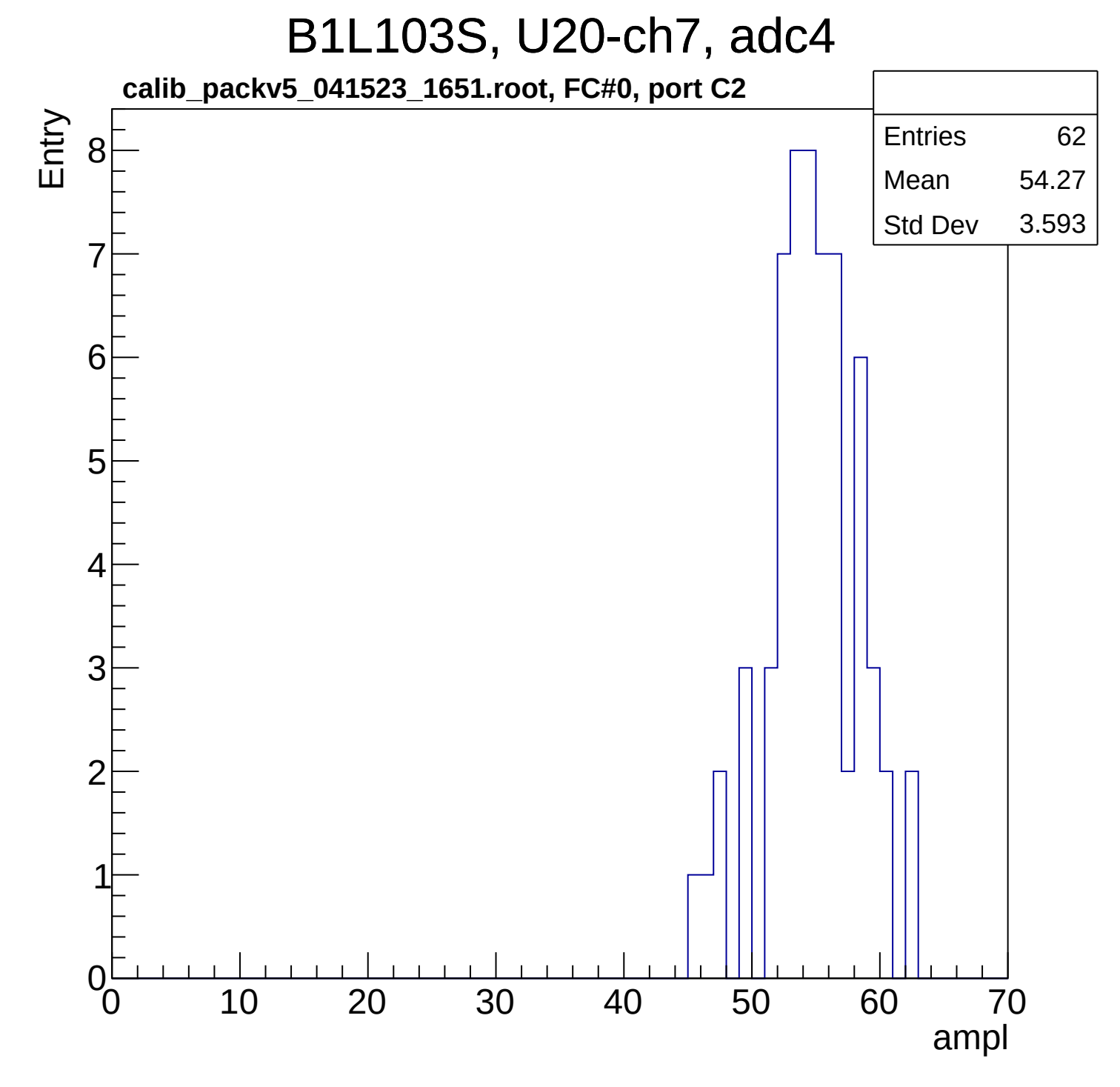
40
50
60
70


B1L103S, U20-ch7, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 54.27
Std Dev 3.593
Entry
ampl
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1
2
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4
5
6
7
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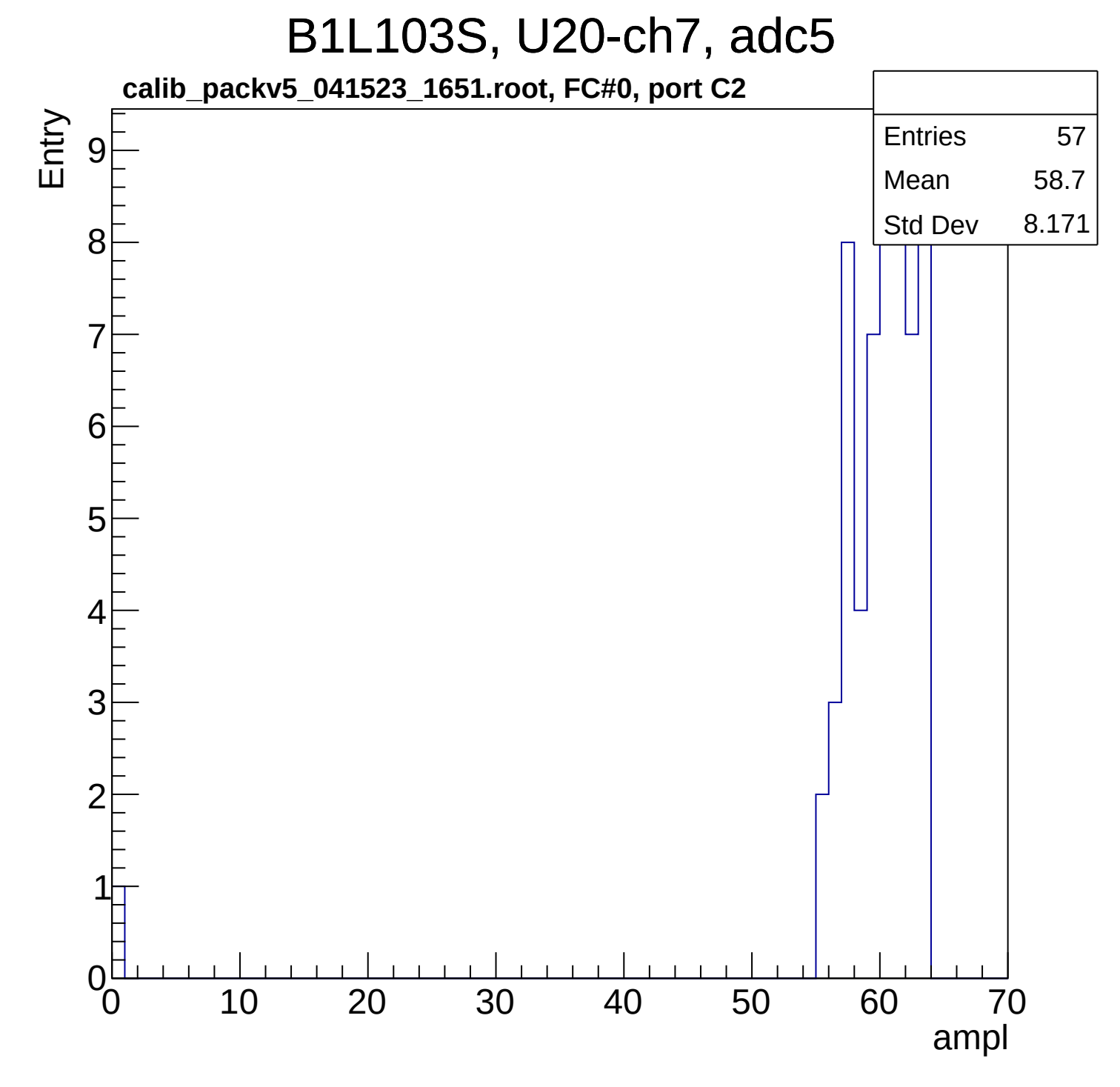
0
10
20
30
40
50
60
70


B1L103S, U20-ch7, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 58.7
Std Dev 8.171
Entry
ampl
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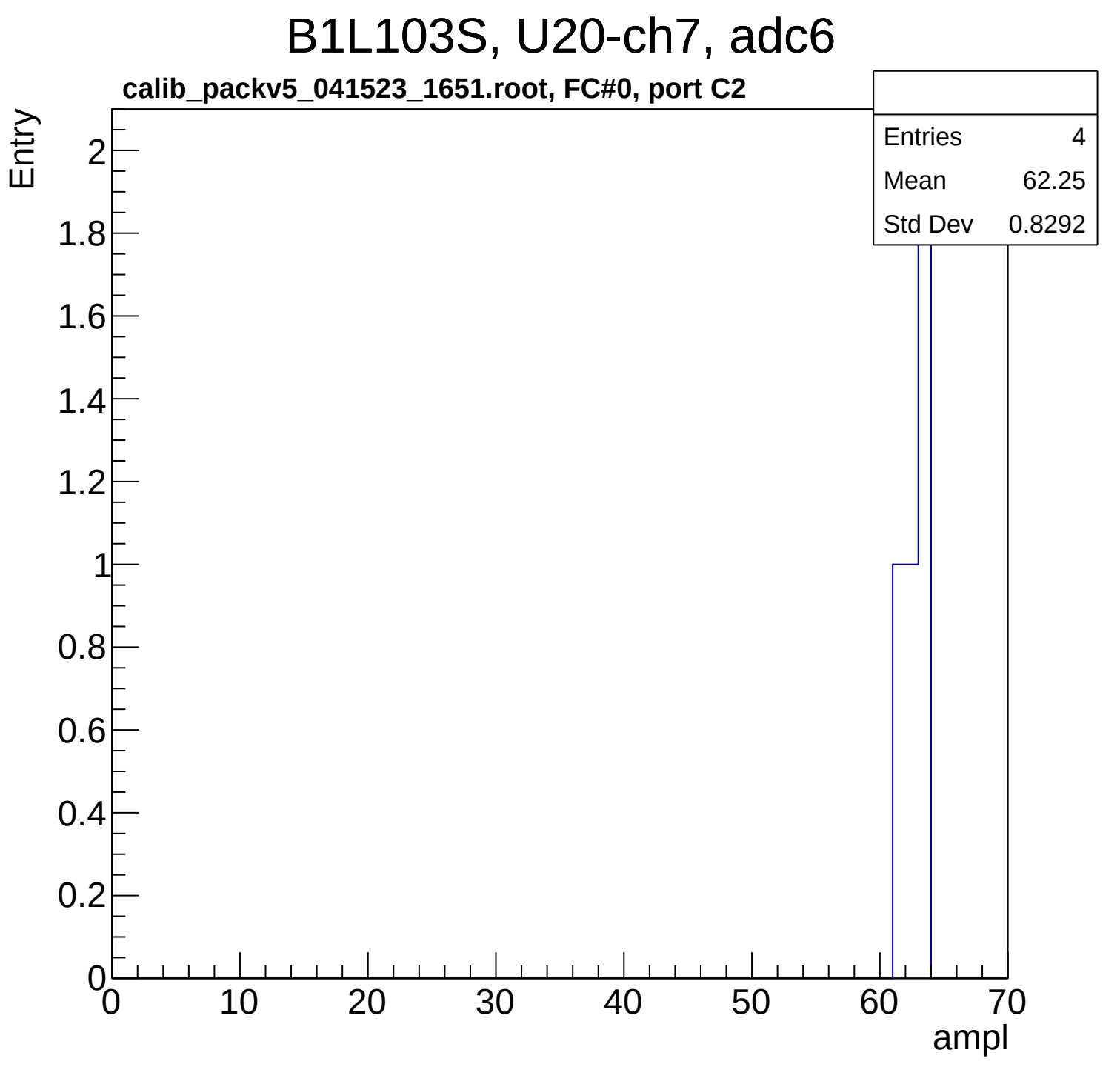
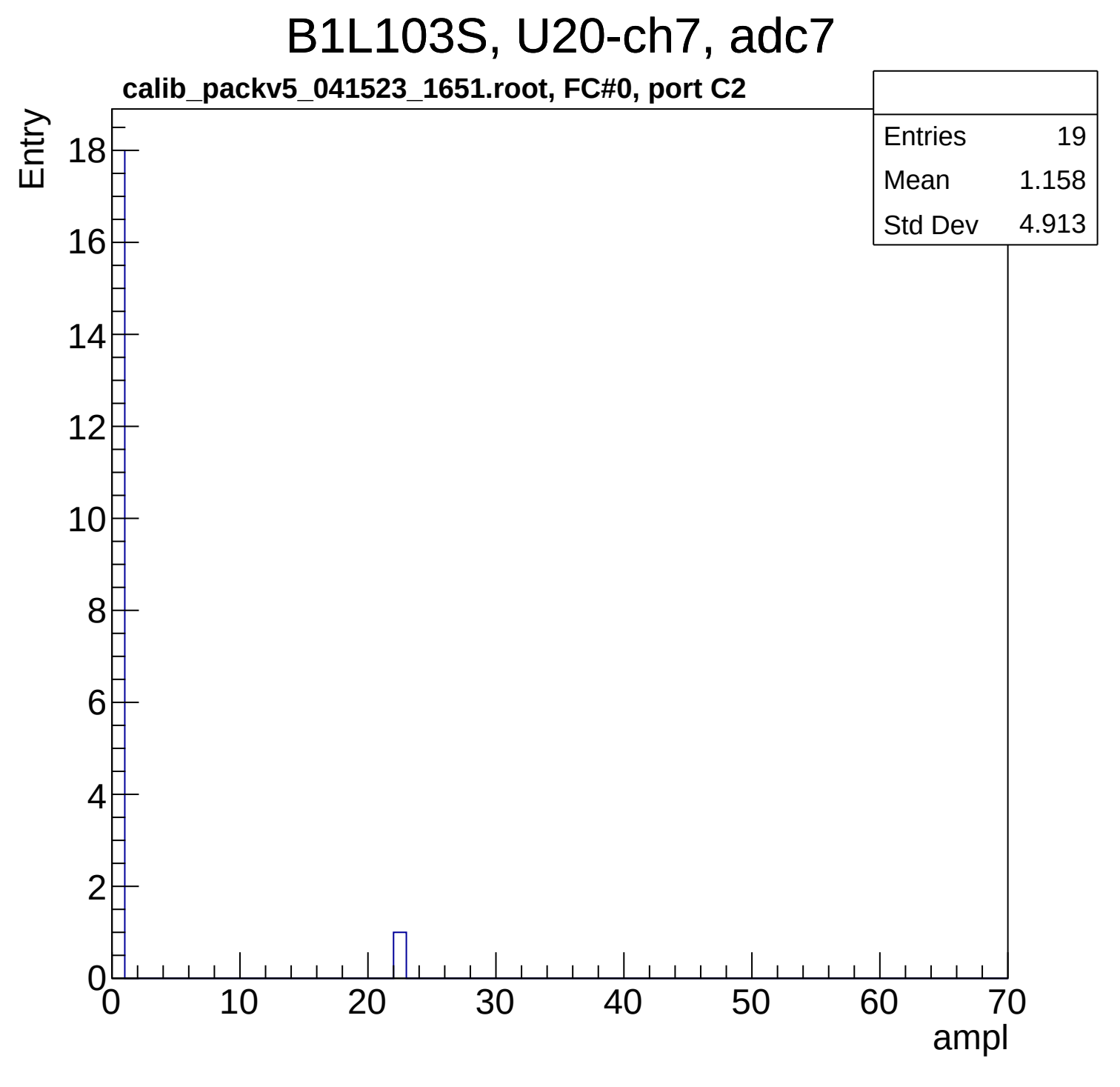
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch7, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 62.25
Std Dev 0.8292
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U20-ch7, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.158
Std Dev 4.913
Entry
ampl
0
2
4
6
8
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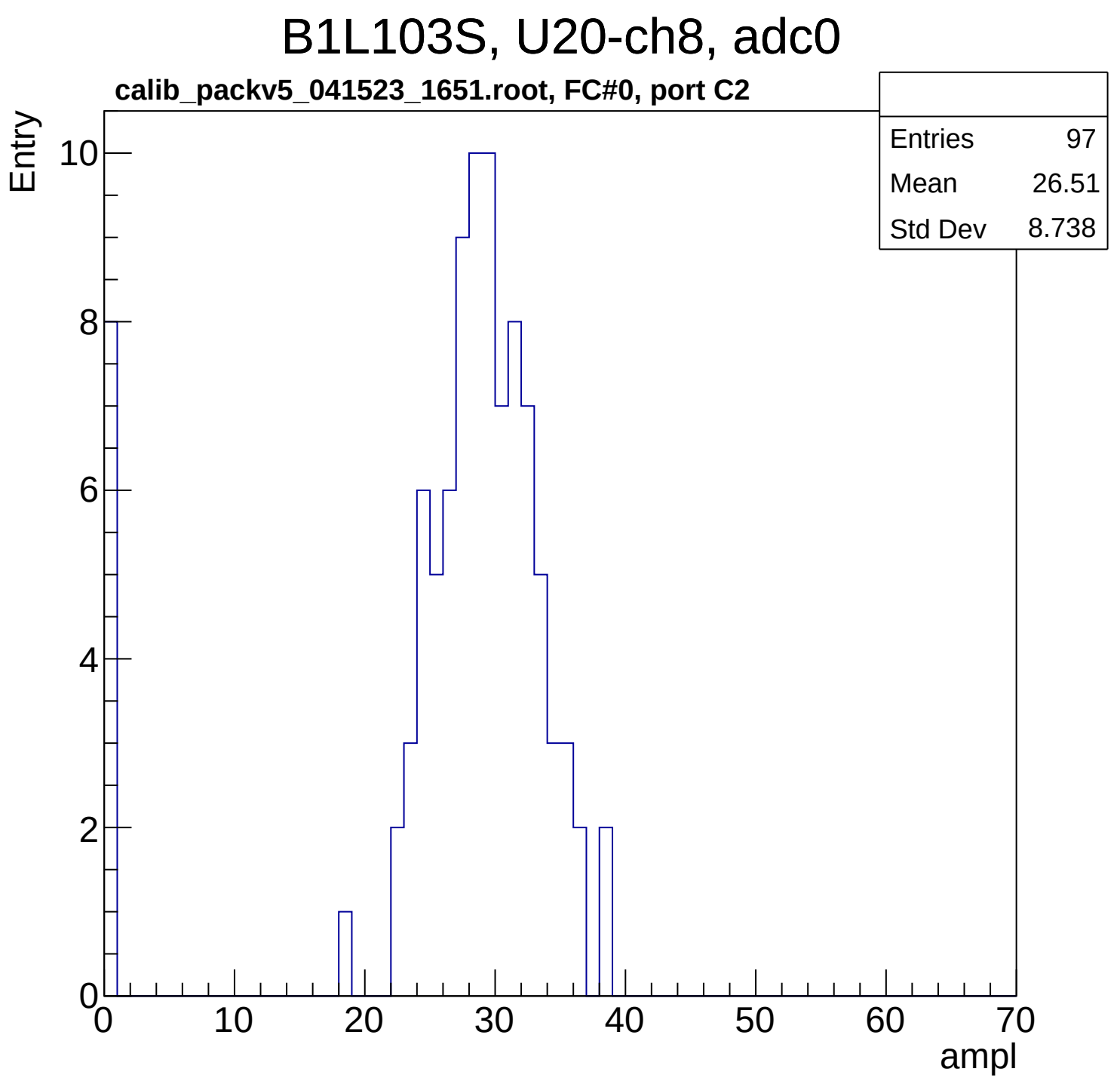
B1L103S, U20-ch8, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 26.51
Std Dev 8.738
Entry
ampl
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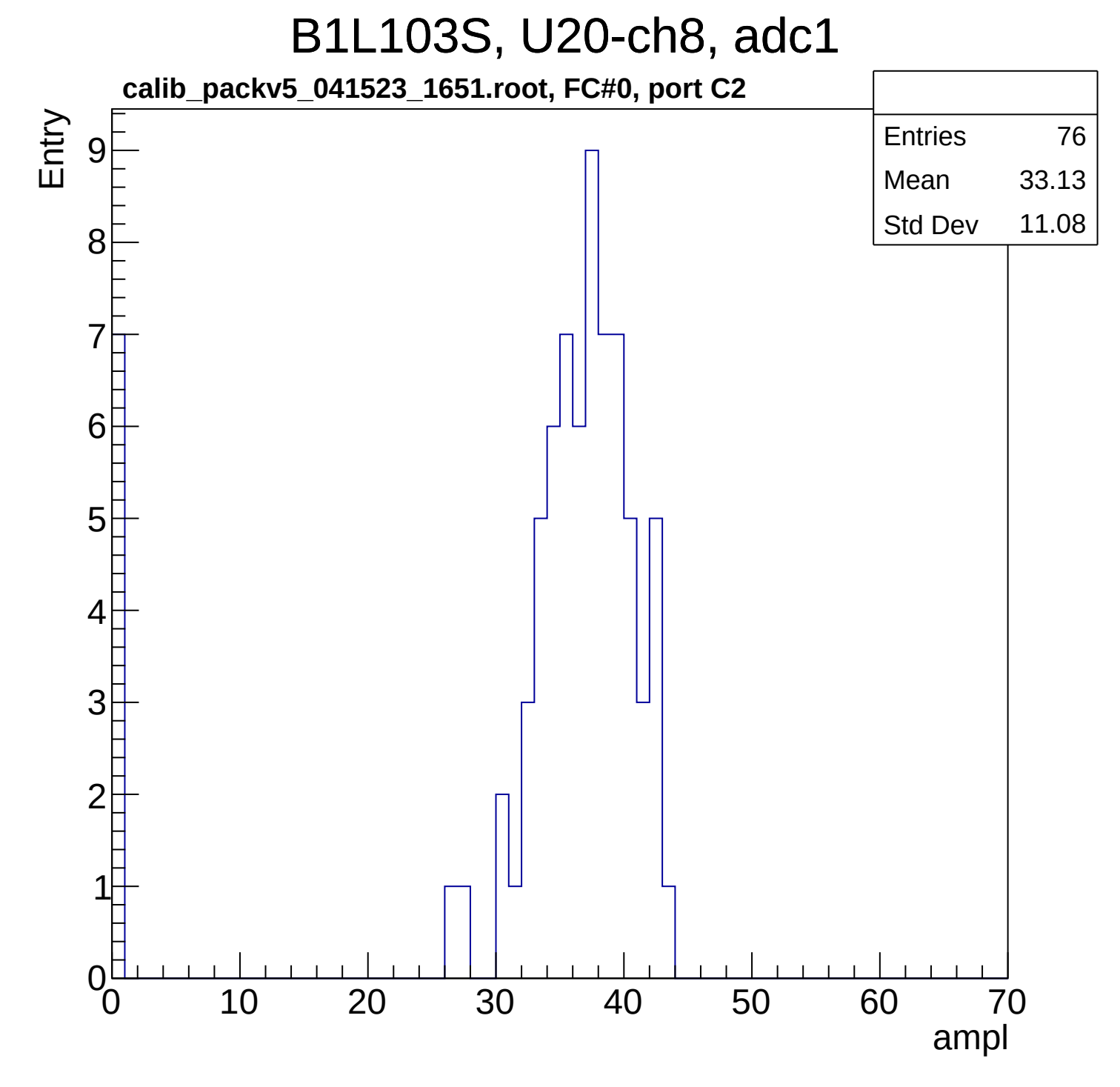
B1L103S, U20-ch8, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 33.13
Std Dev 11.08
Entry
ampl
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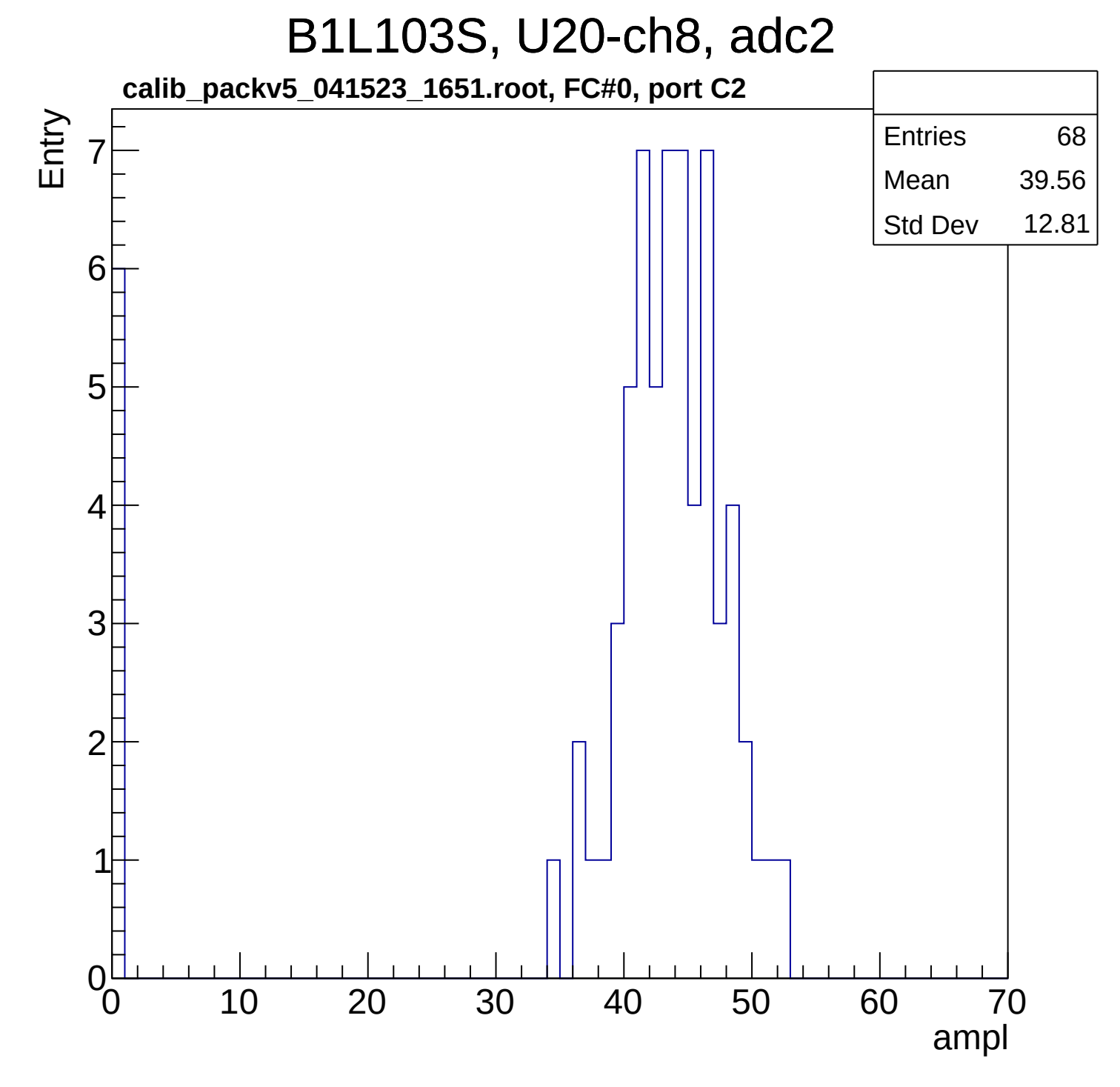
B1L103S, U20-ch8, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 39.56
Std Dev 12.81
Entry
ampl
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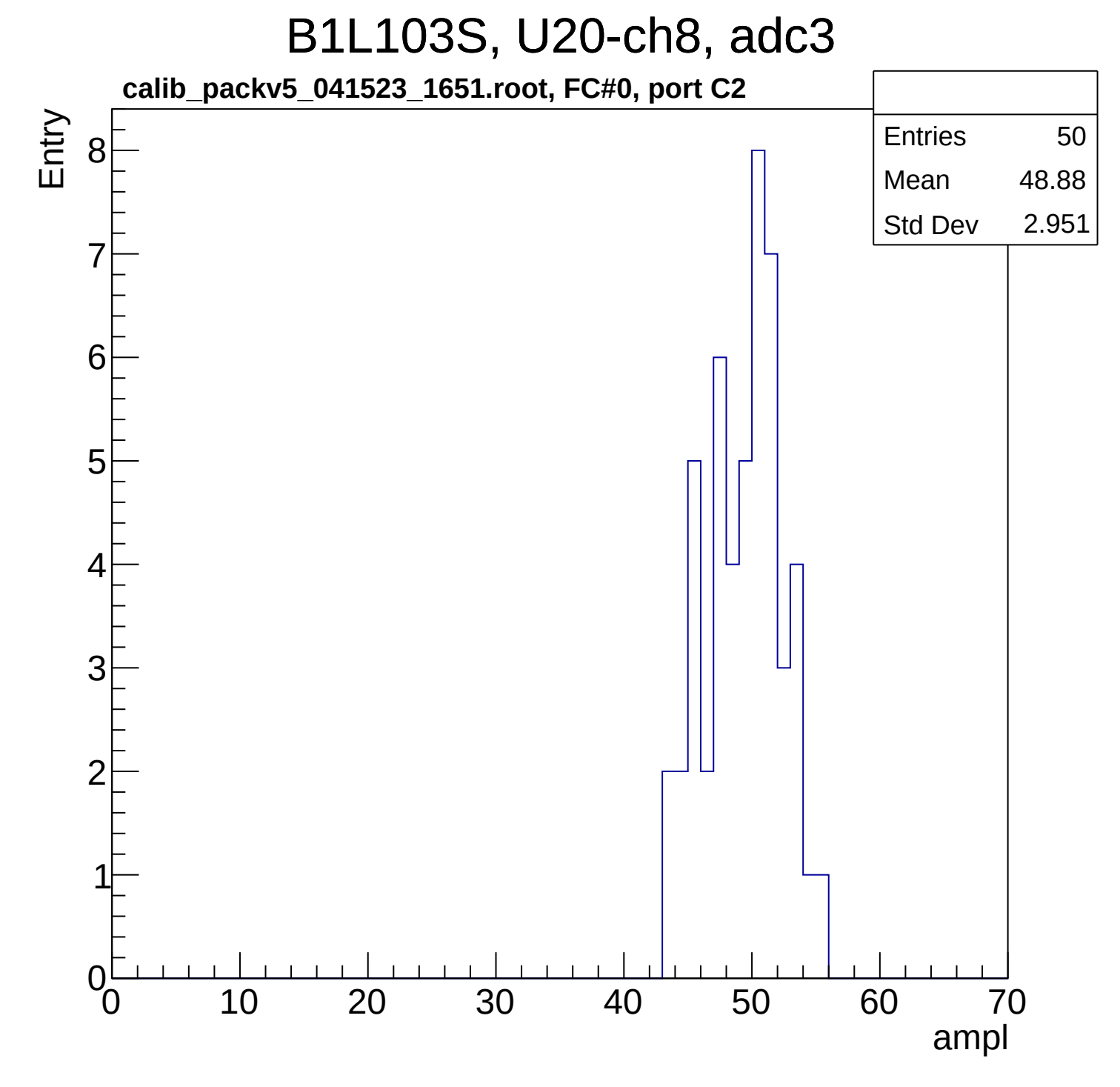
B1L103S, U20-ch8, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 48.88
Std Dev 2.951
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ampl
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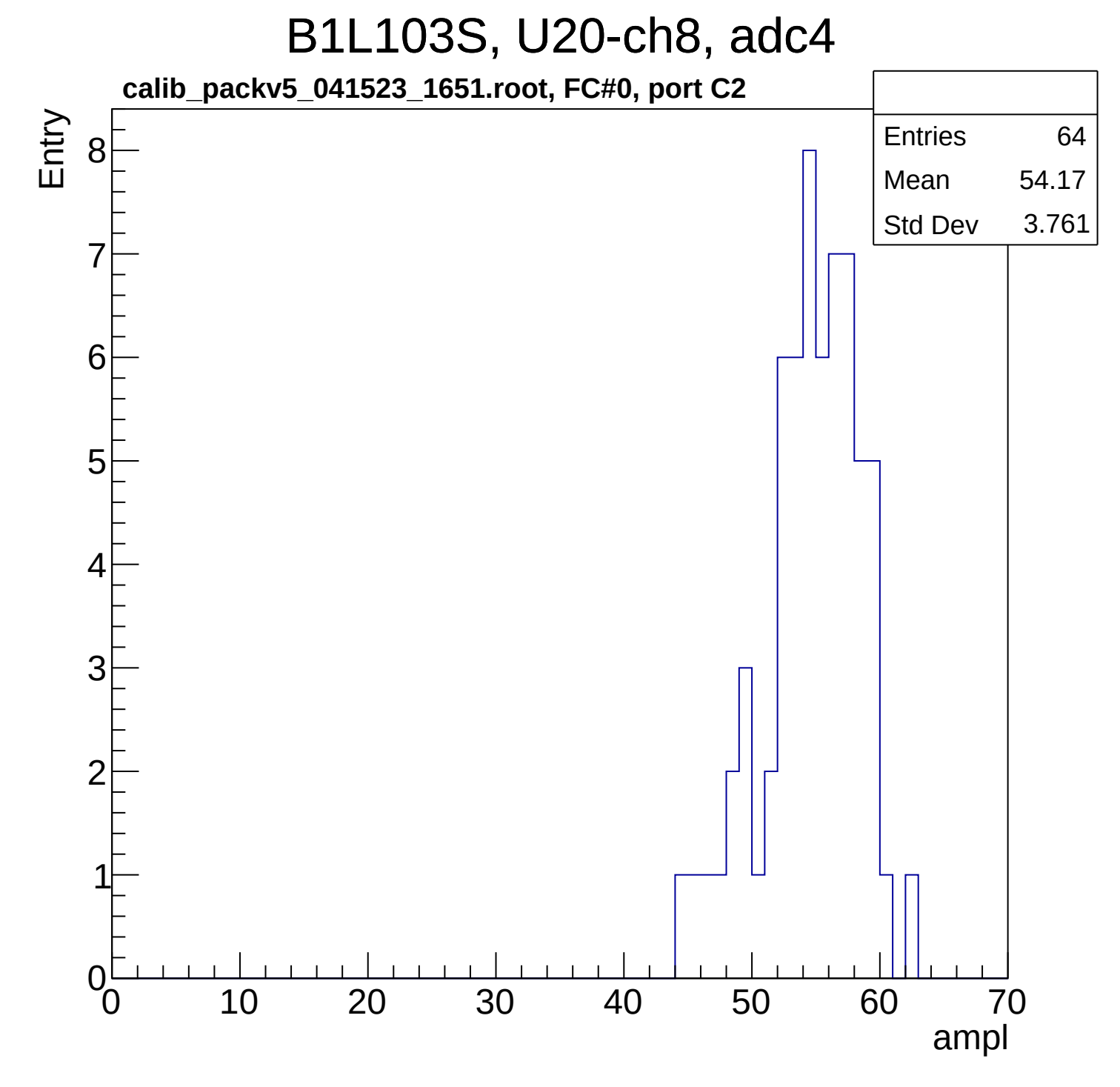
B1L103S, U20-ch8, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 54.17
Std Dev 3.761
Entry
ampl
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5
6
7
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0
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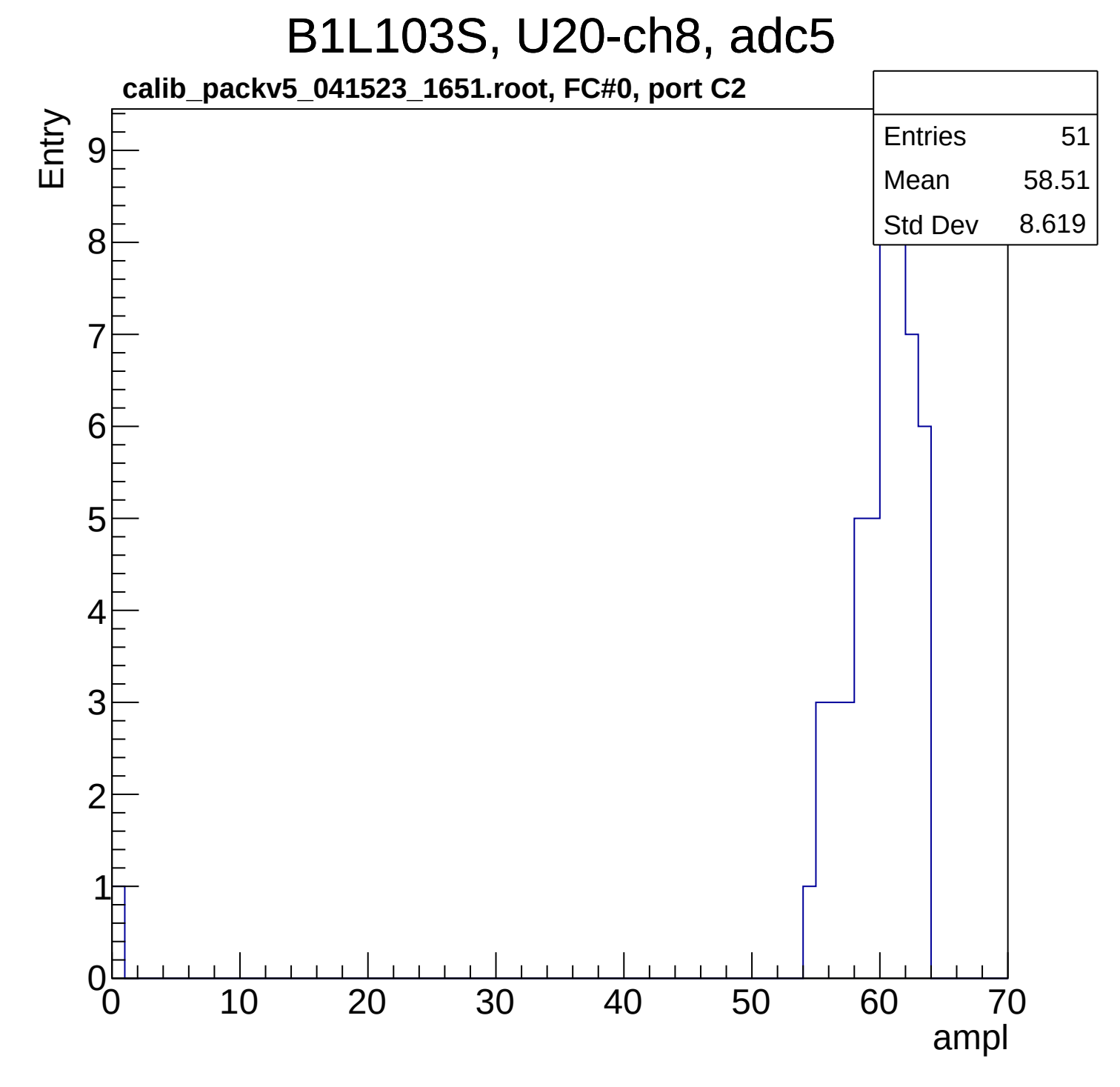
B1L103S, U20-ch8, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 58.51
Std Dev 8.619
Entry
ampl
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6
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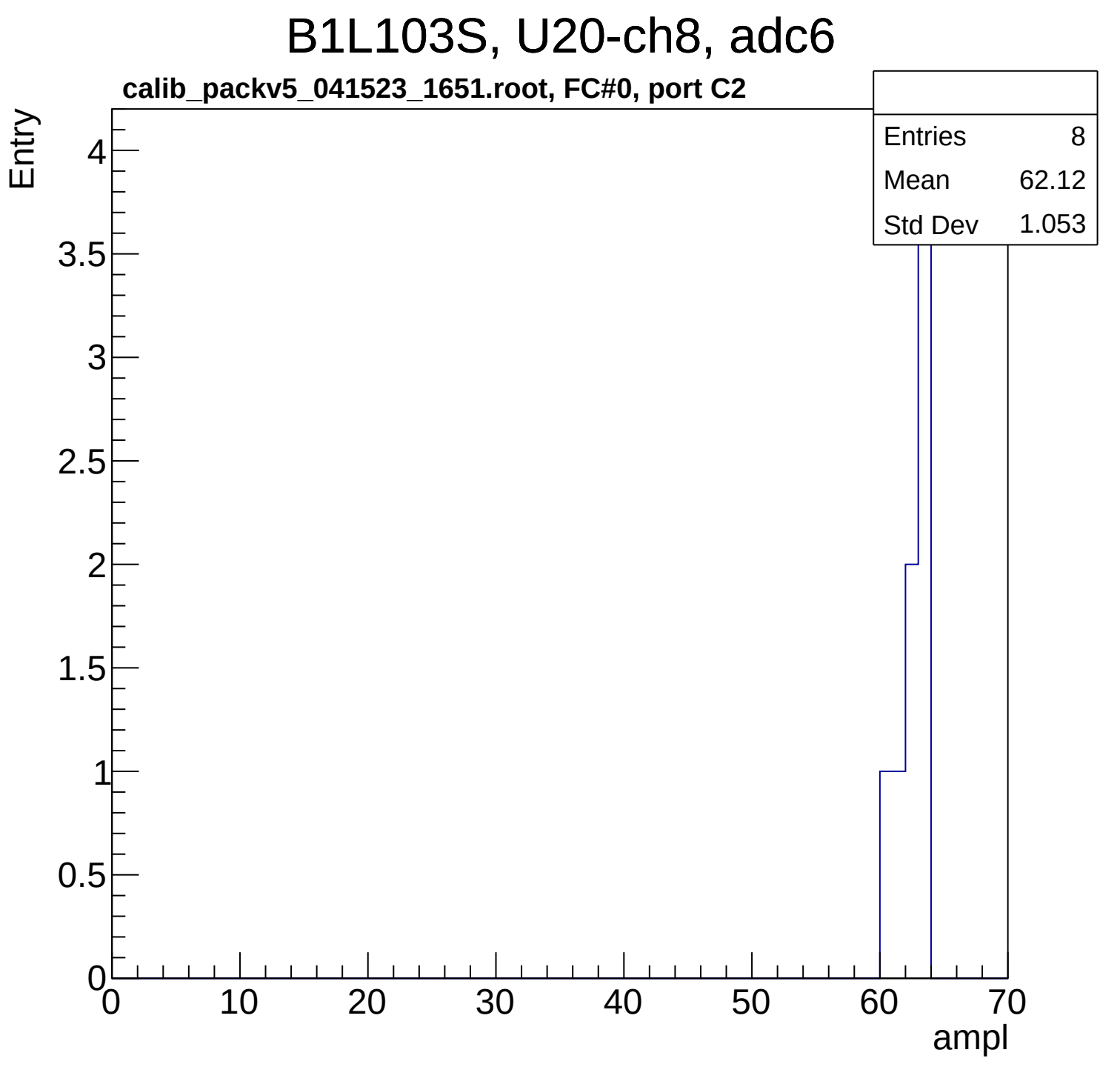
B1L103S, U20-ch8, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 62.12
Std Dev 1.053
Entry
ampl
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1.5
2
2.5
3
3.5
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0
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20
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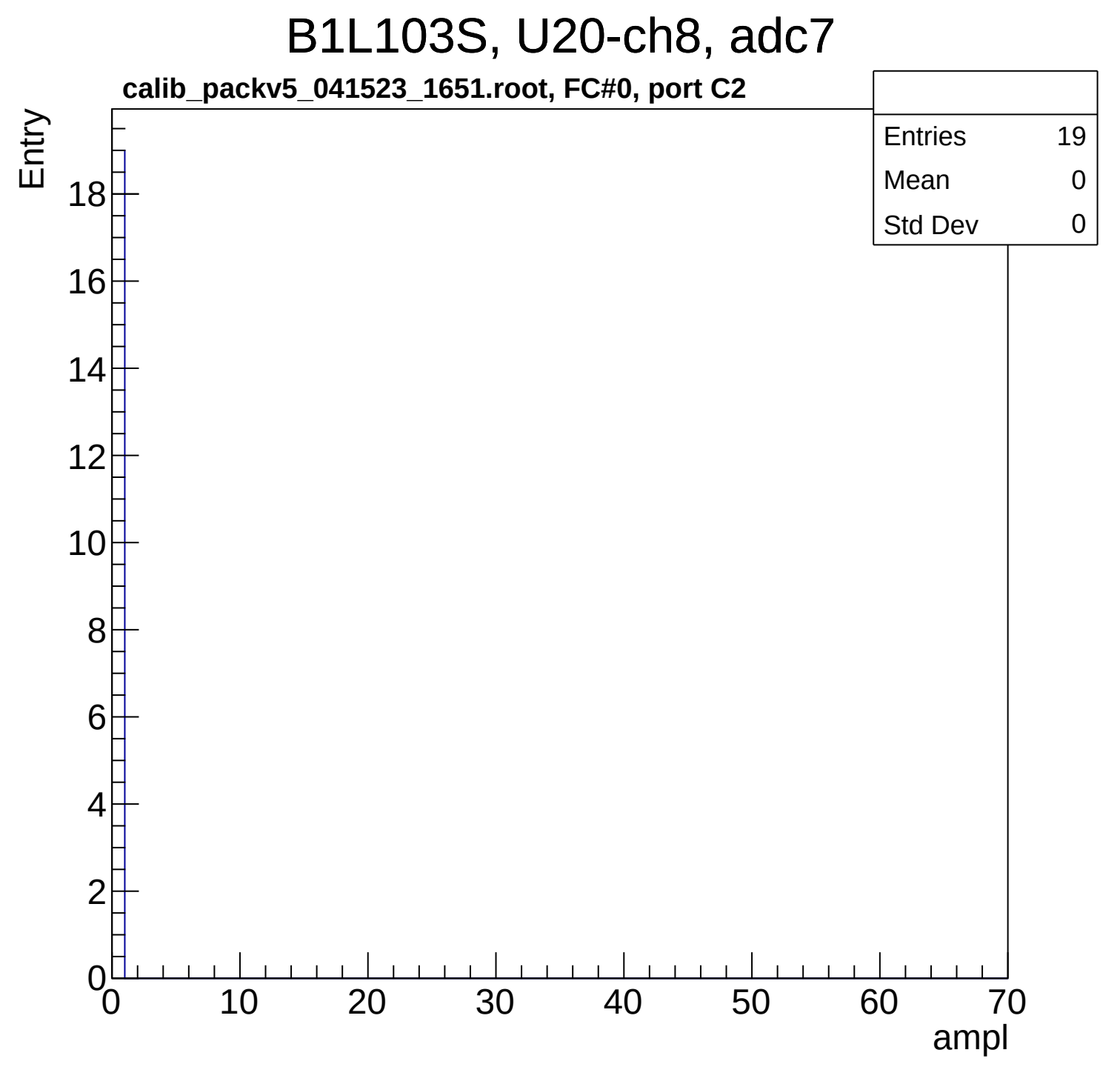
B1L103S, U20-ch8, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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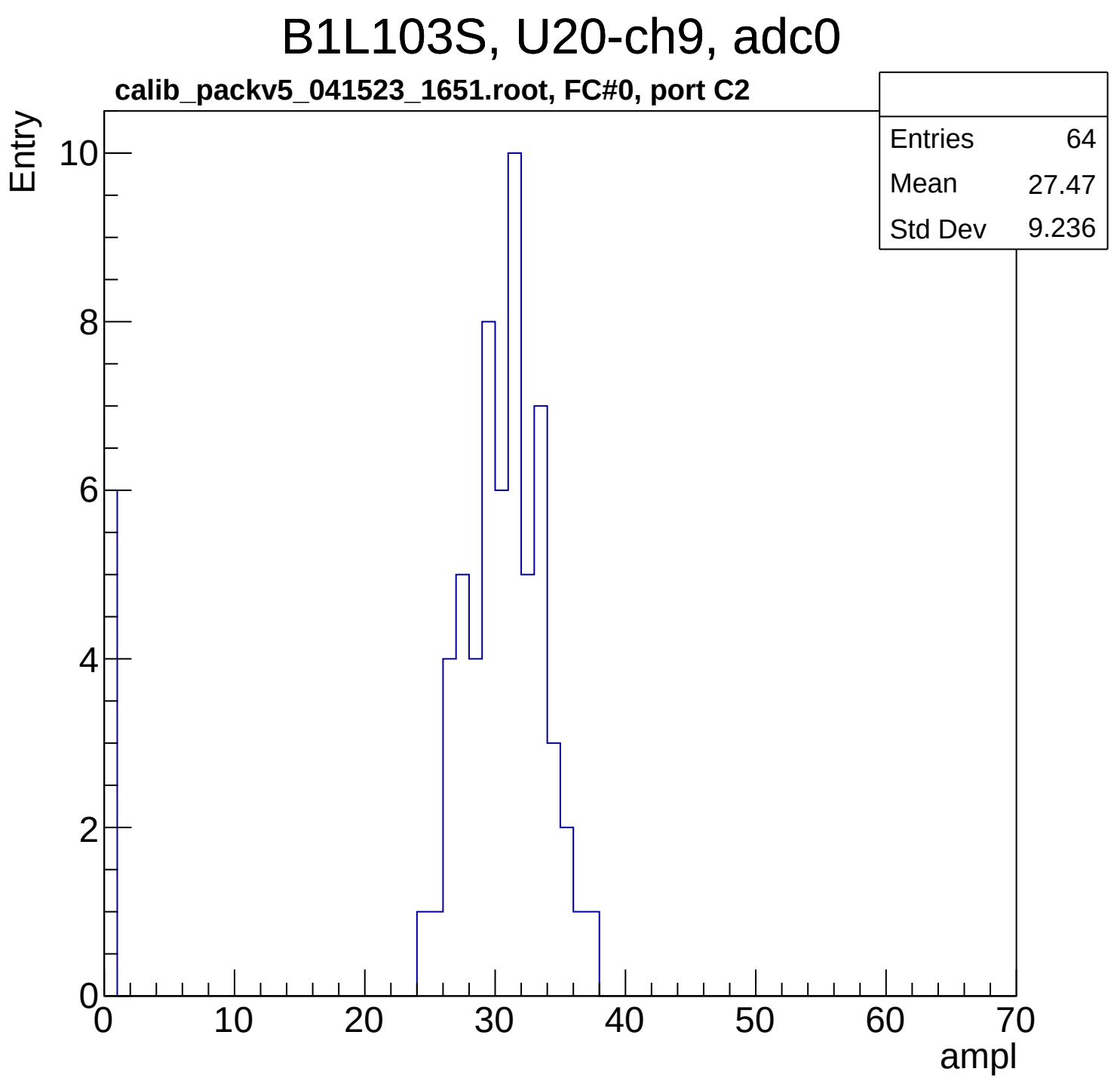
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch9, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 27.47
Std Dev 9.236
Entry
ampl
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4
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0
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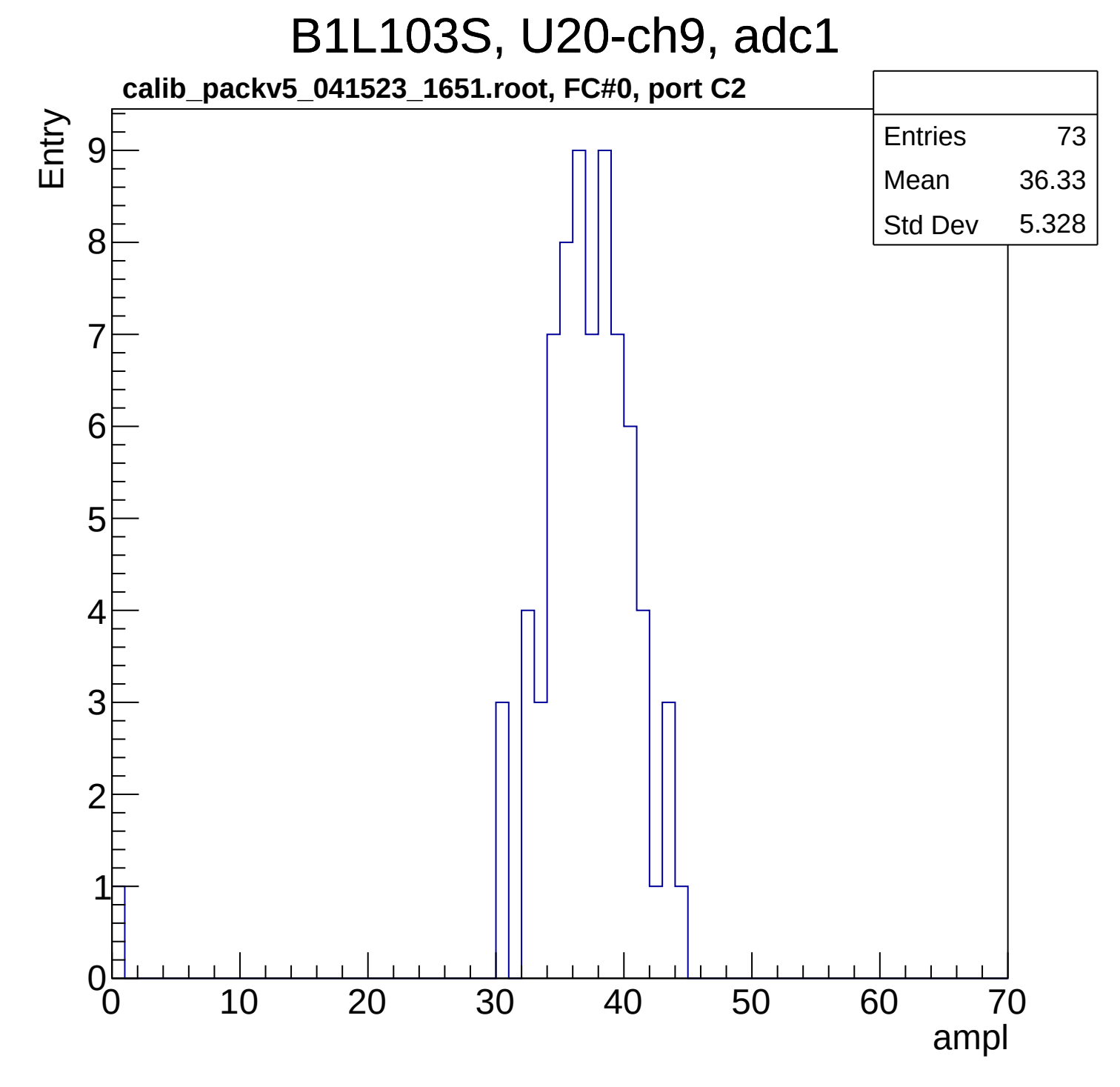
B1L103S, U20-ch9, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 36.33
Std Dev 5.328
Entry
ampl
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2
3
4
5
6
7
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0
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40
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60
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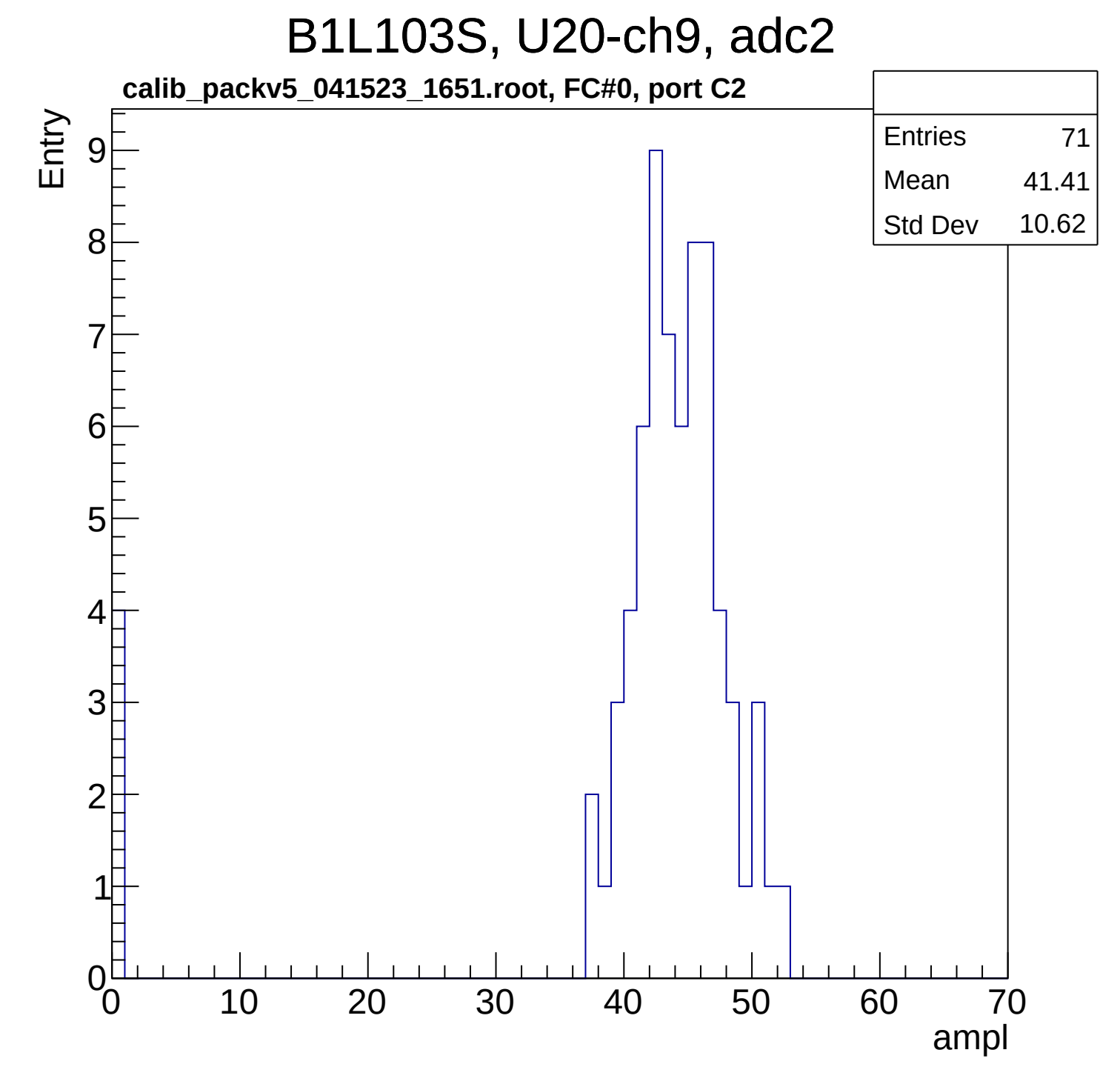
B1L103S, U20-ch9, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 41.41
Std Dev 10.62
Entry
ampl
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2
3
4
5
6
7
8
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0
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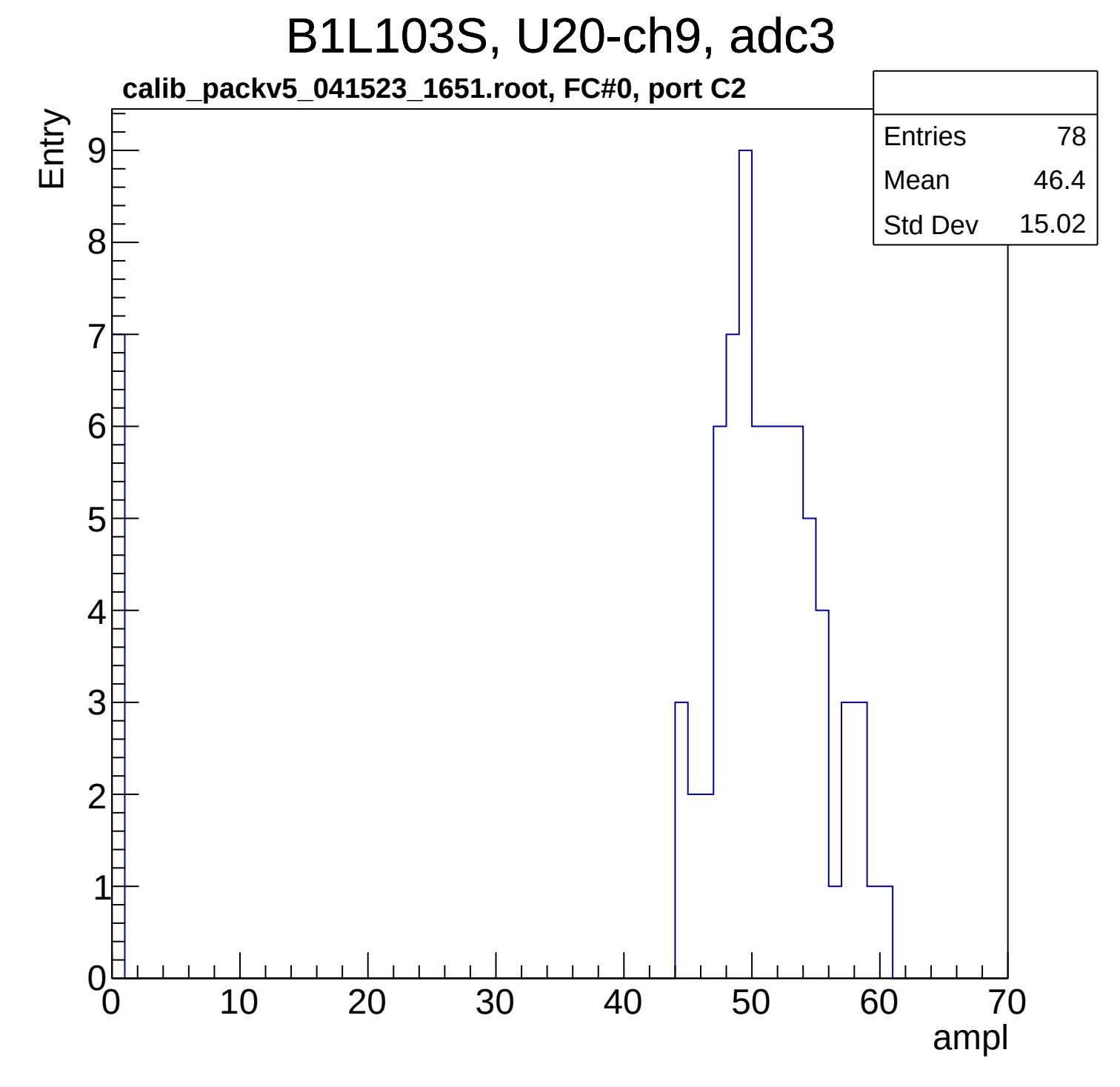
B1L103S, U20-ch9, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 46.4
Std Dev 15.02
Entry
ampl
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2
3
4
5
6
7
8
9
0
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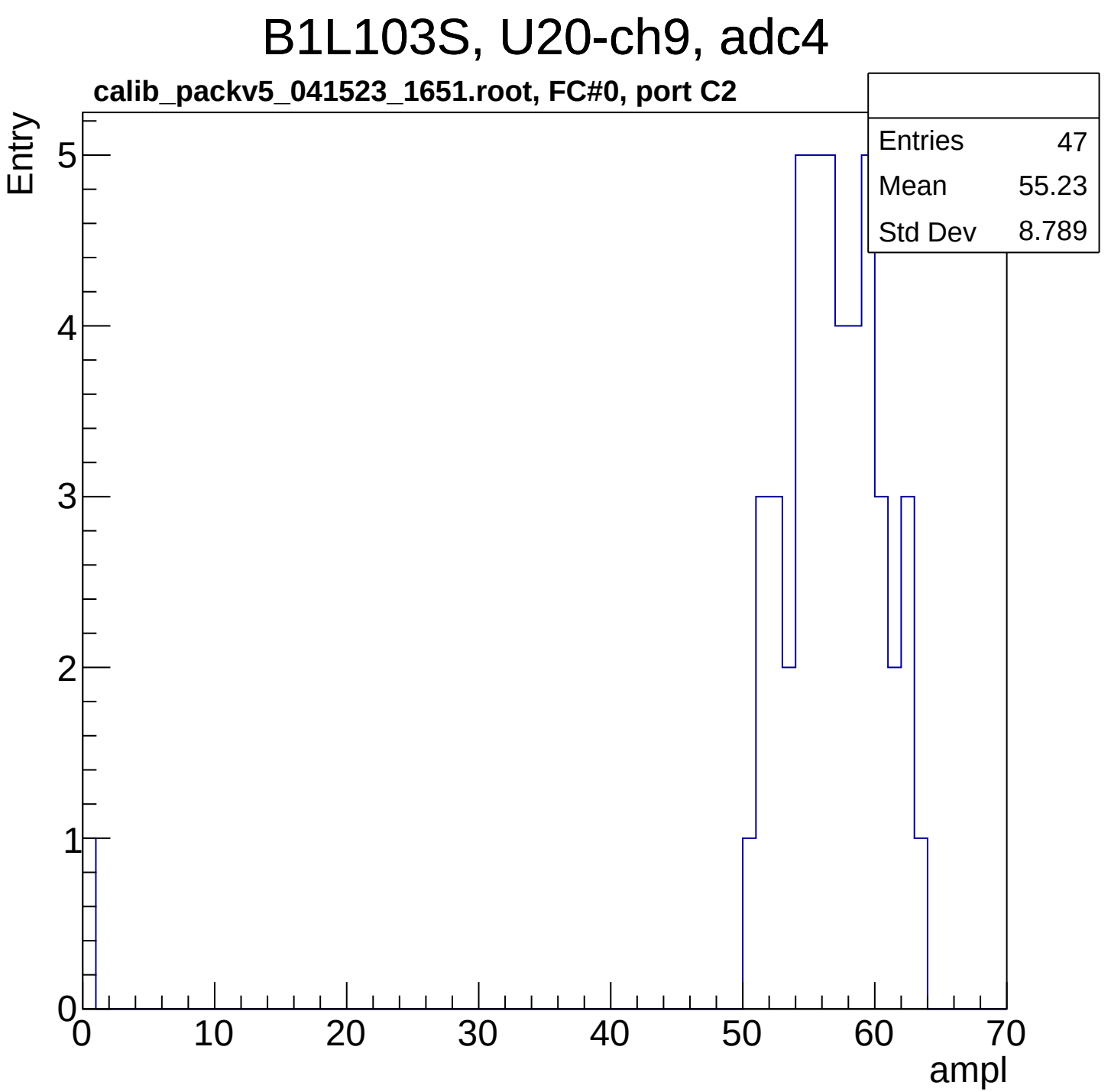
B1L103S, U20-ch9, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 55.23
Std Dev 8.789
Entry
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1
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3
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5
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50
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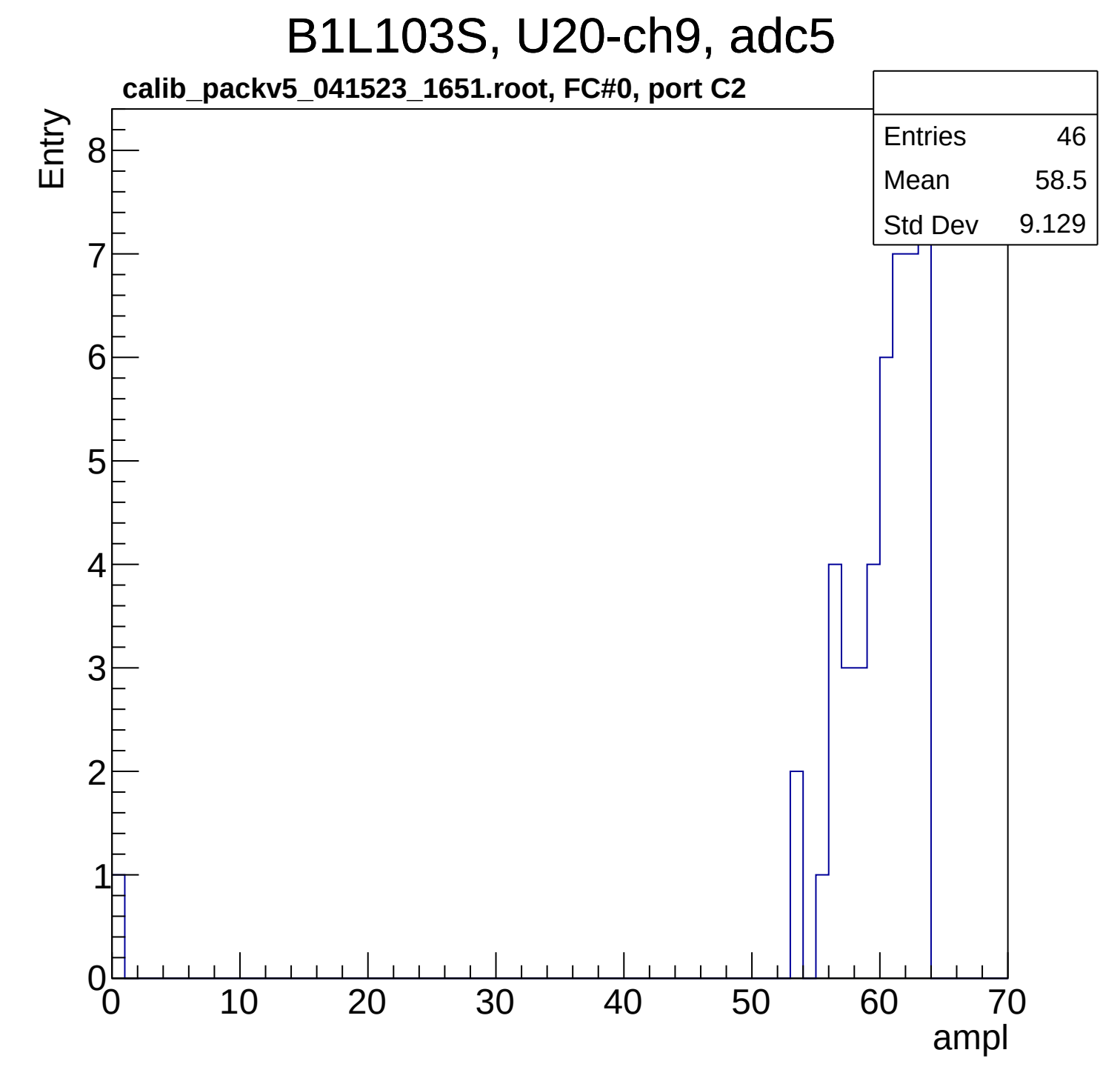
70
ampl


B1L103S, U20-ch9, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 58.5
Std Dev 9.129
Entry
ampl
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5
6
7
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0
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40
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60
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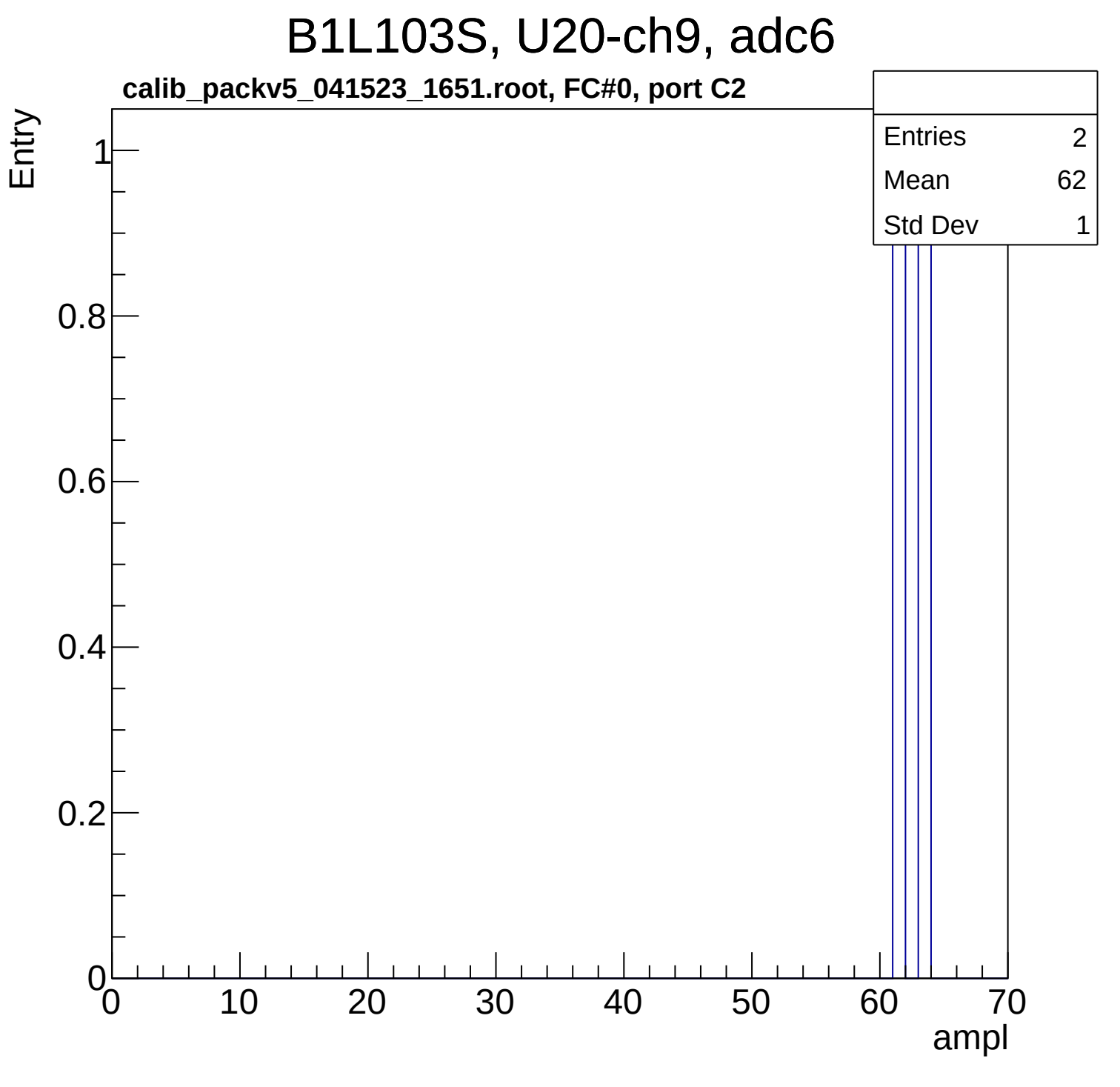
B1L103S, U20-ch9, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 62
Std Dev 1
Entry
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0.6
0.4
0.2
0
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10
20
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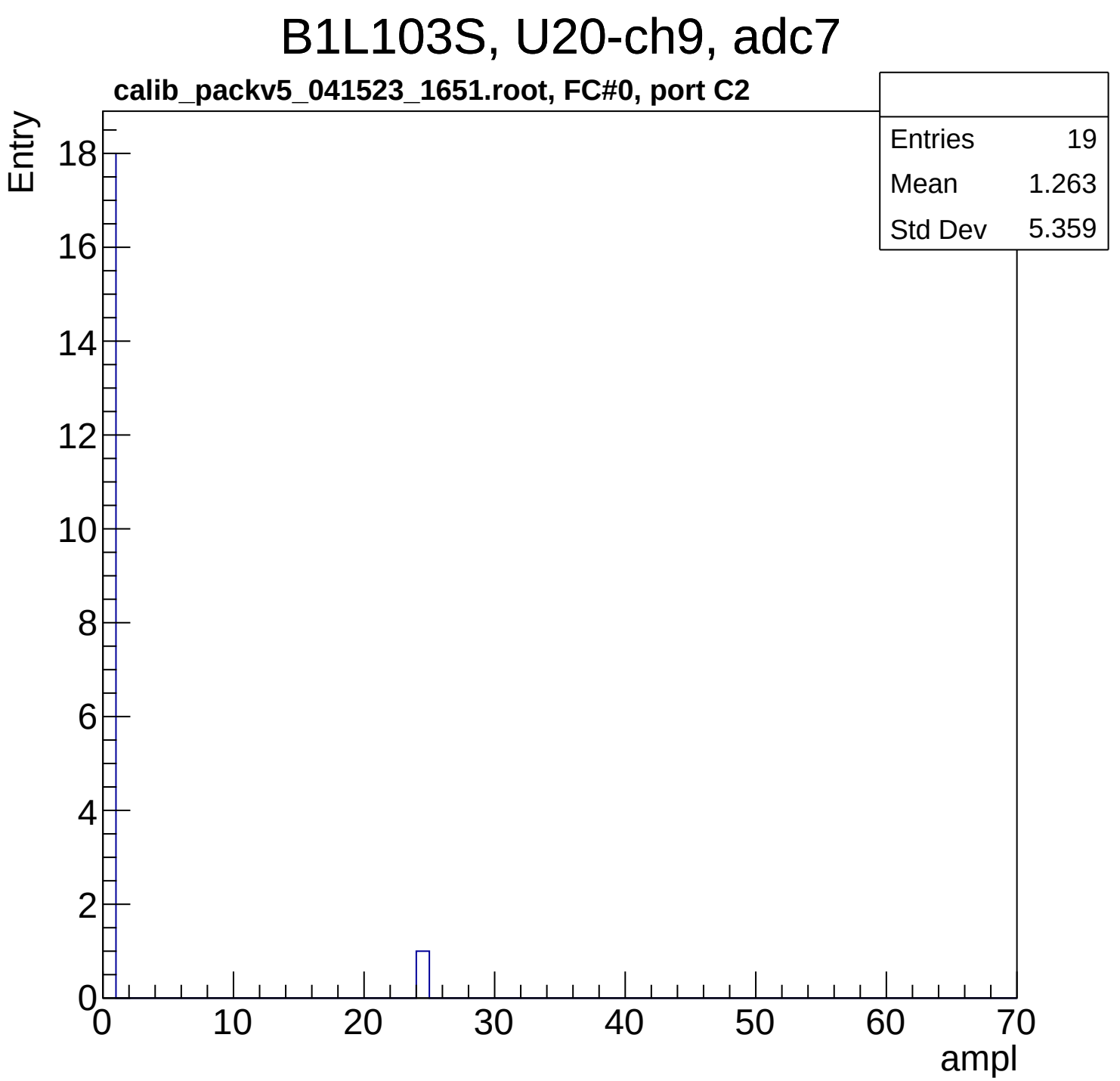
50
60
70
ampl


B1L103S, U20-ch9, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.263
Std Dev 5.359
Entry
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6
8
10
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14
16
18
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10
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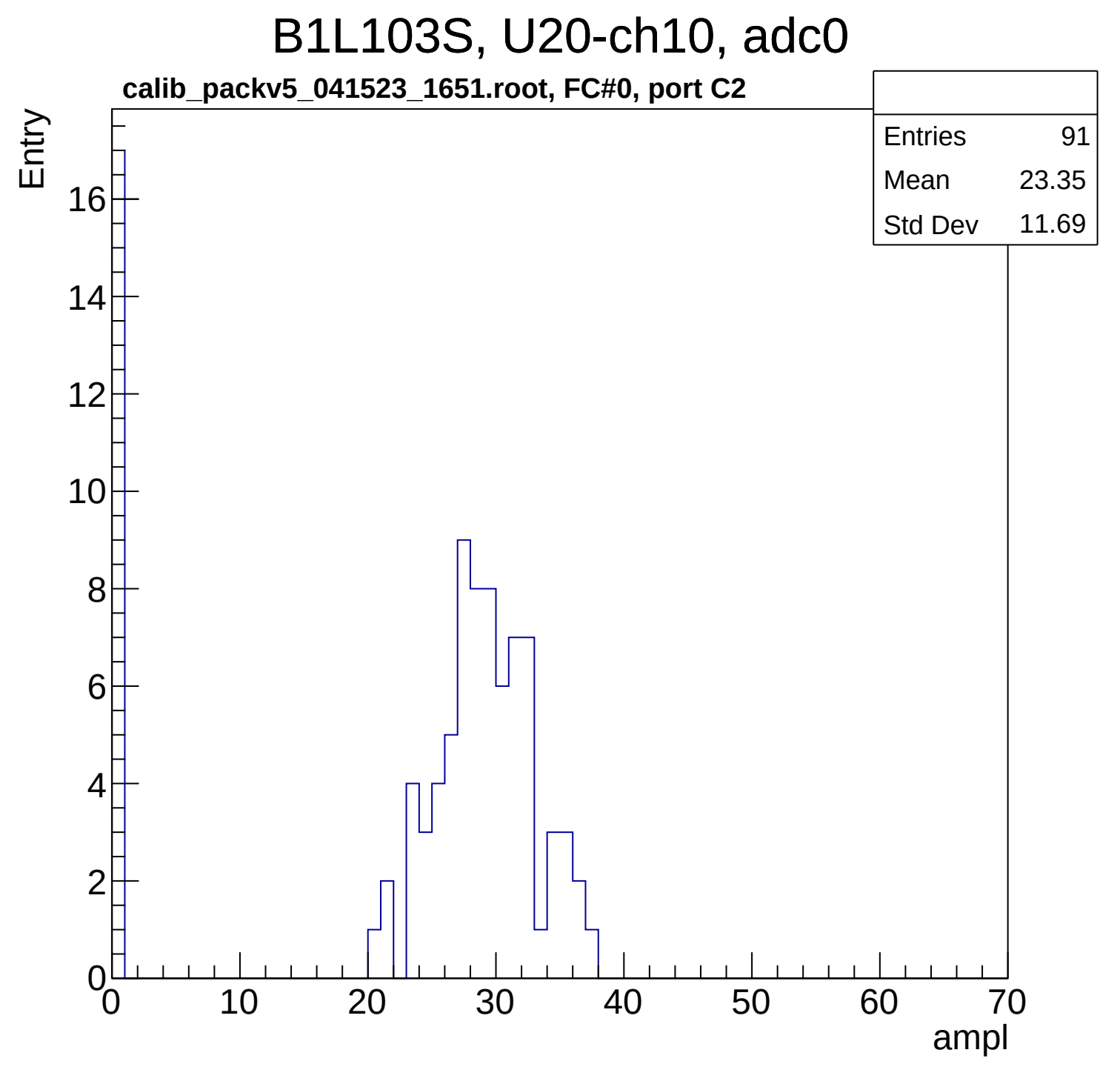
70
ampl


B1L103S, U20-ch10, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 23.35
Std Dev 11.69
Entry
ampl
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4
6
8
10
12
14
16
0
10
20
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40
50
60
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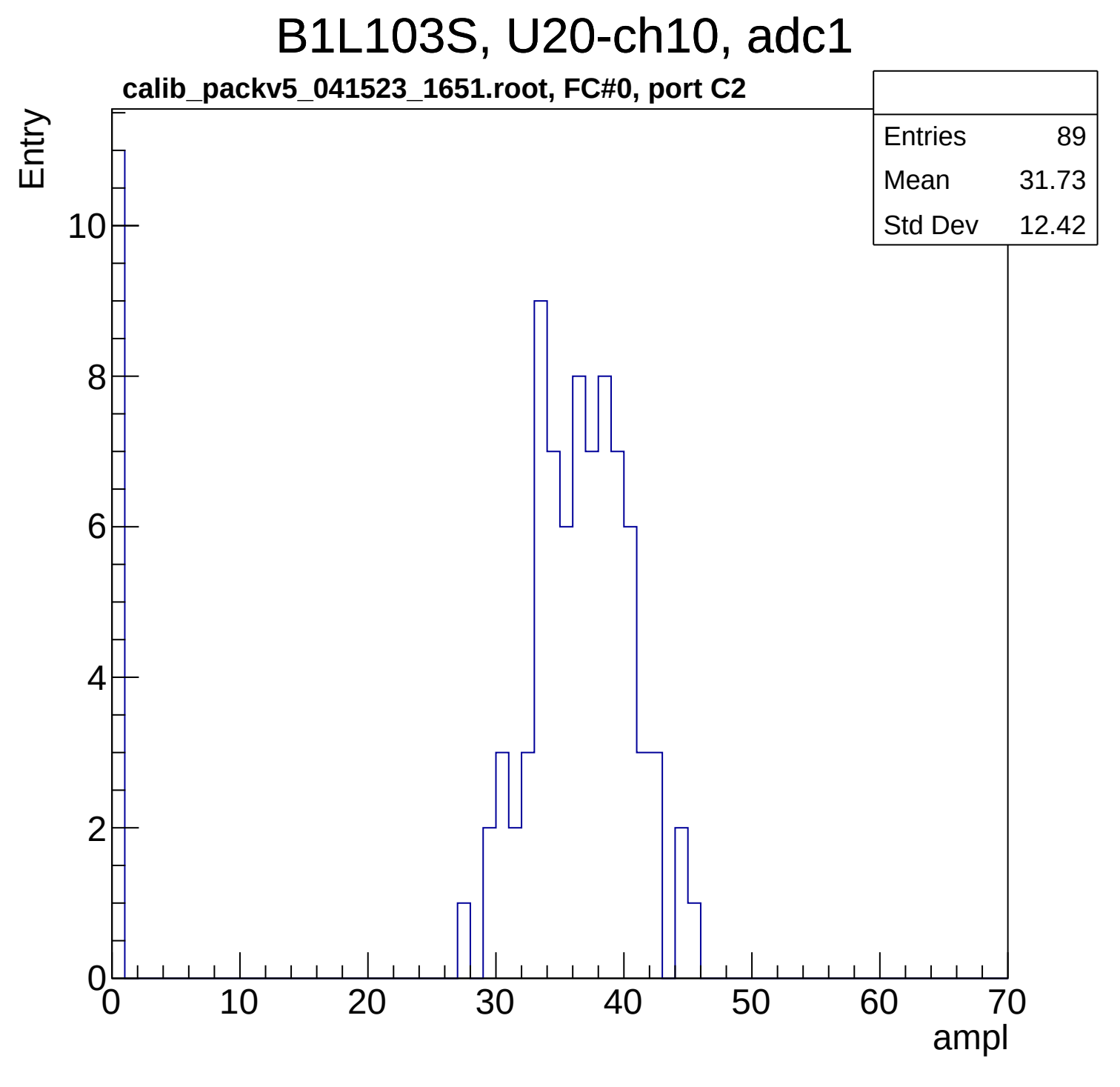
B1L103S, U20-ch10, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 31.73
Std Dev 12.42
Entry
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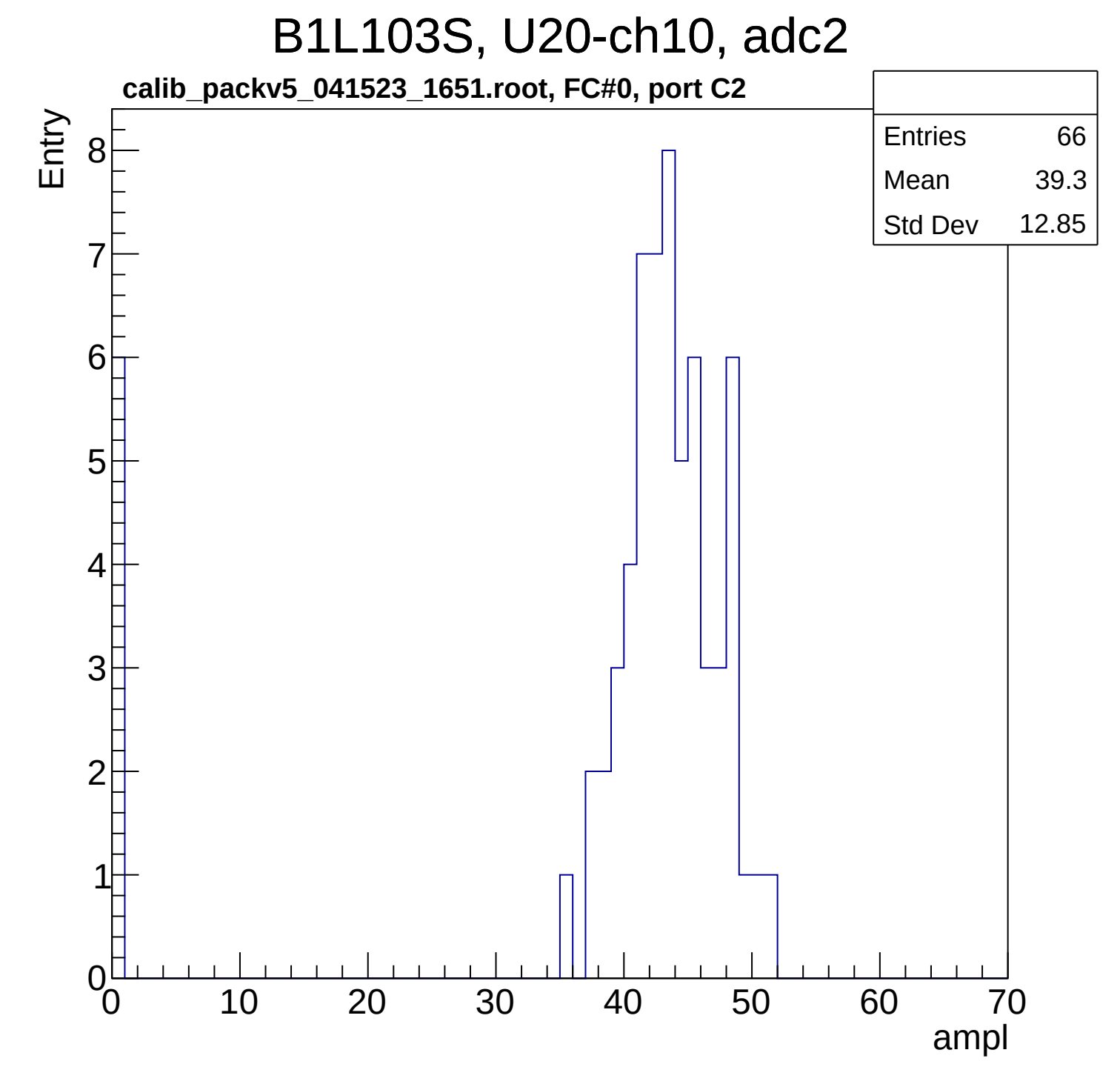
50
60
70
ampl


B1L103S, U20-ch10, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 39.3
Std Dev 12.85
Entry
ampl
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6
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0
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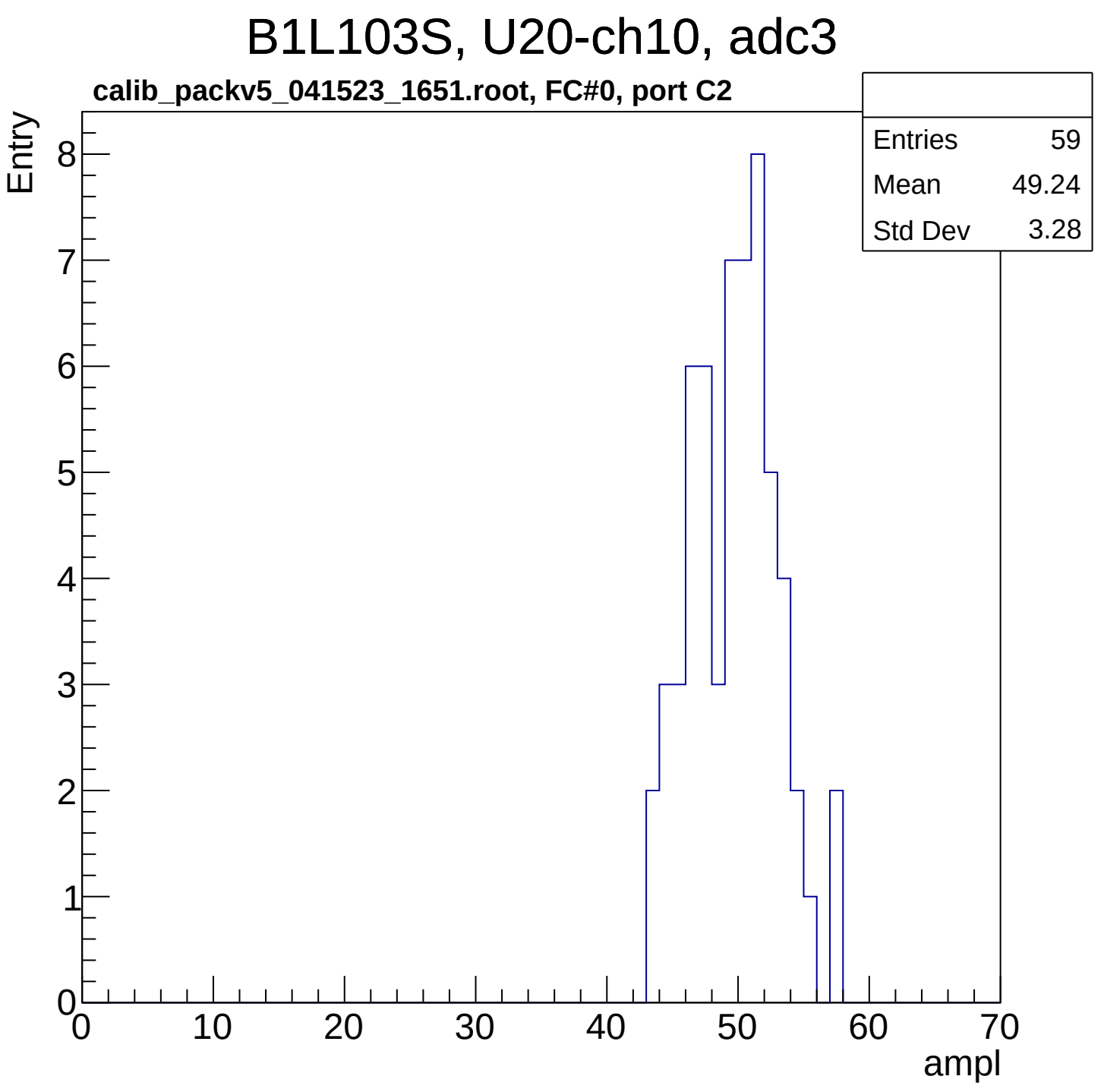
B1L103S, U20-ch10, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 49.24
Std Dev 3.28
Entry
ampl
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7
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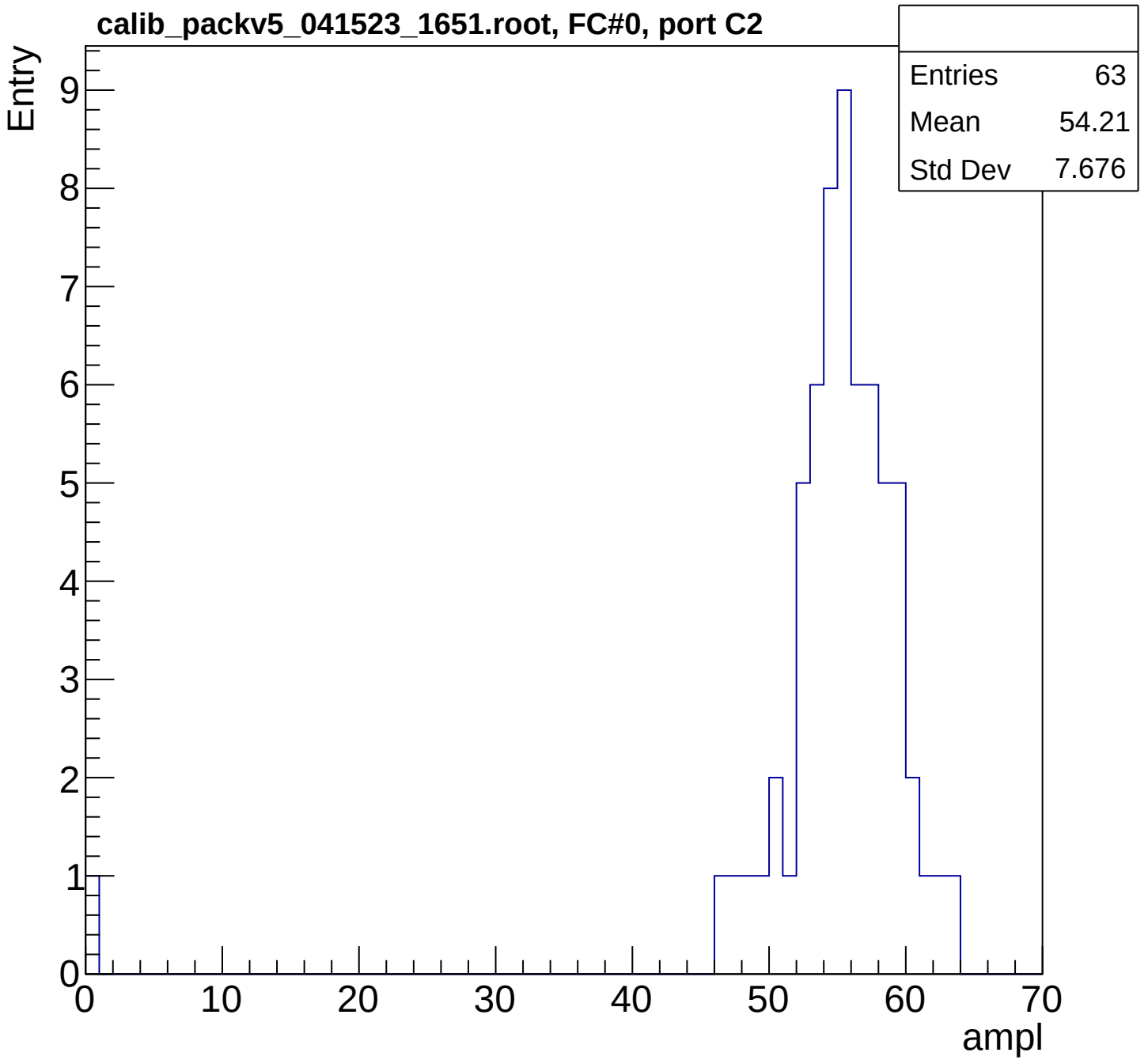
B1L103S, U20-ch10, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 54.21
Std Dev 7.676
Entry
ampl
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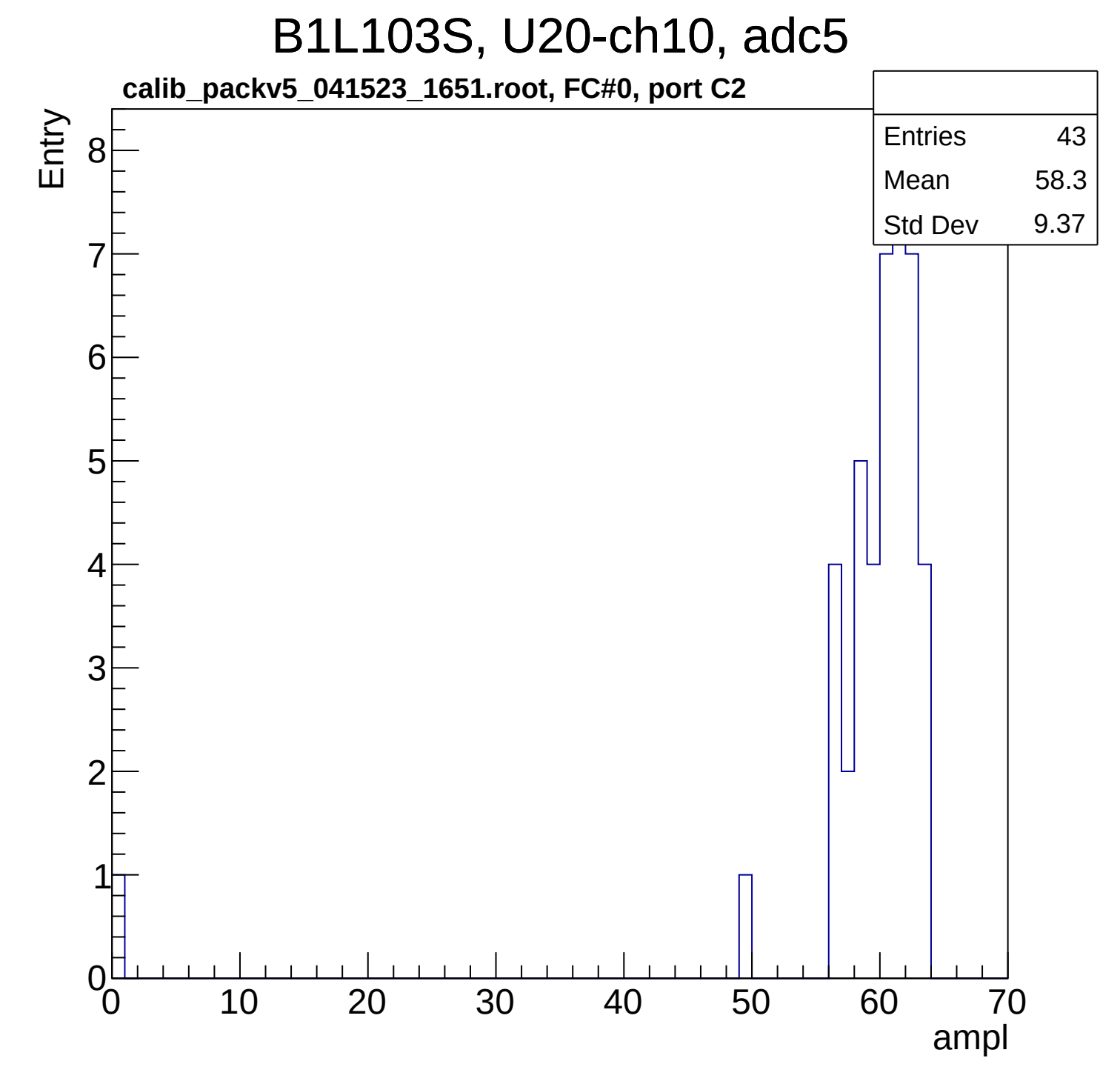
B1L103S, U20-ch10, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 58.3
Std Dev 9.37
Entry
ampl
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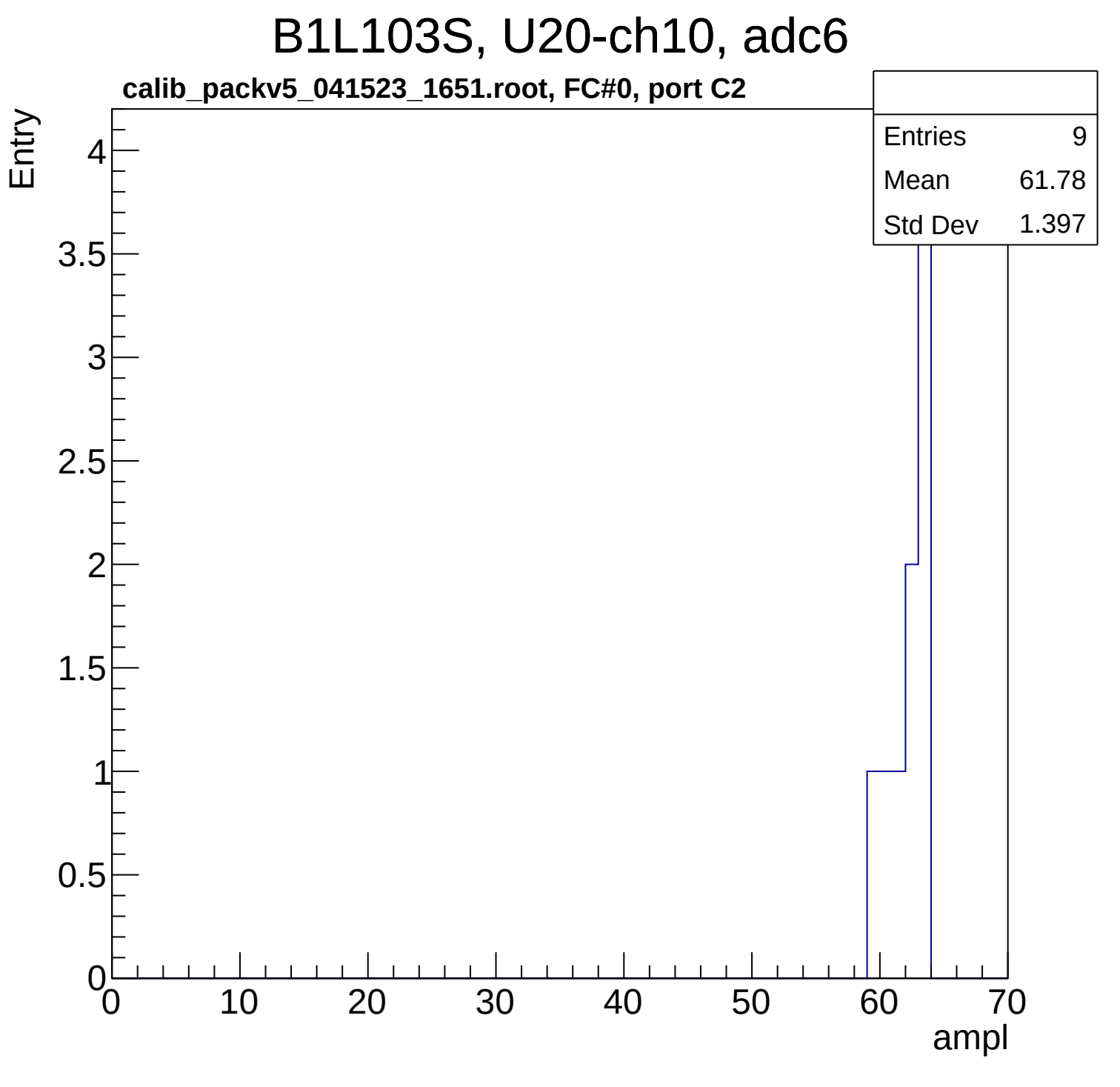
B1L103S, U20-ch10, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 61.78
Std Dev 1.397
Entry
ampl
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3.5
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0
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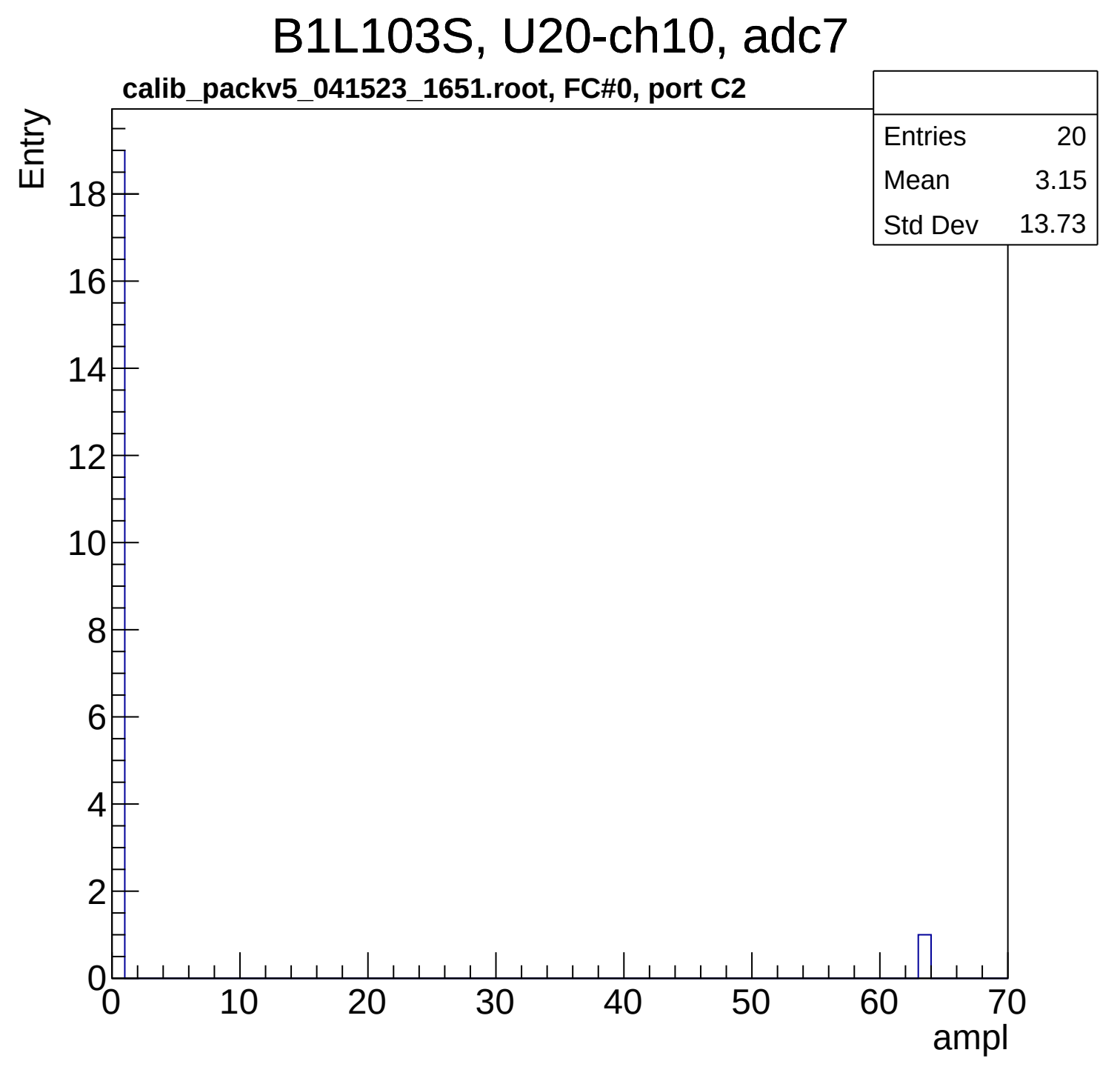
B1L103S, U20-ch10, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
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10
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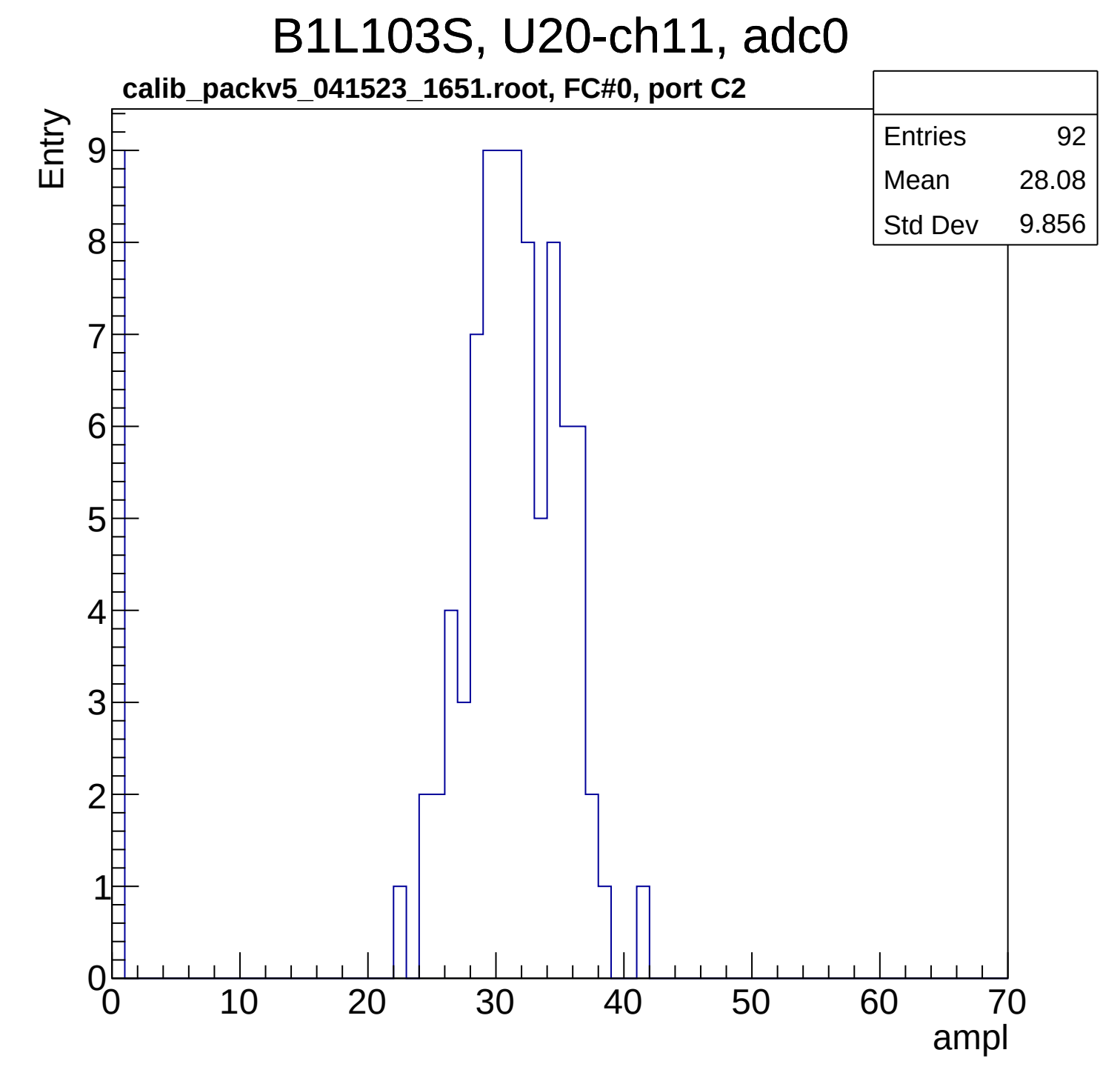
70
ampl


B1L103S, U20-ch11, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 28.08
Std Dev 9.856
Entry
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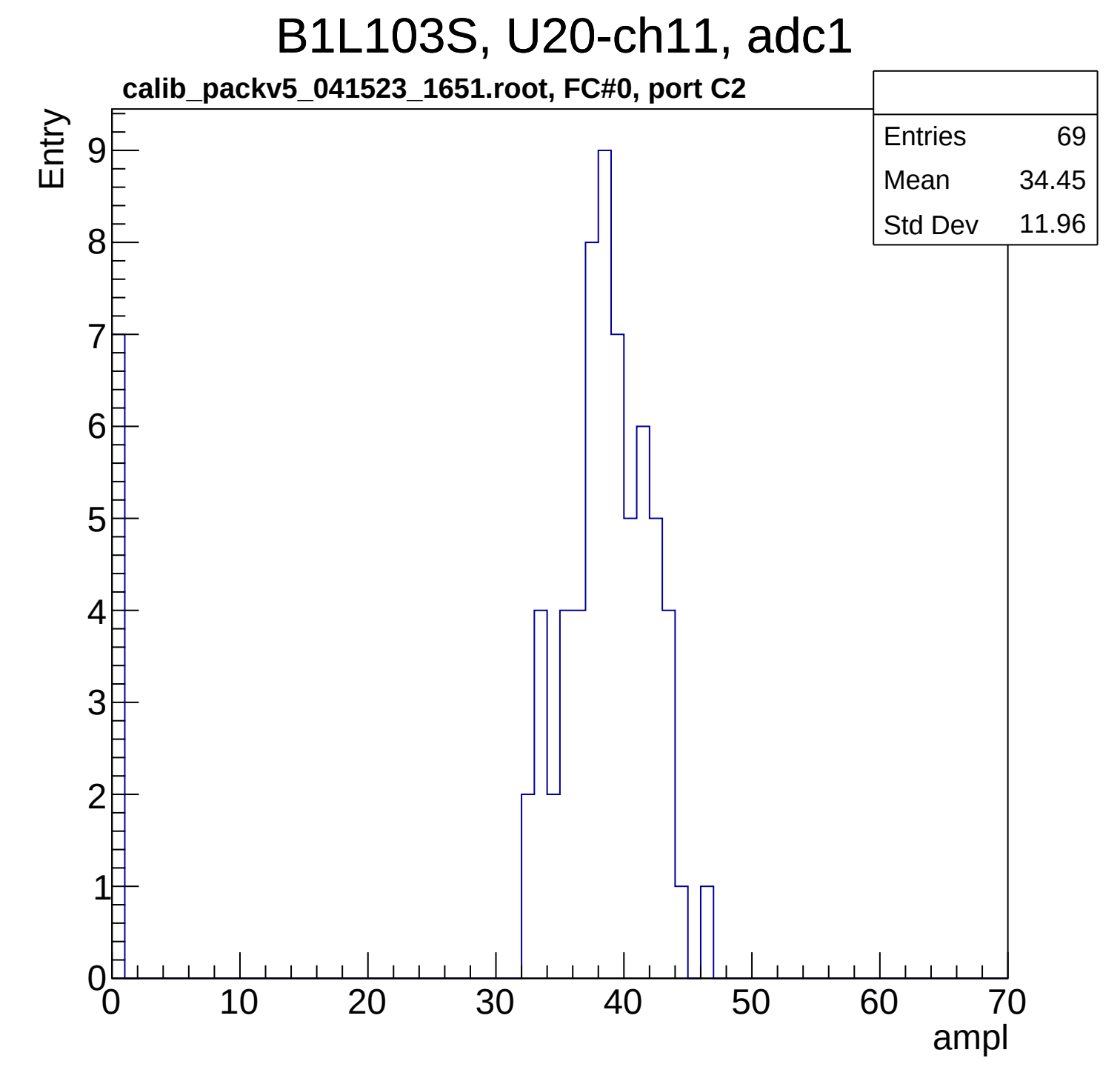
B1L103S, U20-ch11, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 34.45
Std Dev 11.96
Entry
ampl
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6
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0
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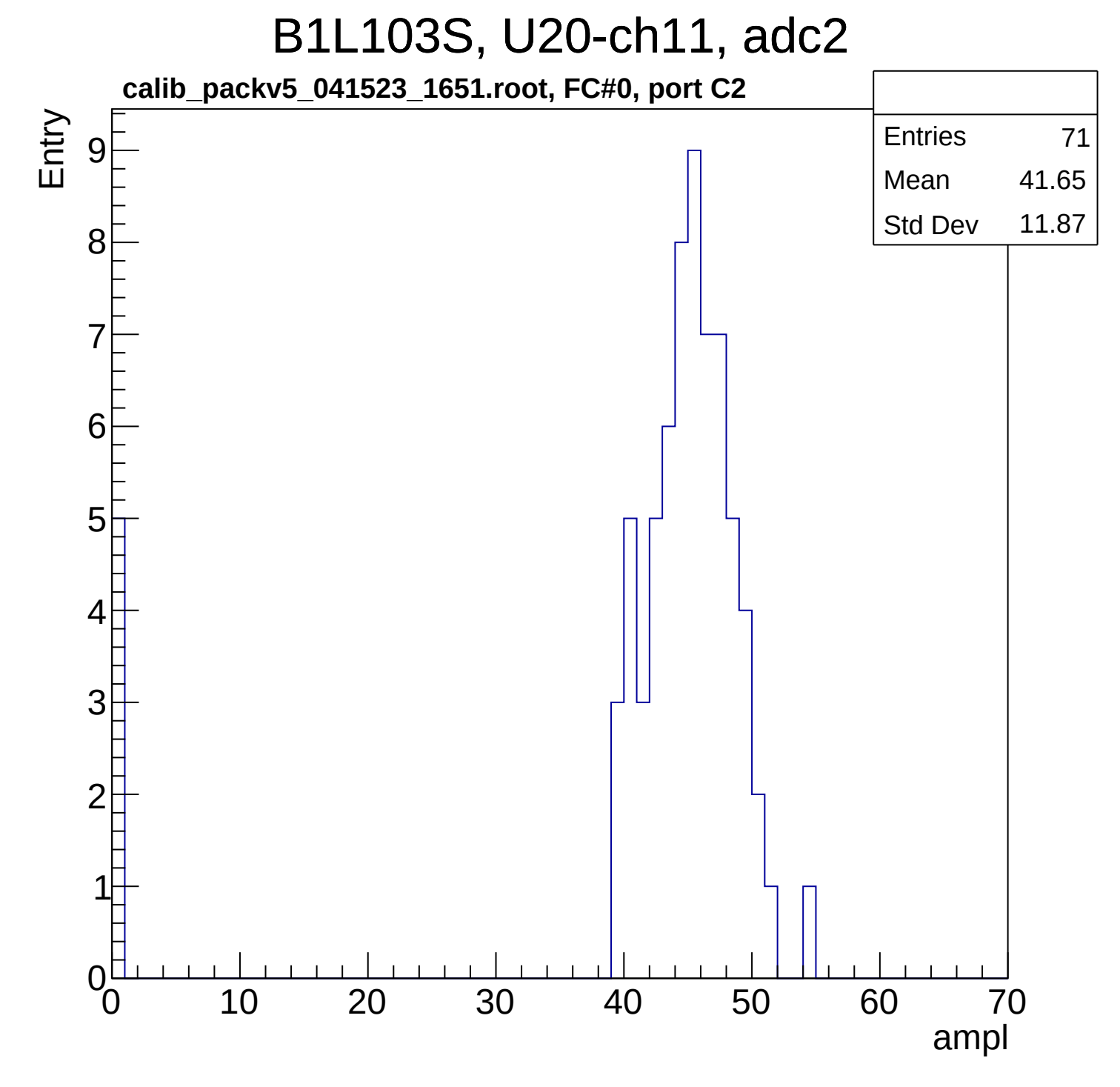
B1L103S, U20-ch11, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 41.65
Std Dev 11.87
Entry
ampl
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4
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0
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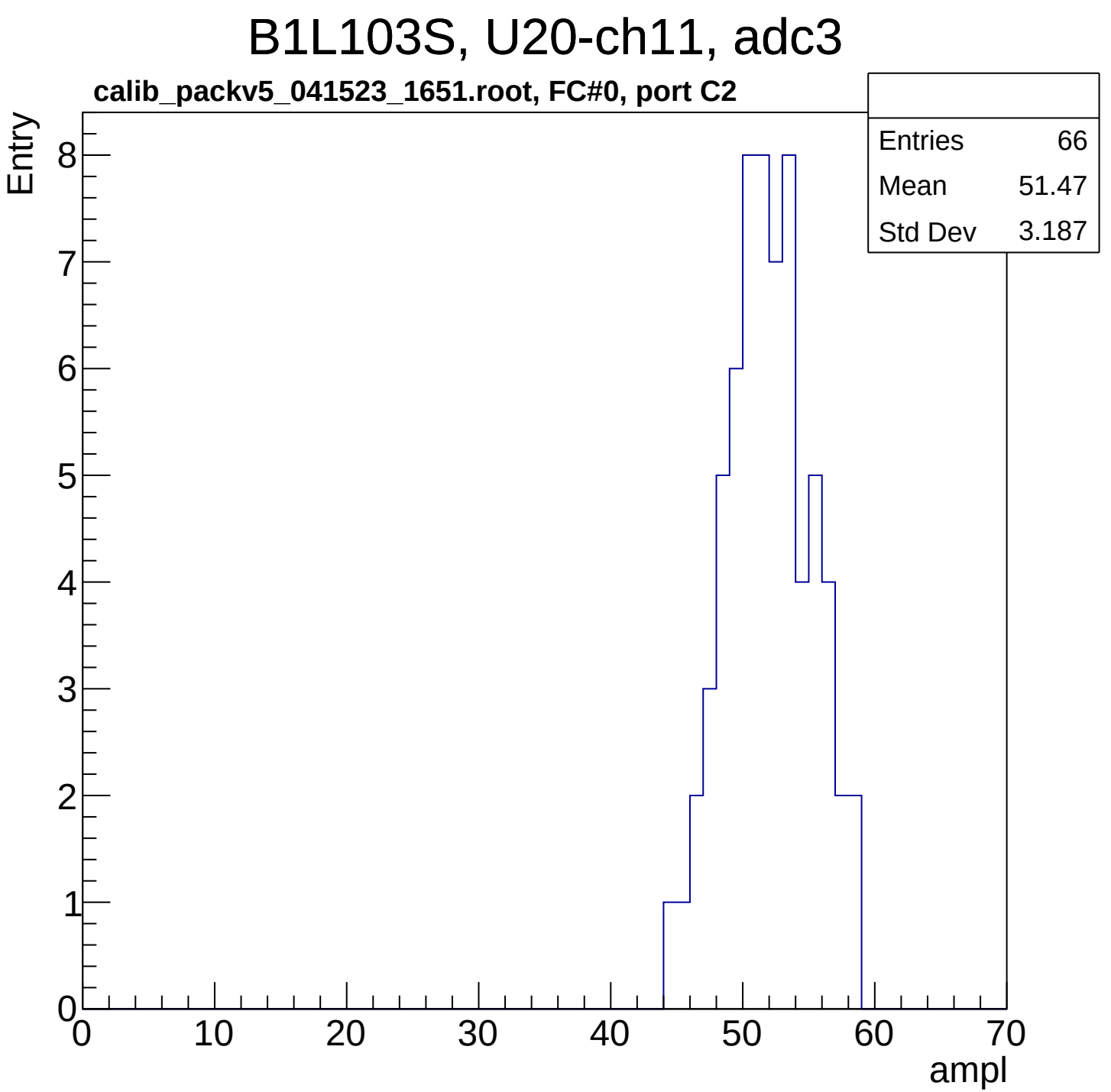
B1L103S, U20-ch11, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 51.47
Std Dev 3.187
Entry
ampl
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4
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0
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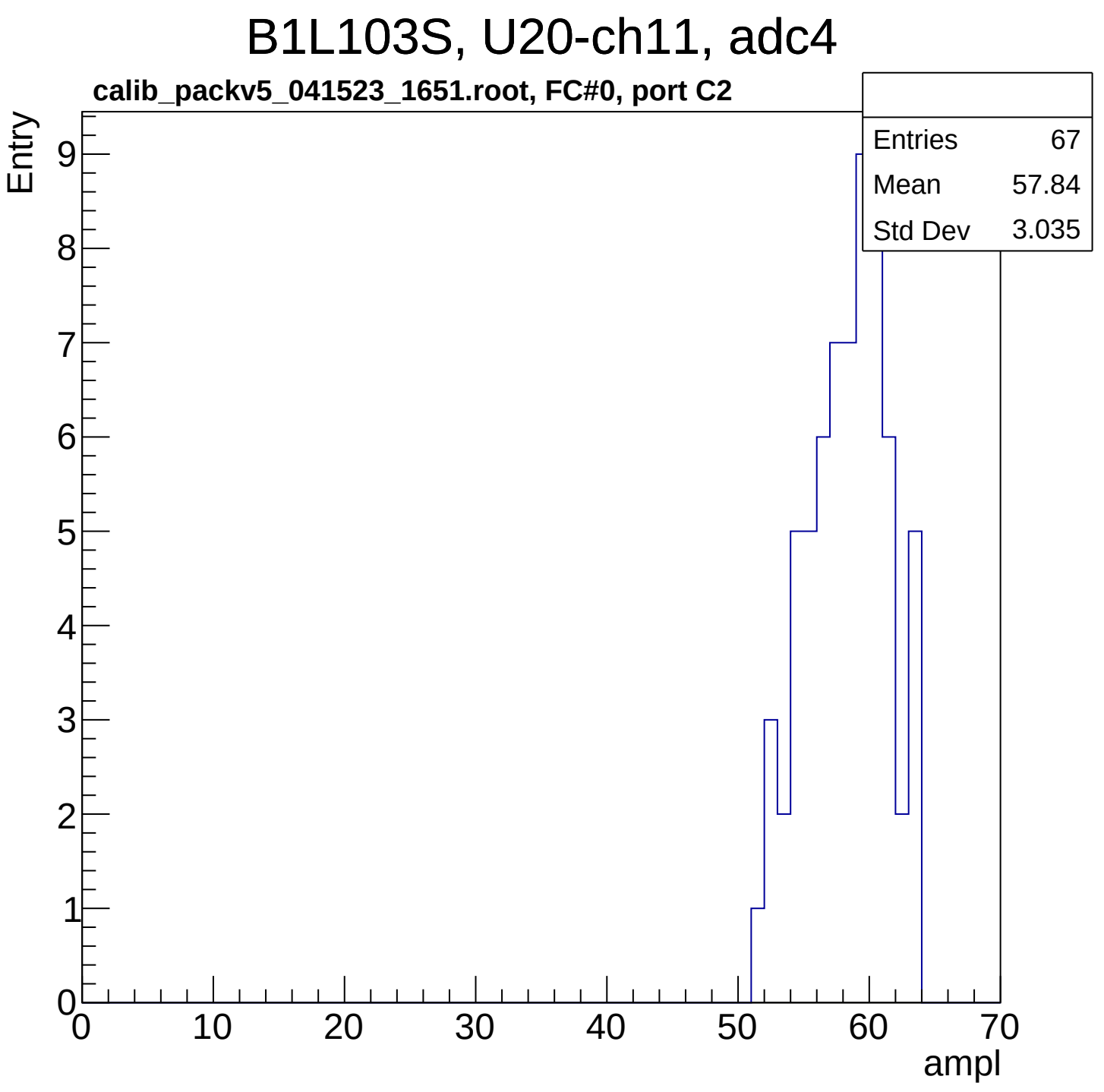
B1L103S, U20-ch11, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 57.84
Std Dev 3.035
Entry
ampl
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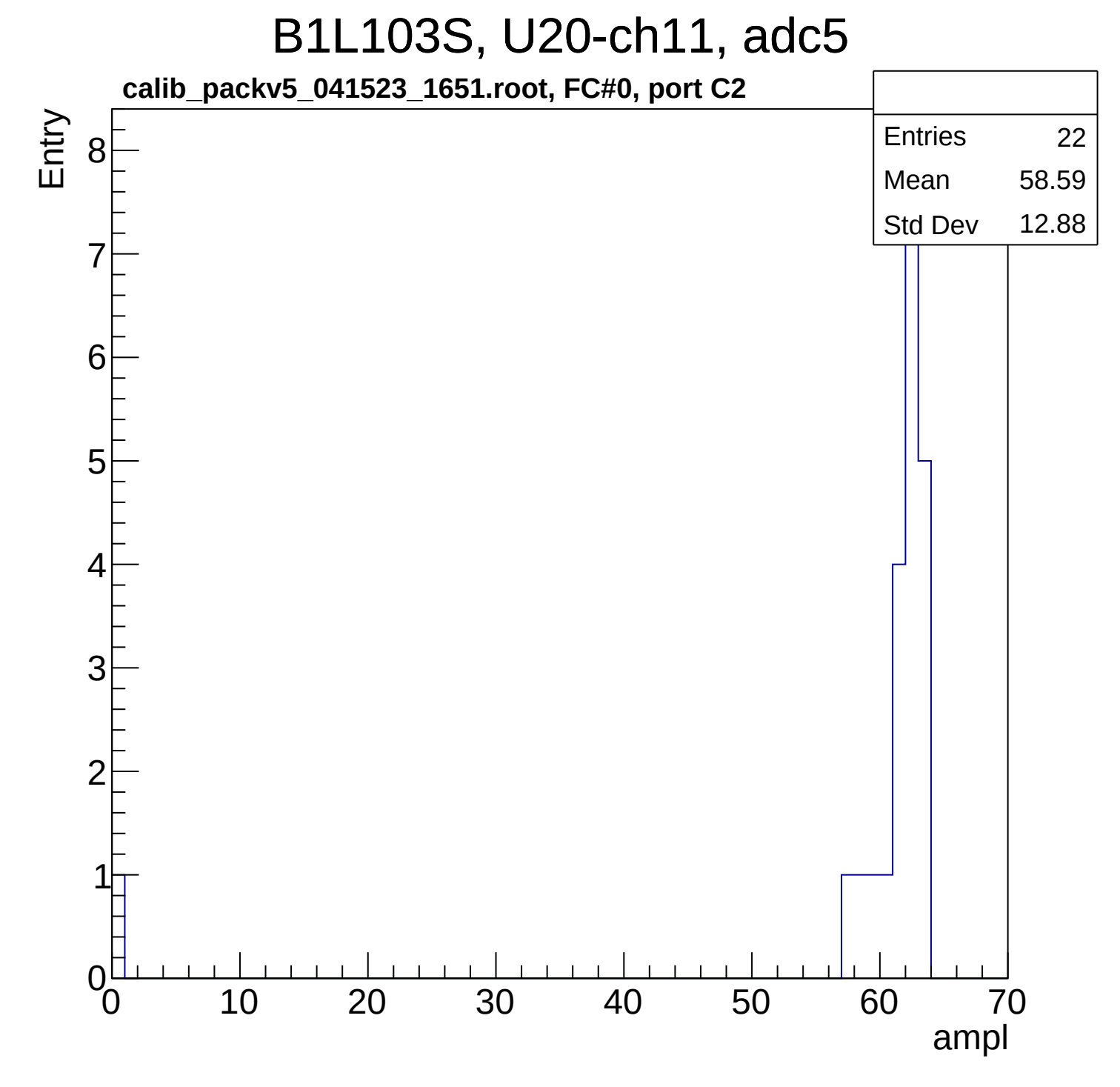
B1L103S, U20-ch11, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 58.59
Std Dev 12.88
Entry
ampl
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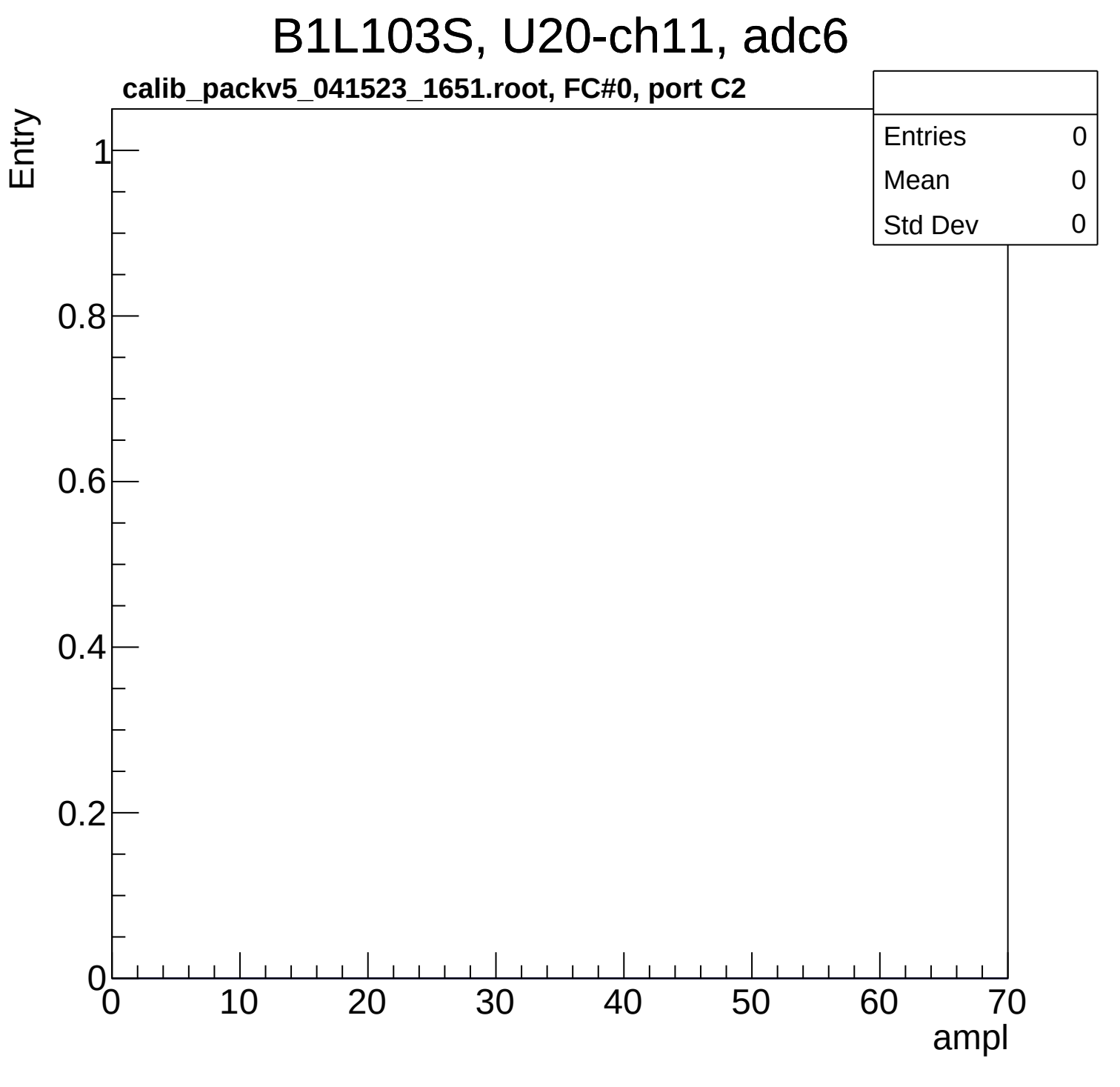
B1L103S, U20-ch11, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 0
Mean 0
Std Dev 0
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0.6
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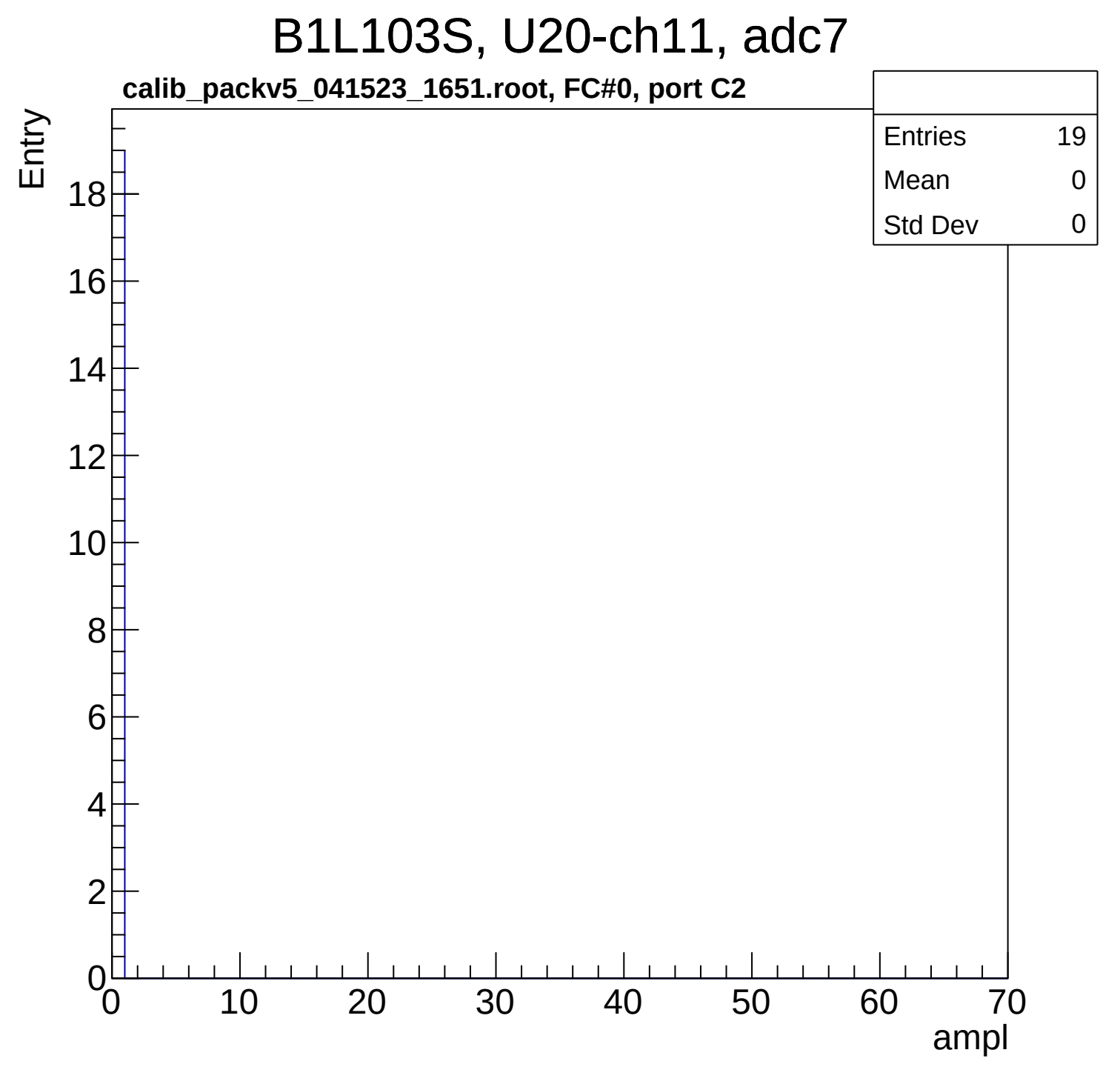
50
60
70
ampl


B1L103S, U20-ch11, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
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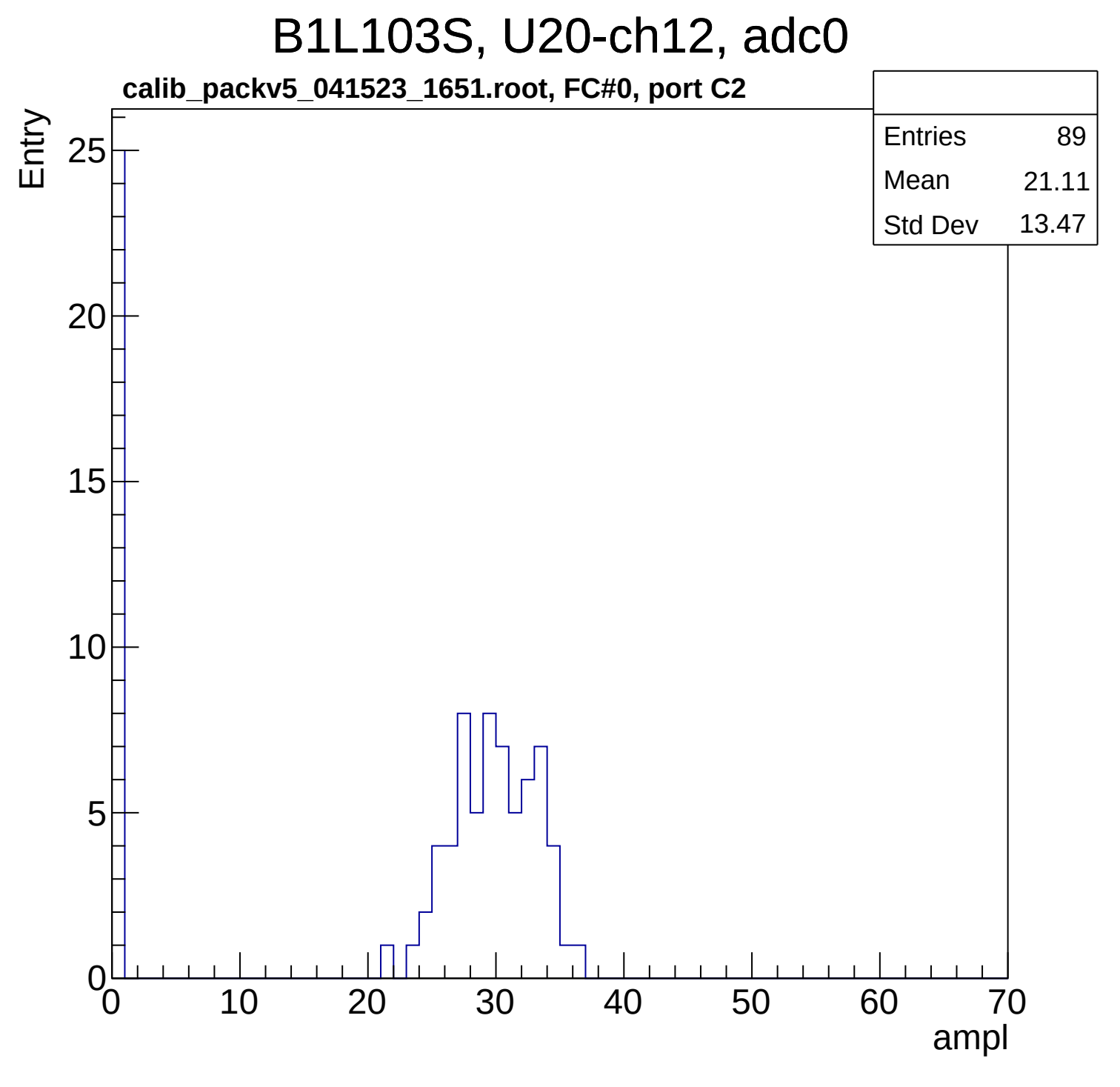
60
70
ampl


B1L103S, U20-ch12, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 21.11
Std Dev 13.47
Entry
0
5
10
15
20
25
0
10
20
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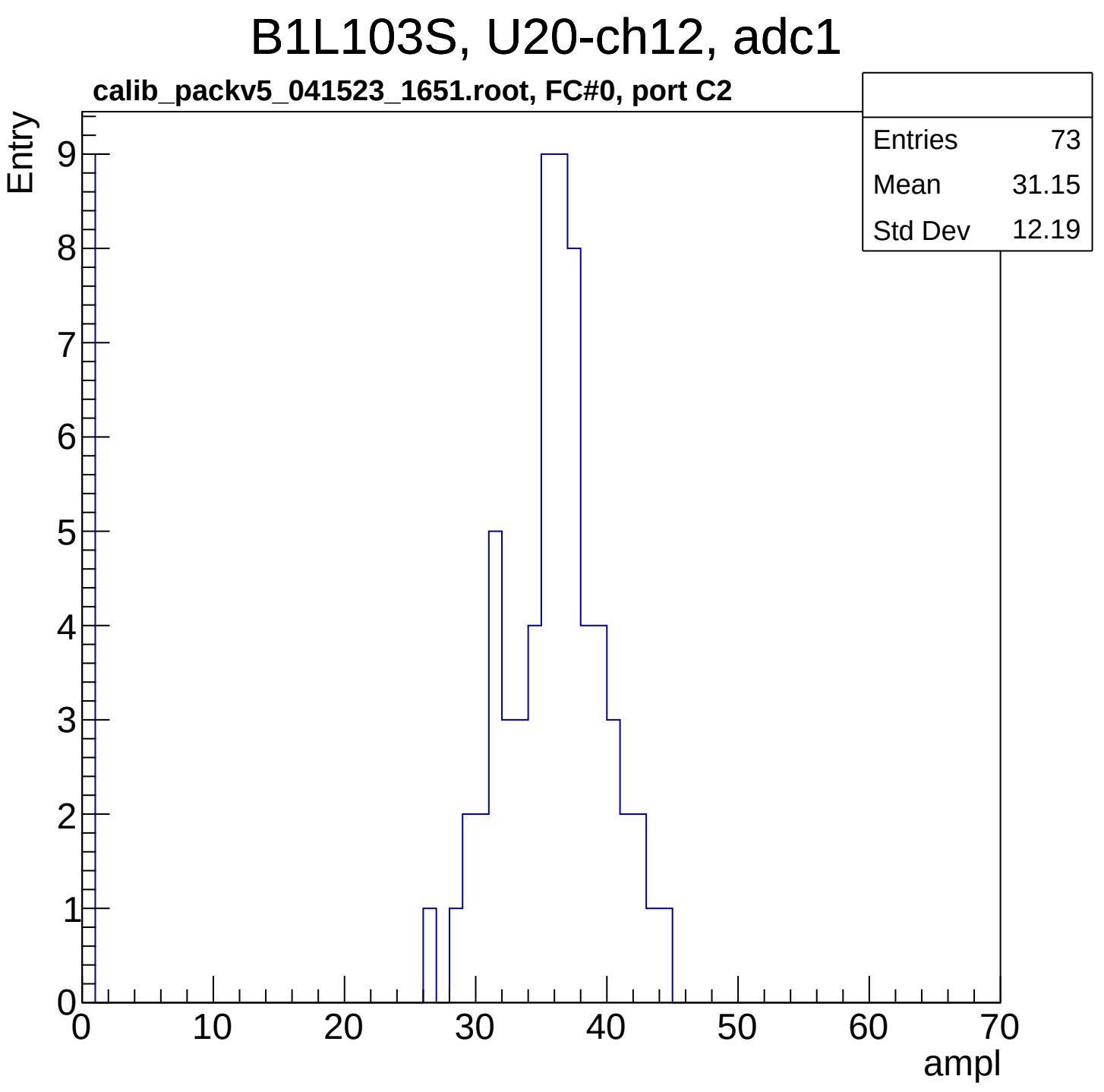
50
60
70
ampl


B1L103S, U20-ch12, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 31.15
Std Dev 12.19
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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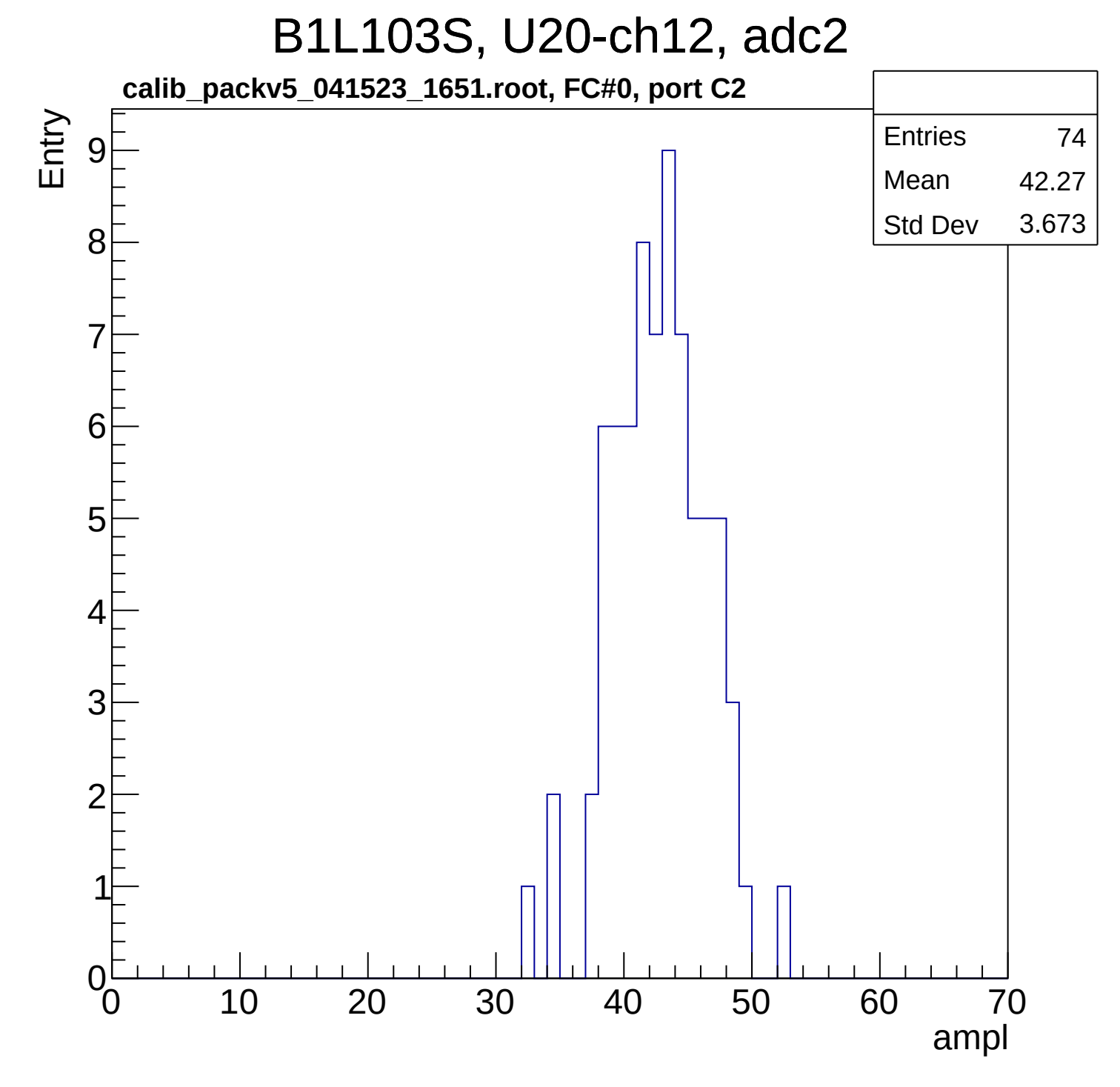
B1L103S, U20-ch12, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 42.27
Std Dev 3.673
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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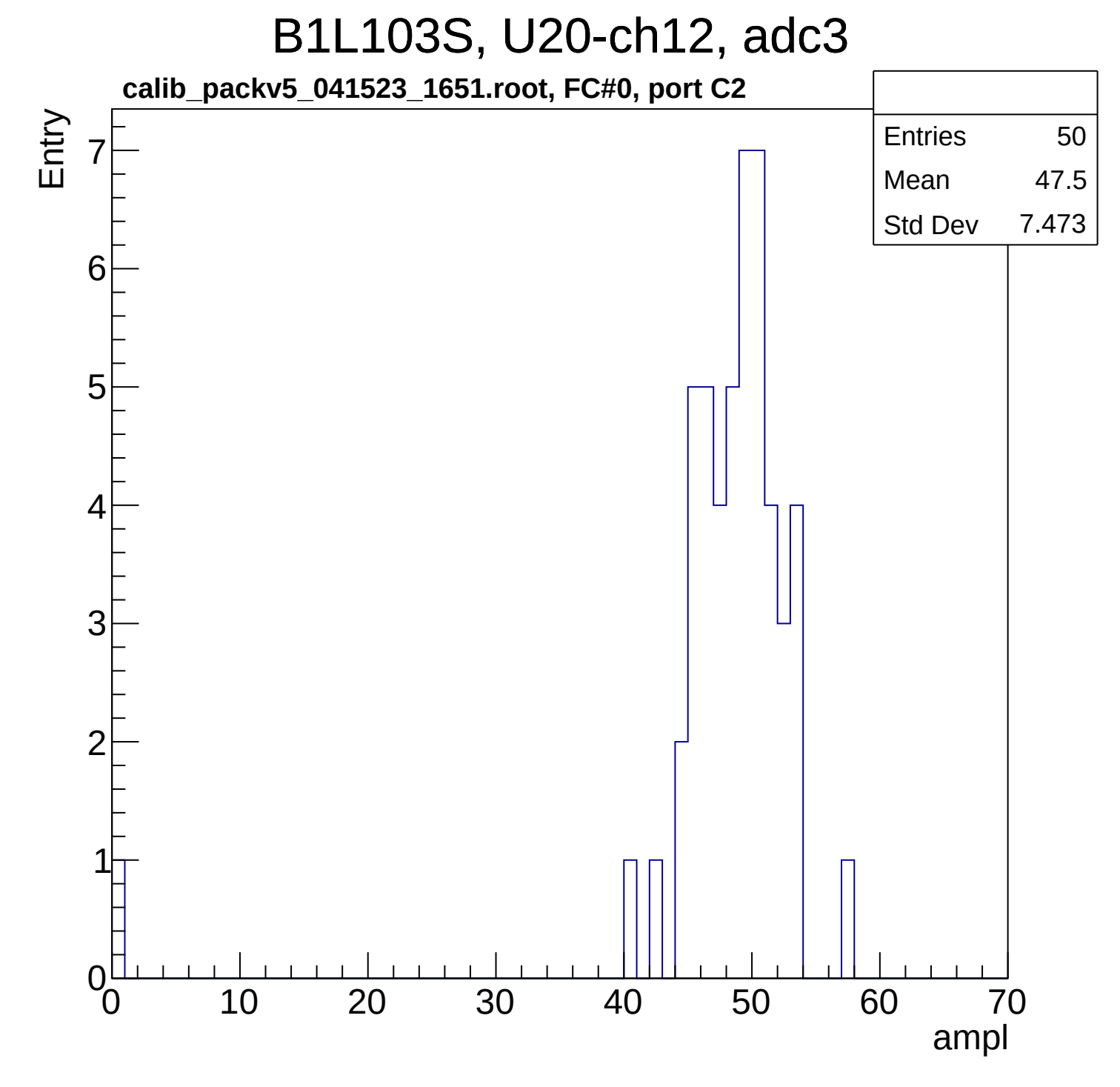
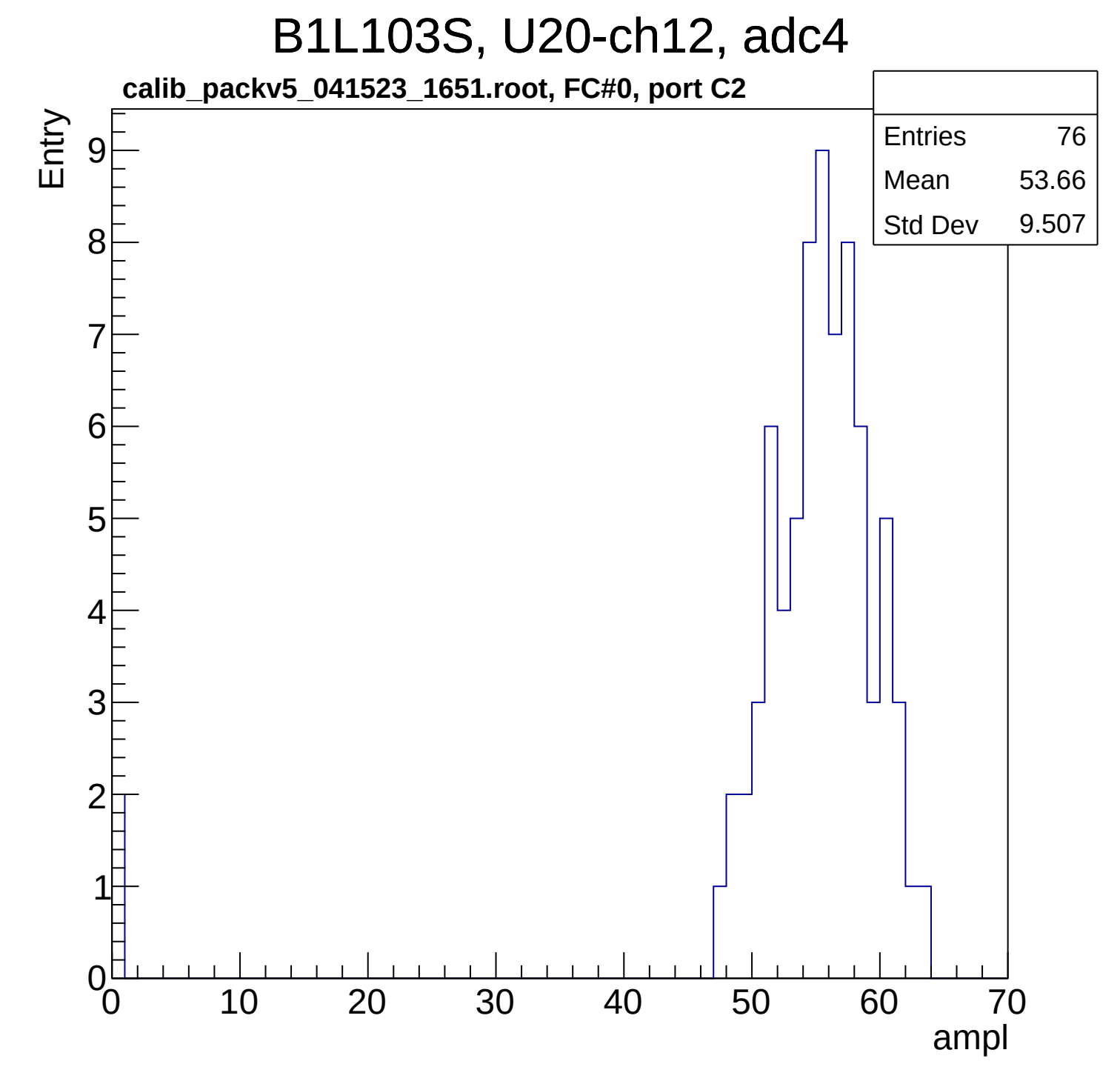
40
50
60
70


B1L103S, U20-ch12, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 47.5
Std Dev 7.473
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U20-ch12, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 53.66
Std Dev 9.507
Entry
ampl
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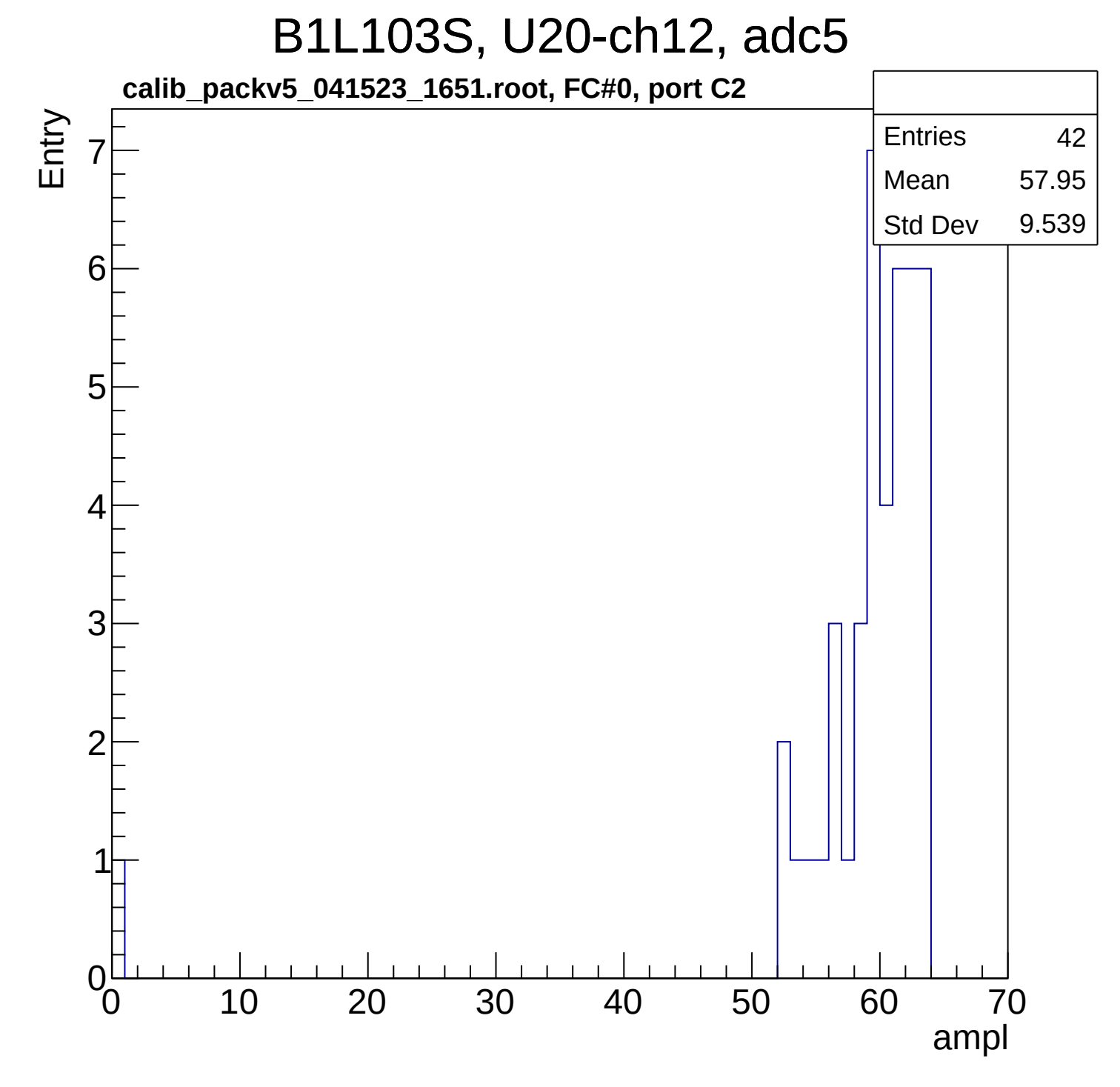
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch12, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 57.95
Std Dev 9.539
Entry
ampl
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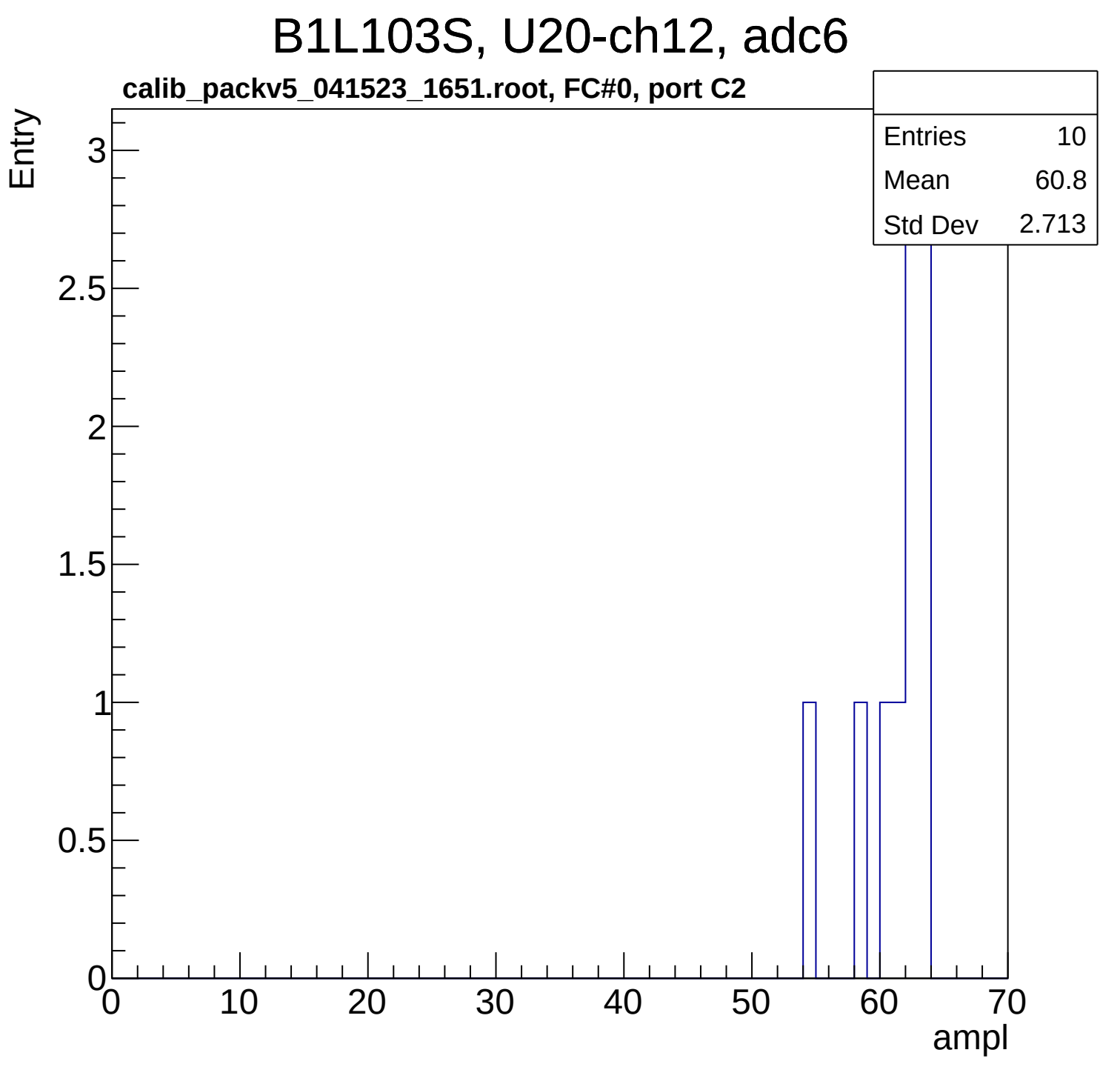
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U20-ch12, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 60.8
Std Dev 2.713
Entry
ampl
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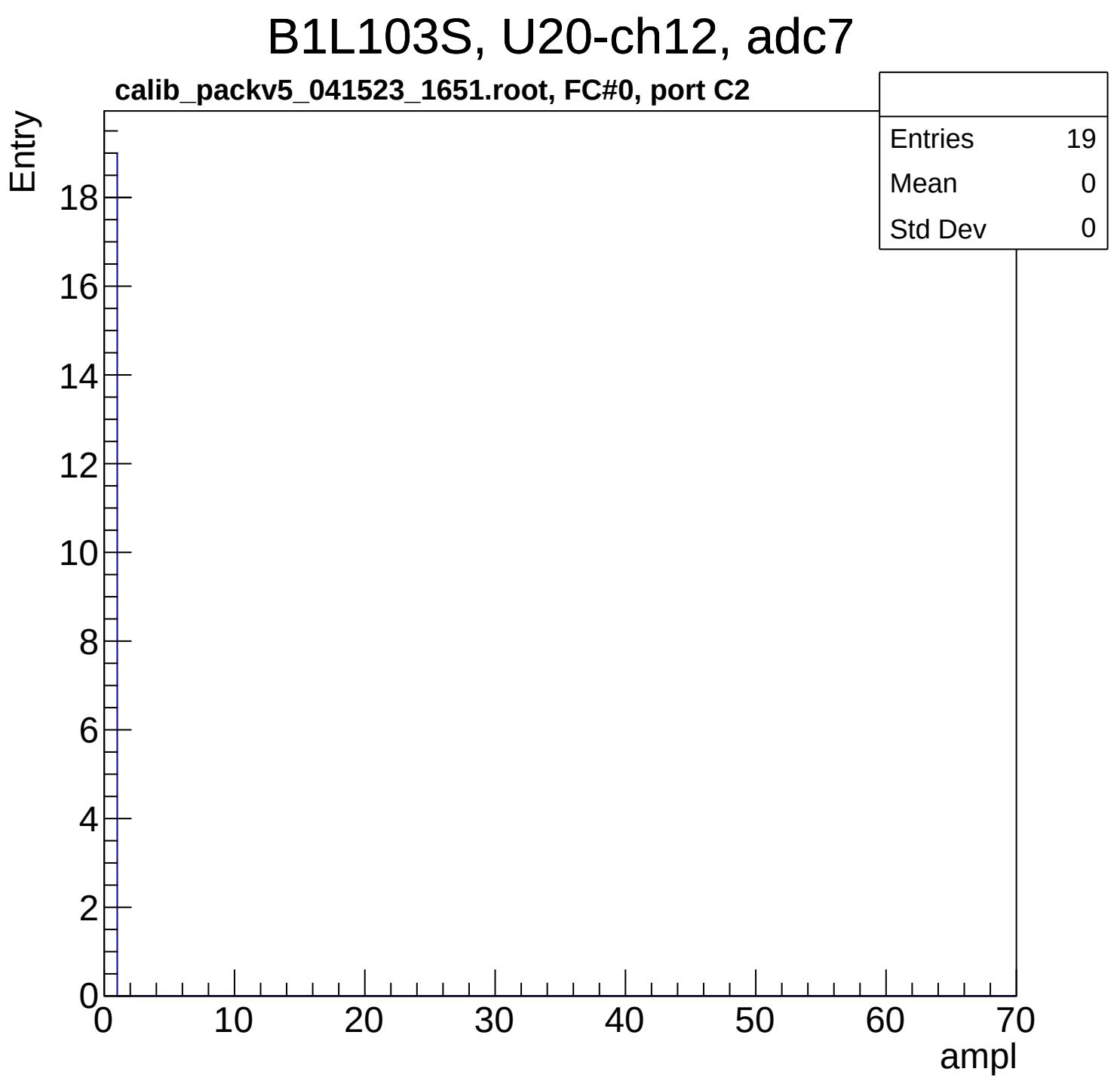
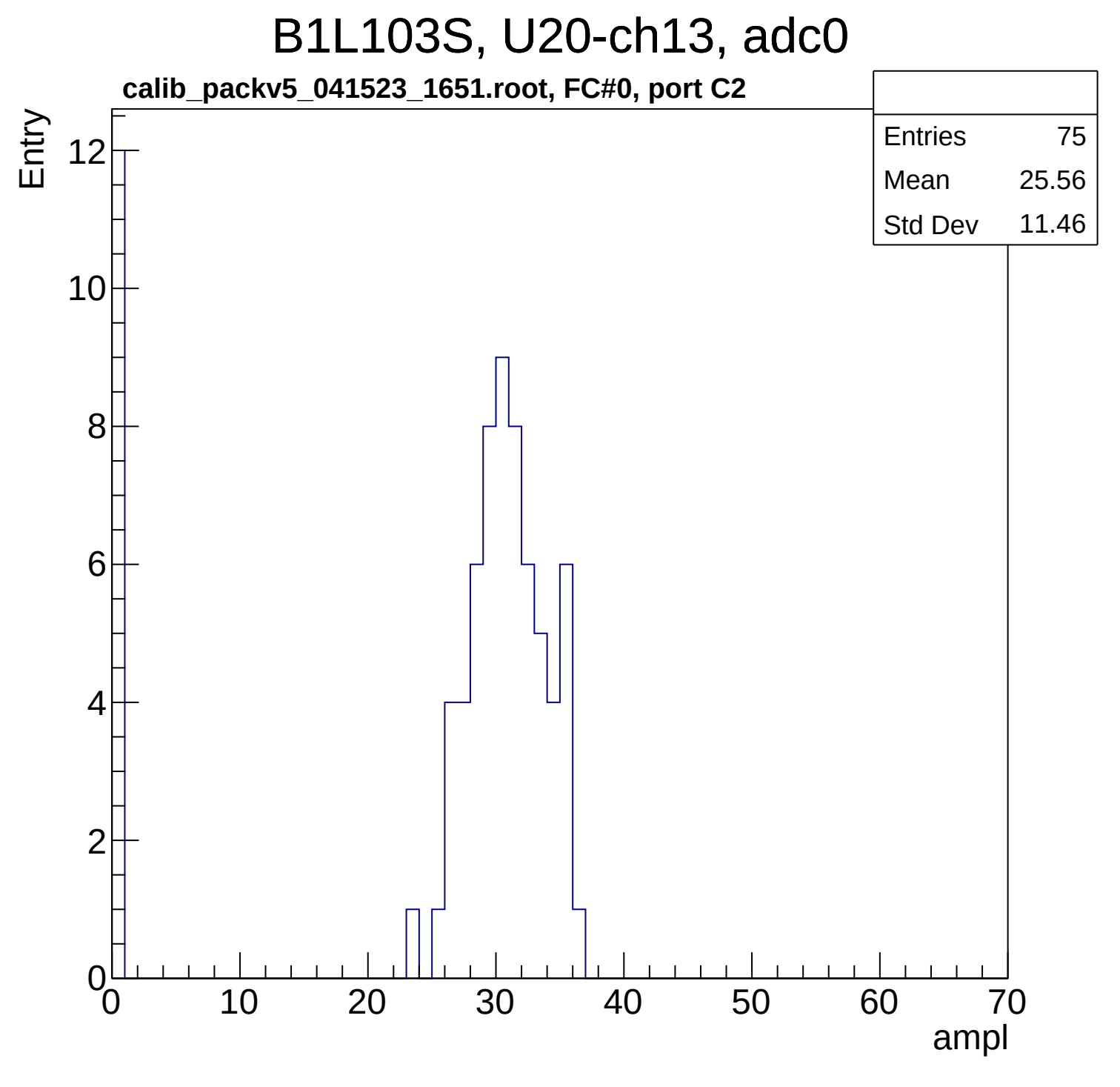
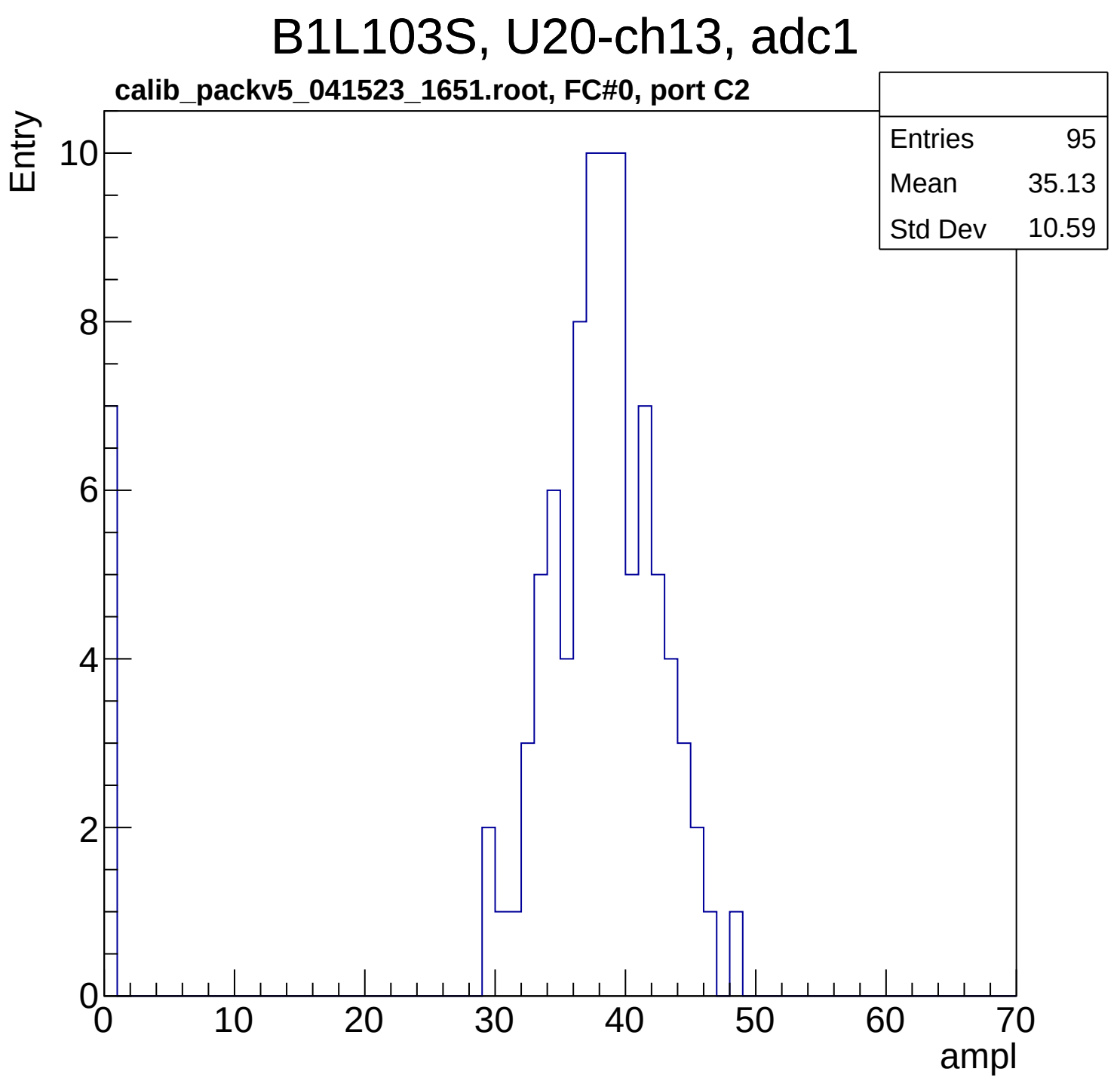
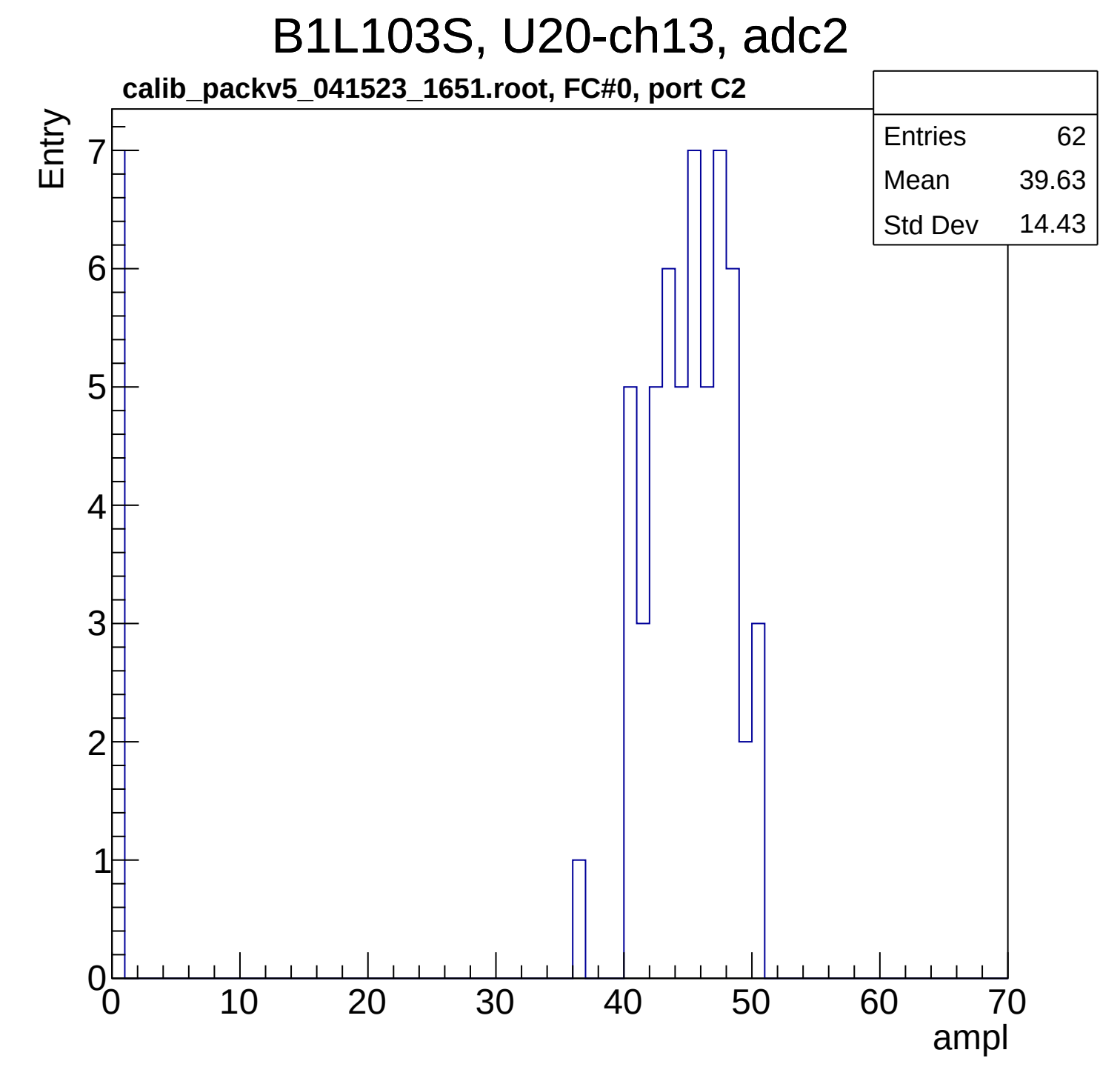
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U20-ch12, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch13, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 25.56
Std Dev 11.46
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch13, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 35.13
Std Dev 10.59
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch13, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 39.63
Std Dev 14.43
Entry
ampl
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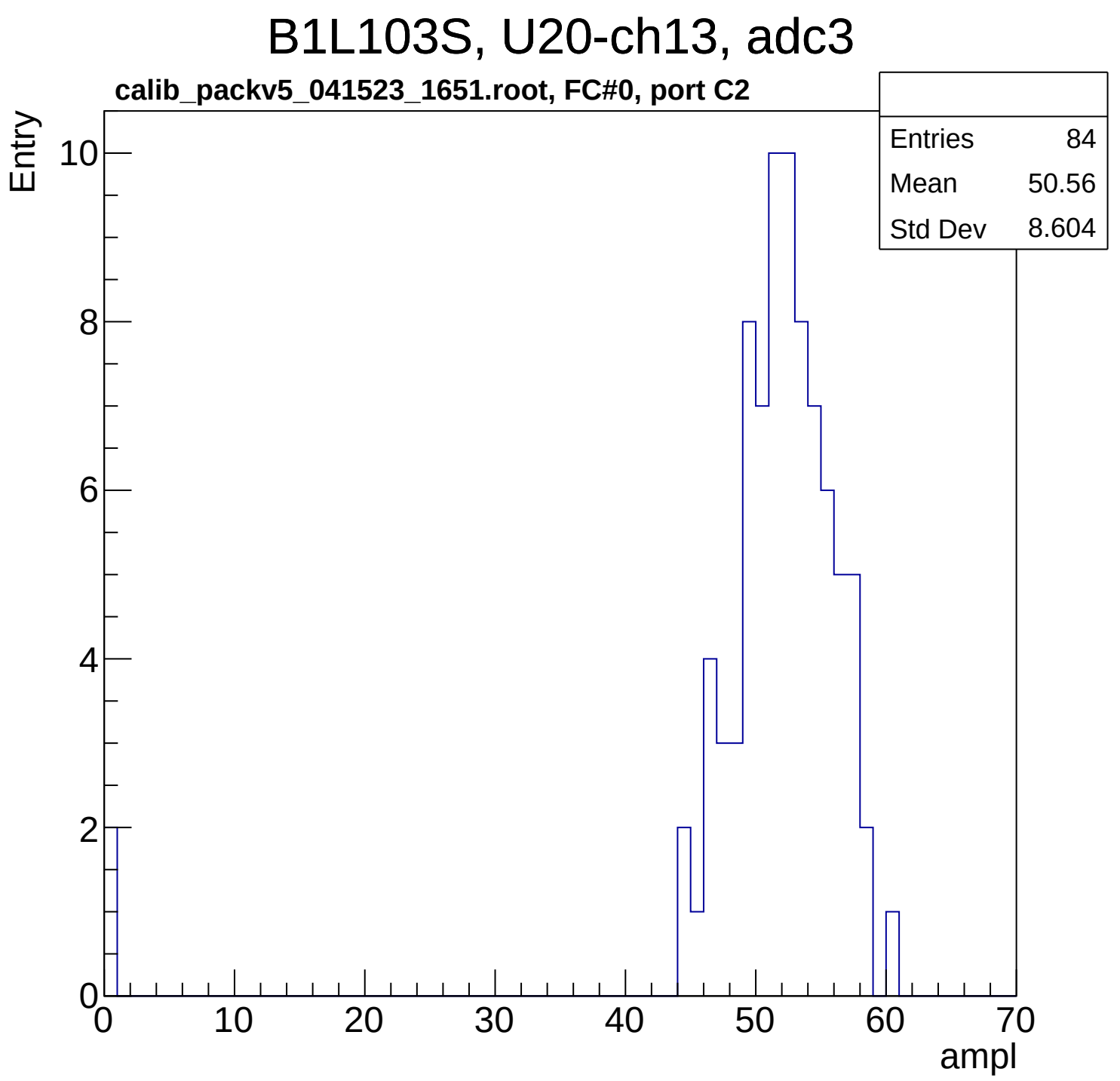
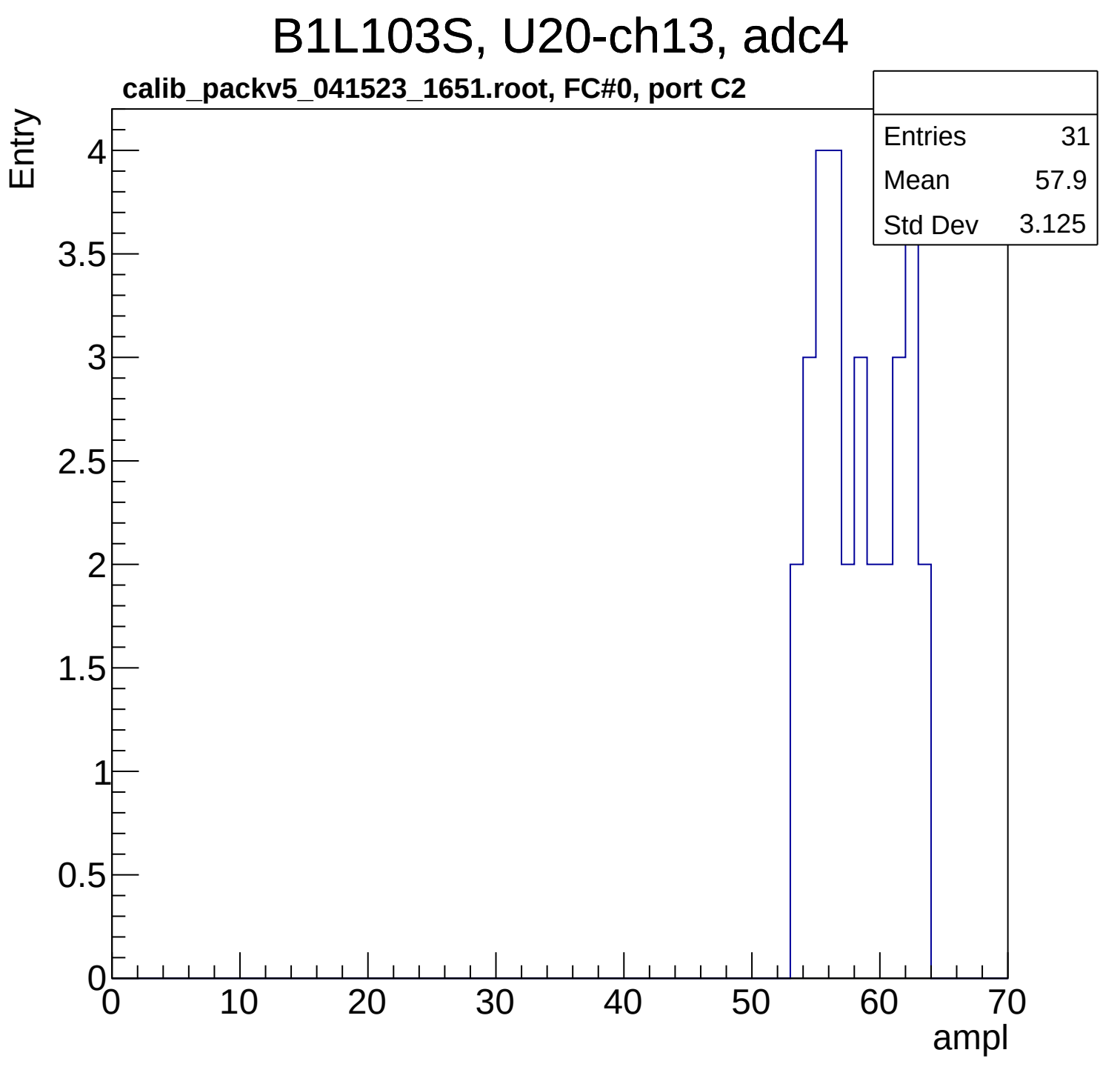
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U20-ch13, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 50.56
Std Dev 8.604
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U20-ch13, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 57.9
Std Dev 3.125
Entry
ampl
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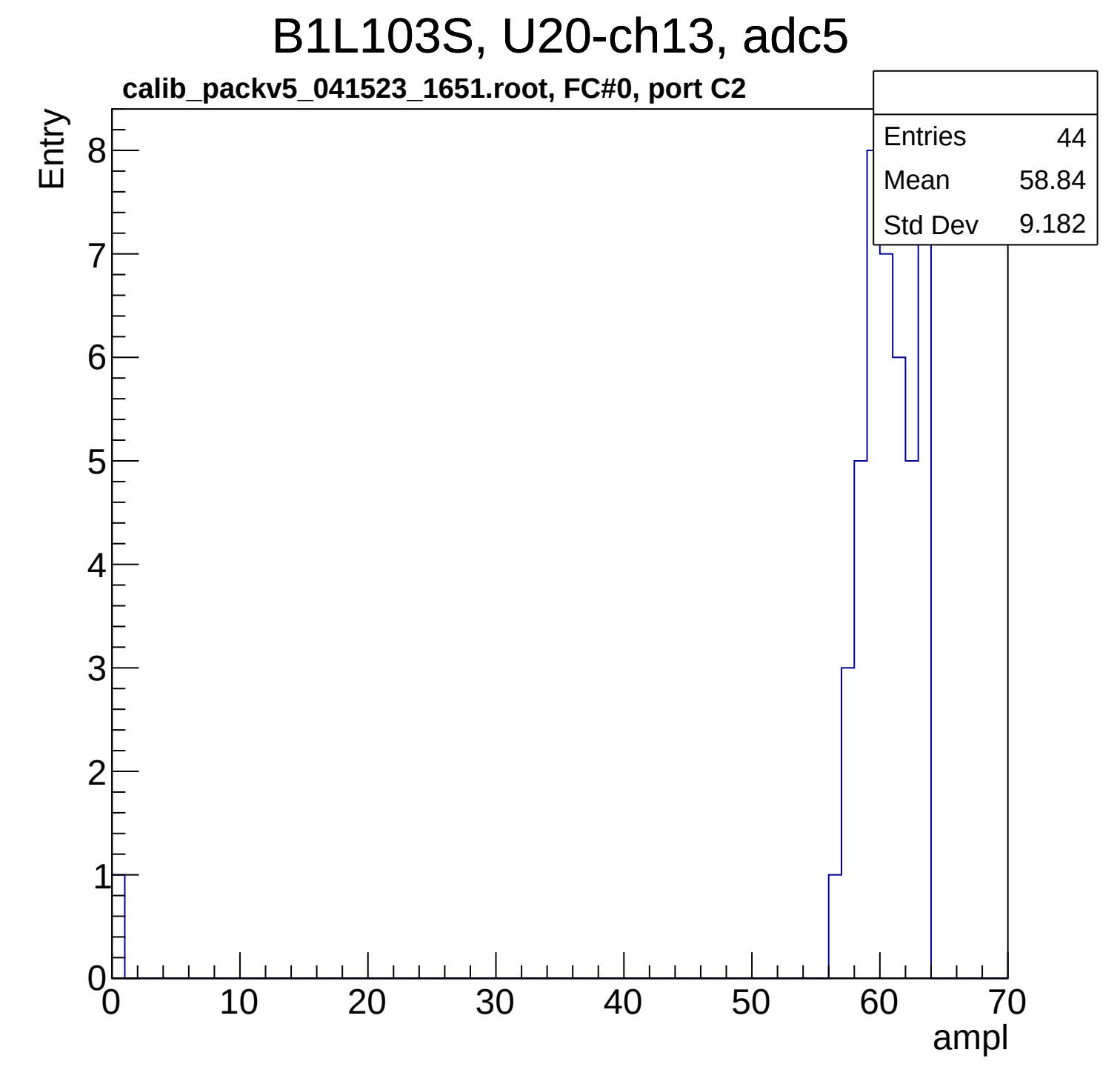
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U20-ch13, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 58.84
Std Dev 9.182
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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60
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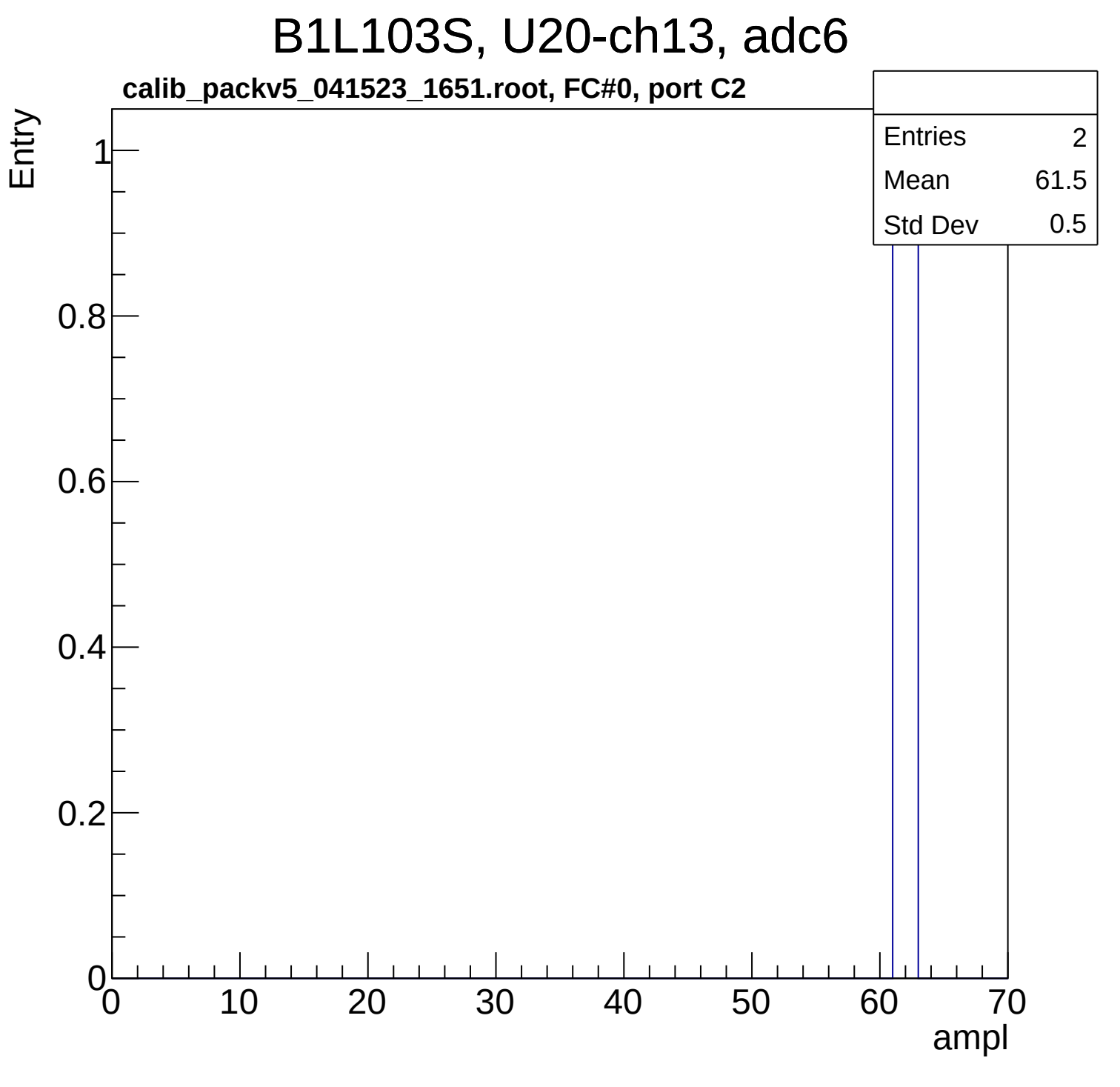
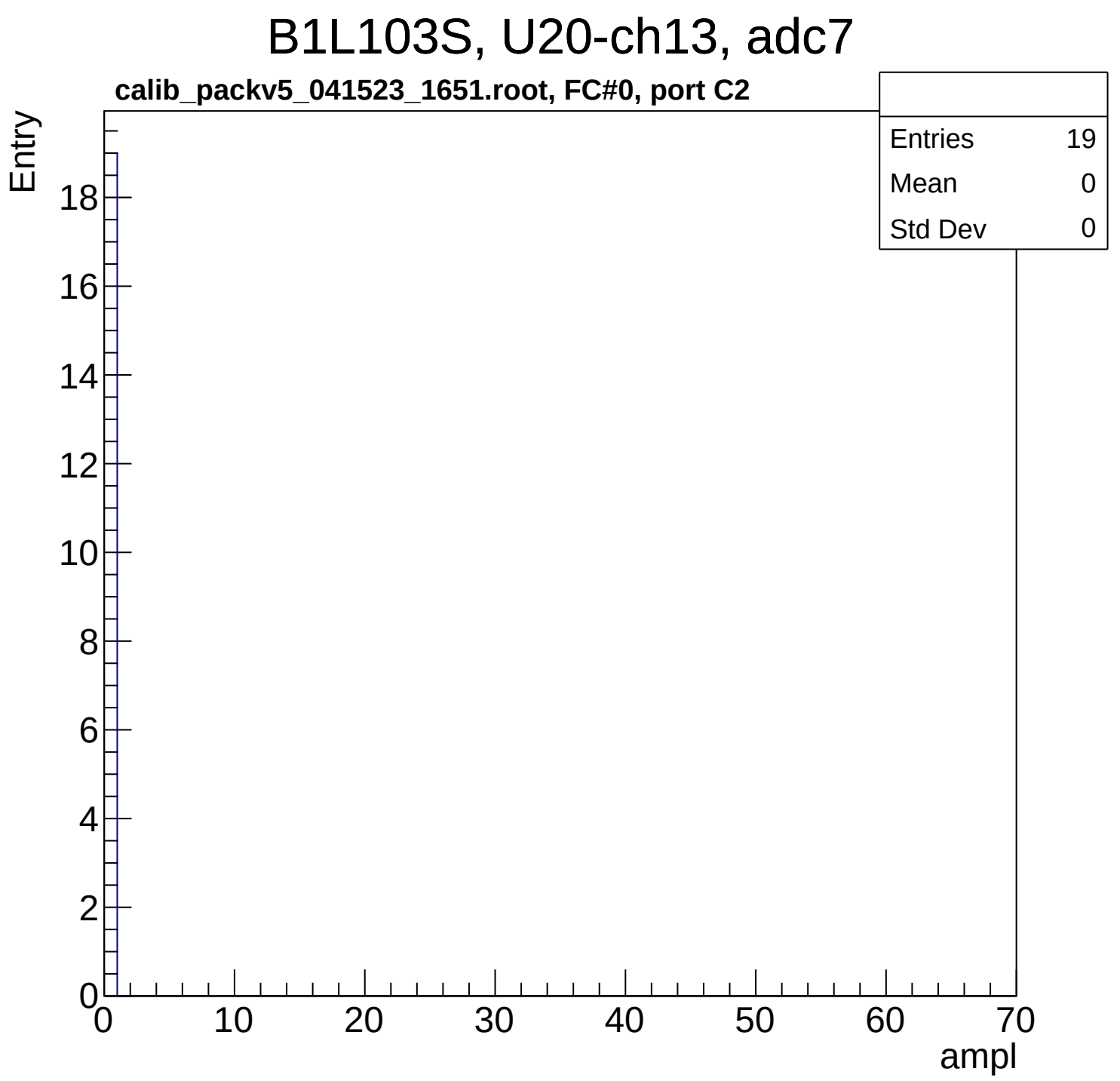
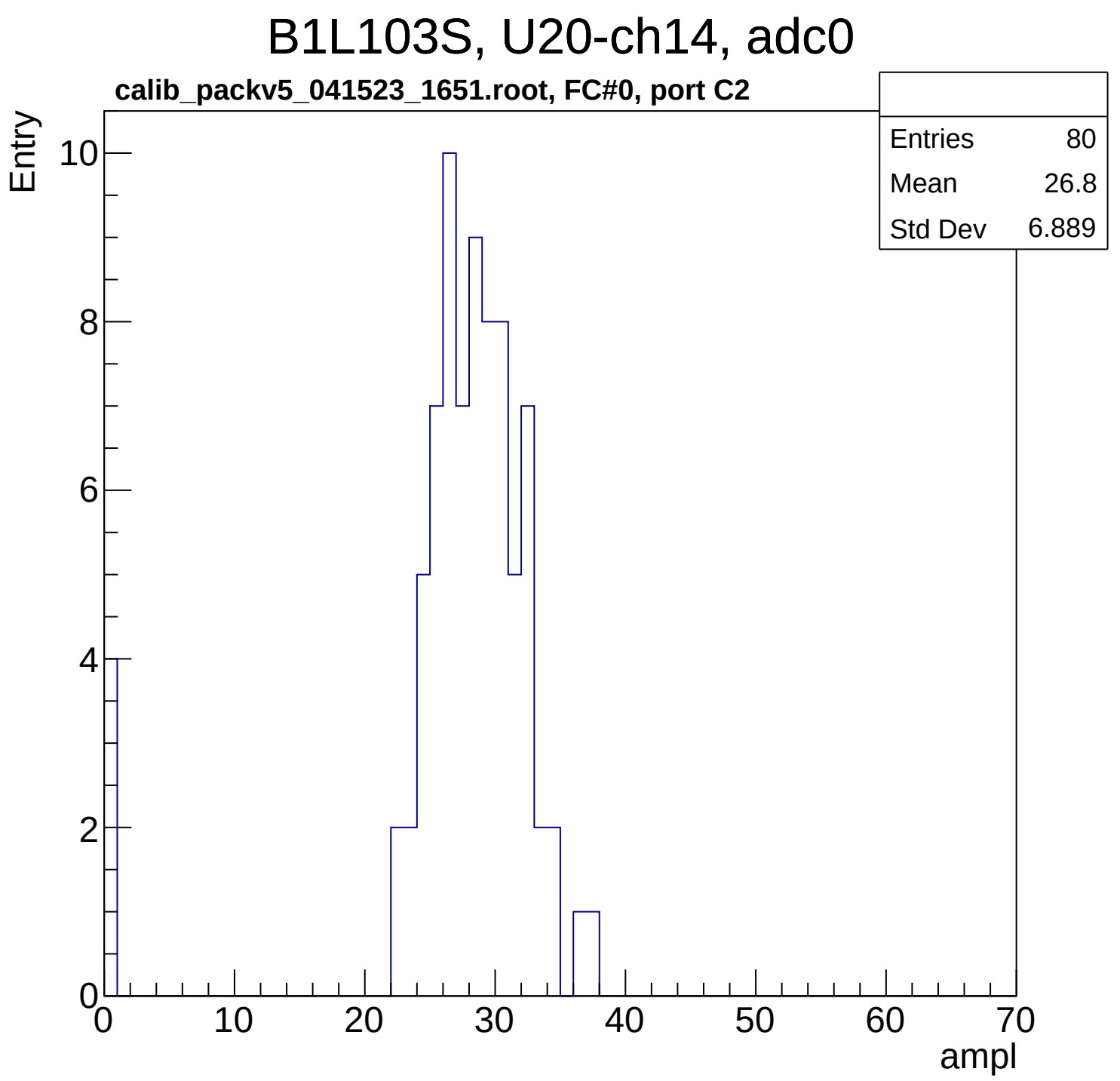
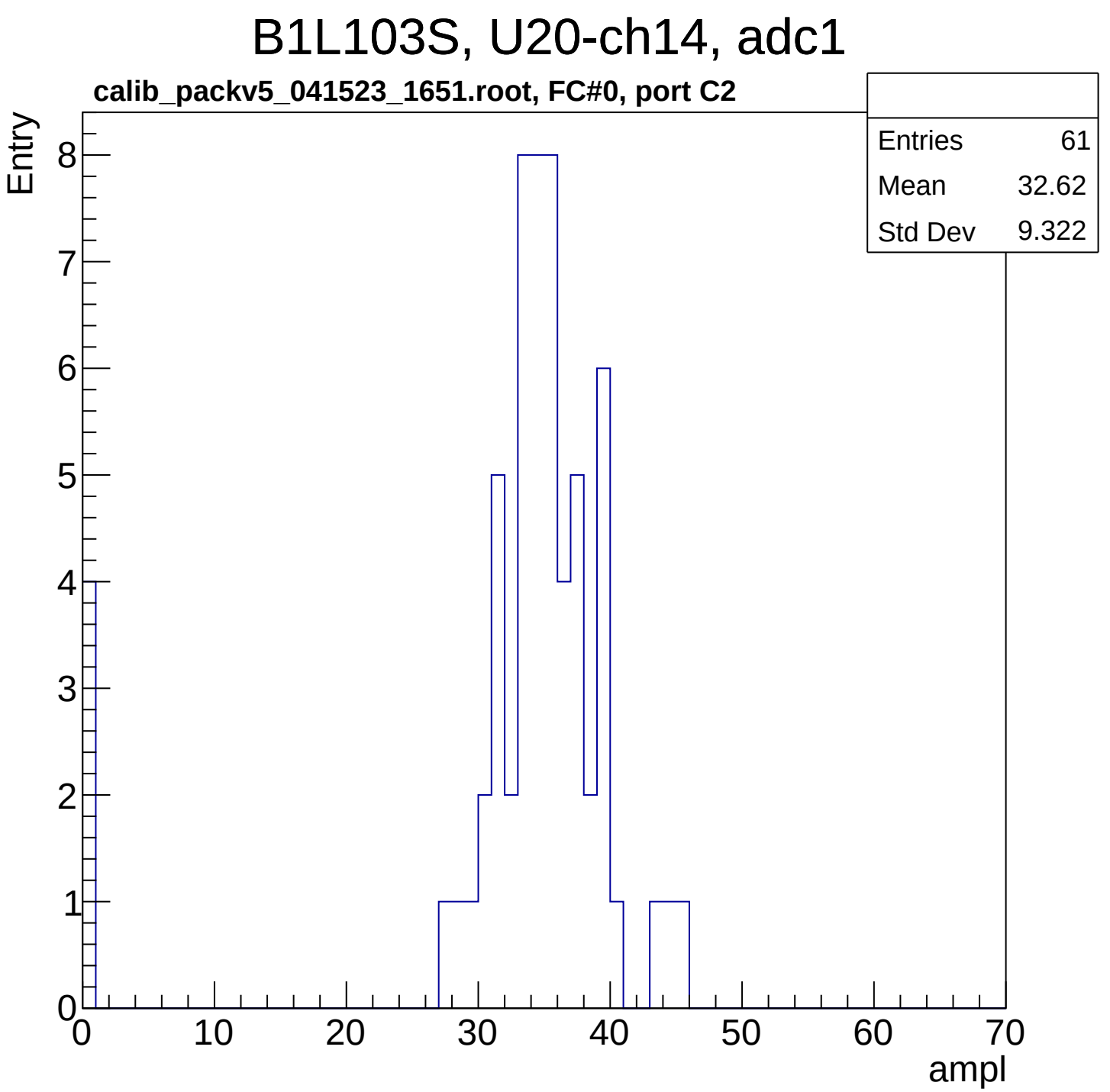

B1L103S, U20-ch13, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 61.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch13, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch14, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 26.8
Std Dev 6.889
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U20-ch14, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 32.62
Std Dev 9.322
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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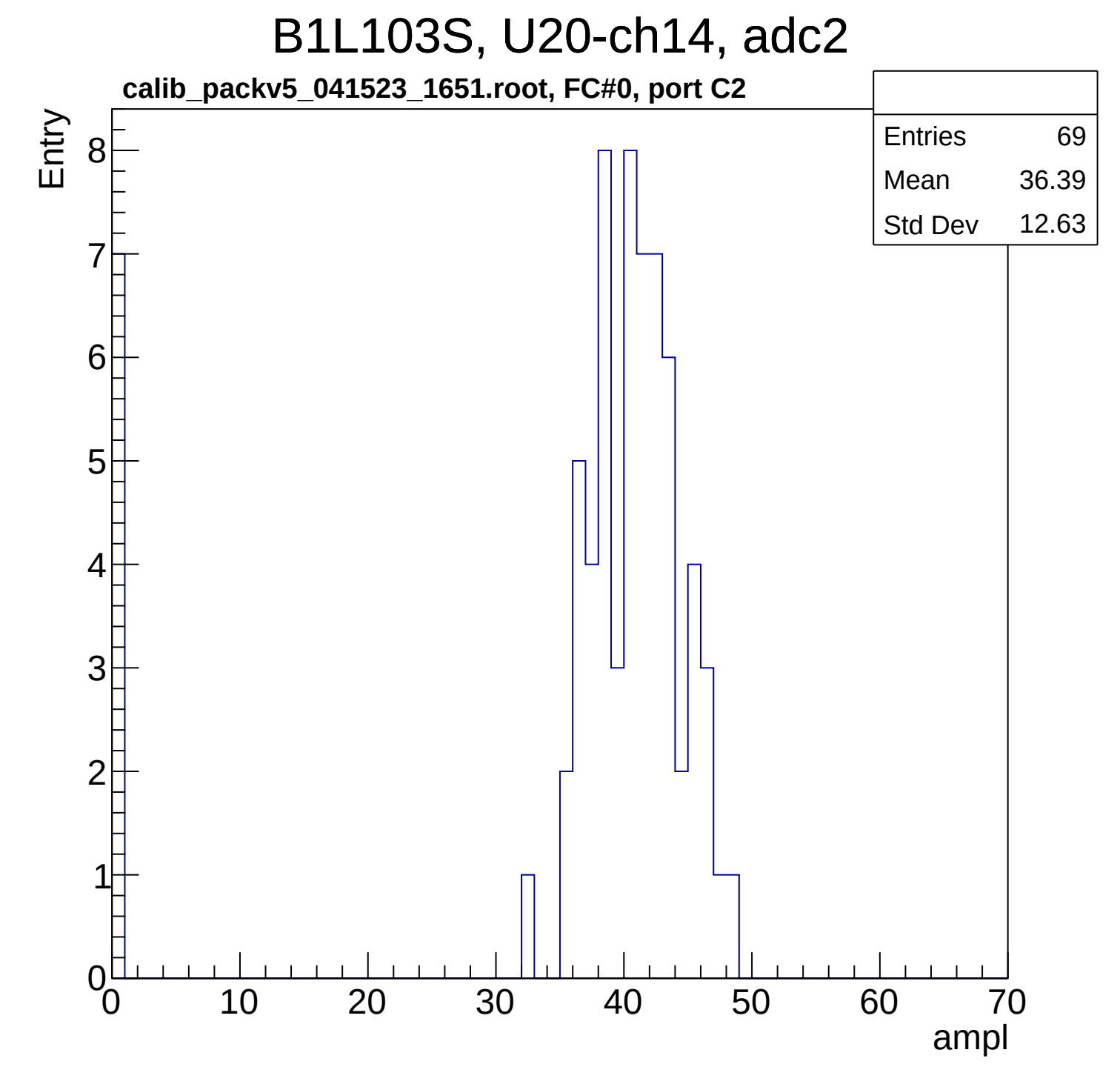
B1L103S, U20-ch14, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 36.39
Std Dev 12.63
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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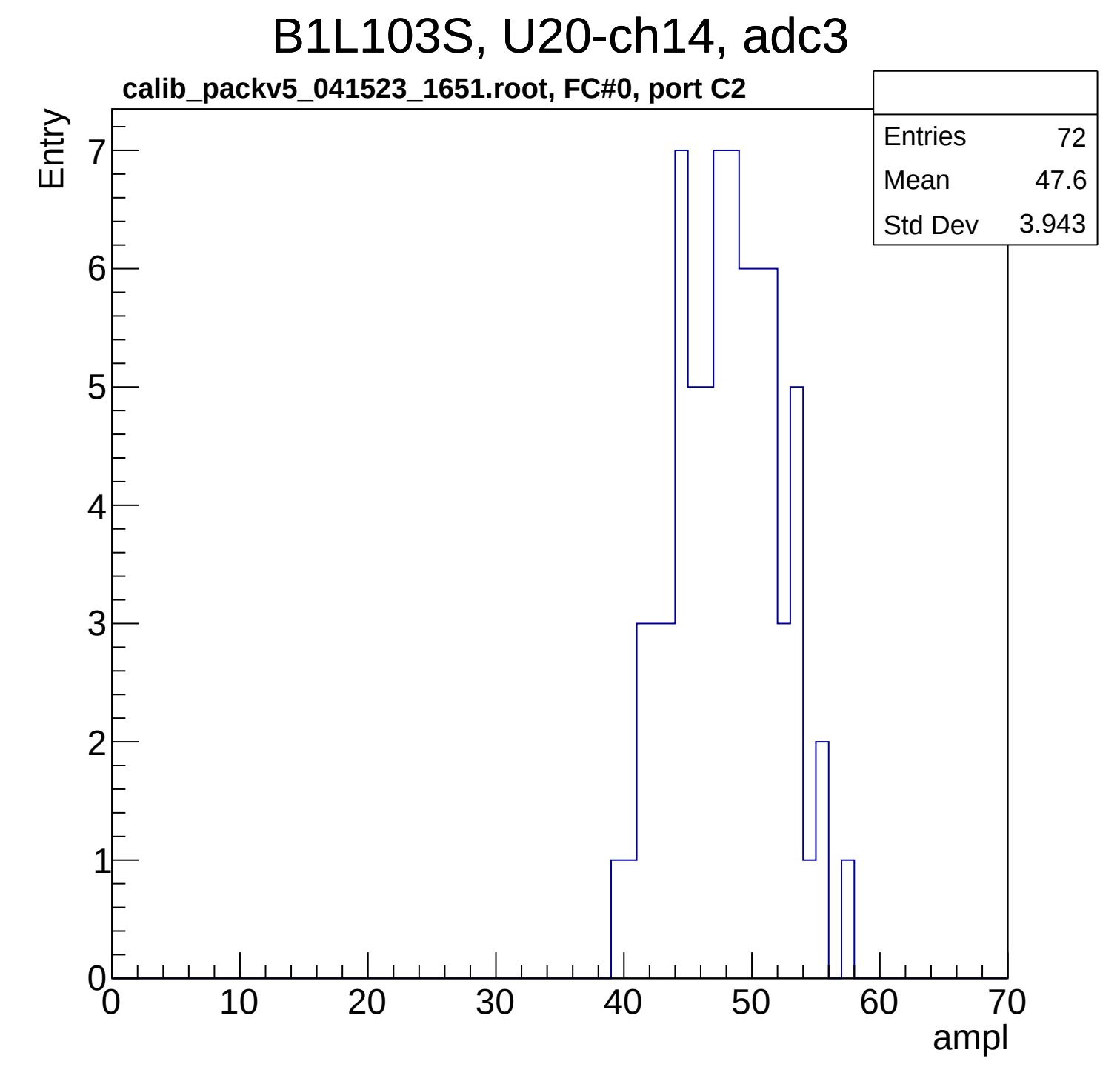
B1L103S, U20-ch14, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 47.6
Std Dev 3.943
Entry
ampl
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1
2
3
4
5
6
7
0
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20
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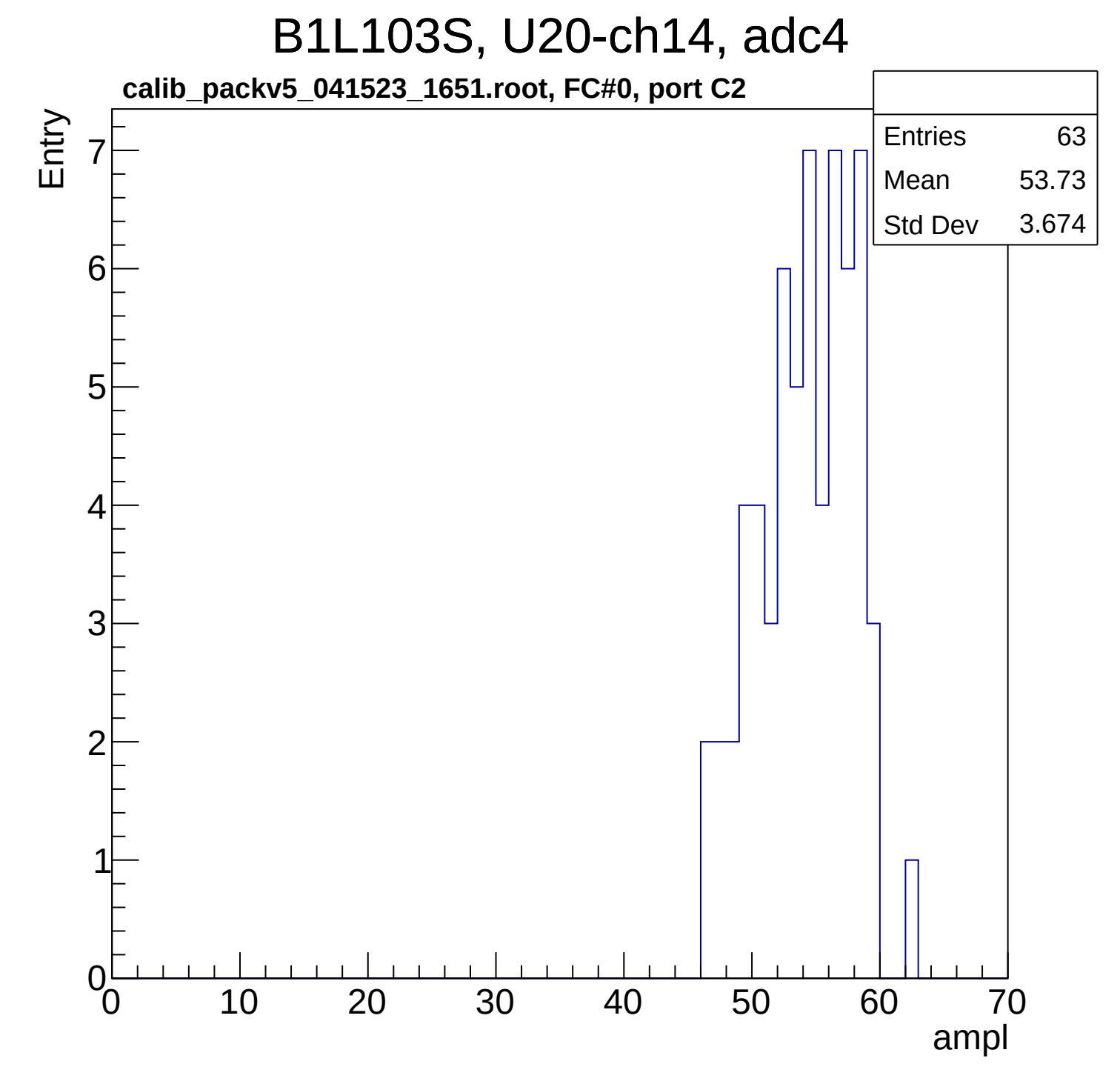
B1L103S, U20-ch14, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 53.73
Std Dev 3.674
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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60
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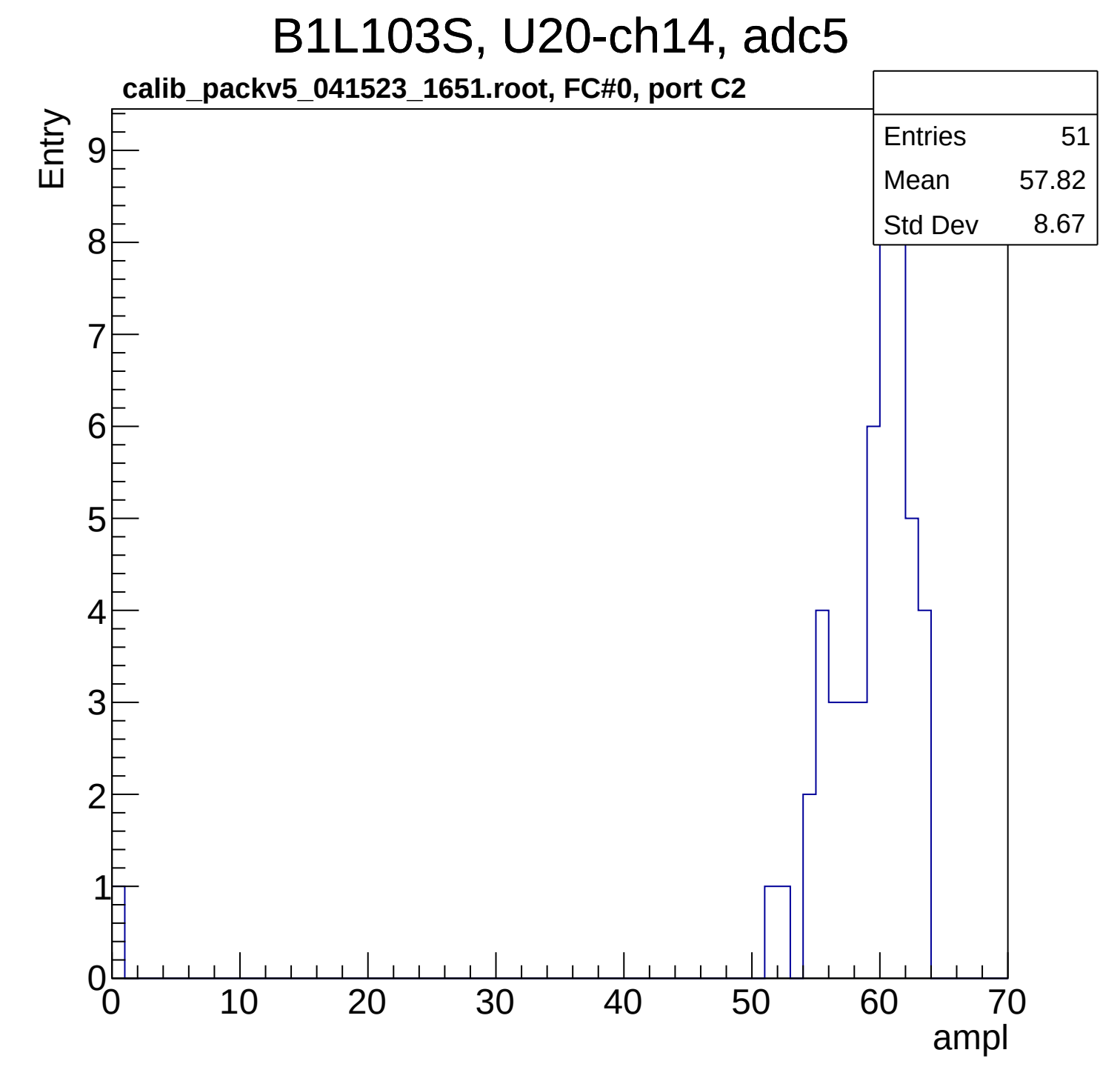
B1L103S, U20-ch14, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 57.82
Std Dev 8.67
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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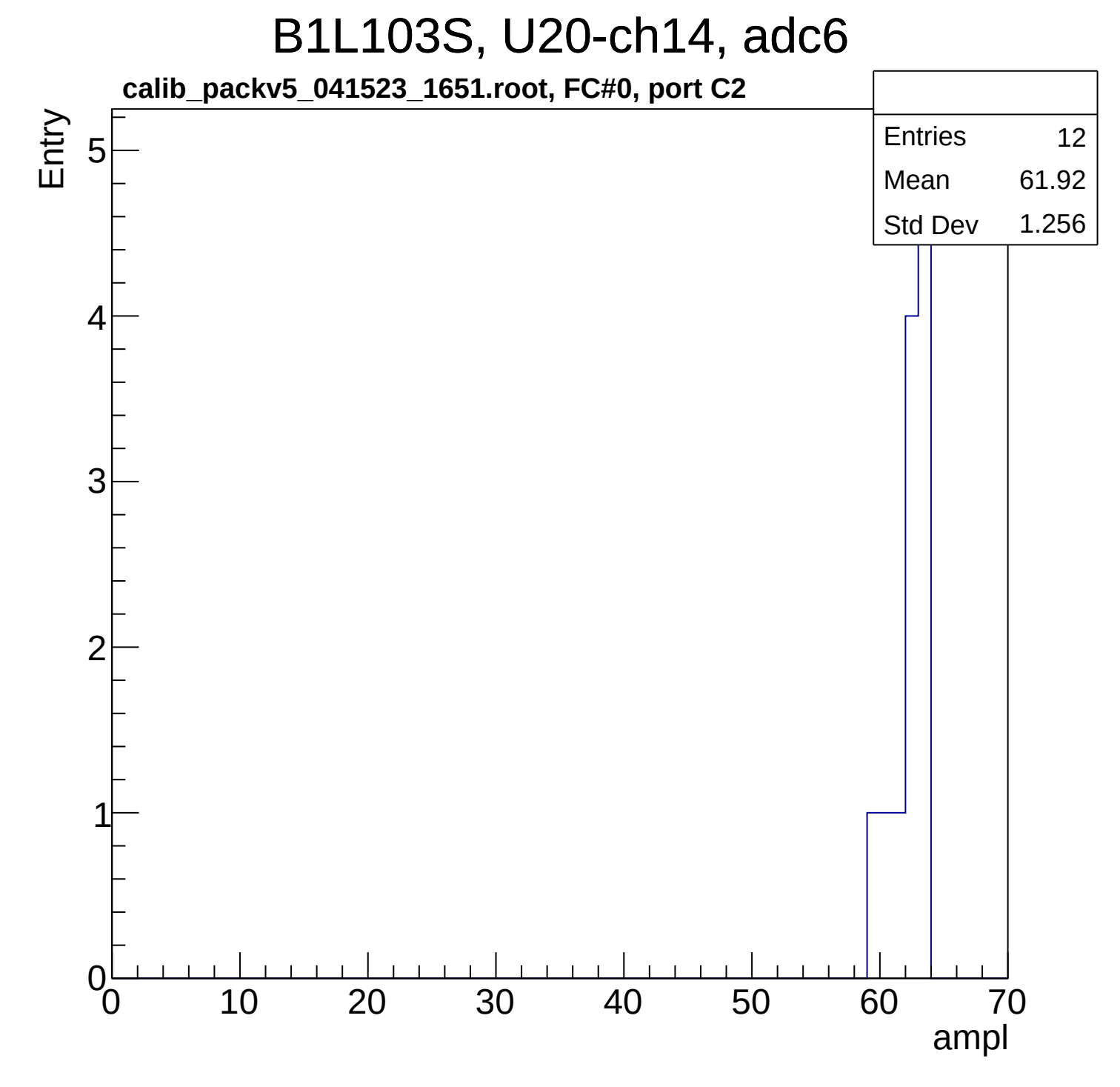
B1L103S, U20-ch14, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.92
Std Dev 1.256
Entry
ampl
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1
2
3
4
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0
10
20
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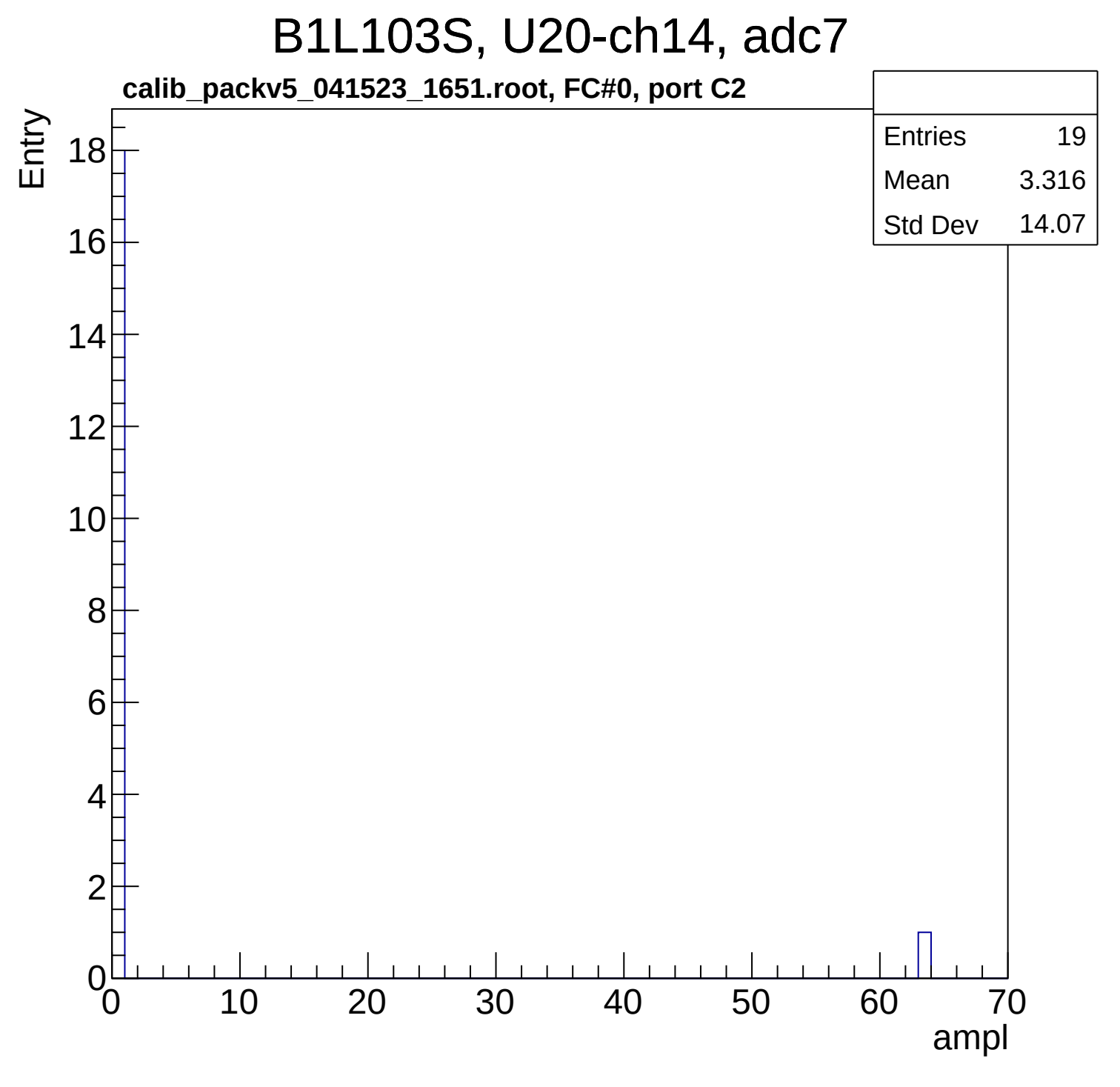
40
50
60
70


B1L103S, U20-ch14, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.316
Std Dev 14.07
Entry
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6
8
10
12
14
16
18
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10
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50
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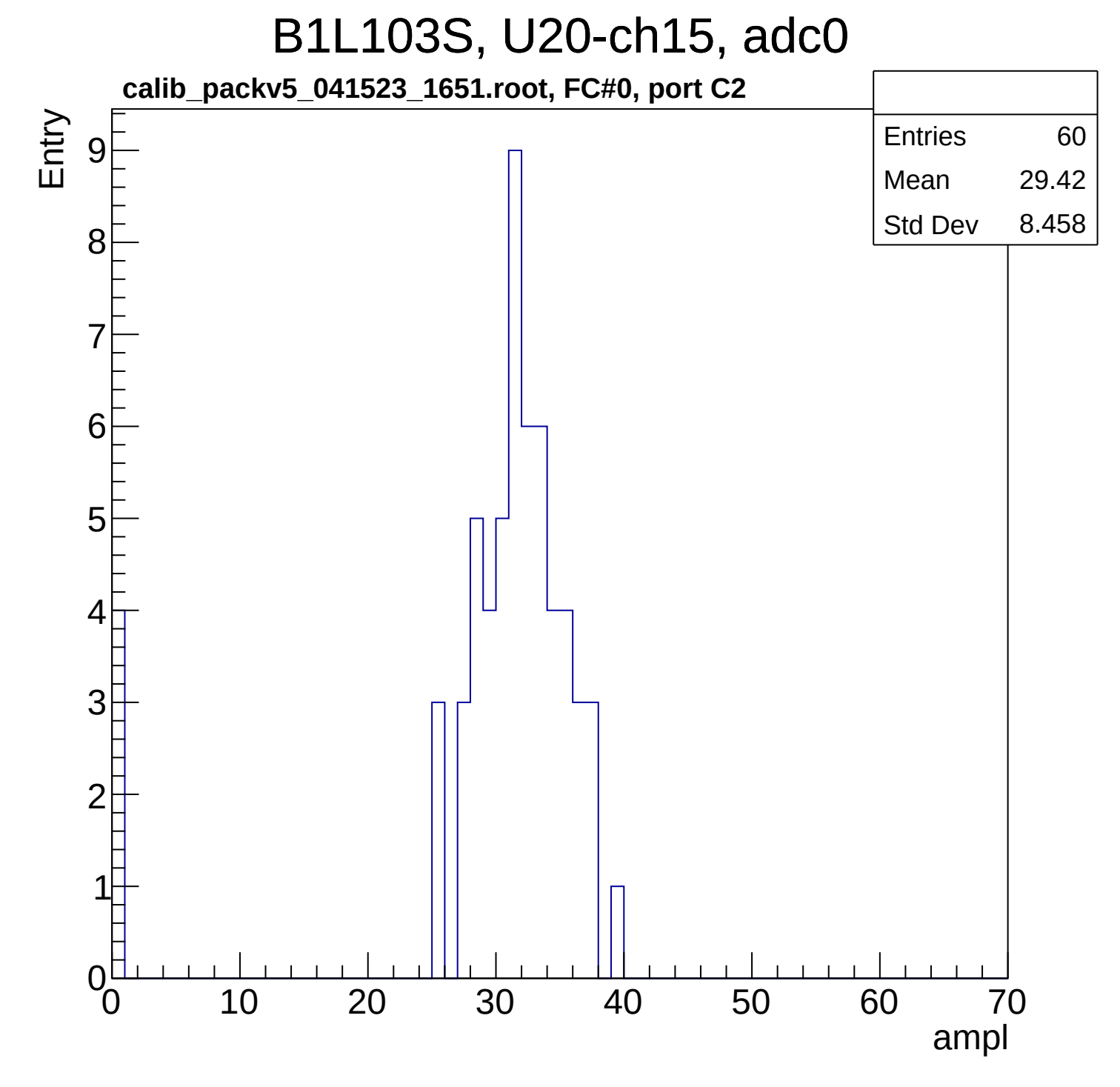
70
ampl


B1L103S, U20-ch15, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 29.42
Std Dev 8.458
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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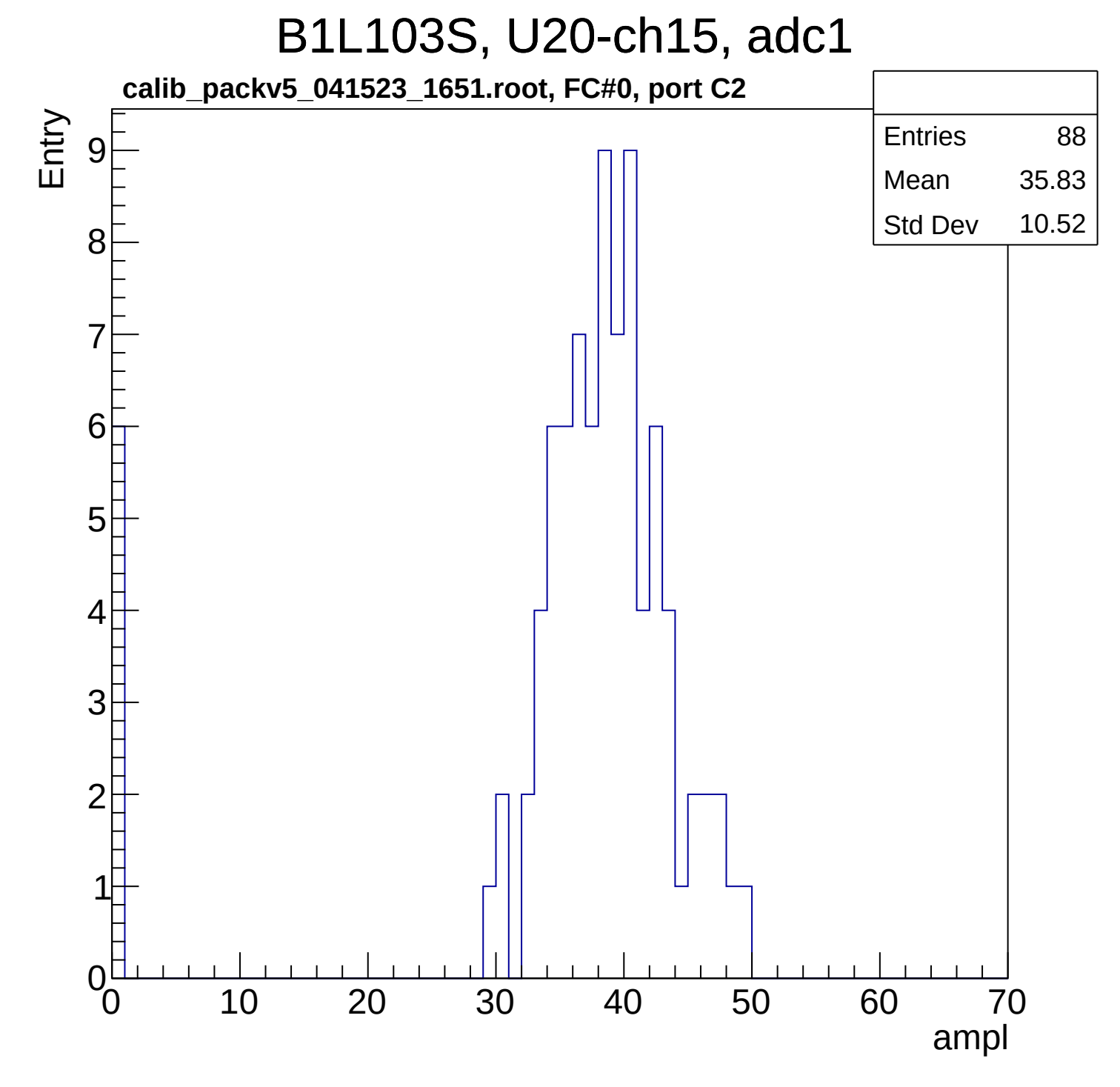
60
70


B1L103S, U20-ch15, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 35.83
Std Dev 10.52
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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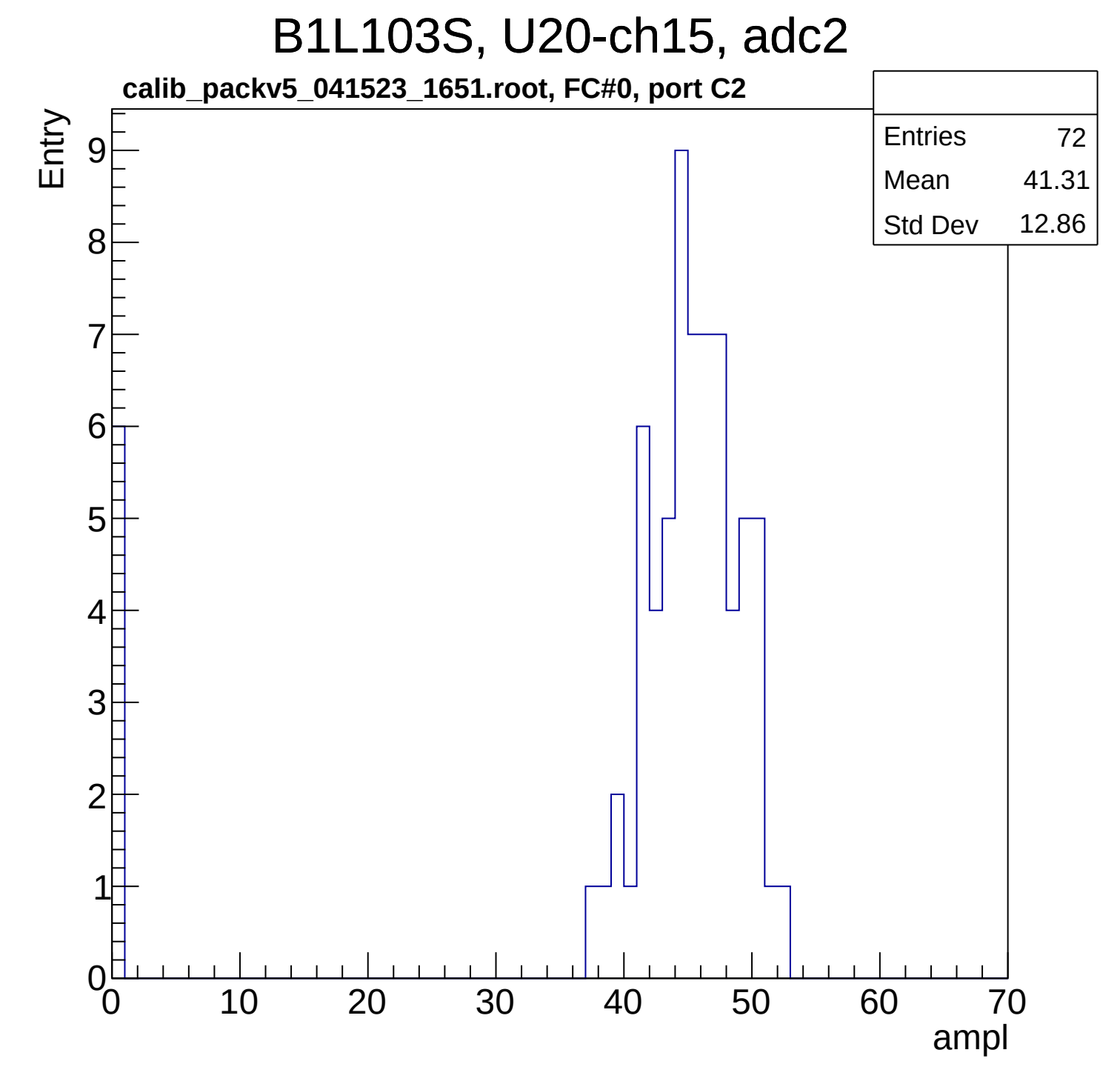
B1L103S, U20-ch15, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 41.31
Std Dev 12.86
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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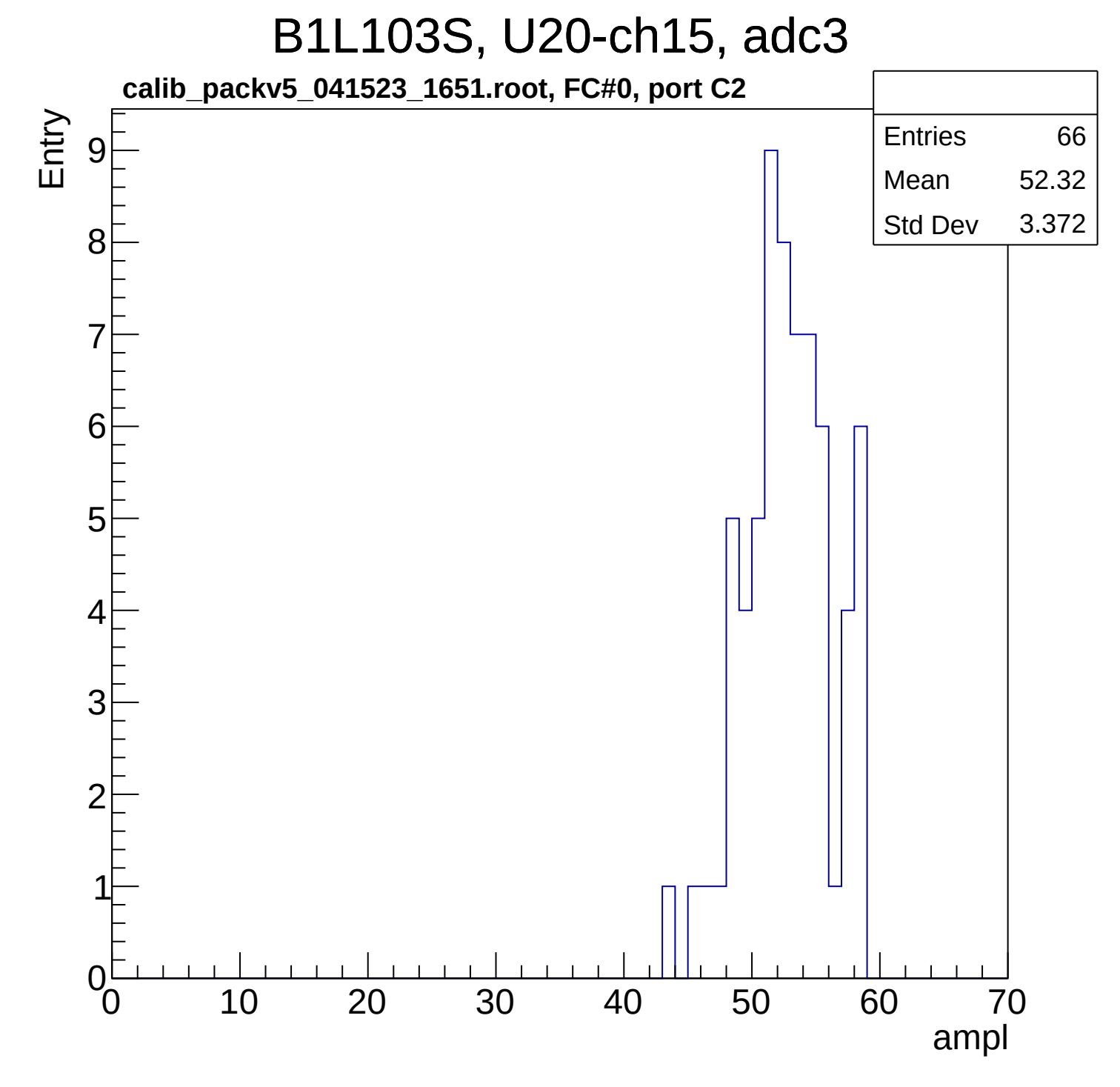
B1L103S, U20-ch15, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 52.32
Std Dev 3.372
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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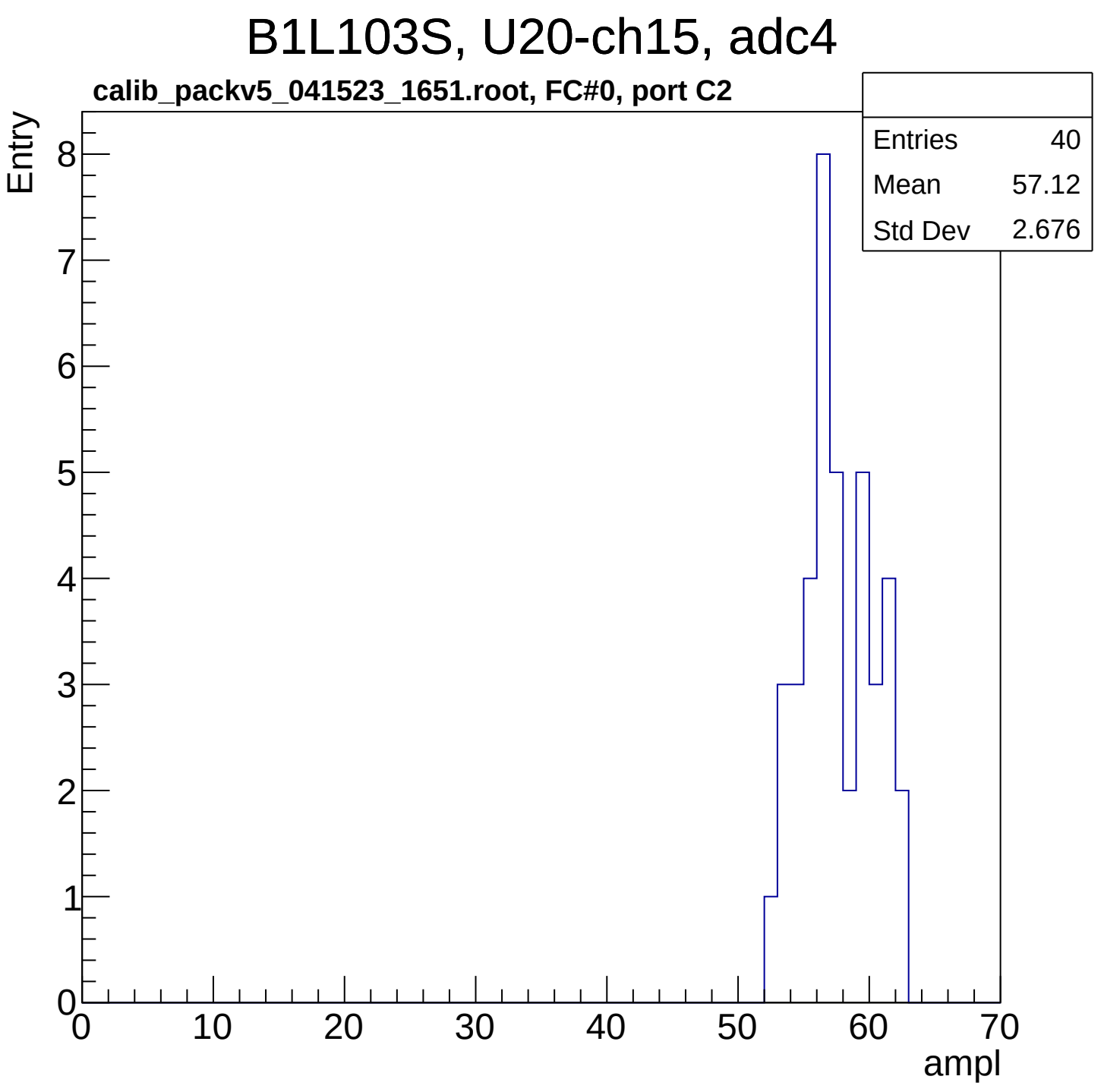
40
50
60
70


B1L103S, U20-ch15, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 57.12
Std Dev 2.676
Entry
ampl
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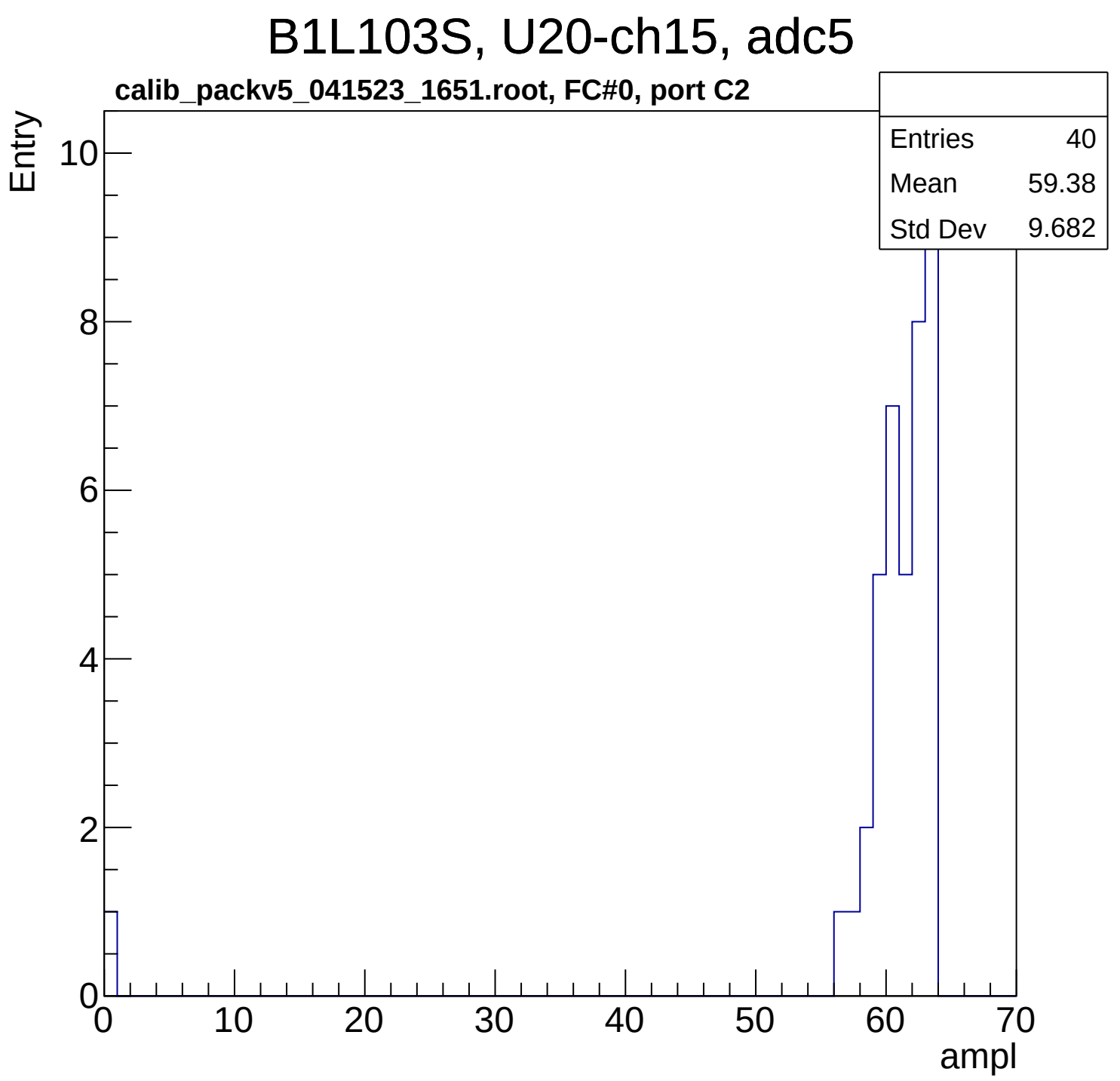
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch15, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 59.38
Std Dev 9.682
Entry
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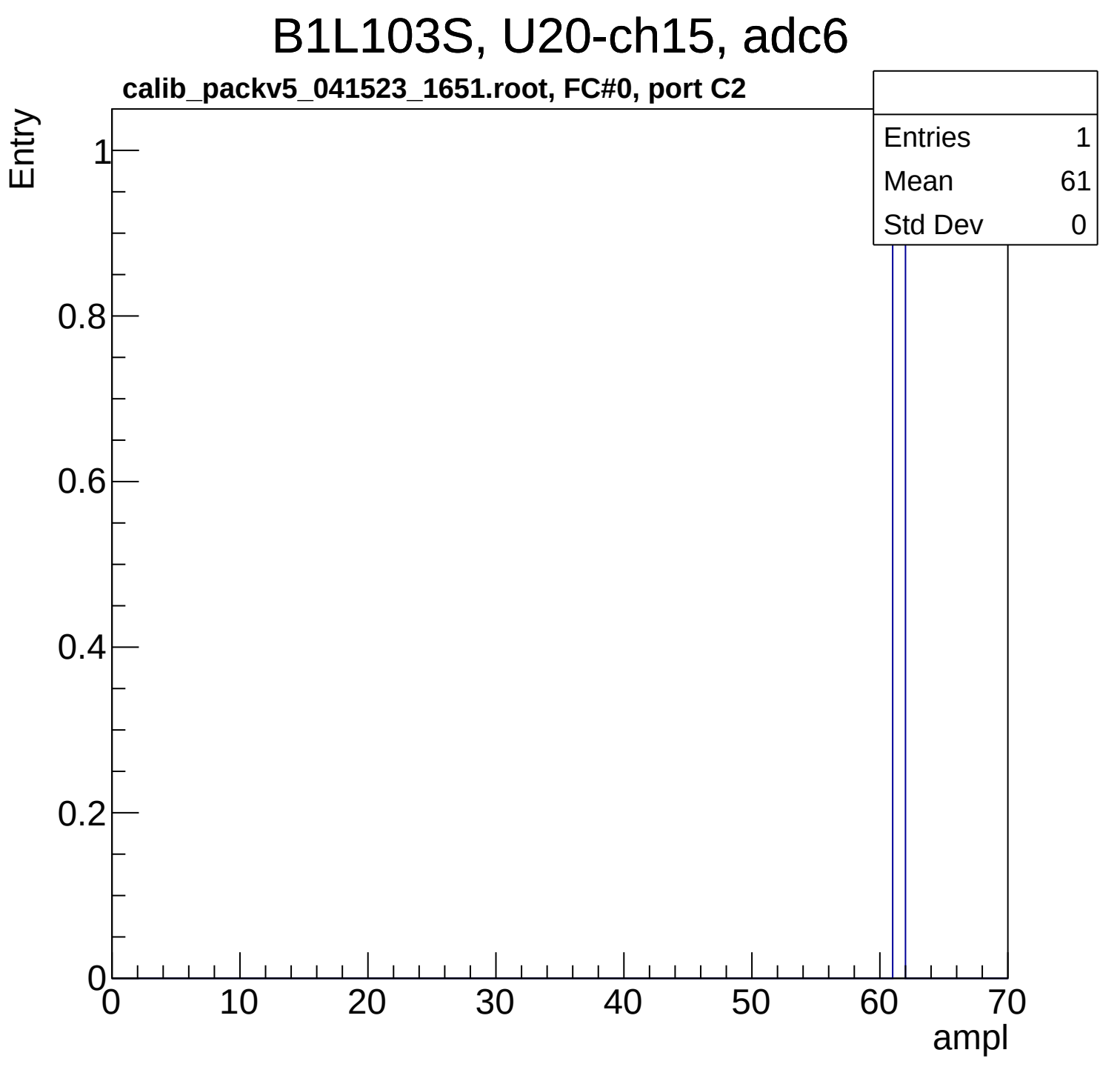
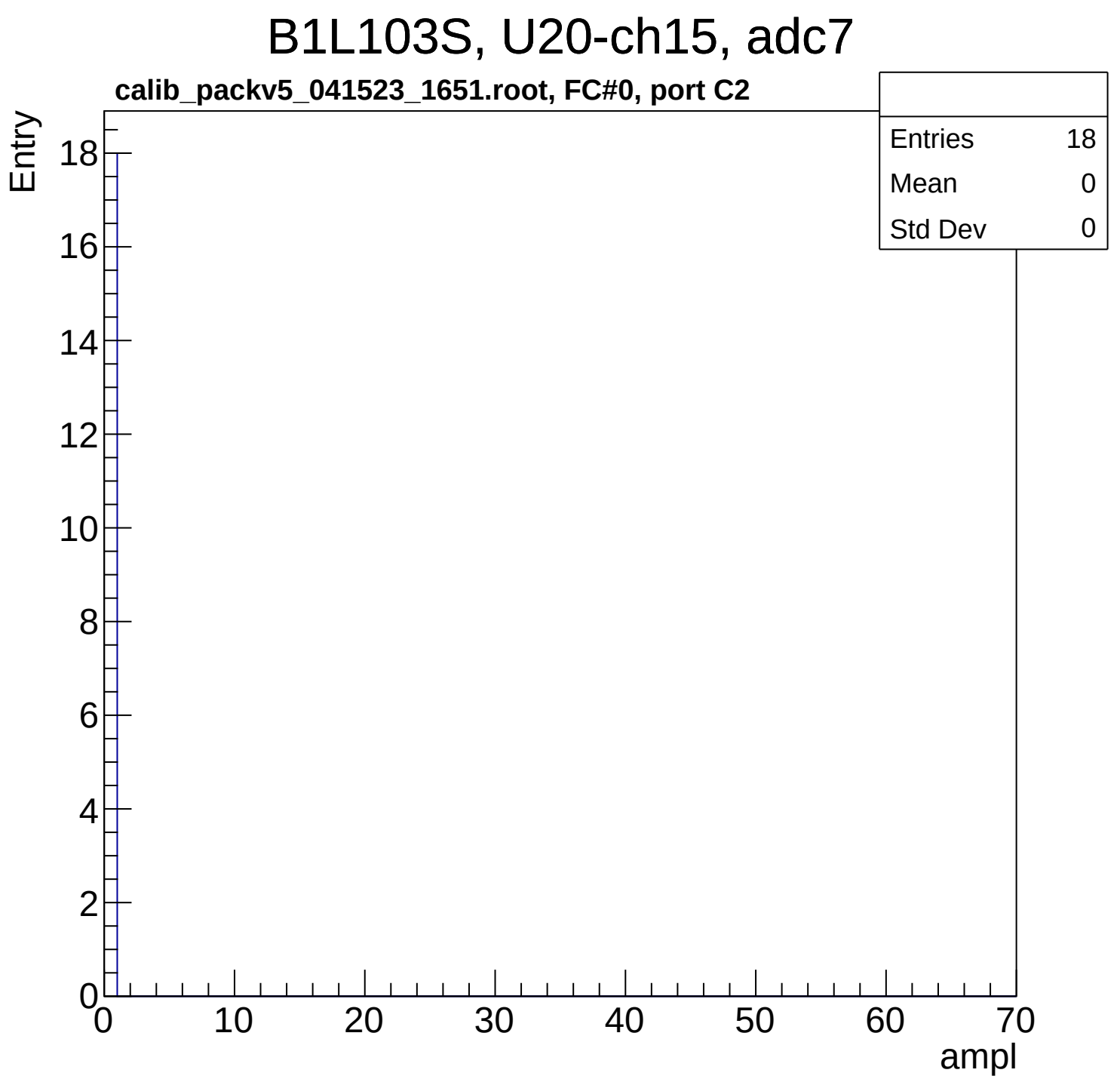
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch15, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 1
Mean 61
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch15, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
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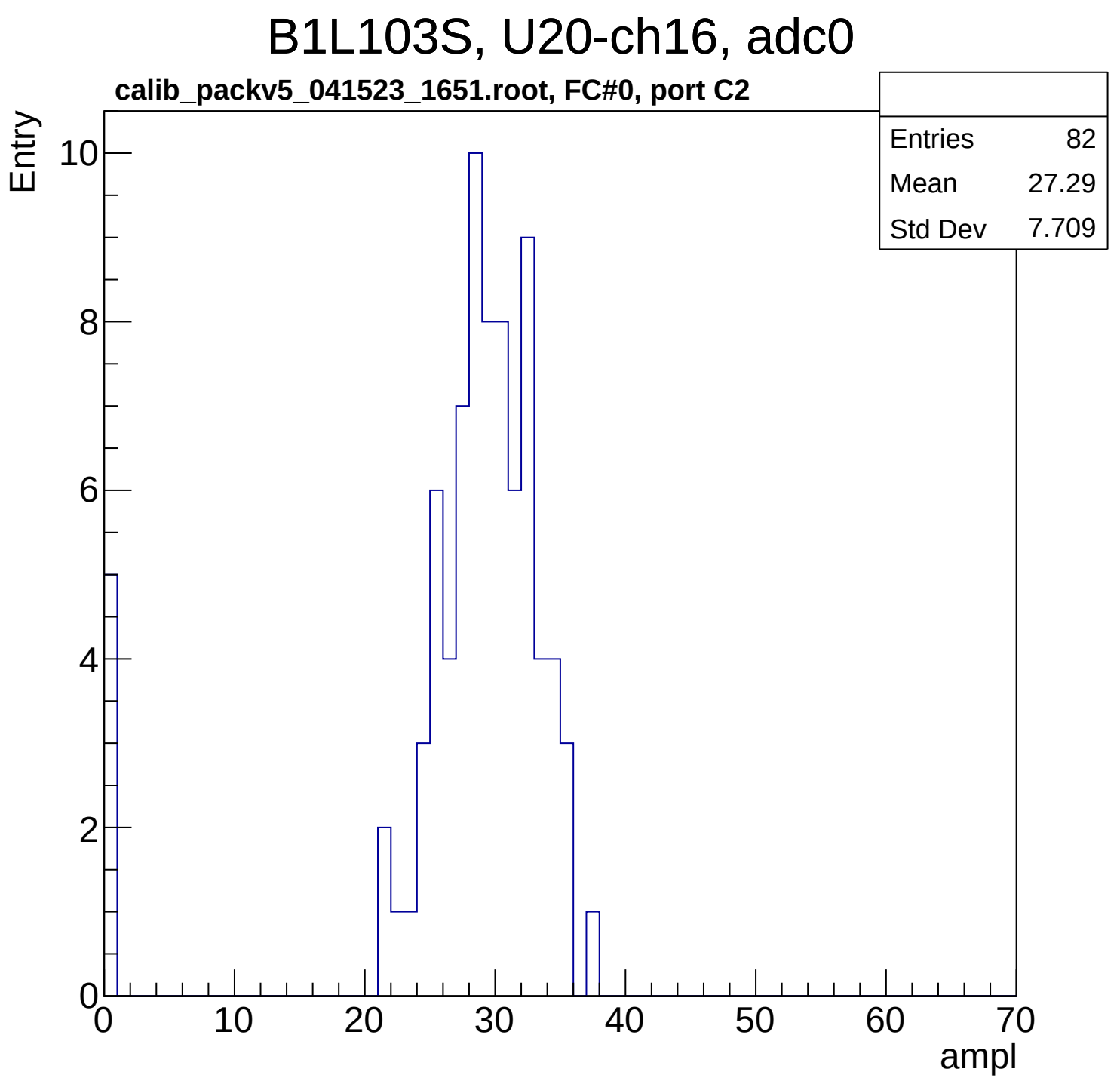
50
60
70
ampl


B1L103S, U20-ch16, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 27.29
Std Dev 7.709
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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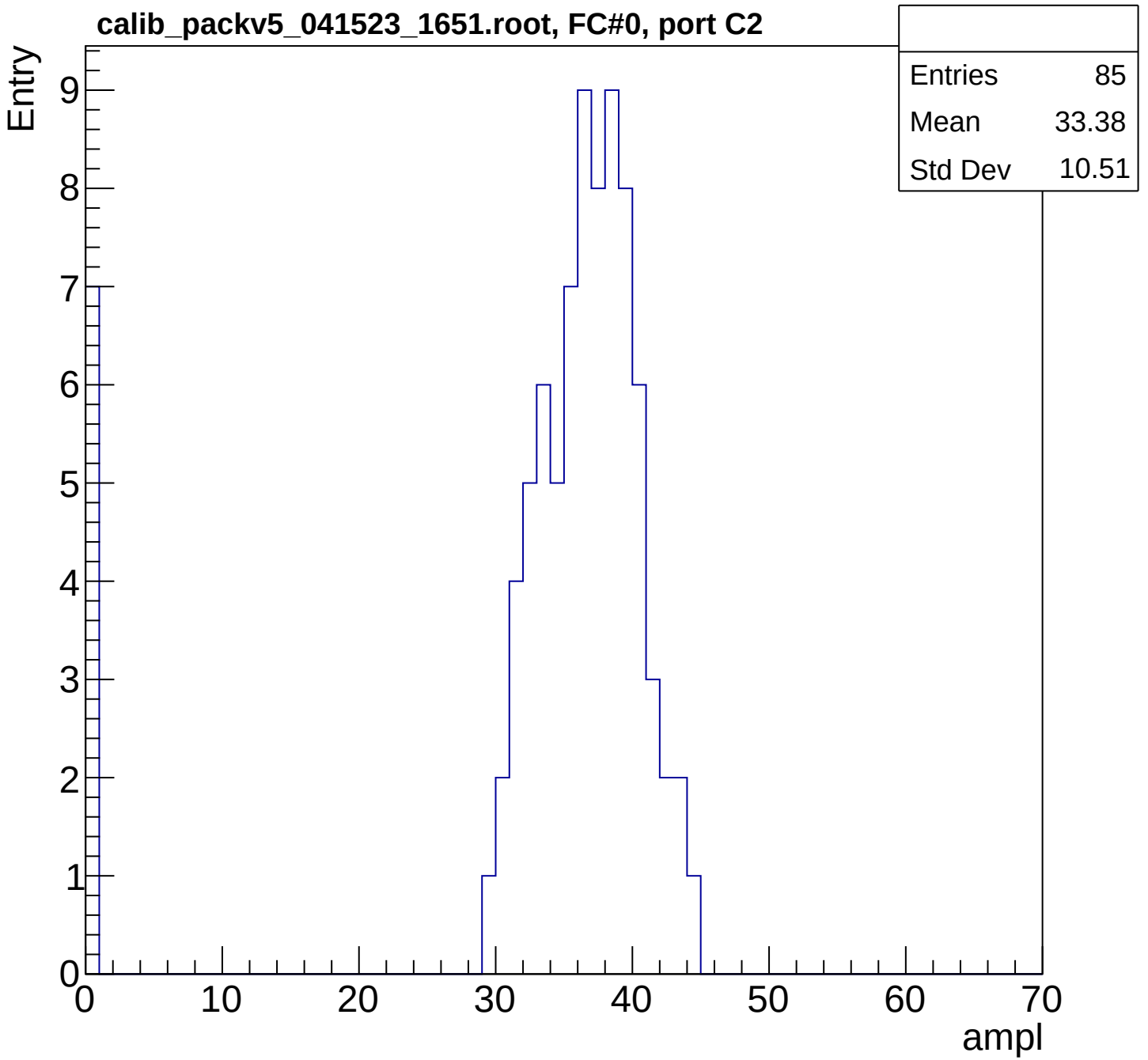
B1L103S, U20-ch16, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 33.38
Std Dev 10.51
Entry
ampl
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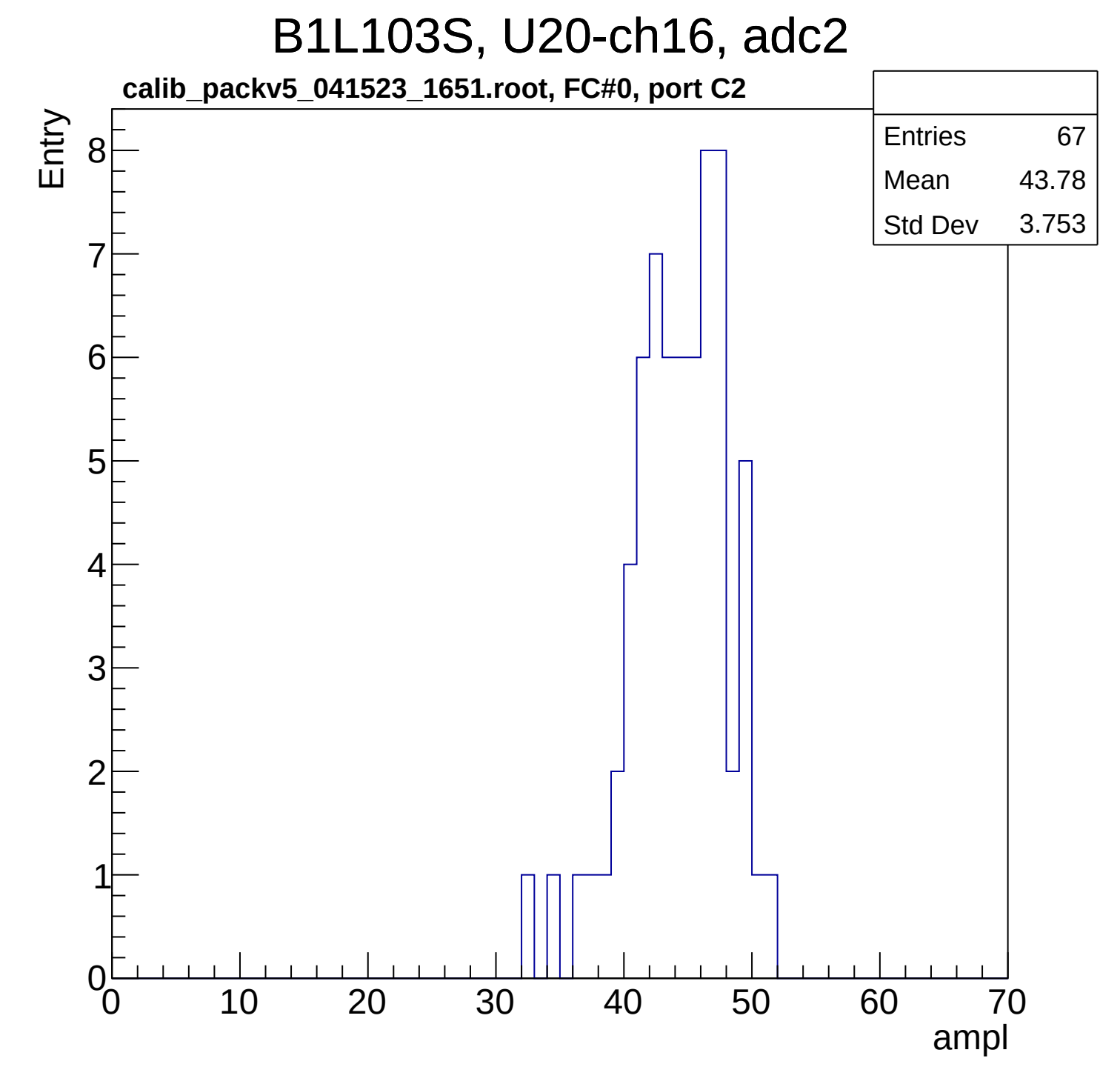
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch16, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 43.78
Std Dev 3.753
Entry
ampl
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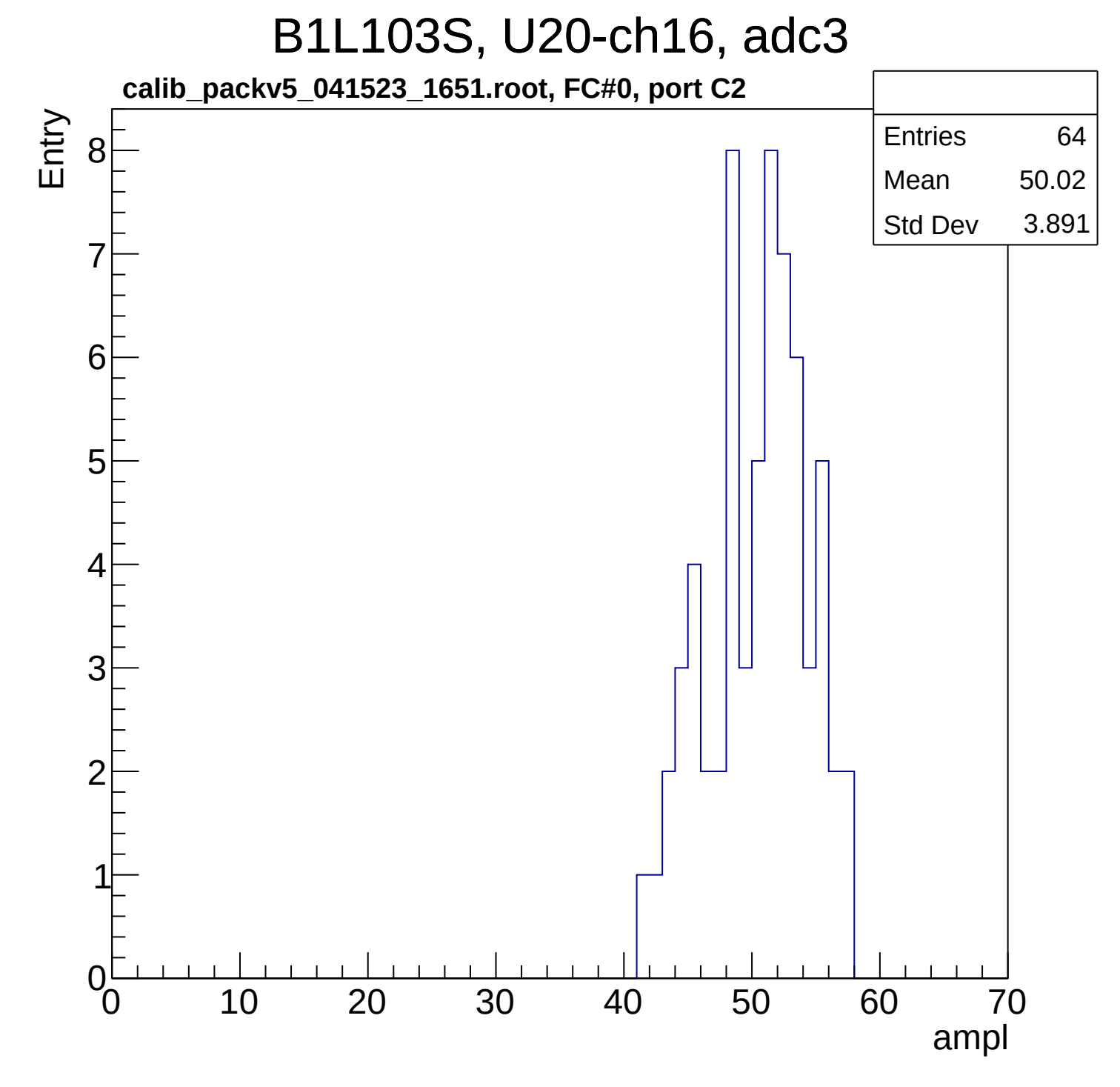
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch16, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 50.02
Std Dev 3.891
Entry
ampl
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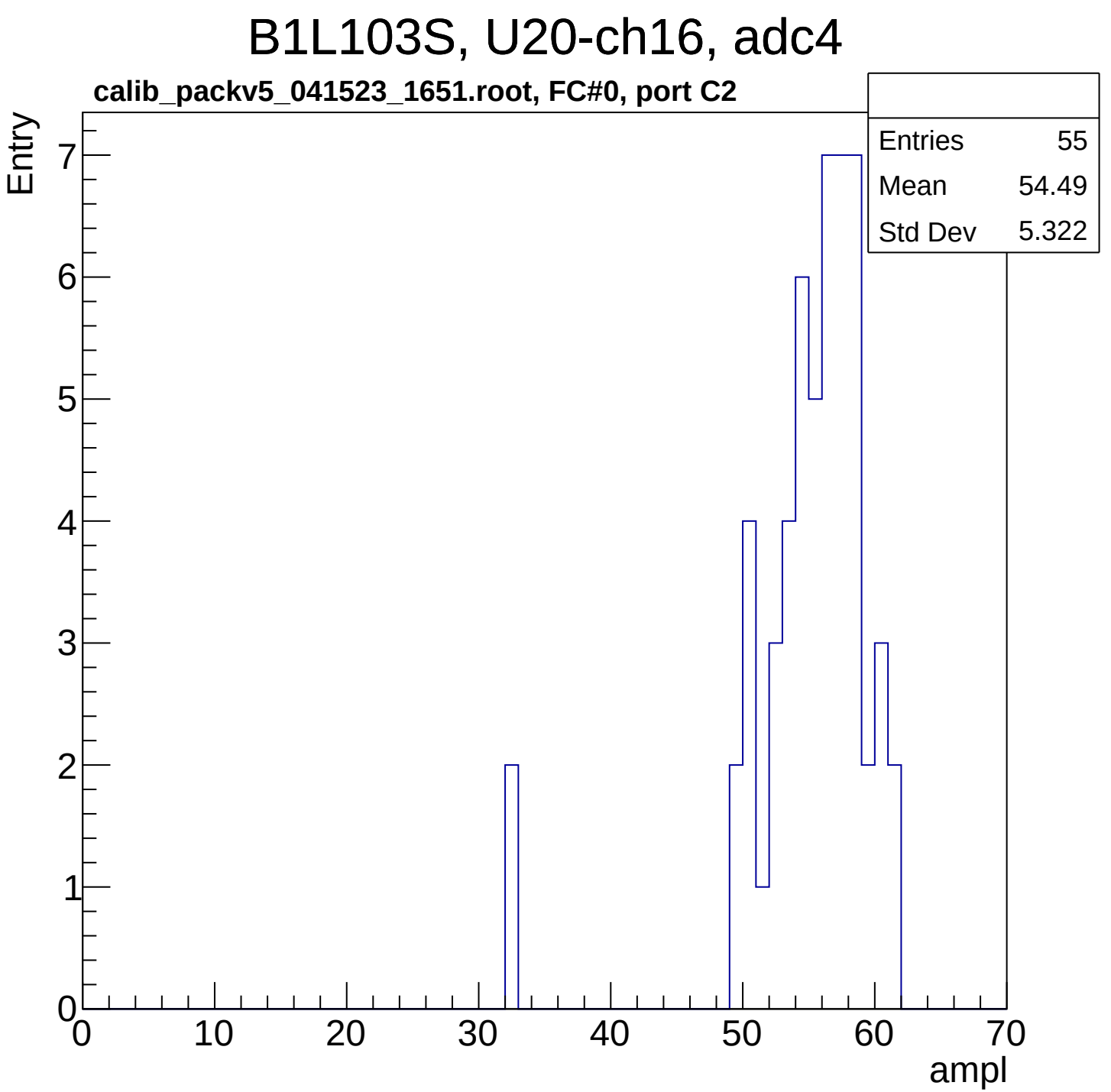
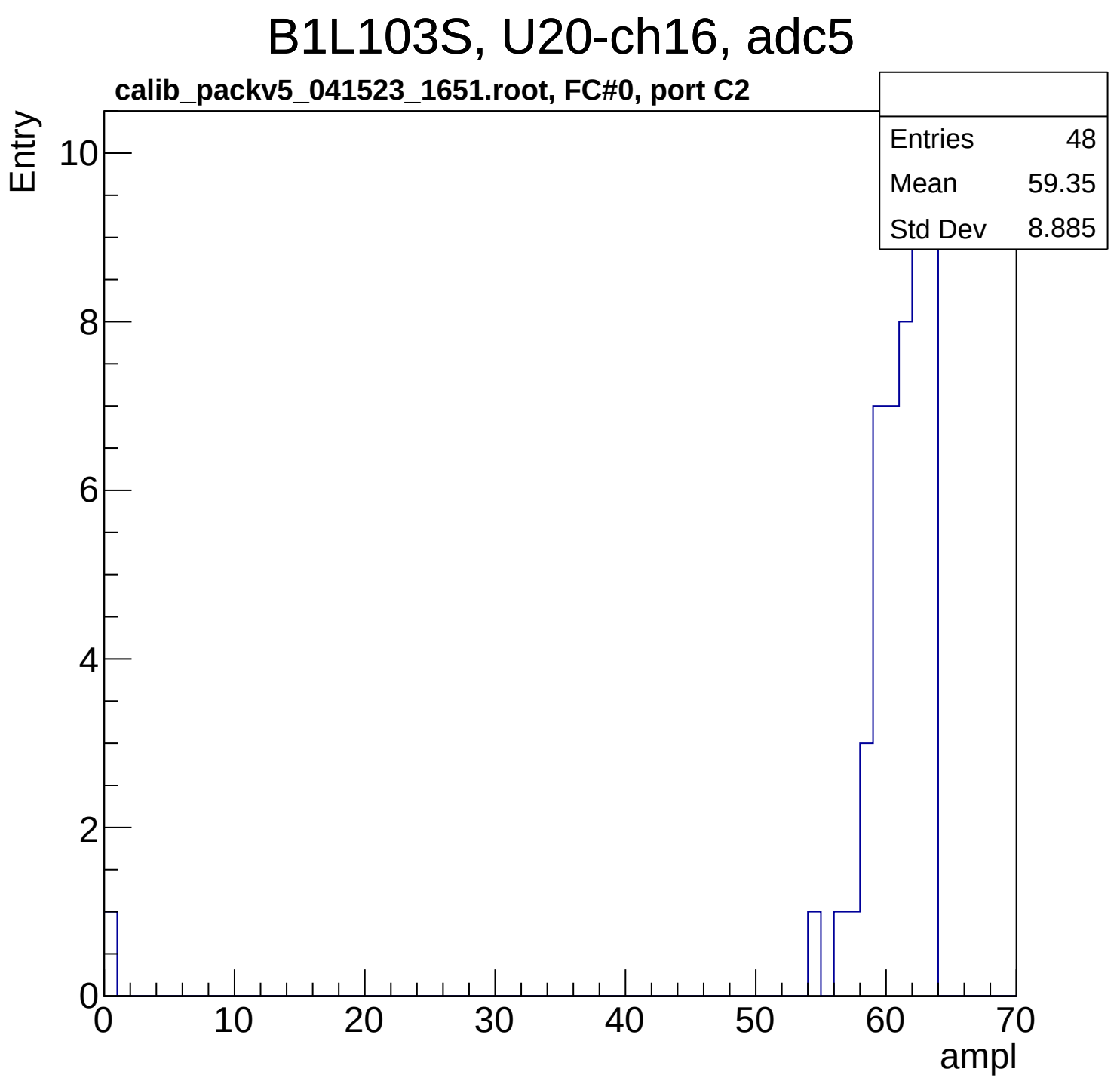
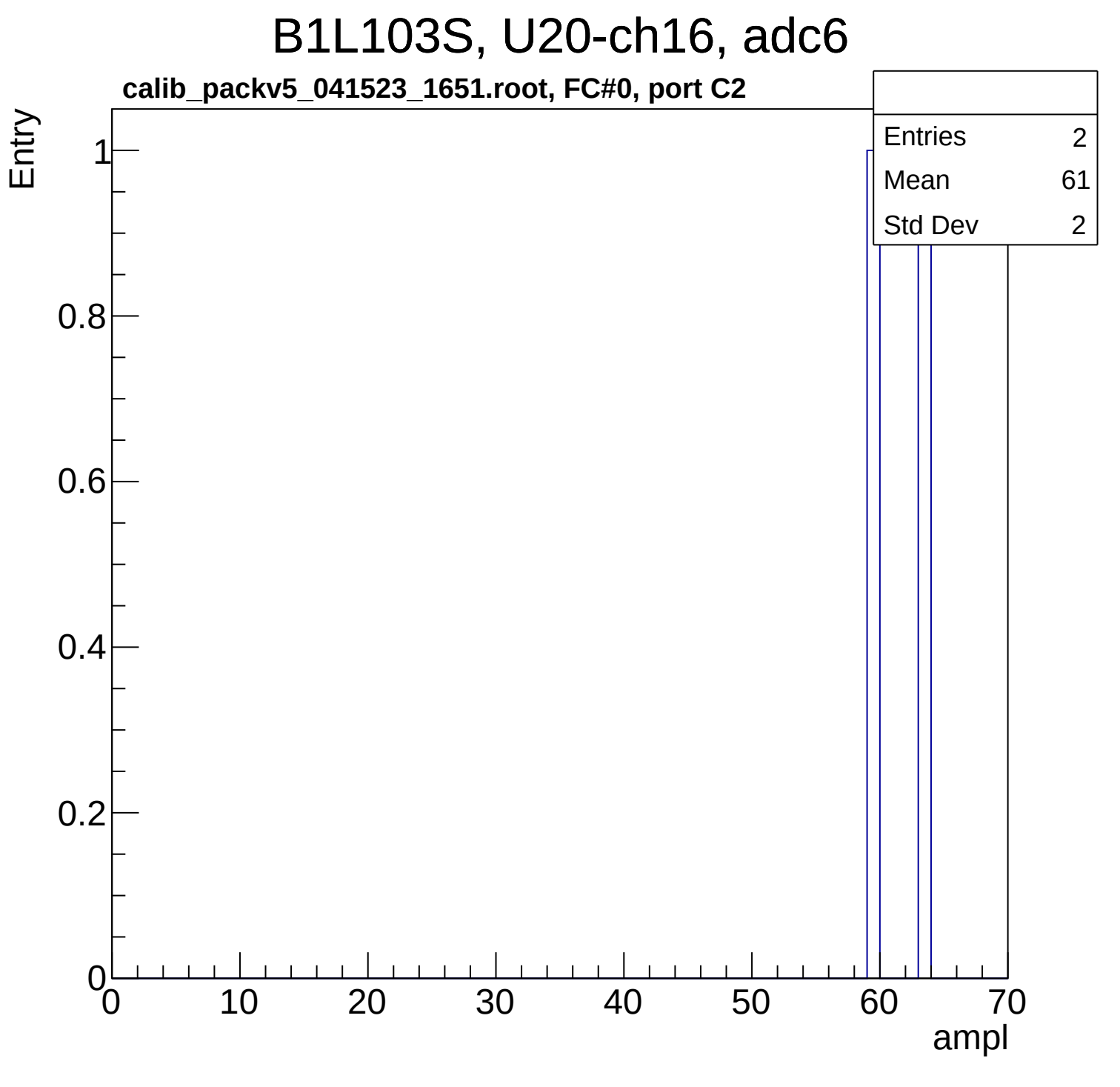
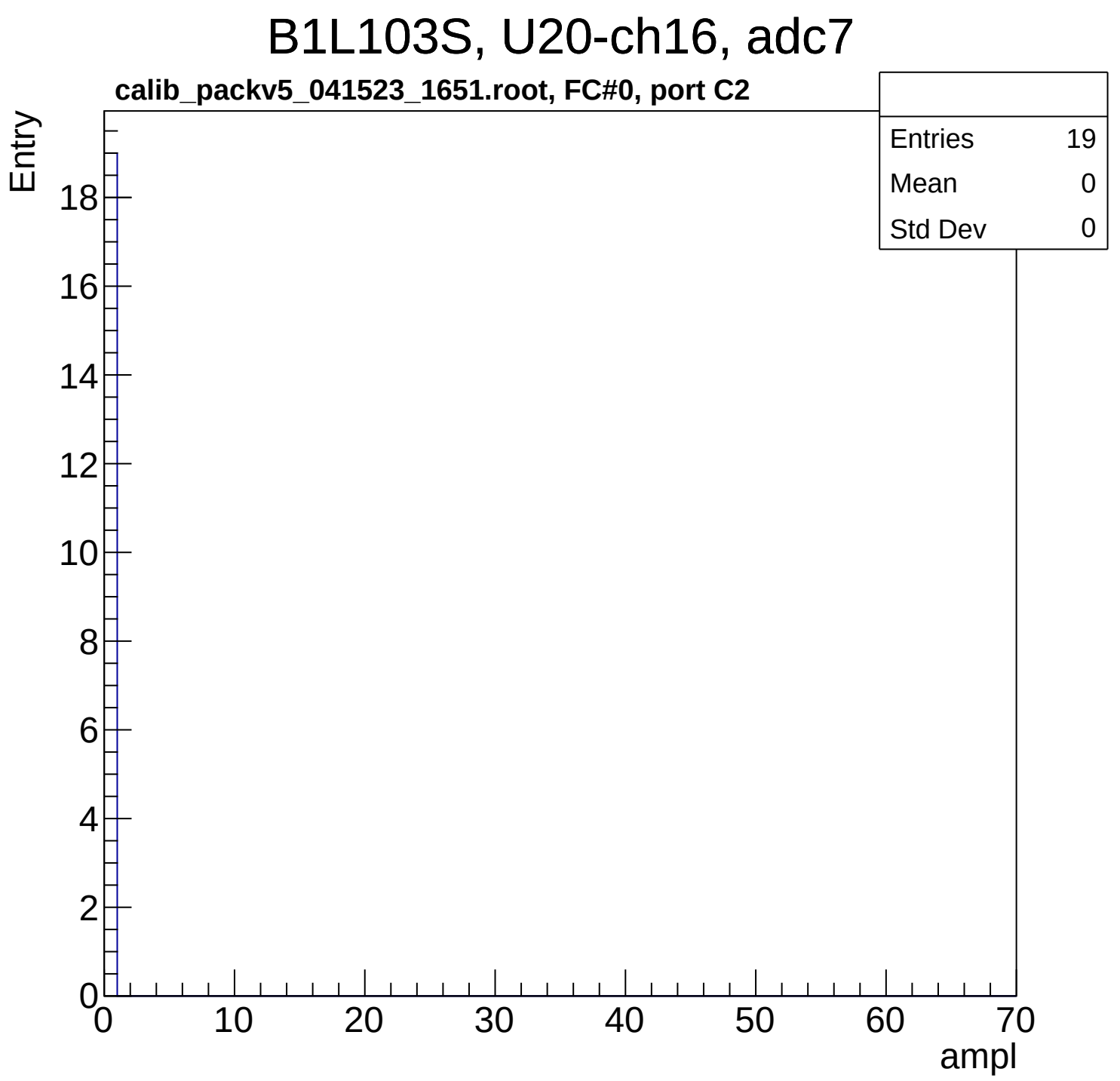
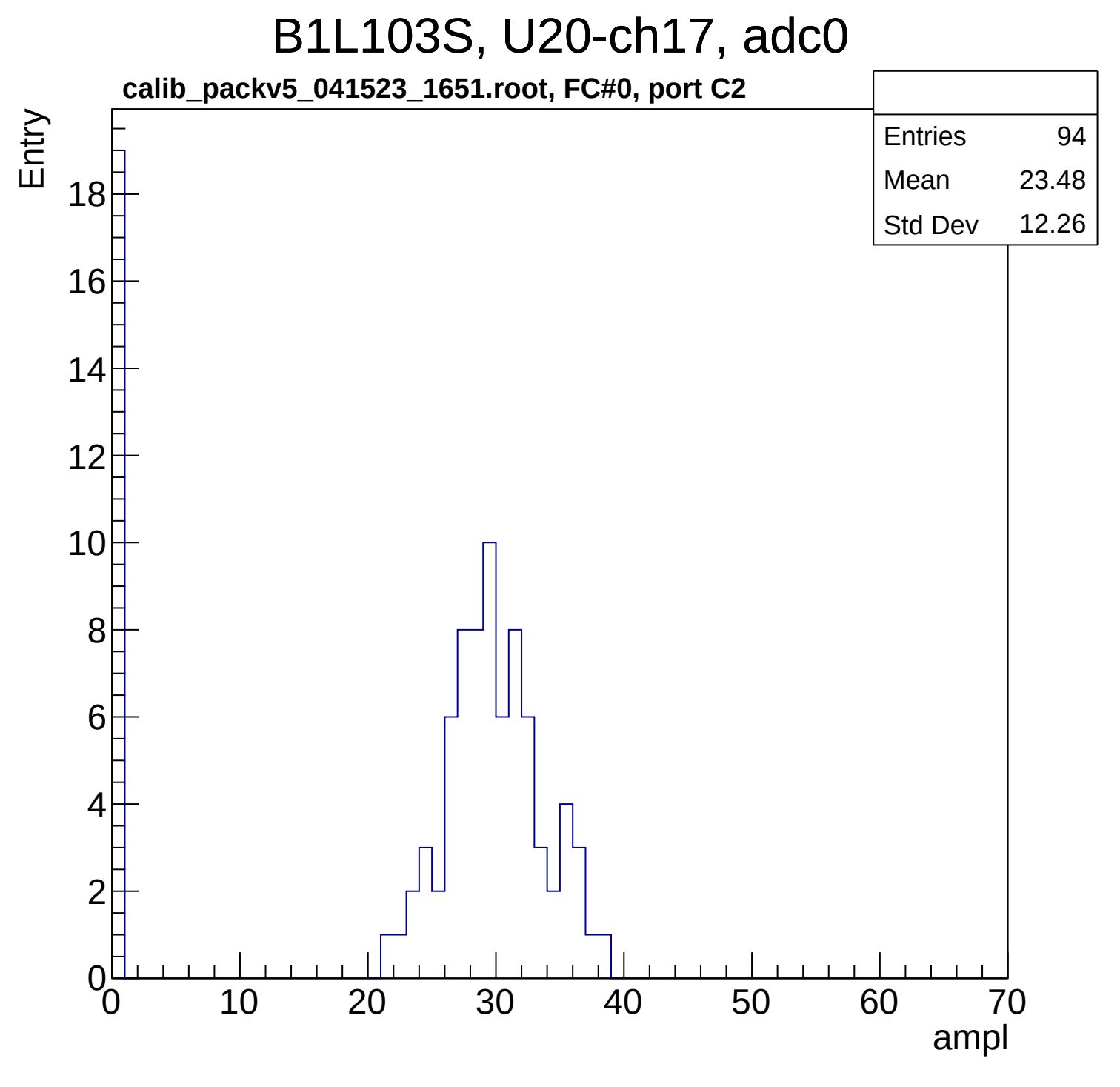
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

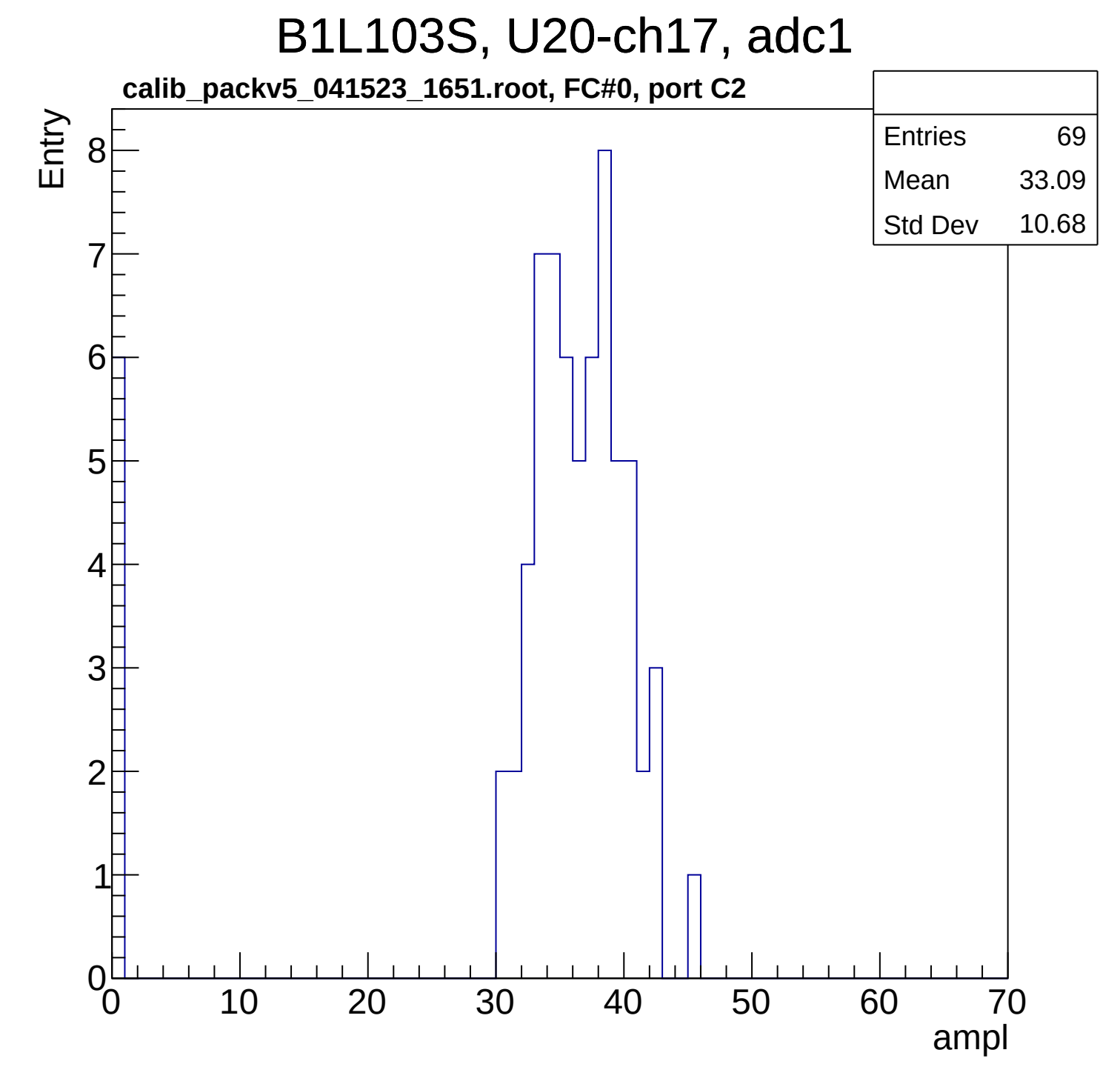

B1L103S, U20-ch16, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 54.49
Std Dev 5.322
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U20-ch16, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 59.35
Std Dev 8.885
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U20-ch16, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 61
Std Dev 2
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch16, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch17, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 23.48
Std Dev 12.26
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch17, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 33.09
Std Dev 10.68
Entry
ampl
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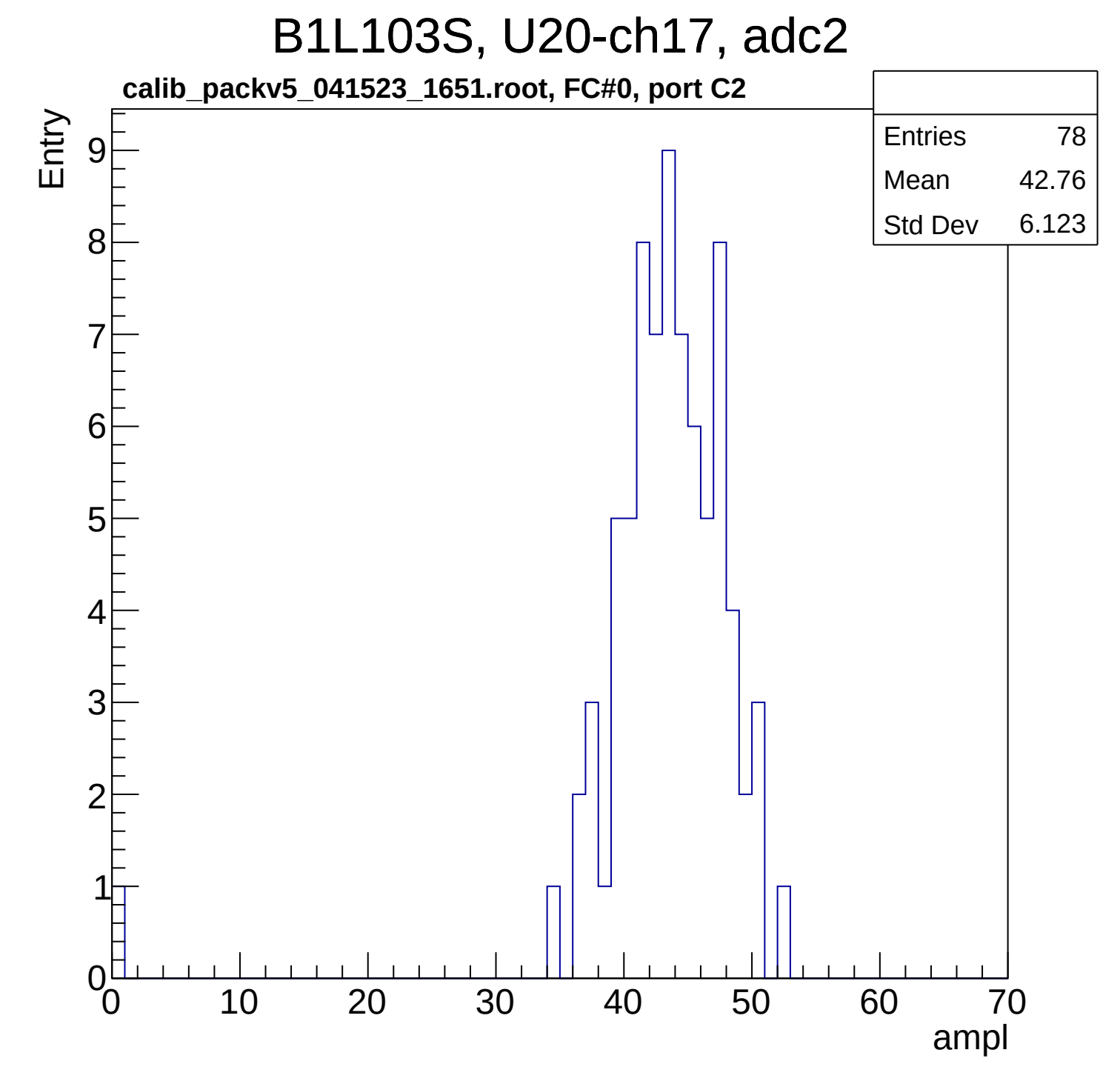
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch17, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 42.76
Std Dev 6.123
Entry
ampl
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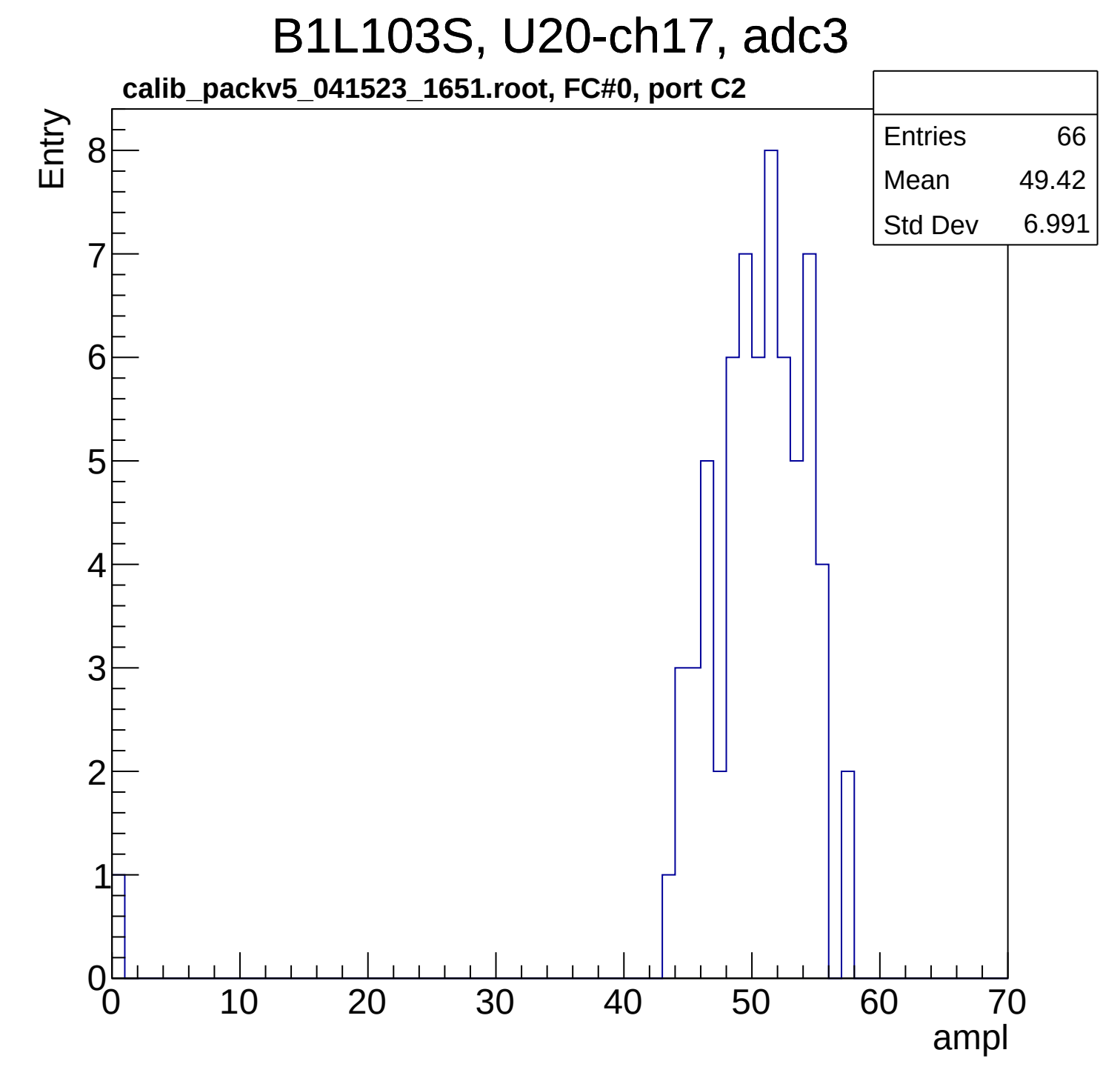
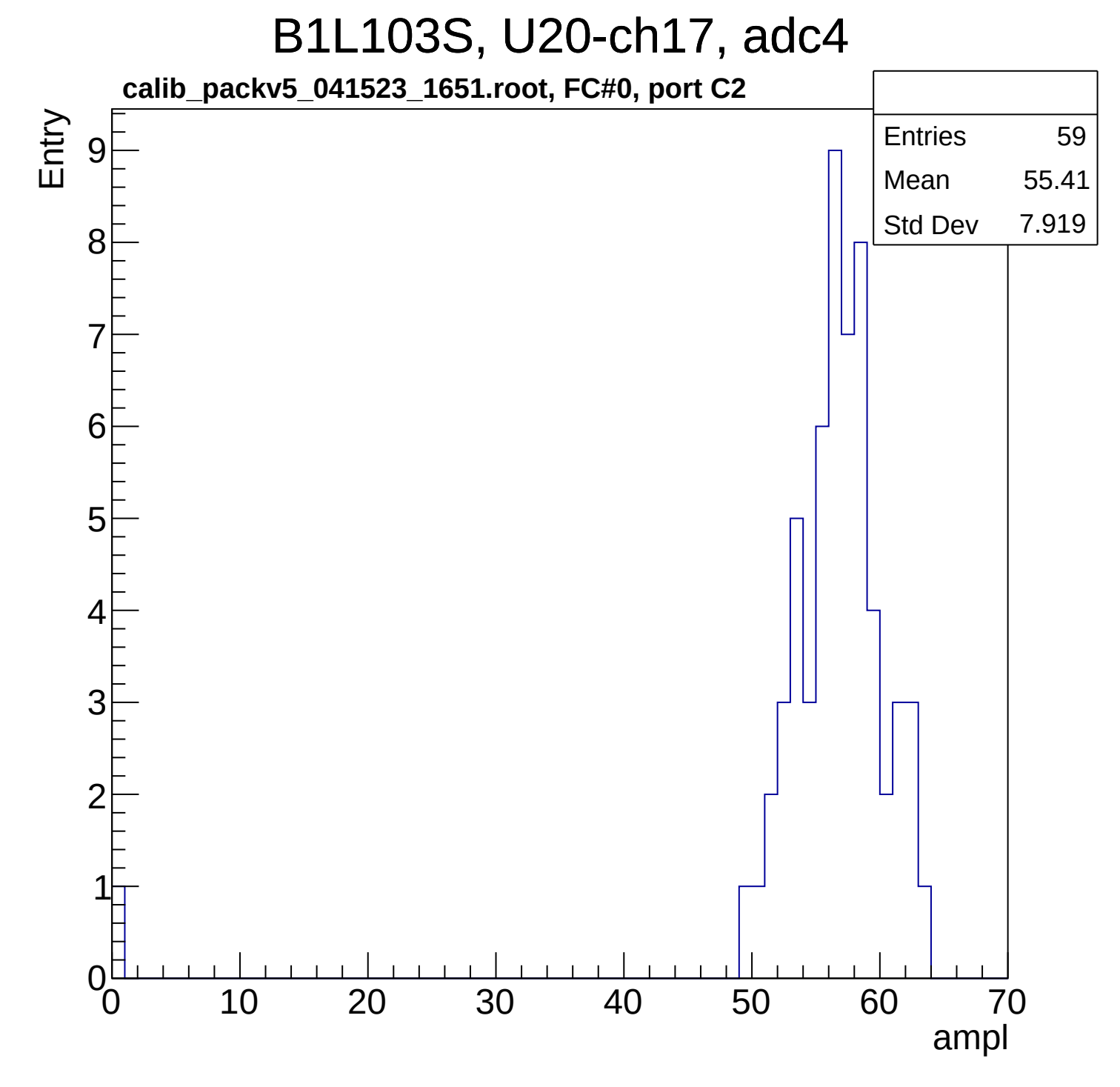
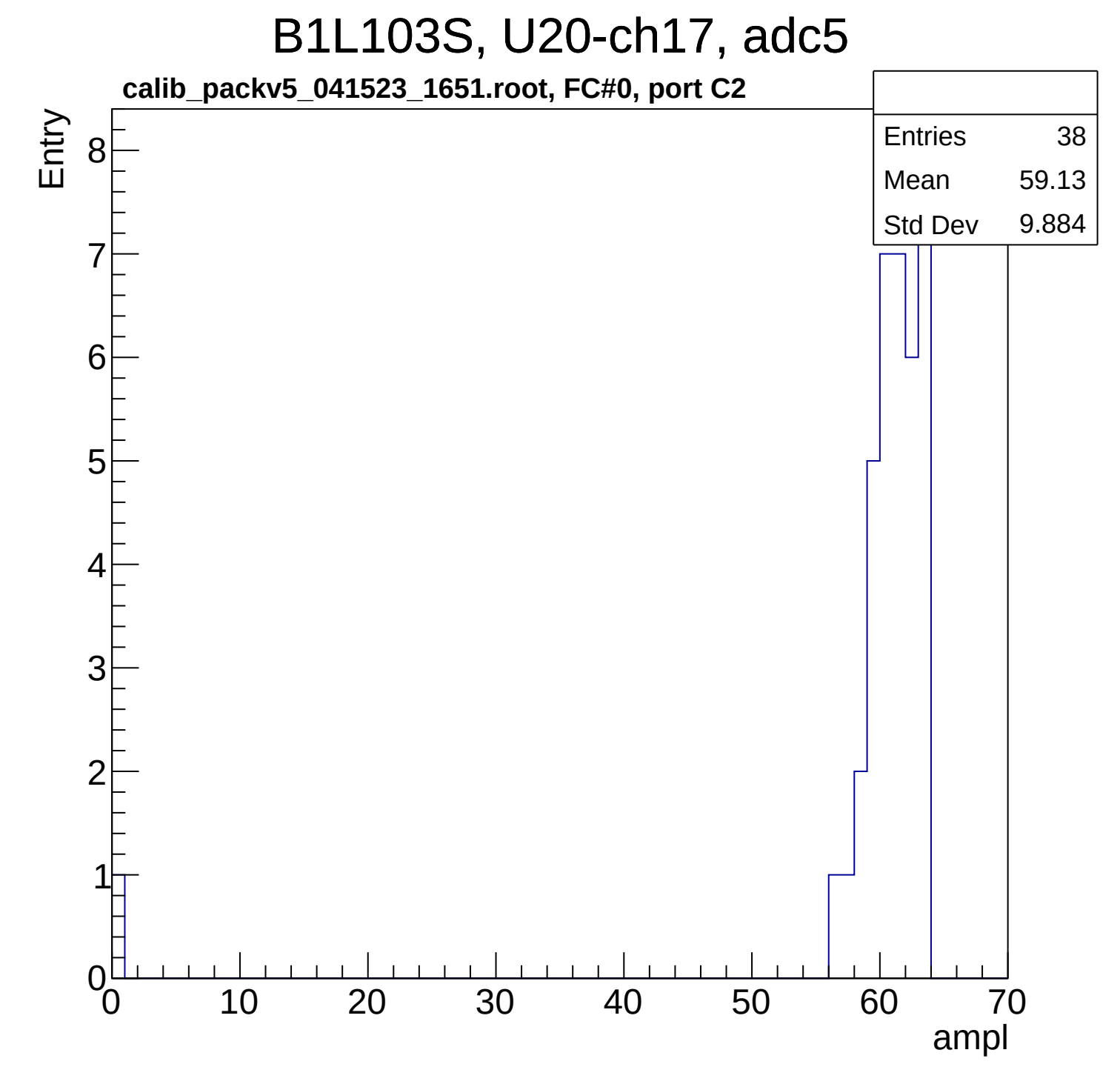
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch17, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 49.42
Std Dev 6.991
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch17, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 55.41
Std Dev 7.919
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch17, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 59.13
Std Dev 9.884
Entry
ampl
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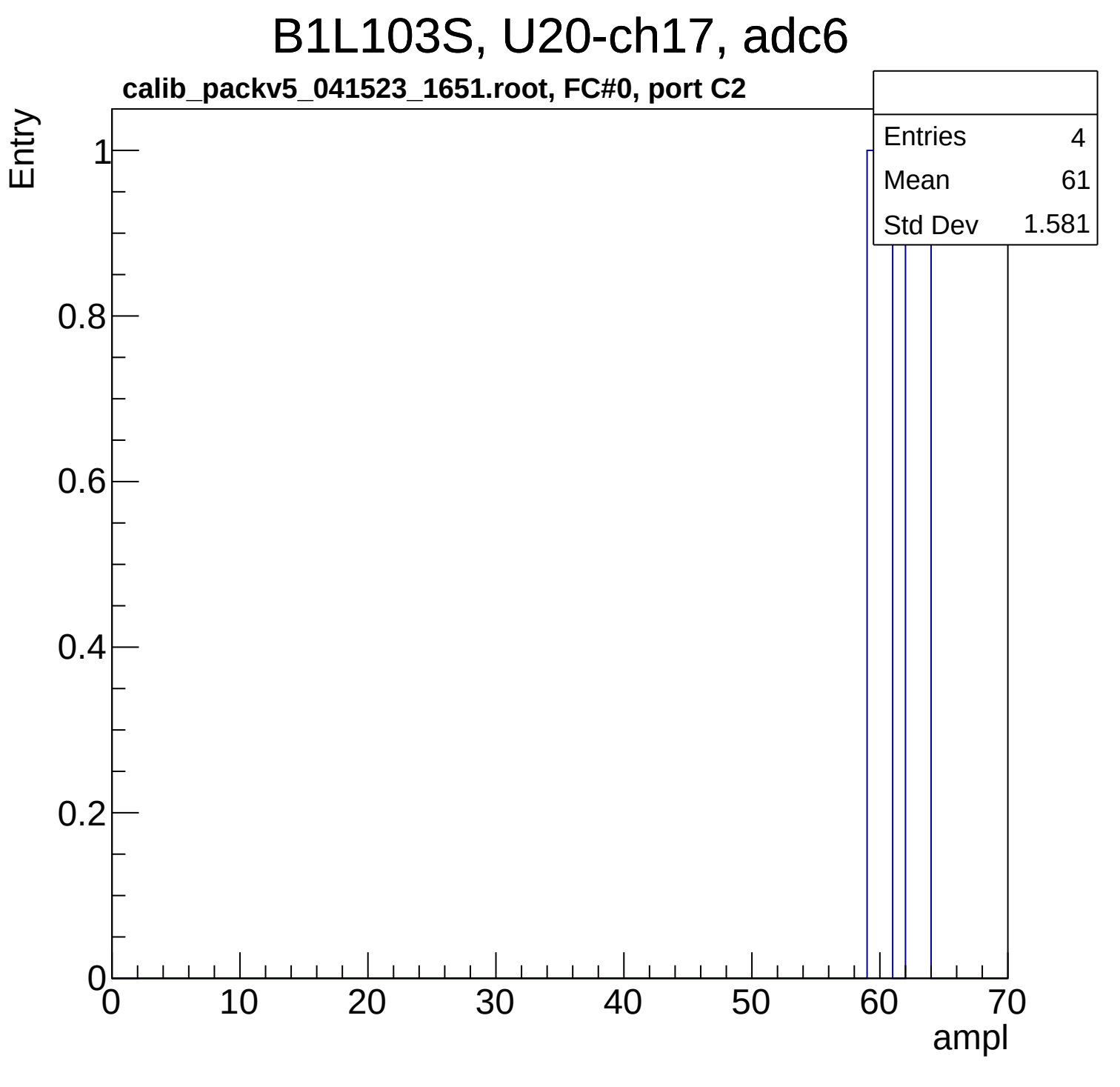
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch17, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 61
Std Dev 1.581
Entry
ampl
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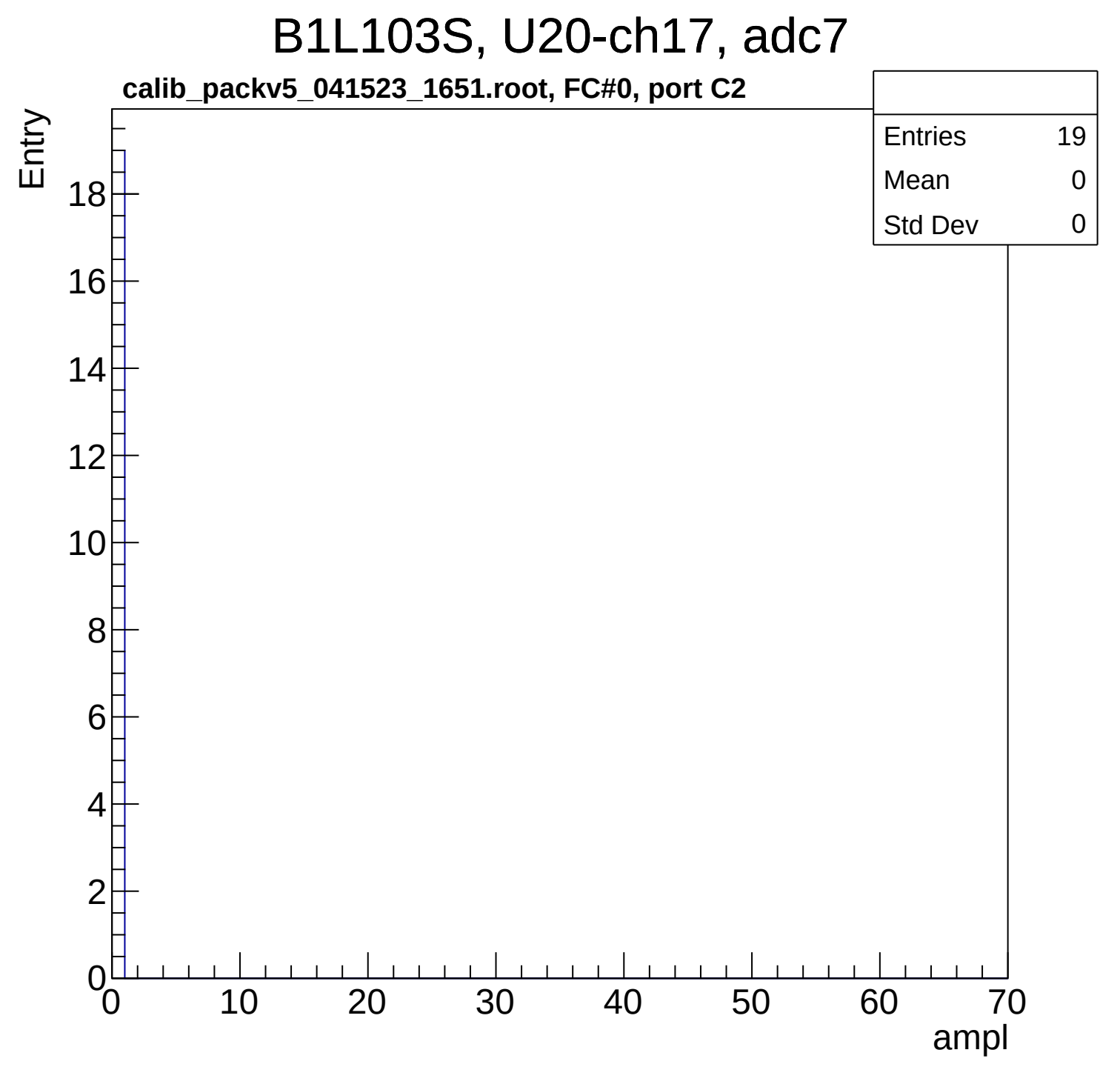
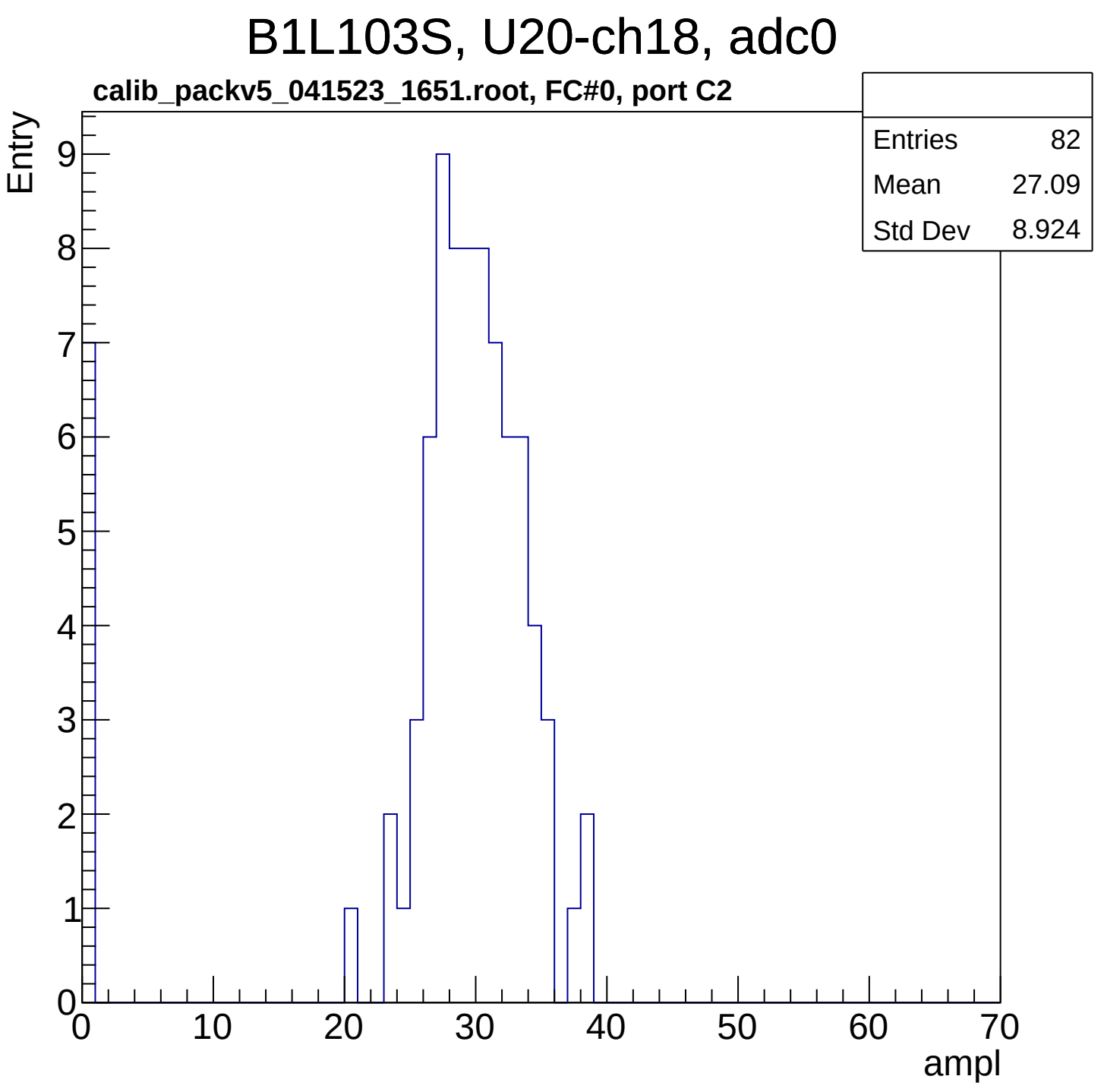
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B1L103S, U20-ch17, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch18, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 27.09
Std Dev 8.924
Entry
ampl
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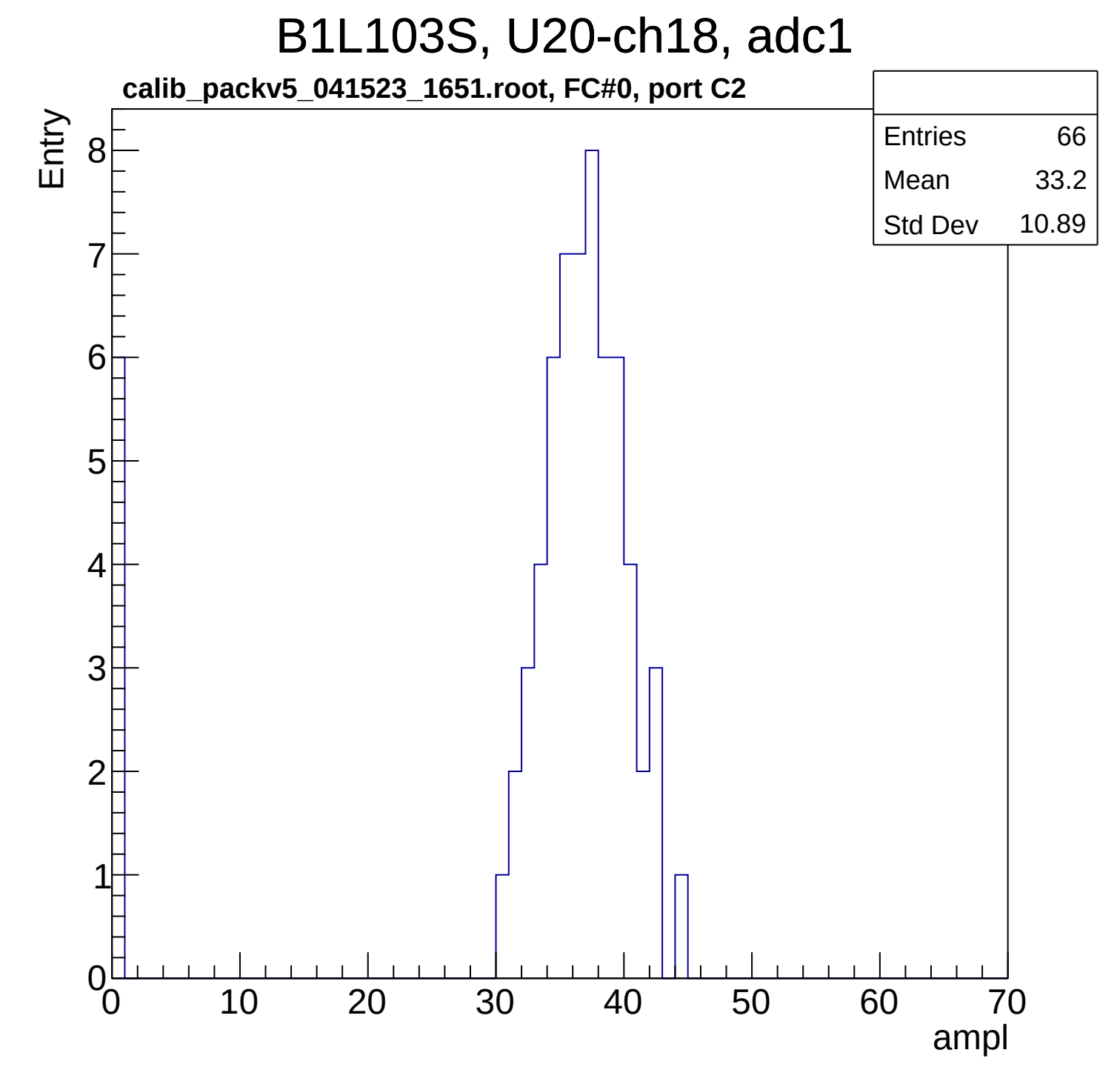
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch18, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 33.2
Std Dev 10.89
Entry
ampl
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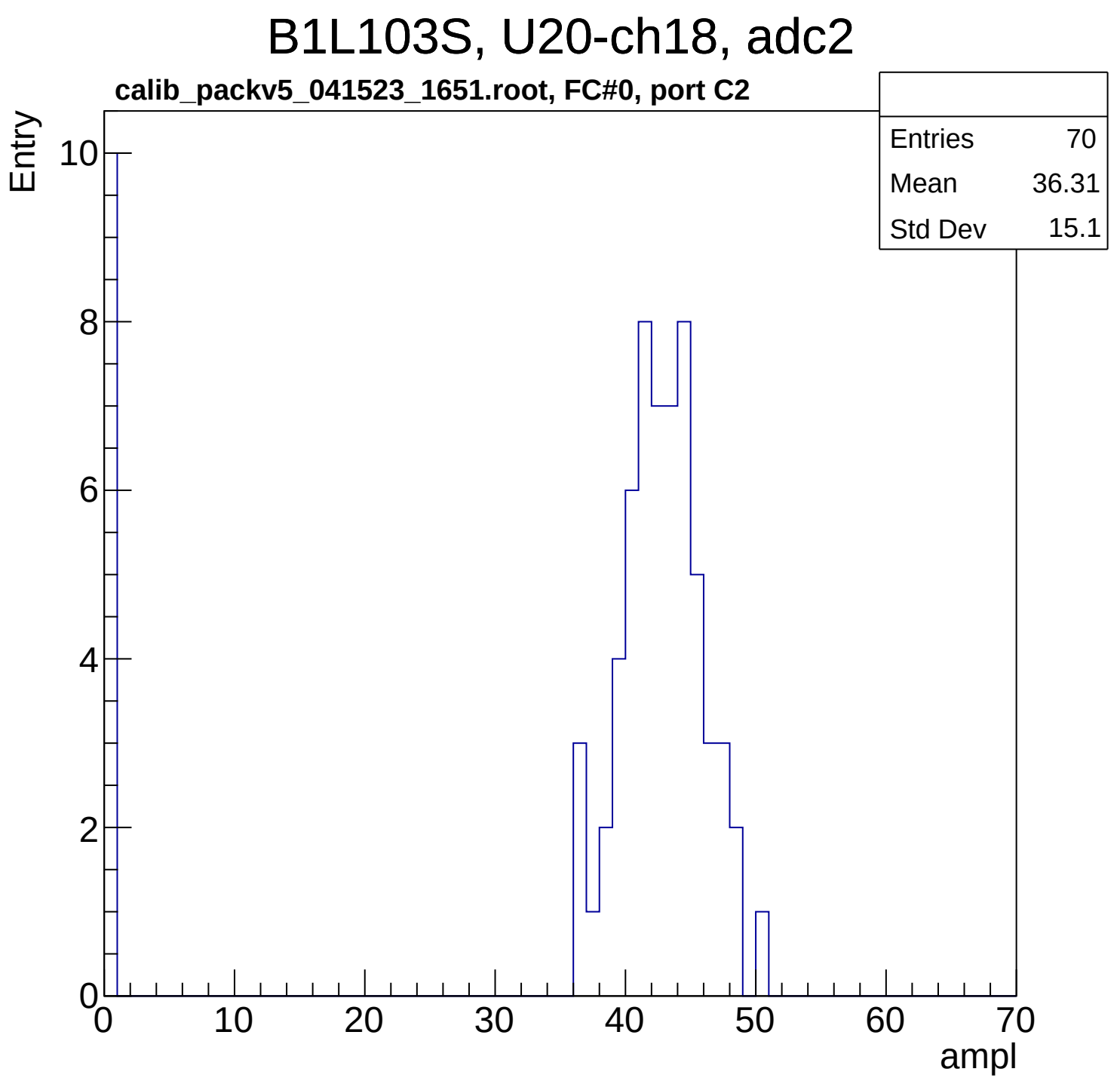
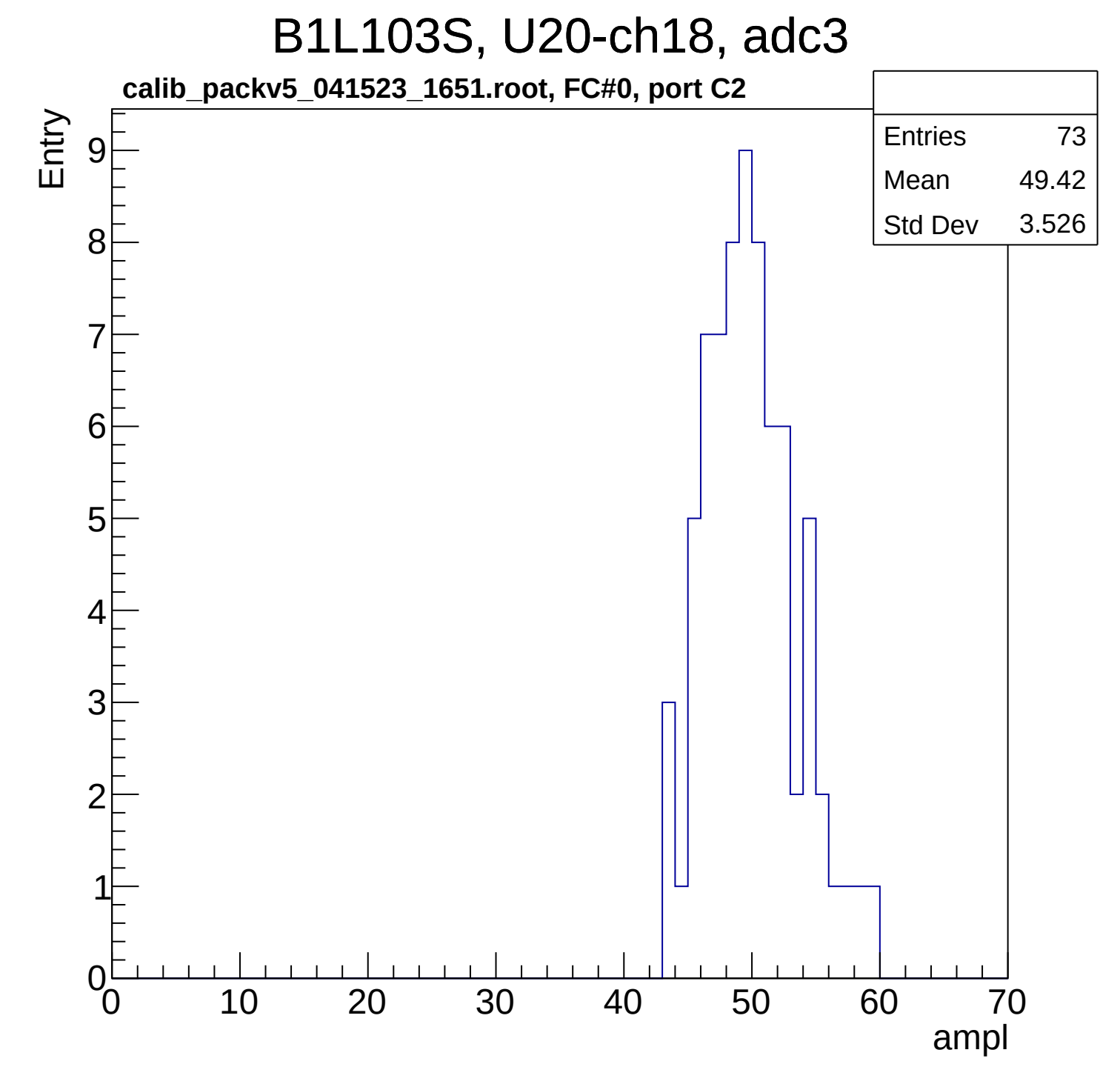
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch18, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 36.31
Std Dev 15.1
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch18, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 49.42
Std Dev 3.526
Entry
ampl
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2
3
4
5
6
7
8
9
0
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50
60
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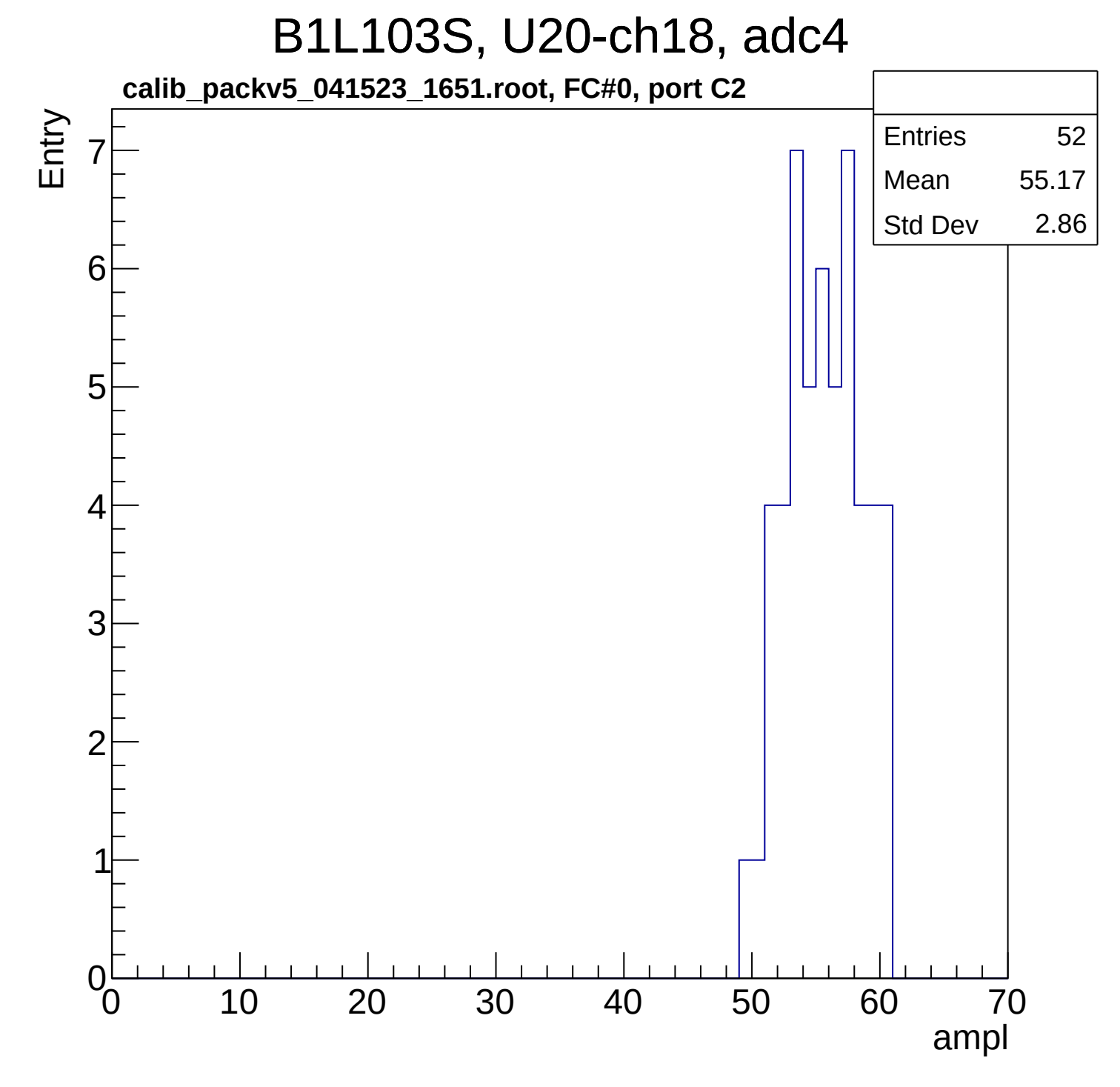
B1L103S, U20-ch18, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 55.17
Std Dev 2.86
Entry
ampl
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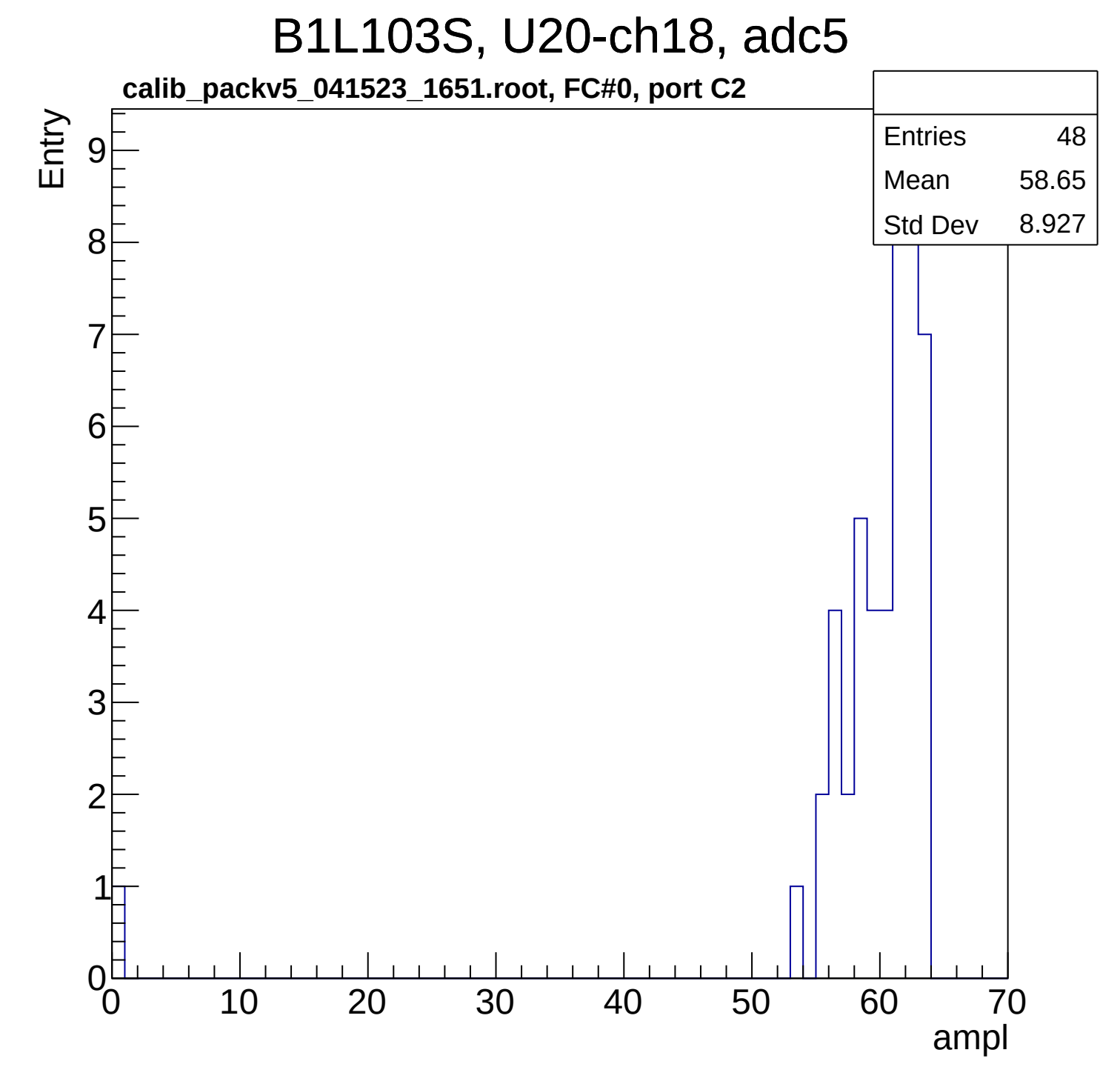
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U20-ch18, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 58.65
Std Dev 8.927
Entry
ampl
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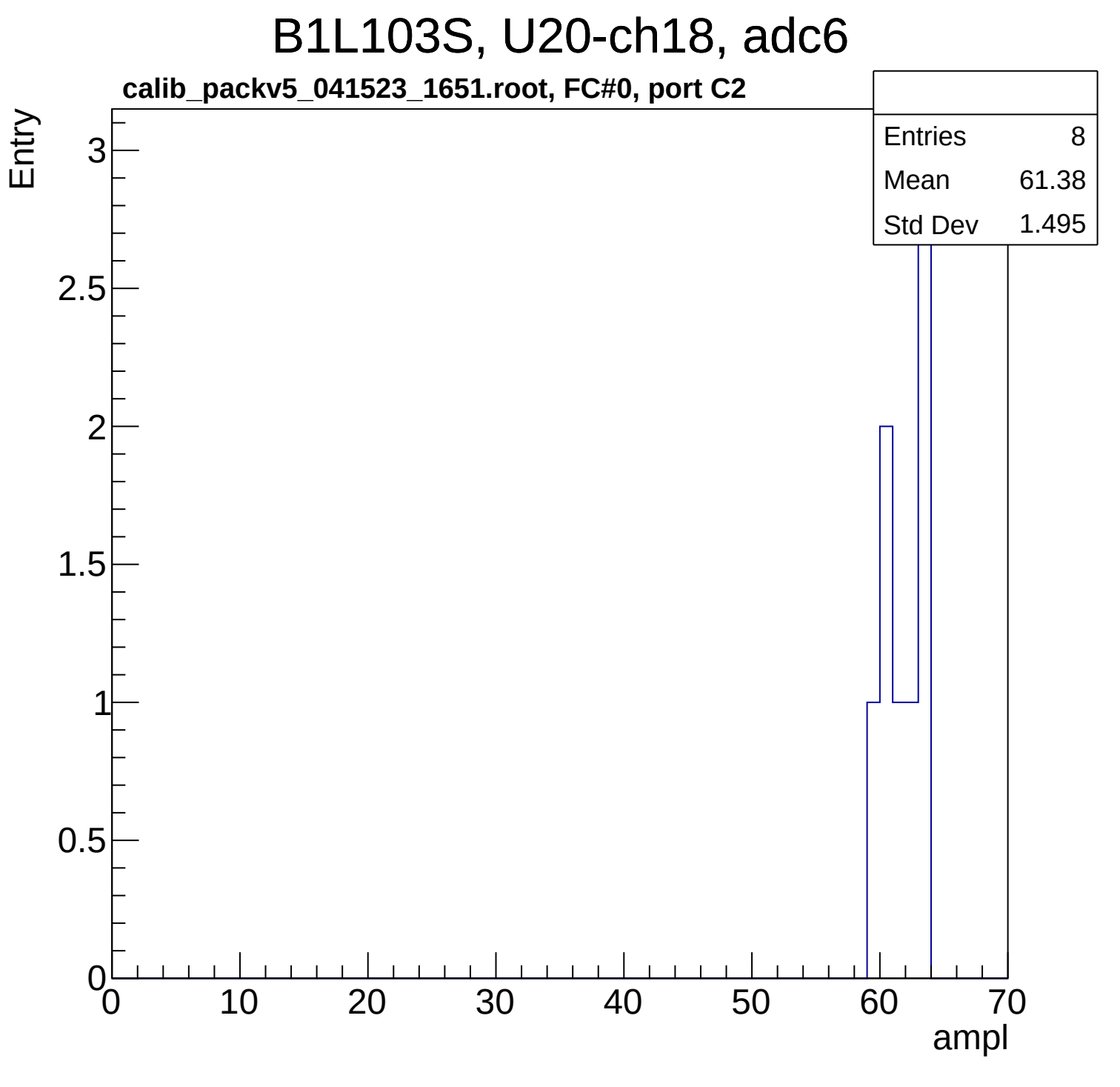
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch18, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 61.38
Std Dev 1.495
Entry
ampl
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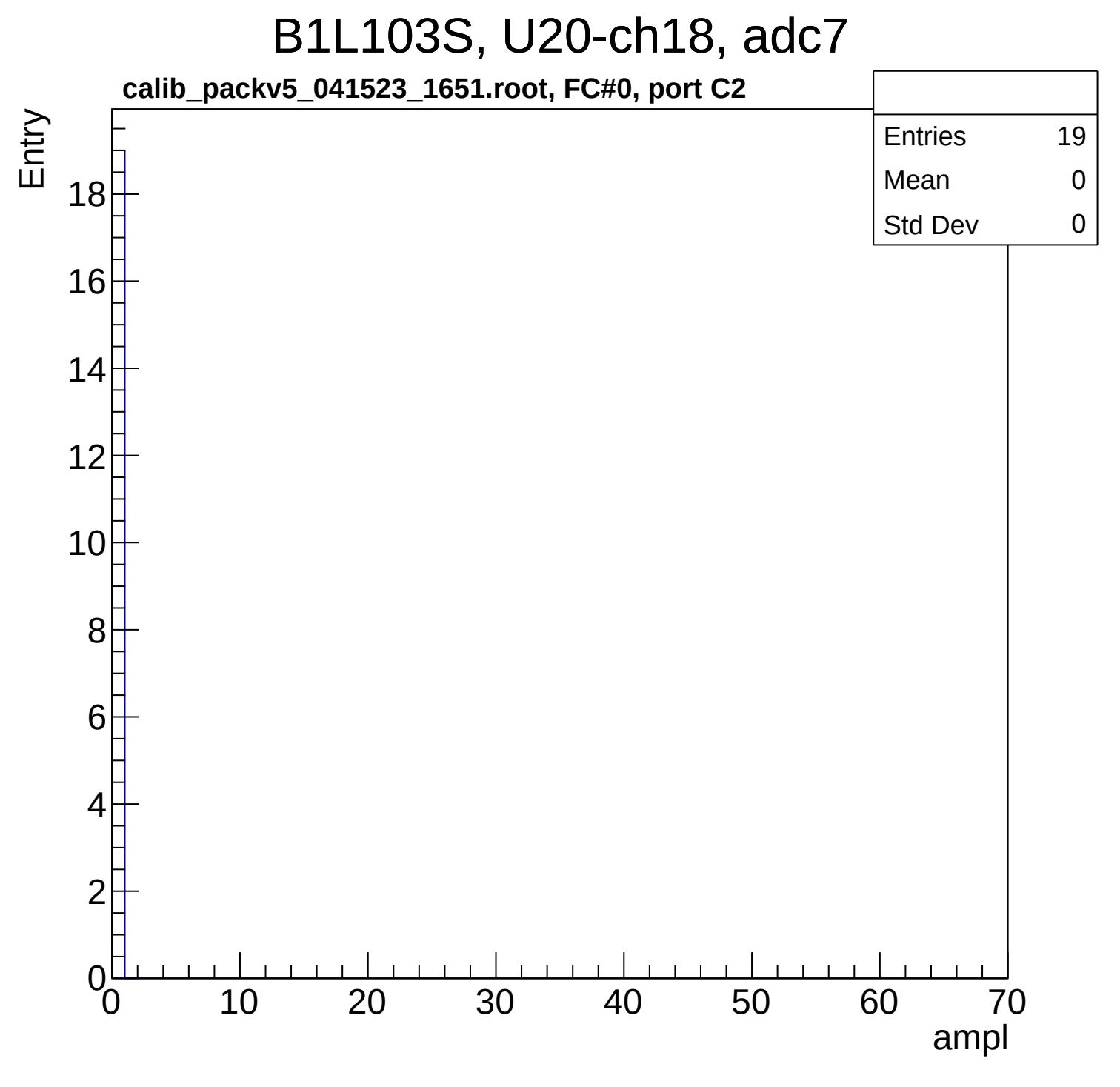
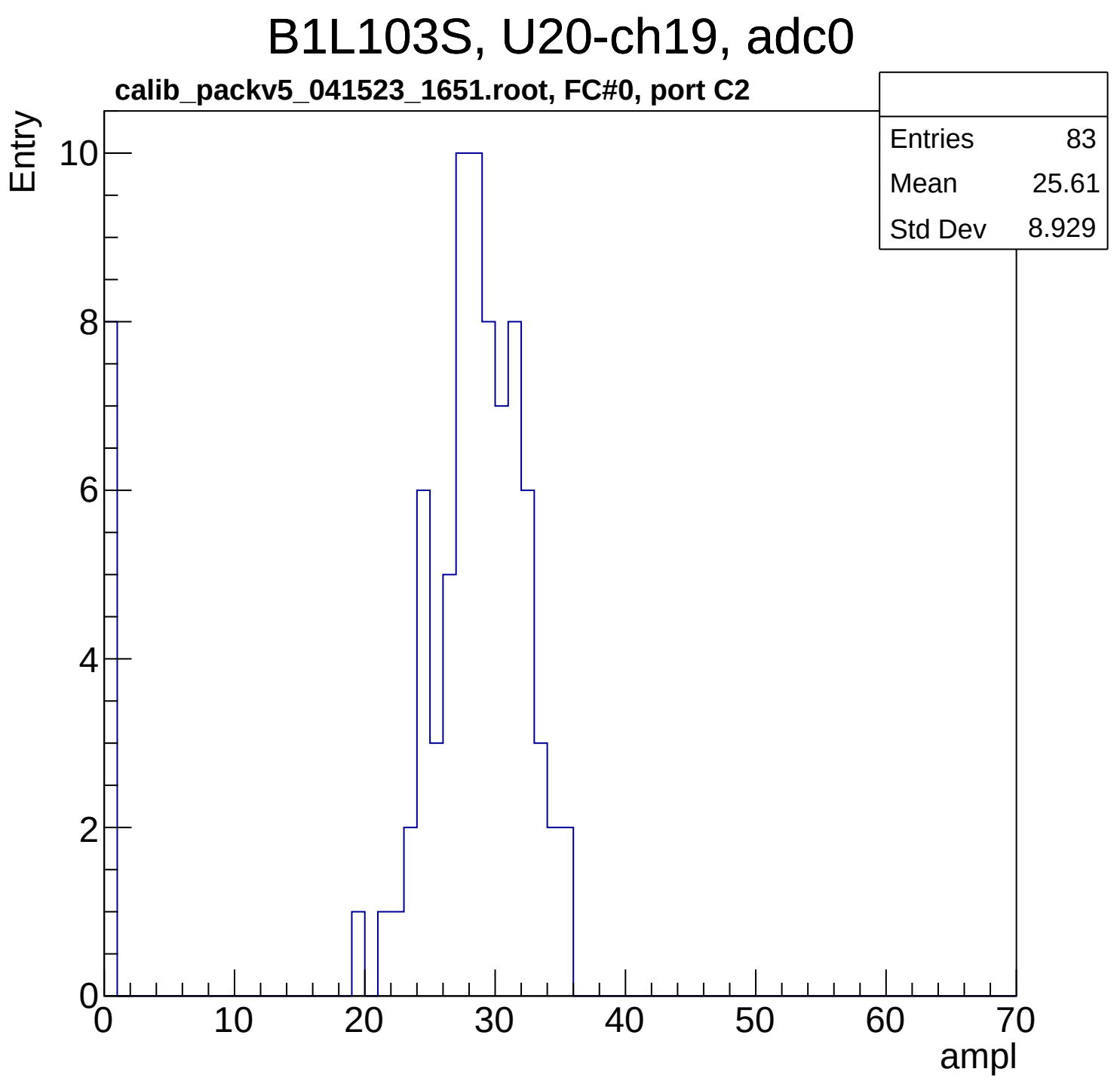
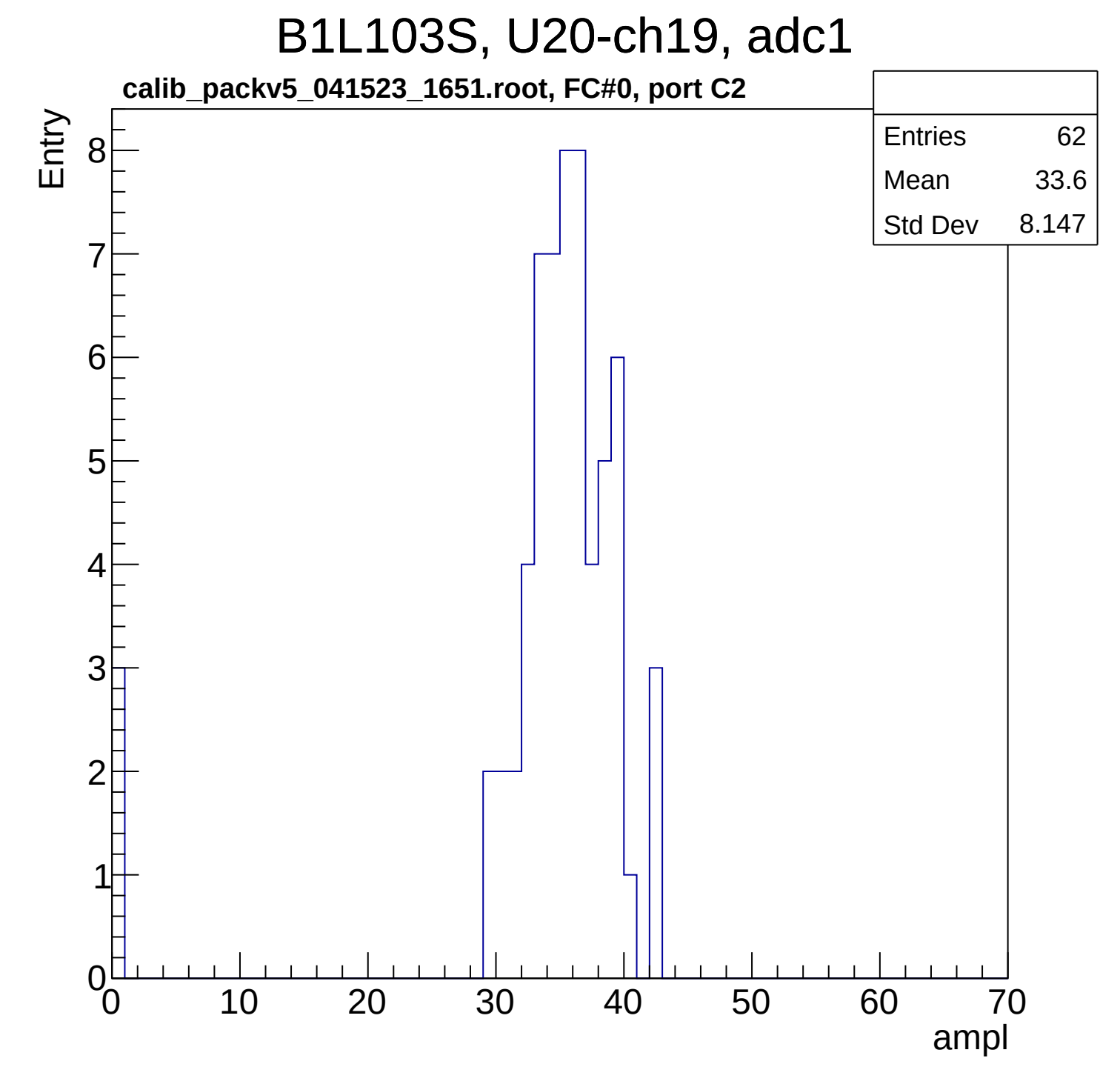
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U20-ch18, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch19, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 25.61
Std Dev 8.929
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch19, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 33.6
Std Dev 8.147
Entry
ampl
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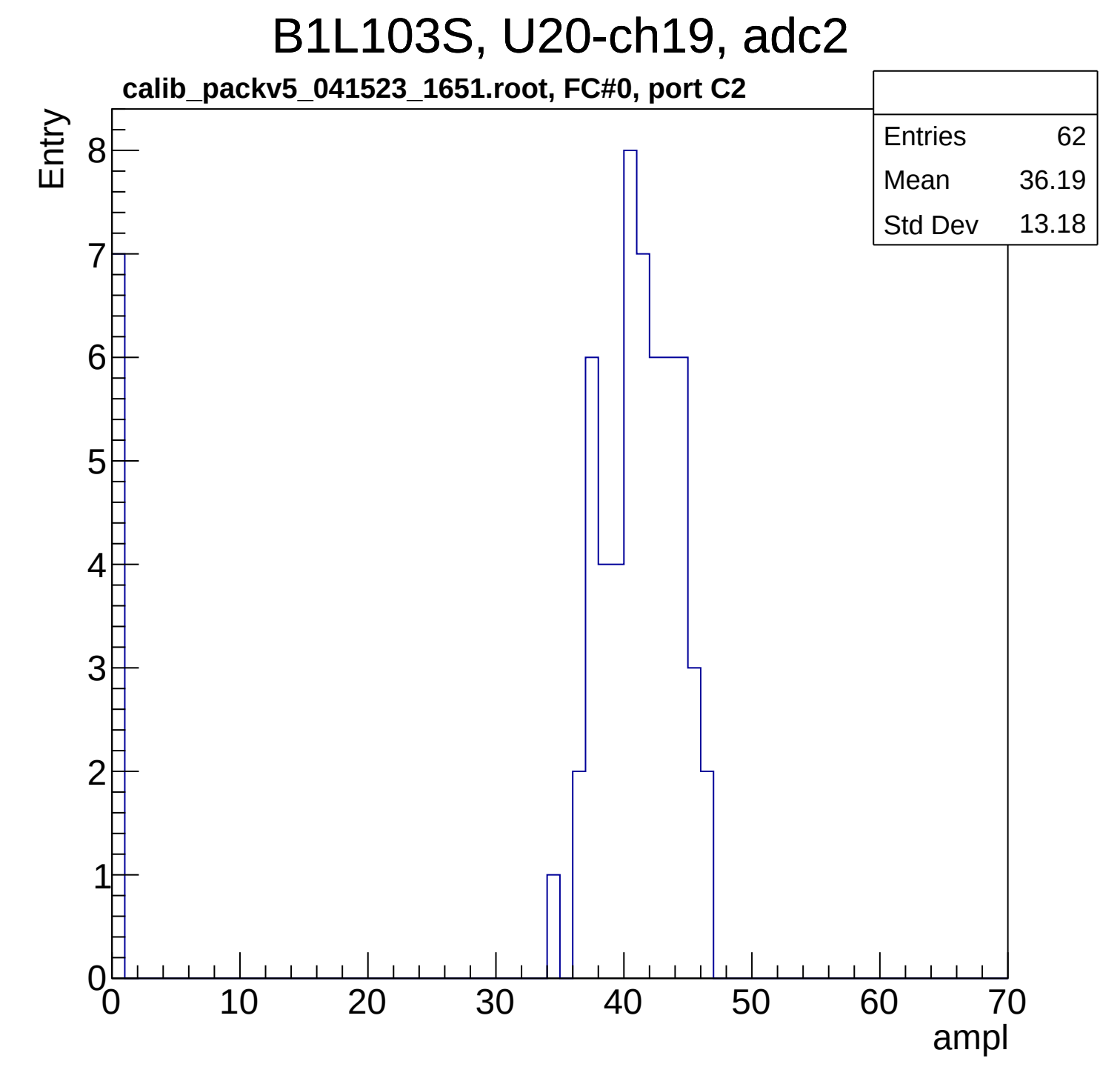
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch19, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 36.19
Std Dev 13.18
Entry
ampl
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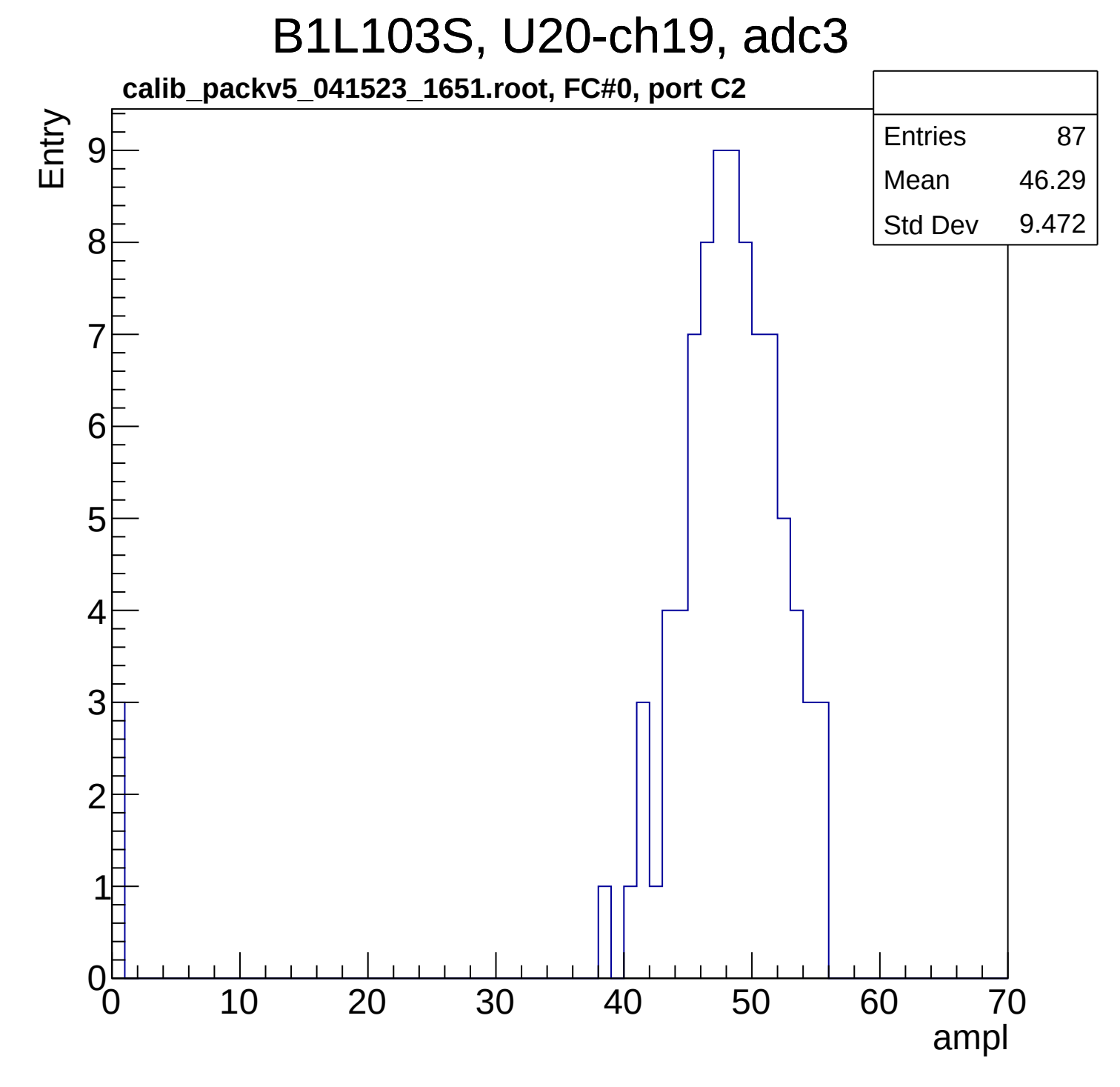
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch19, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 46.29
Std Dev 9.472
Entry
ampl
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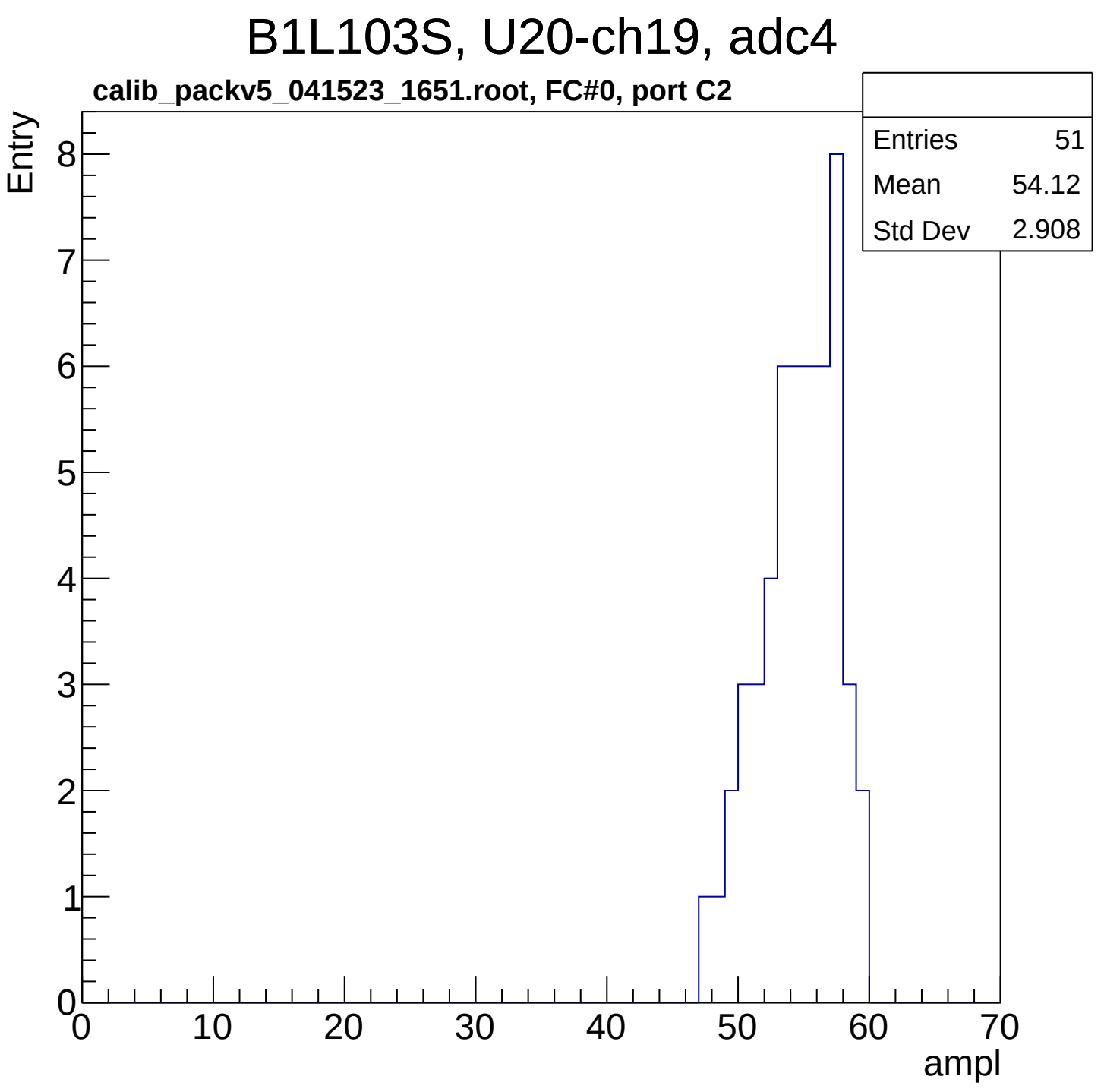
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch19, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 54.12
Std Dev 2.908
Entry
ampl
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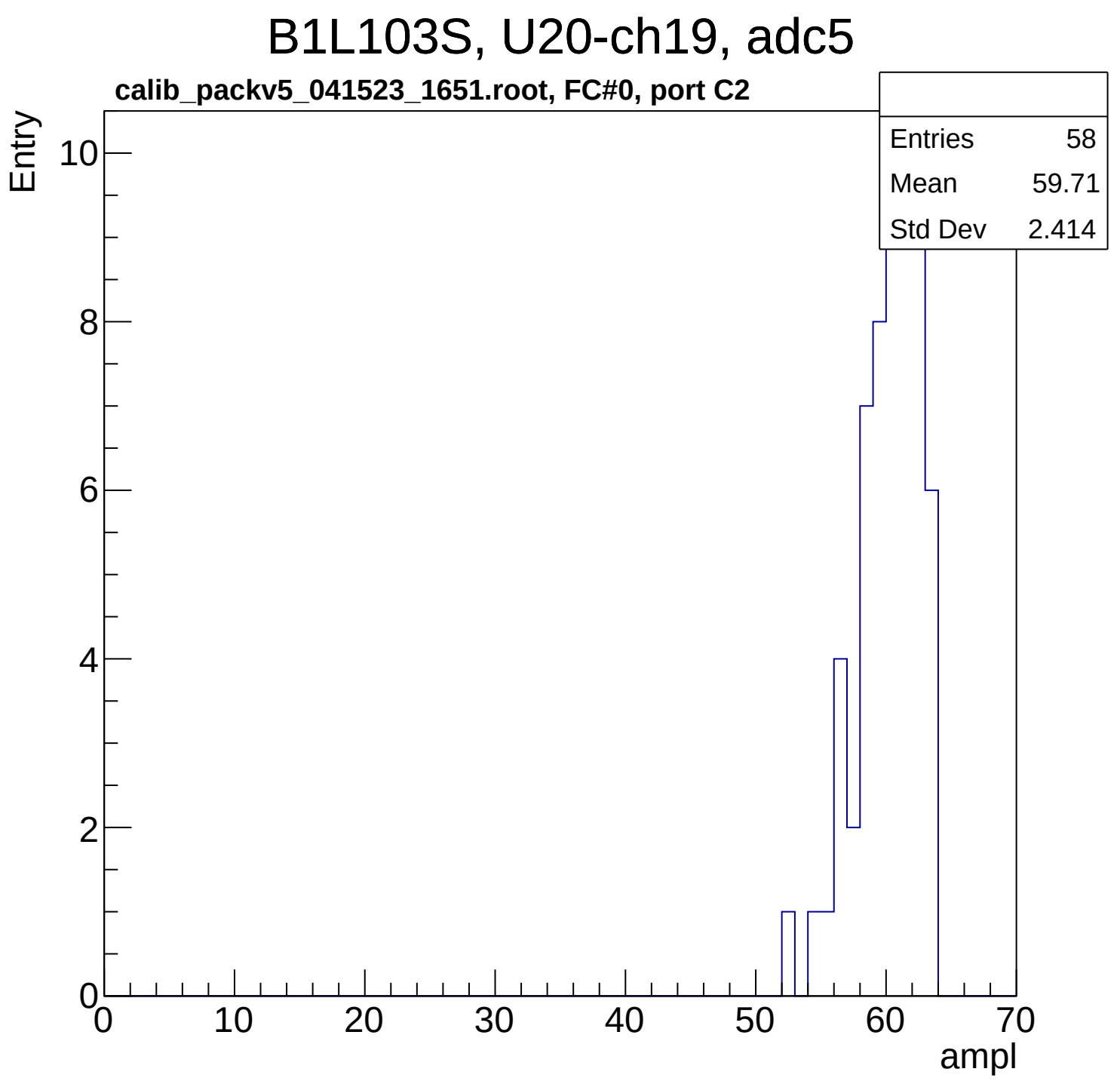
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch19, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 59.71
Std Dev 2.414
Entry
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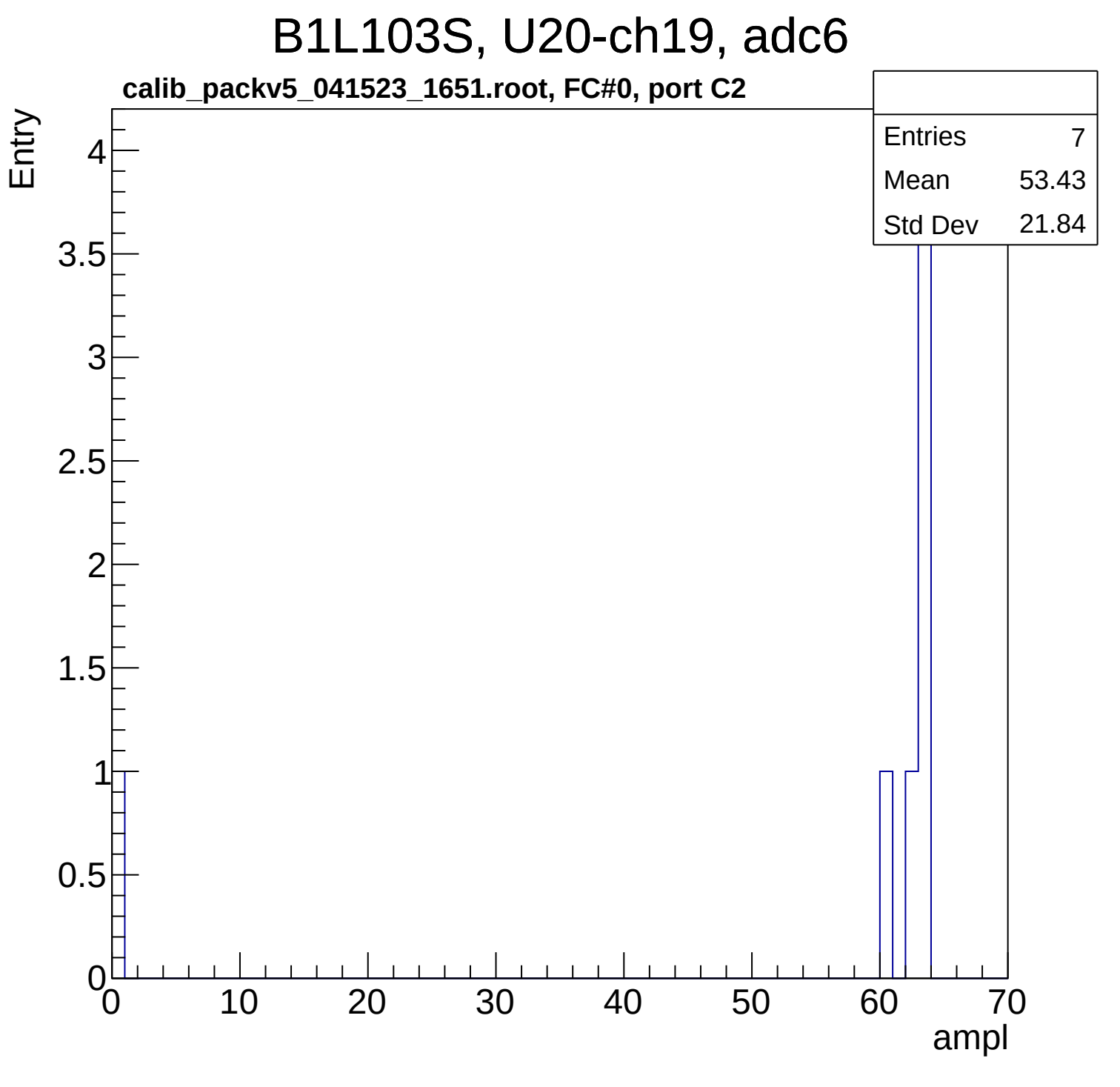
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch19, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 53.43
Std Dev 21.84
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
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60
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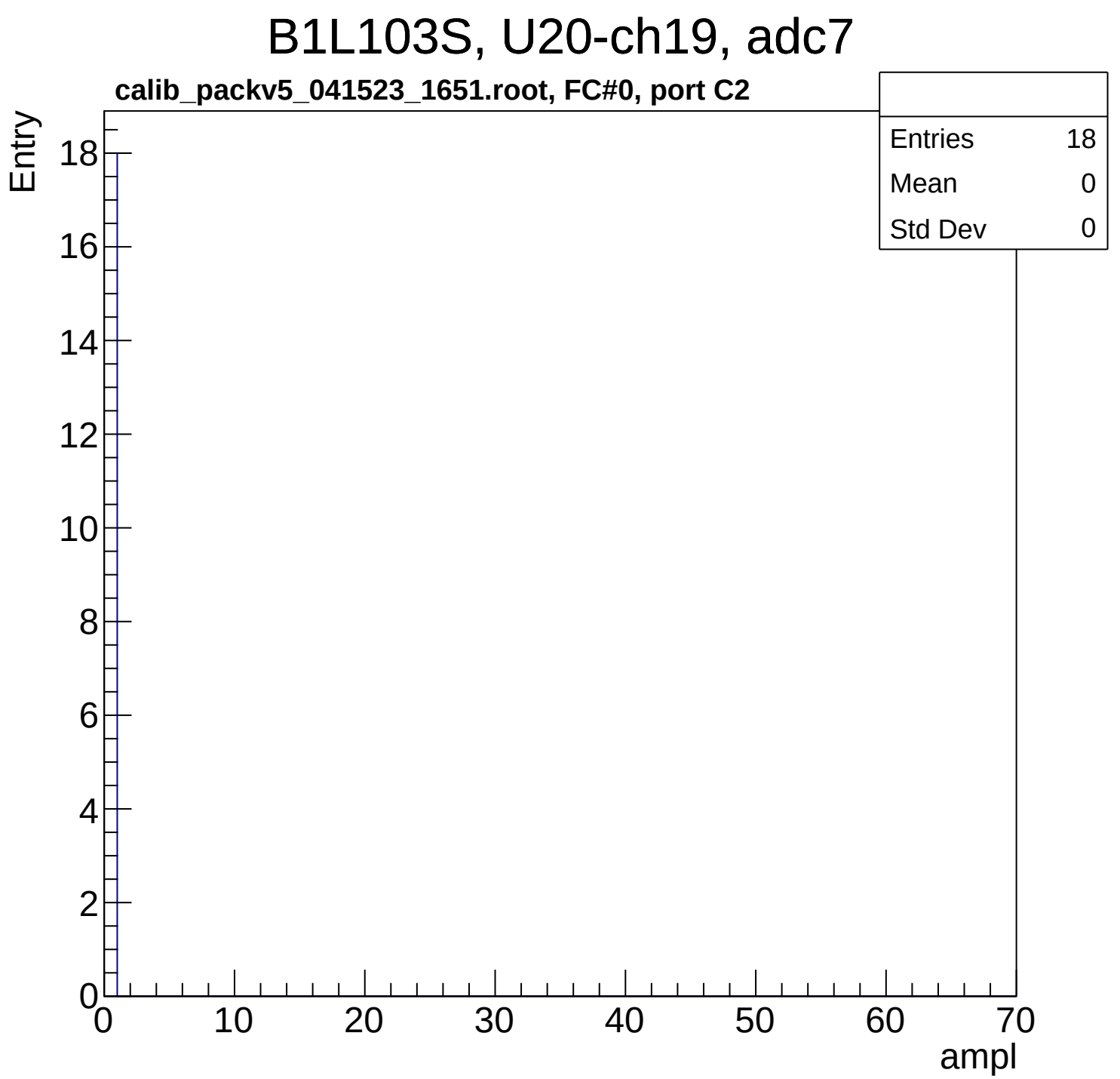
B1L103S, U20-ch19, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
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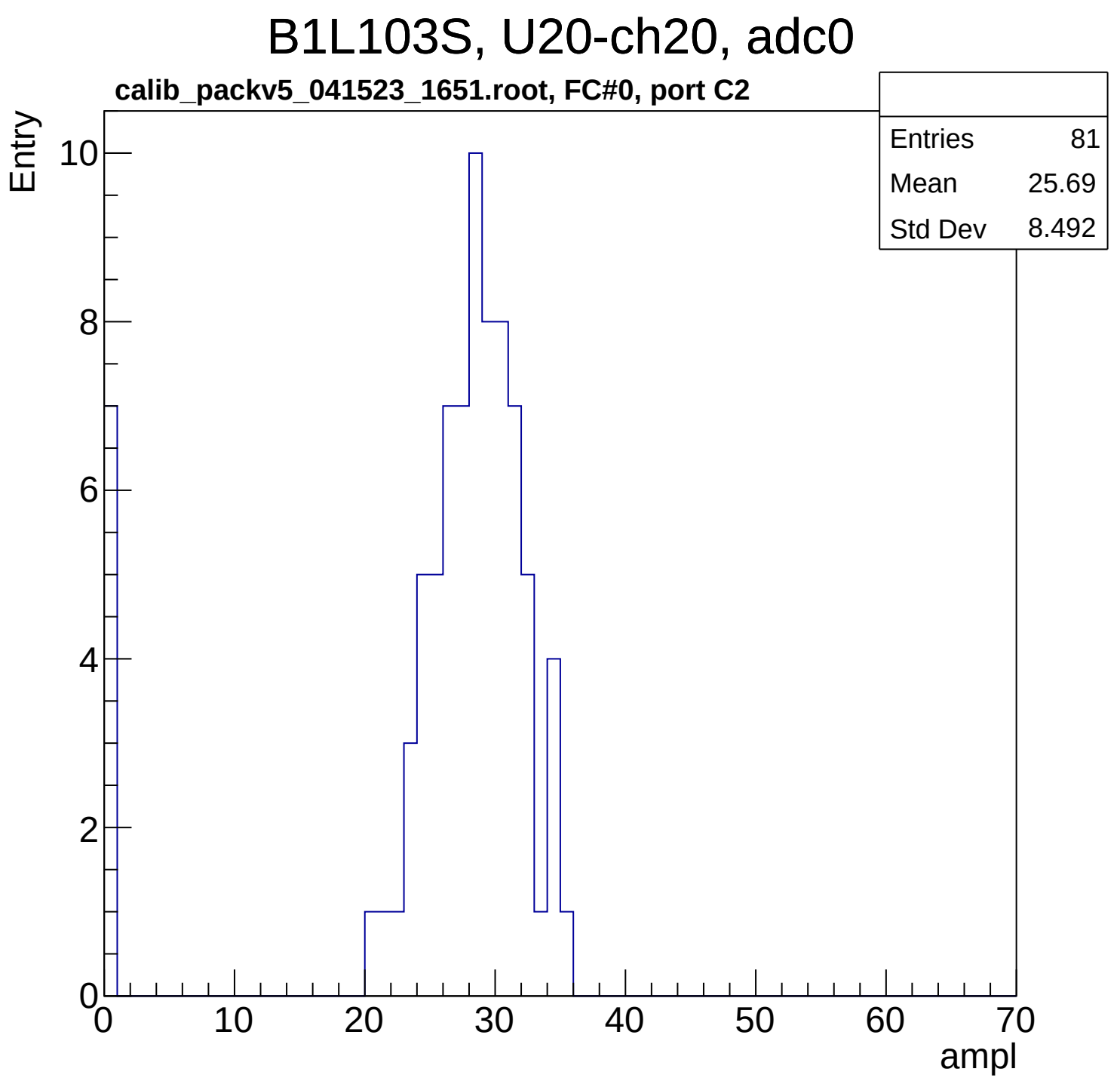
50
60
70
ampl


B1L103S, U20-ch20, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 25.69
Std Dev 8.492
Entry
ampl
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2
4
6
8
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0
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40
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60
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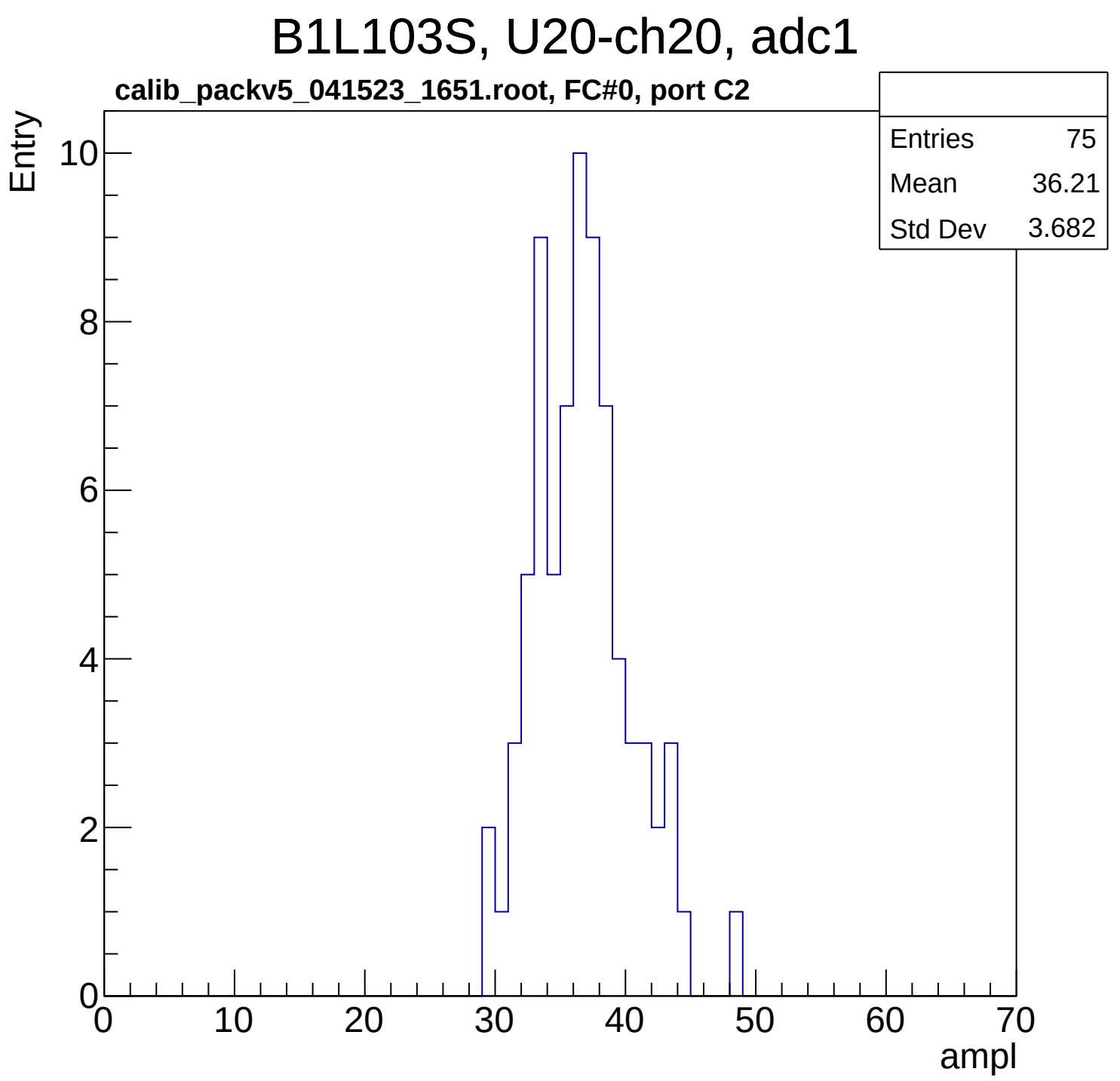
B1L103S, U20-ch20, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 36.21
Std Dev 3.682
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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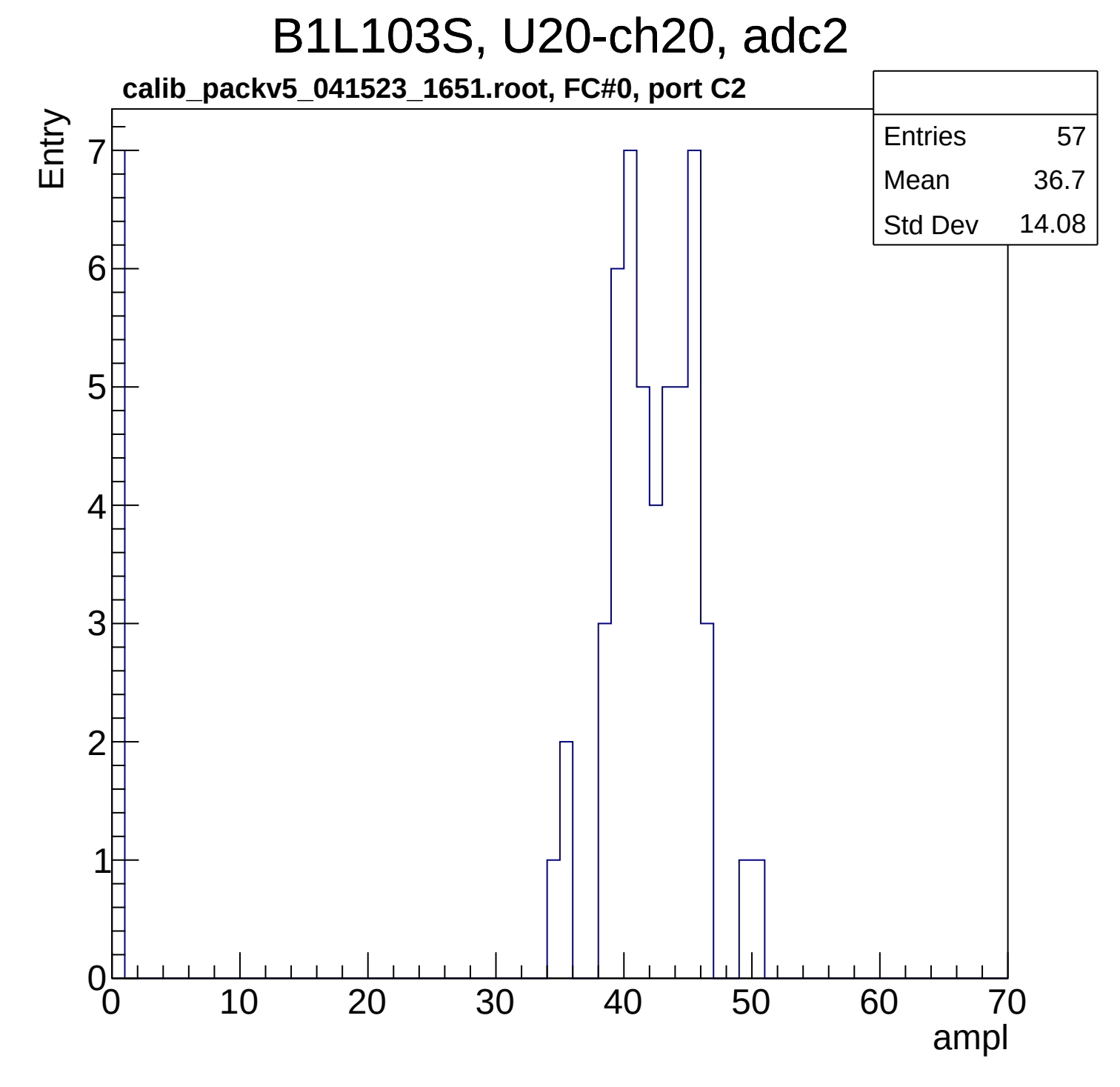
B1L103S, U20-ch20, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 36.7
Std Dev 14.08
Entry
ampl
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2
3
4
5
6
7
0
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20
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40
50
60
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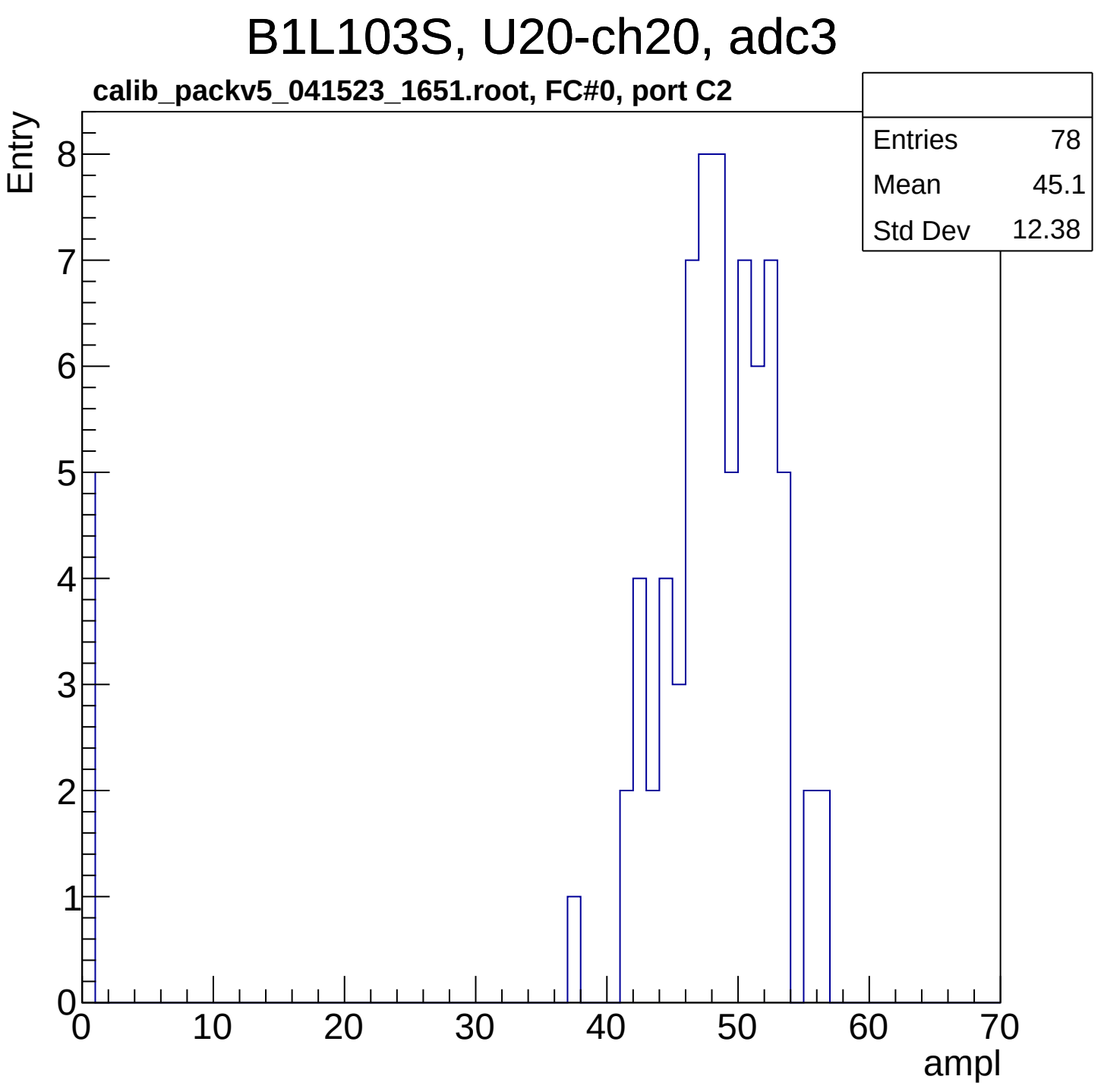
B1L103S, U20-ch20, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 45.1
Std Dev 12.38
Entry
ampl
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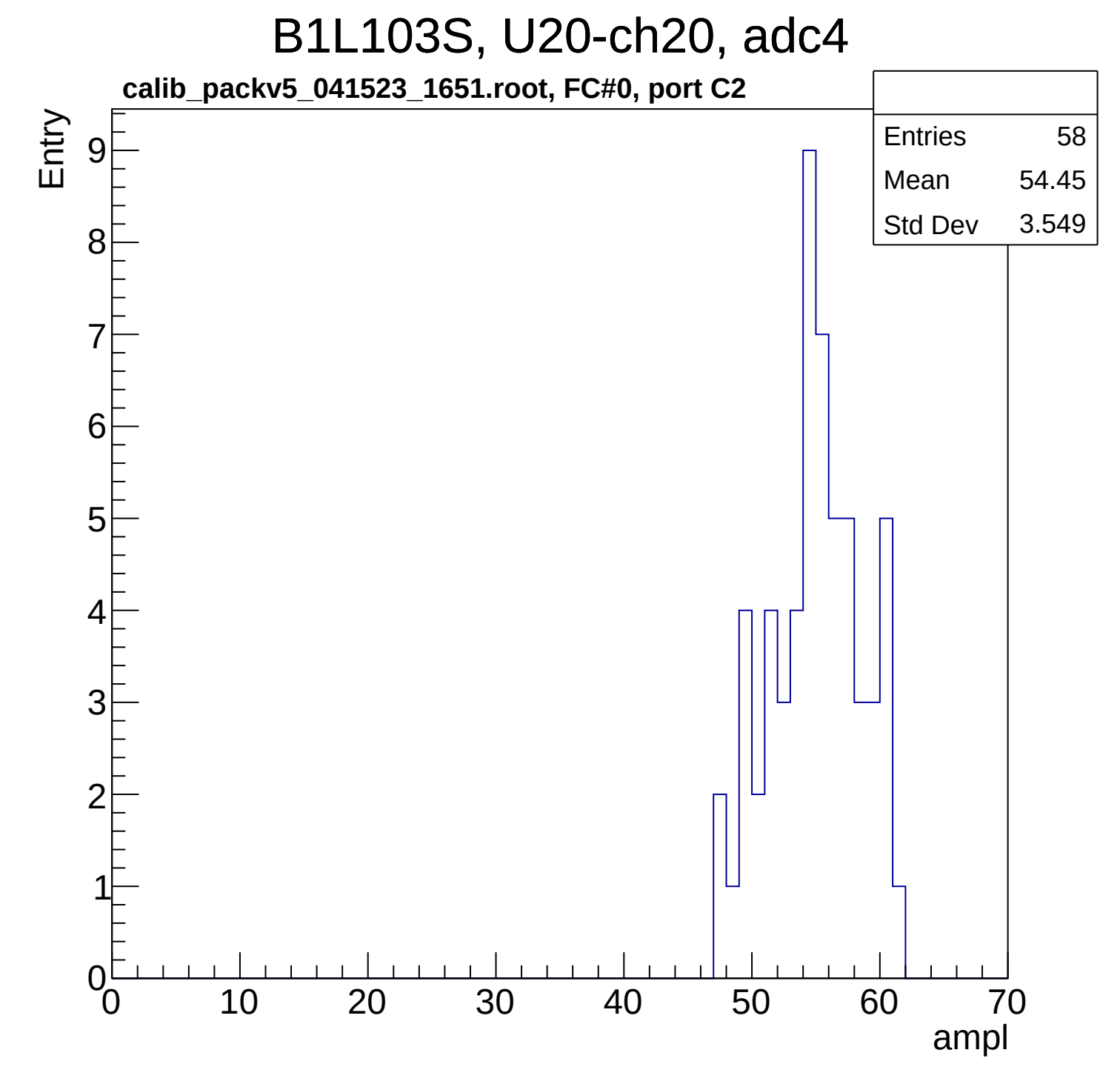
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch20, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 54.45
Std Dev 3.549
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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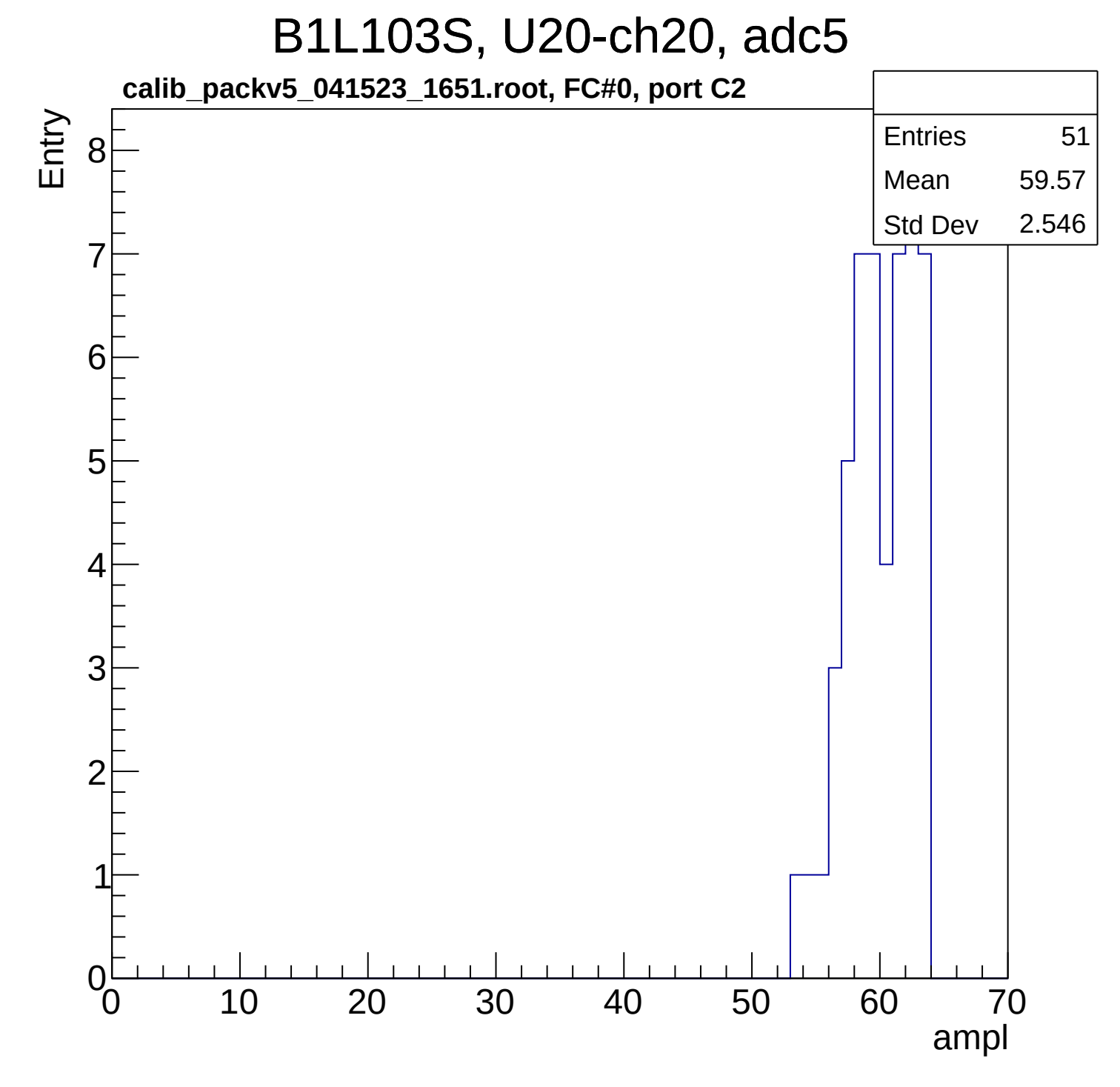
B1L103S, U20-ch20, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 59.57
Std Dev 2.546
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
50
60
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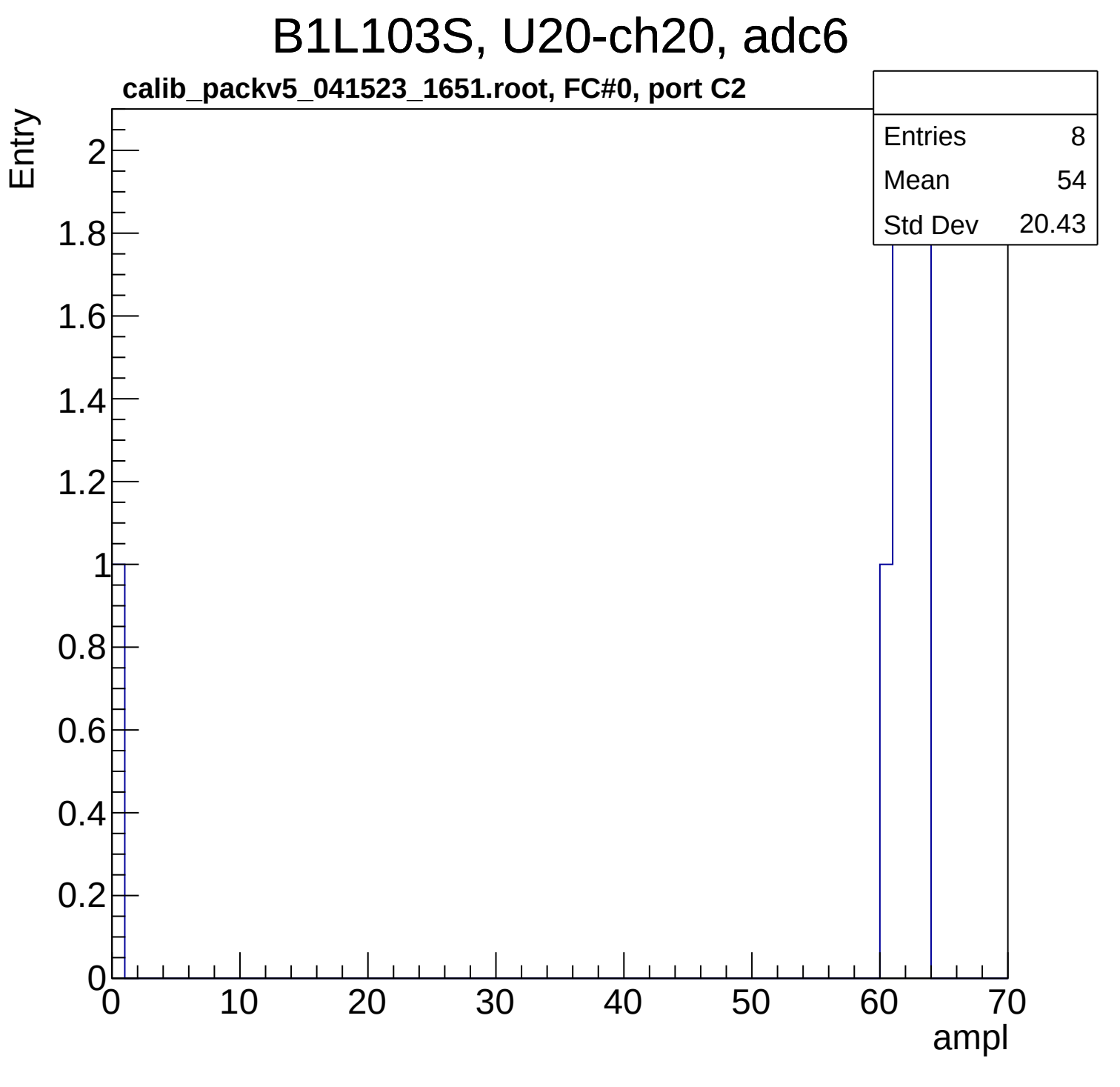
B1L103S, U20-ch20, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 54
Std Dev 20.43
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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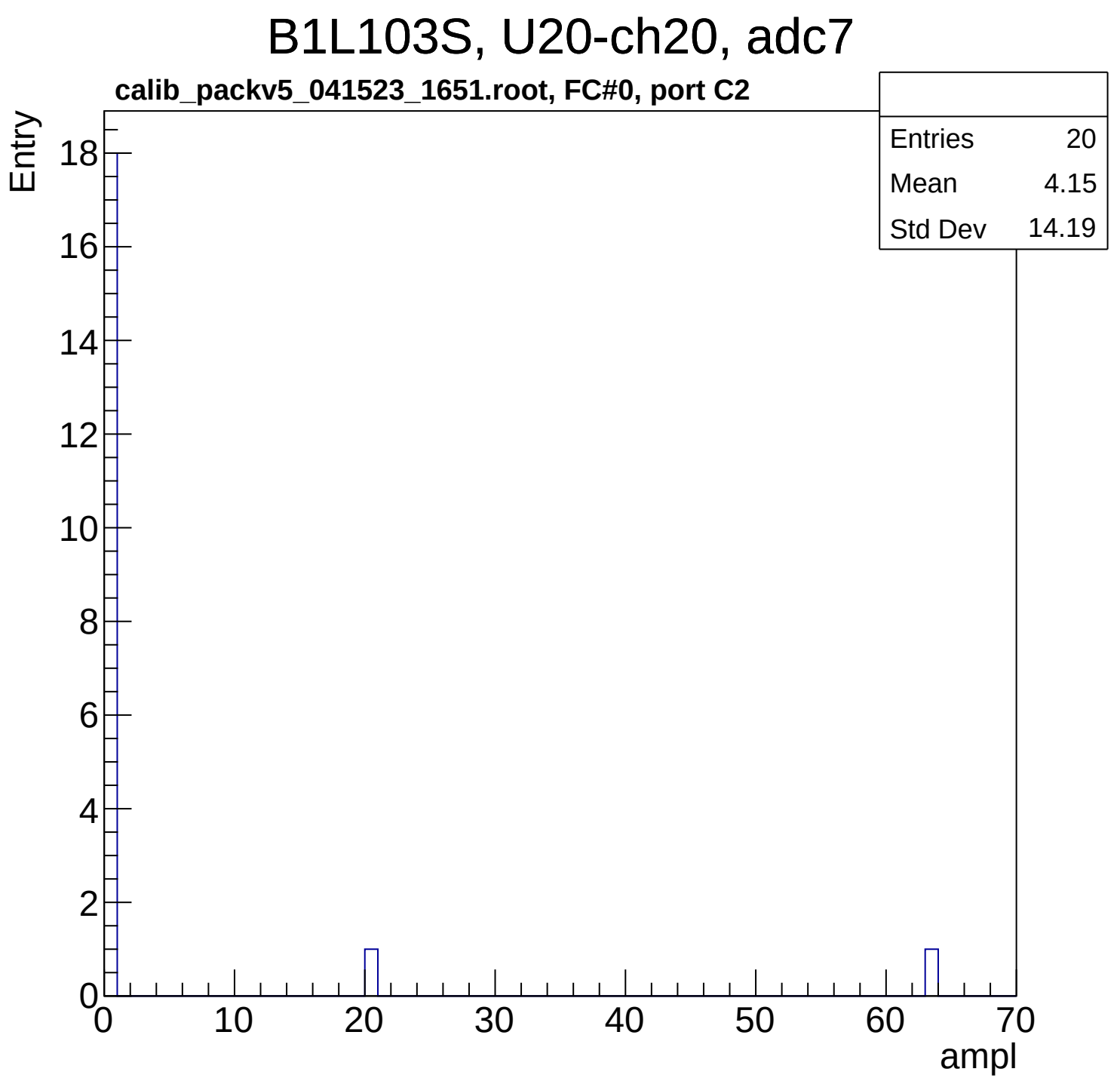
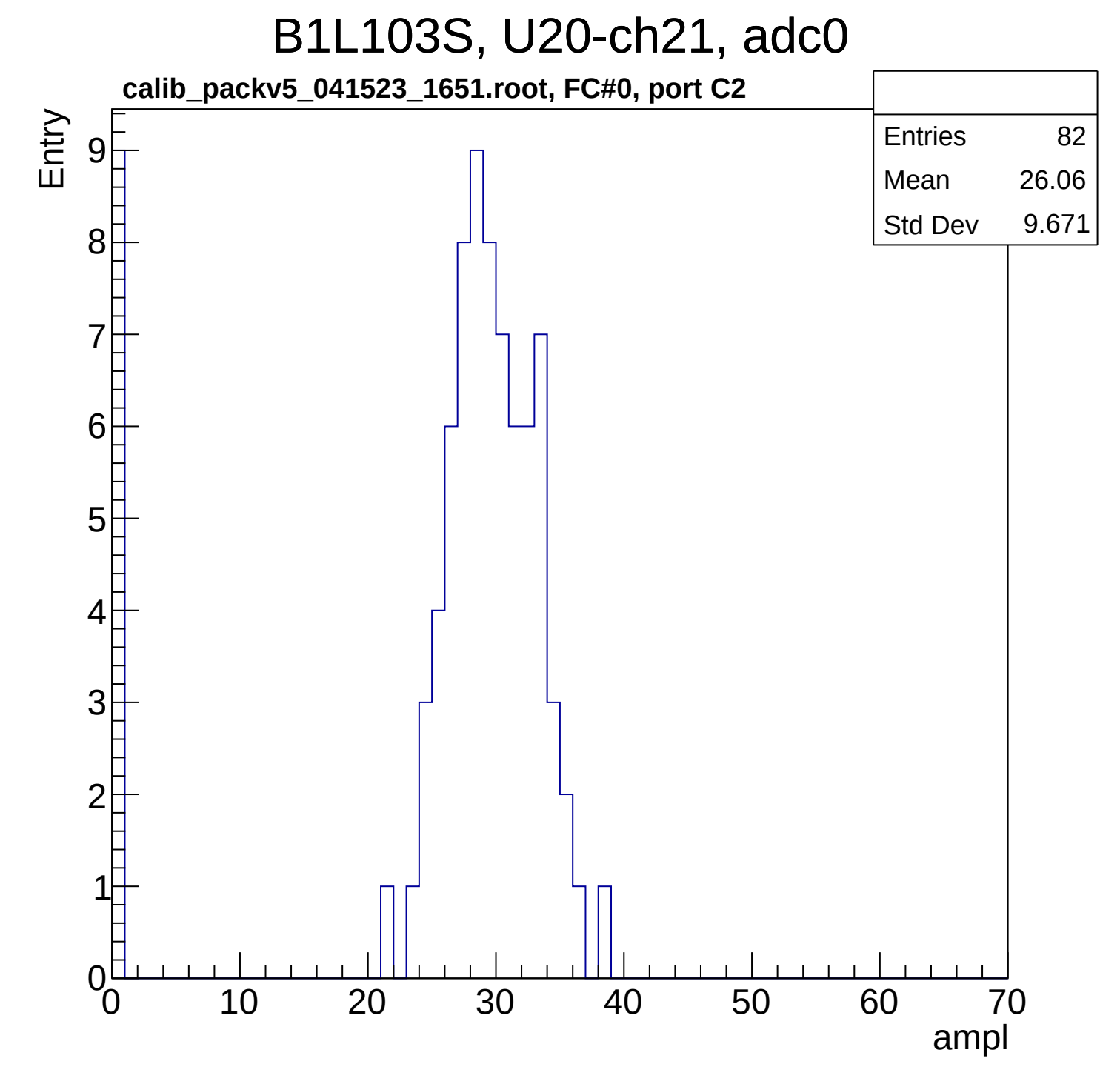

B1L103S, U20-ch20, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4.15
Std Dev 14.19
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch21, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 26.06
Std Dev 9.671
Entry
ampl
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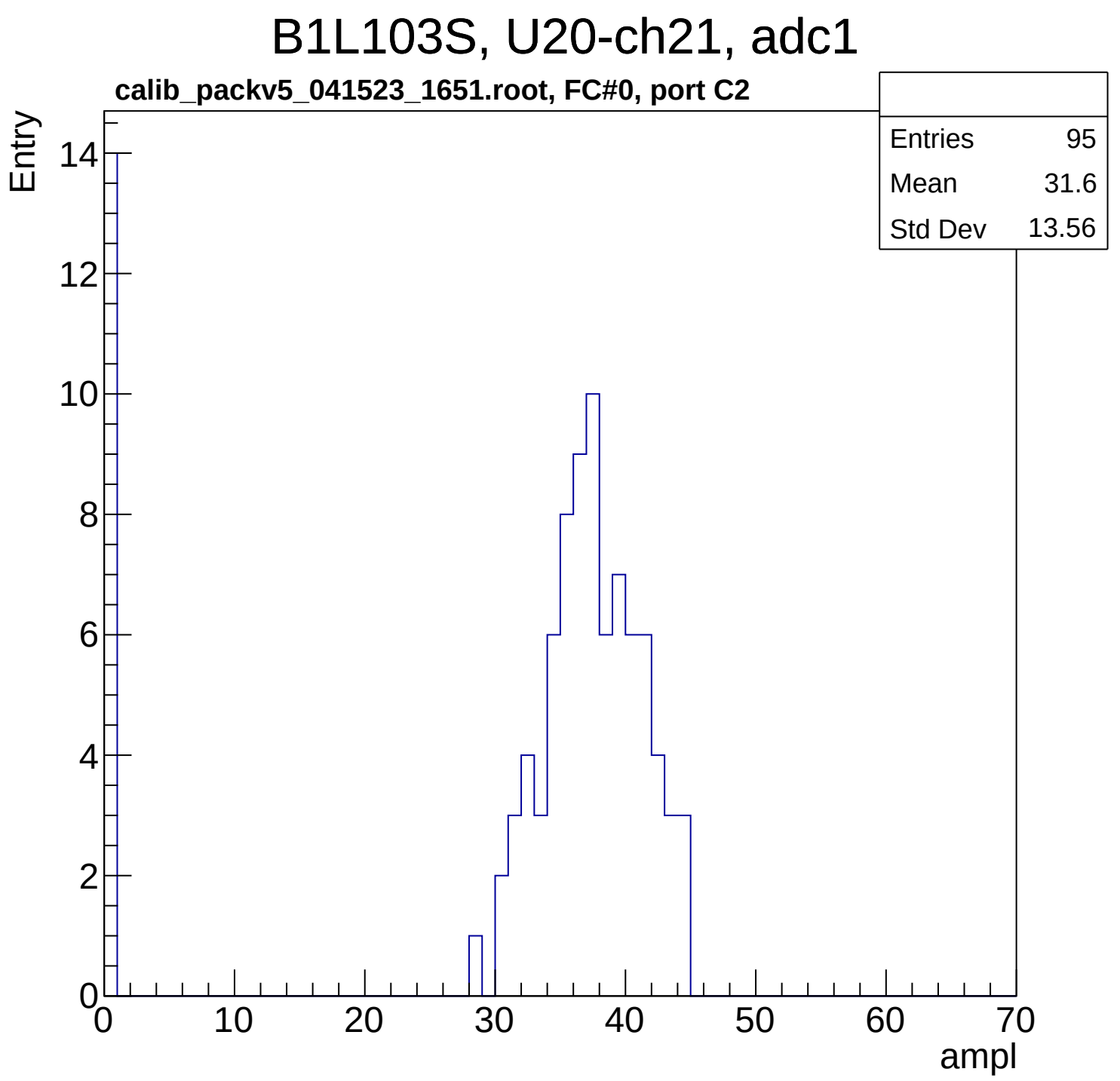
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch21, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 31.6
Std Dev 13.56
Entry
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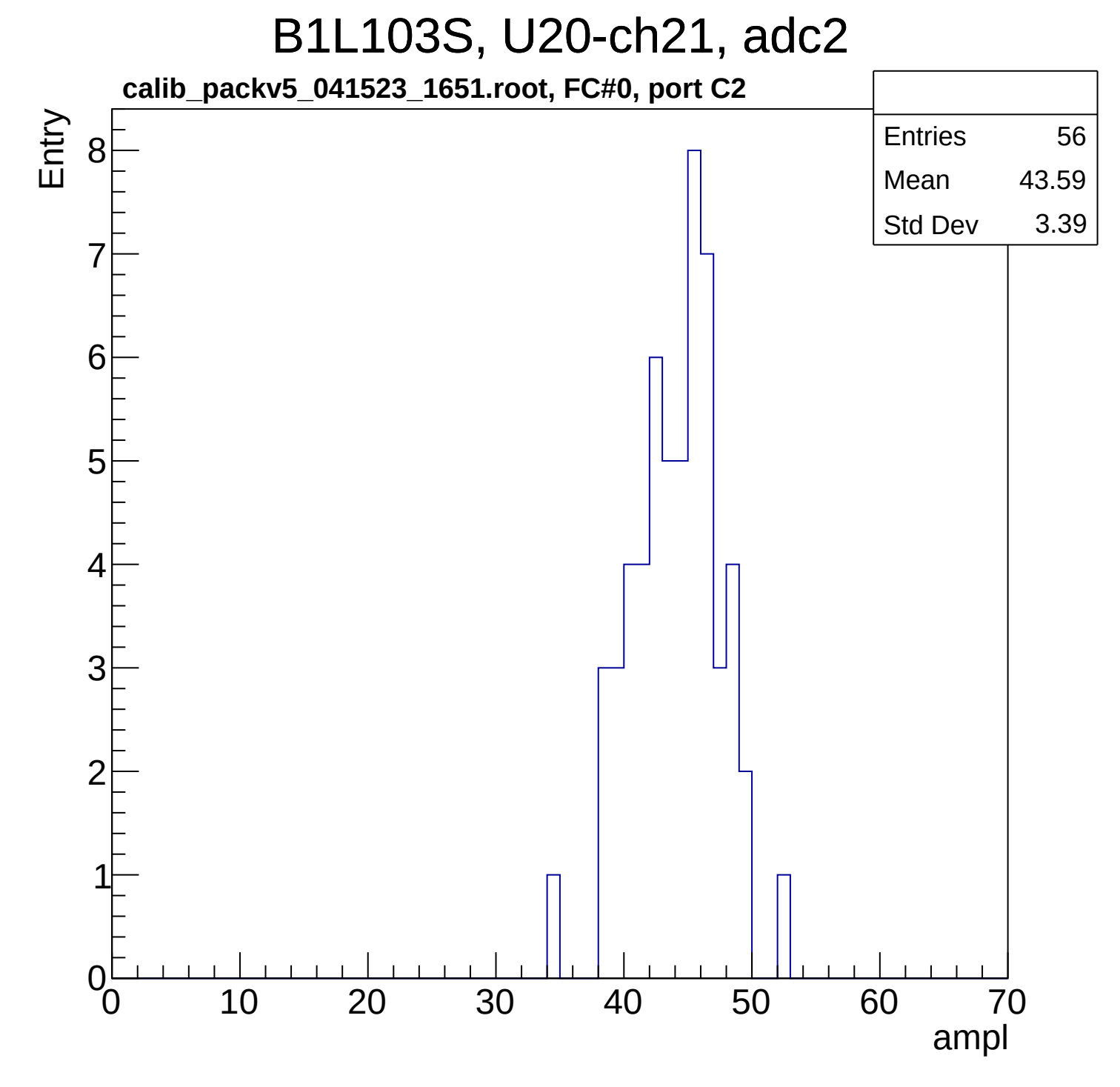
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch21, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 43.59
Std Dev 3.39
Entry
ampl
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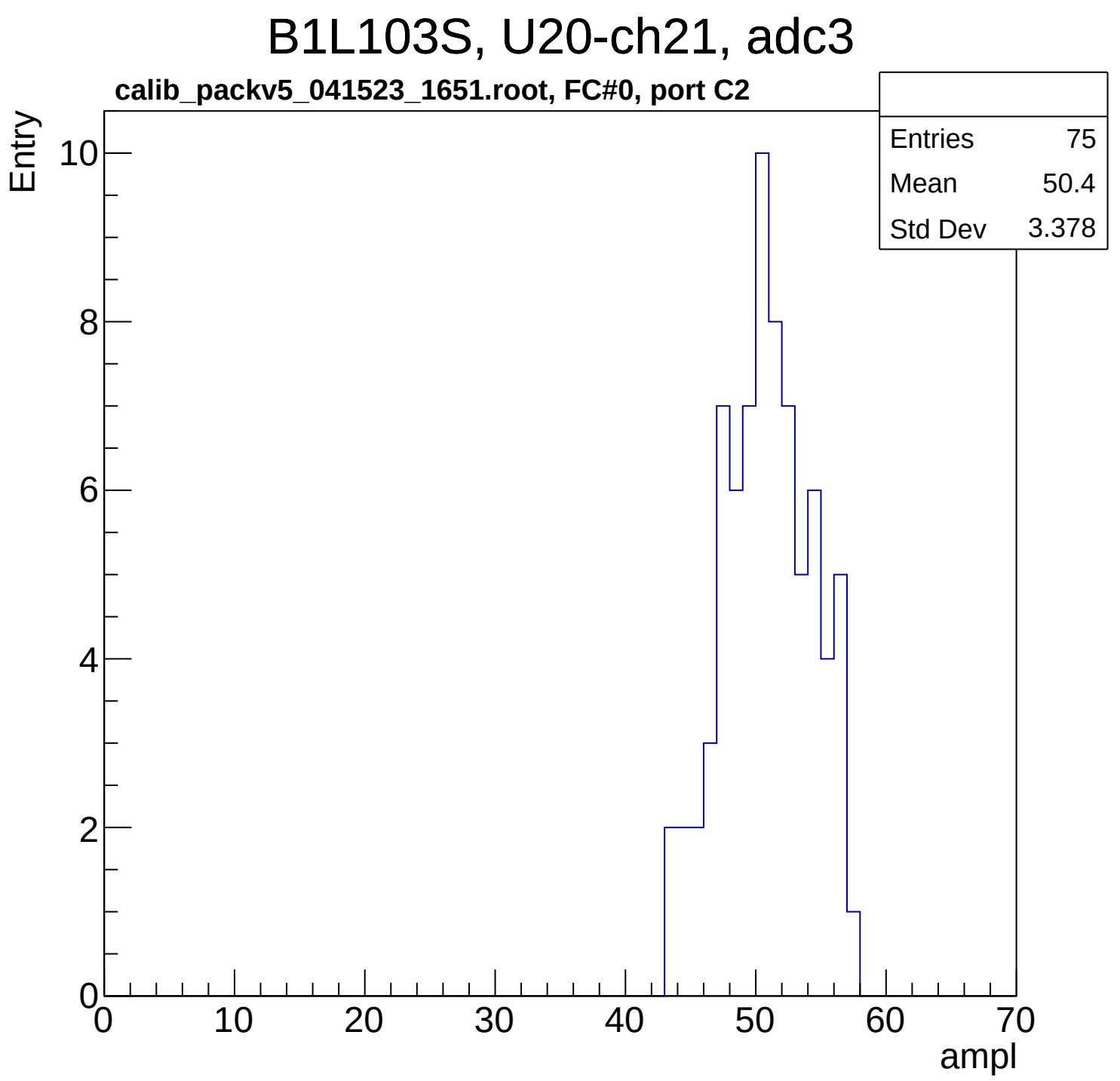
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch21, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 50.4
Std Dev 3.378
Entry
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2
4
6
8
10
0
10
20
30
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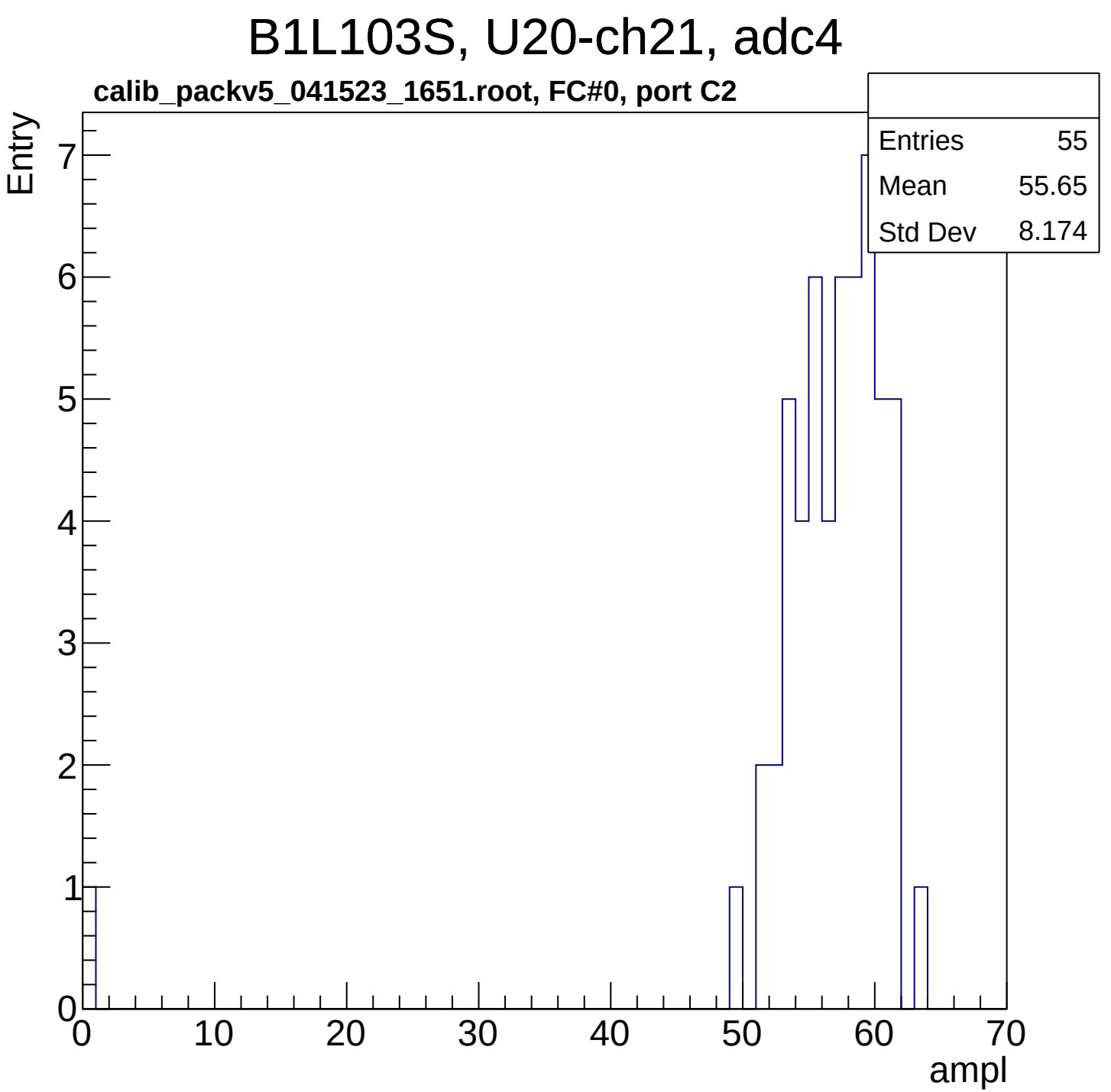
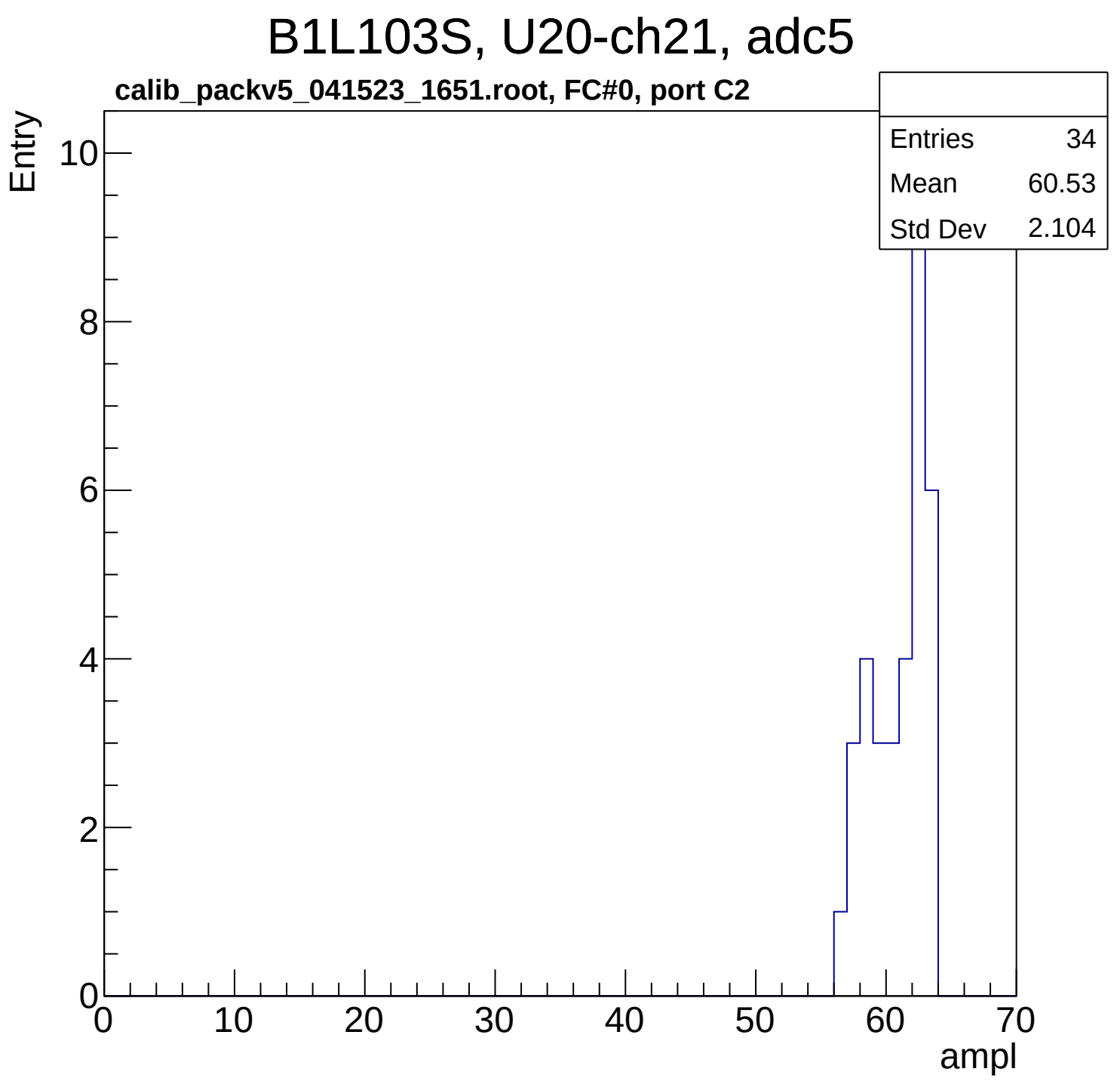
50
60
70
ampl


B1L103S, U20-ch21, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 55.65
Std Dev 8.174
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U20-ch21, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 60.53
Std Dev 2.104
Entry
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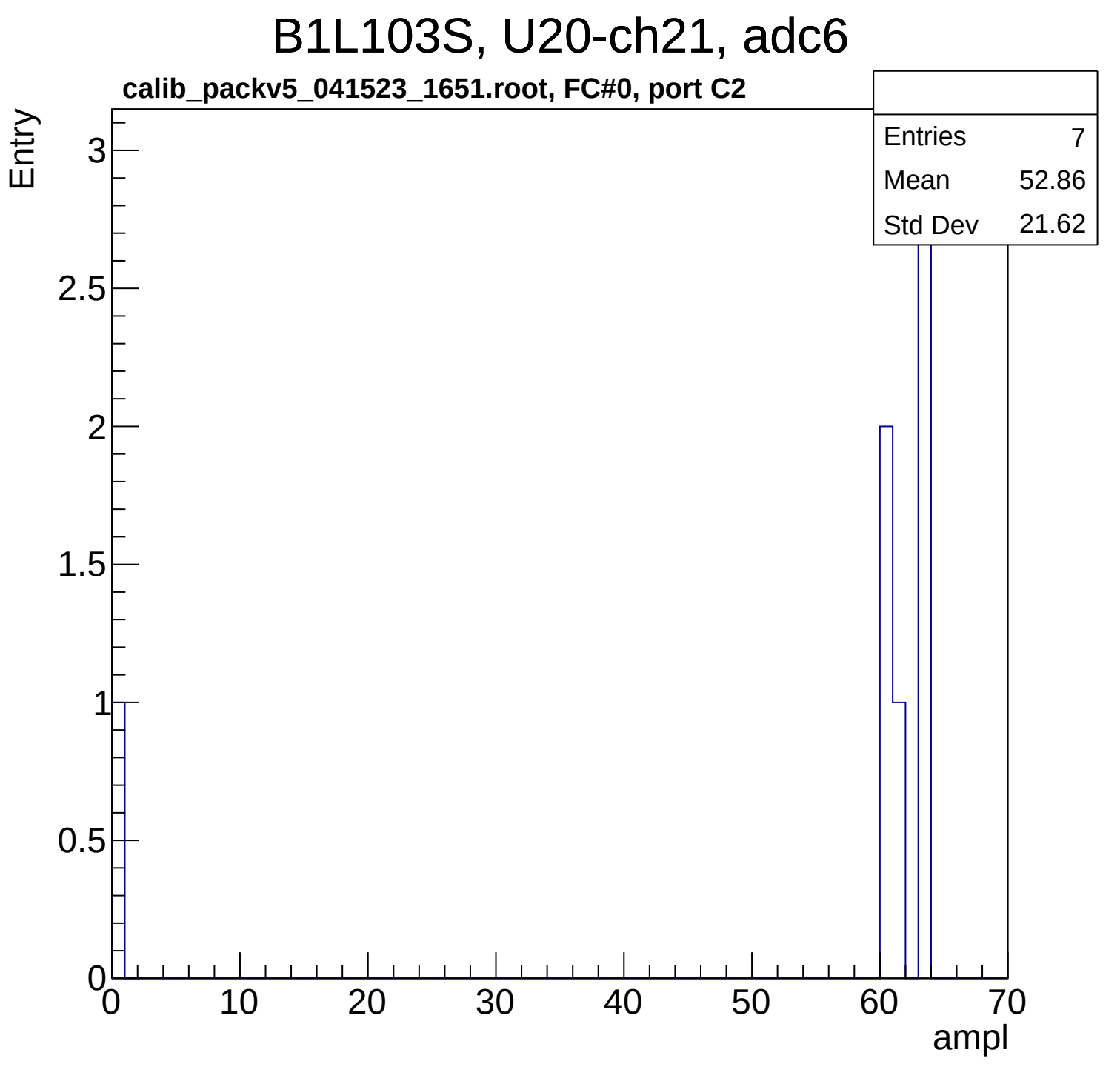
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch21, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 52.86
Std Dev 21.62
Entry
ampl
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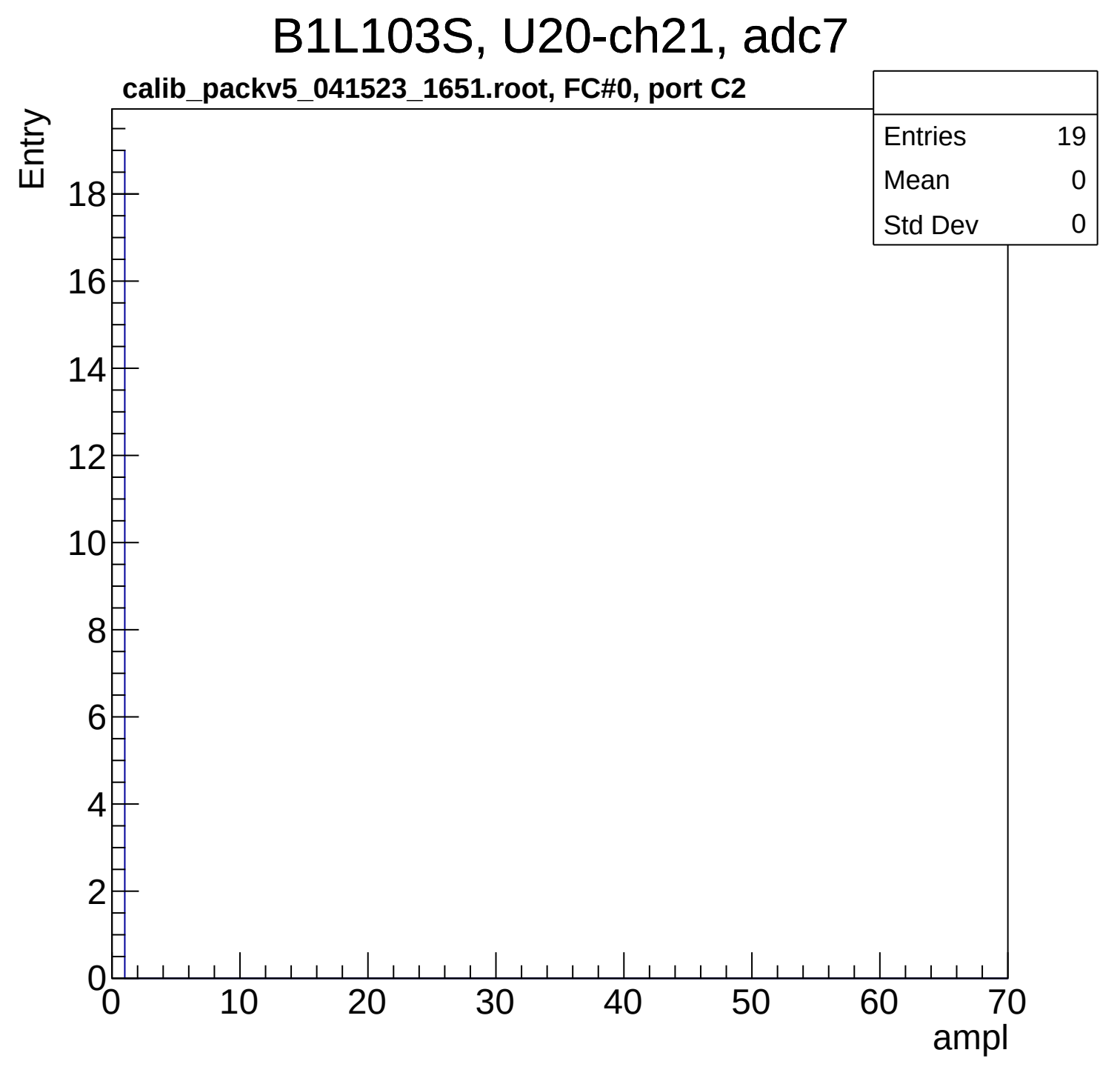
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U20-ch21, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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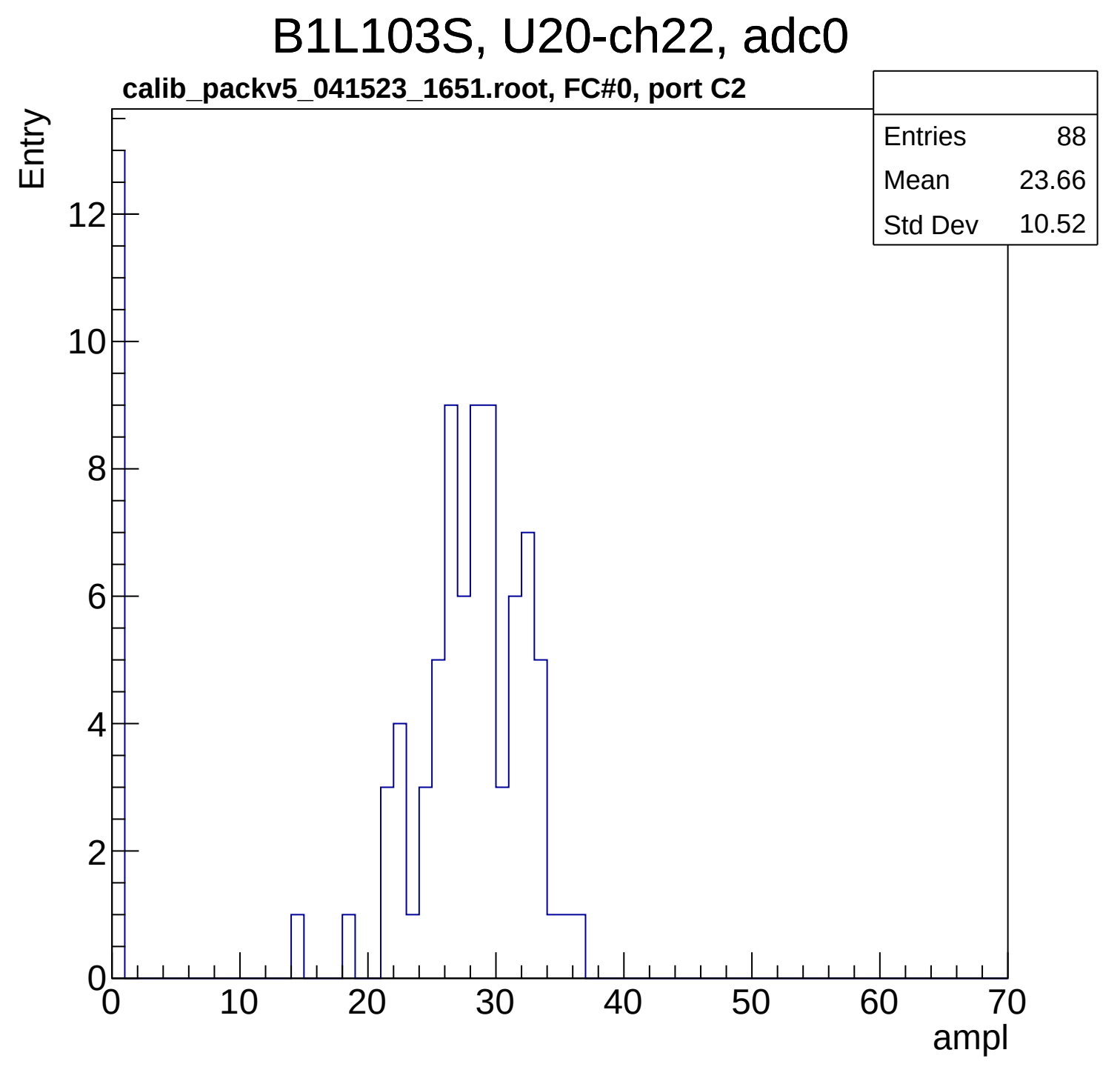
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch22, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 23.66
Std Dev 10.52
Entry
ampl
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2
4
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8
10
12
0
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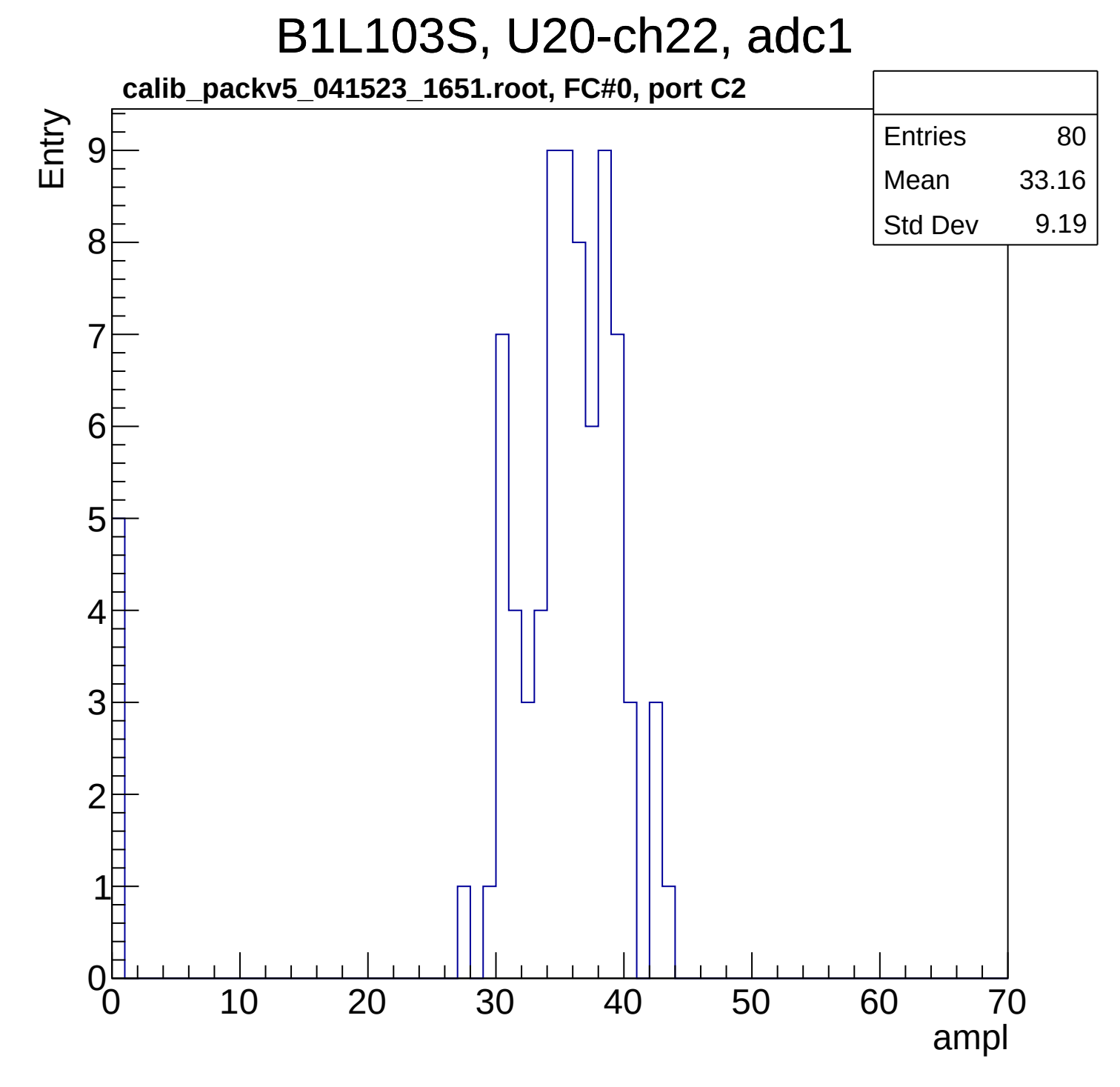
20
30
40
50
60
70


B1L103S, U20-ch22, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 33.16
Std Dev 9.19
Entry
ampl
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3
4
5
6
7
8
9
0
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20
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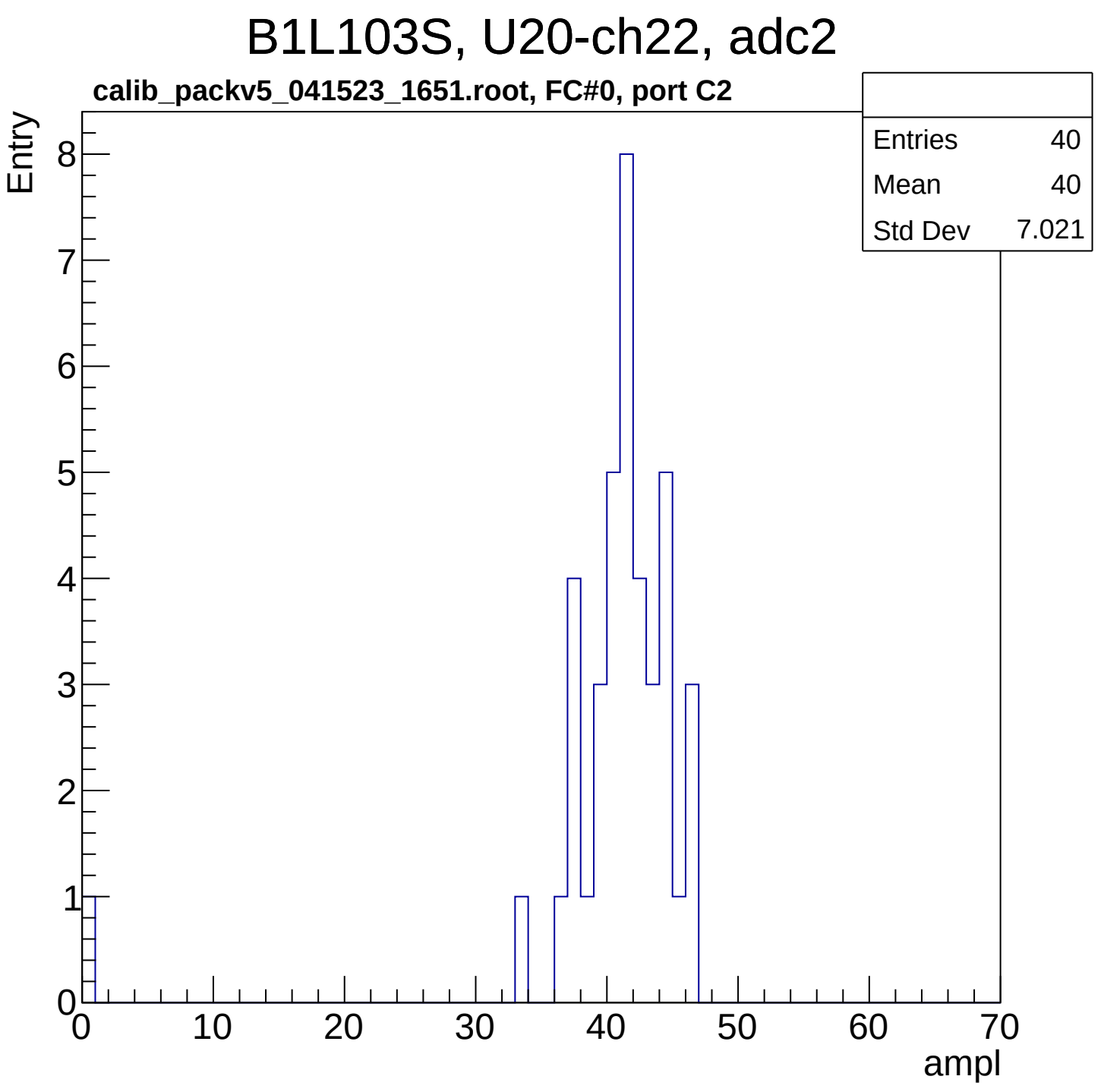
40
50
60
70


B1L103S, U20-ch22, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 40
Std Dev 7.021
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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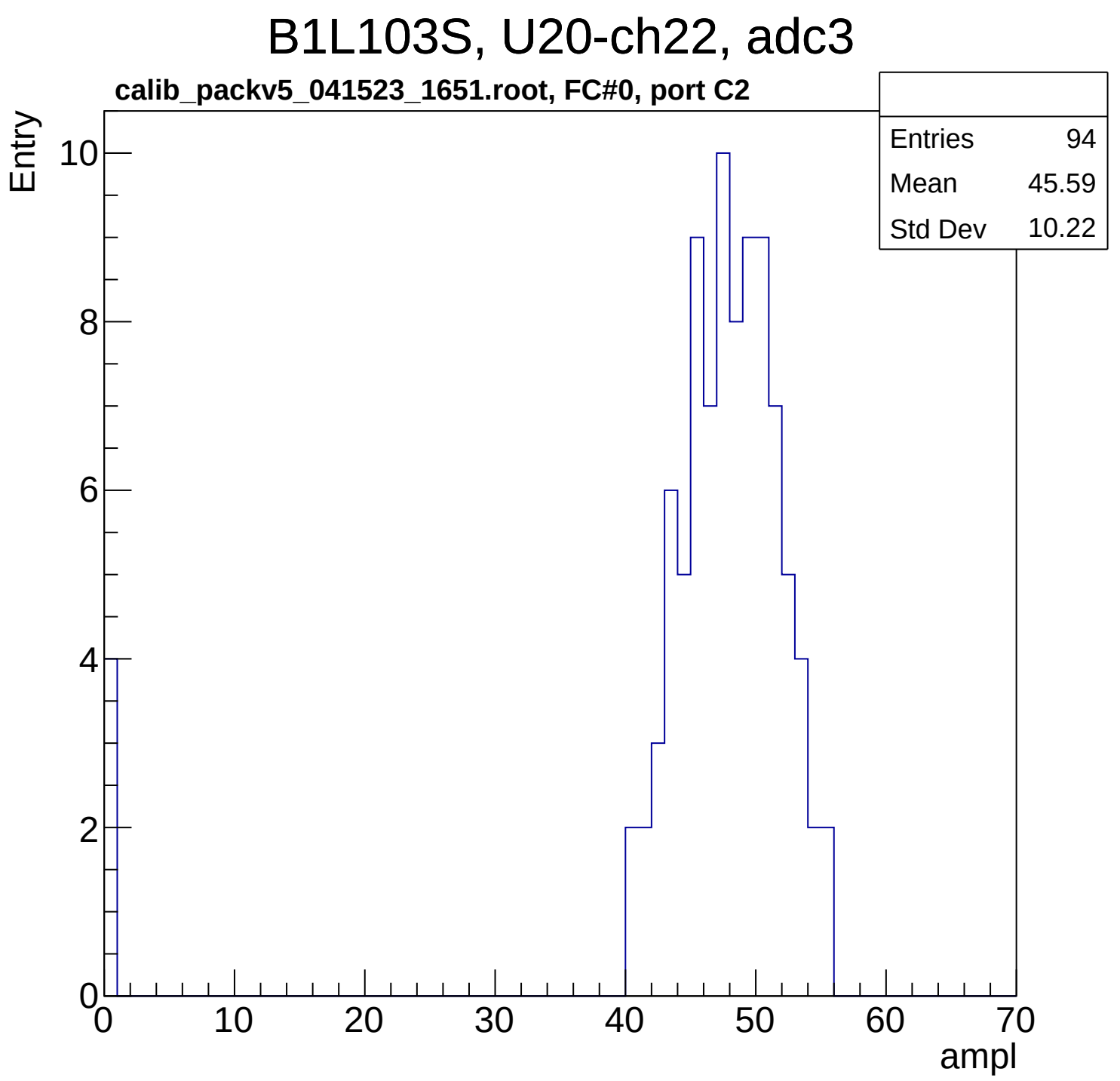
40
50
60
70


B1L103S, U20-ch22, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 45.59
Std Dev 10.22
Entry
ampl
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4
6
8
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0
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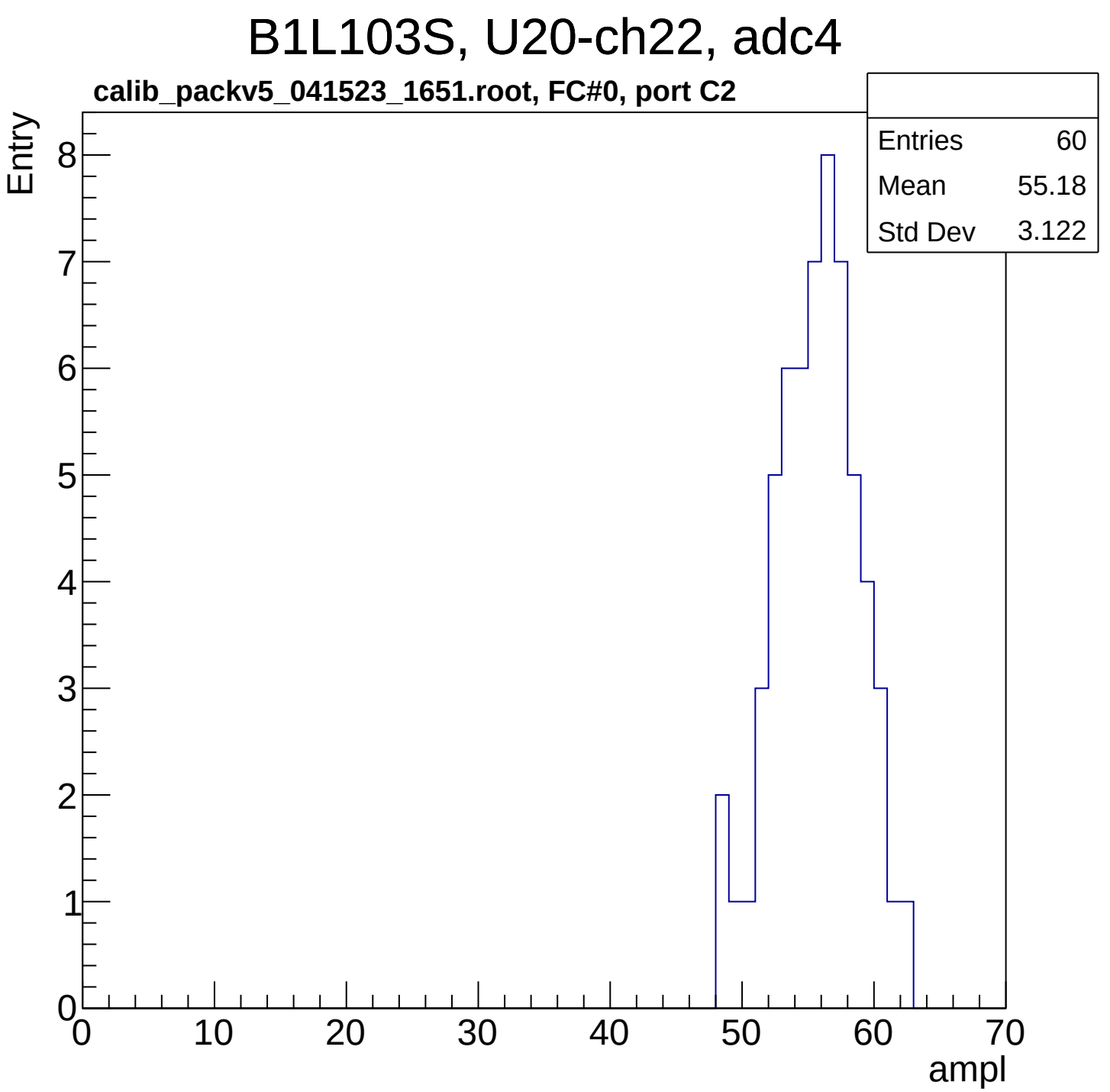
20
30
40
50
60
70


B1L103S, U20-ch22, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 55.18
Std Dev 3.122
Entry
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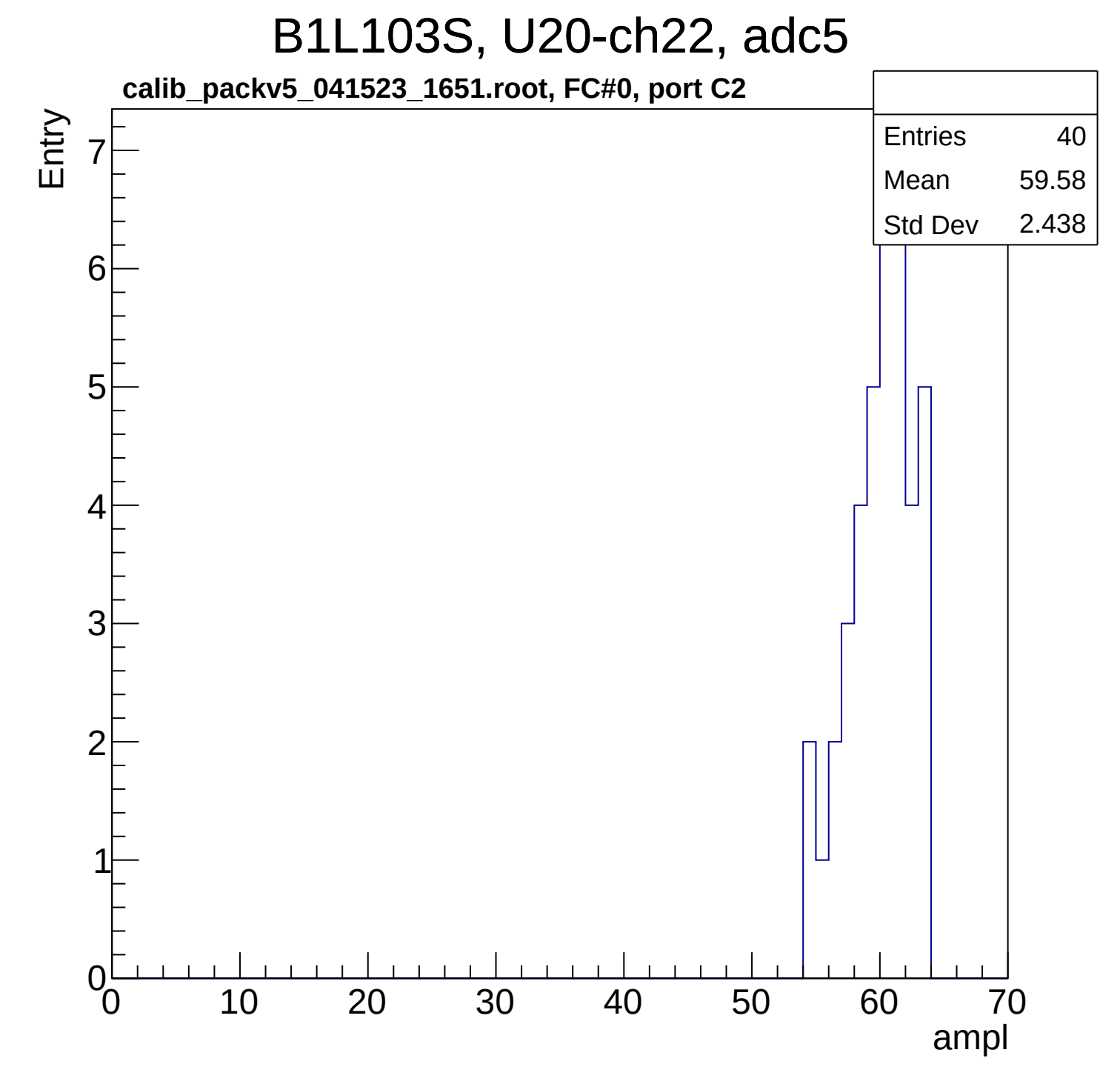
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch22, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 59.58
Std Dev 2.438
Entry
ampl
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1
2
3
4
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6
7
0
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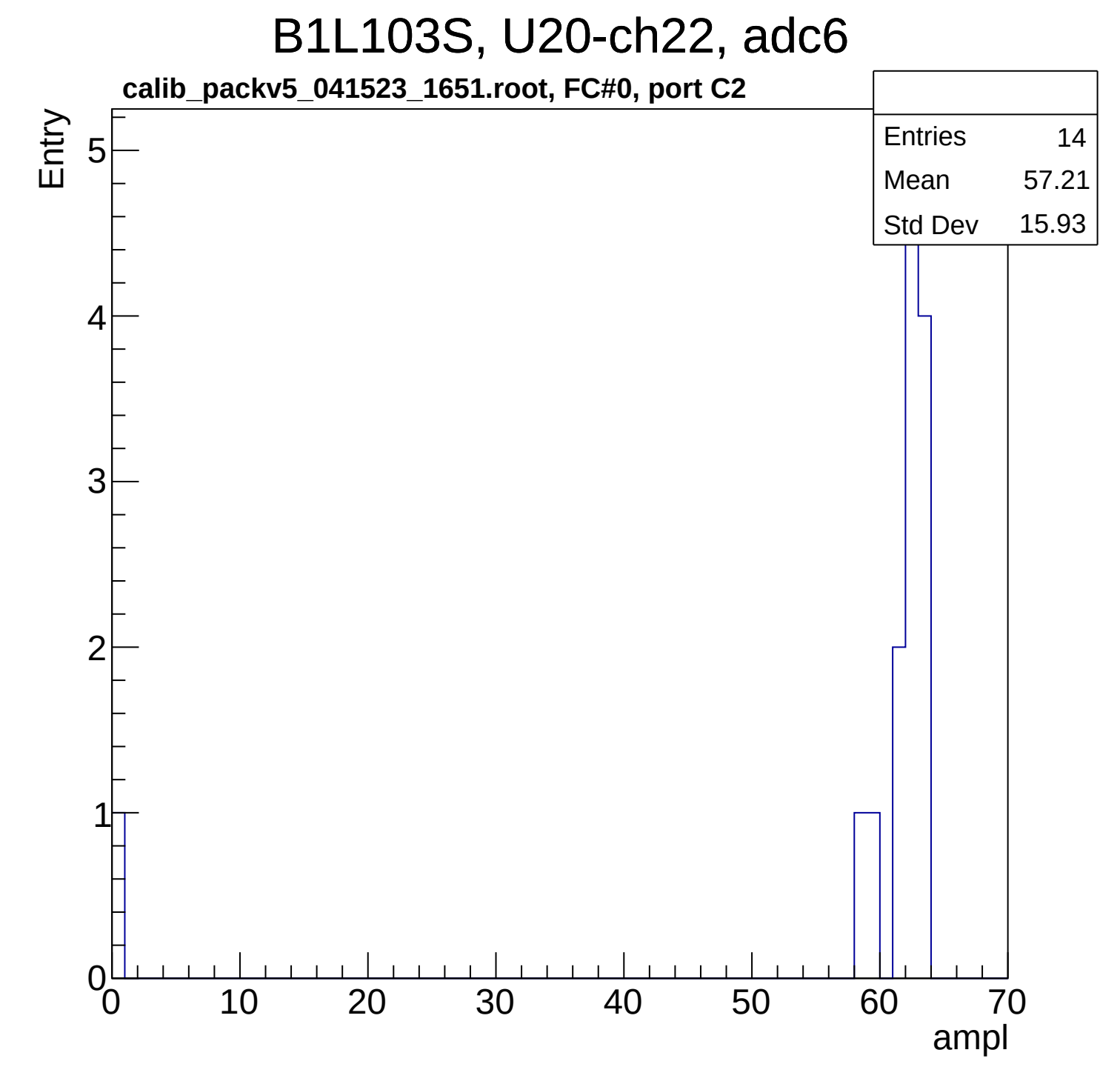
40
50
60
70


B1L103S, U20-ch22, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 57.21
Std Dev 15.93
Entry
ampl
0
1
2
3
4
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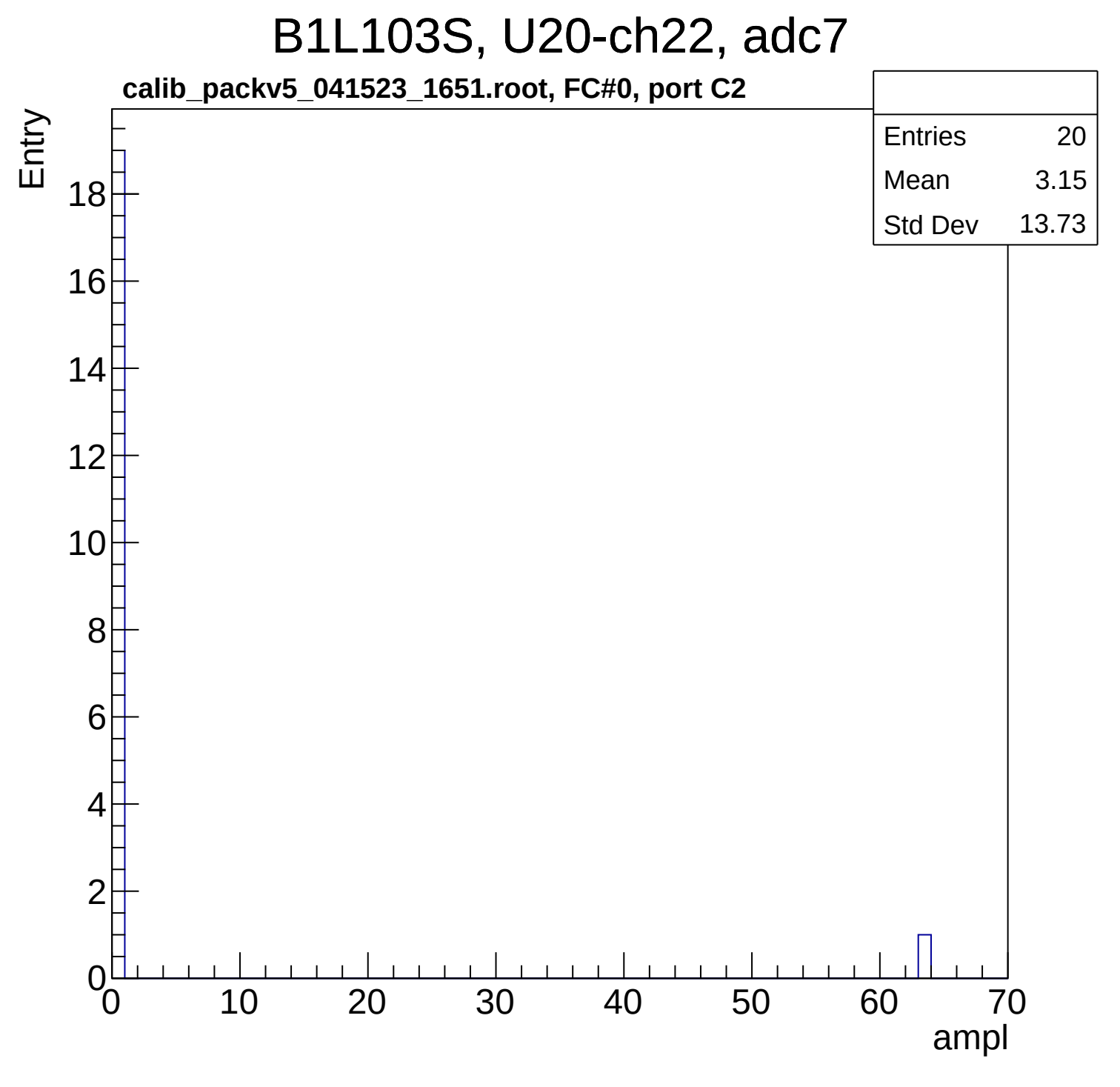
0
10
20
30
40
50
60
70


B1L103S, U20-ch22, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
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6
8
10
12
14
16
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10
20
30
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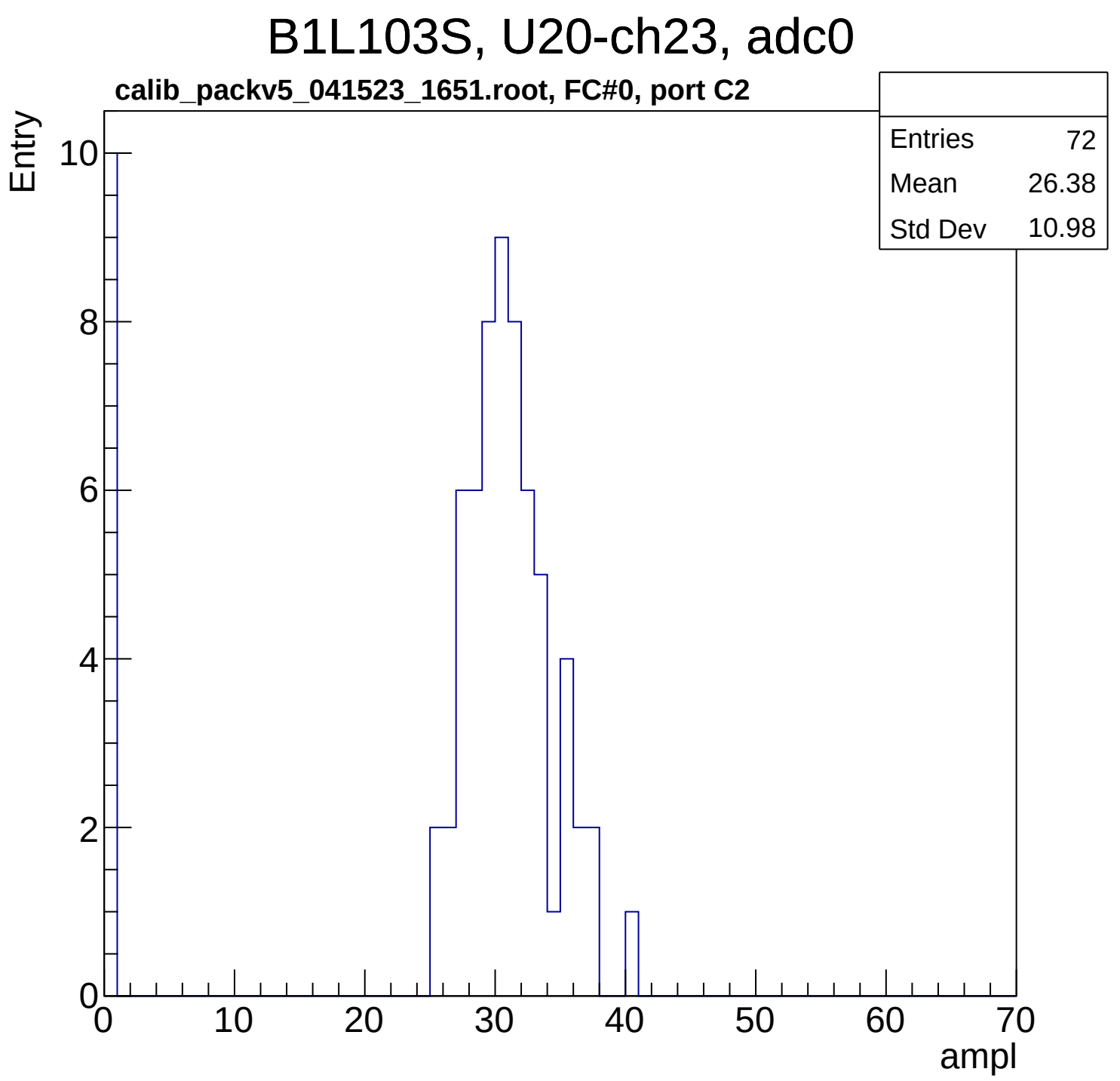
50
60
70
ampl


B1L103S, U20-ch23, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 26.38
Std Dev 10.98
Entry
ampl
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60
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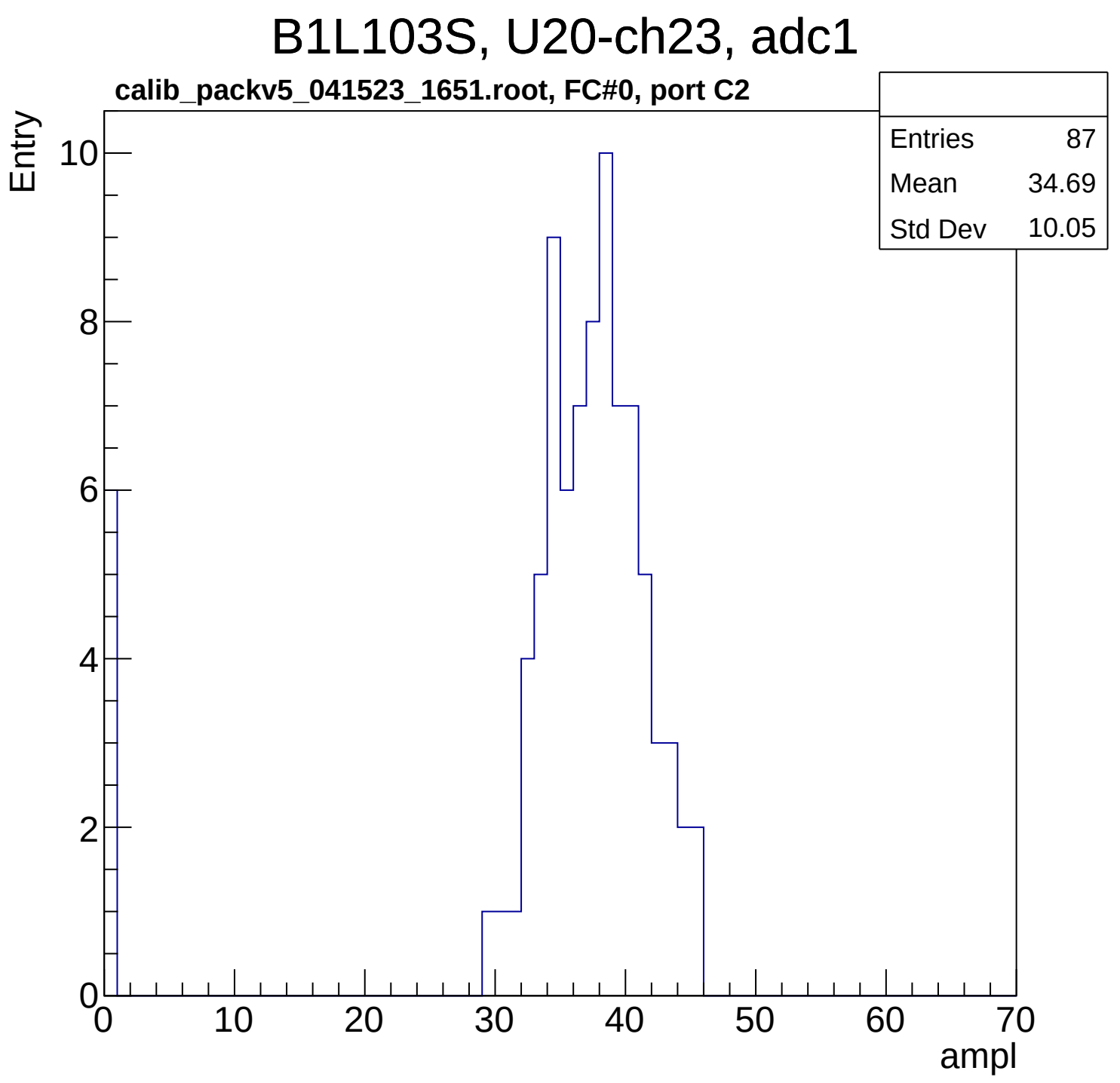
B1L103S, U20-ch23, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 34.69
Std Dev 10.05
Entry
ampl
0
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4
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8
10
0
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30
40
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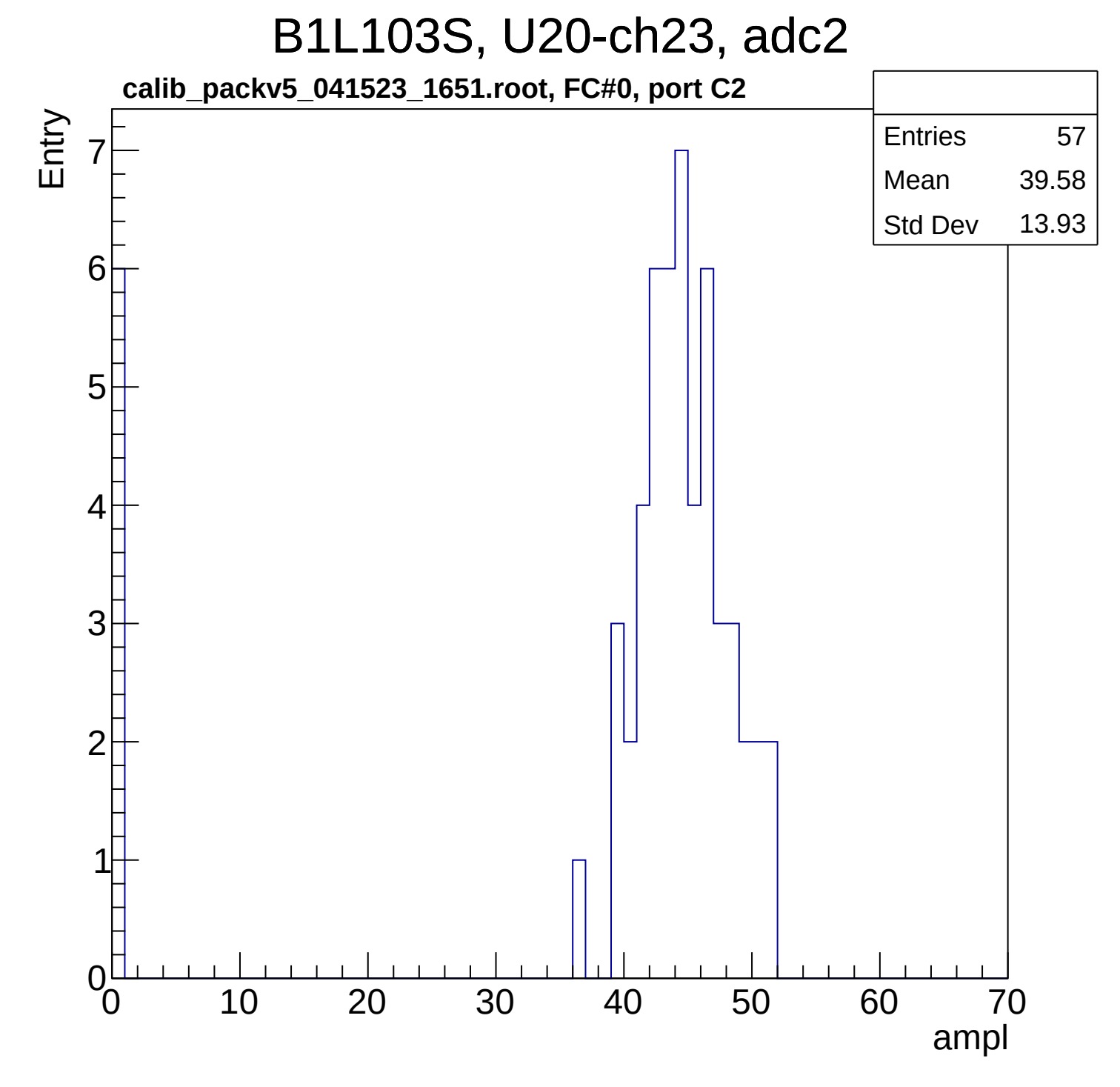
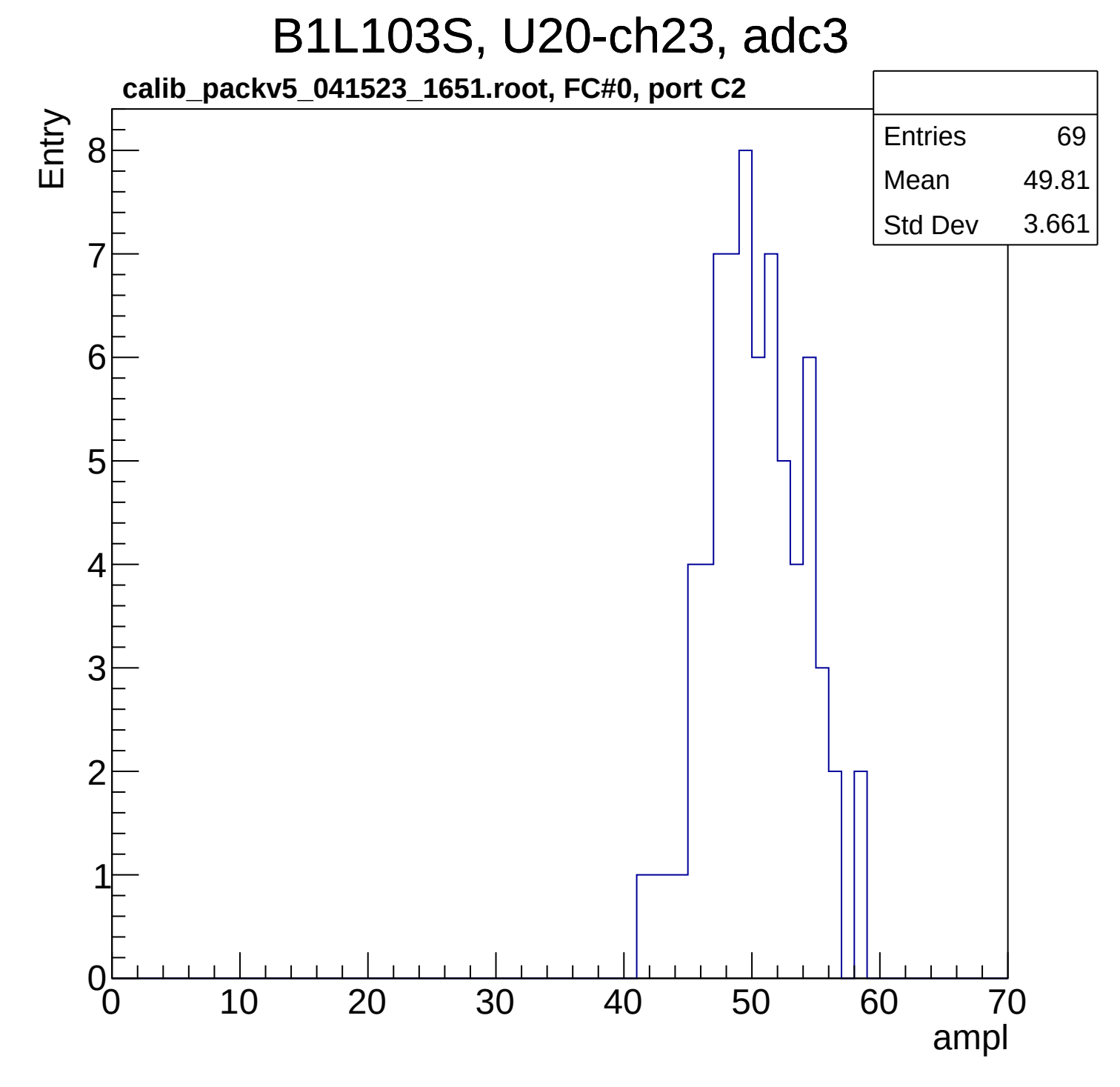
60
70


B1L103S, U20-ch23, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 39.58
Std Dev 13.93
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U20-ch23, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 49.81
Std Dev 3.661
Entry
ampl
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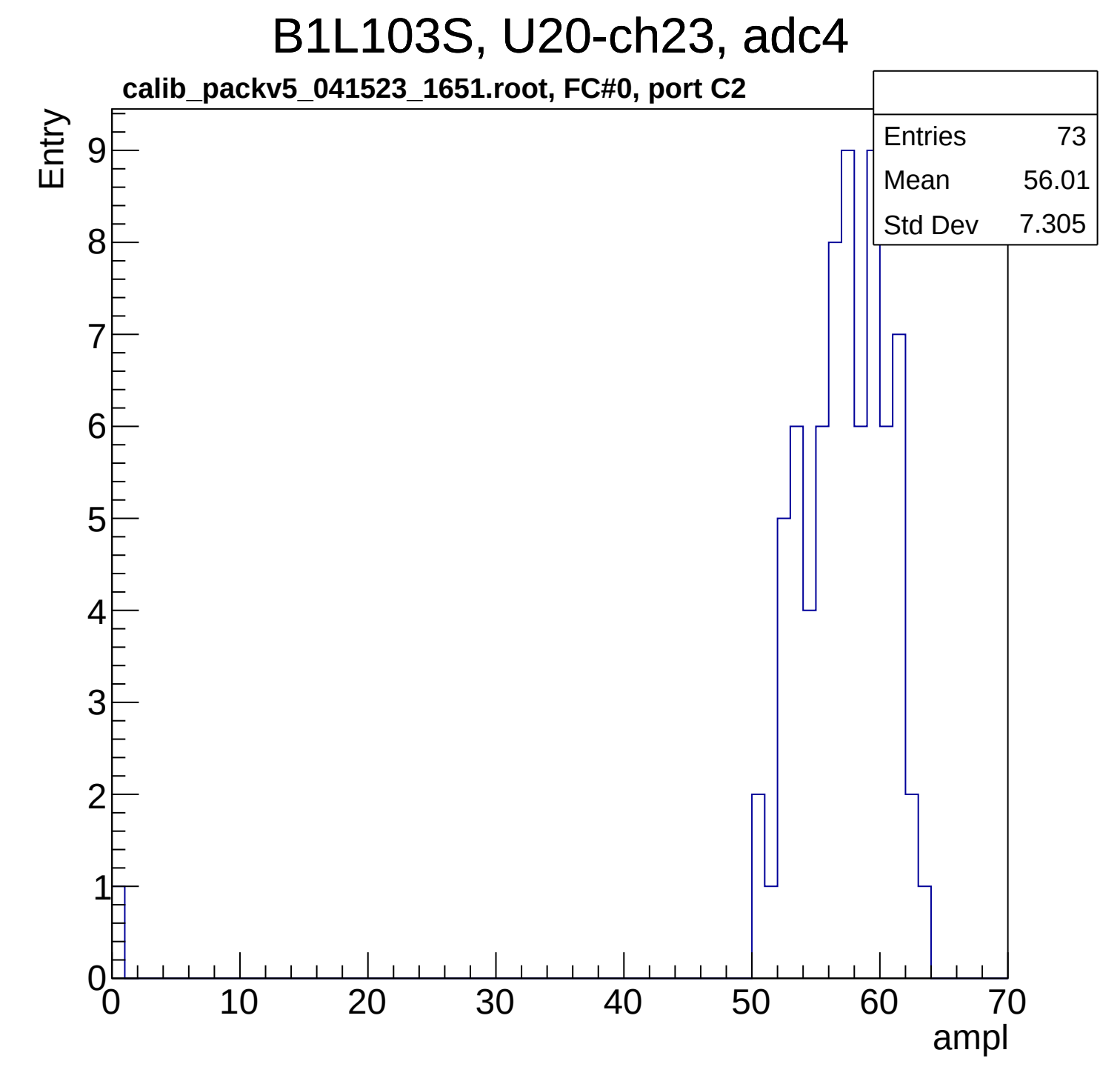
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch23, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 56.01
Std Dev 7.305
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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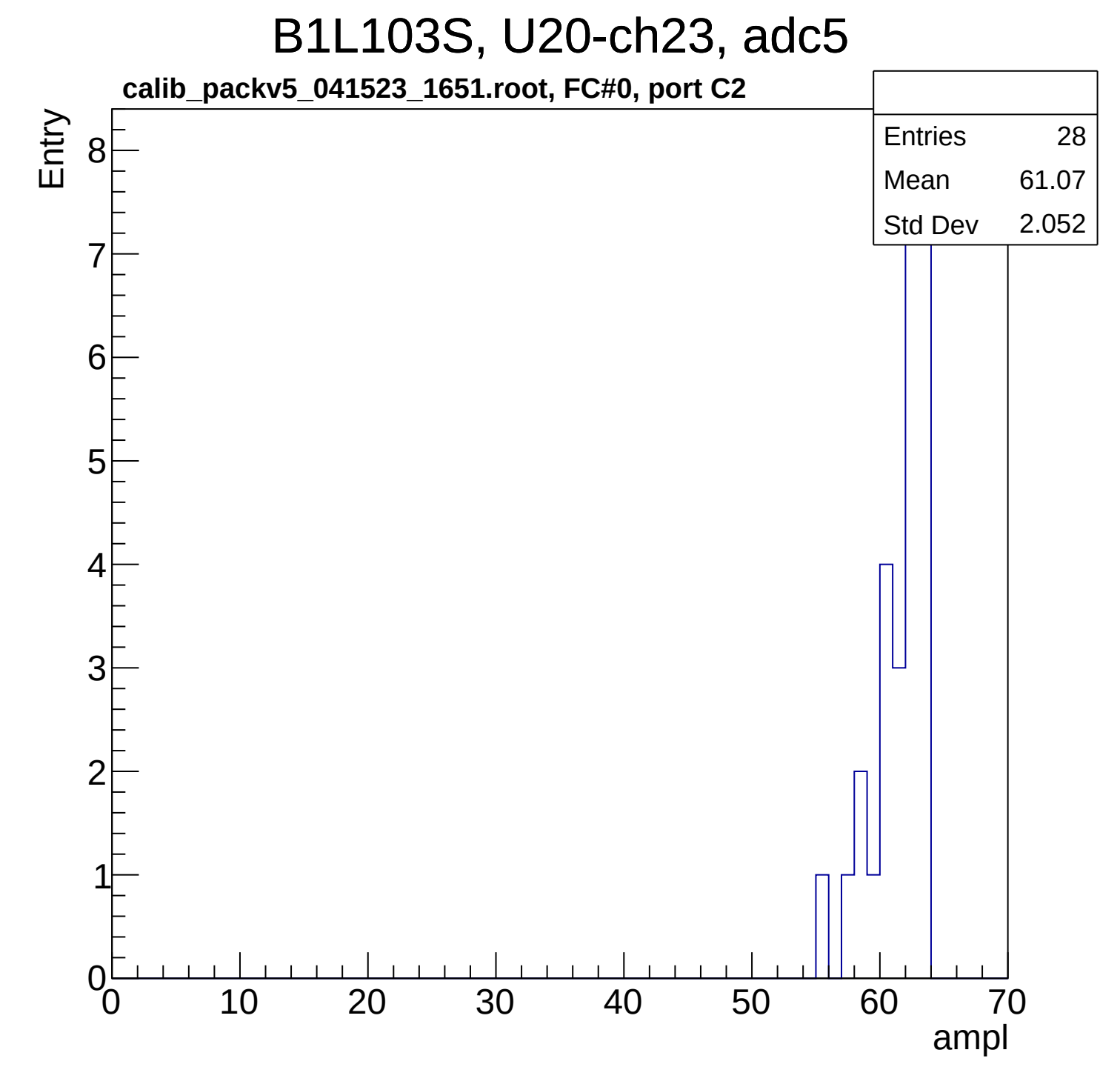
50
60
70


B1L103S, U20-ch23, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 61.07
Std Dev 2.052
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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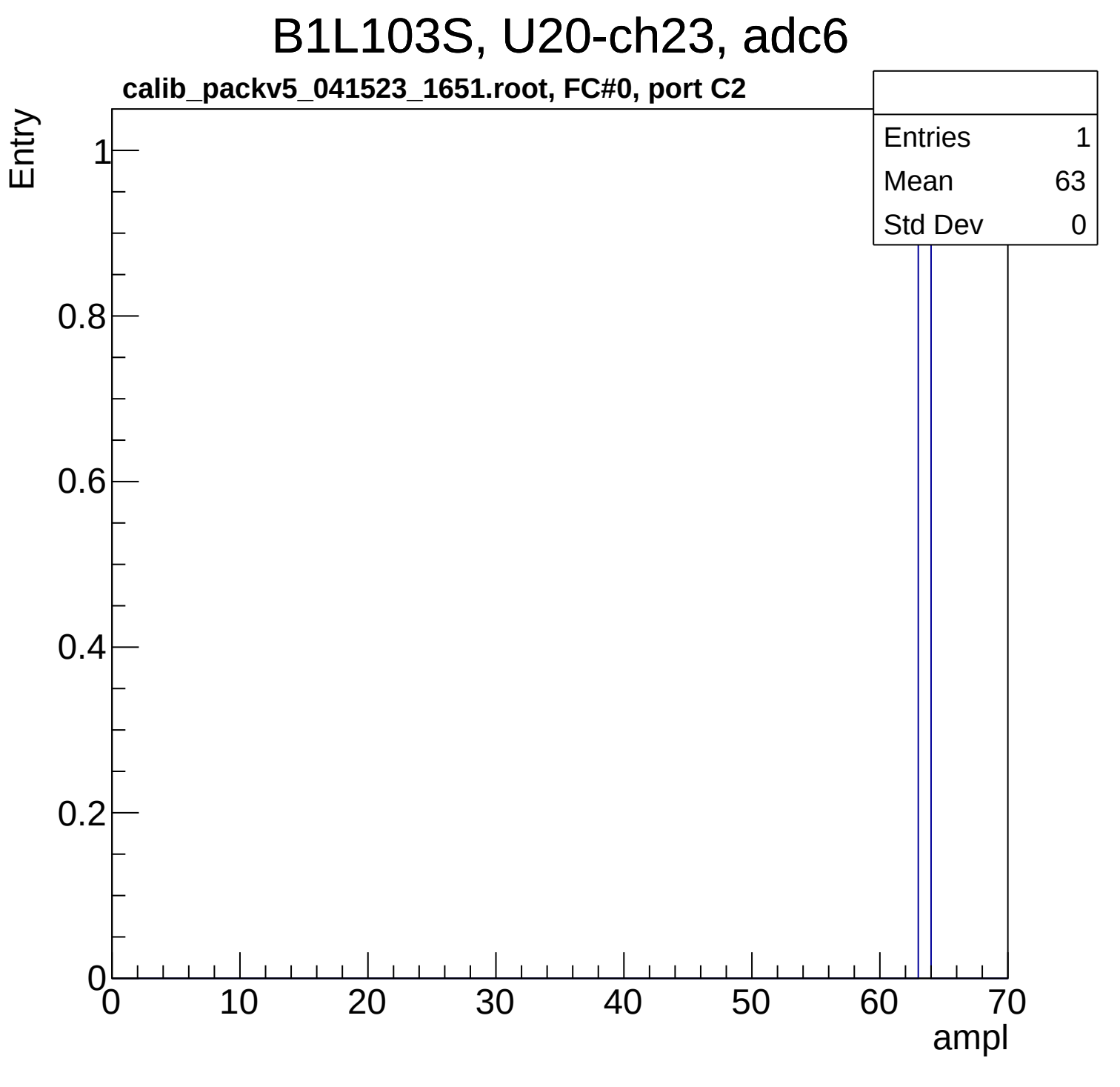
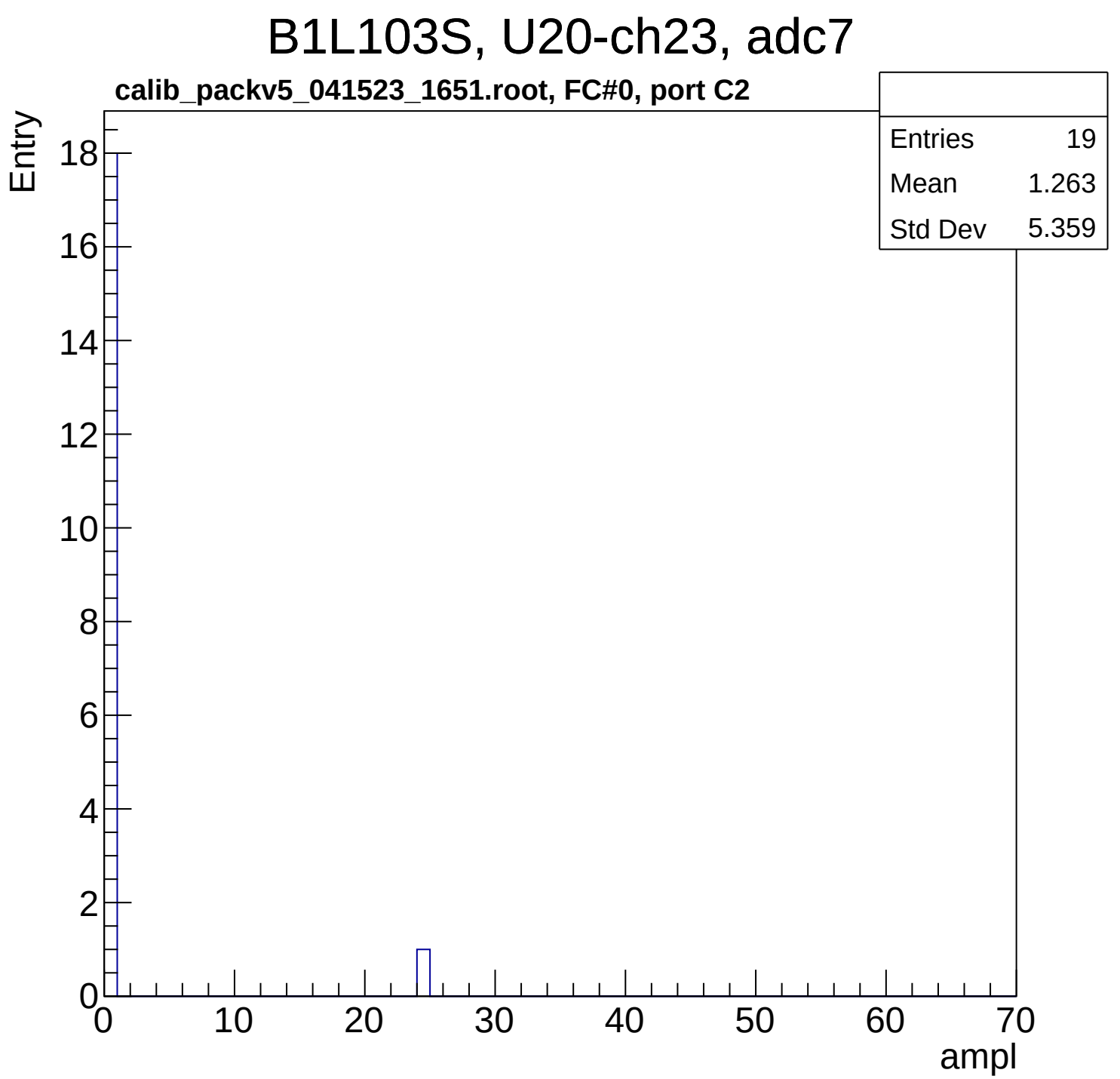
40
50
60
70


B1L103S, U20-ch23, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch23, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.263
Std Dev 5.359
Entry
0
2
4
6
8
10
12
14
16
18
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10
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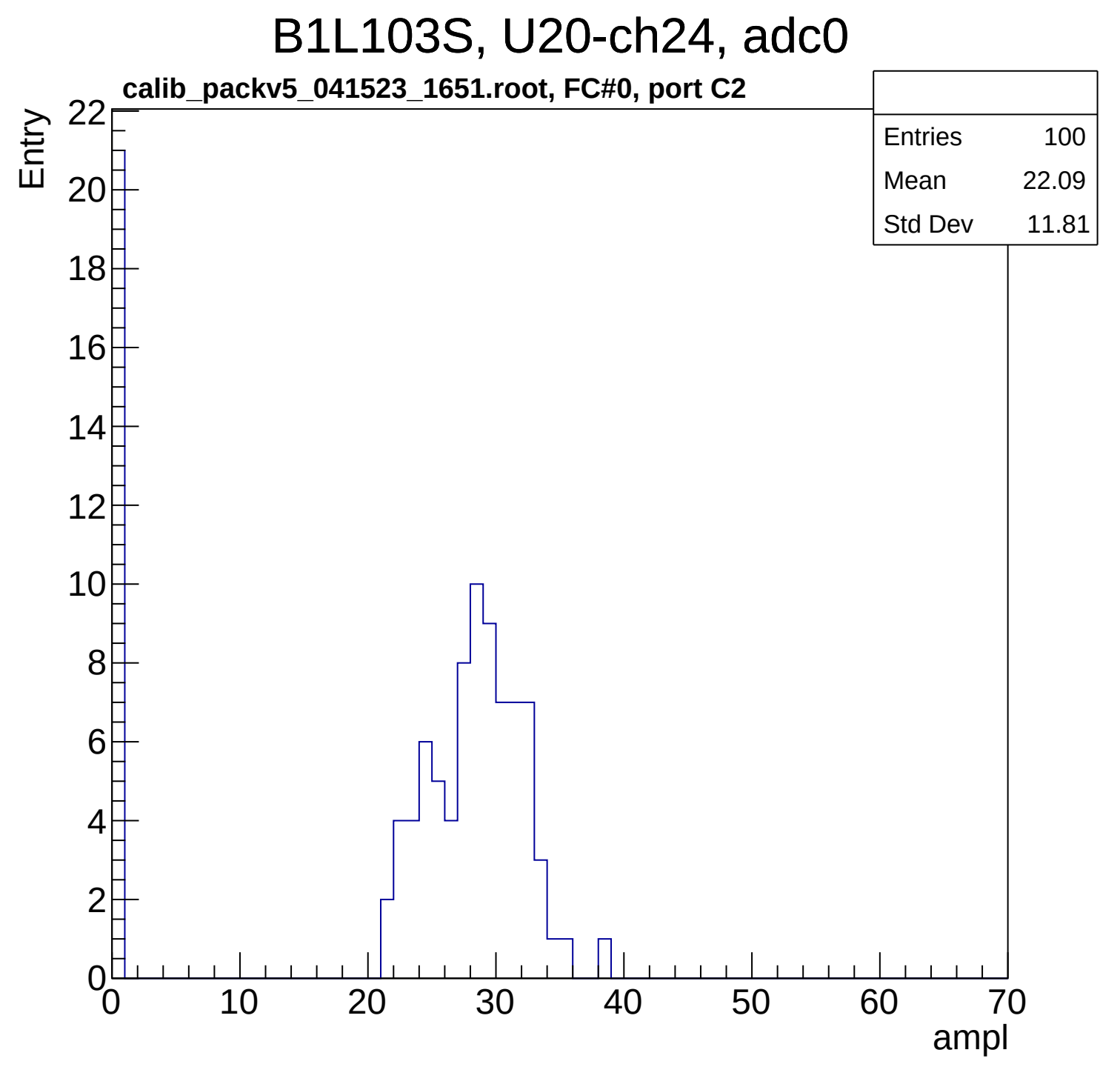
70
ampl


B1L103S, U20-ch24, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 100
Mean 22.09
Std Dev 11.81
Entry
ampl
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2
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8
10
12
14
16
18
20
22
0
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40
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60
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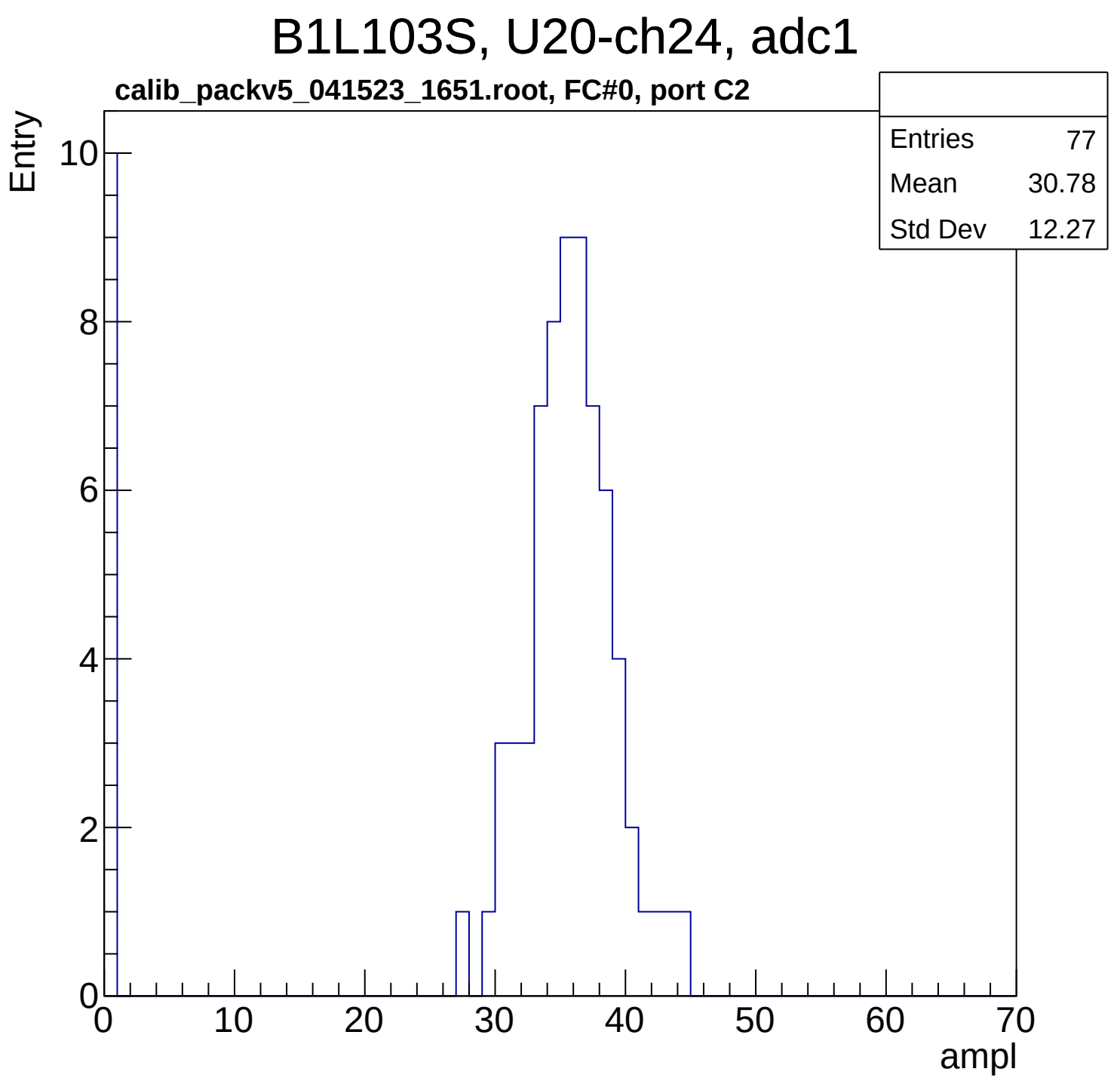
B1L103S, U20-ch24, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 30.78
Std Dev 12.27
Entry
ampl
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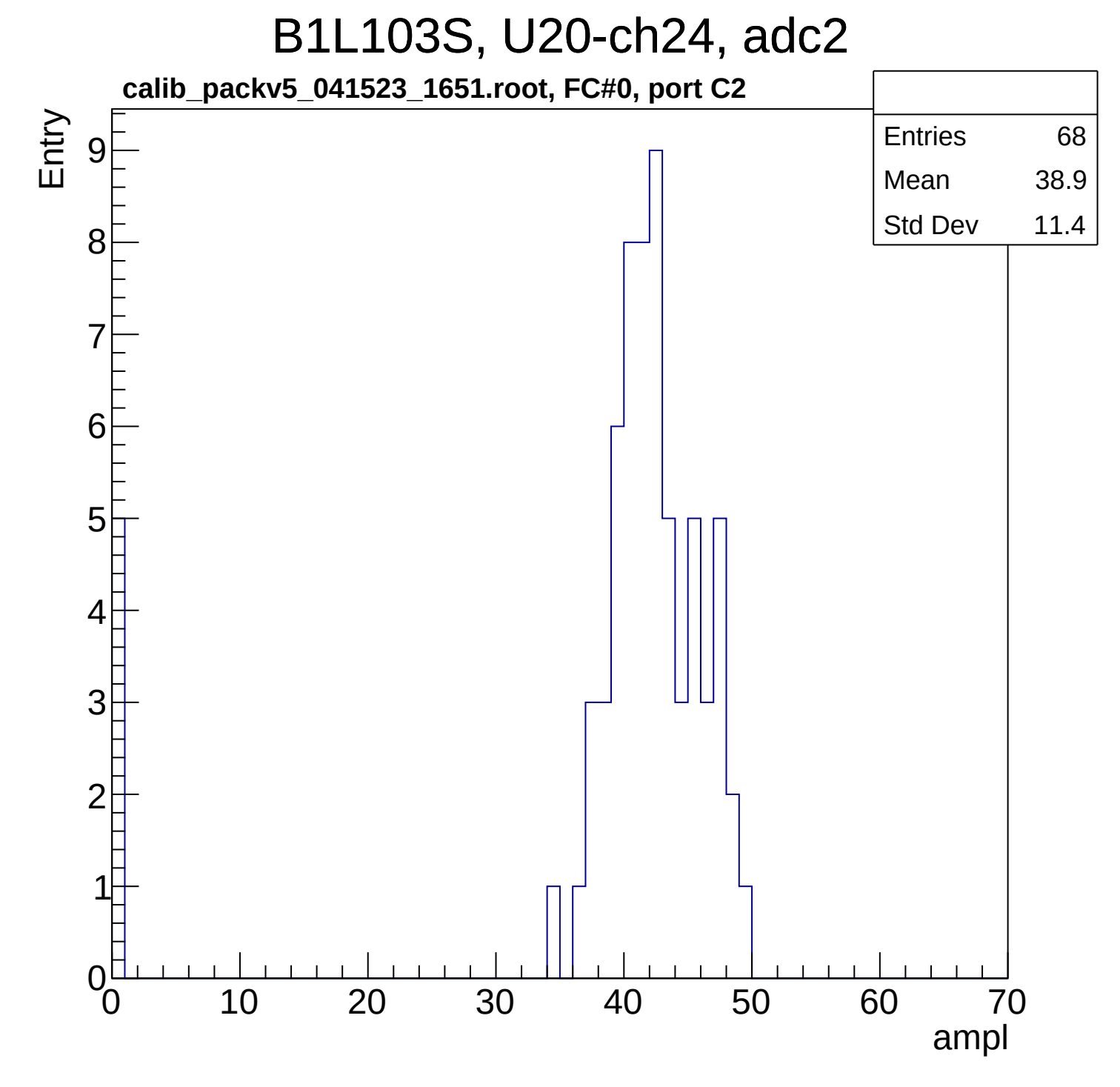
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U20-ch24, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 38.9
Std Dev 11.4
Entry
ampl
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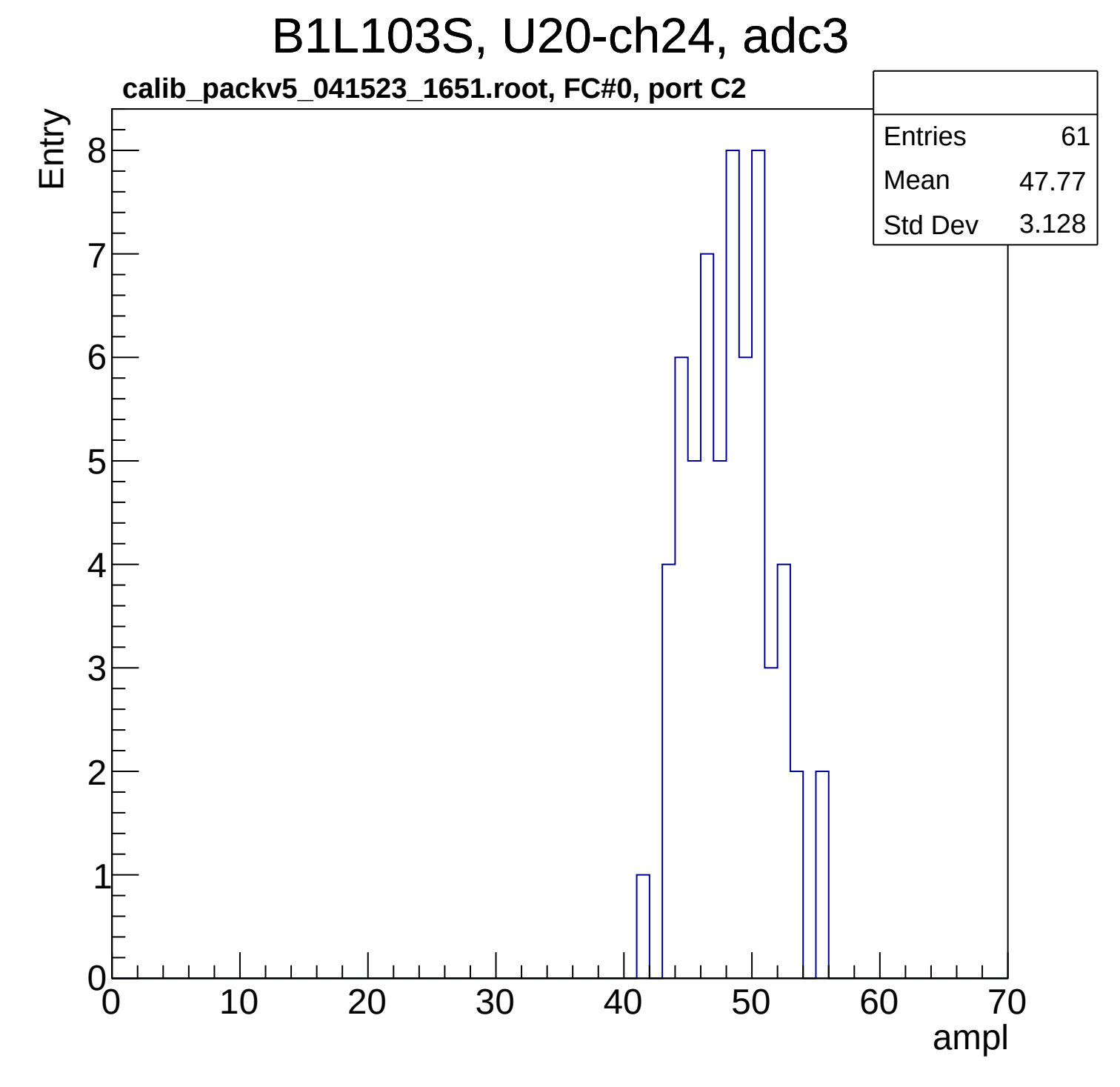
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch24, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 47.77
Std Dev 3.128
Entry
ampl
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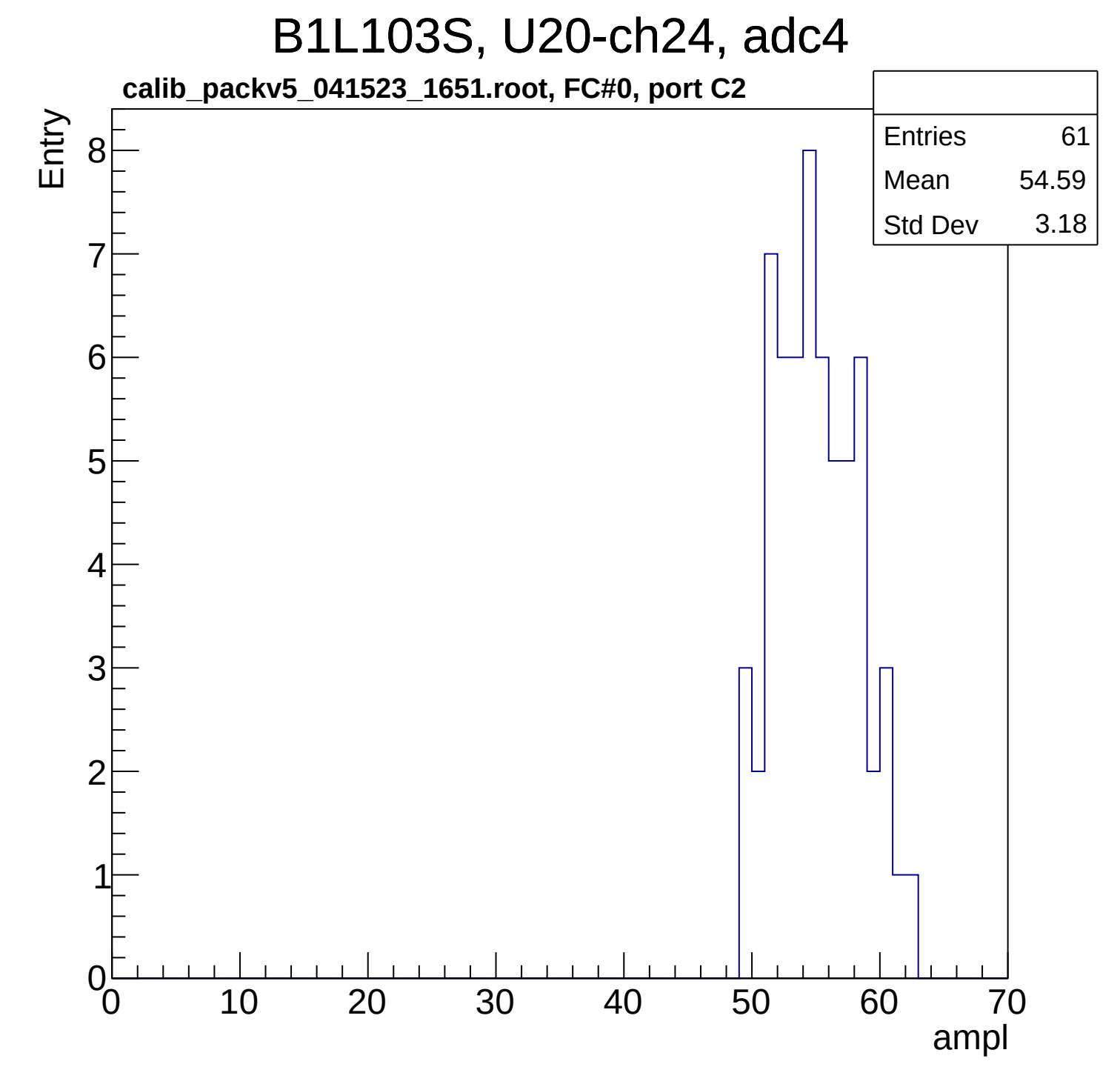
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch24, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 54.59
Std Dev 3.18
Entry
ampl
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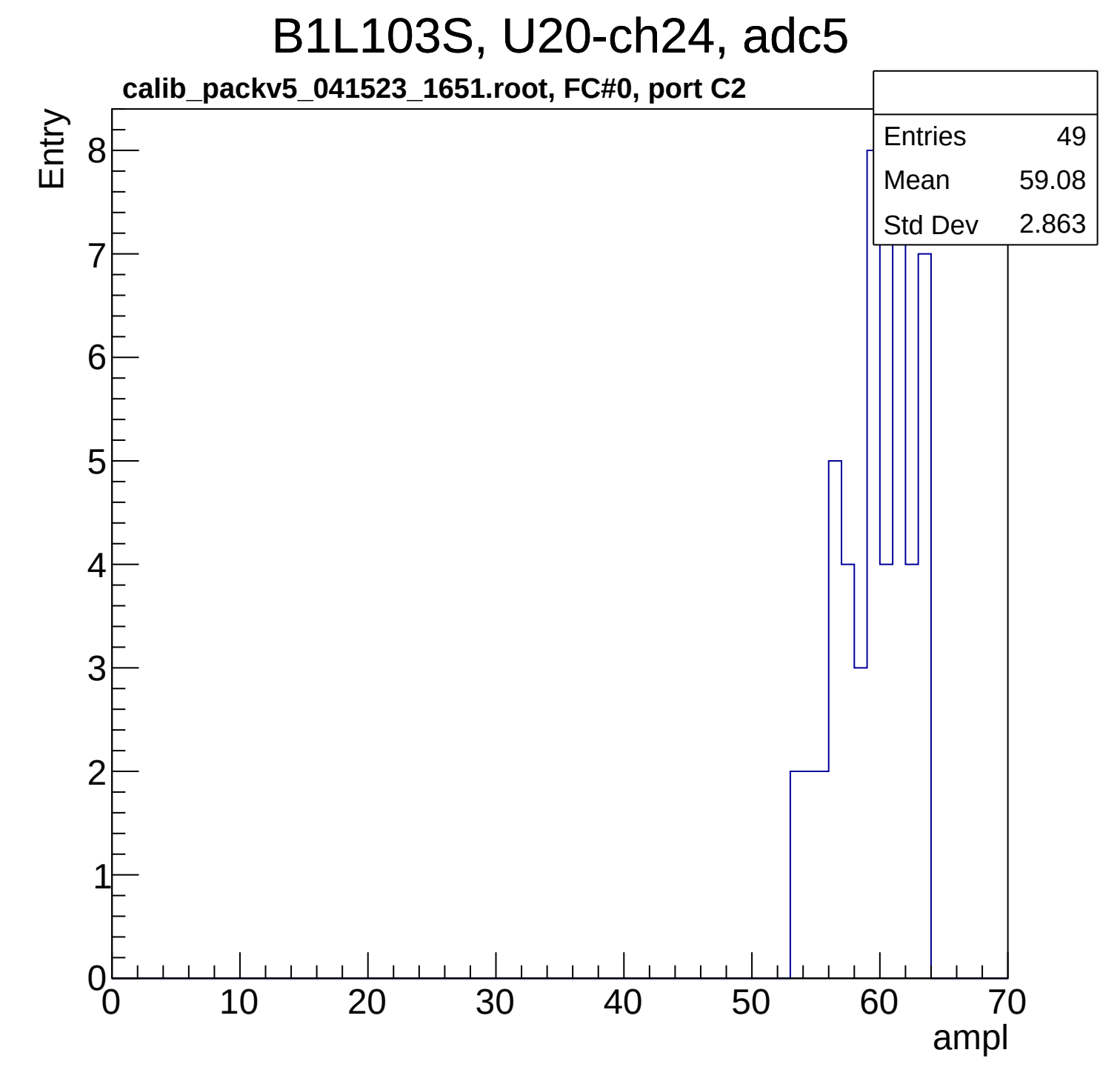
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch24, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 59.08
Std Dev 2.863
Entry
ampl
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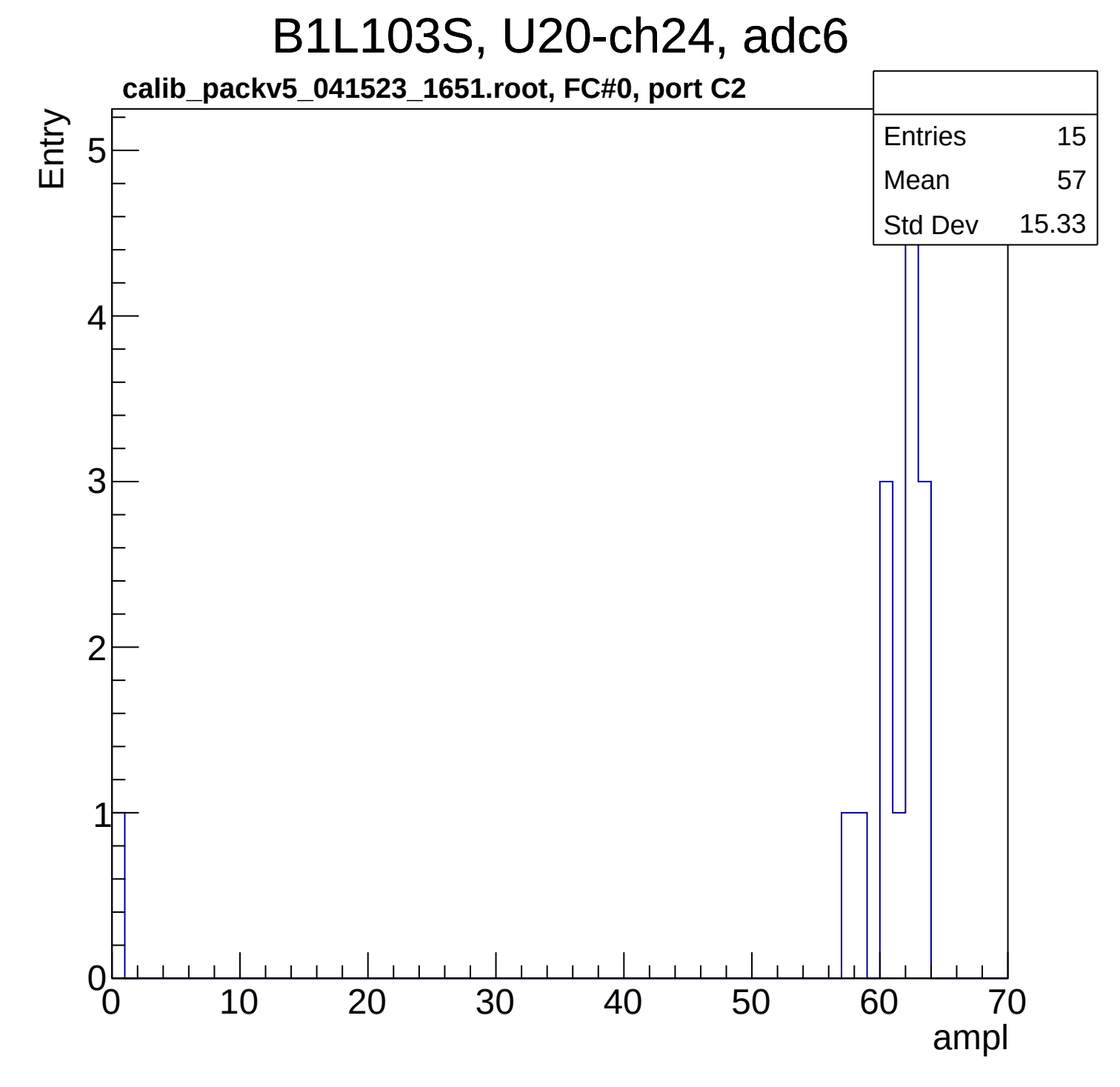
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch24, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 57
Std Dev 15.33
Entry
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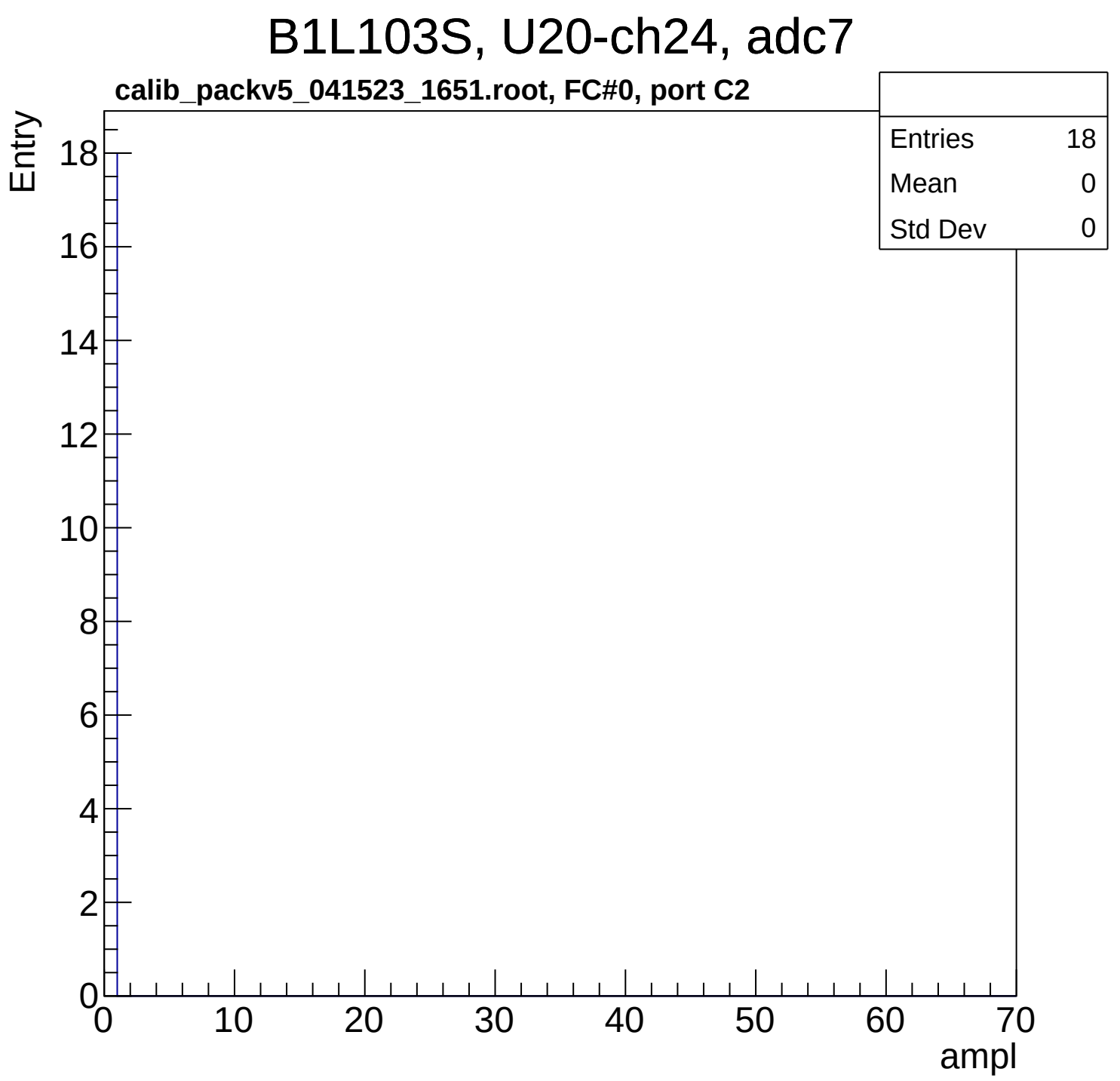
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch24, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
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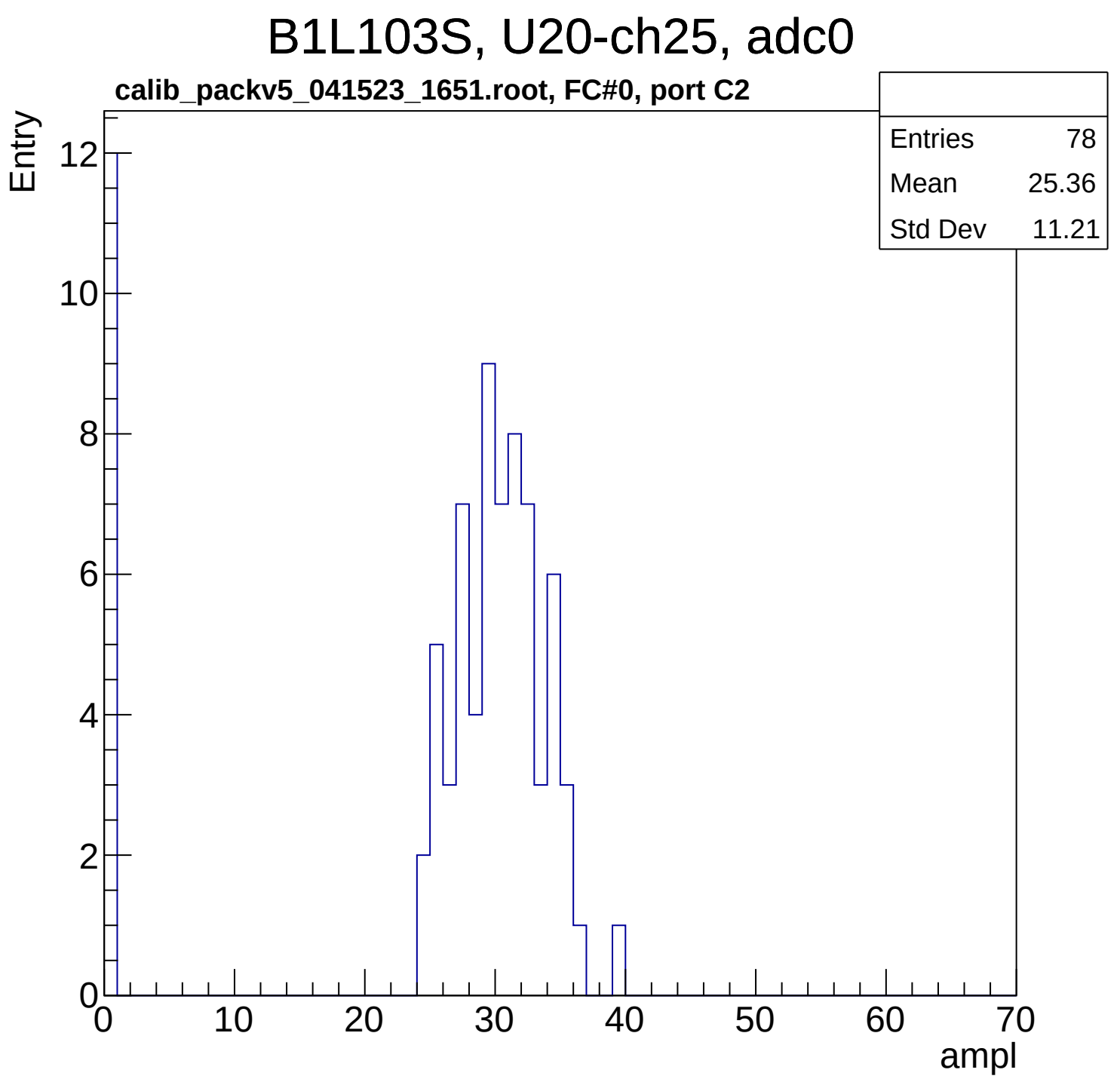
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch25, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 25.36
Std Dev 11.21
Entry
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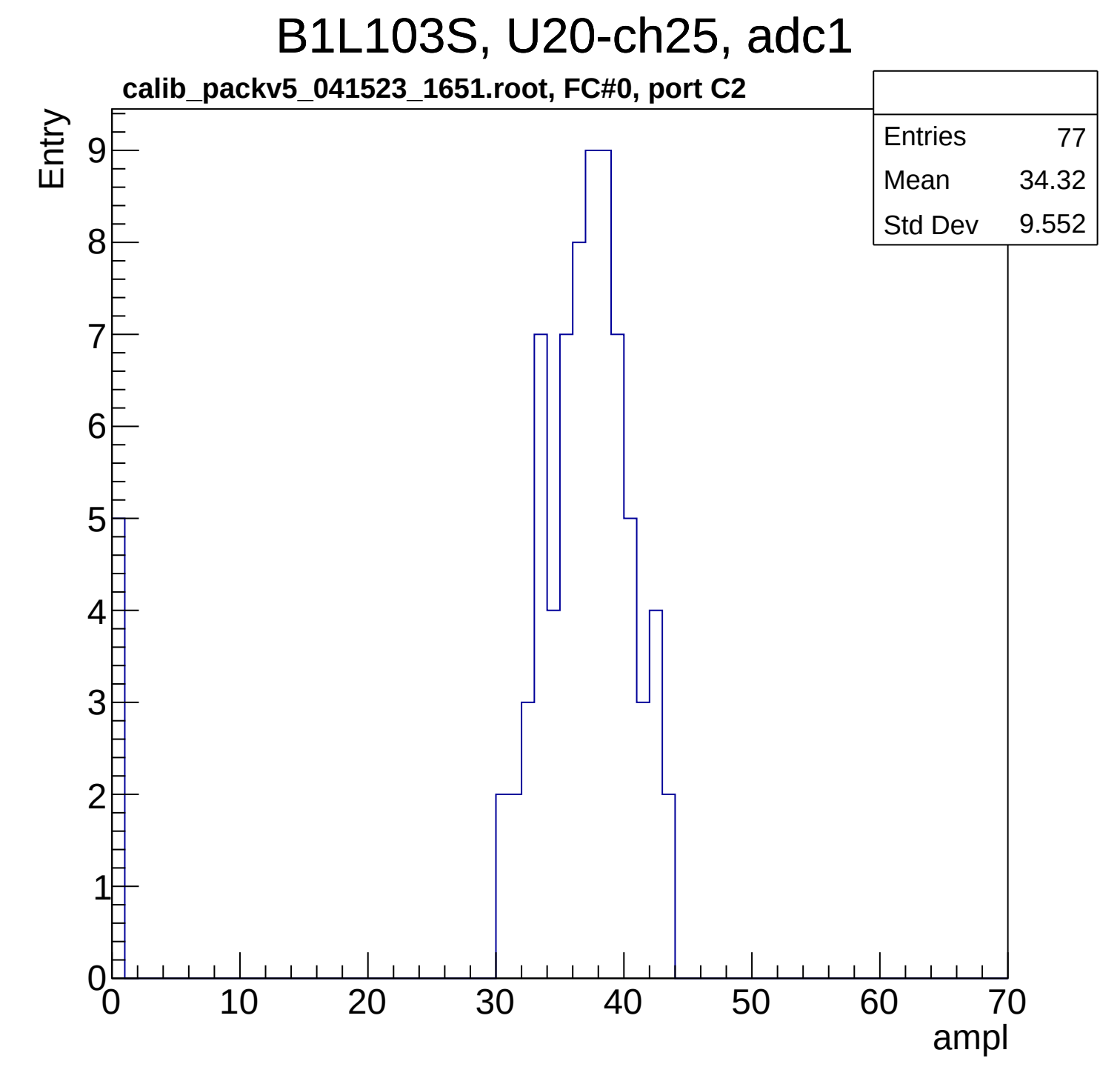
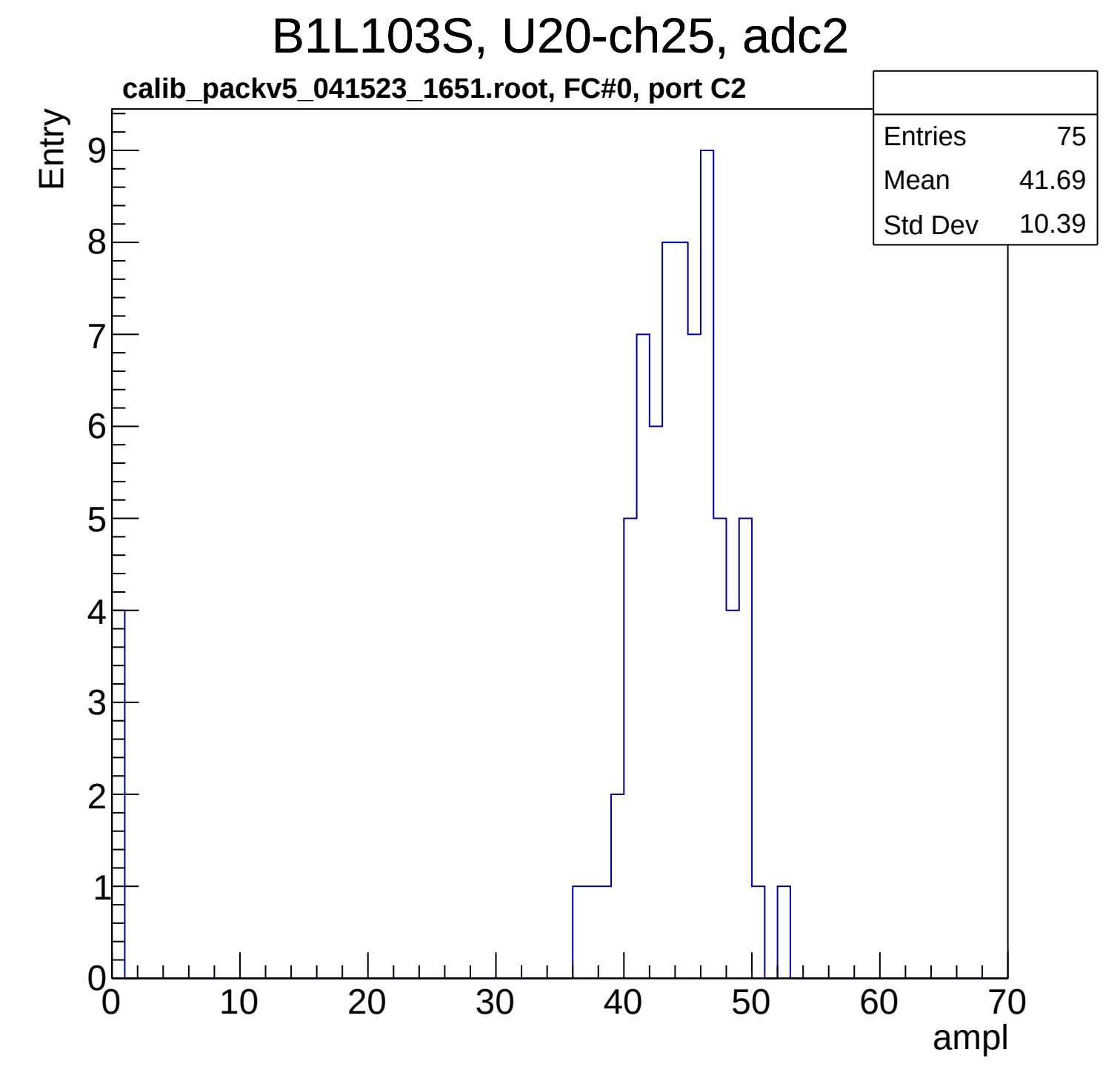
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch25, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 34.32
Std Dev 9.552
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch25, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 41.69
Std Dev 10.39
Entry
ampl
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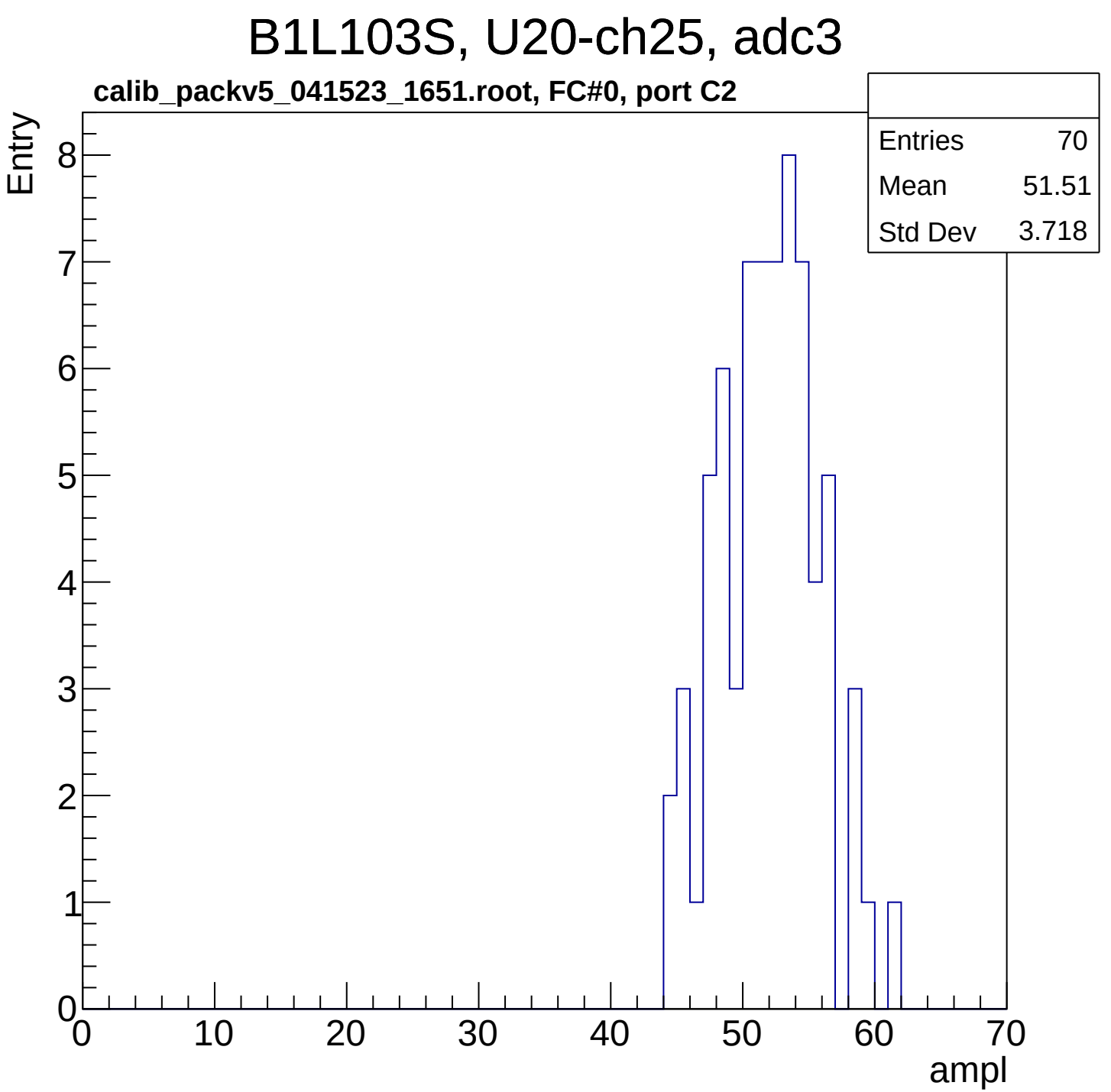
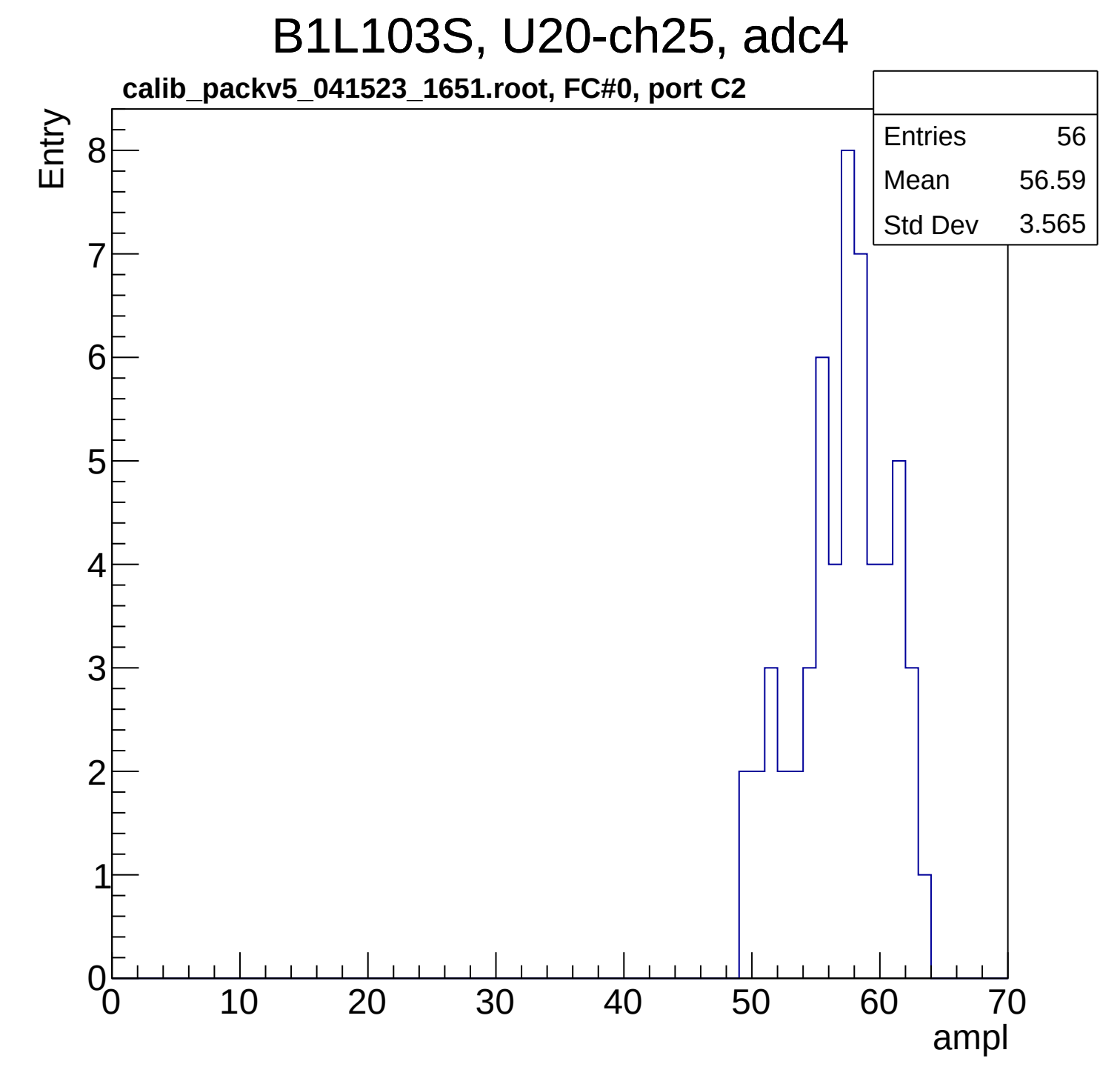
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L103S, U20-ch25, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 51.51
Std Dev 3.718
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch25, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 56.59
Std Dev 3.565
Entry
ampl
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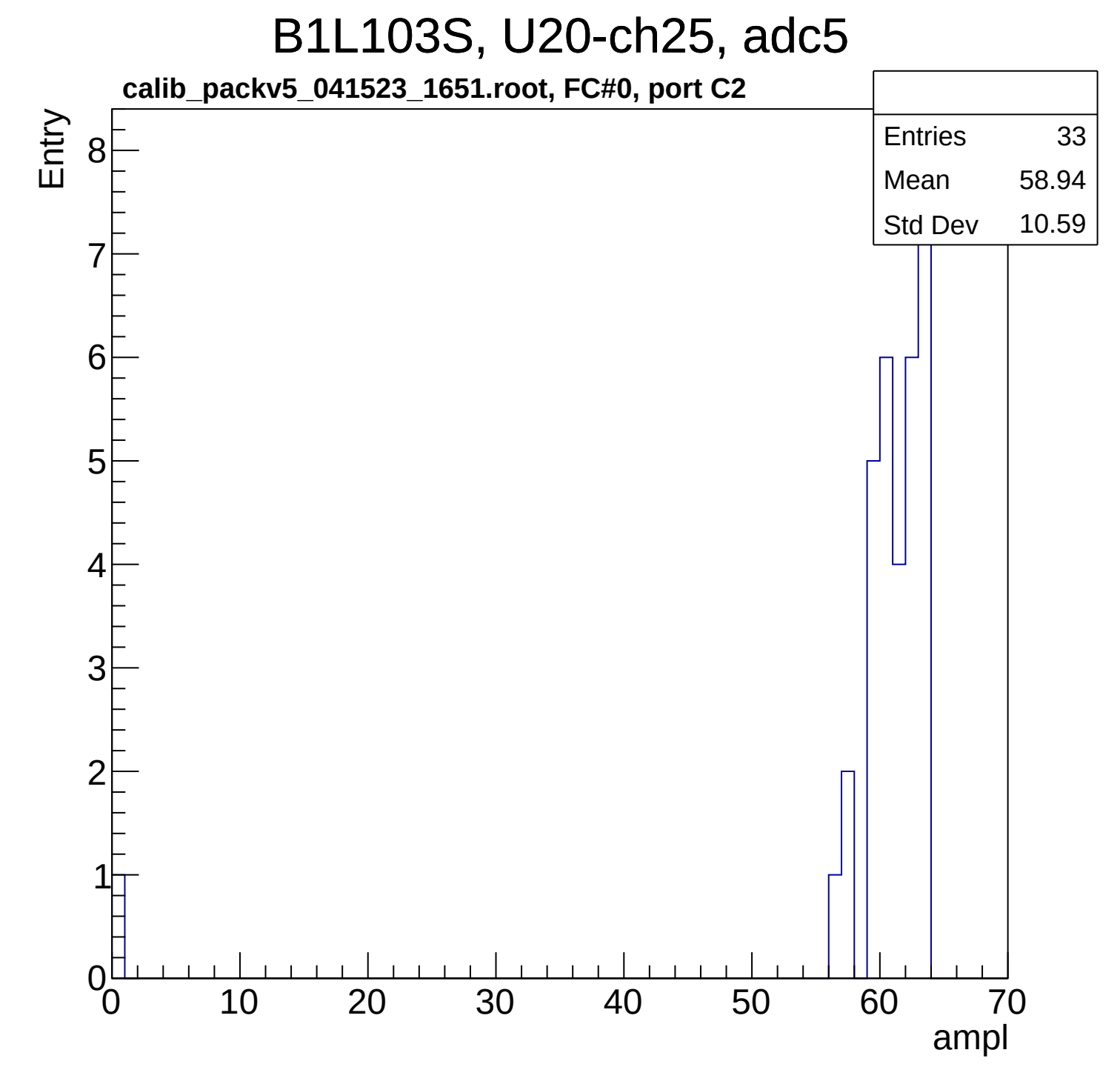
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch25, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 58.94
Std Dev 10.59
Entry
ampl
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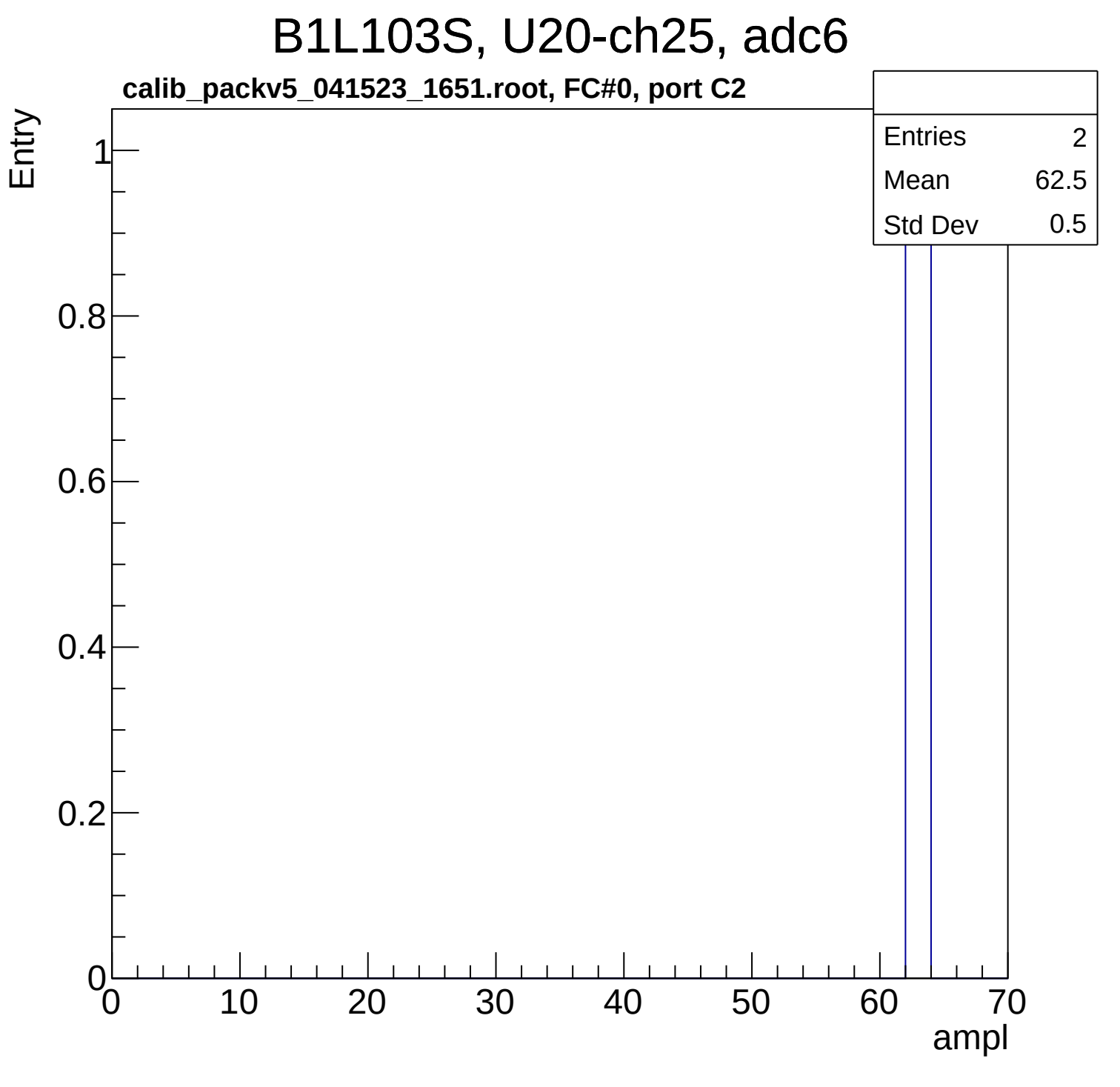
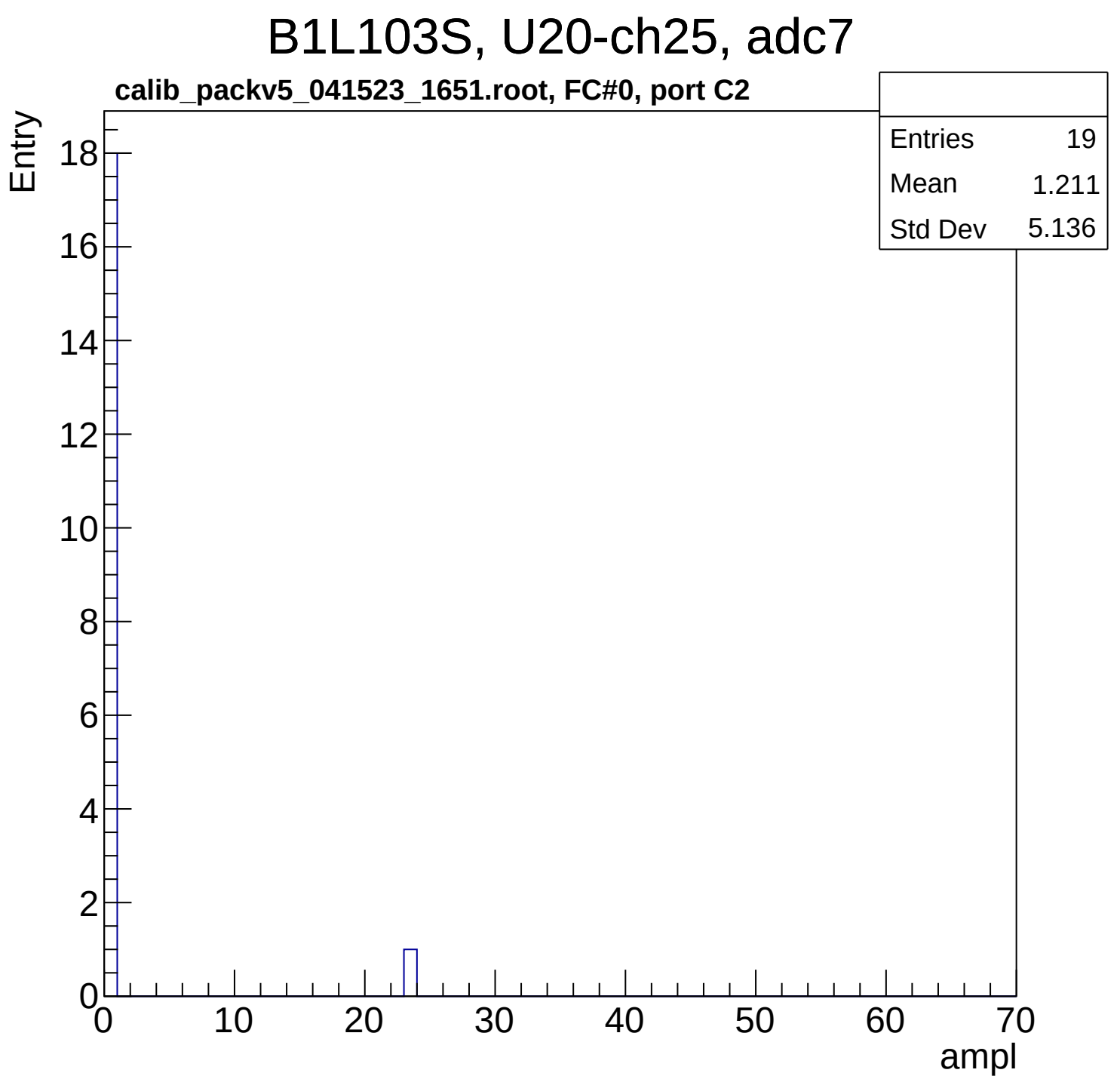
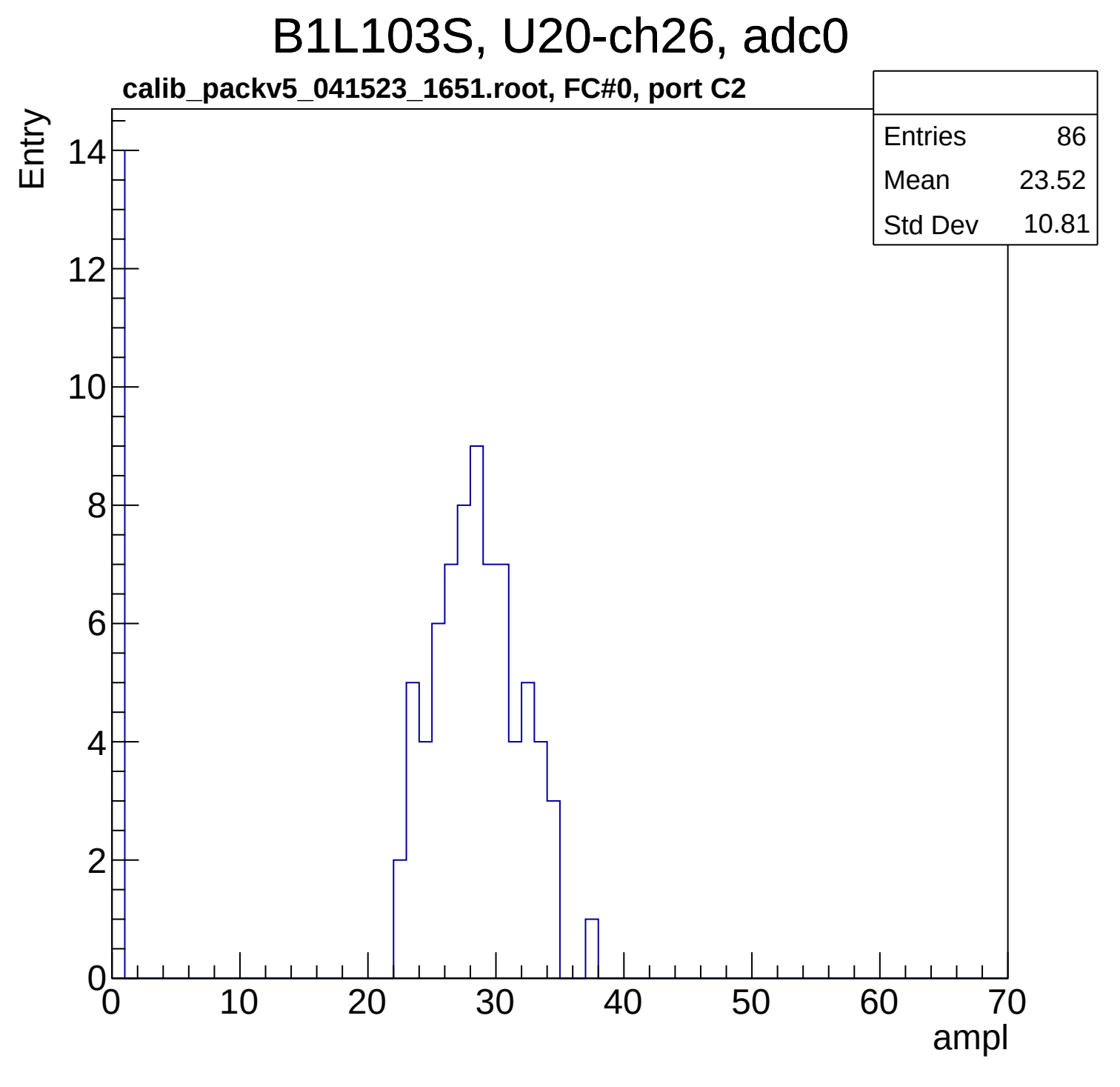
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch25, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch25, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.211
Std Dev 5.136
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch26, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 23.52
Std Dev 10.81
Entry
ampl
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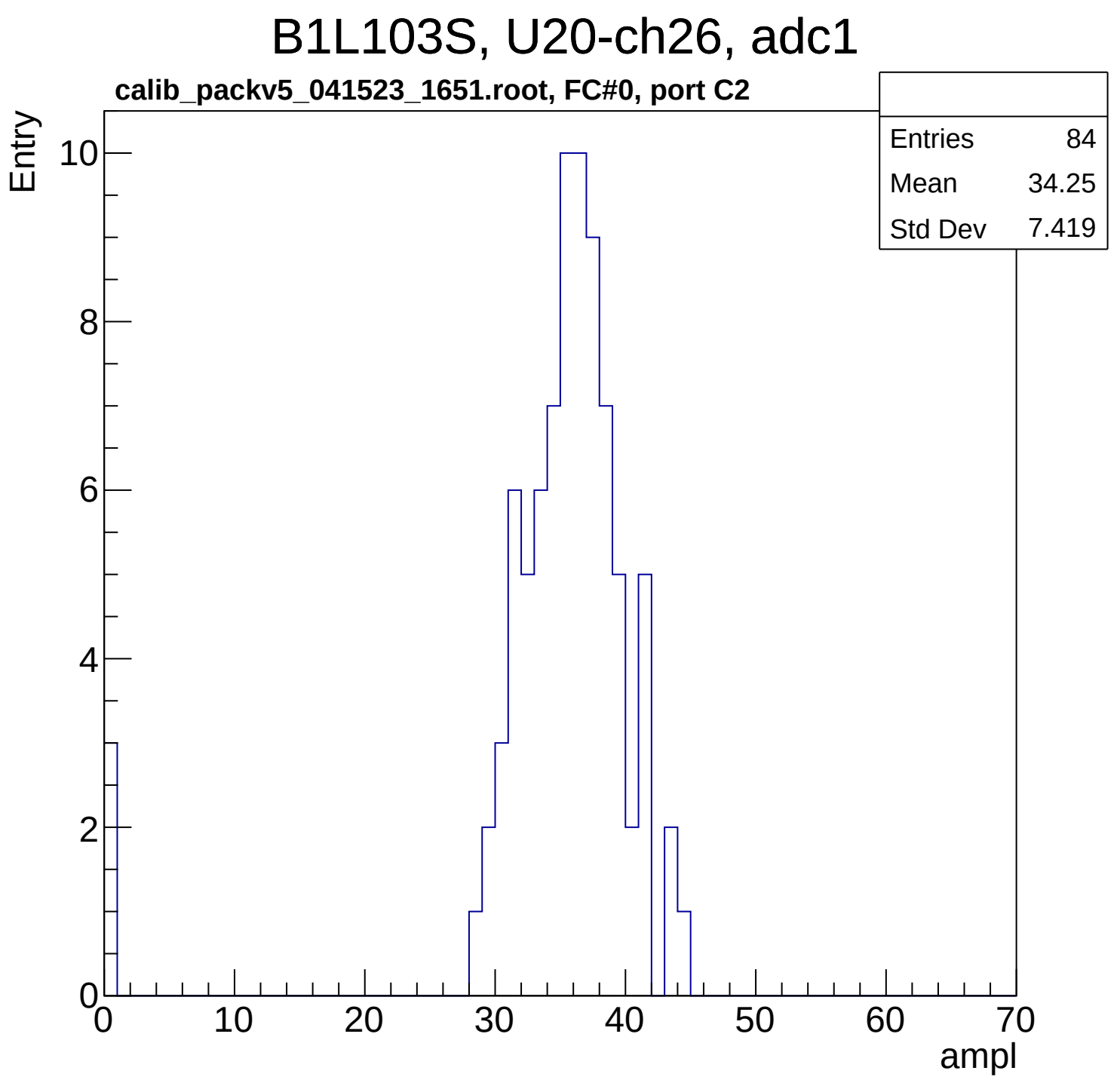
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U20-ch26, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 34.25
Std Dev 7.419
Entry
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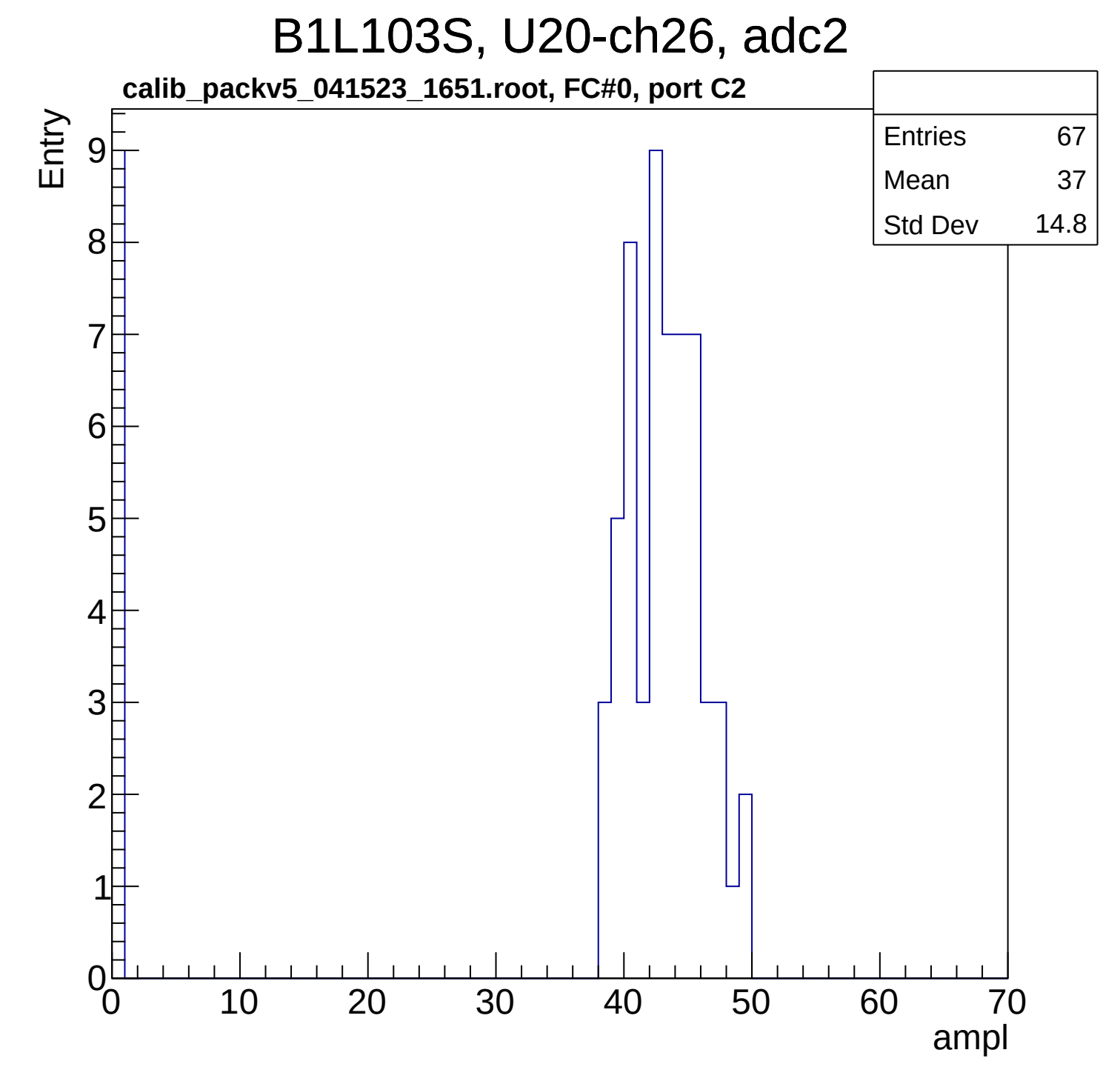
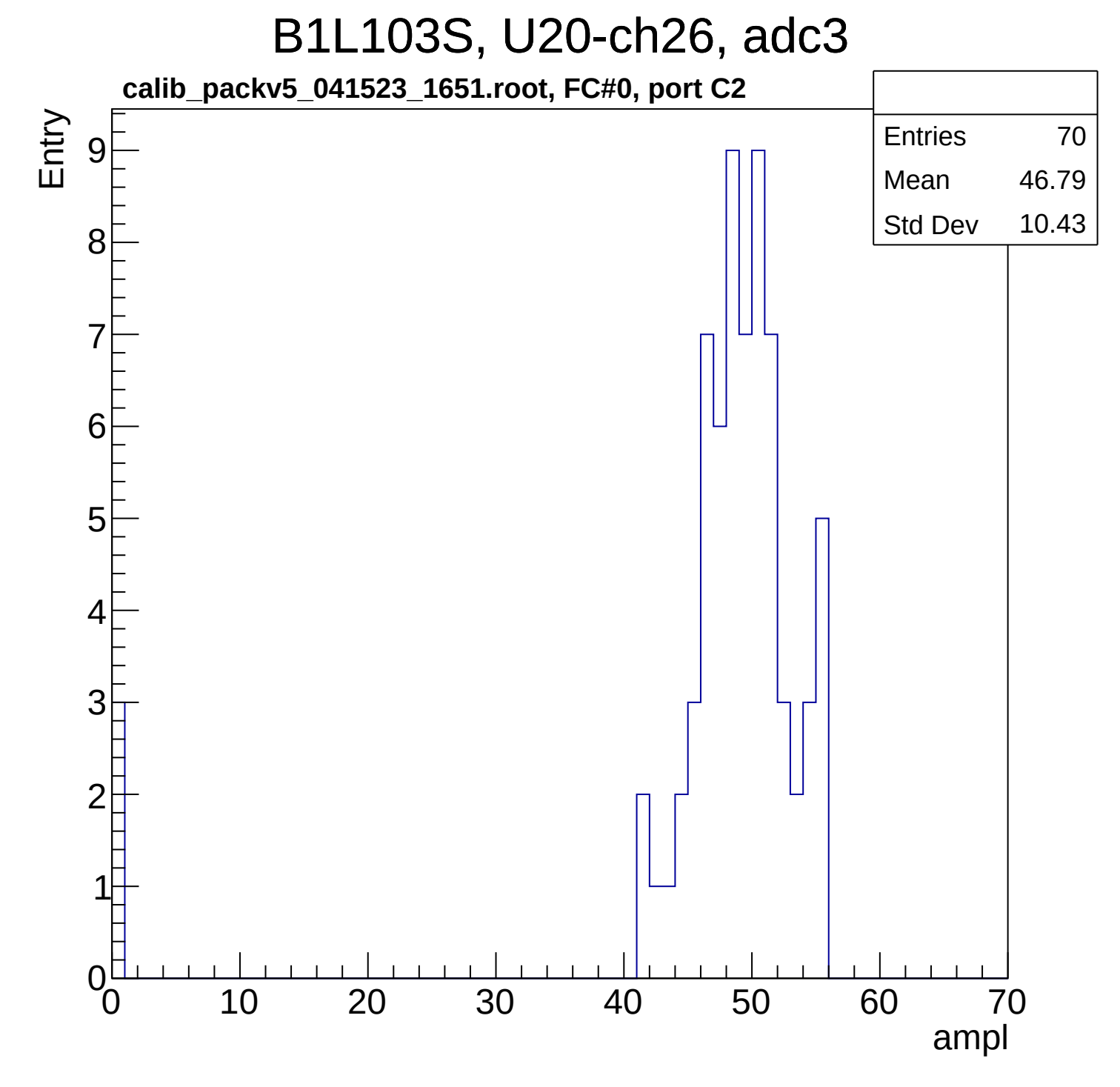
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch26, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 37
Std Dev 14.8
Entry
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch26, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 46.79
Std Dev 10.43
Entry
ampl
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2
3
4
5
6
7
8
9
0
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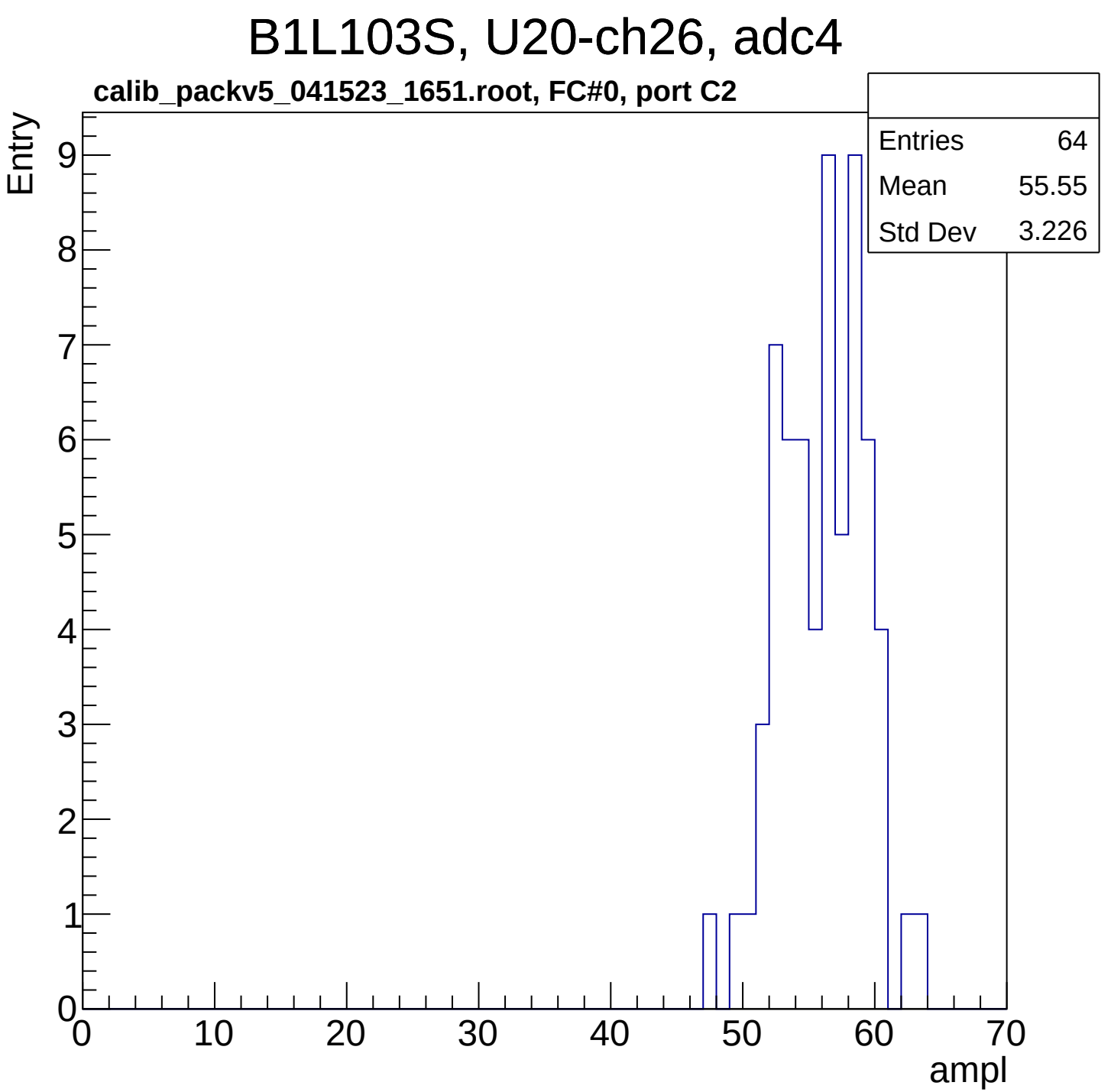
20
30
40
50
60
70


B1L103S, U20-ch26, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 55.55
Std Dev 3.226
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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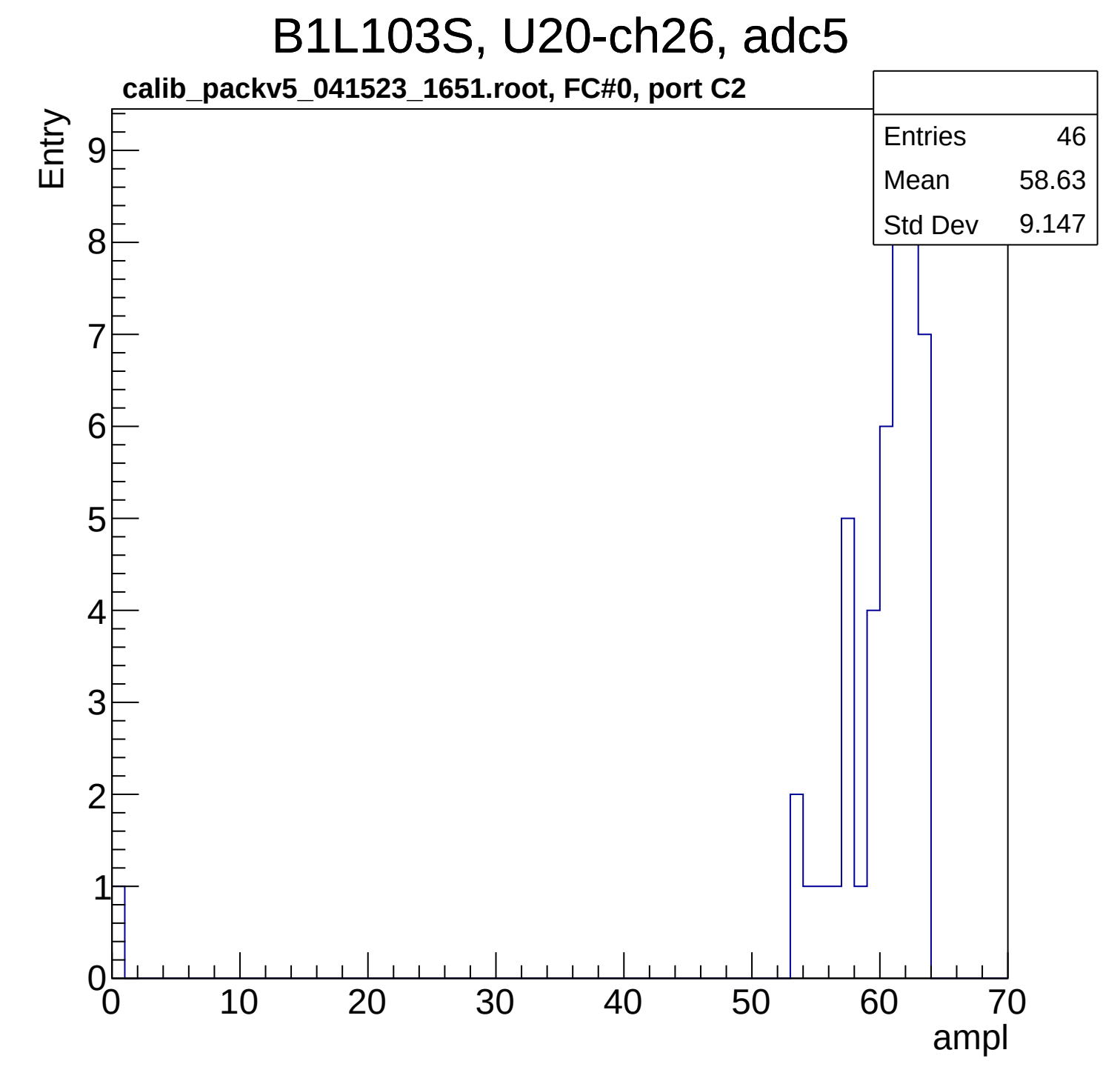
60
70


B1L103S, U20-ch26, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 58.63
Std Dev 9.147
Entry
ampl
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2
3
4
5
6
7
8
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0
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20
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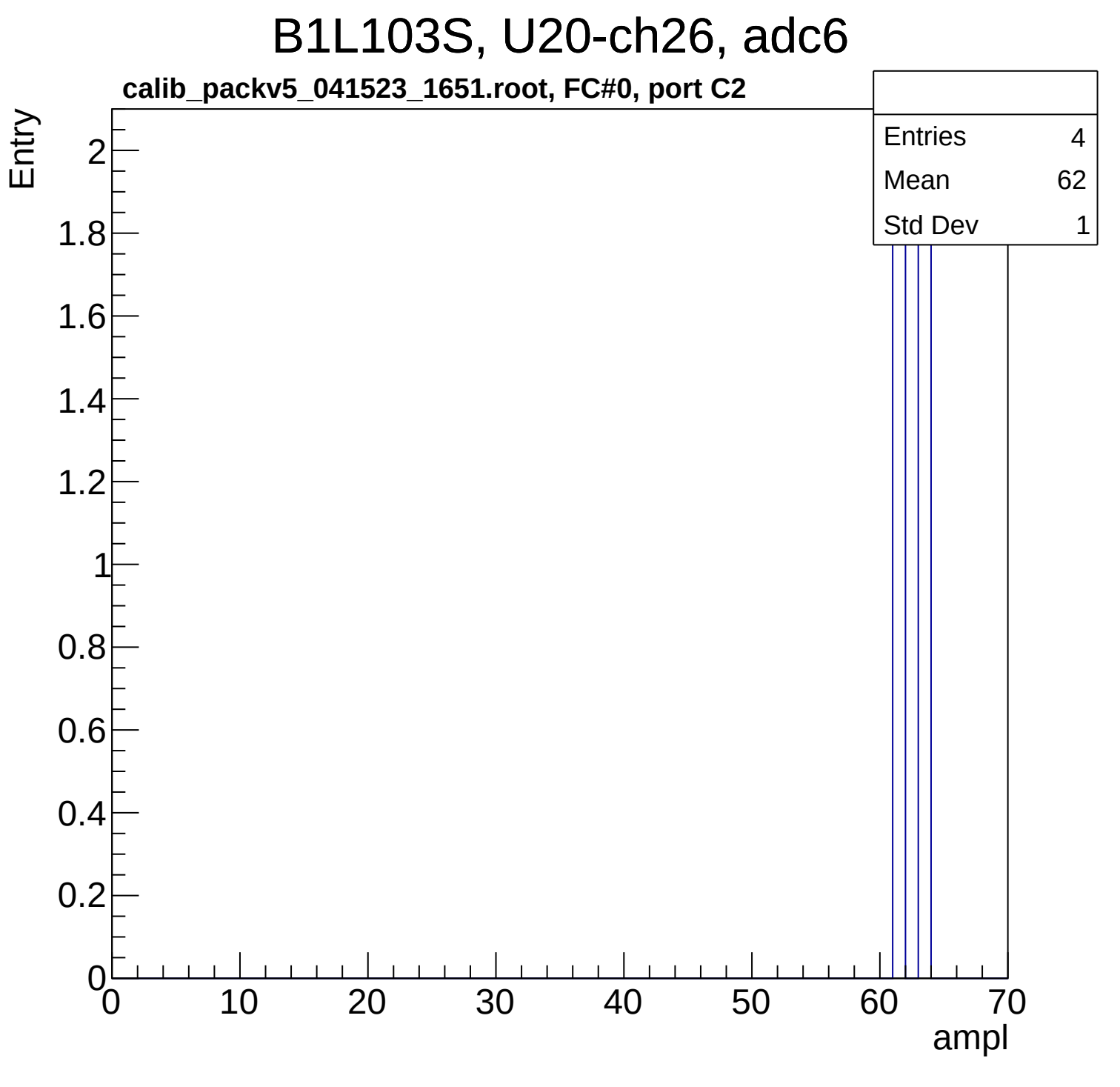
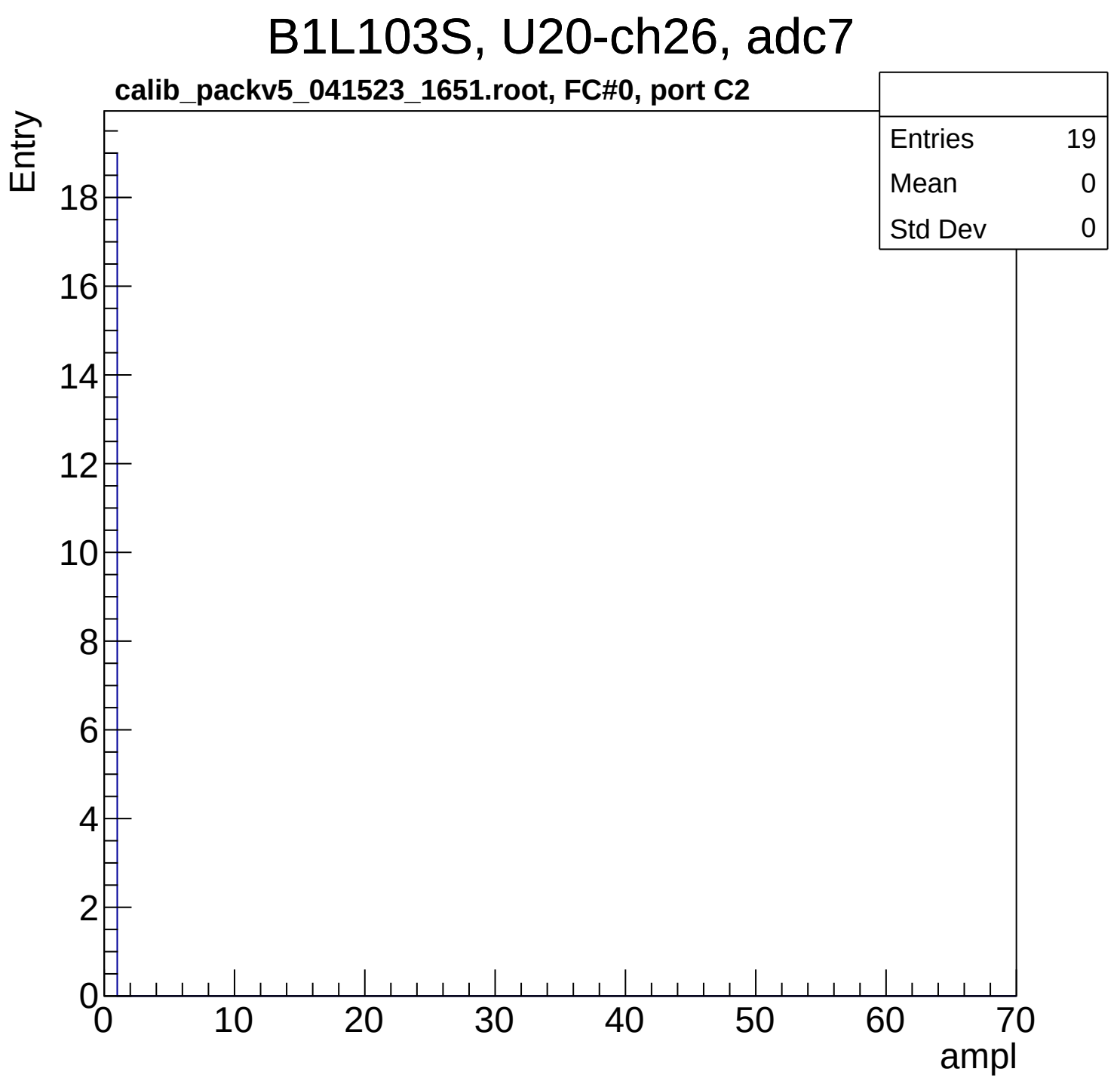
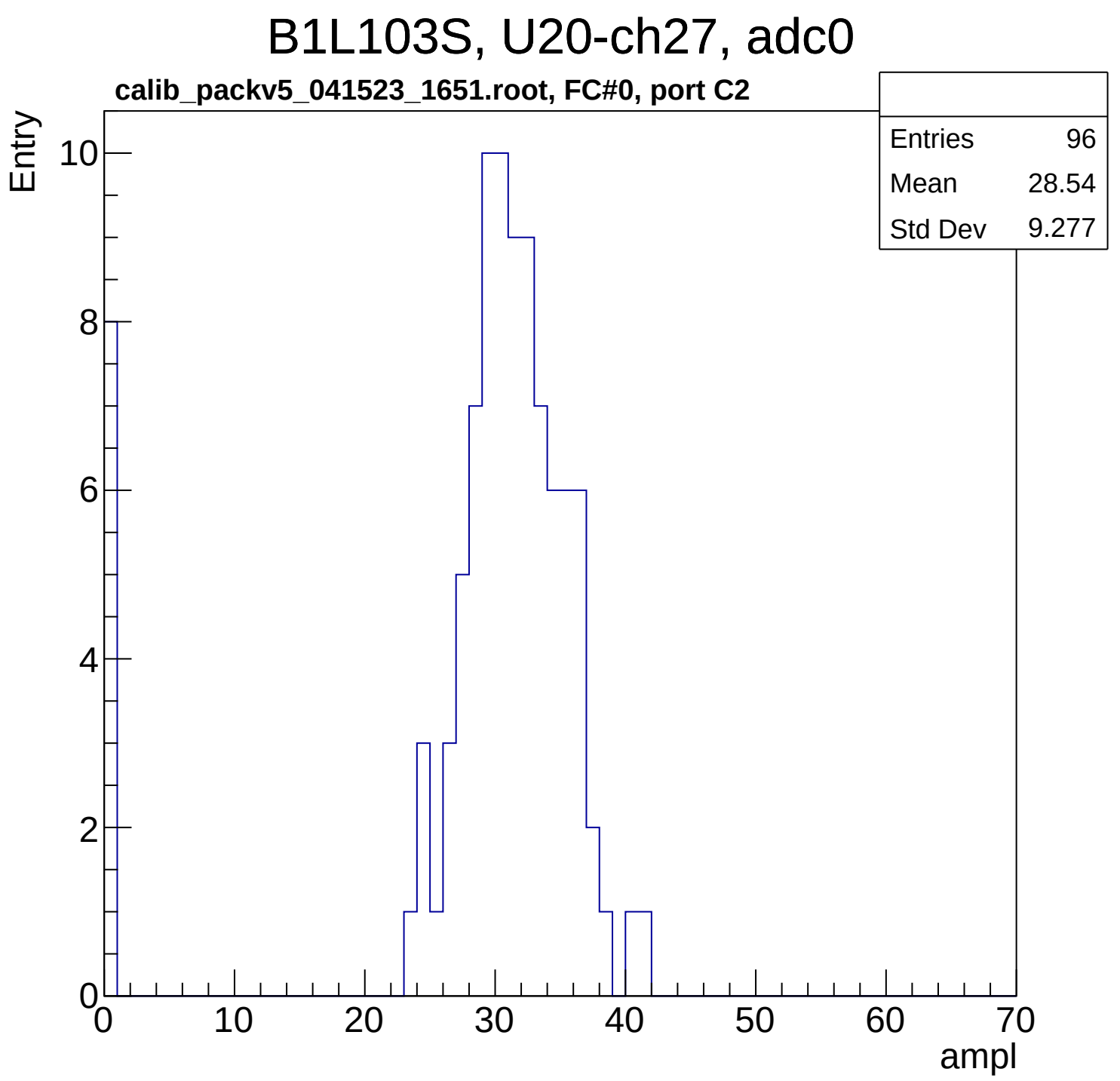
40
50
60
70


B1L103S, U20-ch26, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 62
Std Dev 1
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U20-ch26, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch27, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 96
Mean 28.54
Std Dev 9.277
Entry
0
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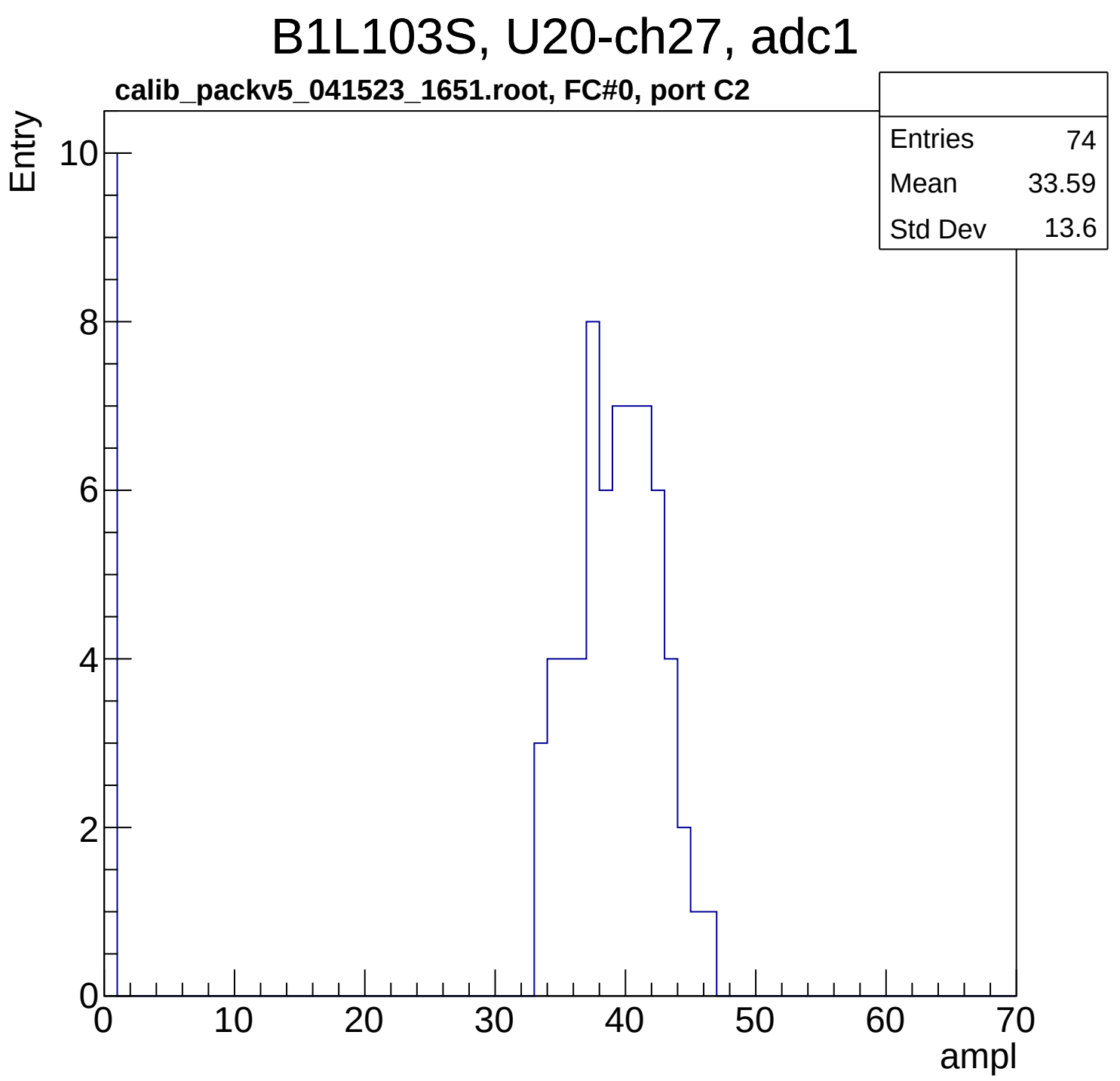
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch27, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 33.59
Std Dev 13.6
Entry
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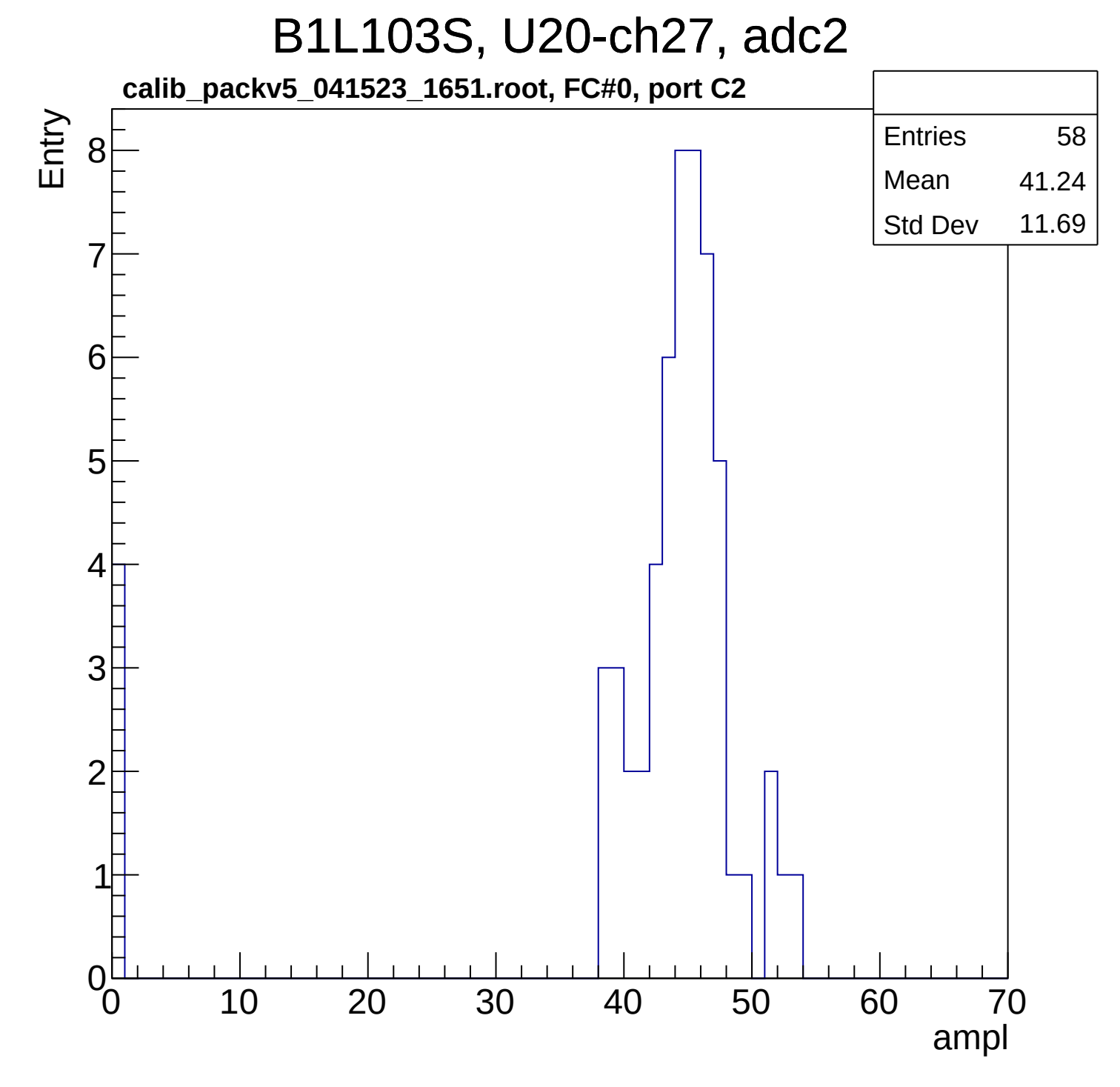
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch27, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 41.24
Std Dev 11.69
Entry
ampl
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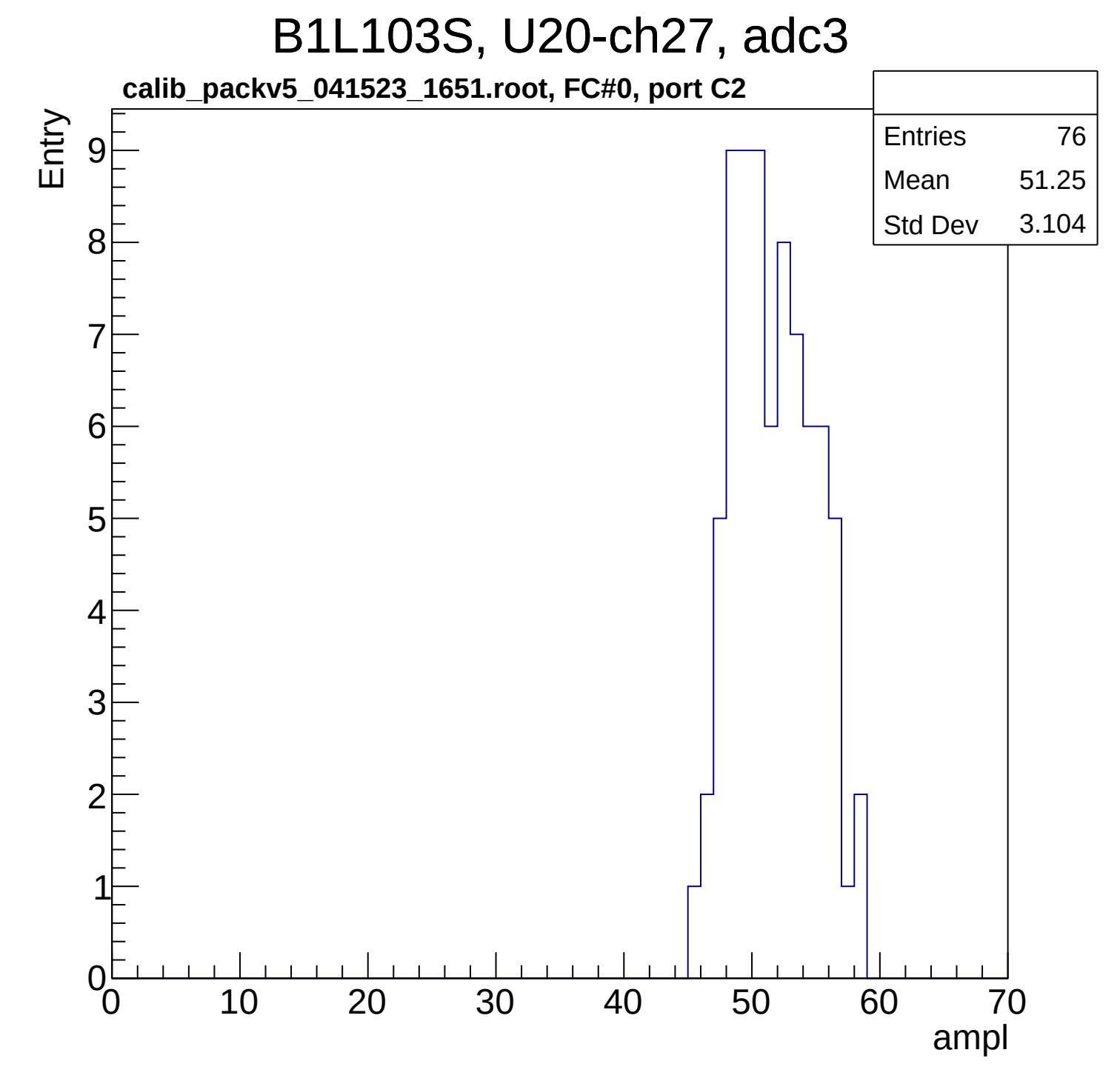
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch27, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 51.25
Std Dev 3.104
Entry
ampl
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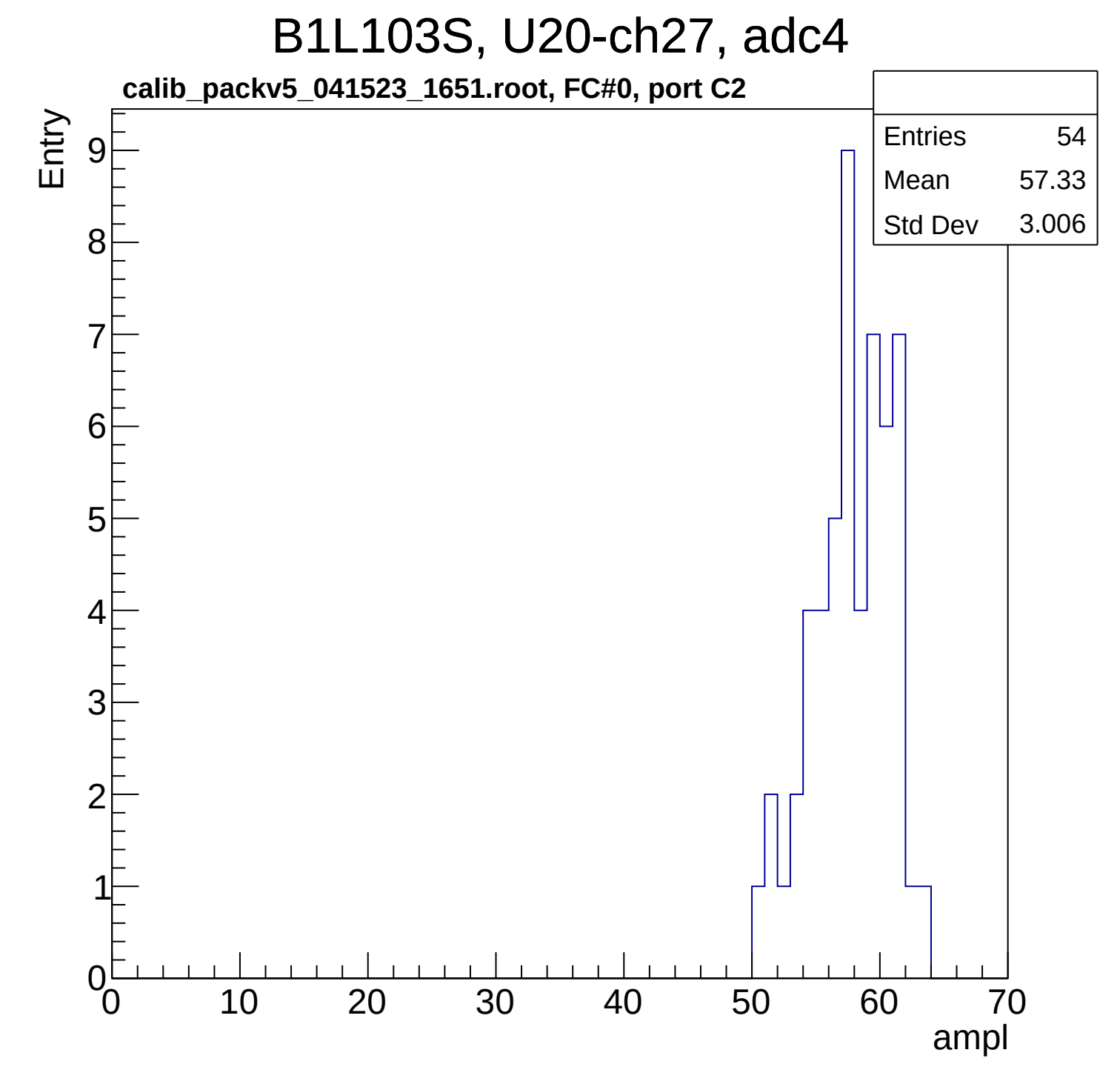
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch27, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 57.33
Std Dev 3.006
Entry
ampl
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2
3
4
5
6
7
8
9
0
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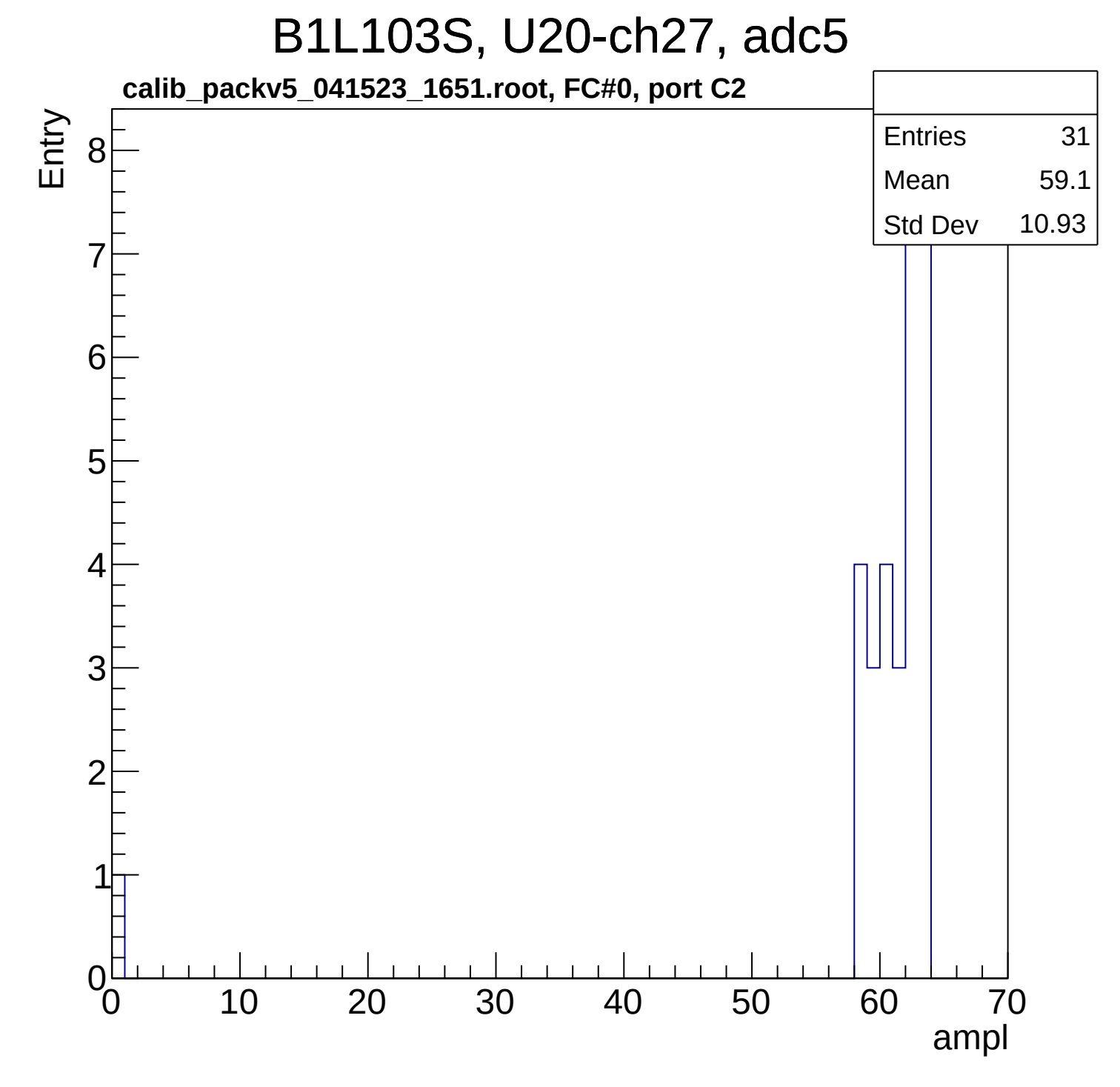
B1L103S, U20-ch27, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 59.1
Std Dev 10.93
Entry
ampl
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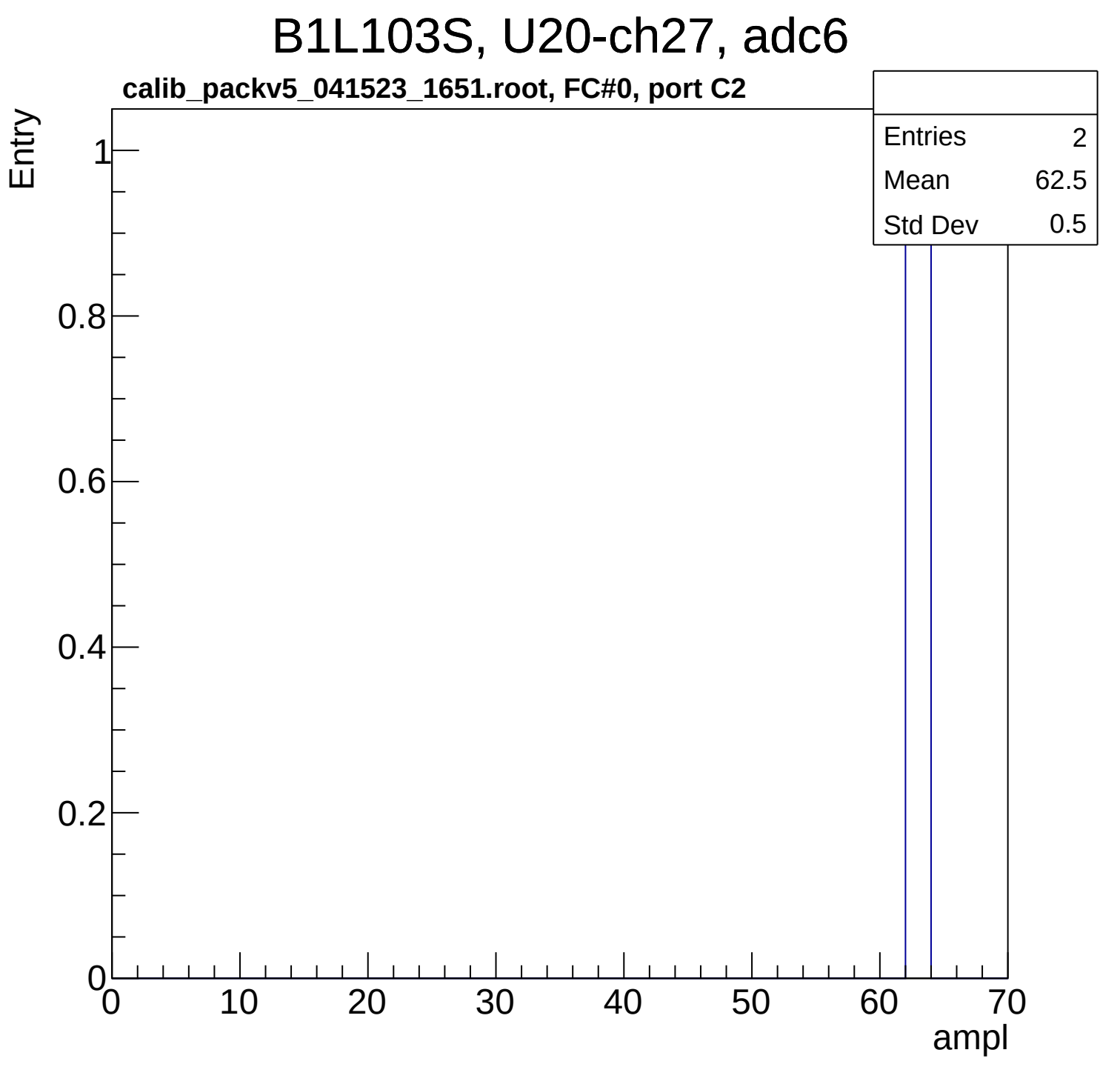
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch27, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
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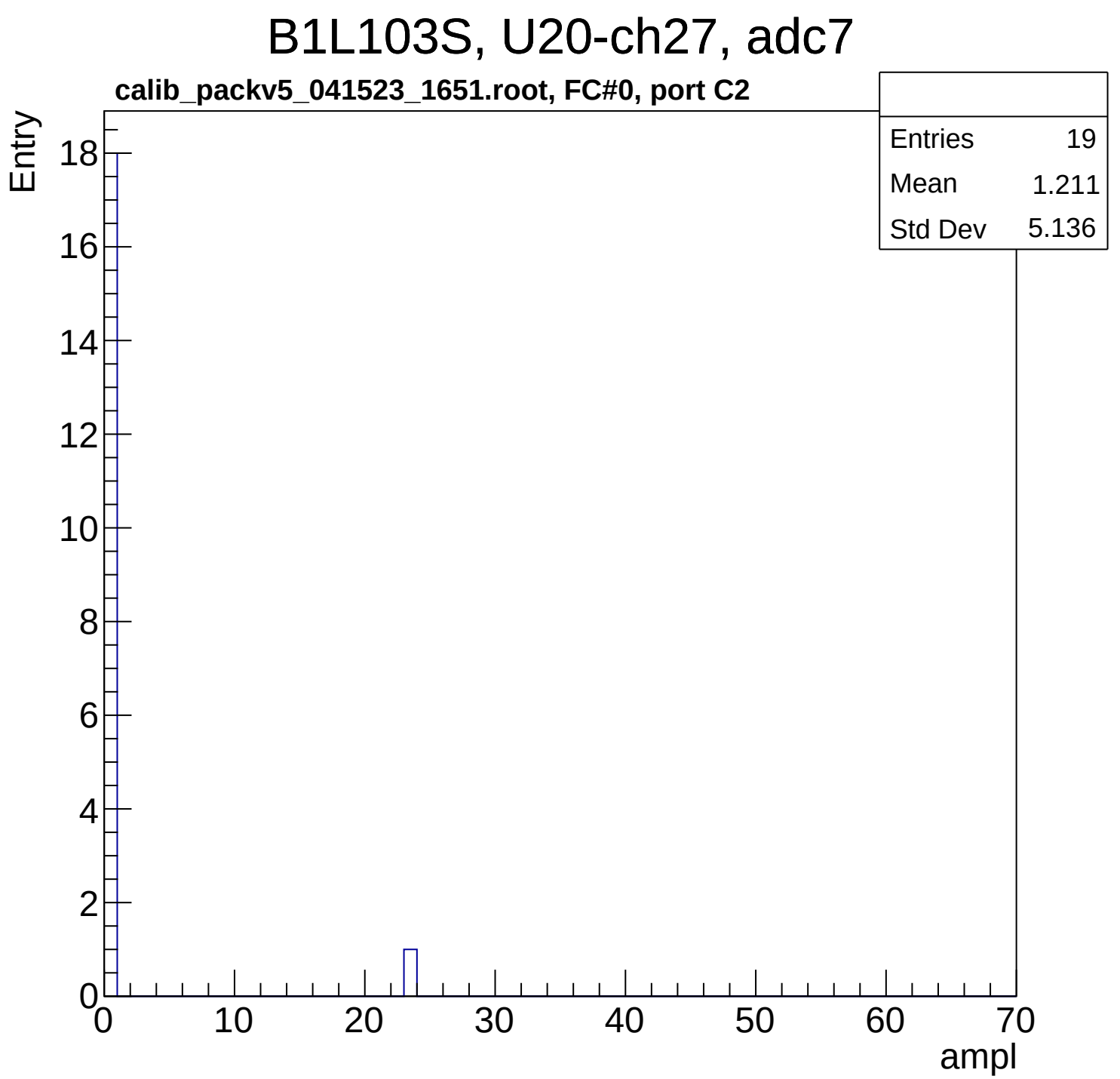
70
ampl


B1L103S, U20-ch27, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.211
Std Dev 5.136
Entry
0
2
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6
8
10
12
14
16
18
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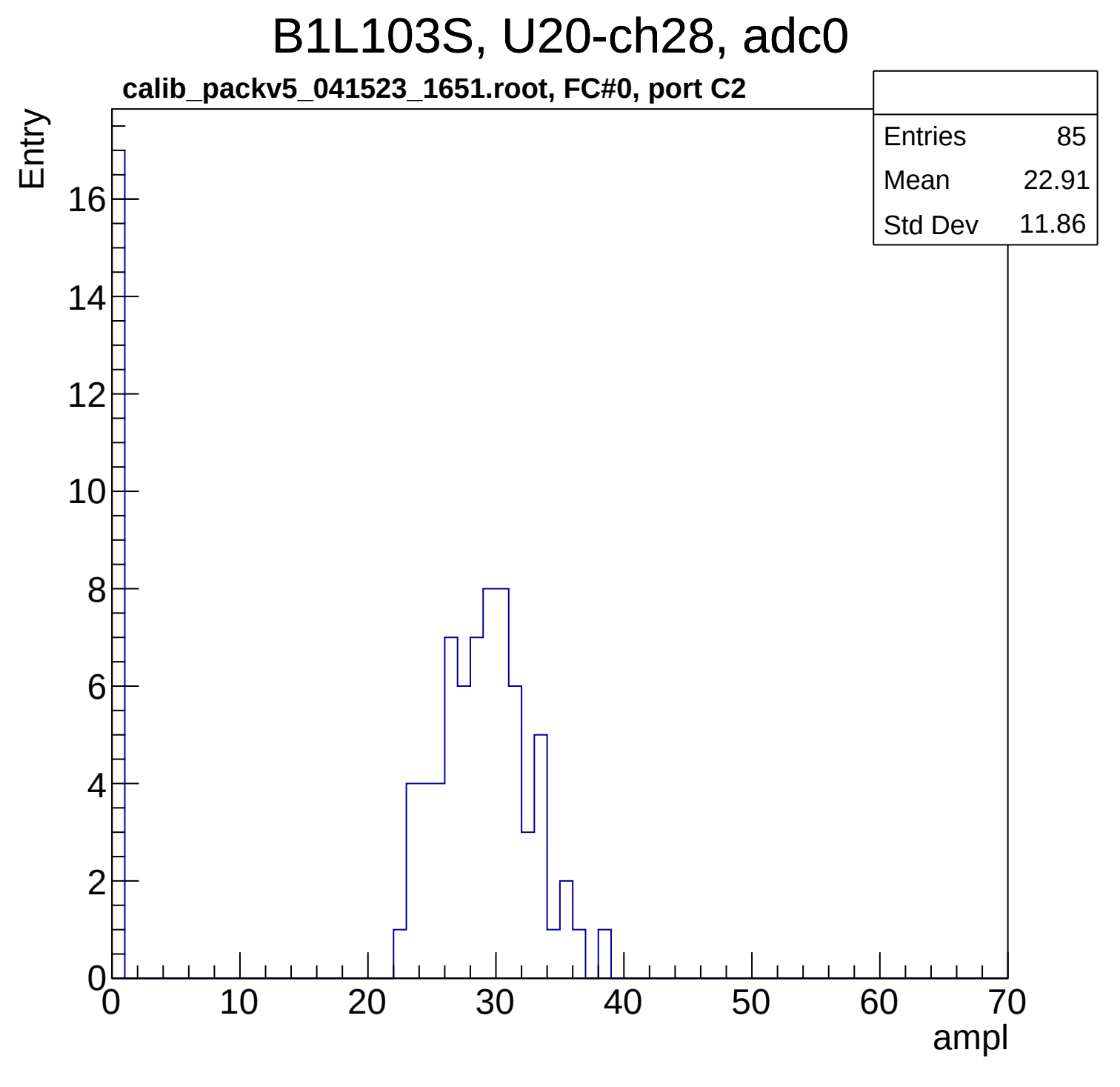
70
ampl


B1L103S, U20-ch28, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 22.91
Std Dev 11.86
Entry
0
2
4
6
8
10
12
14
16
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10
20
30
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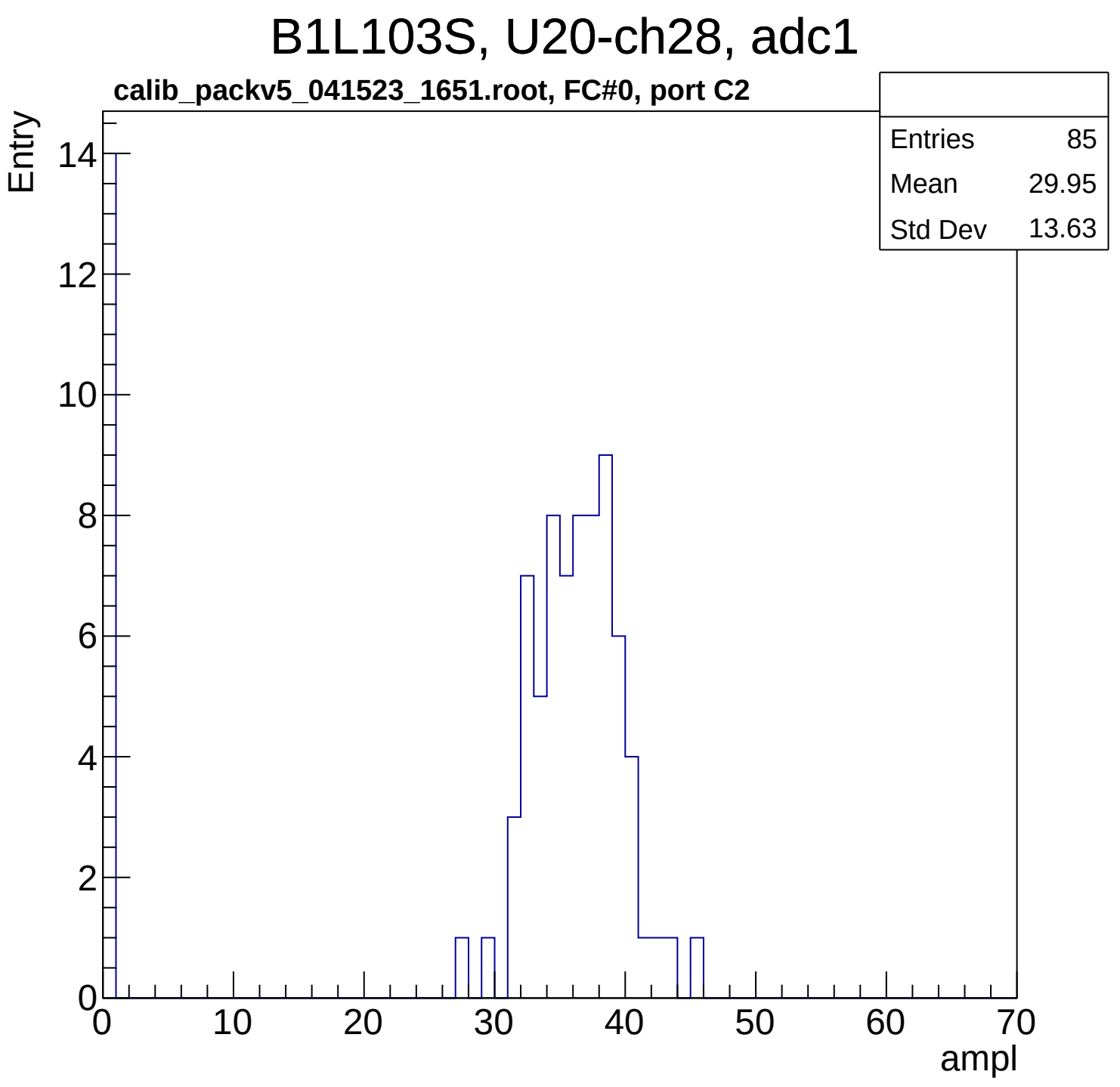
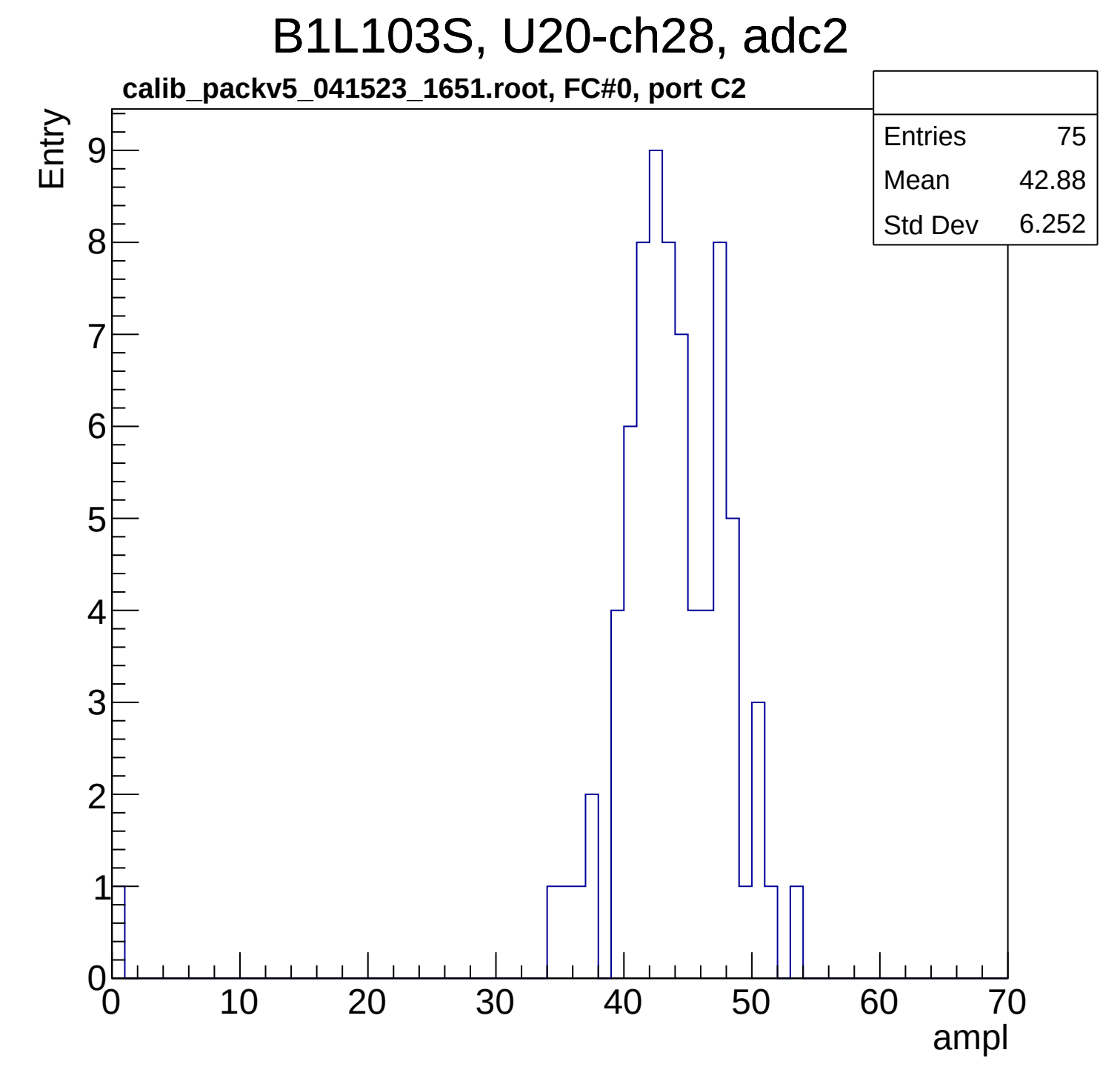
50
60
70
ampl


B1L103S, U20-ch28, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 29.95
Std Dev 13.63
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch28, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 42.88
Std Dev 6.252
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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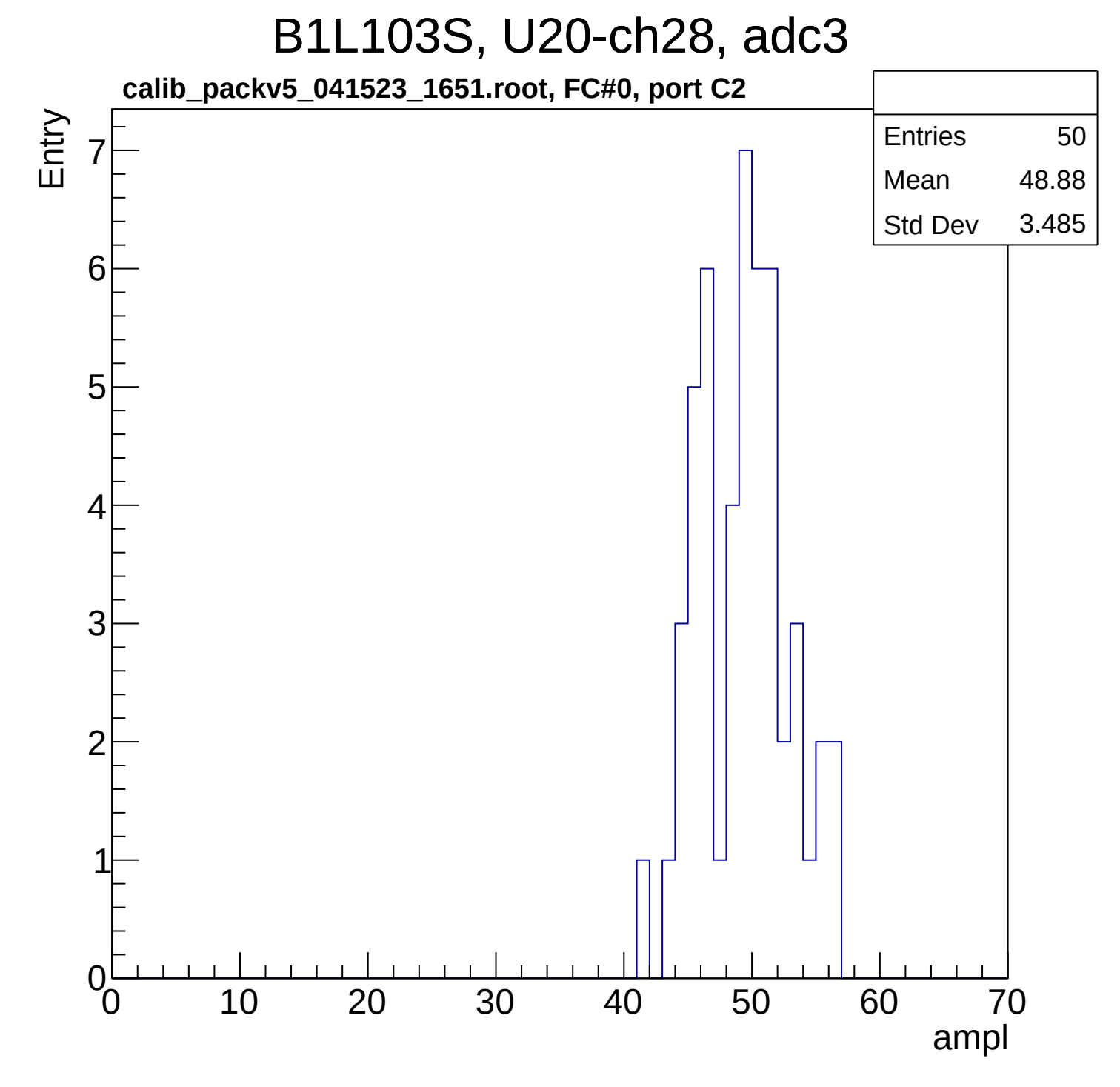
40
50
60
70


B1L103S, U20-ch28, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 48.88
Std Dev 3.485
Entry
ampl
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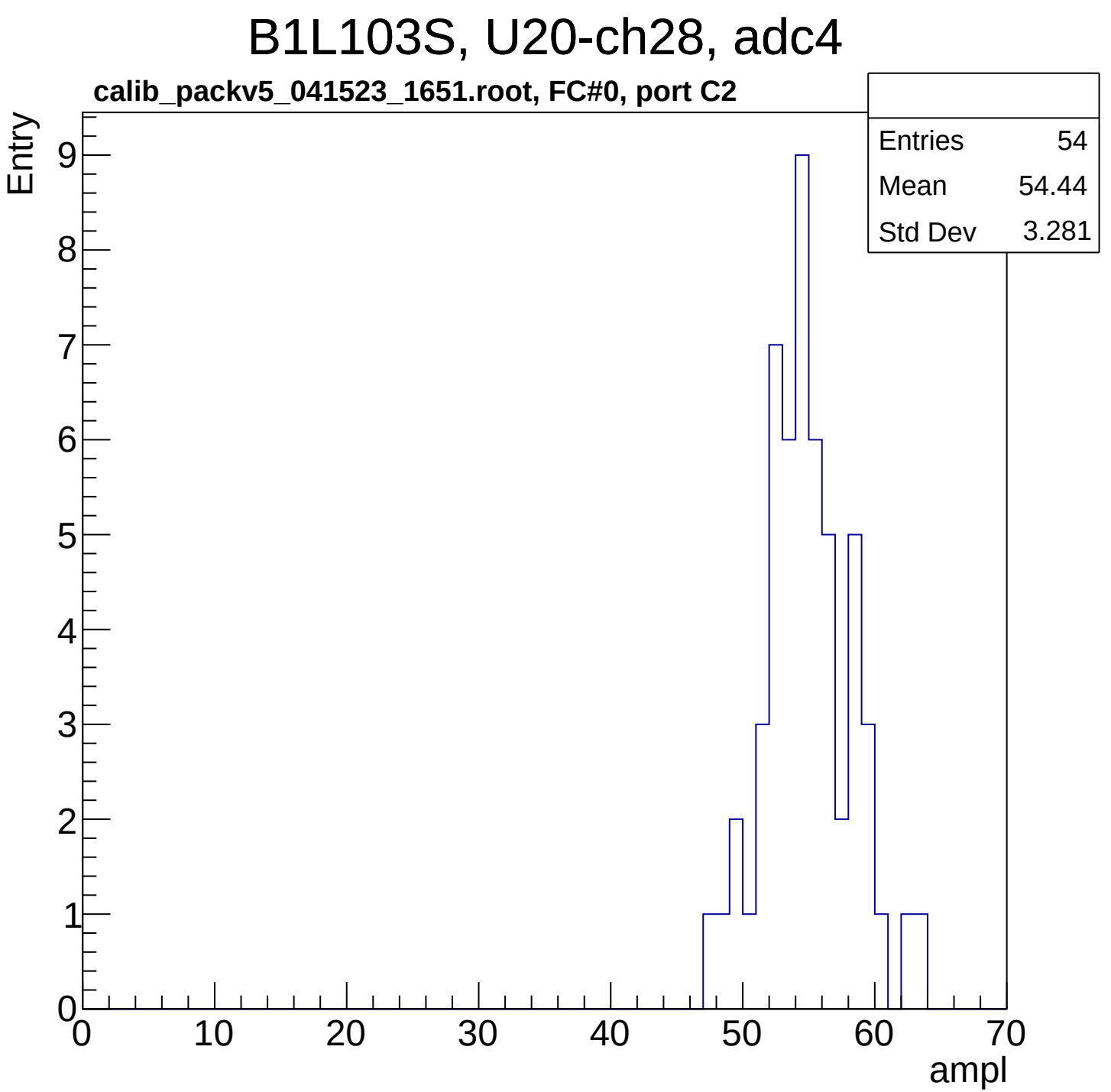
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U20-ch28, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 54.44
Std Dev 3.281
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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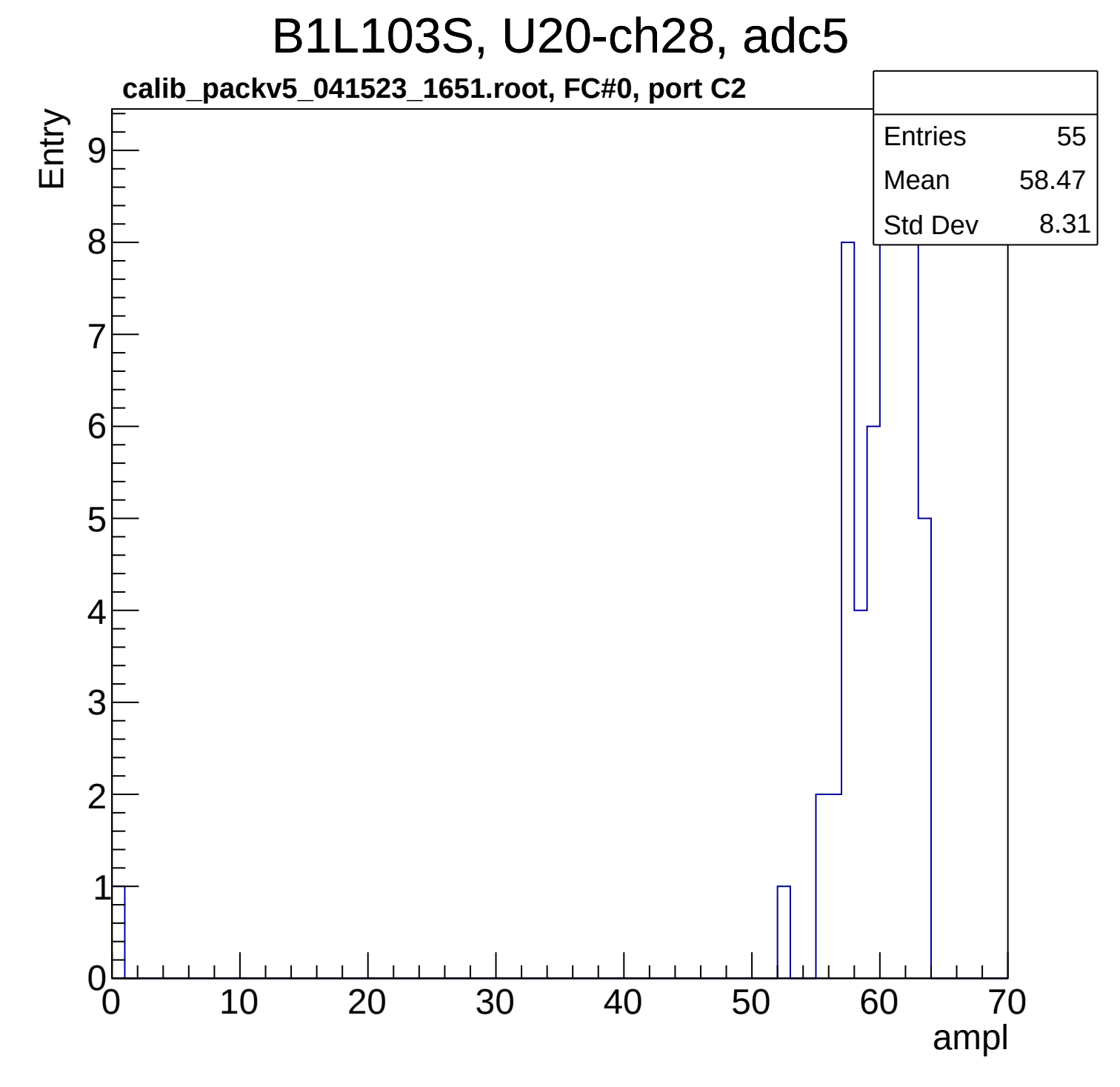
B1L103S, U20-ch28, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 58.47
Std Dev 8.31
Entry
ampl
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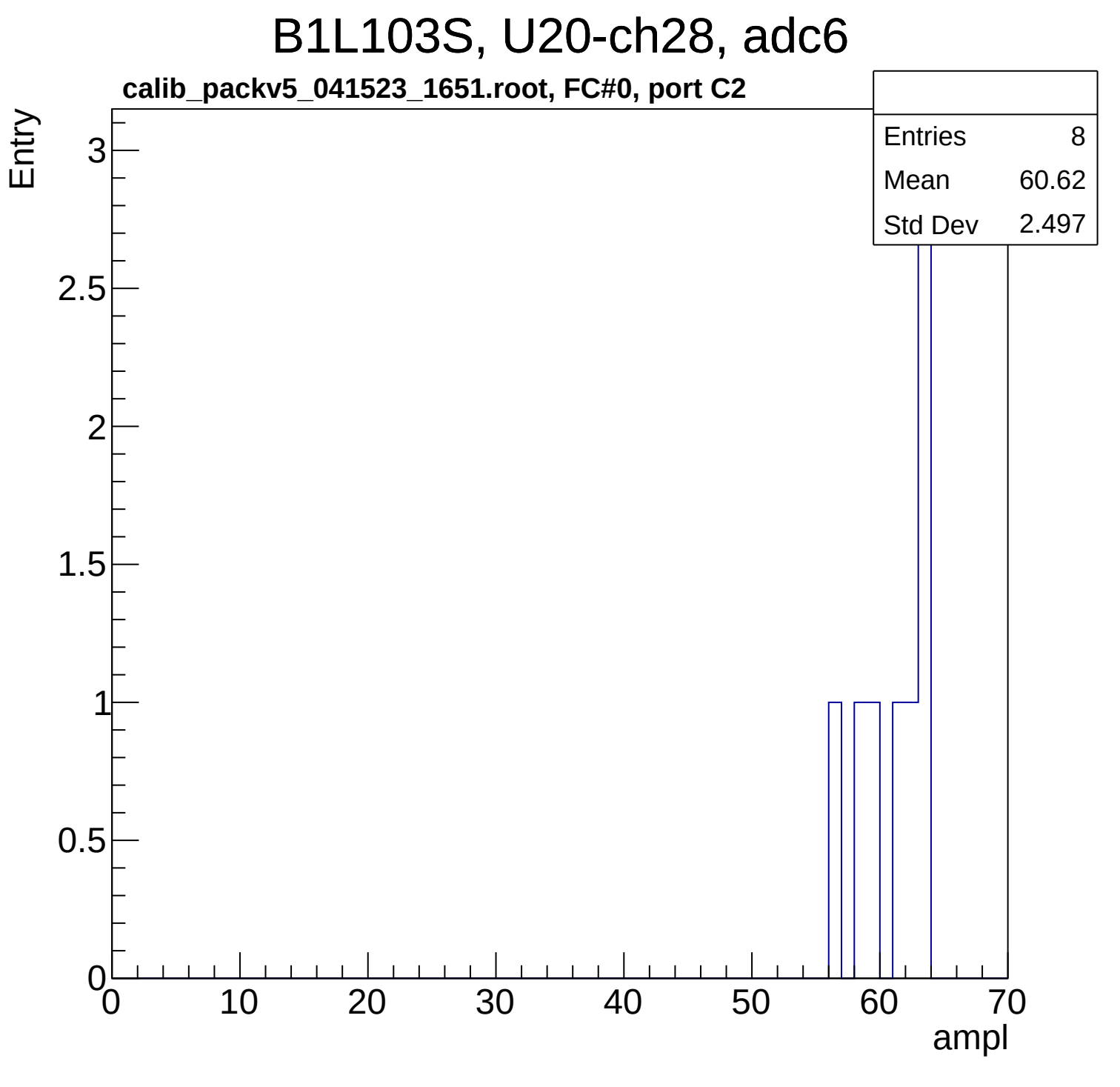
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch28, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 60.62
Std Dev 2.497
Entry
ampl
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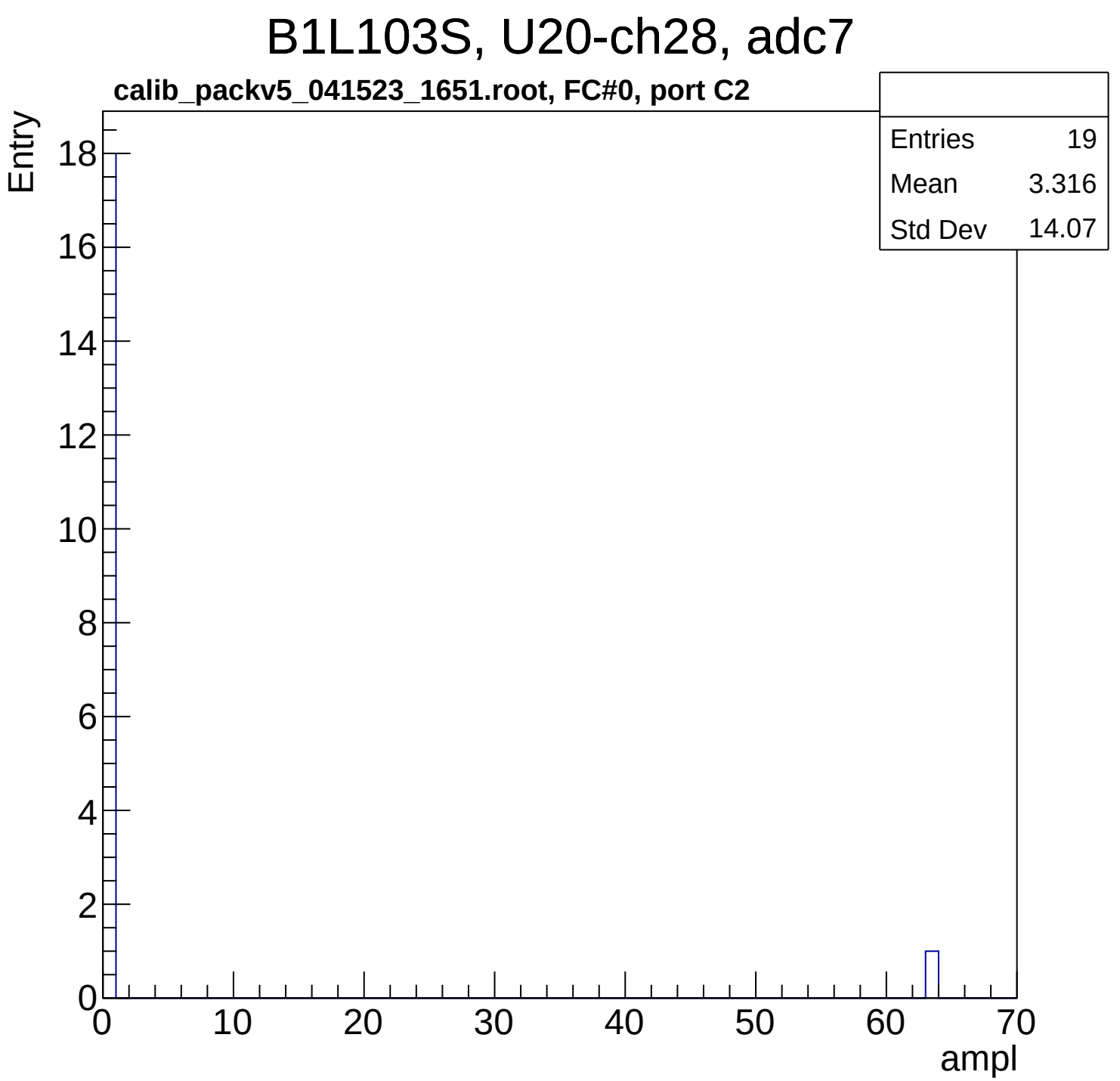
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U20-ch28, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.316
Std Dev 14.07
Entry
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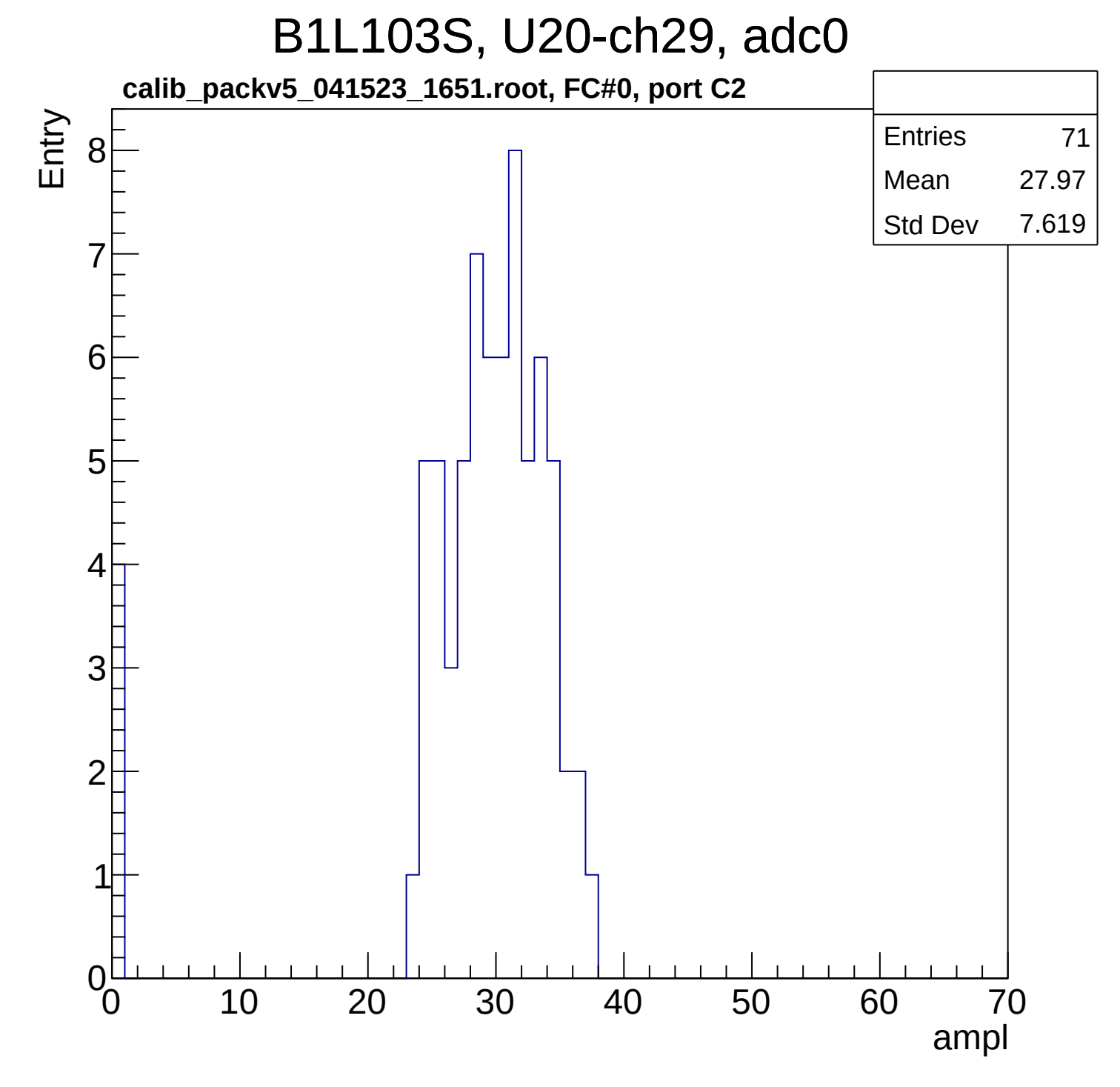
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch29, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 27.97
Std Dev 7.619
Entry
ampl
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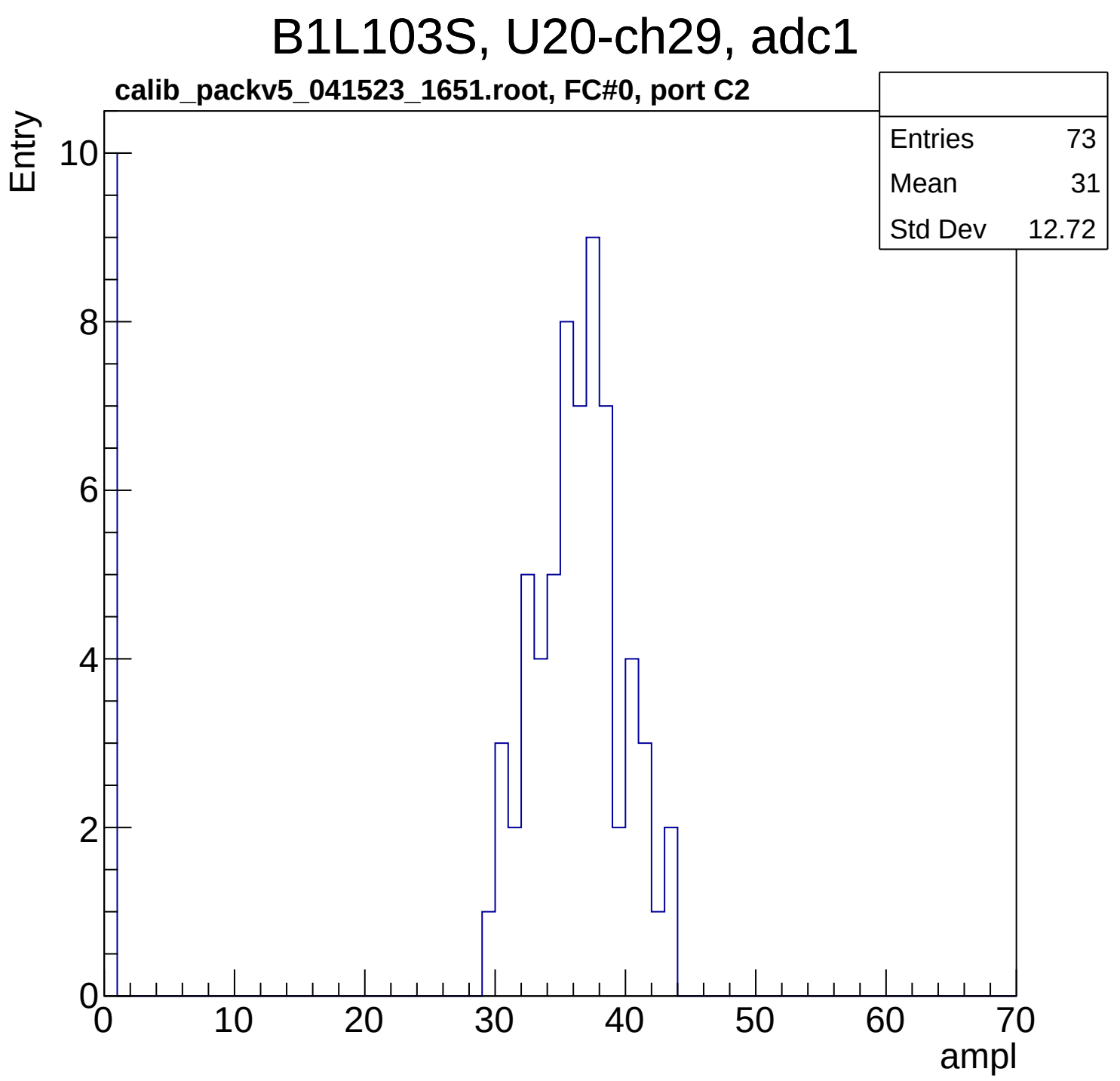
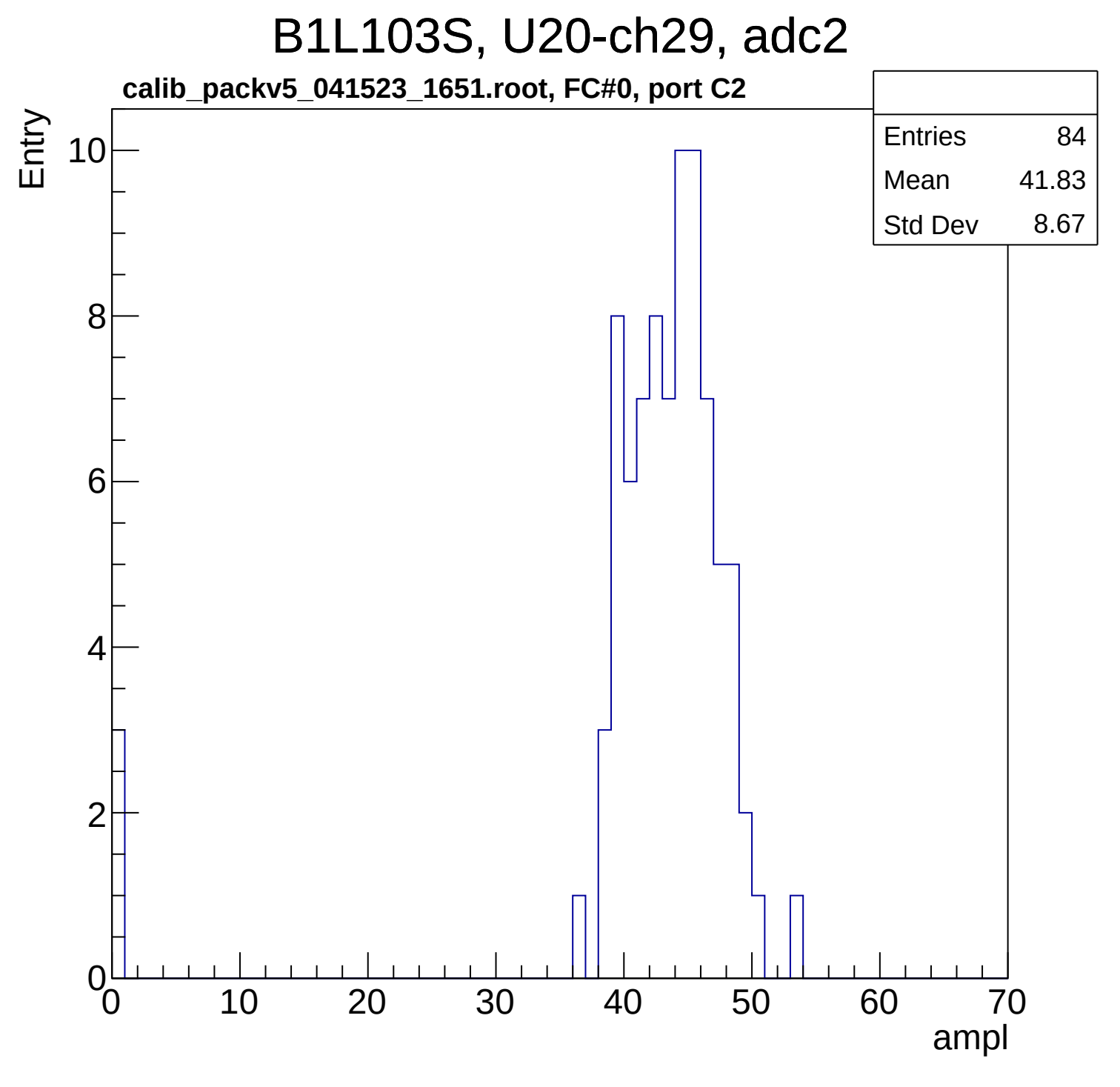
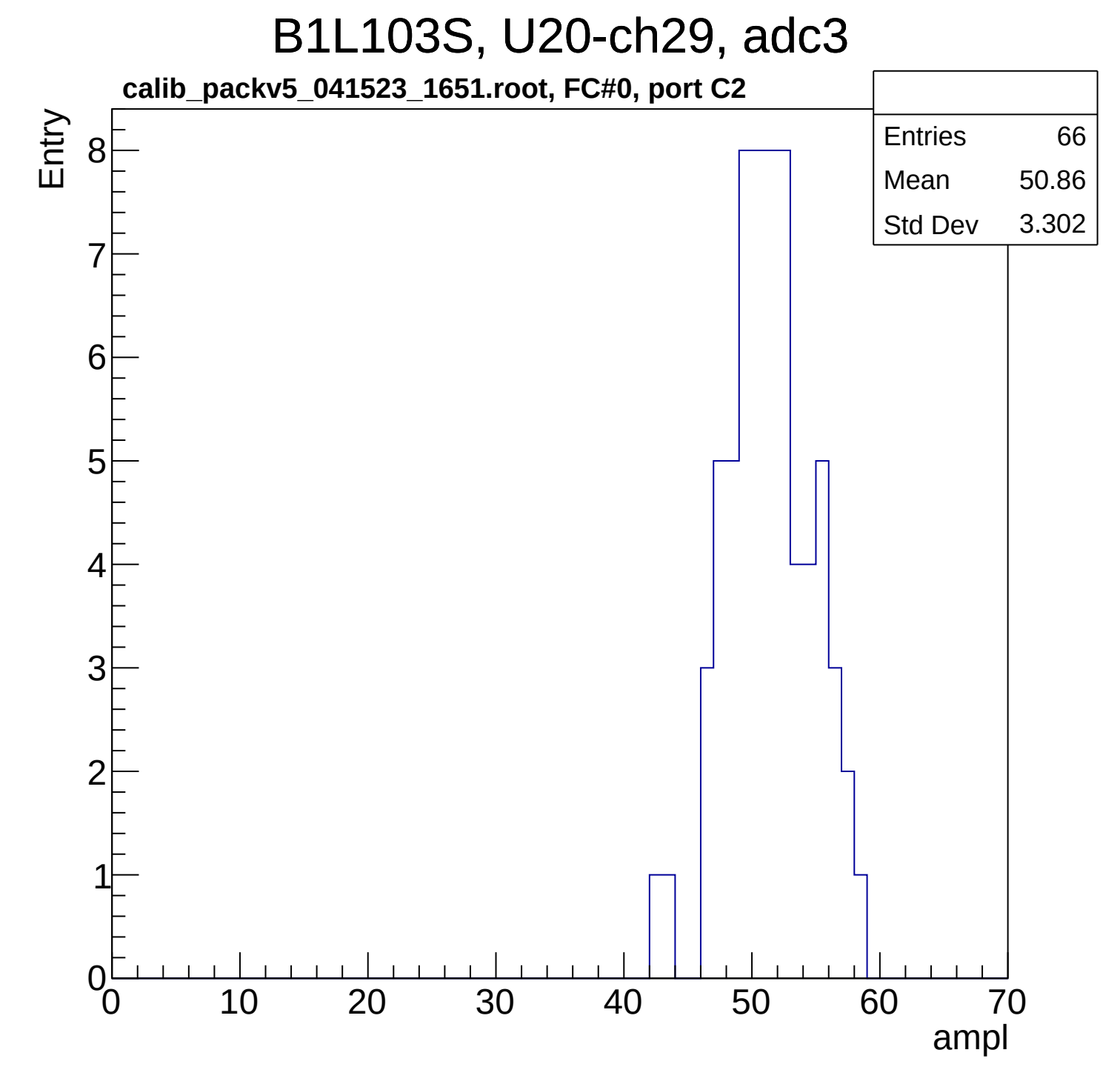
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch29, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 31
Std Dev 12.72
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U20-ch29, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 41.83
Std Dev 8.67
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U20-ch29, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 50.86
Std Dev 3.302
Entry
ampl
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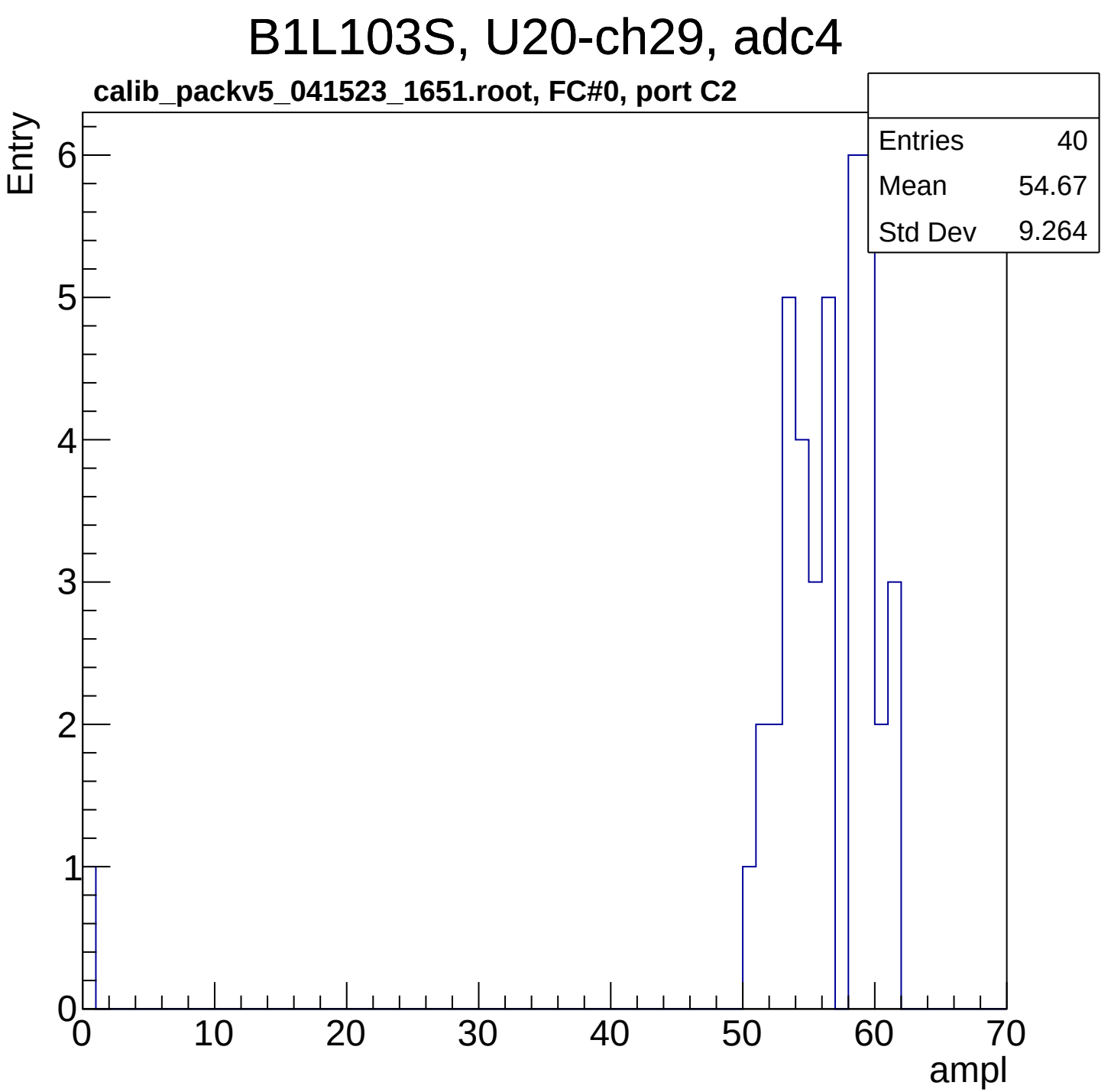
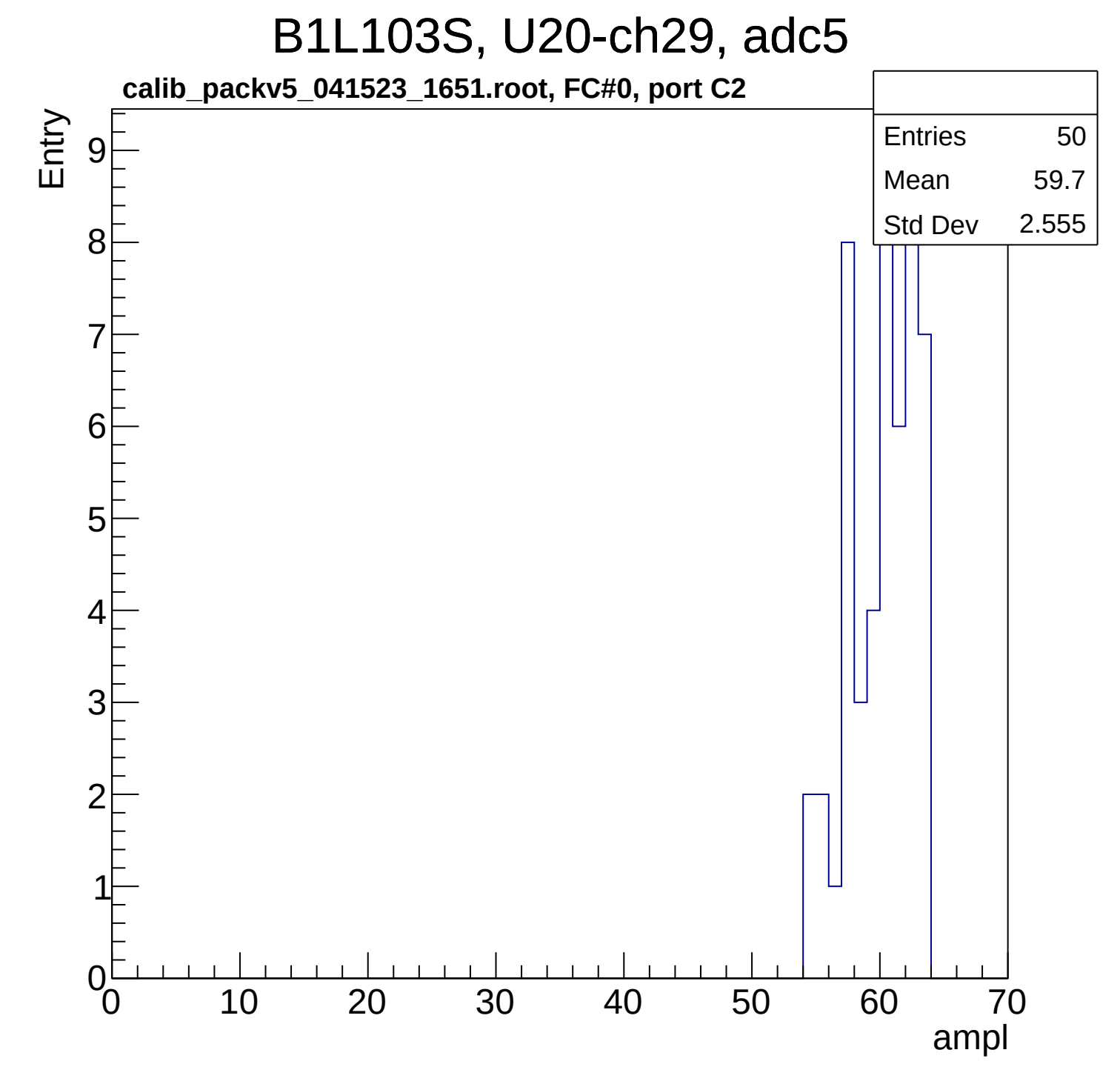
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch29, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 54.67
Std Dev 9.264
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U20-ch29, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 59.7
Std Dev 2.555
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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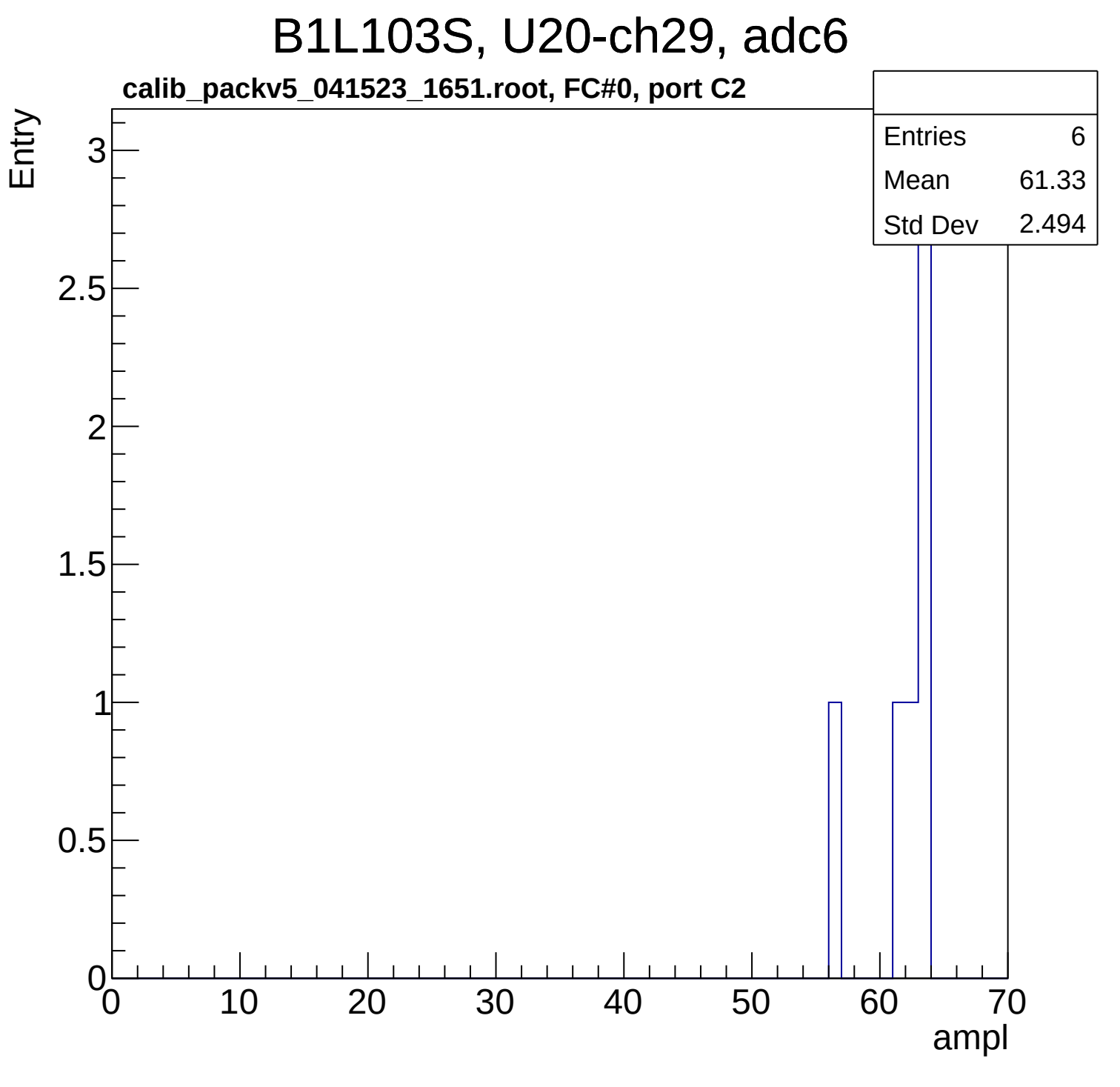
B1L103S, U20-ch29, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 61.33
Std Dev 2.494
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
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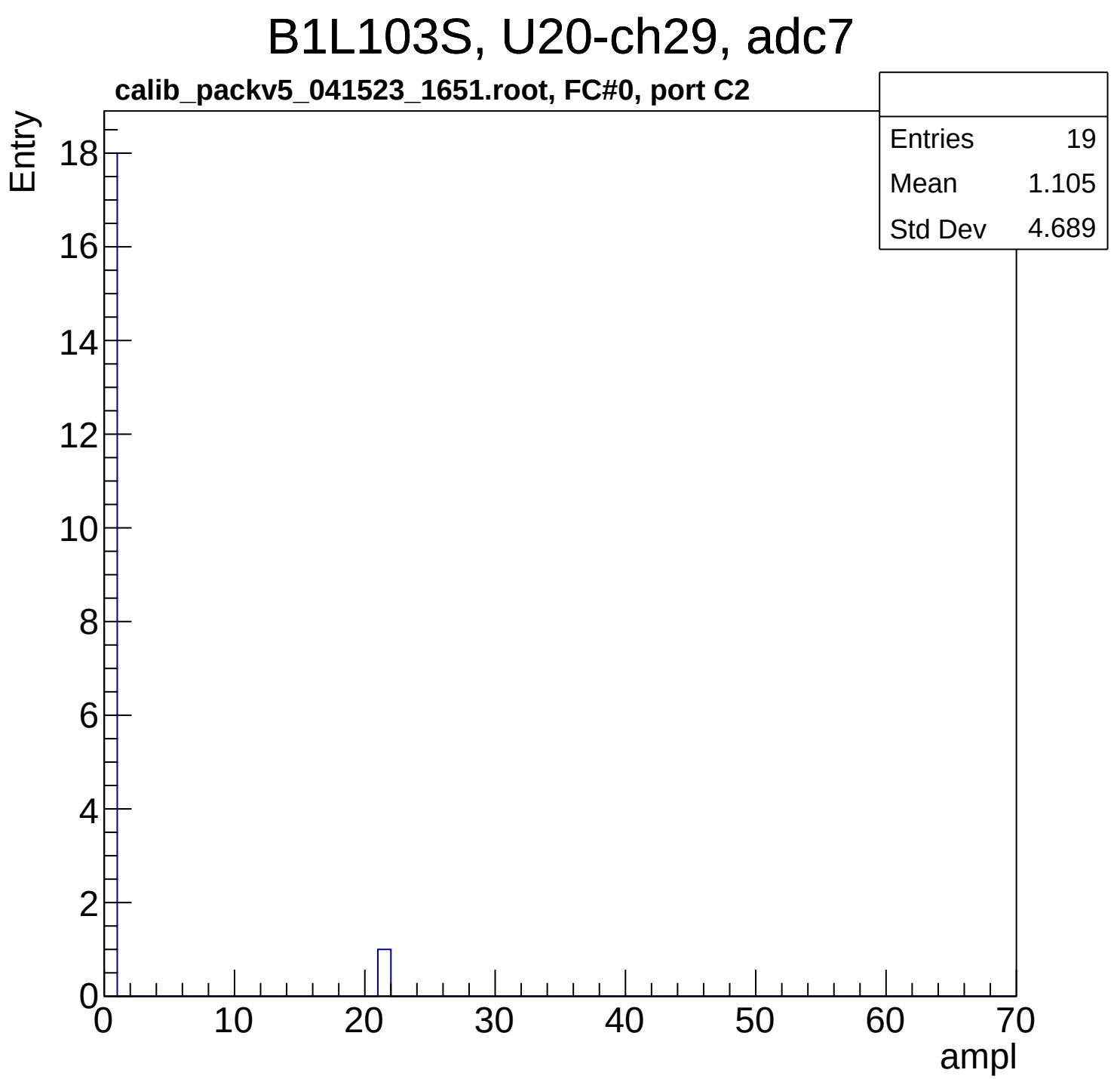
20
30
40
50
60
70


B1L103S, U20-ch29, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.105
Std Dev 4.689
Entry
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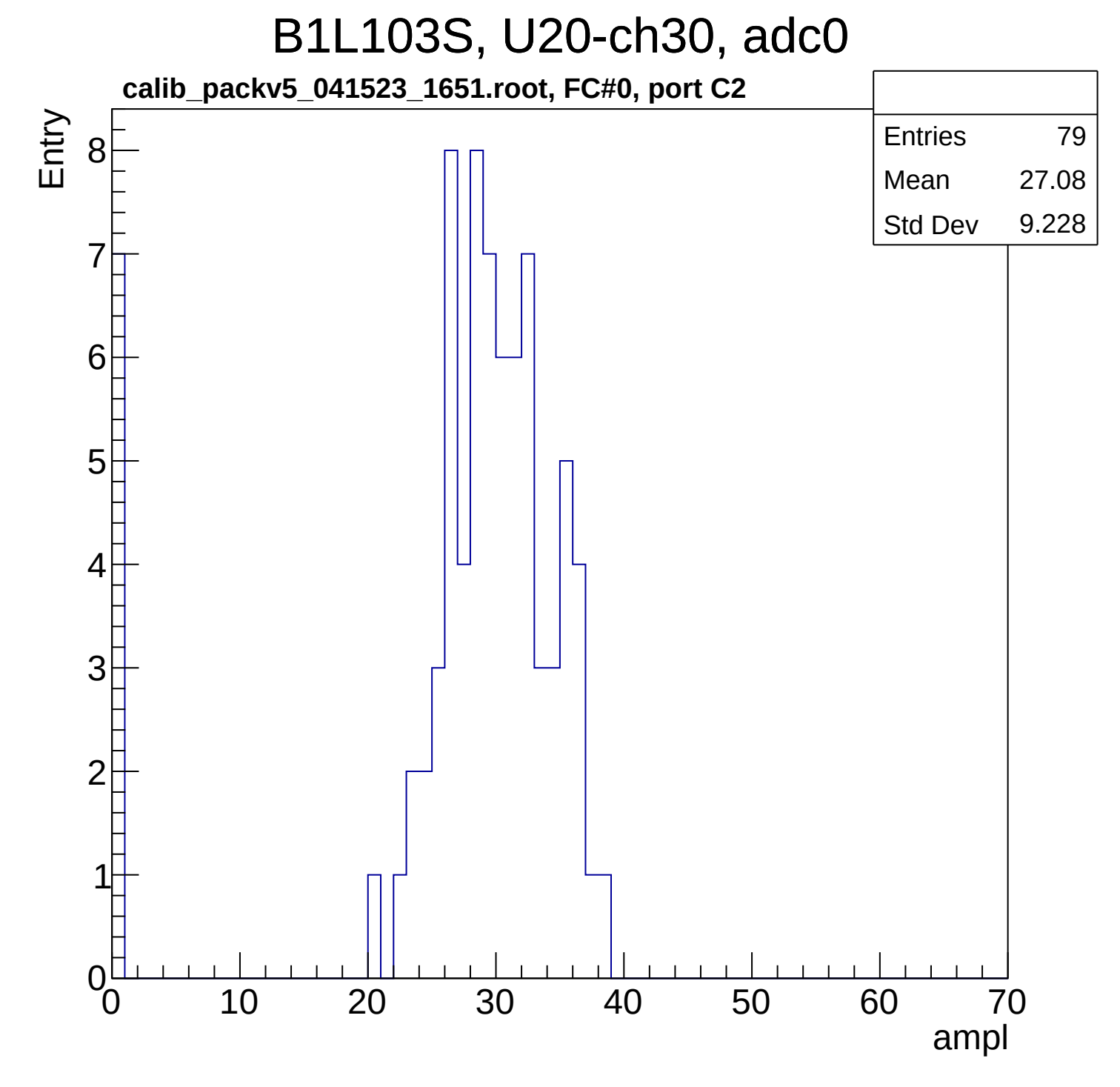
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch30, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 27.08
Std Dev 9.228
Entry
ampl
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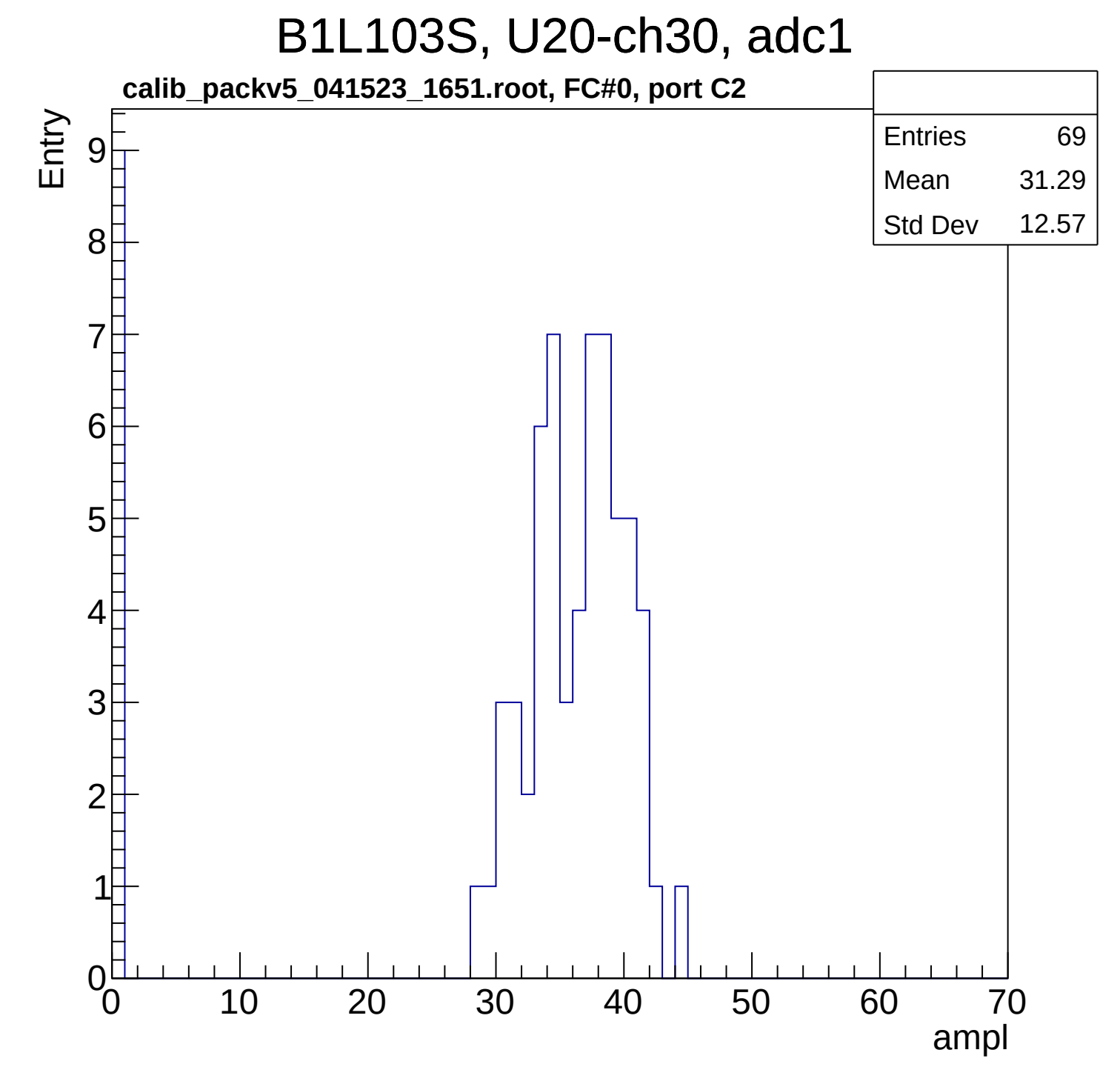
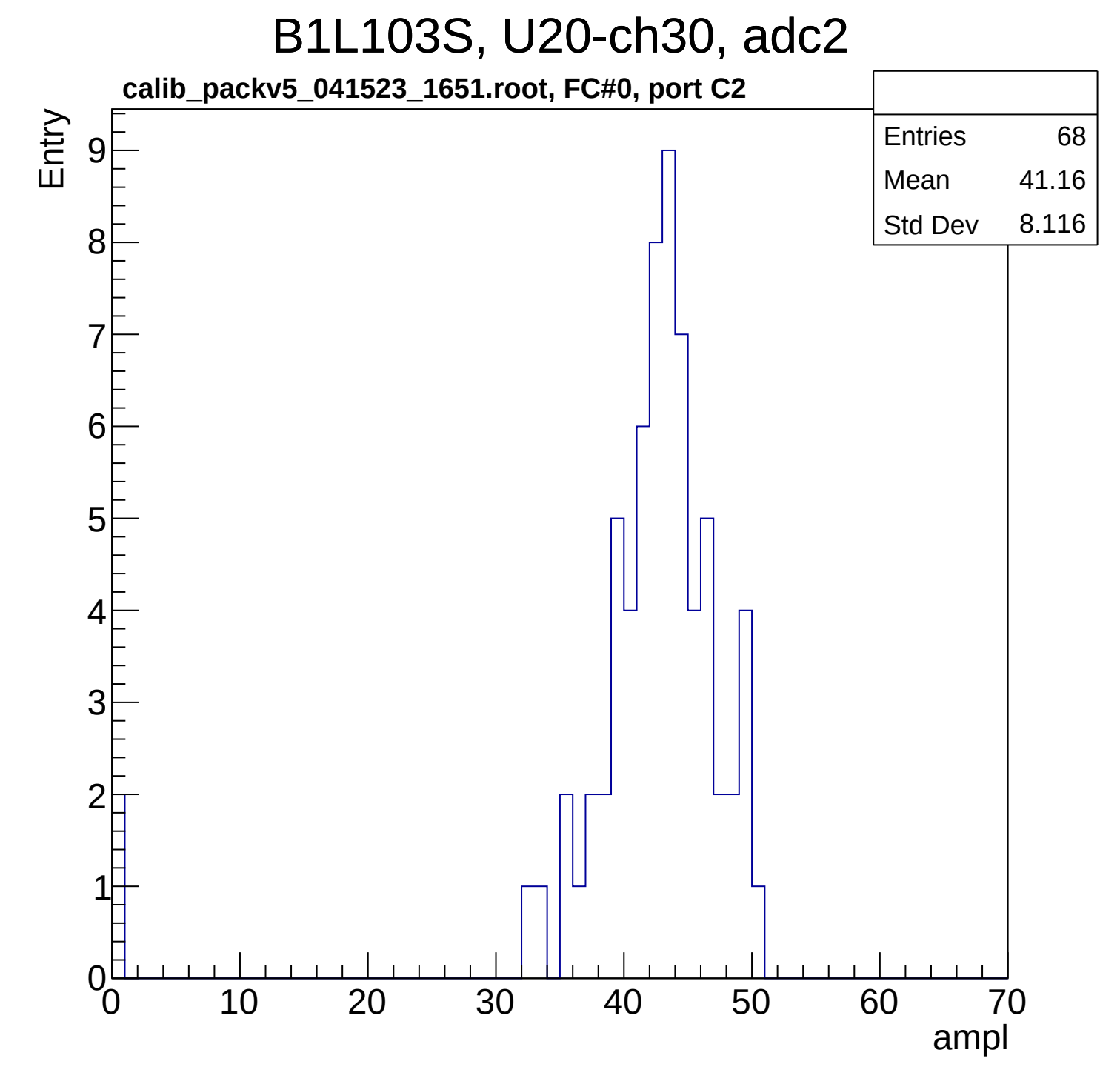
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch30, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 31.29
Std Dev 12.57
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch30, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 41.16
Std Dev 8.116
Entry
ampl
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3
4
5
6
7
8
9
0
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20
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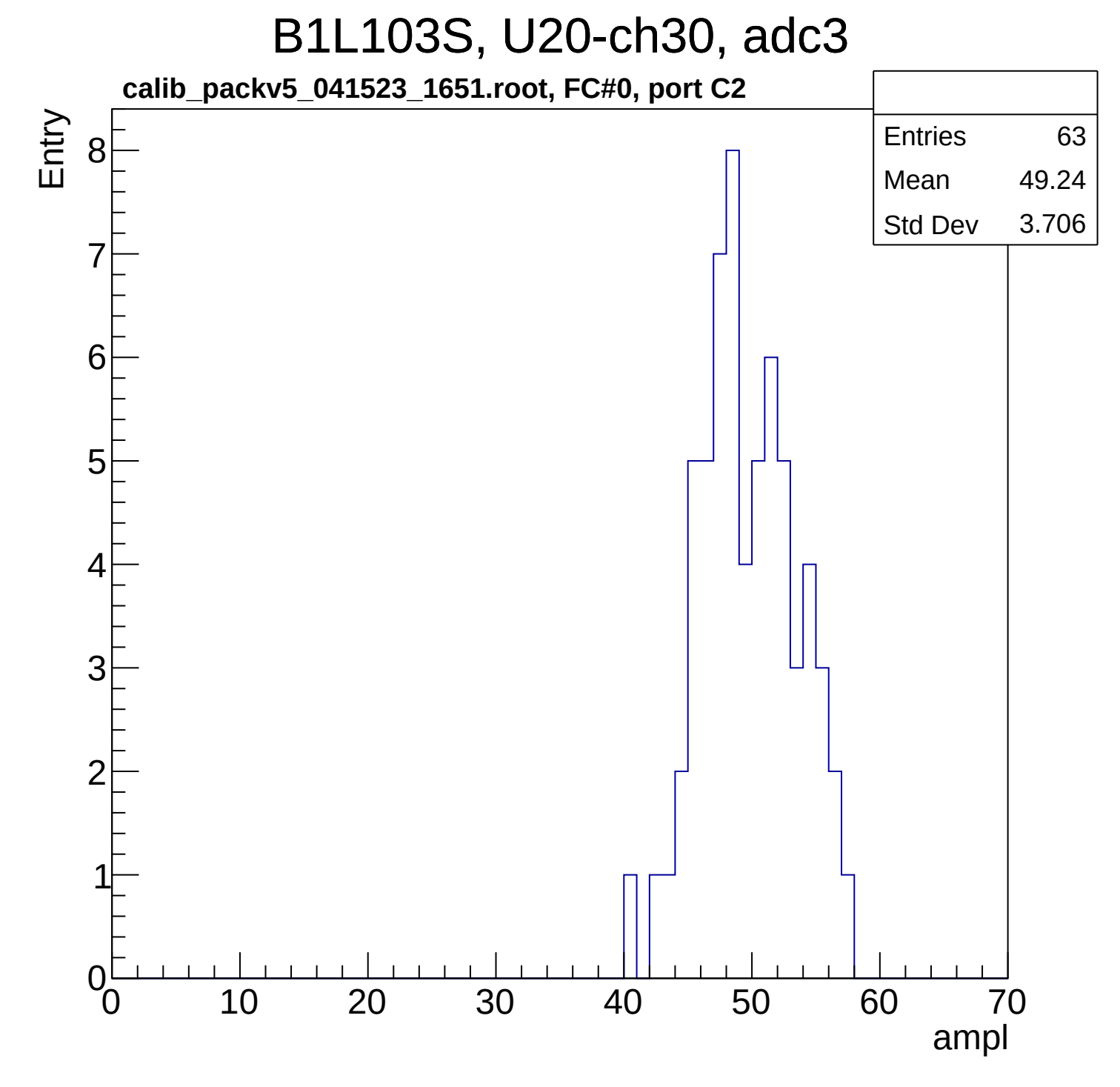
40
50
60
70


B1L103S, U20-ch30, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 49.24
Std Dev 3.706
Entry
ampl
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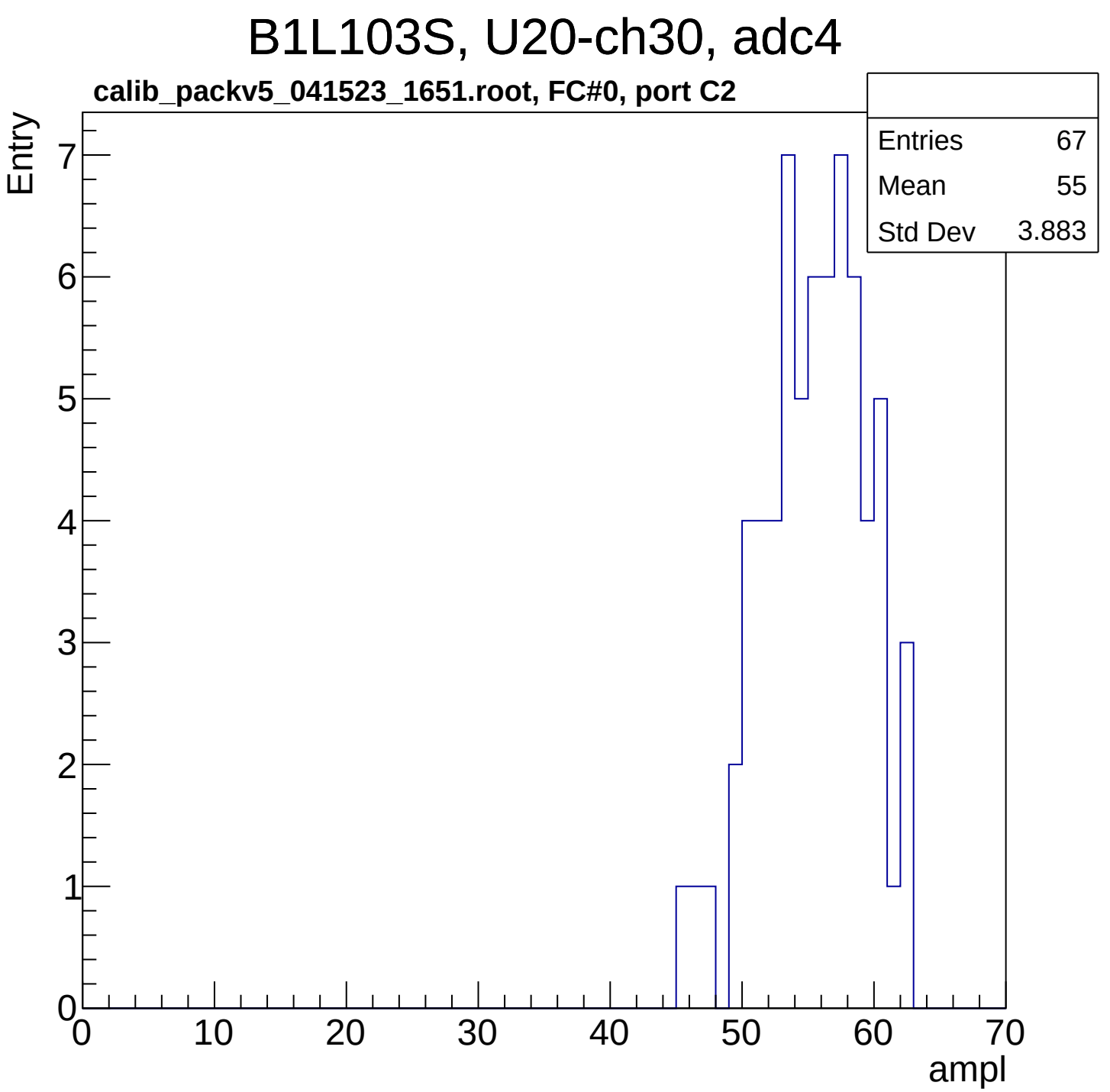
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch30, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 55
Std Dev 3.883
Entry
ampl
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1
2
3
4
5
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0
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20
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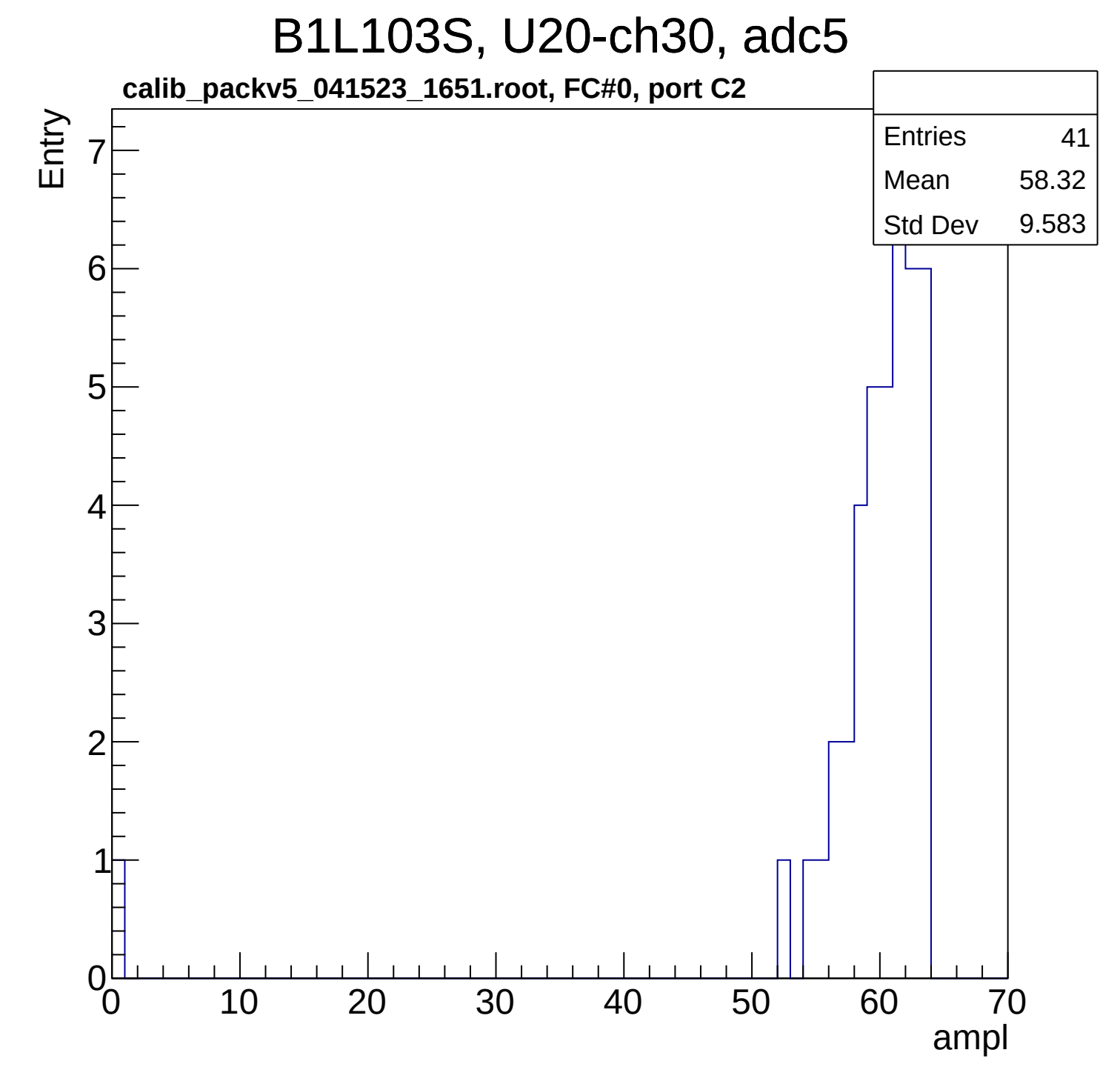
40
50
60
70


B1L103S, U20-ch30, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 58.32
Std Dev 9.583
Entry
ampl
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4
5
6
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0
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20
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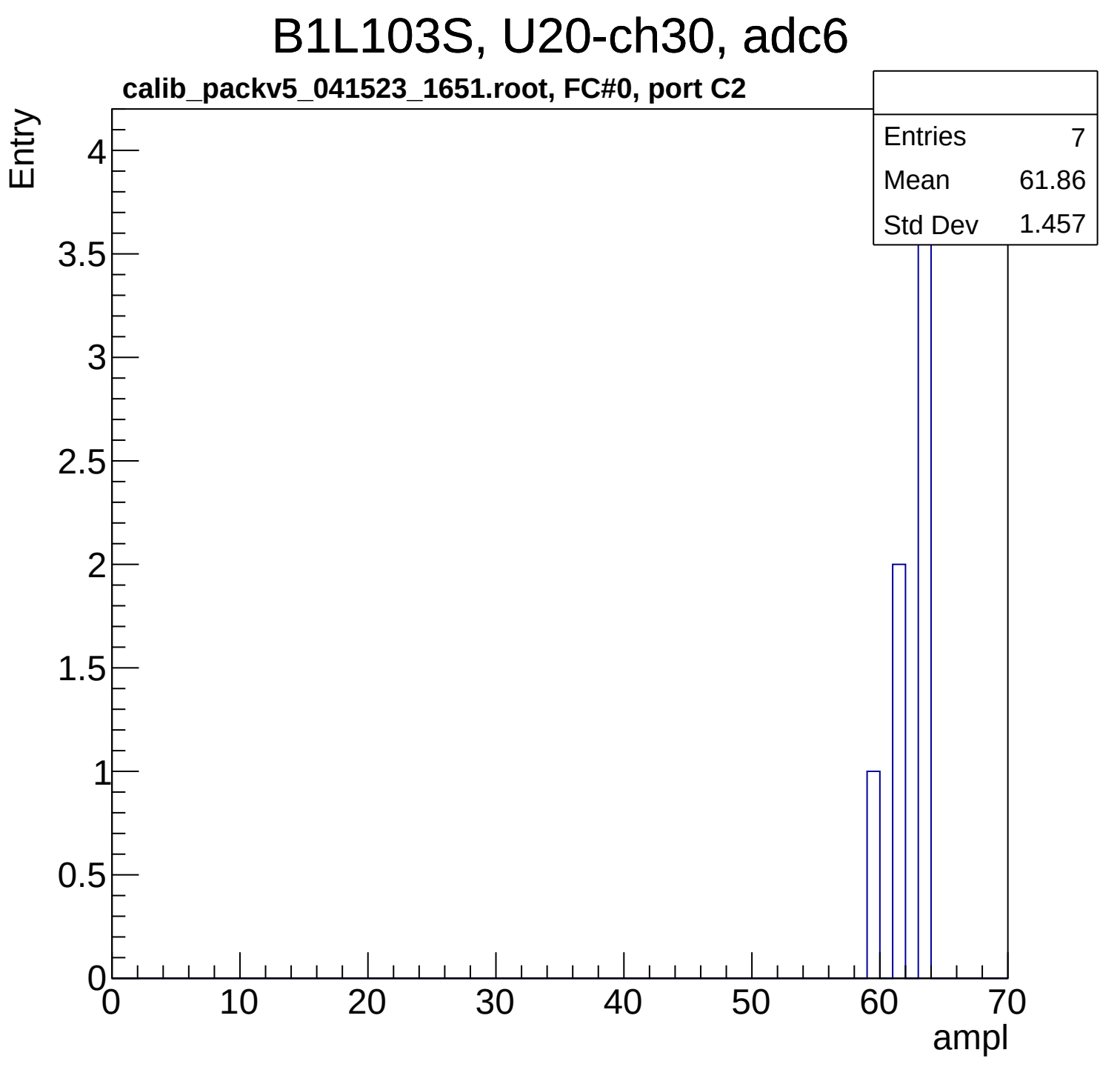
40
50
60
70


B1L103S, U20-ch30, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 61.86
Std Dev 1.457
Entry
ampl
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1.5
2
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3
3.5
4
0
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20
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40
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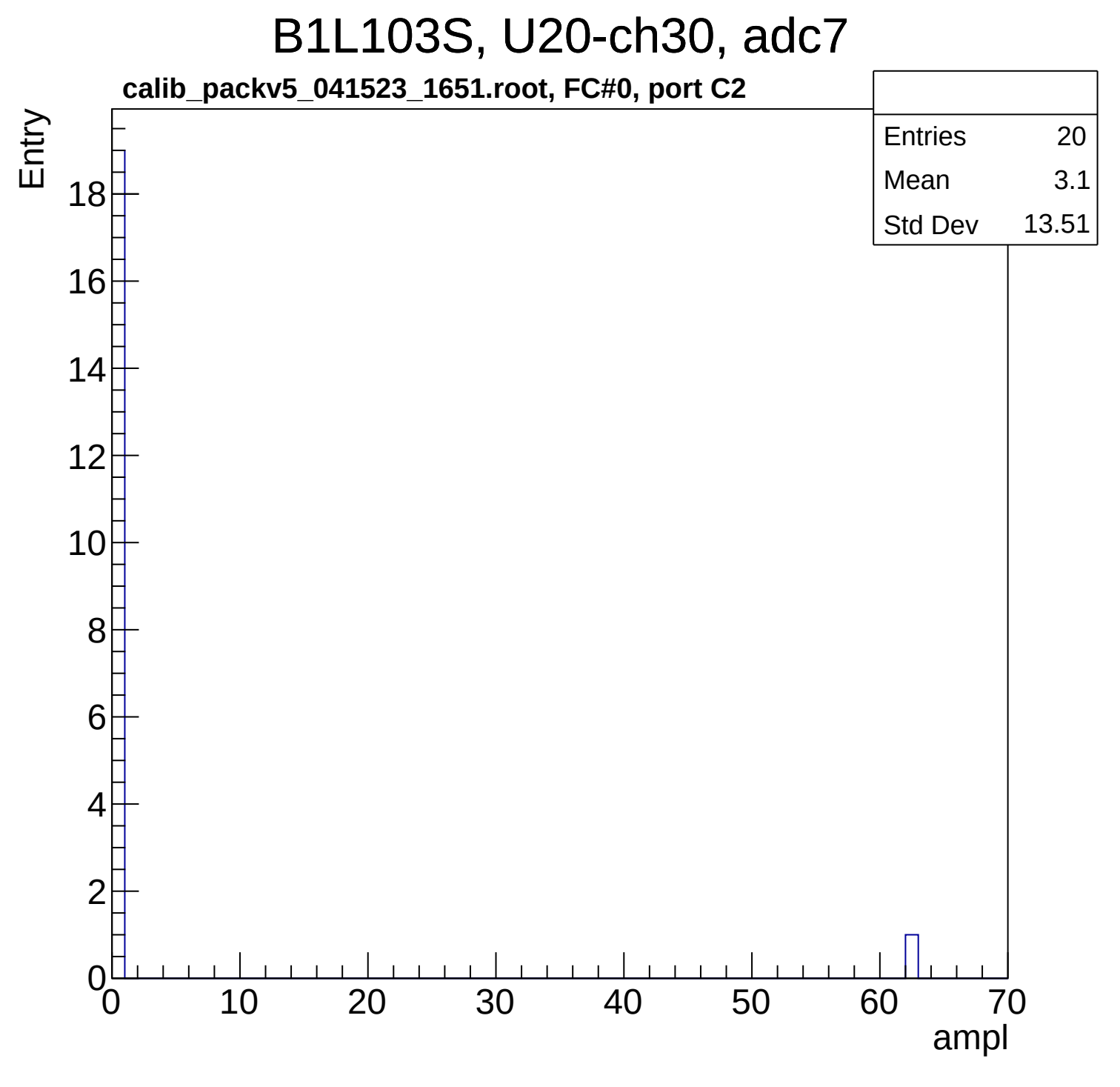
60
70


B1L103S, U20-ch30, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
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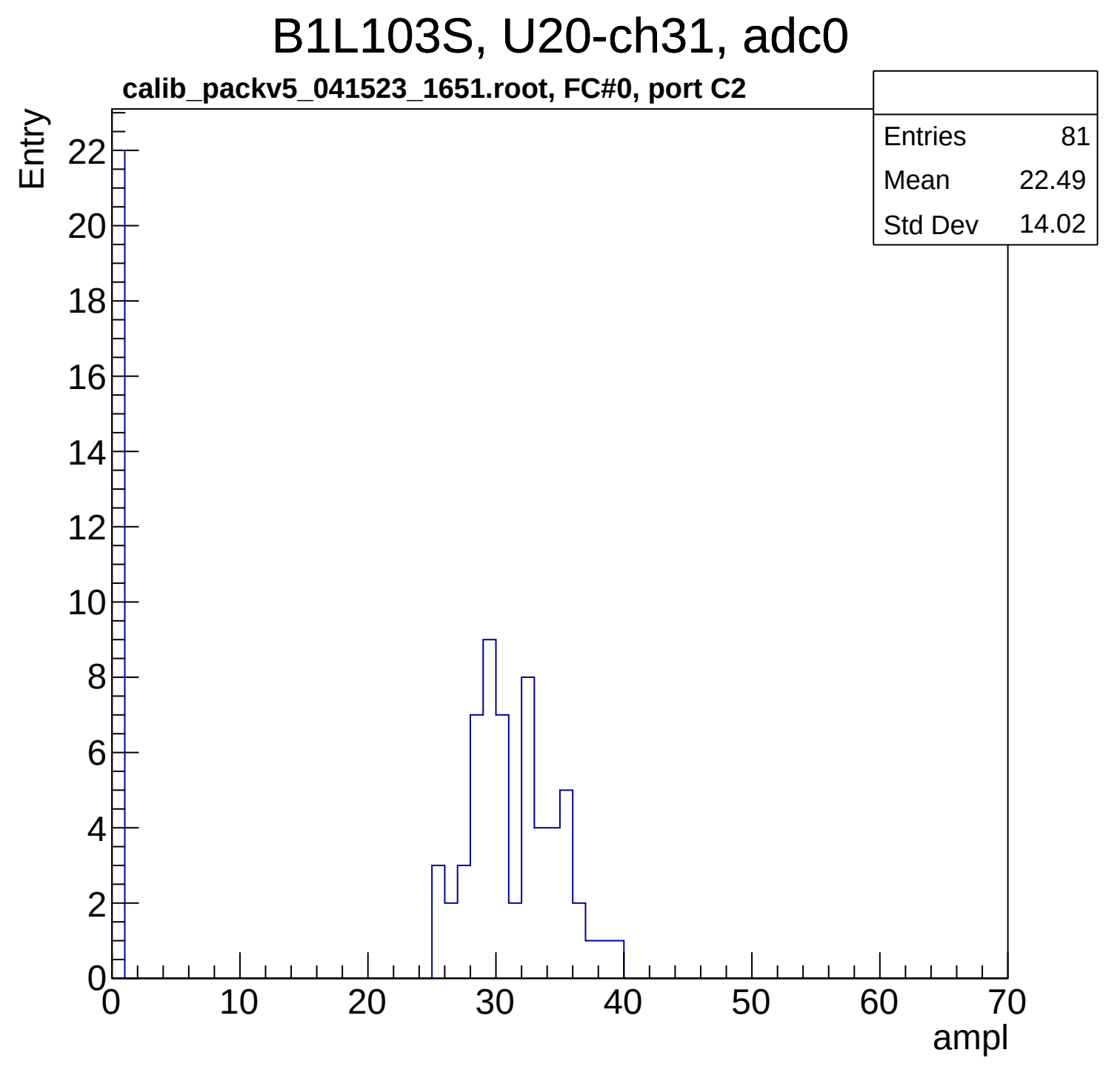
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch31, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 22.49
Std Dev 14.02
Entry
ampl
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2
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6
8
10
12
14
16
18
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0
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40
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60
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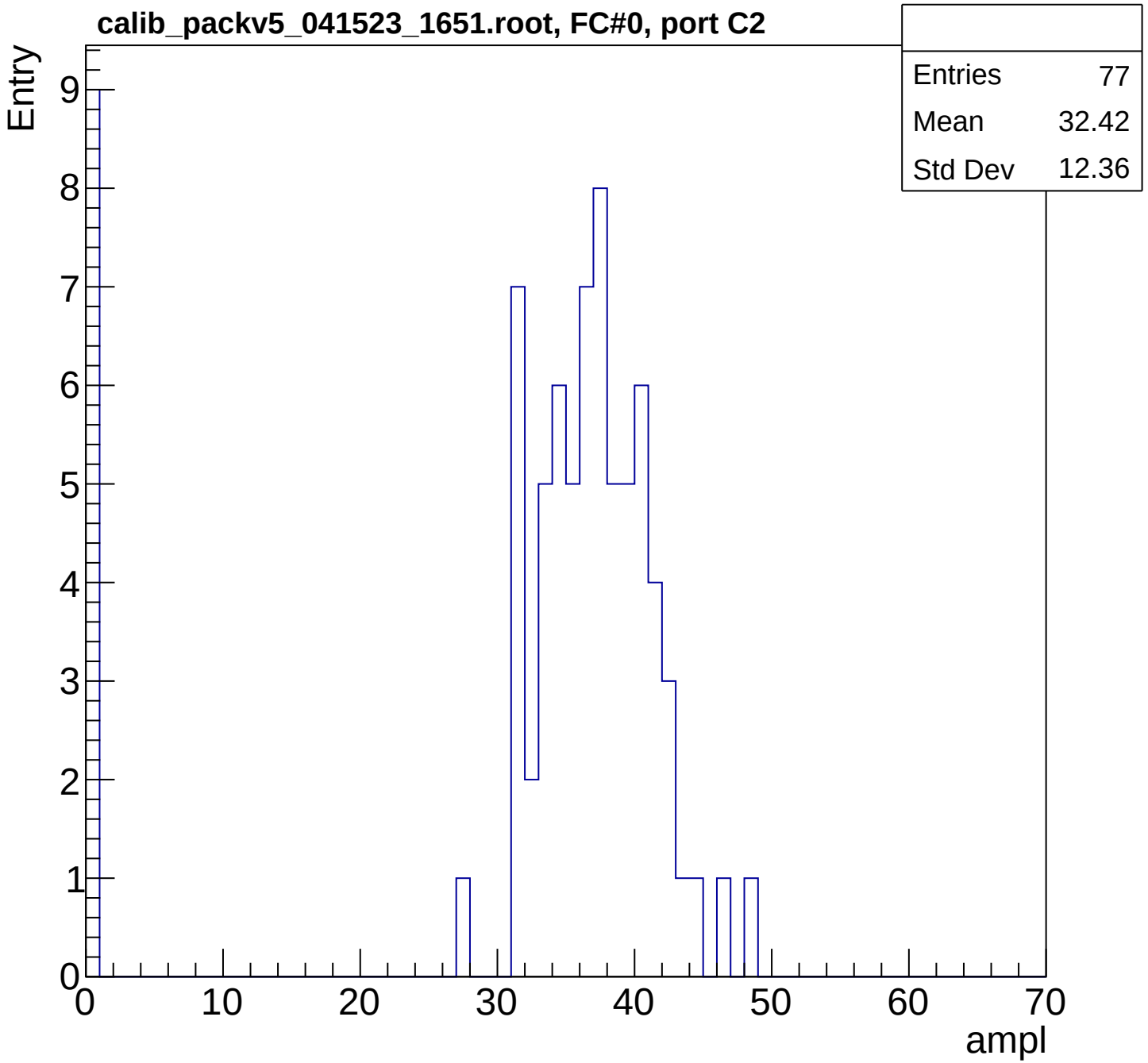
B1L103S, U20-ch31, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 32.42
Std Dev 12.36
Entry
ampl
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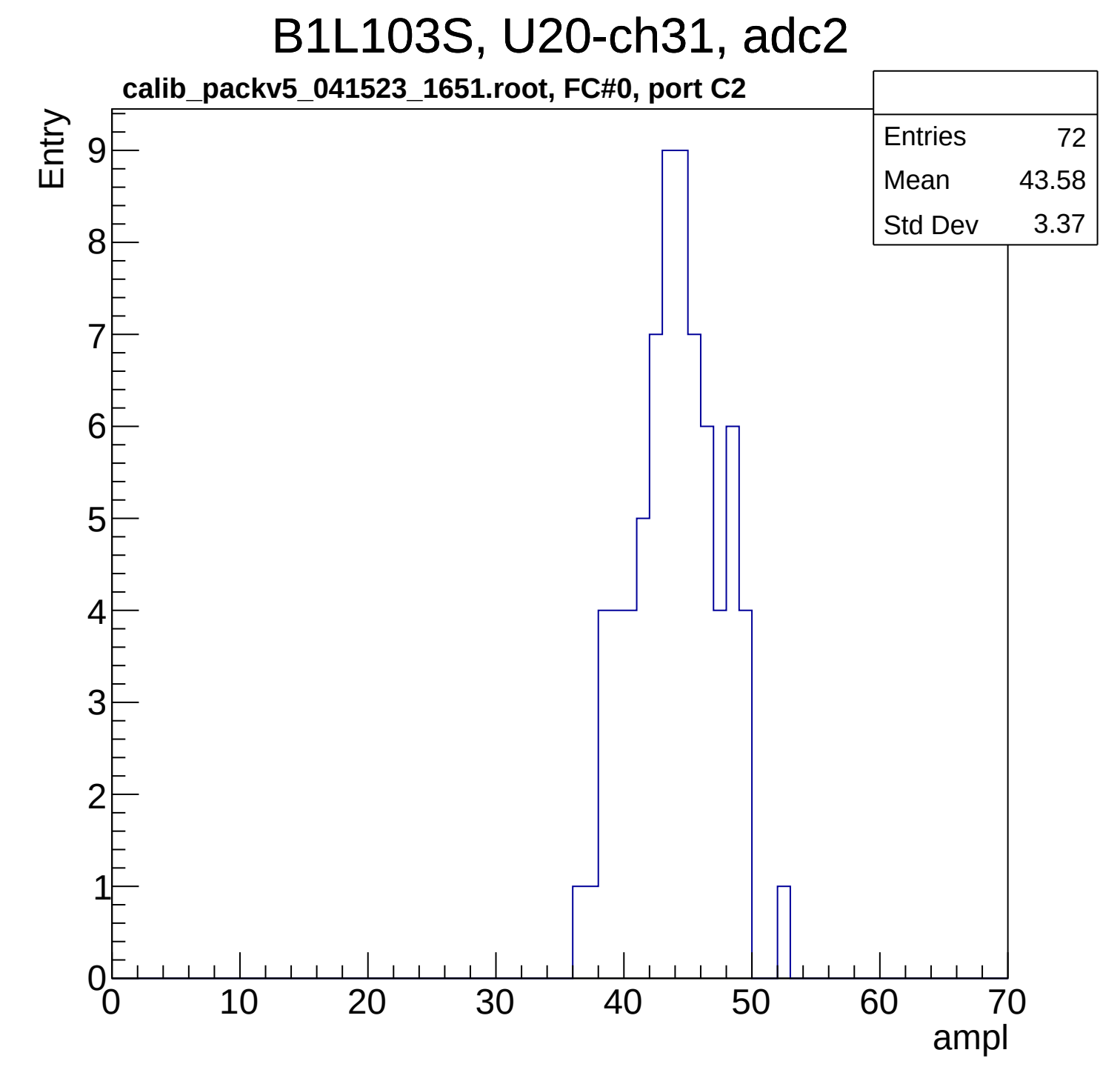
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch31, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 43.58
Std Dev 3.37
Entry
ampl
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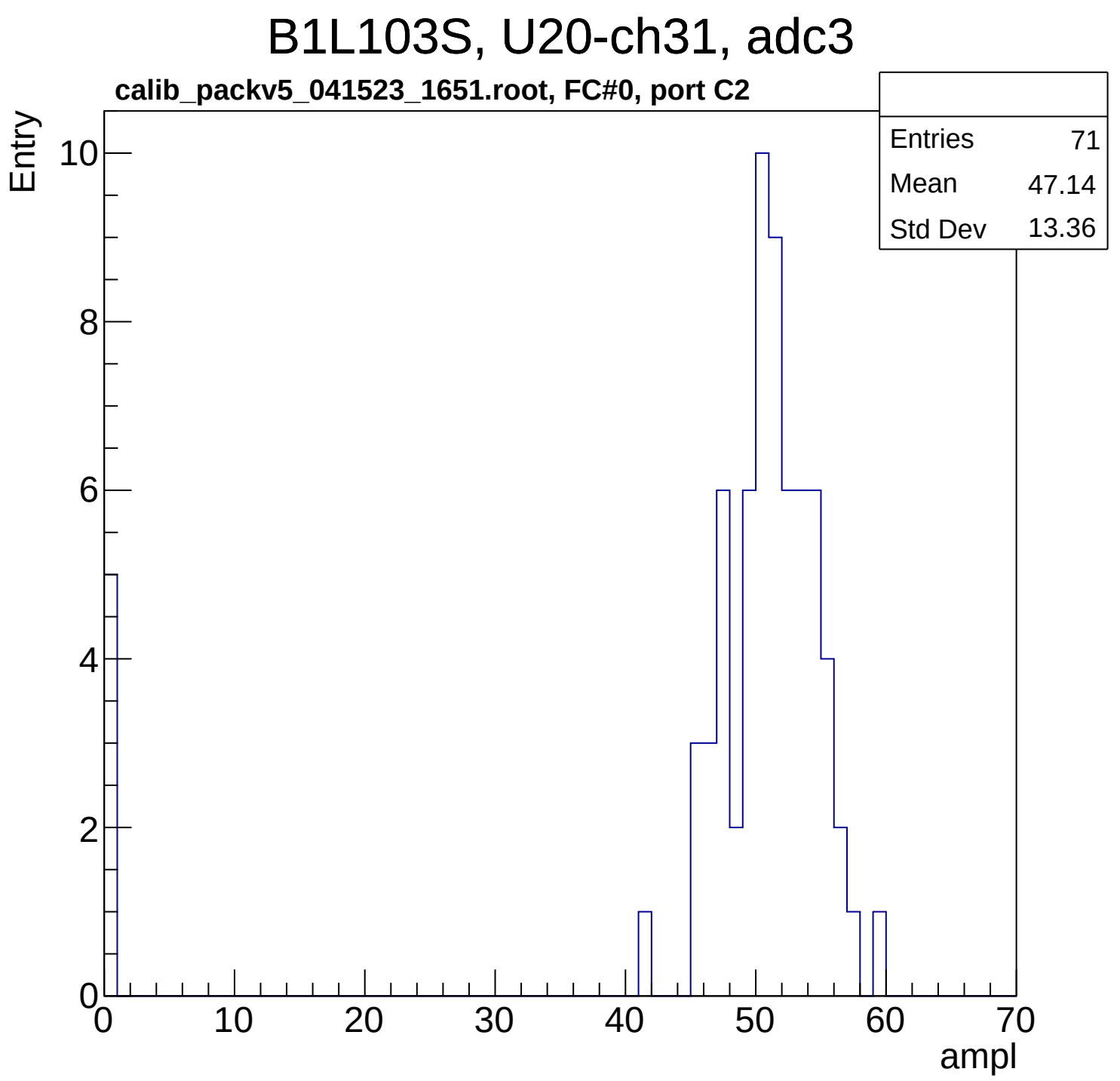
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch31, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 47.14
Std Dev 13.36
Entry
ampl
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2
4
6
8
10
0
10
20
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40
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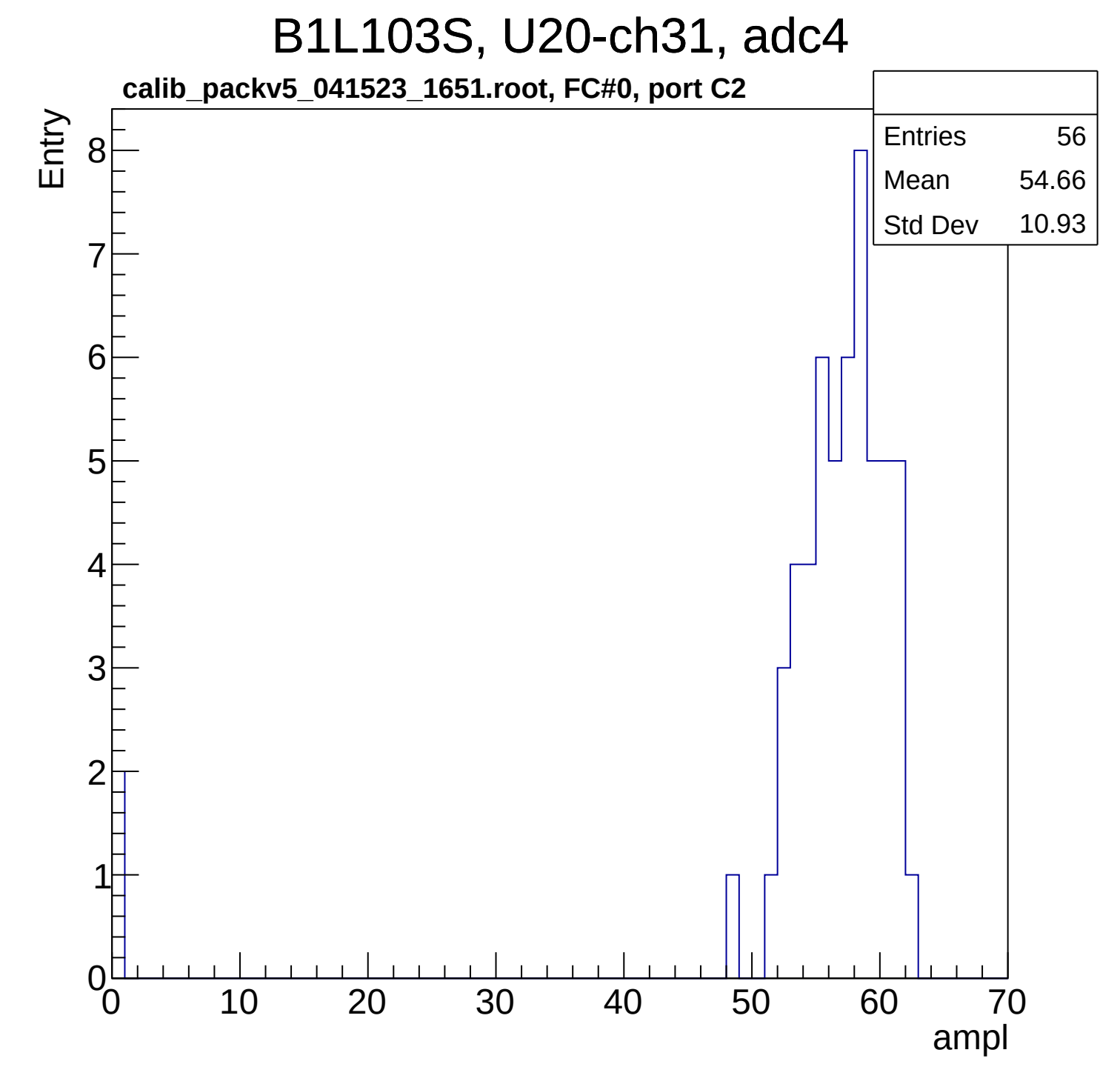
60
70


B1L103S, U20-ch31, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 54.66
Std Dev 10.93
Entry
ampl
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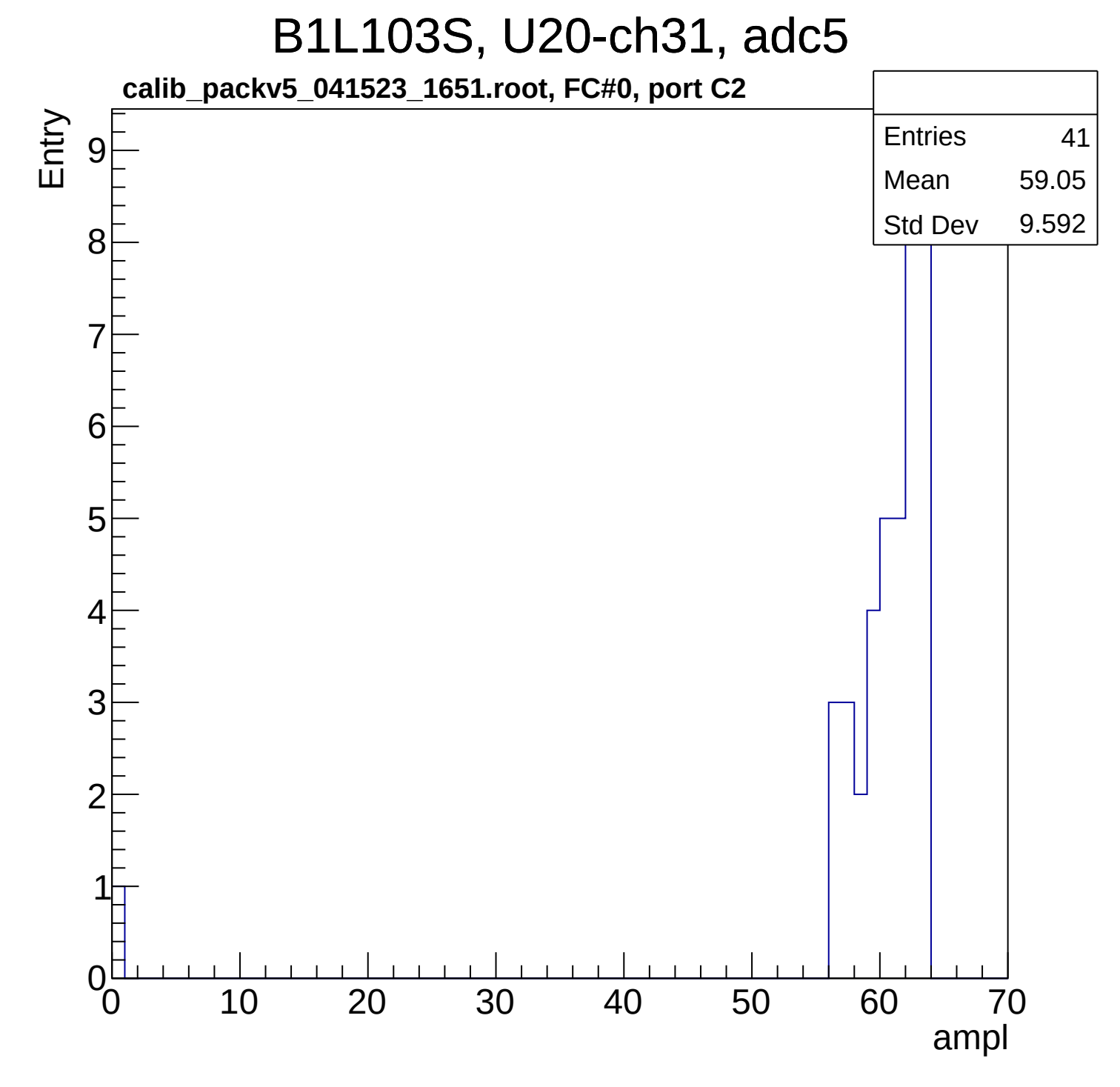
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch31, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 59.05
Std Dev 9.592
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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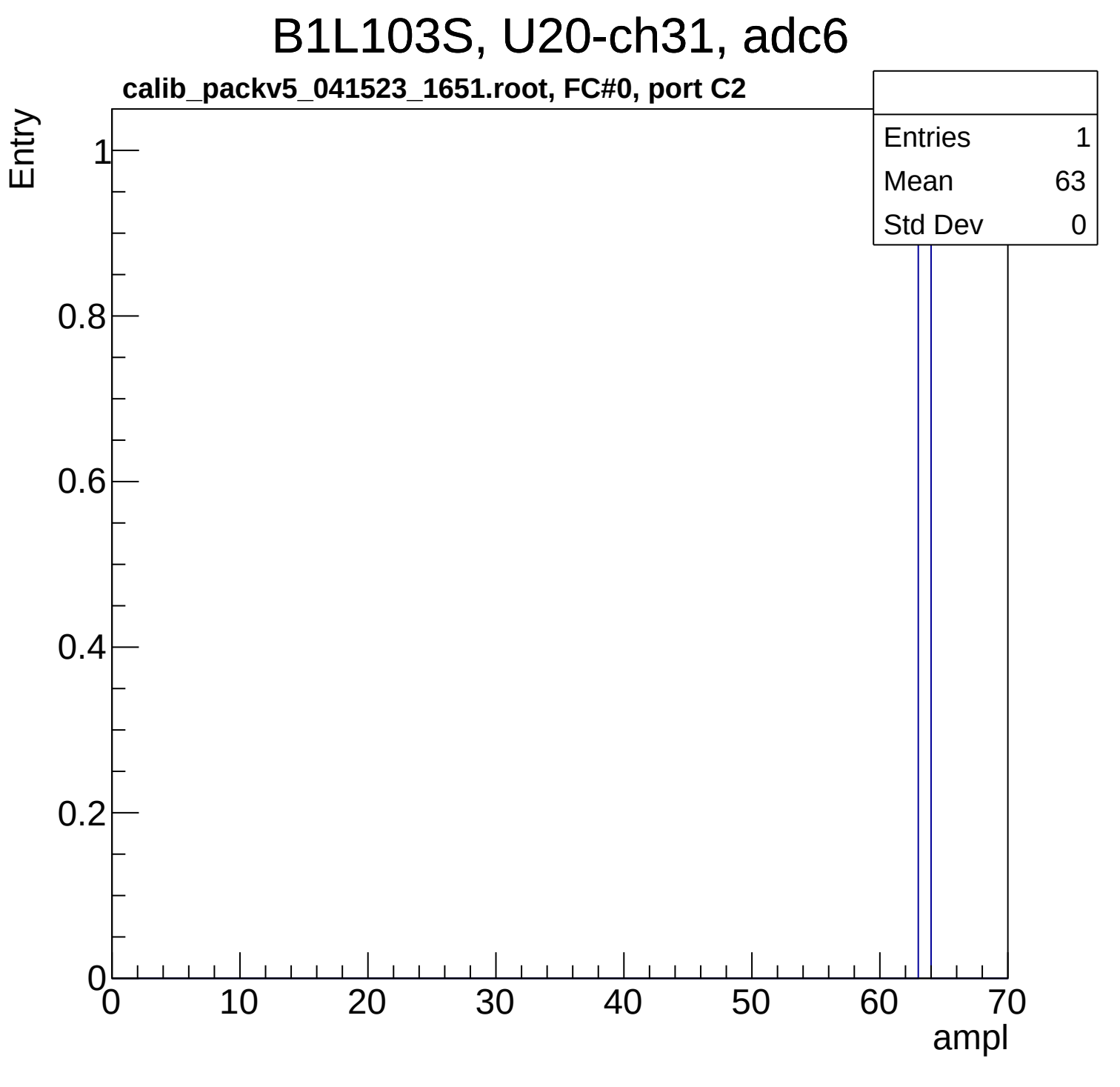
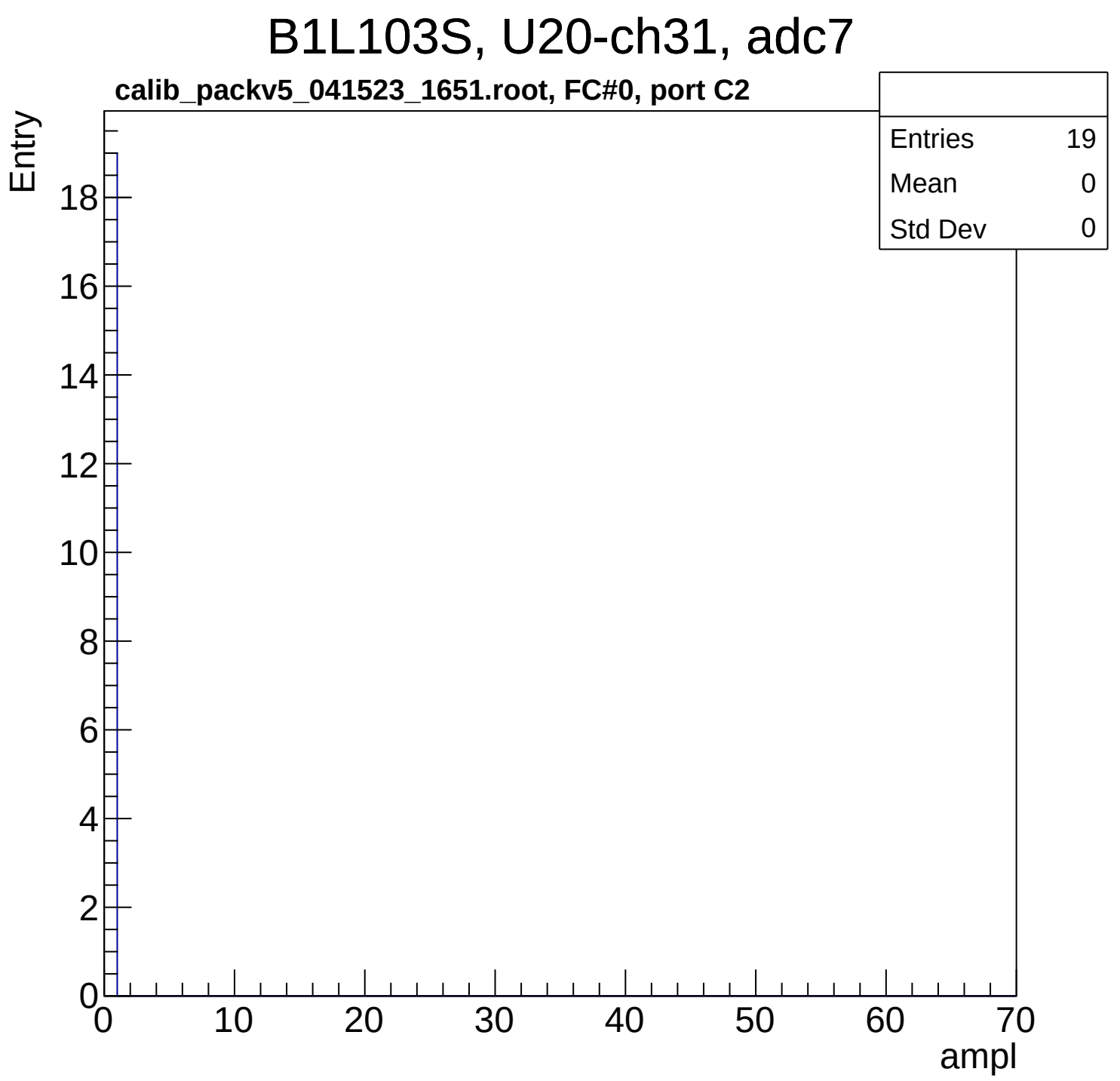

B1L103S, U20-ch31, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch31, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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6
8
10
12
14
16
18
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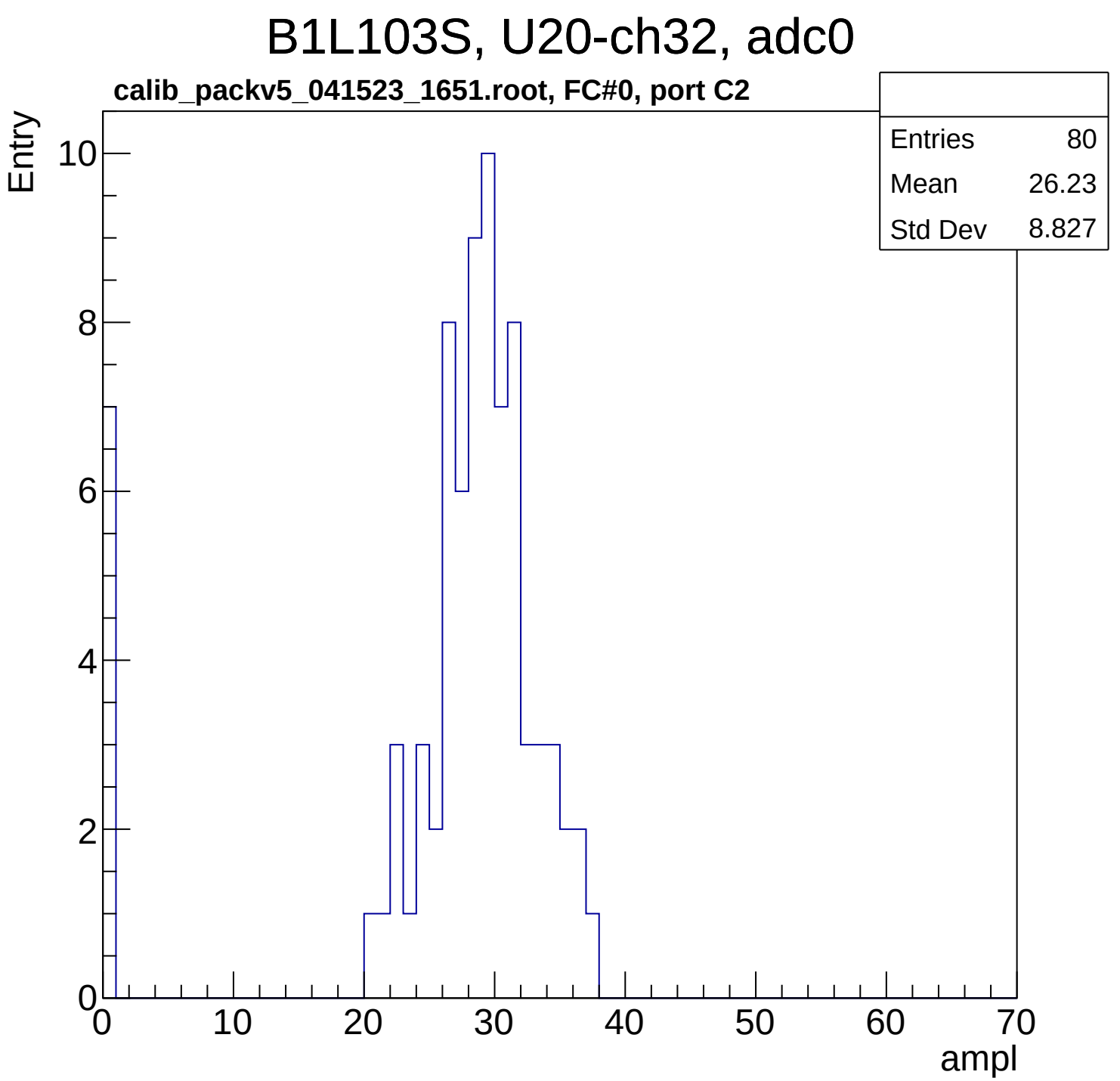
70
ampl


B1L103S, U20-ch32, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 26.23
Std Dev 8.827
Entry
ampl
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2
4
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40
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60
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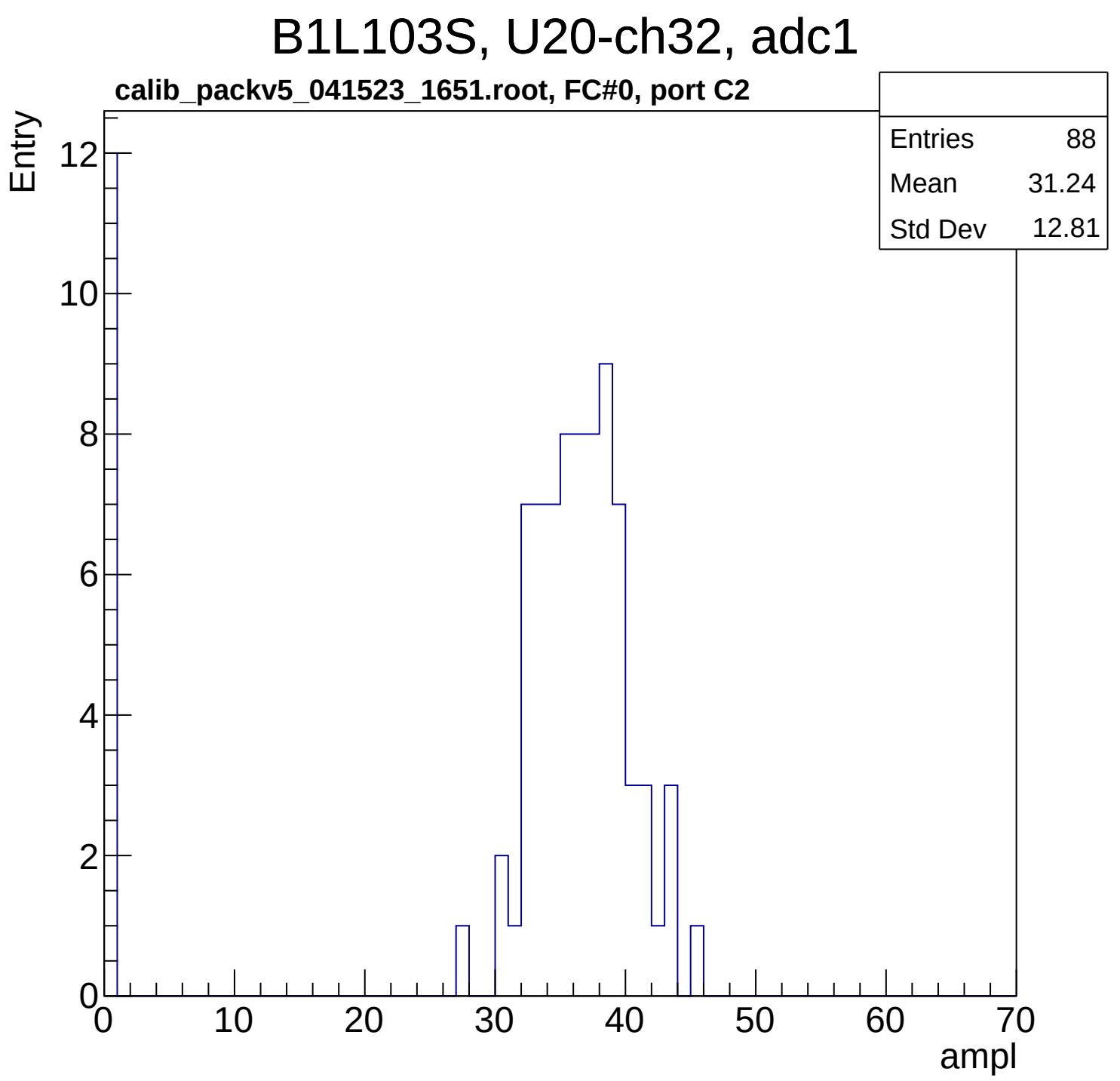
B1L103S, U20-ch32, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 31.24
Std Dev 12.81
Entry
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4
6
8
10
12
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10
20
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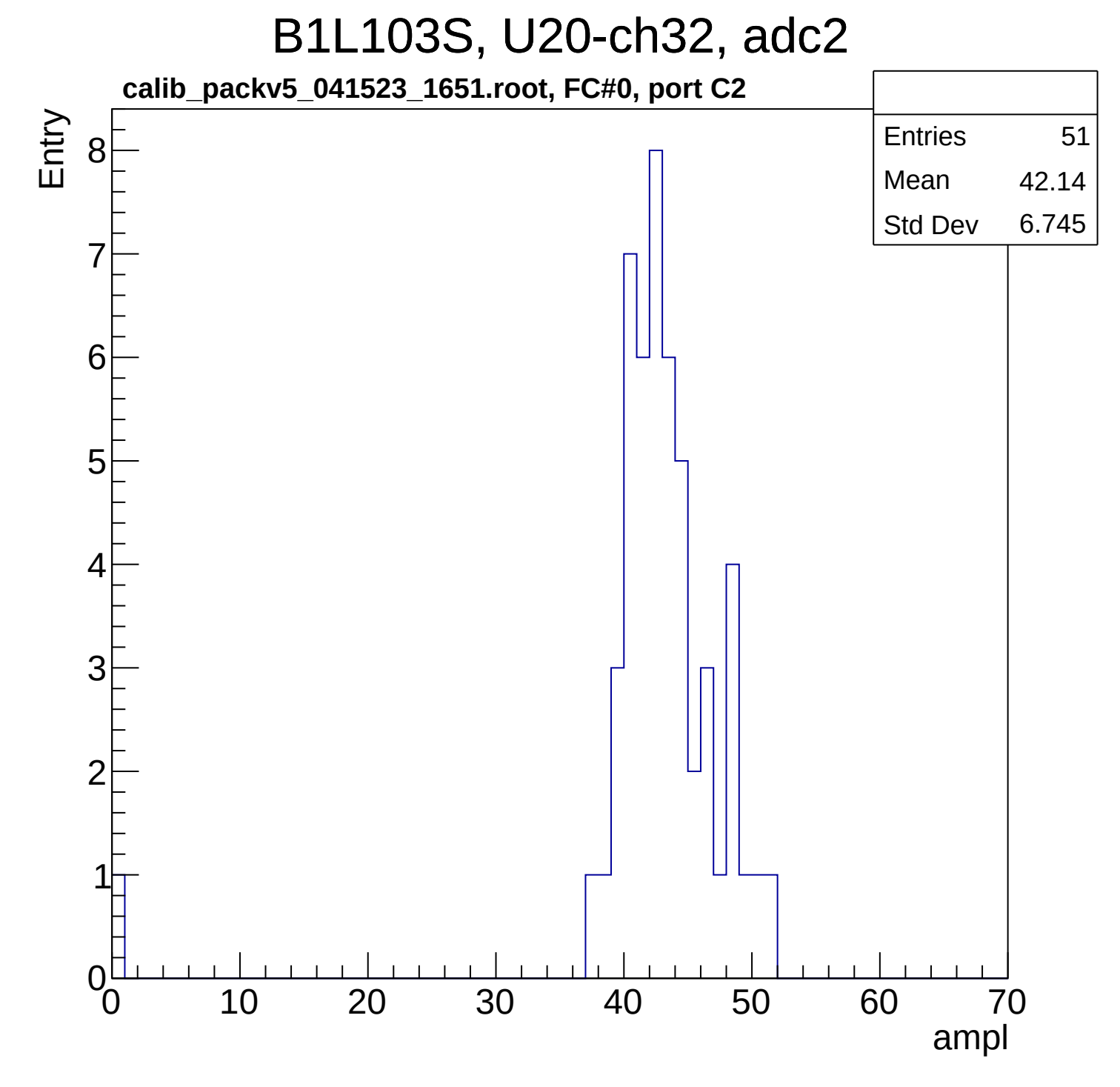
40
50
60
70
ampl


B1L103S, U20-ch32, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 42.14
Std Dev 6.745
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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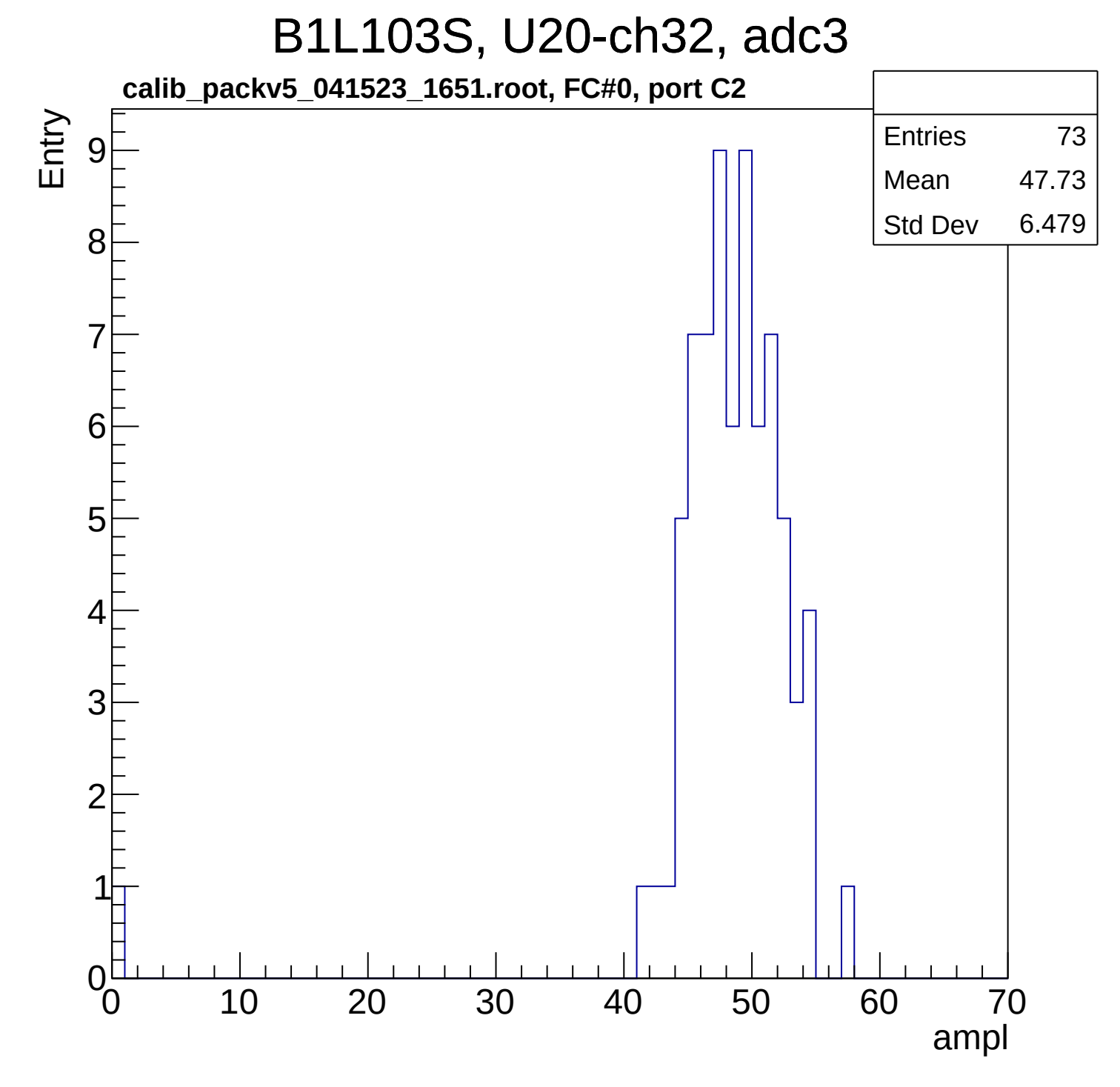
40
50
60
70


B1L103S, U20-ch32, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 47.73
Std Dev 6.479
Entry
ampl
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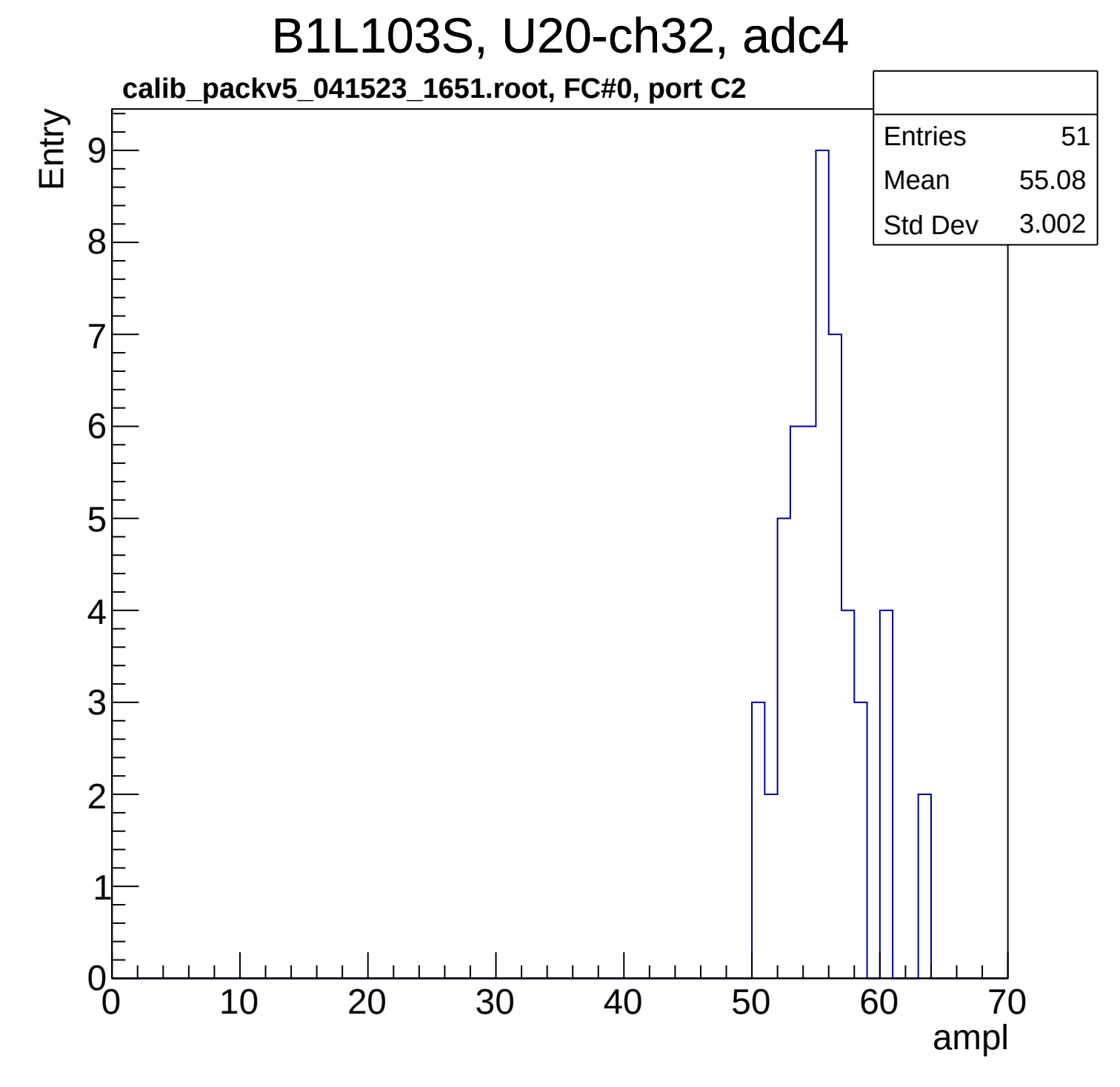
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch32, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 55.08
Std Dev 3.002
Entry
ampl
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3
4
5
6
7
8
9
0
10
20
30
40
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60
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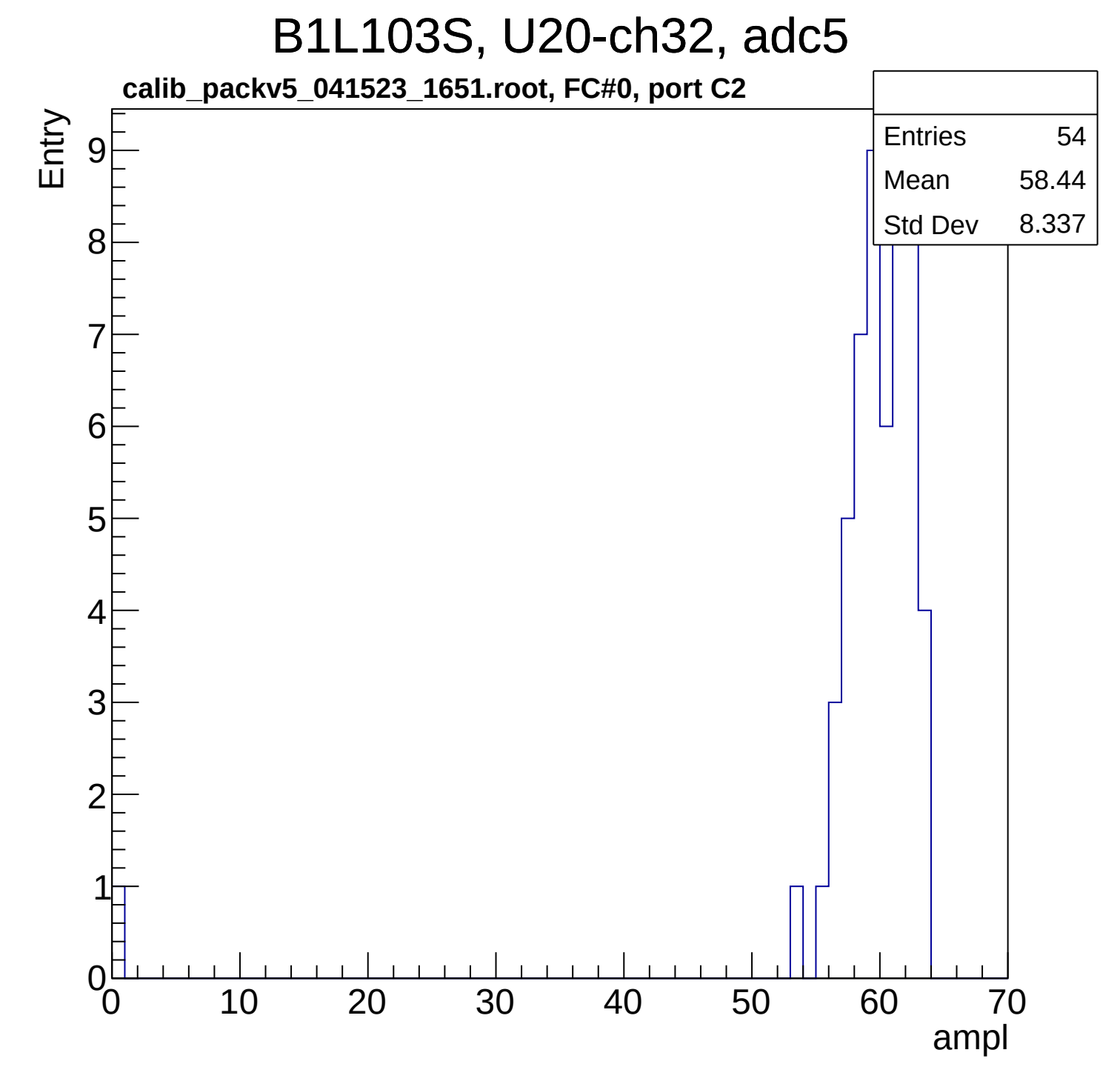
B1L103S, U20-ch32, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 58.44
Std Dev 8.337
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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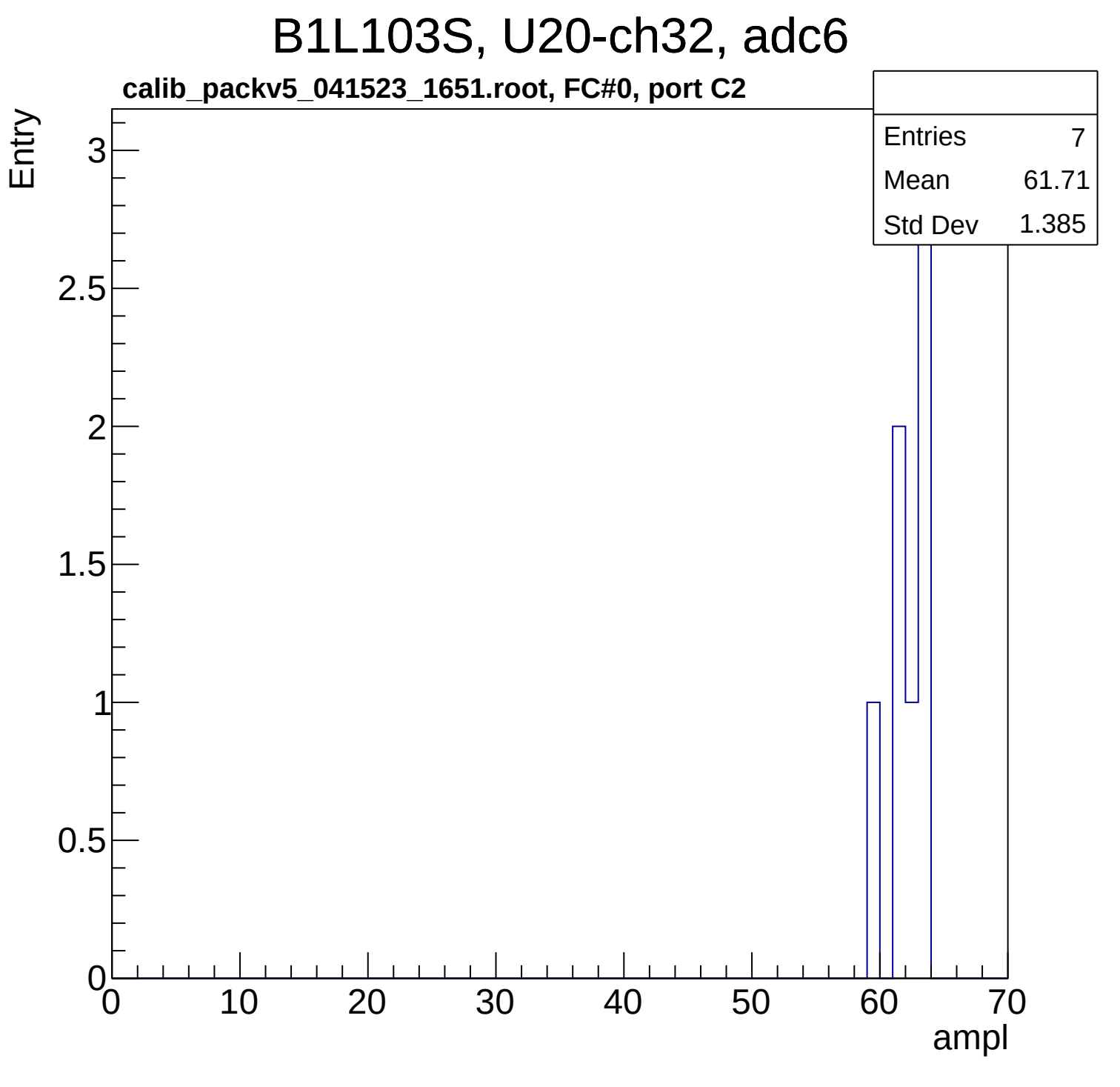
B1L103S, U20-ch32, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 61.71
Std Dev 1.385
Entry
ampl
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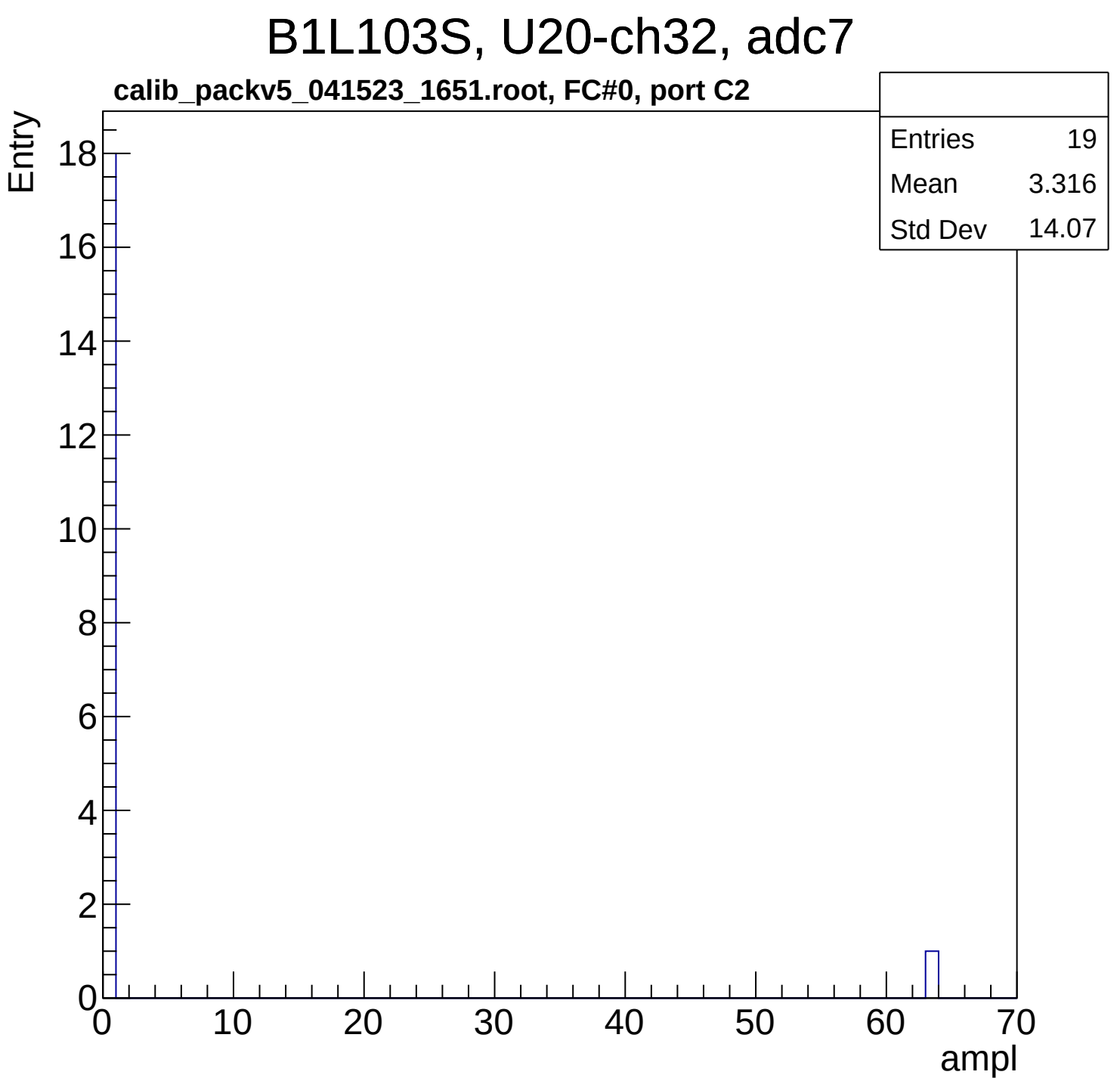
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U20-ch32, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.316
Std Dev 14.07
Entry
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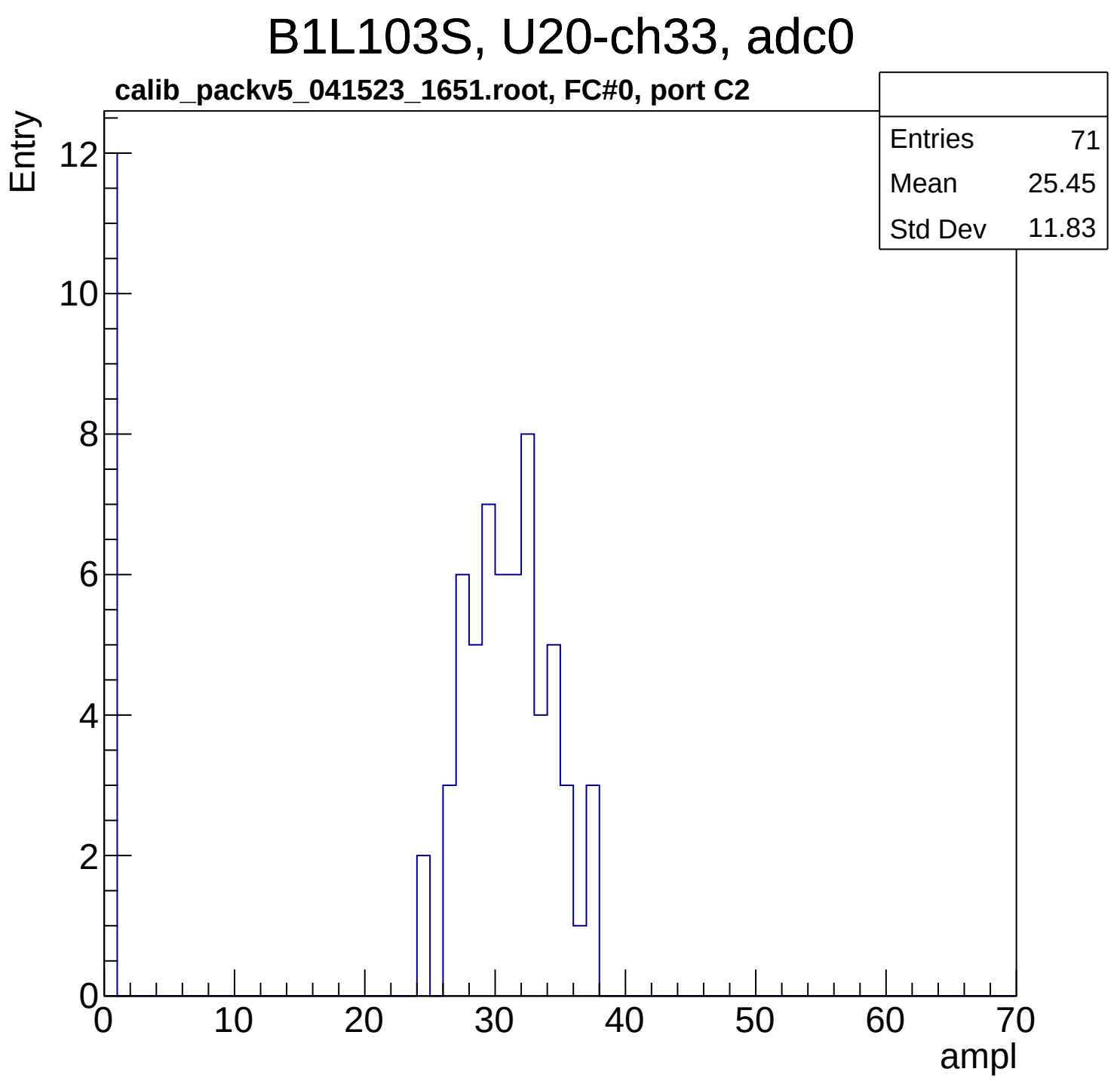
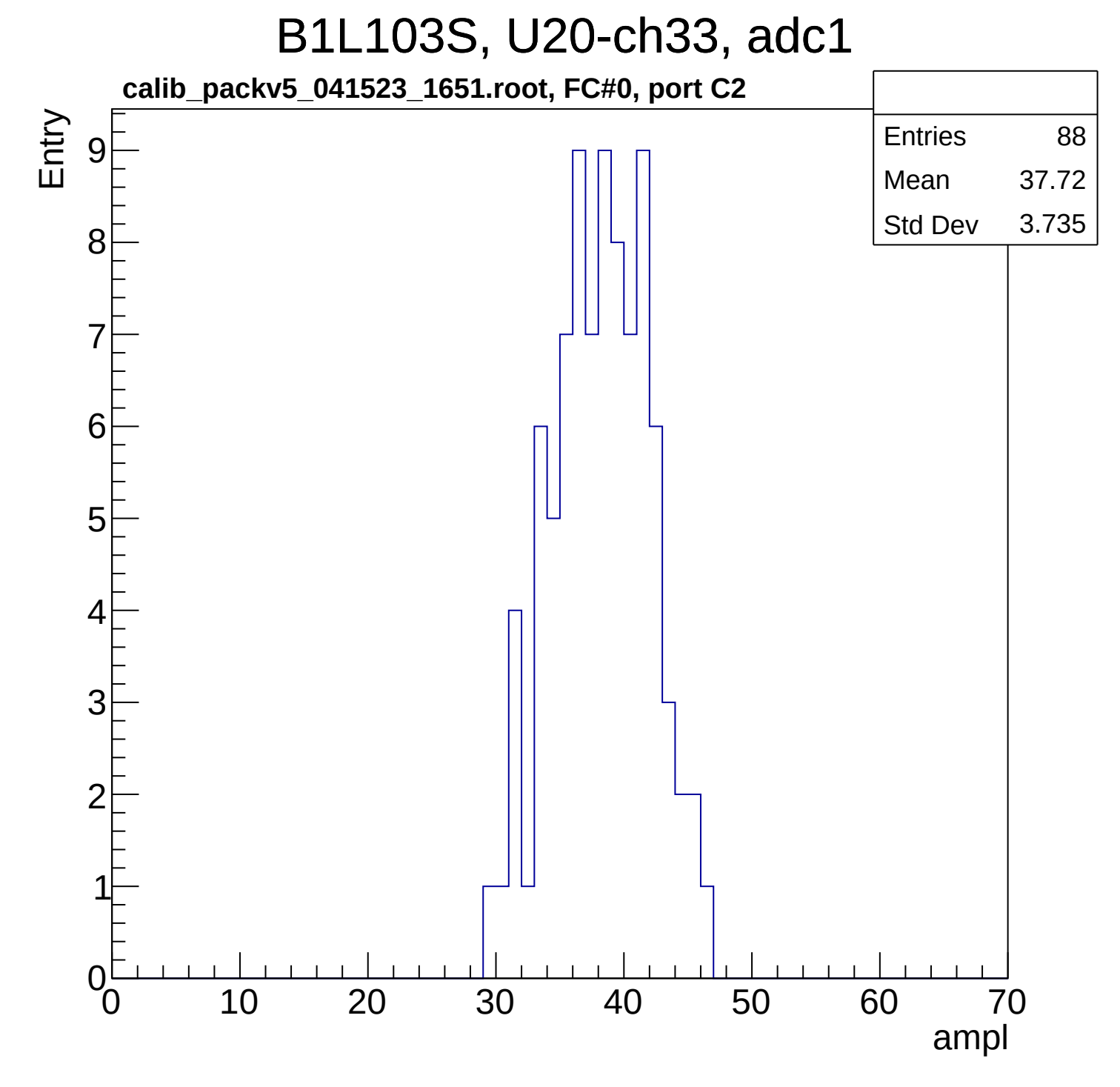
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch33, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 25.45
Std Dev 11.83
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch33, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 37.72
Std Dev 3.735
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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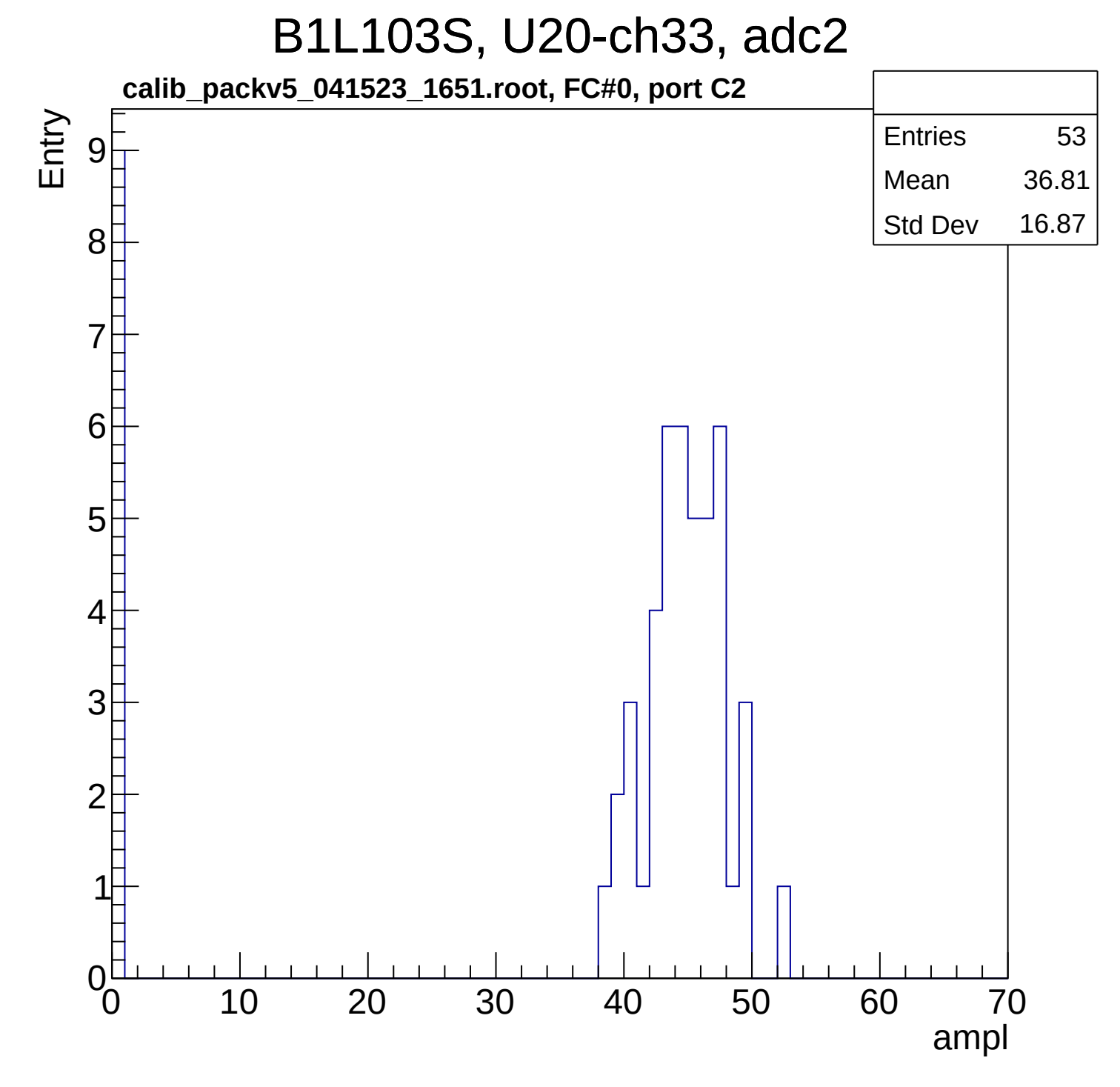
B1L103S, U20-ch33, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 36.81
Std Dev 16.87
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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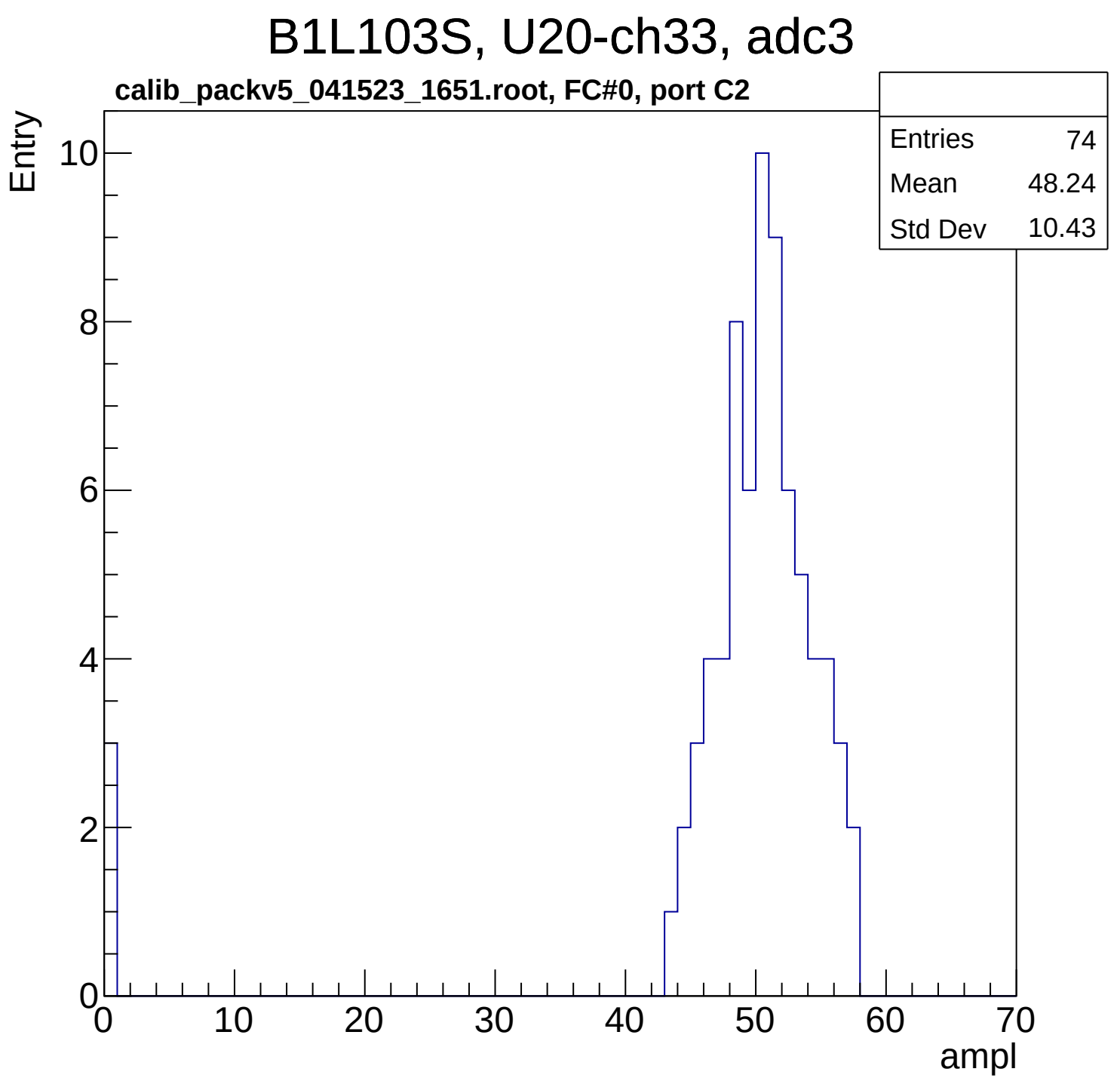
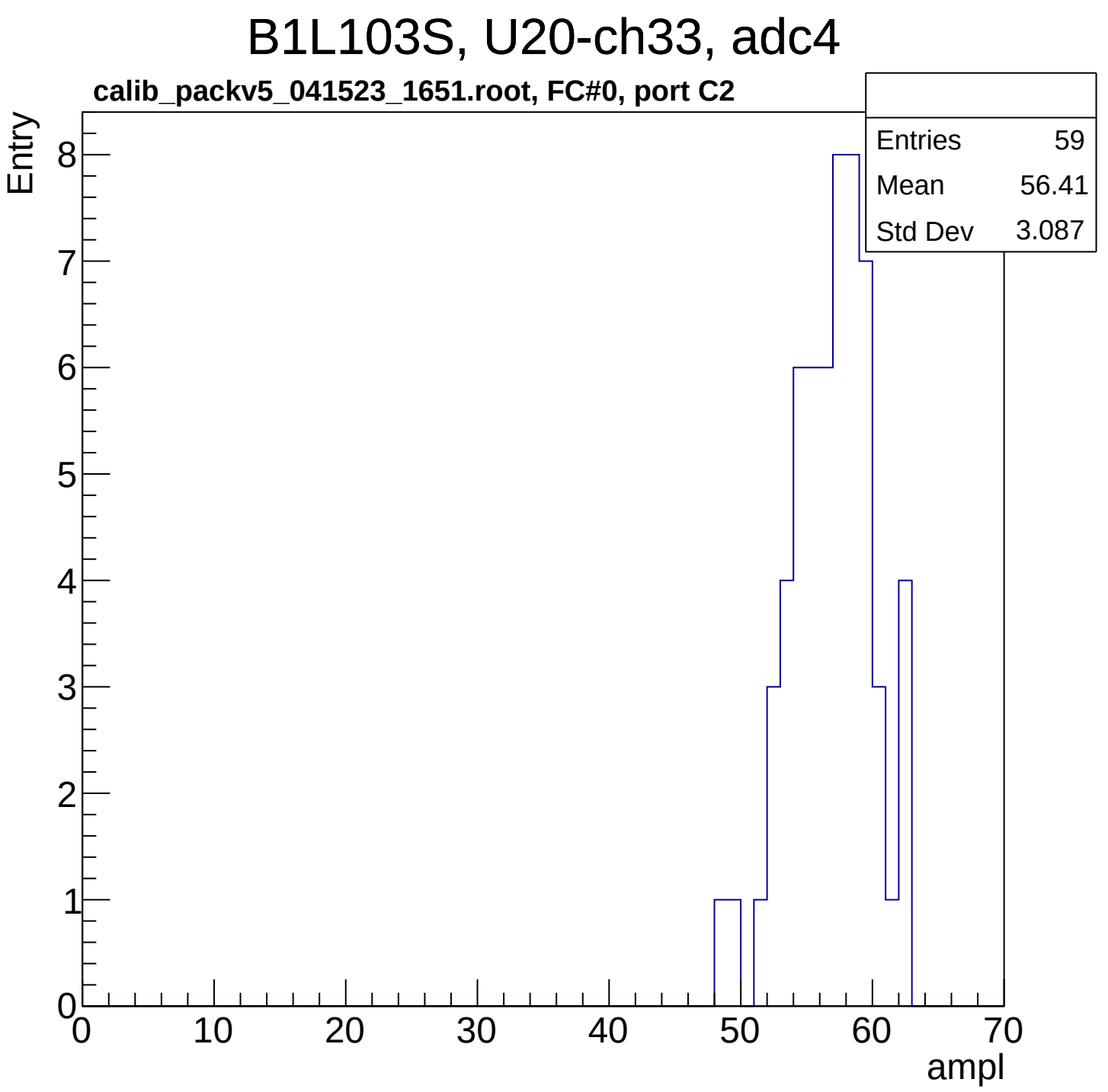

B1L103S, U20-ch33, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 48.24
Std Dev 10.43
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U20-ch33, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 56.41
Std Dev 3.087
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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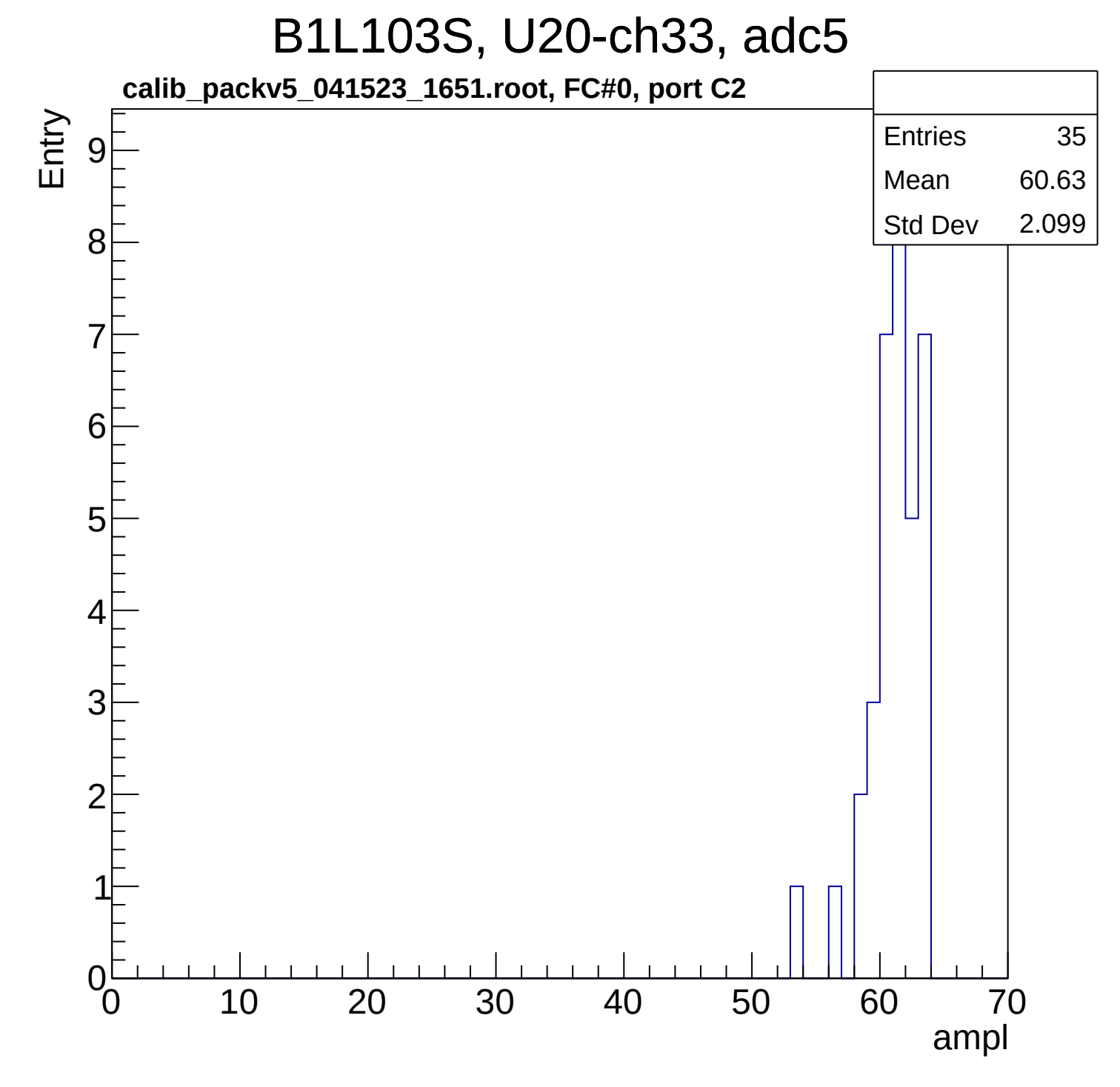
B1L103S, U20-ch33, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 60.63
Std Dev 2.099
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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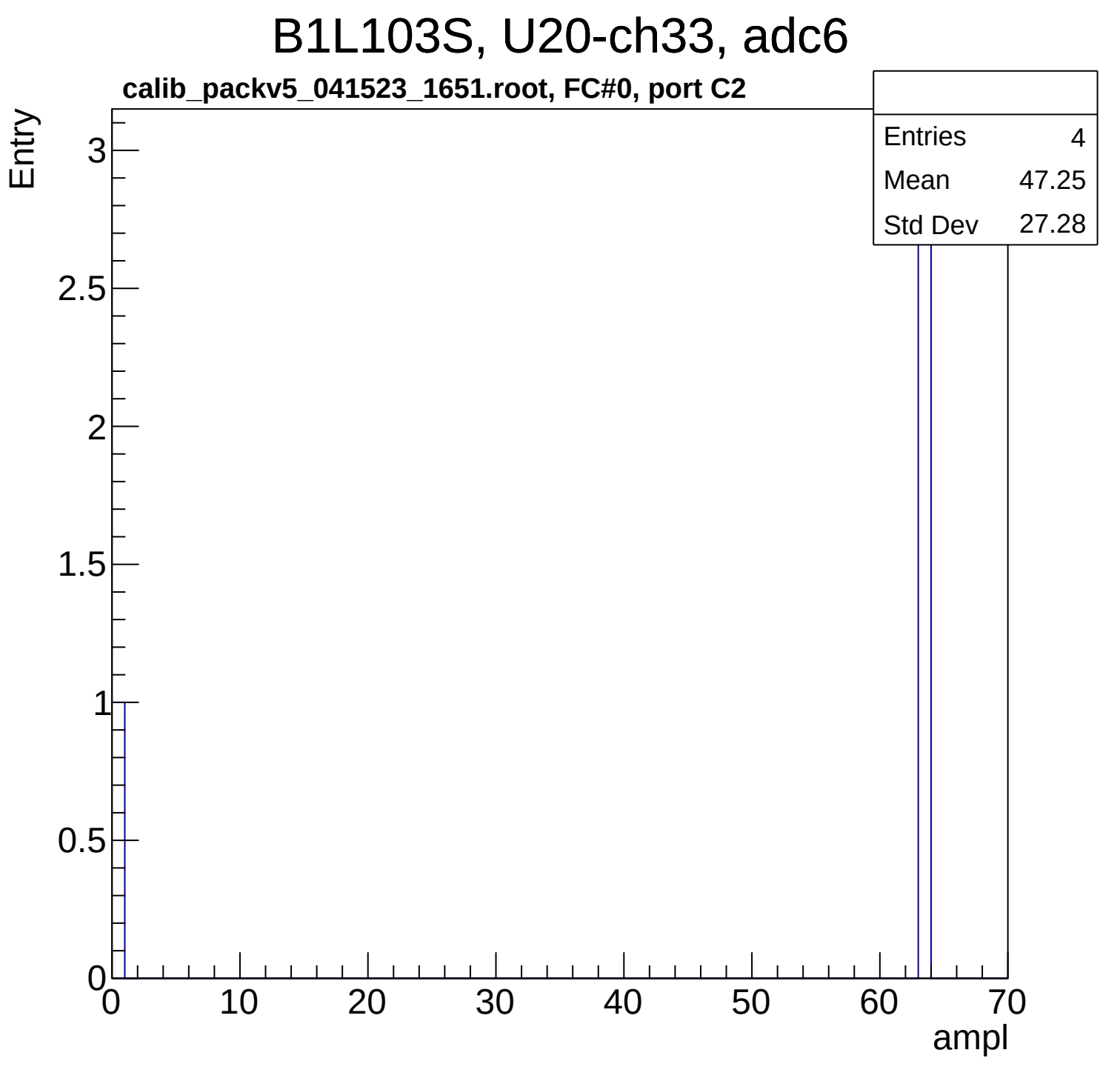
50
60
70


B1L103S, U20-ch33, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 47.25
Std Dev 27.28
Entry
ampl
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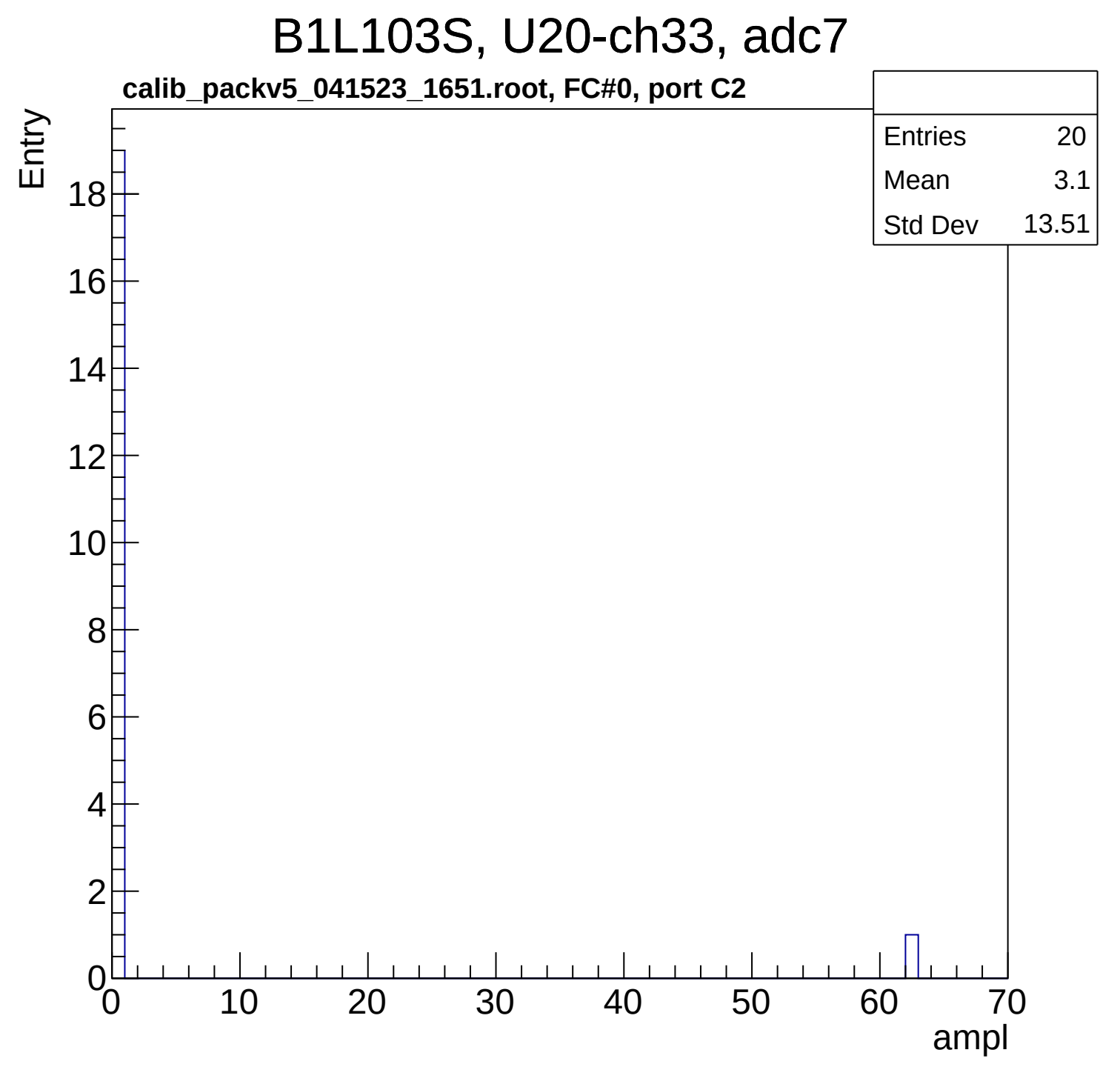
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U20-ch33, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
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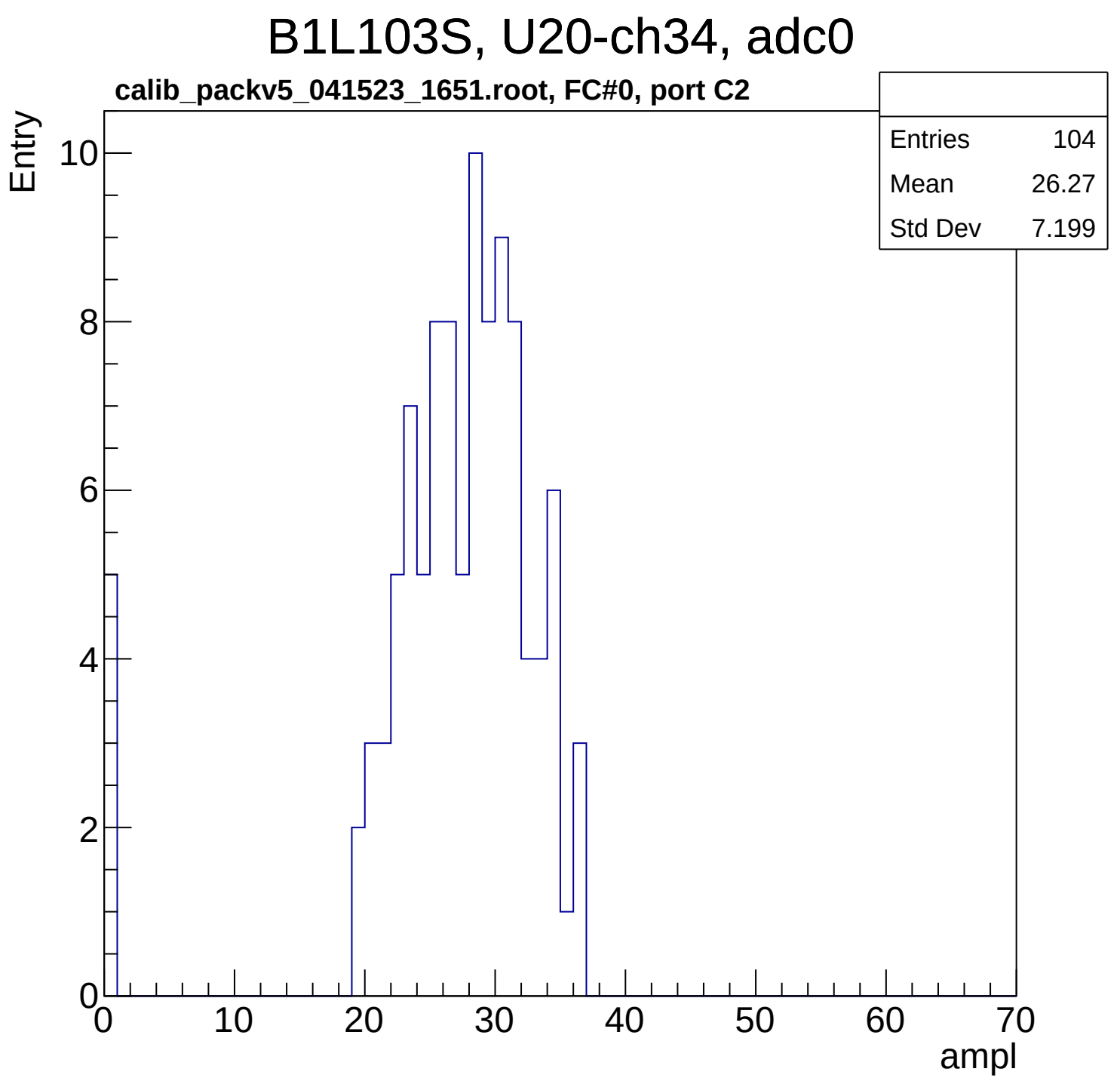
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch34, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 104
Mean 26.27
Std Dev 7.199
Entry
ampl
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2
4
6
8
10
0
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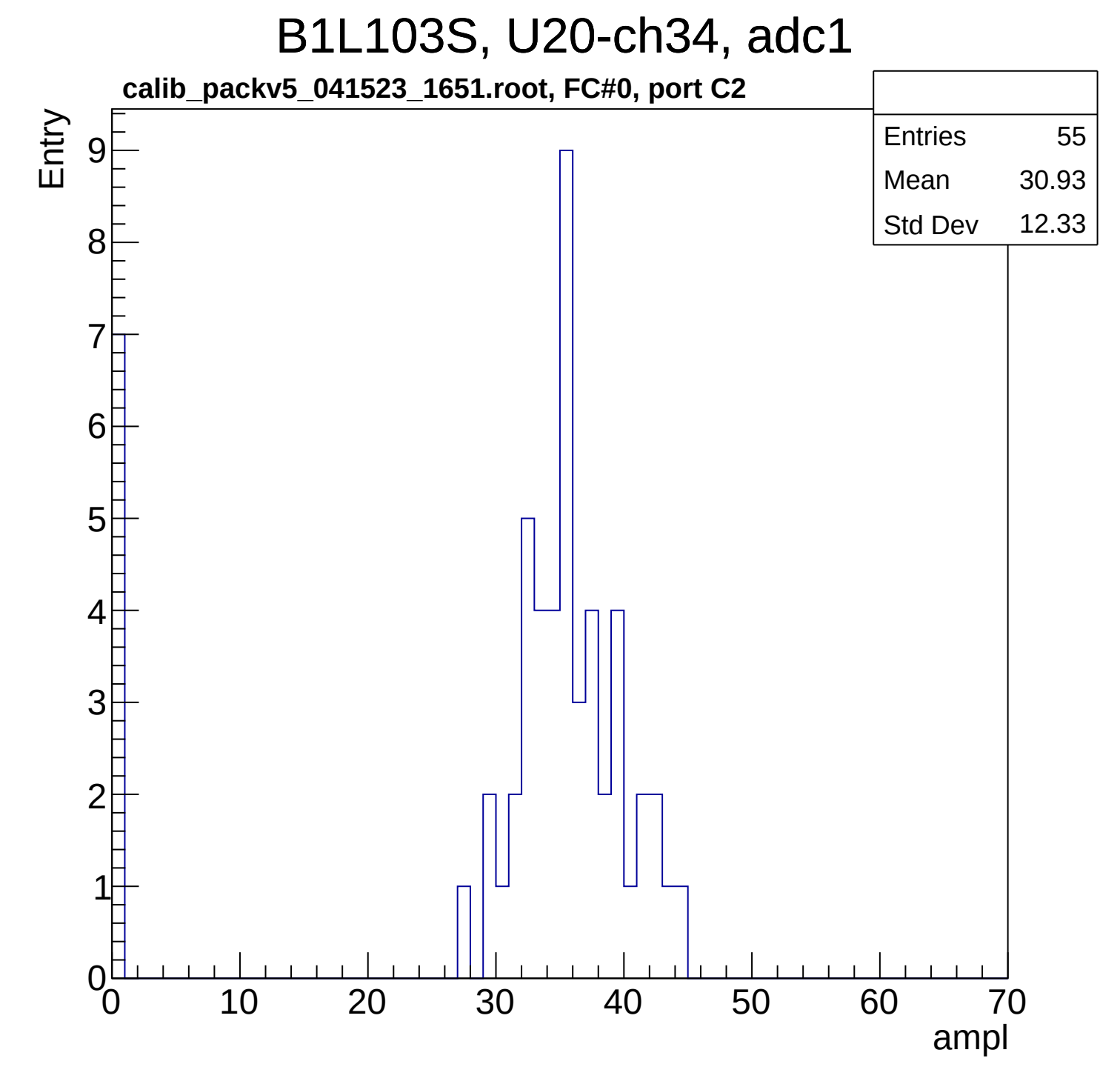
20
30
40
50
60
70


B1L103S, U20-ch34, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 30.93
Std Dev 12.33
Entry
ampl
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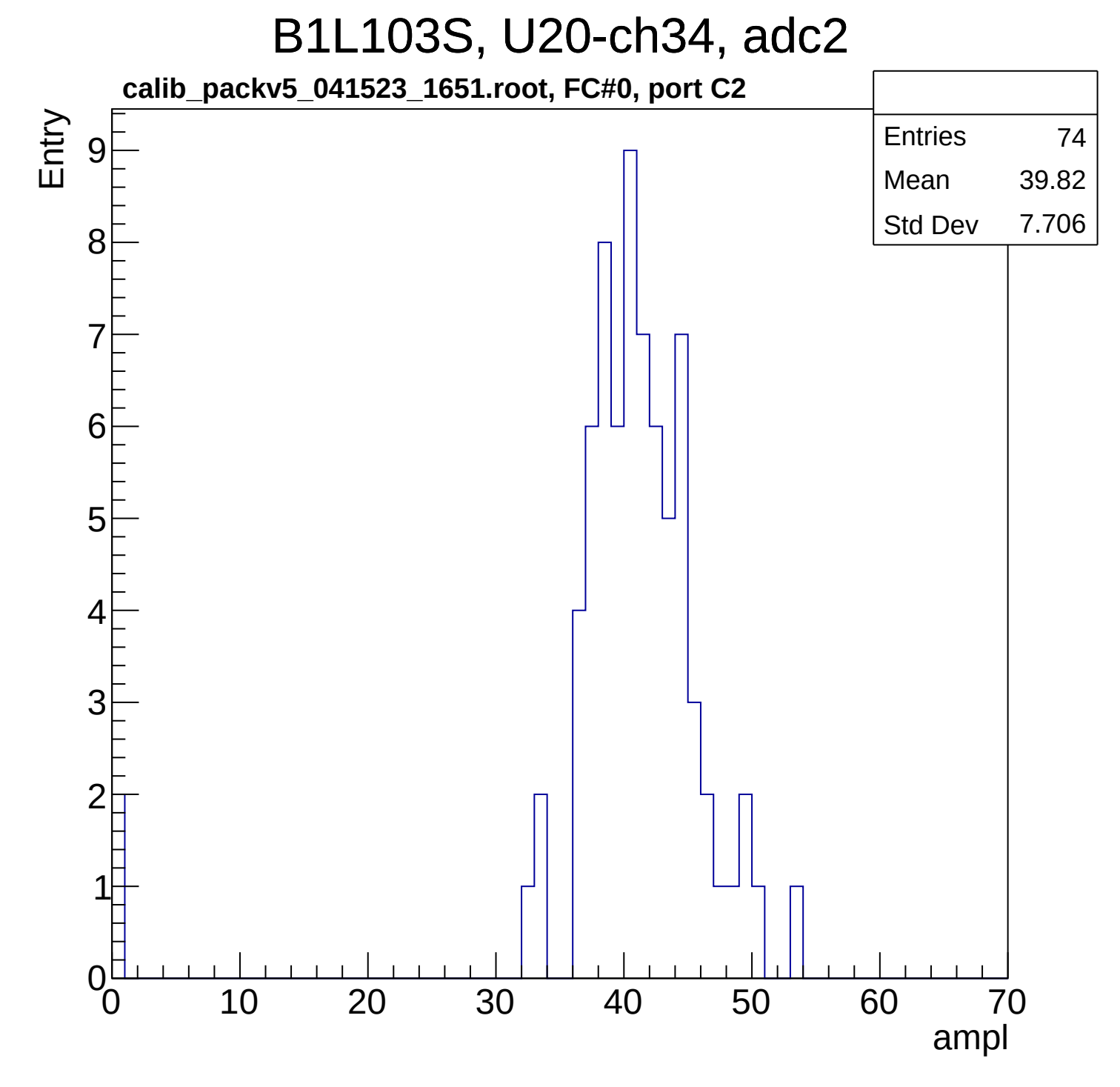
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch34, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 39.82
Std Dev 7.706
Entry
ampl
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3
4
5
6
7
8
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0
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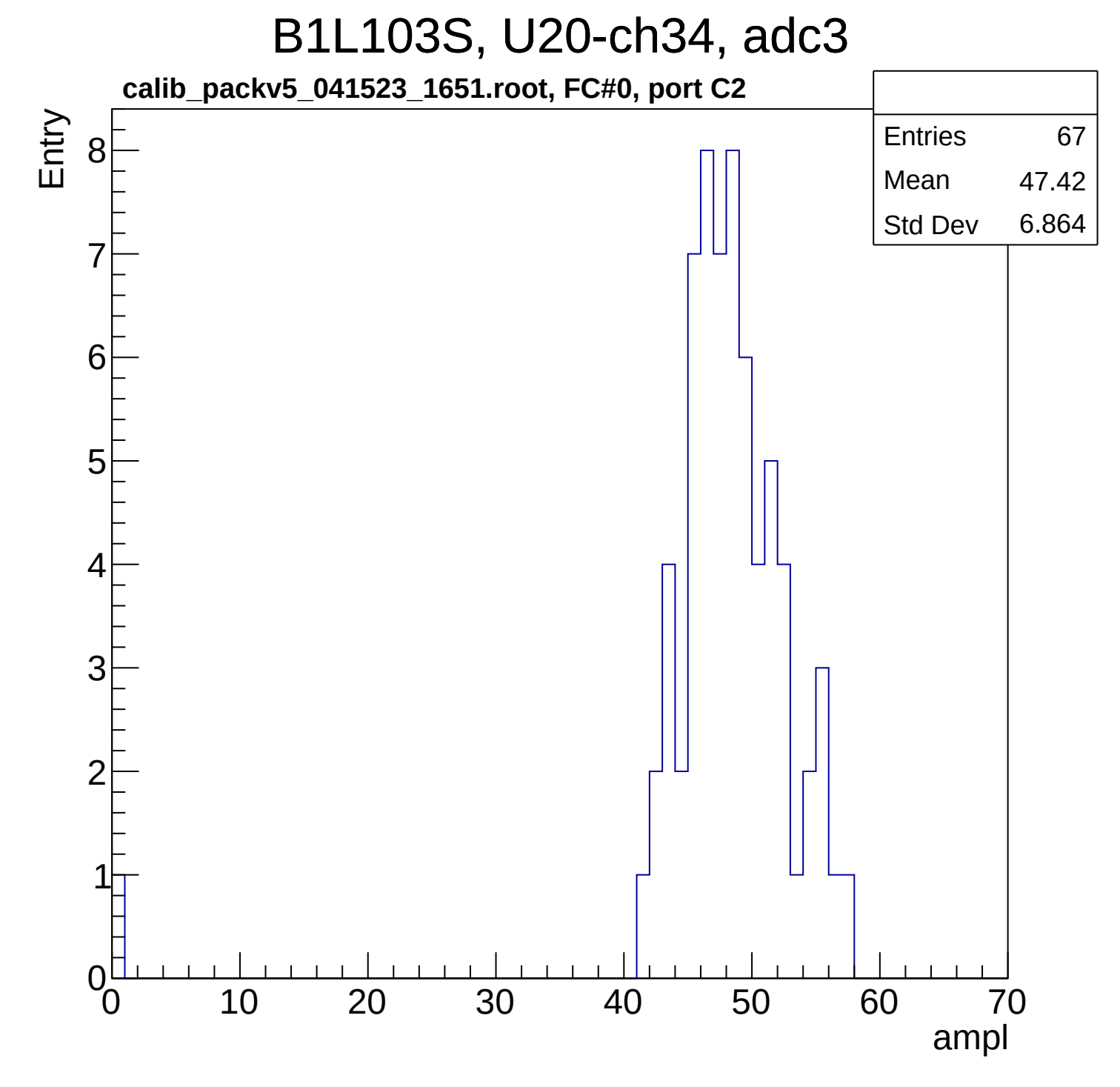
B1L103S, U20-ch34, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 47.42
Std Dev 6.864
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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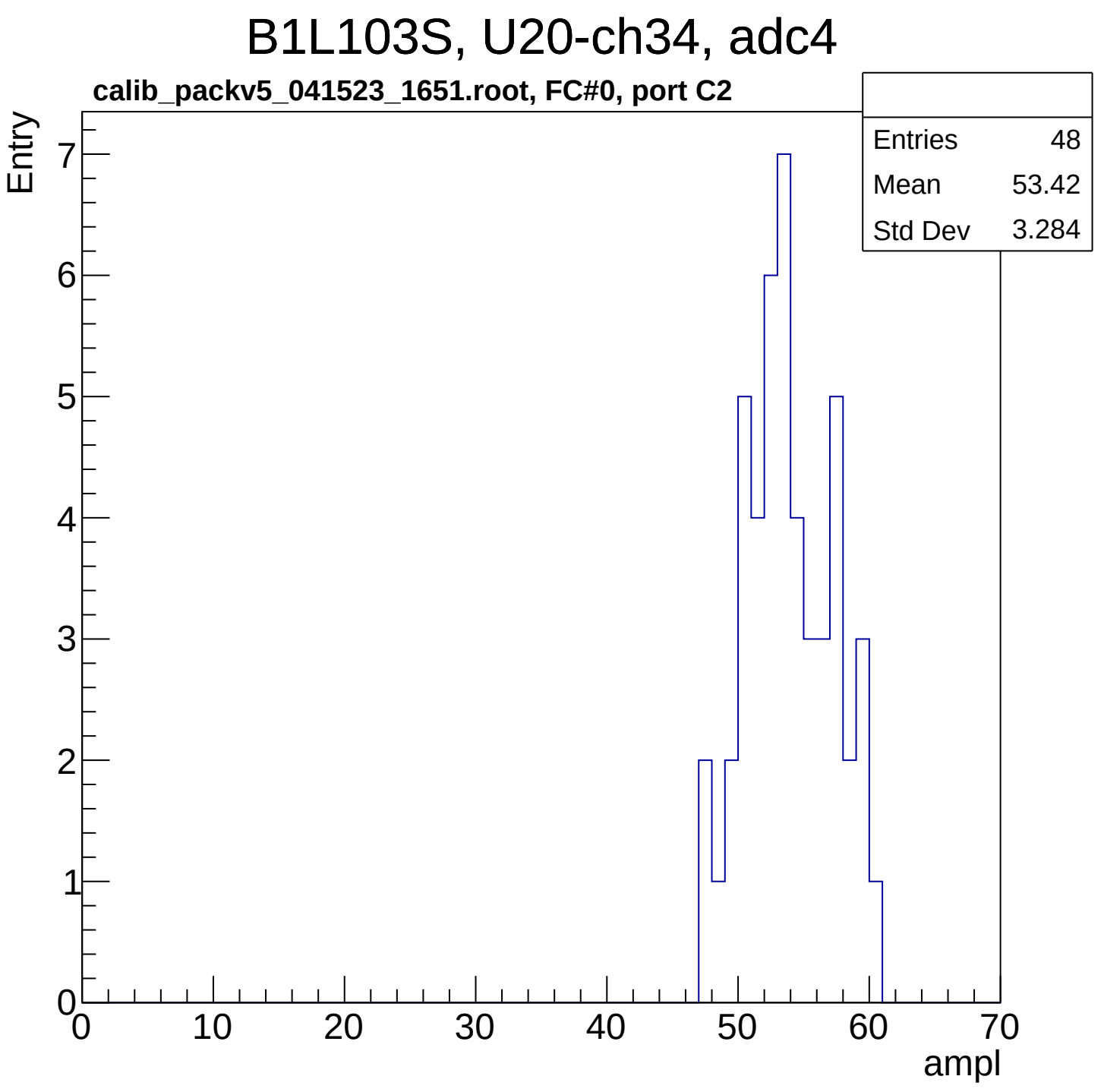
60
70


B1L103S, U20-ch34, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 53.42
Std Dev 3.284
Entry
ampl
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1
2
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4
5
6
7
0
10
20
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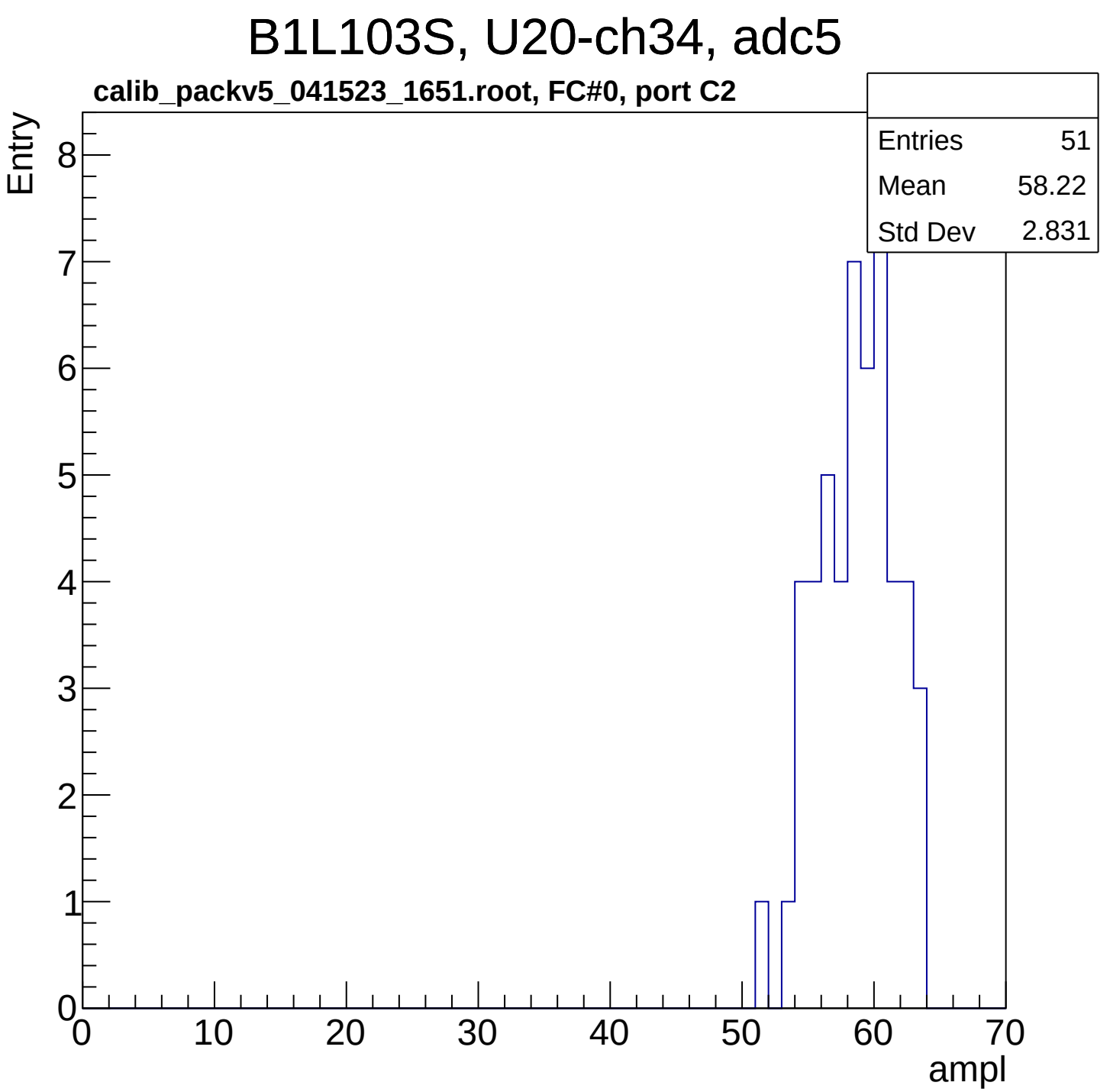
40
50
60
70


B1L103S, U20-ch34, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 58.22
Std Dev 2.831
Entry
ampl
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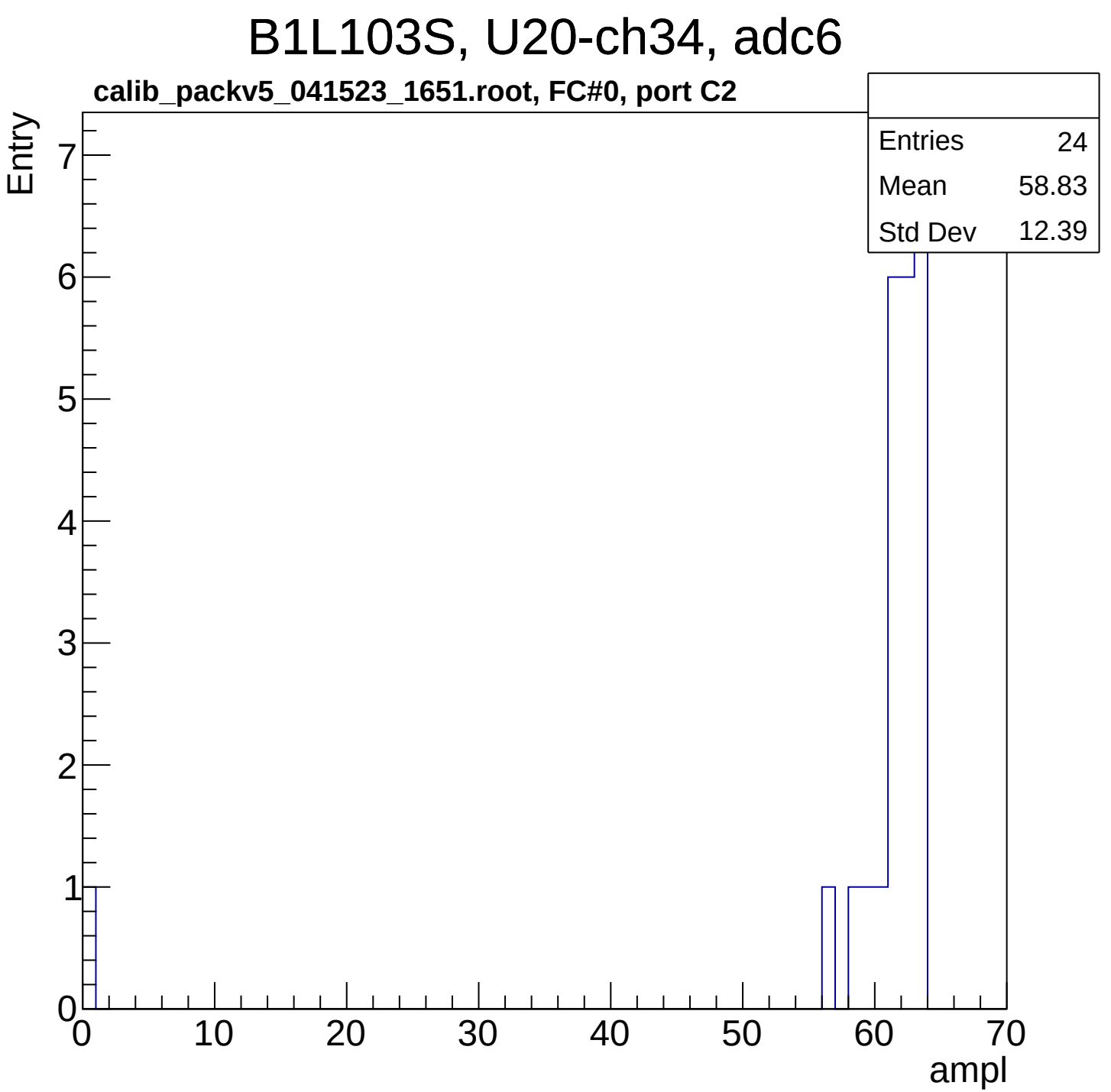
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch34, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 58.83
Std Dev 12.39
Entry
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1
2
3
4
5
6
7
0
10
20
30
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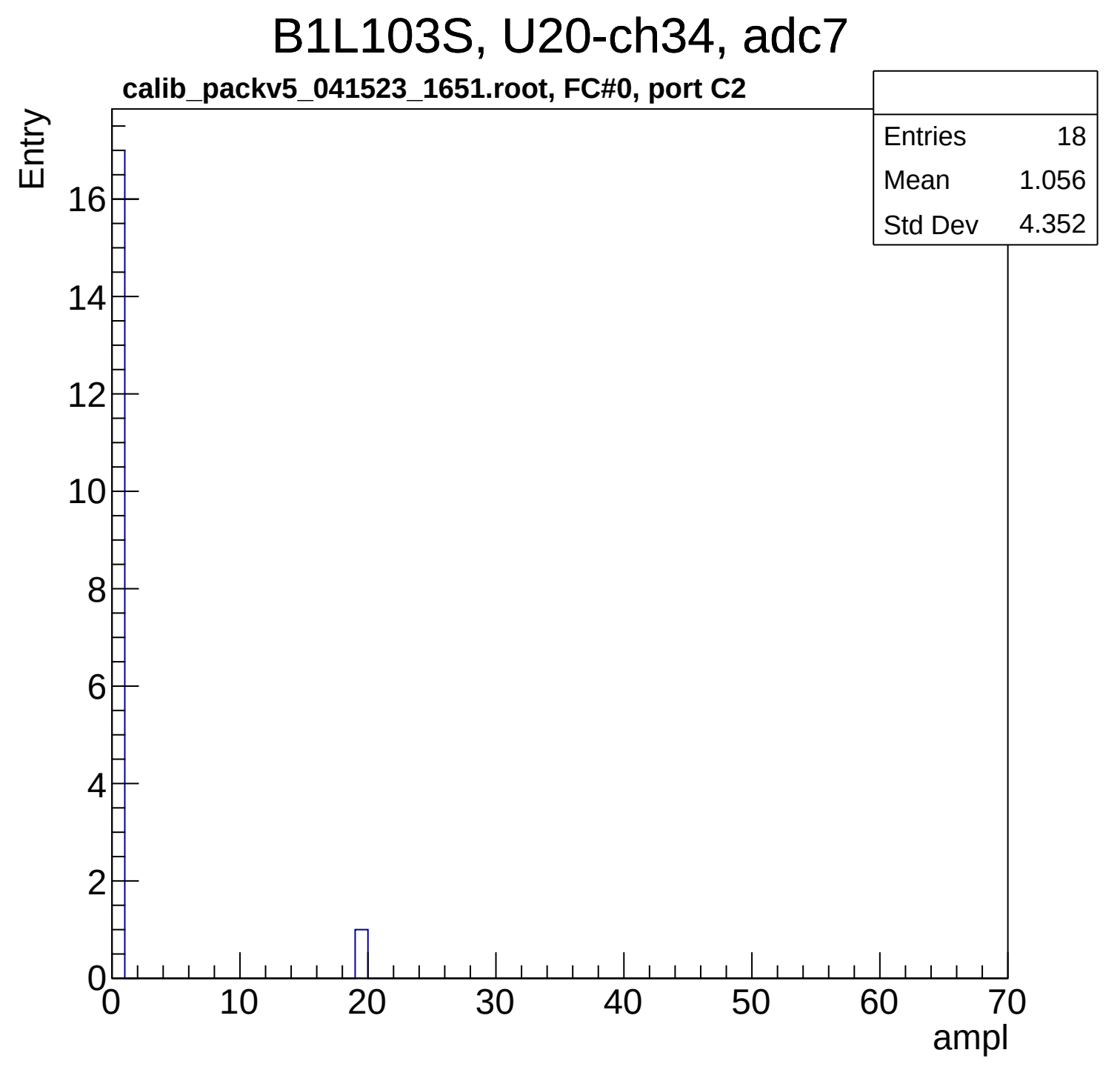
50
60
70
ampl


B1L103S, U20-ch34, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.056
Std Dev 4.352
Entry
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4
6
8
10
12
14
16
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10
20
30
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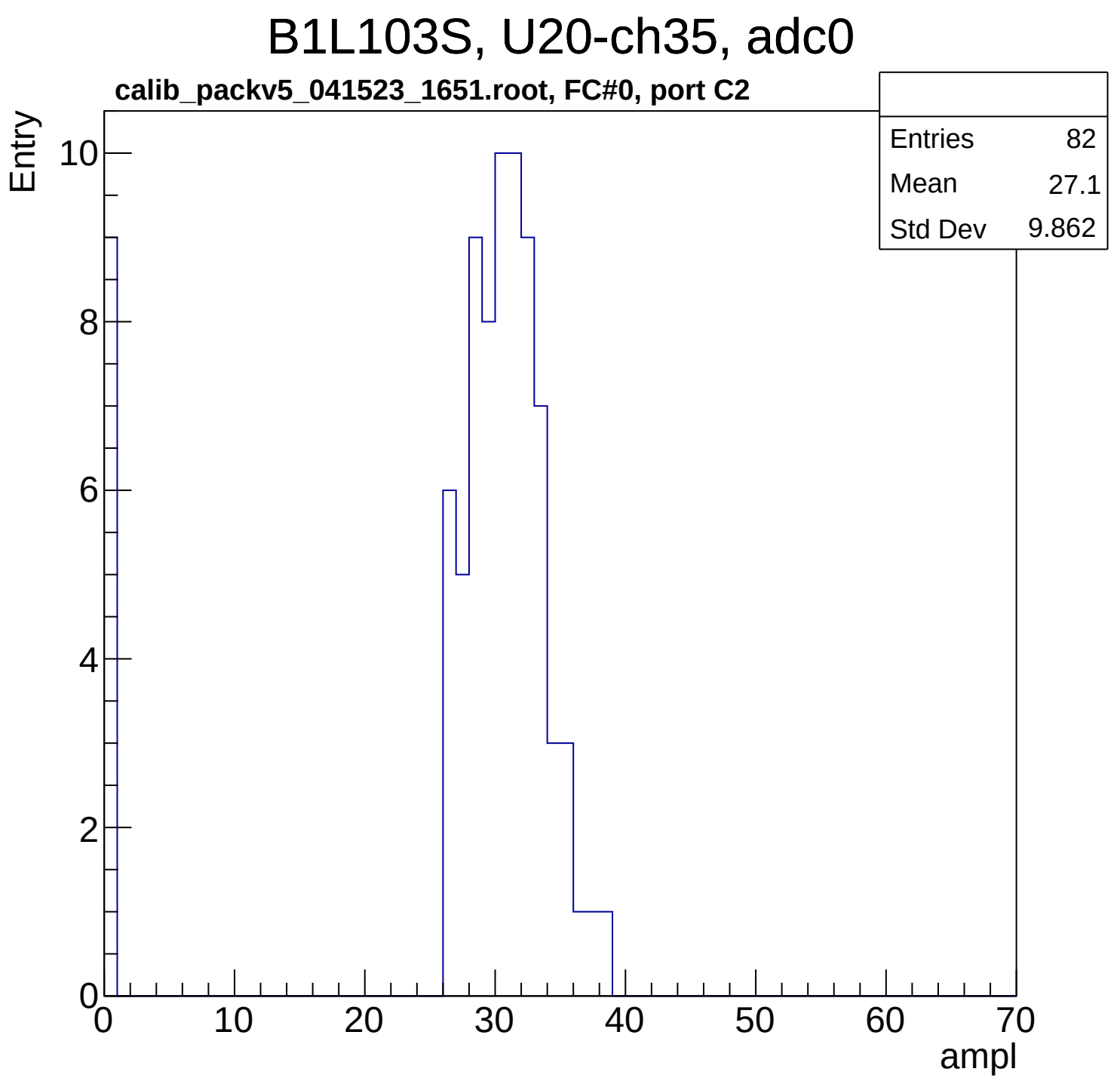
50
60
70
ampl


B1L103S, U20-ch35, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 27.1
Std Dev 9.862
Entry
ampl
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8
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0
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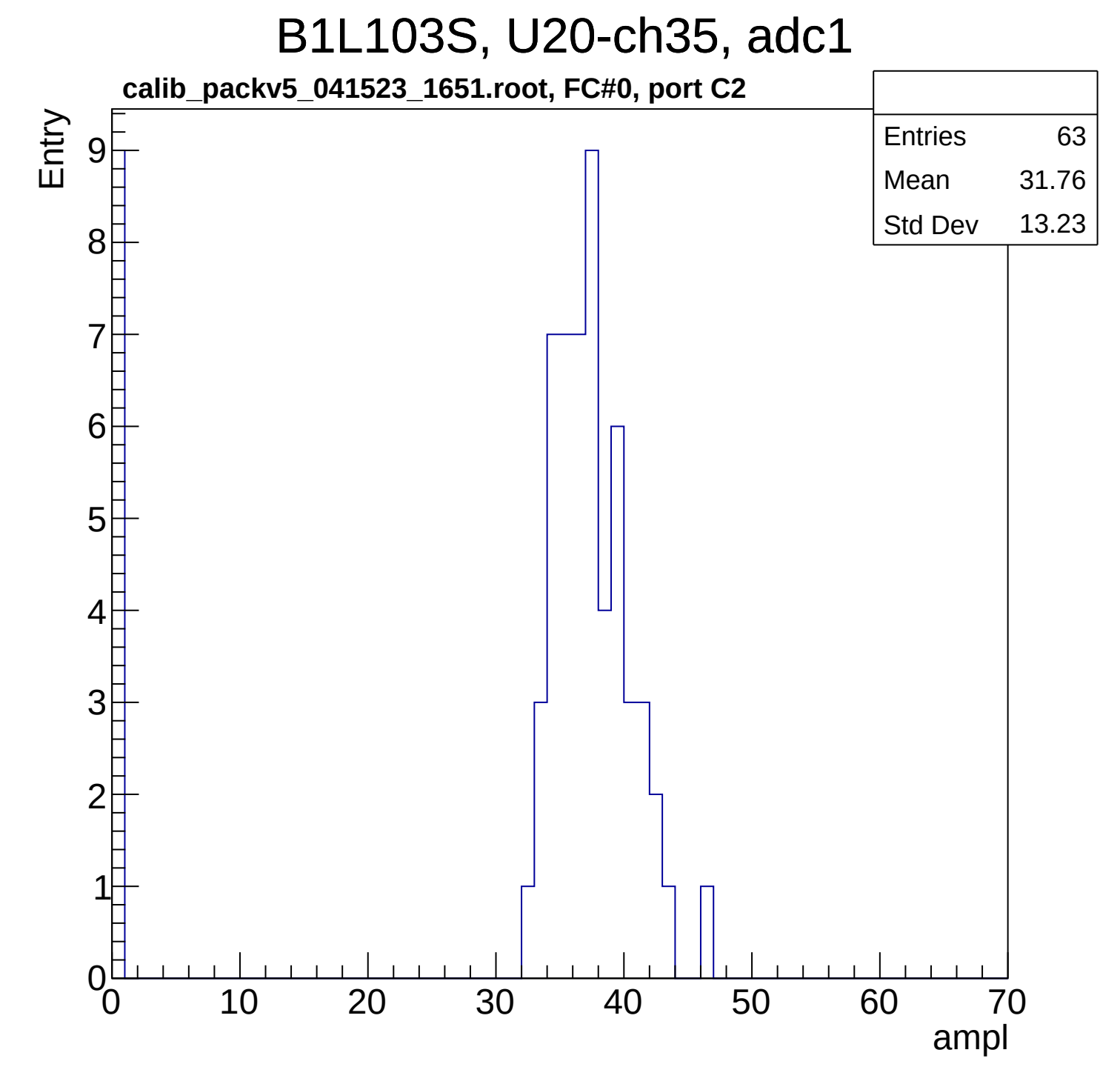
40
50
60
70


B1L103S, U20-ch35, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 31.76
Std Dev 13.23
Entry
ampl
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4
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6
7
8
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0
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40
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60
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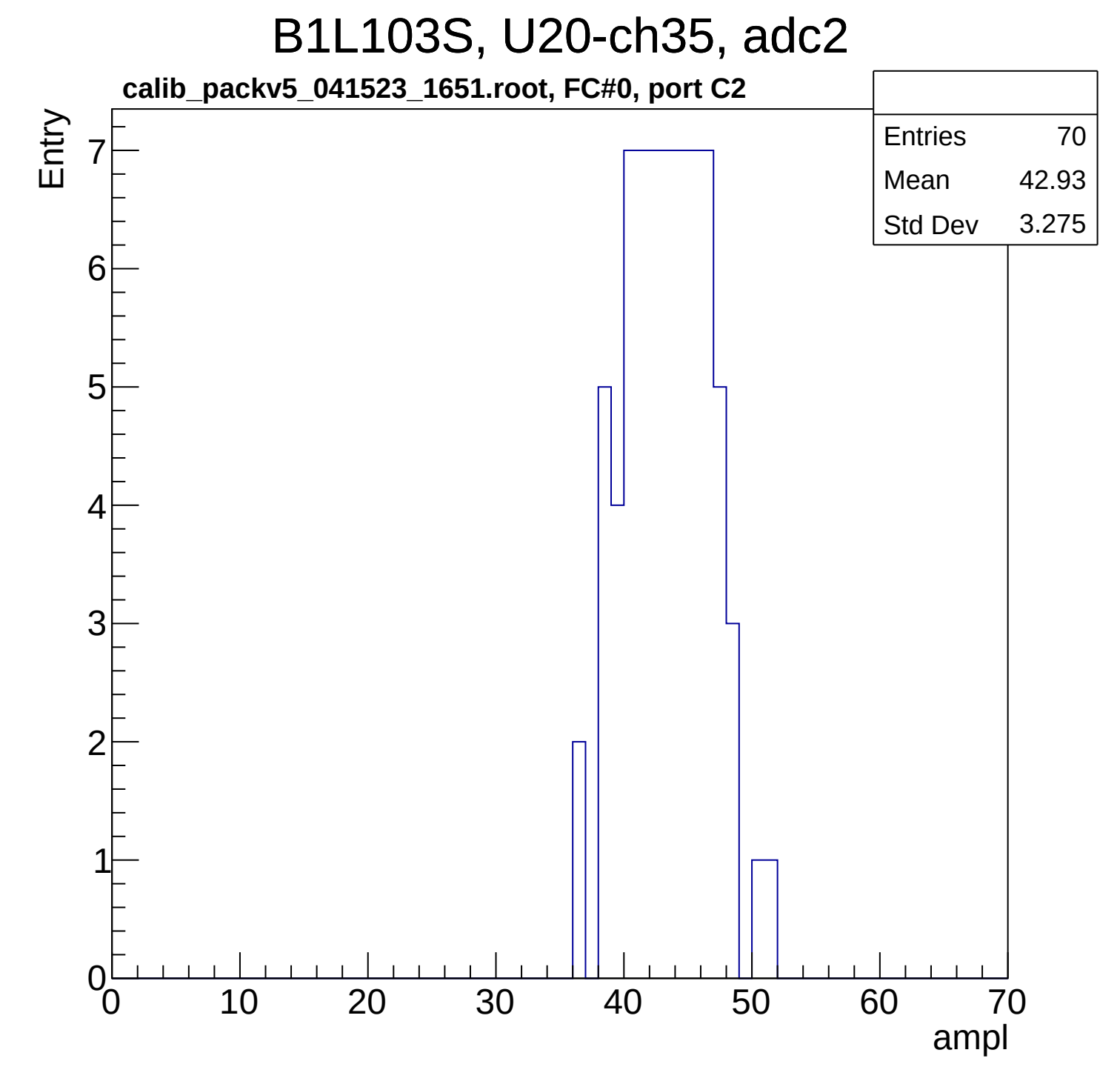
B1L103S, U20-ch35, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 42.93
Std Dev 3.275
Entry
ampl
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4
5
6
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0
10
20
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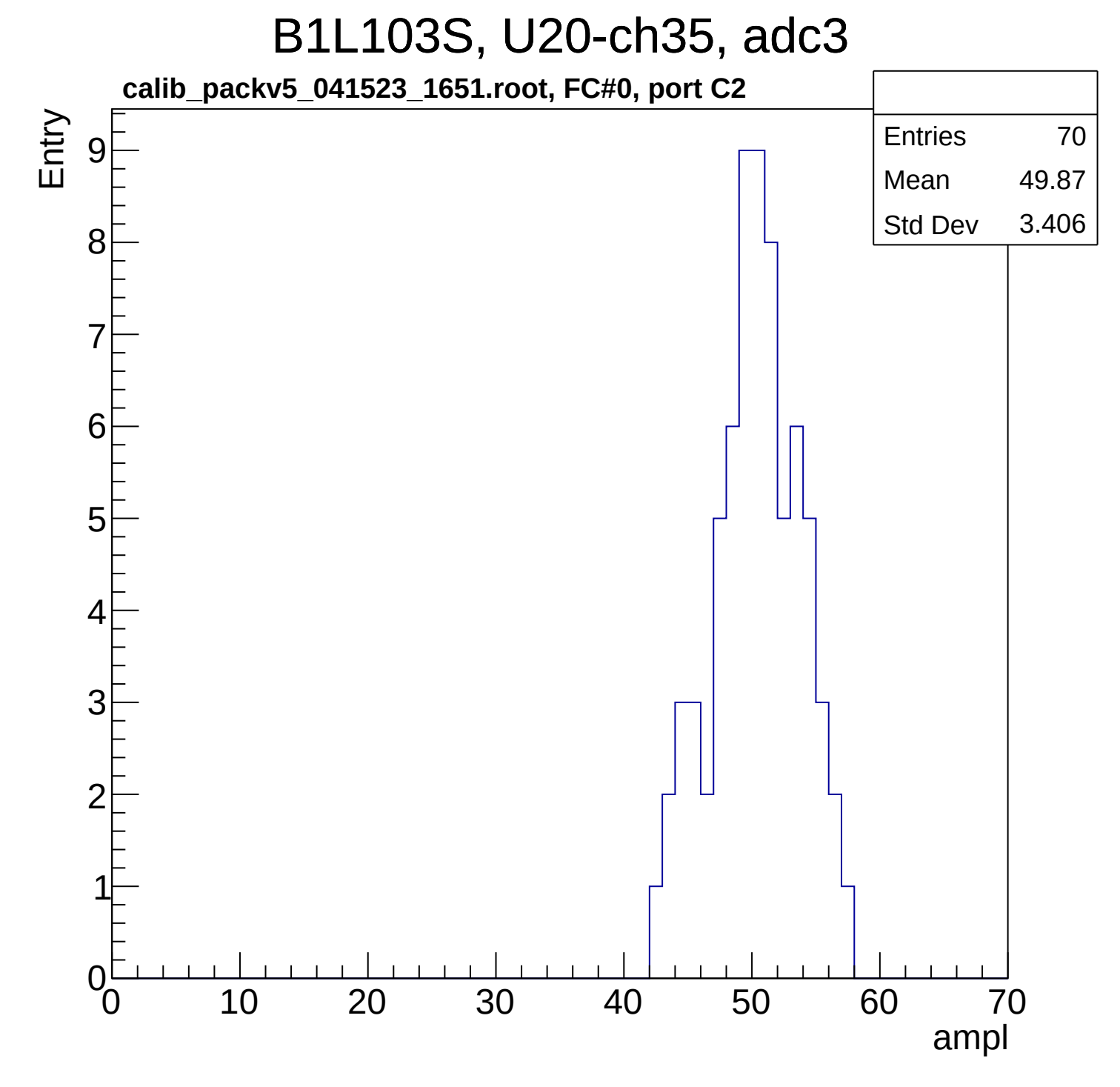
60
70


B1L103S, U20-ch35, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 49.87
Std Dev 3.406
Entry
ampl
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5
6
7
8
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0
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40
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60
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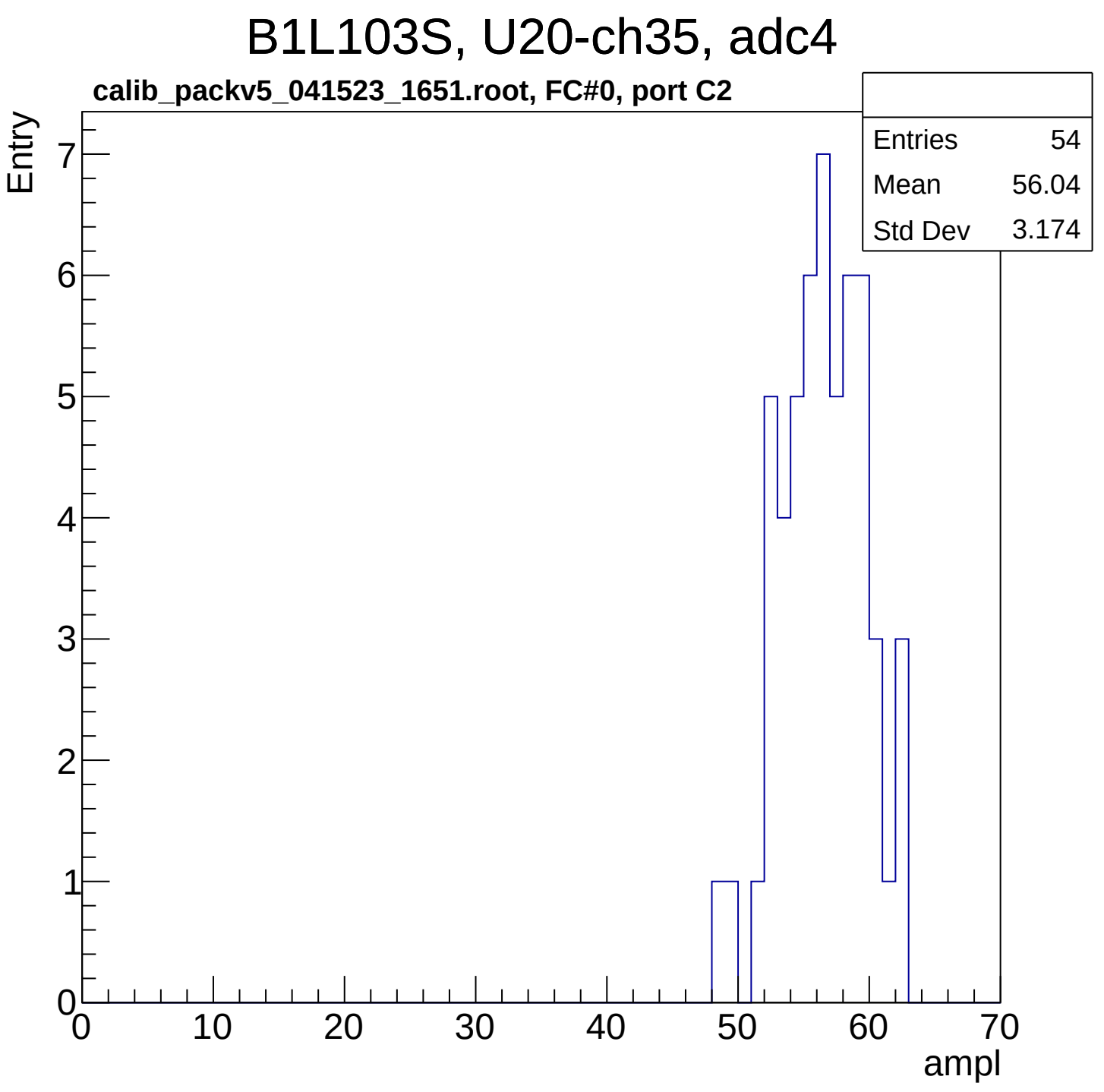
B1L103S, U20-ch35, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 56.04
Std Dev 3.174
Entry
ampl
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3
4
5
6
7
0
10
20
30
40
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60
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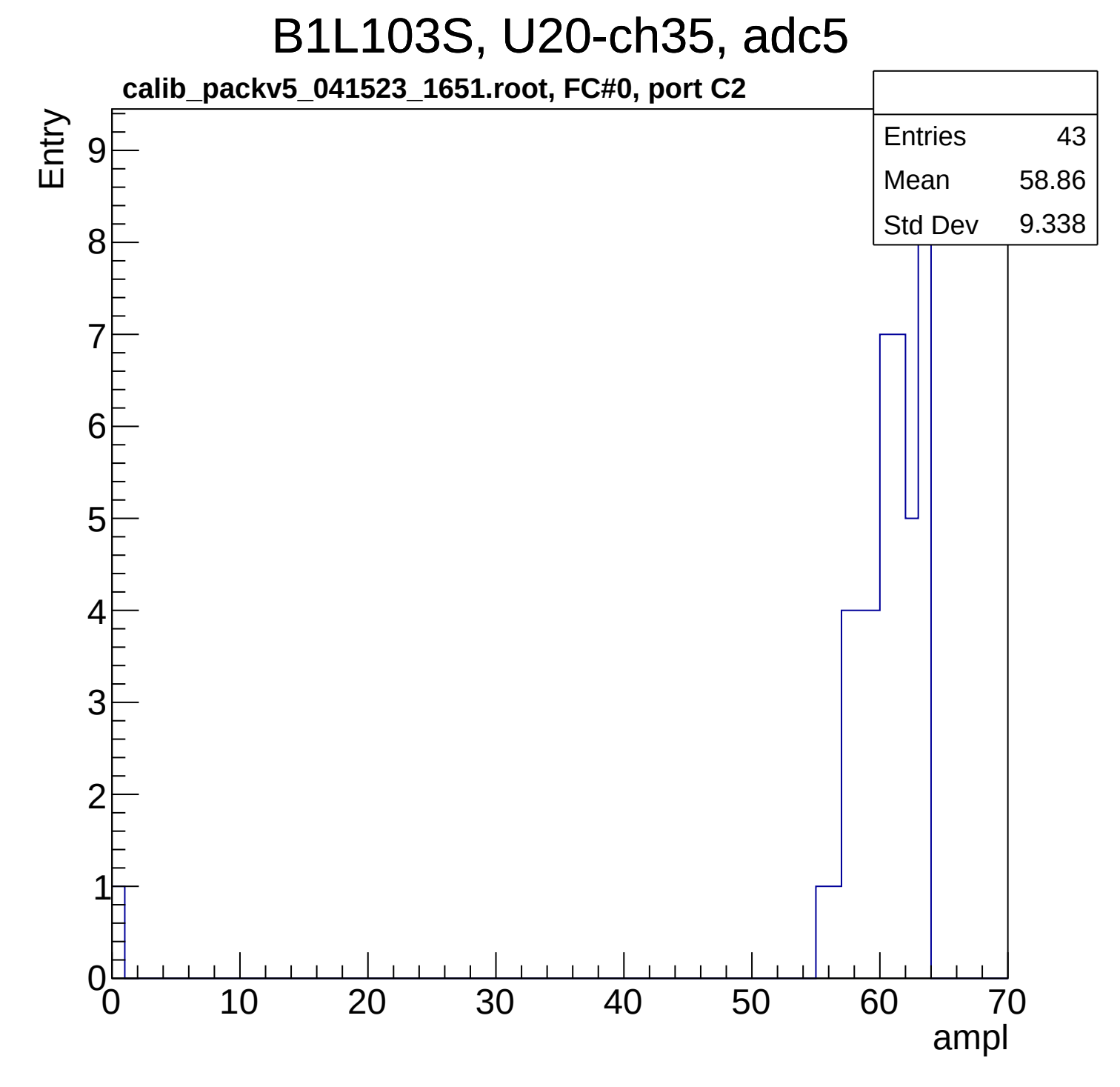
B1L103S, U20-ch35, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 58.86
Std Dev 9.338
Entry
ampl
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3
4
5
6
7
8
9
0
10
20
30
40
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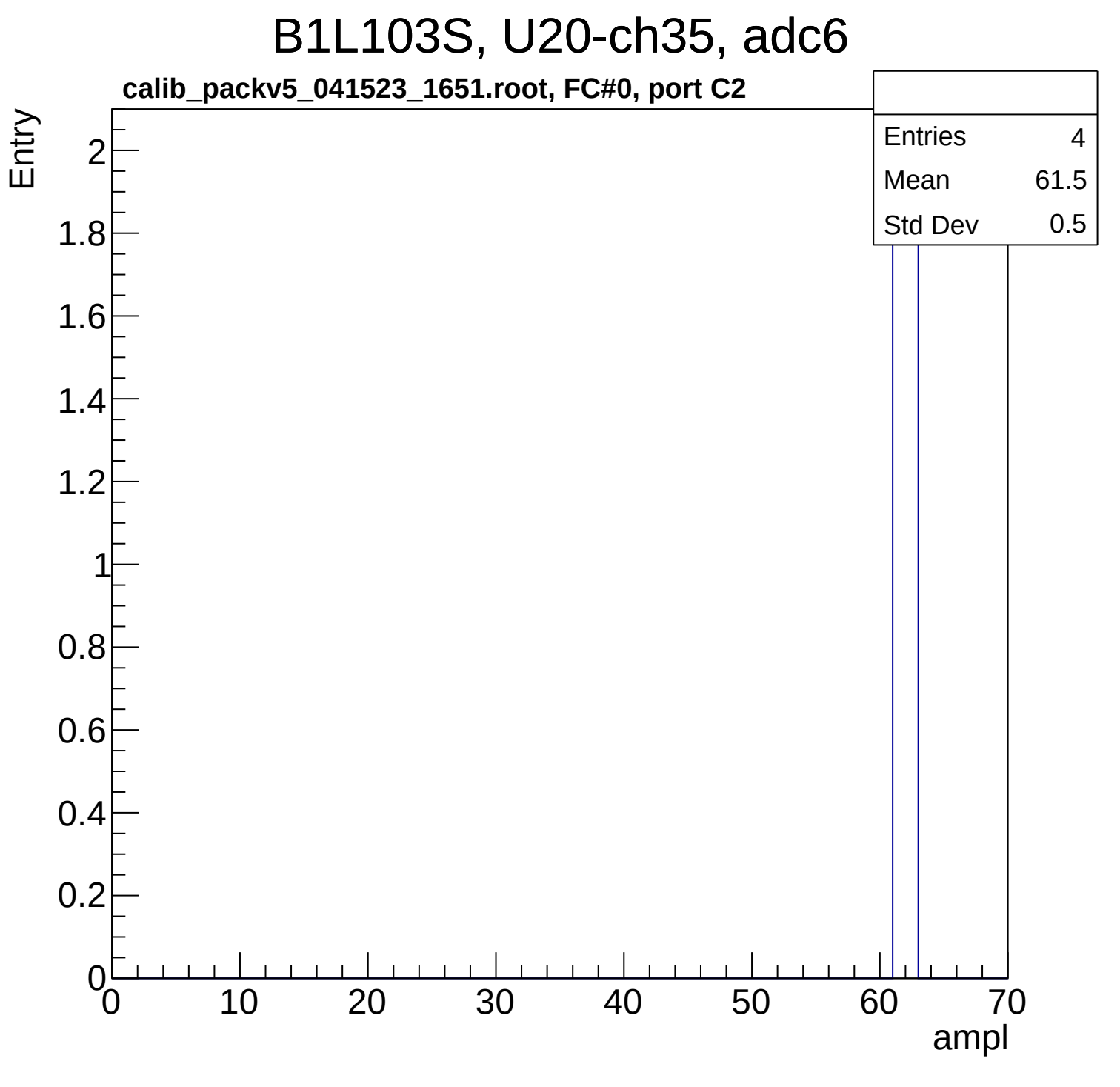
60
70


B1L103S, U20-ch35, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 61.5
Std Dev 0.5
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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60
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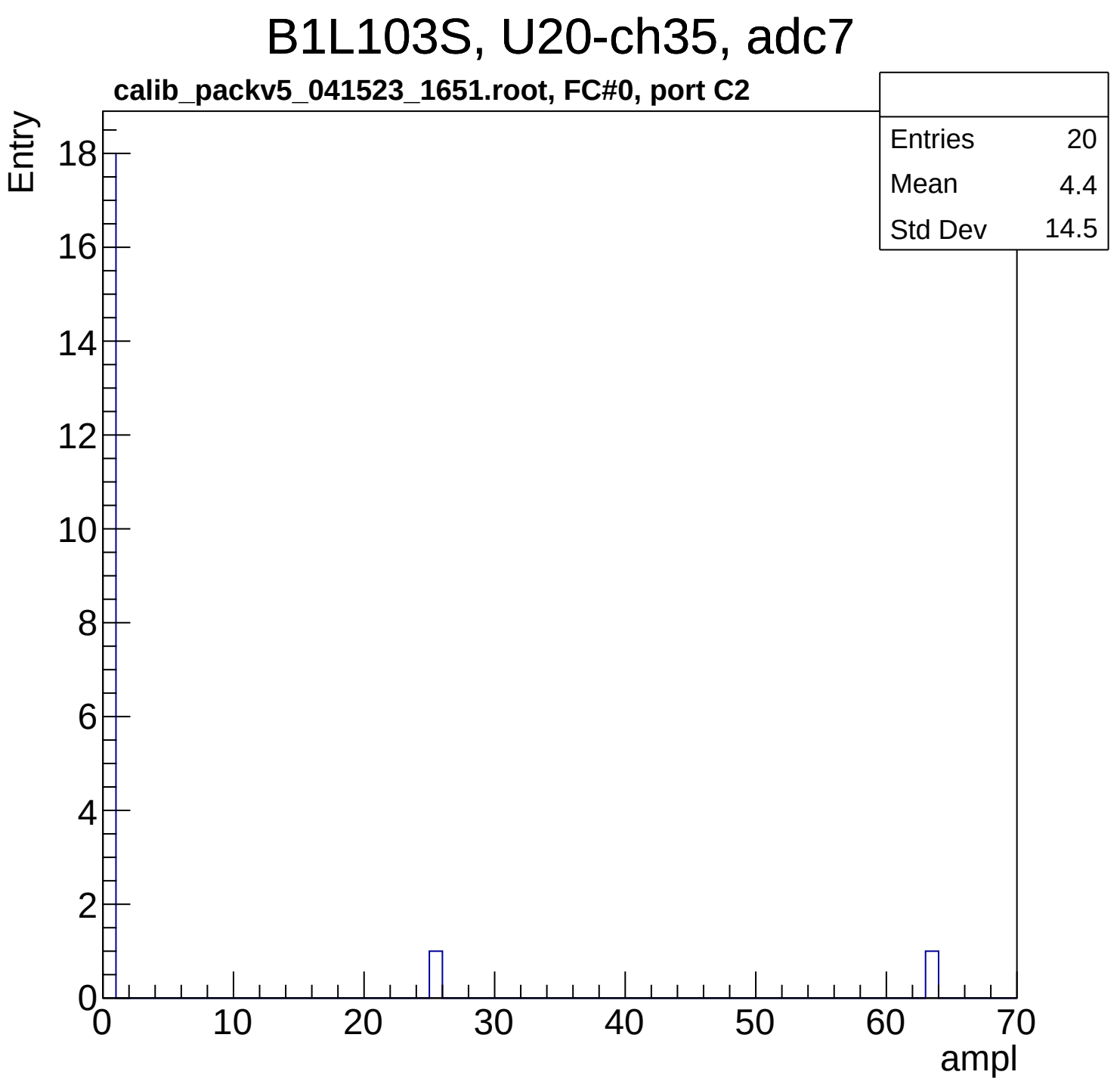
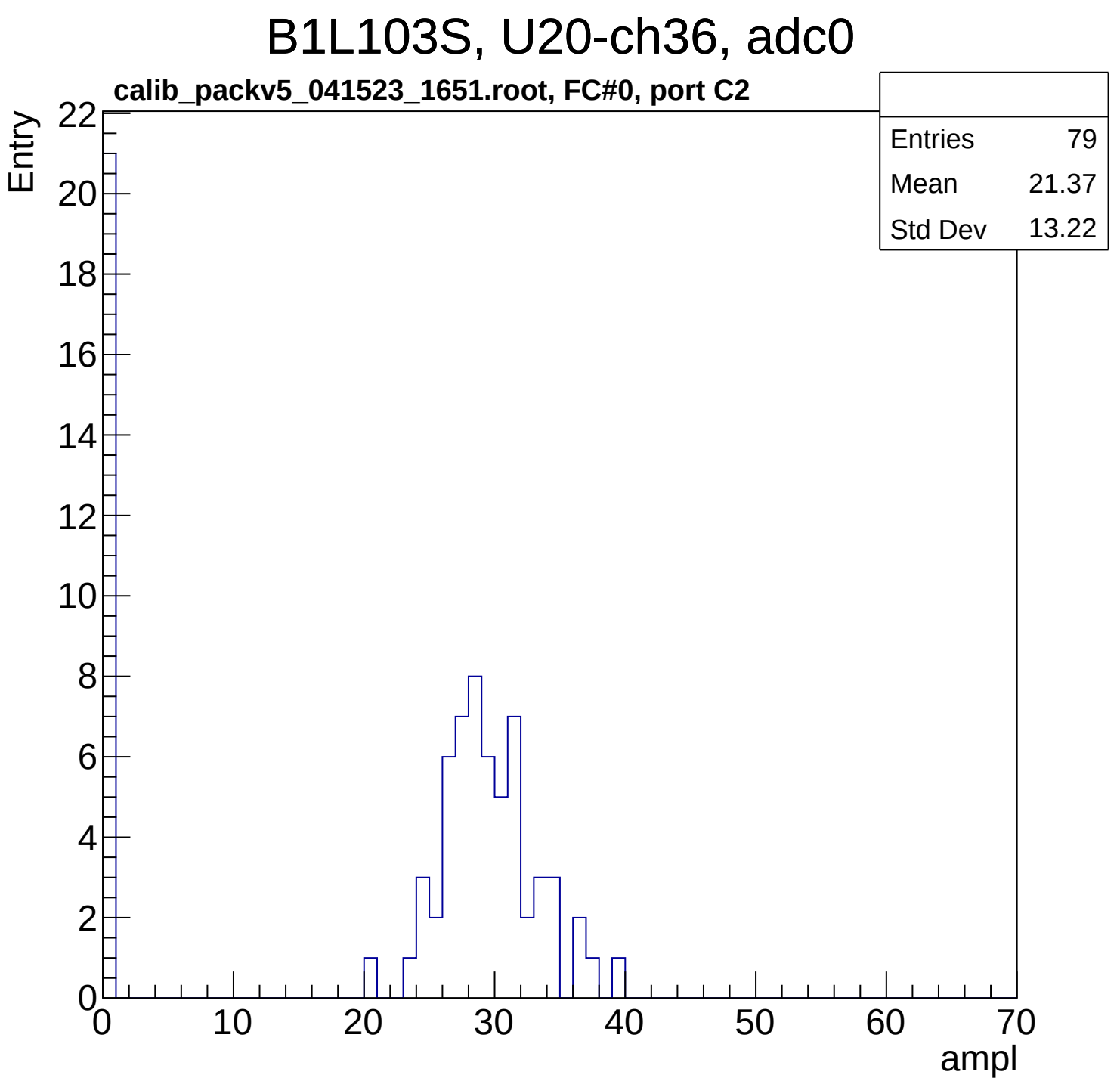
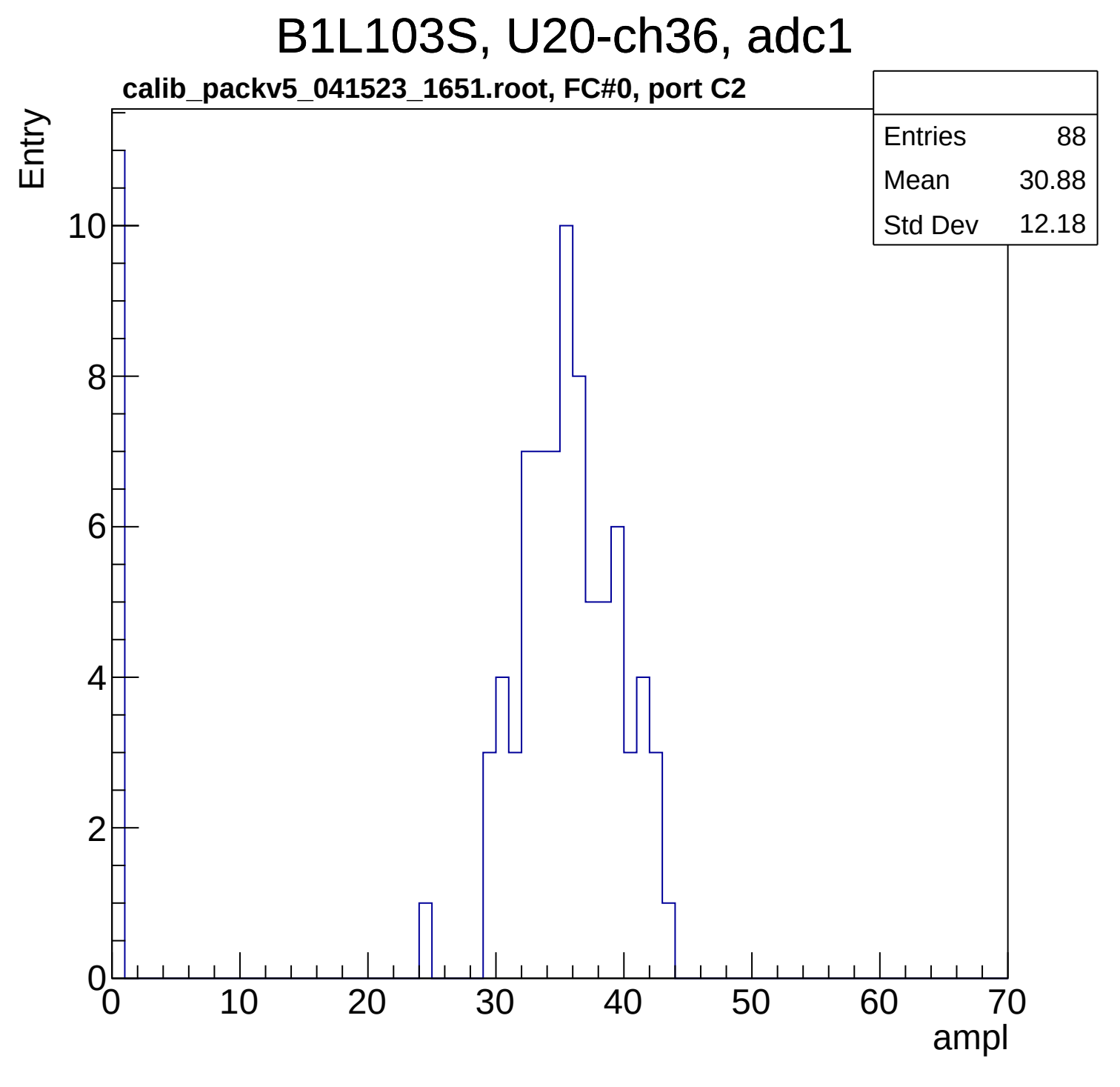
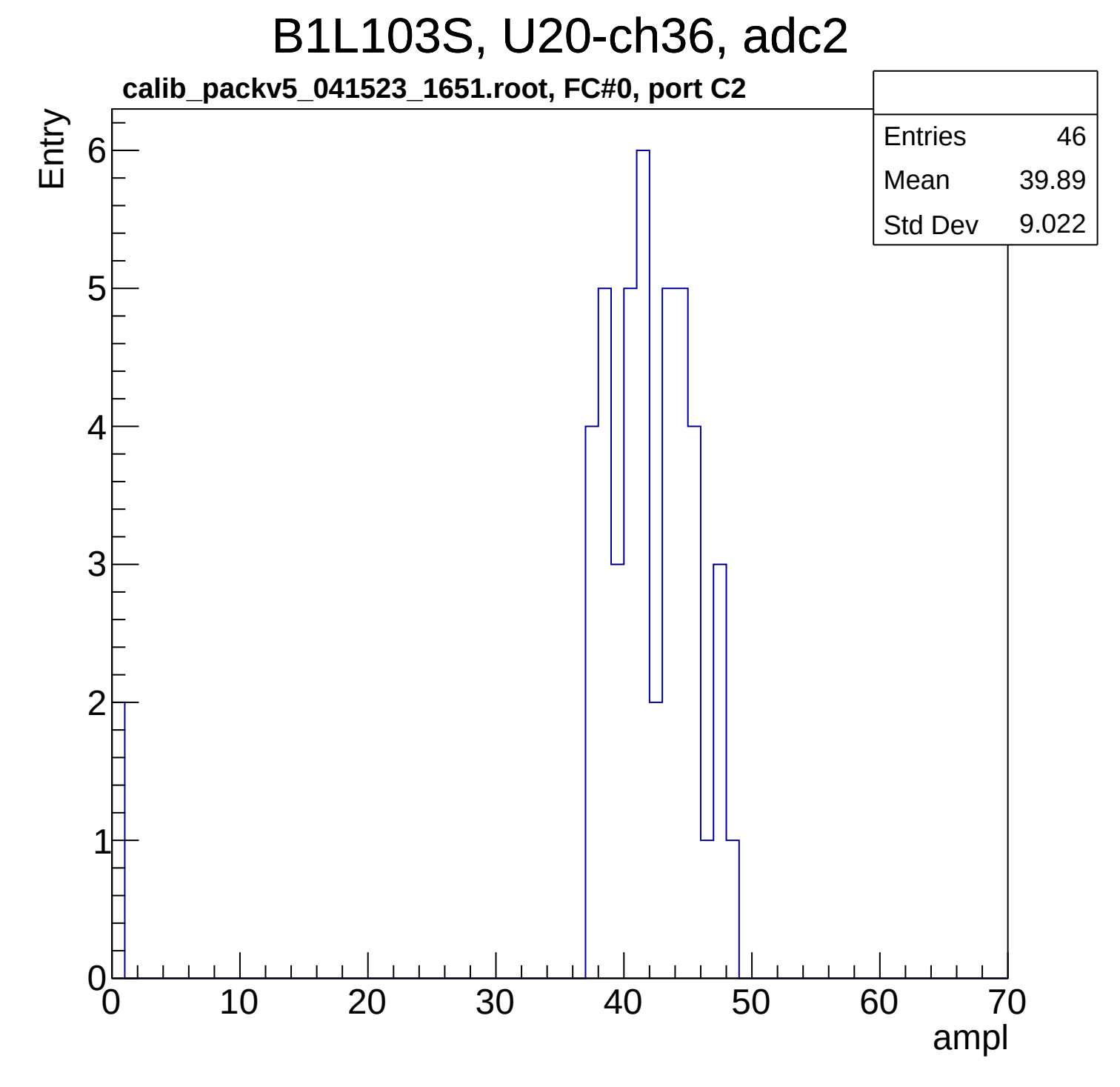
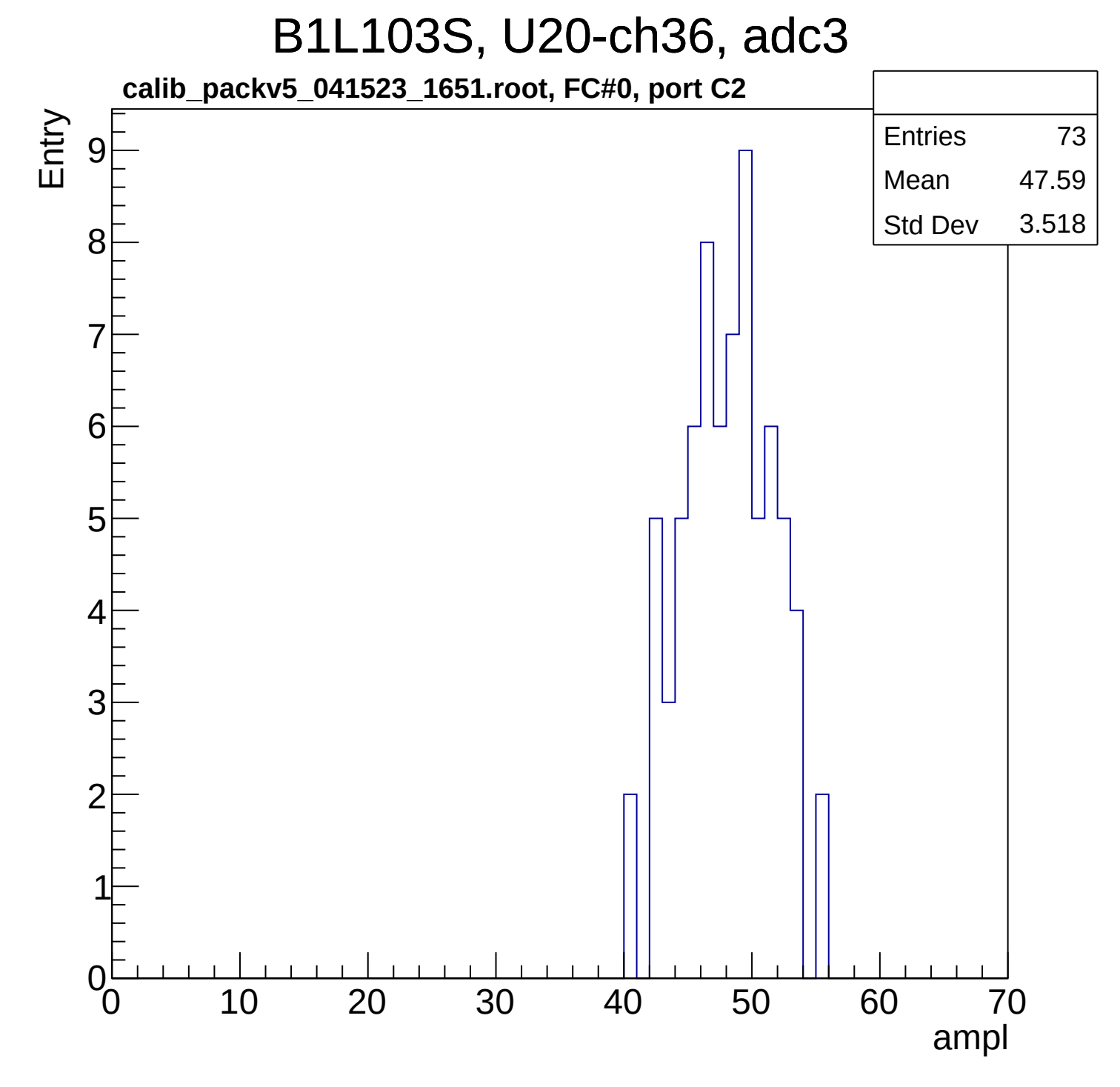

B1L103S, U20-ch35, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4.4
Std Dev 14.5
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch36, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 21.37
Std Dev 13.22
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70


B1L103S, U20-ch36, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 30.88
Std Dev 12.18
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch36, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 39.89
Std Dev 9.022
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch36, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 47.59
Std Dev 3.518
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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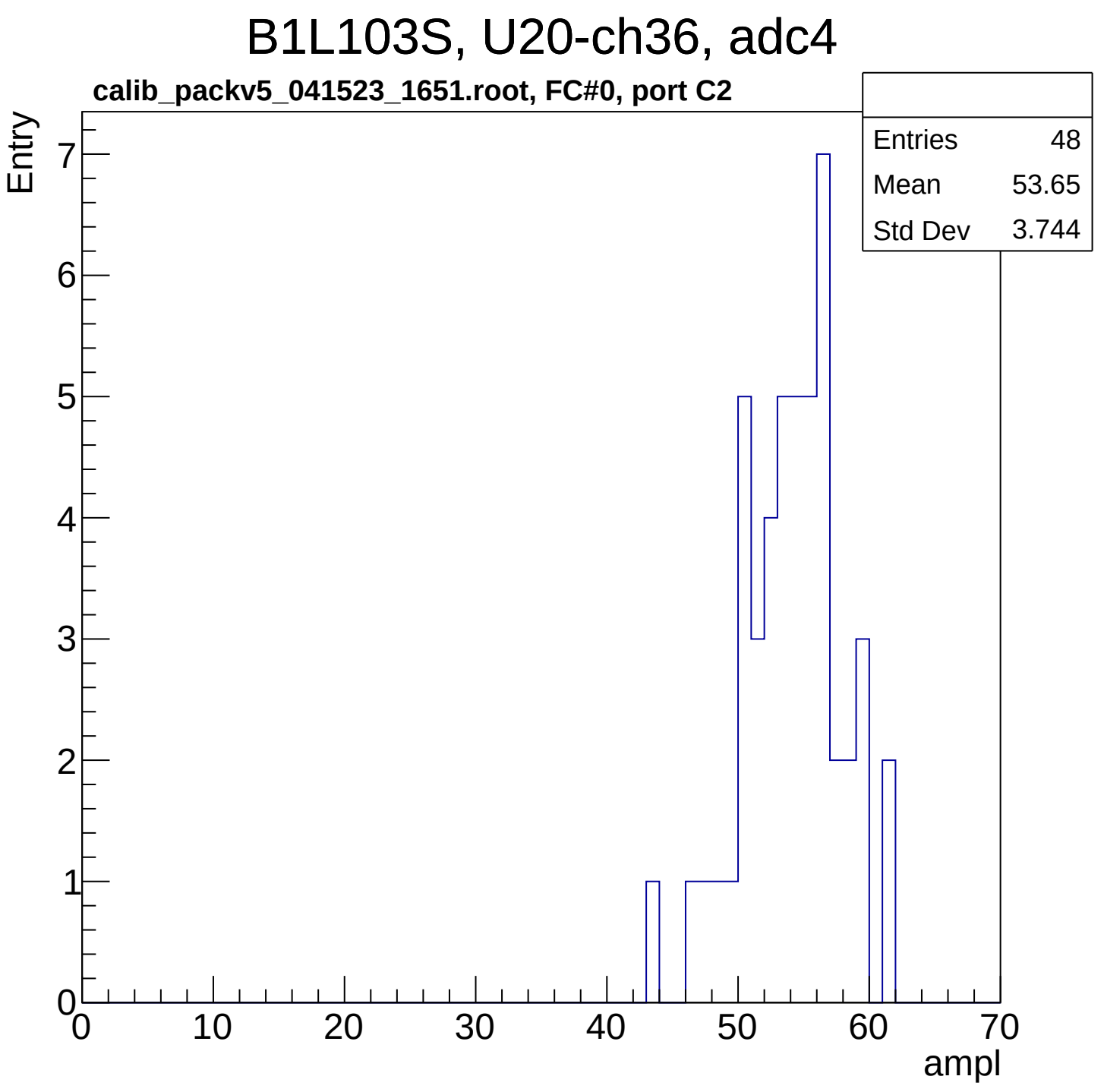
B1L103S, U20-ch36, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 53.65
Std Dev 3.744
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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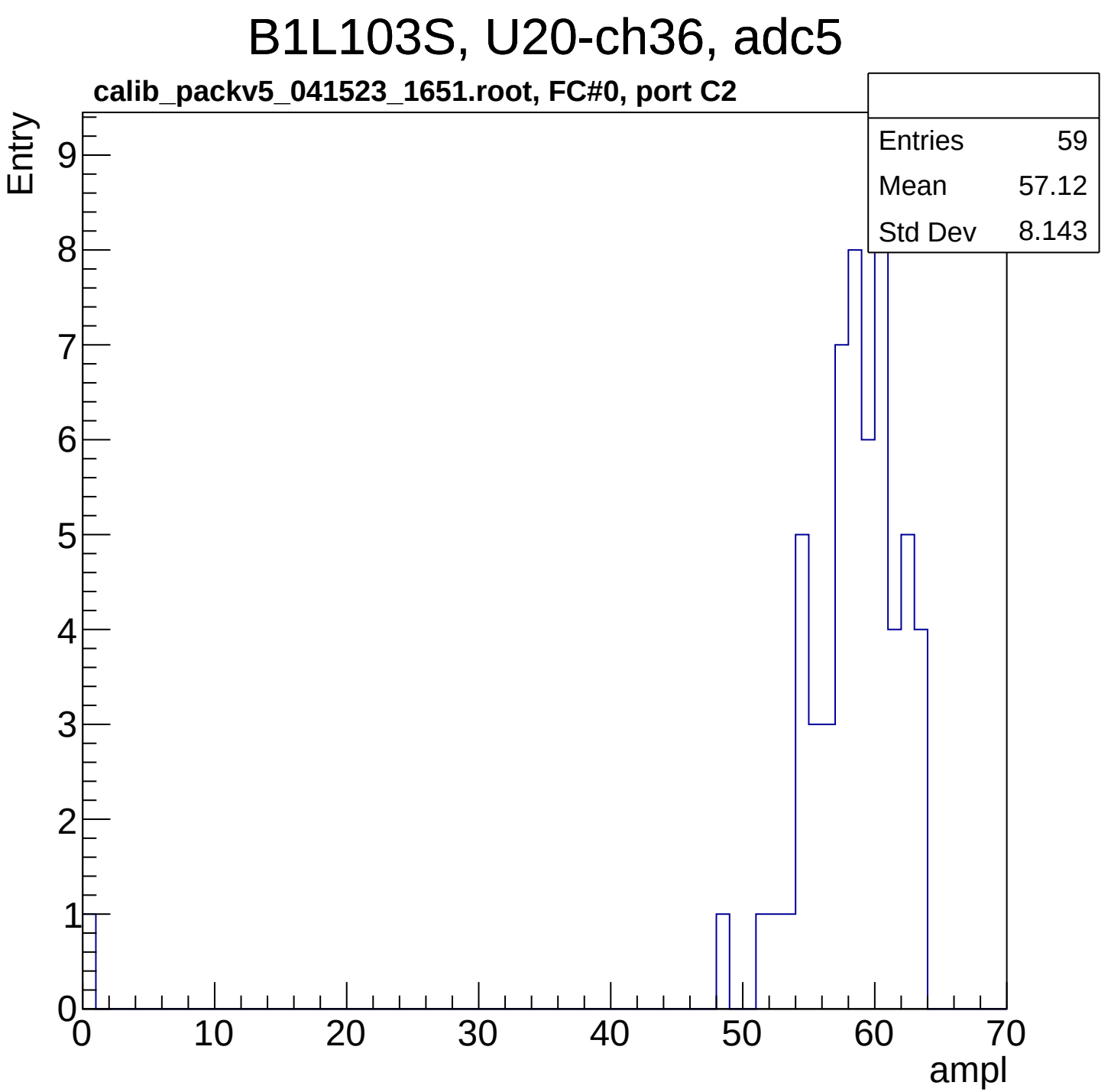
B1L103S, U20-ch36, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 57.12
Std Dev 8.143
Entry
ampl
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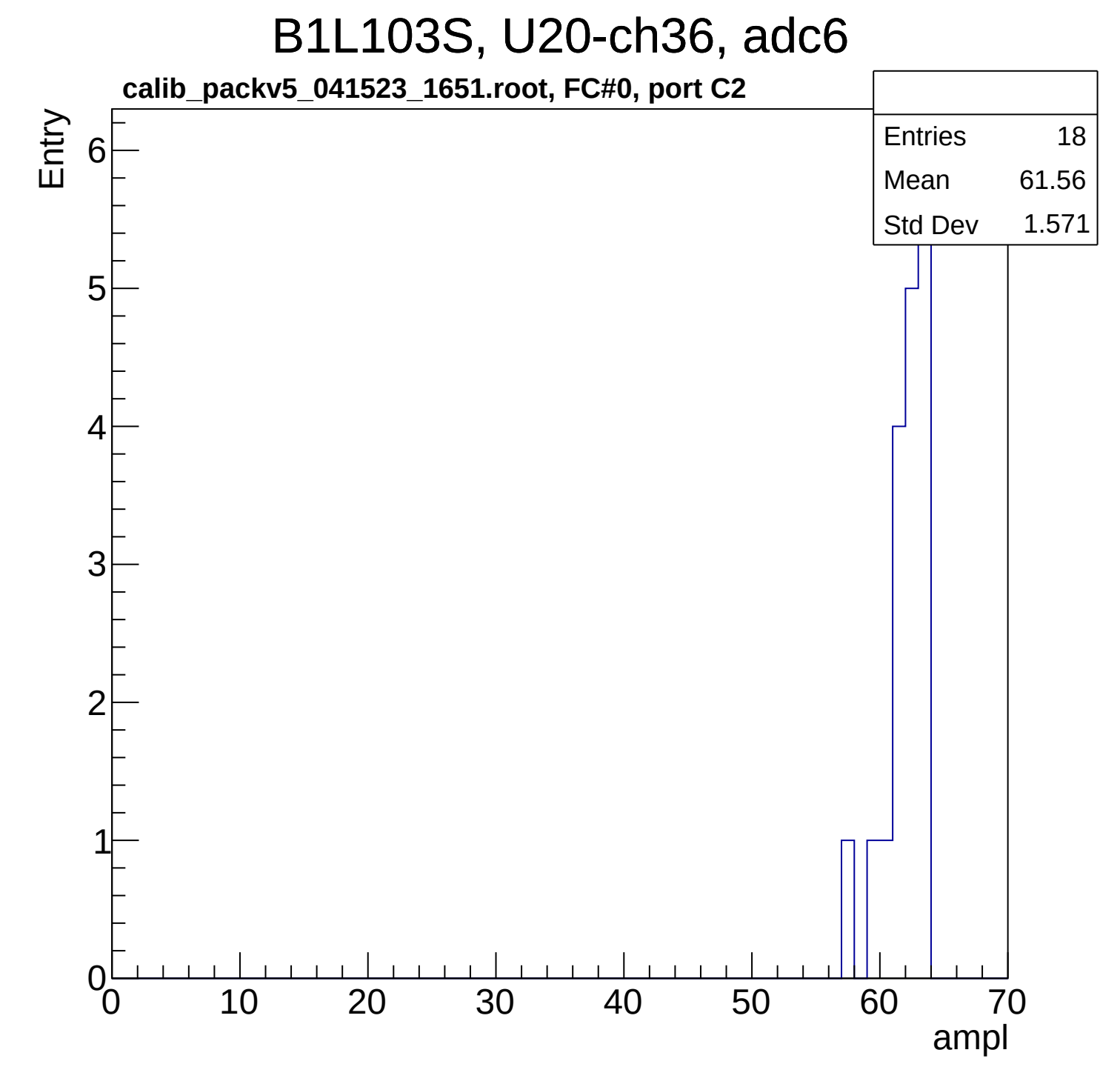
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch36, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 61.56
Std Dev 1.571
Entry
ampl
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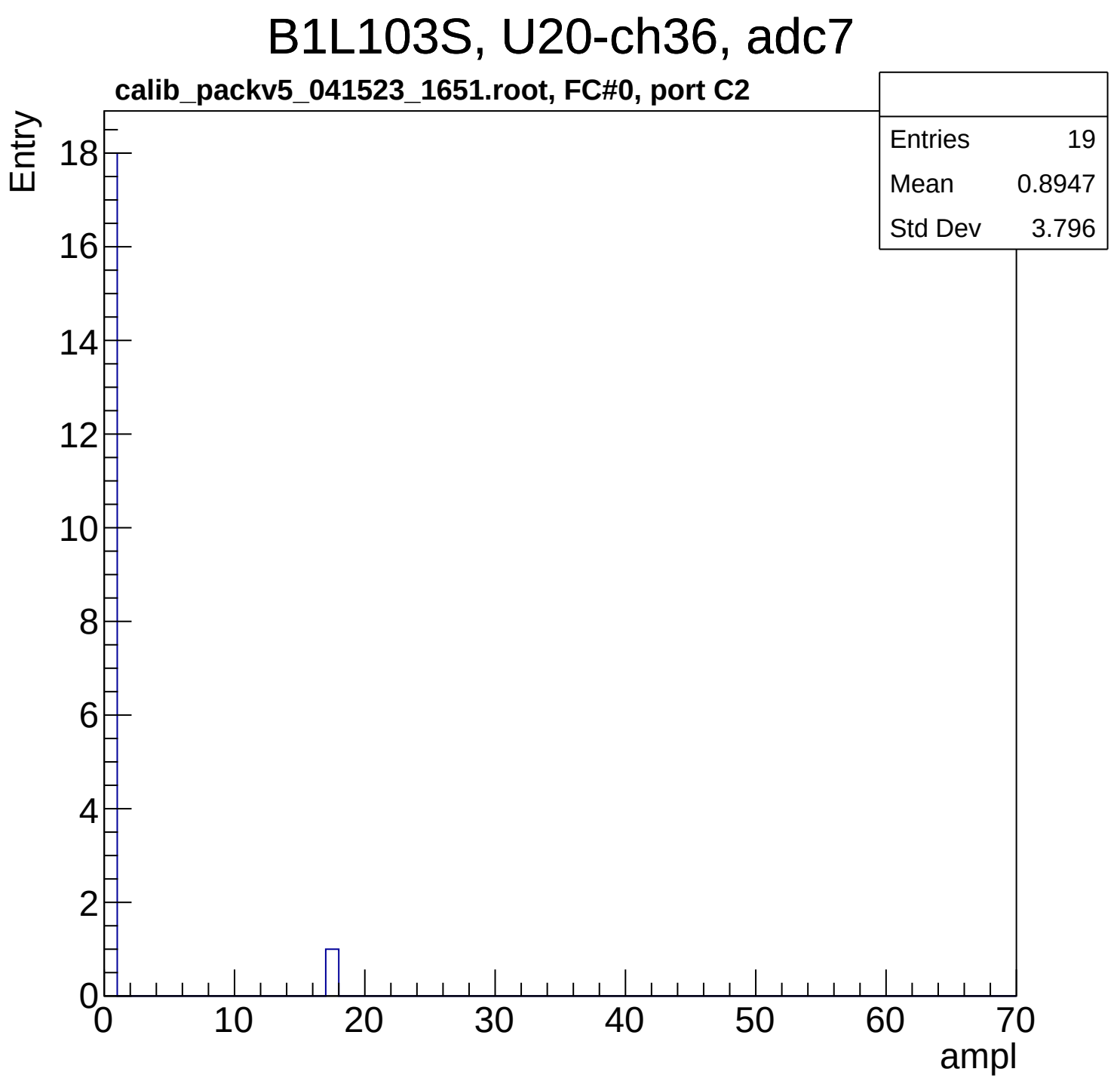
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U20-ch36, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0.8947
Std Dev 3.796
Entry
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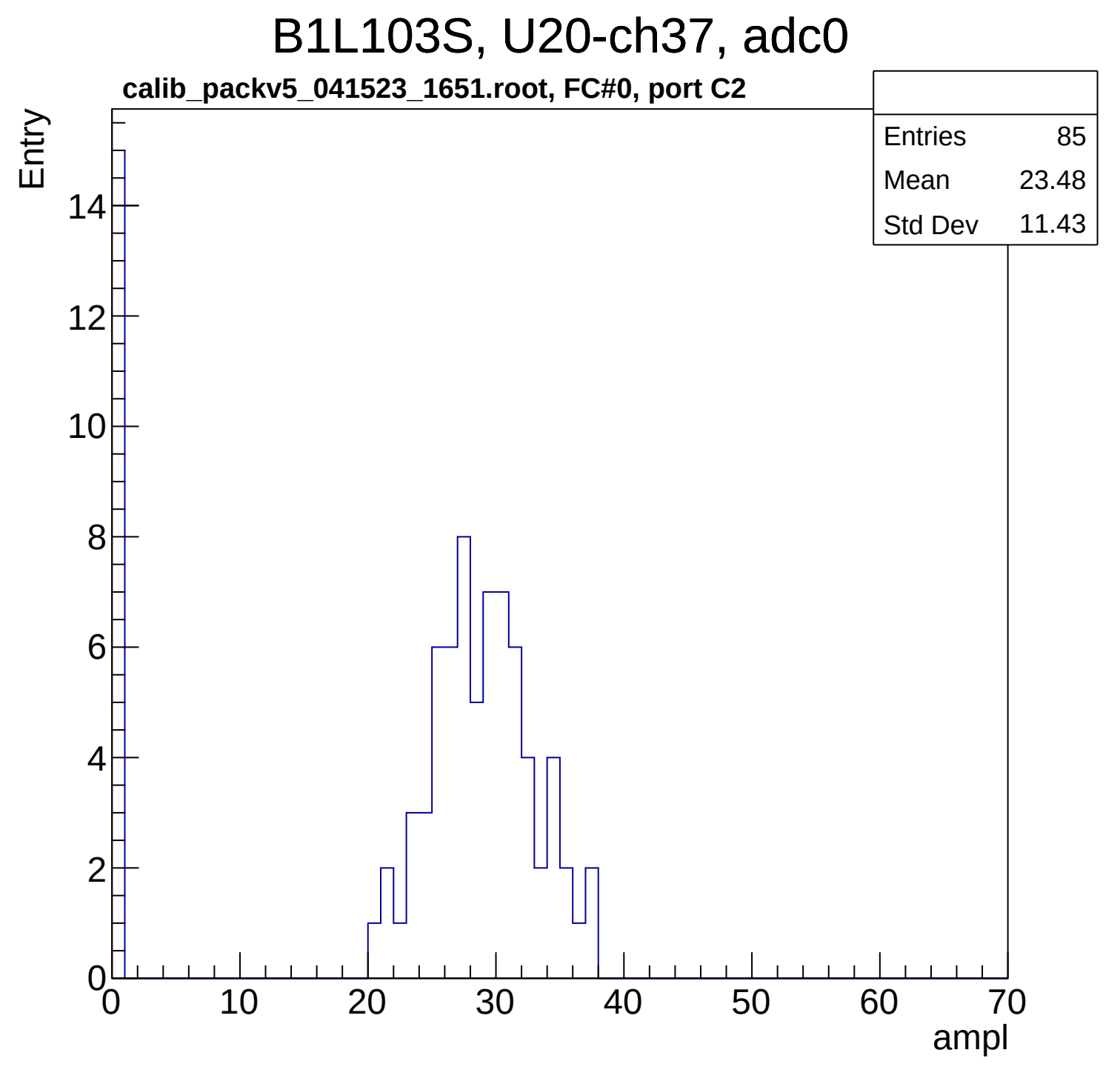
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch37, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 23.48
Std Dev 11.43
Entry
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2
4
6
8
10
12
14
0
10
20
30
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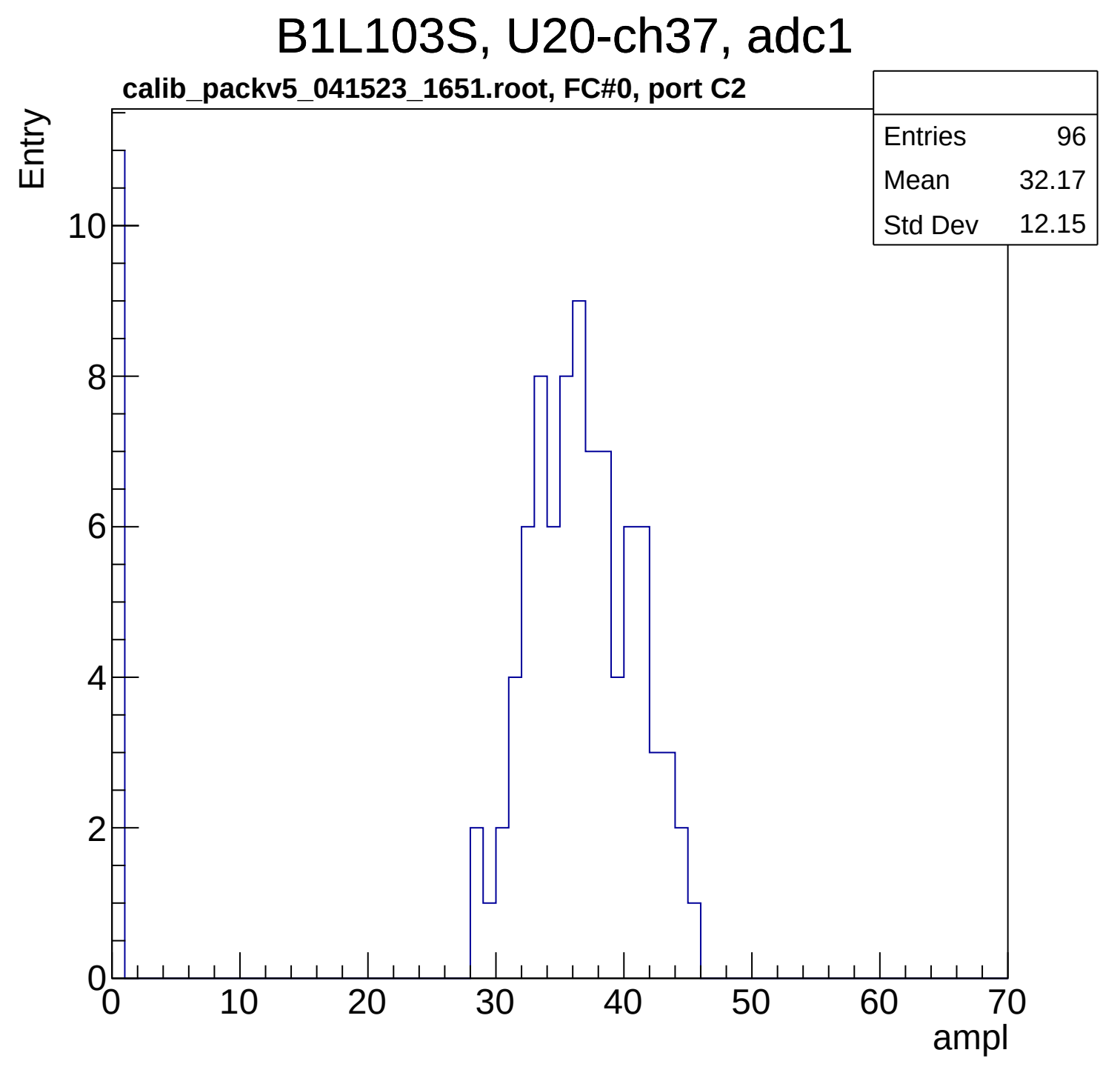
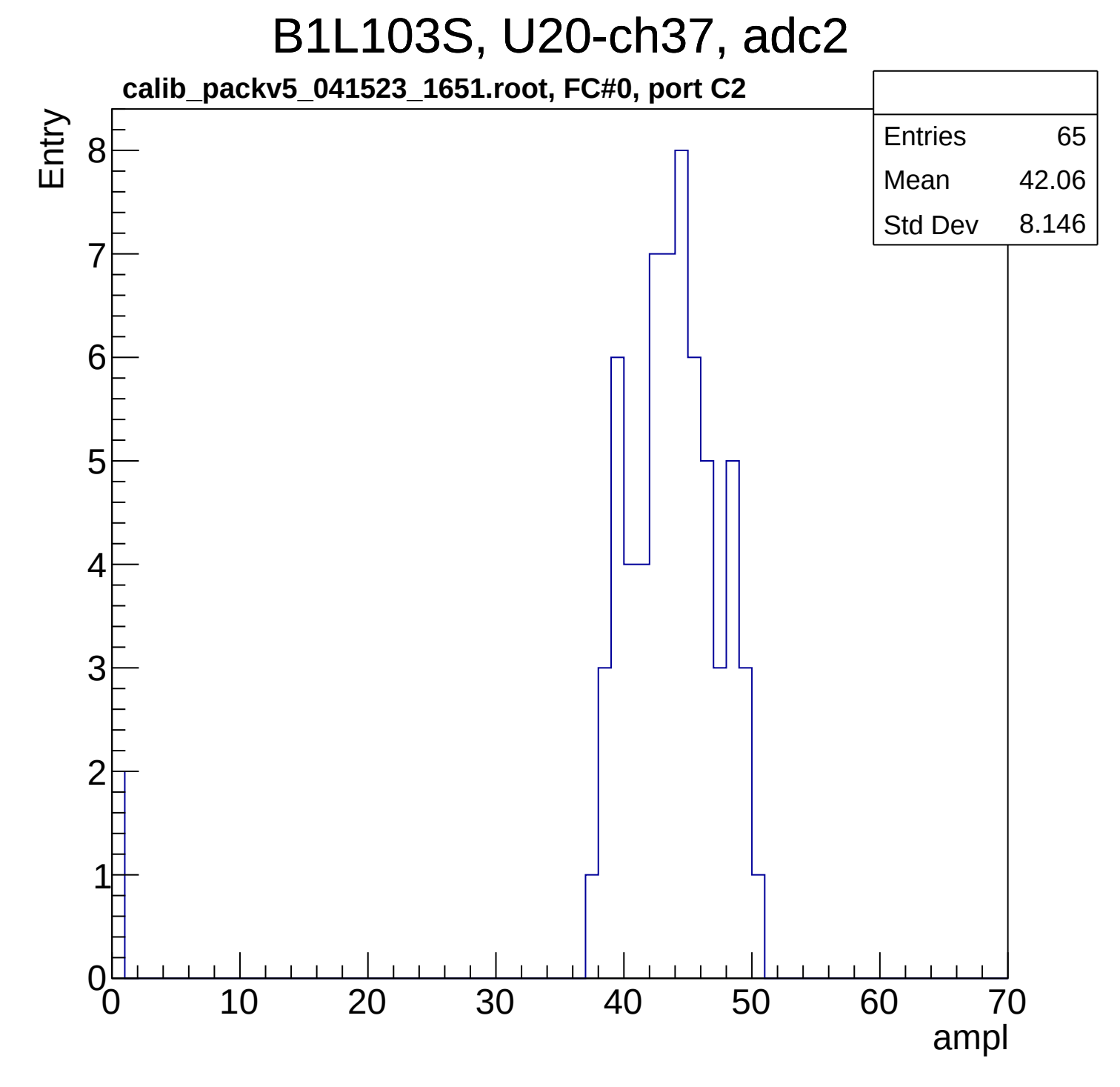
50
60
70
ampl


B1L103S, U20-ch37, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 96
Mean 32.17
Std Dev 12.15
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch37, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 42.06
Std Dev 8.146
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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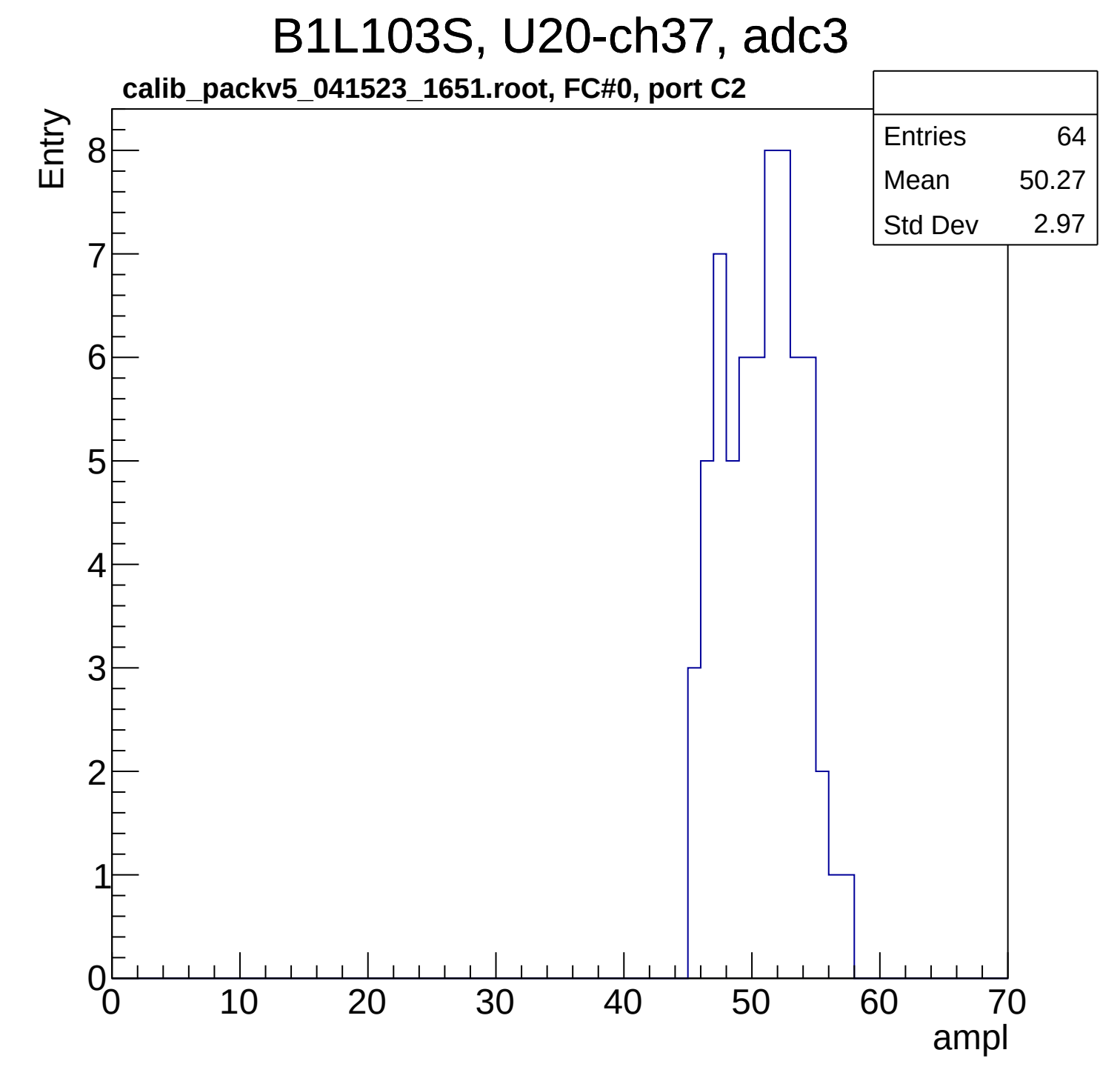
B1L103S, U20-ch37, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 50.27
Std Dev 2.97
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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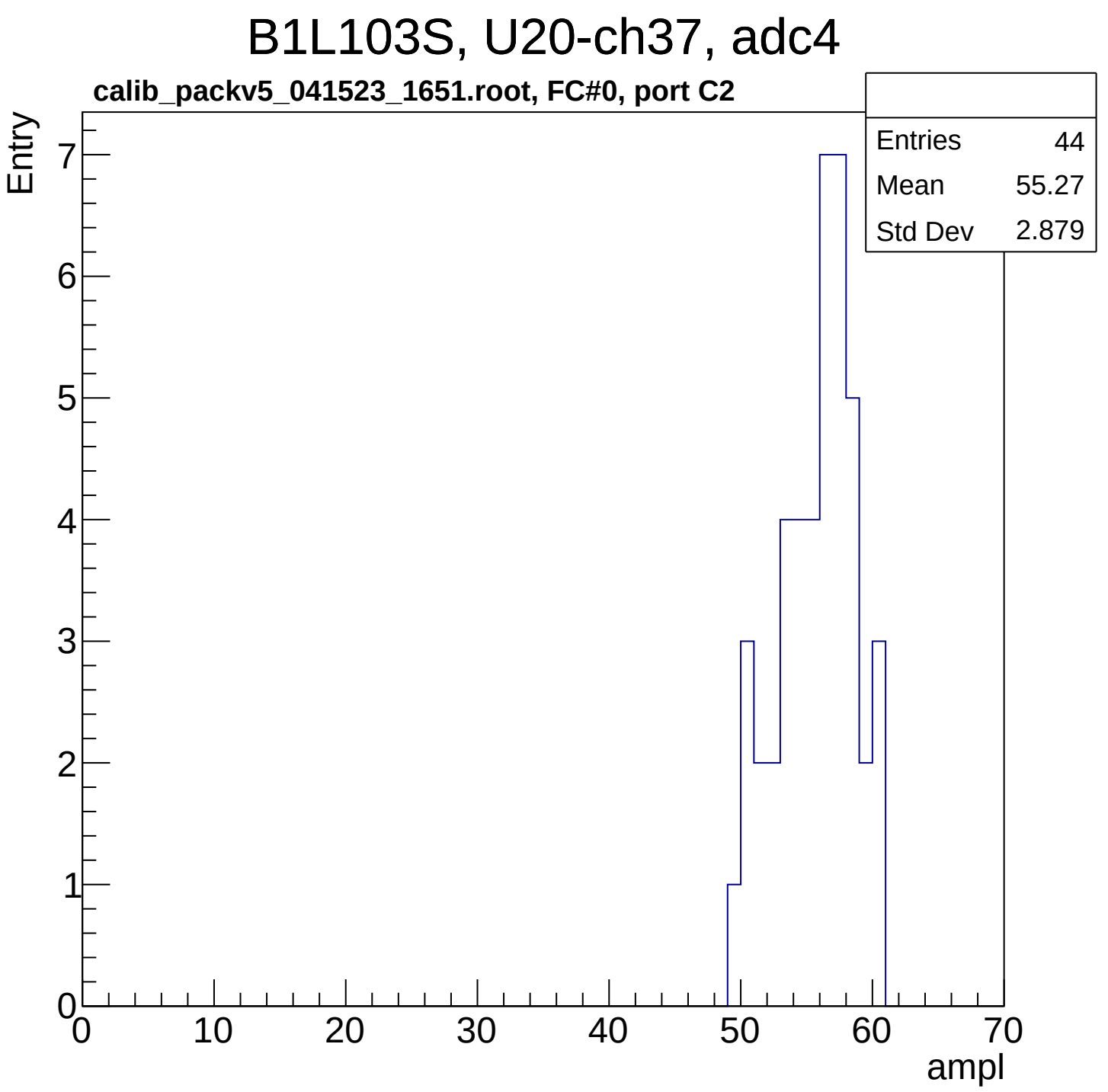
B1L103S, U20-ch37, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 55.27
Std Dev 2.879
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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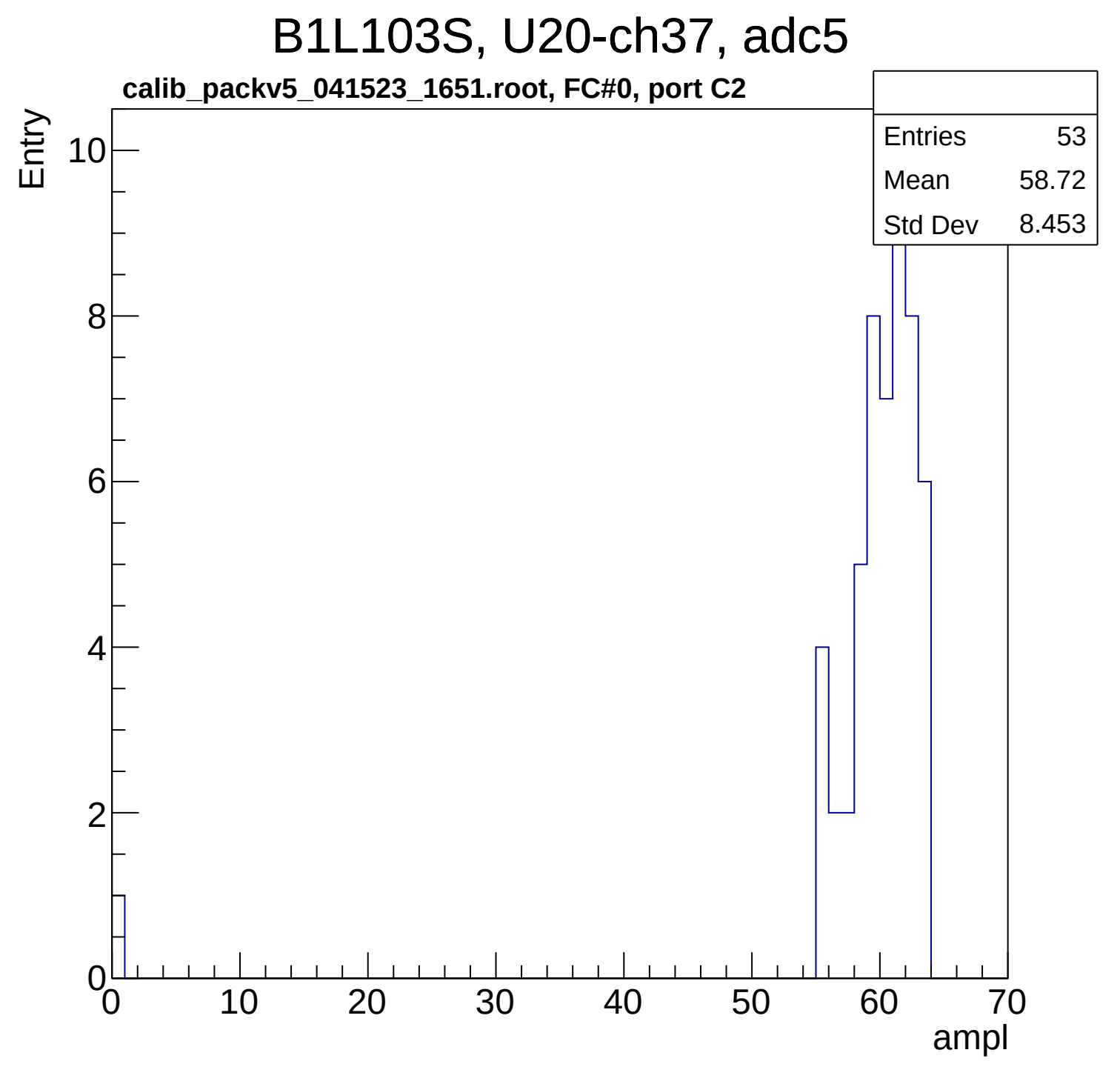
B1L103S, U20-ch37, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 58.72
Std Dev 8.453
Entry
ampl
0
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4
6
8
10
0
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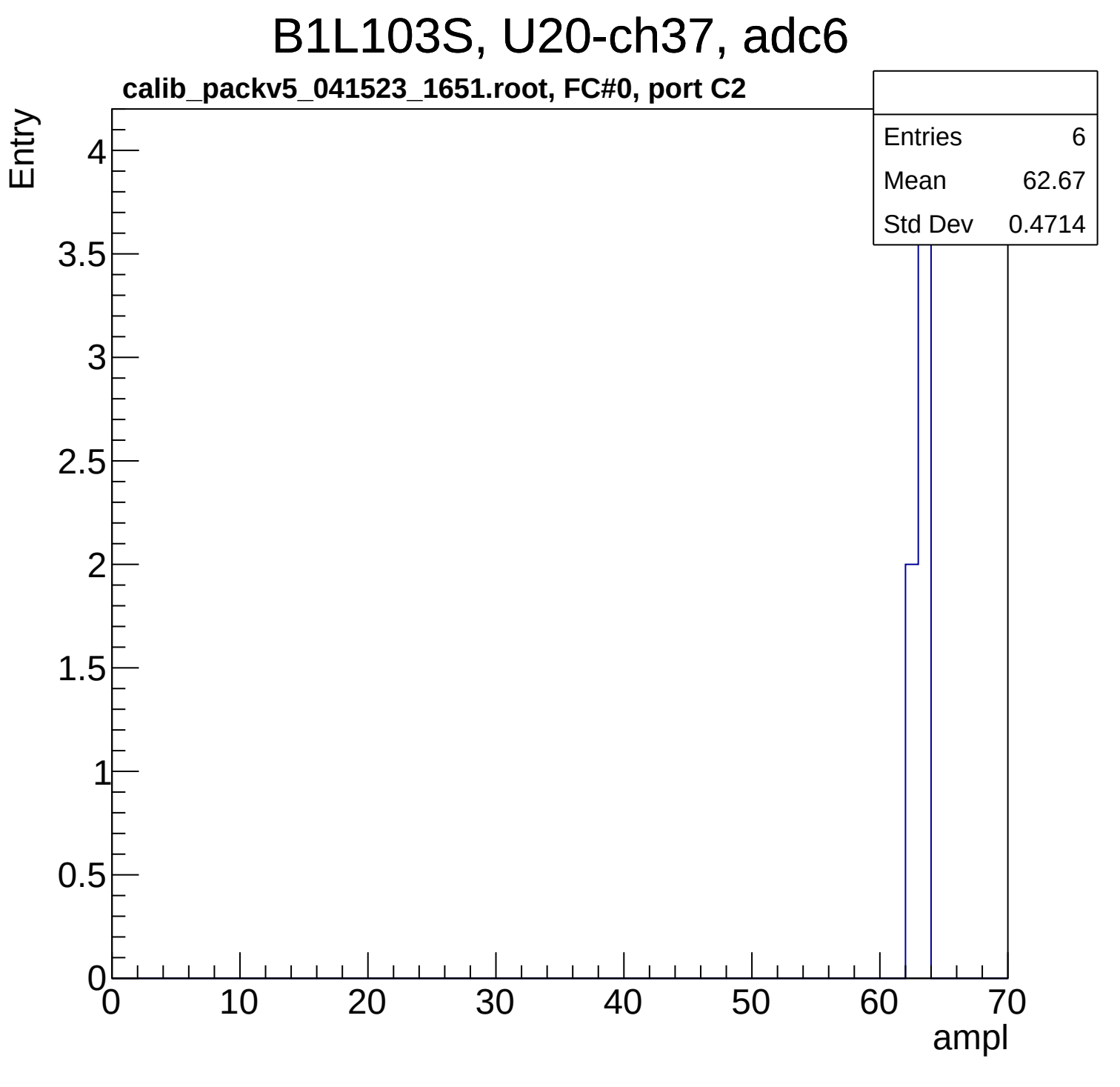
30
40
50
60
70


B1L103S, U20-ch37, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 62.67
Std Dev 0.4714
Entry
ampl
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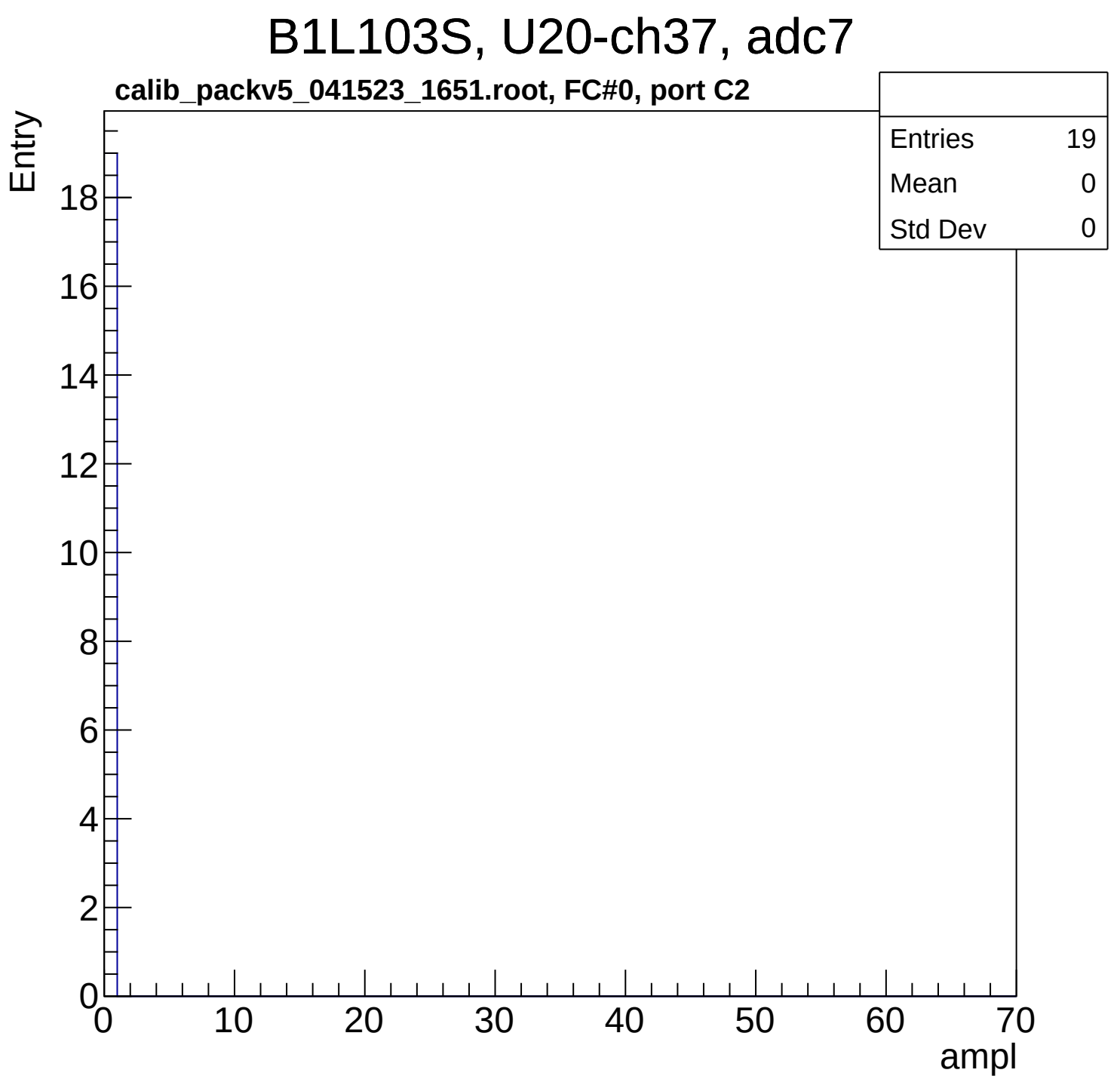
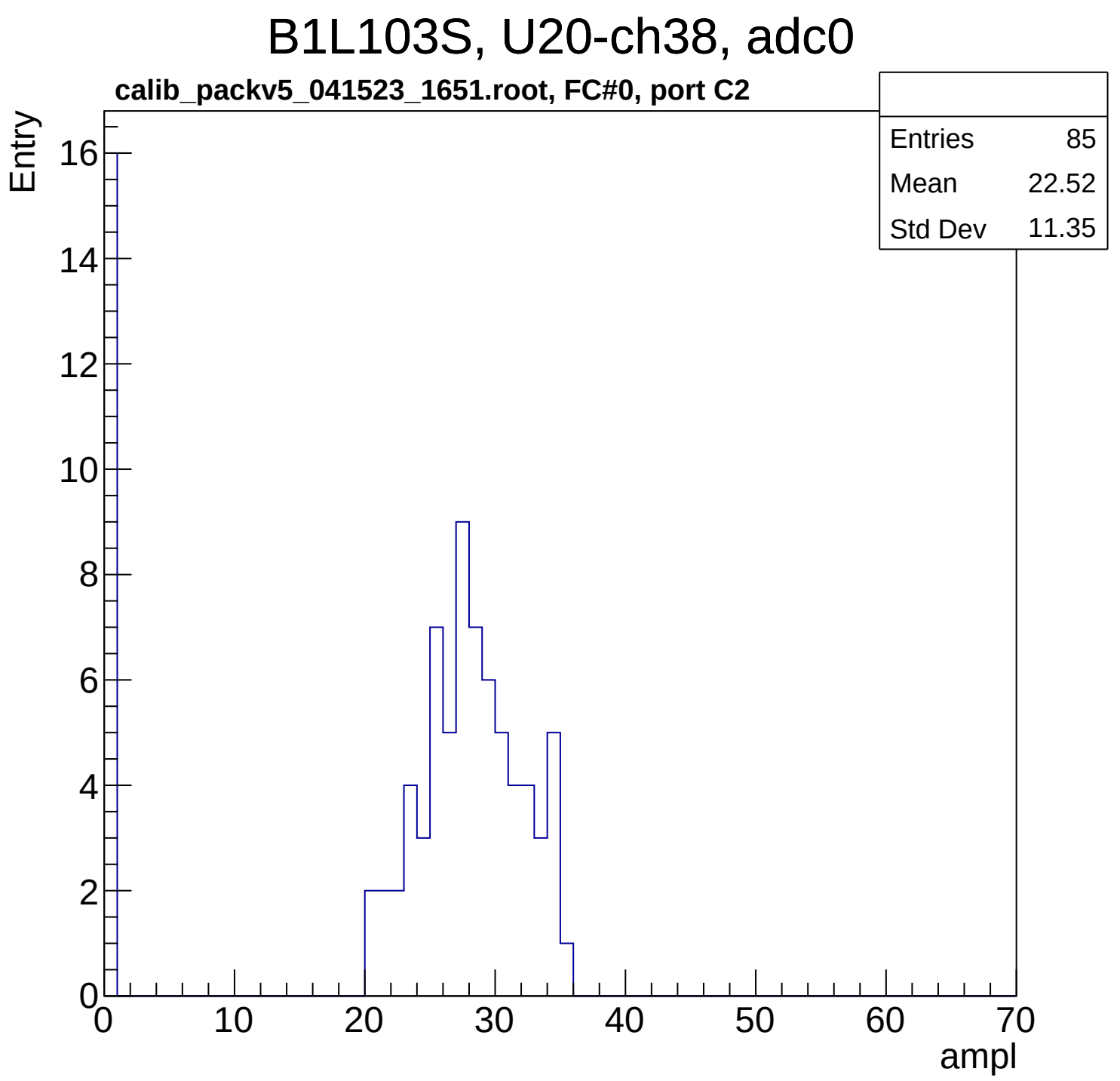
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U20-ch37, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch38, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 22.52
Std Dev 11.35
Entry
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4
6
8
10
12
14
16
0
10
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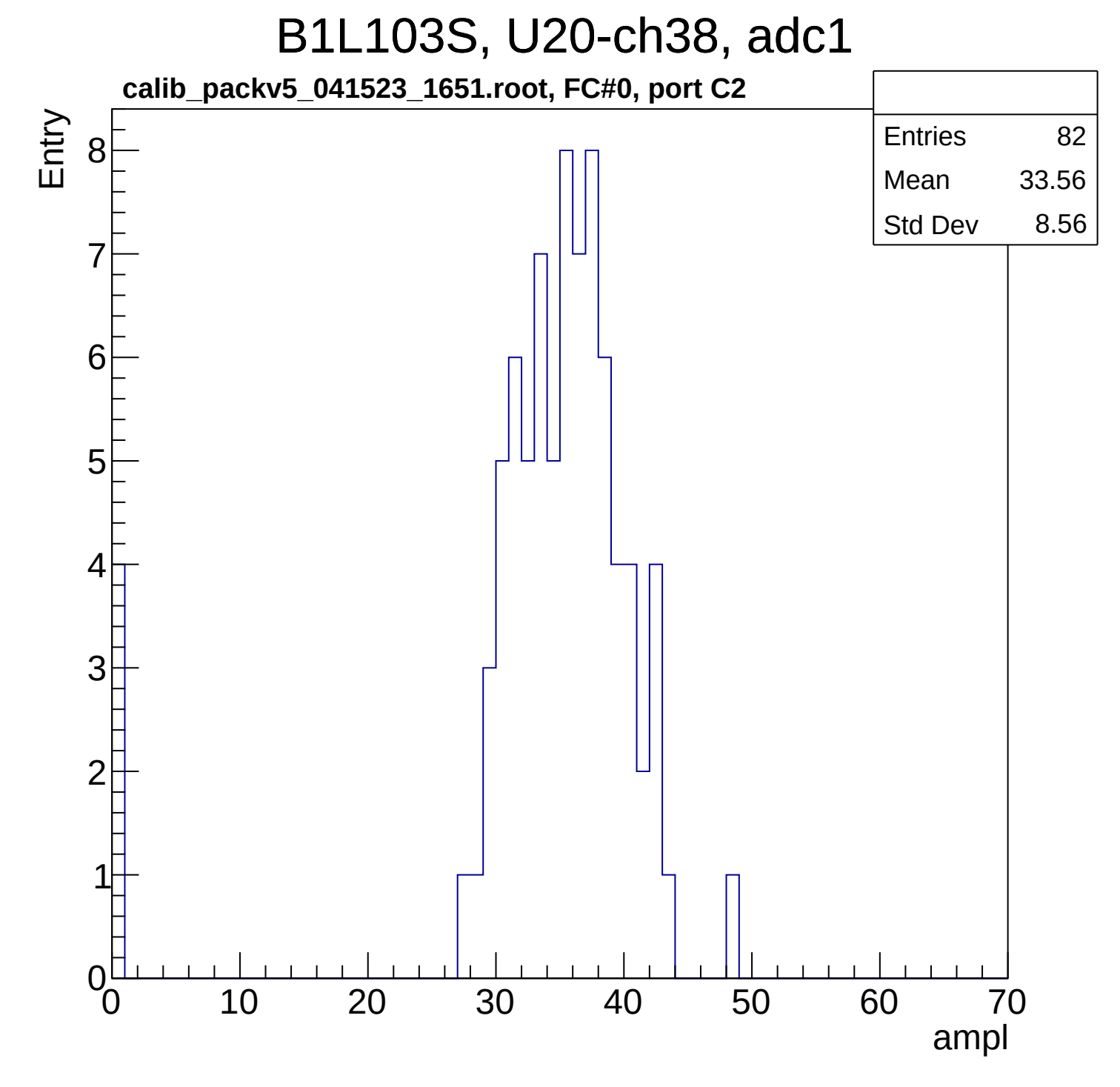
30
40
50
60
70
ampl


B1L103S, U20-ch38, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 33.56
Std Dev 8.56
Entry
ampl
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2
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4
5
6
7
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0
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20
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60
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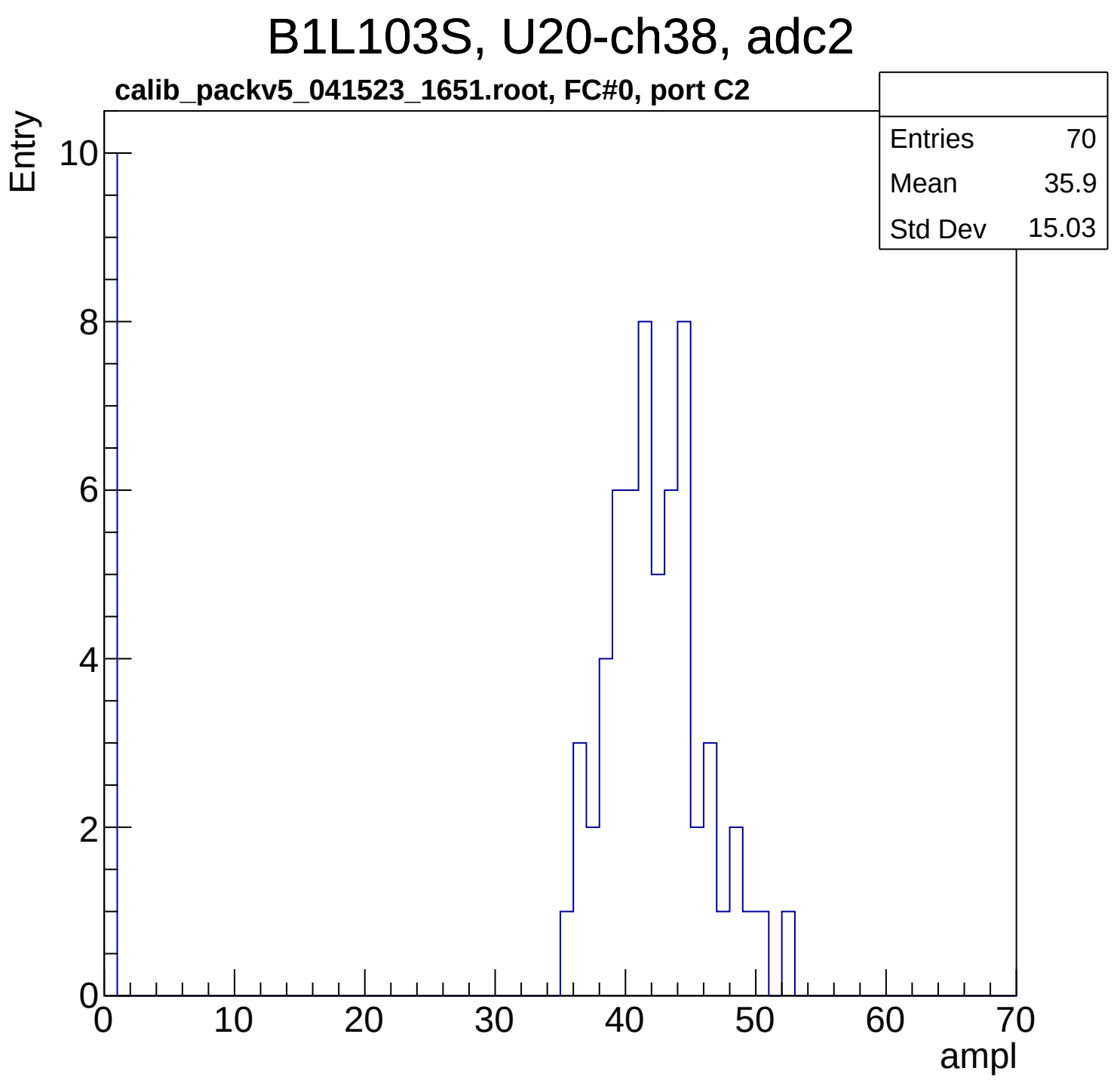
B1L103S, U20-ch38, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 35.9
Std Dev 15.03
Entry
0
2
4
6
8
10
0
10
20
30
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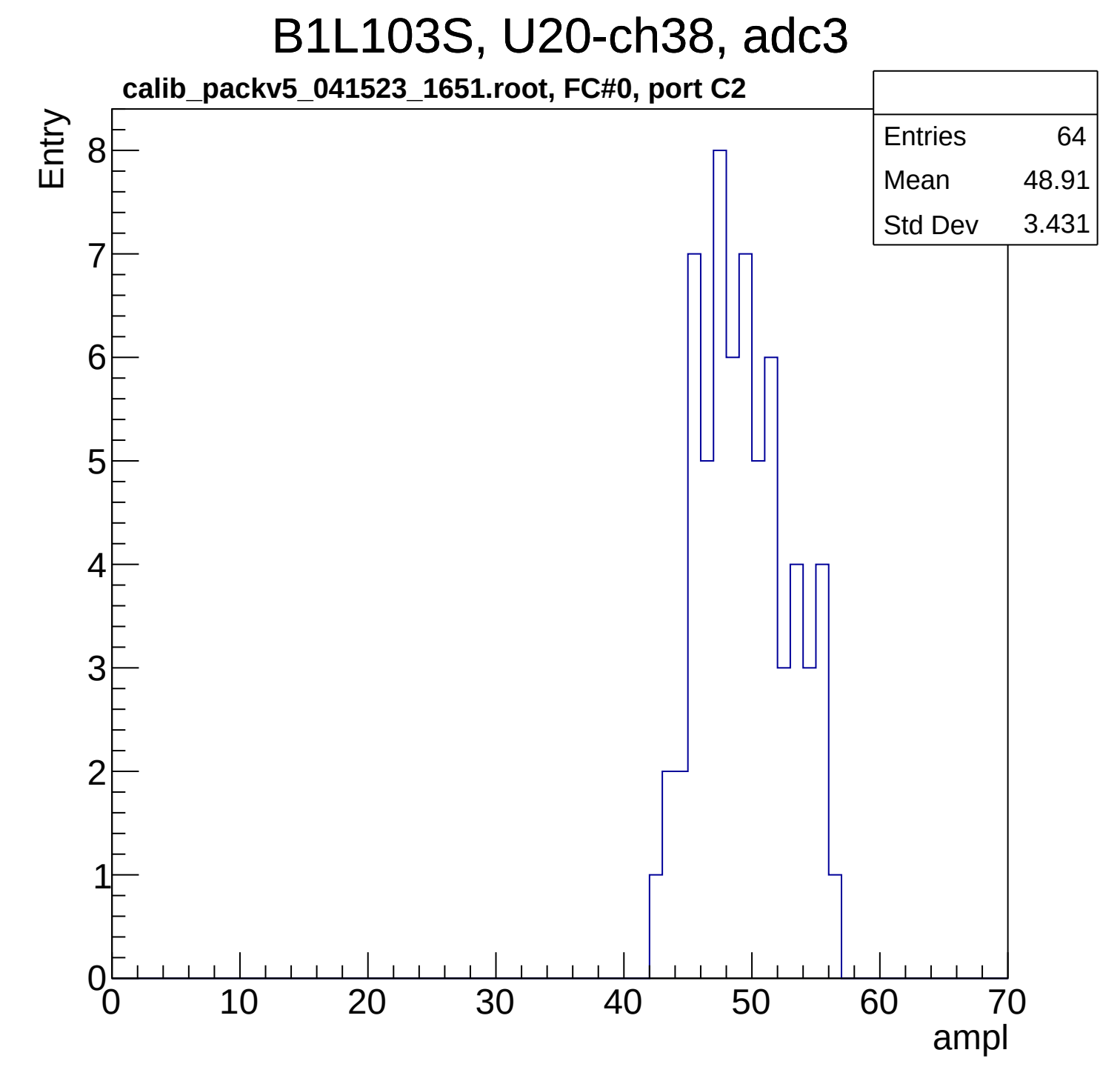
50
60
70
ampl


B1L103S, U20-ch38, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 48.91
Std Dev 3.431
Entry
ampl
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2
3
4
5
6
7
8
0
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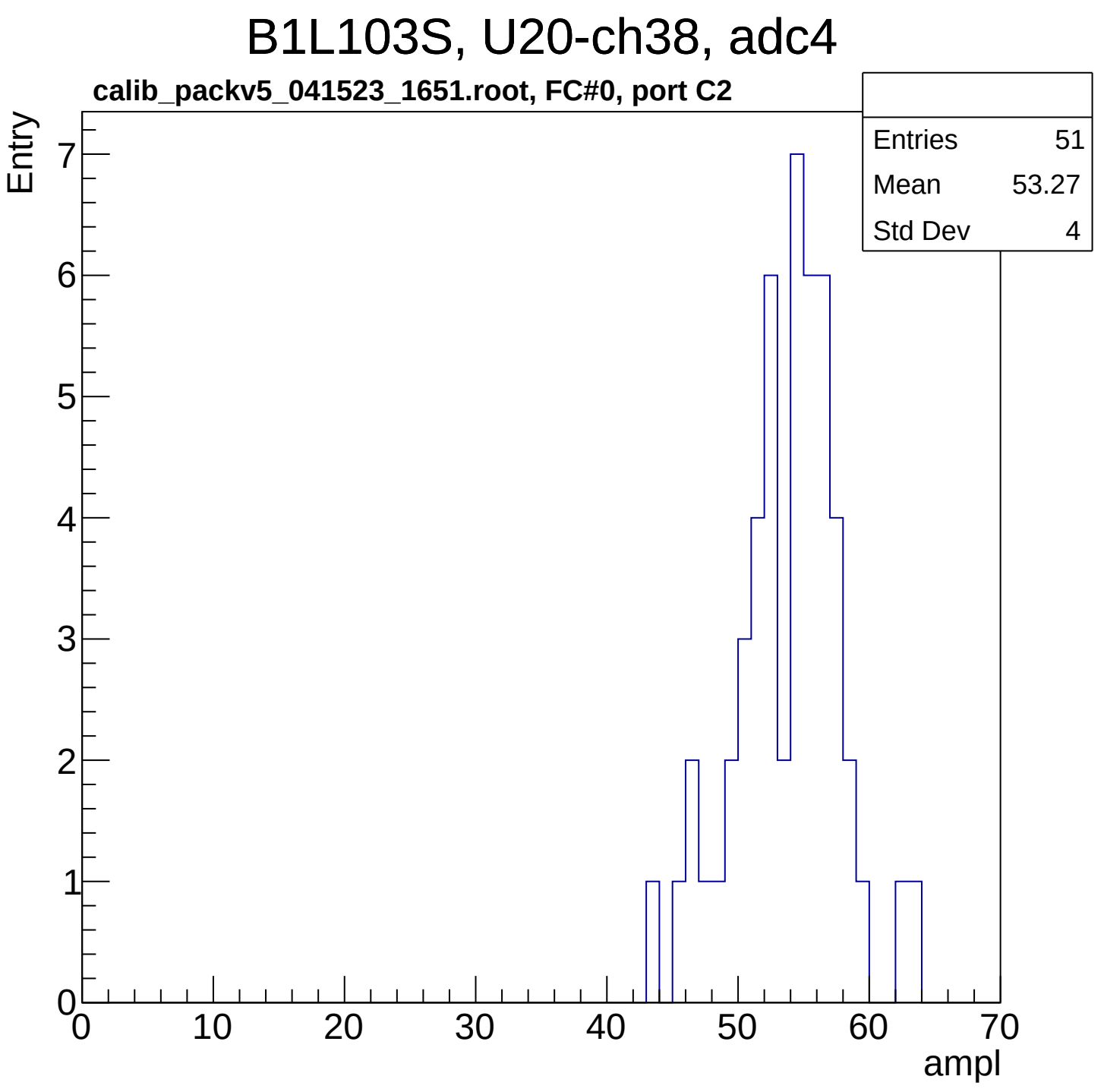
40
50
60
70


B1L103S, U20-ch38, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 53.27
Std Dev 4
Entry
ampl
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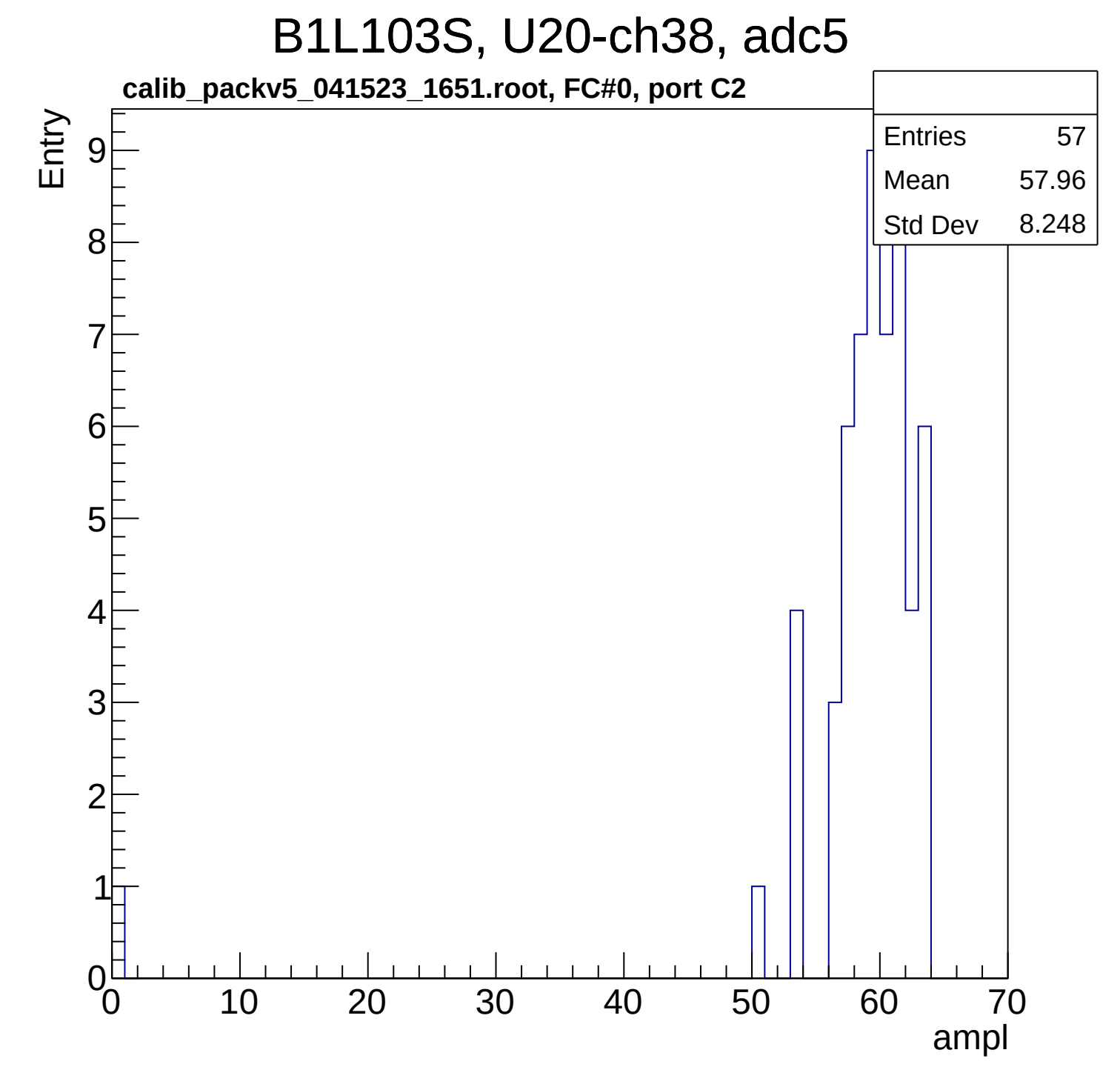
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U20-ch38, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 57.96
Std Dev 8.248
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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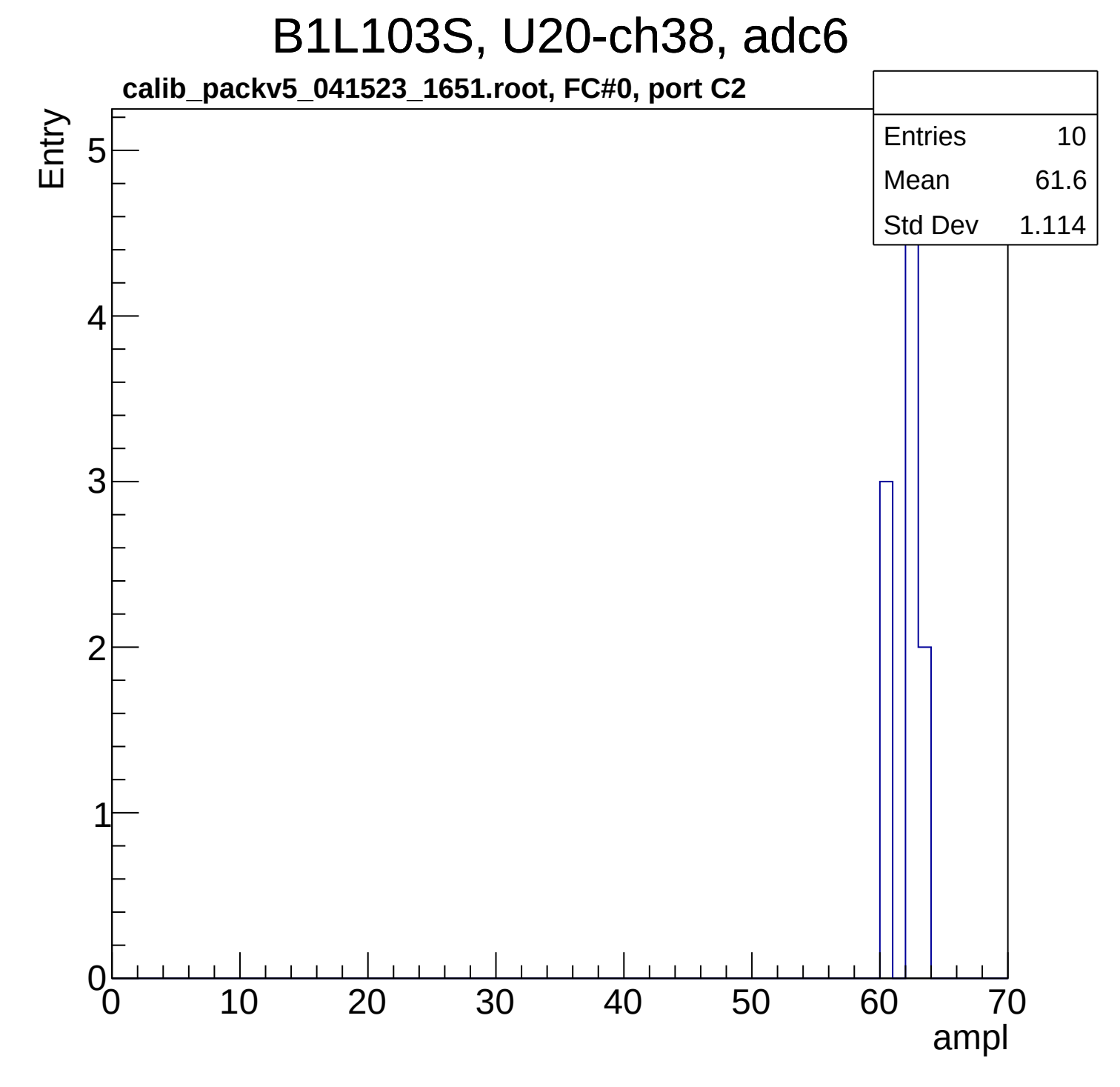
40
50
60
70


B1L103S, U20-ch38, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61.6
Std Dev 1.114
Entry
ampl
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1
2
3
4
5
0
10
20
30
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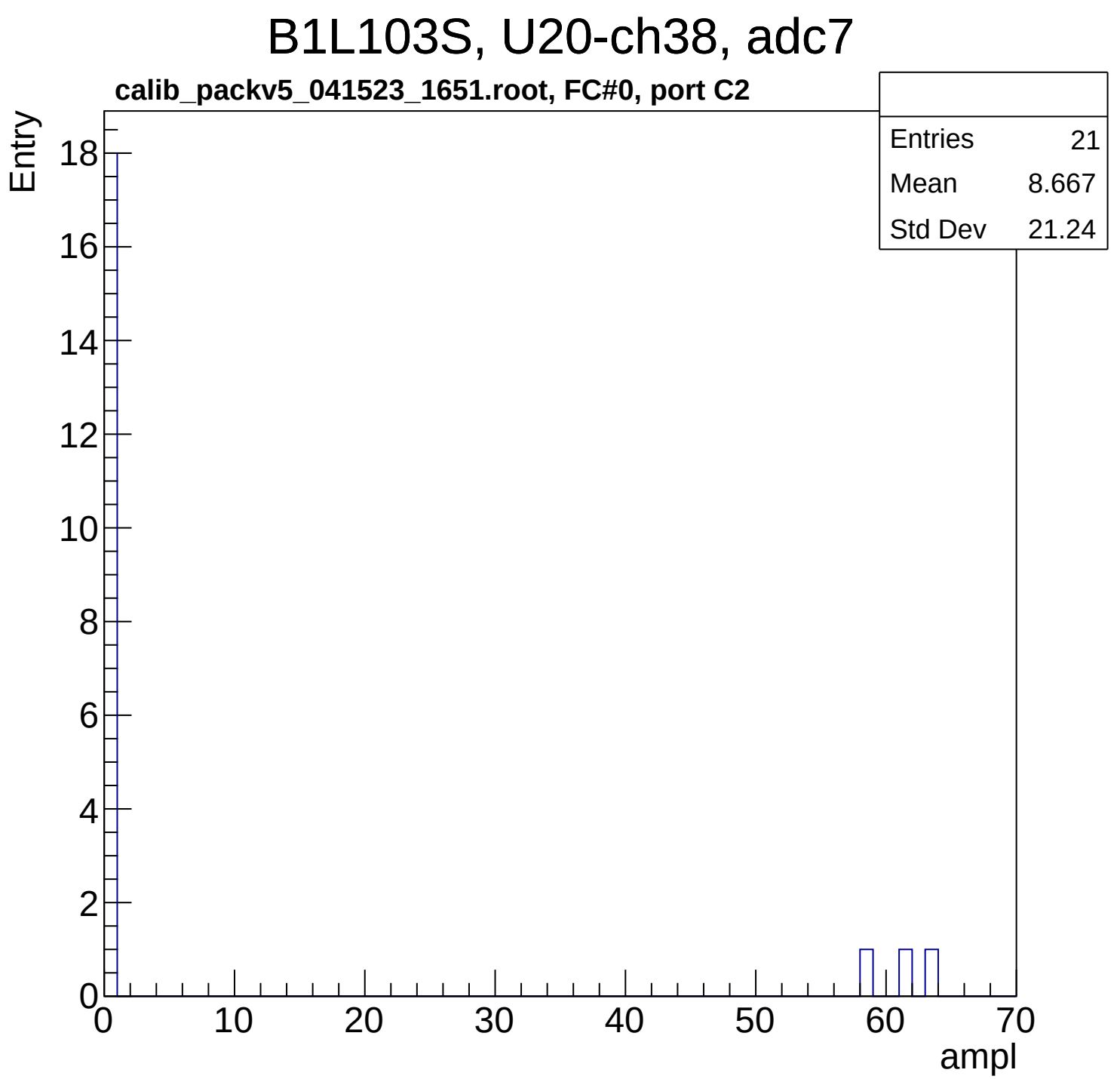
50
60
70


B1L103S, U20-ch38, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 8.667
Std Dev 21.24
Entry
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6
8
10
12
14
16
18
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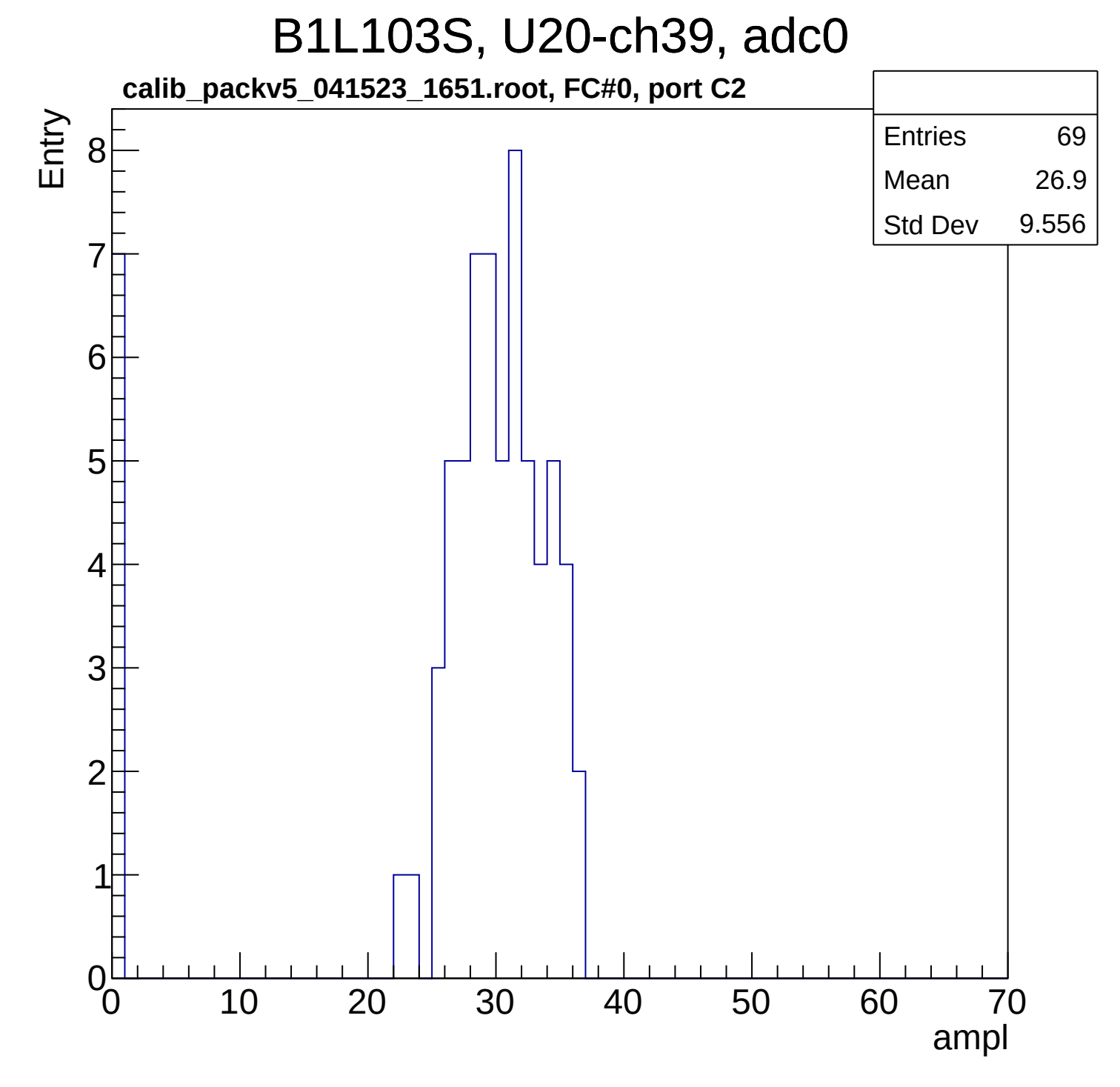
70
ampl


B1L103S, U20-ch39, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 26.9
Std Dev 9.556
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
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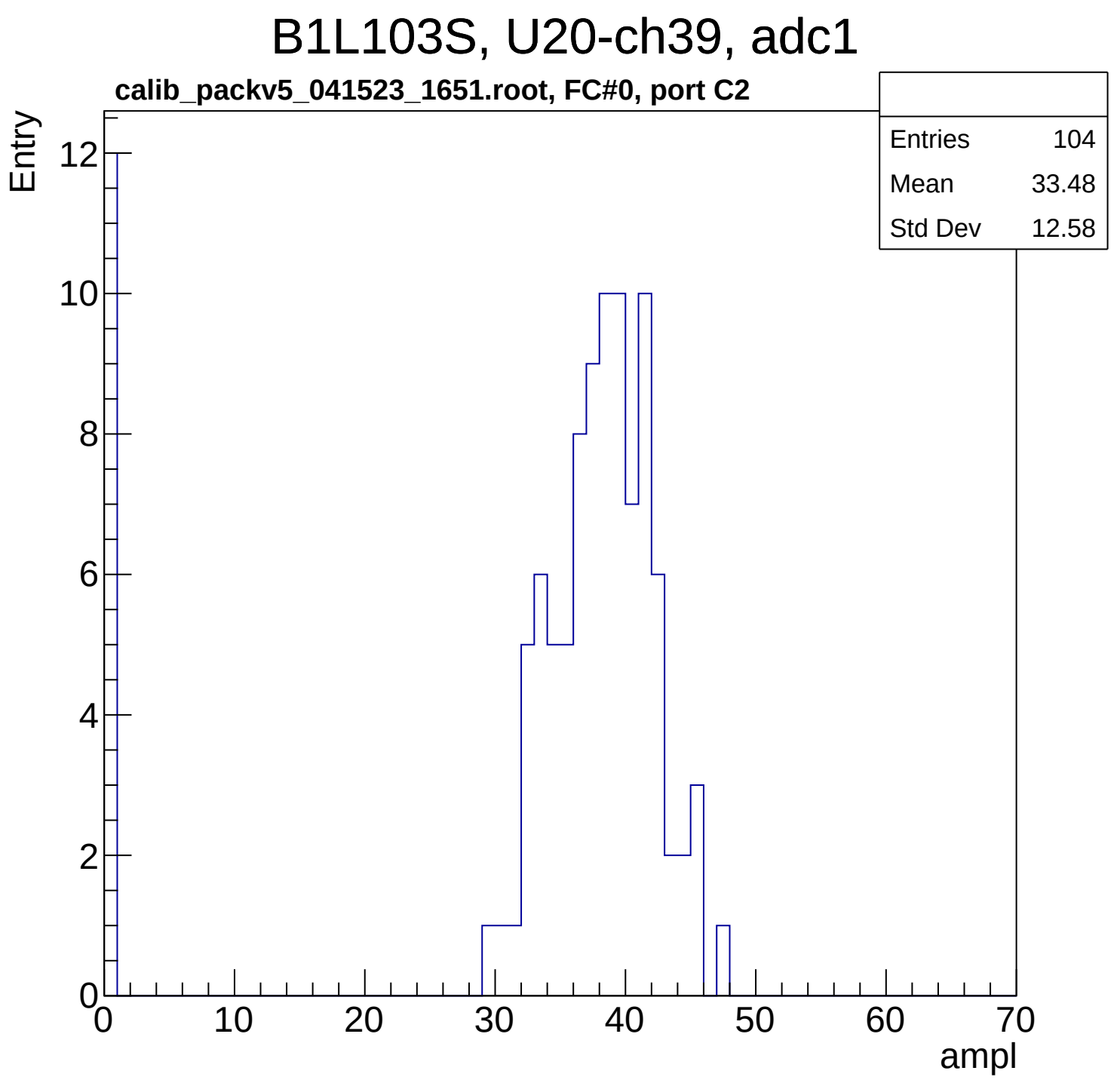
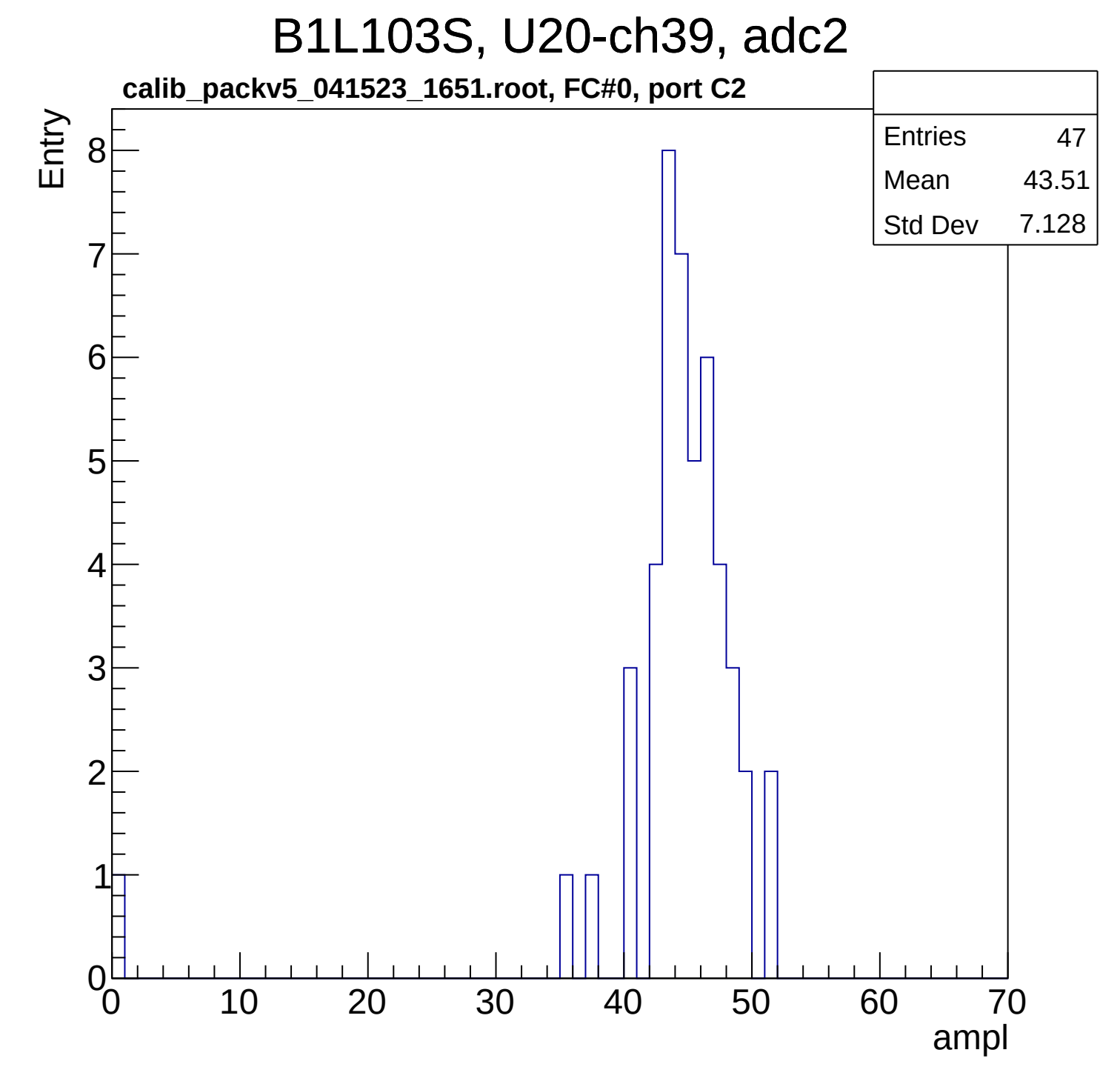
50
60
70


B1L103S, U20-ch39, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 104
Mean 33.48
Std Dev 12.58
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch39, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 43.51
Std Dev 7.128
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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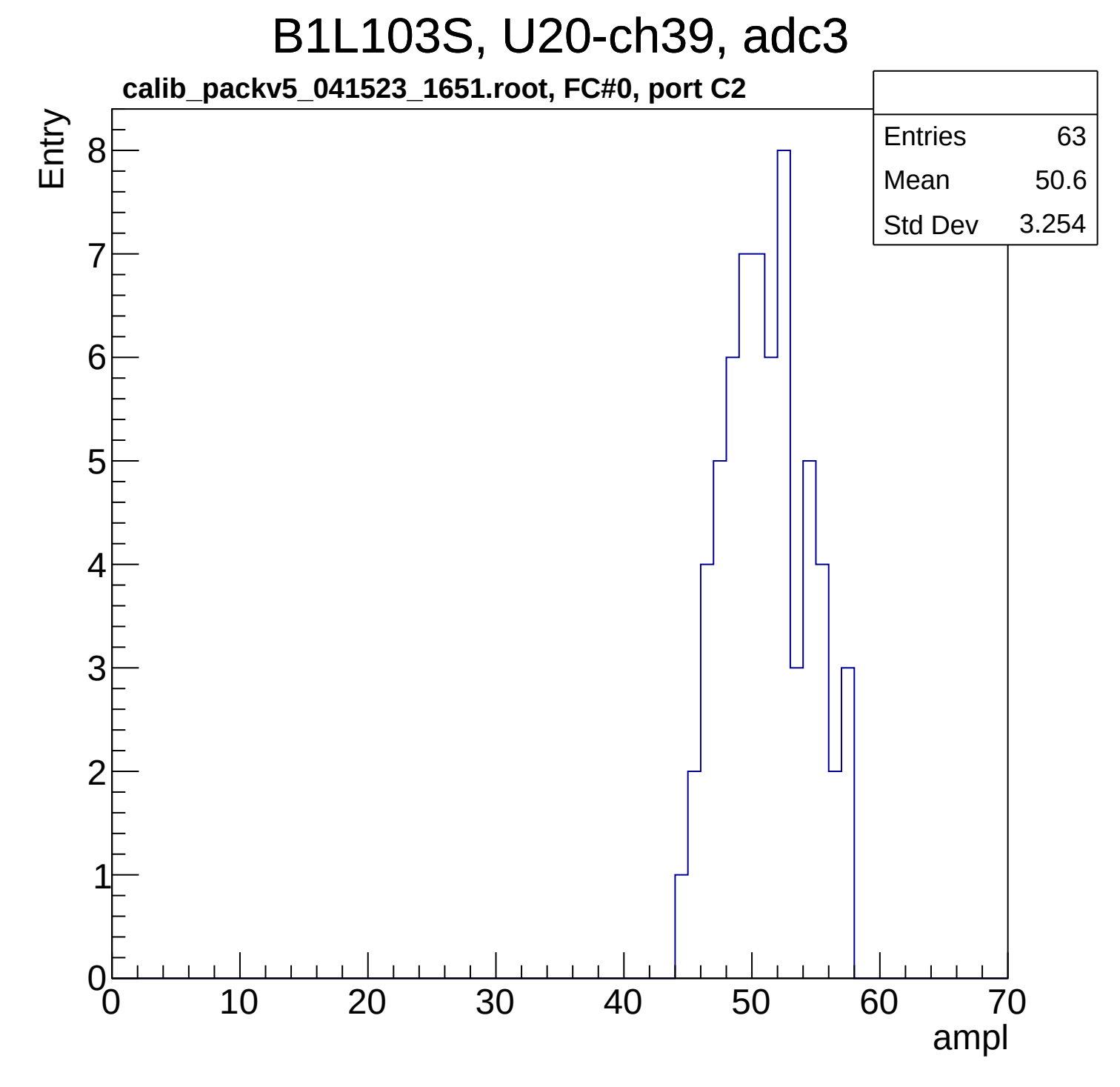
B1L103S, U20-ch39, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 50.6
Std Dev 3.254
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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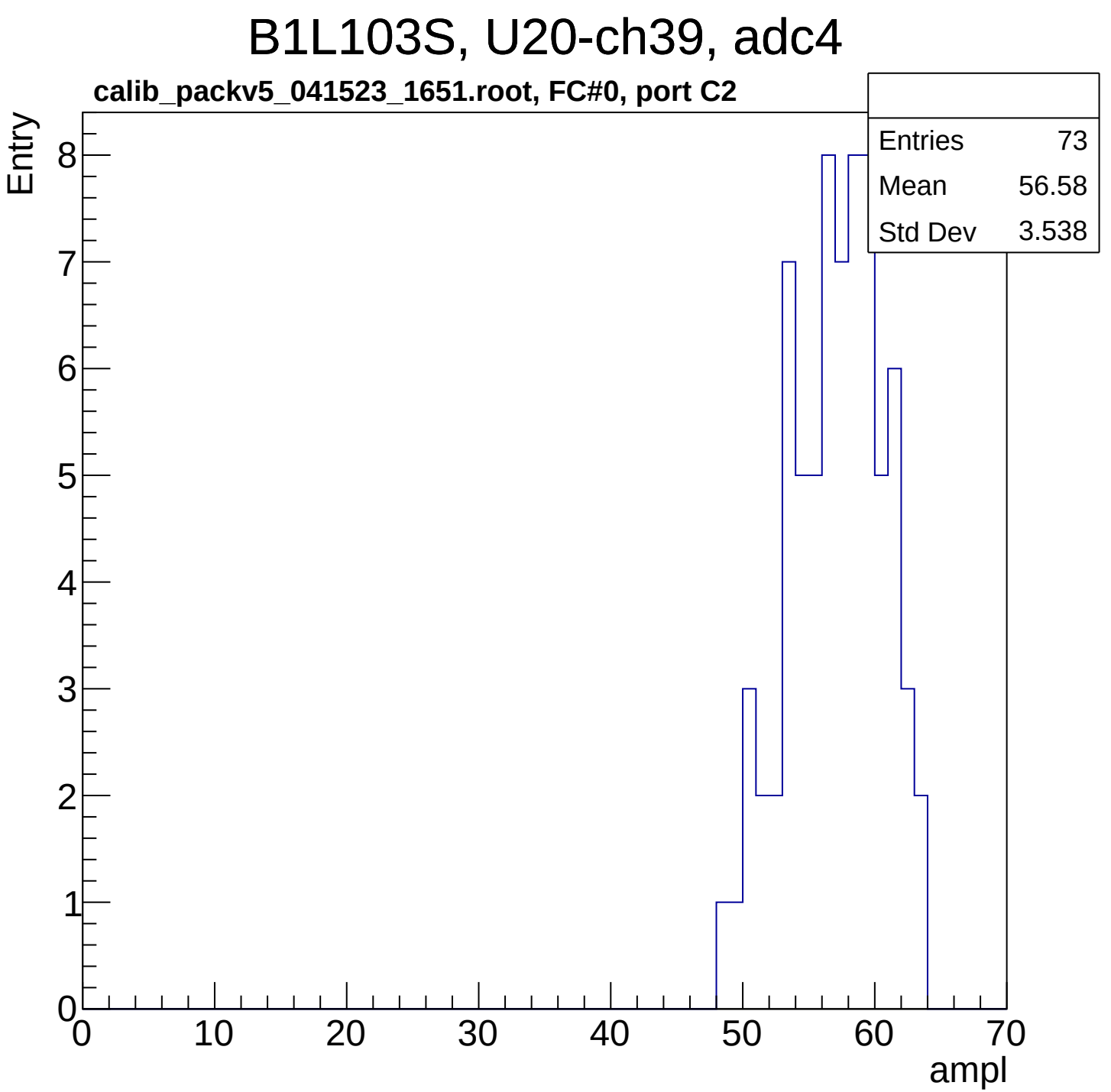
40
50
60
70


B1L103S, U20-ch39, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 56.58
Std Dev 3.538
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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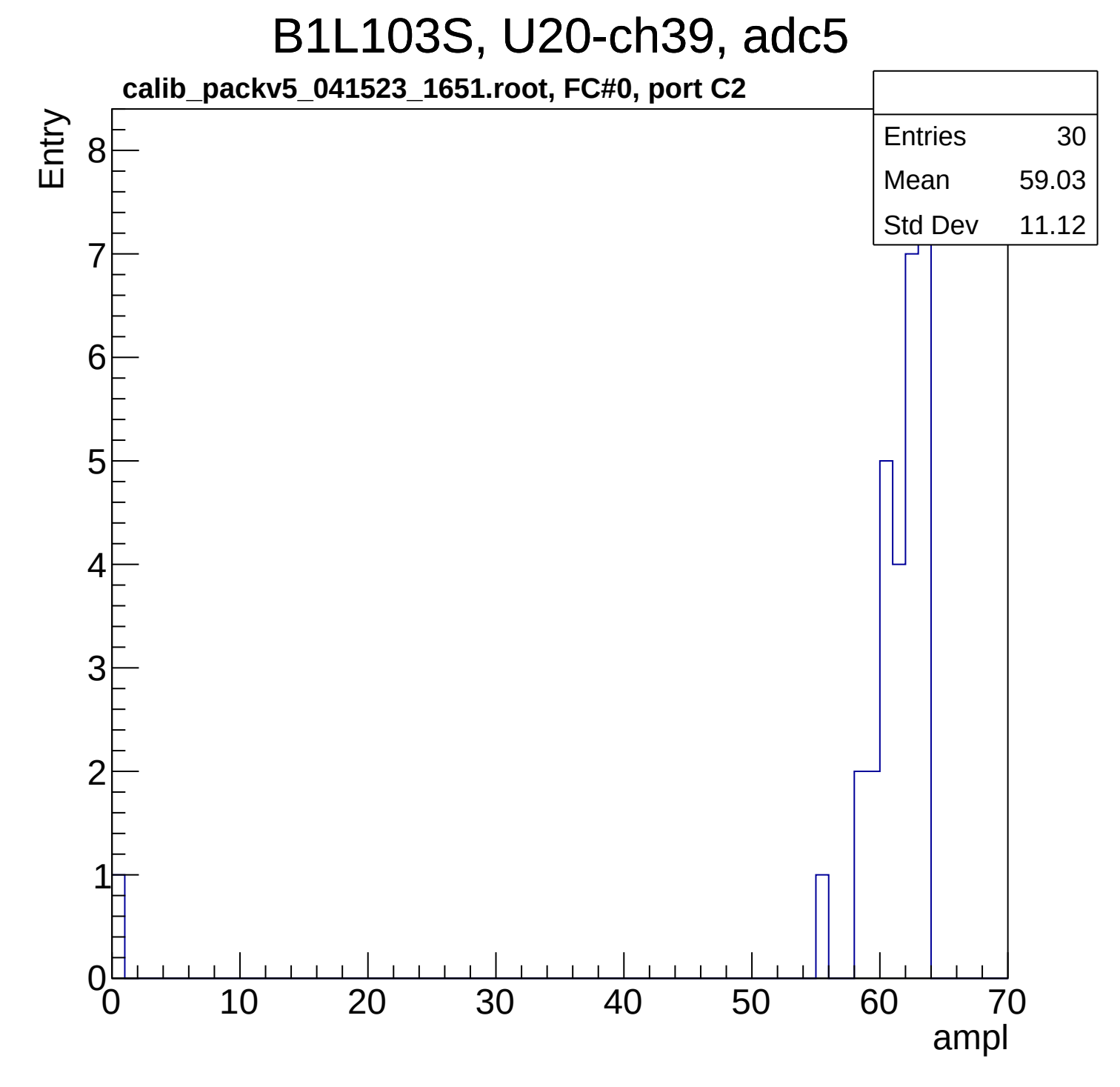
50
60
70


B1L103S, U20-ch39, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 59.03
Std Dev 11.12
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
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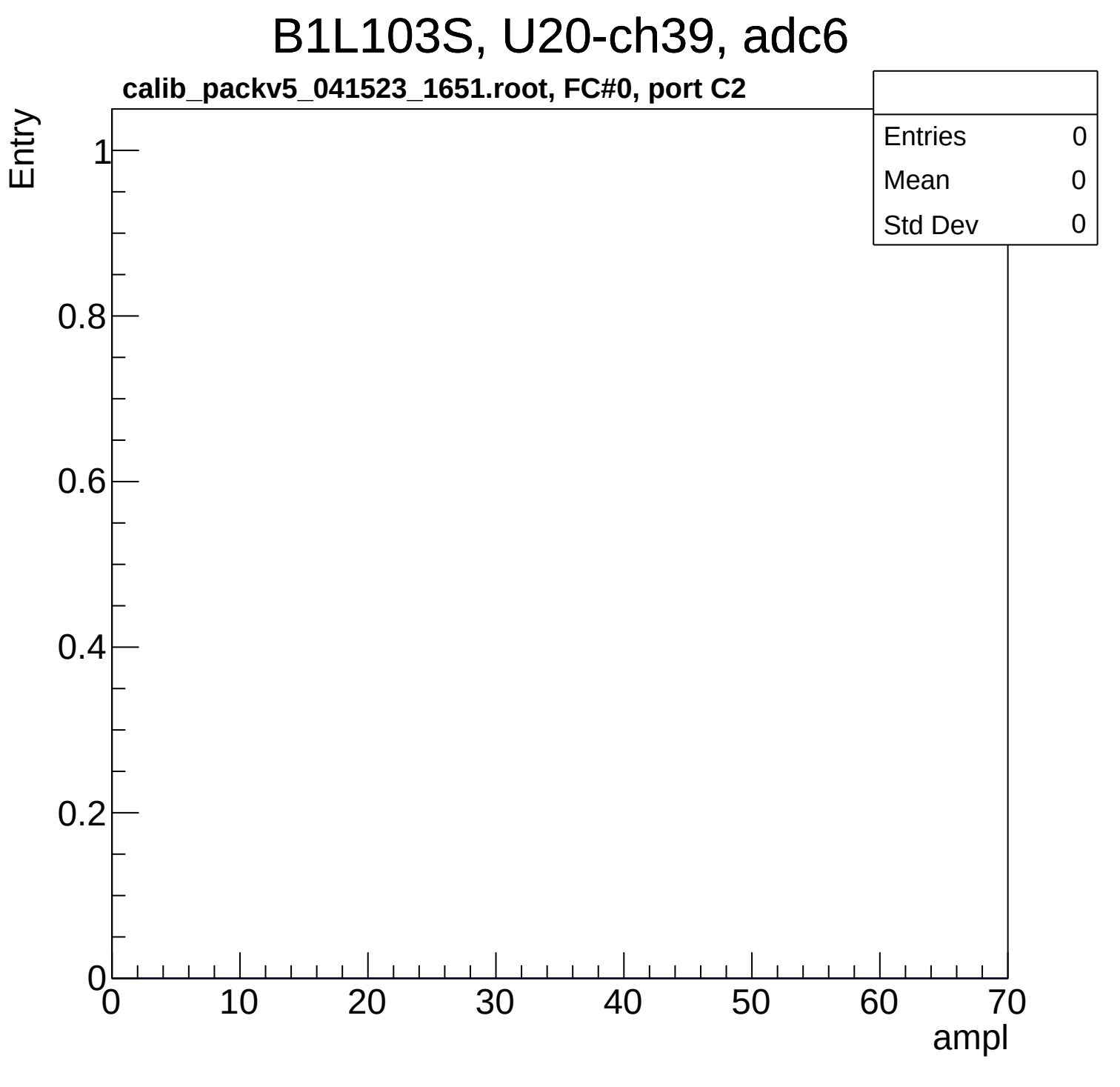
50
60
70


B1L103S, U20-ch39, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
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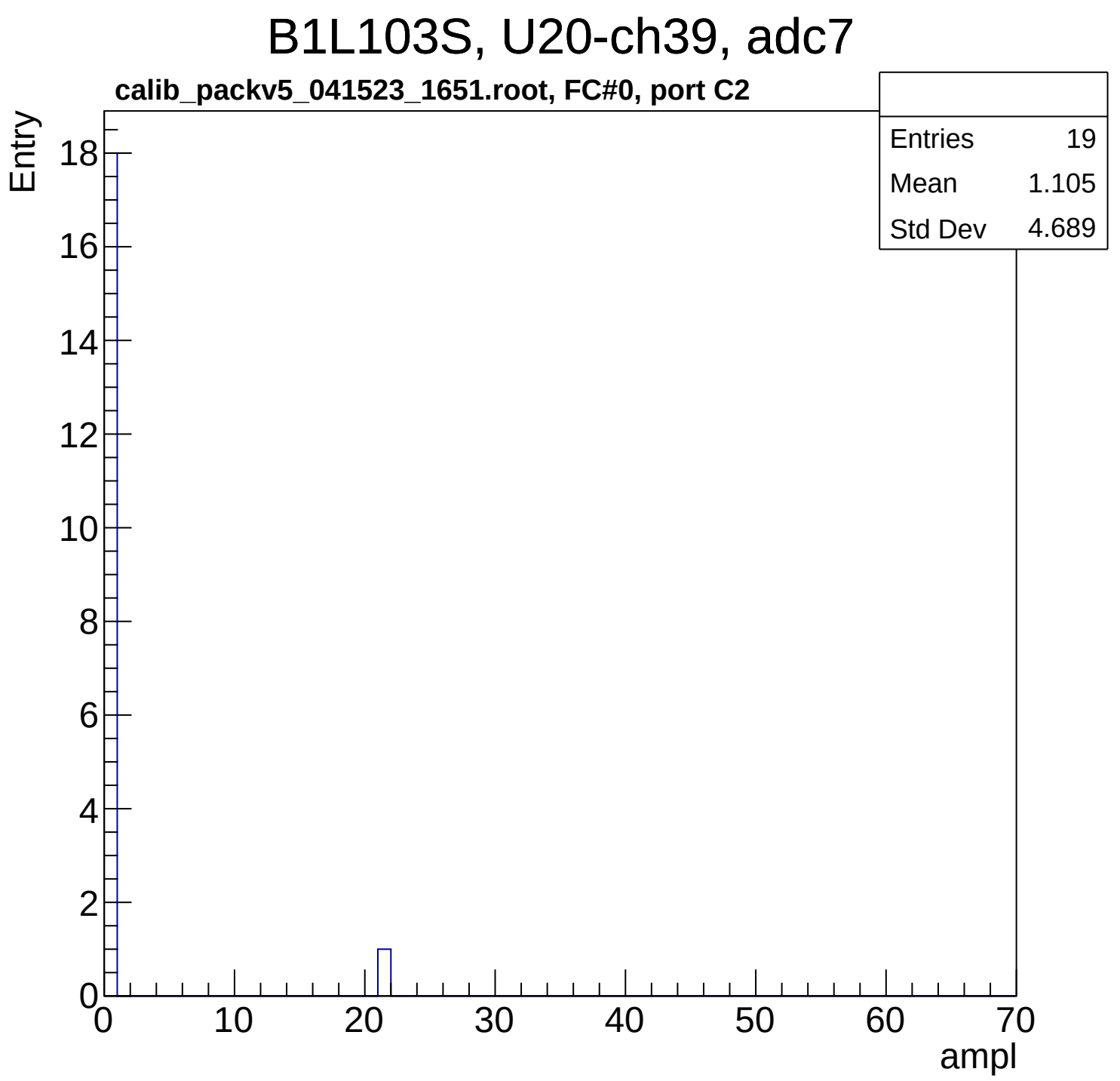
50
60
70
ampl


B1L103S, U20-ch39, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.105
Std Dev 4.689
Entry
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6
8
10
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14
16
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10
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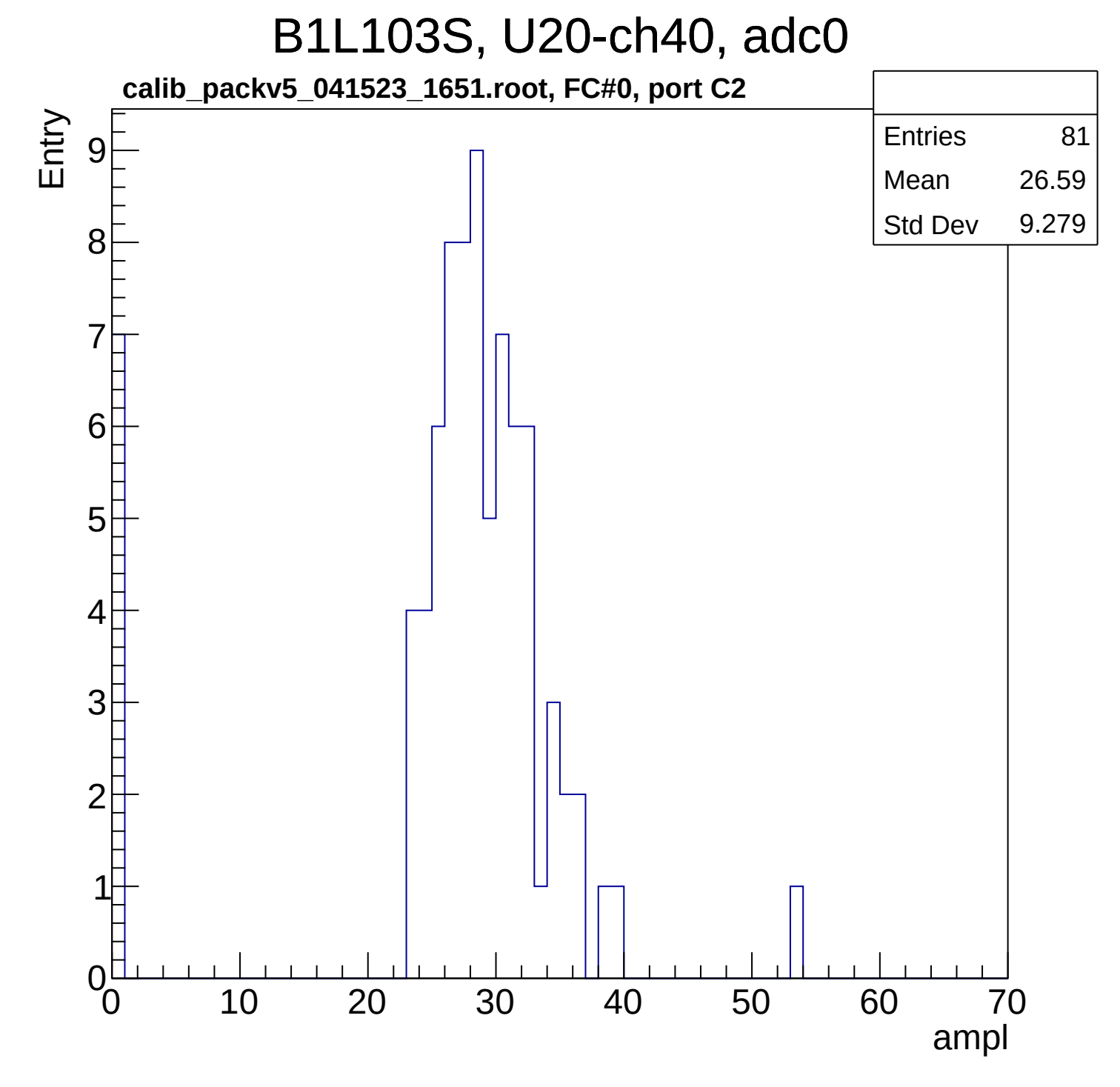
50
60
70
ampl


B1L103S, U20-ch40, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 26.59
Std Dev 9.279
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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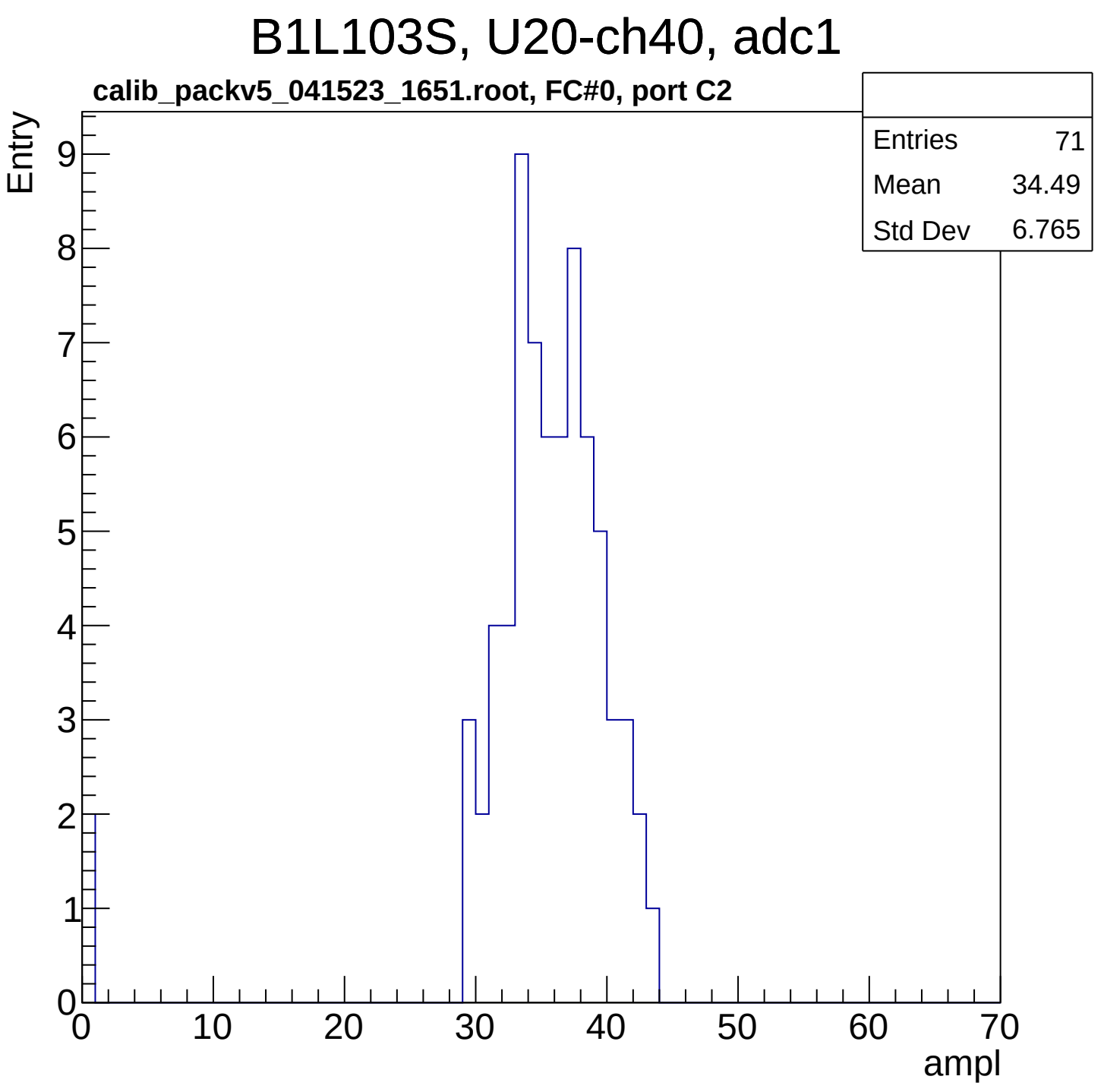
B1L103S, U20-ch40, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 34.49
Std Dev 6.765
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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50
60
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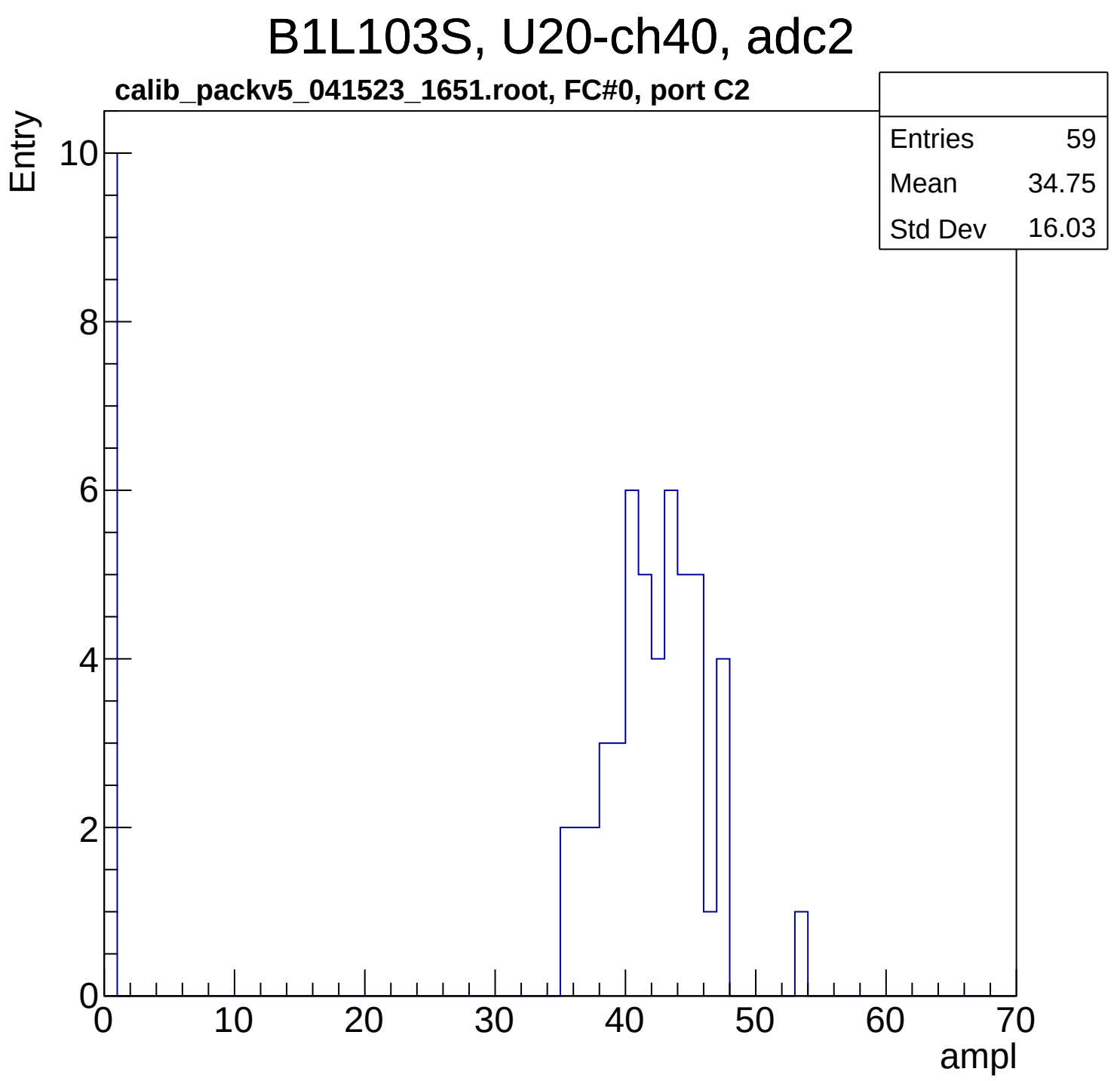
B1L103S, U20-ch40, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 34.75
Std Dev 16.03
Entry
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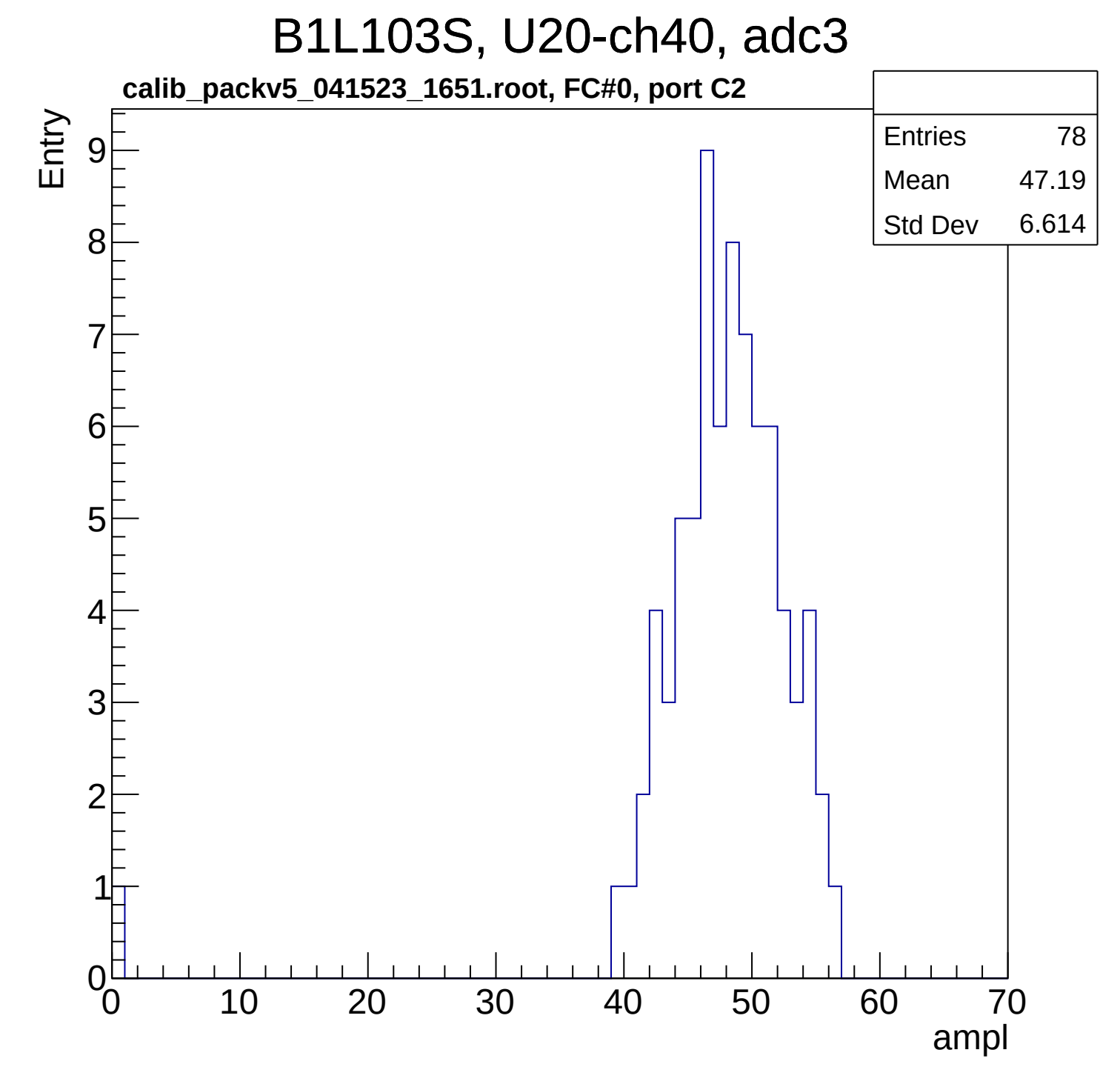
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch40, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 47.19
Std Dev 6.614
Entry
ampl
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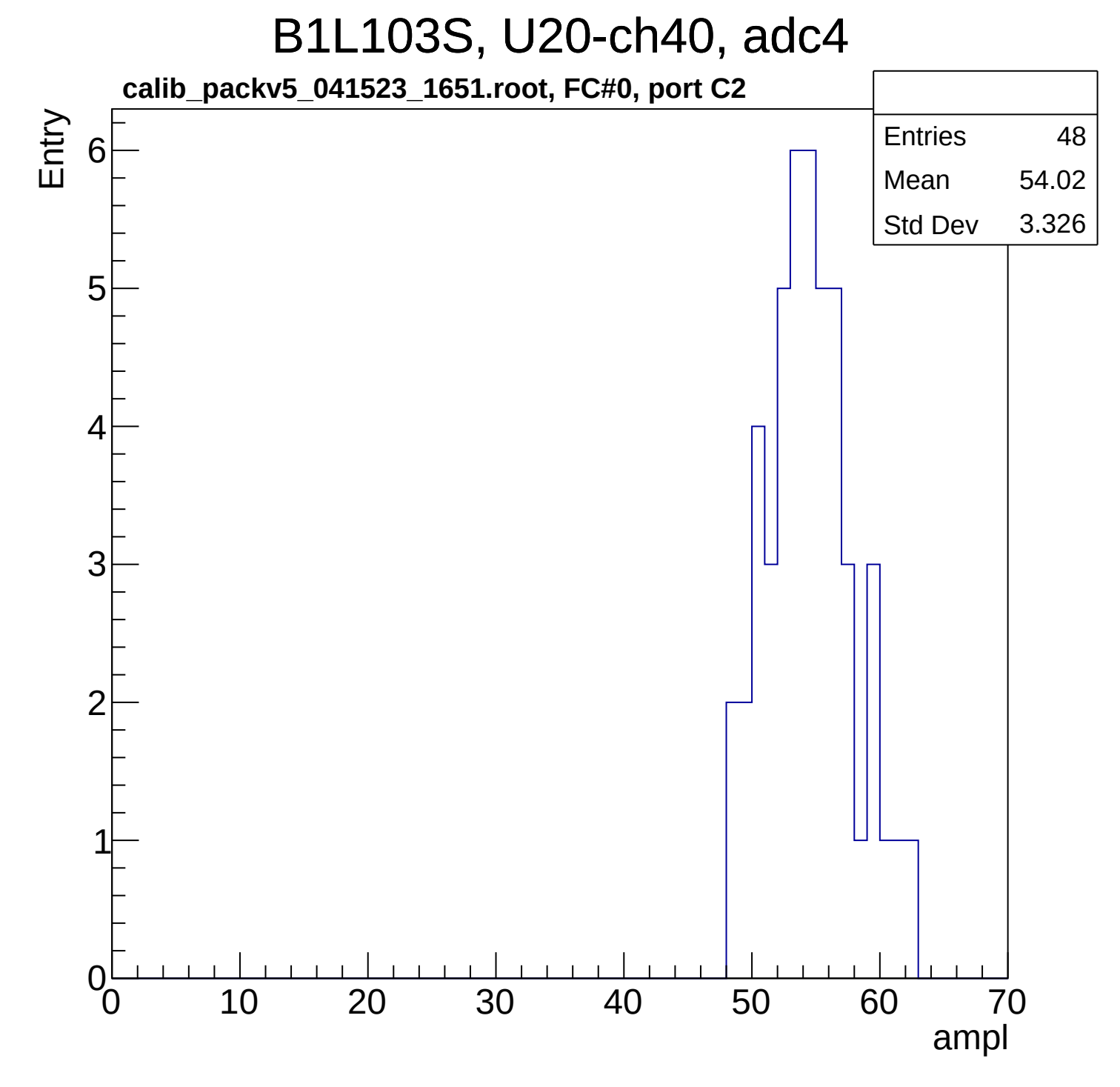
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch40, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 54.02
Std Dev 3.326
Entry
ampl
0
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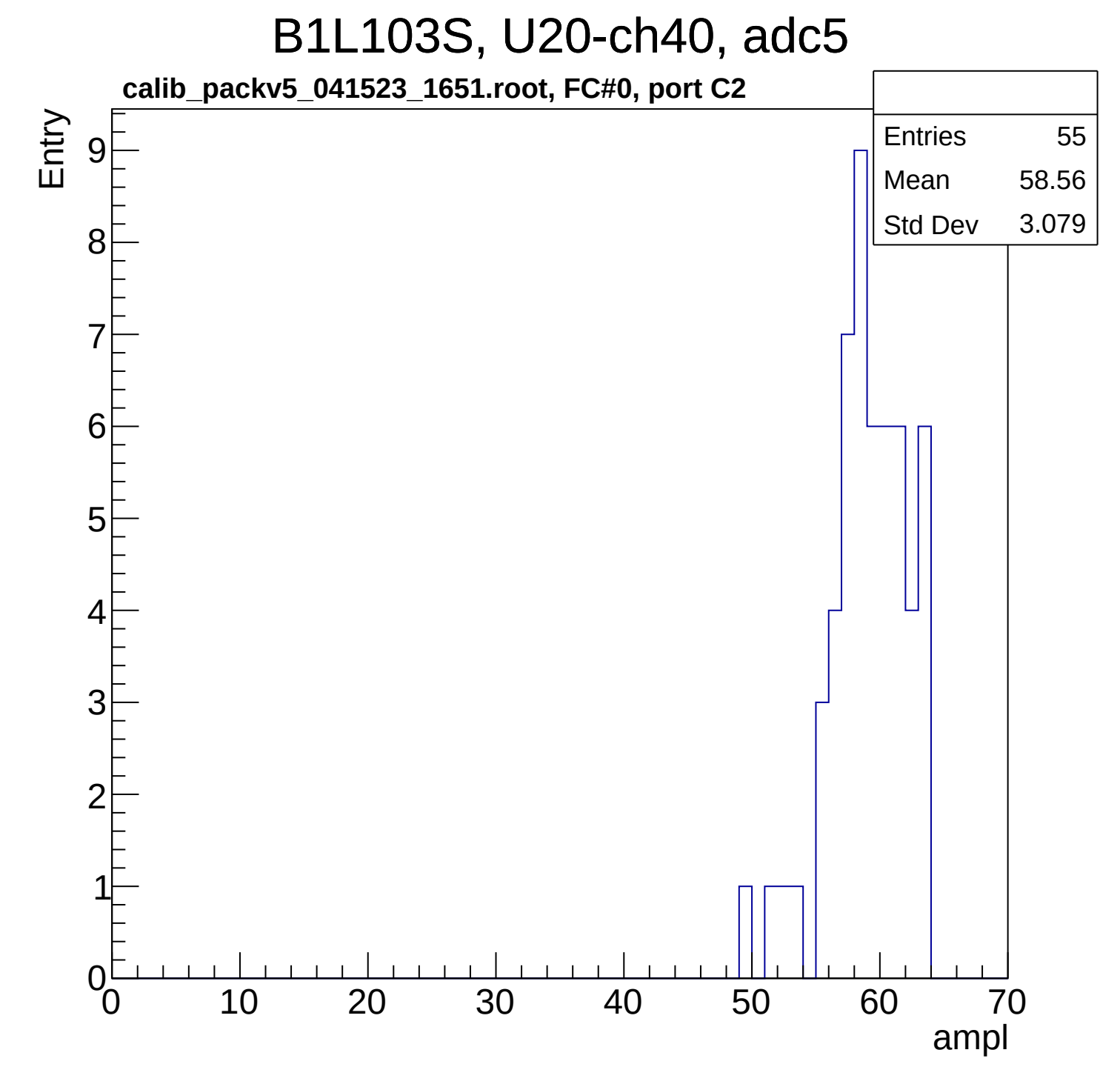
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U20-ch40, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 58.56
Std Dev 3.079
Entry
ampl
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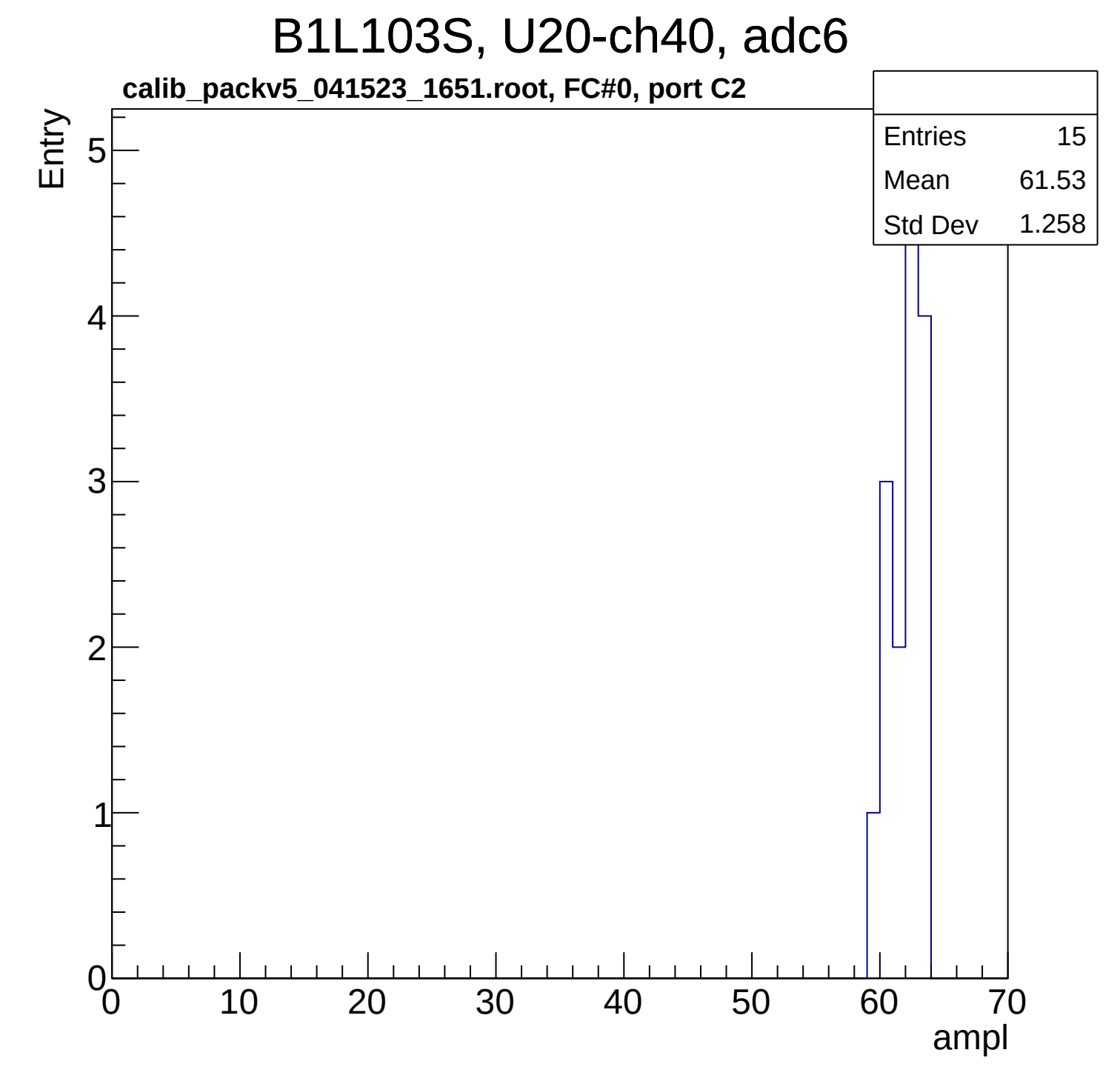
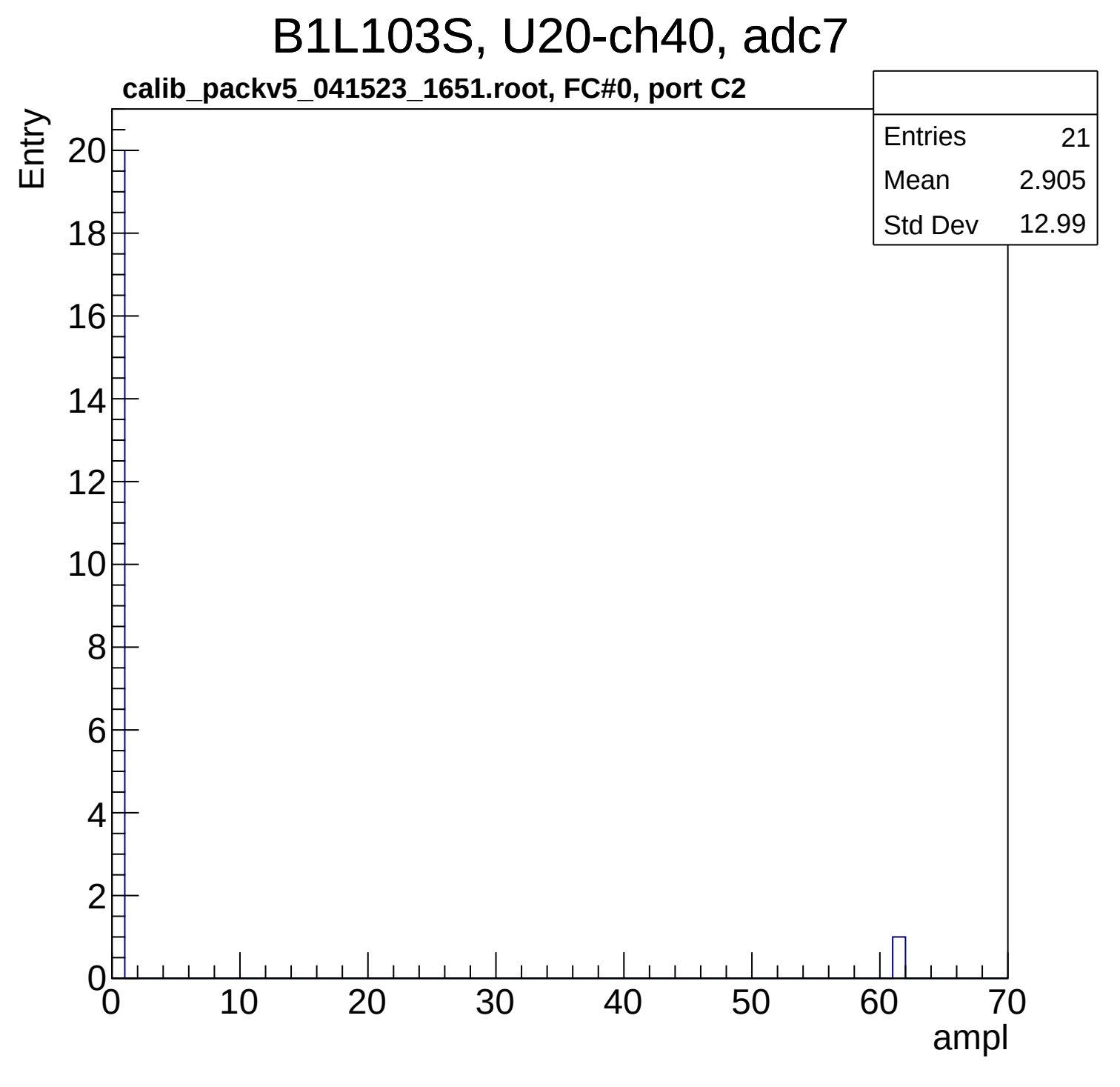
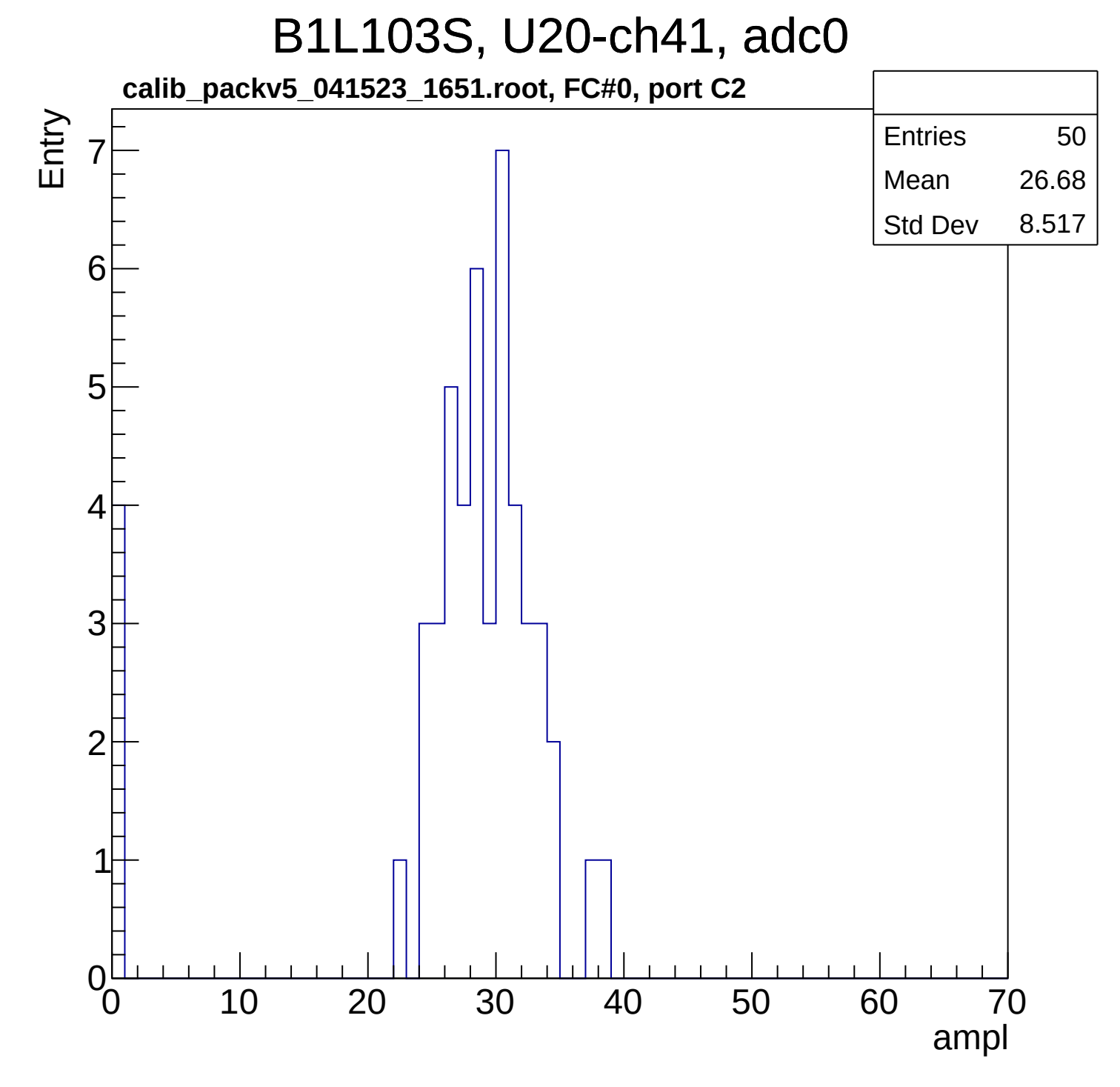
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch40, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 61.53
Std Dev 1.258
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U20-ch40, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 2.905
Std Dev 12.99
Entry
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch41, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 26.68
Std Dev 8.517
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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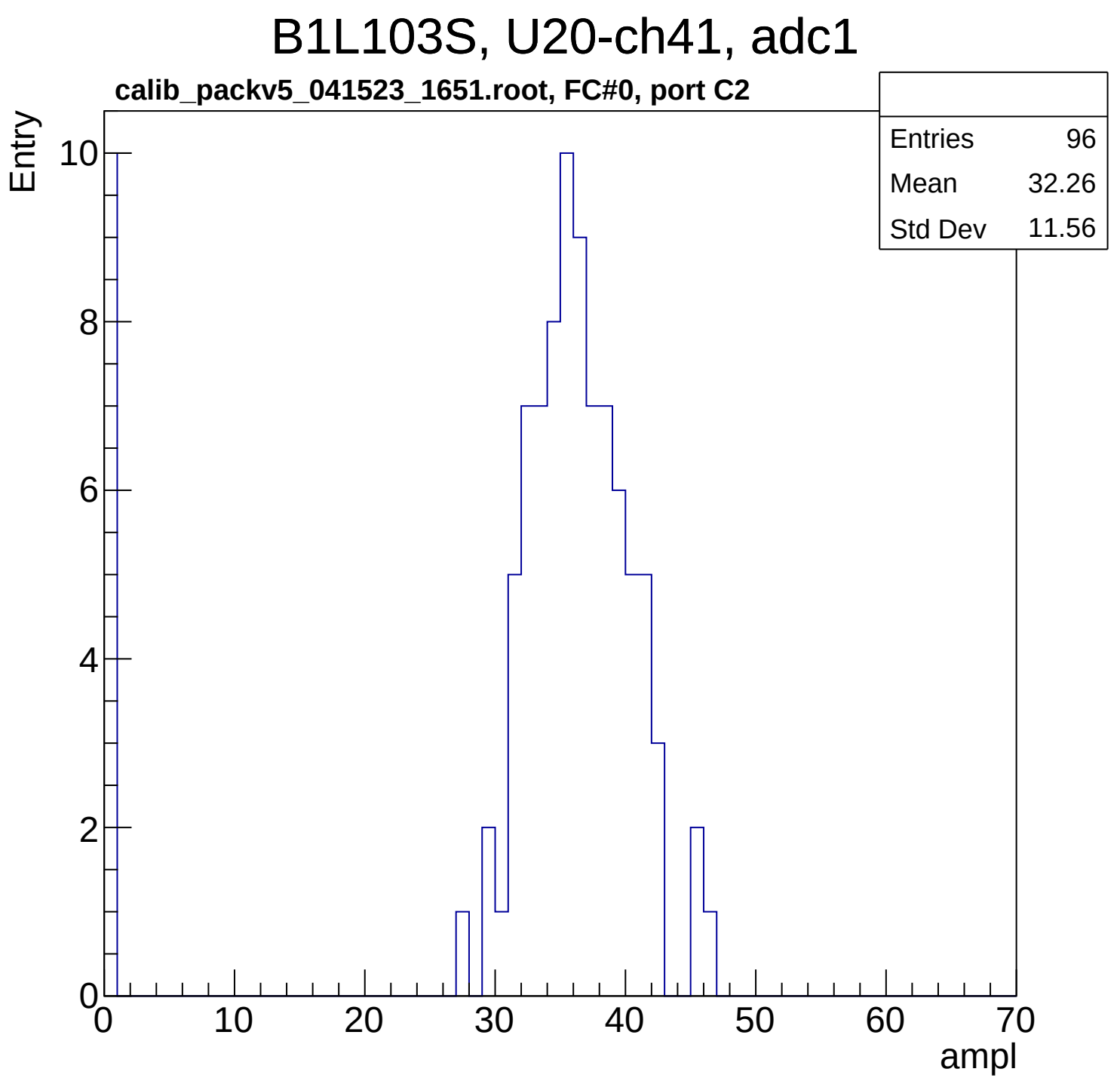
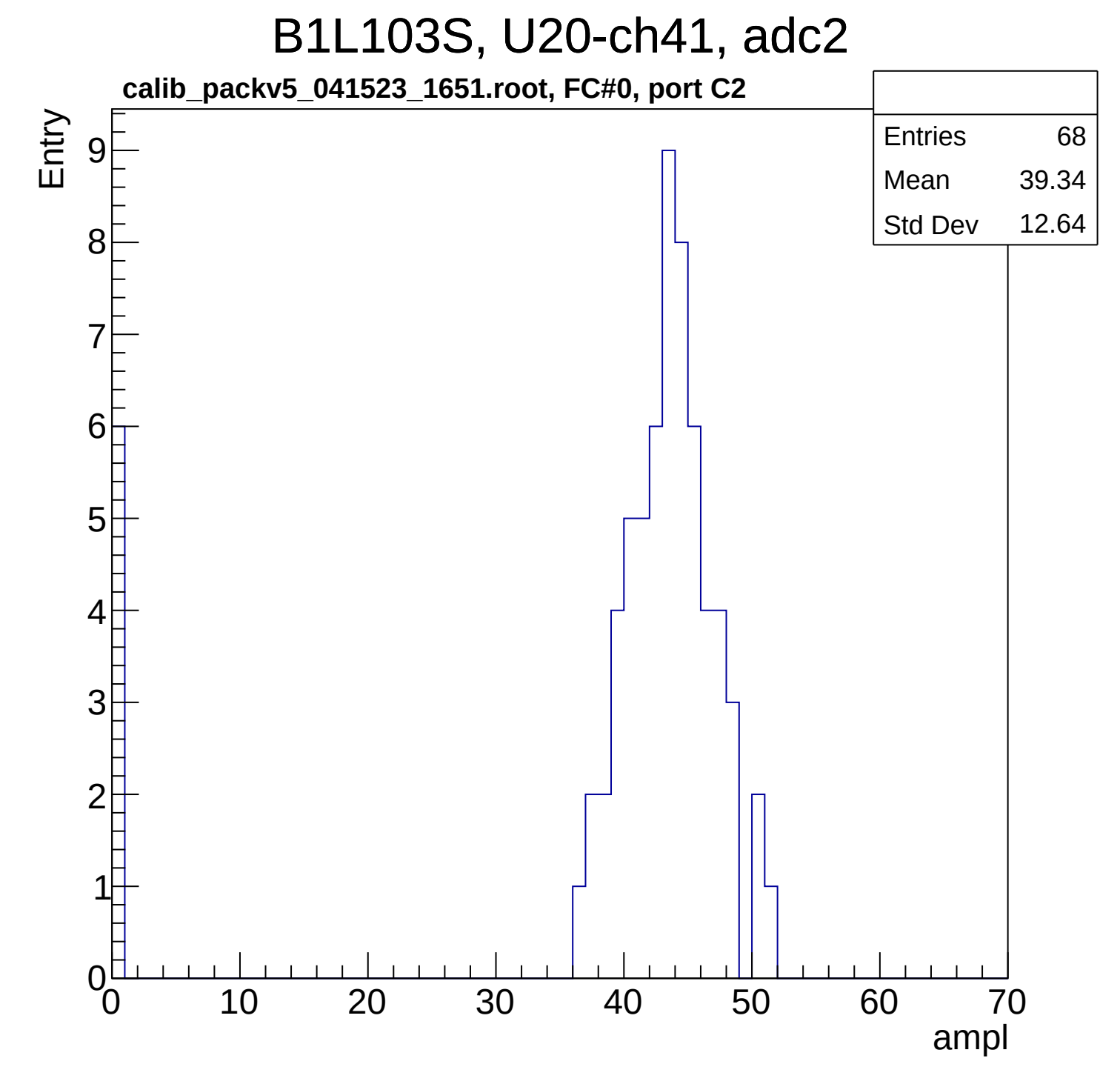

B1L103S, U20-ch41, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 96
Mean 32.26
Std Dev 11.56
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U20-ch41, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 39.34
Std Dev 12.64
Entry
ampl
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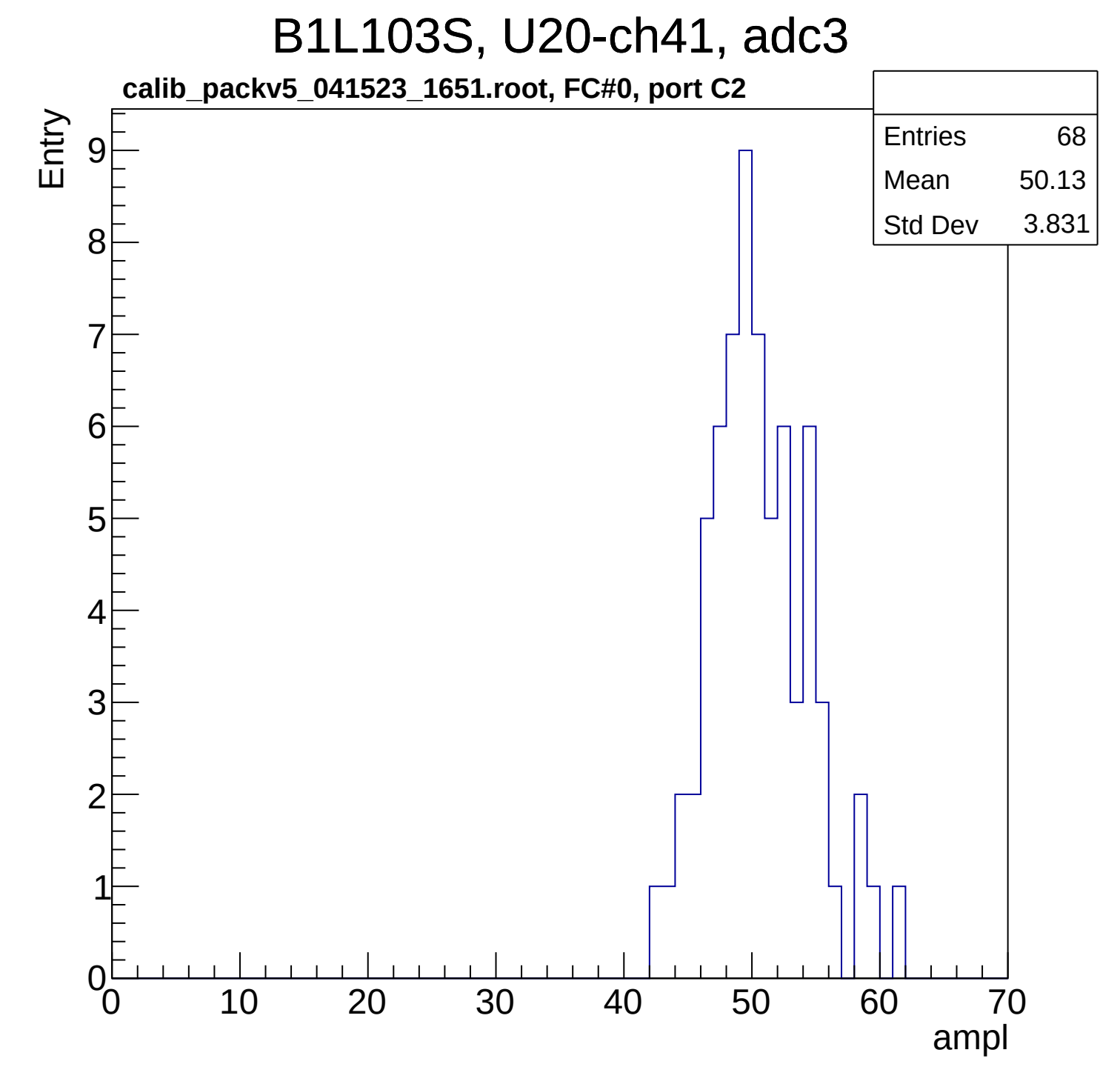
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch41, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 50.13
Std Dev 3.831
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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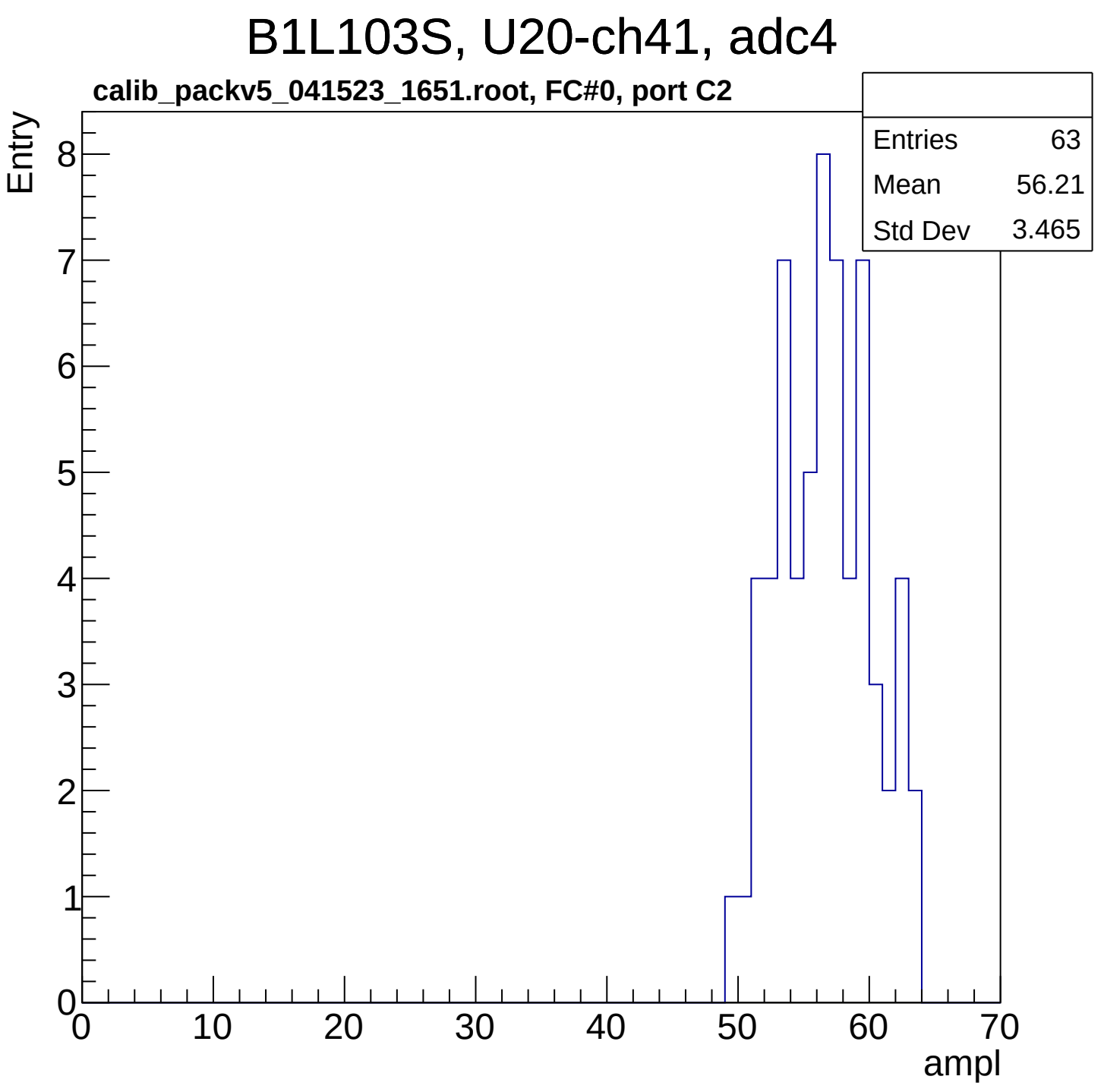
B1L103S, U20-ch41, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 56.21
Std Dev 3.465
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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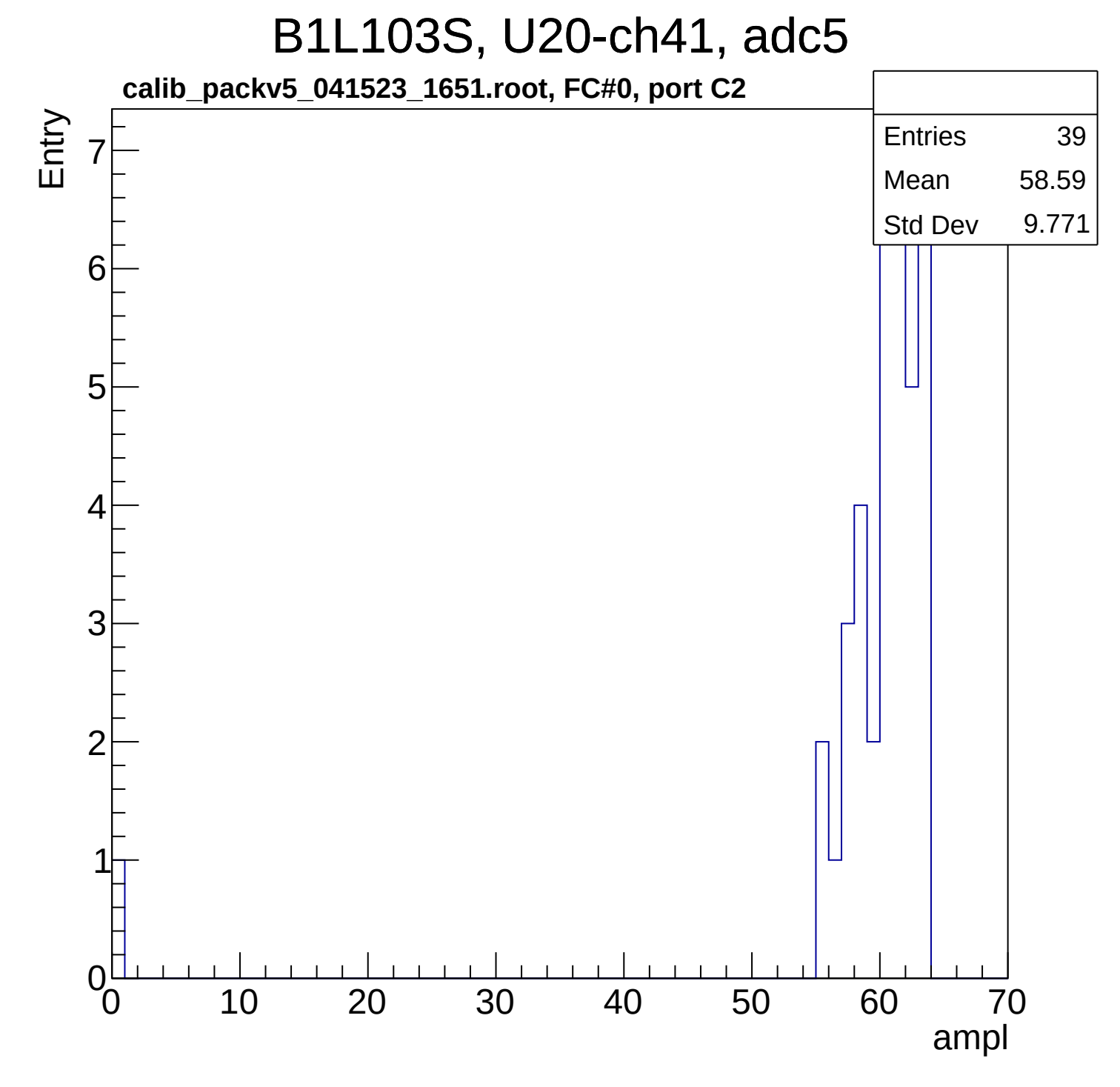
B1L103S, U20-ch41, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 58.59
Std Dev 9.771
Entry
ampl
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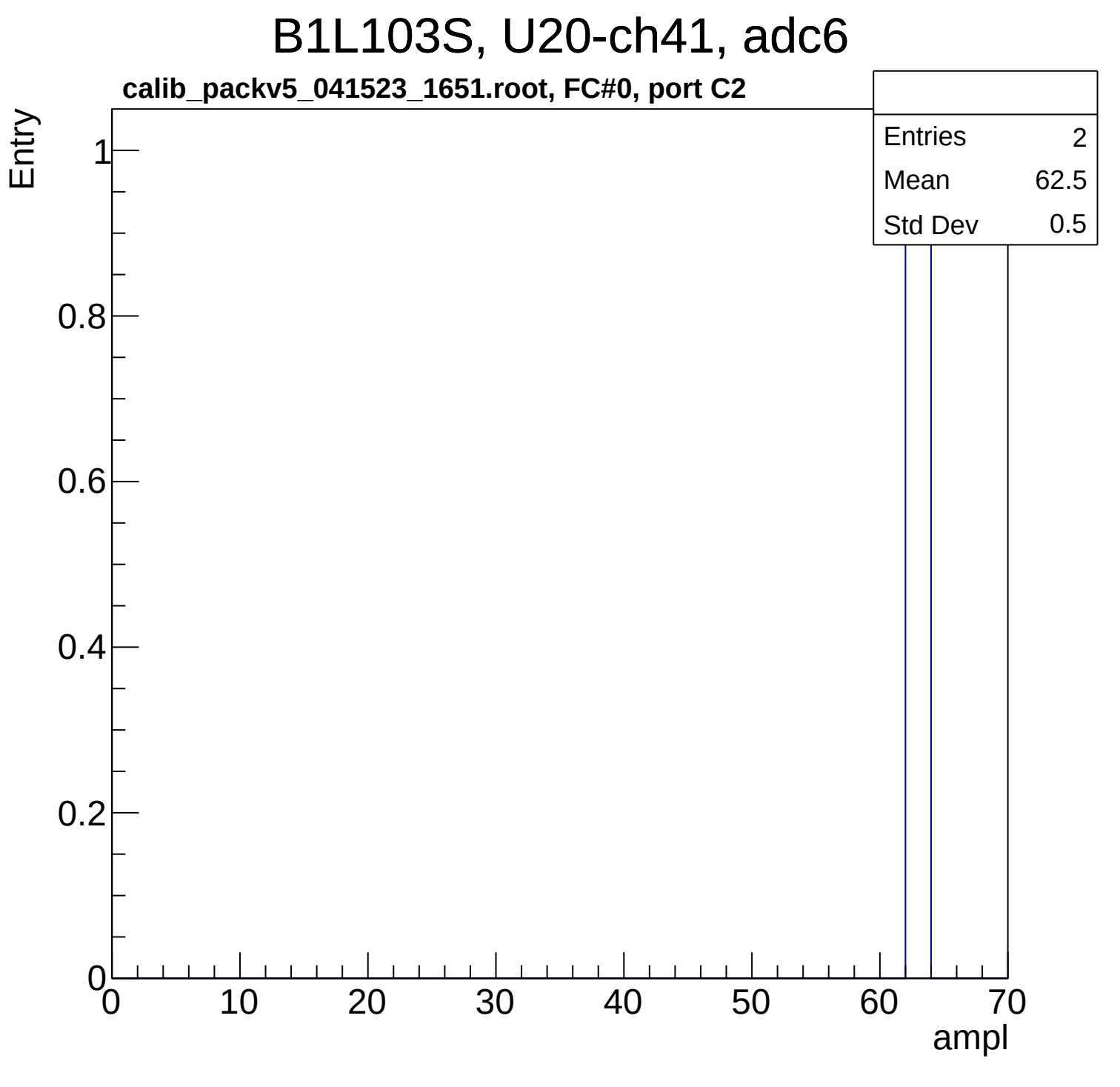
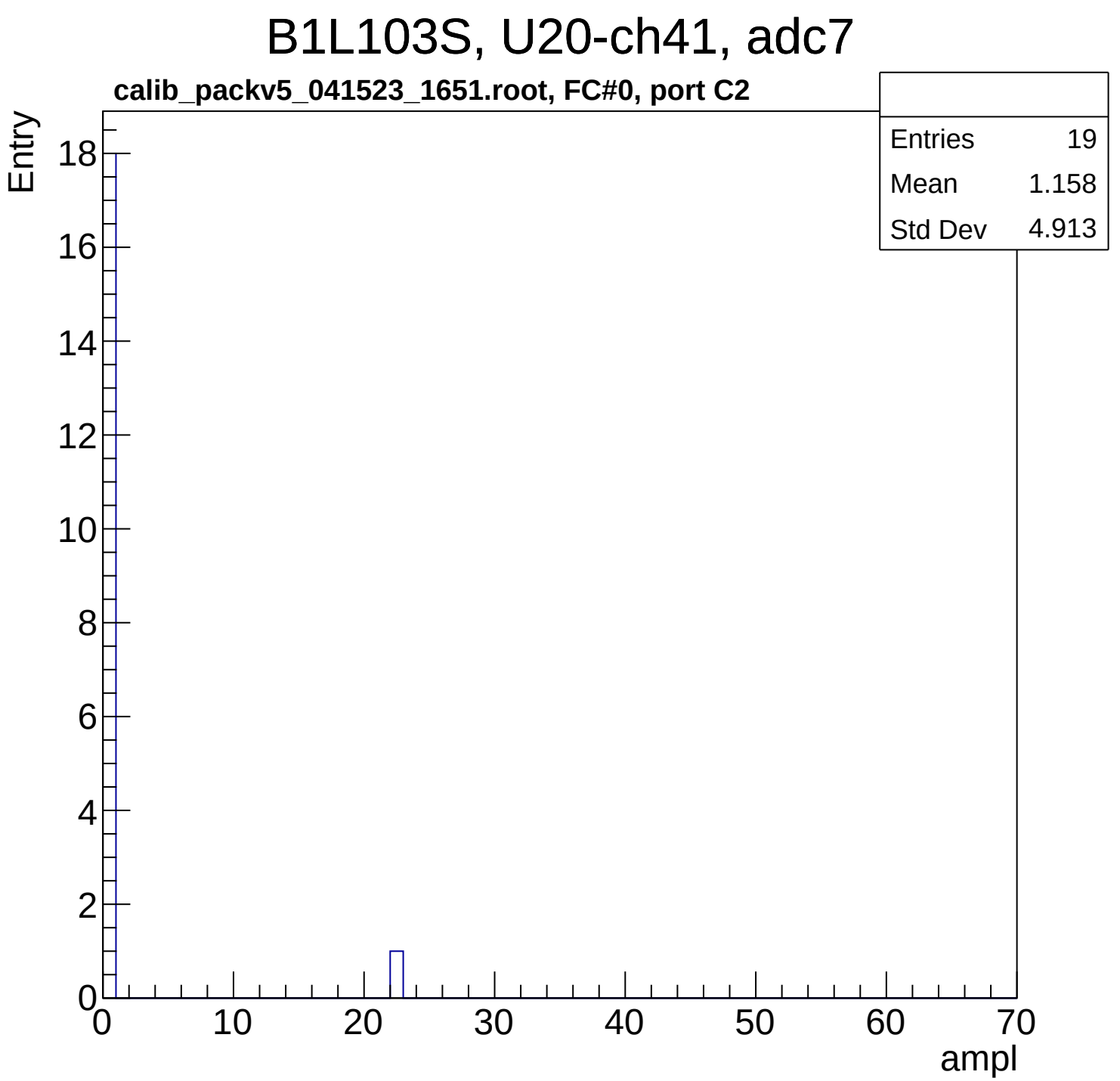
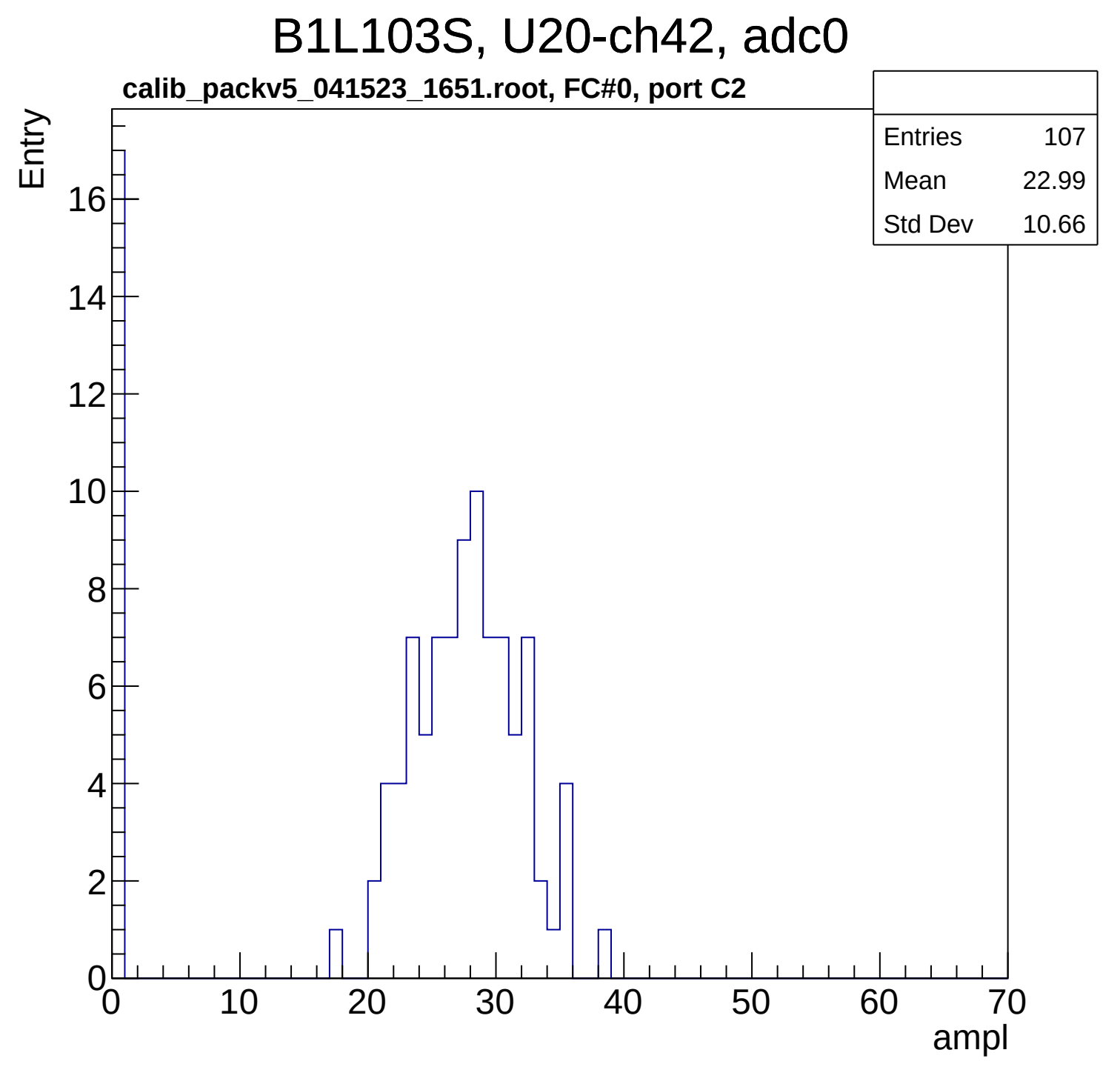
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U20-ch41, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch41, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.158
Std Dev 4.913
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch42, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 107
Mean 22.99
Std Dev 10.66
Entry
ampl
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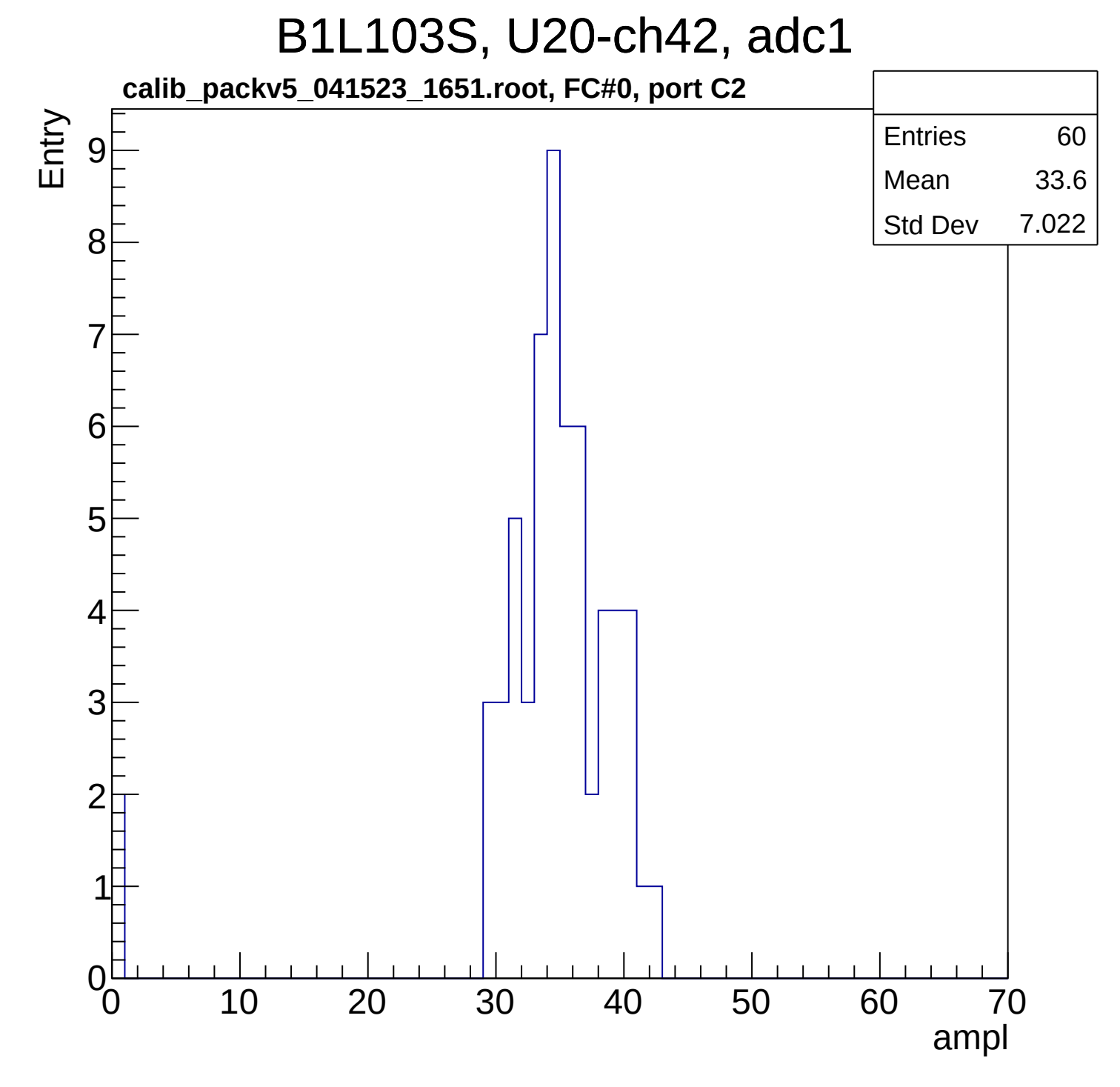
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L103S, U20-ch42, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 33.6
Std Dev 7.022
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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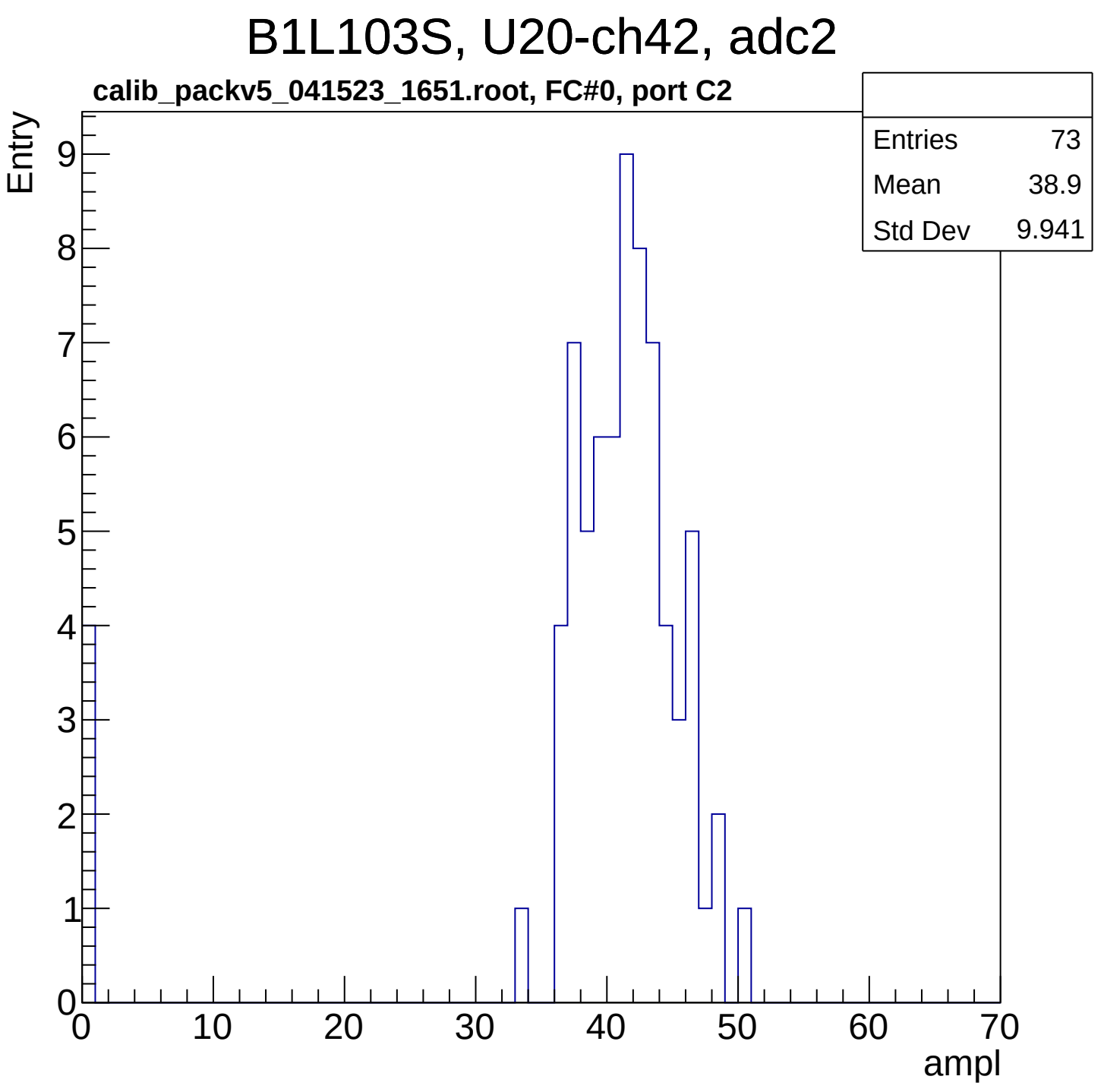
50
60
70


B1L103S, U20-ch42, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 38.9
Std Dev 9.941
Entry
ampl
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3
4
5
6
7
8
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0
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20
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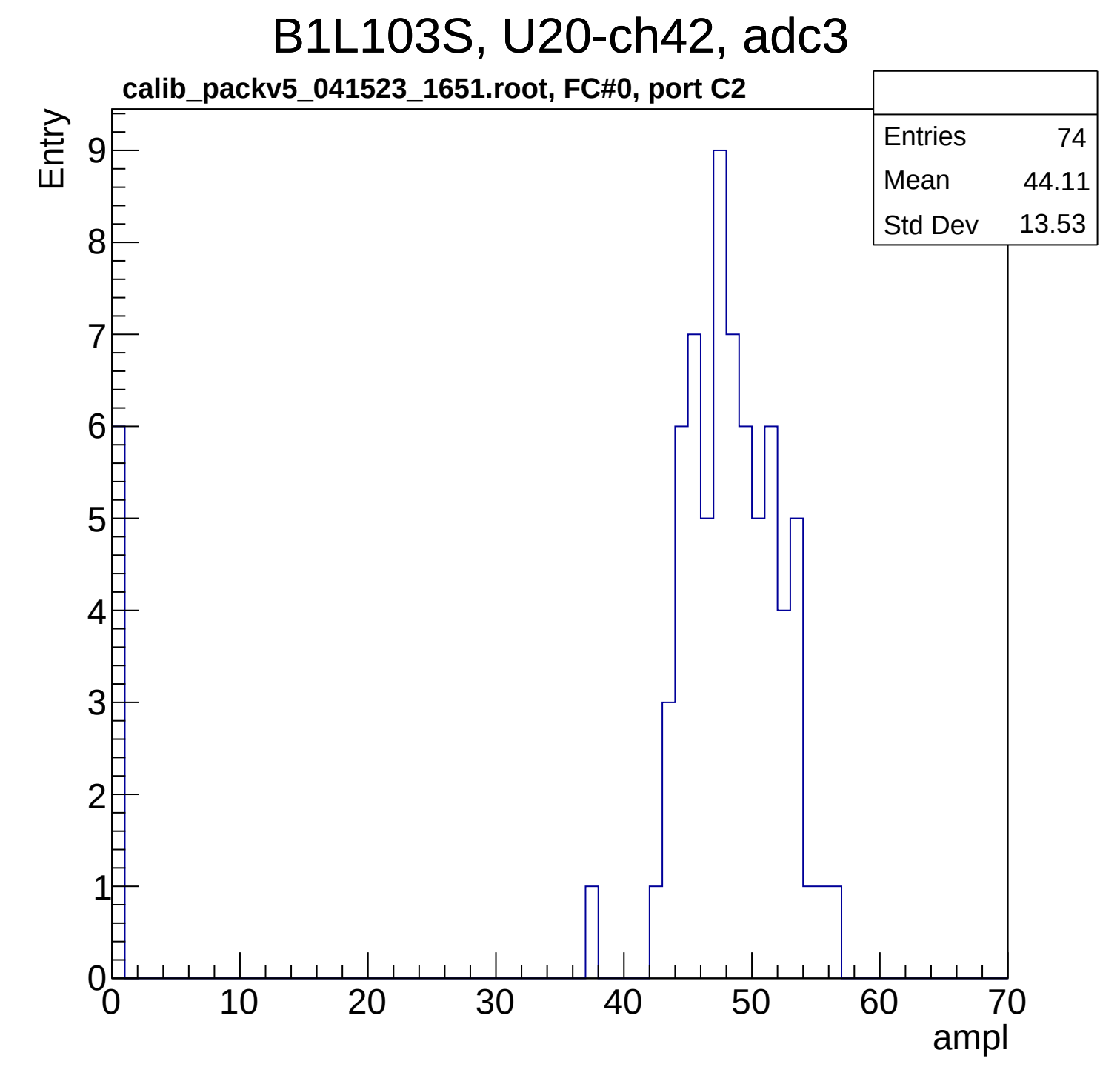
60
70


B1L103S, U20-ch42, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 44.11
Std Dev 13.53
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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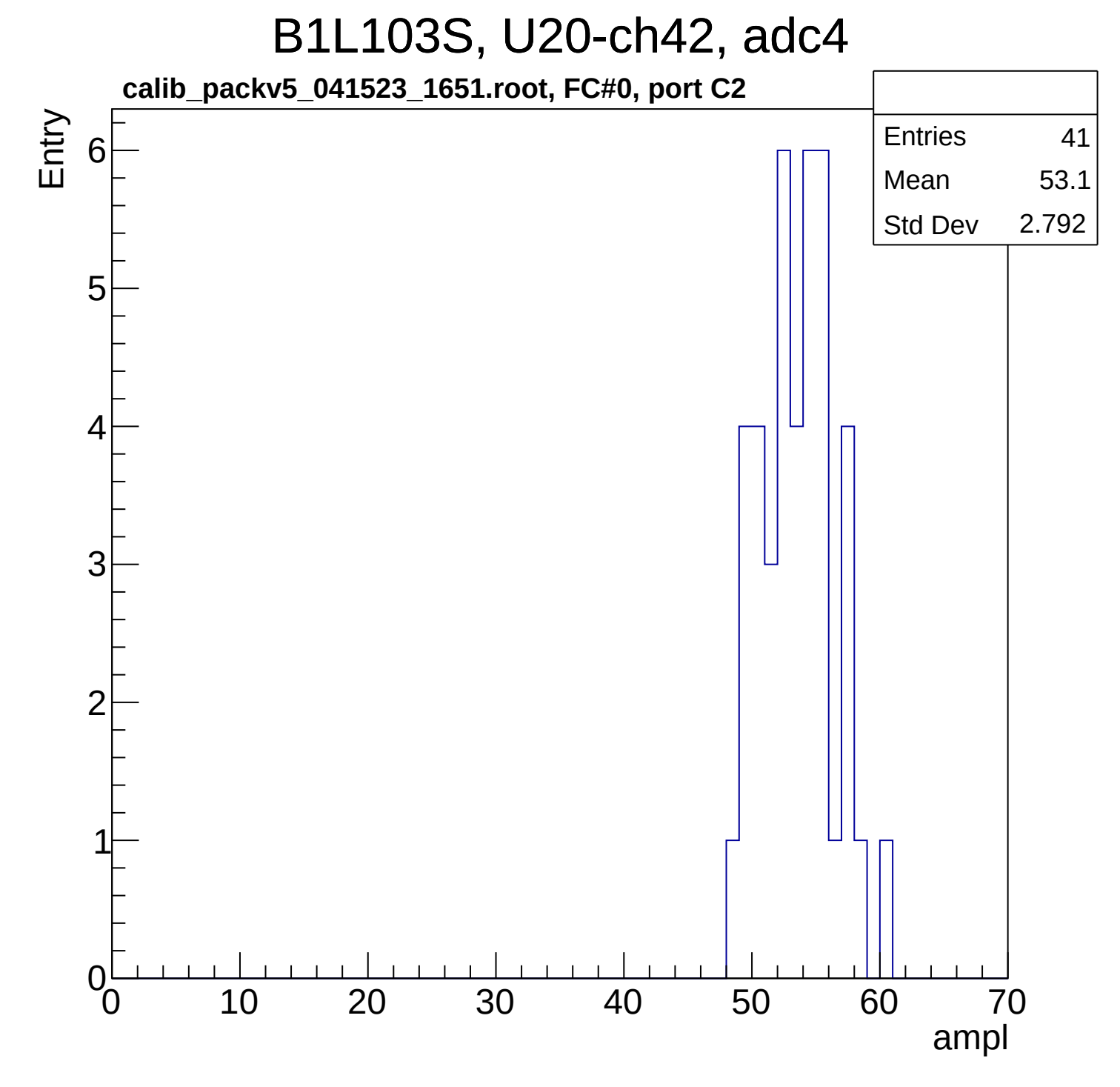
40
50
60
70


B1L103S, U20-ch42, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 53.1
Std Dev 2.792
Entry
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1
2
3
4
5
6
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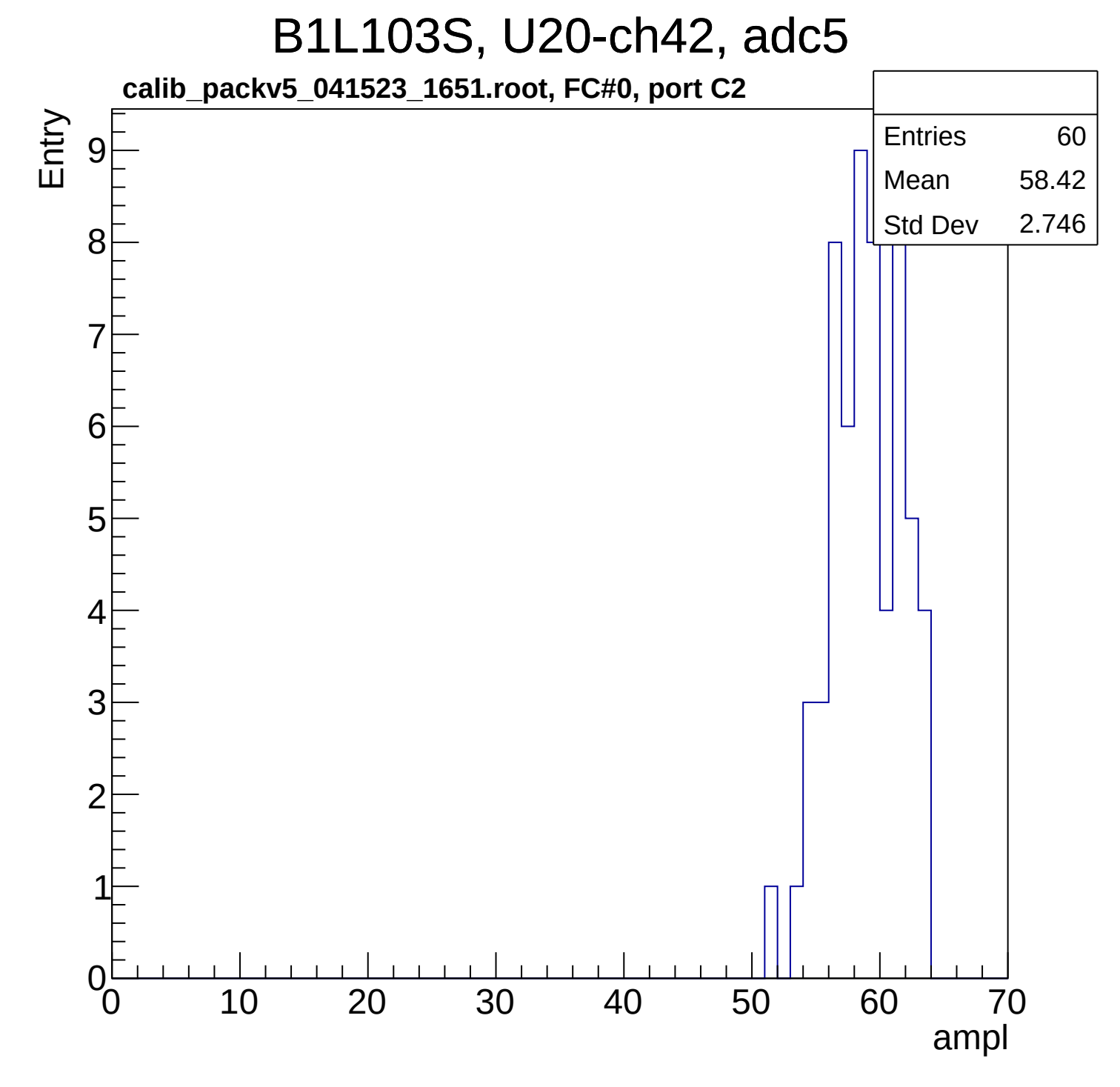
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch42, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 58.42
Std Dev 2.746
Entry
ampl
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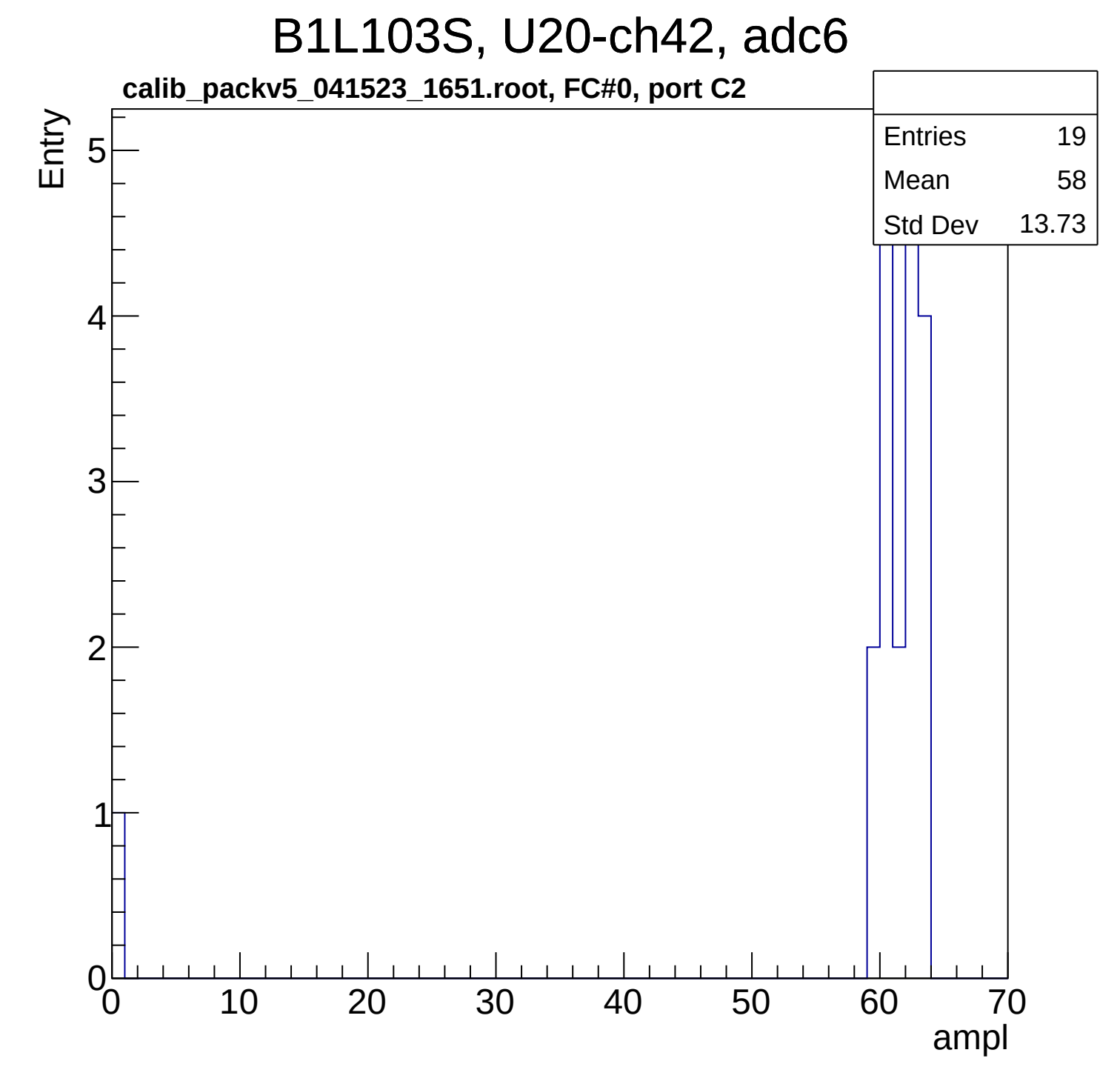
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch42, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 58
Std Dev 13.73
Entry
ampl
0
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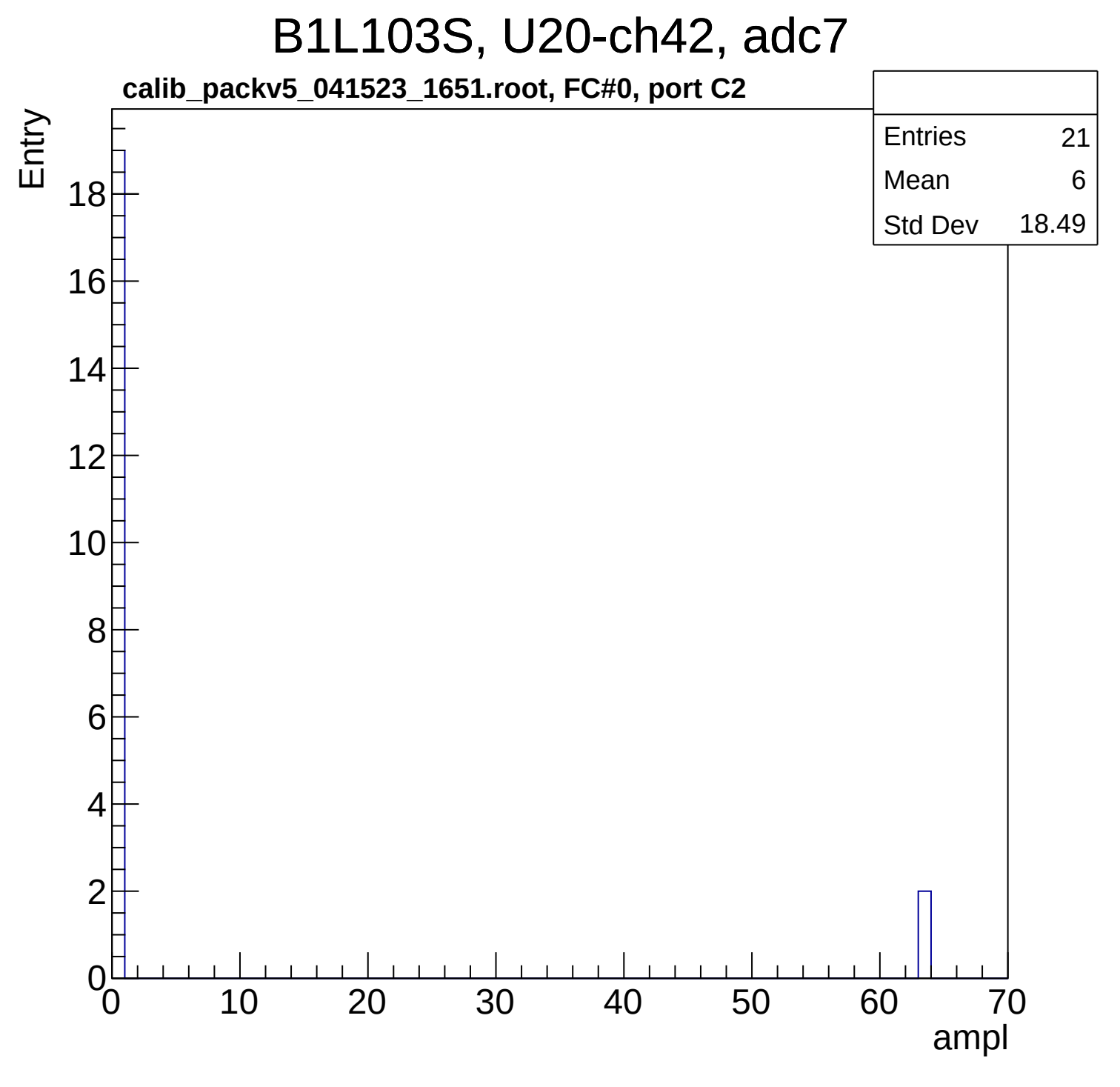
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U20-ch42, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 6
Std Dev 18.49
Entry
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6
8
10
12
14
16
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10
20
30
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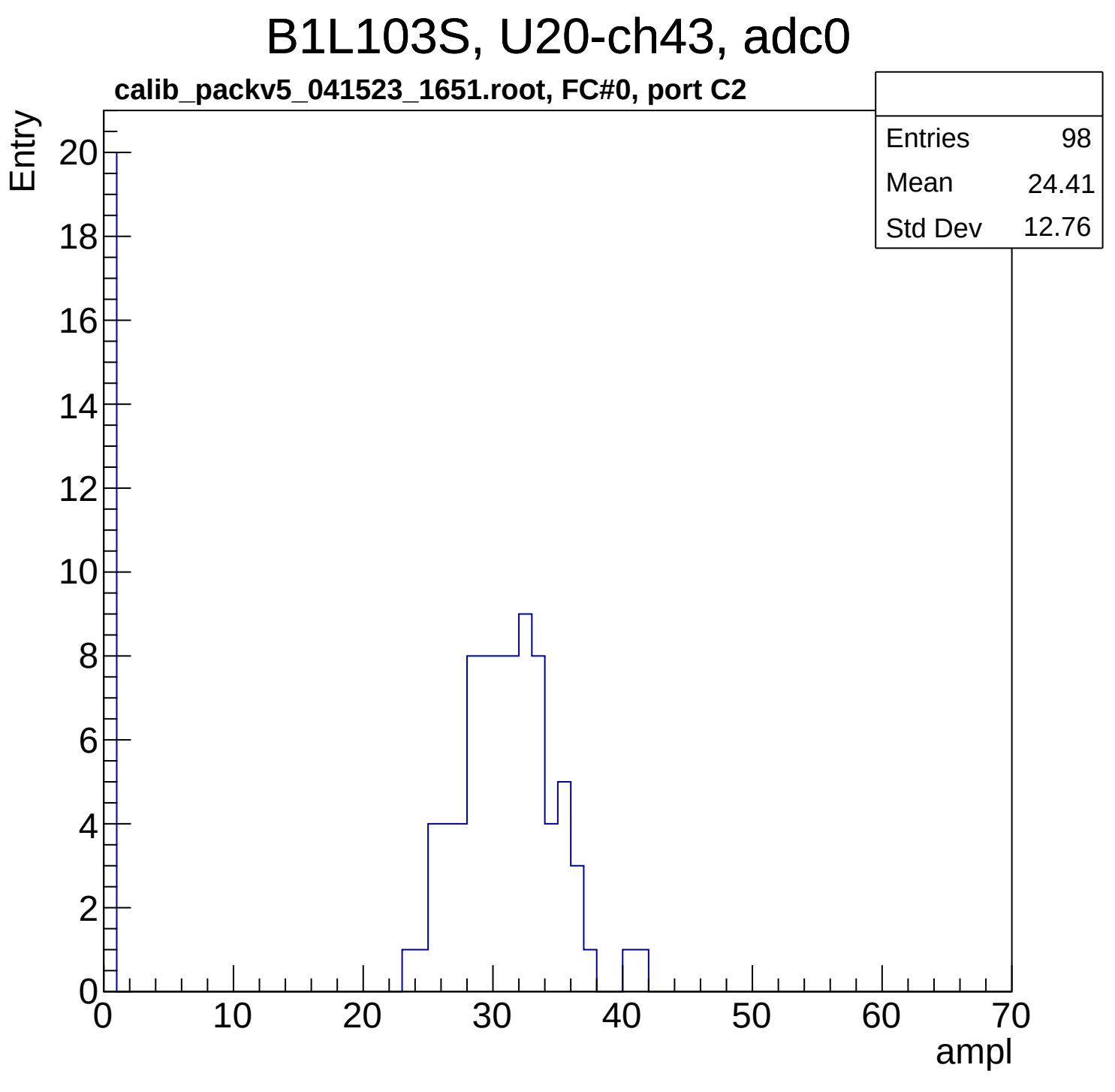
50
60
70
ampl


B1L103S, U20-ch43, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 98
Mean 24.41
Std Dev 12.76
Entry
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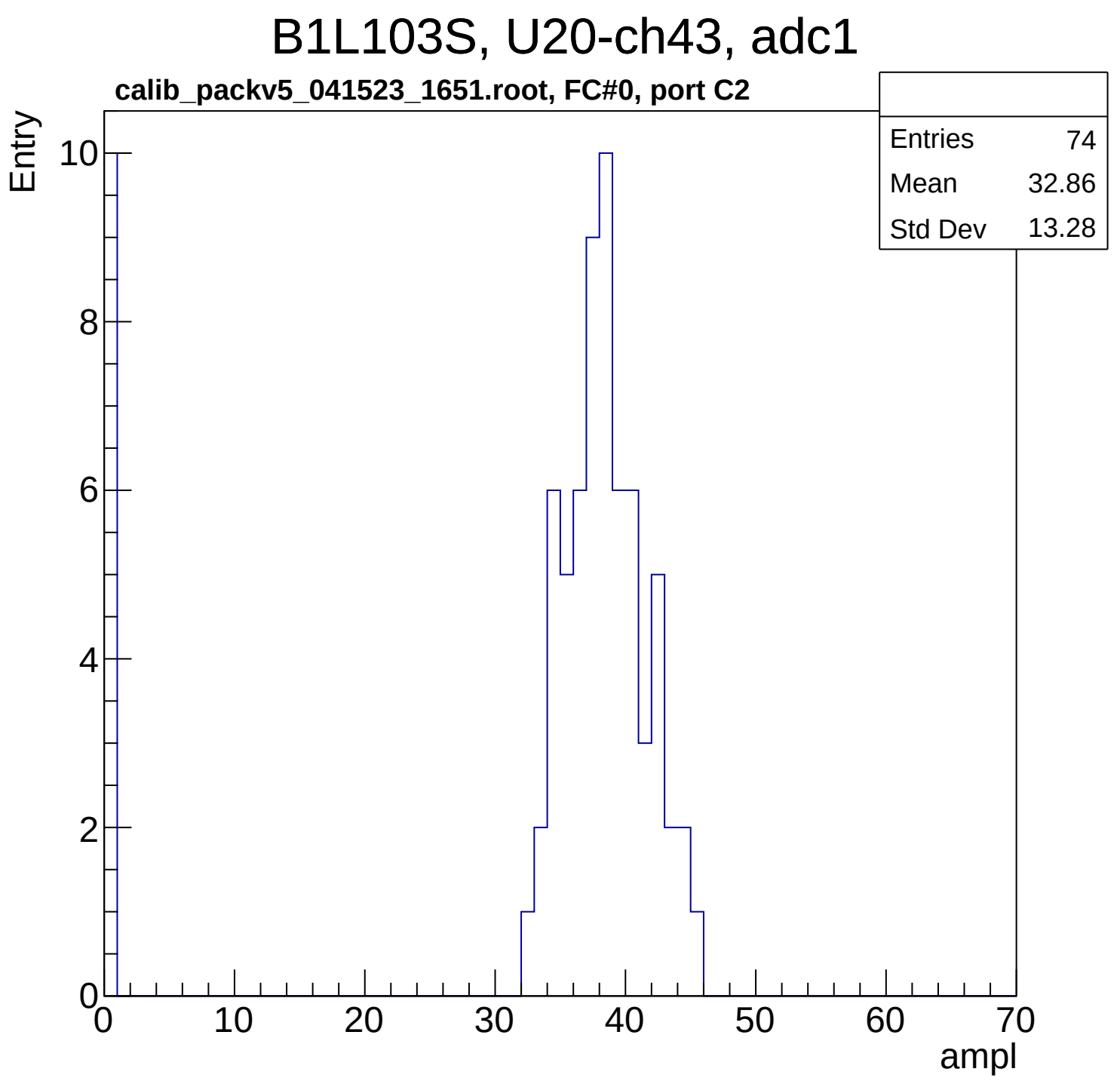
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch43, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 32.86
Std Dev 13.28
Entry
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8
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0
10
20
30
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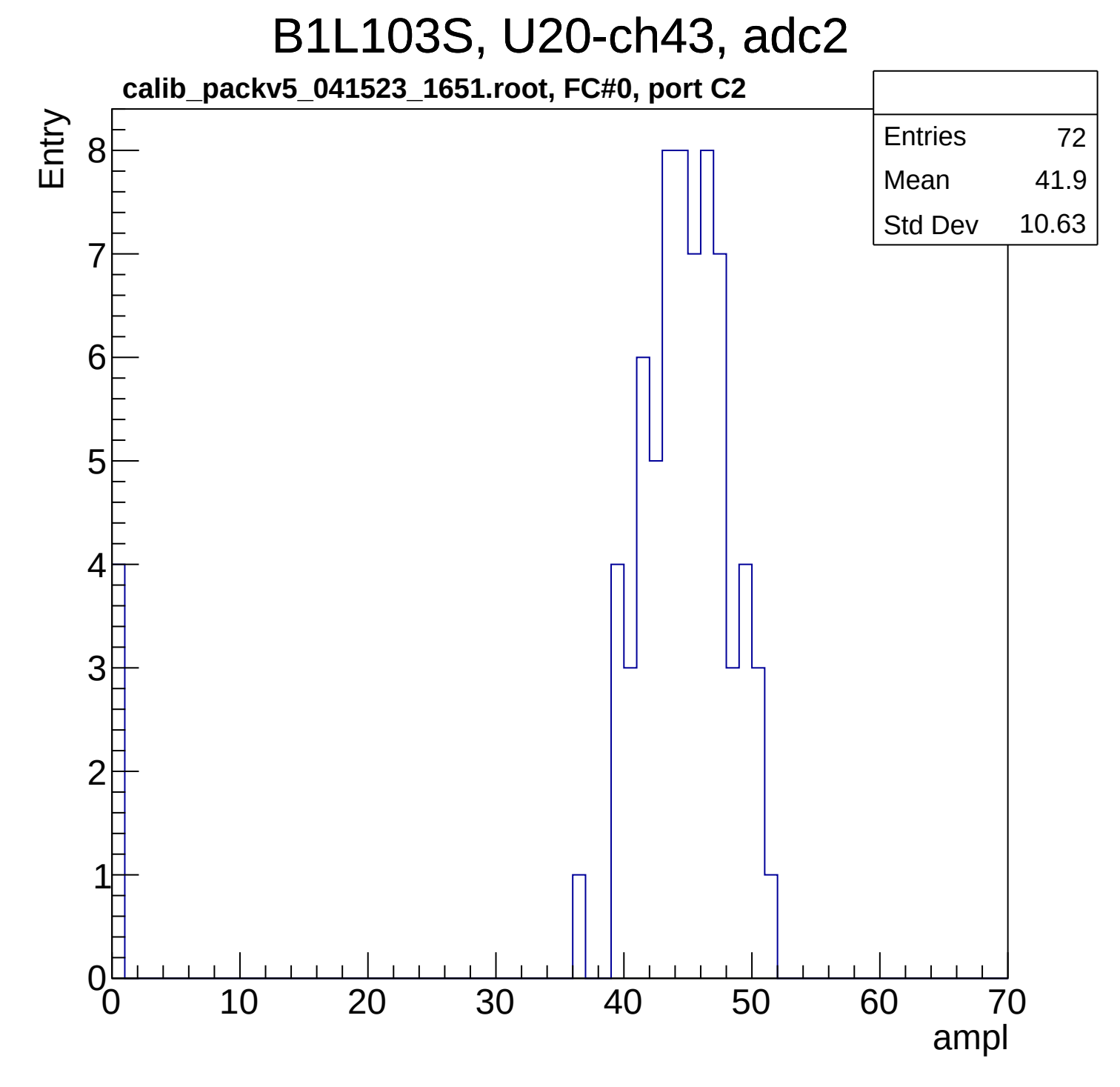
50
60
70
ampl


B1L103S, U20-ch43, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 41.9
Std Dev 10.63
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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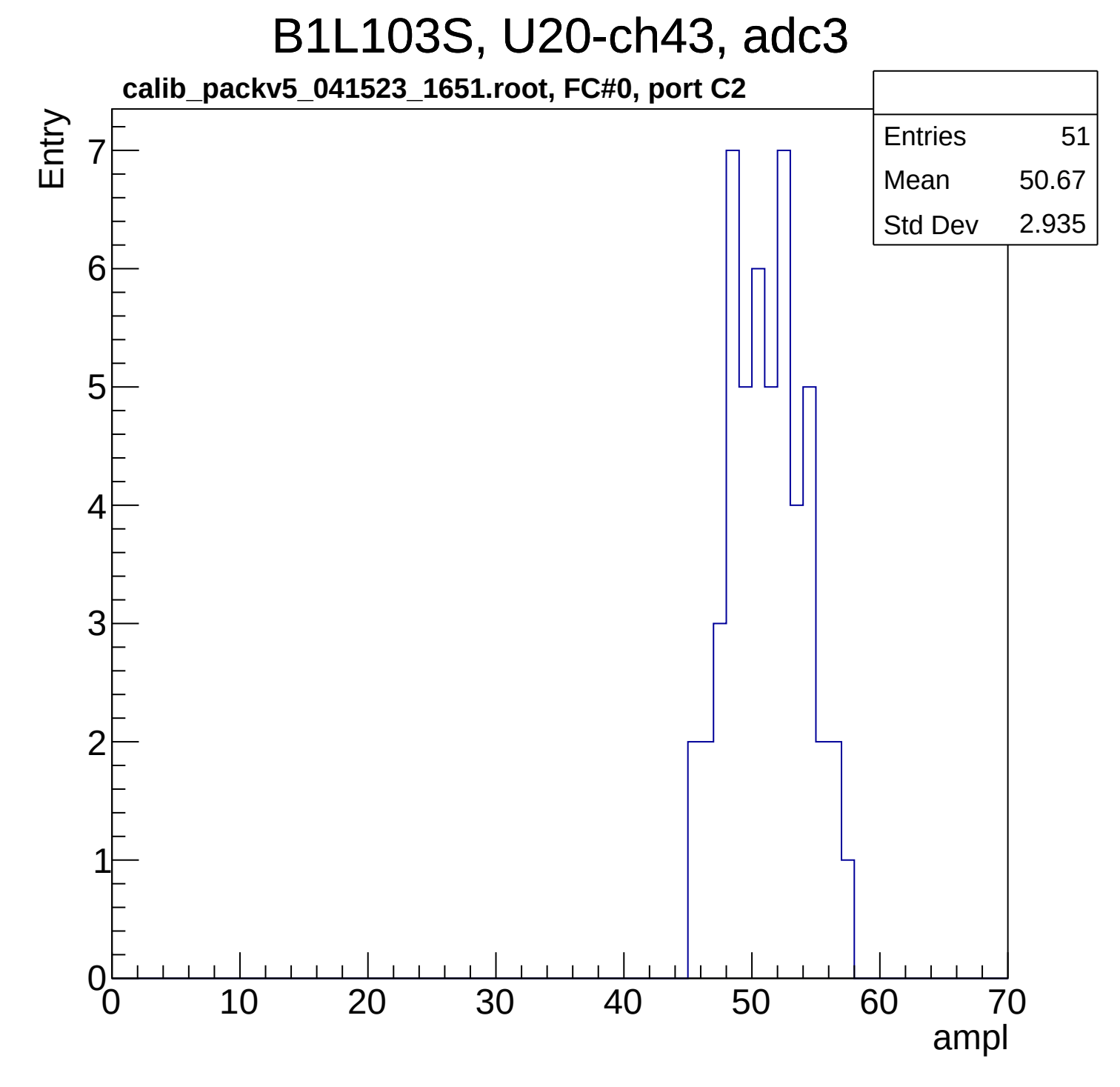
40
50
60
70


B1L103S, U20-ch43, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 50.67
Std Dev 2.935
Entry
ampl
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7
0
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20
30
40
50
60
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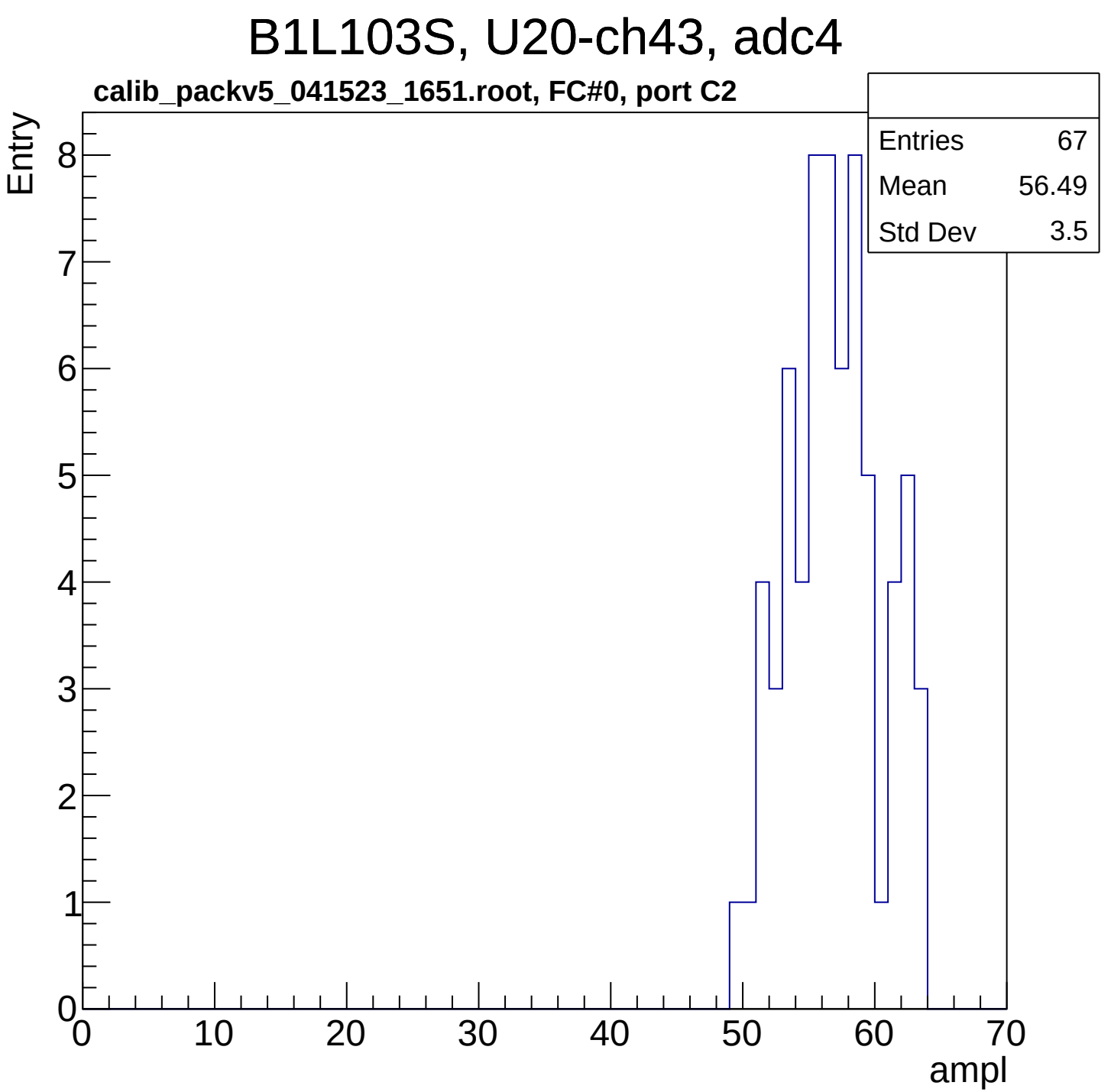
B1L103S, U20-ch43, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 56.49
Std Dev 3.5
Entry
ampl
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2
3
4
5
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8
0
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40
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60
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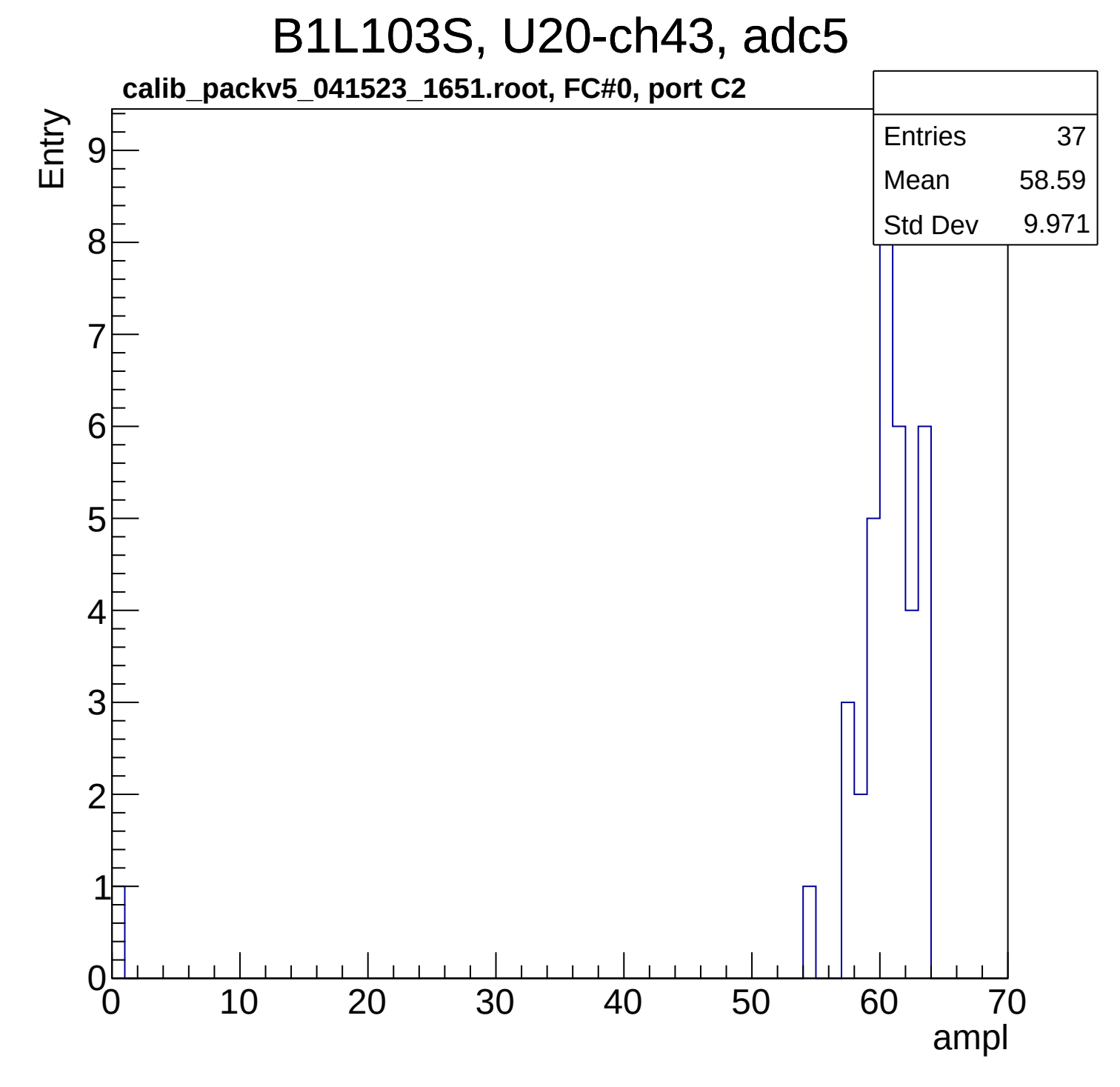
B1L103S, U20-ch43, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 58.59
Std Dev 9.971
Entry
ampl
0
1
2
3
4
5
6
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8
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0
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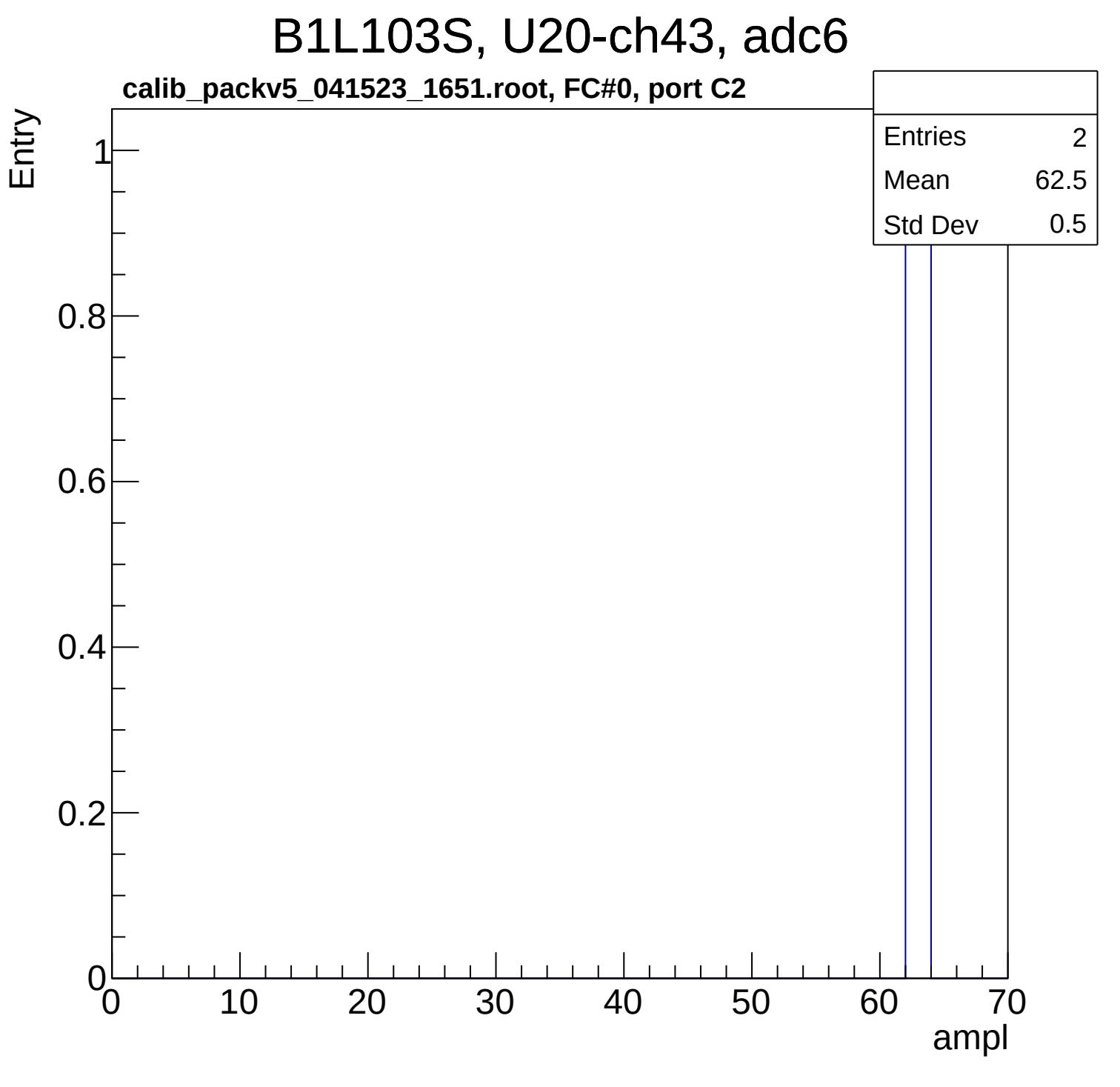
60
70


B1L103S, U20-ch43, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
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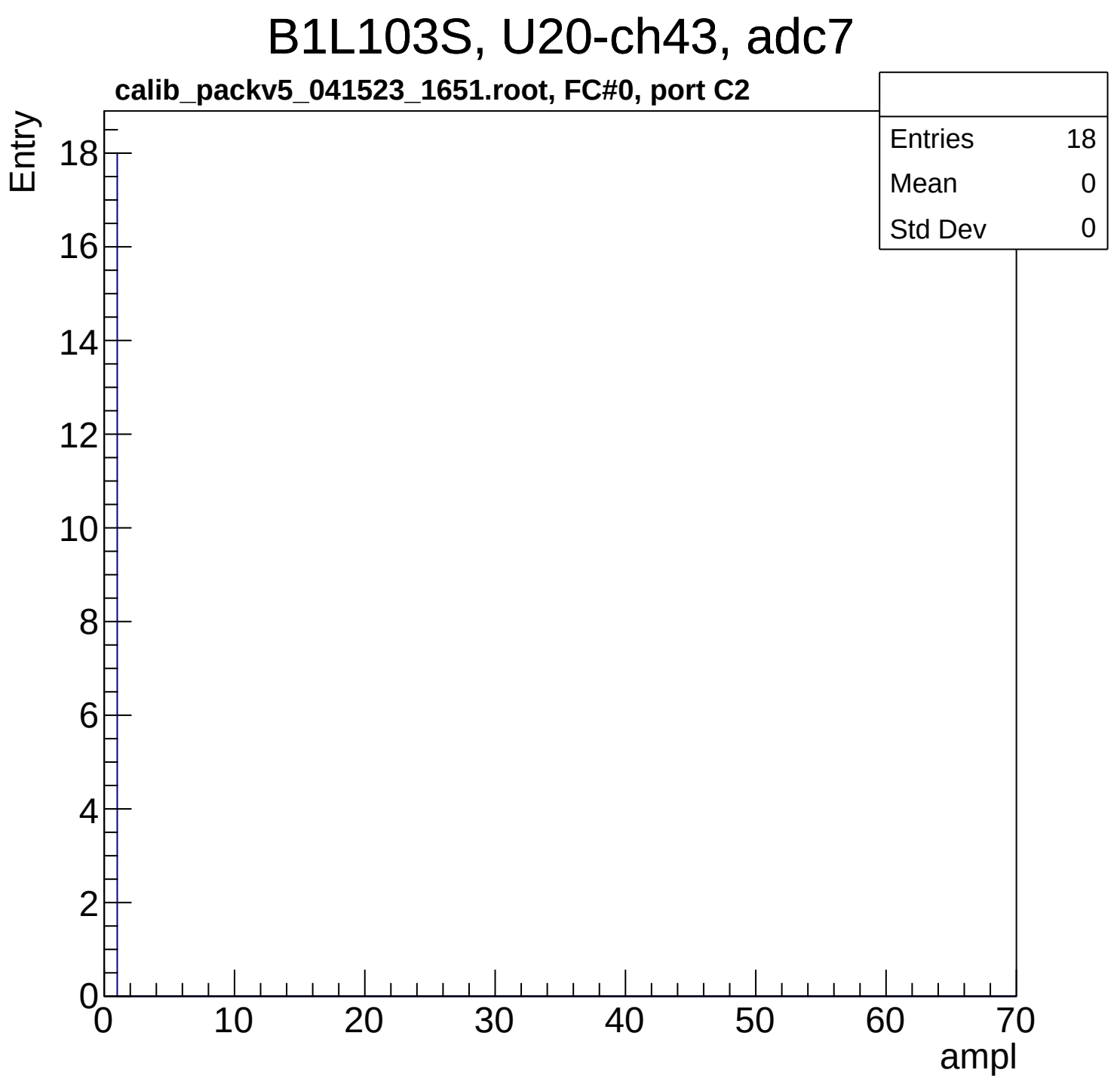
50
60
70
ampl


B1L103S, U20-ch43, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
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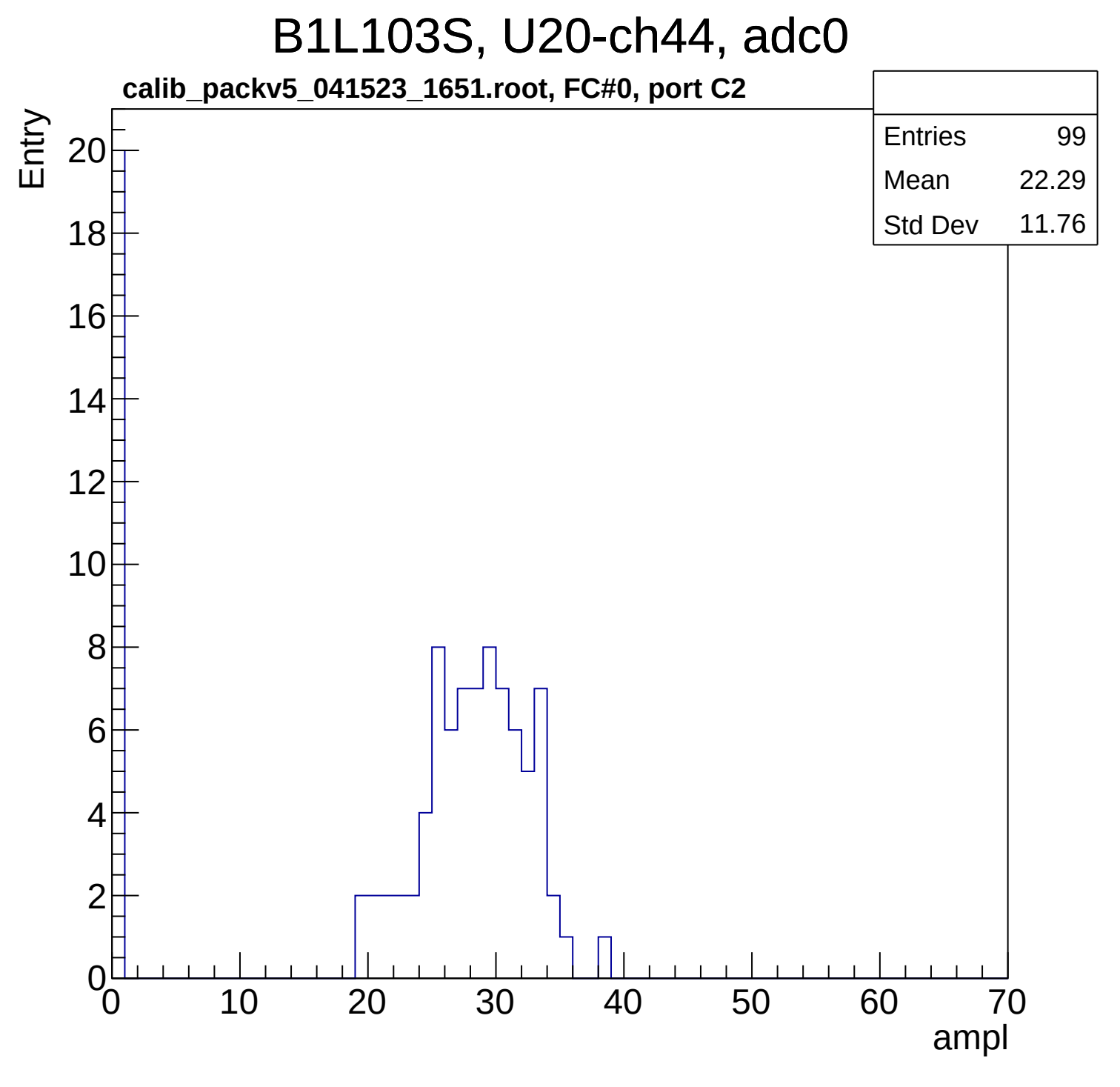
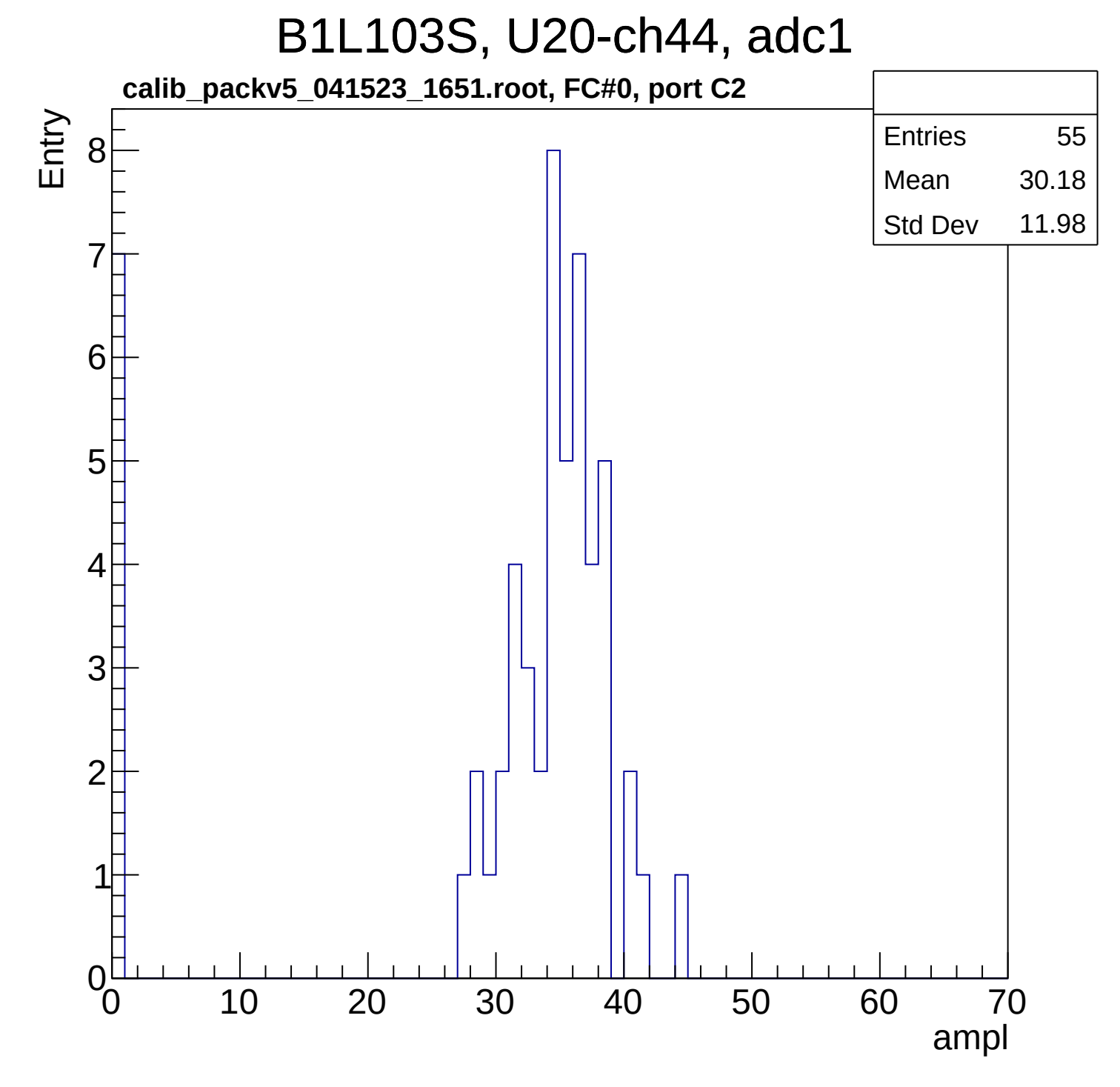
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch44, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 22.29
Std Dev 11.76
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70


B1L103S, U20-ch44, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 30.18
Std Dev 11.98
Entry
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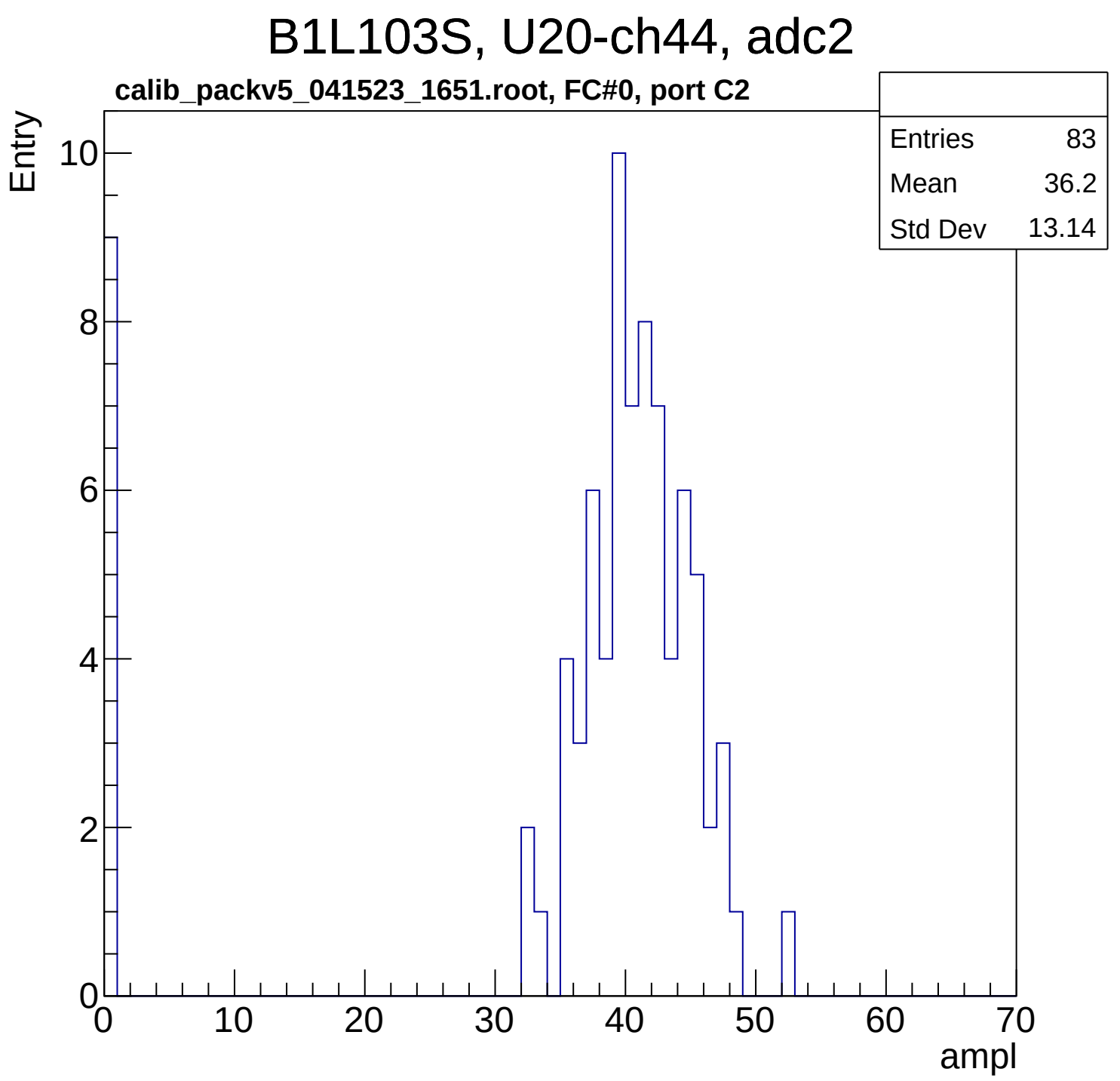
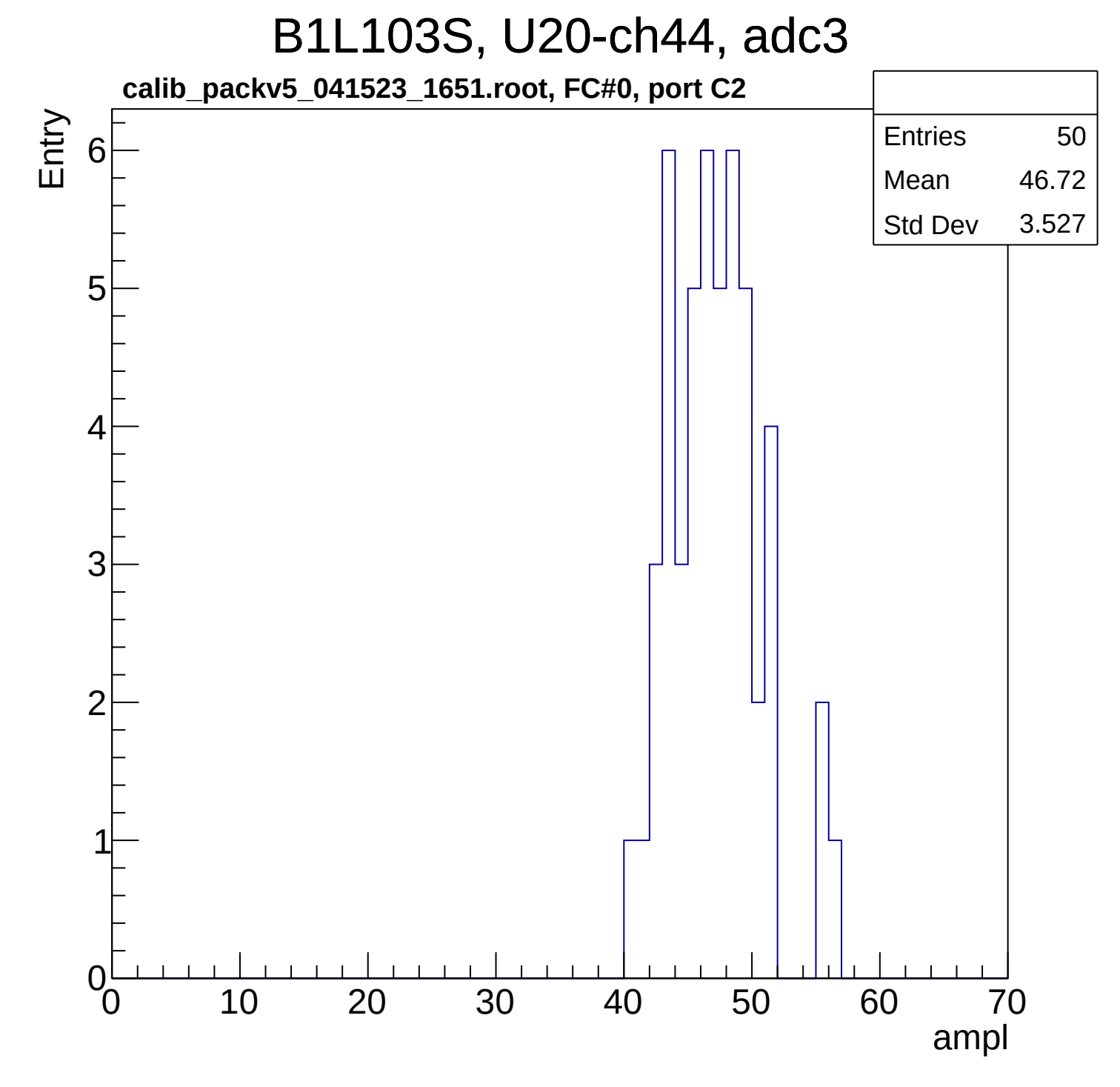
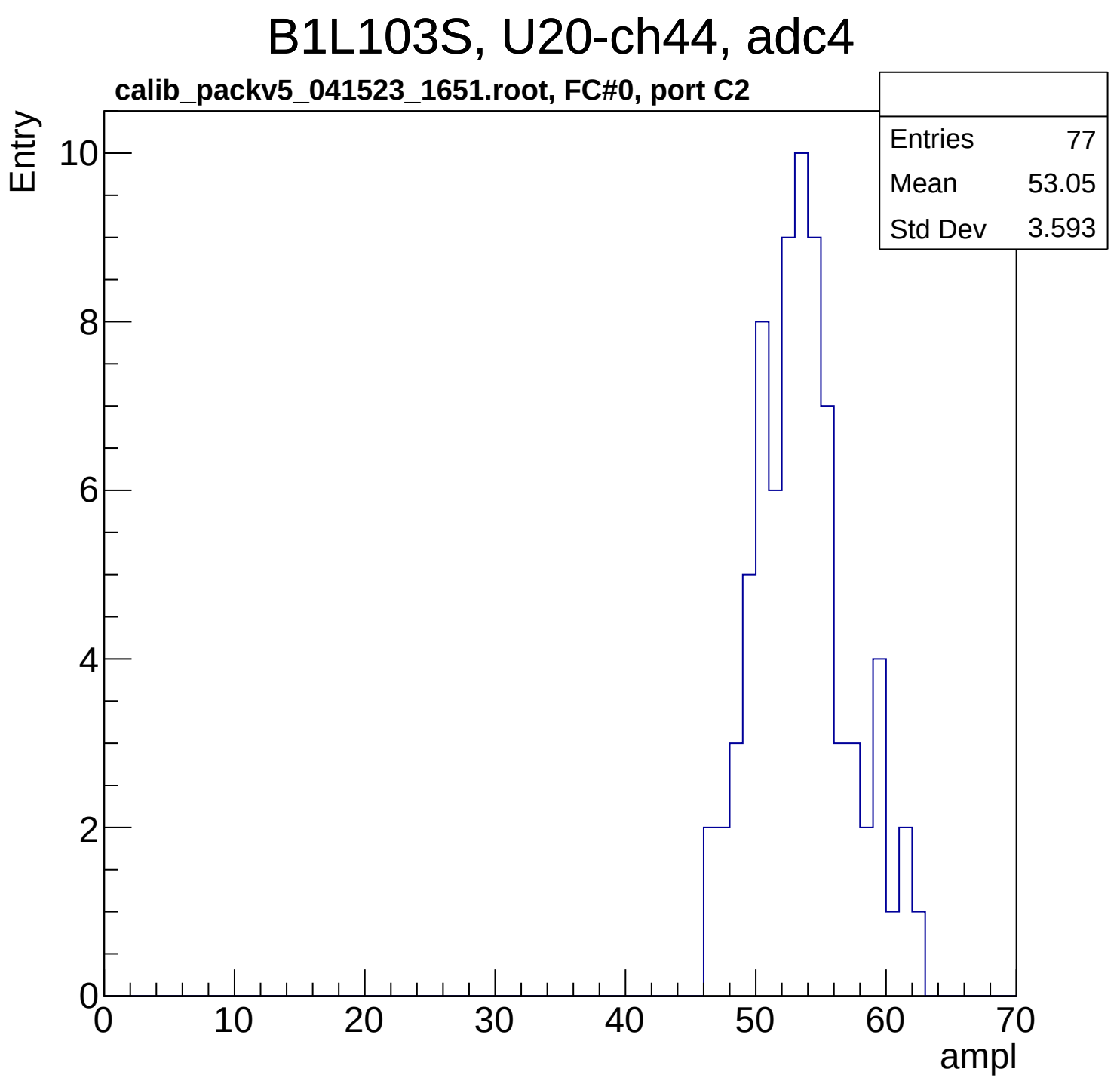
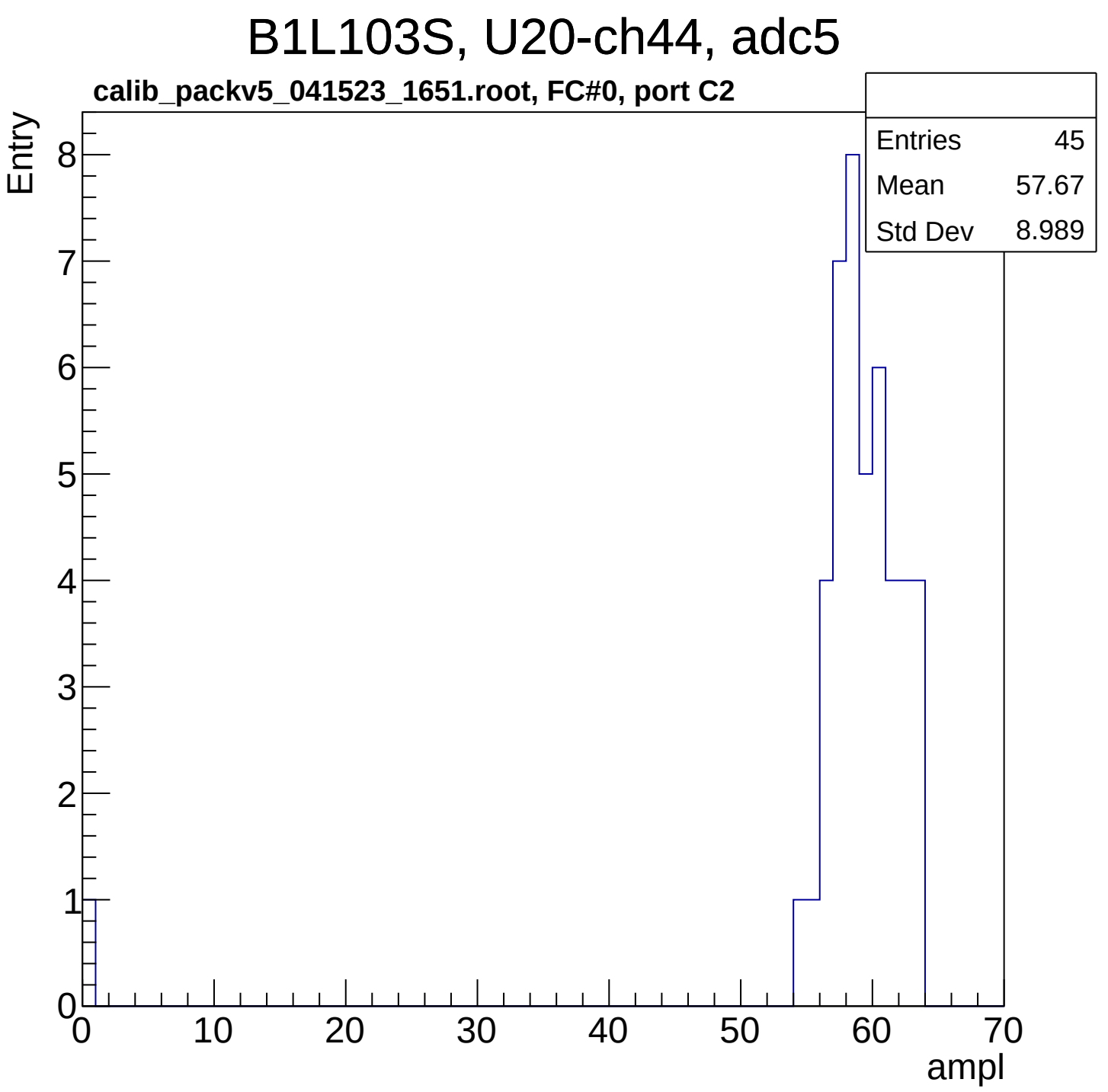
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch44, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 36.2
Std Dev 13.14
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U20-ch44, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 46.72
Std Dev 3.527
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U20-ch44, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 53.05
Std Dev 3.593
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch44, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 57.67
Std Dev 8.989
Entry
ampl
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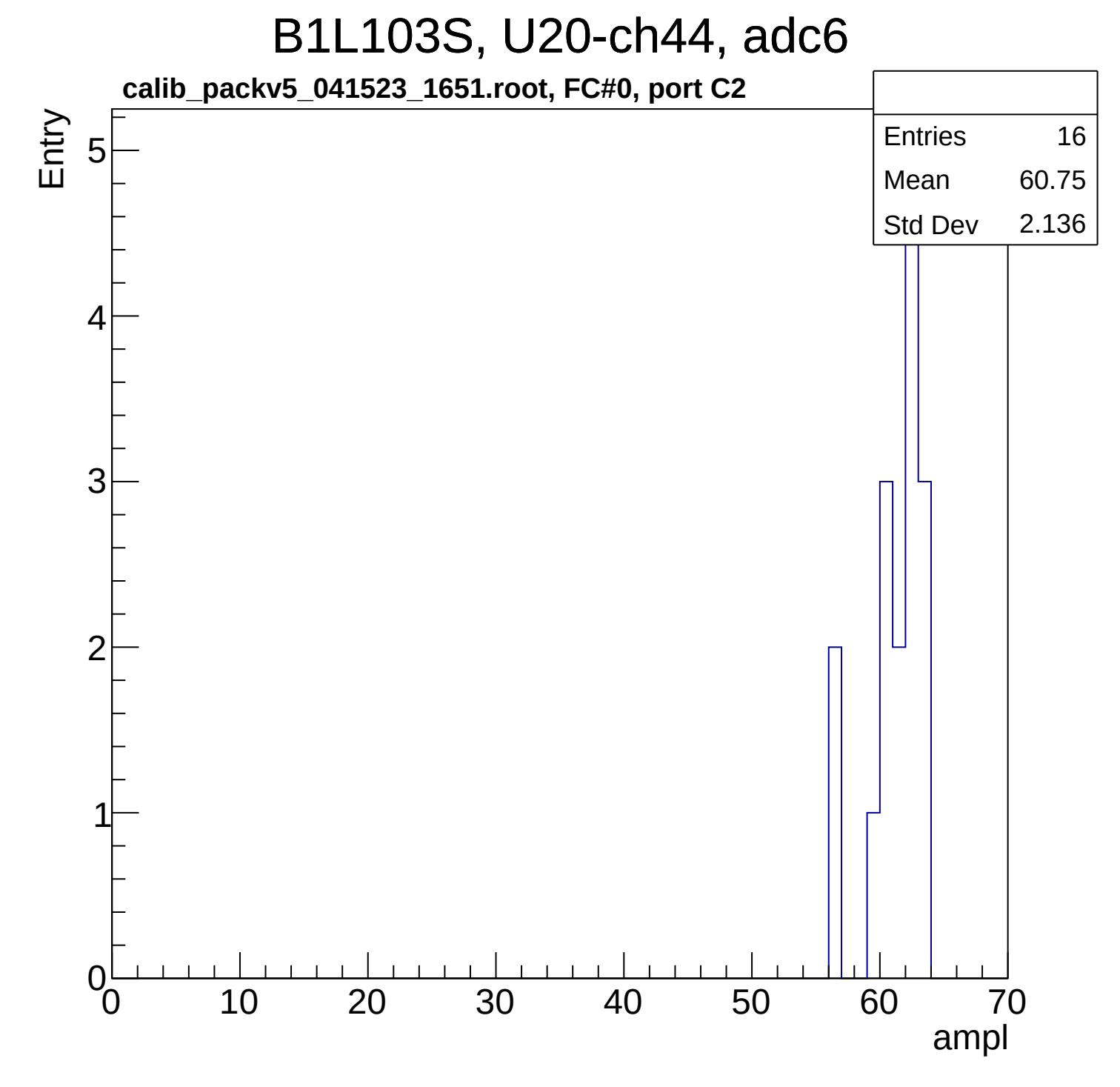
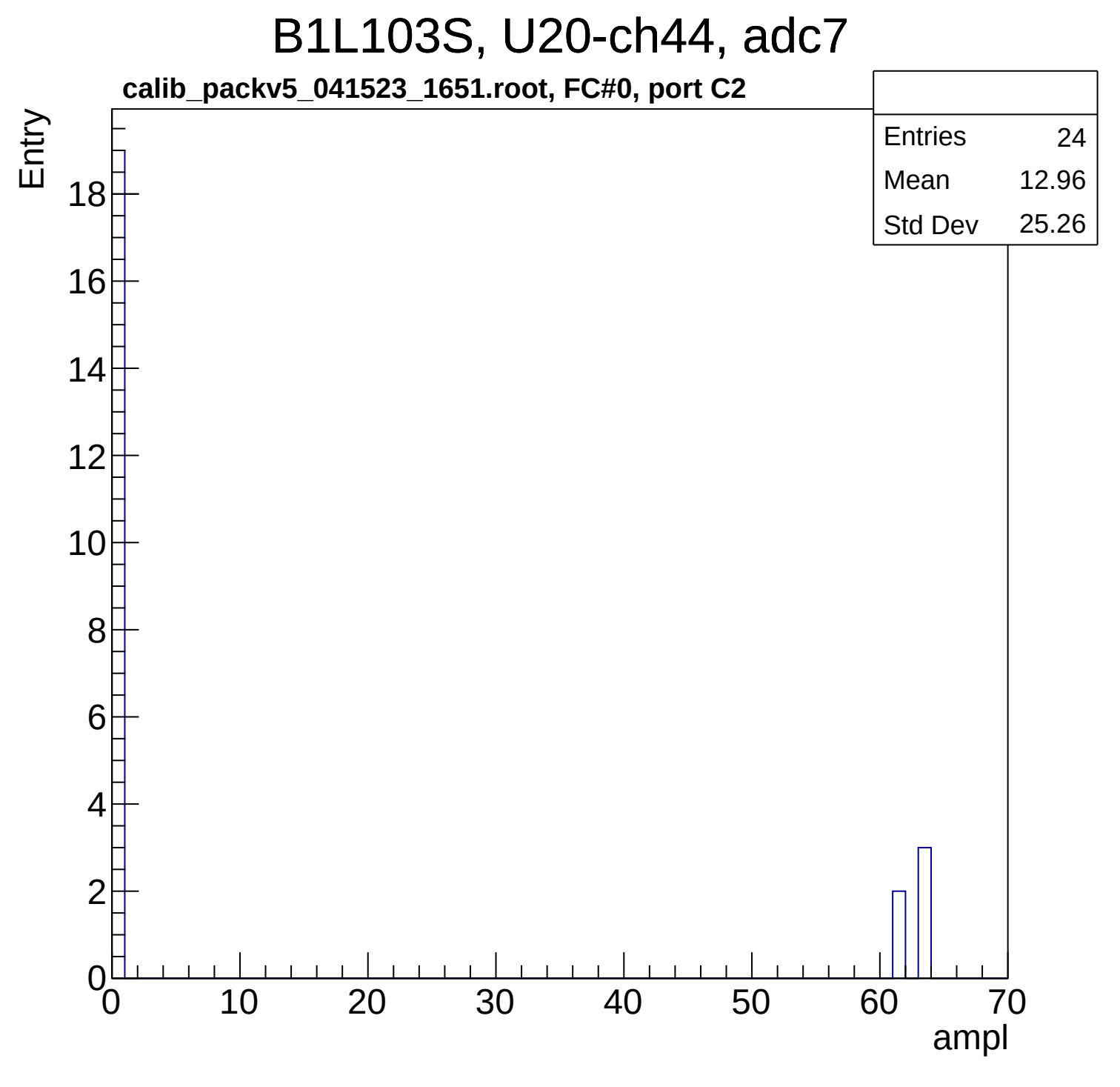
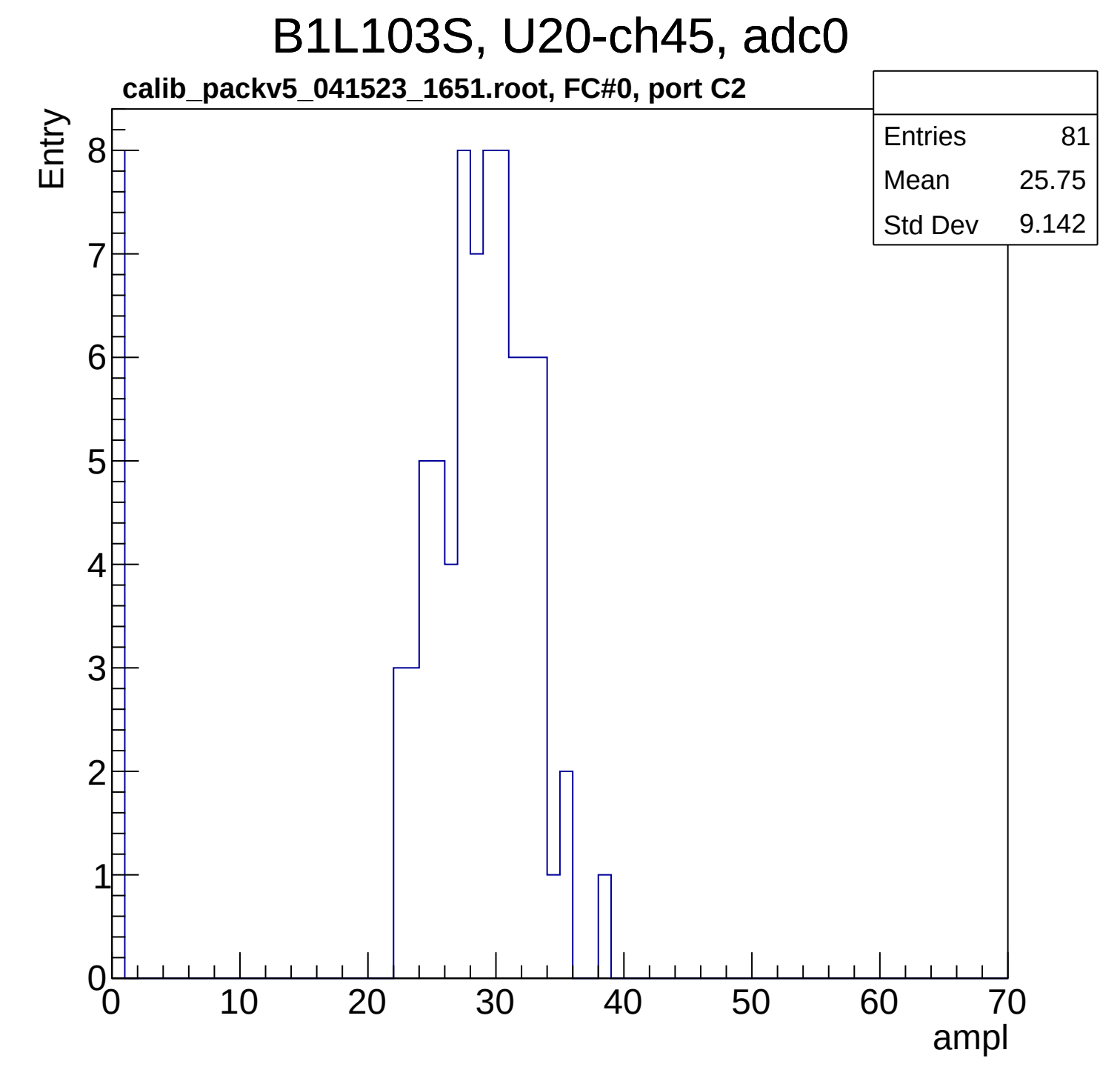
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch44, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 60.75
Std Dev 2.136
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U20-ch44, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 12.96
Std Dev 25.26
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch45, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 25.75
Std Dev 9.142
Entry
ampl
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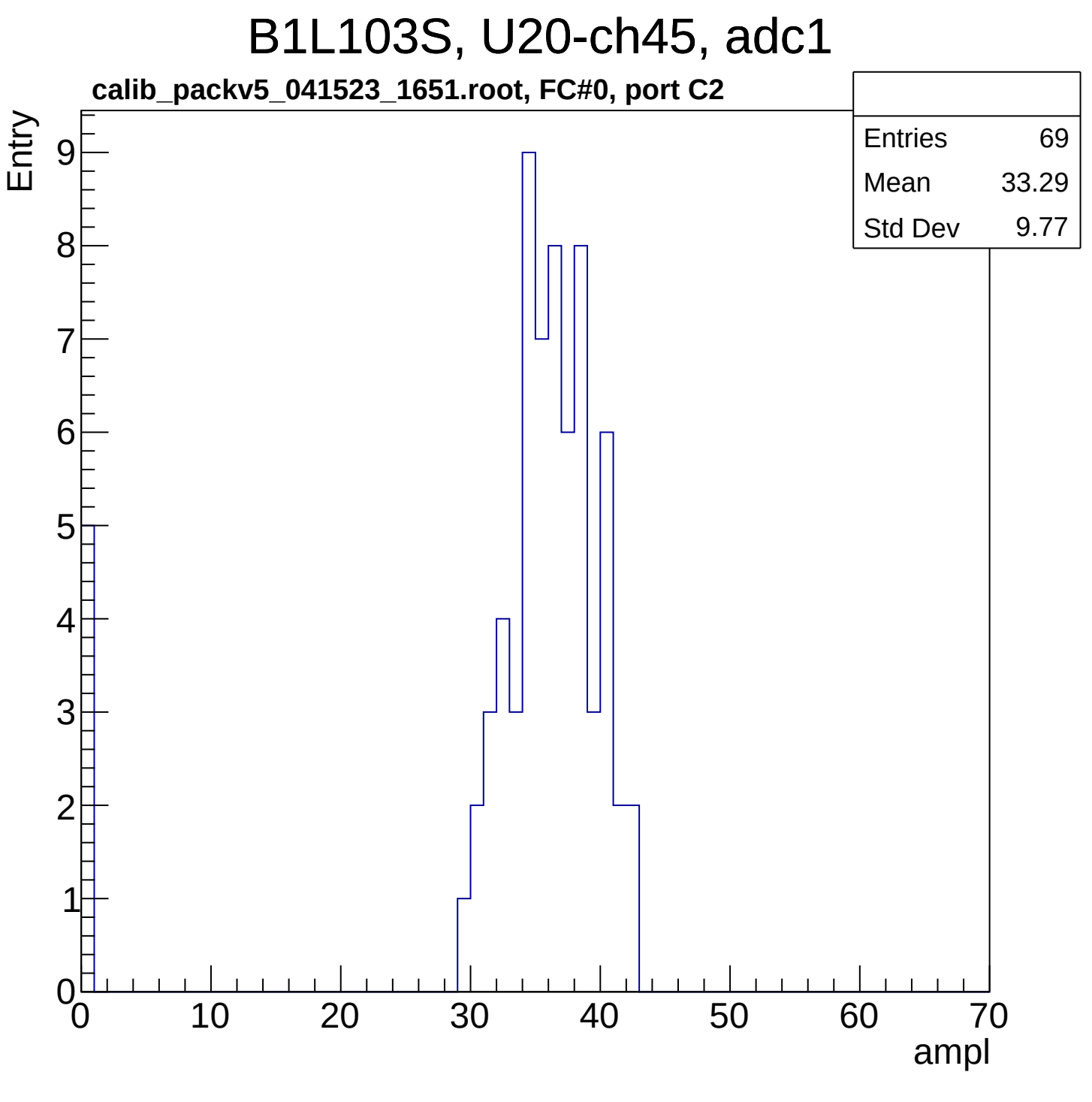
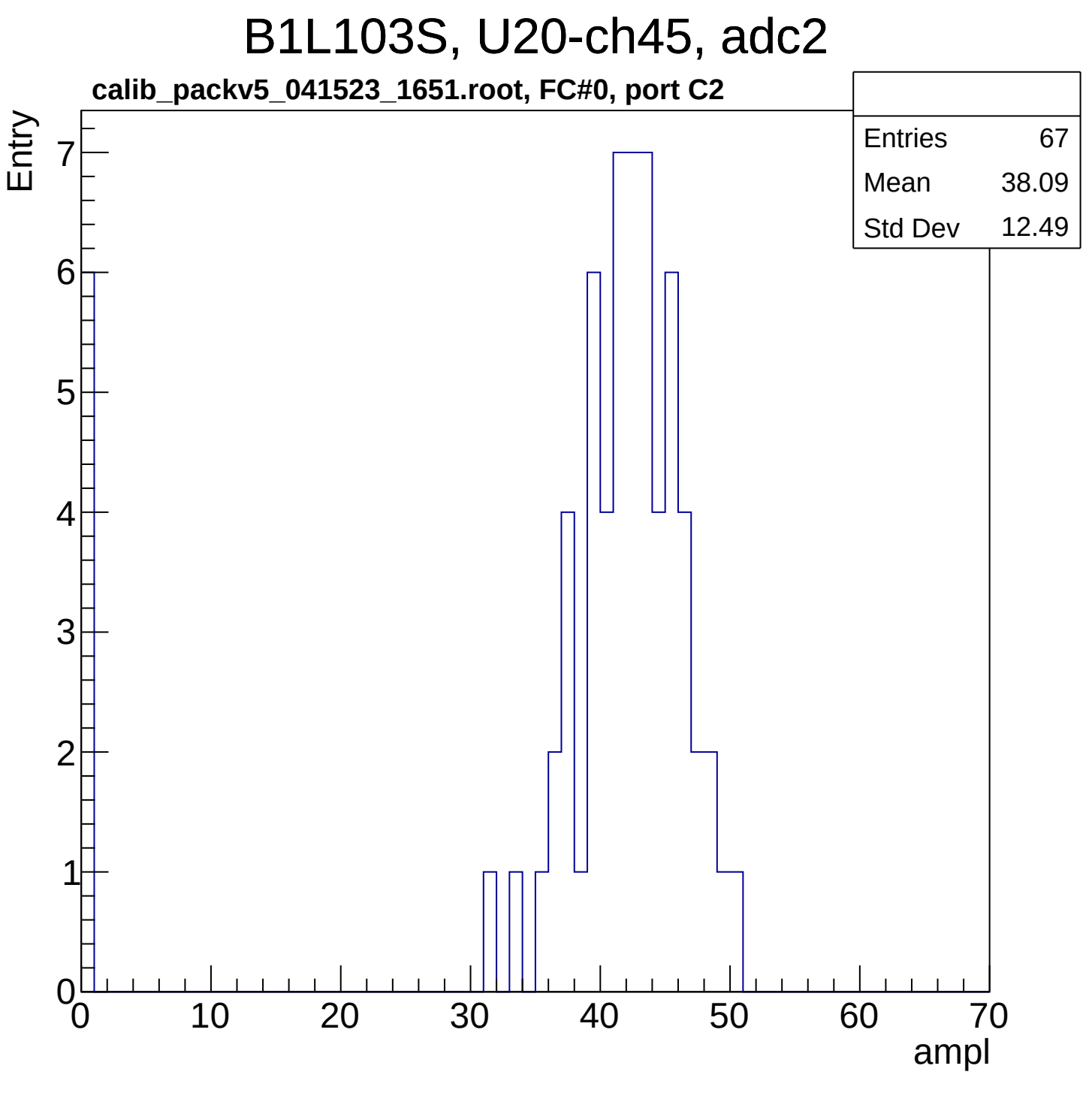
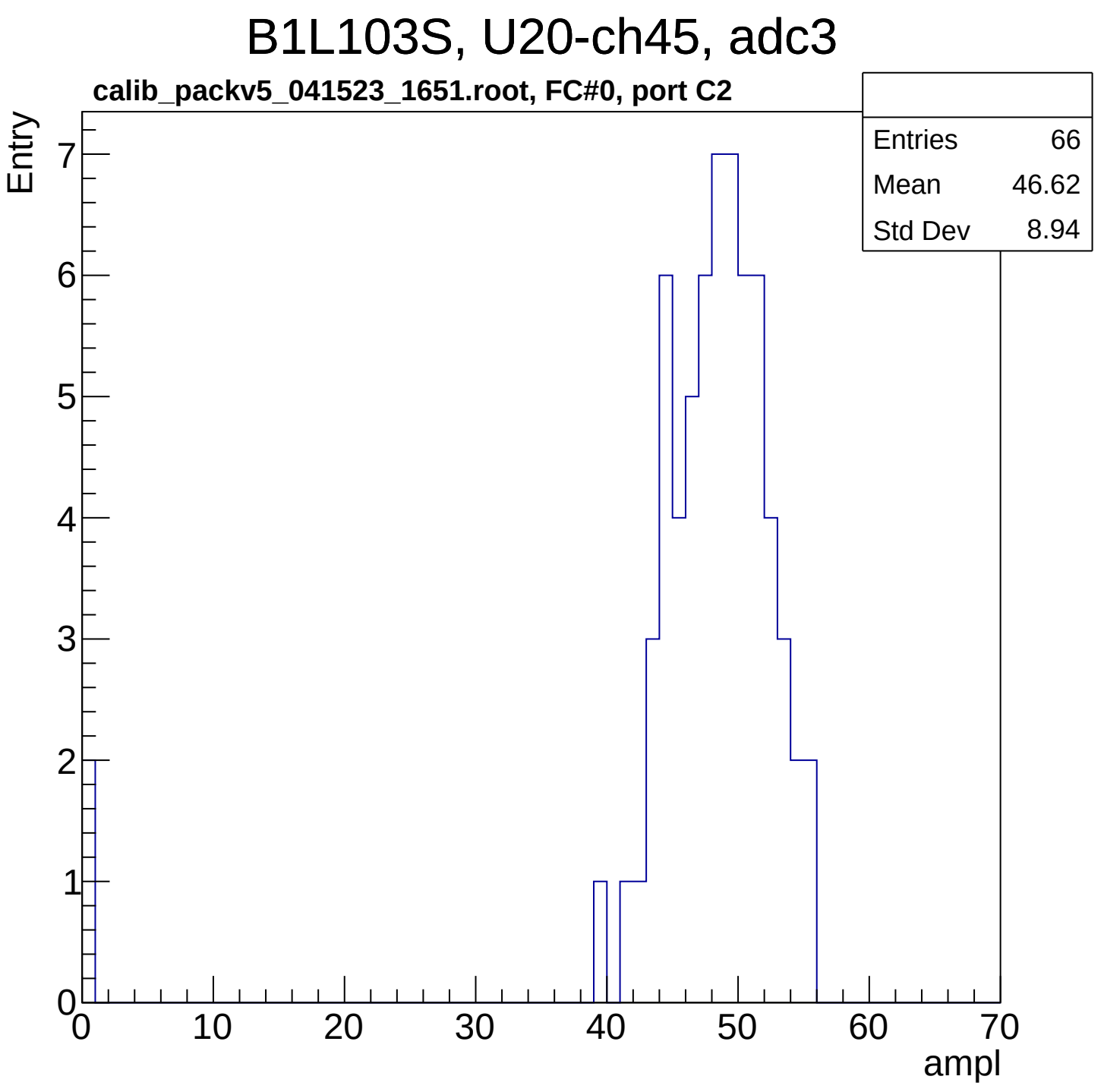
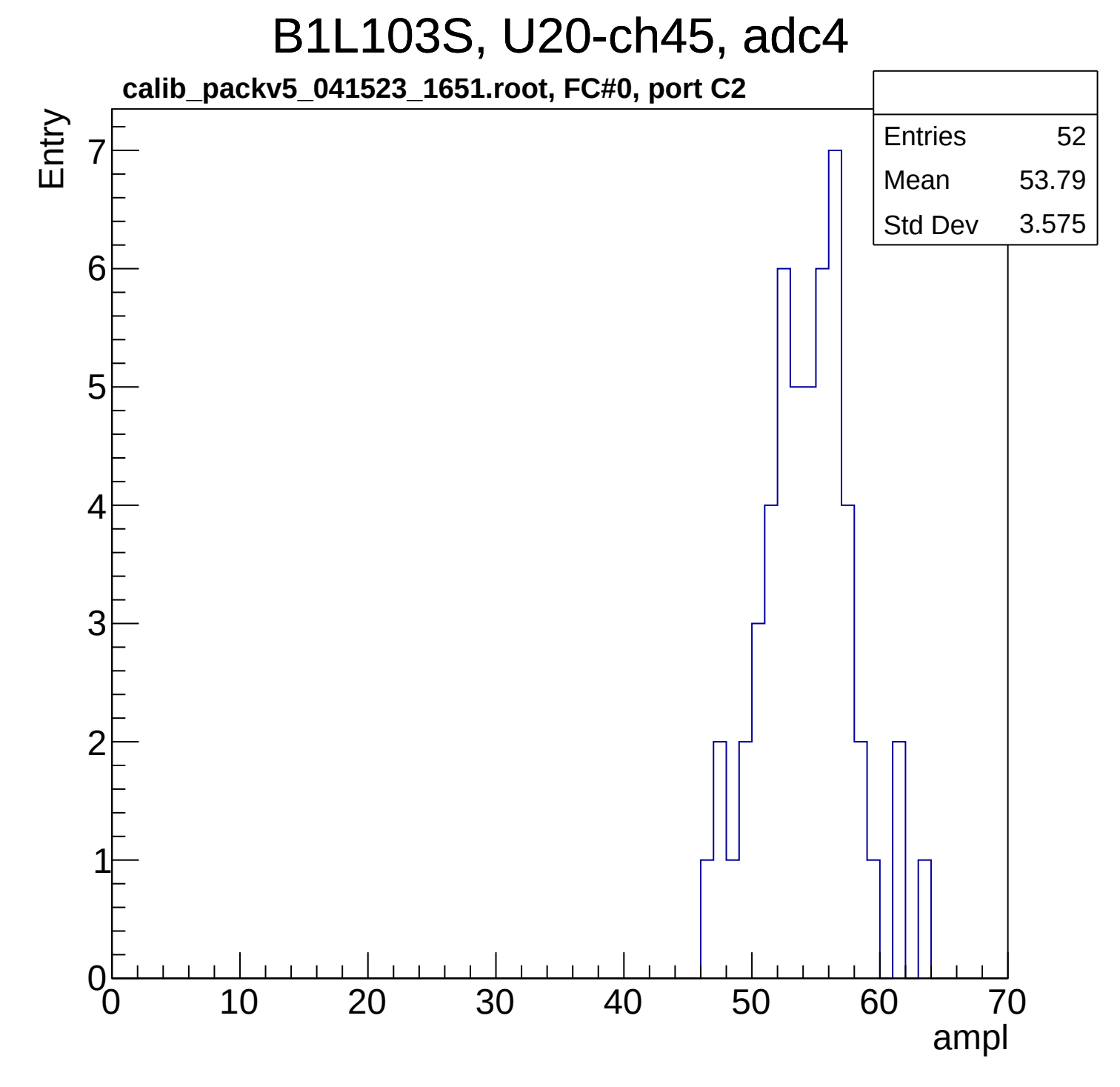
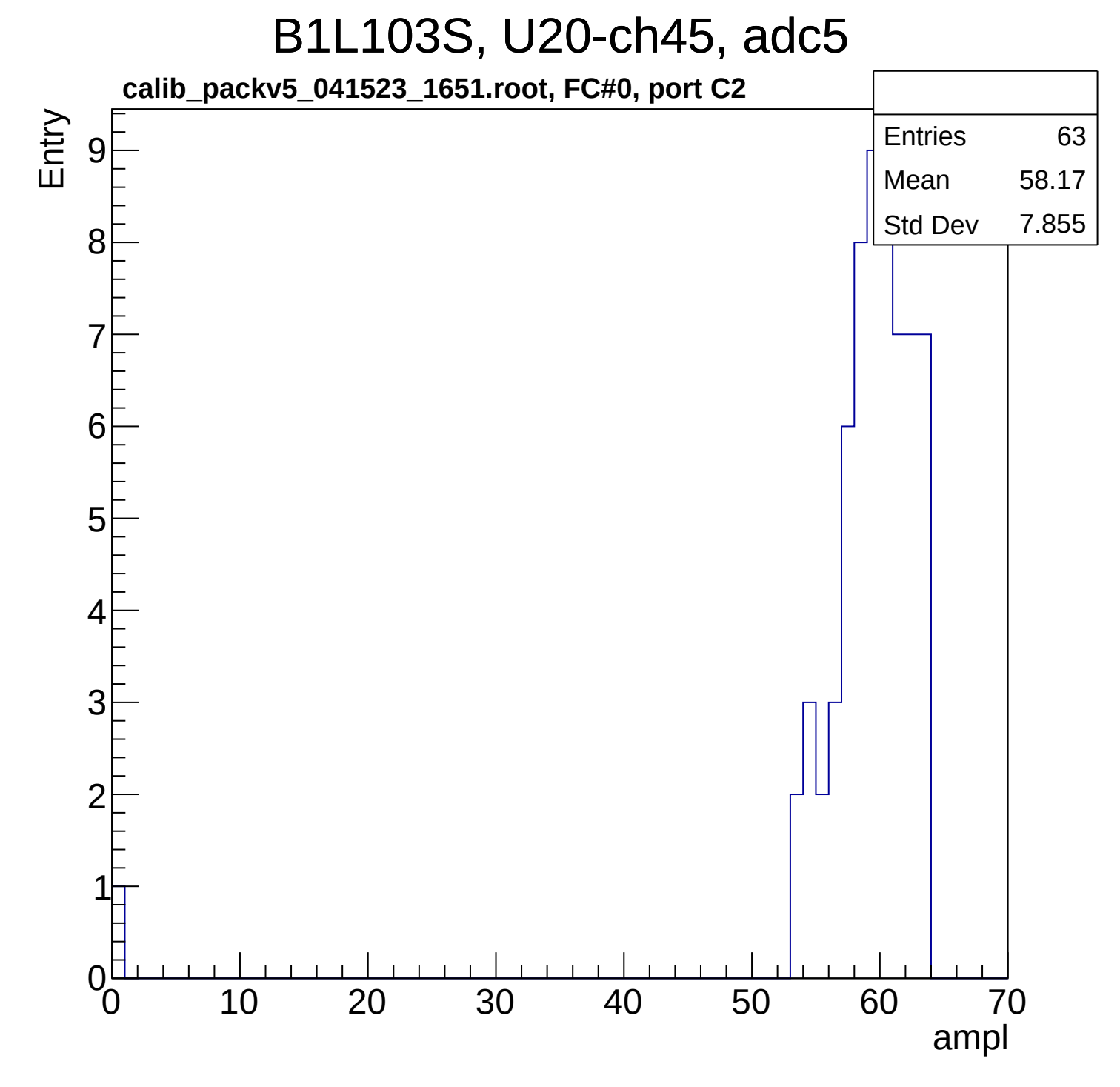
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch45, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 33.29
Std Dev 9.77
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch45, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 38.09
Std Dev 12.49
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U20-ch45, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 46.62
Std Dev 8.94
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U20-ch45, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 53.79
Std Dev 3.575
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U20-ch45, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 58.17
Std Dev 7.855
Entry
ampl
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2
3
4
5
6
7
8
9
0
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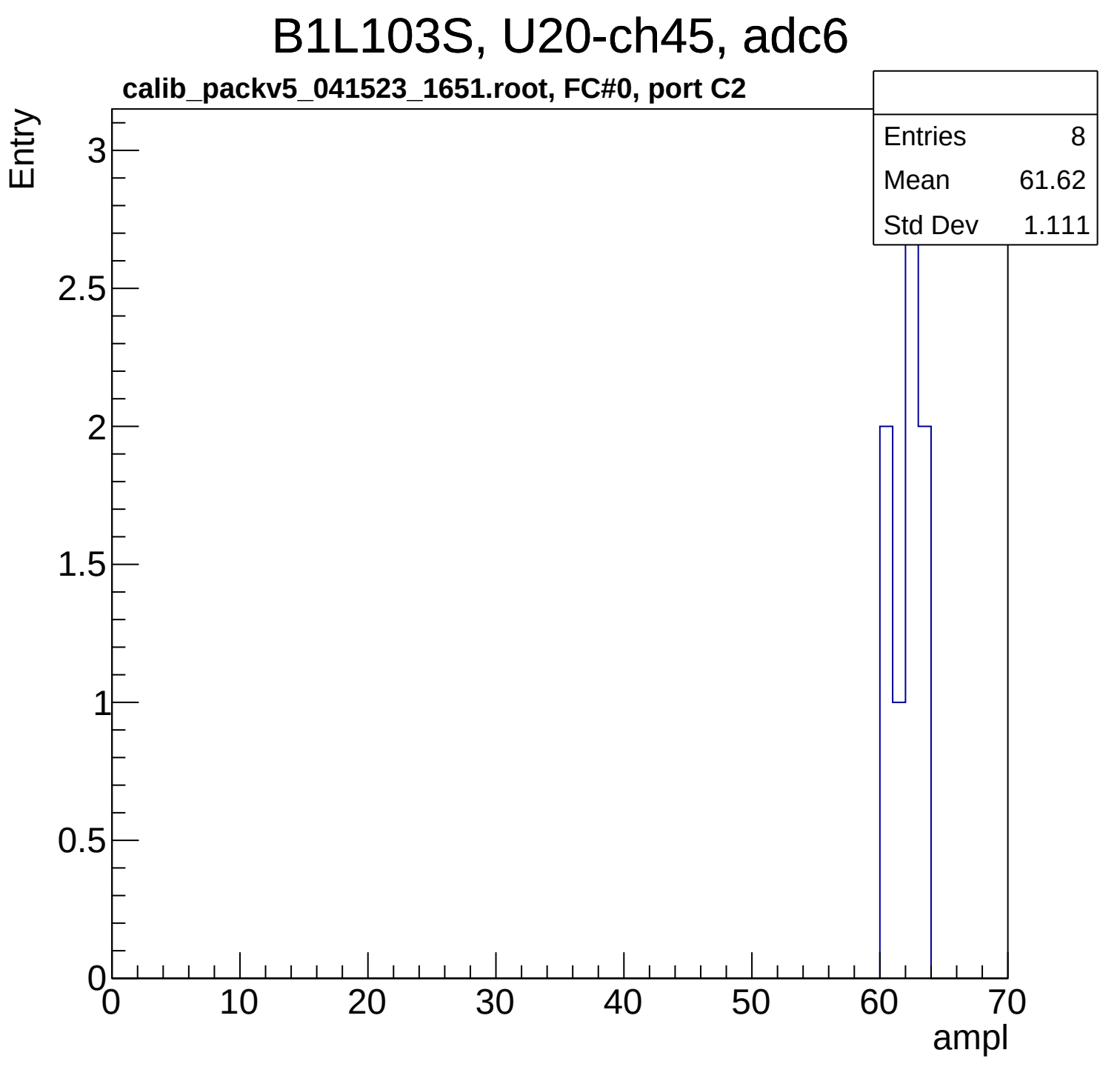
20
30
40
50
60
70


B1L103S, U20-ch45, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 61.62
Std Dev 1.111
Entry
ampl
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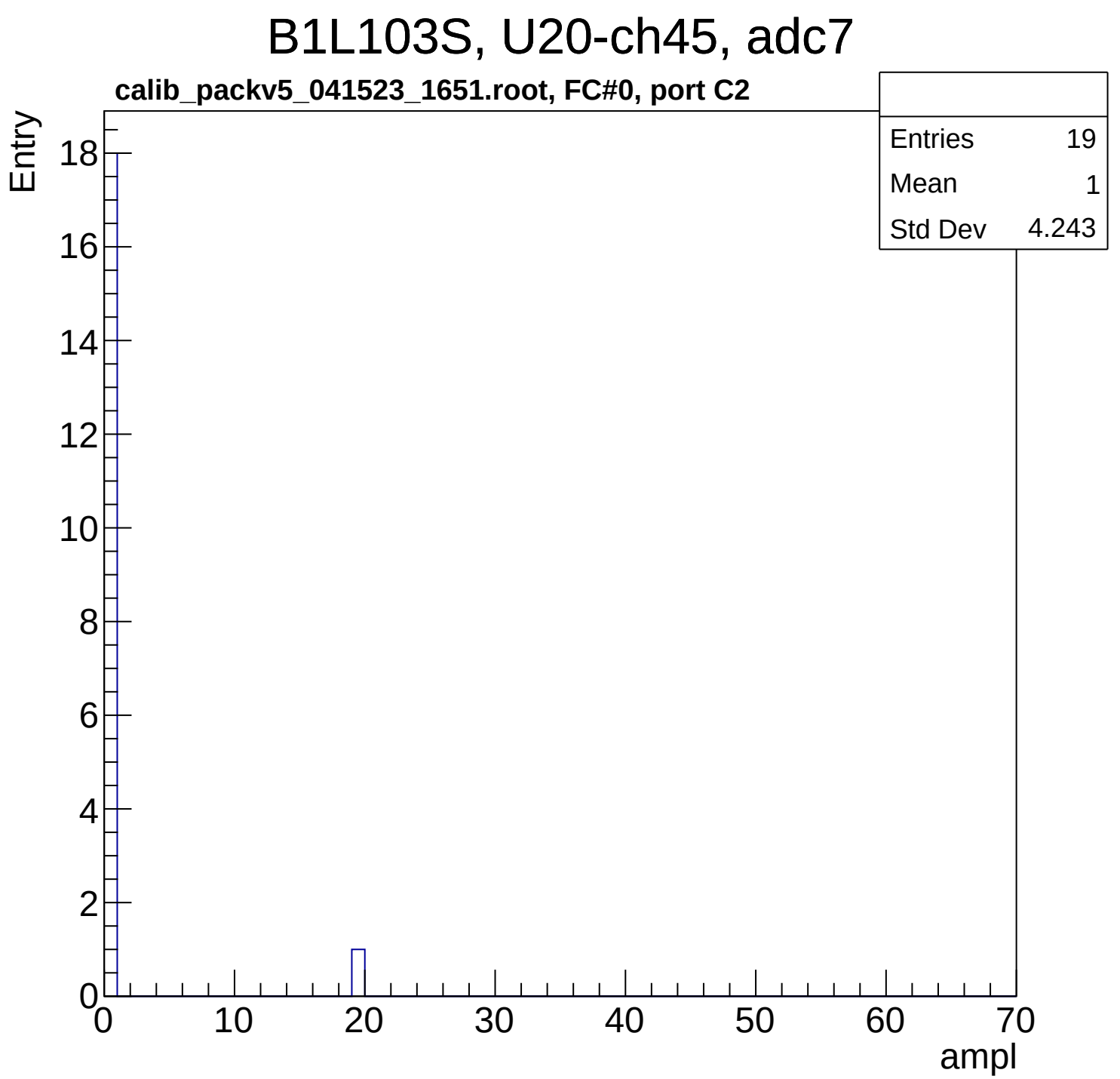
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U20-ch45, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1
Std Dev 4.243
Entry
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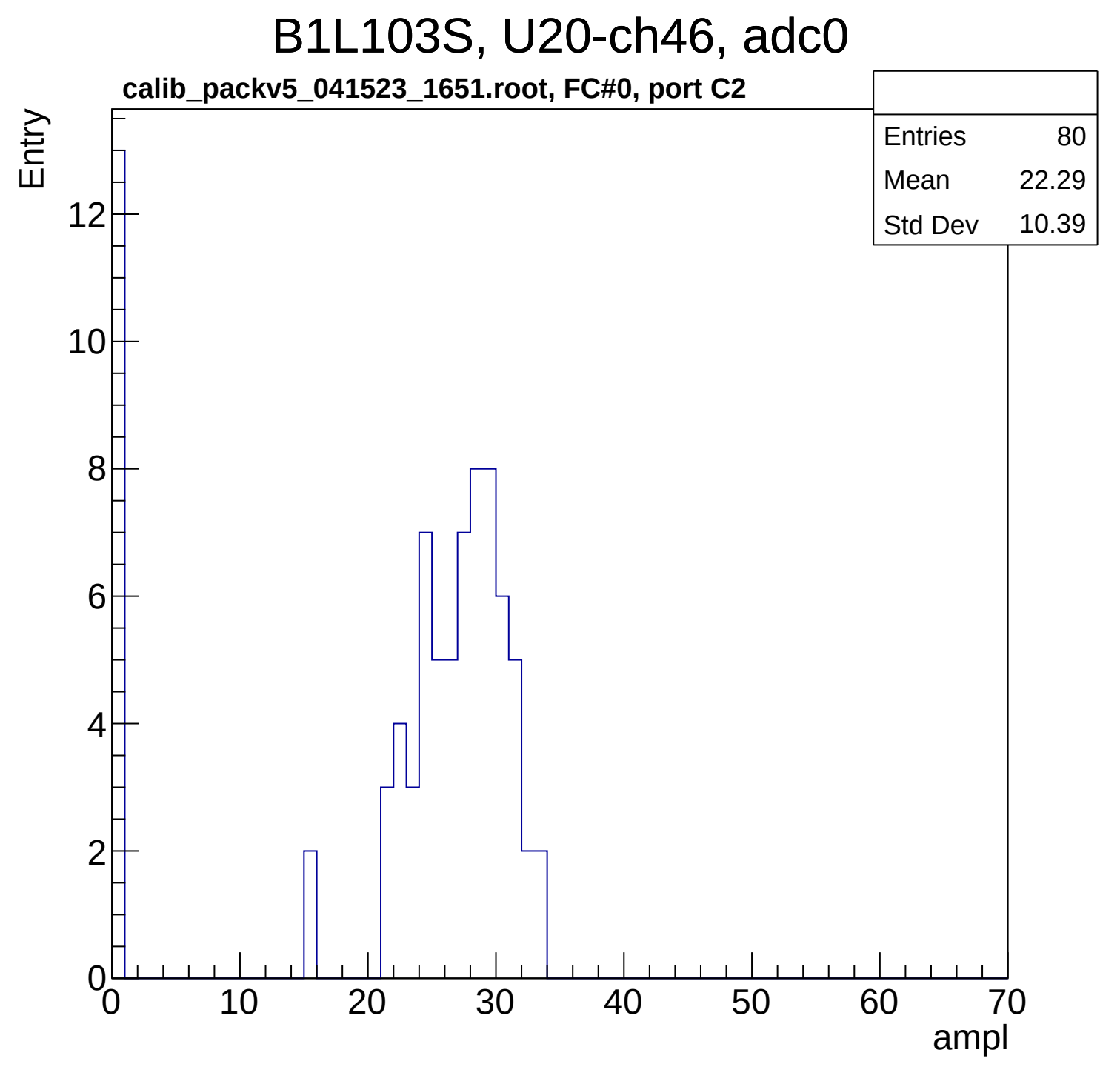
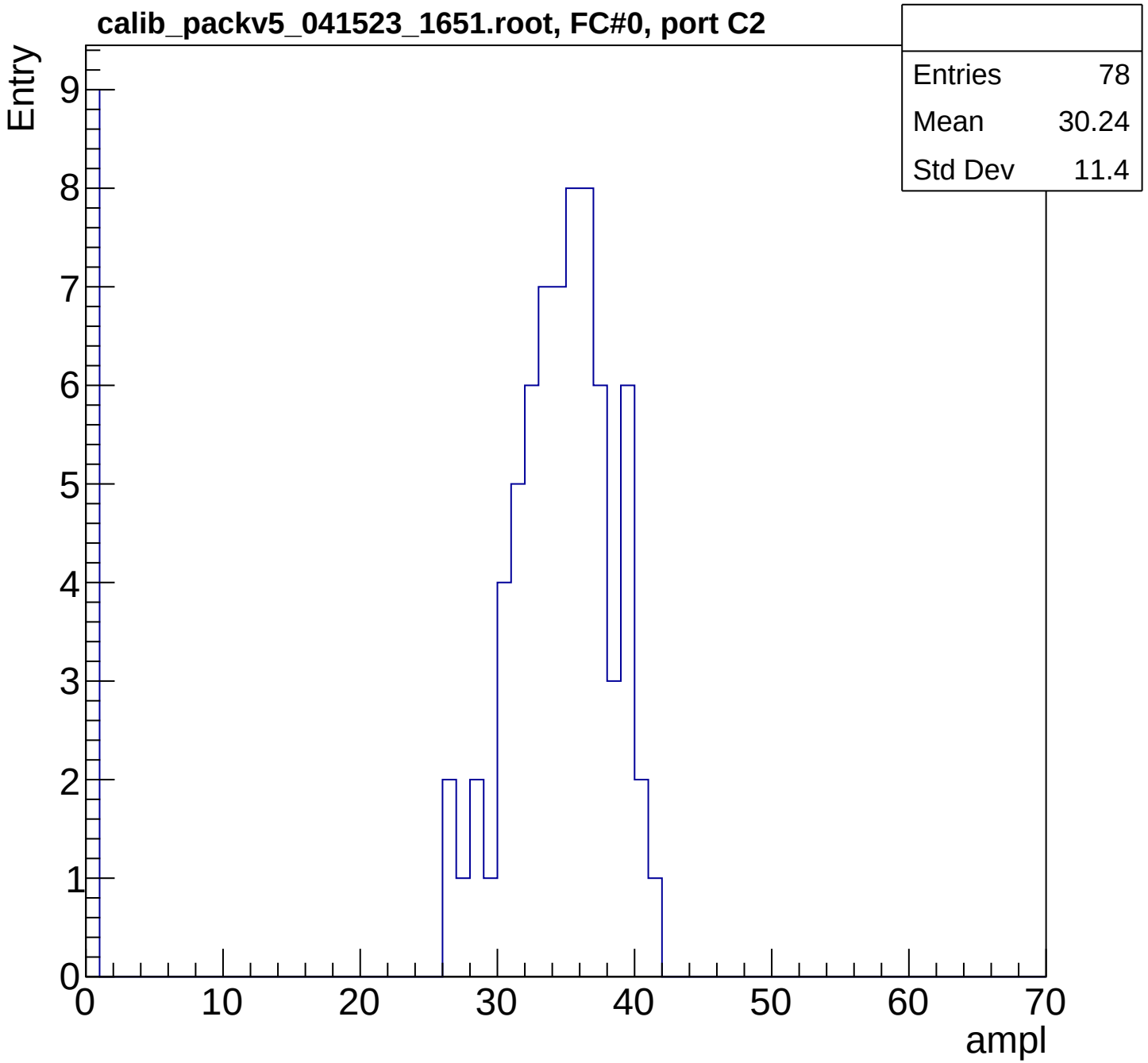
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch46, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 22.29
Std Dev 10.39
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch46, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 30.24
Std Dev 11.4
Entry
ampl
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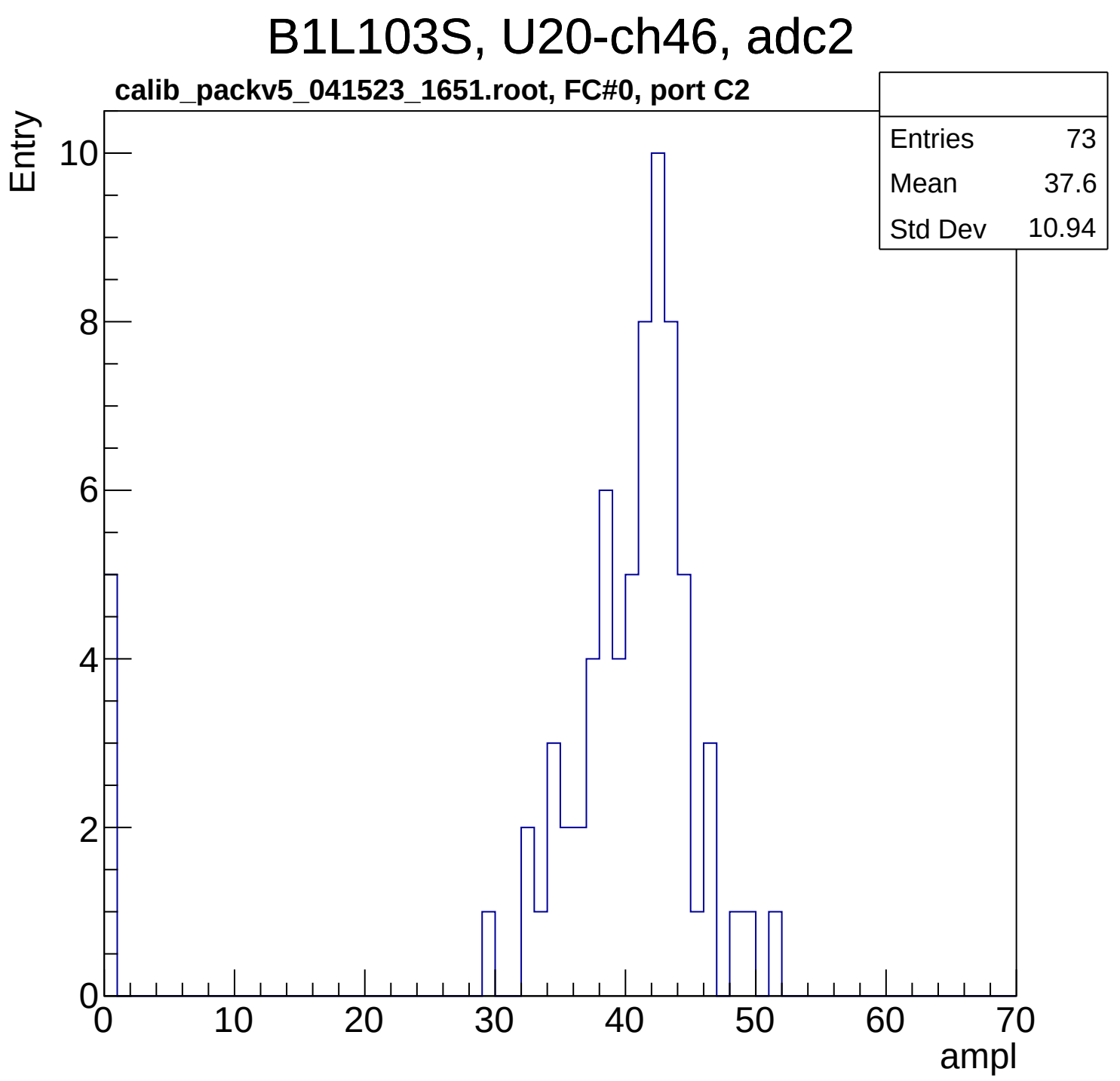
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch46, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 37.6
Std Dev 10.94
Entry
ampl
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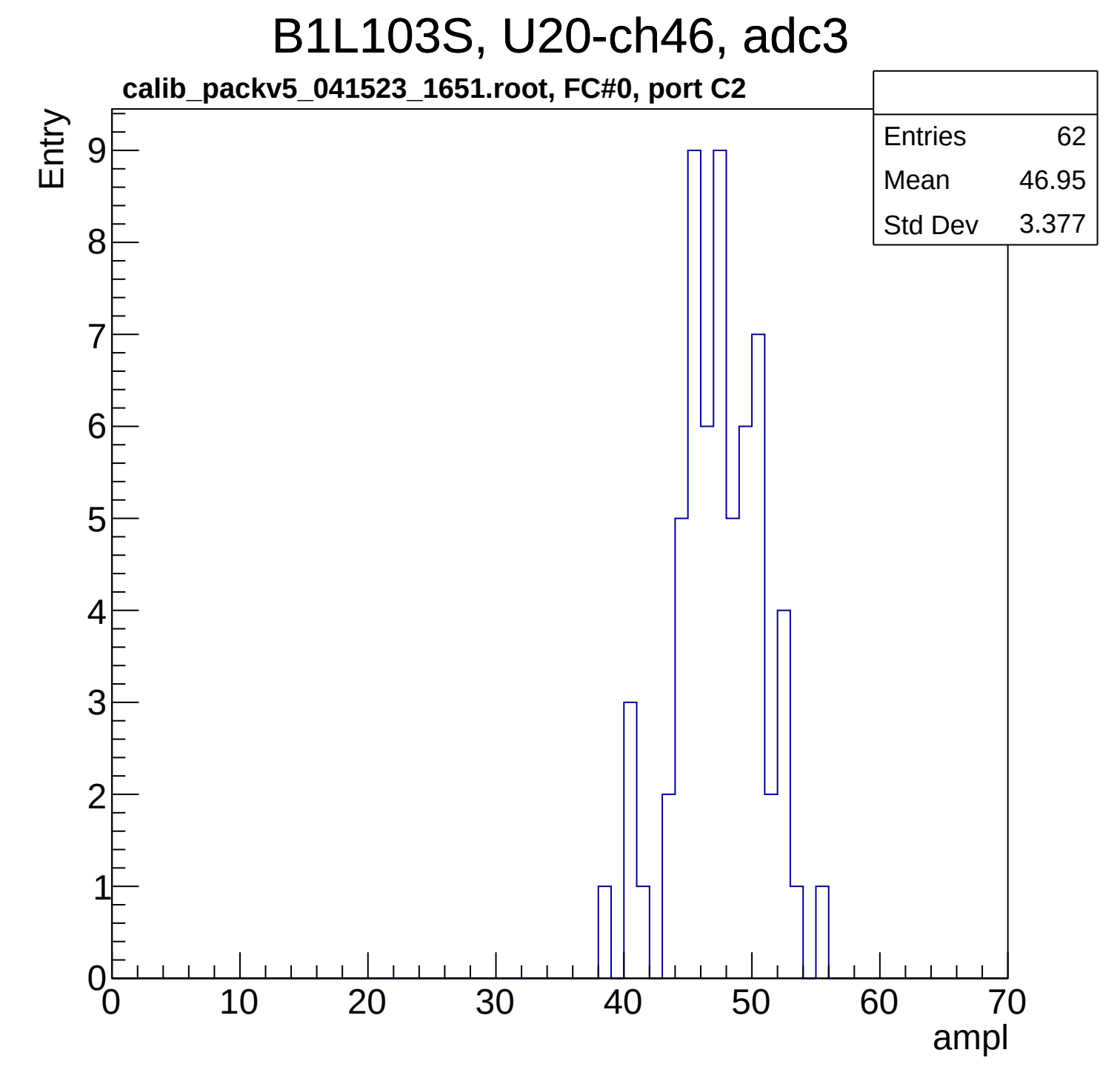
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U20-ch46, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 46.95
Std Dev 3.377
Entry
ampl
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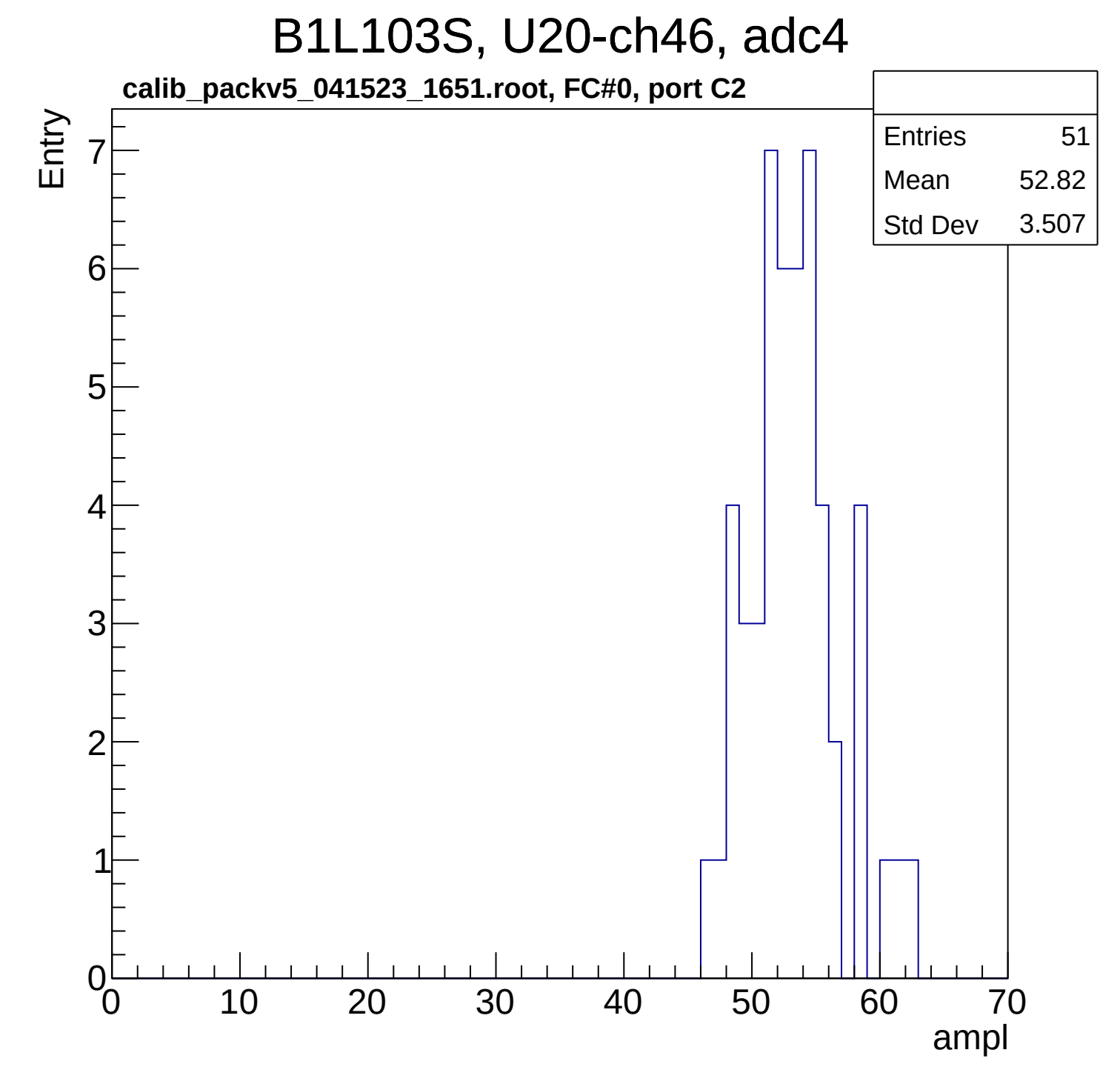
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch46, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 52.82
Std Dev 3.507
Entry
ampl
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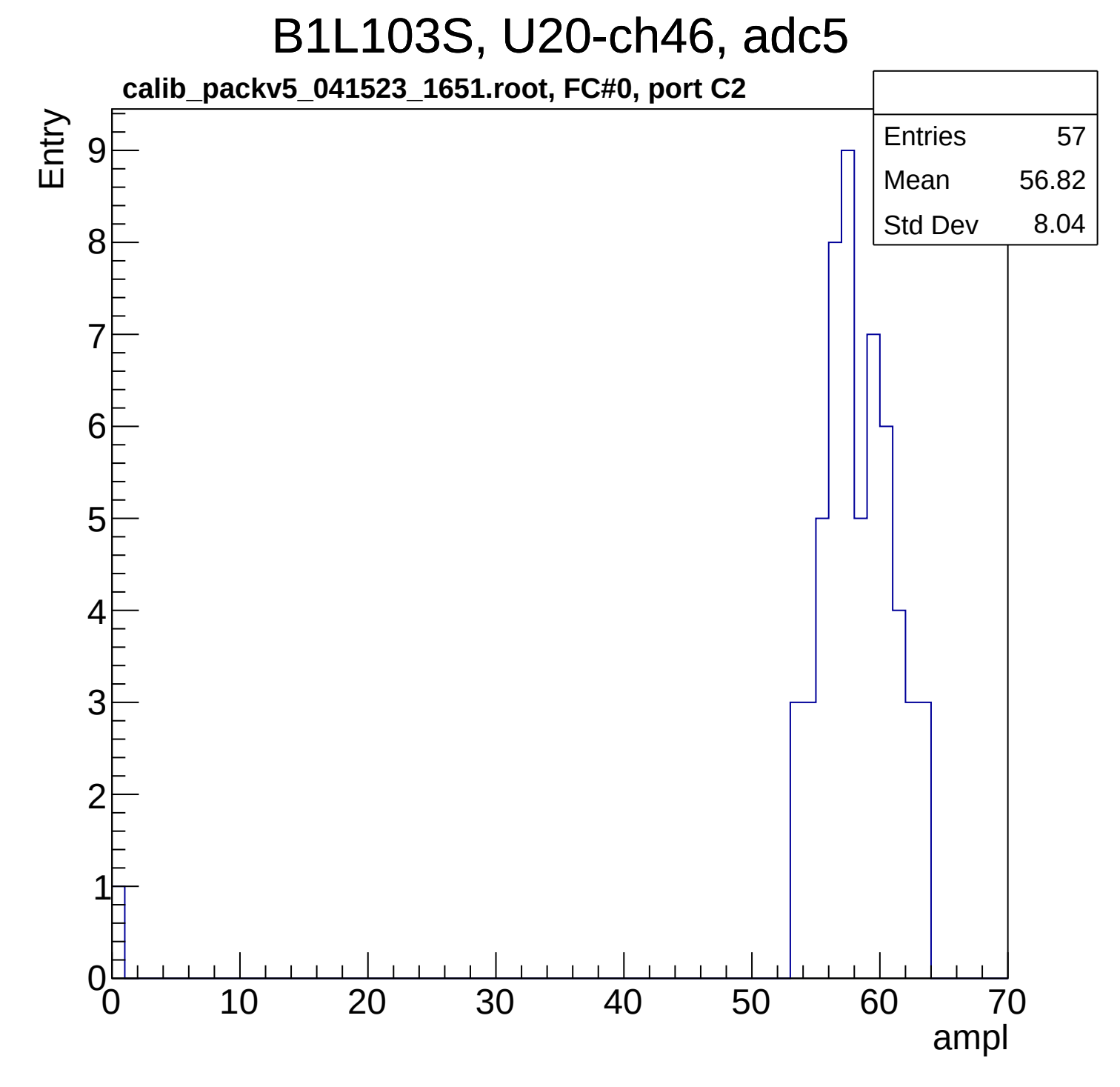
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U20-ch46, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 56.82
Std Dev 8.04
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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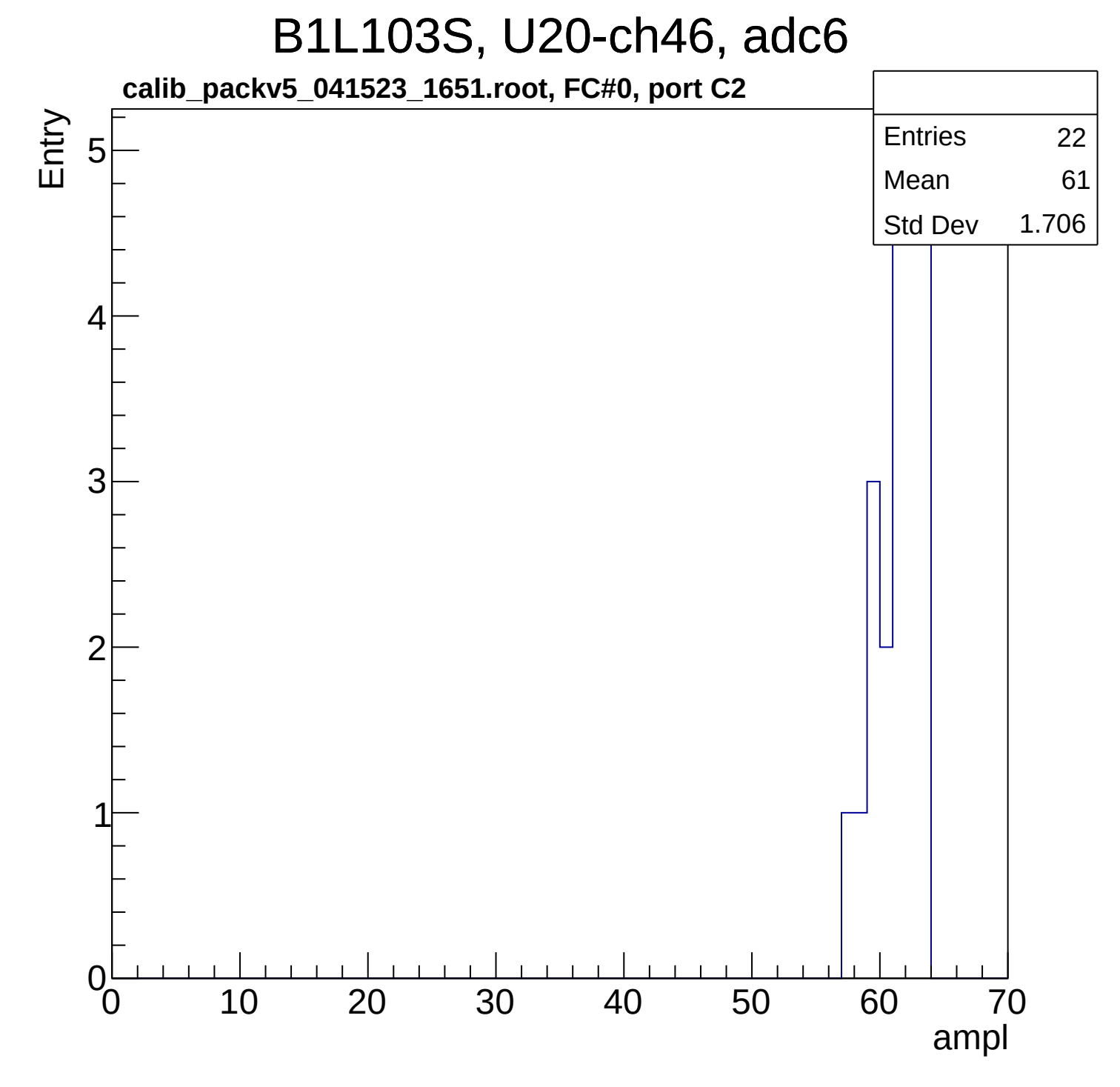
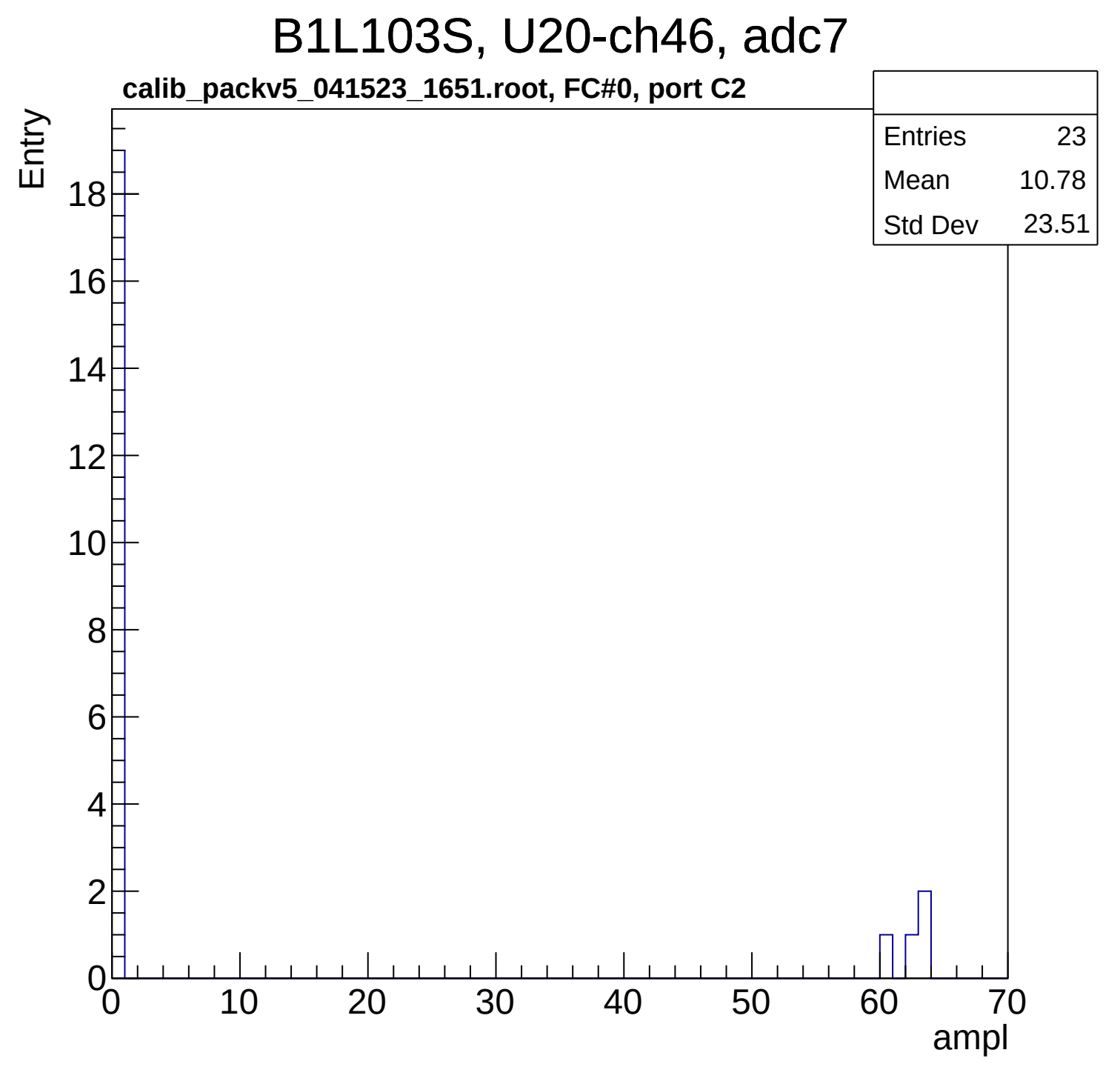
40
50
60
70


B1L103S, U20-ch46, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 61
Std Dev 1.706
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U20-ch46, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 10.78
Std Dev 23.51
Entry
0
2
4
6
8
10
12
14
16
18
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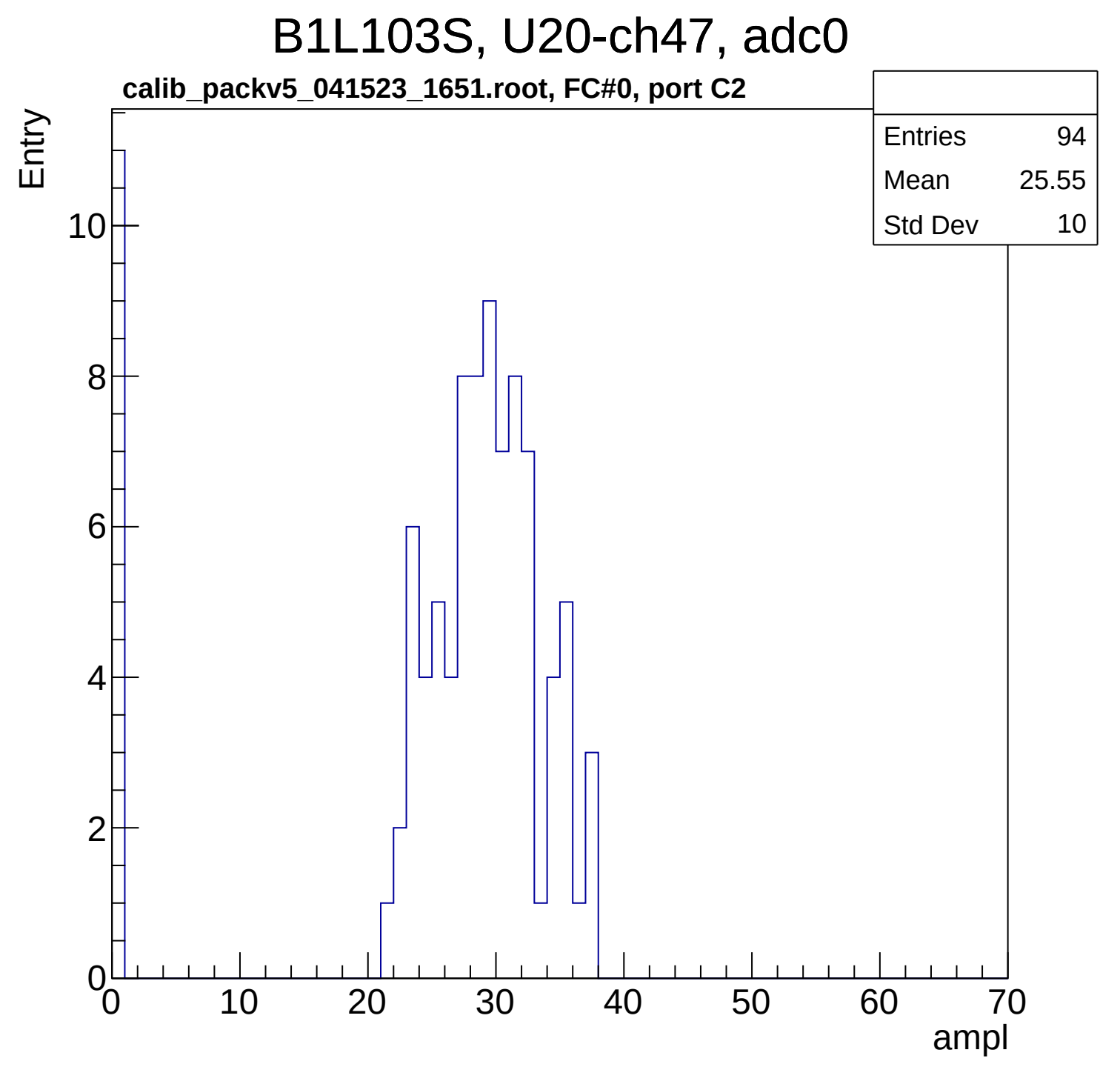
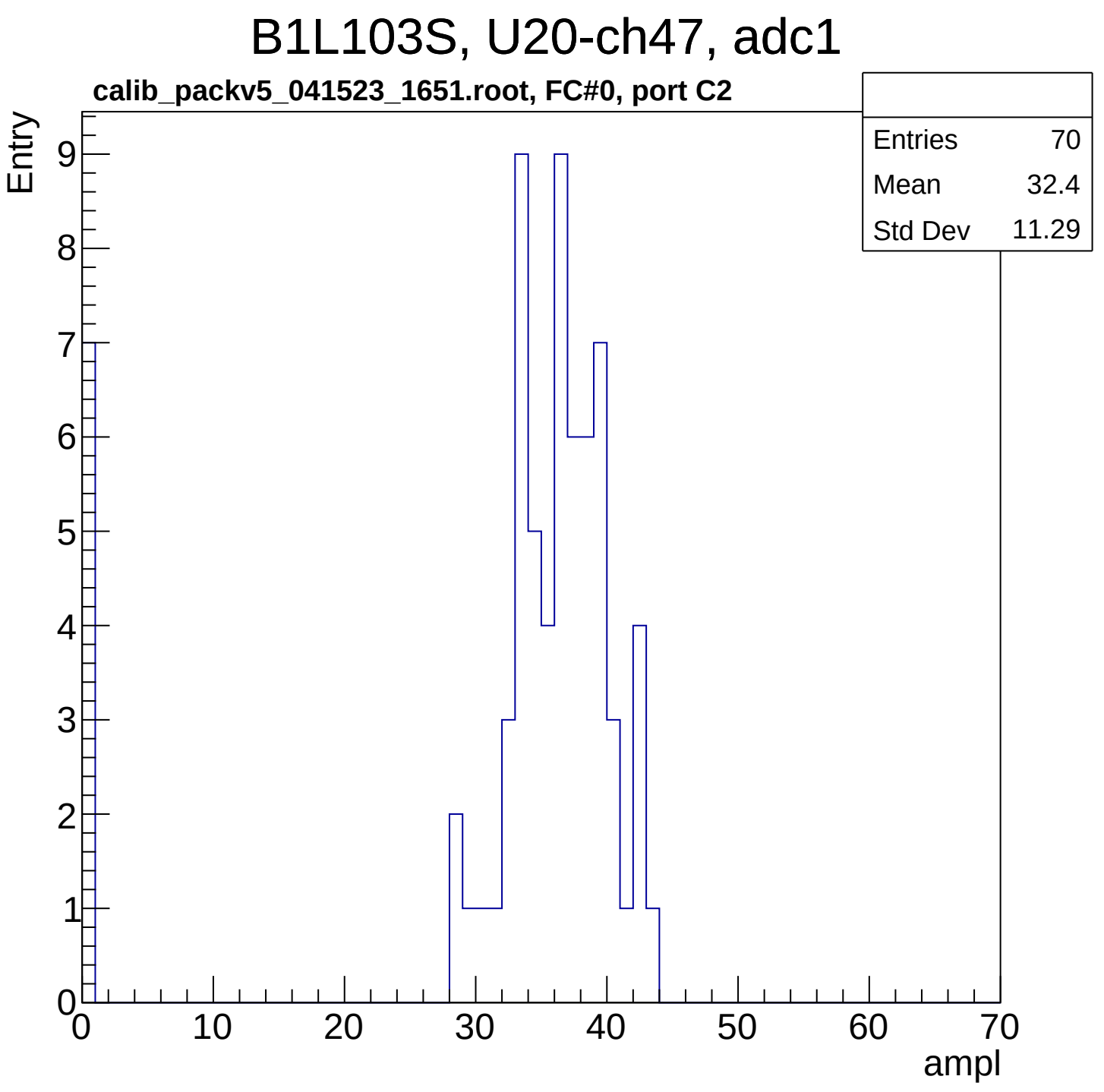
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch47, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 25.55
Std Dev 10
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U20-ch47, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 32.4
Std Dev 11.29
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
10
20
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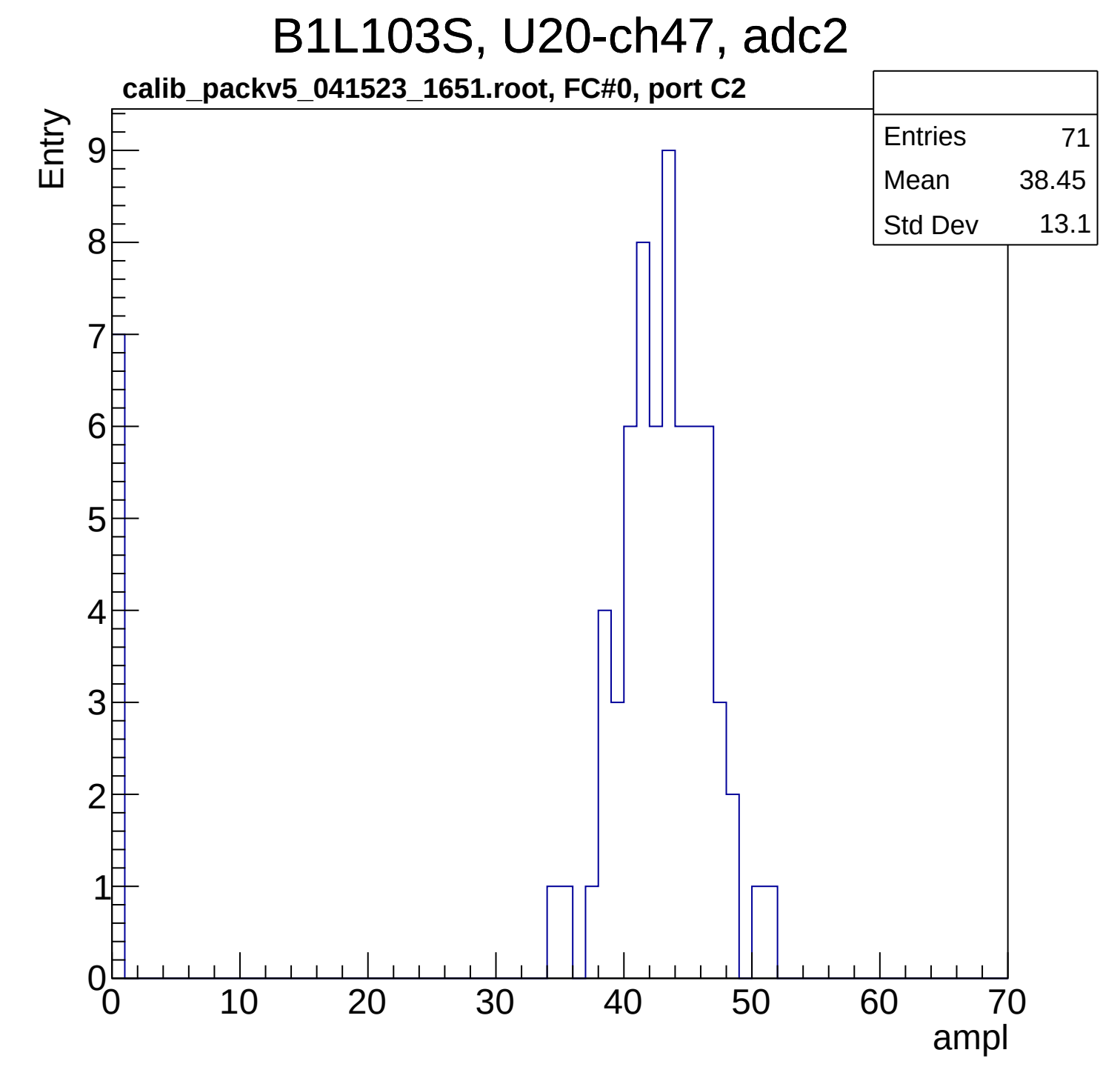
40
50
60
70


B1L103S, U20-ch47, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 38.45
Std Dev 13.1
Entry
ampl
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2
3
4
5
6
7
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40
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60
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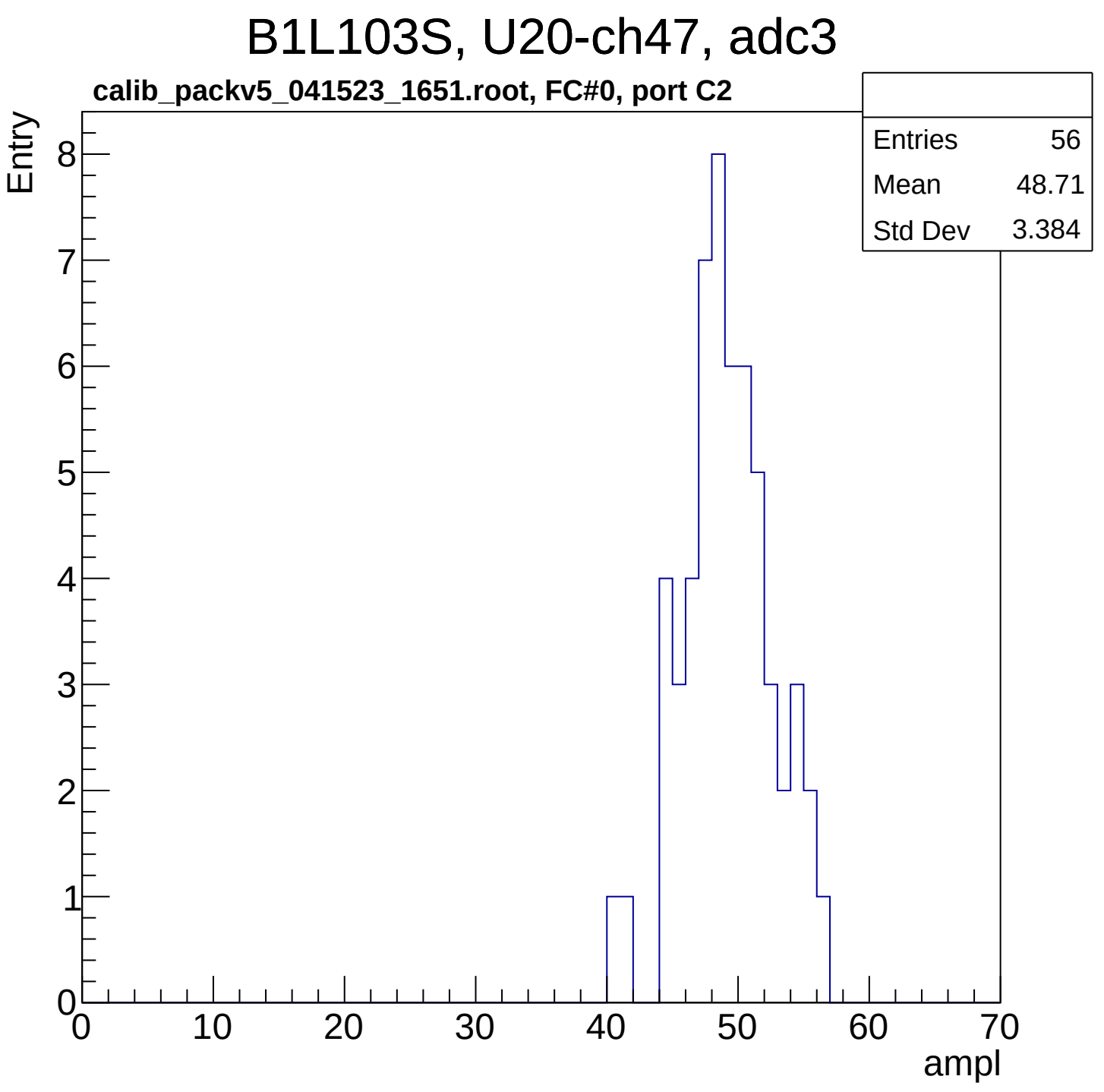
B1L103S, U20-ch47, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 48.71
Std Dev 3.384
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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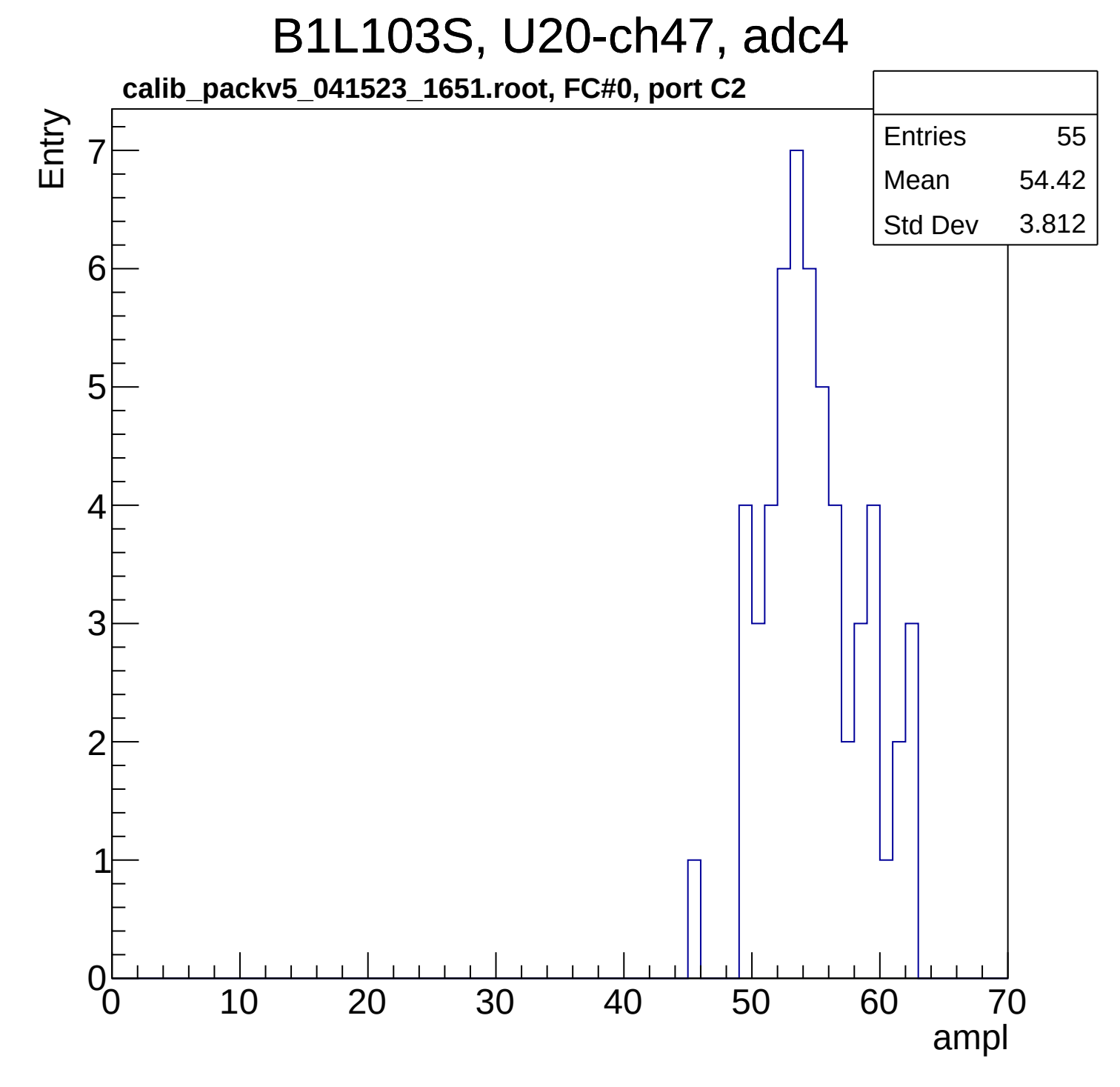
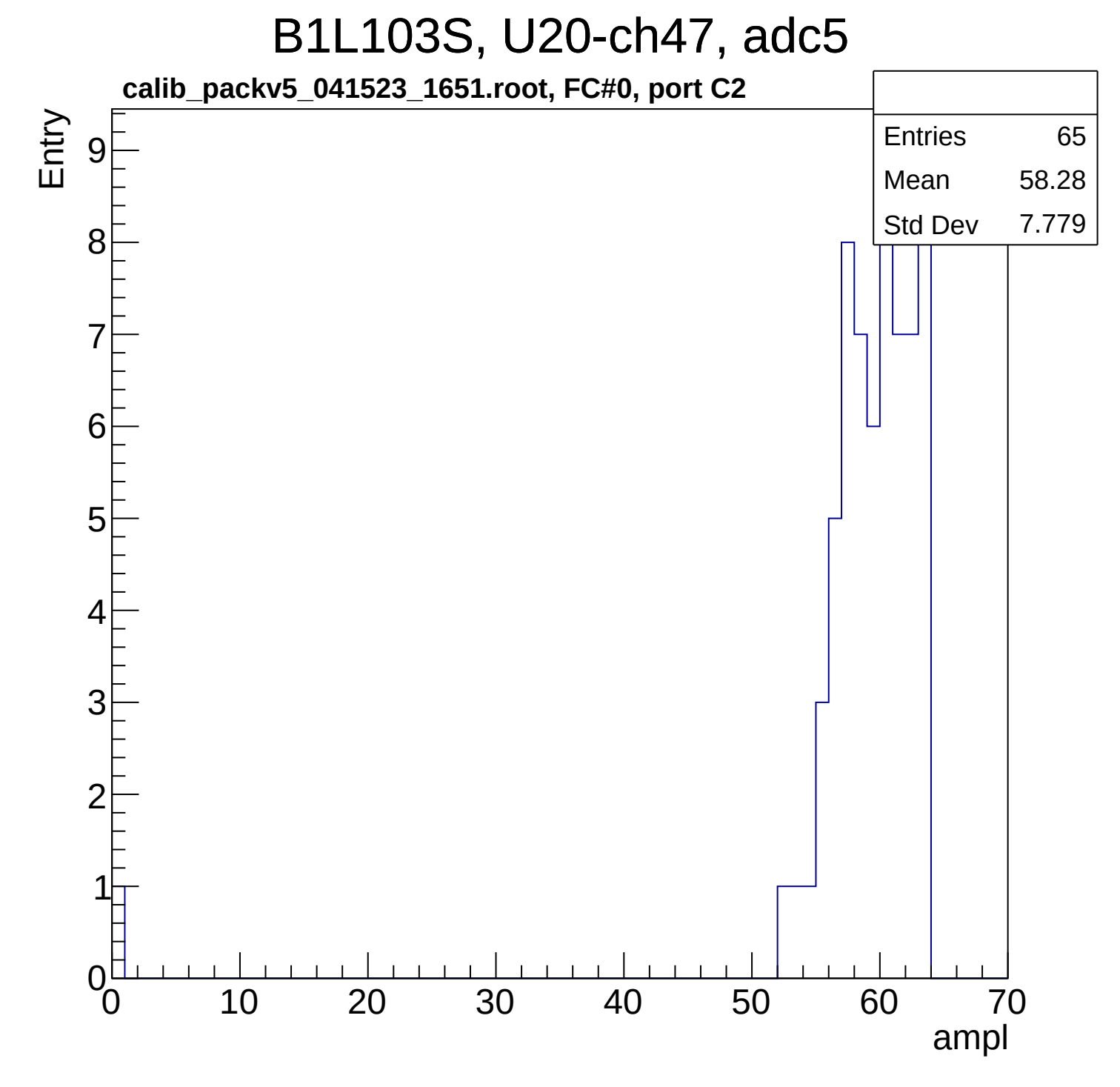

B1L103S, U20-ch47, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 54.42
Std Dev 3.812
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U20-ch47, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 58.28
Std Dev 7.779
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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20
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40
50
60
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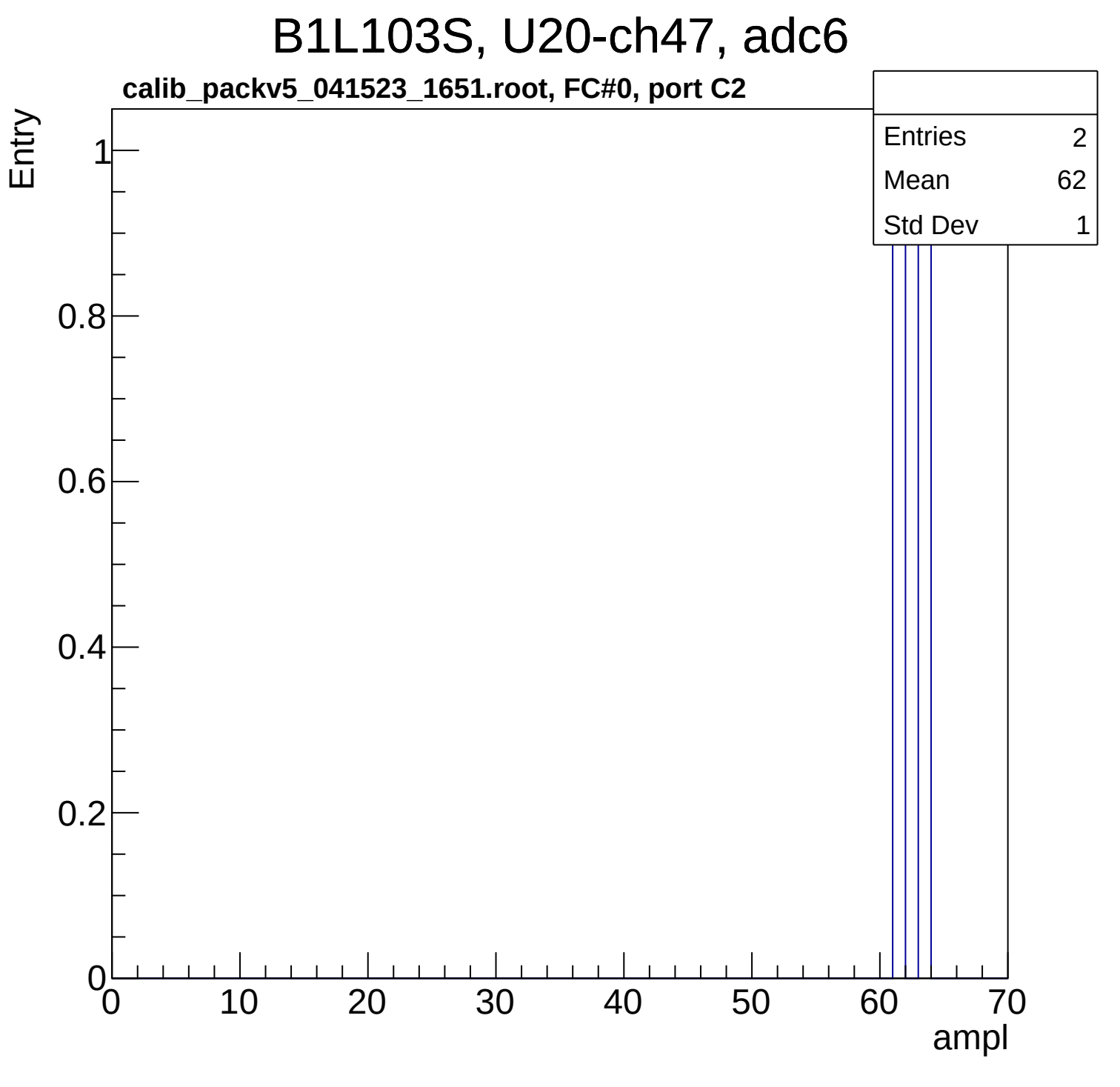
B1L103S, U20-ch47, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 62
Std Dev 1
Entry
ampl
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0.2
0.4
0.6
0.8
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0
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40
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60
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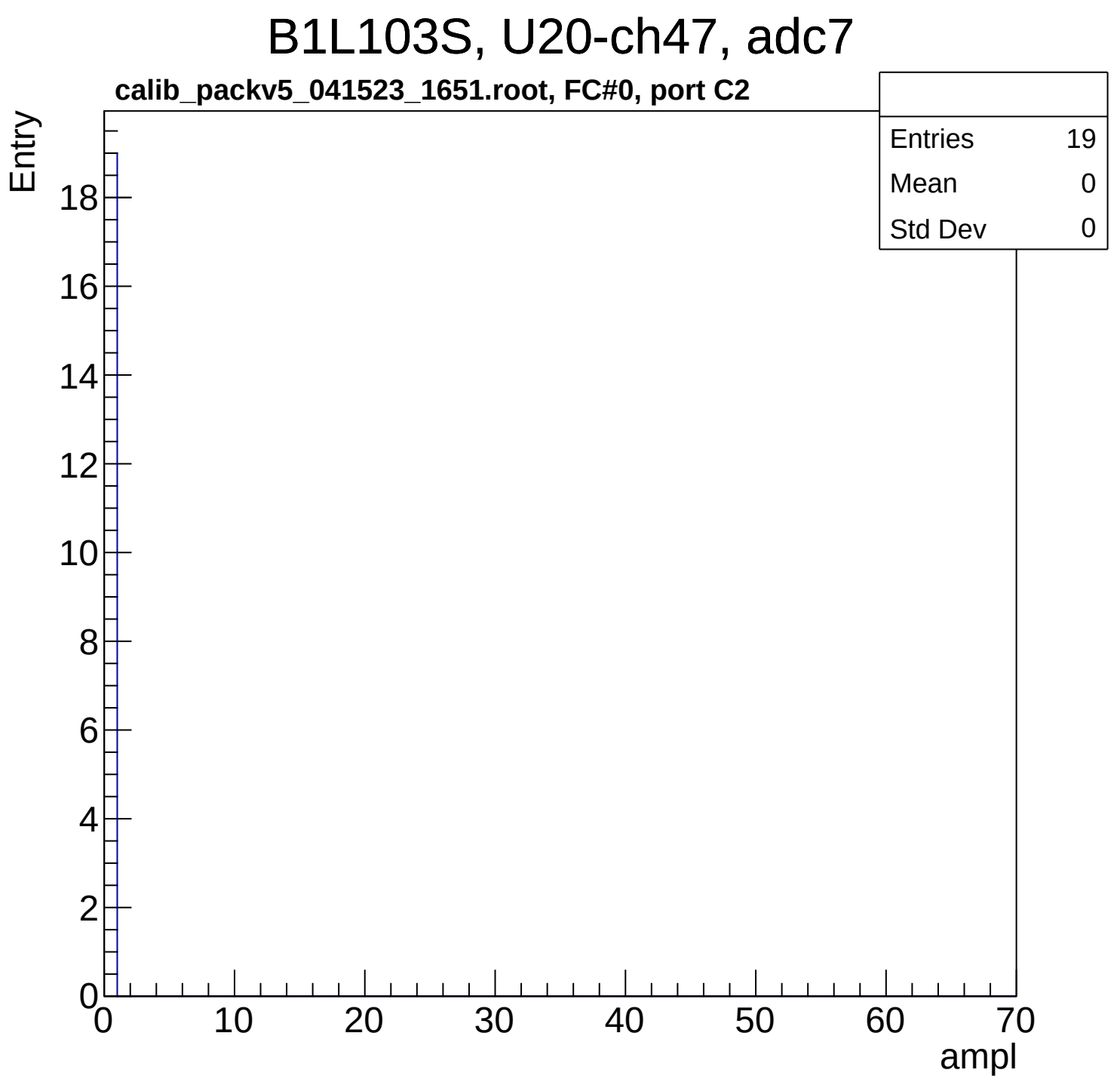
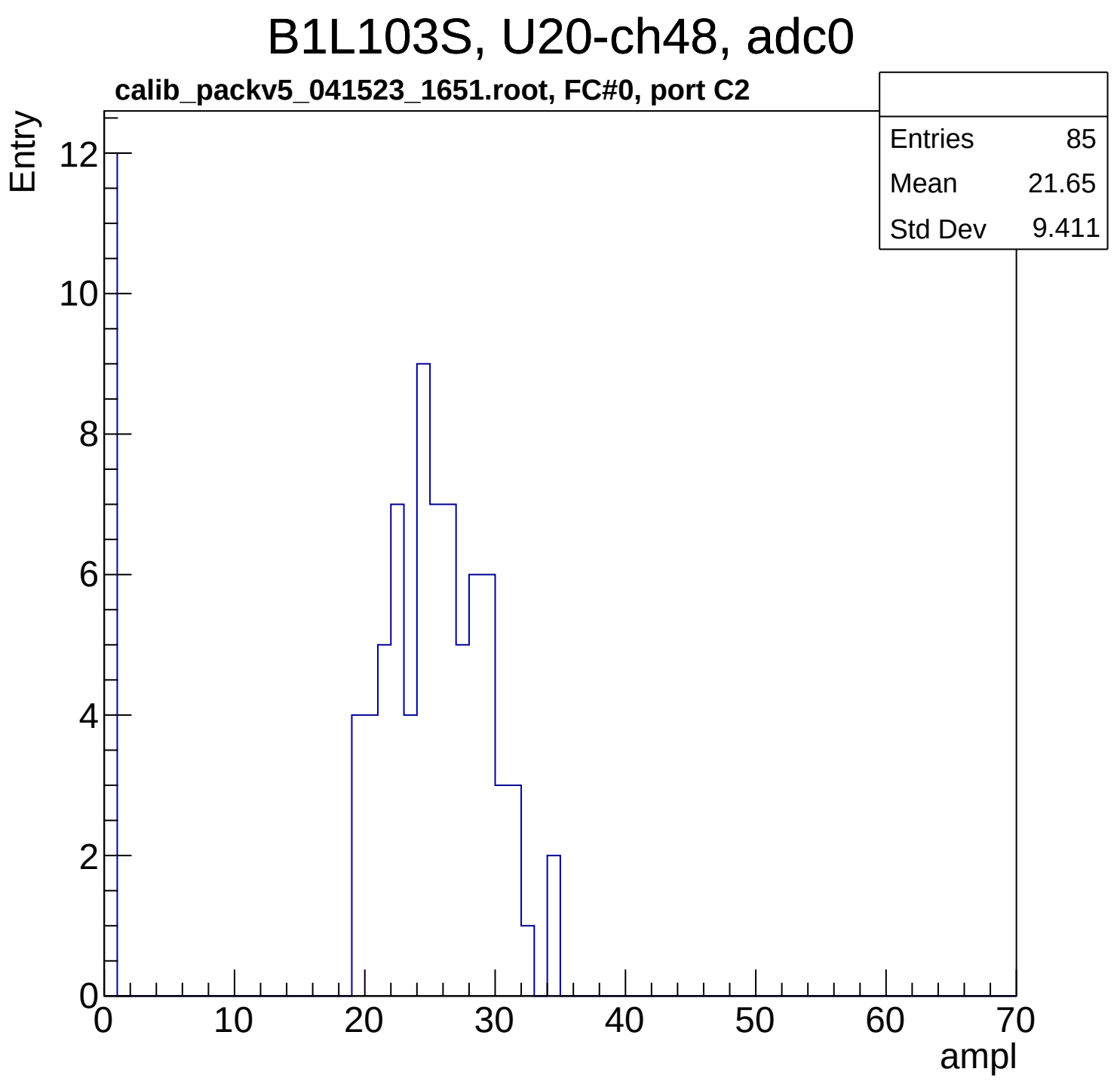
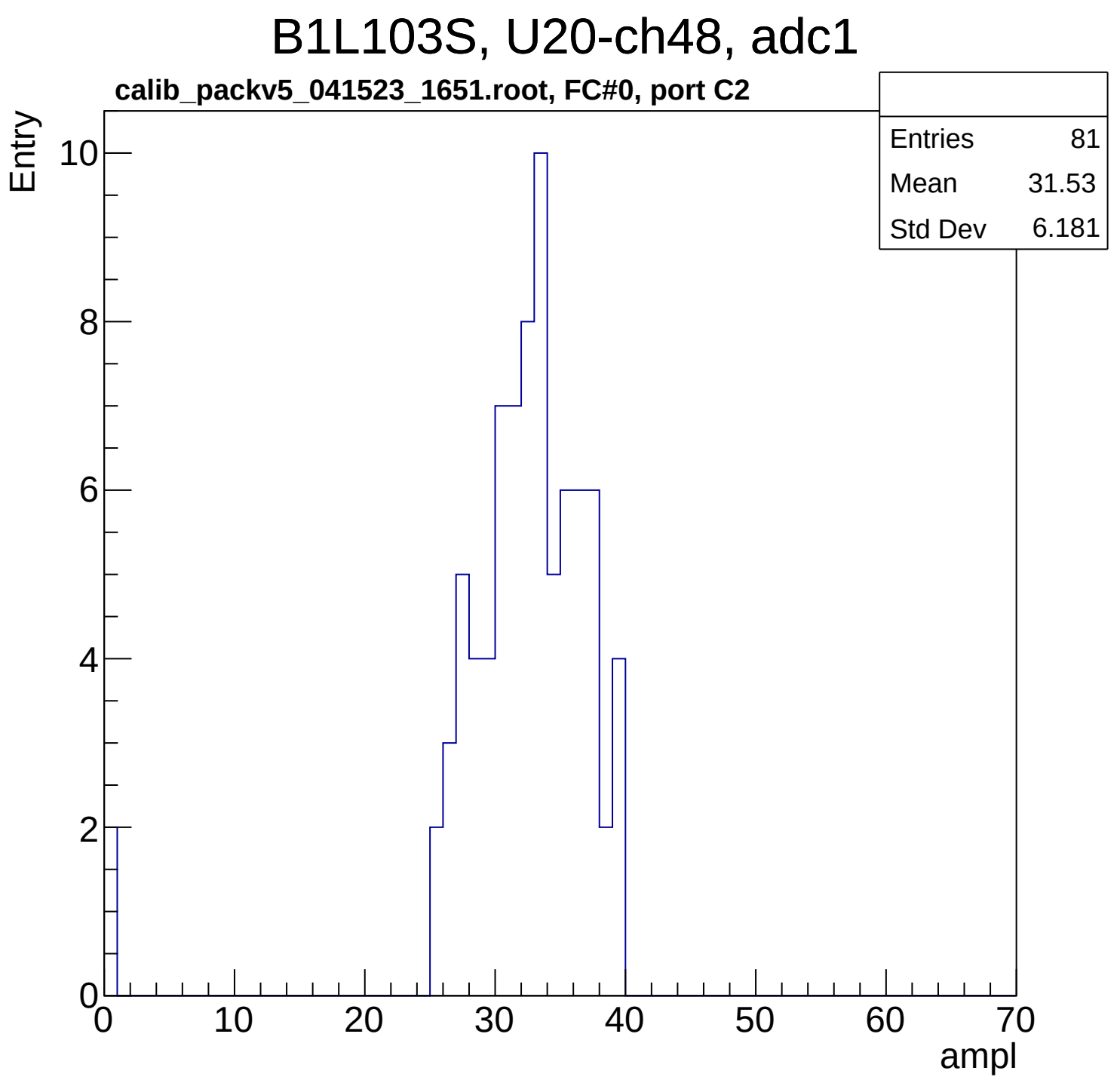
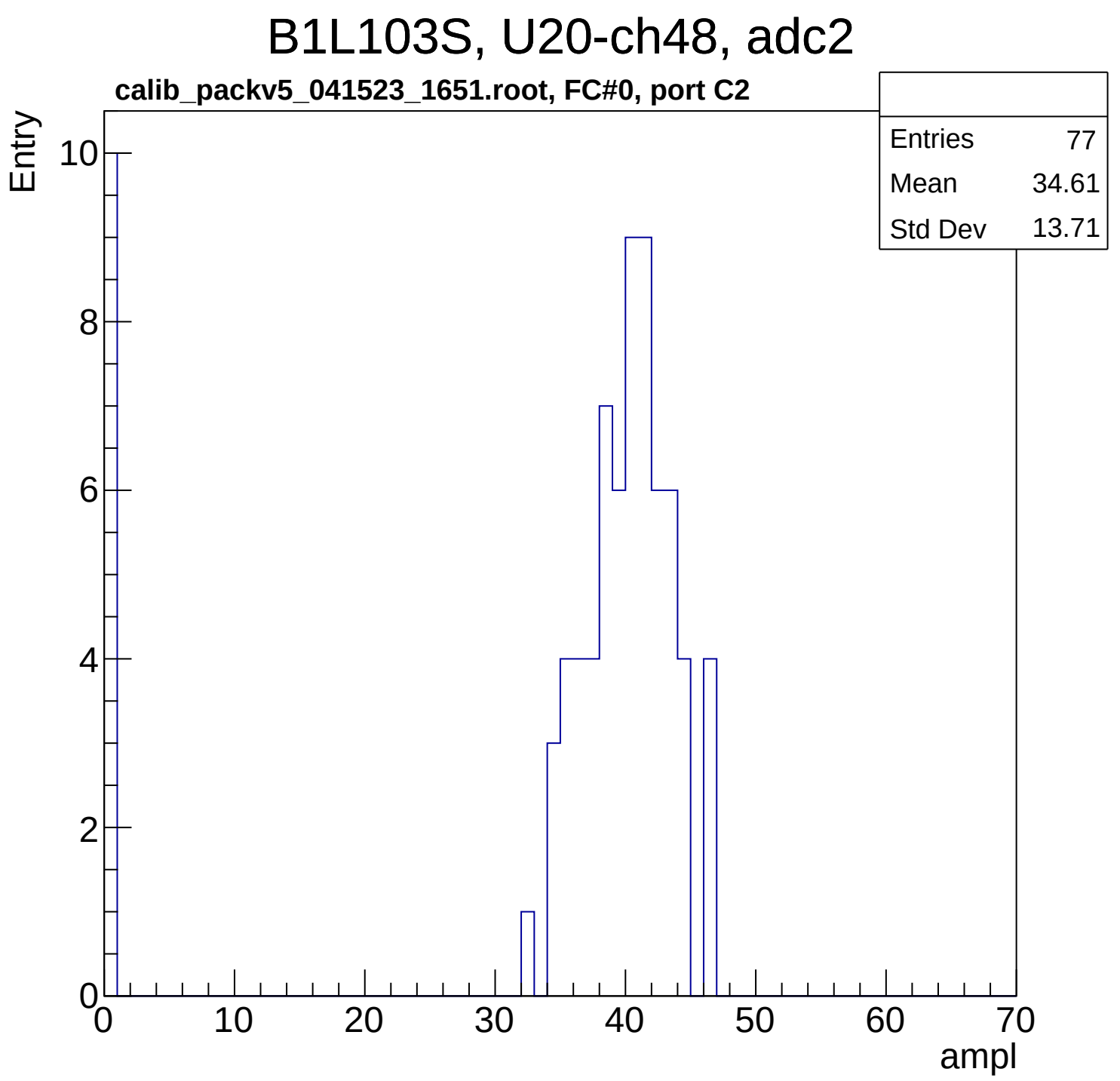
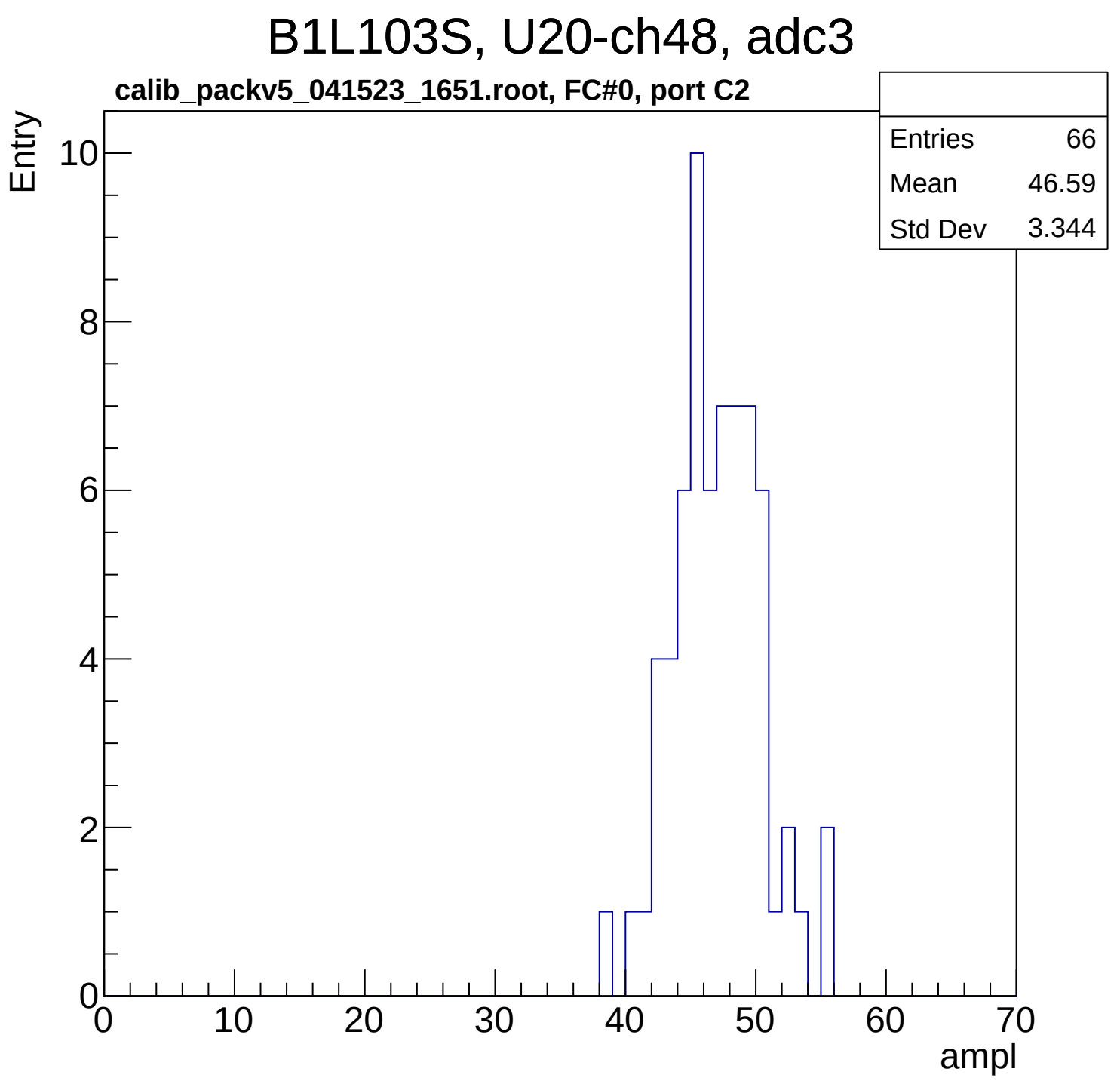
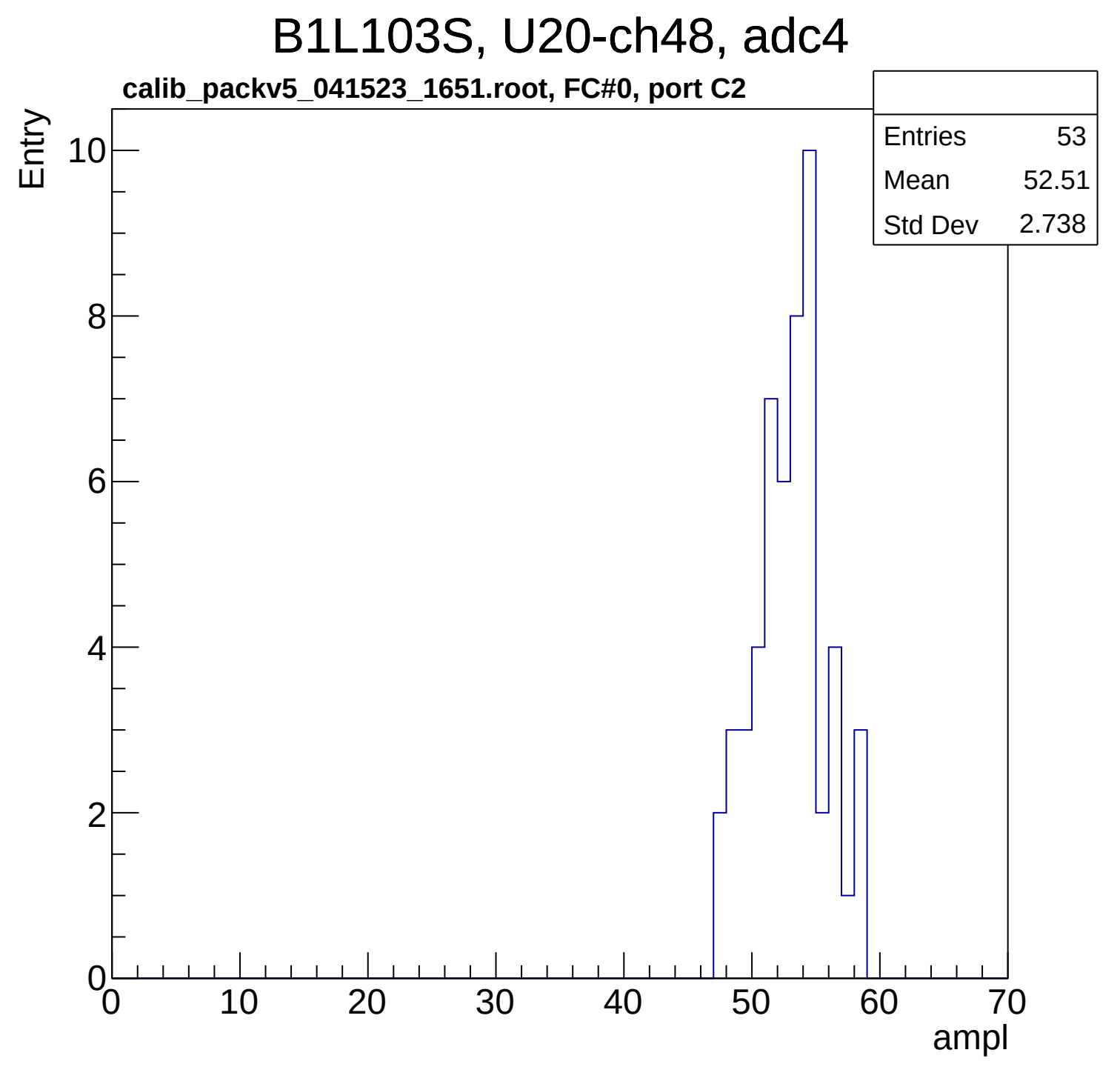

B1L103S, U20-ch47, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

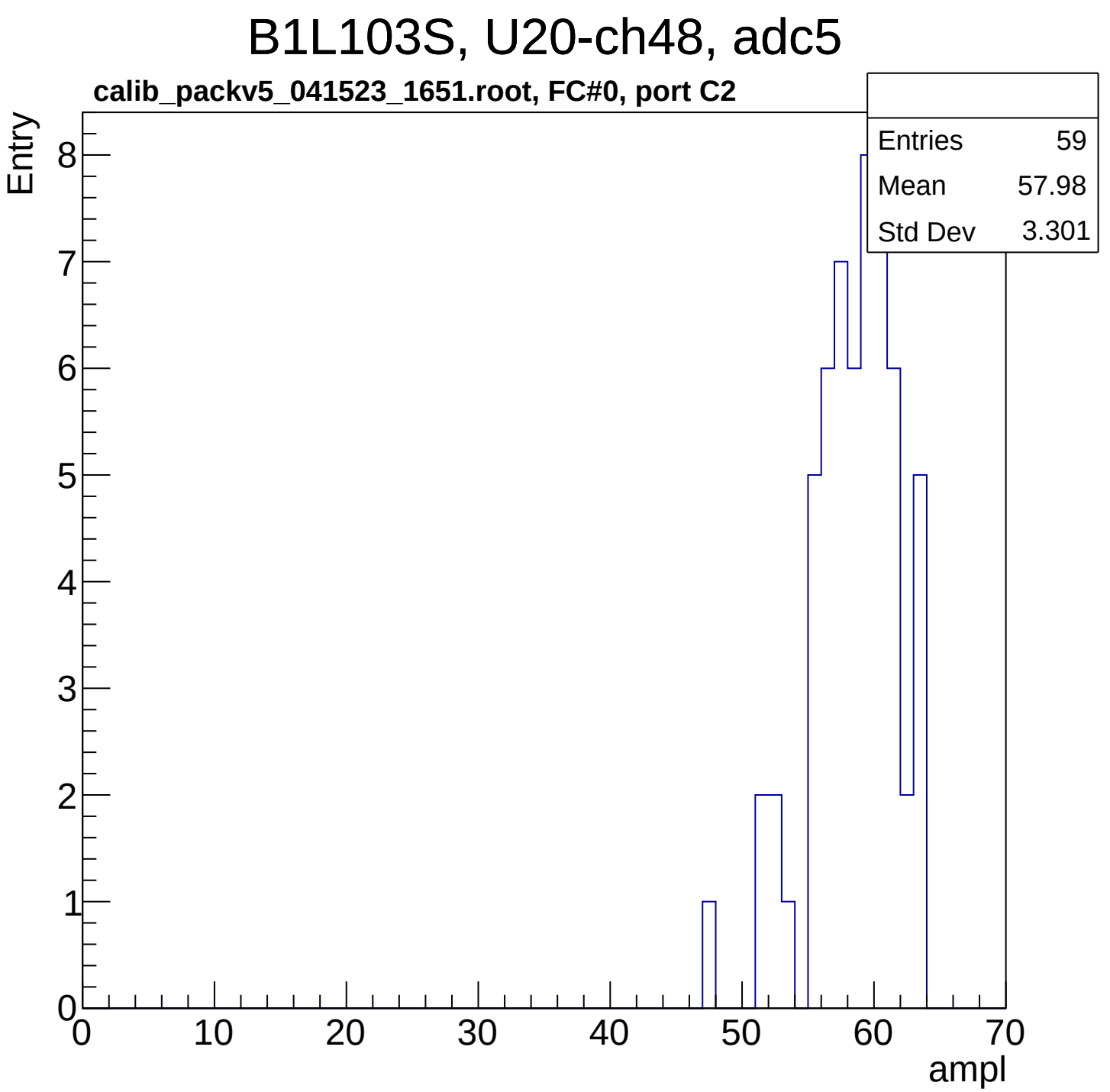

B1L103S, U20-ch48, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 21.65
Std Dev 9.411
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch48, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 31.53
Std Dev 6.181
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U20-ch48, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 34.61
Std Dev 13.71
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch48, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 46.59
Std Dev 3.344
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U20-ch48, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 52.51
Std Dev 2.738
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch48, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 57.98
Std Dev 3.301
Entry
ampl
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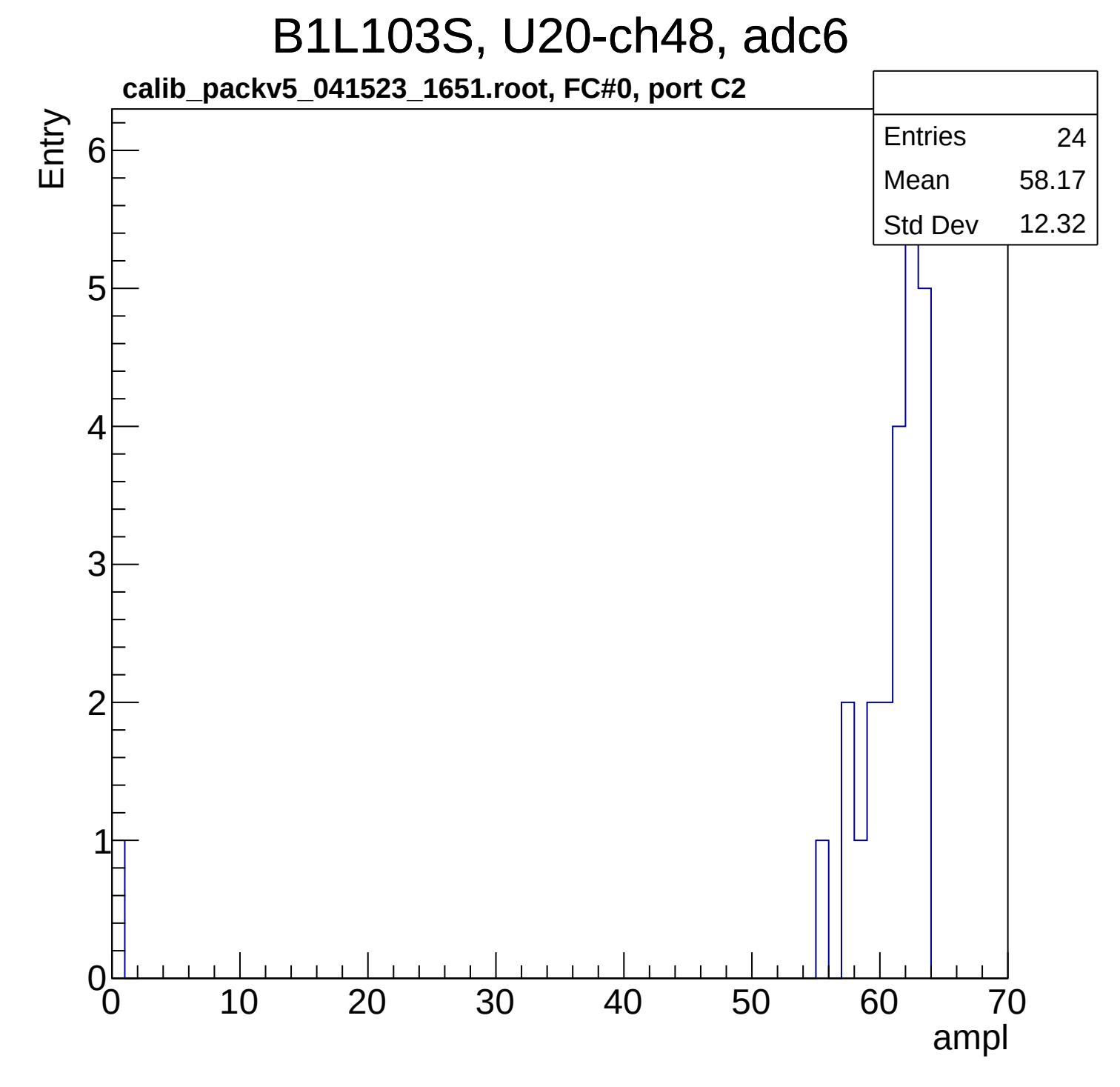
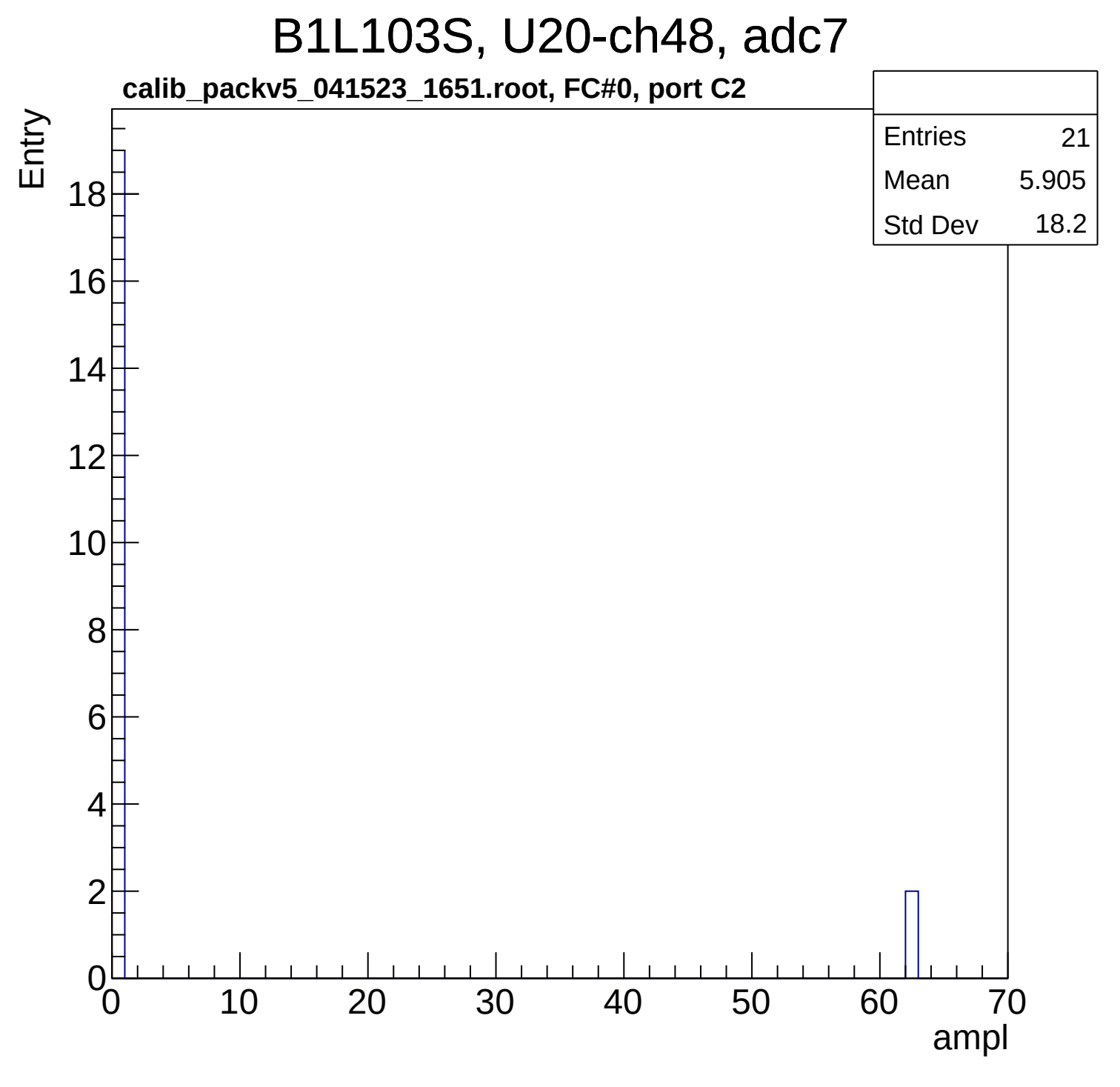
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch48, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 58.17
Std Dev 12.32
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U20-ch48, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.905
Std Dev 18.2
Entry
0
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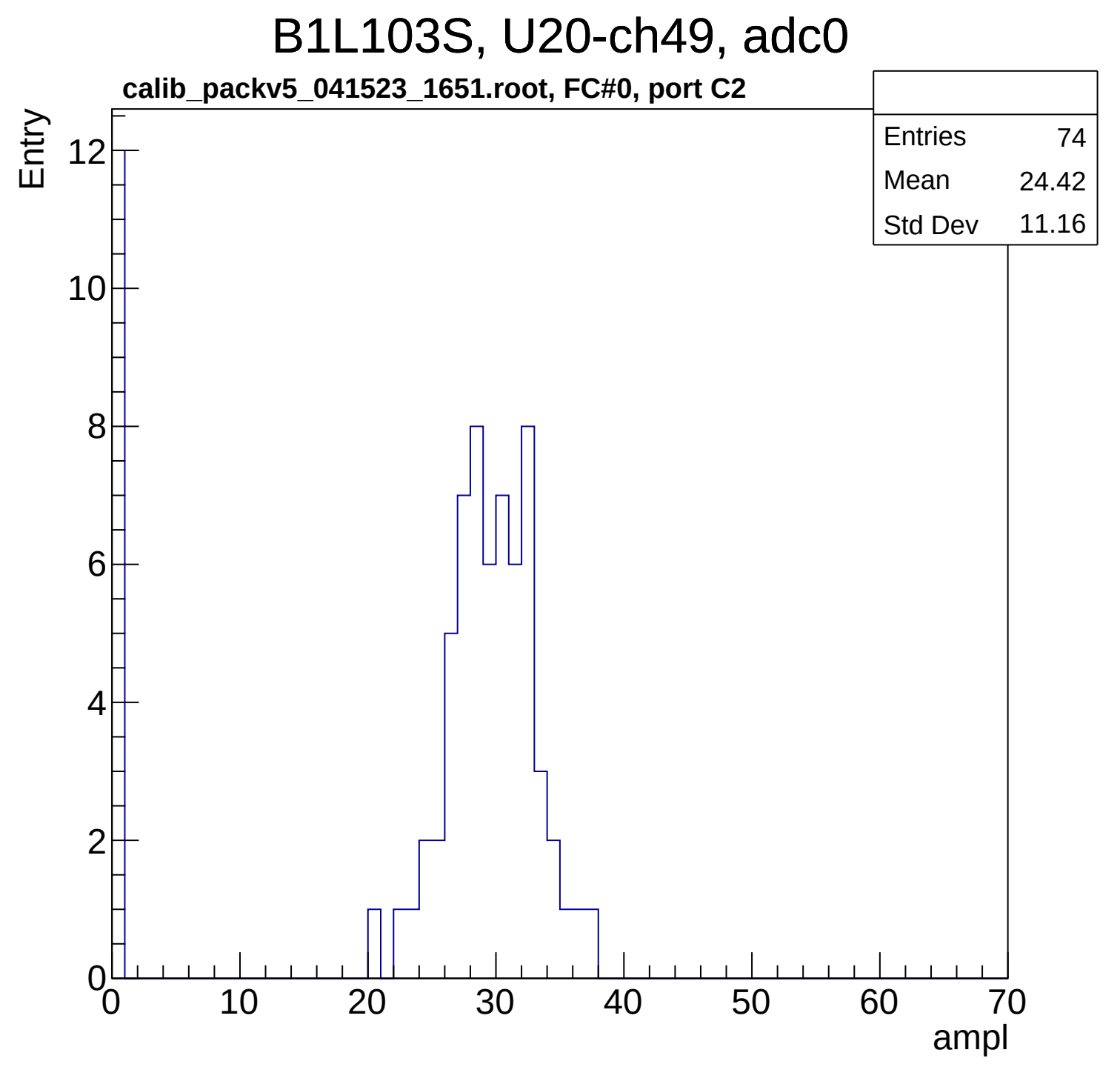
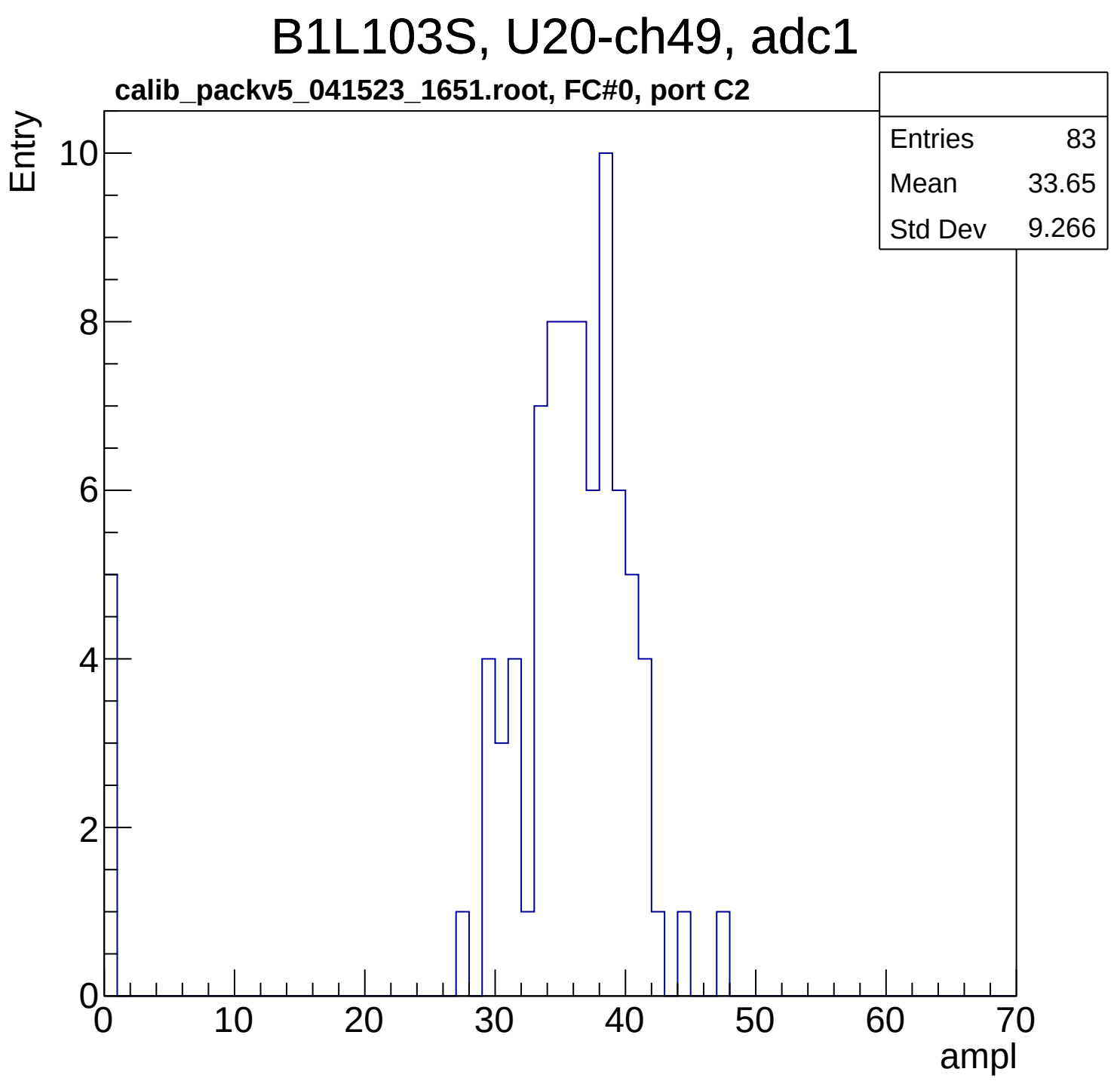
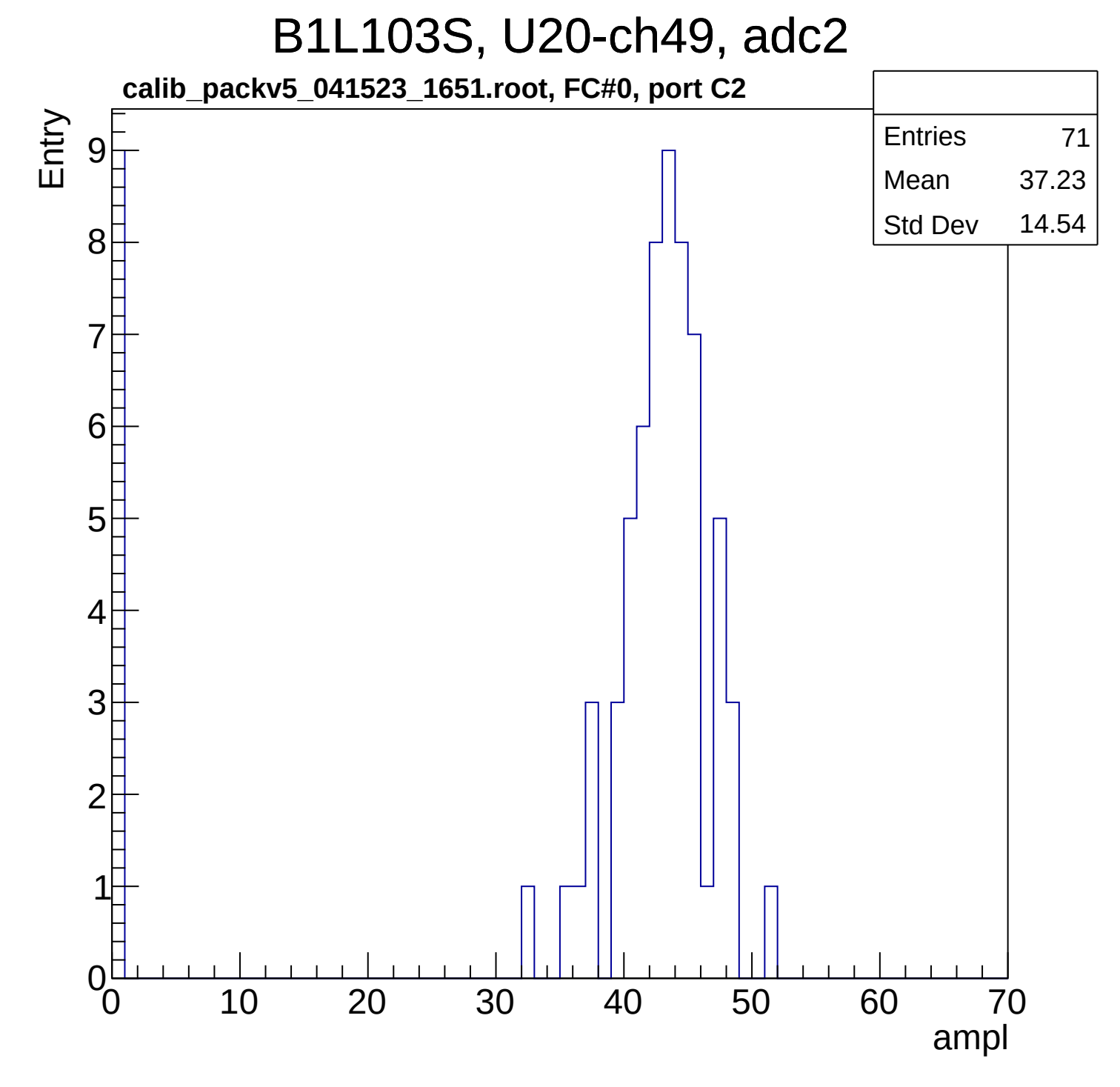
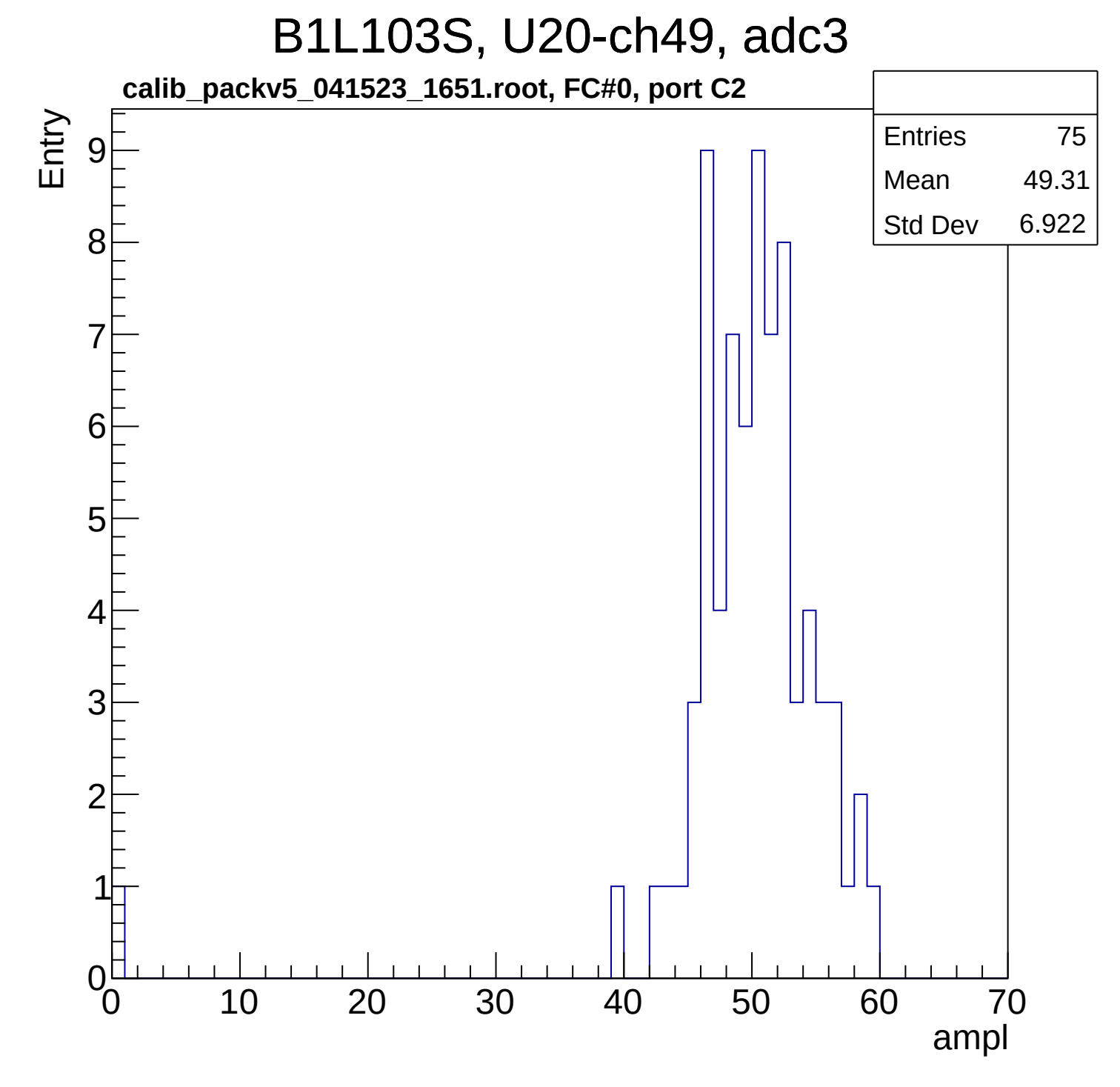
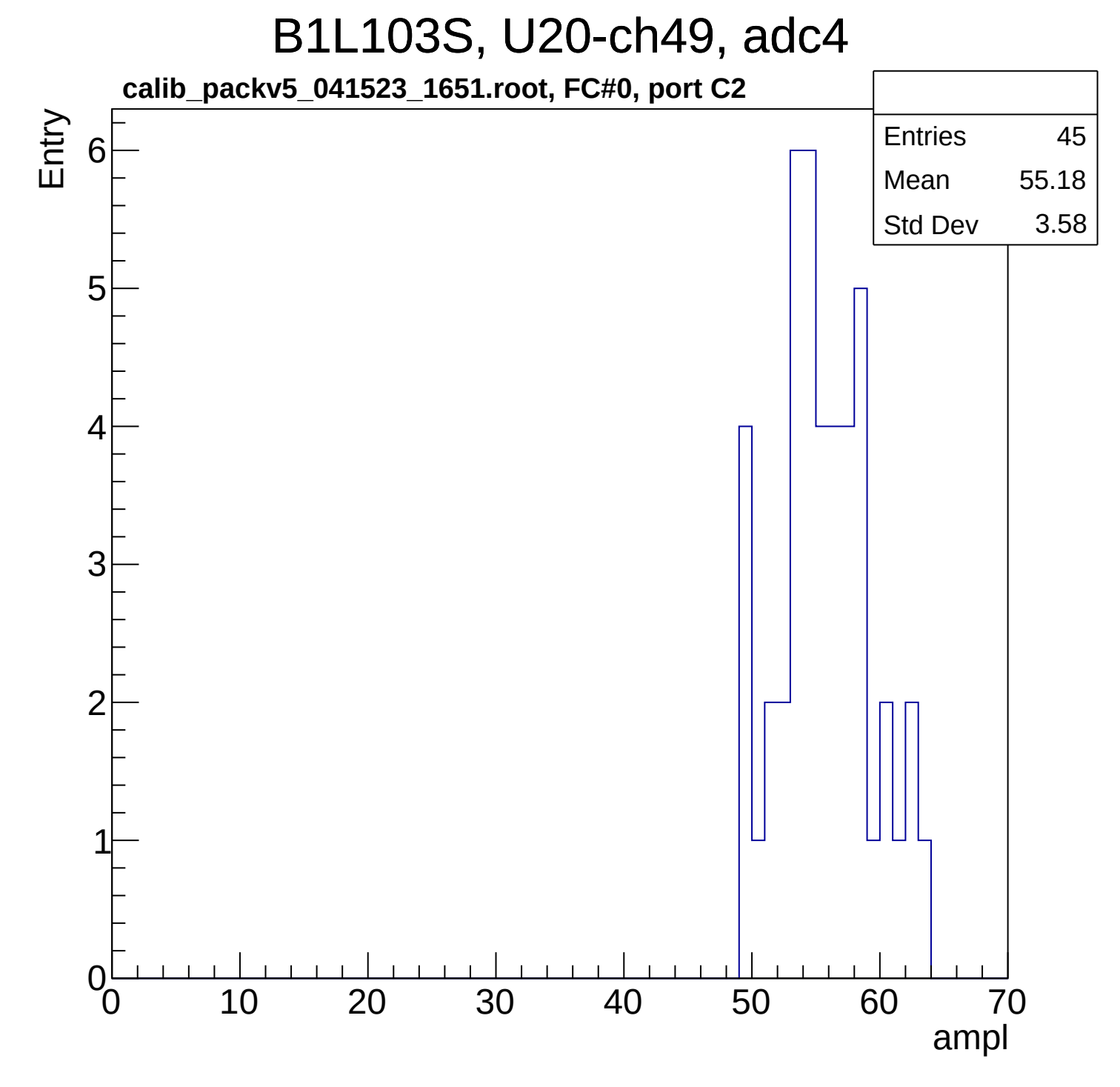
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

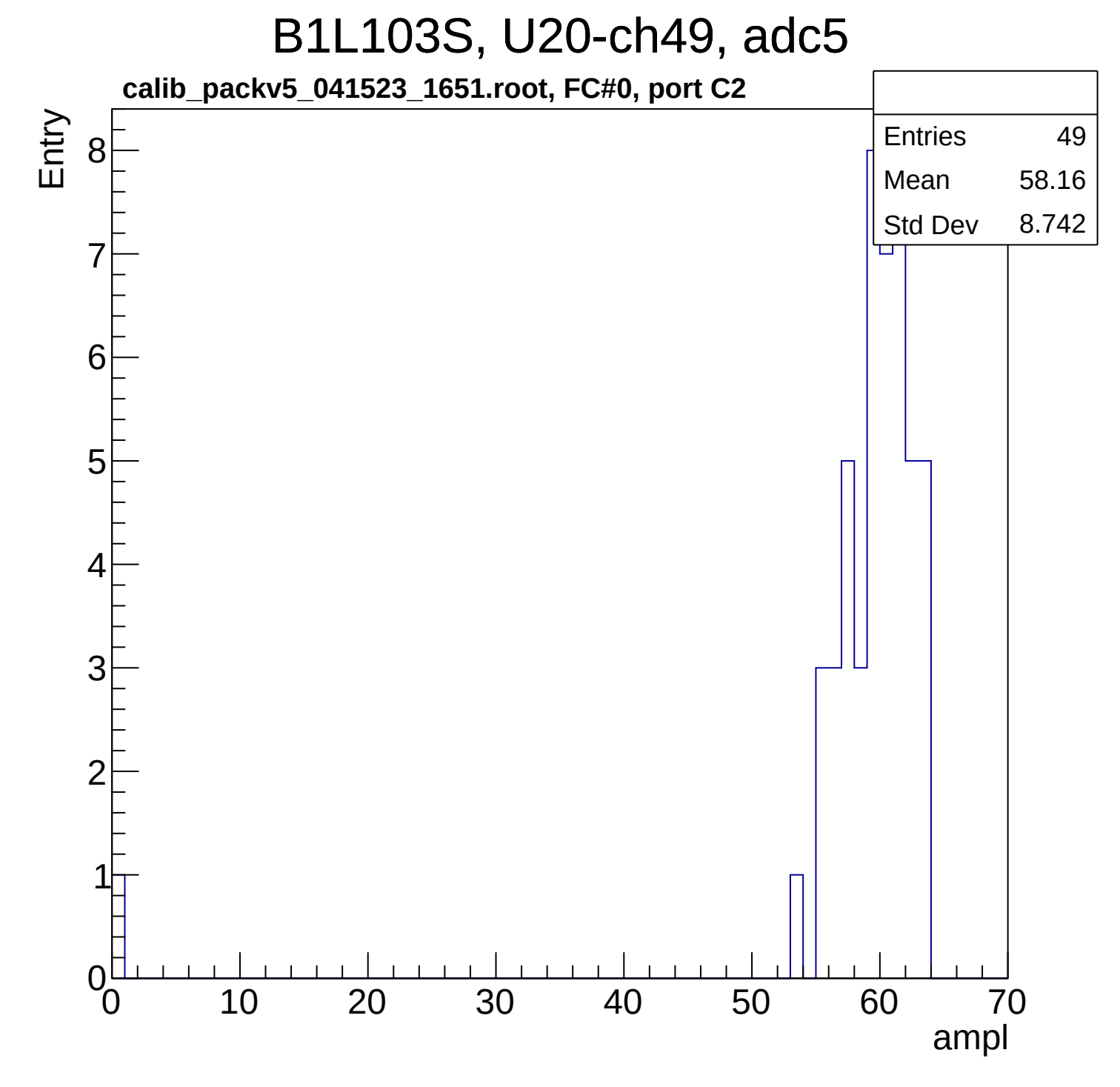

B1L103S, U20-ch49, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 24.42
Std Dev 11.16
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

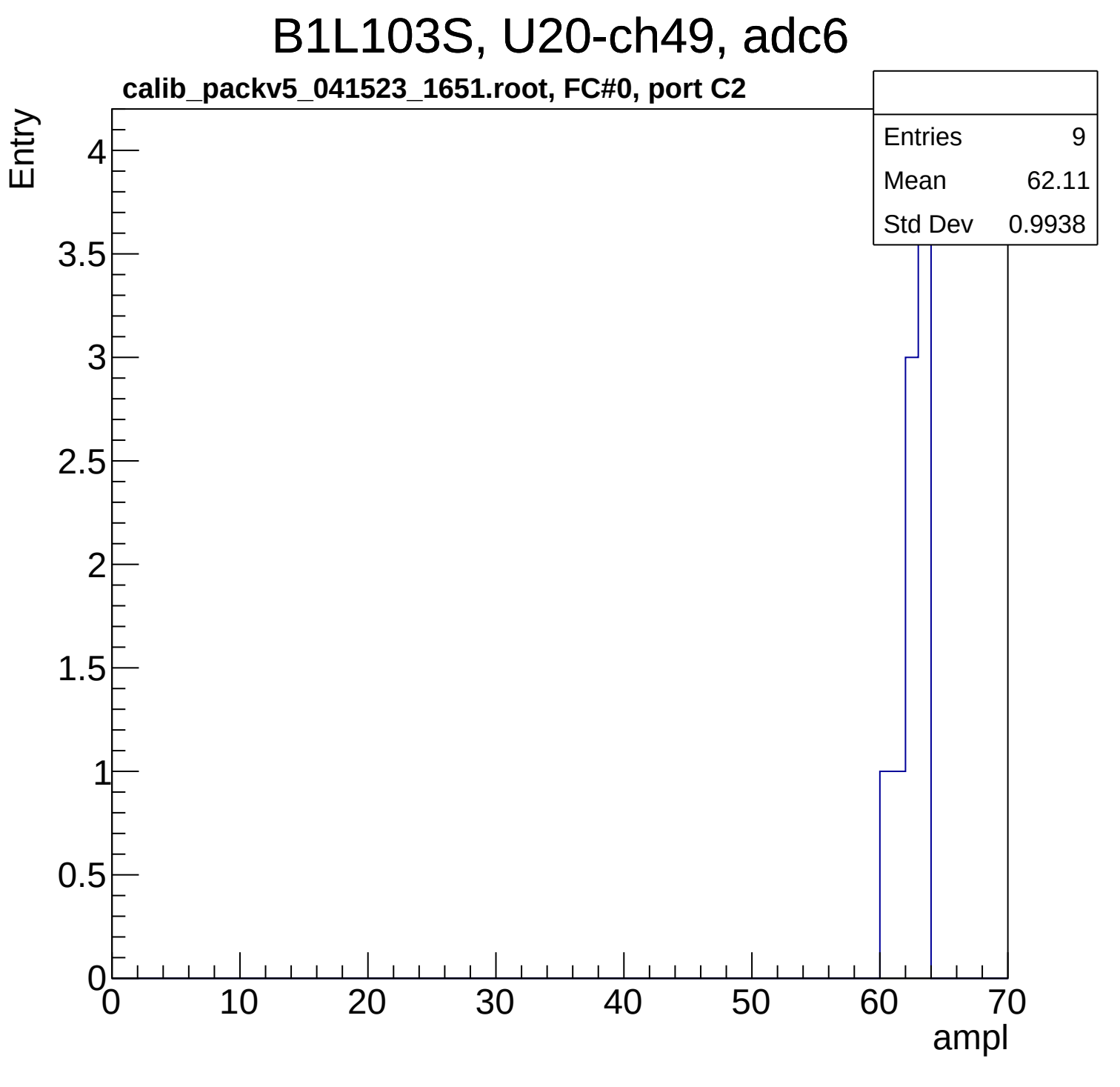

B1L103S, U20-ch49, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 33.65
Std Dev 9.266
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

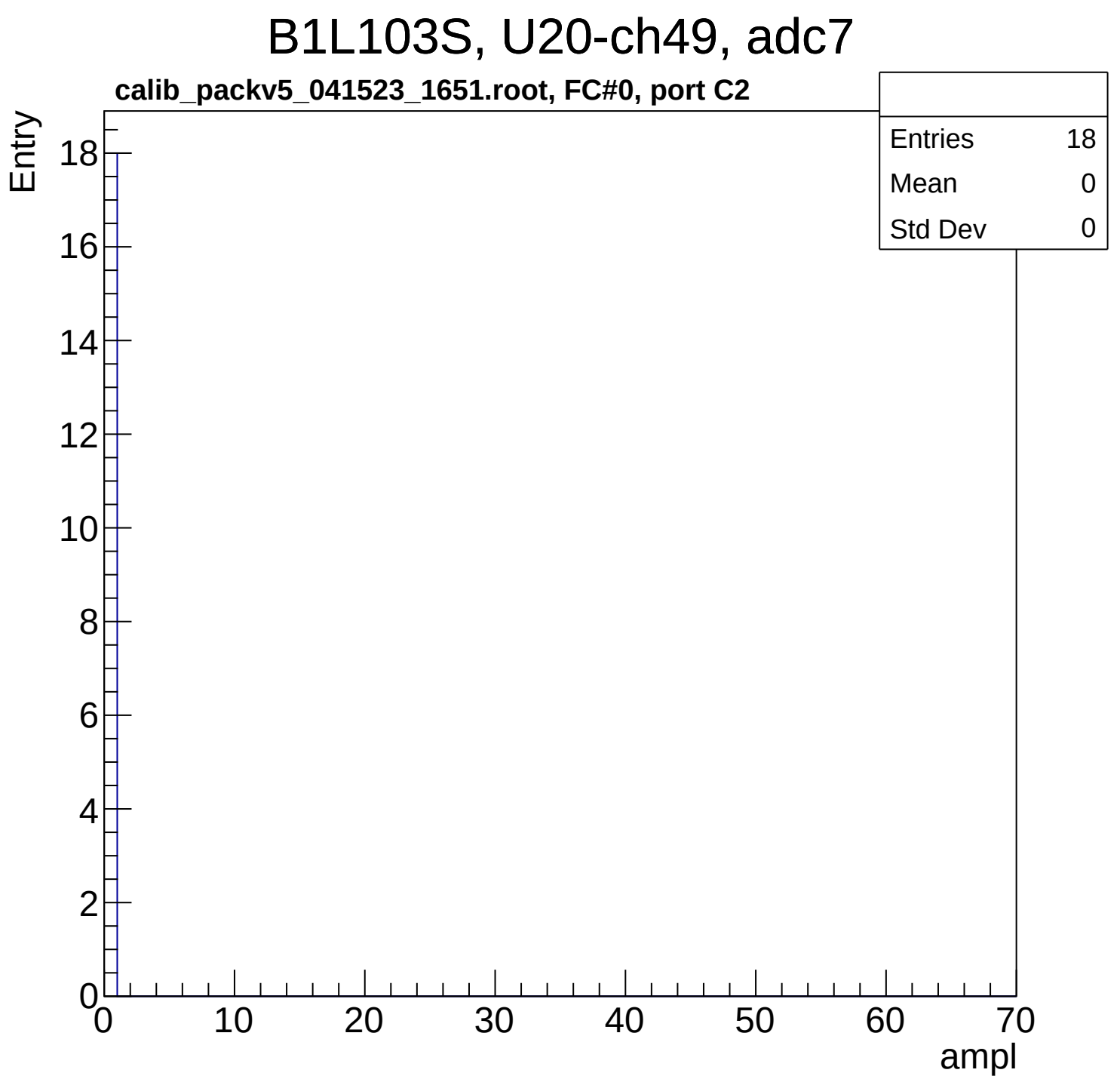

B1L103S, U20-ch49, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 37.23
Std Dev 14.54
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

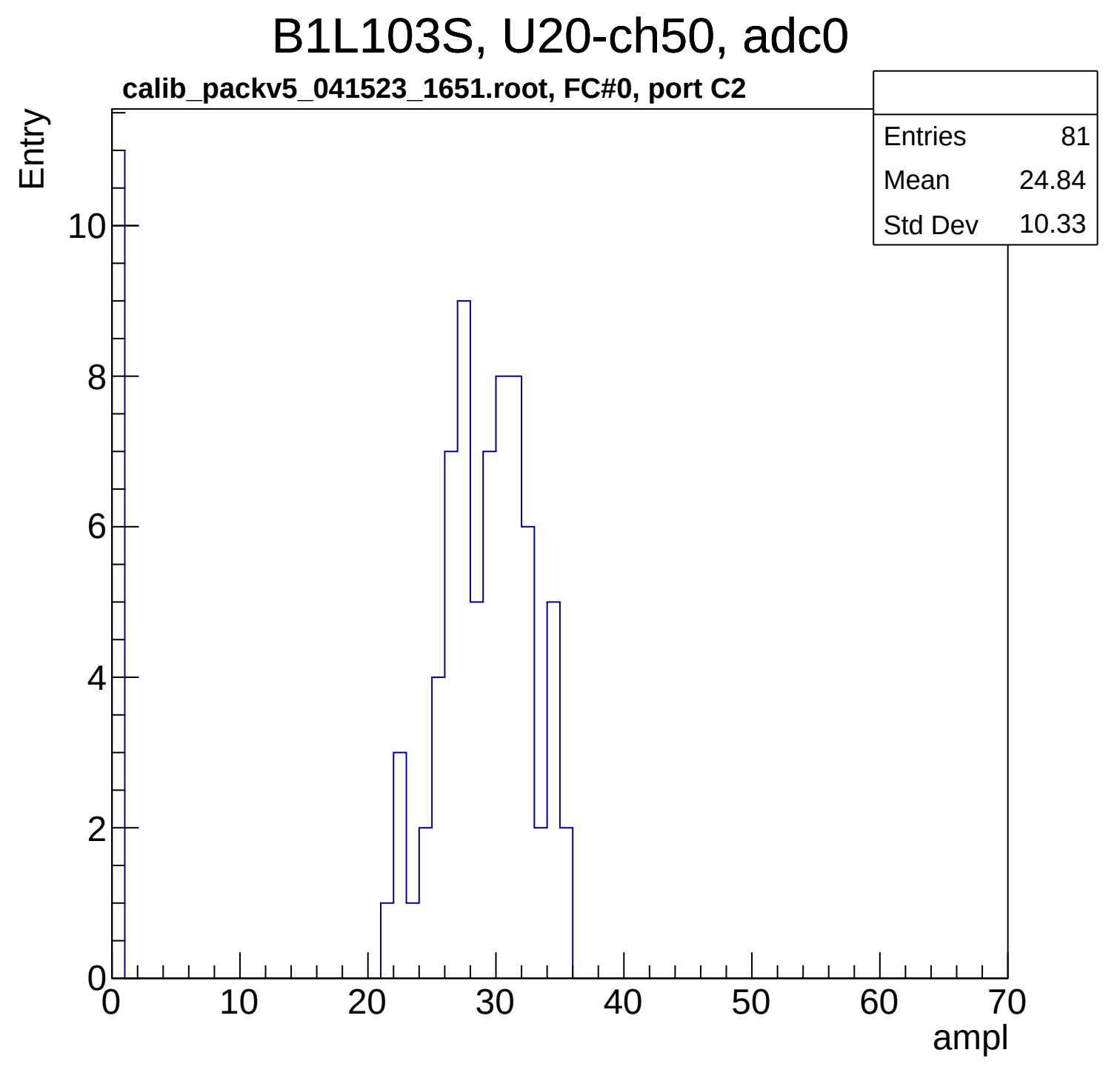

B1L103S, U20-ch49, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 49.31
Std Dev 6.922
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

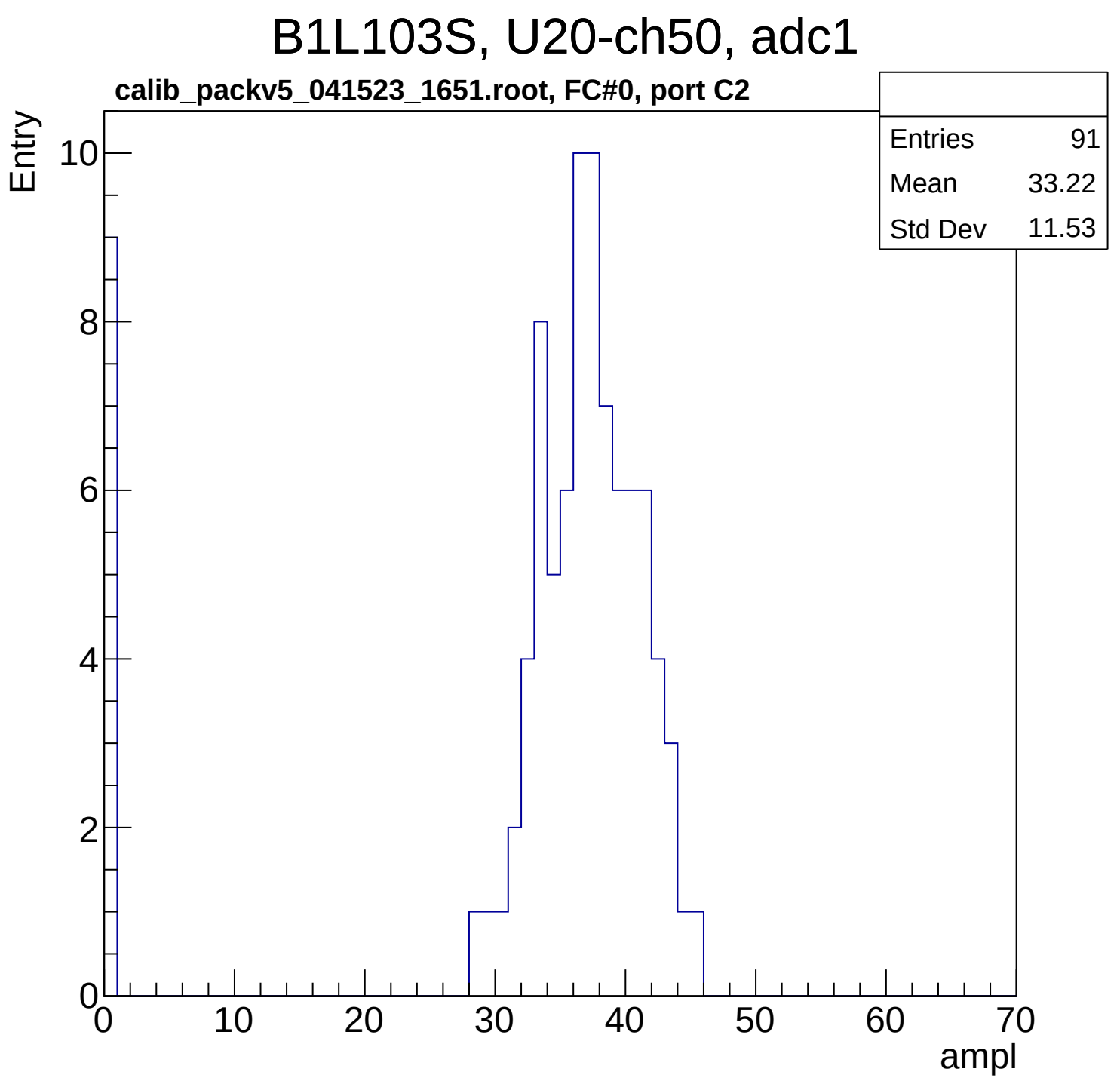

B1L103S, U20-ch49, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 55.18
Std Dev 3.58
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

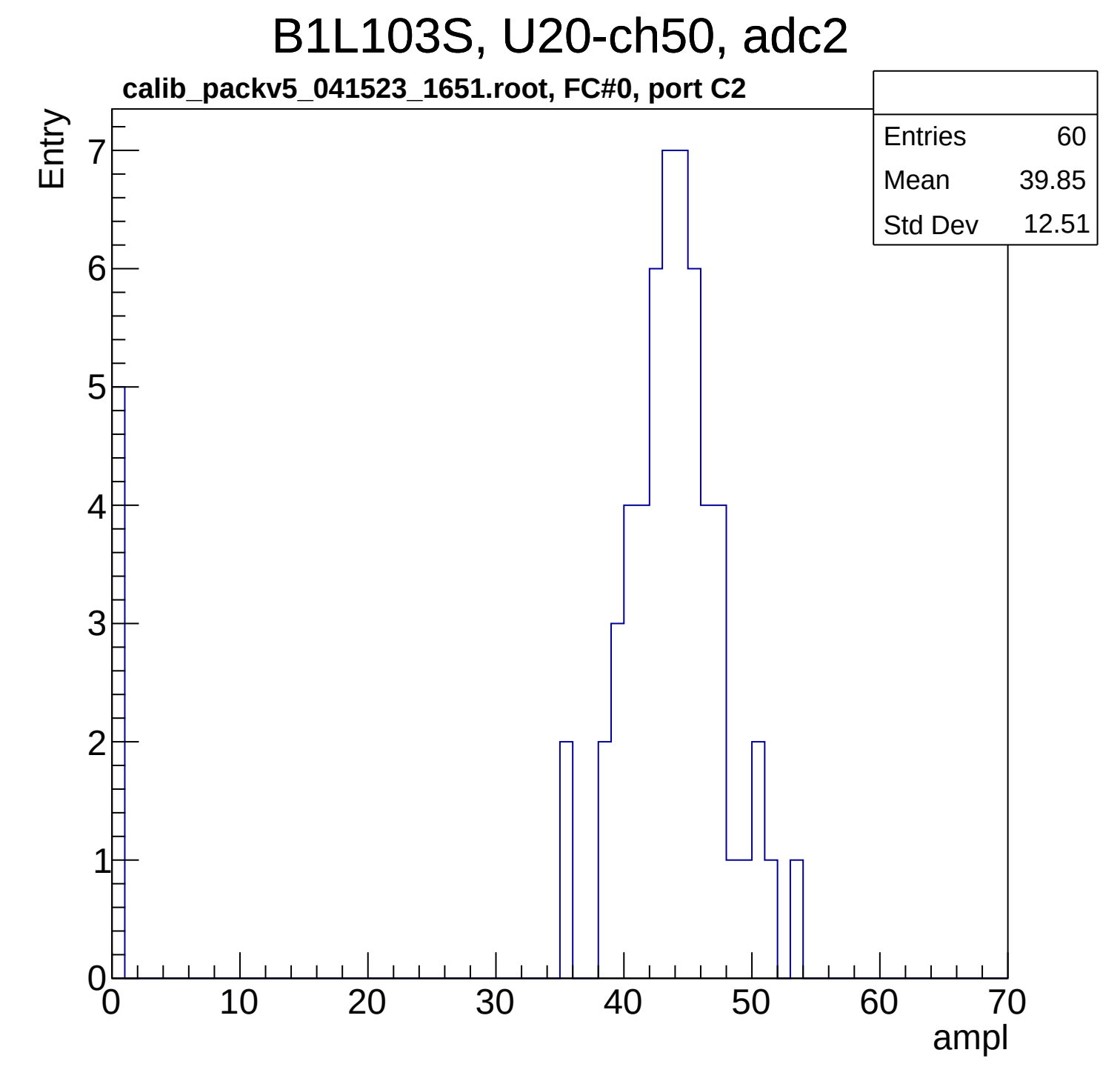

B1L103S, U20-ch49, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 58.16
Std Dev 8.742
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch49, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 62.11
Std Dev 0.9938
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U20-ch49, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch50, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 24.84
Std Dev 10.33
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch50, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 33.22
Std Dev 11.53
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U20-ch50, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 39.85
Std Dev 12.51
Entry
ampl
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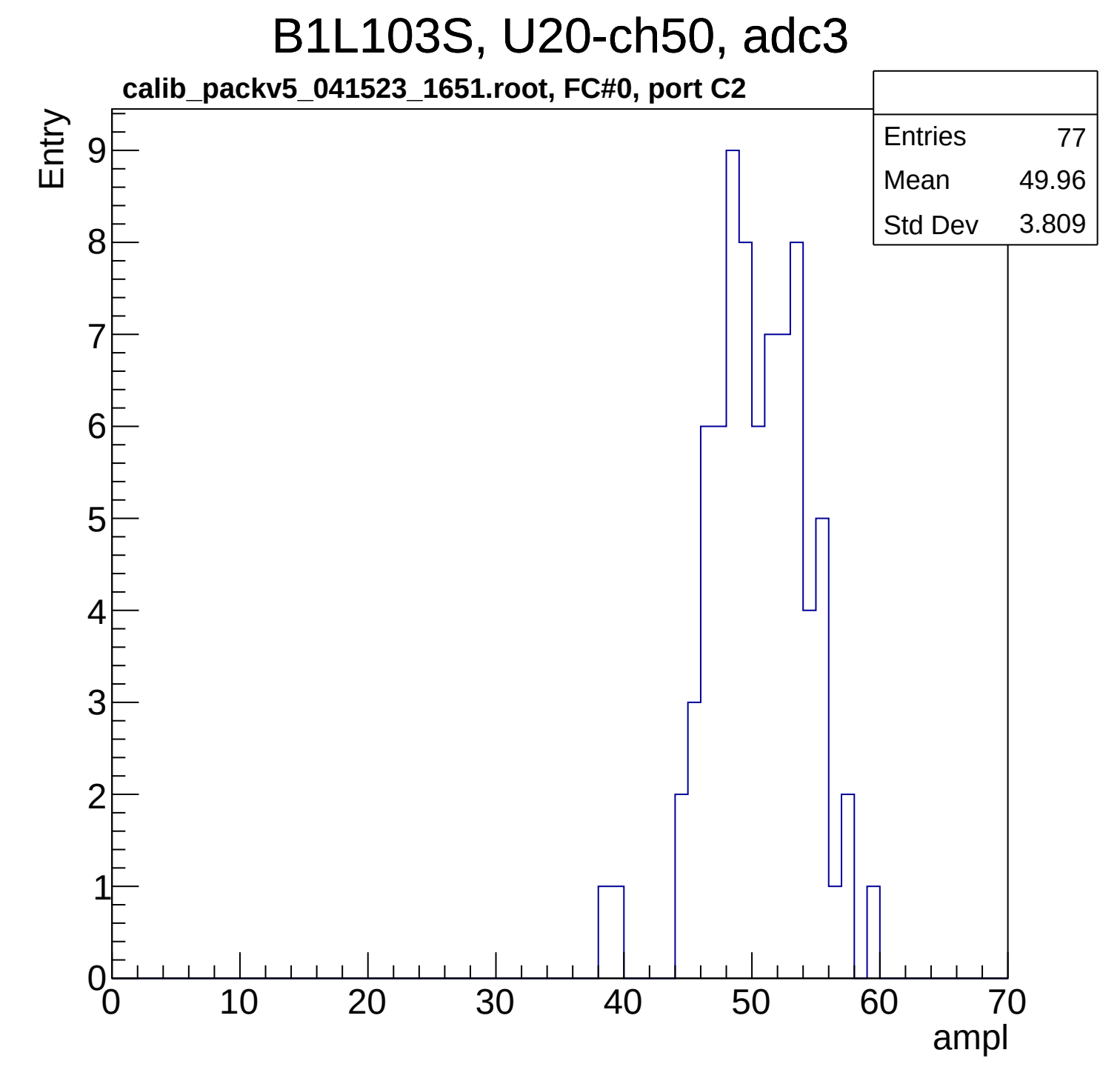
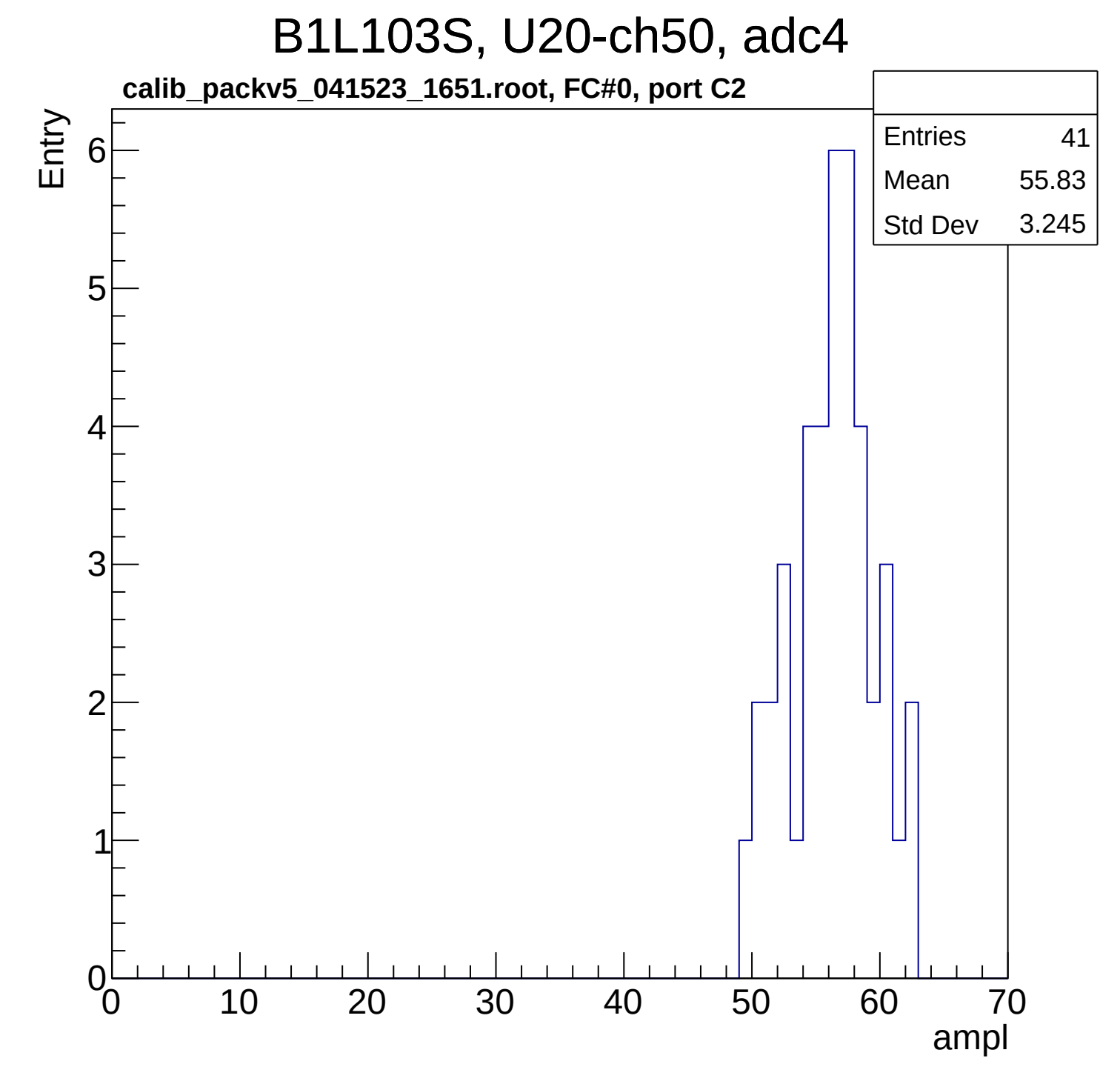
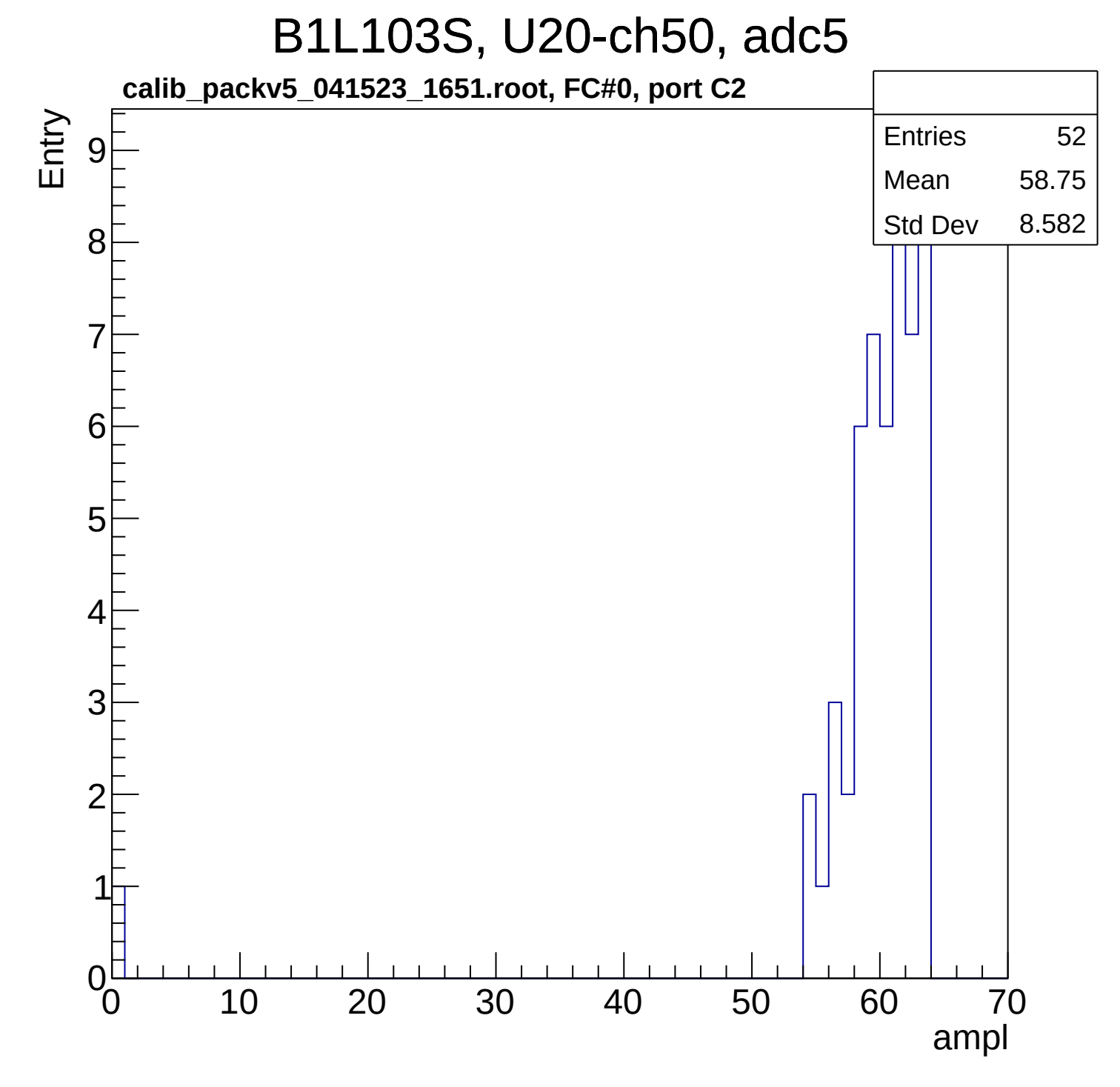
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U20-ch50, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 49.96
Std Dev 3.809
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch50, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 55.83
Std Dev 3.245
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U20-ch50, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 58.75
Std Dev 8.582
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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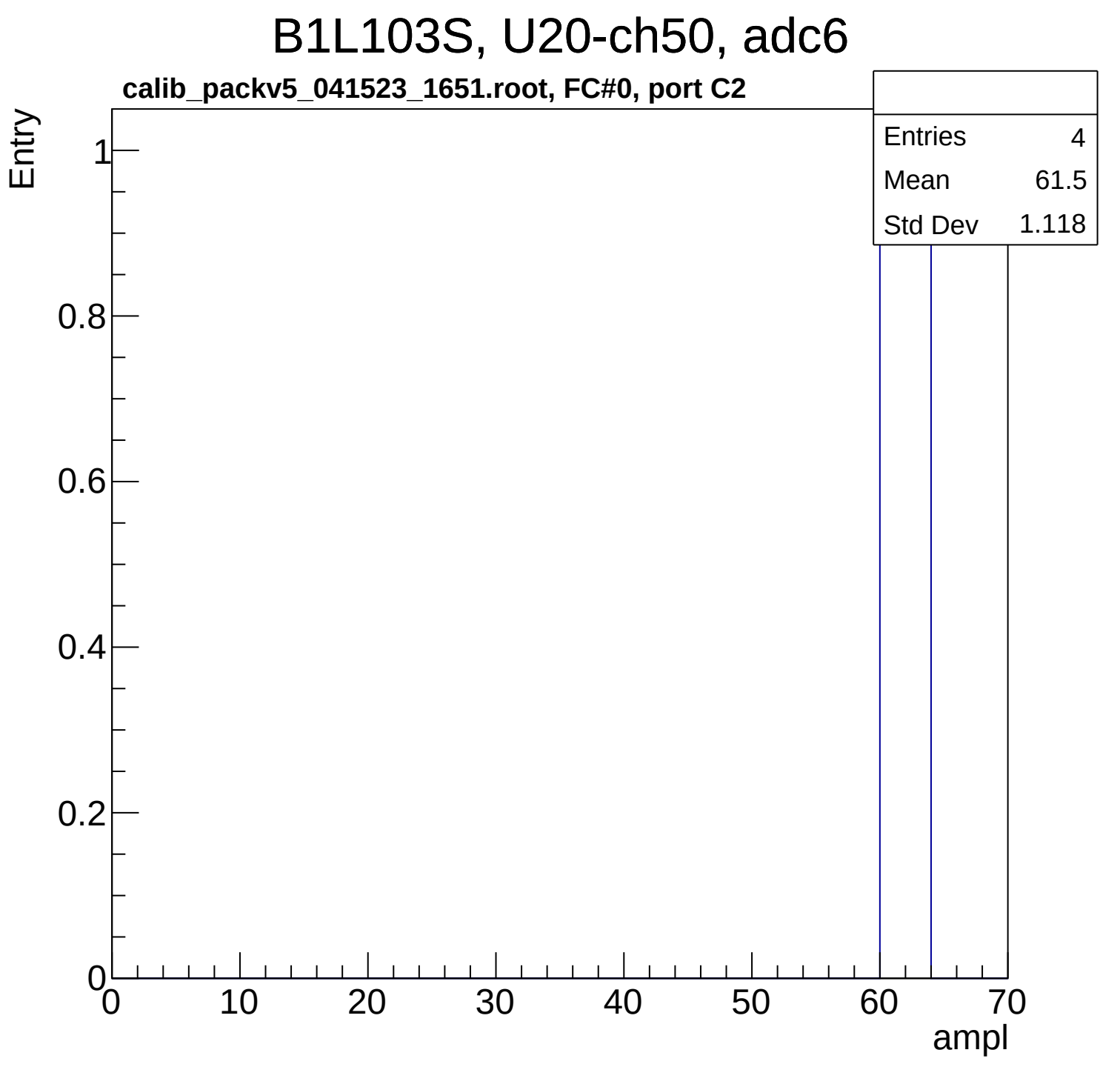
60
70


B1L103S, U20-ch50, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 61.5
Std Dev 1.118
Entry
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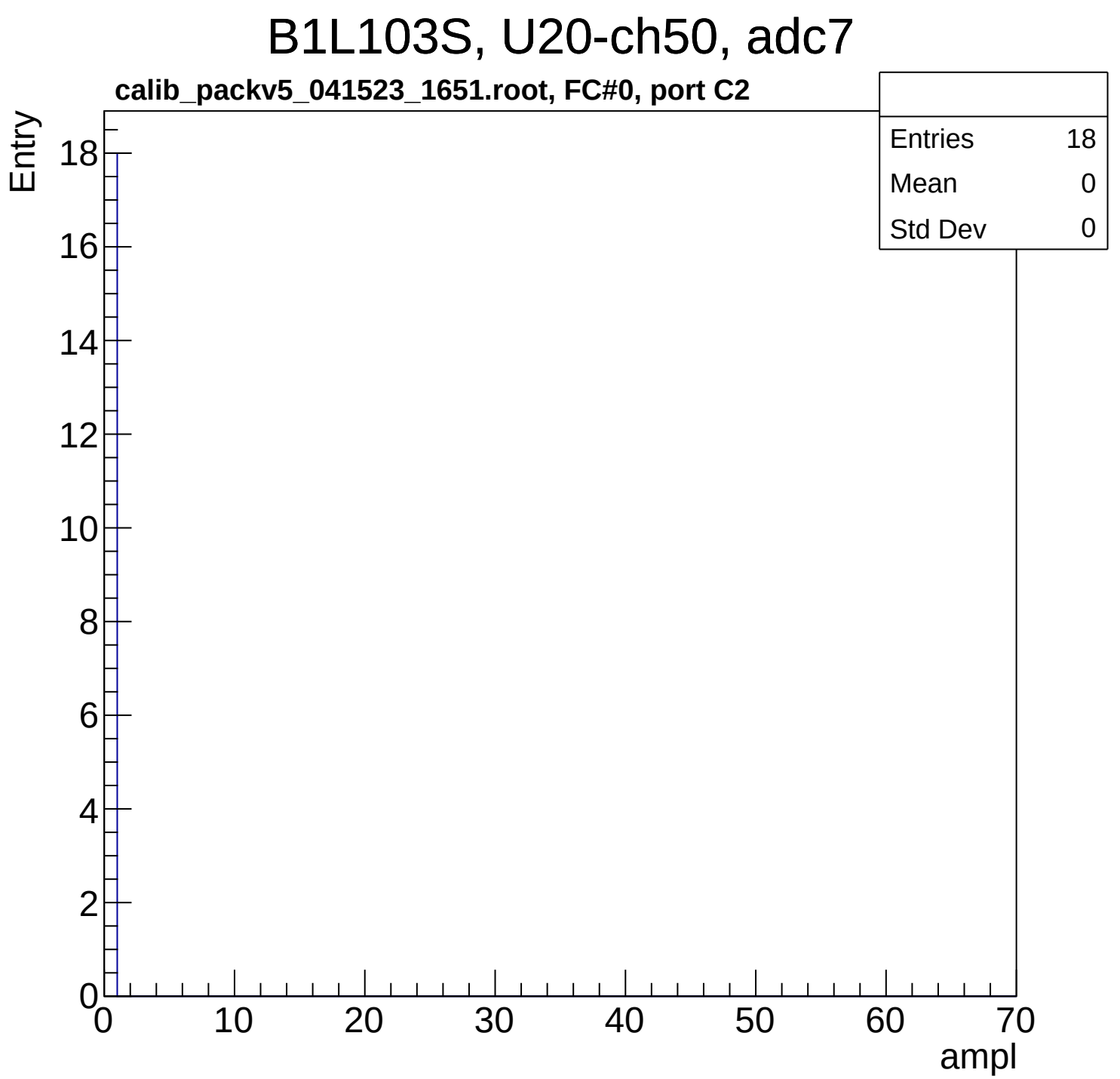
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch50, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
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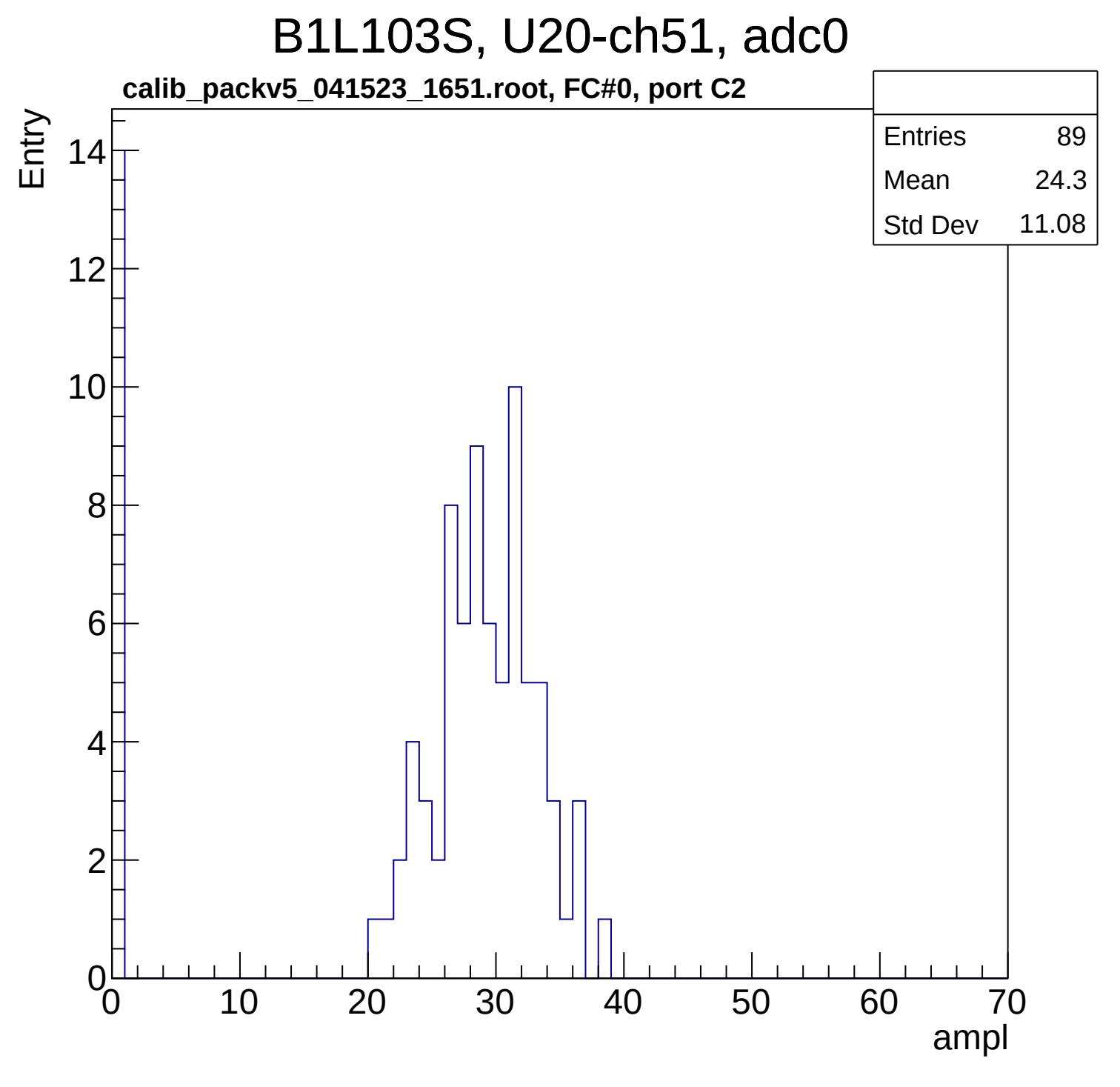
50
60
70
ampl


B1L103S, U20-ch51, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 24.3
Std Dev 11.08
Entry
ampl
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2
4
6
8
10
12
14
0
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40
50
60
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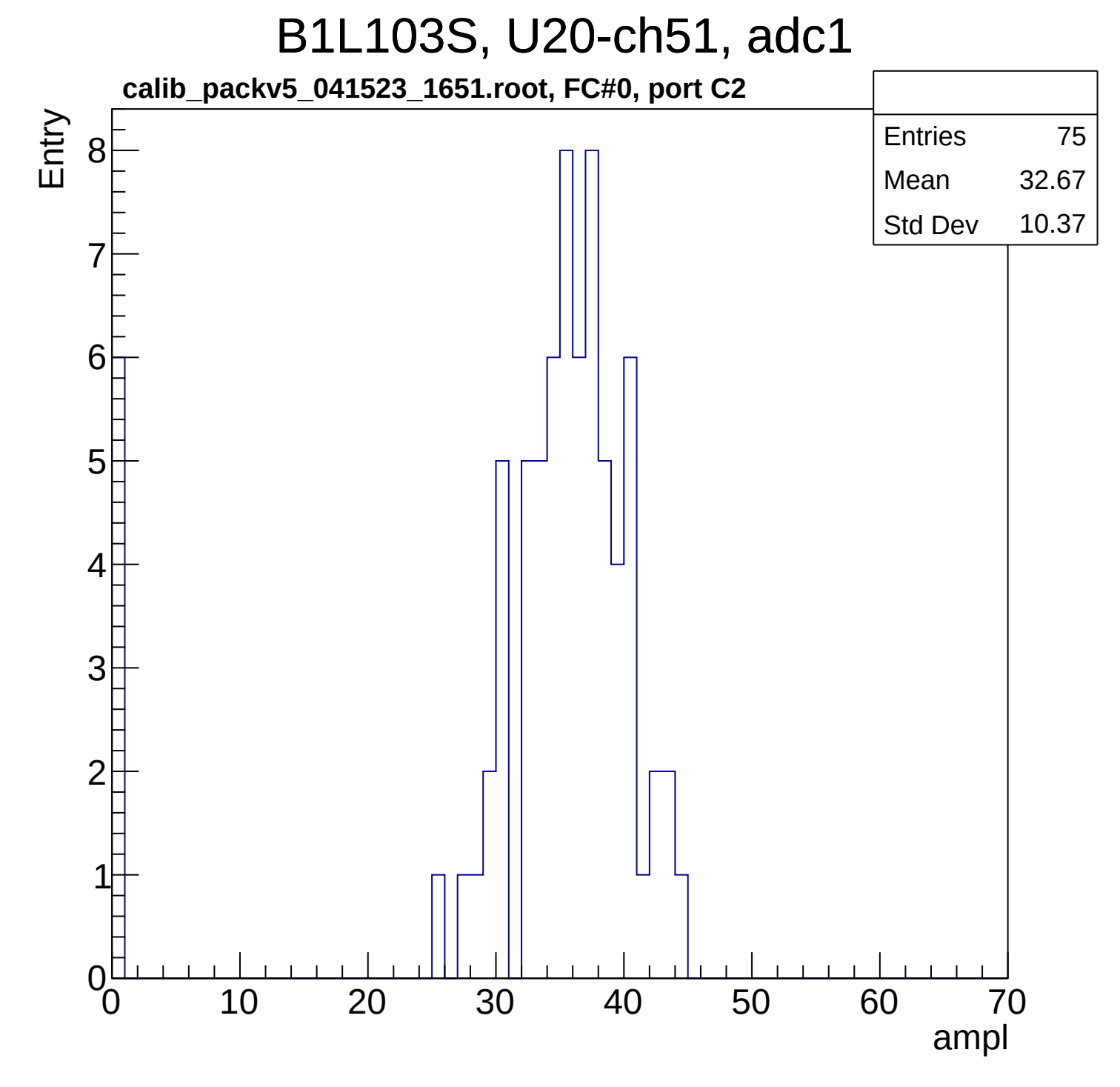
B1L103S, U20-ch51, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 32.67
Std Dev 10.37
Entry
ampl
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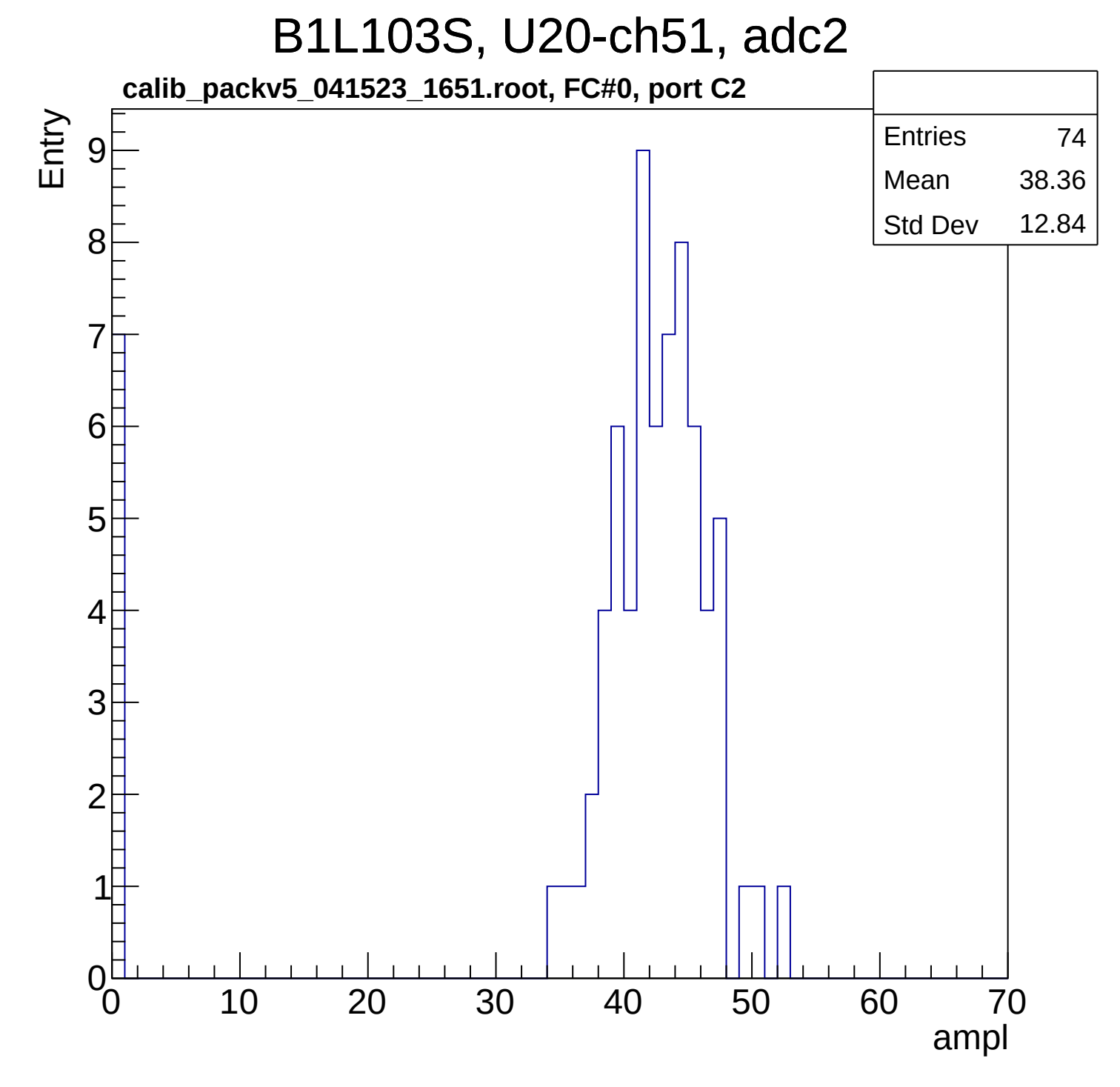
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch51, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 38.36
Std Dev 12.84
Entry
ampl
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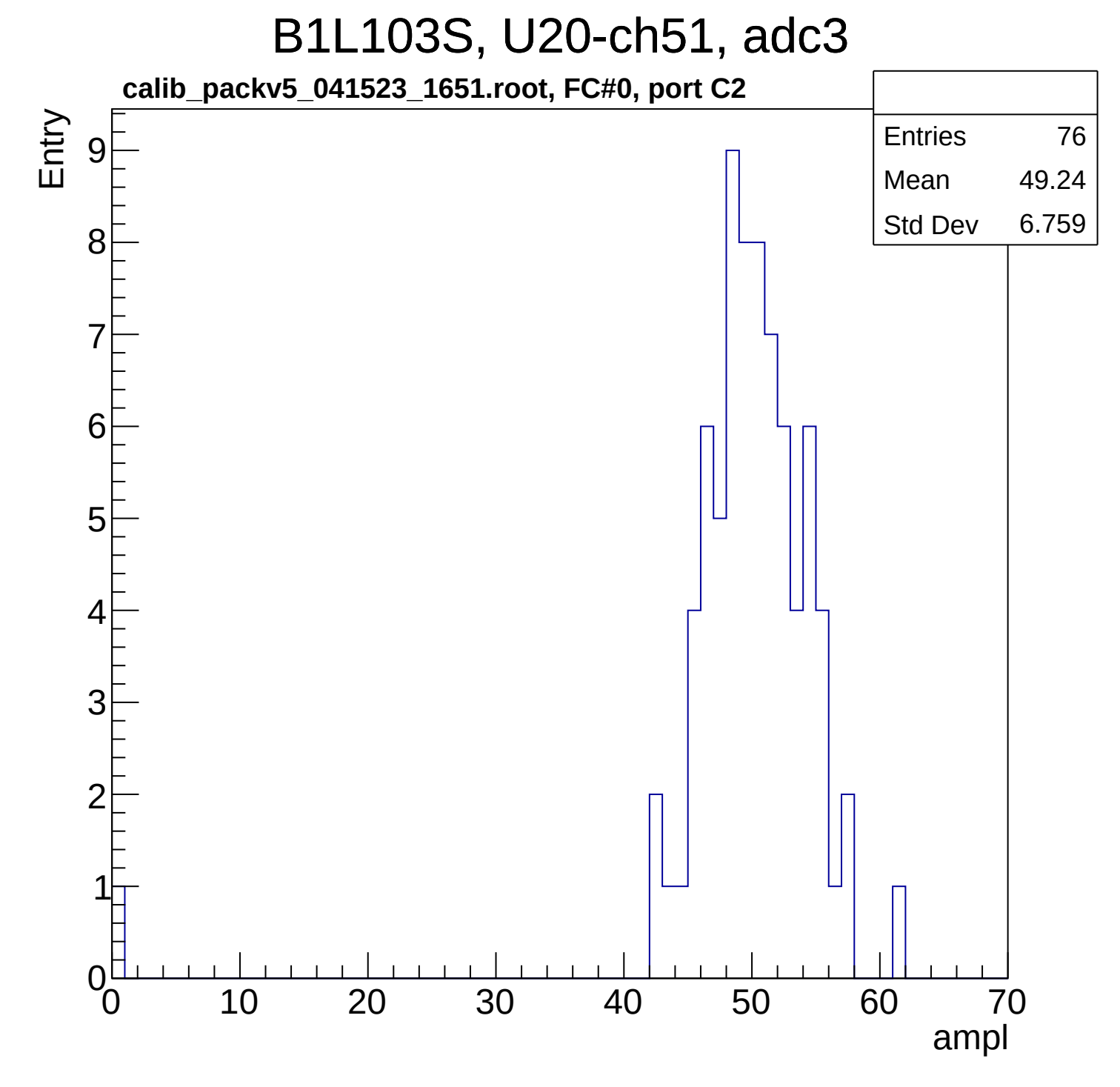
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch51, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 49.24
Std Dev 6.759
Entry
ampl
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2
3
4
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6
7
8
9
0
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60
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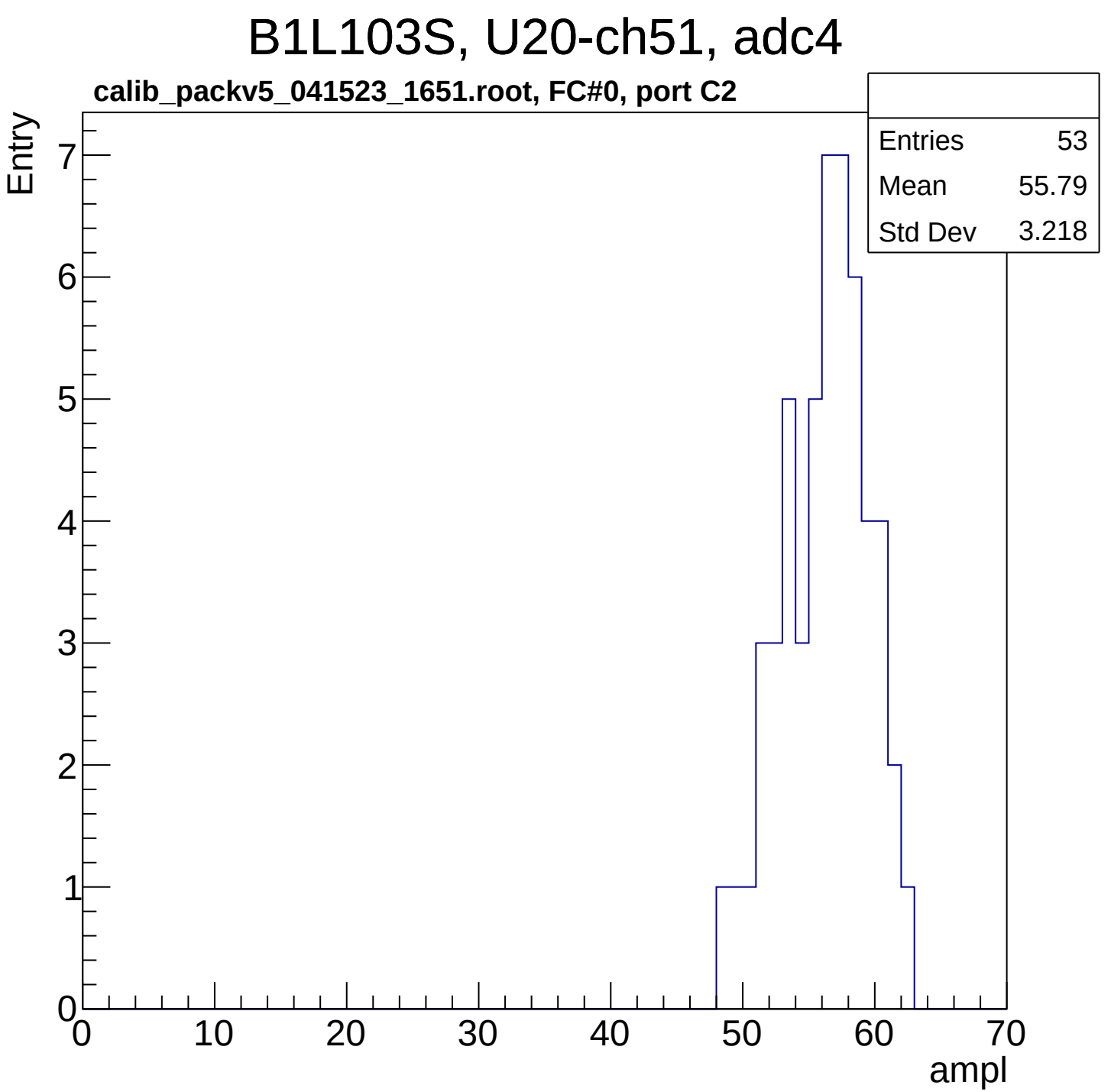
B1L103S, U20-ch51, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 55.79
Std Dev 3.218
Entry
ampl
0
1
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4
5
6
7
0
10
20
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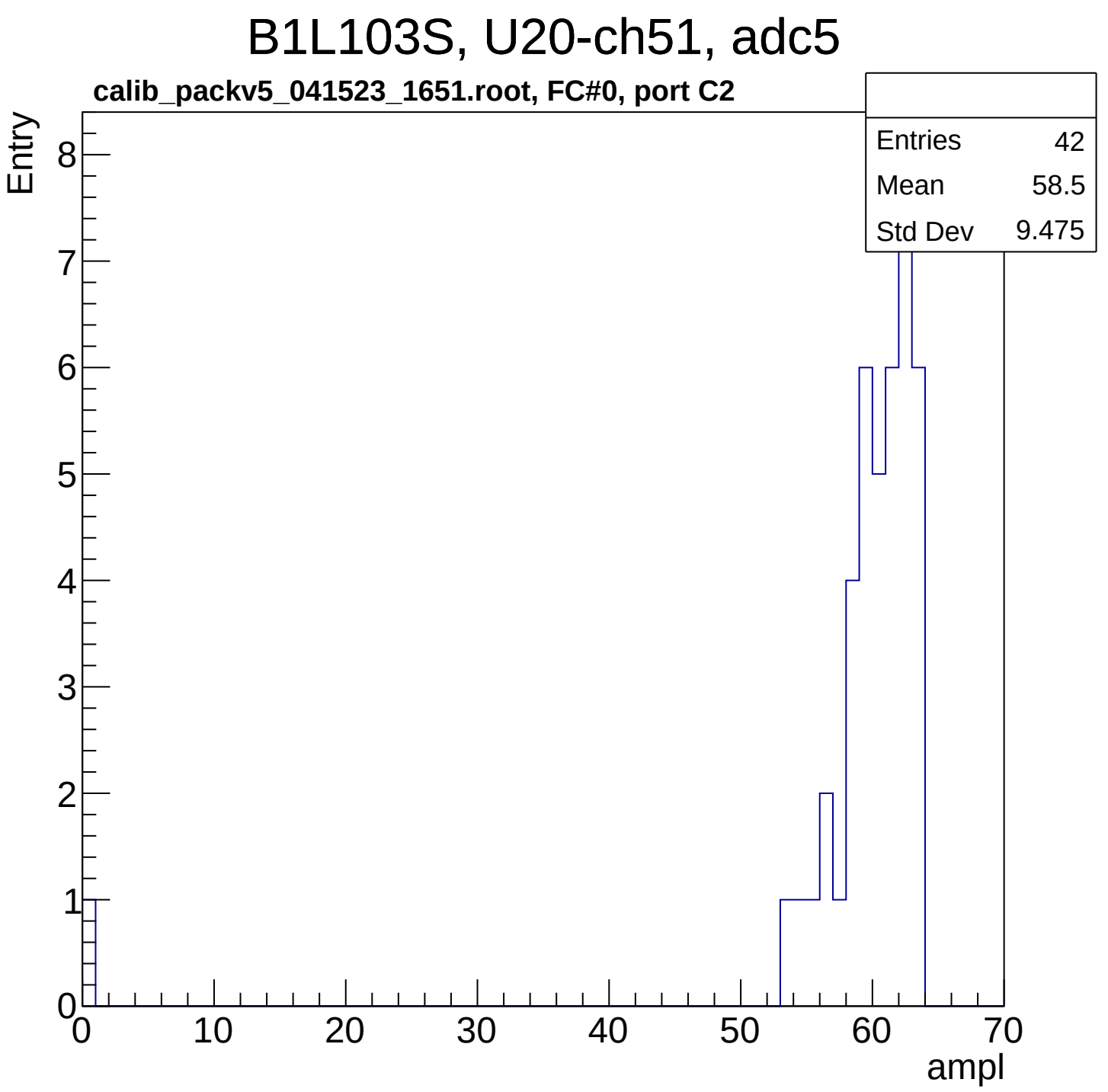
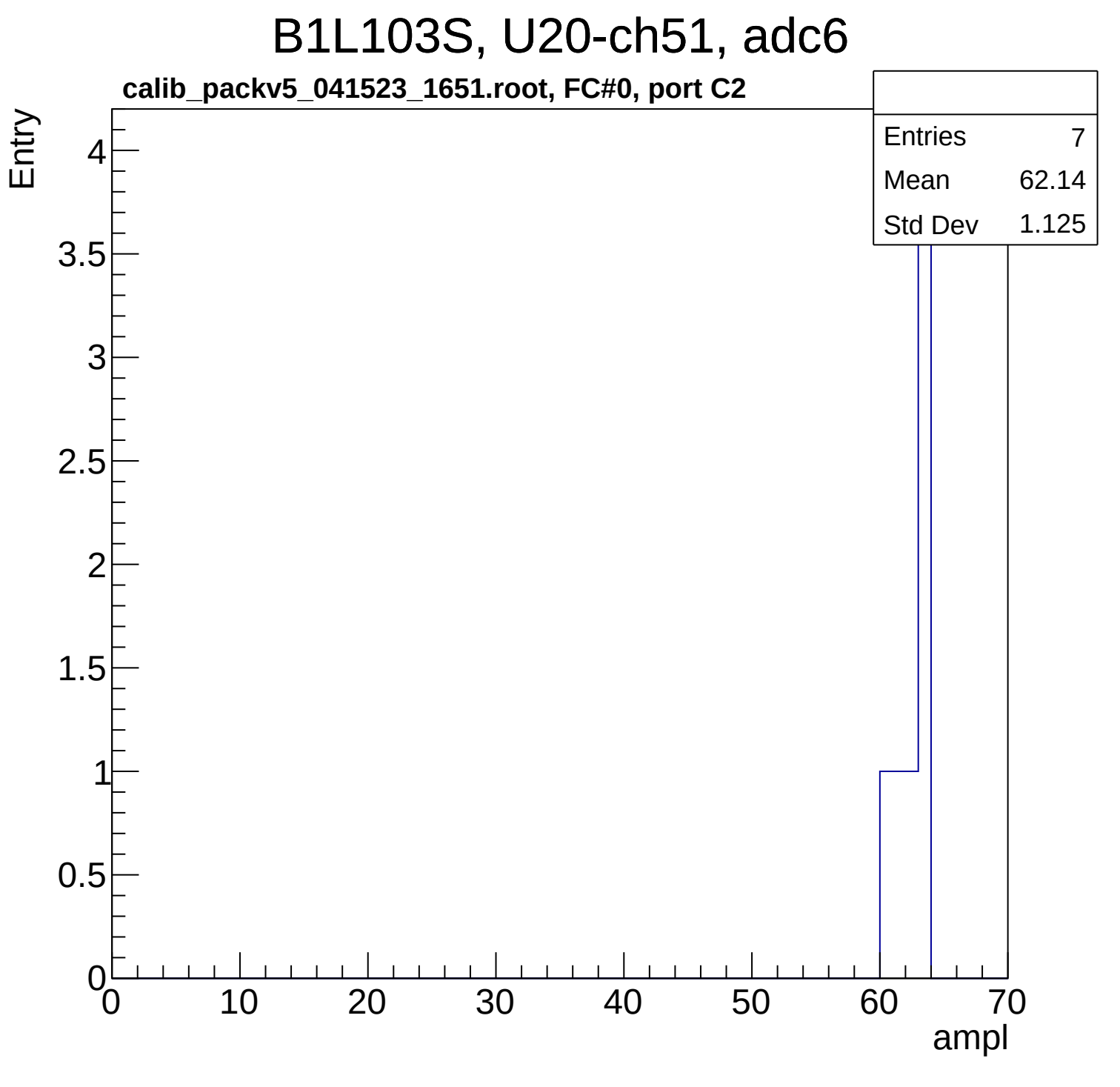
40
50
60
70


B1L103S, U20-ch51, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 58.5
Std Dev 9.475
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch51, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 62.14
Std Dev 1.125
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
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20
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60
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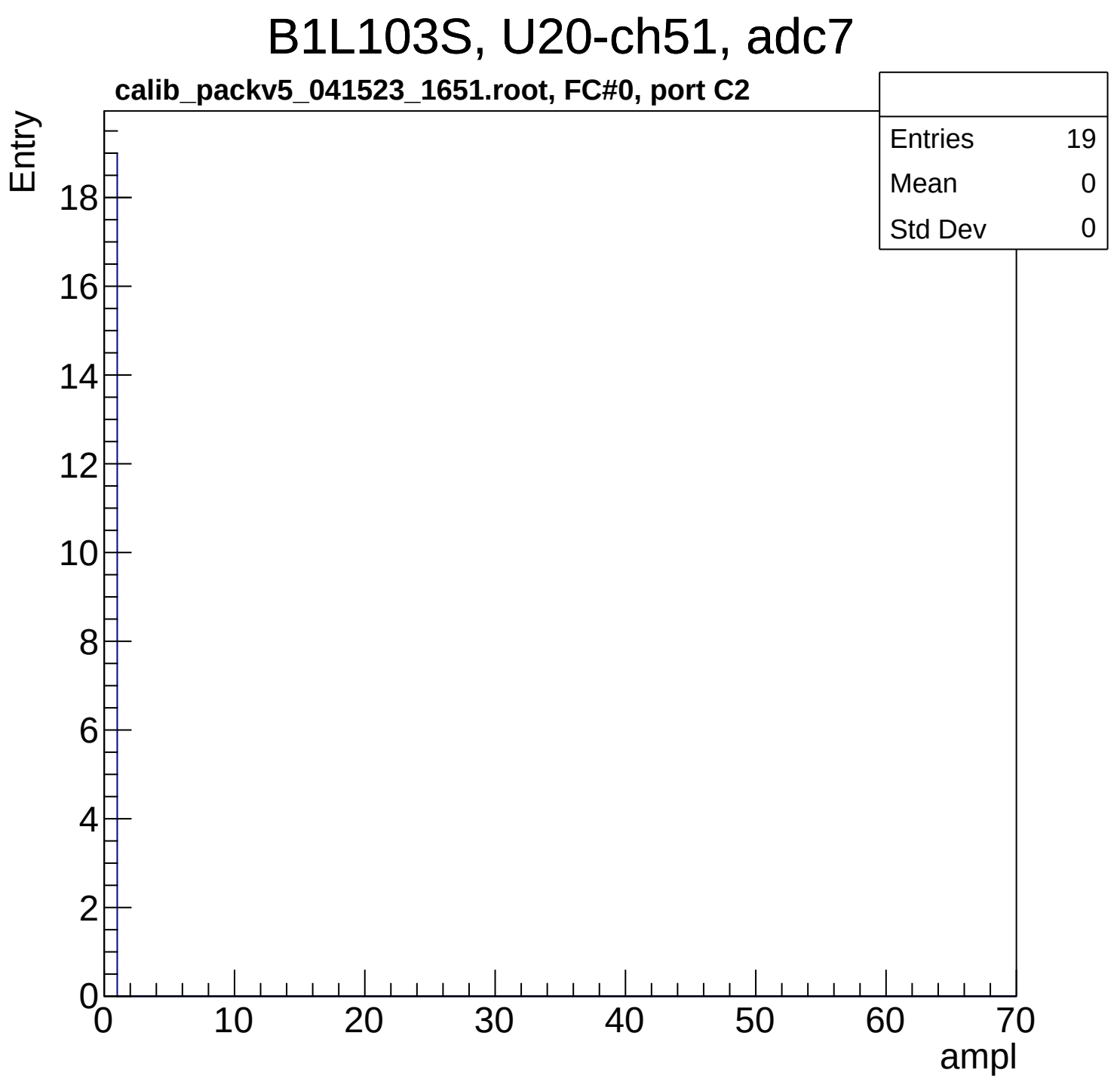
B1L103S, U20-ch51, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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2
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6
8
10
12
14
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18
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10
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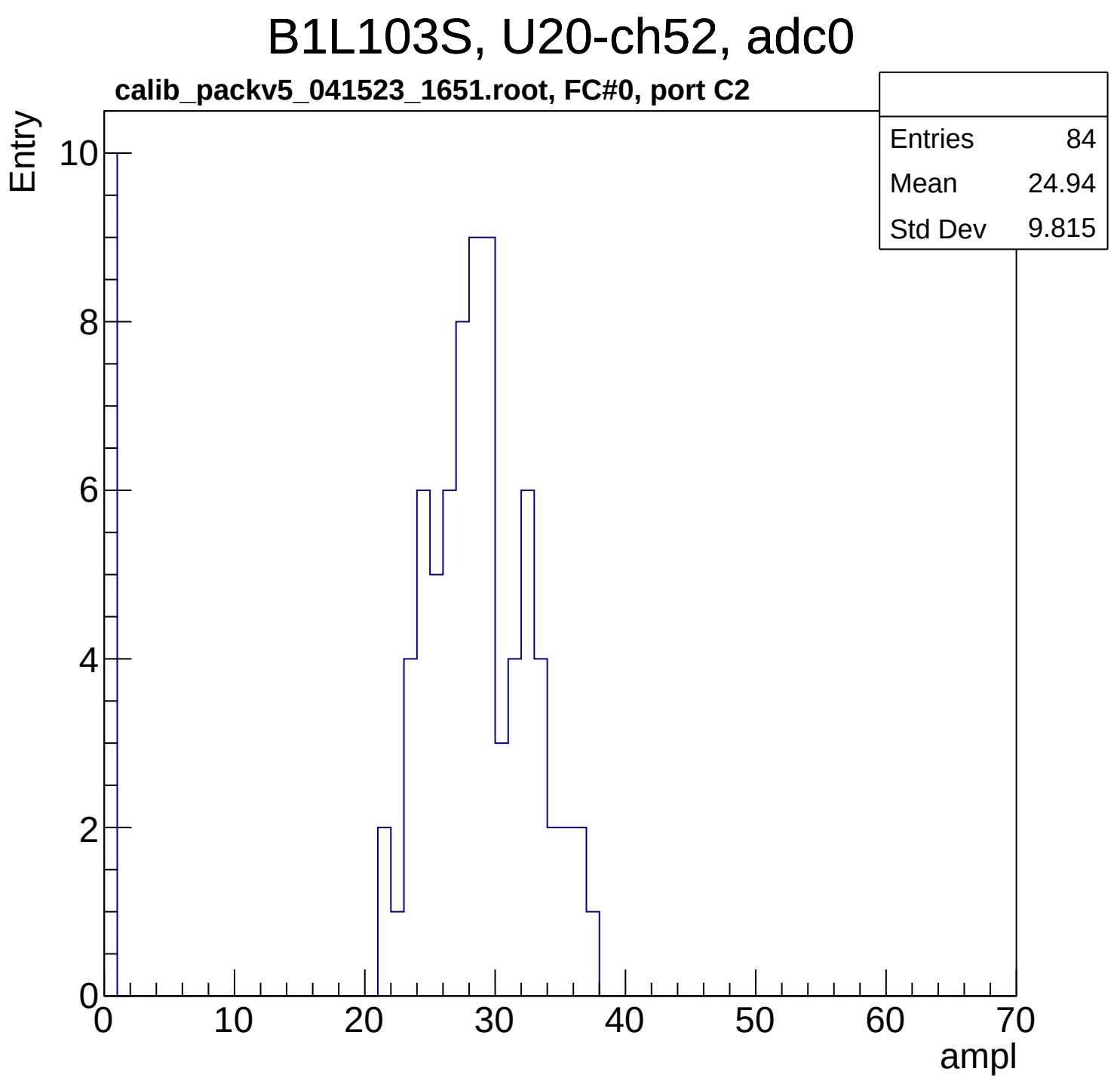
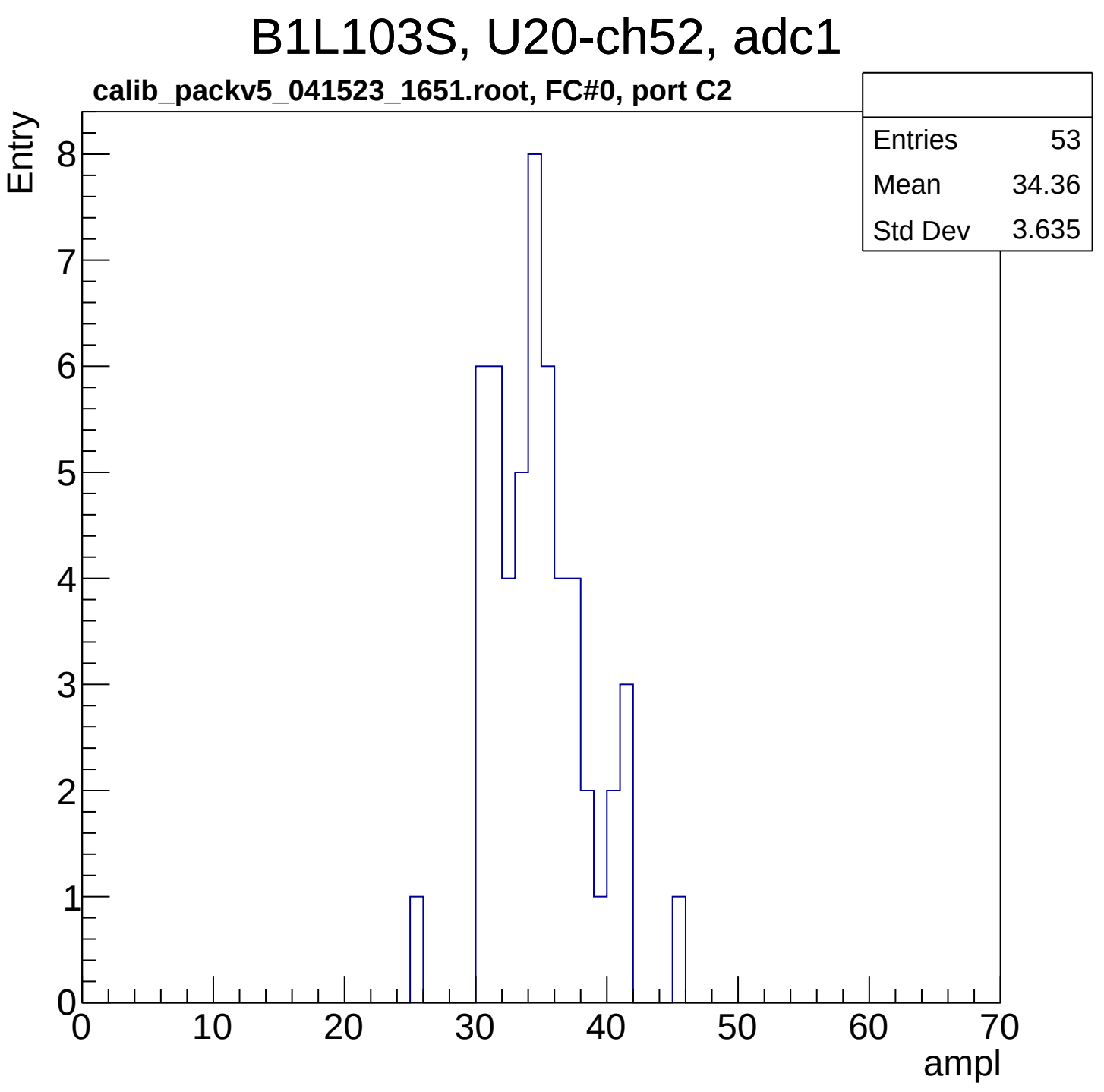
50
60
70
ampl


B1L103S, U20-ch52, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 24.94
Std Dev 9.815
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch52, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 34.36
Std Dev 3.635
Entry
ampl
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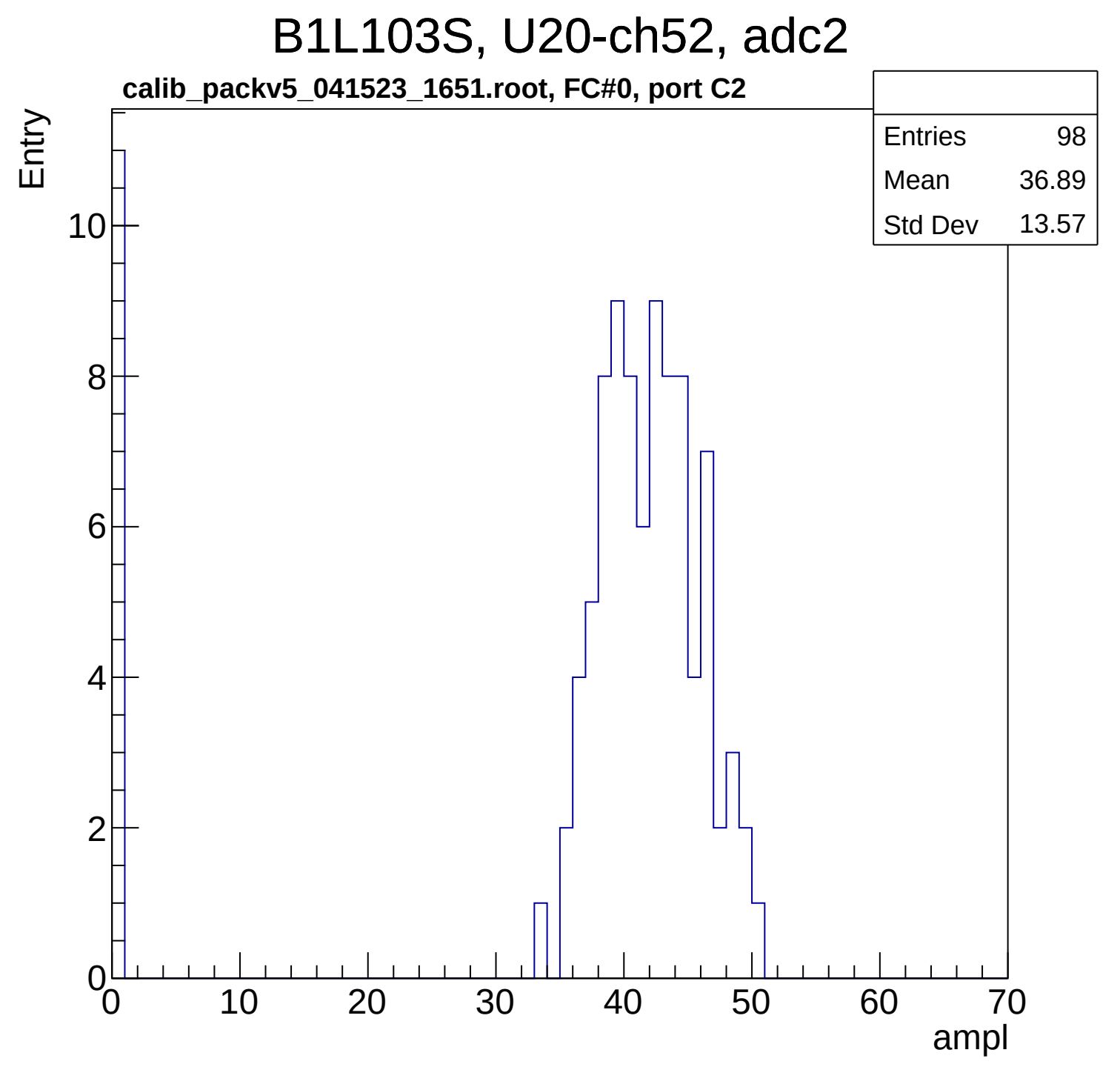
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch52, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 98
Mean 36.89
Std Dev 13.57
Entry
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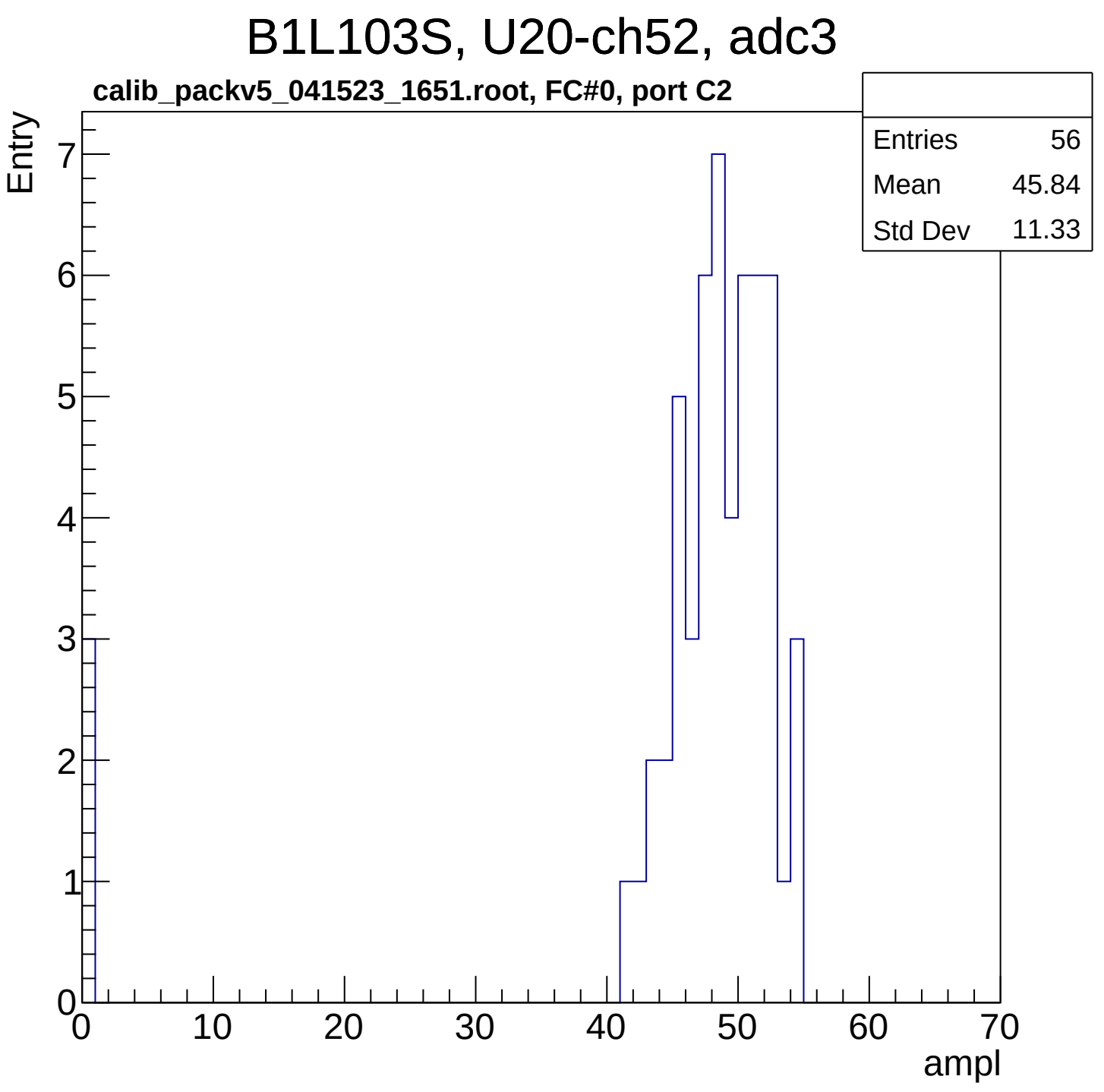
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch52, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 45.84
Std Dev 11.33
Entry
ampl
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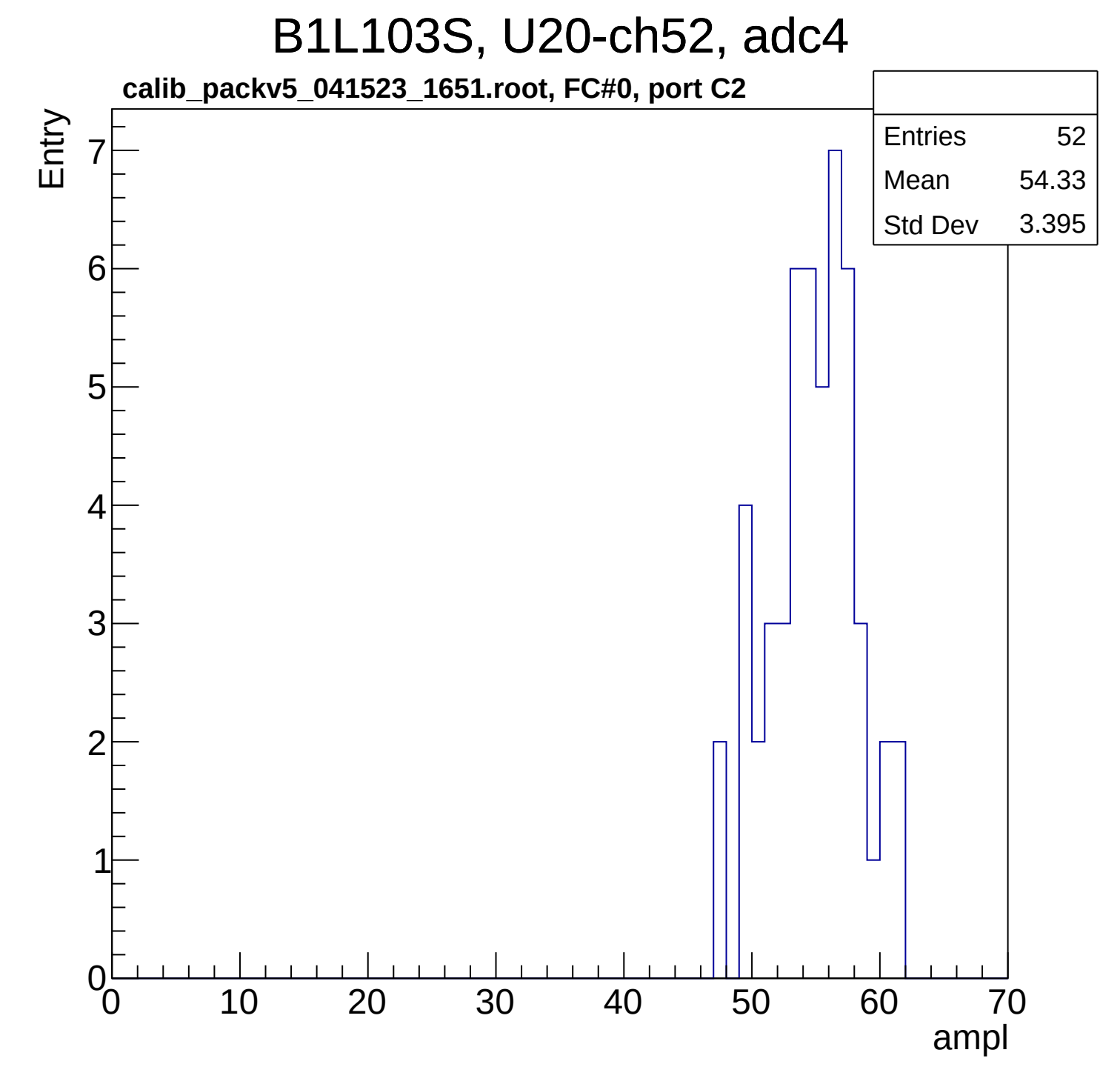
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U20-ch52, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 54.33
Std Dev 3.395
Entry
ampl
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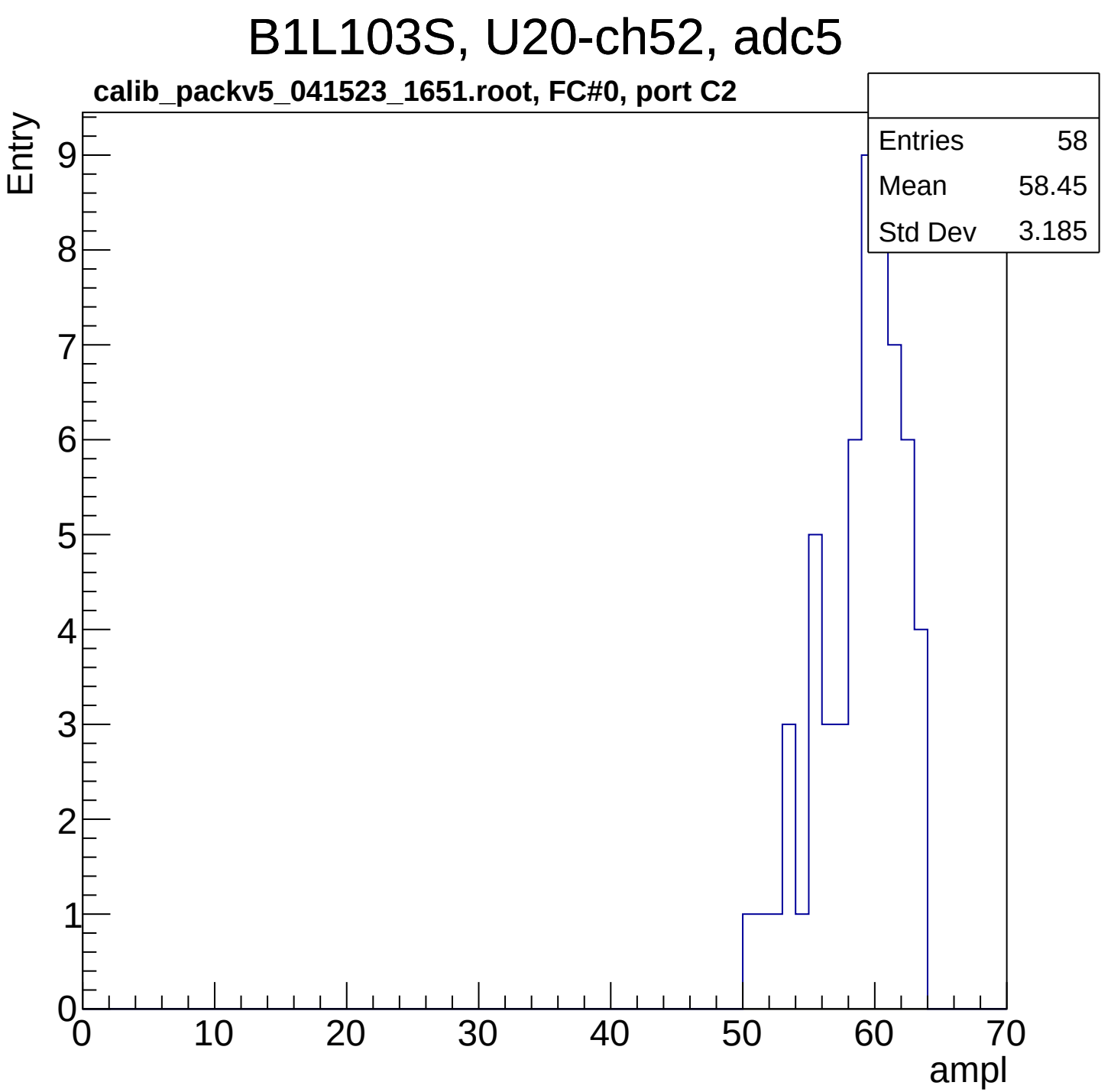
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U20-ch52, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 58.45
Std Dev 3.185
Entry
ampl
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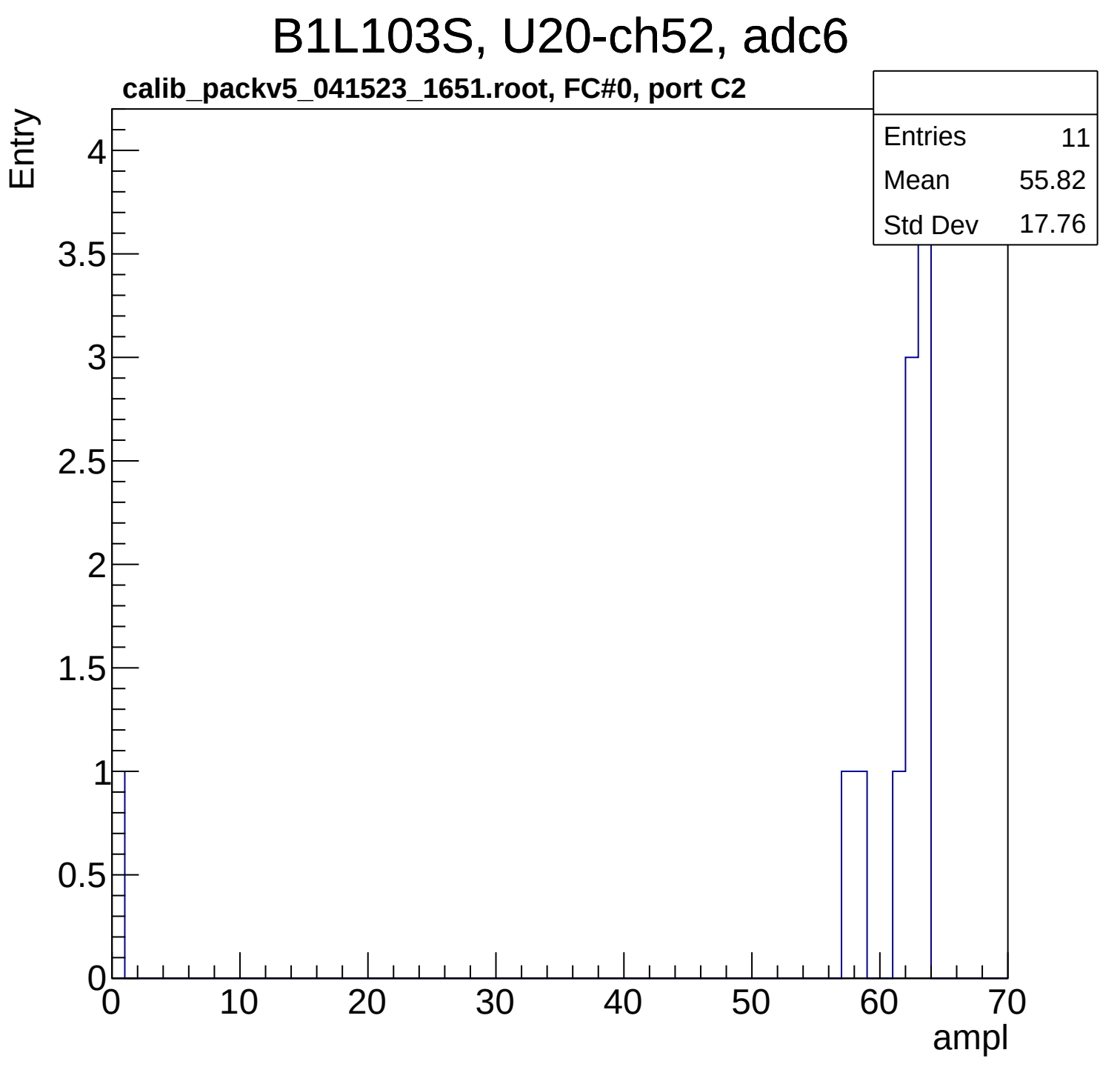
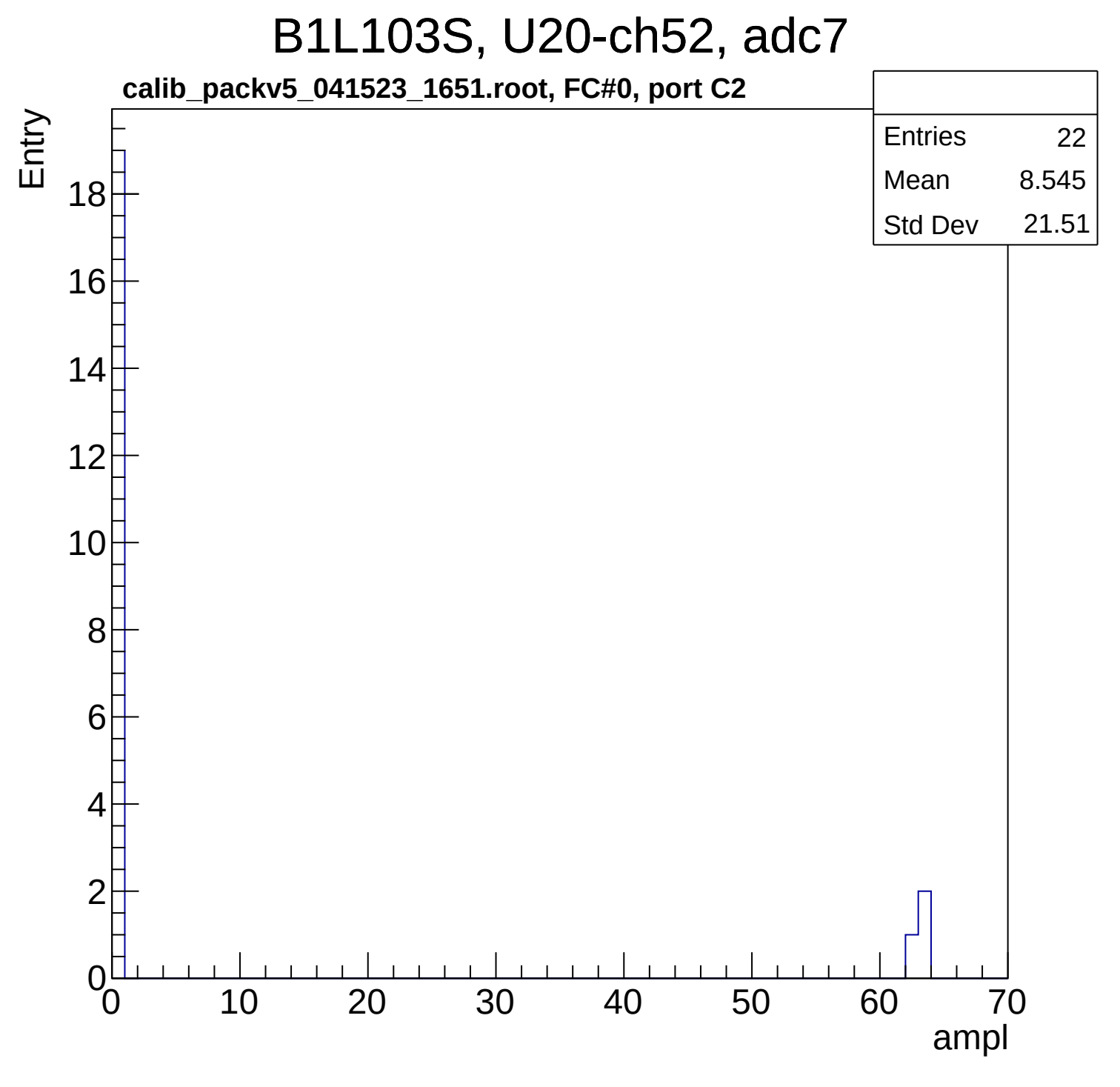
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch52, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 55.82
Std Dev 17.76
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U20-ch52, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.545
Std Dev 21.51
Entry
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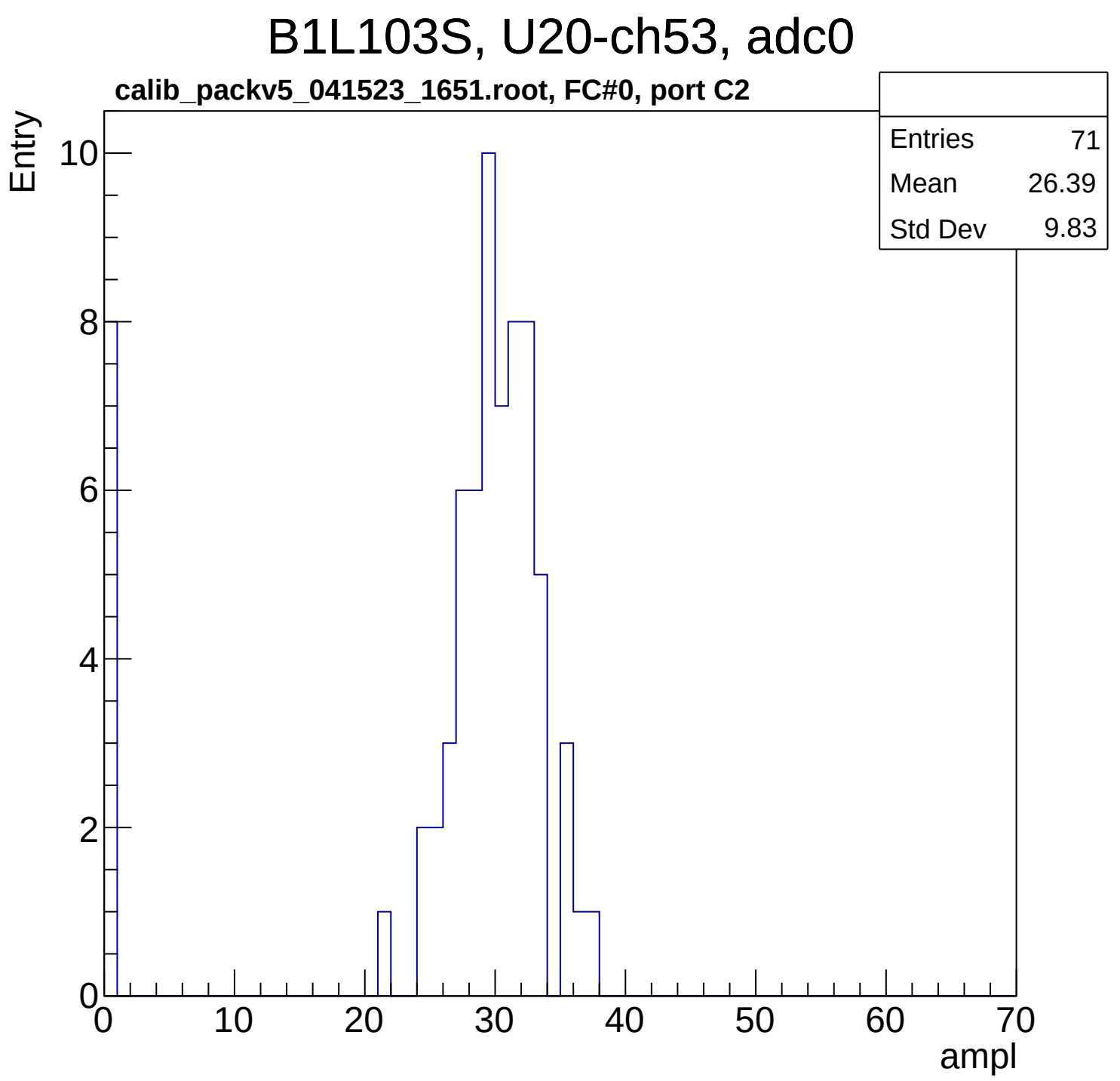
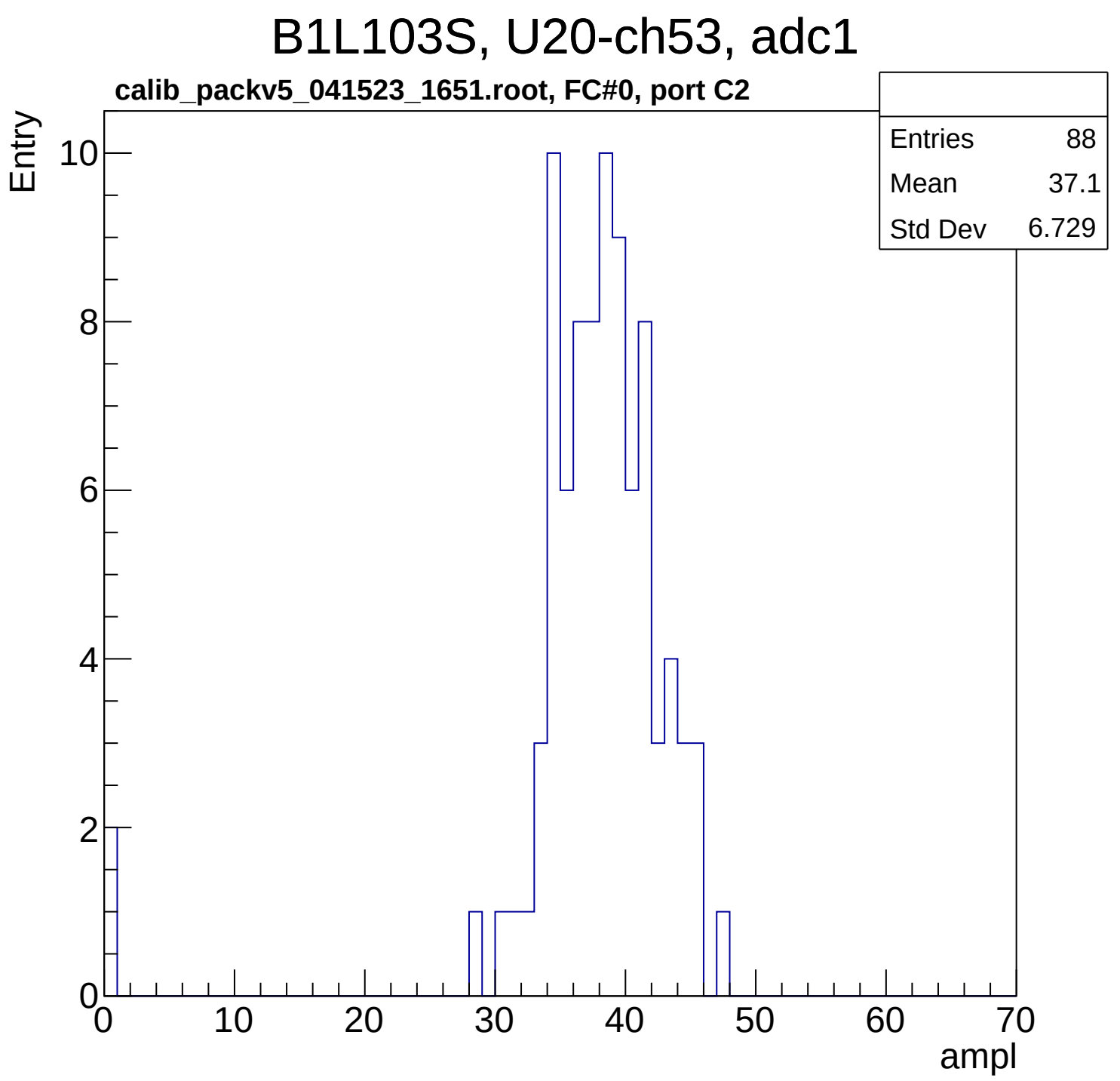
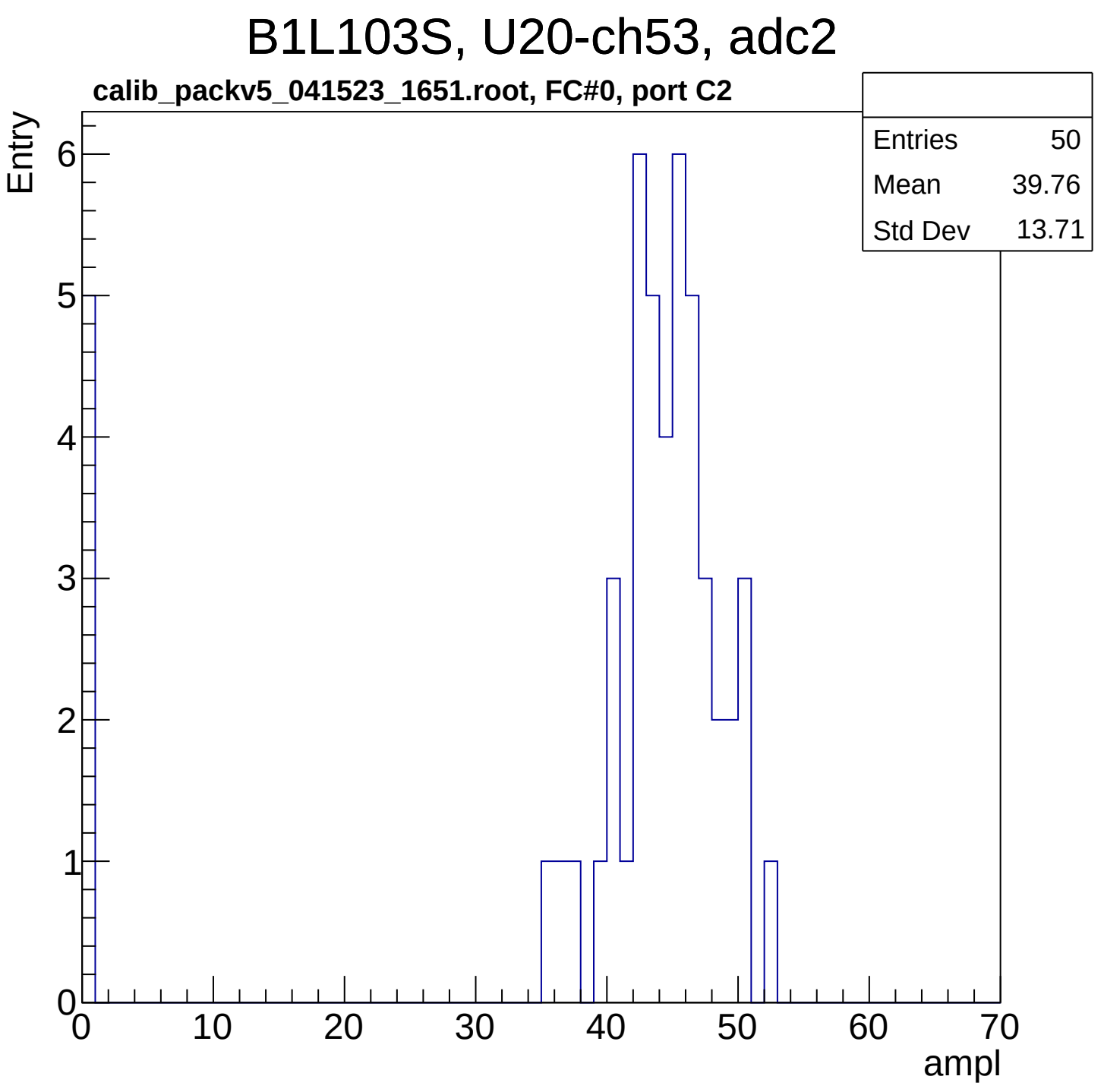
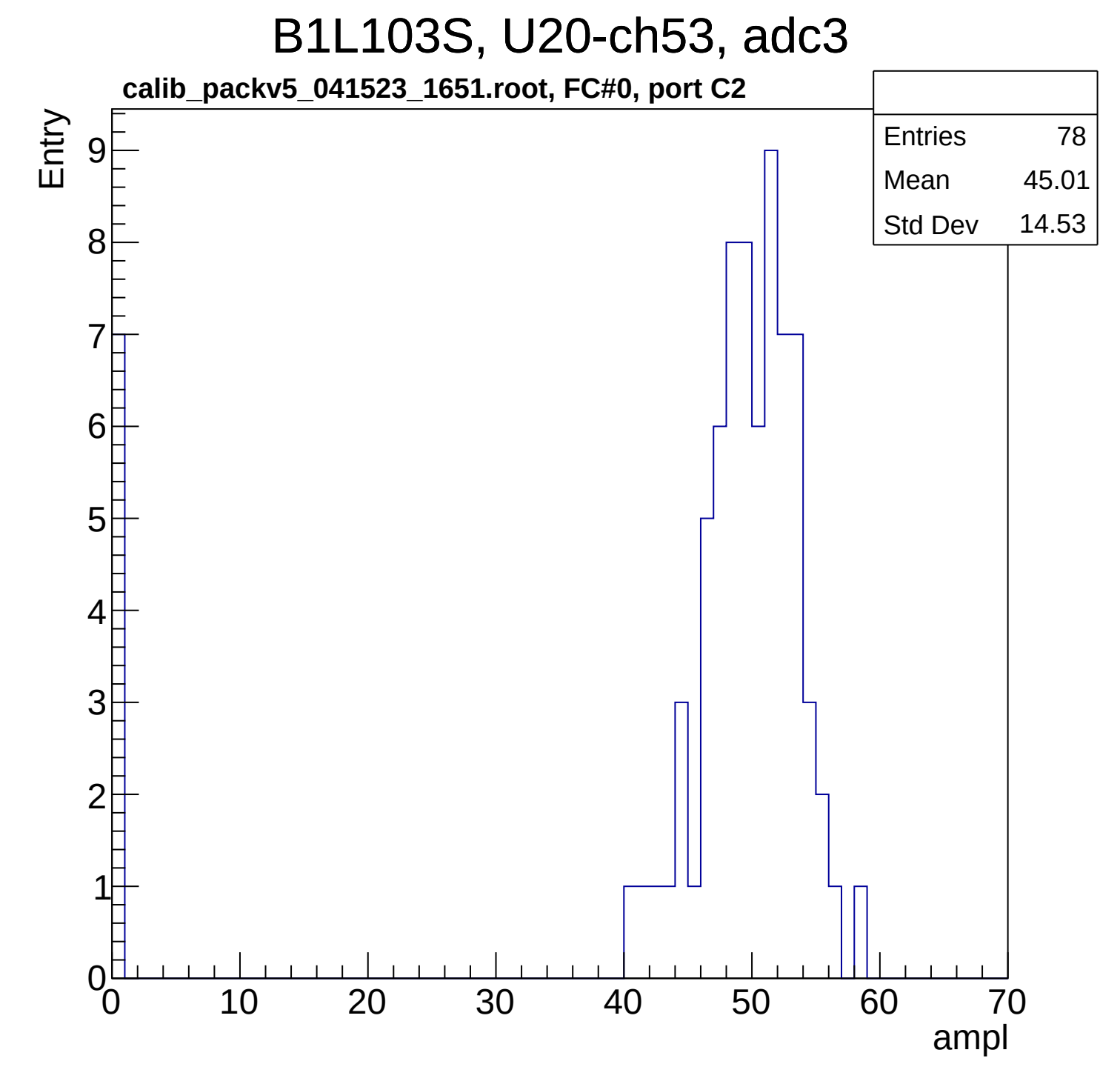
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch53, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 26.39
Std Dev 9.83
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch53, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 37.1
Std Dev 6.729
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U20-ch53, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 39.76
Std Dev 13.71
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch53, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 45.01
Std Dev 14.53
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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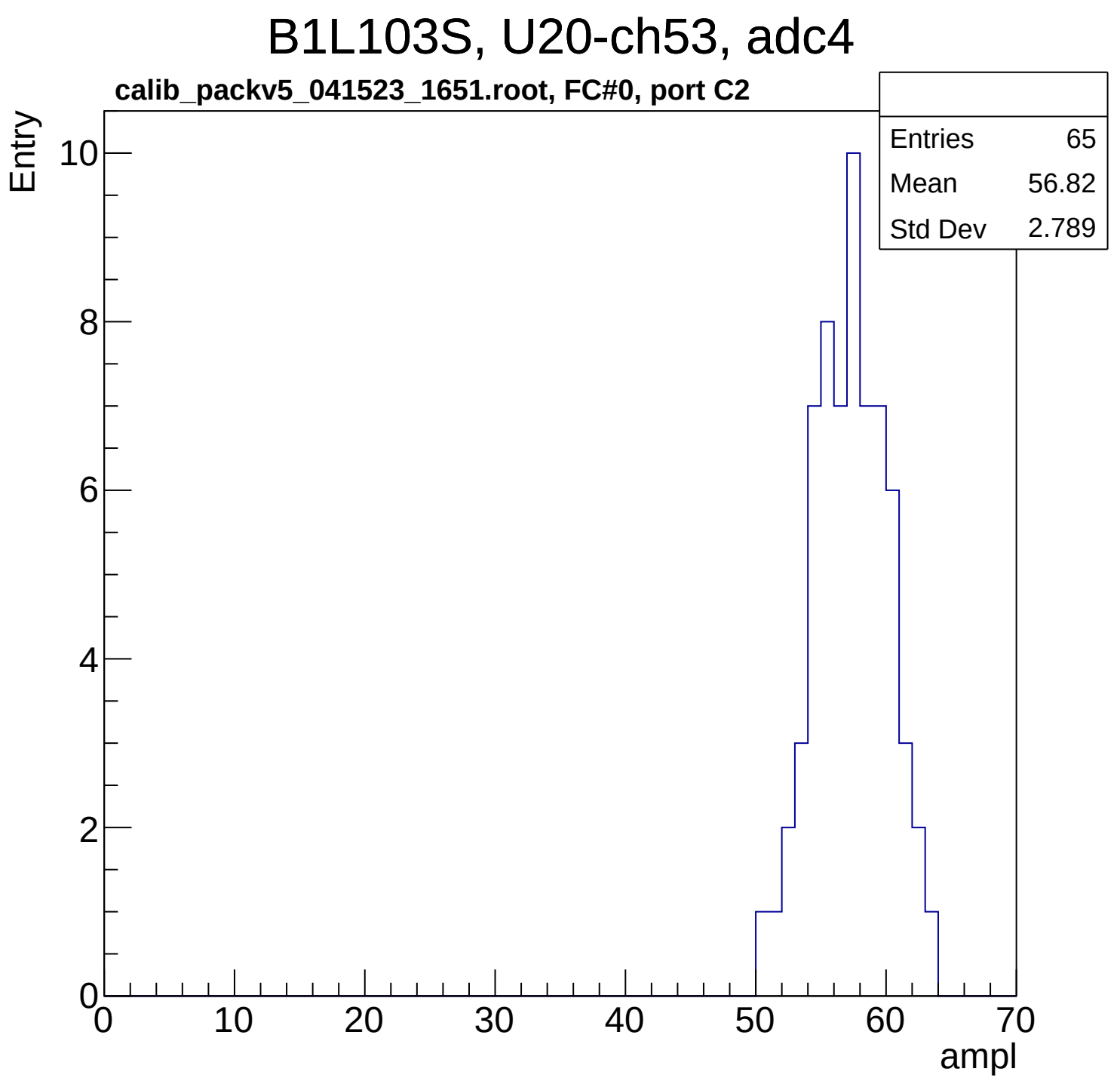
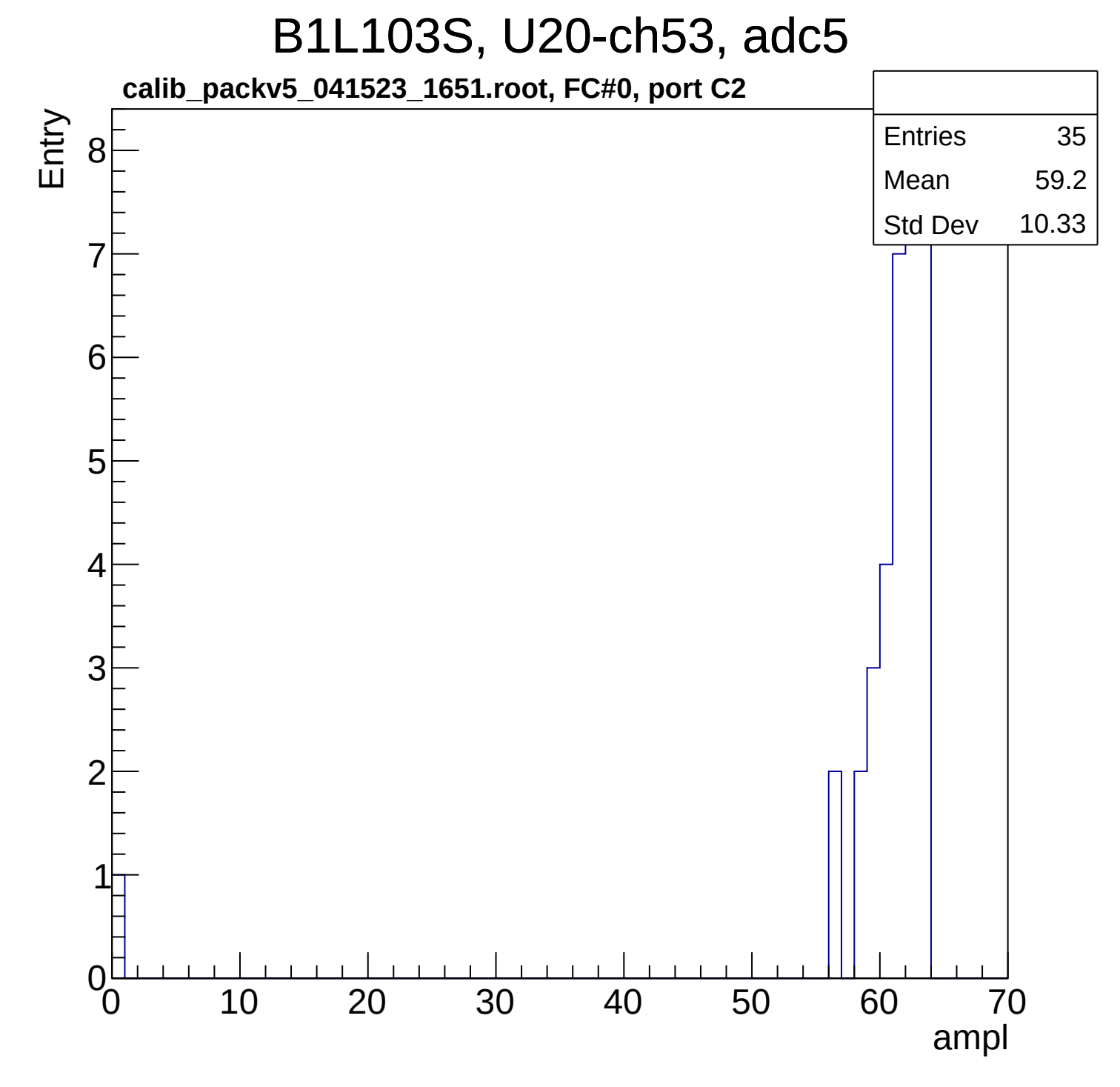
40
50
60
70


B1L103S, U20-ch53, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 56.82
Std Dev 2.789
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U20-ch53, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 59.2
Std Dev 10.33
Entry
ampl
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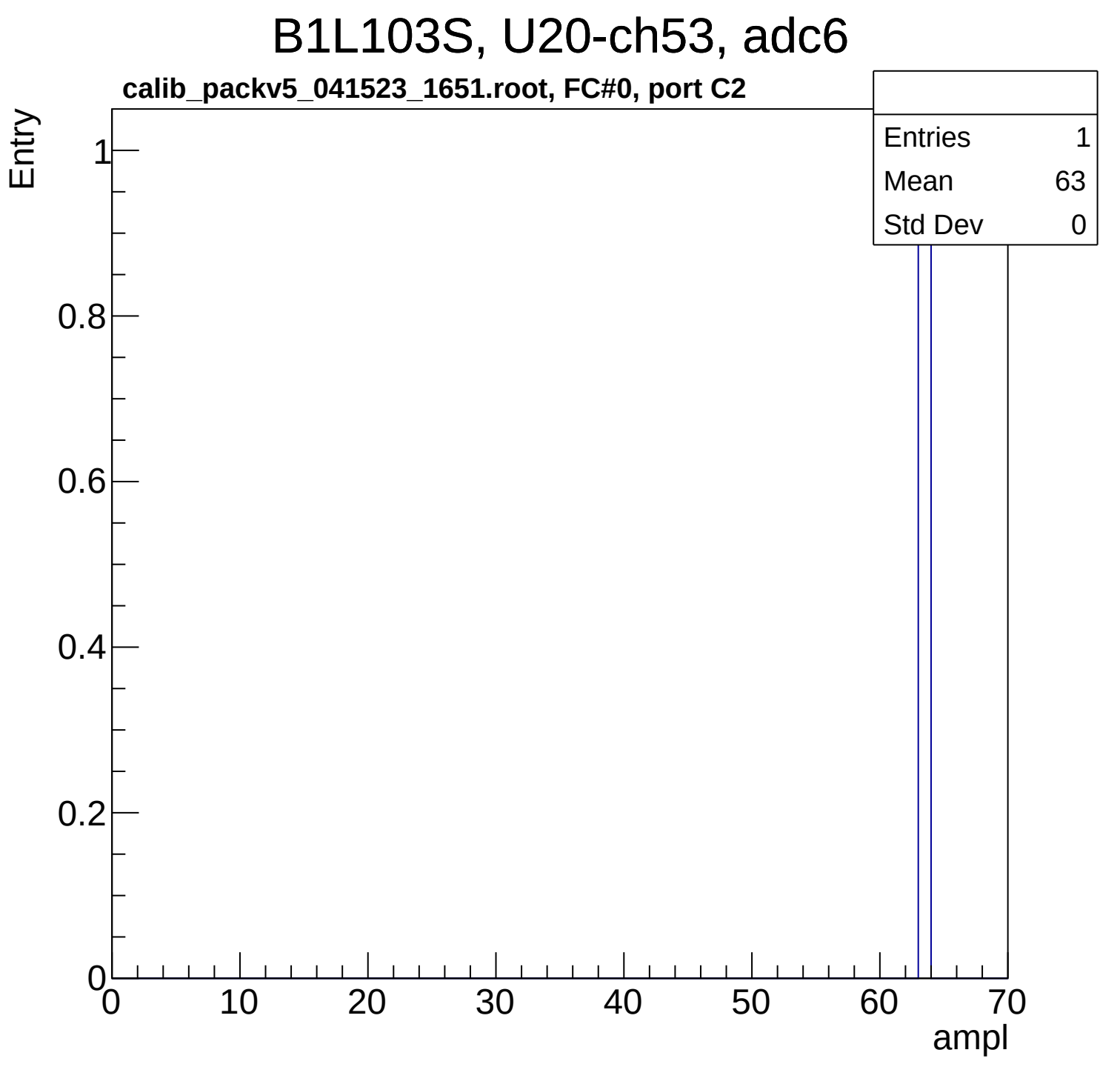
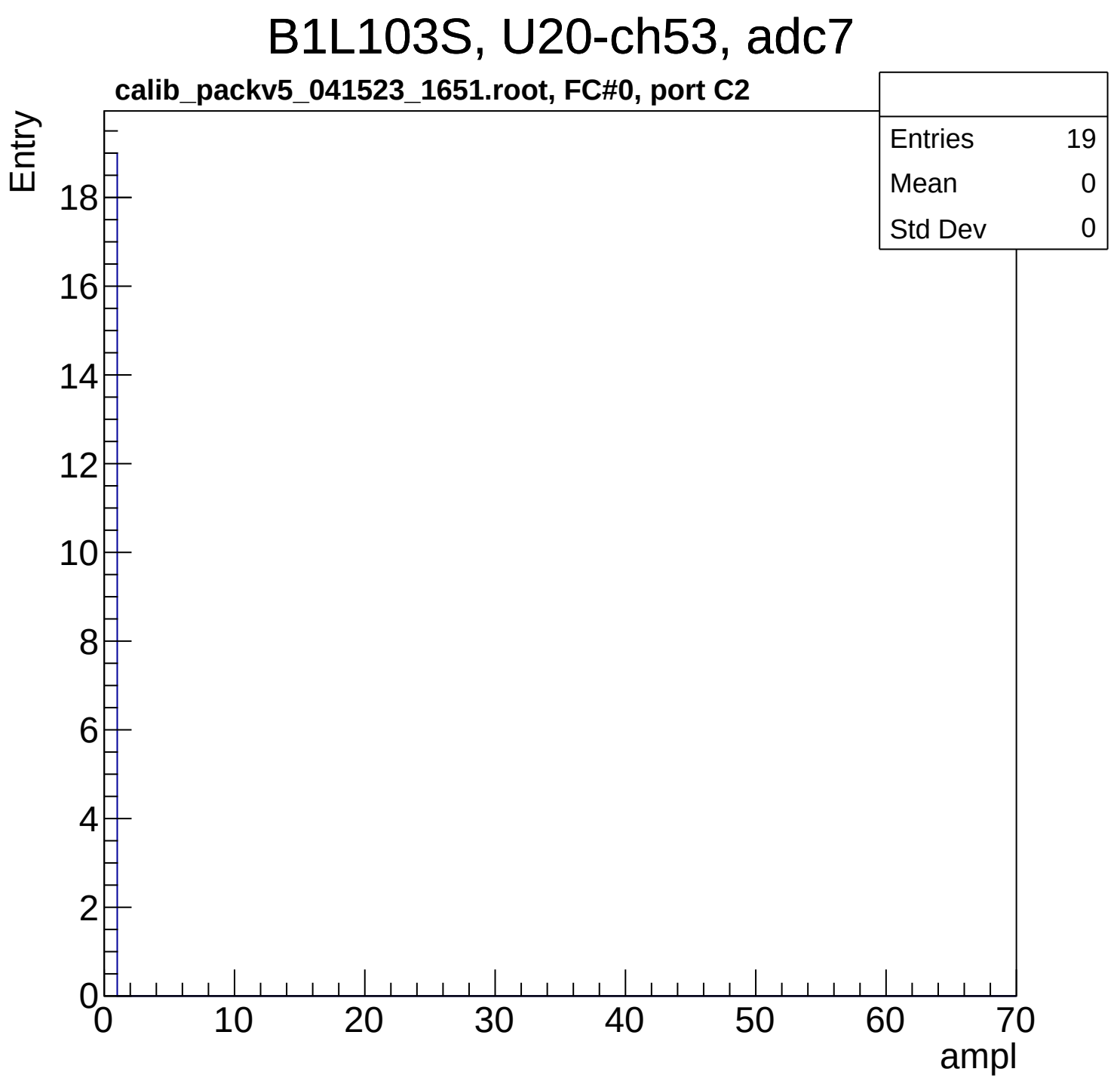
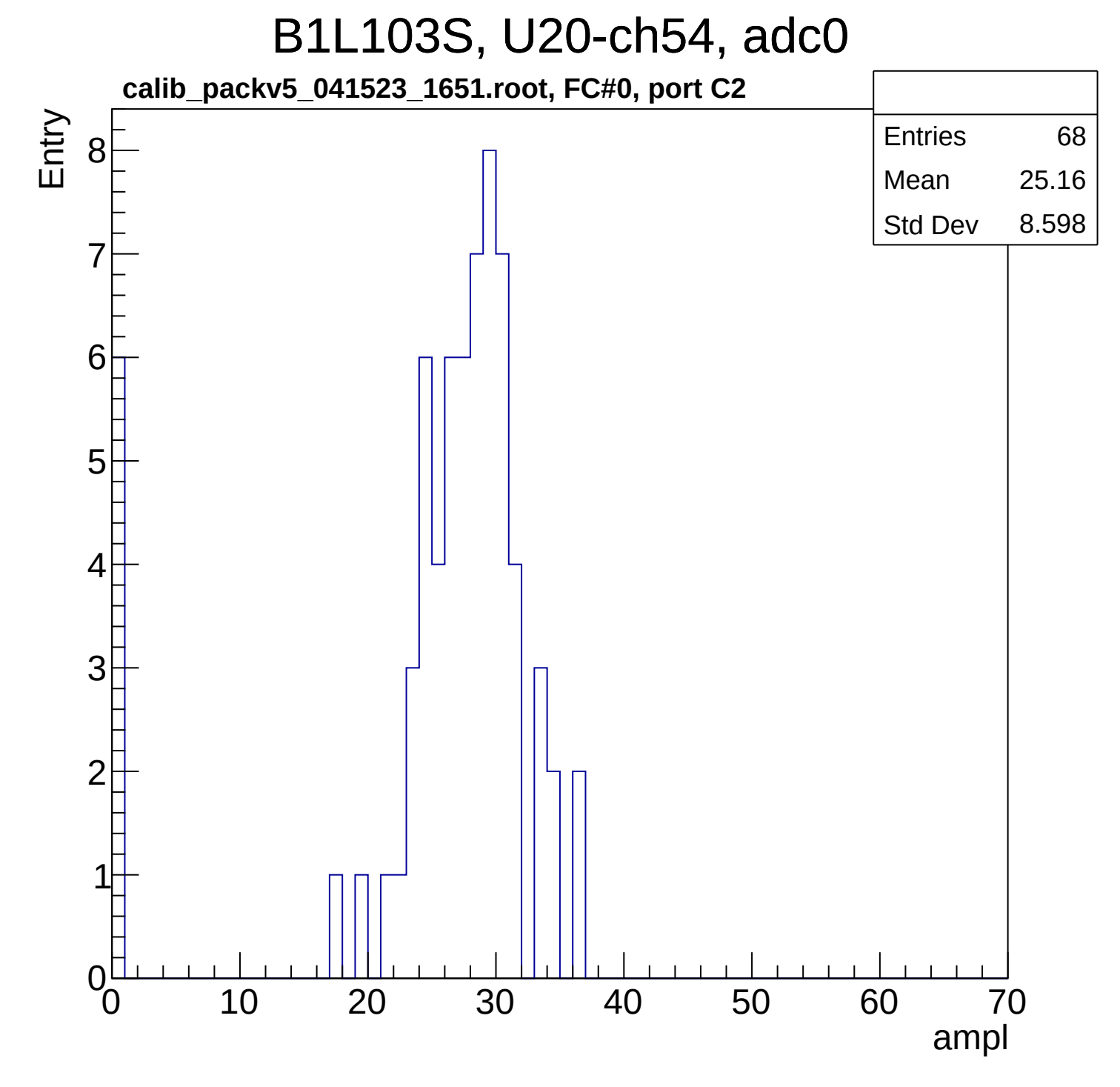
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch53, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch53, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch54, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 25.16
Std Dev 8.598
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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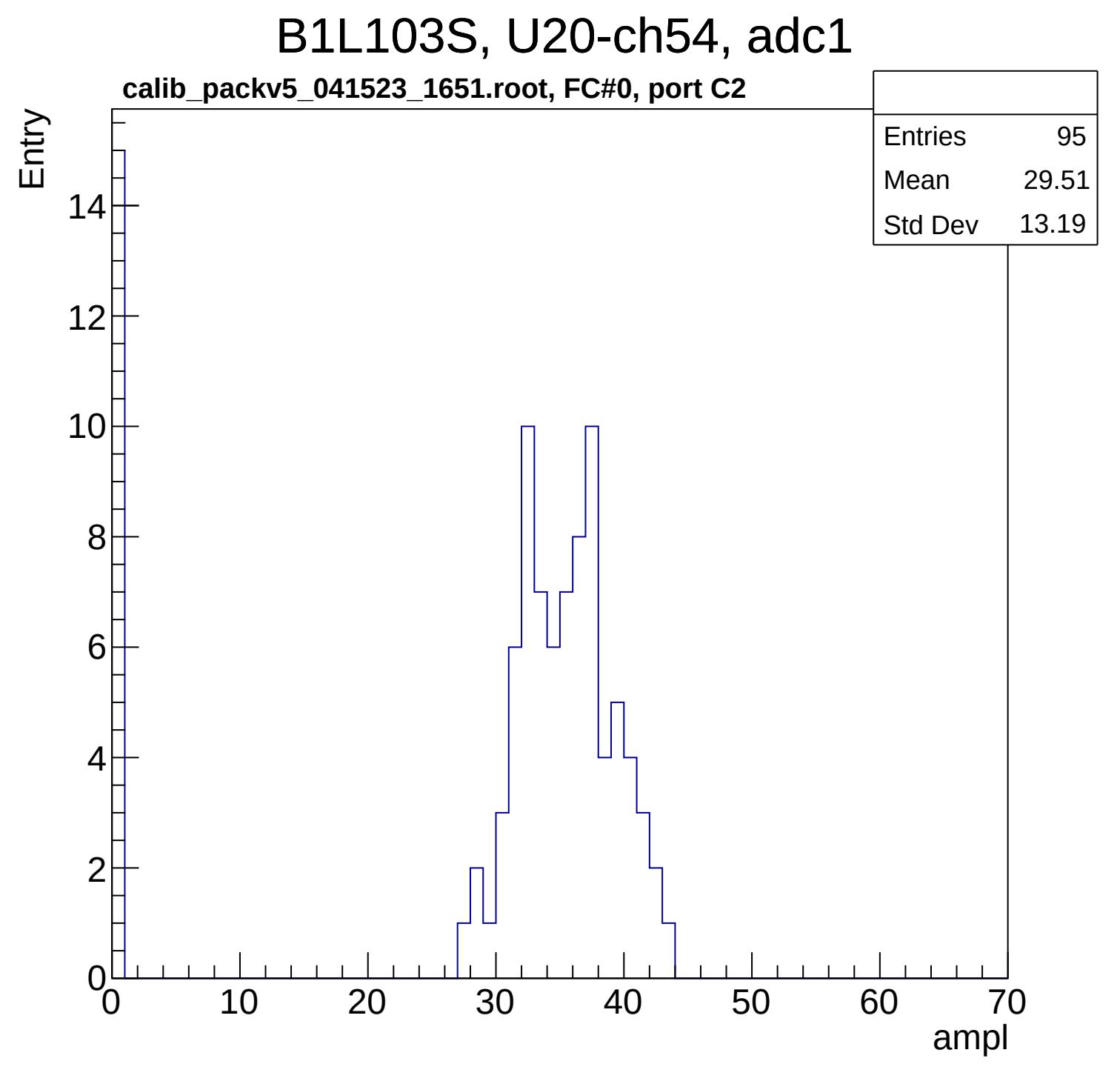
40
50
60
70


B1L103S, U20-ch54, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 29.51
Std Dev 13.19
Entry
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2
4
6
8
10
12
14
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10
20
30
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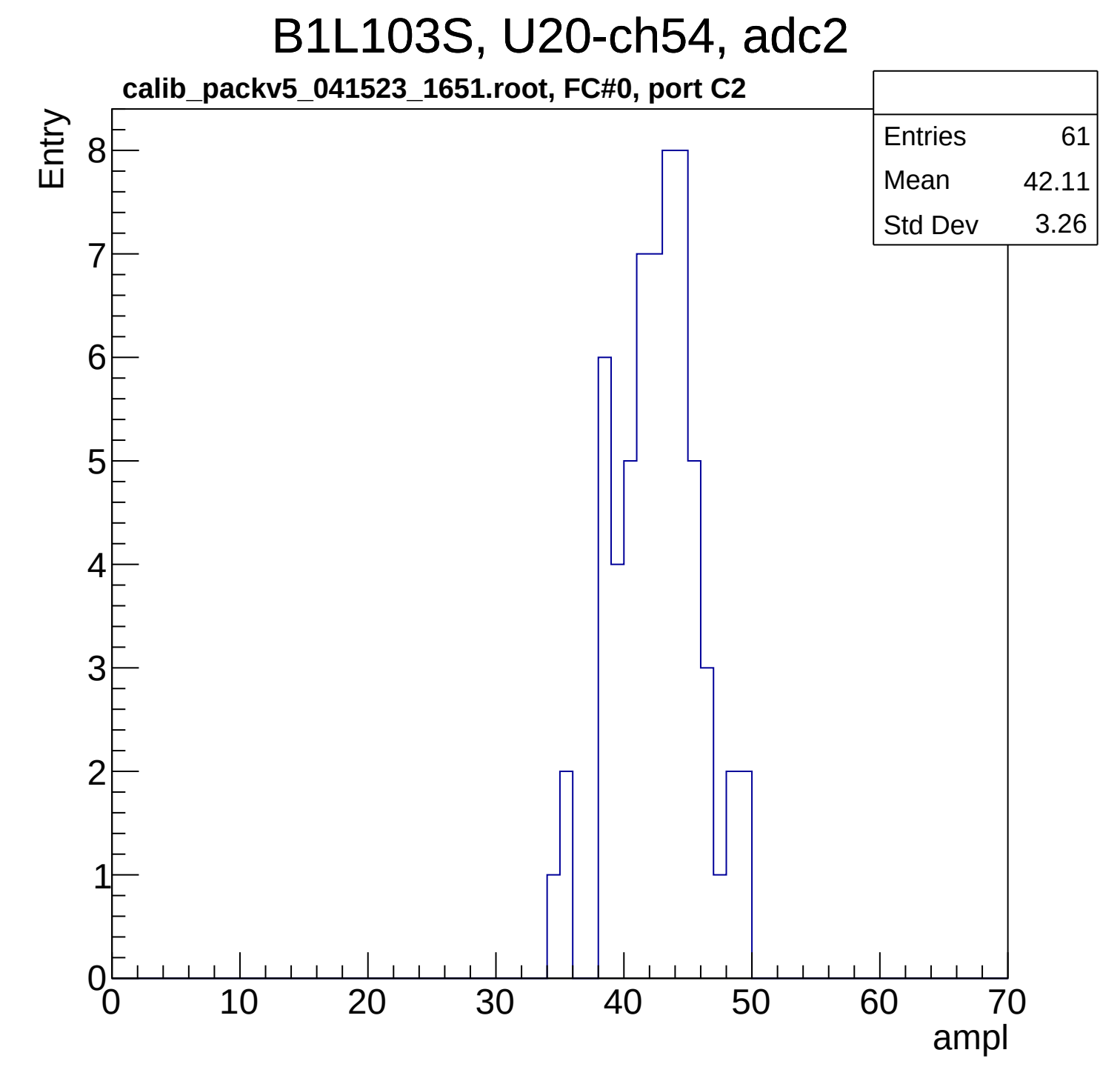
50
60
70
ampl


B1L103S, U20-ch54, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 42.11
Std Dev 3.26
Entry
ampl
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5
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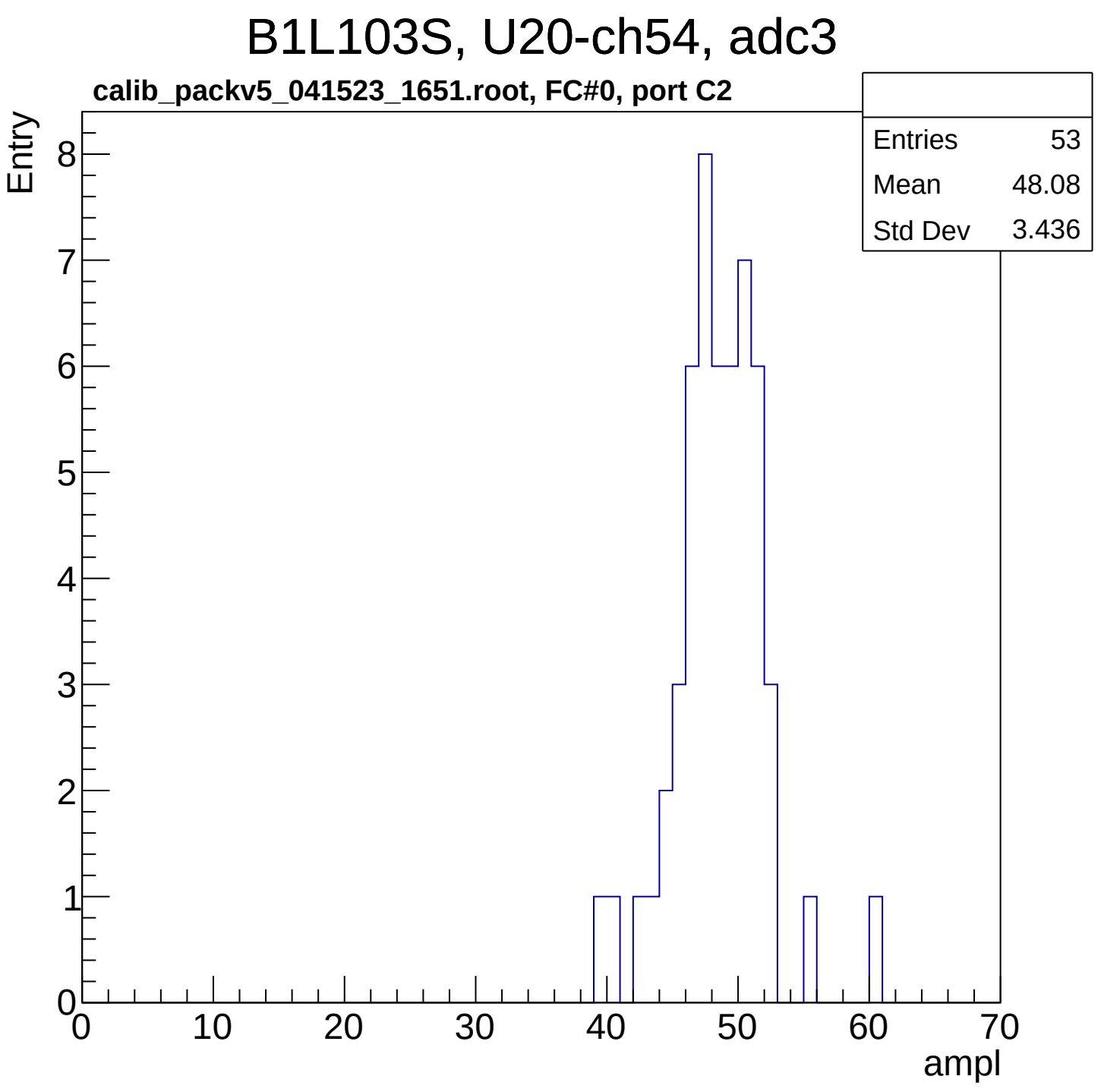
B1L103S, U20-ch54, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 48.08
Std Dev 3.436
Entry
ampl
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2
3
4
5
6
7
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0
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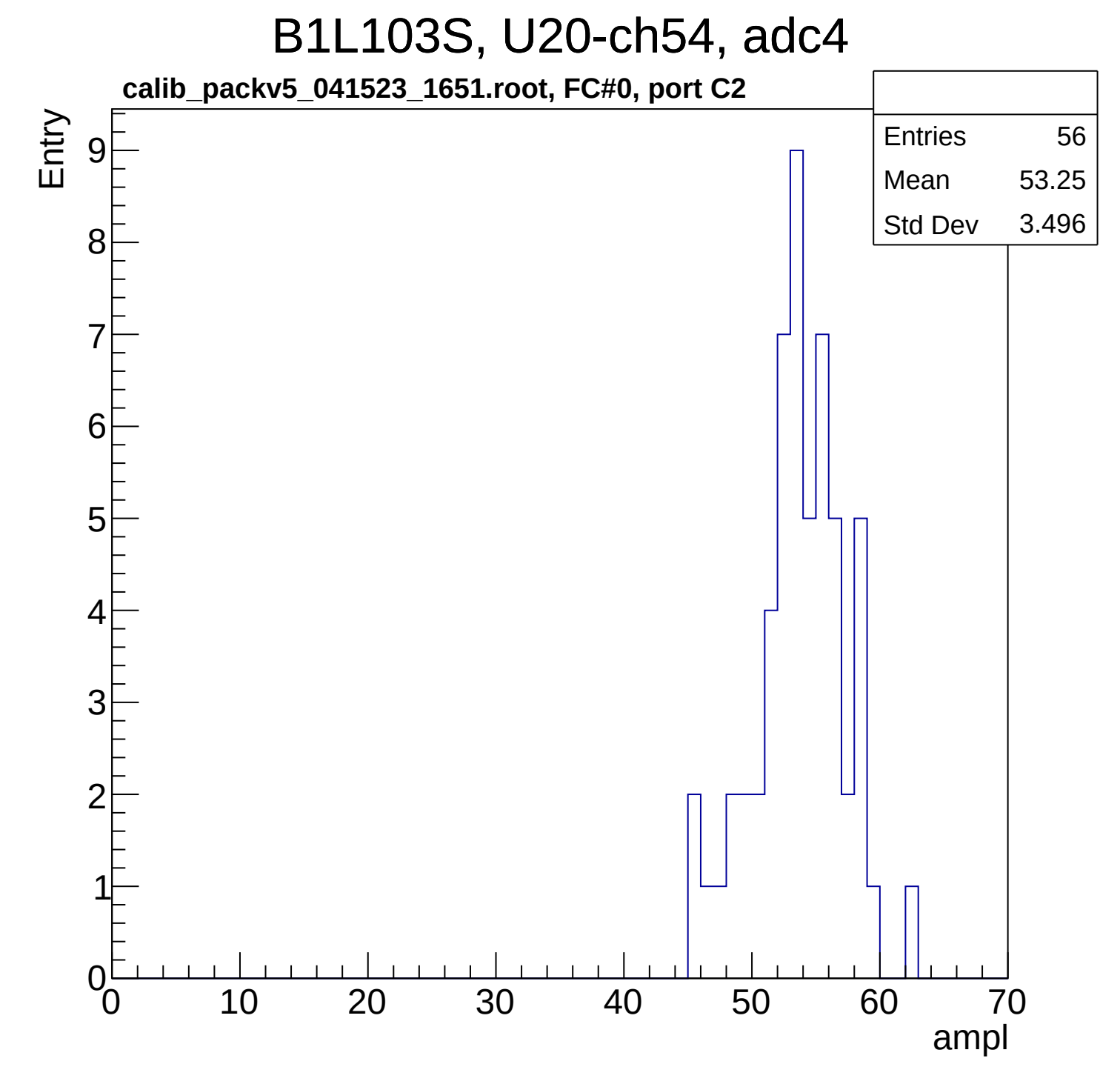
20
30
40
50
60
70


B1L103S, U20-ch54, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 53.25
Std Dev 3.496
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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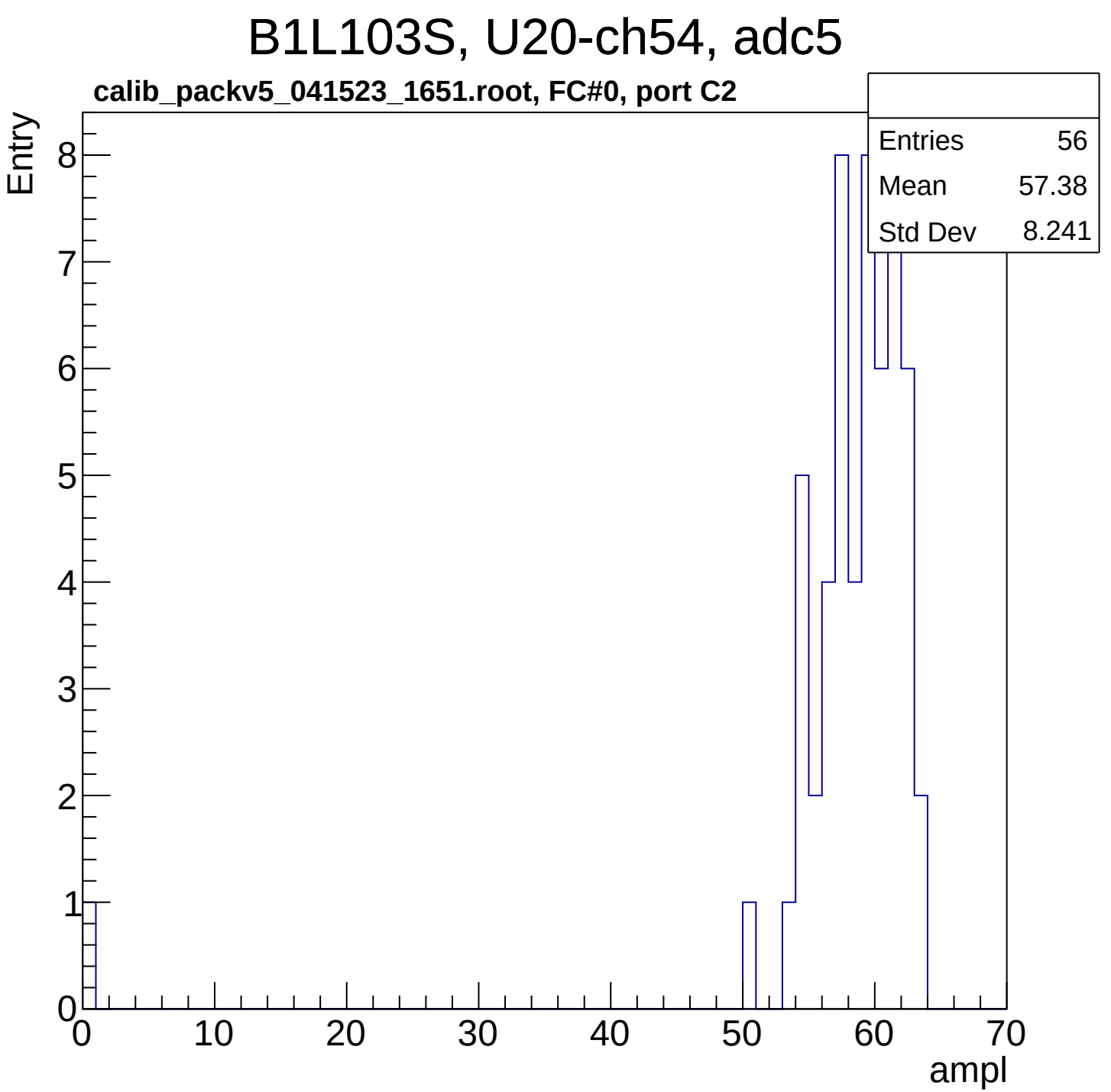
B1L103S, U20-ch54, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 57.38
Std Dev 8.241
Entry
ampl
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2
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5
6
7
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0
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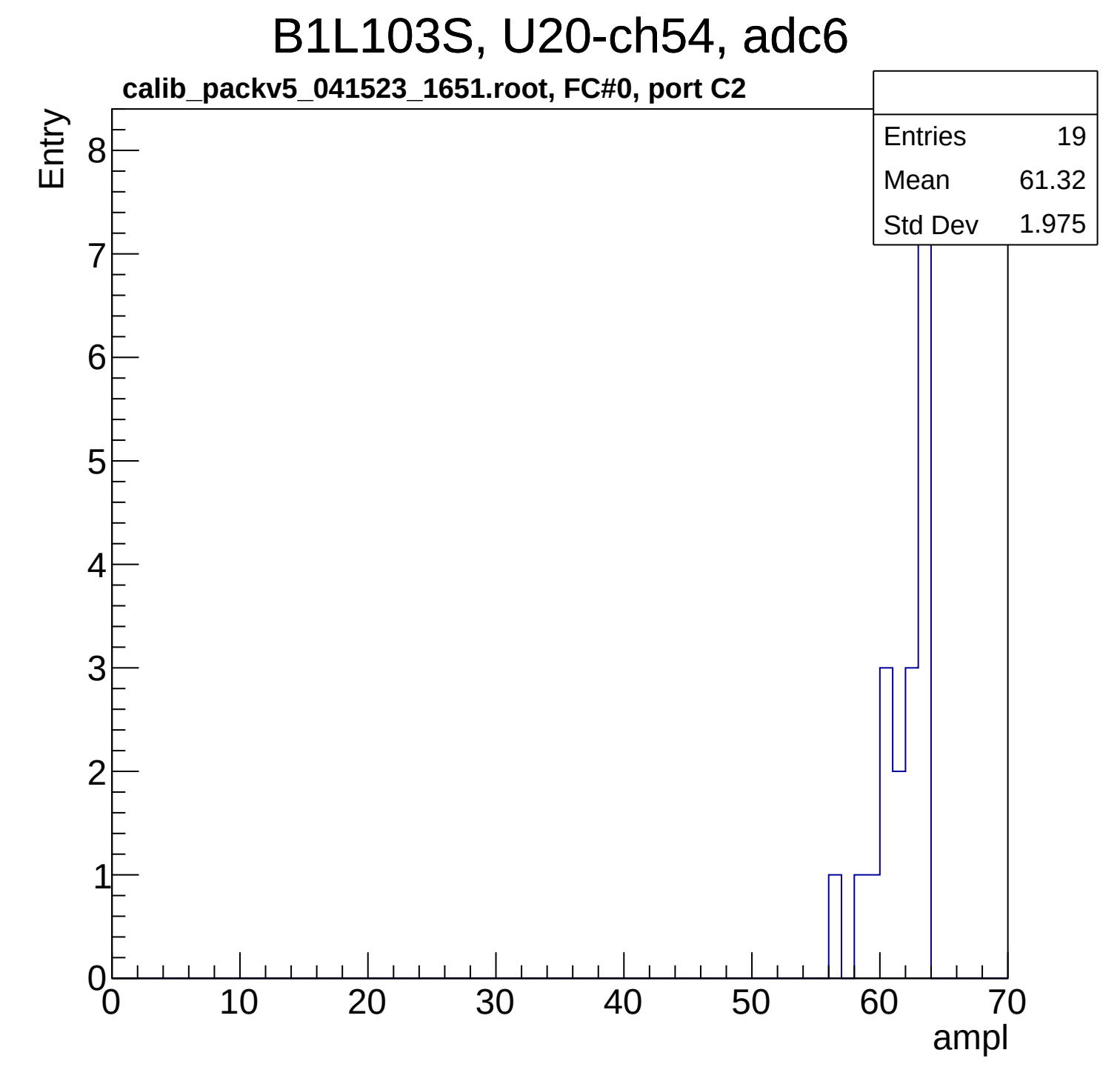
40
50
60
70


B1L103S, U20-ch54, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 61.32
Std Dev 1.975
Entry
ampl
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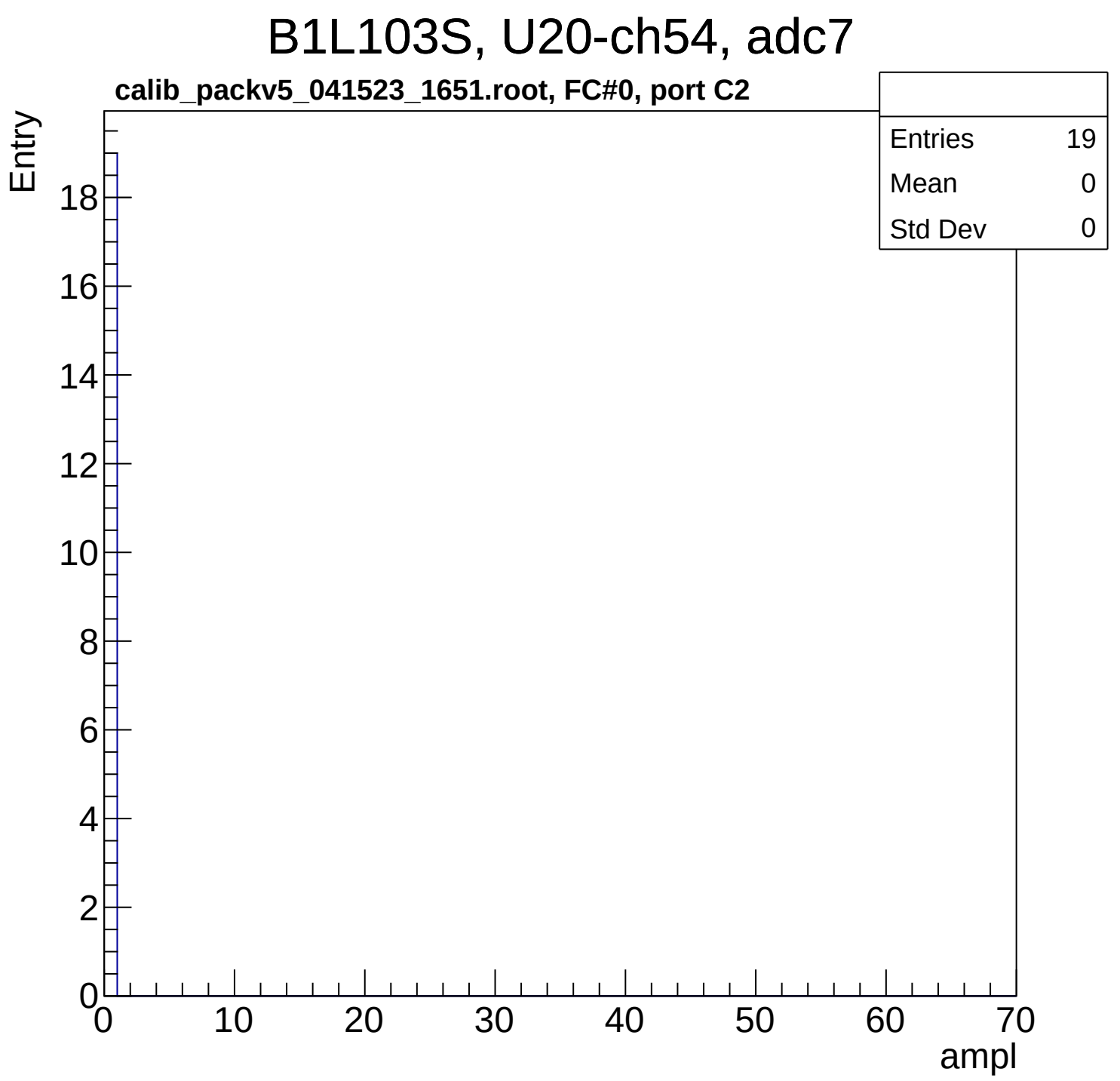
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch54, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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8
10
12
14
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10
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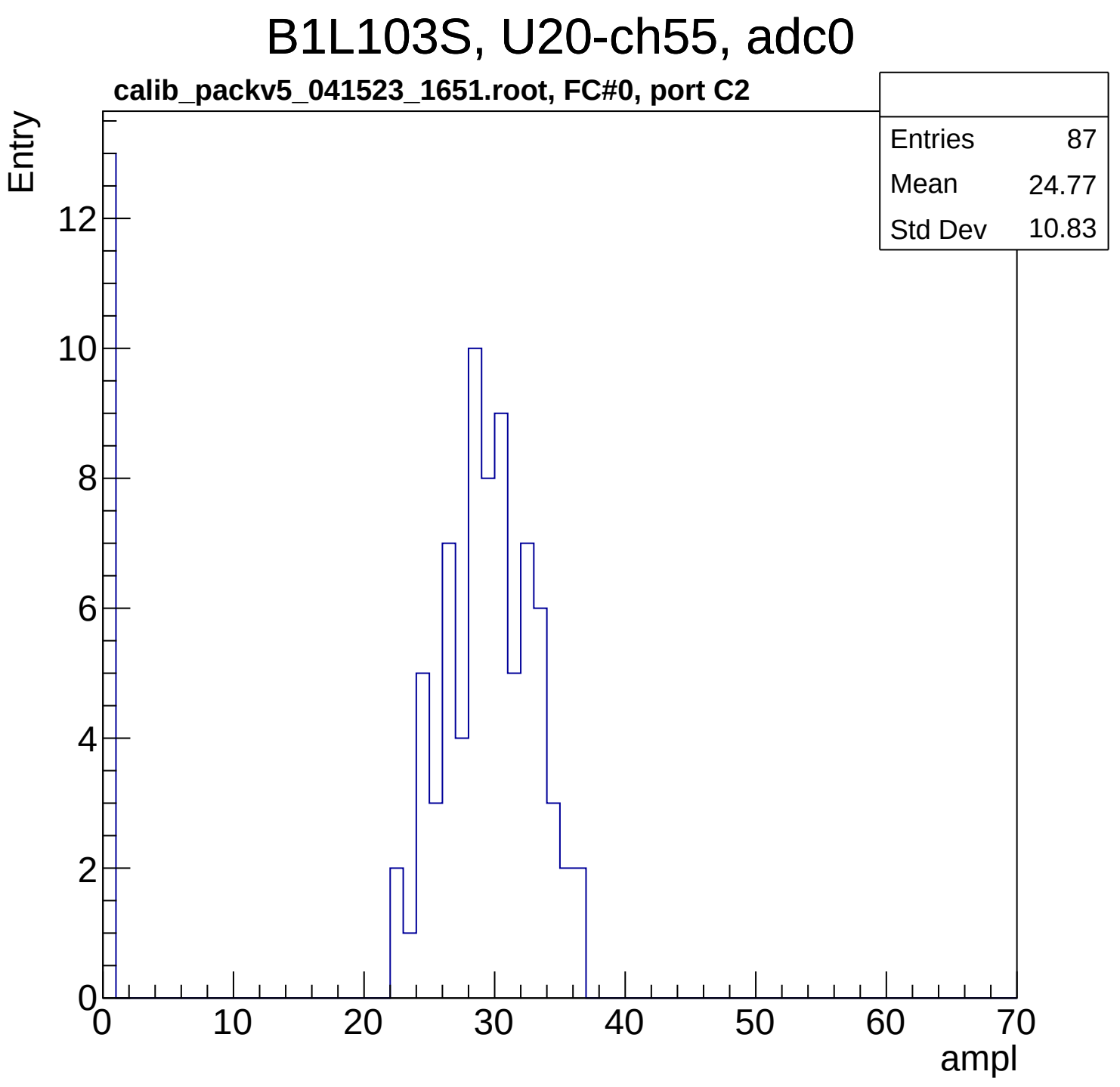
50
60
70
ampl


B1L103S, U20-ch55, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 24.77
Std Dev 10.83
Entry
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8
10
12
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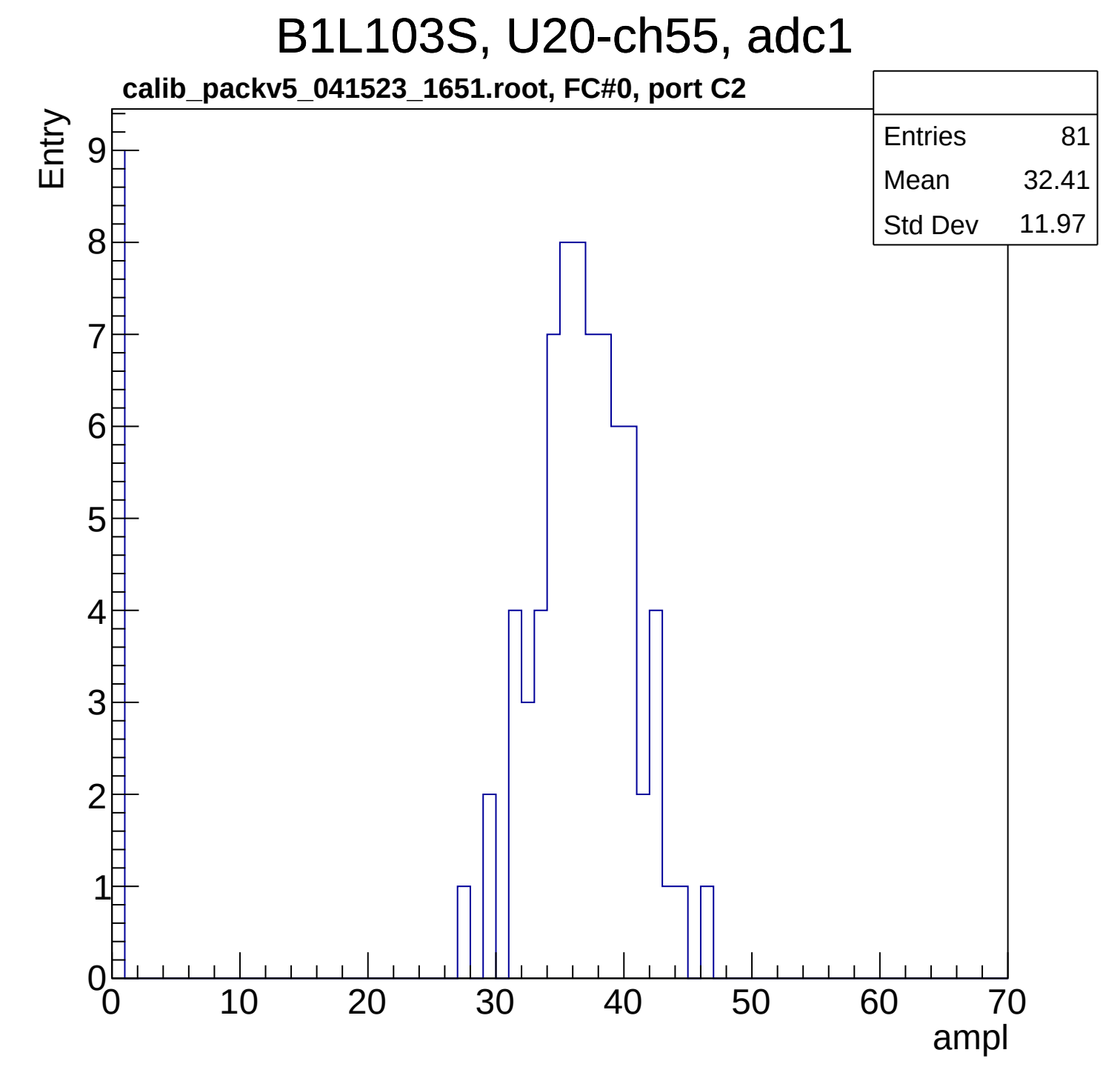
60
70
ampl


B1L103S, U20-ch55, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 32.41
Std Dev 11.97
Entry
ampl
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2
3
4
5
6
7
8
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0
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20
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40
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60
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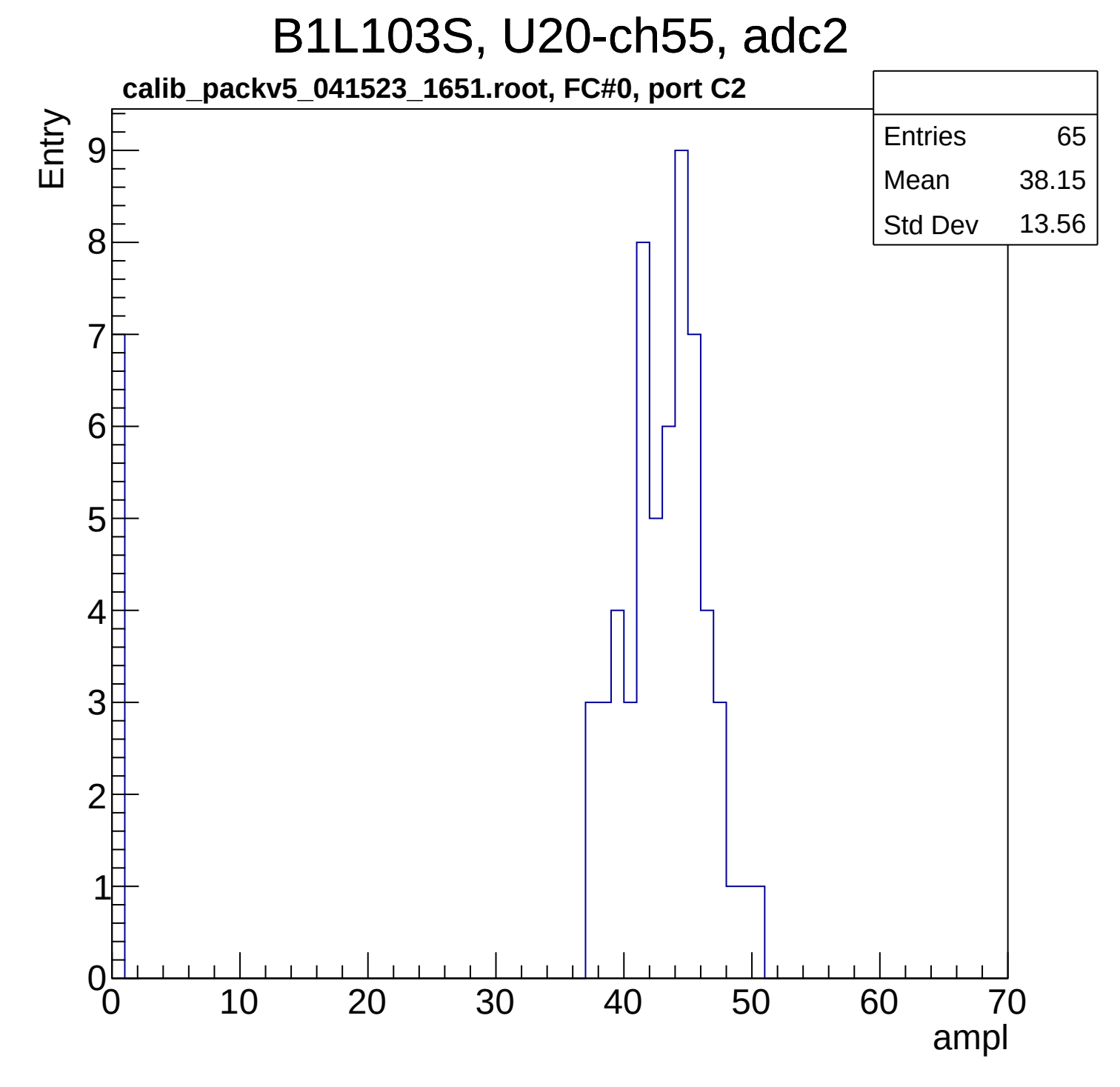
B1L103S, U20-ch55, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 38.15
Std Dev 13.56
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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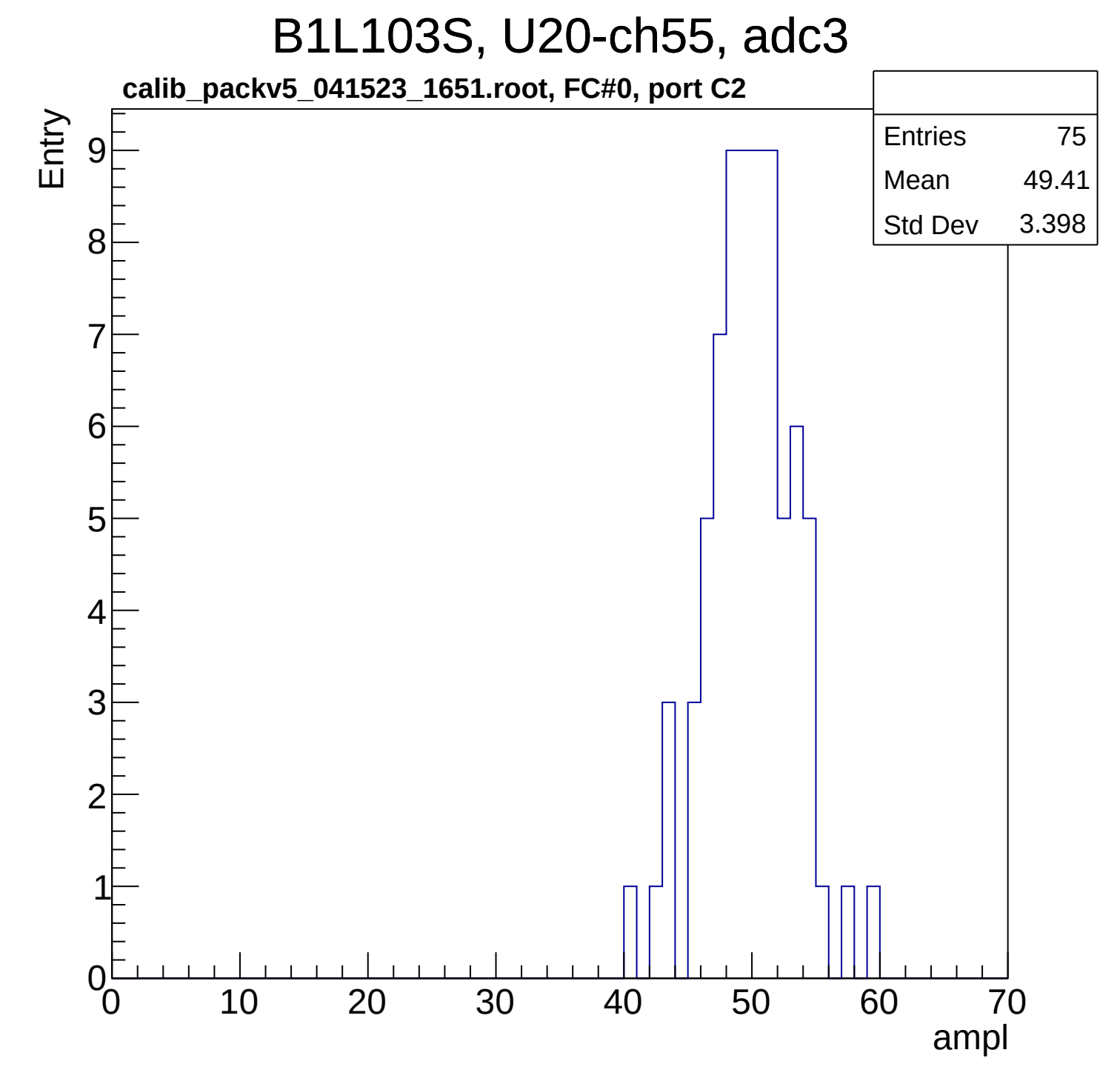
40
50
60
70


B1L103S, U20-ch55, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 49.41
Std Dev 3.398
Entry
ampl
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4
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6
7
8
9
0
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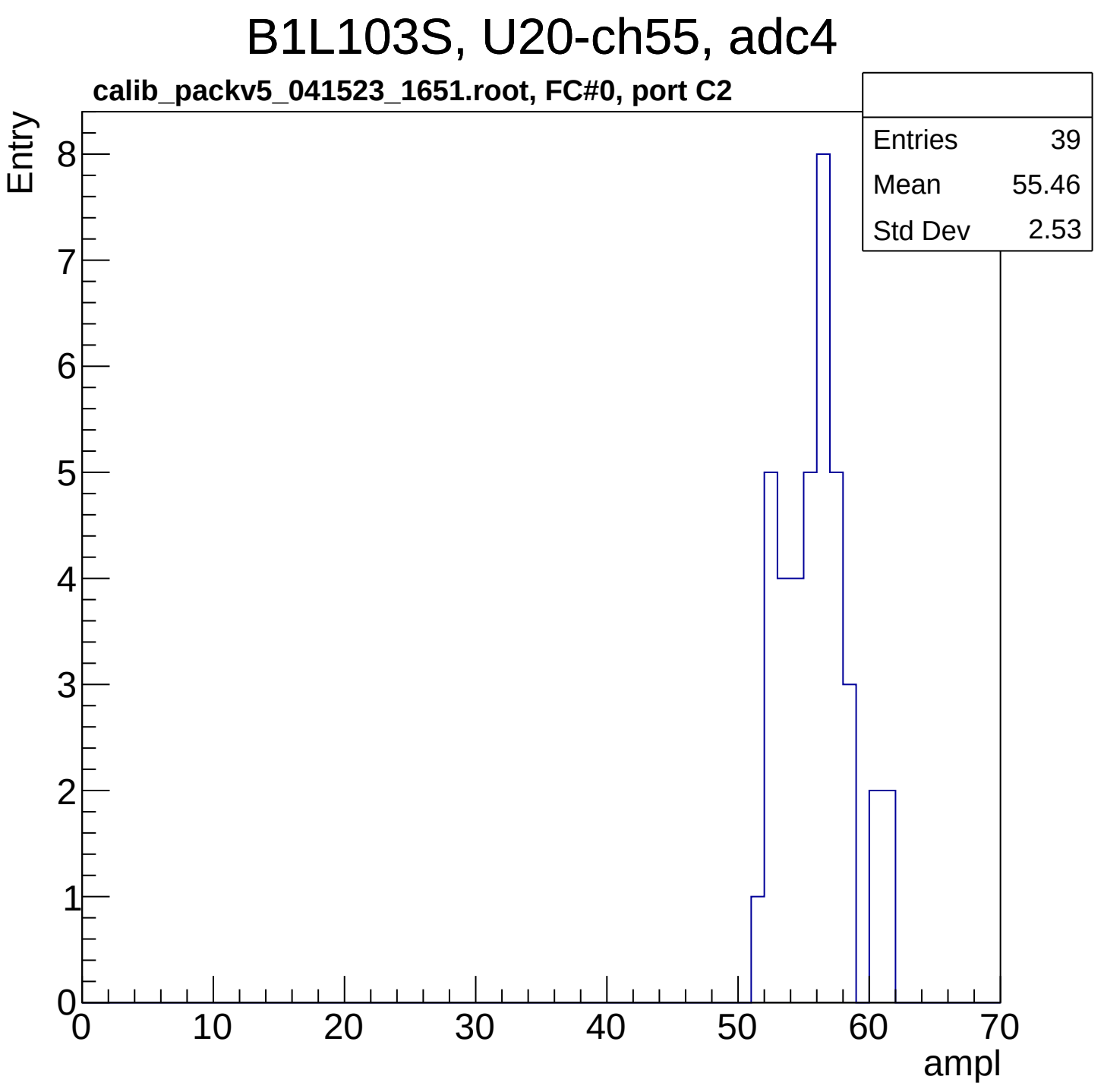
60
70


B1L103S, U20-ch55, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 55.46
Std Dev 2.53
Entry
ampl
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60
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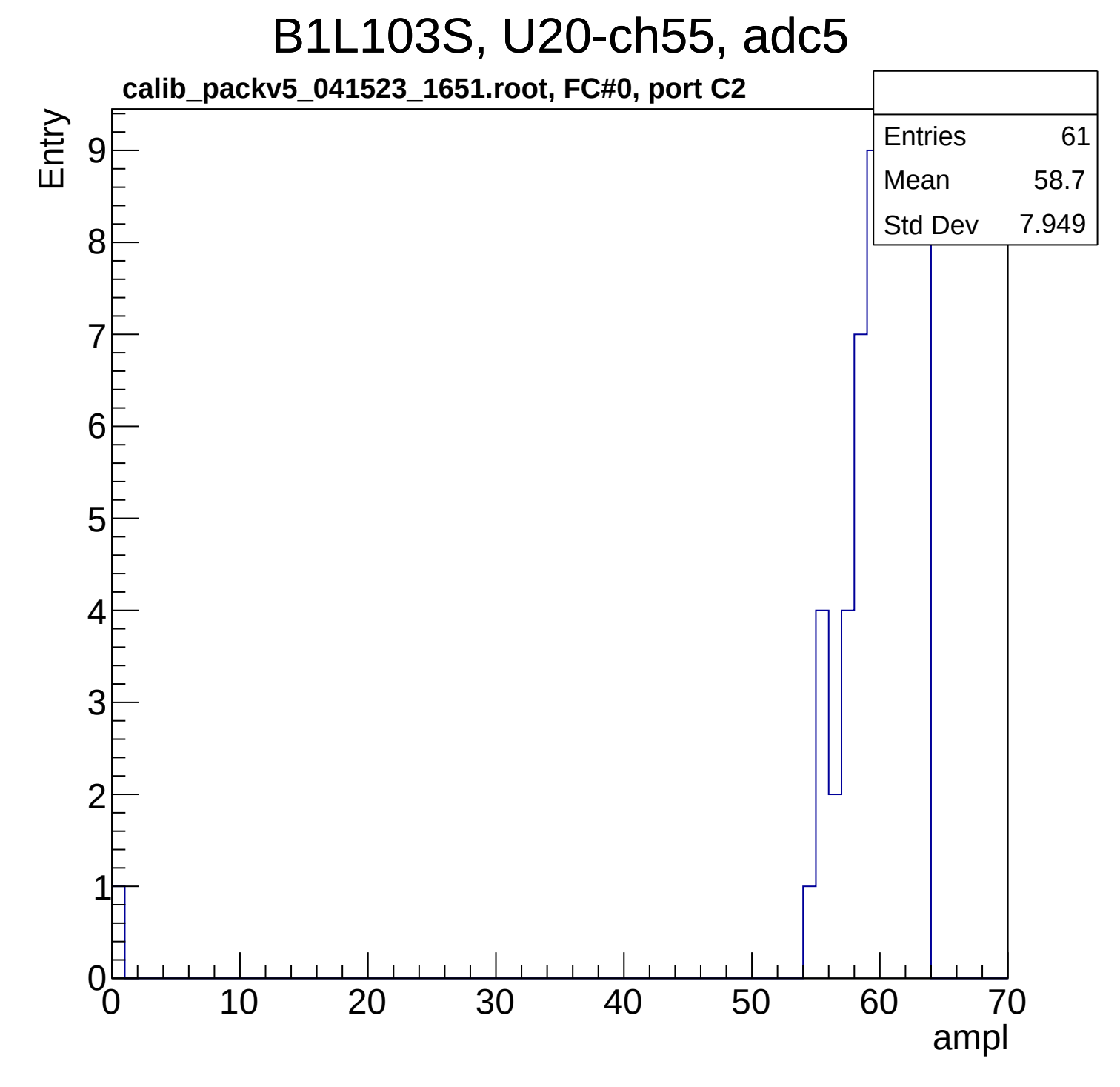
B1L103S, U20-ch55, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 58.7
Std Dev 7.949
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
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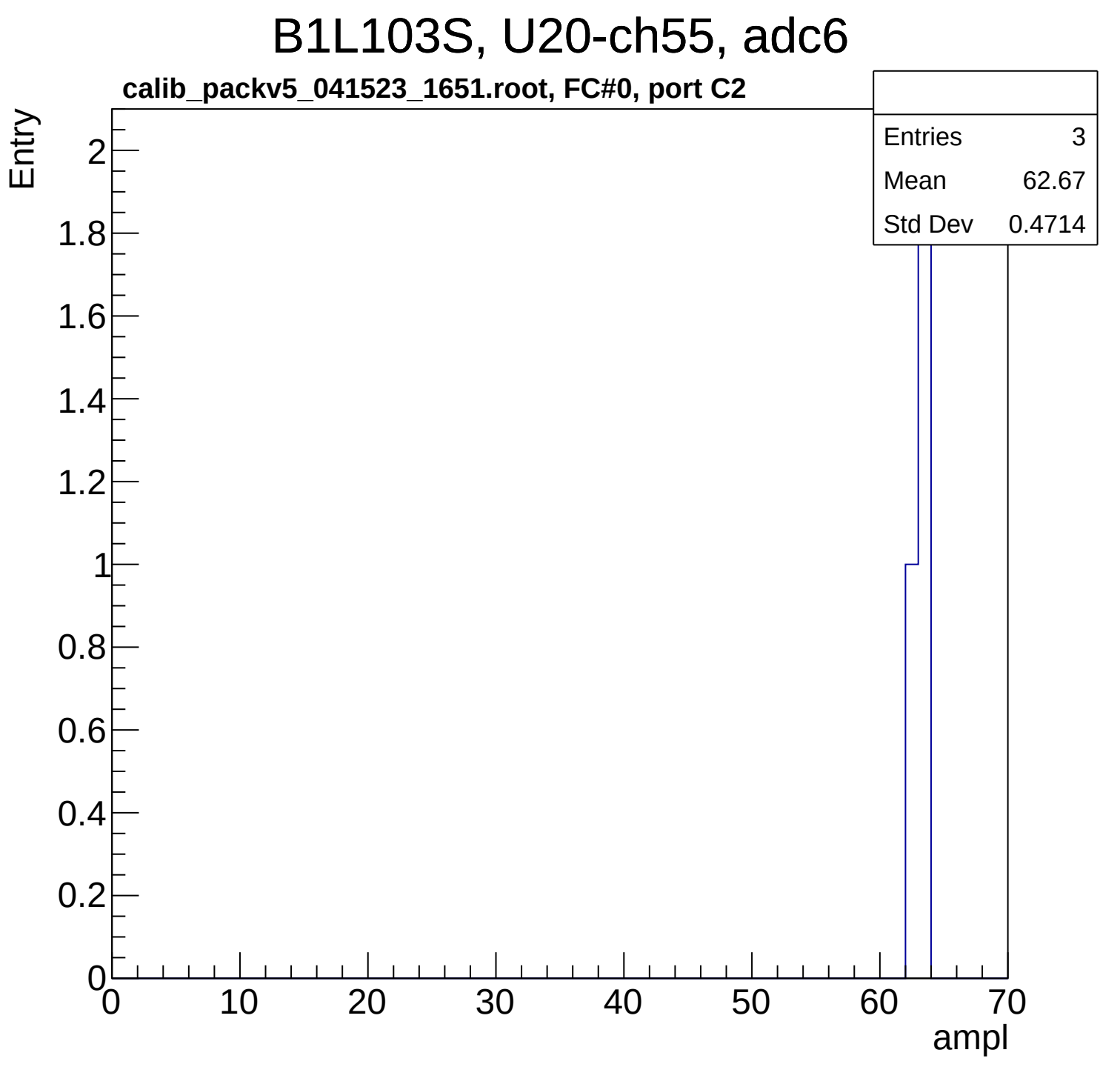
40
50
60
70


B1L103S, U20-ch55, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 62.67
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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40
50
60
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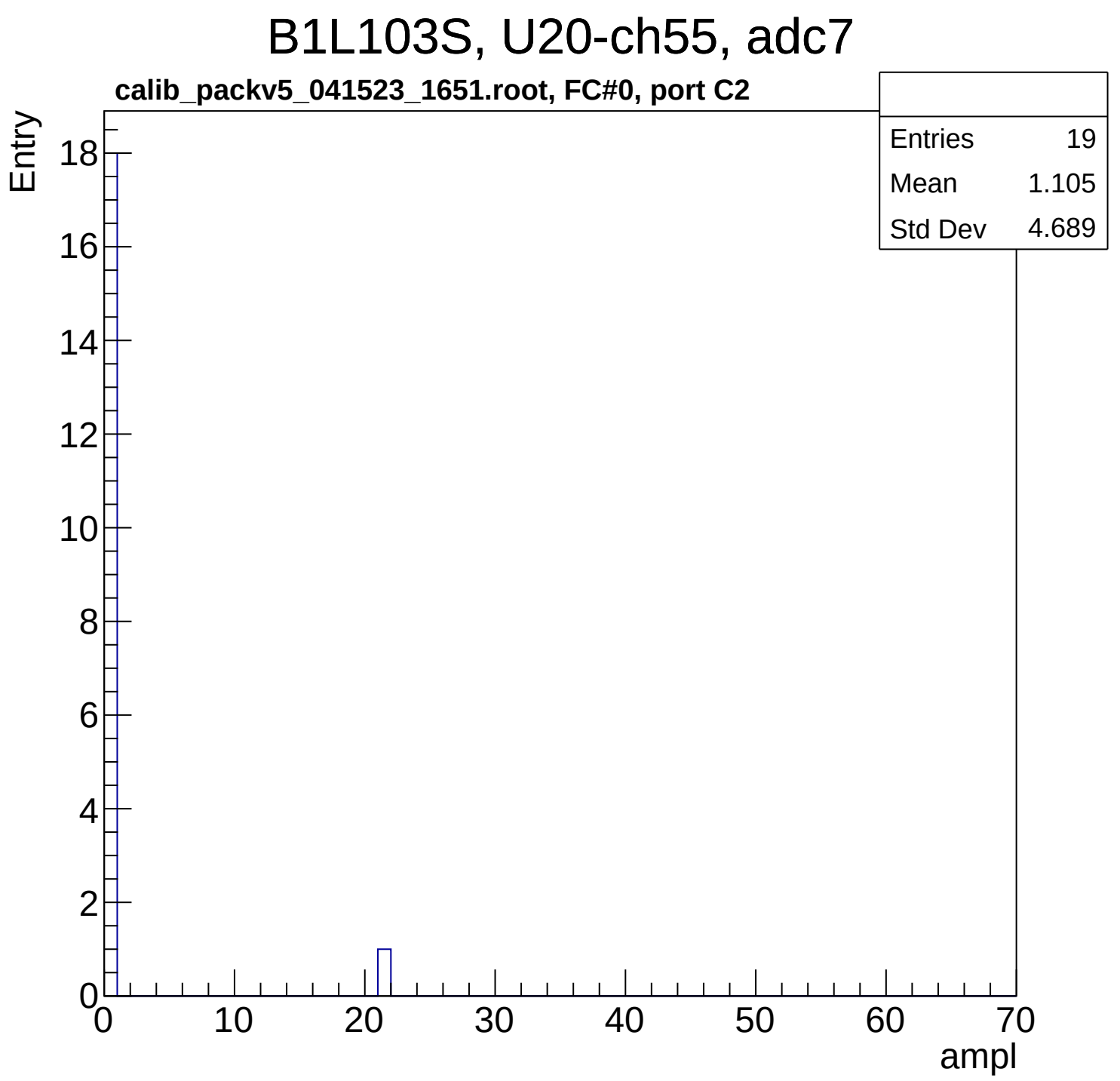
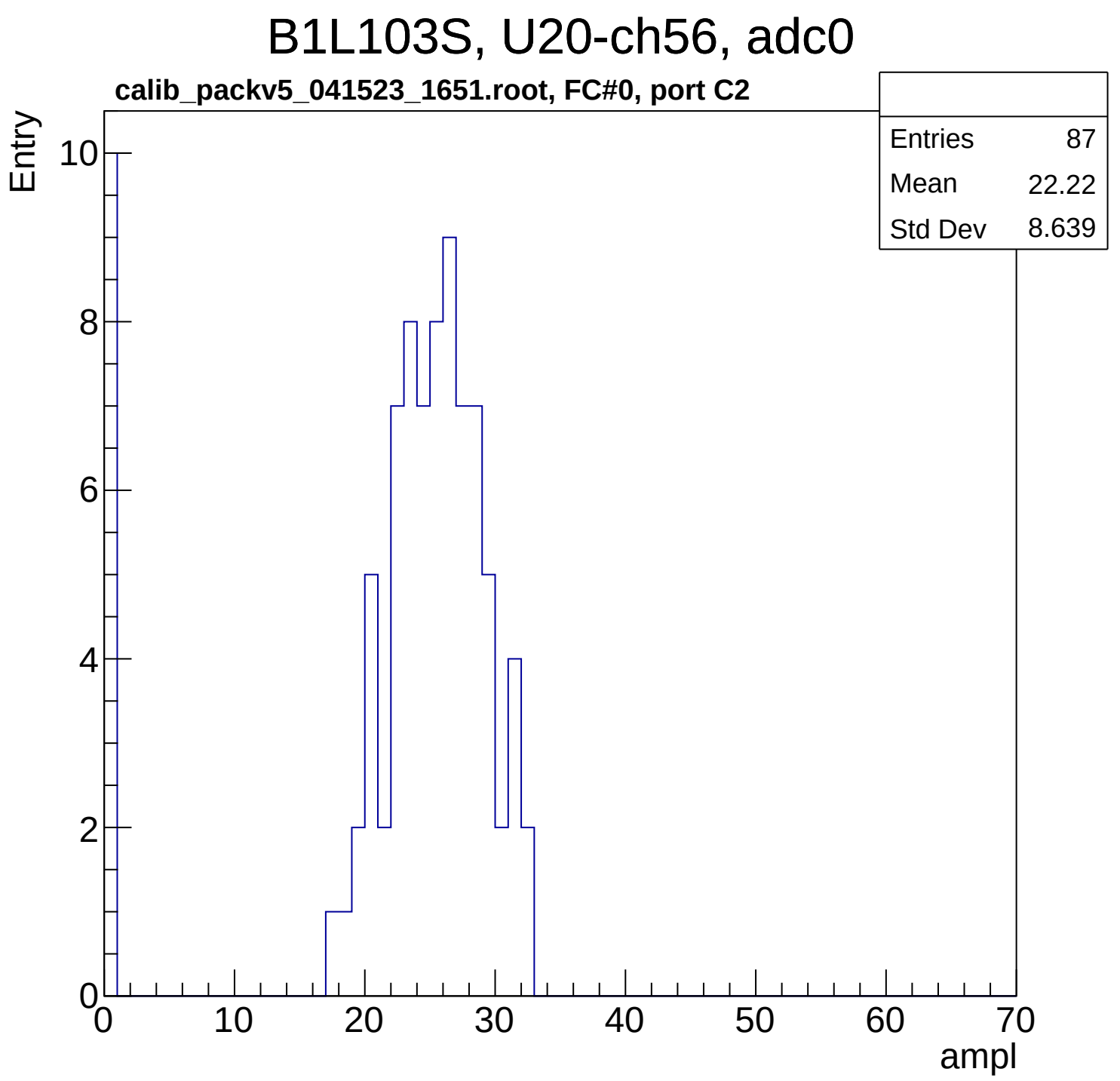
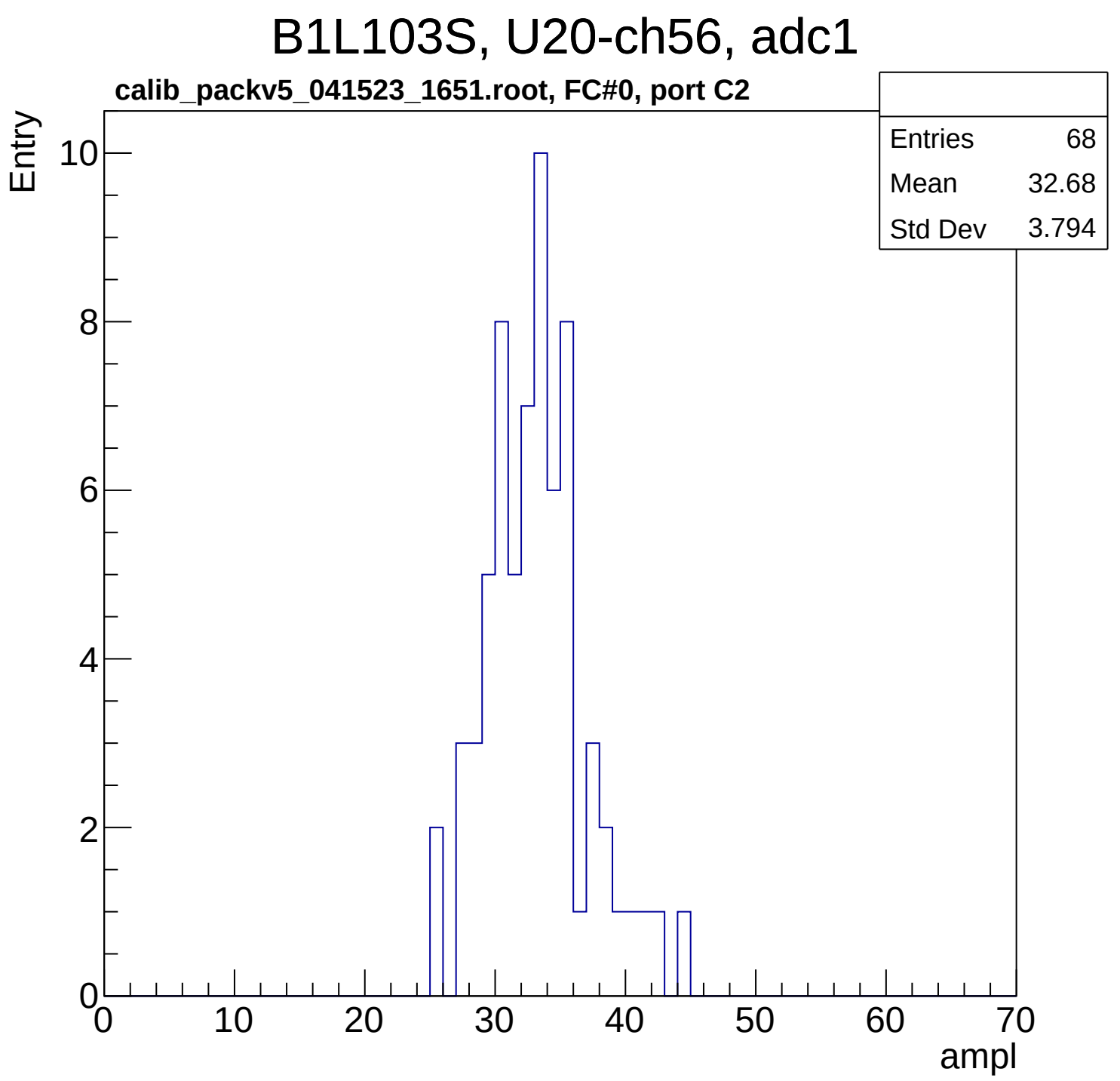
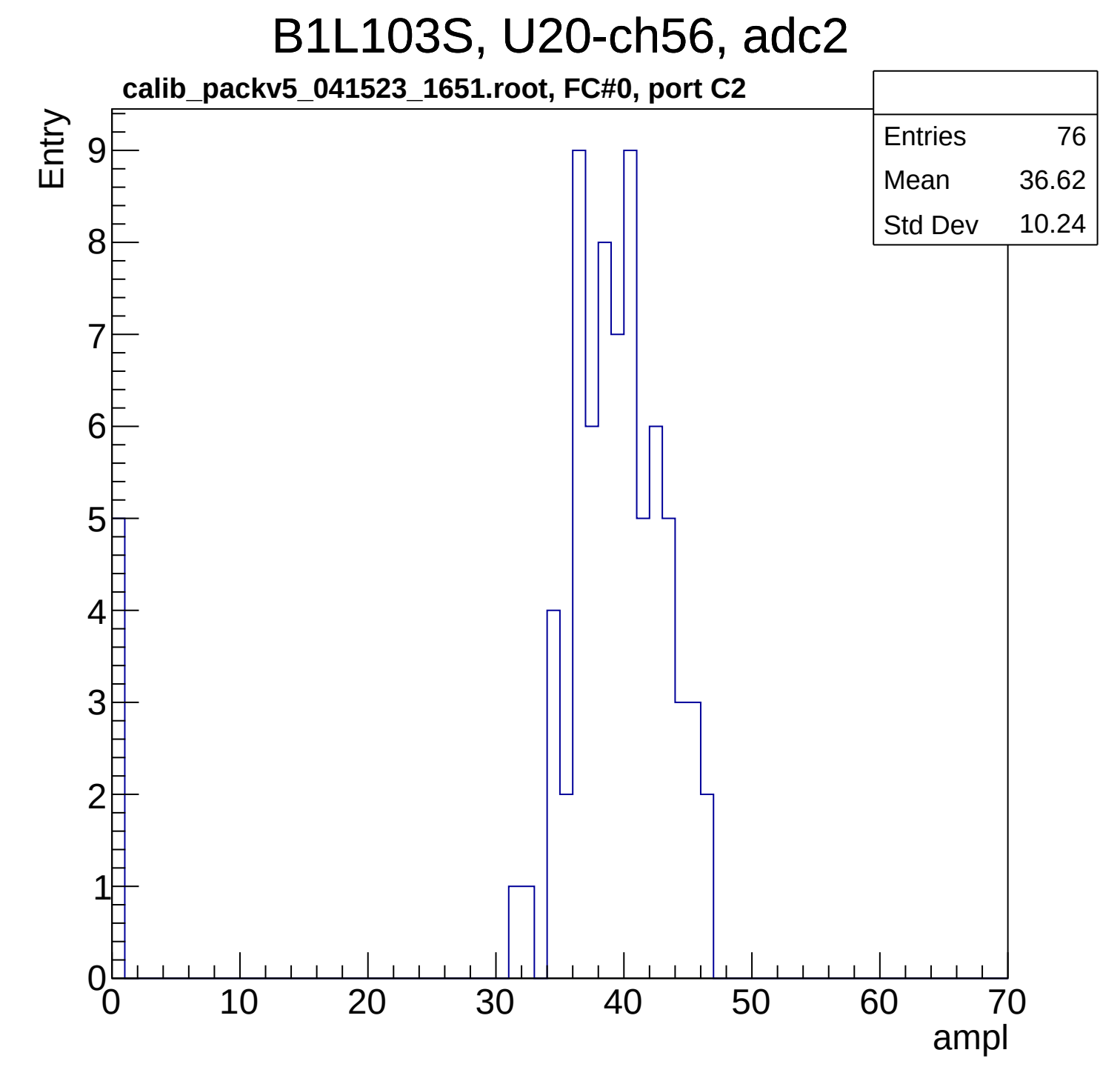
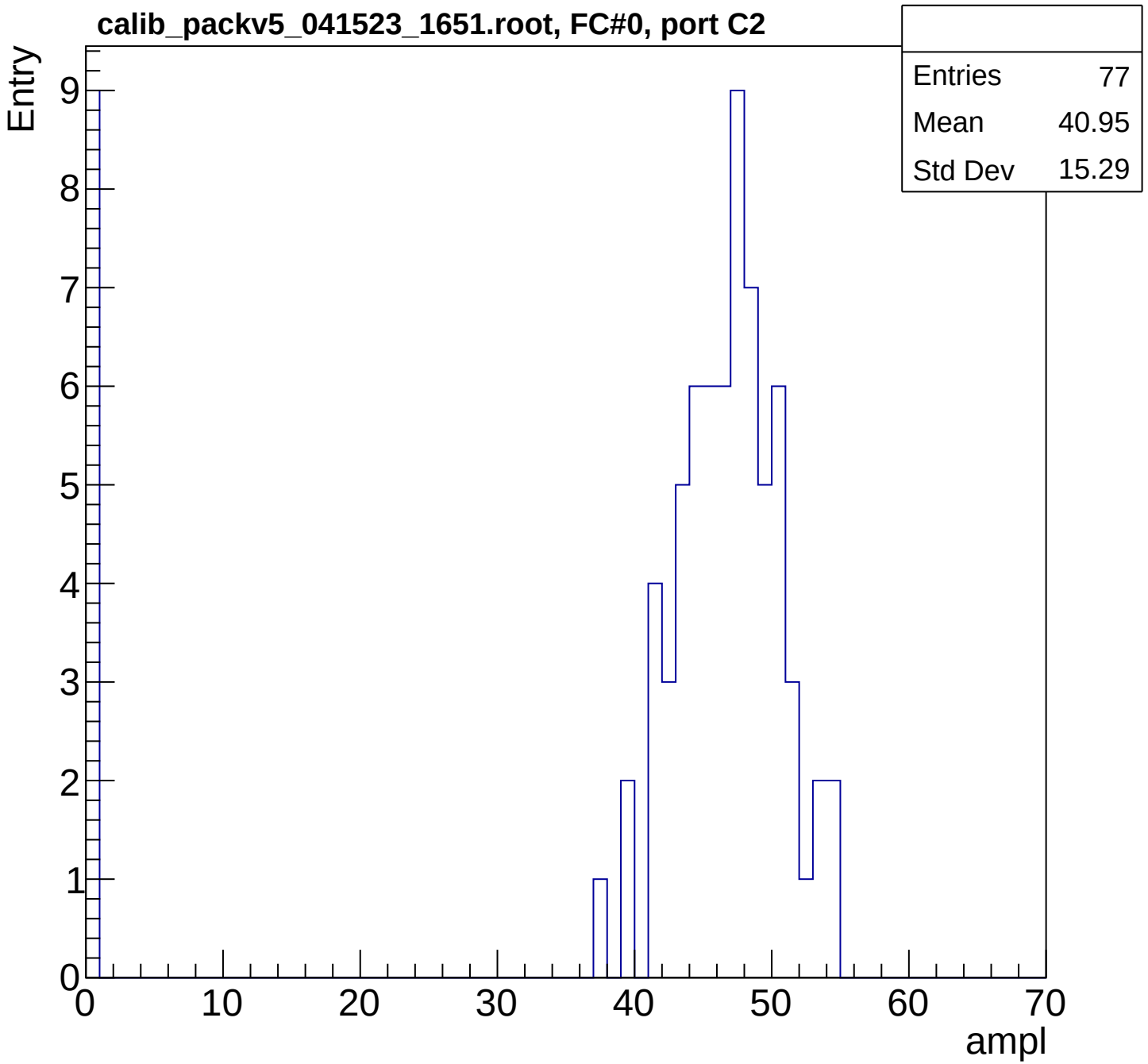
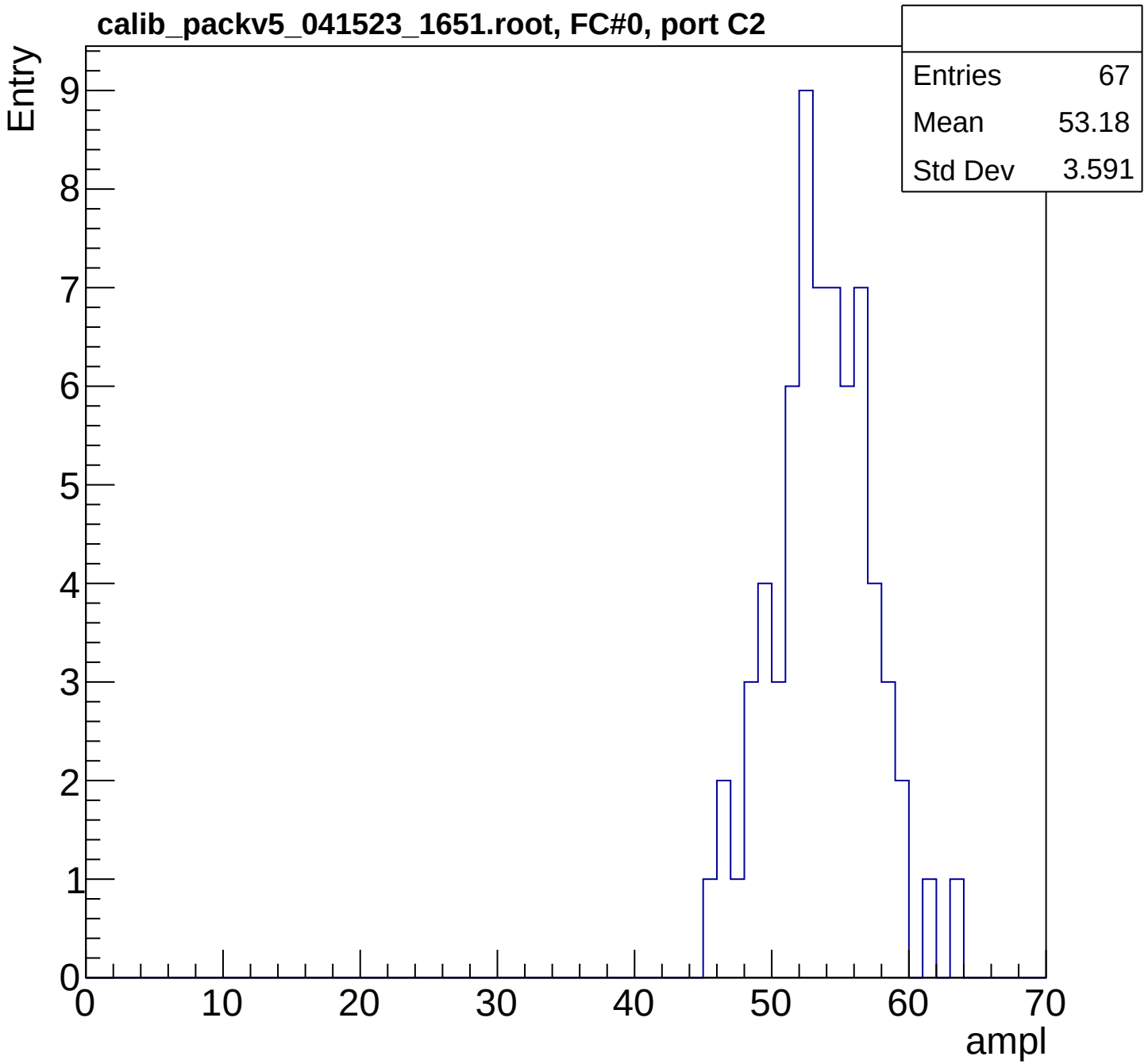

B1L103S, U20-ch55, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.105
Std Dev 4.689
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch56, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 22.22
Std Dev 8.639
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch56, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 32.68
Std Dev 3.794
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U20-ch56, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 36.62
Std Dev 10.24
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch56, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 40.95
Std Dev 15.29
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch56, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 53.18
Std Dev 3.591
Entry
ampl
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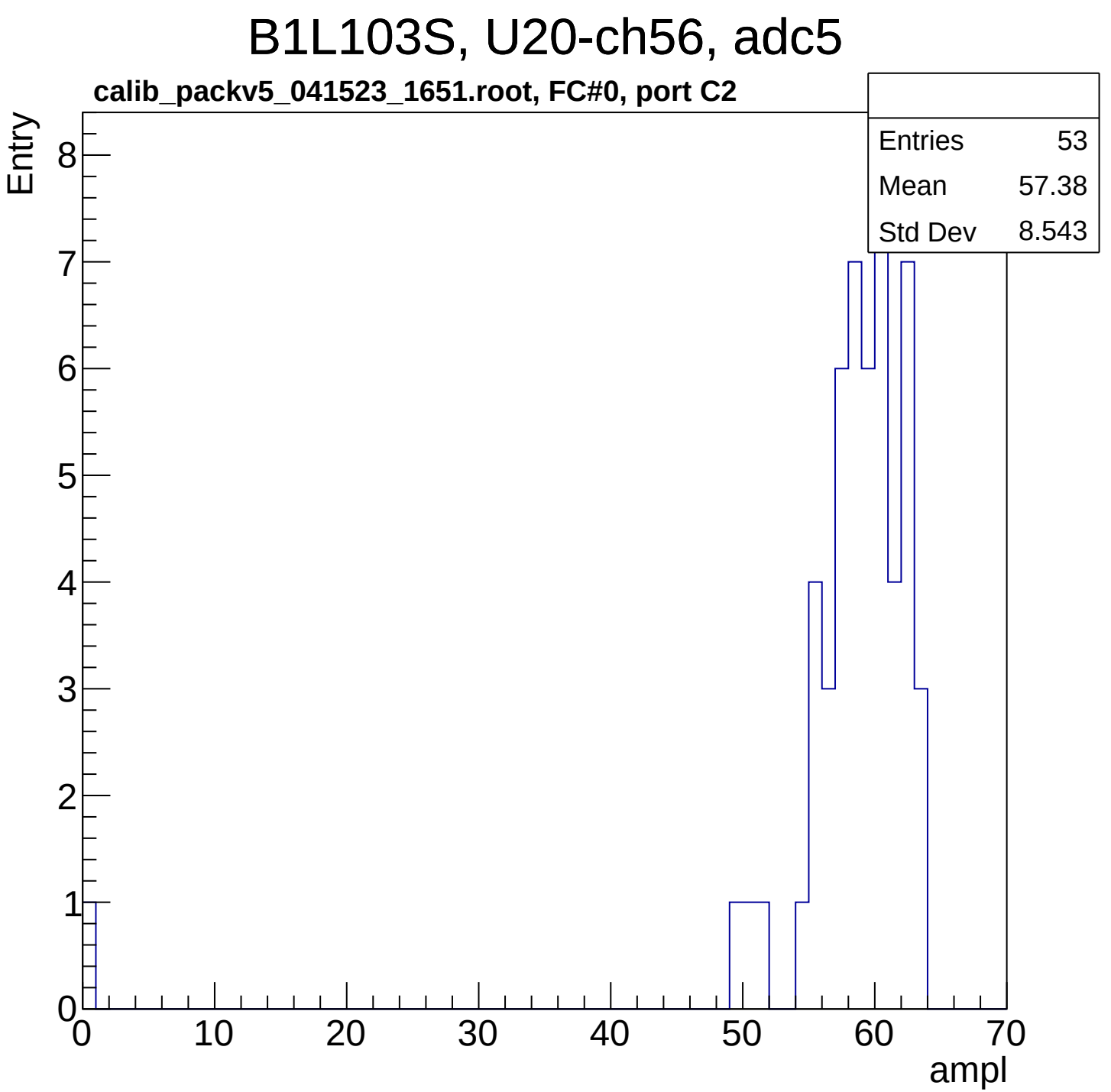
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch56, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 57.38
Std Dev 8.543
Entry
ampl
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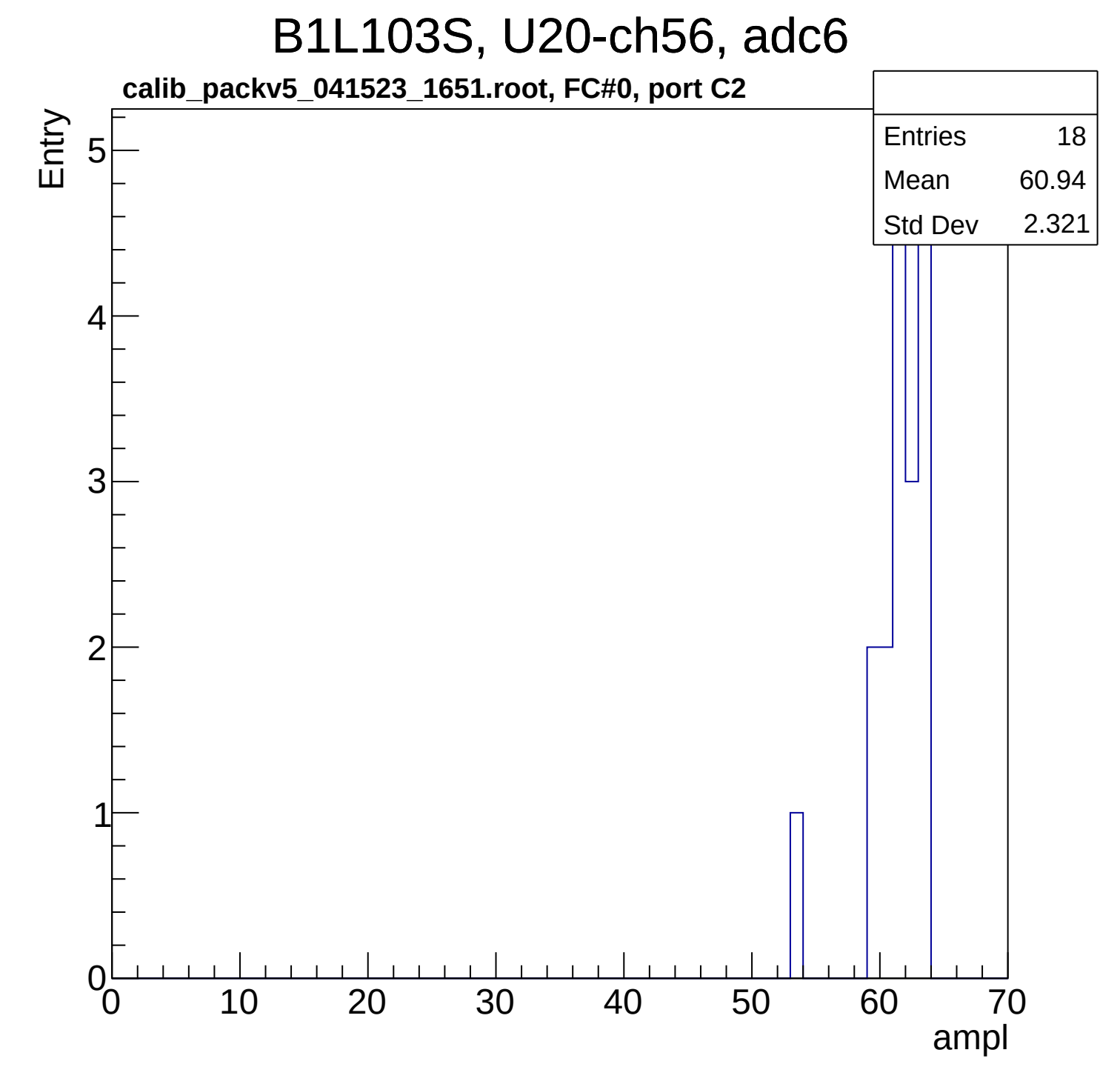
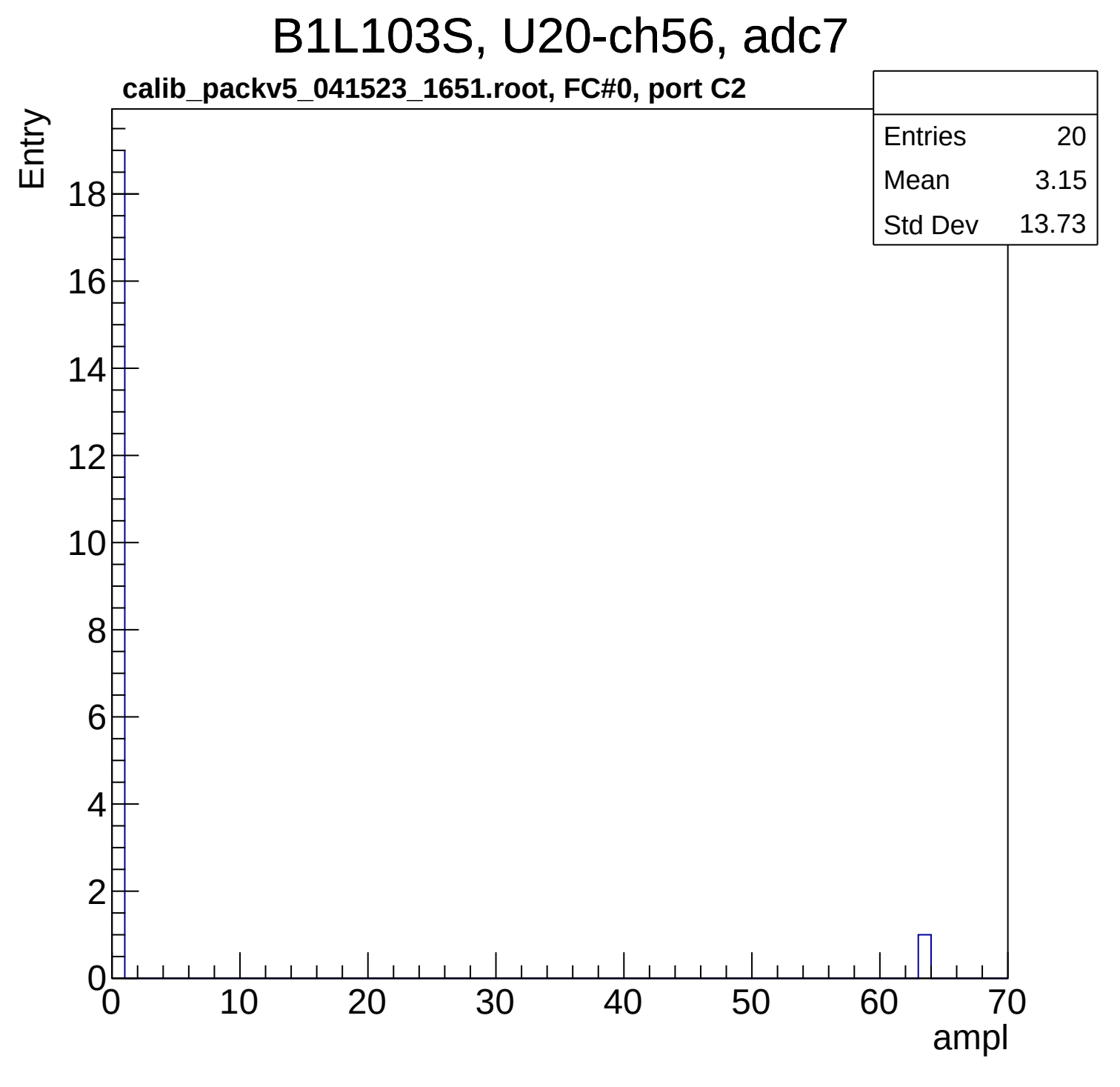
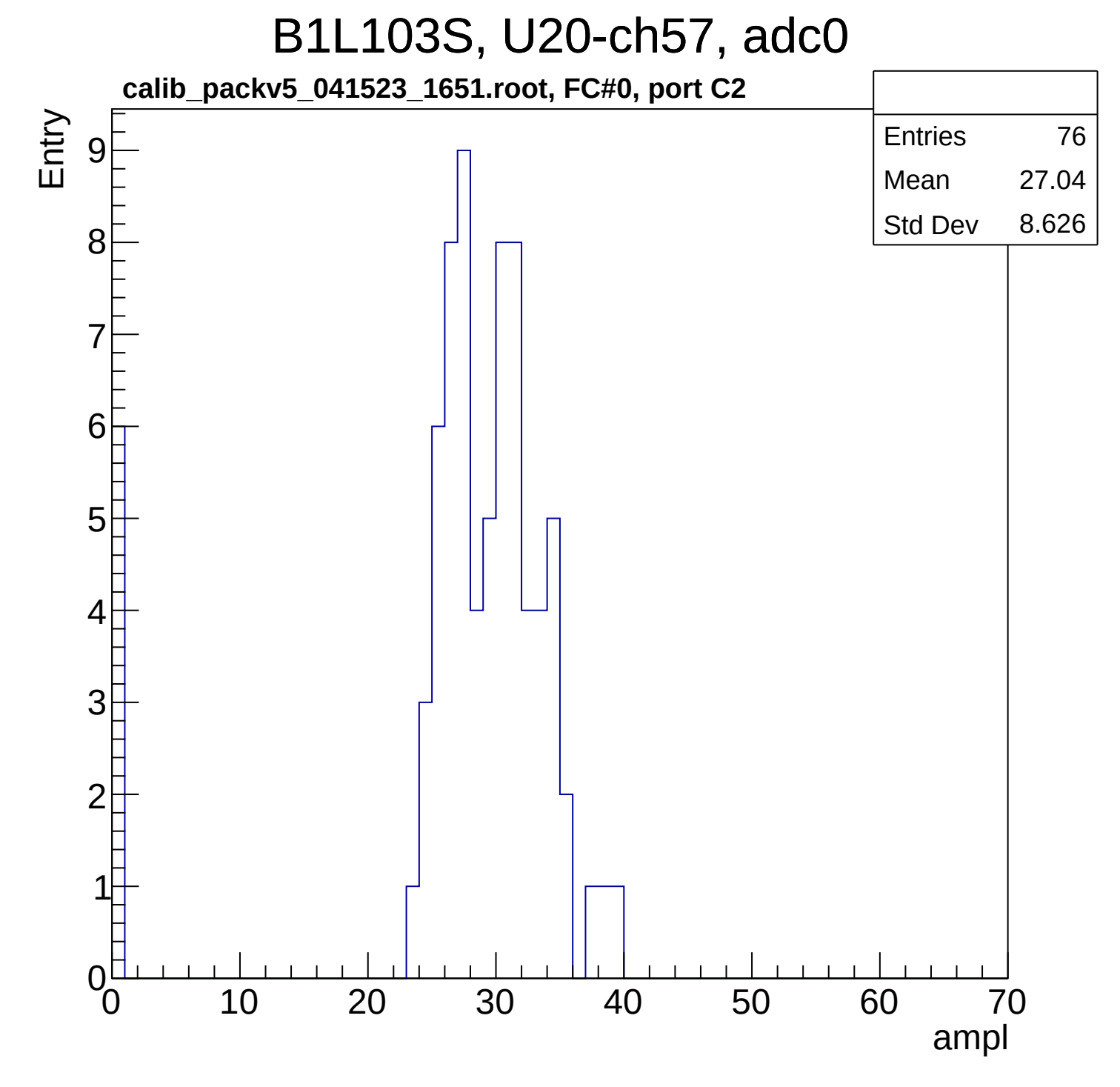
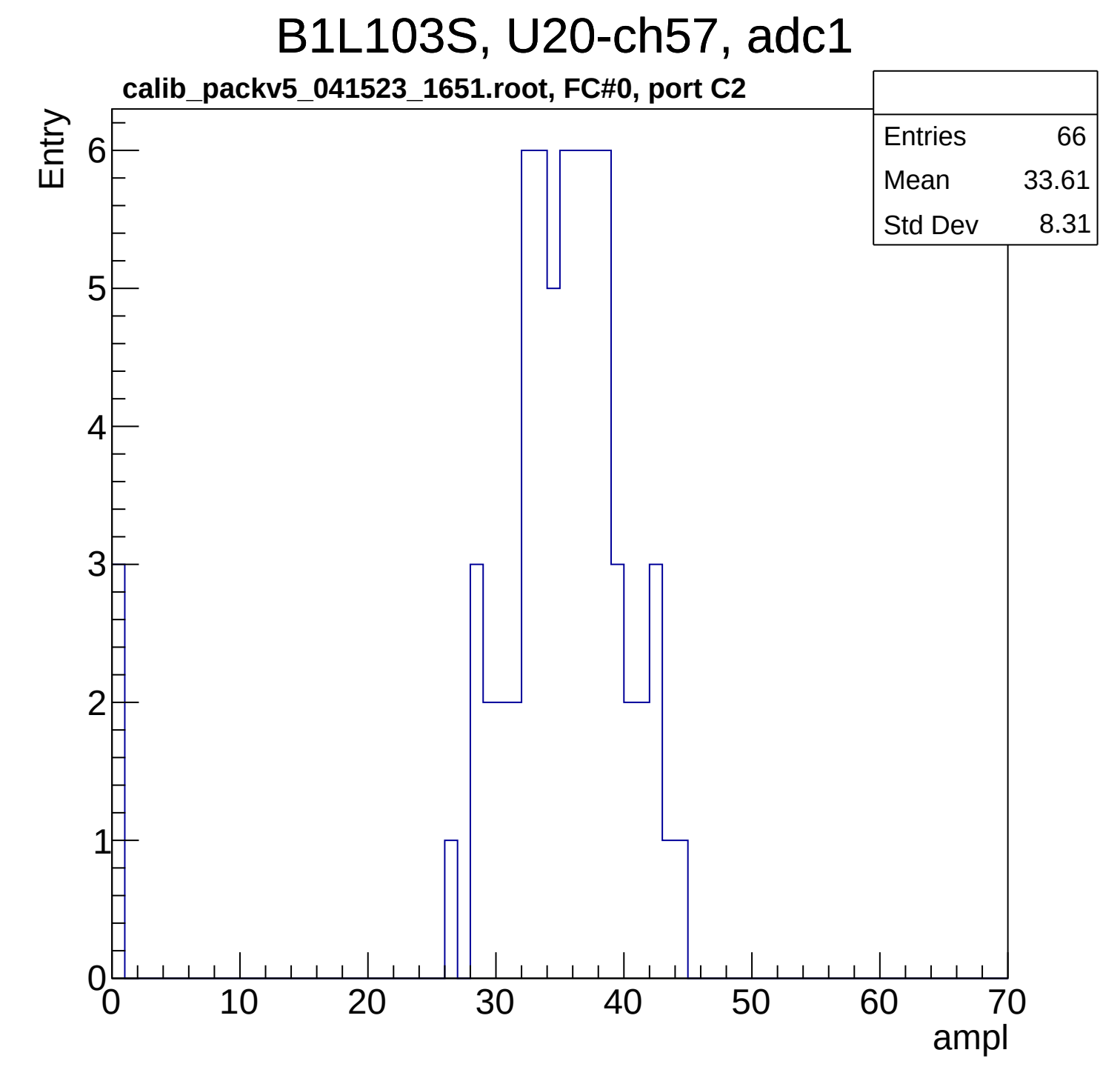
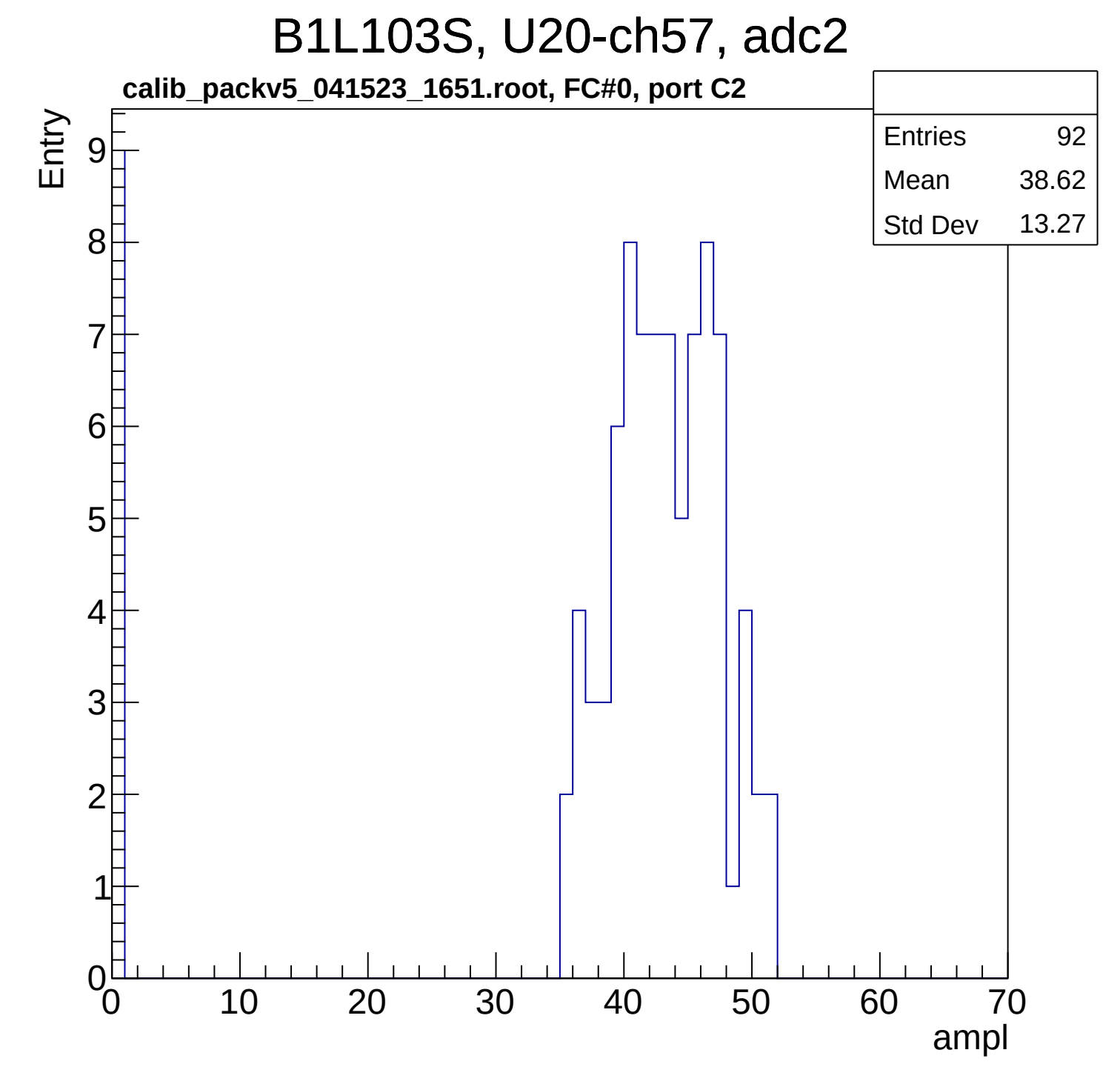
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch56, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 60.94
Std Dev 2.321
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U20-ch56, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch57, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 27.04
Std Dev 8.626
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch57, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 33.61
Std Dev 8.31
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U20-ch57, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 38.62
Std Dev 13.27
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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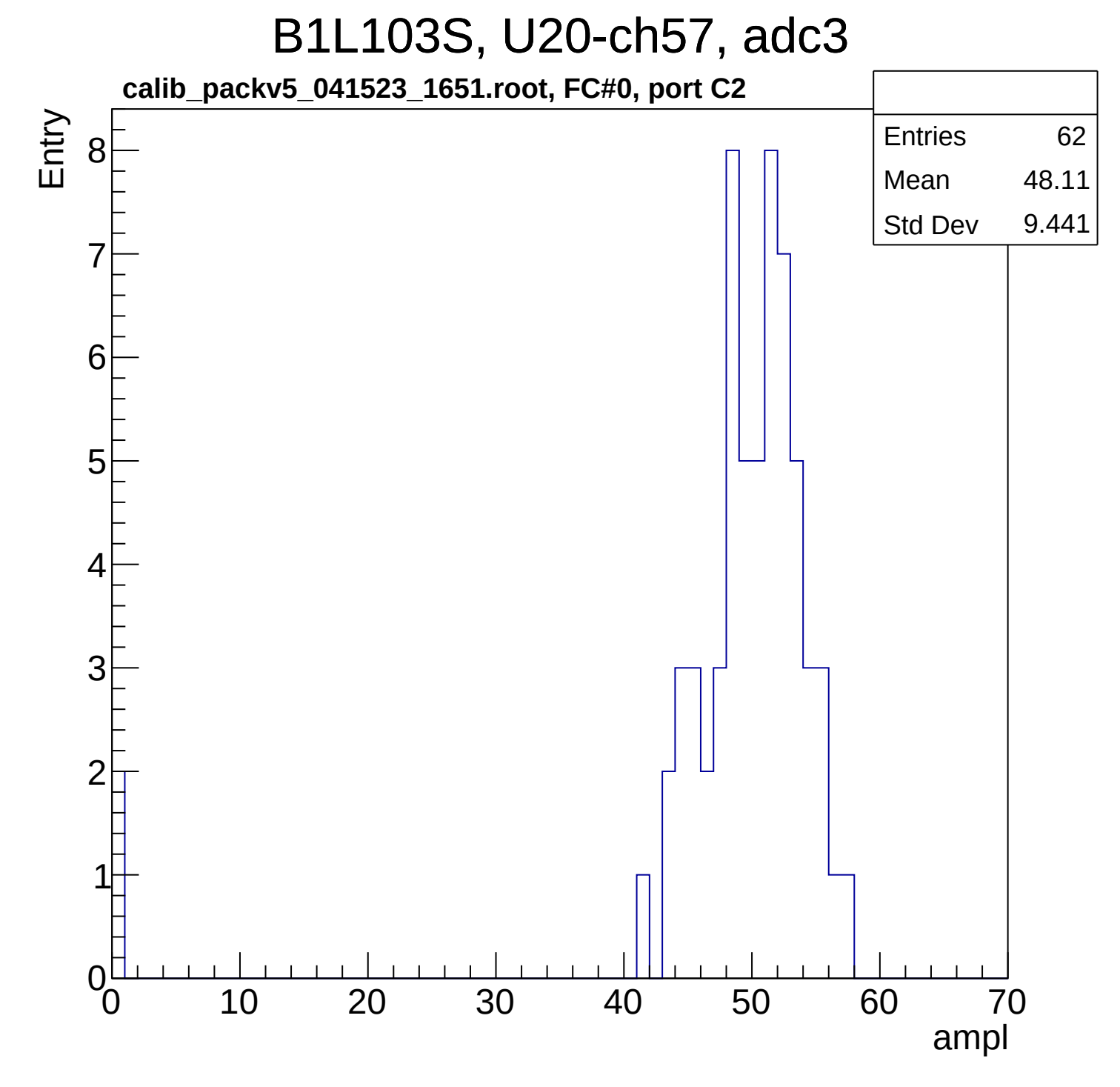
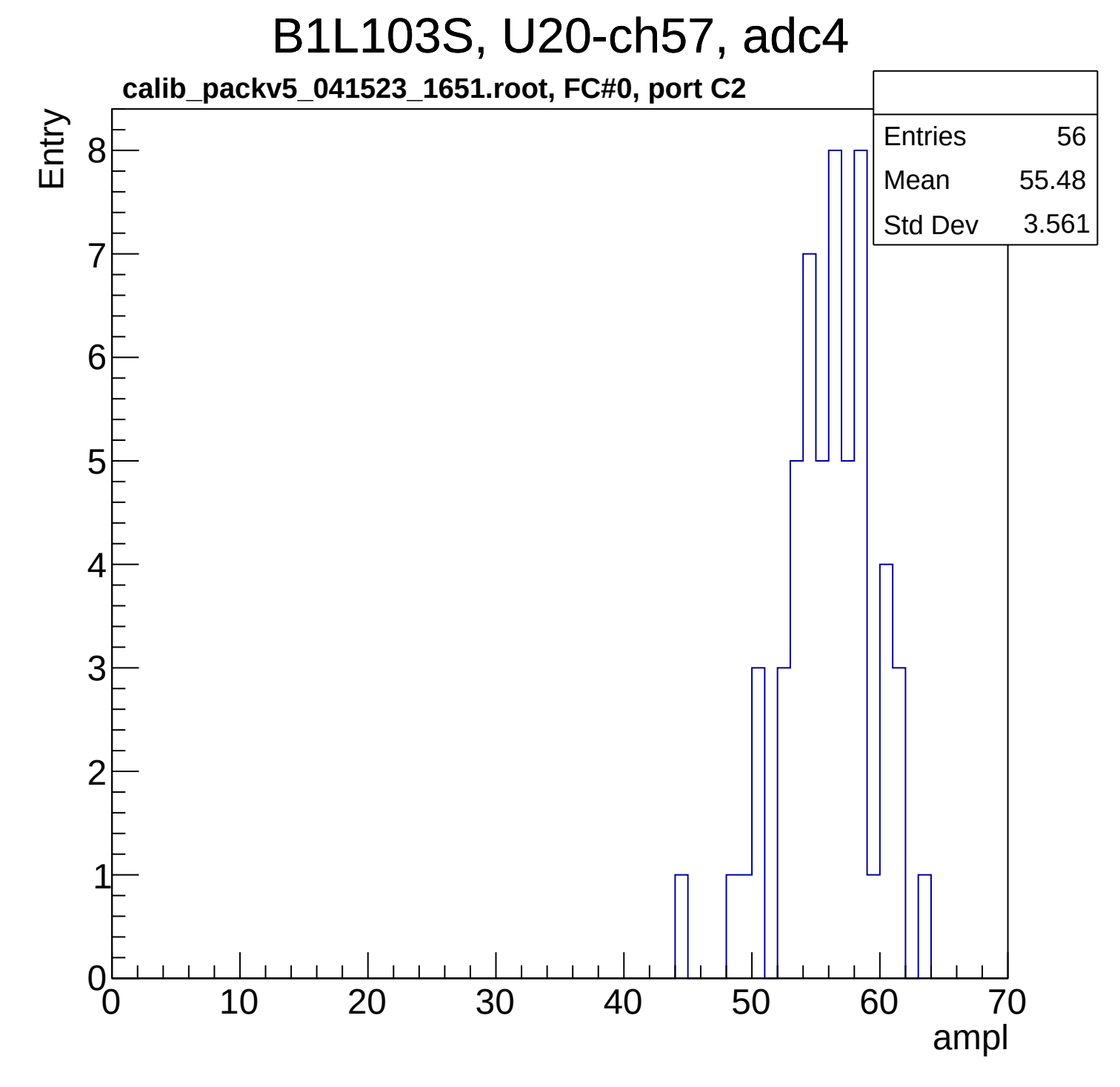

B1L103S, U20-ch57, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 48.11
Std Dev 9.441
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch57, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 55.48
Std Dev 3.561
Entry
ampl
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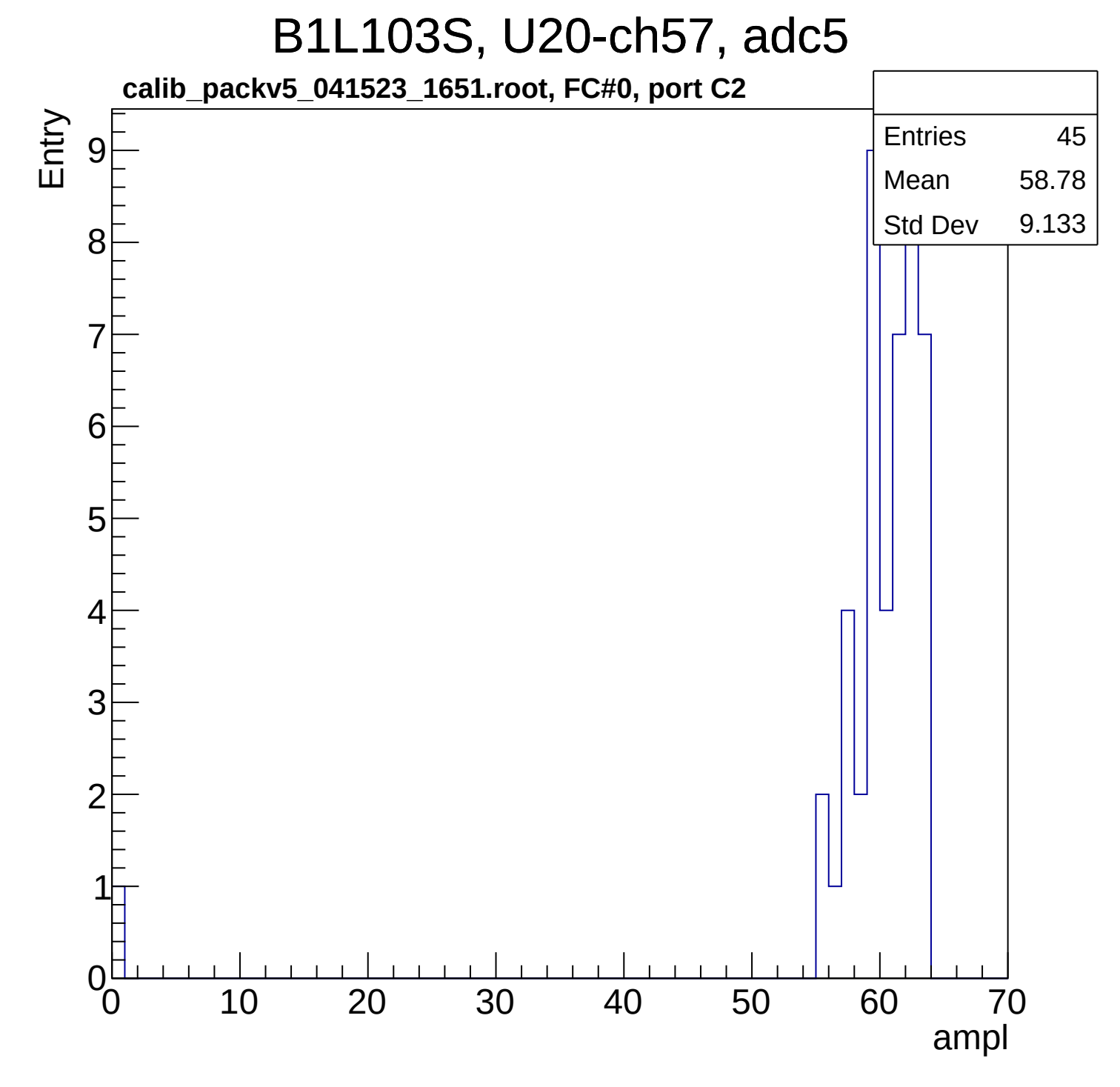
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch57, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 58.78
Std Dev 9.133
Entry
ampl
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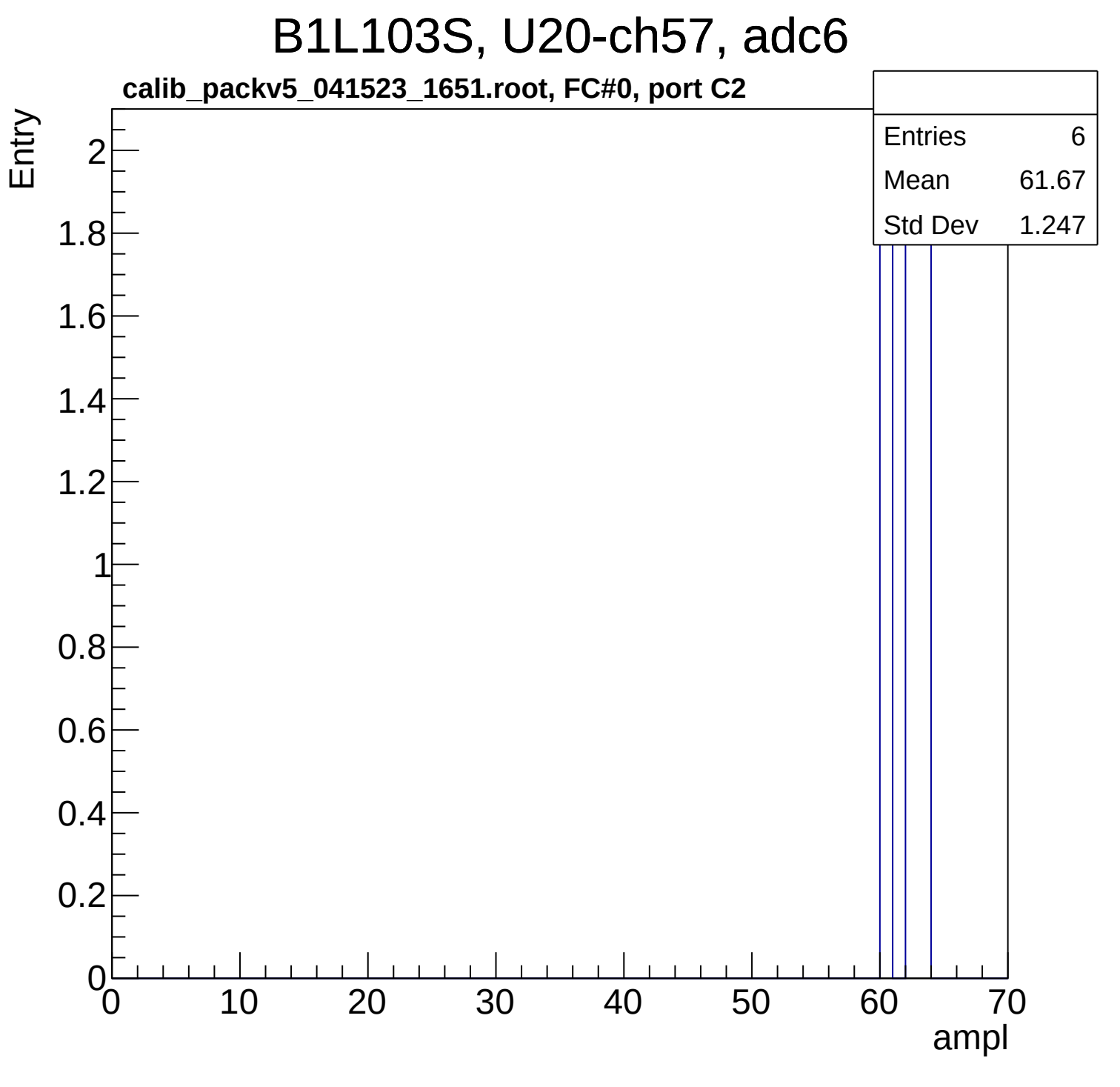
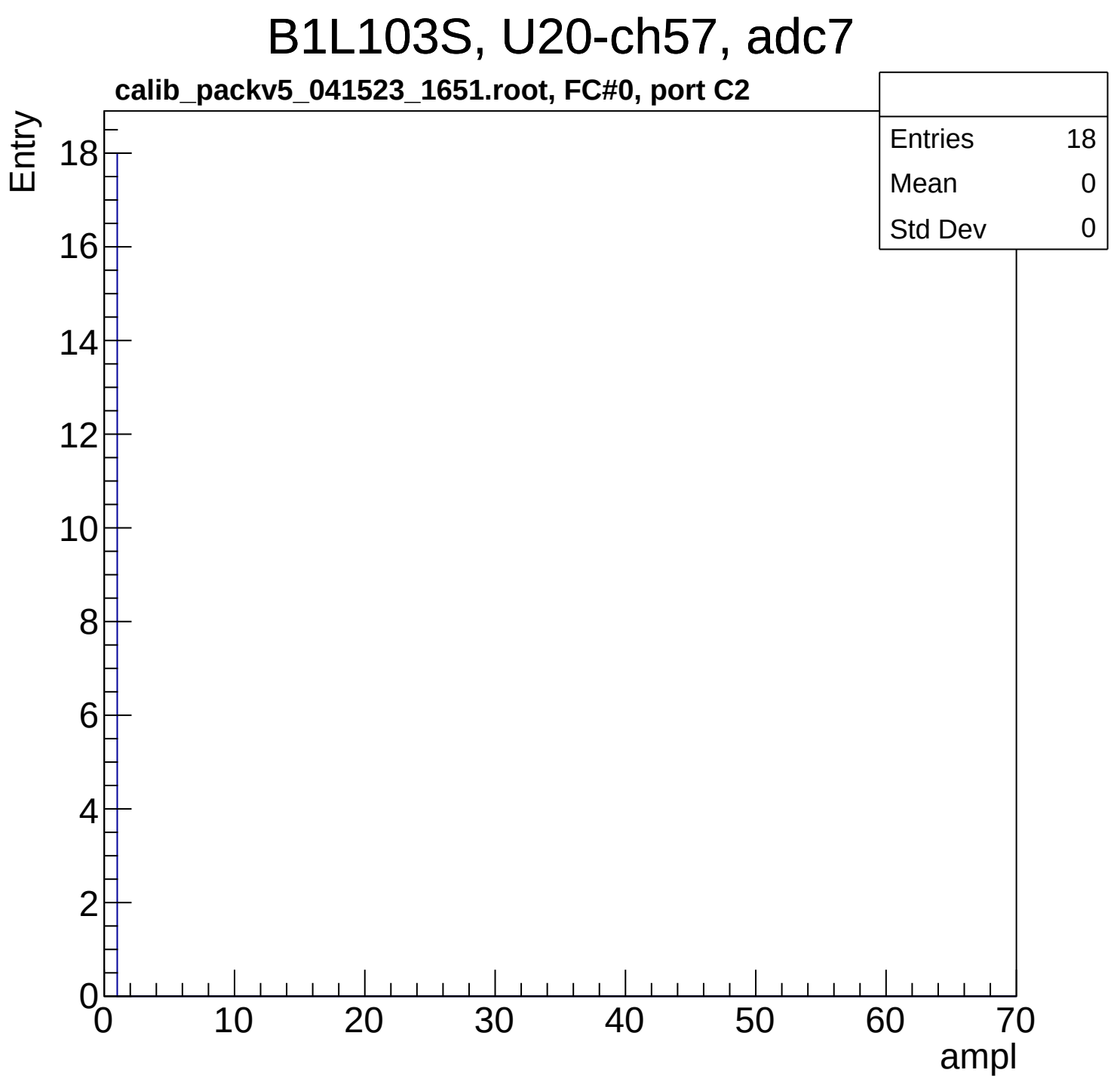
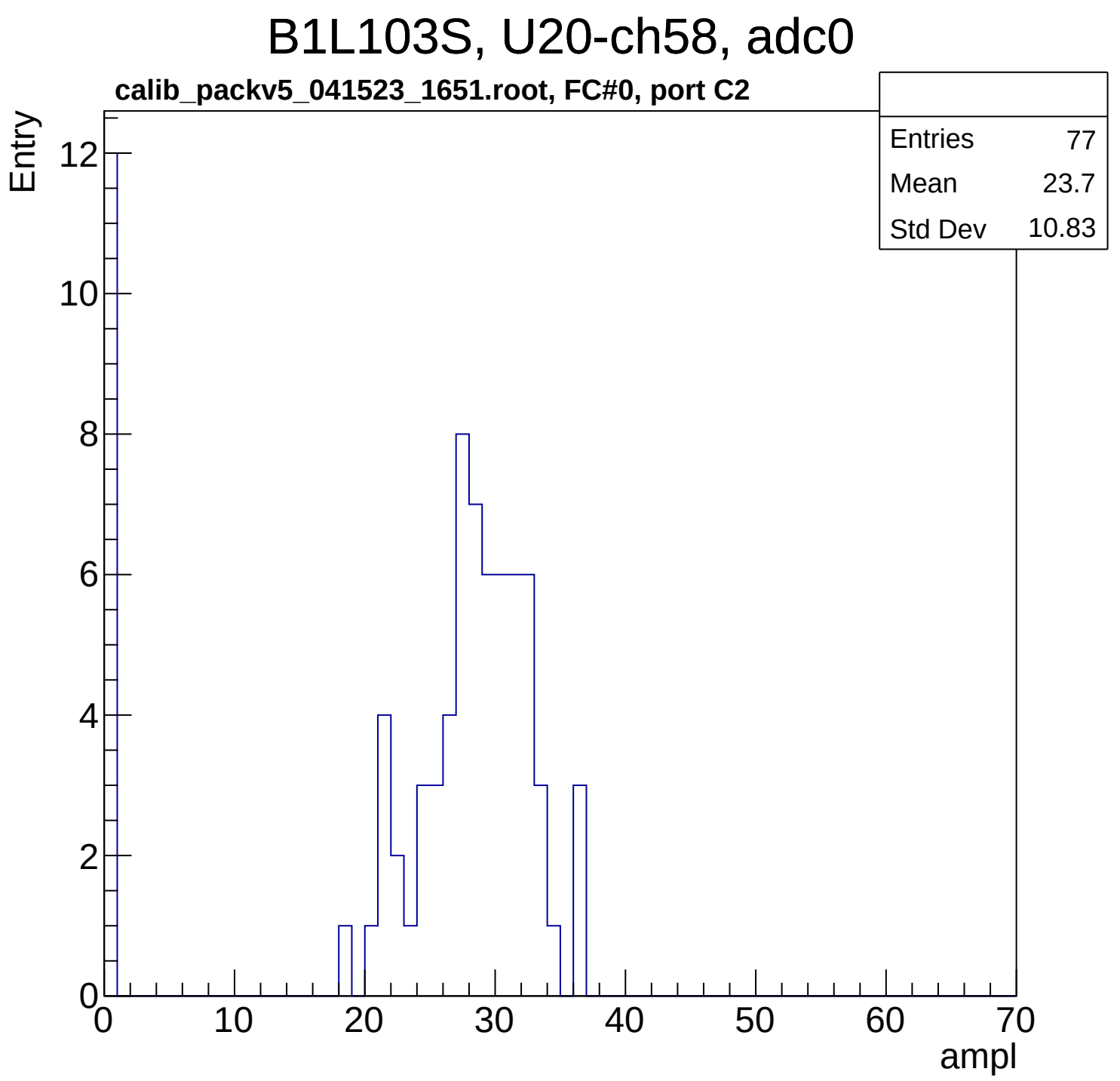
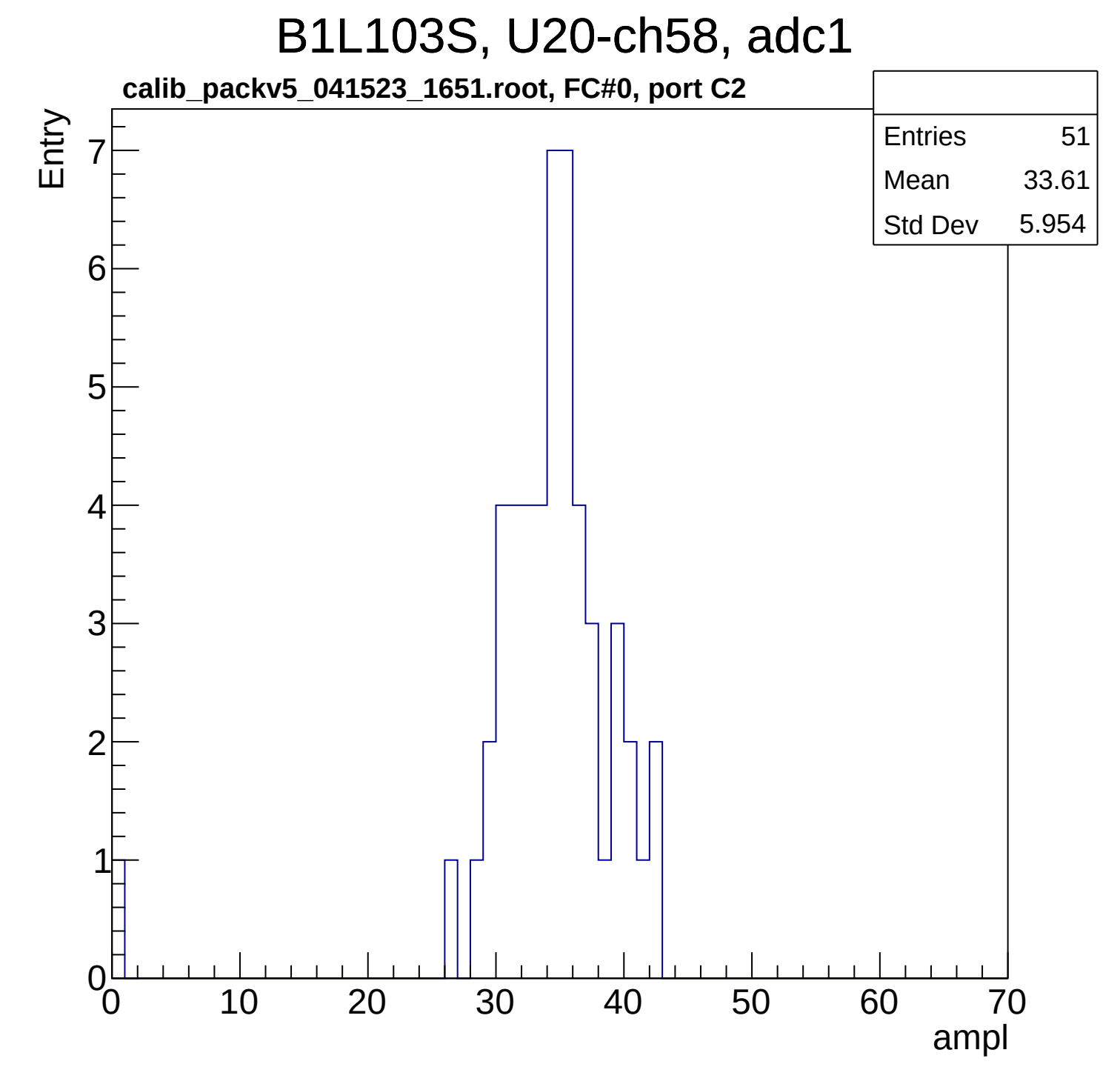
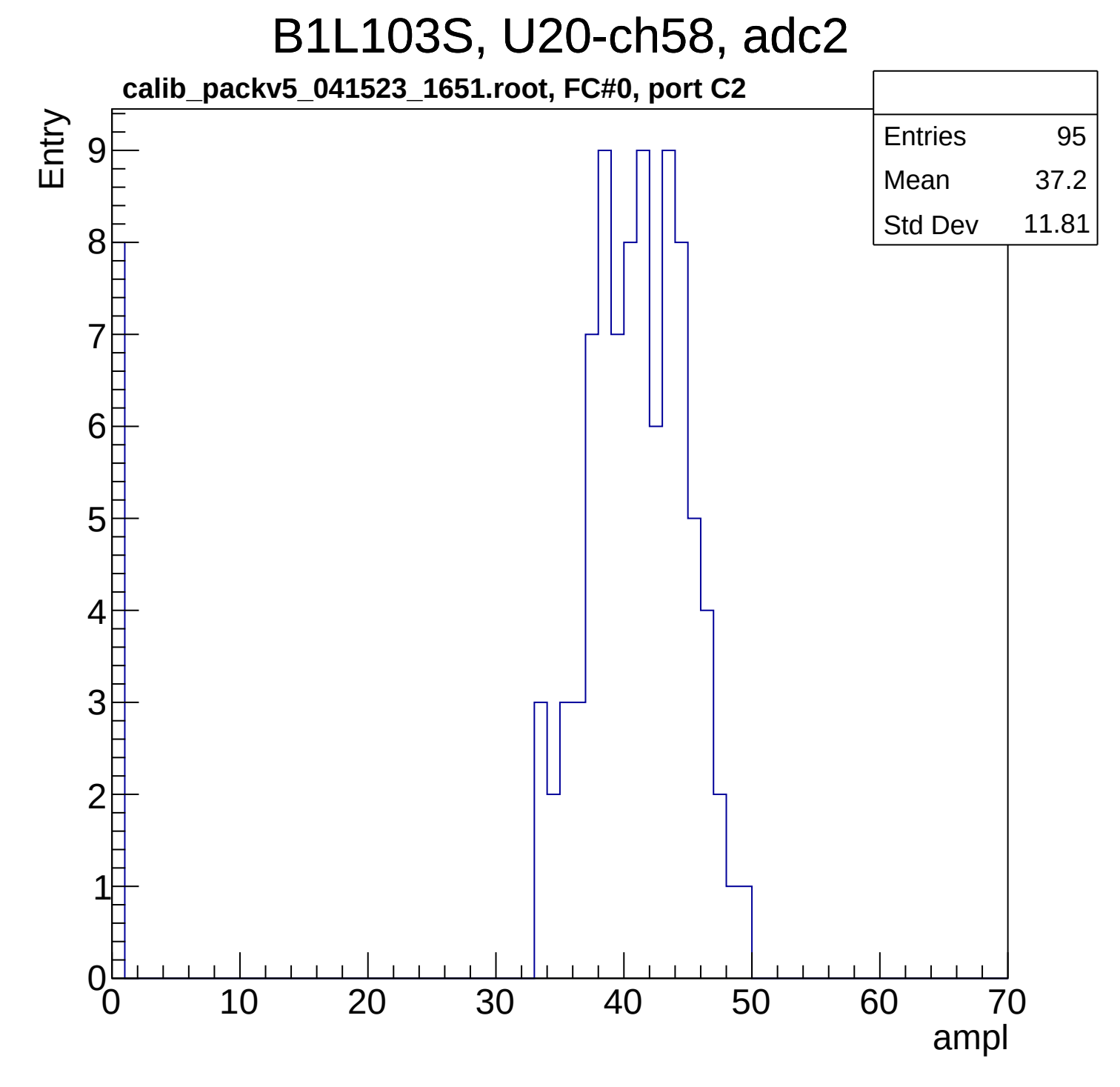
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9

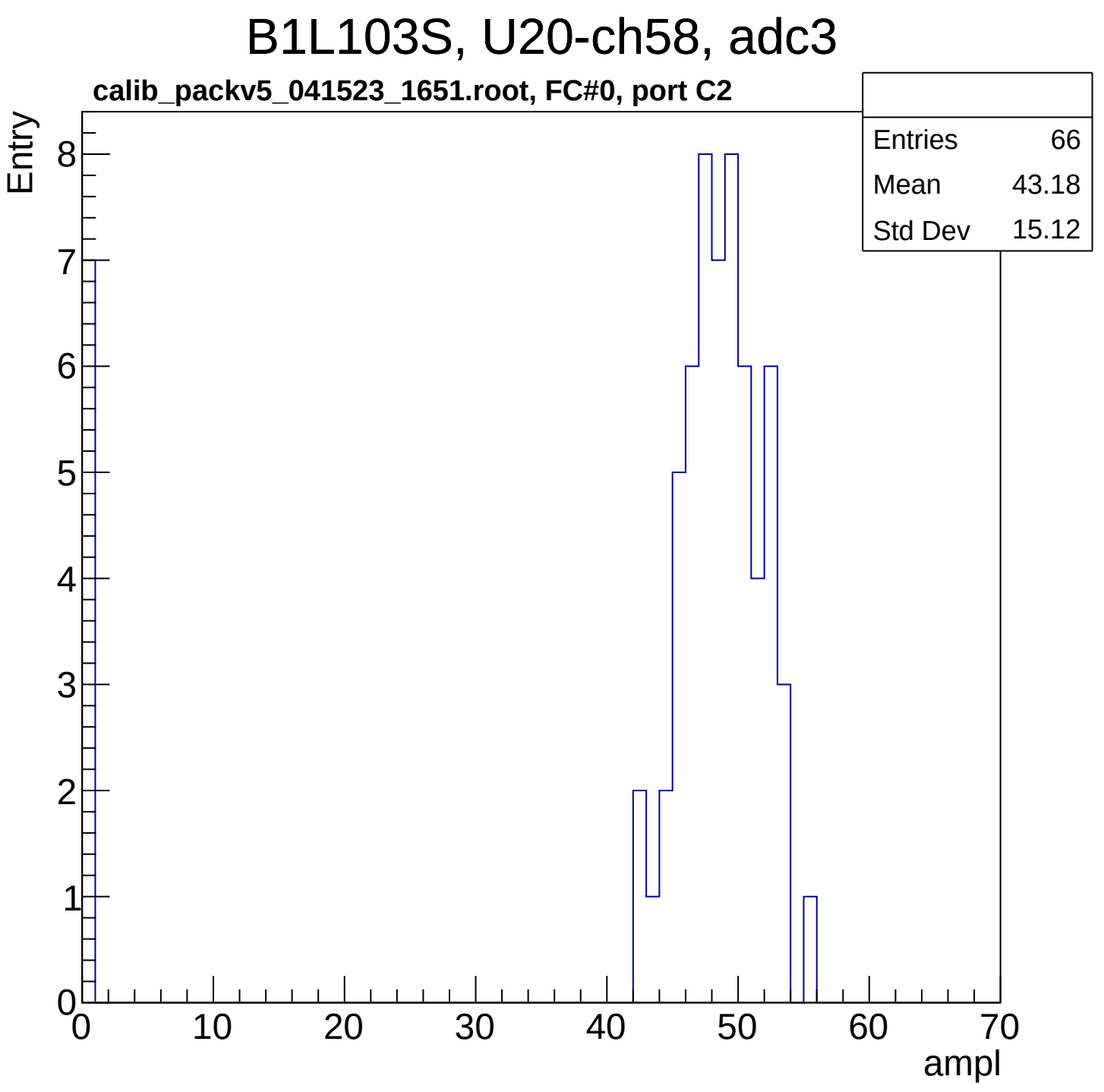

B1L103S, U20-ch57, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 61.67
Std Dev 1.247
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U20-ch57, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch58, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 23.7
Std Dev 10.83
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch58, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 33.61
Std Dev 5.954
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U20-ch58, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 37.2
Std Dev 11.81
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch58, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 43.18
Std Dev 15.12
Entry
ampl
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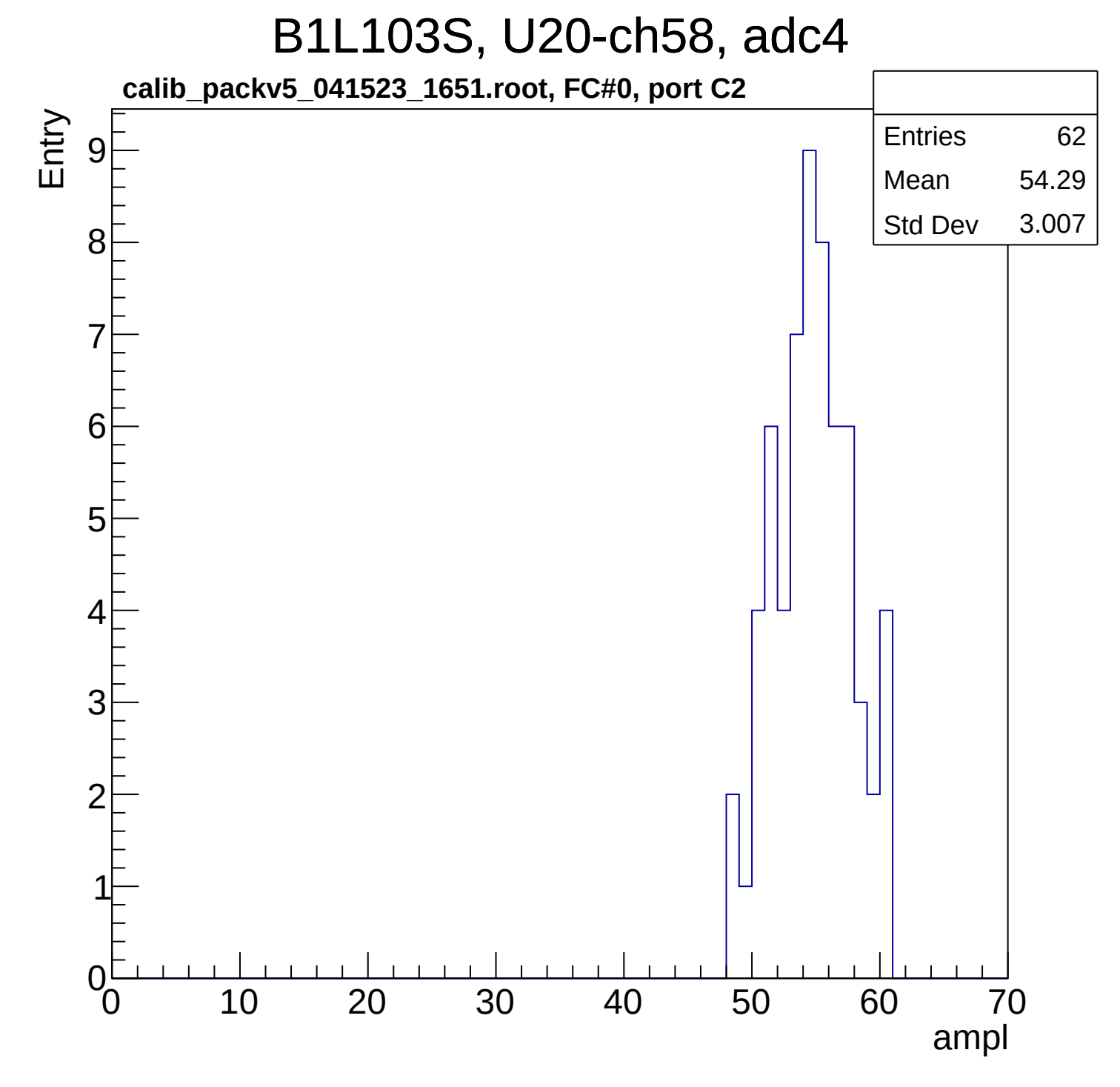
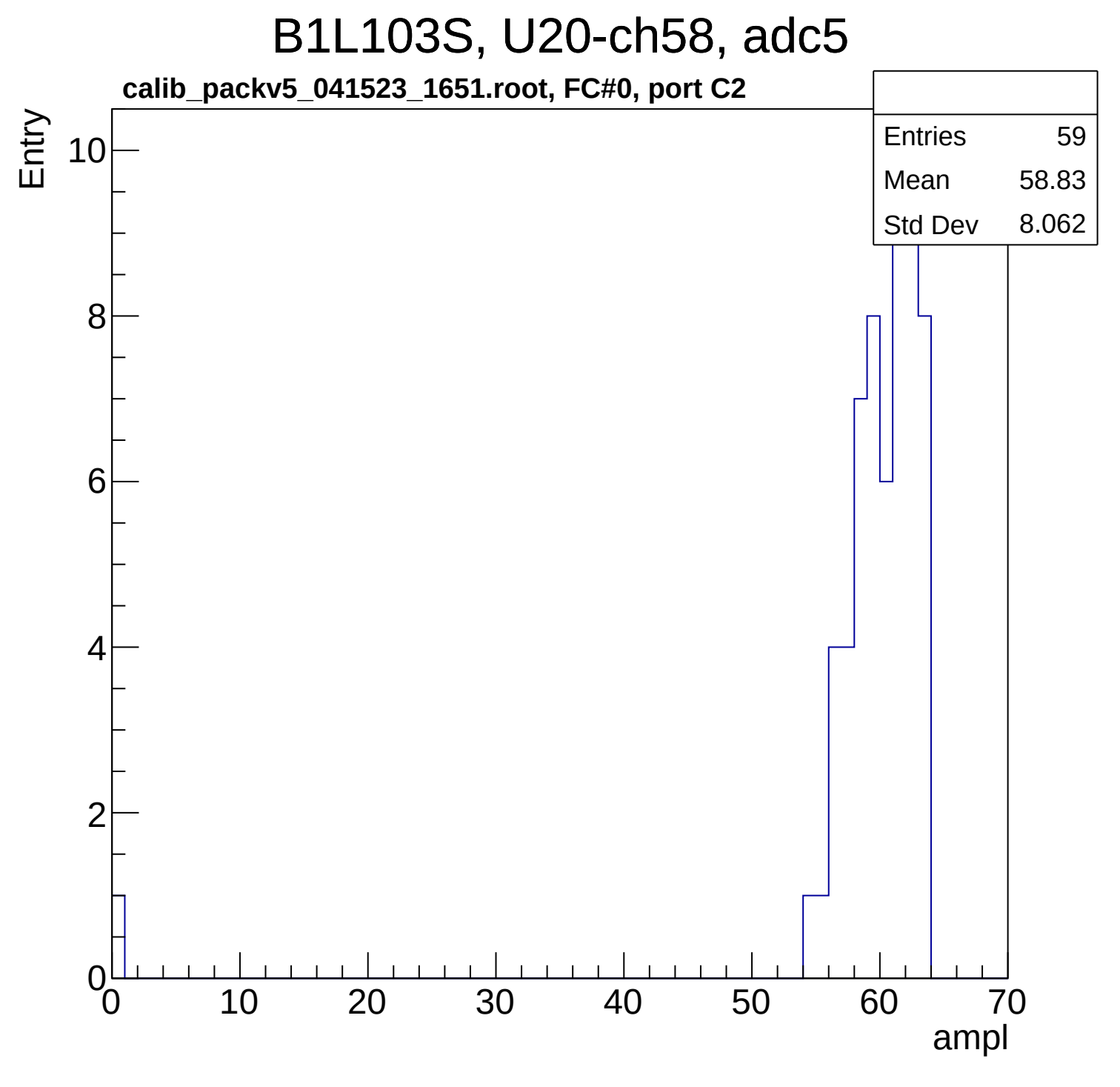
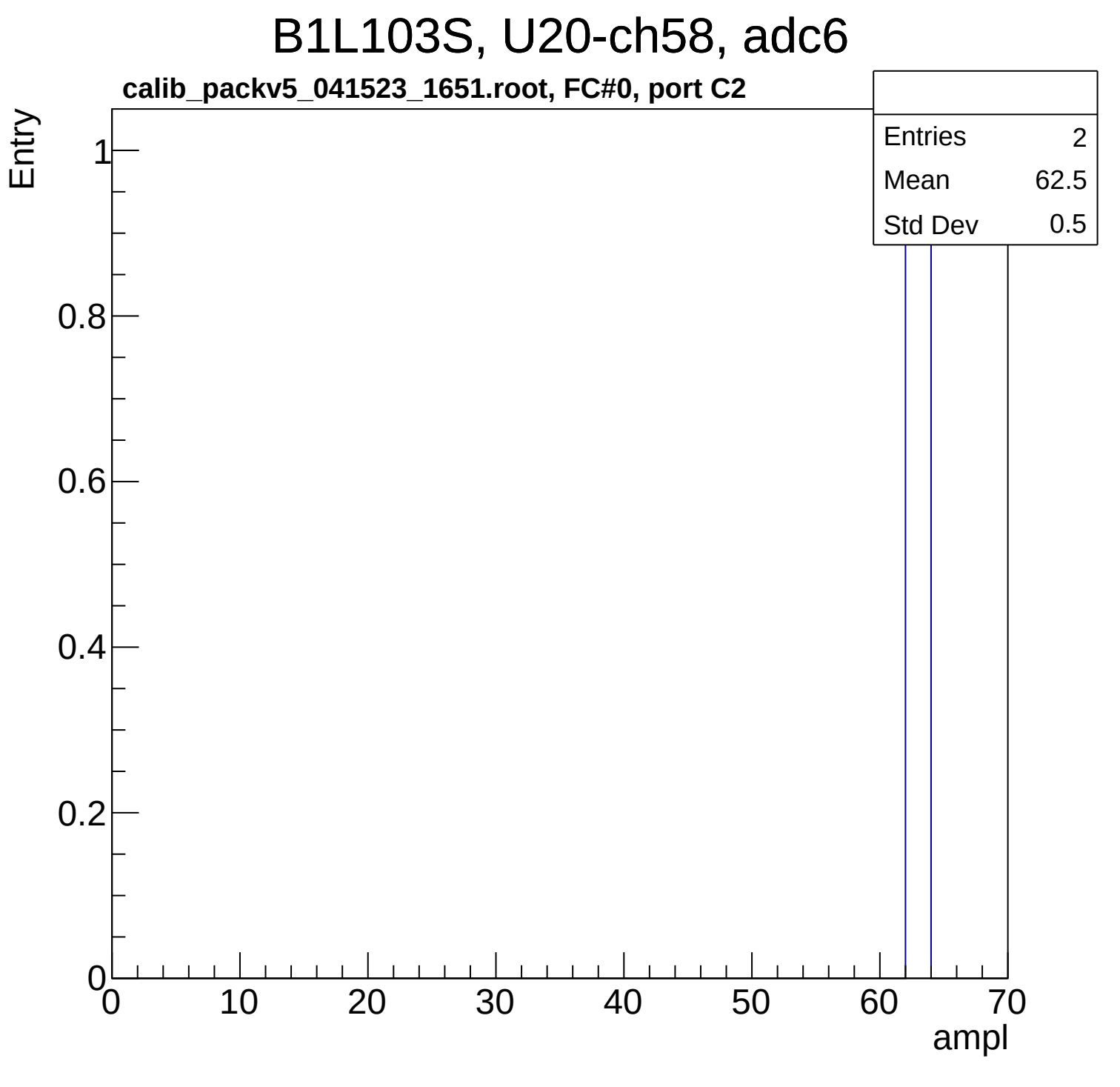
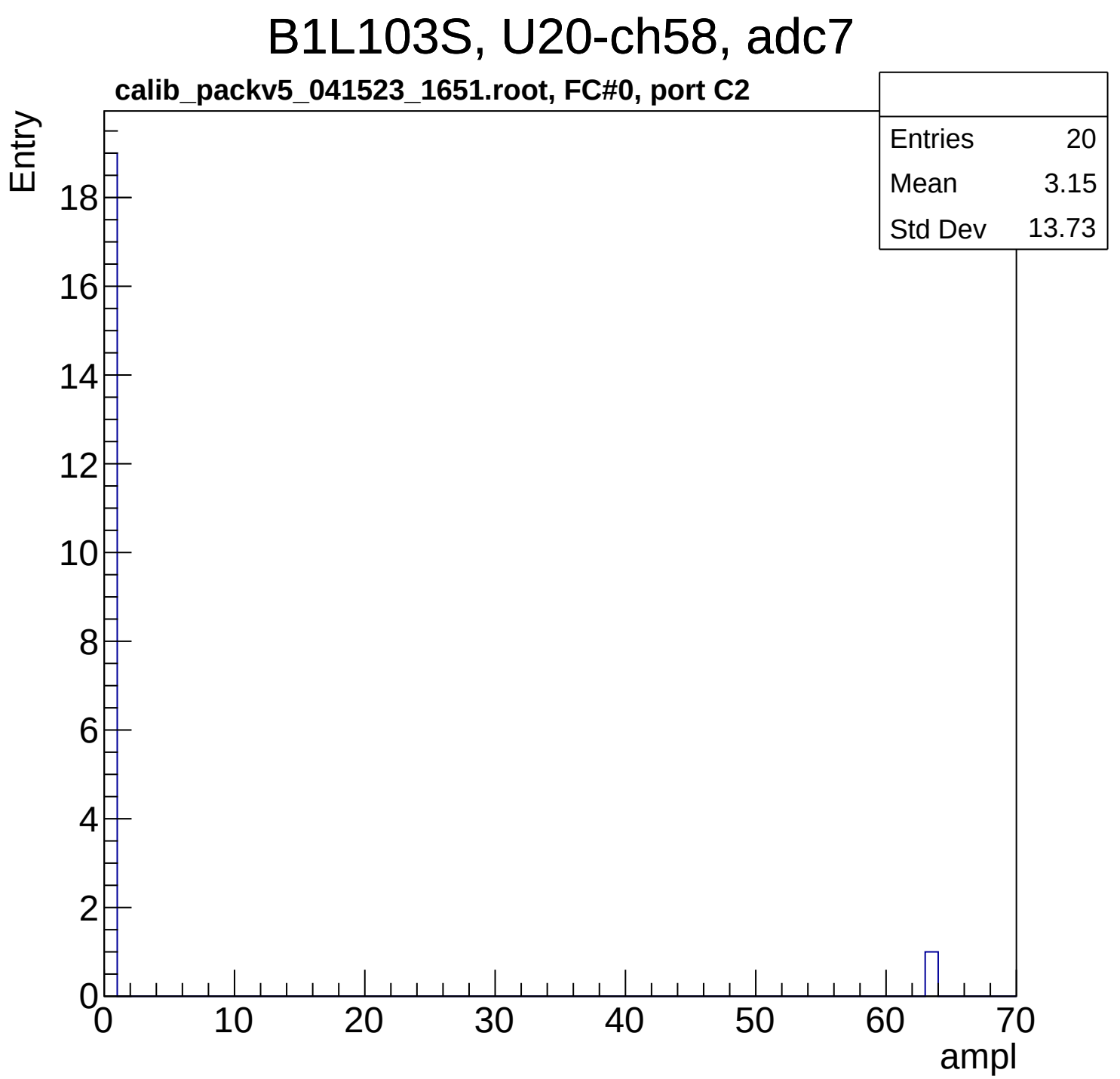
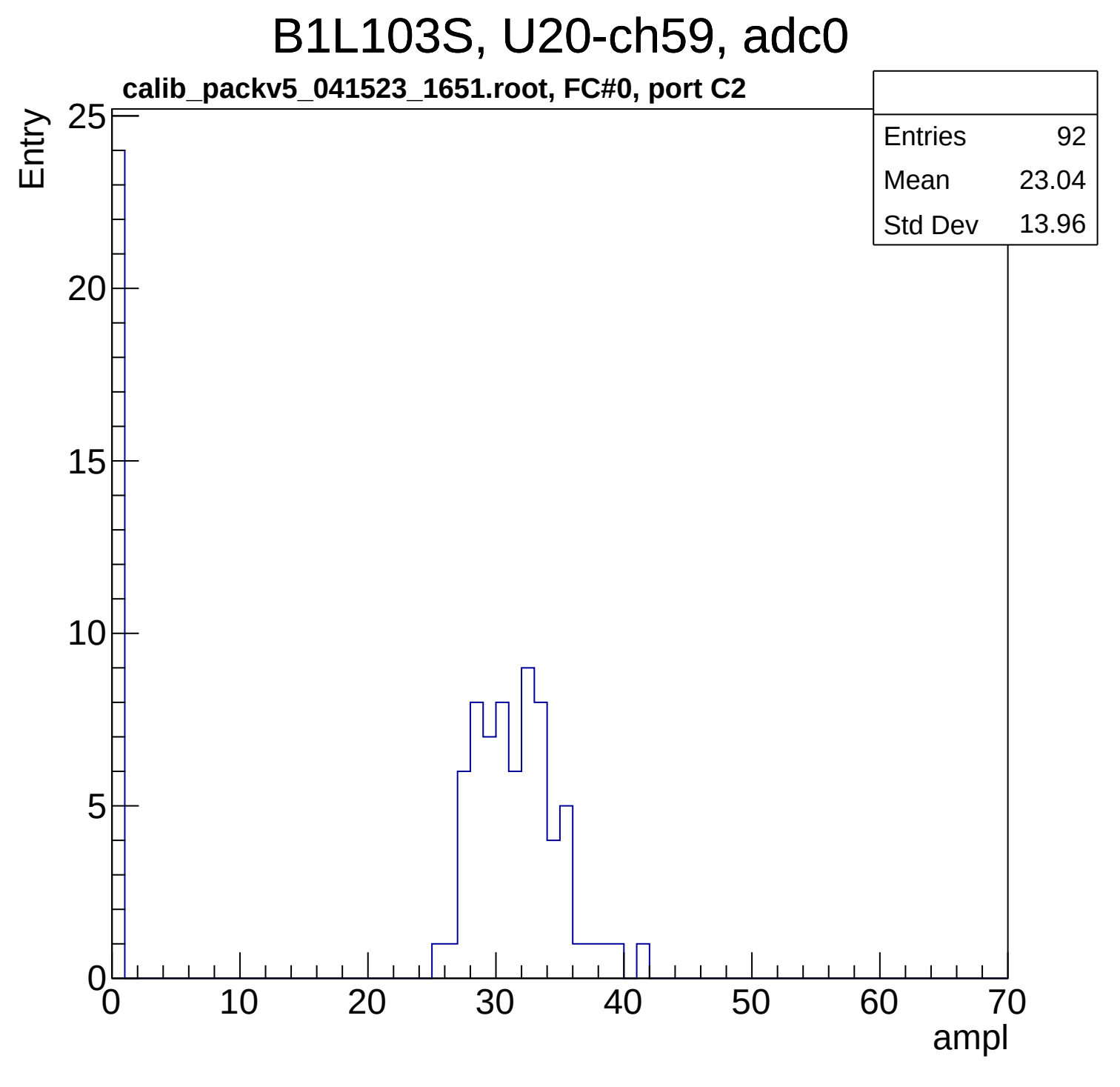
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

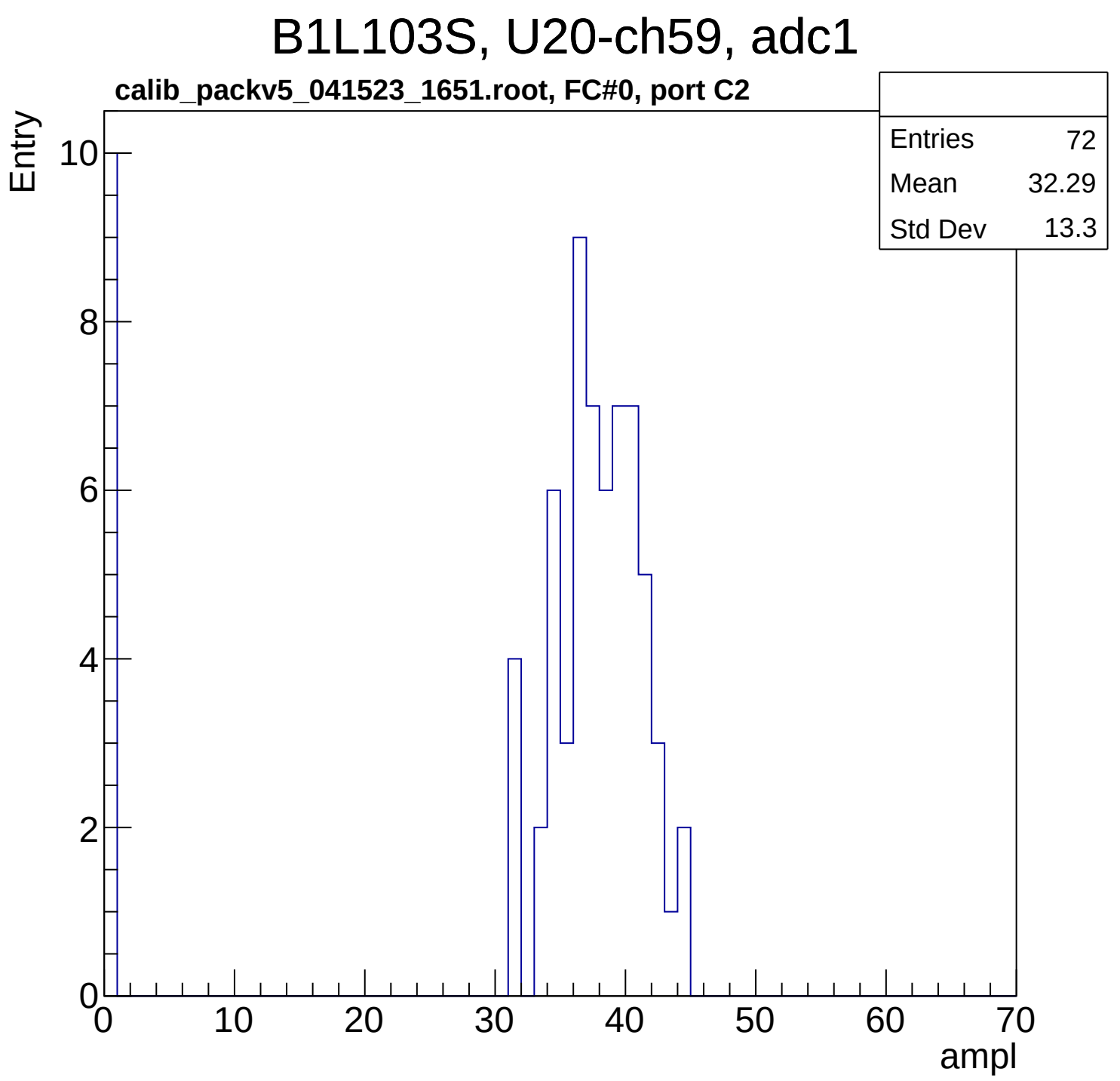

B1L103S, U20-ch58, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 54.29
Std Dev 3.007
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

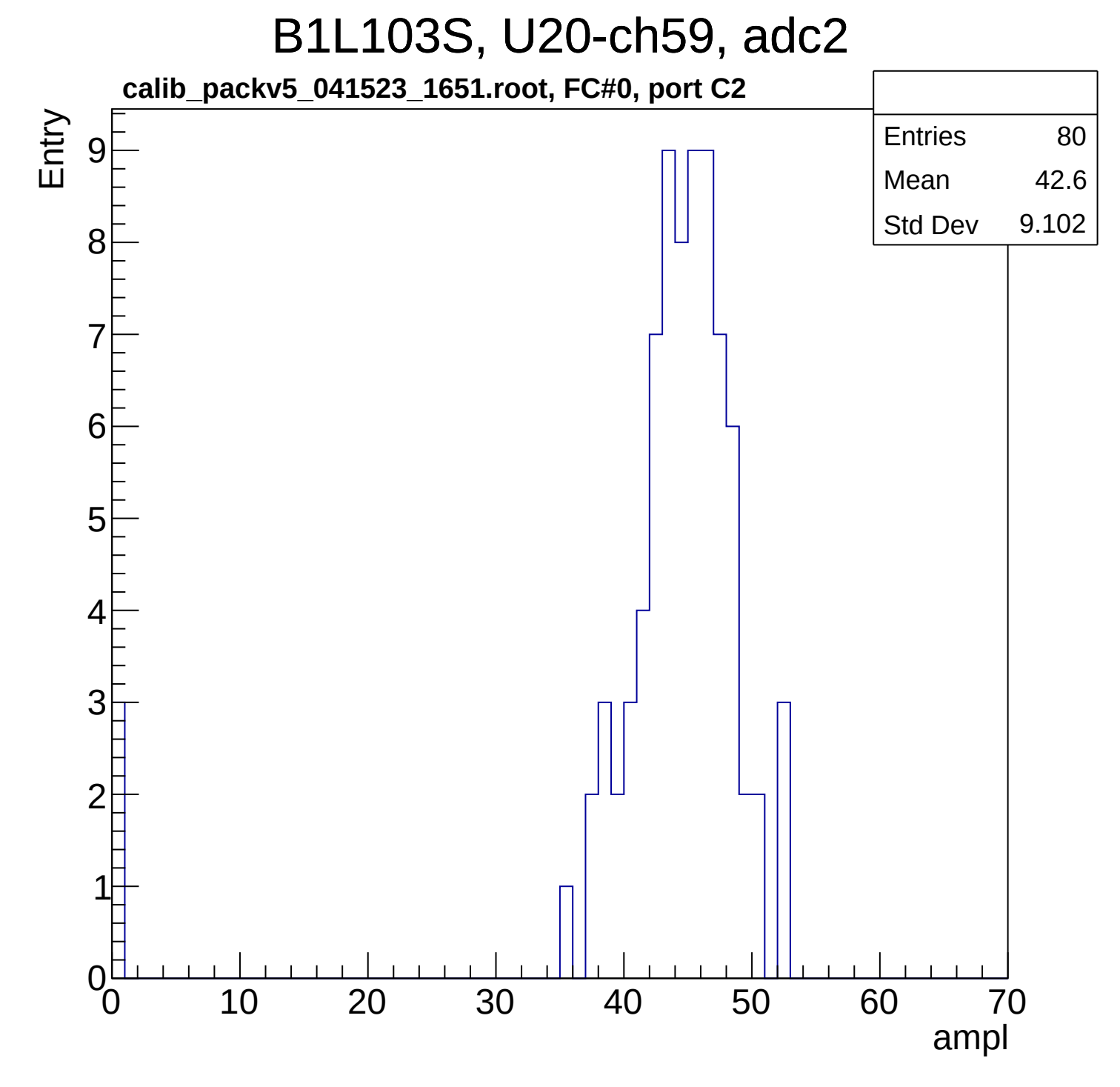

B1L103S, U20-ch58, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 58.83
Std Dev 8.062
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch58, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch58, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch59, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 23.04
Std Dev 13.96
Entry
ampl
0
5
10
15
20
25
0
10
20
30
40
50
60
70


B1L103S, U20-ch59, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 32.29
Std Dev 13.3
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch59, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 42.6
Std Dev 9.102
Entry
ampl
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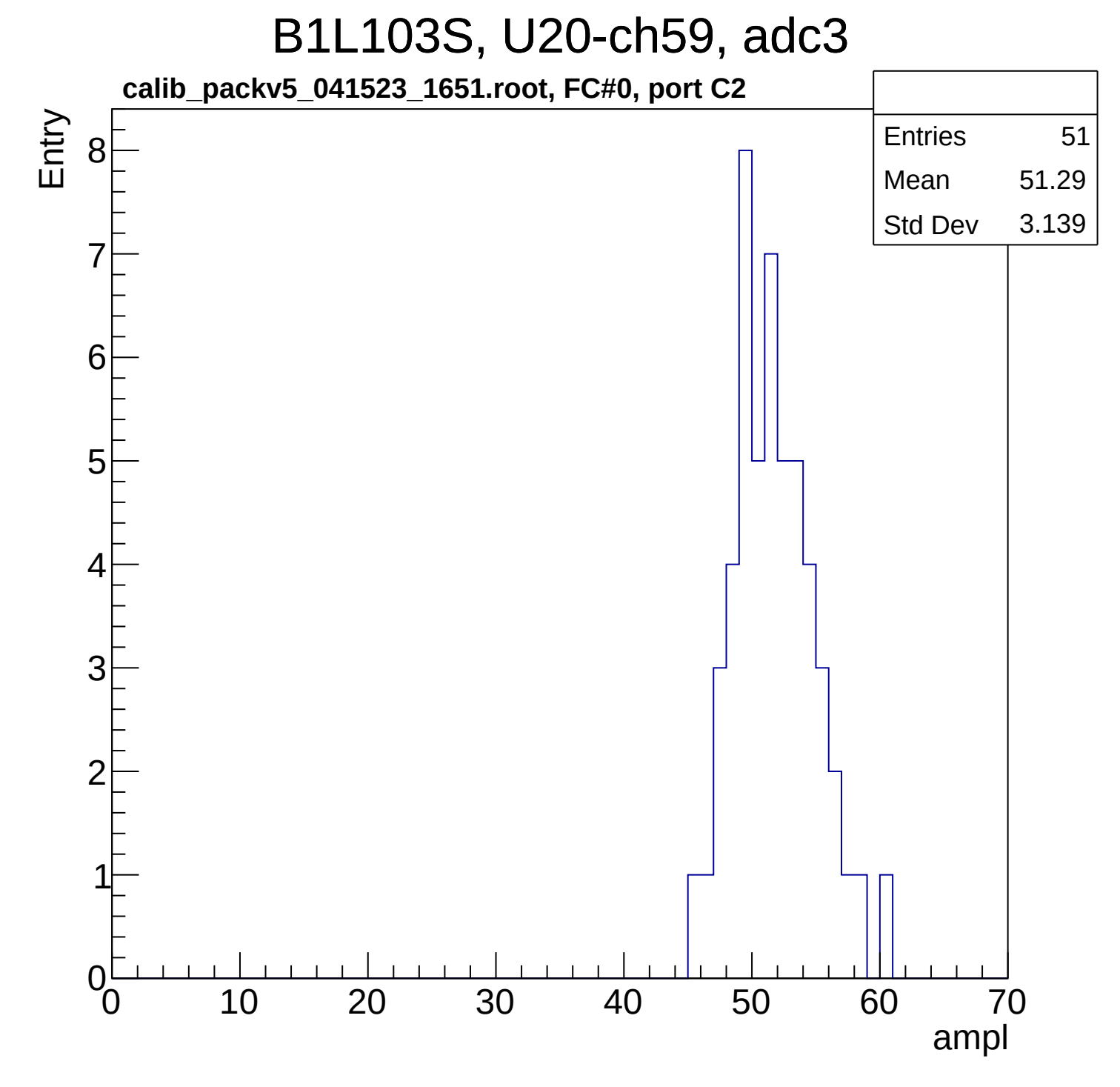
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch59, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 51.29
Std Dev 3.139
Entry
ampl
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1
2
3
4
5
6
7
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0
10
20
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40
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60
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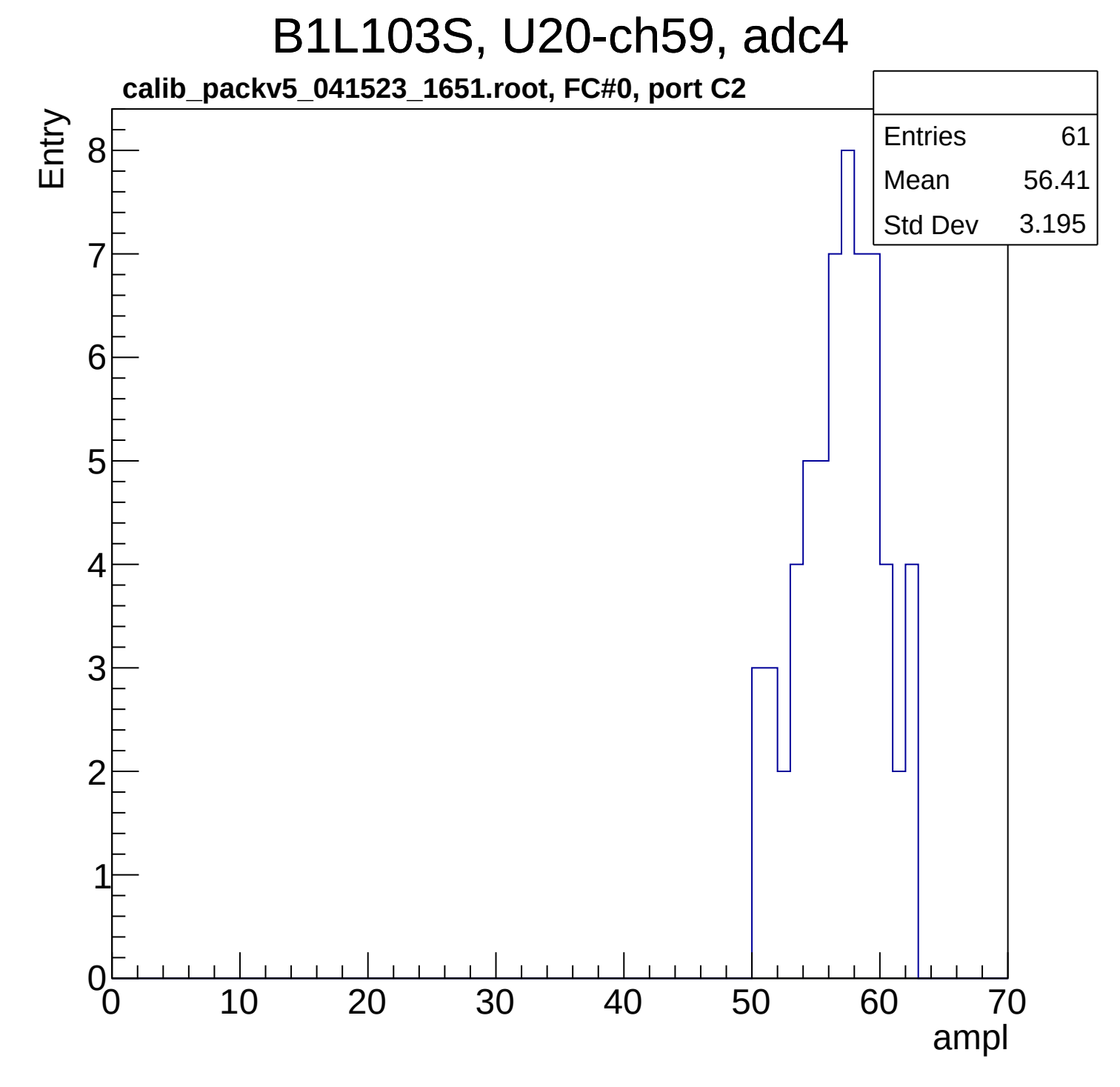
B1L103S, U20-ch59, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 56.41
Std Dev 3.195
Entry
ampl
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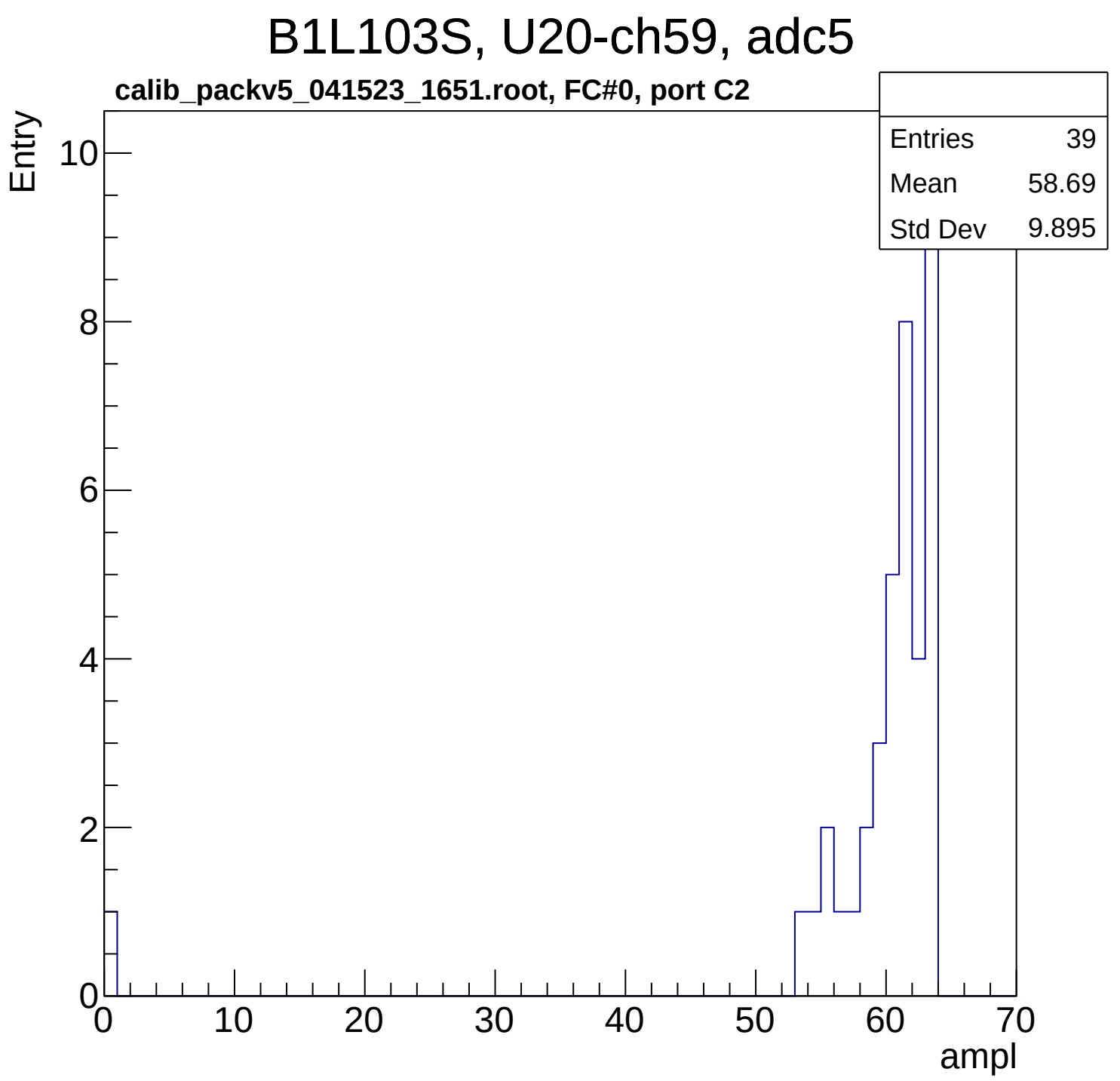
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch59, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 58.69
Std Dev 9.895
Entry
0
2
4
6
8
10
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10
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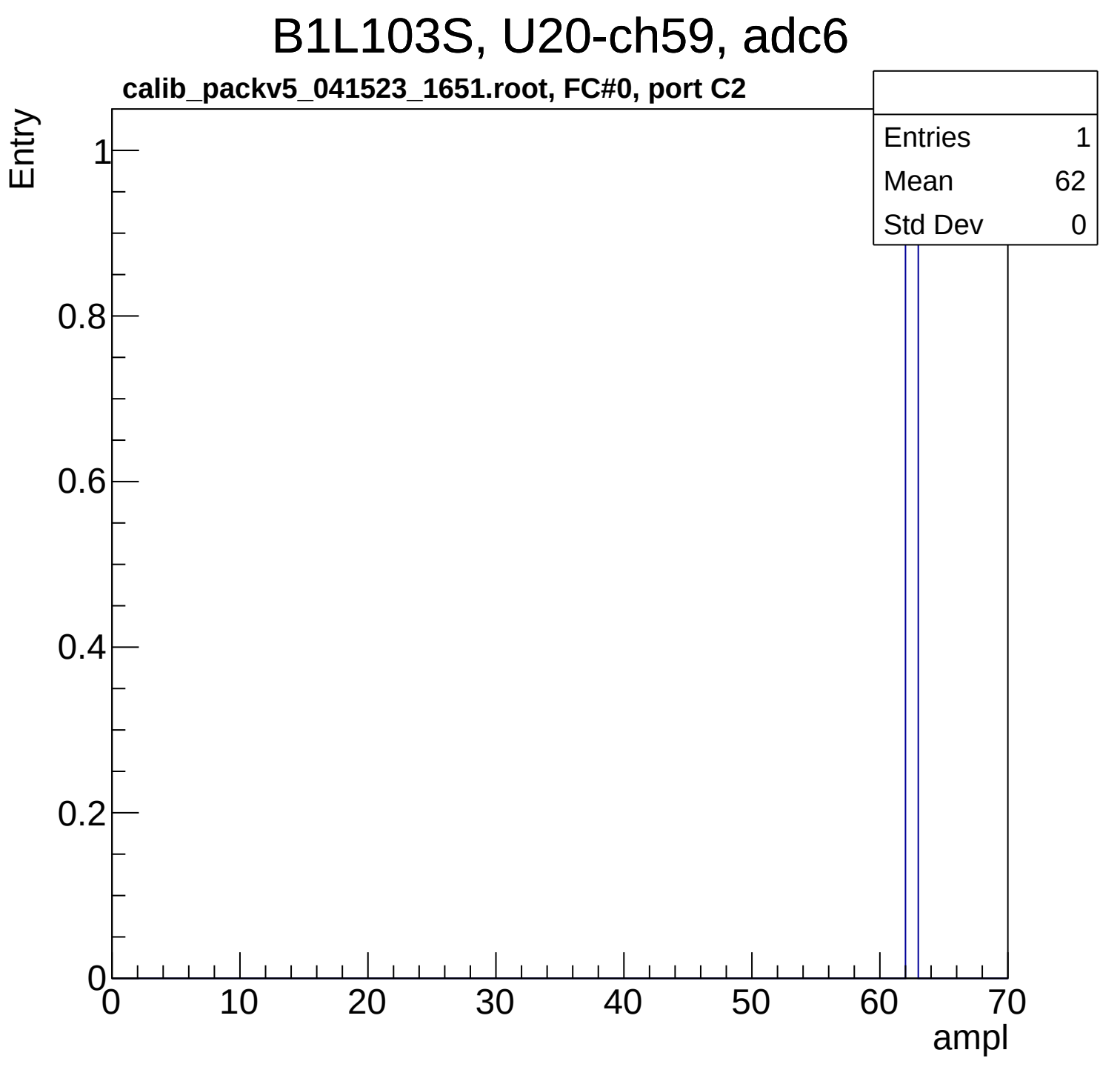
50
60
70
ampl


B1L103S, U20-ch59, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 1
Mean 62
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
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10
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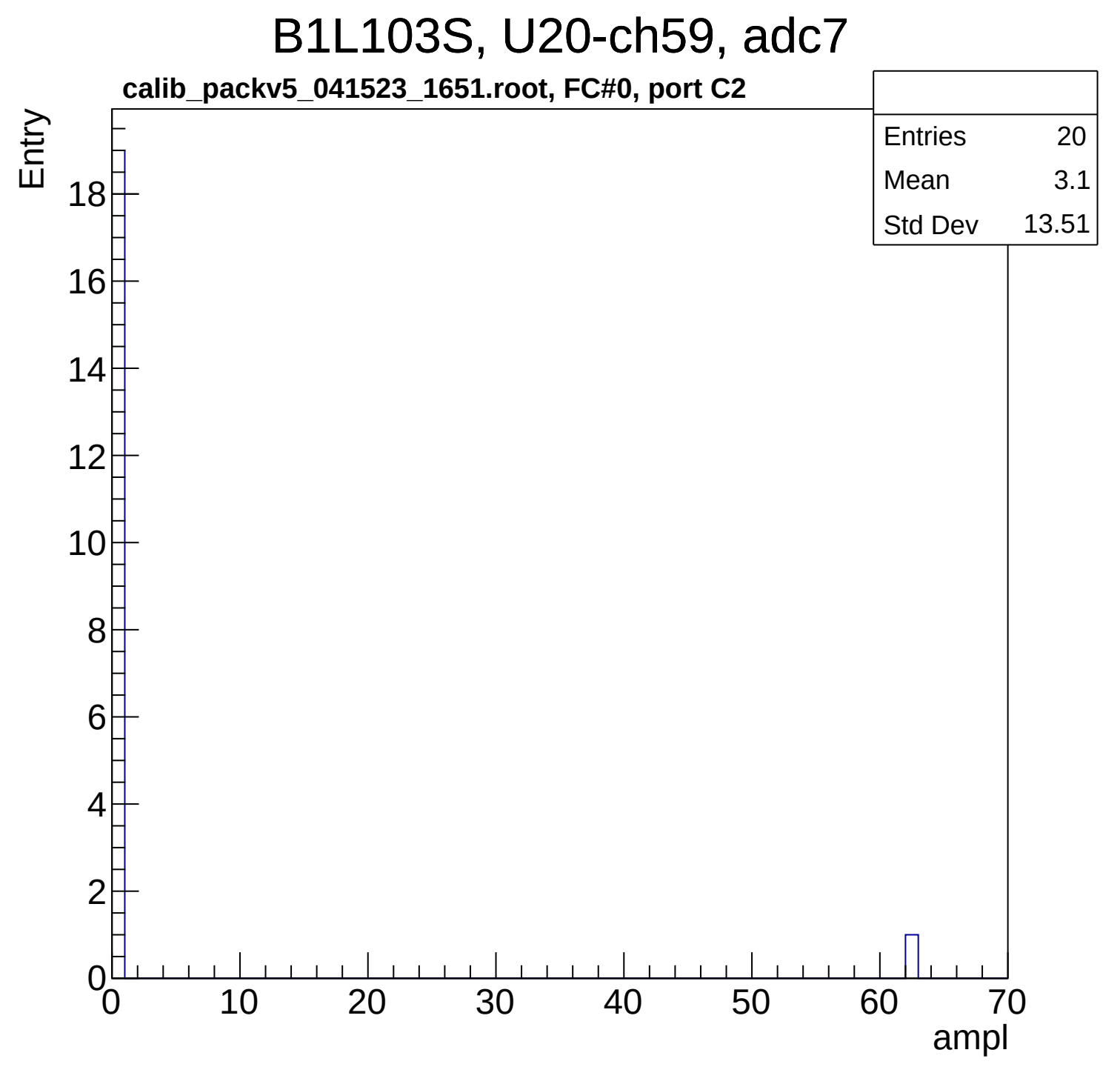
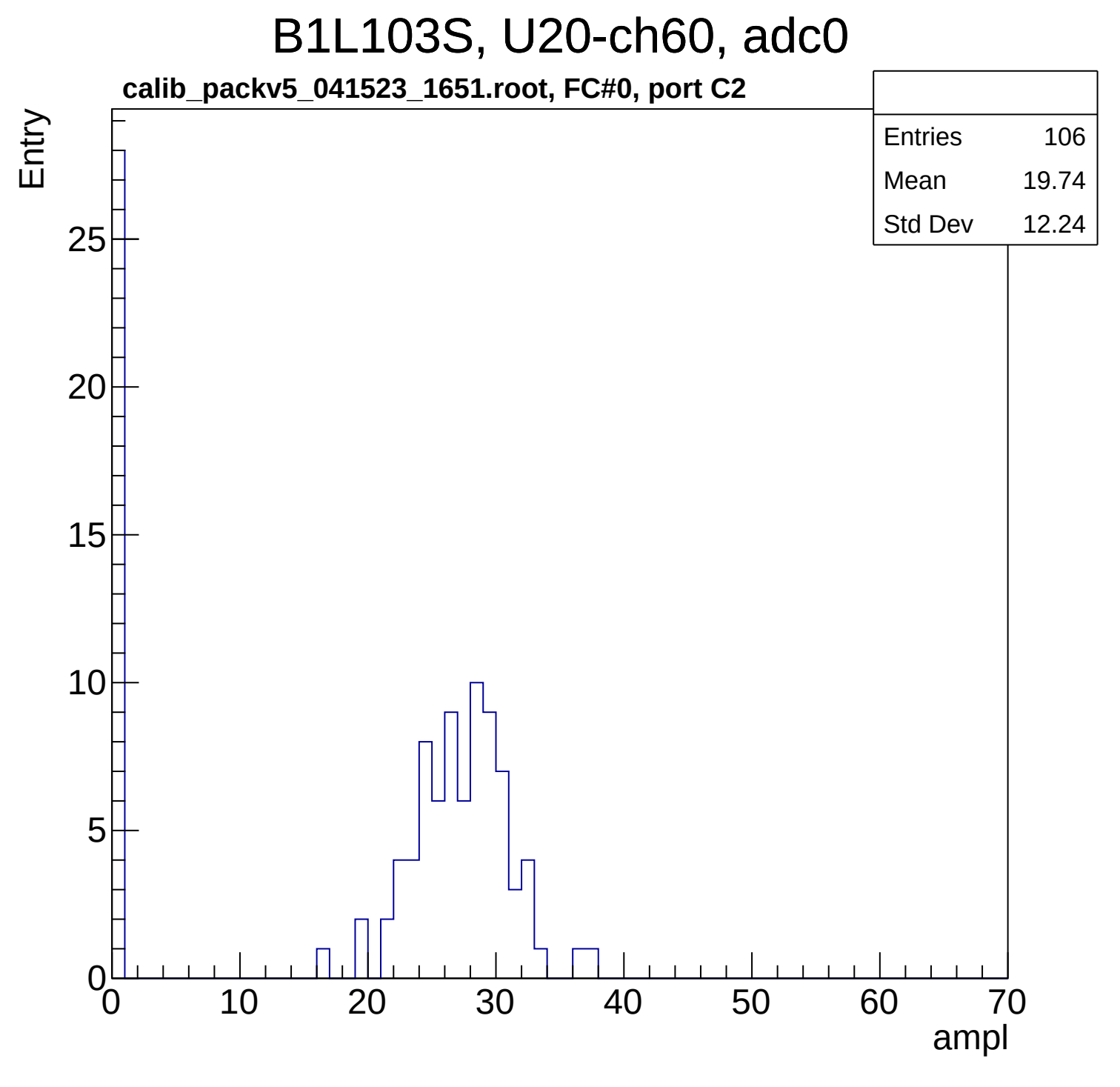
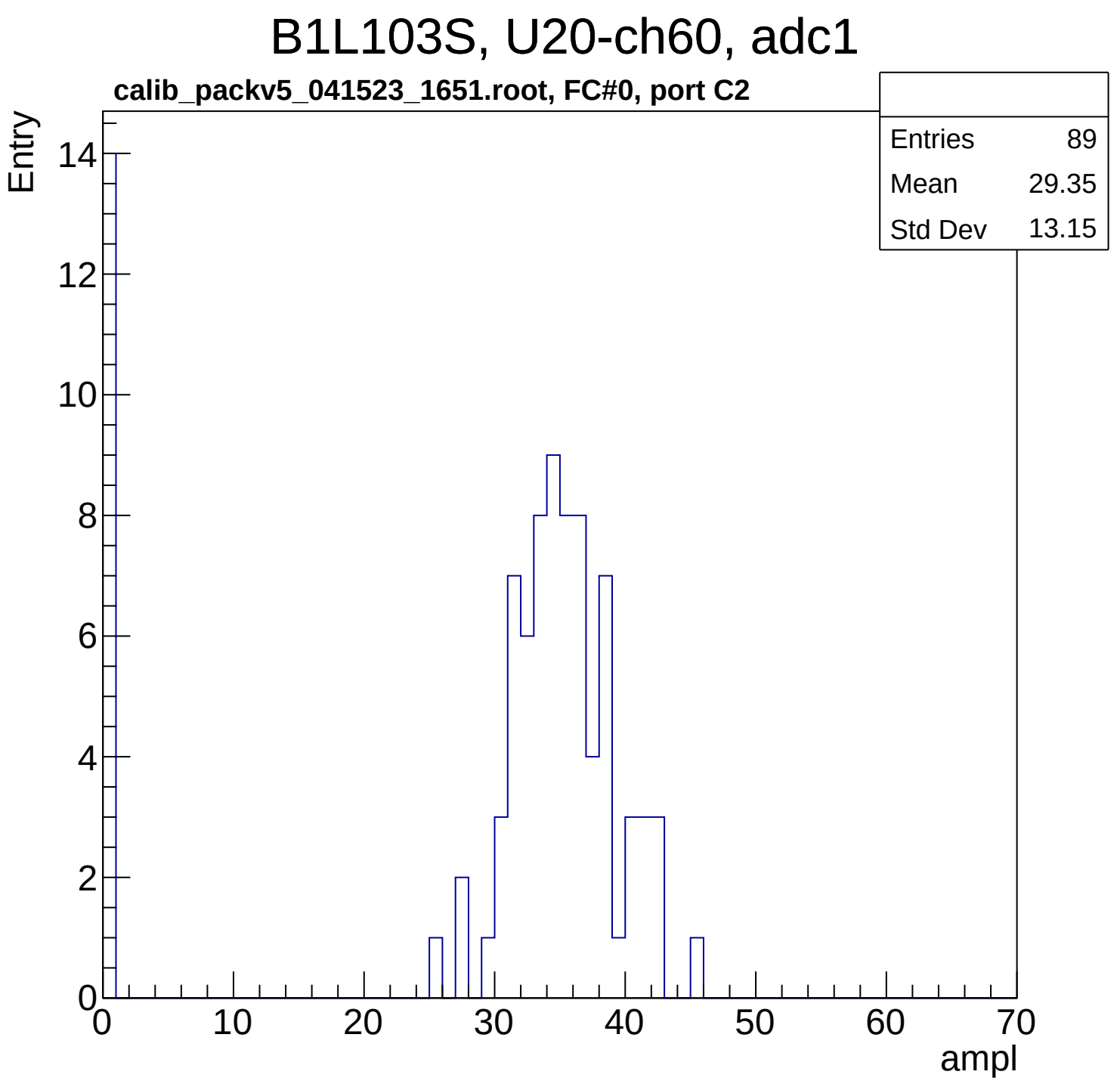
70
ampl


B1L103S, U20-ch59, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch60, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 106
Mean 19.74
Std Dev 12.24
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch60, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 29.35
Std Dev 13.15
Entry
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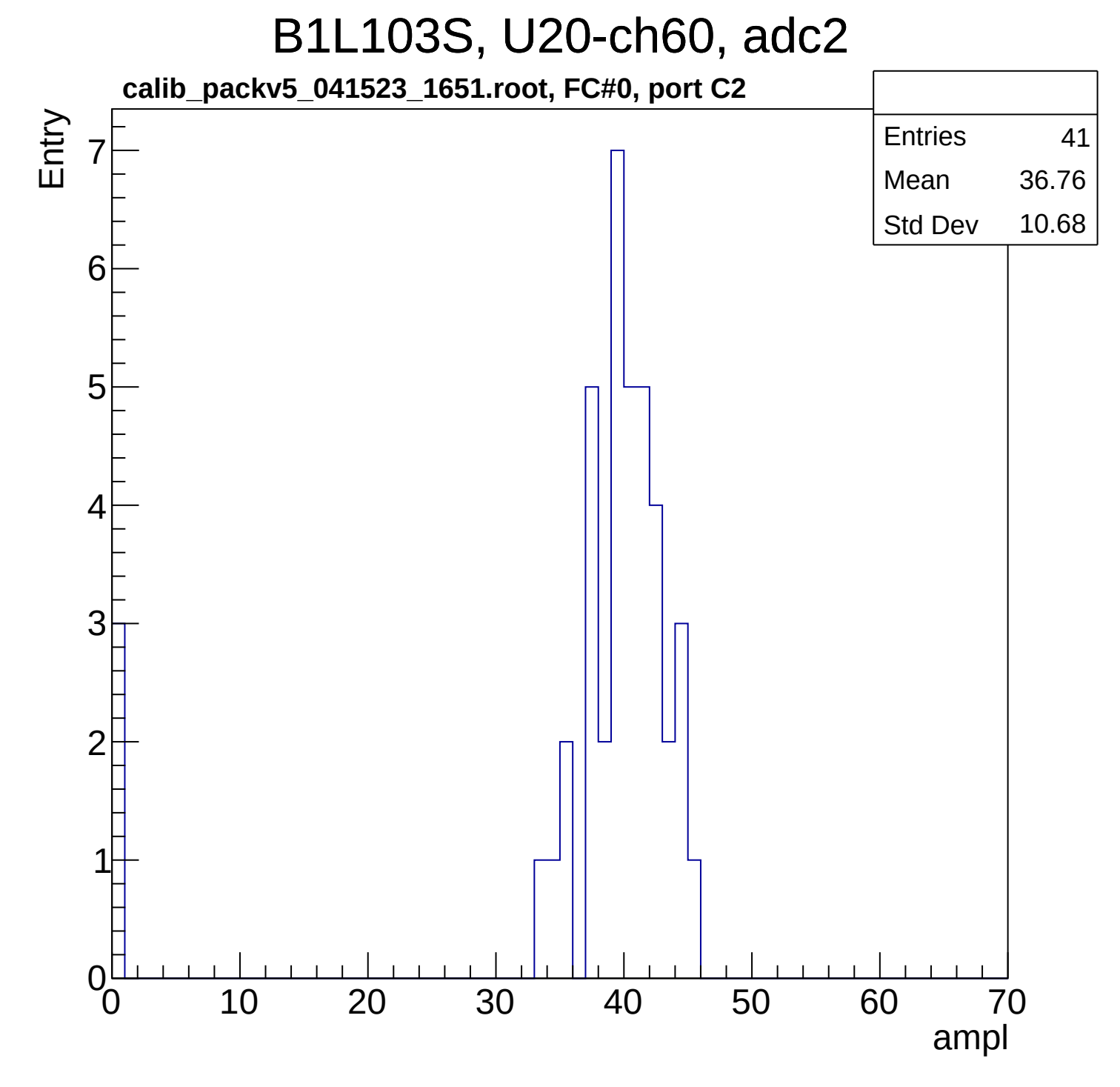
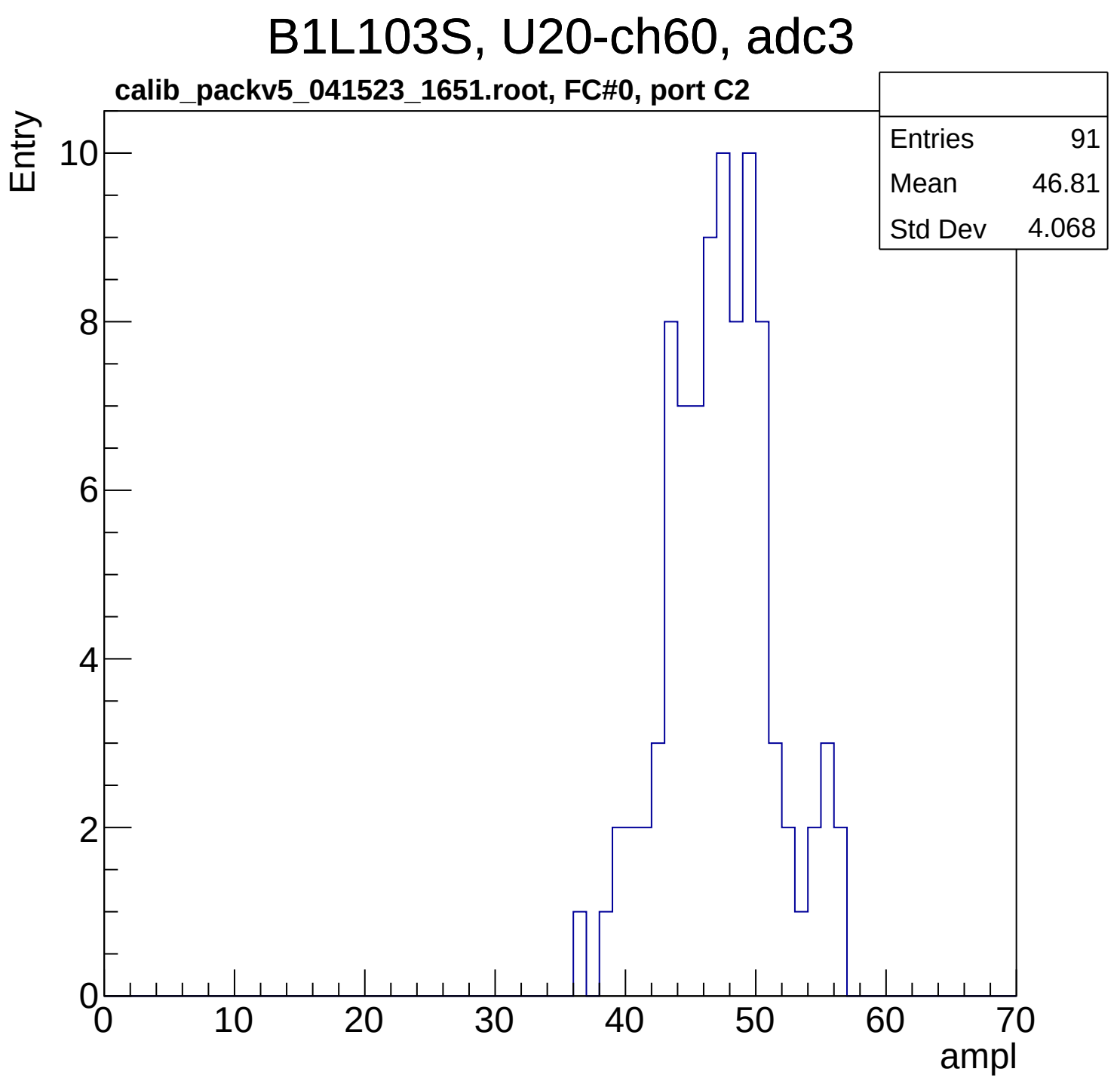
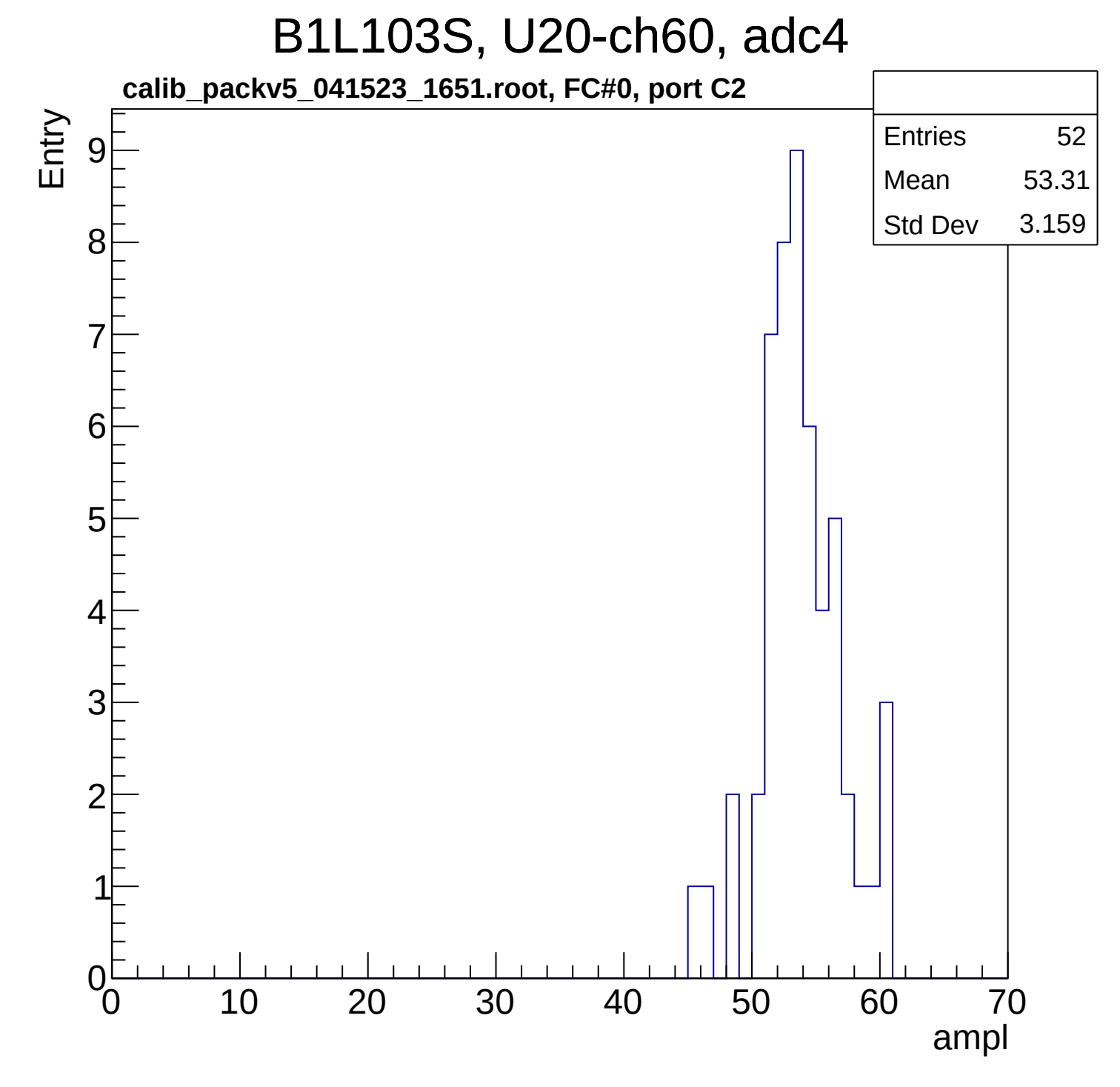
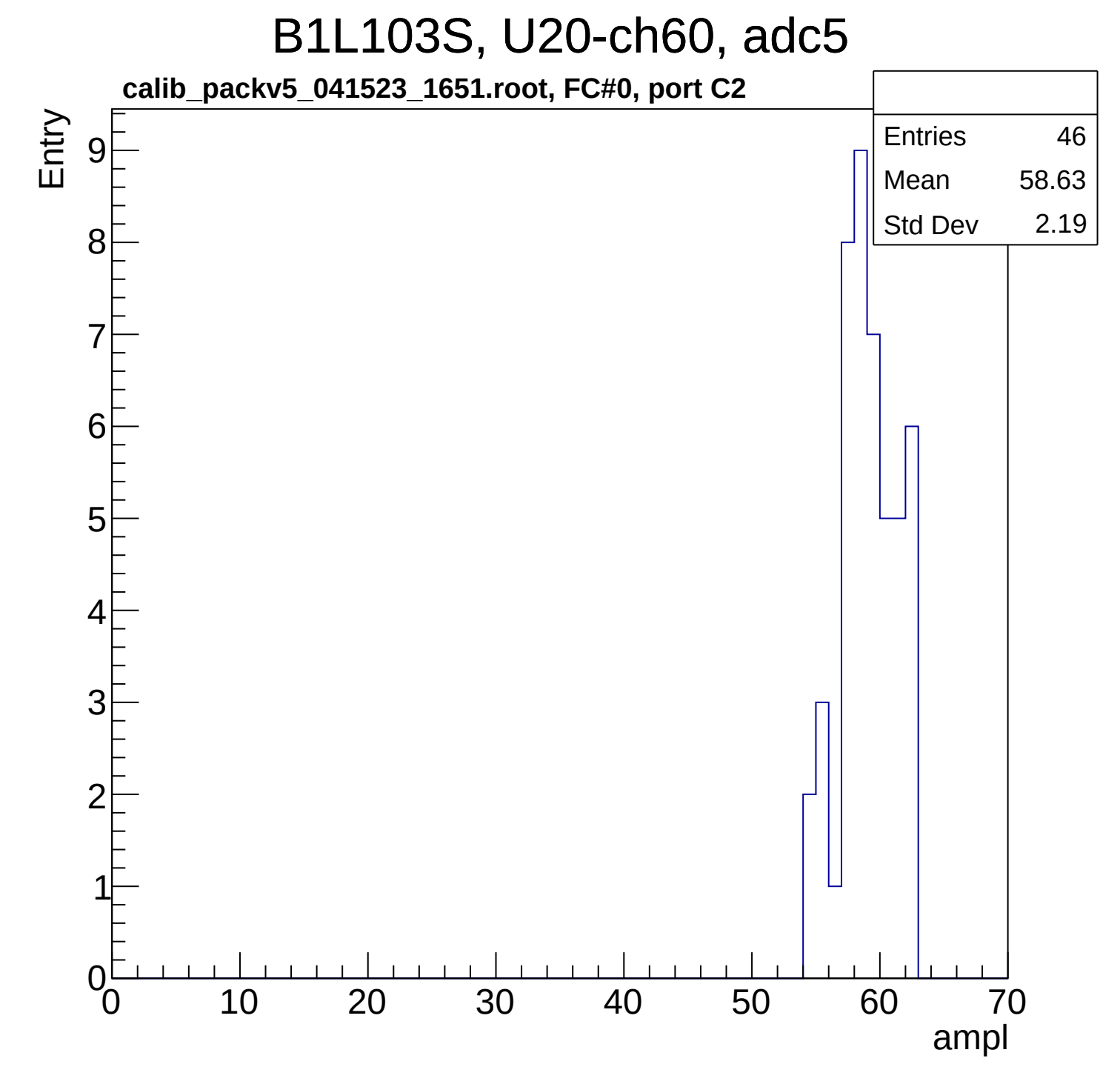
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch60, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 36.76
Std Dev 10.68
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U20-ch60, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 46.81
Std Dev 4.068
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U20-ch60, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 53.31
Std Dev 3.159
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch60, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 58.63
Std Dev 2.19
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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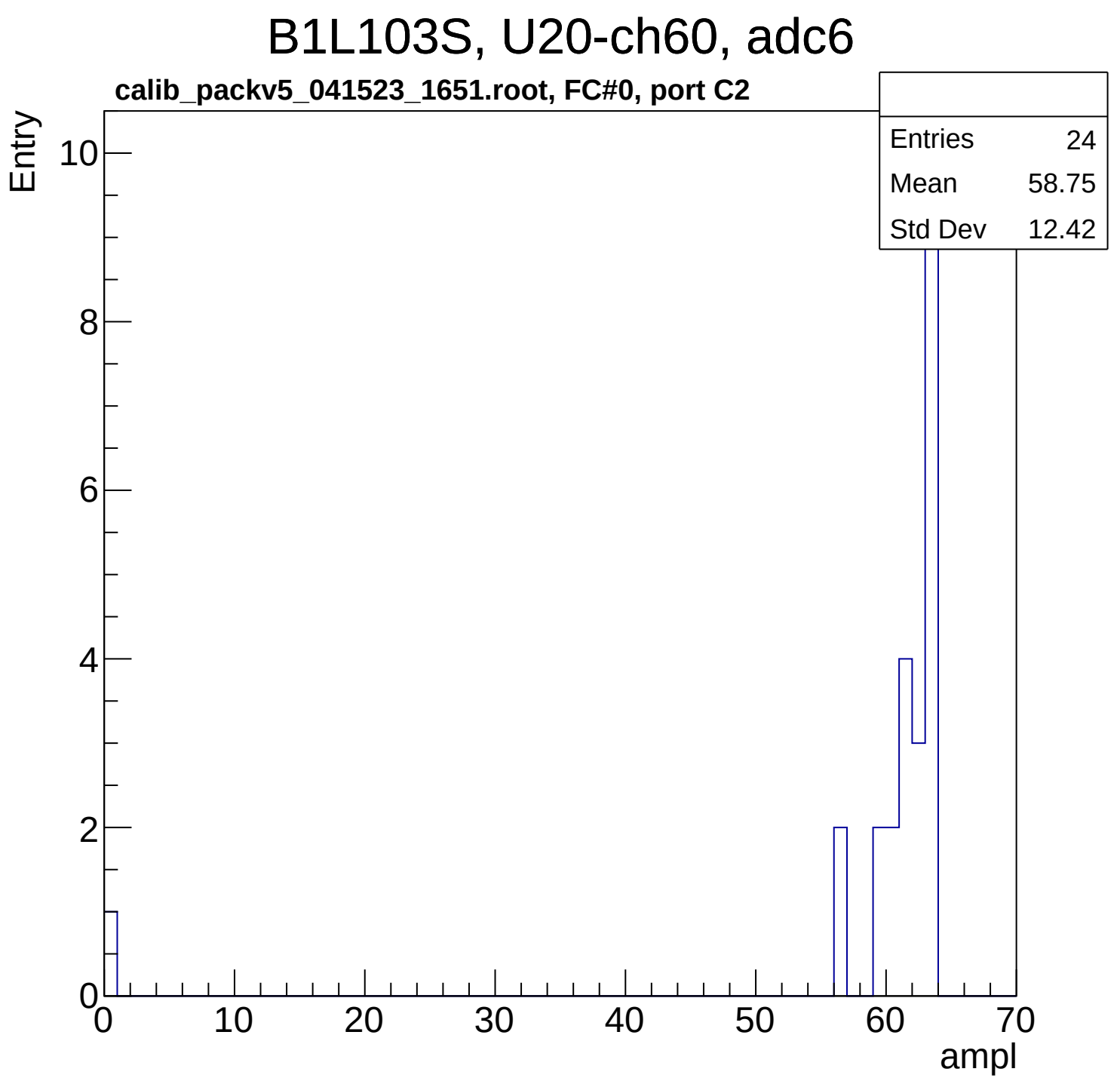
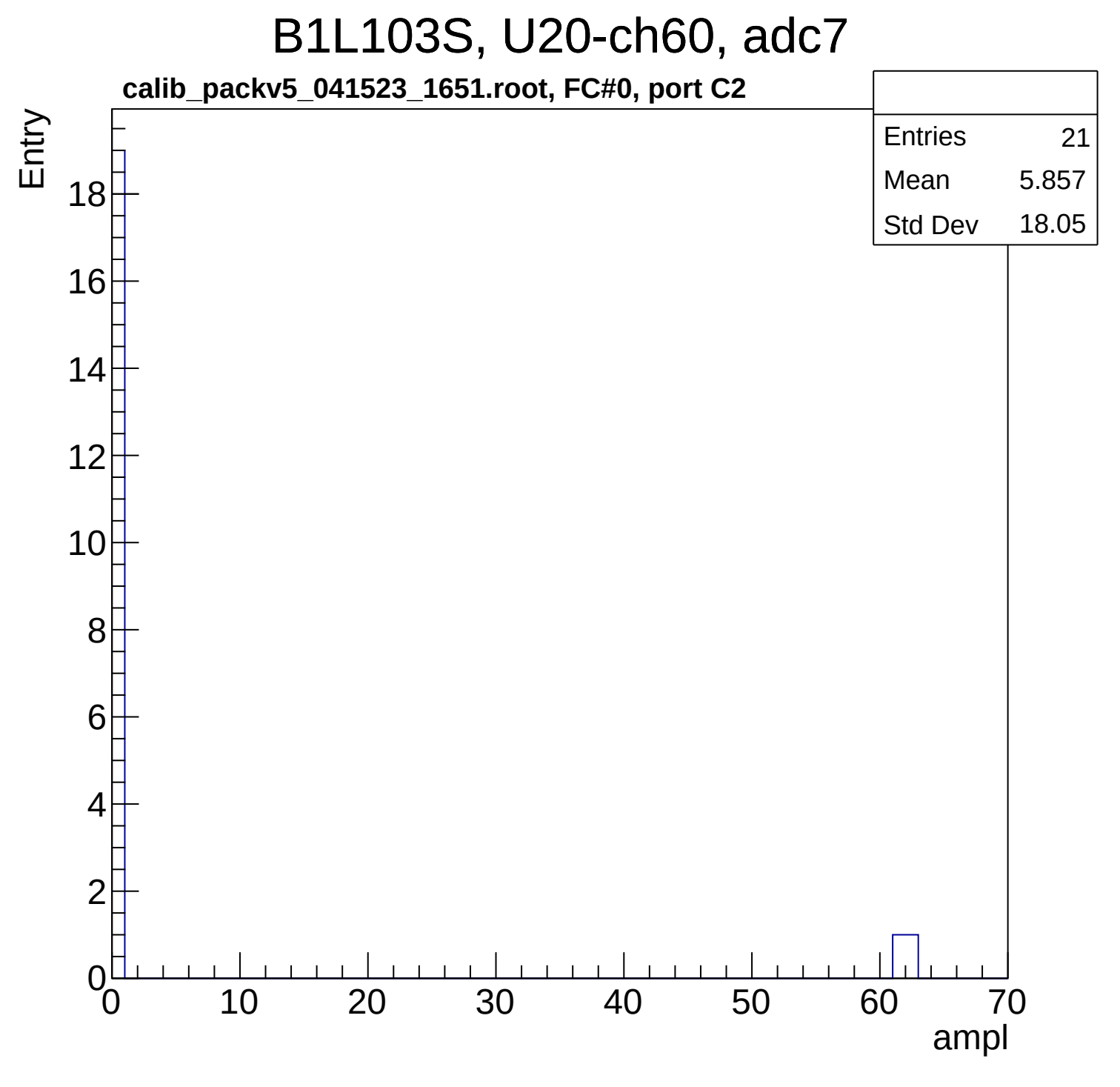

B1L103S, U20-ch60, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 58.75
Std Dev 12.42
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch60, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.857
Std Dev 18.05
Entry
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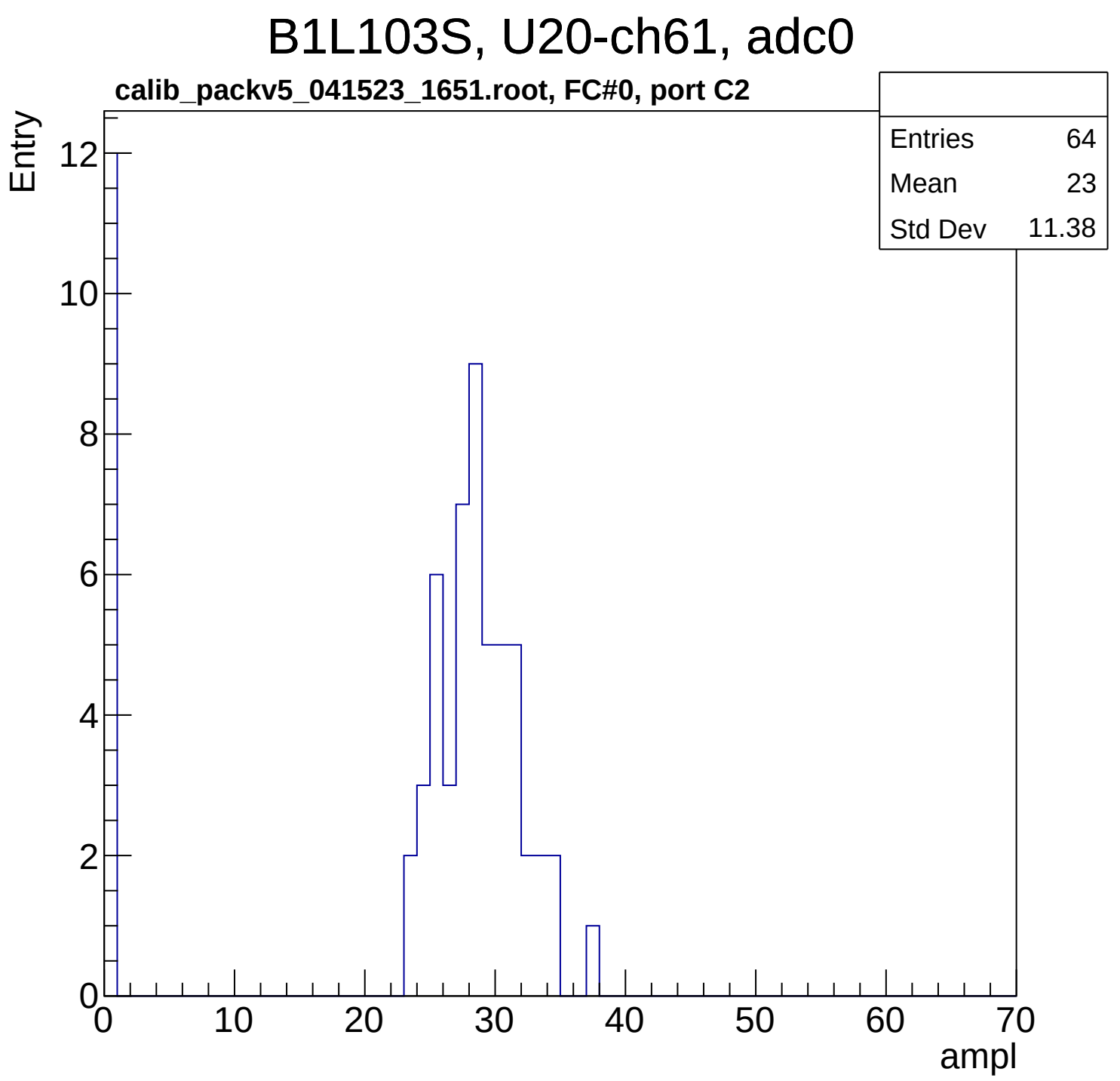
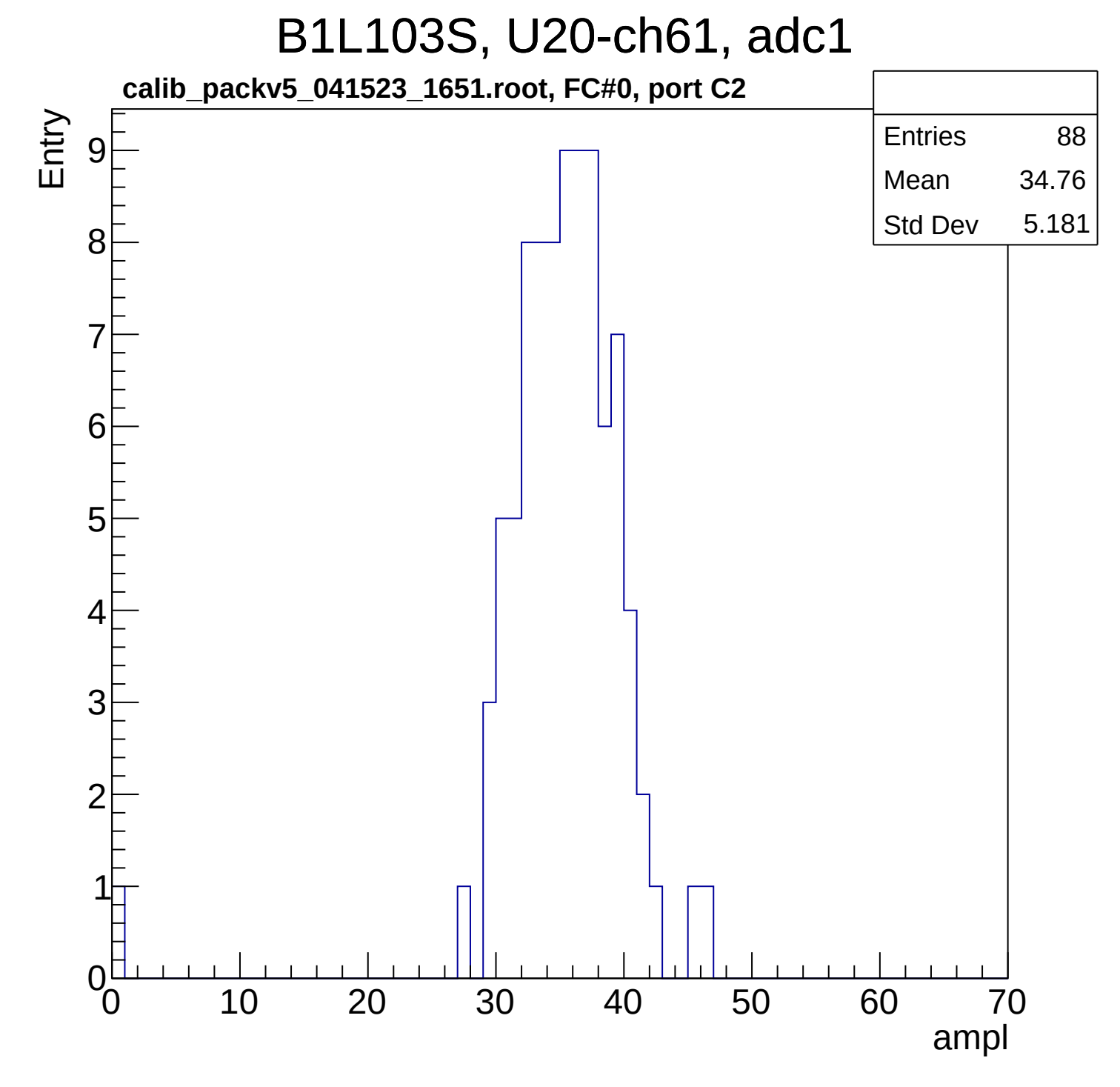
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch61, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 23
Std Dev 11.38
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch61, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 34.76
Std Dev 5.181
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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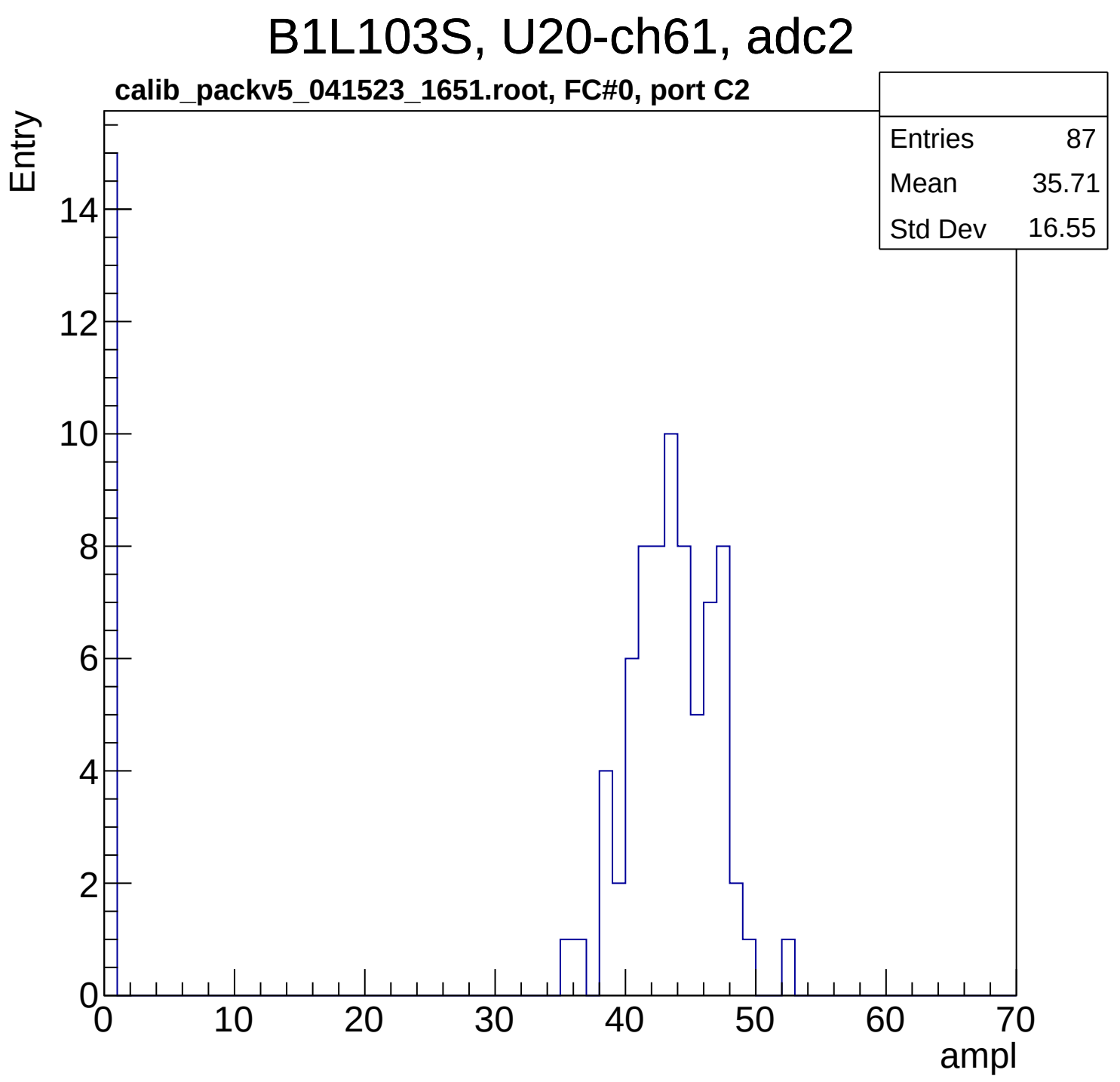
B1L103S, U20-ch61, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 35.71
Std Dev 16.55
Entry
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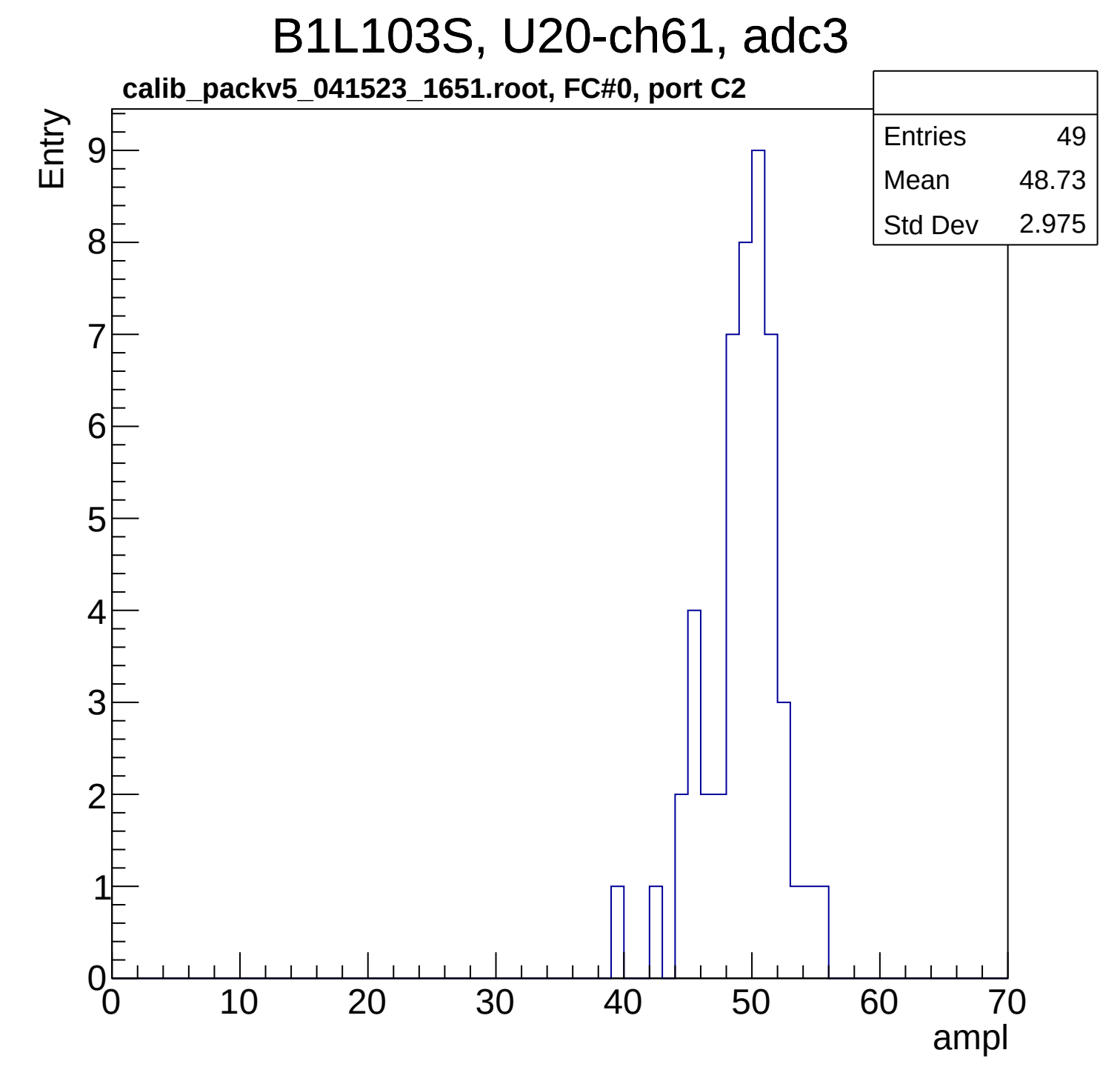
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch61, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 48.73
Std Dev 2.975
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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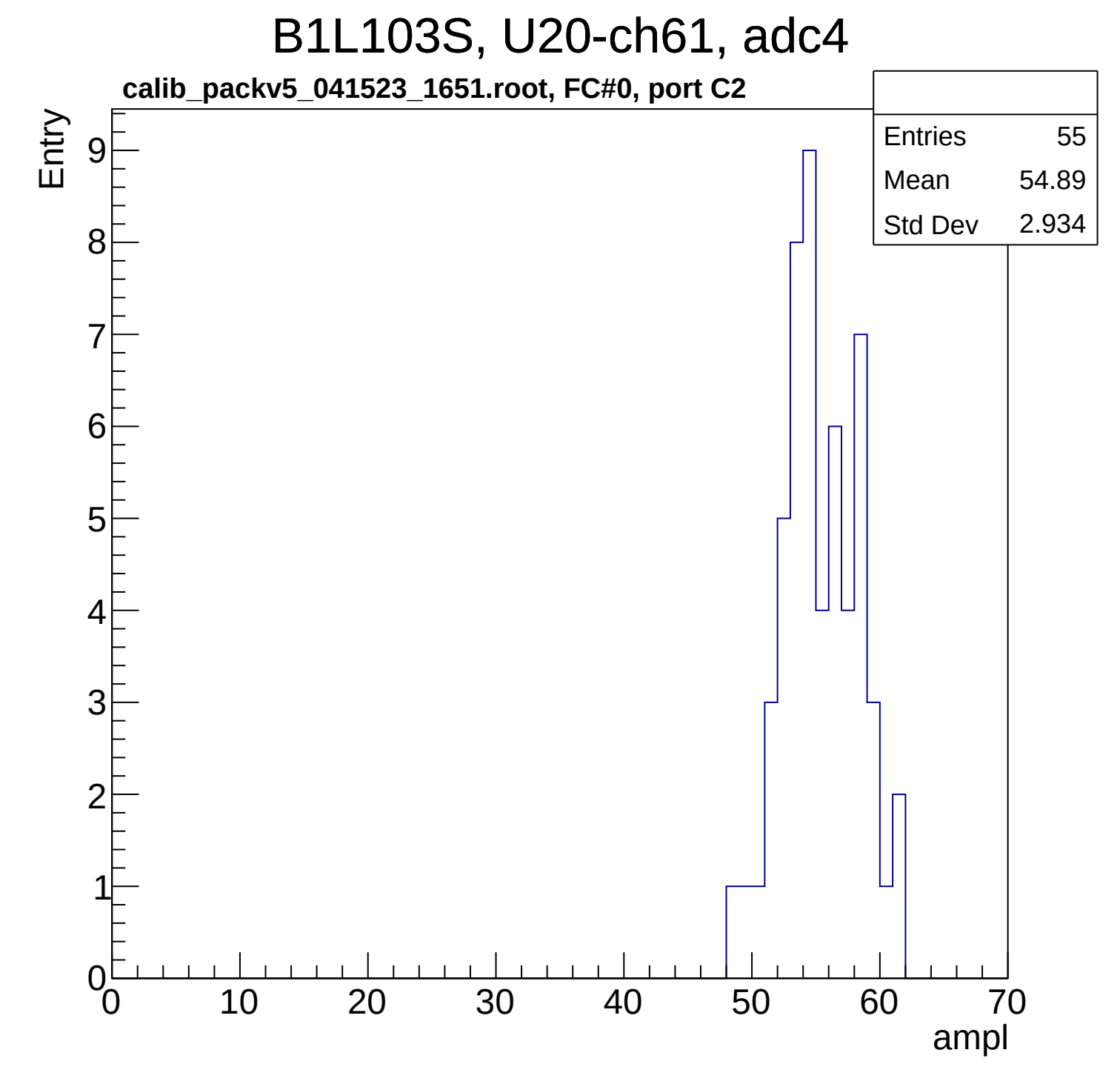
40
50
60
70


B1L103S, U20-ch61, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 54.89
Std Dev 2.934
Entry
ampl
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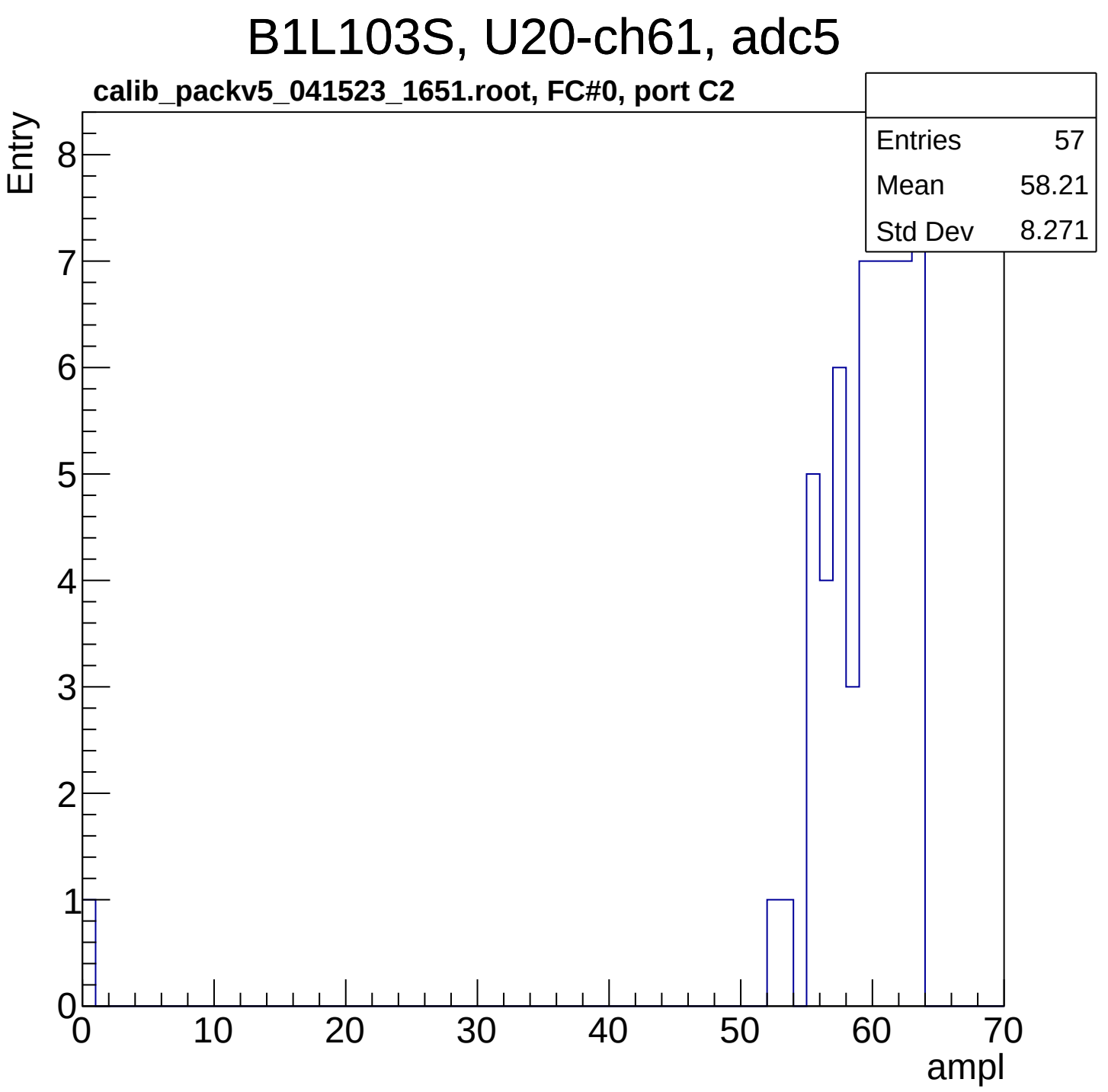
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch61, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 58.21
Std Dev 8.271
Entry
ampl
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1
2
3
4
5
6
7
8
0
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60
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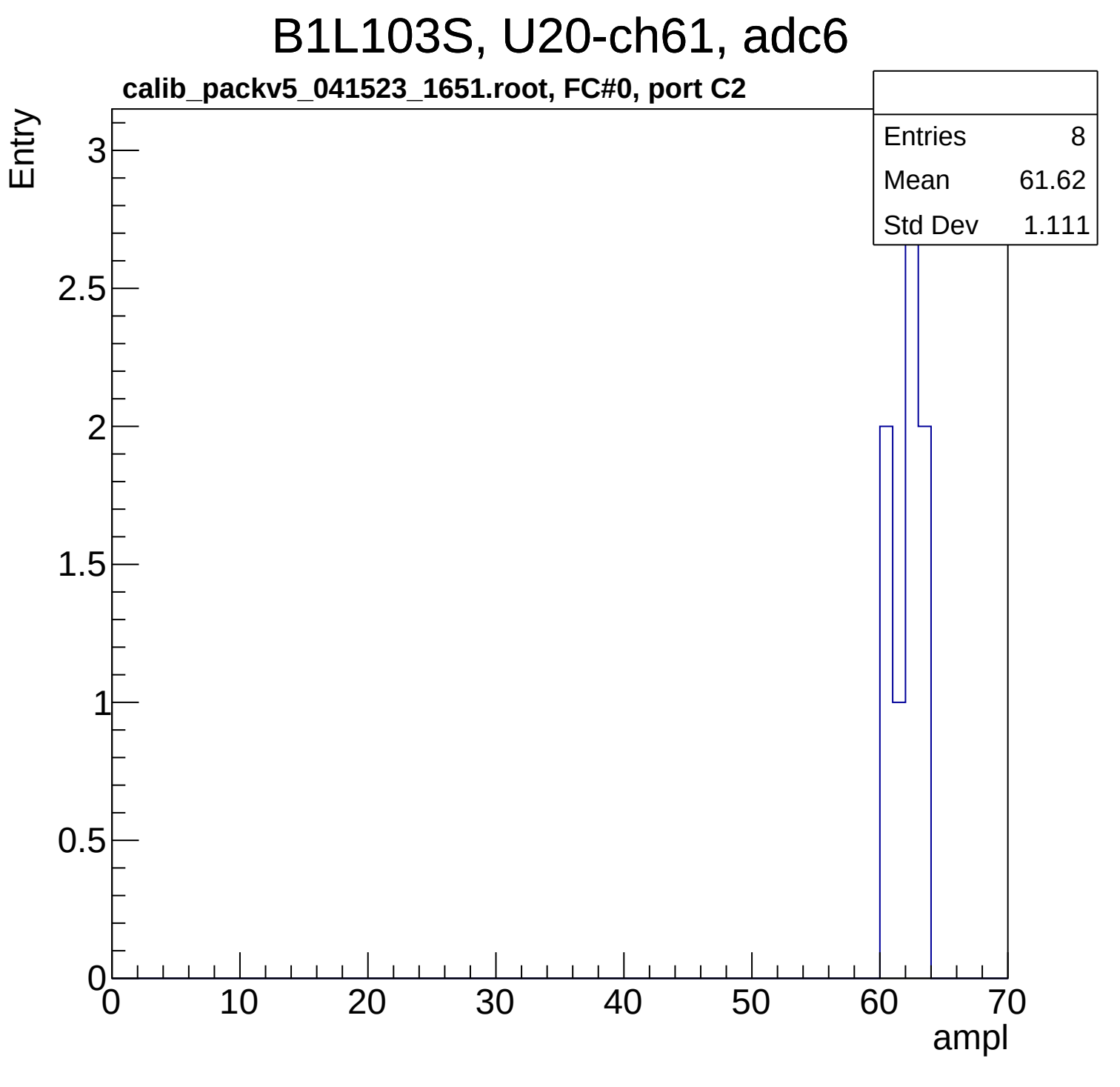
B1L103S, U20-ch61, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 61.62
Std Dev 1.111
Entry
ampl
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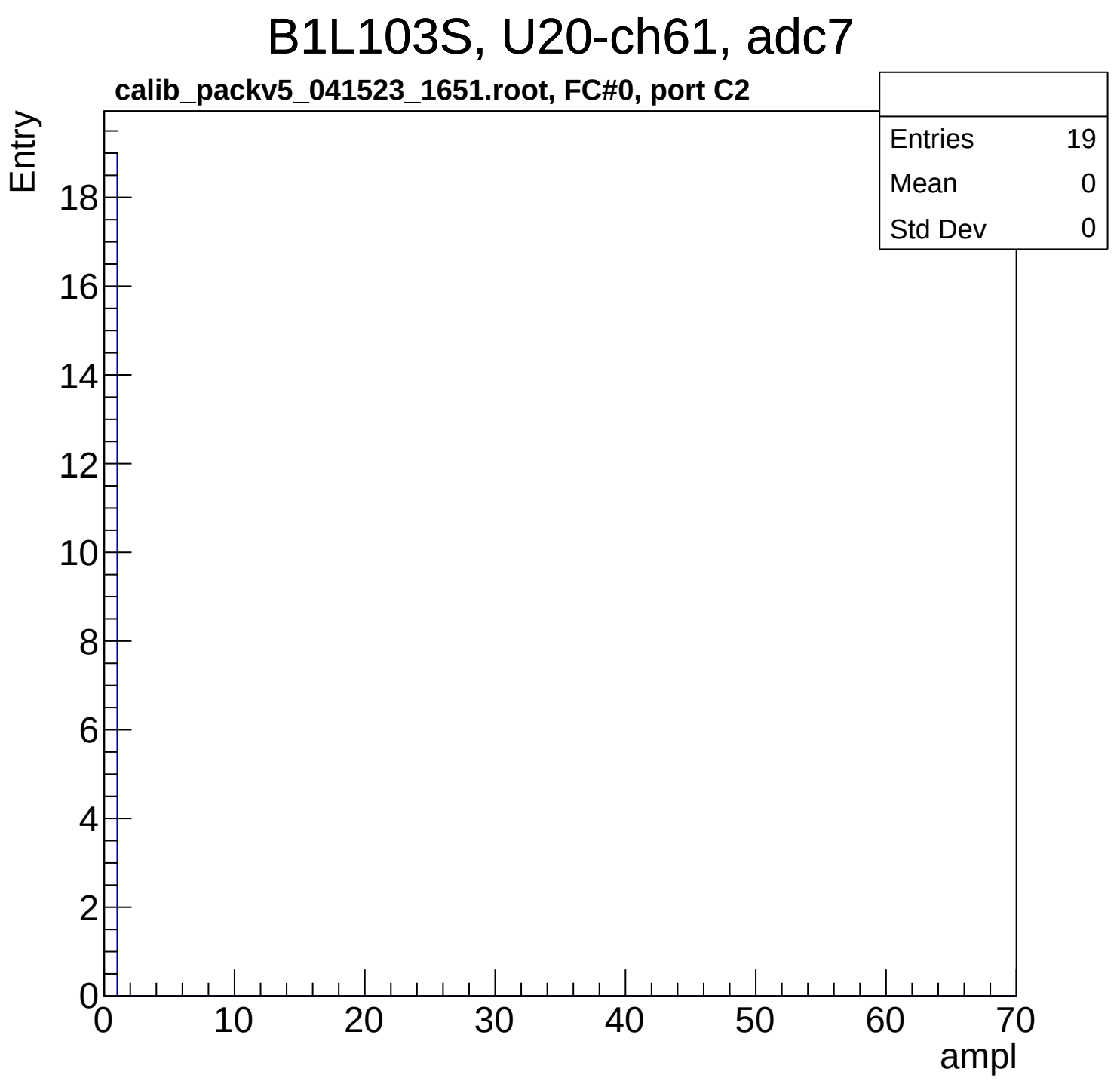
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U20-ch61, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
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6
8
10
12
14
16
18
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10
20
30
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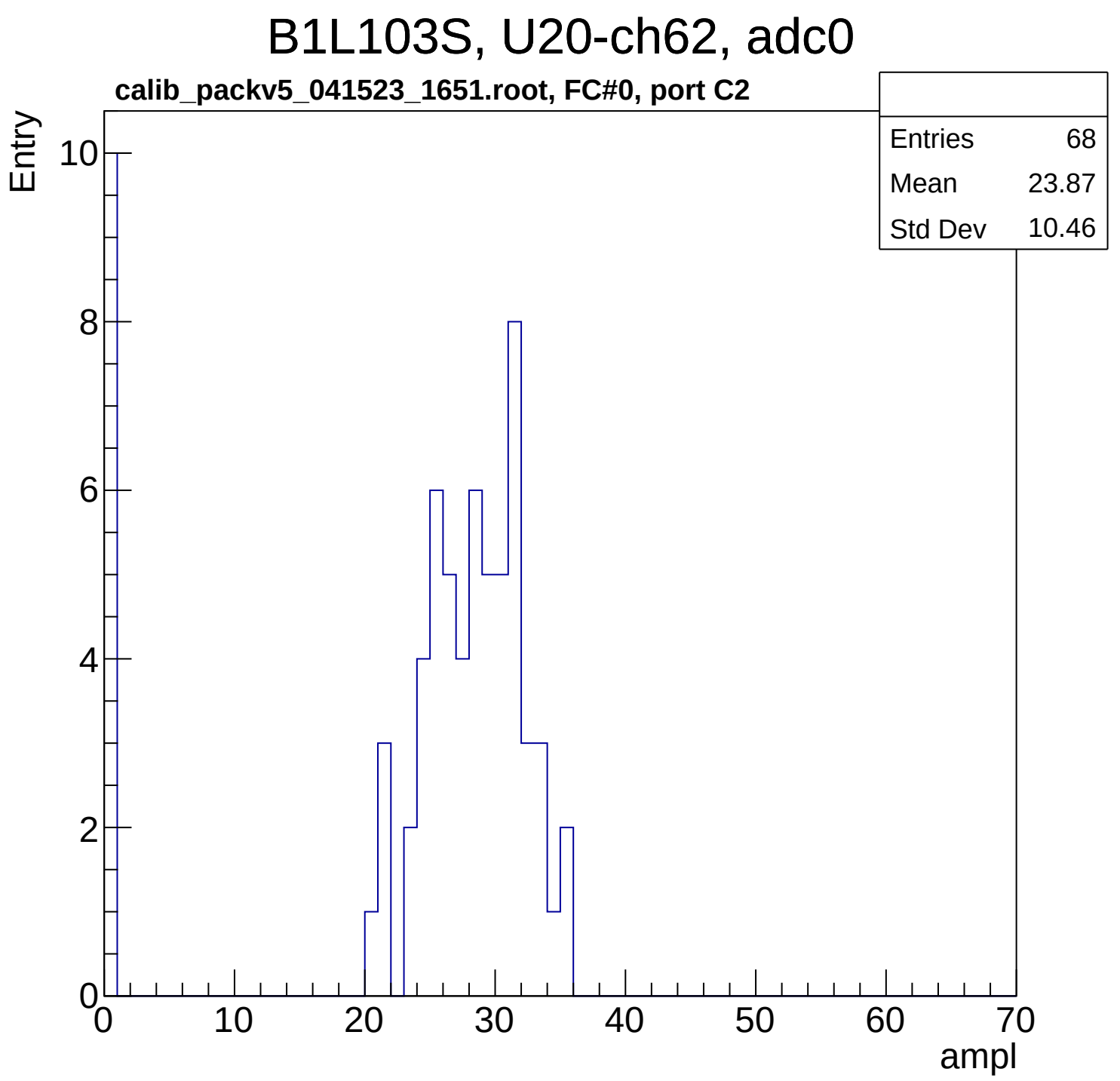
50
60
70
ampl


B1L103S, U20-ch62, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 23.87
Std Dev 10.46
Entry
0
2
4
6
8
10
0
10
20
30
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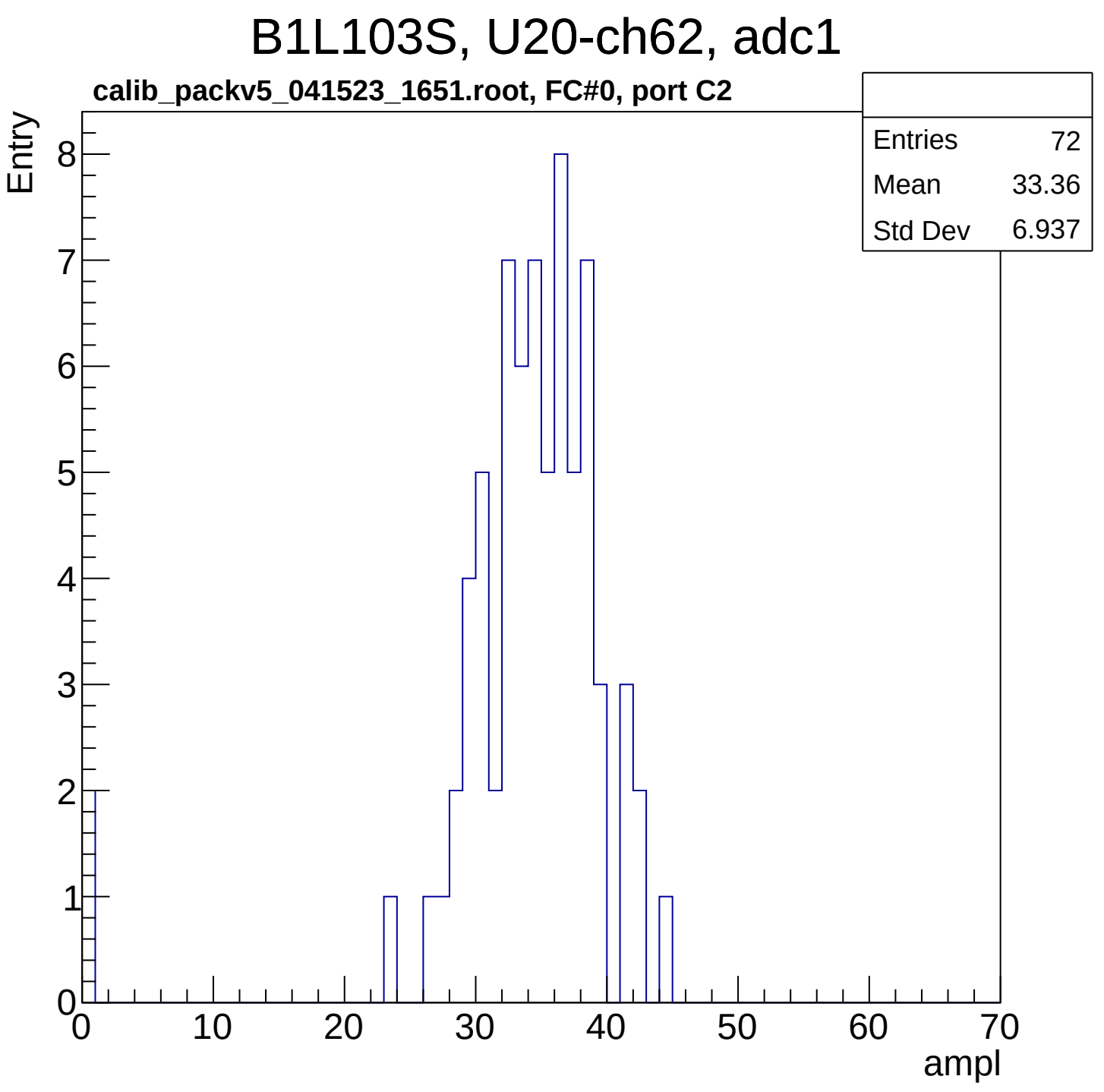
50
60
70
ampl


B1L103S, U20-ch62, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 33.36
Std Dev 6.937
Entry
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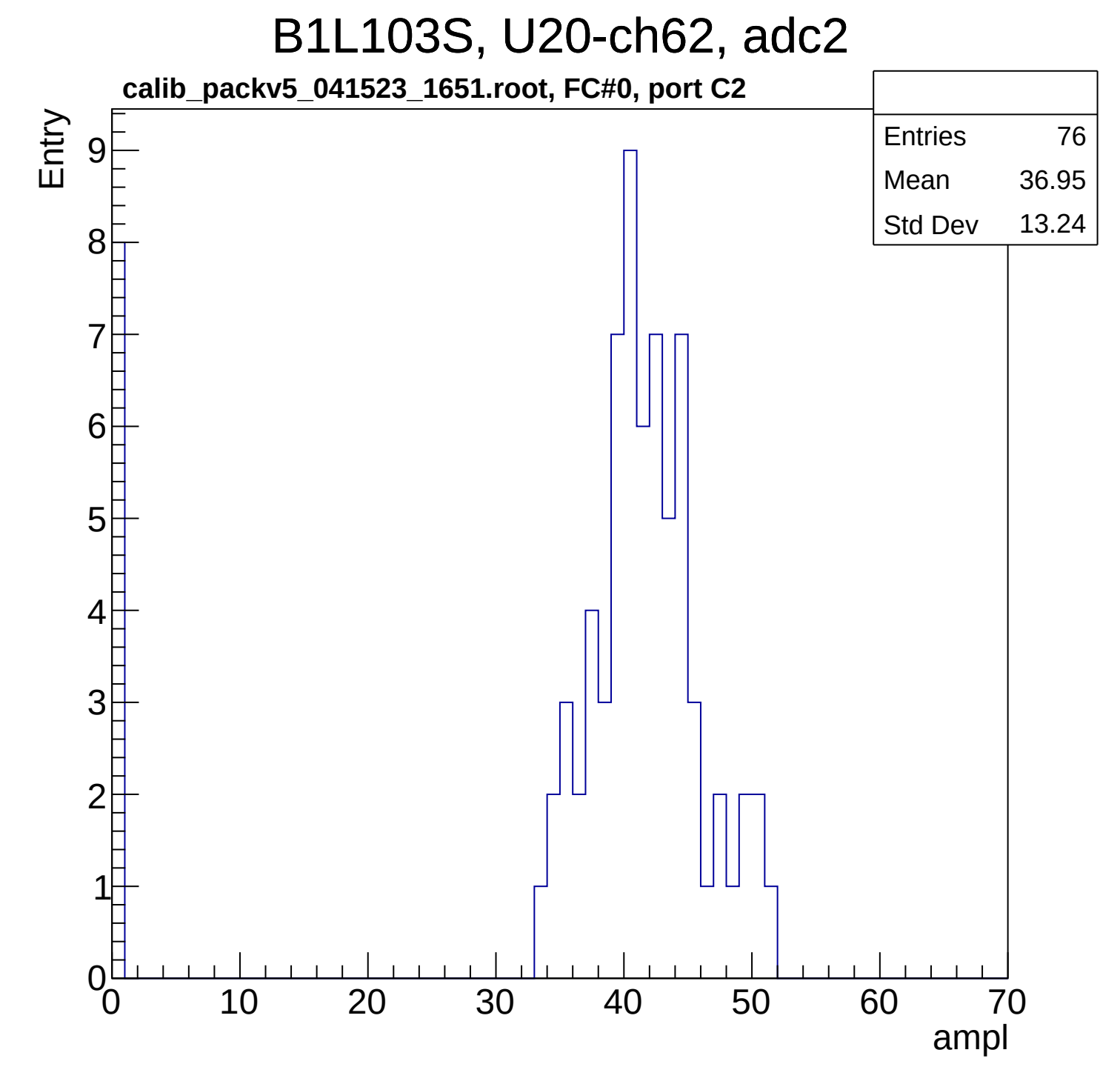
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch62, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 36.95
Std Dev 13.24
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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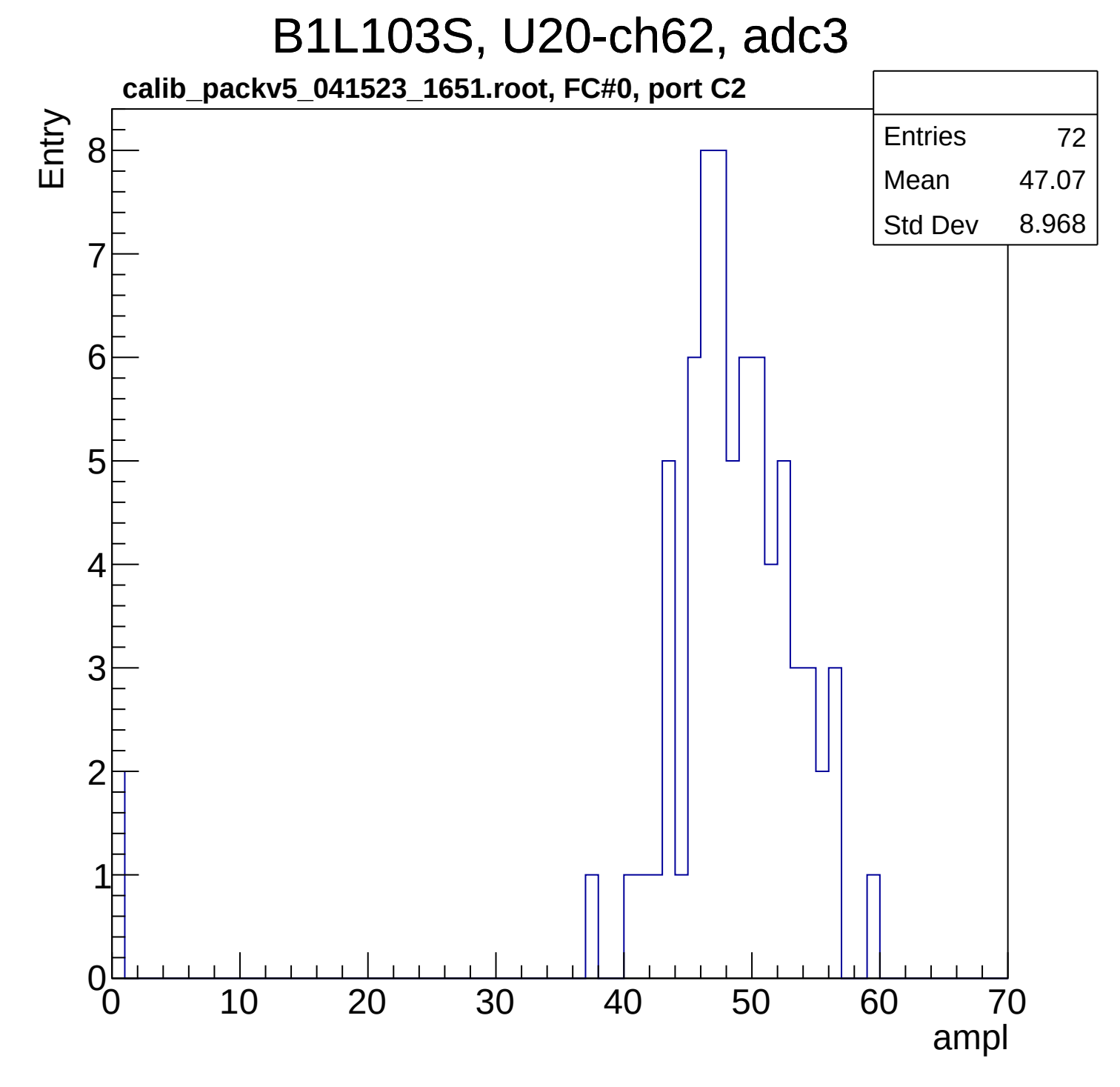
40
50
60
70


B1L103S, U20-ch62, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 47.07
Std Dev 8.968
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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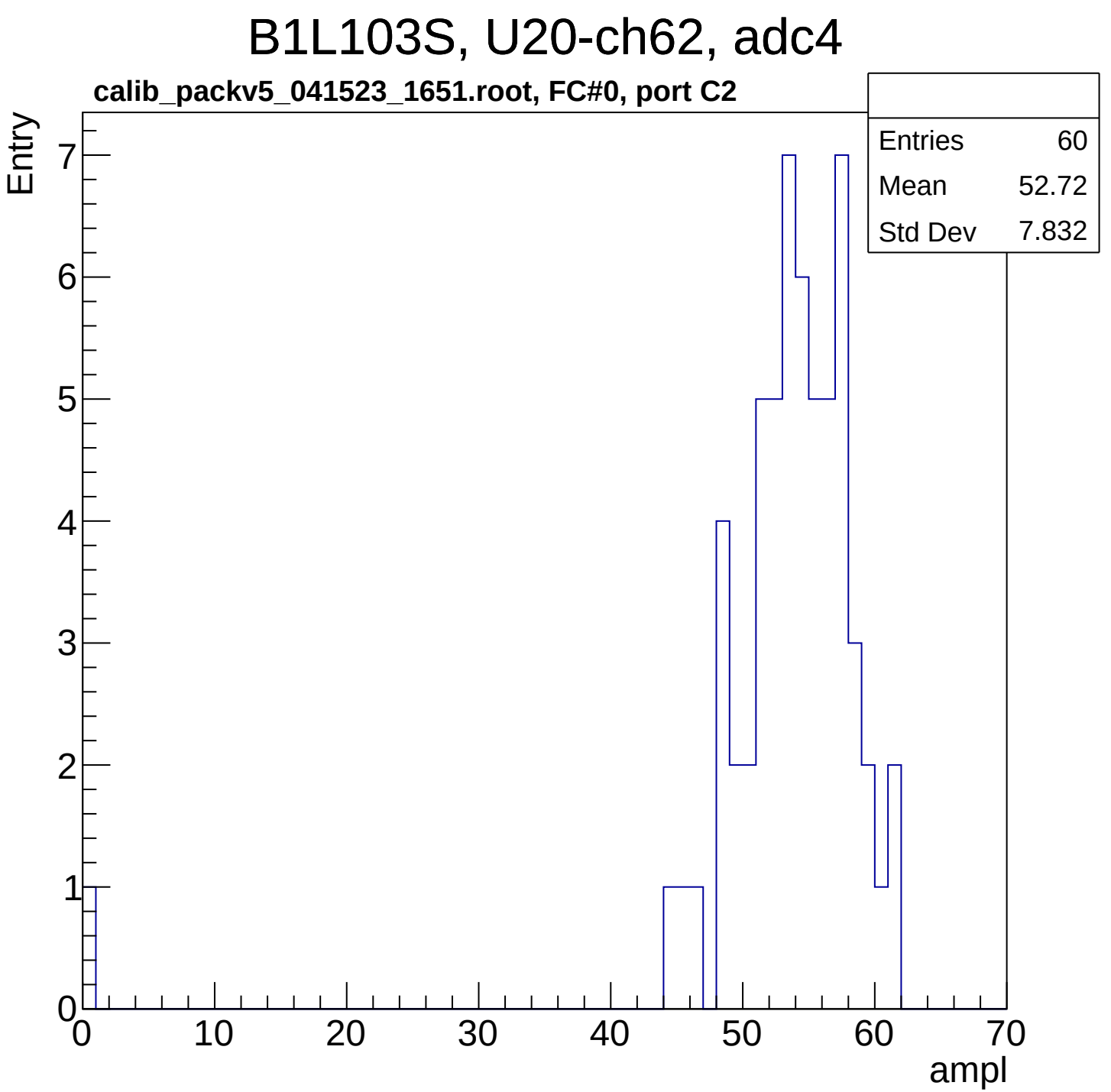
40
50
60
70


B1L103S, U20-ch62, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 52.72
Std Dev 7.832
Entry
ampl
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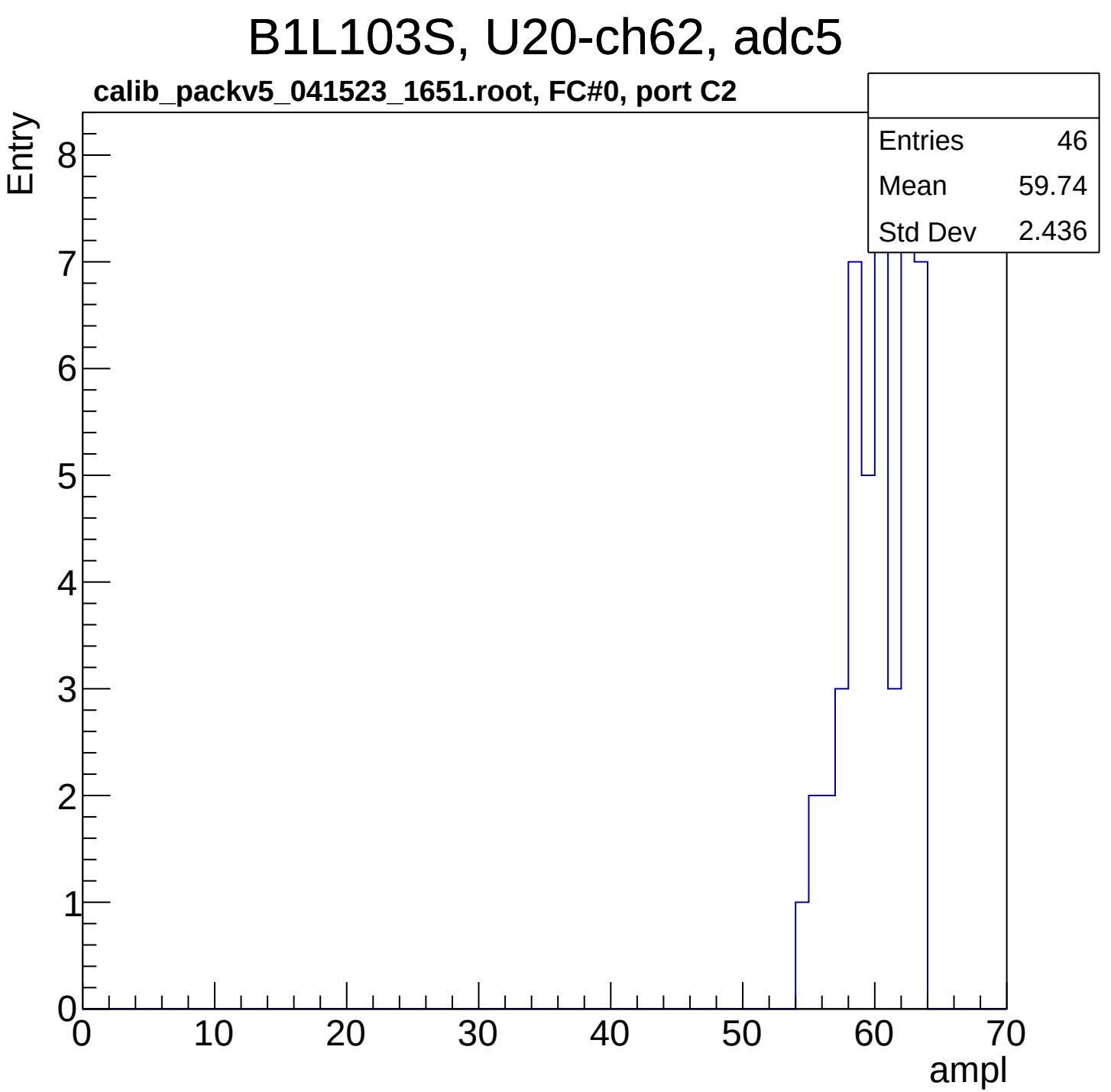
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U20-ch62, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 59.74
Std Dev 2.436
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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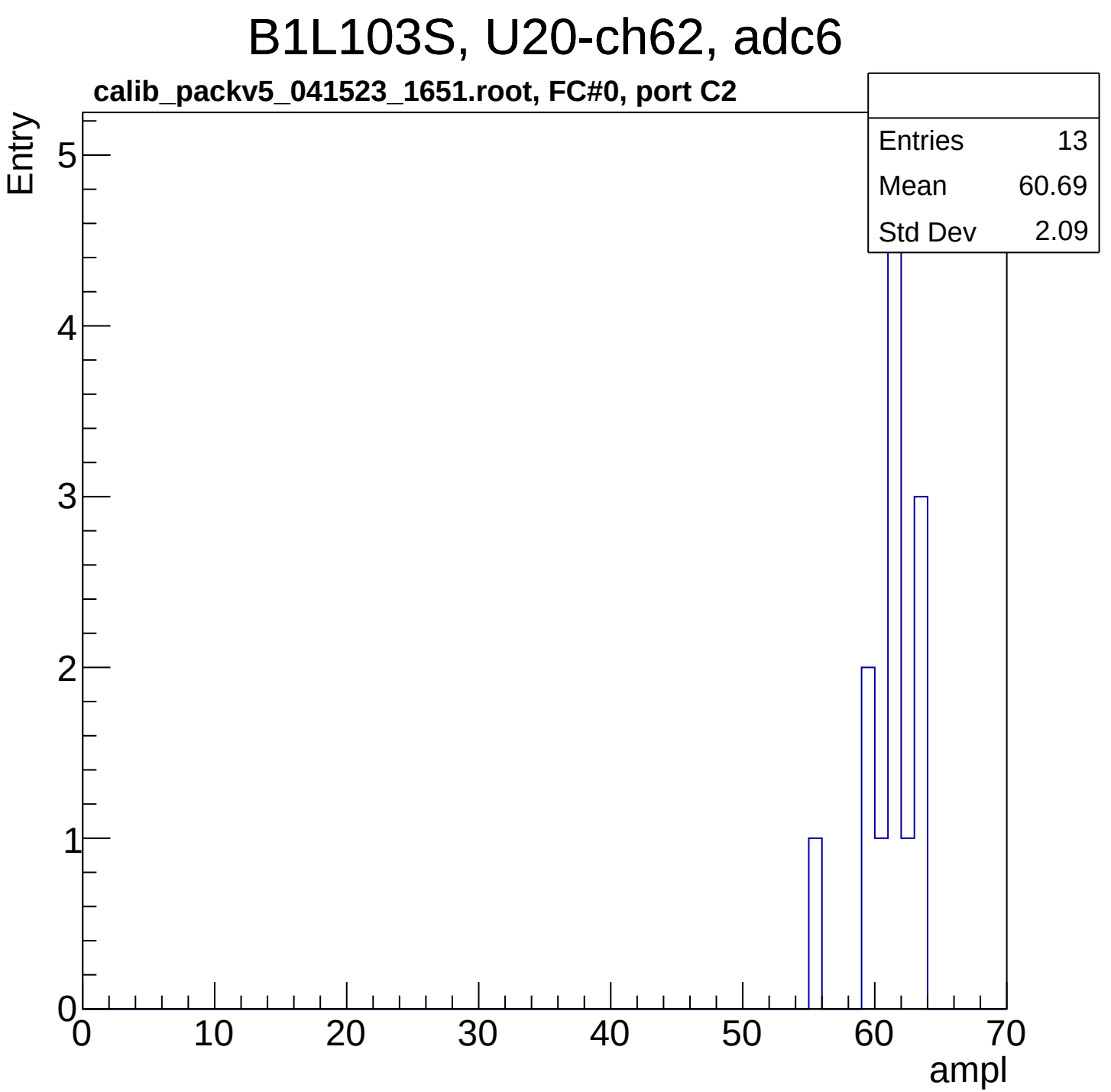
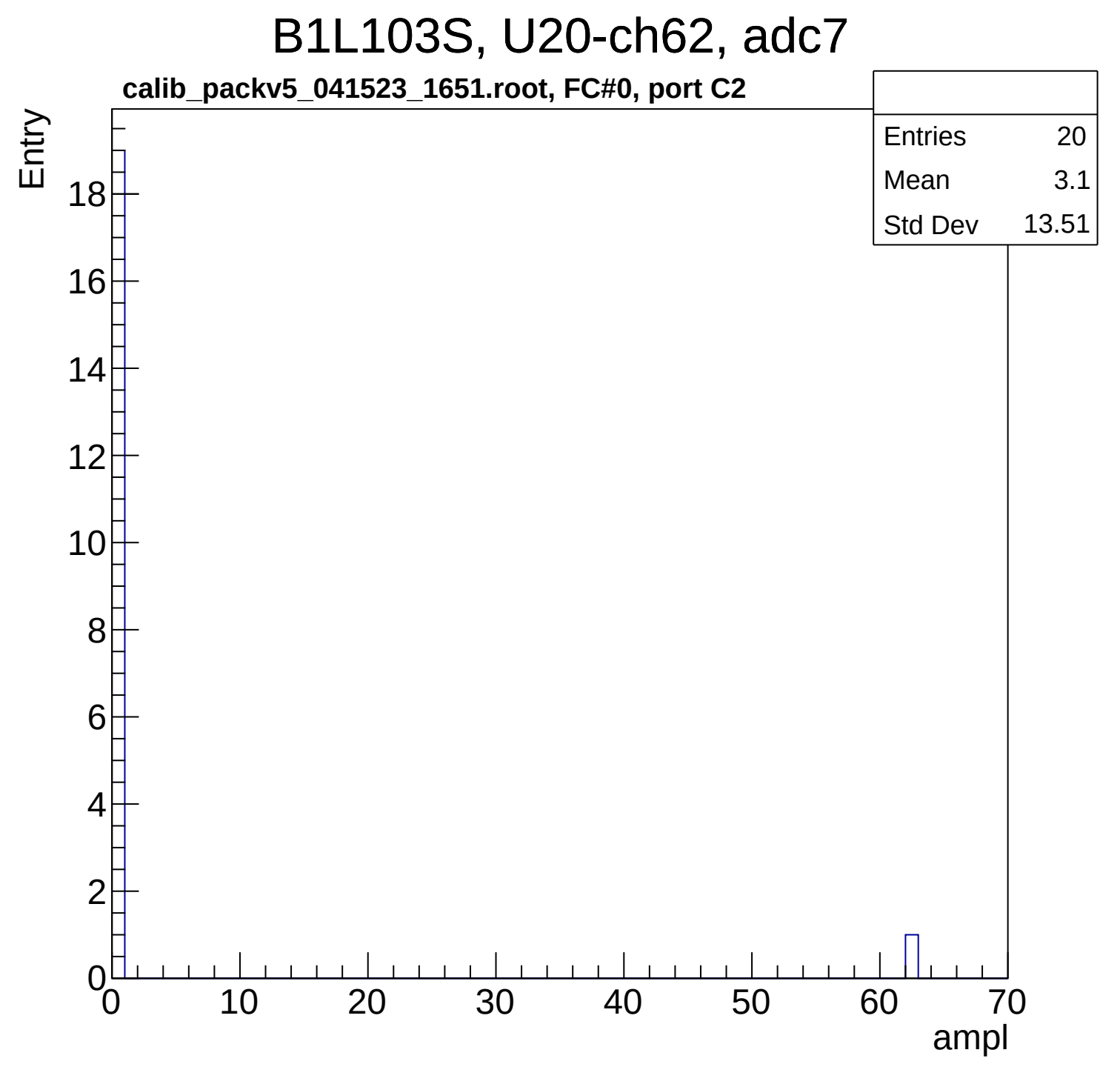
40
50
60
70


B1L103S, U20-ch62, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 60.69
Std Dev 2.09
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U20-ch62, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
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4
6
8
10
12
14
16
18
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10
20
30
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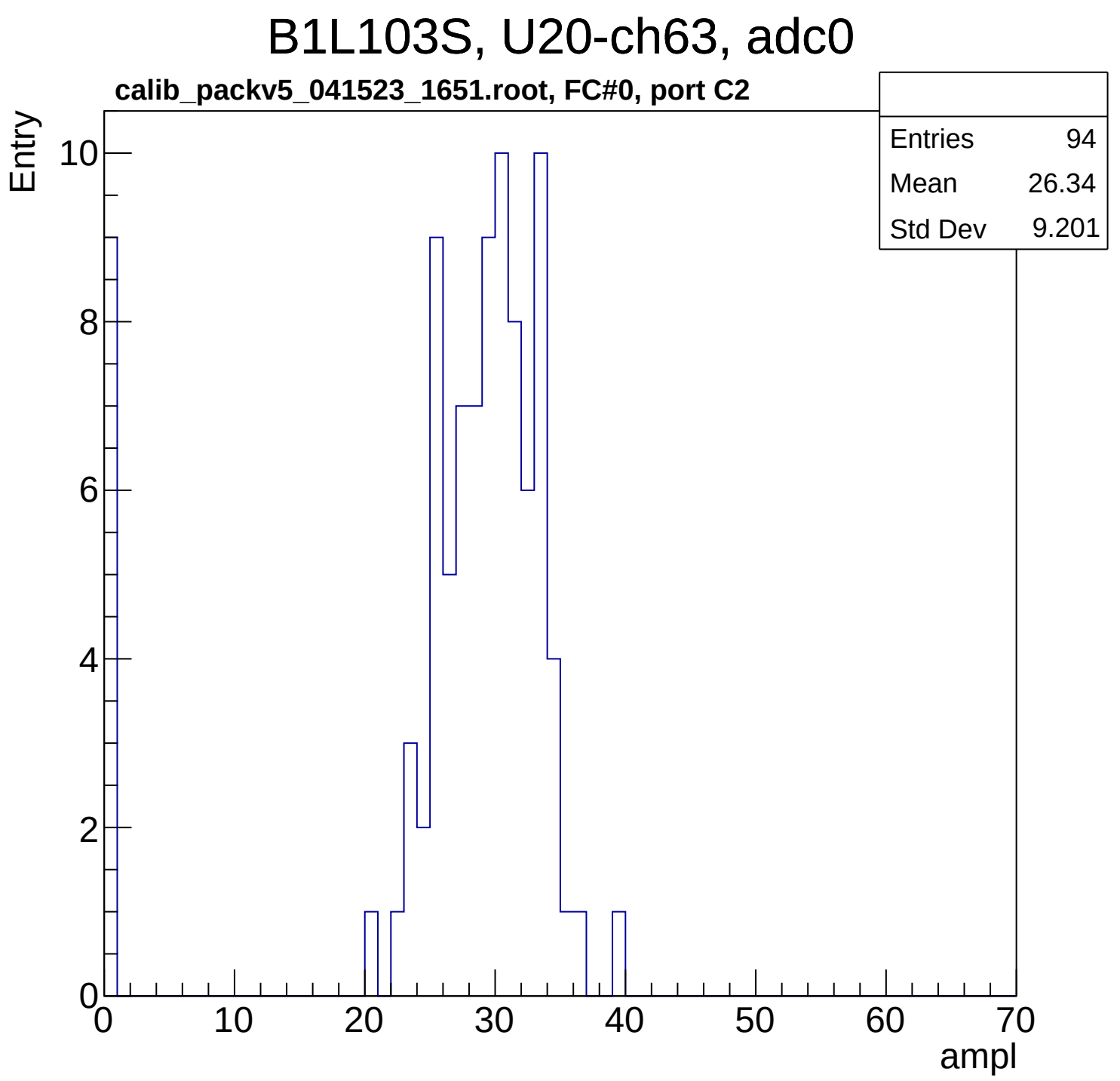
50
60
70
ampl


B1L103S, U20-ch63, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 26.34
Std Dev 9.201
Entry
0
2
4
6
8
10
0
10
20
30
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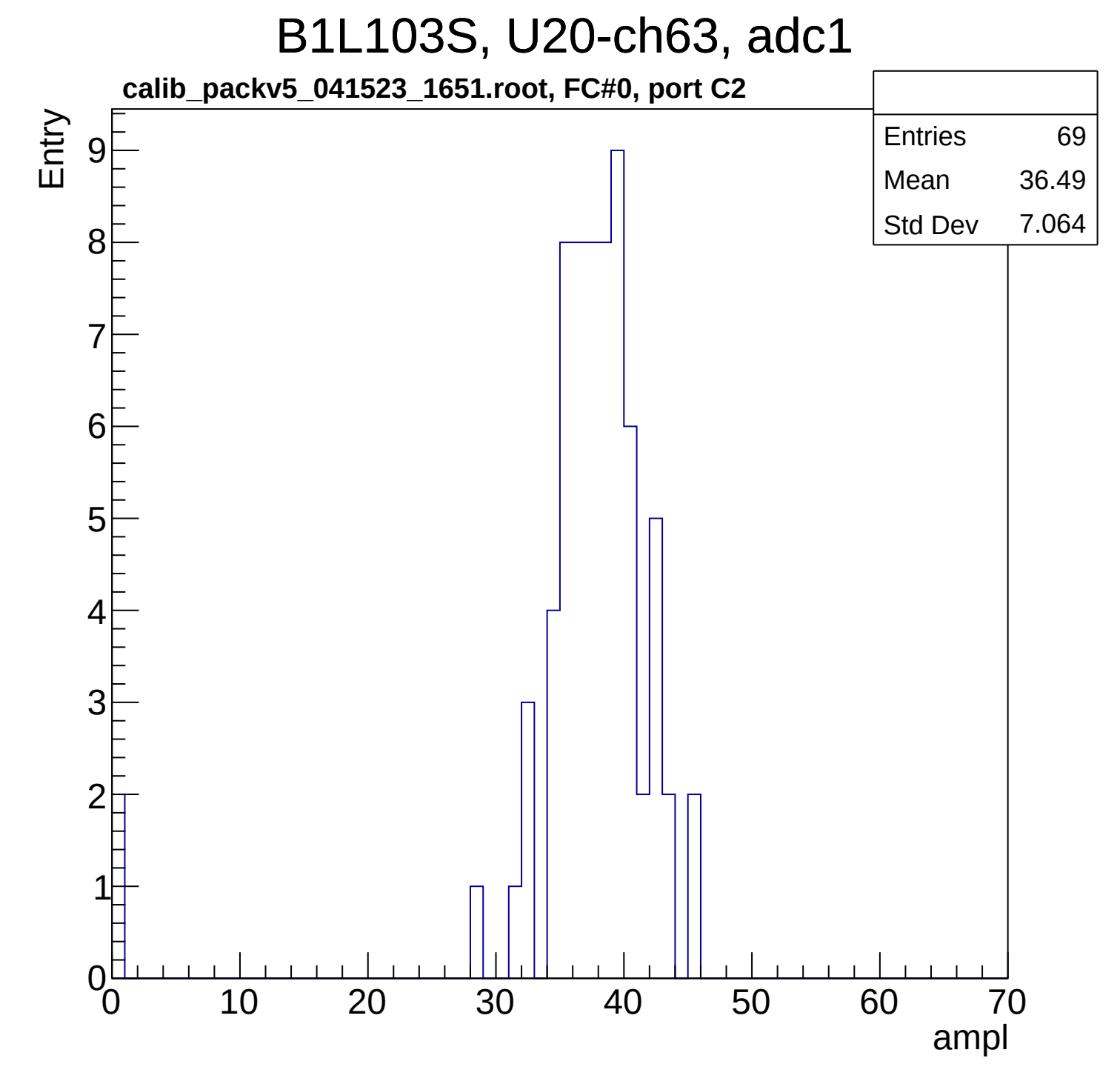
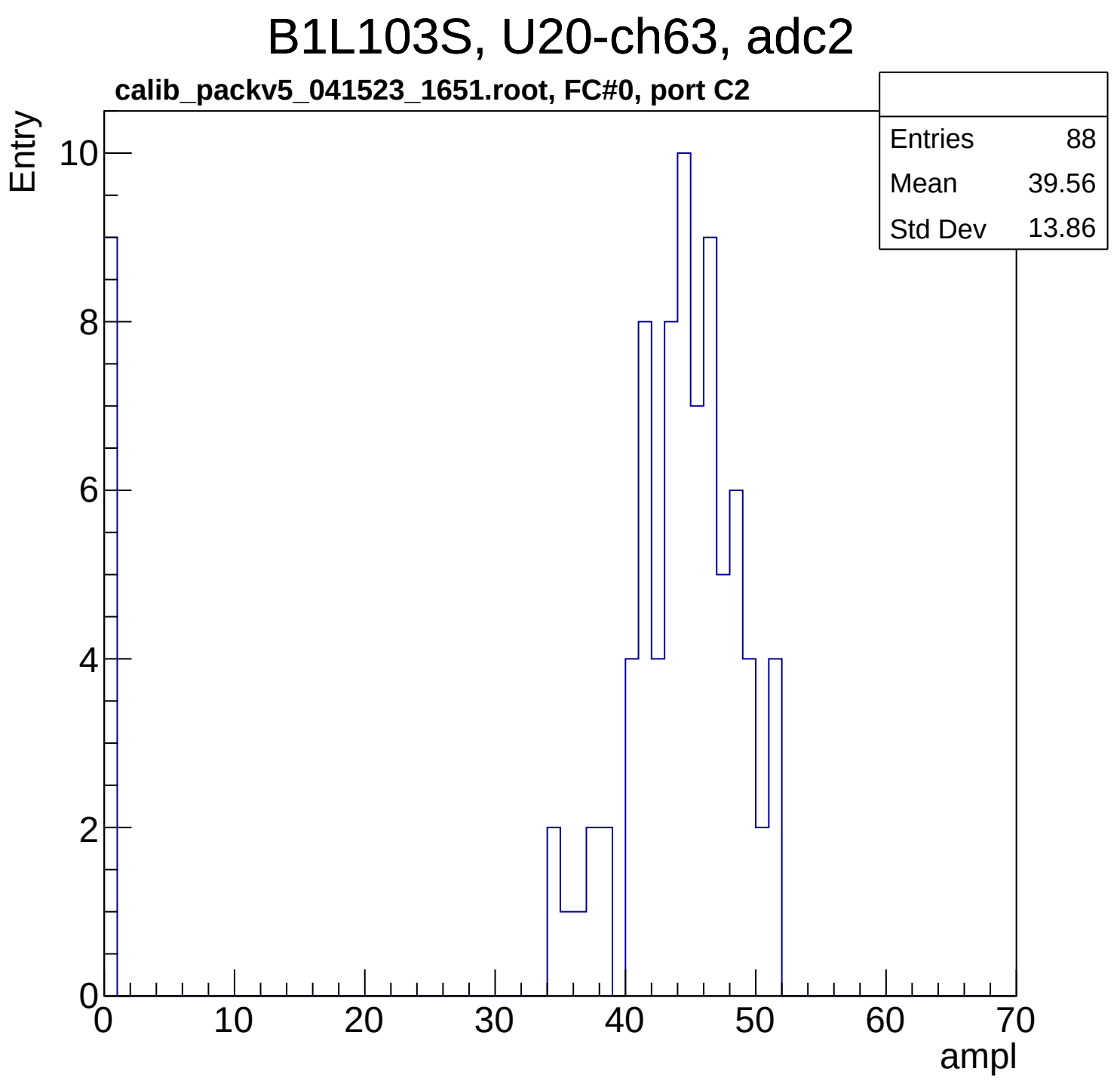
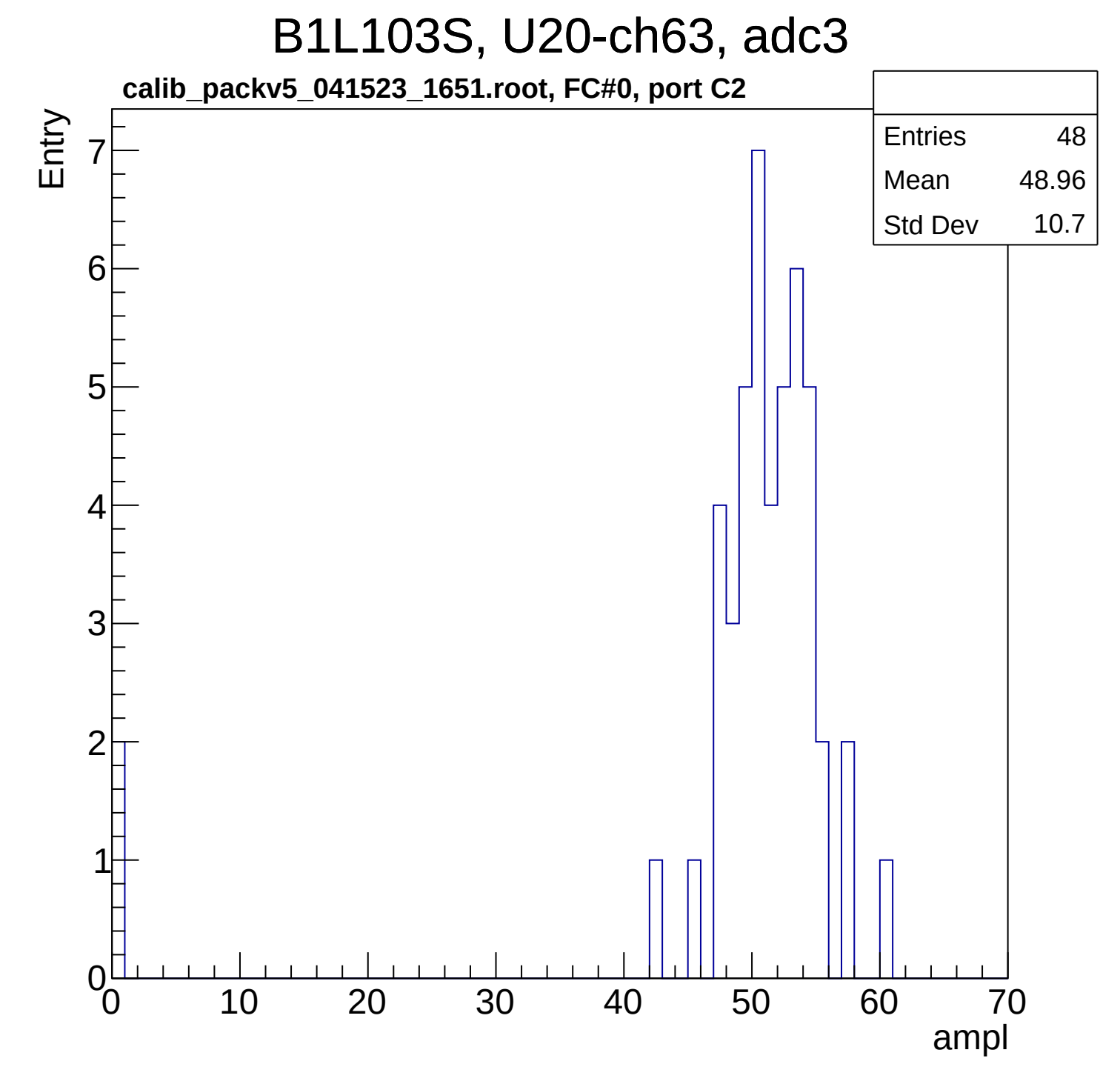
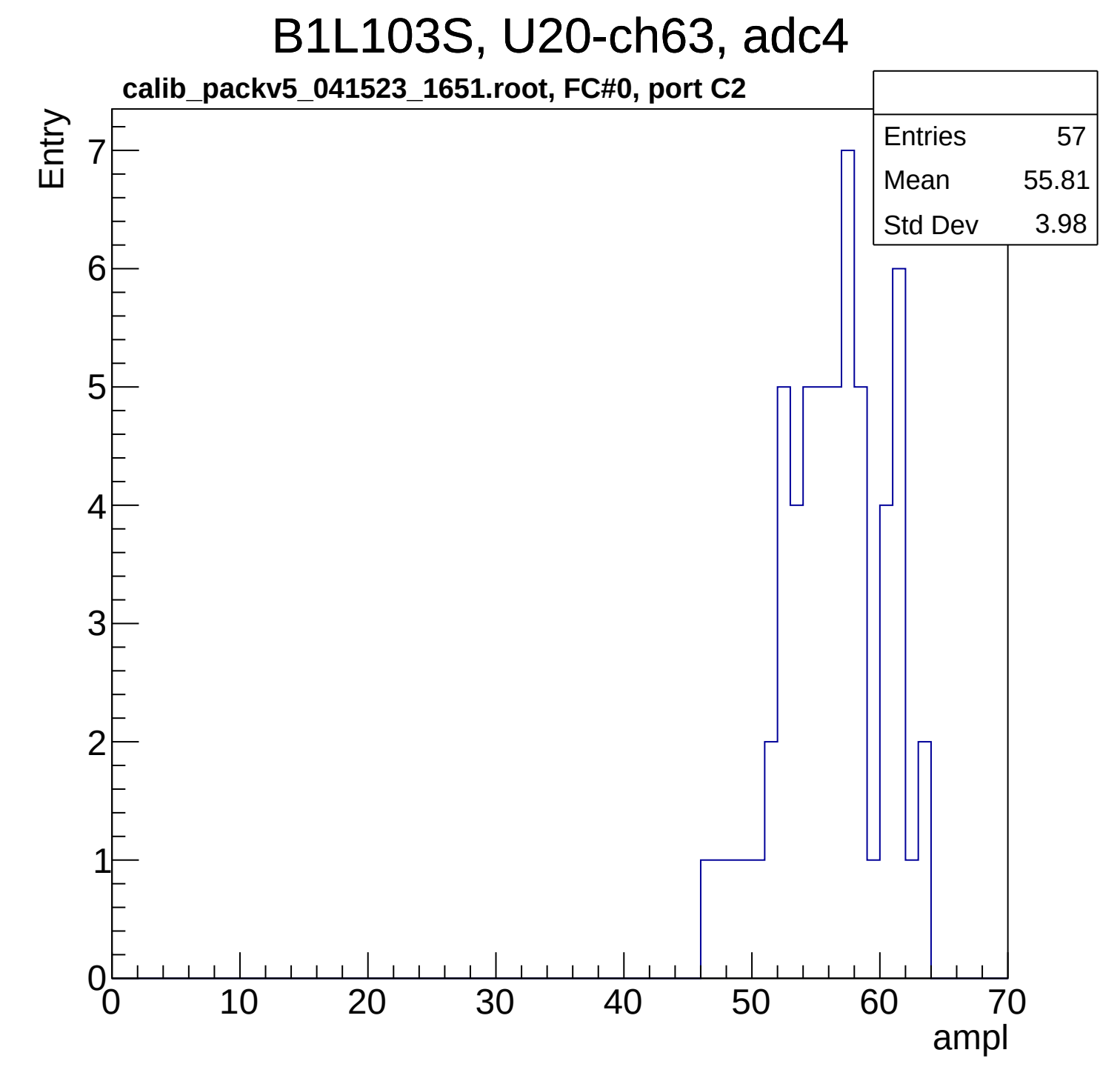
50
60
70
ampl


B1L103S, U20-ch63, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 36.49
Std Dev 7.064
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch63, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 39.56
Std Dev 13.86
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch63, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 48.96
Std Dev 10.7
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U20-ch63, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 55.81
Std Dev 3.98
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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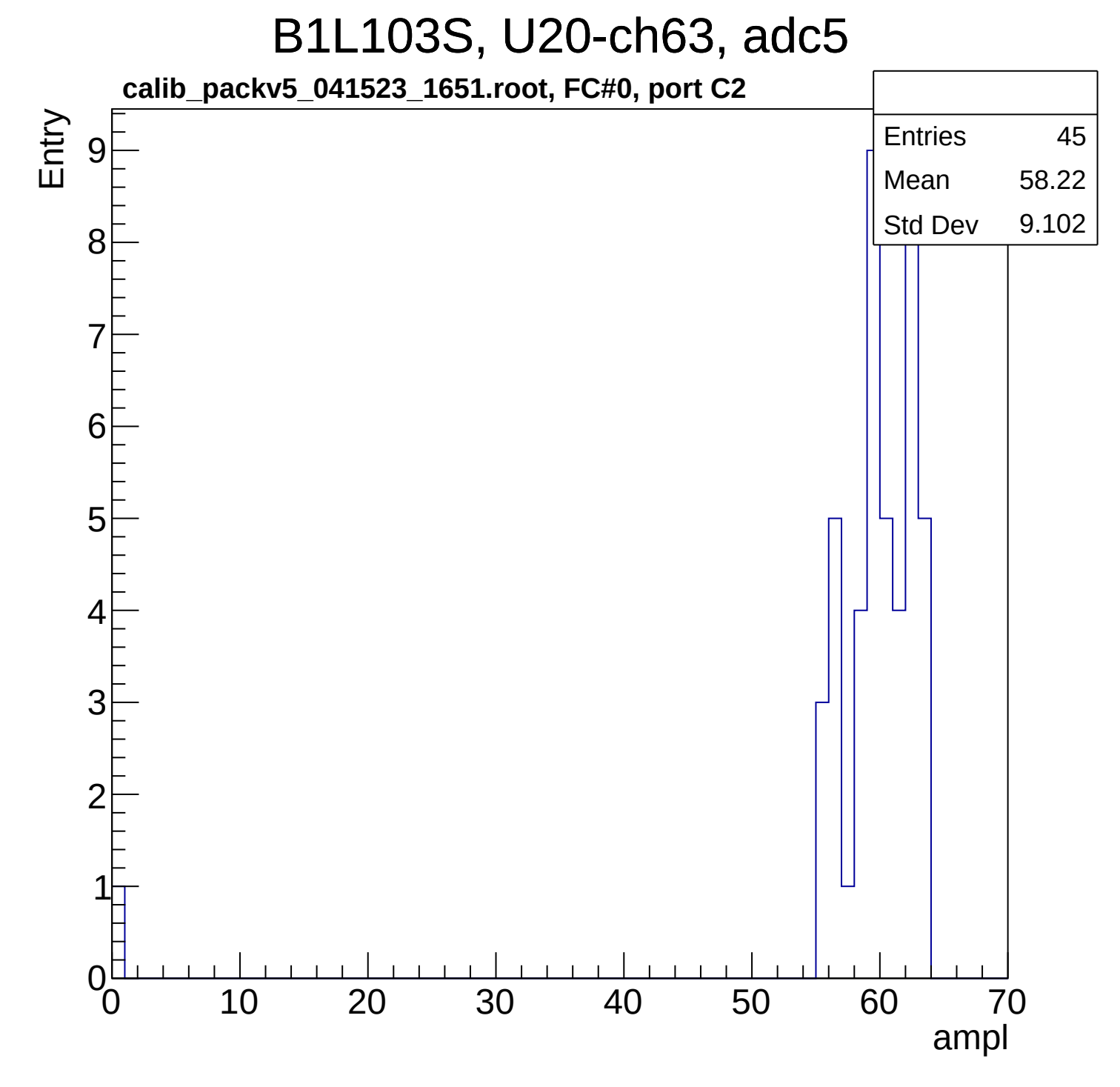
B1L103S, U20-ch63, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 58.22
Std Dev 9.102
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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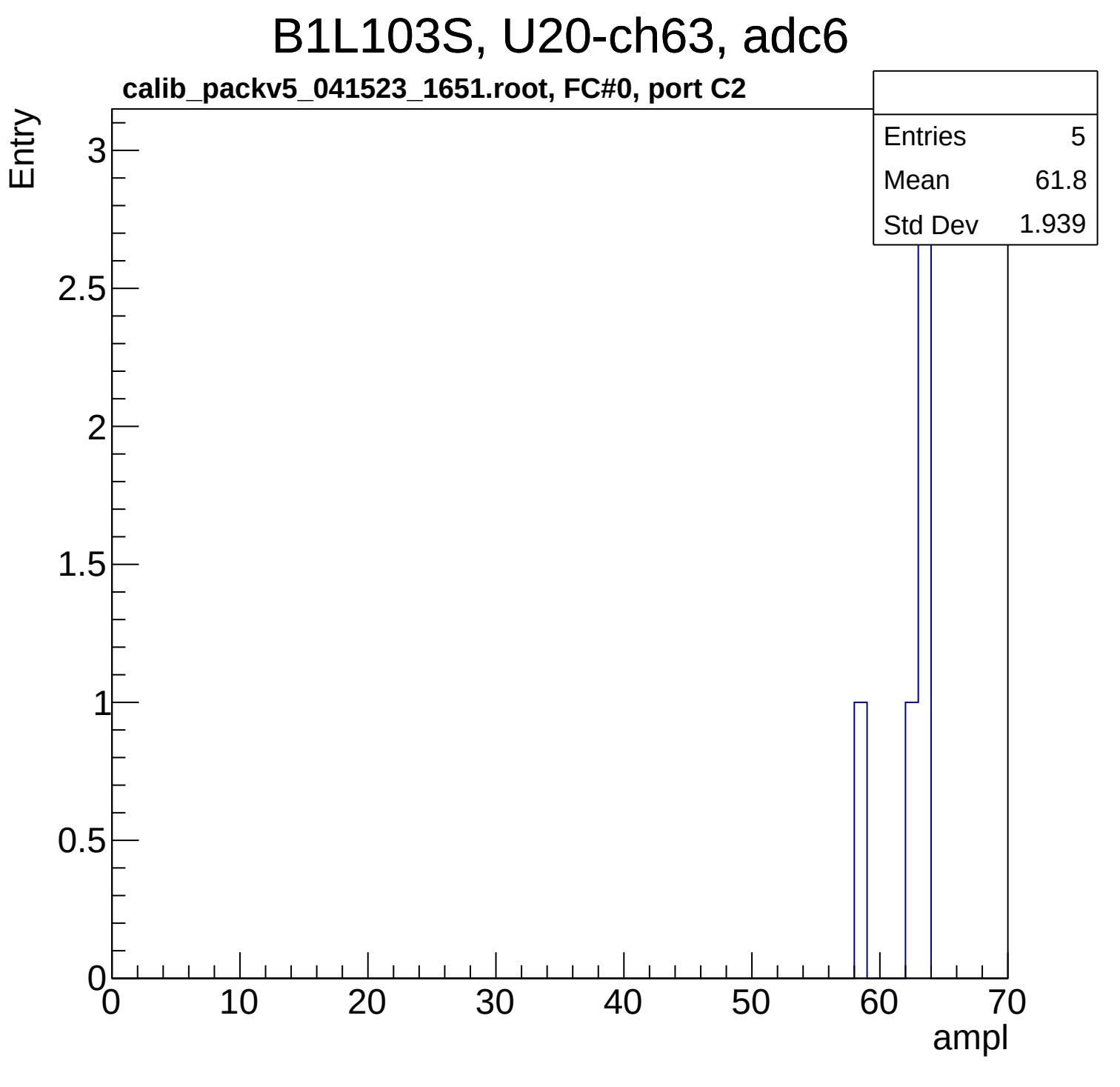
B1L103S, U20-ch63, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 61.8
Std Dev 1.939
Entry
ampl
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0.5
1
1.5
2
2.5
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0
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60
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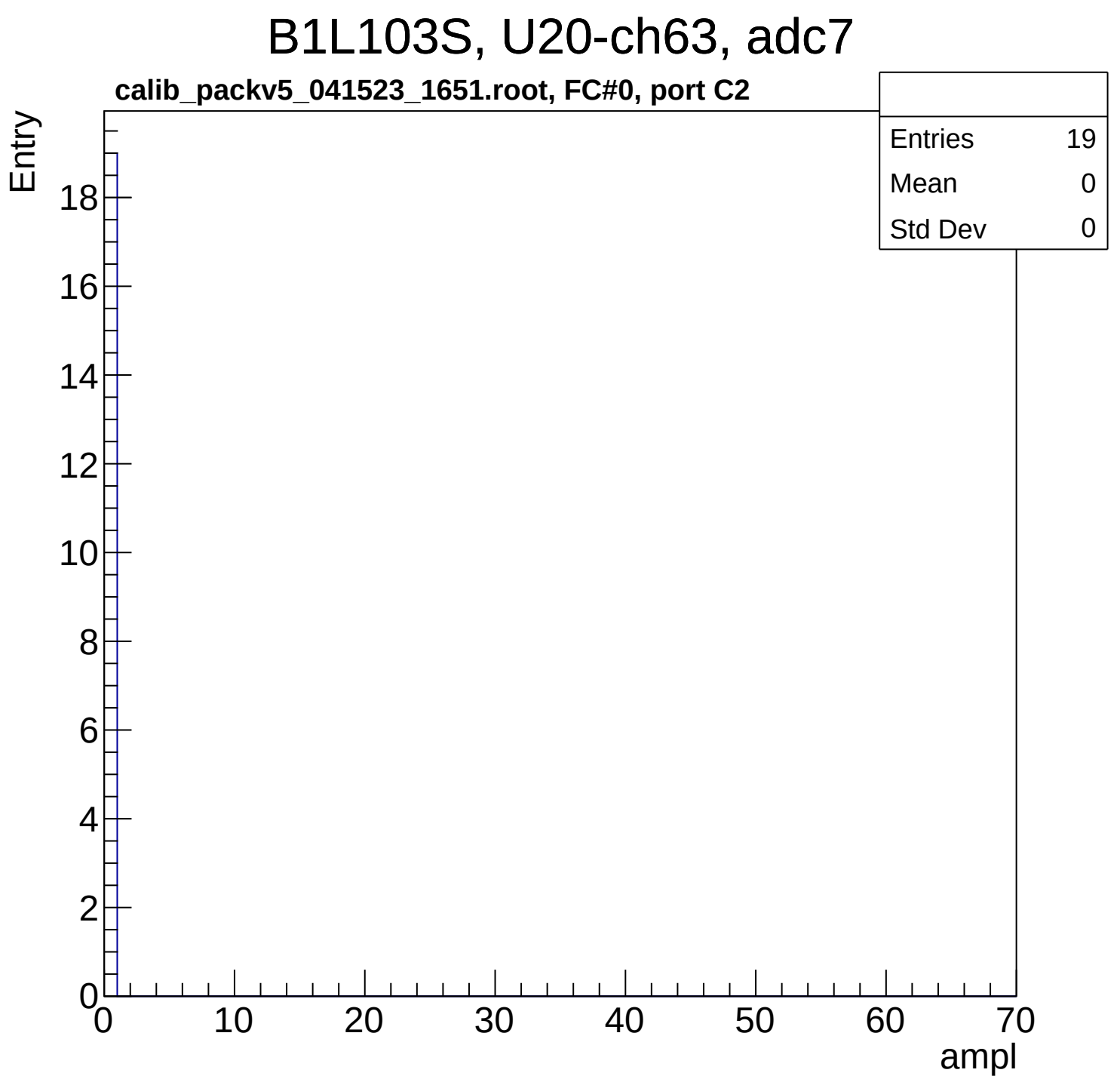
B1L103S, U20-ch63, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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6
8
10
12
14
16
18
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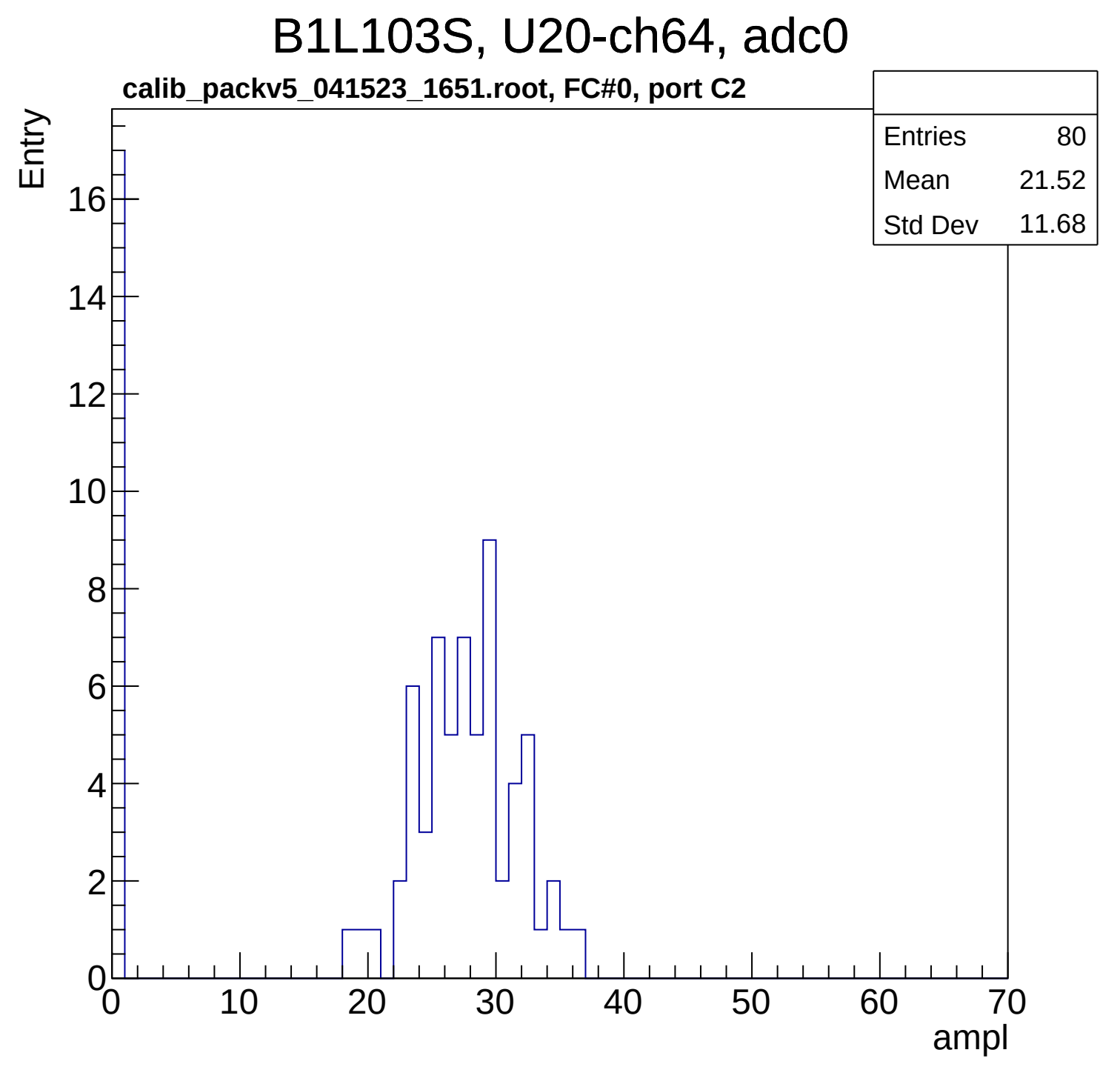
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch64, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 21.52
Std Dev 11.68
Entry
ampl
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4
6
8
10
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14
16
0
10
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40
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60
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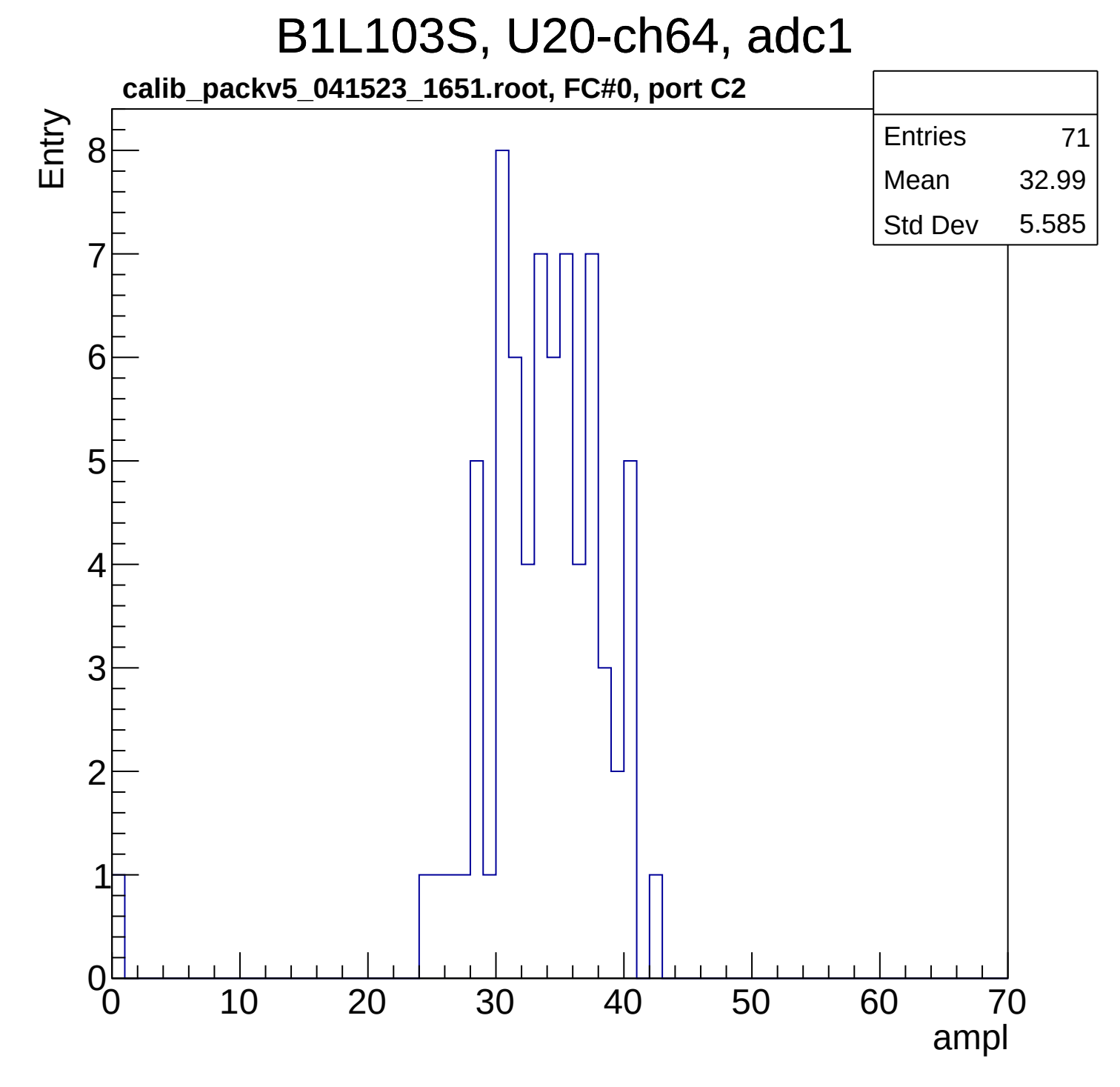
B1L103S, U20-ch64, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 32.99
Std Dev 5.585
Entry
ampl
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2
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5
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0
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60
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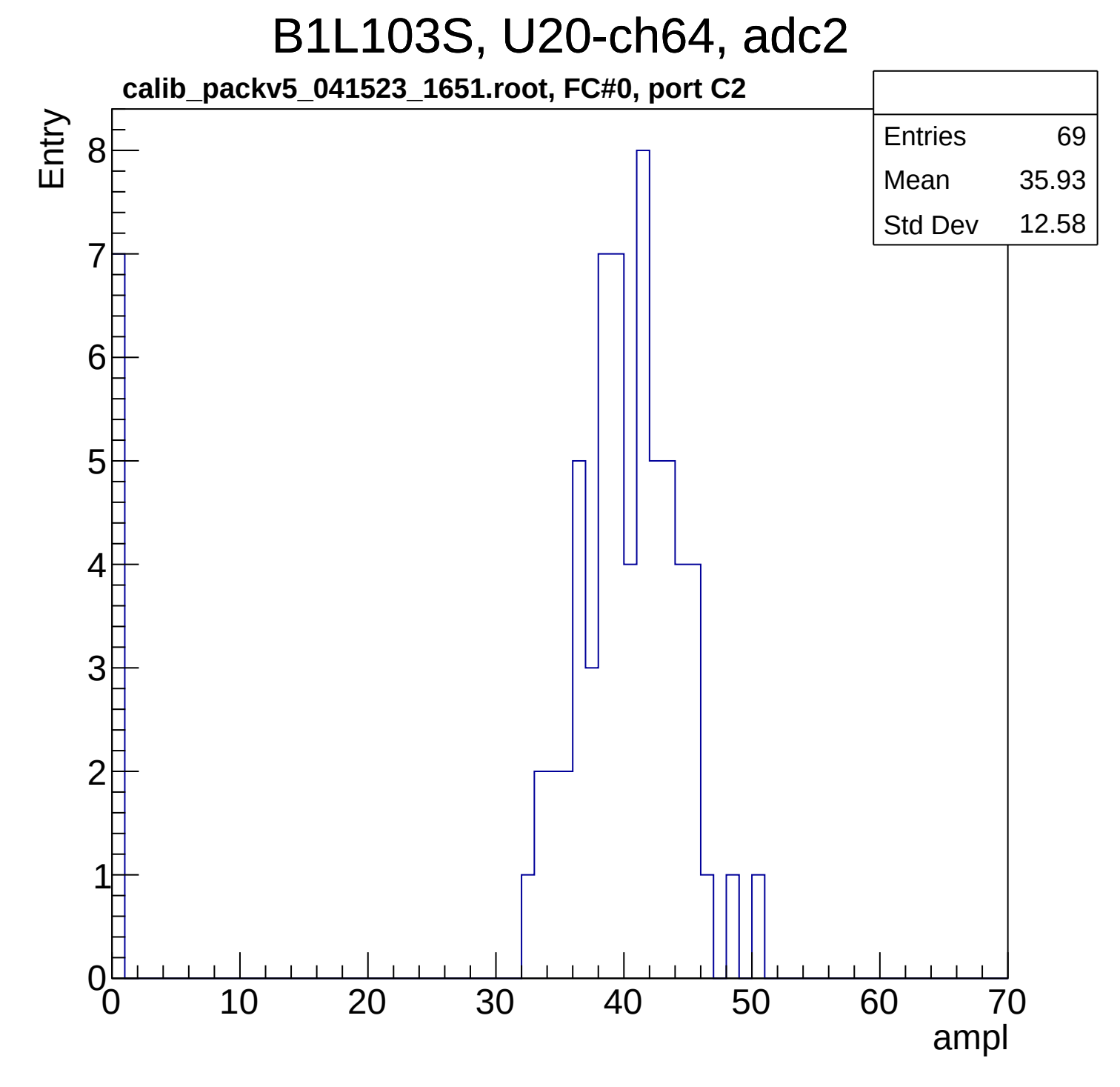
B1L103S, U20-ch64, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 35.93
Std Dev 12.58
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
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60
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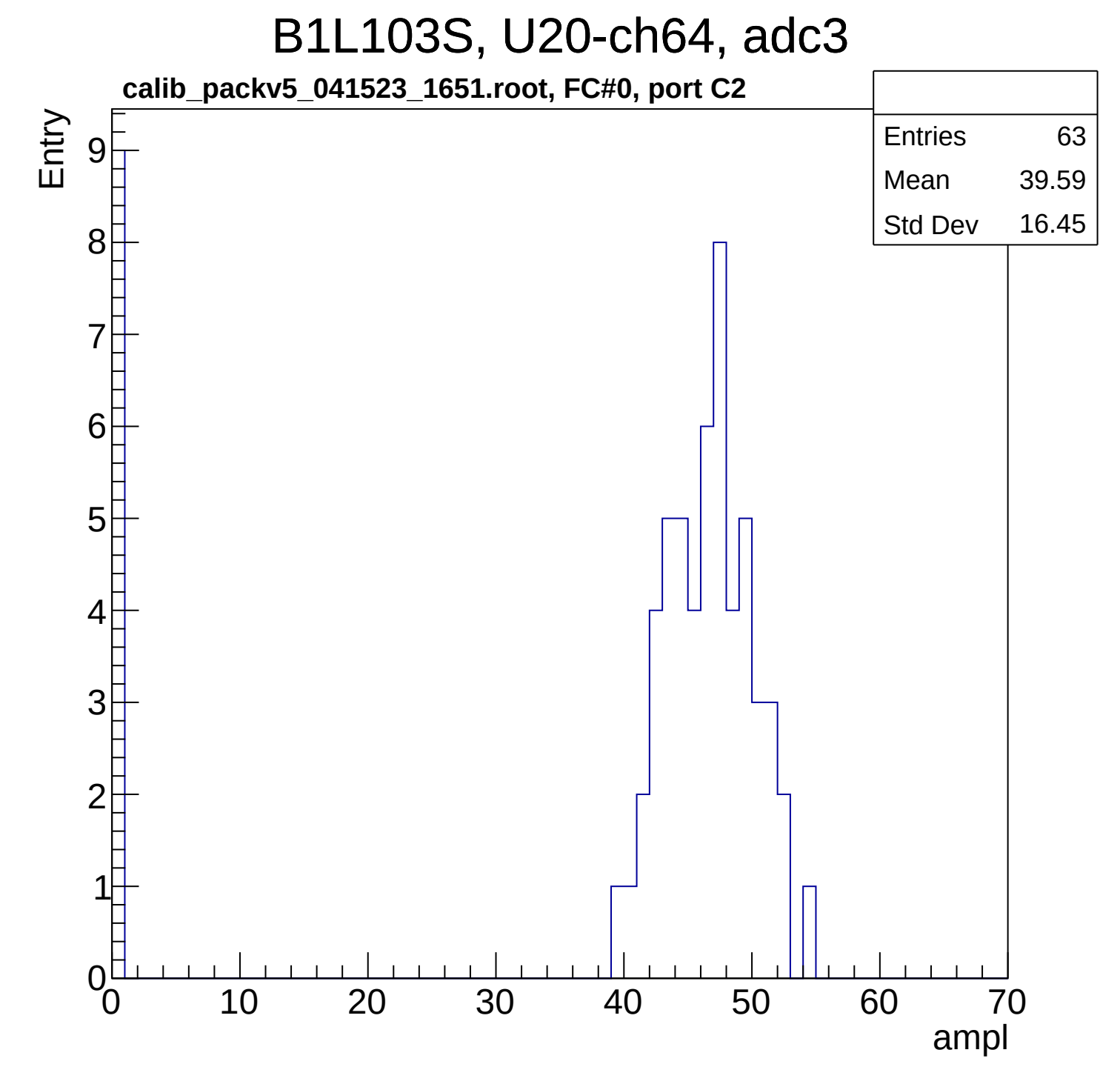
B1L103S, U20-ch64, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 39.59
Std Dev 16.45
Entry
ampl
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3
4
5
6
7
8
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0
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60
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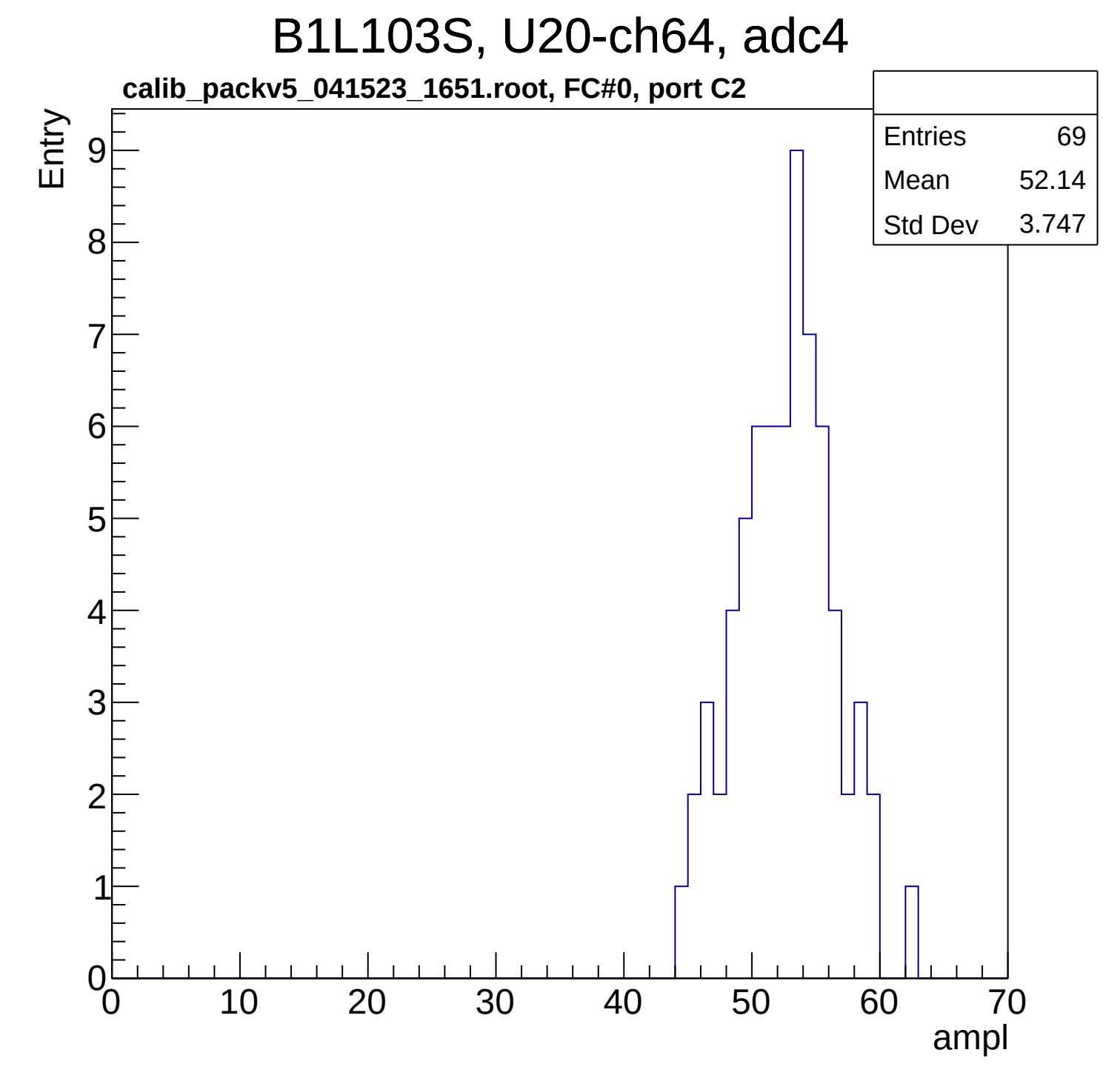
B1L103S, U20-ch64, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 52.14
Std Dev 3.747
Entry
ampl
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3
4
5
6
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0
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20
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40
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60
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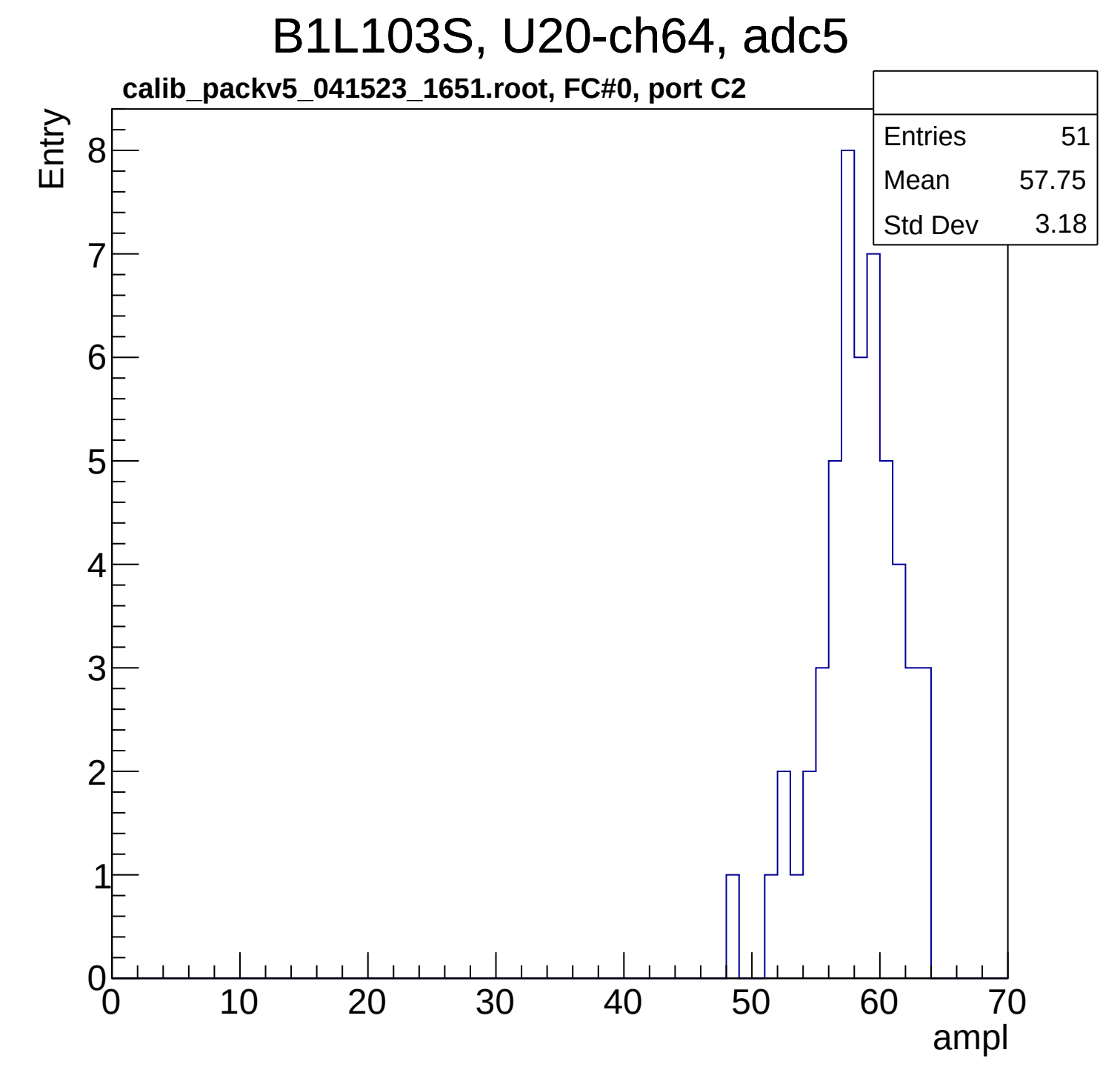
B1L103S, U20-ch64, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 57.75
Std Dev 3.18
Entry
ampl
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2
3
4
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6
7
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0
10
20
30
40
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60
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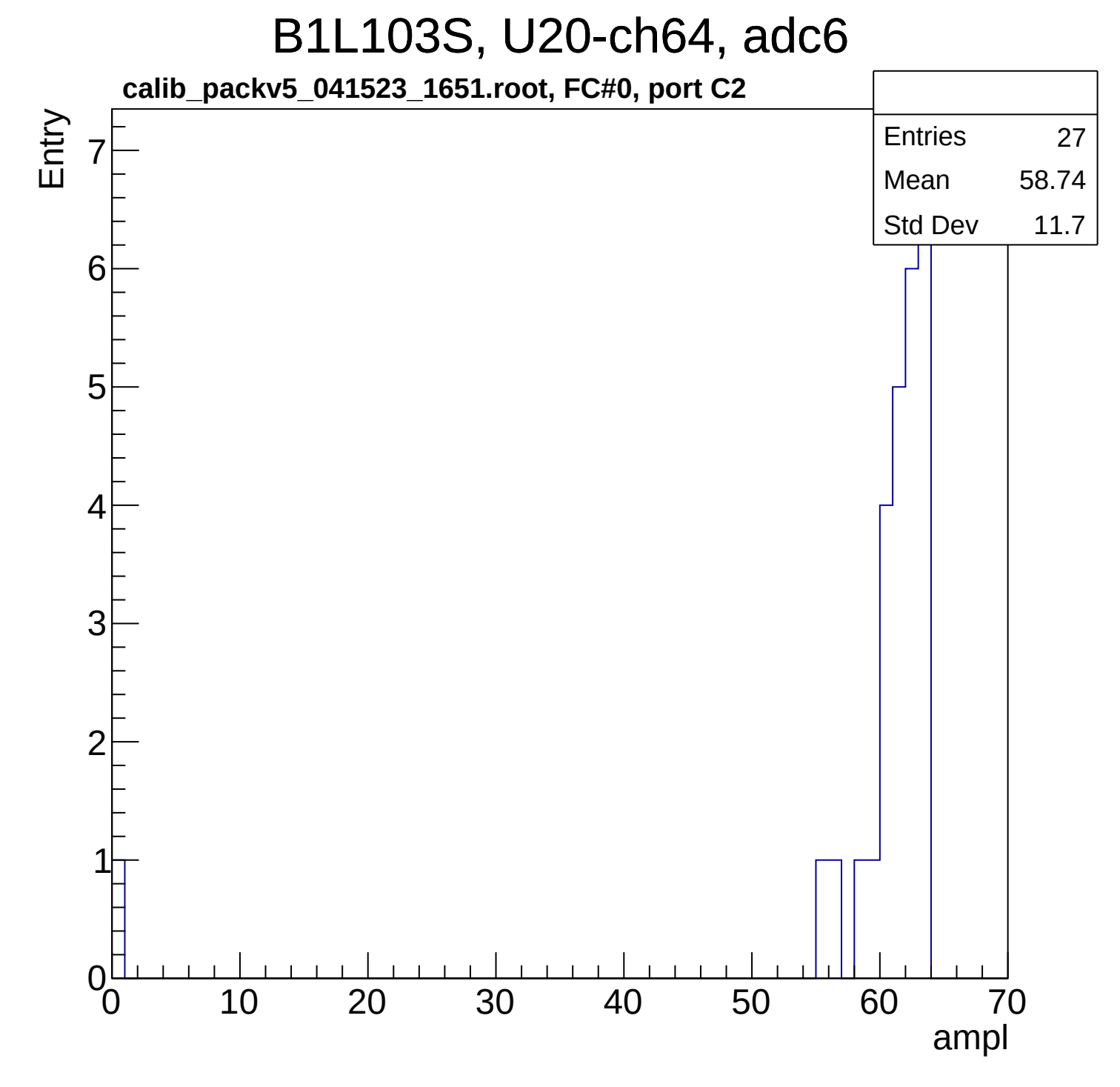
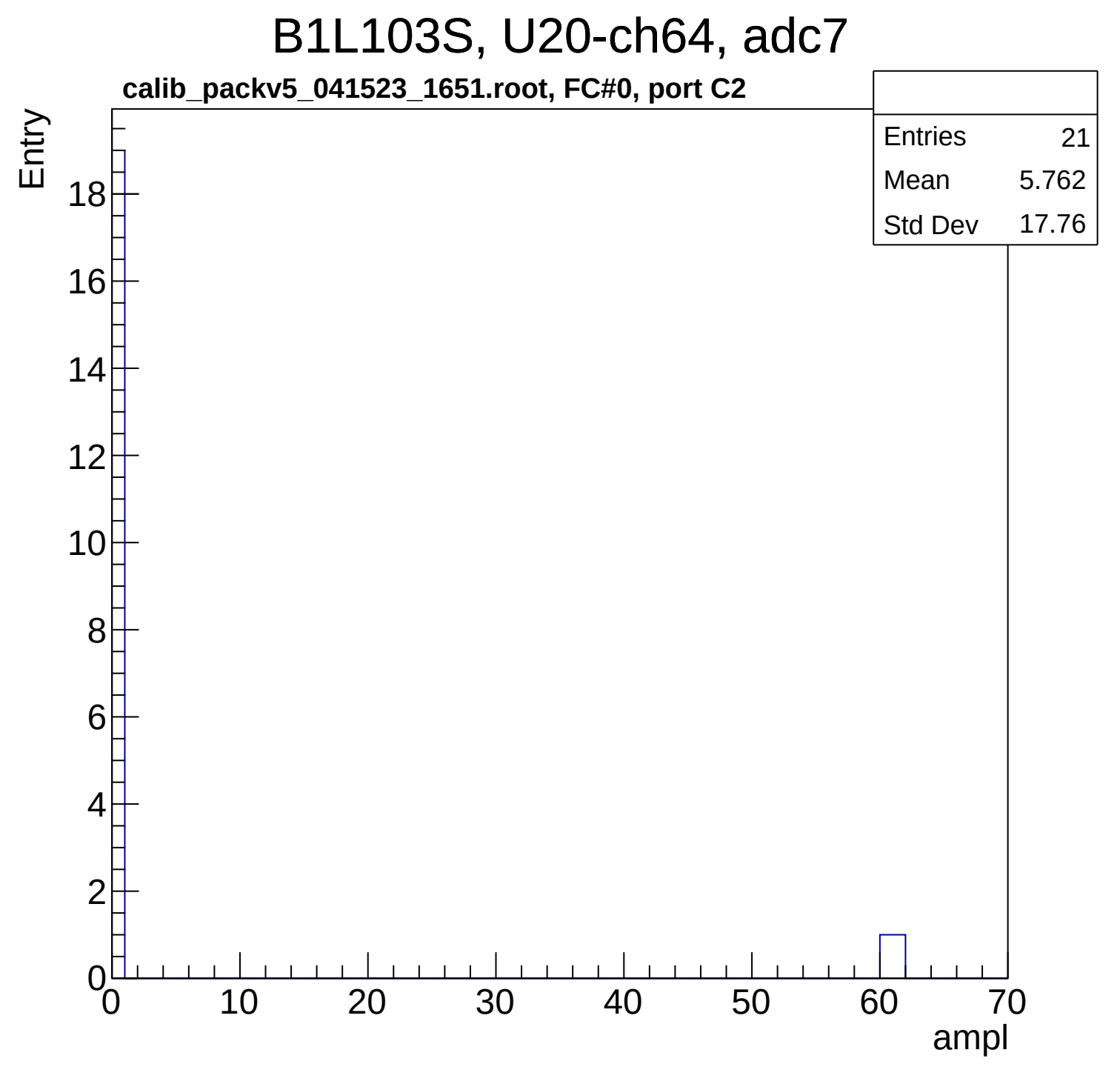

B1L103S, U20-ch64, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 58.74
Std Dev 11.7
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U20-ch64, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.762
Std Dev 17.76
Entry
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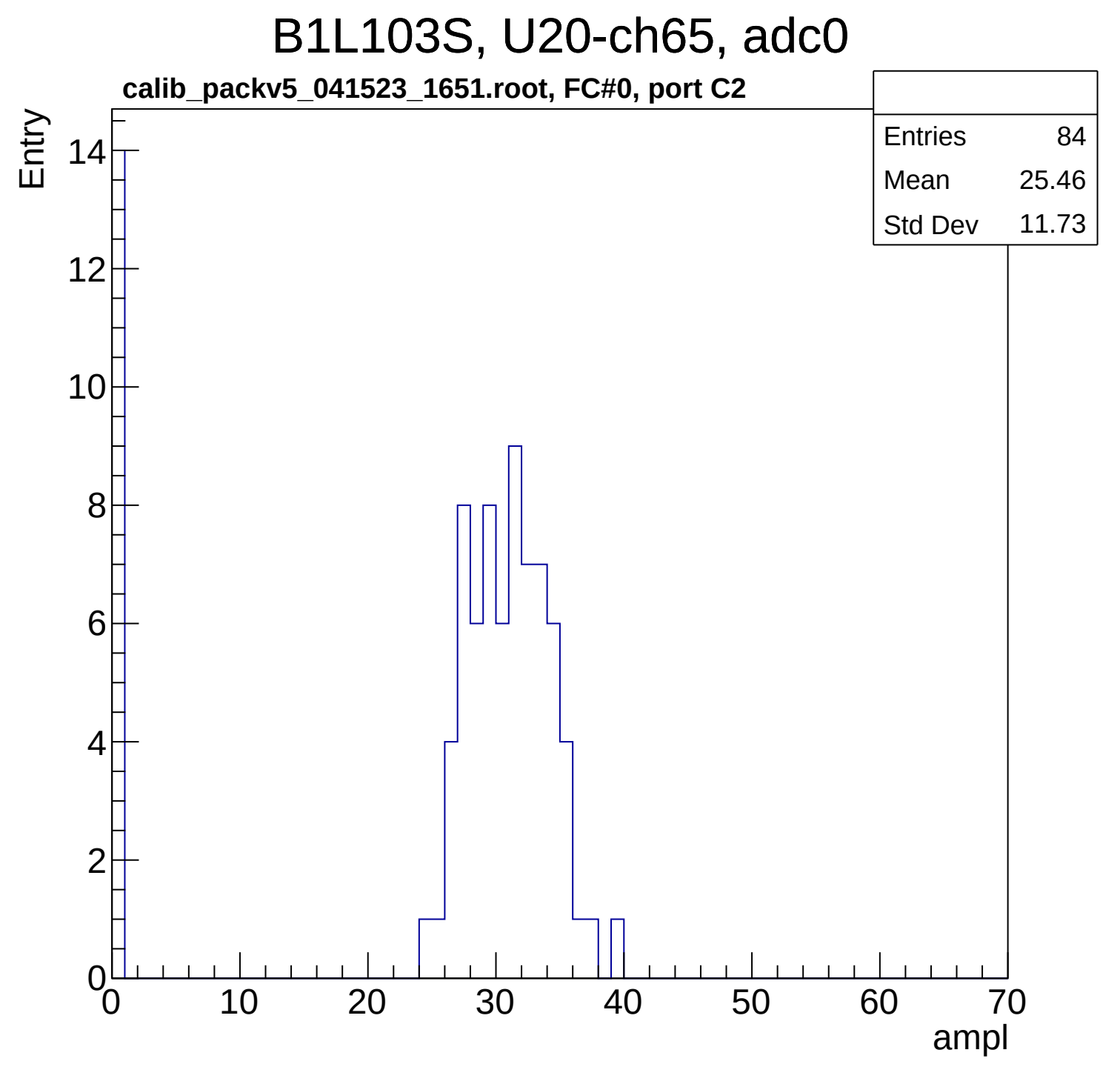
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch65, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 25.46
Std Dev 11.73
Entry
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2
4
6
8
10
12
14
0
10
20
30
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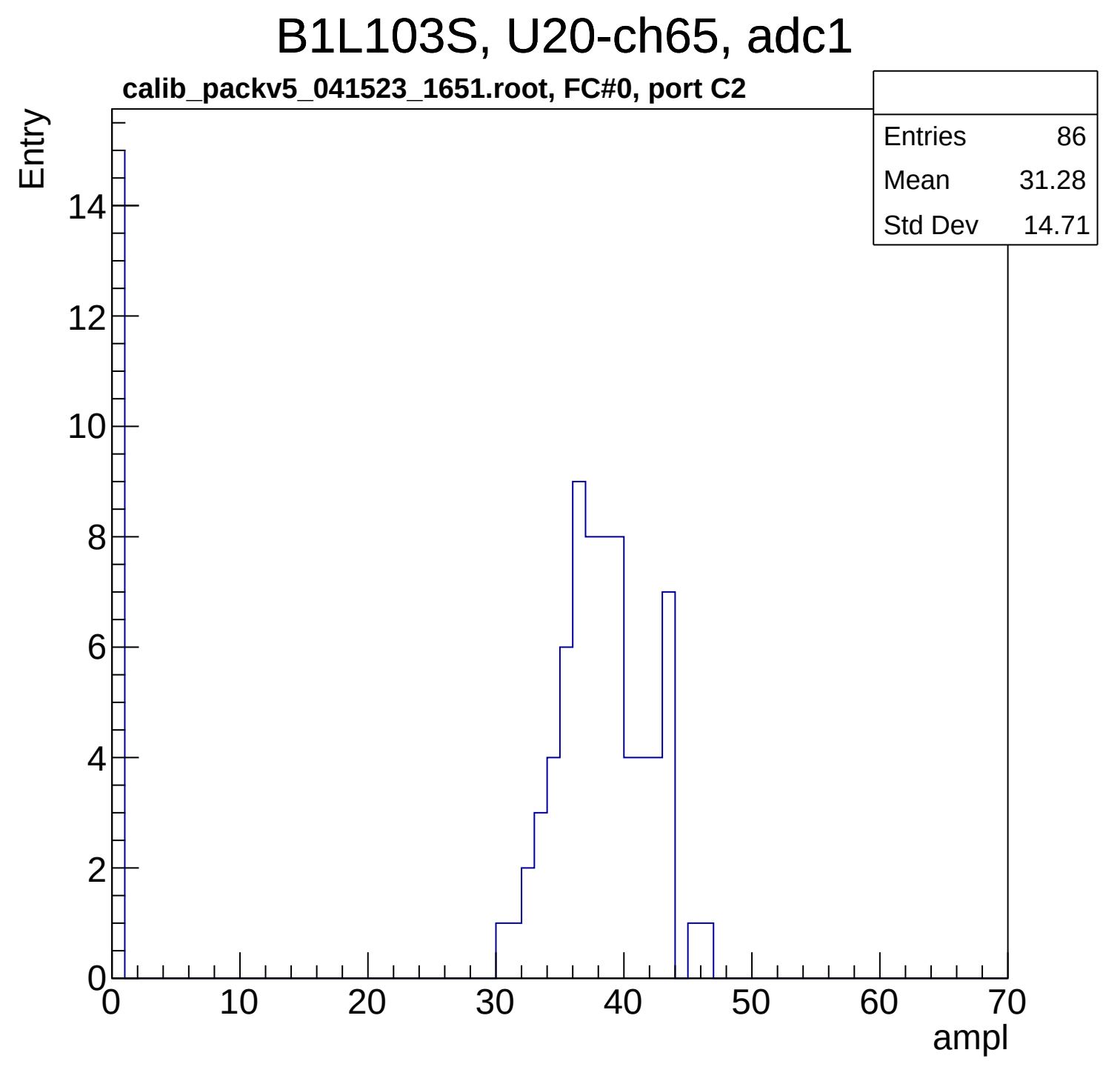
50
60
70
ampl


B1L103S, U20-ch65, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 31.28
Std Dev 14.71
Entry
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2
4
6
8
10
12
14
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10
20
30
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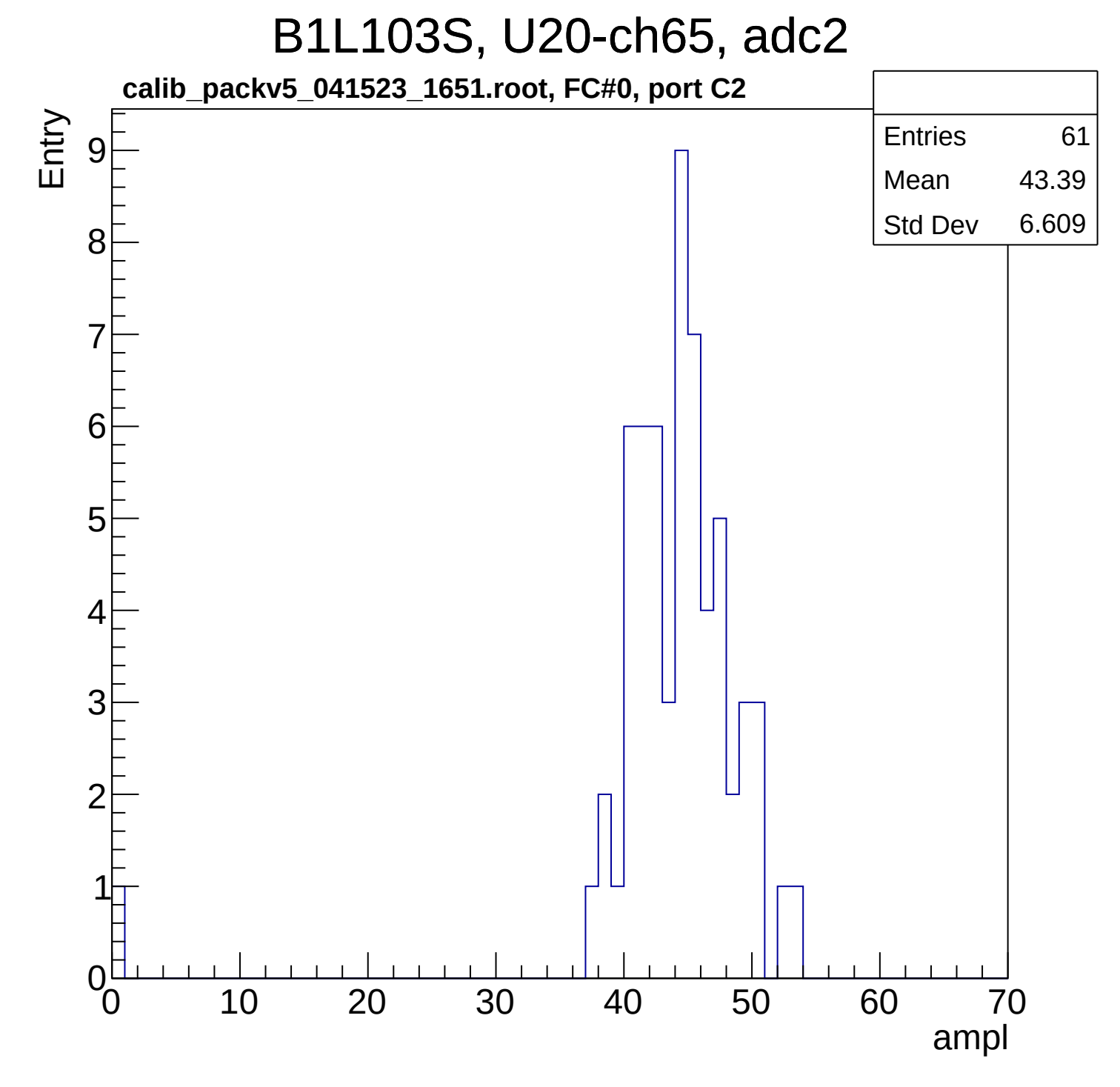
50
60
70
ampl


B1L103S, U20-ch65, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 43.39
Std Dev 6.609
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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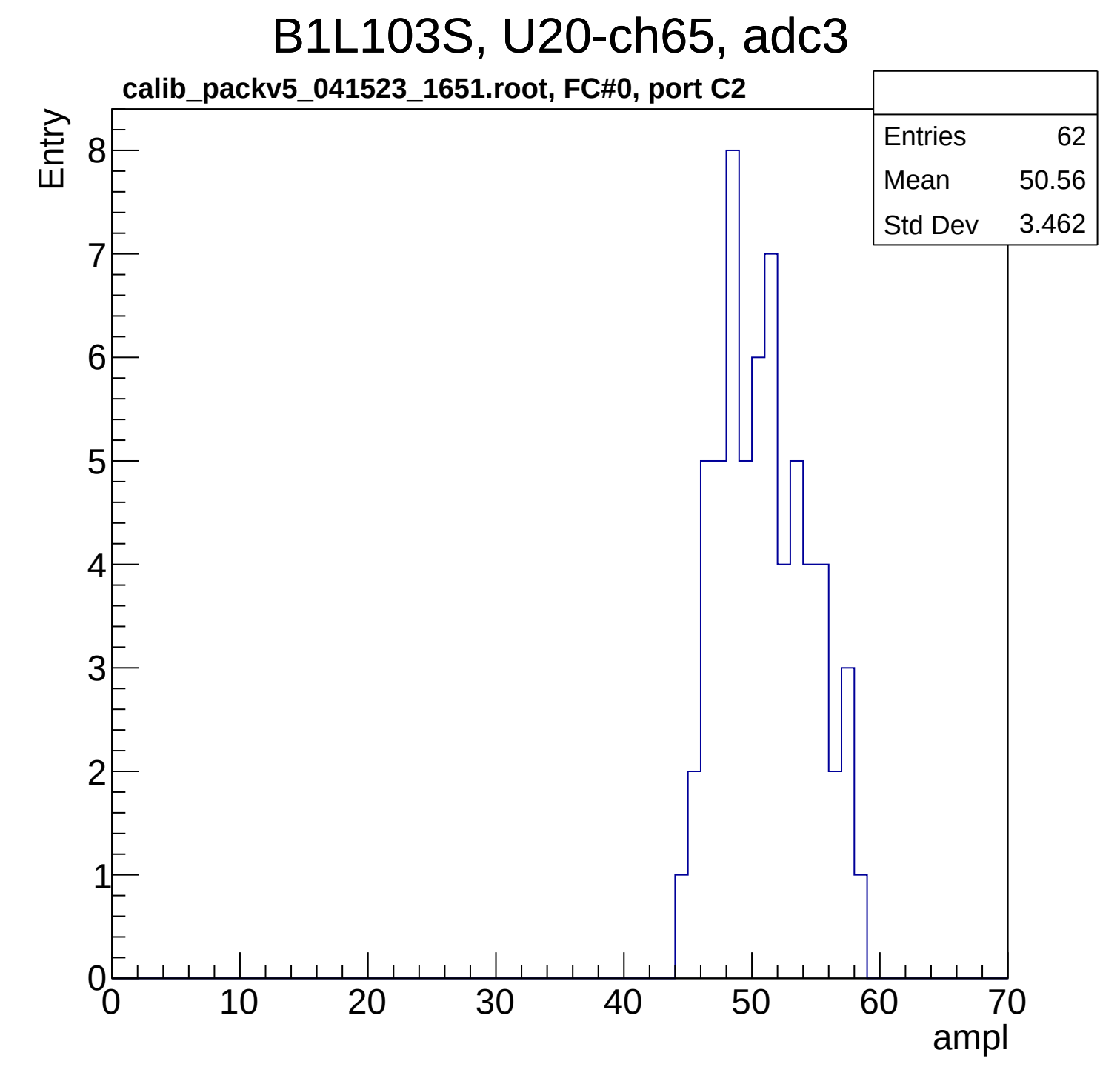
B1L103S, U20-ch65, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 50.56
Std Dev 3.462
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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60
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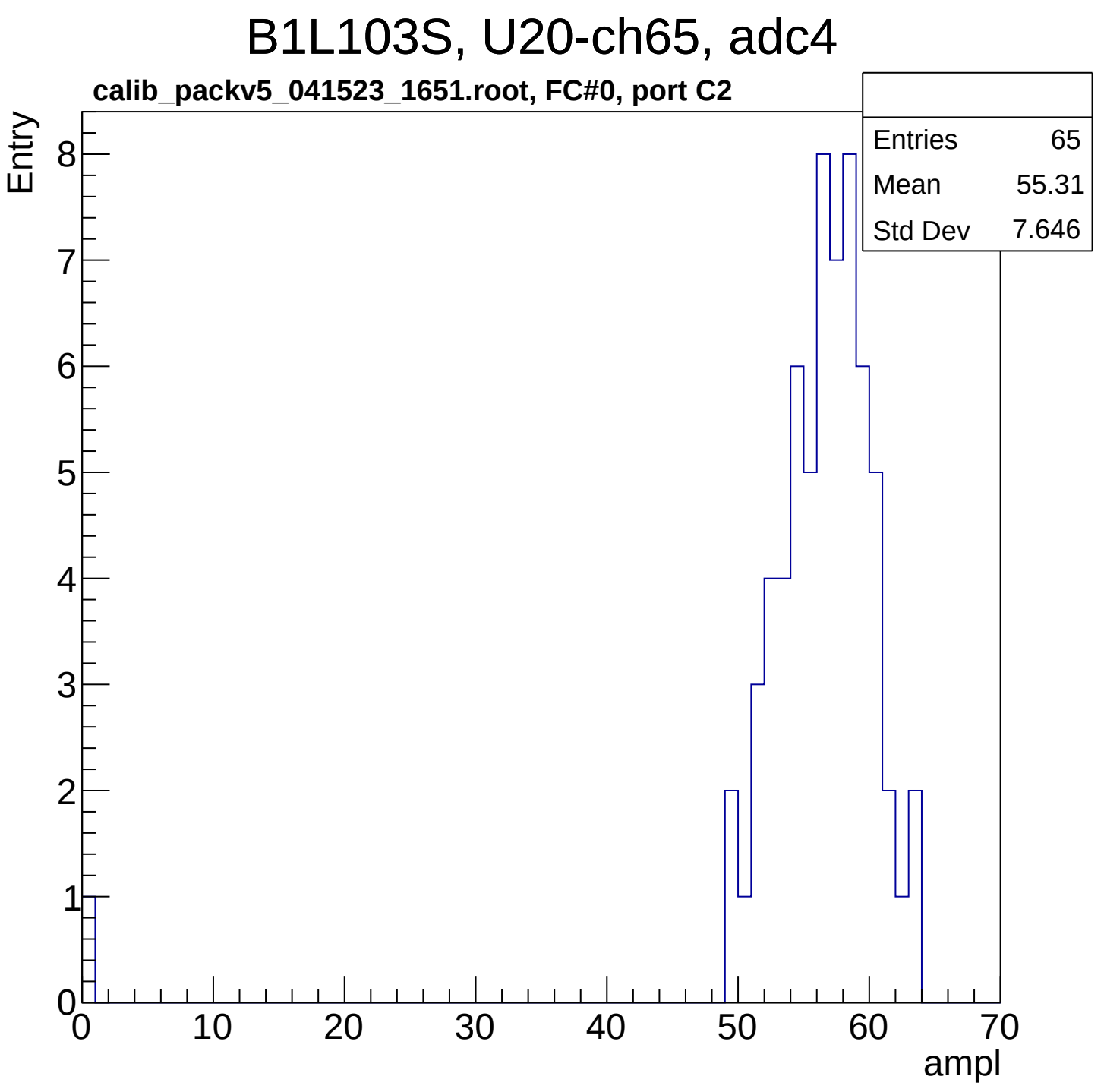
B1L103S, U20-ch65, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 55.31
Std Dev 7.646
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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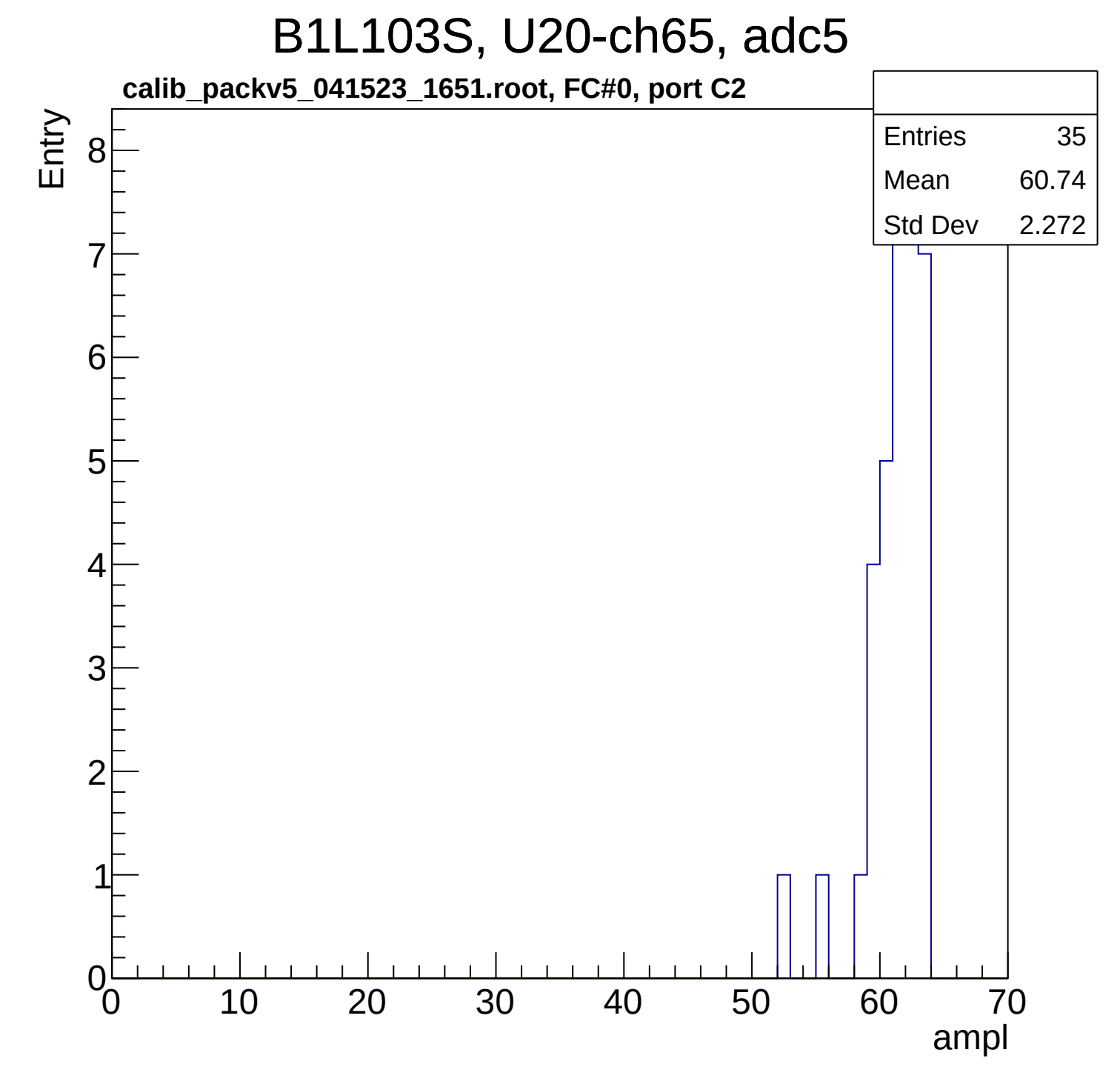
B1L103S, U20-ch65, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 60.74
Std Dev 2.272
Entry
ampl
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1
2
3
4
5
6
7
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0
10
20
30
40
50
60
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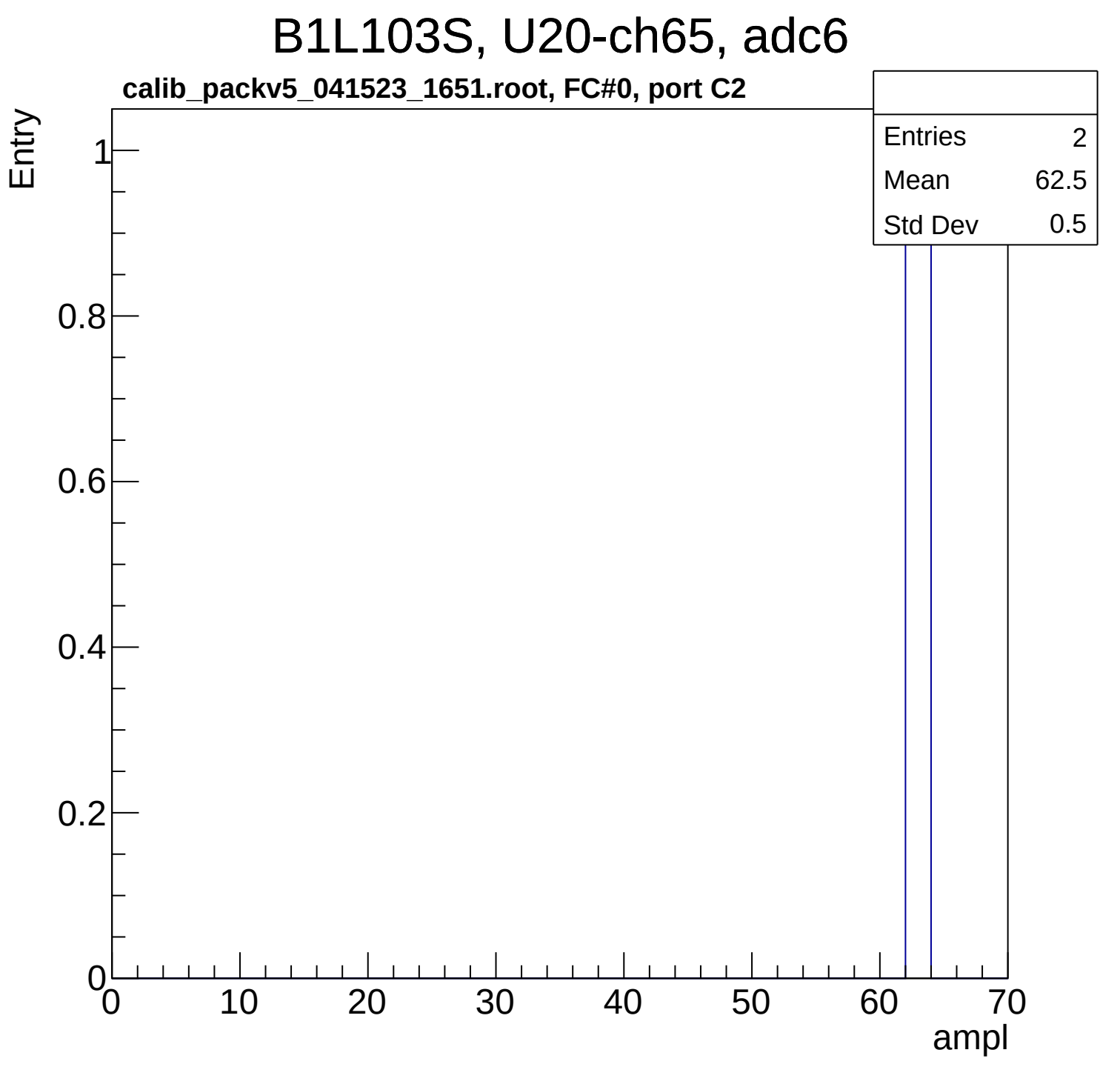
B1L103S, U20-ch65, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
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0.6
0.4
0.2
0
0
10
20
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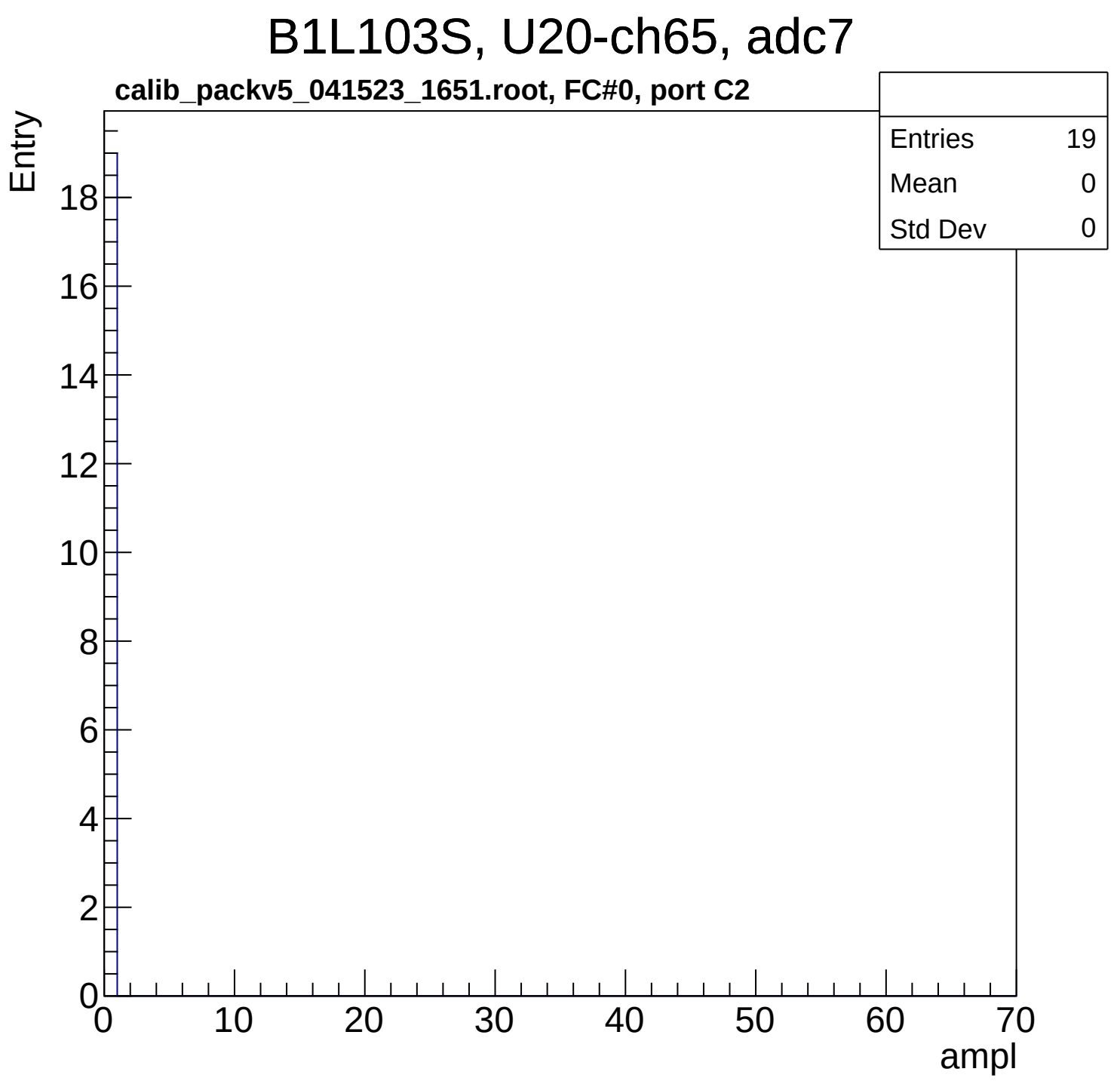
50
60
70
ampl


B1L103S, U20-ch65, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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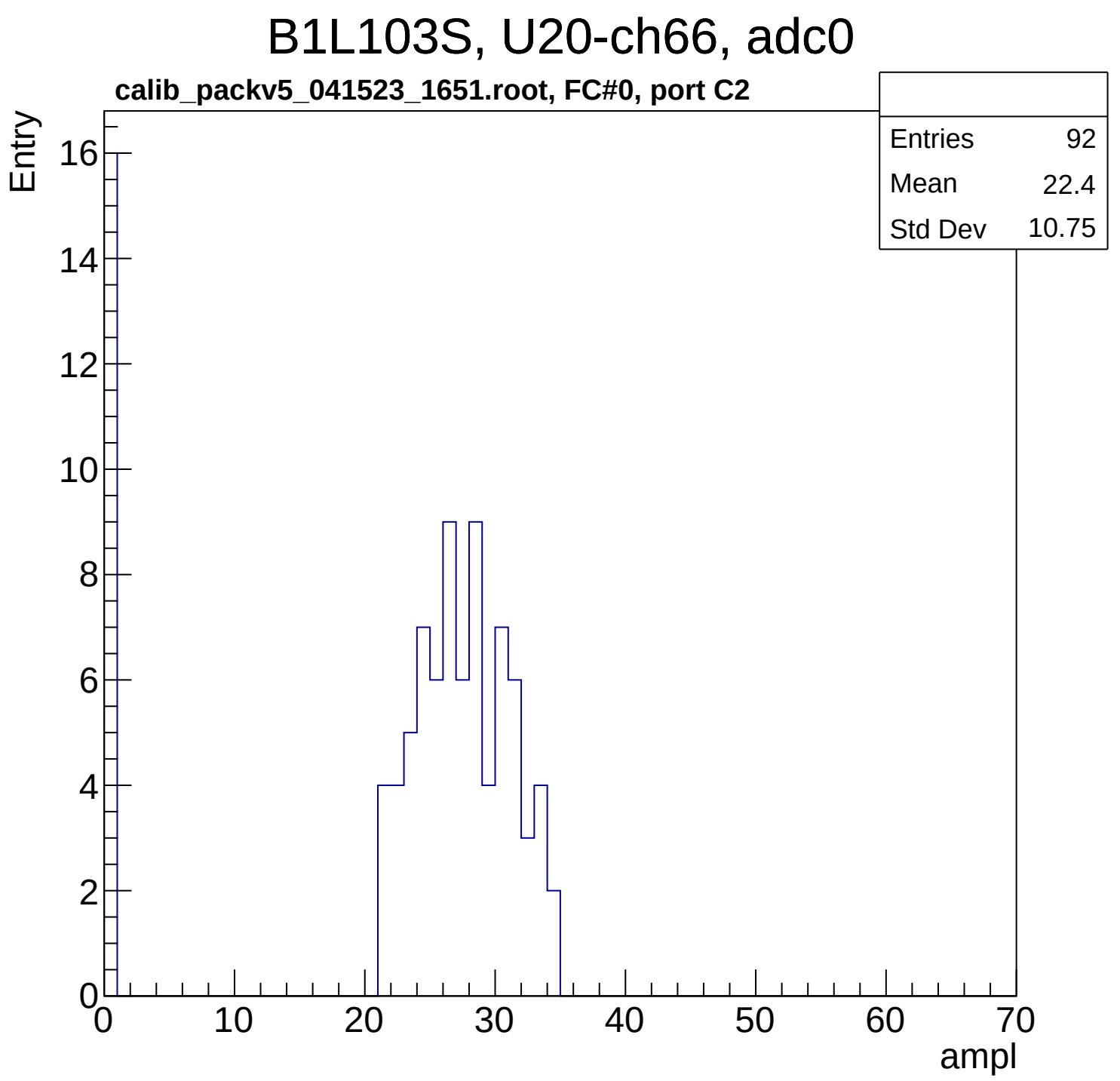
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch66, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 22.4
Std Dev 10.75
Entry
ampl
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4
6
8
10
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16
0
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20
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40
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60
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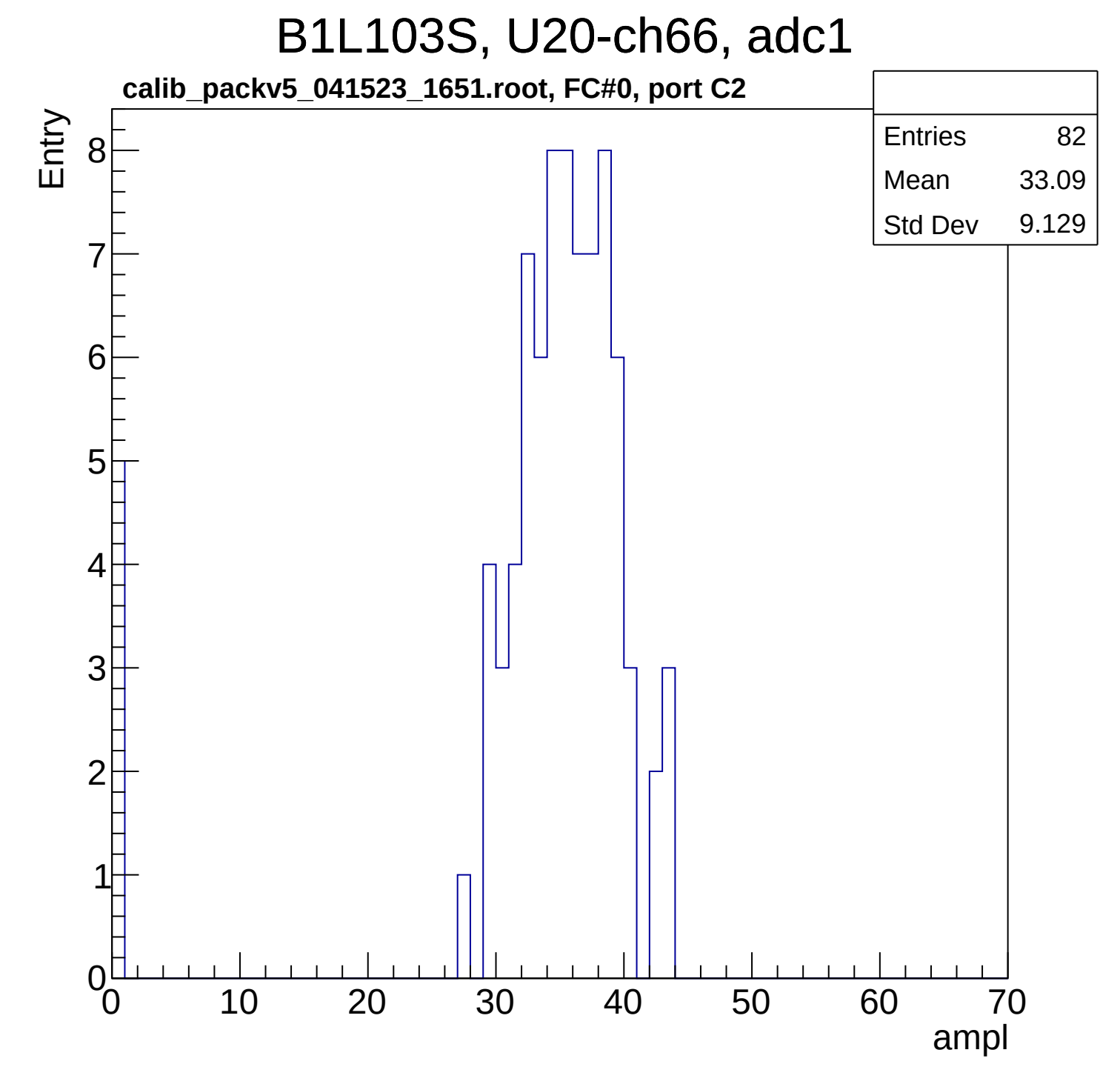
B1L103S, U20-ch66, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 33.09
Std Dev 9.129
Entry
ampl
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4
5
6
7
8
0
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20
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40
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60
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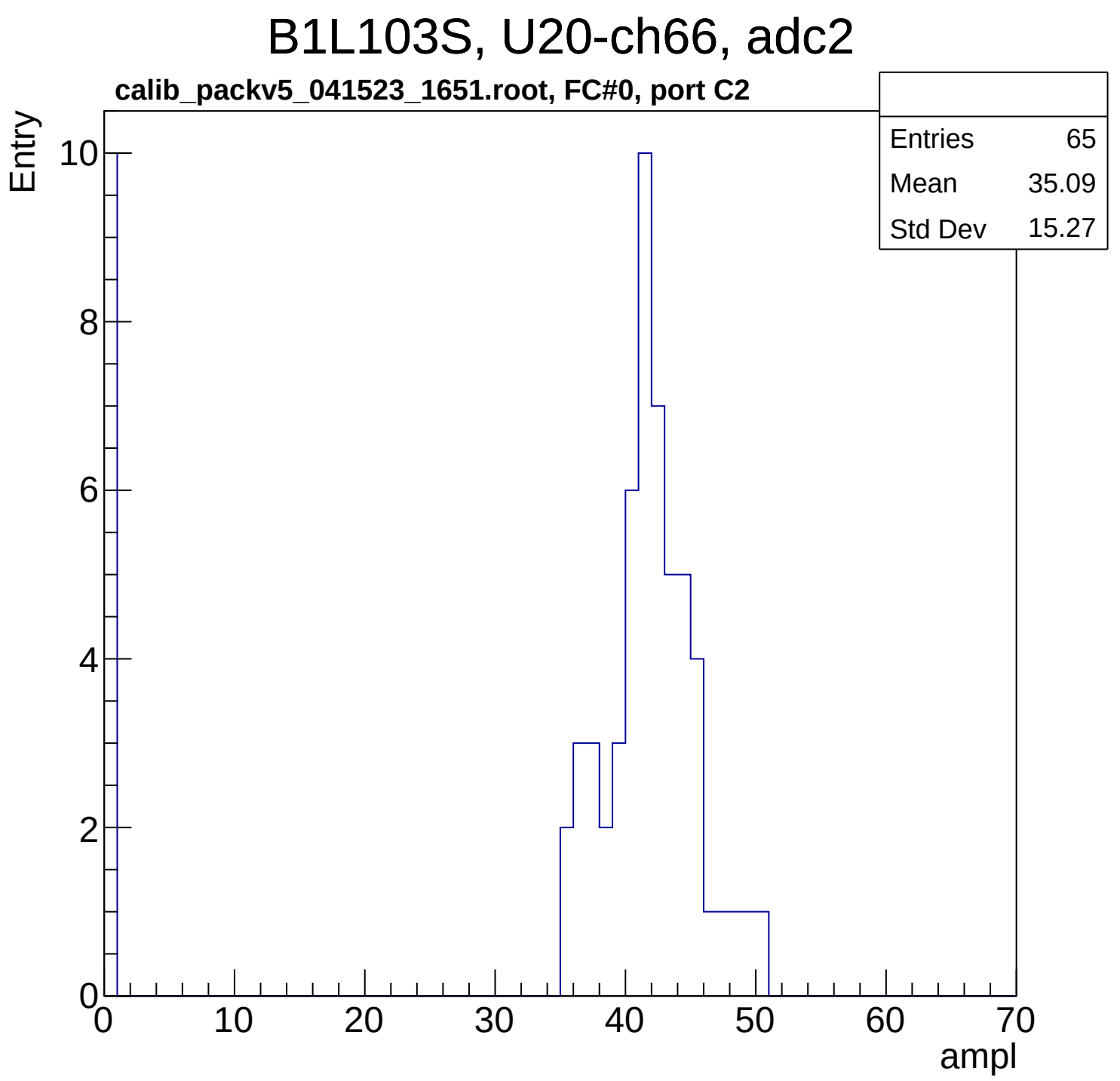
B1L103S, U20-ch66, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 35.09
Std Dev 15.27
Entry
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2
4
6
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10
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10
20
30
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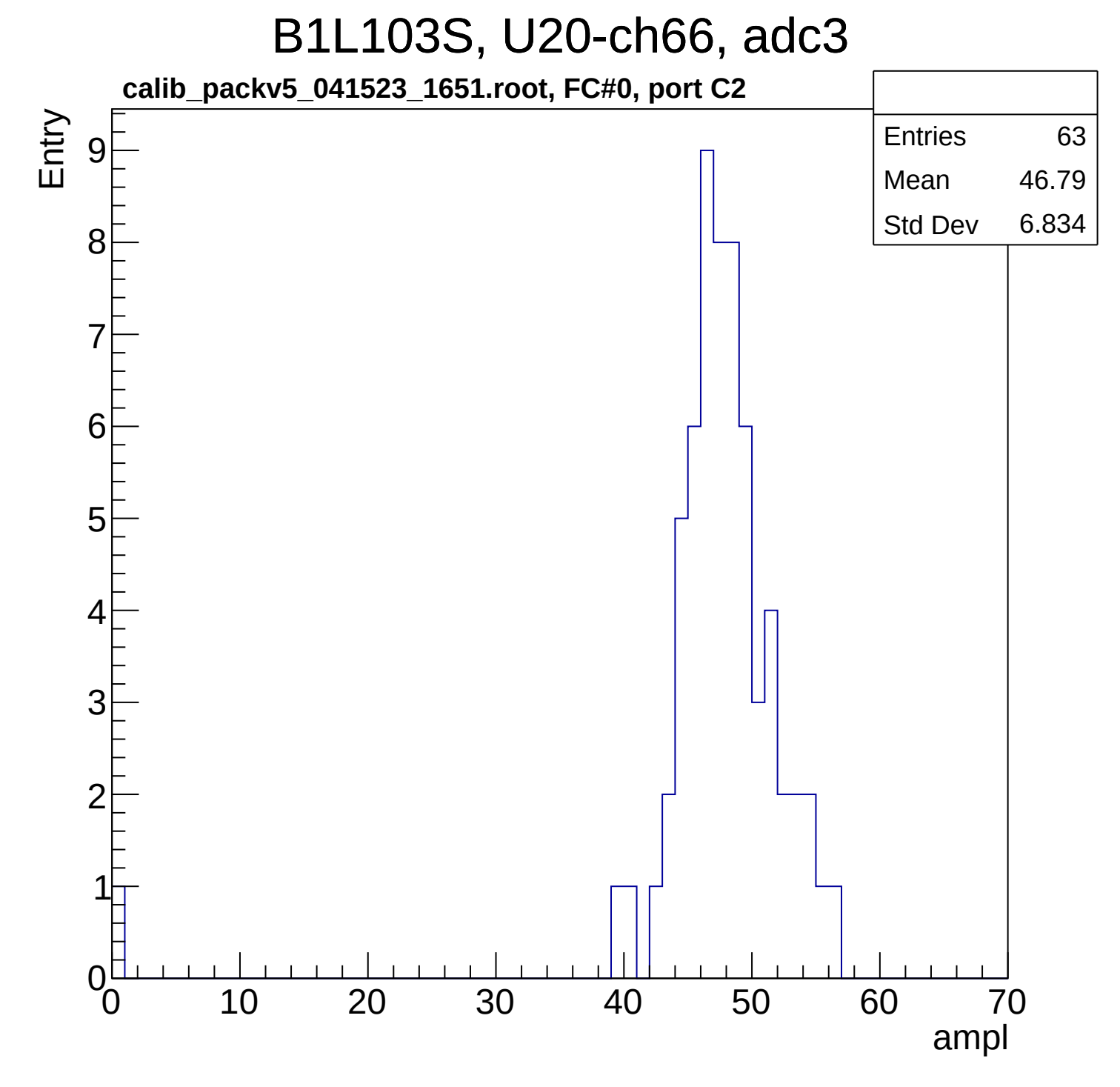
50
60
70
ampl


B1L103S, U20-ch66, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 46.79
Std Dev 6.834
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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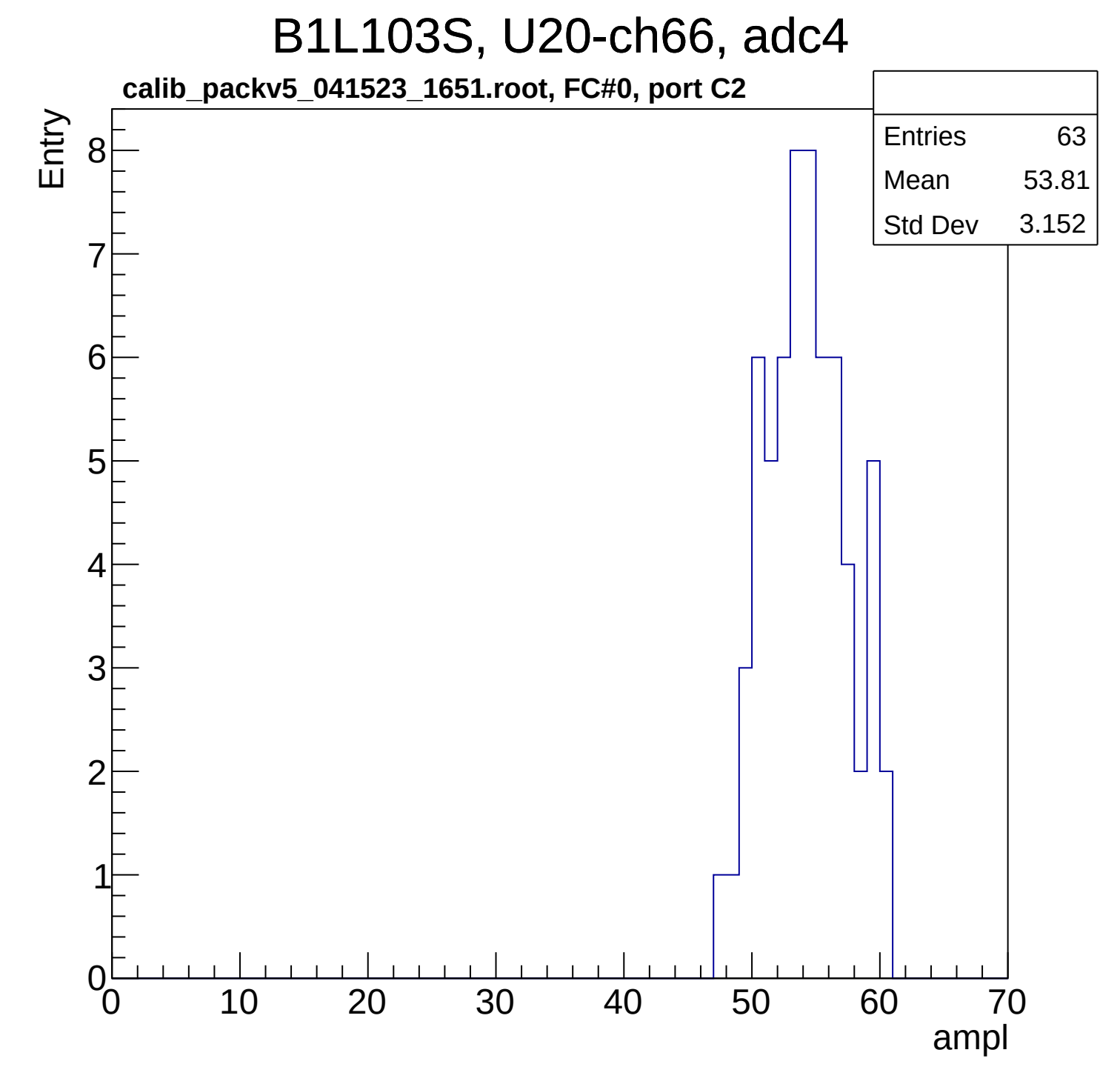
40
50
60
70


B1L103S, U20-ch66, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 53.81
Std Dev 3.152
Entry
ampl
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2
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4
5
6
7
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0
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20
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40
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60
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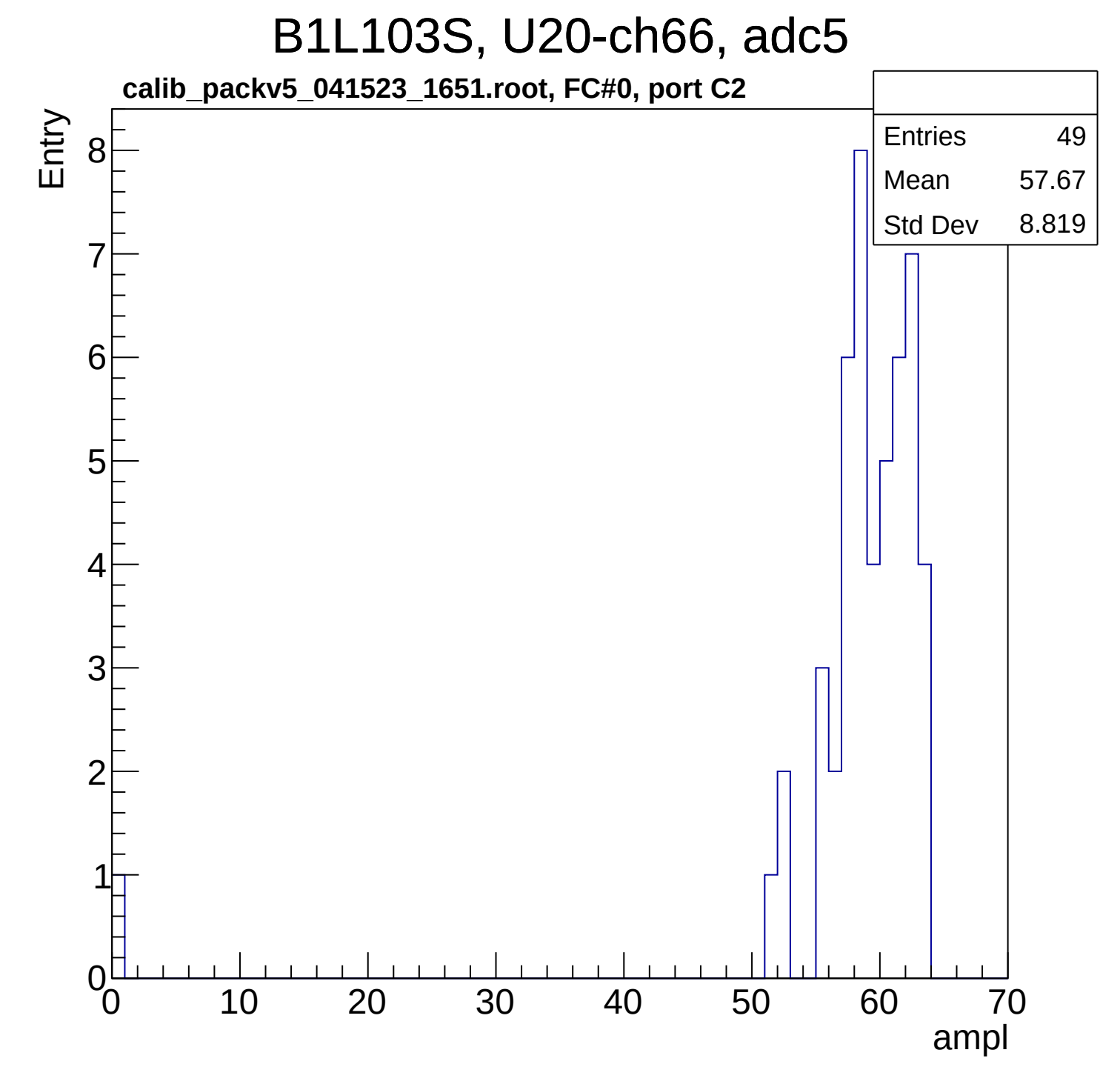
B1L103S, U20-ch66, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 57.67
Std Dev 8.819
Entry
ampl
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2
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4
5
6
7
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0
10
20
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40
50
60
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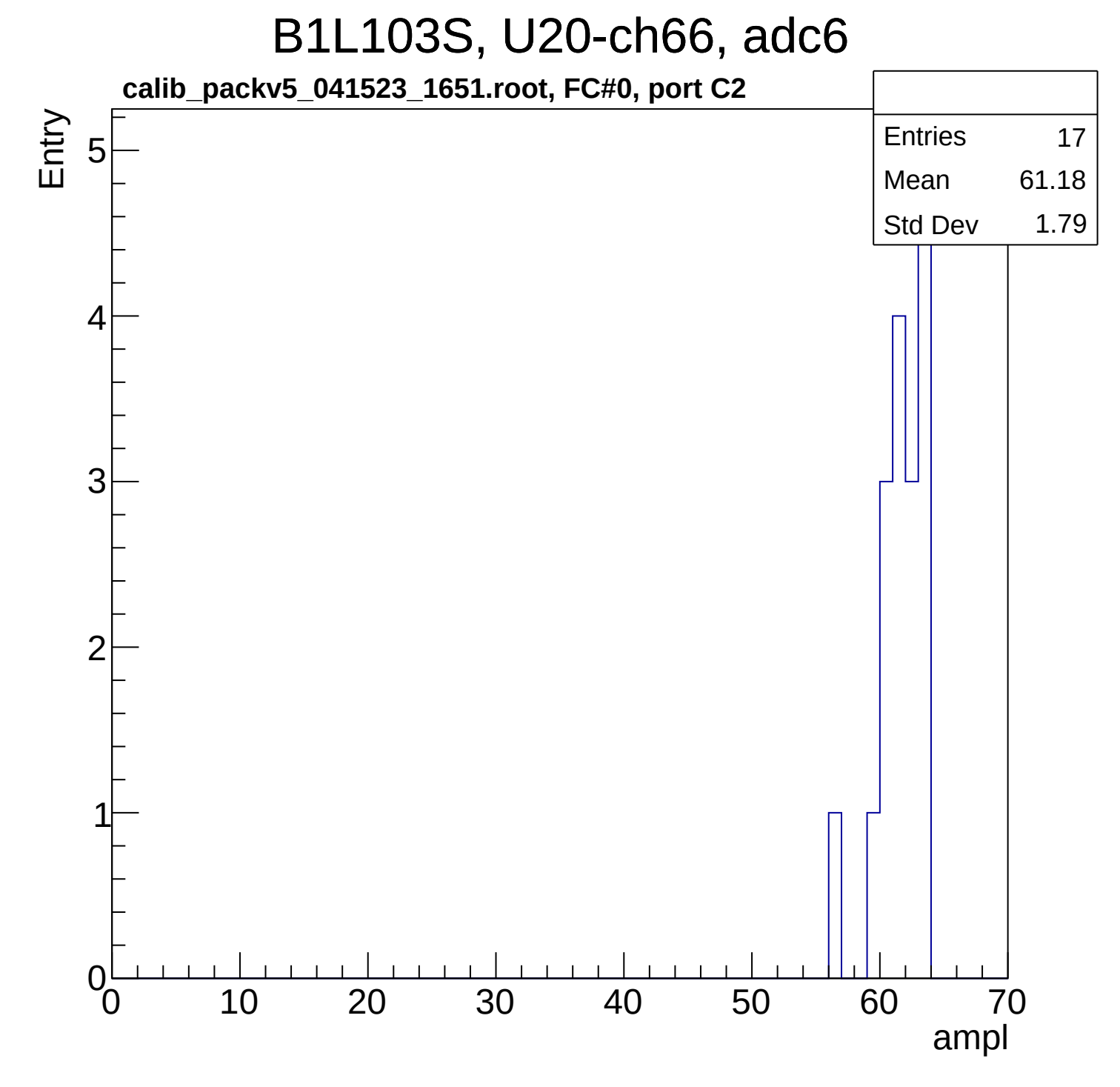
B1L103S, U20-ch66, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 61.18
Std Dev 1.79
Entry
ampl
0
1
2
3
4
5
0
10
20
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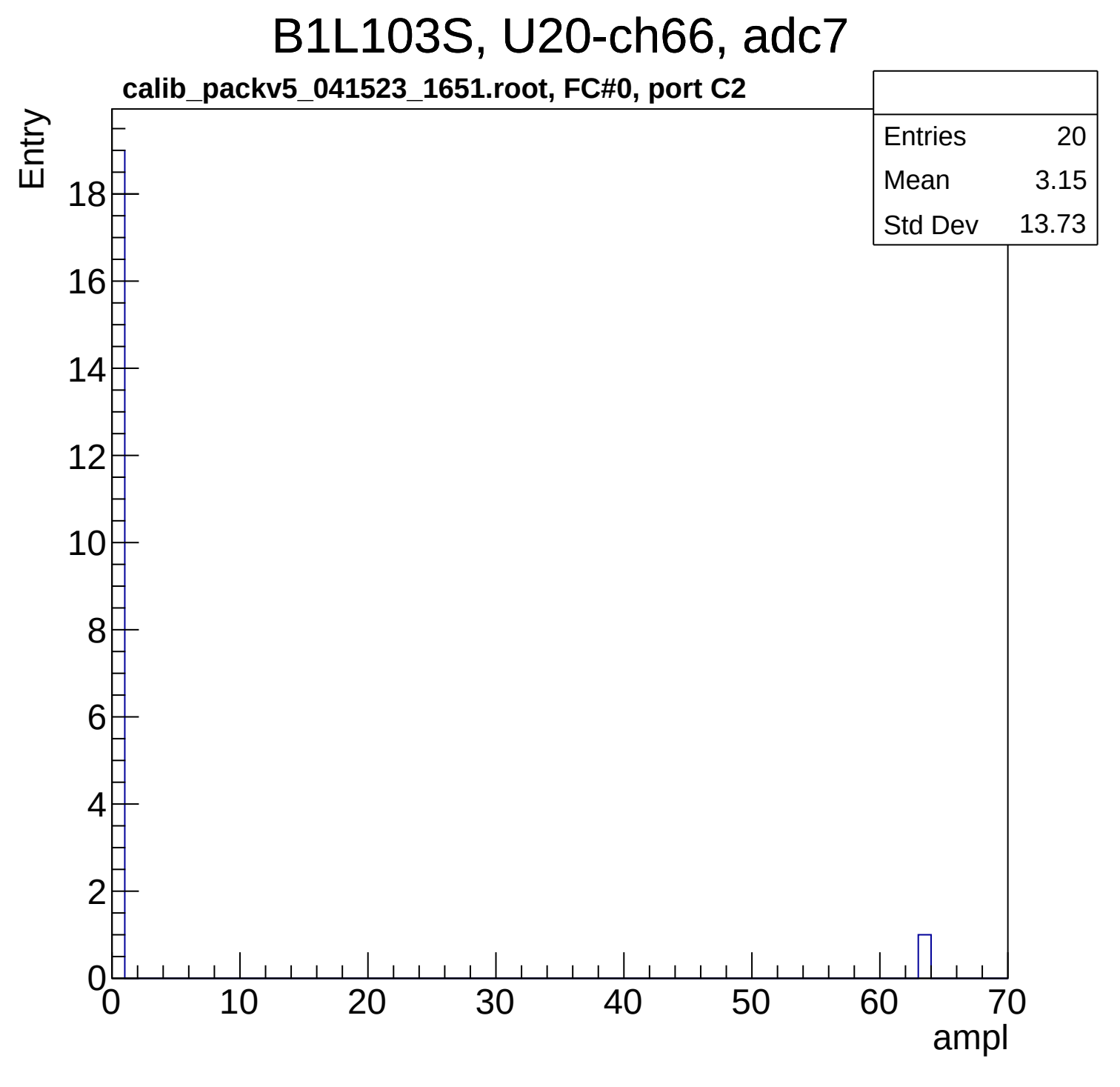
40
50
60
70


B1L103S, U20-ch66, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
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6
8
10
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16
18
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10
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50
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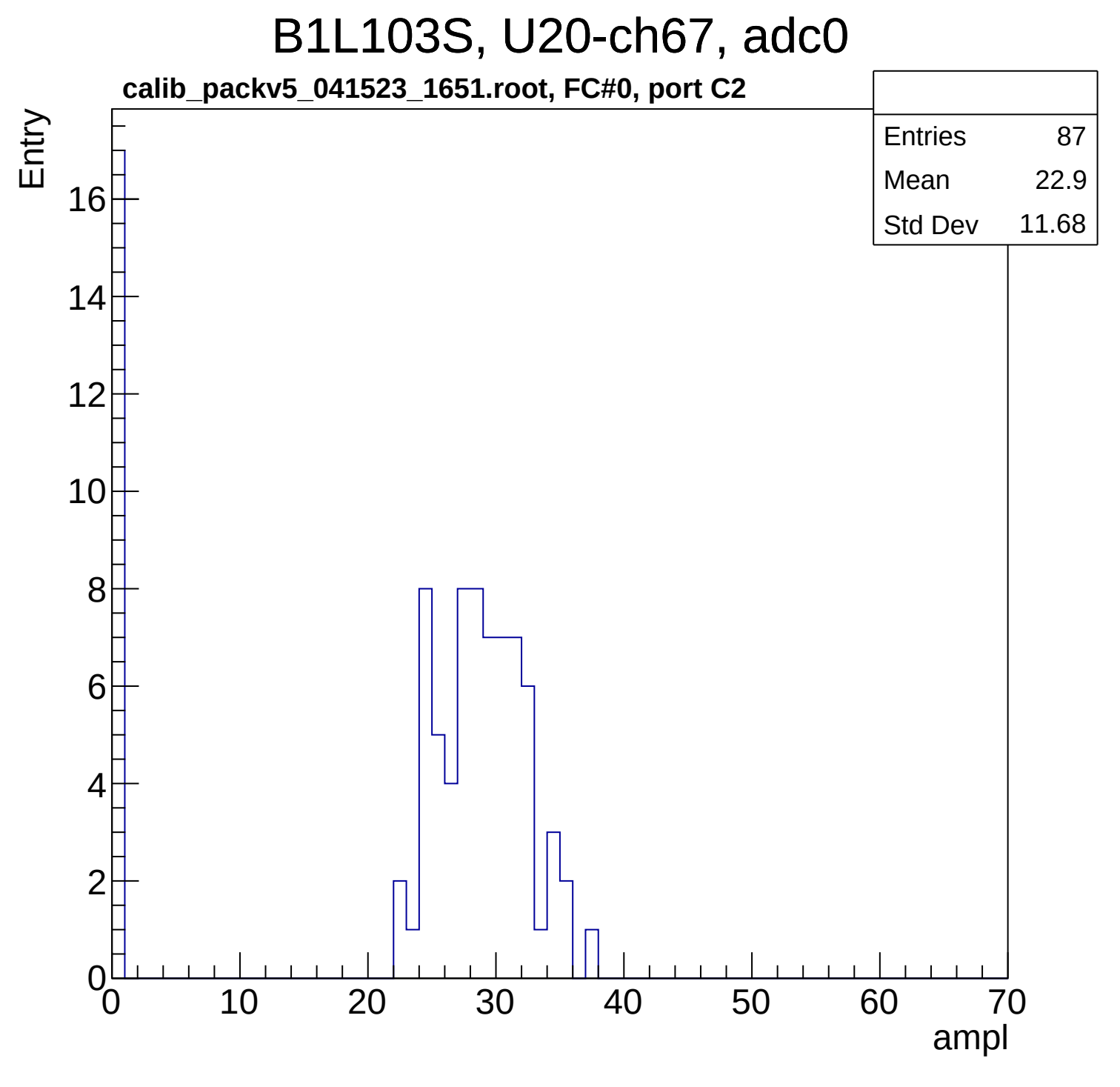
70
ampl


B1L103S, U20-ch67, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 22.9
Std Dev 11.68
Entry
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20
30
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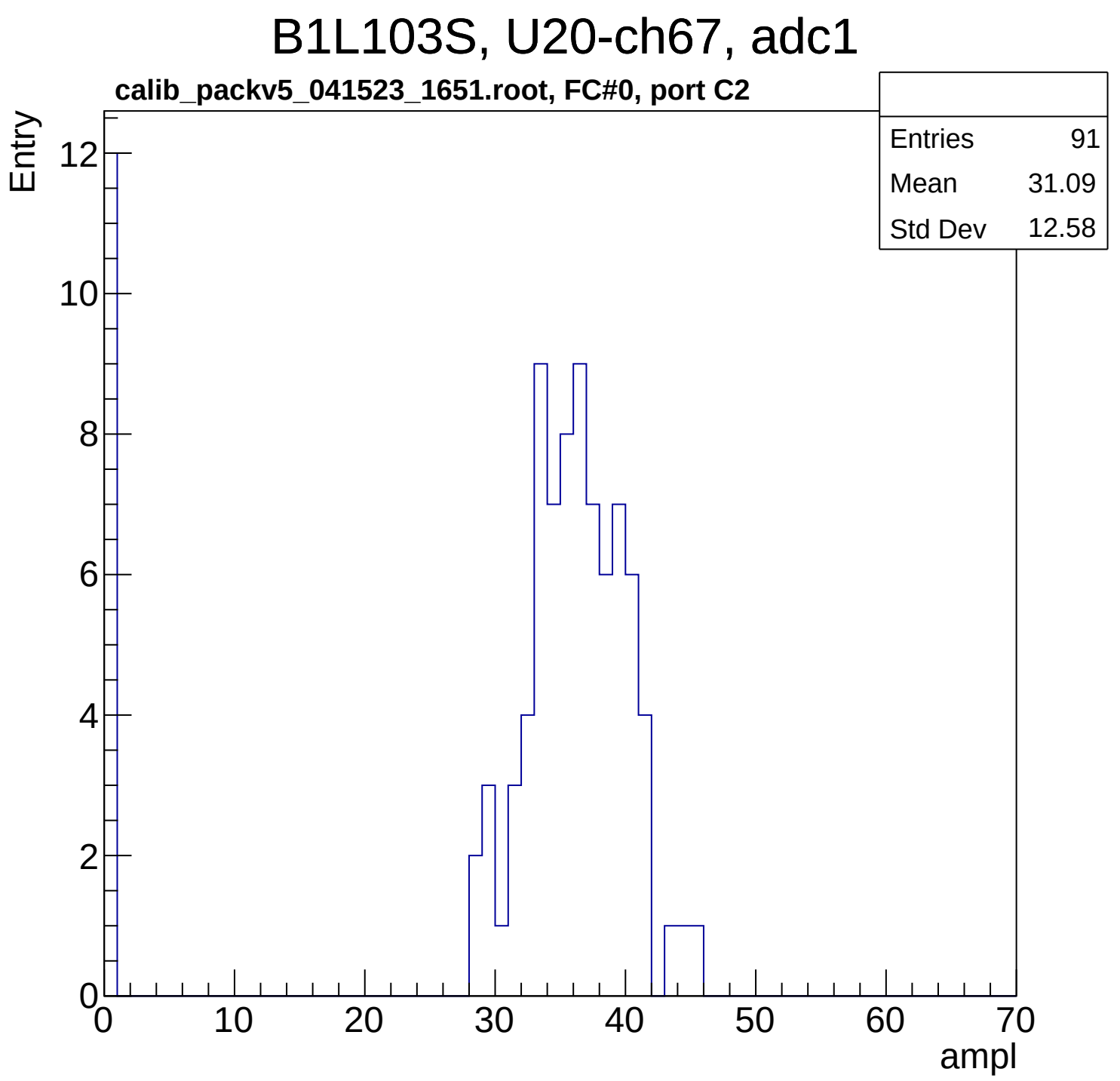
50
60
70
ampl


B1L103S, U20-ch67, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 31.09
Std Dev 12.58
Entry
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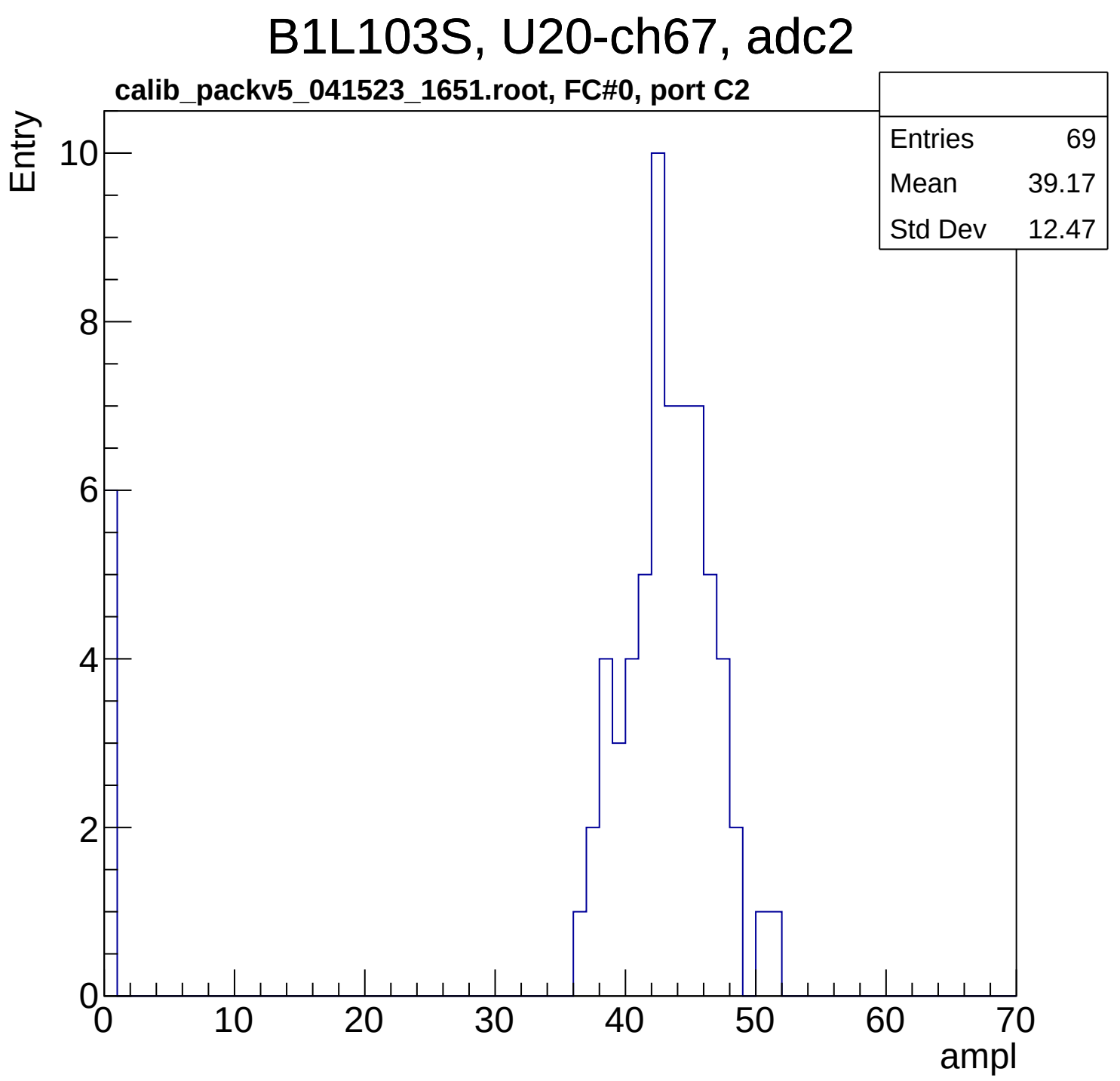
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch67, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 39.17
Std Dev 12.47
Entry
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6
8
10
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10
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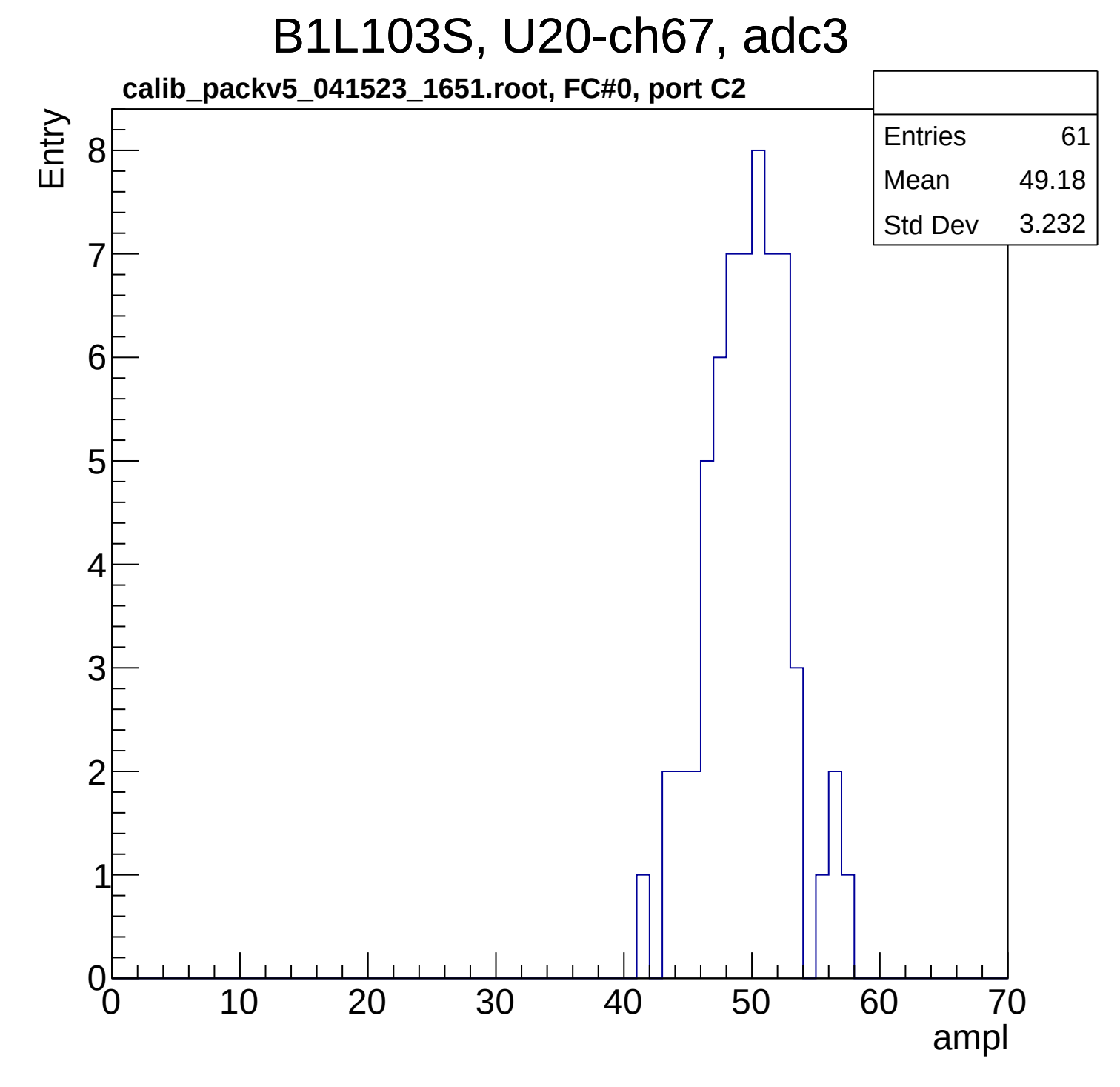
30
40
50
60
70
ampl


B1L103S, U20-ch67, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 49.18
Std Dev 3.232
Entry
ampl
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4
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6
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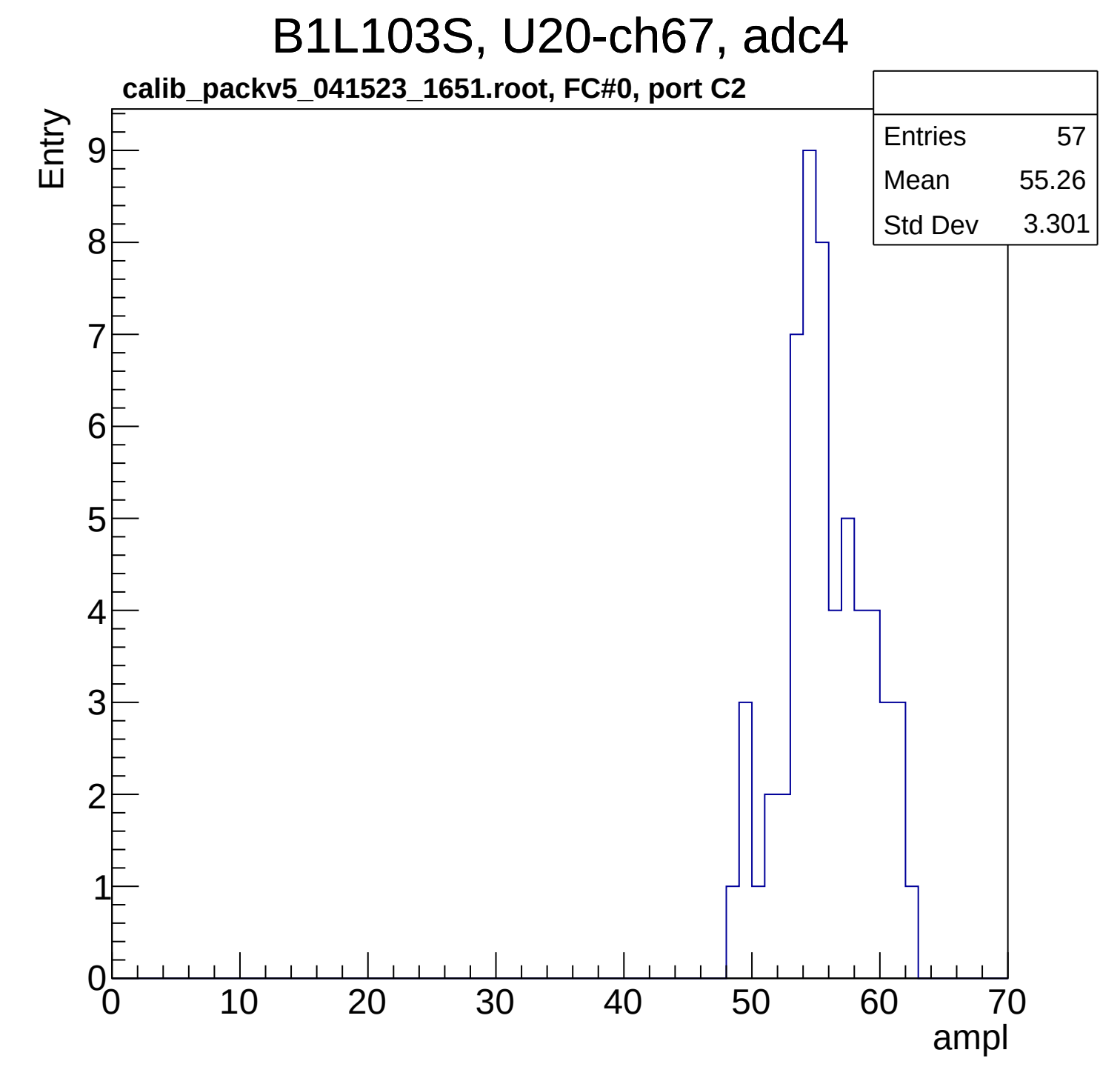
B1L103S, U20-ch67, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 55.26
Std Dev 3.301
Entry
ampl
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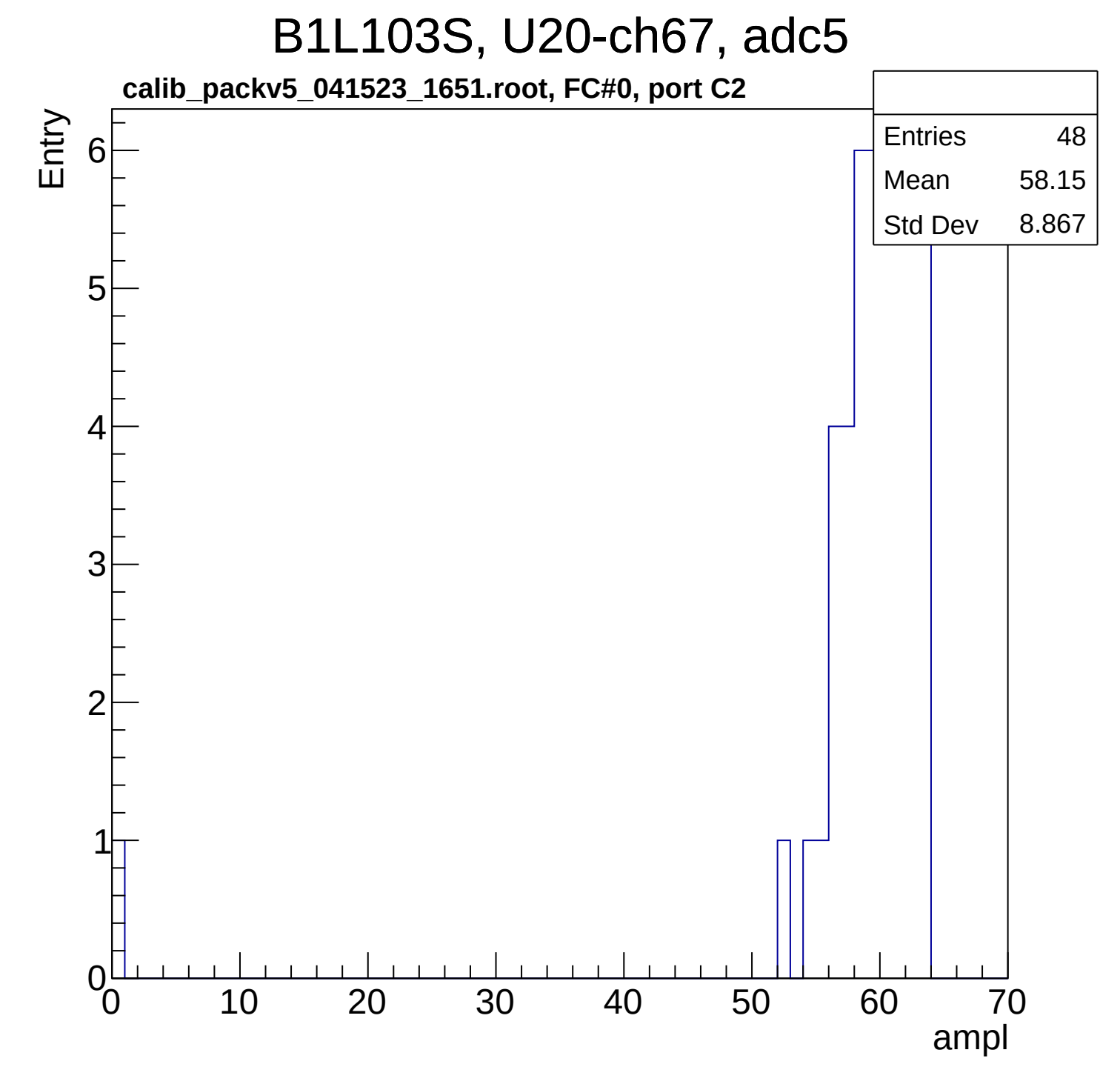
B1L103S, U20-ch67, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 58.15
Std Dev 8.867
Entry
ampl
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1
2
3
4
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0
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60
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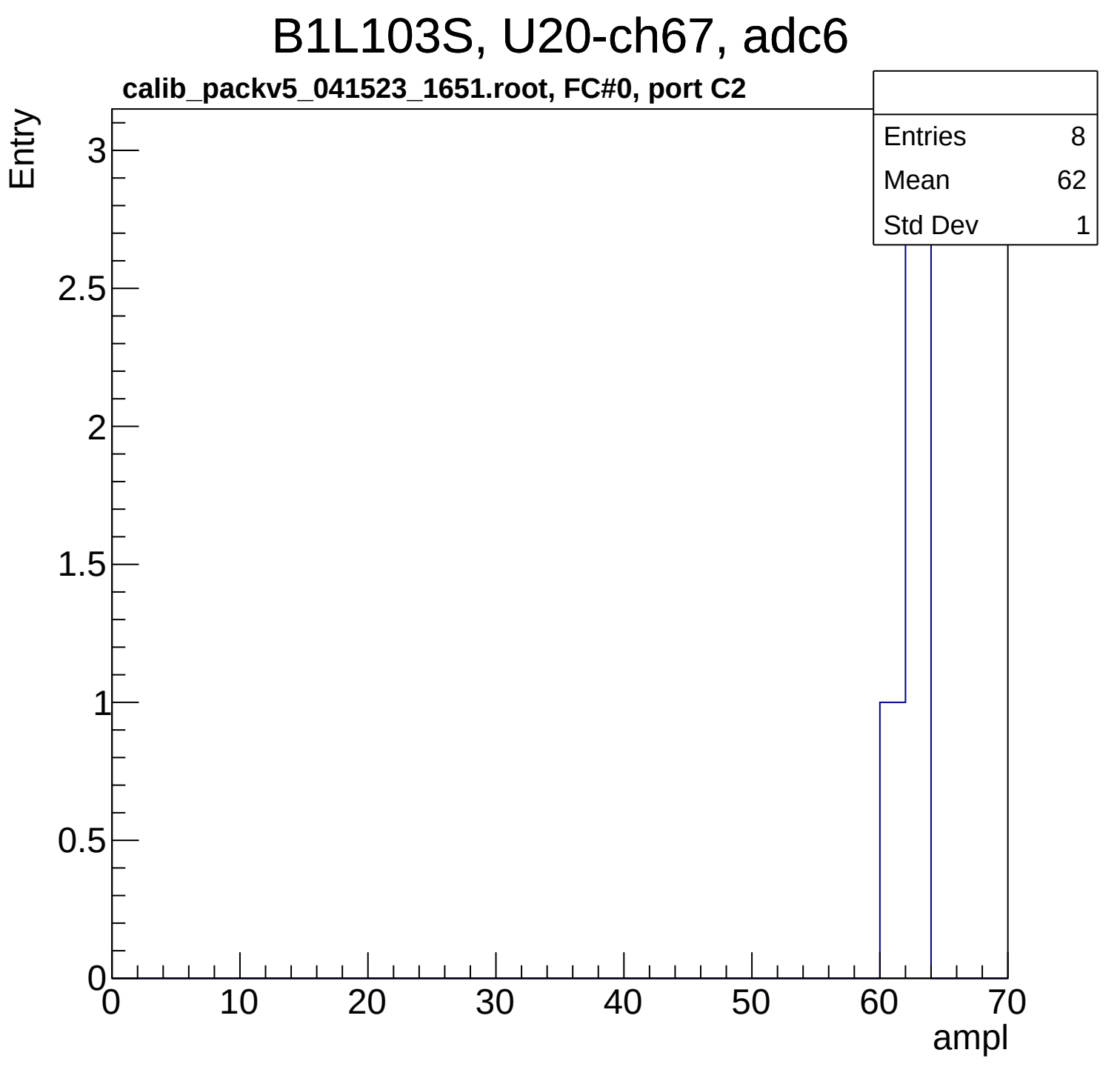
B1L103S, U20-ch67, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 62
Std Dev 1
Entry
ampl
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1
1.5
2
2.5
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0
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20
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40
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60
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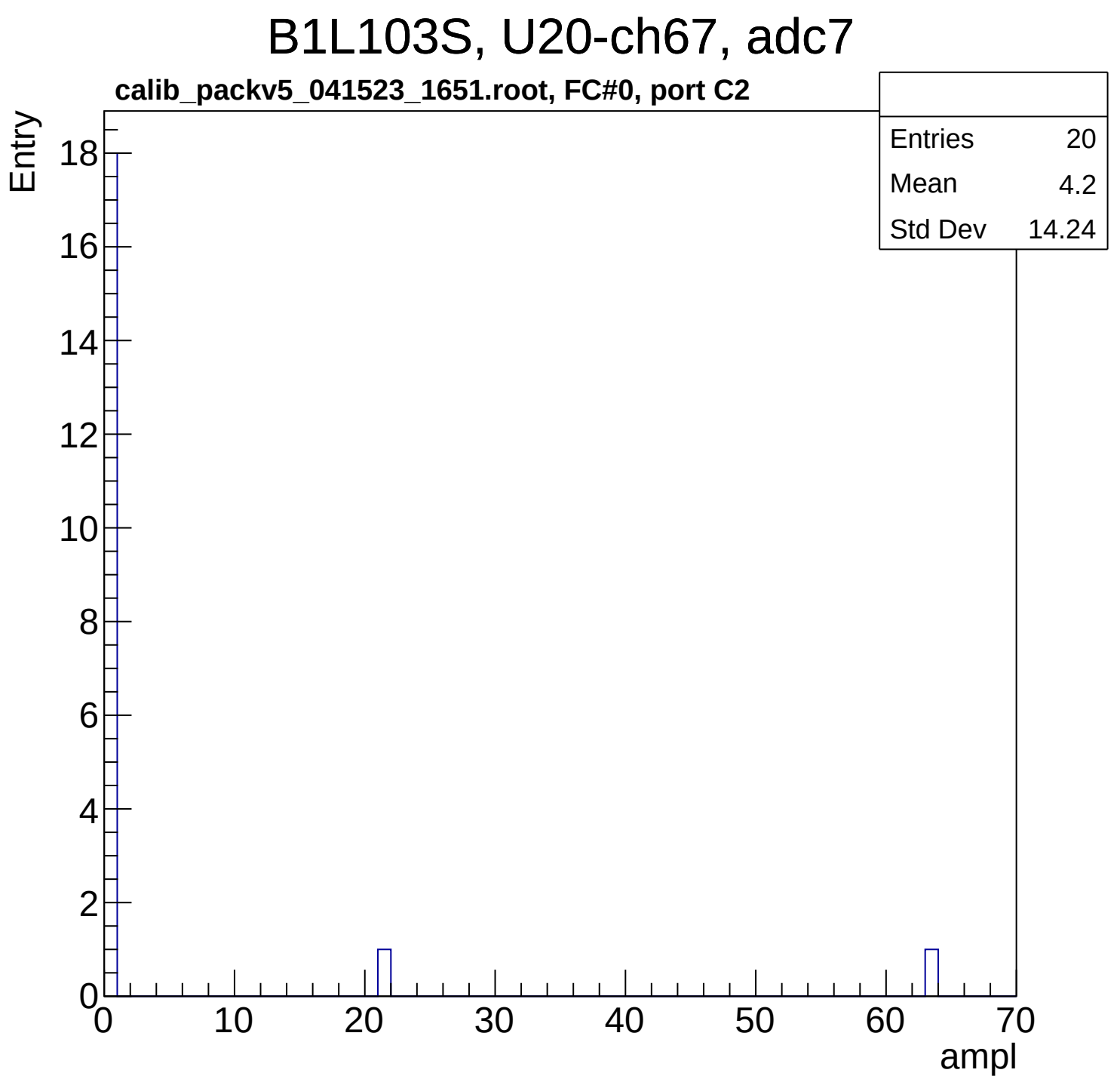
B1L103S, U20-ch67, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4.2
Std Dev 14.24
Entry
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4
6
8
10
12
14
16
18
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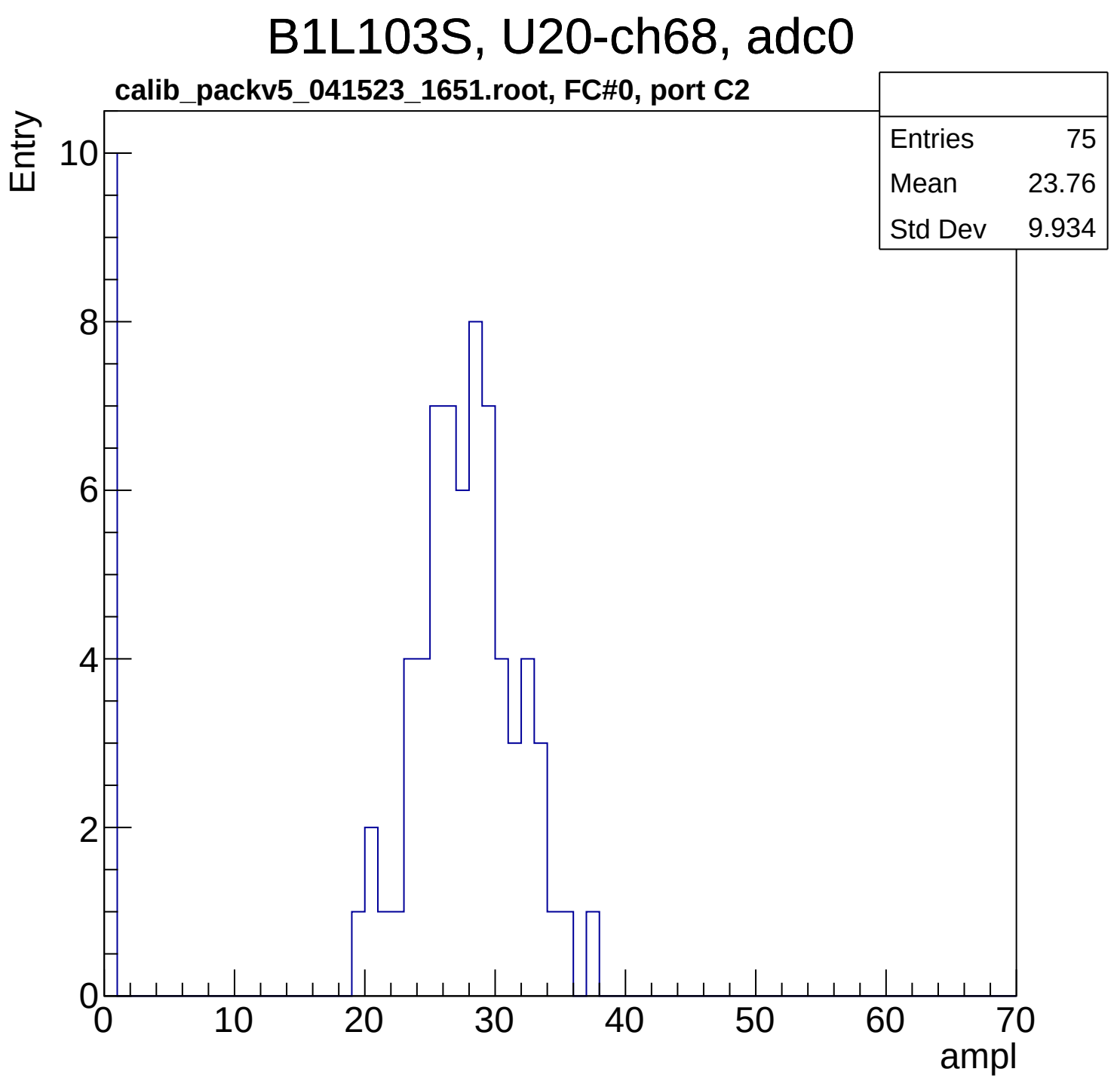
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch68, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 23.76
Std Dev 9.934
Entry
ampl
0
2
4
6
8
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0
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20
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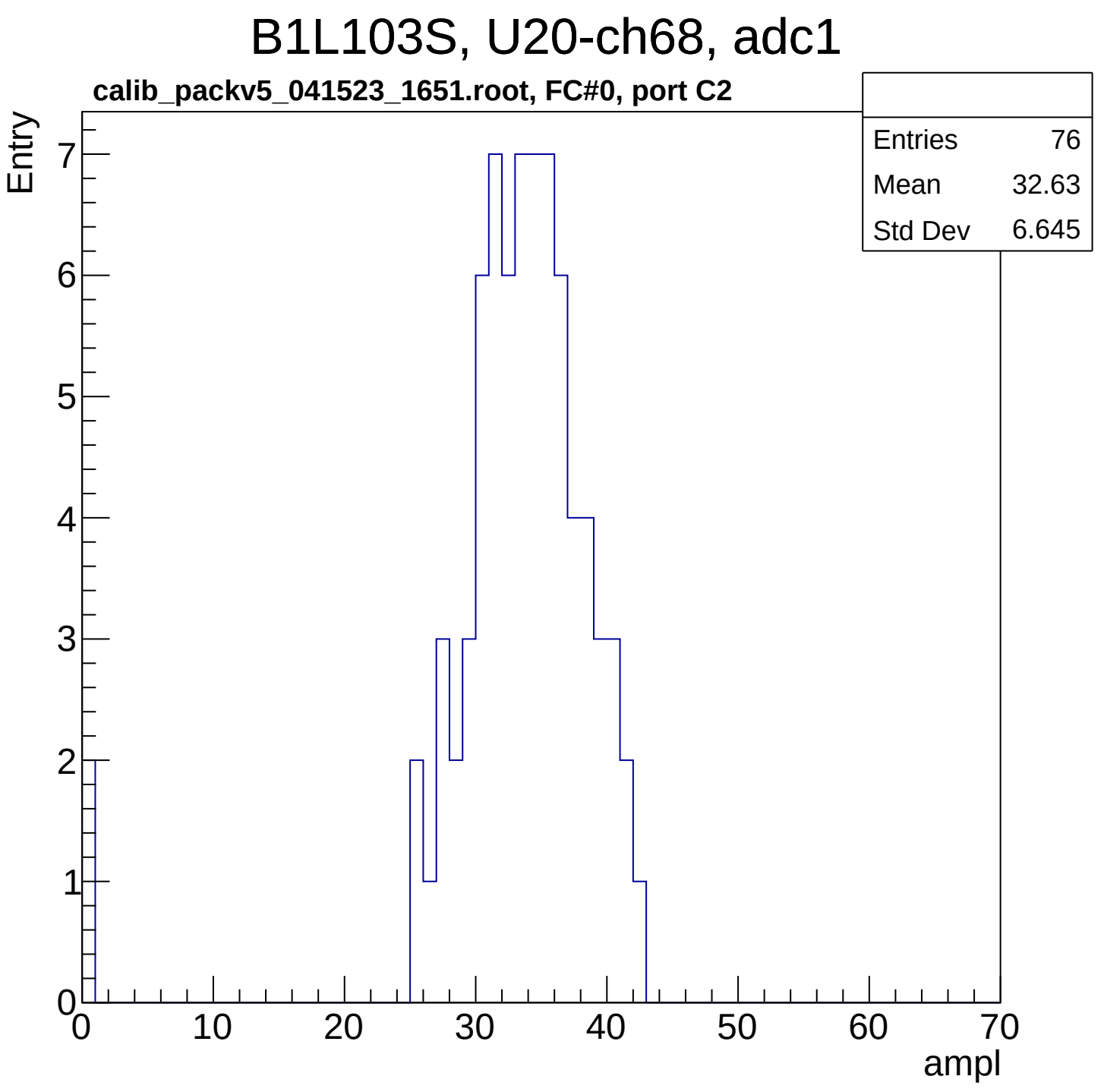
40
50
60
70


B1L103S, U20-ch68, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 32.63
Std Dev 6.645
Entry
ampl
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1
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3
4
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6
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0
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20
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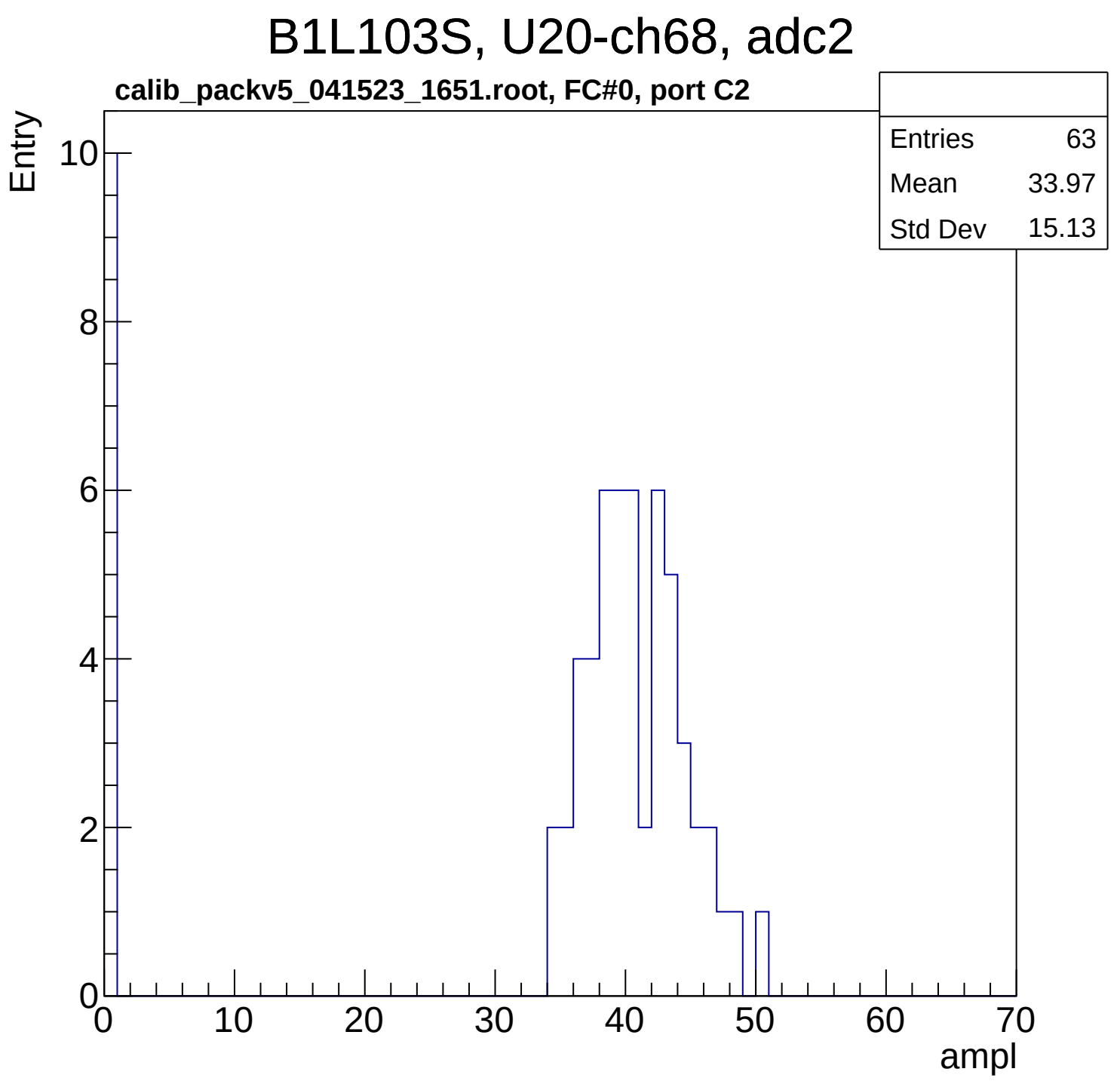
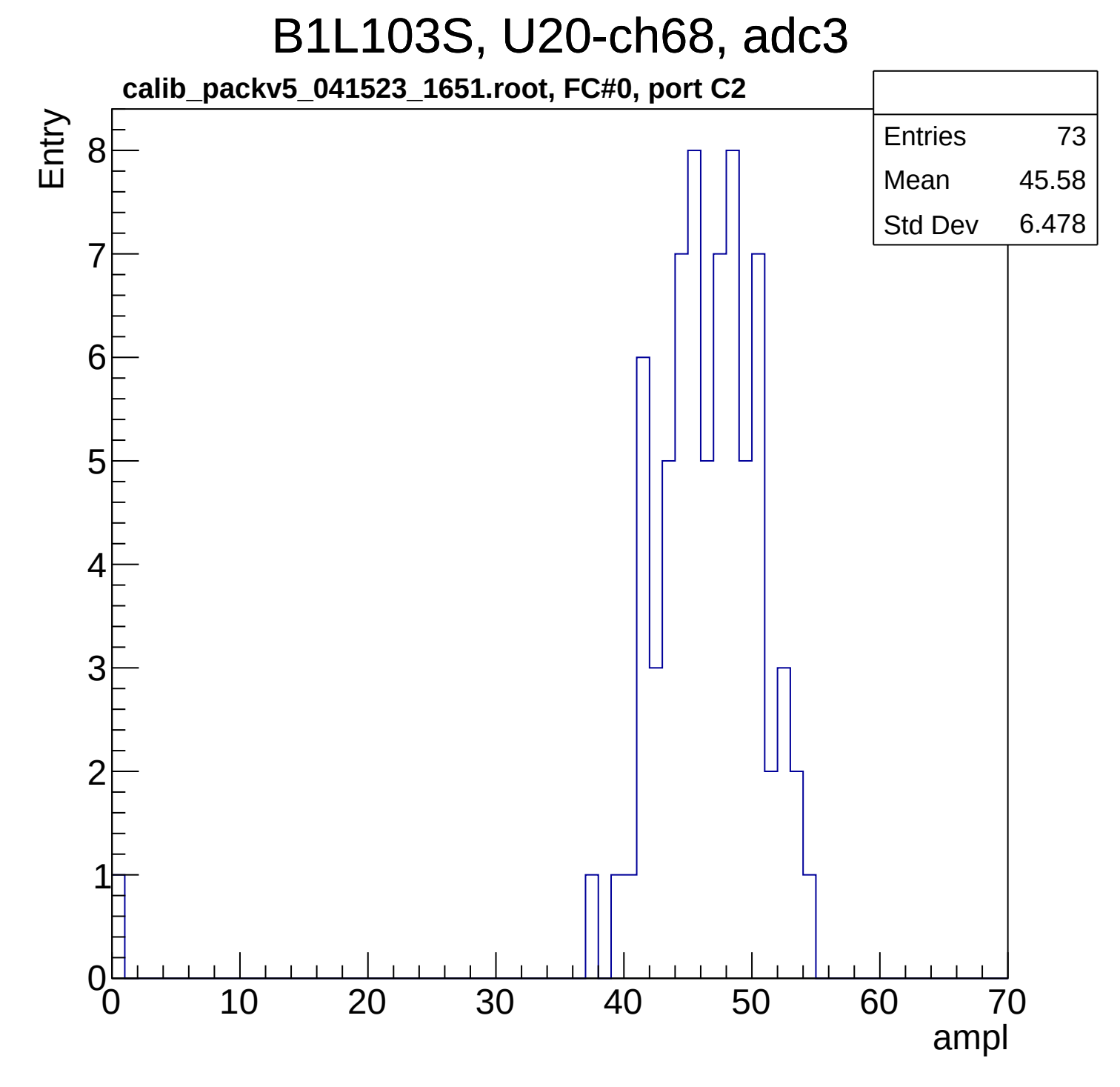
40
50
60
70


B1L103S, U20-ch68, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 33.97
Std Dev 15.13
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch68, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 45.58
Std Dev 6.478
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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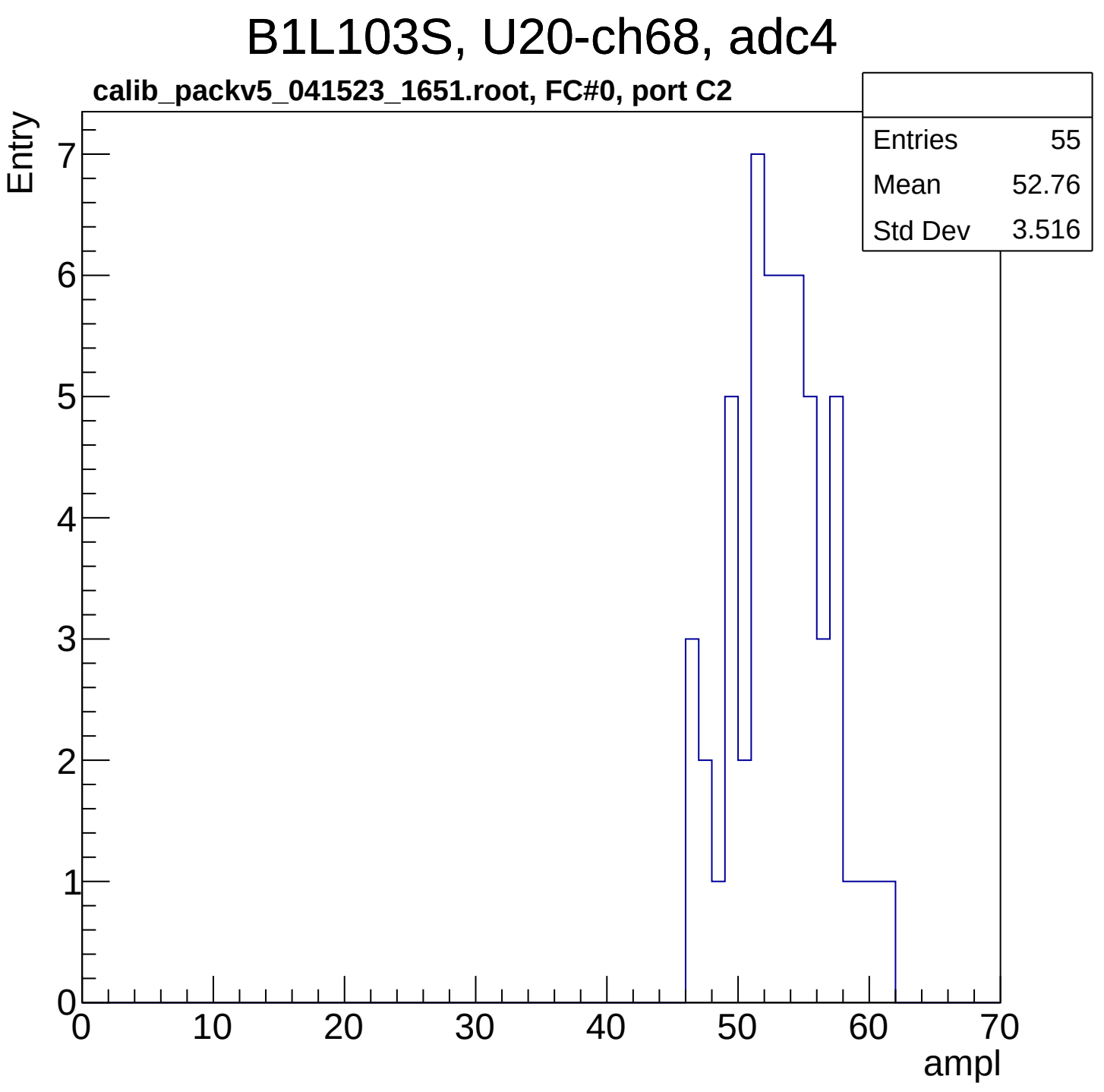
B1L103S, U20-ch68, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 52.76
Std Dev 3.516
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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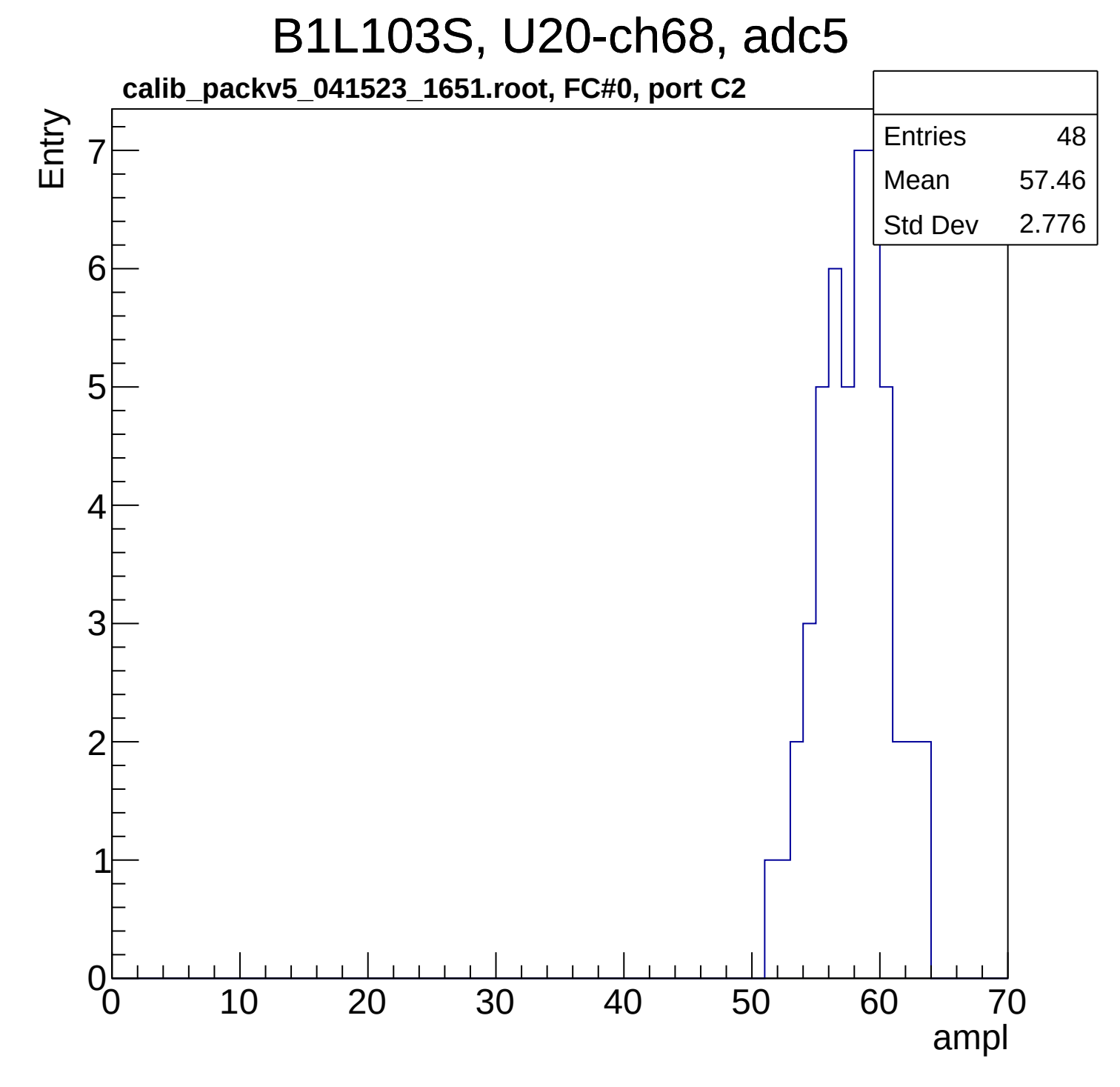
B1L103S, U20-ch68, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 57.46
Std Dev 2.776
Entry
ampl
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4
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6
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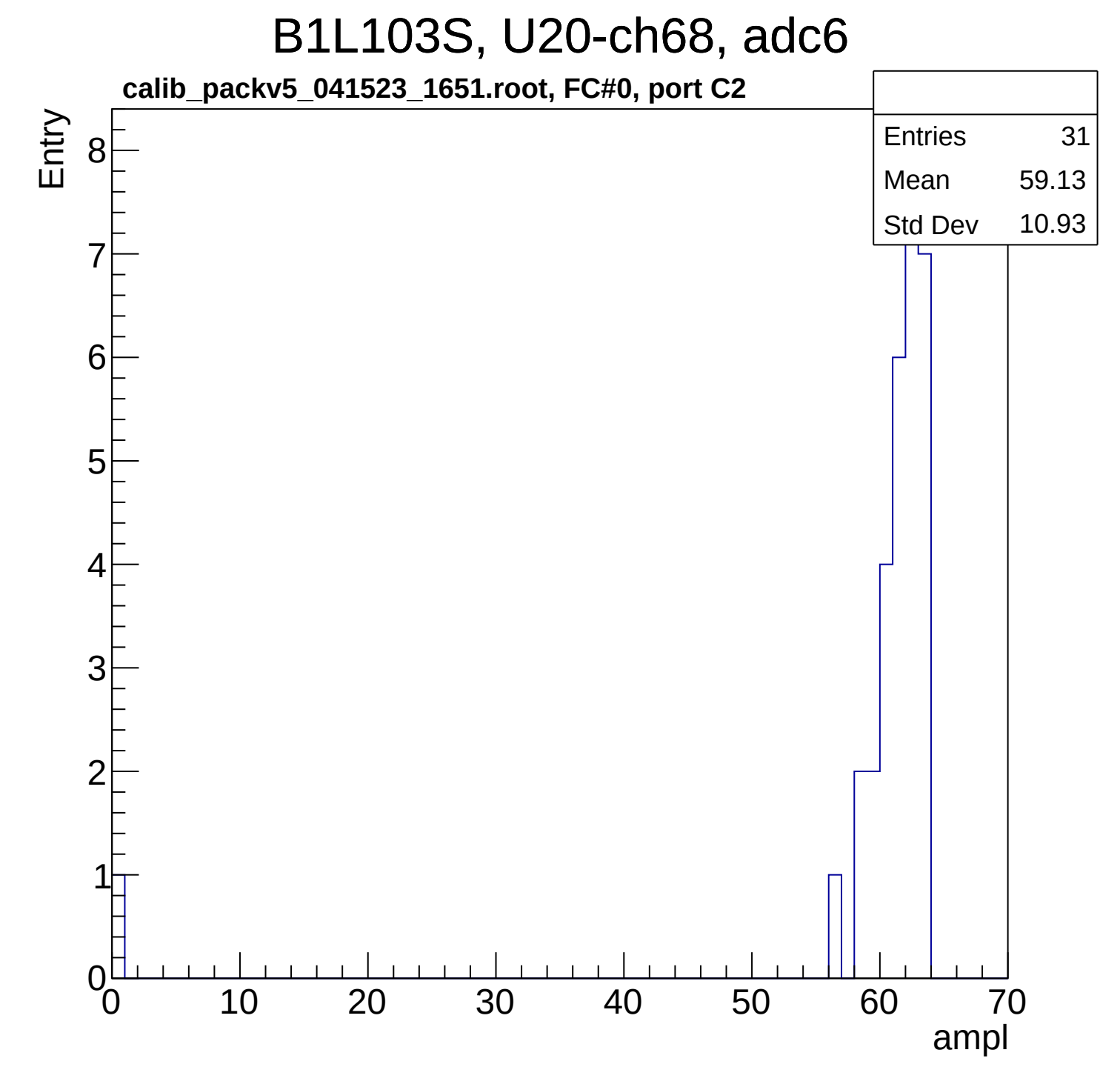
B1L103S, U20-ch68, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 59.13
Std Dev 10.93
Entry
ampl
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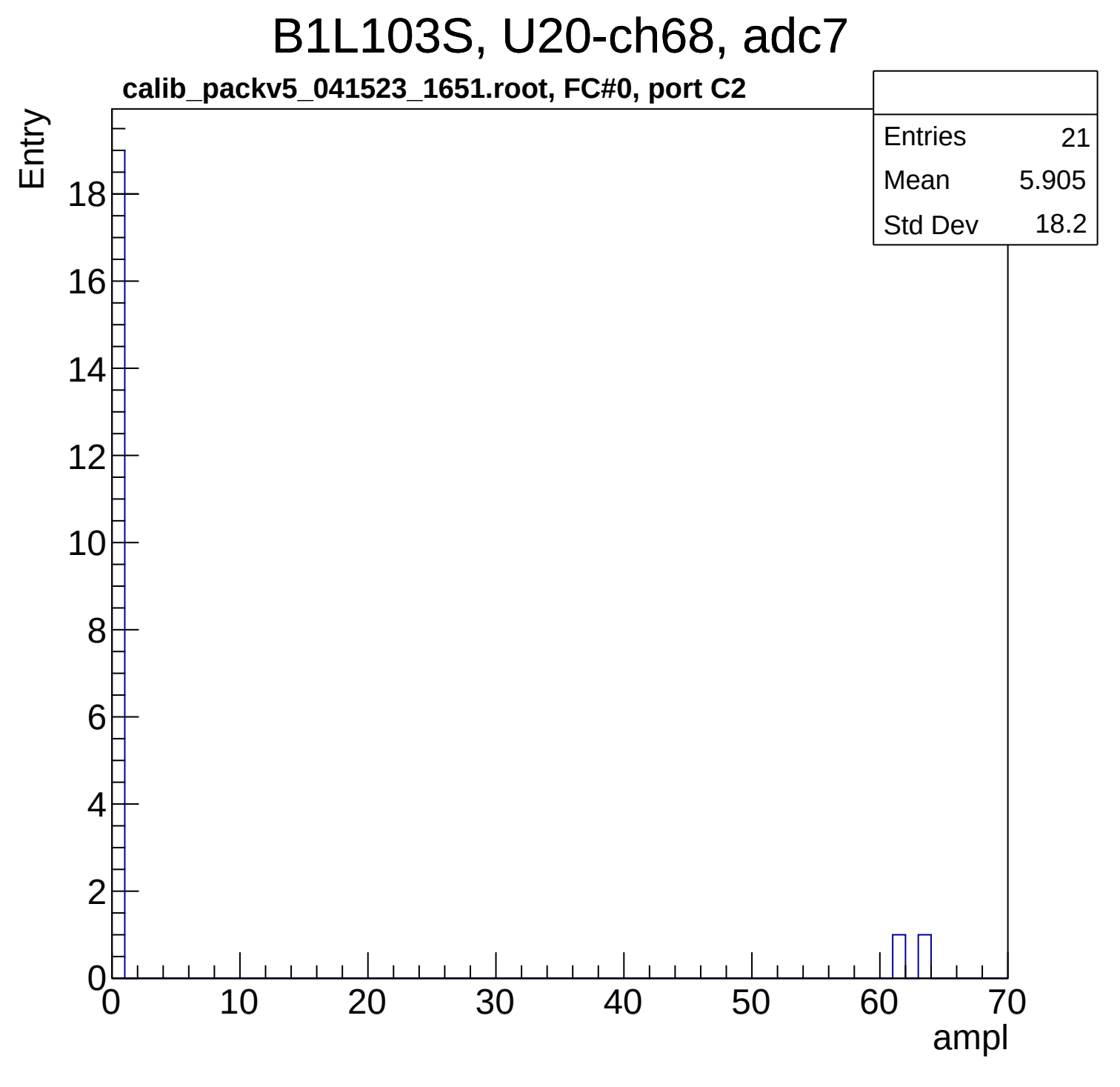
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch68, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.905
Std Dev 18.2
Entry
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6
8
10
12
14
16
18
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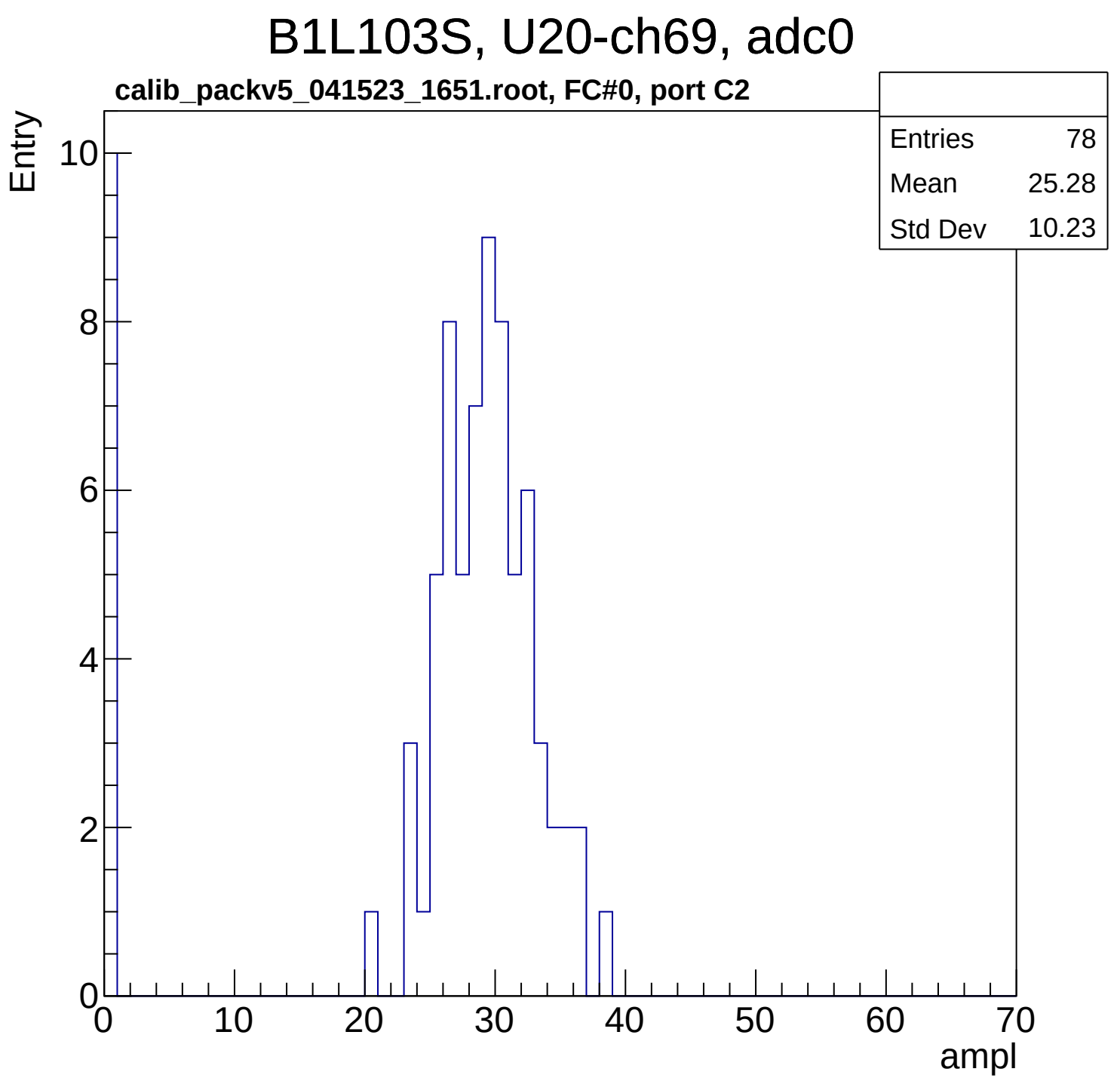
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch69, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 25.28
Std Dev 10.23
Entry
ampl
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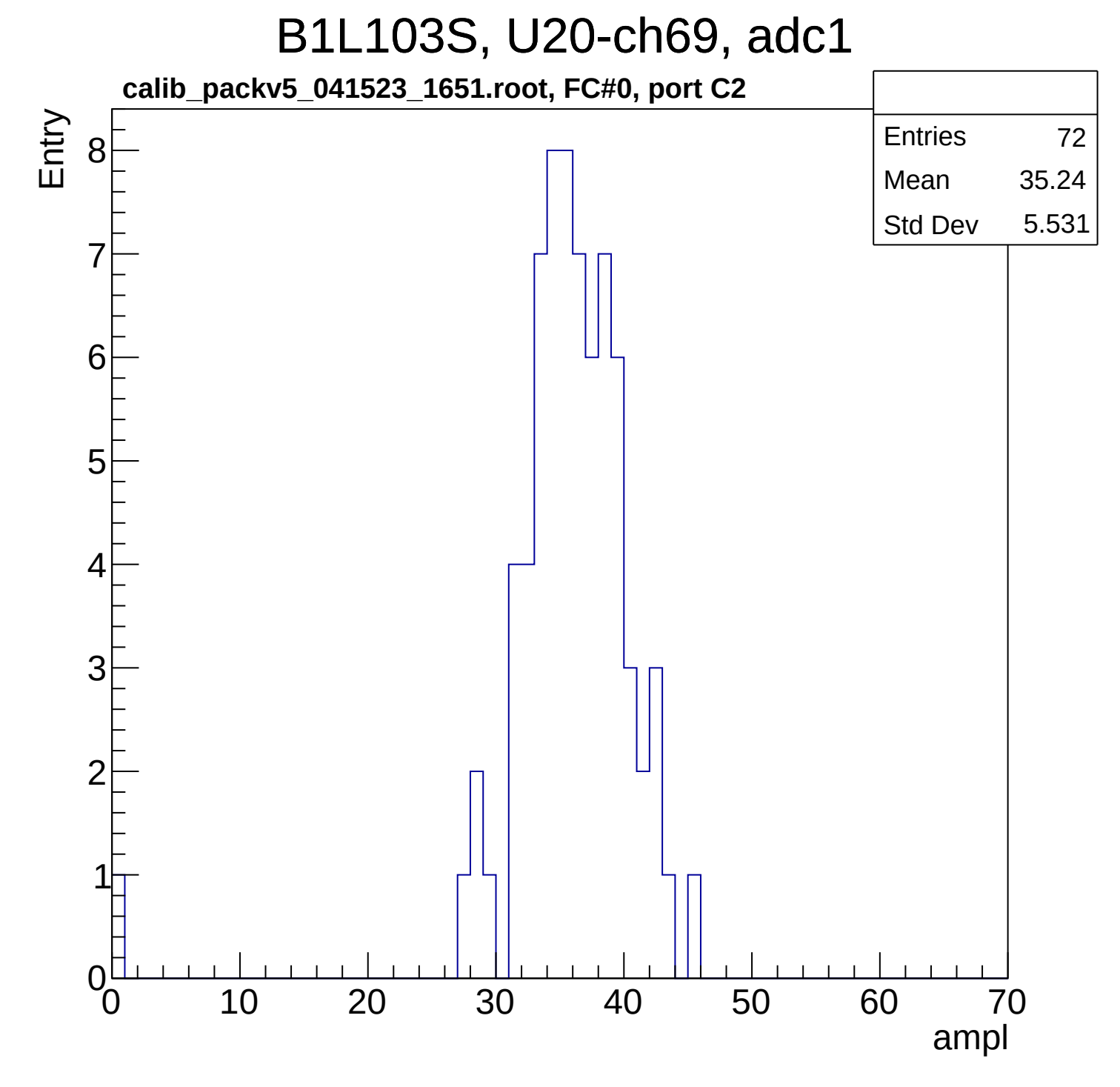
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U20-ch69, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 35.24
Std Dev 5.531
Entry
ampl
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2
3
4
5
6
7
8
0
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50
60
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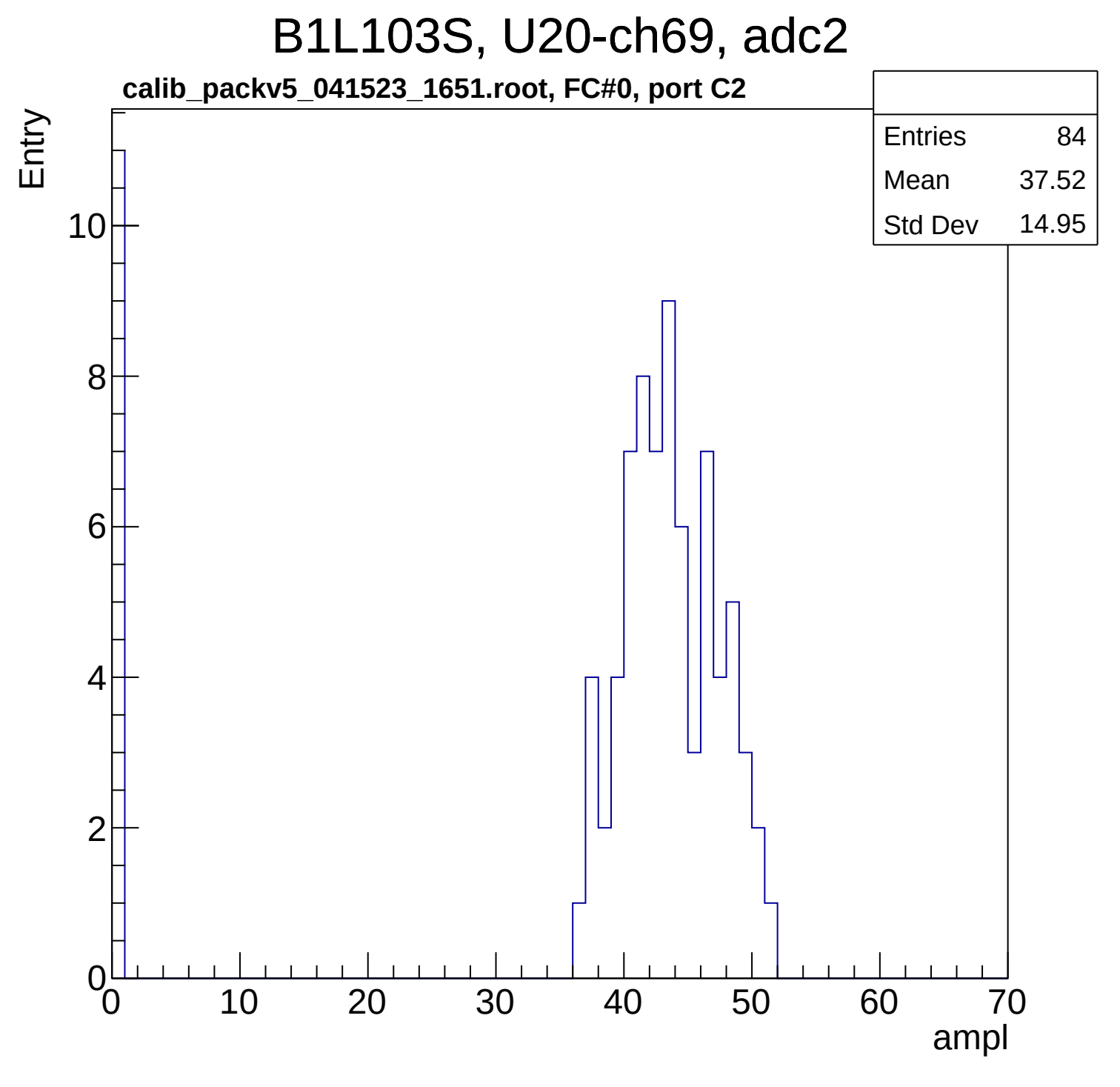
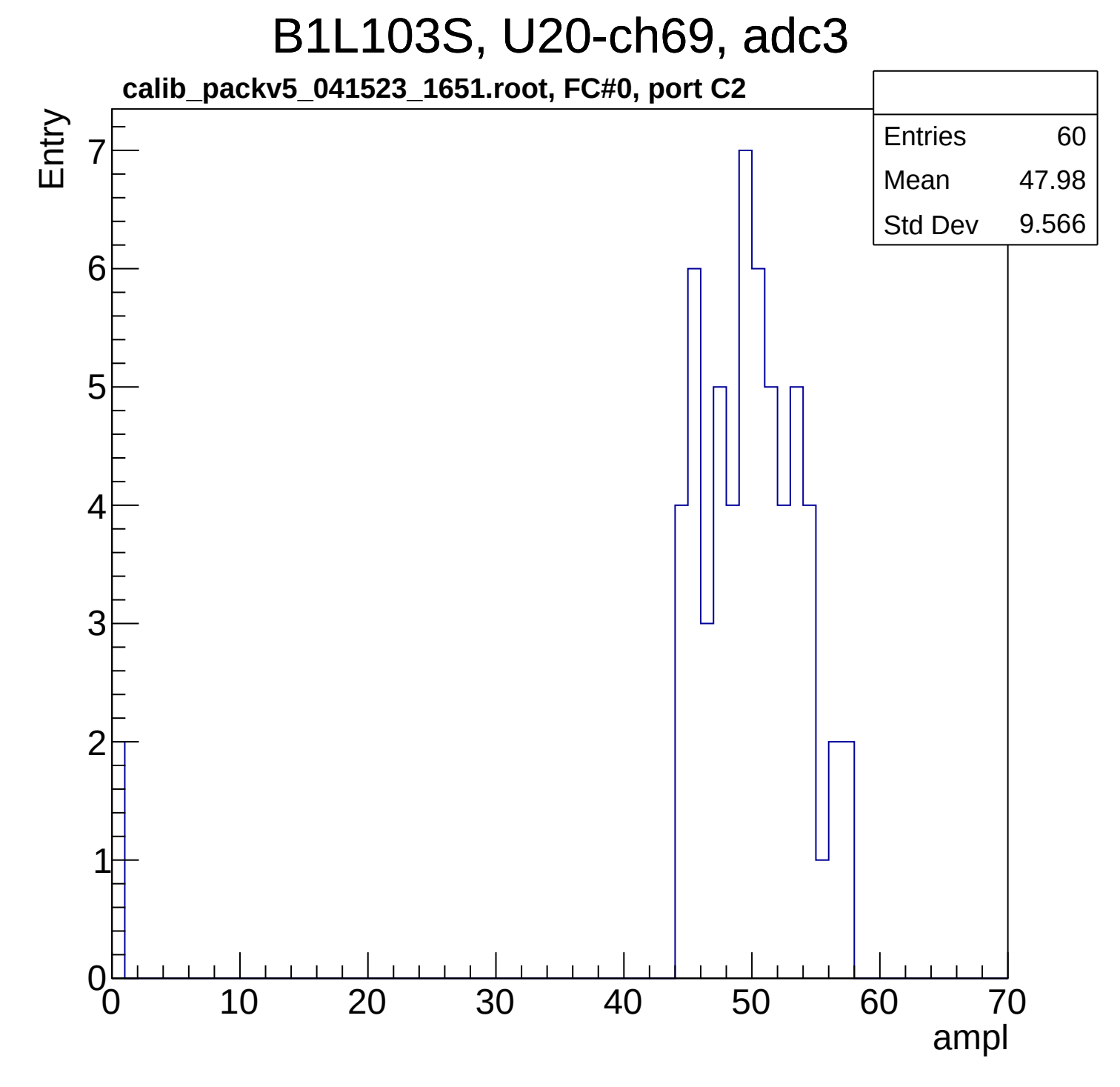
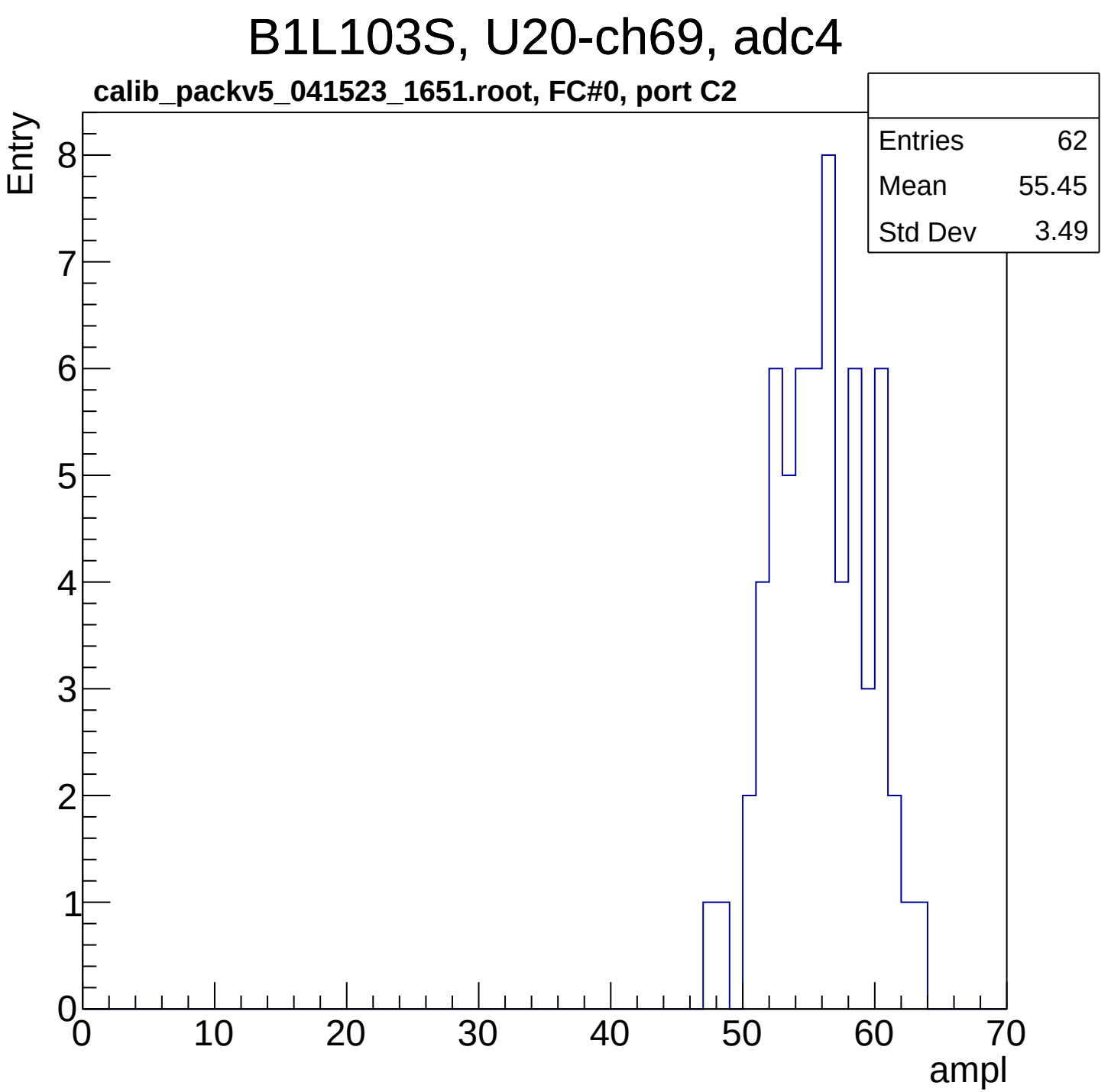

B1L103S, U20-ch69, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 37.52
Std Dev 14.95
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch69, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 47.98
Std Dev 9.566
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U20-ch69, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 55.45
Std Dev 3.49
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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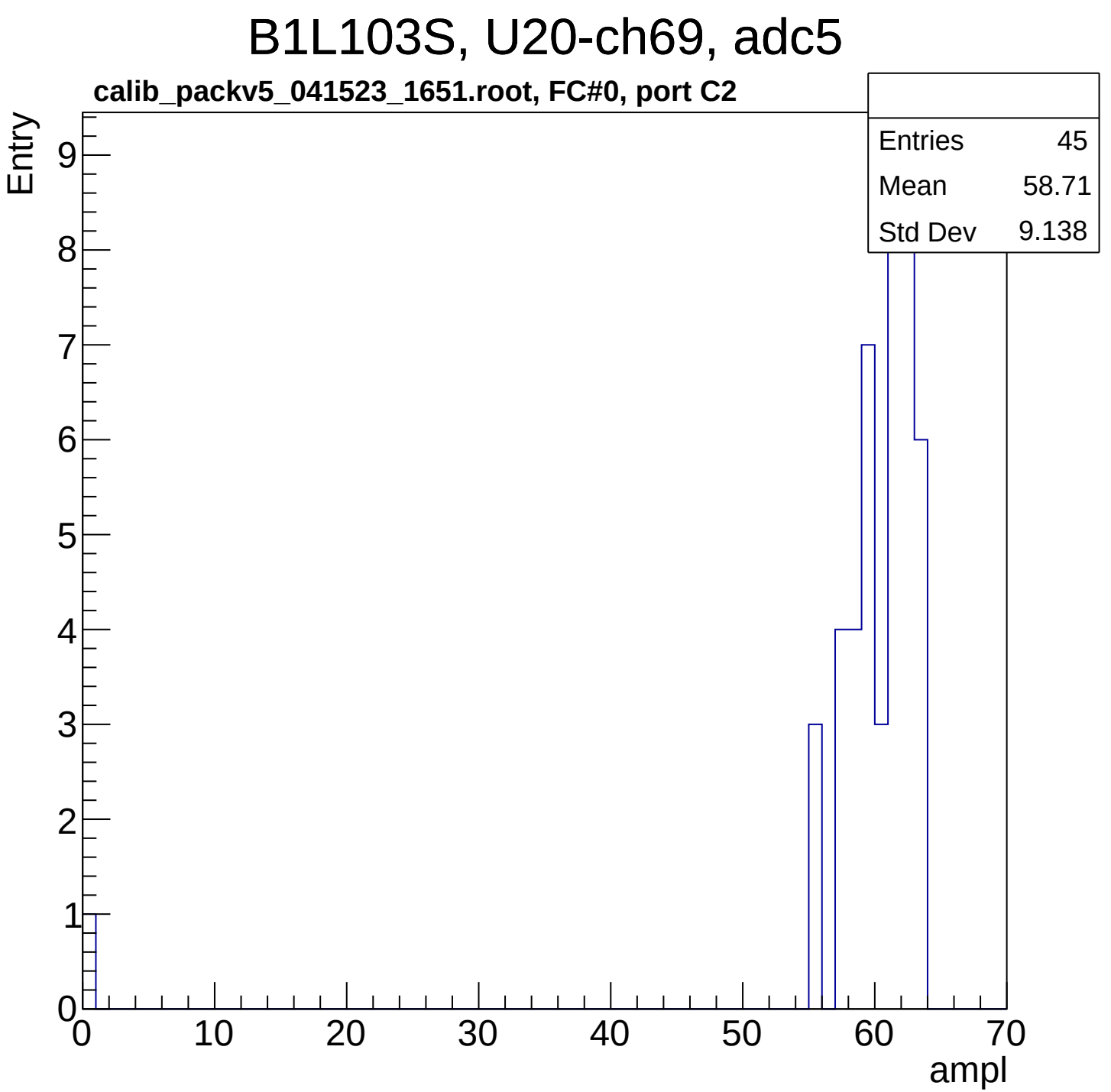
B1L103S, U20-ch69, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 58.71
Std Dev 9.138
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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60
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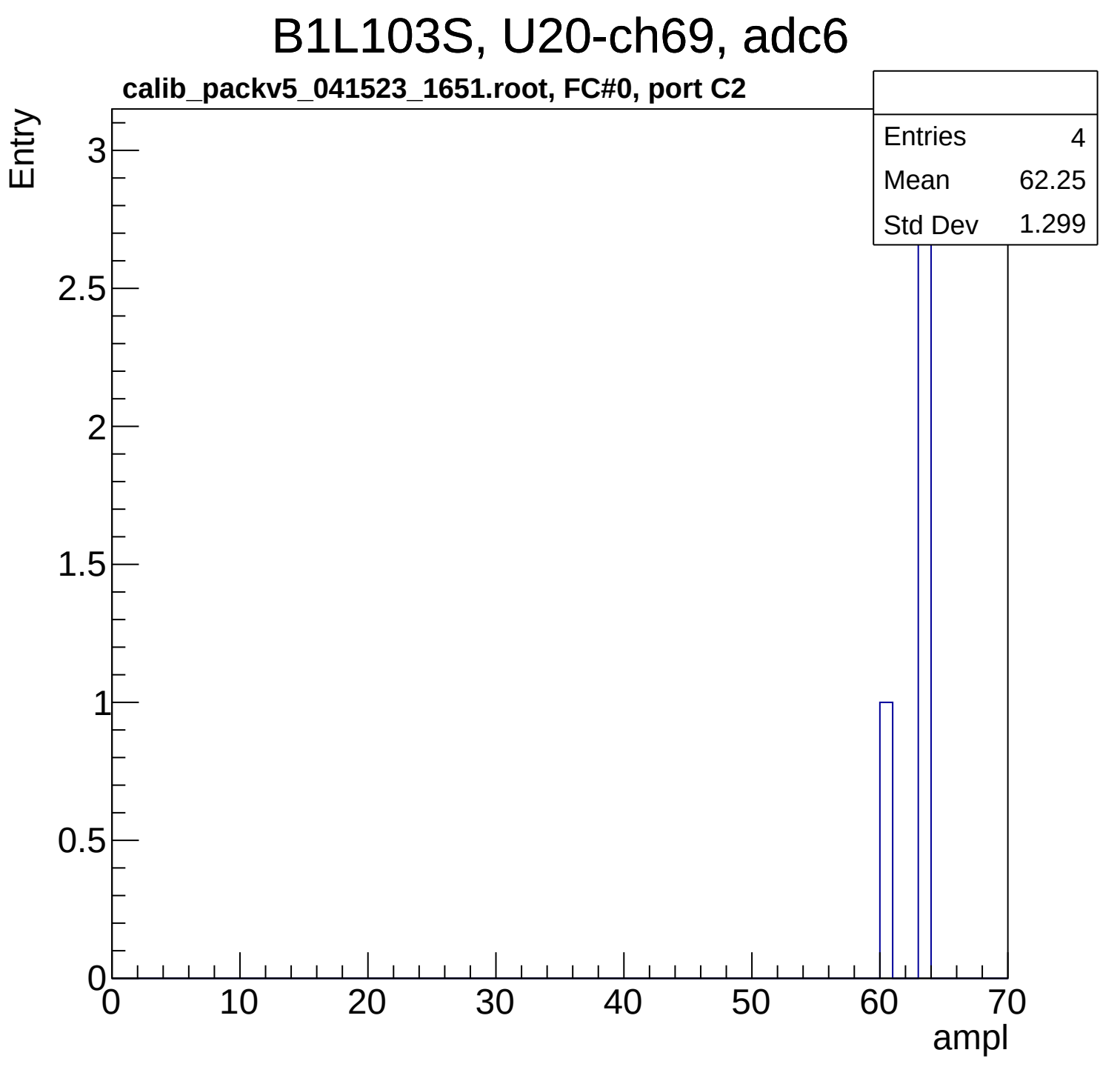
B1L103S, U20-ch69, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 62.25
Std Dev 1.299
Entry
ampl
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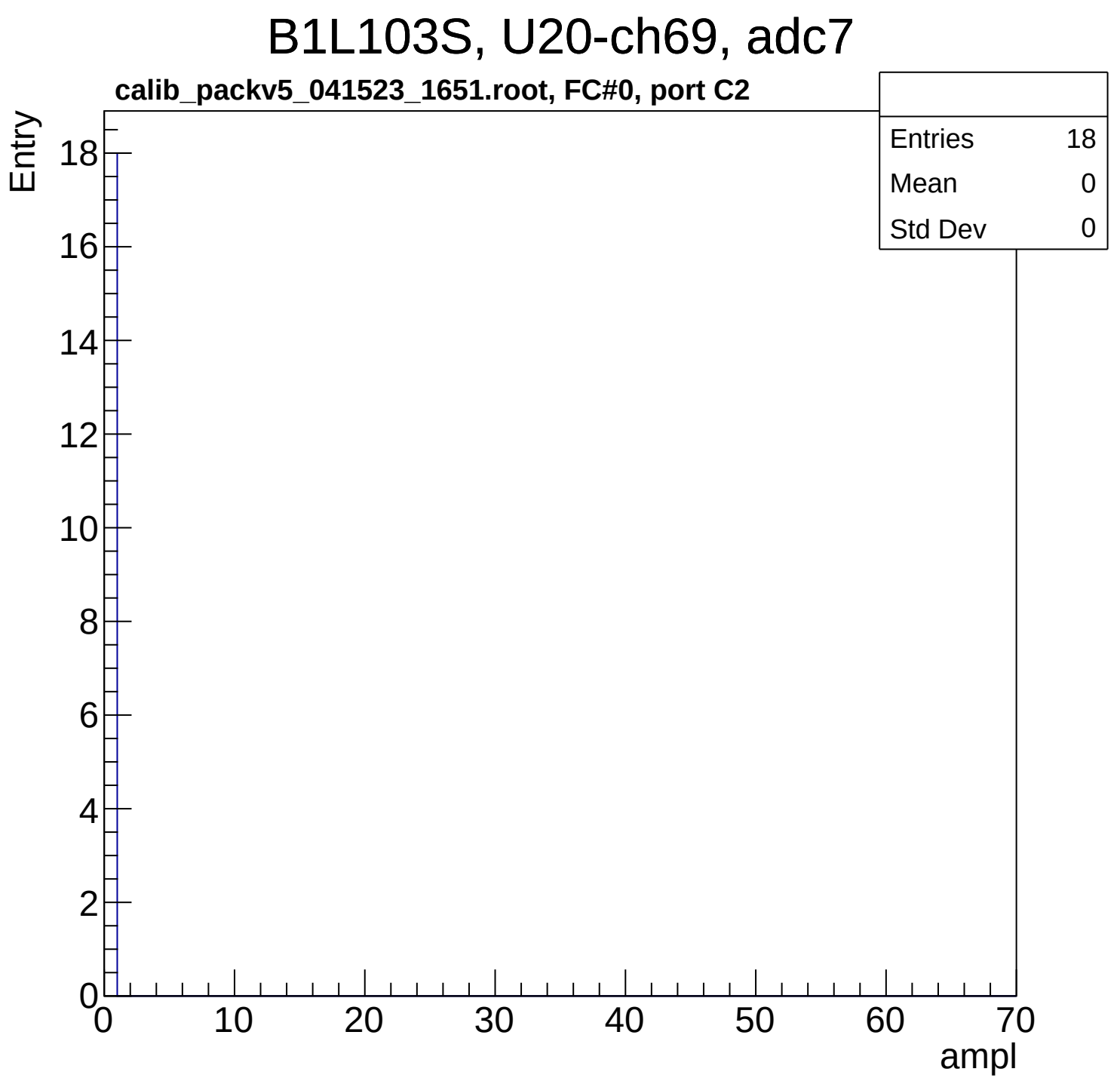
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U20-ch69, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
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2
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6
8
10
12
14
16
18
0
10
20
30
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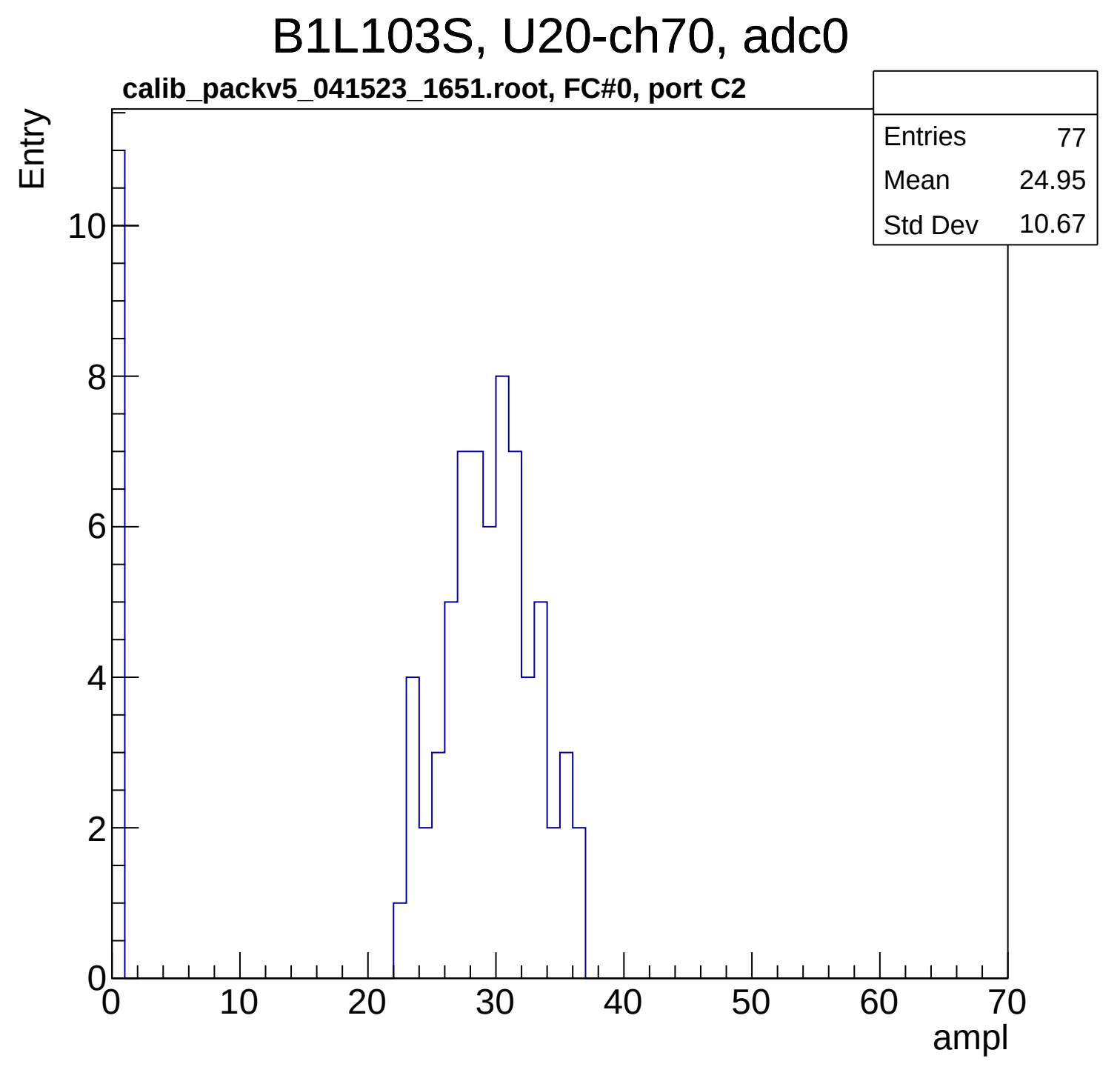
50
60
70
ampl


B1L103S, U20-ch70, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 24.95
Std Dev 10.67
Entry
0
2
4
6
8
10
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20
30
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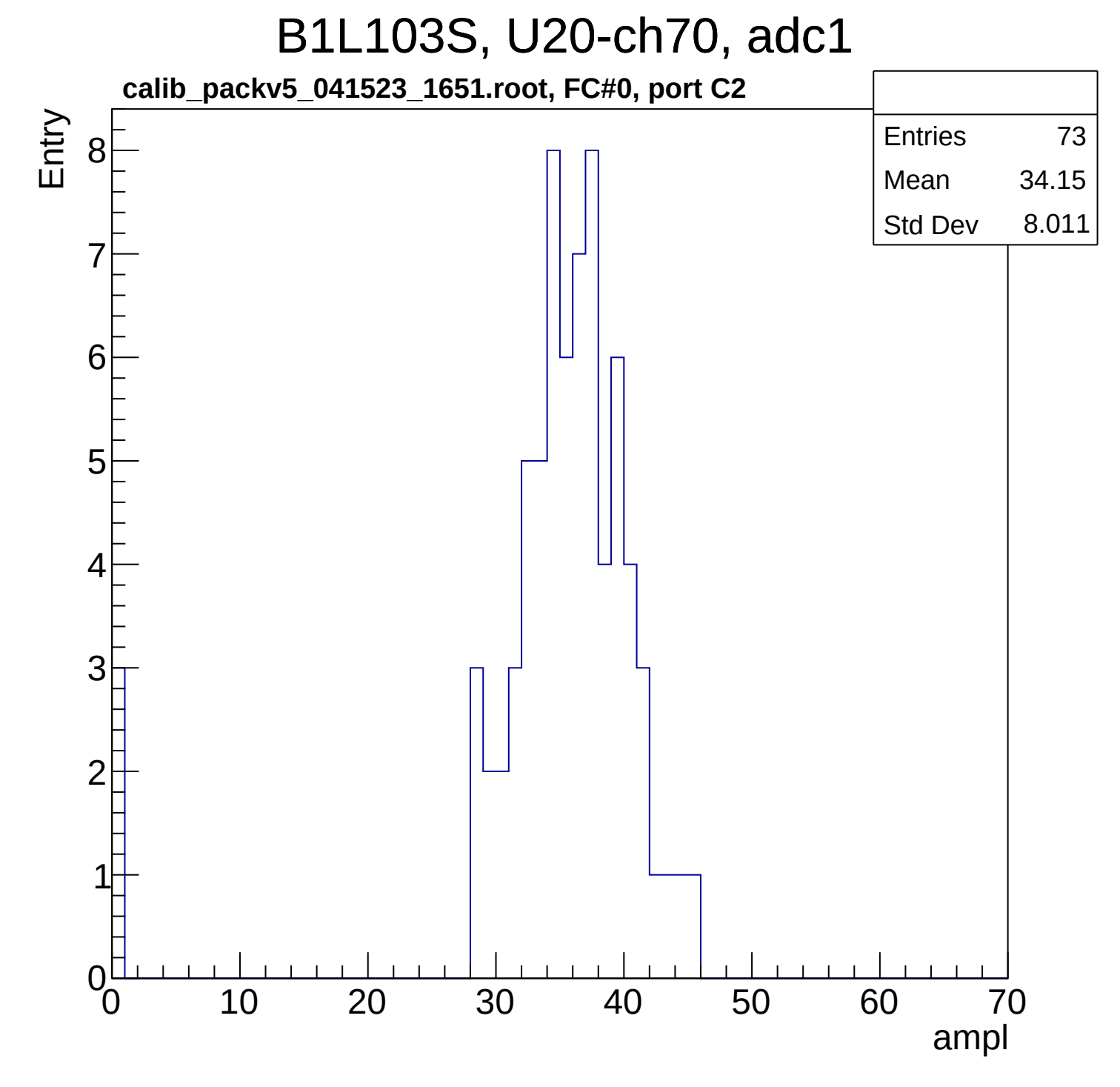
50
60
70
ampl


B1L103S, U20-ch70, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 34.15
Std Dev 8.011
Entry
ampl
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2
3
4
5
6
7
8
0
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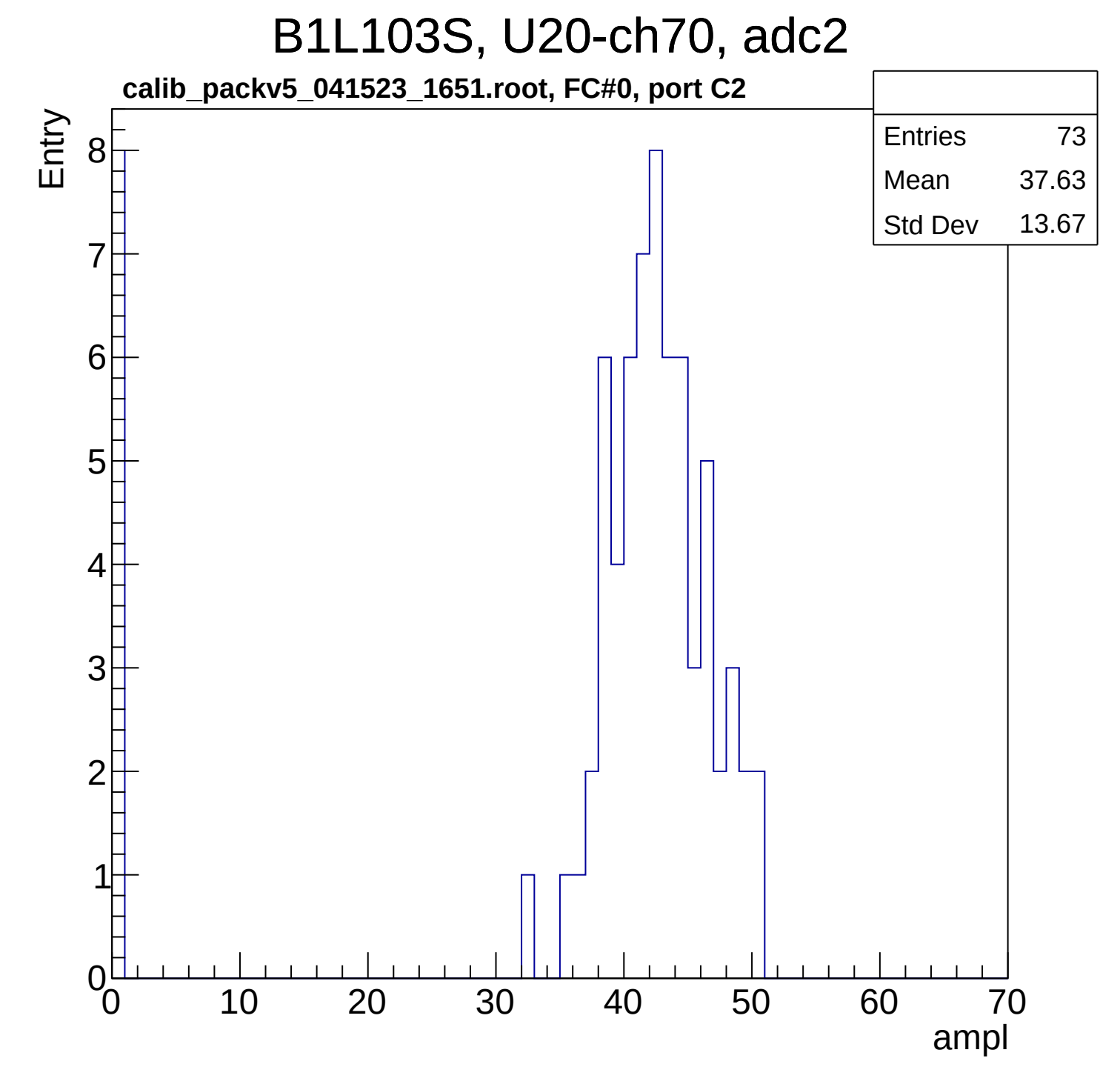
B1L103S, U20-ch70, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 37.63
Std Dev 13.67
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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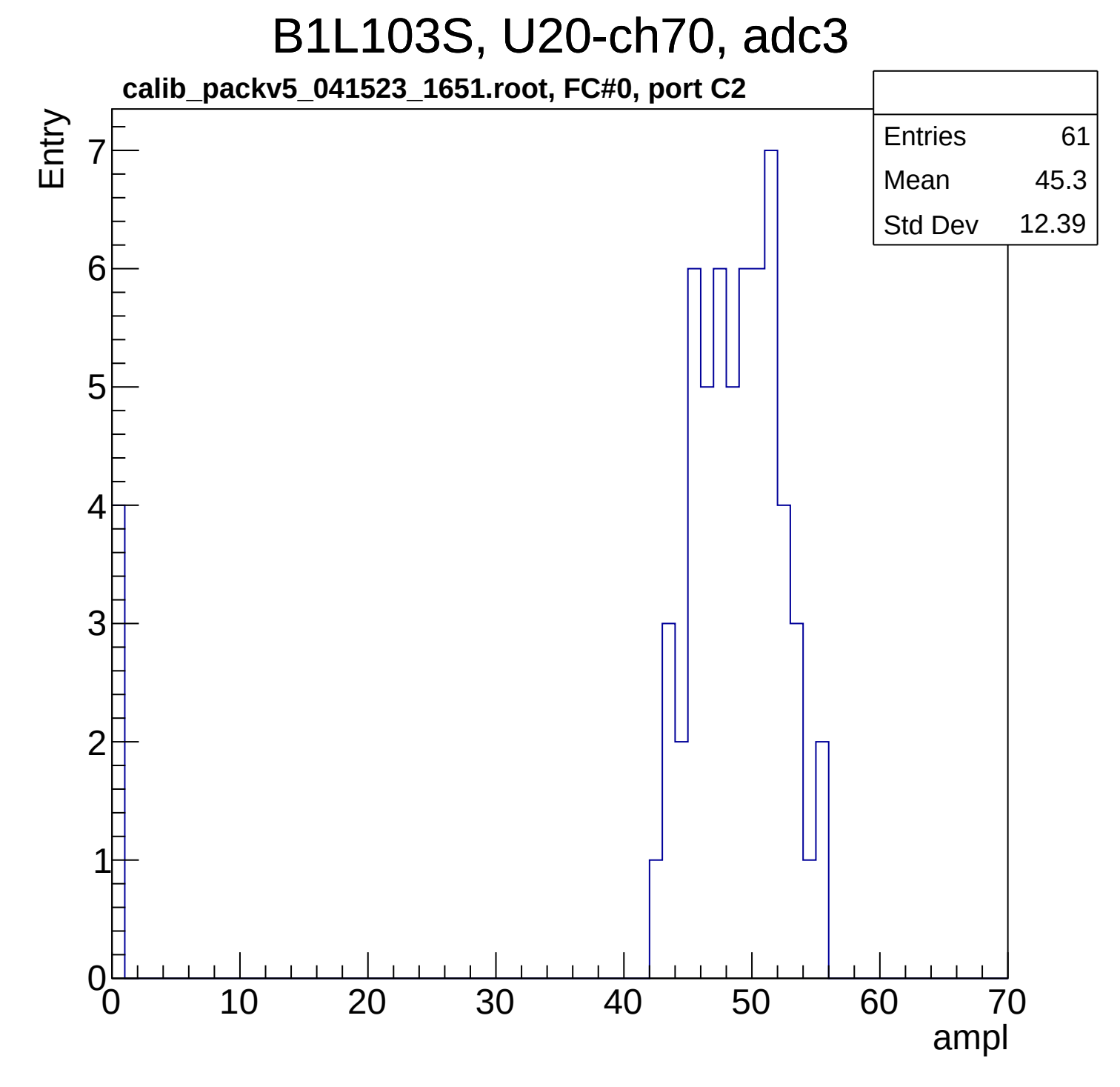
40
50
60
70


B1L103S, U20-ch70, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 45.3
Std Dev 12.39
Entry
ampl
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3
4
5
6
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0
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20
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40
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60
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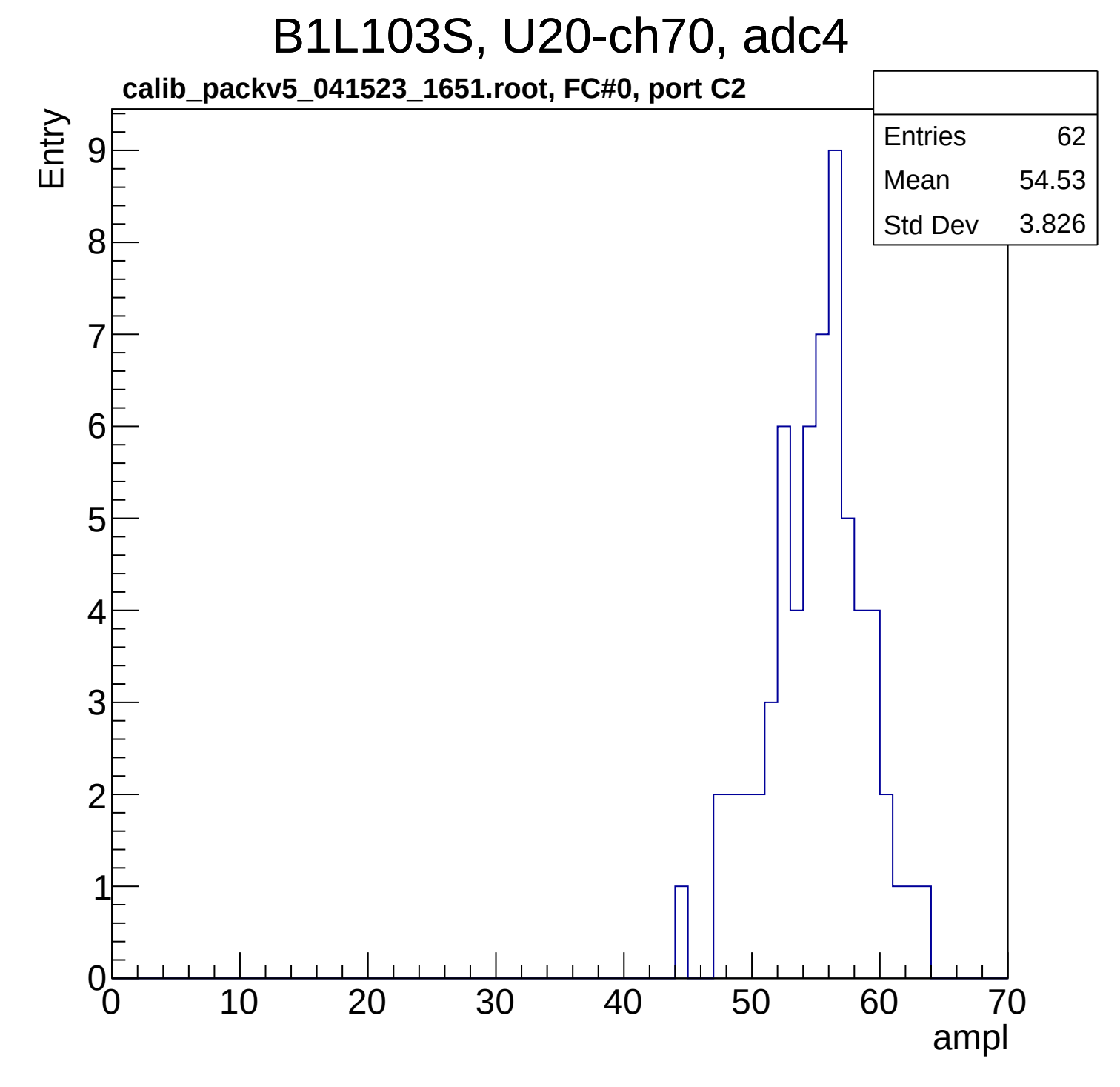
B1L103S, U20-ch70, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 54.53
Std Dev 3.826
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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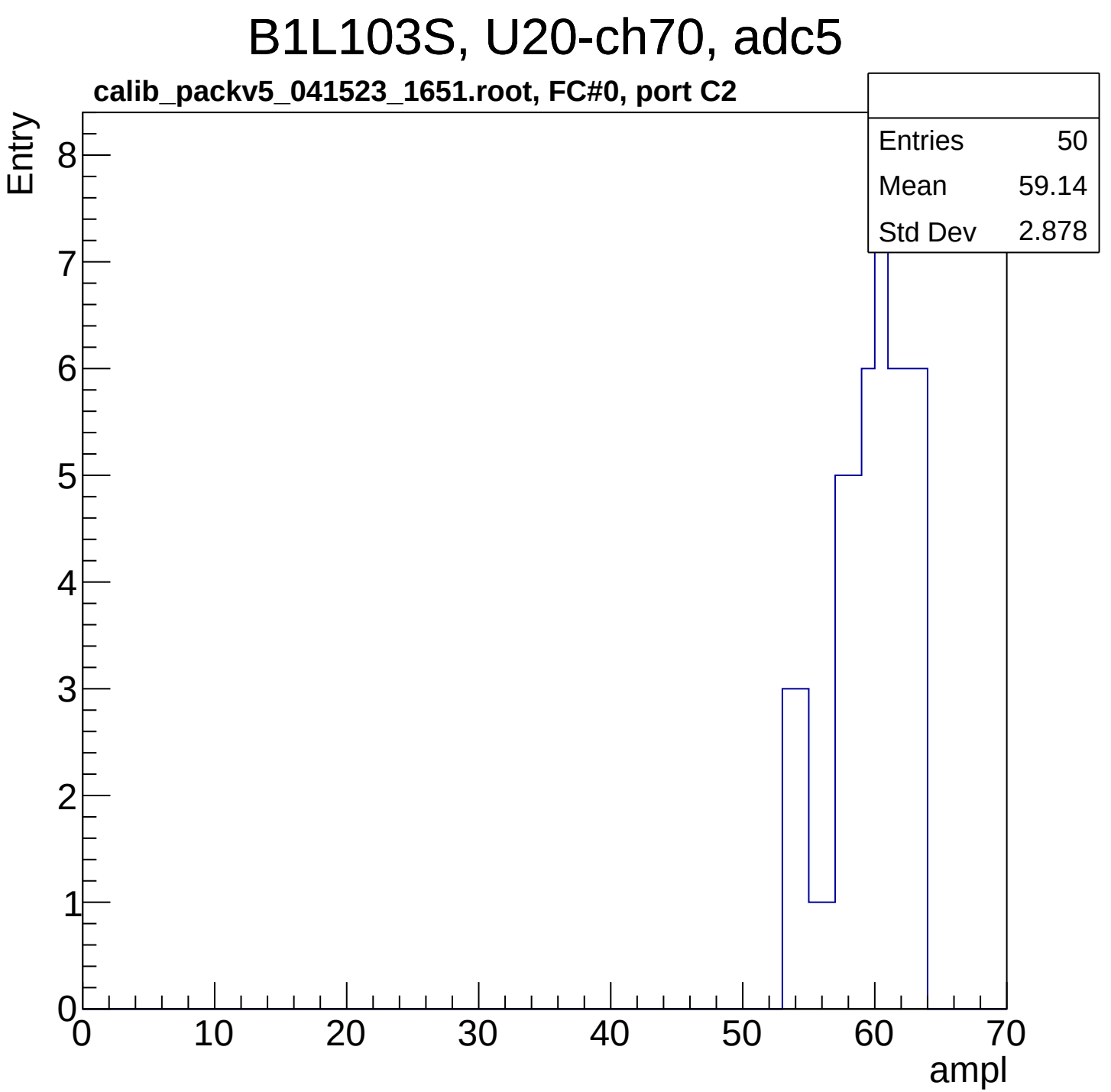
40
50
60
70


B1L103S, U20-ch70, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 59.14
Std Dev 2.878
Entry
ampl
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1
2
3
4
5
6
7
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0
10
20
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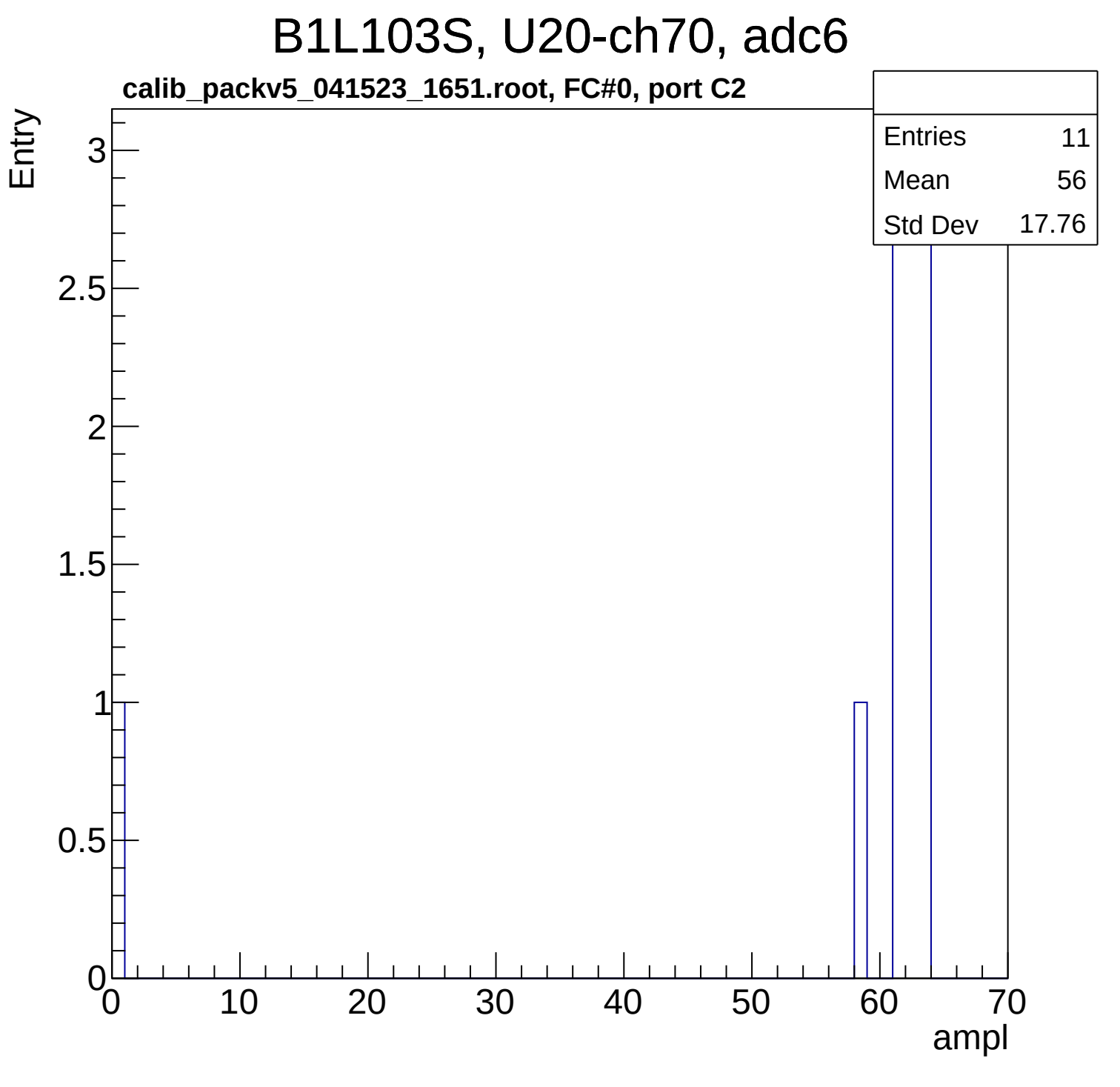
40
50
60
70


B1L103S, U20-ch70, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 56
Std Dev 17.76
Entry
ampl
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1.5
2
2.5
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0
10
20
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40
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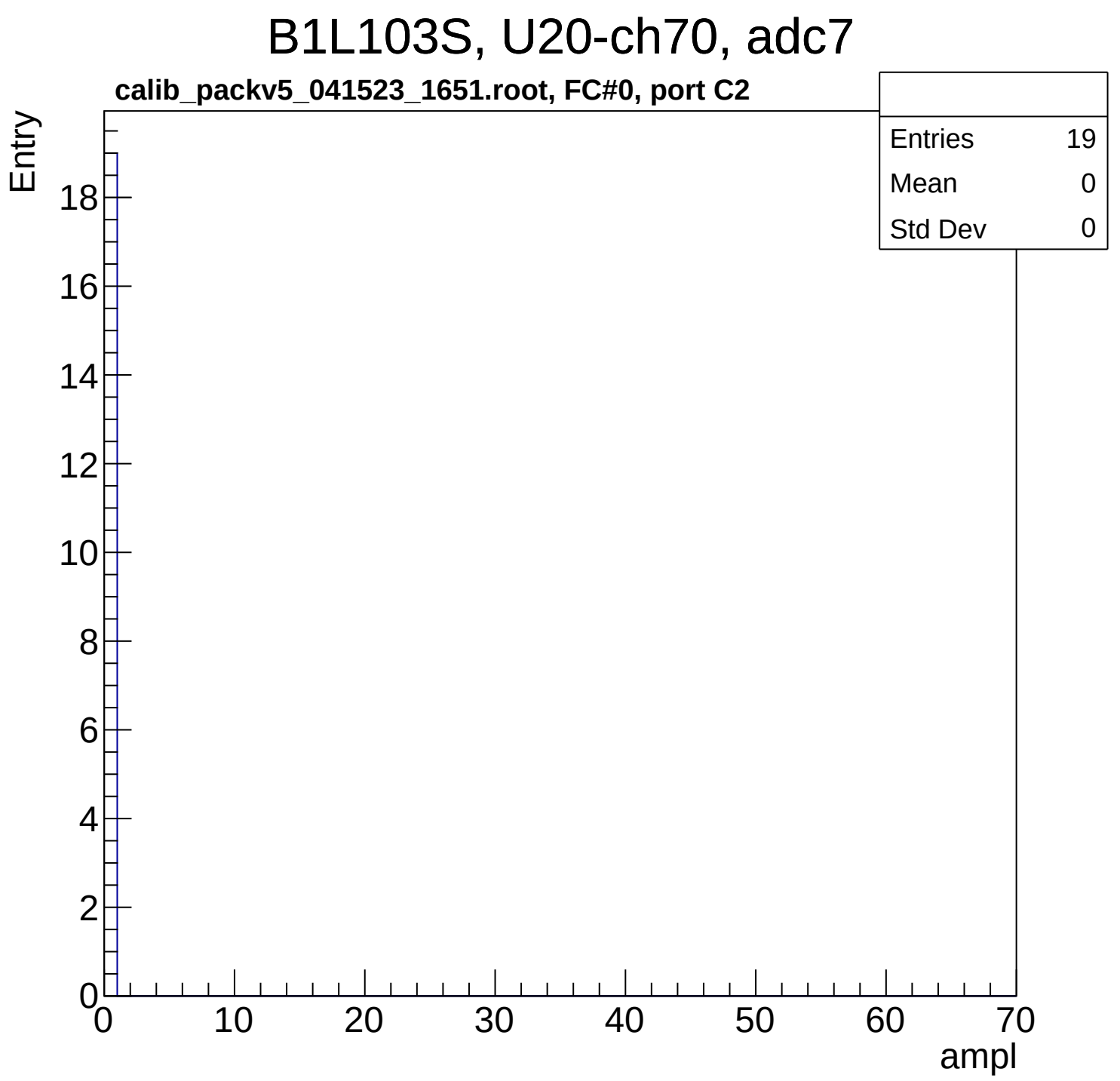
60
70


B1L103S, U20-ch70, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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2
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6
8
10
12
14
16
18
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30
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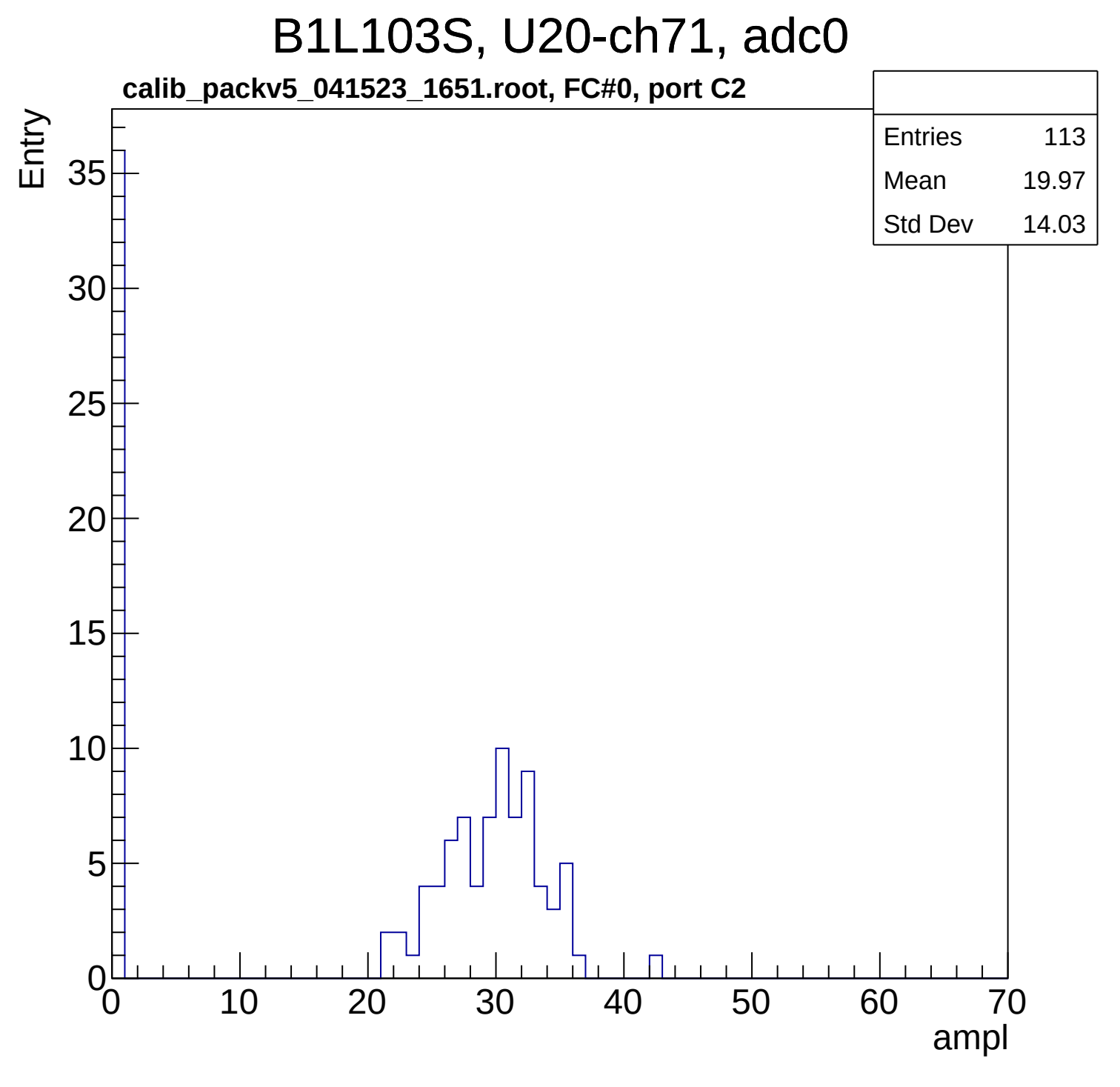
50
60
70
ampl


B1L103S, U20-ch71, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 113
Mean 19.97
Std Dev 14.03
Entry
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5
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15
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25
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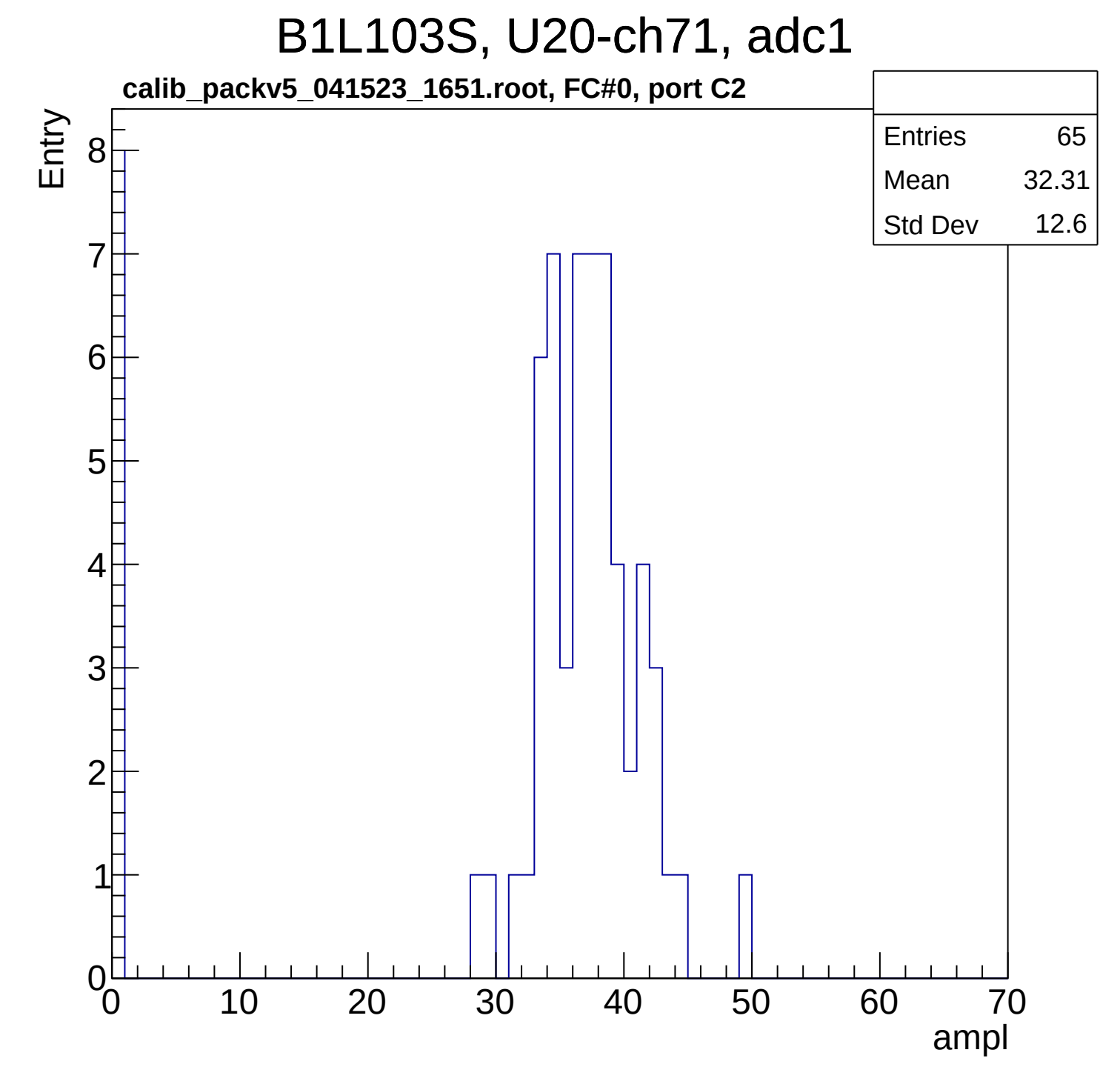
60
70
ampl


B1L103S, U20-ch71, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 32.31
Std Dev 12.6
Entry
ampl
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1
2
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4
5
6
7
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0
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40
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60
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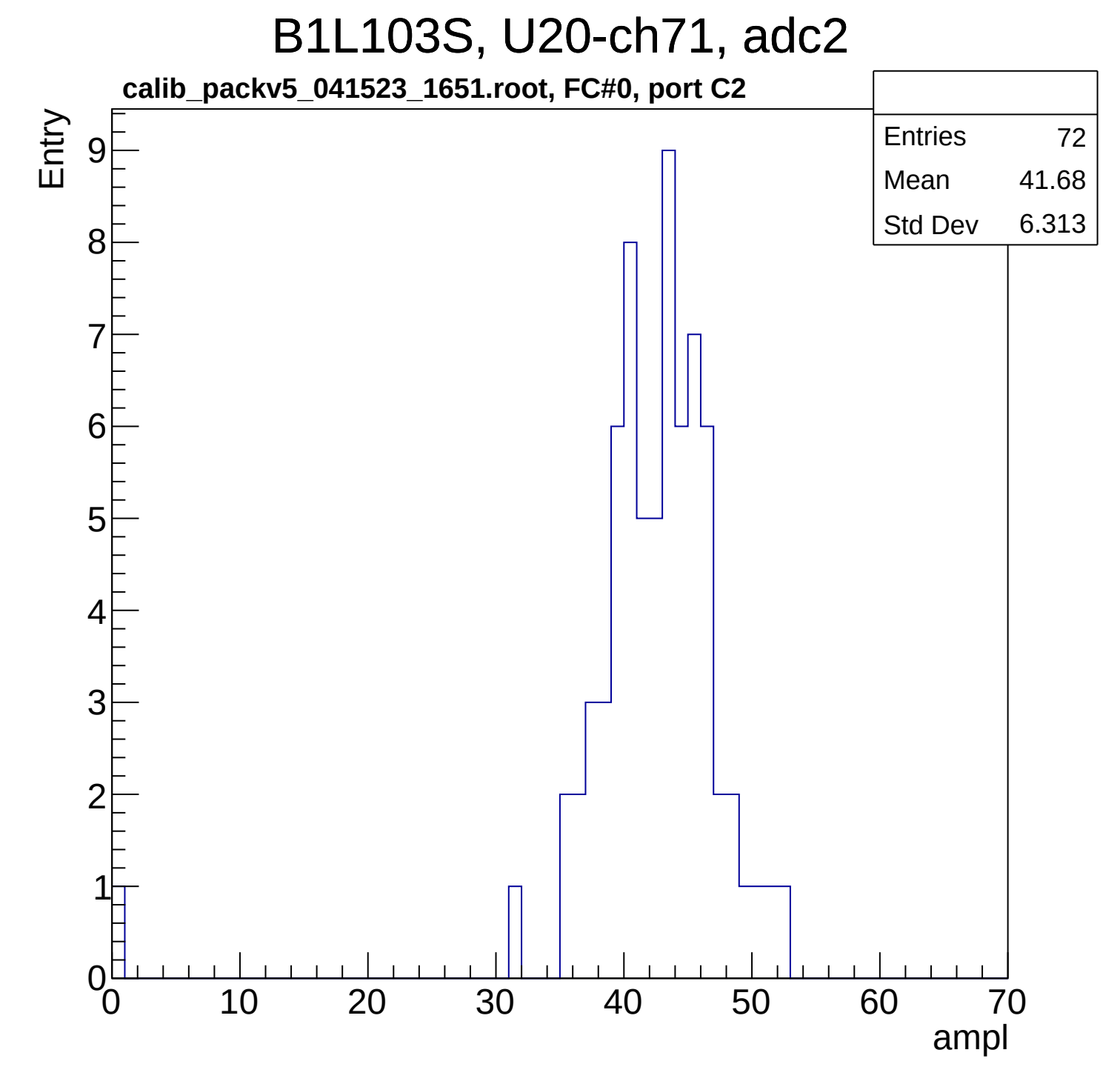
B1L103S, U20-ch71, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 41.68
Std Dev 6.313
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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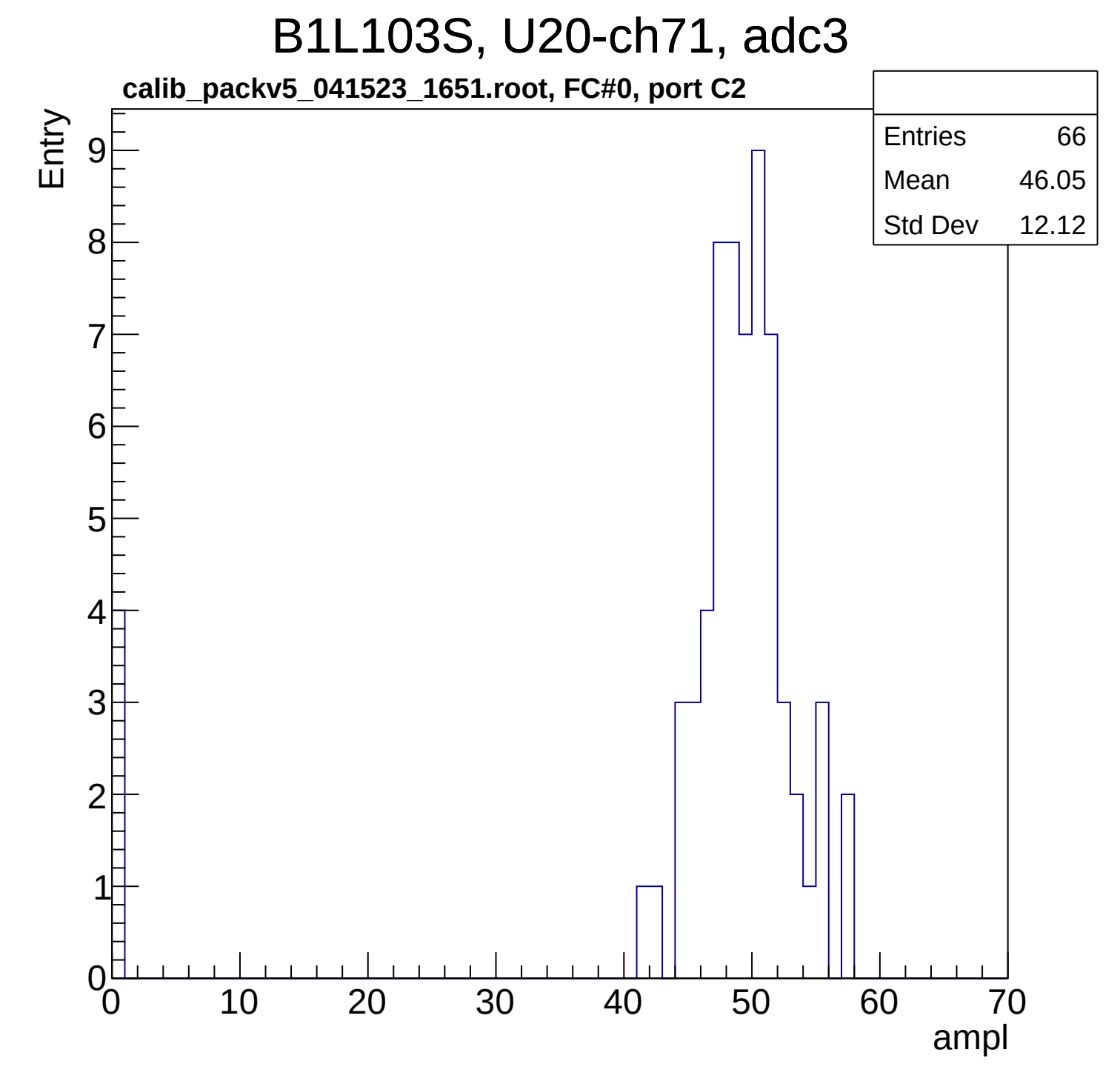
B1L103S, U20-ch71, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 46.05
Std Dev 12.12
Entry
ampl
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10
20
30
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2
3
4
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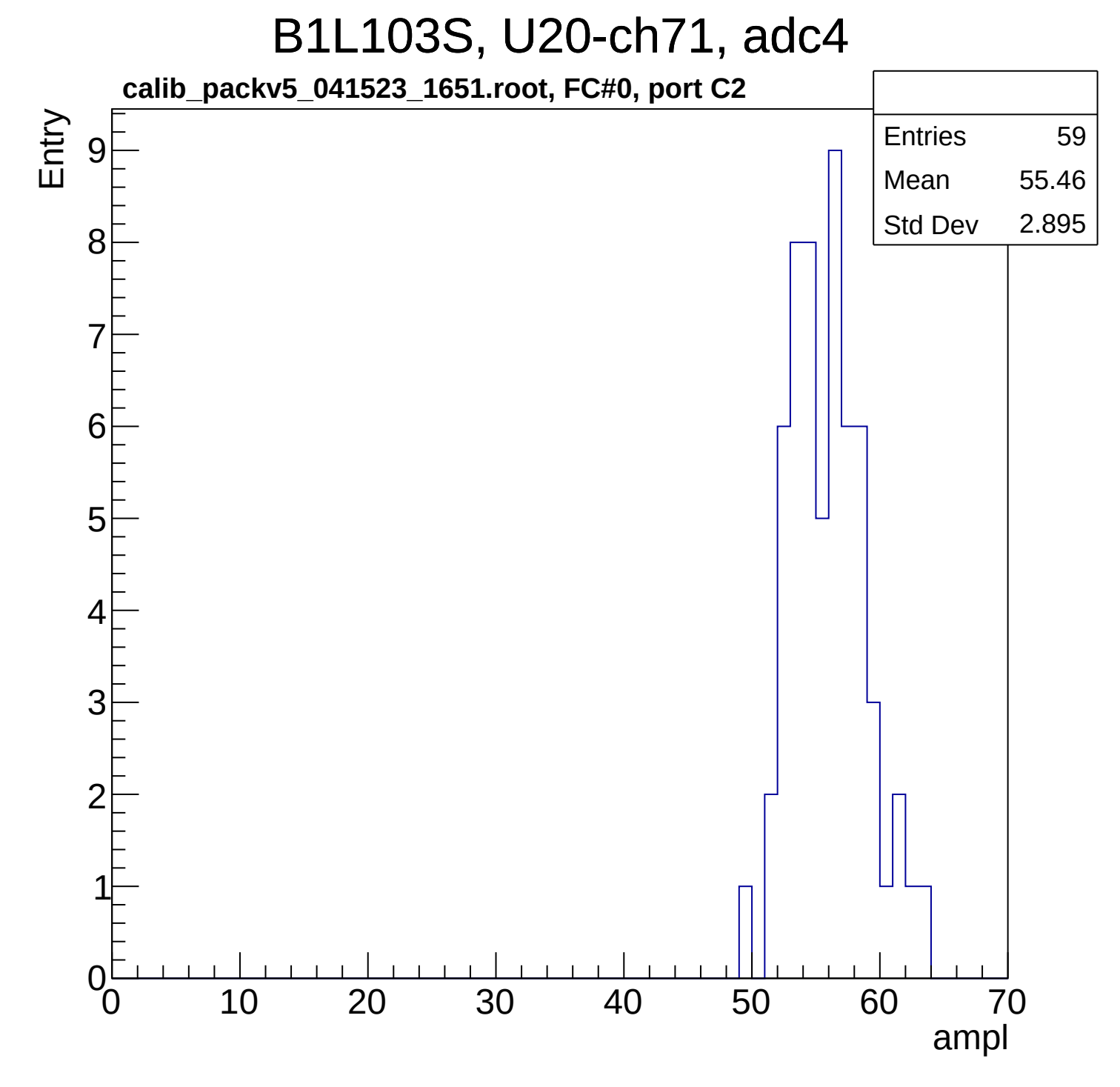
7
8
9


B1L103S, U20-ch71, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 55.46
Std Dev 2.895
Entry
ampl
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2
3
4
5
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60
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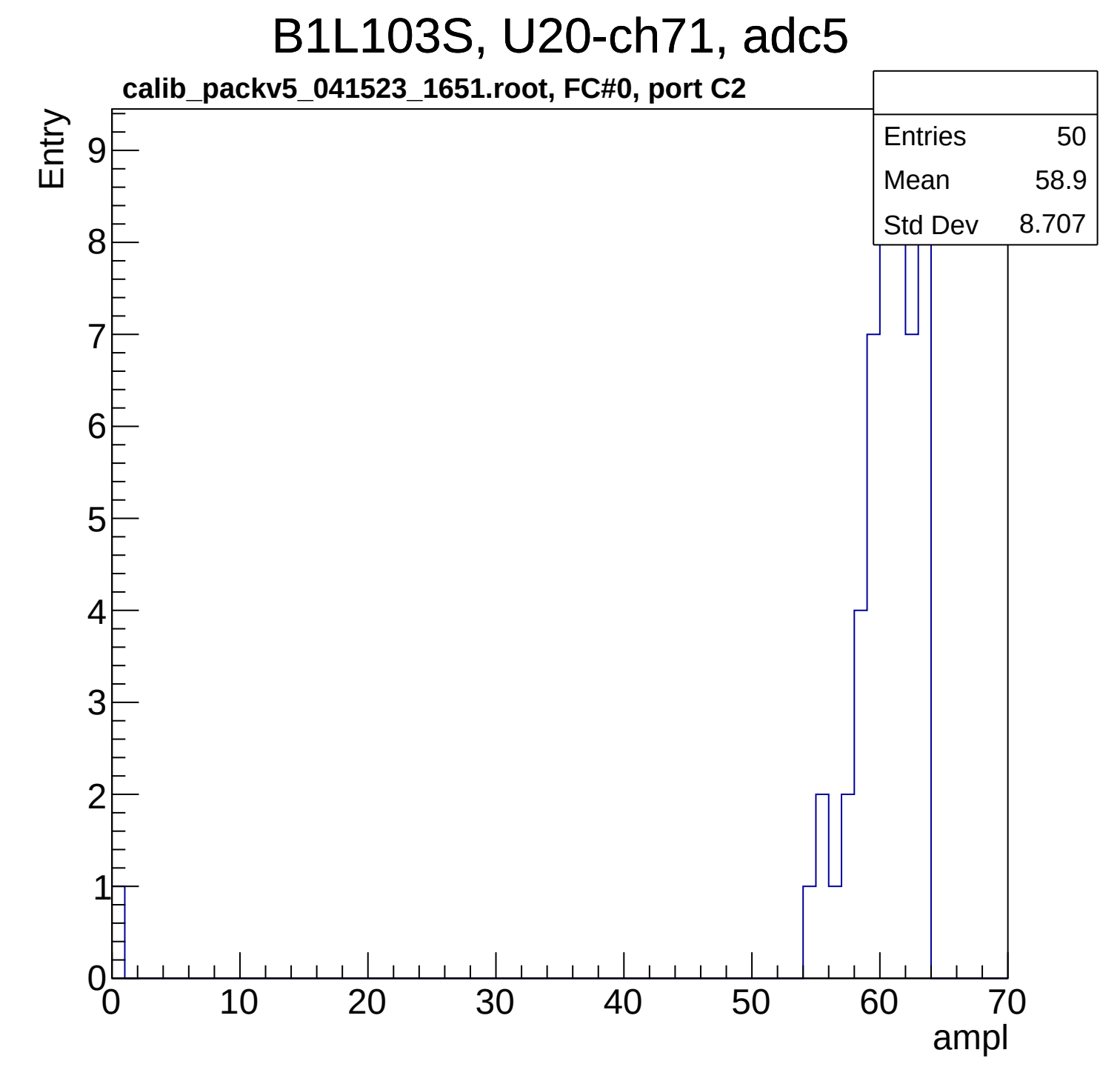
B1L103S, U20-ch71, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 58.9
Std Dev 8.707
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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60
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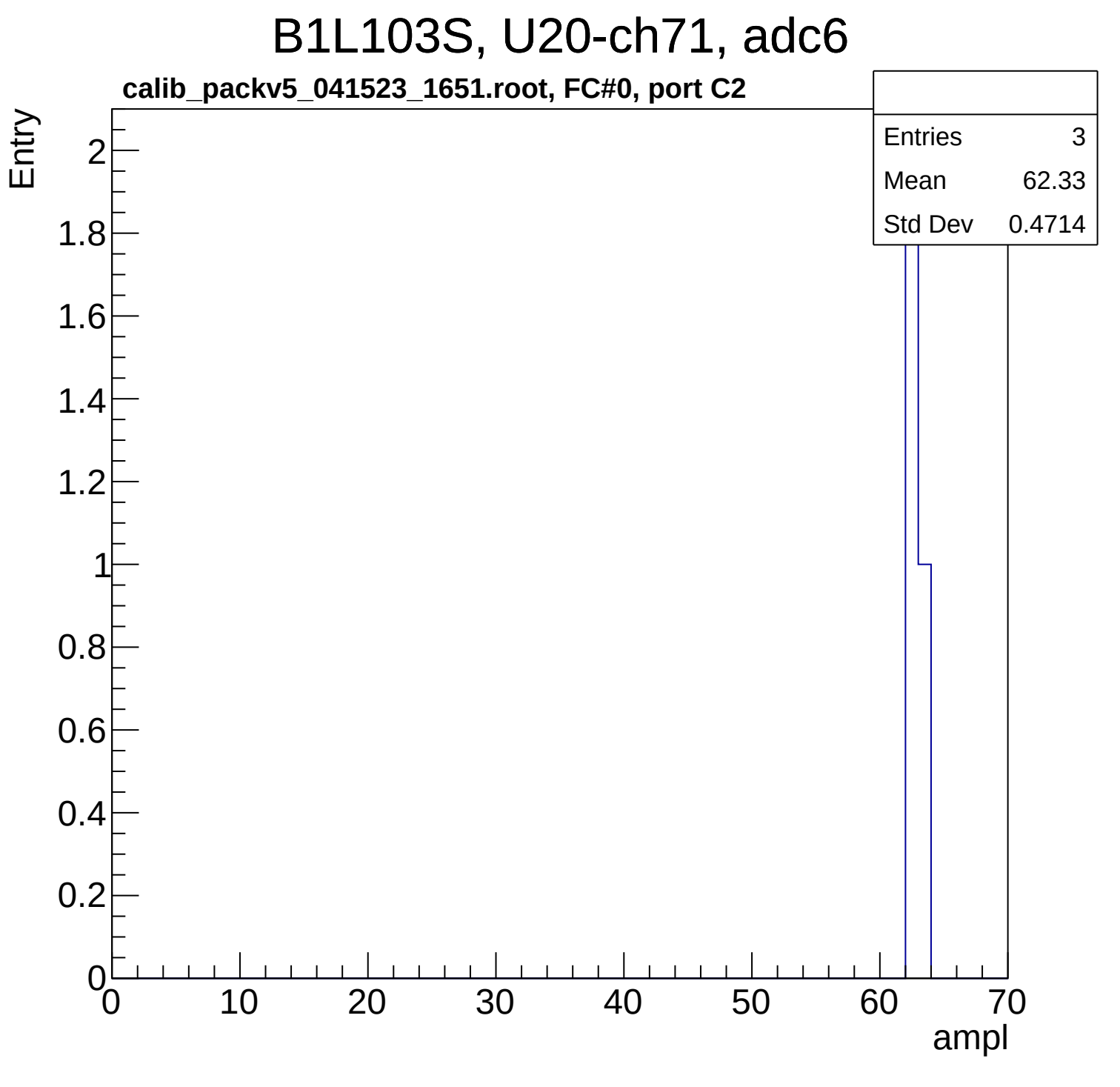
B1L103S, U20-ch71, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 62.33
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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40
50
60
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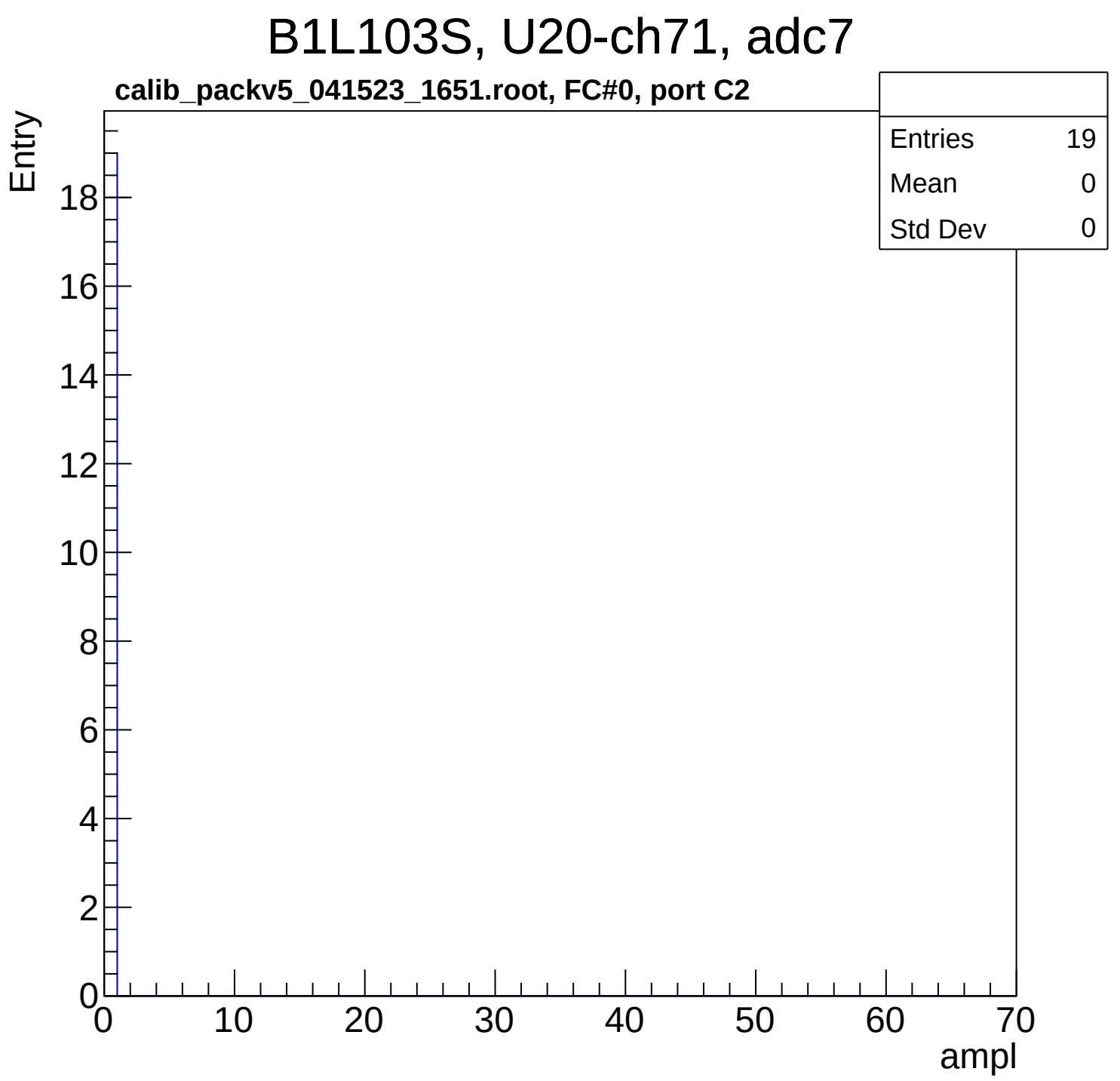
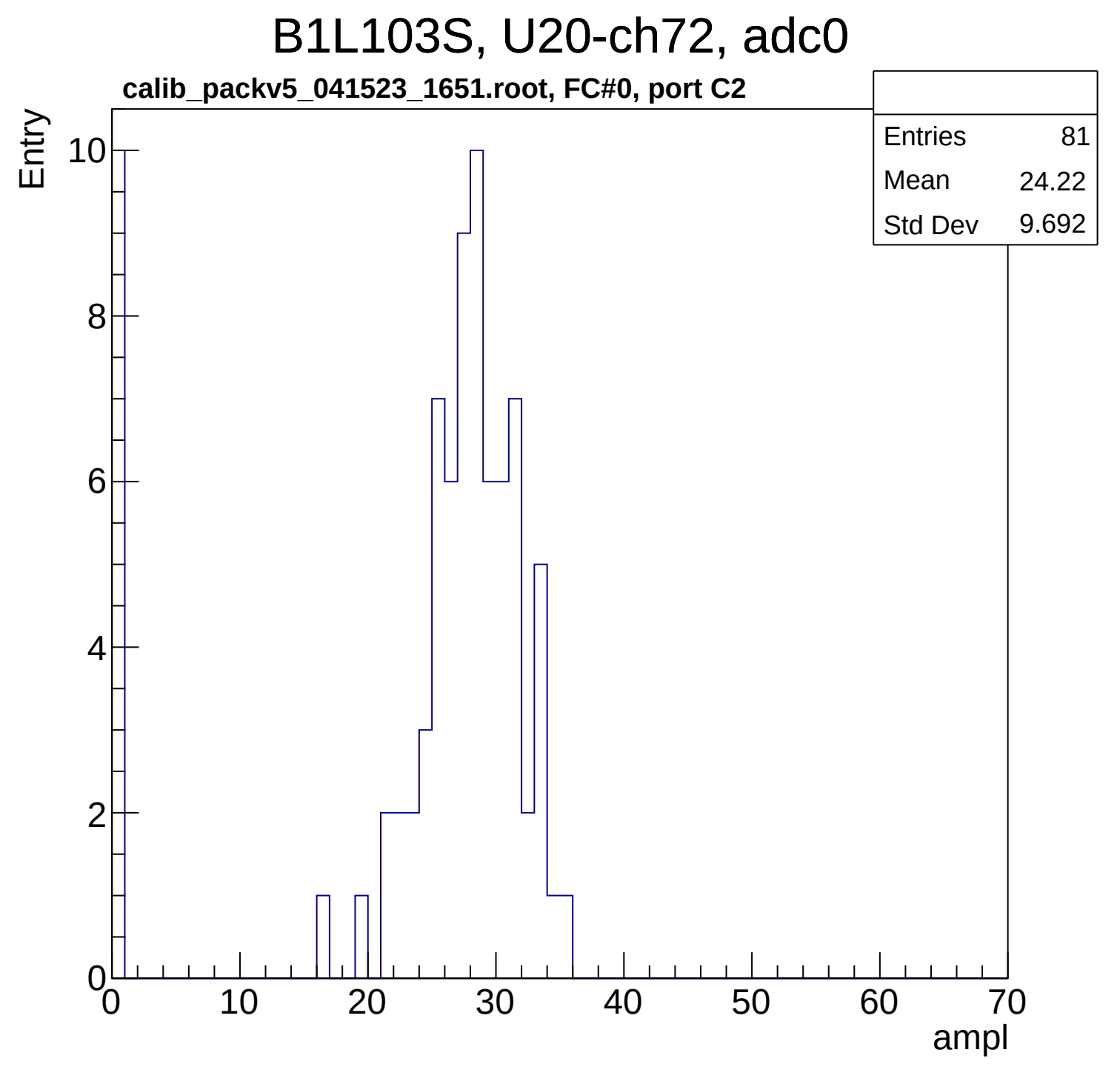
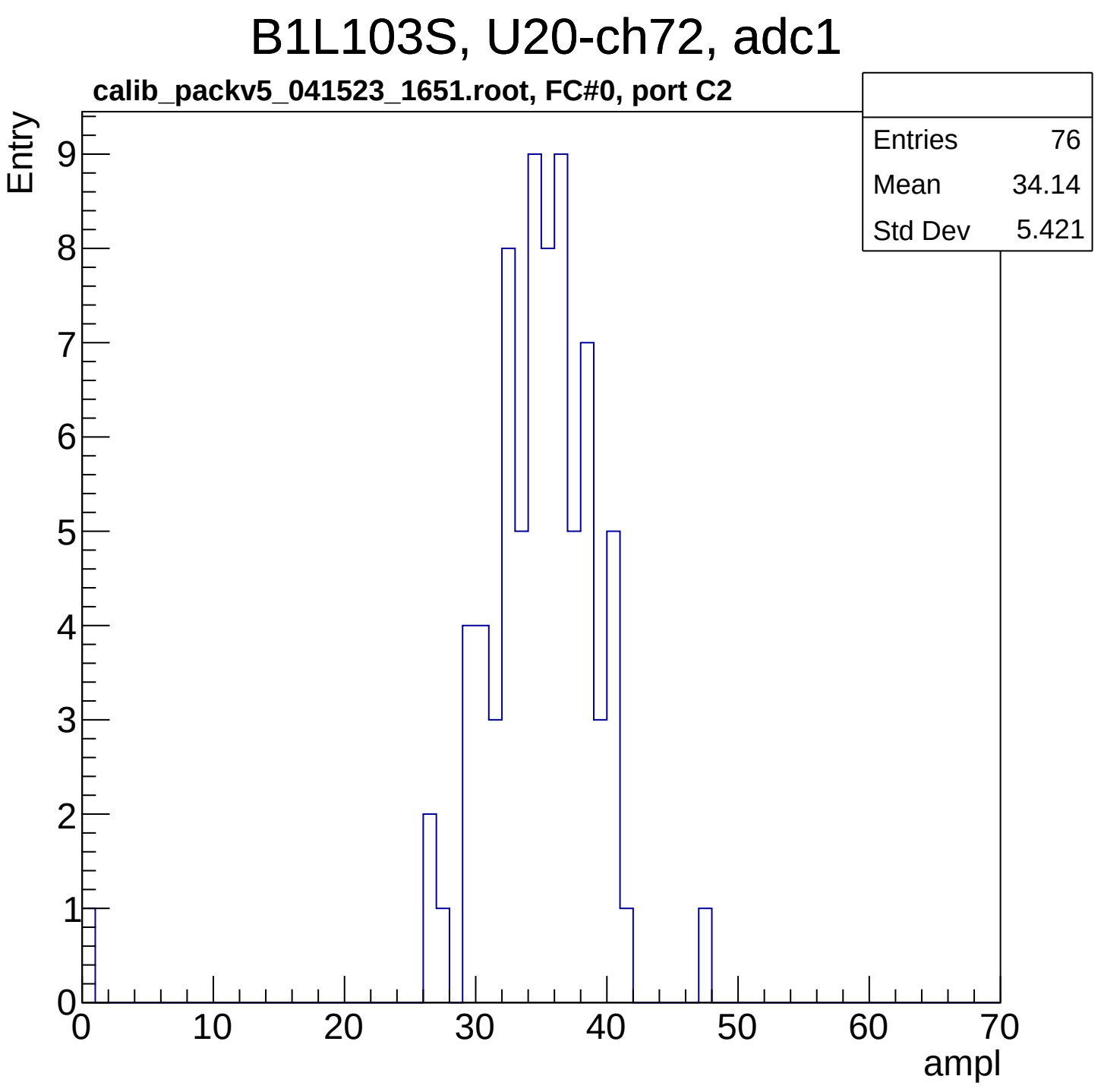

B1L103S, U20-ch71, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch72, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 24.22
Std Dev 9.692
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U20-ch72, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 34.14
Std Dev 5.421
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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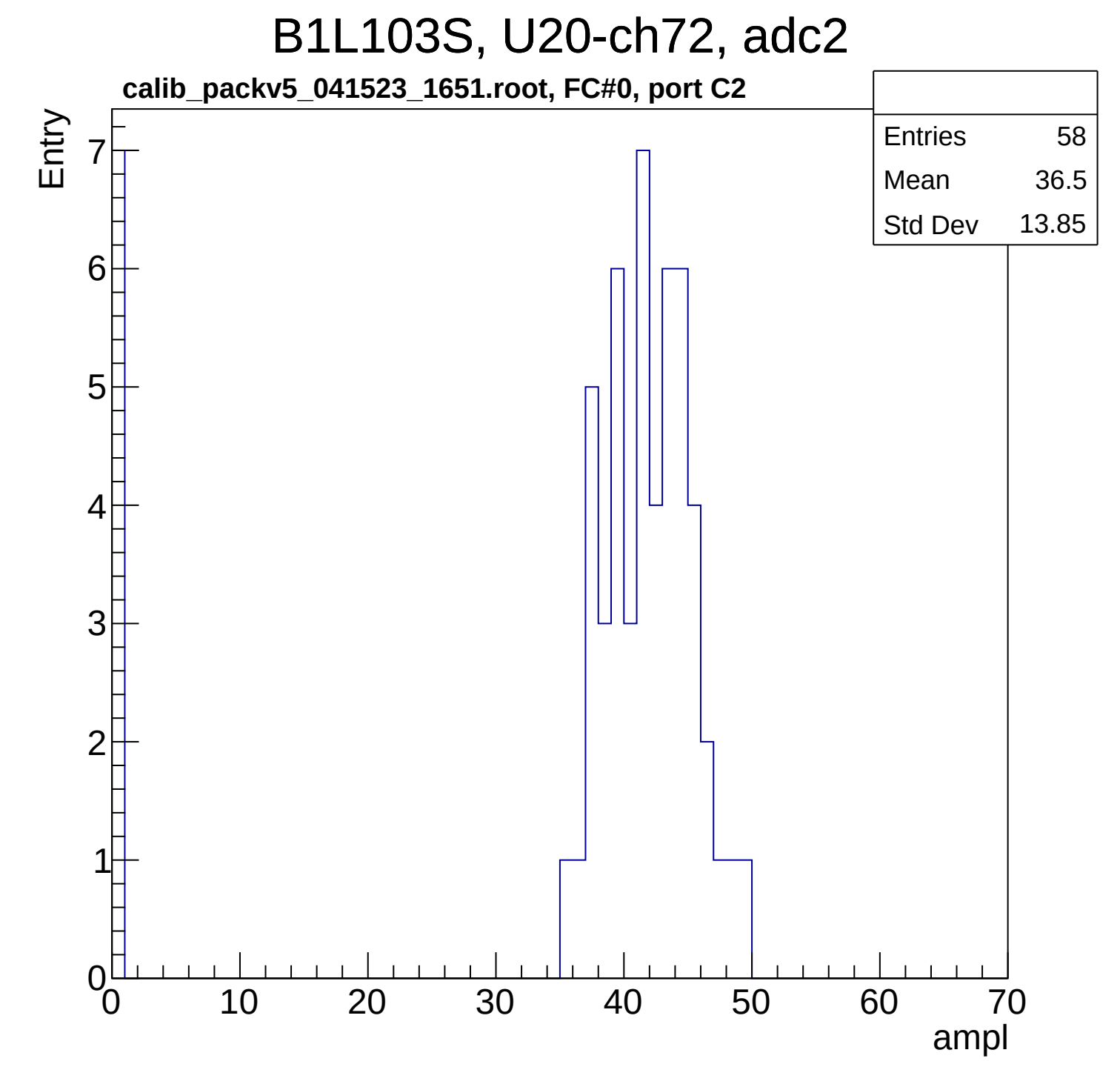
B1L103S, U20-ch72, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 36.5
Std Dev 13.85
Entry
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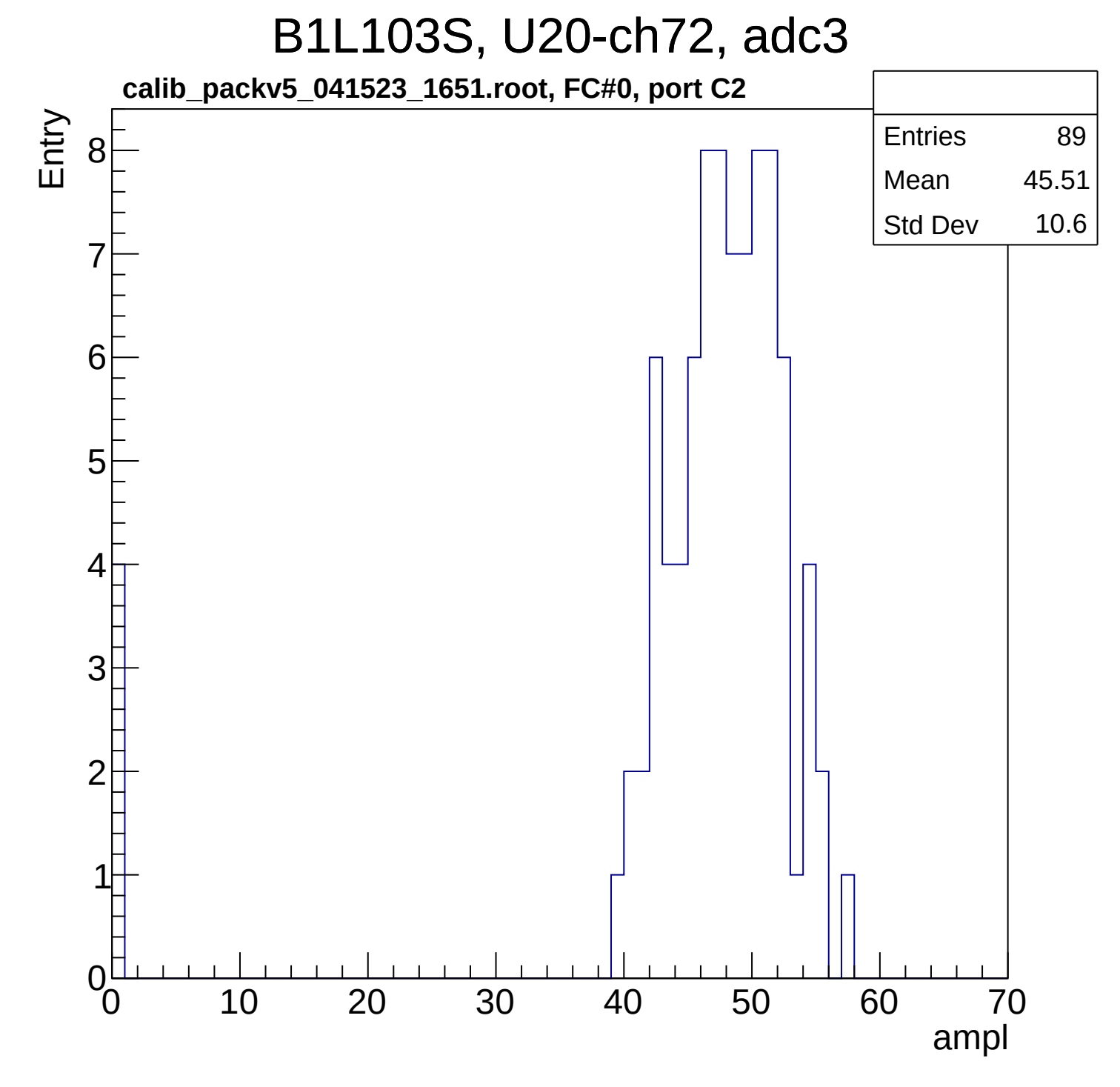
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch72, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 45.51
Std Dev 10.6
Entry
ampl
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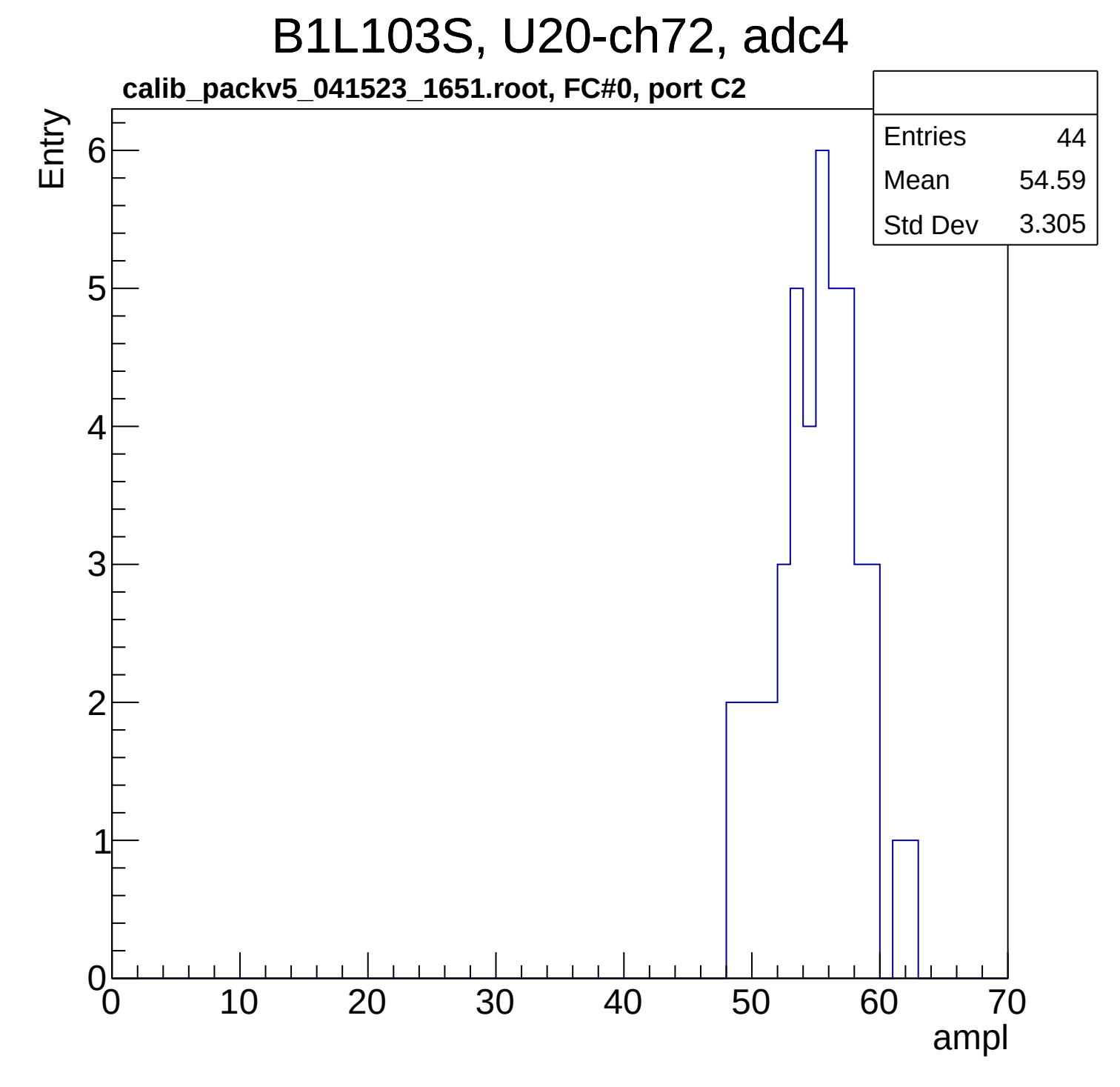
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch72, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 54.59
Std Dev 3.305
Entry
ampl
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3
4
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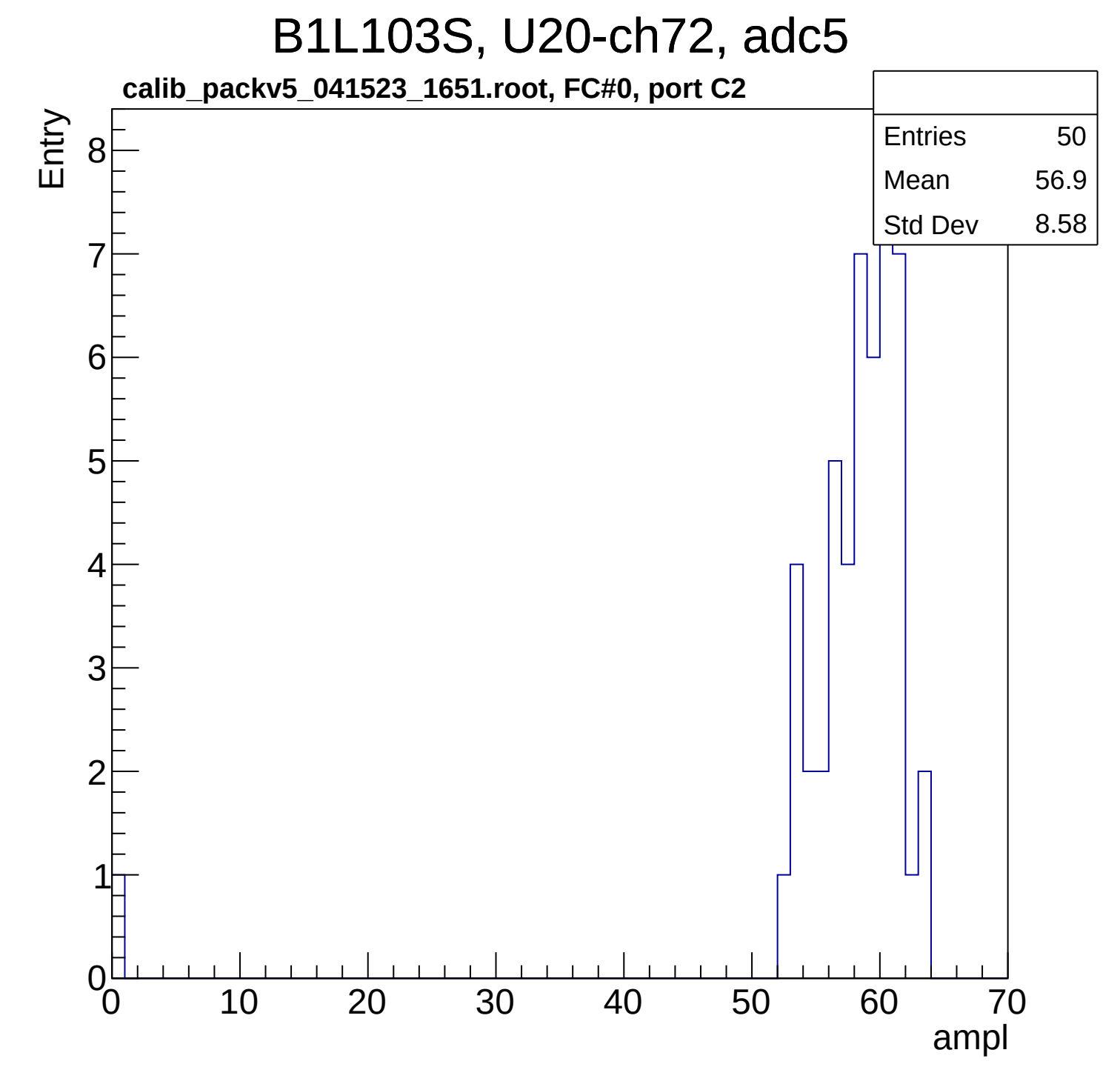
0
10
20
30
40
50
60
70


B1L103S, U20-ch72, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 56.9
Std Dev 8.58
Entry
ampl
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4
5
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0
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20
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60
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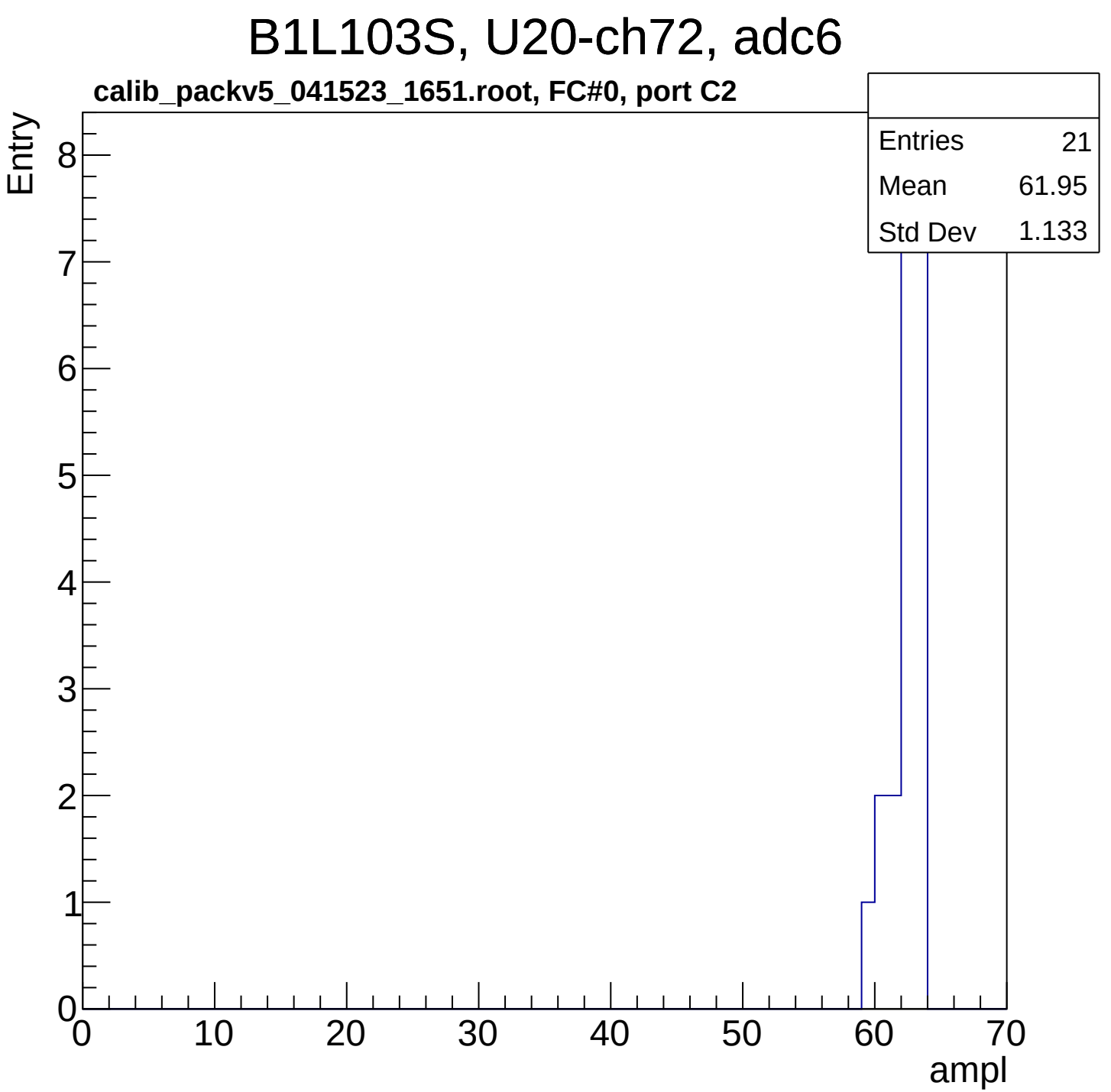
B1L103S, U20-ch72, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 61.95
Std Dev 1.133
Entry
ampl
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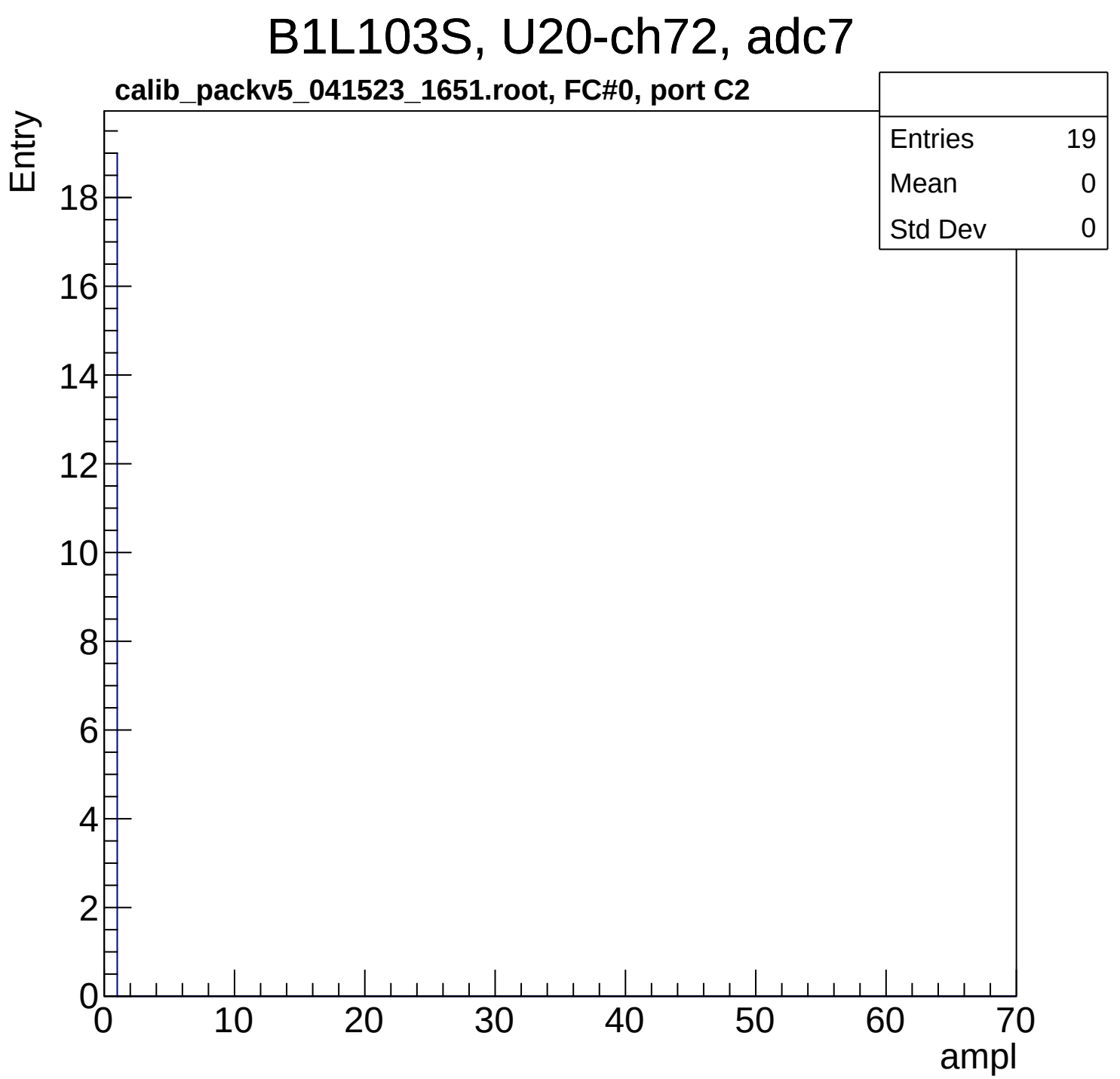
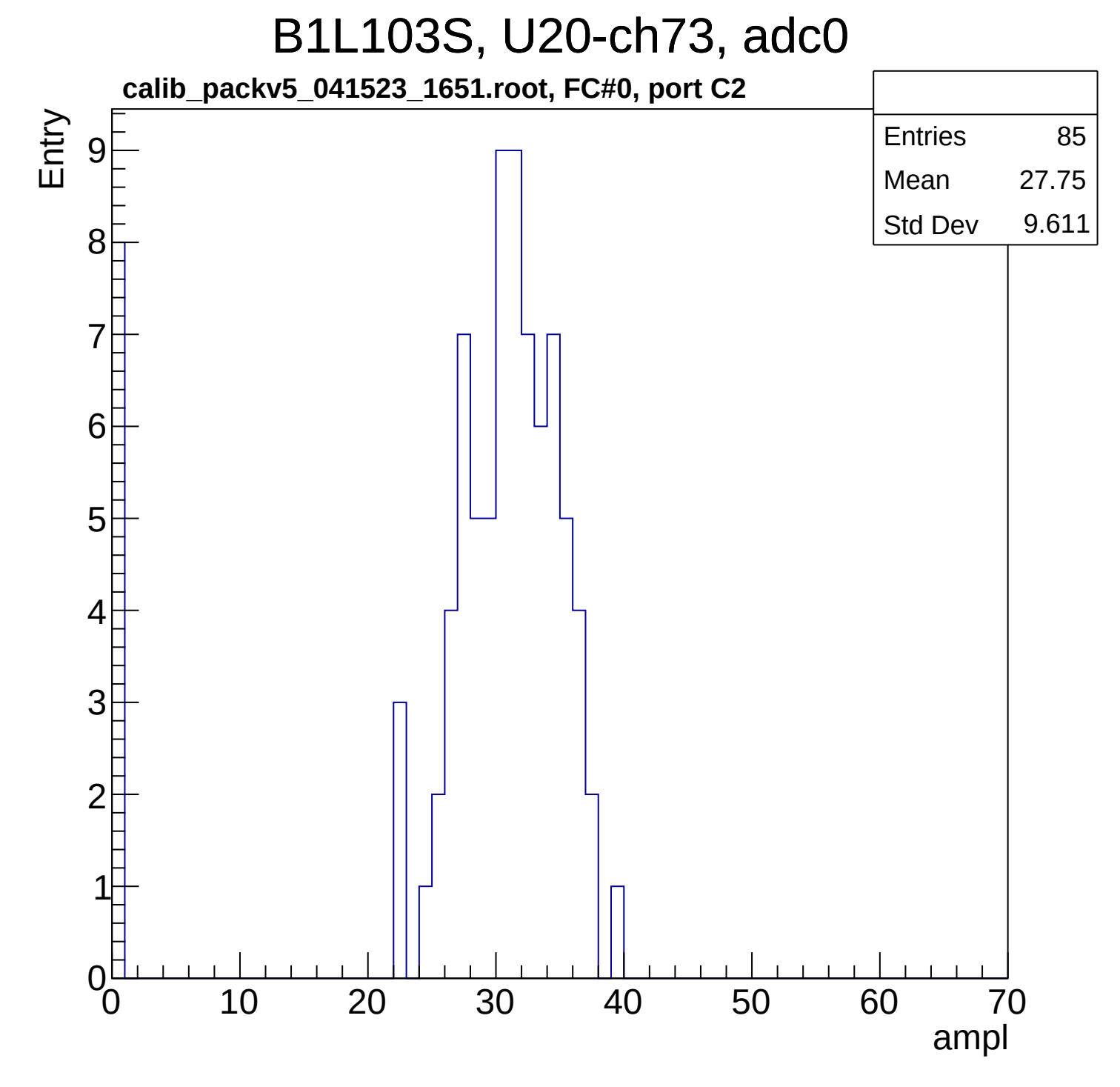
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch72, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch73, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 27.75
Std Dev 9.611
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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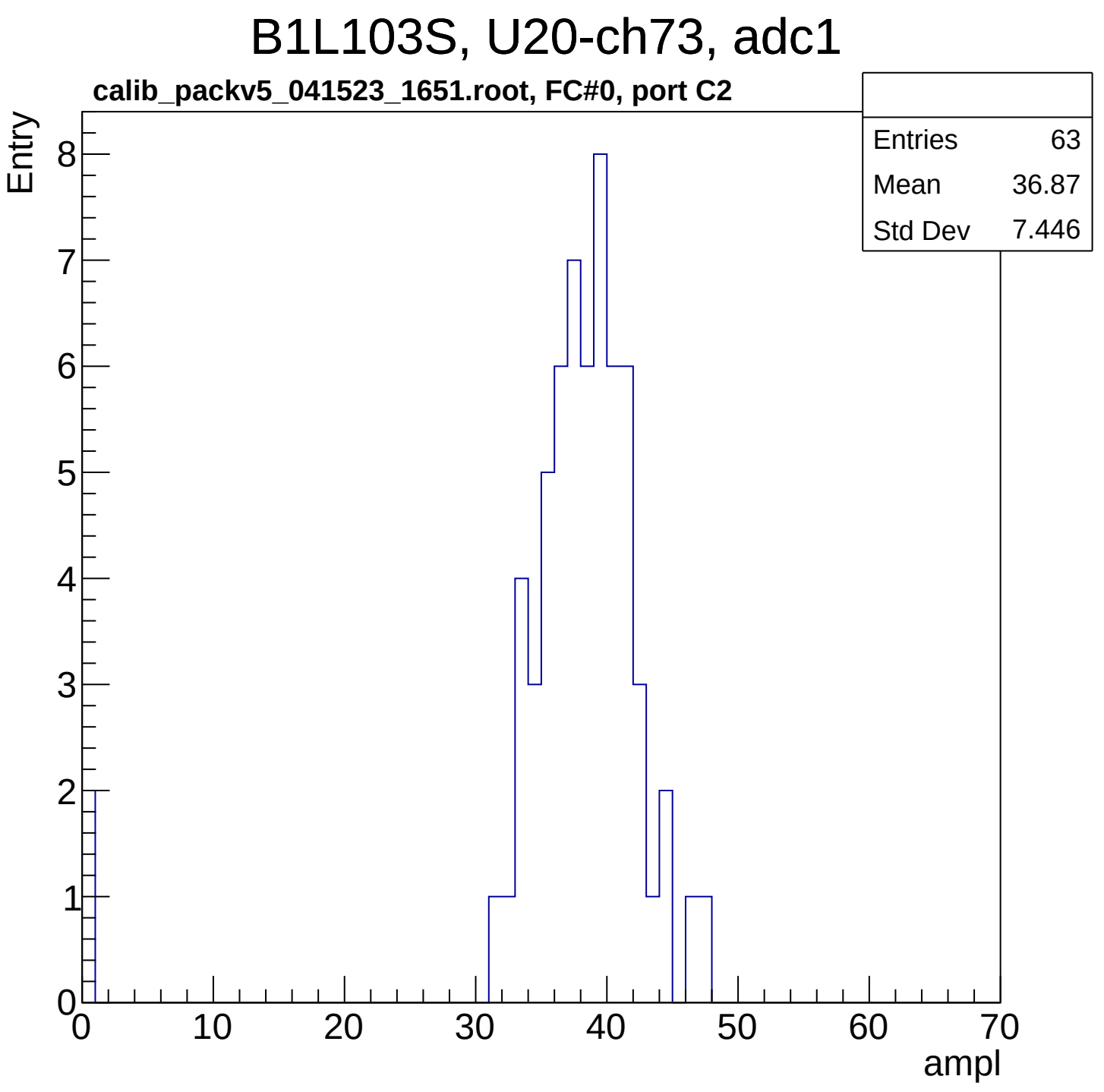
B1L103S, U20-ch73, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 36.87
Std Dev 7.446
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
50
60
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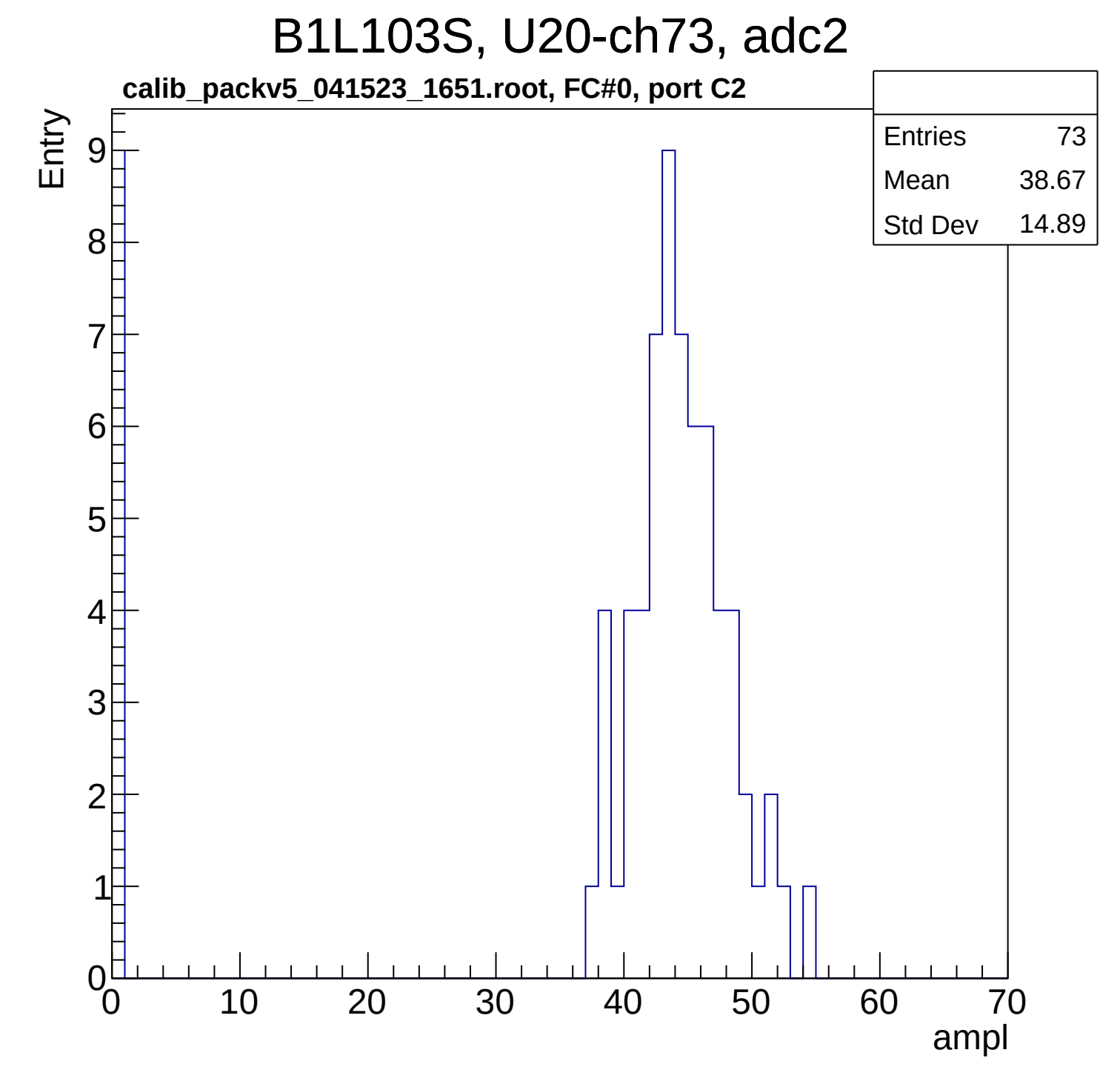
B1L103S, U20-ch73, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 38.67
Std Dev 14.89
Entry
ampl
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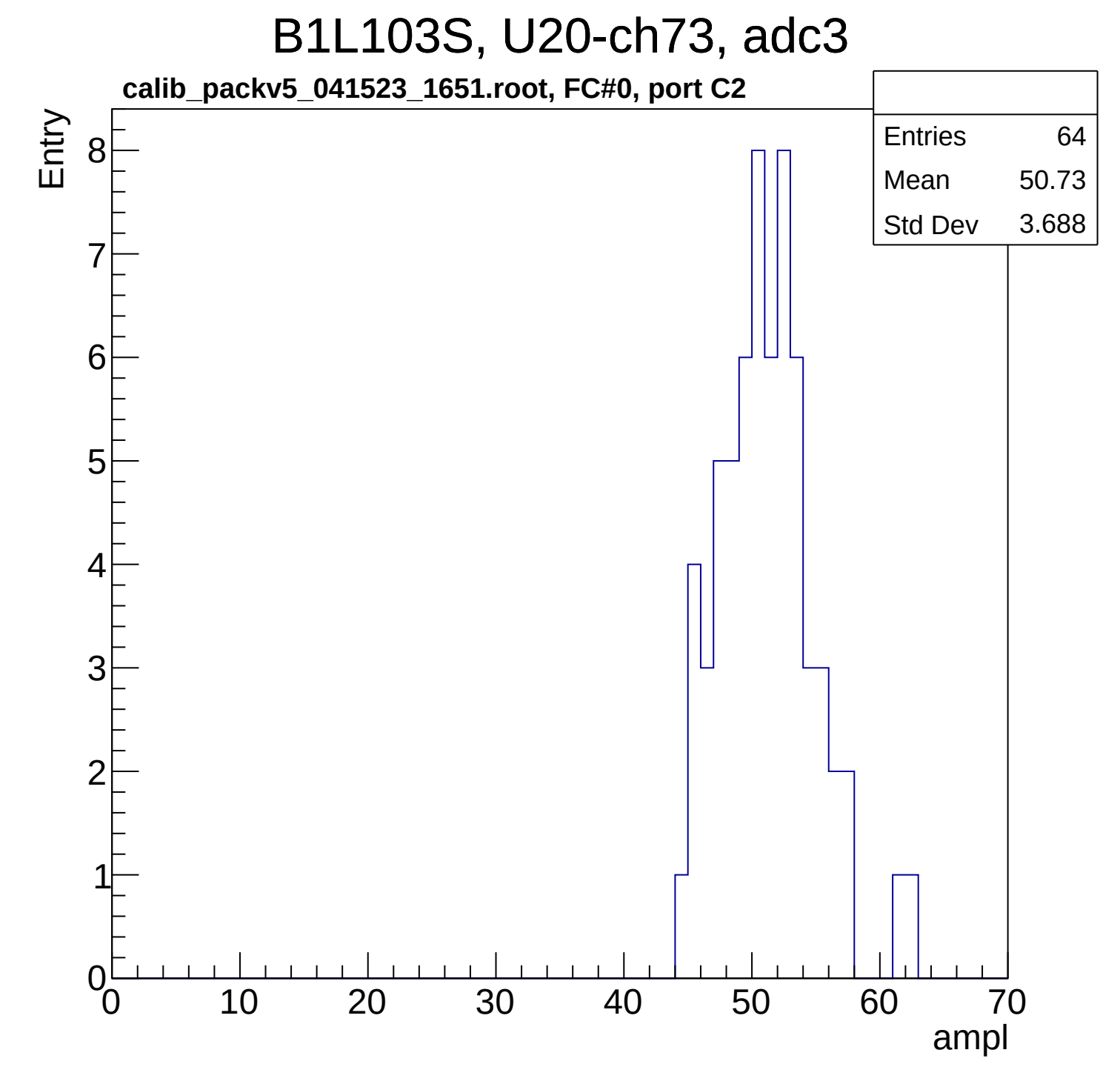
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch73, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 50.73
Std Dev 3.688
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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60
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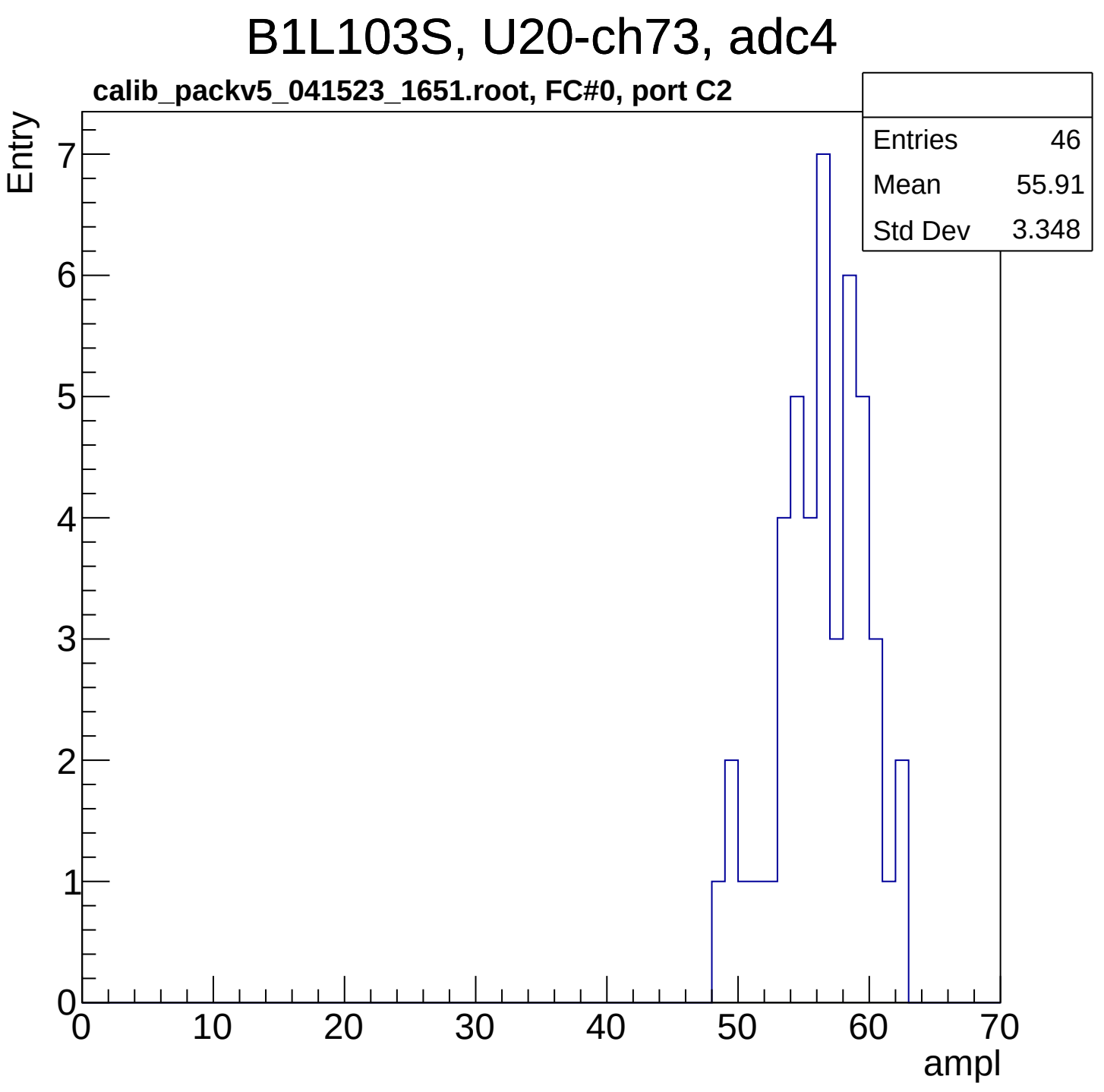
B1L103S, U20-ch73, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 55.91
Std Dev 3.348
Entry
ampl
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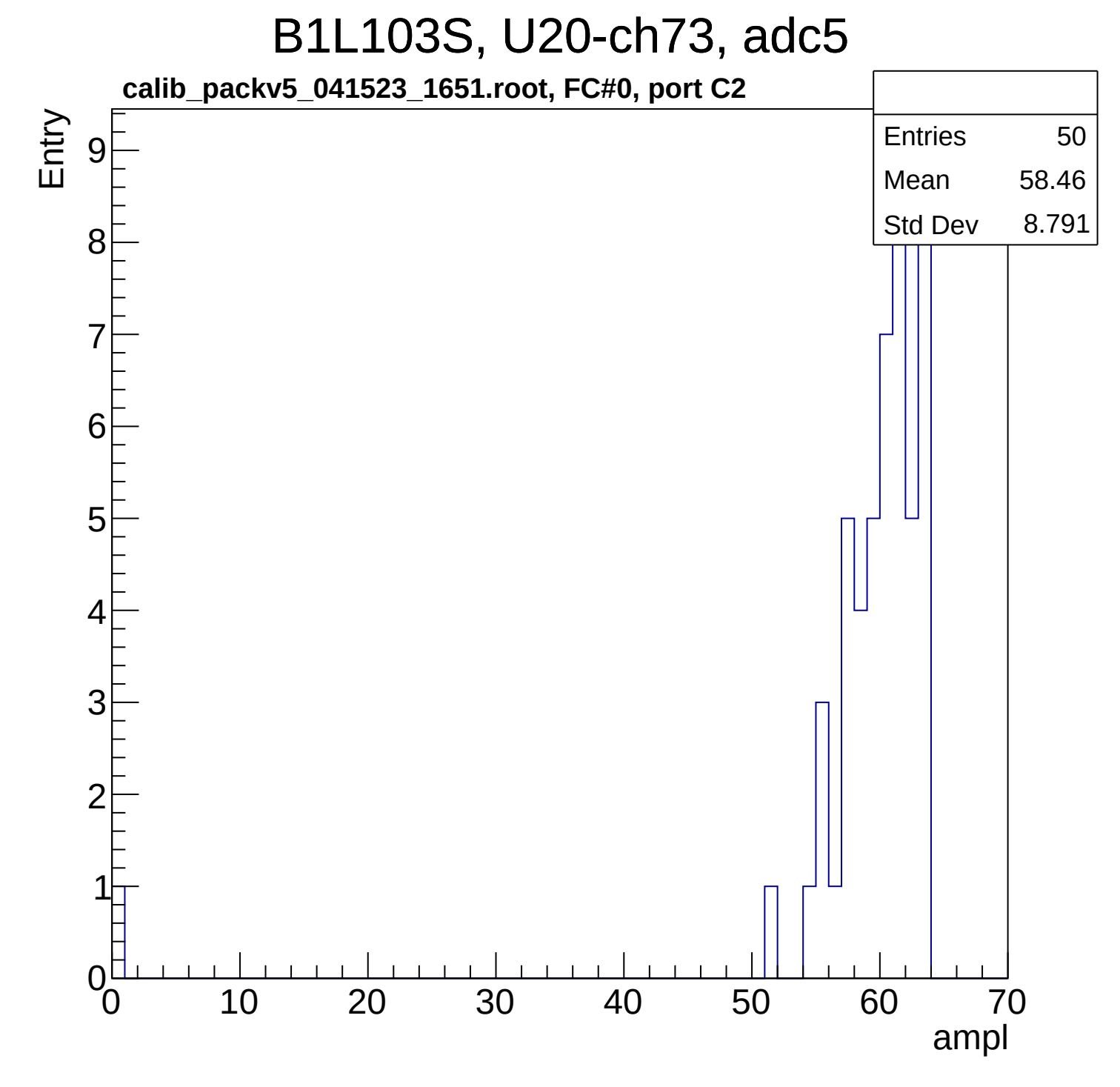
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U20-ch73, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 58.46
Std Dev 8.791
Entry
ampl
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2
3
4
5
6
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8
9
0
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40
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60
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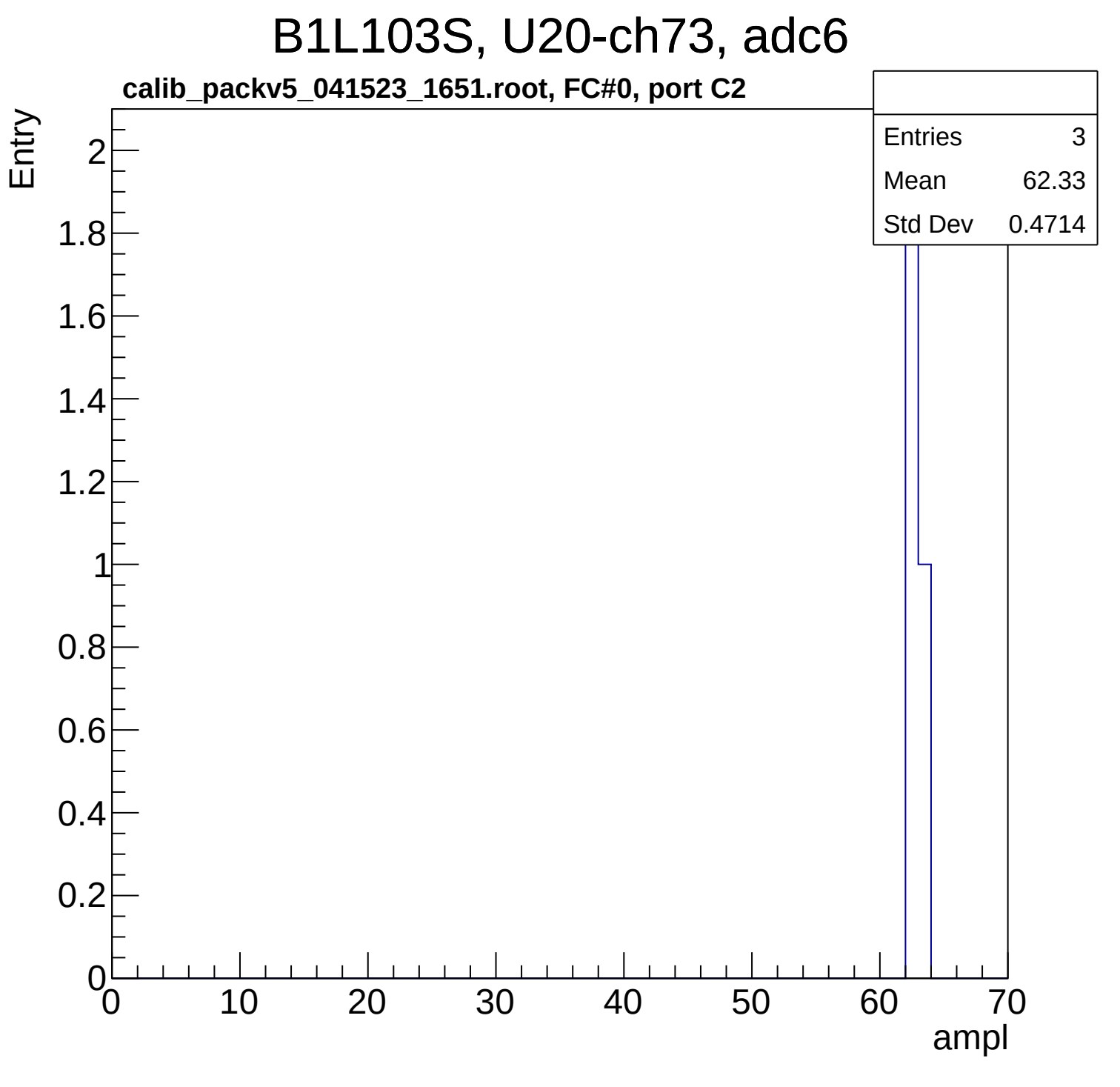
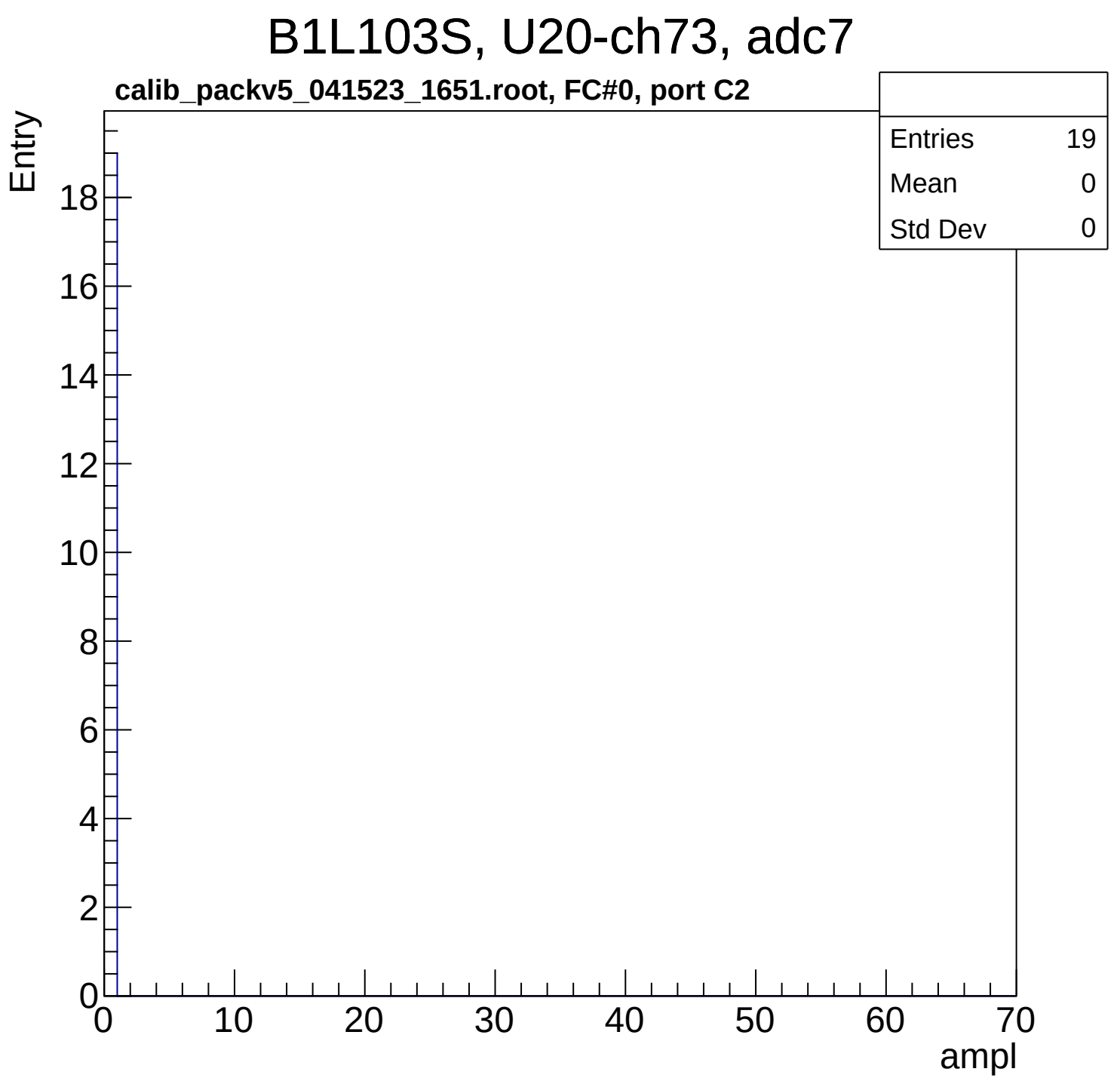
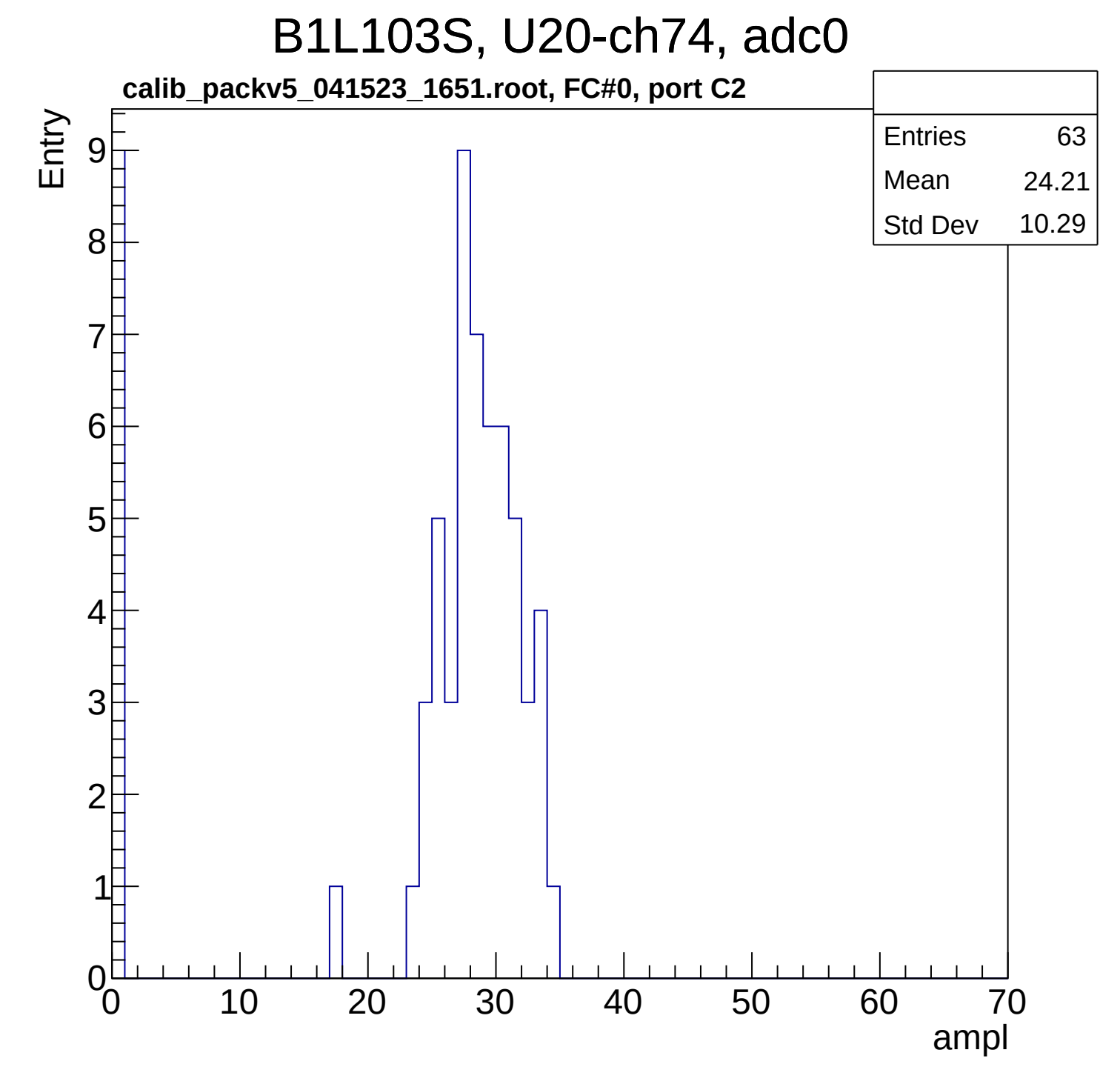

B1L103S, U20-ch73, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 62.33
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U20-ch73, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch74, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 24.21
Std Dev 10.29
Entry
ampl
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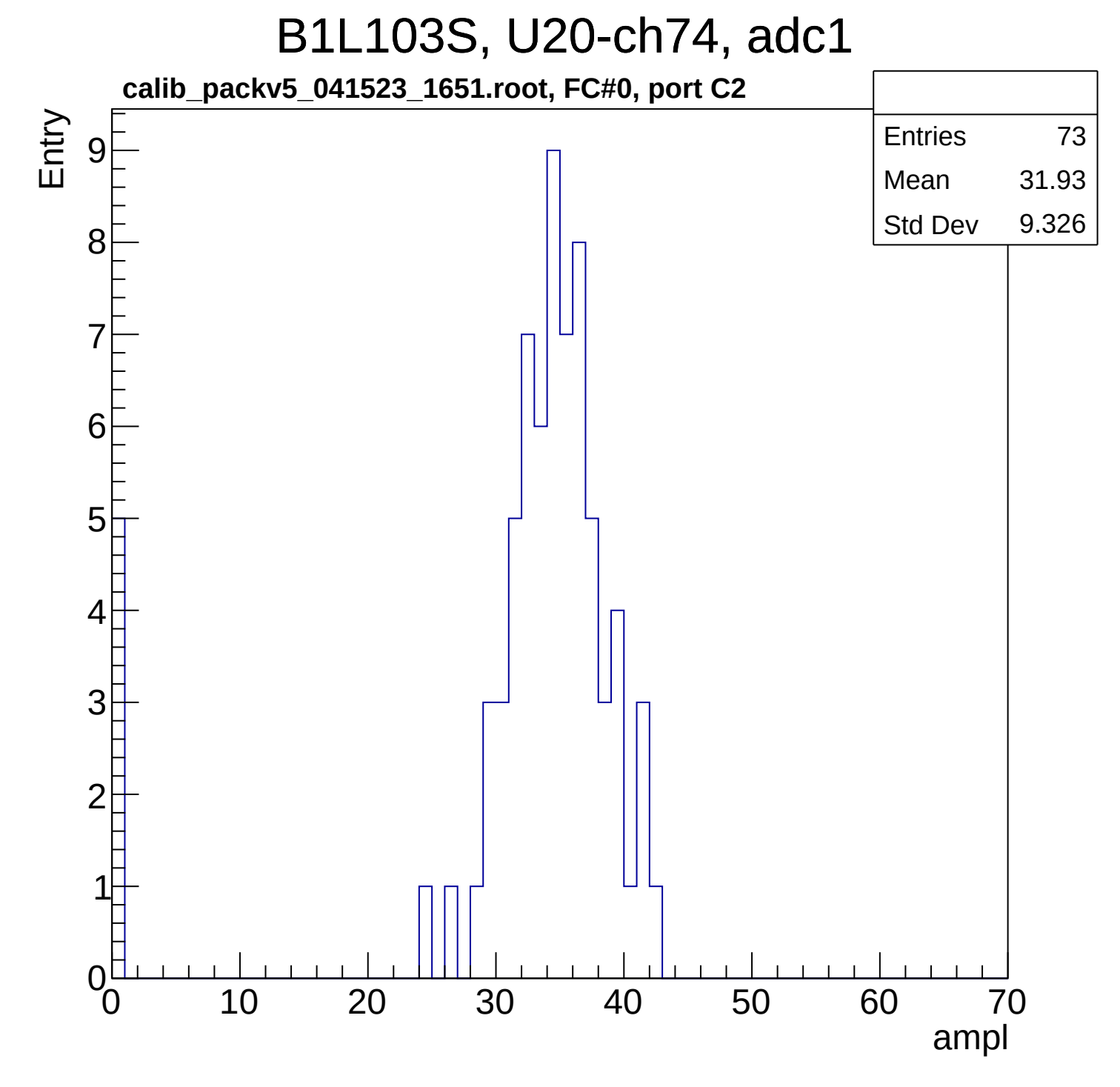
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch74, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 31.93
Std Dev 9.326
Entry
ampl
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2
3
4
5
6
7
8
9
0
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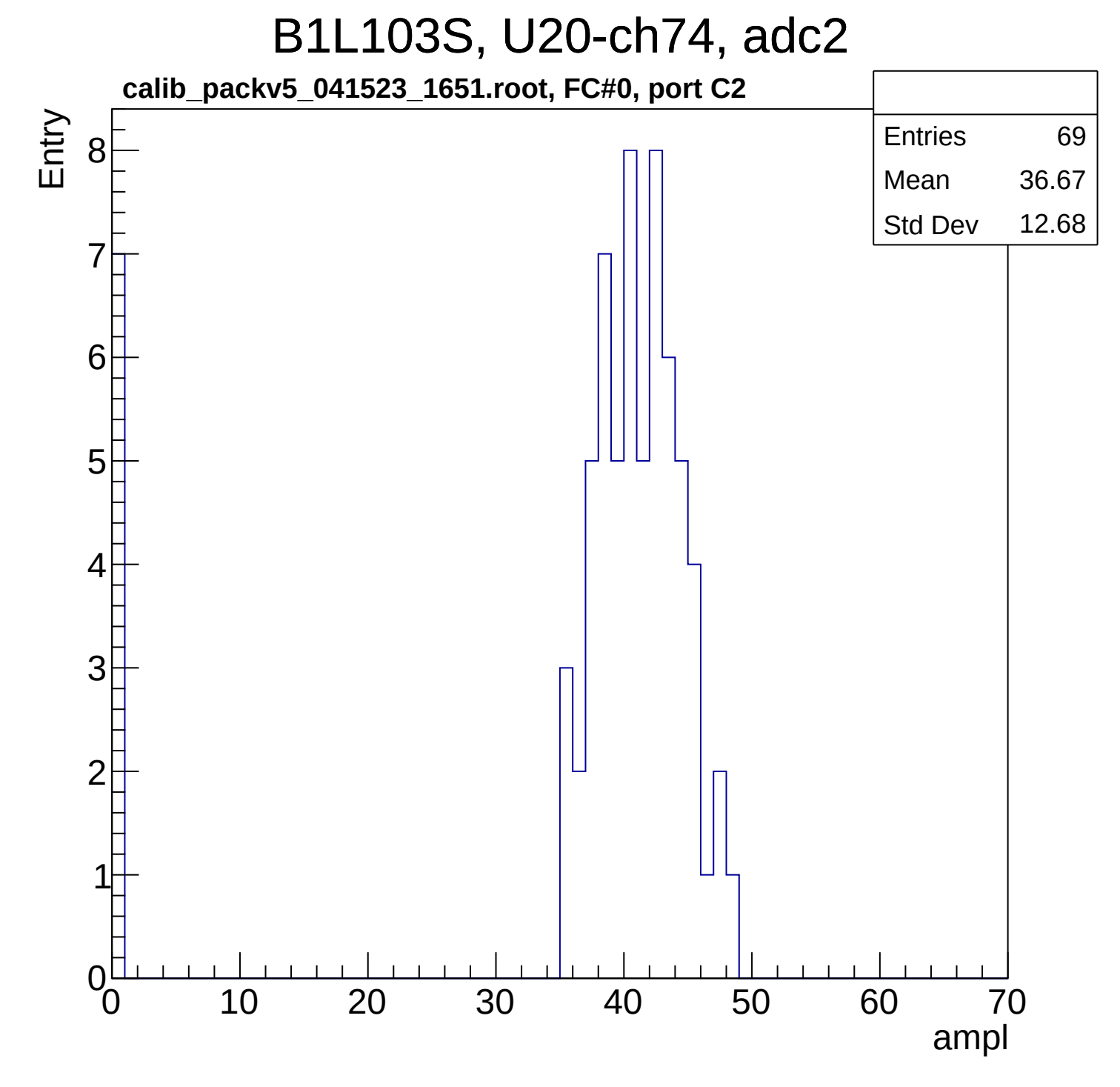
B1L103S, U20-ch74, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 36.67
Std Dev 12.68
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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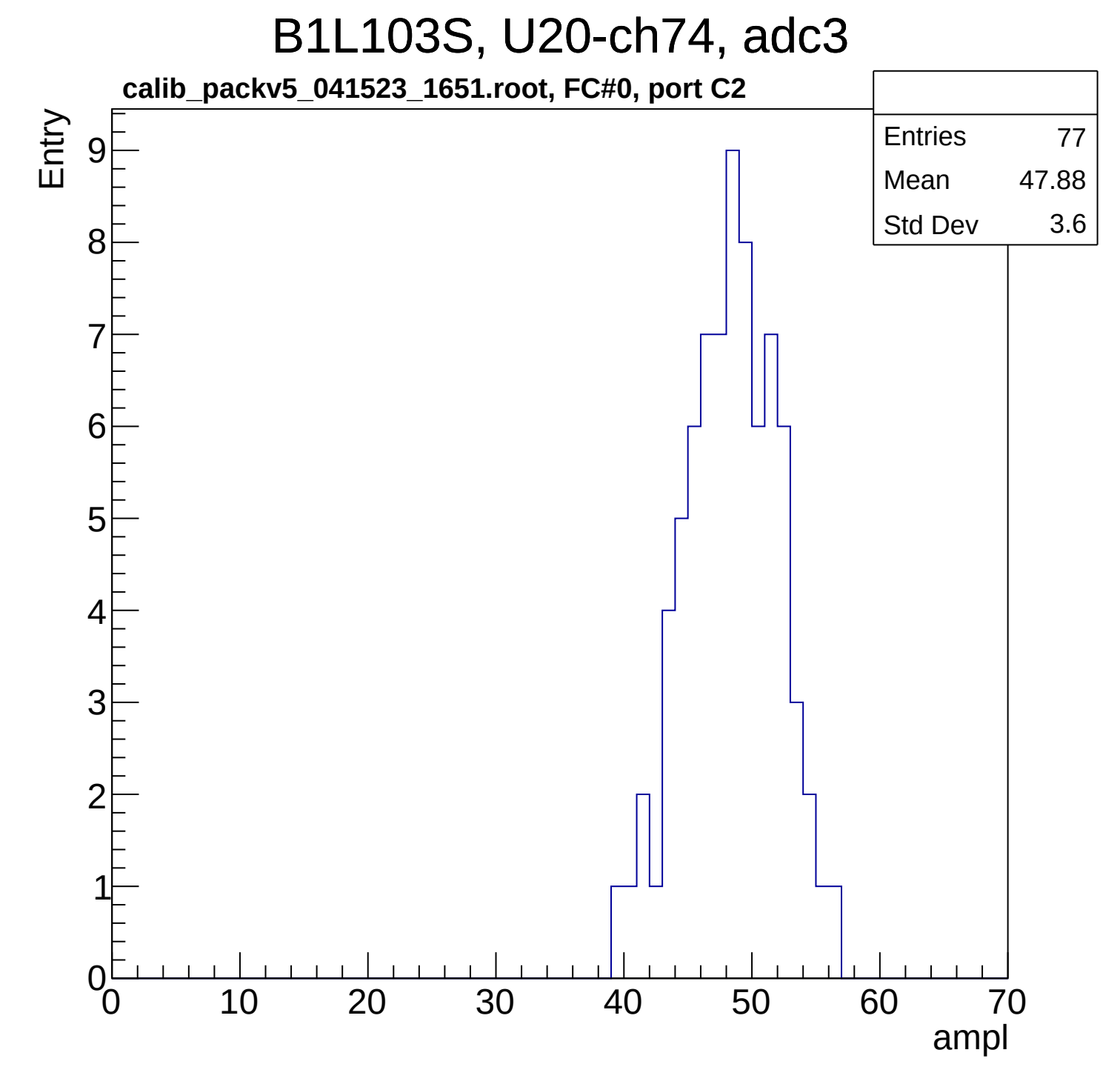
40
50
60
70


B1L103S, U20-ch74, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 47.88
Std Dev 3.6
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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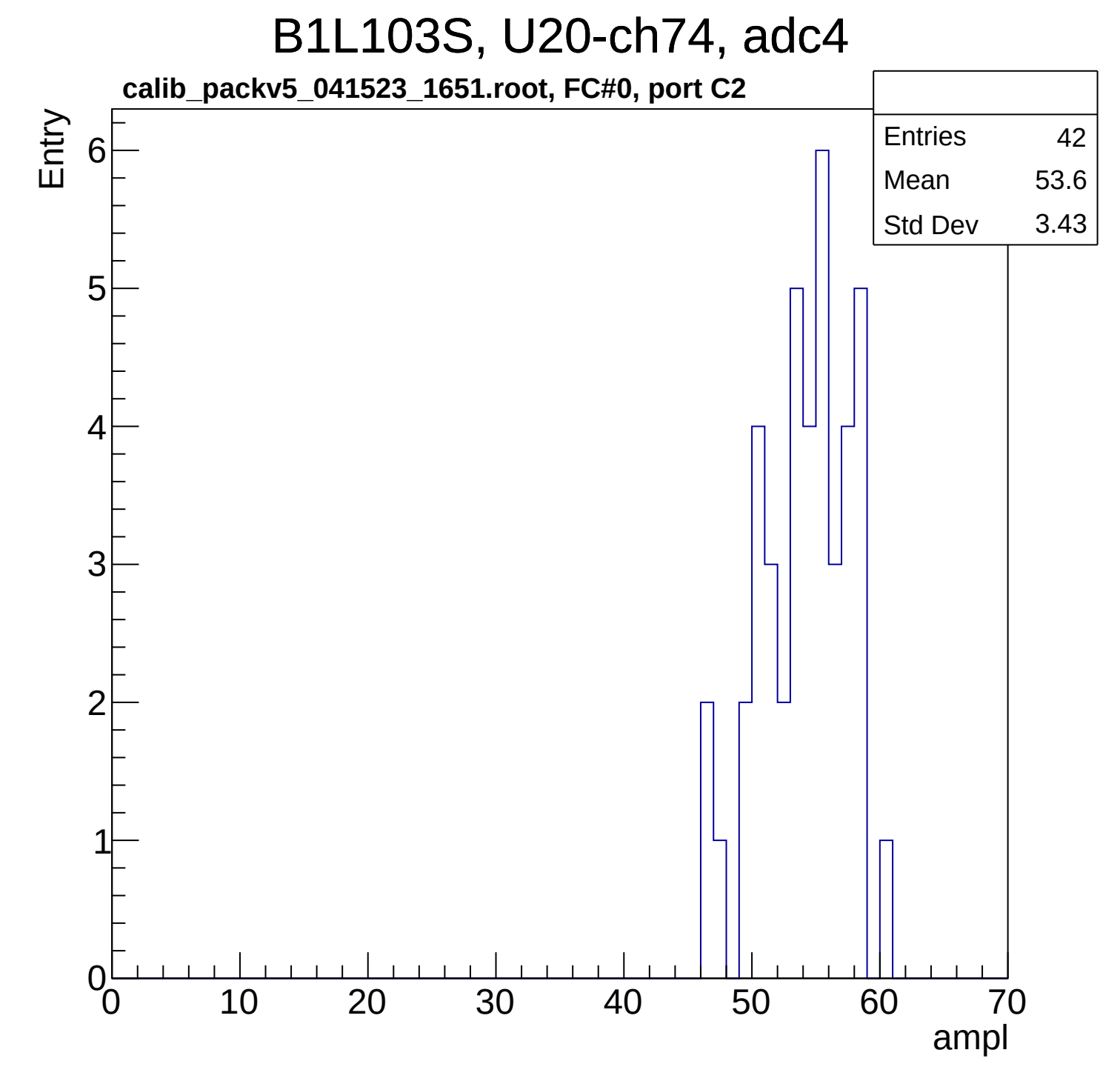
40
50
60
70


B1L103S, U20-ch74, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 53.6
Std Dev 3.43
Entry
ampl
0
1
2
3
4
5
6
0
10
20
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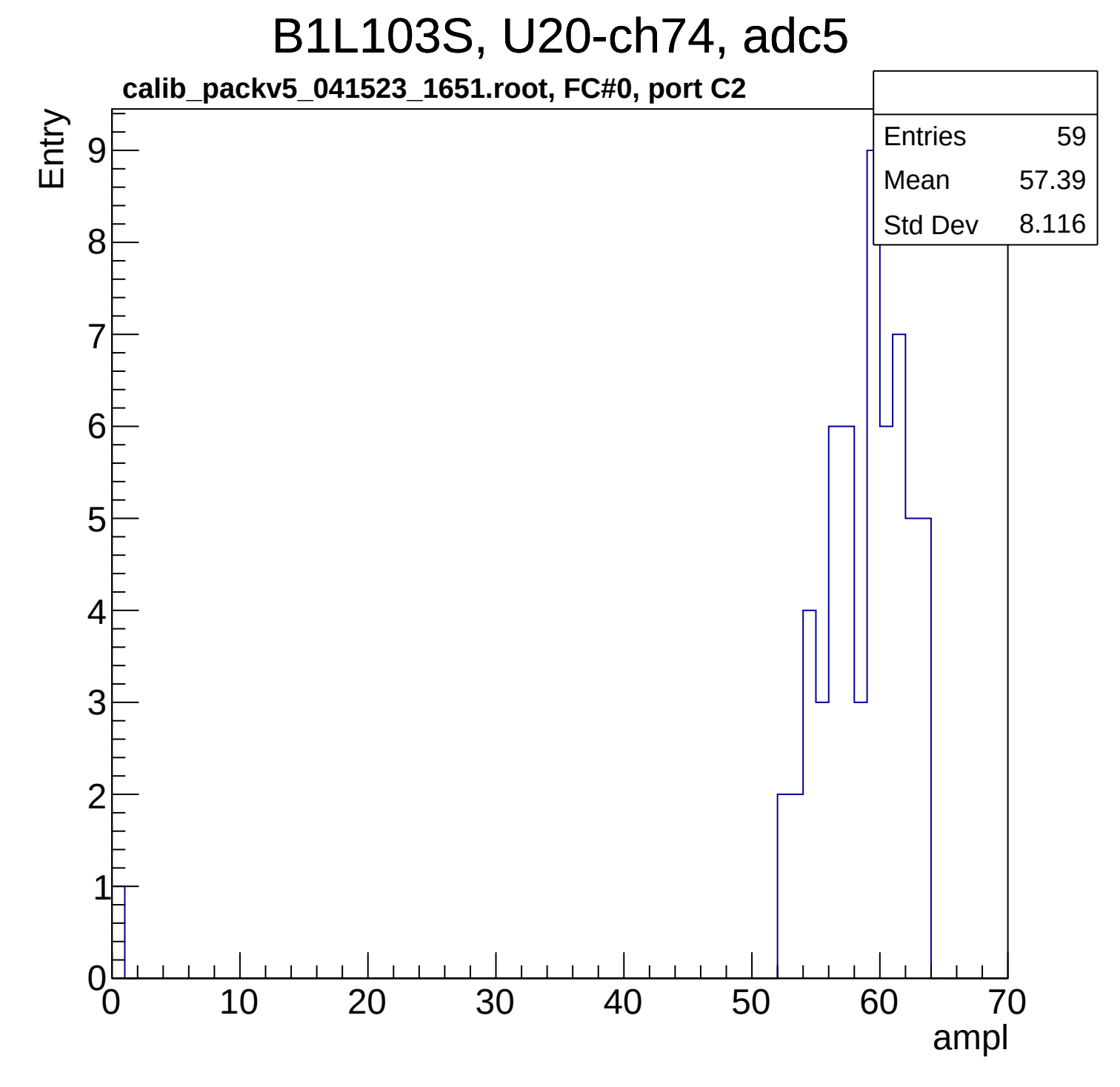
40
50
60
70


B1L103S, U20-ch74, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 57.39
Std Dev 8.116
Entry
ampl
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3
4
5
6
7
8
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0
10
20
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40
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60
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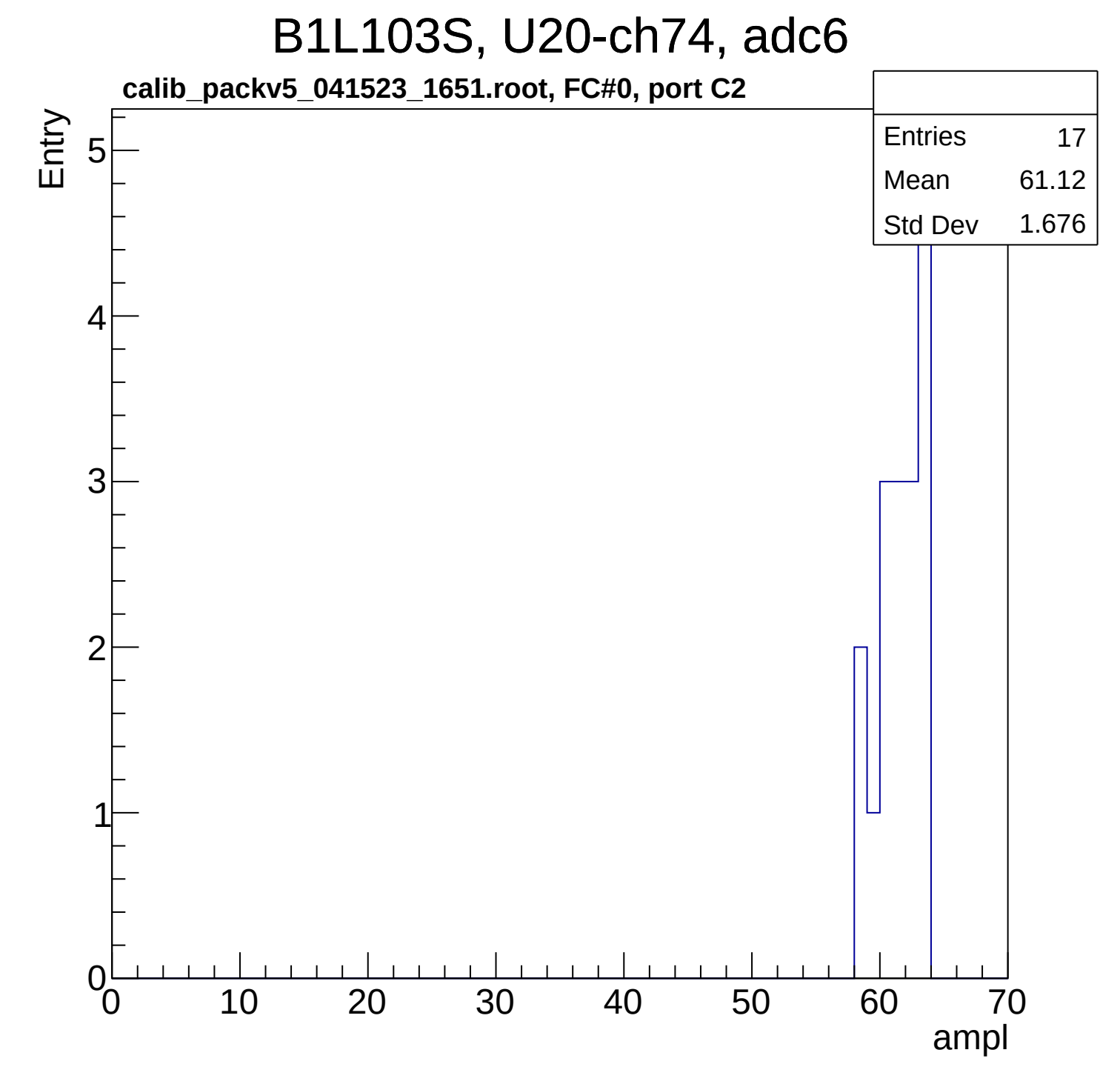
B1L103S, U20-ch74, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 61.12
Std Dev 1.676
Entry
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2
3
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5
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10
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30
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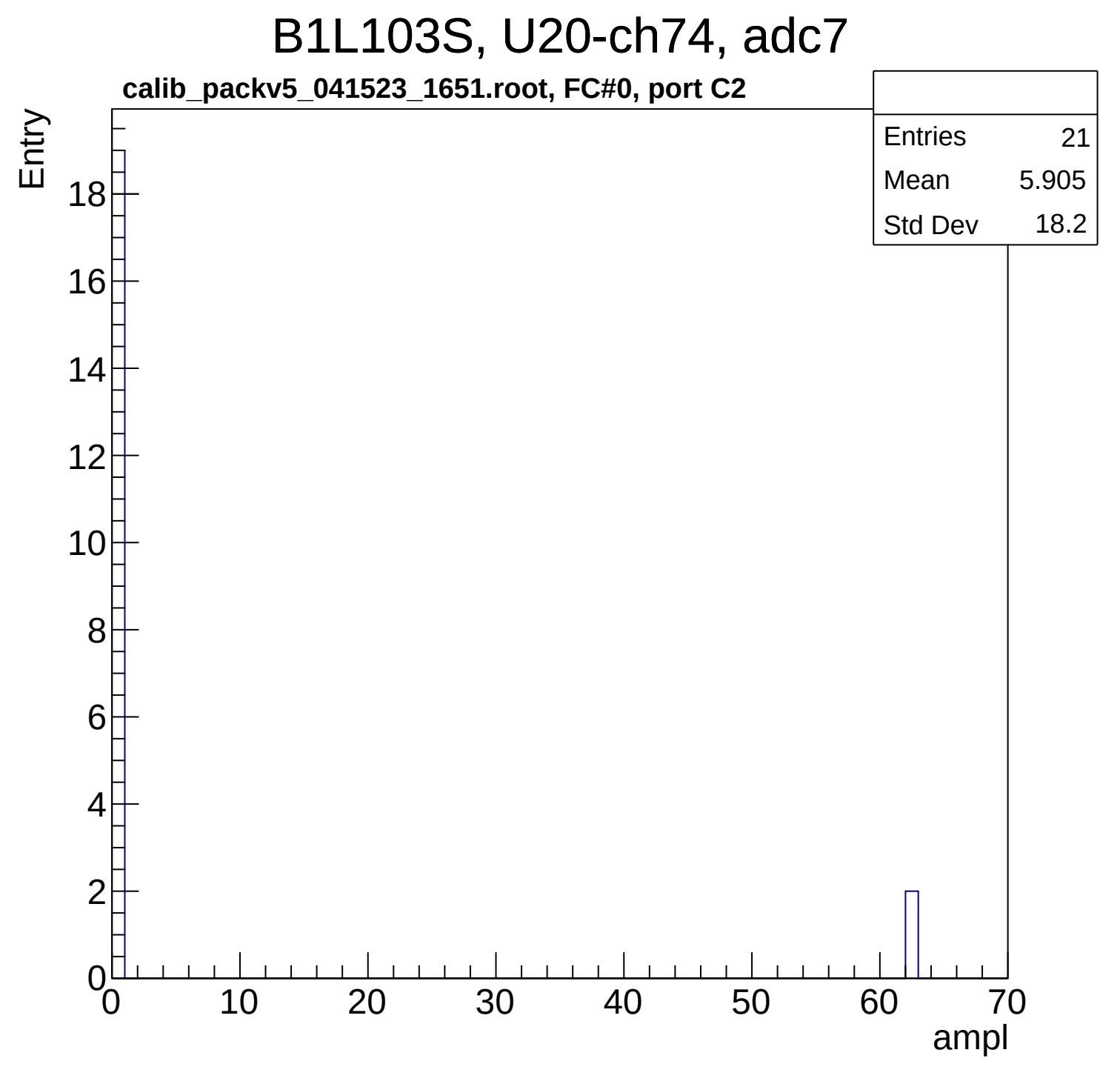
50
60
70
ampl


B1L103S, U20-ch74, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.905
Std Dev 18.2
Entry
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6
8
10
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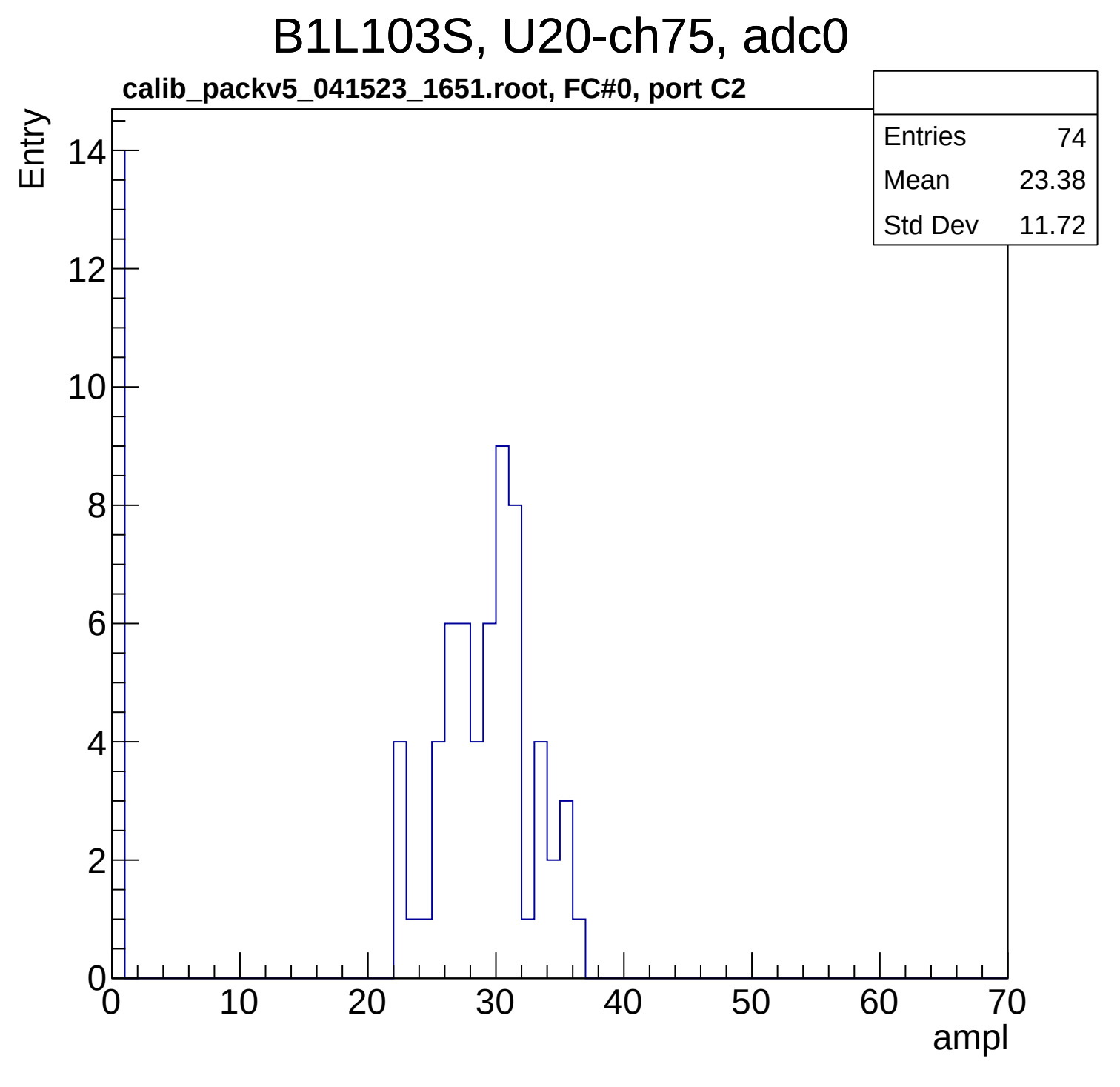
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch75, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 23.38
Std Dev 11.72
Entry
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4
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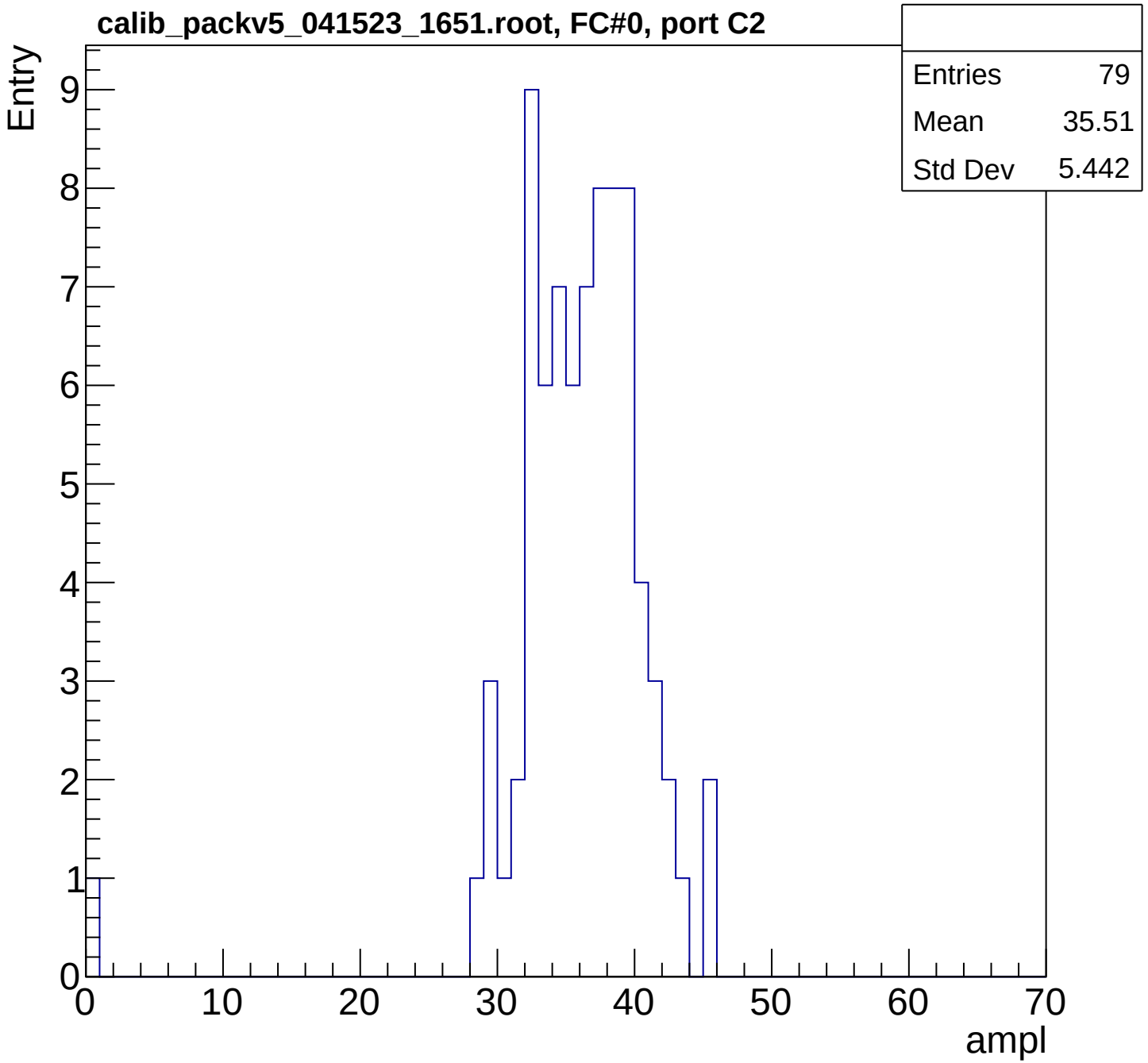
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch75, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 35.51
Std Dev 5.442
Entry
ampl
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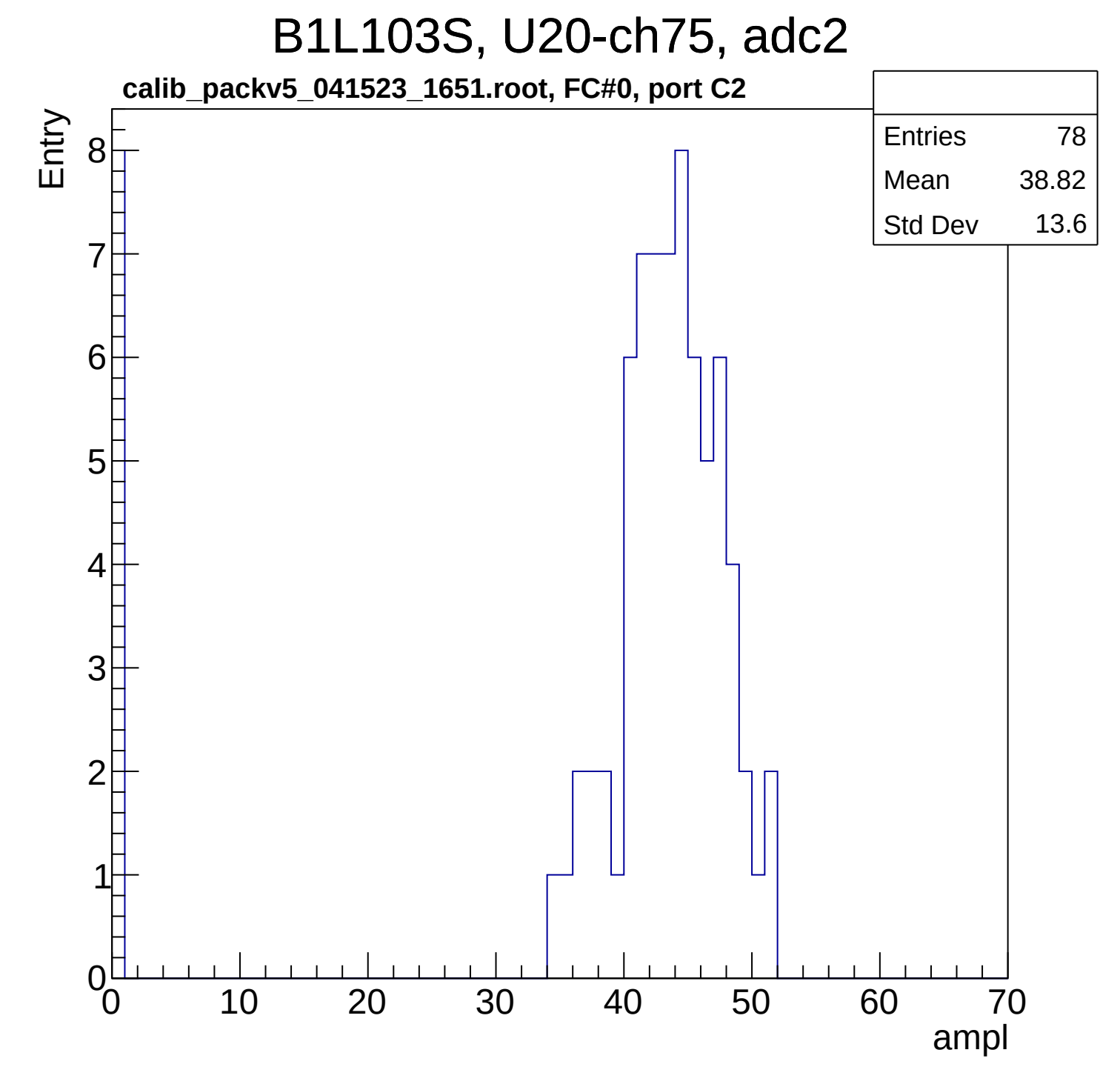
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch75, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 38.82
Std Dev 13.6
Entry
ampl
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2
3
4
5
6
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0
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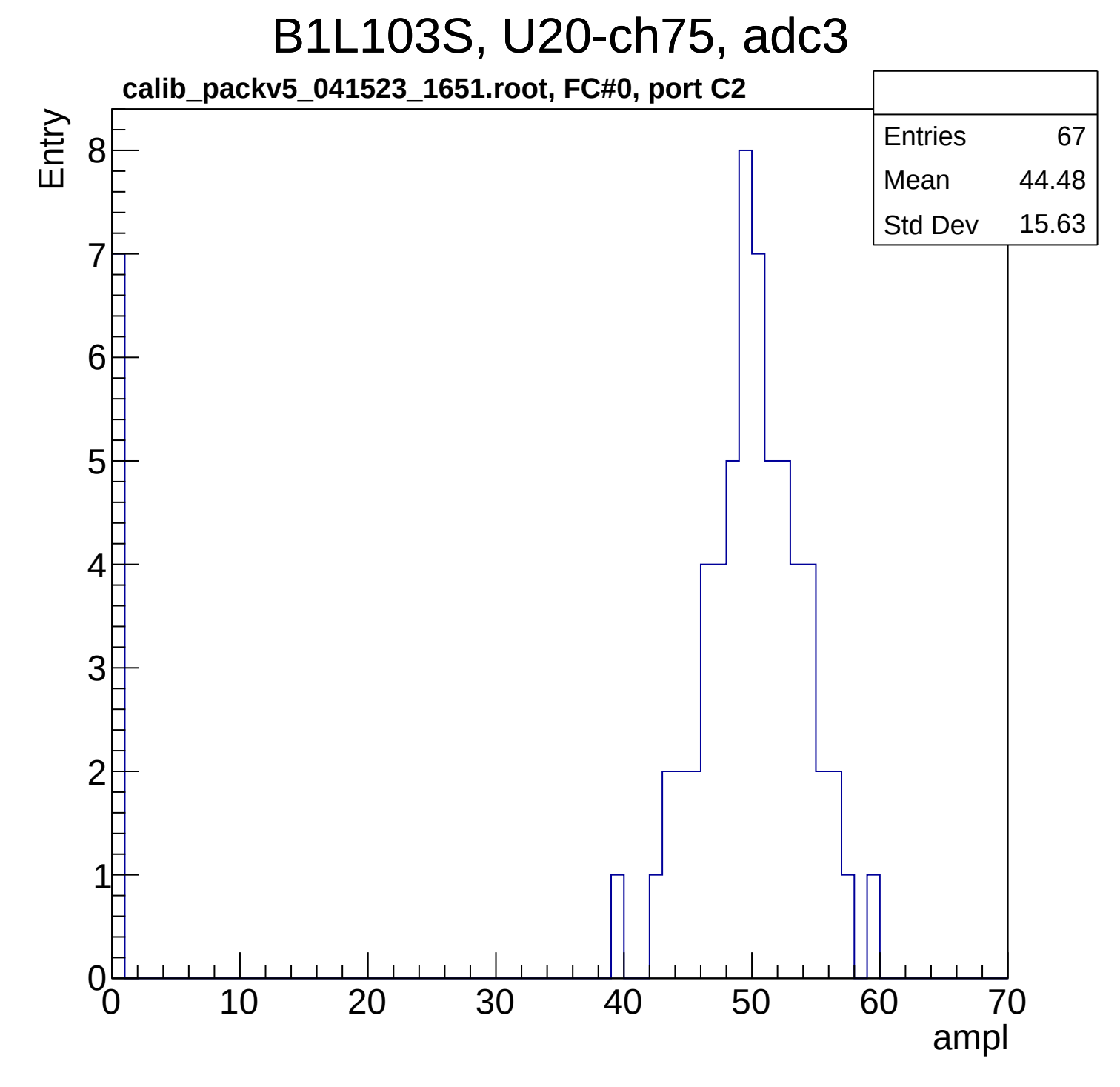
B1L103S, U20-ch75, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 44.48
Std Dev 15.63
Entry
ampl
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2
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4
5
6
7
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0
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20
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40
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60
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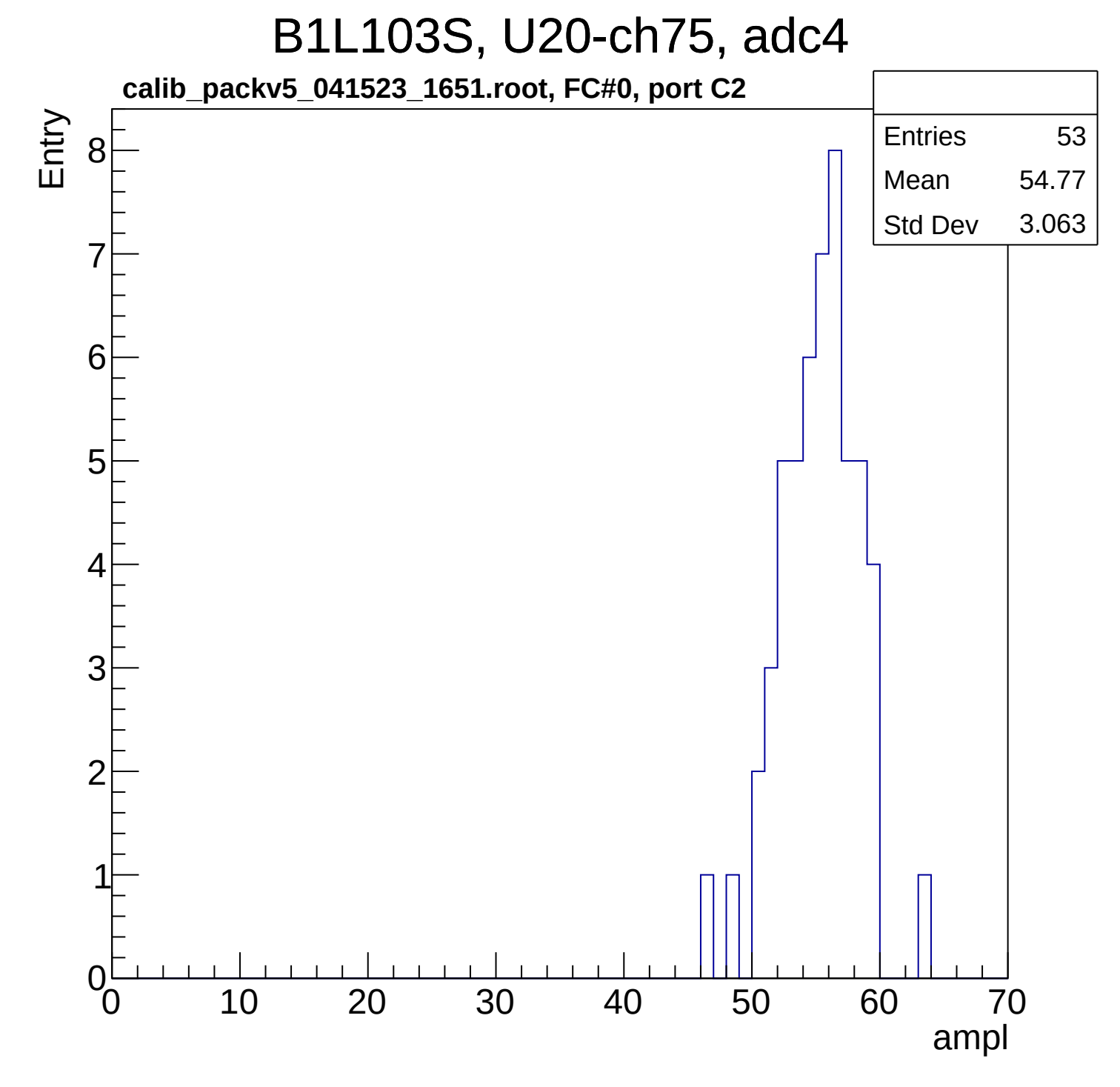
B1L103S, U20-ch75, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 54.77
Std Dev 3.063
Entry
ampl
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1
2
3
4
5
6
7
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0
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40
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60
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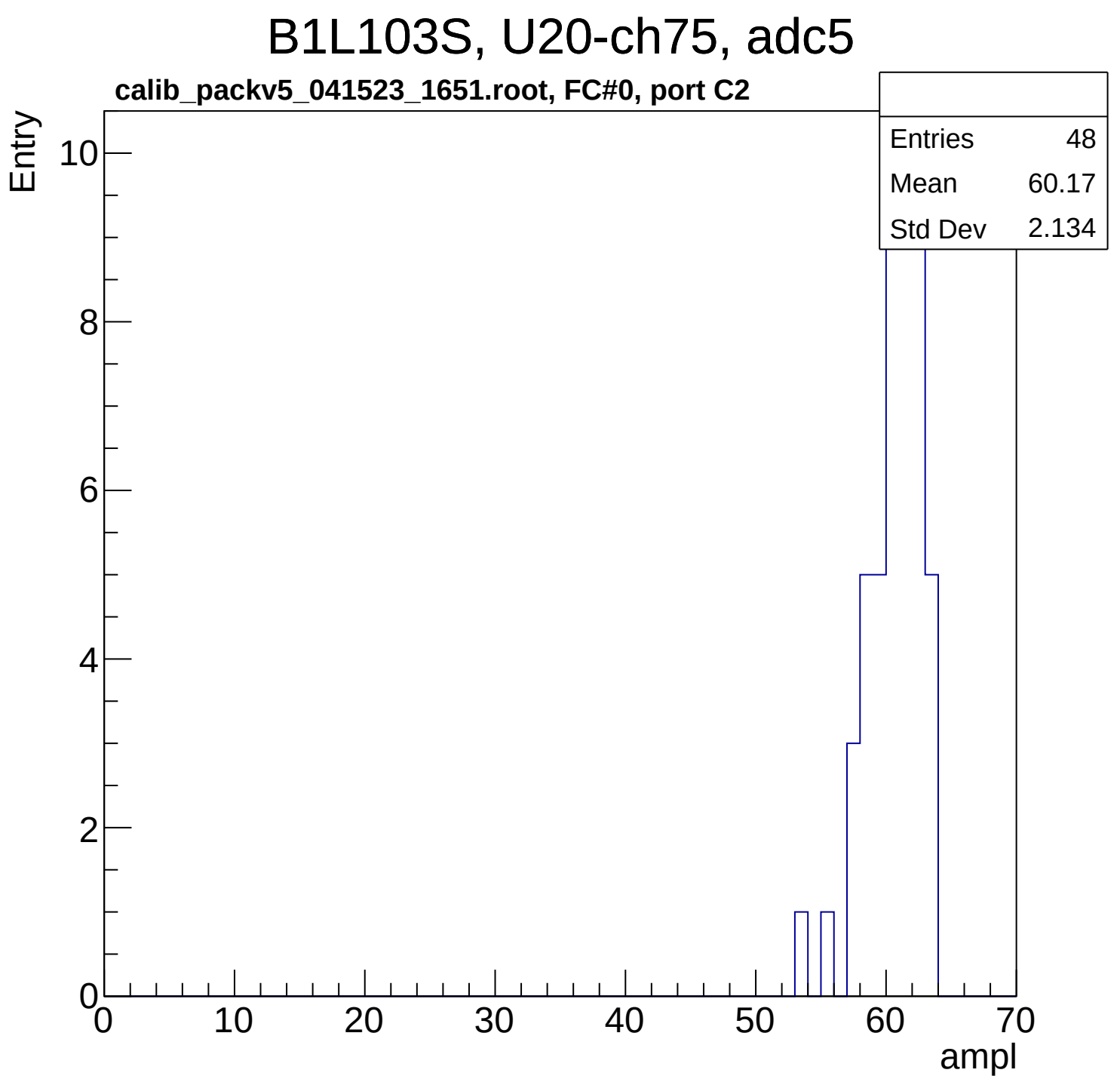
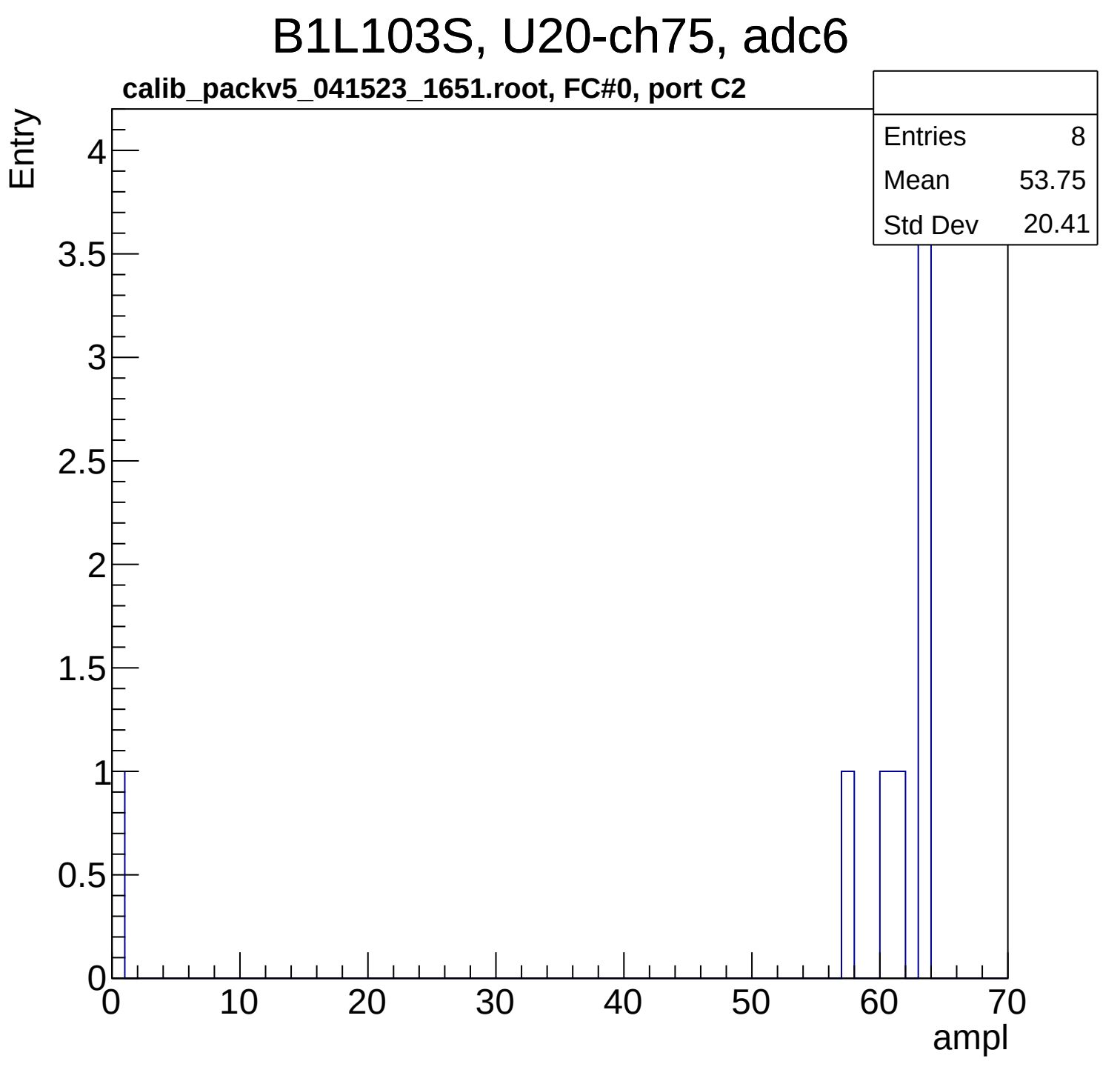

B1L103S, U20-ch75, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 60.17
Std Dev 2.134
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U20-ch75, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 53.75
Std Dev 20.41
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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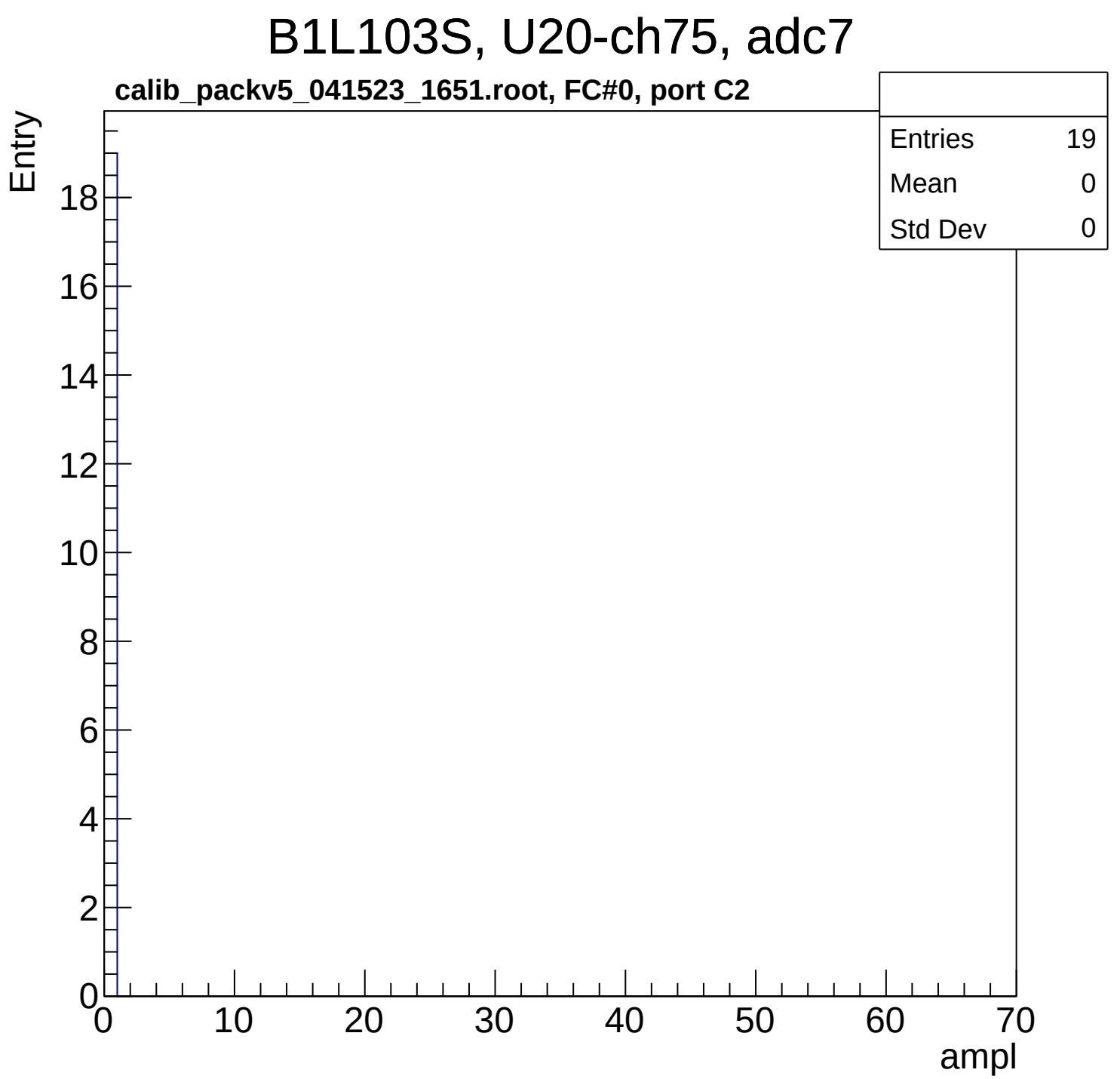
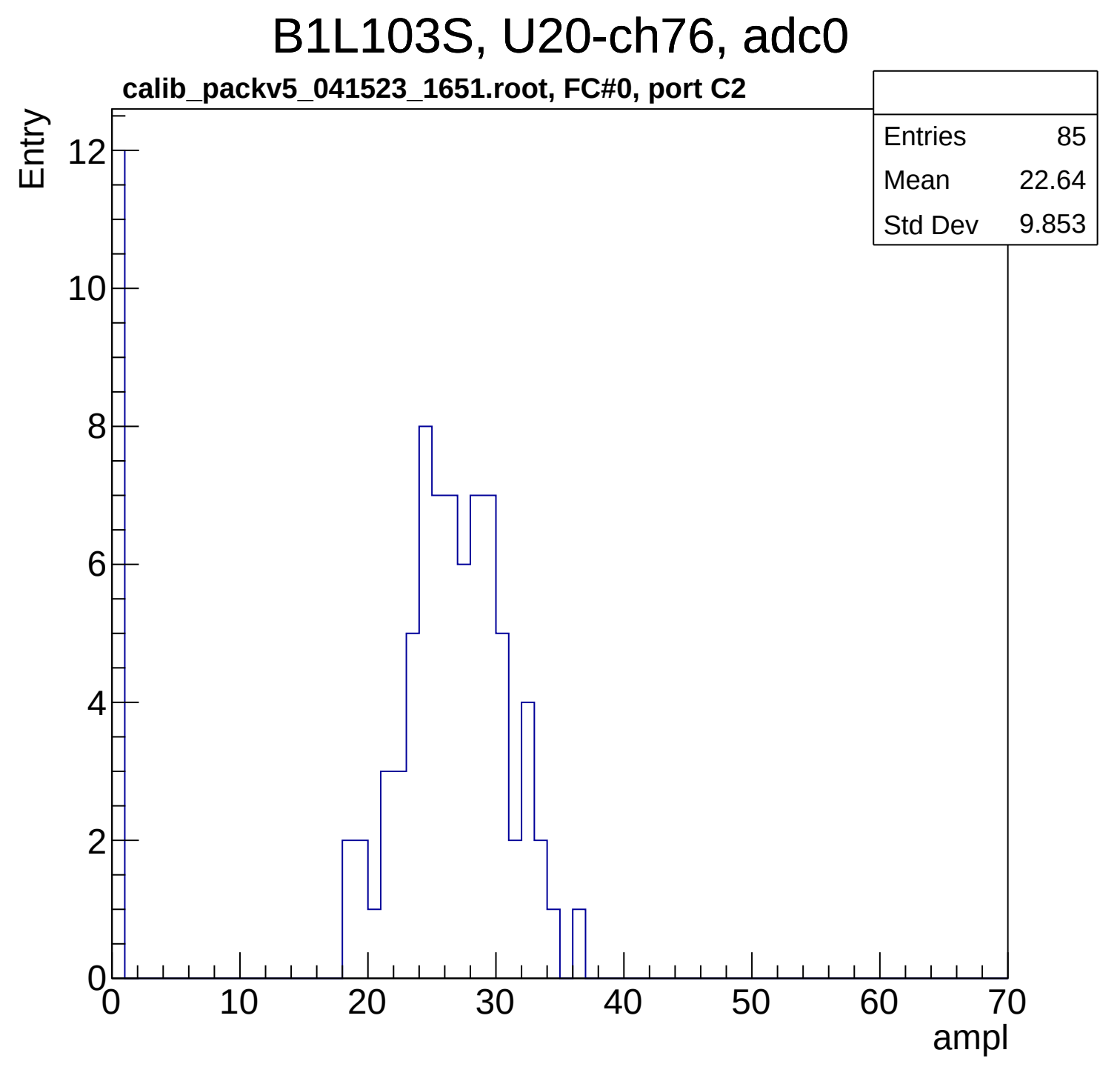
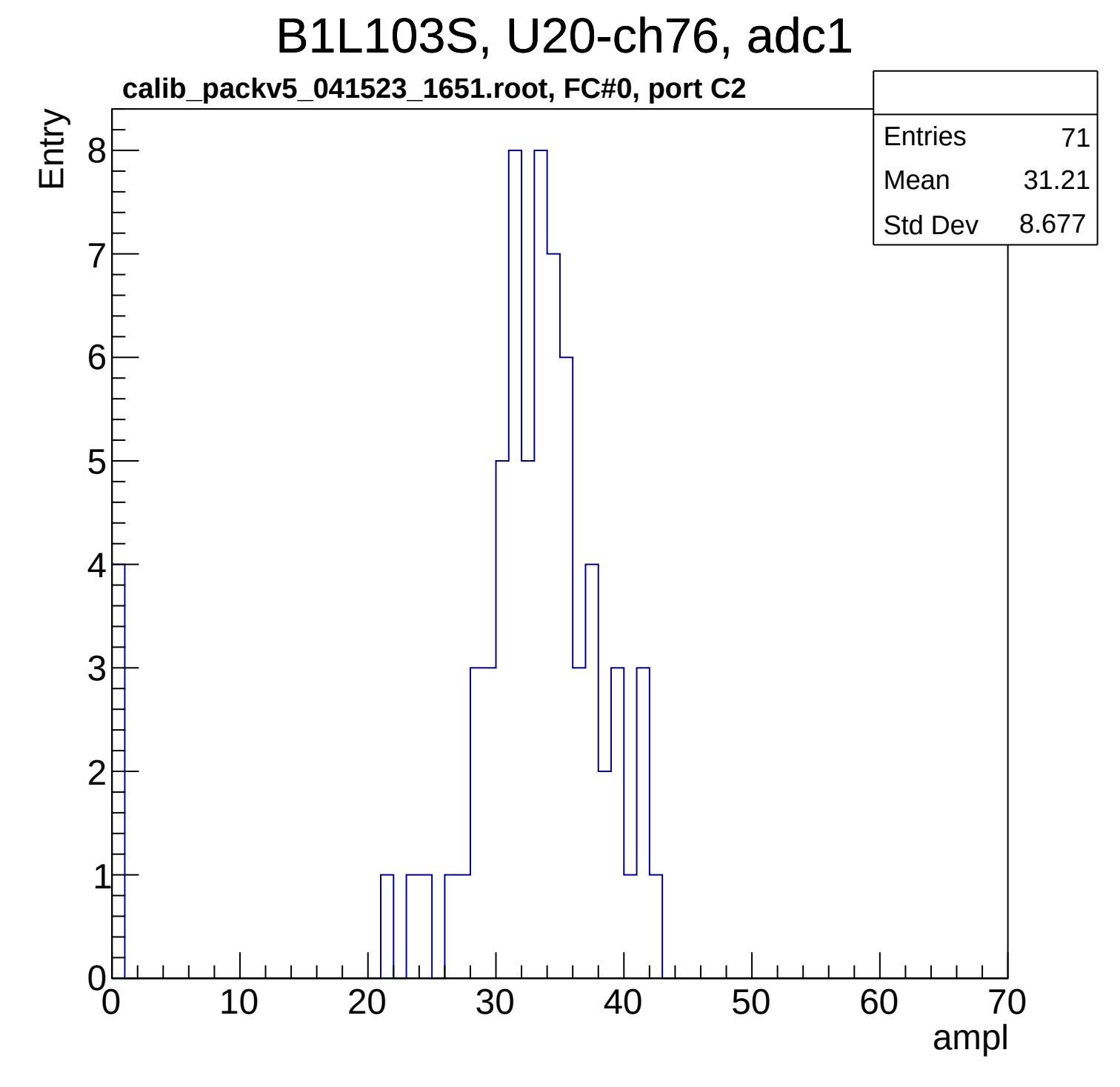

B1L103S, U20-ch75, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch76, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 22.64
Std Dev 9.853
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U20-ch76, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 31.21
Std Dev 8.677
Entry
ampl
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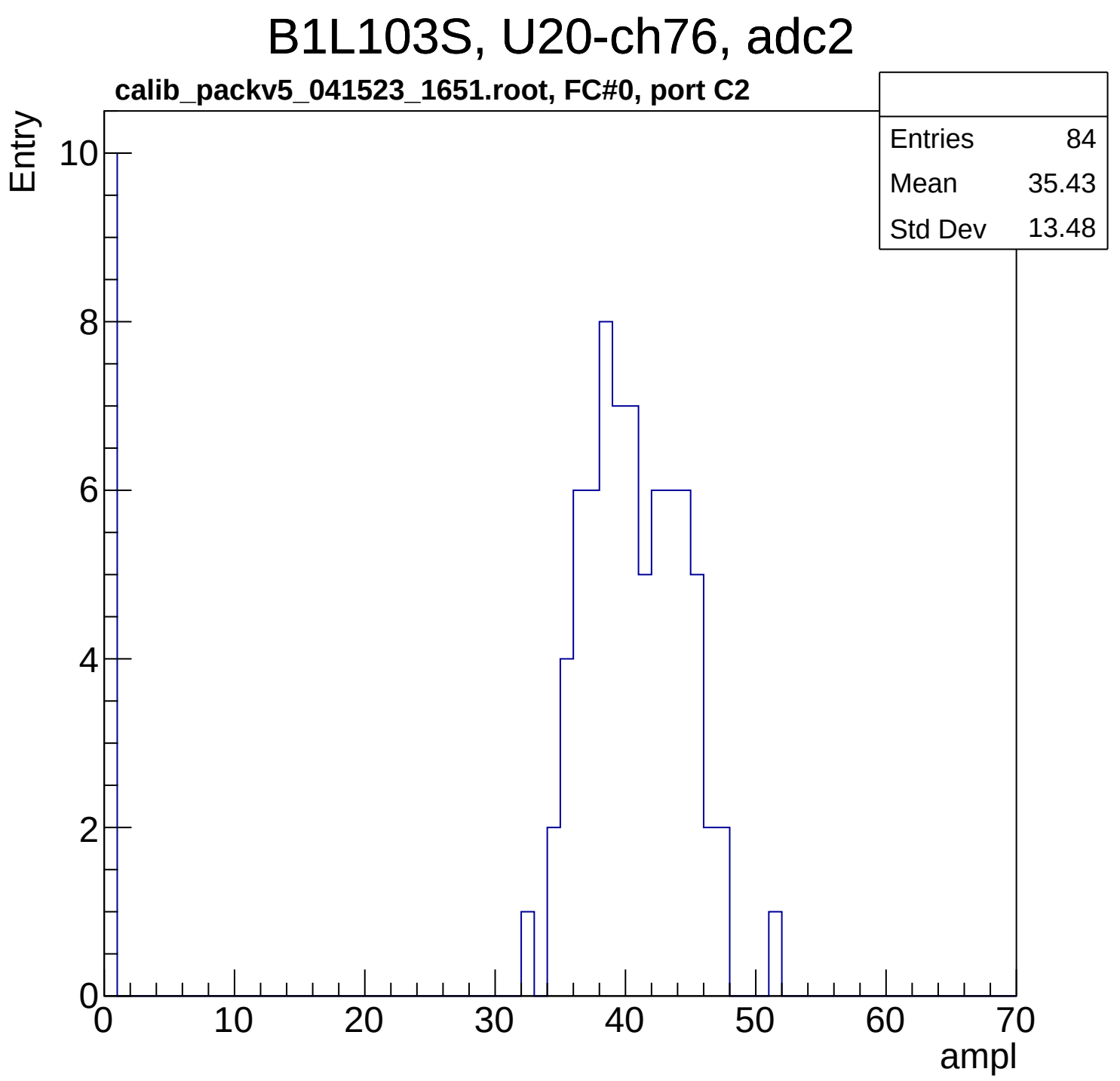
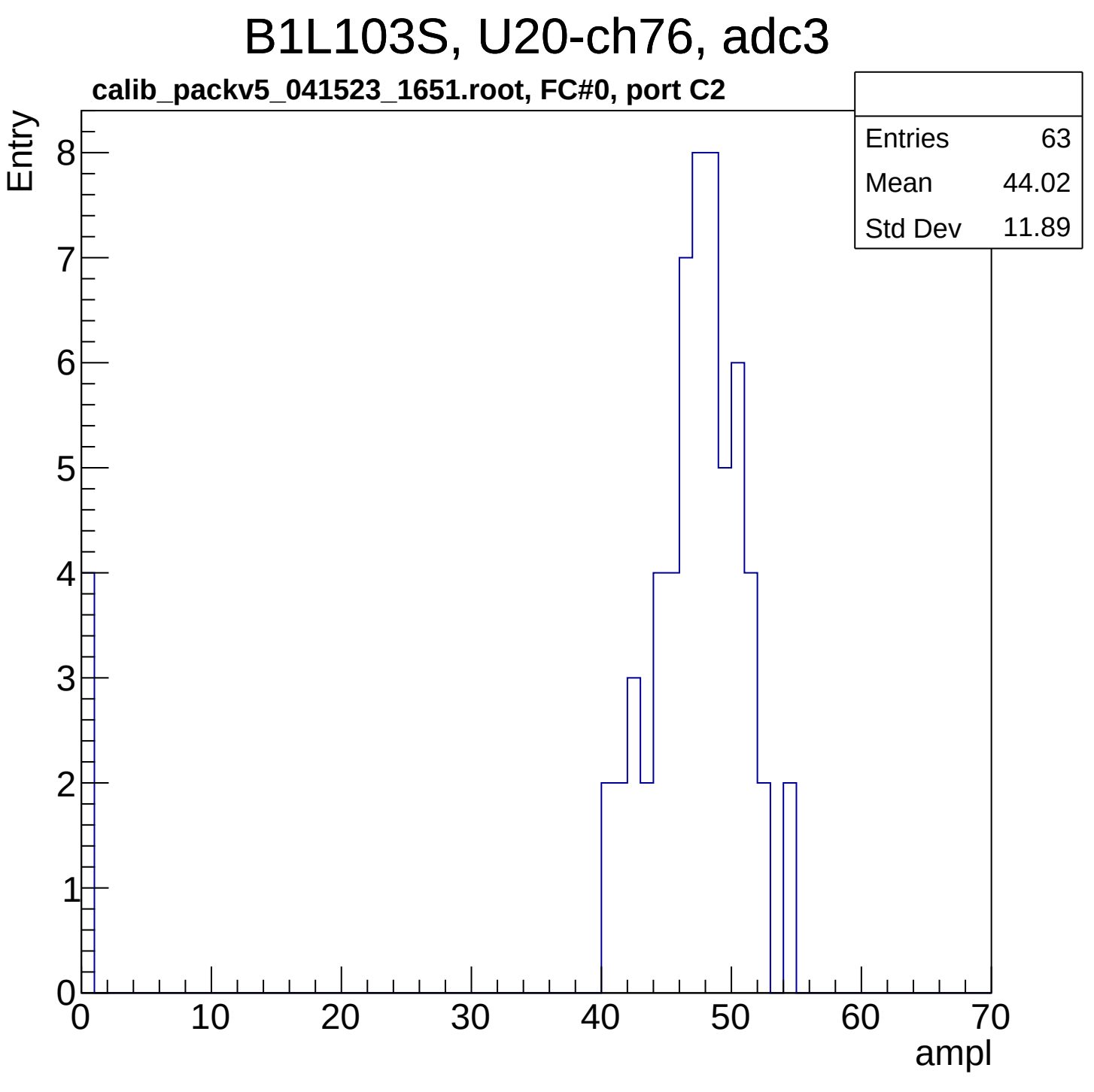
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch76, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 35.43
Std Dev 13.48
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U20-ch76, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 44.02
Std Dev 11.89
Entry
ampl
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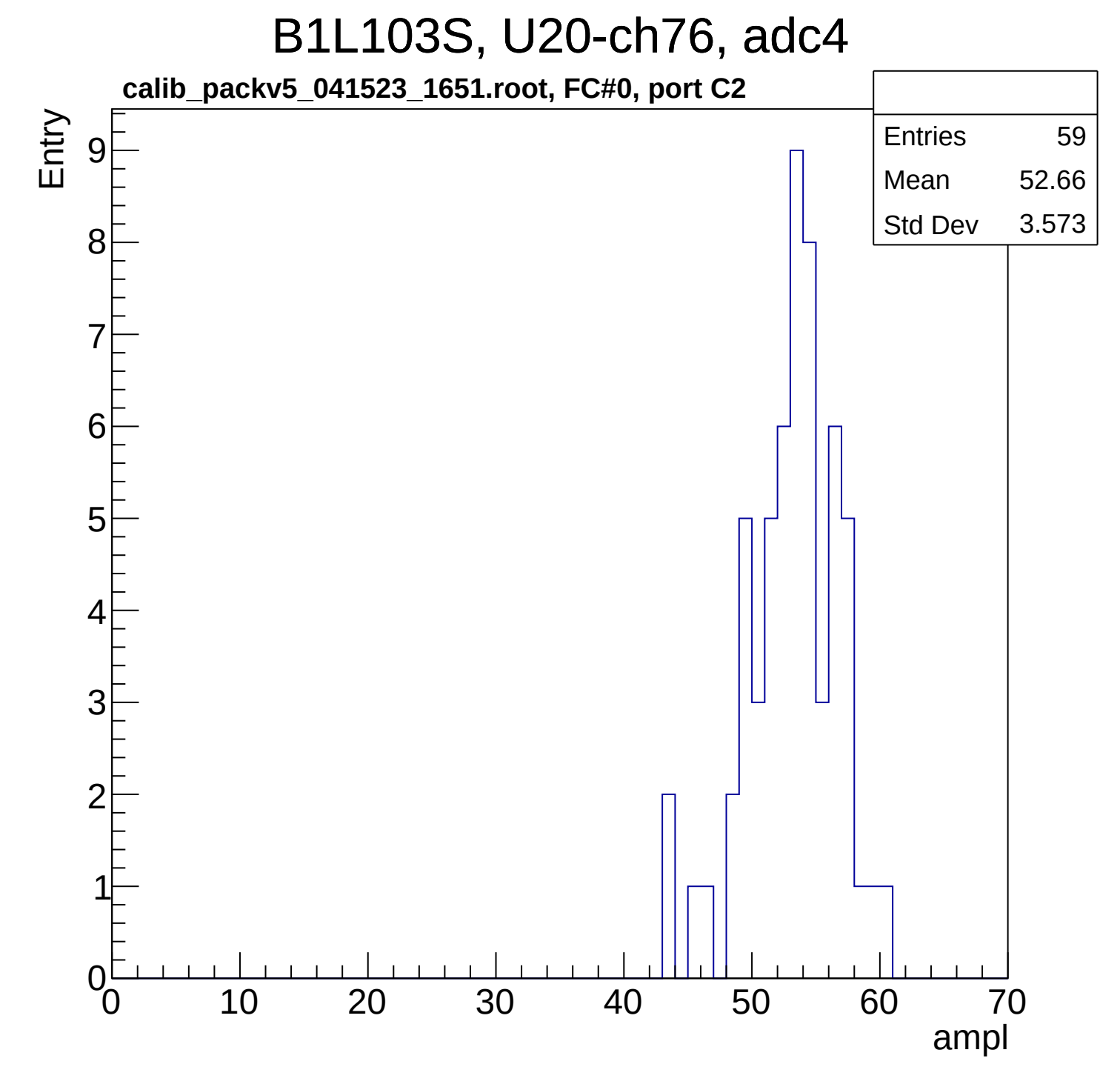
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch76, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 52.66
Std Dev 3.573
Entry
ampl
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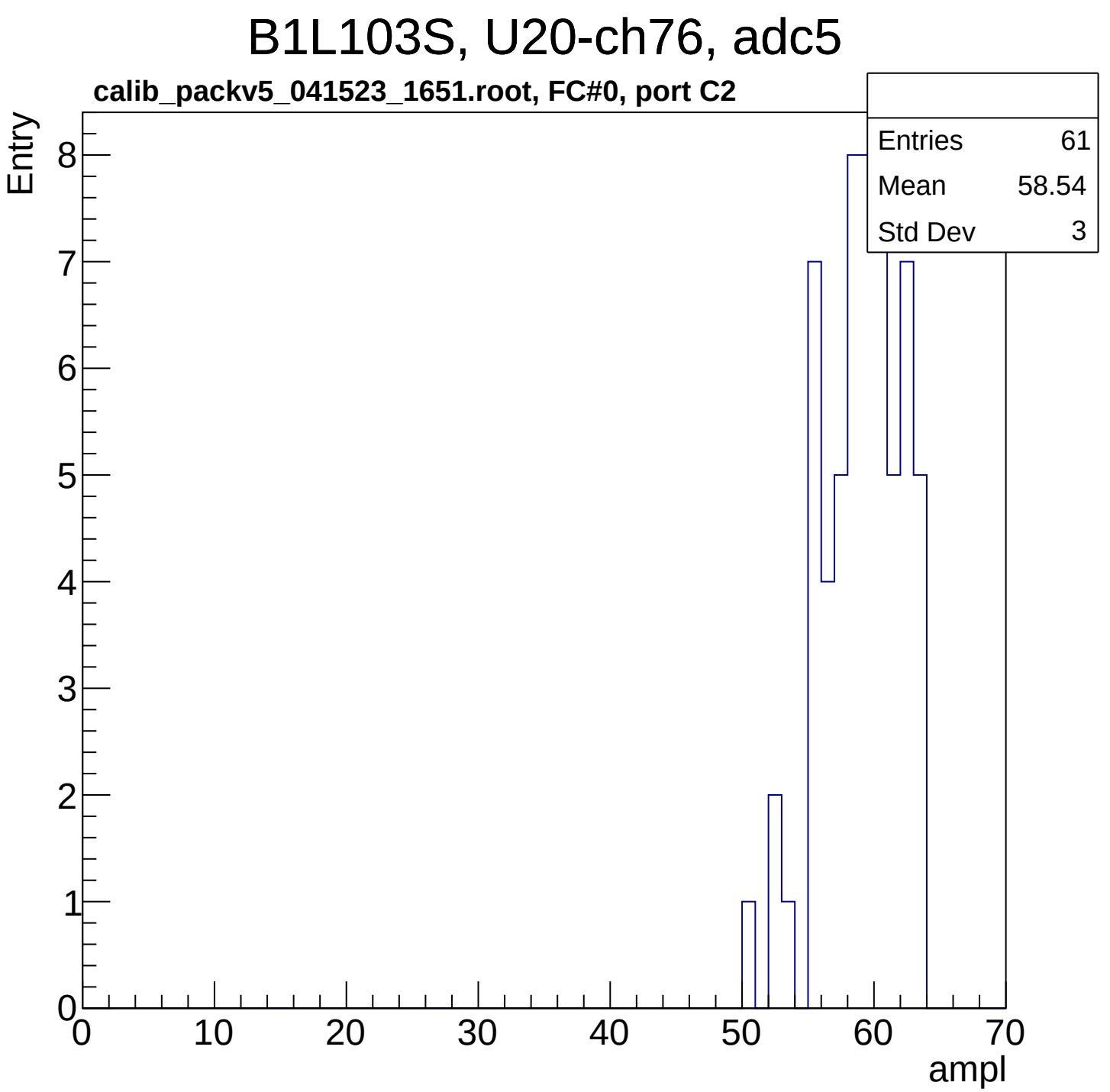
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch76, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 58.54
Std Dev 3
Entry
ampl
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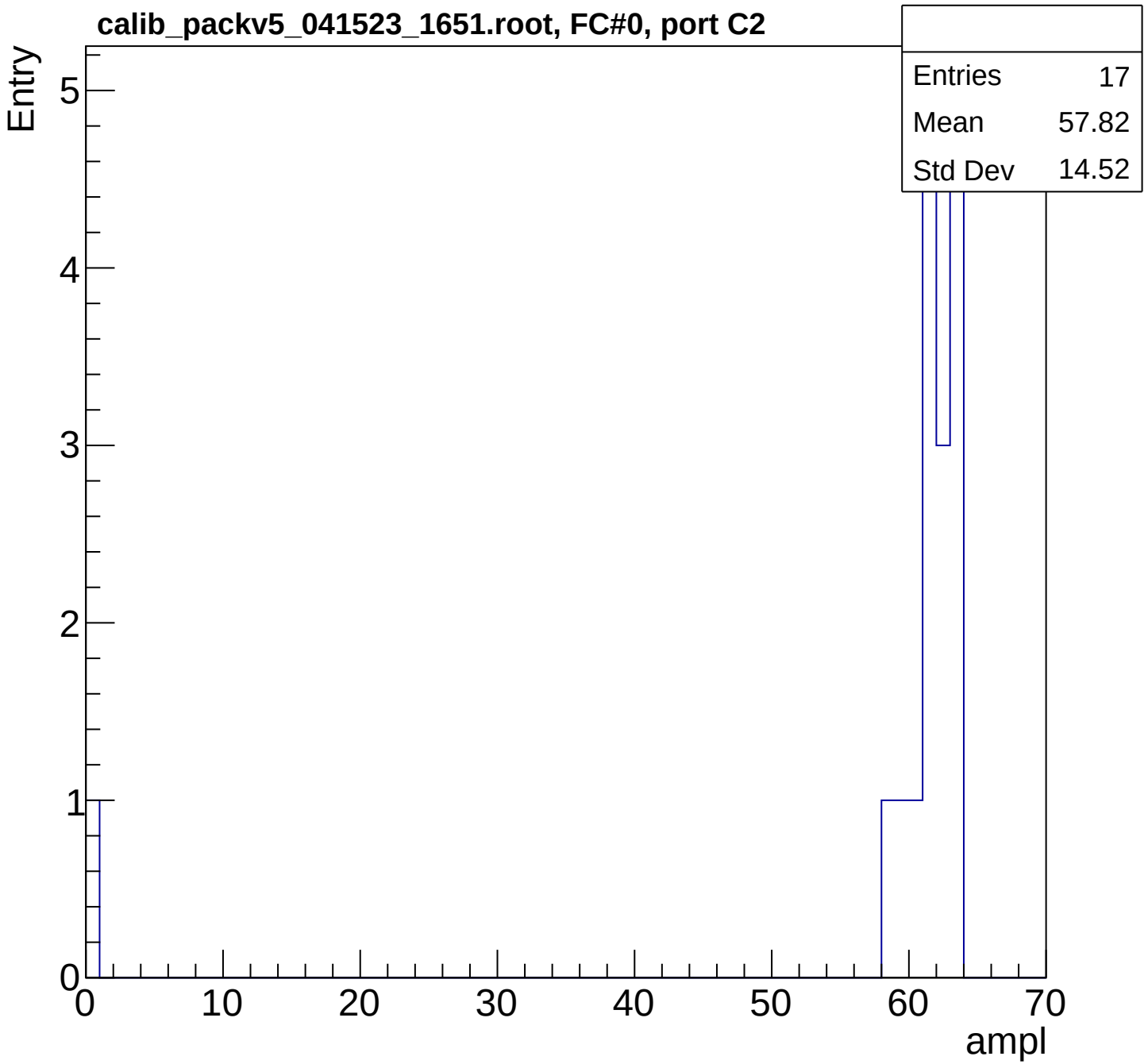
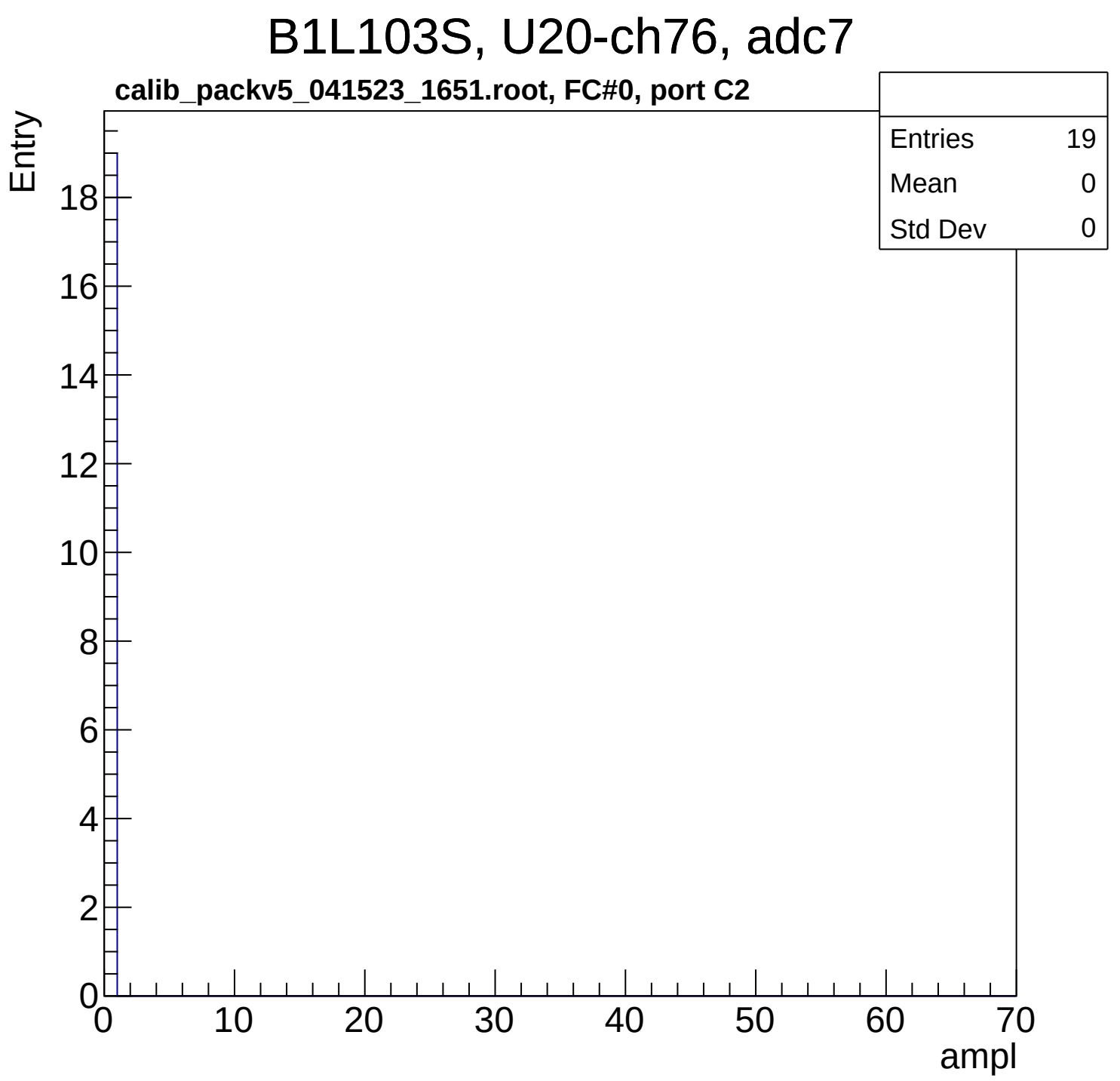
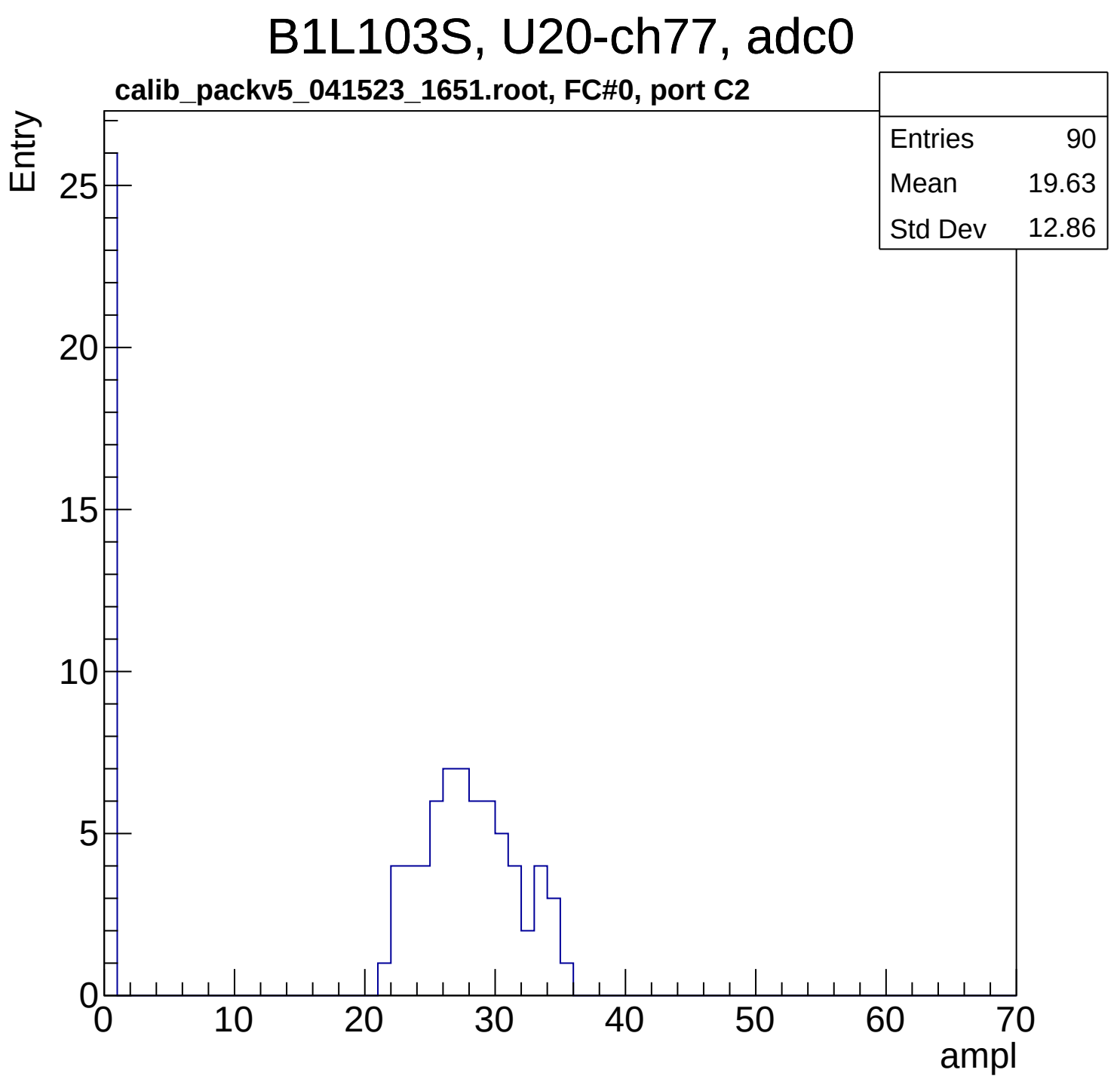
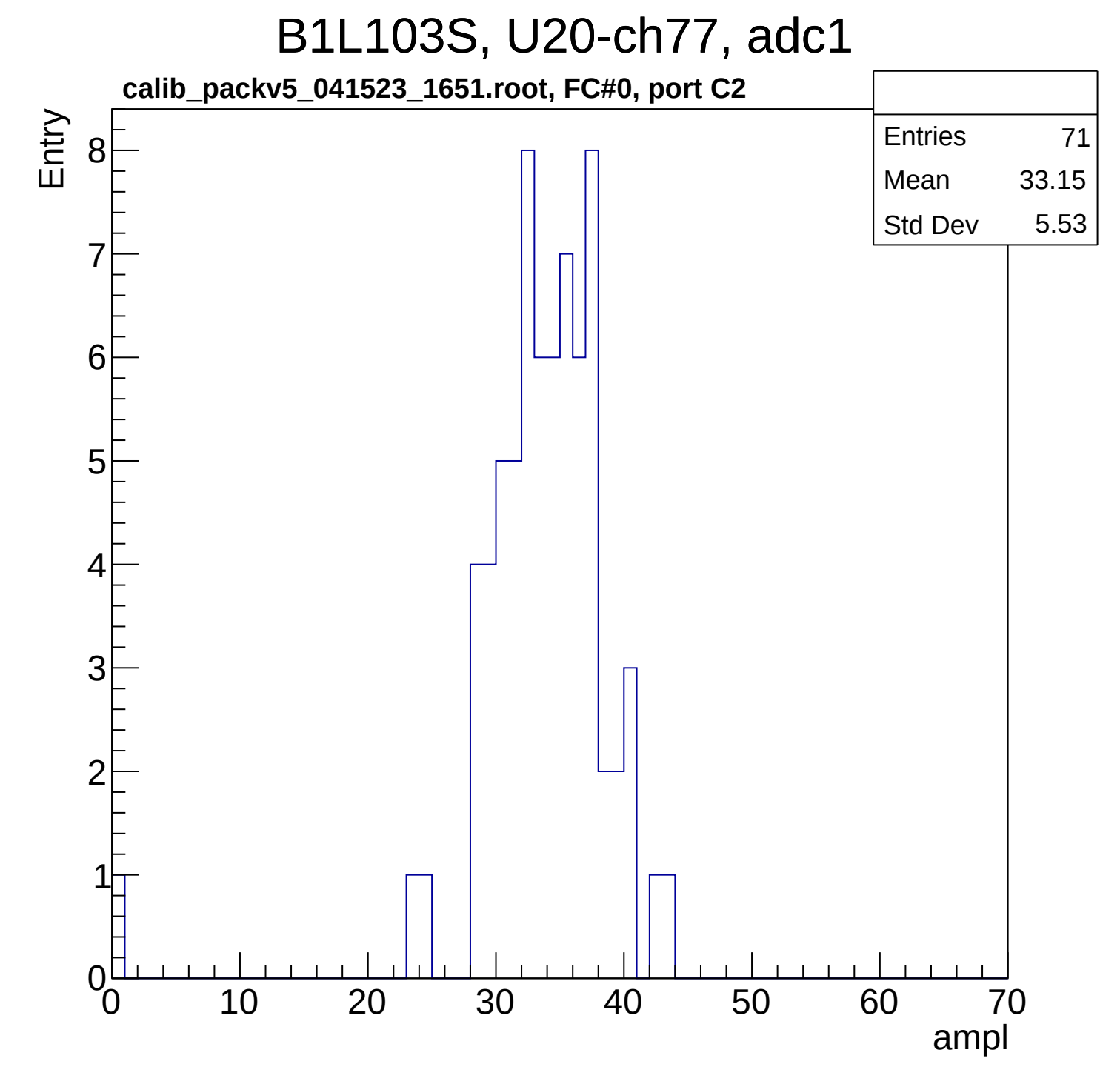
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch76, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 57.82
Std Dev 14.52
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch76, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch77, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 19.63
Std Dev 12.86
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch77, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 33.15
Std Dev 5.53
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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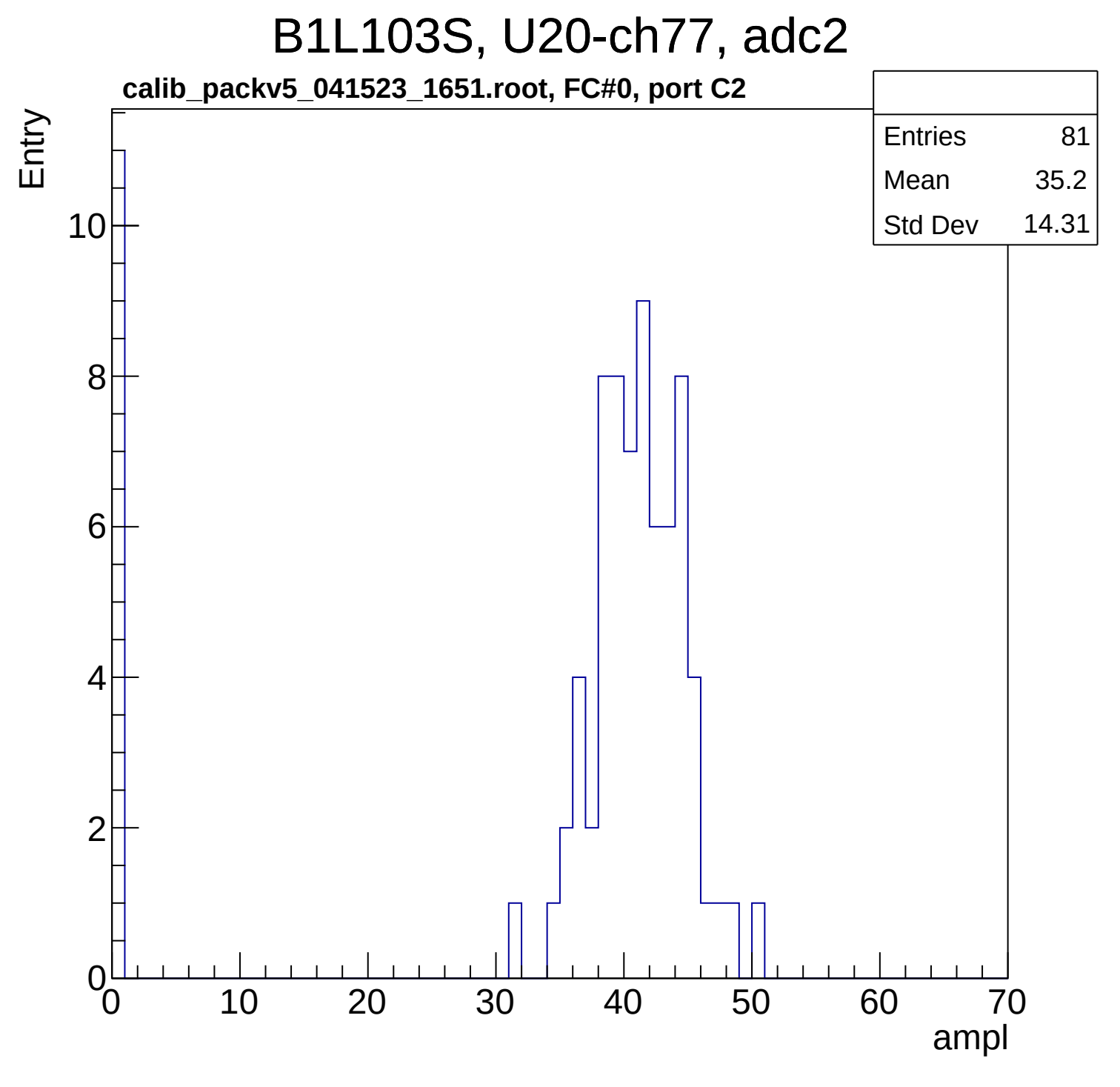
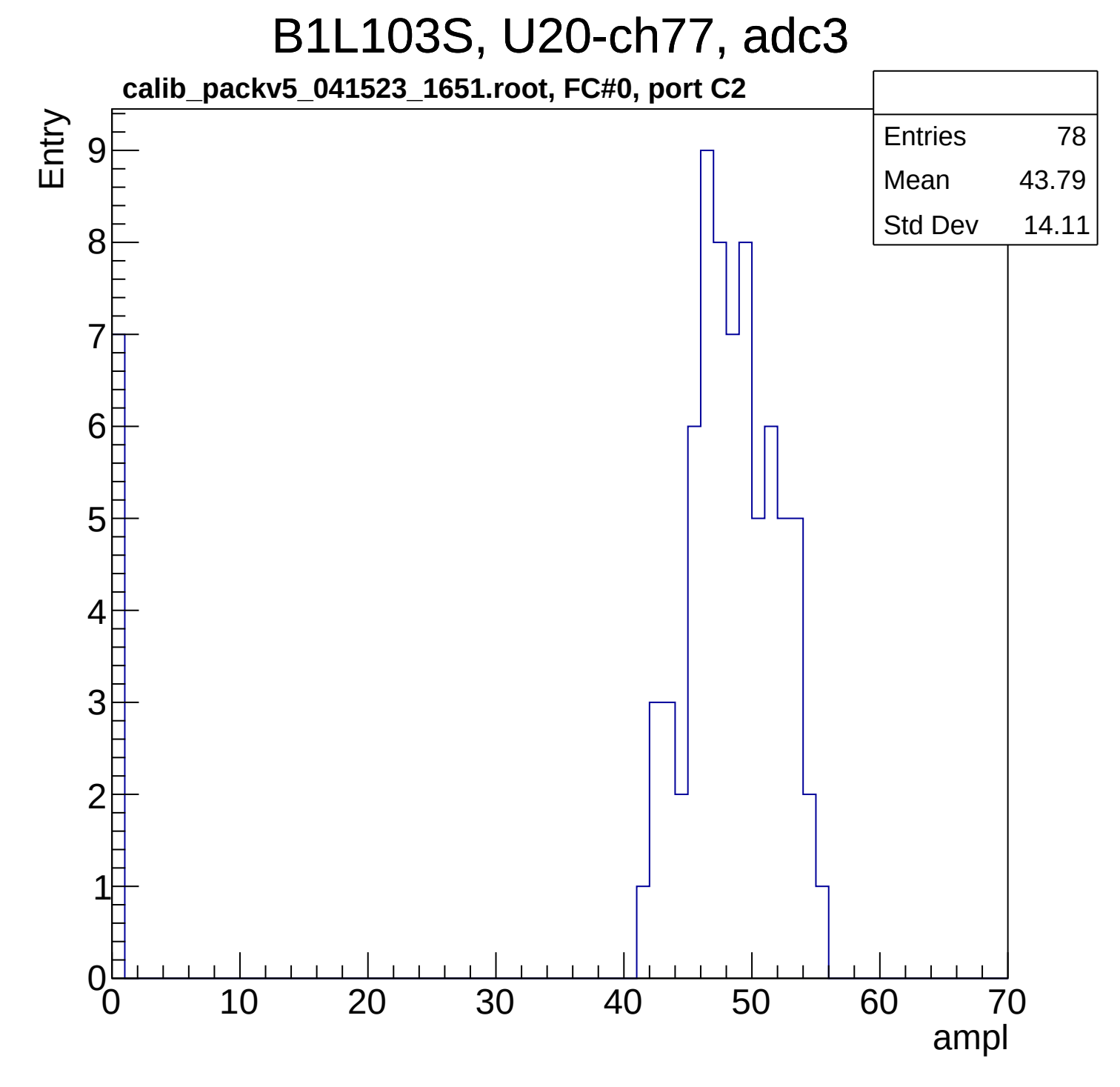

B1L103S, U20-ch77, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 35.2
Std Dev 14.31
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch77, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 43.79
Std Dev 14.11
Entry
ampl
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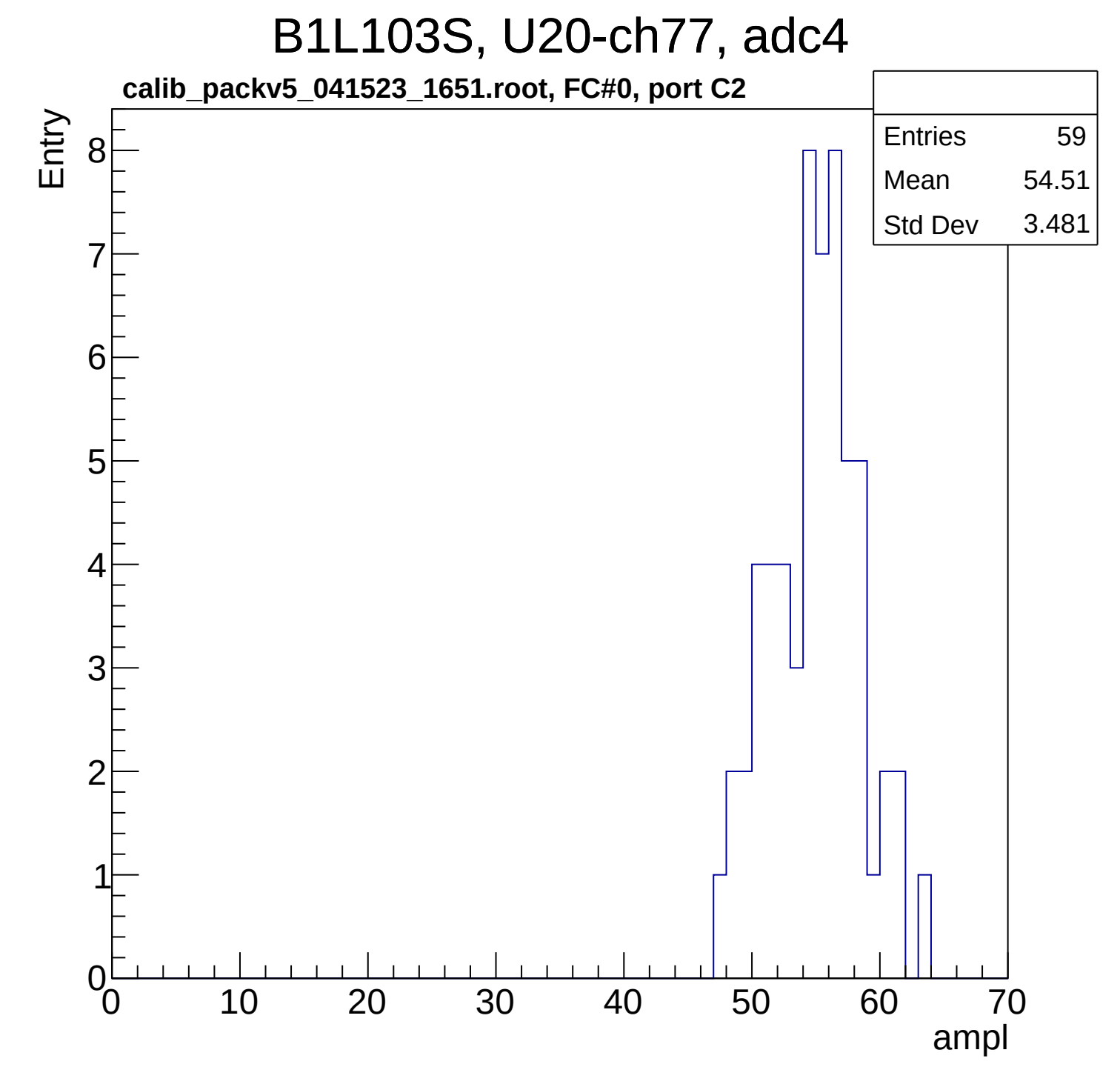
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch77, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 54.51
Std Dev 3.481
Entry
ampl
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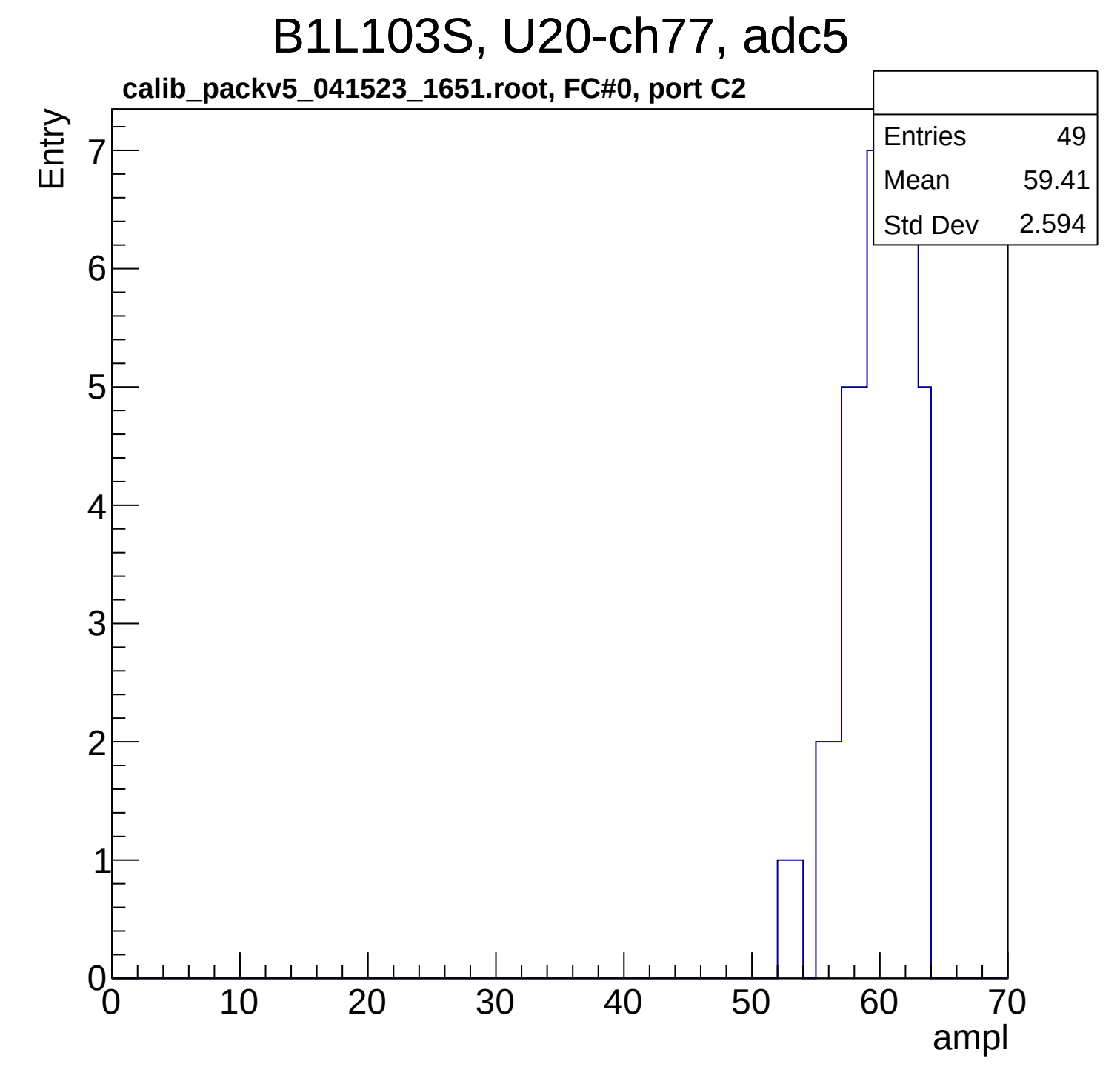
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch77, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 59.41
Std Dev 2.594
Entry
ampl
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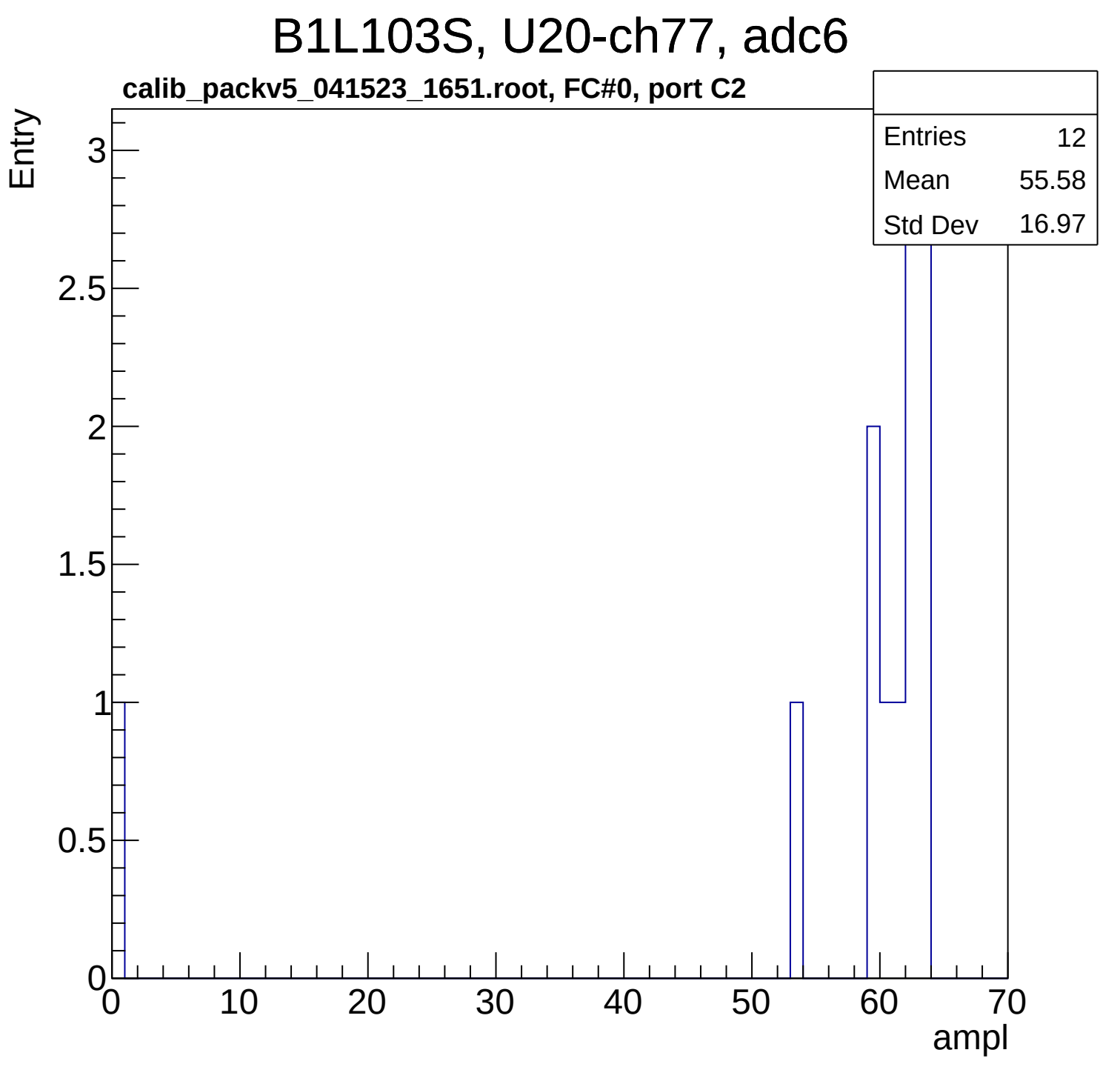
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U20-ch77, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 55.58
Std Dev 16.97
Entry
ampl
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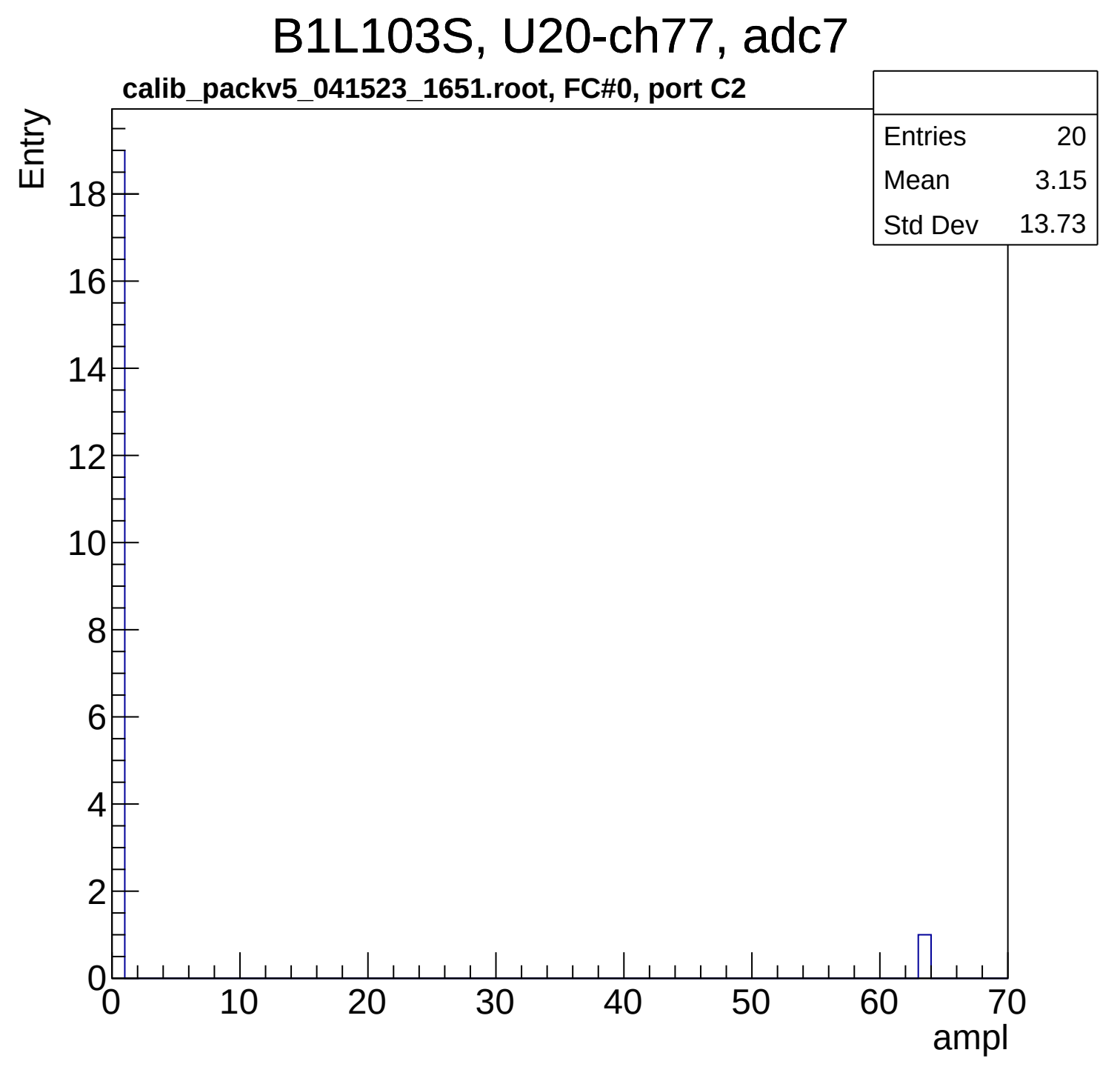
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U20-ch77, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
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6
8
10
12
14
16
18
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10
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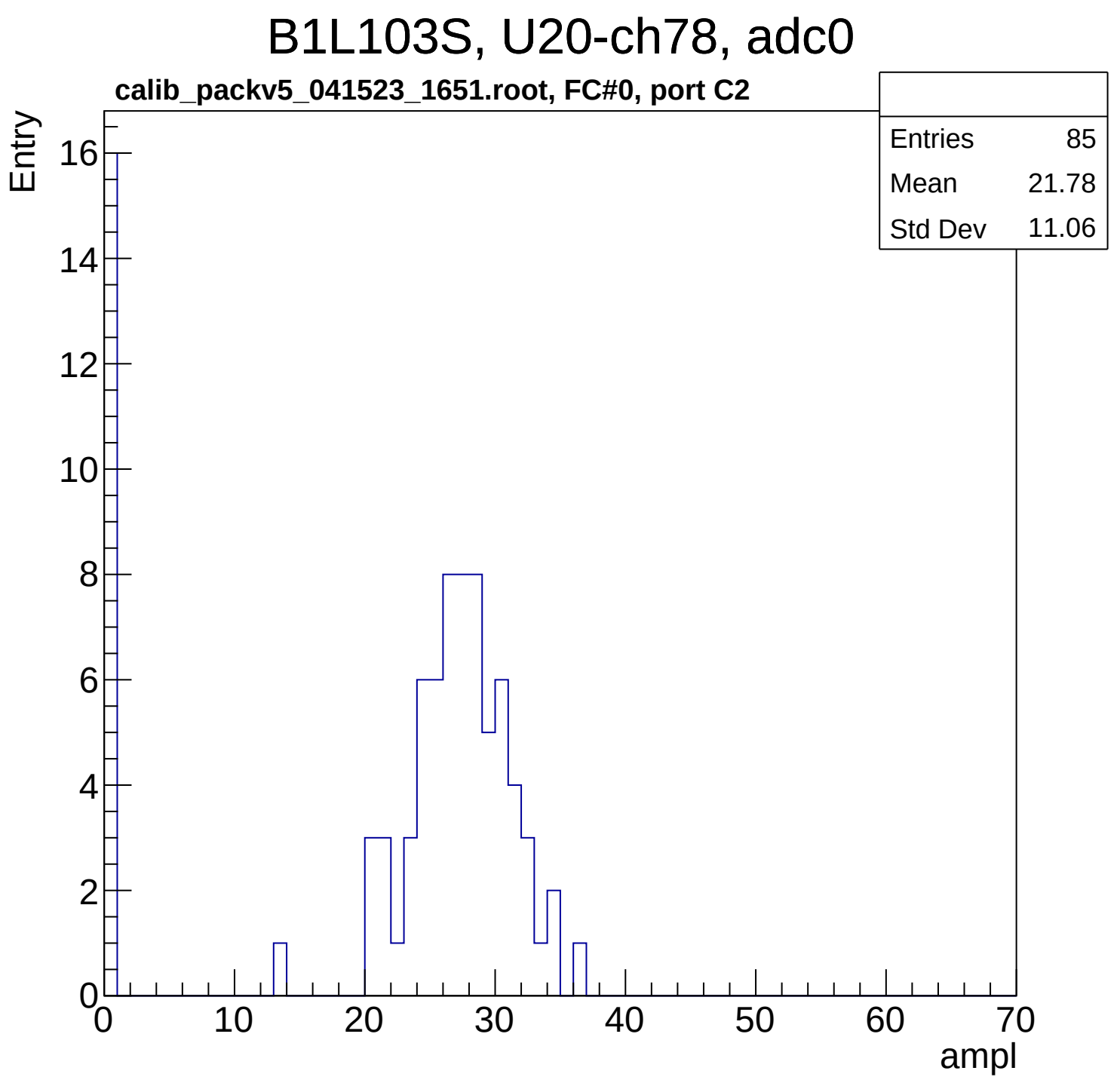
30
40
50
60
70
ampl


B1L103S, U20-ch78, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 21.78
Std Dev 11.06
Entry
ampl
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4
6
8
10
12
14
16
0
10
20
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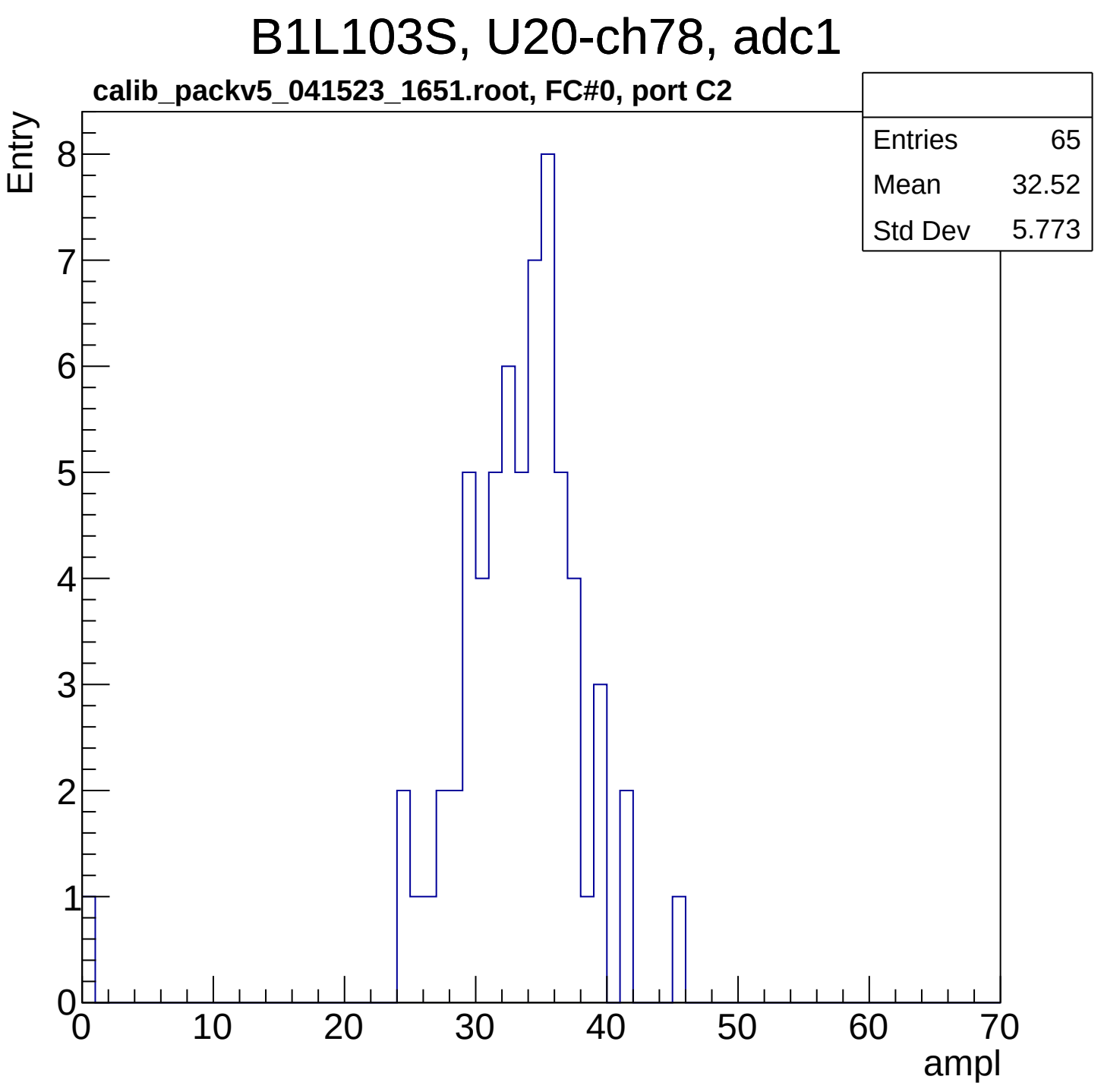
40
50
60
70


B1L103S, U20-ch78, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 32.52
Std Dev 5.773
Entry
ampl
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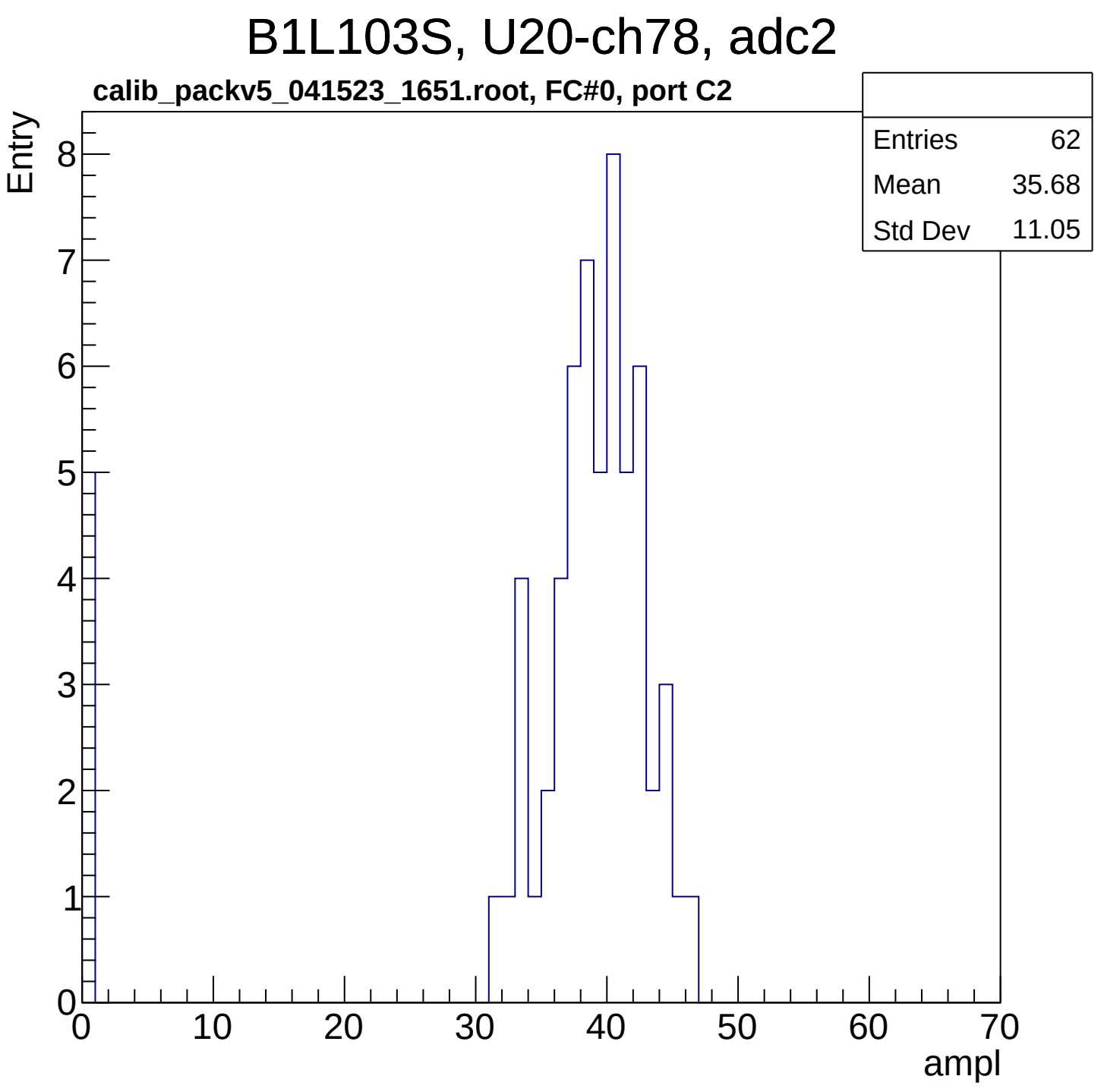
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch78, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 35.68
Std Dev 11.05
Entry
ampl
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2
3
4
5
6
7
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0
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20
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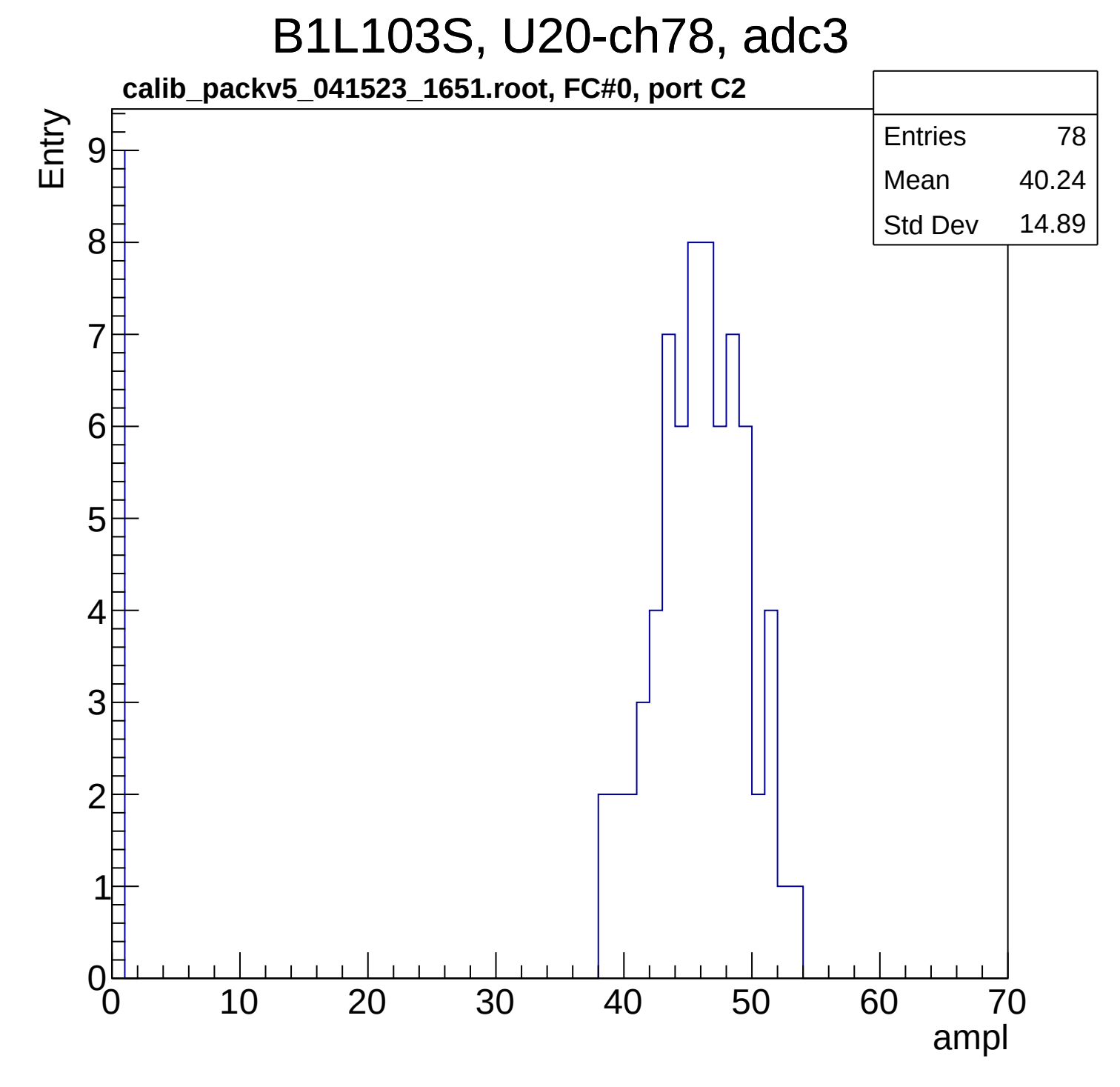
40
50
60
70


B1L103S, U20-ch78, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 40.24
Std Dev 14.89
Entry
ampl
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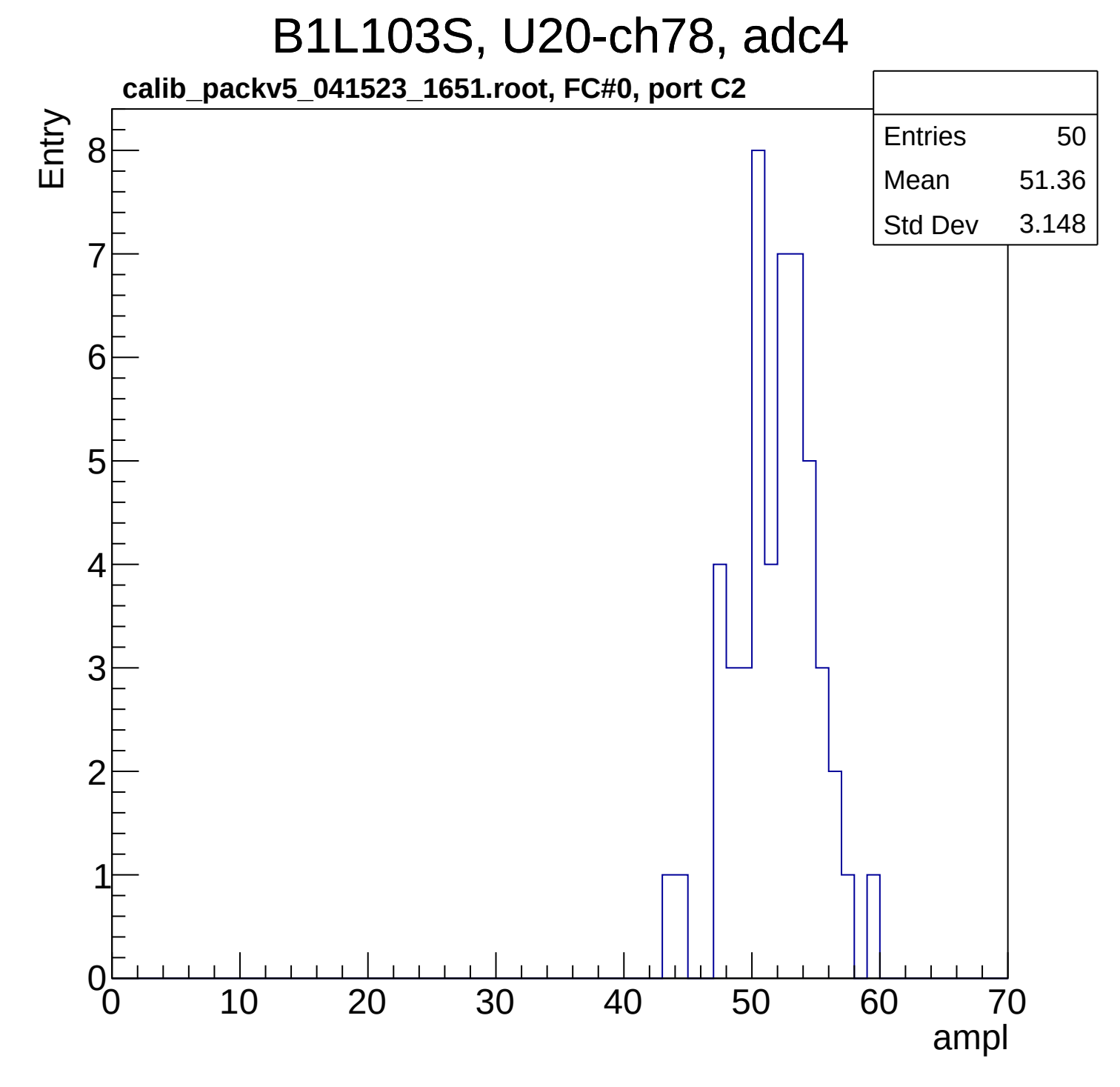
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch78, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 51.36
Std Dev 3.148
Entry
ampl
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1
2
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4
5
6
7
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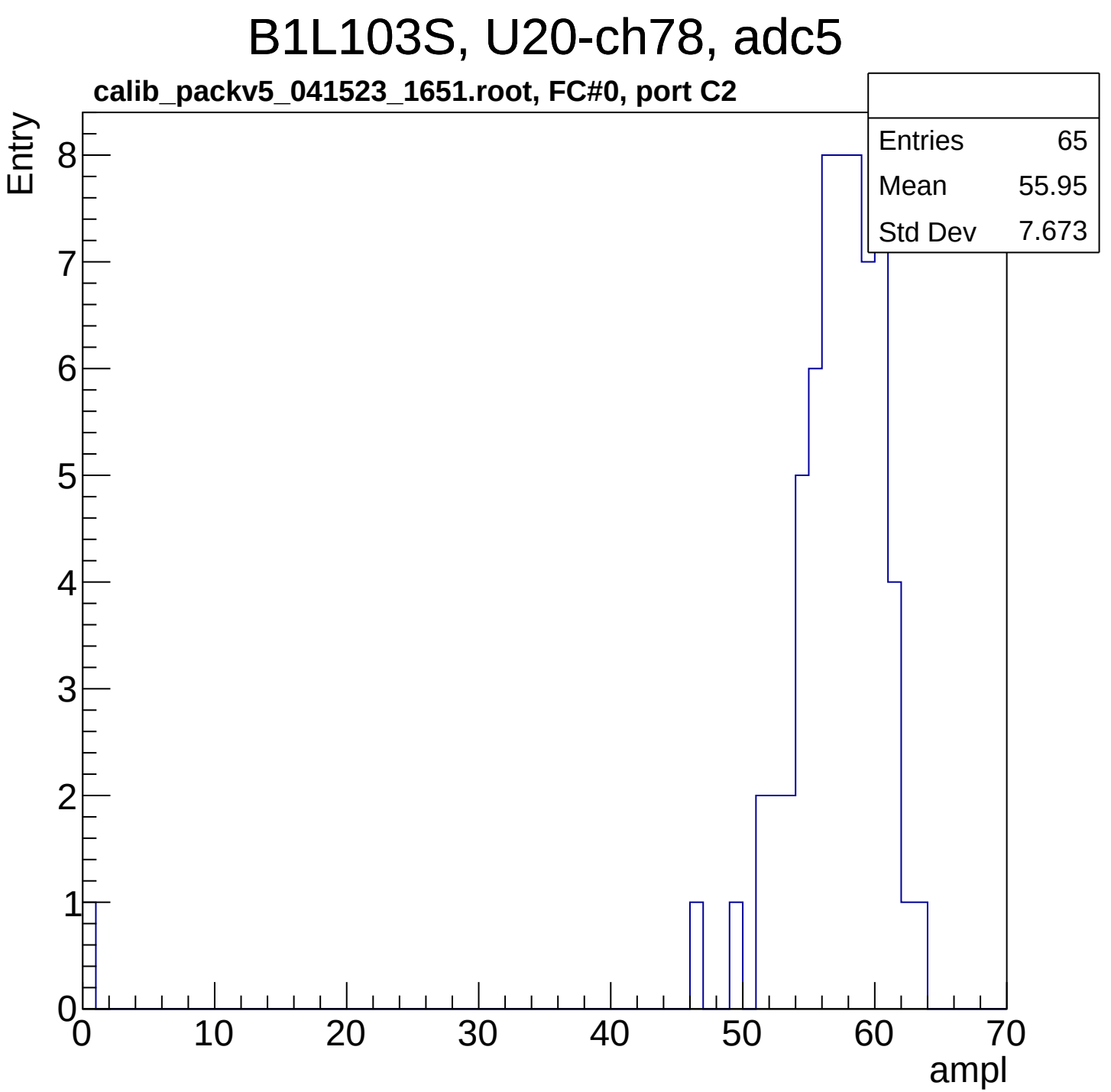
0
10
20
30
40
50
60
70


B1L103S, U20-ch78, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 55.95
Std Dev 7.673
Entry
ampl
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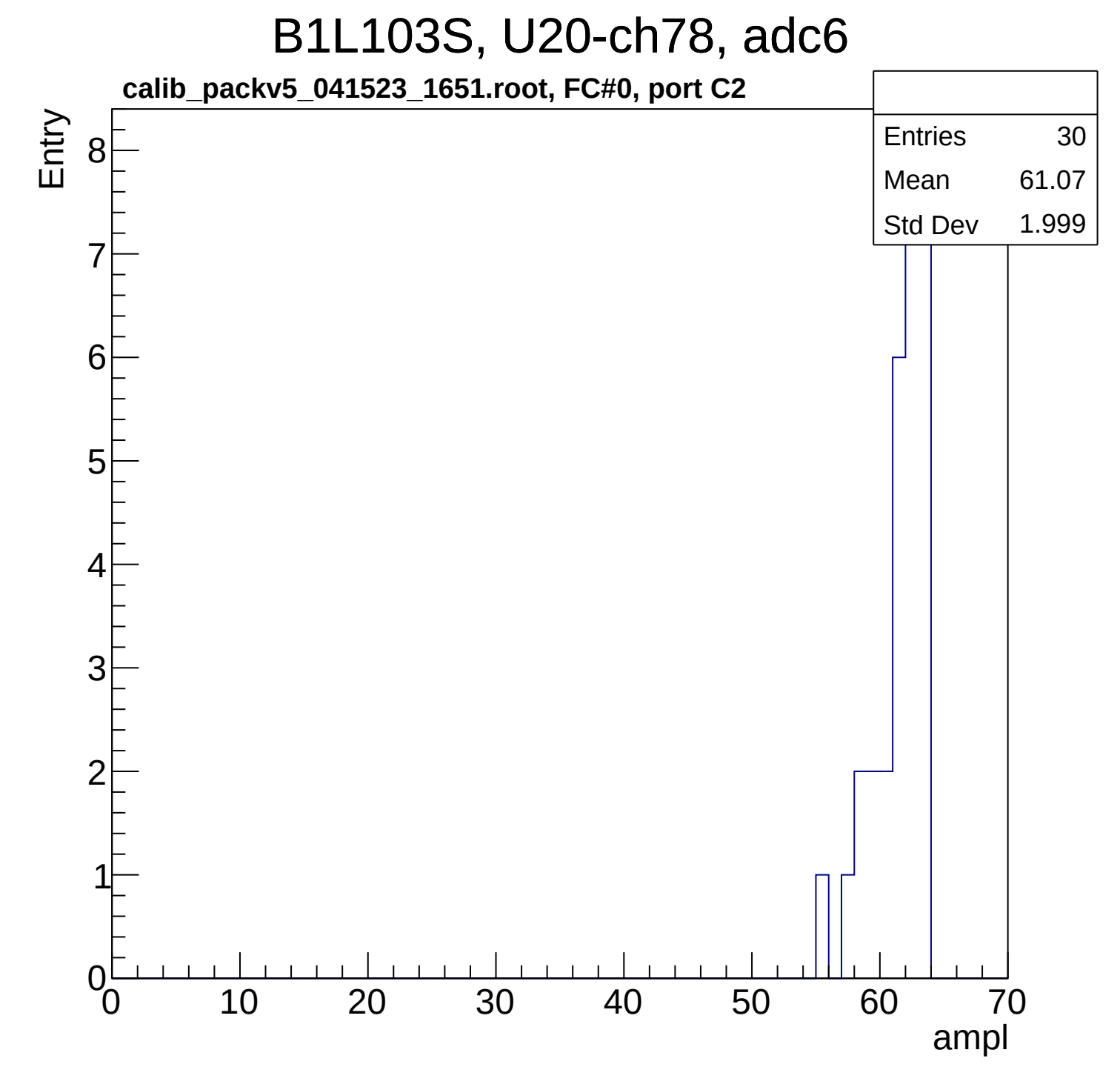
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch78, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 61.07
Std Dev 1.999
Entry
ampl
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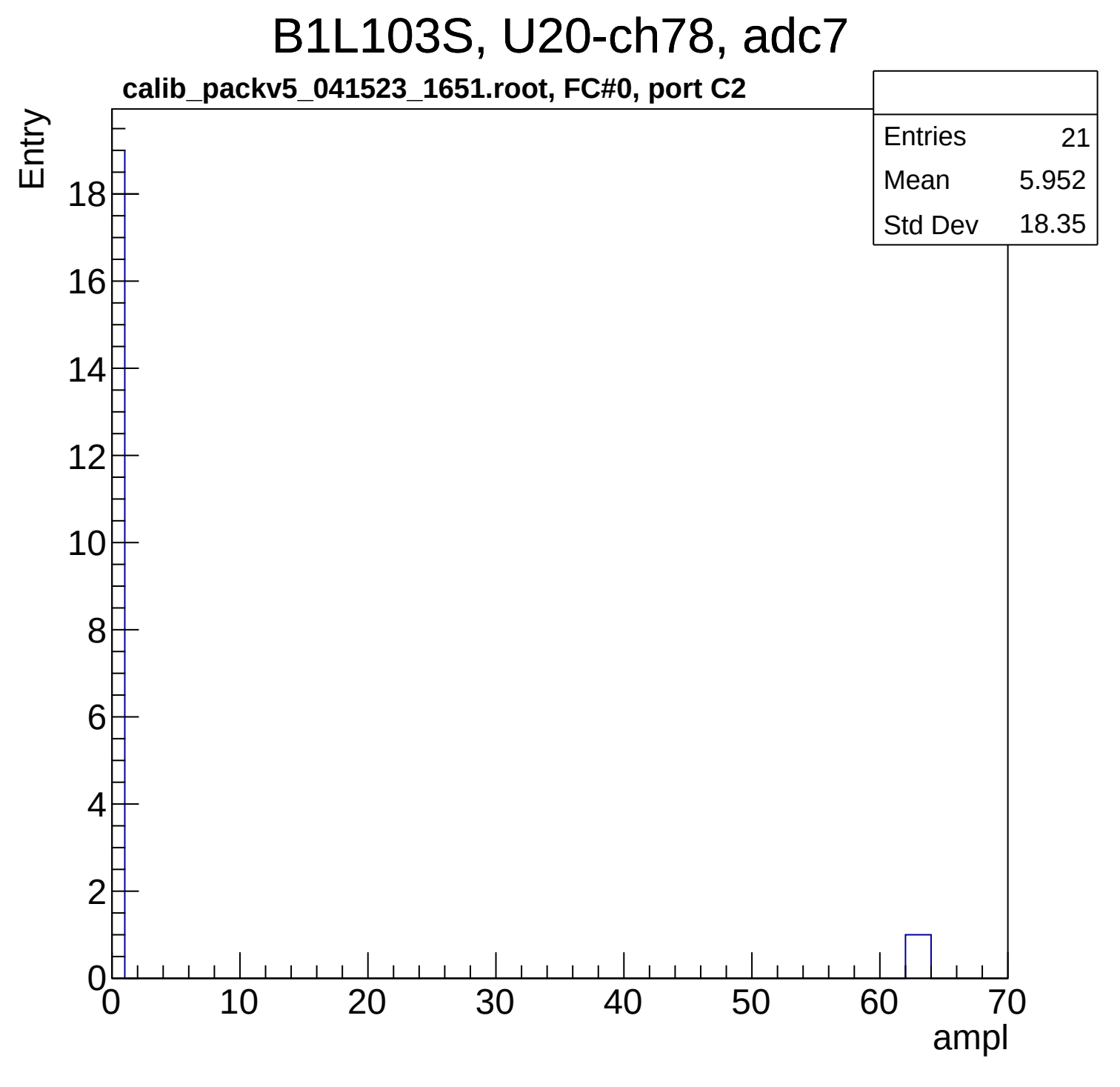
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch78, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.952
Std Dev 18.35
Entry
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6
8
10
12
14
16
18
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10
20
30
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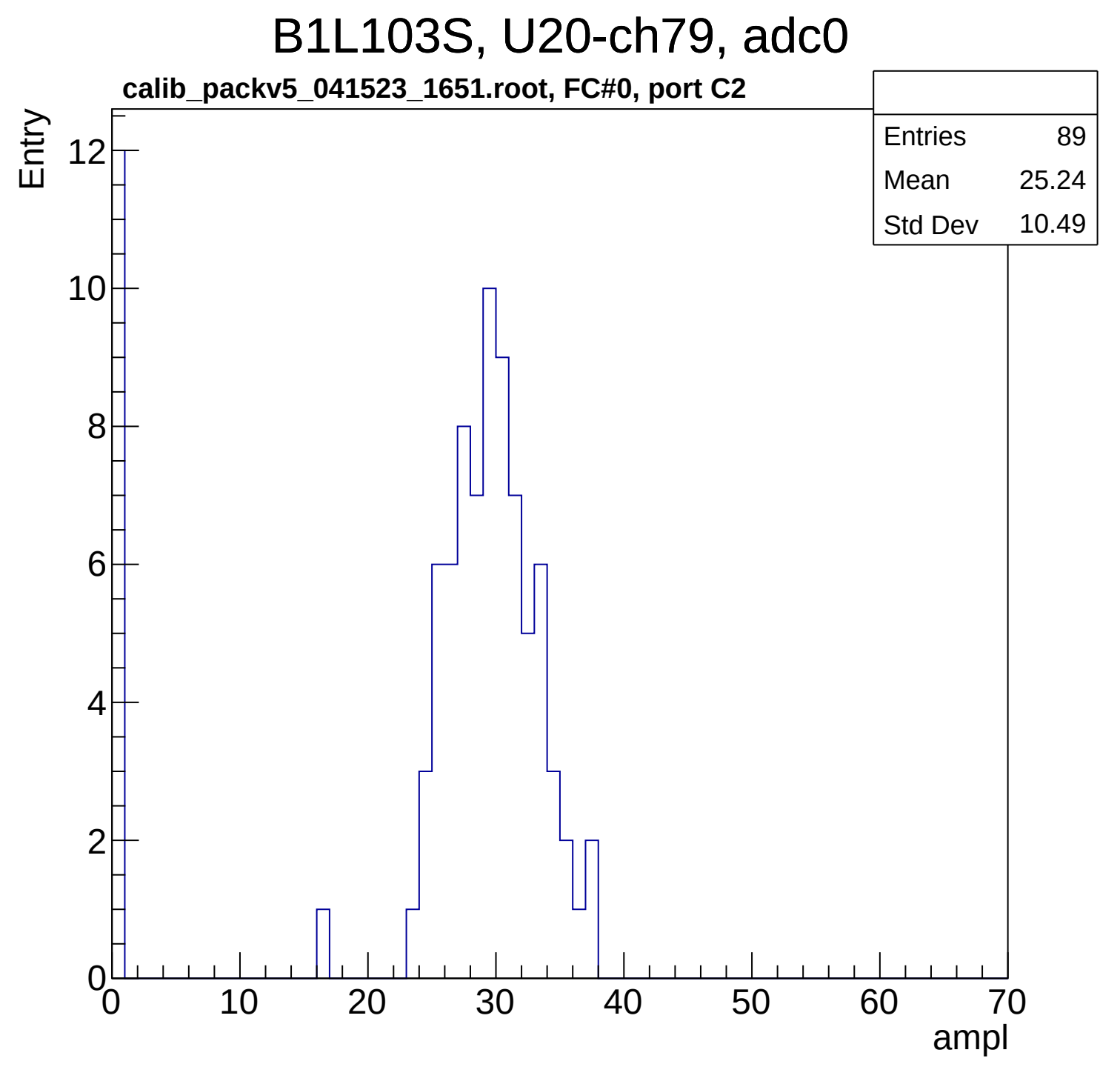
50
60
70
ampl


B1L103S, U20-ch79, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 25.24
Std Dev 10.49
Entry
ampl
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6
8
10
12
0
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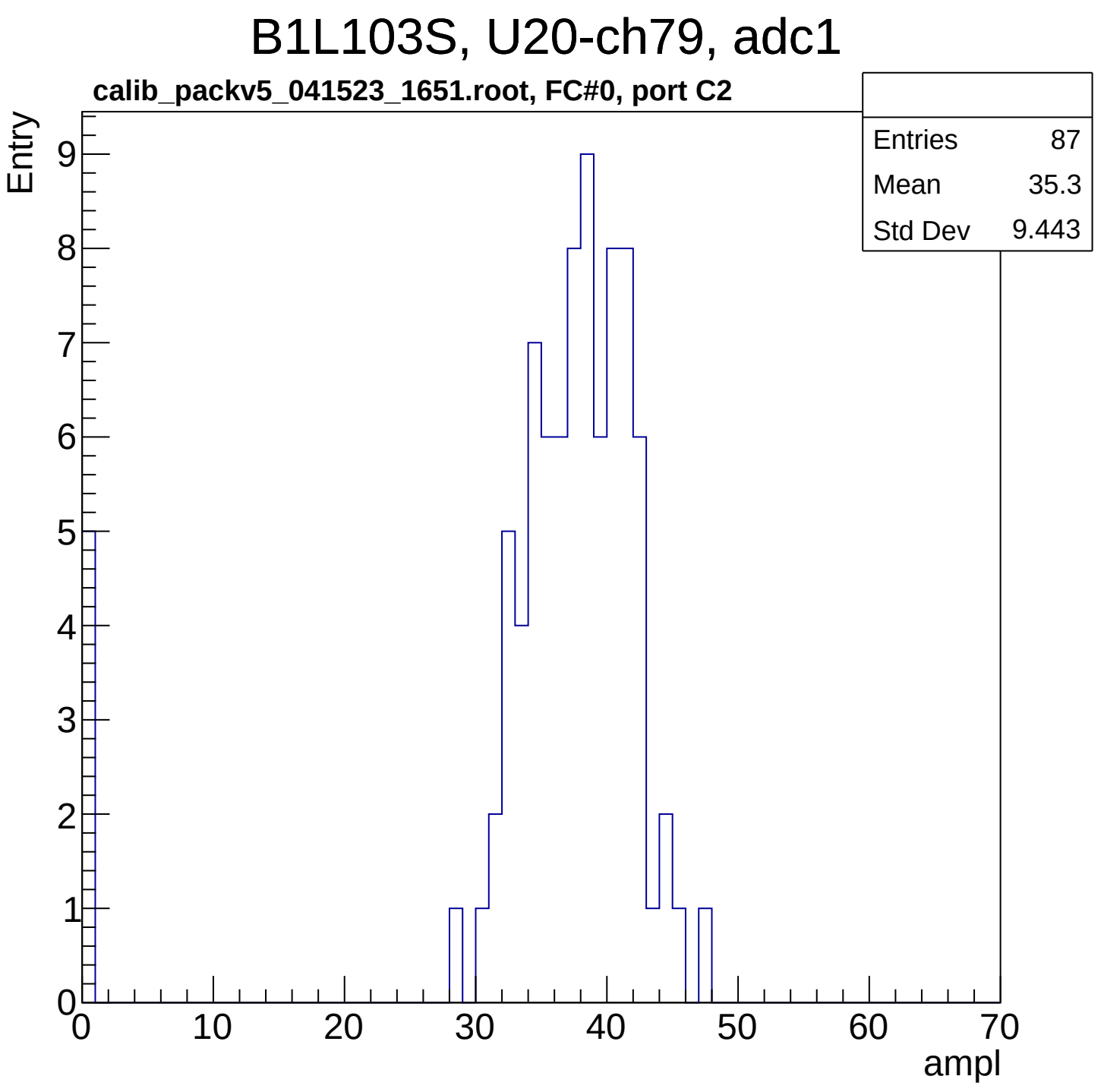
20
30
40
50
60
70


B1L103S, U20-ch79, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 35.3
Std Dev 9.443
Entry
ampl
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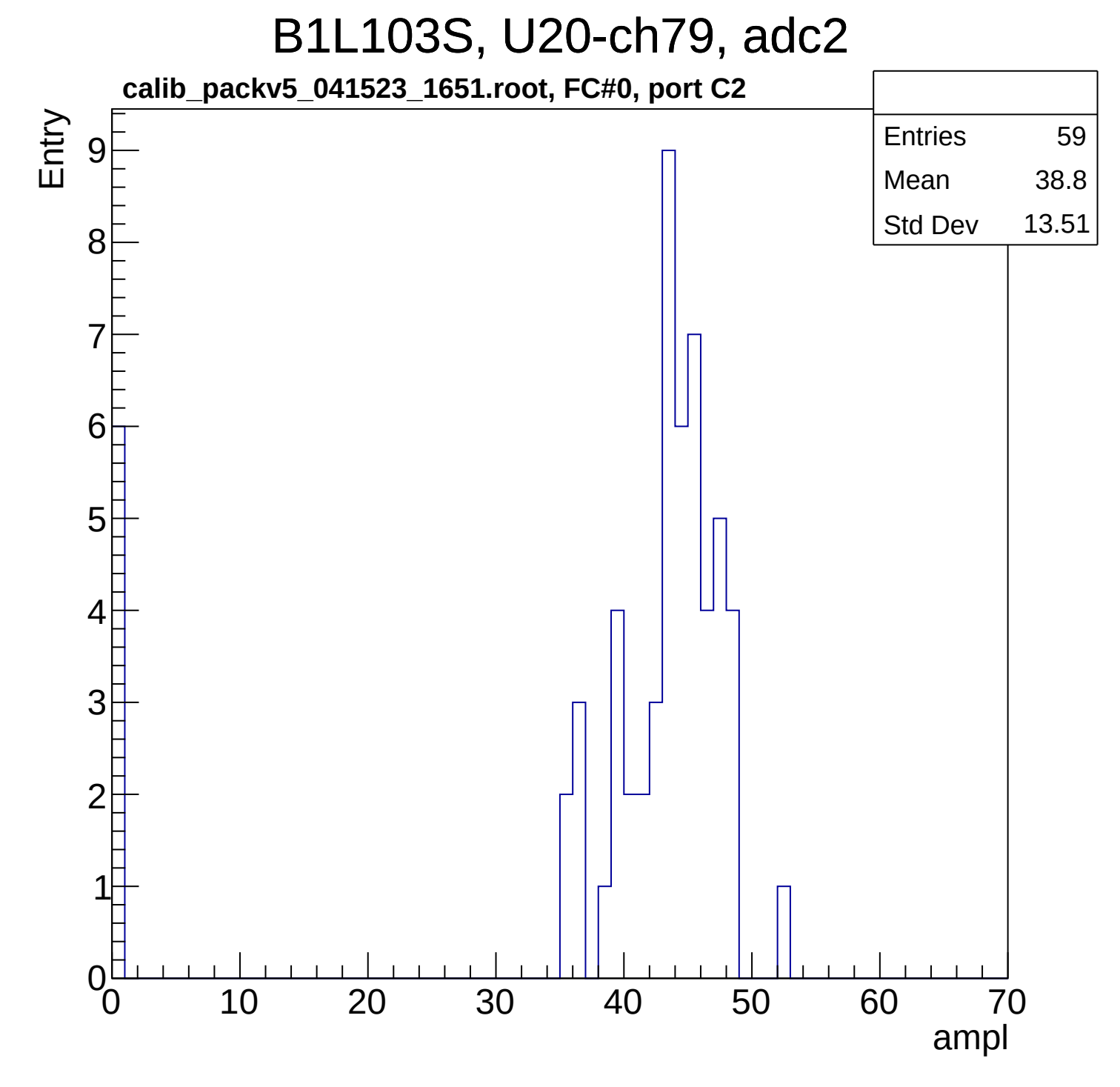
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch79, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 38.8
Std Dev 13.51
Entry
ampl
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3
4
5
6
7
8
9
0
10
20
30
40
50
60
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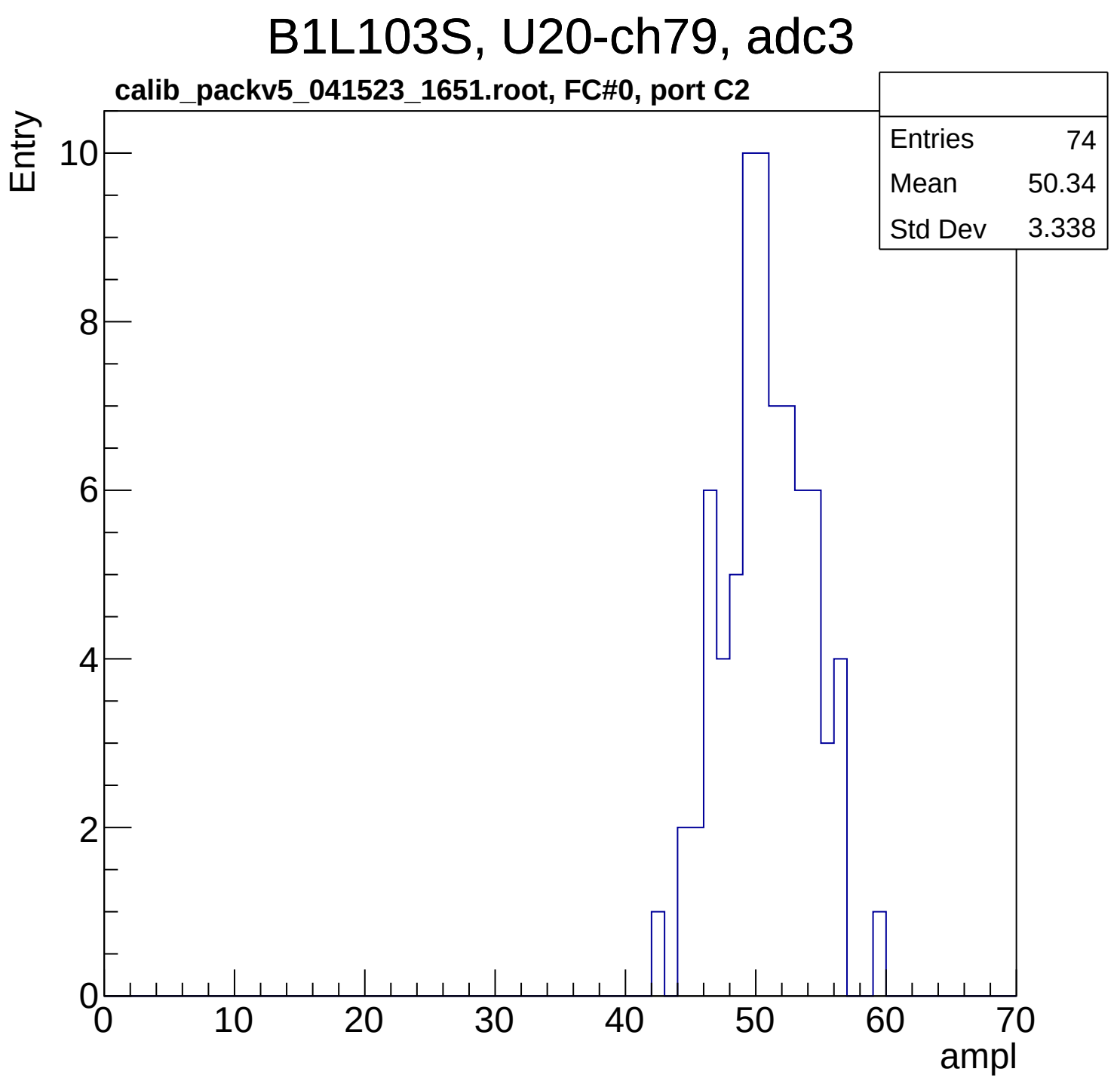
B1L103S, U20-ch79, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 50.34
Std Dev 3.338
Entry
ampl
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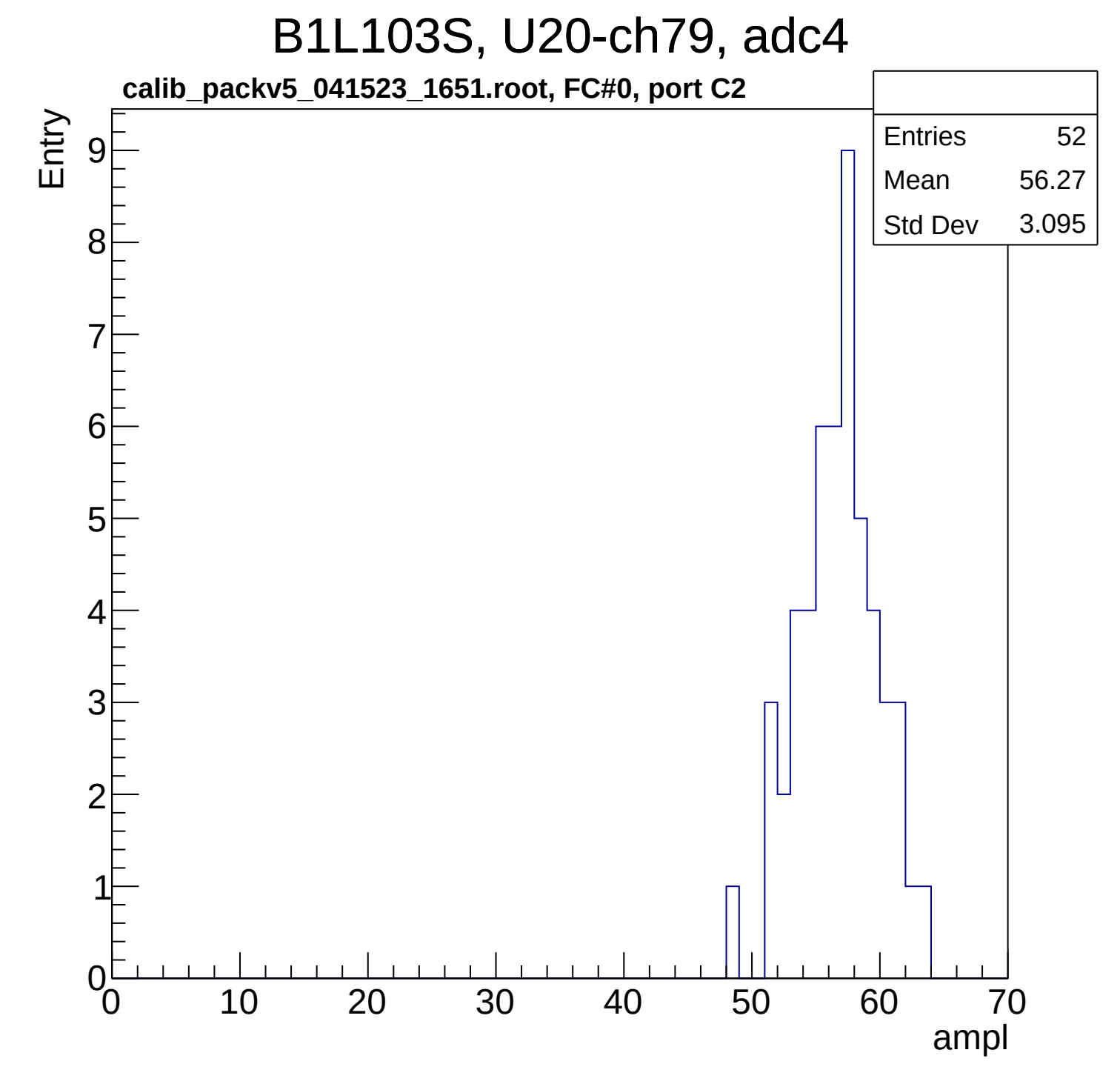
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U20-ch79, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 56.27
Std Dev 3.095
Entry
ampl
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6
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0
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60
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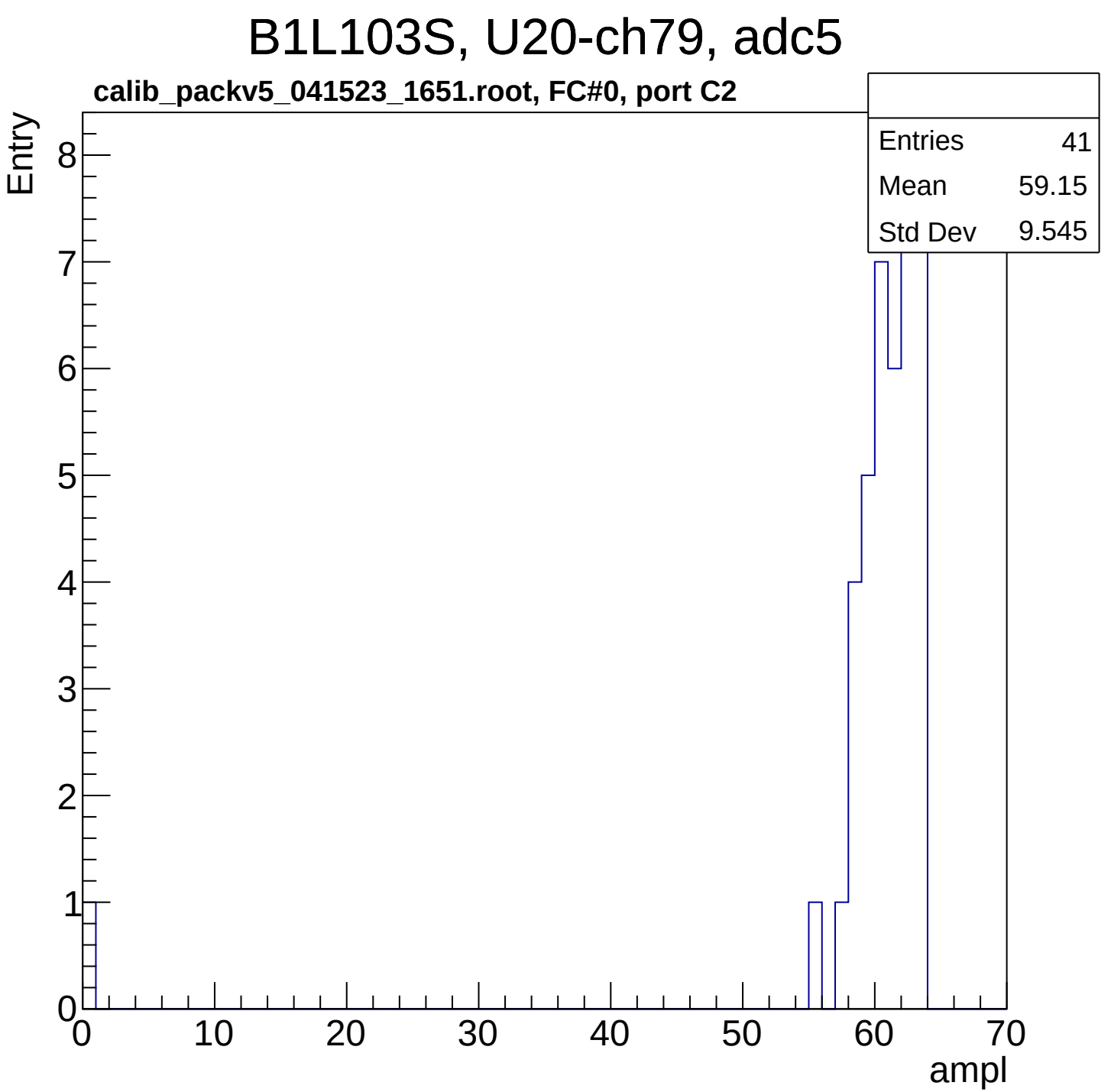
B1L103S, U20-ch79, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 59.15
Std Dev 9.545
Entry
ampl
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7
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60
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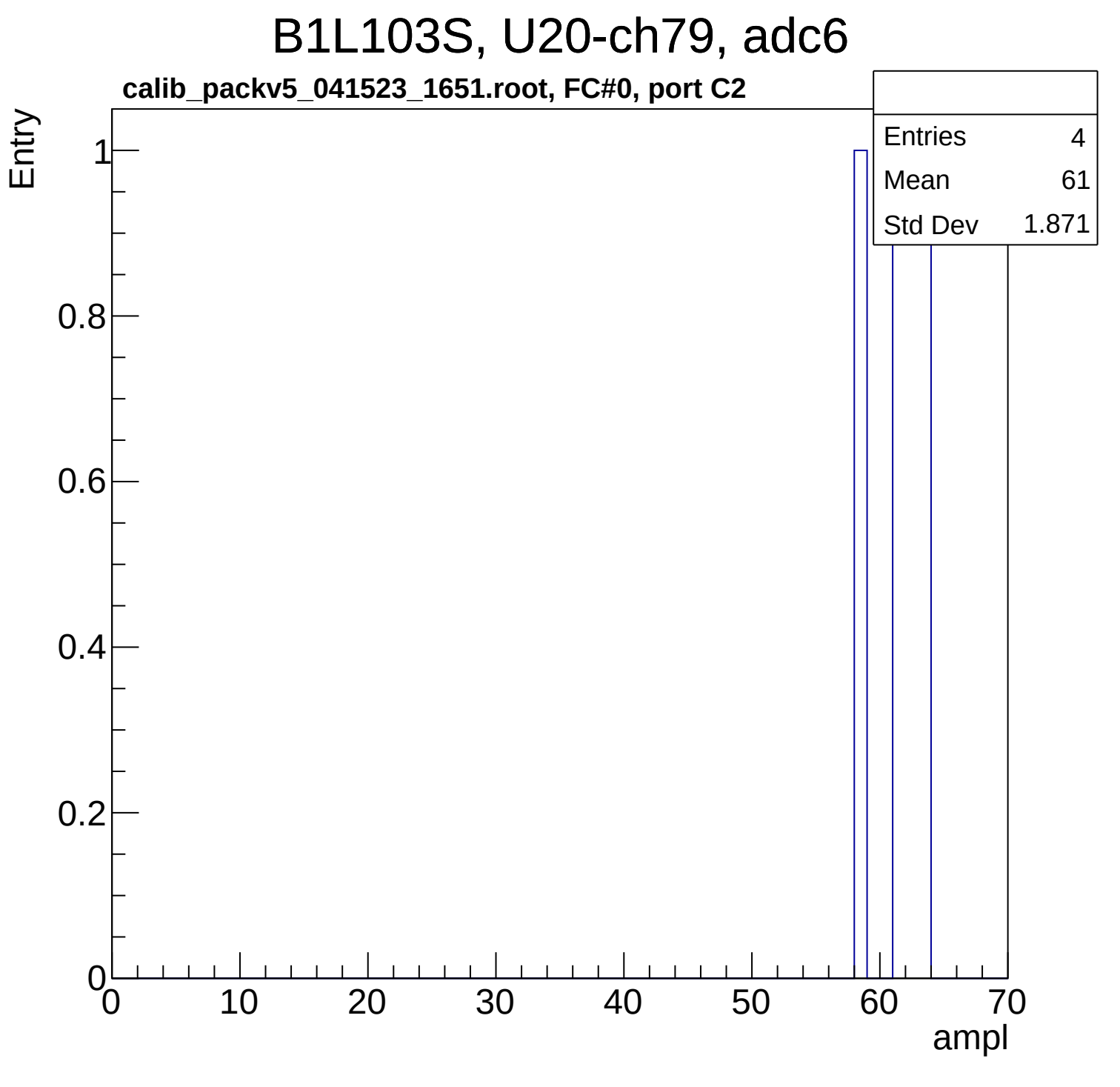
B1L103S, U20-ch79, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 61
Std Dev 1.871
Entry
ampl
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0.2
0.4
0.6
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0
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60
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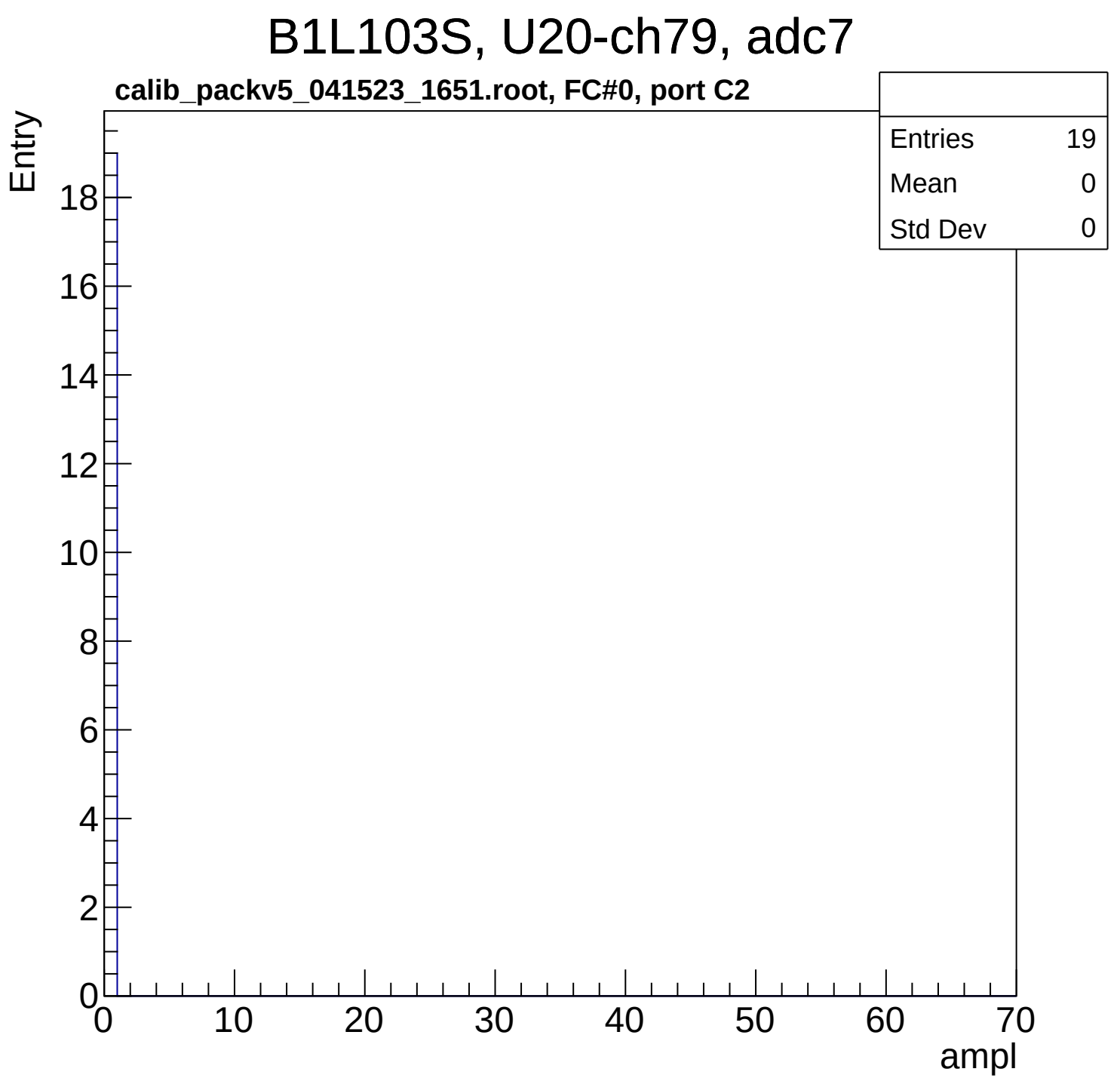
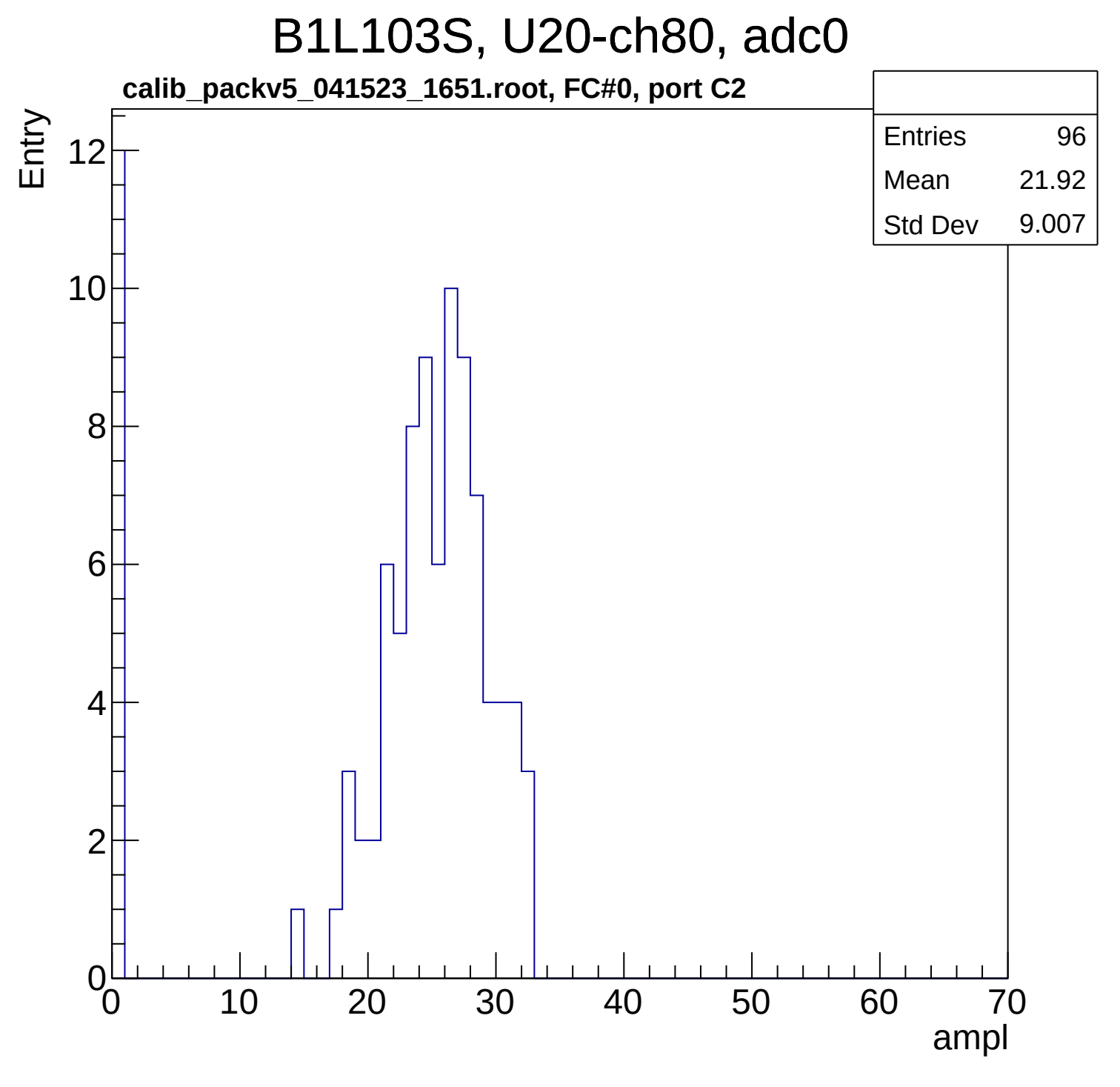

B1L103S, U20-ch79, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch80, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 96
Mean 21.92
Std Dev 9.007
Entry
ampl
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6
8
10
12
0
10
20
30
40
50
60
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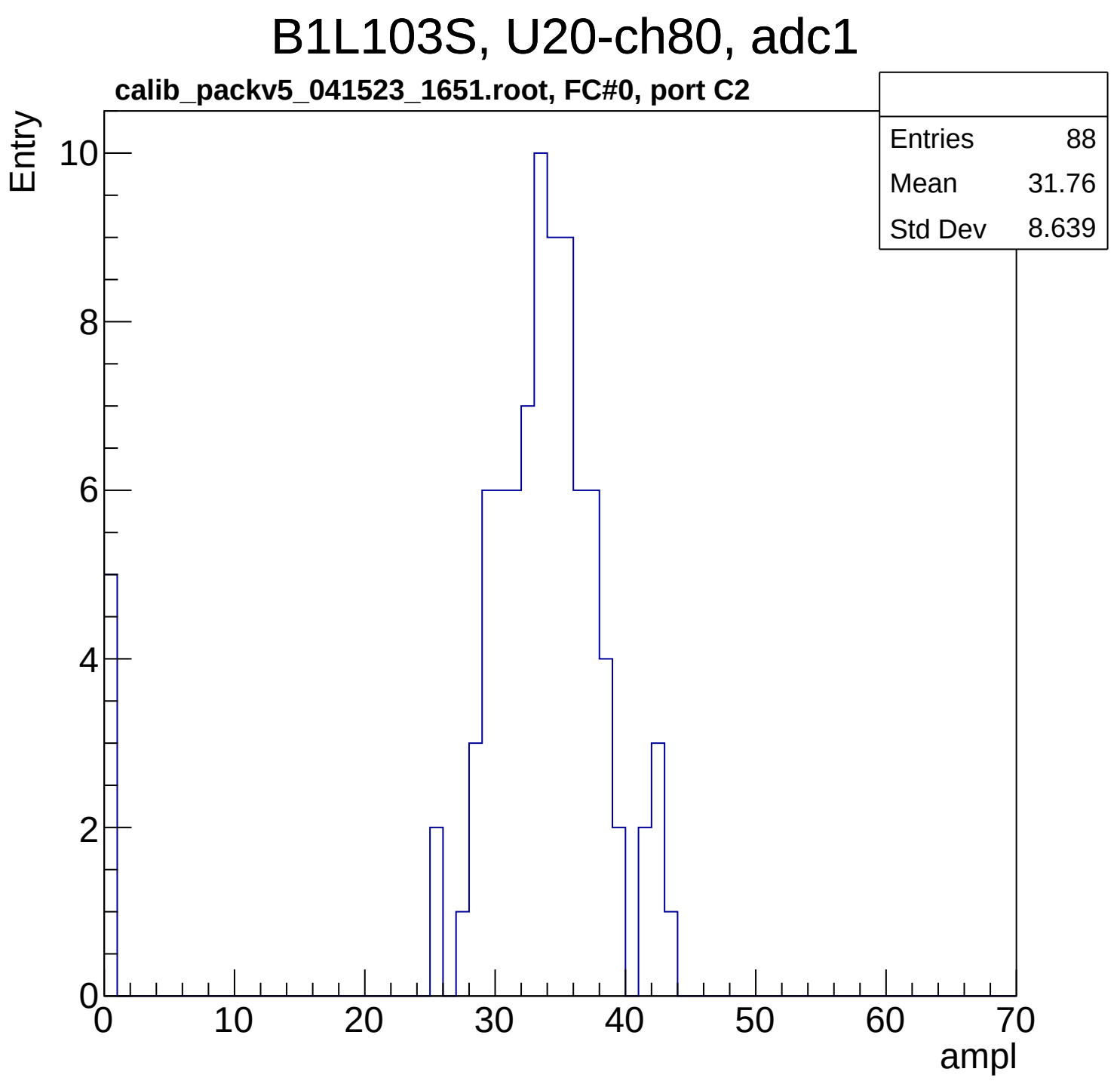
B1L103S, U20-ch80, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 31.76
Std Dev 8.639
Entry
ampl
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4
6
8
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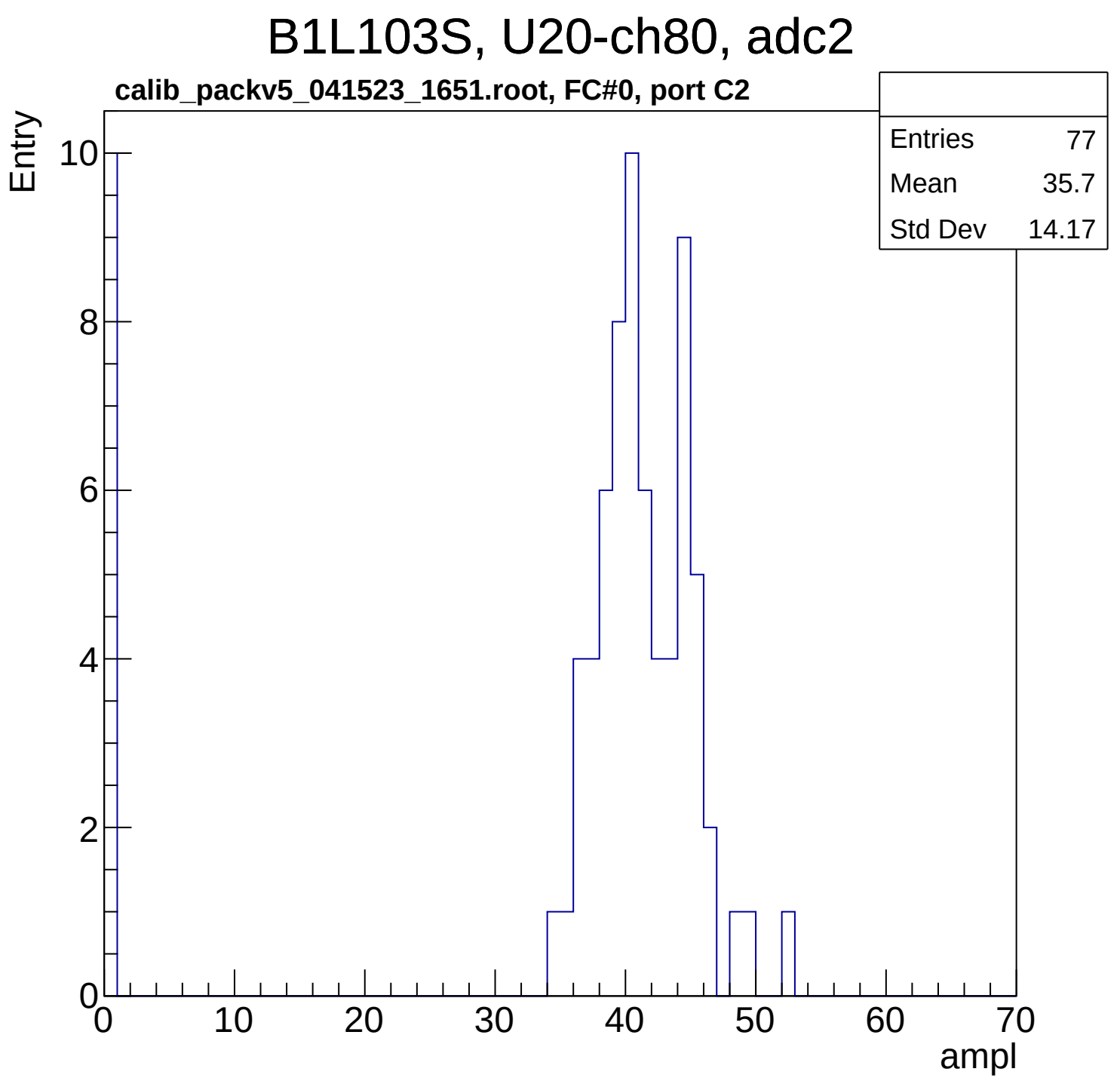
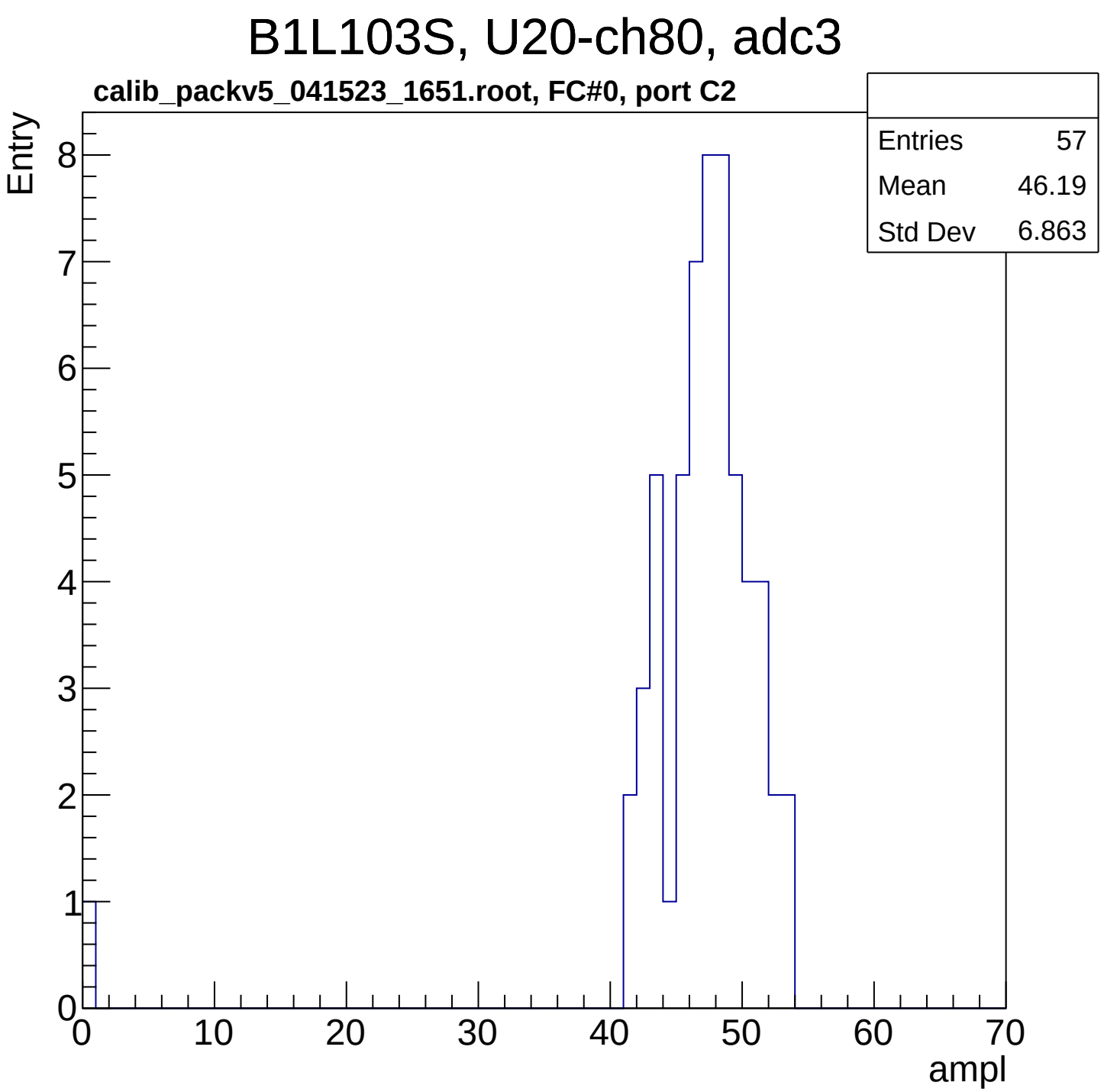
0
10
20
30
40
50
60
70


B1L103S, U20-ch80, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 35.7
Std Dev 14.17
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch80, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 46.19
Std Dev 6.863
Entry
ampl
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2
3
4
5
6
7
8
0
10
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40
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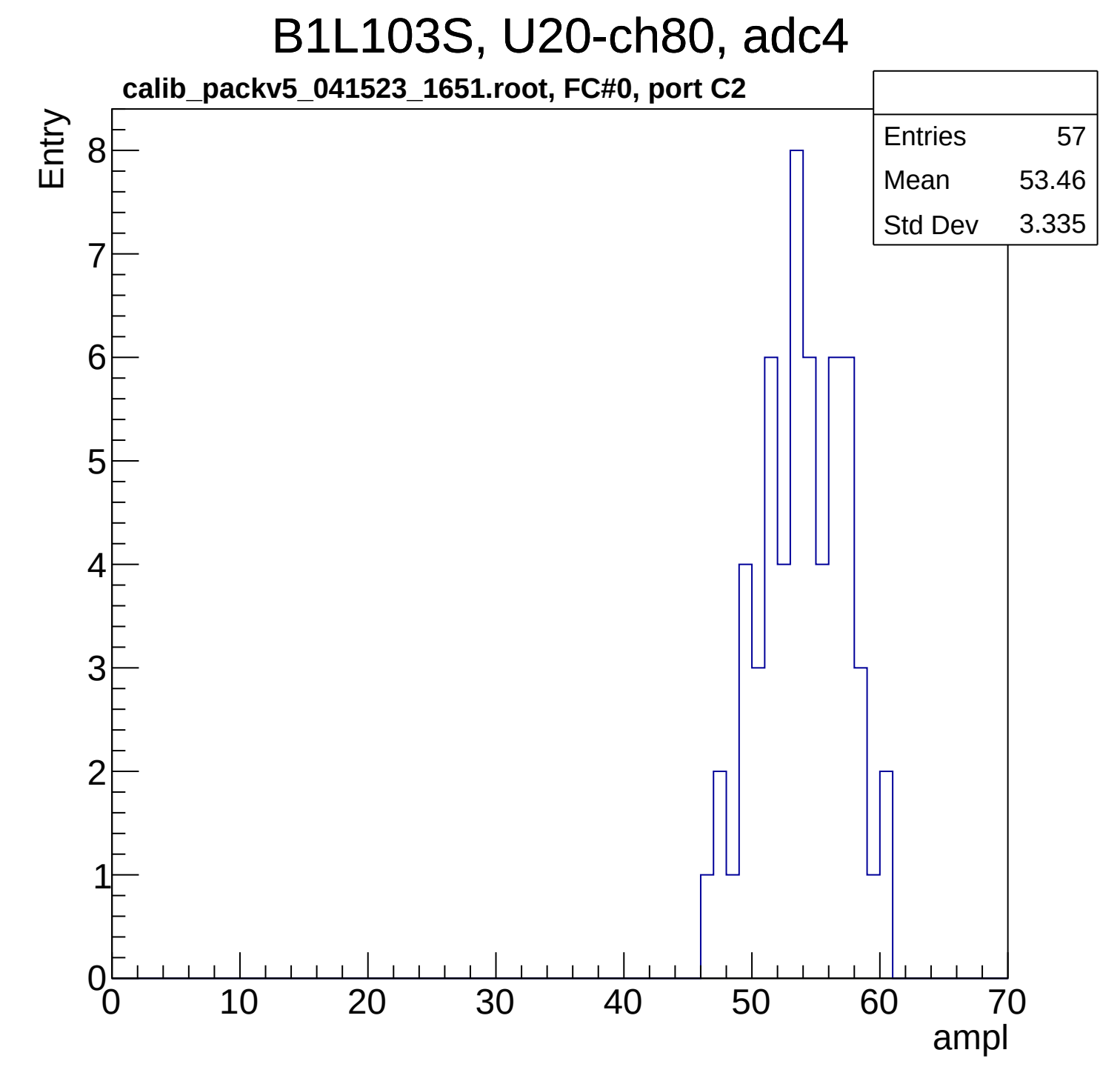
60
70


B1L103S, U20-ch80, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 53.46
Std Dev 3.335
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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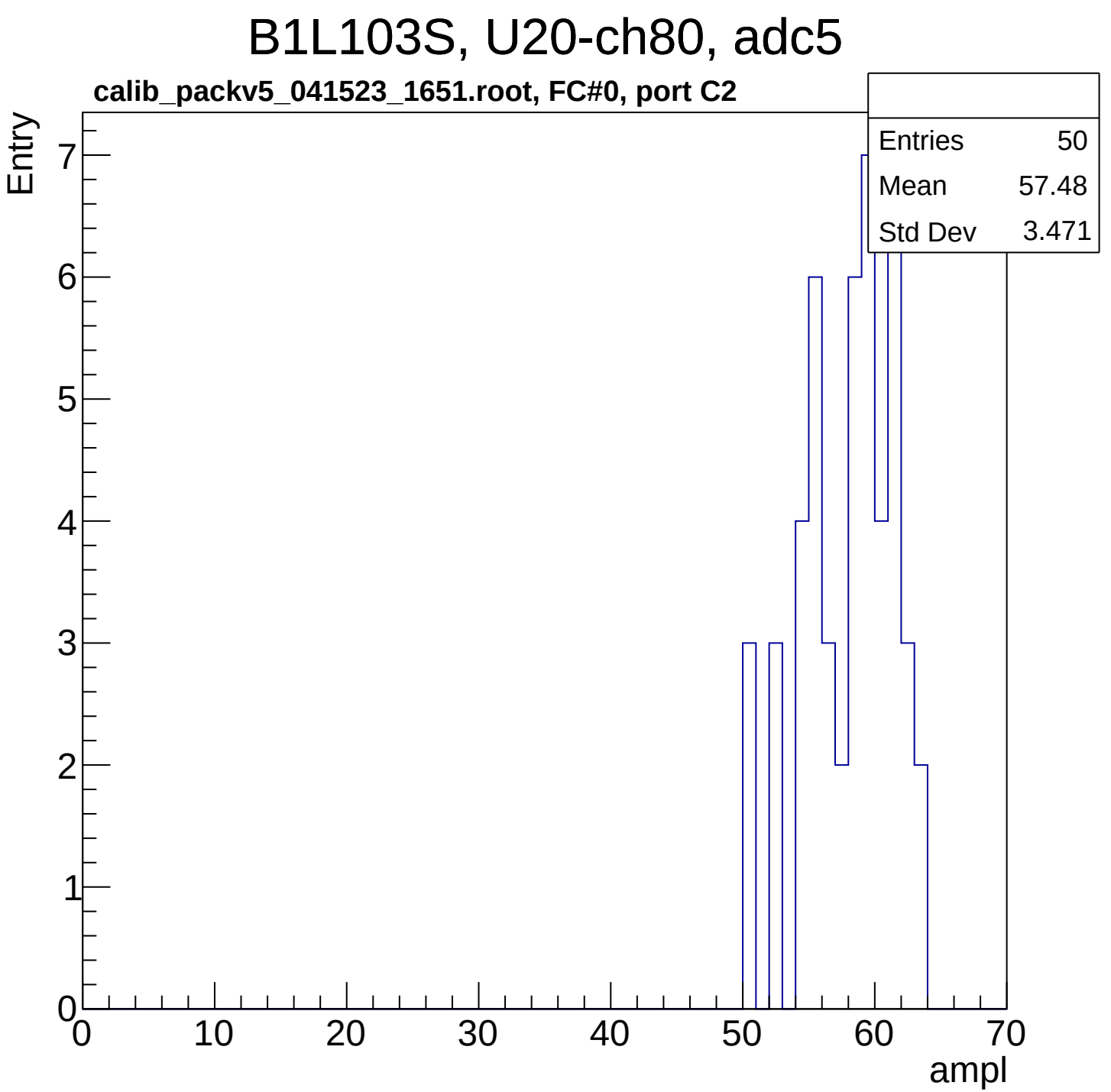
B1L103S, U20-ch80, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 57.48
Std Dev 3.471
Entry
ampl
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2
3
4
5
6
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0
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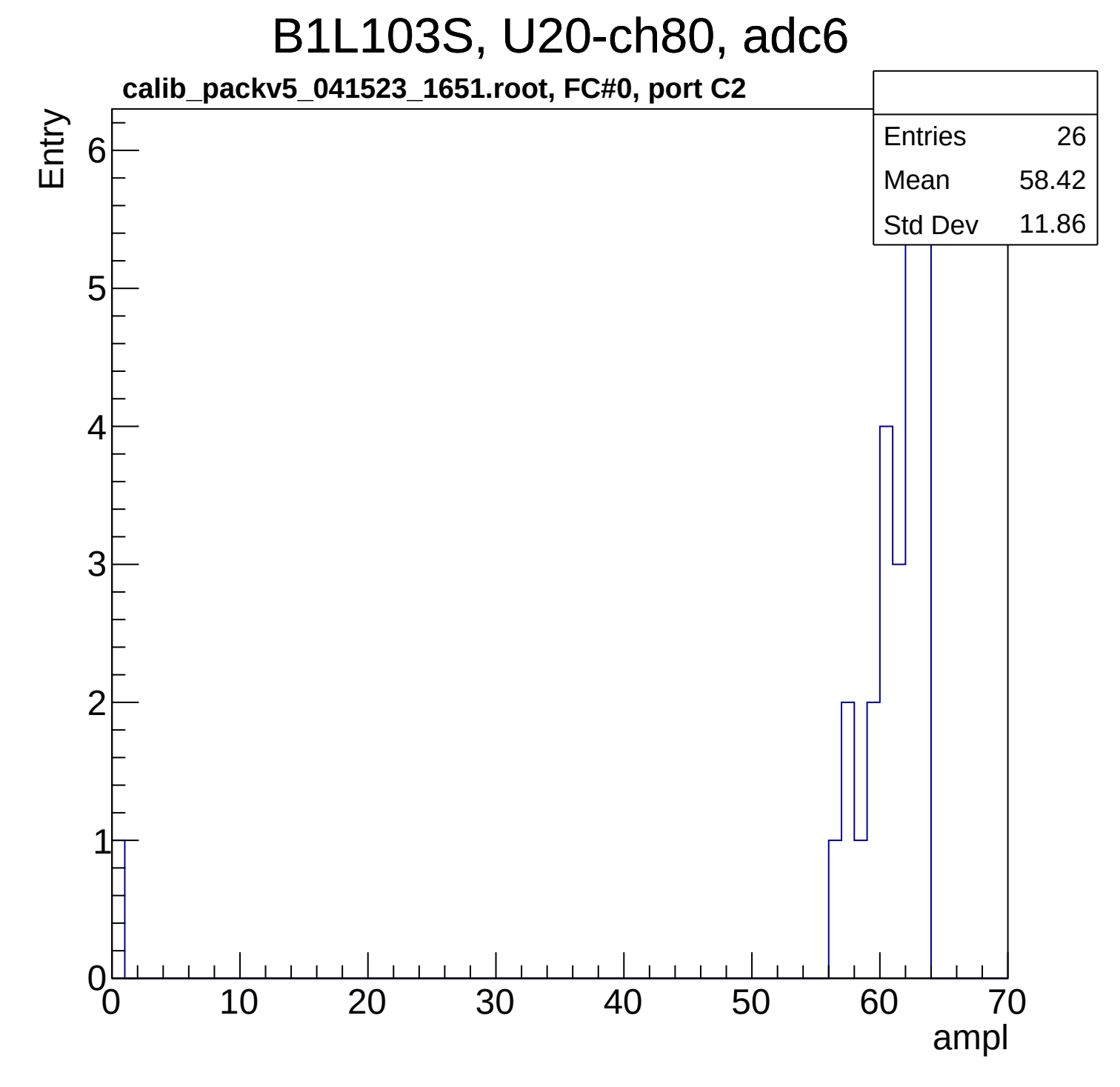
20
30
40
50
60
70


B1L103S, U20-ch80, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 58.42
Std Dev 11.86
Entry
ampl
0
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2
3
4
5
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0
10
20
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40
50
60
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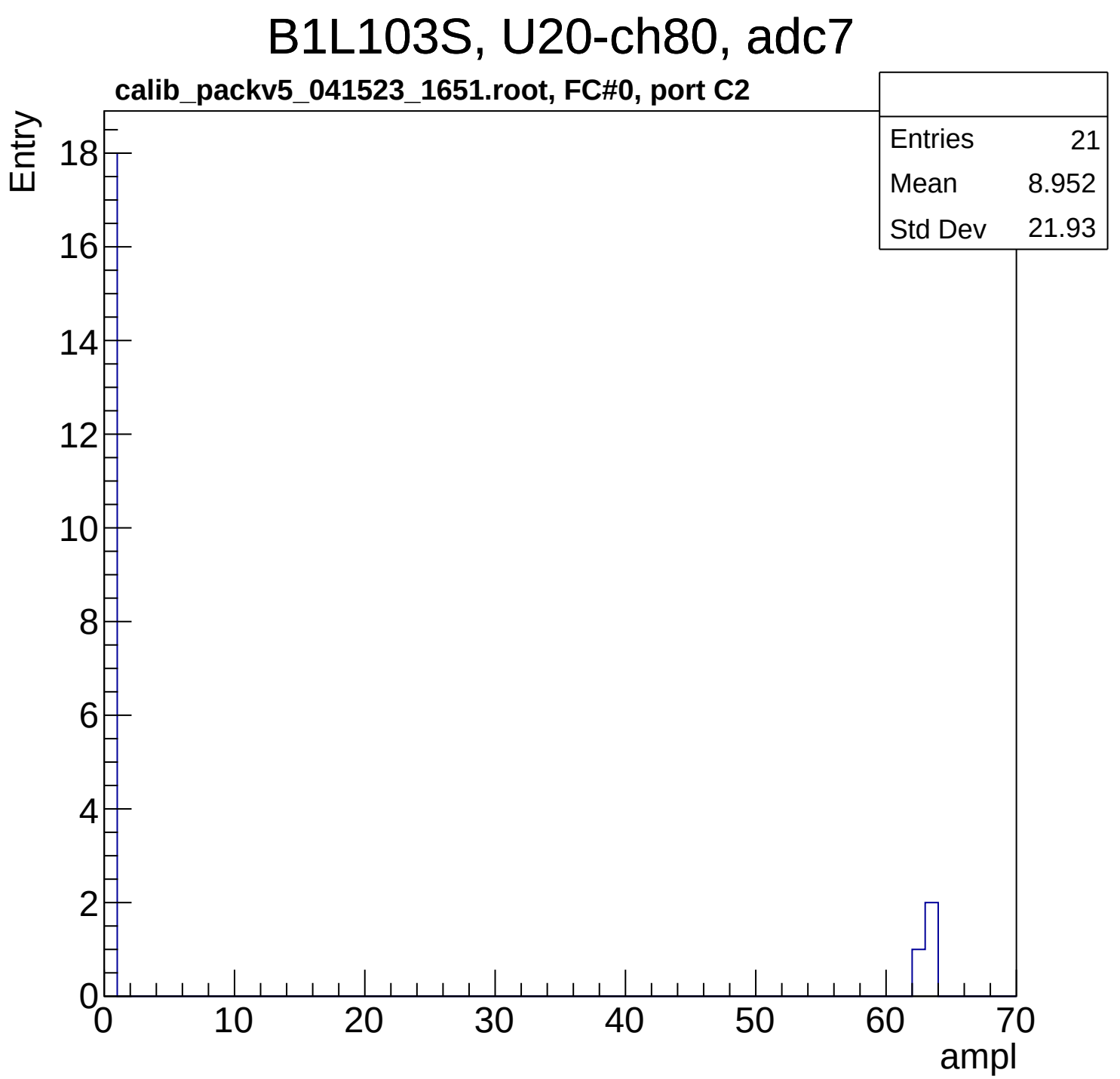
B1L103S, U20-ch80, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 8.952
Std Dev 21.93
Entry
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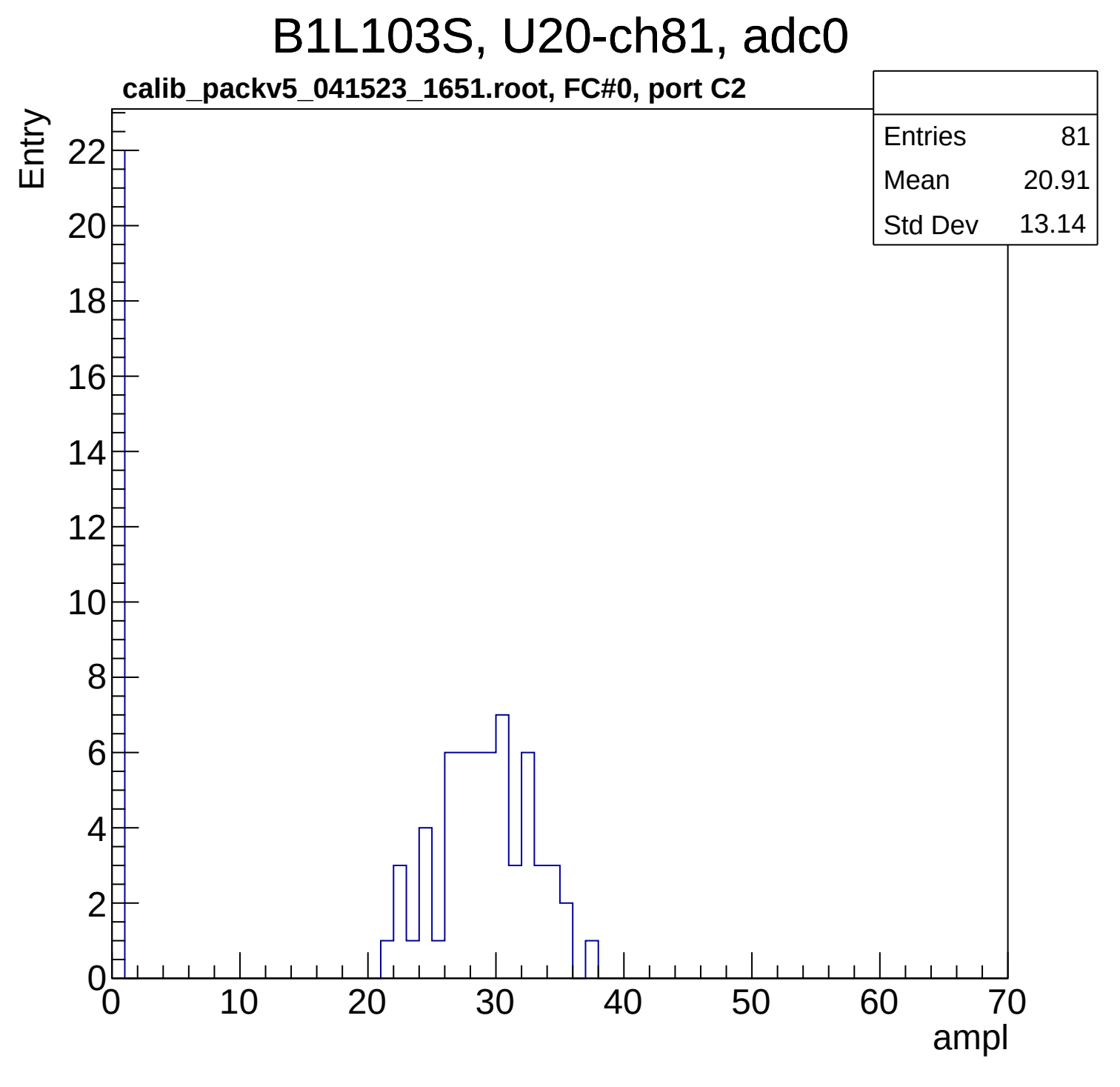
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch81, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 20.91
Std Dev 13.14
Entry
ampl
0
2
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6
8
10
12
14
16
18
20
22
0
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20
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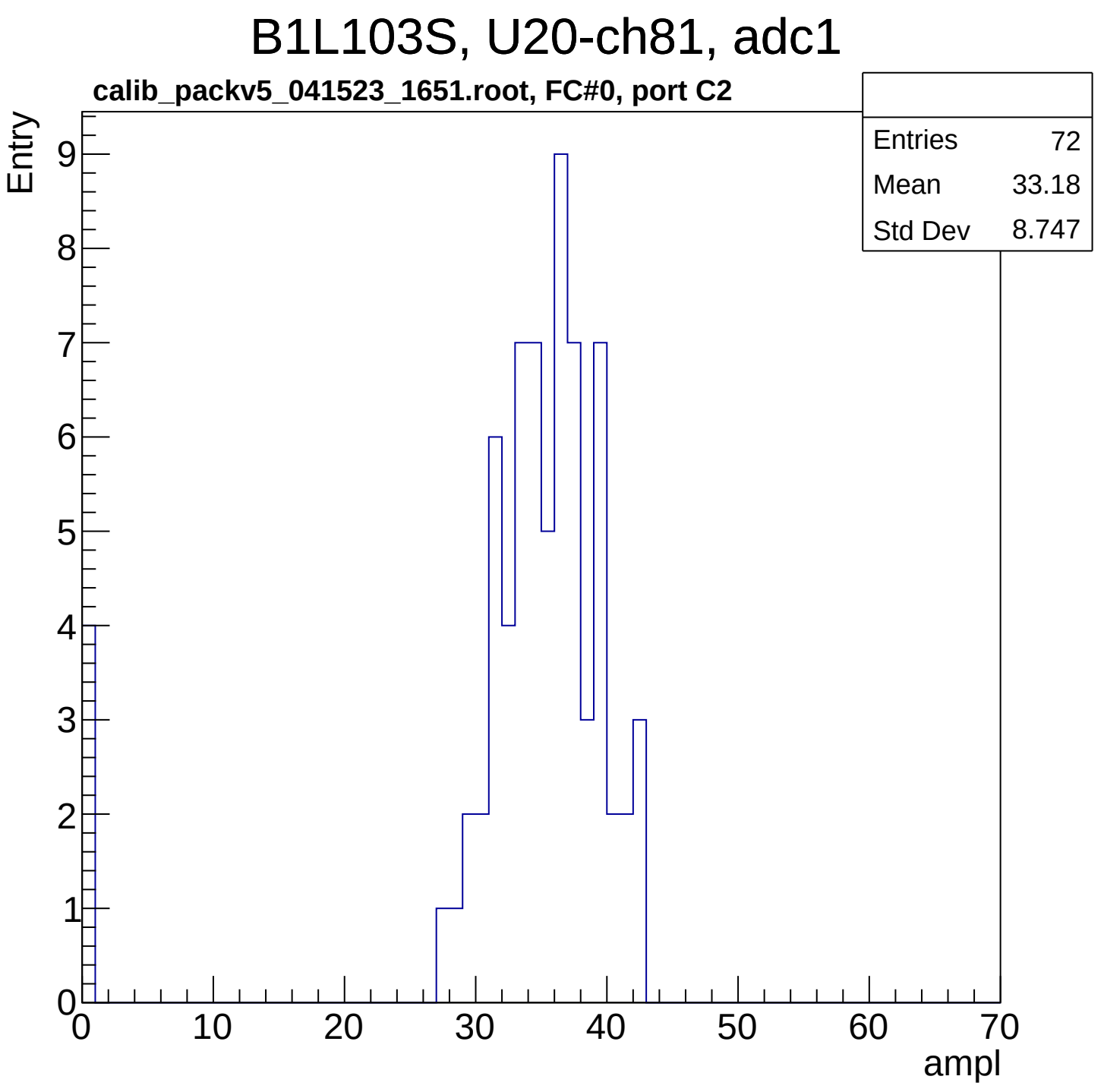
40
50
60
70


B1L103S, U20-ch81, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 33.18
Std Dev 8.747
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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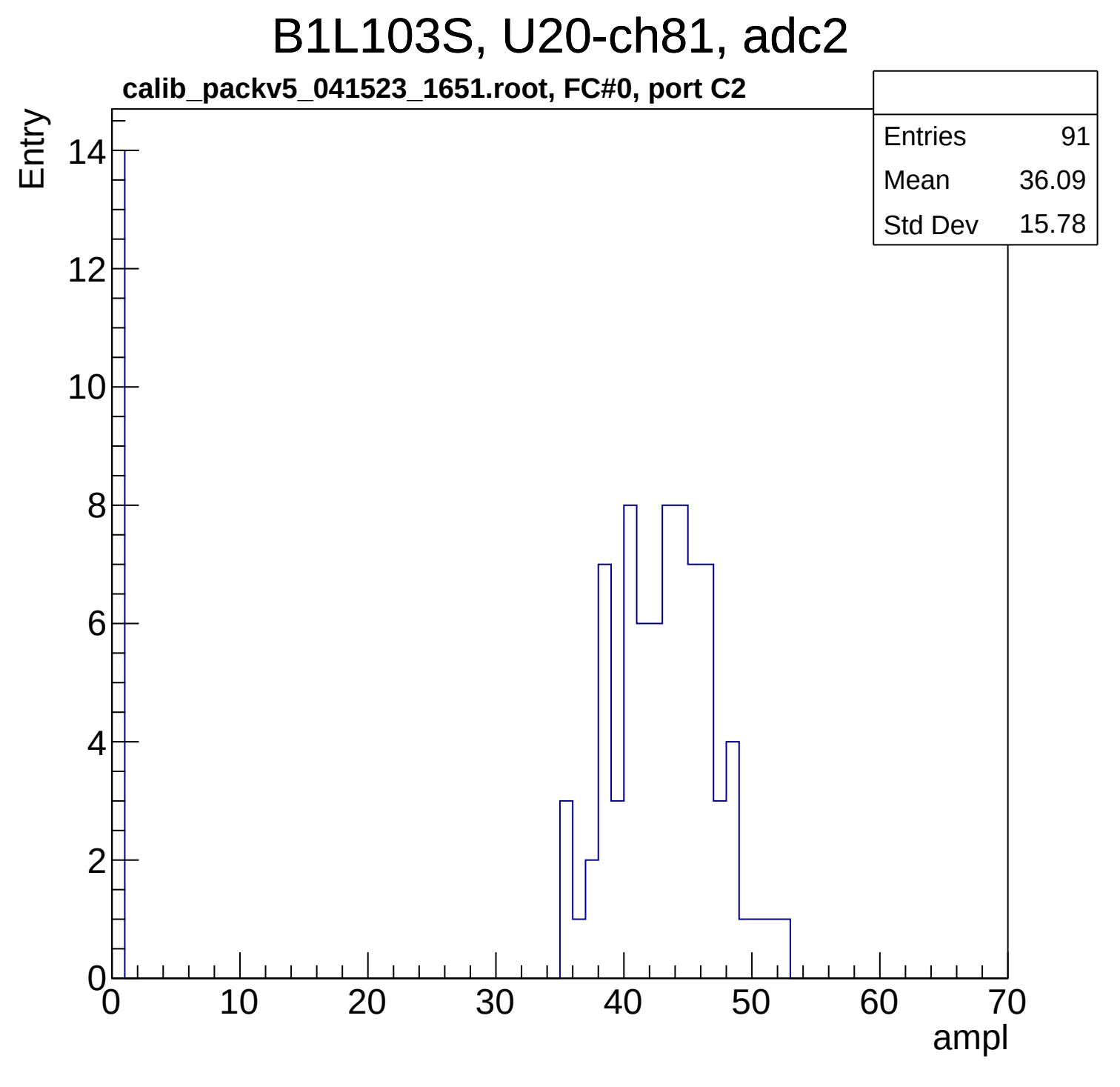
B1L103S, U20-ch81, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 36.09
Std Dev 15.78
Entry
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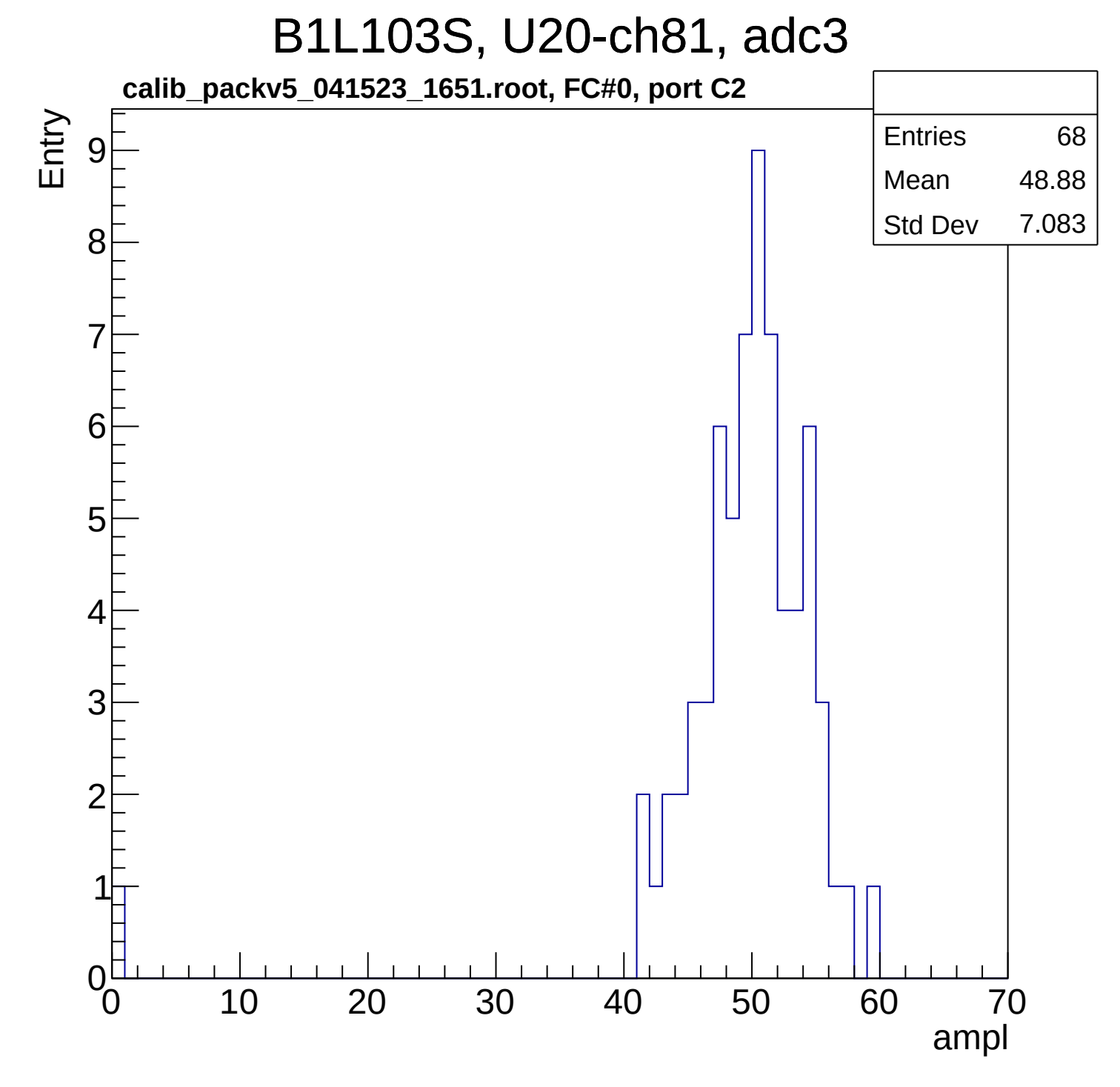
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch81, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 48.88
Std Dev 7.083
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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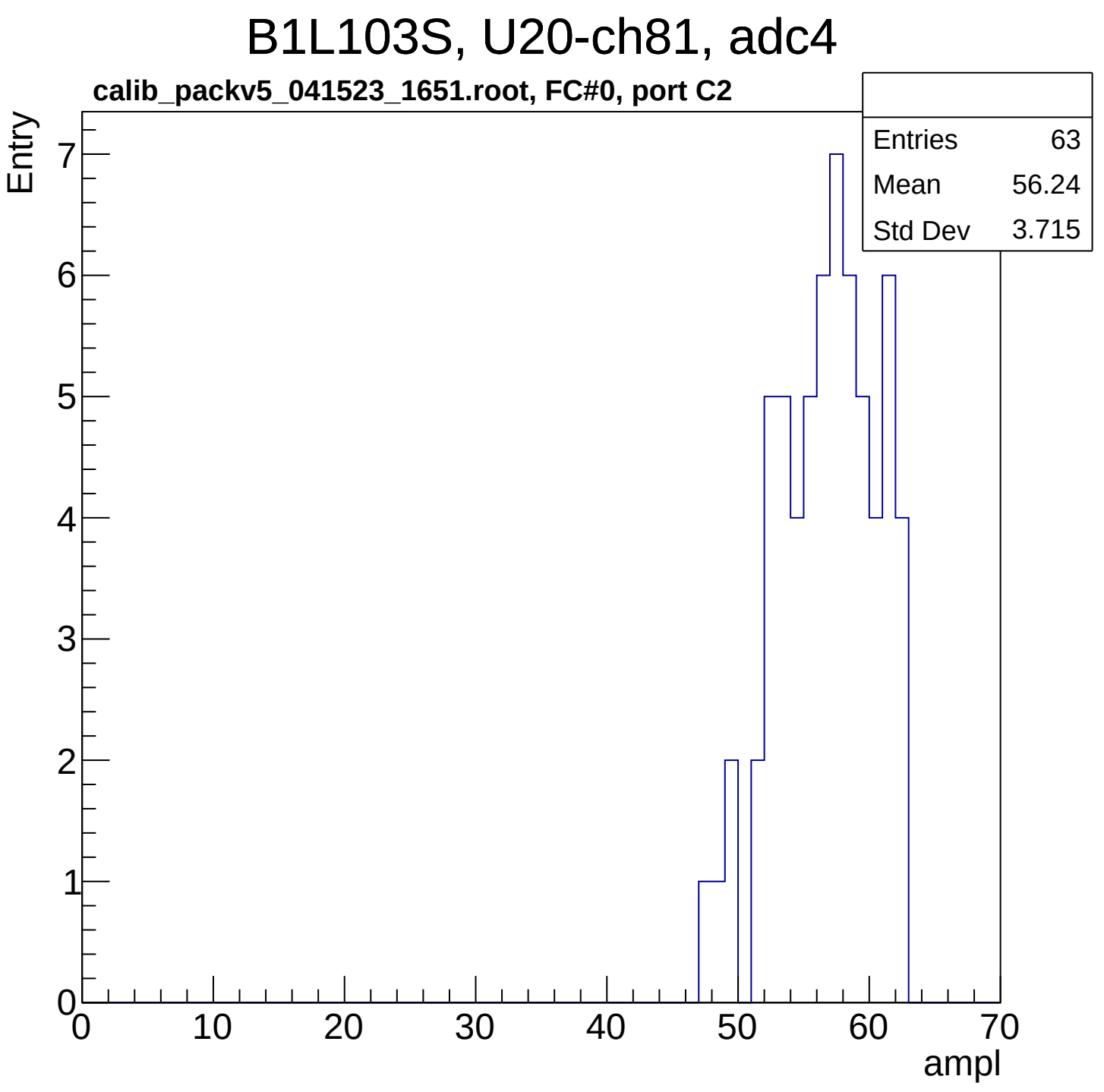
B1L103S, U20-ch81, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 56.24
Std Dev 3.715
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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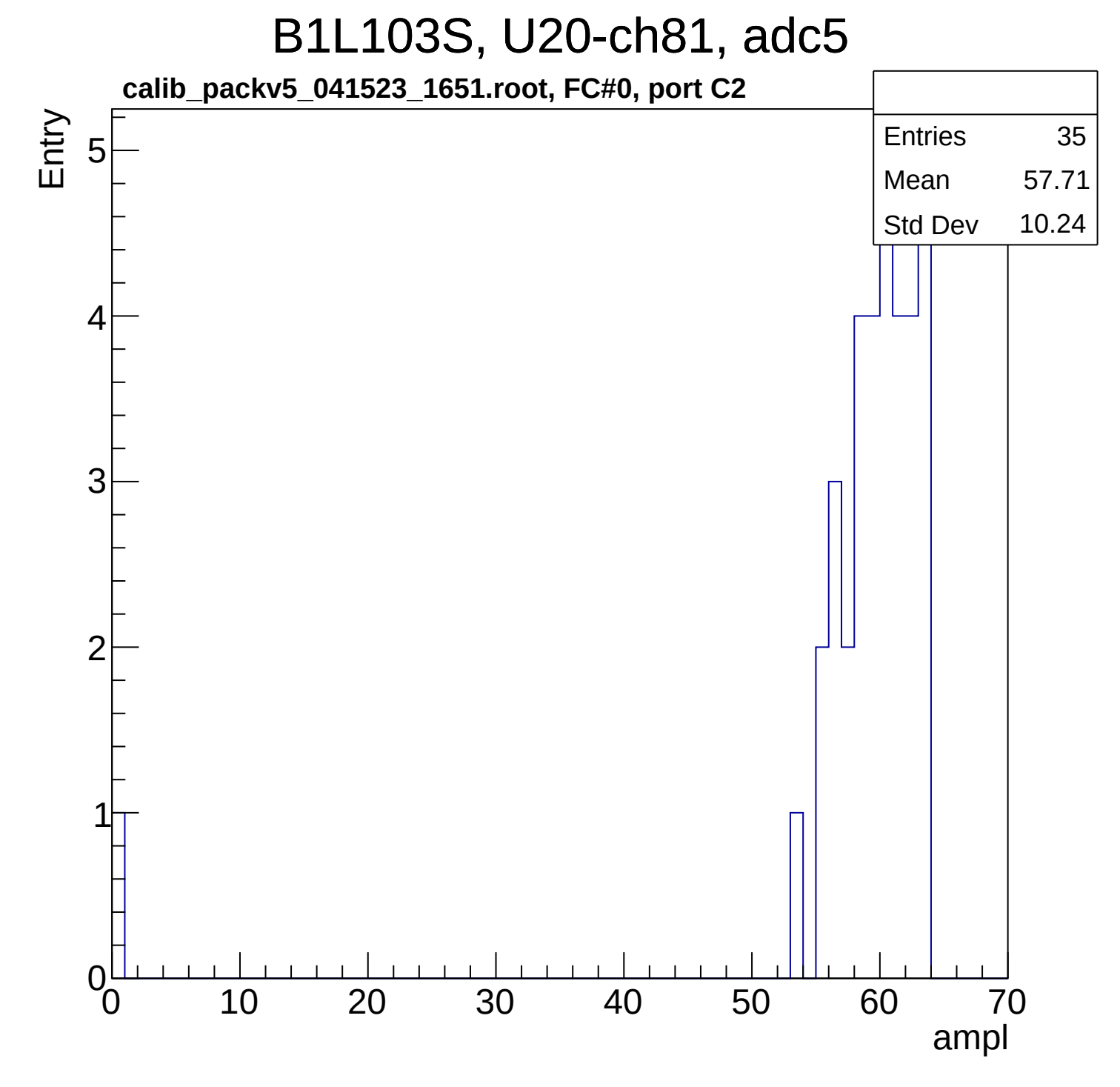
B1L103S, U20-ch81, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 57.71
Std Dev 10.24
Entry
ampl
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2
3
4
5
0
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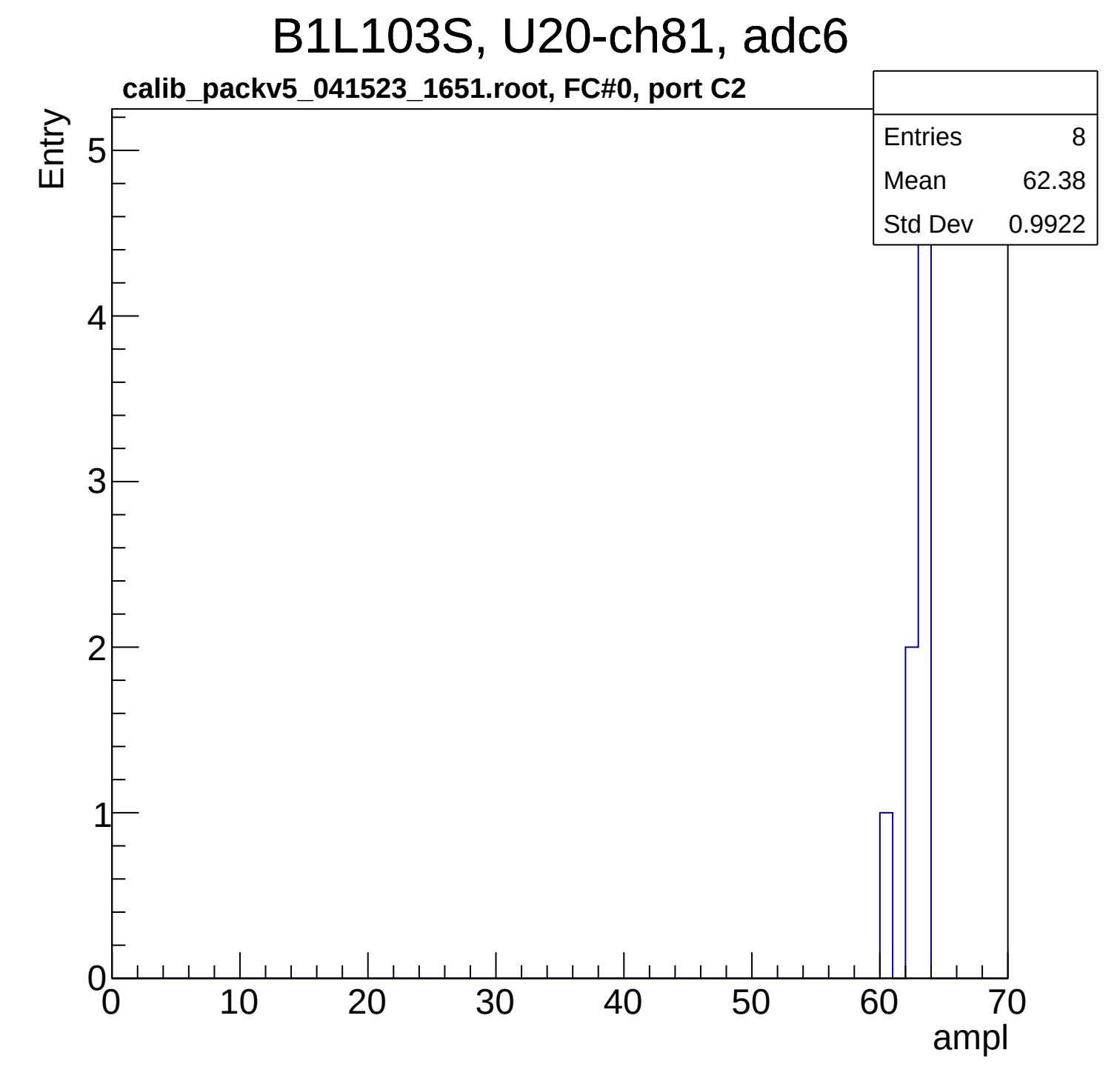
20
30
40
50
60
70


B1L103S, U20-ch81, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 62.38
Std Dev 0.9922
Entry
ampl
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2
3
4
5
0
10
20
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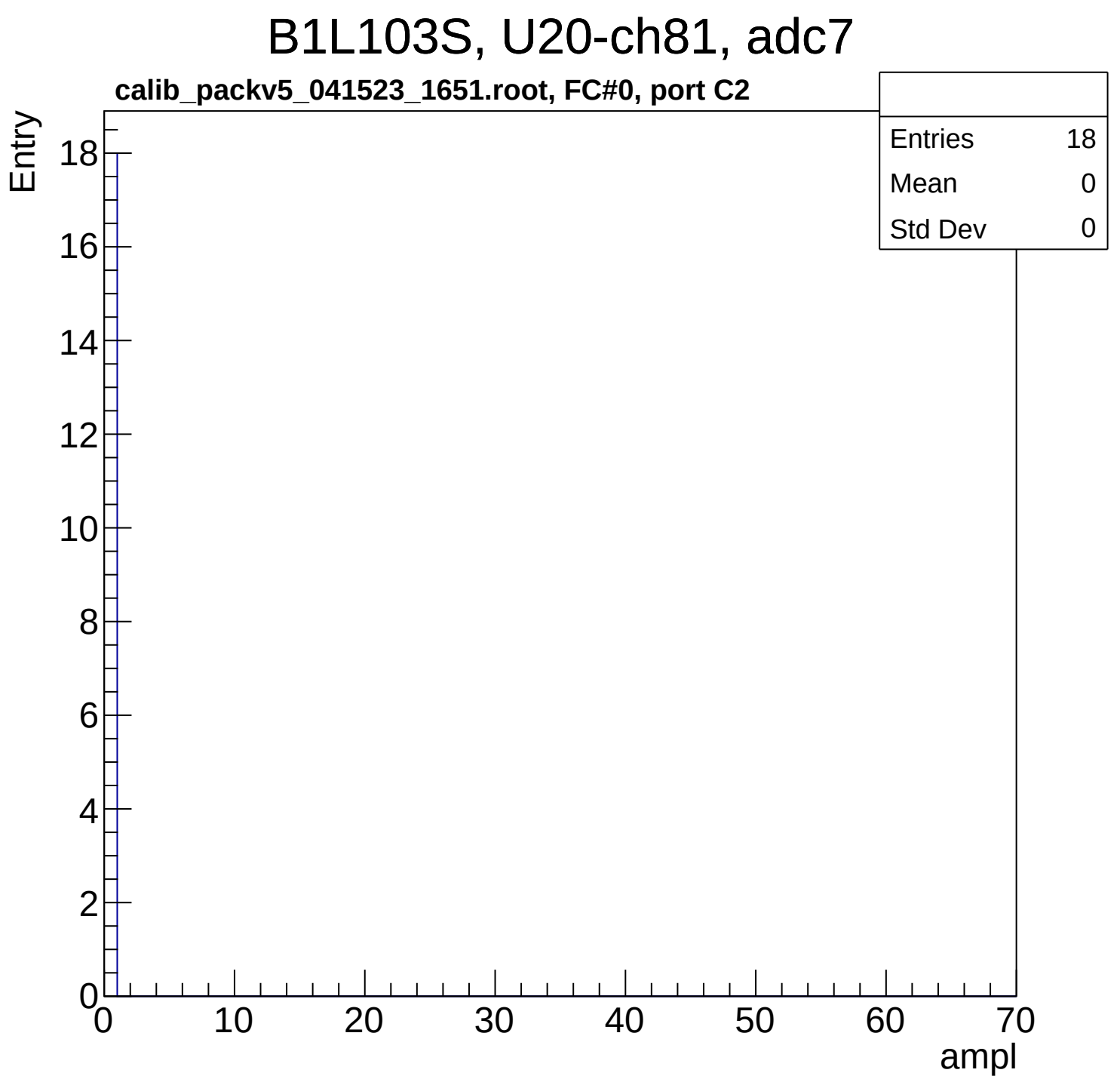
40
50
60
70


B1L103S, U20-ch81, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
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6
8
10
12
14
16
18
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10
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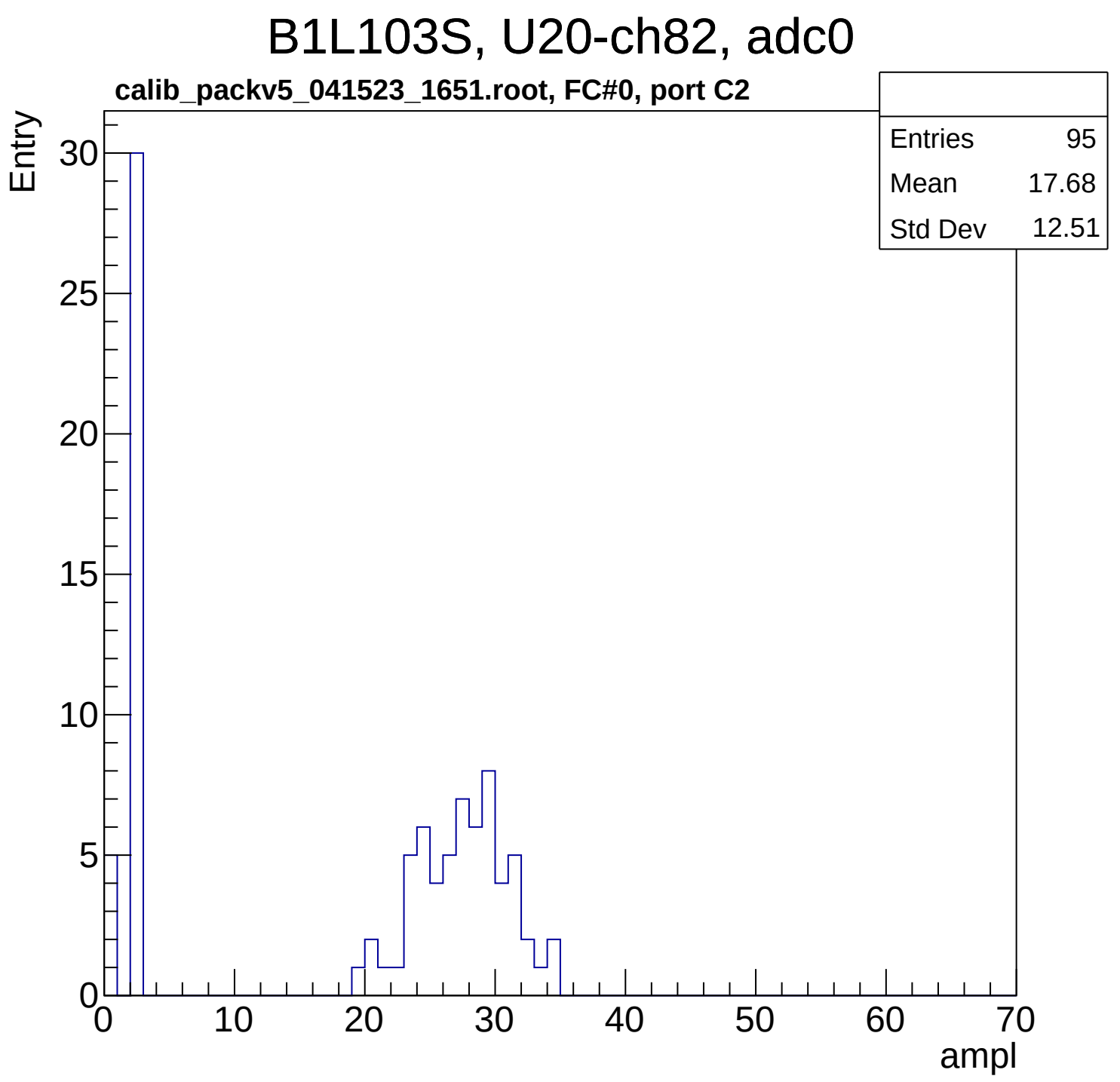
50
60
70
ampl


B1L103S, U20-ch82, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 17.68
Std Dev 12.51
Entry
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5
10
15
20
25
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10
20
30
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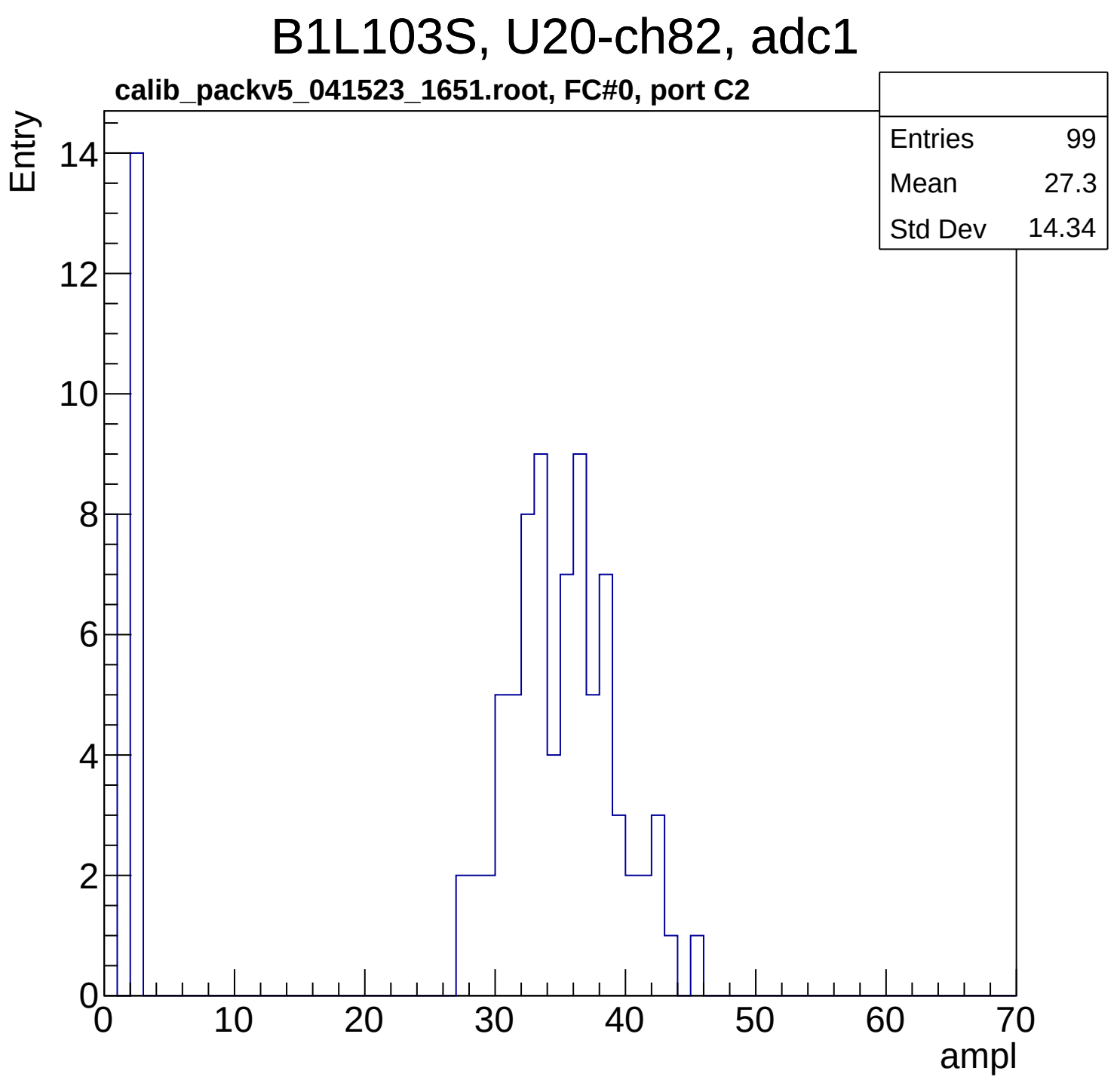
50
60
70
ampl


B1L103S, U20-ch82, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 27.3
Std Dev 14.34
Entry
ampl
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2
4
6
8
10
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0
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20
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60
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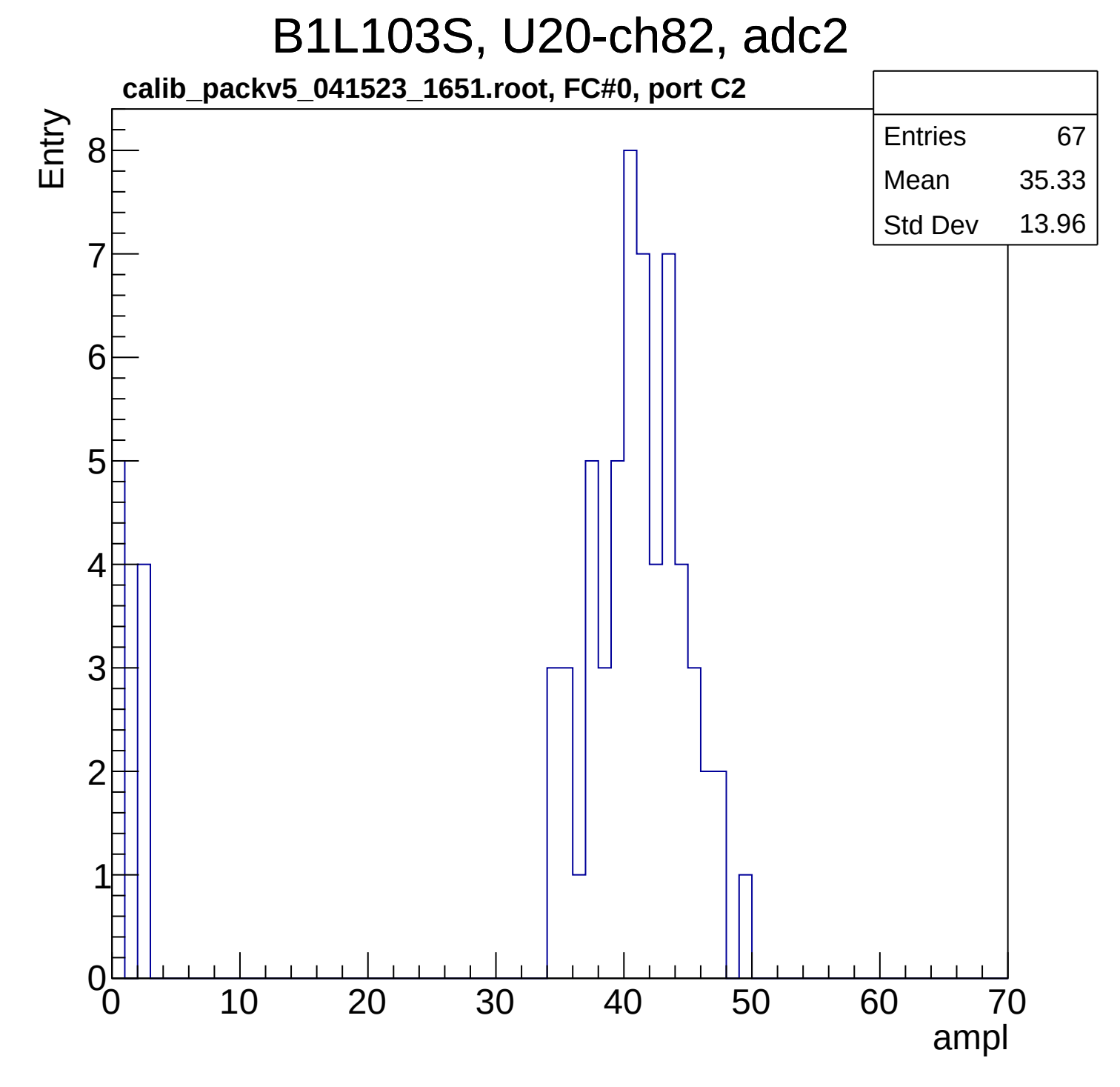
B1L103S, U20-ch82, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 35.33
Std Dev 13.96
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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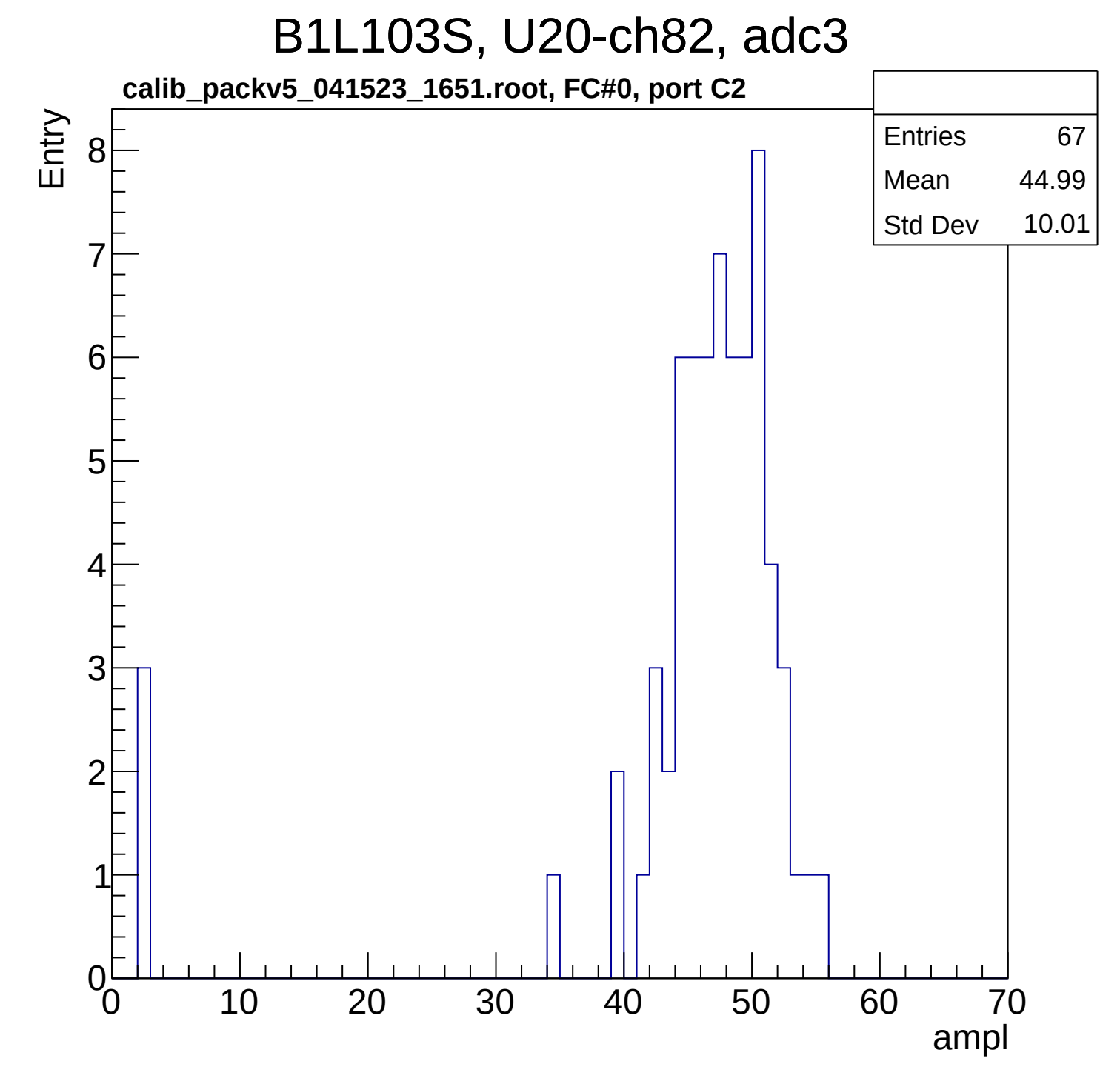
60
70


B1L103S, U20-ch82, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 44.99
Std Dev 10.01
Entry
ampl
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2
3
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5
6
7
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0
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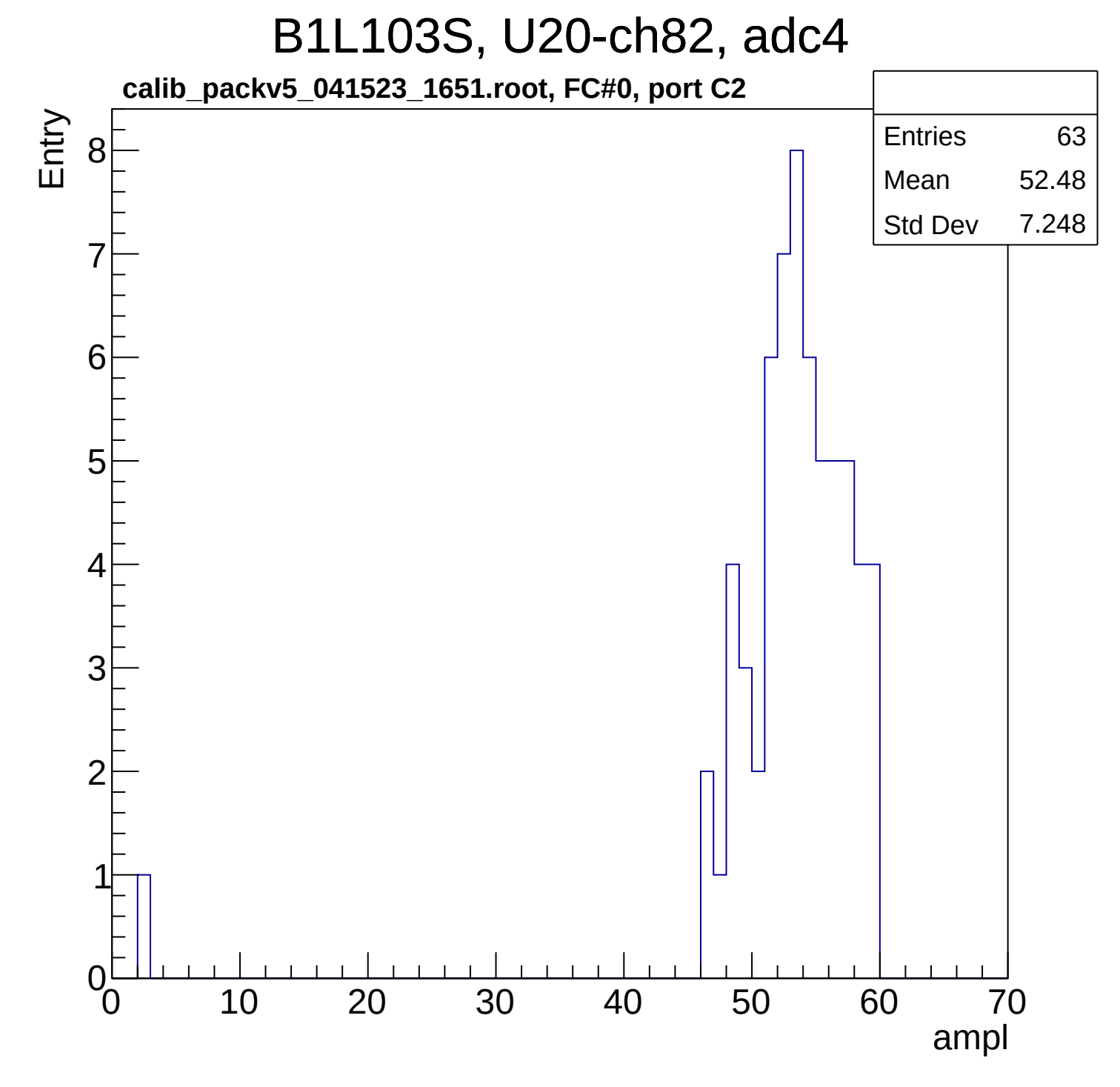
B1L103S, U20-ch82, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 52.48
Std Dev 7.248
Entry
ampl
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2
3
4
5
6
7
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0
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60
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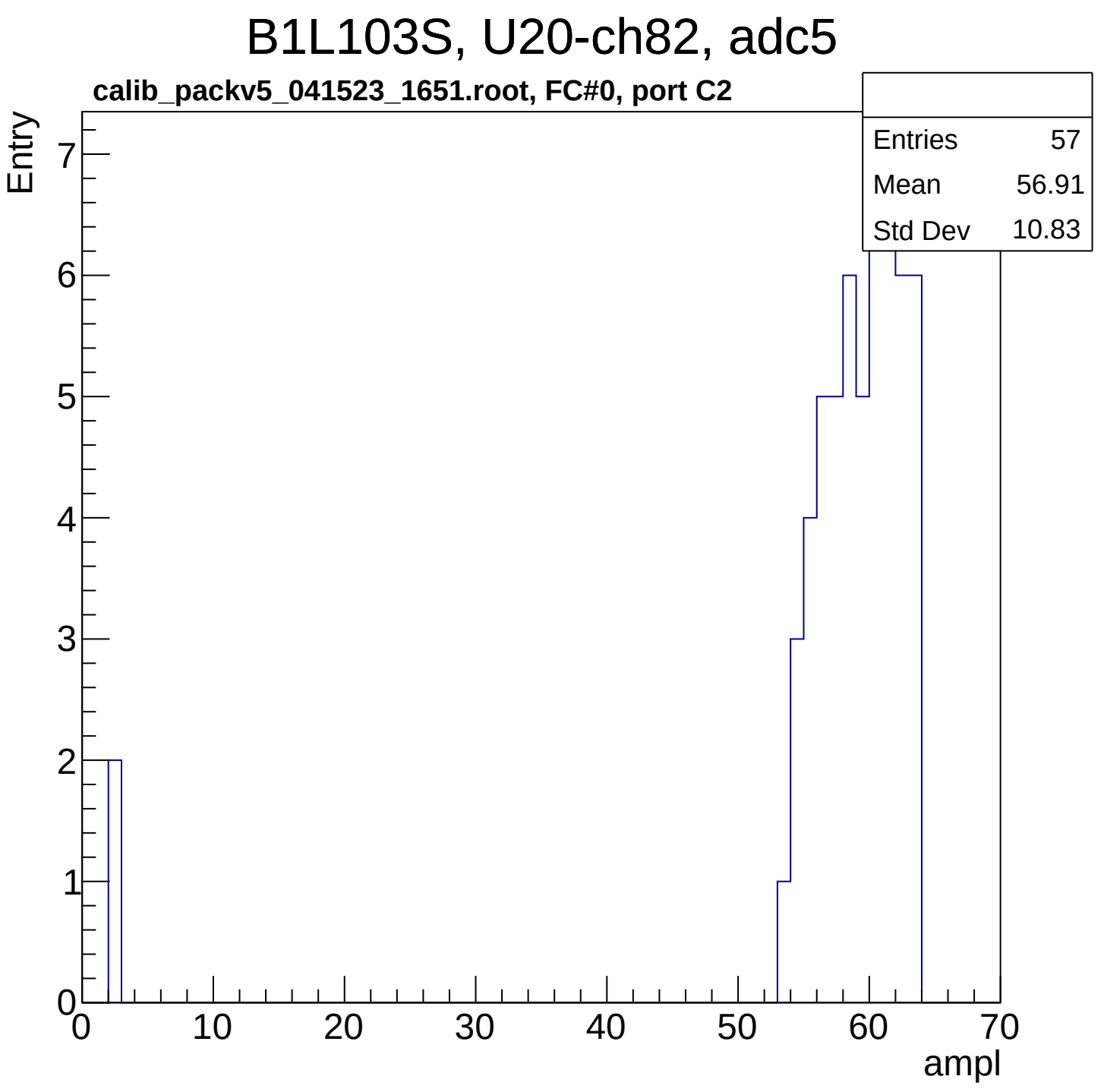
B1L103S, U20-ch82, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 56.91
Std Dev 10.83
Entry
ampl
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1
2
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4
5
6
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0
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60
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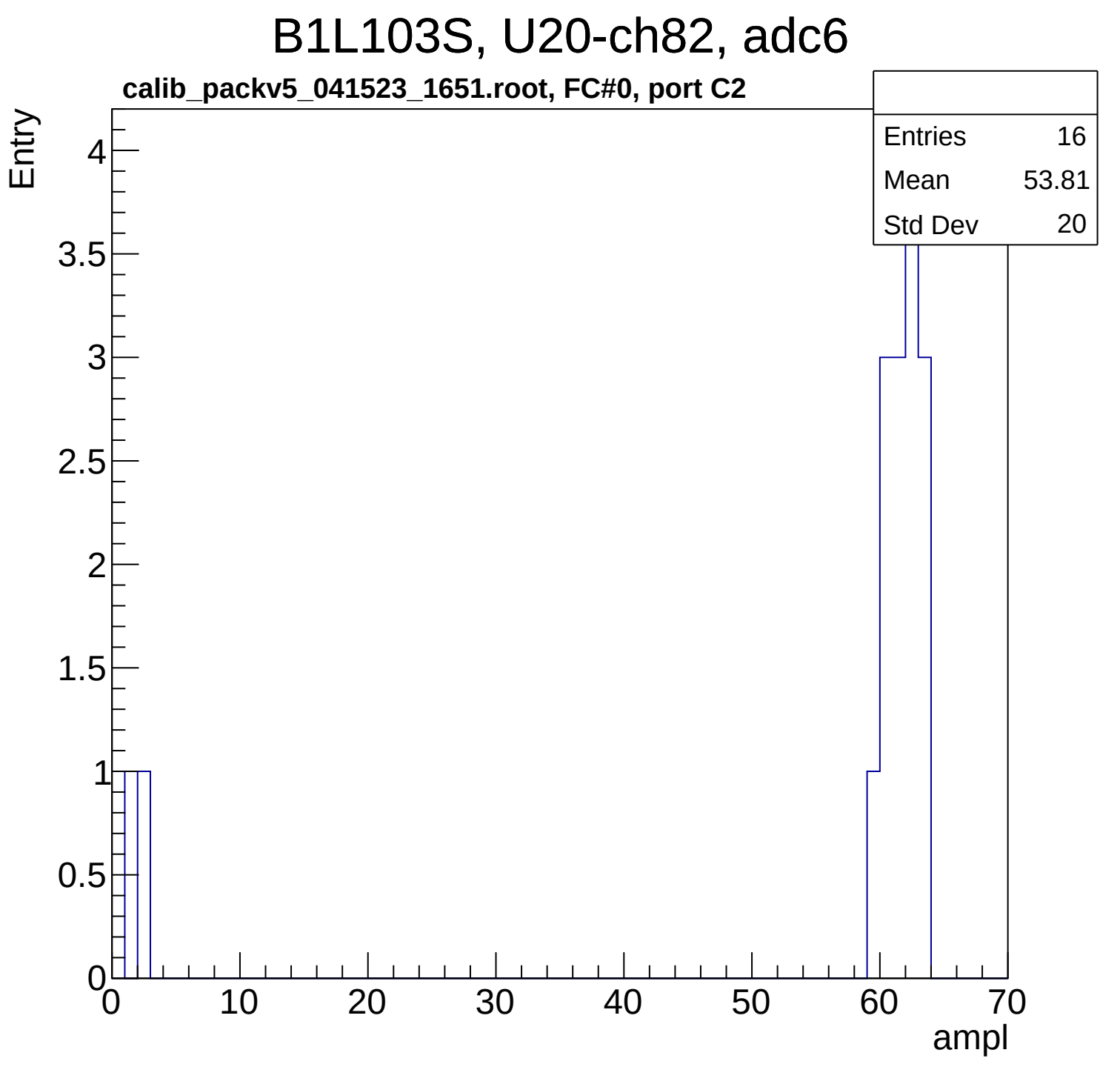
B1L103S, U20-ch82, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 53.81
Std Dev 20
Entry
ampl
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1.5
2
2.5
3
3.5
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0
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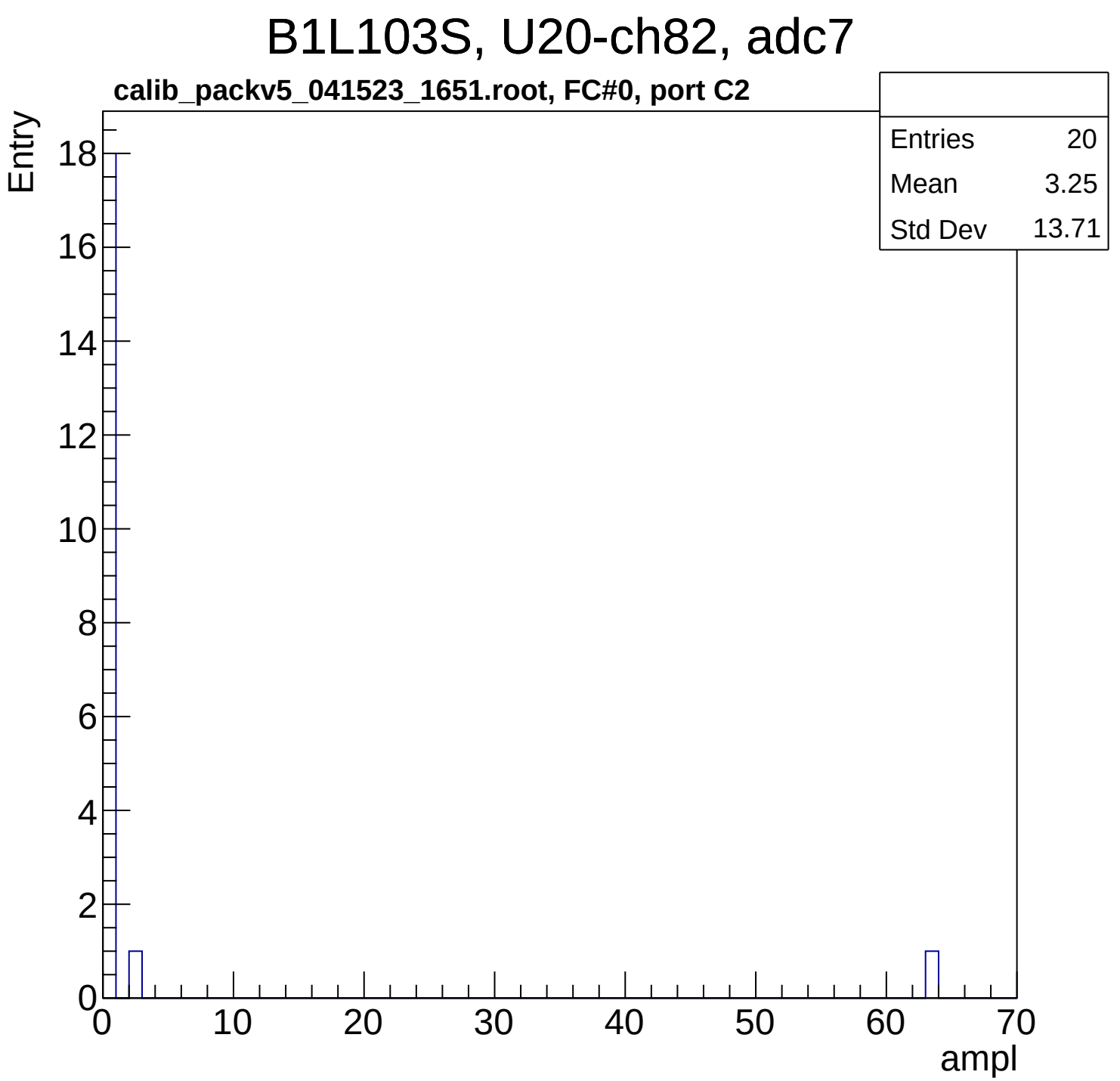
B1L103S, U20-ch82, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.25
Std Dev 13.71
Entry
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10
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14
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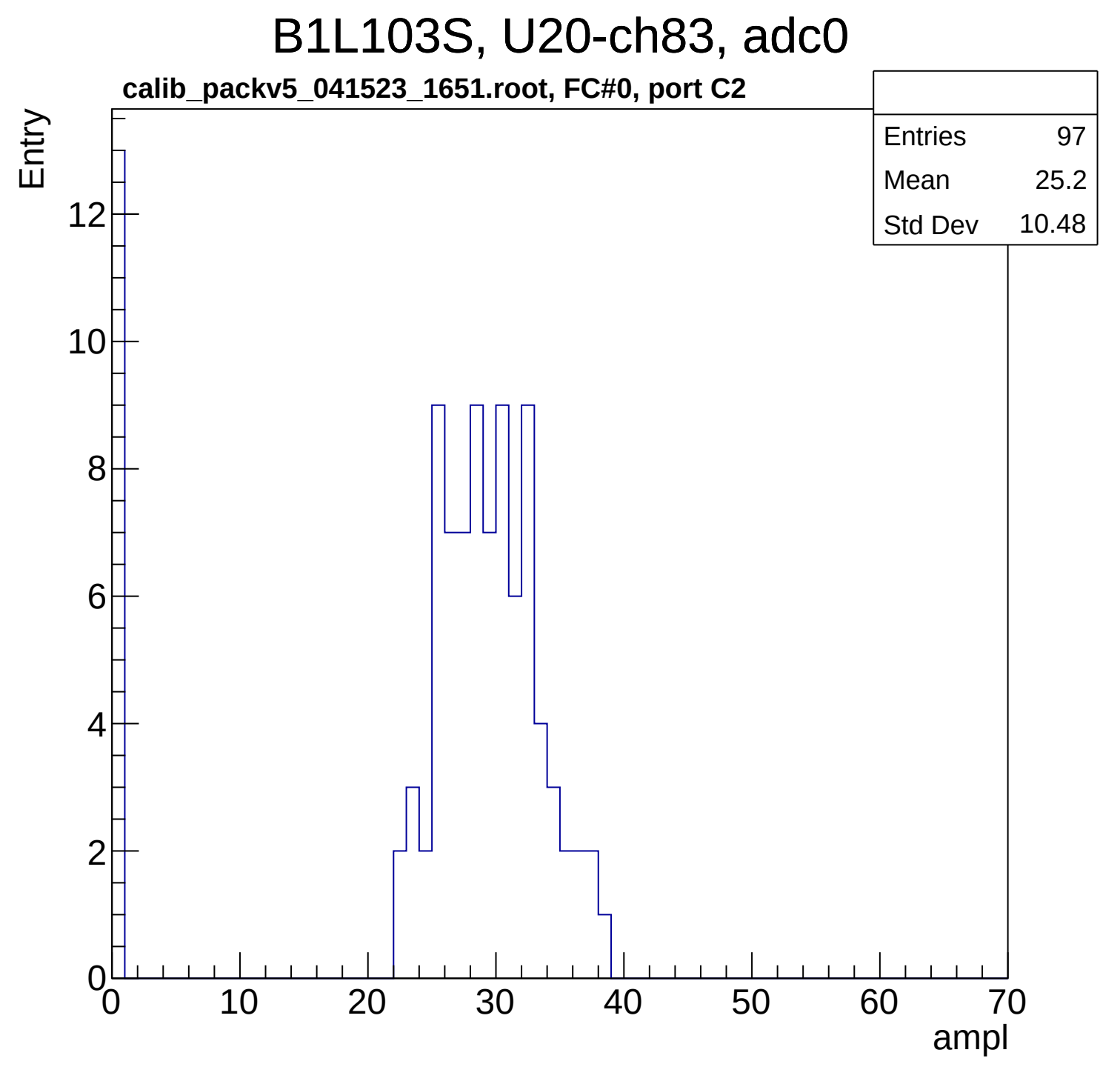
50
60
70
ampl


B1L103S, U20-ch83, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 25.2
Std Dev 10.48
Entry
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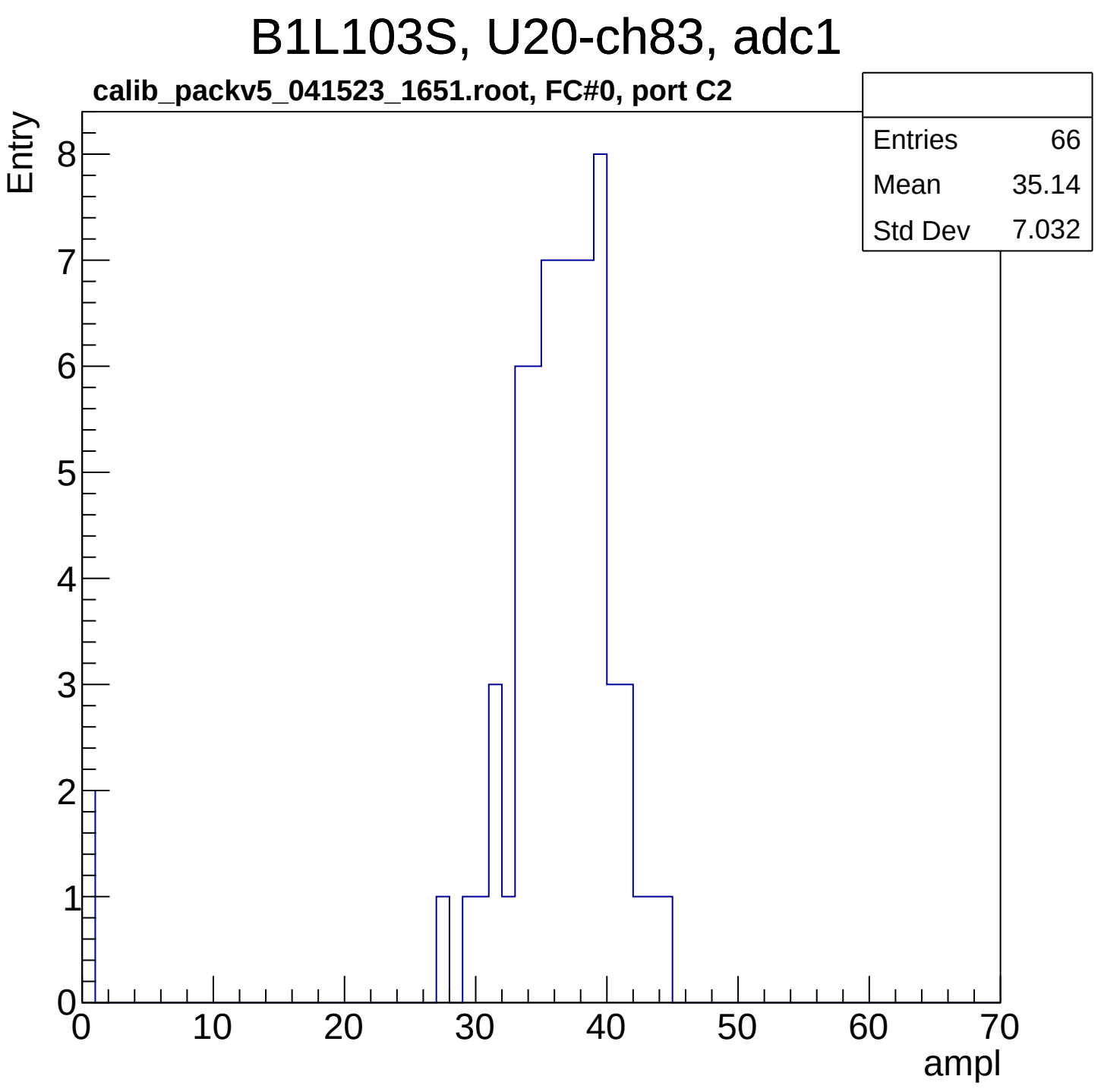
30
40
50
60
70
ampl


B1L103S, U20-ch83, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 35.14
Std Dev 7.032
Entry
ampl
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3
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5
6
7
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0
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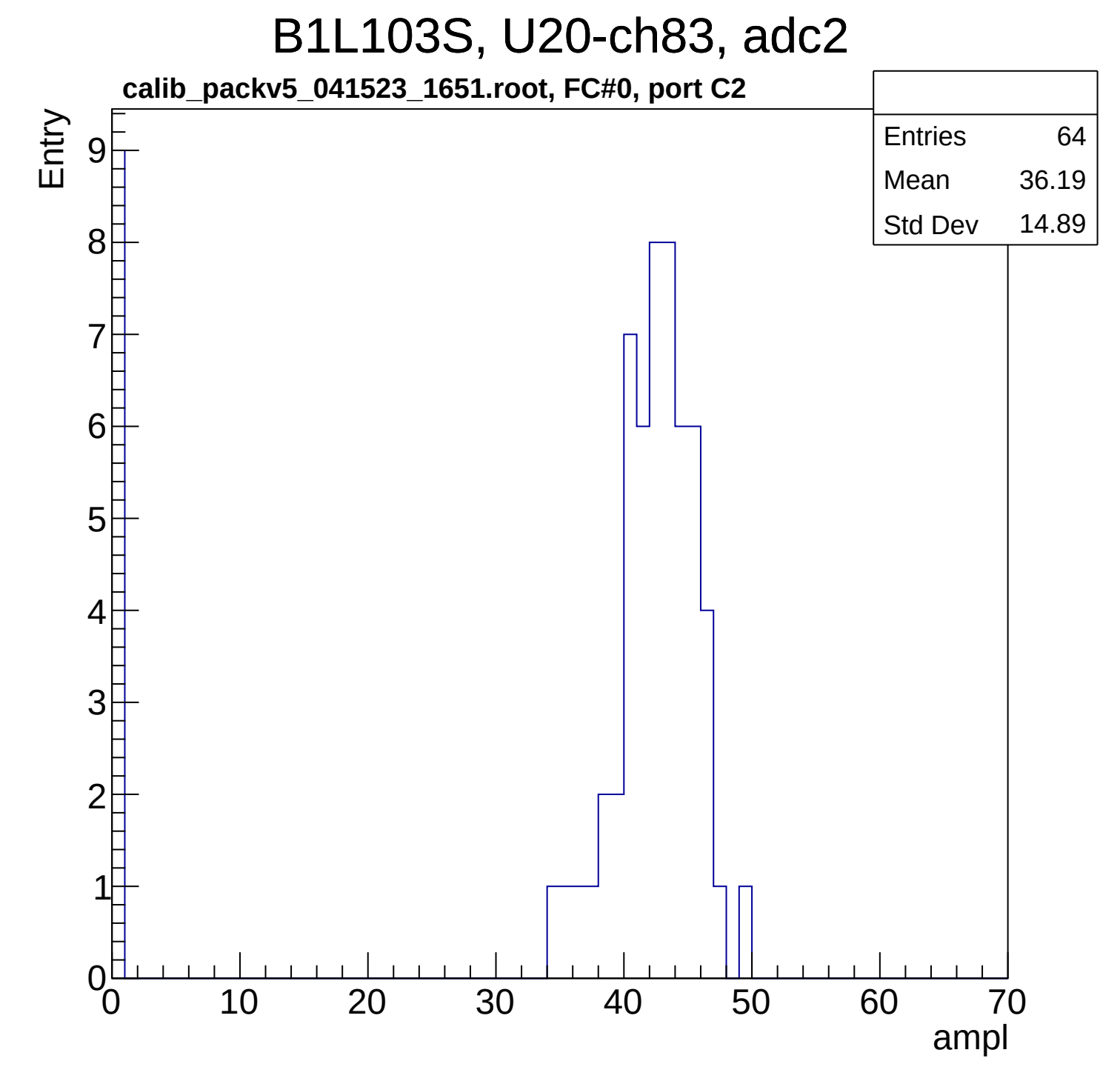
B1L103S, U20-ch83, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 36.19
Std Dev 14.89
Entry
ampl
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3
4
5
6
7
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0
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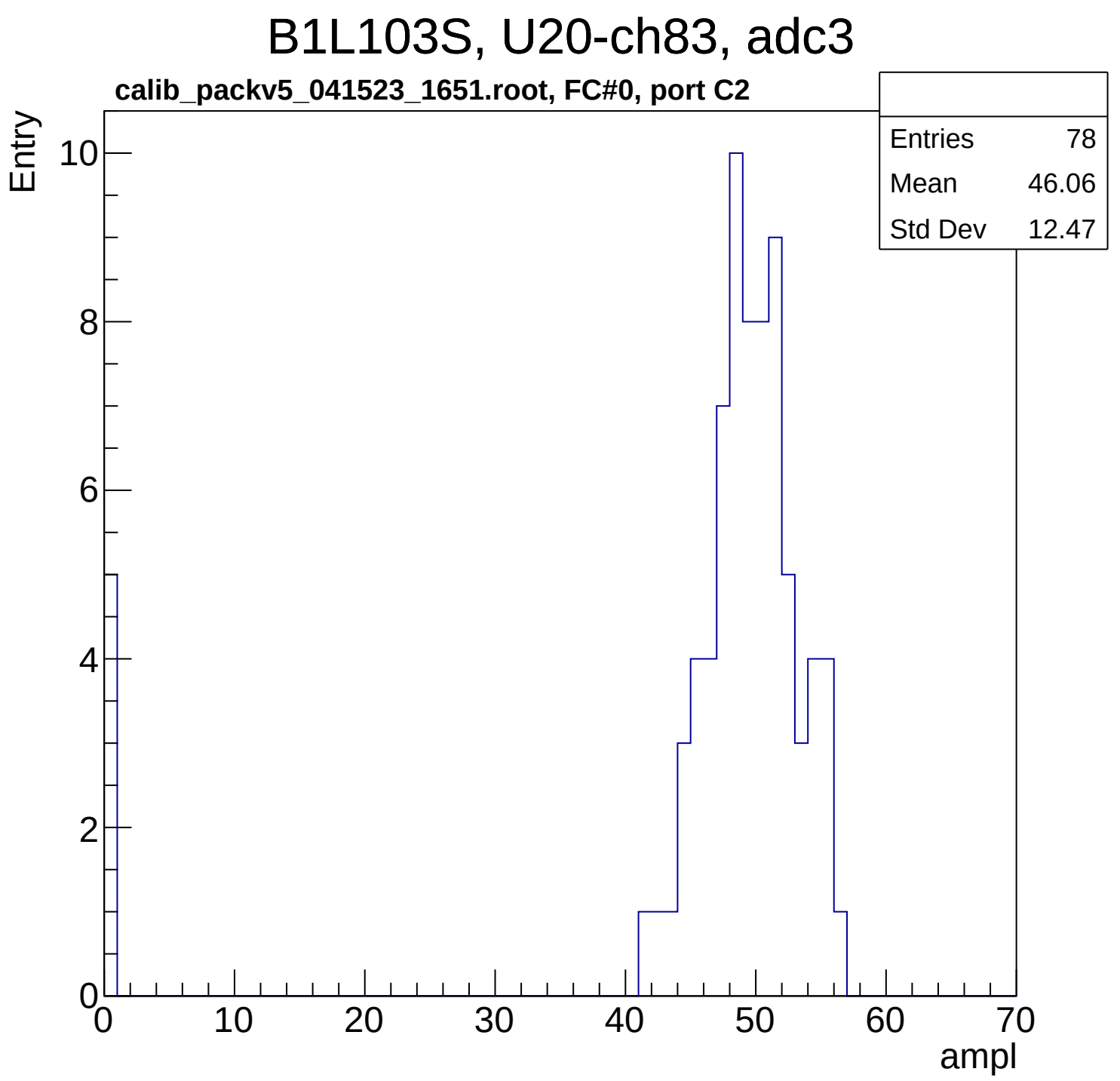
B1L103S, U20-ch83, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 46.06
Std Dev 12.47
Entry
ampl
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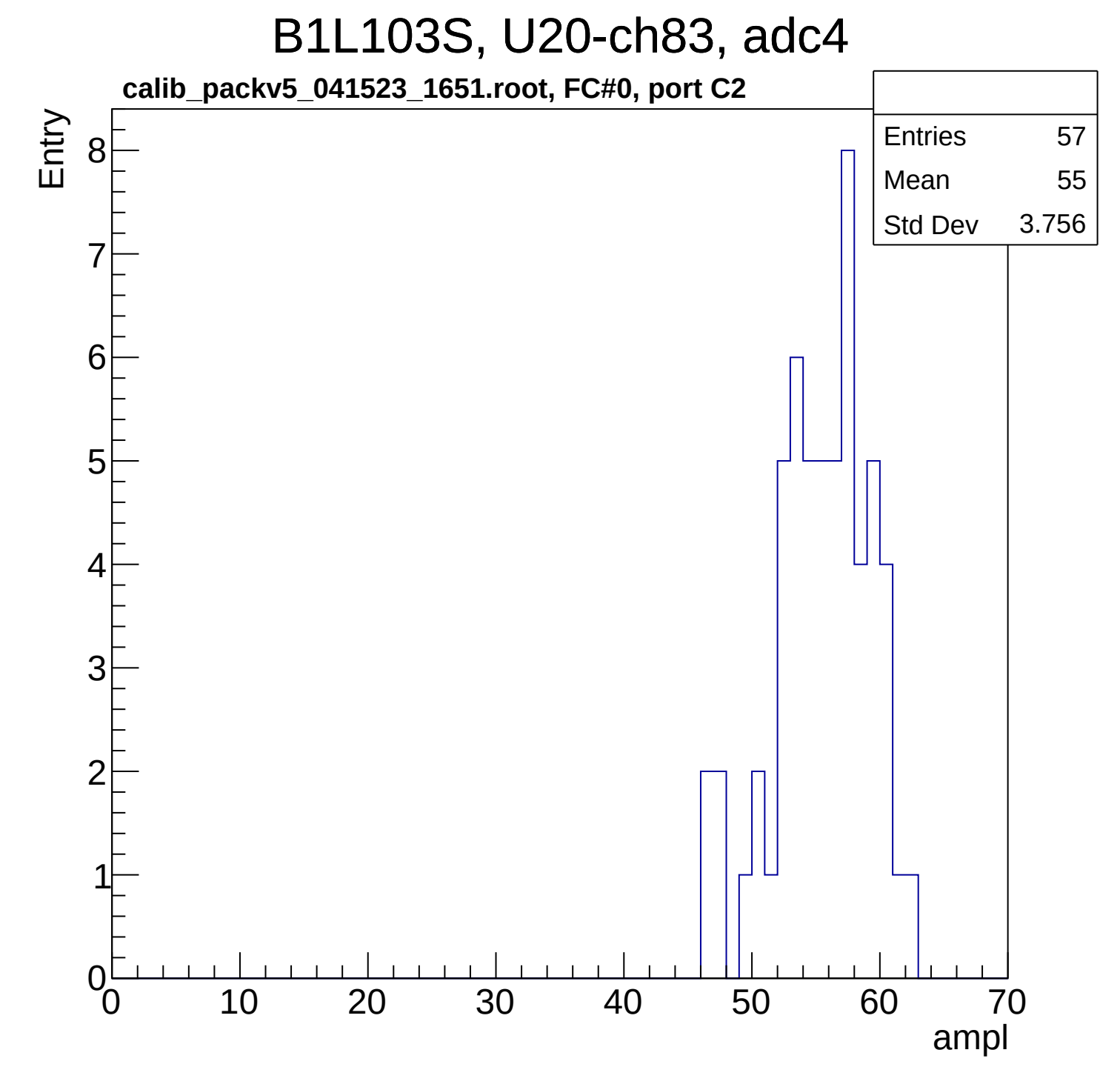
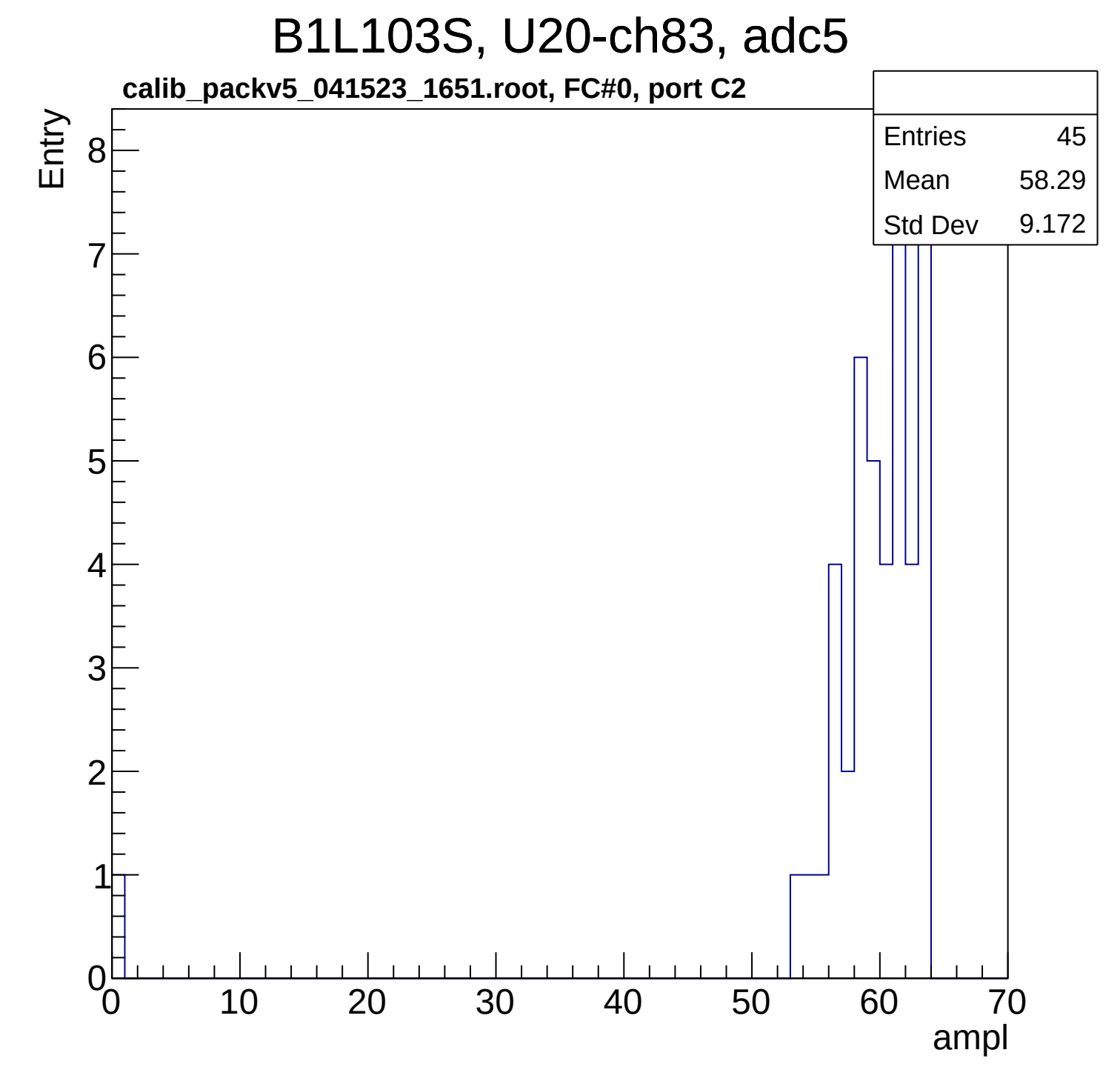

B1L103S, U20-ch83, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 55
Std Dev 3.756
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch83, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 58.29
Std Dev 9.172
Entry
ampl
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1
2
3
4
5
6
7
8
0
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40
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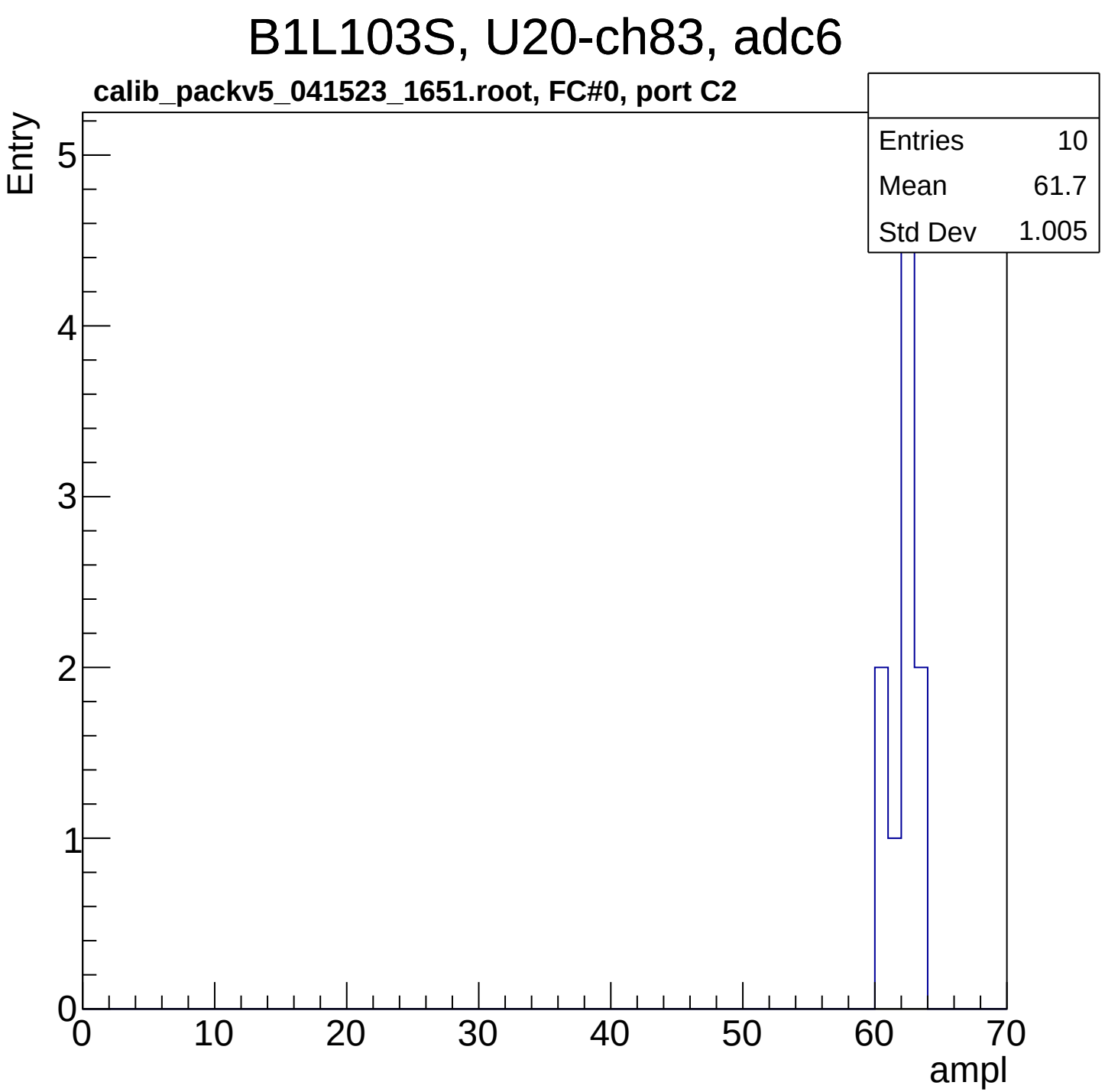
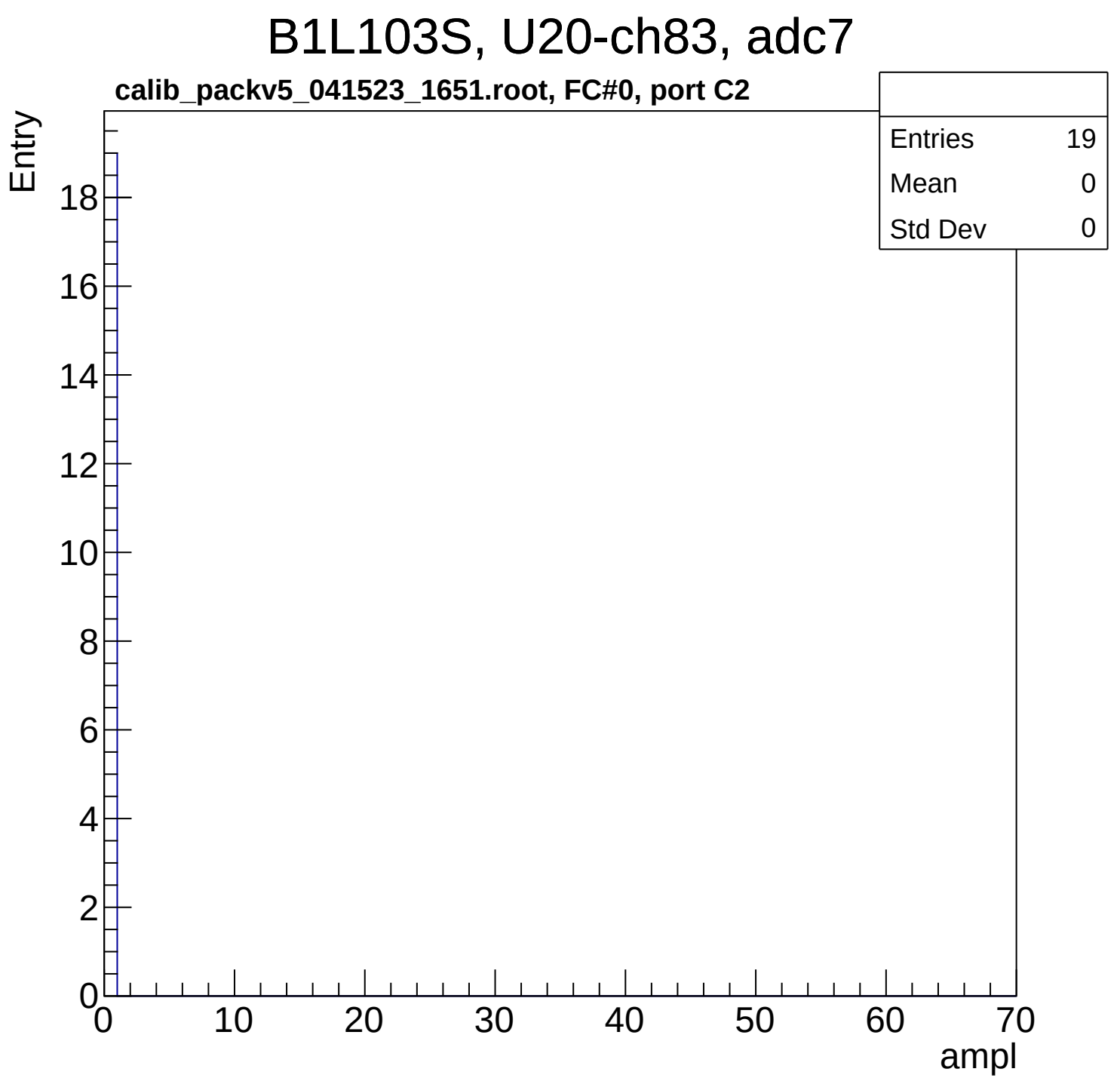
60
70


B1L103S, U20-ch83, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61.7
Std Dev 1.005
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch83, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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2
4
6
8
10
12
14
16
18
0
10
20
30
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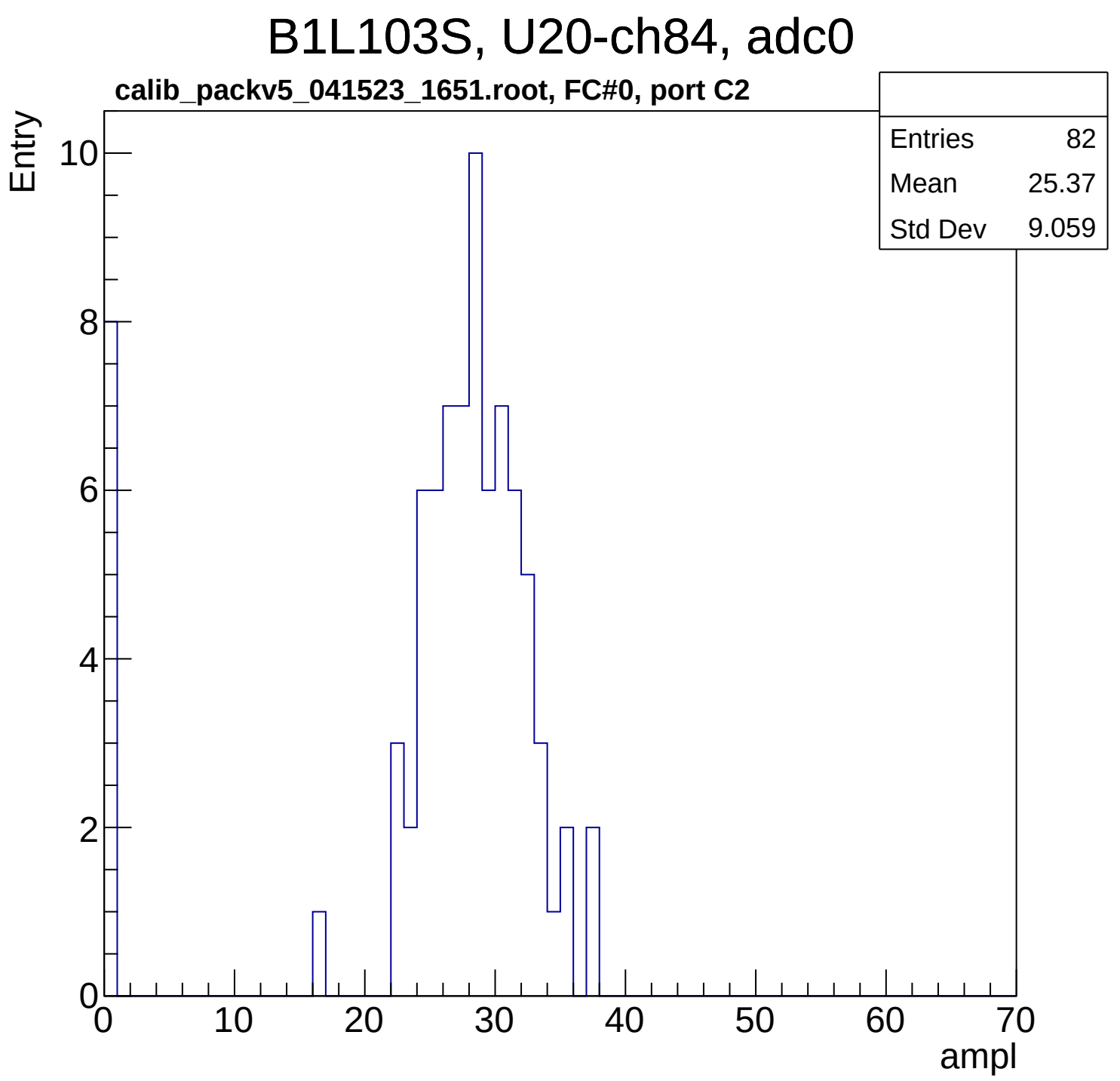
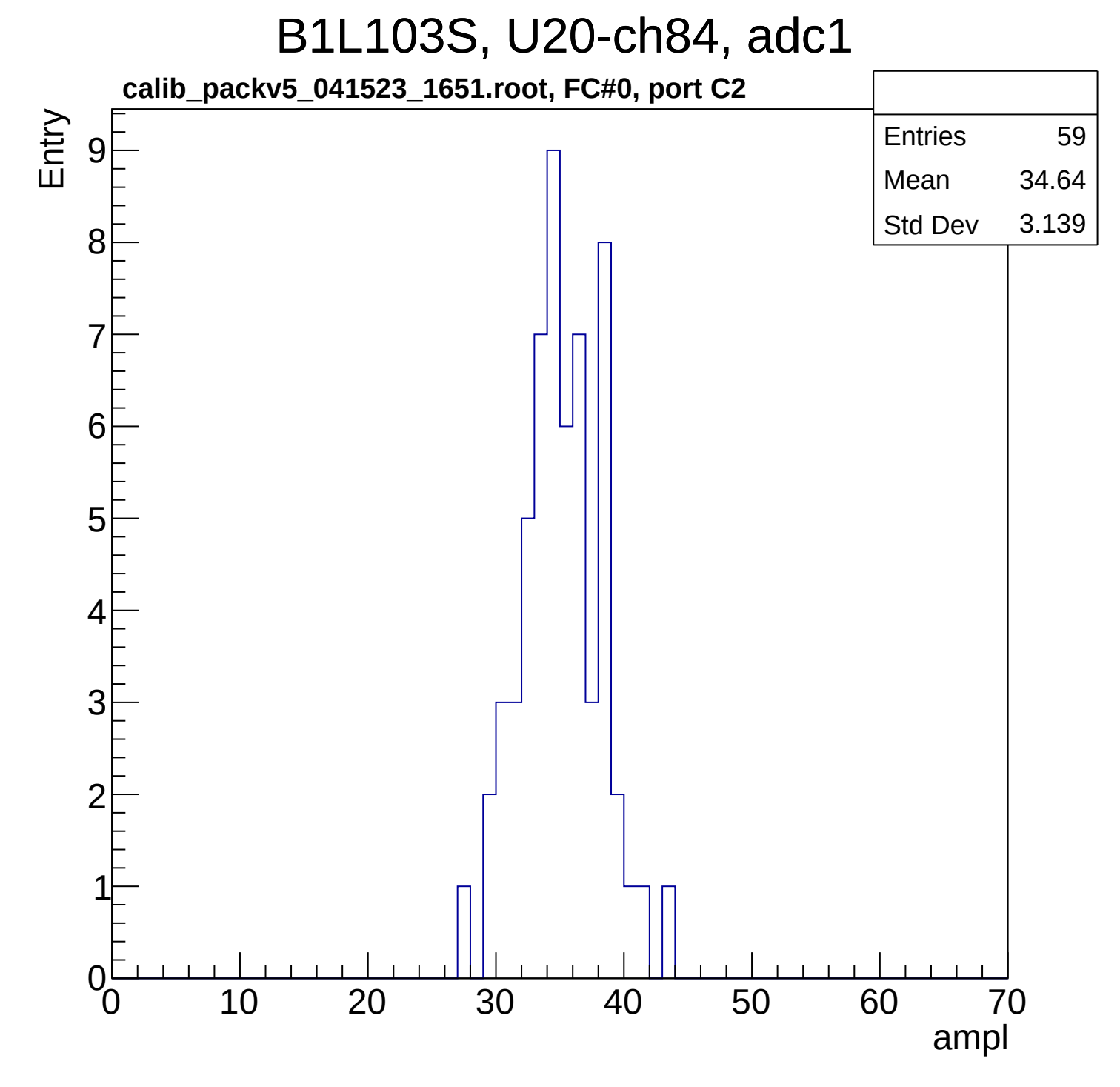
50
60
70
ampl


B1L103S, U20-ch84, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 25.37
Std Dev 9.059
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U20-ch84, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 34.64
Std Dev 3.139
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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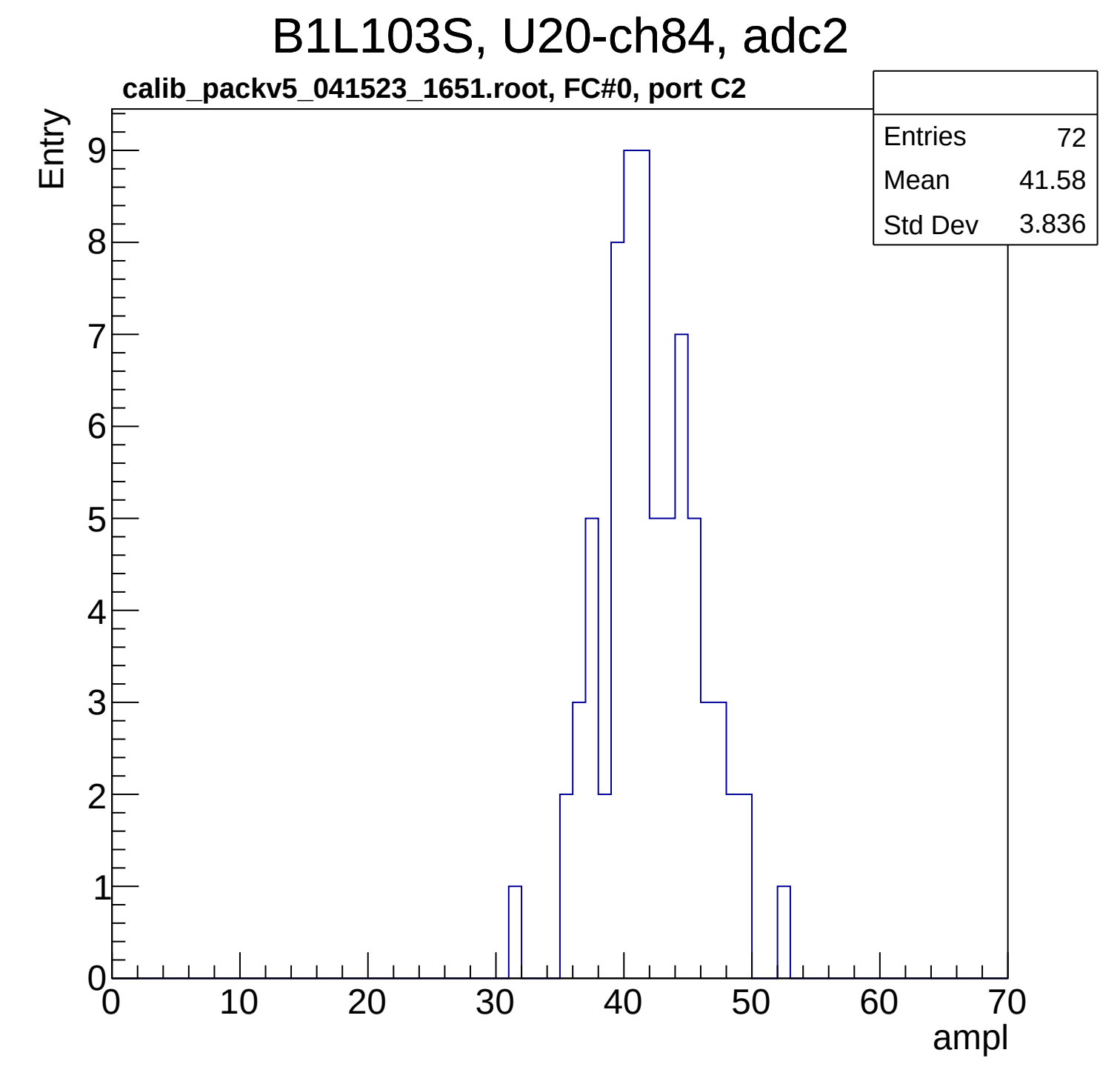
B1L103S, U20-ch84, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 41.58
Std Dev 3.836
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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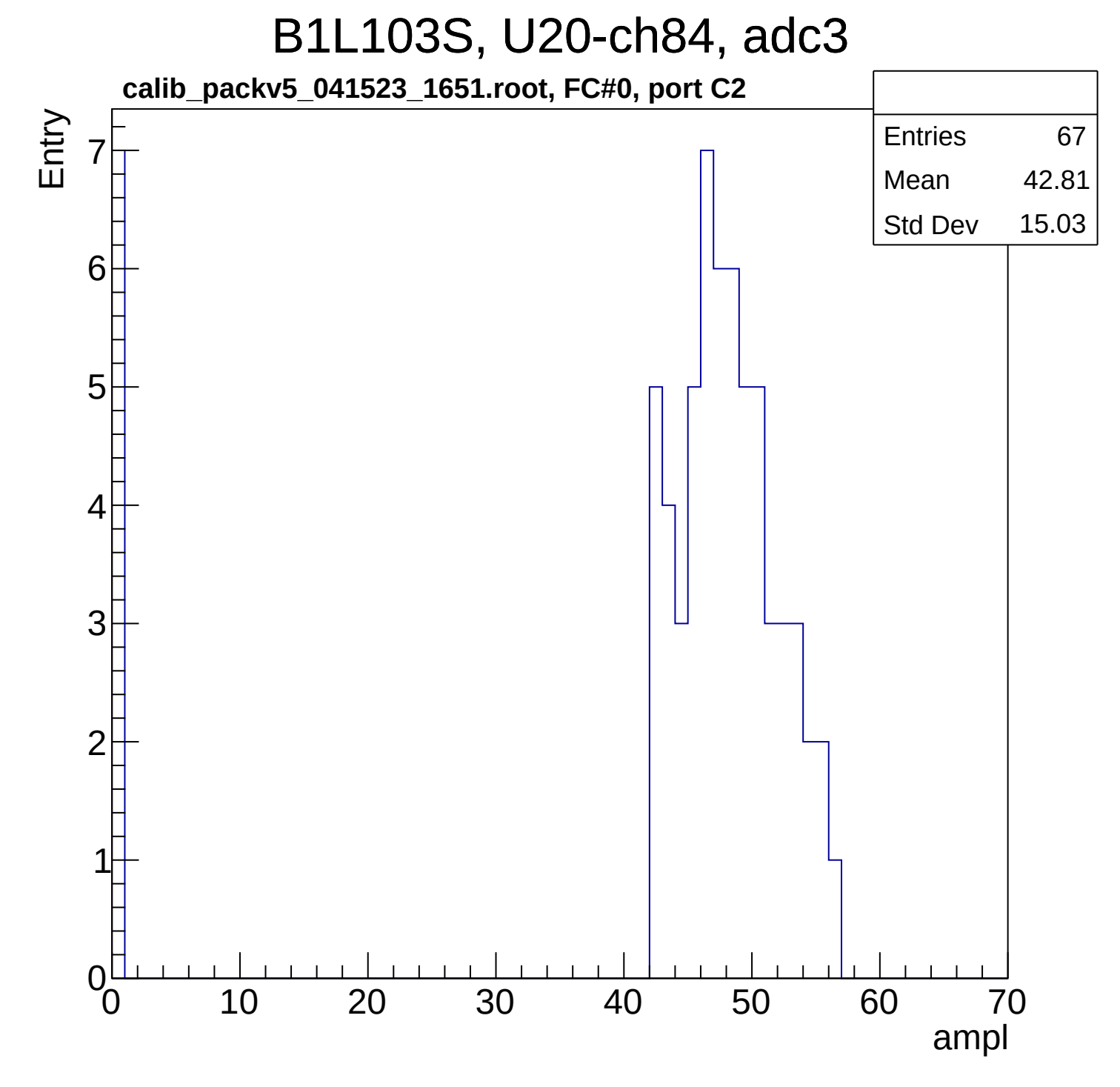
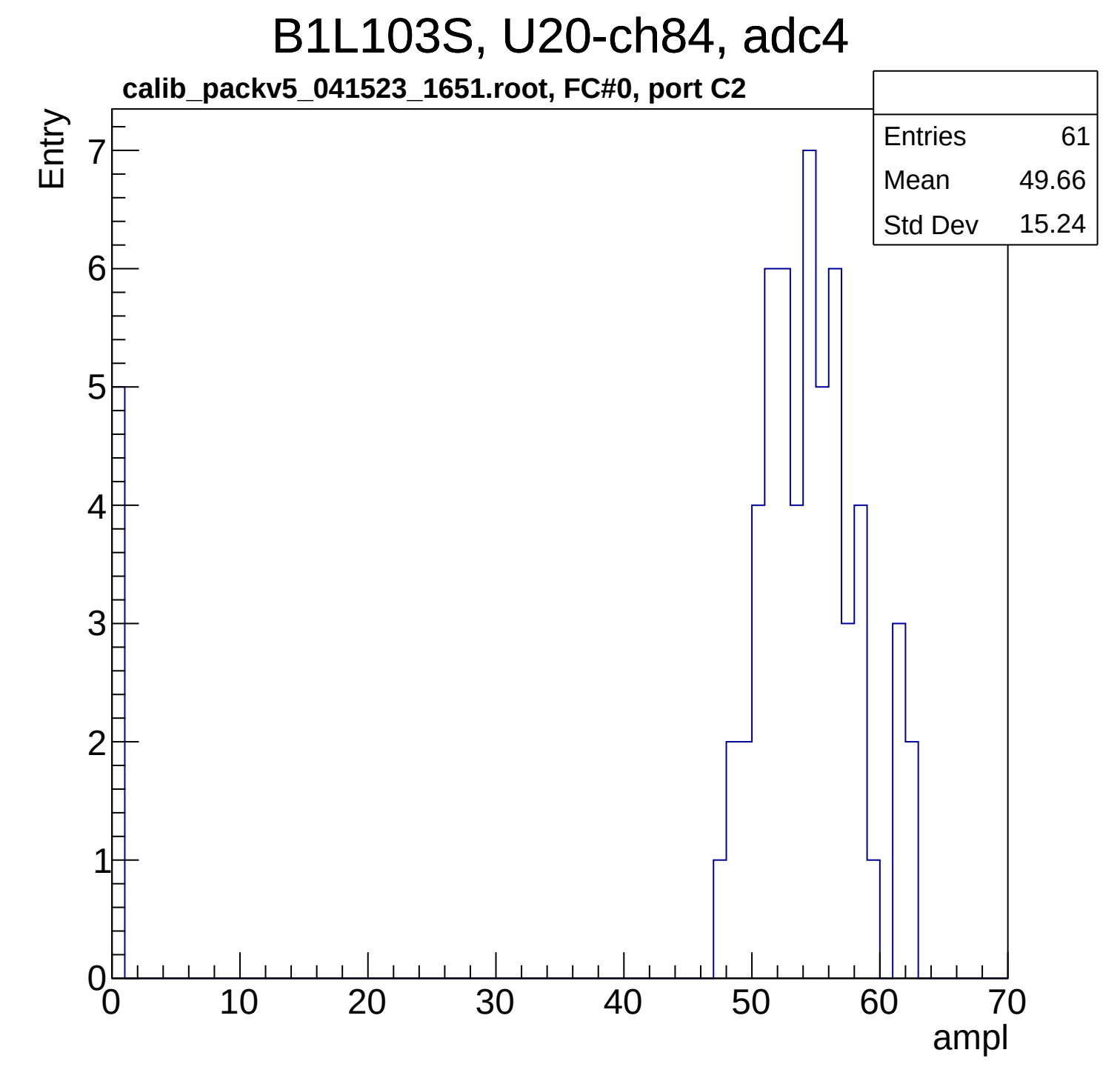

B1L103S, U20-ch84, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 42.81
Std Dev 15.03
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U20-ch84, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 49.66
Std Dev 15.24
Entry
ampl
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1
2
3
4
5
6
7
0
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40
50
60
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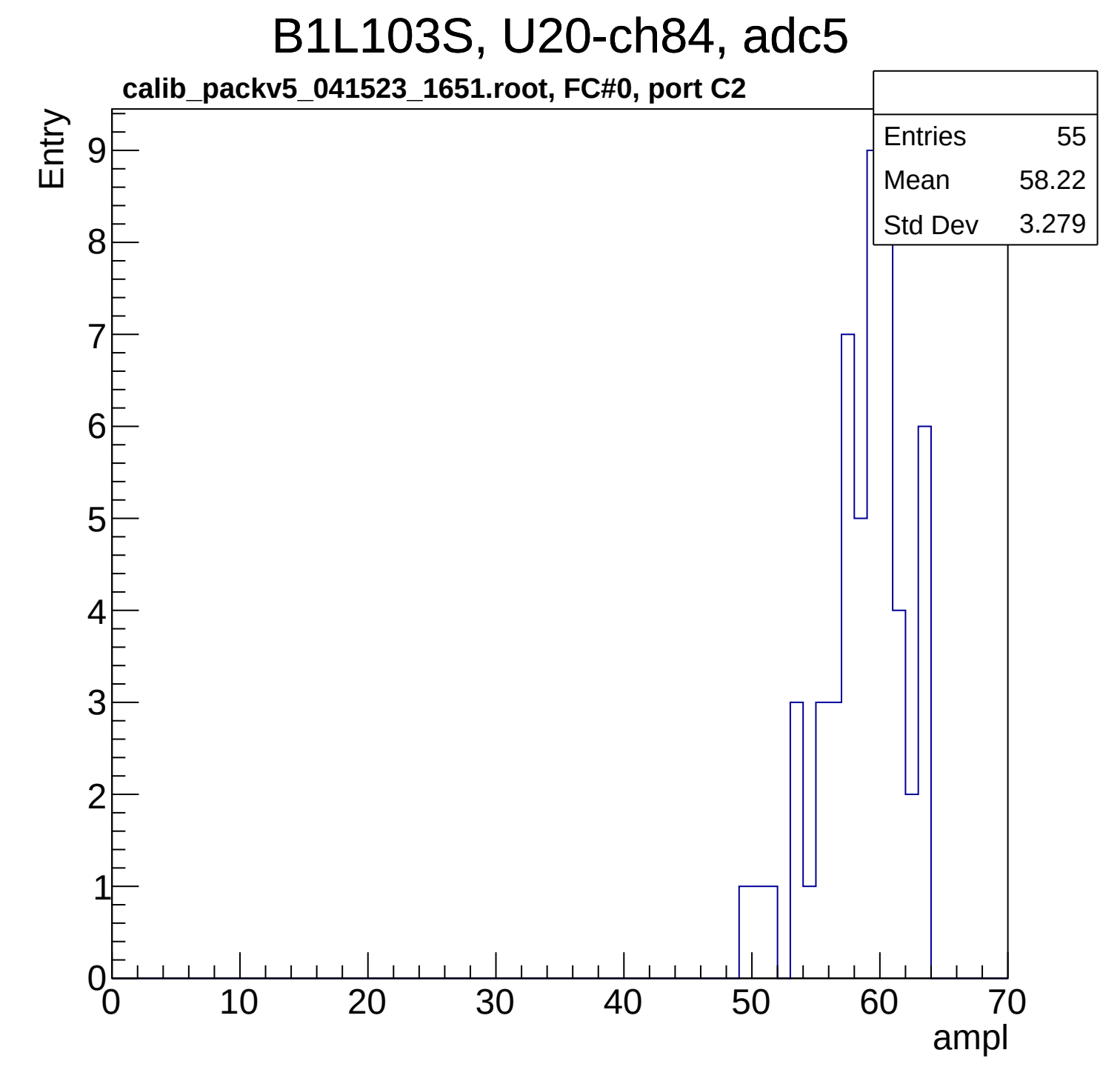
B1L103S, U20-ch84, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 58.22
Std Dev 3.279
Entry
ampl
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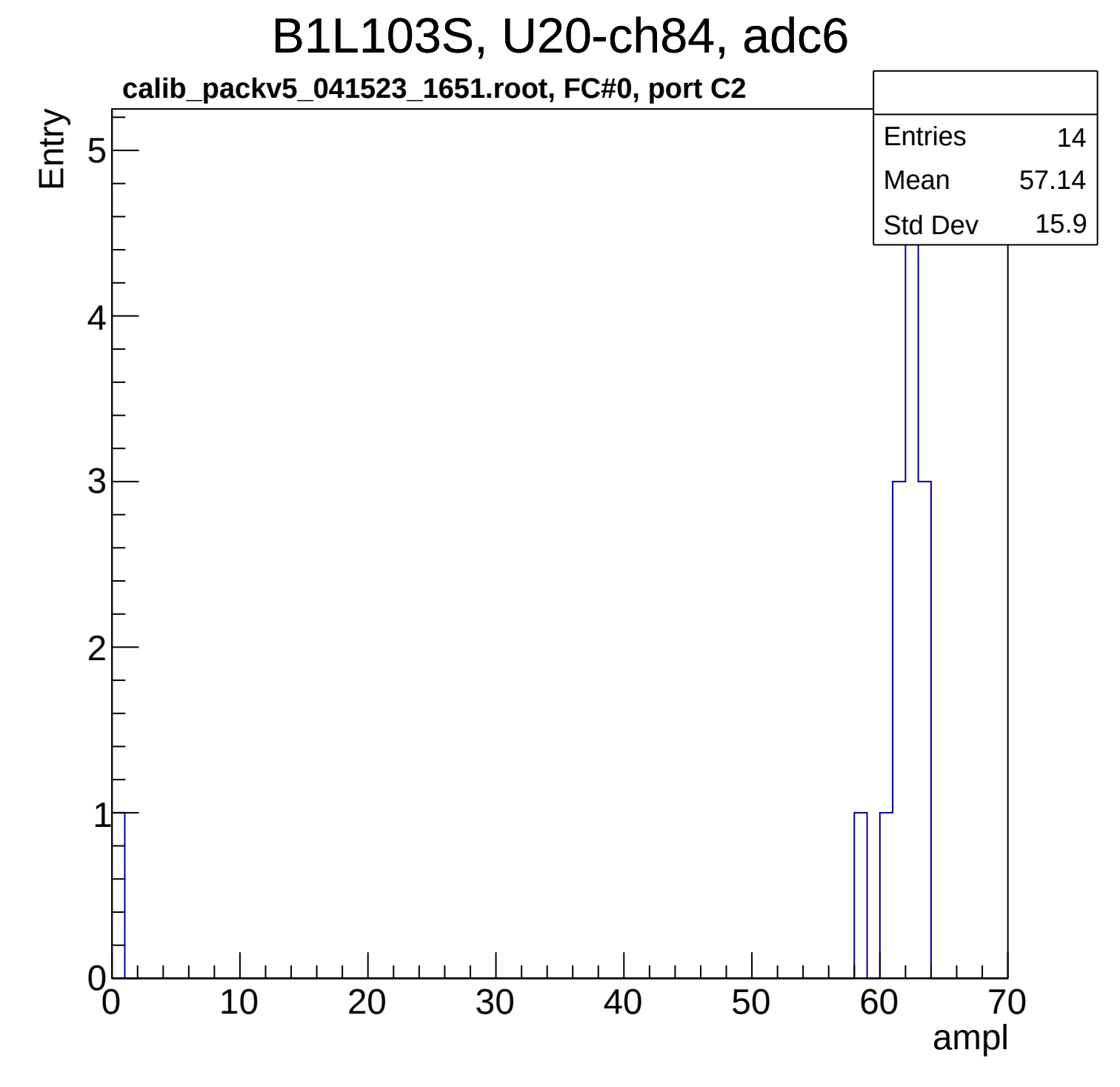
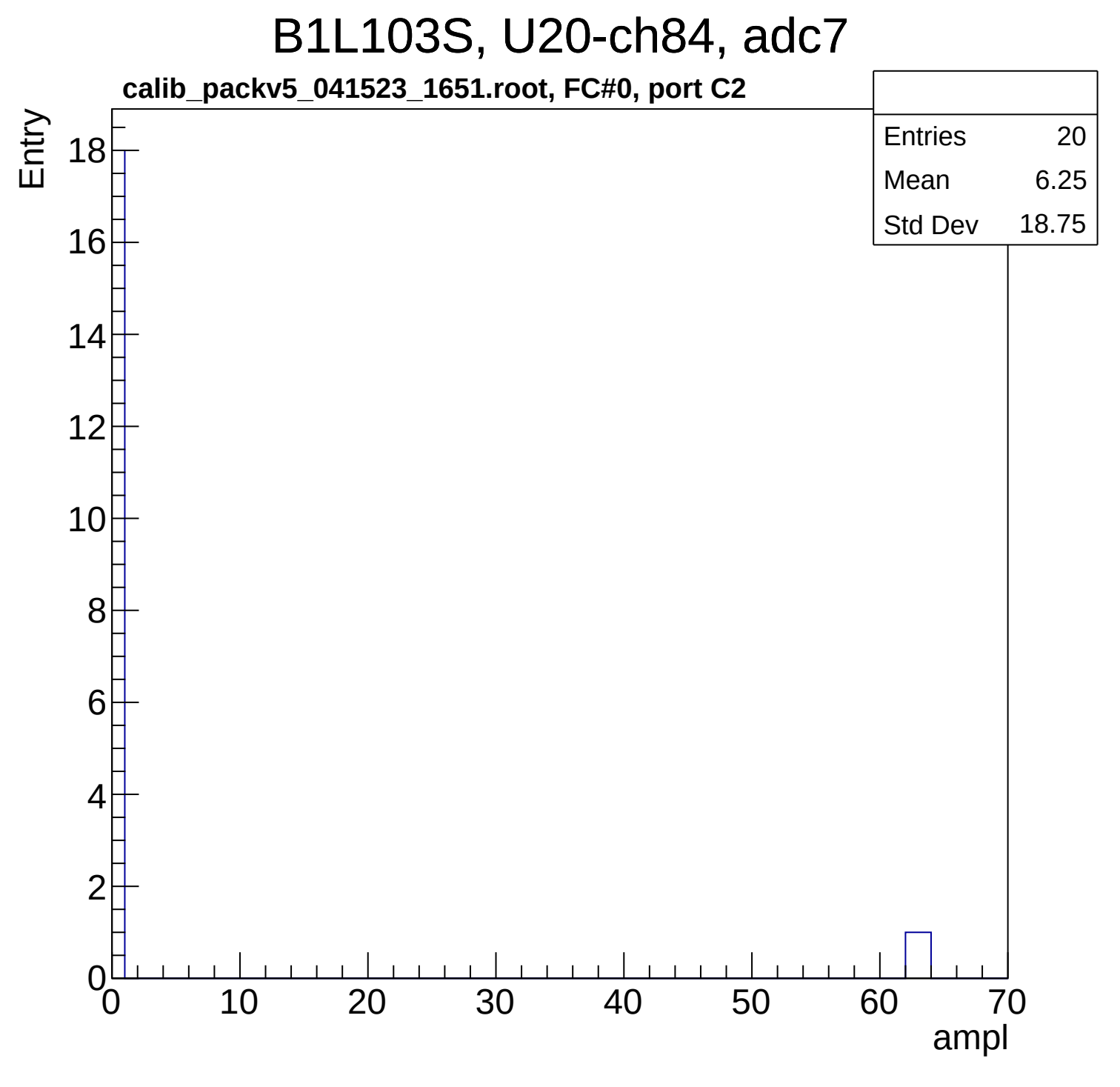
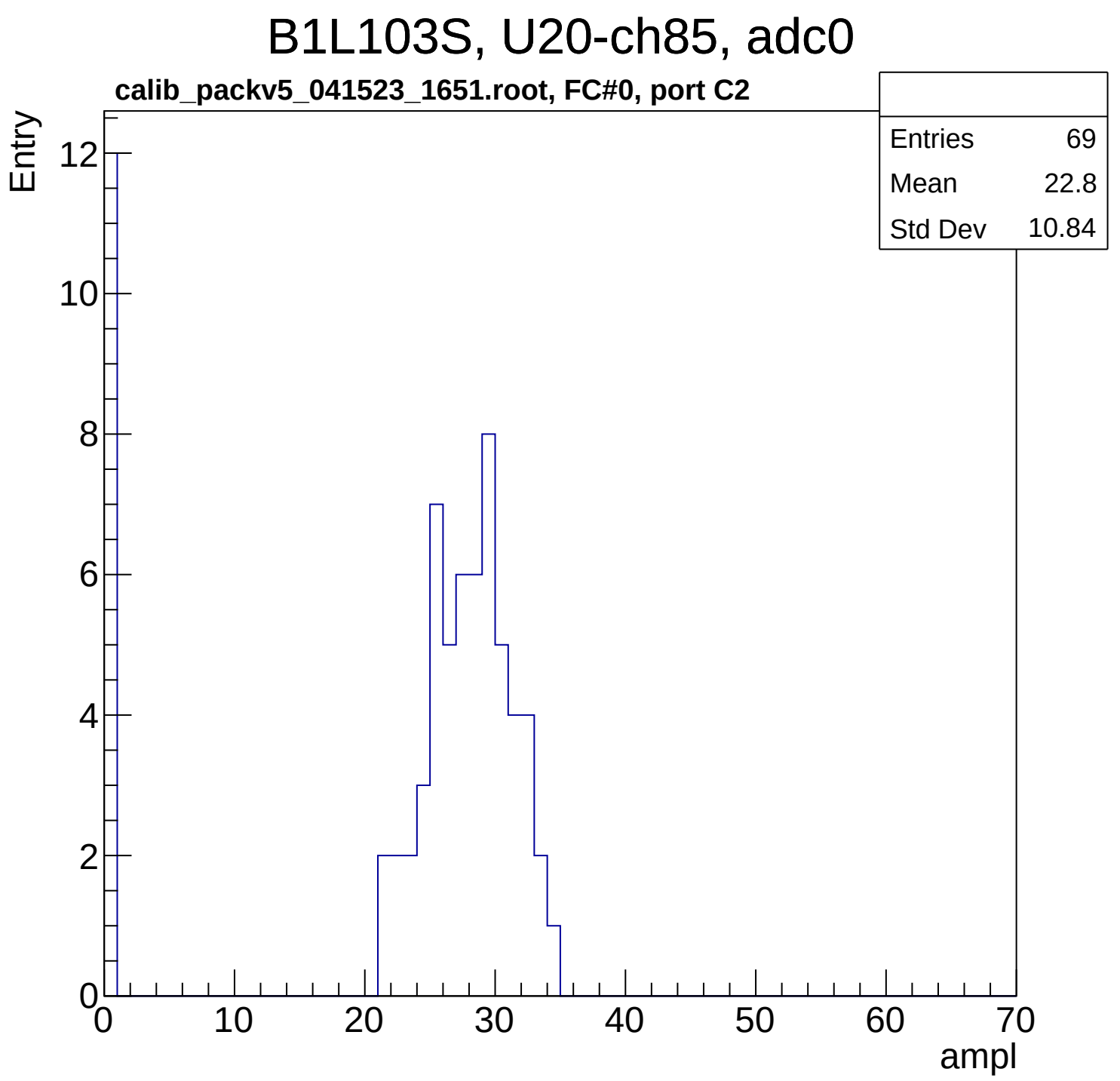
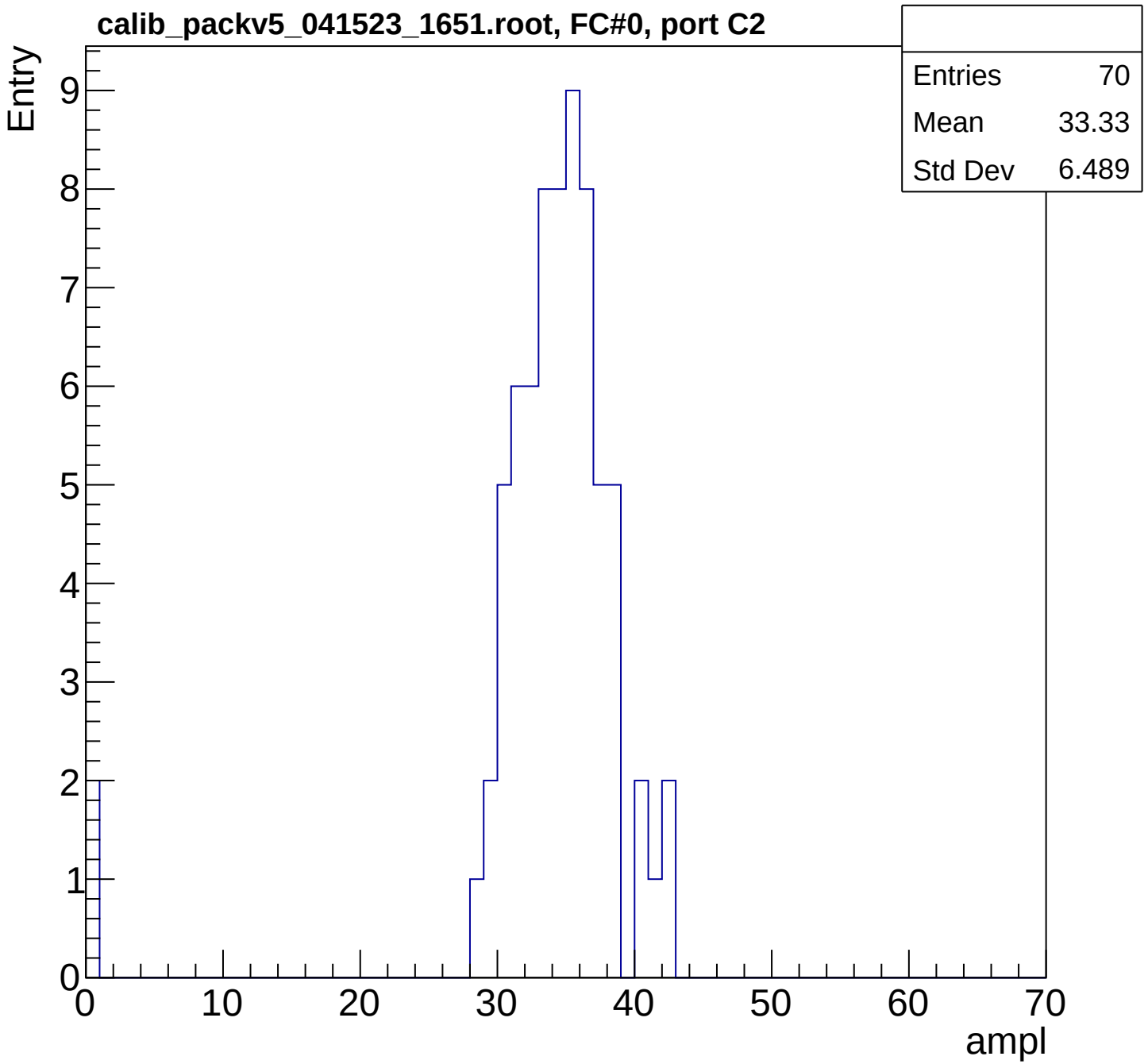
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch84, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 57.14
Std Dev 15.9
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch84, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 6.25
Std Dev 18.75
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch85, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 22.8
Std Dev 10.84
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch85, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 33.33
Std Dev 6.489
Entry
ampl
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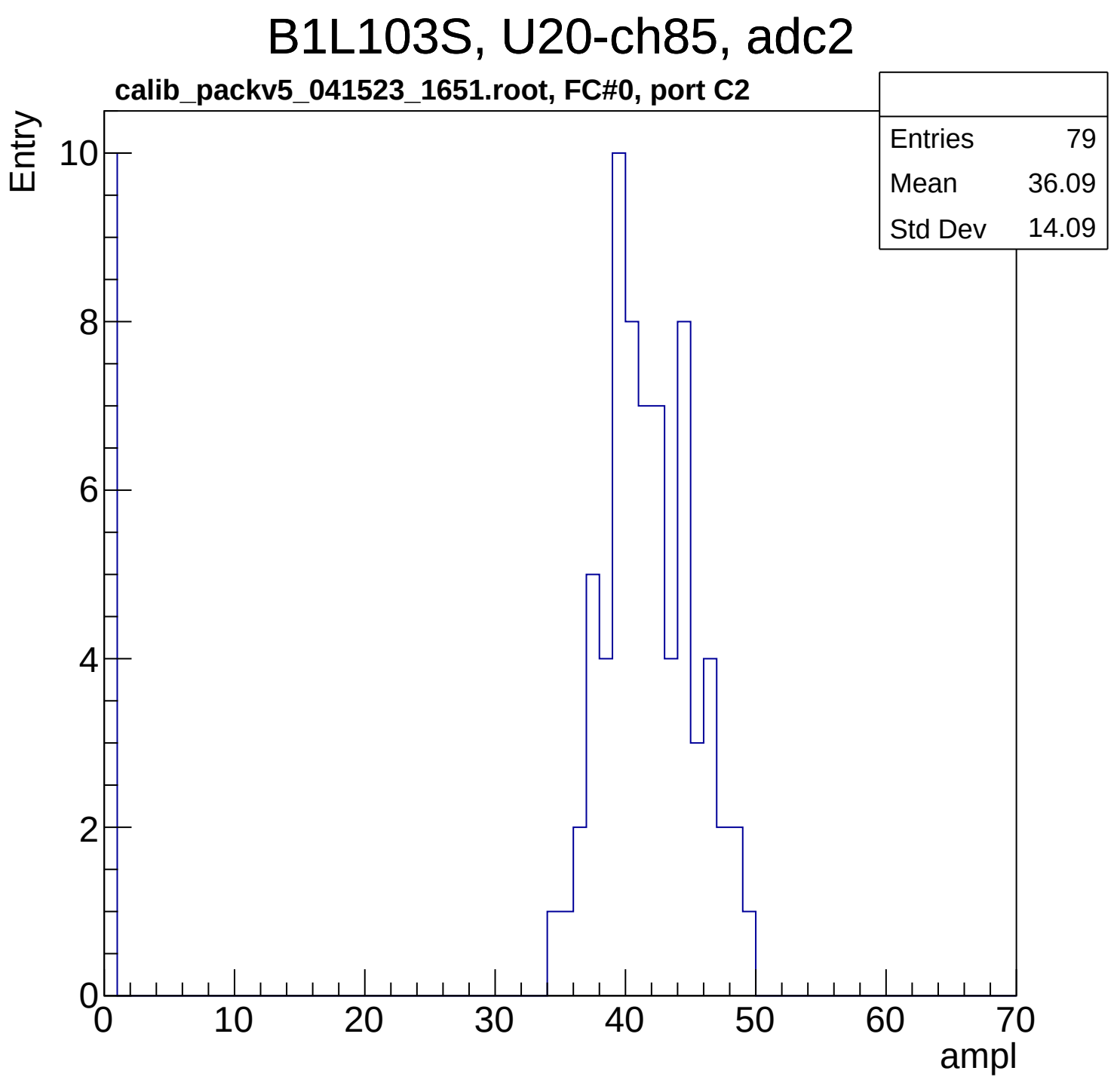
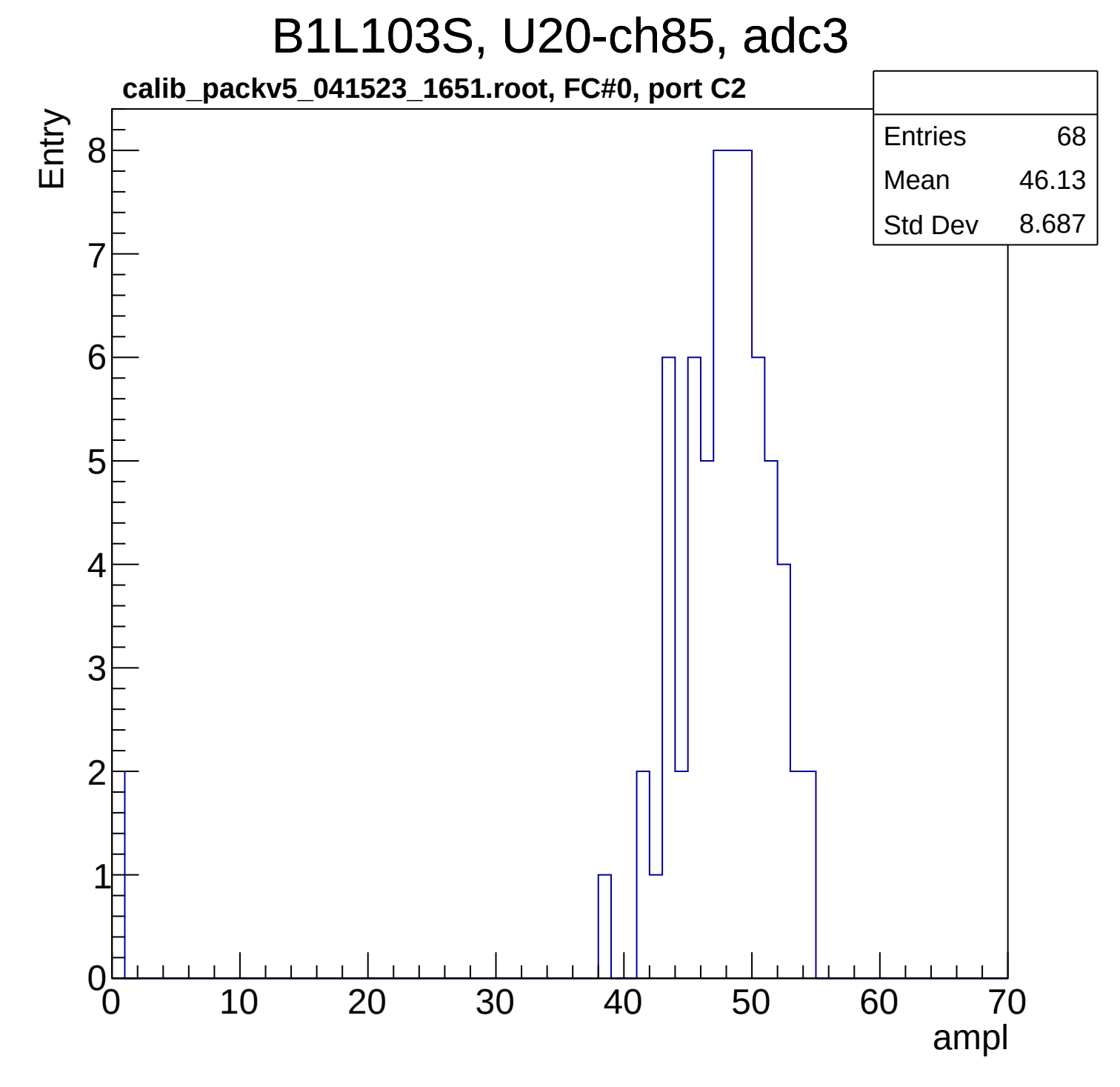
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch85, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 36.09
Std Dev 14.09
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch85, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 46.13
Std Dev 8.687
Entry
ampl
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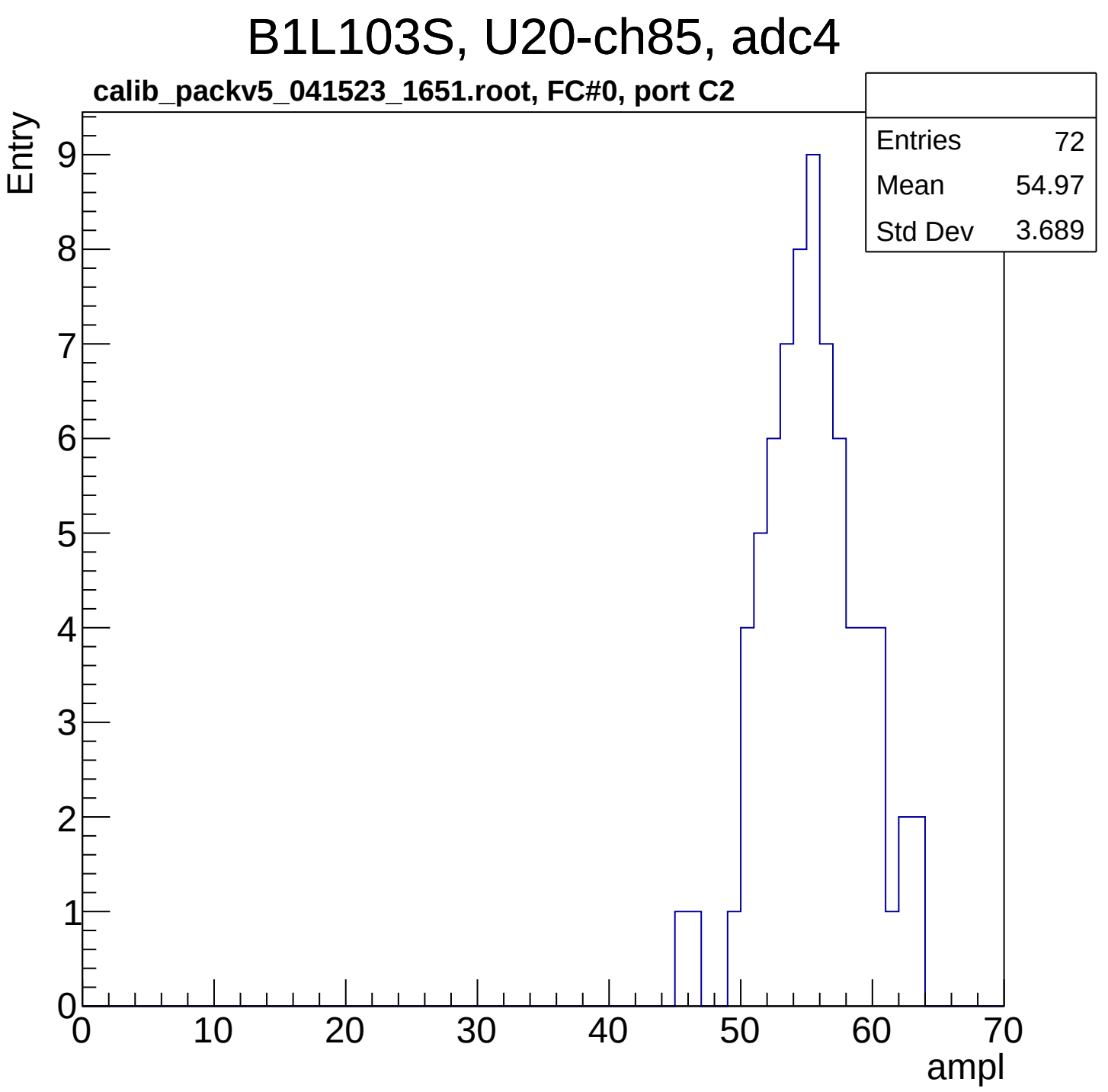
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch85, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 54.97
Std Dev 3.689
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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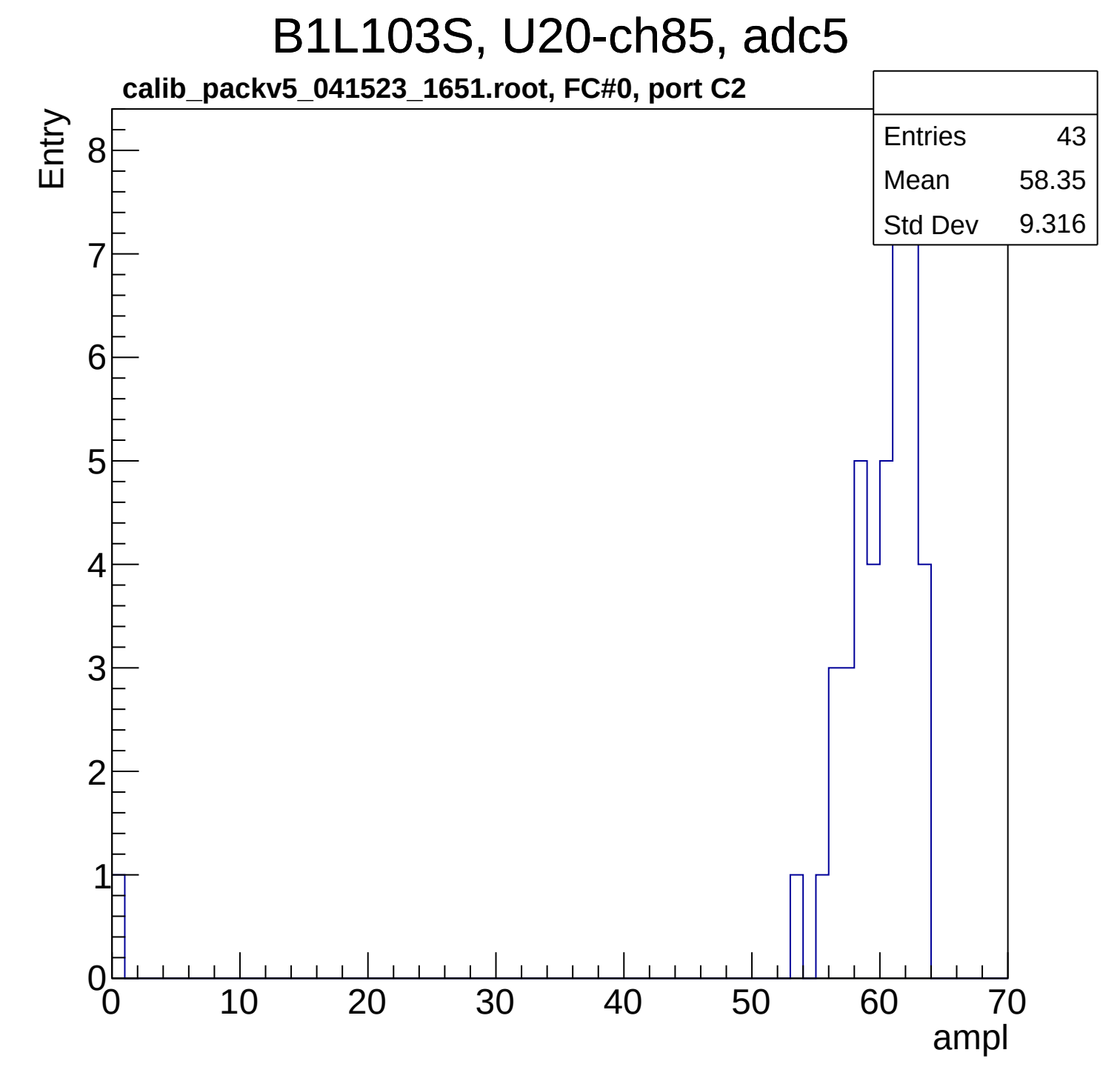
B1L103S, U20-ch85, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 58.35
Std Dev 9.316
Entry
ampl
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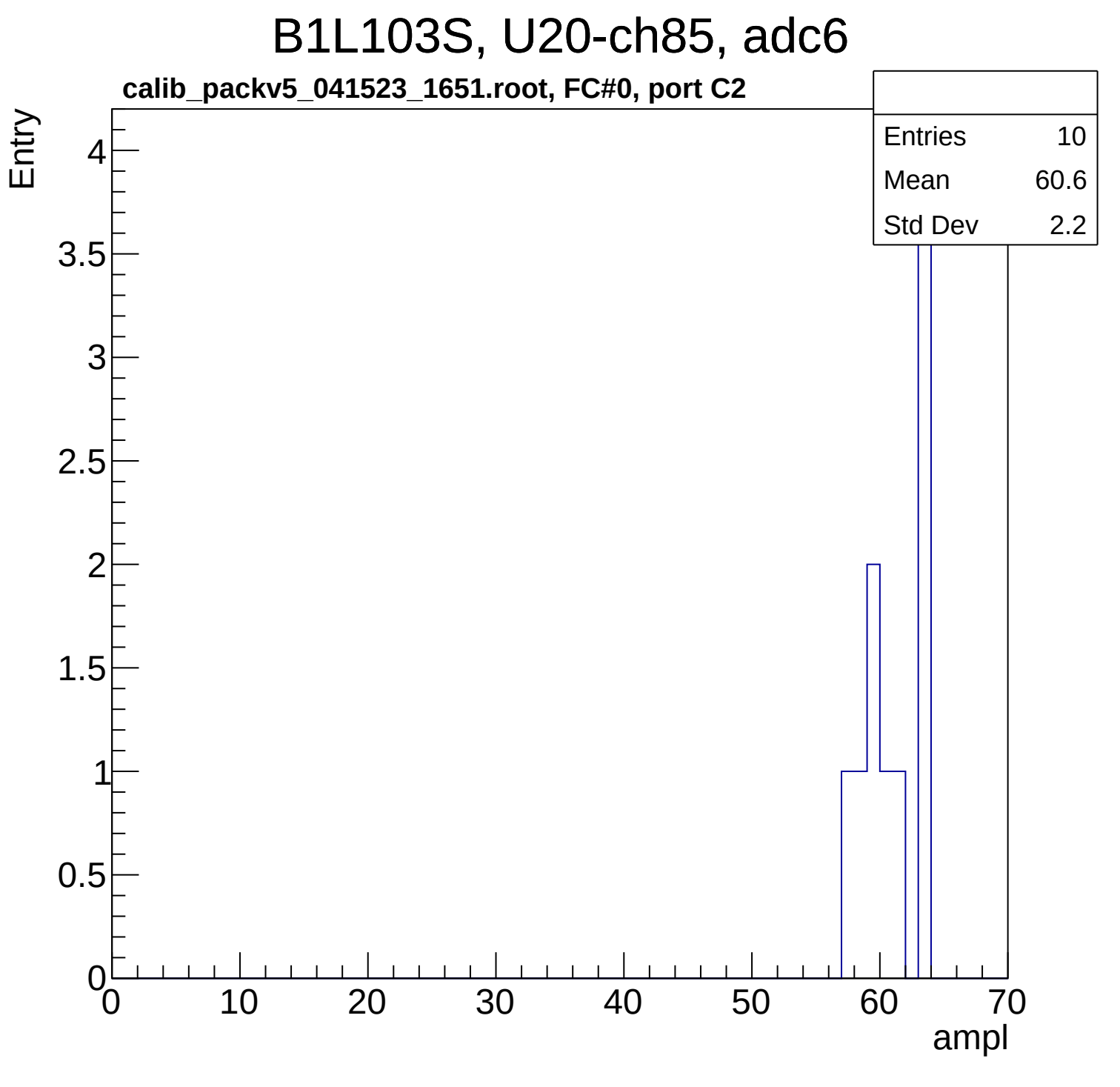
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch85, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 60.6
Std Dev 2.2
Entry
ampl
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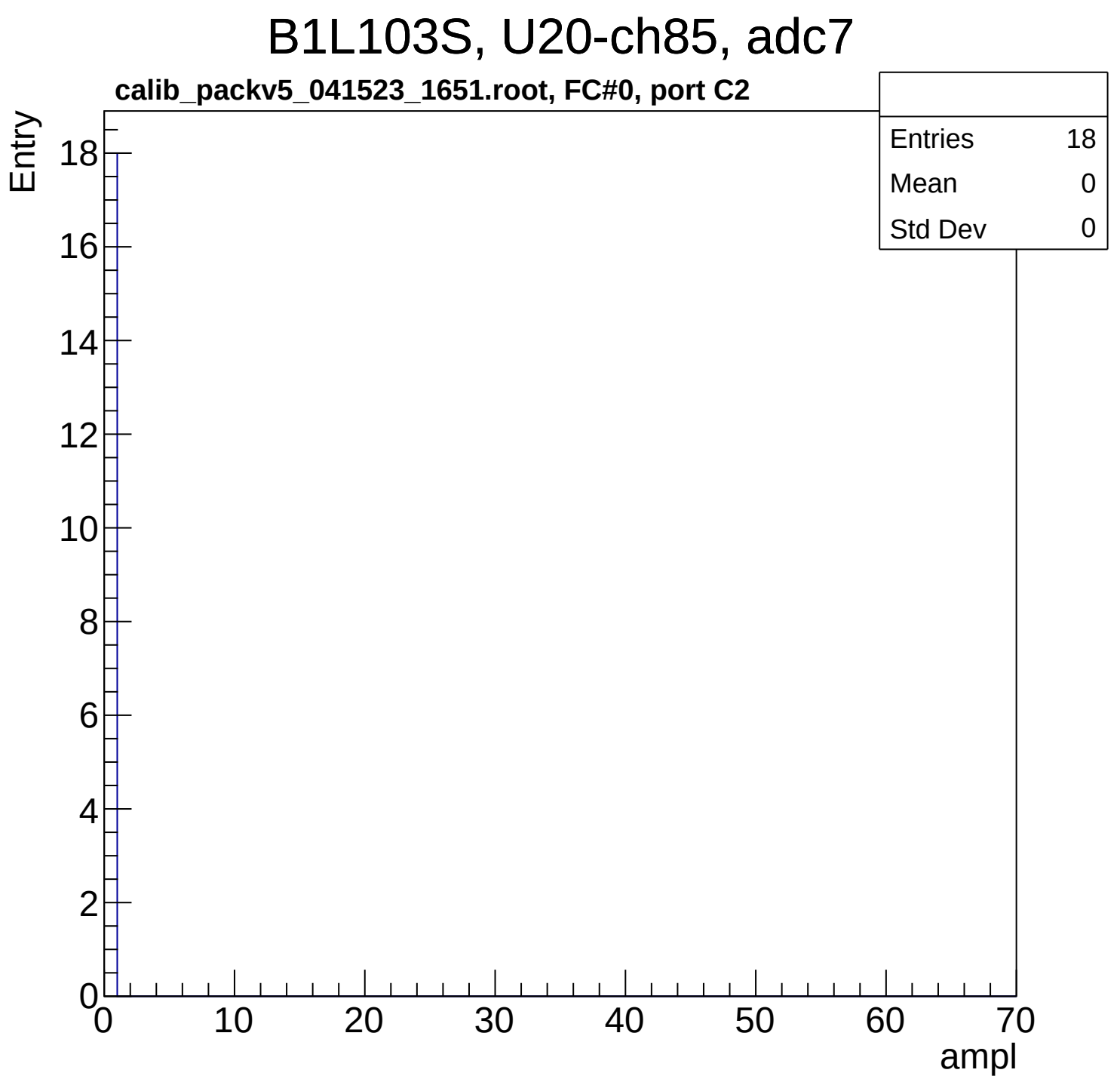
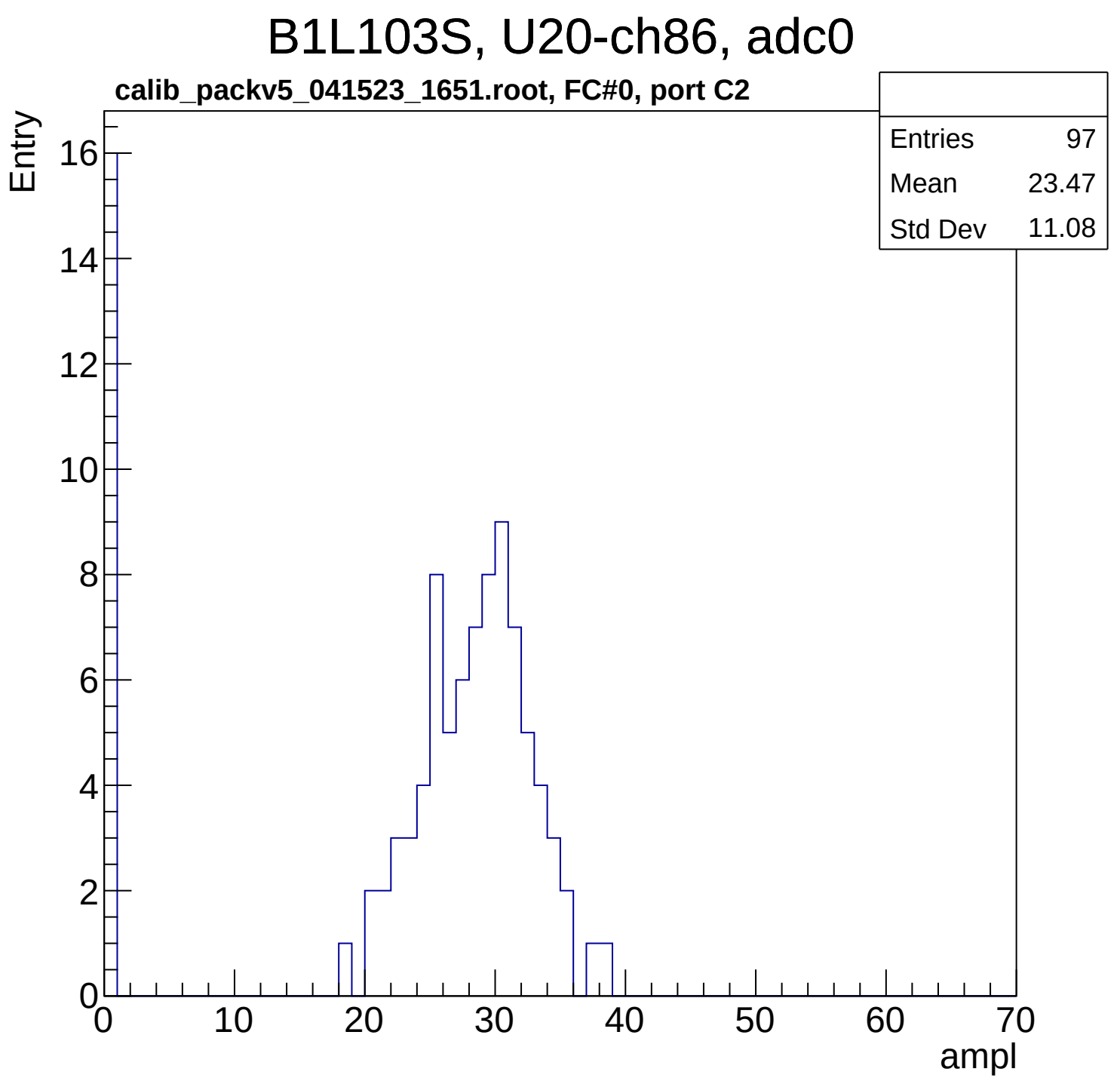
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U20-ch85, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch86, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 23.47
Std Dev 11.08
Entry
ampl
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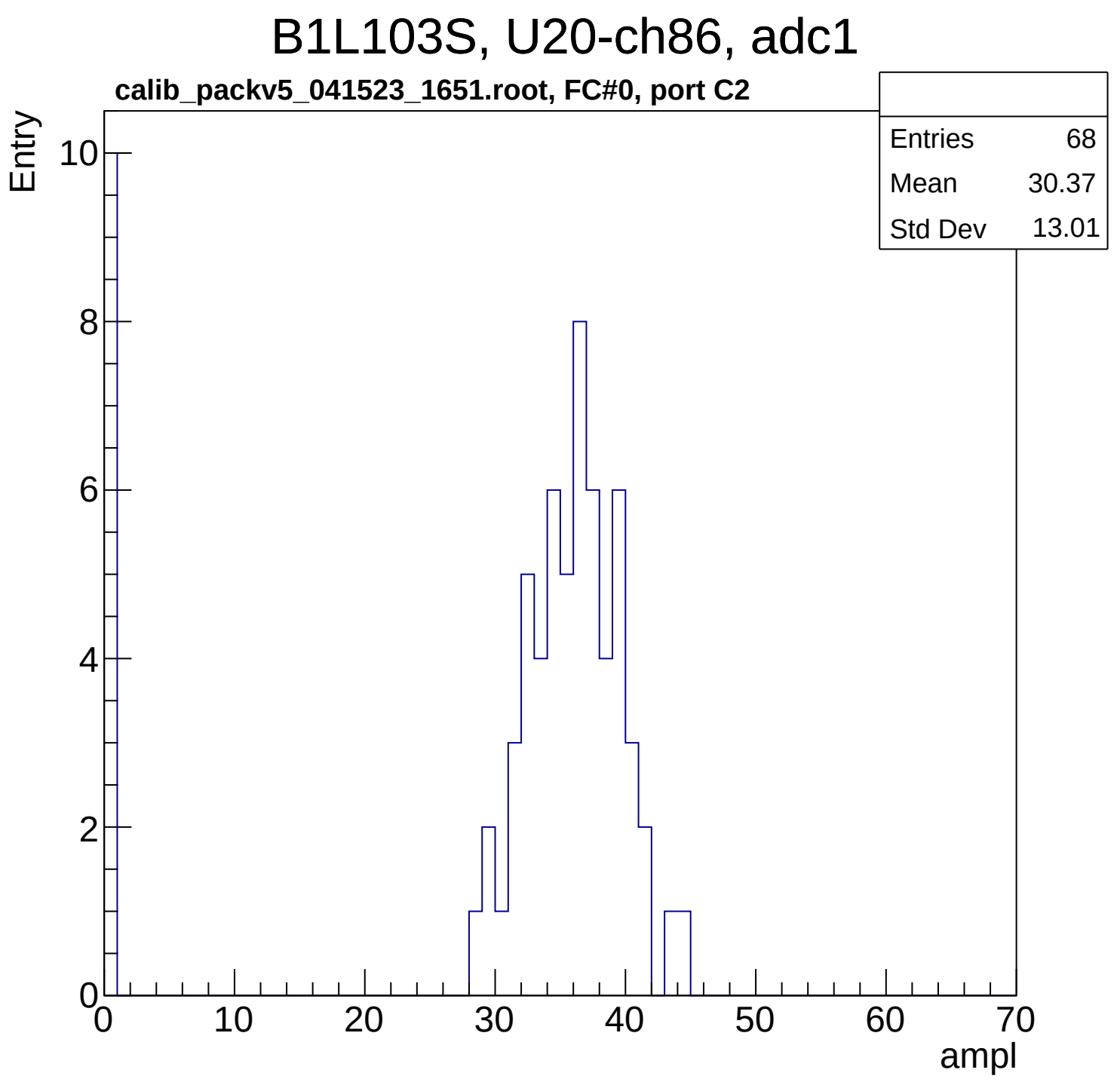
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L103S, U20-ch86, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 30.37
Std Dev 13.01
Entry
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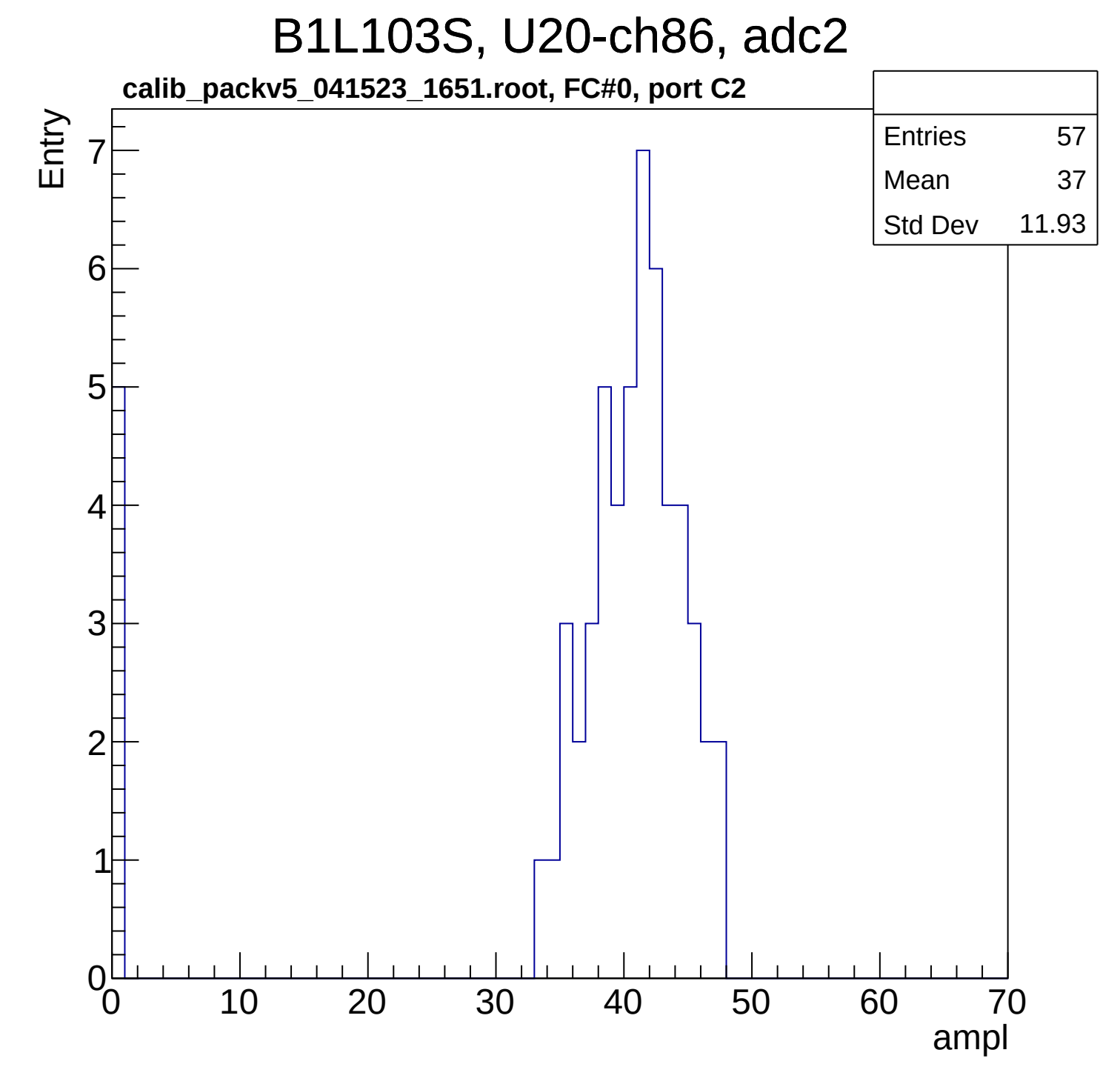
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch86, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 37
Std Dev 11.93
Entry
ampl
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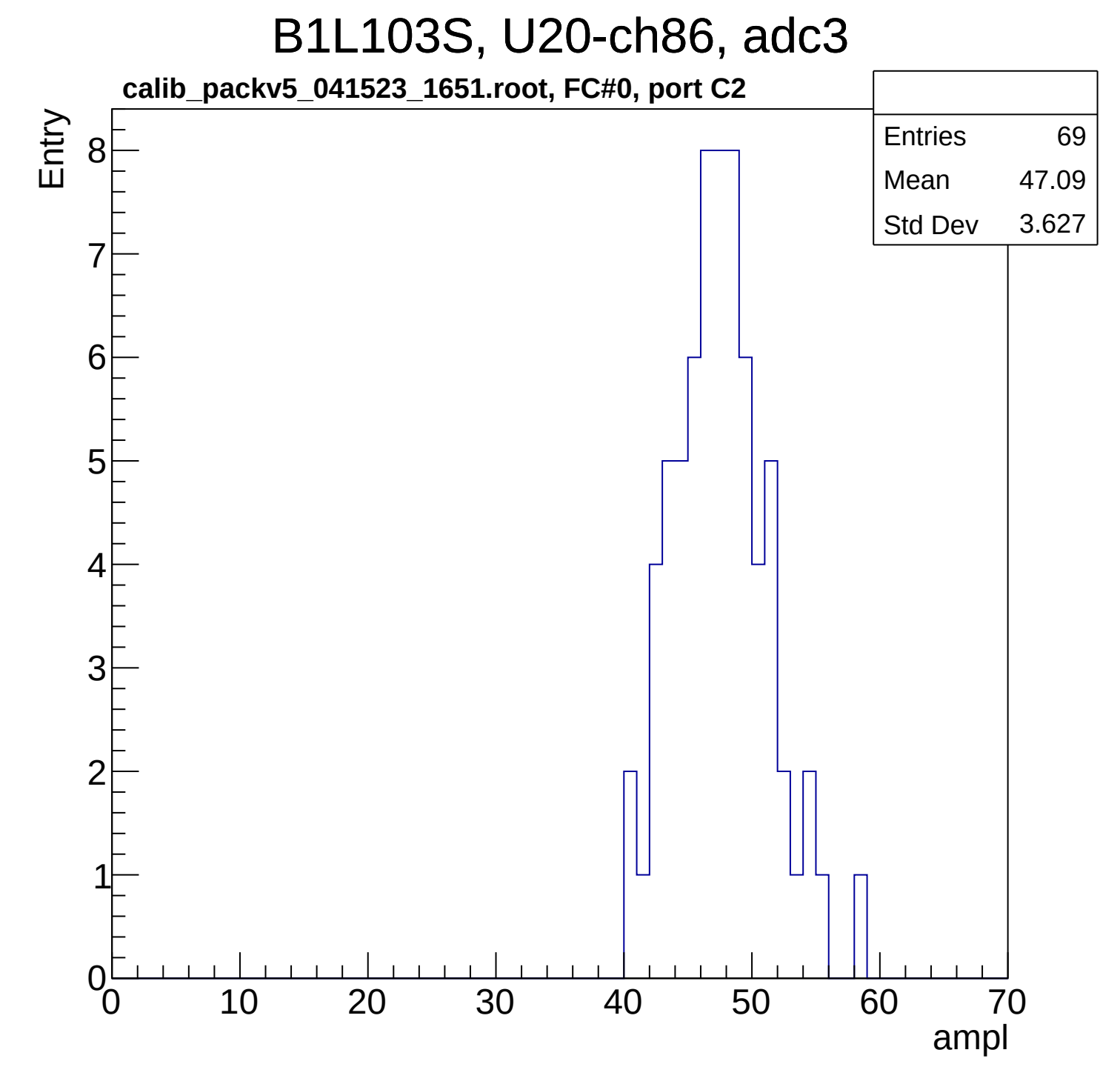
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U20-ch86, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 47.09
Std Dev 3.627
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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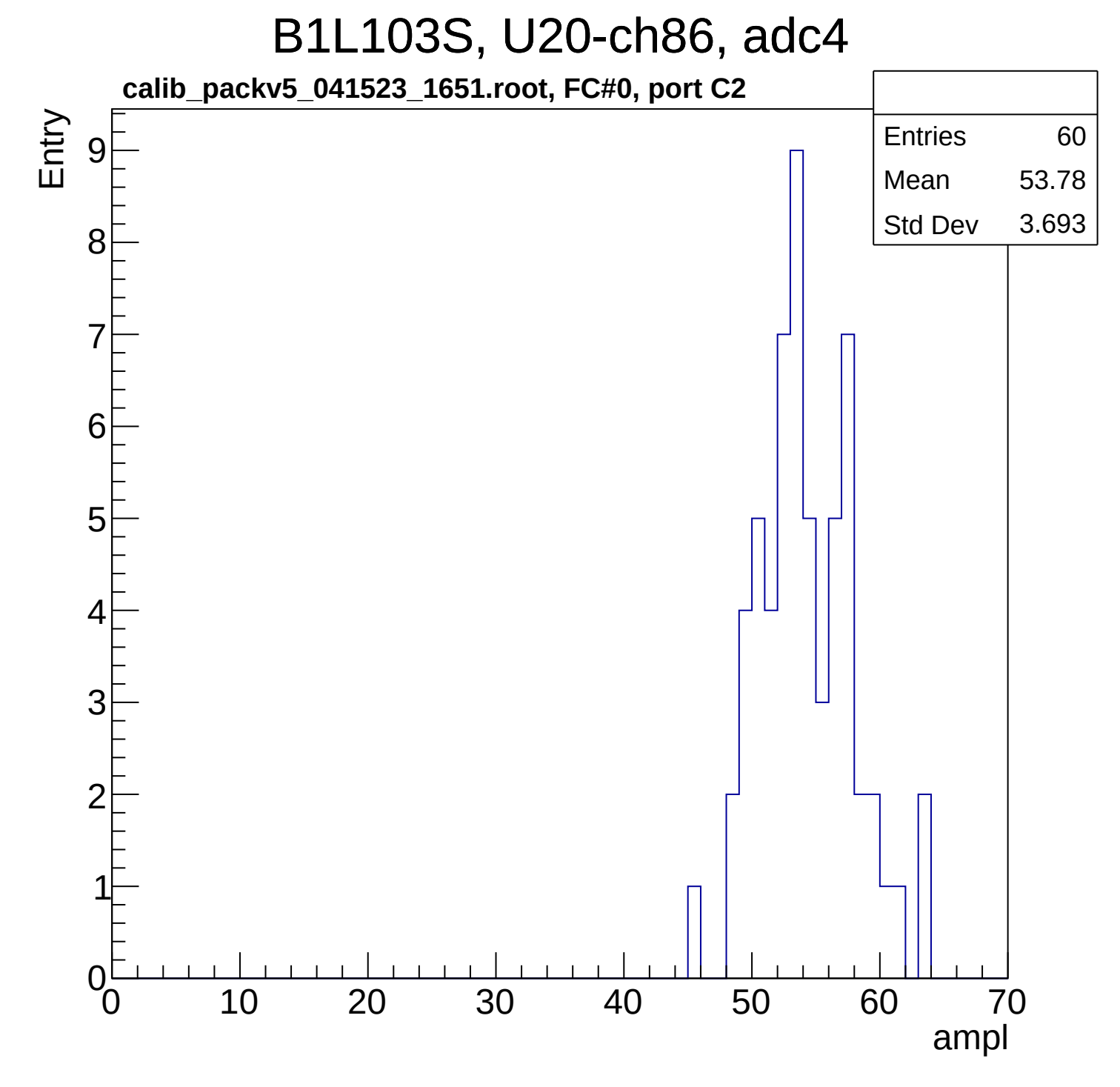
50
60
70


B1L103S, U20-ch86, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 53.78
Std Dev 3.693
Entry
ampl
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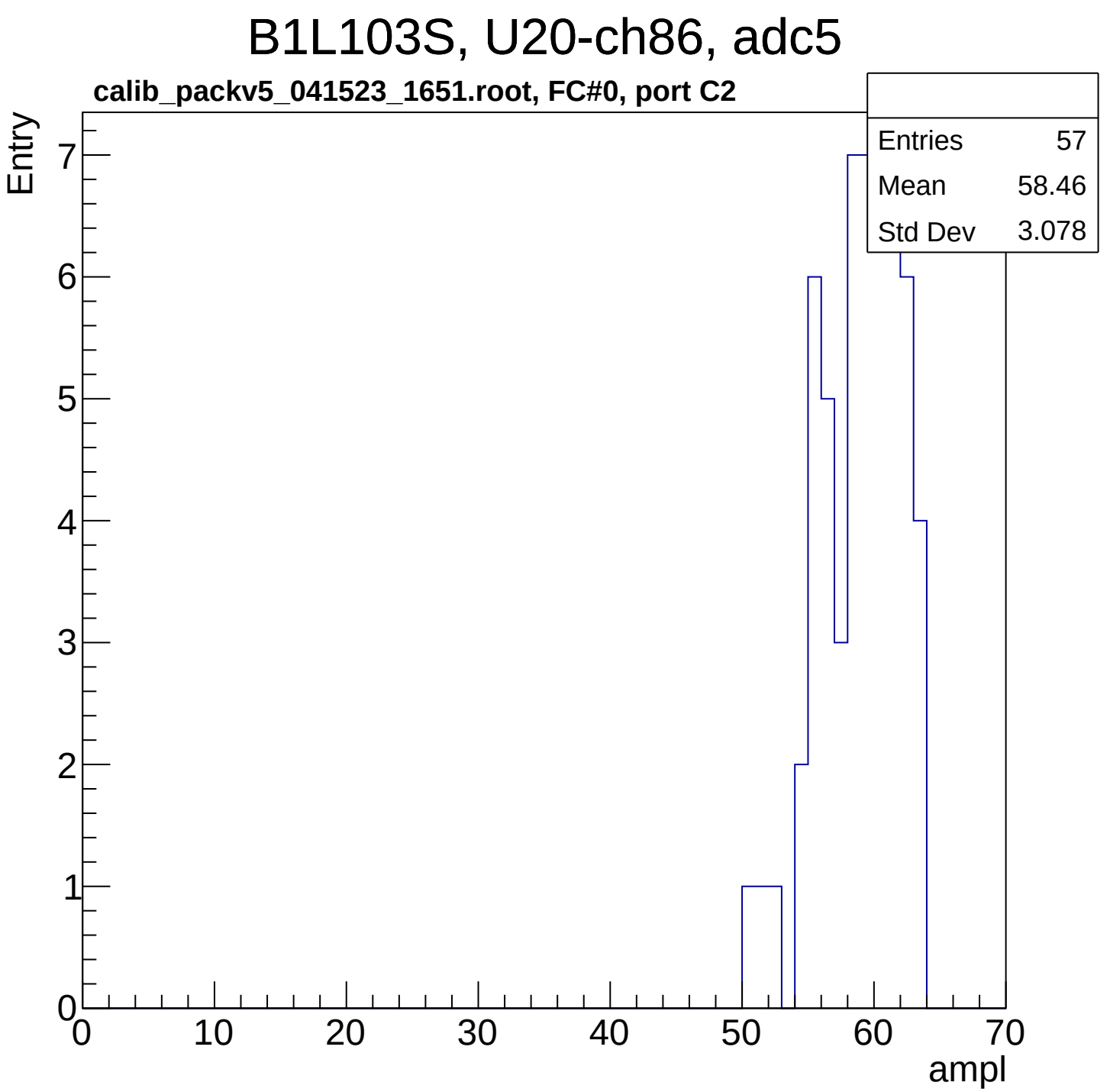
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch86, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 58.46
Std Dev 3.078
Entry
ampl
0
1
2
3
4
5
6
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0
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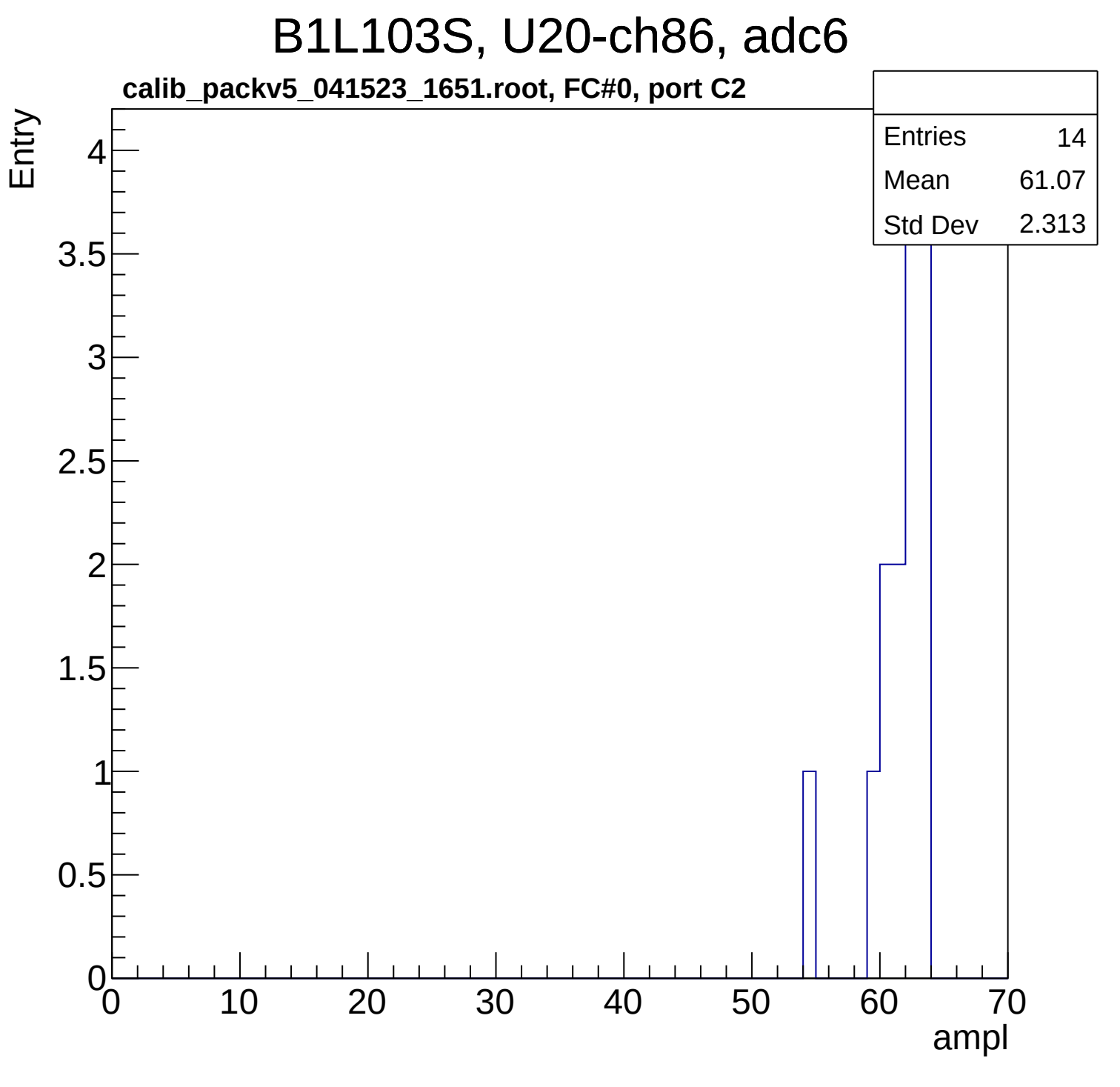
20
30
40
50
60
70


B1L103S, U20-ch86, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 61.07
Std Dev 2.313
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
10
20
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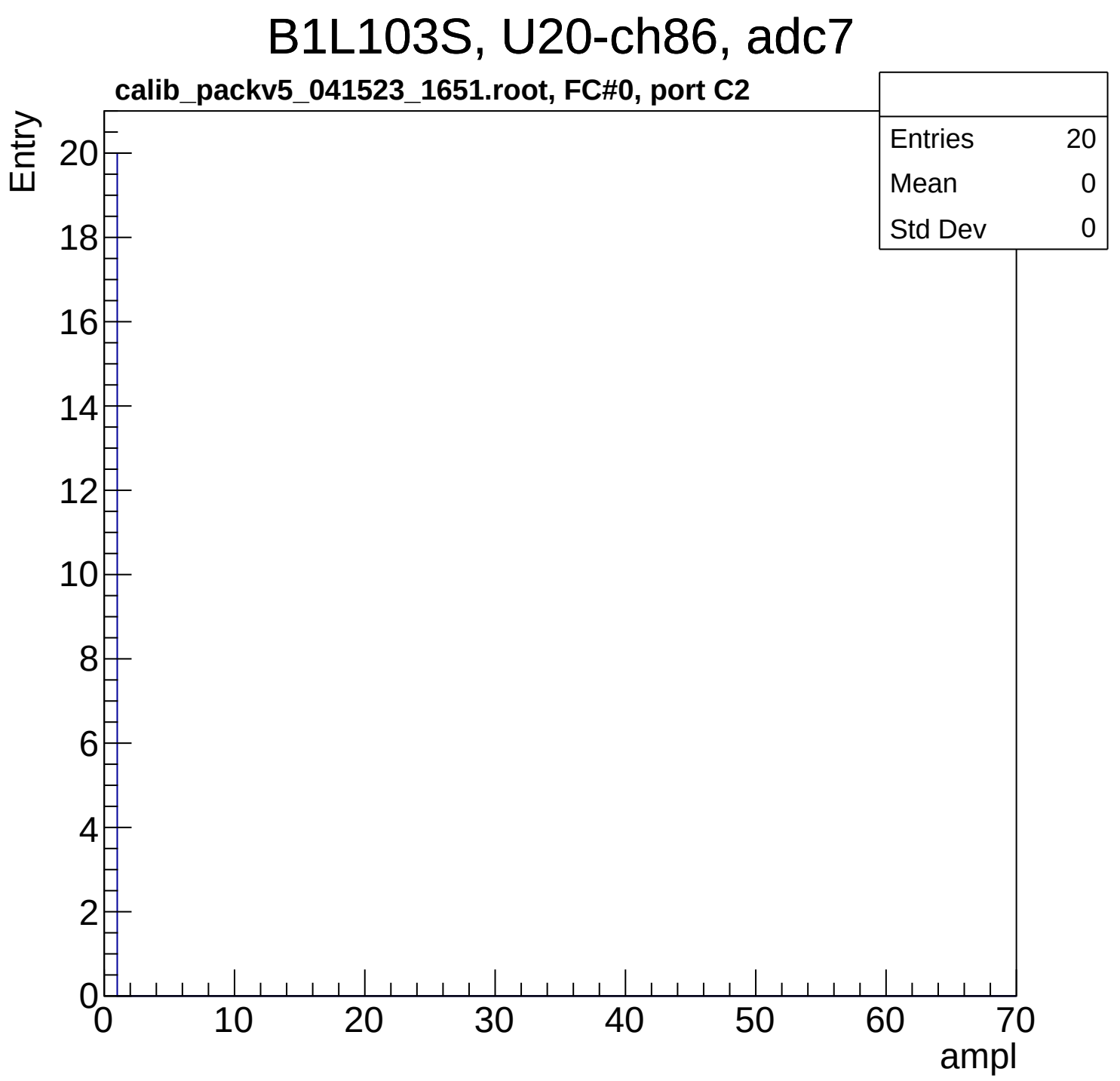
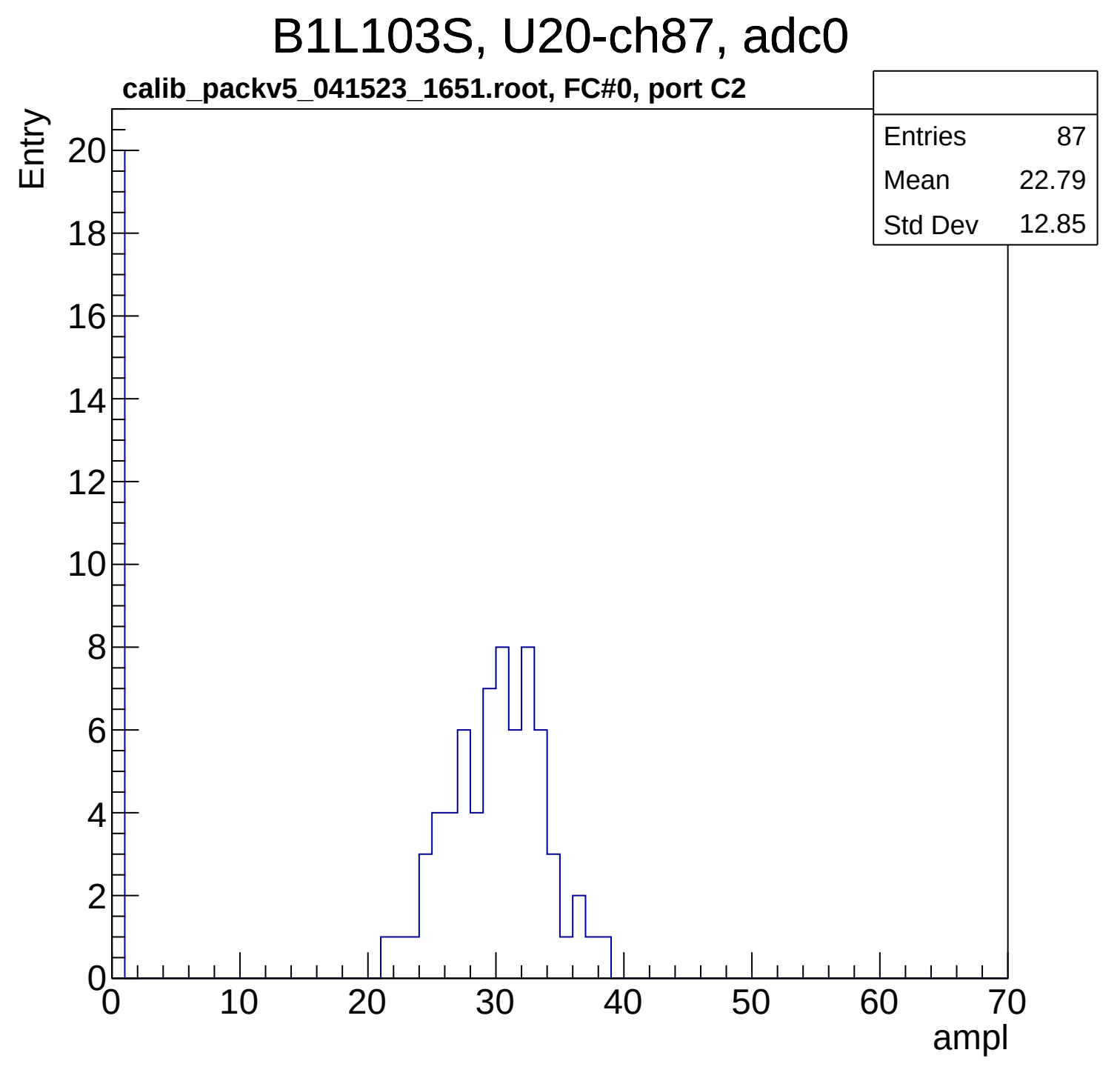
50
60
70


B1L103S, U20-ch86, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch87, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 22.79
Std Dev 12.85
Entry
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8
10
12
14
16
18
20
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10
20
30
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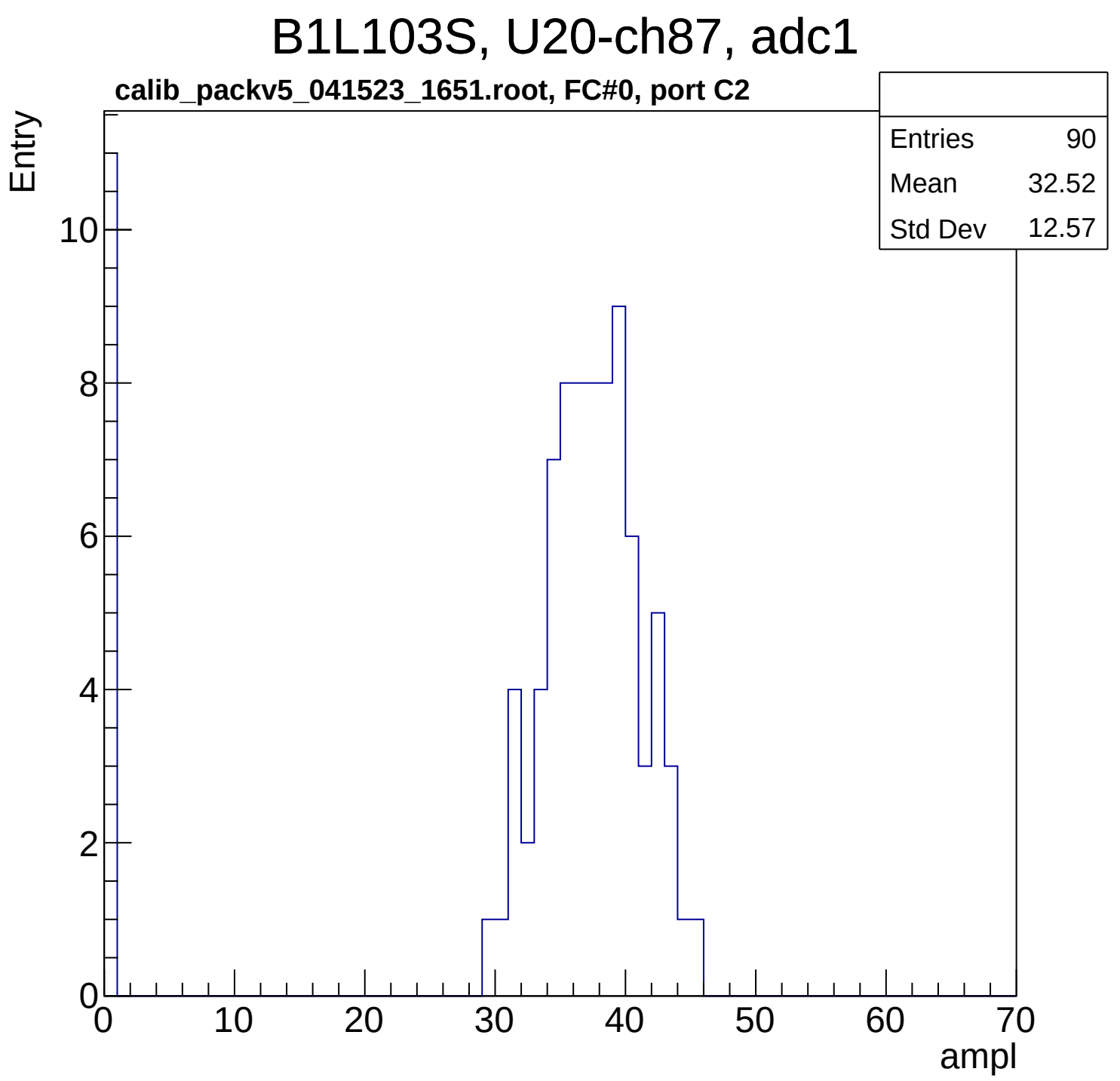
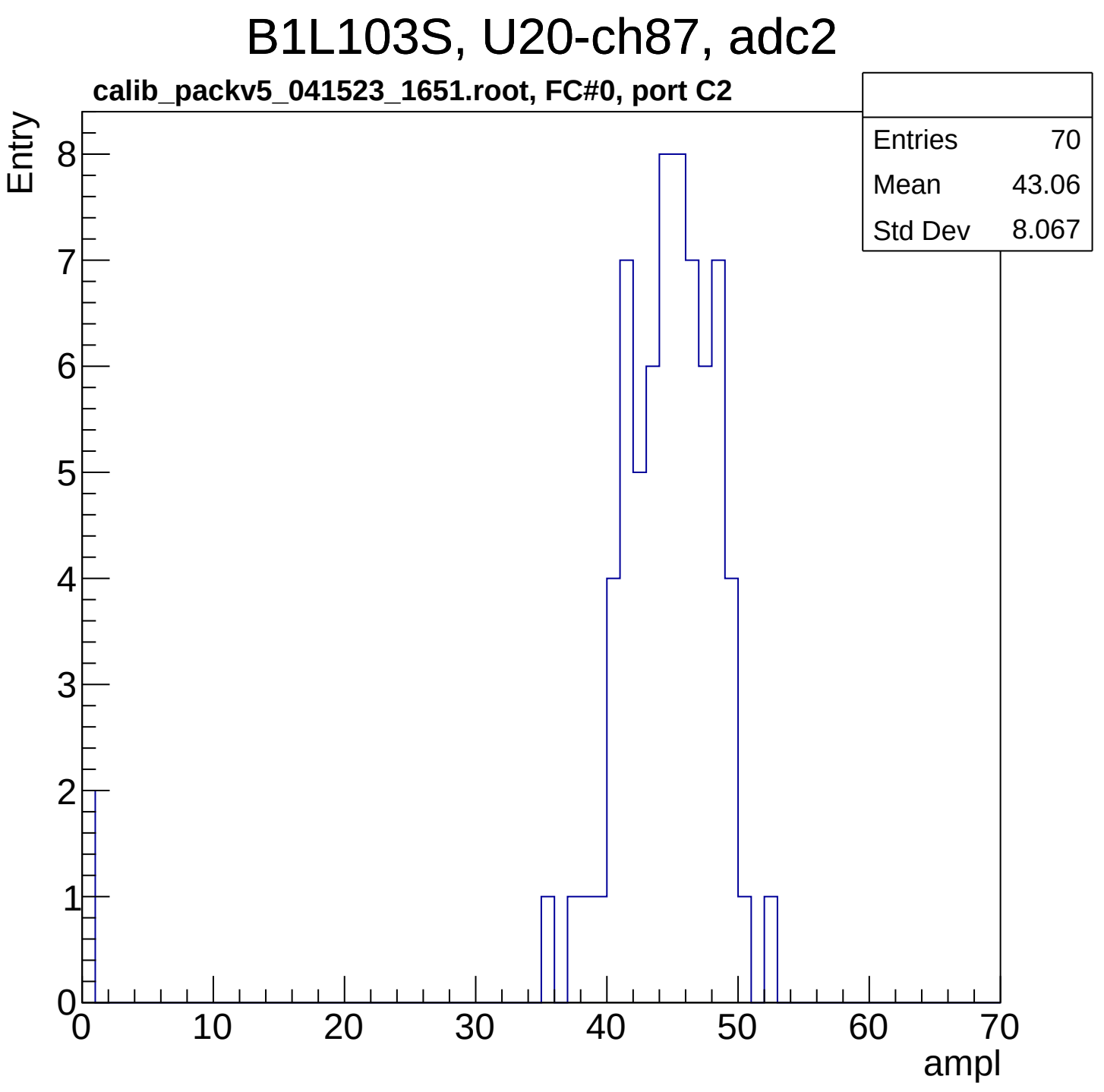
50
60
70
ampl


B1L103S, U20-ch87, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 32.52
Std Dev 12.57
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch87, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 43.06
Std Dev 8.067
Entry
ampl
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2
3
4
5
6
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8
0
10
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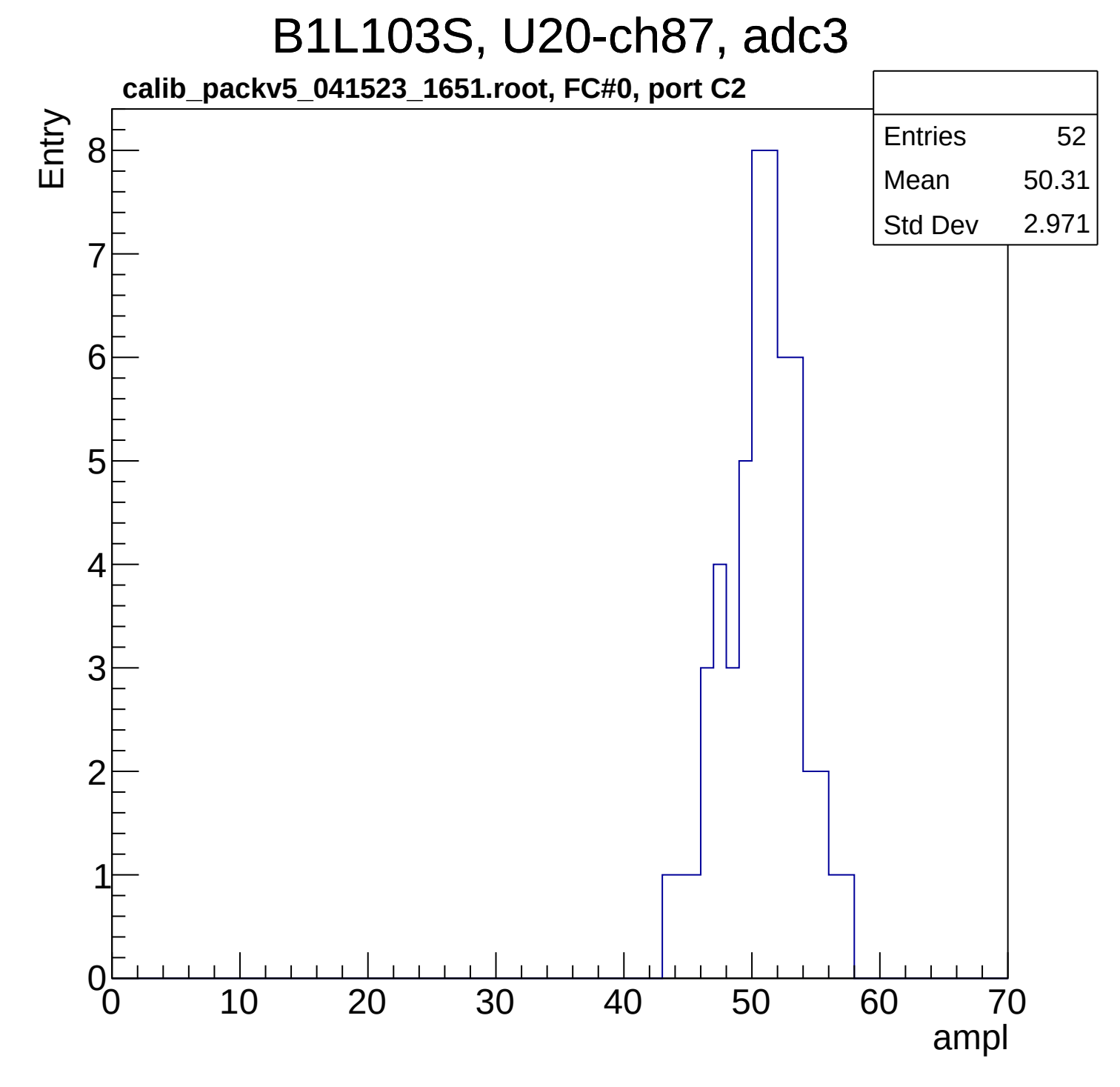
30
40
50
60
70


B1L103S, U20-ch87, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 50.31
Std Dev 2.971
Entry
ampl
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5
6
7
8
0
10
20
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40
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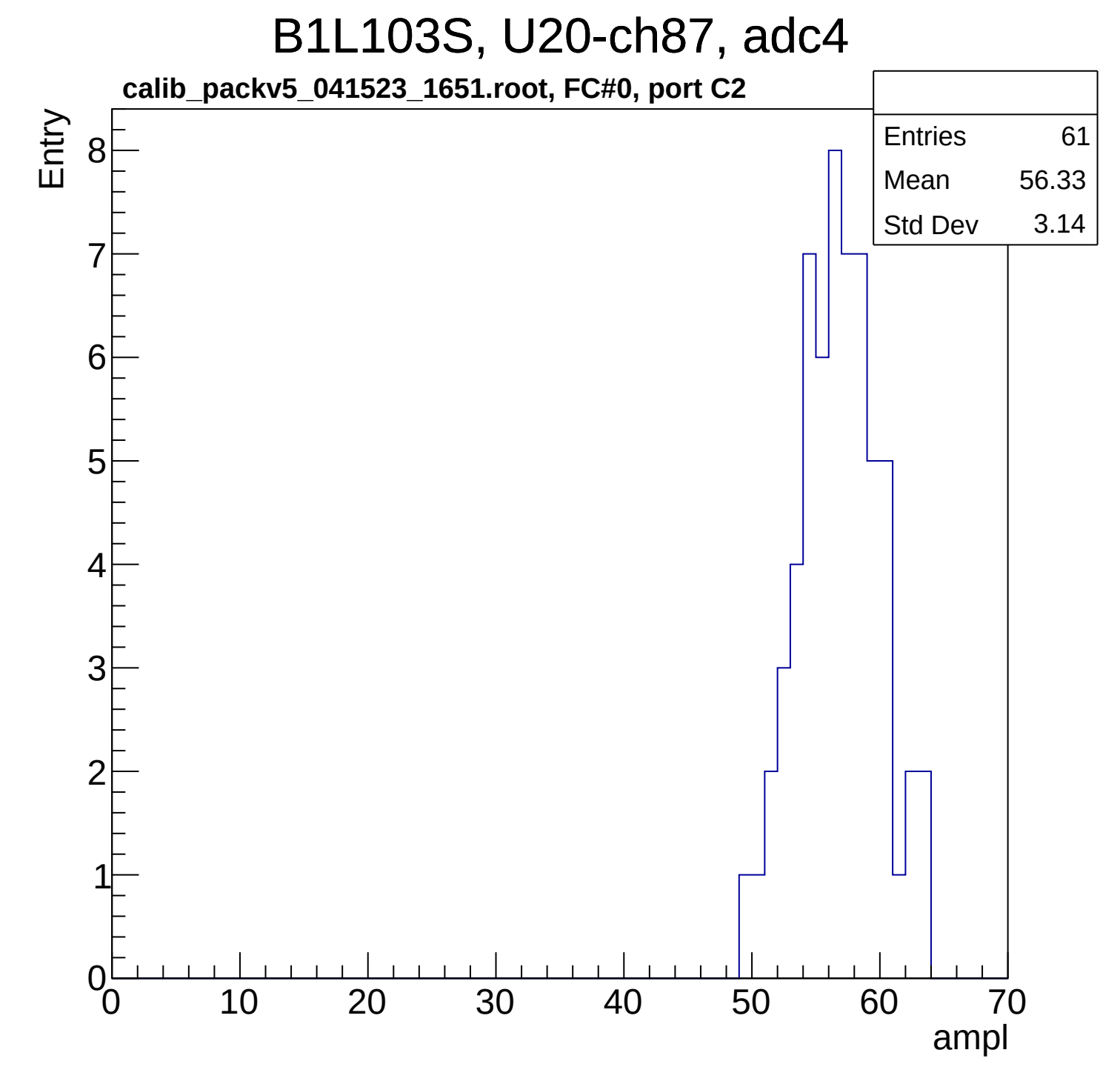
60
70


B1L103S, U20-ch87, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 56.33
Std Dev 3.14
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
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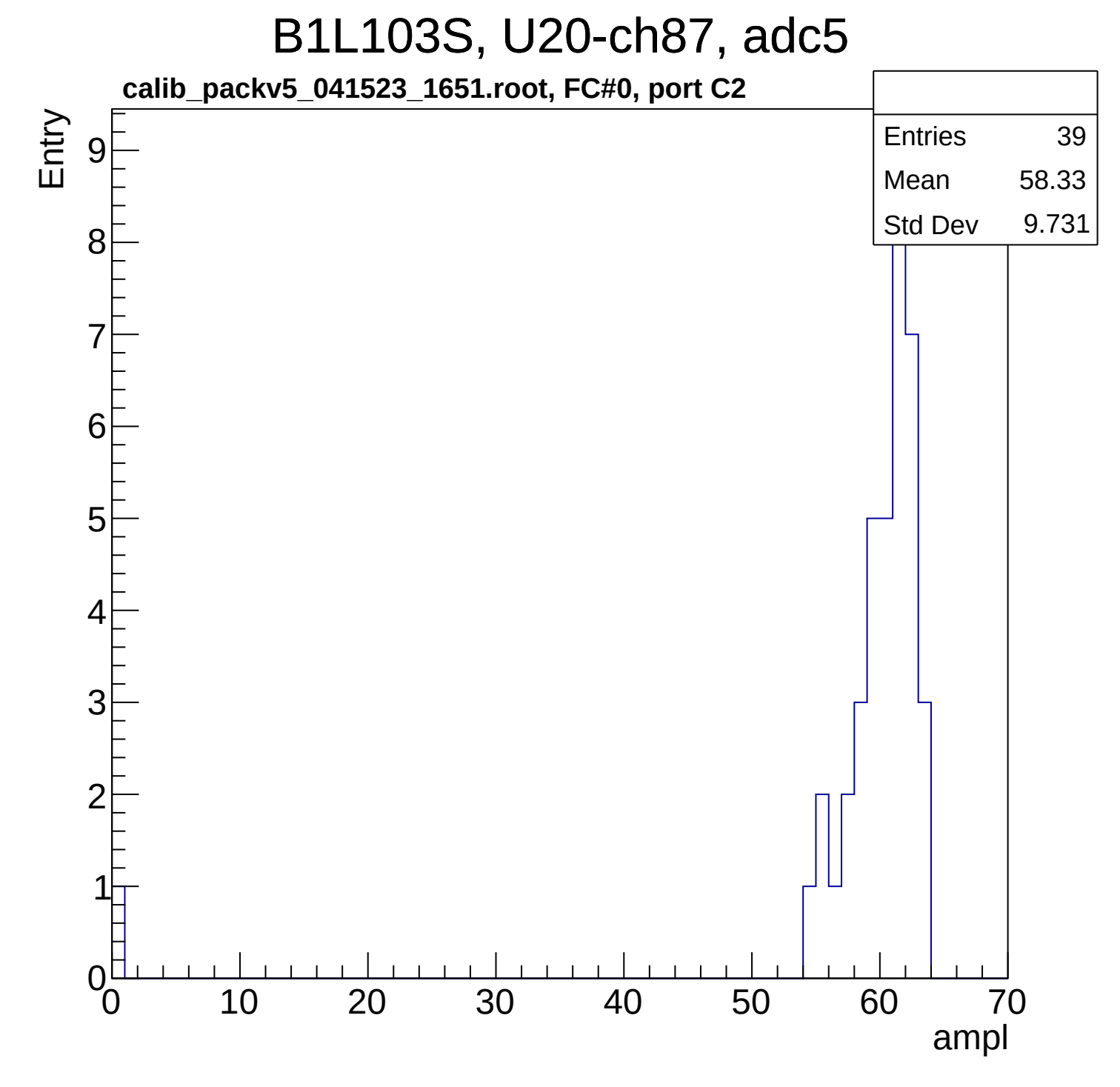
B1L103S, U20-ch87, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 58.33
Std Dev 9.731
Entry
ampl
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3
4
5
6
7
8
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0
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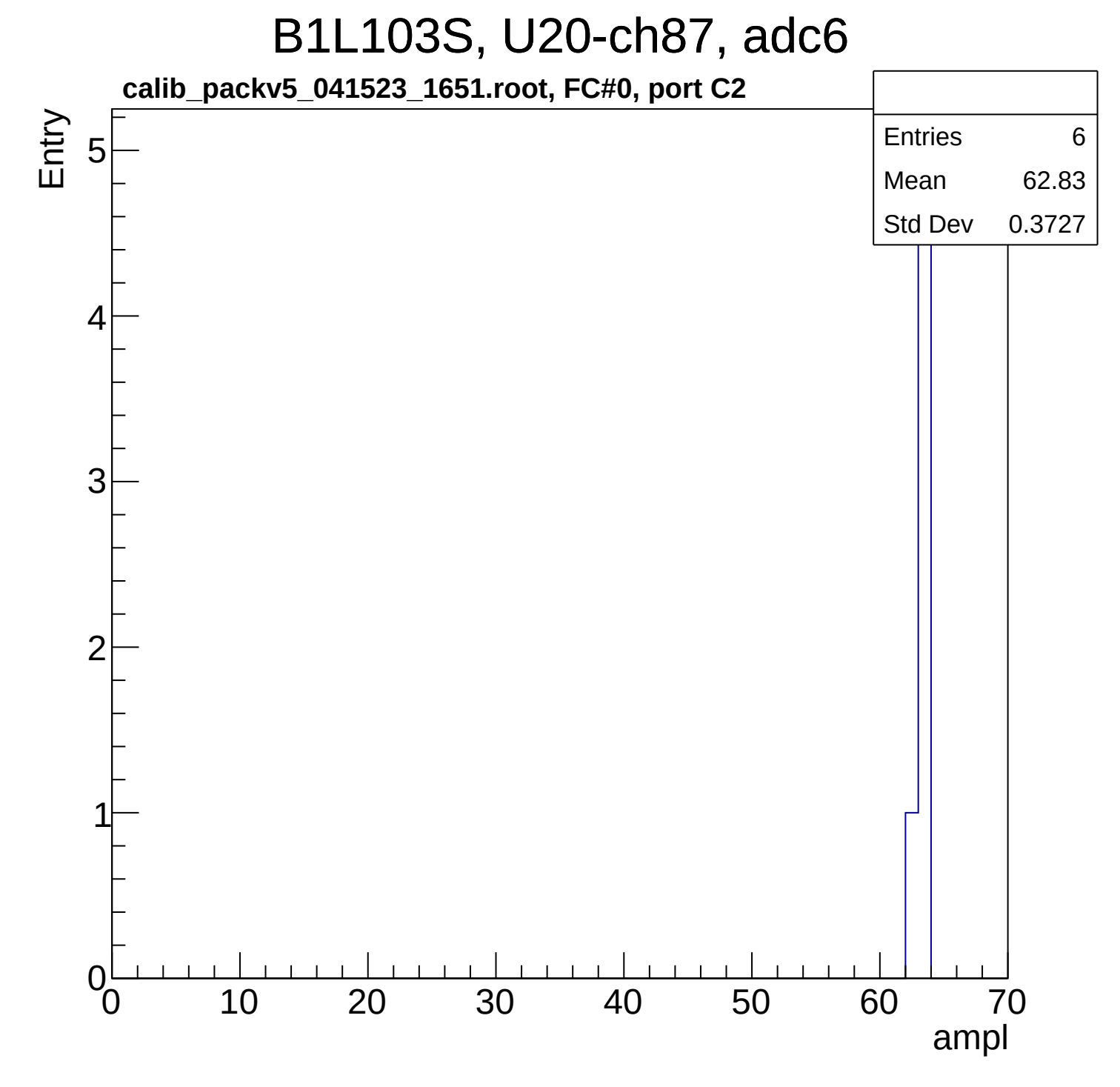
B1L103S, U20-ch87, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 62.83
Std Dev 0.3727
Entry
ampl
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2
3
4
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0
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20
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40
50
60
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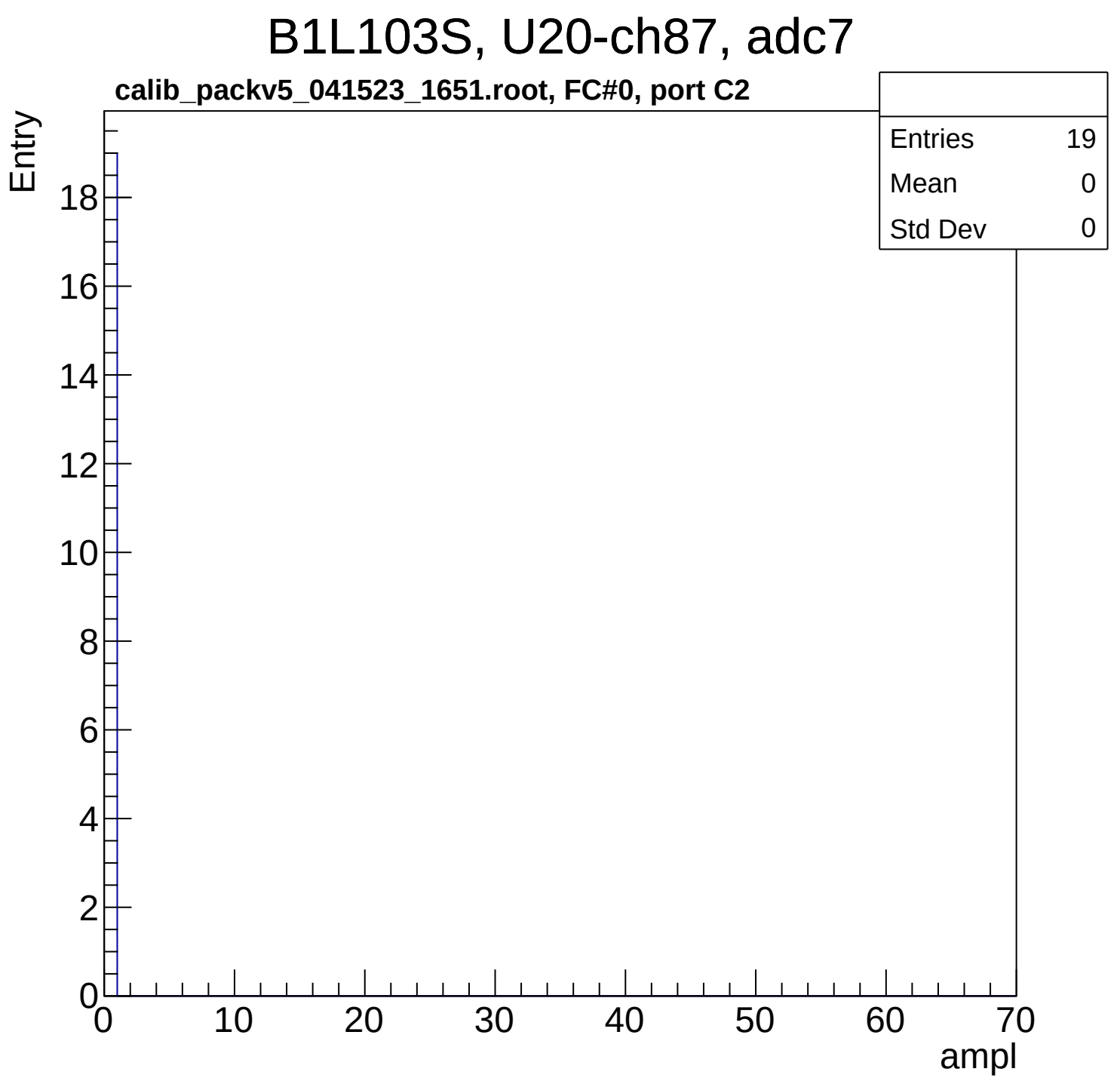
B1L103S, U20-ch87, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
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6
8
10
12
14
16
18
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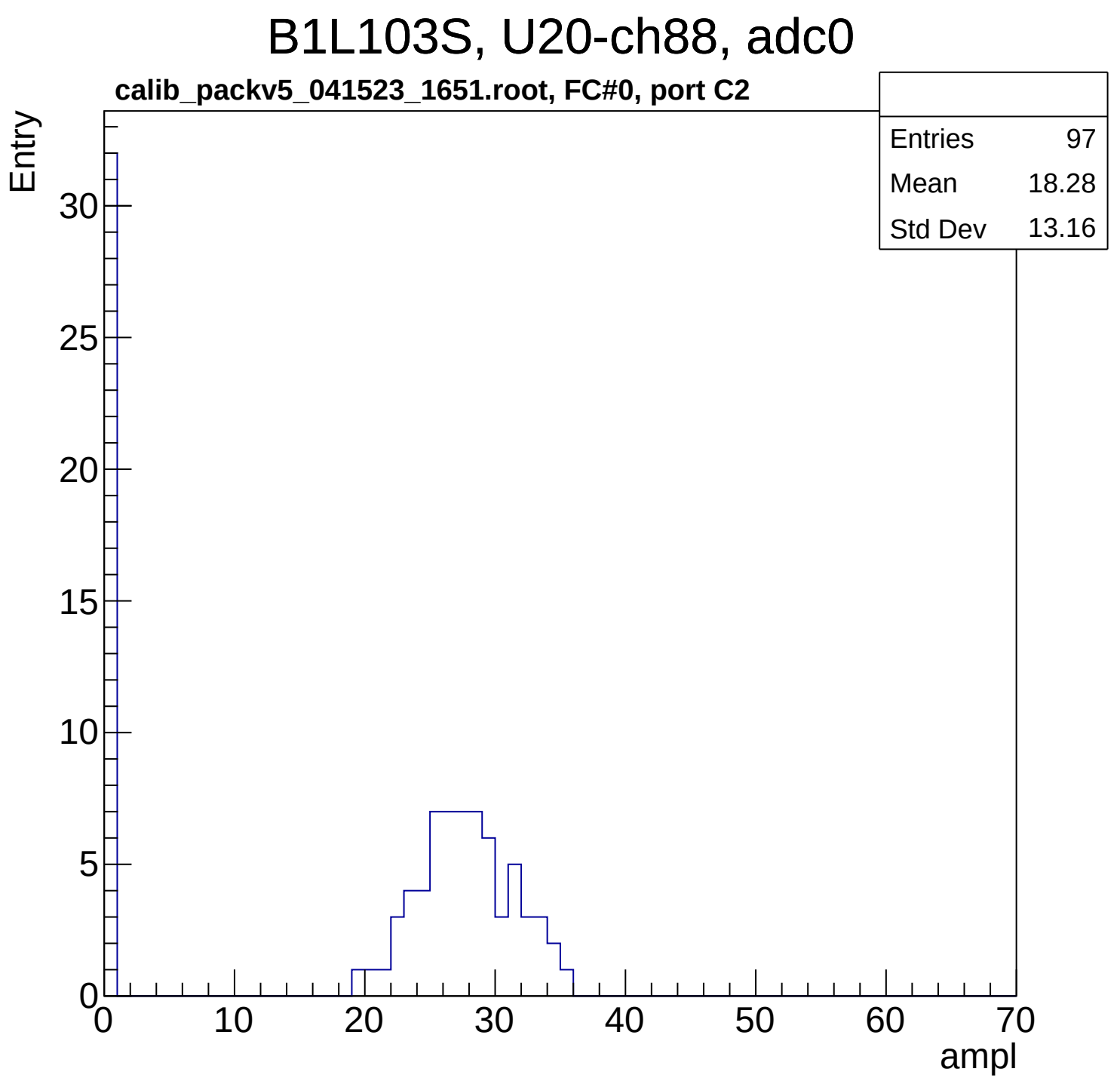
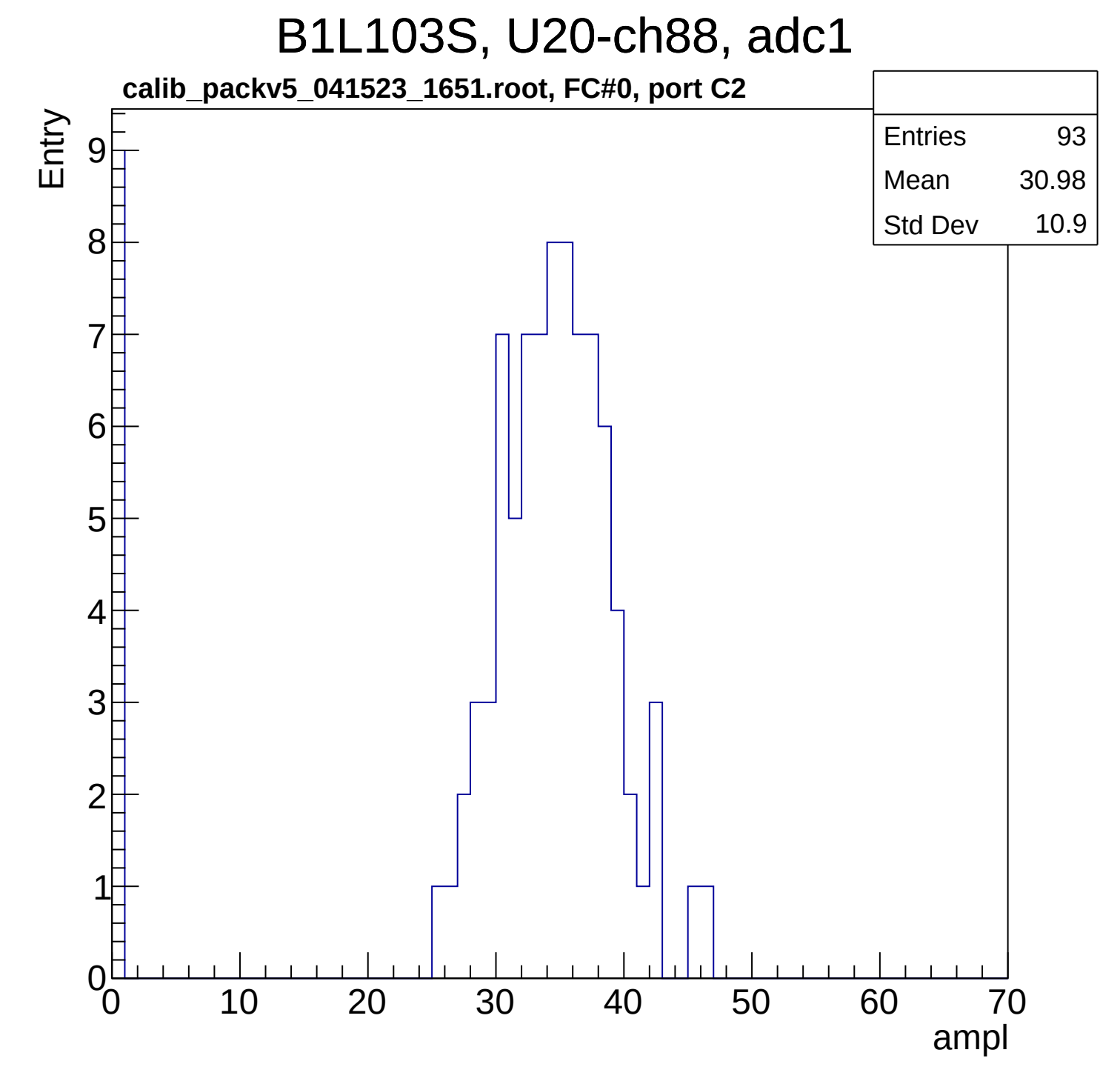
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch88, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 18.28
Std Dev 13.16
Entry
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch88, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 30.98
Std Dev 10.9
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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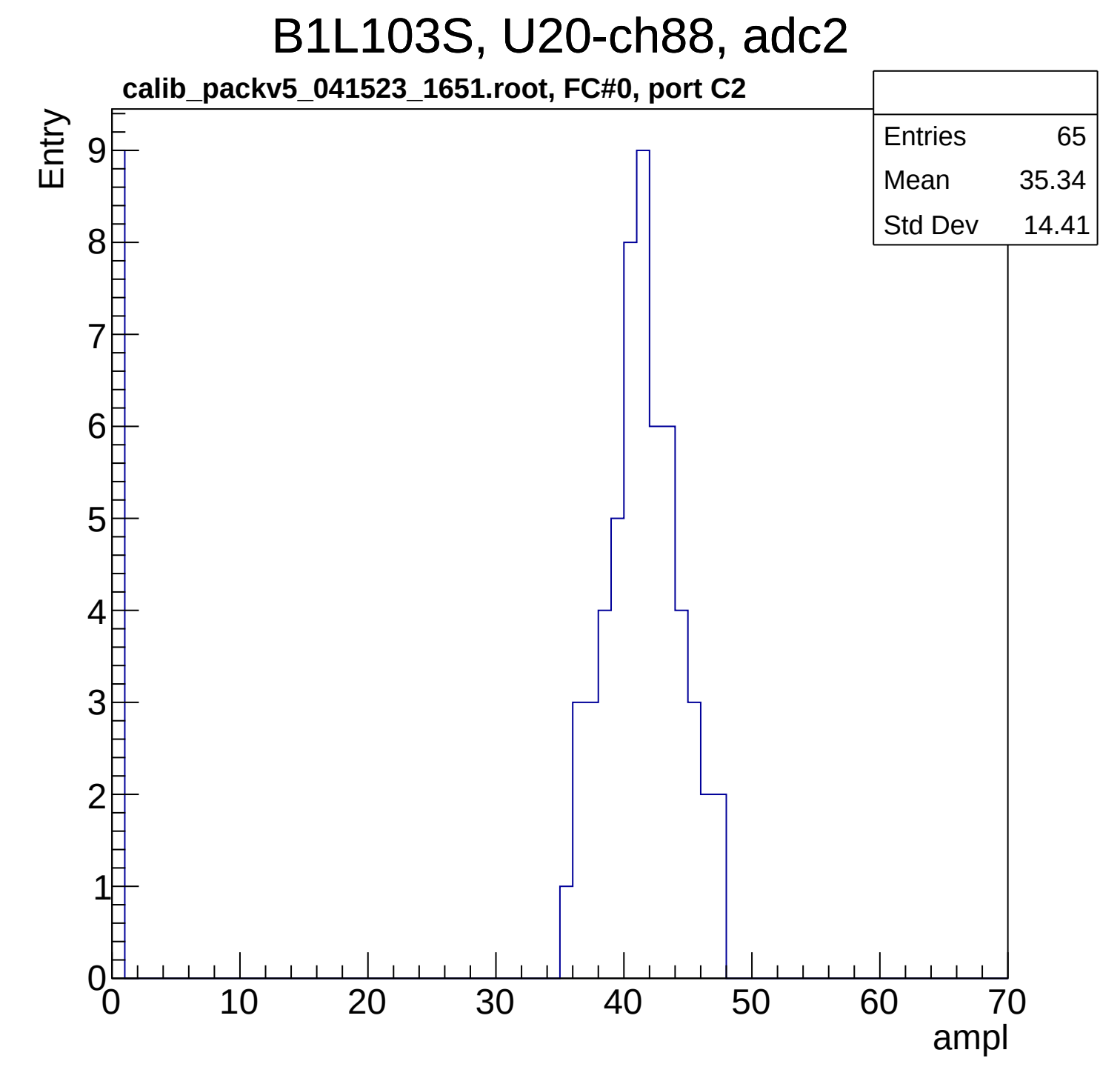
B1L103S, U20-ch88, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 35.34
Std Dev 14.41
Entry
ampl
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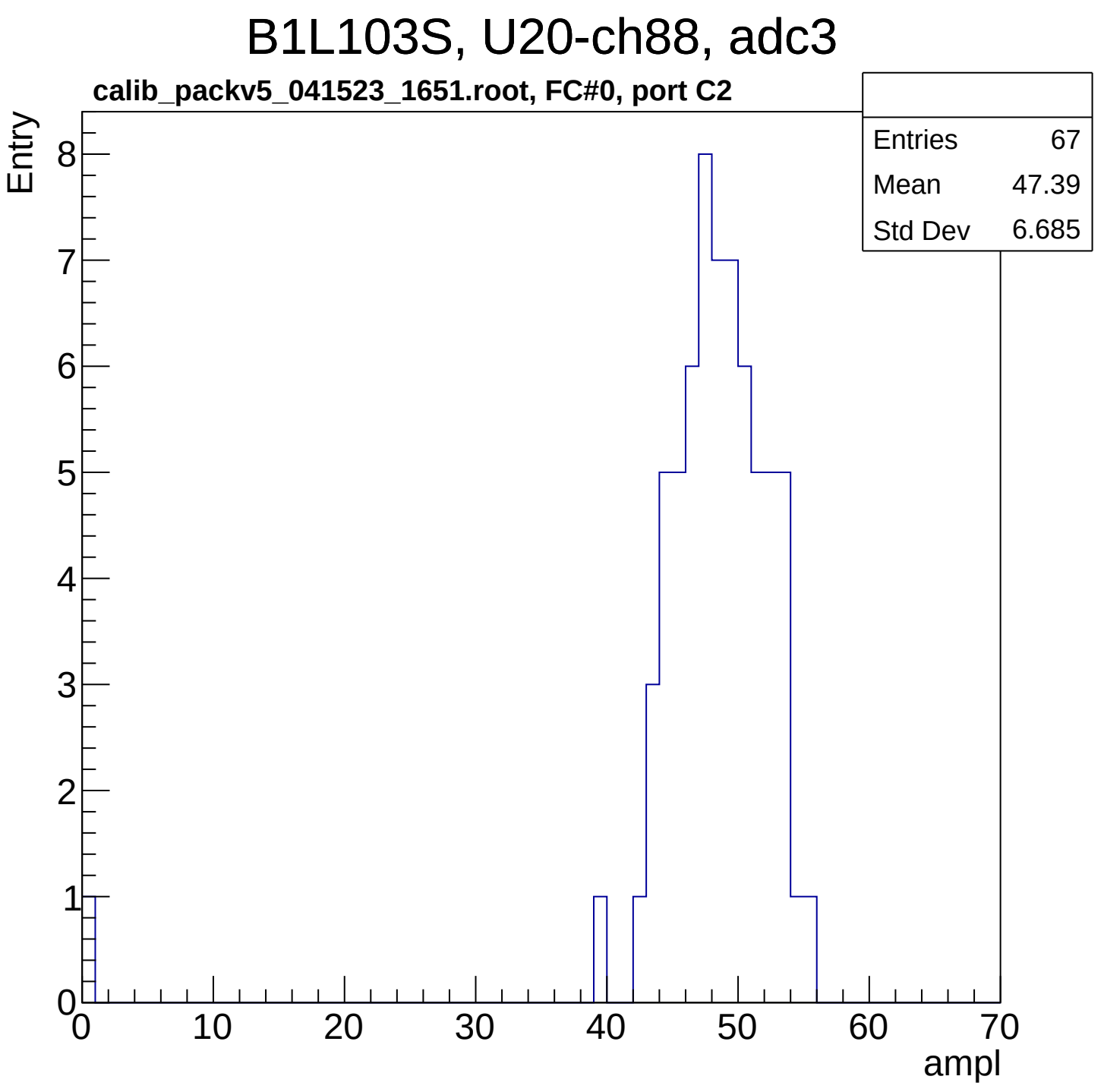
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch88, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 47.39
Std Dev 6.685
Entry
ampl
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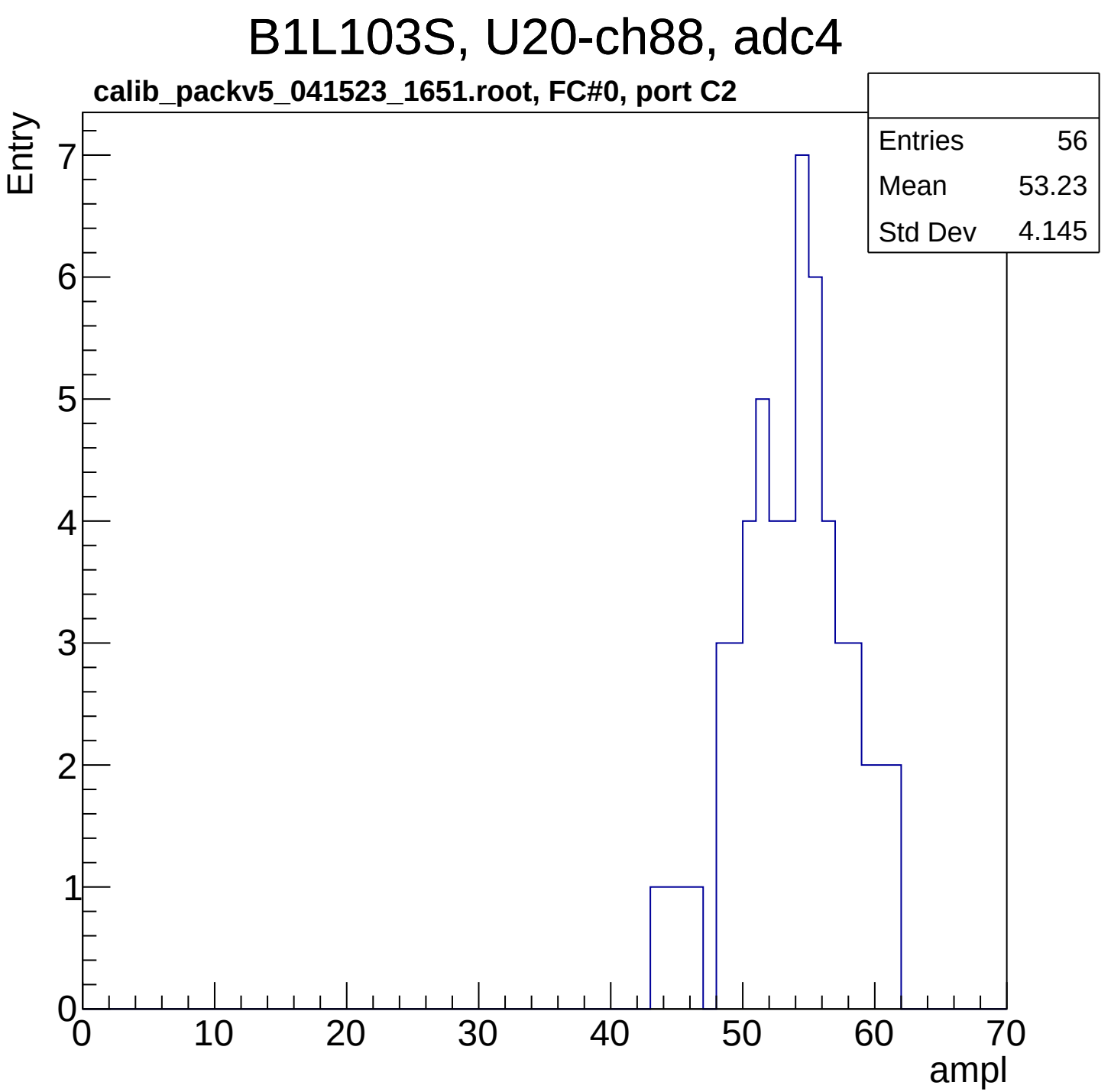
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch88, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 53.23
Std Dev 4.145
Entry
ampl
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2
3
4
5
6
7
0
10
20
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40
50
60
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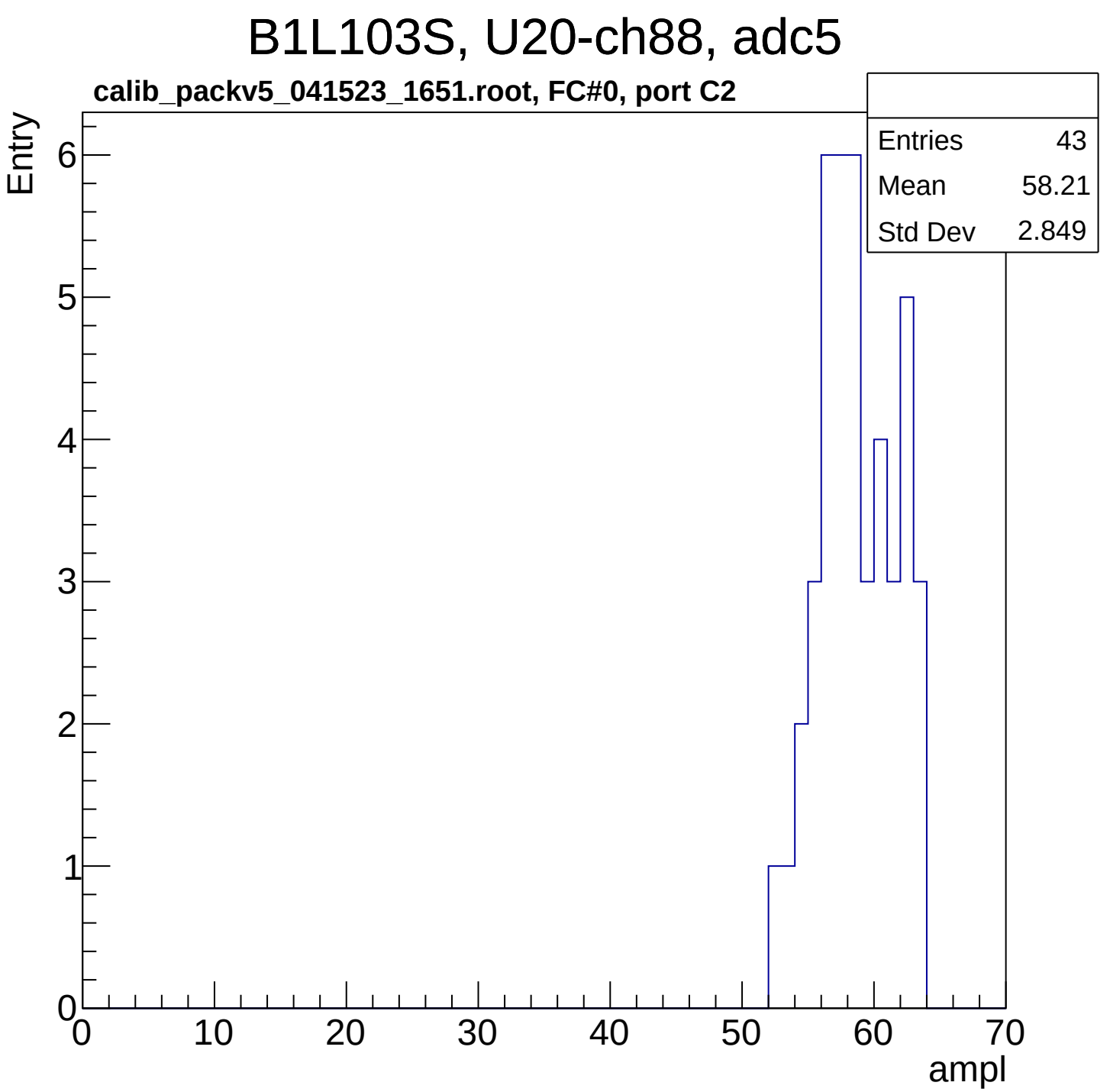
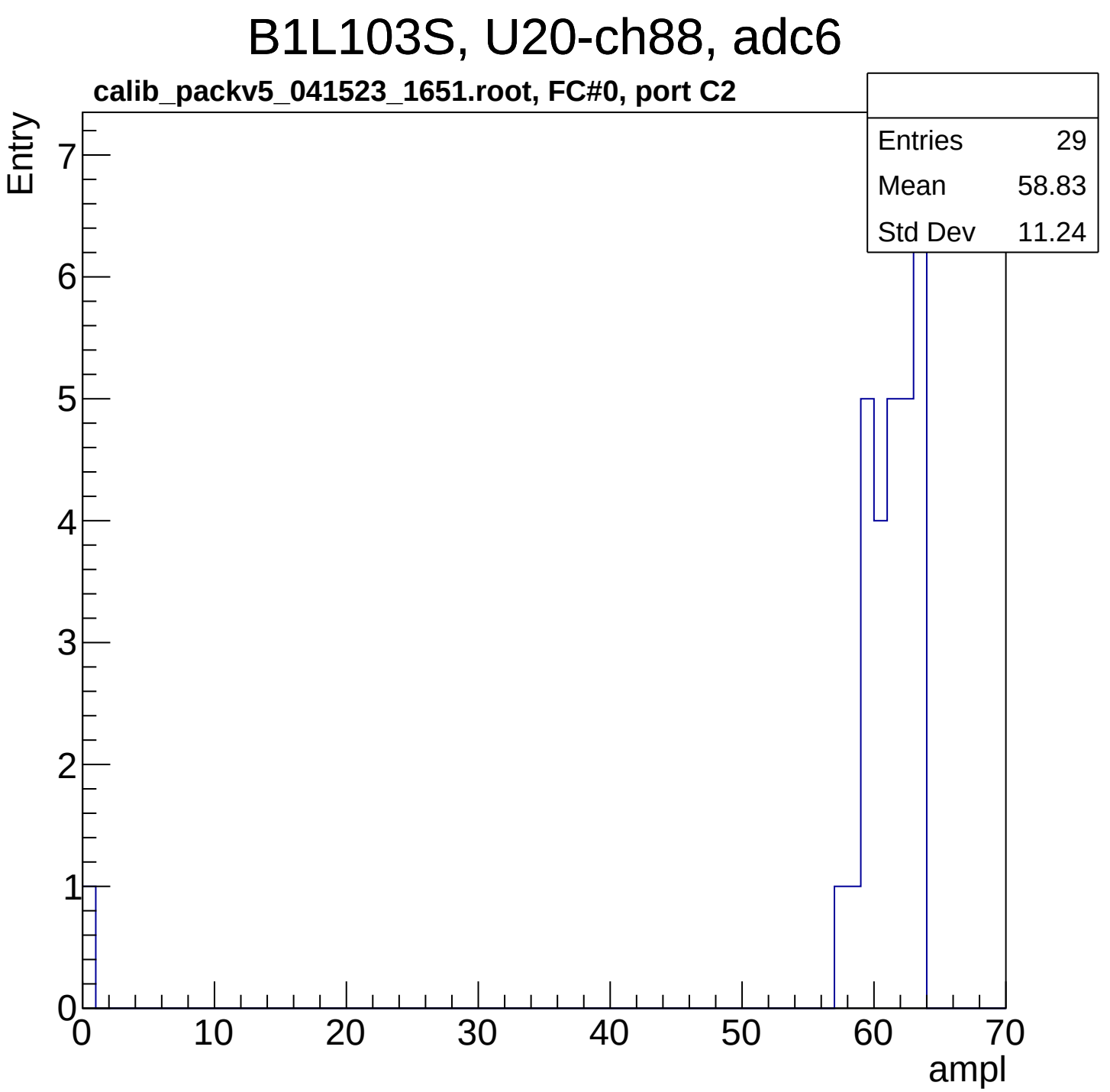
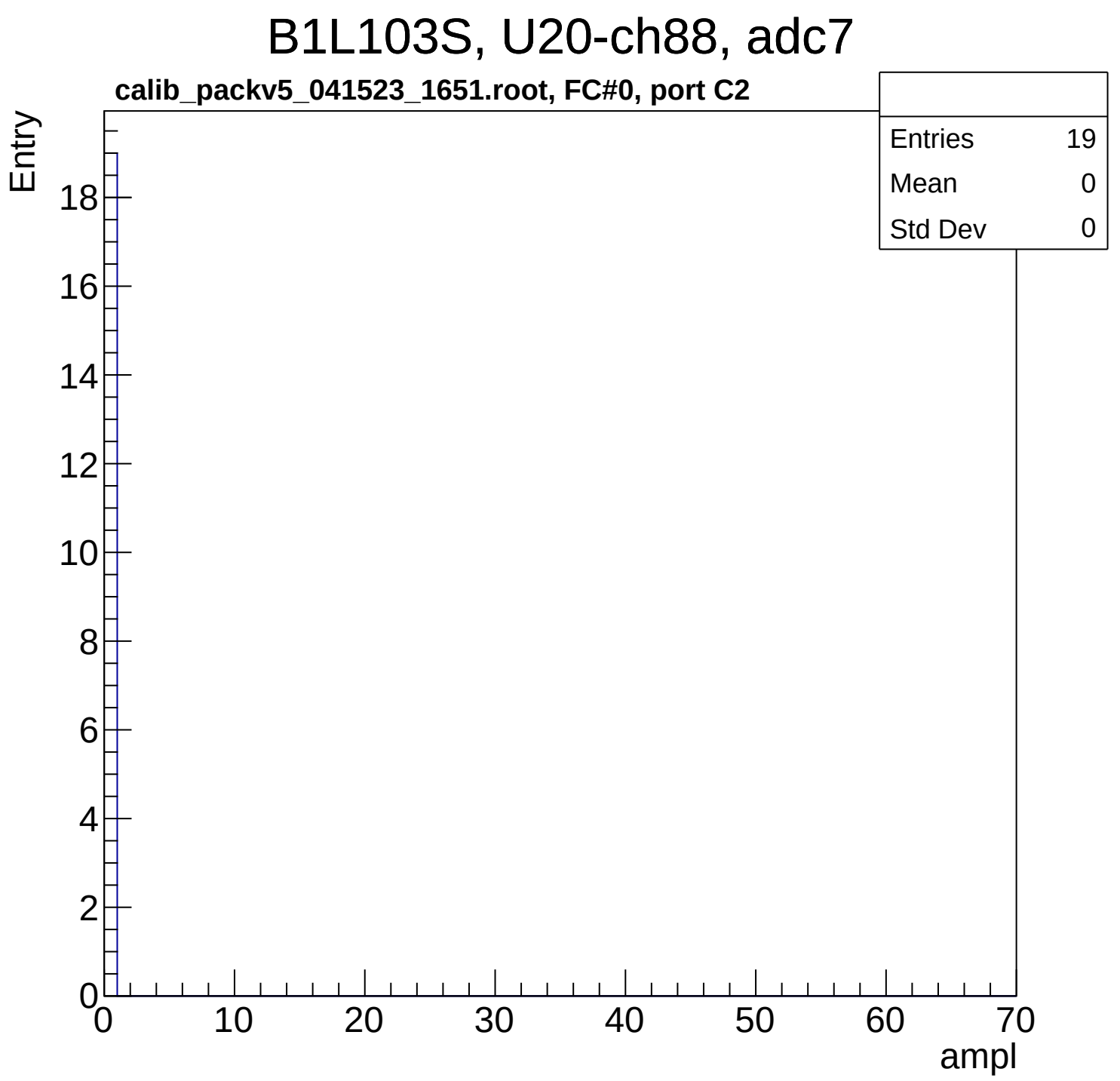
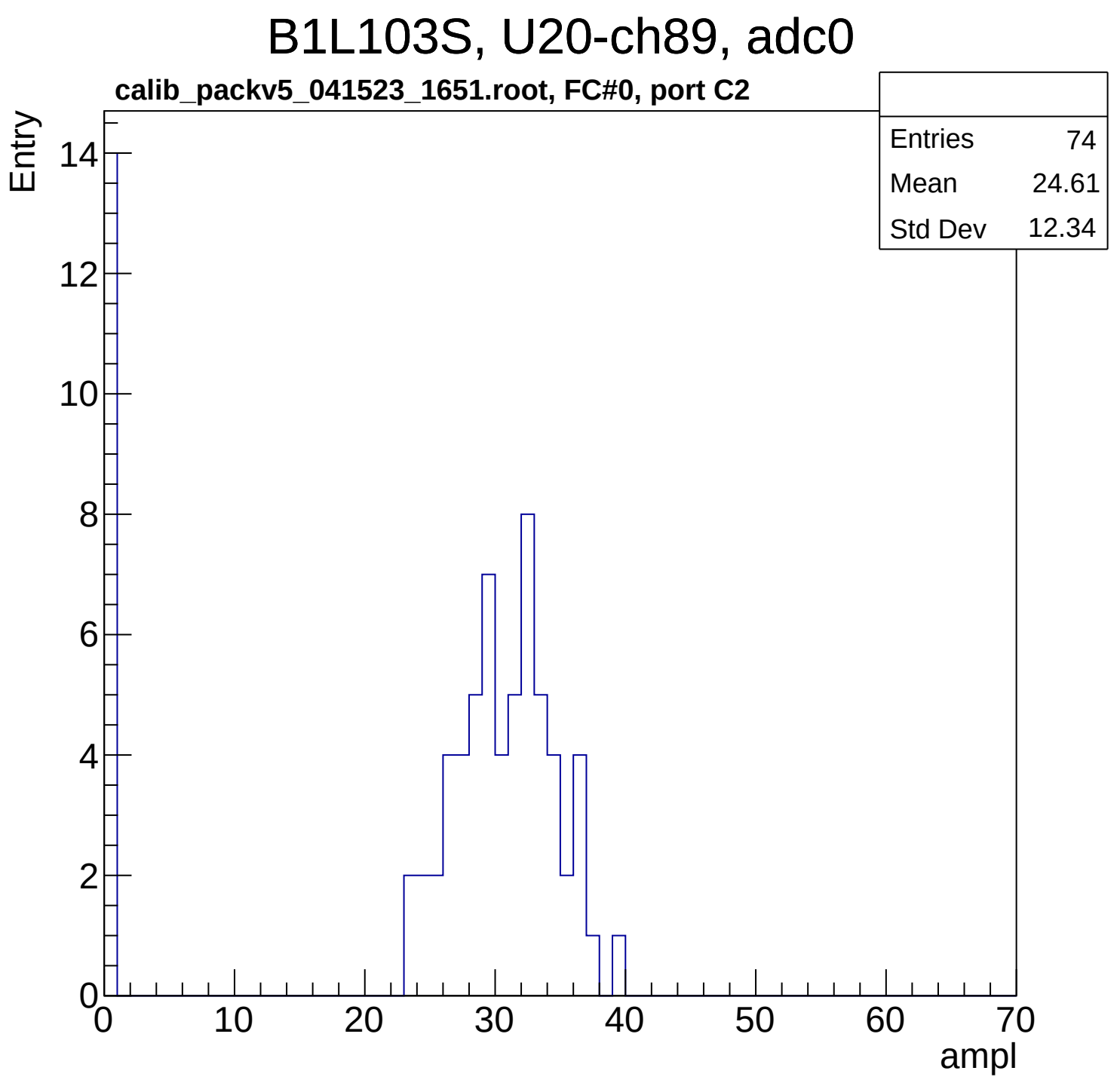

B1L103S, U20-ch88, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 58.21
Std Dev 2.849
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U20-ch88, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 58.83
Std Dev 11.24
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U20-ch88, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch89, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 24.61
Std Dev 12.34
Entry
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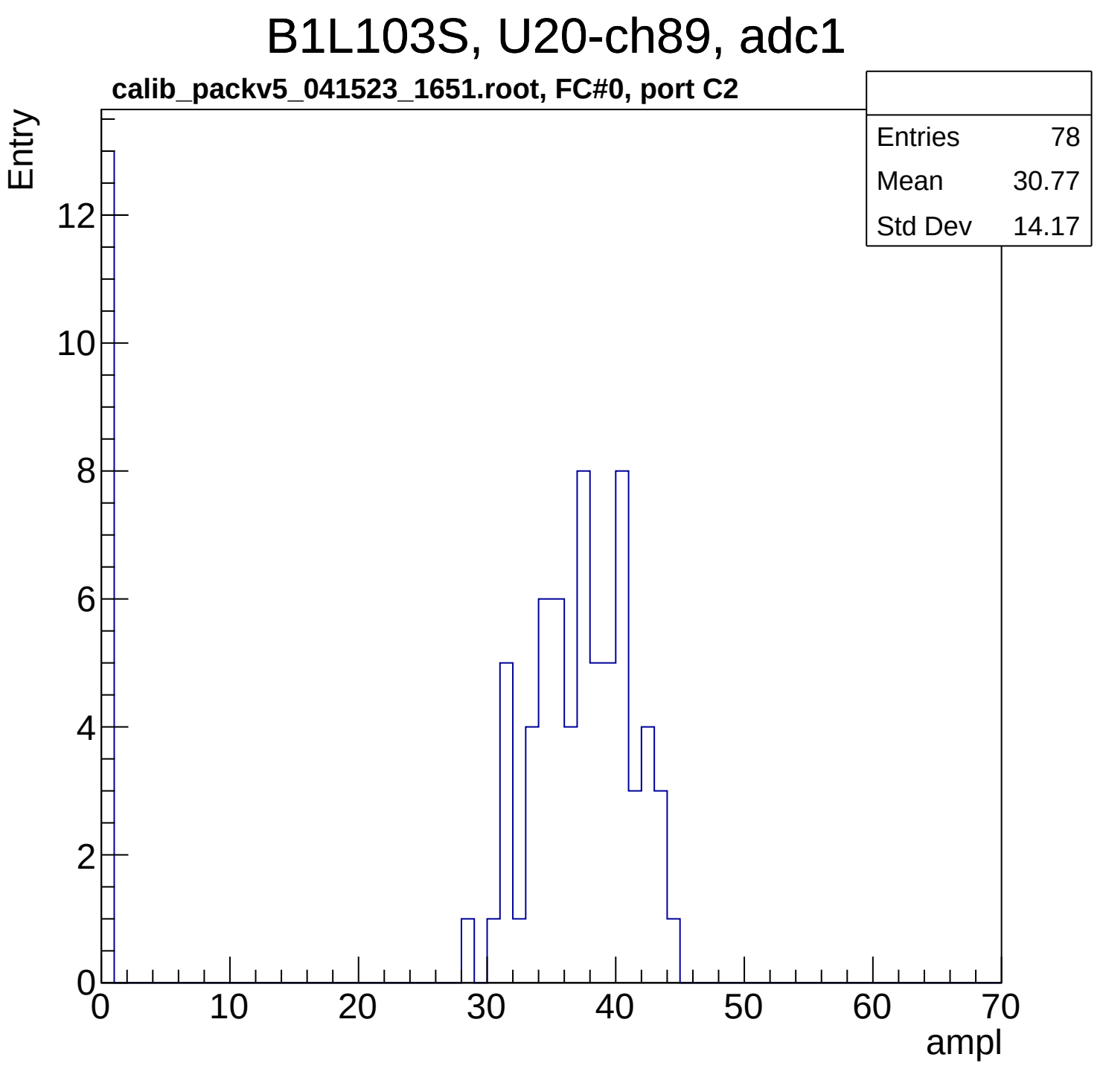
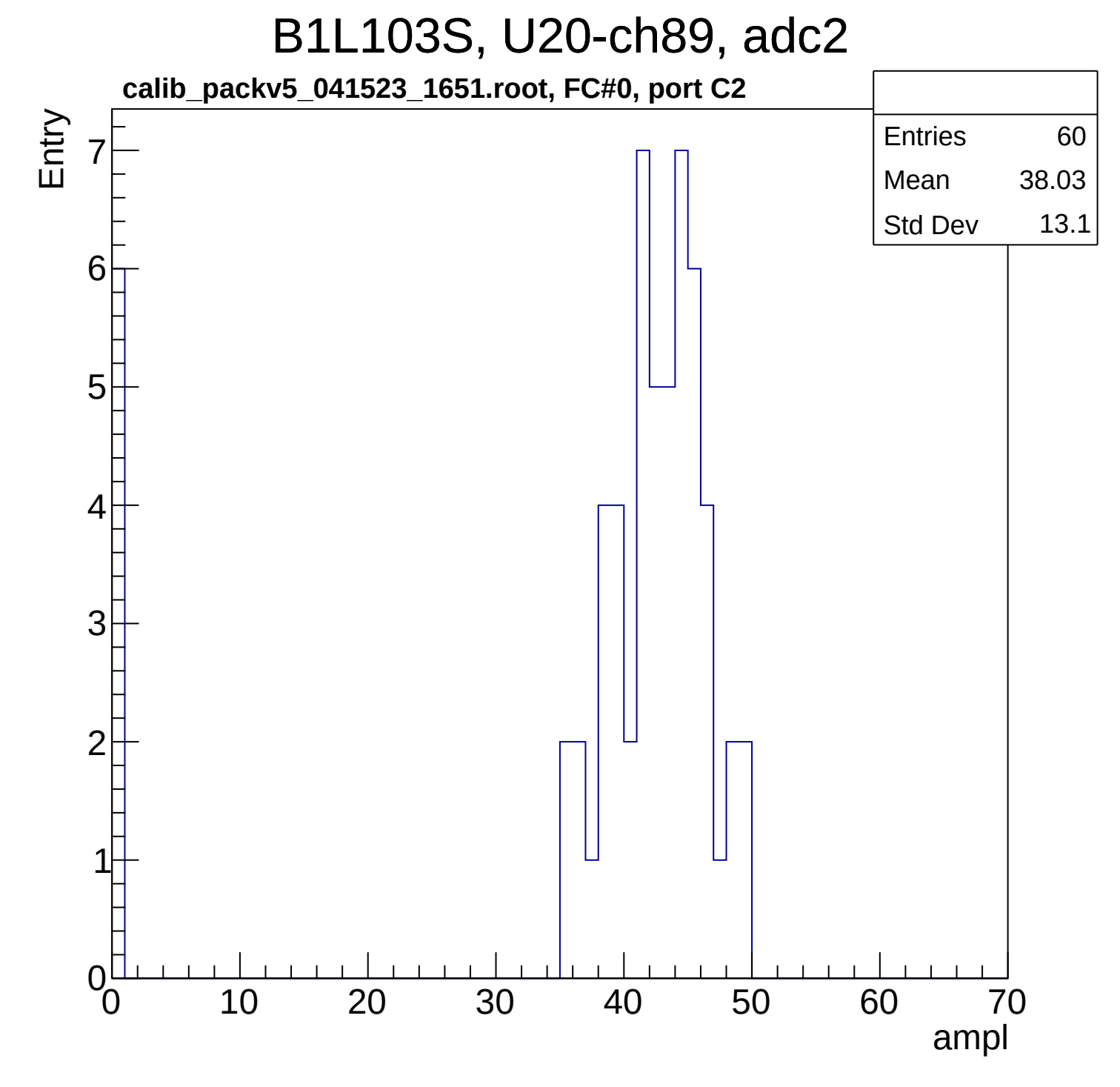
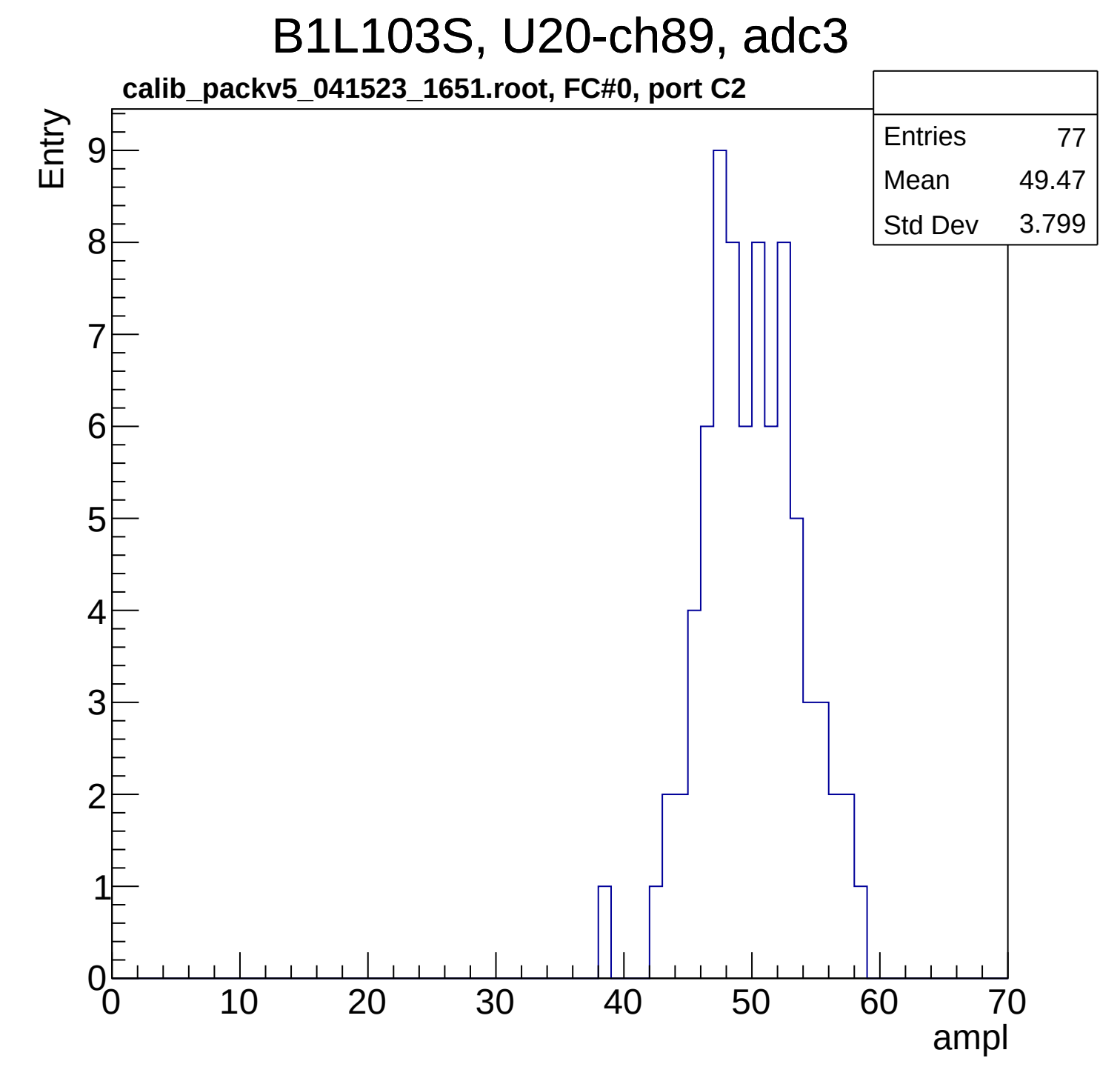
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch89, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 30.77
Std Dev 14.17
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch89, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 38.03
Std Dev 13.1
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U20-ch89, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 49.47
Std Dev 3.799
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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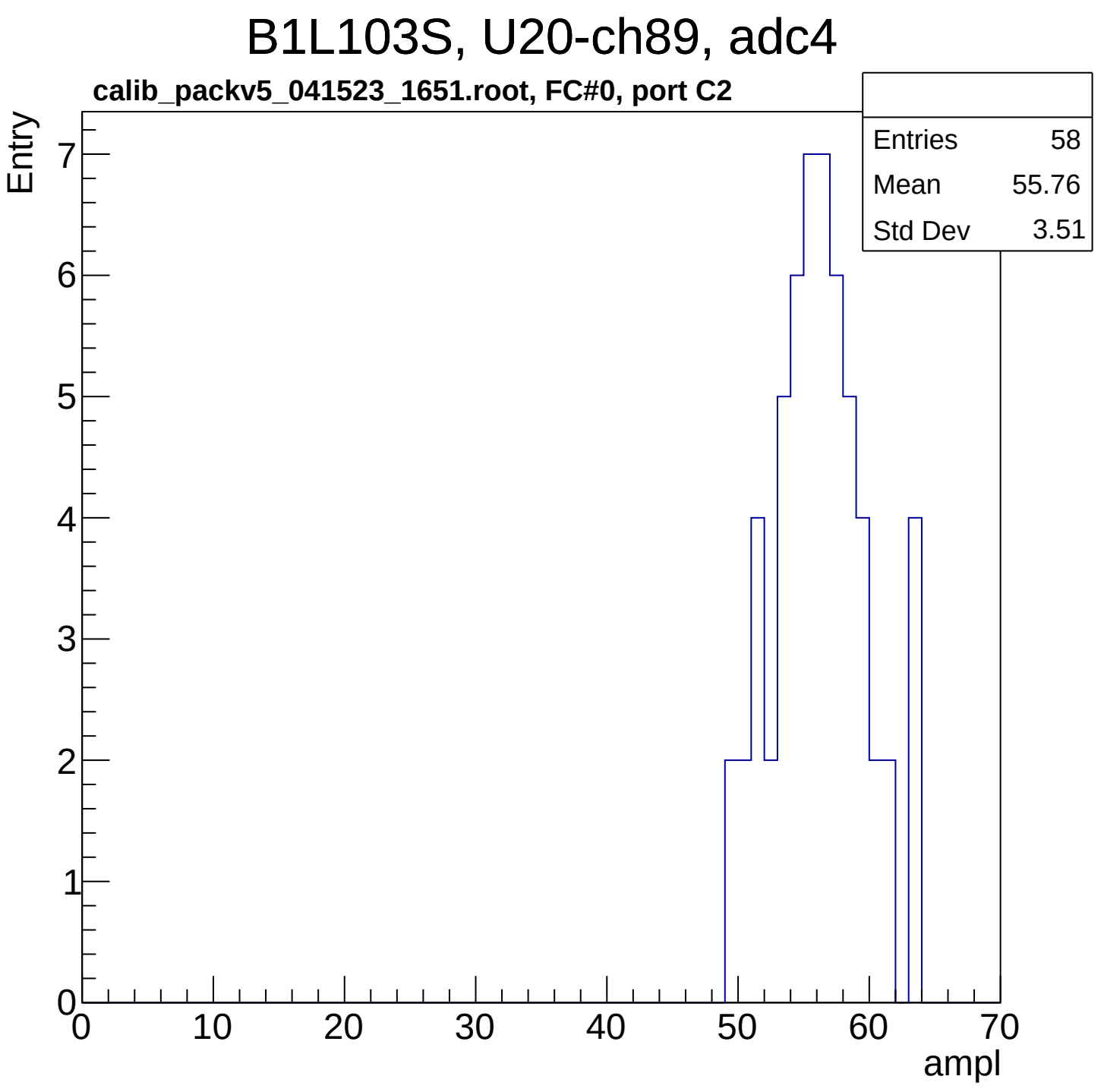
B1L103S, U20-ch89, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 55.76
Std Dev 3.51
Entry
ampl
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1
2
3
4
5
6
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0
10
20
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60
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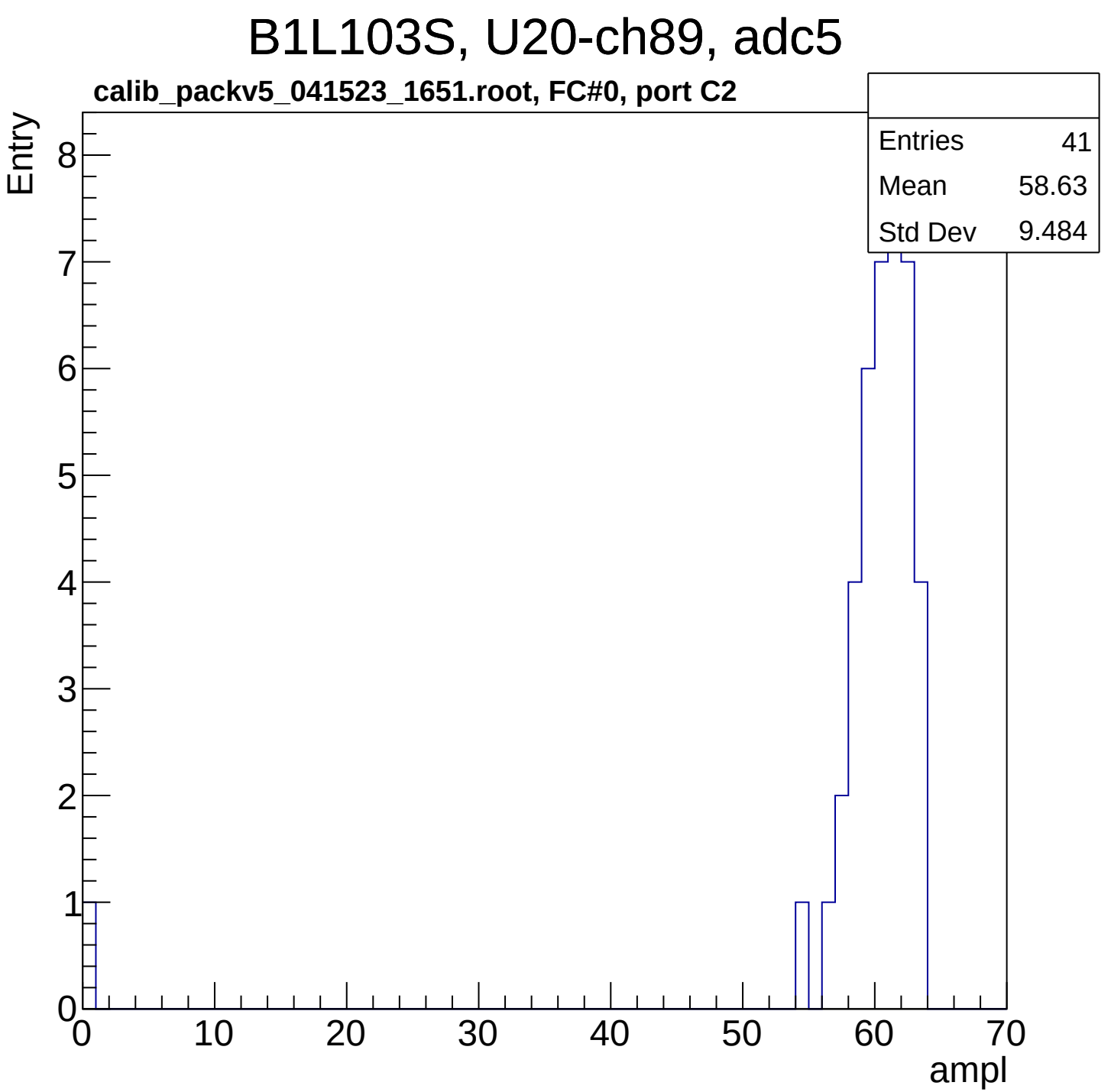
B1L103S, U20-ch89, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 58.63
Std Dev 9.484
Entry
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3
4
5
6
7
8
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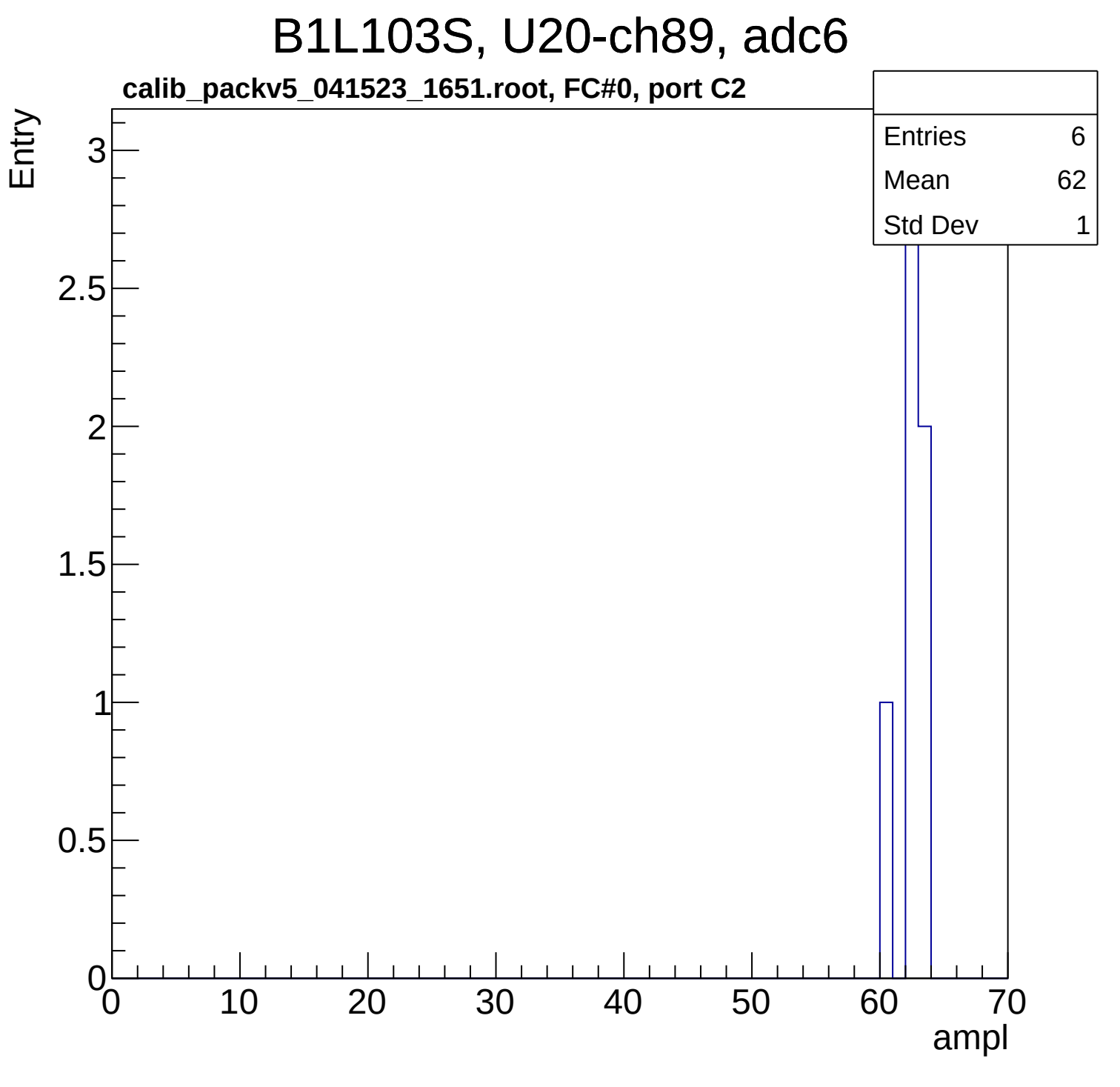
50
60
70
ampl


B1L103S, U20-ch89, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 62
Std Dev 1
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
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40
50
60
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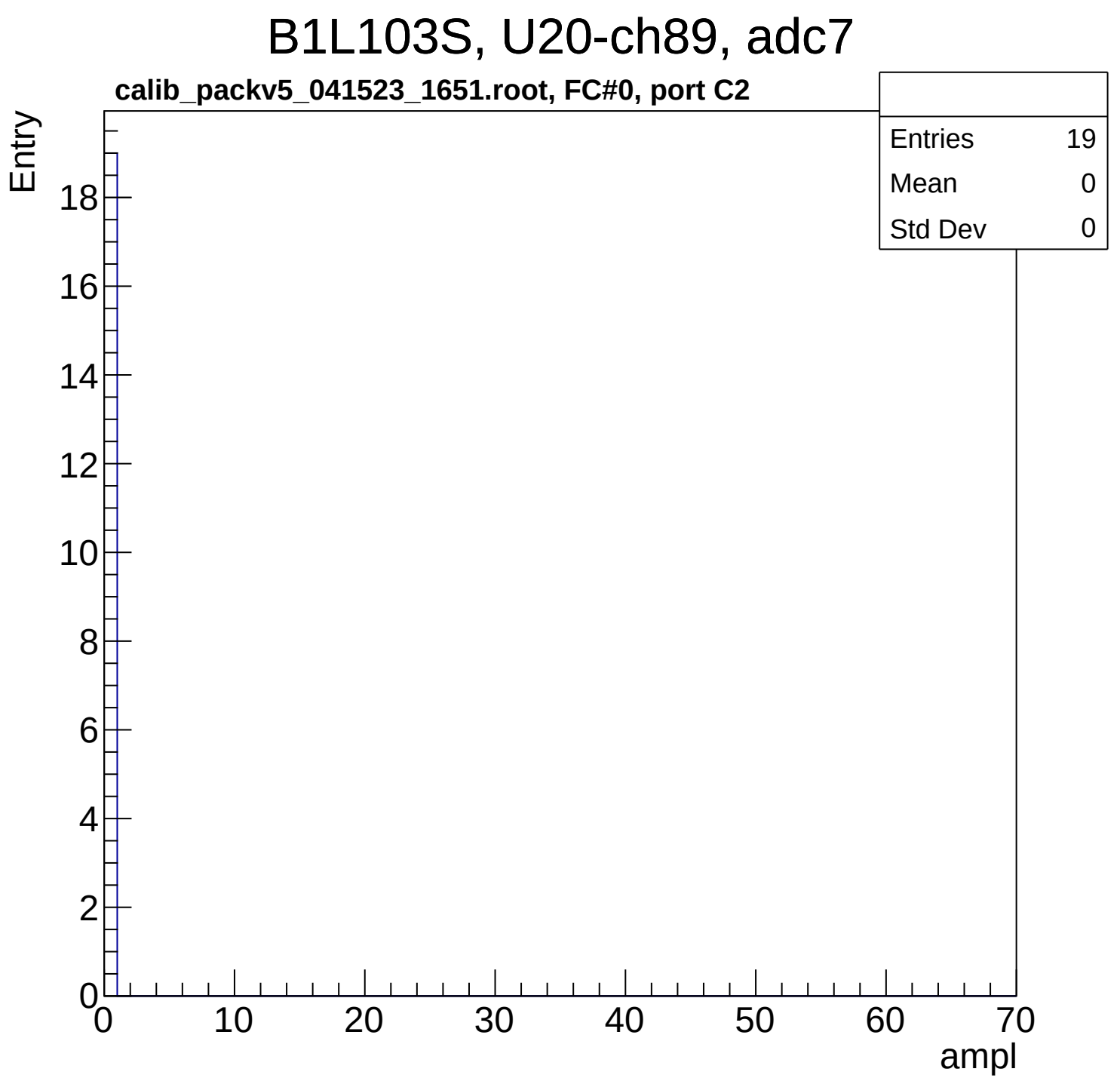
B1L103S, U20-ch89, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
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50
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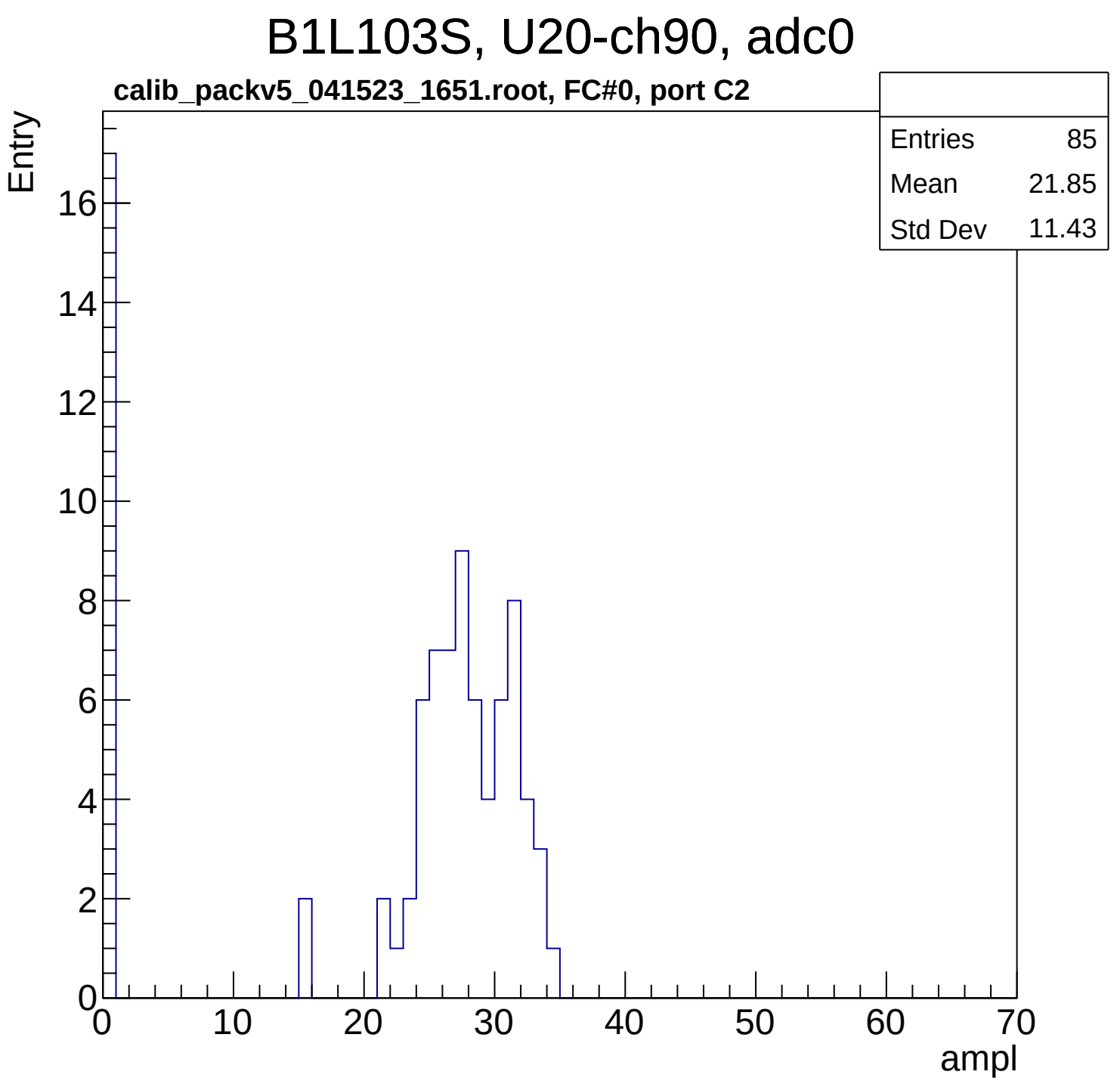
70
ampl


B1L103S, U20-ch90, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 21.85
Std Dev 11.43
Entry
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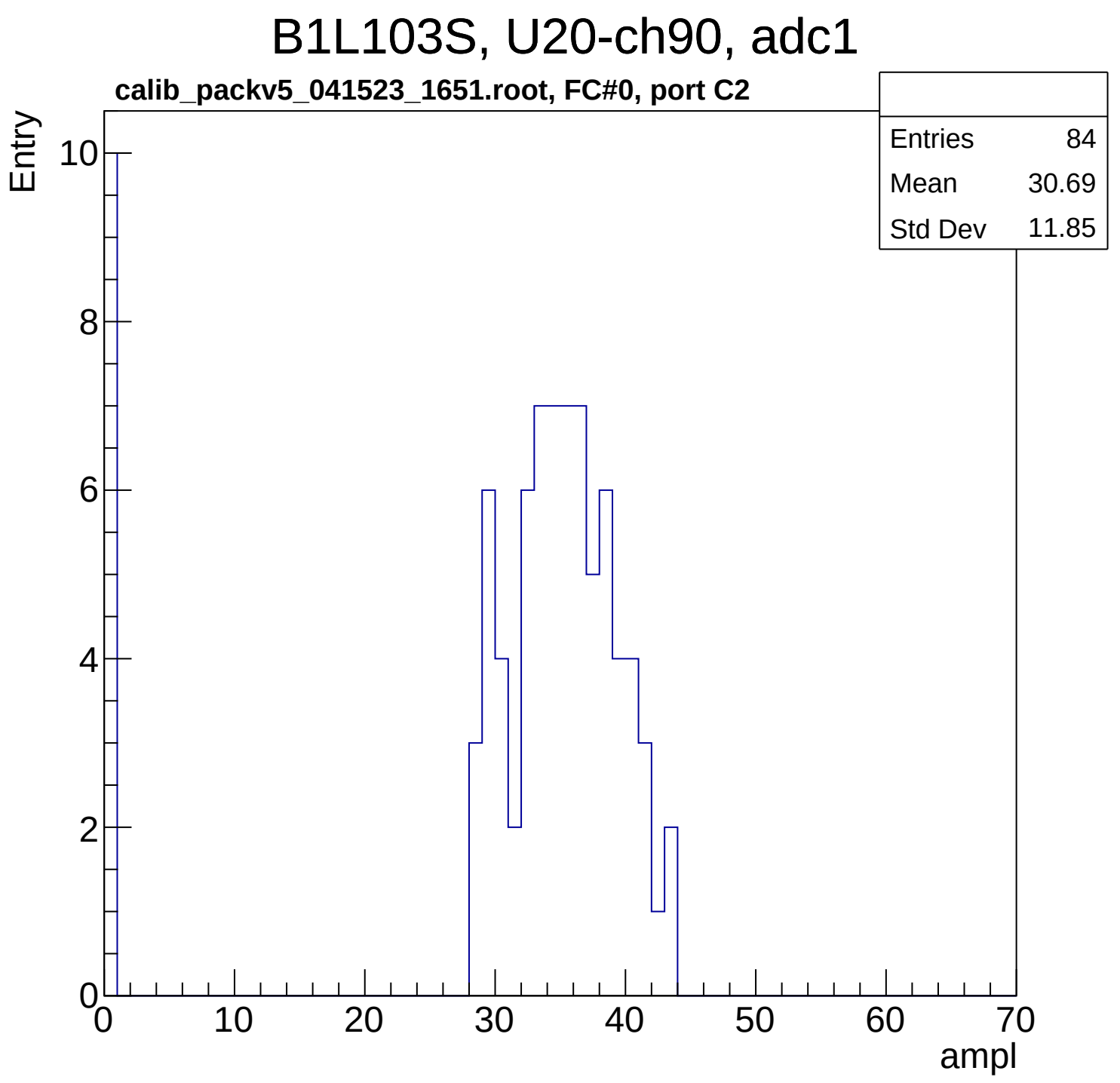
70
ampl


B1L103S, U20-ch90, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 30.69
Std Dev 11.85
Entry
ampl
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6
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0
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20
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60
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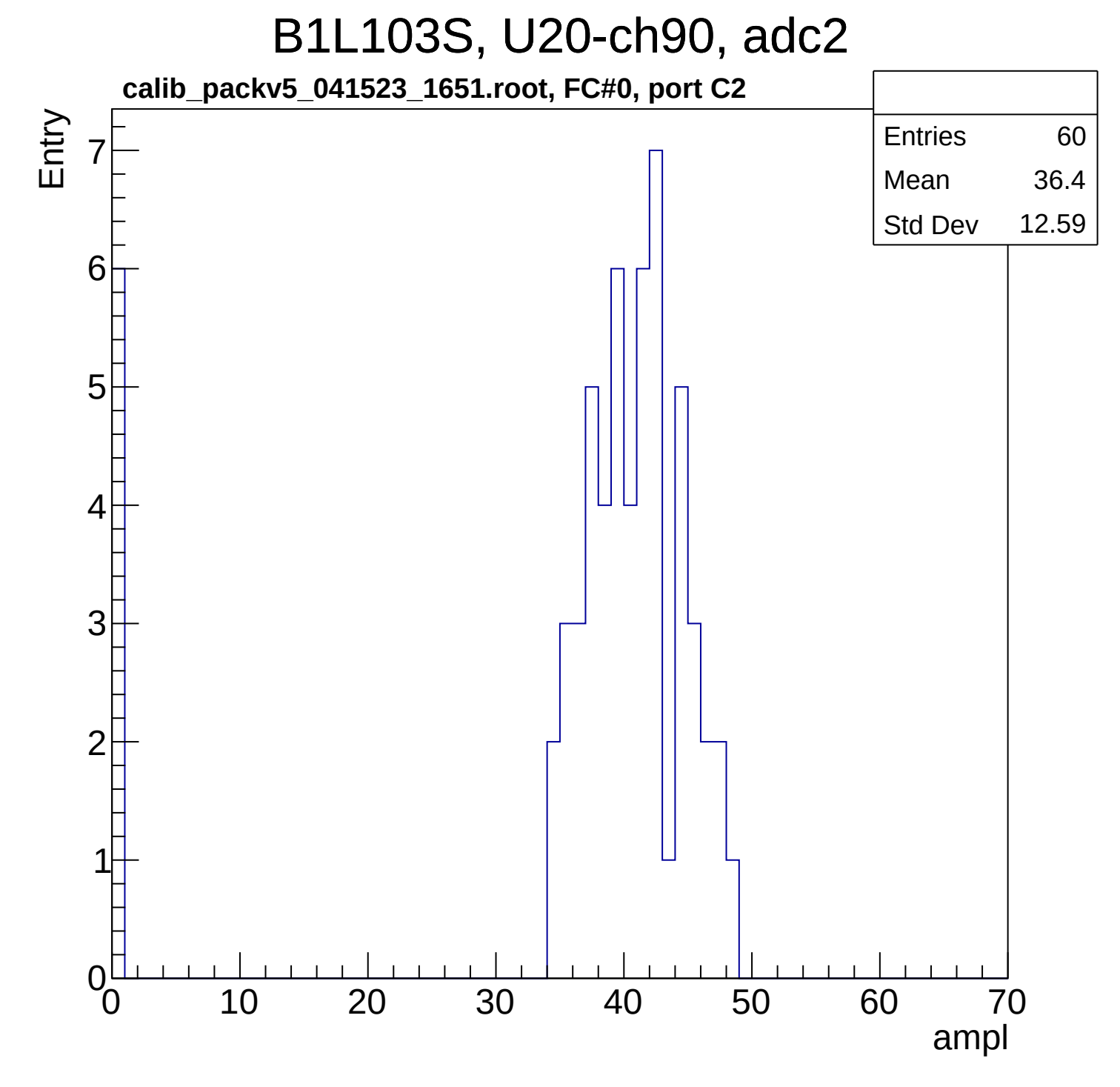
B1L103S, U20-ch90, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 36.4
Std Dev 12.59
Entry
ampl
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3
4
5
6
7
0
10
20
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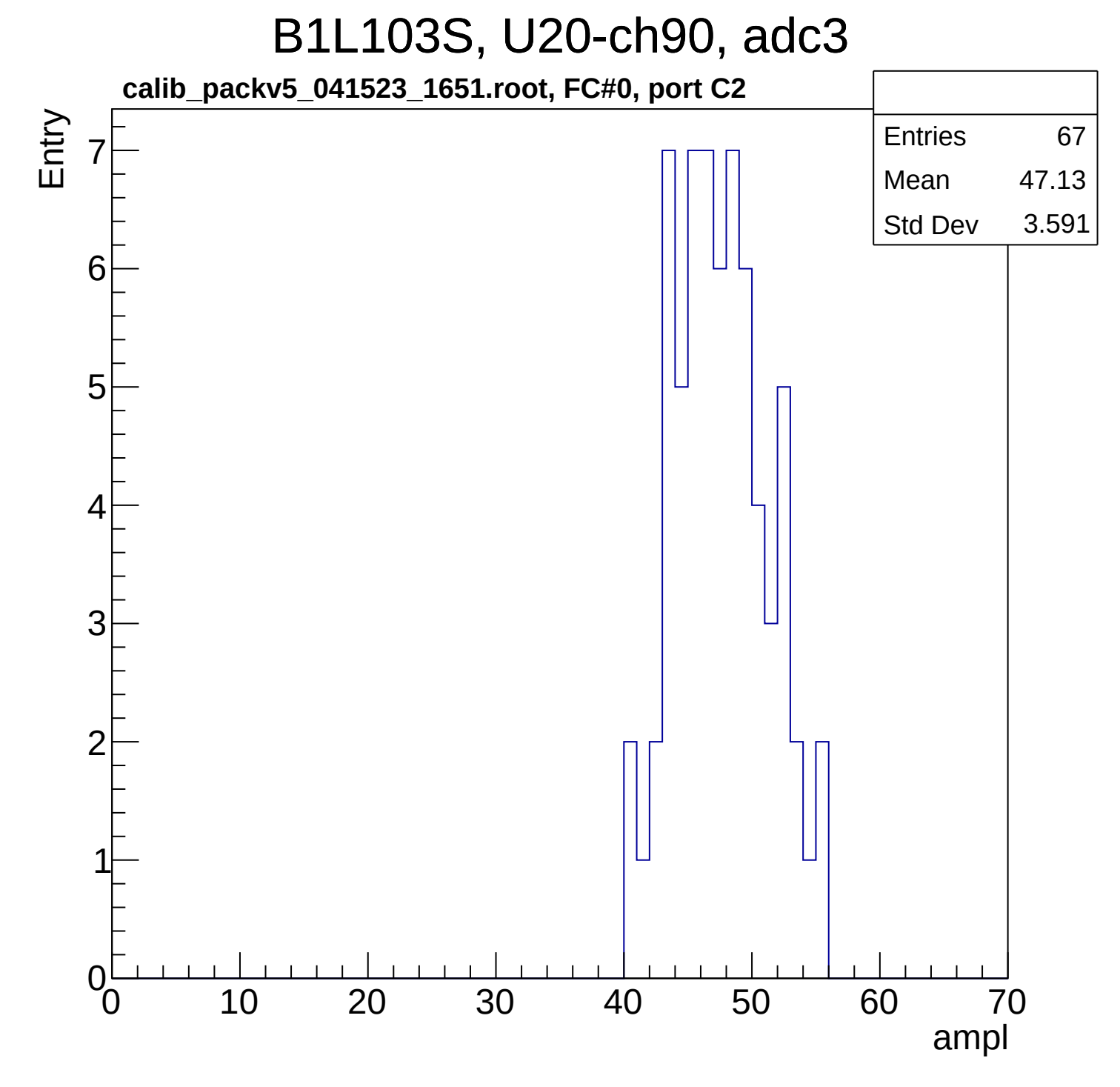
B1L103S, U20-ch90, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 47.13
Std Dev 3.591
Entry
ampl
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1
2
3
4
5
6
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0
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20
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60
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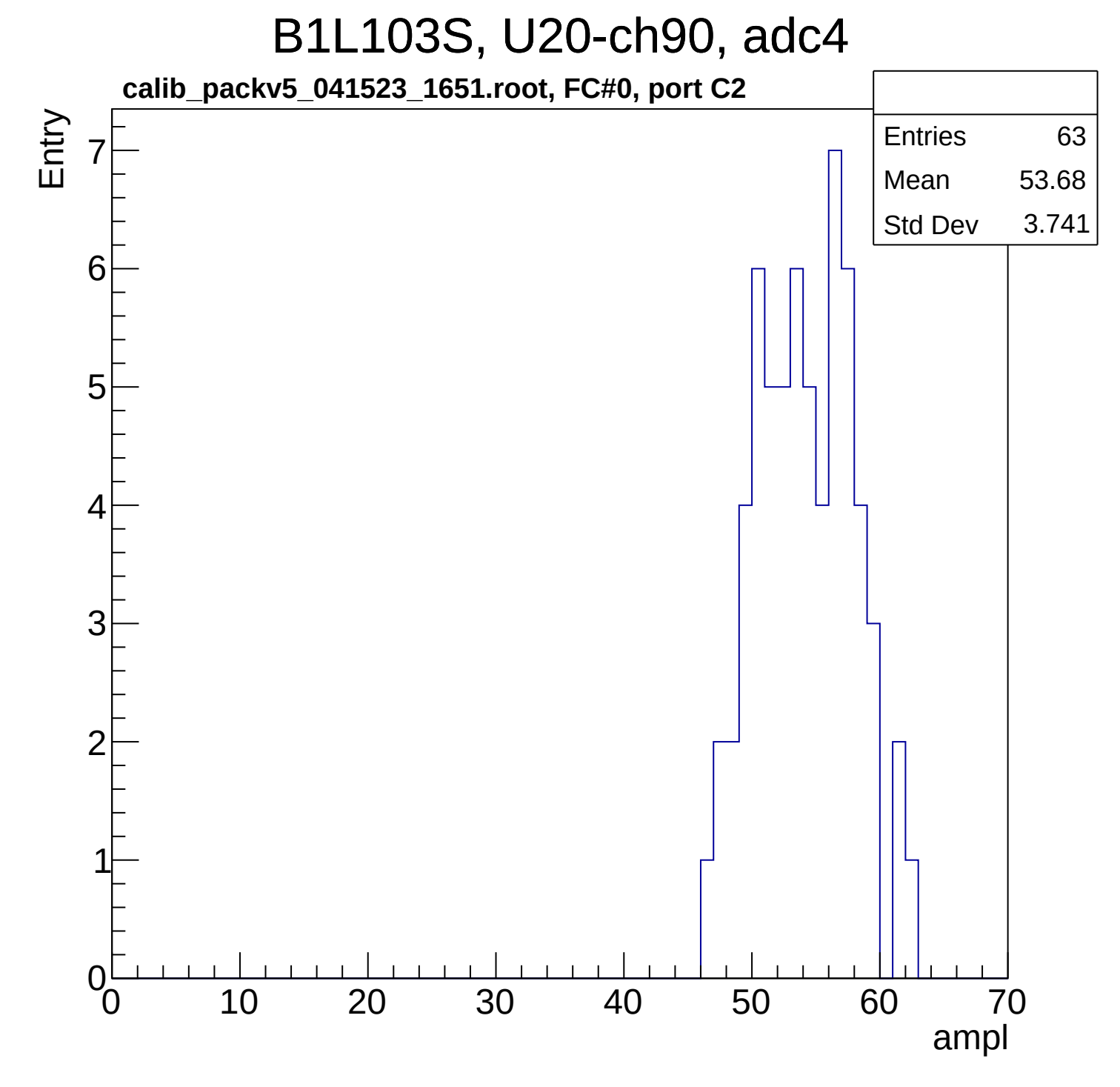
B1L103S, U20-ch90, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 53.68
Std Dev 3.741
Entry
ampl
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0
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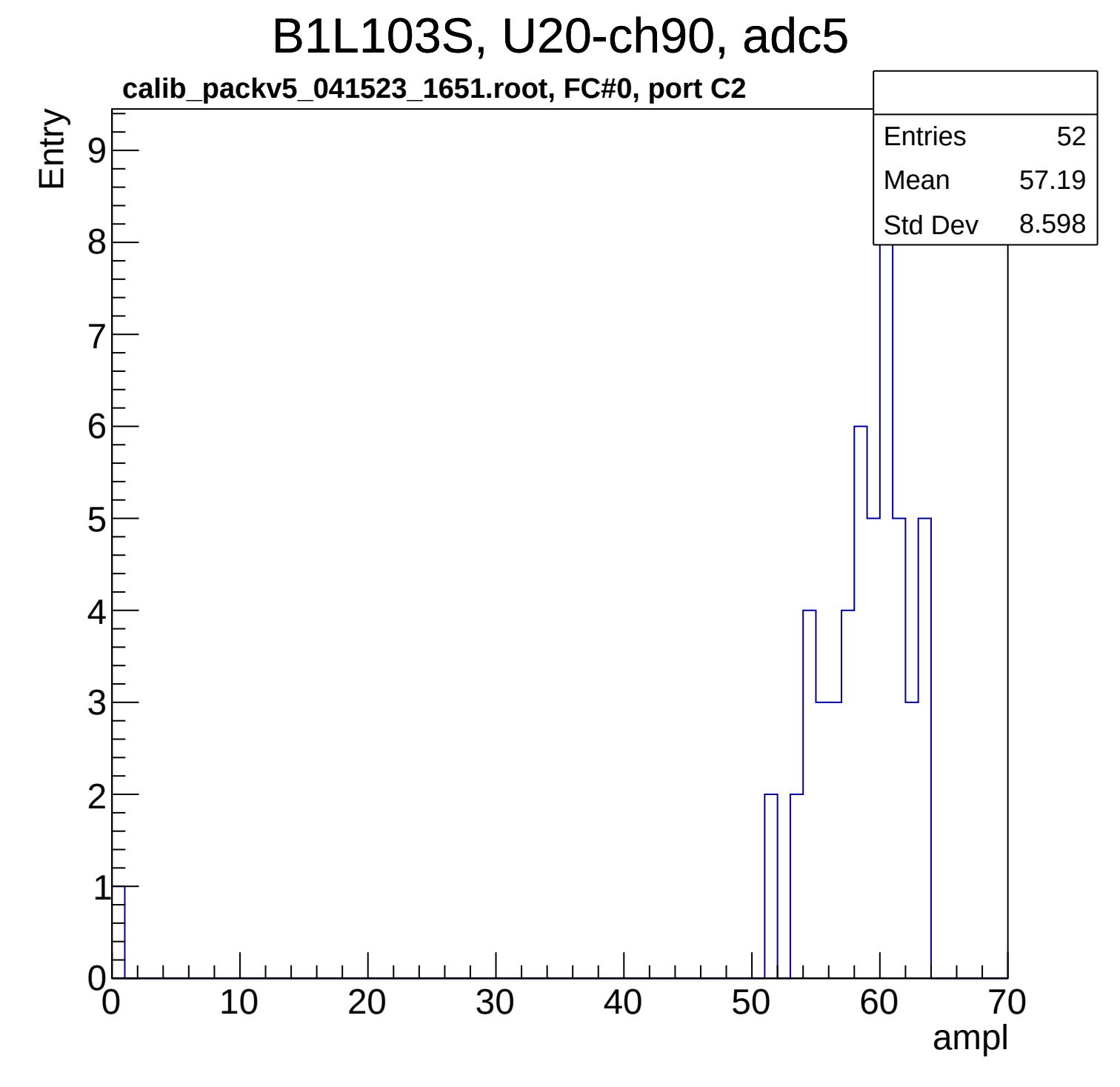
B1L103S, U20-ch90, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 57.19
Std Dev 8.598
Entry
ampl
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3
4
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6
7
8
9
0
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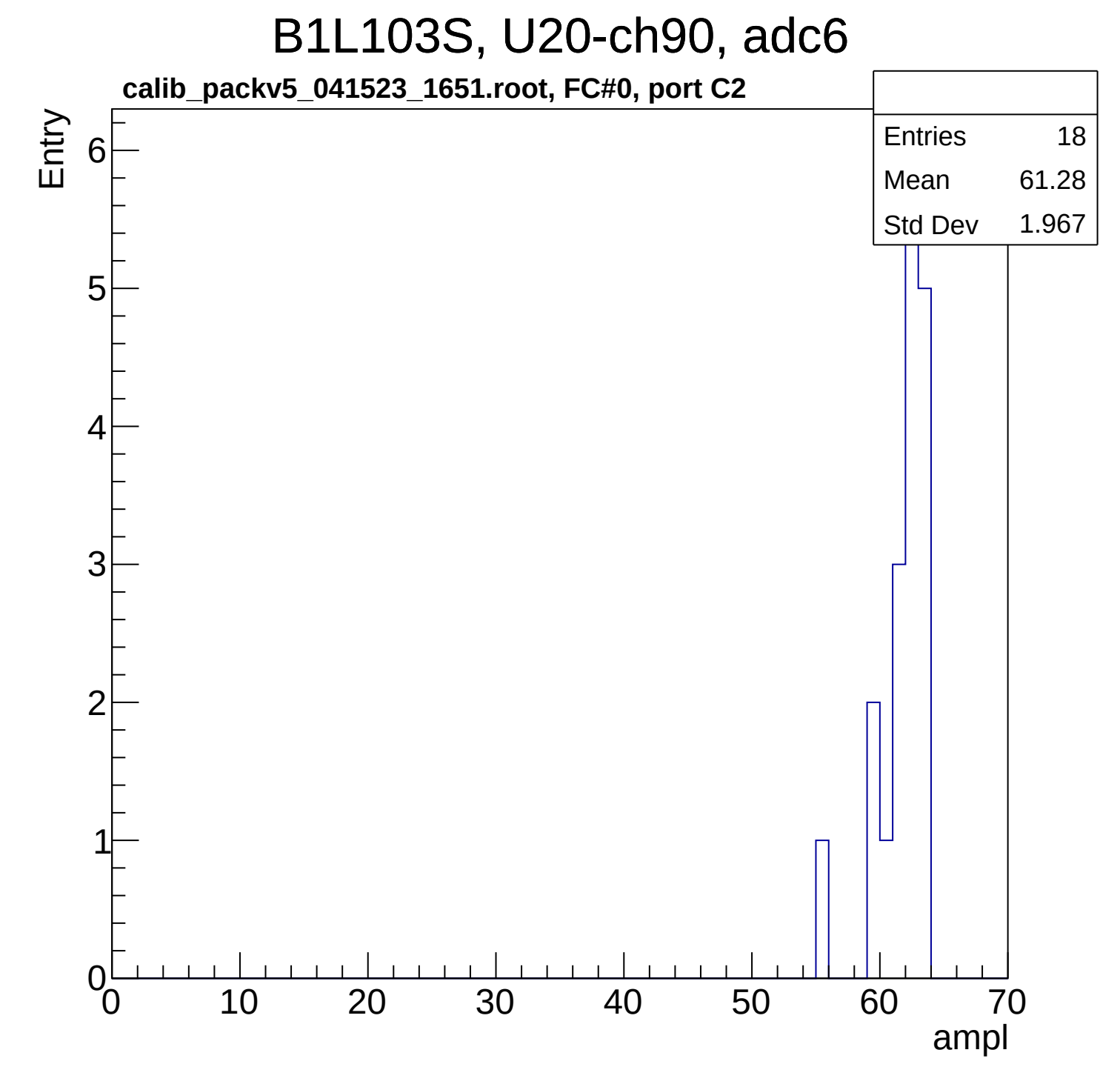
B1L103S, U20-ch90, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 61.28
Std Dev 1.967
Entry
ampl
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0
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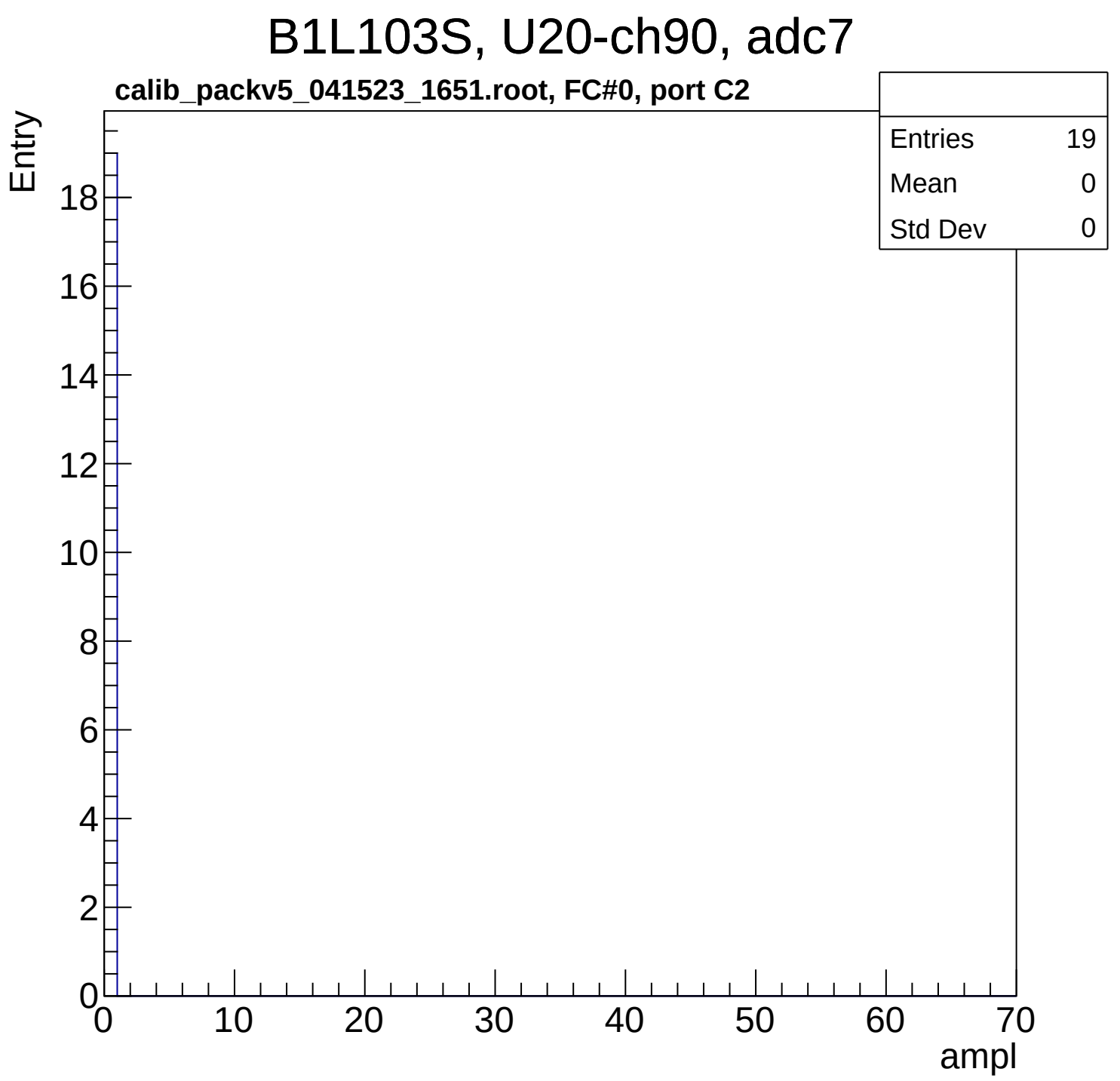
B1L103S, U20-ch90, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
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50
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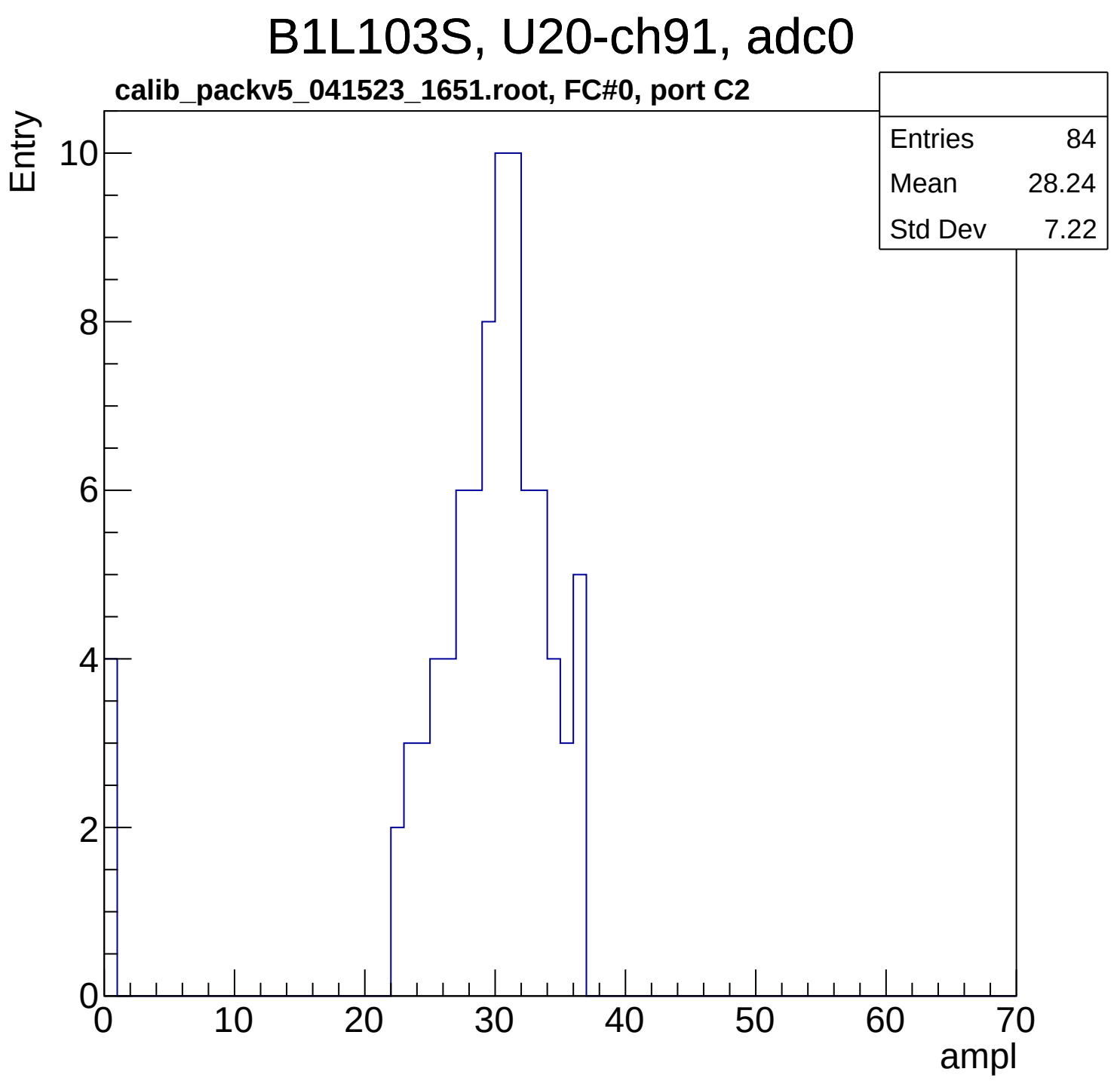
70
ampl


B1L103S, U20-ch91, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 28.24
Std Dev 7.22
Entry
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2
4
6
8
10
0
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20
30
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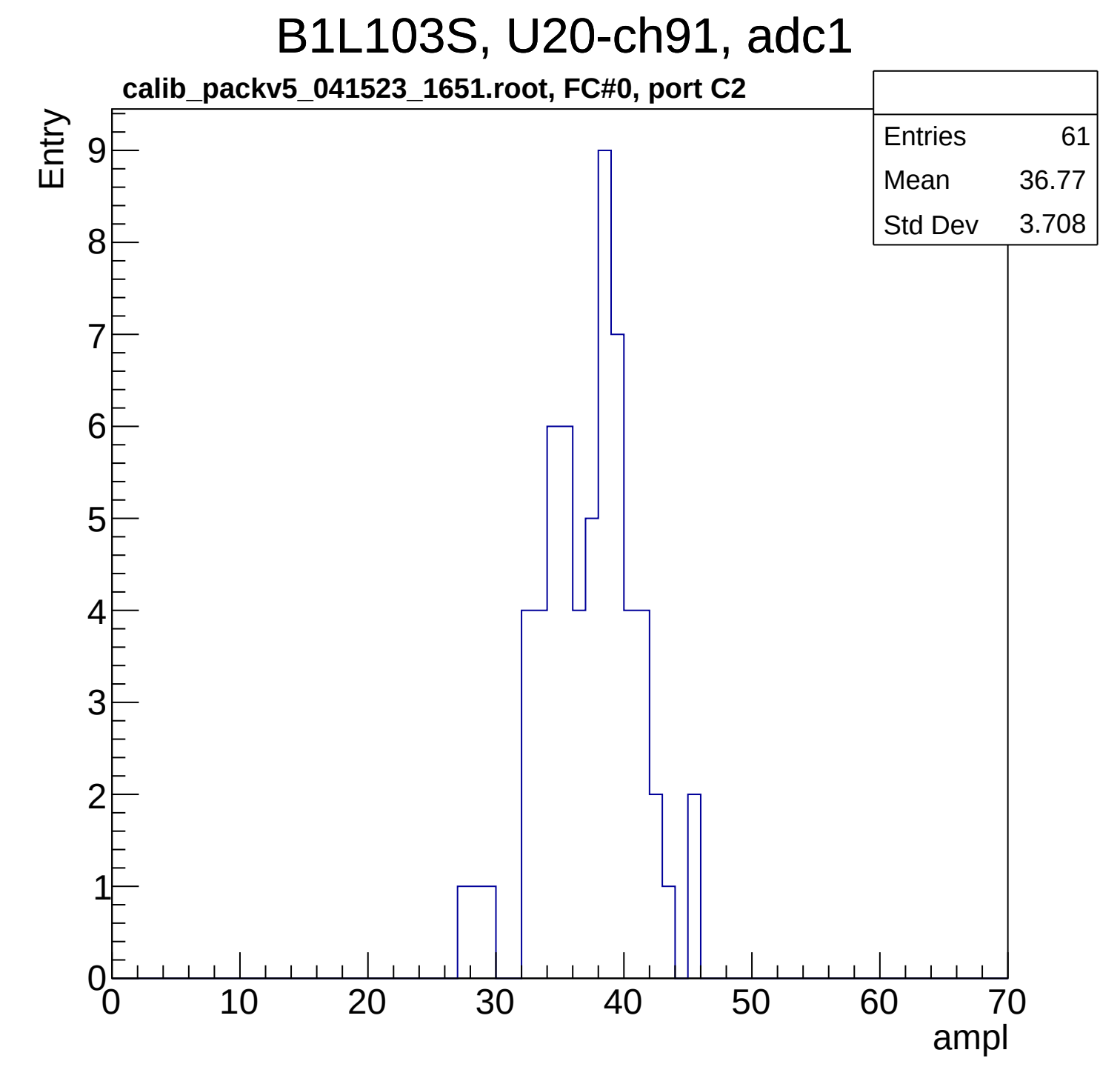
50
60
70
ampl


B1L103S, U20-ch91, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 36.77
Std Dev 3.708
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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60
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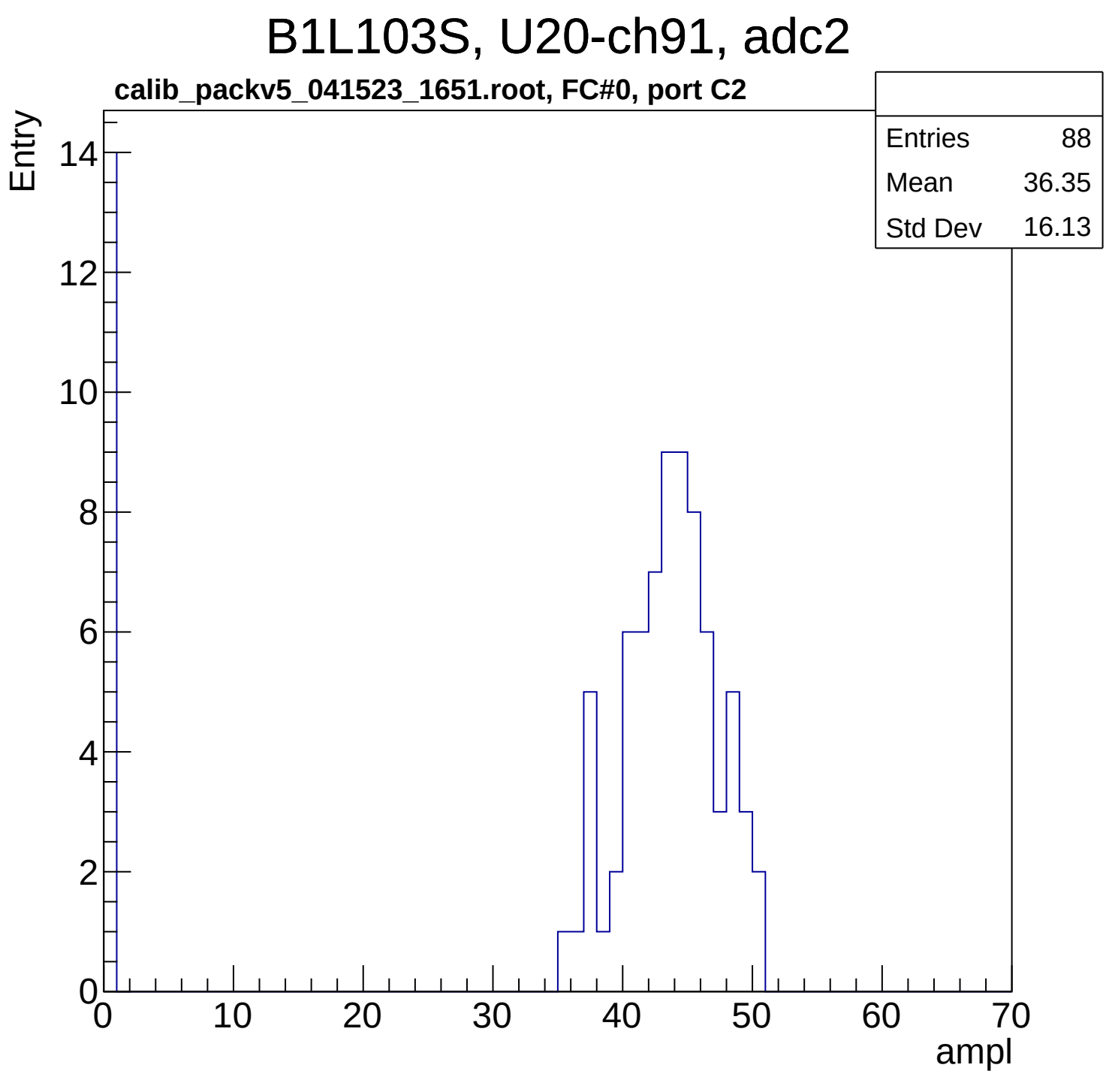
B1L103S, U20-ch91, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 36.35
Std Dev 16.13
Entry
ampl
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4
6
8
10
12
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20
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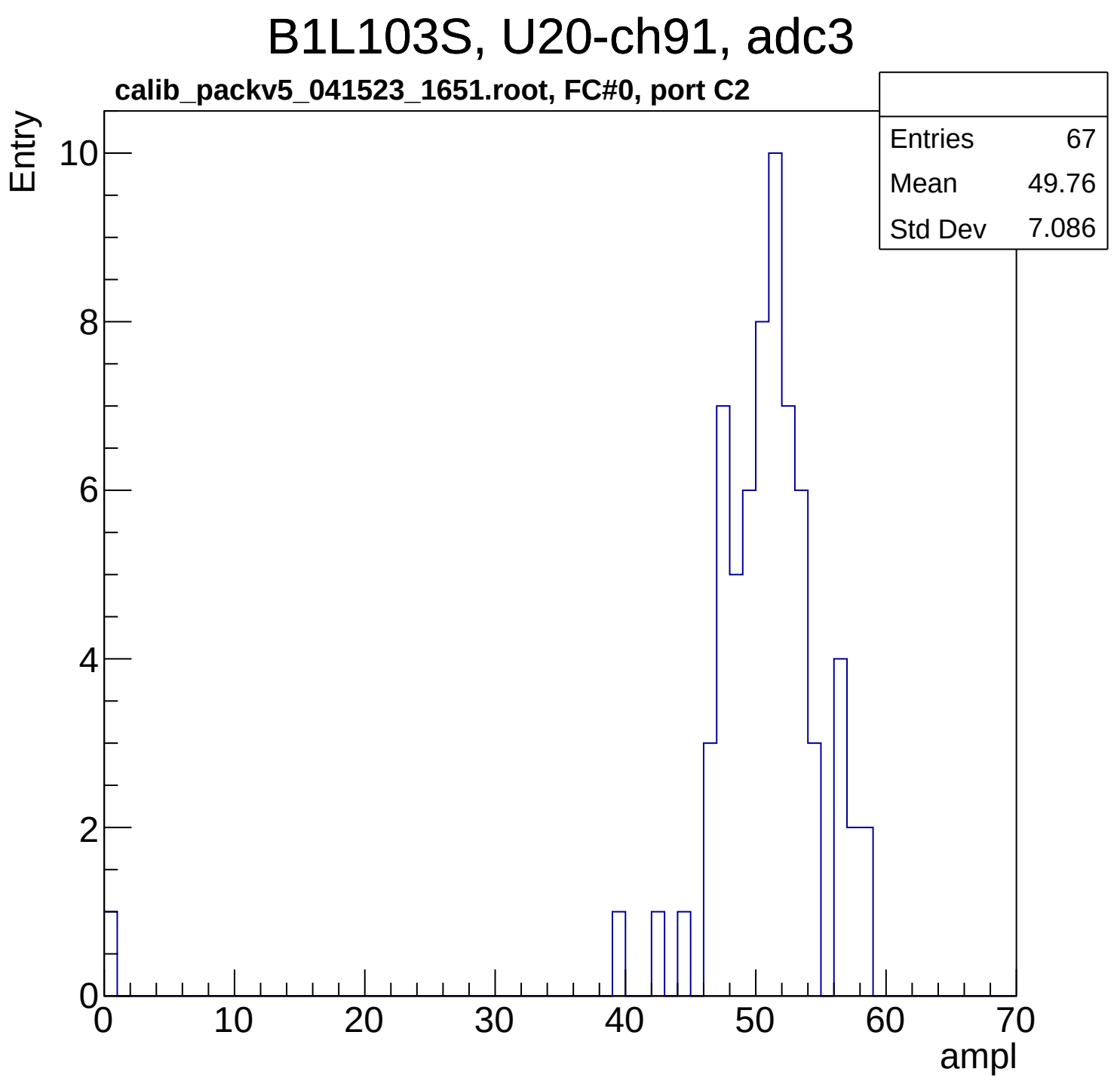
B1L103S, U20-ch91, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 49.76
Std Dev 7.086
Entry
ampl
0
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4
6
8
10
0
10
20
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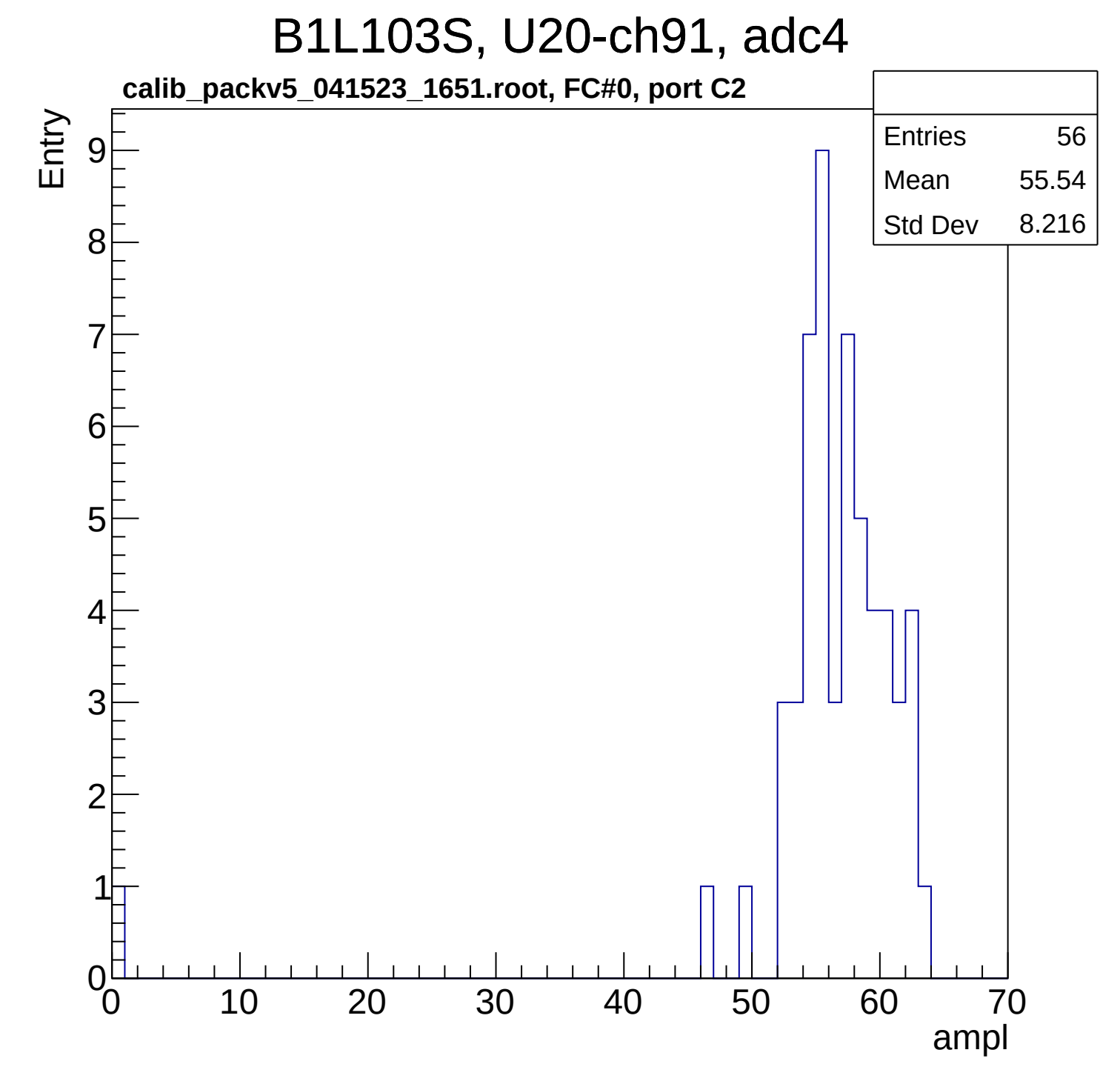
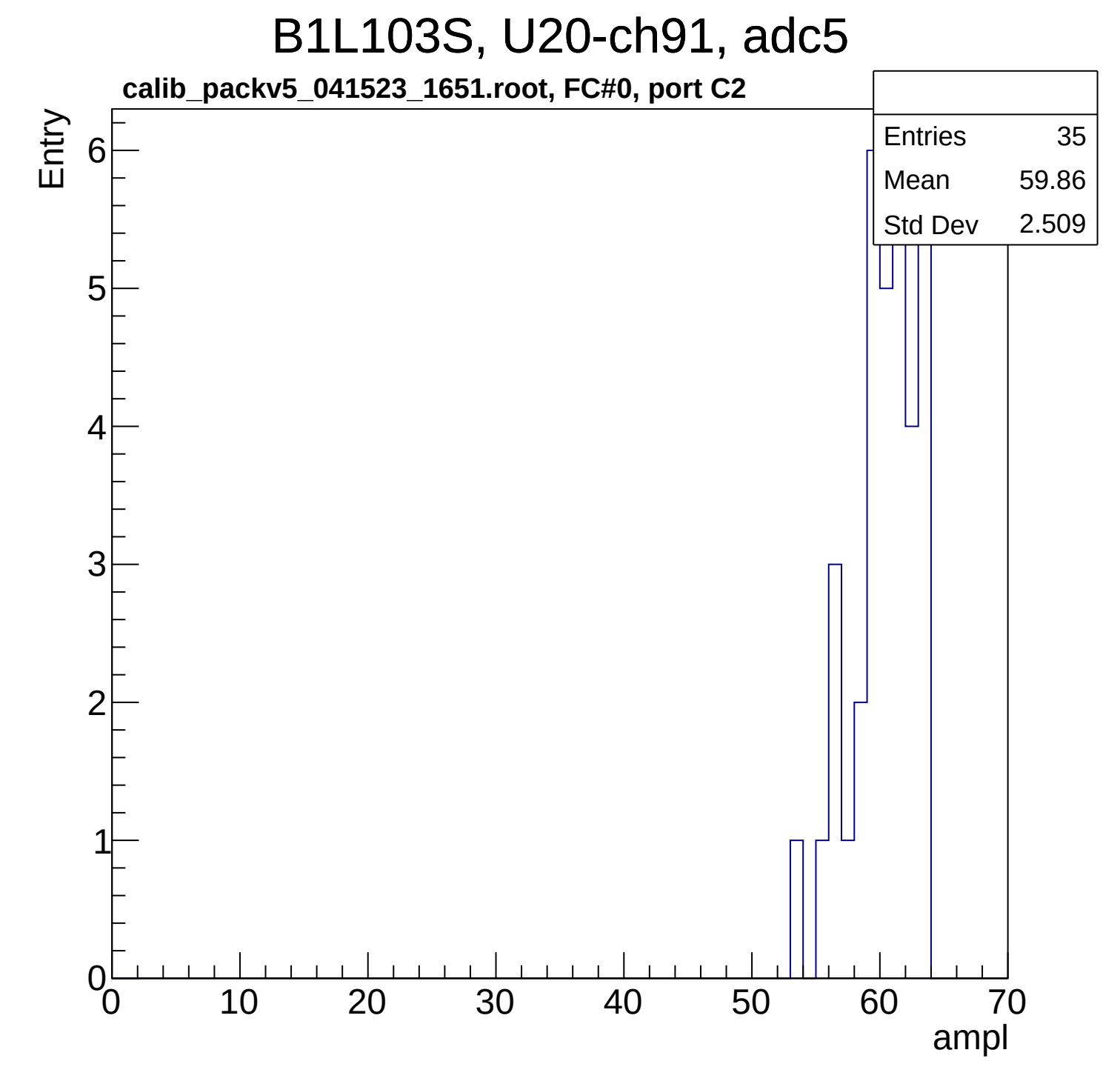
40
50
60
70


B1L103S, U20-ch91, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 55.54
Std Dev 8.216
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch91, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 59.86
Std Dev 2.509
Entry
ampl
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3
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0
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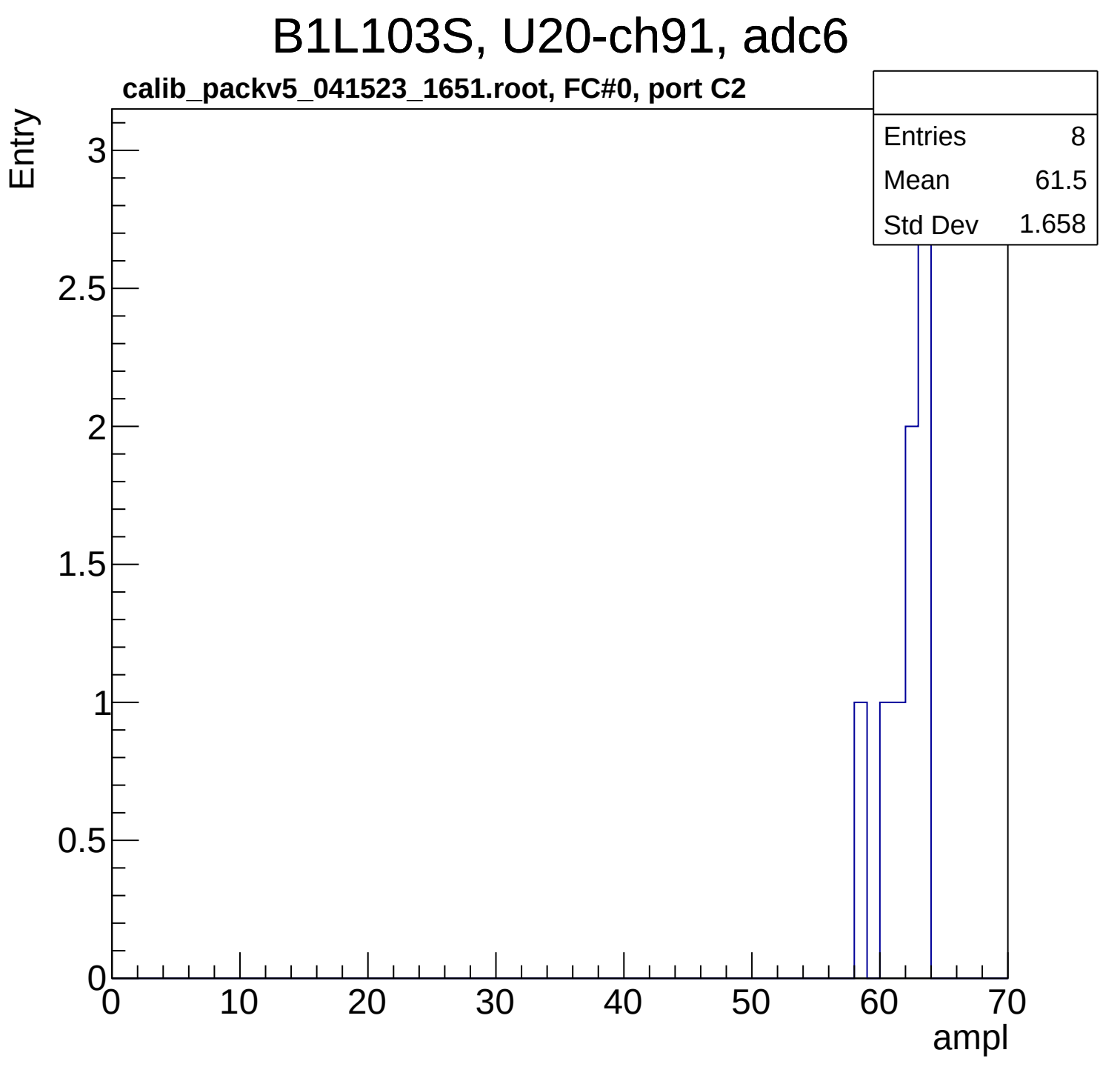
B1L103S, U20-ch91, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 61.5
Std Dev 1.658
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
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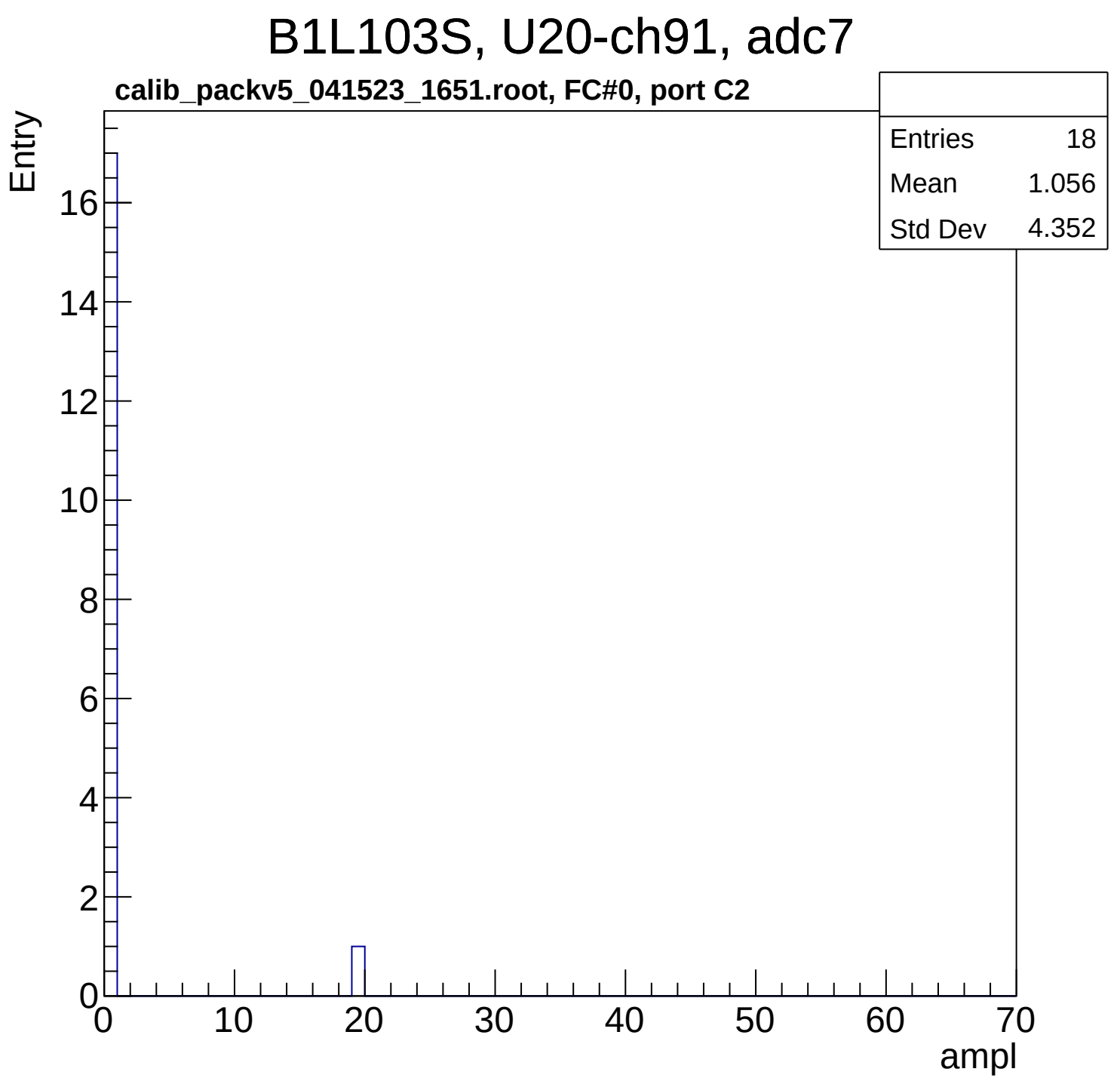
40
50
60
70


B1L103S, U20-ch91, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.056
Std Dev 4.352
Entry
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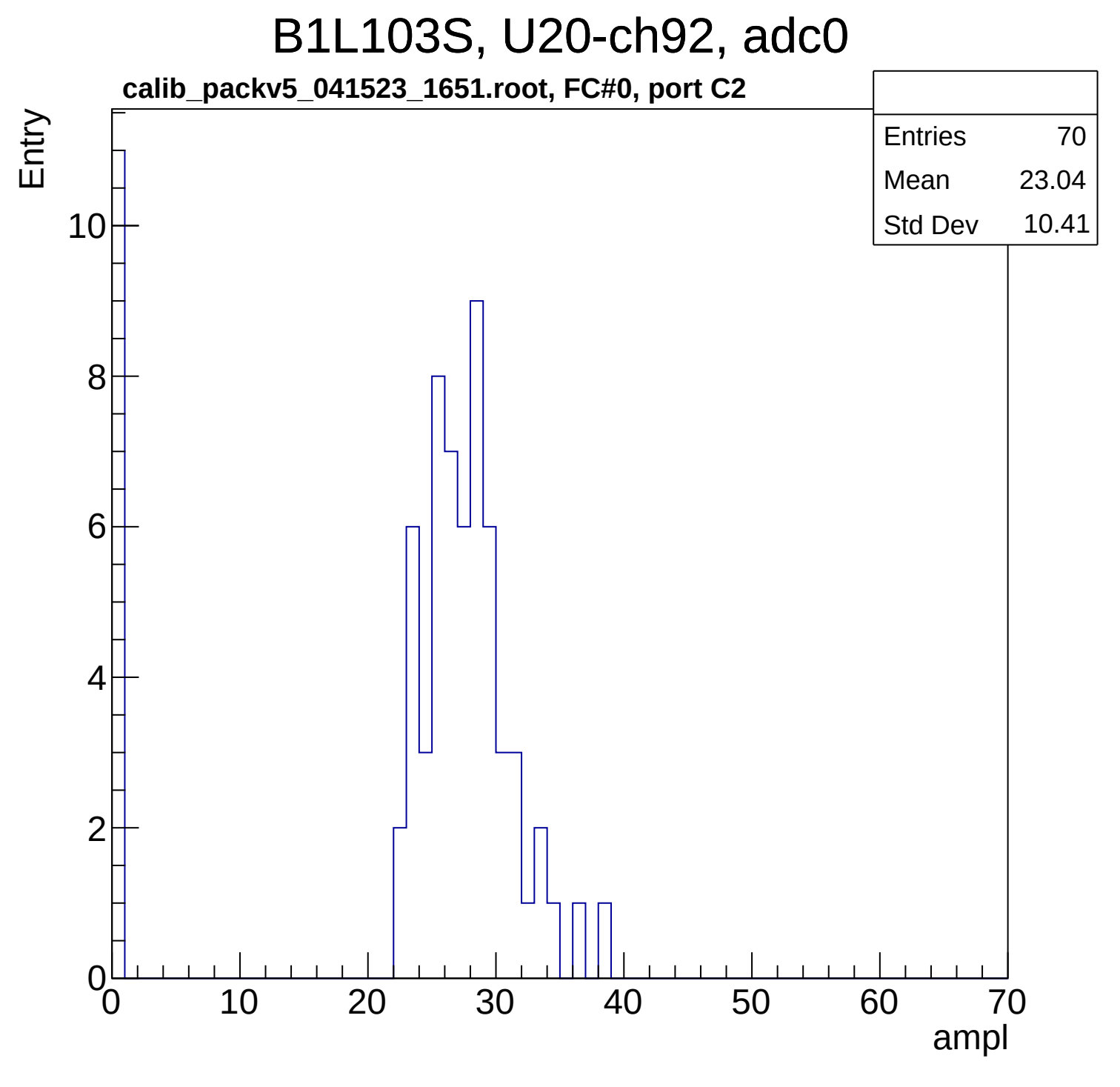
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch92, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 23.04
Std Dev 10.41
Entry
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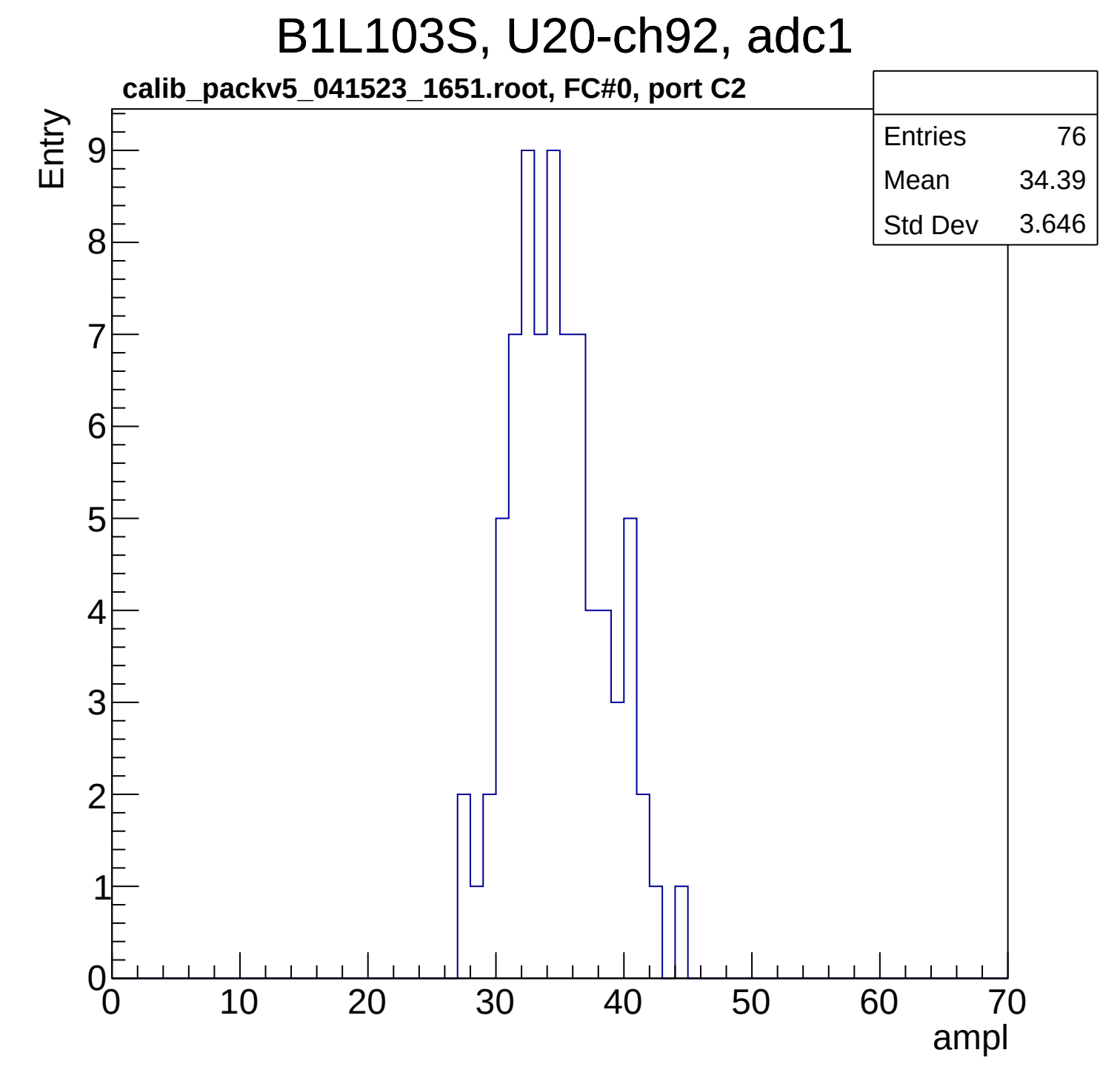
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch92, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 34.39
Std Dev 3.646
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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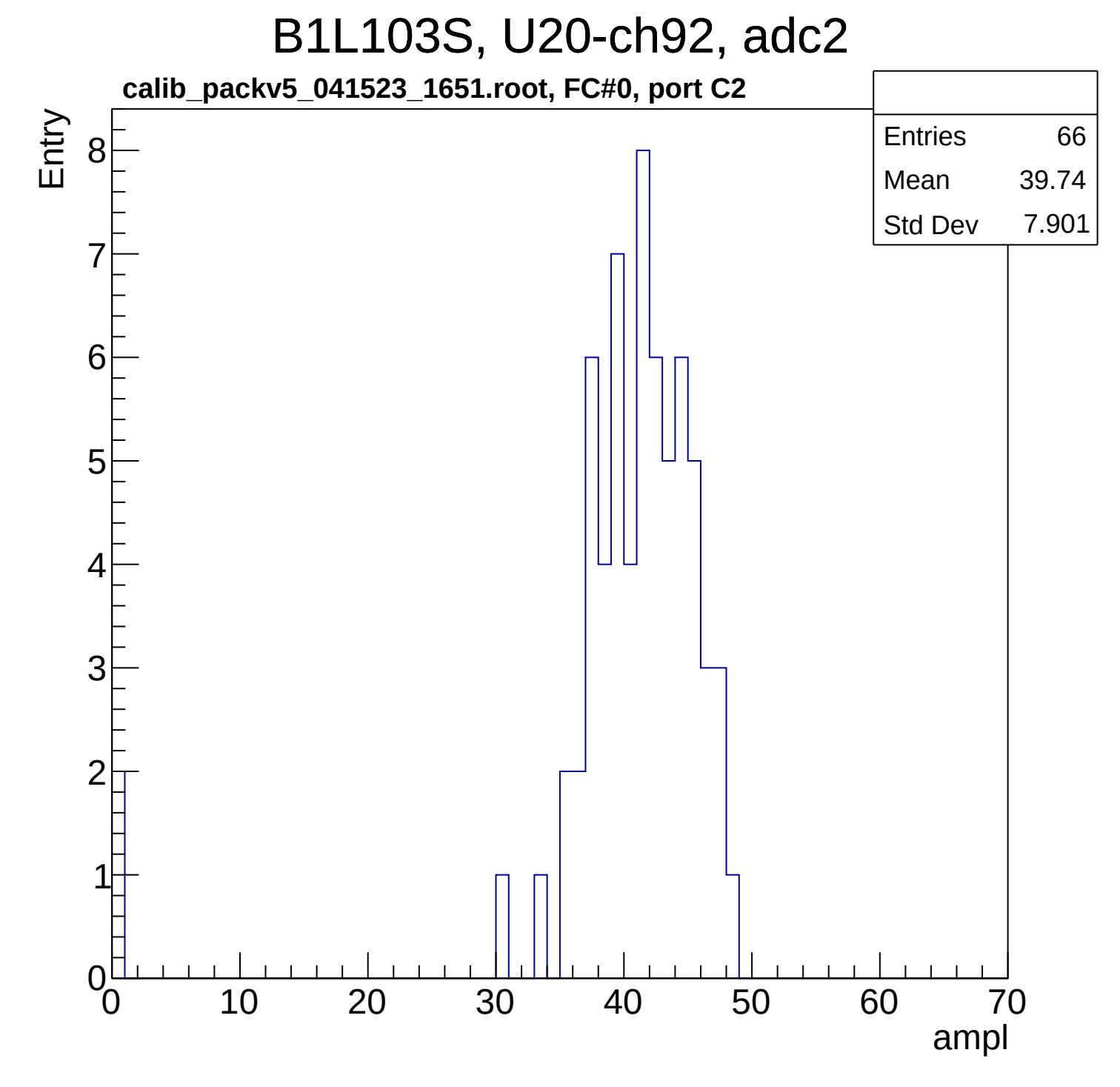
B1L103S, U20-ch92, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 39.74
Std Dev 7.901
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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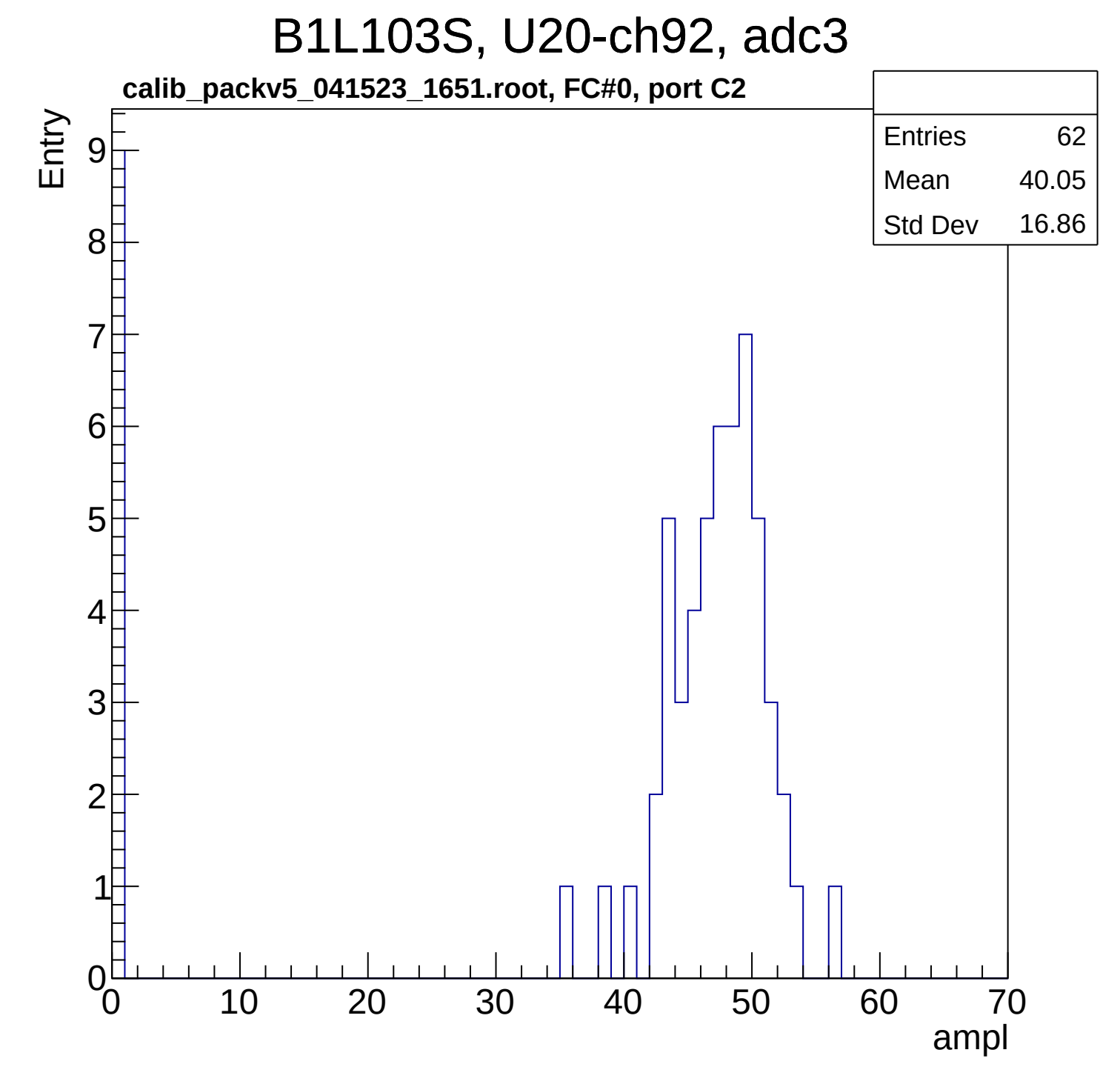
B1L103S, U20-ch92, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 40.05
Std Dev 16.86
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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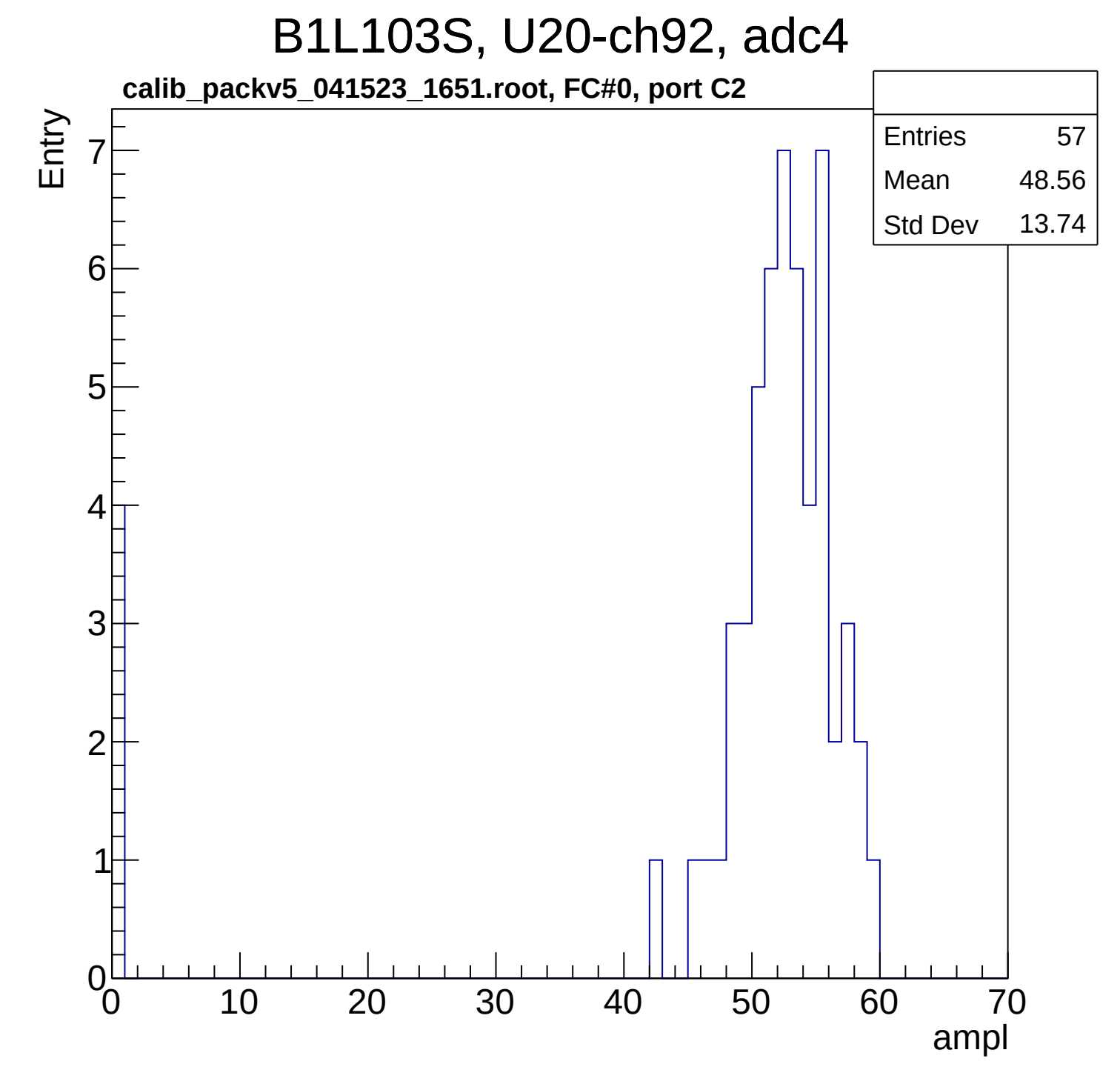
40
50
60
70


B1L103S, U20-ch92, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 48.56
Std Dev 13.74
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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40
50
60
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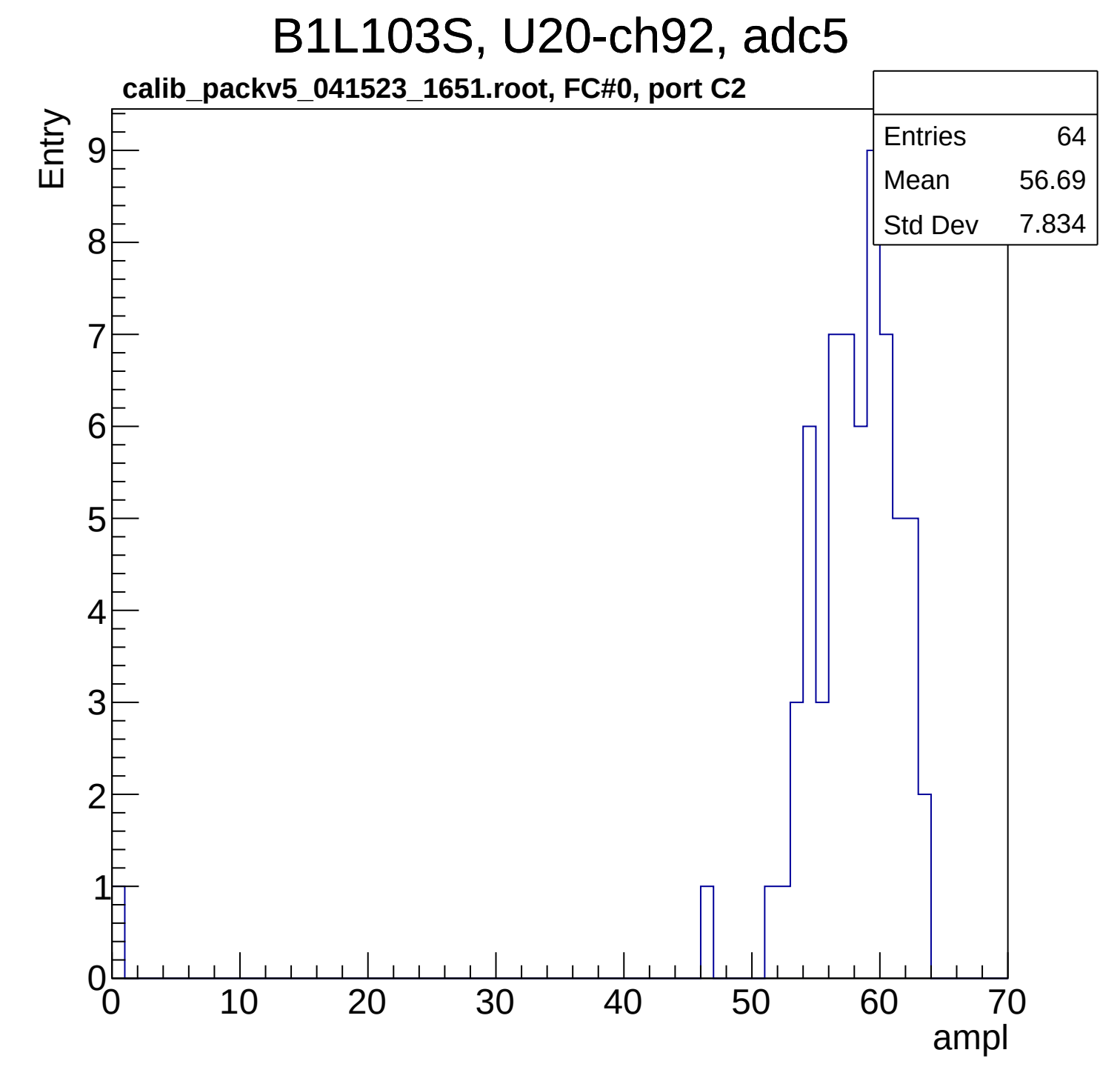
B1L103S, U20-ch92, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 56.69
Std Dev 7.834
Entry
ampl
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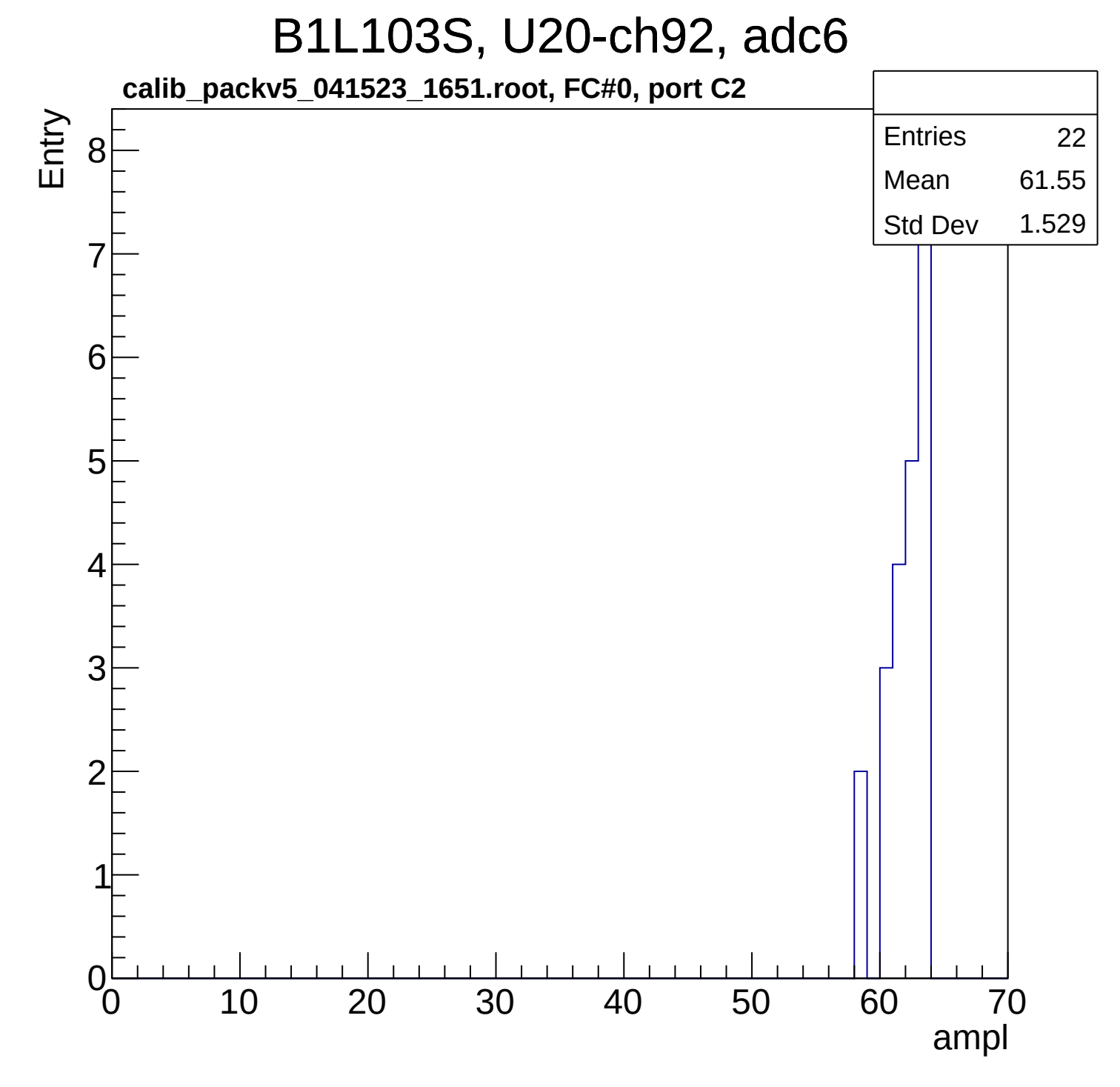
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch92, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 61.55
Std Dev 1.529
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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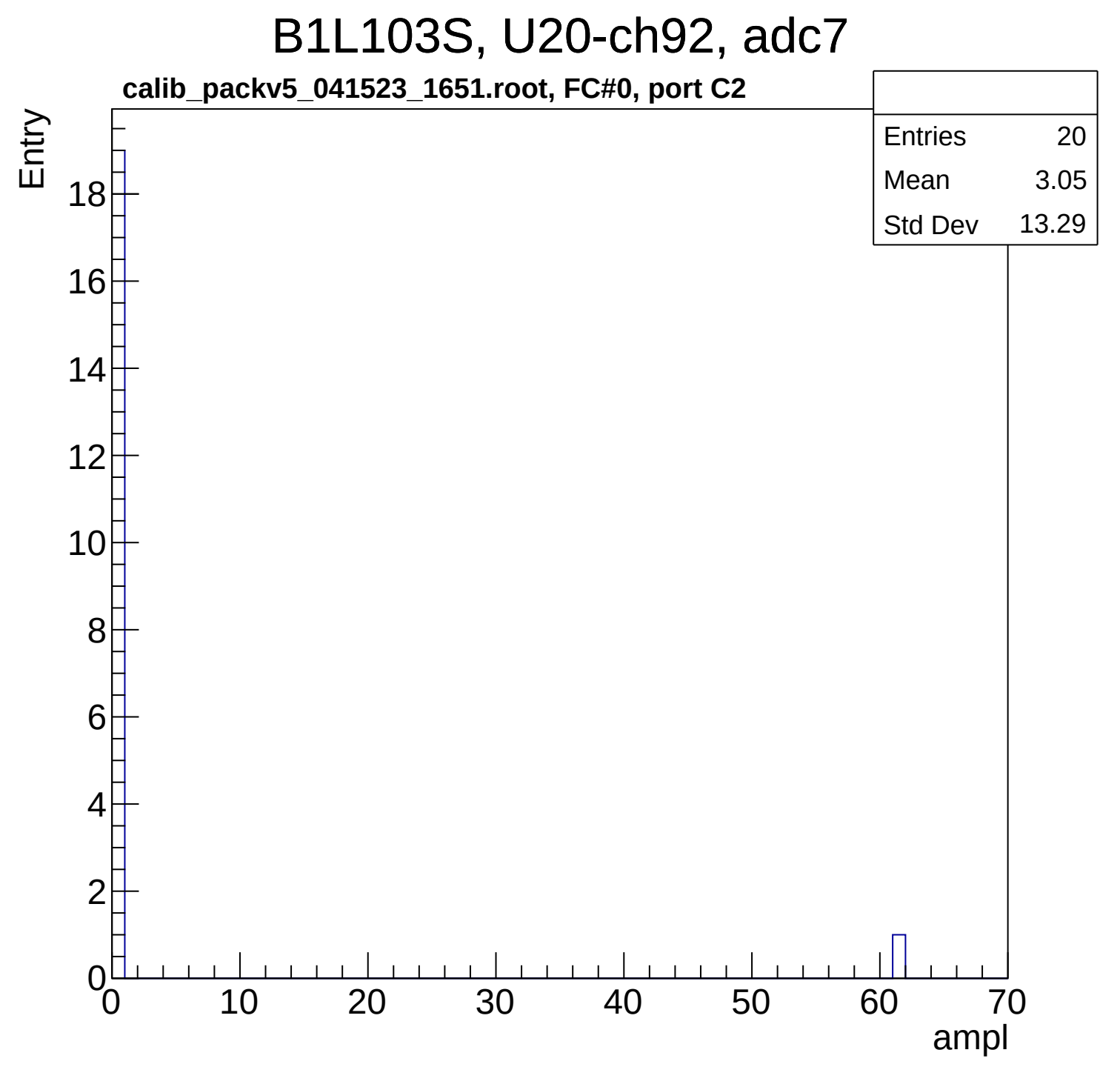
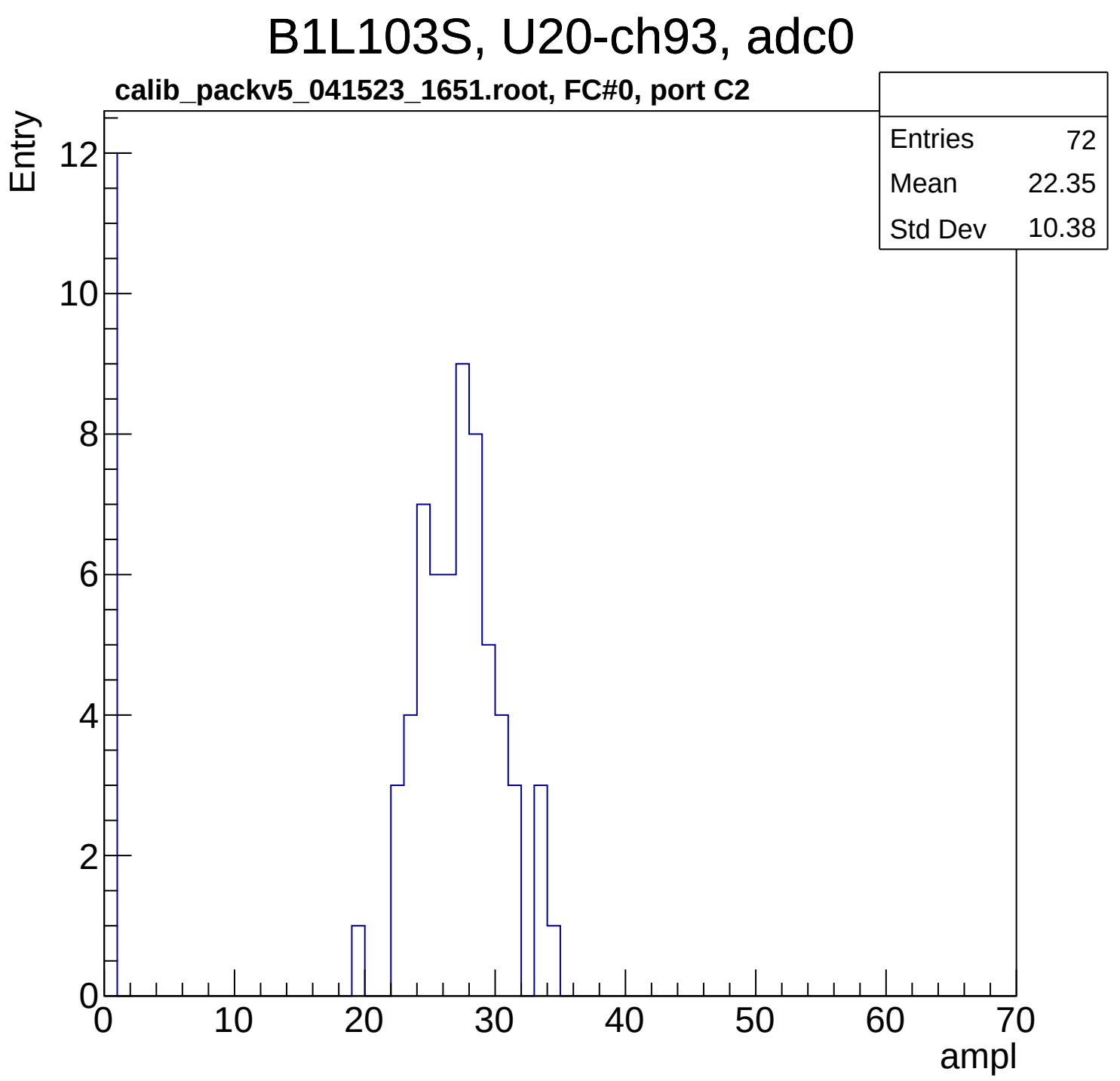
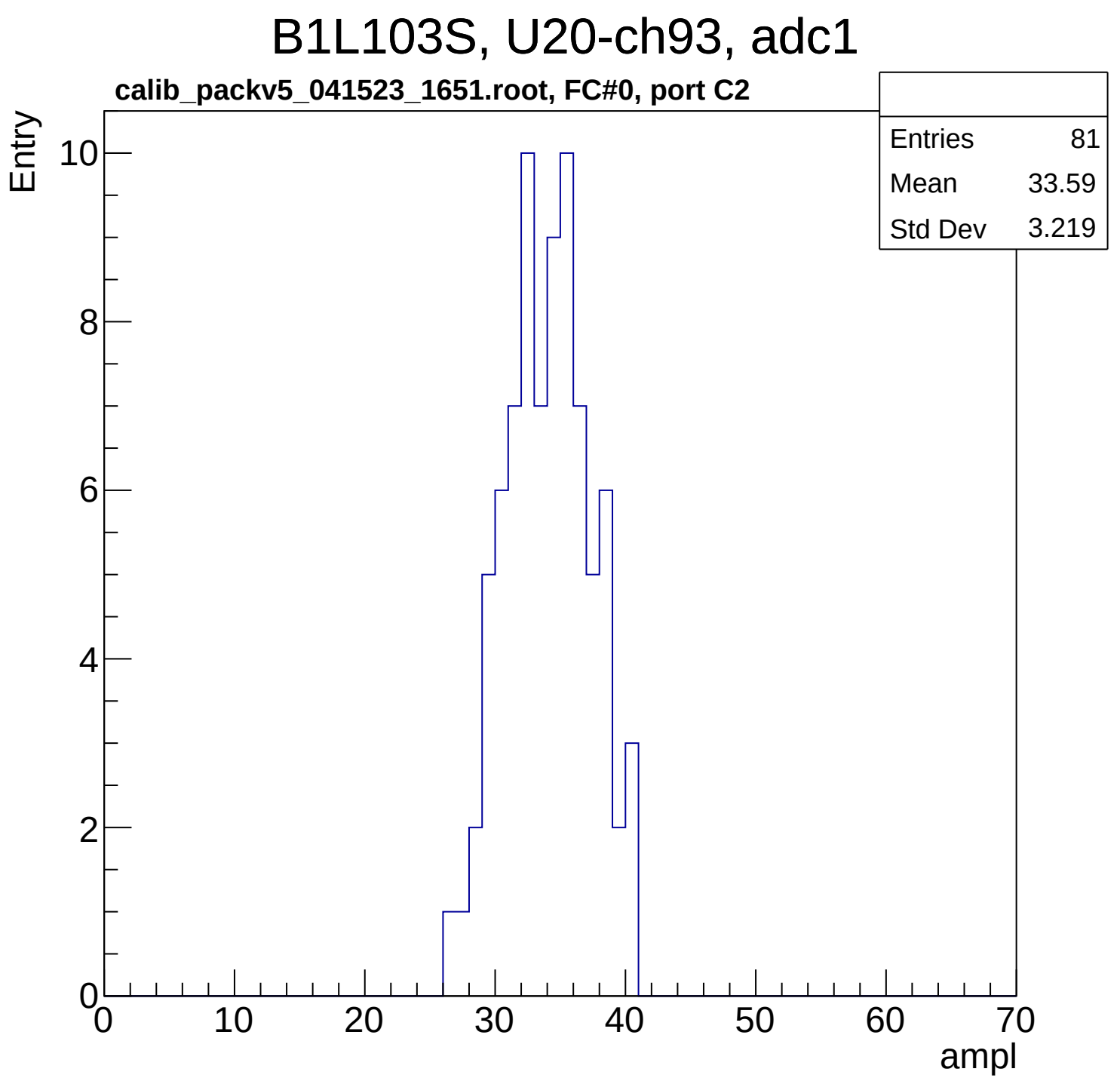

B1L103S, U20-ch92, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.05
Std Dev 13.29
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch93, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 22.35
Std Dev 10.38
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch93, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 33.59
Std Dev 3.219
Entry
0
2
4
6
8
10
0
10
20
30
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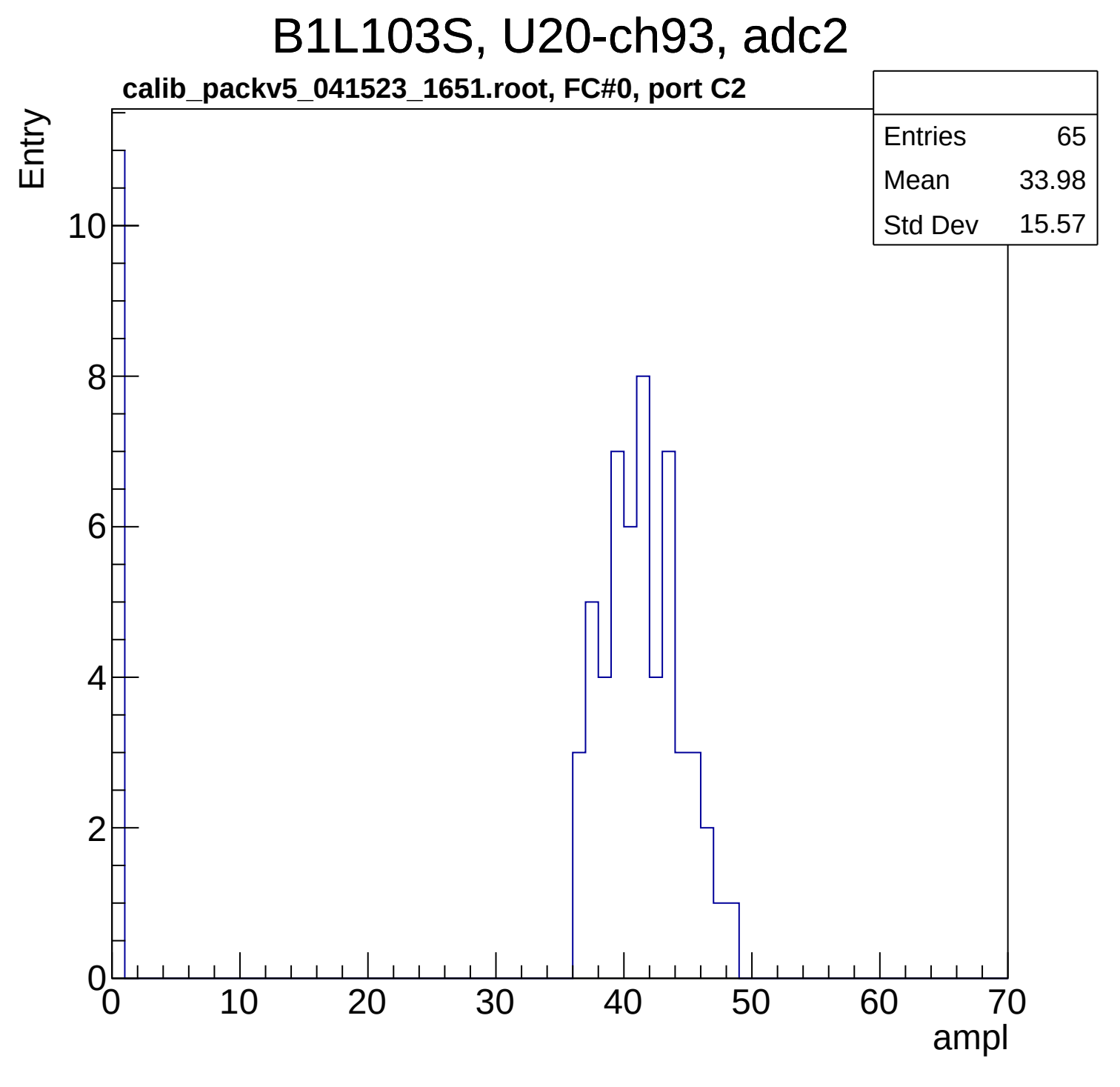
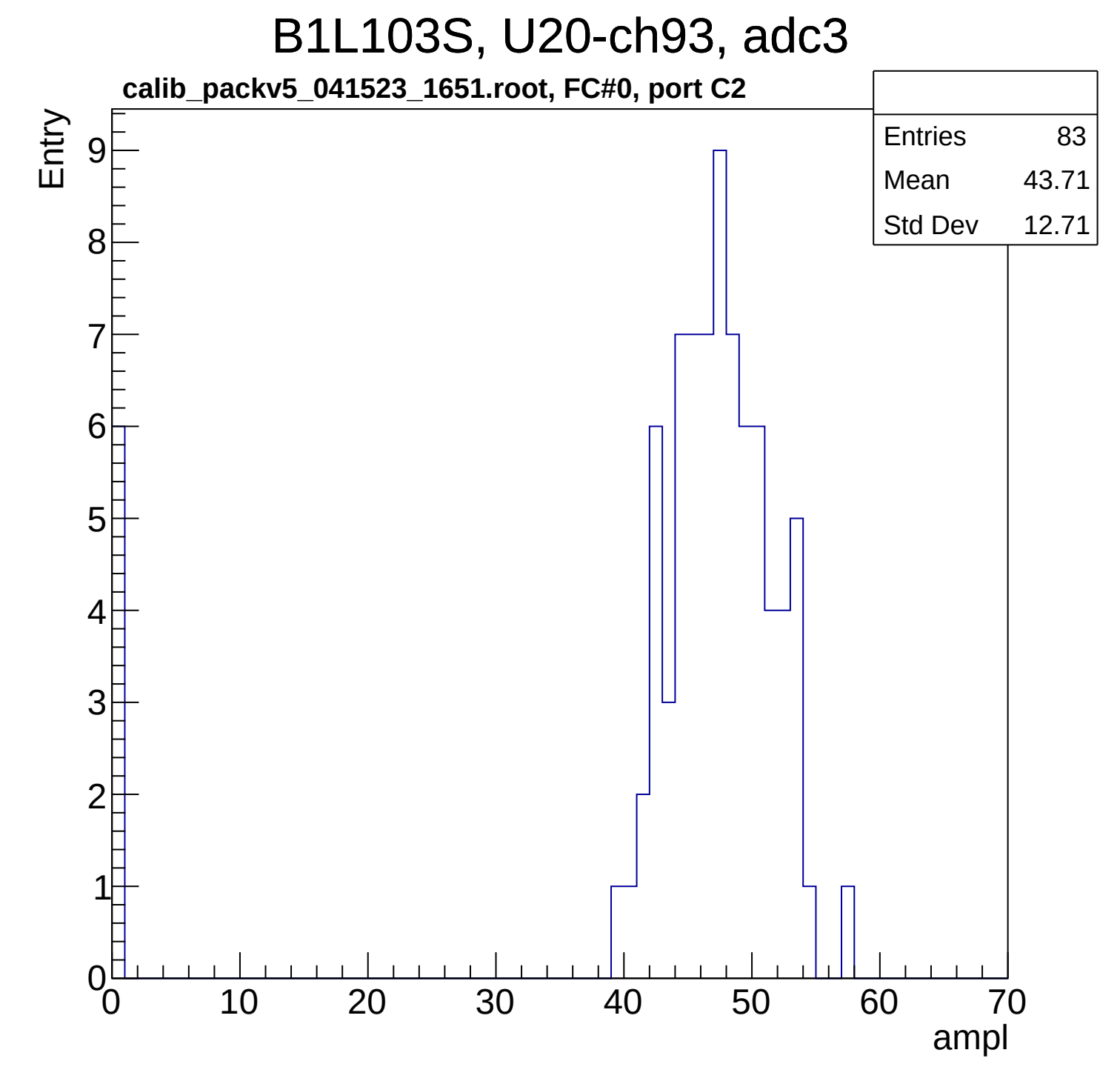
50
60
70
ampl


B1L103S, U20-ch93, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 33.98
Std Dev 15.57
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch93, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 43.71
Std Dev 12.71
Entry
ampl
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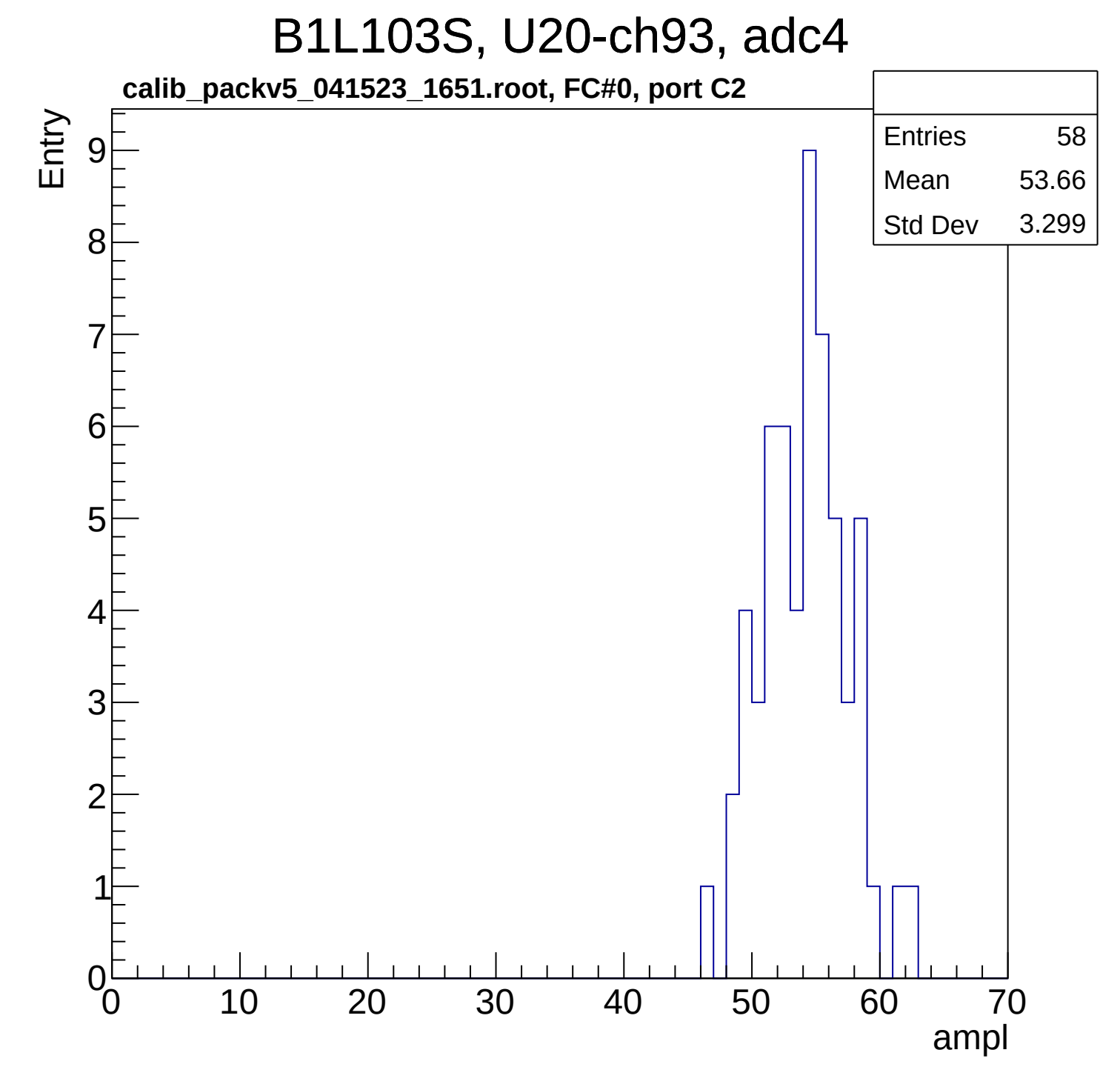
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch93, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 53.66
Std Dev 3.299
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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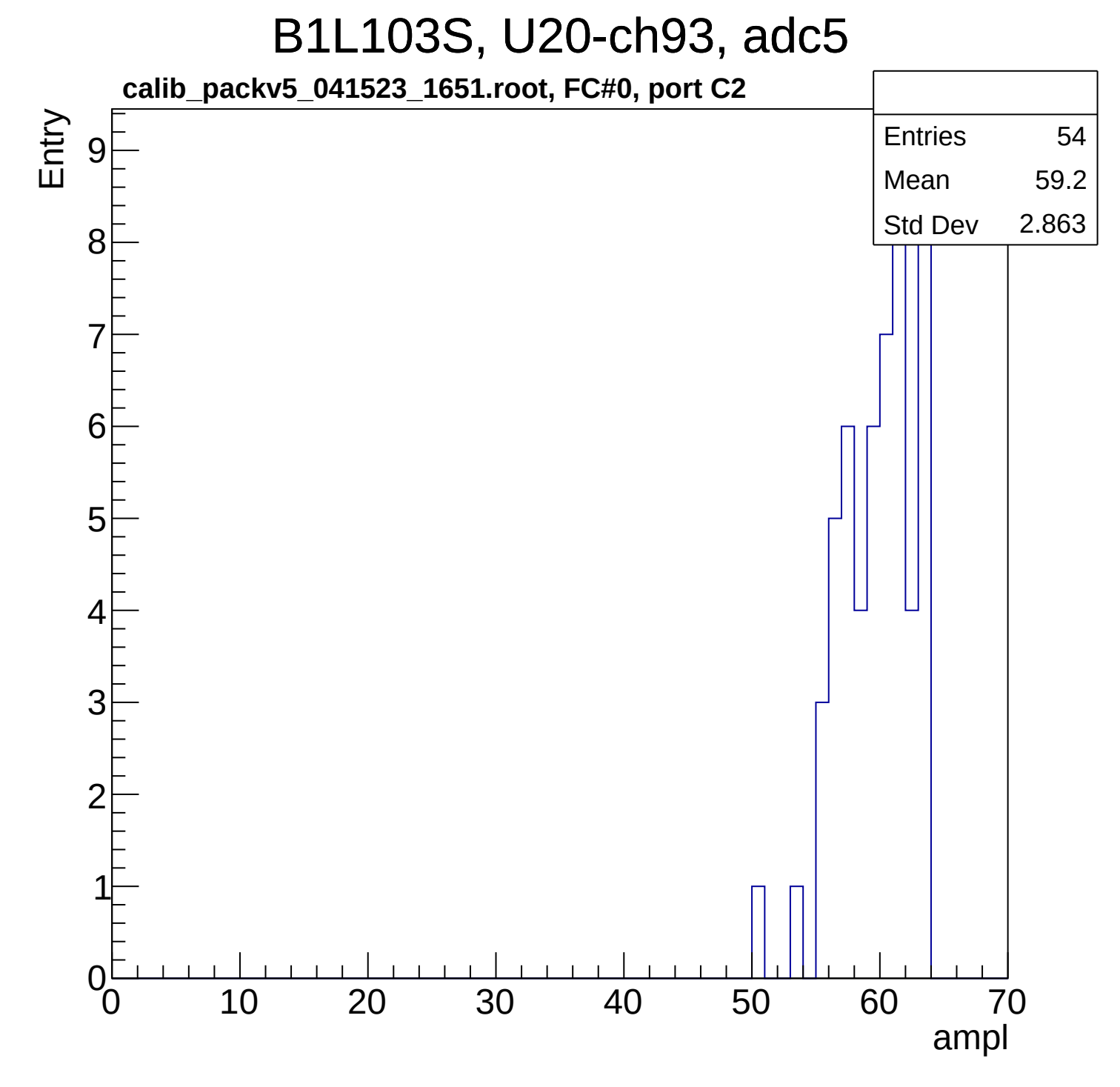
B1L103S, U20-ch93, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 59.2
Std Dev 2.863
Entry
ampl
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3
4
5
6
7
8
9
0
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20
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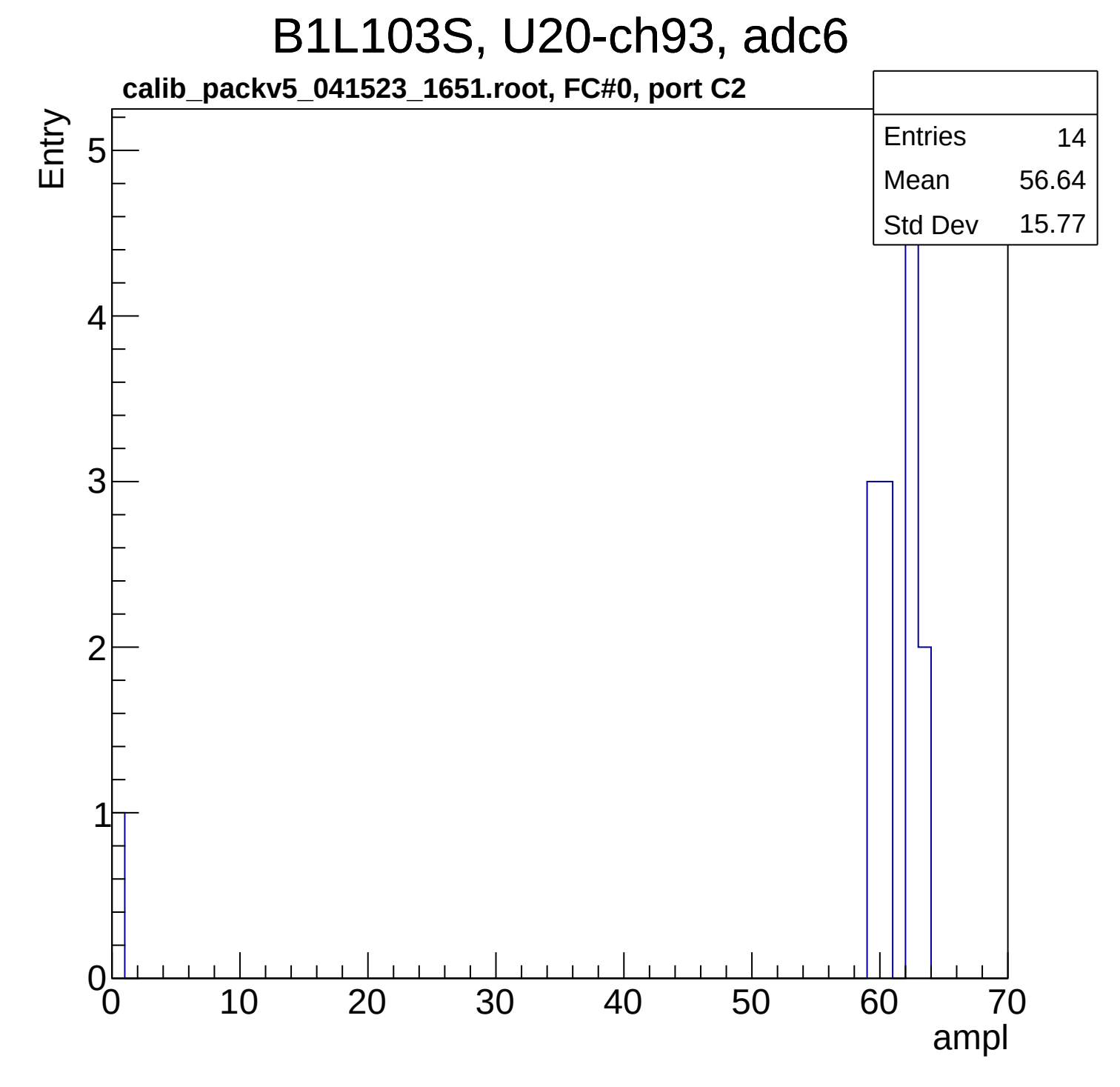
40
50
60
70


B1L103S, U20-ch93, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 56.64
Std Dev 15.77
Entry
0
1
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3
4
5
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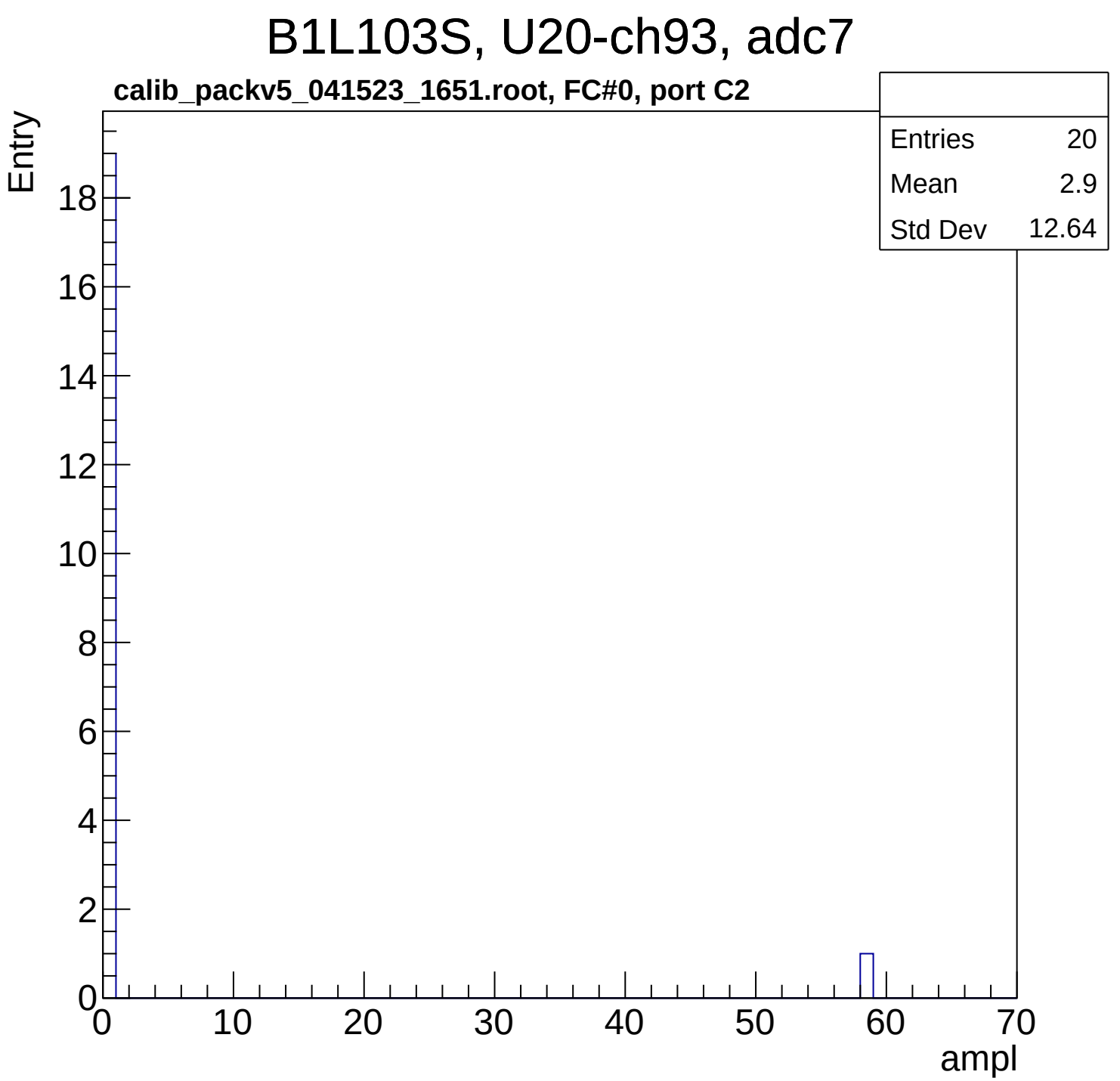
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch93, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 2.9
Std Dev 12.64
Entry
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6
8
10
12
14
16
18
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10
20
30
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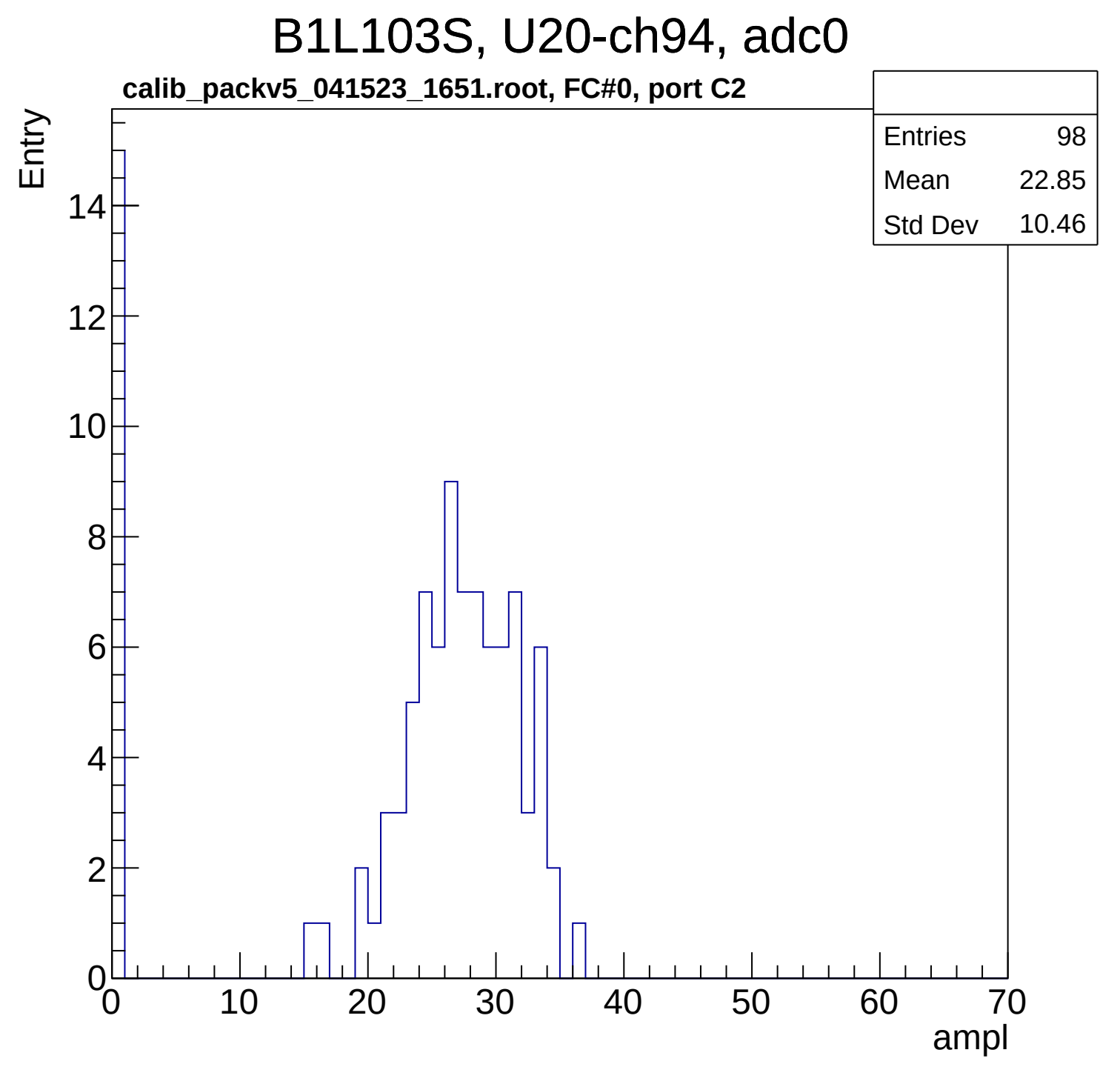
50
60
70
ampl


B1L103S, U20-ch94, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 98
Mean 22.85
Std Dev 10.46
Entry
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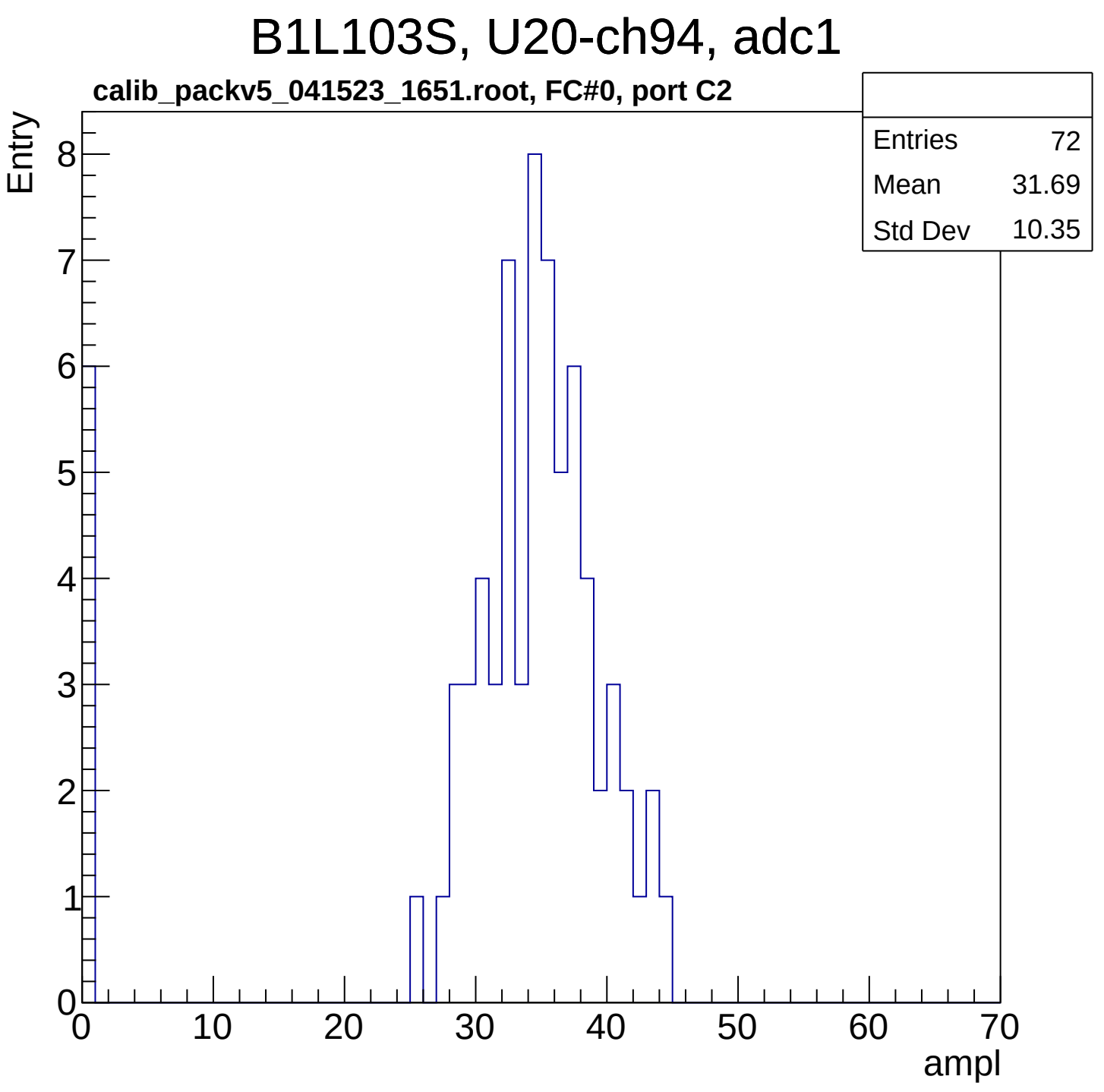
70
ampl


B1L103S, U20-ch94, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 31.69
Std Dev 10.35
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
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60
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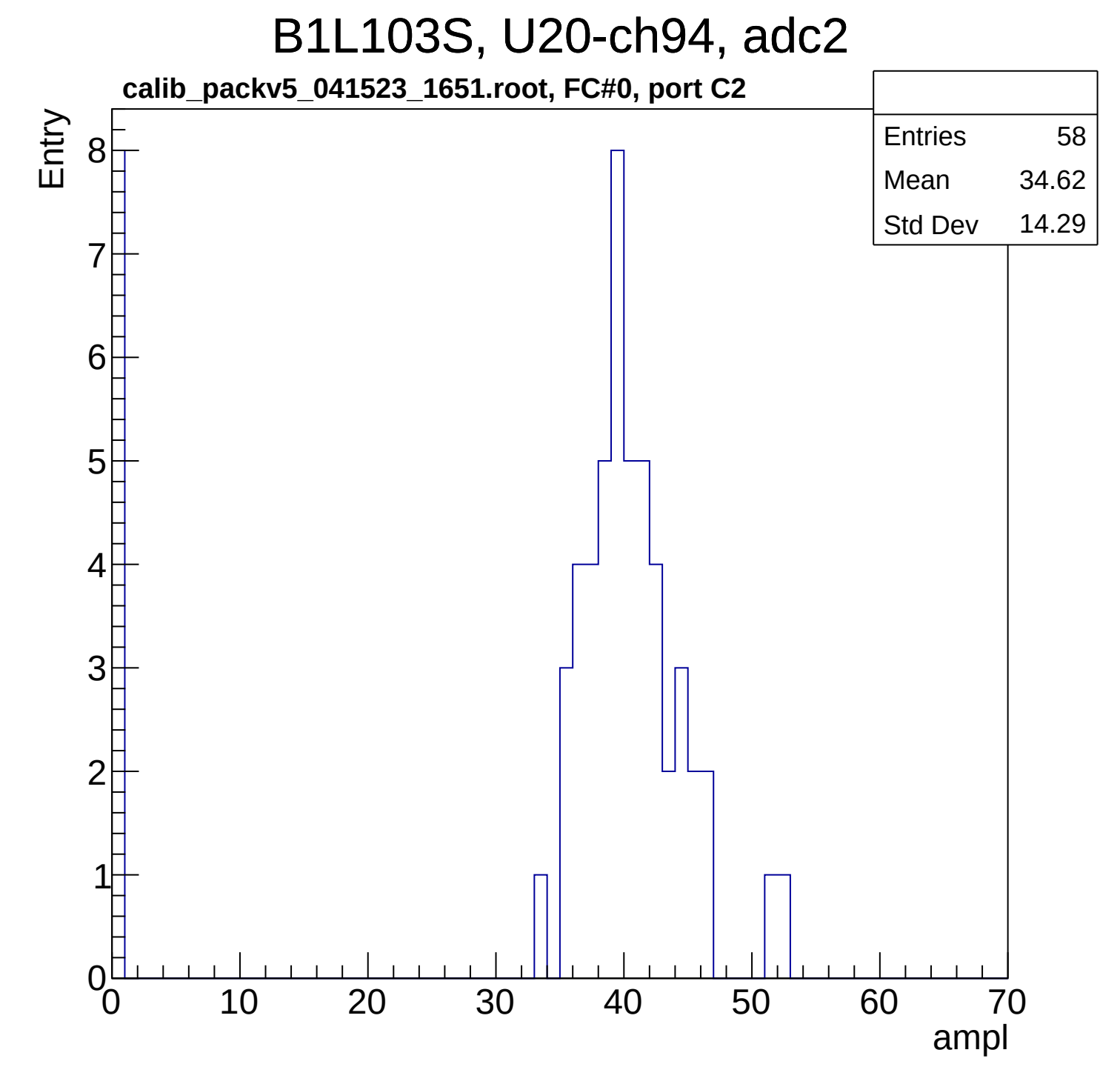
B1L103S, U20-ch94, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 34.62
Std Dev 14.29
Entry
ampl
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2
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5
6
7
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0
10
20
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40
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60
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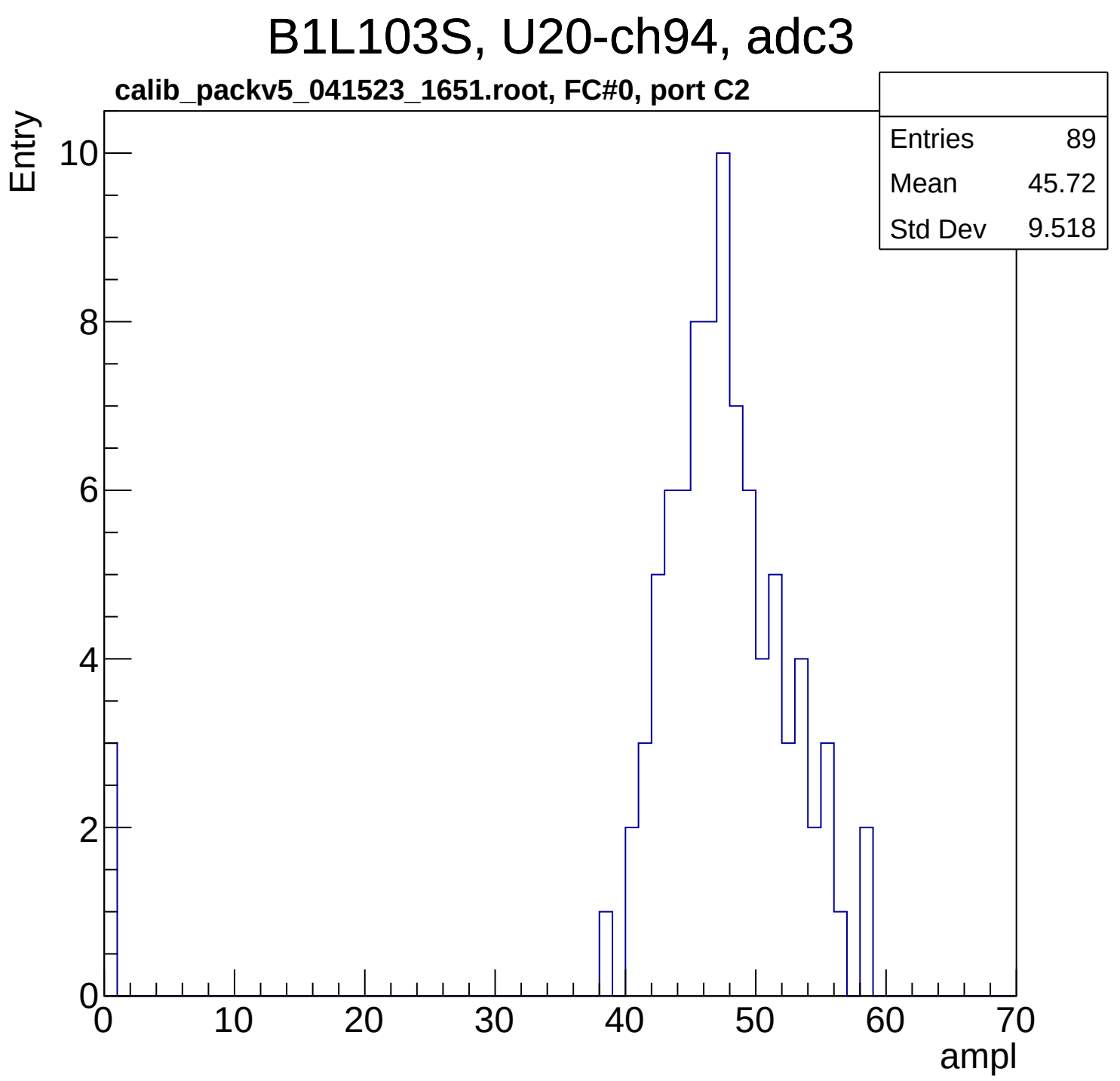
B1L103S, U20-ch94, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 45.72
Std Dev 9.518
Entry
ampl
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4
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8
10
0
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20
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40
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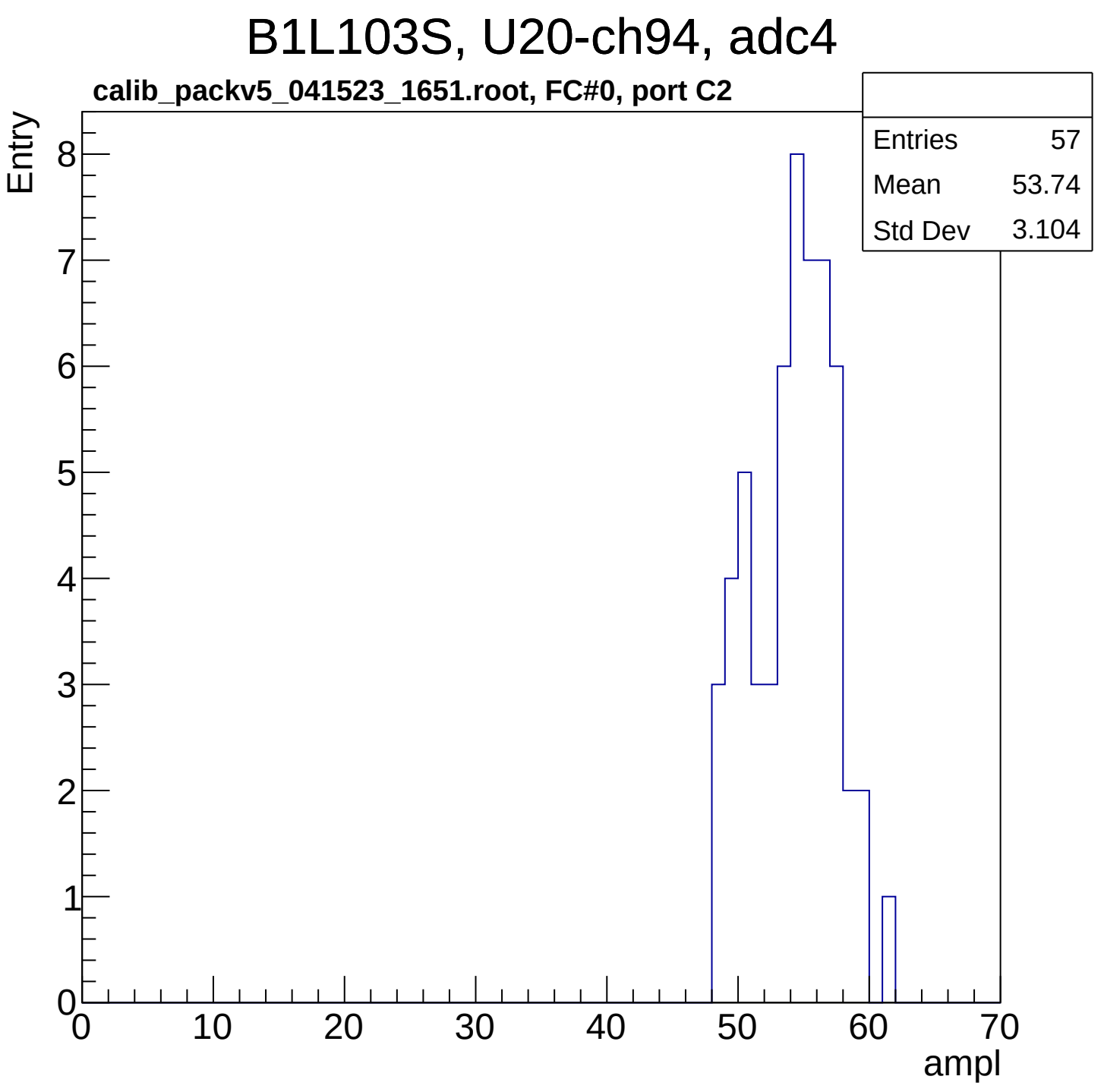
60
70


B1L103S, U20-ch94, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 53.74
Std Dev 3.104
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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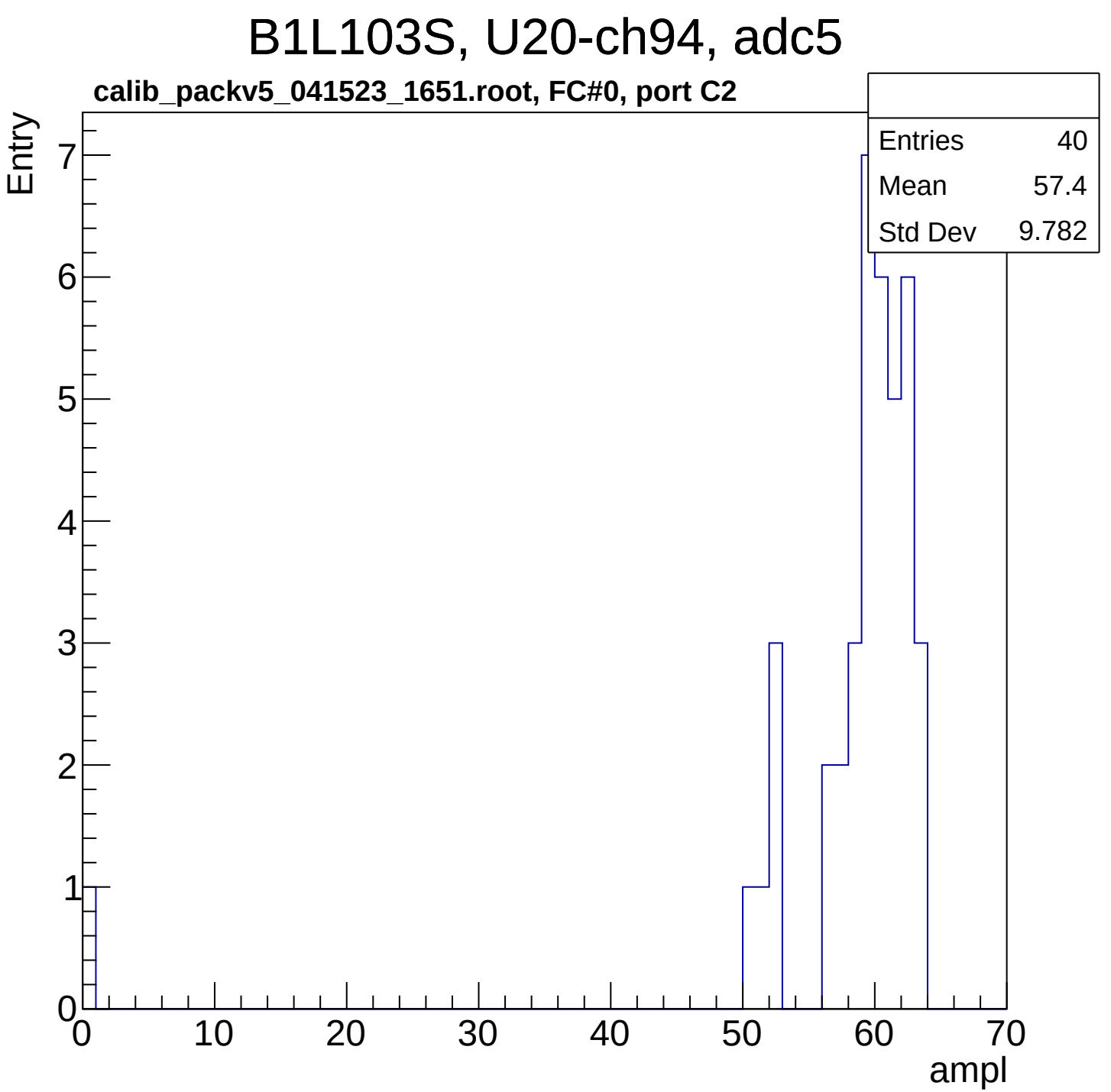
40
50
60
70


B1L103S, U20-ch94, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 57.4
Std Dev 9.782
Entry
ampl
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1
2
3
4
5
6
7
0
10
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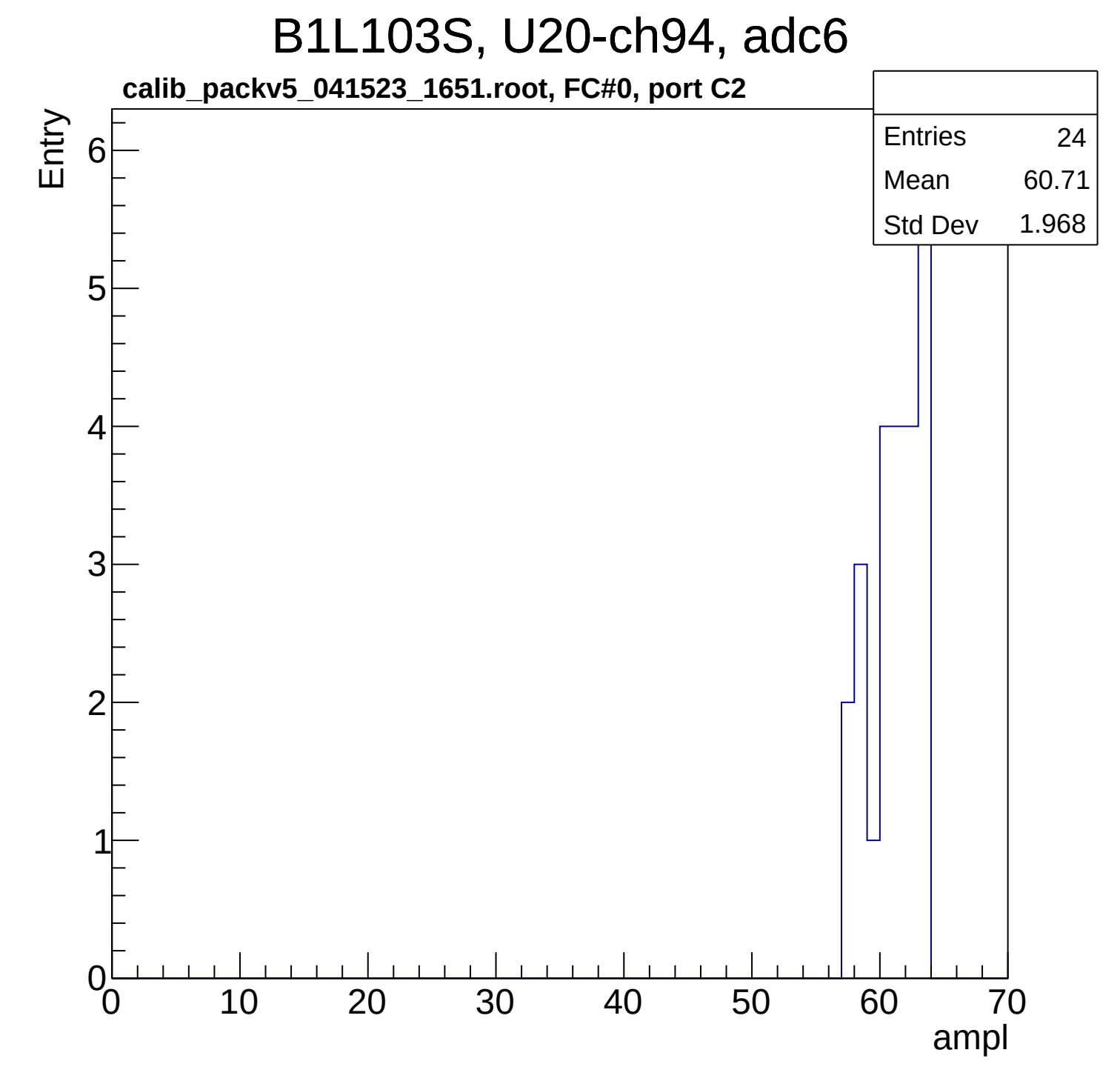
60
70


B1L103S, U20-ch94, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 60.71
Std Dev 1.968
Entry
ampl
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3
4
5
6
0
10
20
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60
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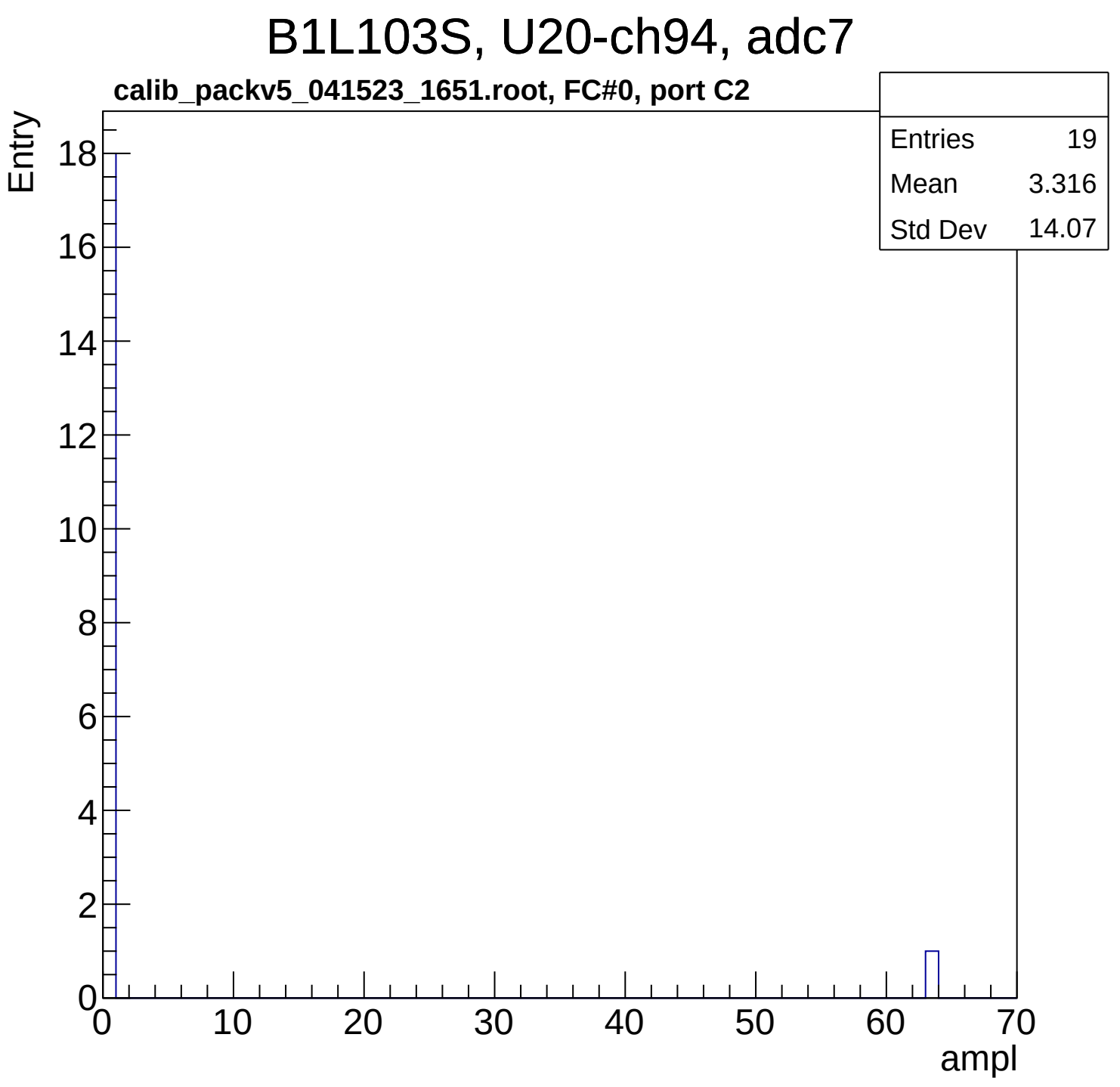
B1L103S, U20-ch94, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.316
Std Dev 14.07
Entry
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6
8
10
12
14
16
18
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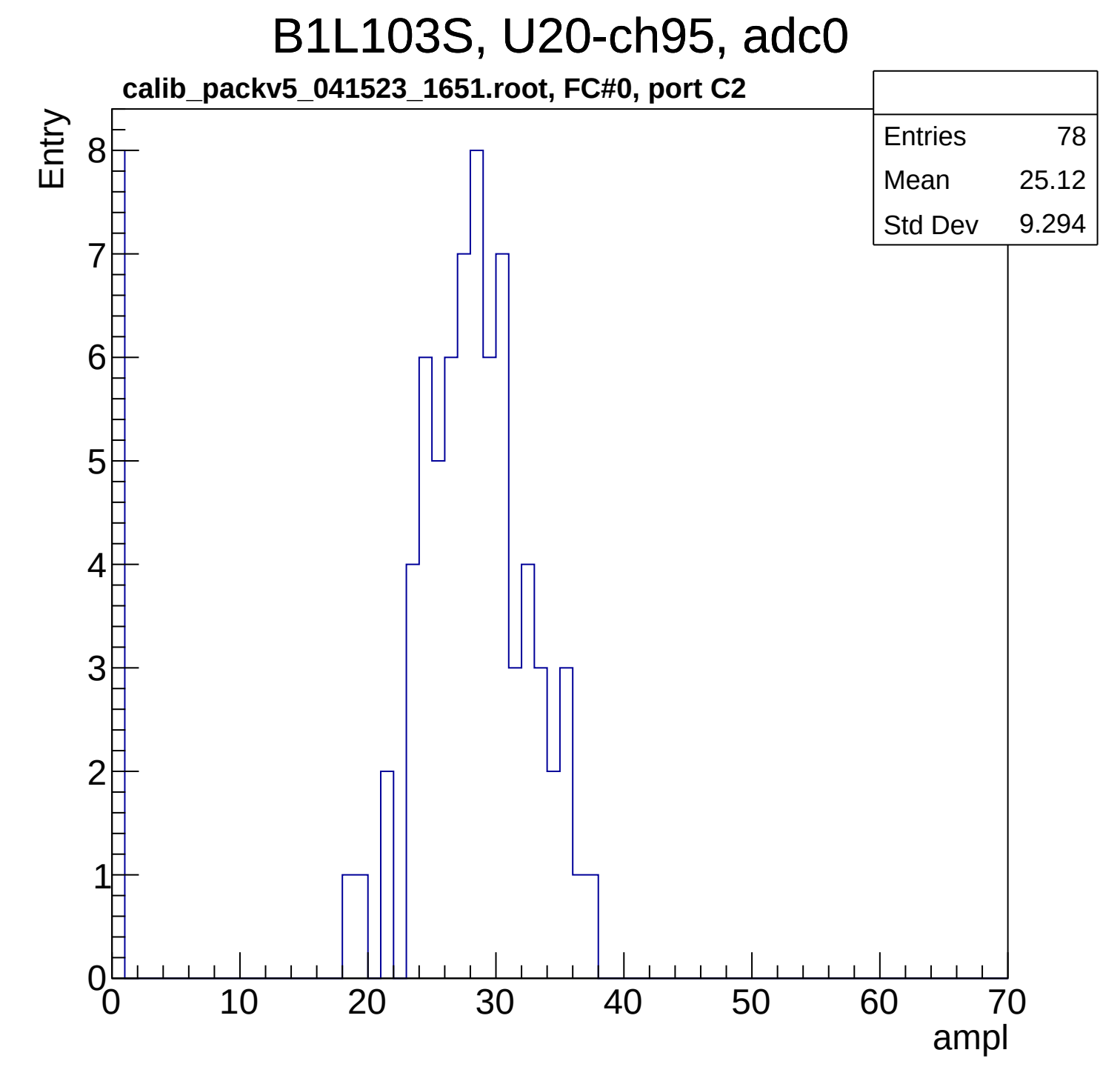
70
ampl


B1L103S, U20-ch95, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 25.12
Std Dev 9.294
Entry
ampl
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5
6
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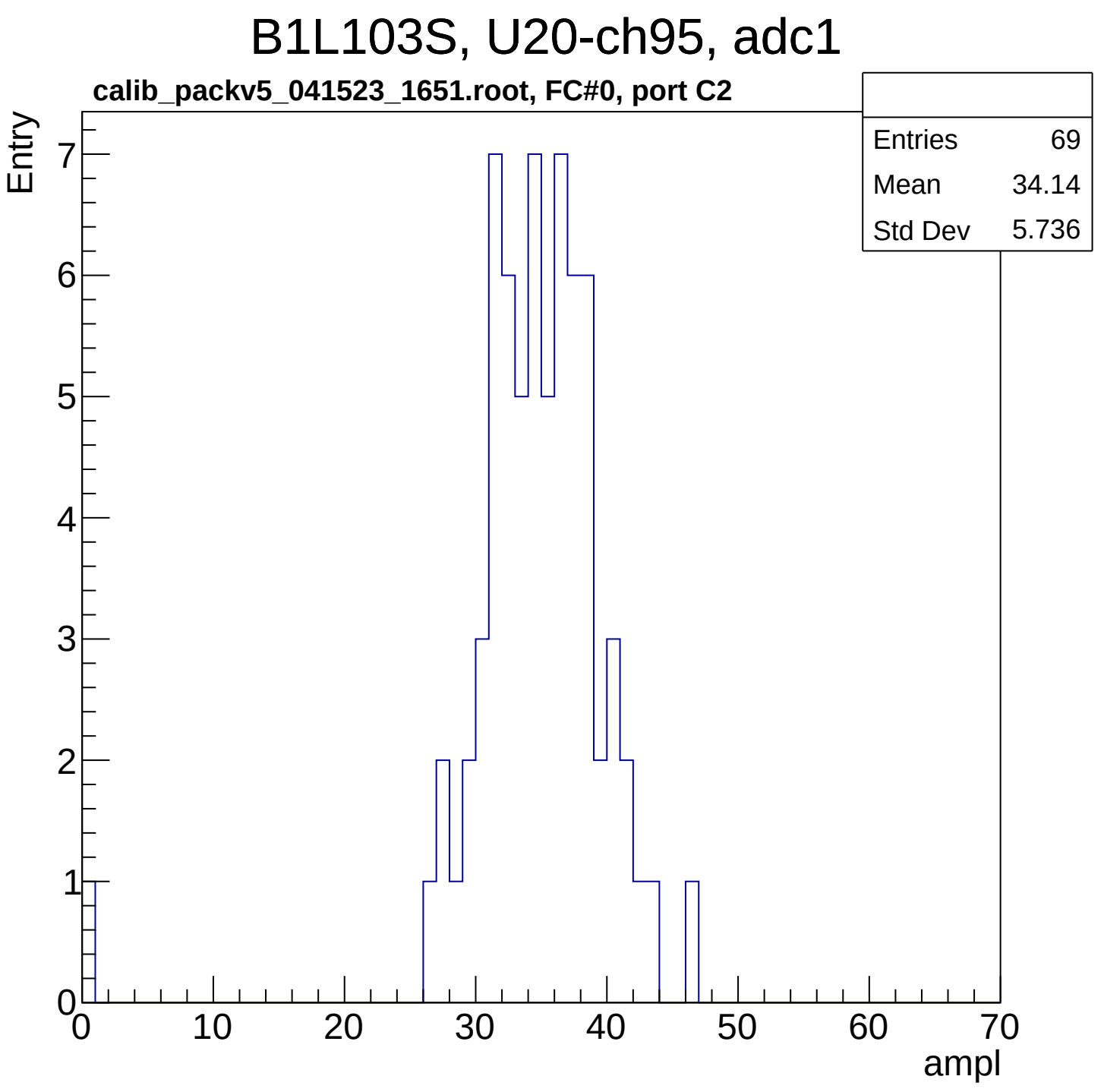
70


B1L103S, U20-ch95, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 34.14
Std Dev 5.736
Entry
ampl
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2
3
4
5
6
7
0
10
20
30
40
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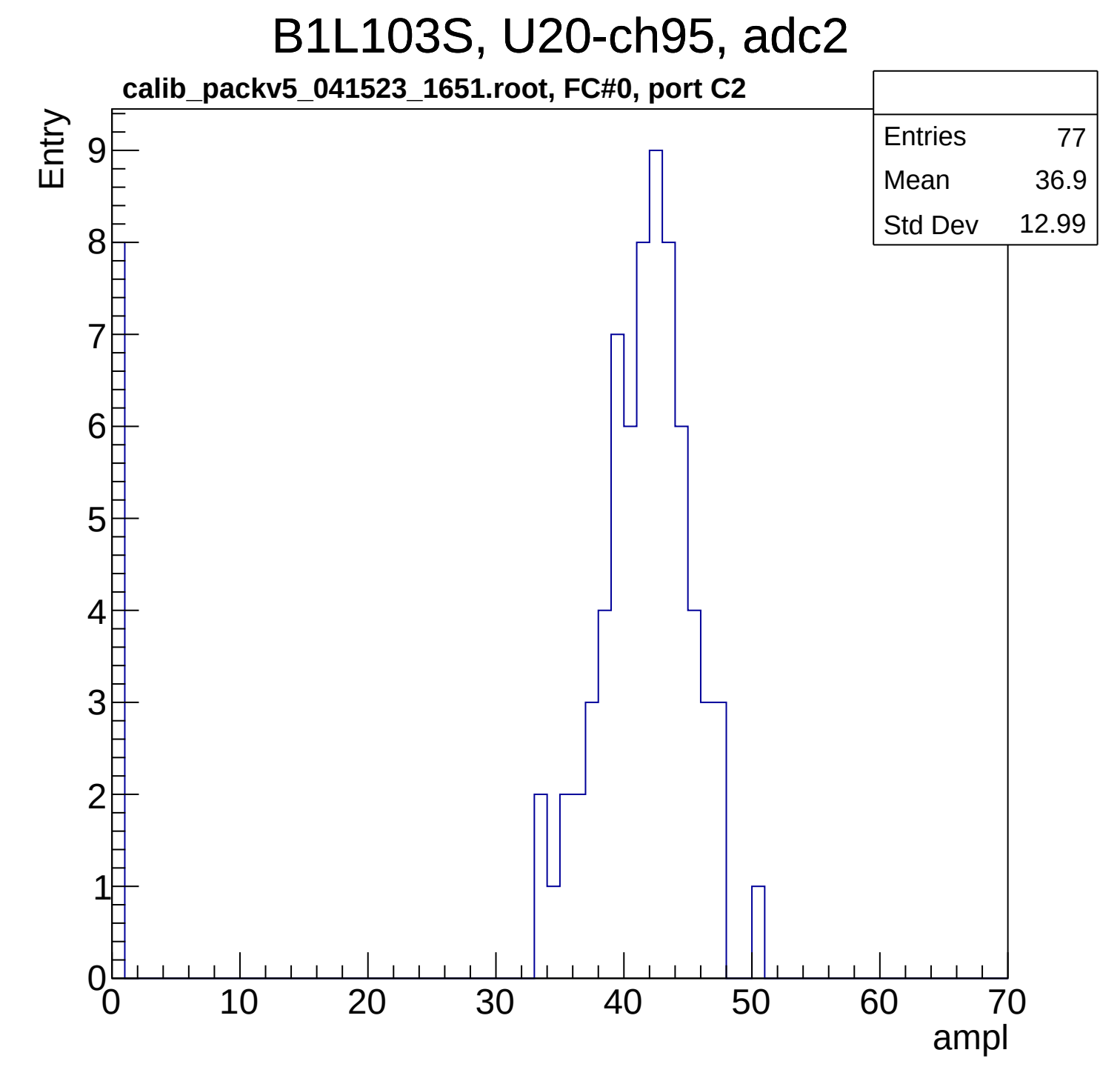
70


B1L103S, U20-ch95, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 36.9
Std Dev 12.99
Entry
ampl
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2
3
4
5
6
7
8
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60
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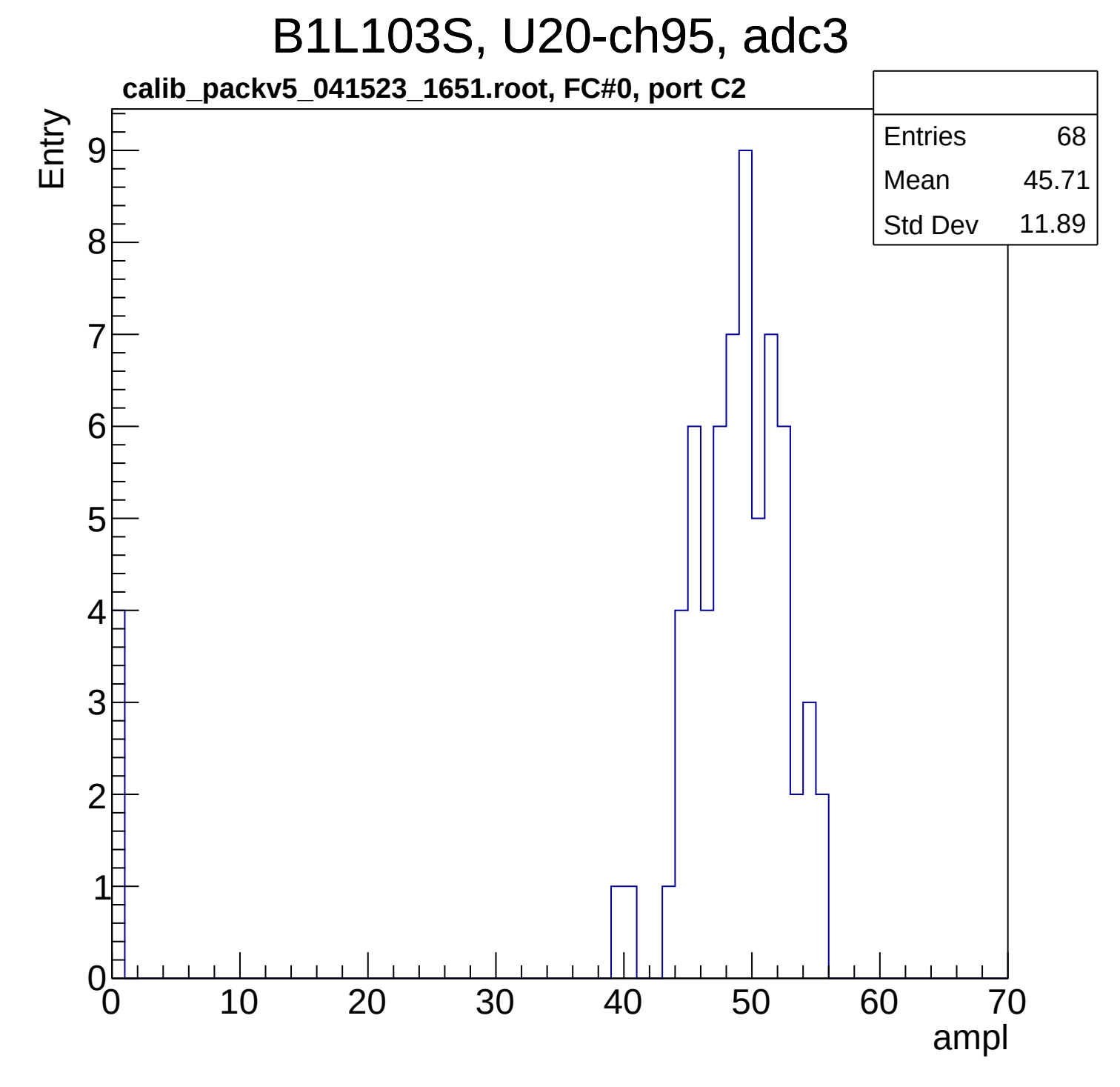
B1L103S, U20-ch95, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 45.71
Std Dev 11.89
Entry
ampl
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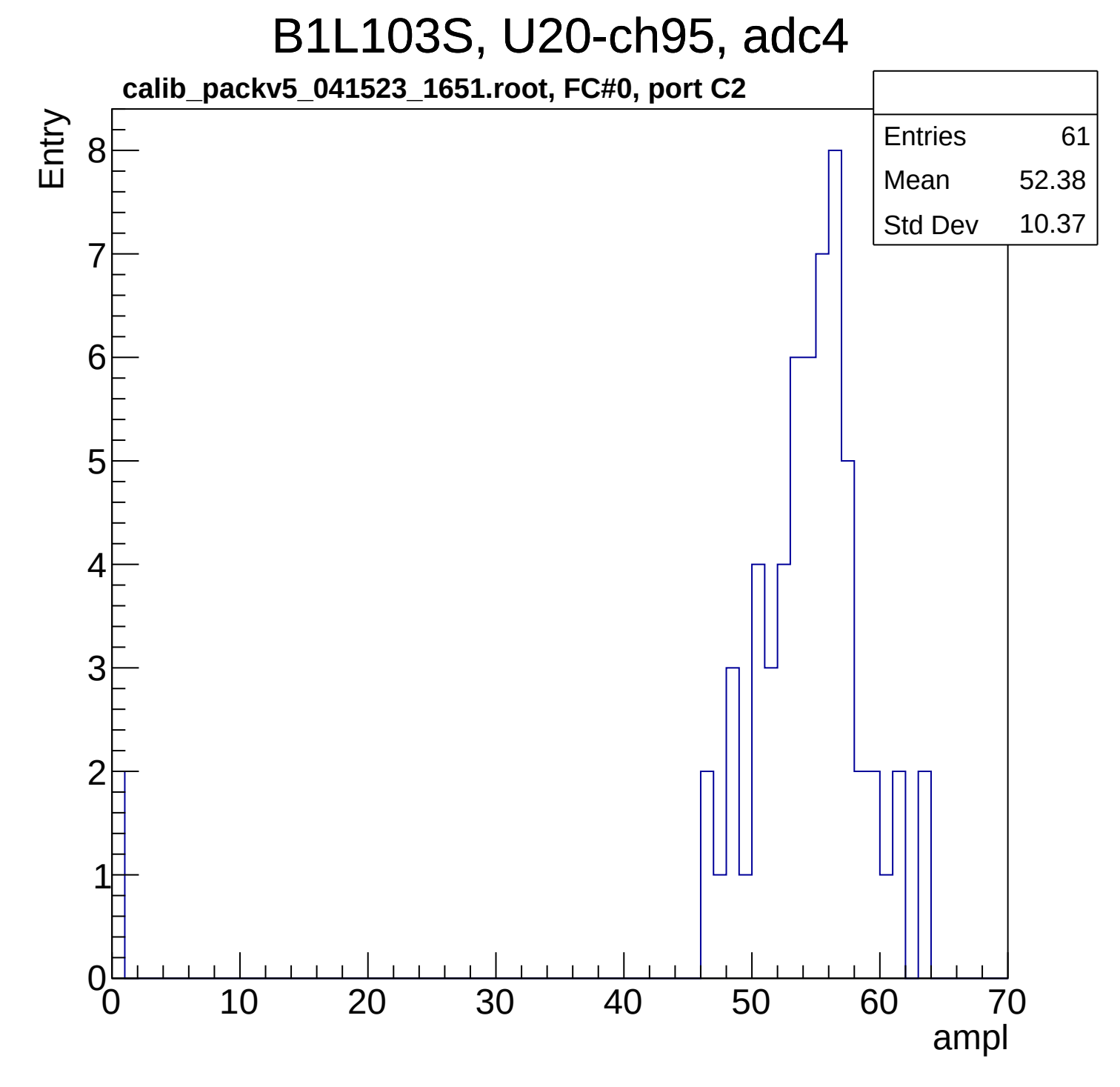
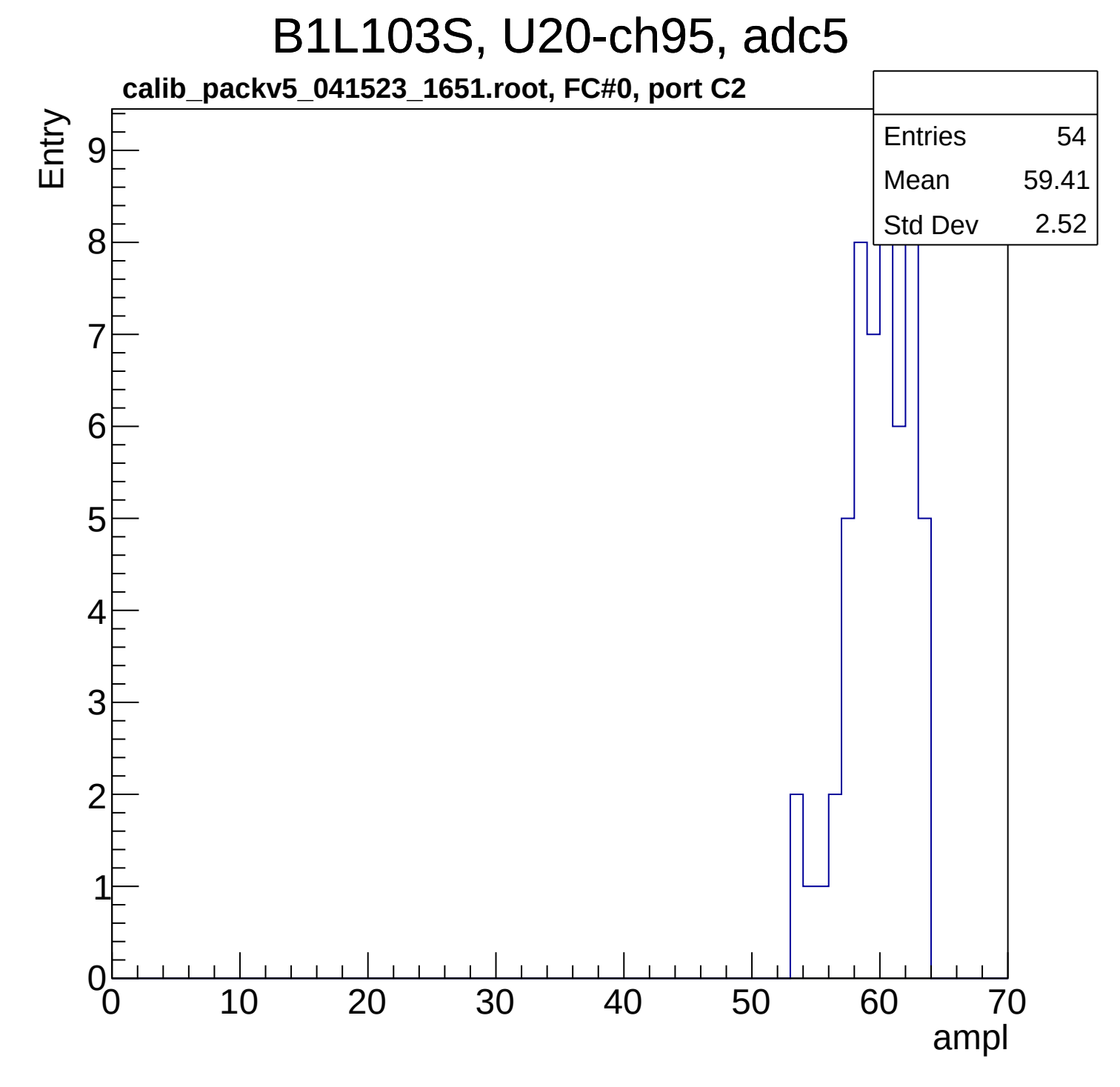
7
8
9


B1L103S, U20-ch95, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 52.38
Std Dev 10.37
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch95, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 59.41
Std Dev 2.52
Entry
ampl
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10
20
30
40
50
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1
2
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4
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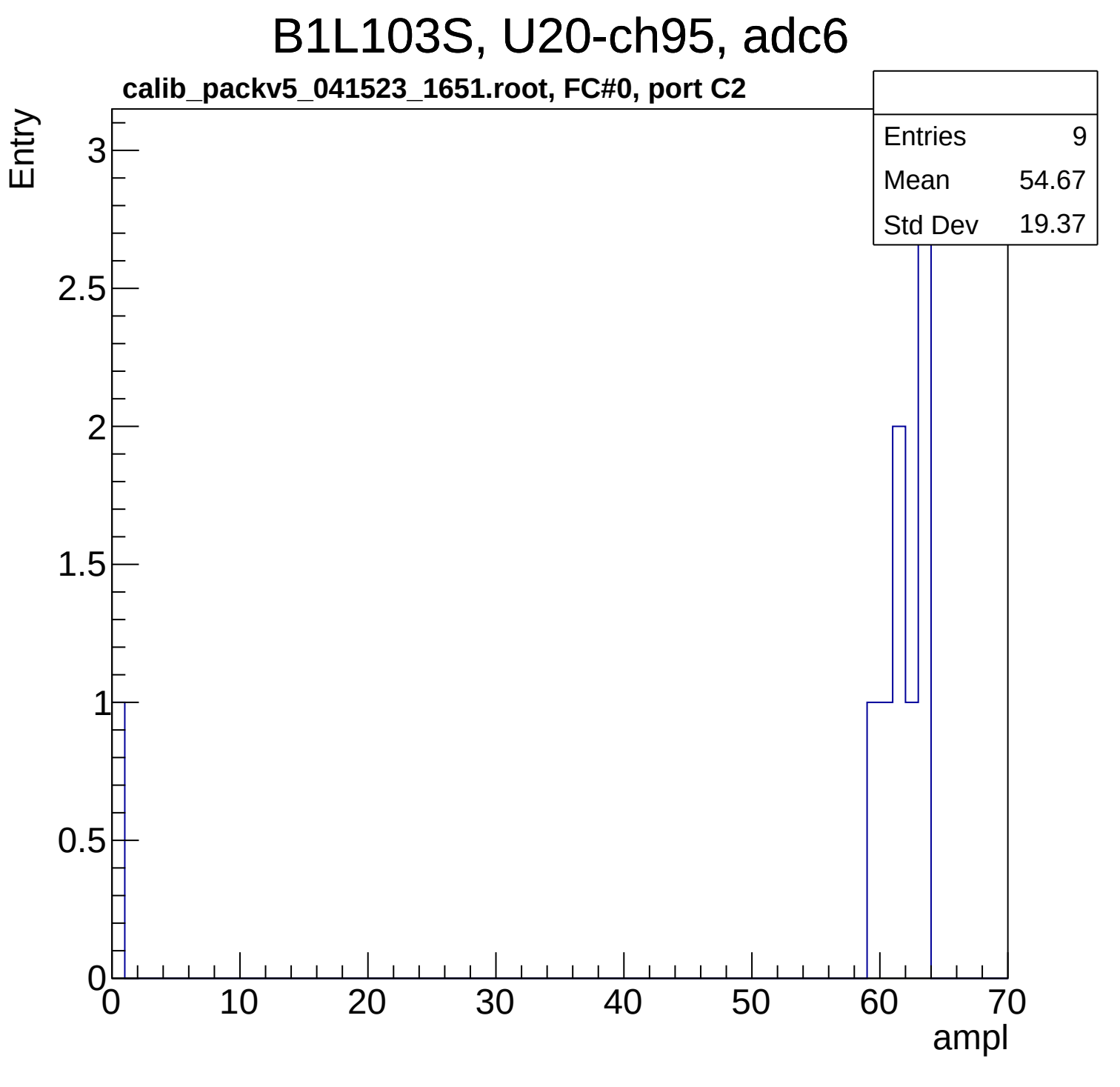
6
7
8
9


B1L103S, U20-ch95, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 54.67
Std Dev 19.37
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
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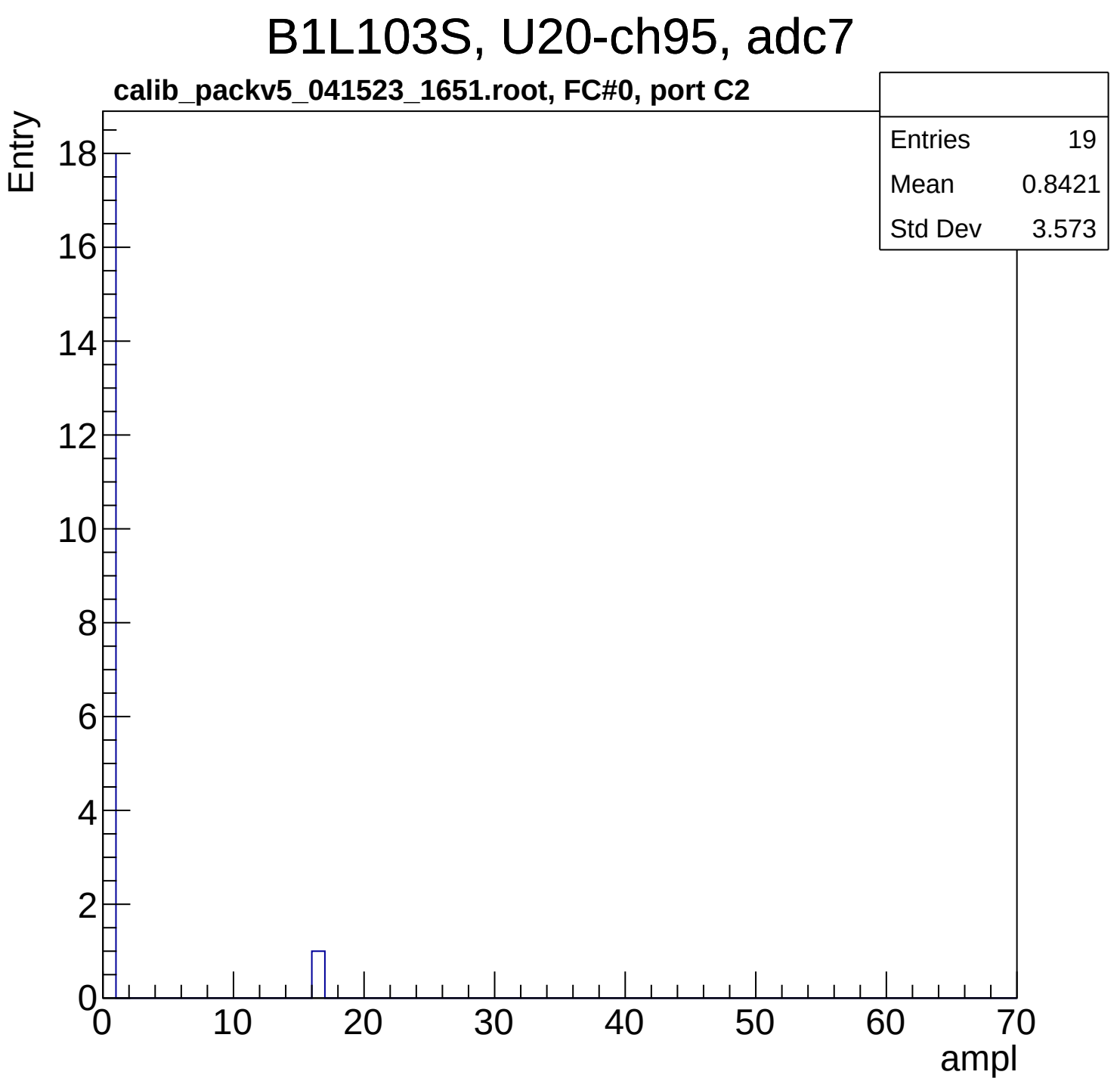
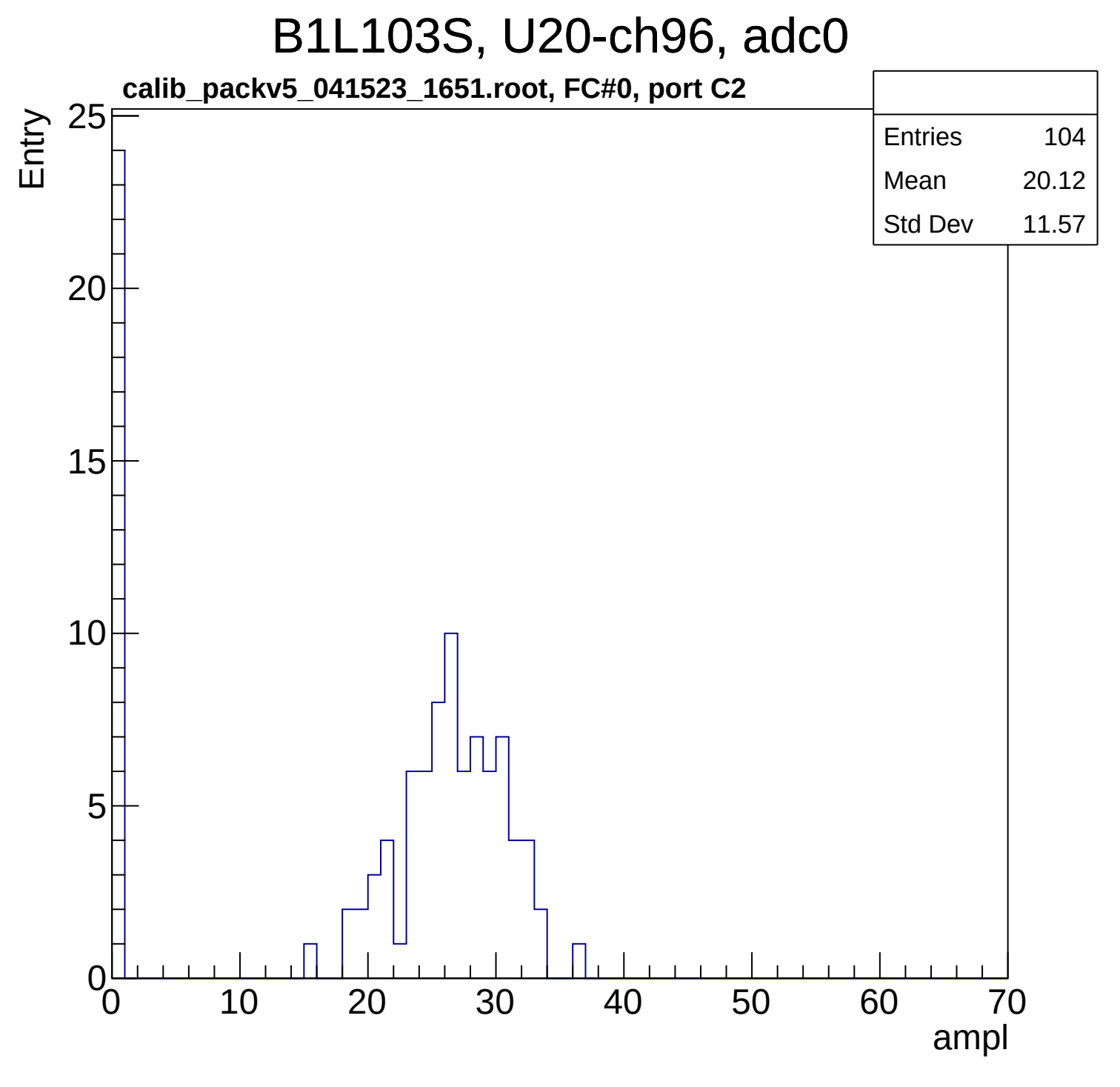
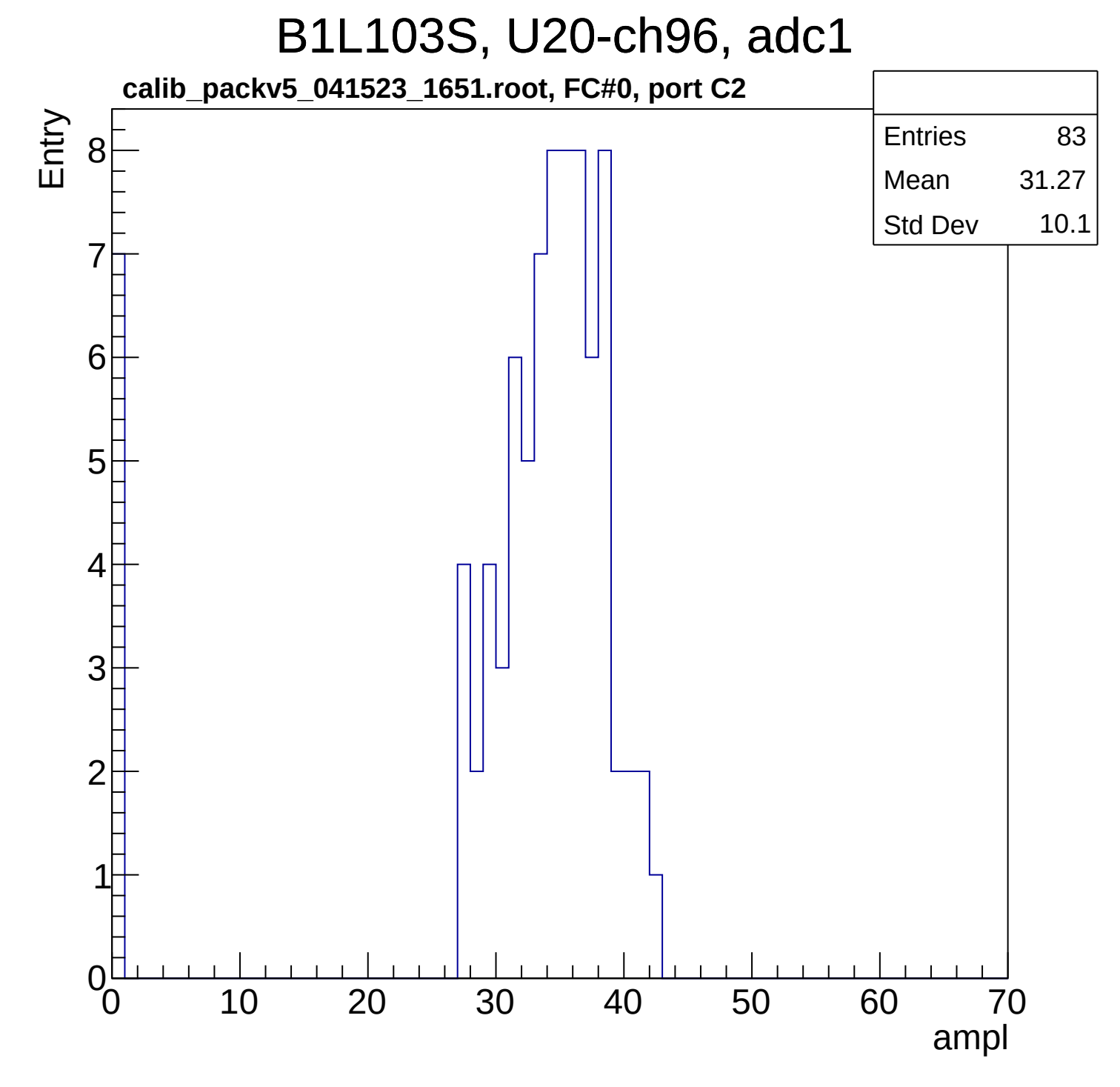

B1L103S, U20-ch95, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0.8421
Std Dev 3.573
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch96, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 104
Mean 20.12
Std Dev 11.57
Entry
ampl
0
5
10
15
20
25
0
10
20
30
40
50
60
70


B1L103S, U20-ch96, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 31.27
Std Dev 10.1
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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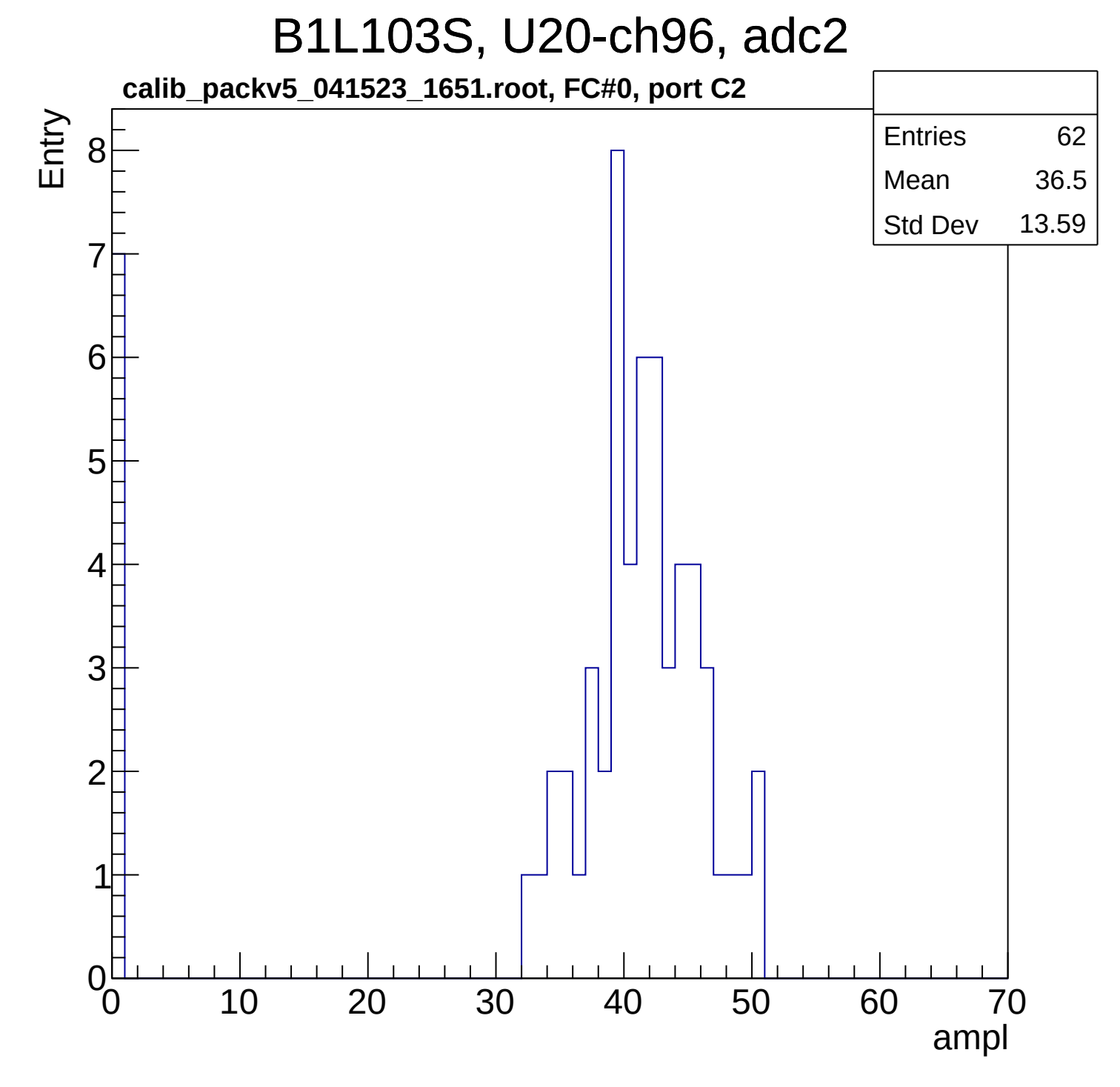
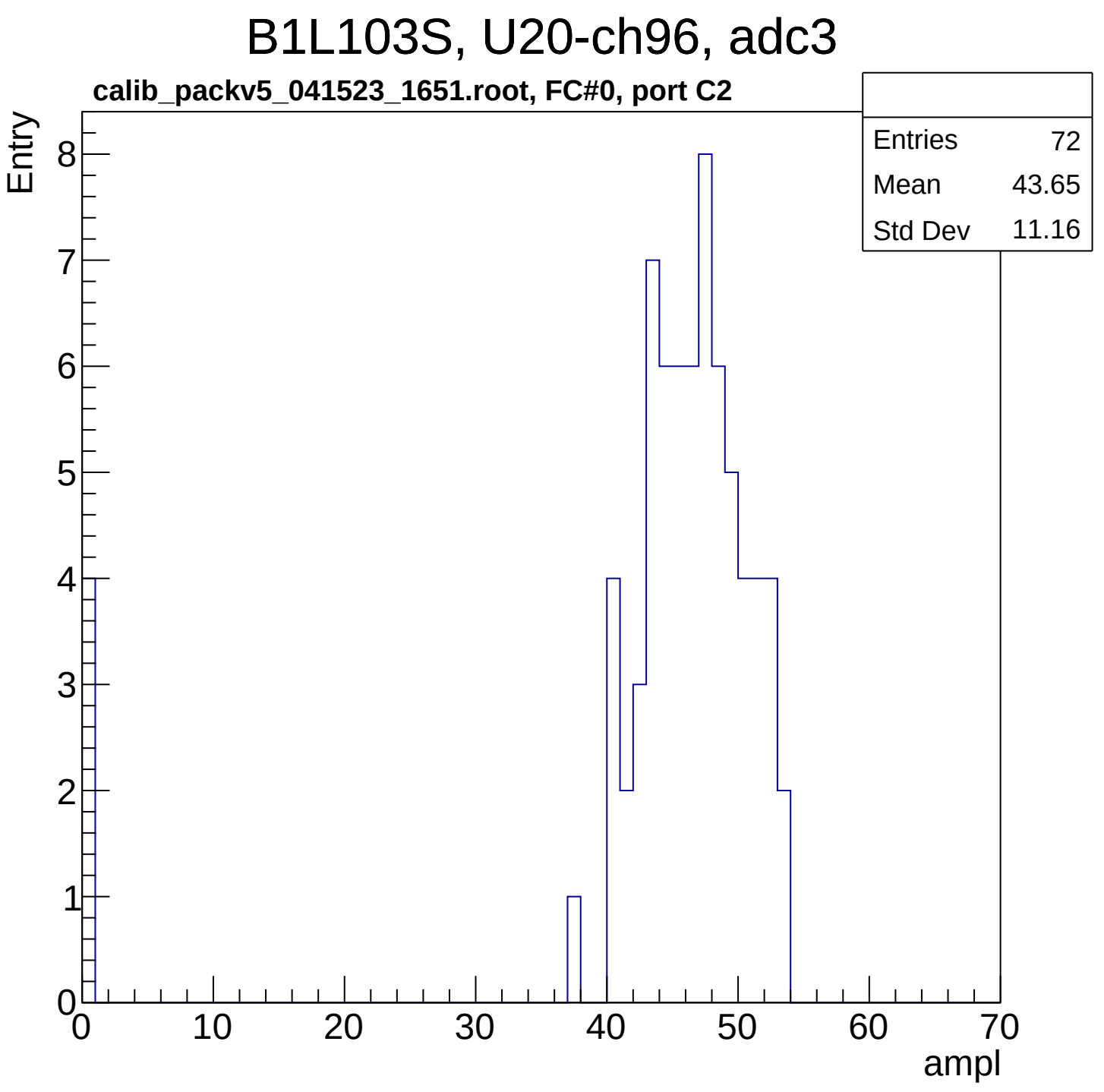

B1L103S, U20-ch96, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 36.5
Std Dev 13.59
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch96, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 43.65
Std Dev 11.16
Entry
ampl
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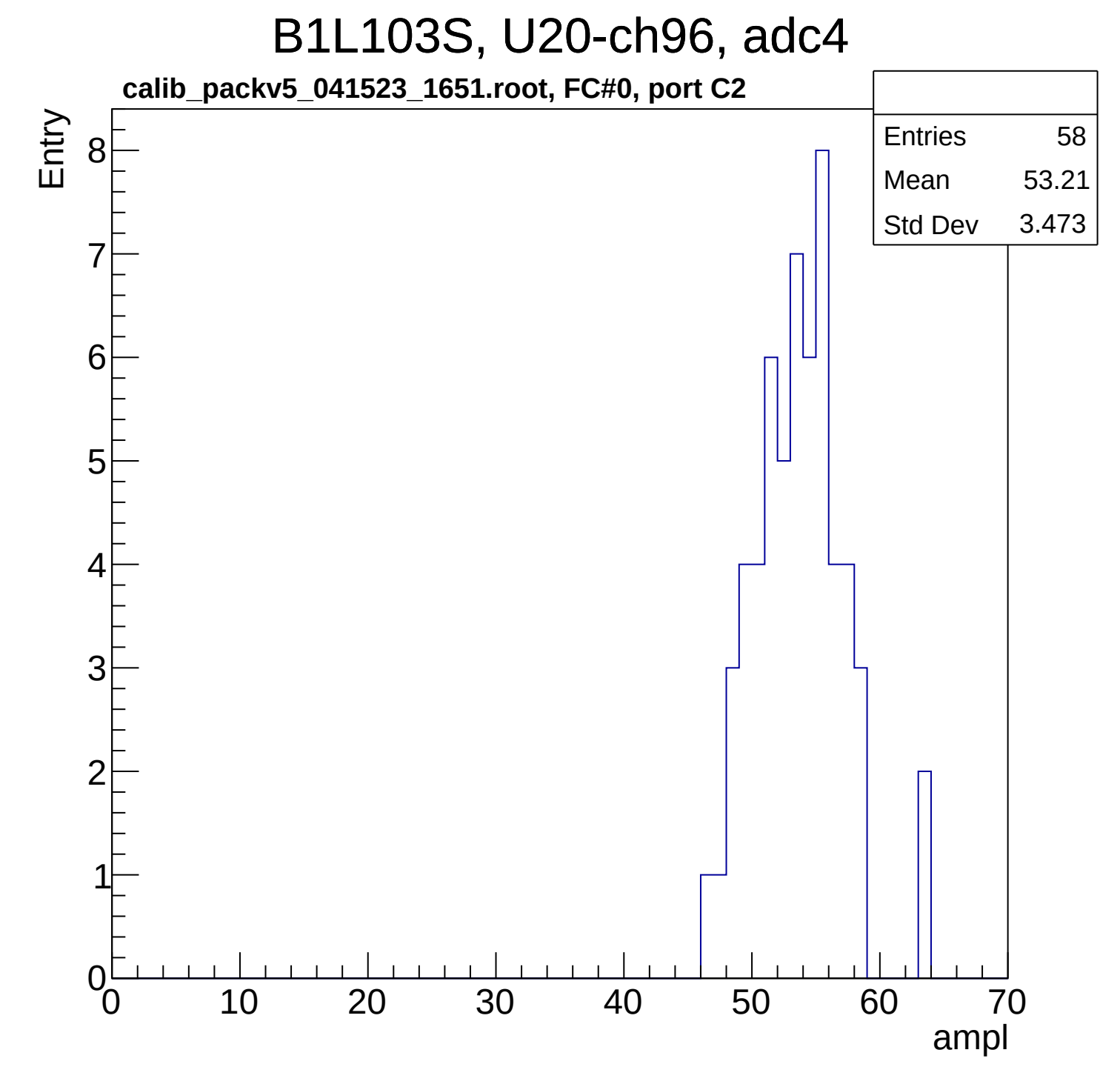
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch96, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 53.21
Std Dev 3.473
Entry
ampl
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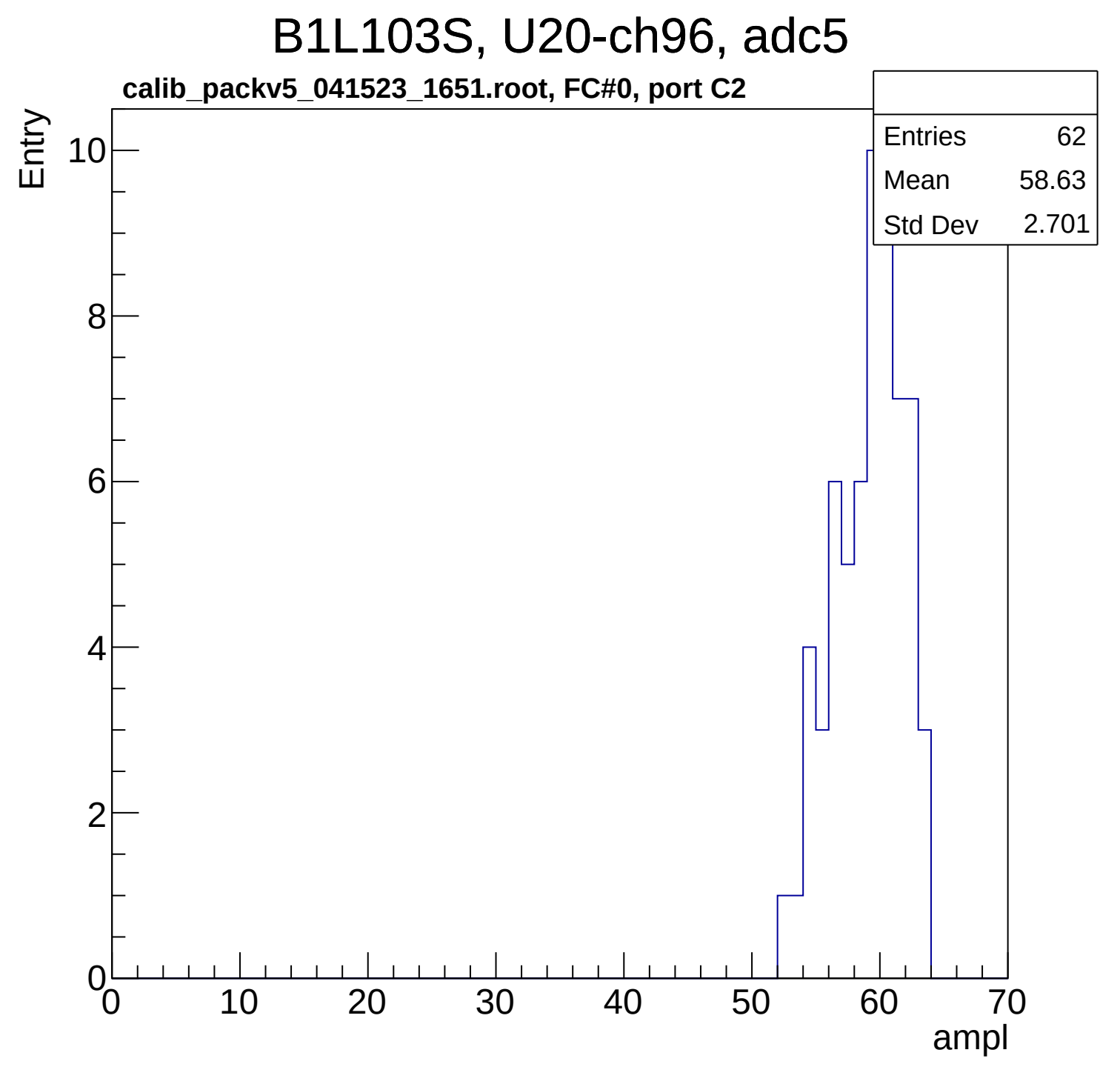
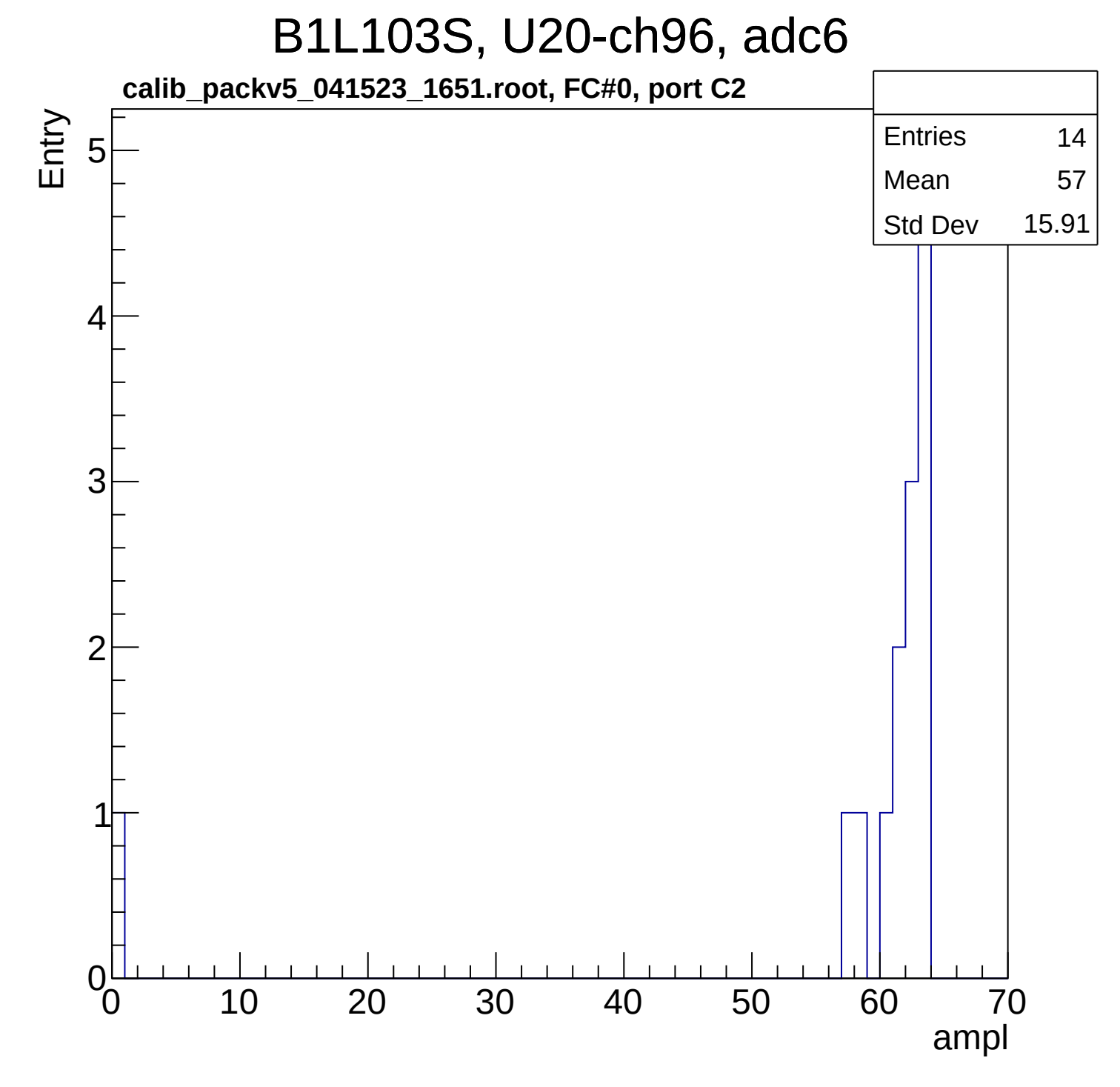
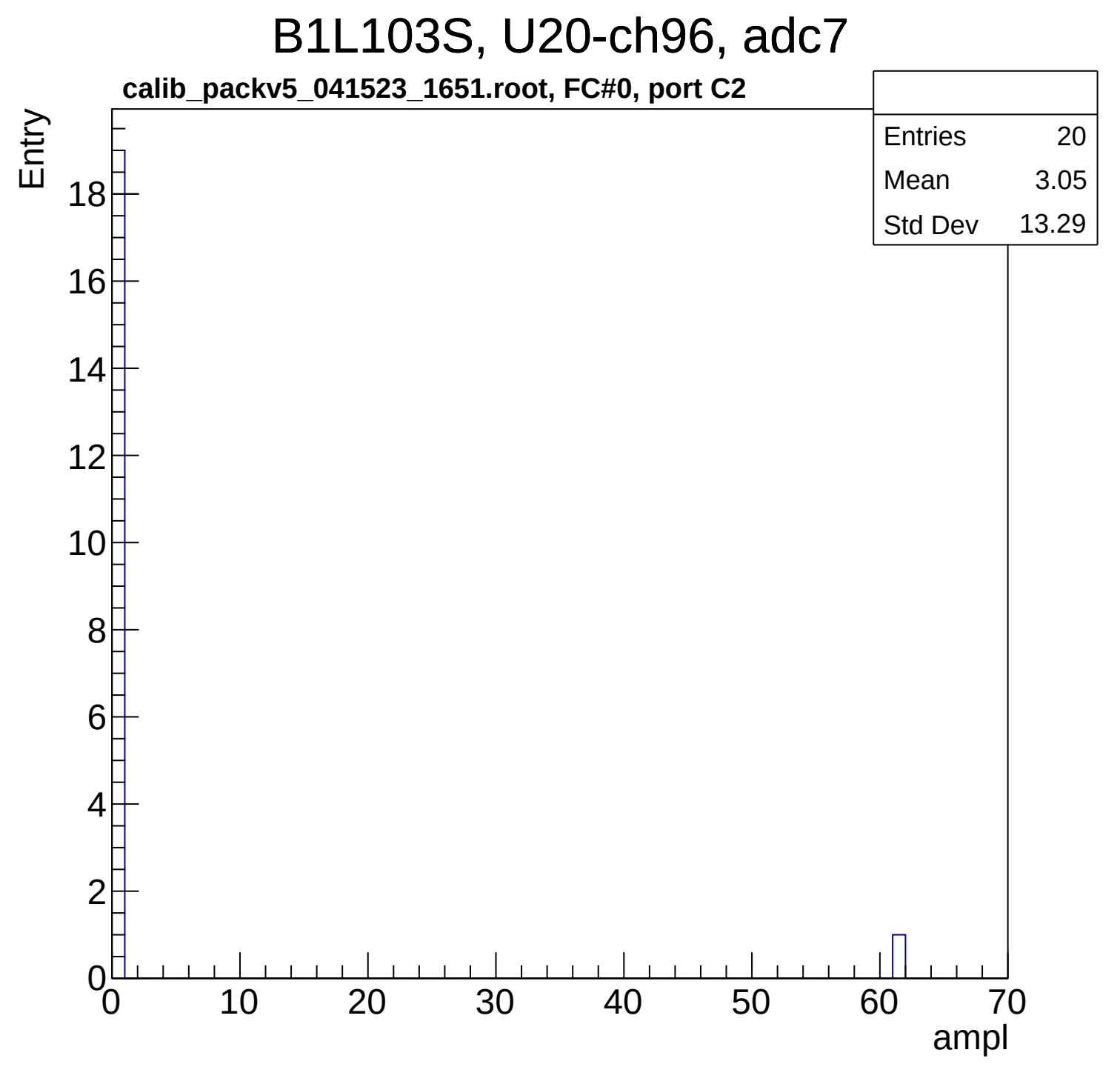
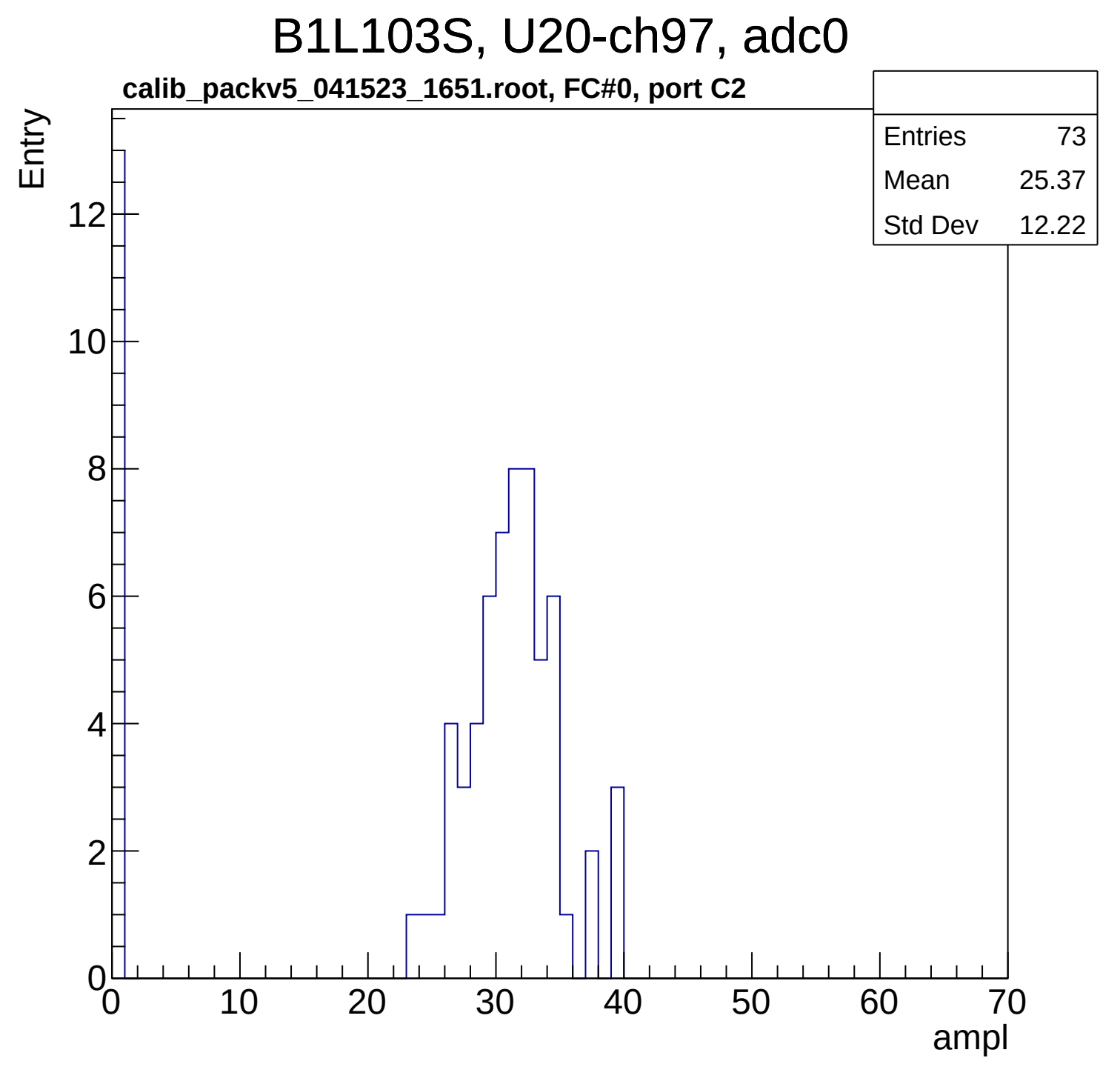
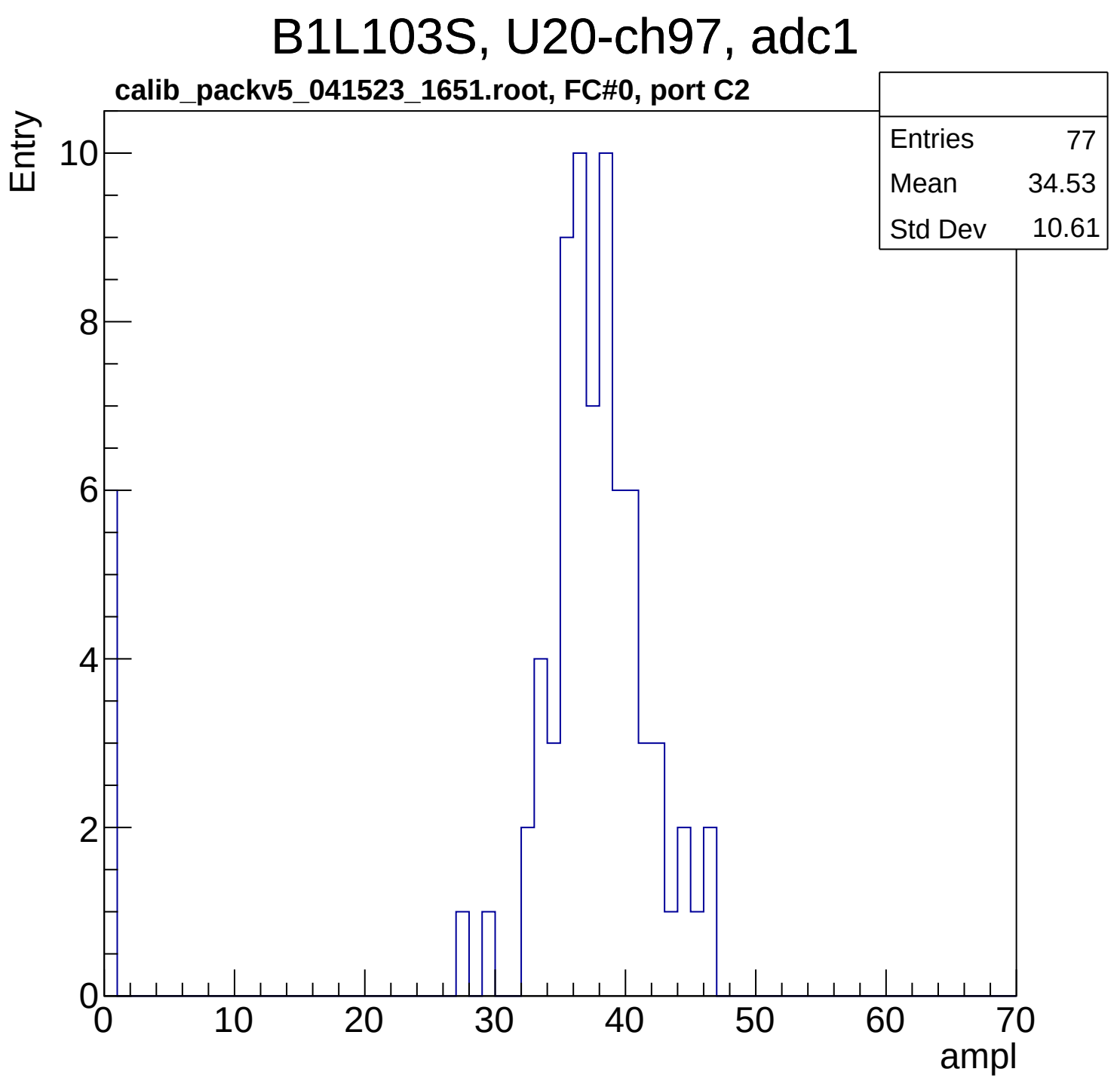
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch96, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 58.63
Std Dev 2.701
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch96, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 57
Std Dev 15.91
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch96, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.05
Std Dev 13.29
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch97, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 25.37
Std Dev 12.22
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch97, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 34.53
Std Dev 10.61
Entry
0
2
4
6
8
10
0
10
20
30
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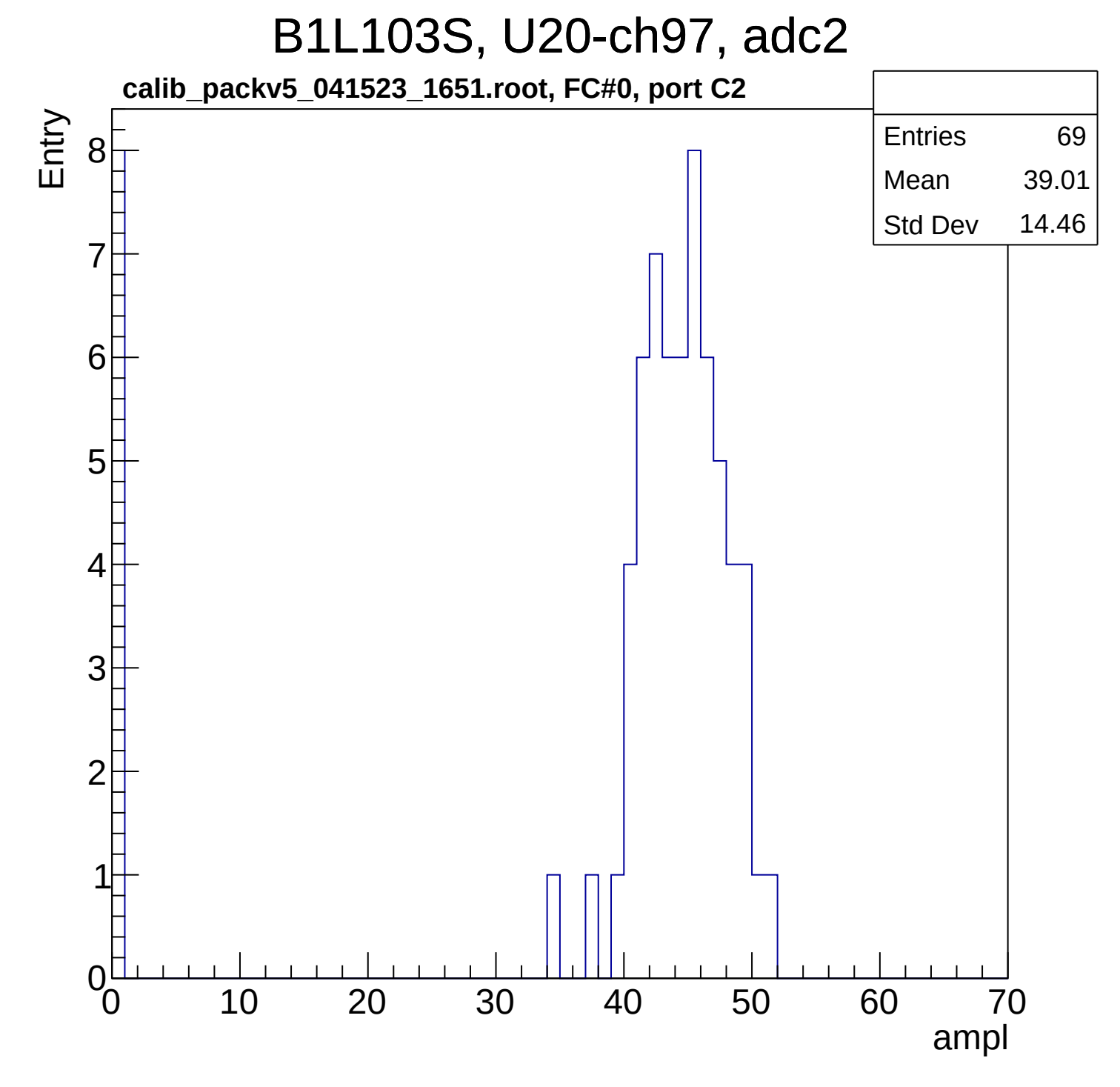
50
60
70
ampl


B1L103S, U20-ch97, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 39.01
Std Dev 14.46
Entry
ampl
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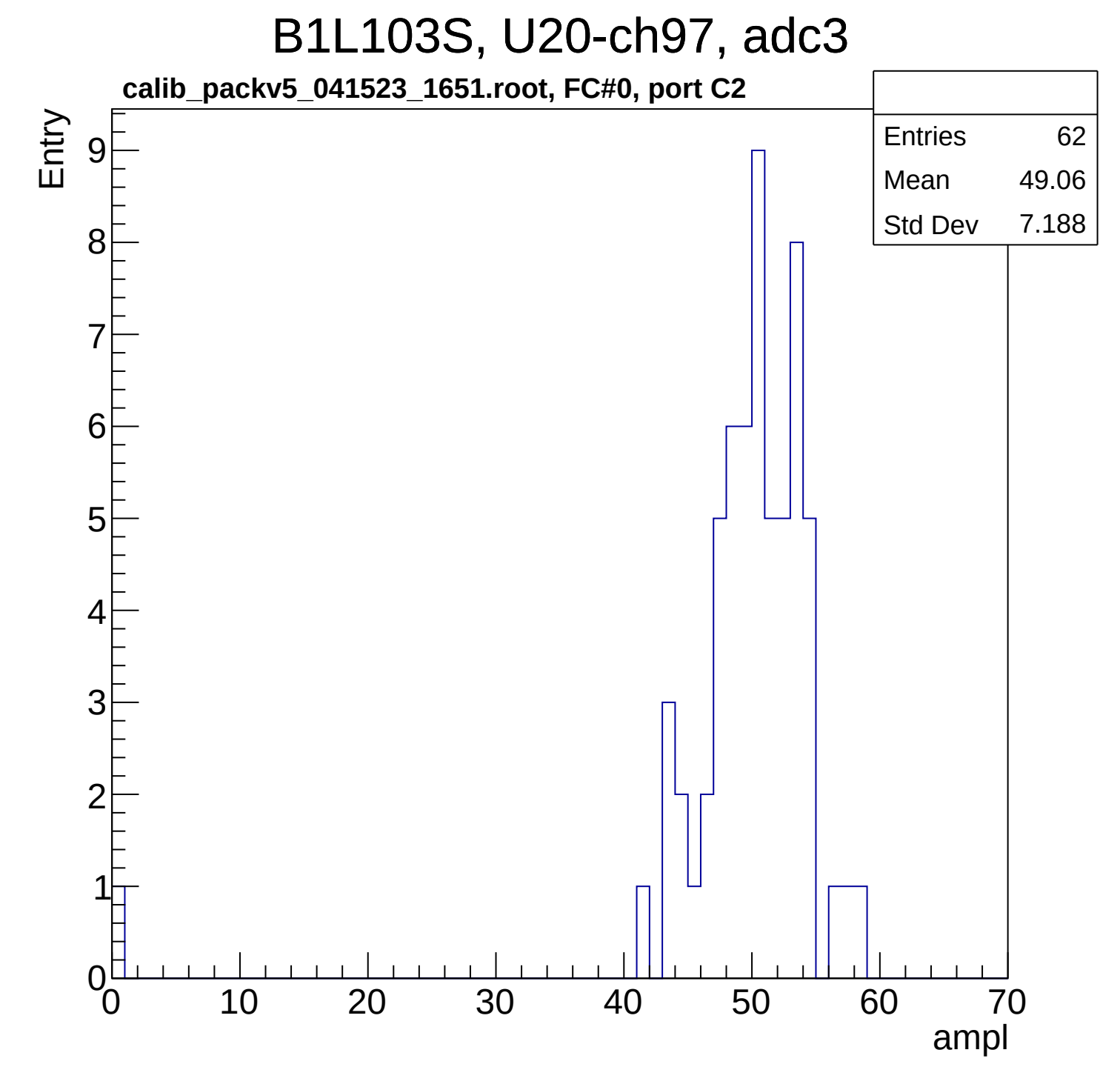
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch97, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 49.06
Std Dev 7.188
Entry
ampl
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2
3
4
5
6
7
8
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0
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40
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60
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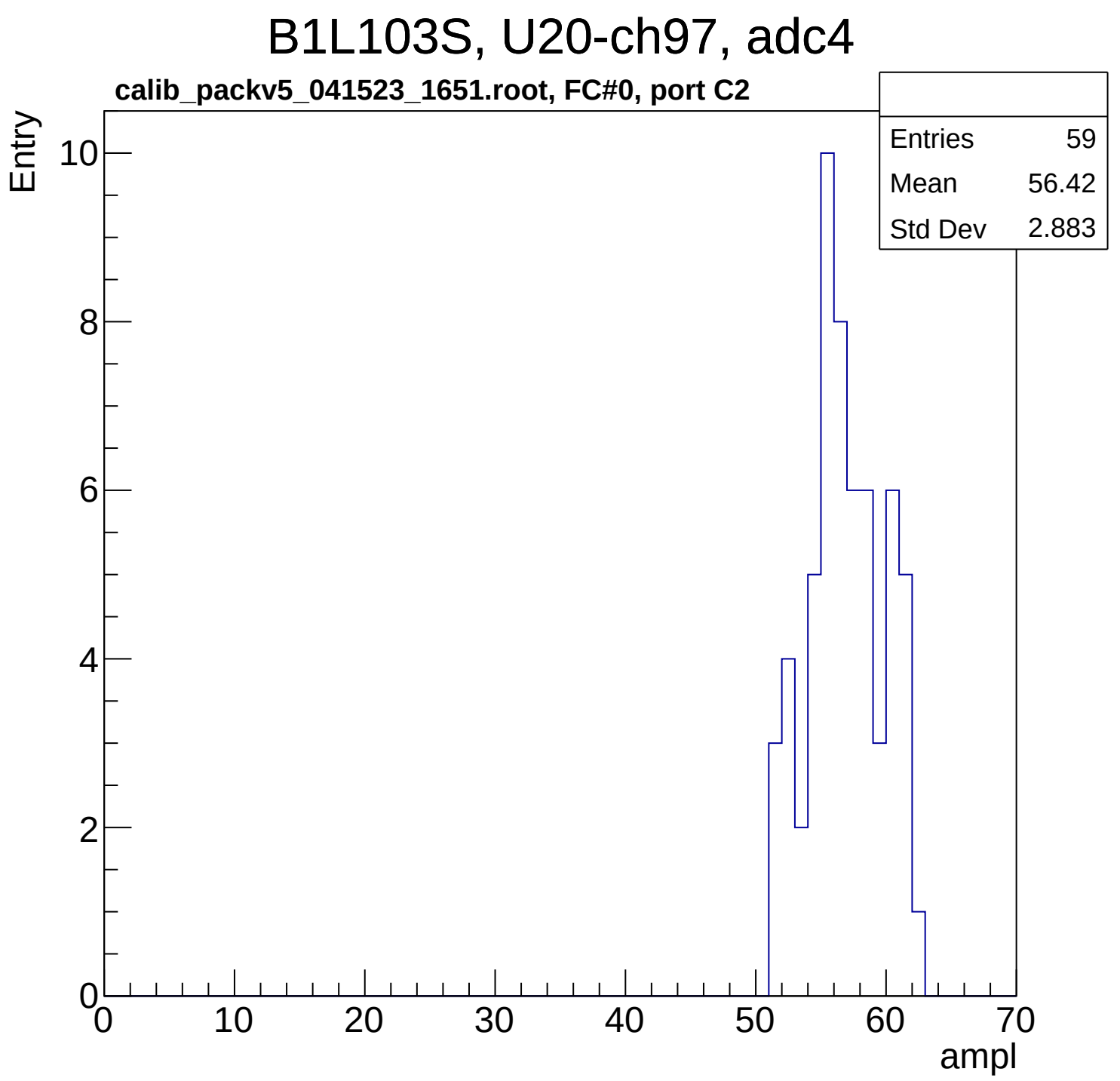
B1L103S, U20-ch97, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 56.42
Std Dev 2.883
Entry
ampl
0
2
4
6
8
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0
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40
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60
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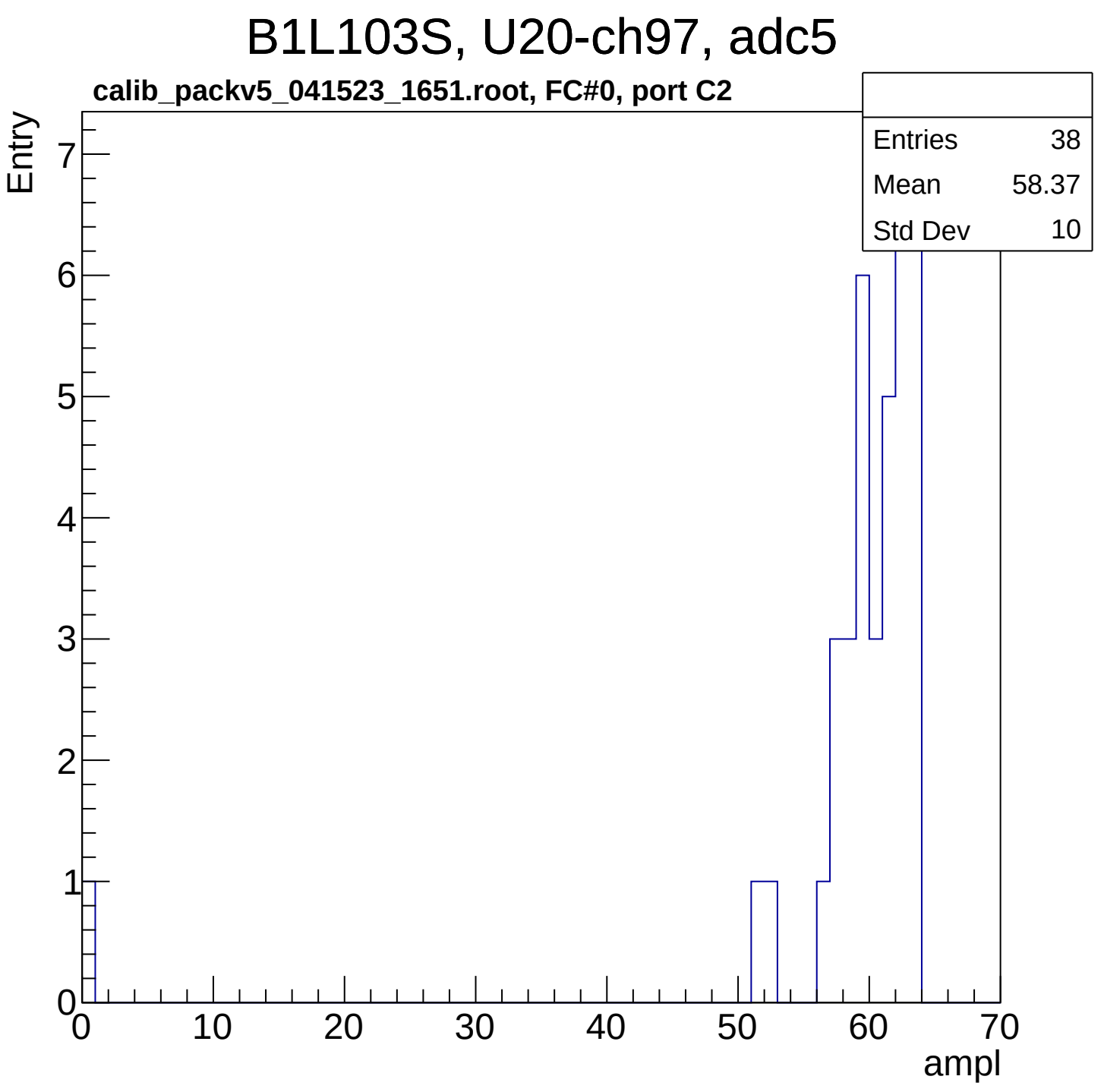
B1L103S, U20-ch97, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 58.37
Std Dev 10
Entry
ampl
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1
2
3
4
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6
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0
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20
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40
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60
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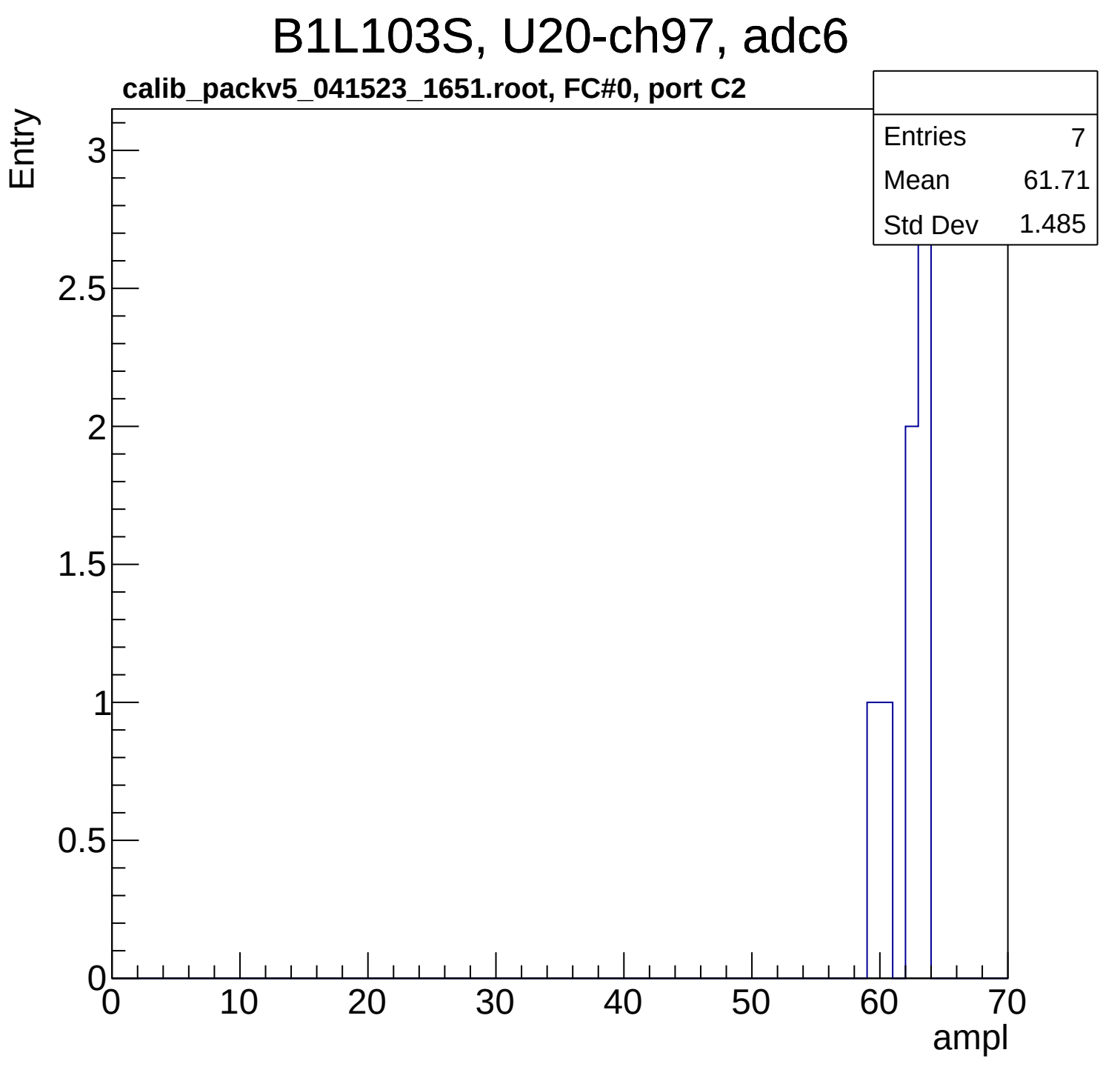
B1L103S, U20-ch97, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 61.71
Std Dev 1.485
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
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40
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60
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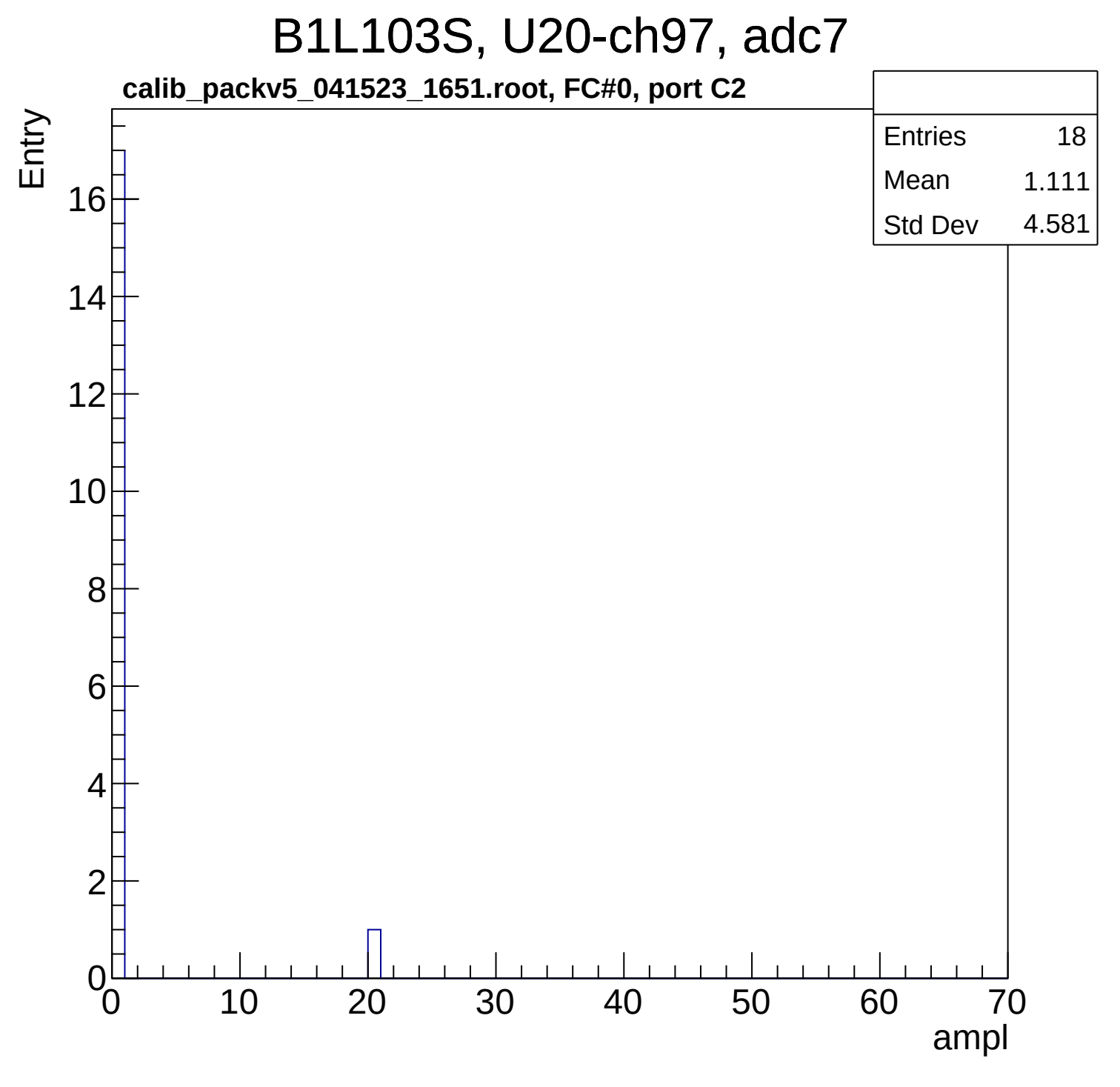
B1L103S, U20-ch97, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.111
Std Dev 4.581
Entry
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4
6
8
10
12
14
16
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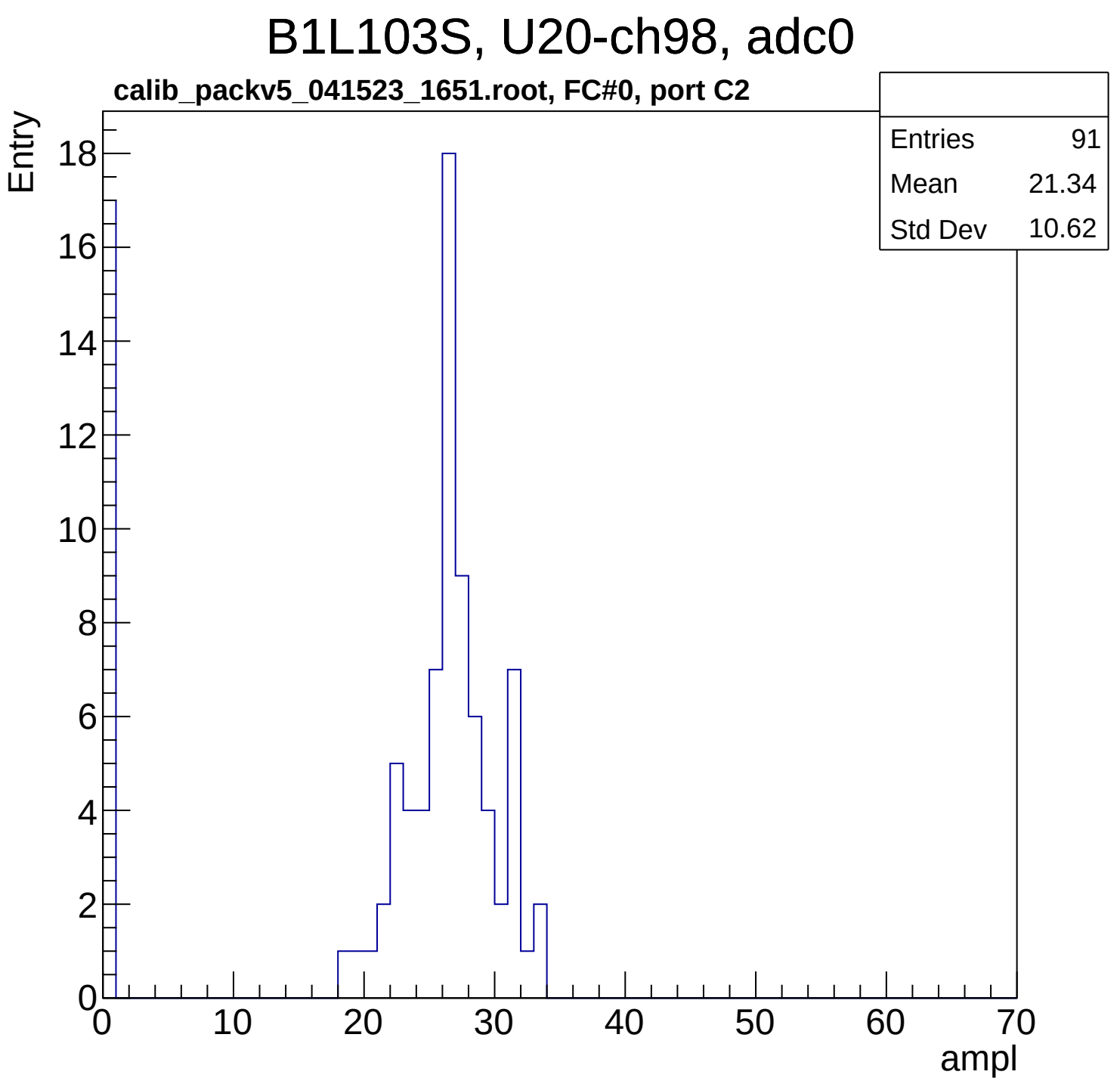
70
ampl


B1L103S, U20-ch98, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 21.34
Std Dev 10.62
Entry
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6
8
10
12
14
16
18
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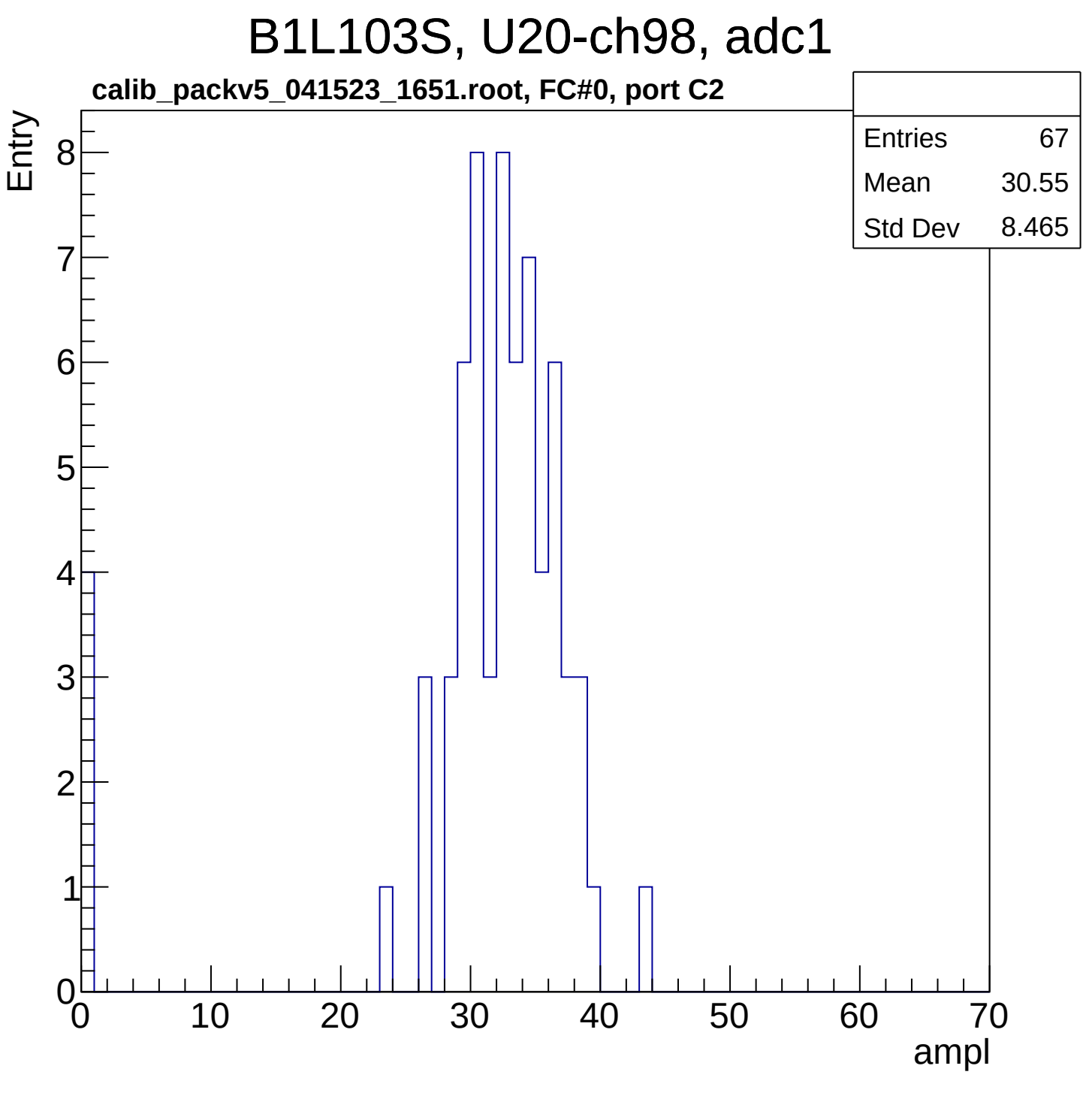
70
ampl


B1L103S, U20-ch98, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 30.55
Std Dev 8.465
Entry
ampl
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3
4
5
6
7
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0
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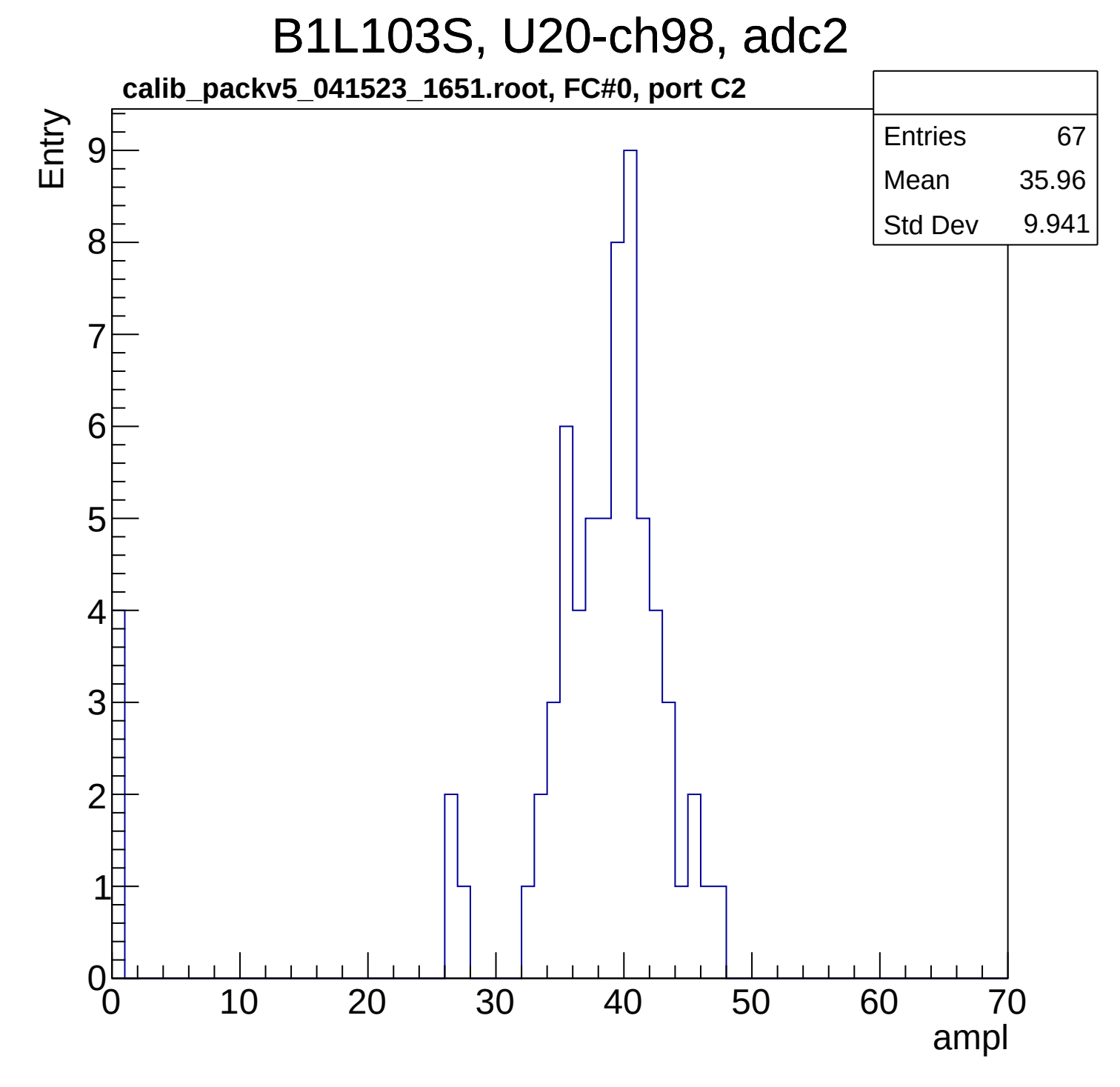
B1L103S, U20-ch98, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 35.96
Std Dev 9.941
Entry
ampl
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2
3
4
5
6
7
8
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0
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20
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60
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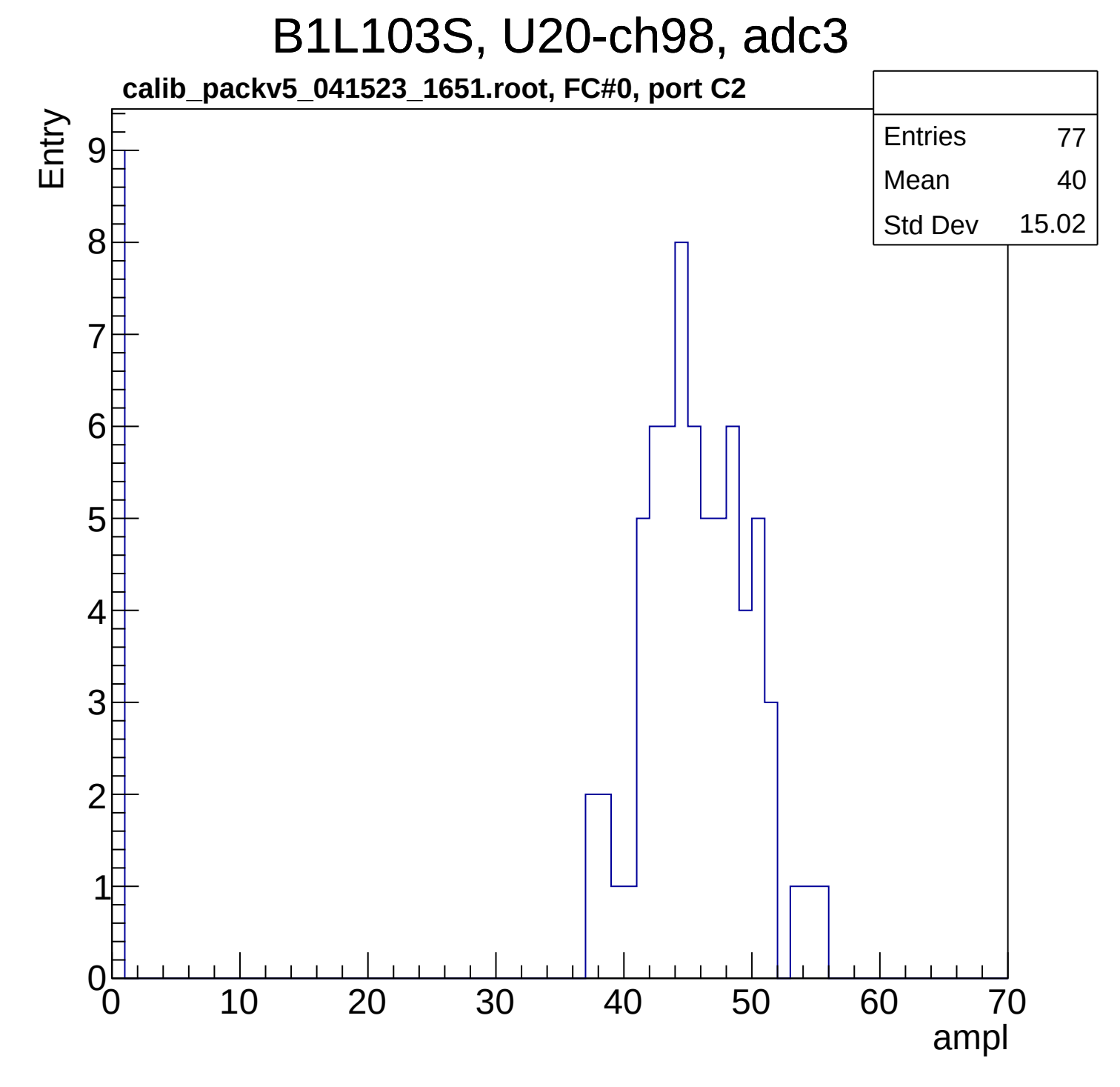
B1L103S, U20-ch98, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 40
Std Dev 15.02
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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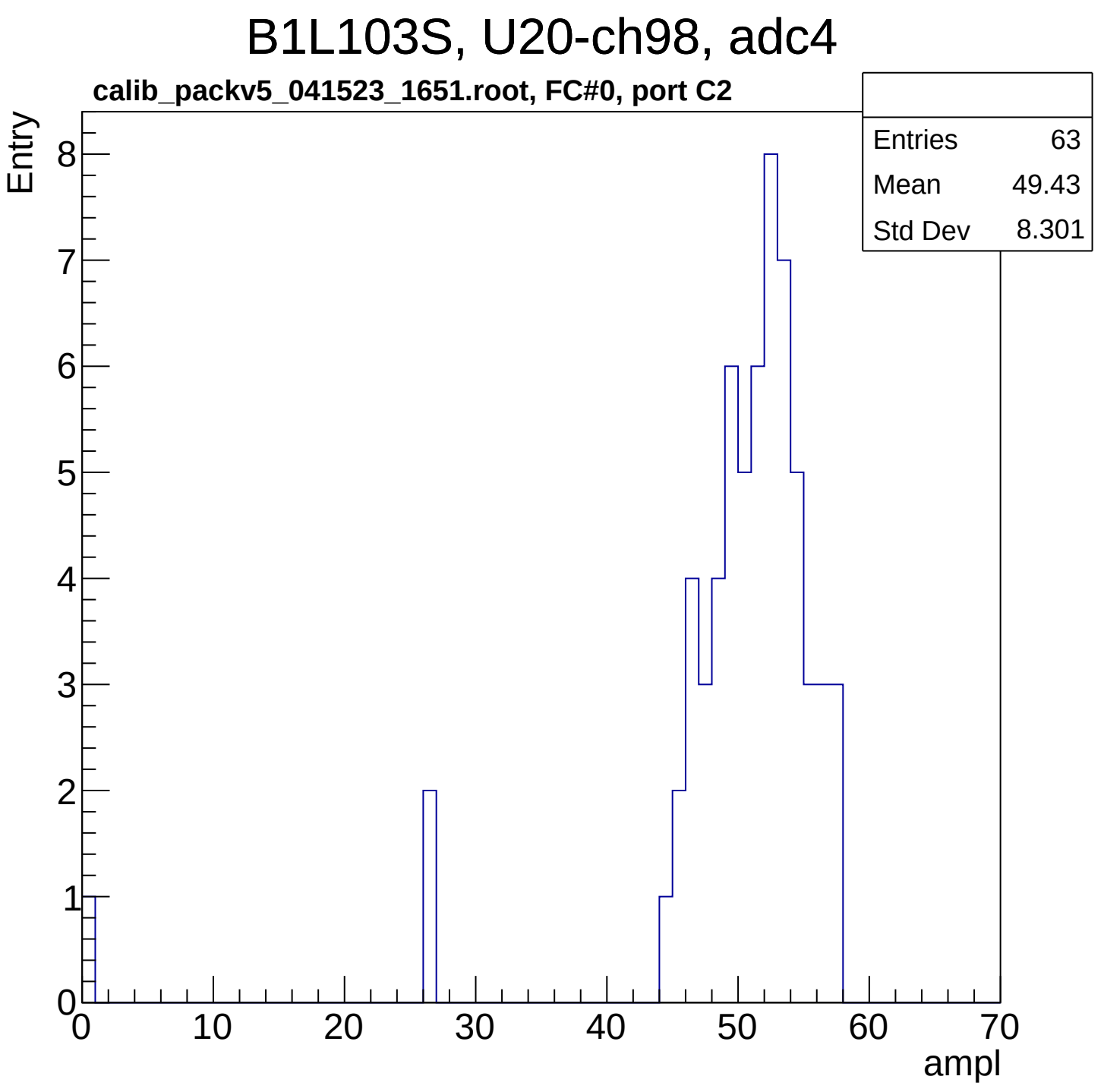
B1L103S, U20-ch98, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 49.43
Std Dev 8.301
Entry
ampl
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2
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4
5
6
7
8
0
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20
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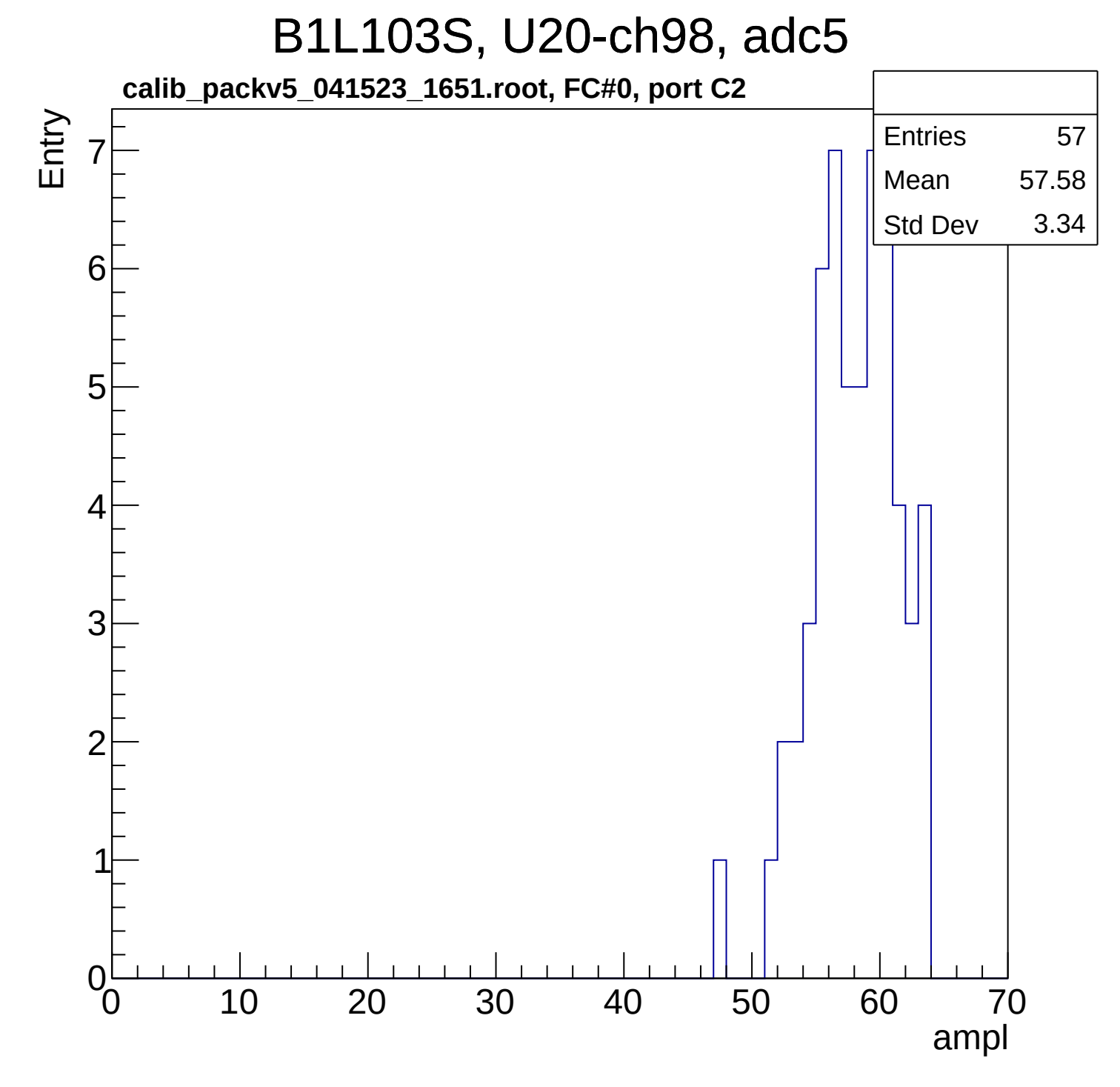
40
50
60
70


B1L103S, U20-ch98, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 57.58
Std Dev 3.34
Entry
ampl
0
1
2
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4
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6
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0
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20
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40
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60
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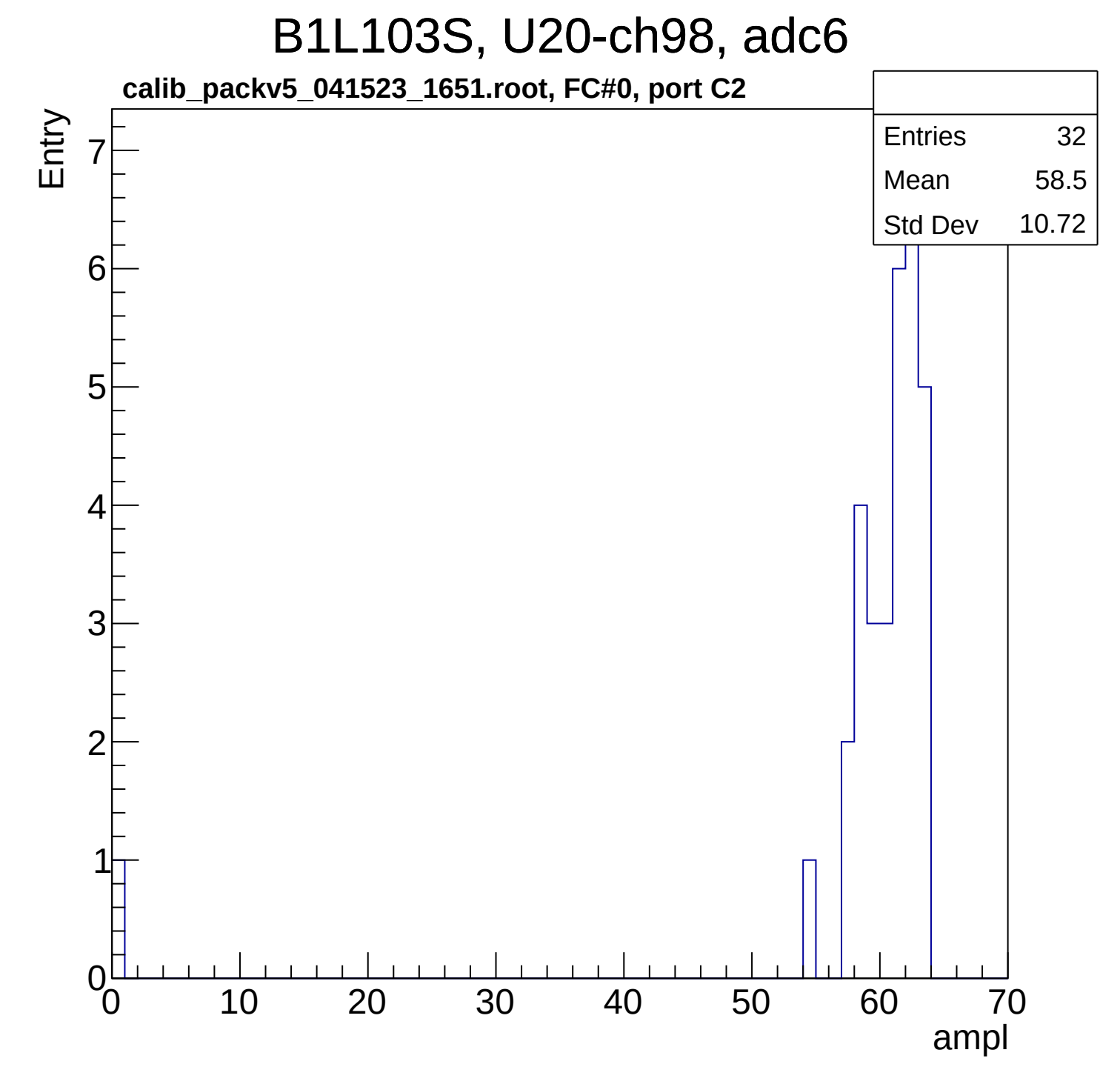
B1L103S, U20-ch98, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 58.5
Std Dev 10.72
Entry
ampl
0
1
2
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4
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6
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0
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20
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40
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60
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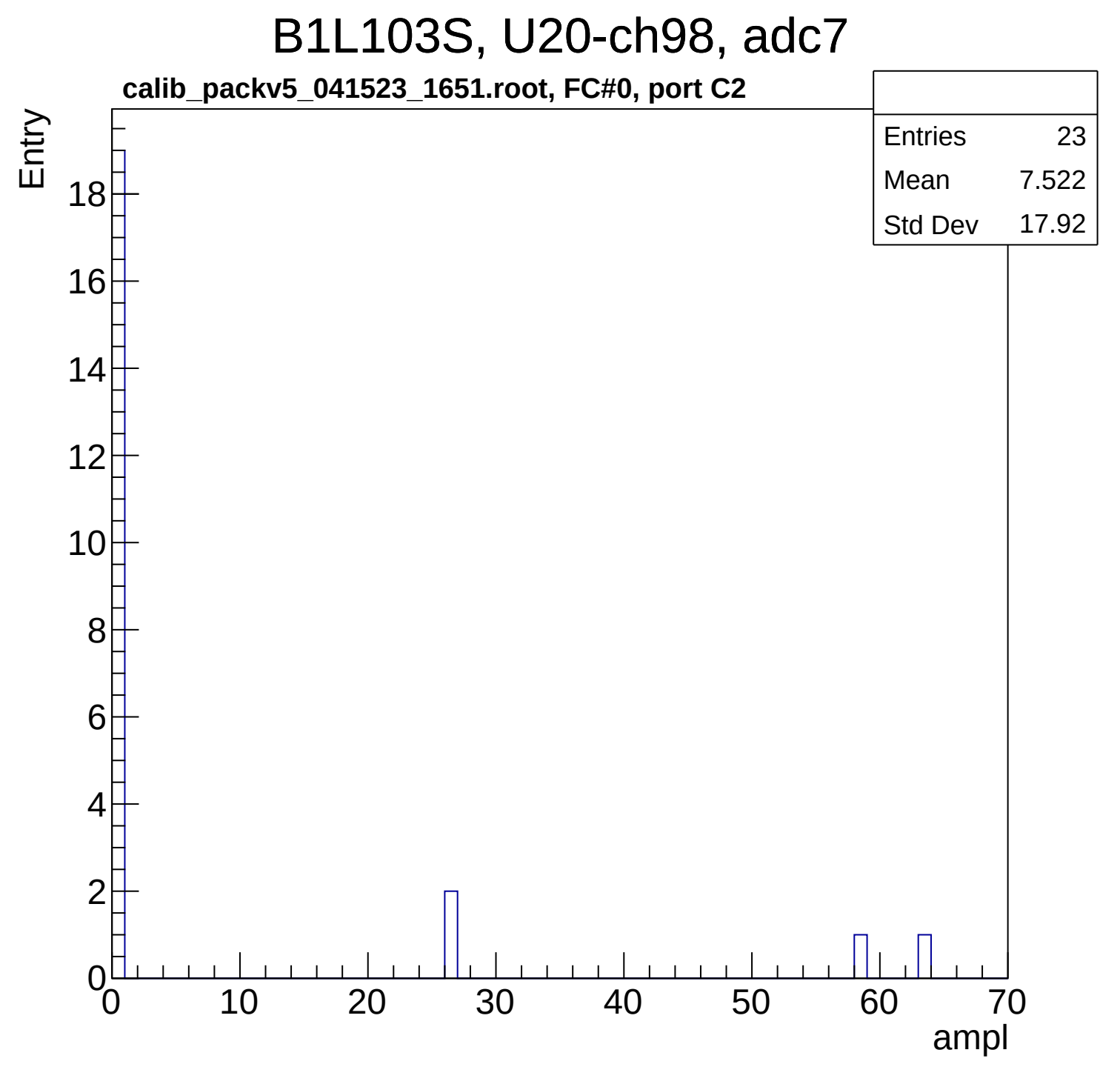
B1L103S, U20-ch98, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 7.522
Std Dev 17.92
Entry
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6
8
10
12
14
16
18
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10
20
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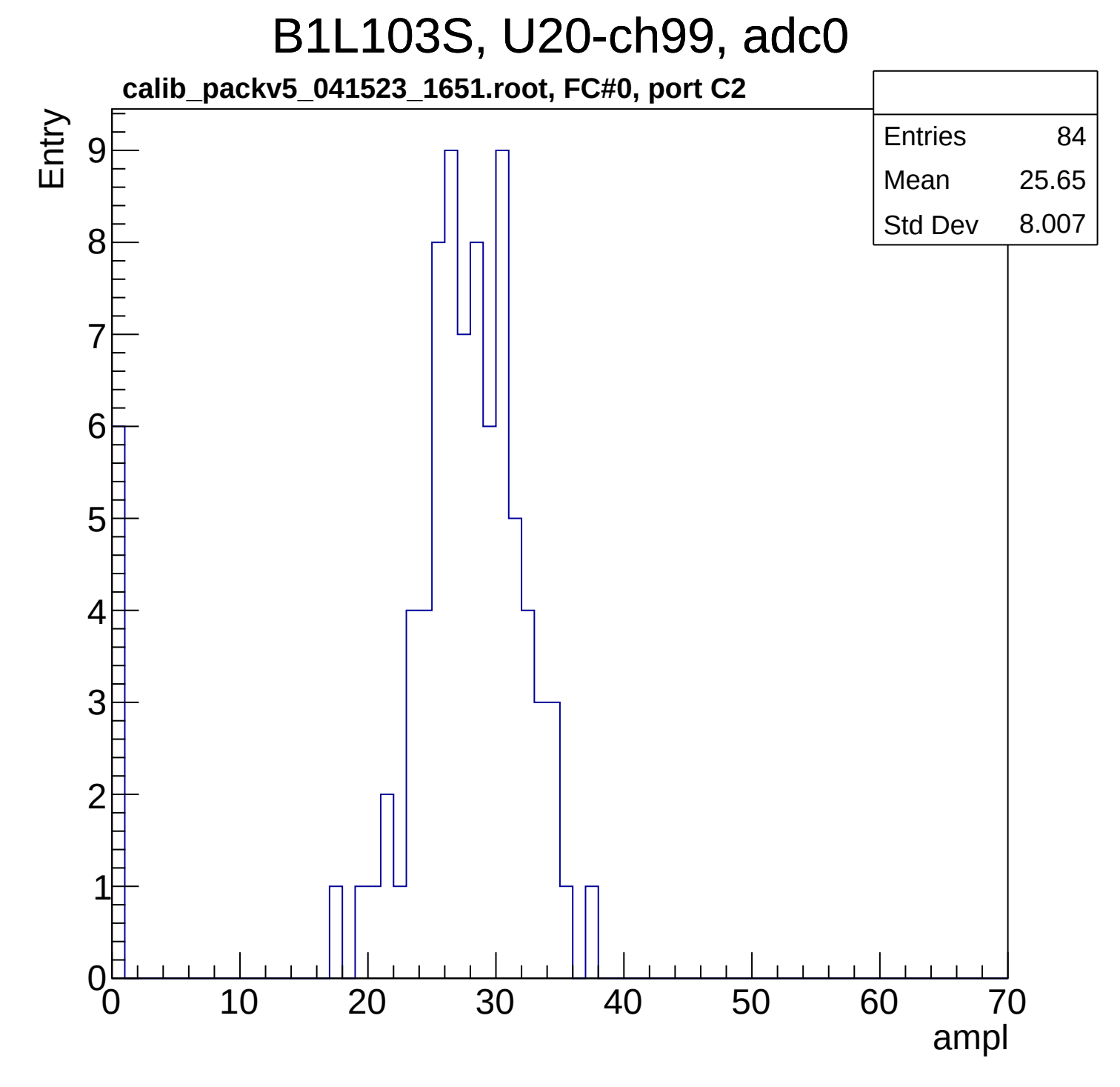
50
60
70
ampl


B1L103S, U20-ch99, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 25.65
Std Dev 8.007
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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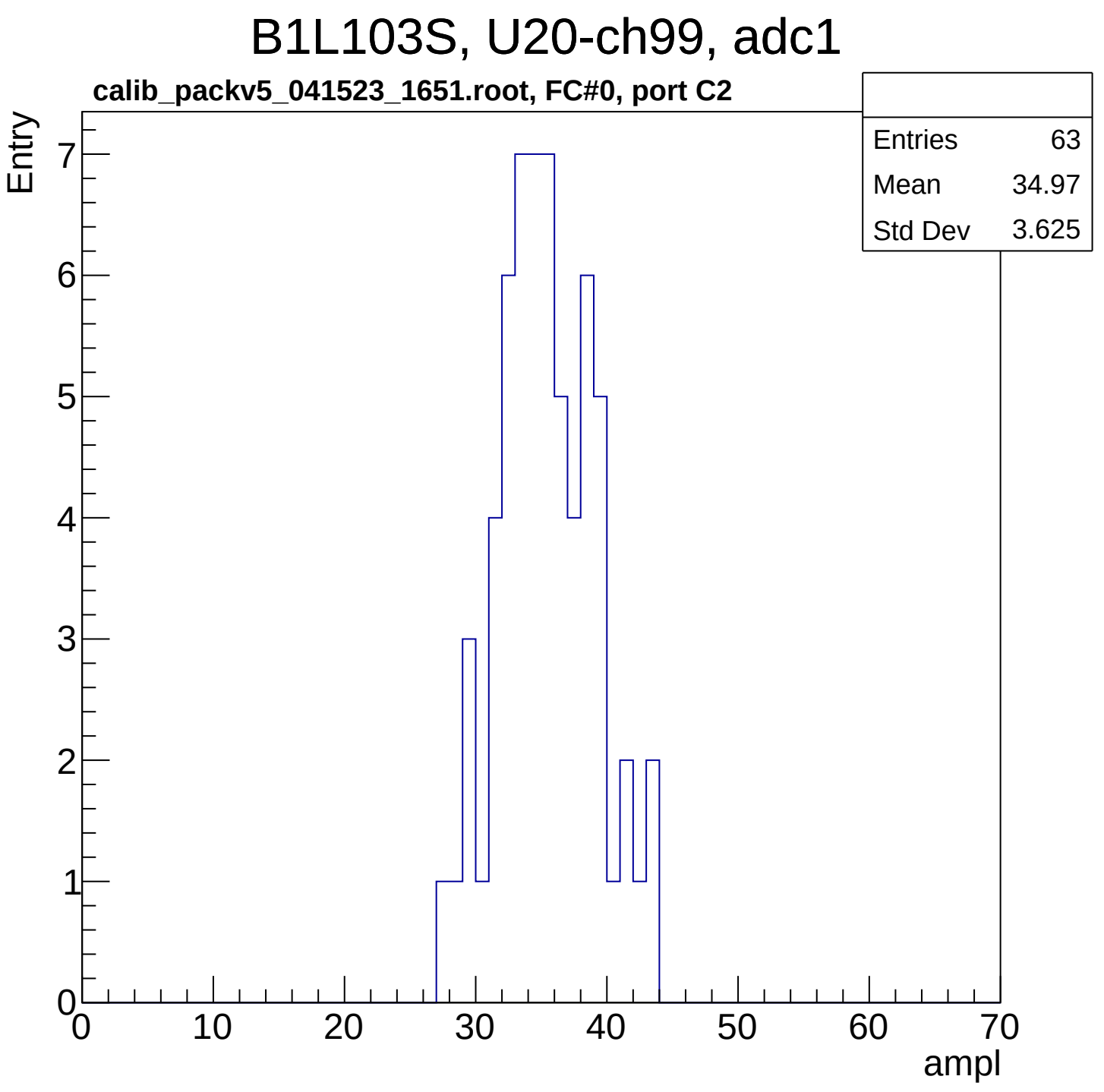
60
70


B1L103S, U20-ch99, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 34.97
Std Dev 3.625
Entry
ampl
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1
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4
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0
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40
50
60
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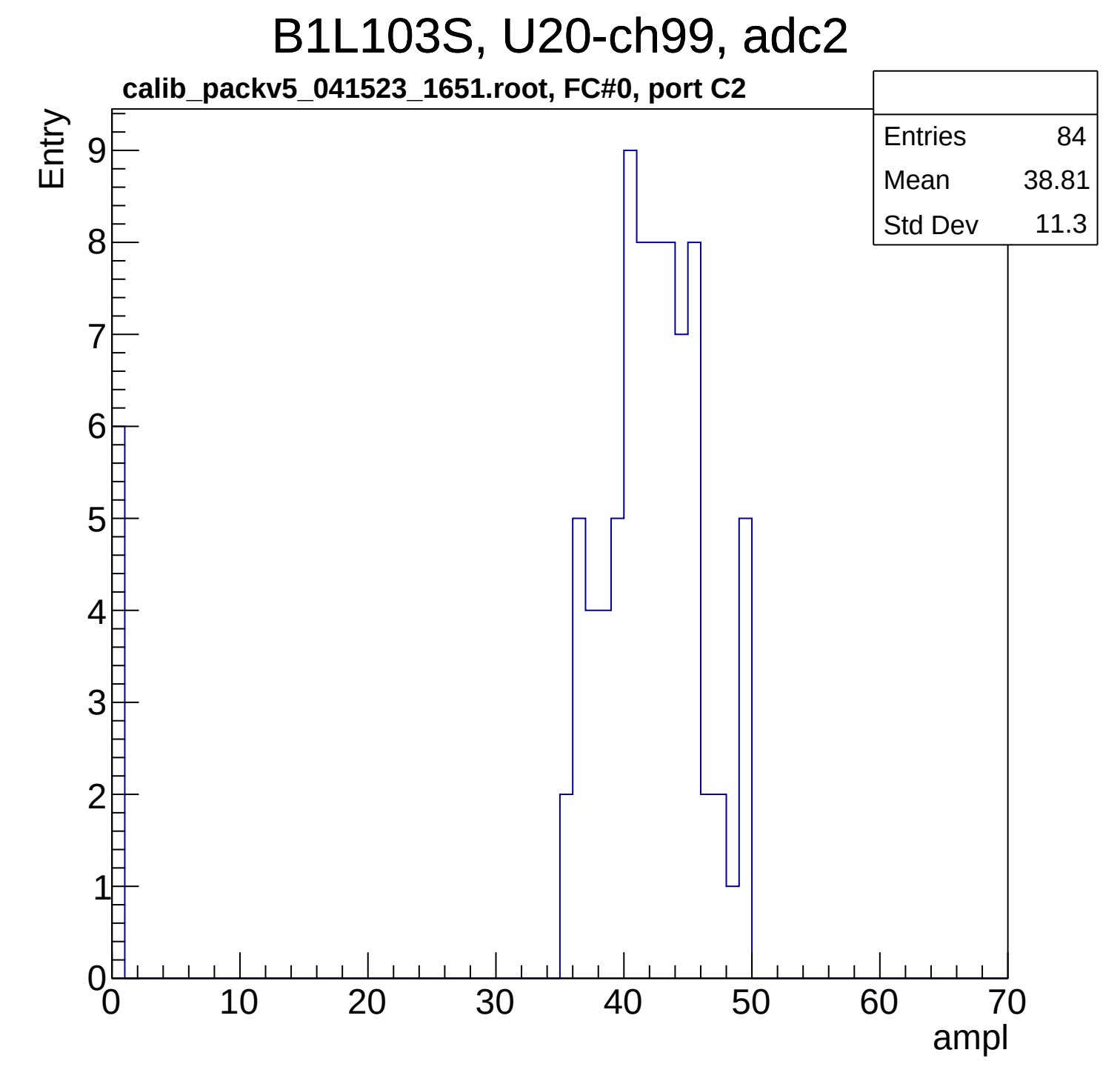
B1L103S, U20-ch99, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 38.81
Std Dev 11.3
Entry
ampl
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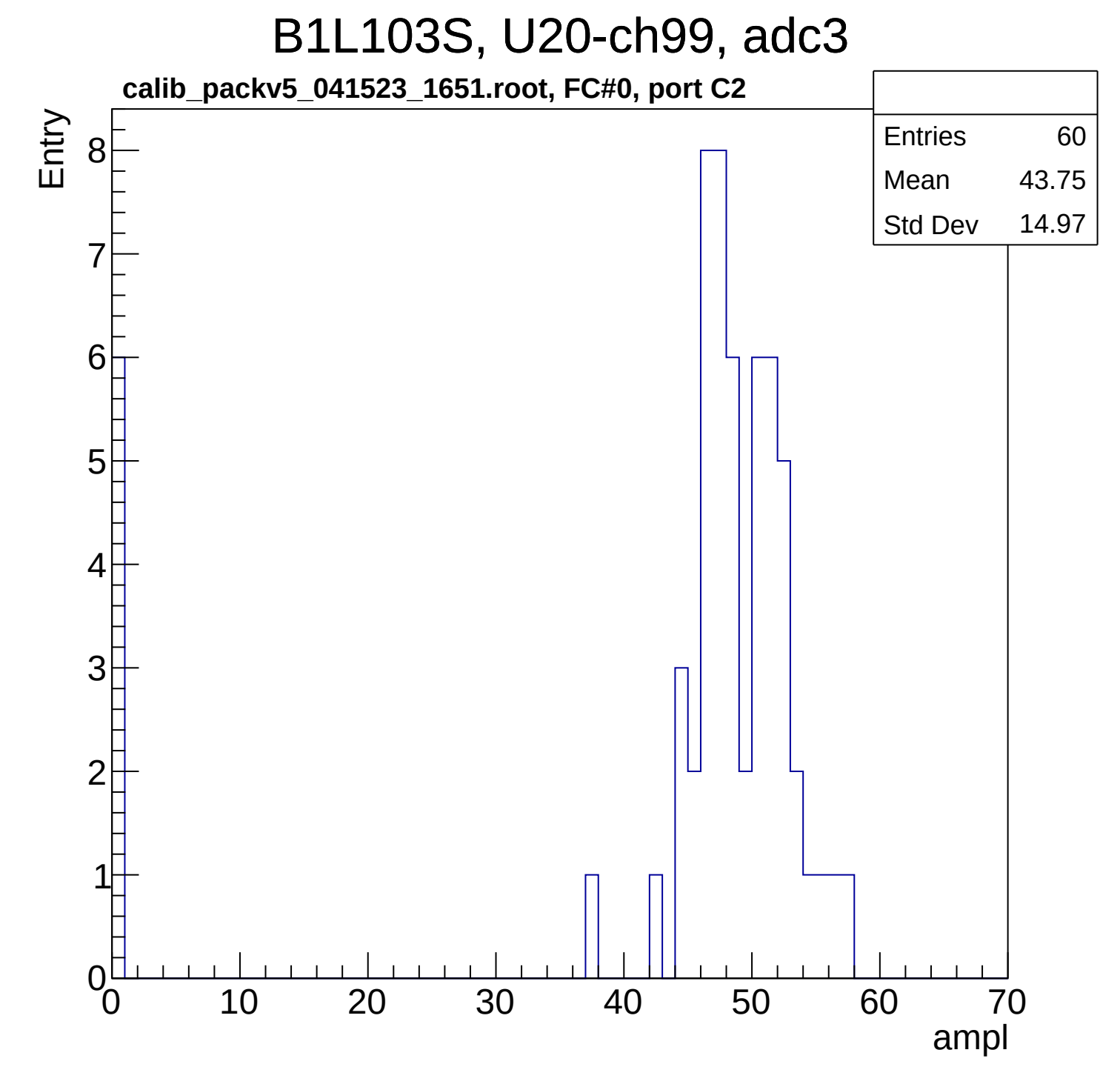
B1L103S, U20-ch99, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 43.75
Std Dev 14.97
Entry
ampl
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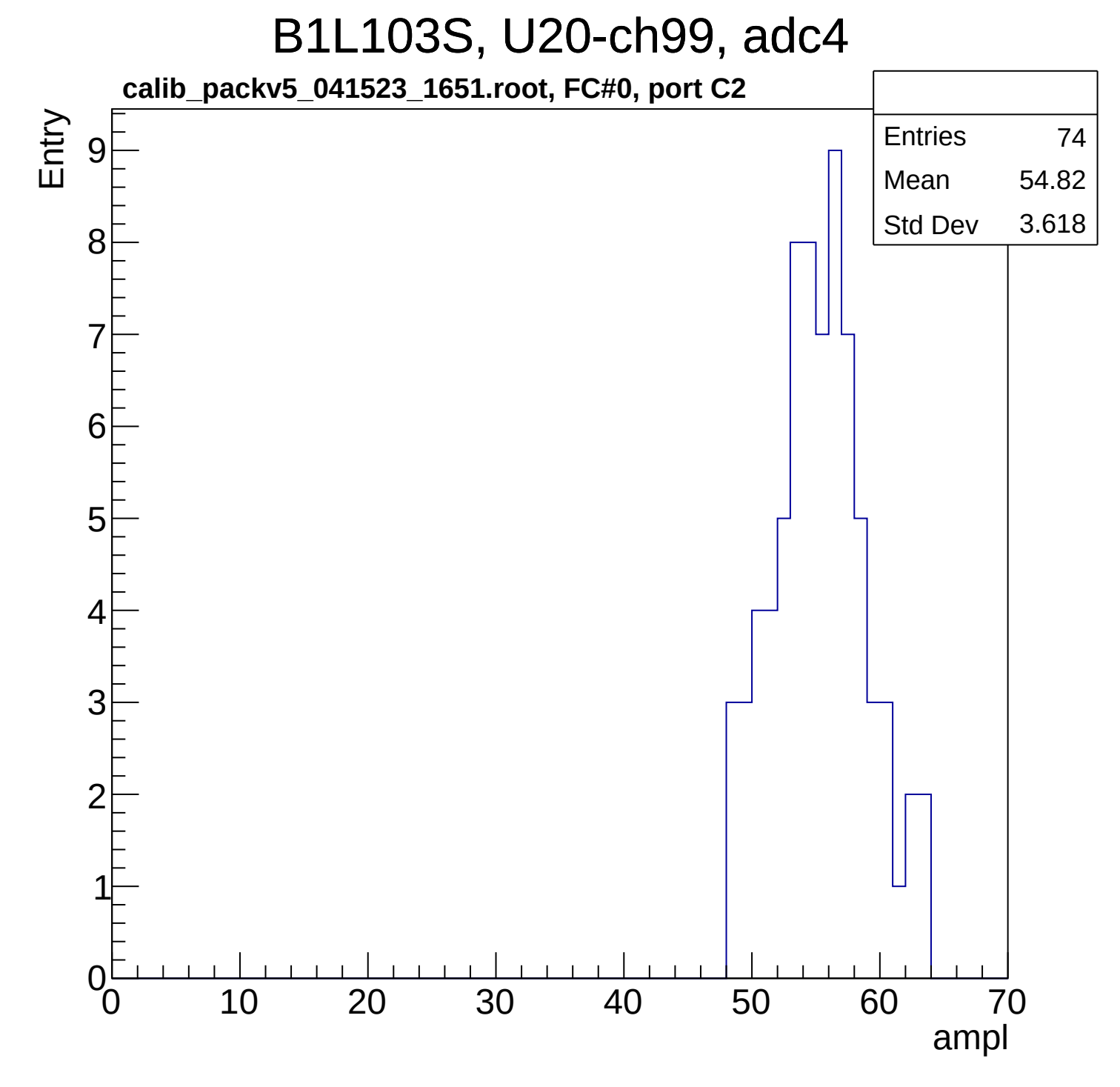
B1L103S, U20-ch99, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 54.82
Std Dev 3.618
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
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60
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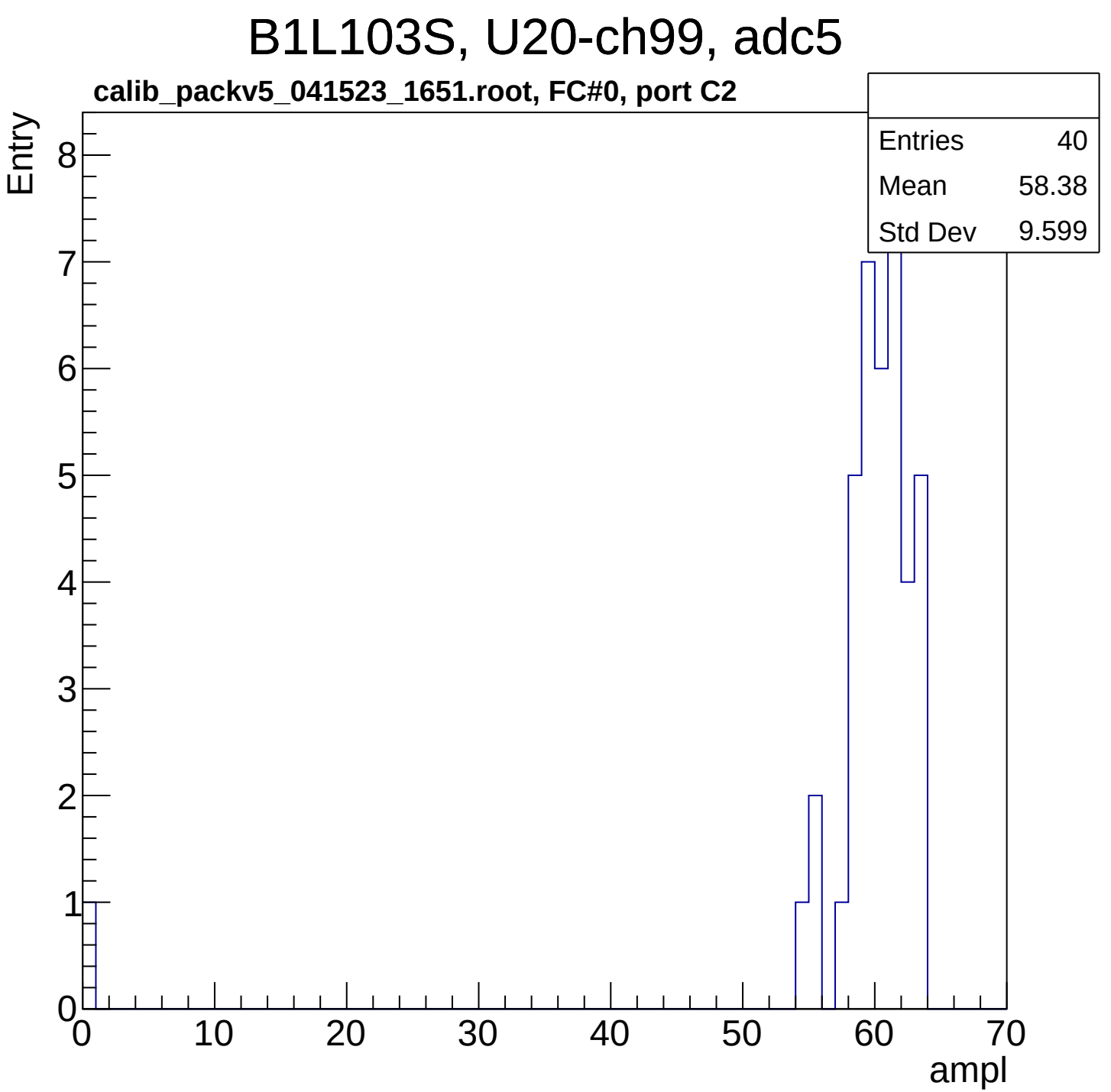
B1L103S, U20-ch99, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 58.38
Std Dev 9.599
Entry
ampl
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2
3
4
5
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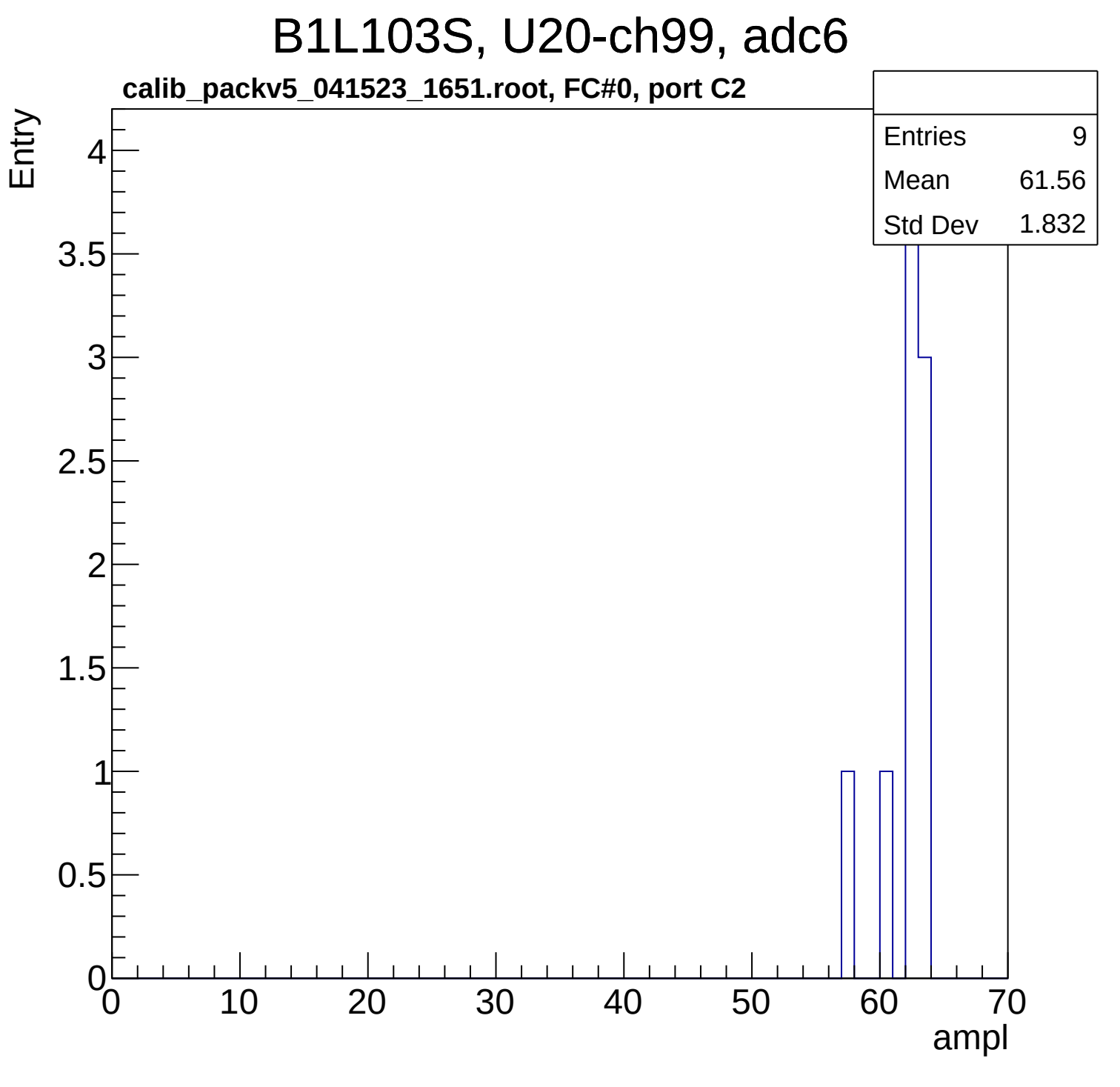
B1L103S, U20-ch99, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 61.56
Std Dev 1.832
Entry
ampl
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0.5
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1.5
2
2.5
3
3.5
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0
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60
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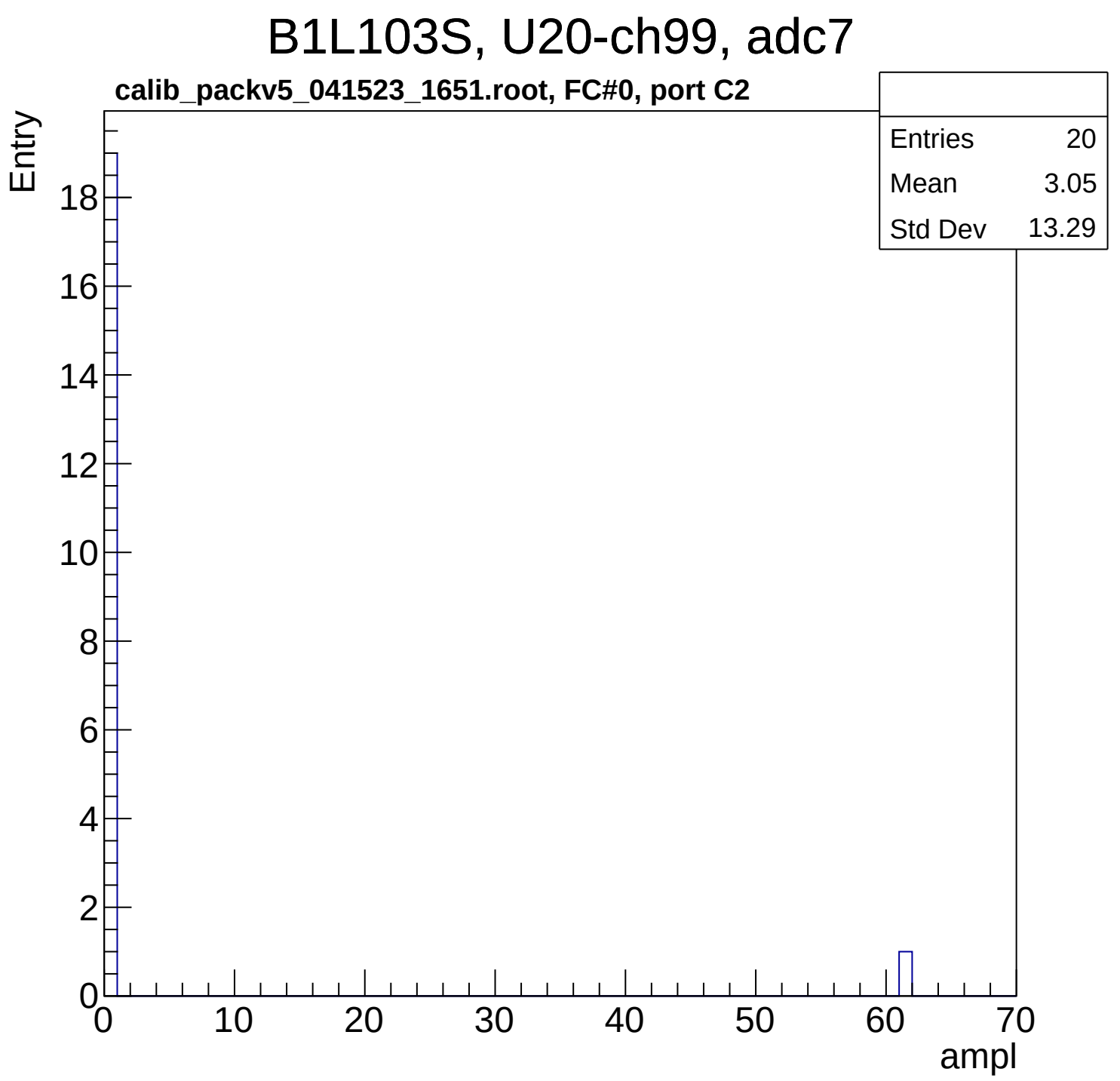
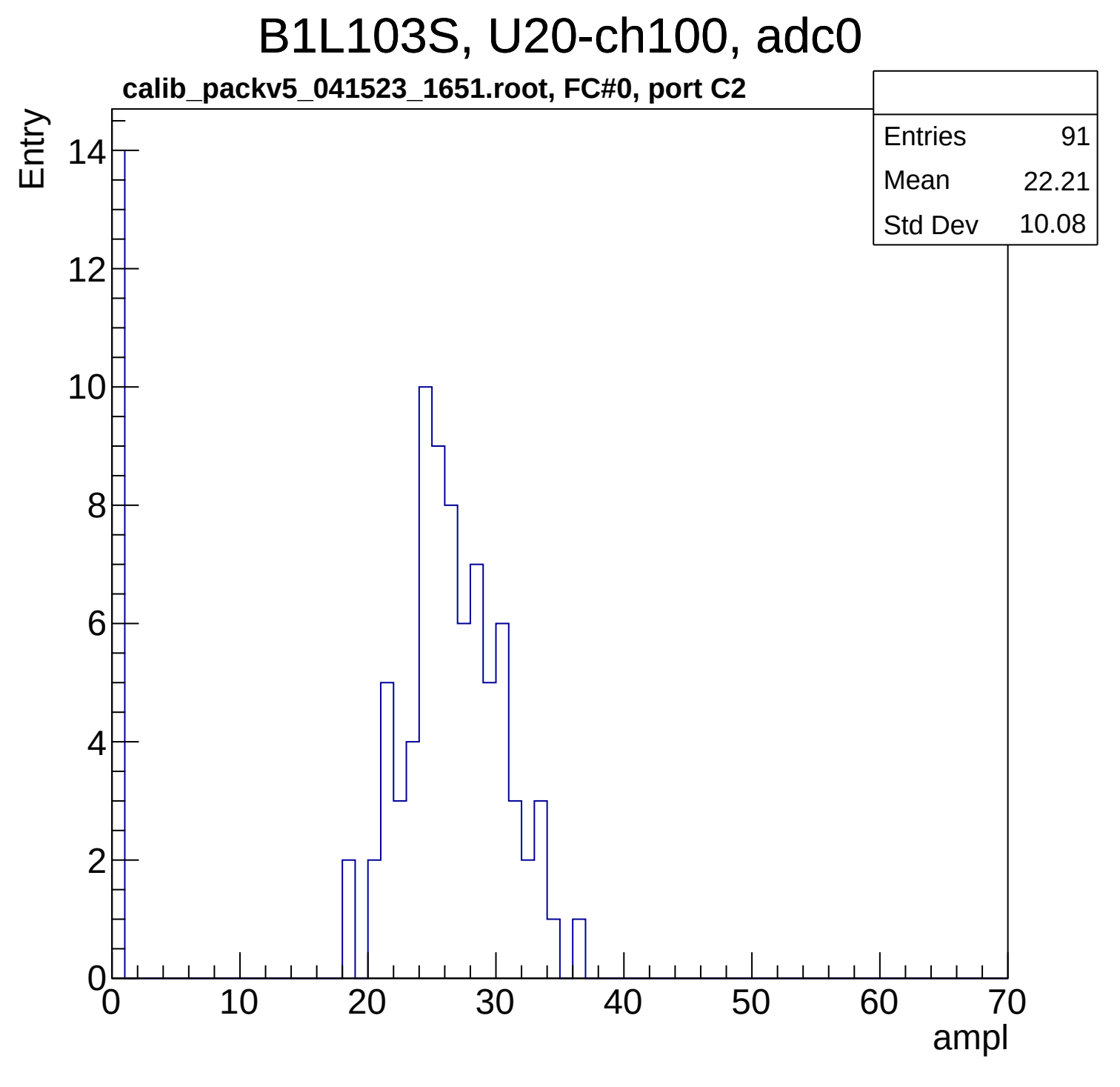

B1L103S, U20-ch99, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.05
Std Dev 13.29
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch100, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 22.21
Std Dev 10.08
Entry
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6
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10
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14
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10
20
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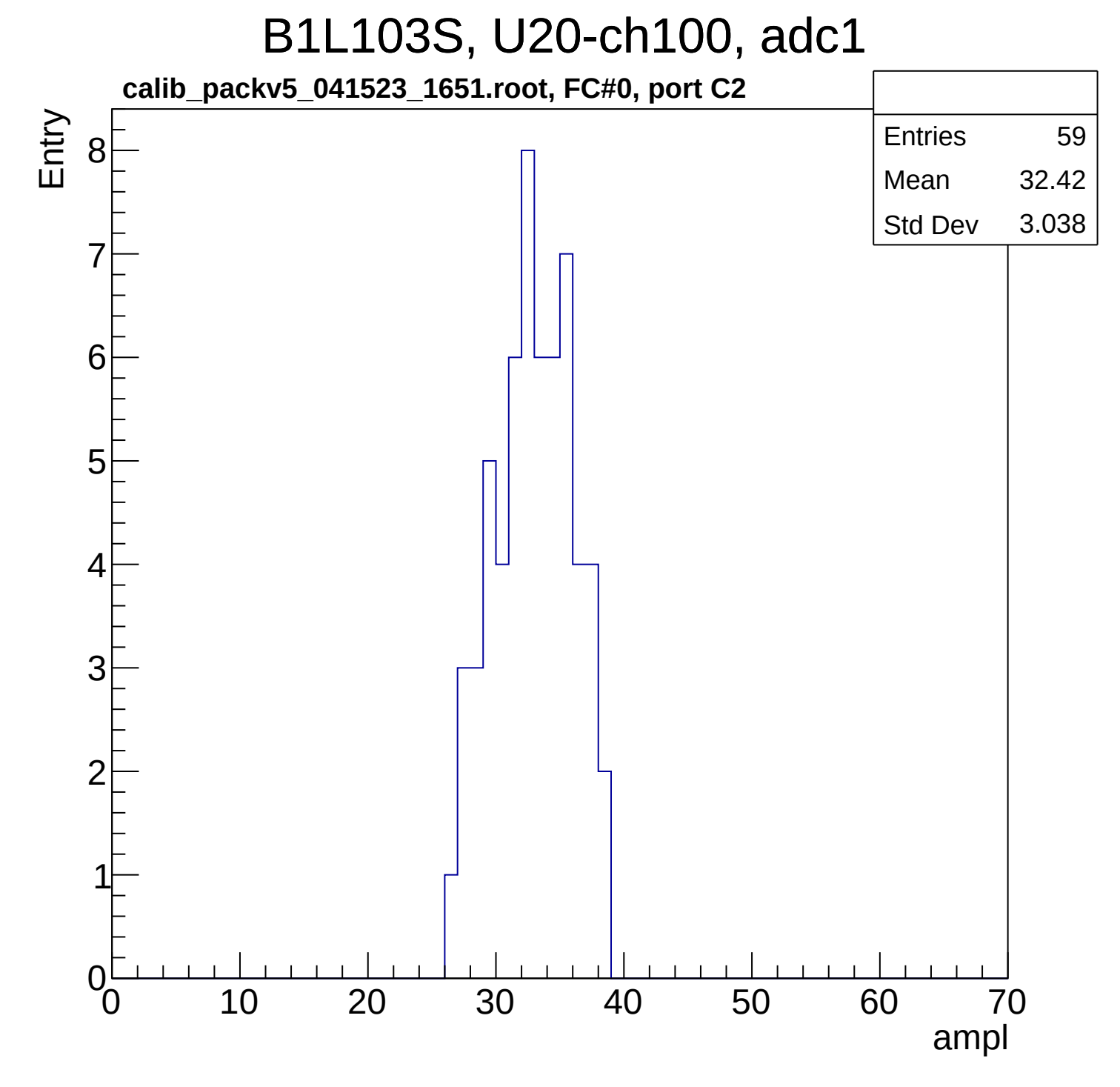
50
60
70
ampl


B1L103S, U20-ch100, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 32.42
Std Dev 3.038
Entry
ampl
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3
4
5
6
7
8
0
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20
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40
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60
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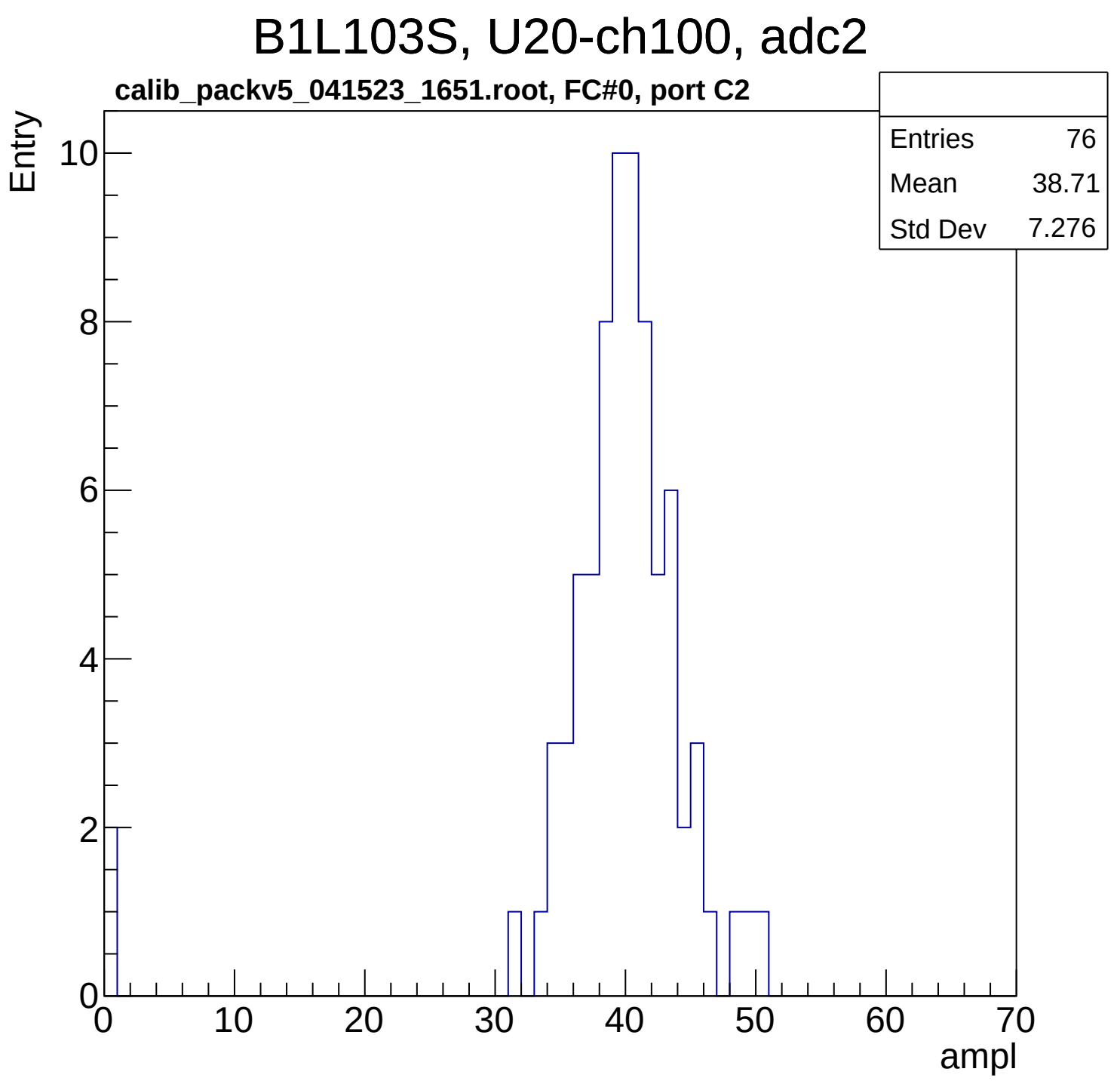
B1L103S, U20-ch100, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 38.71
Std Dev 7.276
Entry
ampl
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8
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0
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20
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40
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60
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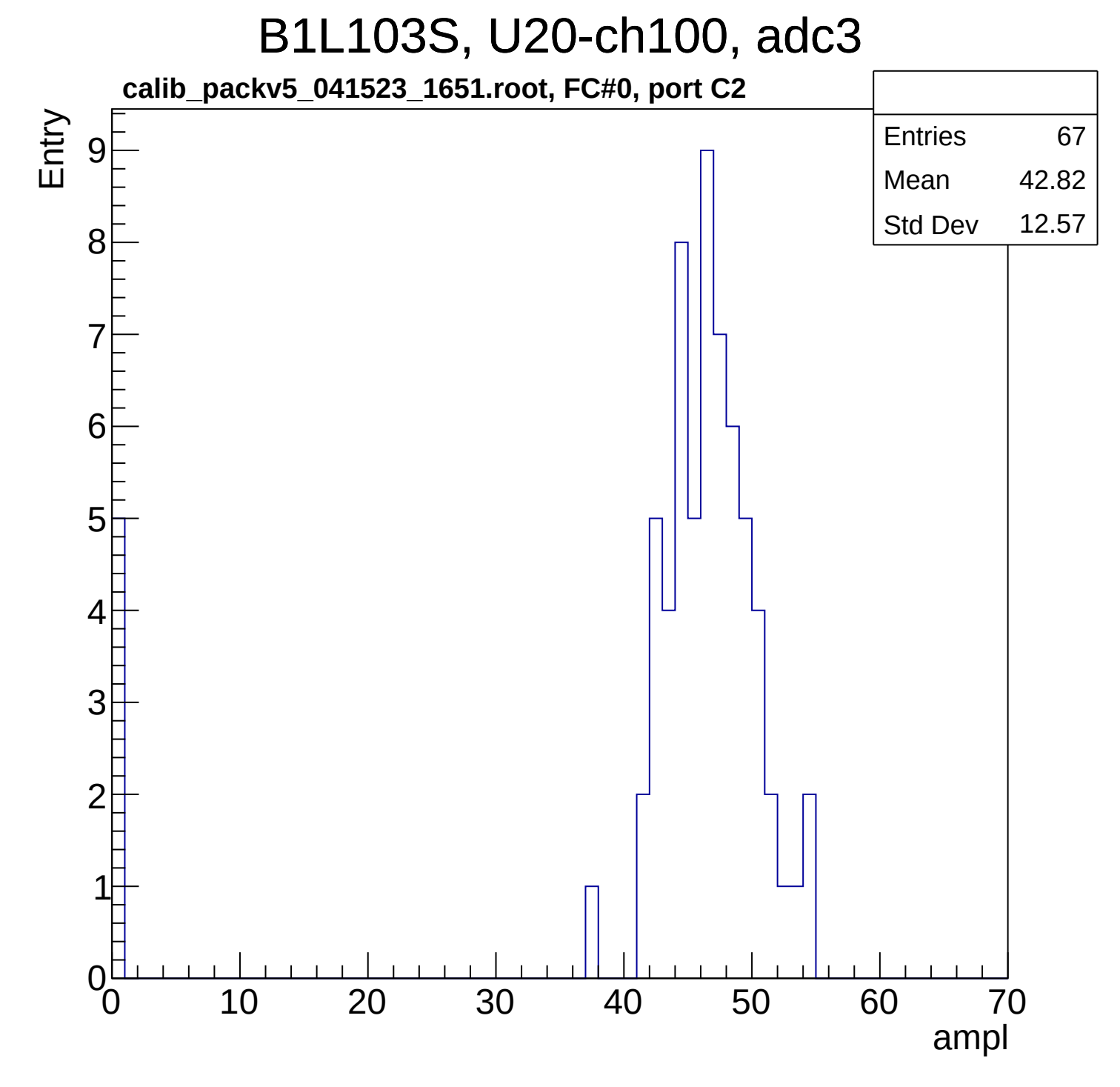
B1L103S, U20-ch100, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 42.82
Std Dev 12.57
Entry
ampl
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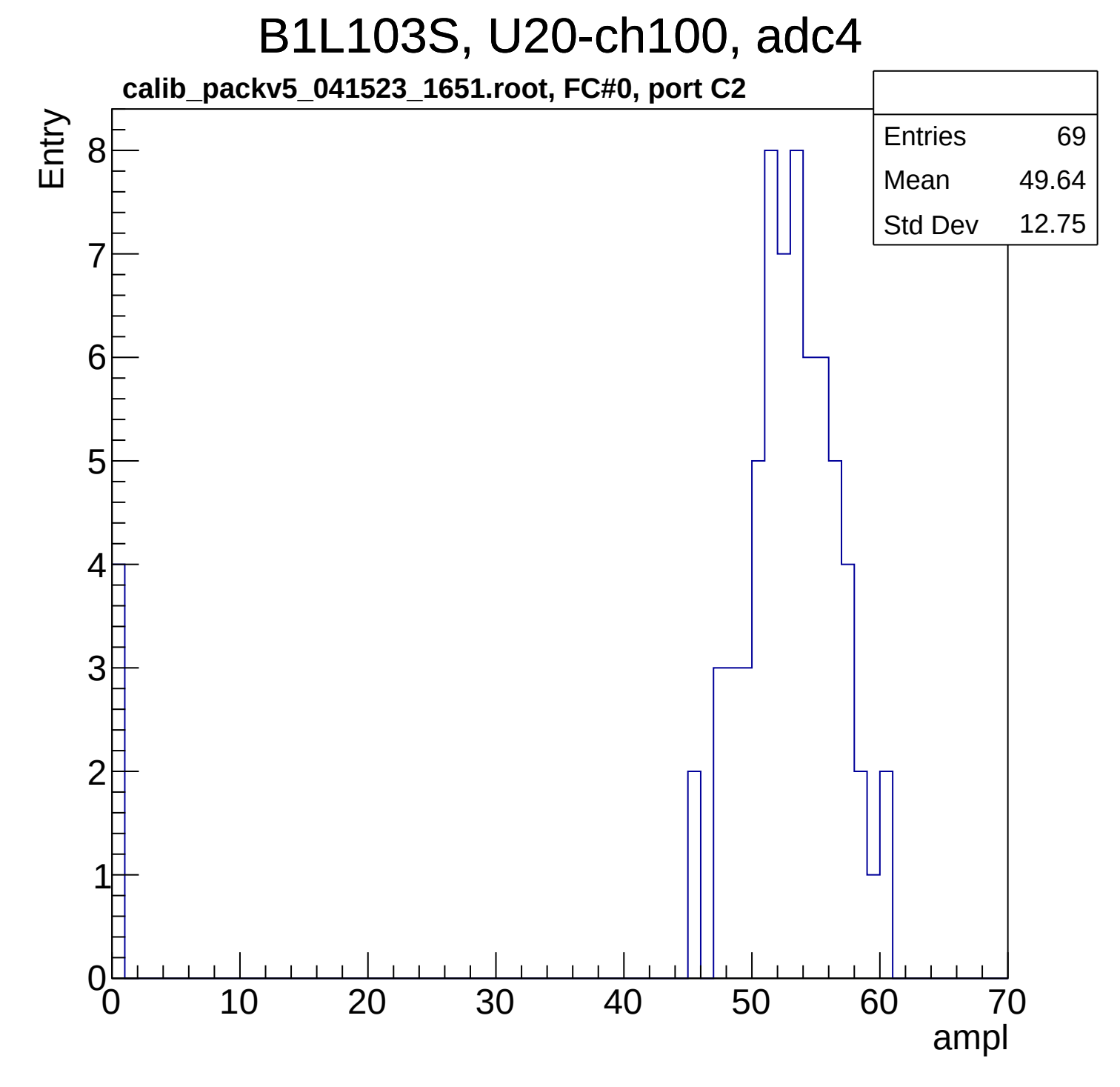
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L103S, U20-ch100, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 49.64
Std Dev 12.75
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
50
60
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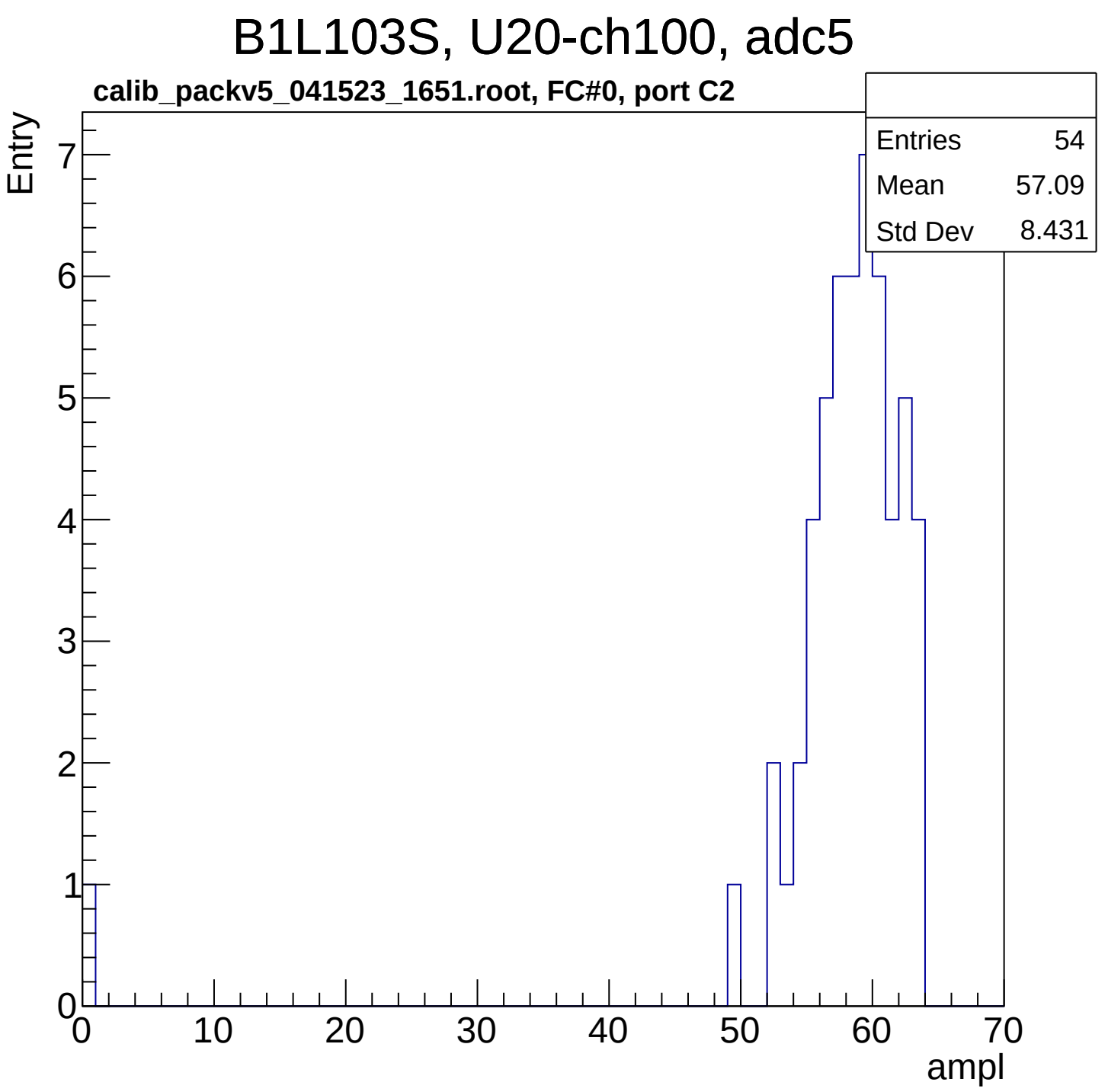
B1L103S, U20-ch100, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 57.09
Std Dev 8.431
Entry
ampl
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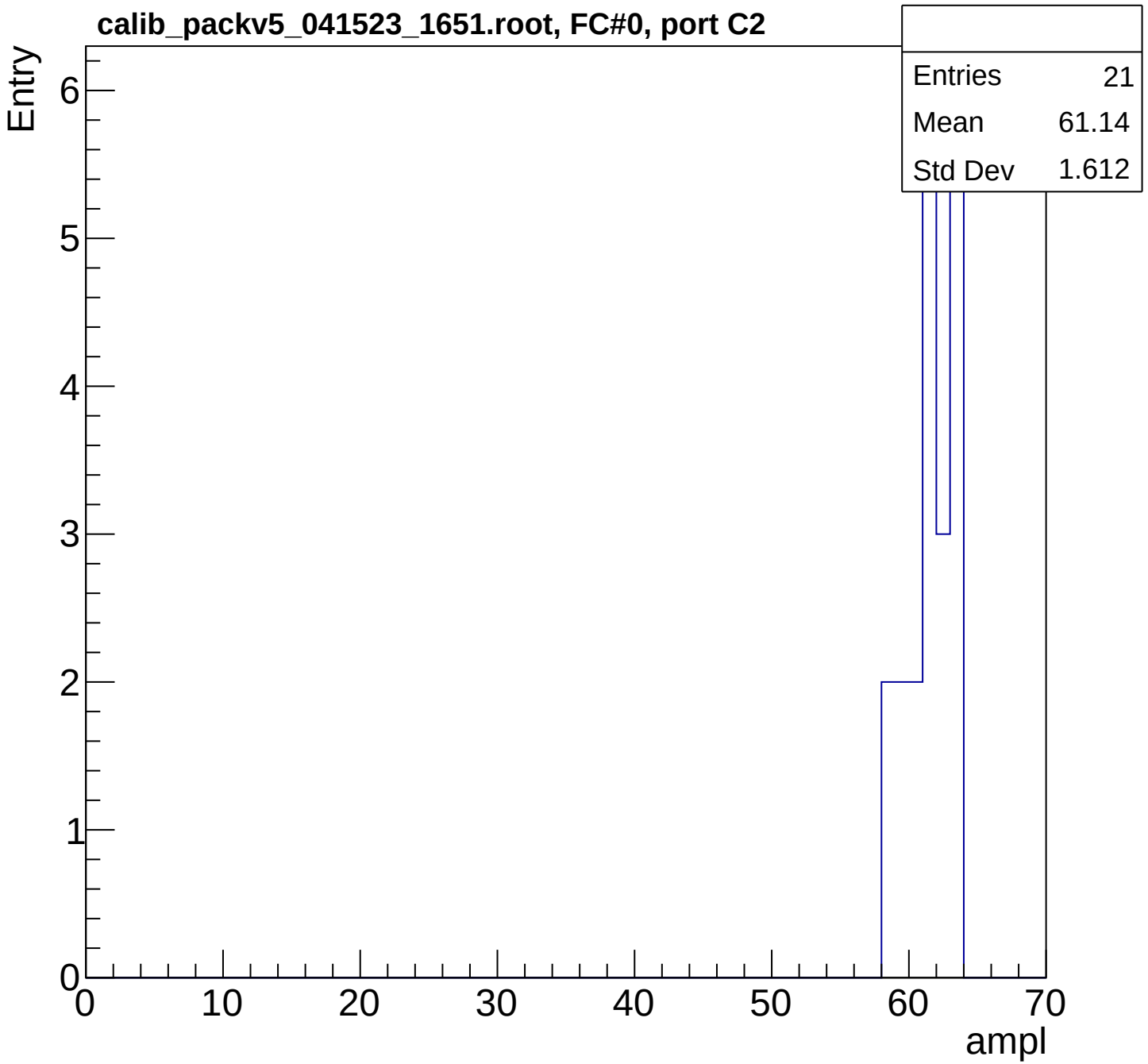
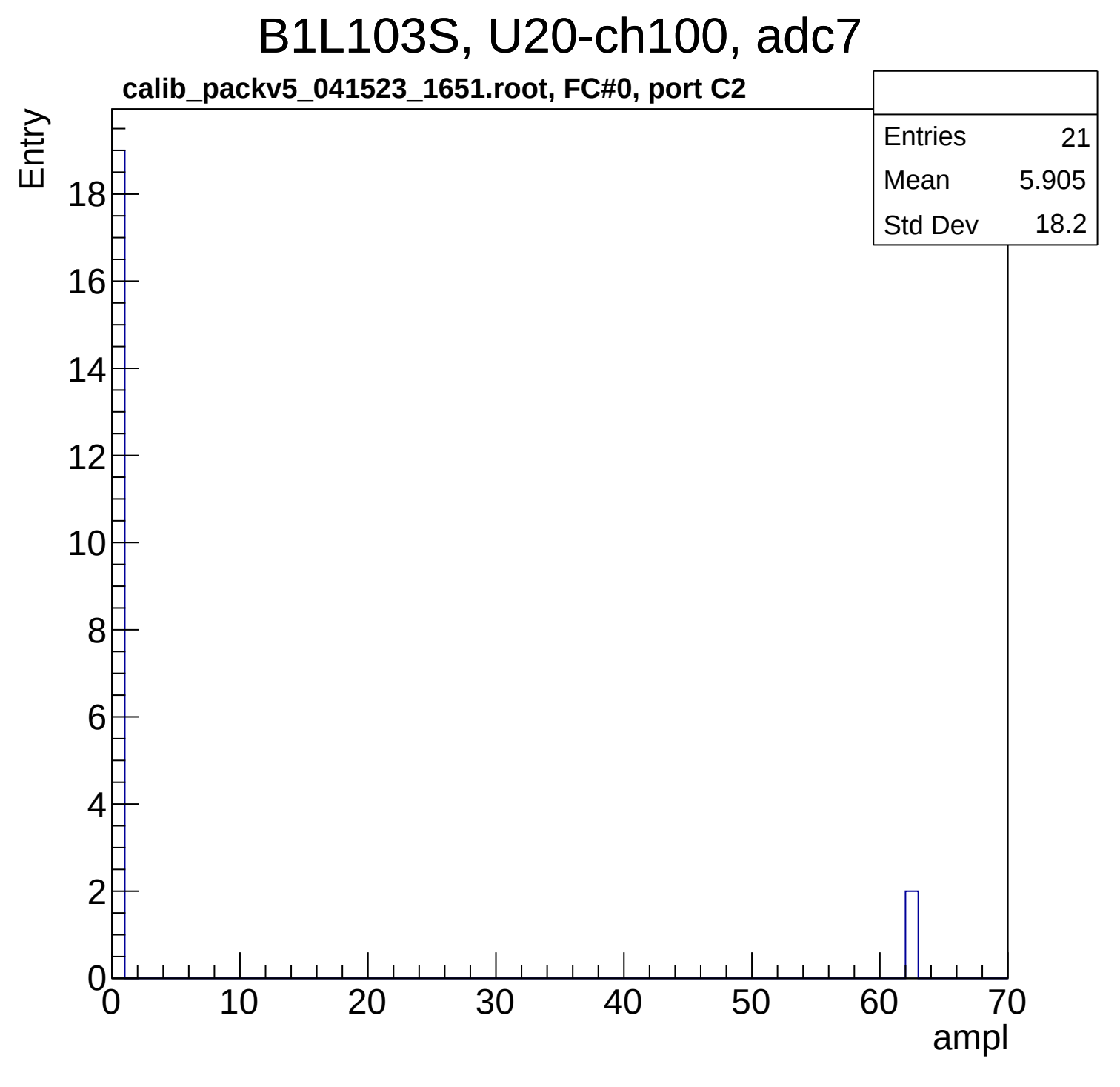
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U20-ch100, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 61.14
Std Dev 1.612
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U20-ch100, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.905
Std Dev 18.2
Entry
ampl
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4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
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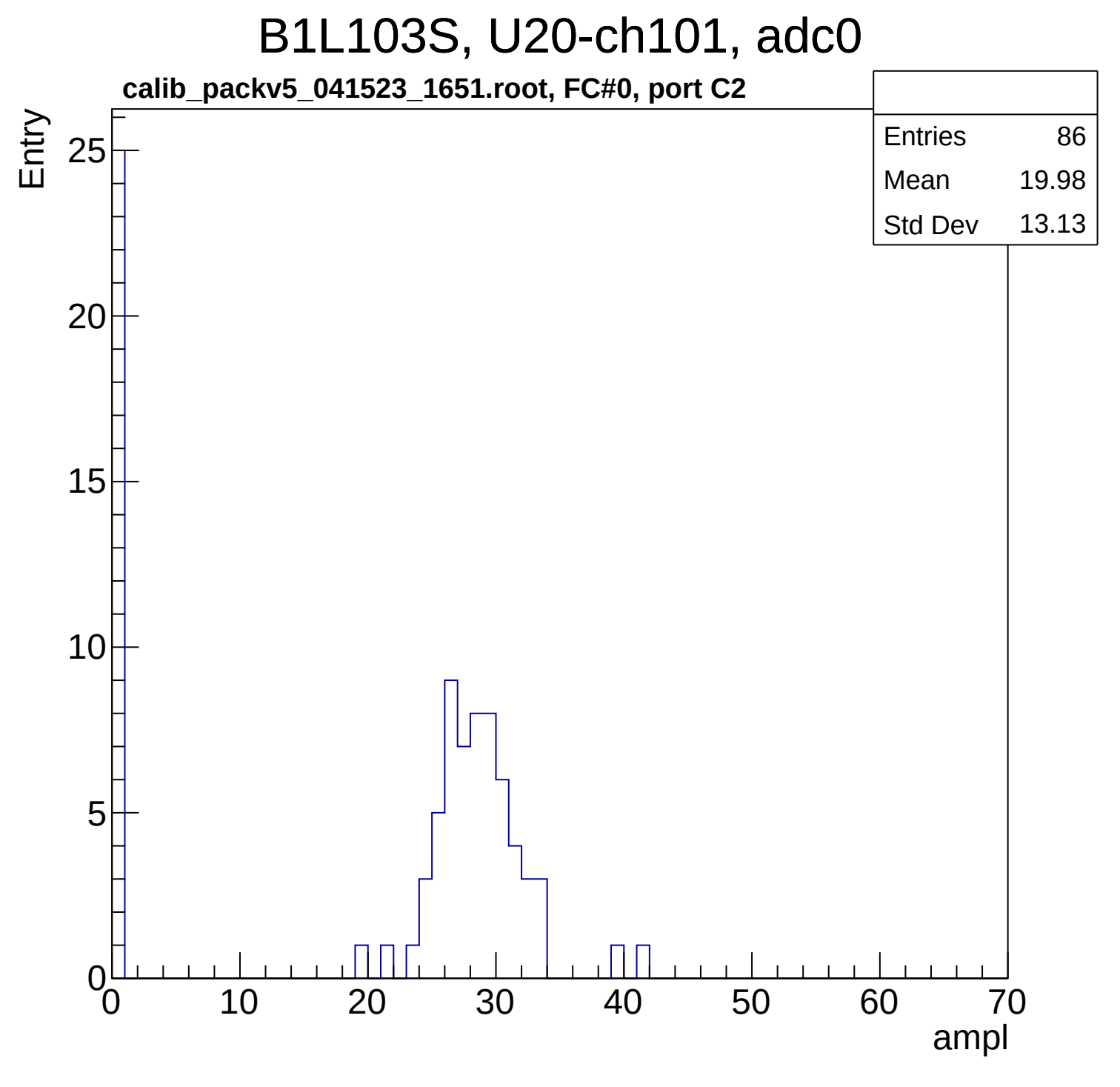
B1L103S, U20-ch101, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 19.98
Std Dev 13.13
Entry
0
5
10
15
20
25
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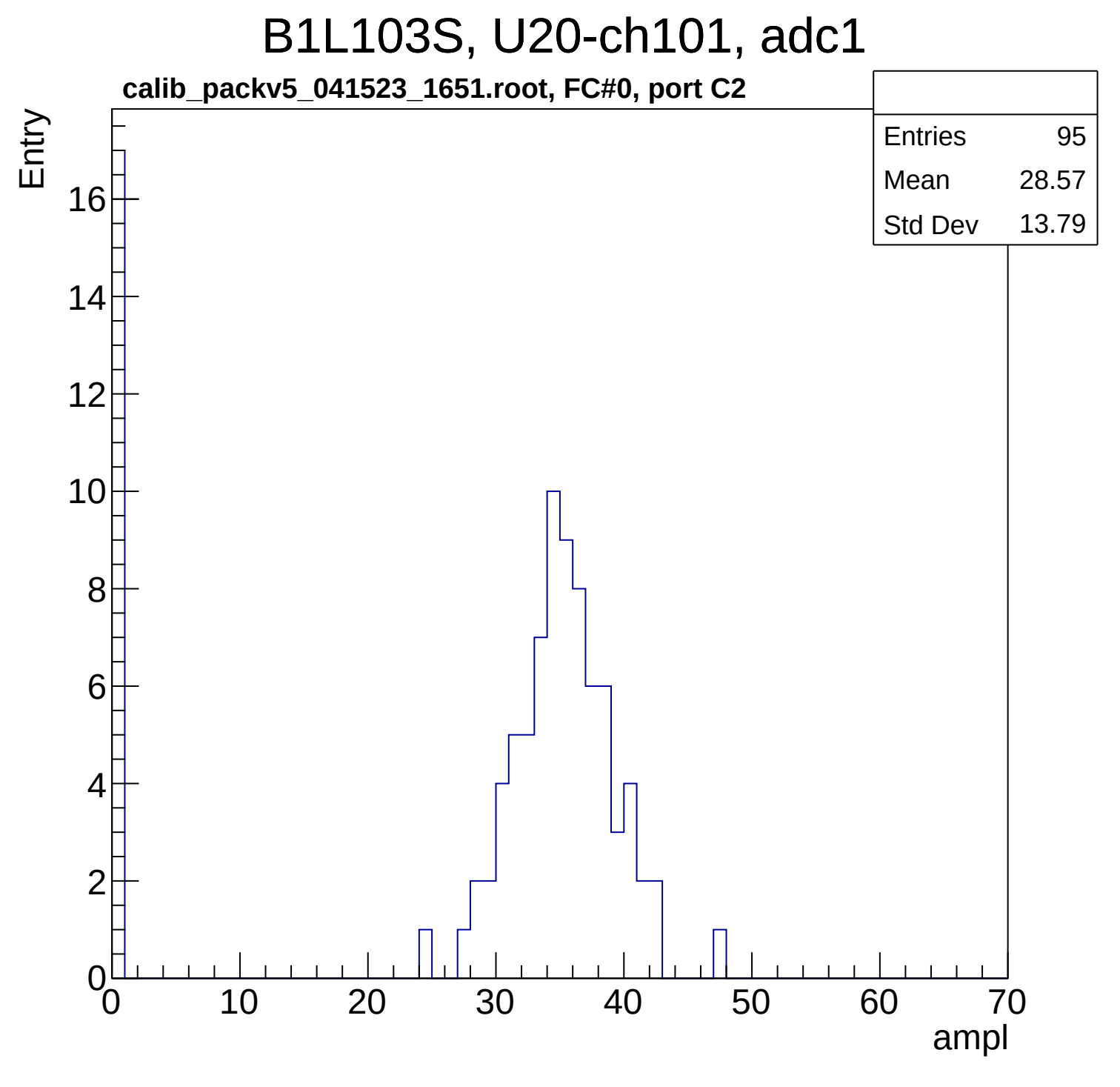
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch101, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 28.57
Std Dev 13.79
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
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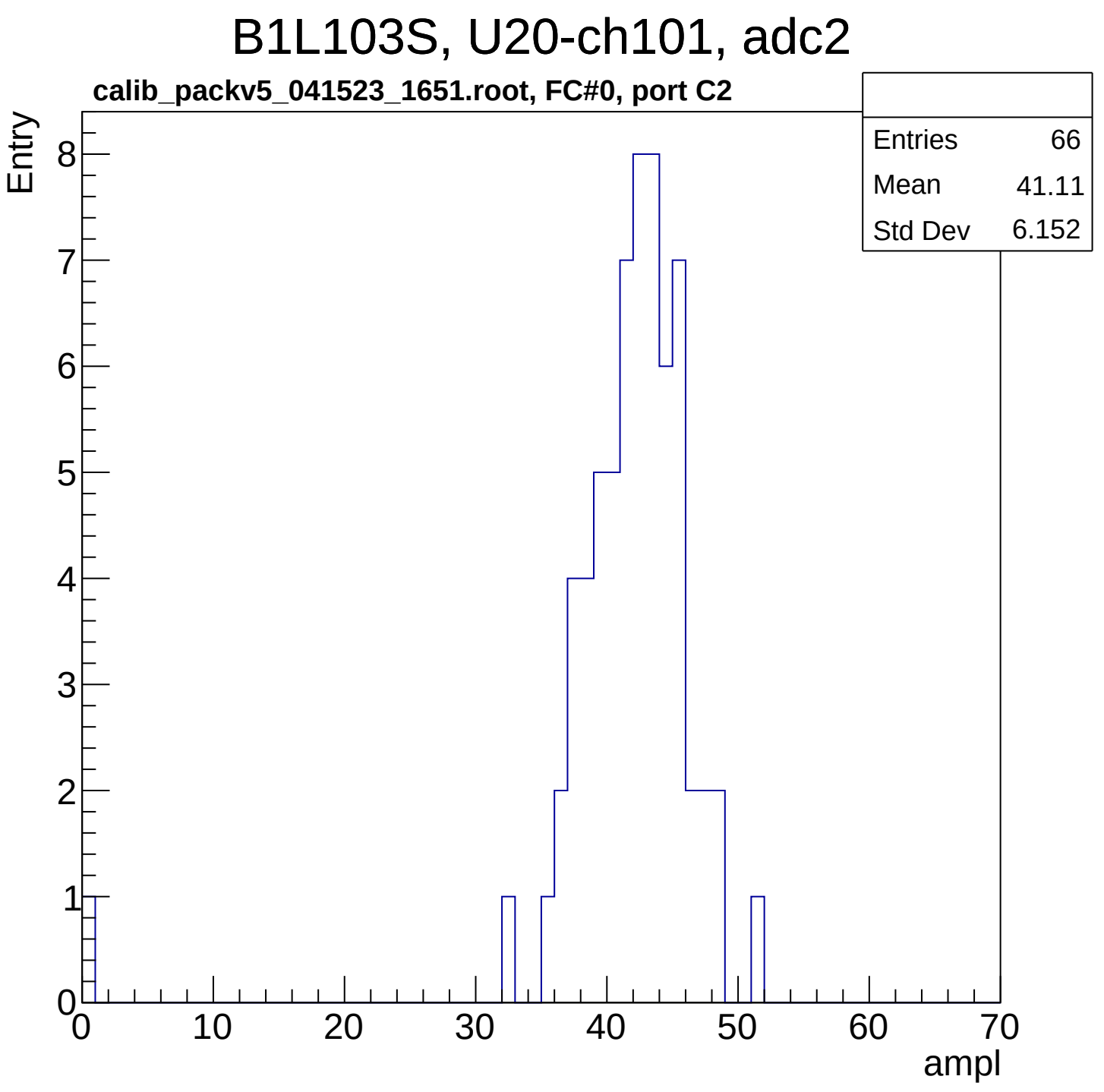
B1L103S, U20-ch101, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 41.11
Std Dev 6.152
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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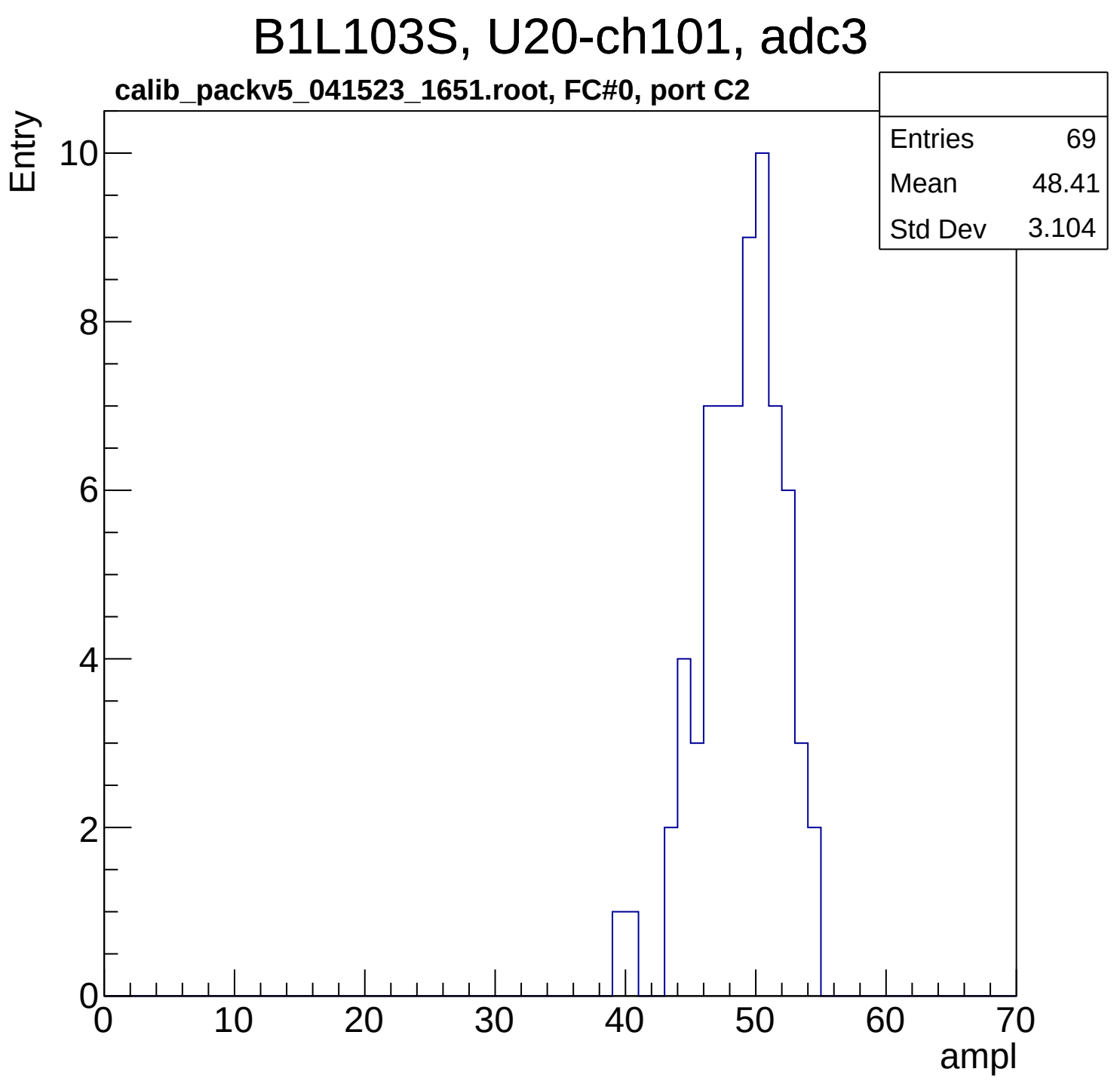
B1L103S, U20-ch101, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 48.41
Std Dev 3.104
Entry
ampl
0
2
4
6
8
10
0
10
20
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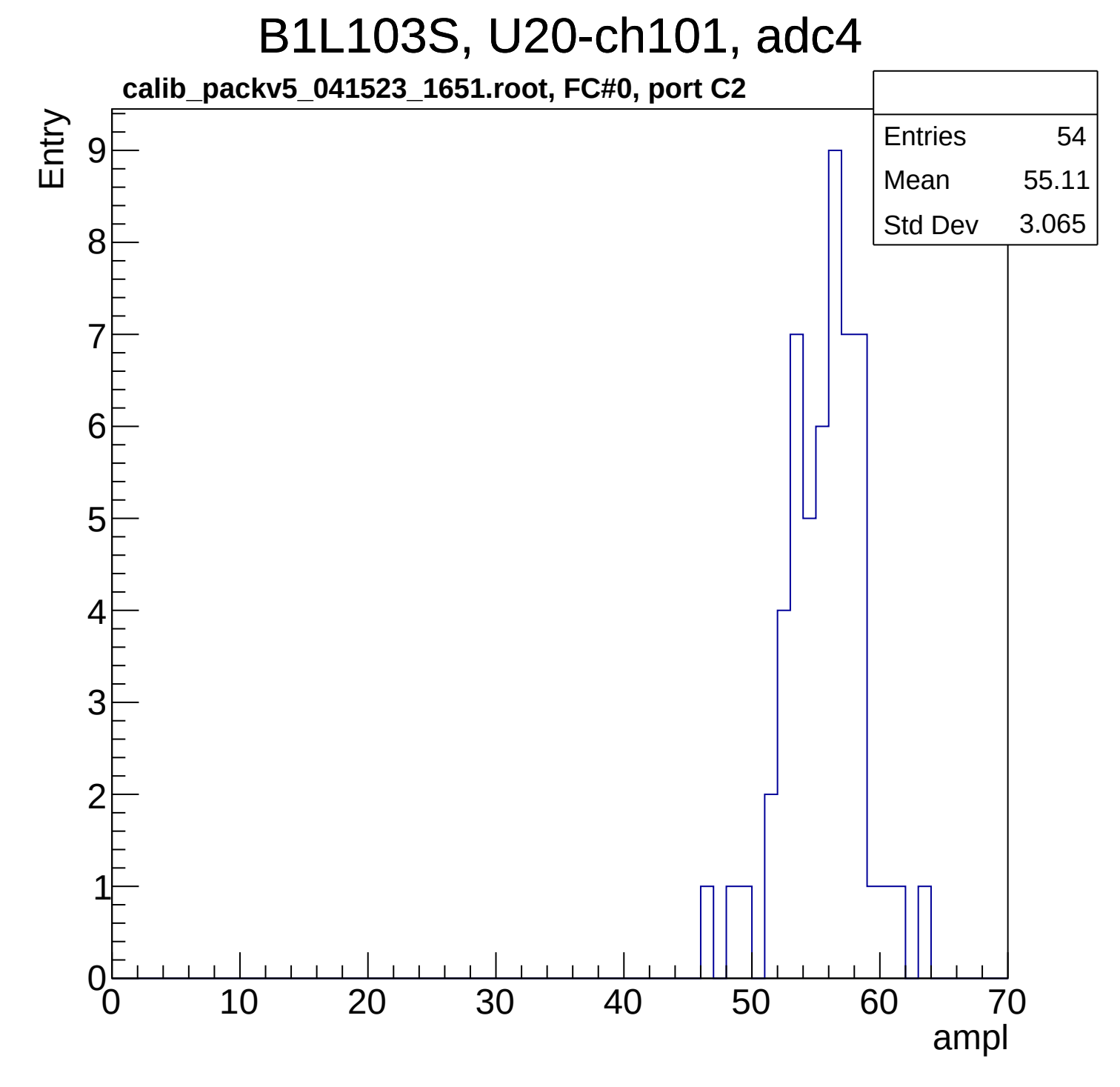
40
50
60
70


B1L103S, U20-ch101, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 55.11
Std Dev 3.065
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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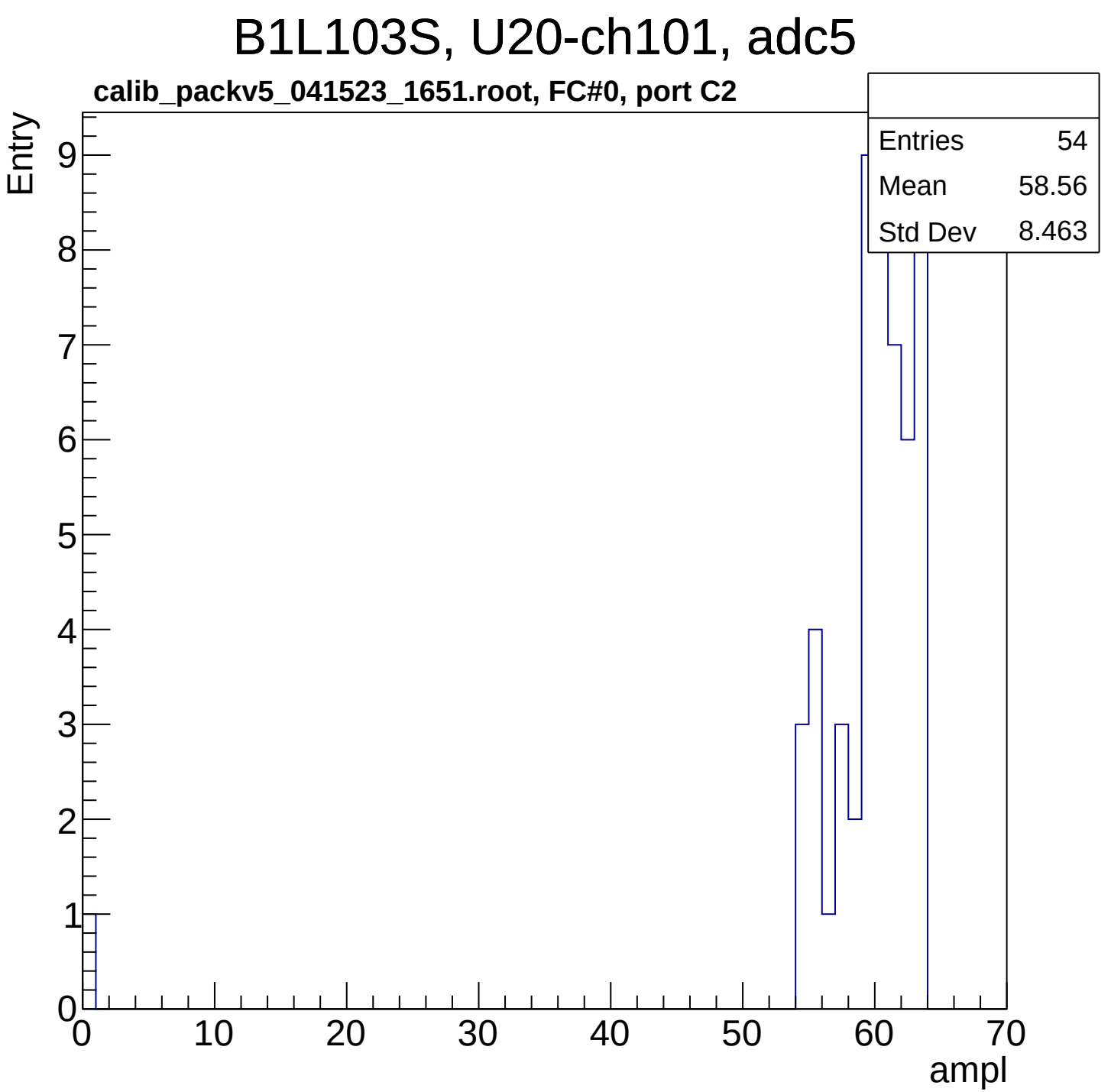
B1L103S, U20-ch101, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 58.56
Std Dev 8.463
Entry
ampl
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4
5
6
7
8
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0
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60
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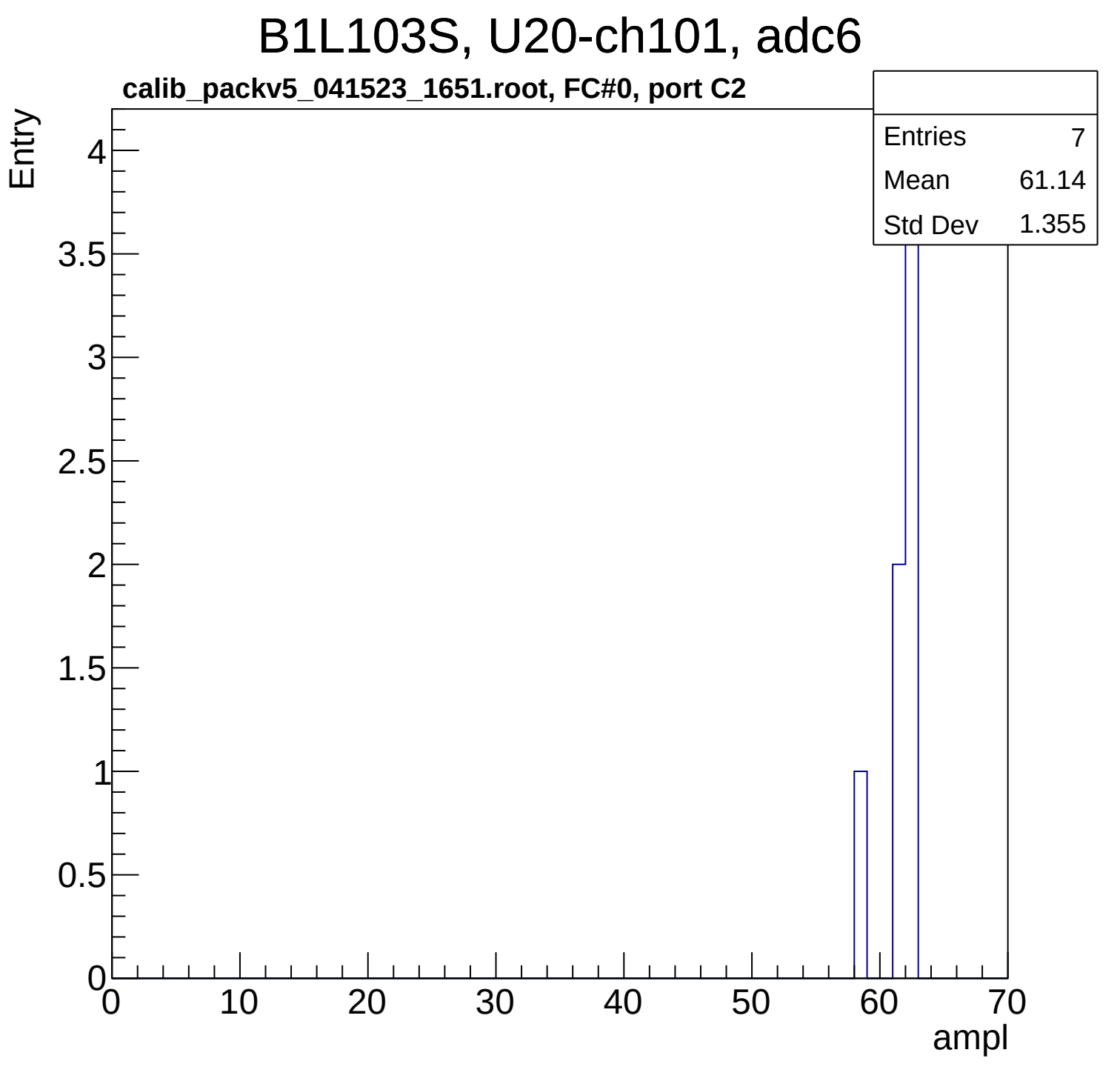
B1L103S, U20-ch101, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 61.14
Std Dev 1.355
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
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20
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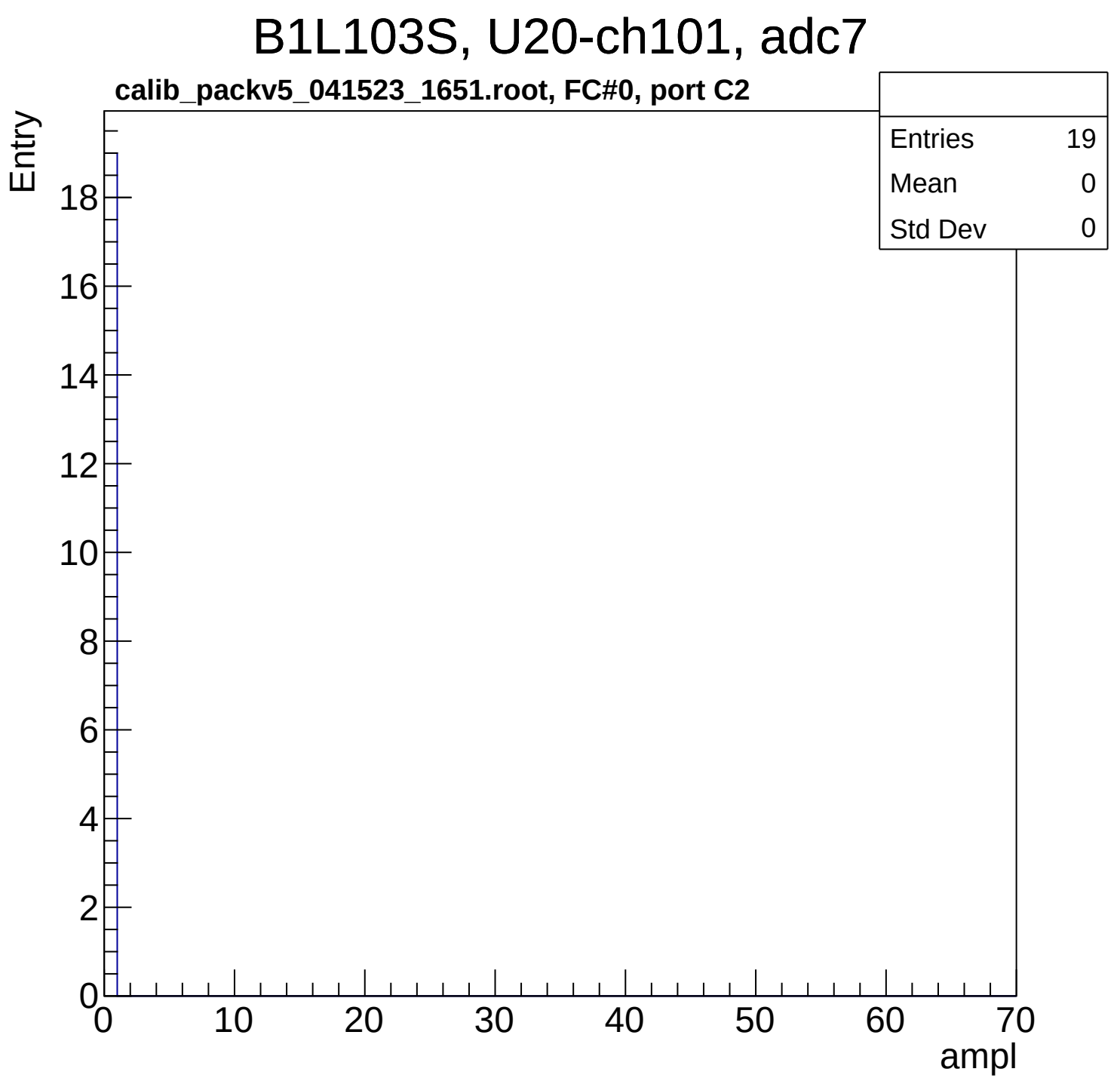
40
50
60
70


B1L103S, U20-ch101, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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2
4
6
8
10
12
14
16
18
0
10
20
30
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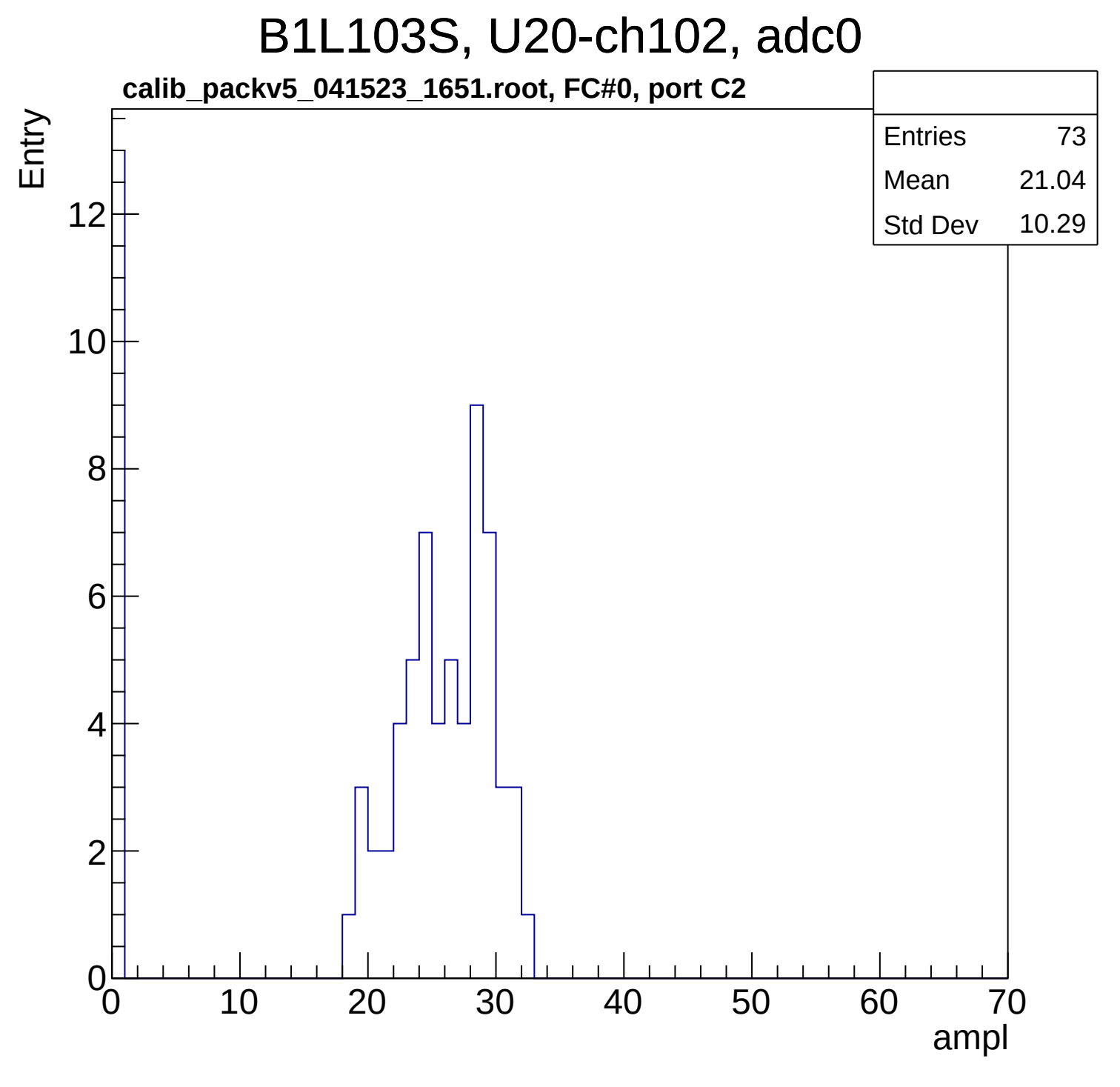
50
60
70
ampl


B1L103S, U20-ch102, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 21.04
Std Dev 10.29
Entry
0
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4
6
8
10
12
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10
20
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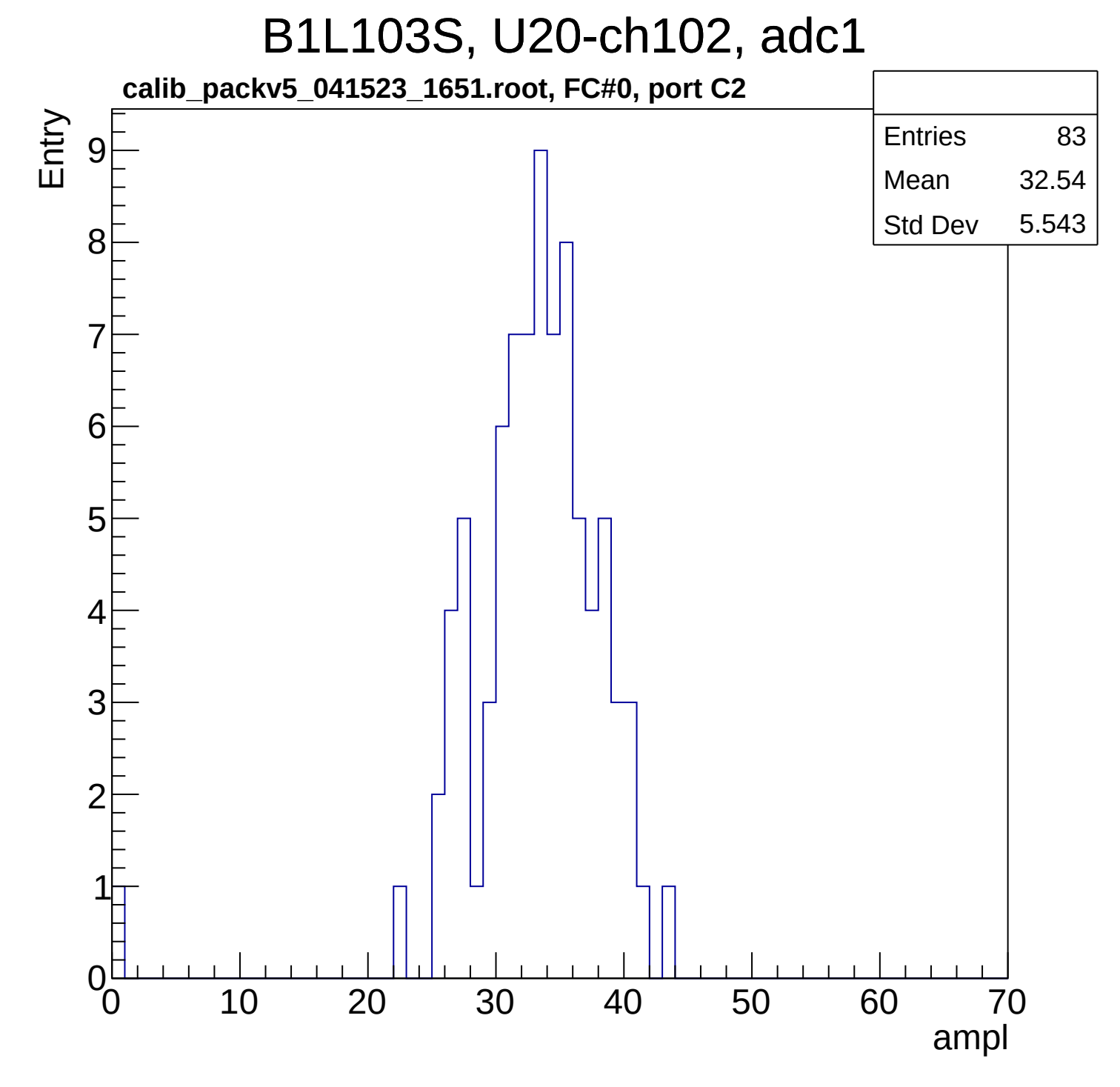
60
70
ampl


B1L103S, U20-ch102, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 32.54
Std Dev 5.543
Entry
ampl
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4
5
6
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0
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60
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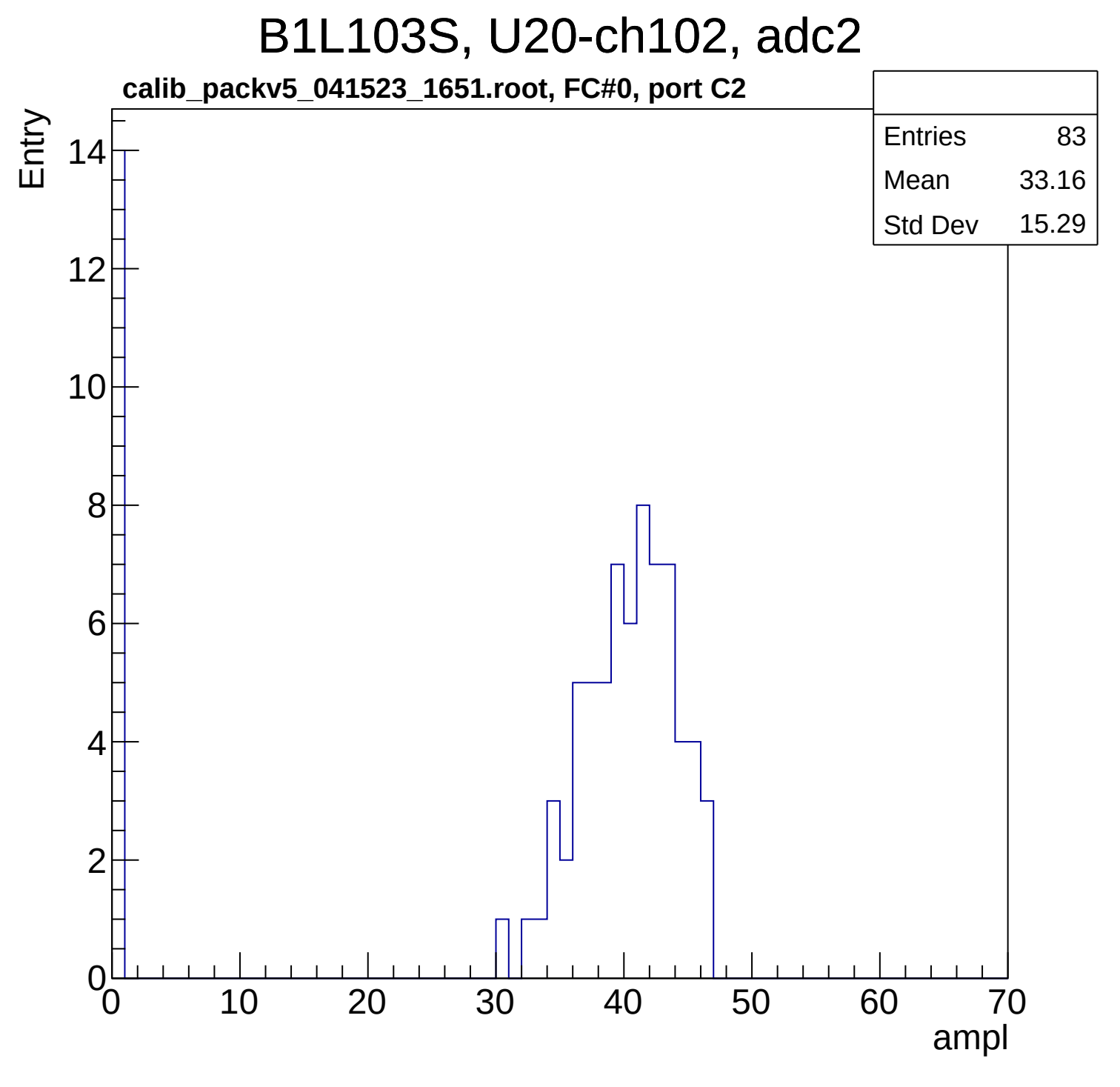
B1L103S, U20-ch102, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 33.16
Std Dev 15.29
Entry
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2
4
6
8
10
12
14
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10
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30
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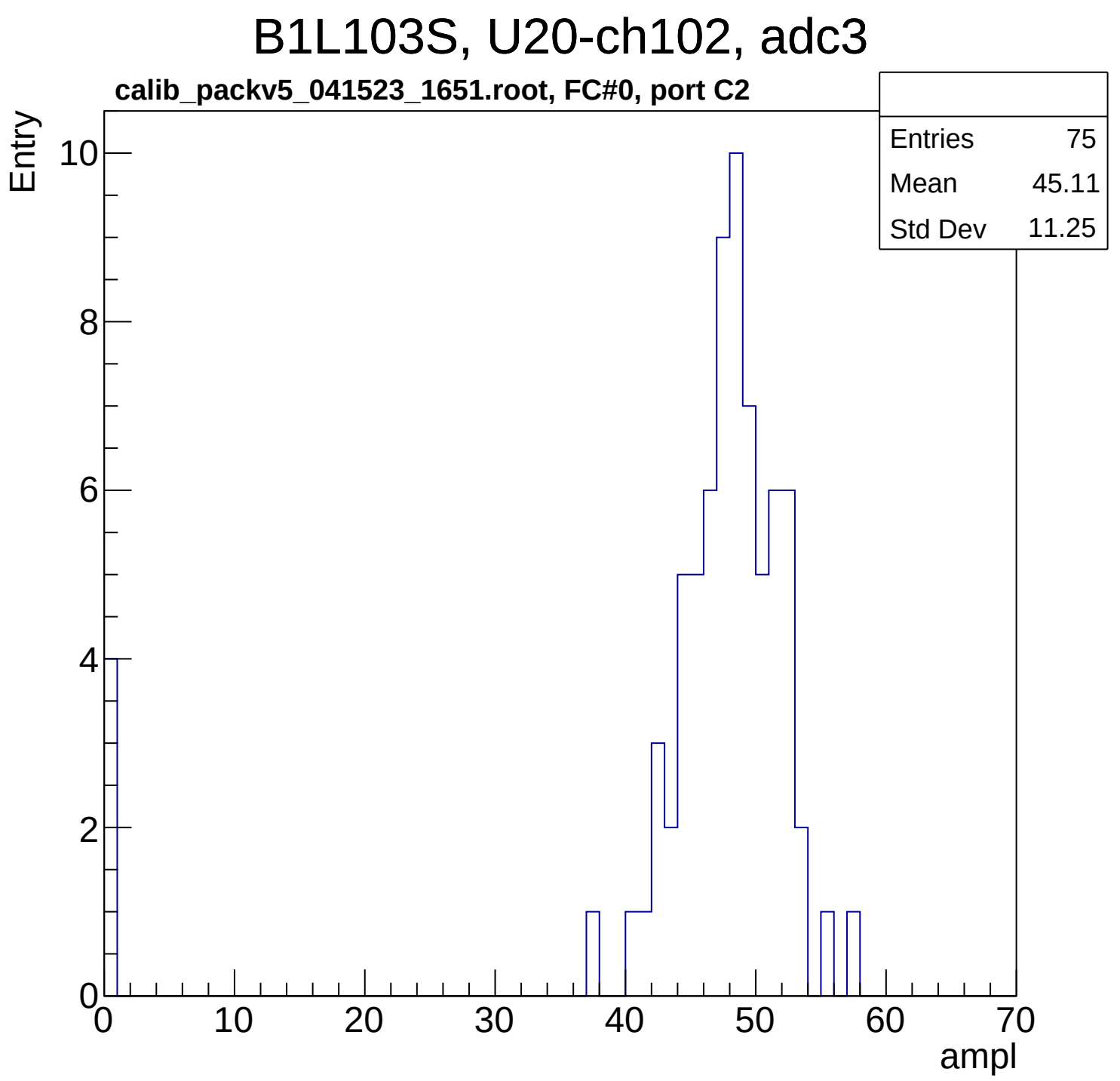
50
60
70
ampl


B1L103S, U20-ch102, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 45.11
Std Dev 11.25
Entry
ampl
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4
6
8
10
0
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20
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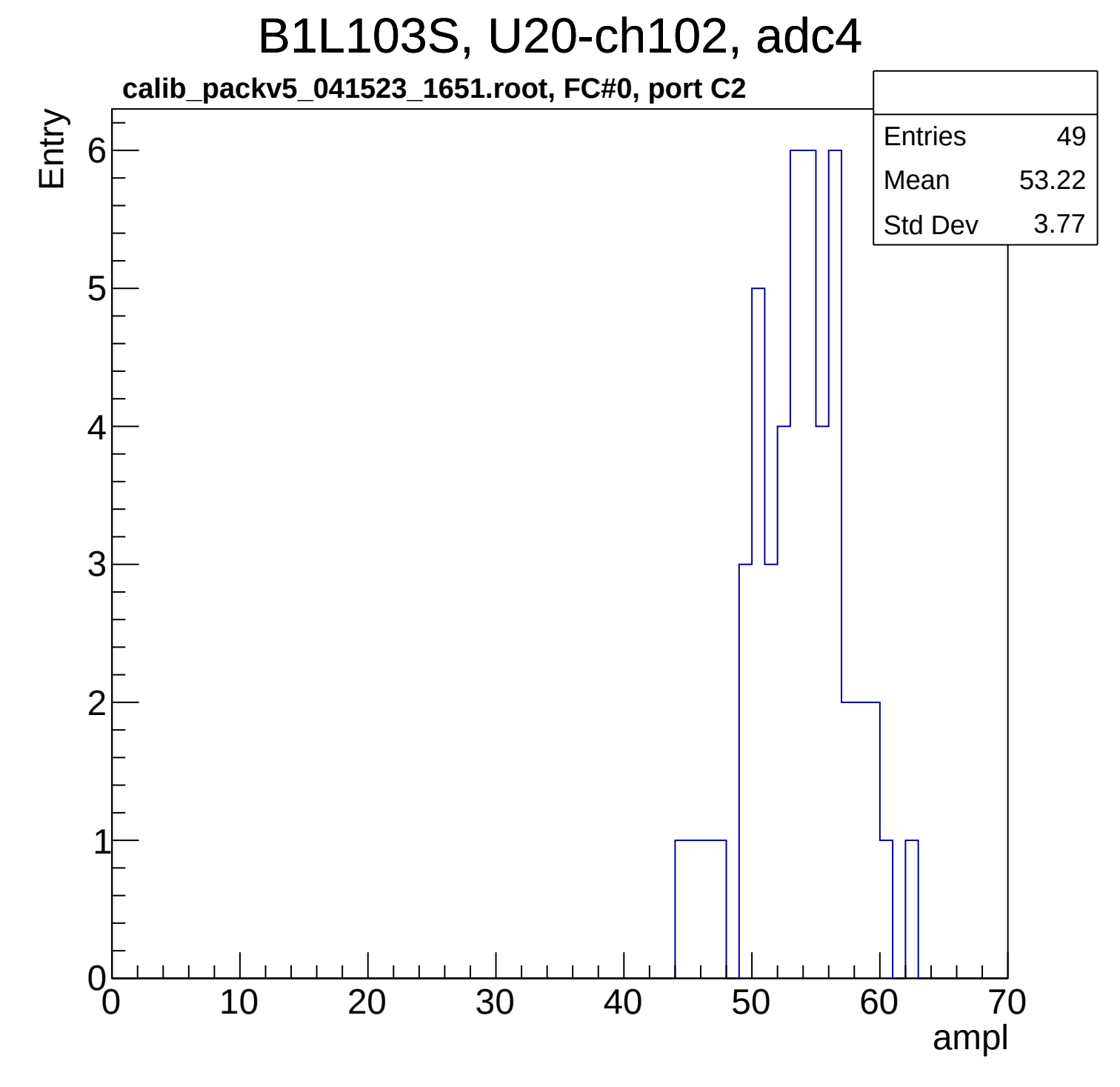
50
60
70


B1L103S, U20-ch102, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 53.22
Std Dev 3.77
Entry
ampl
0
1
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3
4
5
6
0
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20
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40
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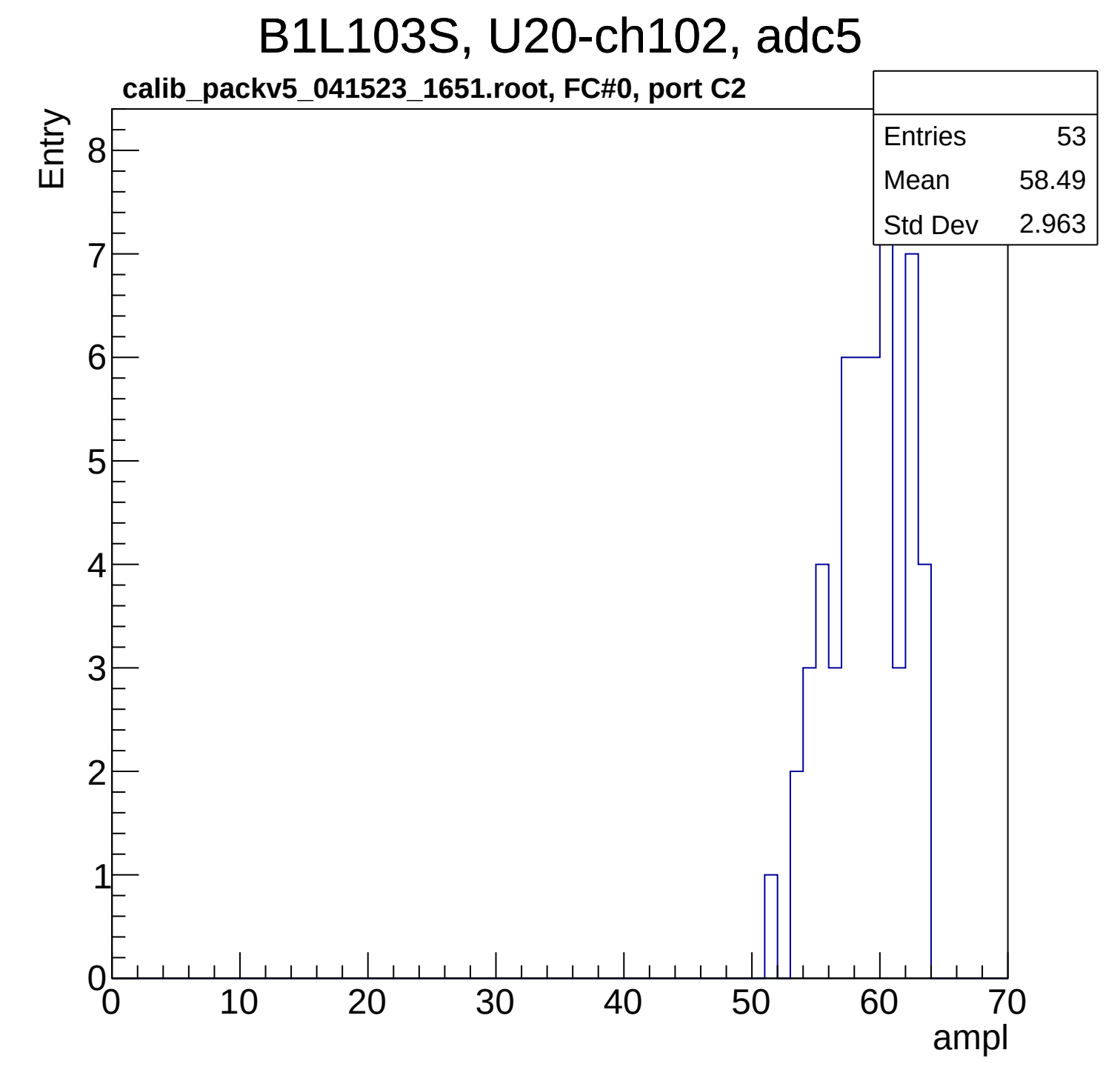
60
70


B1L103S, U20-ch102, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 58.49
Std Dev 2.963
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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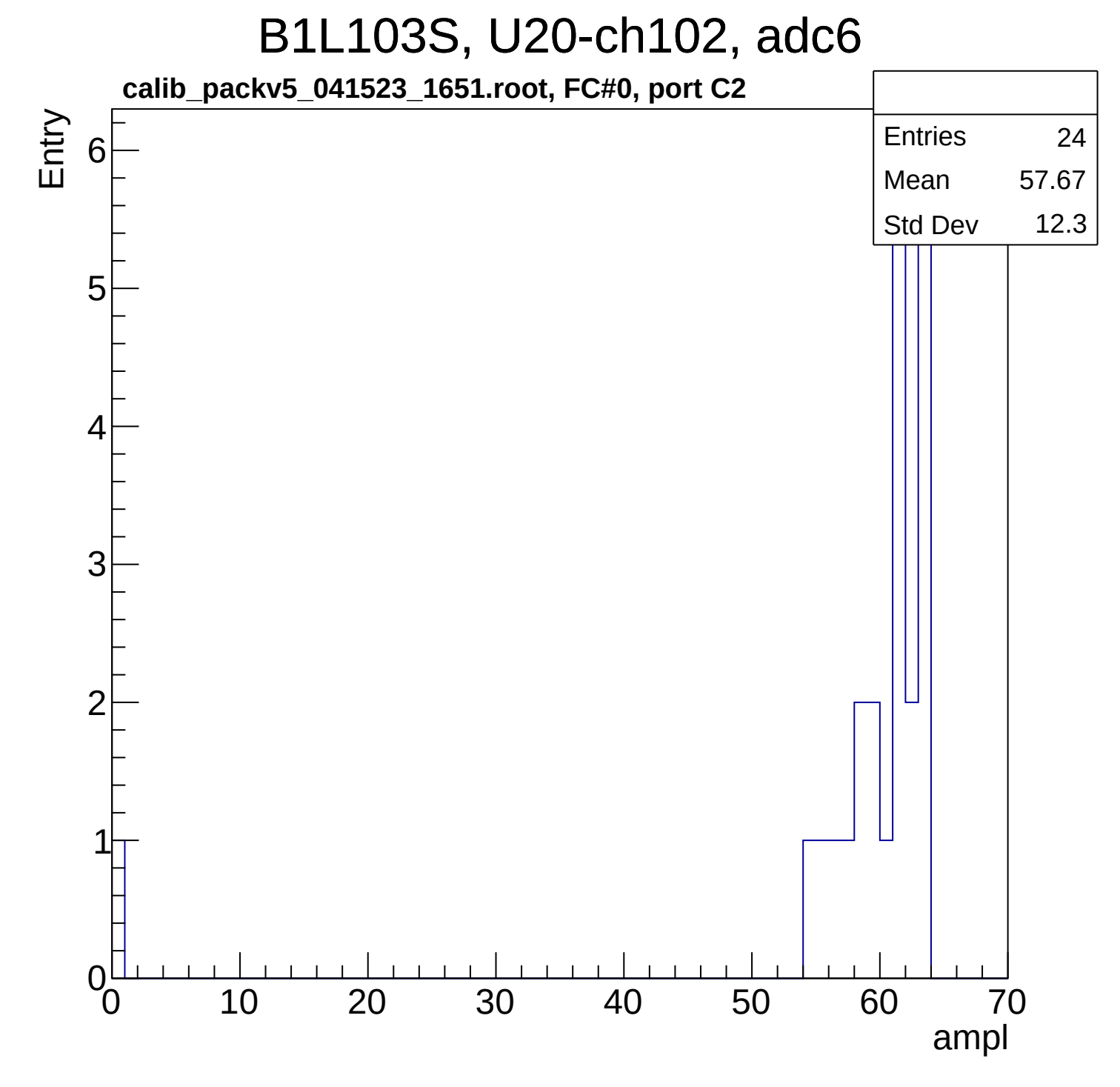
B1L103S, U20-ch102, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 57.67
Std Dev 12.3
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
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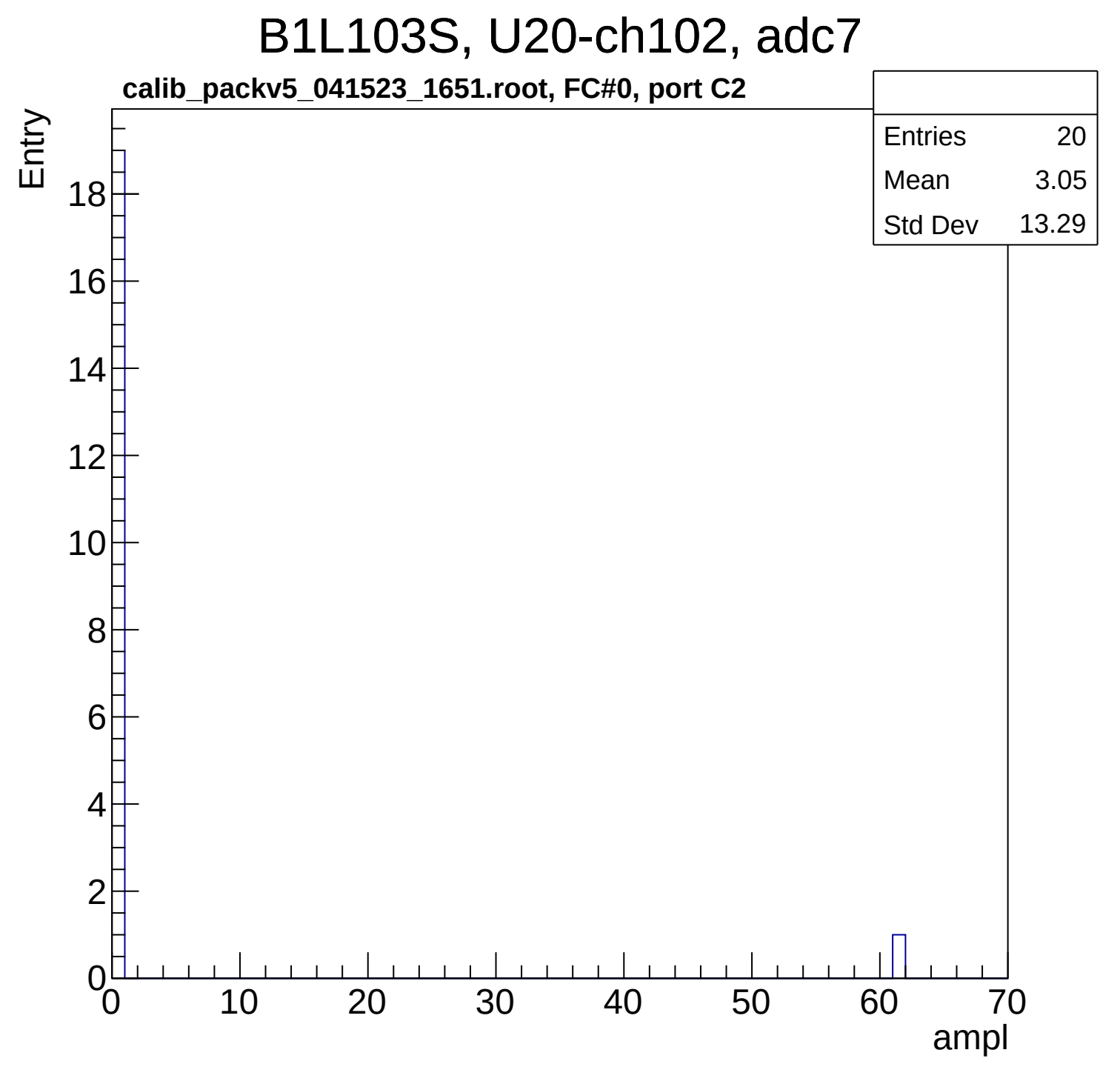
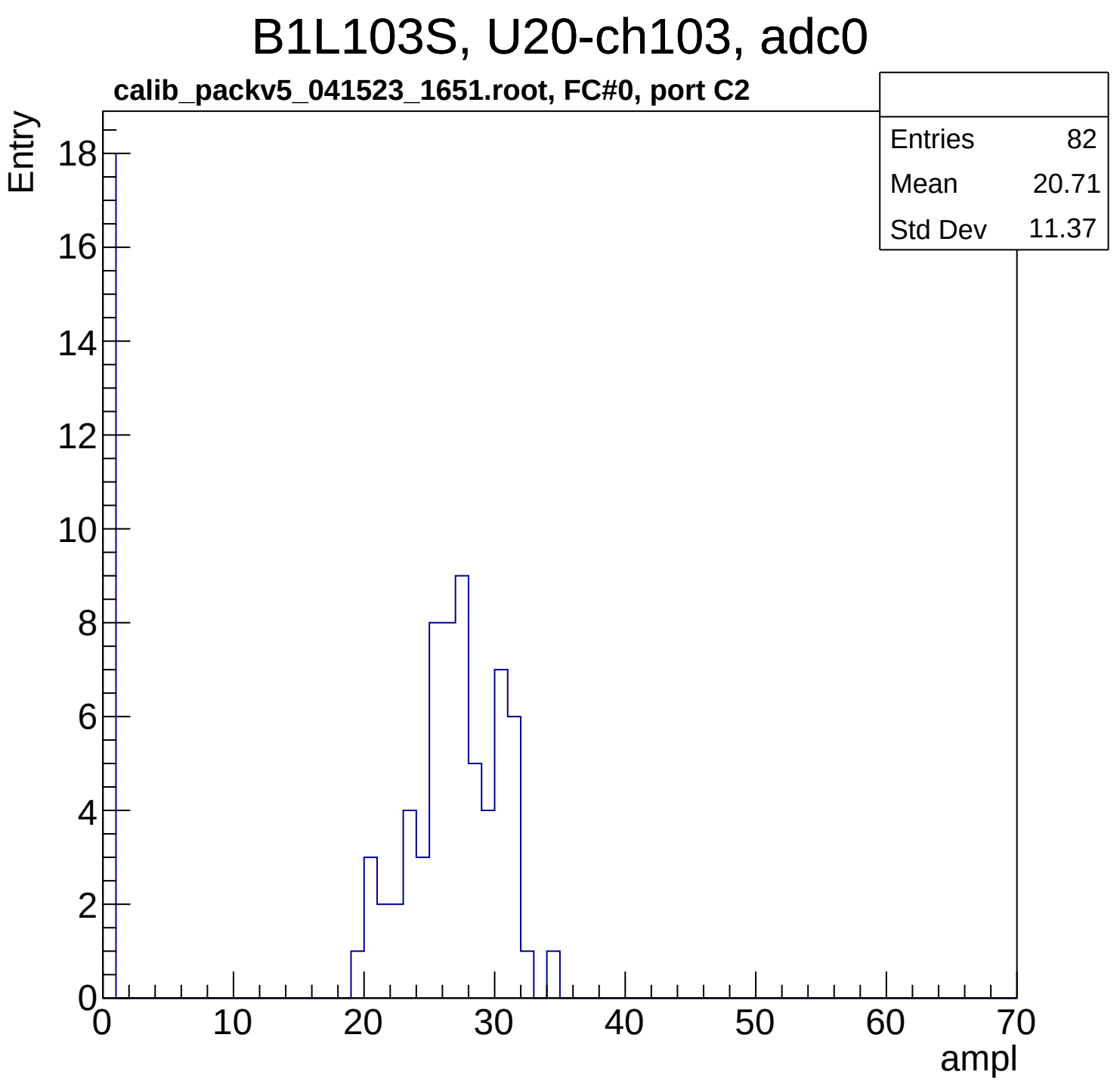

B1L103S, U20-ch102, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.05
Std Dev 13.29
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch103, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 20.71
Std Dev 11.37
Entry
ampl
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4
6
8
10
12
14
16
18
0
10
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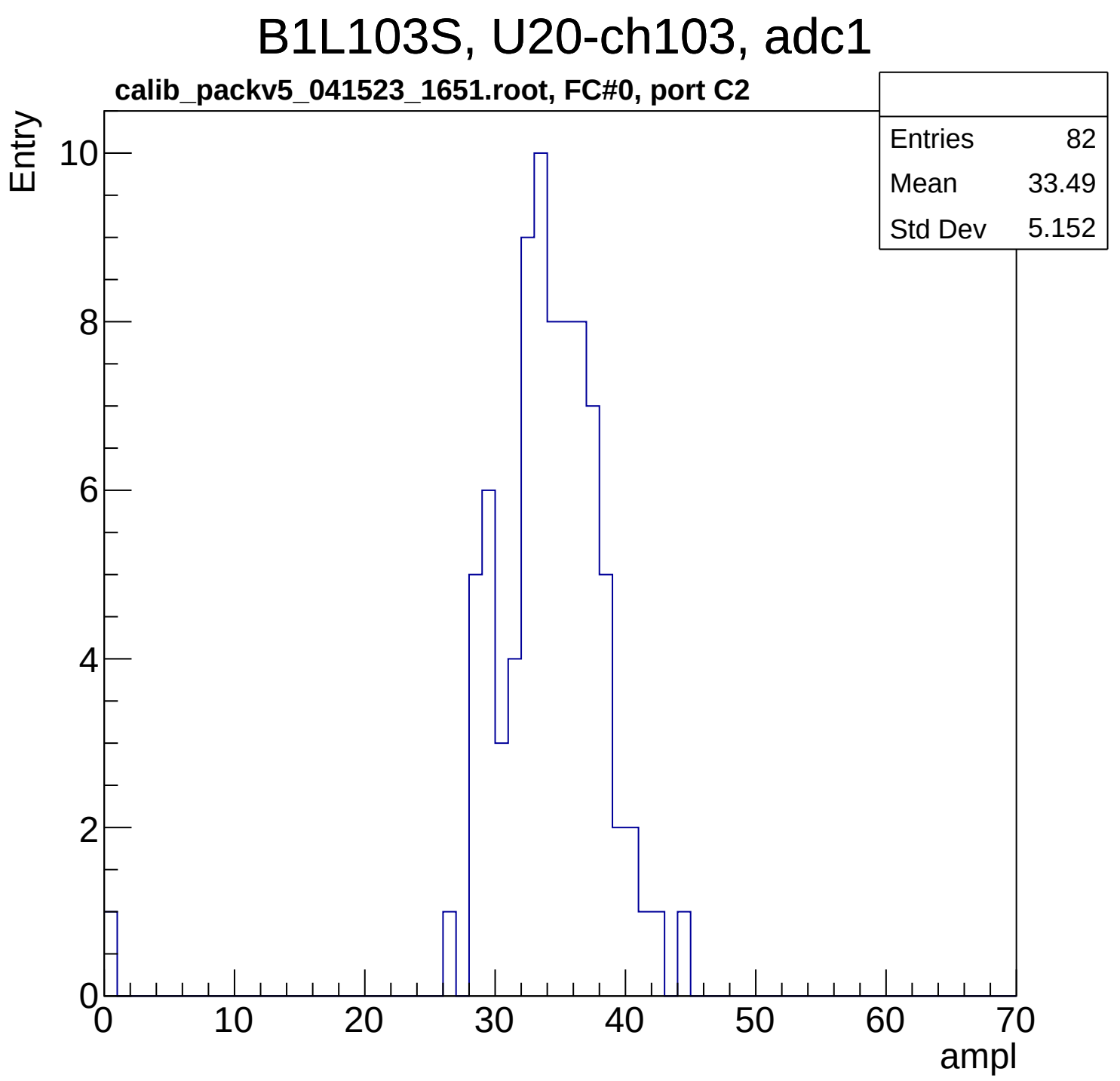
B1L103S, U20-ch103, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 33.49
Std Dev 5.152
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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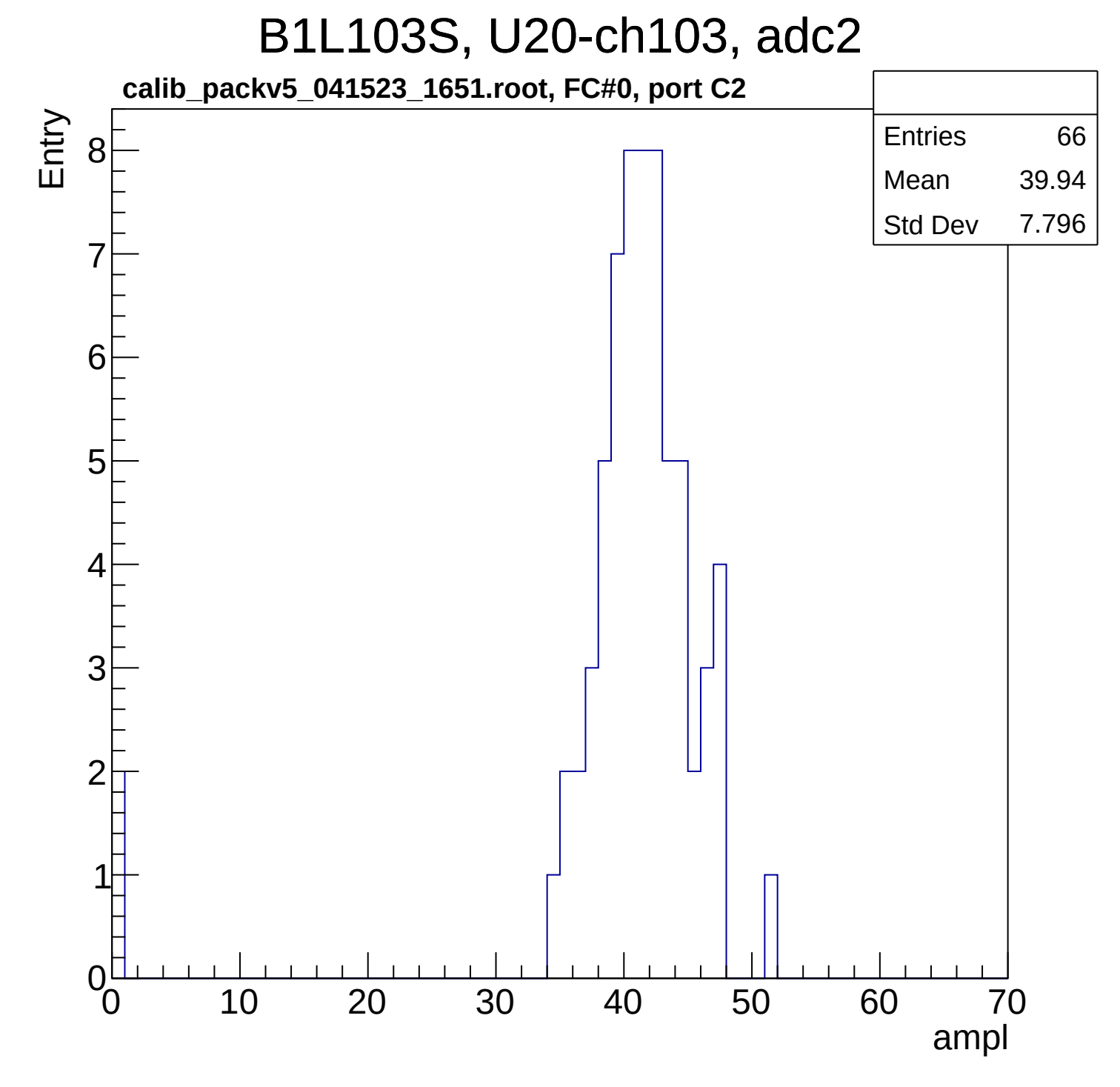
B1L103S, U20-ch103, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 39.94
Std Dev 7.796
Entry
ampl
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1
2
3
4
5
6
7
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0
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60
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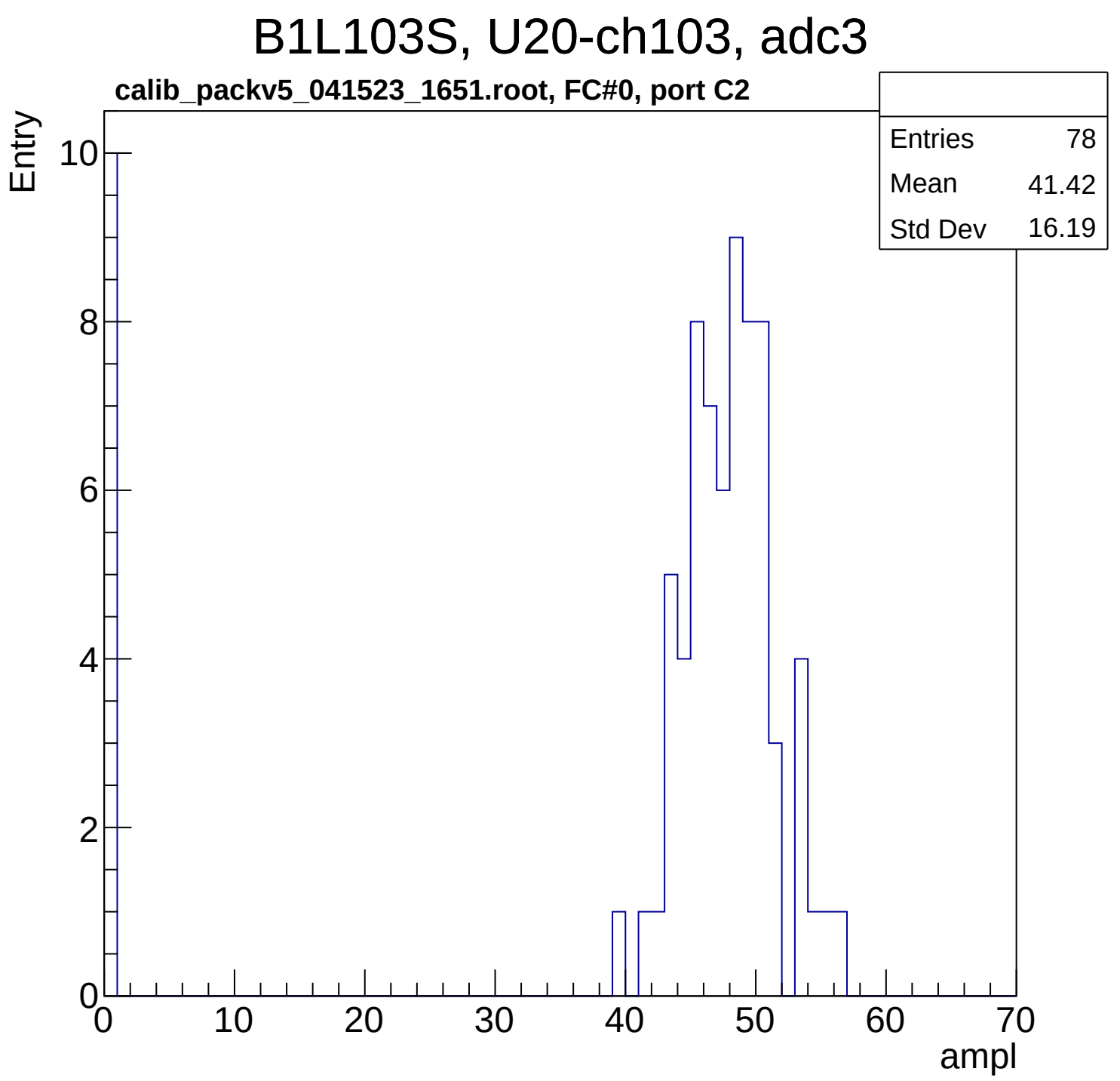
B1L103S, U20-ch103, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 41.42
Std Dev 16.19
Entry
ampl
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8
10
0
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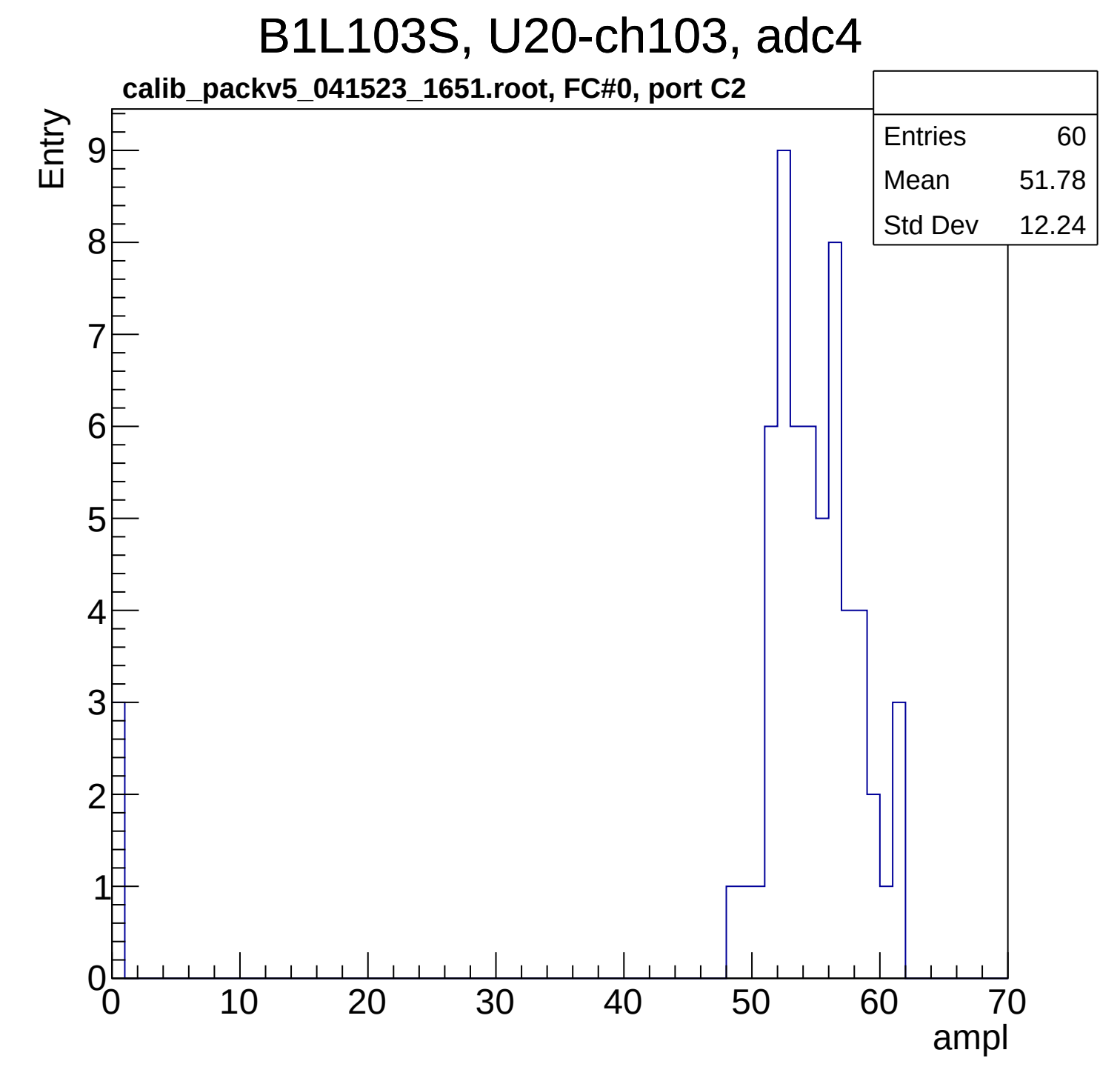
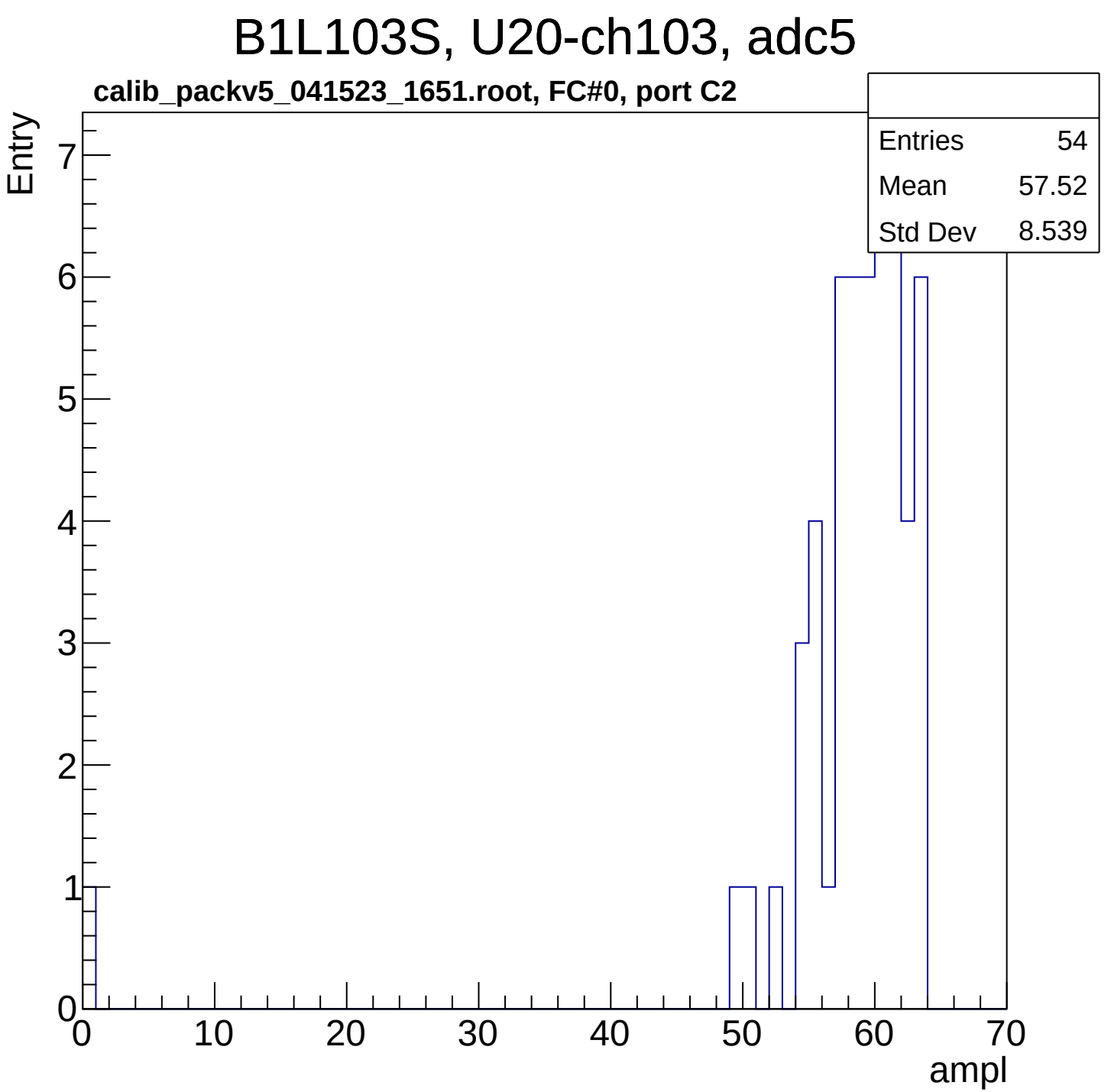
40
50
60
70


B1L103S, U20-ch103, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 51.78
Std Dev 12.24
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch103, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 57.52
Std Dev 8.539
Entry
ampl
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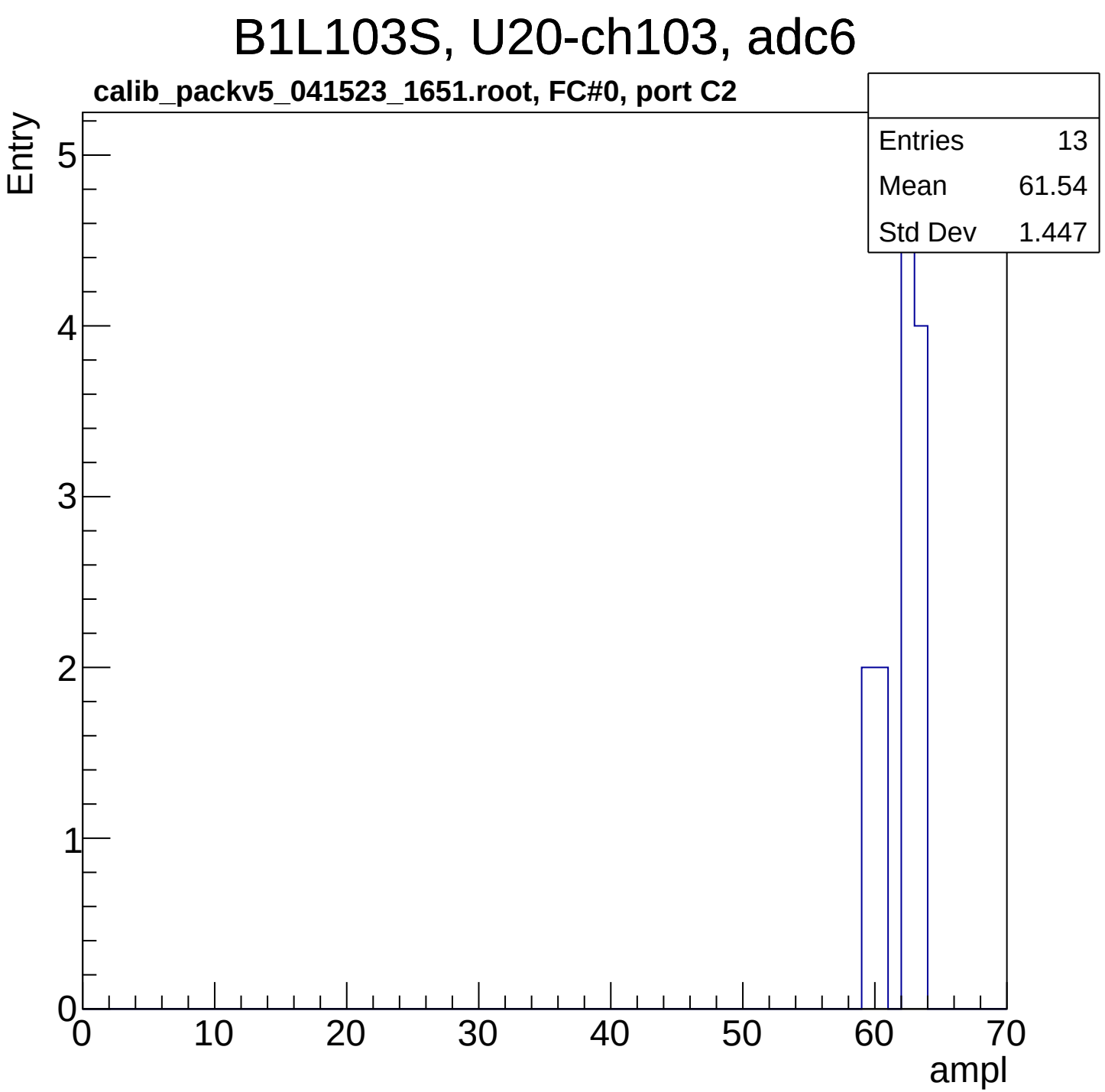
B1L103S, U20-ch103, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 61.54
Std Dev 1.447
Entry
ampl
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4
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0
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60
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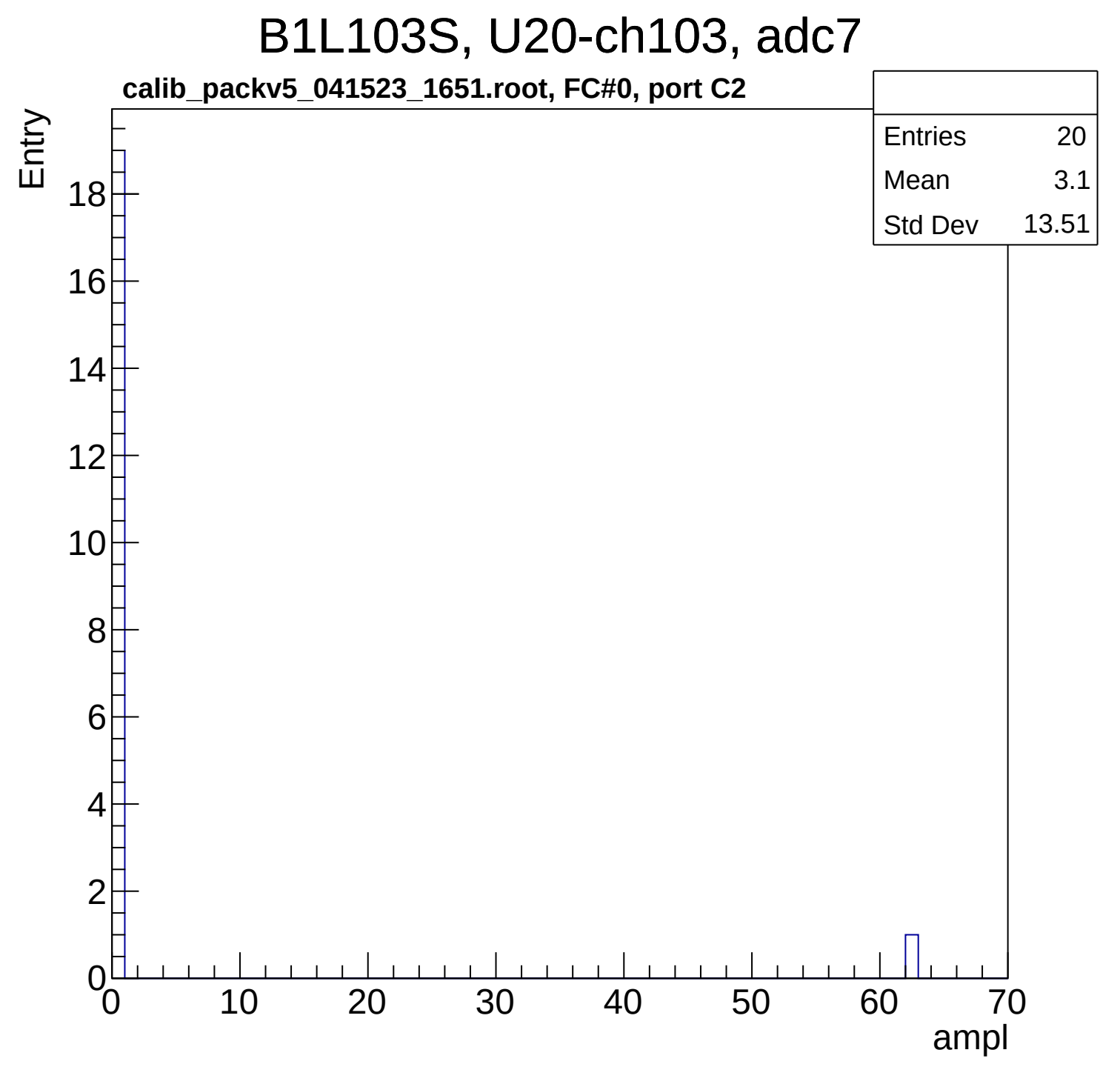
B1L103S, U20-ch103, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
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6
8
10
12
14
16
18
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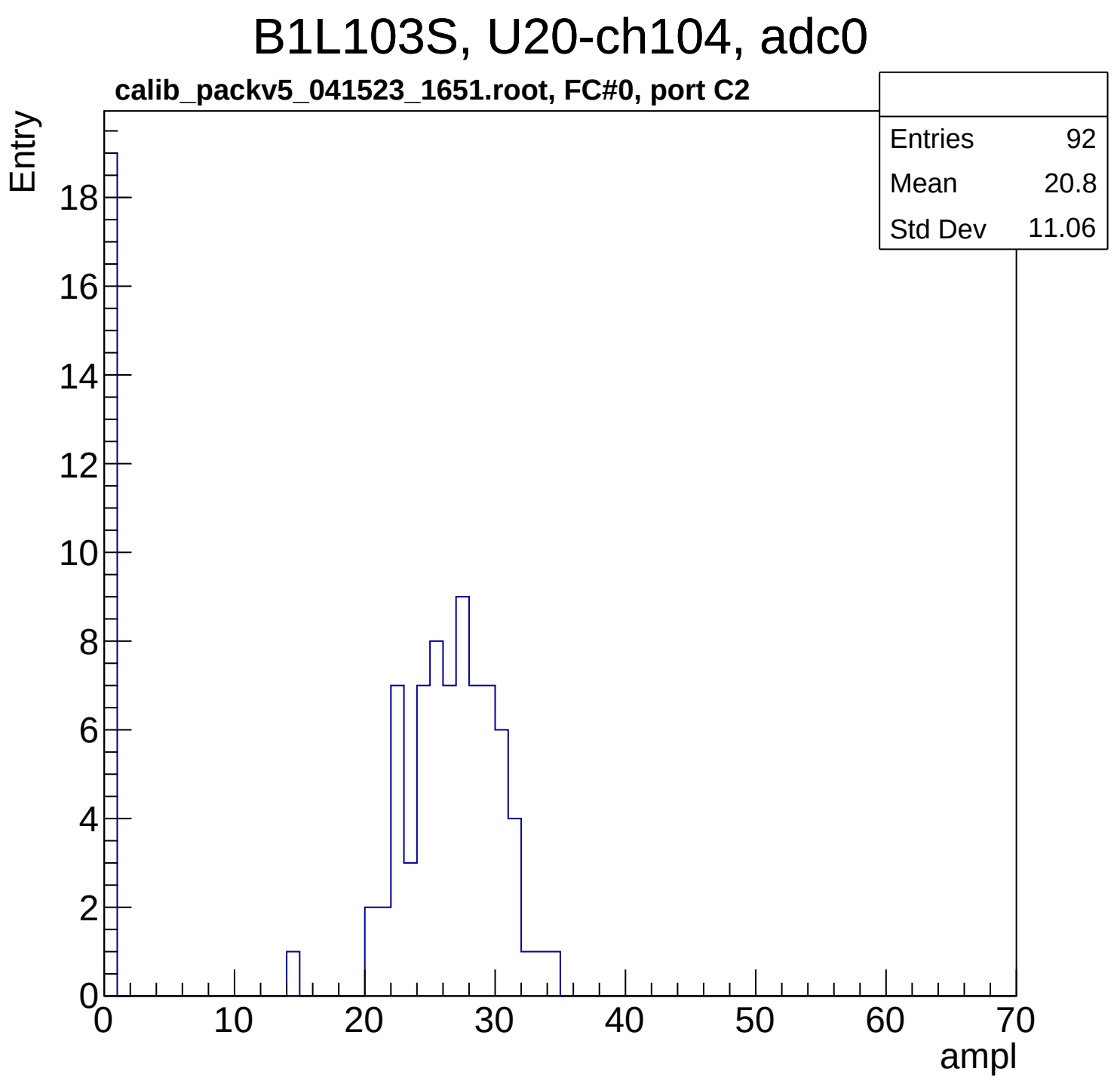
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch104, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 20.8
Std Dev 11.06
Entry
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8
10
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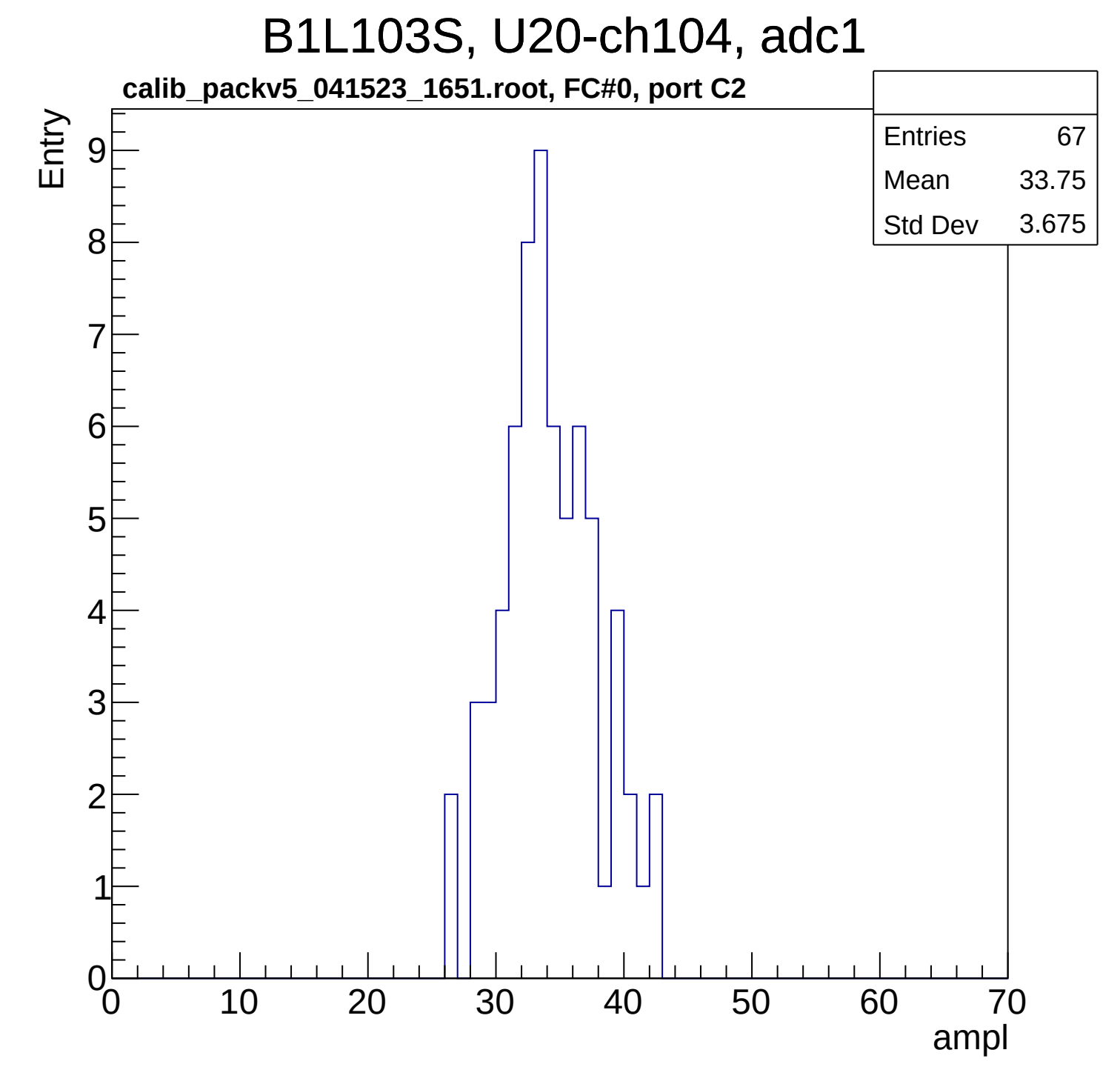
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch104, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 33.75
Std Dev 3.675
Entry
ampl
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3
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6
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8
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0
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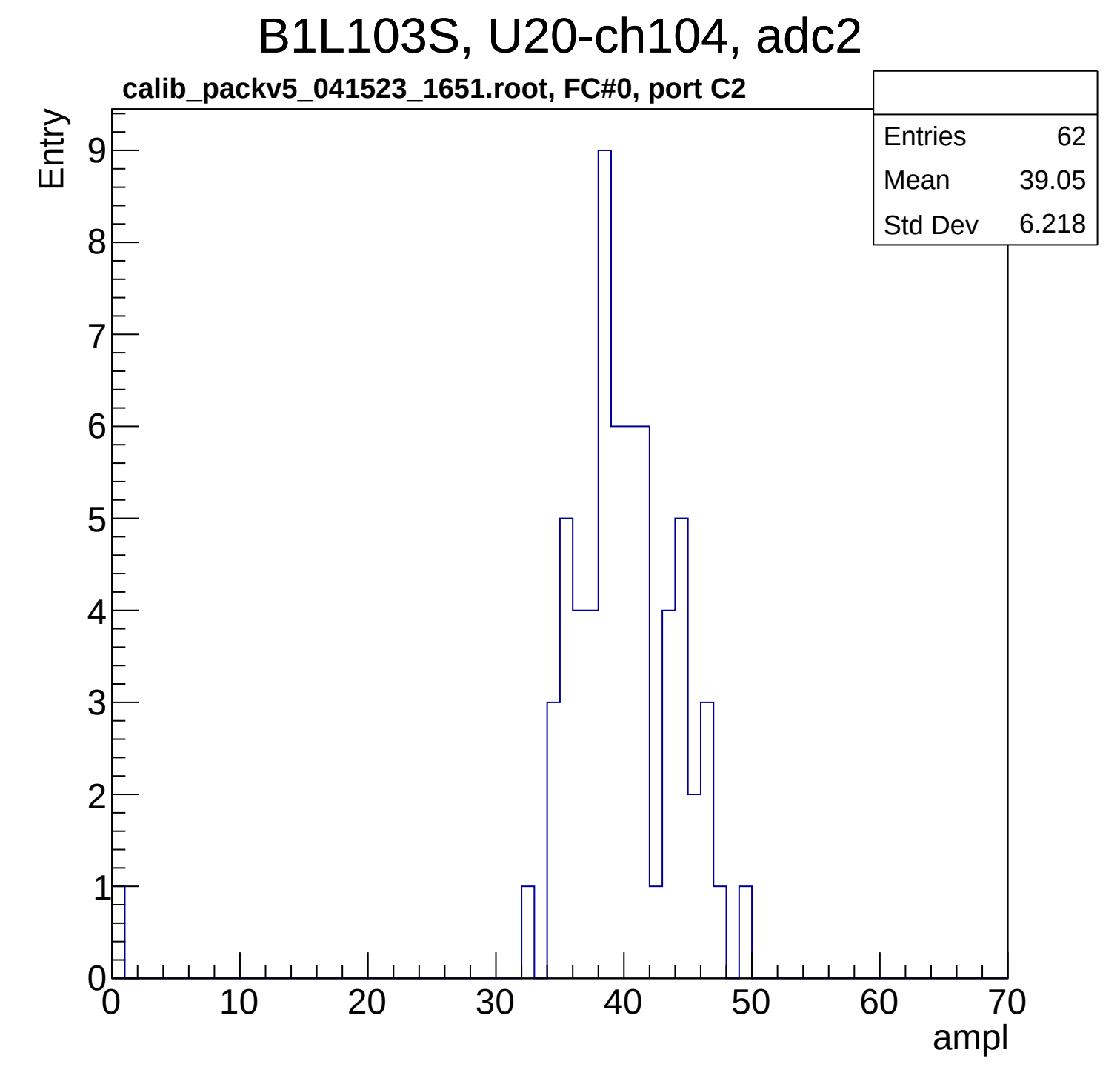
B1L103S, U20-ch104, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 39.05
Std Dev 6.218
Entry
ampl
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2
3
4
5
6
7
8
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0
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60
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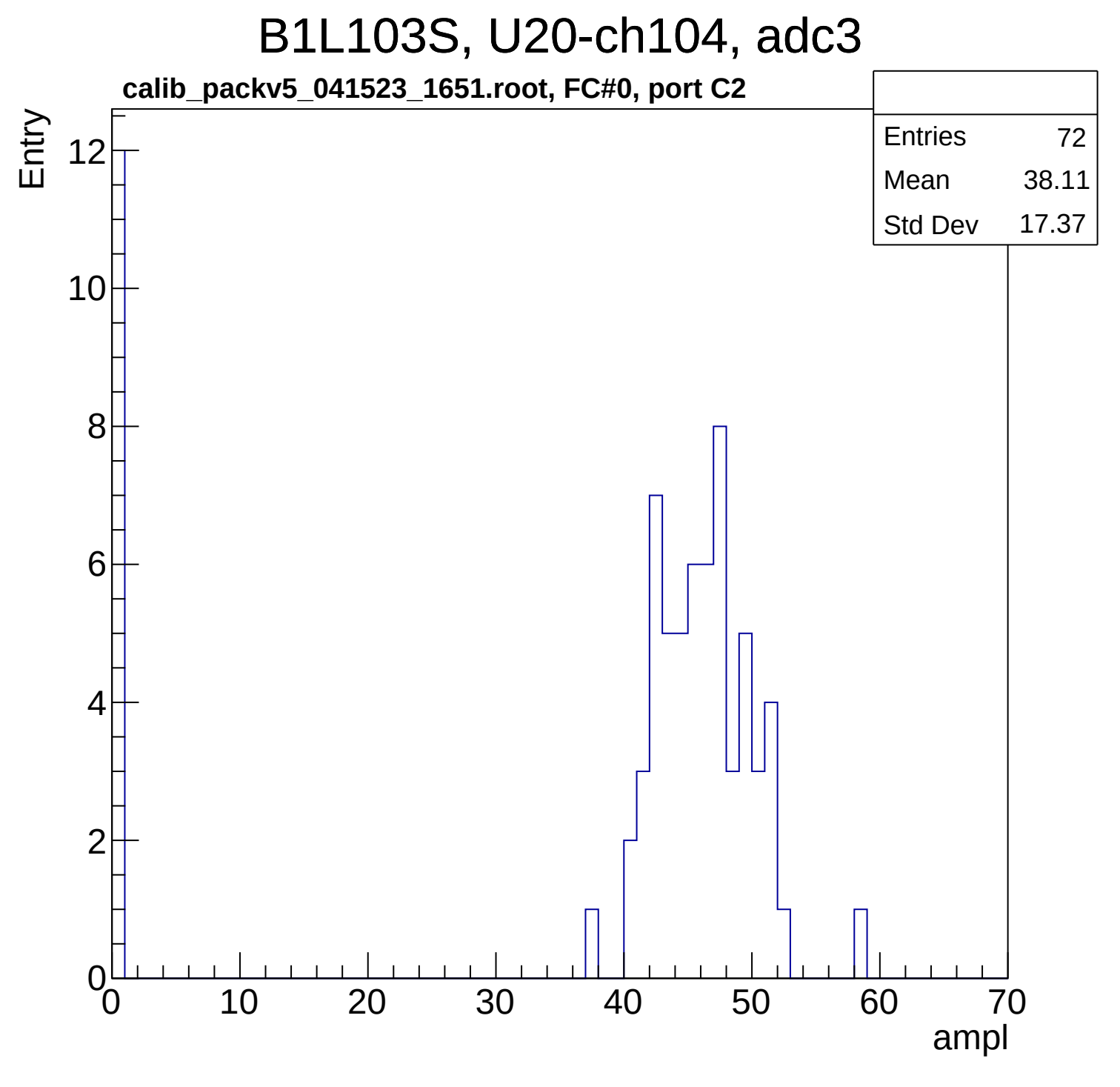
B1L103S, U20-ch104, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 38.11
Std Dev 17.37
Entry
ampl
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2
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6
8
10
12
0
10
20
30
40
50
60
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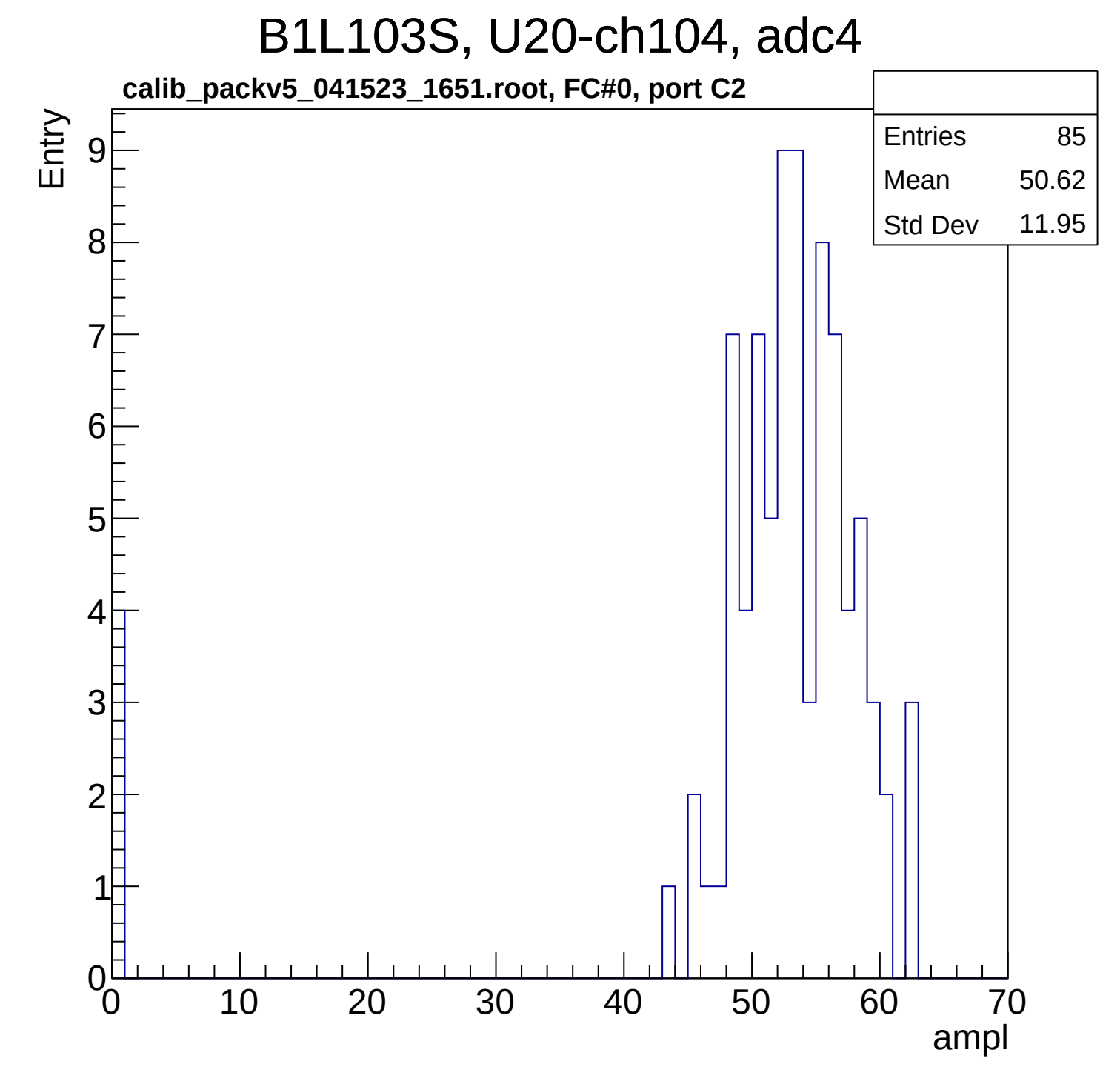
B1L103S, U20-ch104, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 50.62
Std Dev 11.95
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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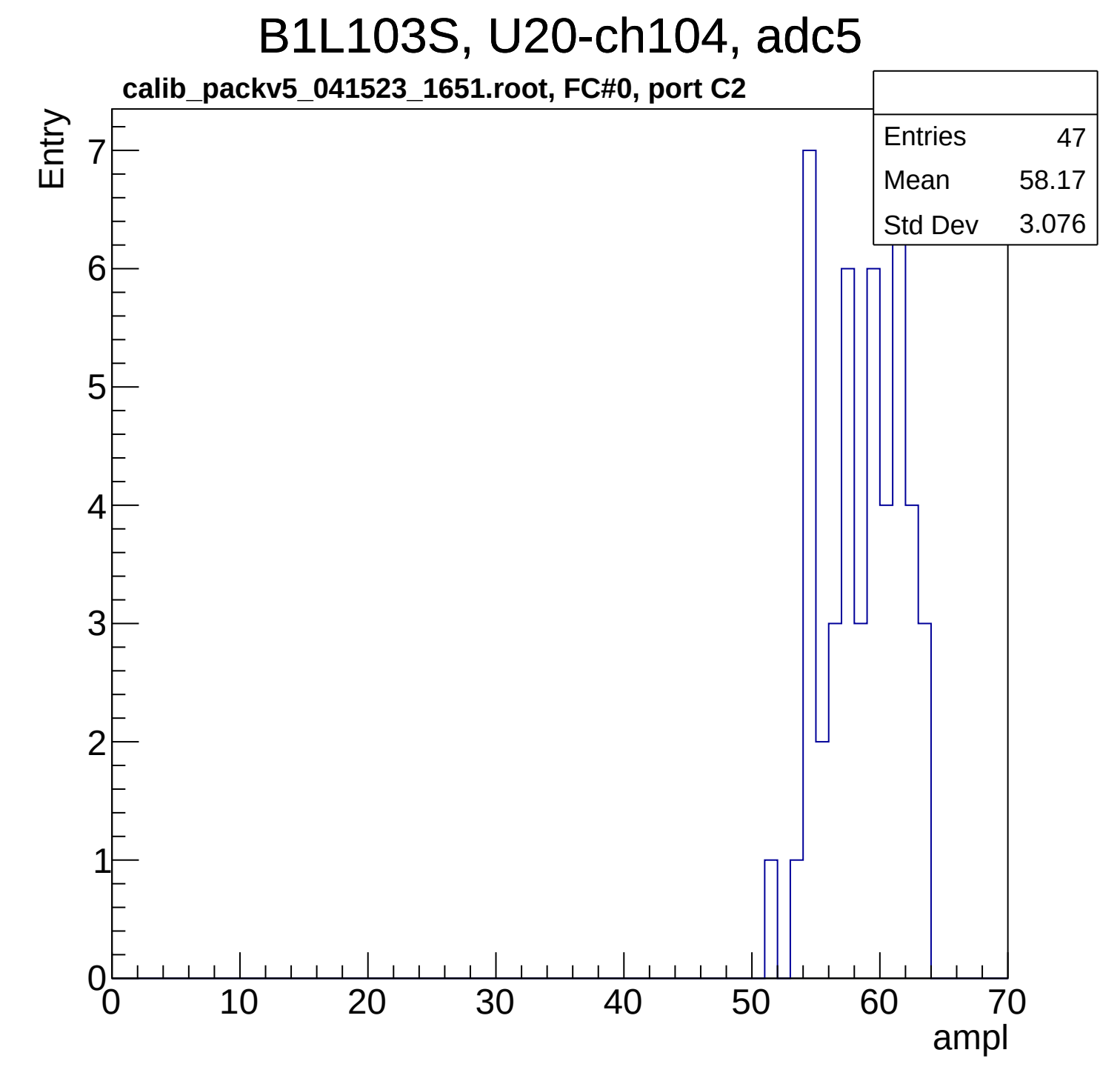
B1L103S, U20-ch104, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 58.17
Std Dev 3.076
Entry
ampl
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2
3
4
5
6
7
0
10
20
30
40
50
60
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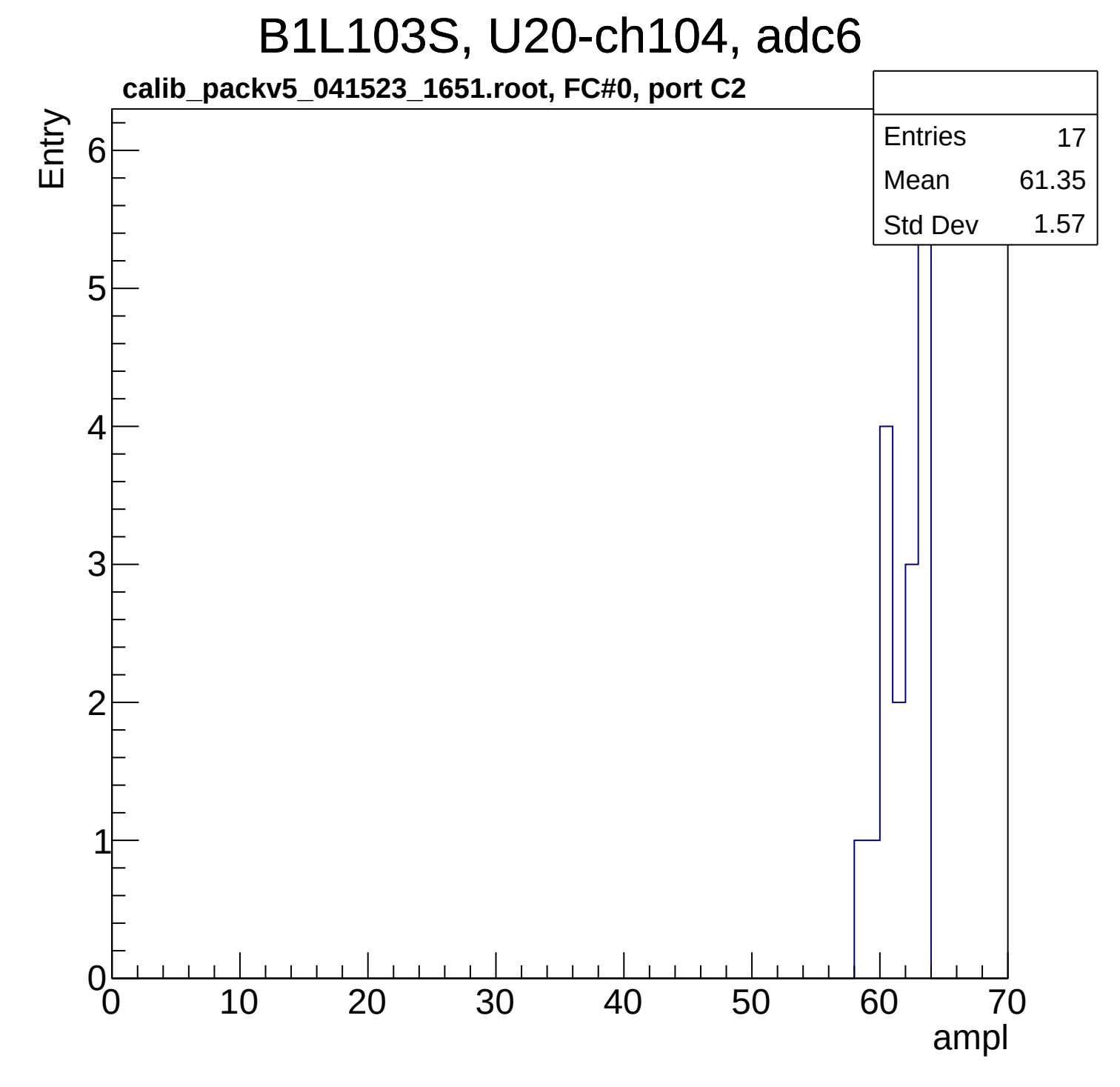
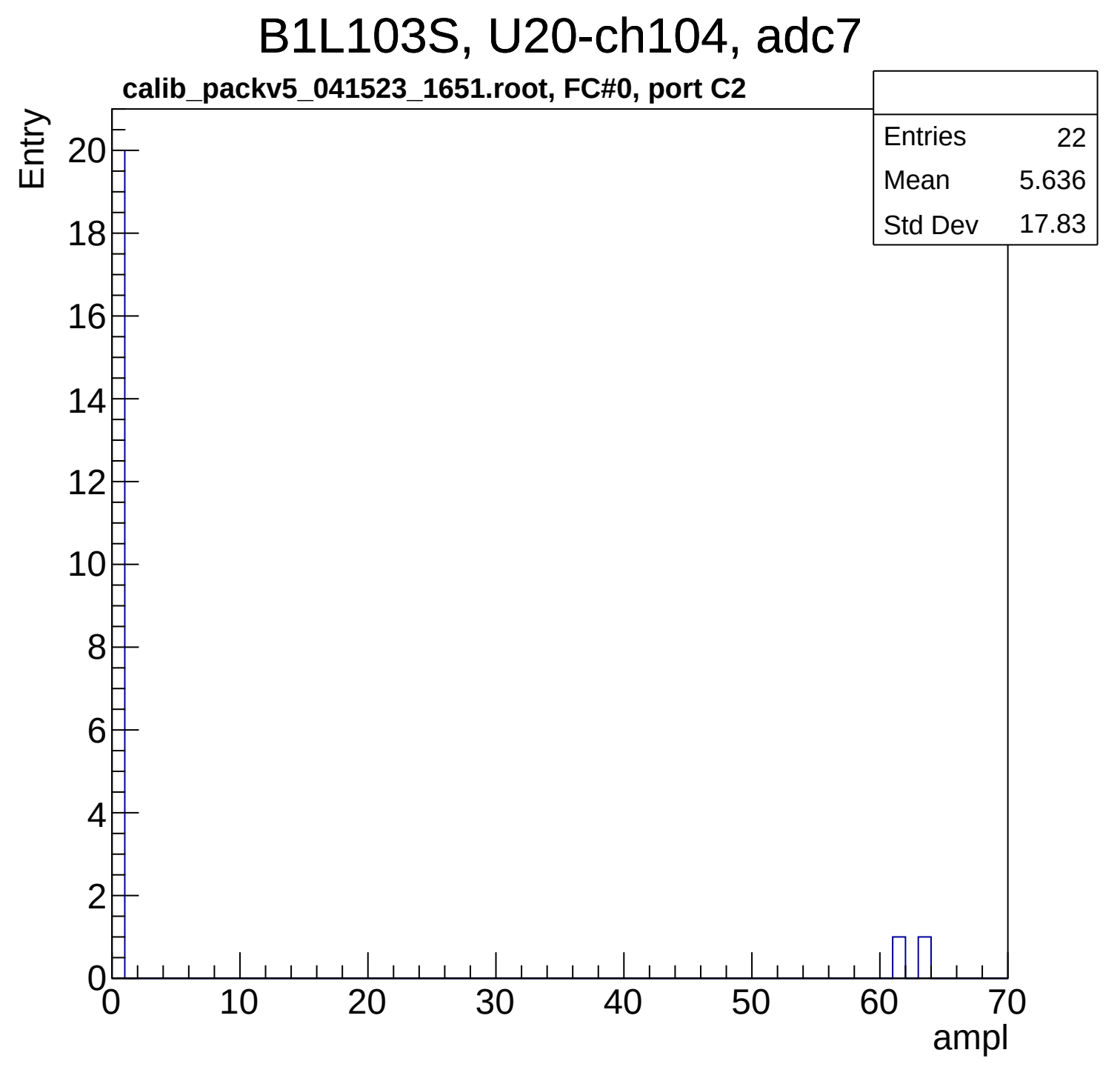

B1L103S, U20-ch104, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 61.35
Std Dev 1.57
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U20-ch104, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 5.636
Std Dev 17.83
Entry
0
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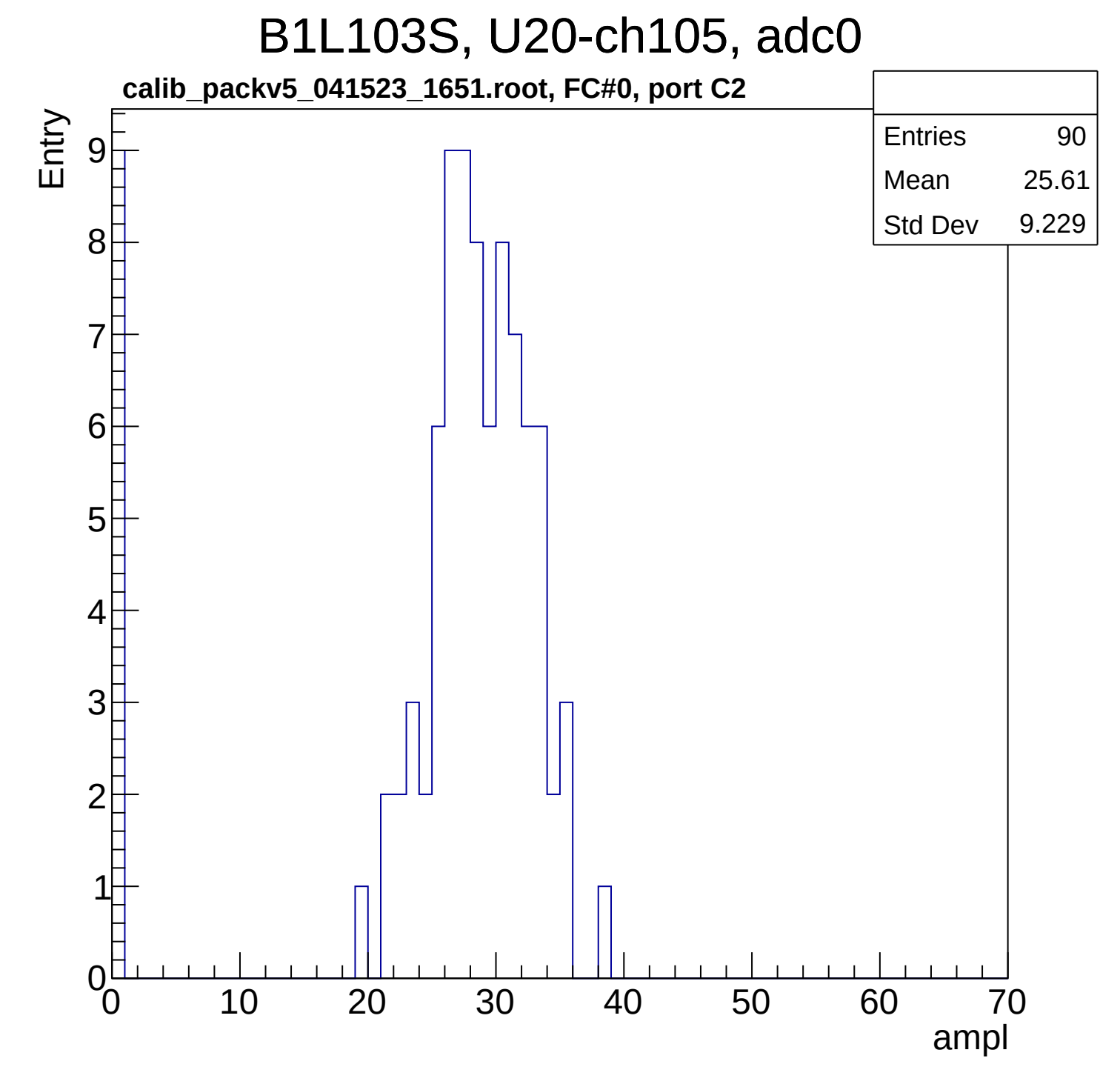
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch105, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 25.61
Std Dev 9.229
Entry
ampl
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3
4
5
6
7
8
9
0
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40
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60
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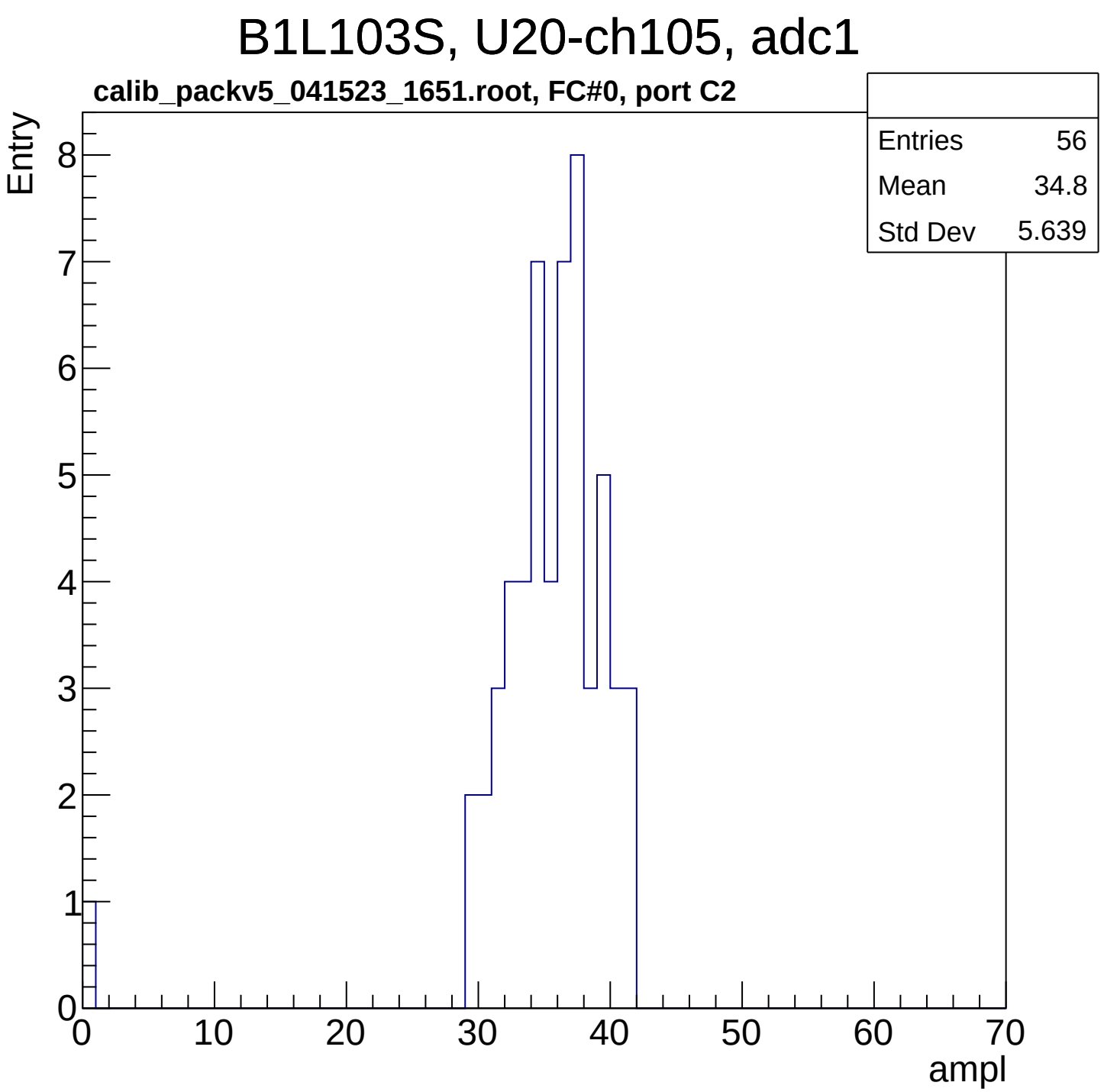
B1L103S, U20-ch105, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 34.8
Std Dev 5.639
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
50
60
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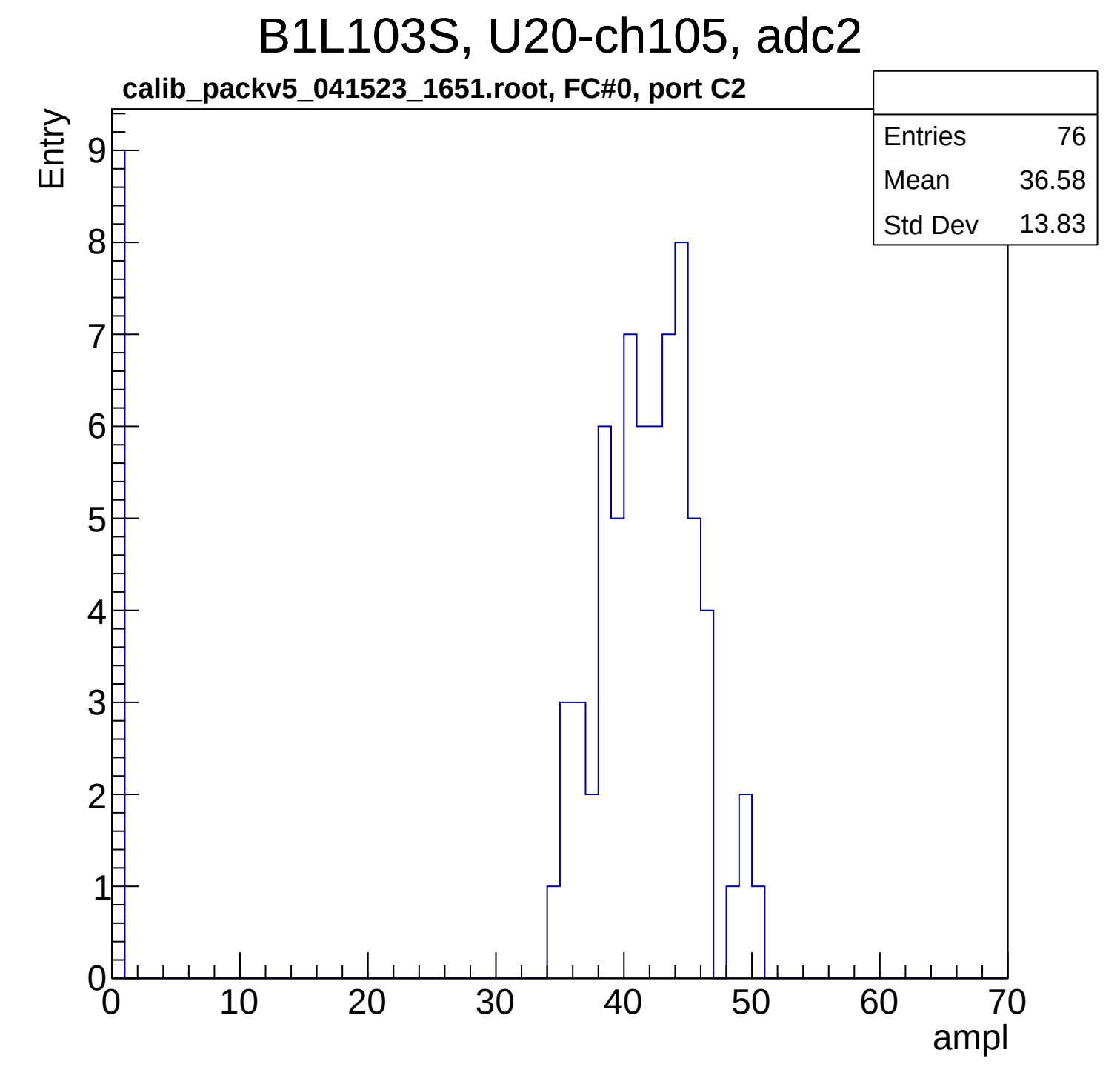
B1L103S, U20-ch105, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 36.58
Std Dev 13.83
Entry
ampl
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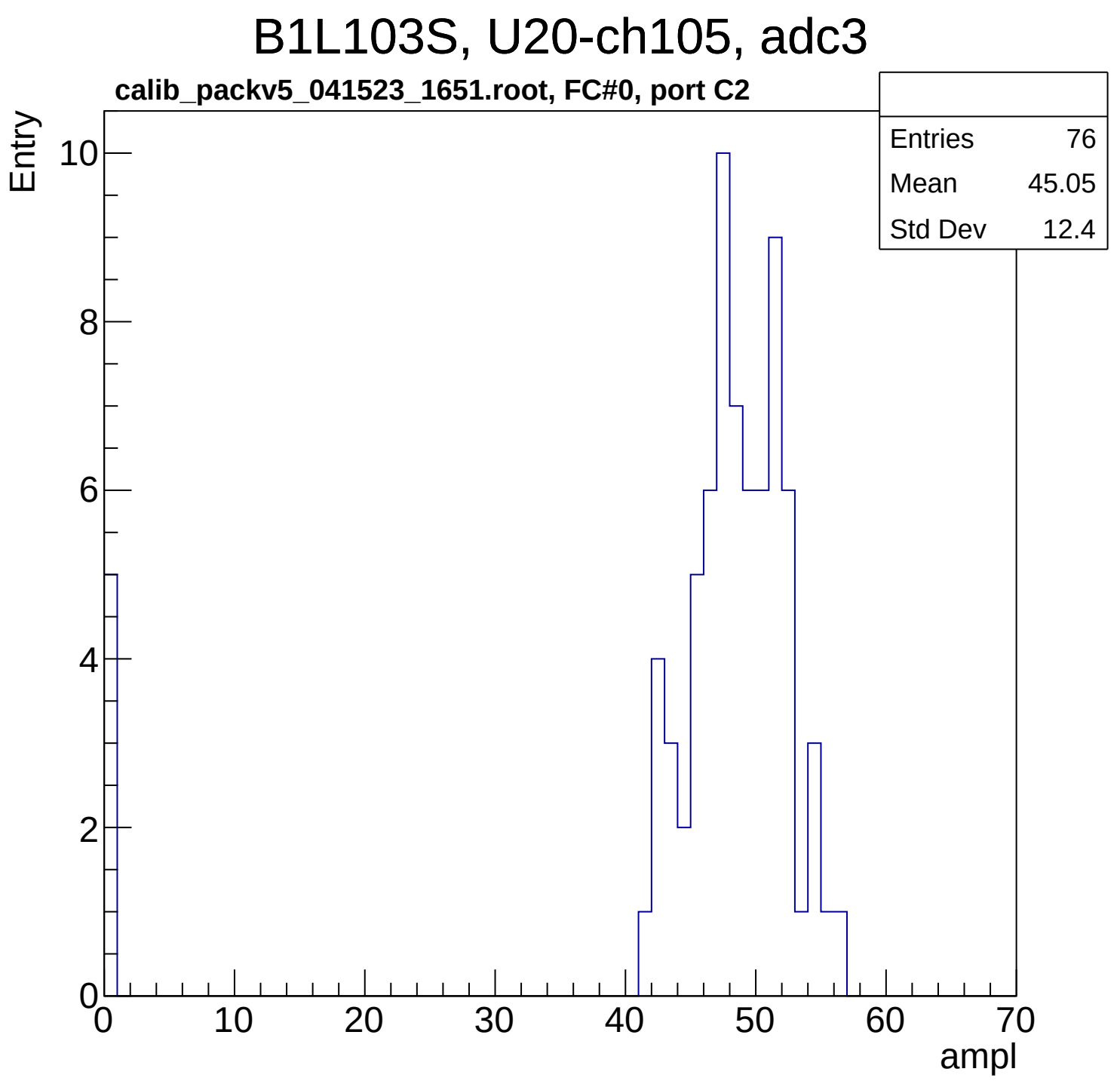
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch105, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 45.05
Std Dev 12.4
Entry
ampl
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4
6
8
10
0
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20
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40
50
60
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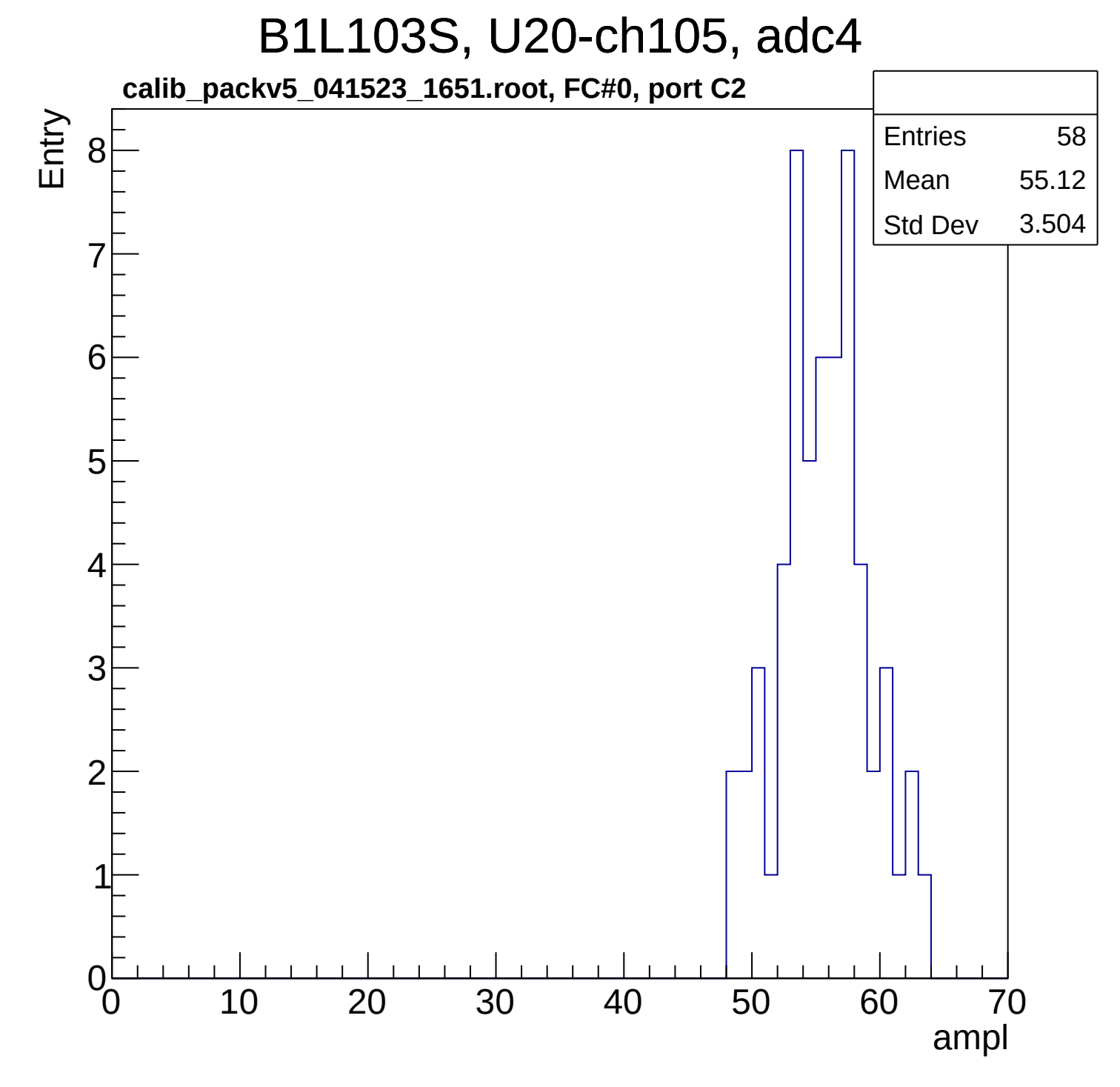
B1L103S, U20-ch105, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 55.12
Std Dev 3.504
Entry
ampl
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5
6
7
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0
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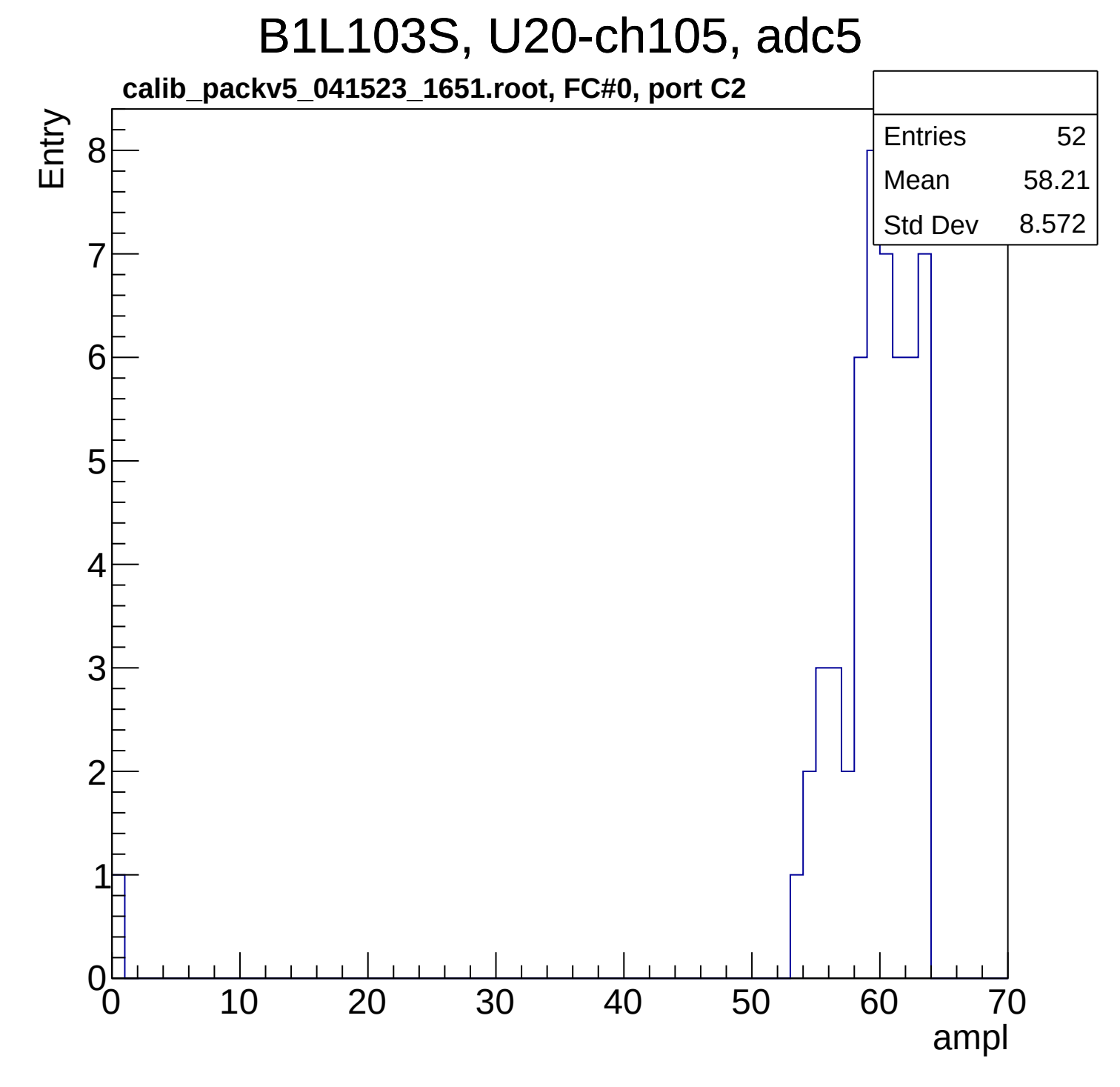
B1L103S, U20-ch105, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 58.21
Std Dev 8.572
Entry
ampl
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4
5
6
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60
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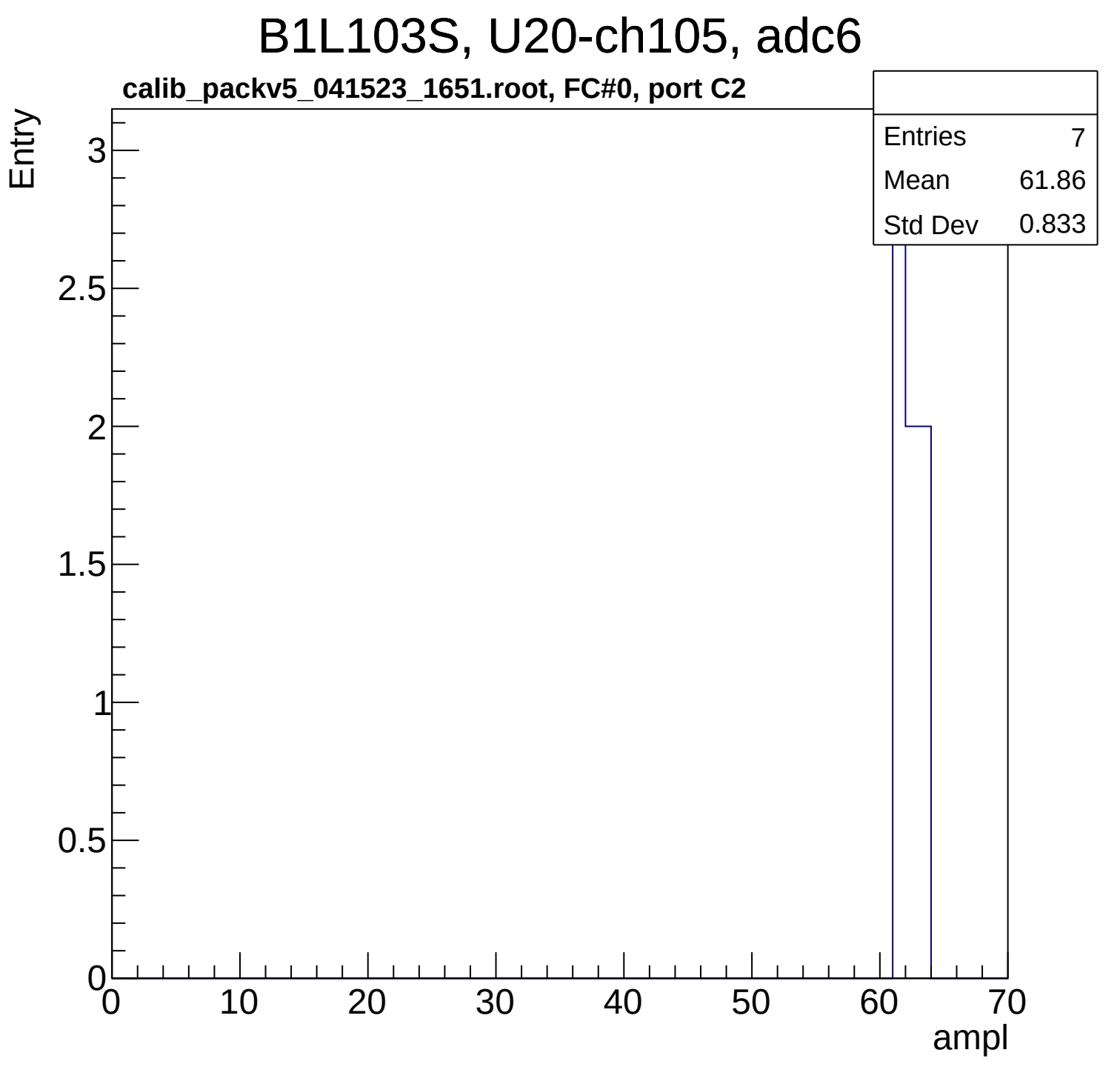
B1L103S, U20-ch105, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 61.86
Std Dev 0.833
Entry
ampl
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1
1.5
2
2.5
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0
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60
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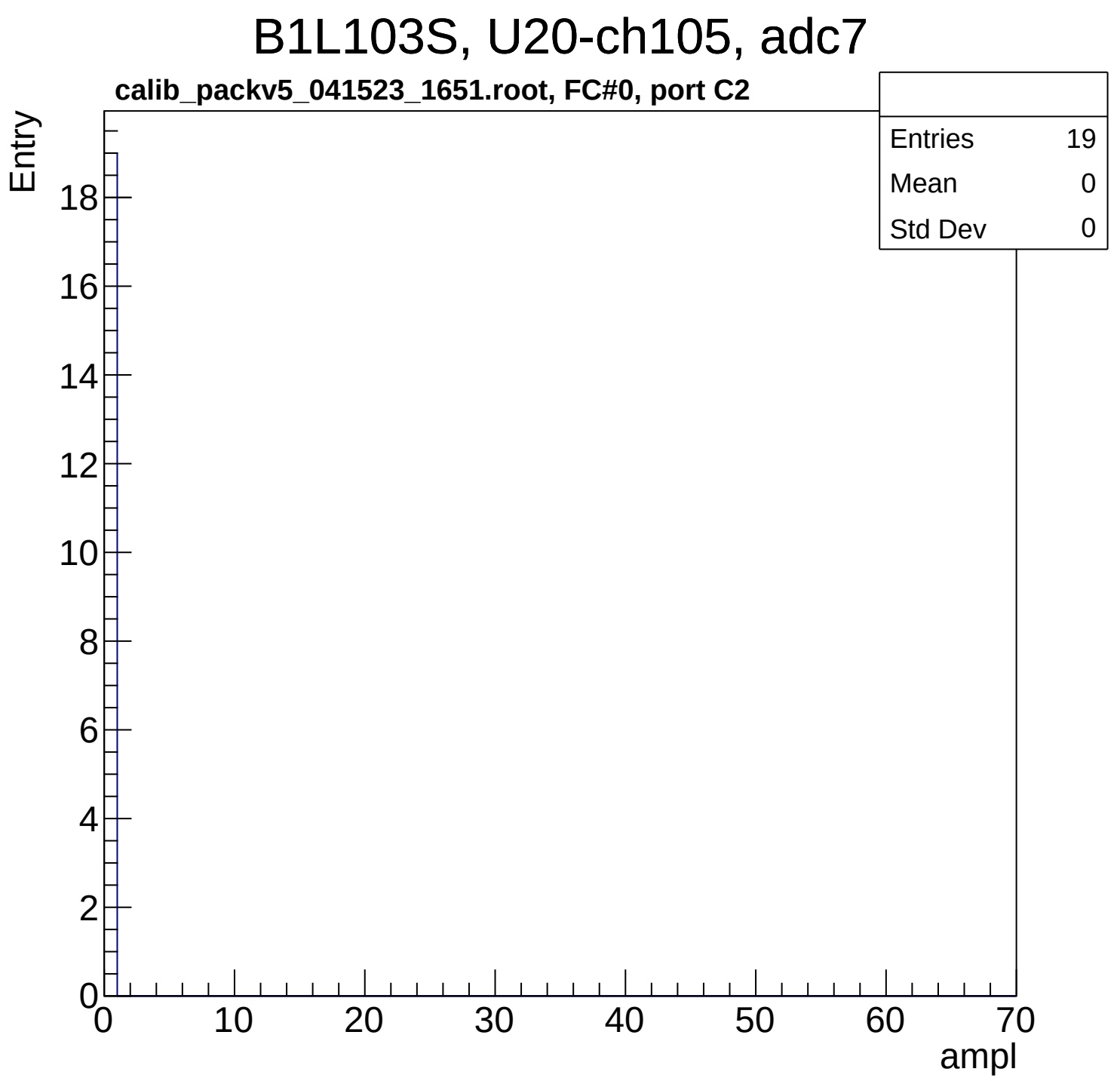
B1L103S, U20-ch105, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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6
8
10
12
14
16
18
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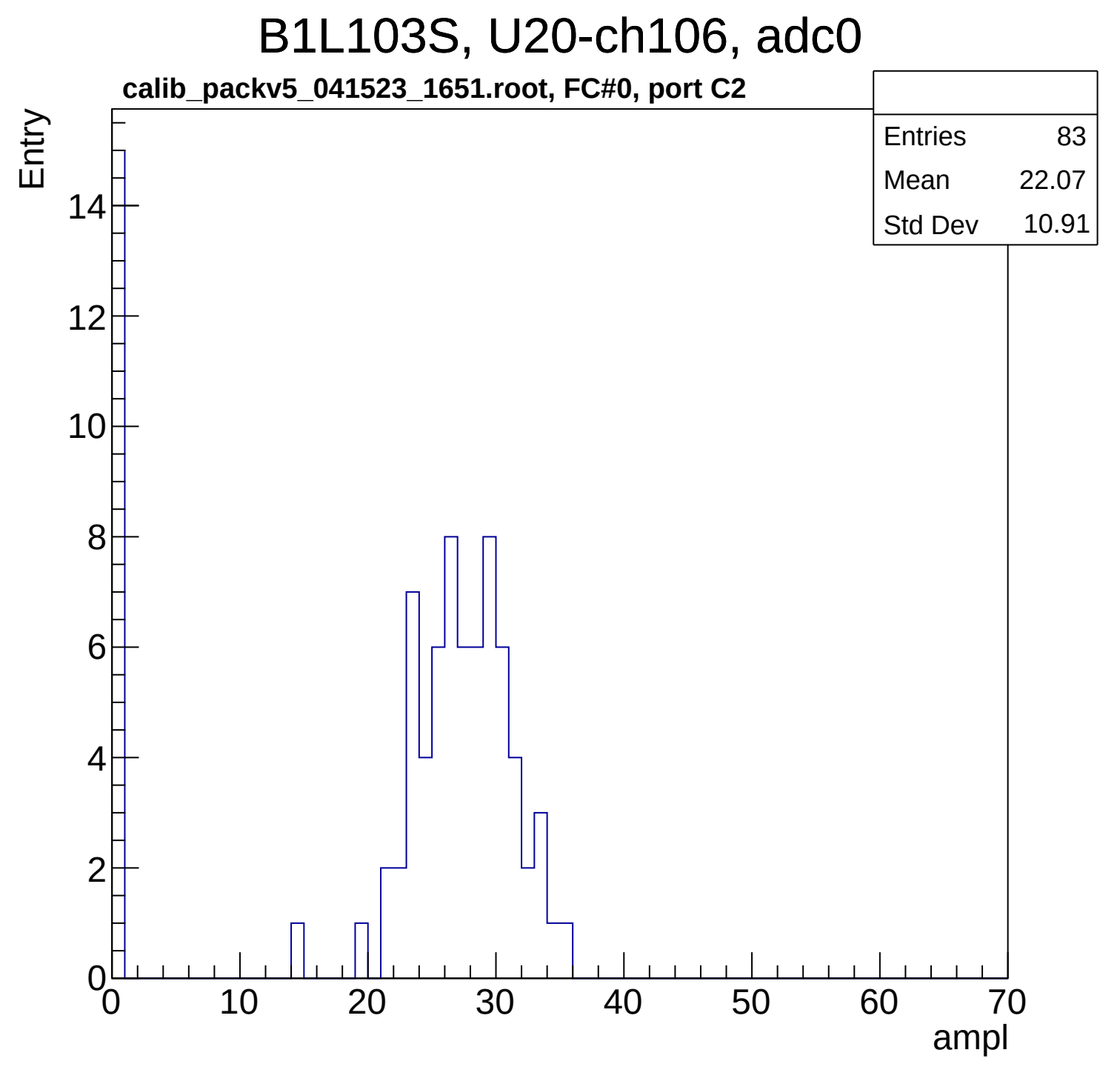
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch106, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 22.07
Std Dev 10.91
Entry
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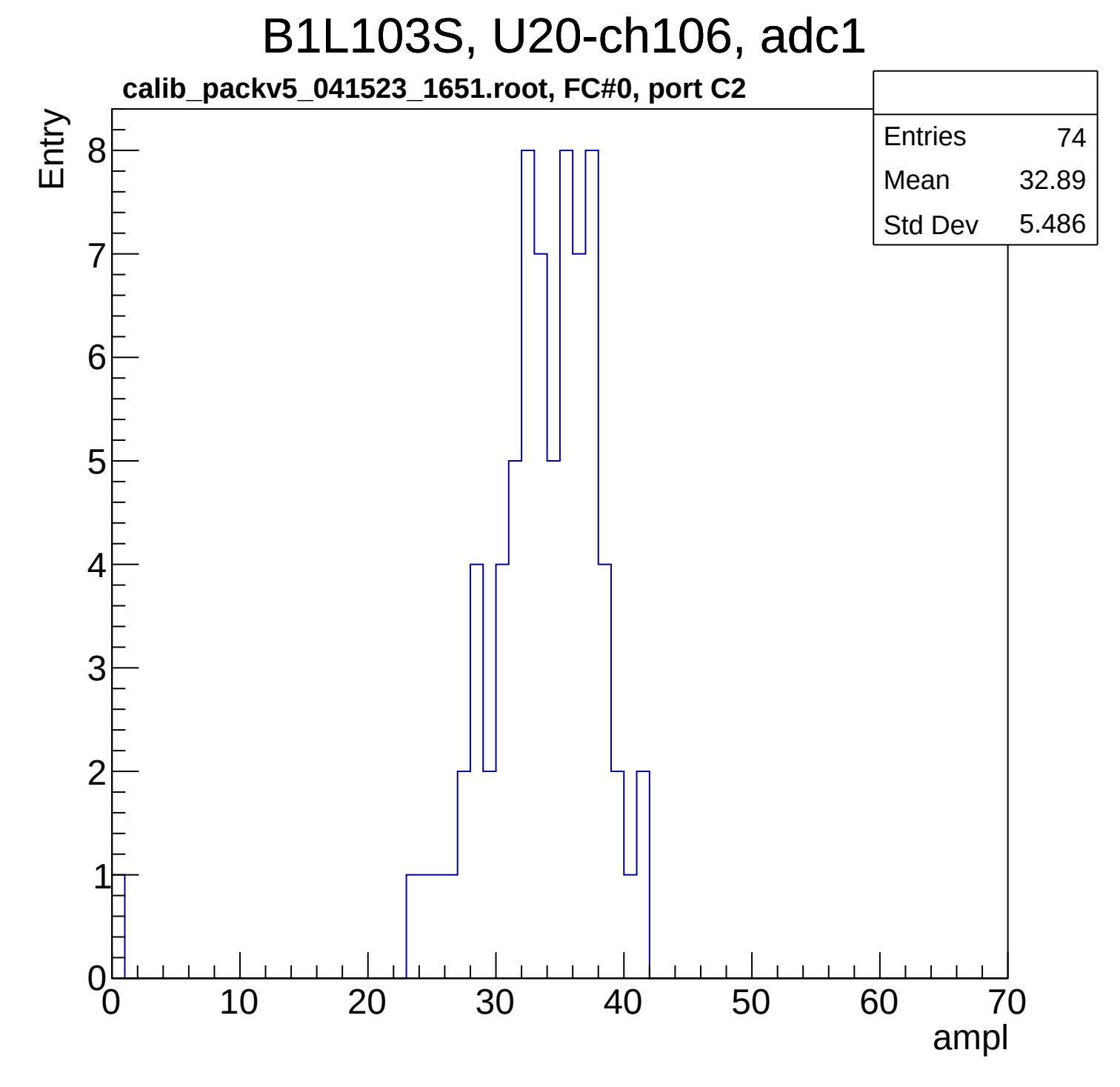
70
ampl


B1L103S, U20-ch106, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 32.89
Std Dev 5.486
Entry
ampl
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0
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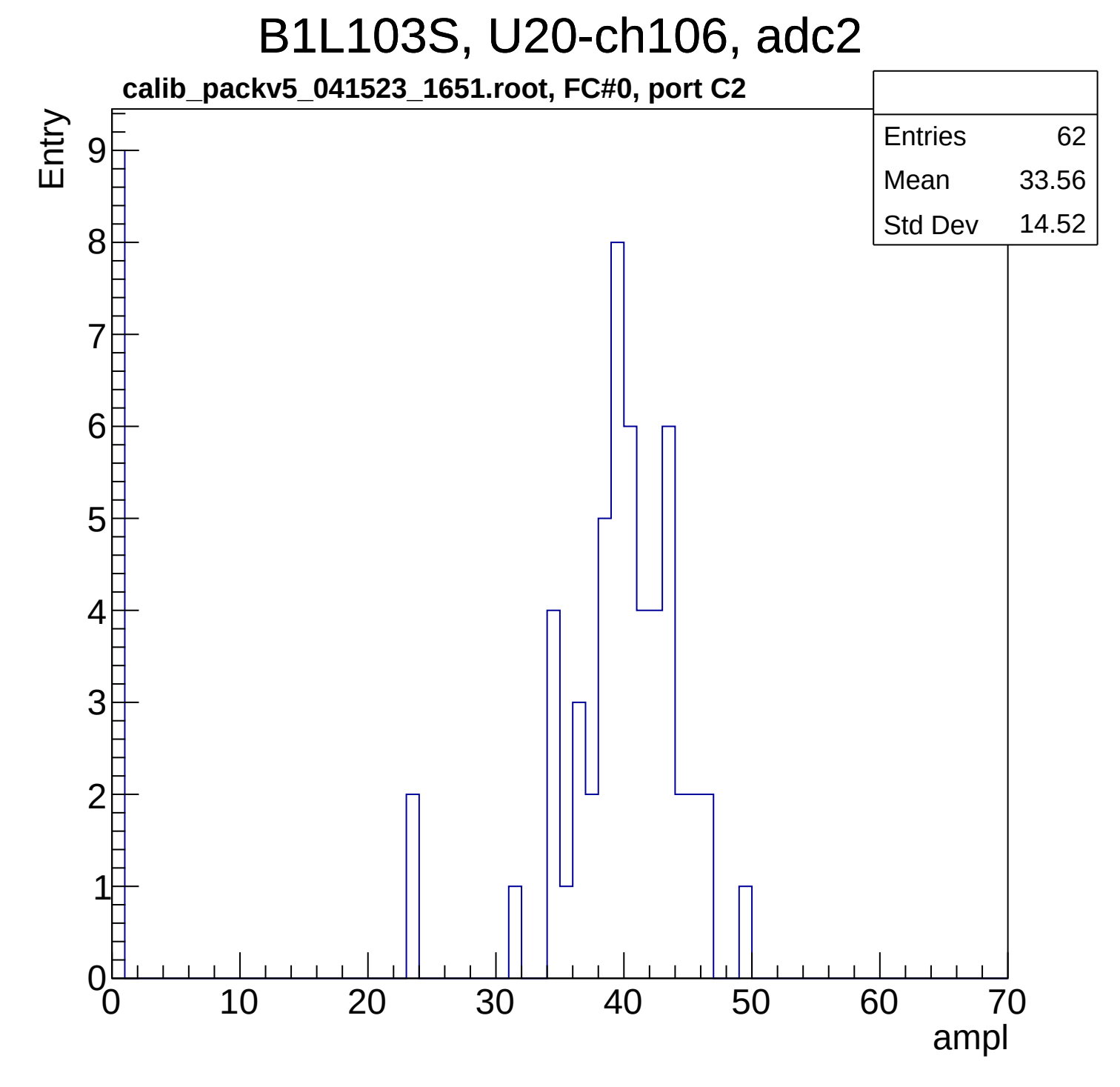
B1L103S, U20-ch106, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 33.56
Std Dev 14.52
Entry
ampl
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2
3
4
5
6
7
8
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0
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60
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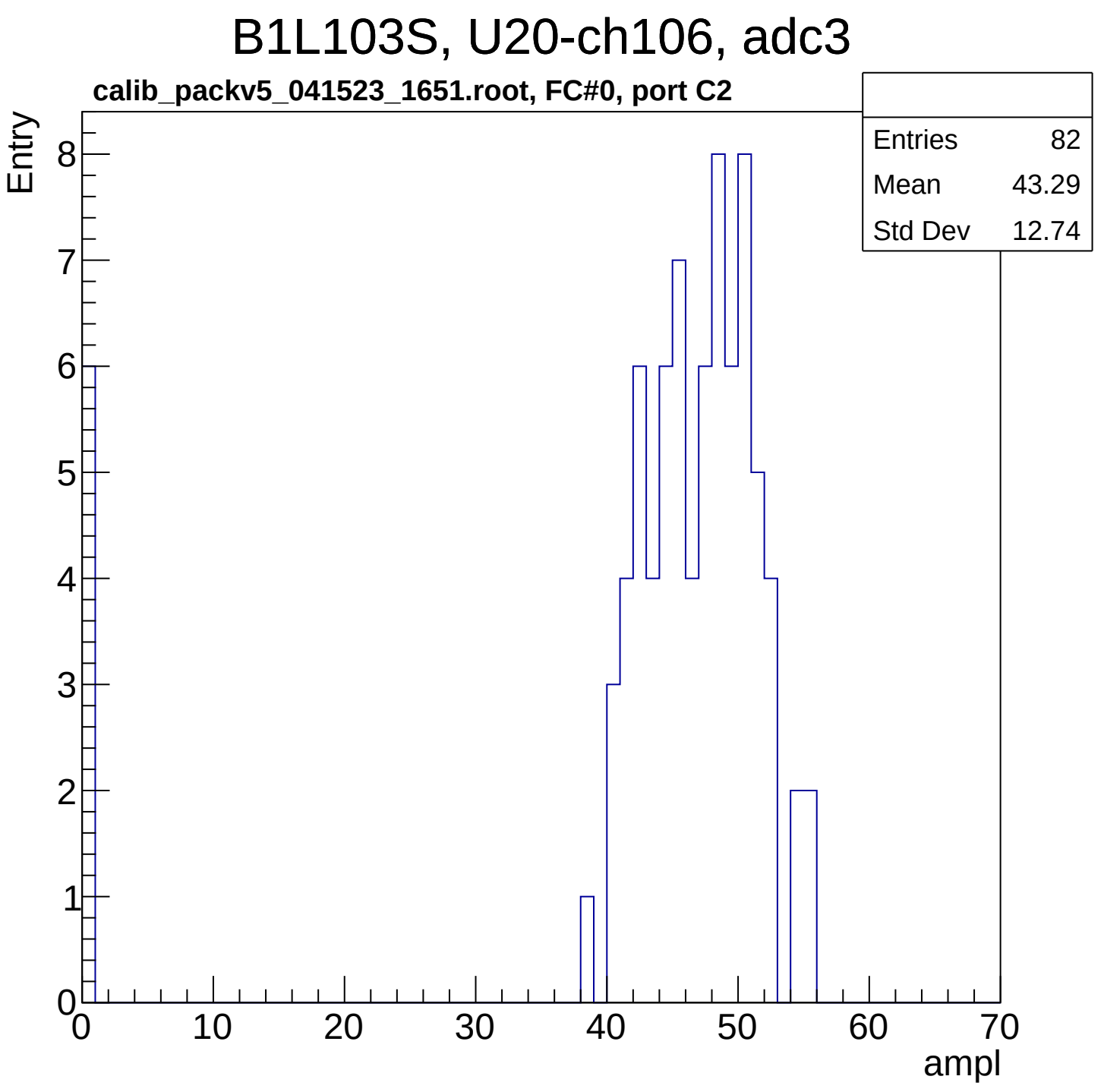
B1L103S, U20-ch106, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 43.29
Std Dev 12.74
Entry
ampl
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2
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5
6
7
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0
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40
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60
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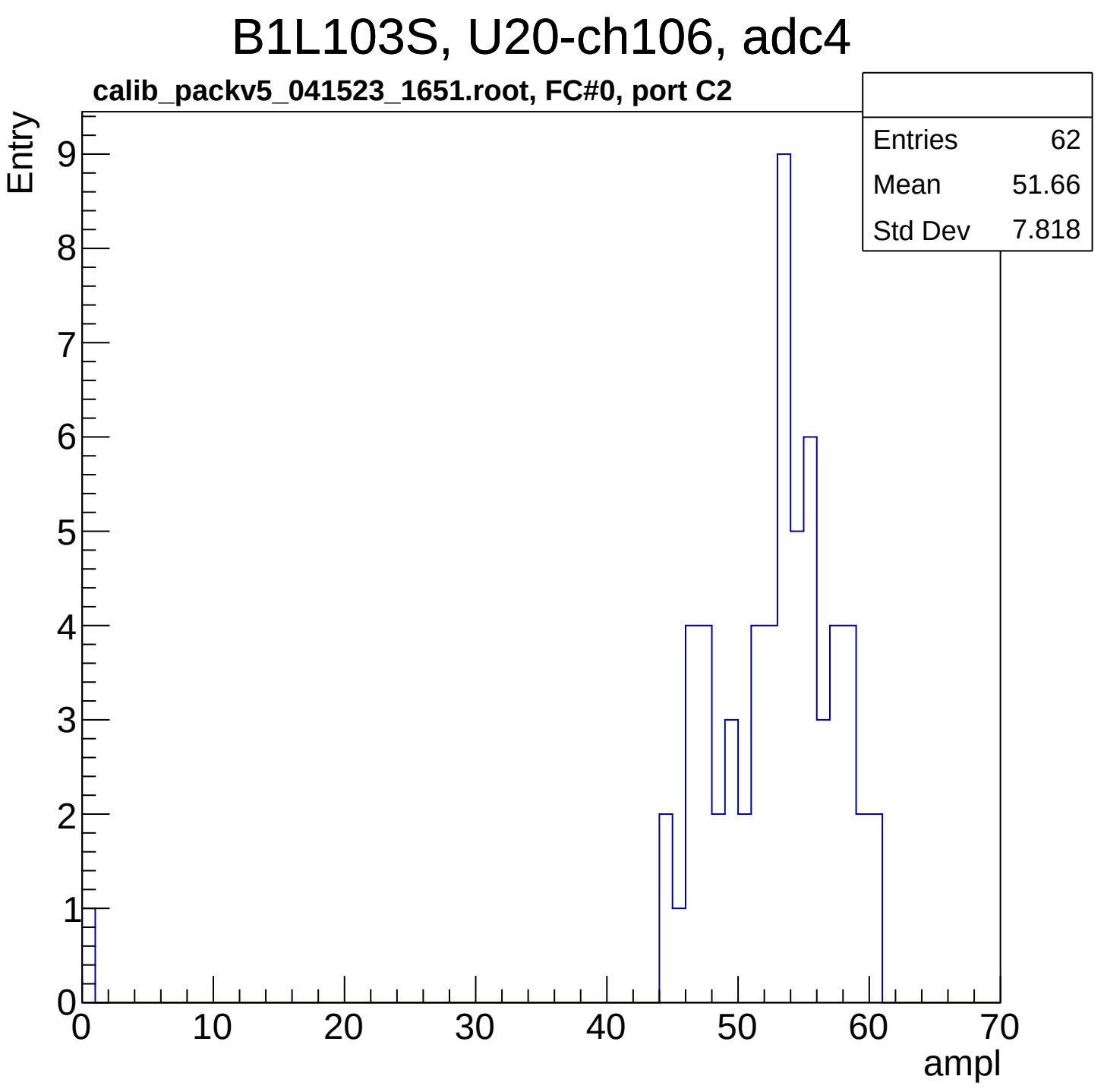
B1L103S, U20-ch106, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 51.66
Std Dev 7.818
Entry
ampl
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6
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8
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0
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40
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60
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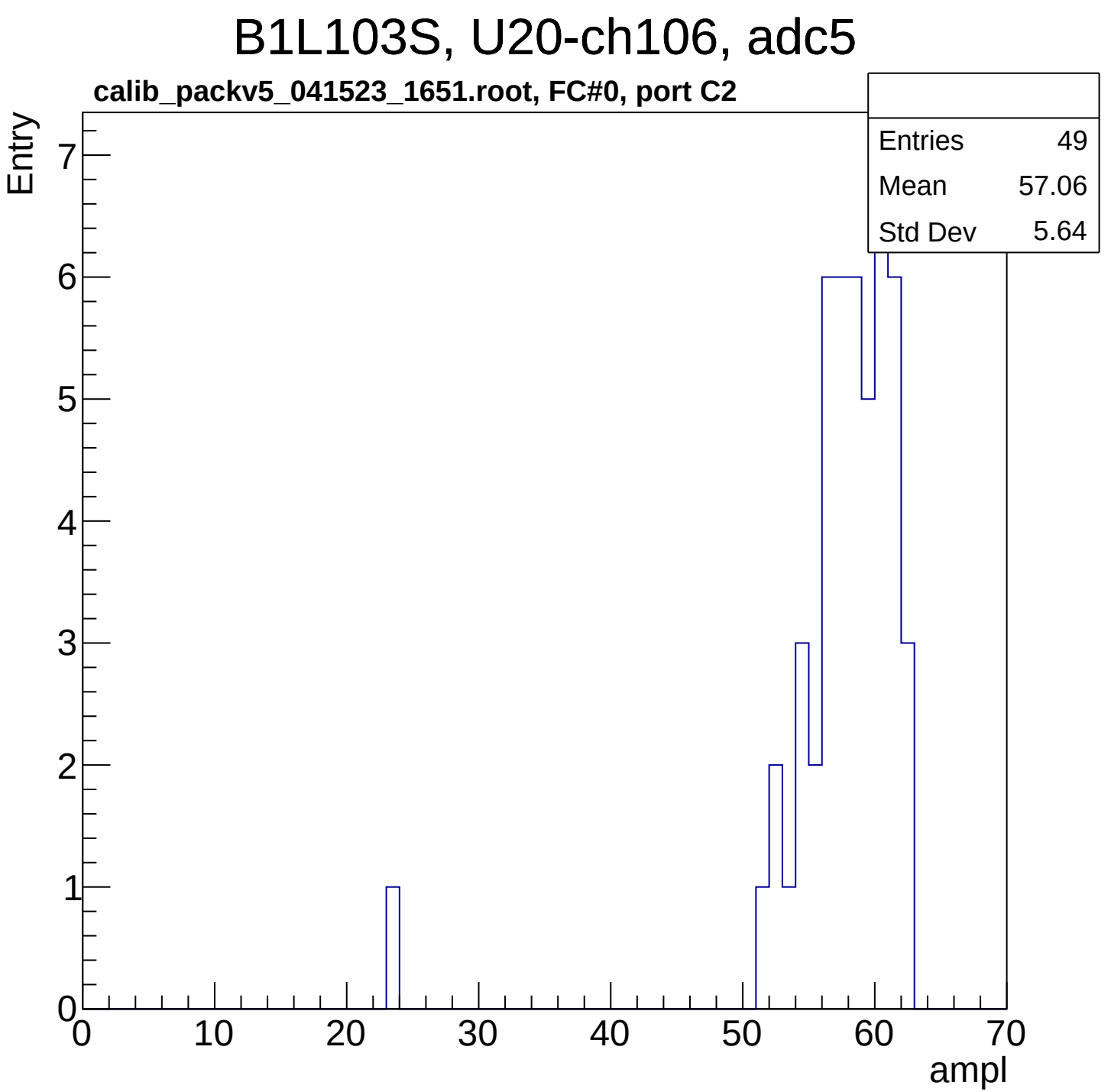
B1L103S, U20-ch106, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 57.06
Std Dev 5.64
Entry
ampl
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4
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6
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0
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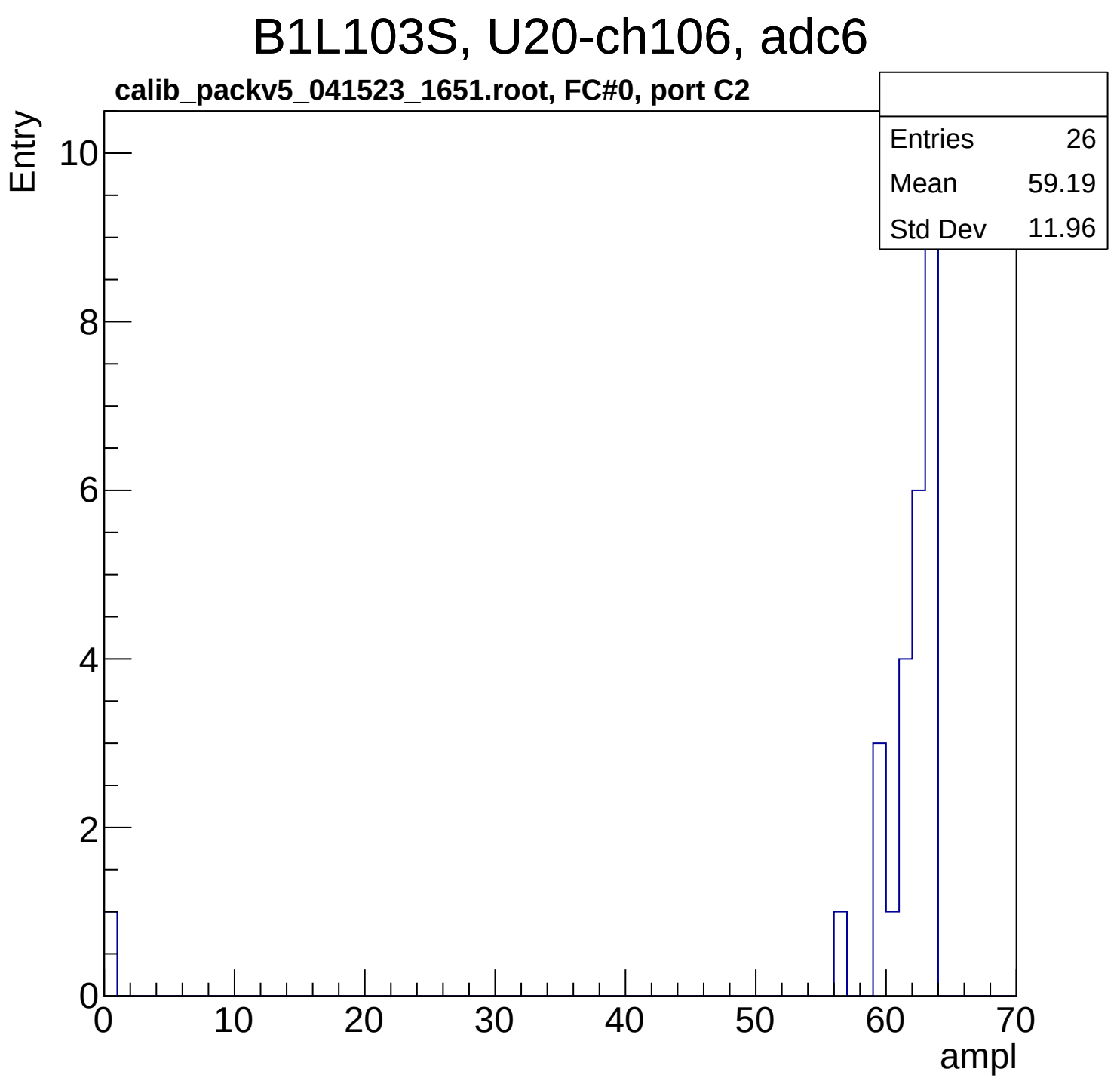
B1L103S, U20-ch106, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 59.19
Std Dev 11.96
Entry
ampl
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0
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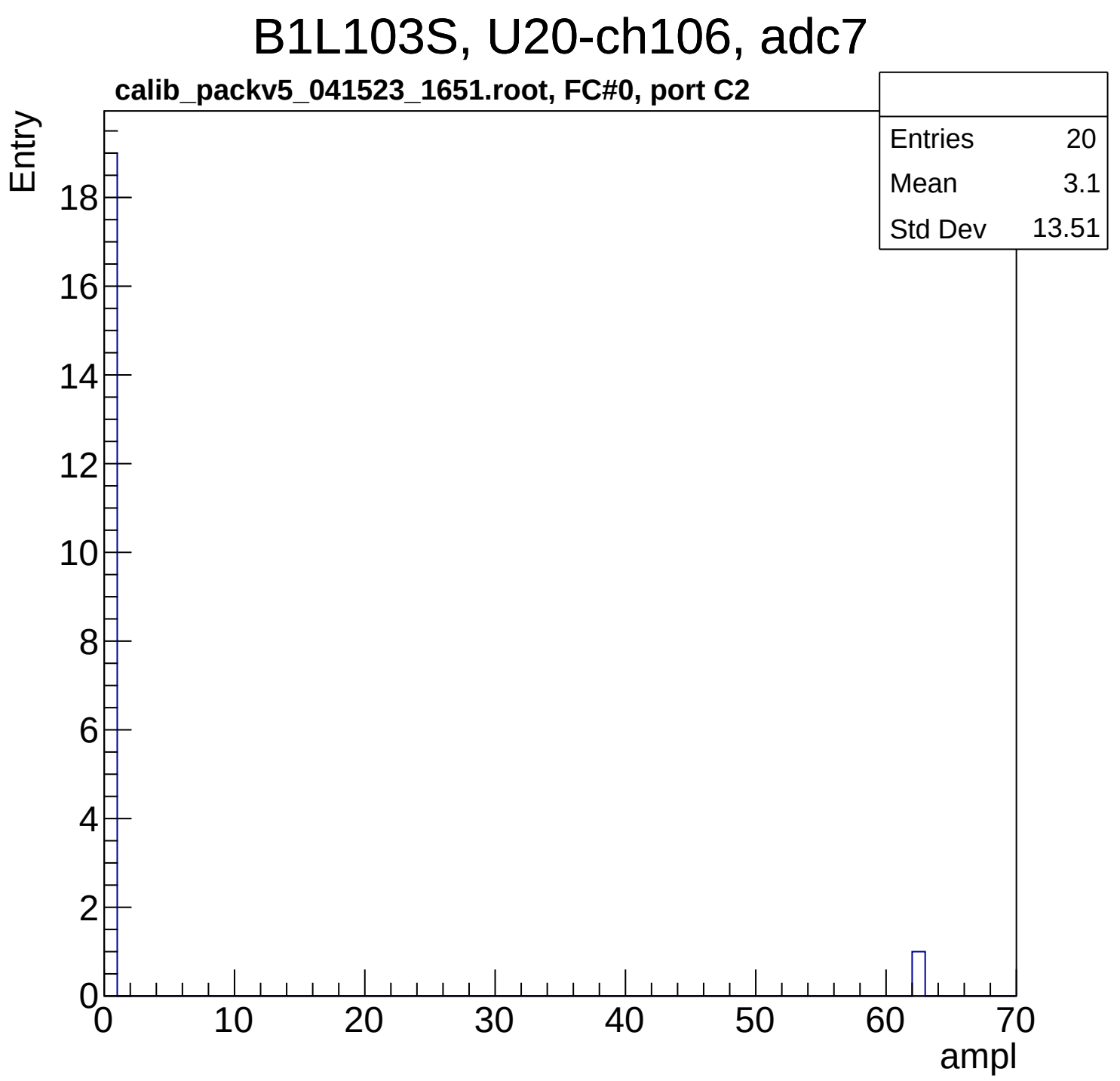
70


B1L103S, U20-ch106, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
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6
8
10
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14
16
18
0
10
20
30
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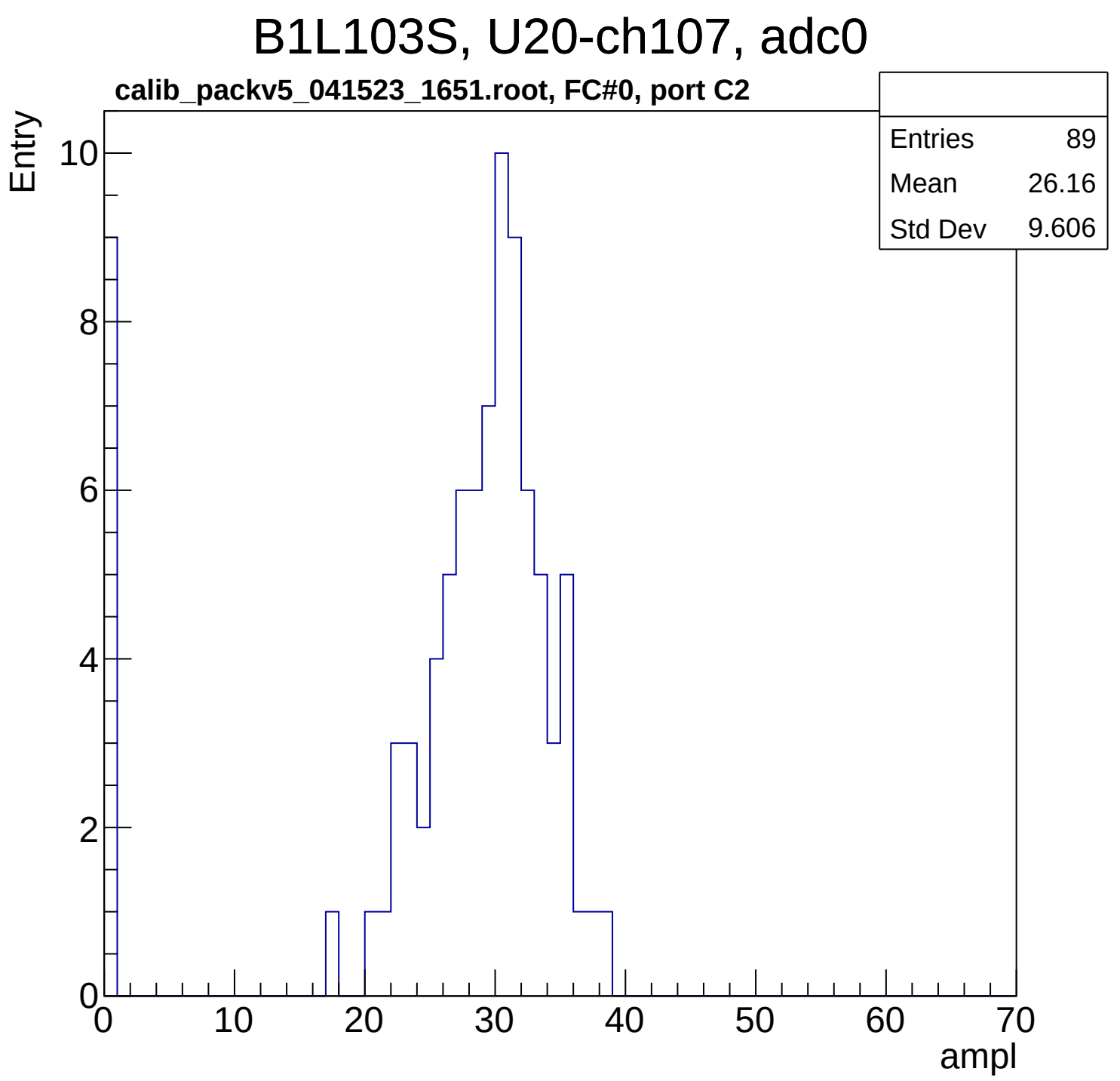
50
60
70
ampl


B1L103S, U20-ch107, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 26.16
Std Dev 9.606
Entry
ampl
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4
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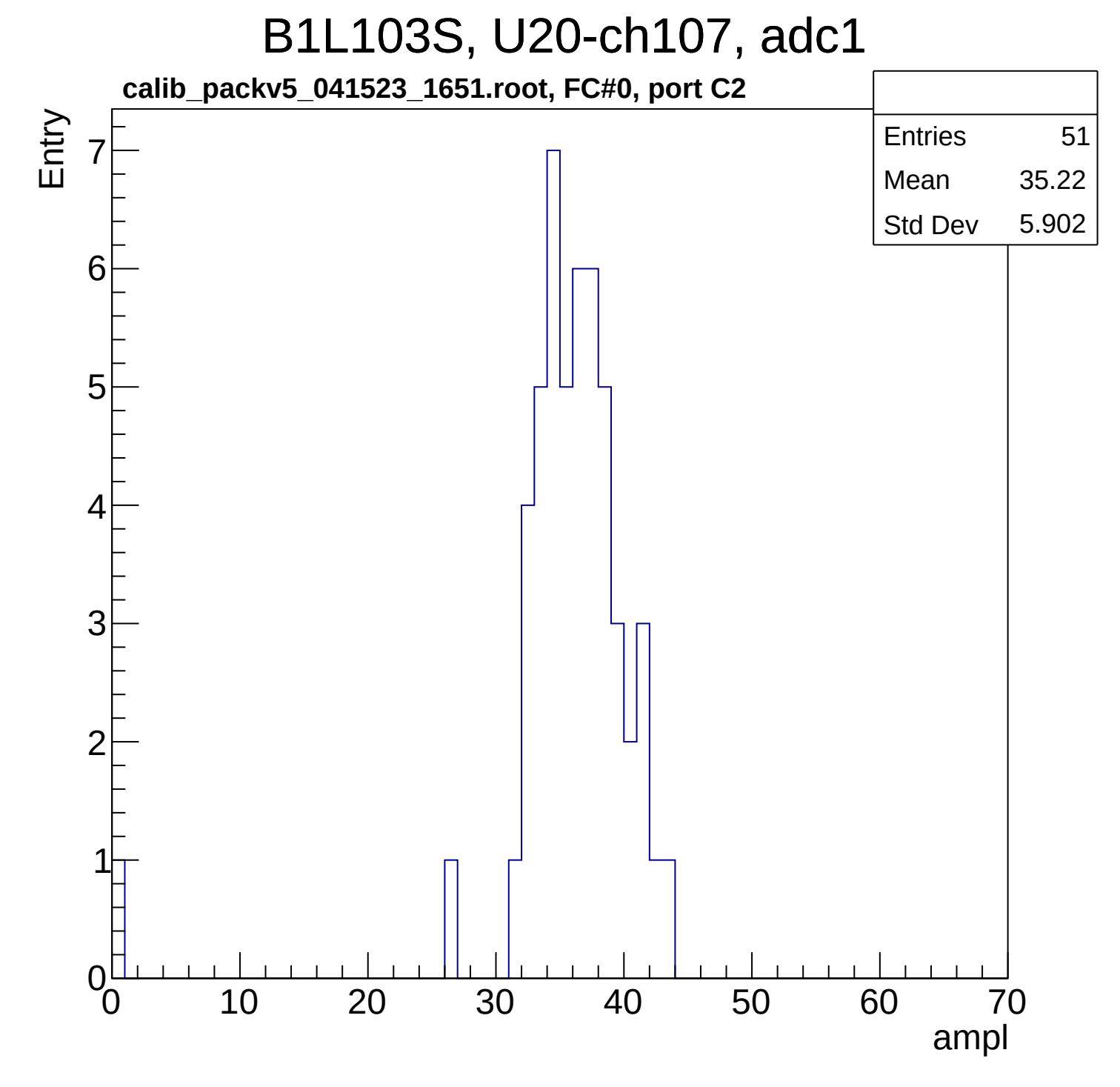
8
10
0
10
20
30
40
50
60
70


B1L103S, U20-ch107, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 35.22
Std Dev 5.902
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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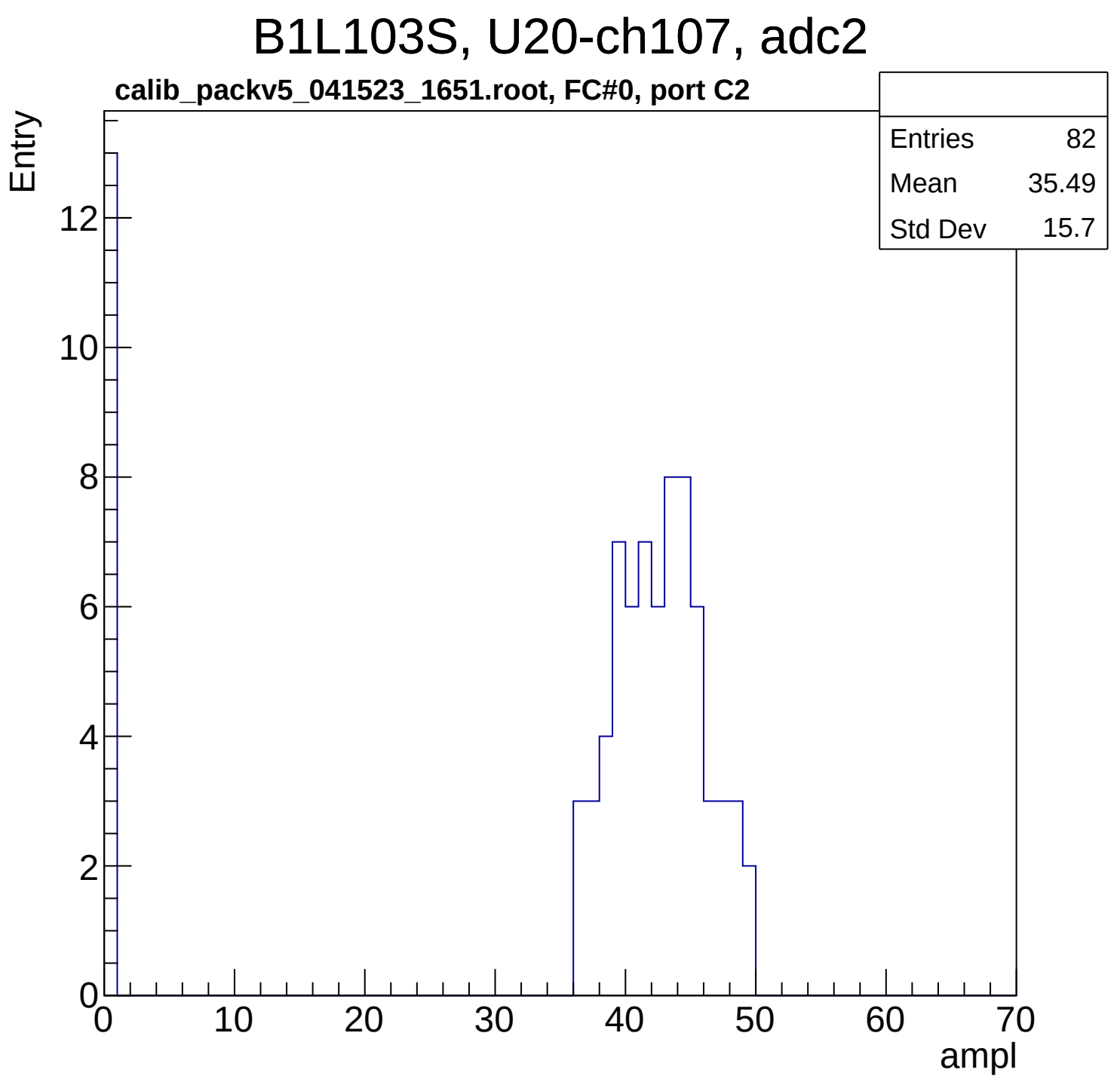
40
50
60
70


B1L103S, U20-ch107, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 35.49
Std Dev 15.7
Entry
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10
20
30
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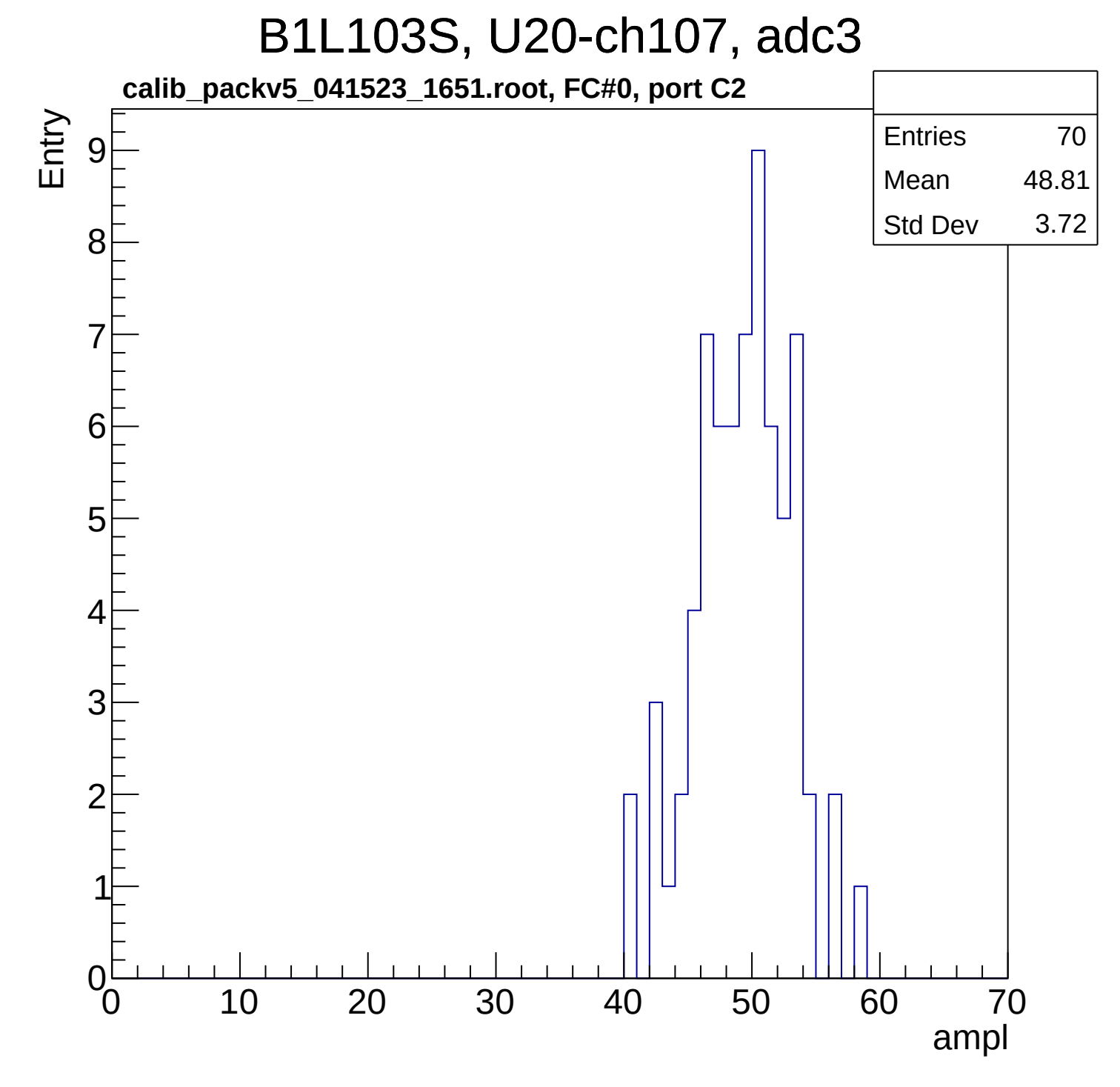
50
60
70
ampl


B1L103S, U20-ch107, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 48.81
Std Dev 3.72
Entry
ampl
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2
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4
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6
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0
10
20
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40
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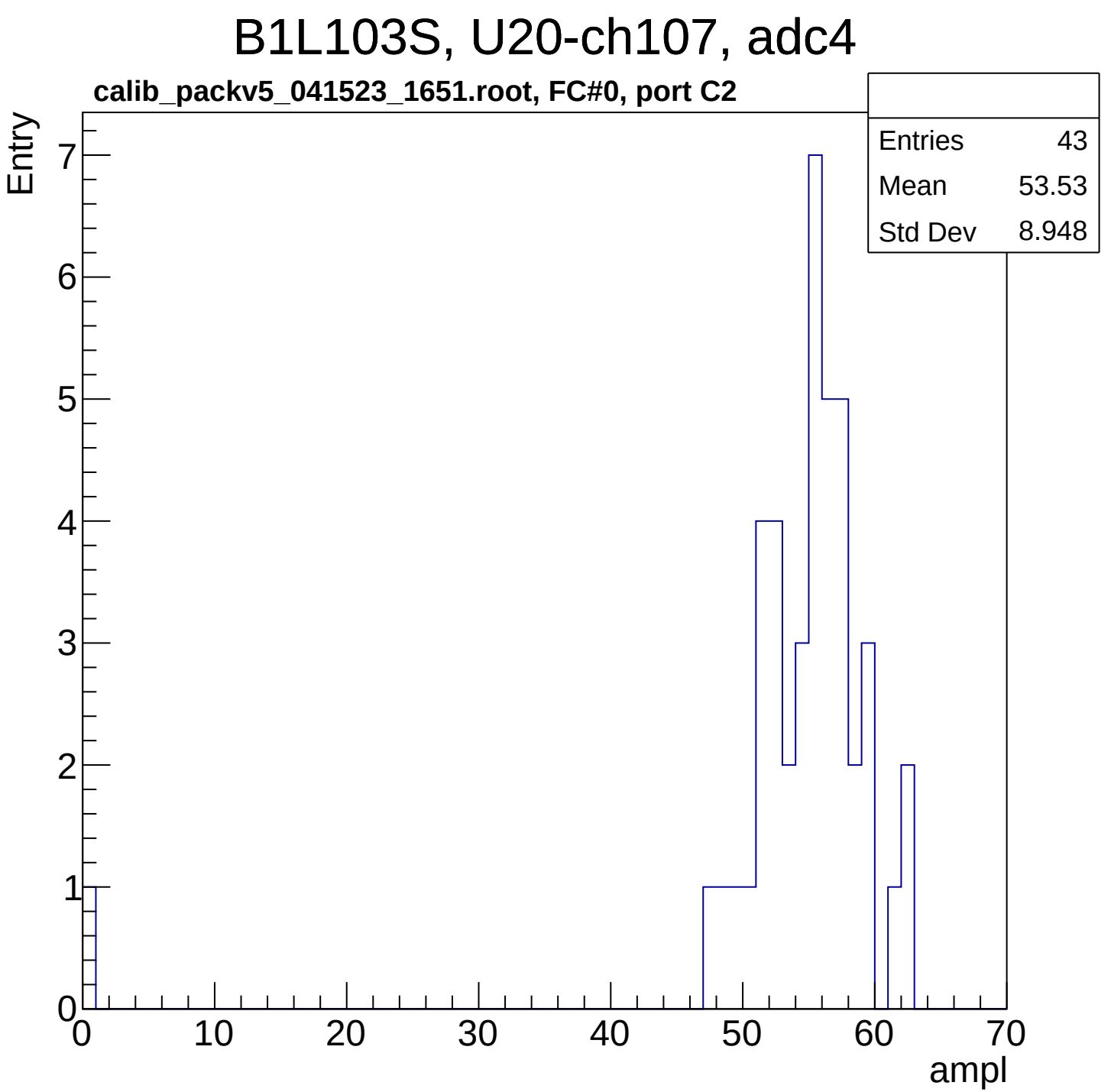
60
70


B1L103S, U20-ch107, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 53.53
Std Dev 8.948
Entry
ampl
0
1
2
3
4
5
6
7
0
10
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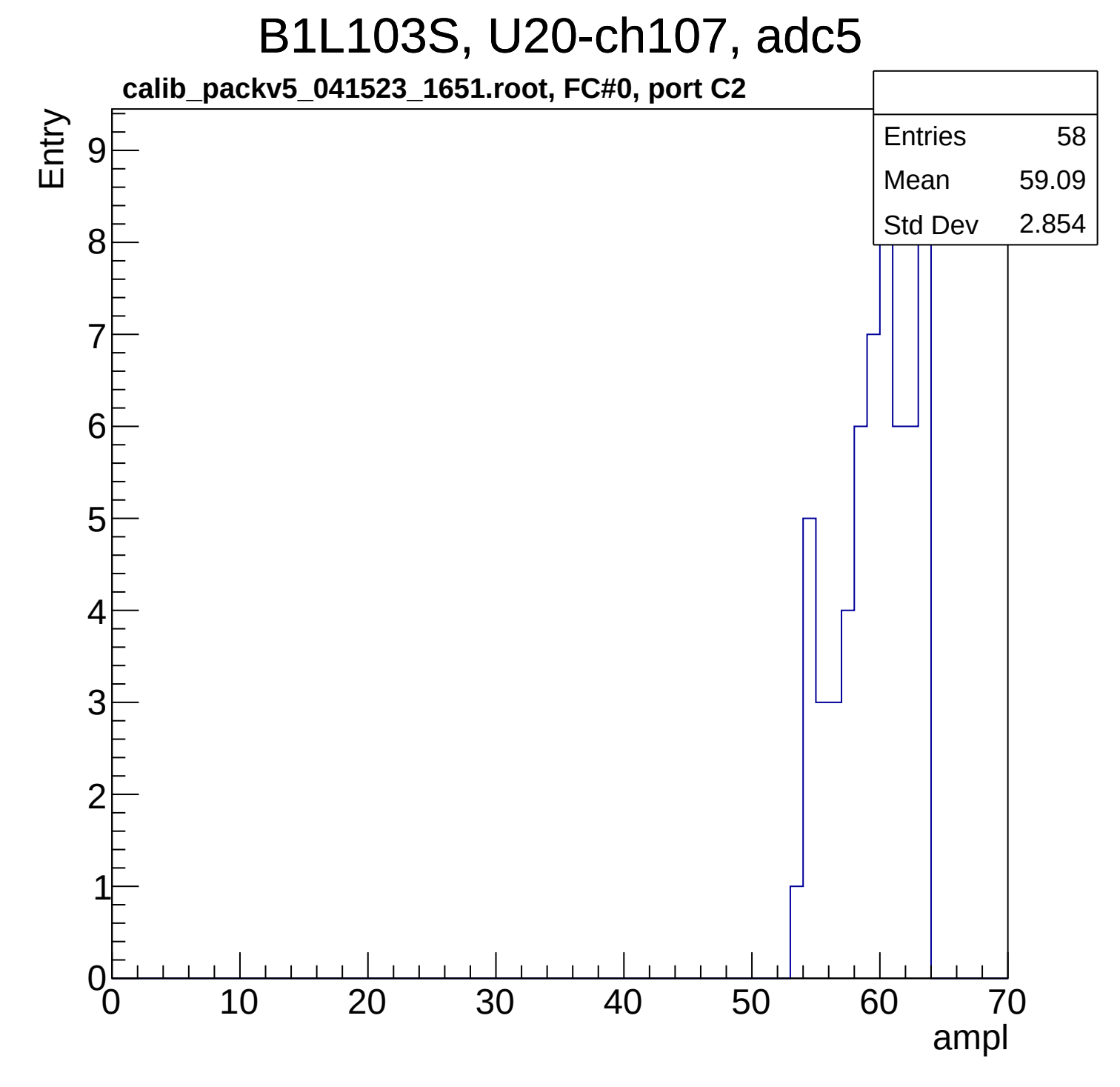
B1L103S, U20-ch107, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 59.09
Std Dev 2.854
Entry
ampl
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2
3
4
5
6
7
8
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0
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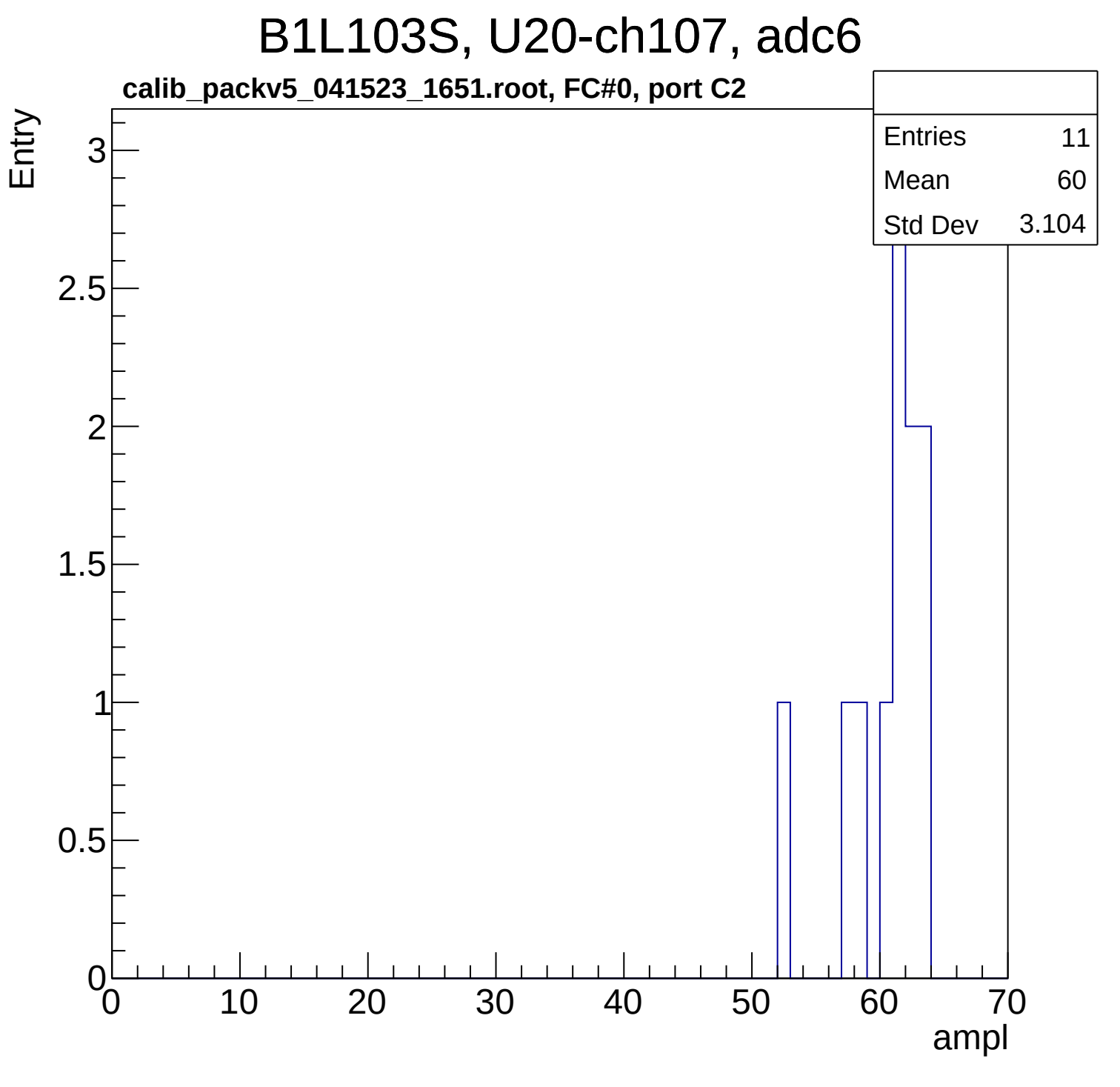
B1L103S, U20-ch107, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 60
Std Dev 3.104
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
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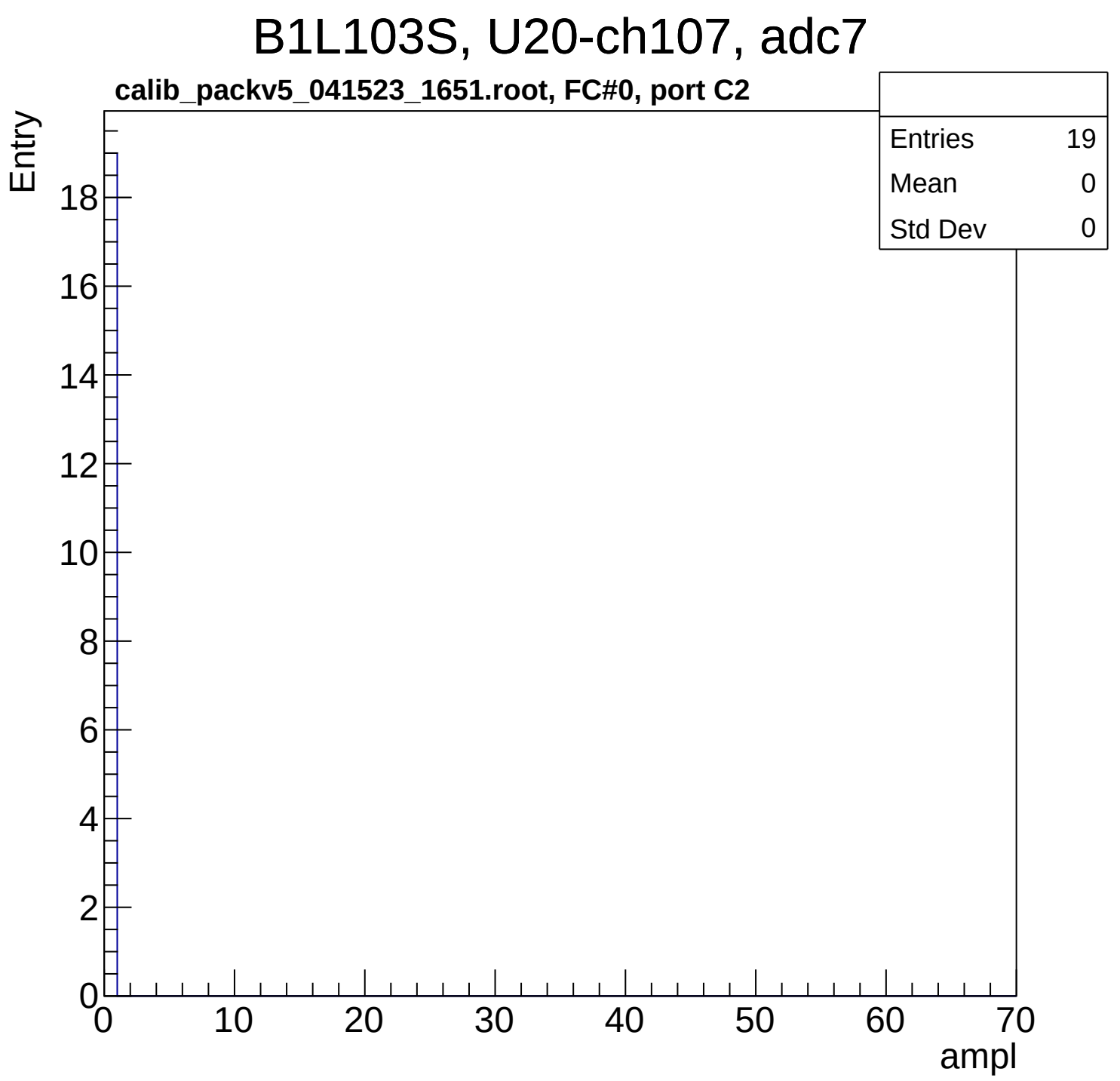
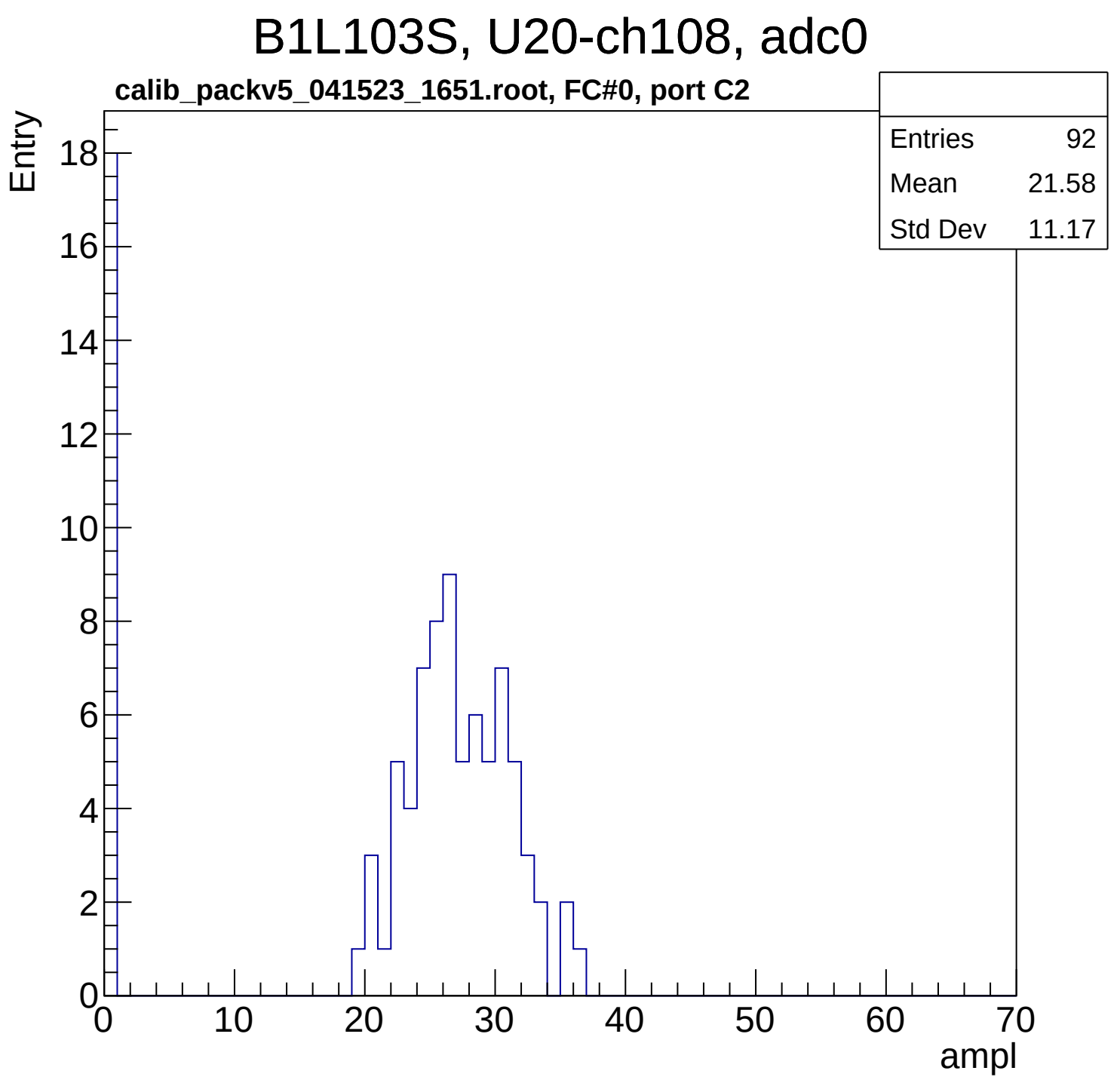
40
50
60
70


B1L103S, U20-ch107, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch108, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 21.58
Std Dev 11.17
Entry
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6
8
10
12
14
16
18
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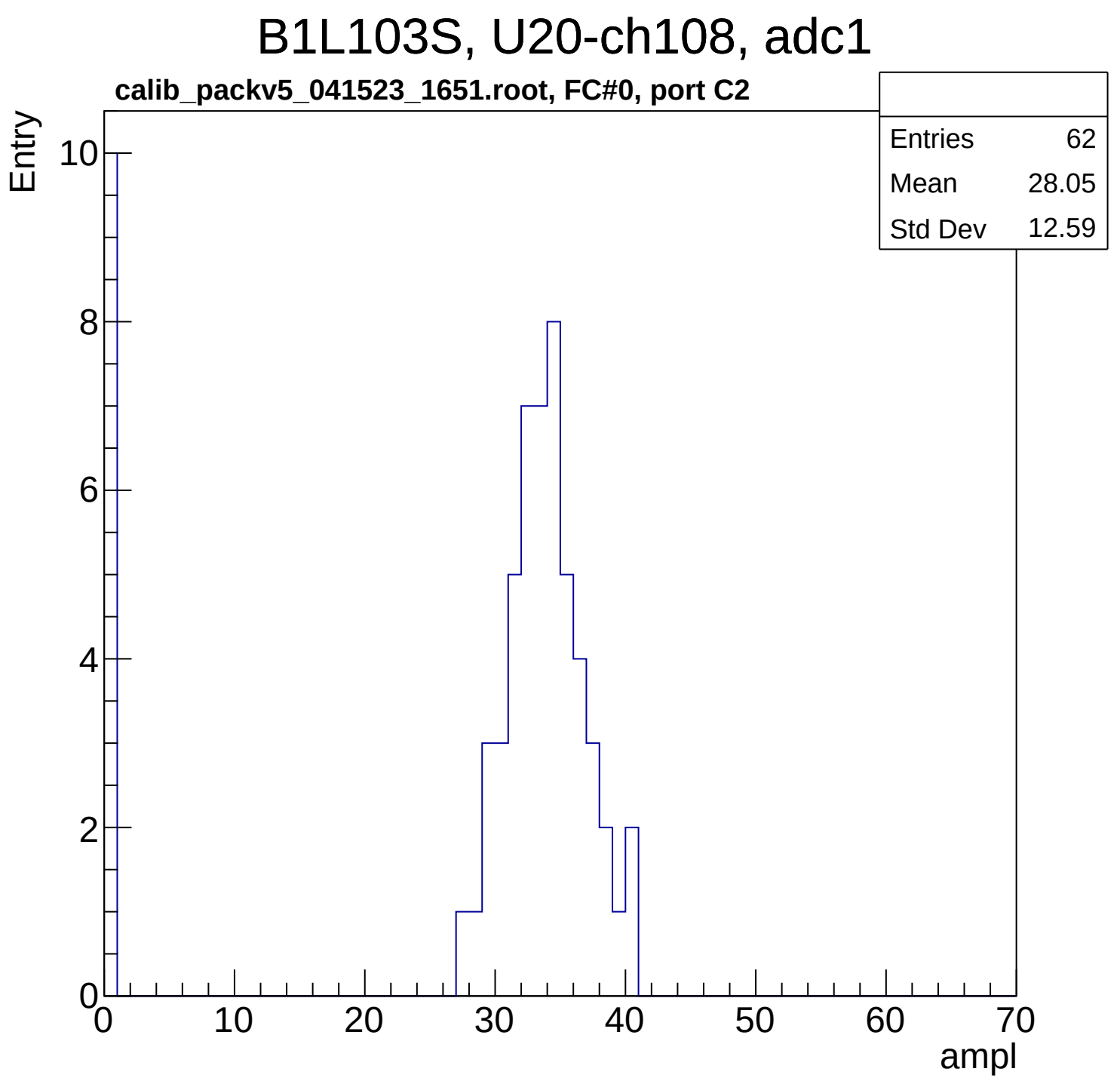
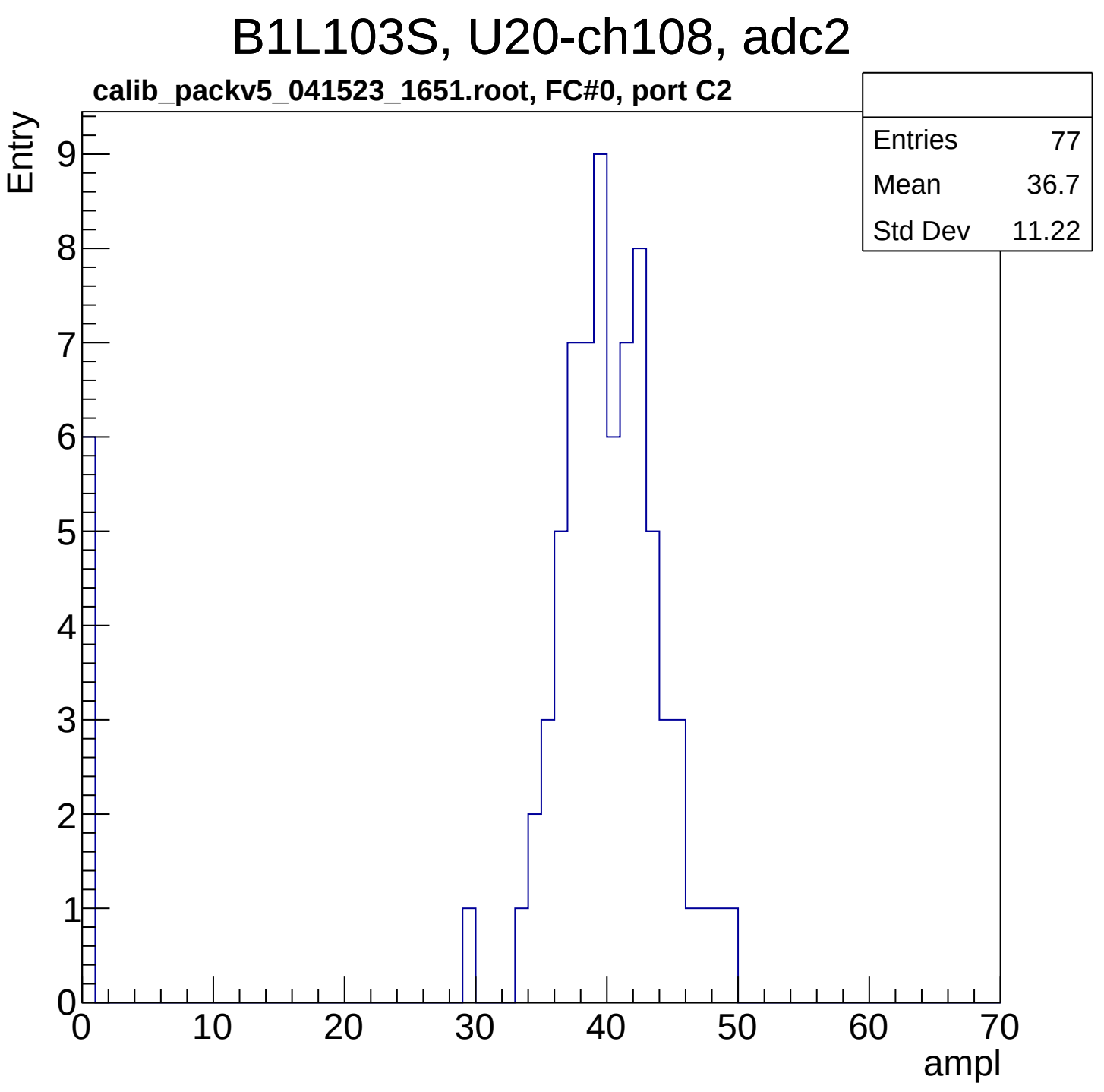
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch108, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 28.05
Std Dev 12.59
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch108, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 36.7
Std Dev 11.22
Entry
ampl
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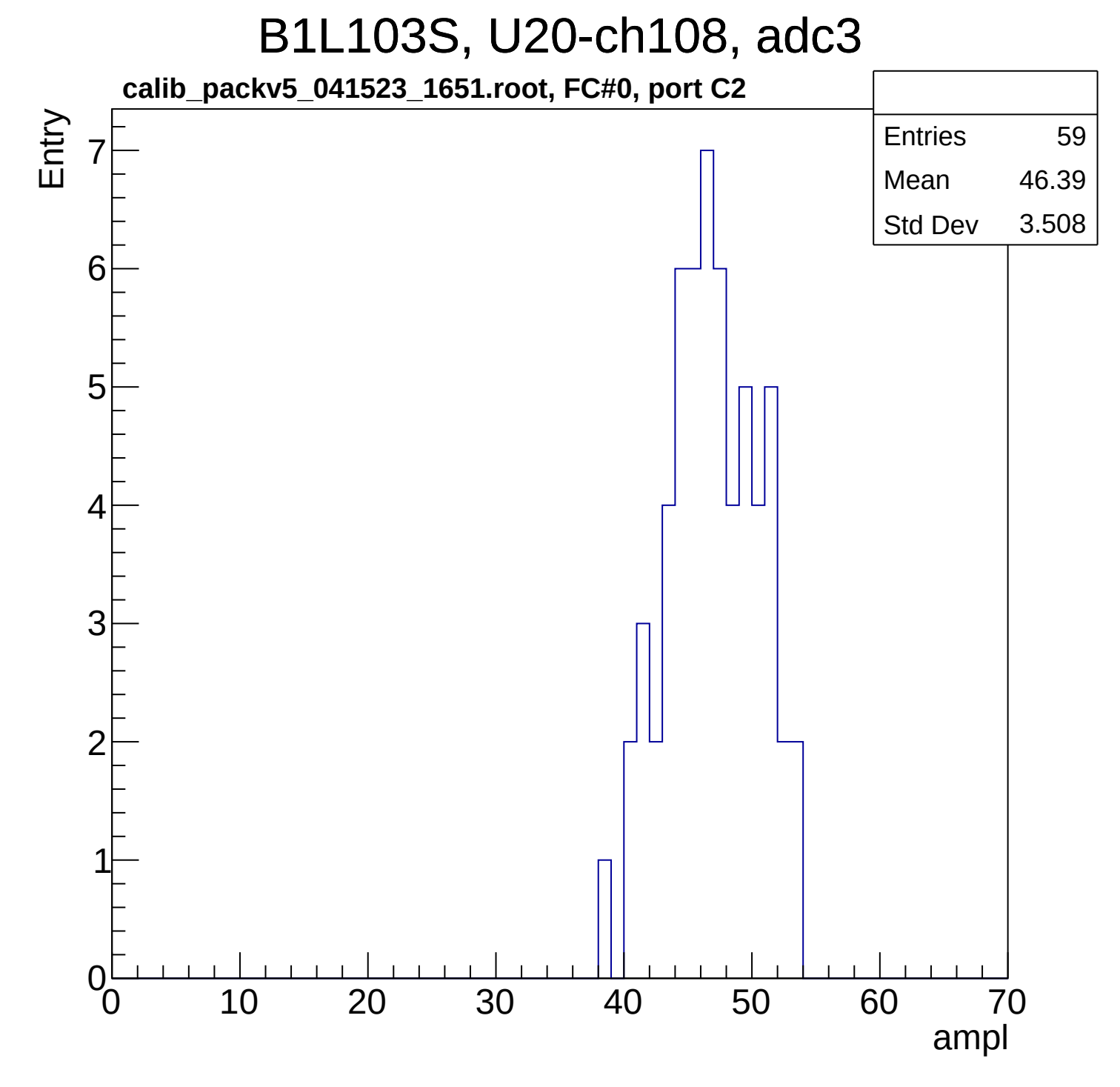
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch108, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 46.39
Std Dev 3.508
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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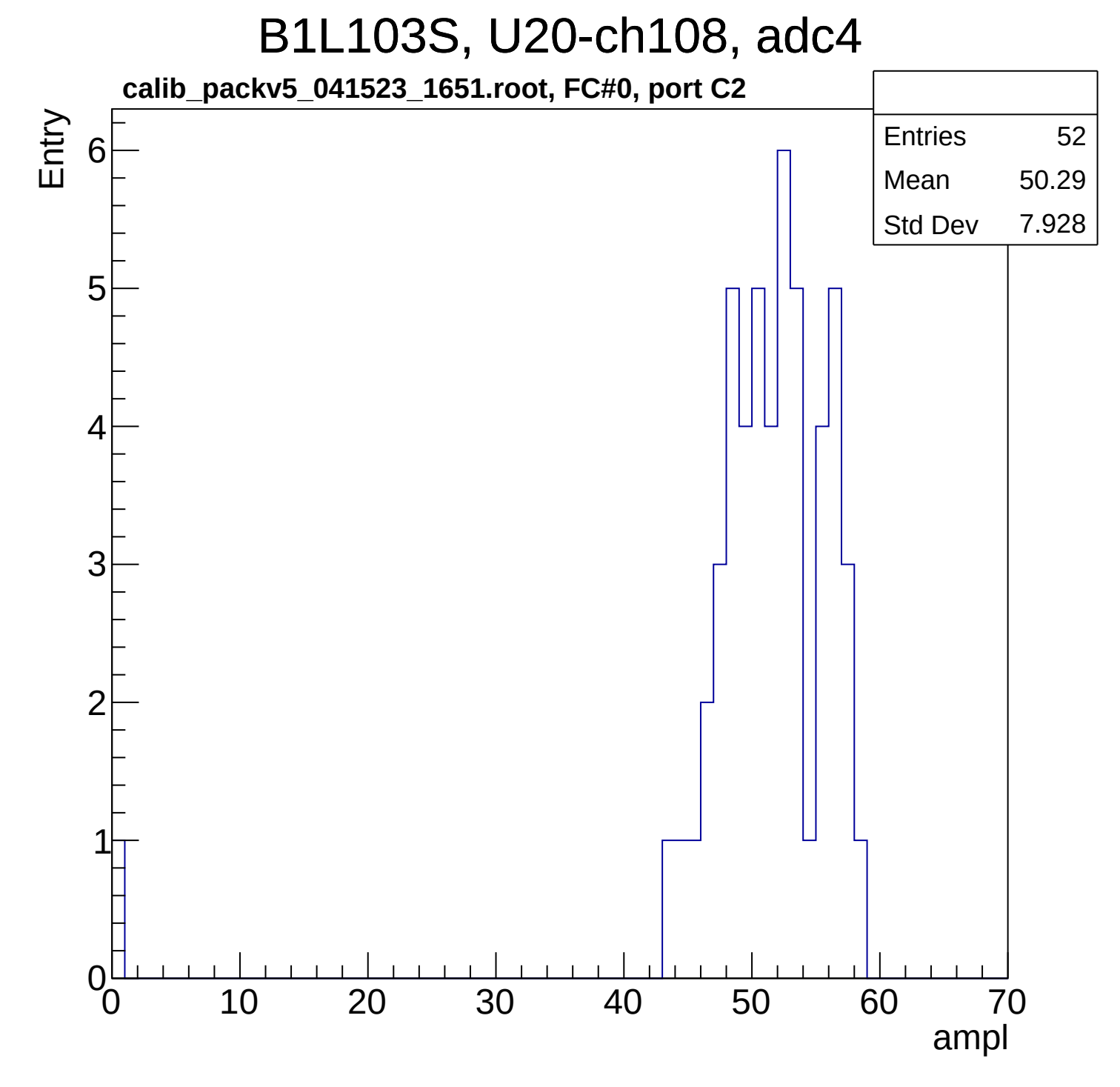
B1L103S, U20-ch108, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 50.29
Std Dev 7.928
Entry
ampl
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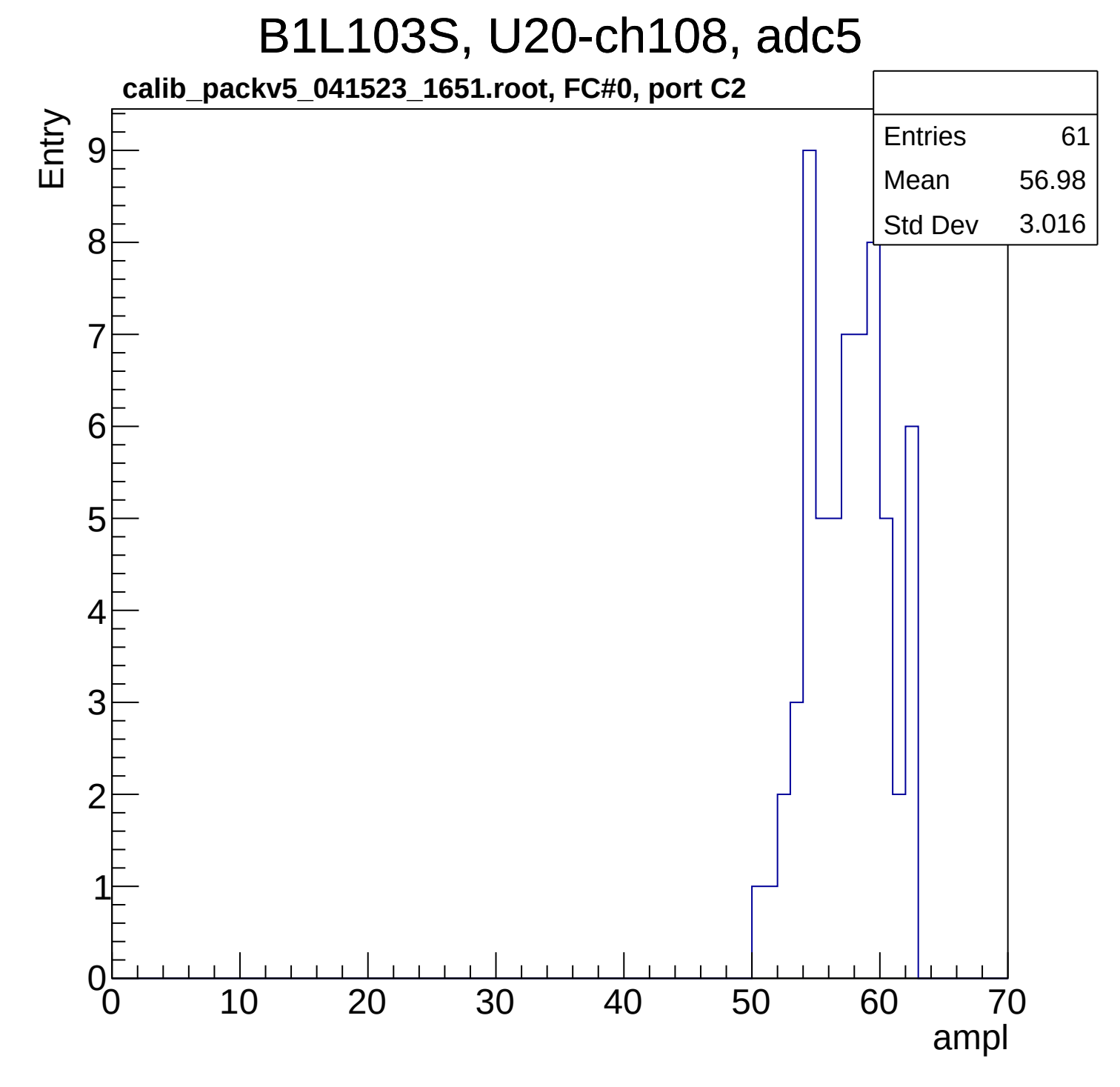
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U20-ch108, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 56.98
Std Dev 3.016
Entry
ampl
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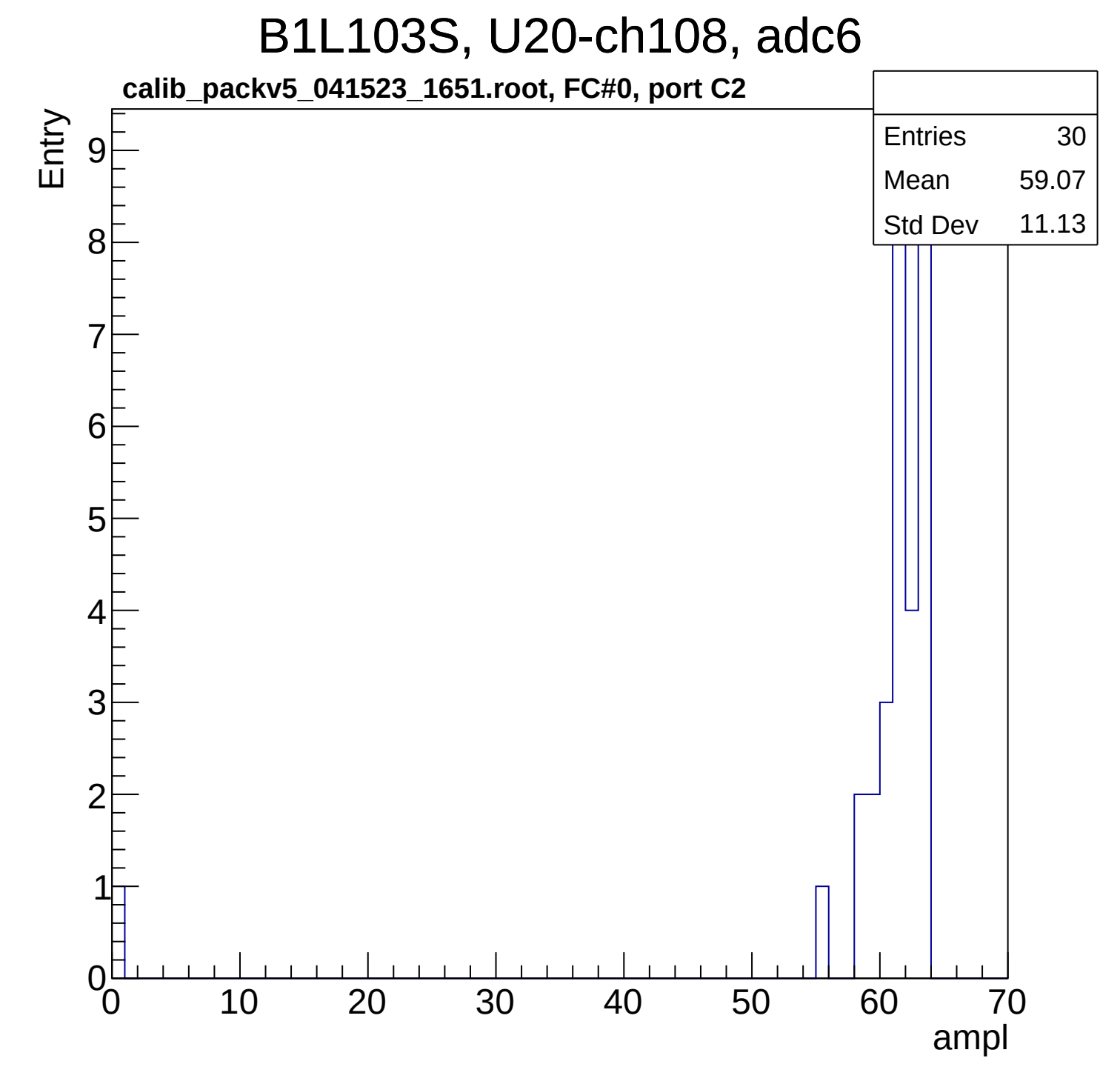
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch108, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 59.07
Std Dev 11.13
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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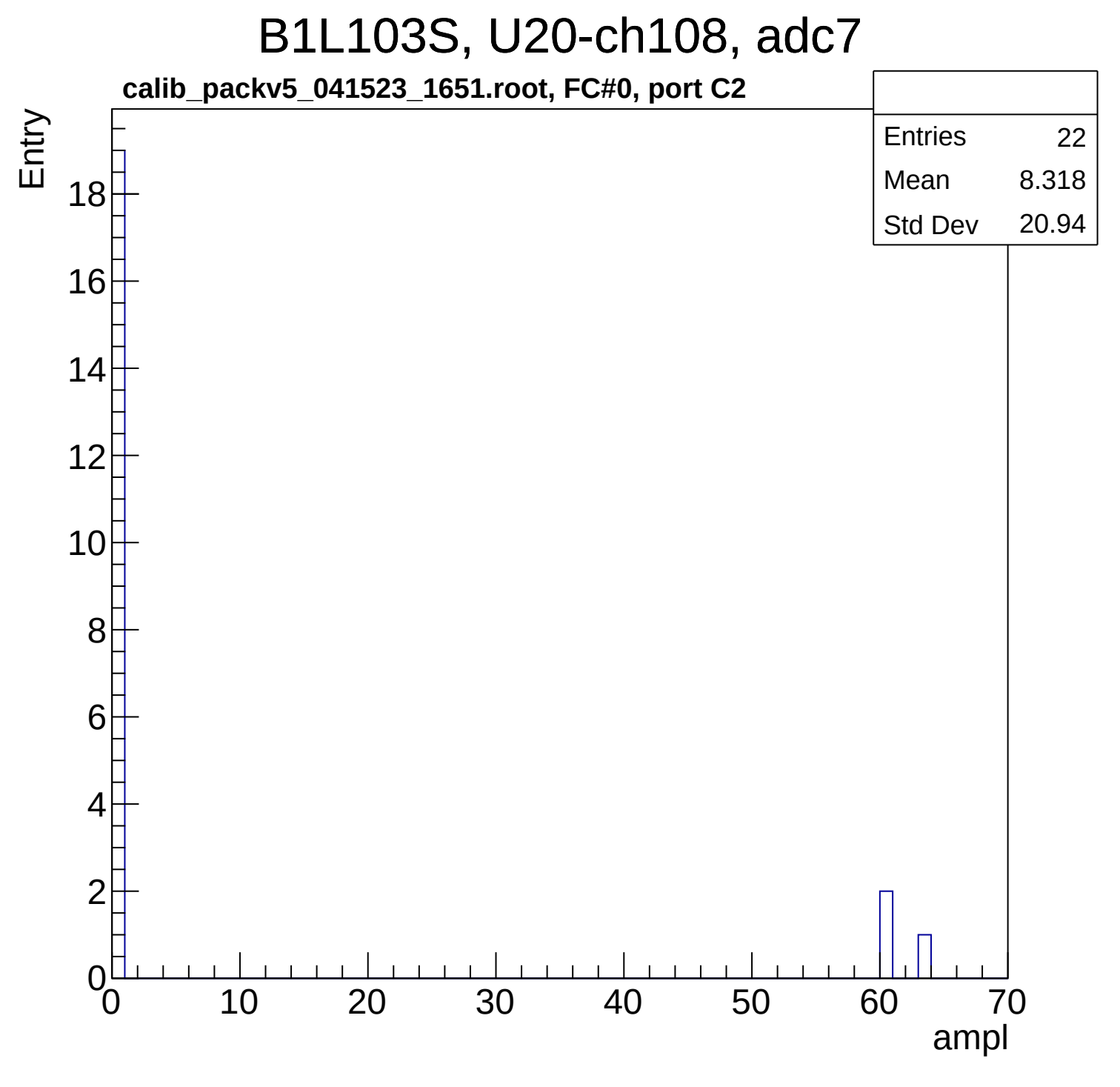
B1L103S, U20-ch108, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.318
Std Dev 20.94
Entry
0
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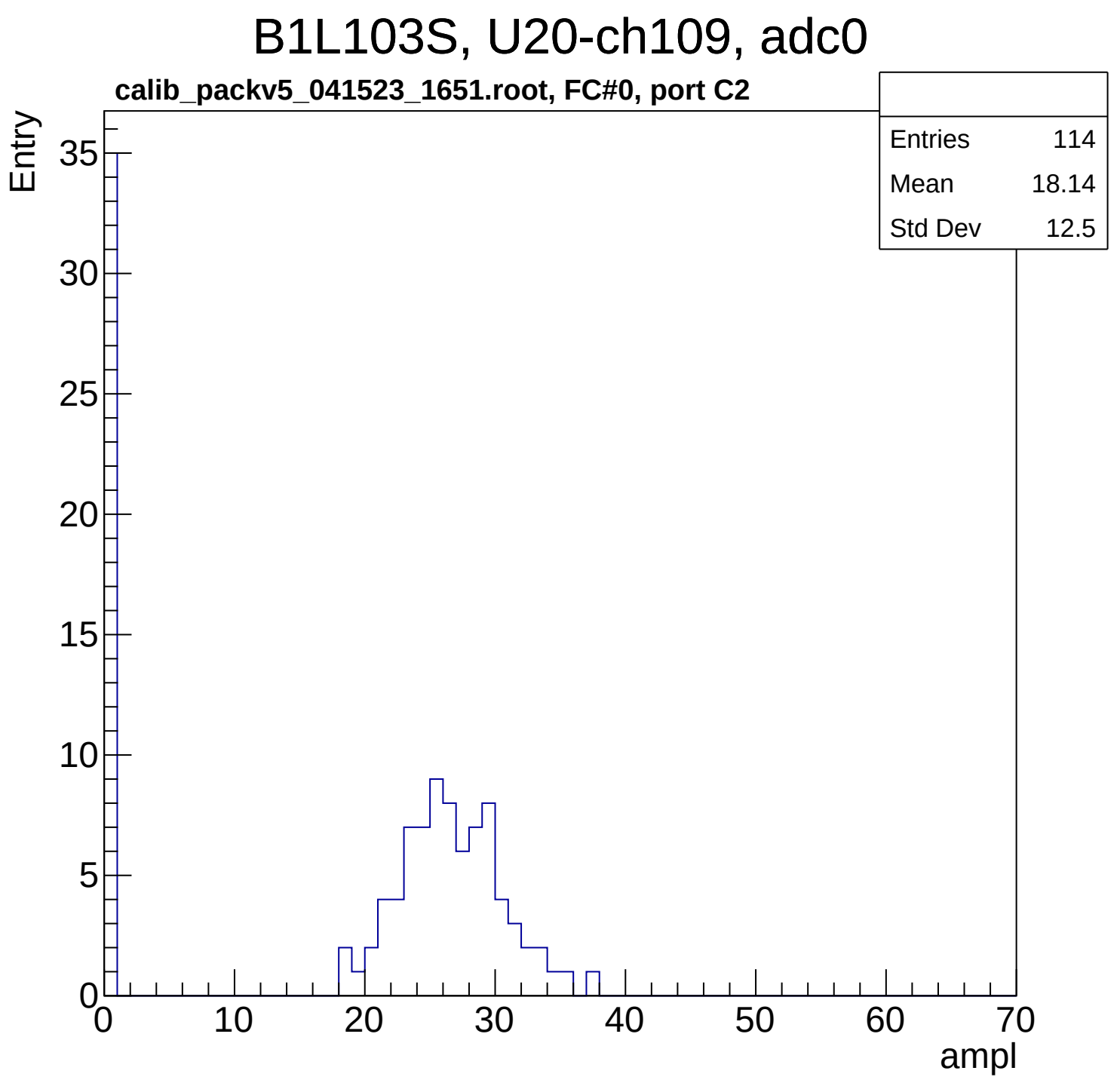
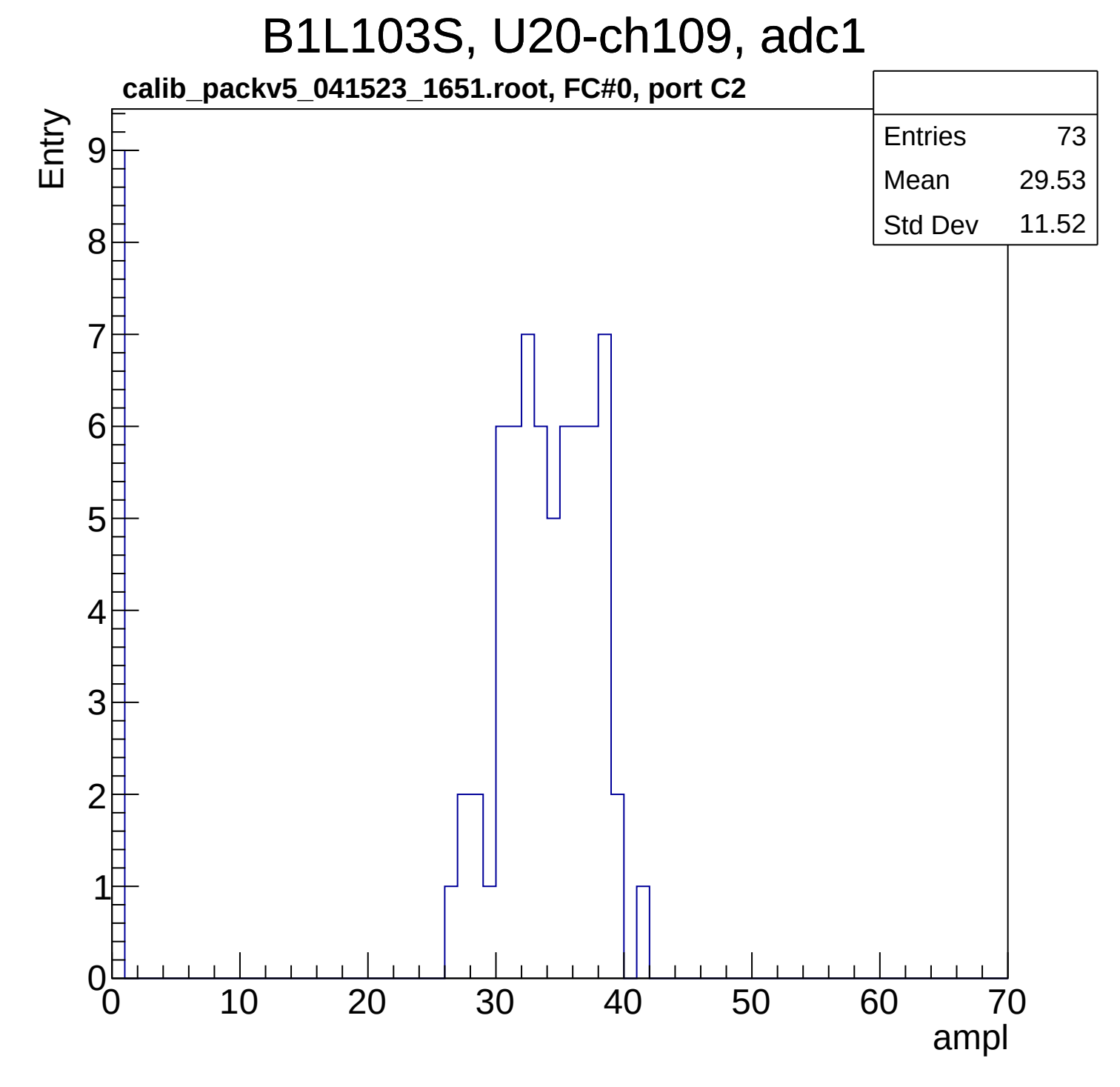
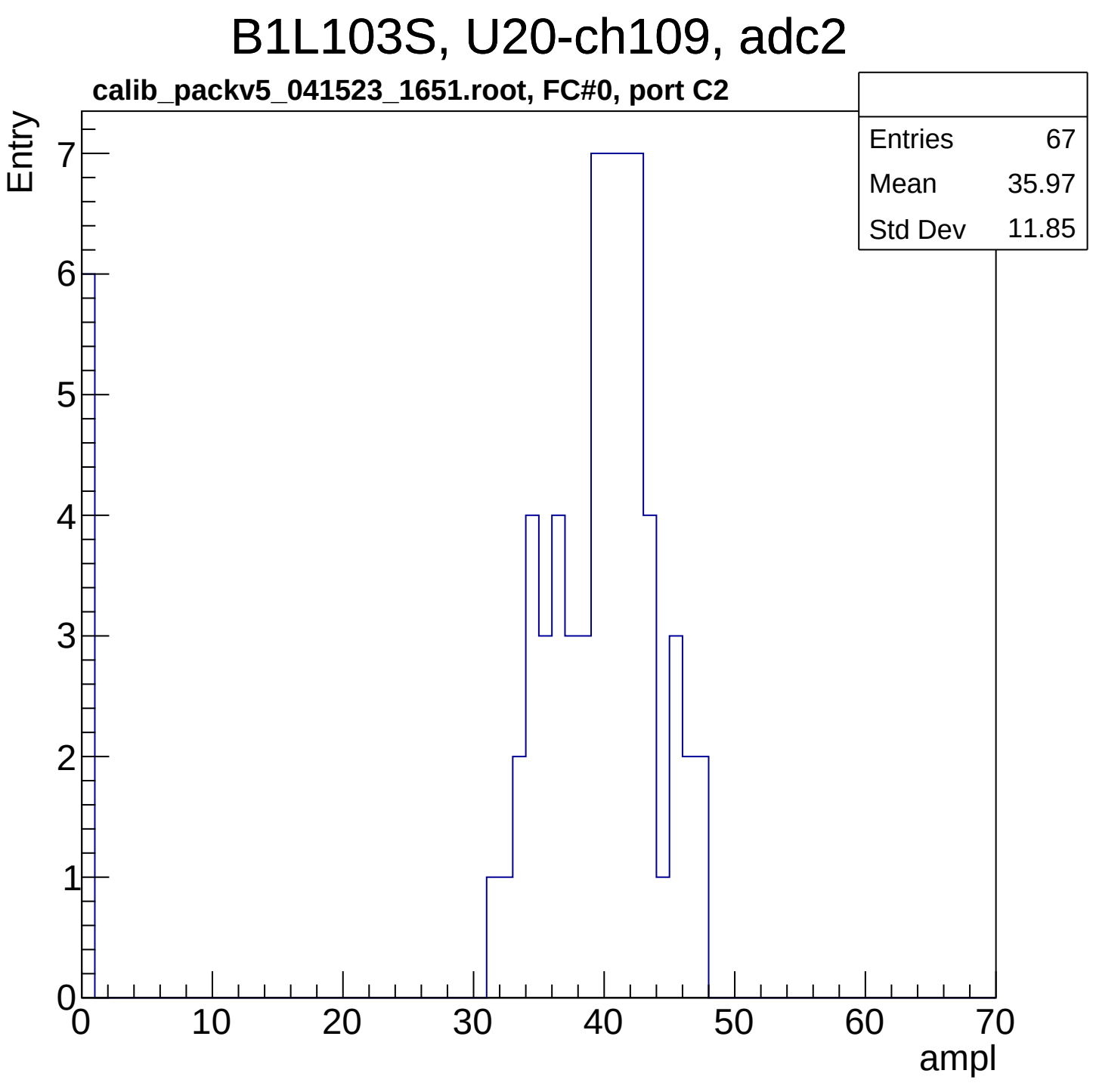
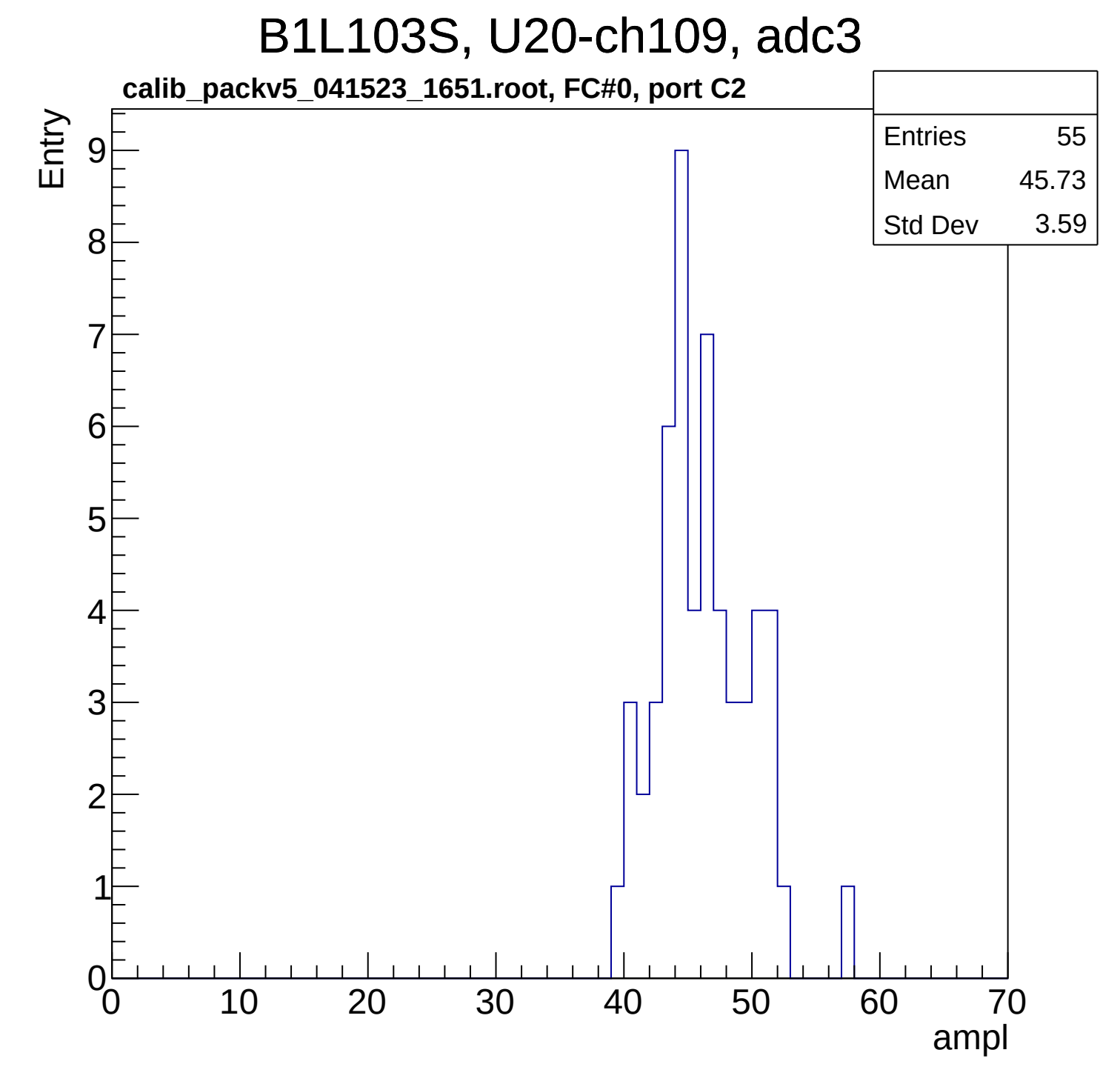
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch109, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 114
Mean 18.14
Std Dev 12.5
Entry
ampl
0
5
10
15
20
25
30
35
0
10
20
30
40
50
60
70


B1L103S, U20-ch109, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 29.53
Std Dev 11.52
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch109, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 35.97
Std Dev 11.85
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U20-ch109, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 45.73
Std Dev 3.59
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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30
40
50
60
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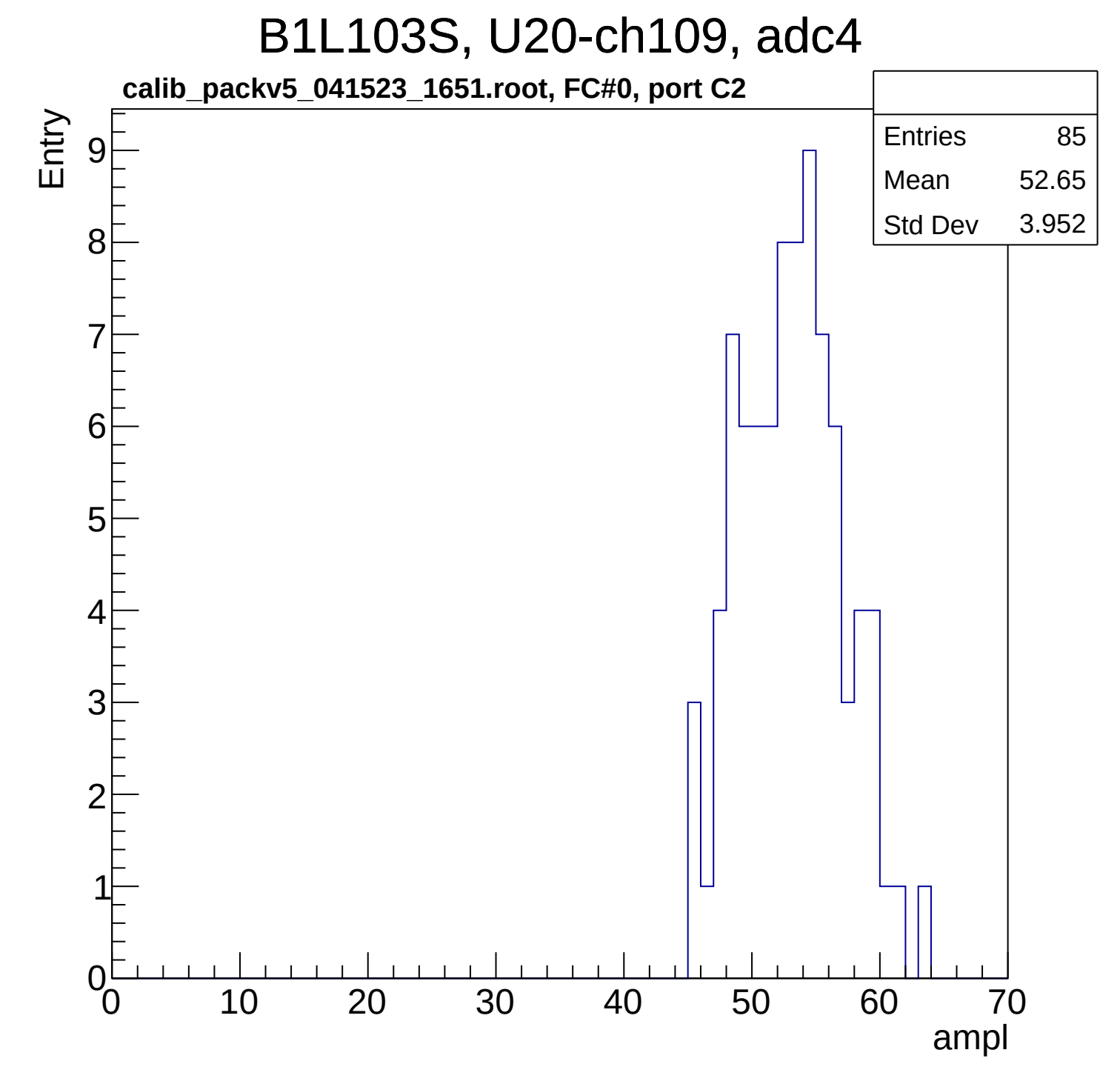
B1L103S, U20-ch109, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 52.65
Std Dev 3.952
Entry
ampl
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2
3
4
5
6
7
8
9
0
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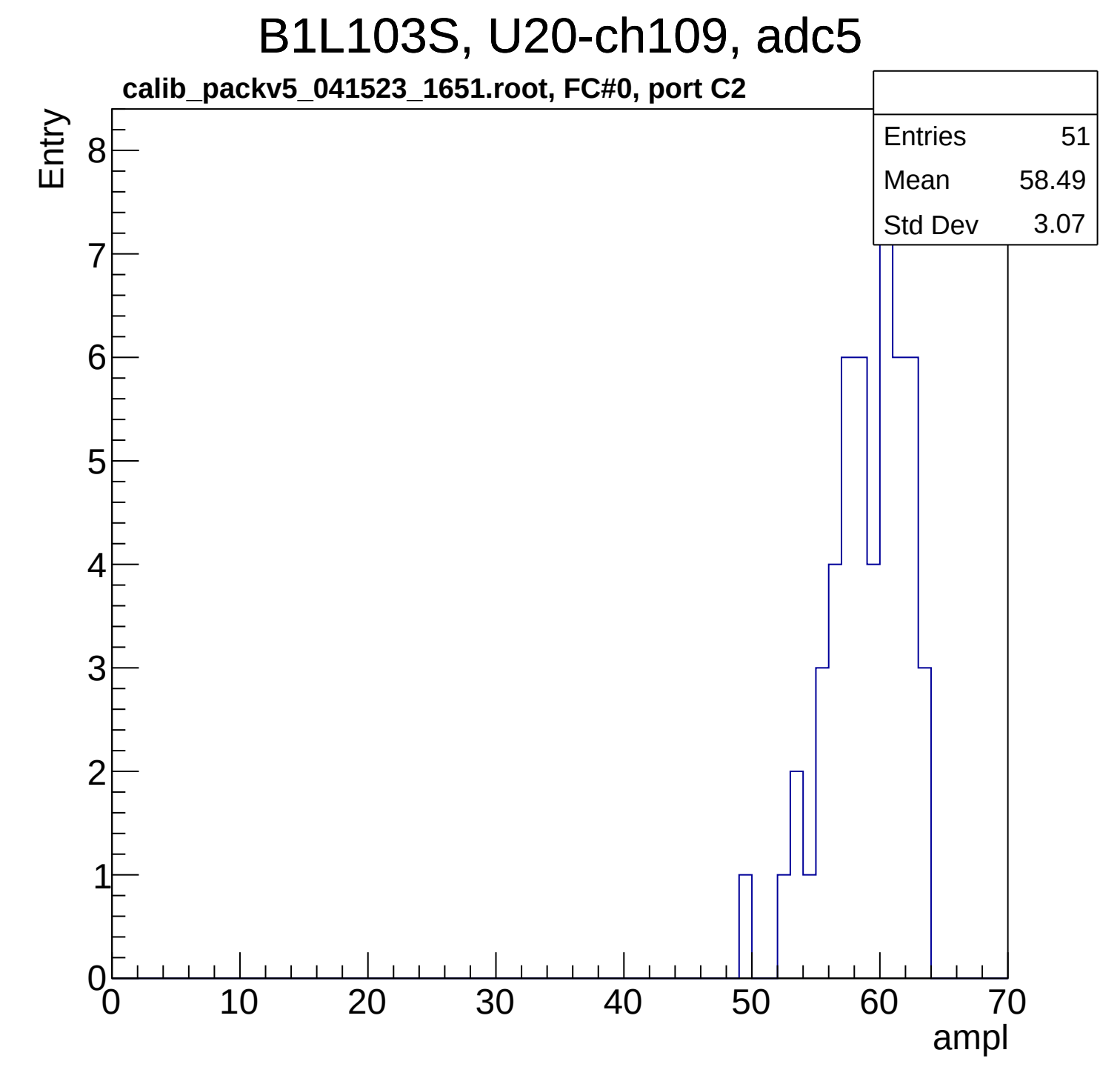
20
30
40
50
60
70


B1L103S, U20-ch109, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 58.49
Std Dev 3.07
Entry
ampl
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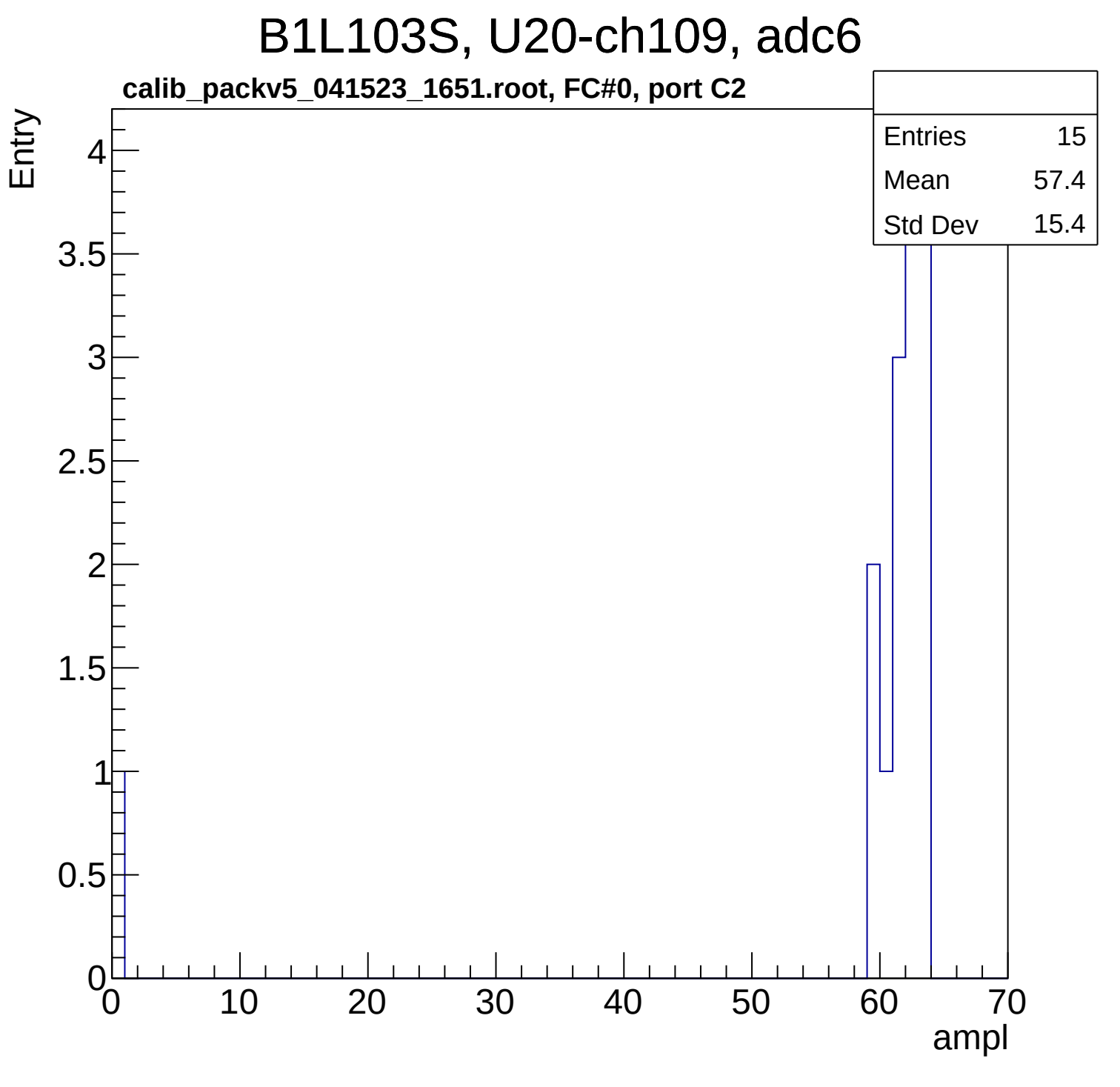
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch109, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 57.4
Std Dev 15.4
Entry
ampl
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0.5
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1.5
2
2.5
3
3.5
4
0
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20
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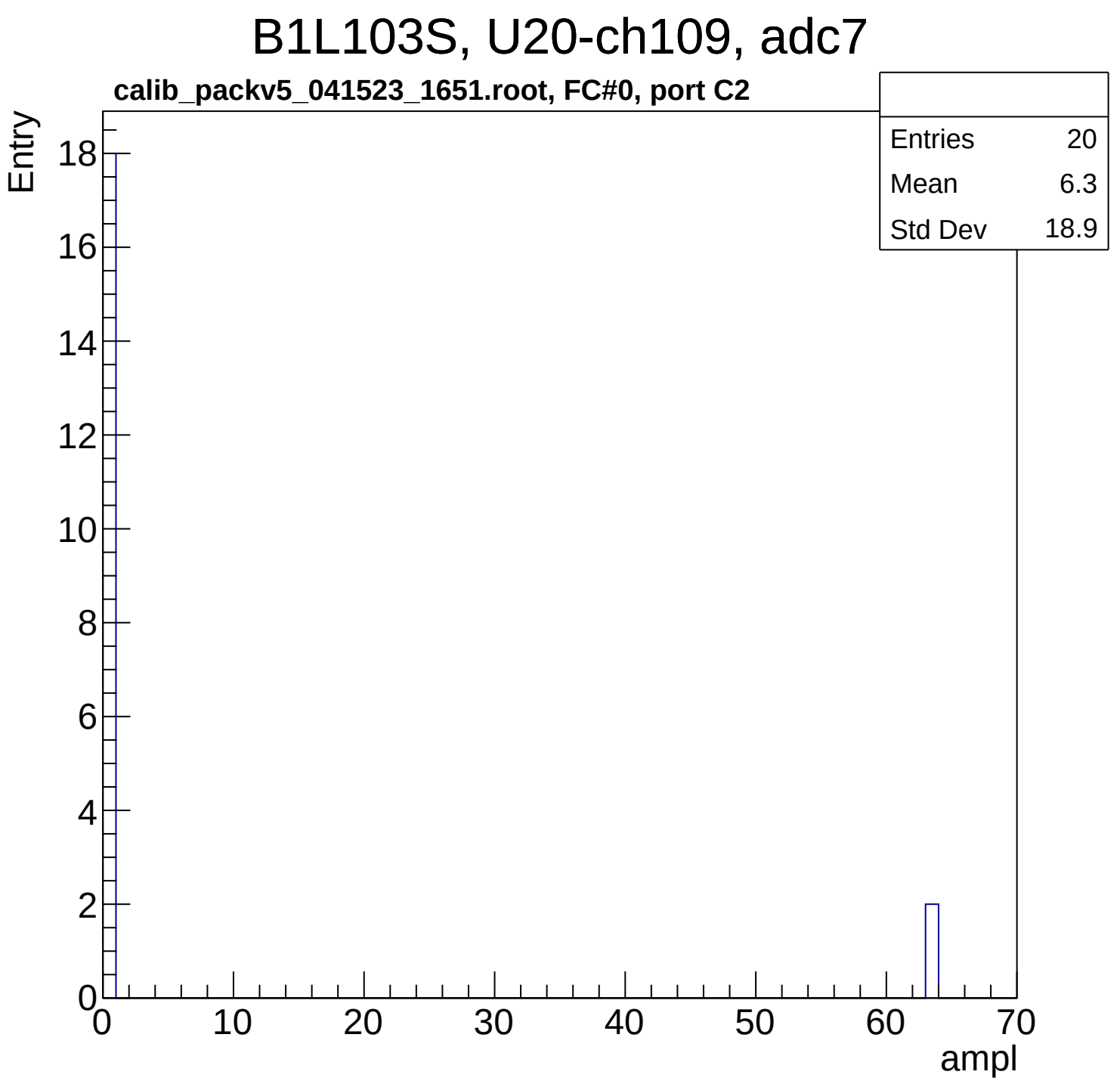
40
50
60
70


B1L103S, U20-ch109, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 6.3
Std Dev 18.9
Entry
0
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6
8
10
12
14
16
18
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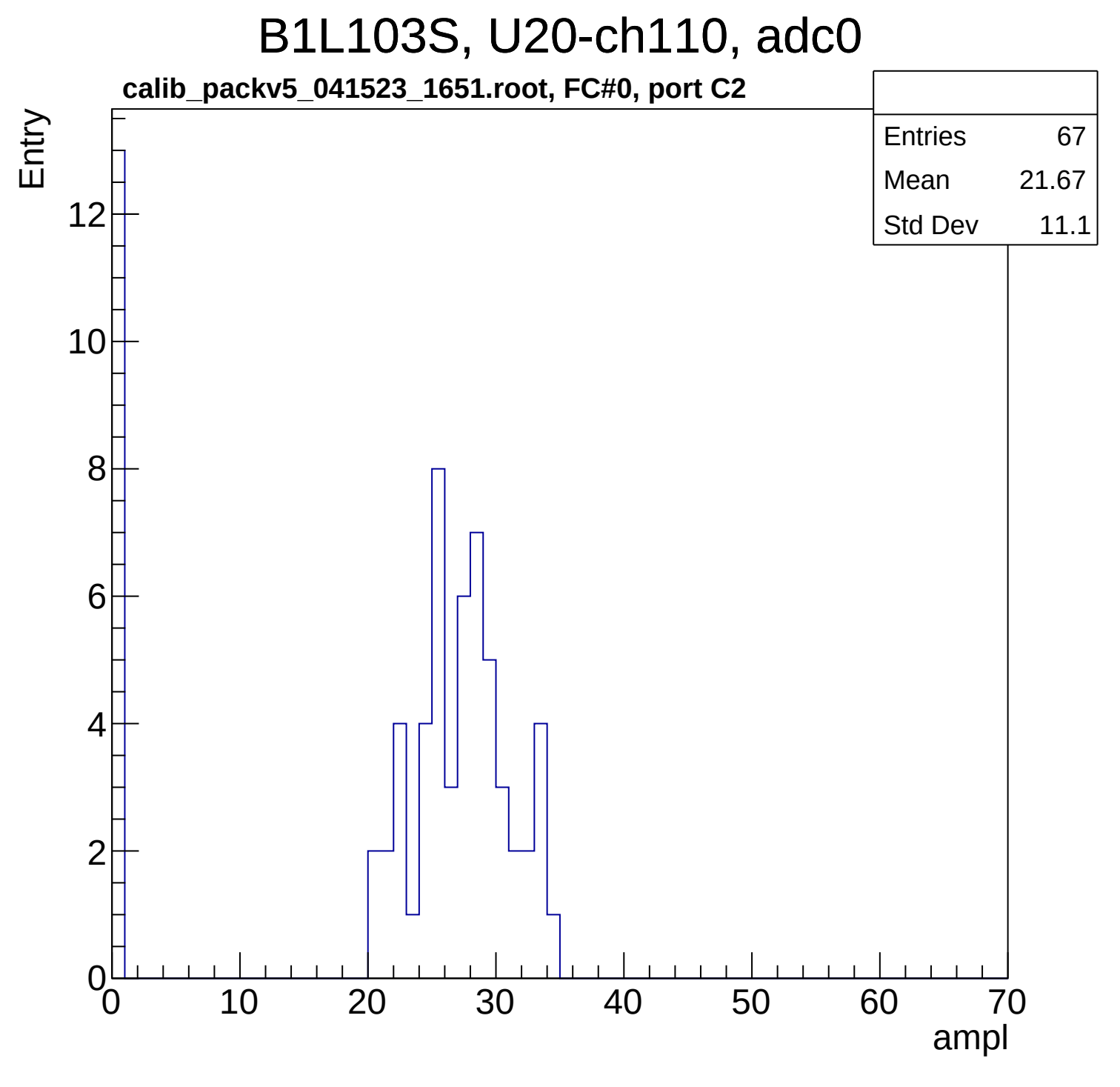
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch110, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 21.67
Std Dev 11.1
Entry
0
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4
6
8
10
12
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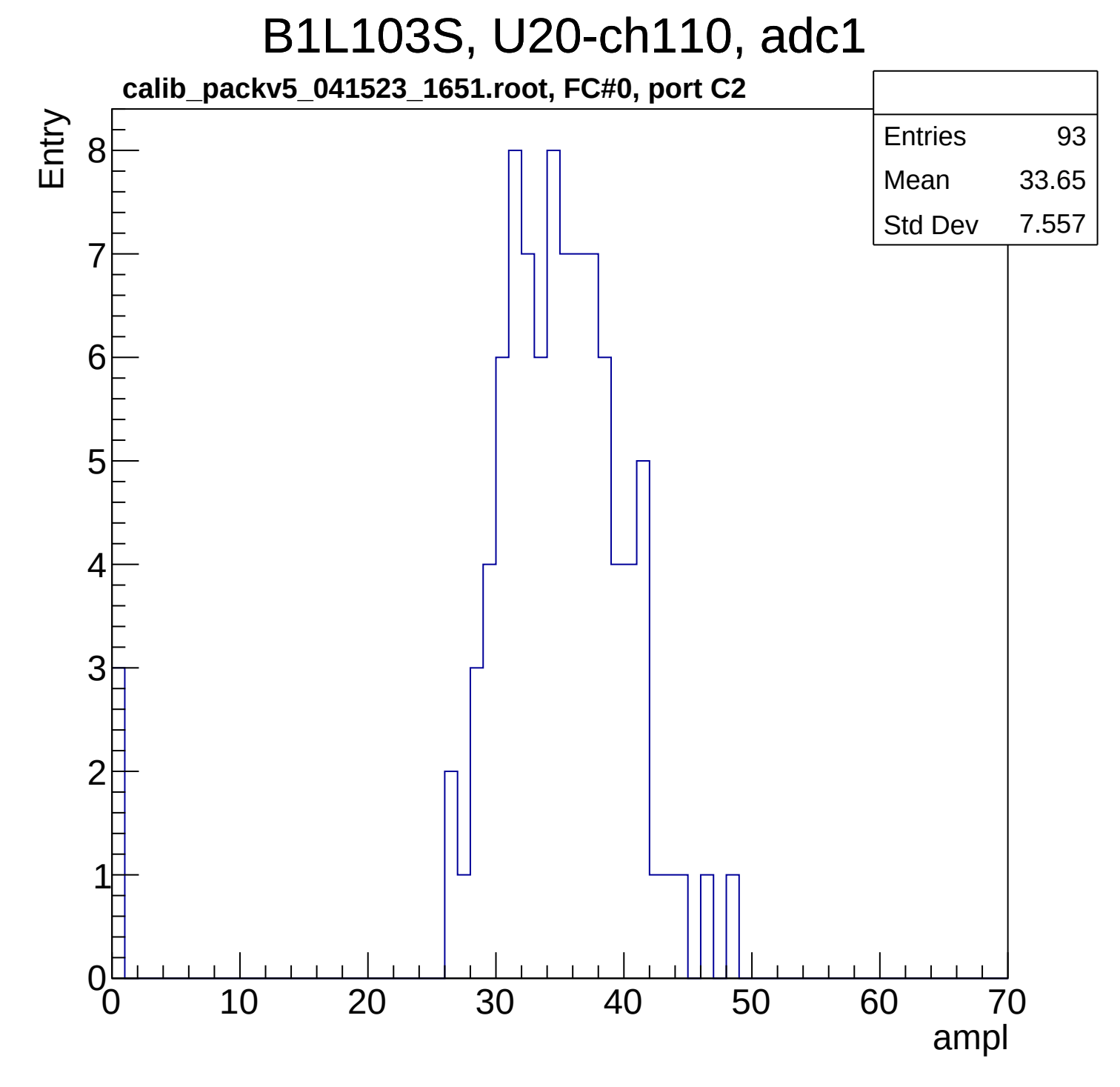
50
60
70
ampl


B1L103S, U20-ch110, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 33.65
Std Dev 7.557
Entry
ampl
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6
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0
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20
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60
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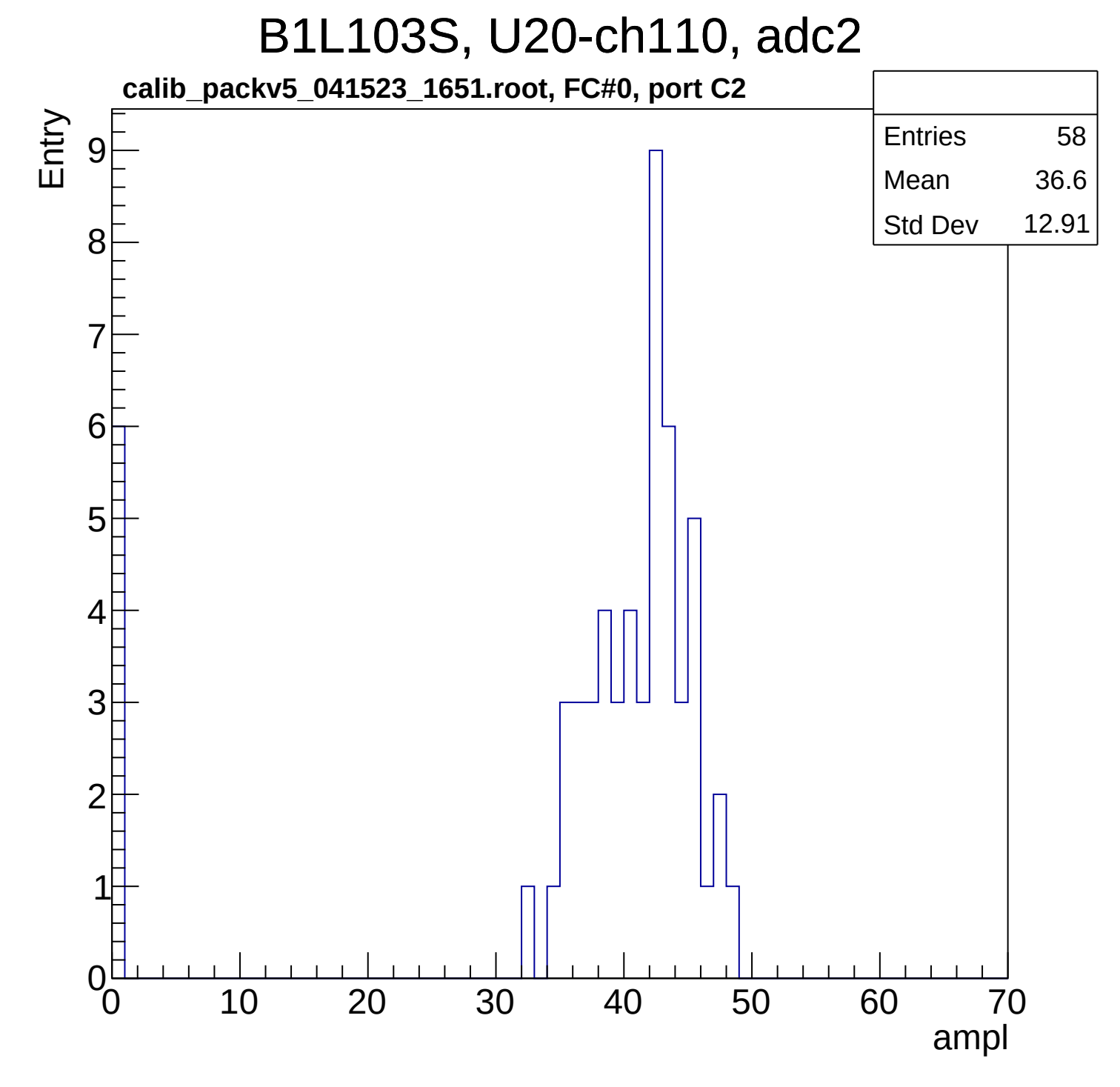
B1L103S, U20-ch110, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 36.6
Std Dev 12.91
Entry
ampl
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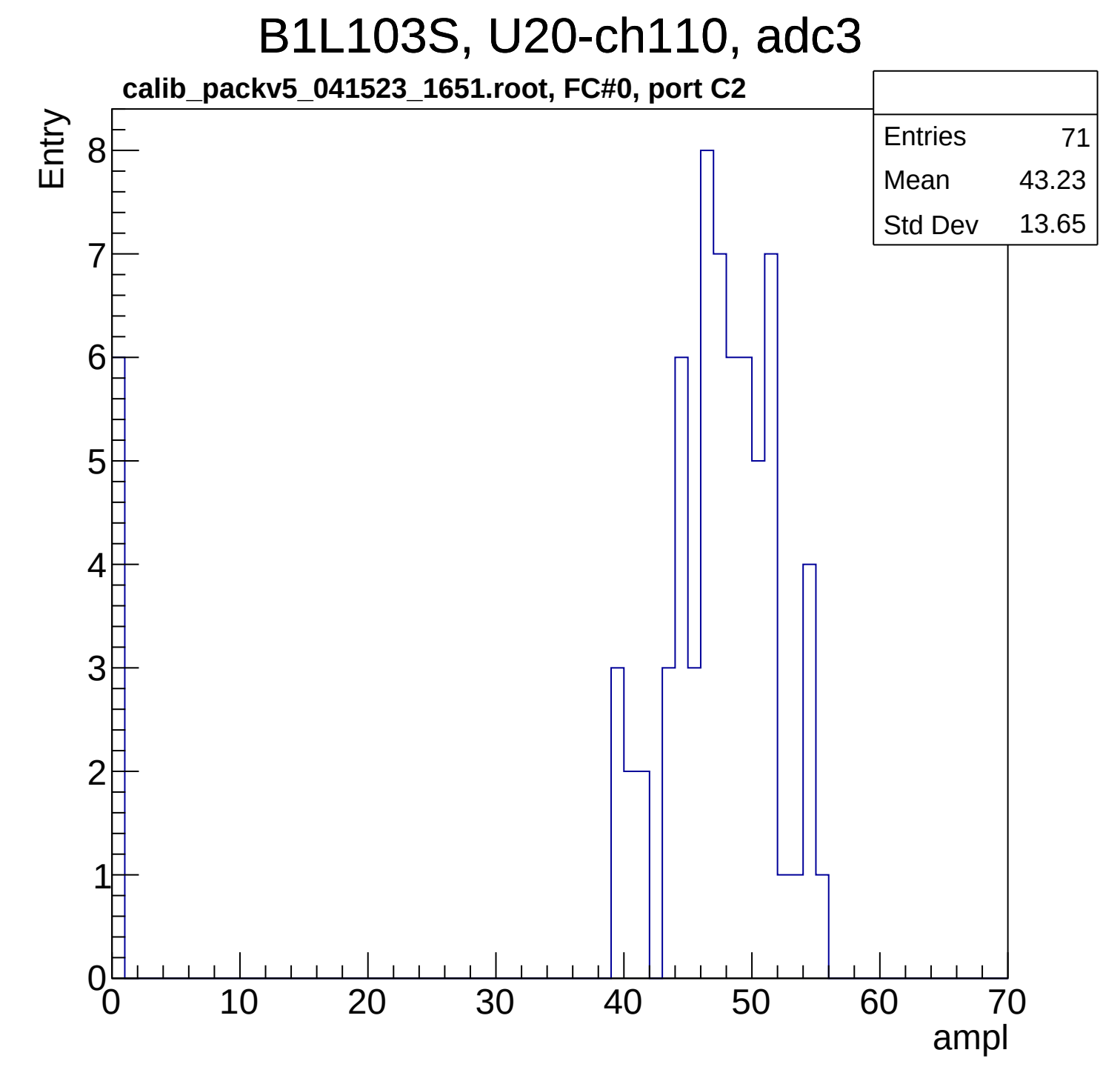
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch110, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 43.23
Std Dev 13.65
Entry
ampl
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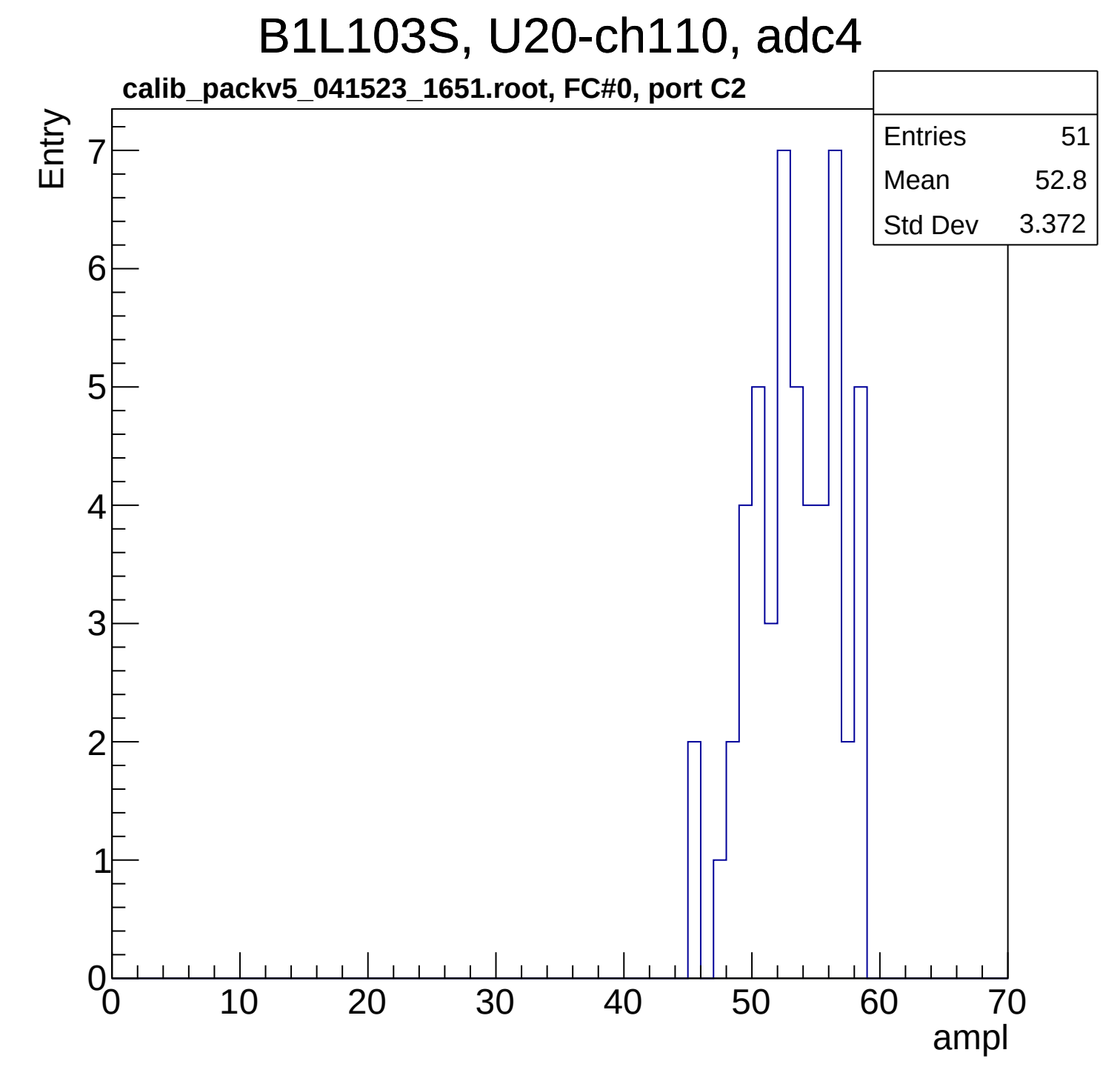
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch110, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 52.8
Std Dev 3.372
Entry
ampl
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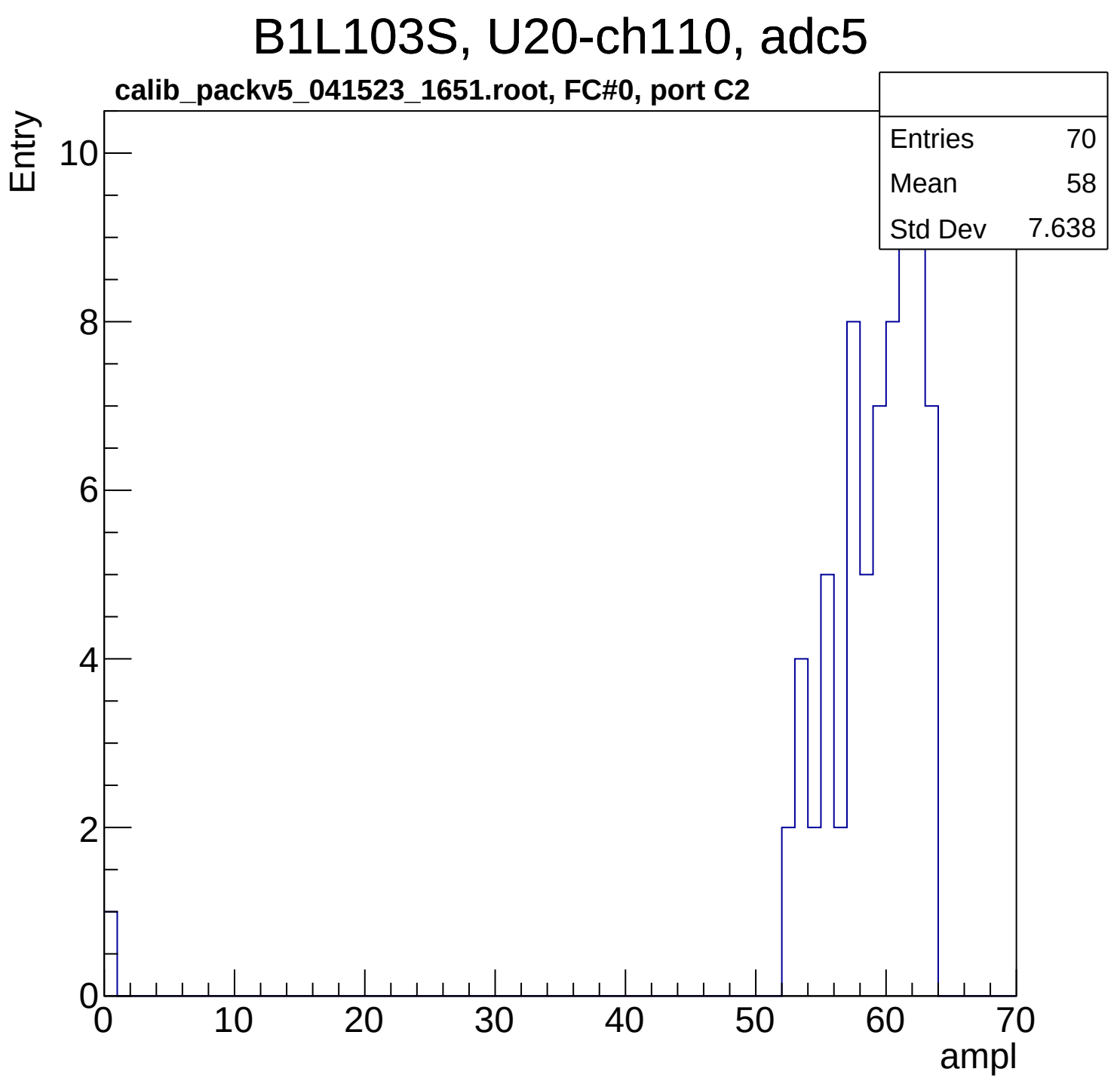
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U20-ch110, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 58
Std Dev 7.638
Entry
ampl
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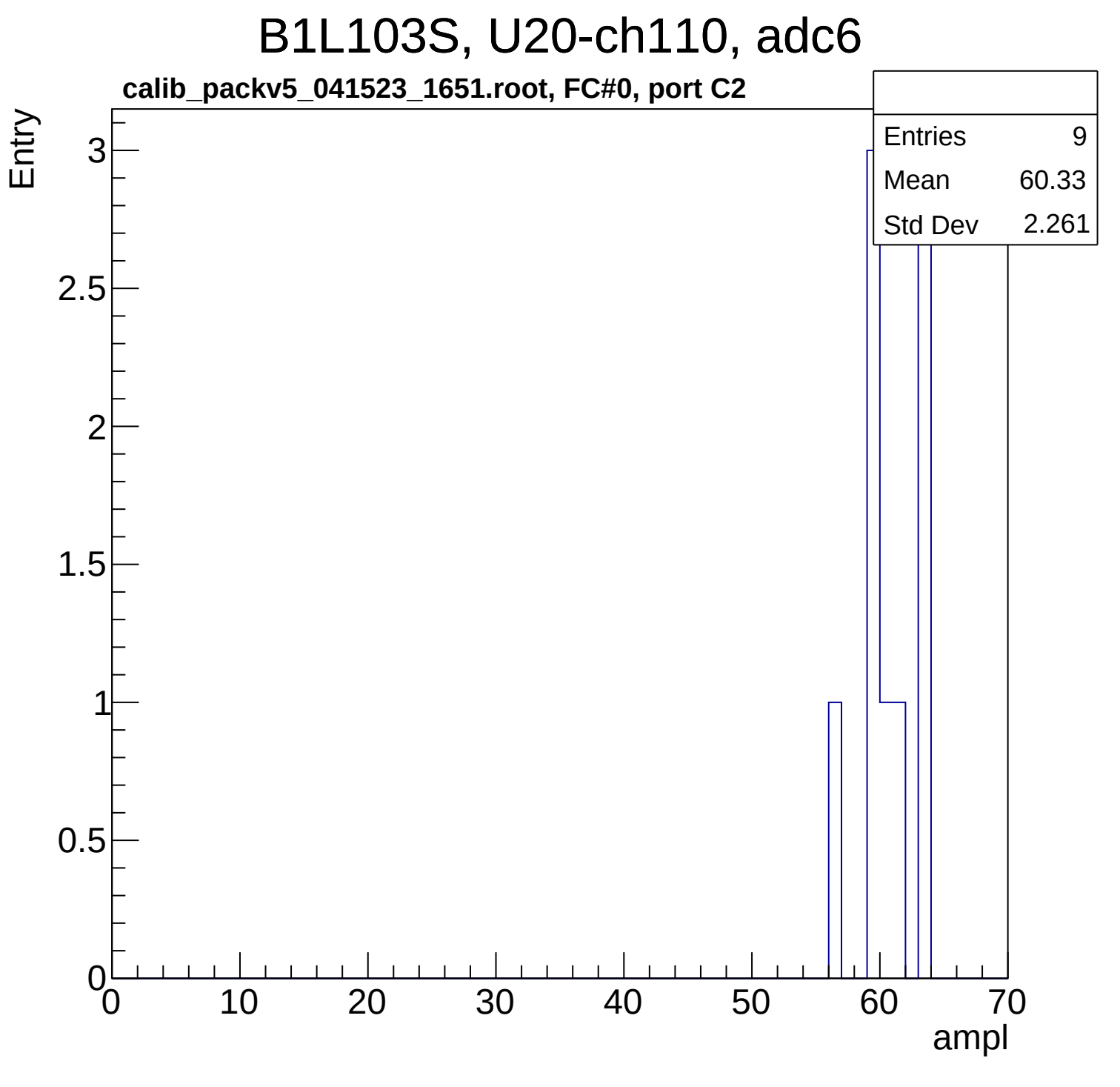
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U20-ch110, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 60.33
Std Dev 2.261
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
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20
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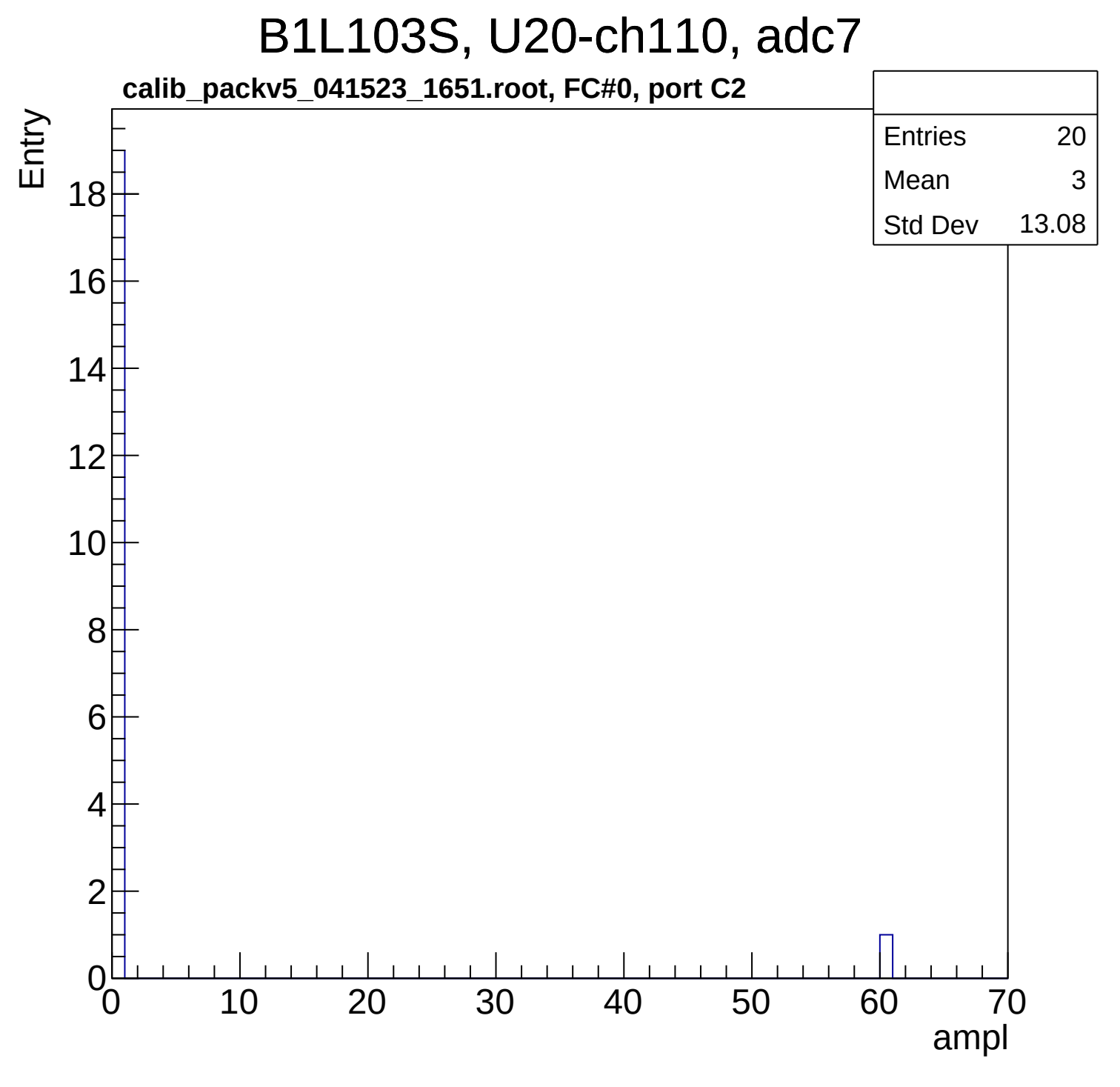
40
50
60
70


B1L103S, U20-ch110, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3
Std Dev 13.08
Entry
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6
8
10
12
14
16
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10
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30
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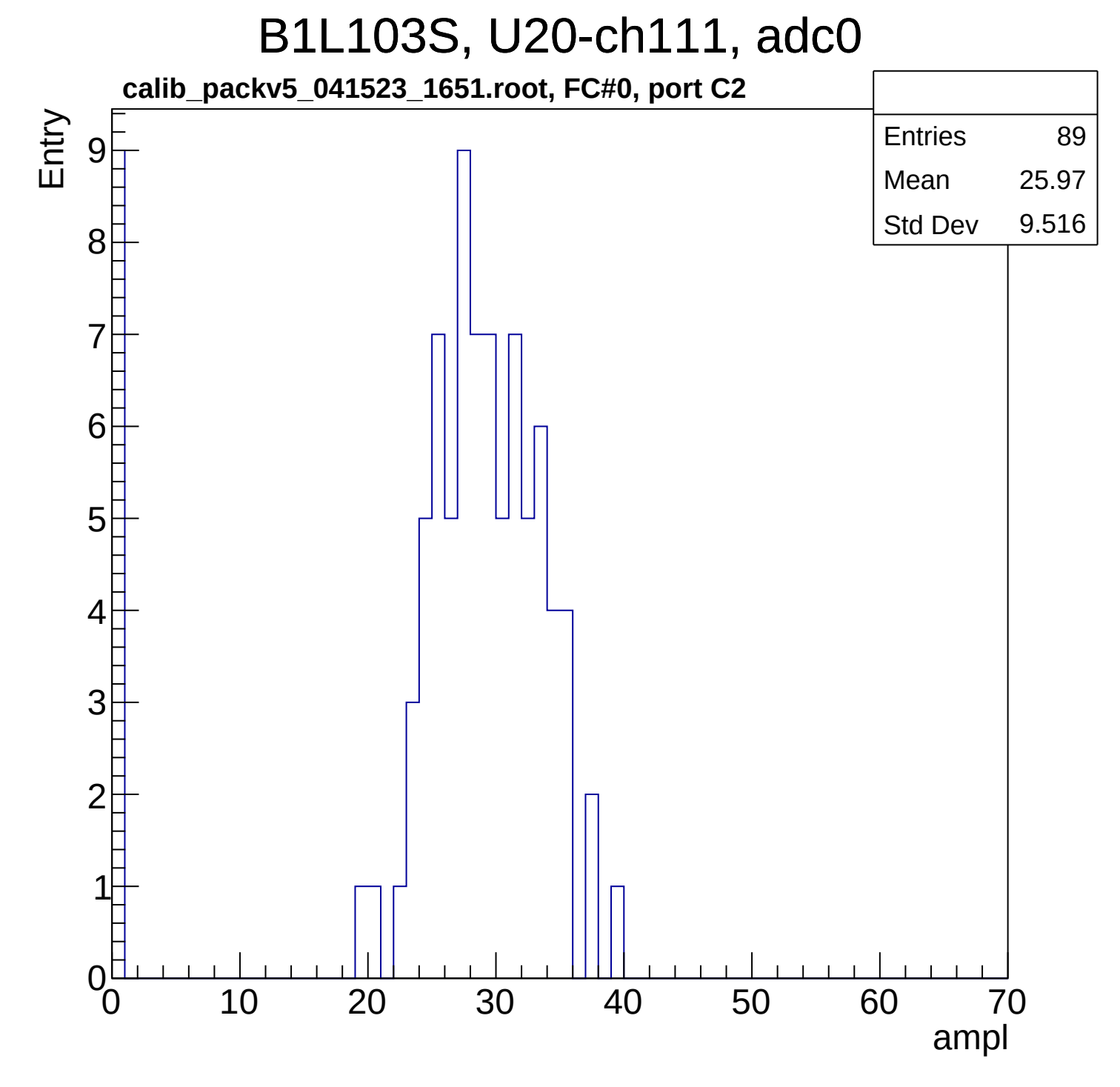
50
60
70
ampl


B1L103S, U20-ch111, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 25.97
Std Dev 9.516
Entry
ampl
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3
4
5
6
7
8
9
0
10
20
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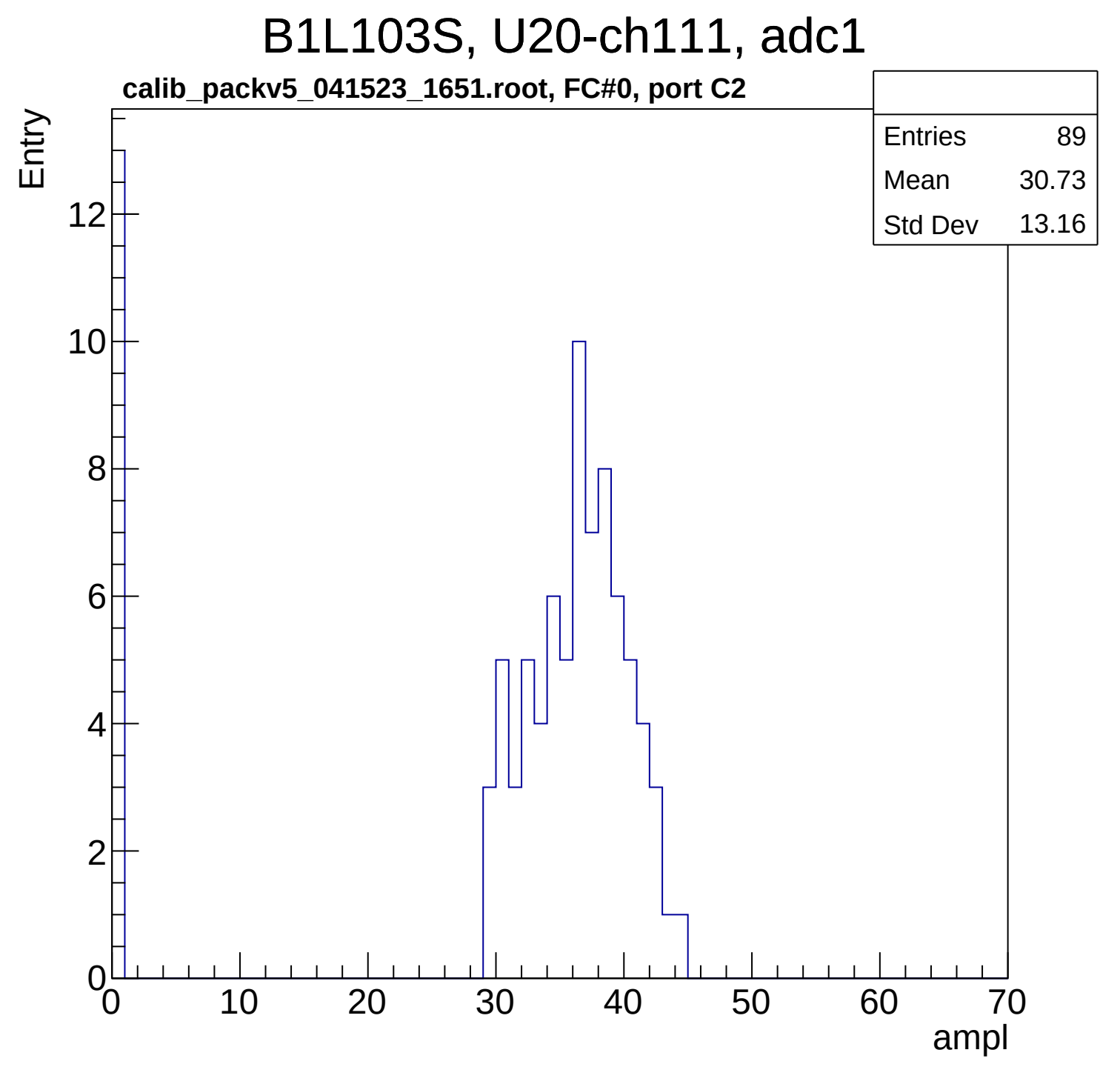
60
70


B1L103S, U20-ch111, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 30.73
Std Dev 13.16
Entry
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2
4
6
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10
12
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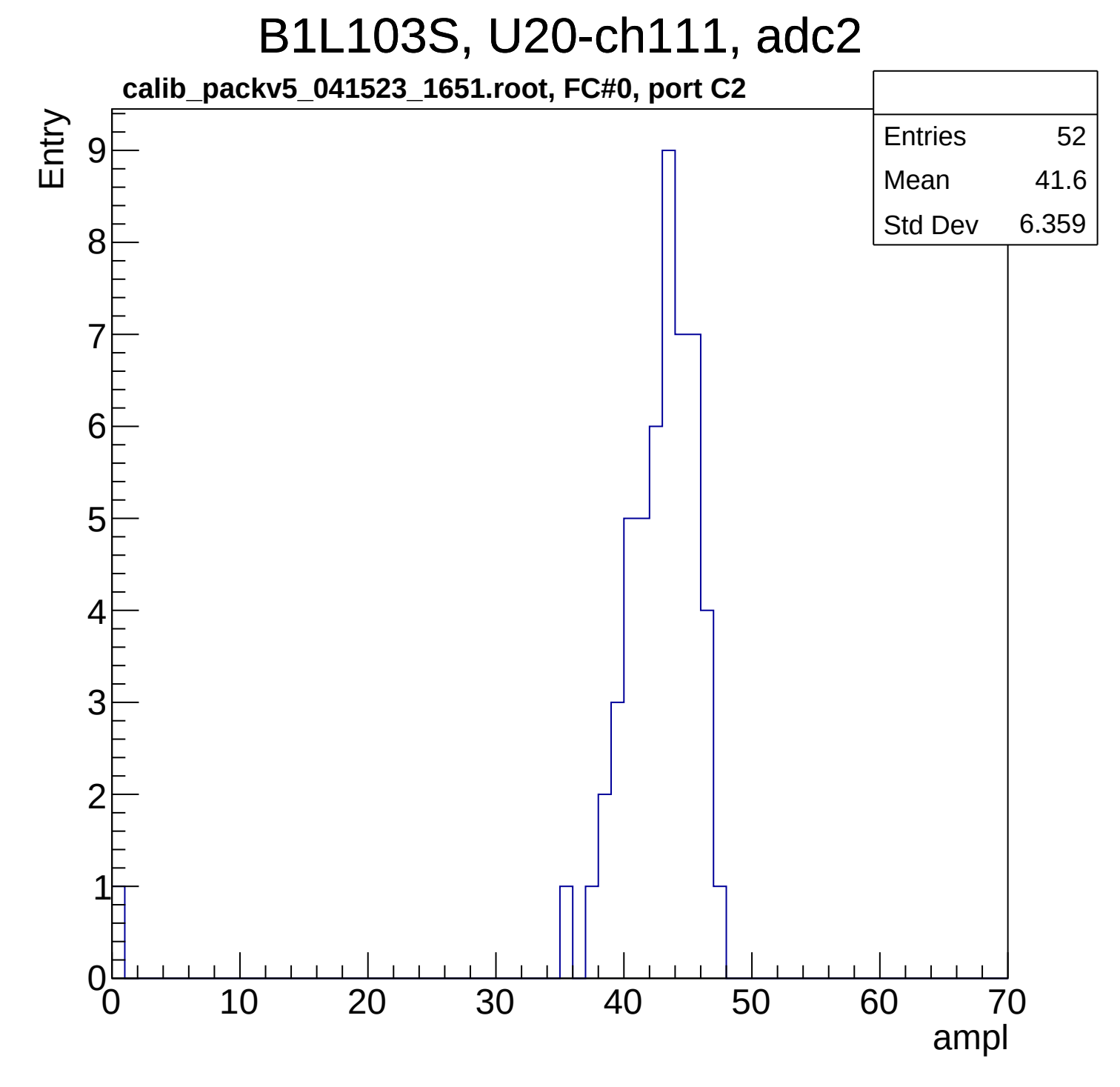
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch111, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 41.6
Std Dev 6.359
Entry
ampl
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3
4
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60
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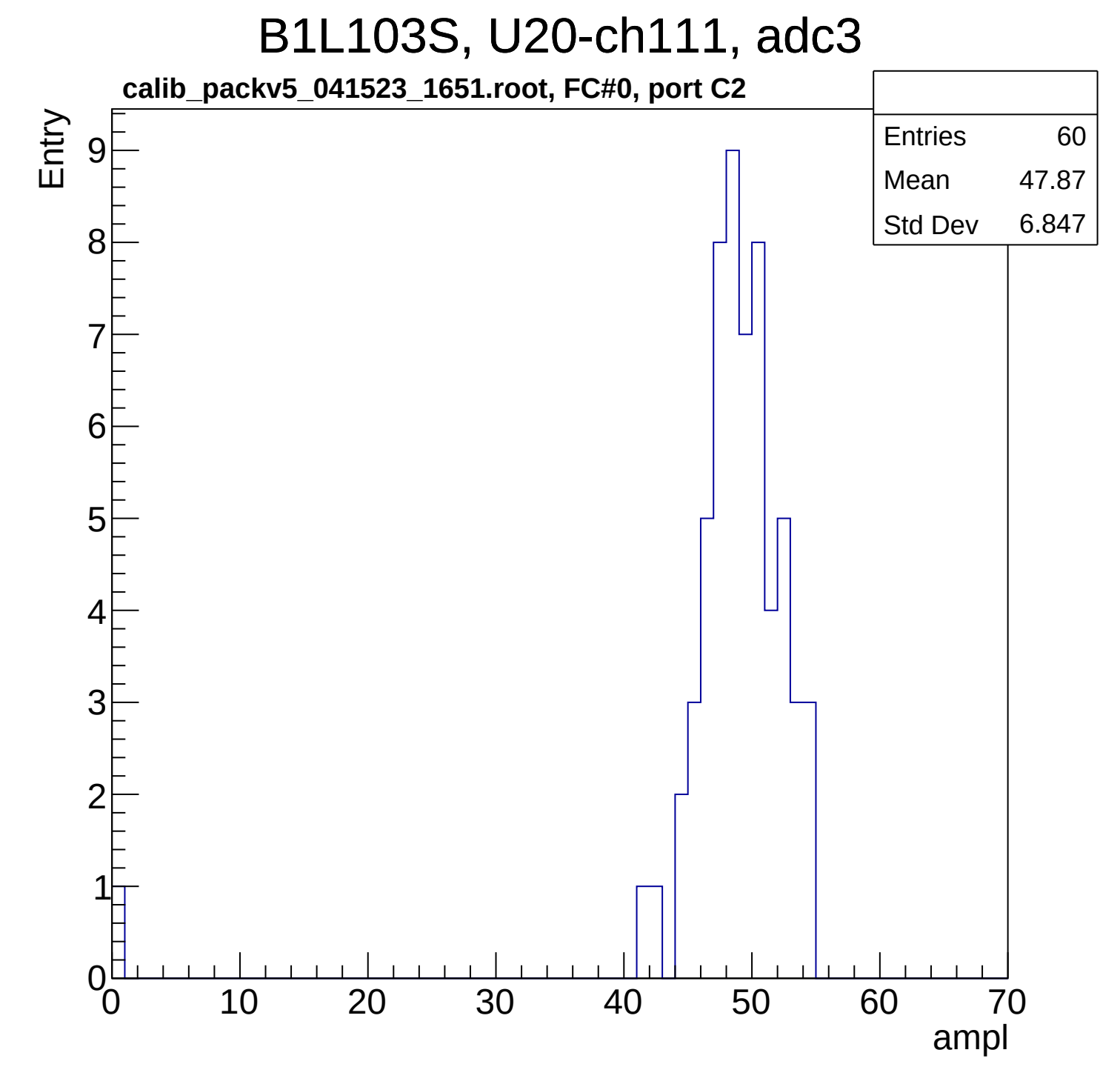
B1L103S, U20-ch111, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 47.87
Std Dev 6.847
Entry
ampl
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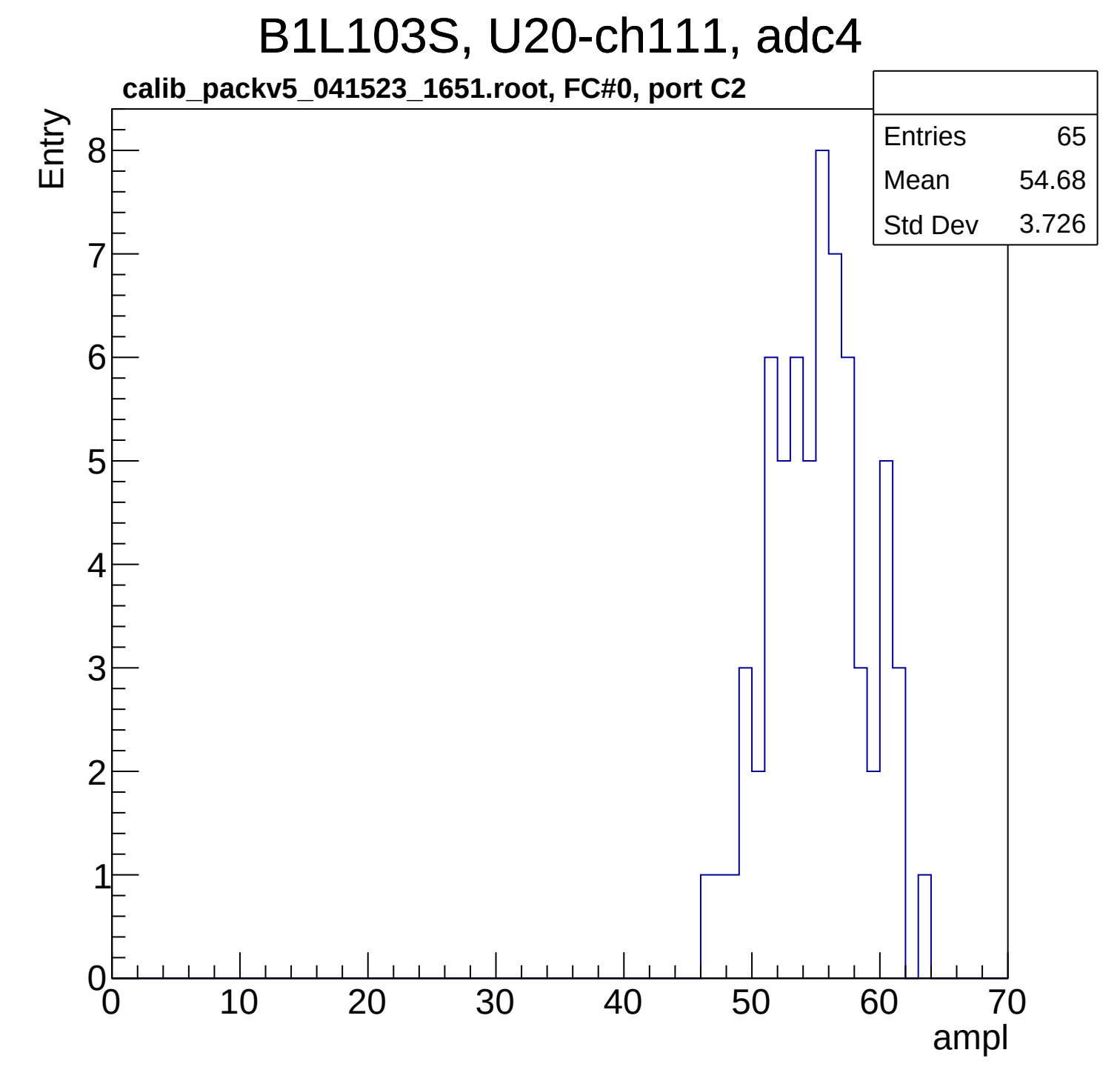
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch111, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 54.68
Std Dev 3.726
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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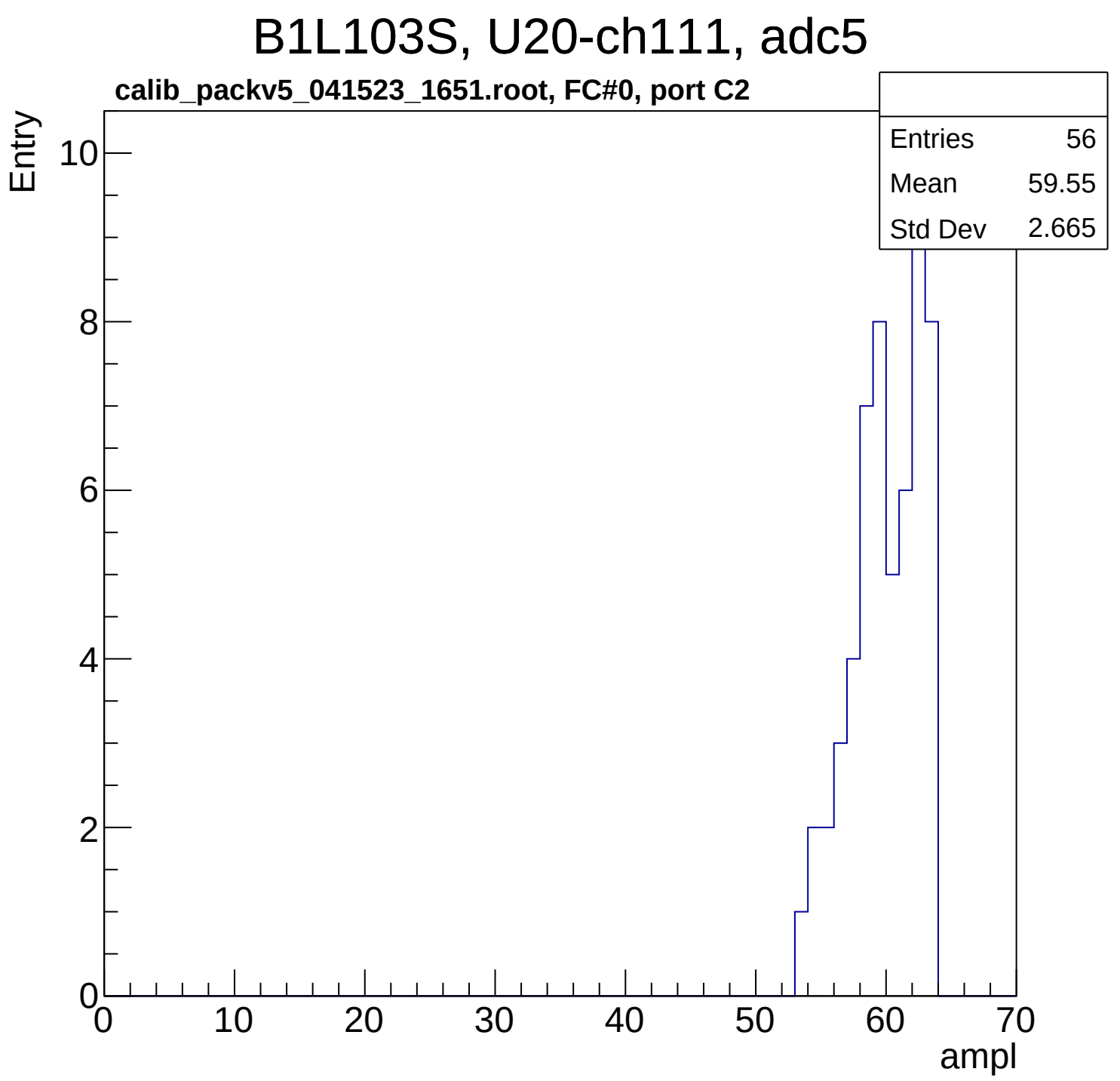
B1L103S, U20-ch111, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 59.55
Std Dev 2.665
Entry
ampl
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2
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0
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40
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60
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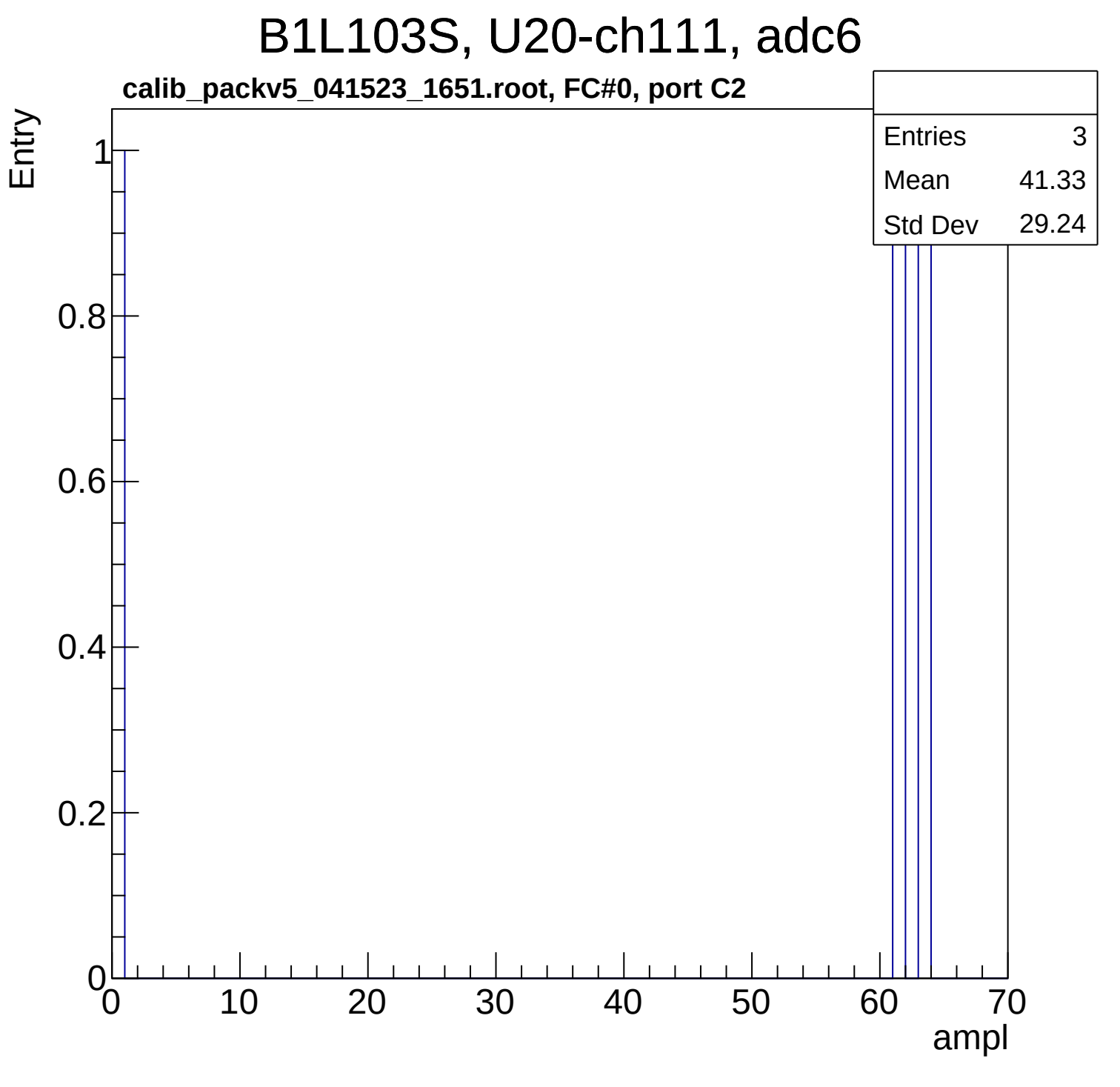
B1L103S, U20-ch111, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 41.33
Std Dev 29.24
Entry
ampl
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0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
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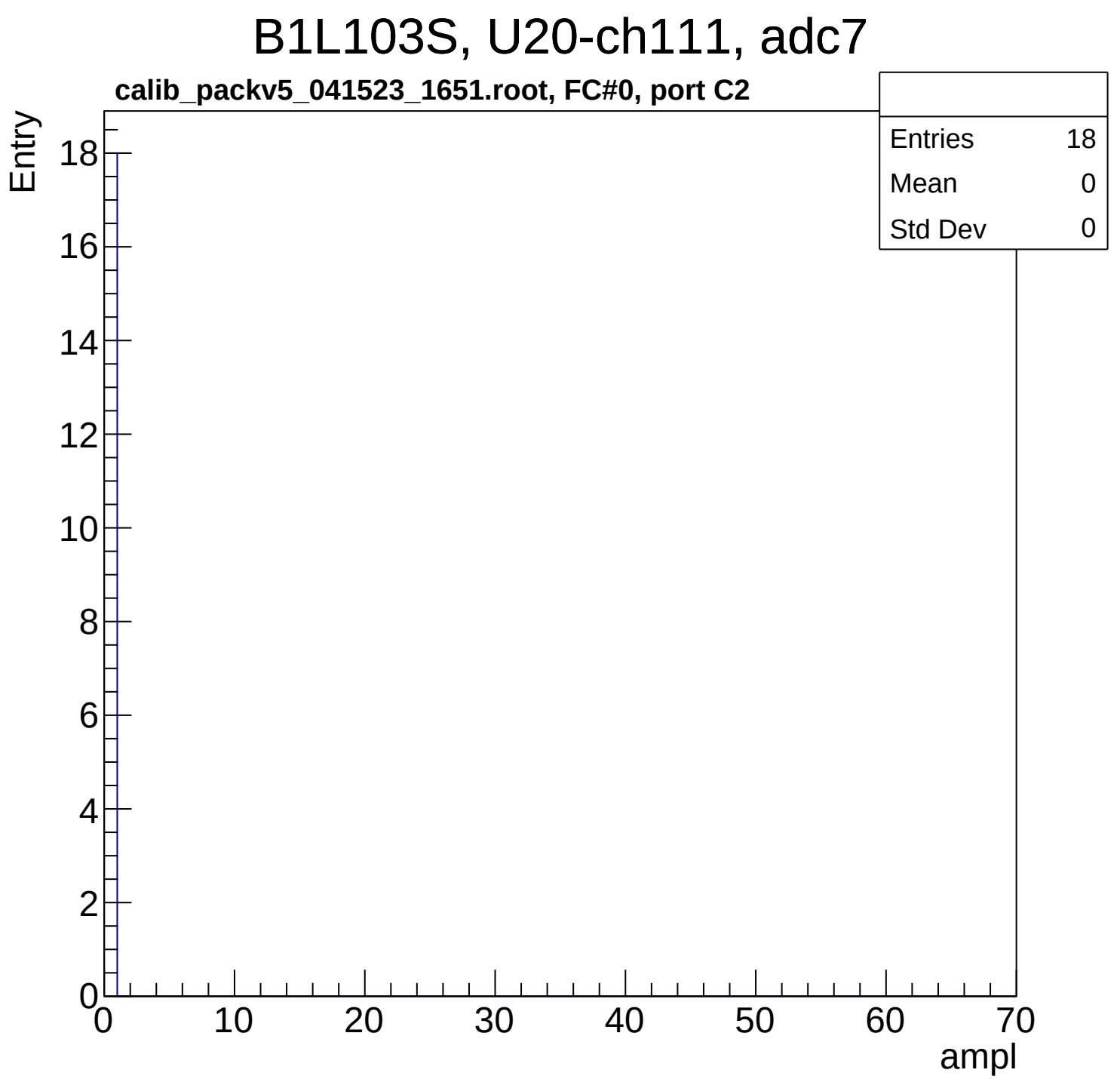
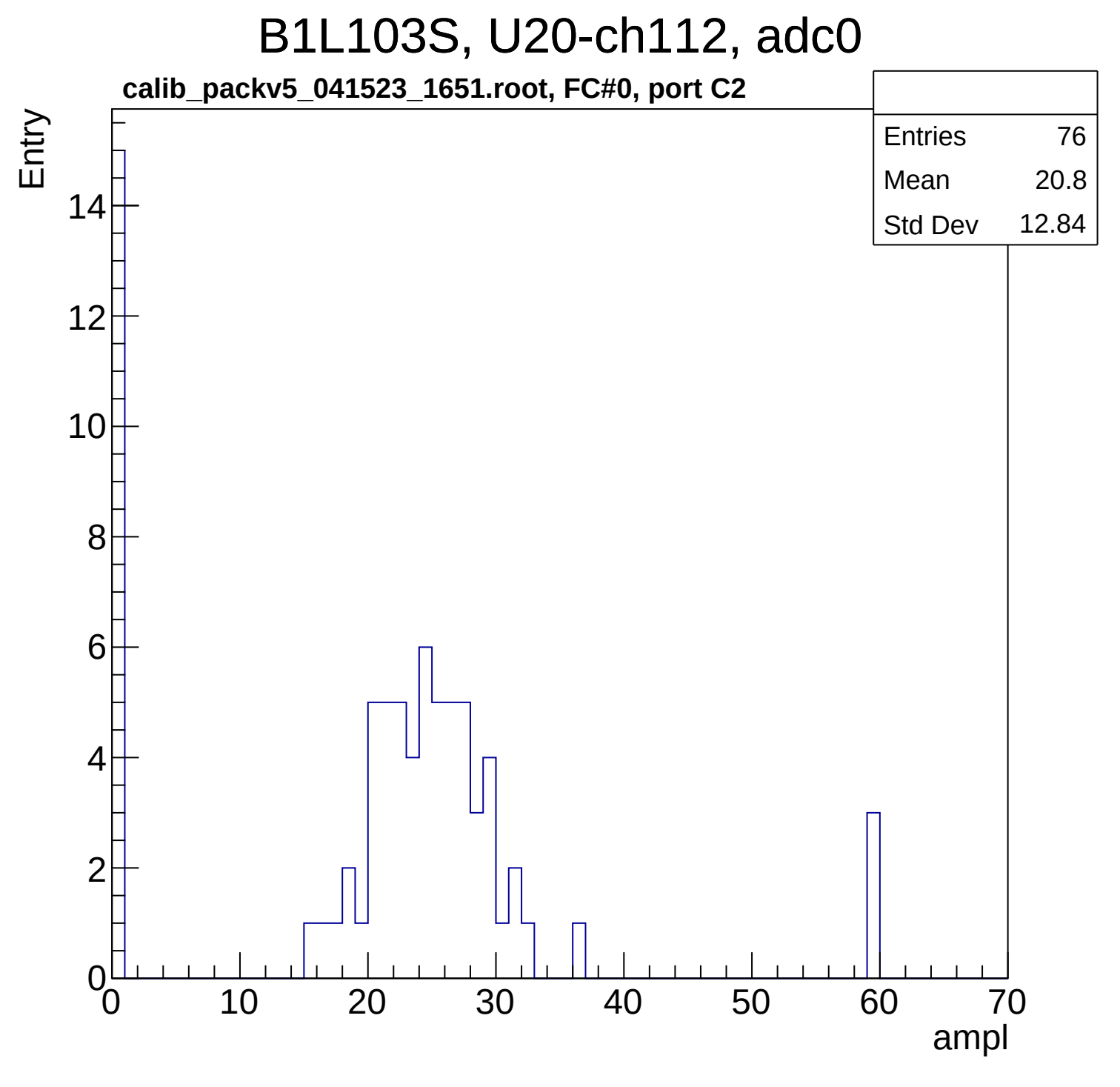

B1L103S, U20-ch111, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch112, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 20.8
Std Dev 12.84
Entry
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6
8
10
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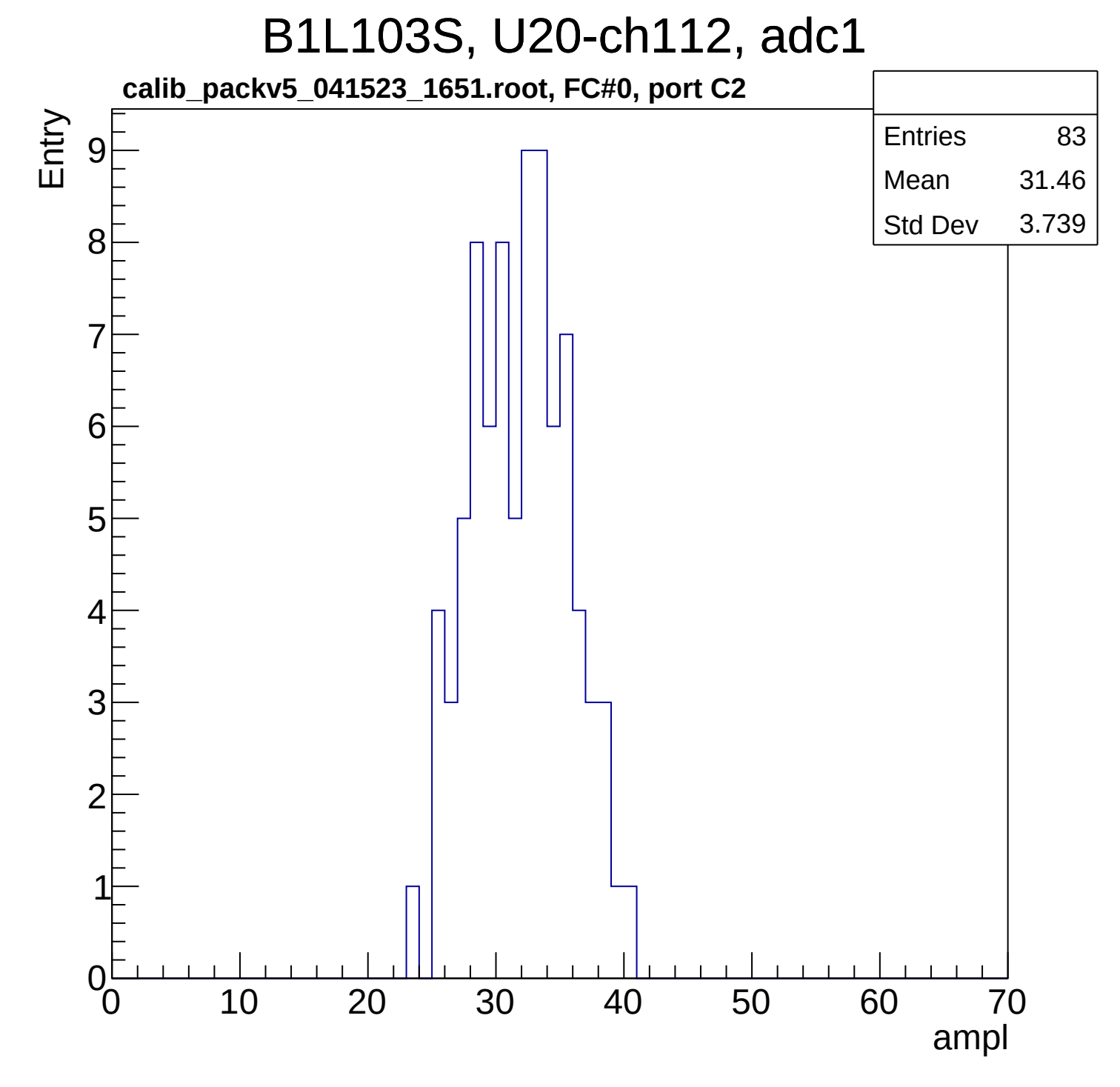
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch112, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 31.46
Std Dev 3.739
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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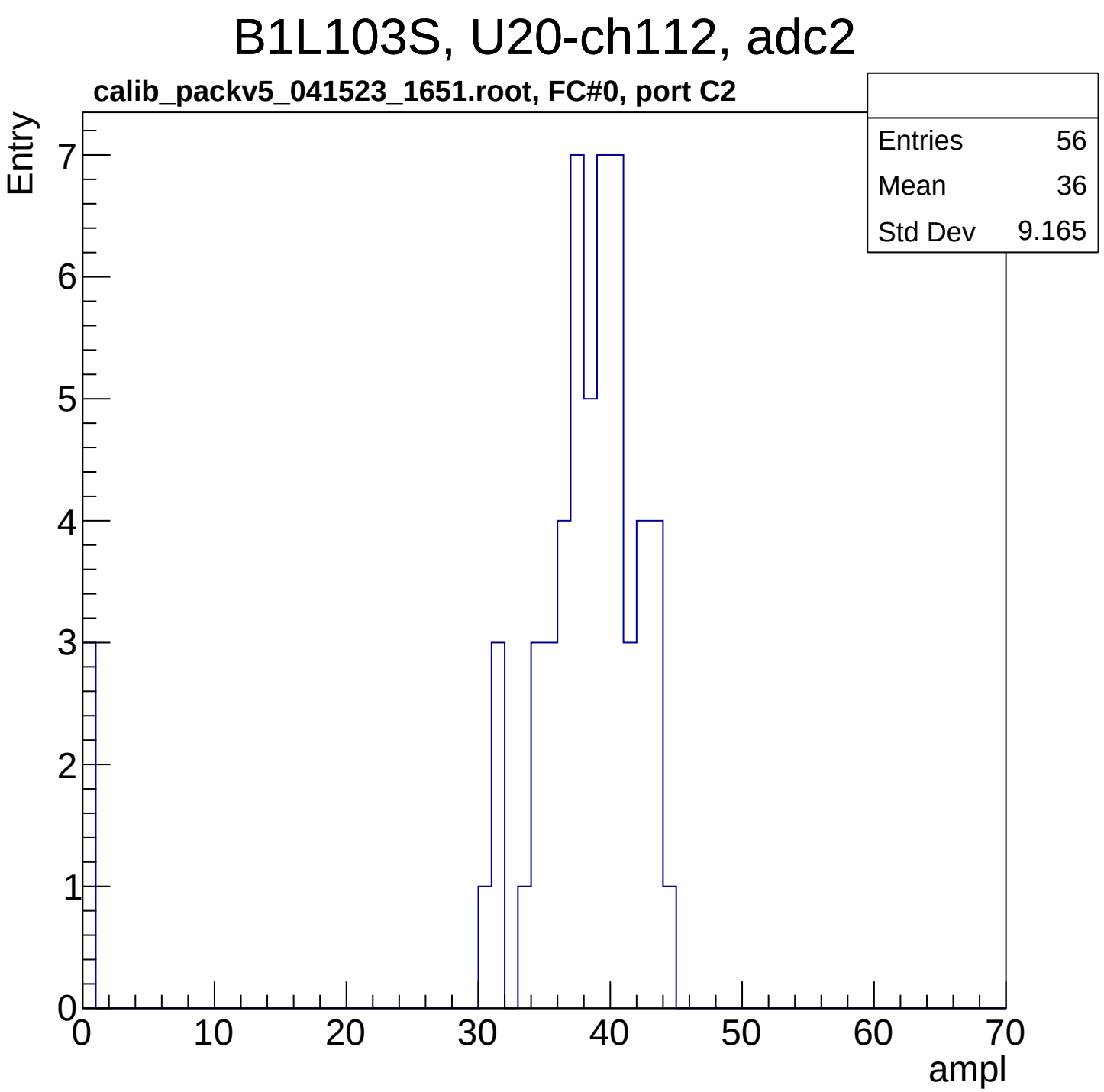
B1L103S, U20-ch112, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 36
Std Dev 9.165
Entry
ampl
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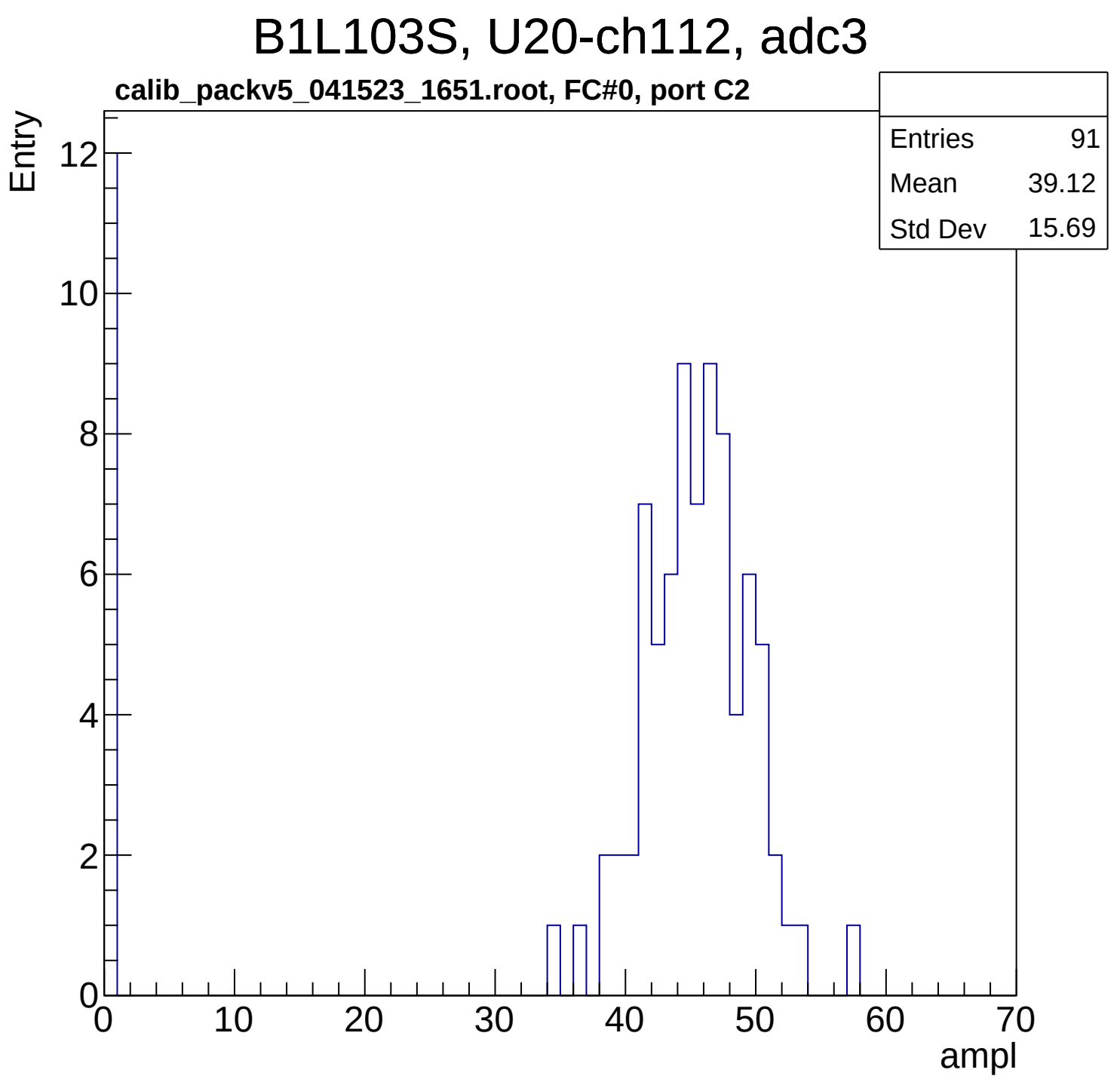
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U20-ch112, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 39.12
Std Dev 15.69
Entry
ampl
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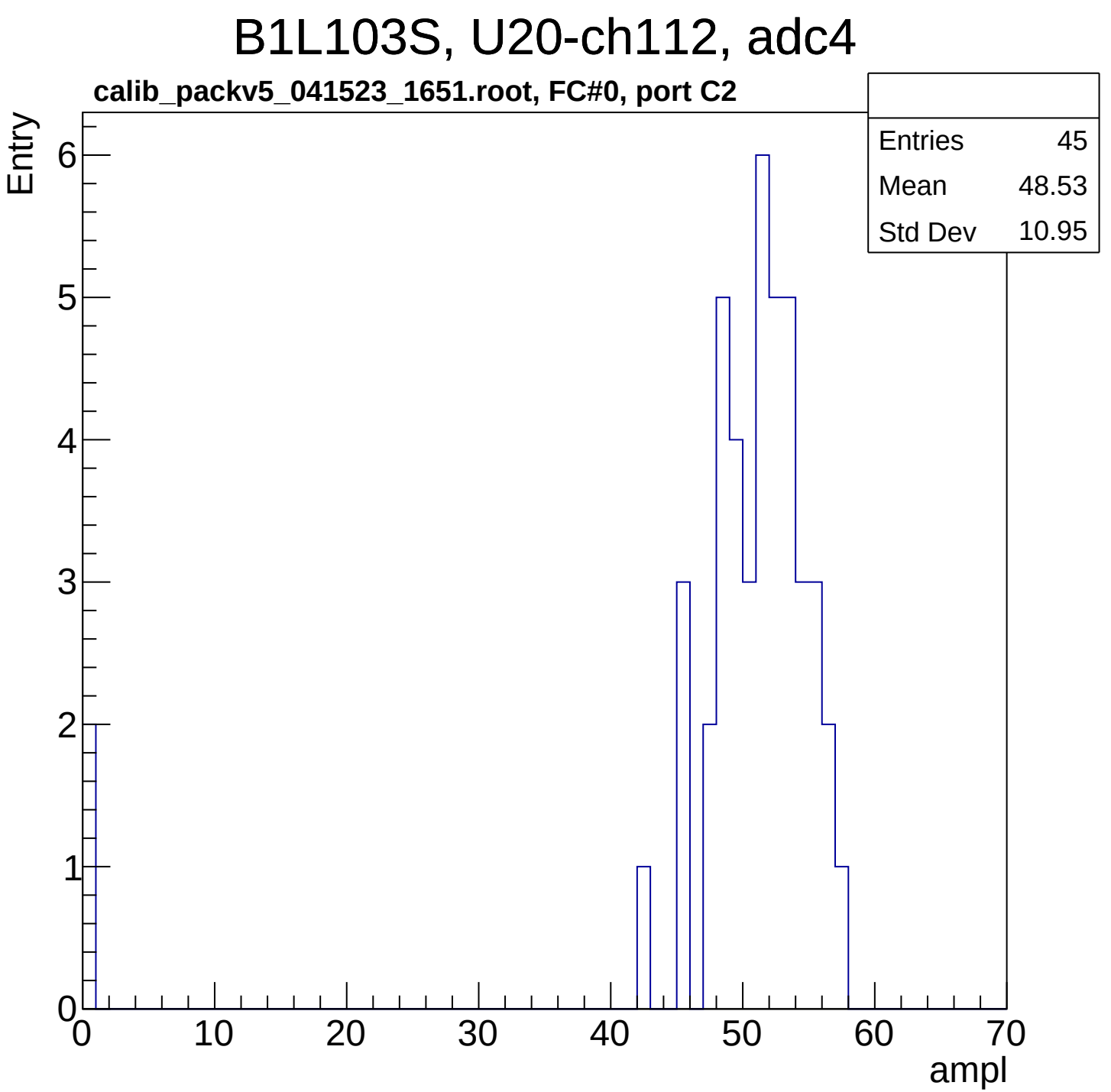
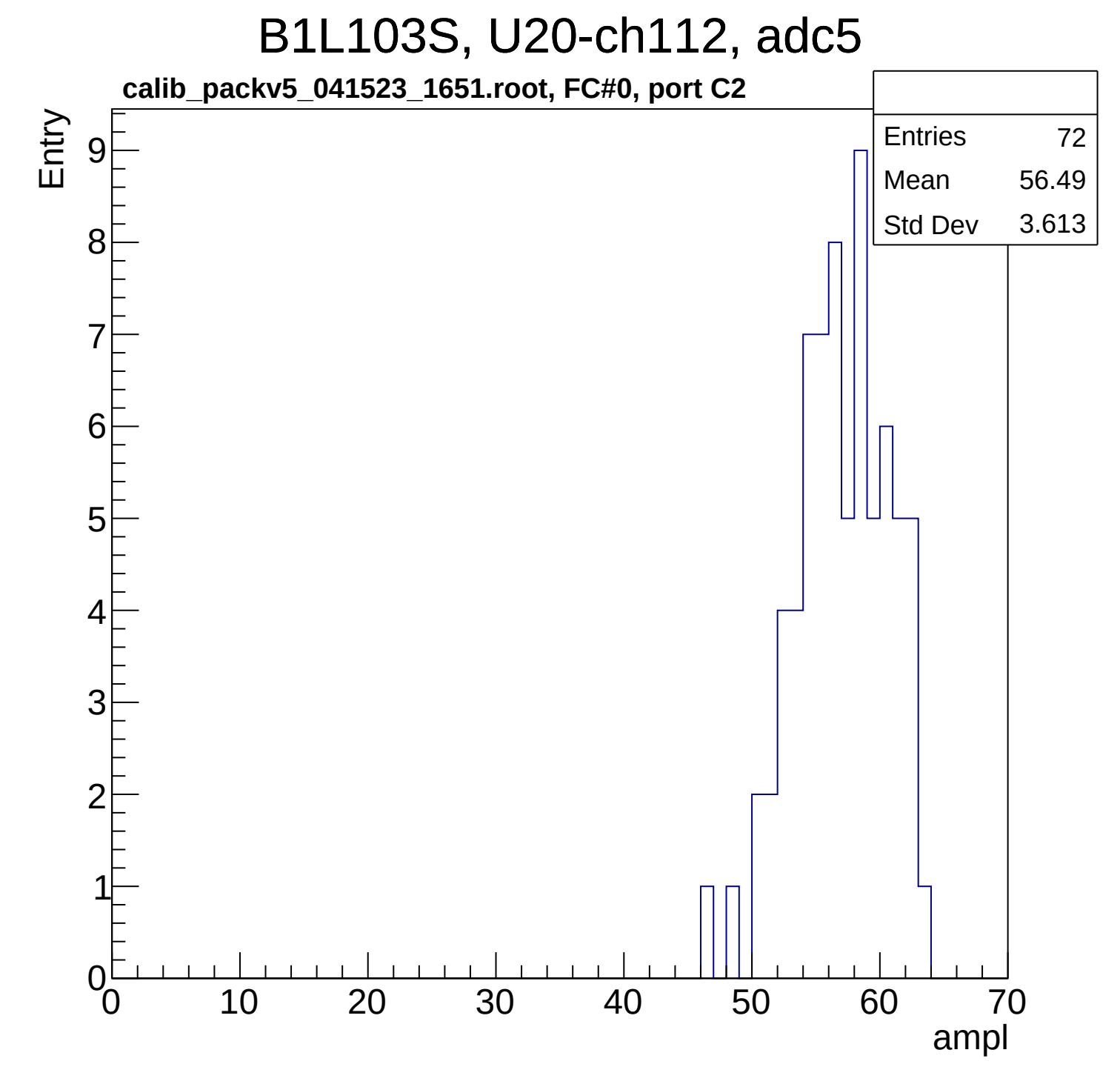
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U20-ch112, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 48.53
Std Dev 10.95
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch112, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 56.49
Std Dev 3.613
Entry
ampl
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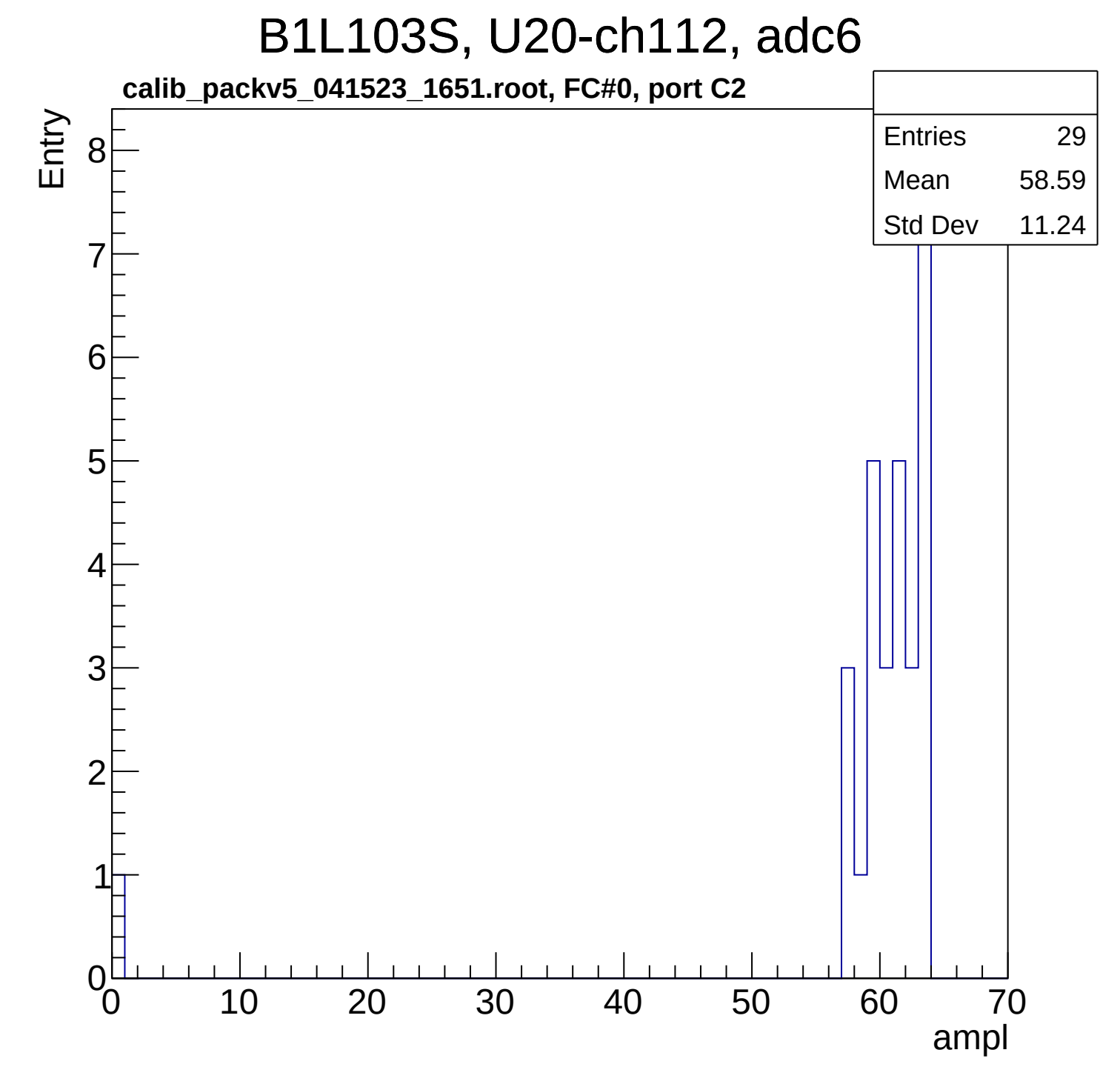
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch112, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 58.59
Std Dev 11.24
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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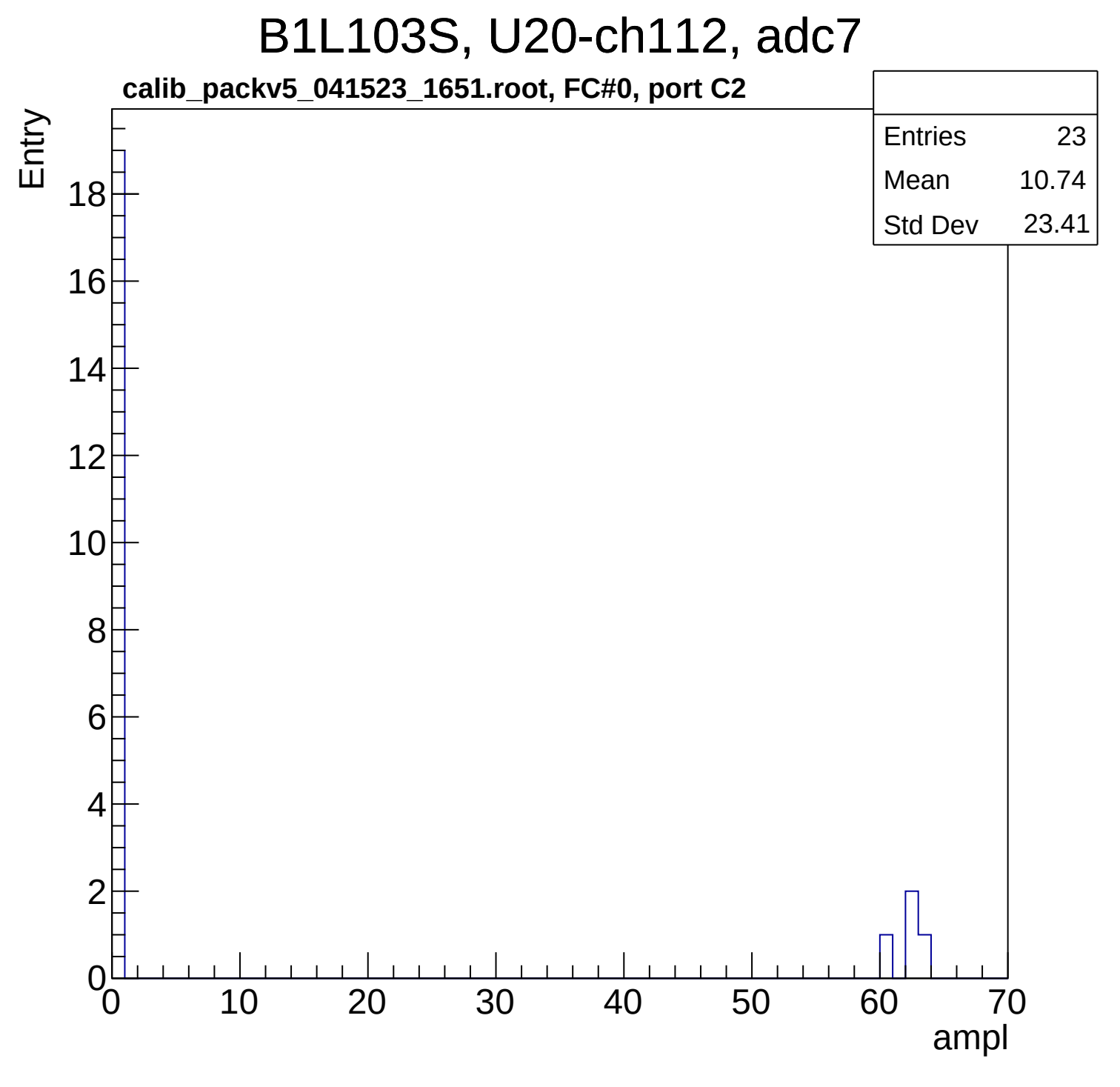
B1L103S, U20-ch112, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 10.74
Std Dev 23.41
Entry
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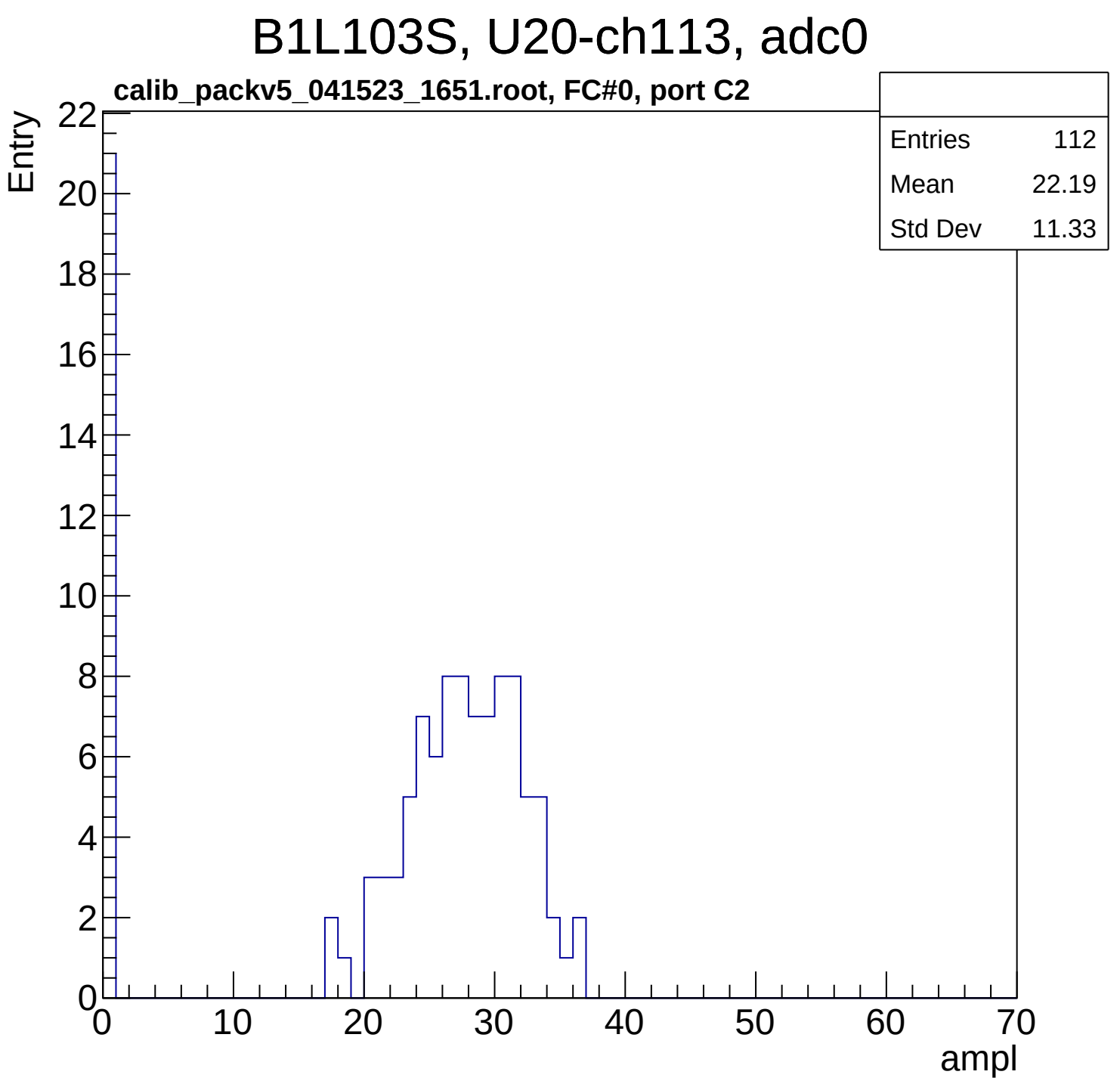
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch113, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 112
Mean 22.19
Std Dev 11.33
Entry
ampl
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6
8
10
12
14
16
18
20
22
0
10
20
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40
50
60
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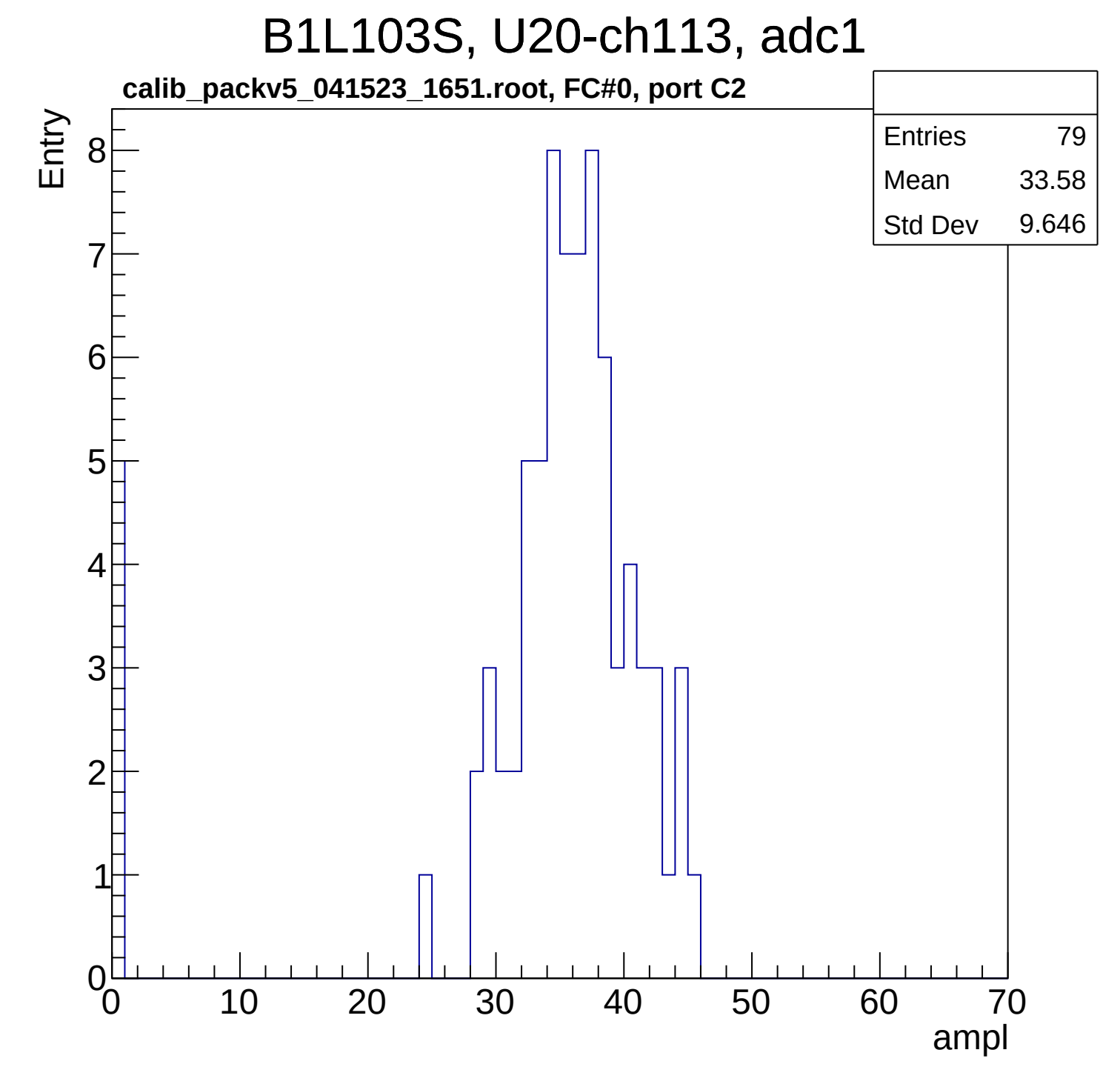
B1L103S, U20-ch113, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 33.58
Std Dev 9.646
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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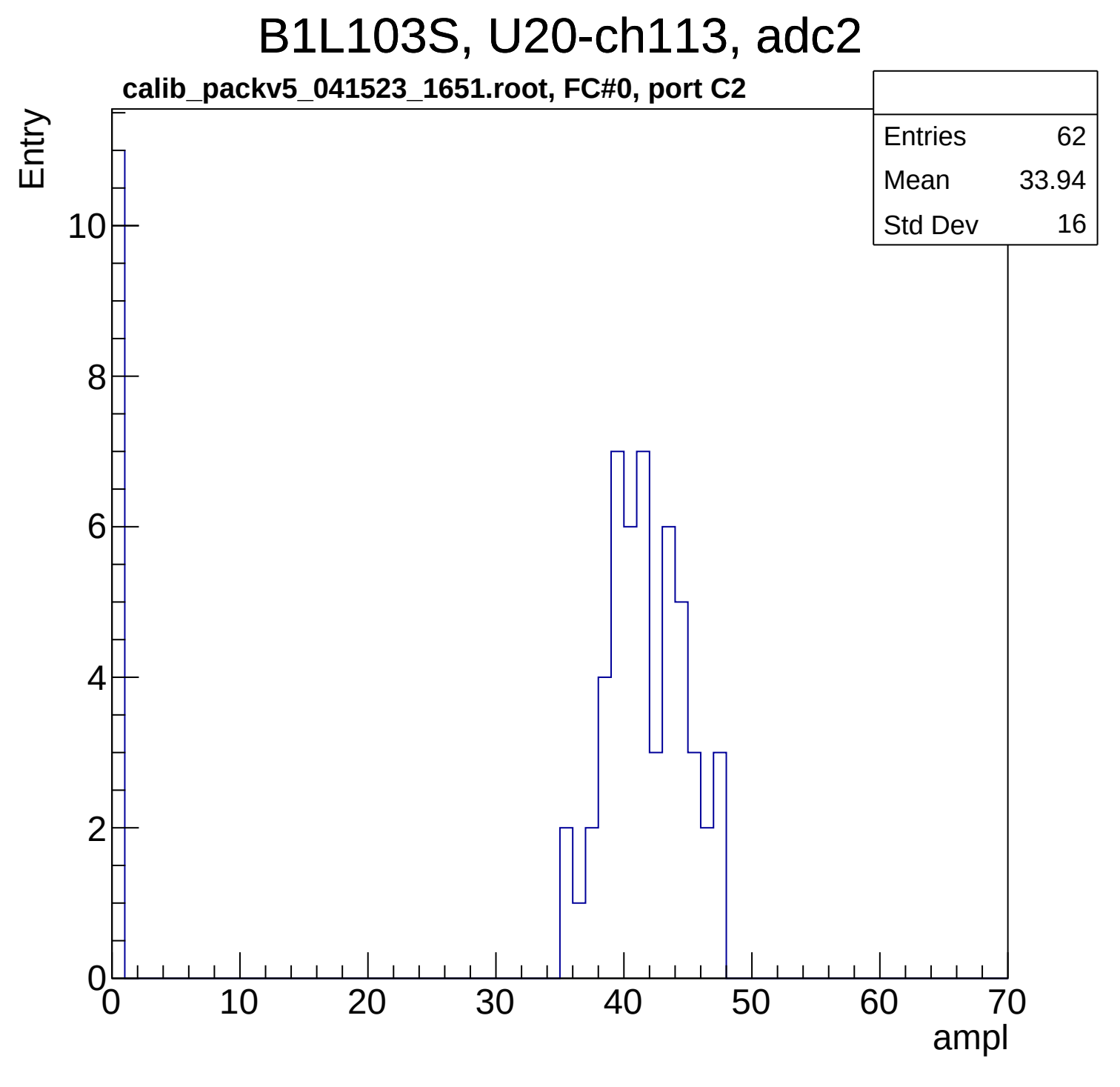
40
50
60
70


B1L103S, U20-ch113, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 33.94
Std Dev 16
Entry
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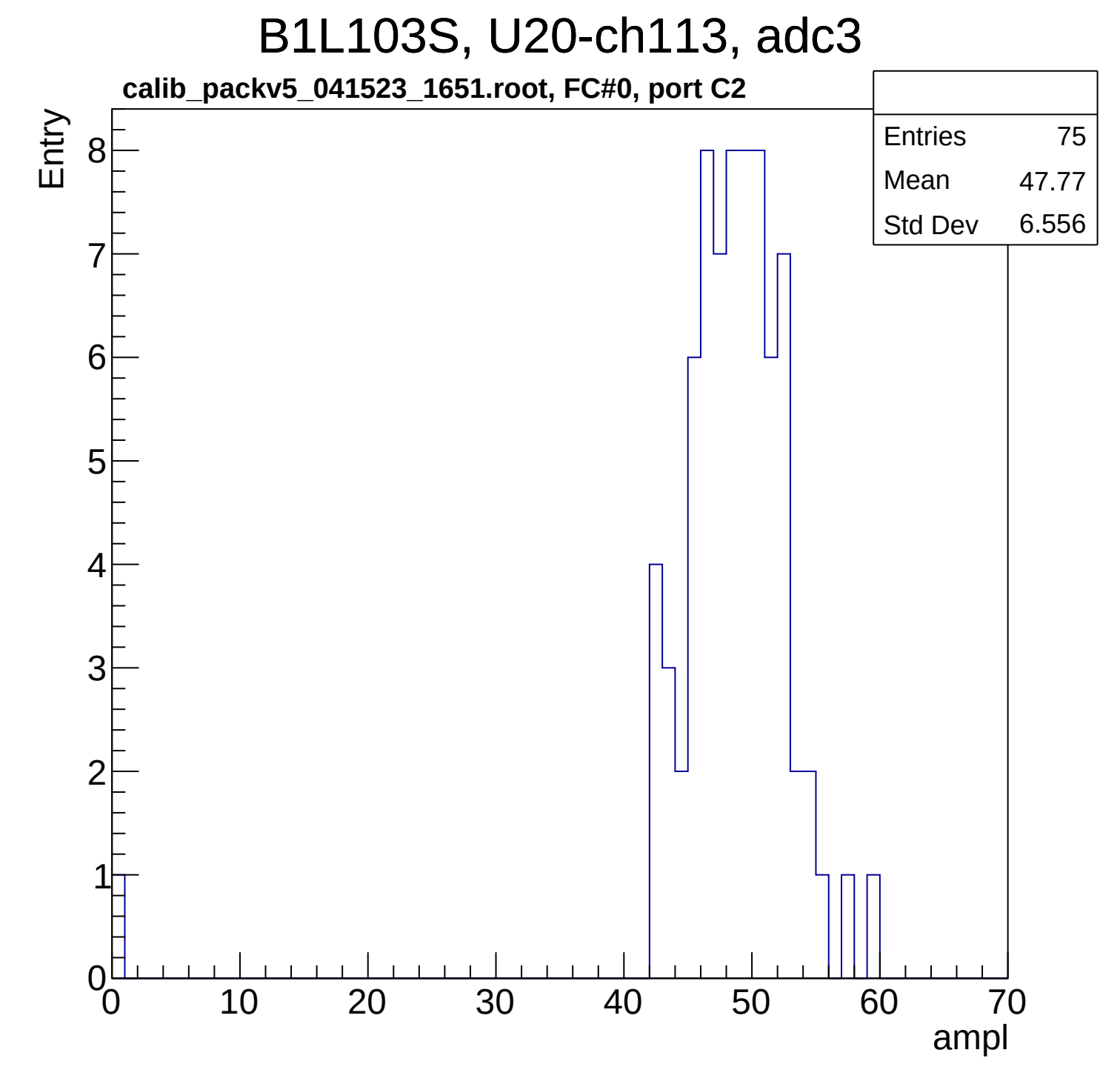
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch113, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 47.77
Std Dev 6.556
Entry
ampl
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2
3
4
5
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0
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40
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60
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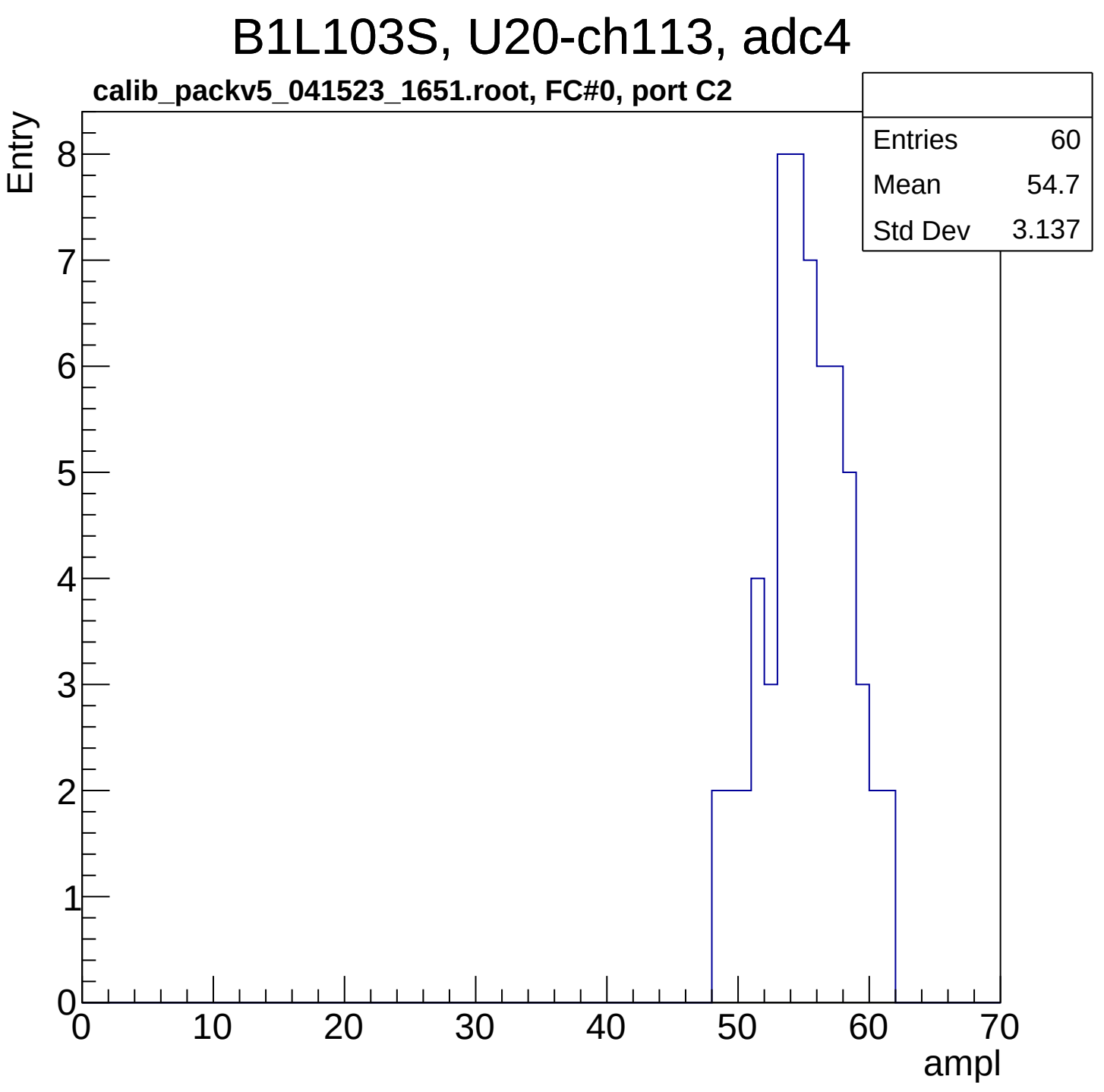
B1L103S, U20-ch113, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 54.7
Std Dev 3.137
Entry
ampl
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1
2
3
4
5
6
7
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0
10
20
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40
50
60
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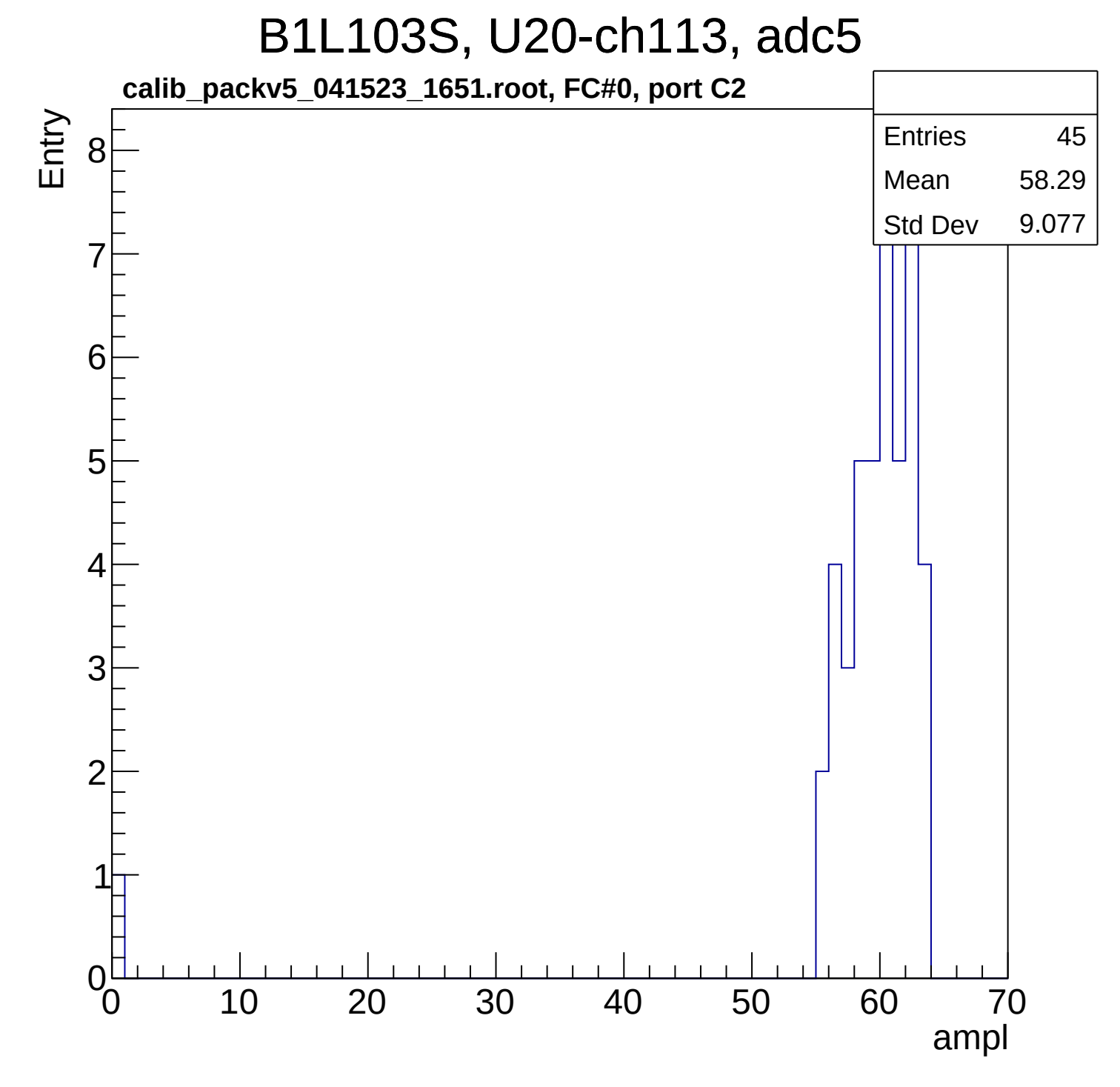
B1L103S, U20-ch113, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 58.29
Std Dev 9.077
Entry
ampl
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5
6
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0
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60
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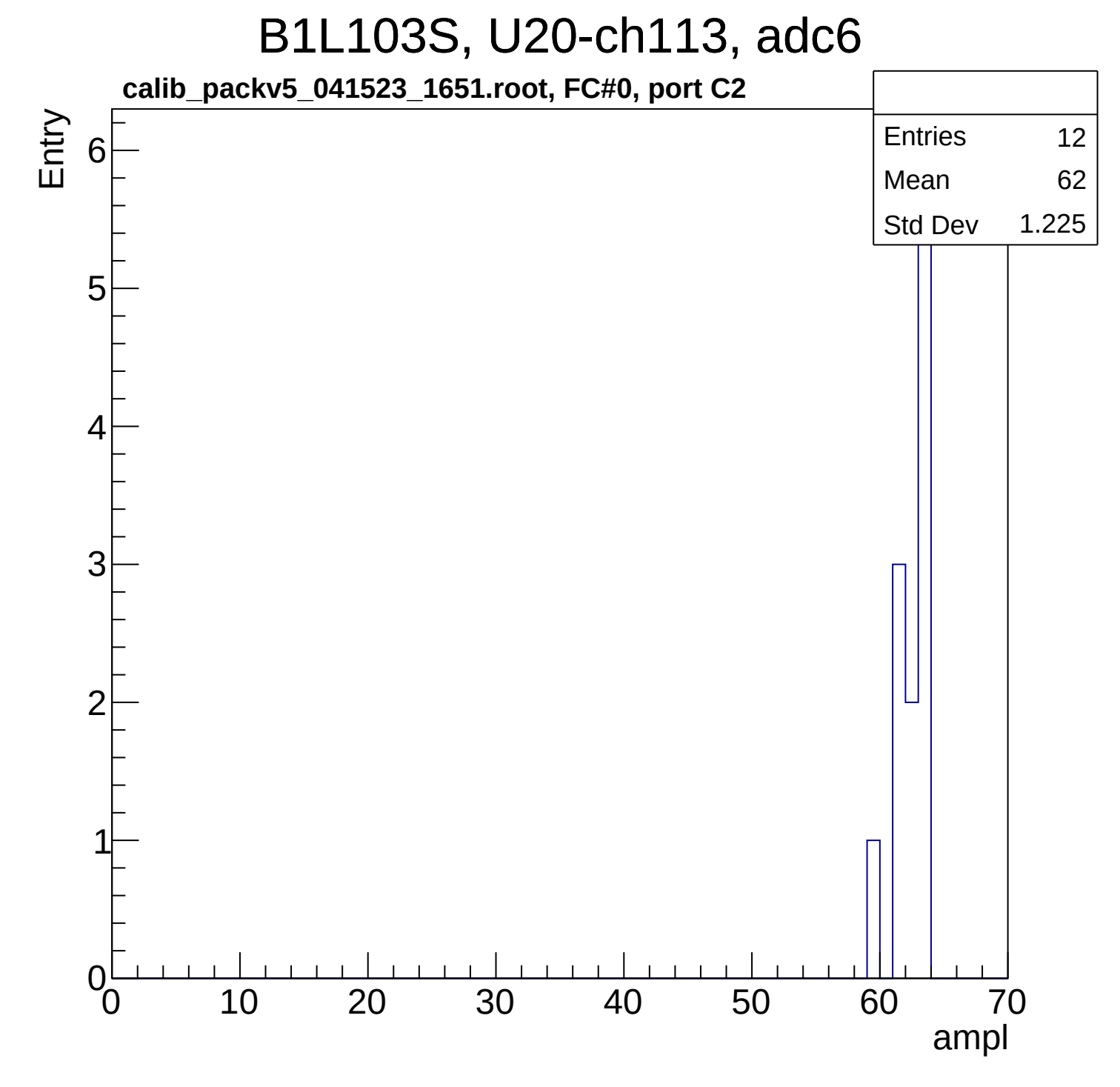
B1L103S, U20-ch113, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 62
Std Dev 1.225
Entry
ampl
0
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0
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20
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40
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60
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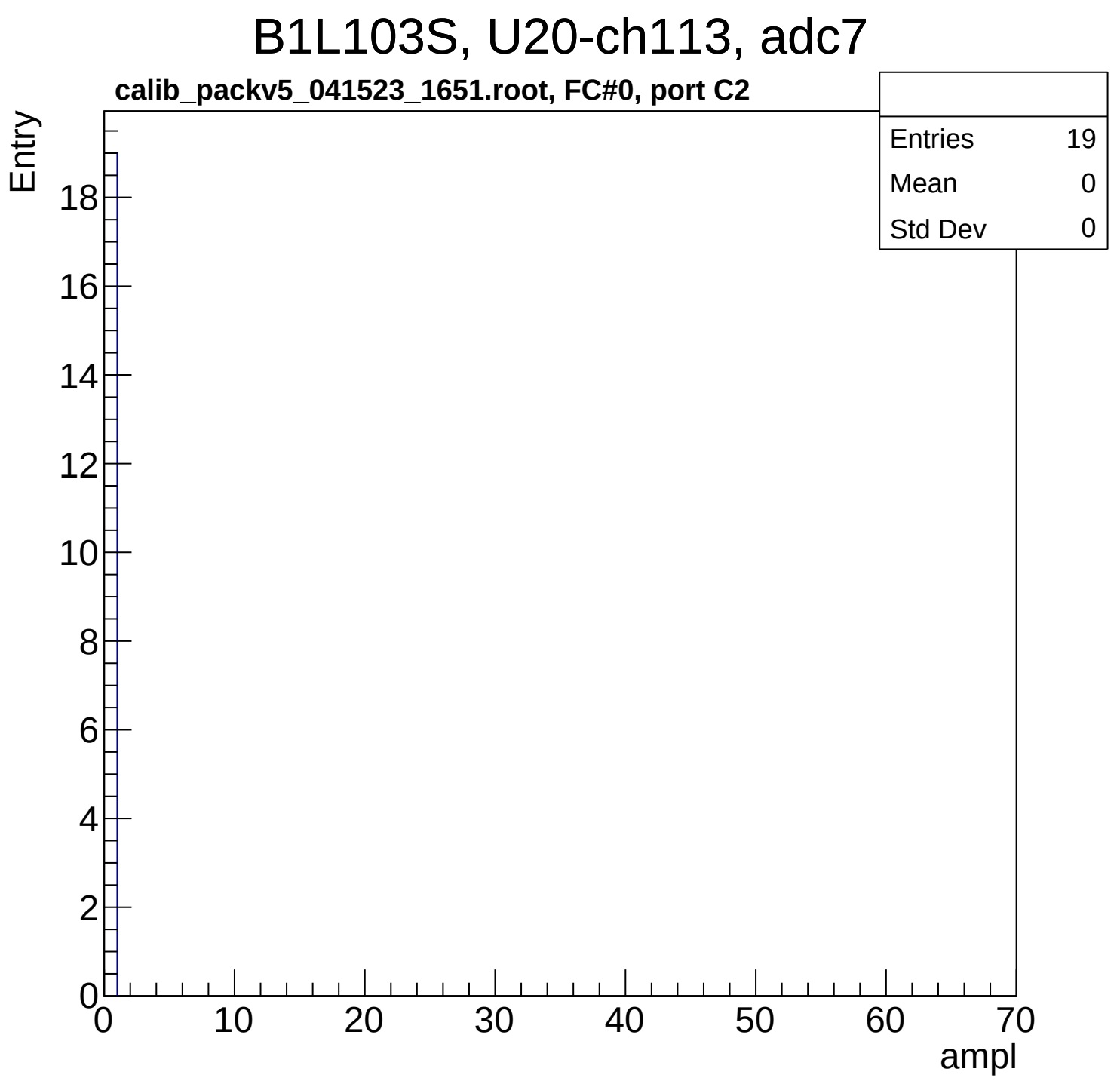
B1L103S, U20-ch113, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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6
8
10
12
14
16
18
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10
20
30
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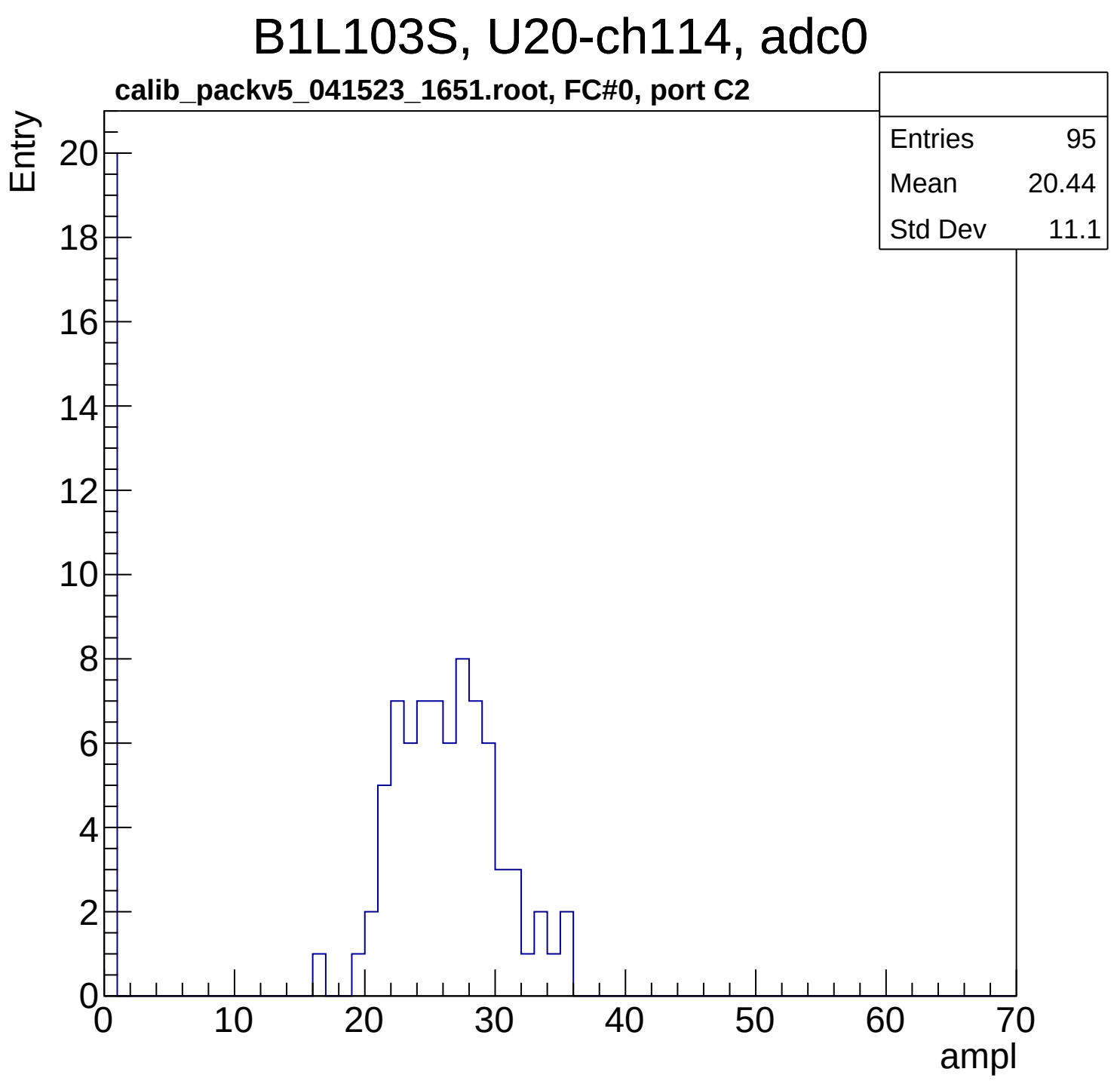
50
60
70
ampl


B1L103S, U20-ch114, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 20.44
Std Dev 11.1
Entry
ampl
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8
10
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0
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60
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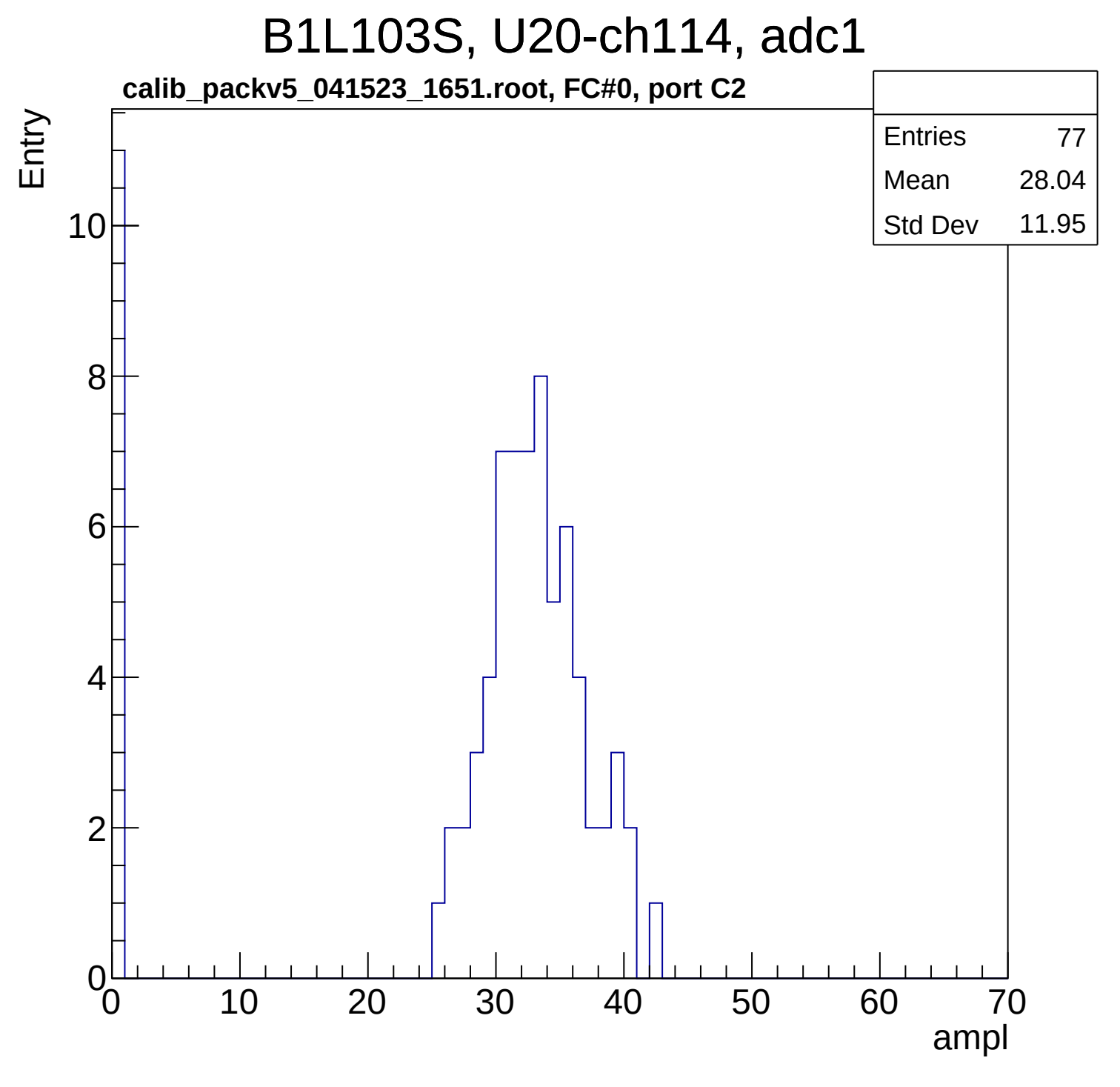
B1L103S, U20-ch114, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 28.04
Std Dev 11.95
Entry
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30
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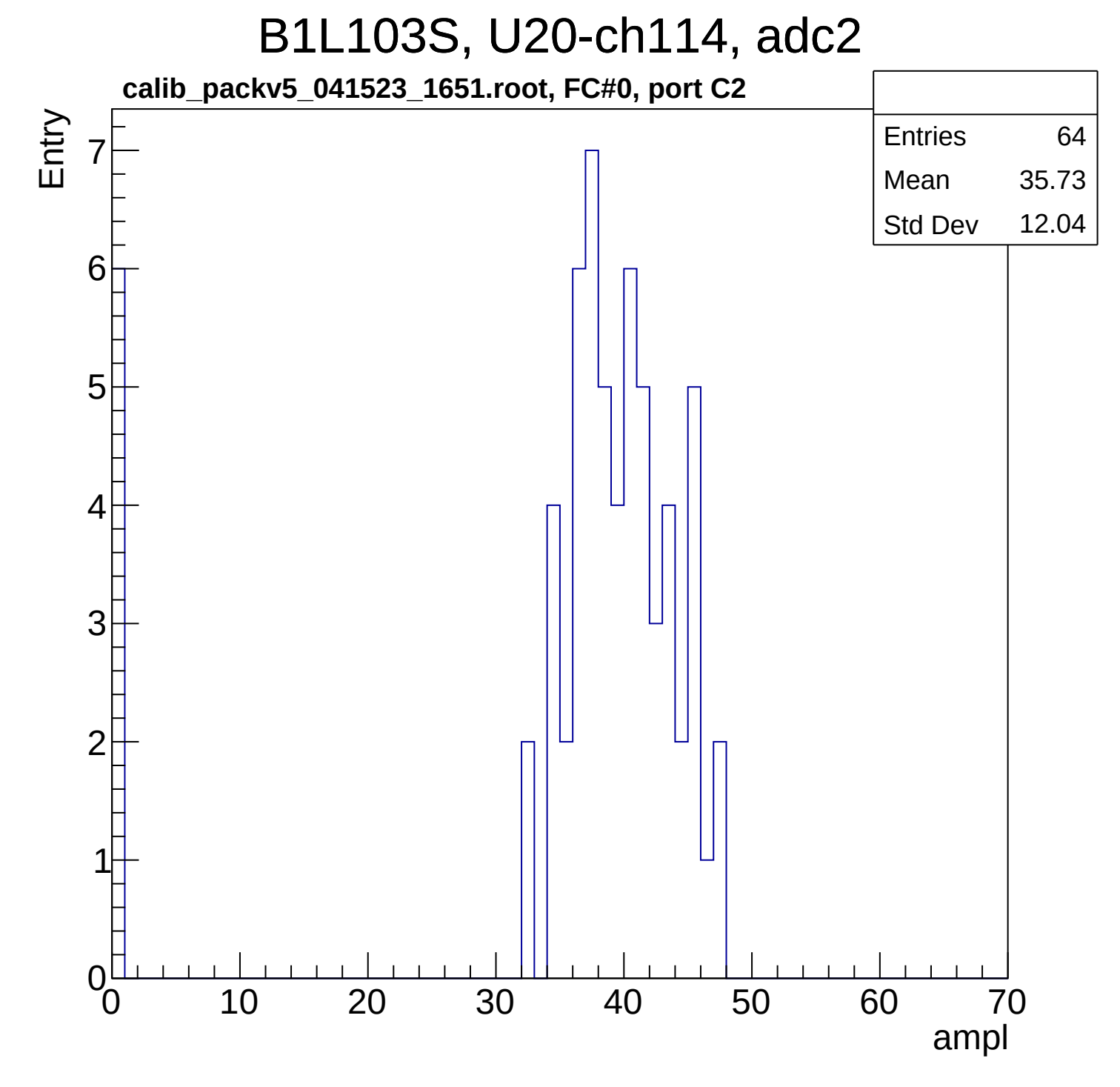
50
60
70
ampl


B1L103S, U20-ch114, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 35.73
Std Dev 12.04
Entry
ampl
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4
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0
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20
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40
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60
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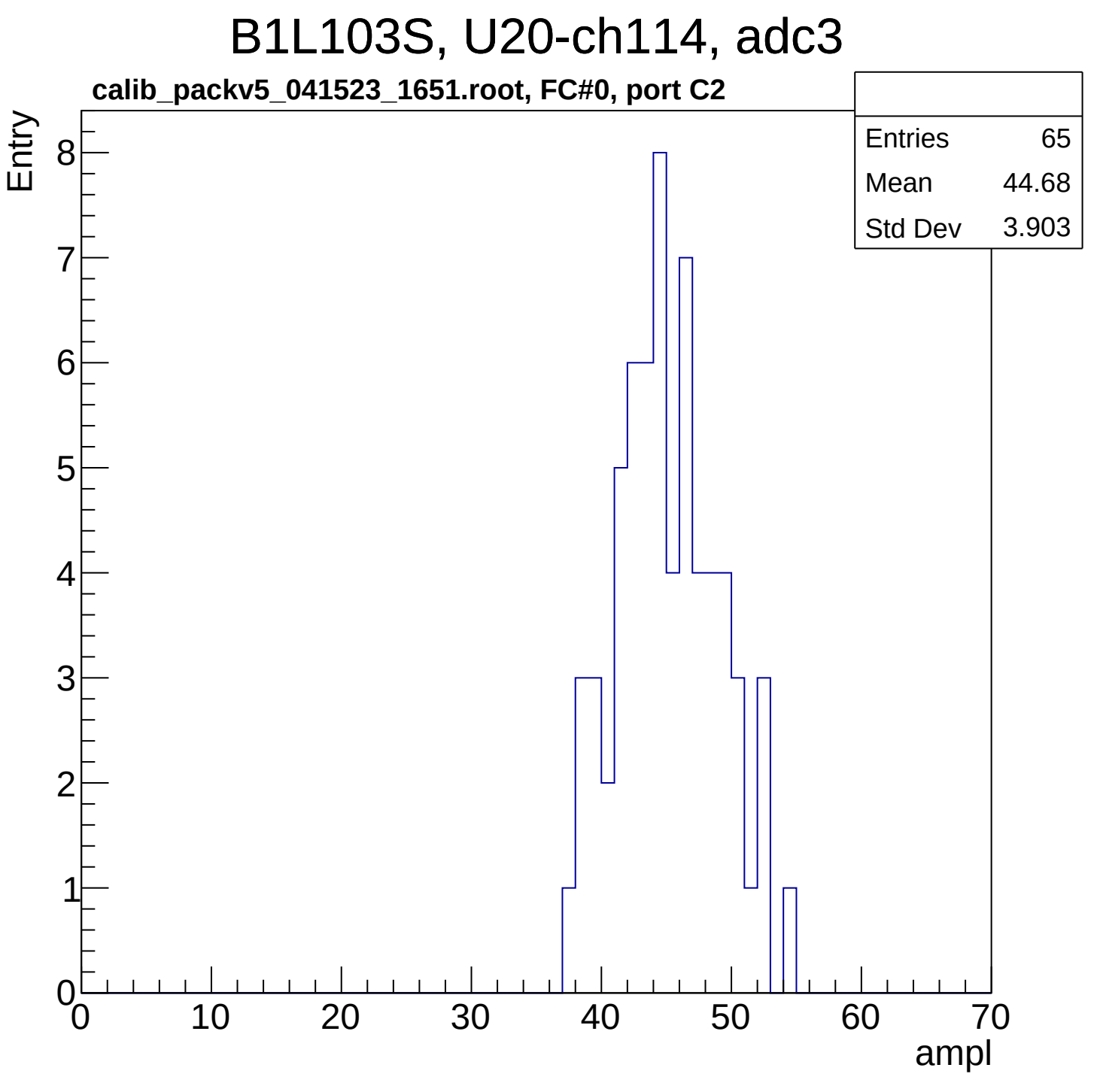
B1L103S, U20-ch114, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 44.68
Std Dev 3.903
Entry
ampl
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5
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0
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60
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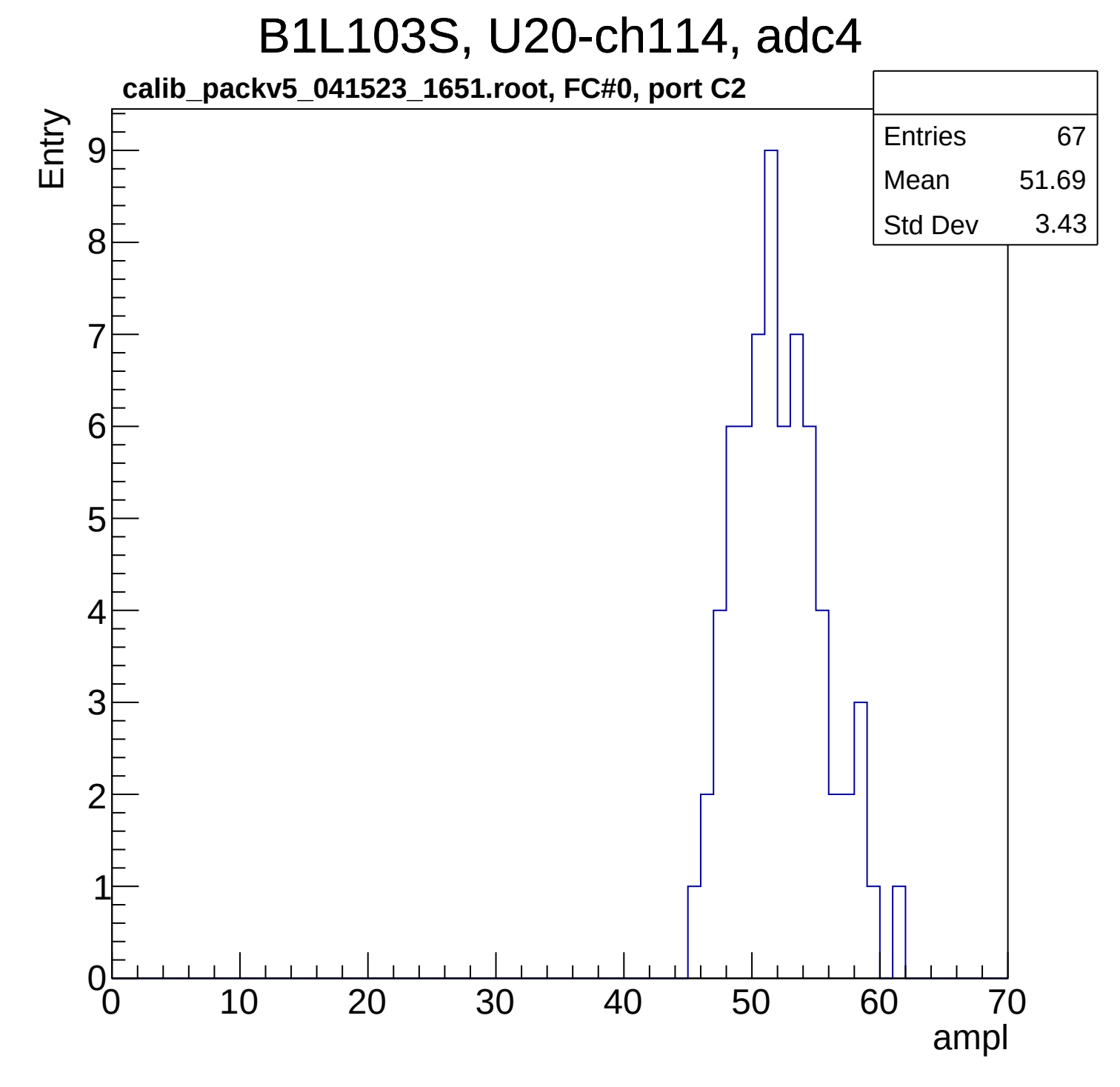
B1L103S, U20-ch114, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 51.69
Std Dev 3.43
Entry
ampl
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6
7
8
9
0
10
20
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40
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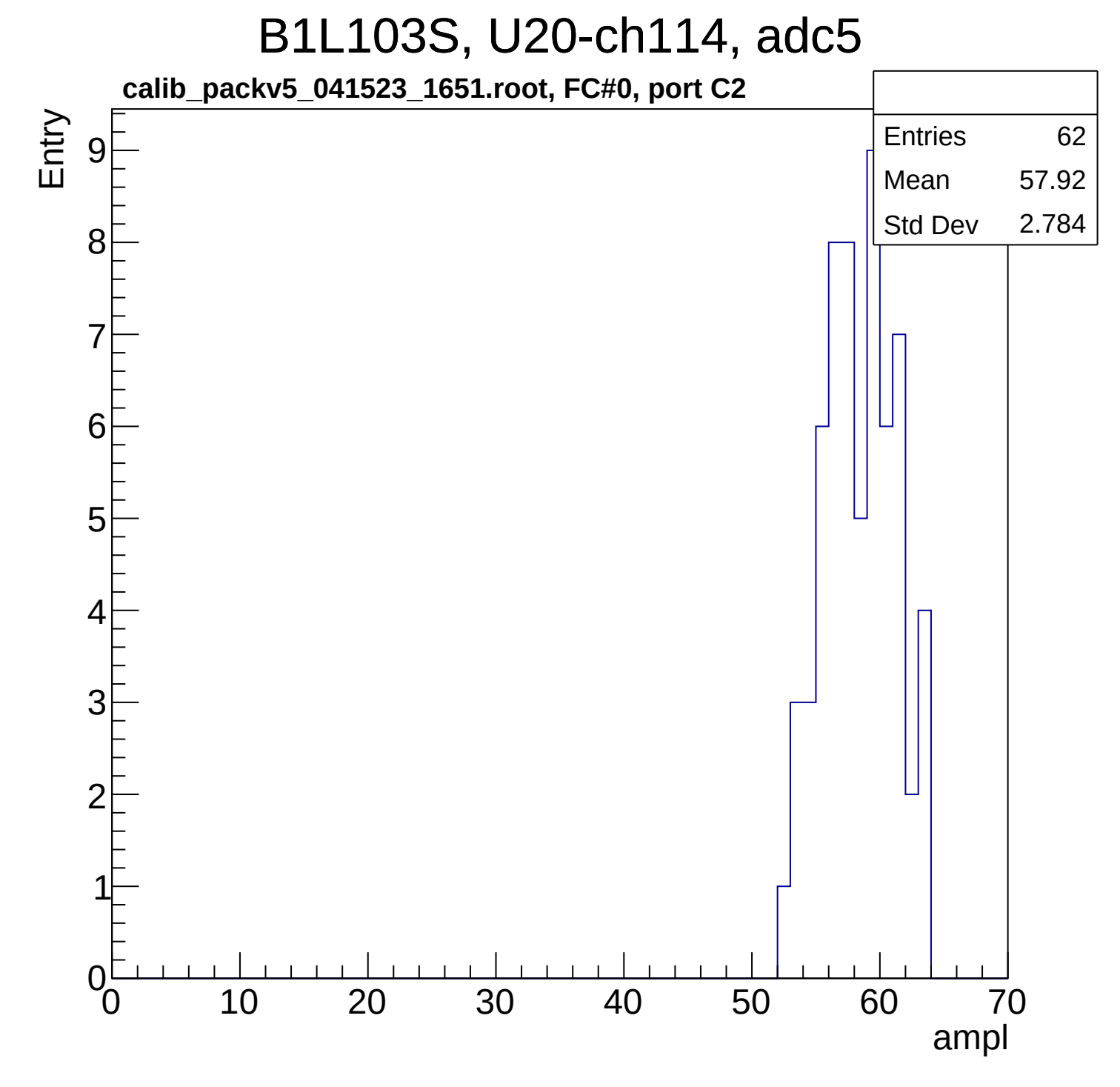
60
70


B1L103S, U20-ch114, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 57.92
Std Dev 2.784
Entry
ampl
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0
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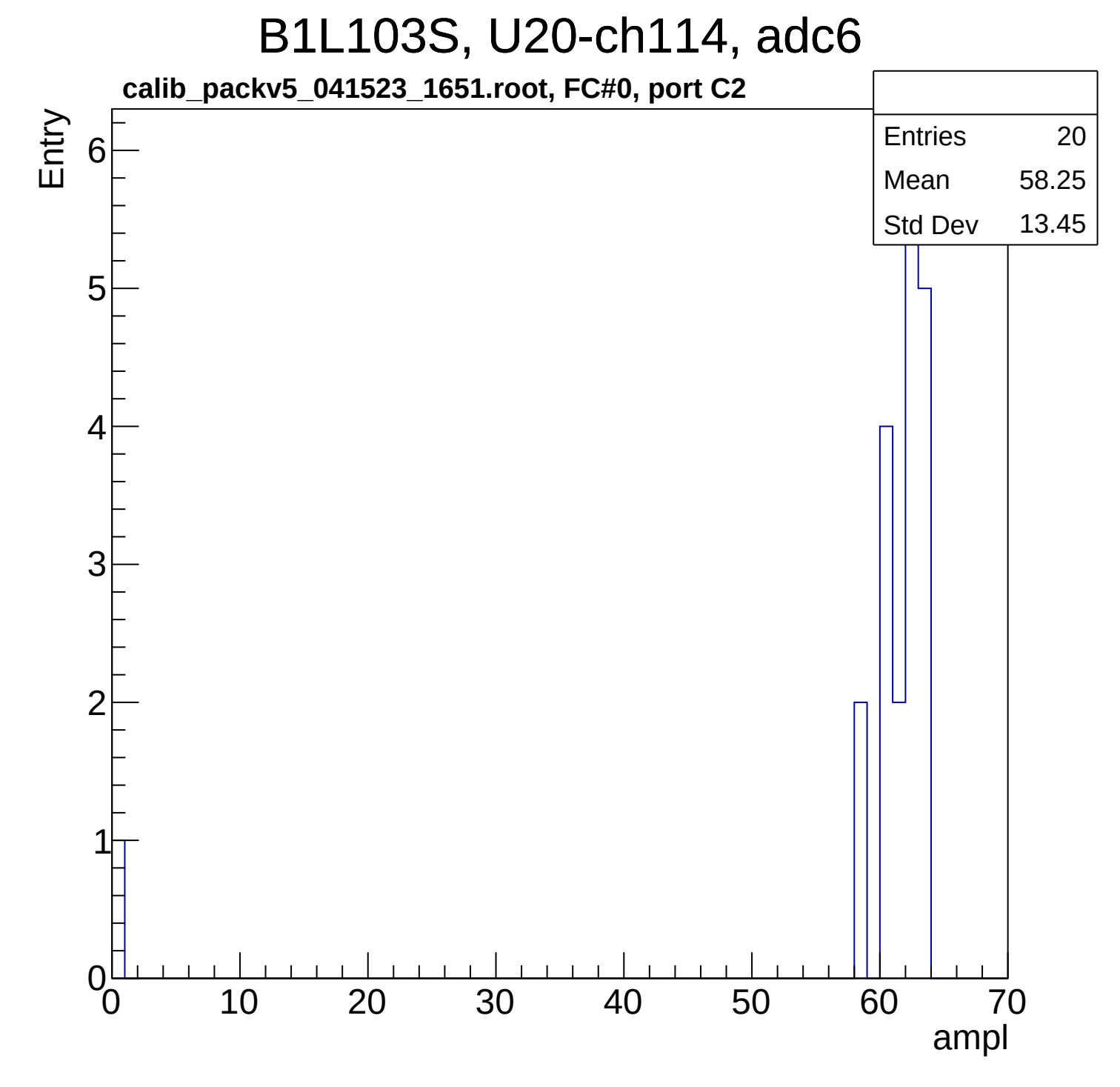
B1L103S, U20-ch114, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 58.25
Std Dev 13.45
Entry
ampl
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1
2
3
4
5
6
0
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20
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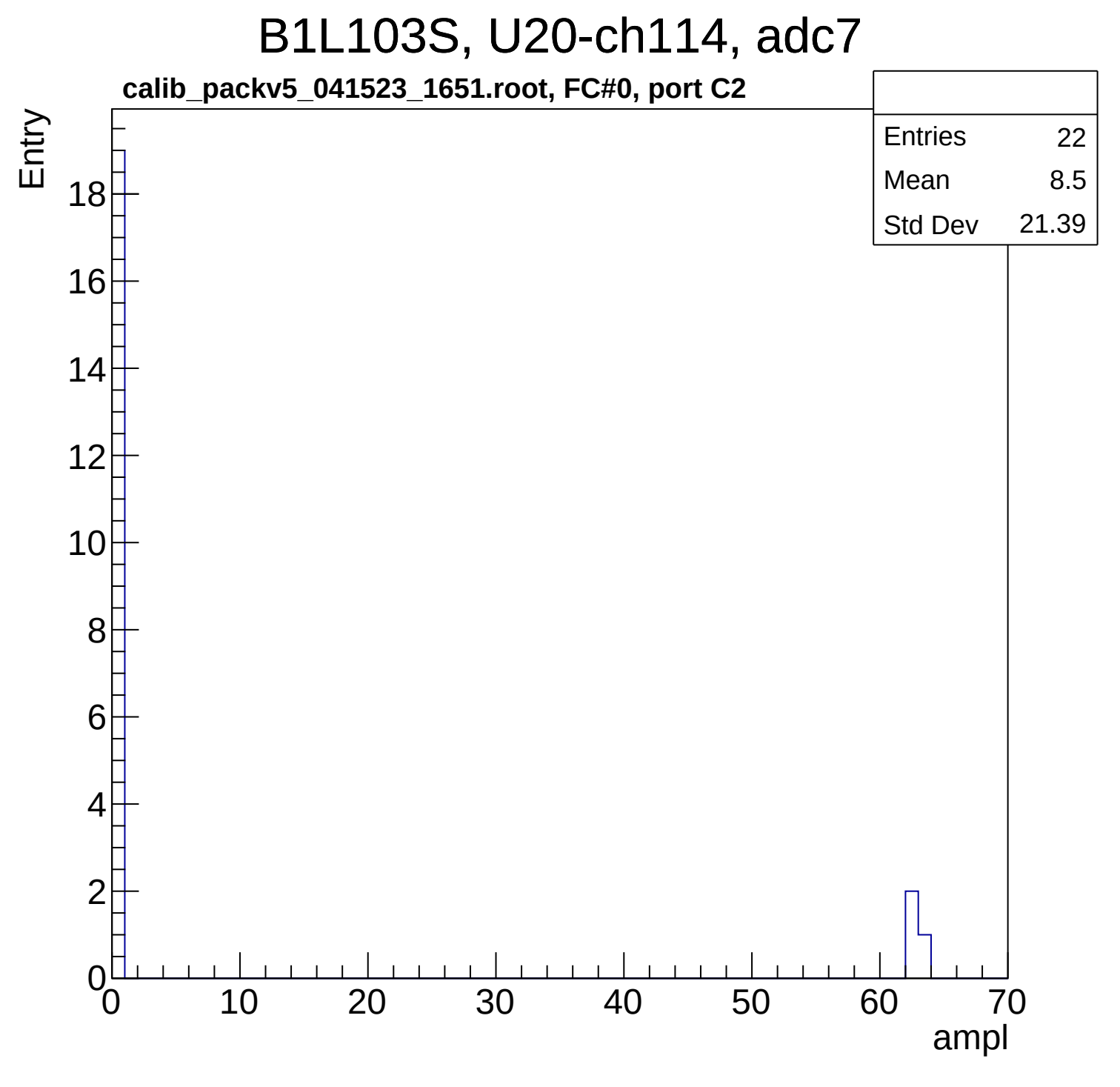
40
50
60
70


B1L103S, U20-ch114, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.5
Std Dev 21.39
Entry
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8
10
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14
16
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30
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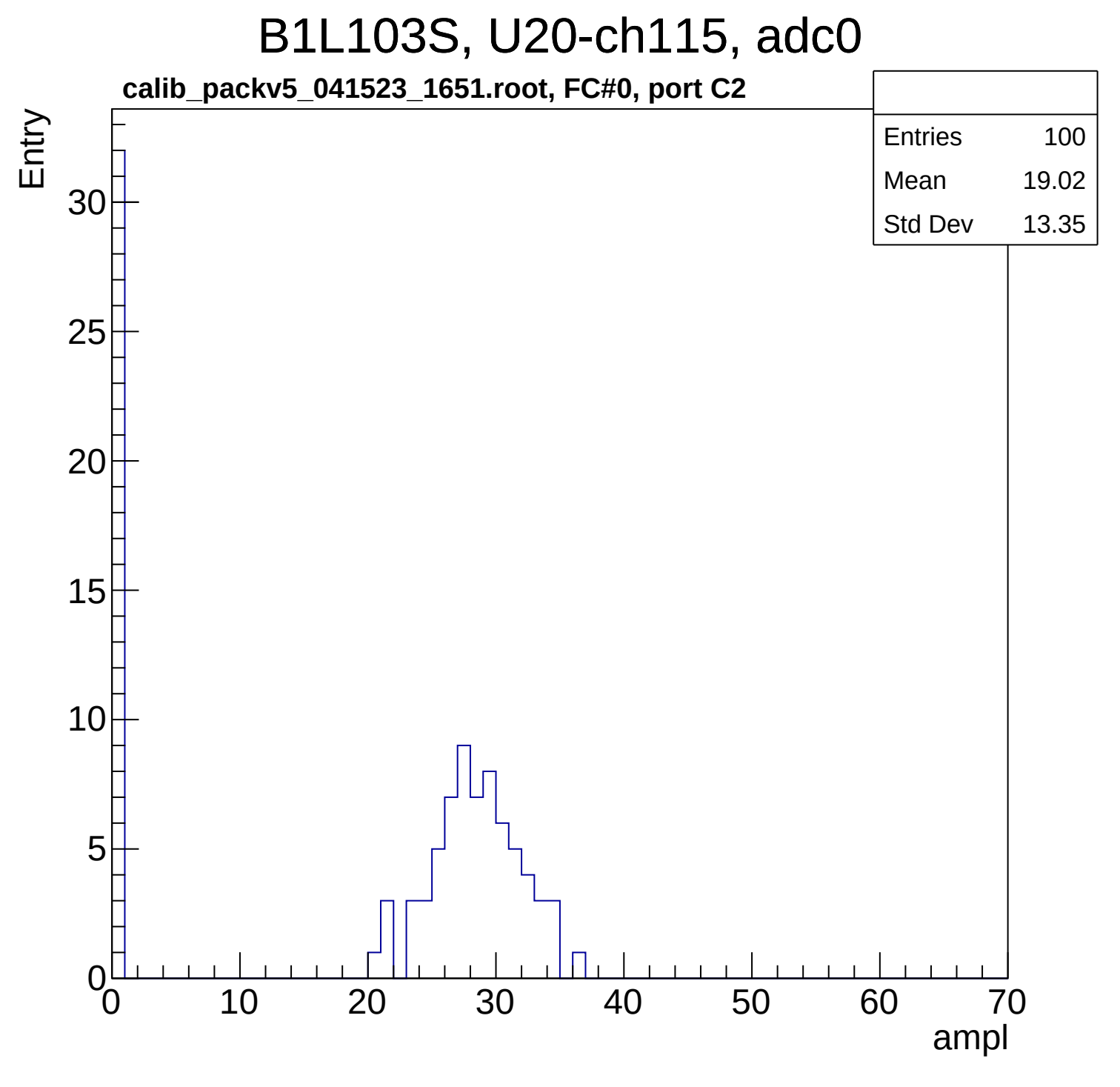
50
60
70
ampl


B1L103S, U20-ch115, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 100
Mean 19.02
Std Dev 13.35
Entry
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20
25
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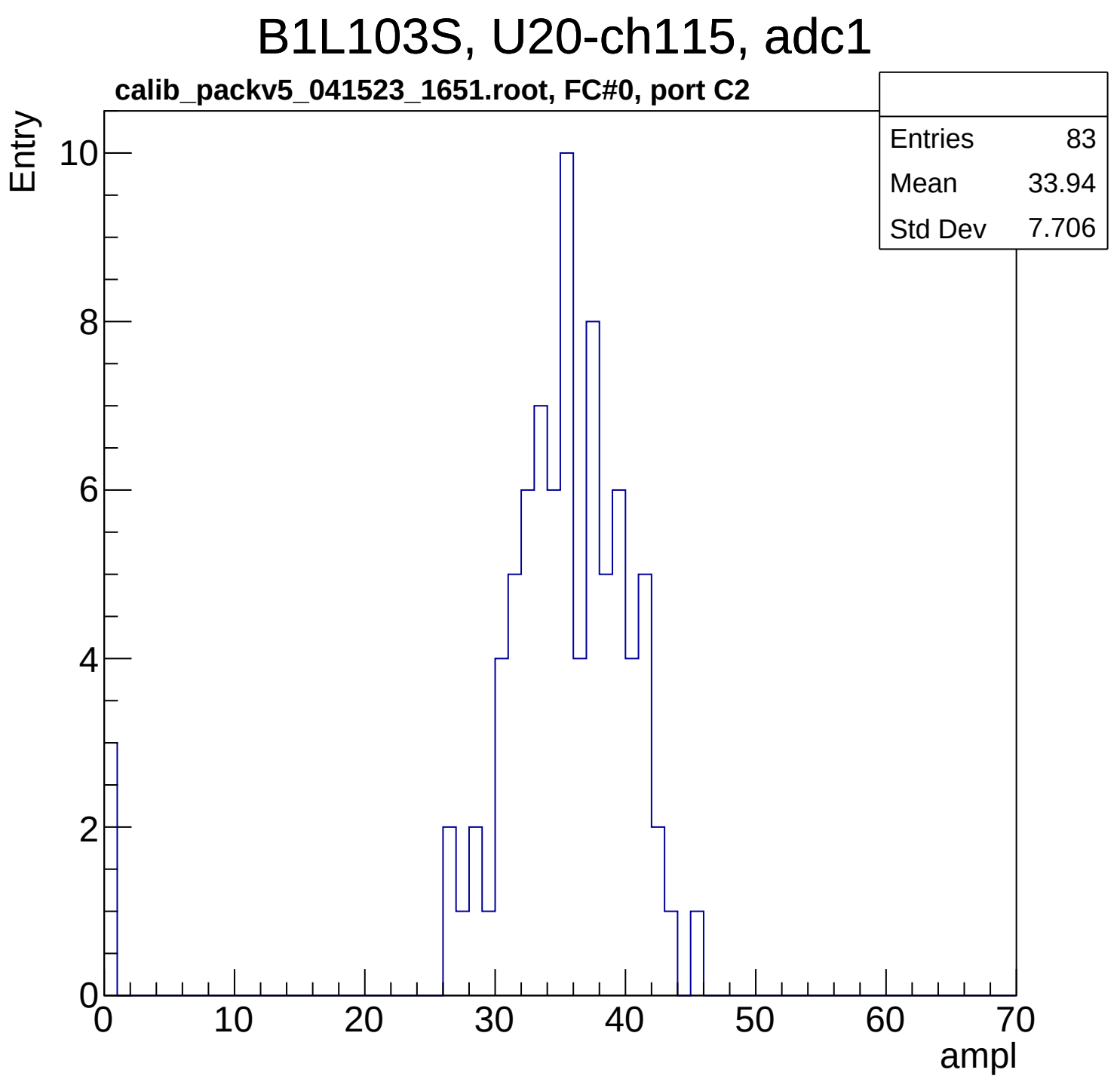
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch115, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 33.94
Std Dev 7.706
Entry
0
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4
6
8
10
0
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20
30
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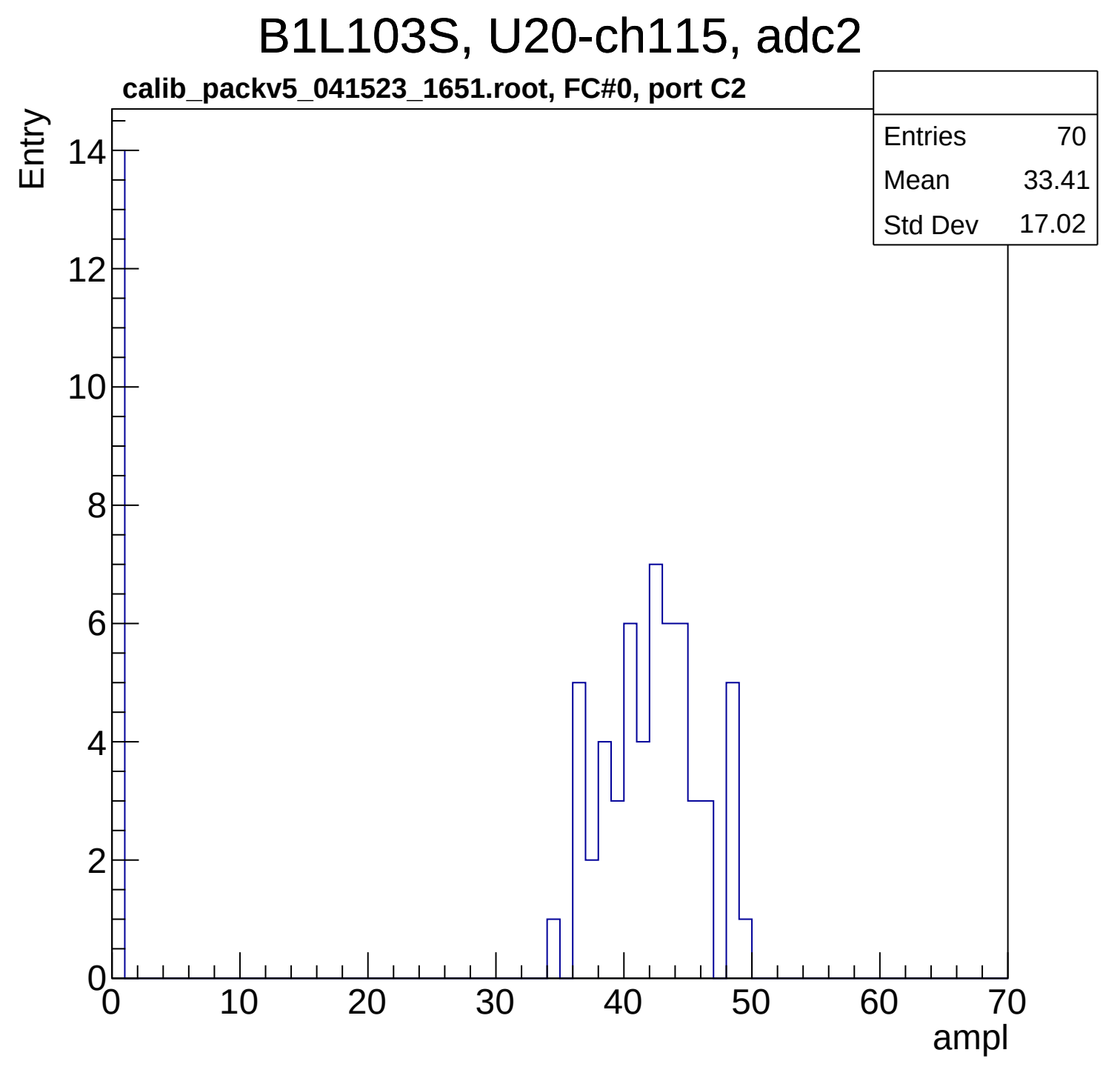
50
60
70
ampl


B1L103S, U20-ch115, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 33.41
Std Dev 17.02
Entry
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4
6
8
10
12
14
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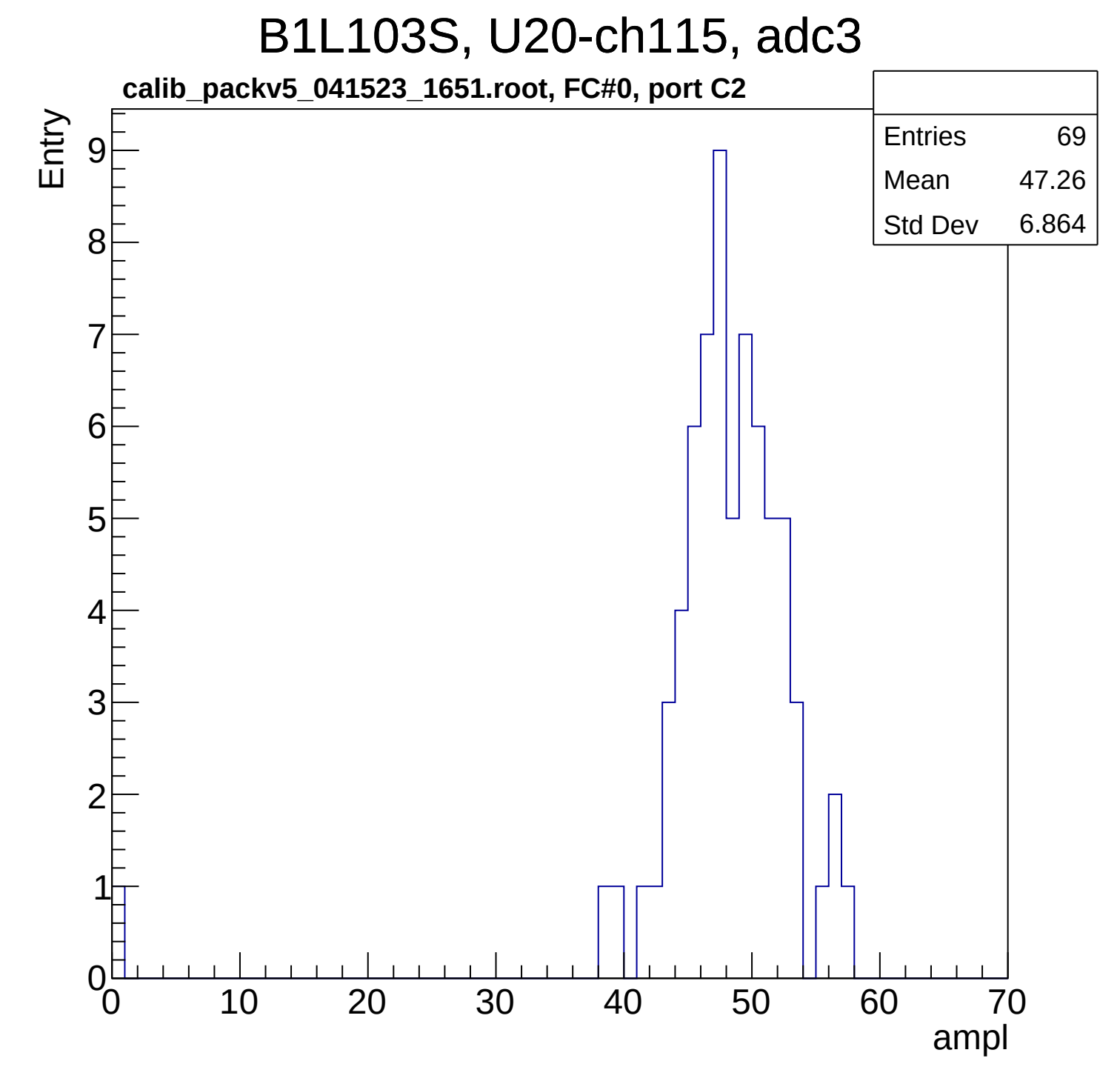
50
60
70
ampl


B1L103S, U20-ch115, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 47.26
Std Dev 6.864
Entry
ampl
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3
4
5
6
7
8
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0
10
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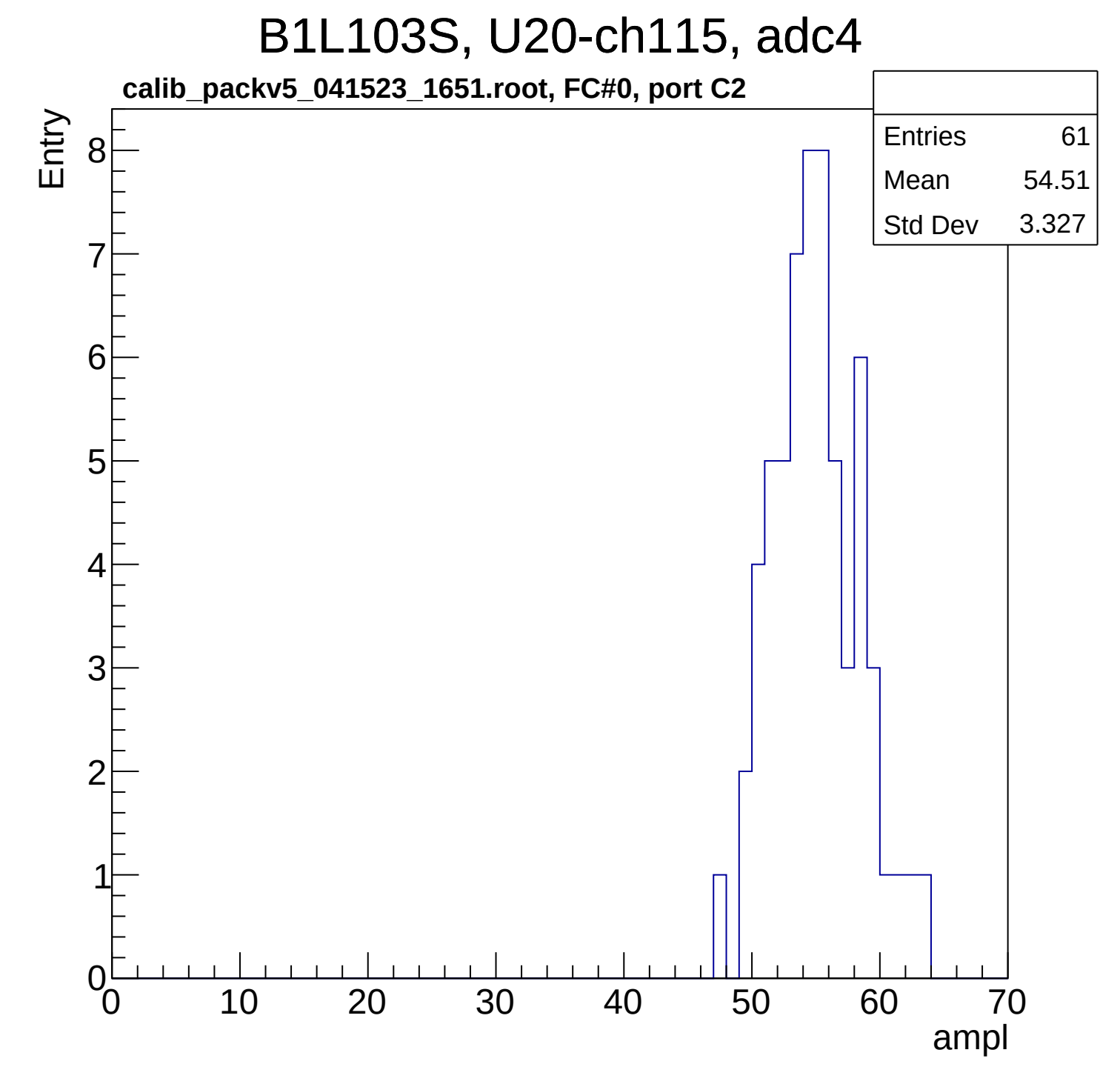
B1L103S, U20-ch115, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 54.51
Std Dev 3.327
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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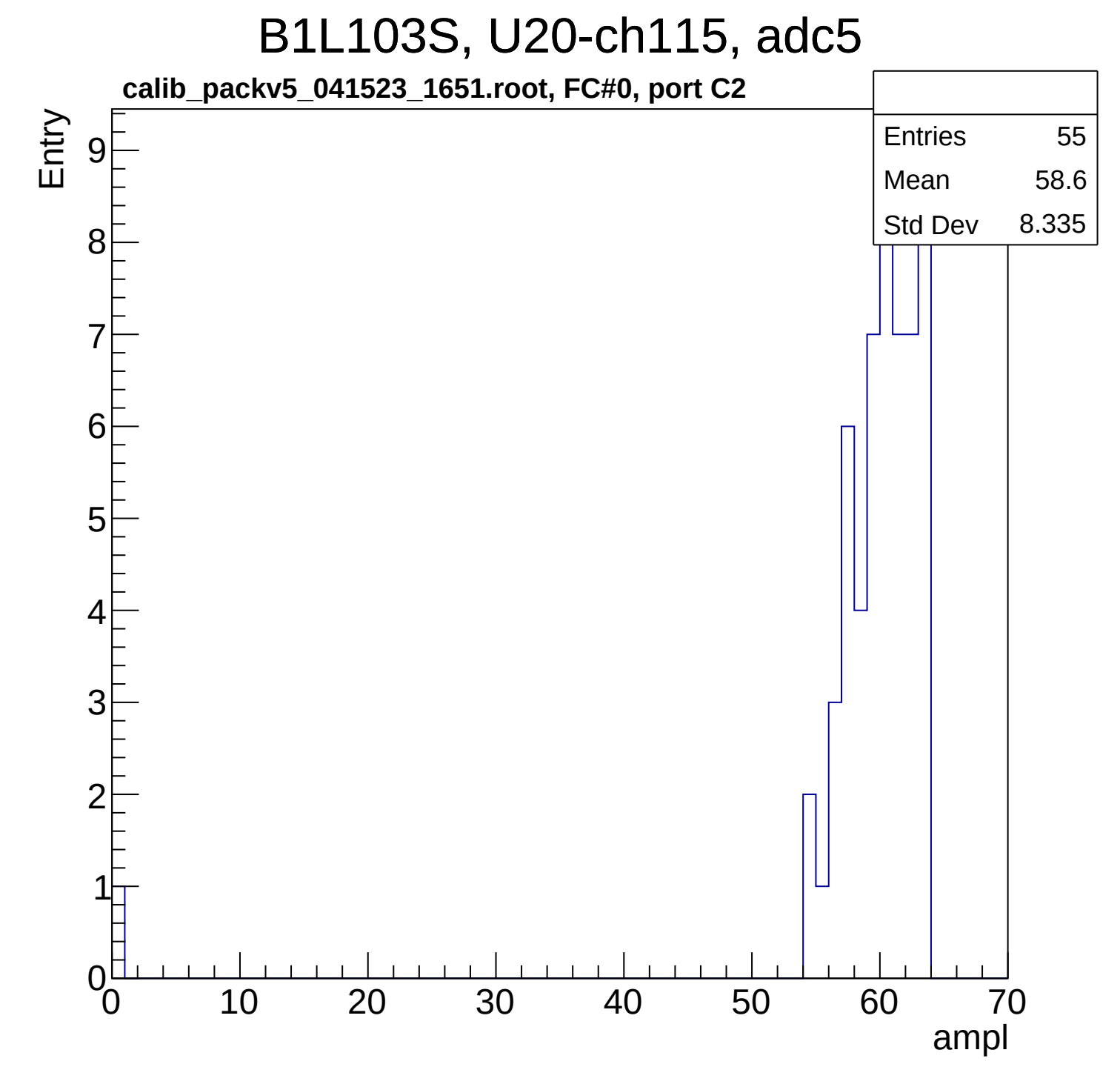
B1L103S, U20-ch115, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 58.6
Std Dev 8.335
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
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40
50
60
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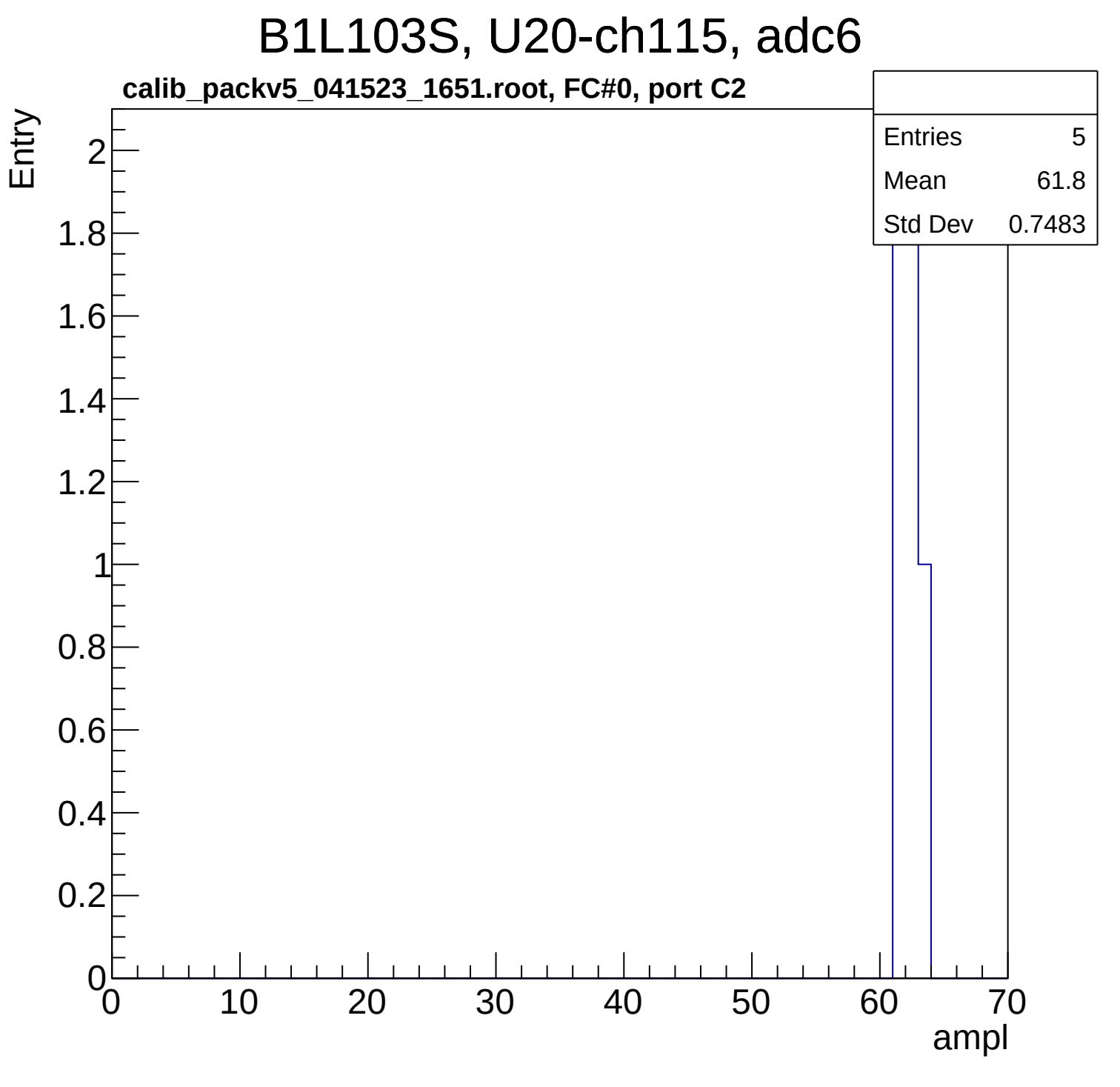
B1L103S, U20-ch115, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 61.8
Std Dev 0.7483
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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20
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40
50
60
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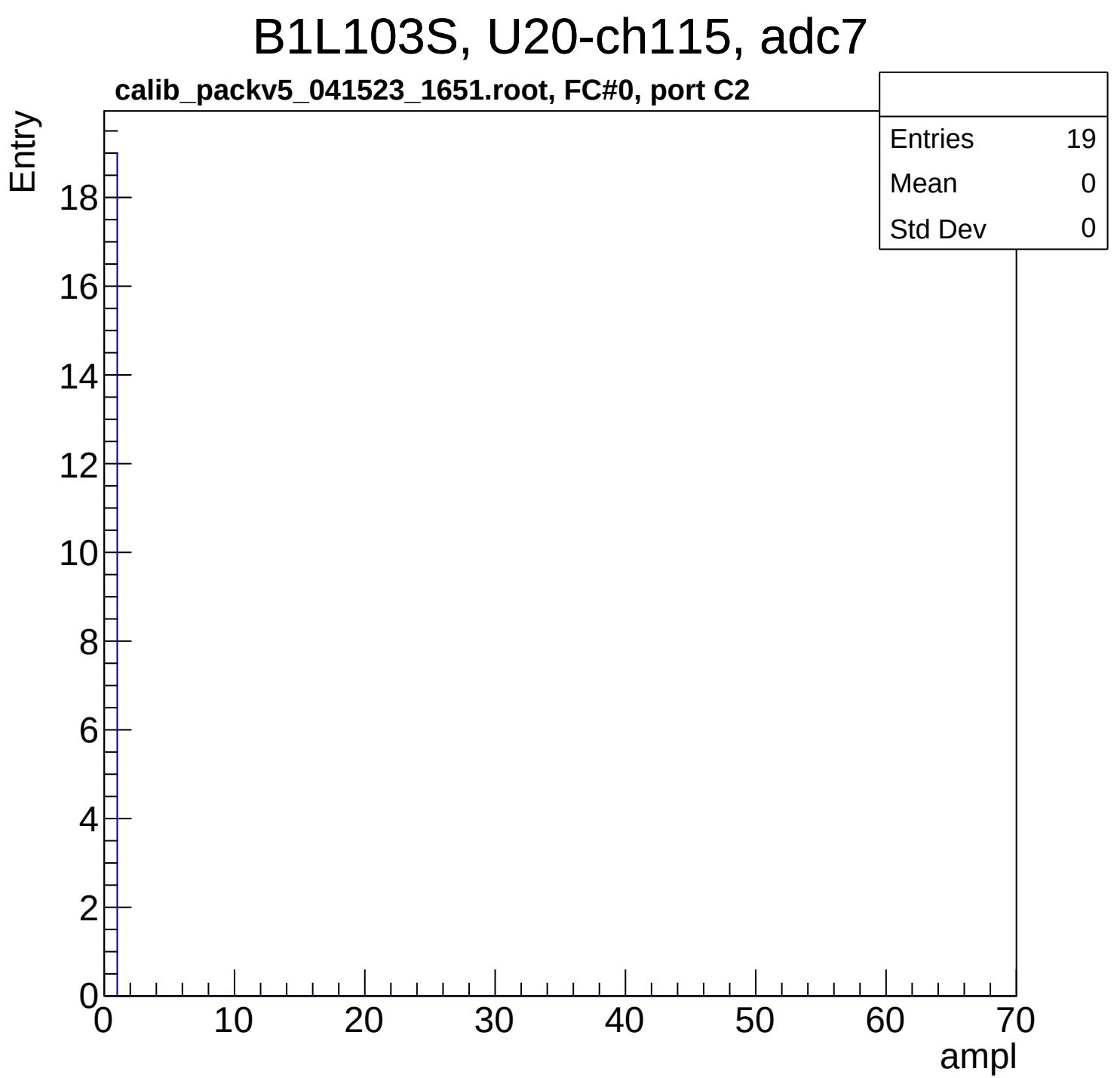
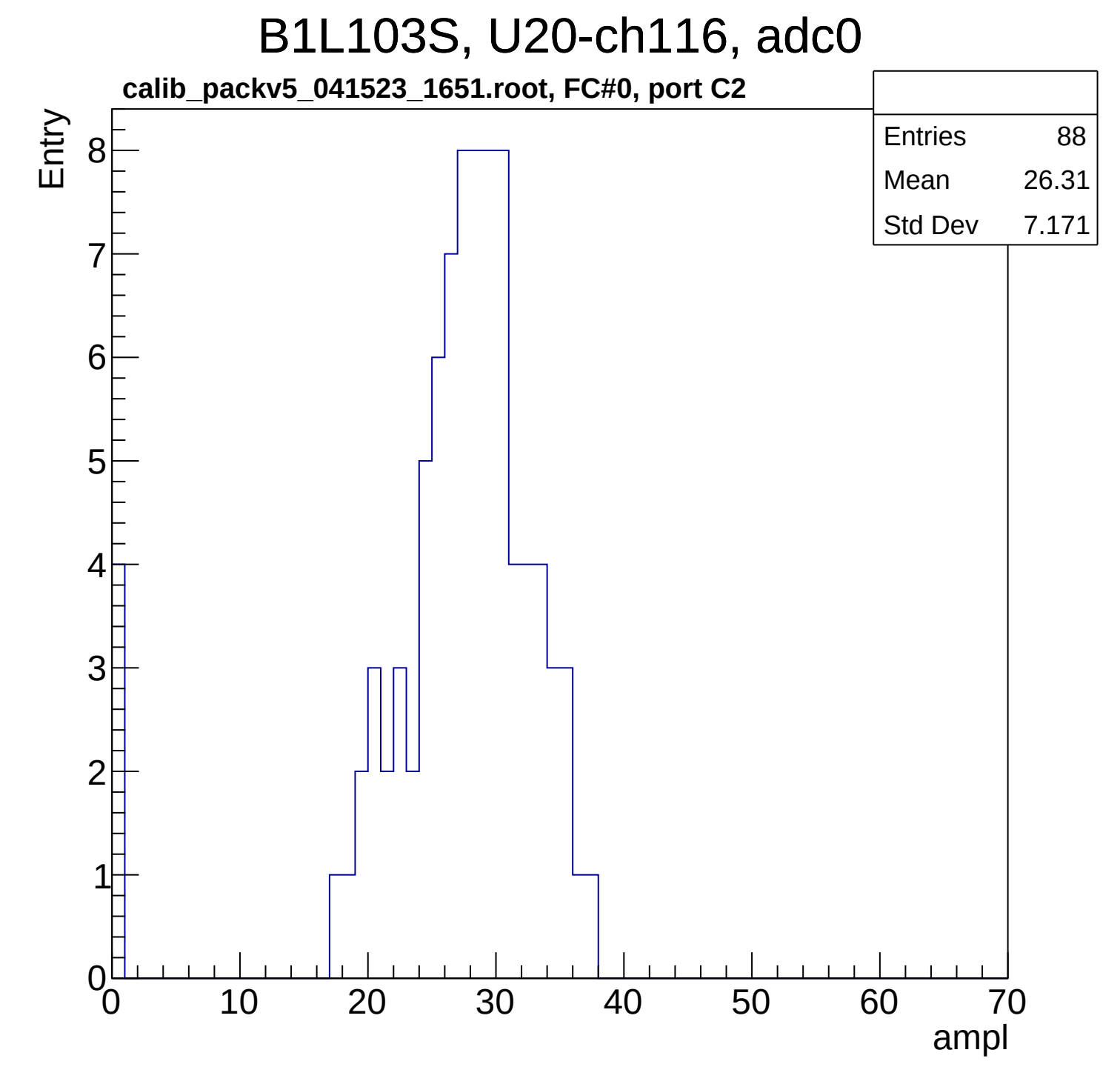

B1L103S, U20-ch115, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch116, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 26.31
Std Dev 7.171
Entry
ampl
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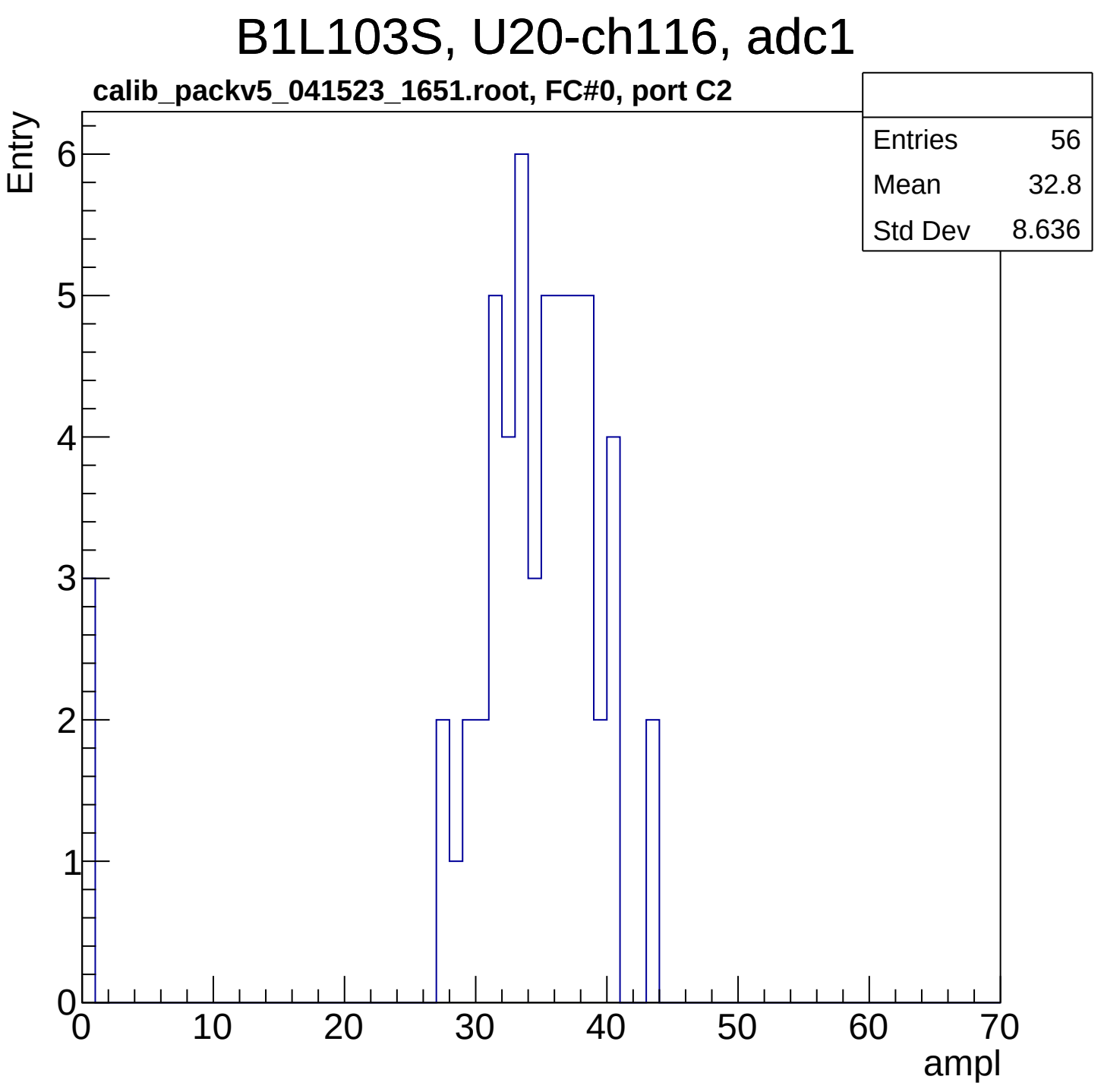
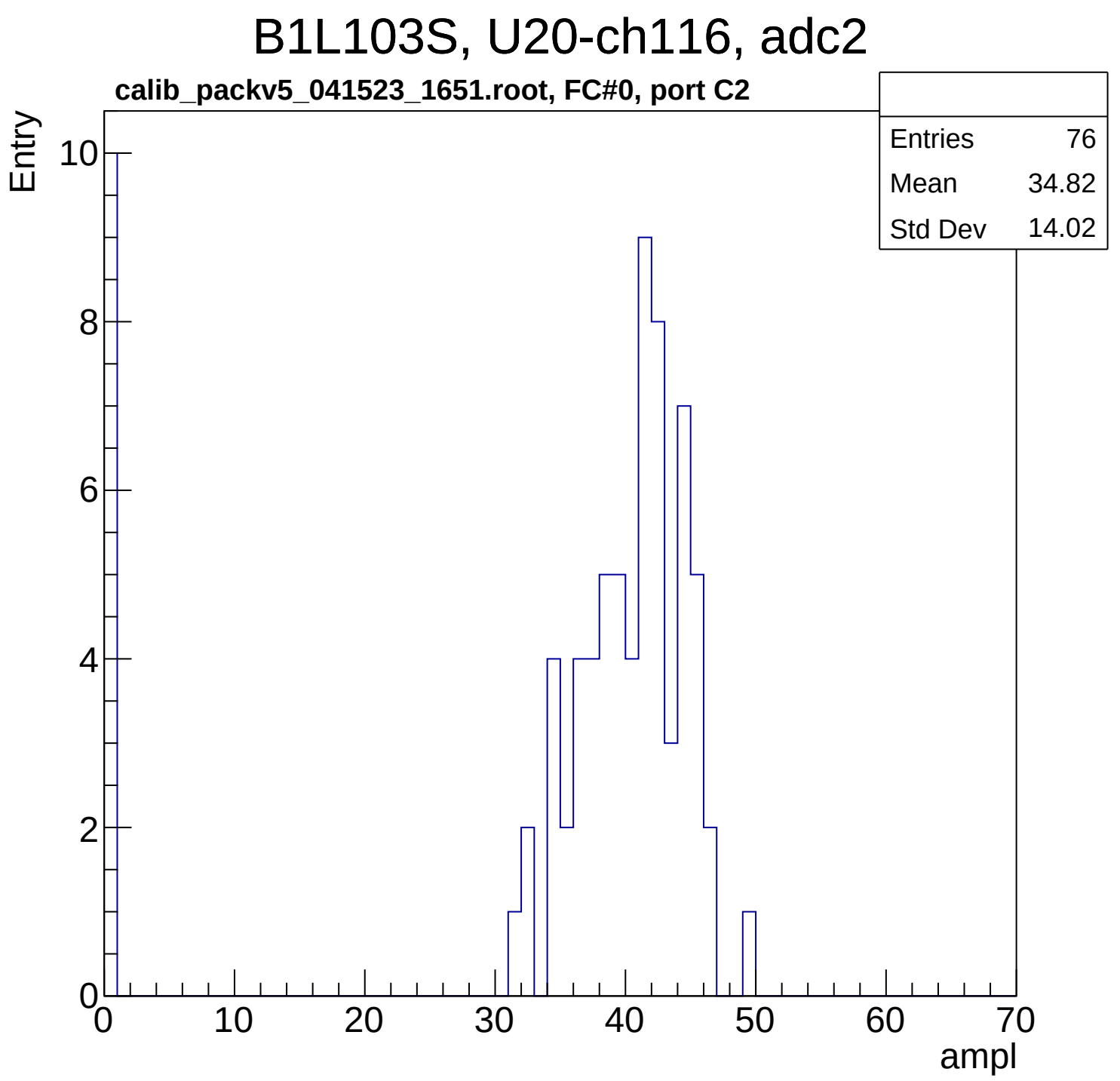
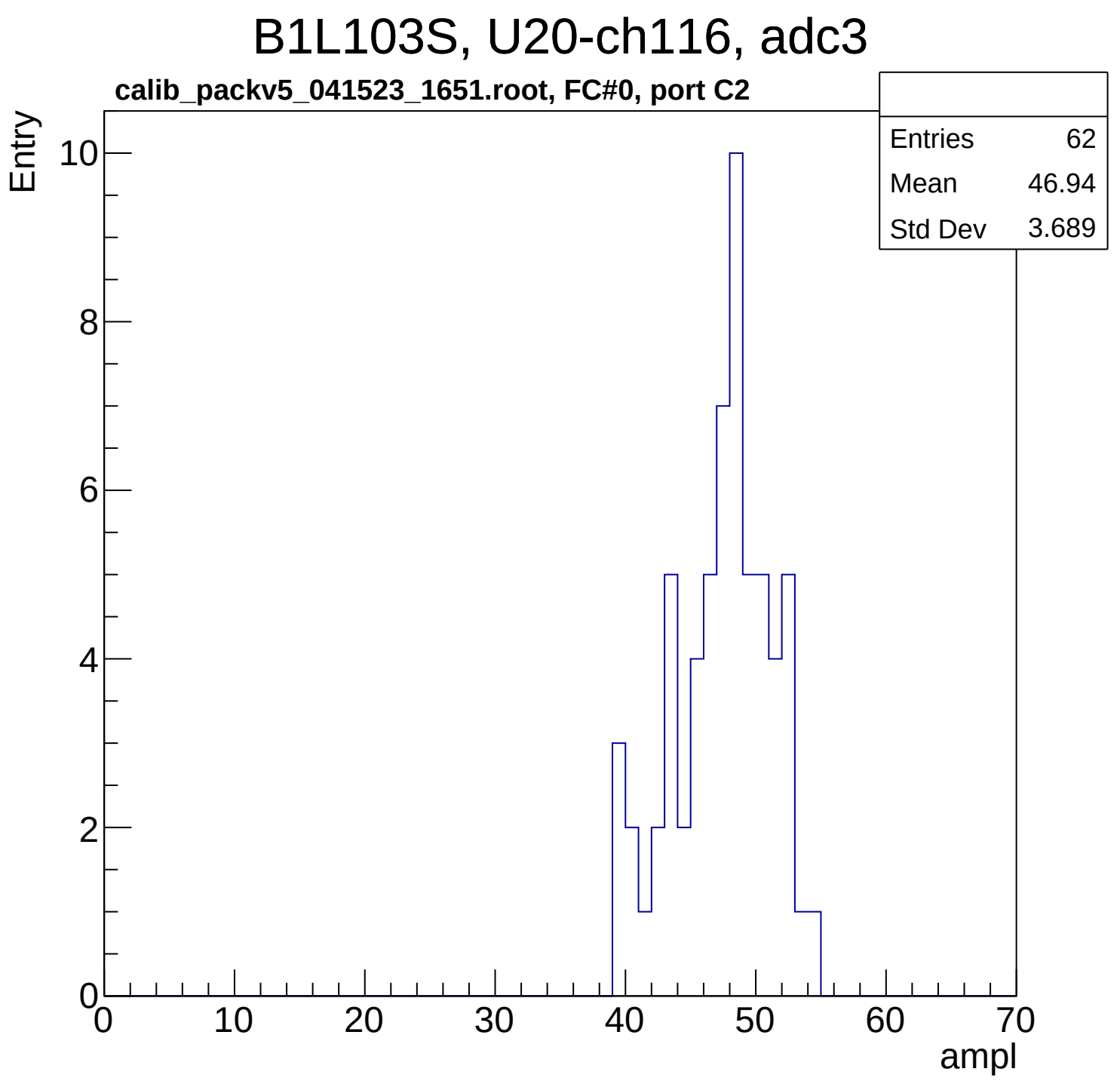
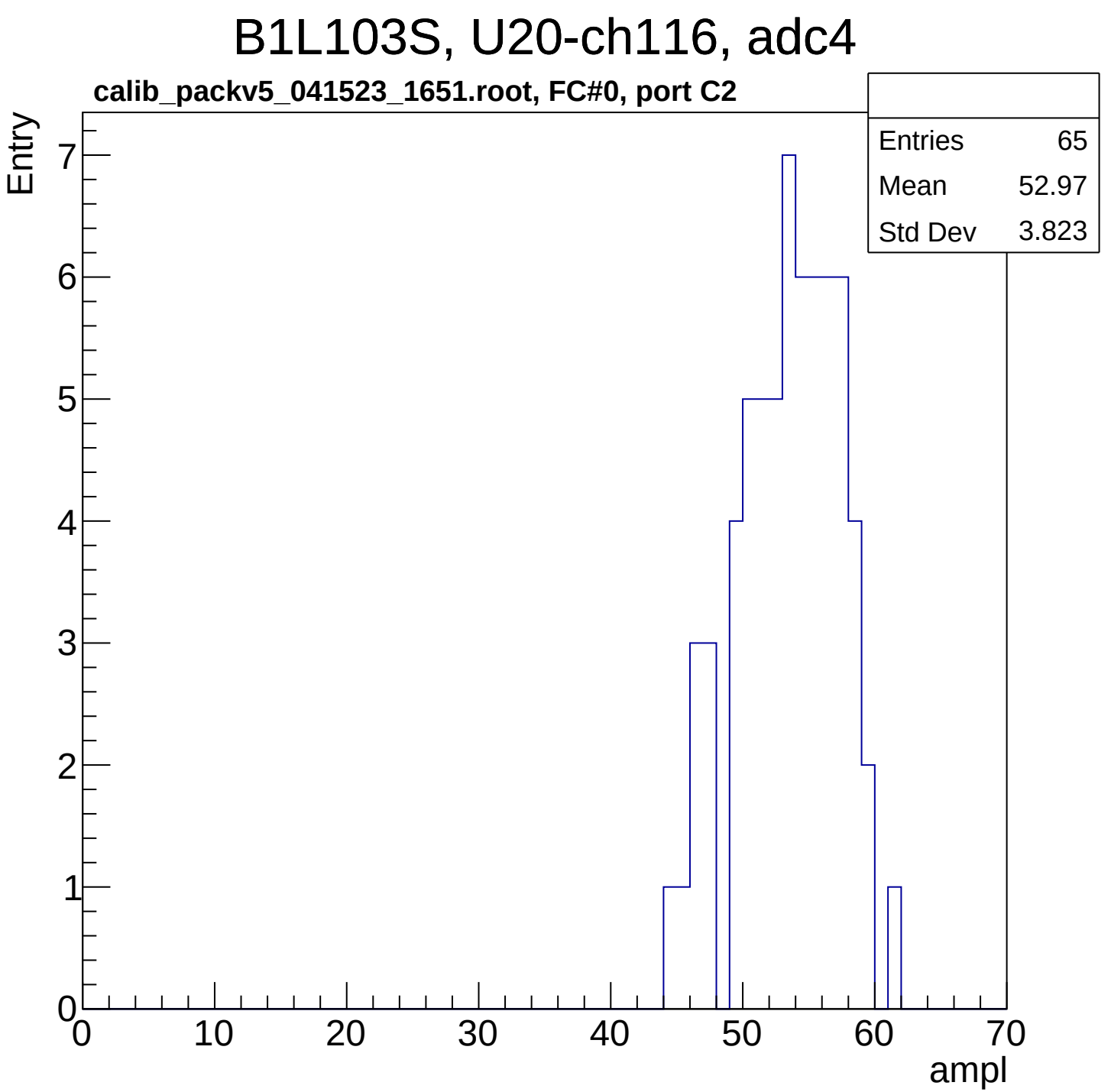
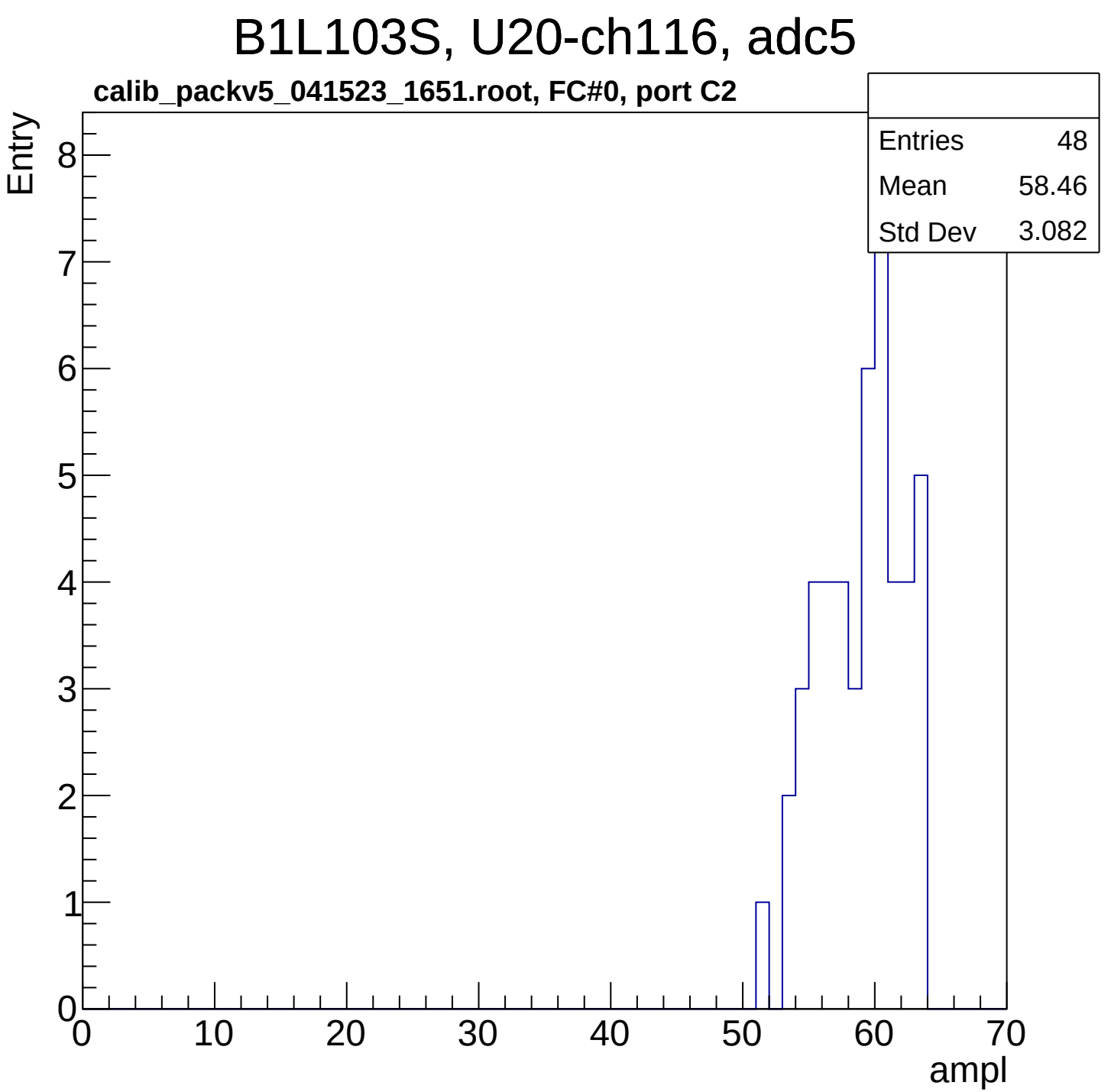
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch116, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 32.8
Std Dev 8.636
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch116, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 34.82
Std Dev 14.02
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U20-ch116, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 46.94
Std Dev 3.689
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U20-ch116, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 52.97
Std Dev 3.823
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U20-ch116, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 58.46
Std Dev 3.082
Entry
ampl
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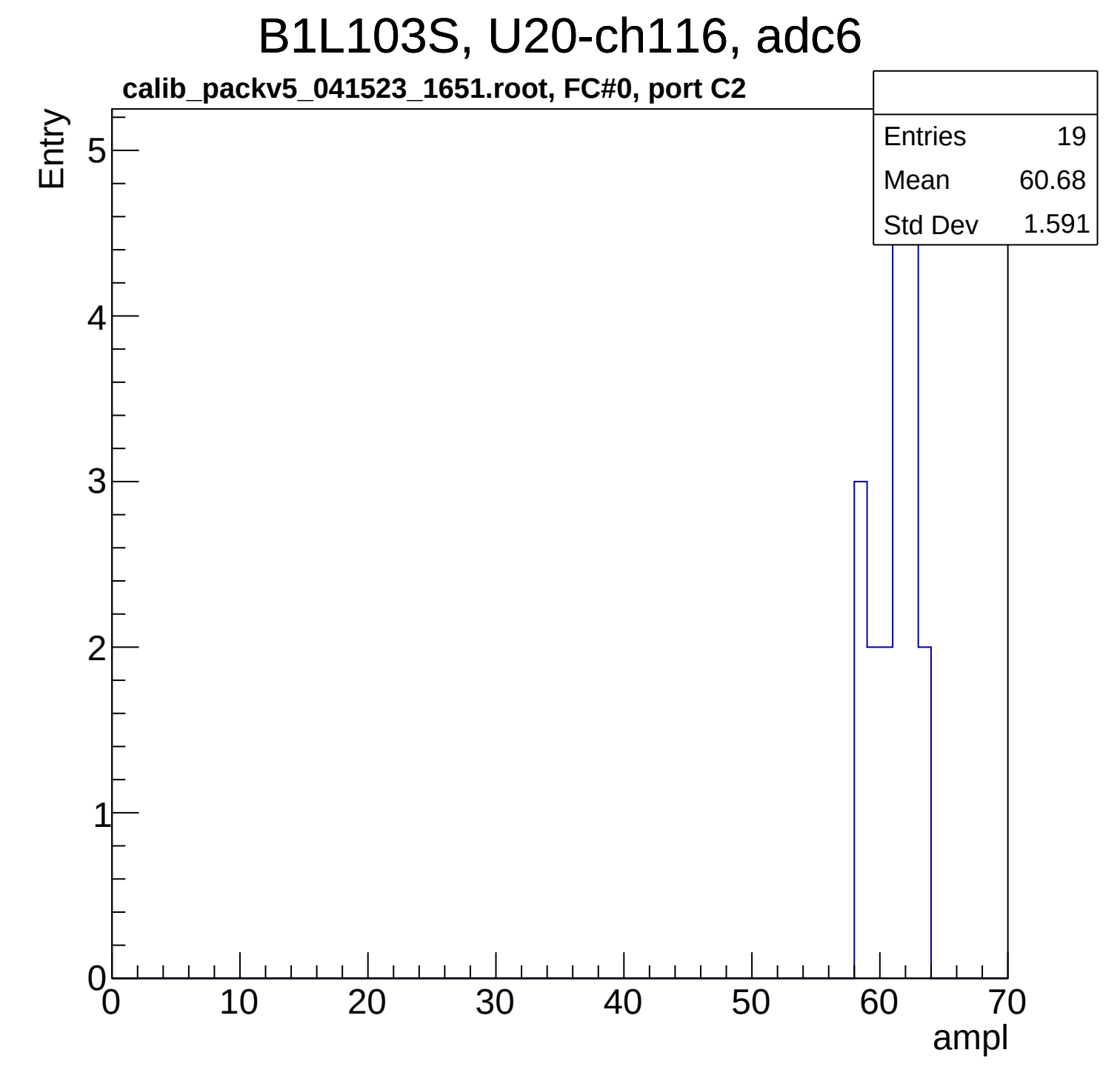
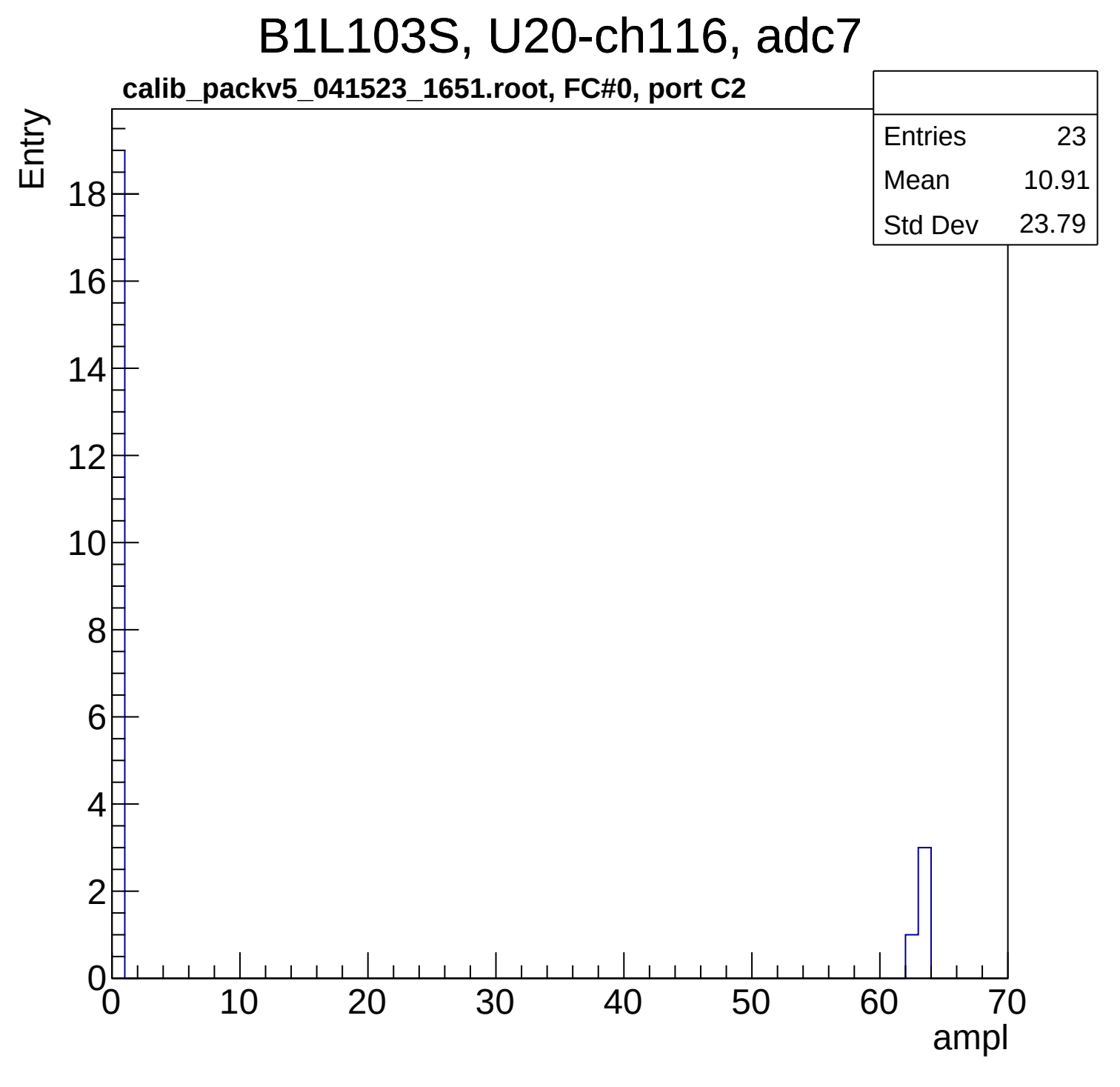
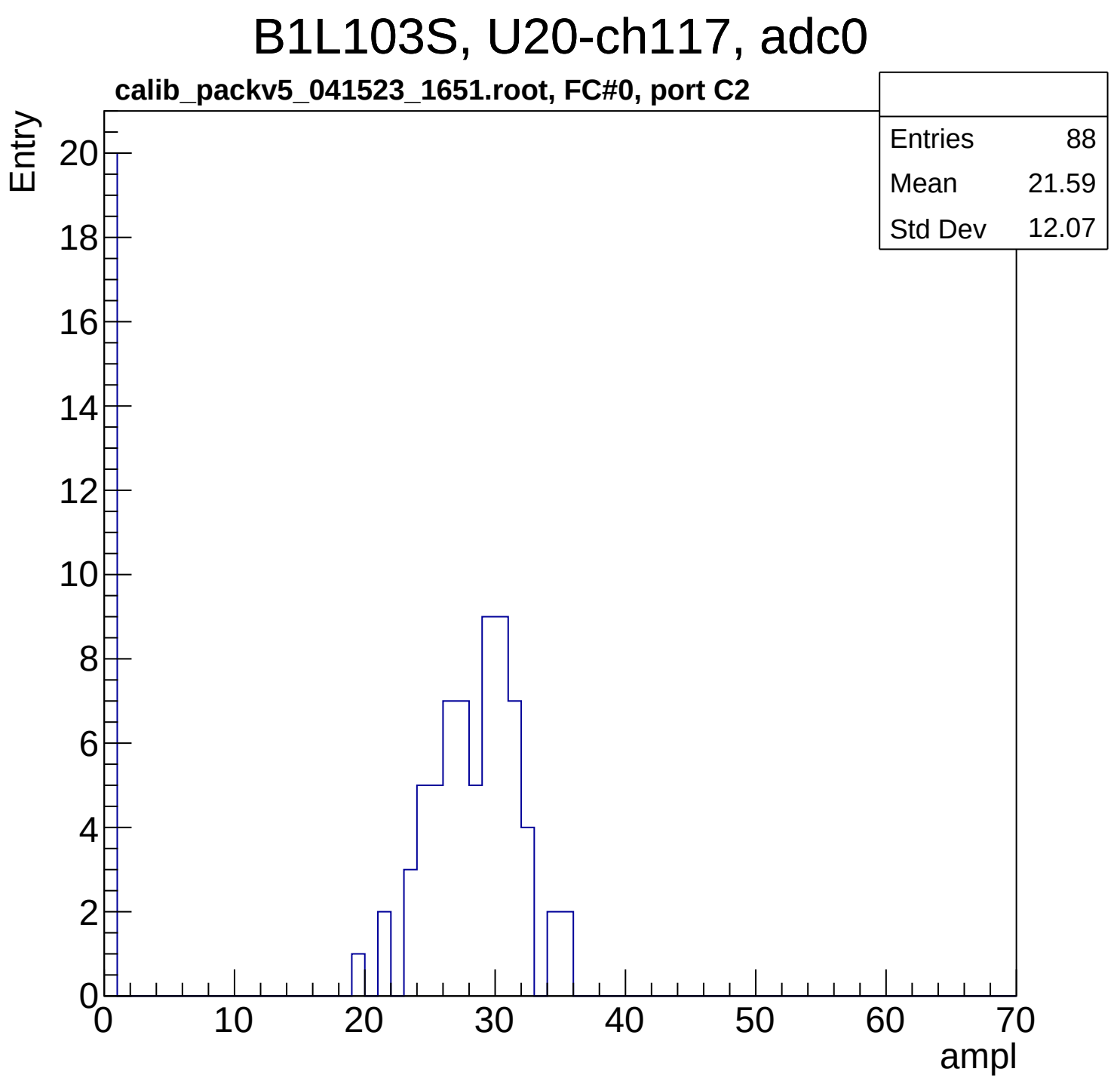
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch116, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 60.68
Std Dev 1.591
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U20-ch116, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 10.91
Std Dev 23.79
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch117, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 21.59
Std Dev 12.07
Entry
ampl
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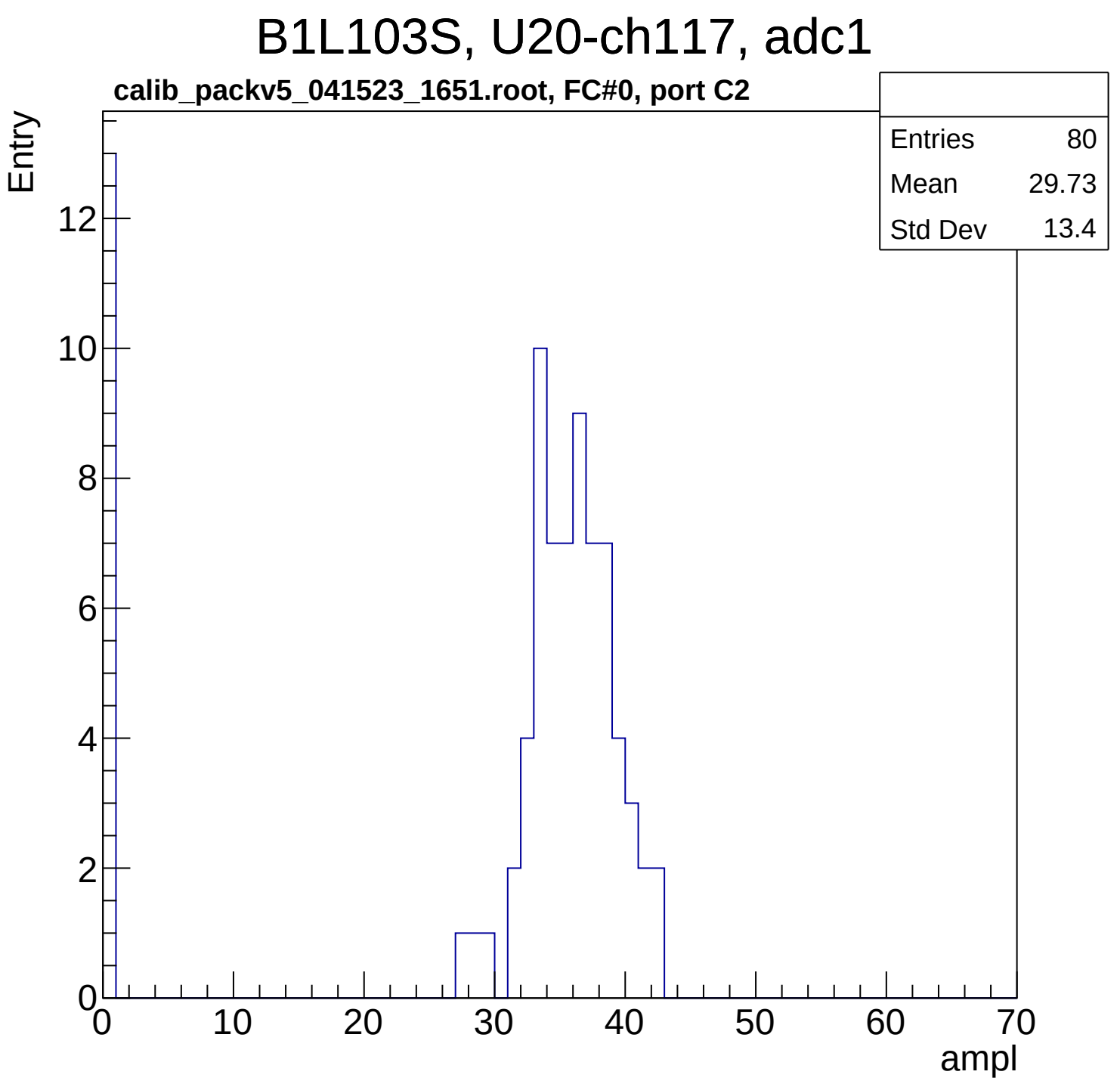
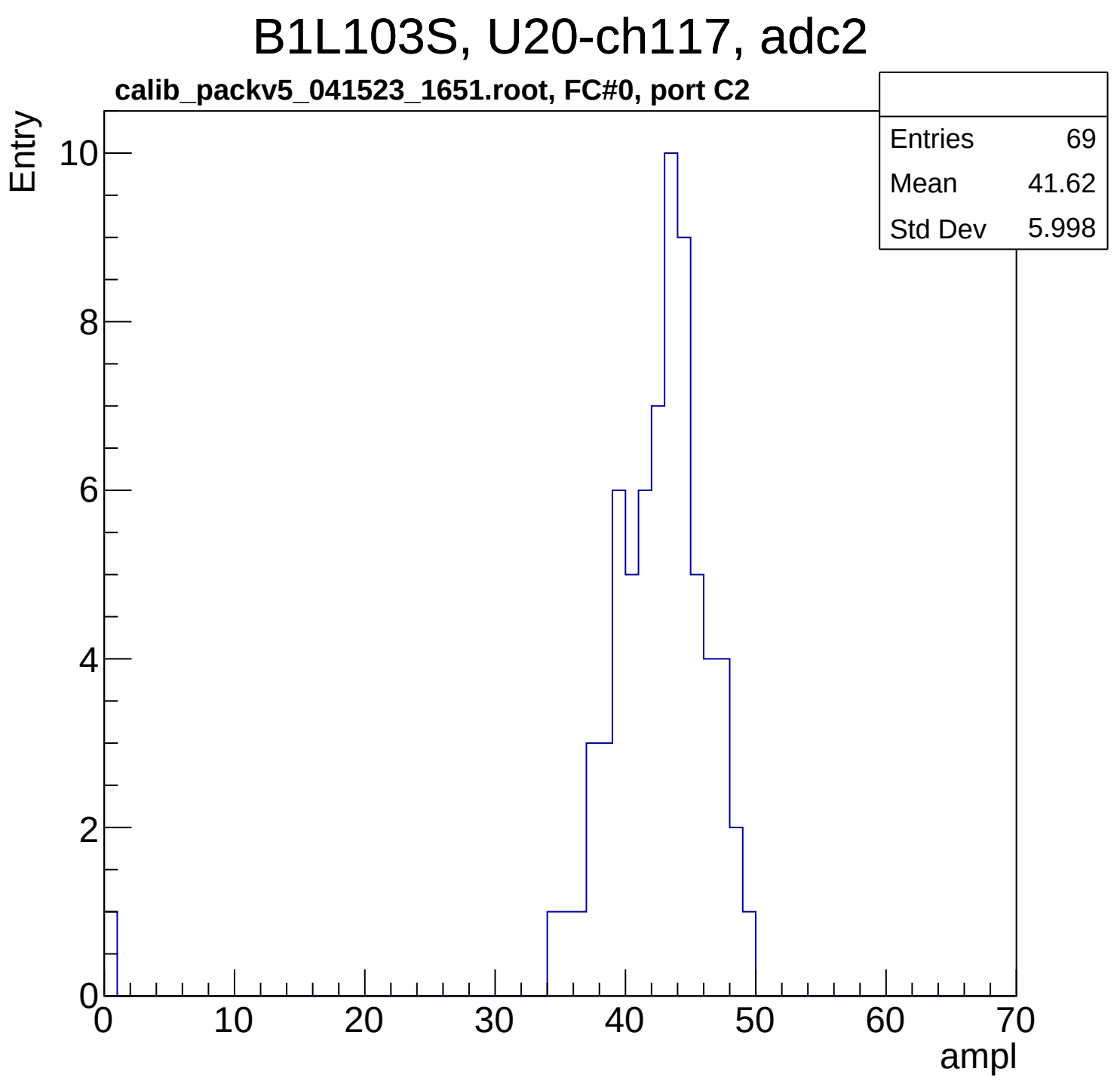
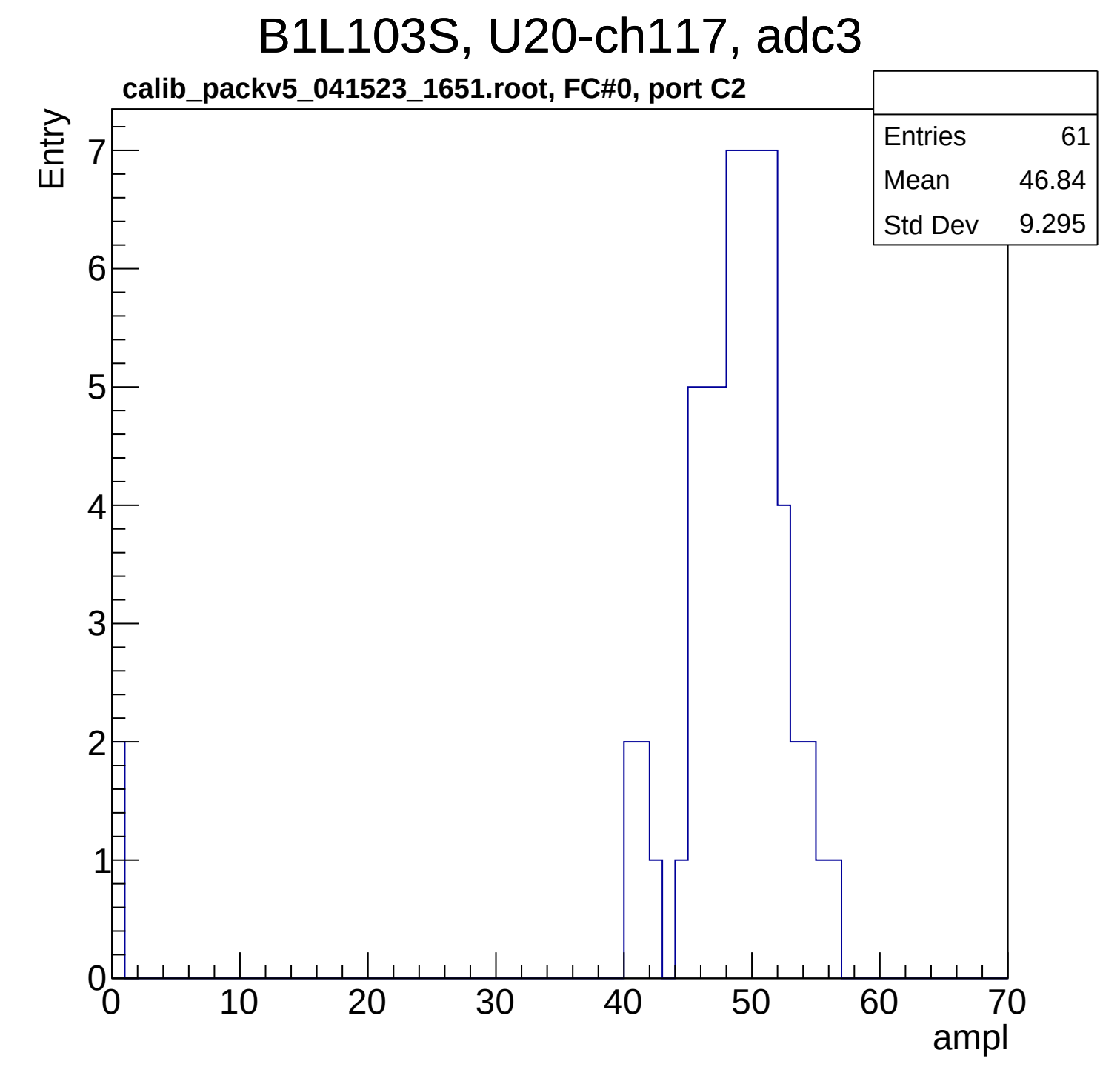
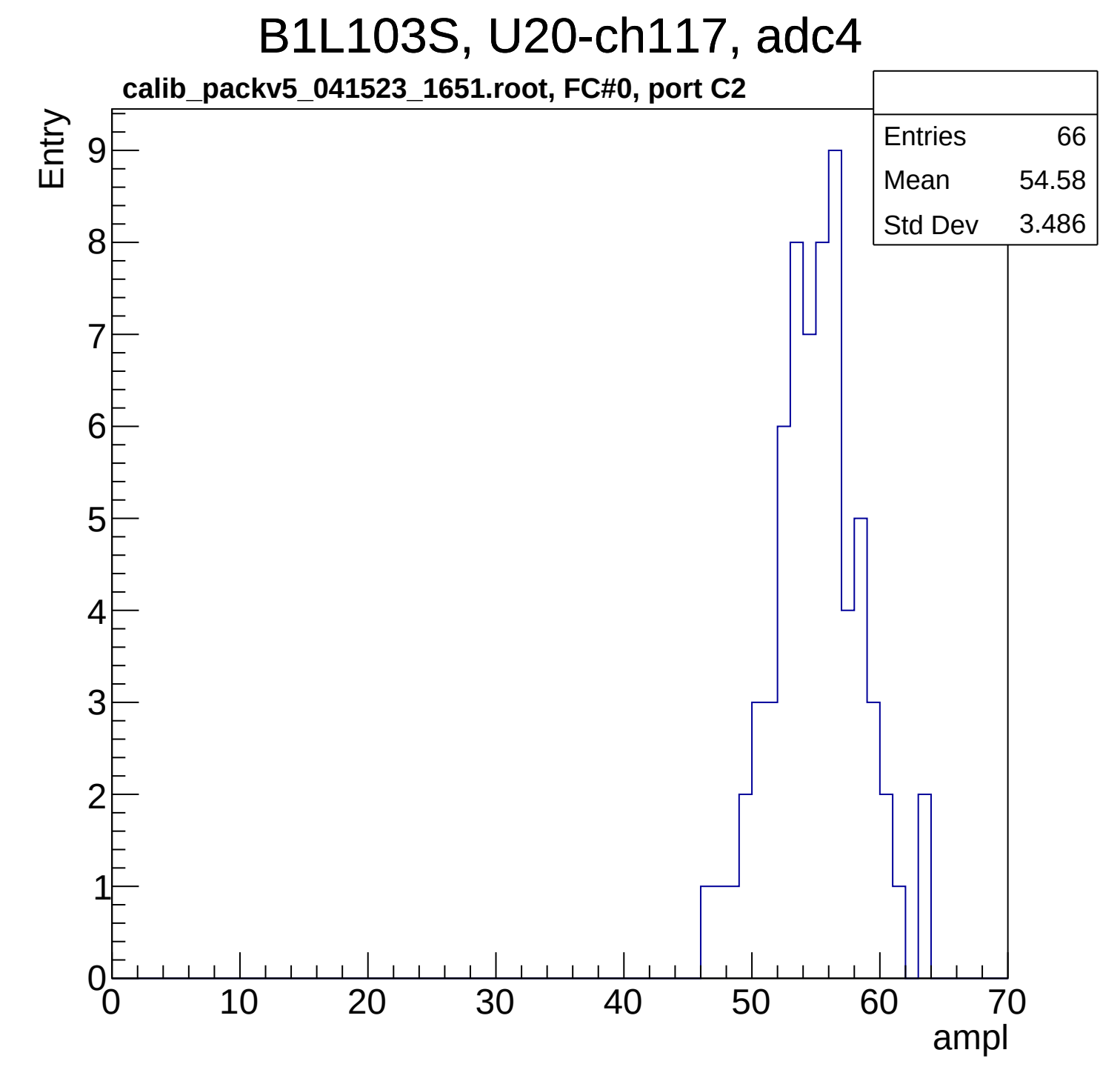
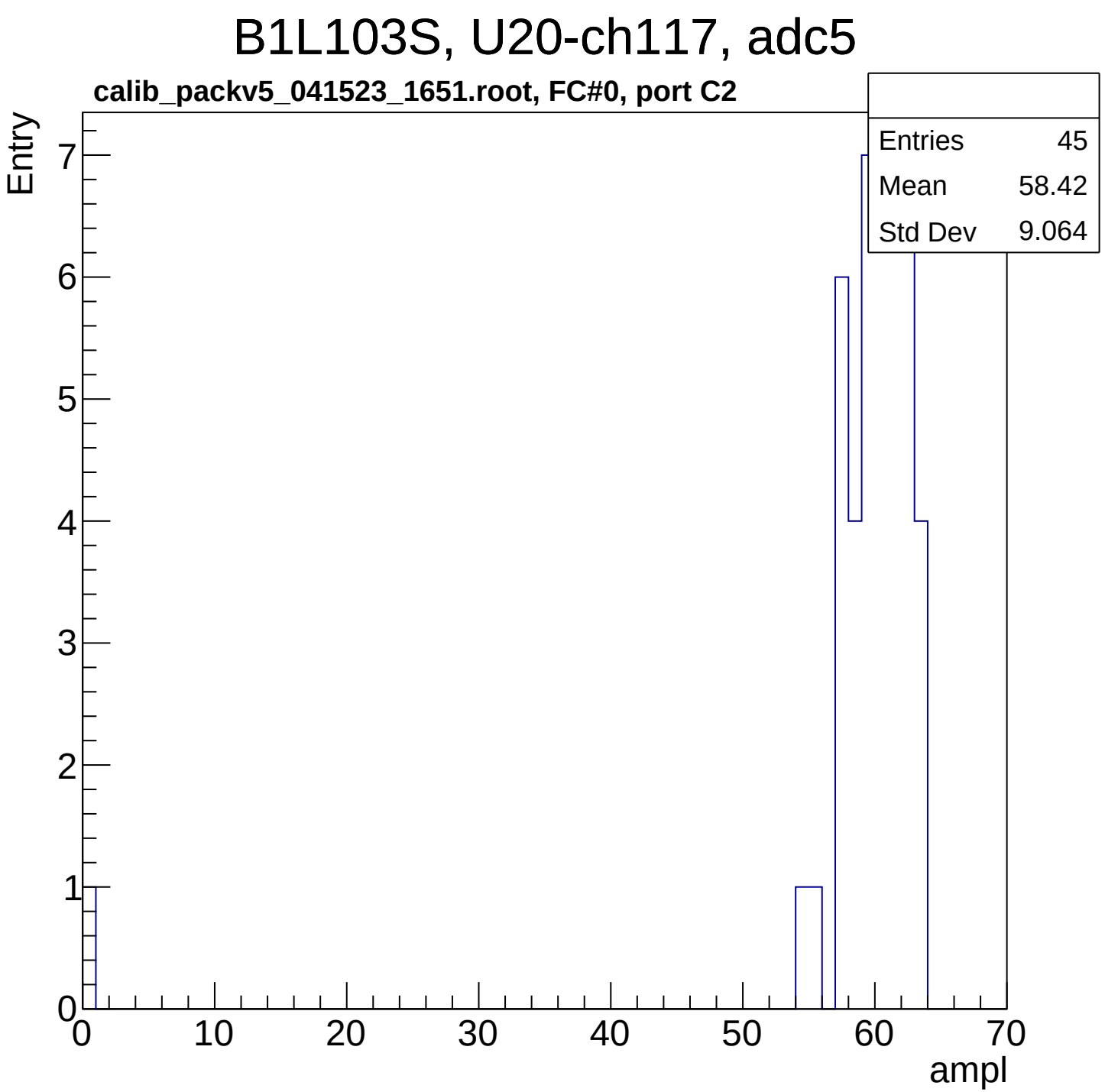
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70


B1L103S, U20-ch117, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 29.73
Std Dev 13.4
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U20-ch117, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 41.62
Std Dev 5.998
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U20-ch117, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 46.84
Std Dev 9.295
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U20-ch117, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 54.58
Std Dev 3.486
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch117, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 58.42
Std Dev 9.064
Entry
ampl
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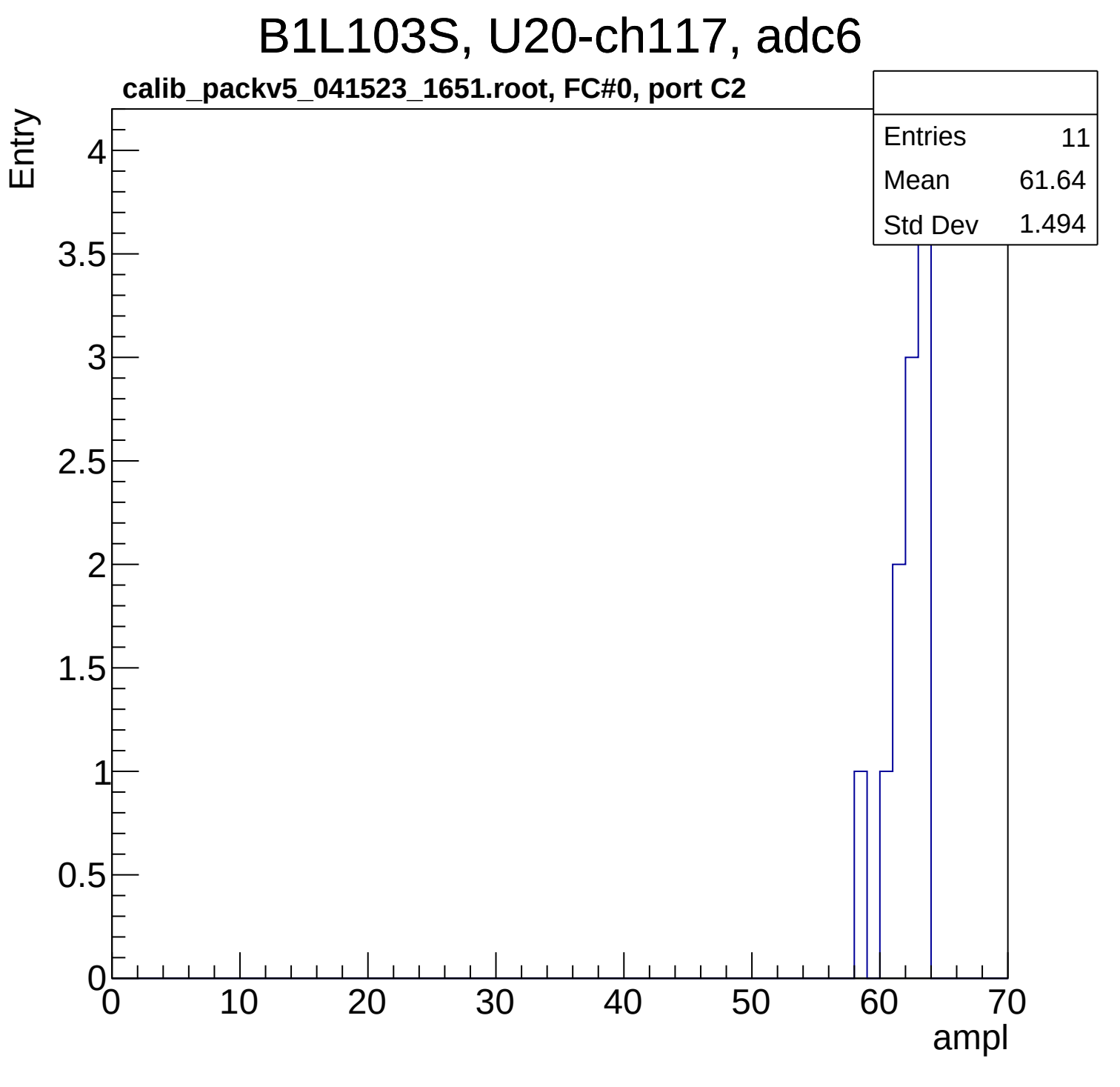
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U20-ch117, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 61.64
Std Dev 1.494
Entry
ampl
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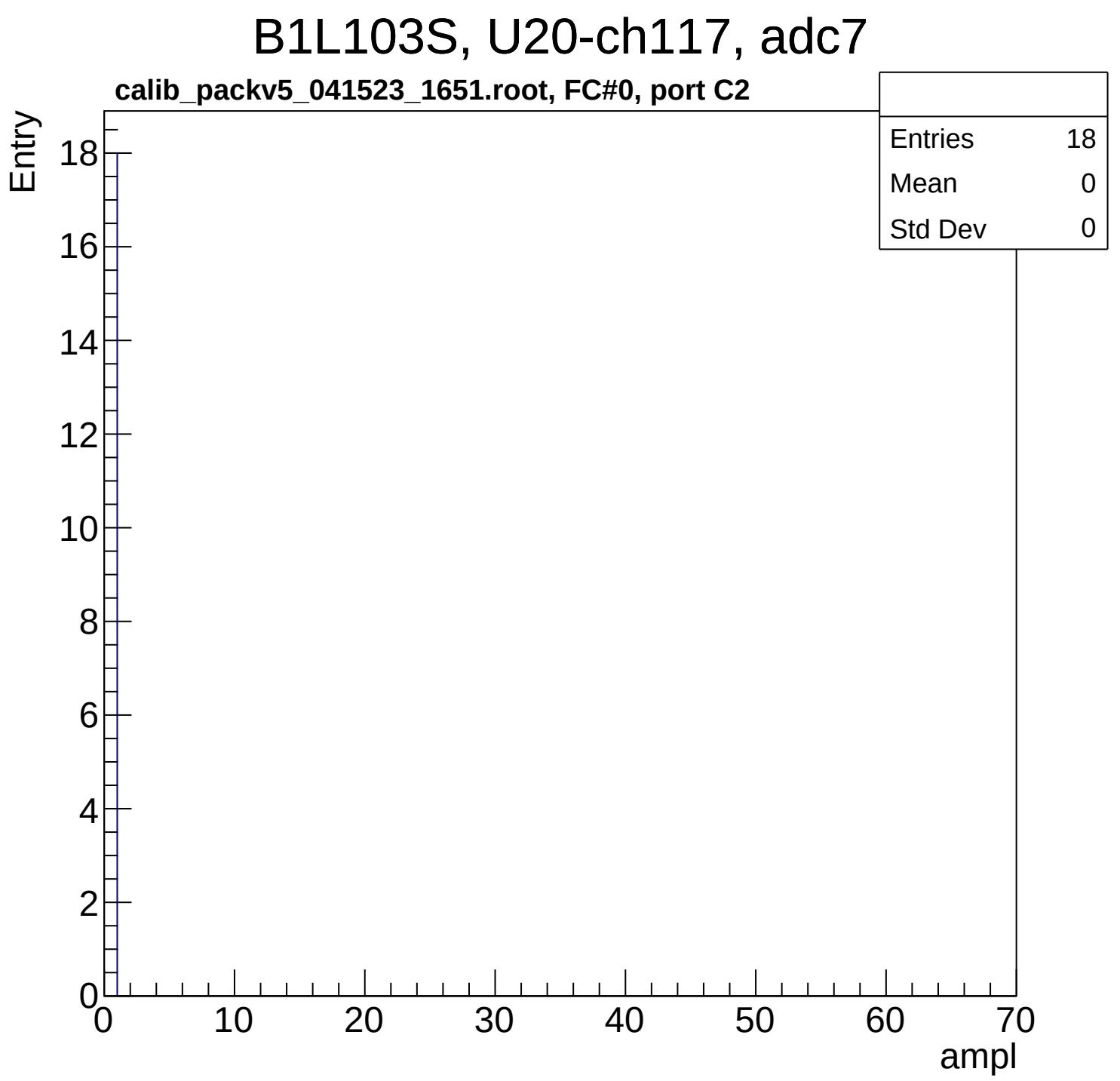
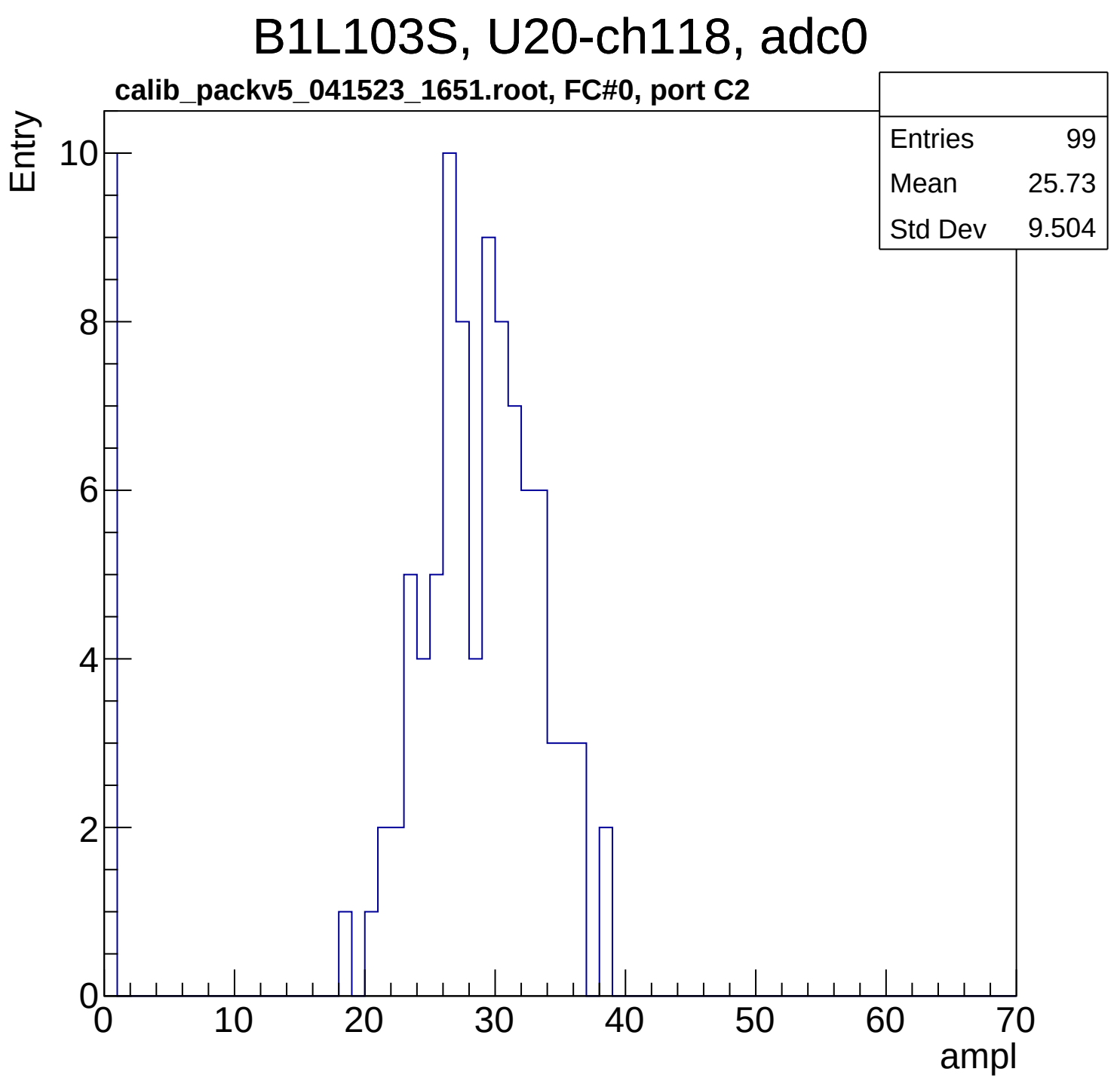
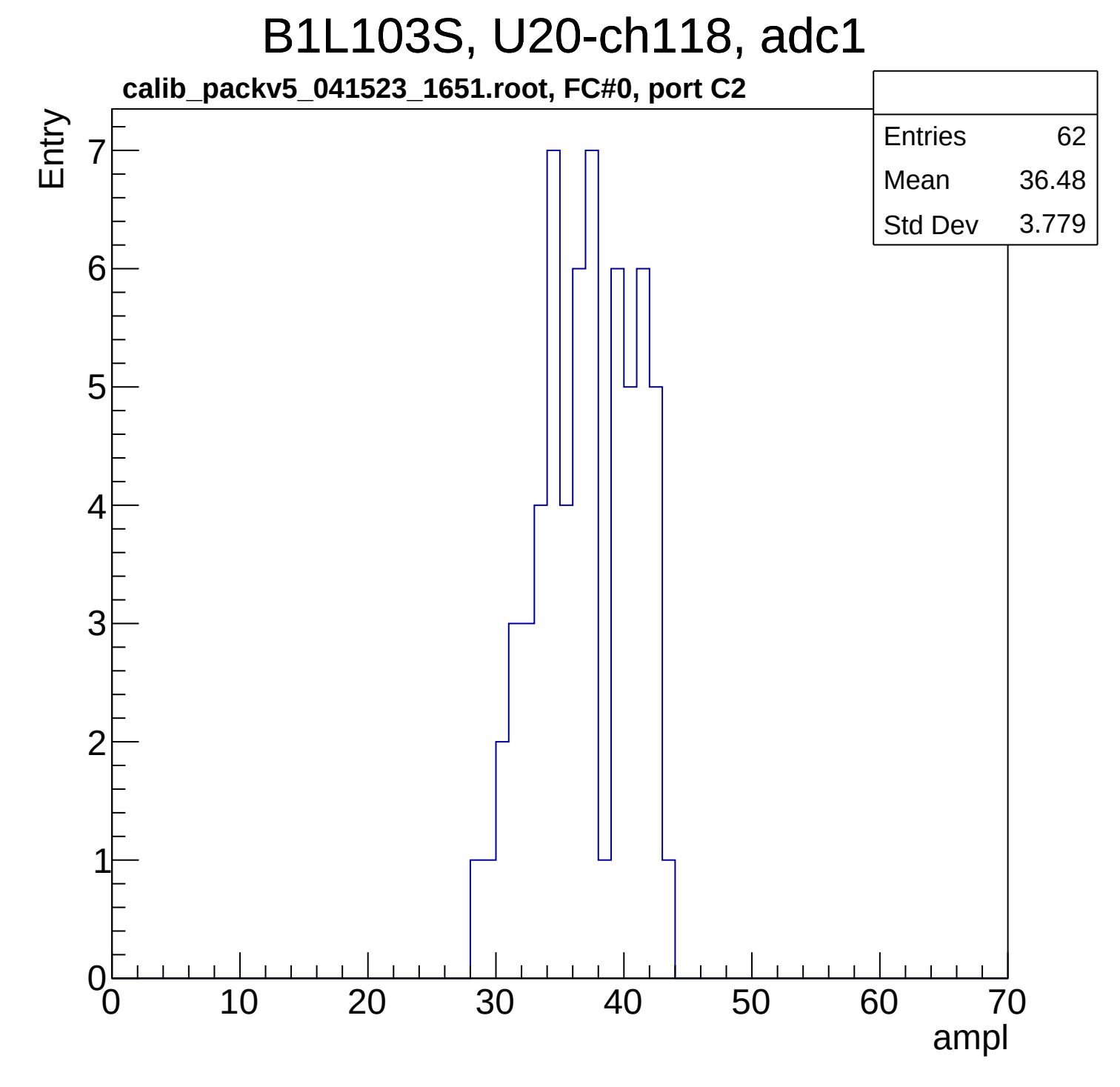
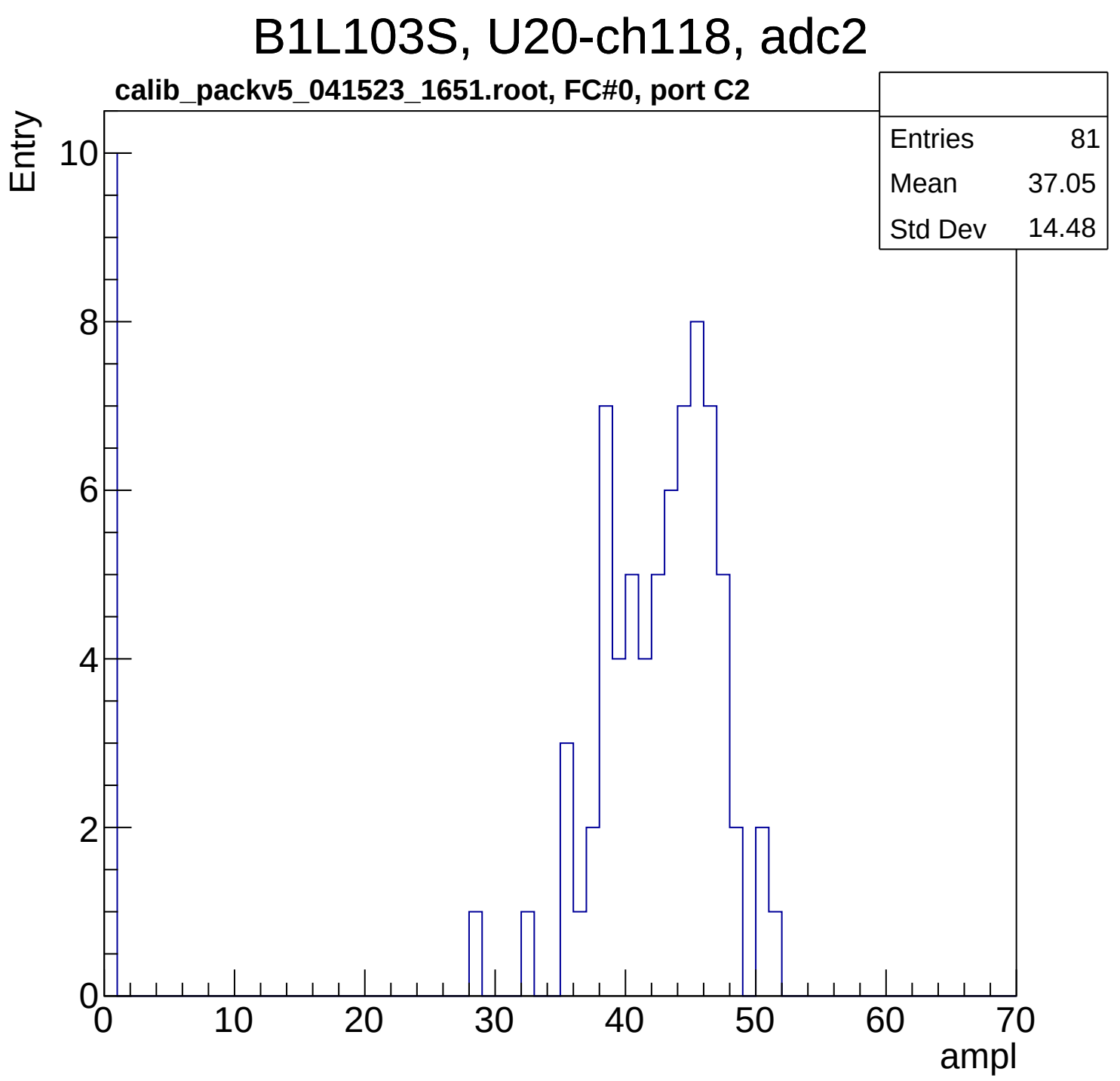
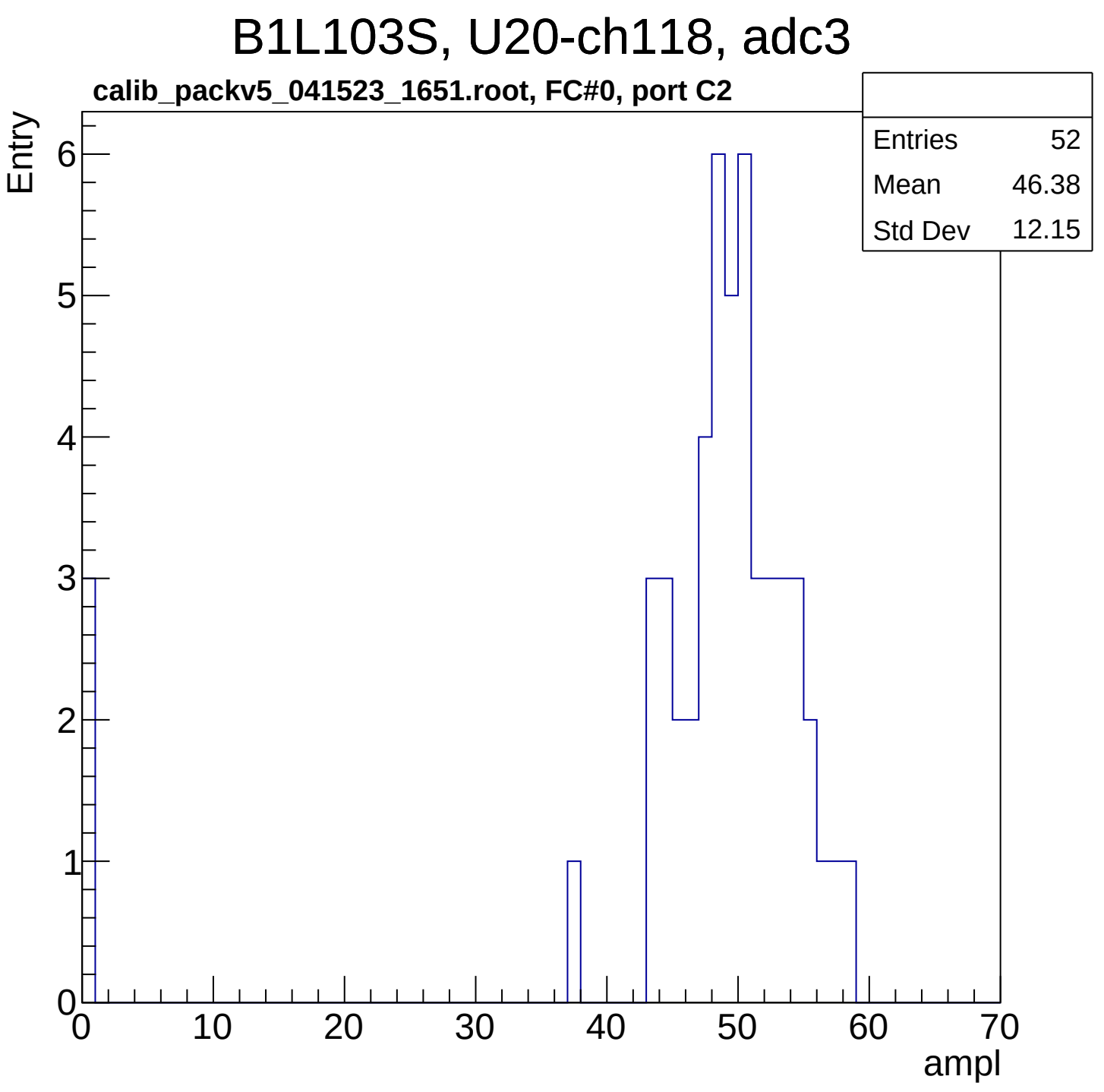
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

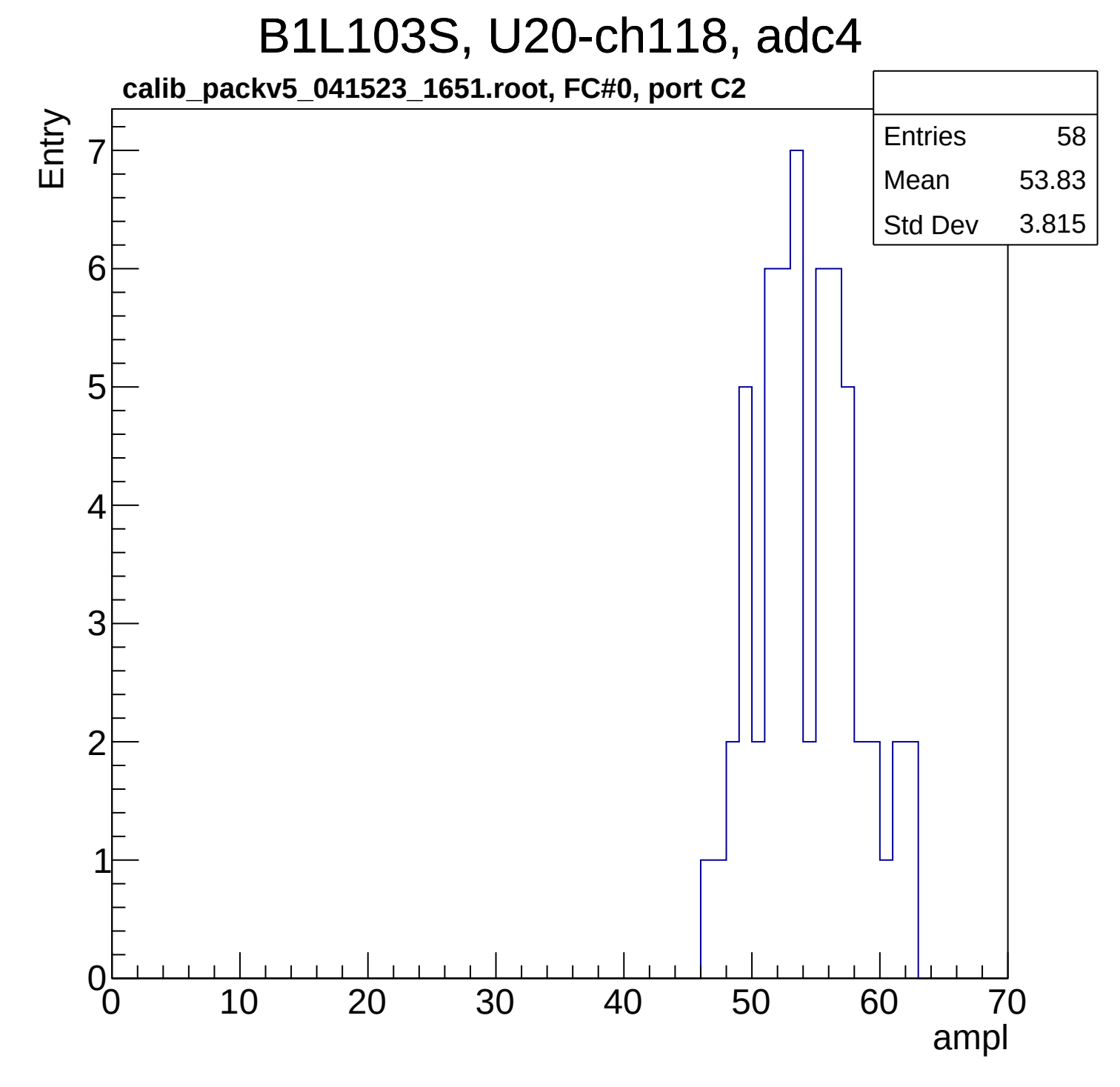

B1L103S, U20-ch117, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch118, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 25.73
Std Dev 9.504
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U20-ch118, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 36.48
Std Dev 3.779
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U20-ch118, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 37.05
Std Dev 14.48
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U20-ch118, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 46.38
Std Dev 12.15
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch118, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 53.83
Std Dev 3.815
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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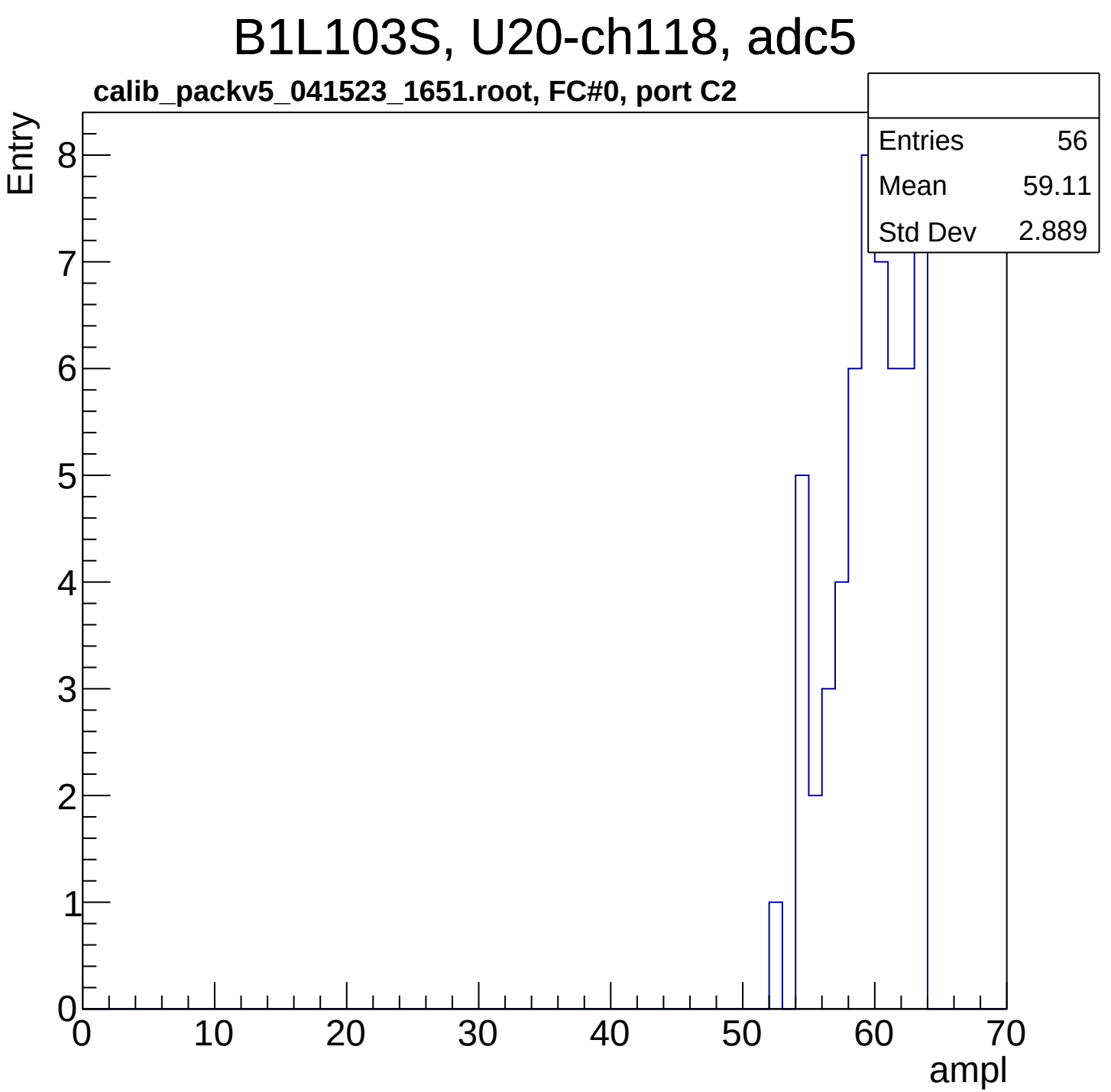
40
50
60
70


B1L103S, U20-ch118, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 59.11
Std Dev 2.889
Entry
ampl
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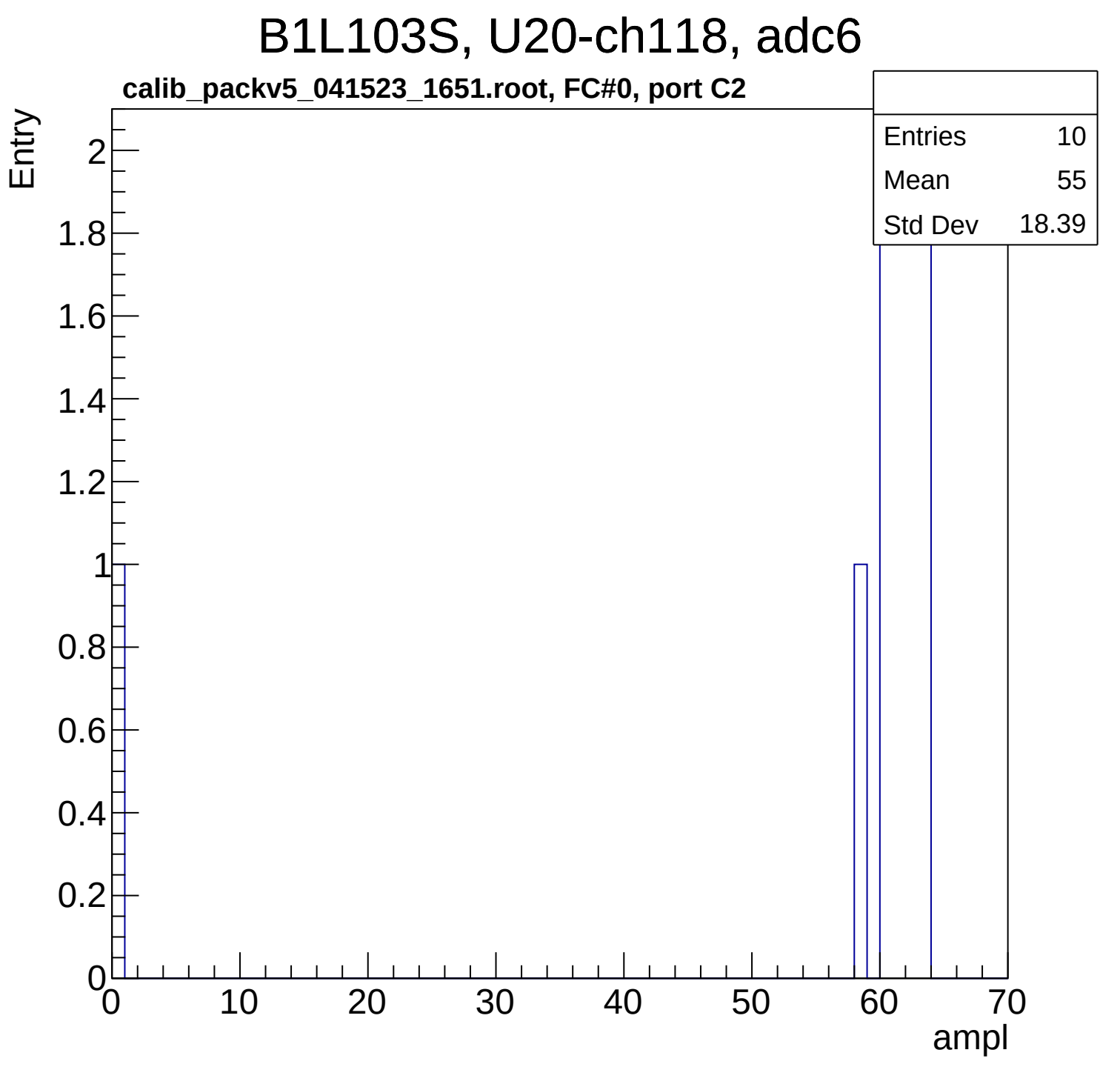
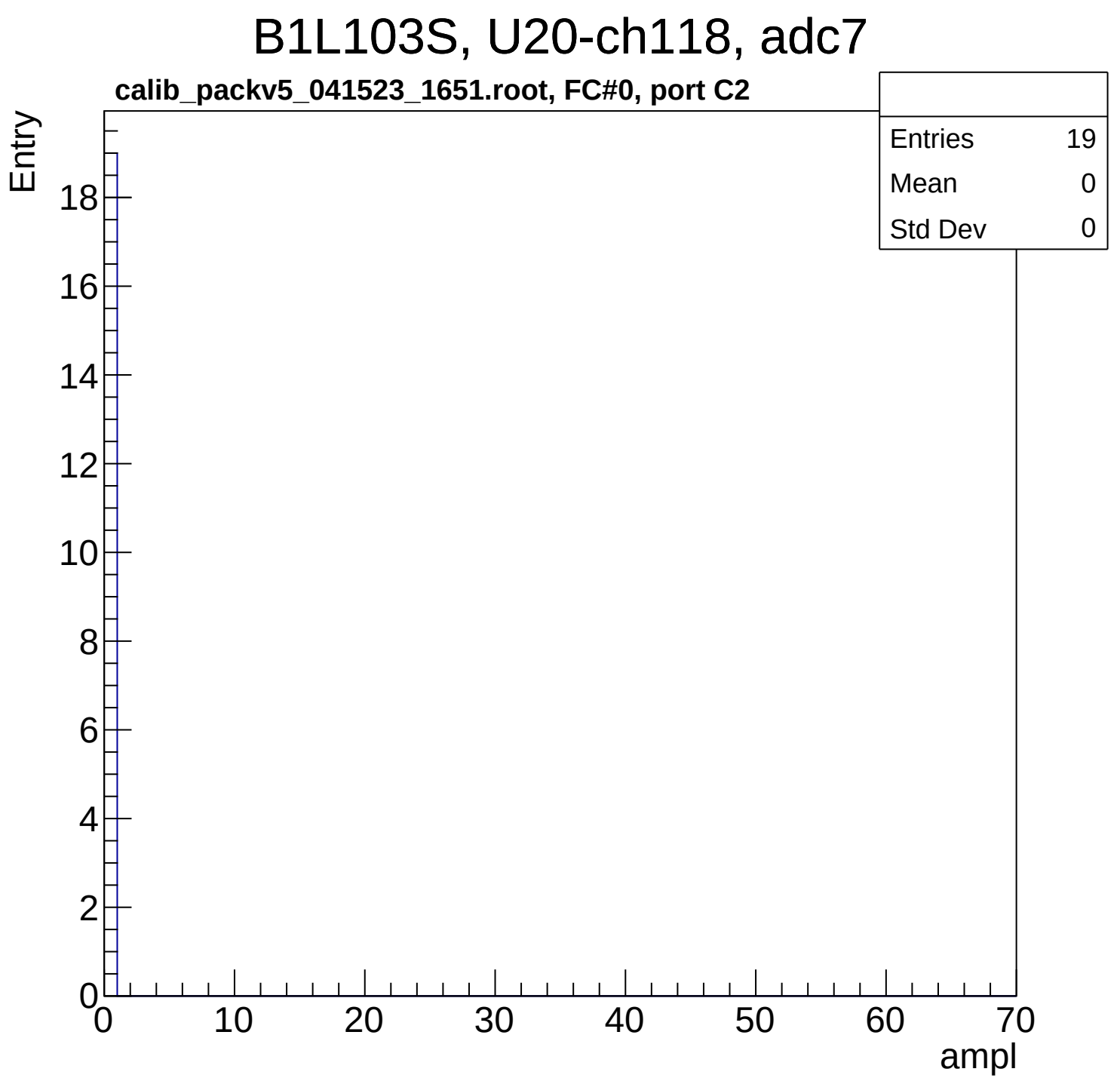
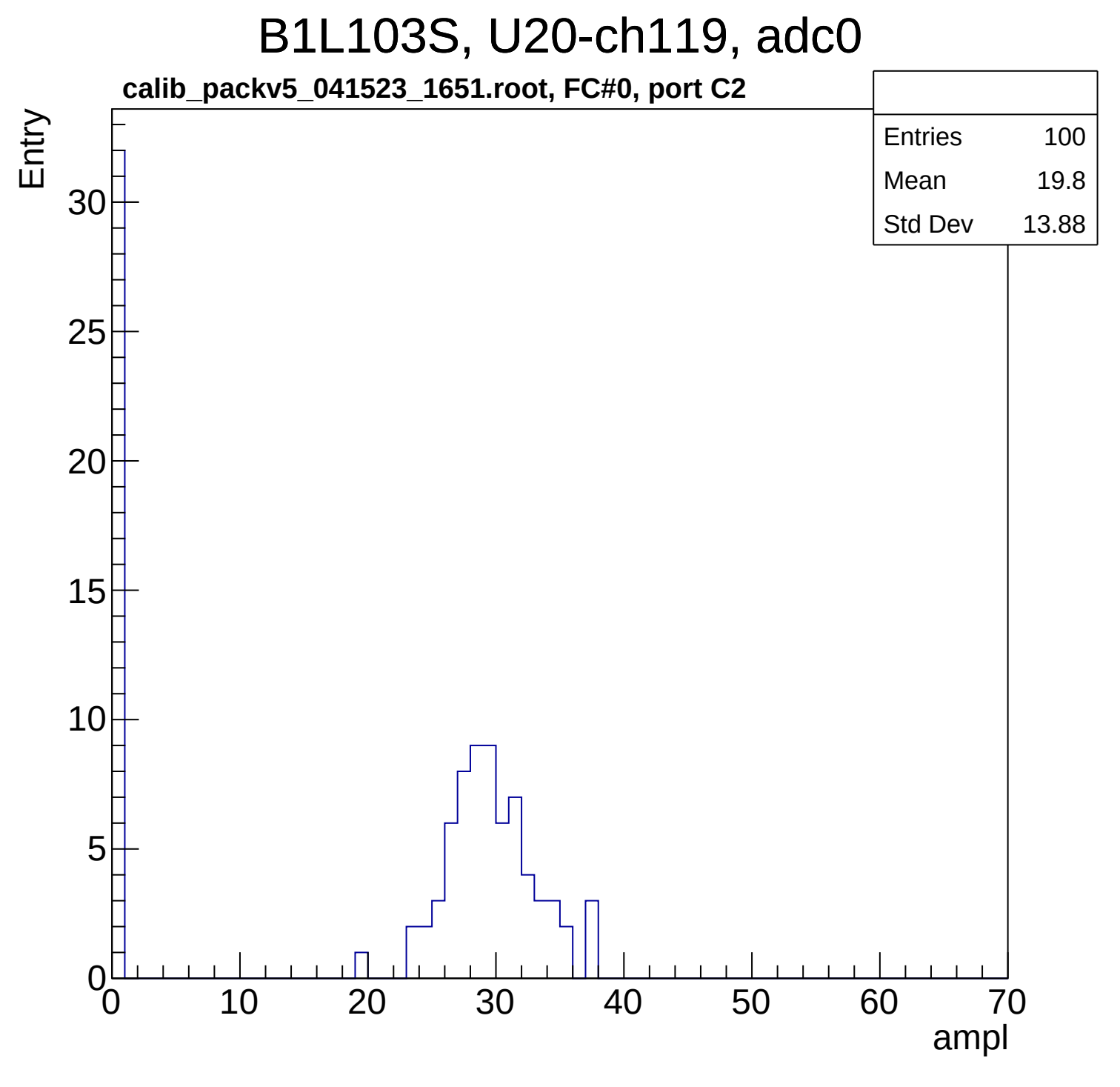
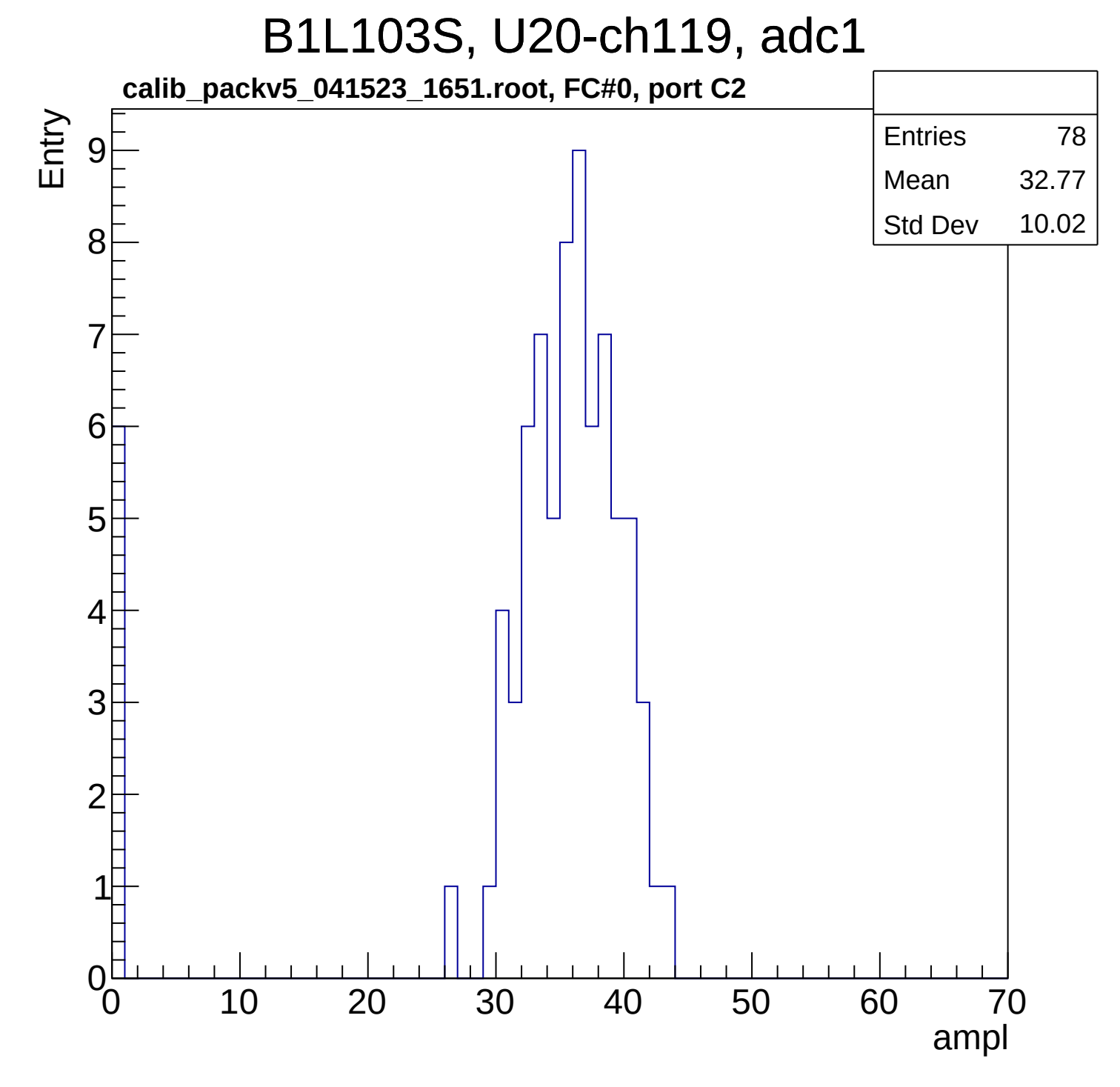
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch118, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 55
Std Dev 18.39
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U20-ch118, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch119, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 100
Mean 19.8
Std Dev 13.88
Entry
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch119, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 32.77
Std Dev 10.02
Entry
ampl
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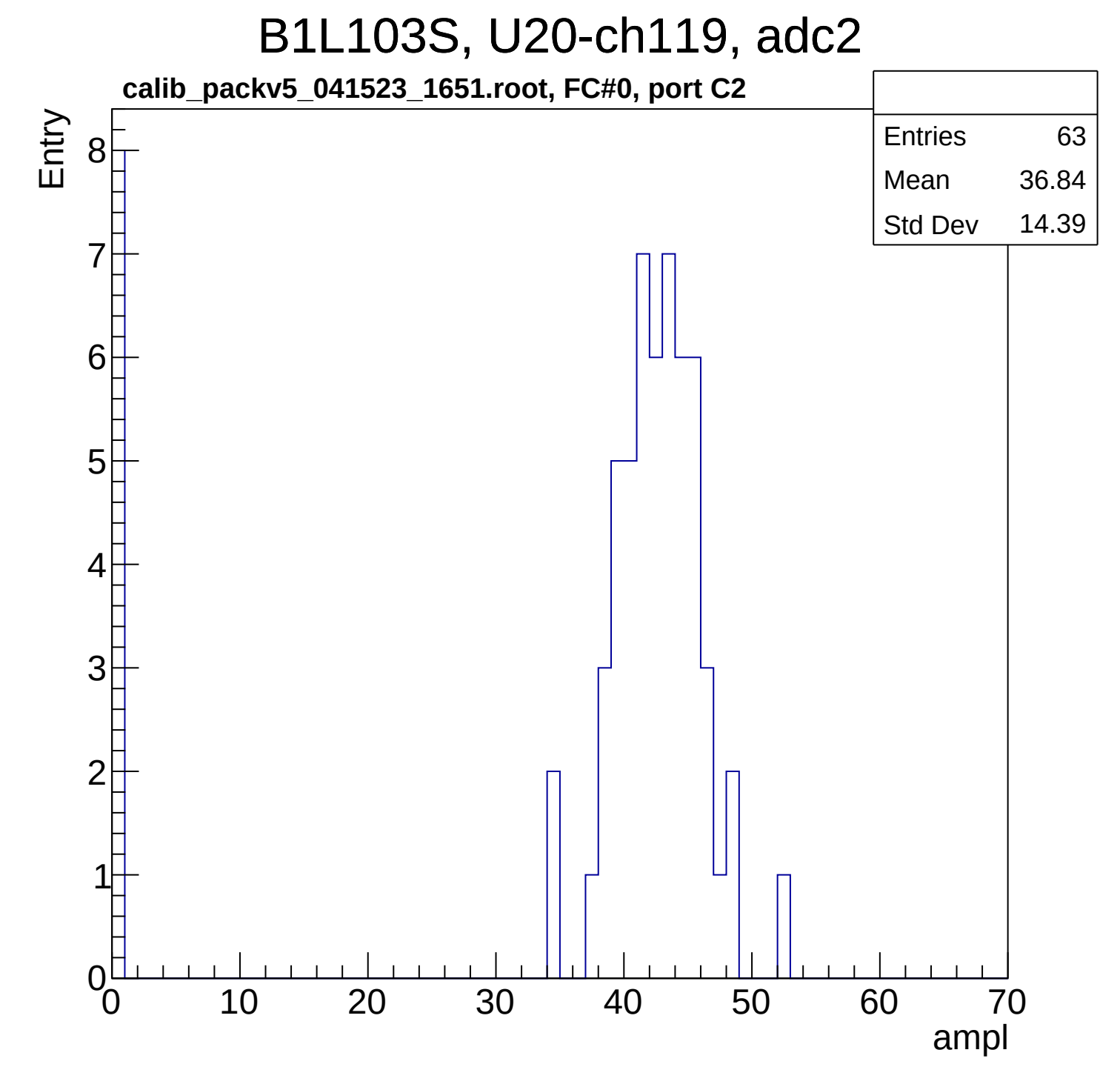
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch119, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 36.84
Std Dev 14.39
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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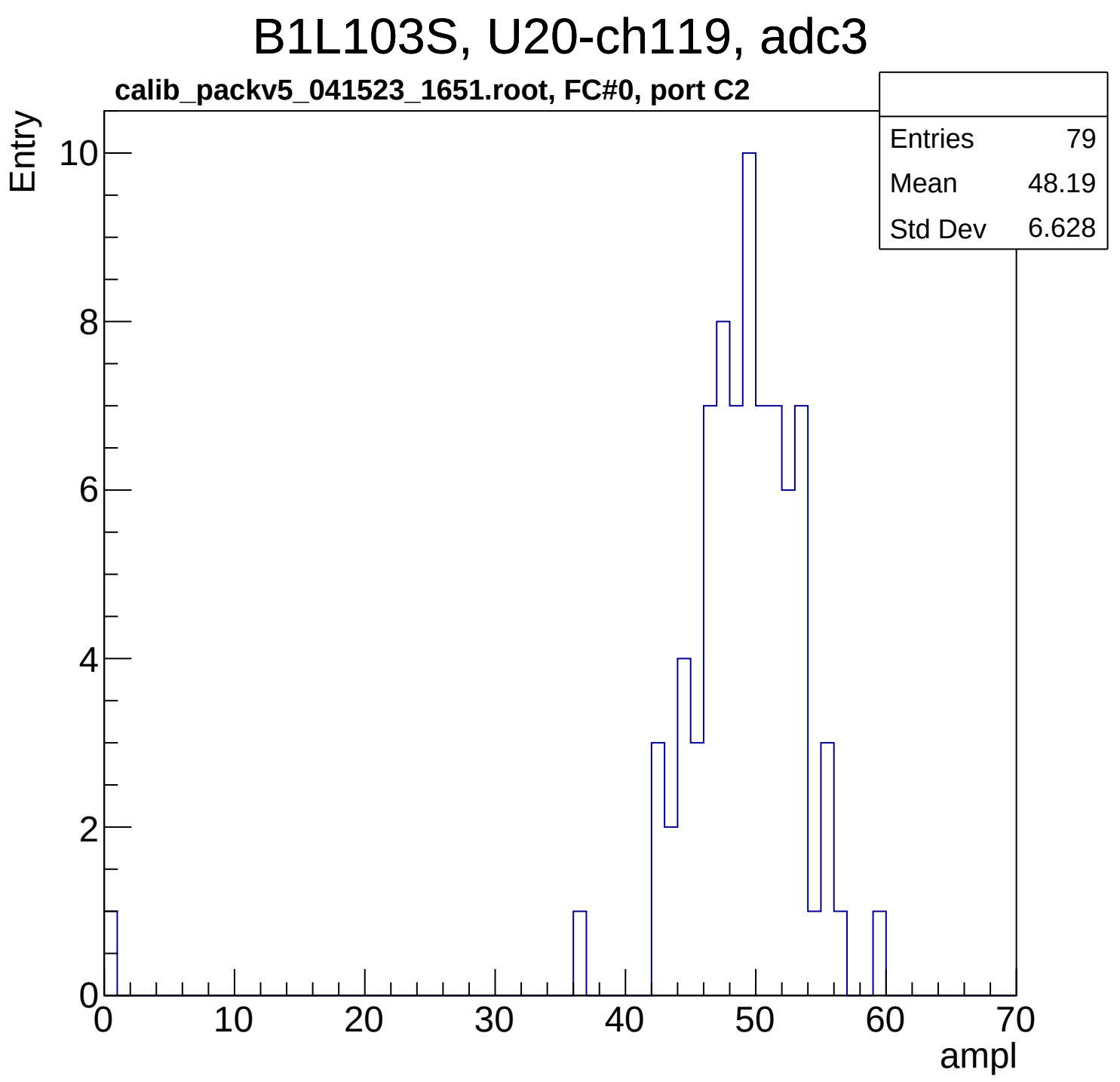
B1L103S, U20-ch119, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 48.19
Std Dev 6.628
Entry
ampl
0
2
4
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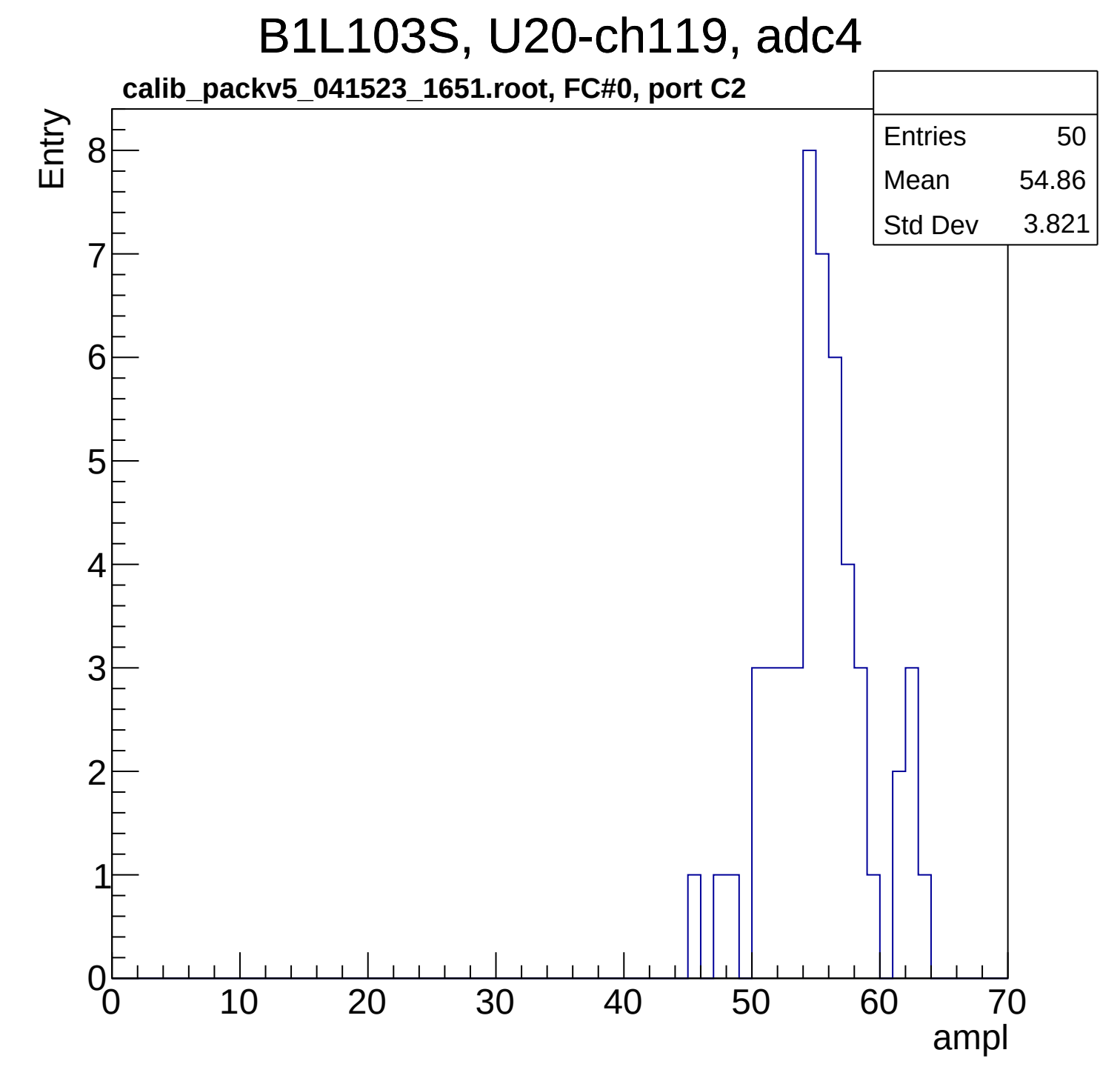
30
40
50
60
70


B1L103S, U20-ch119, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 54.86
Std Dev 3.821
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
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40
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60
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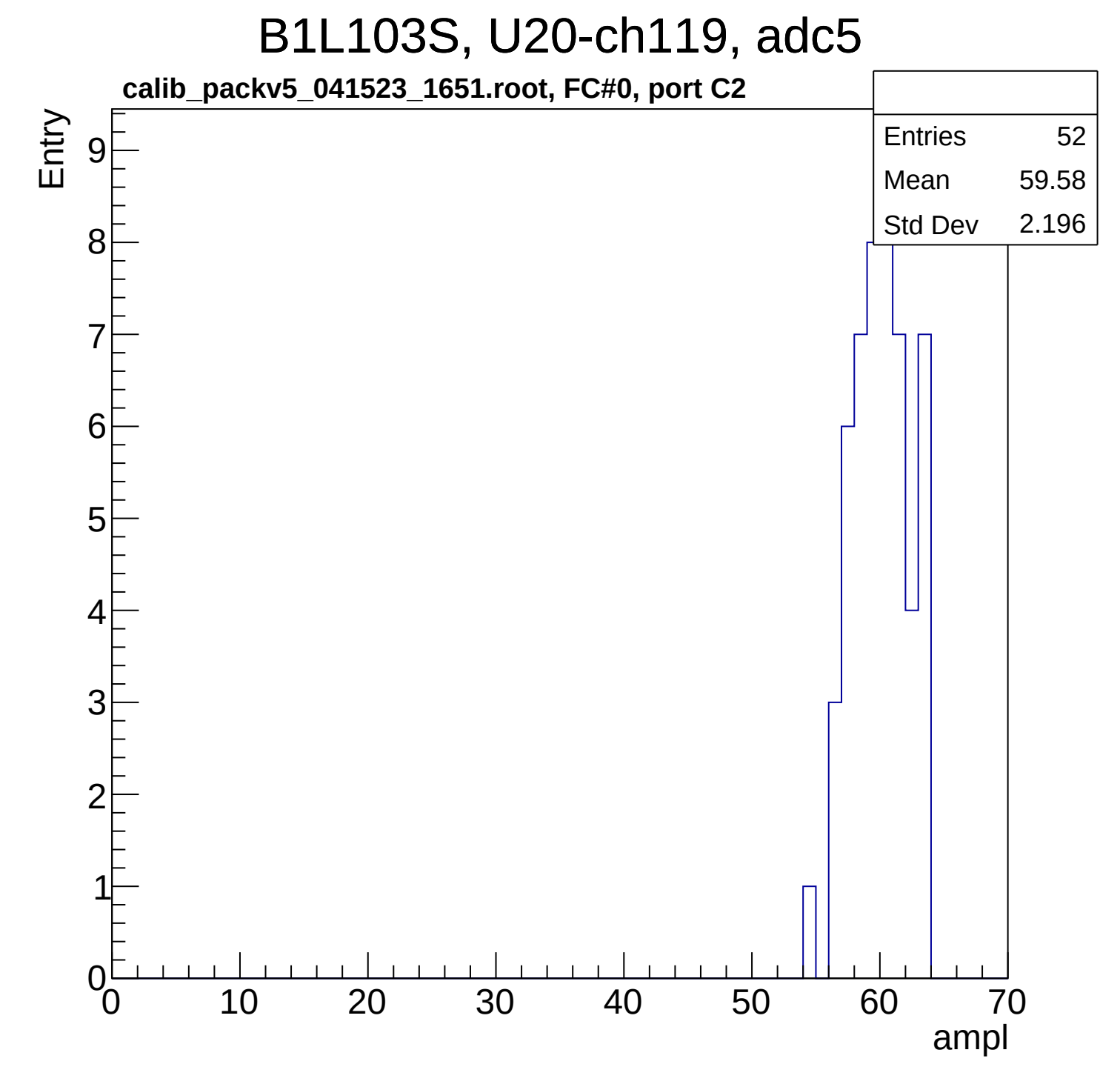
B1L103S, U20-ch119, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 59.58
Std Dev 2.196
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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40
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60
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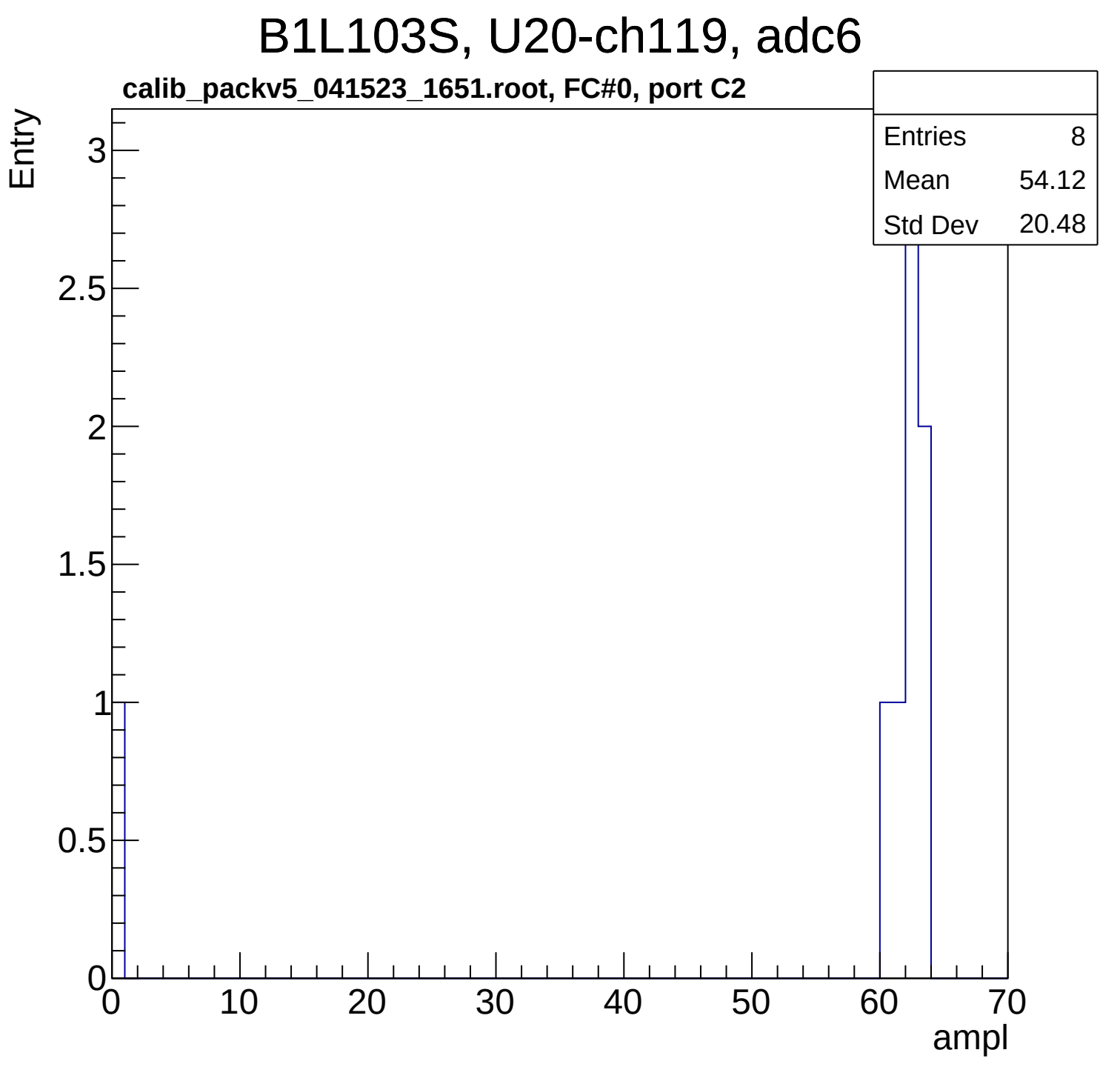
B1L103S, U20-ch119, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 54.12
Std Dev 20.48
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
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20
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40
50
60
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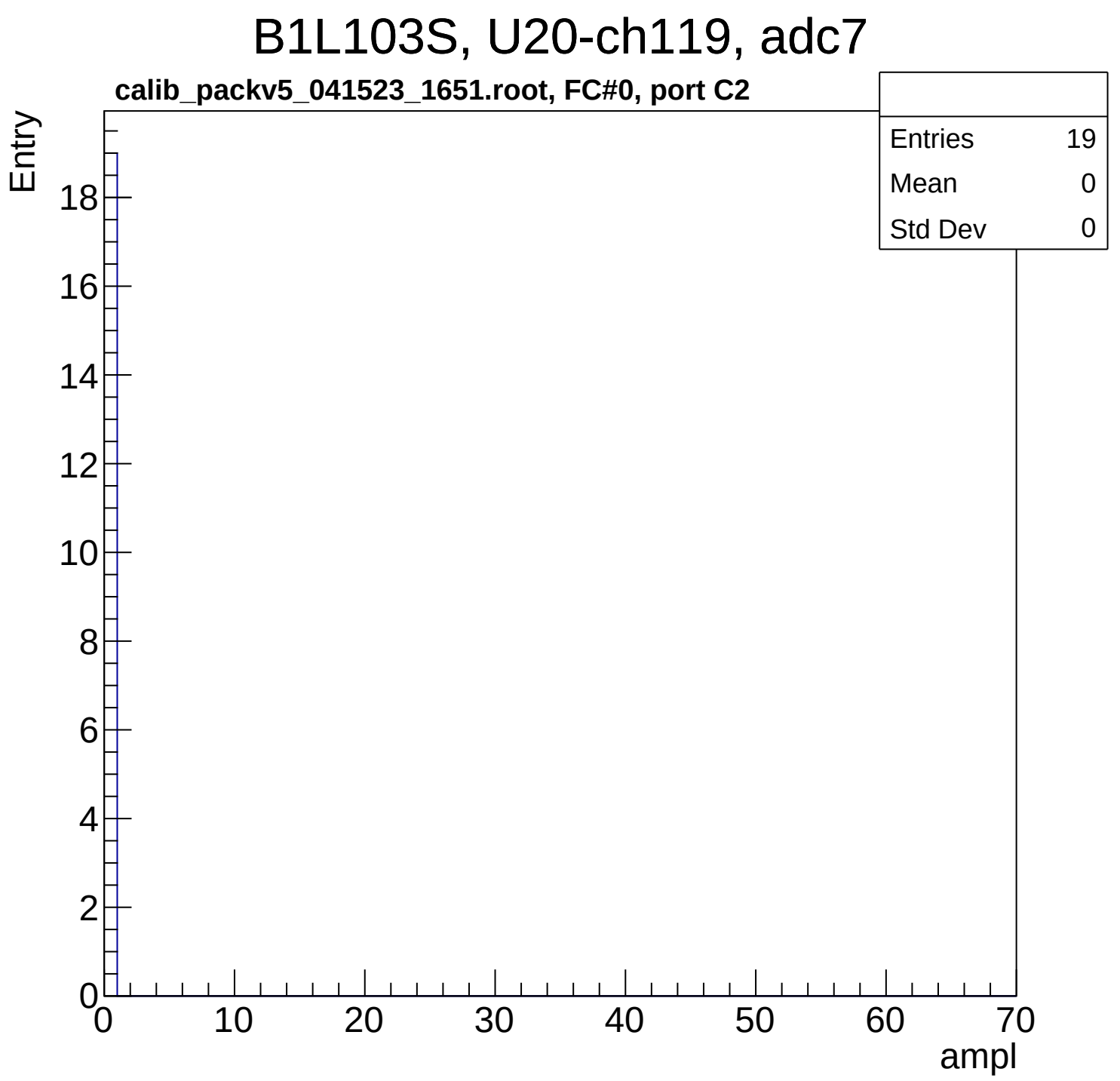
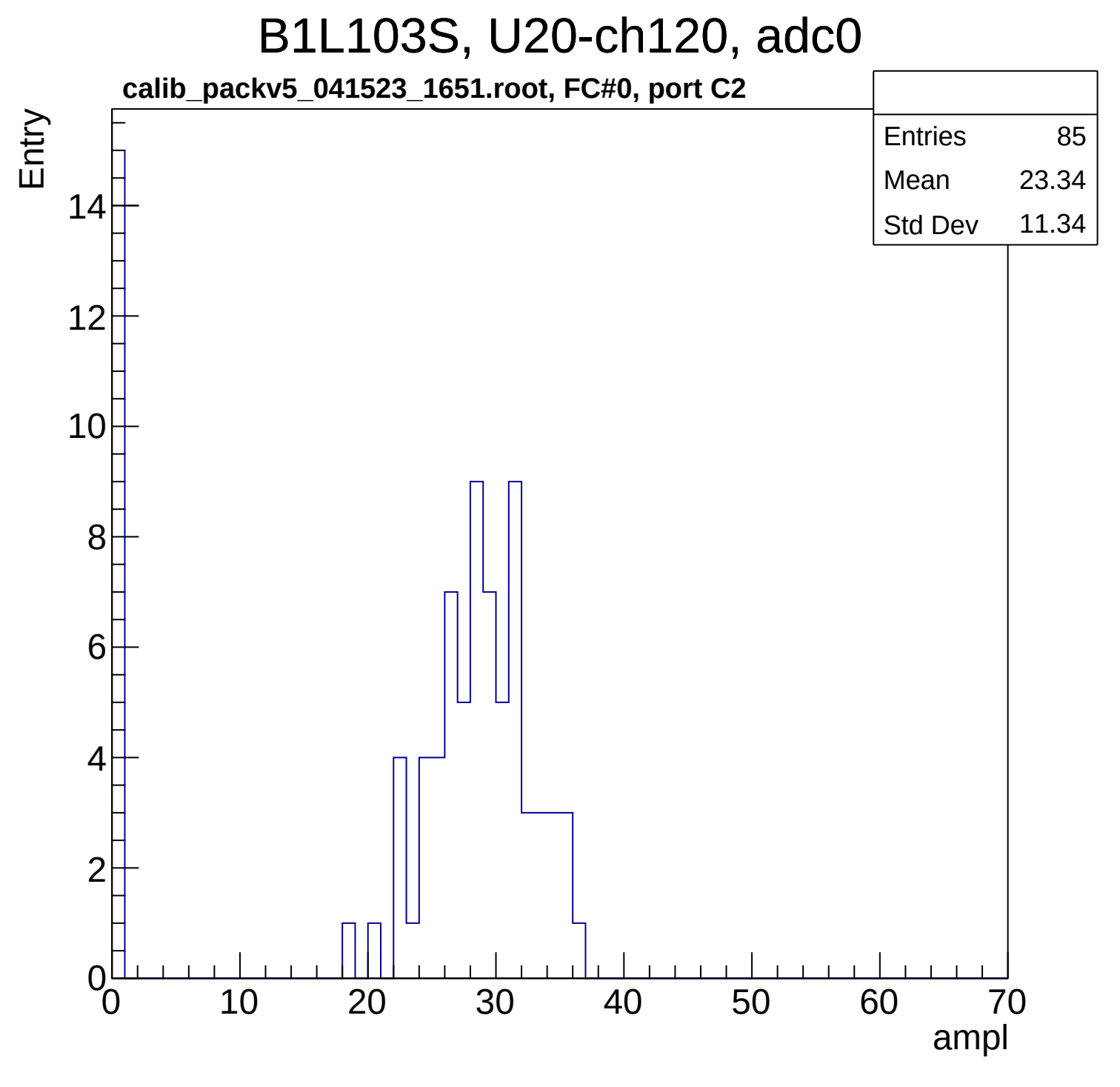

B1L103S, U20-ch119, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch120, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 23.34
Std Dev 11.34
Entry
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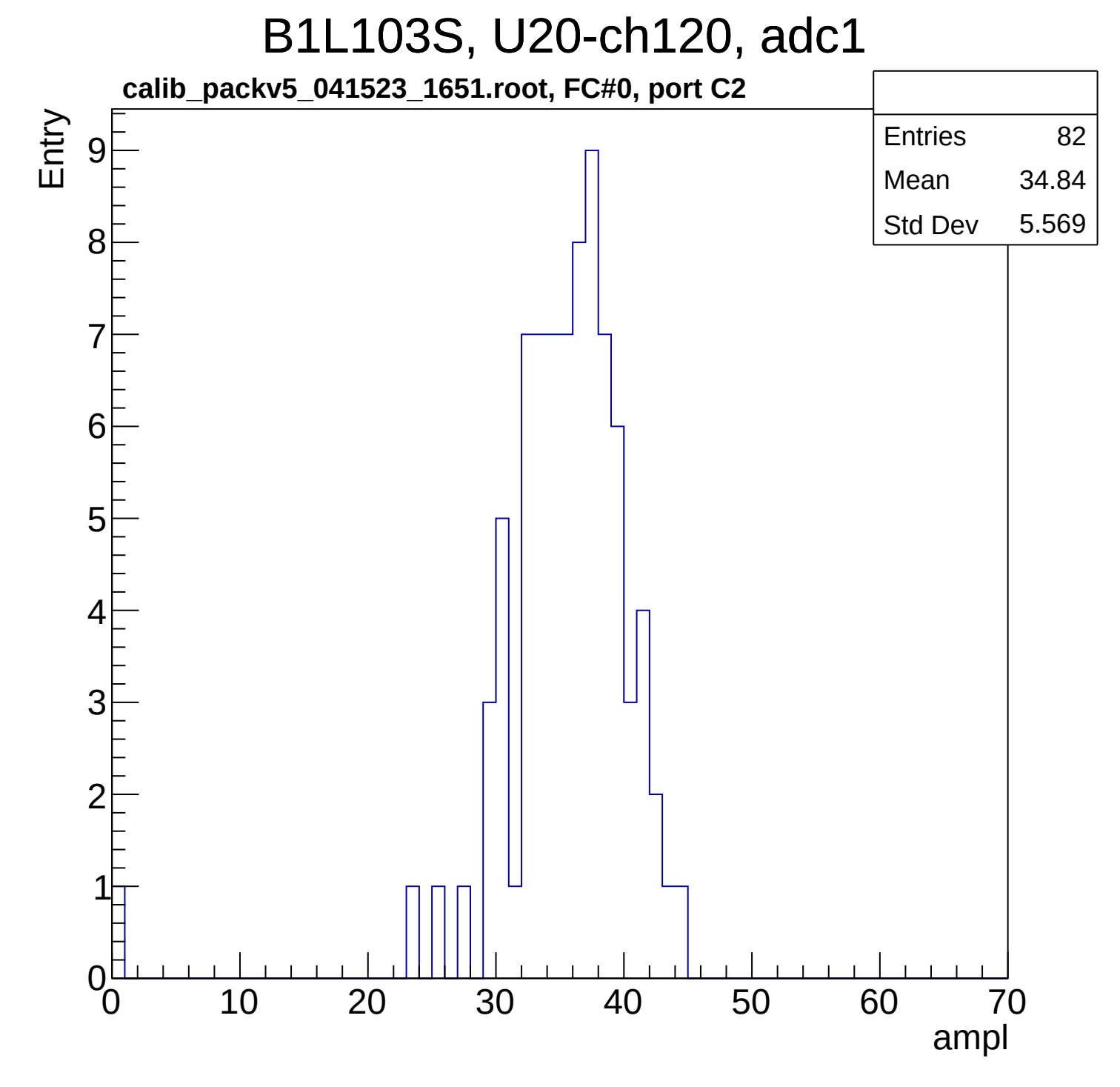
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch120, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 34.84
Std Dev 5.569
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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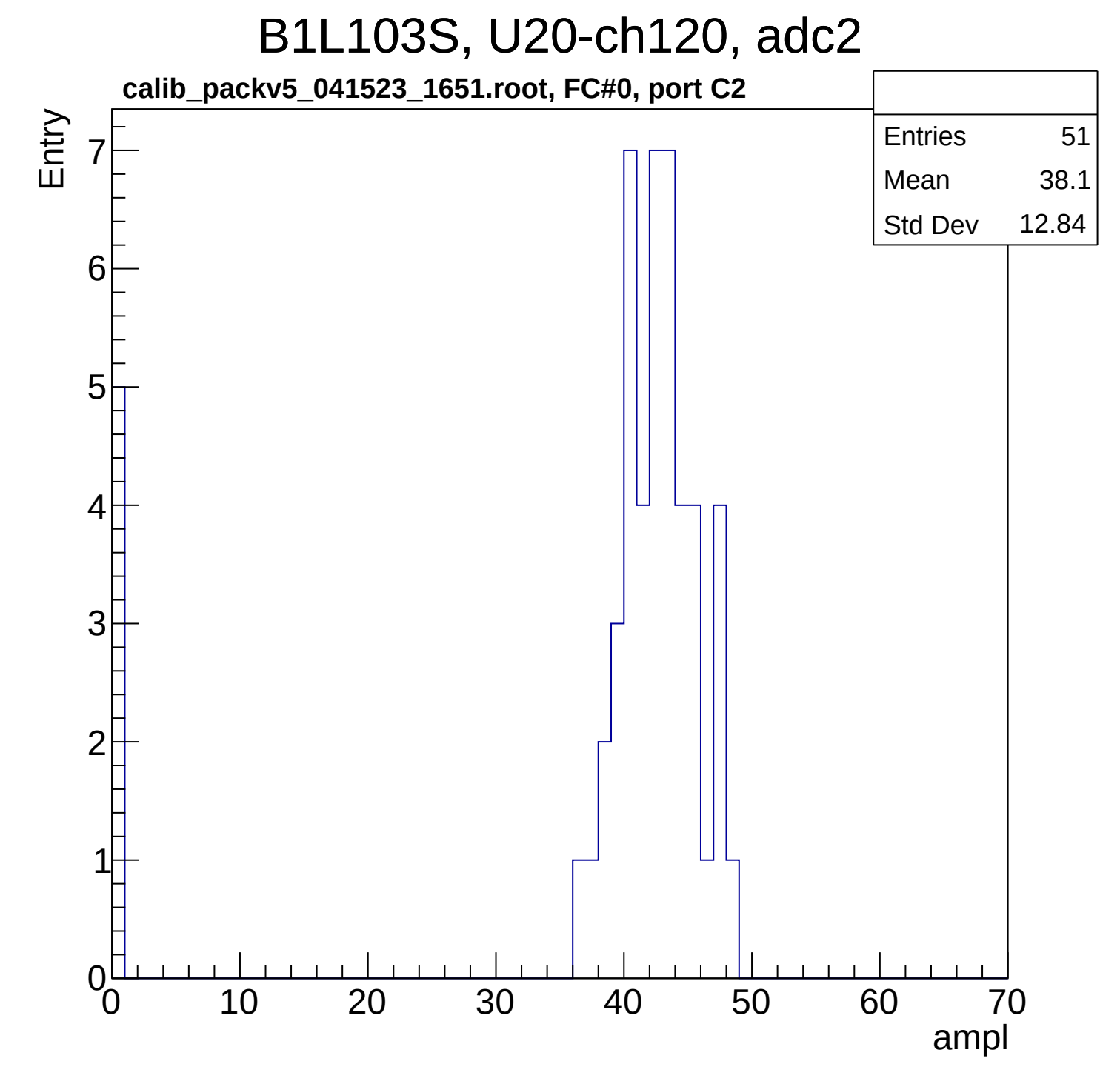
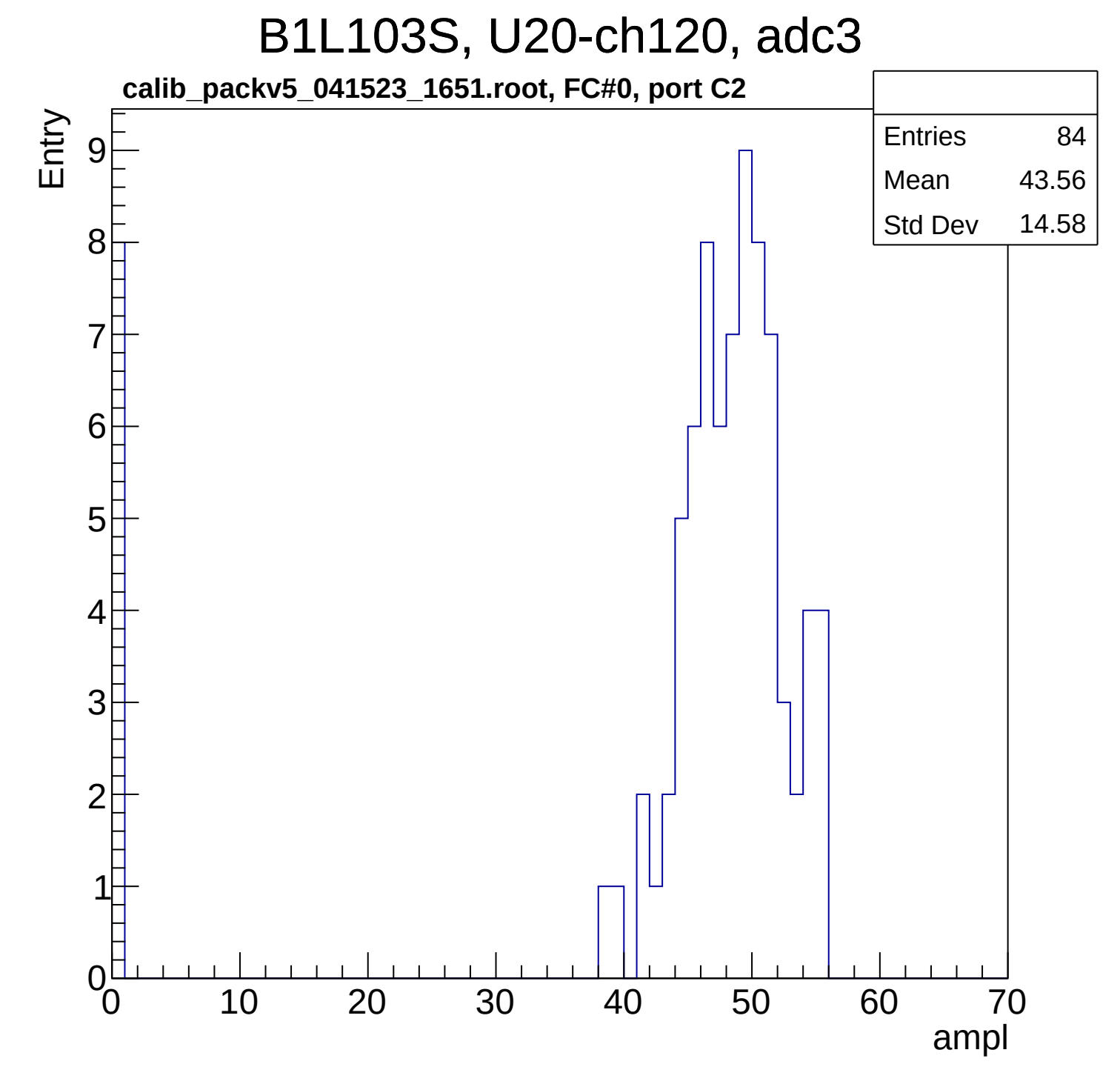

B1L103S, U20-ch120, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 38.1
Std Dev 12.84
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U20-ch120, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 43.56
Std Dev 14.58
Entry
ampl
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3
4
5
6
7
8
9
0
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40
50
60
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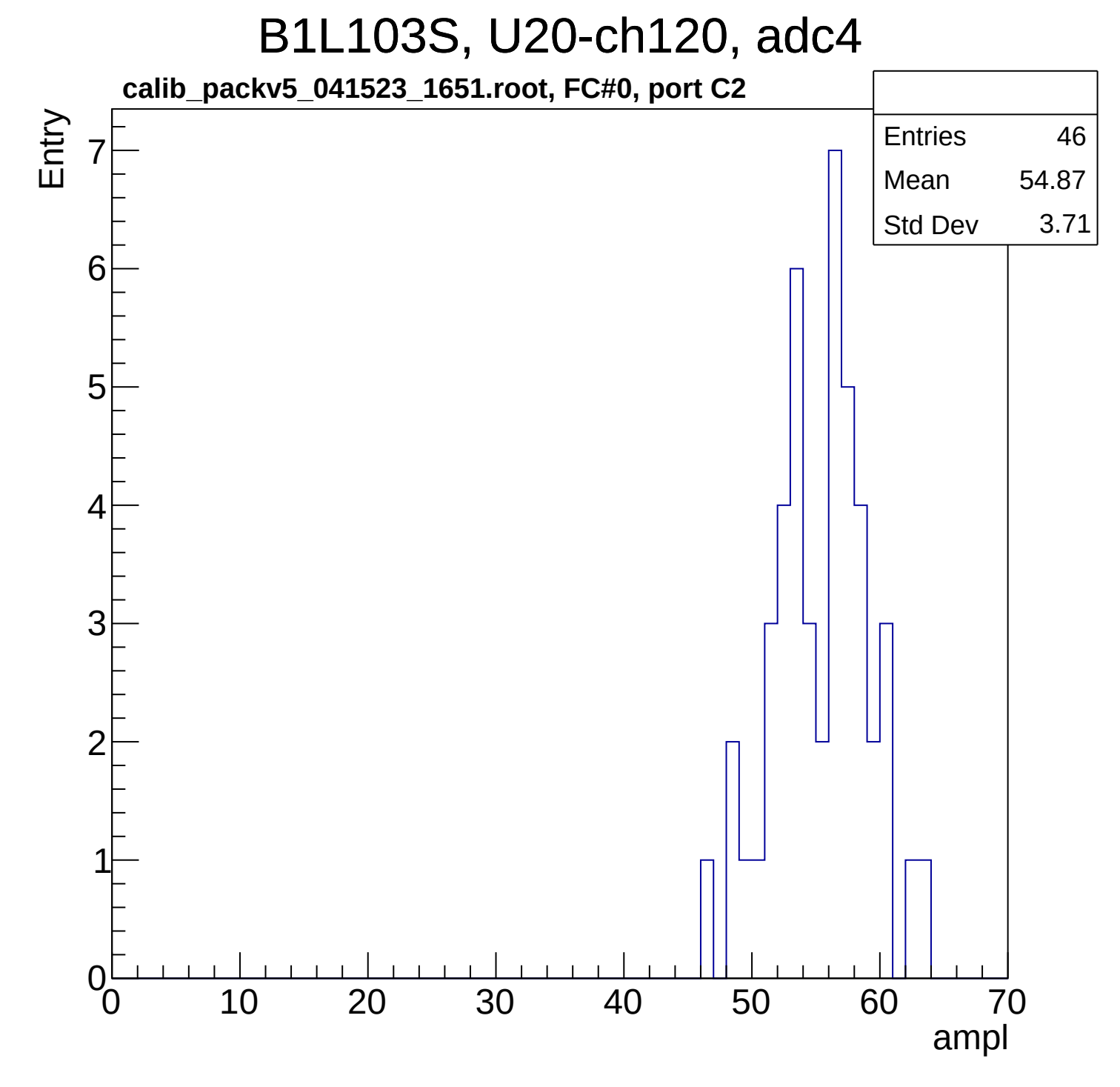
B1L103S, U20-ch120, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 54.87
Std Dev 3.71
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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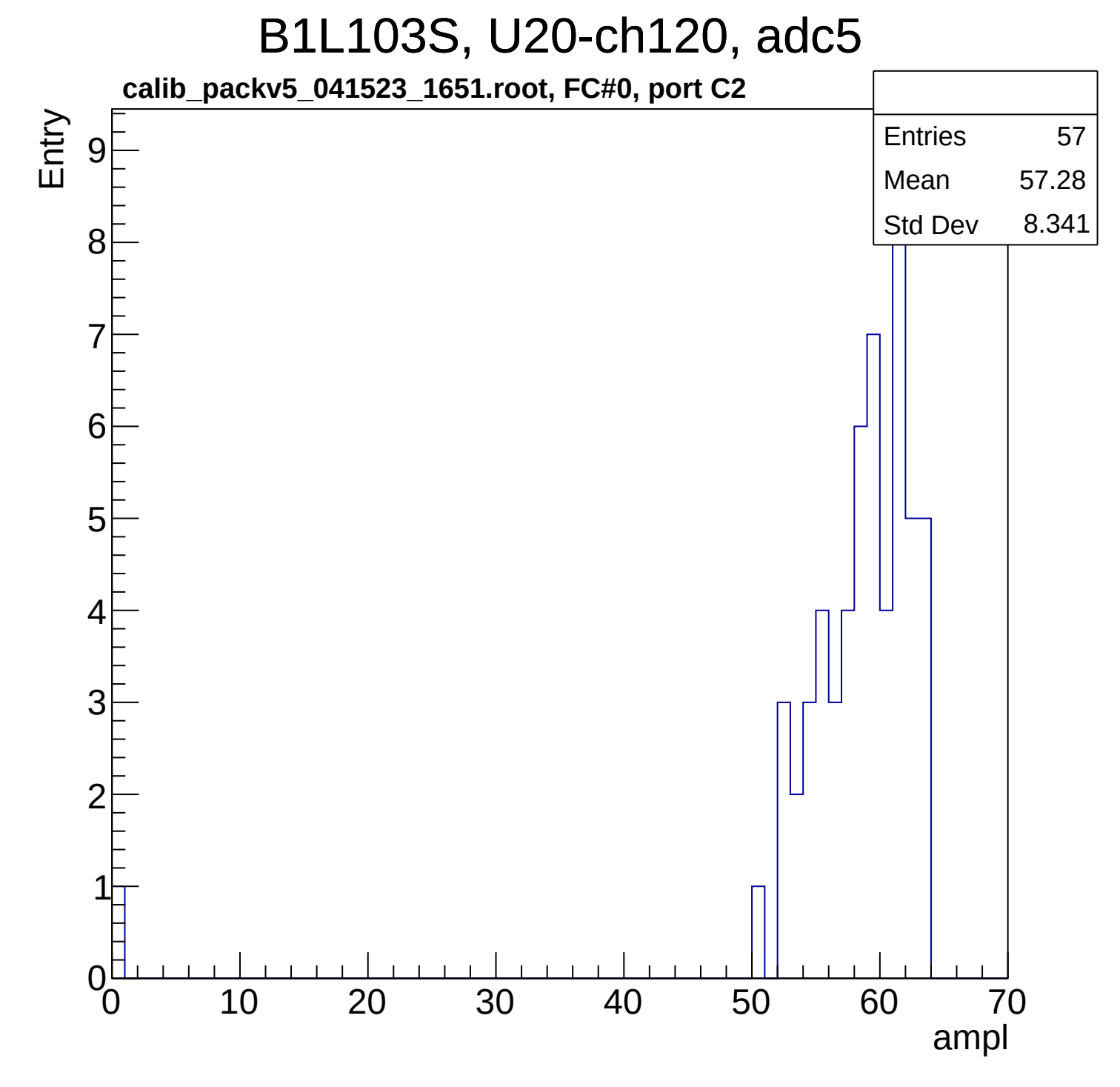
B1L103S, U20-ch120, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 57.28
Std Dev 8.341
Entry
ampl
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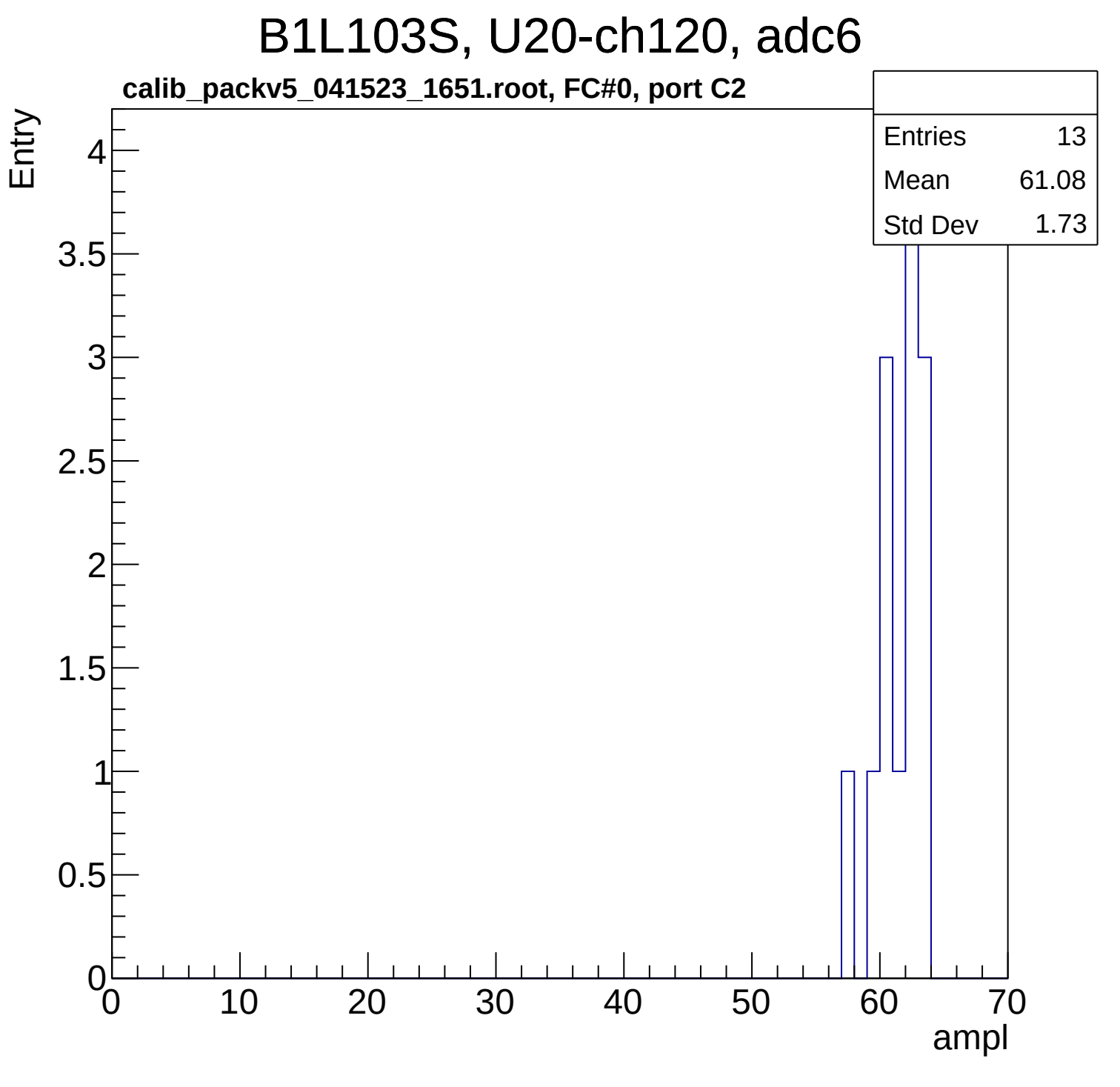
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch120, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 61.08
Std Dev 1.73
Entry
ampl
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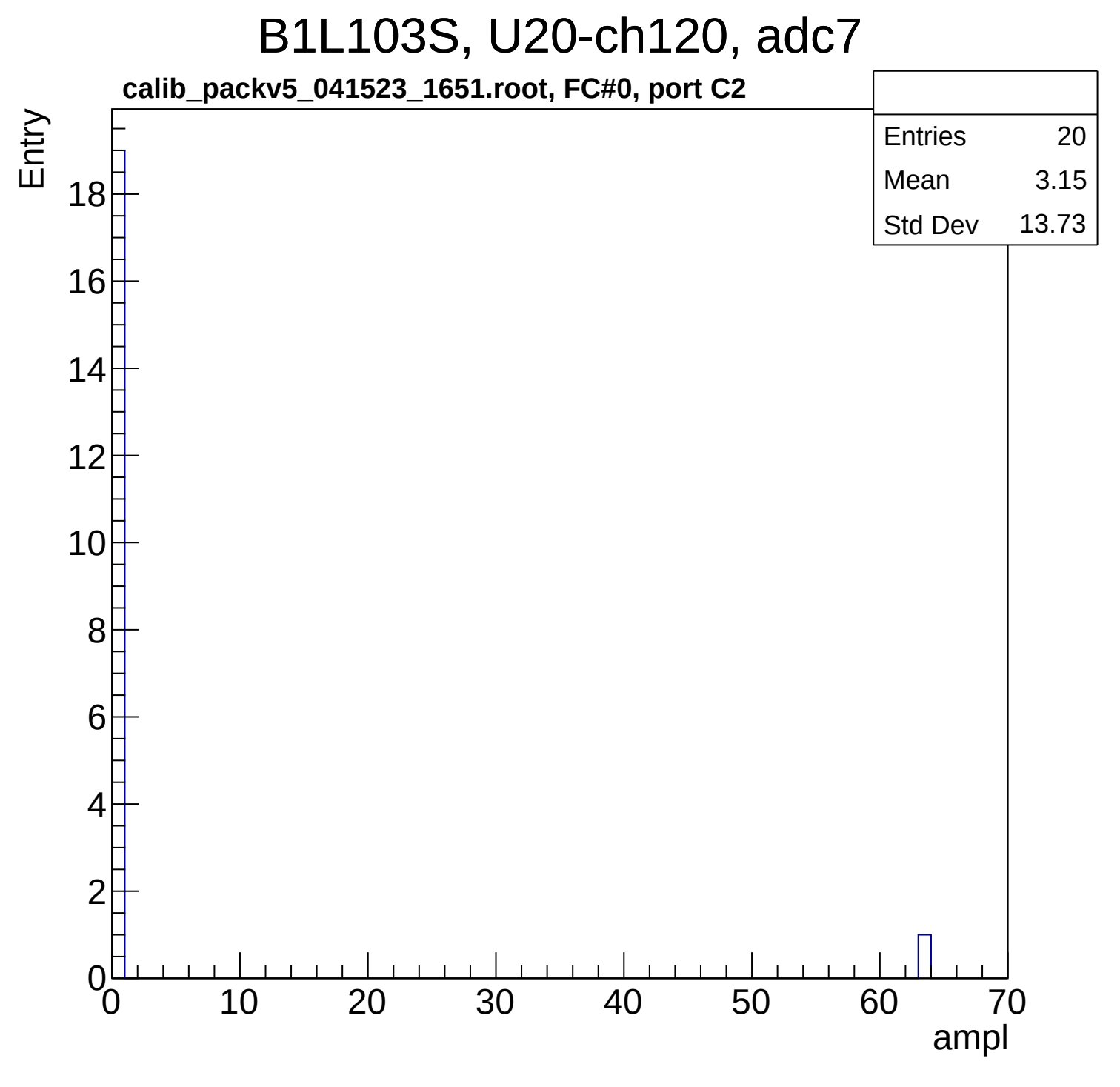
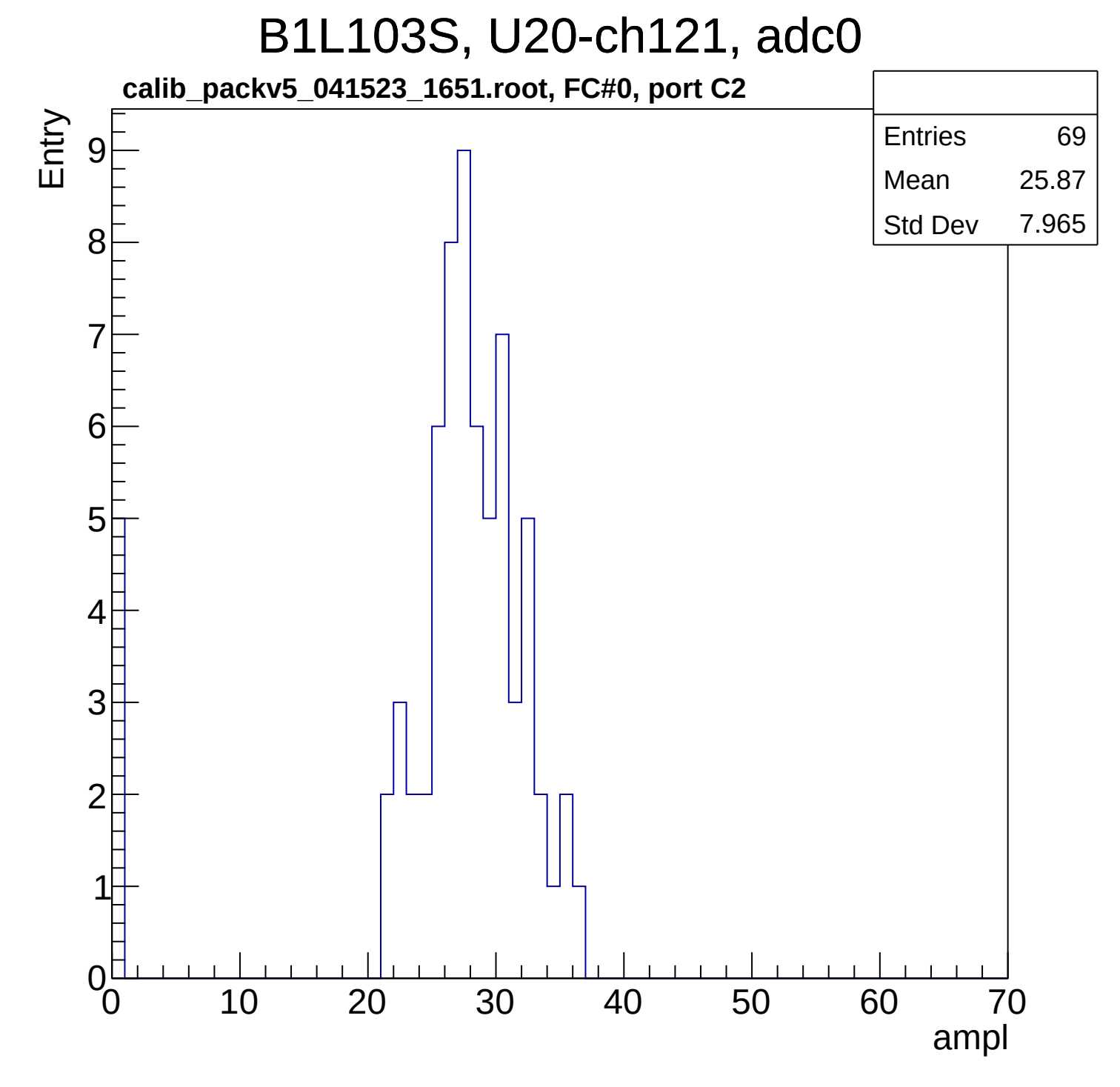
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U20-ch120, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch121, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 25.87
Std Dev 7.965
Entry
ampl
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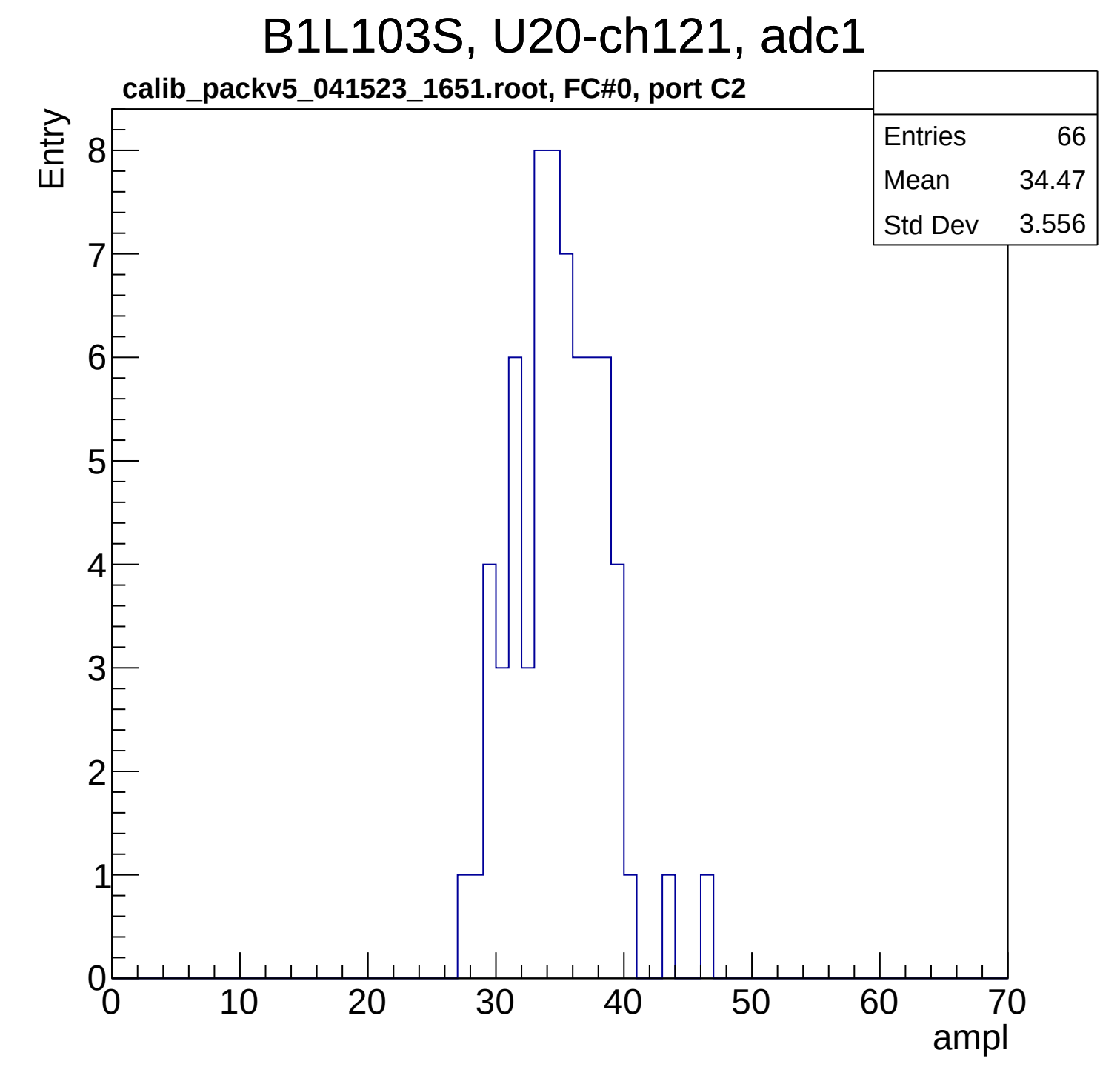
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch121, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 34.47
Std Dev 3.556
Entry
ampl
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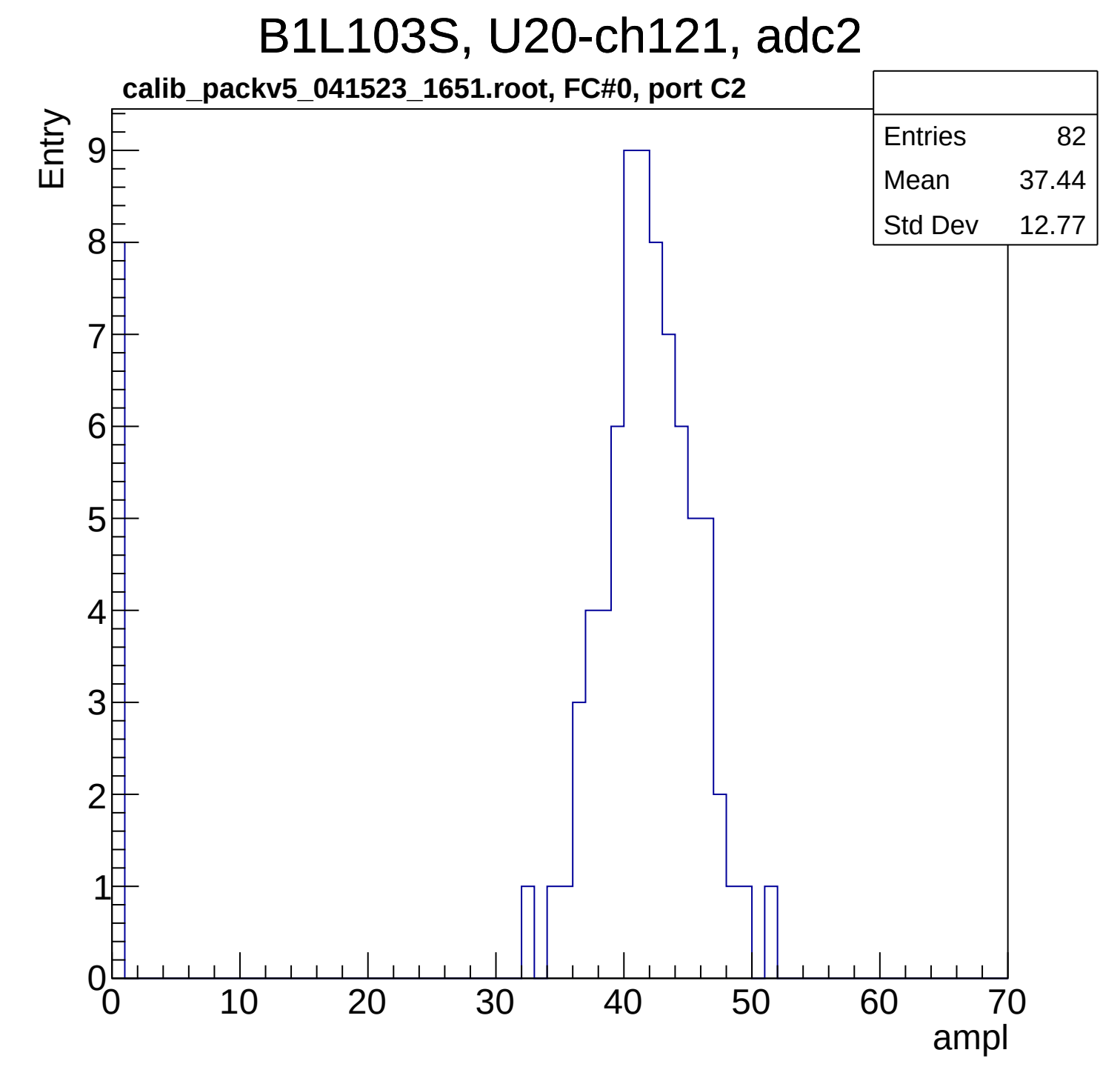
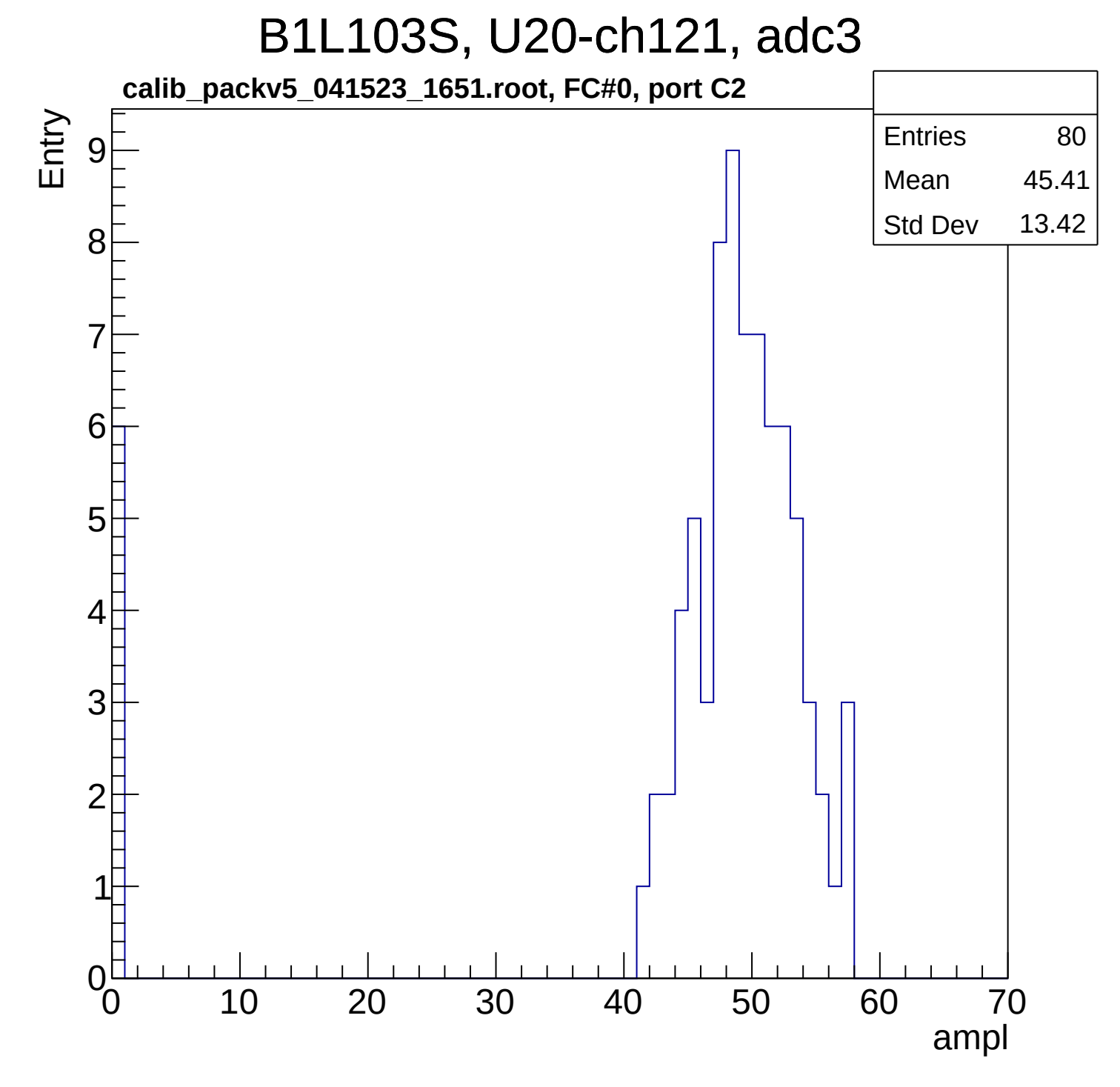
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch121, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 37.44
Std Dev 12.77
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch121, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 45.41
Std Dev 13.42
Entry
ampl
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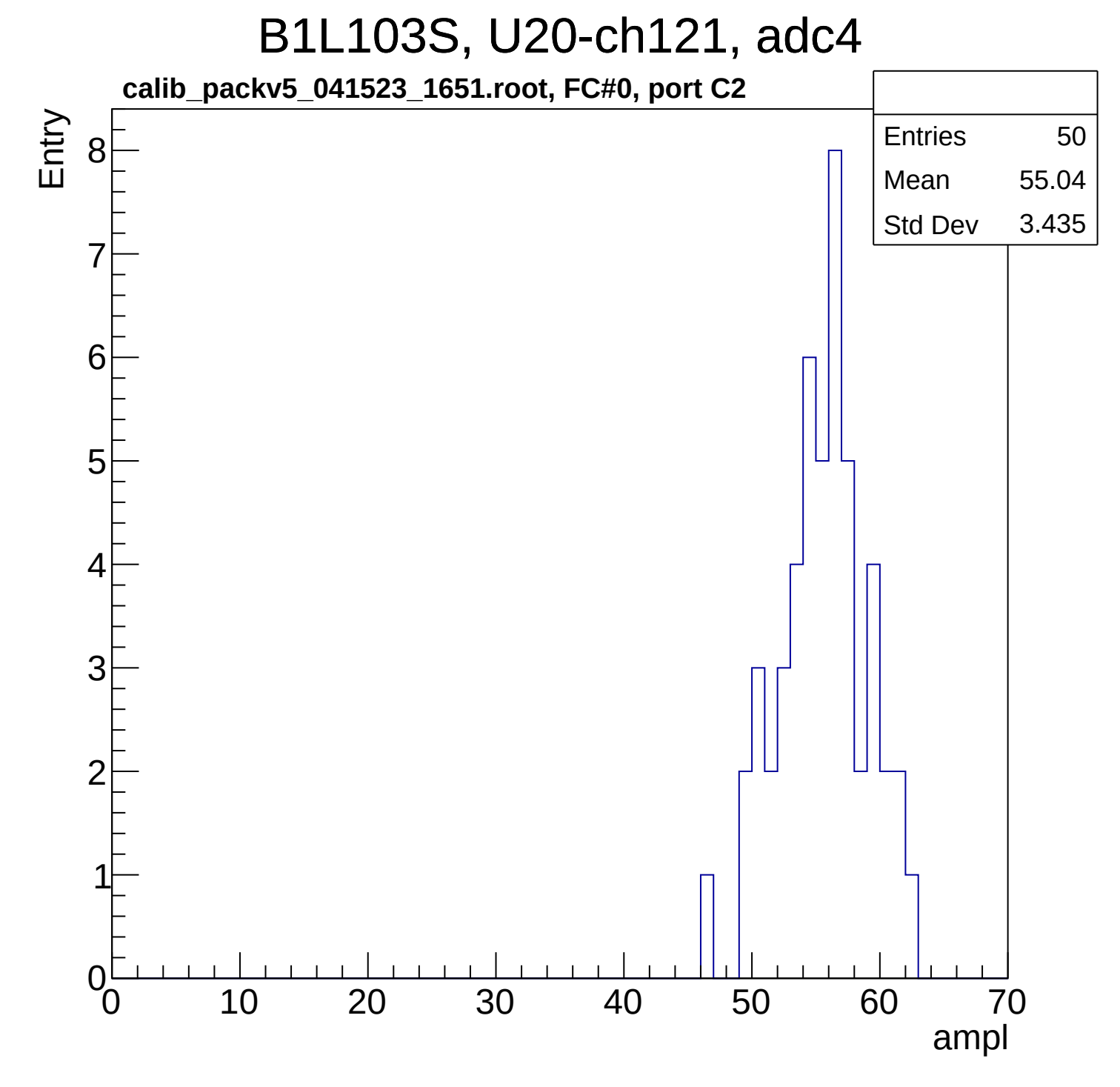
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch121, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 55.04
Std Dev 3.435
Entry
ampl
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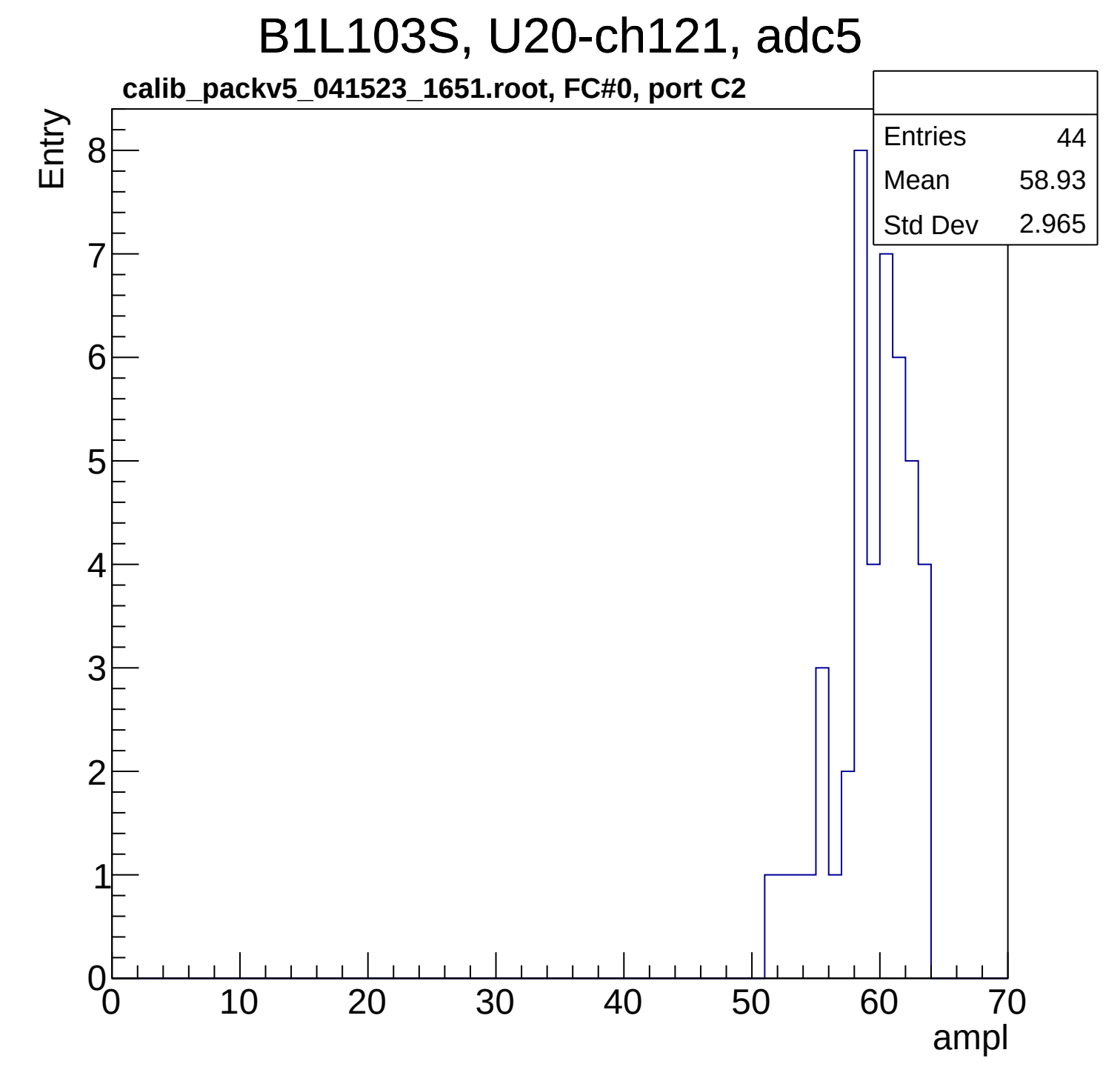
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch121, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 58.93
Std Dev 2.965
Entry
ampl
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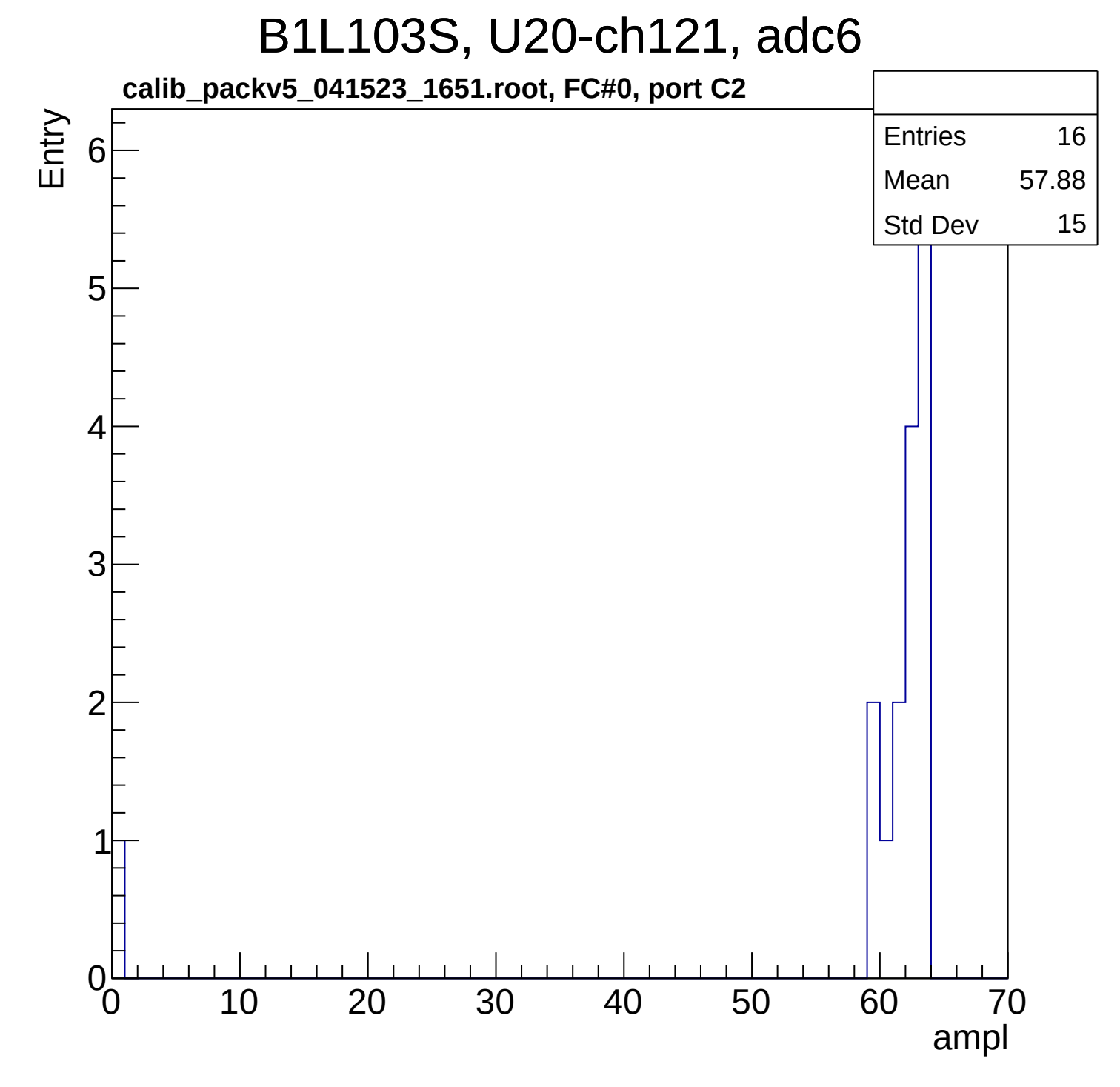
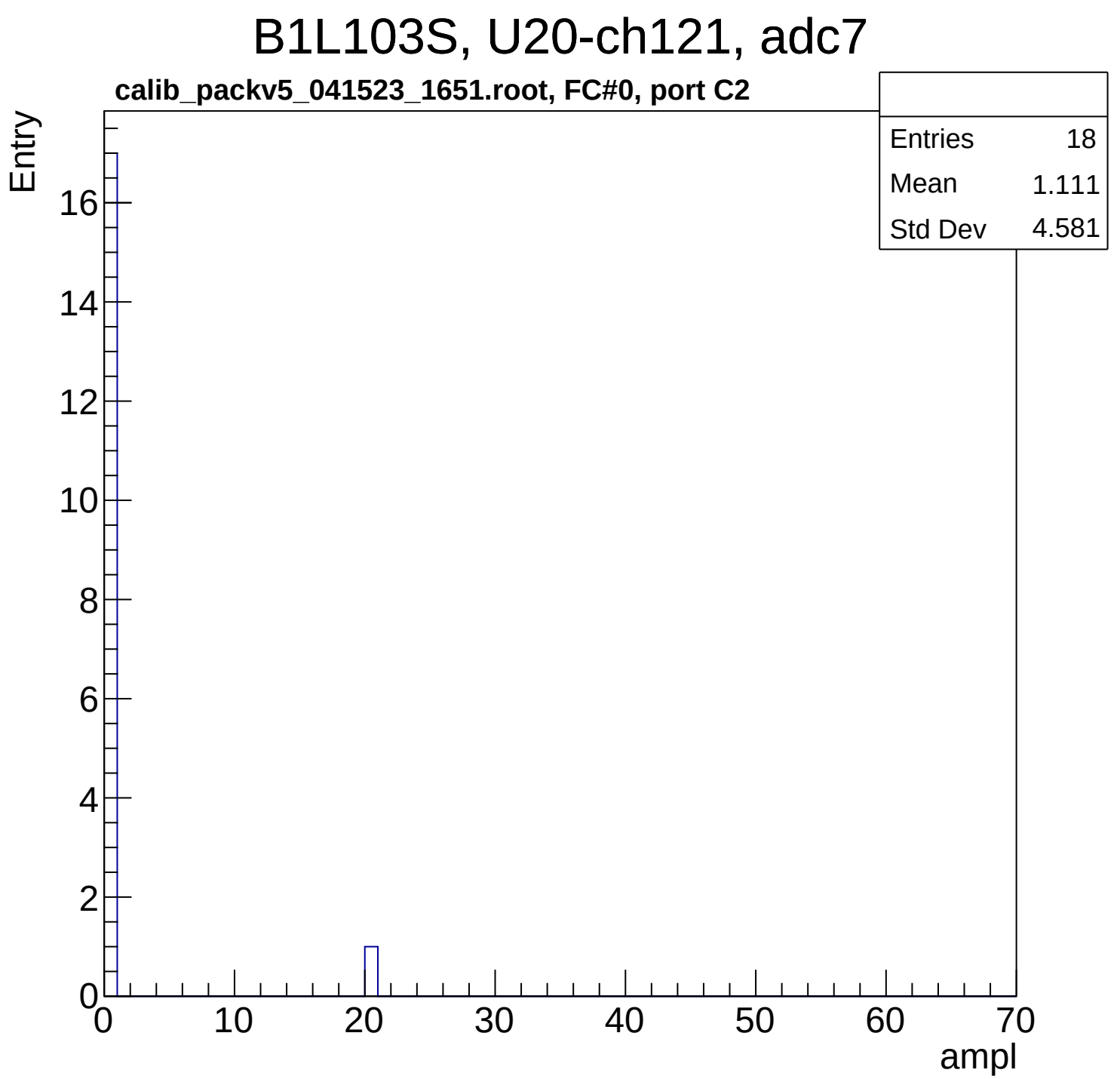
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch121, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 57.88
Std Dev 15
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U20-ch121, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.111
Std Dev 4.581
Entry
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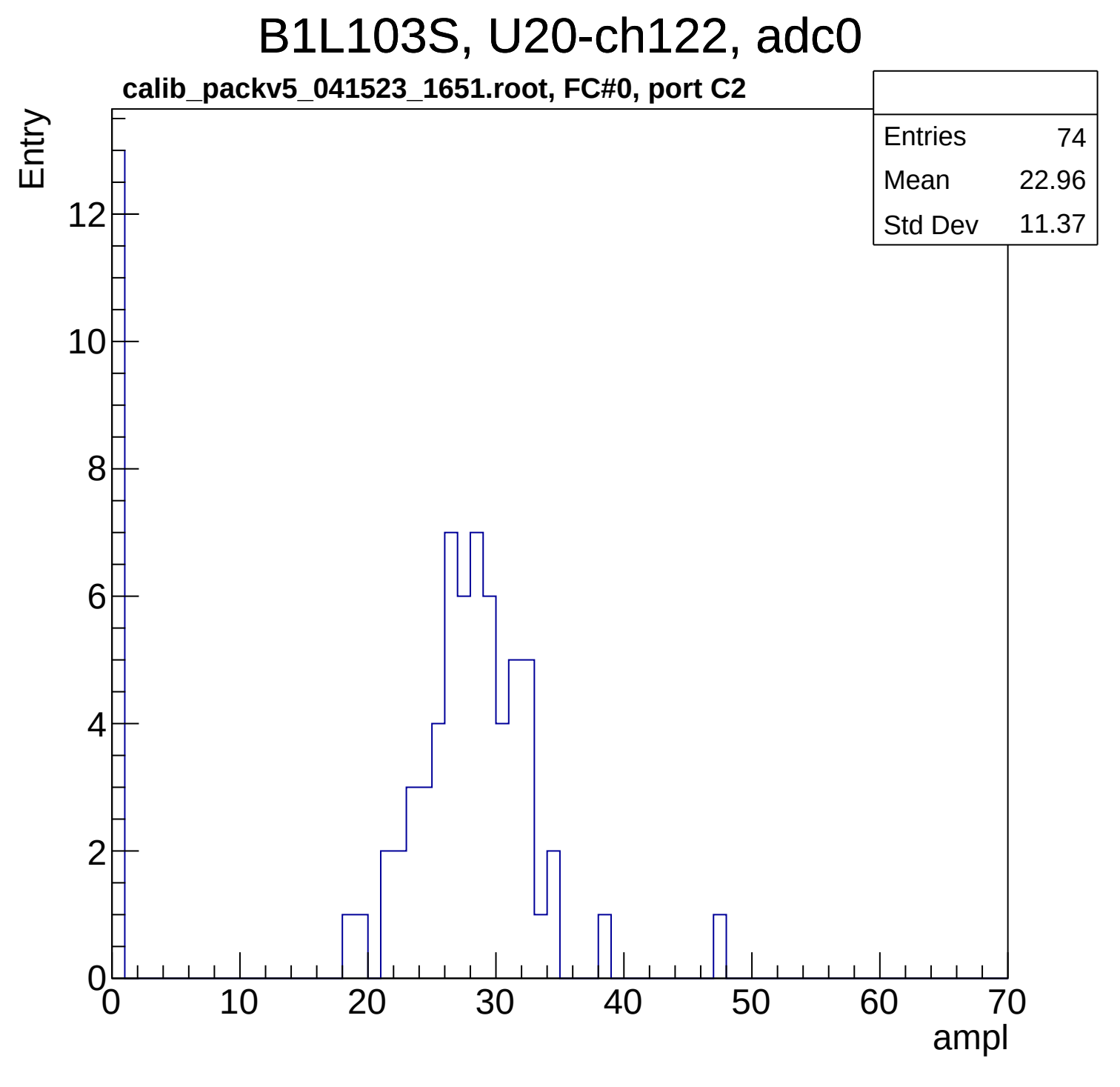
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch122, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 22.96
Std Dev 11.37
Entry
ampl
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4
6
8
10
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0
10
20
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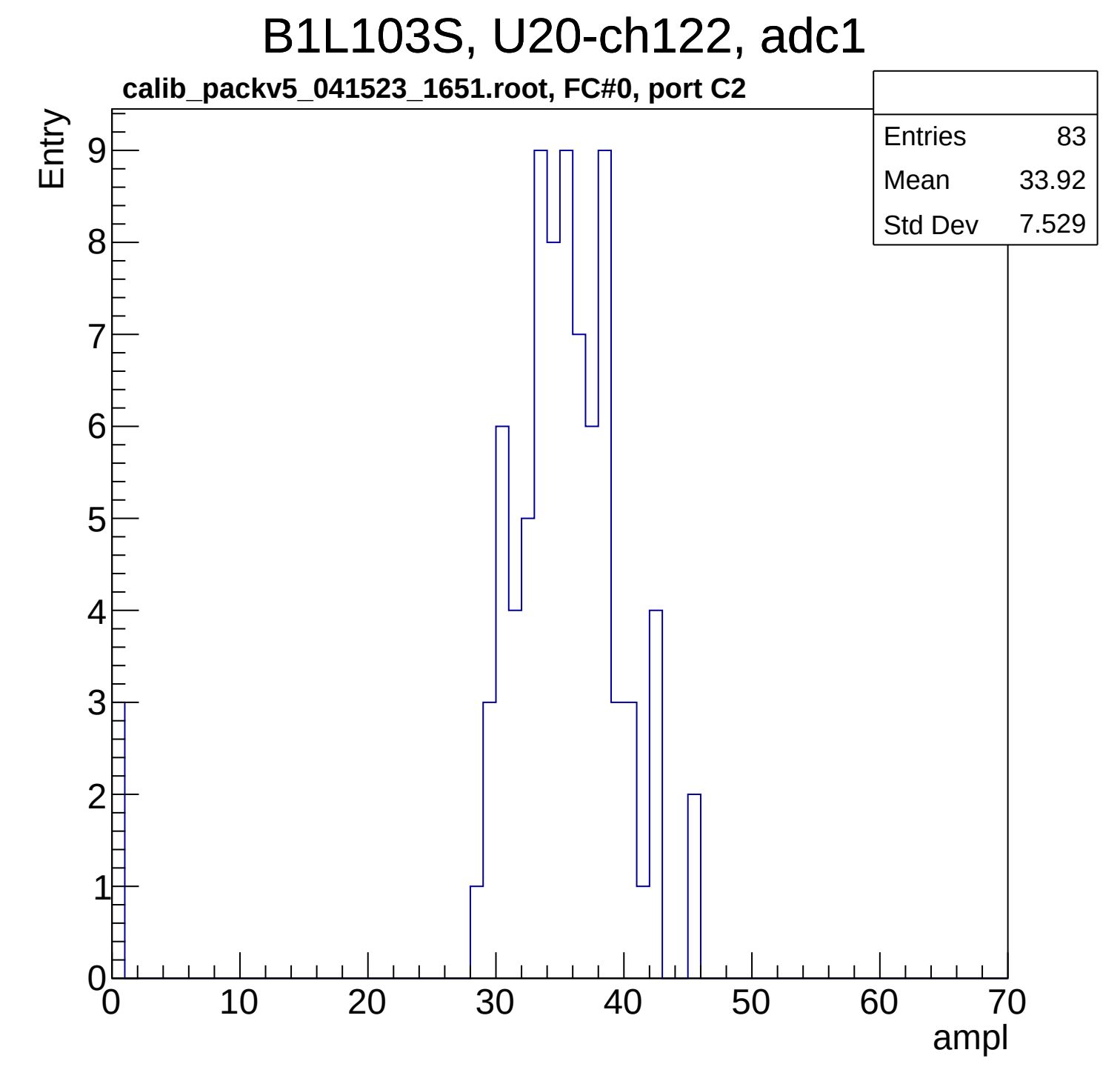
50
60
70


B1L103S, U20-ch122, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 33.92
Std Dev 7.529
Entry
ampl
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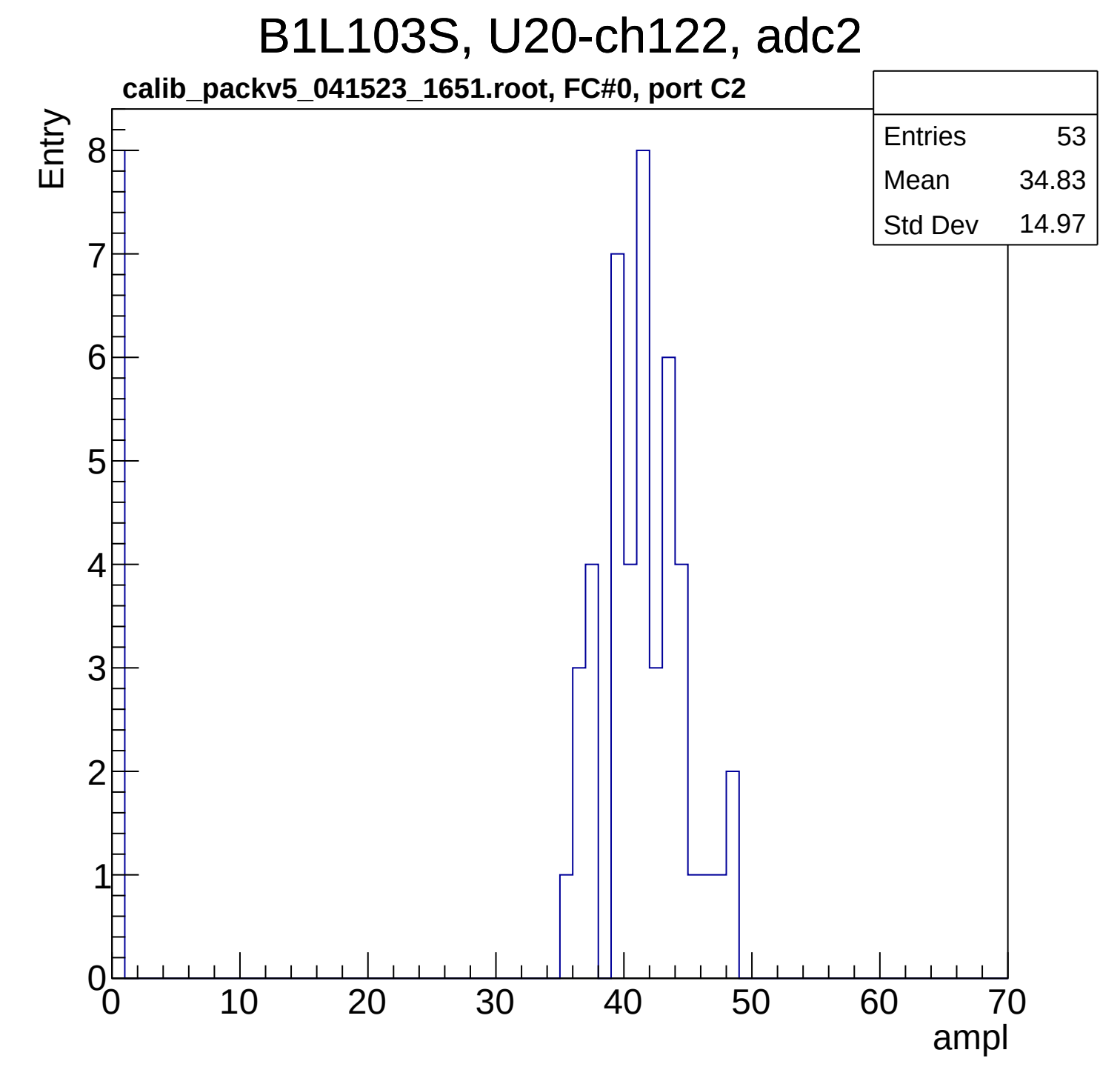
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch122, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 34.83
Std Dev 14.97
Entry
ampl
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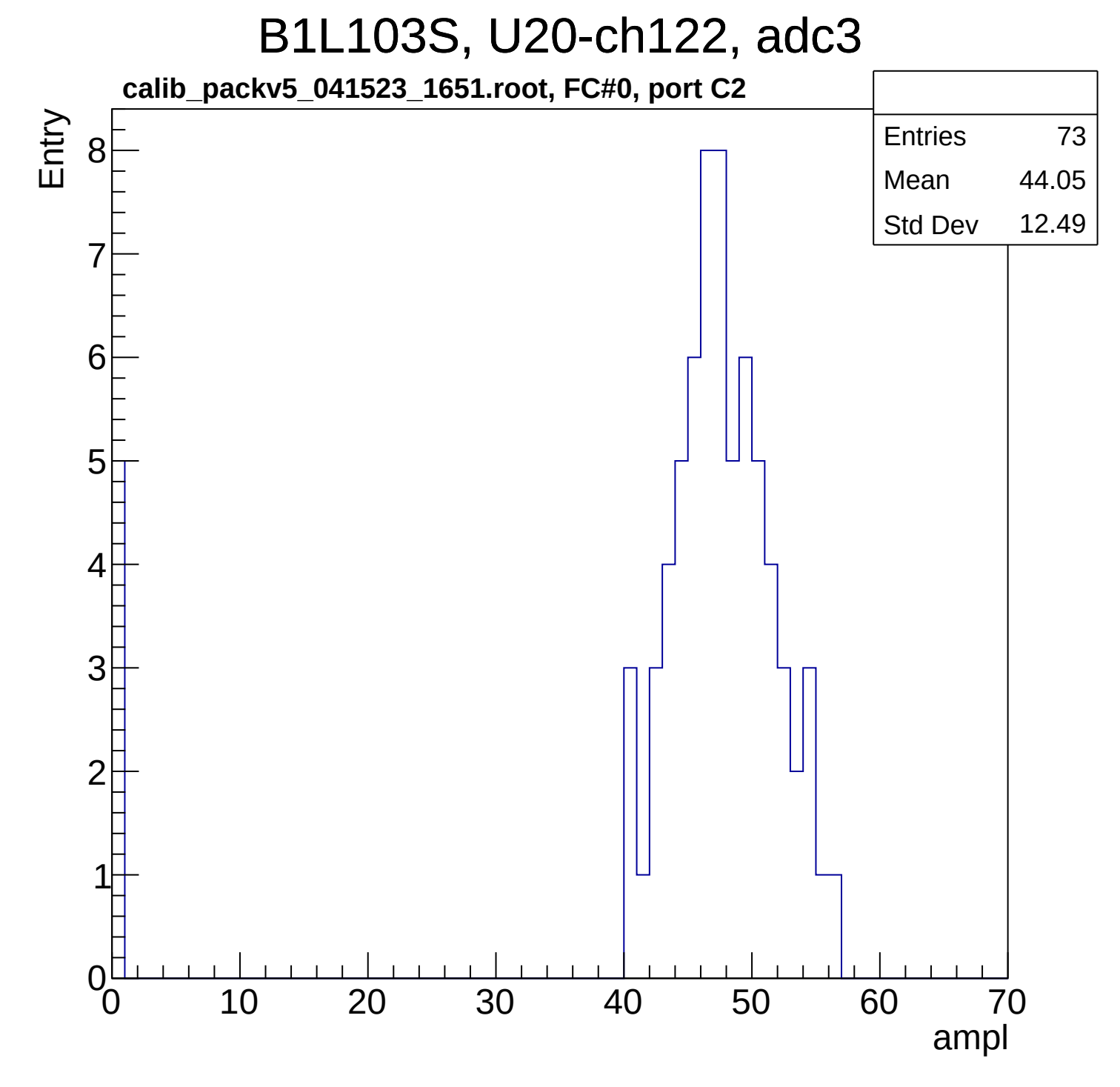
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch122, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 44.05
Std Dev 12.49
Entry
ampl
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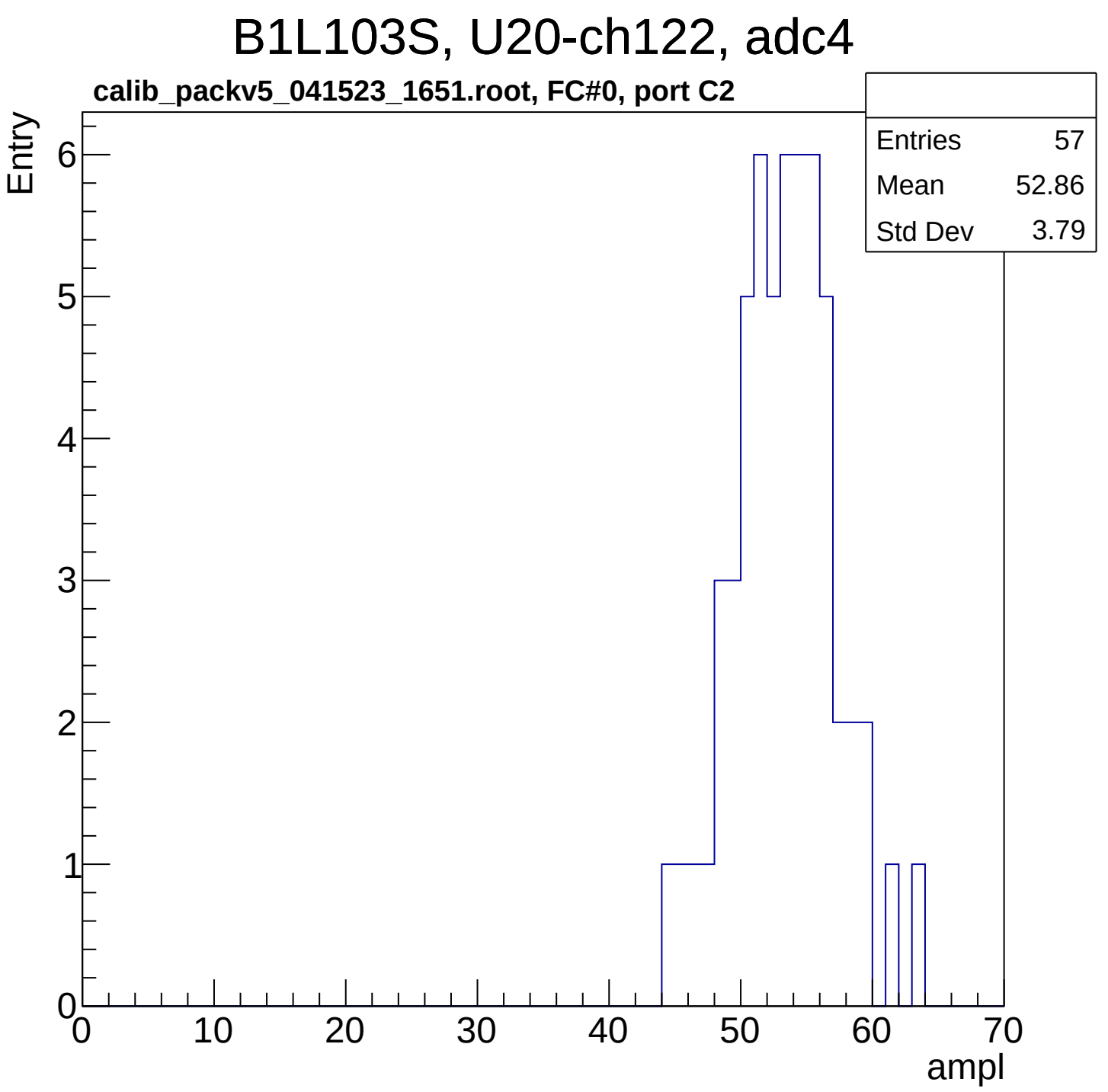
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch122, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 52.86
Std Dev 3.79
Entry
0
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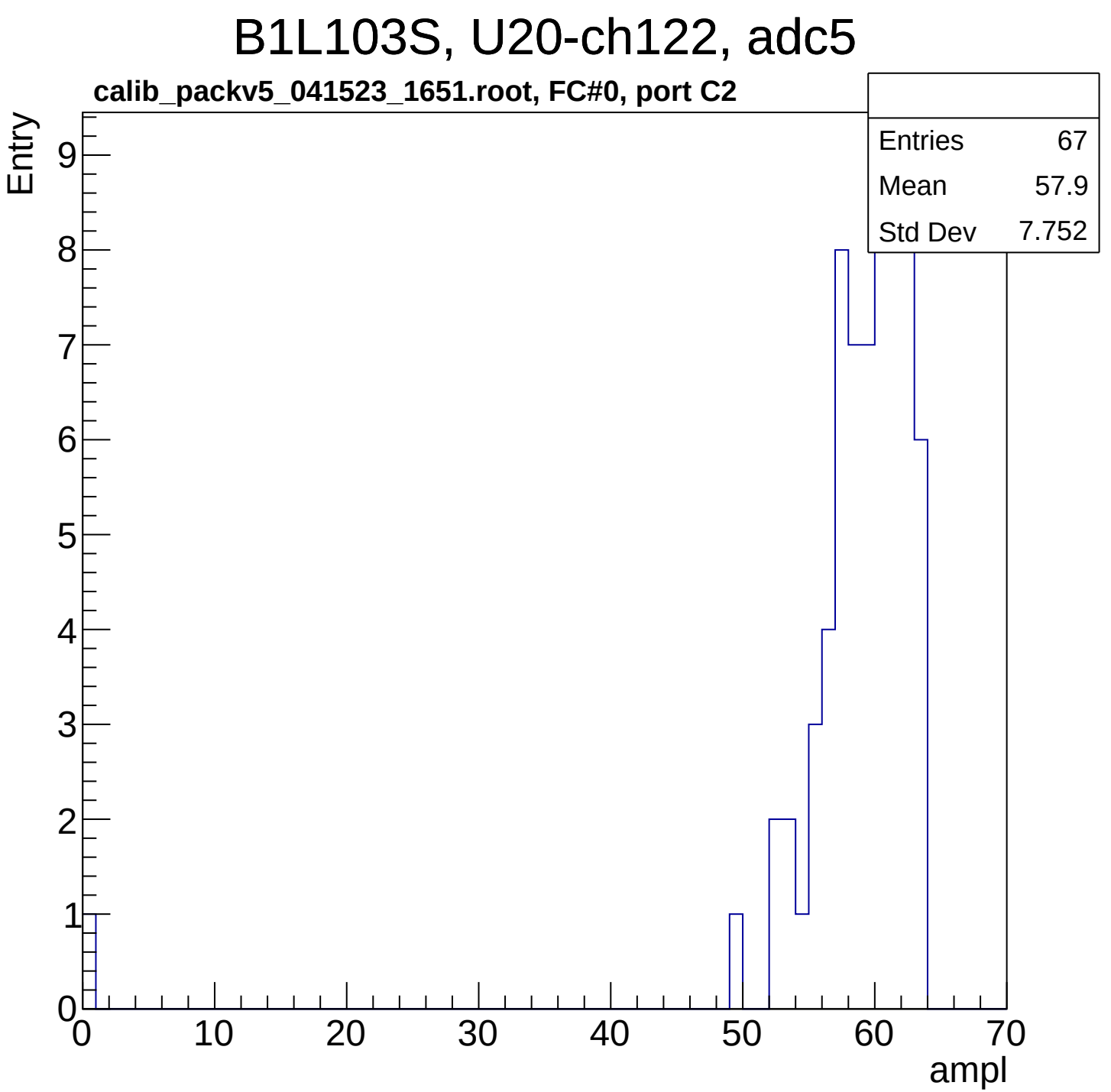
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch122, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 57.9
Std Dev 7.752
Entry
ampl
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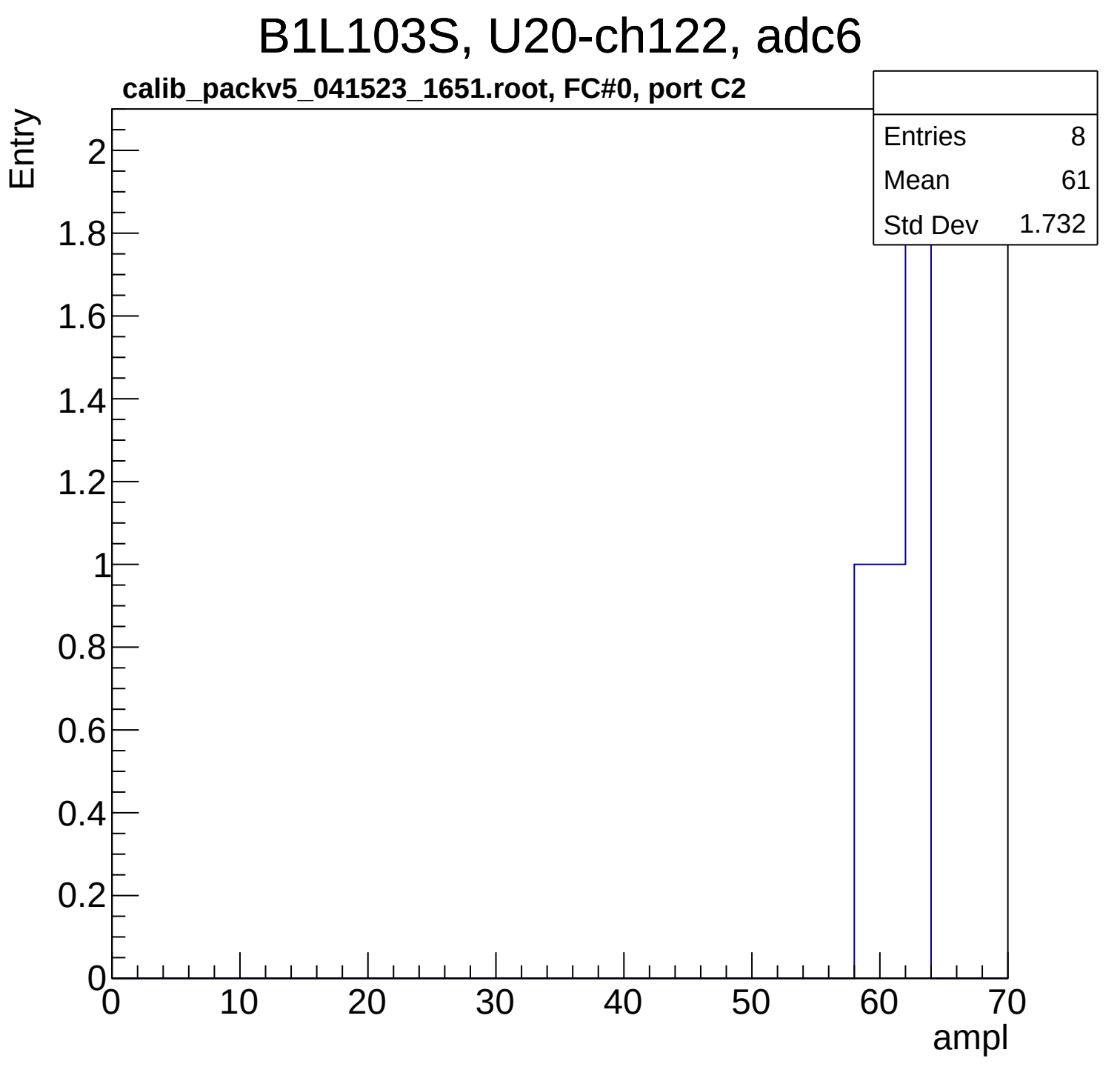
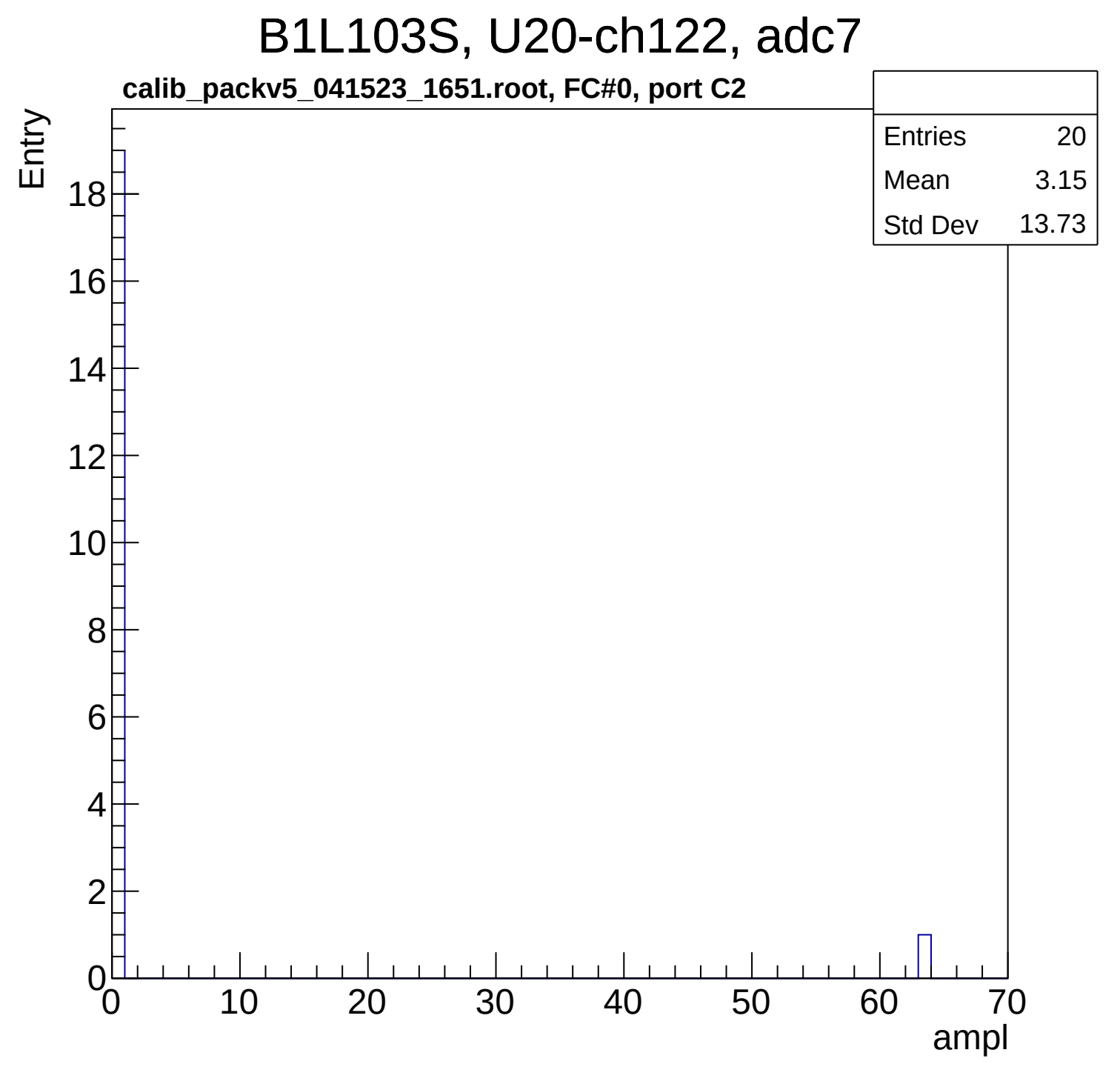
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch122, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 61
Std Dev 1.732
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U20-ch122, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
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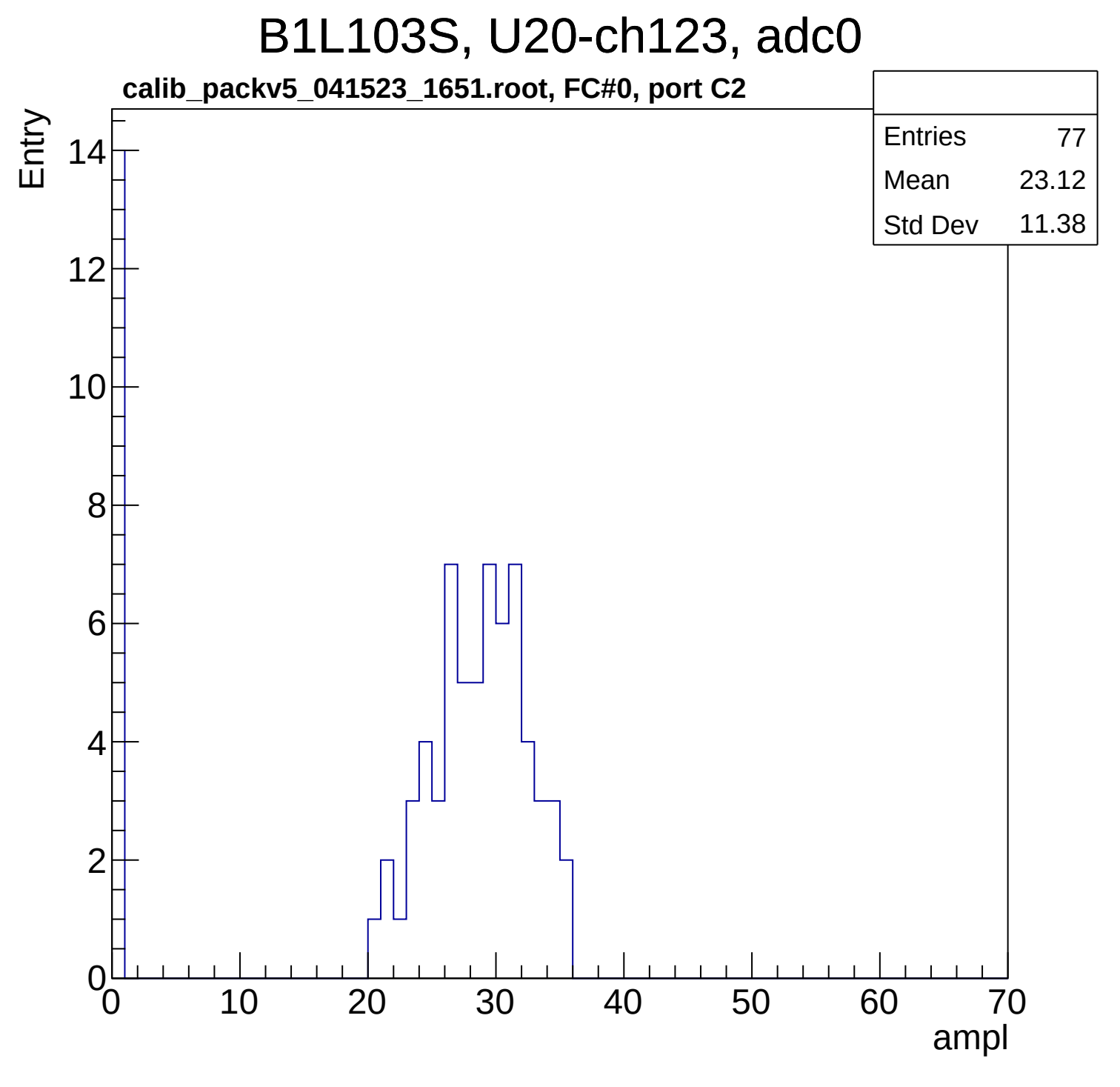
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch123, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 23.12
Std Dev 11.38
Entry
ampl
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8
10
12
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0
10
20
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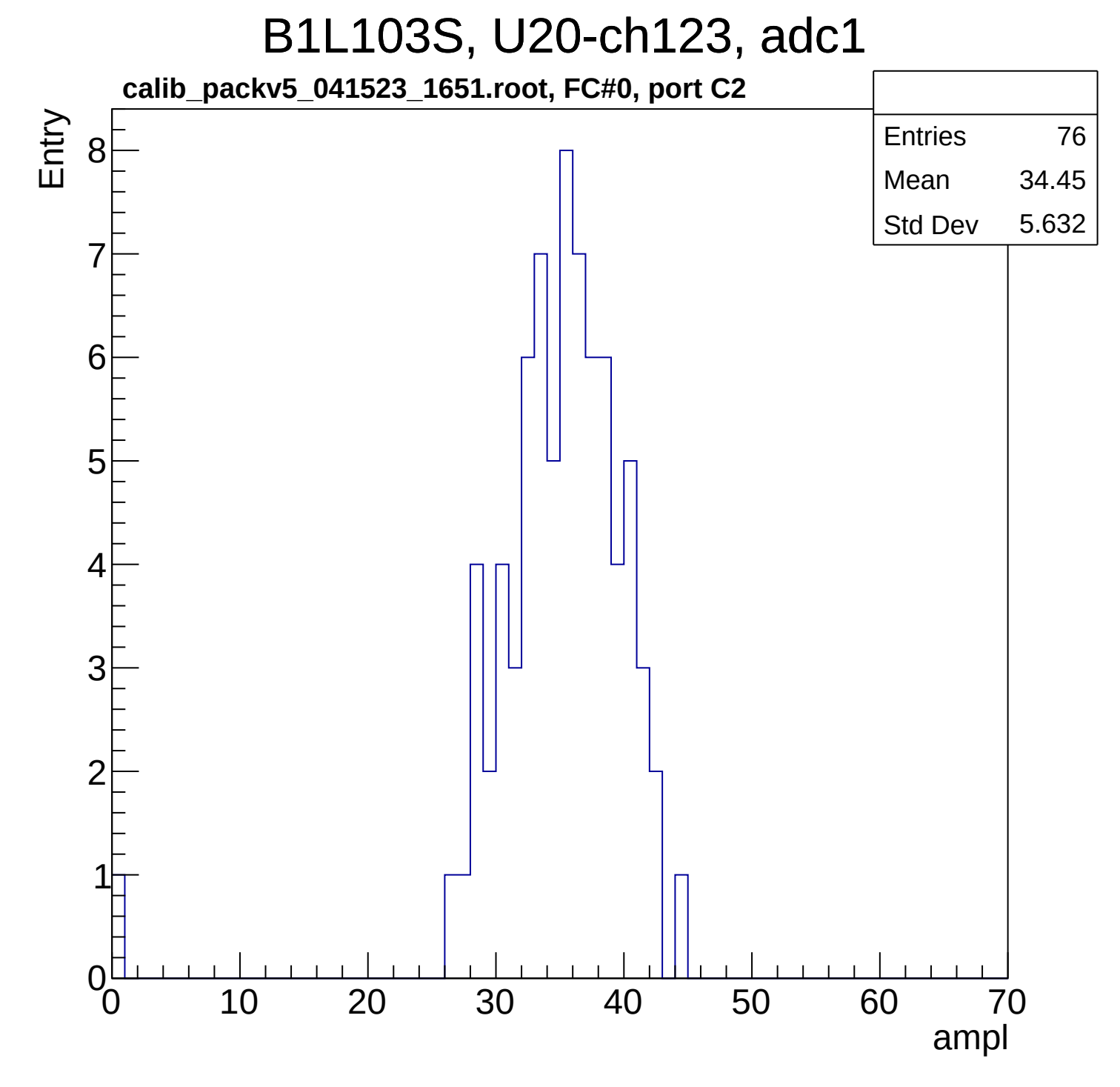
40
50
60
70


B1L103S, U20-ch123, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 34.45
Std Dev 5.632
Entry
ampl
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1
2
3
4
5
6
7
8
0
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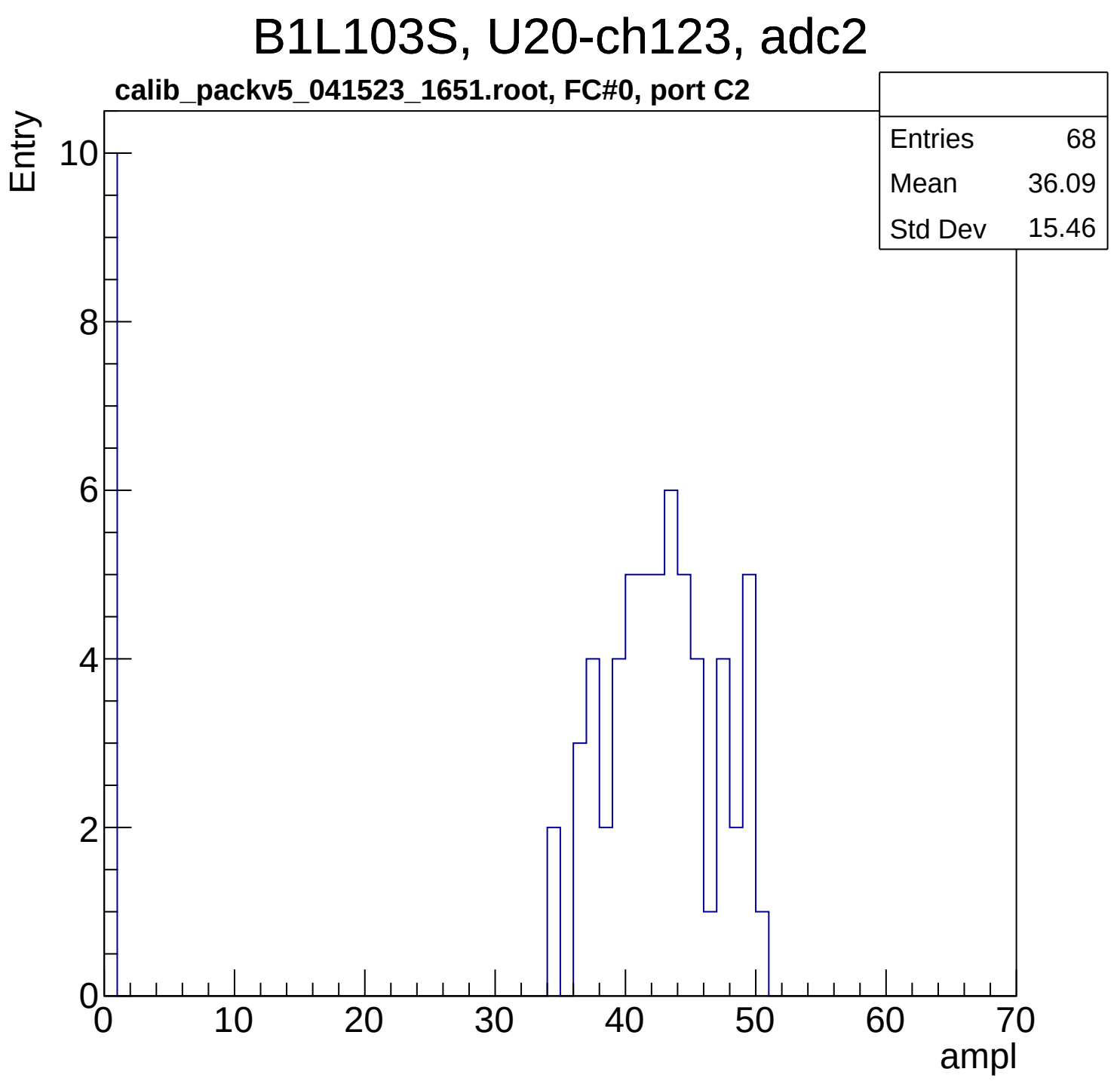
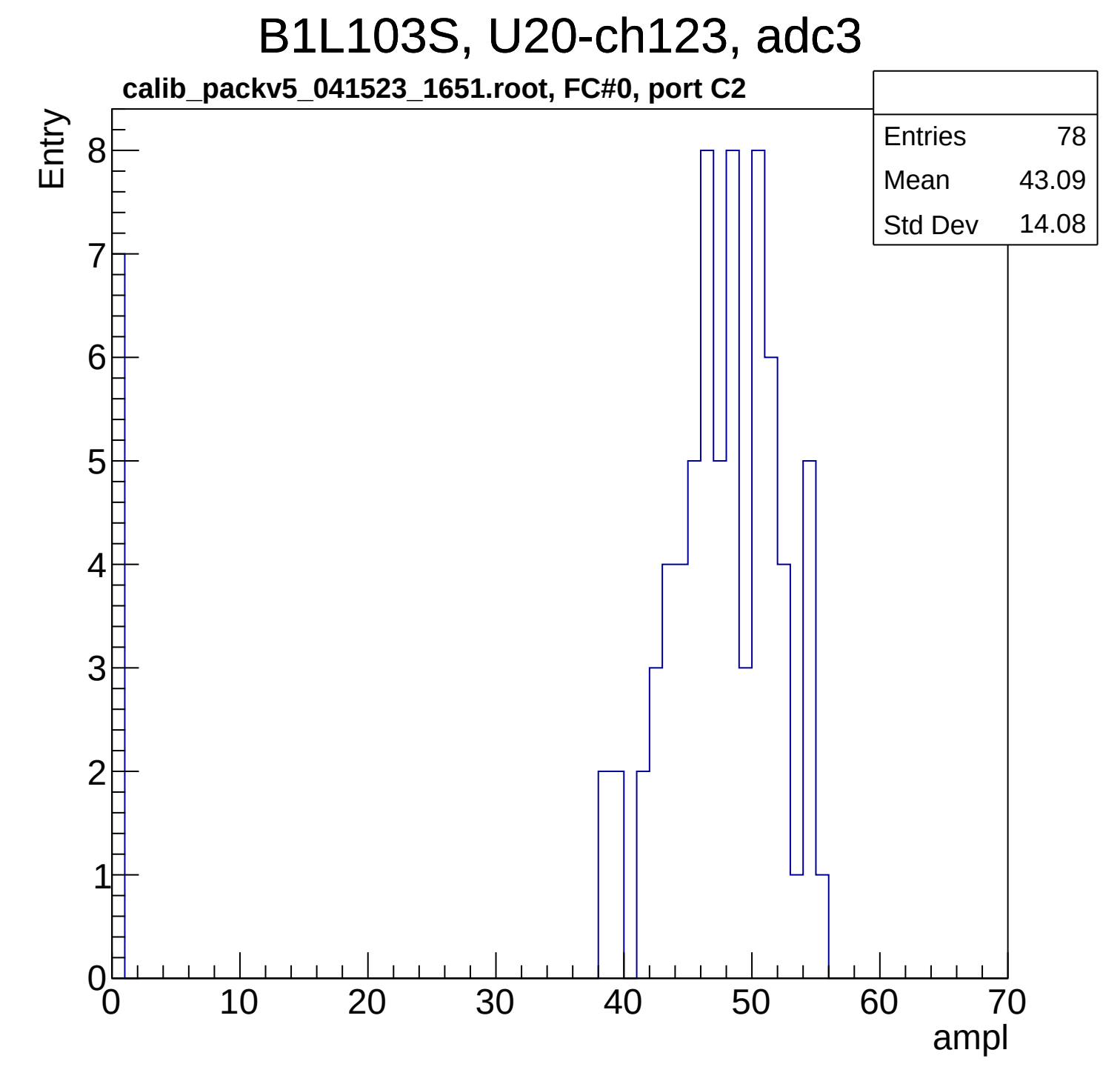
20
30
40
50
60
70


B1L103S, U20-ch123, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 36.09
Std Dev 15.46
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch123, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 43.09
Std Dev 14.08
Entry
ampl
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1
2
3
4
5
6
7
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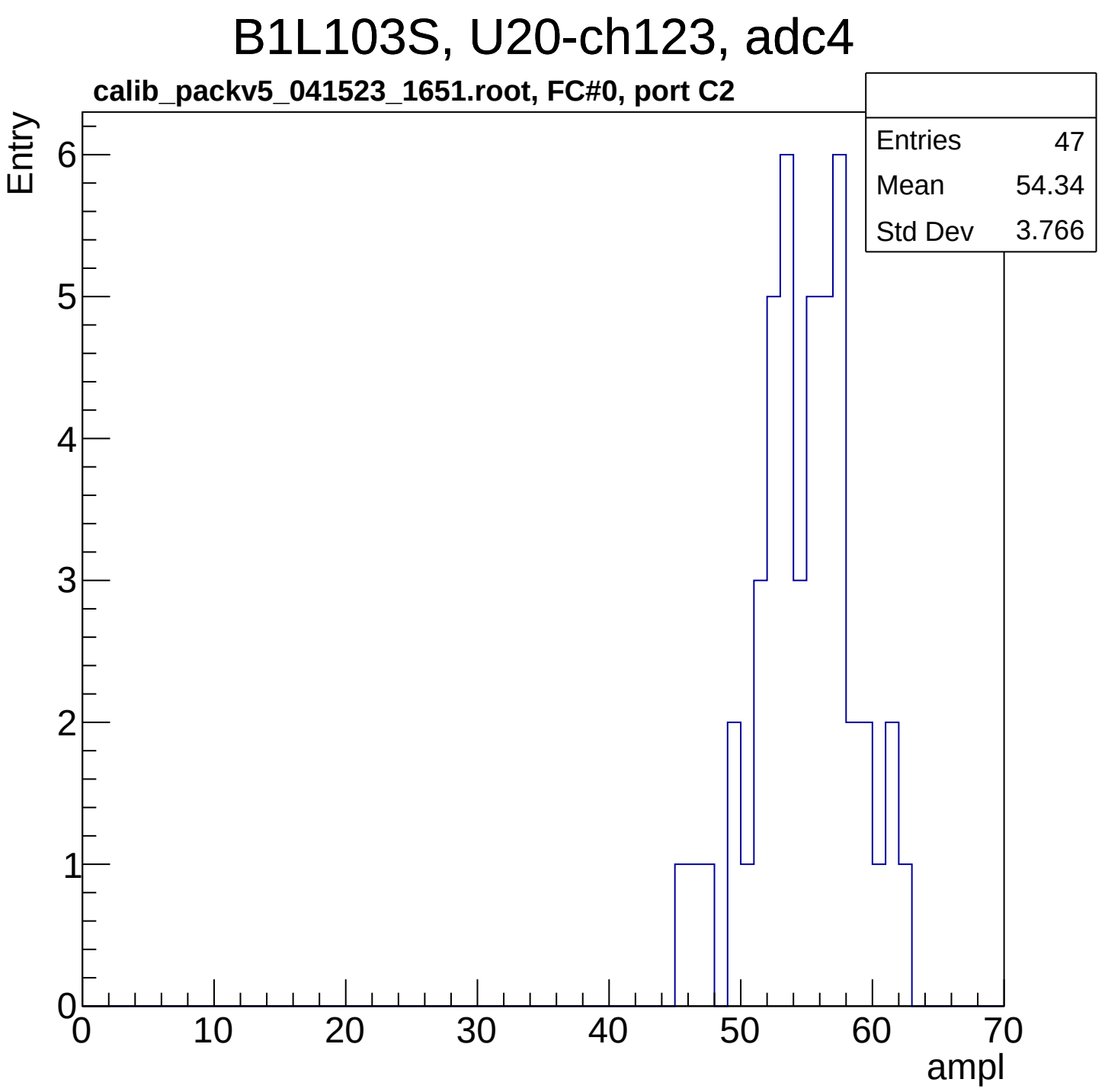
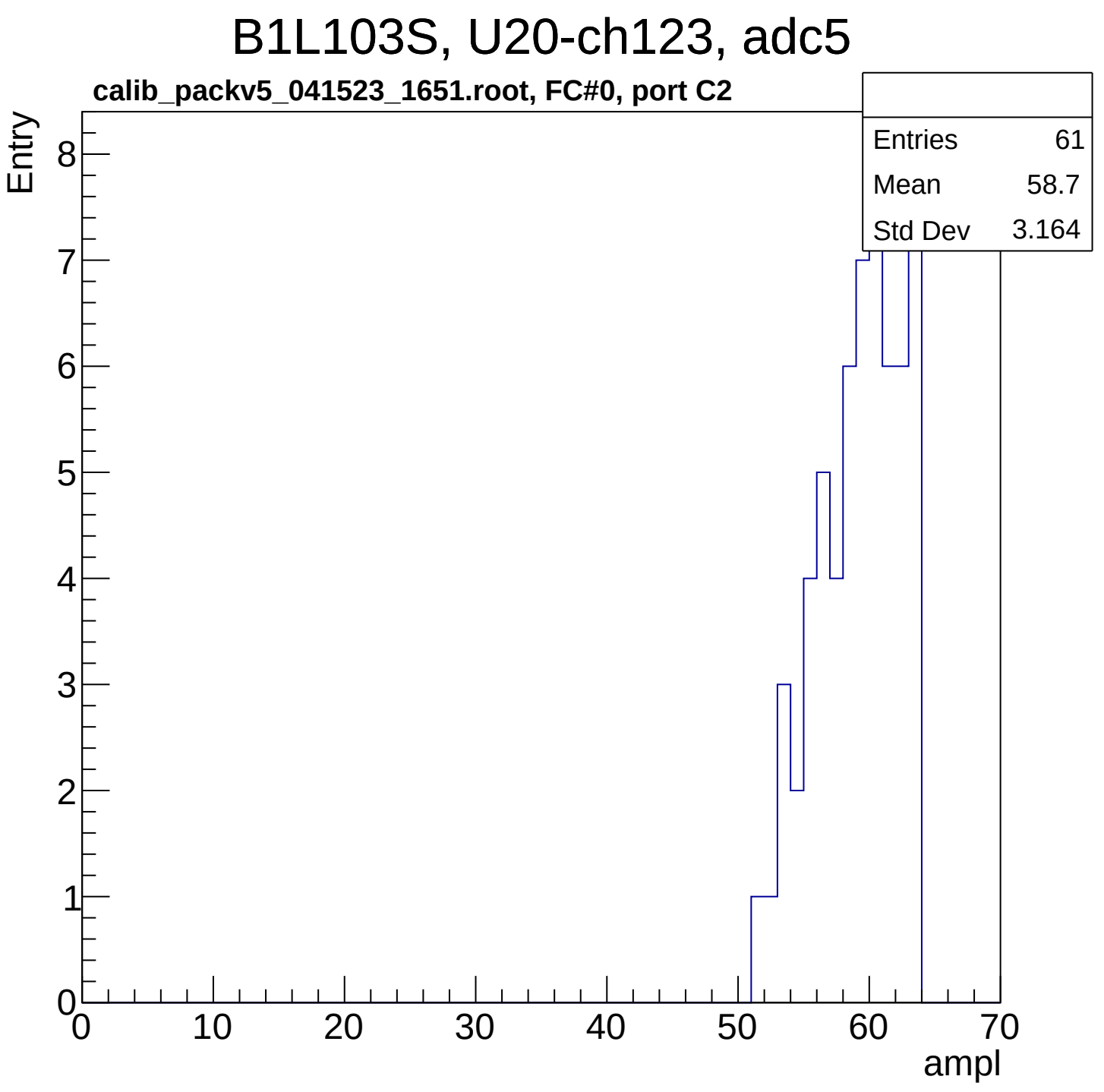
0
10
20
30
40
50
60
70


B1L103S, U20-ch123, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 54.34
Std Dev 3.766
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U20-ch123, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 58.7
Std Dev 3.164
Entry
0
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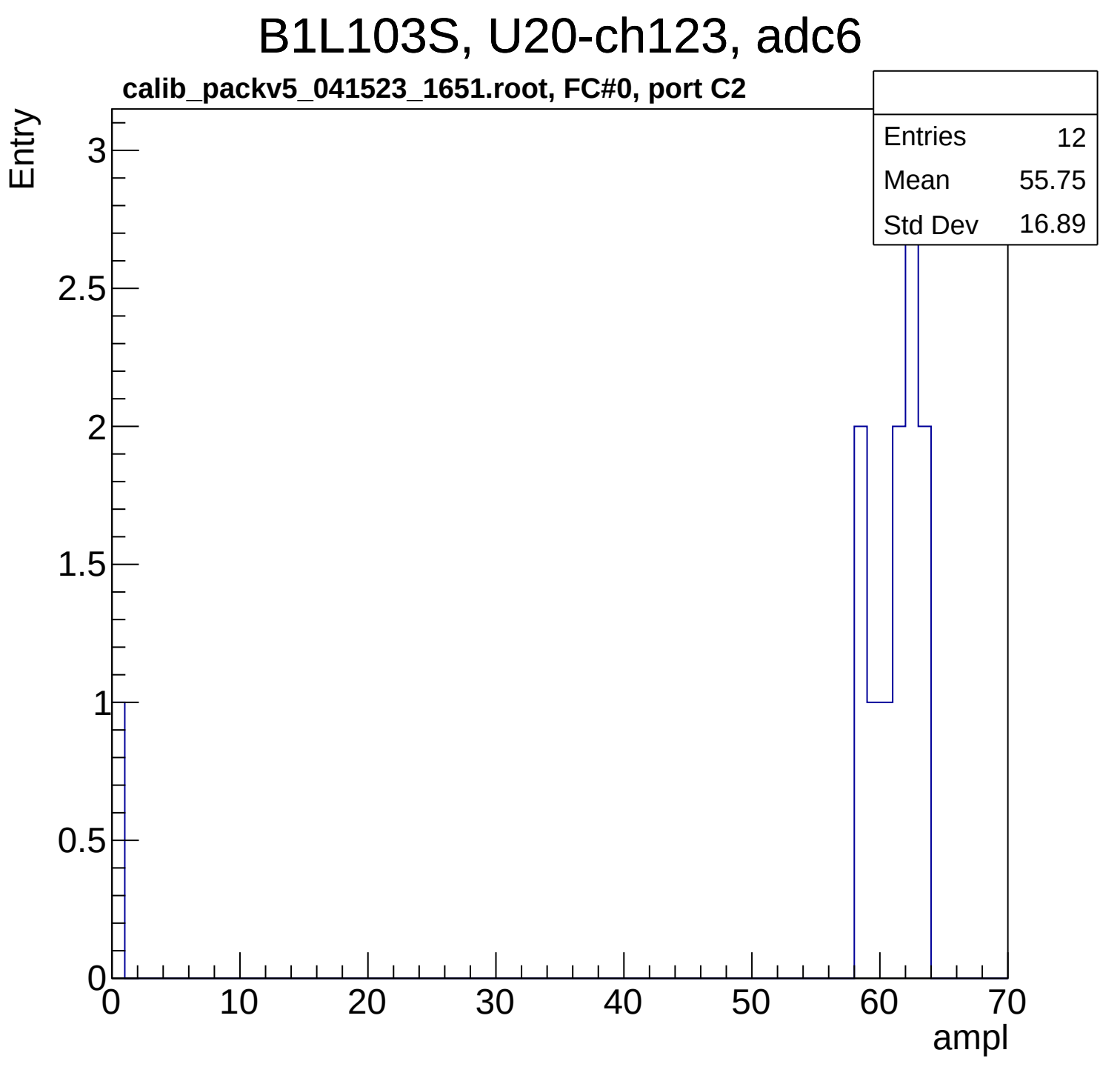
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch123, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 55.75
Std Dev 16.89
Entry
ampl
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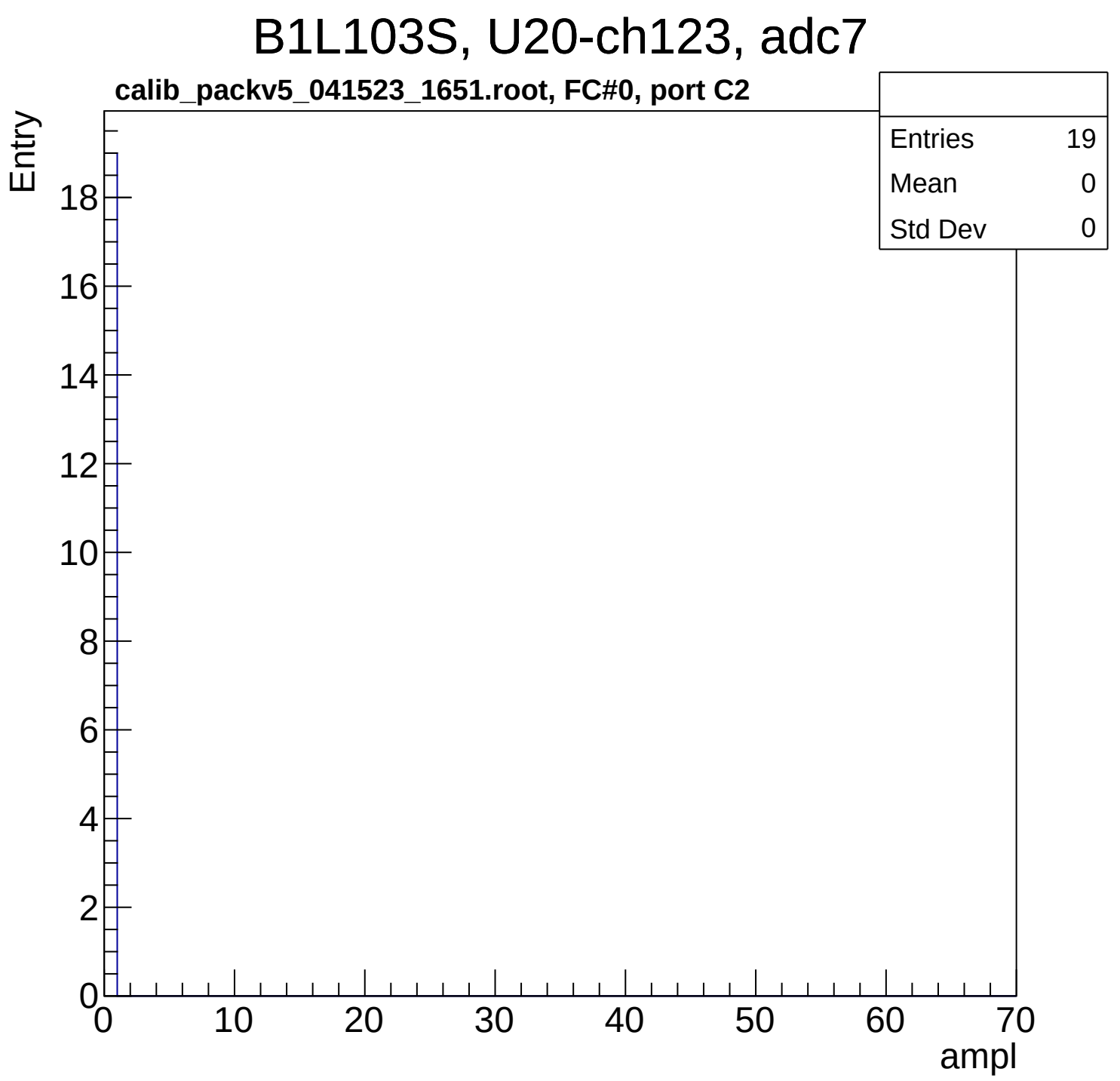
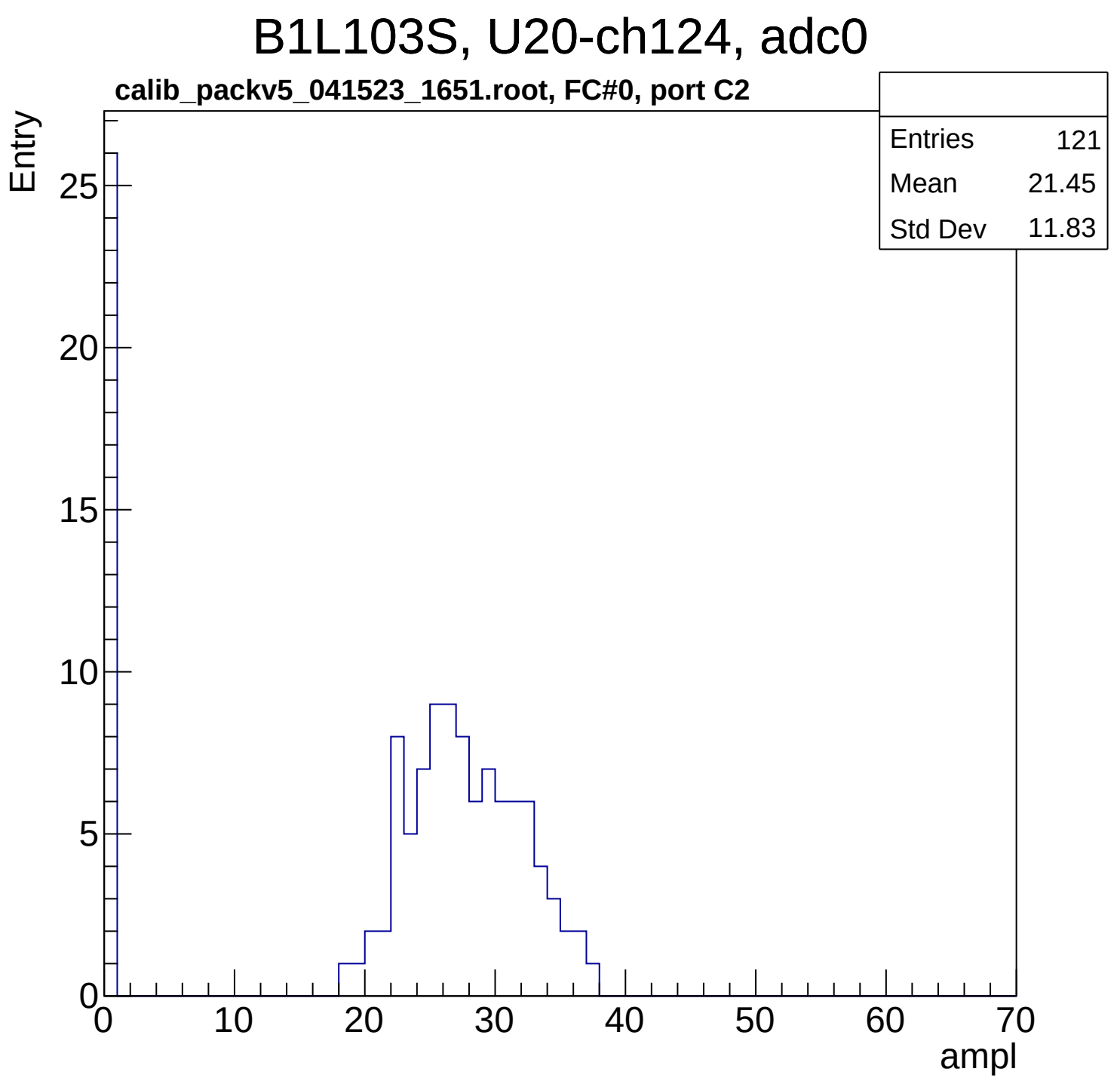
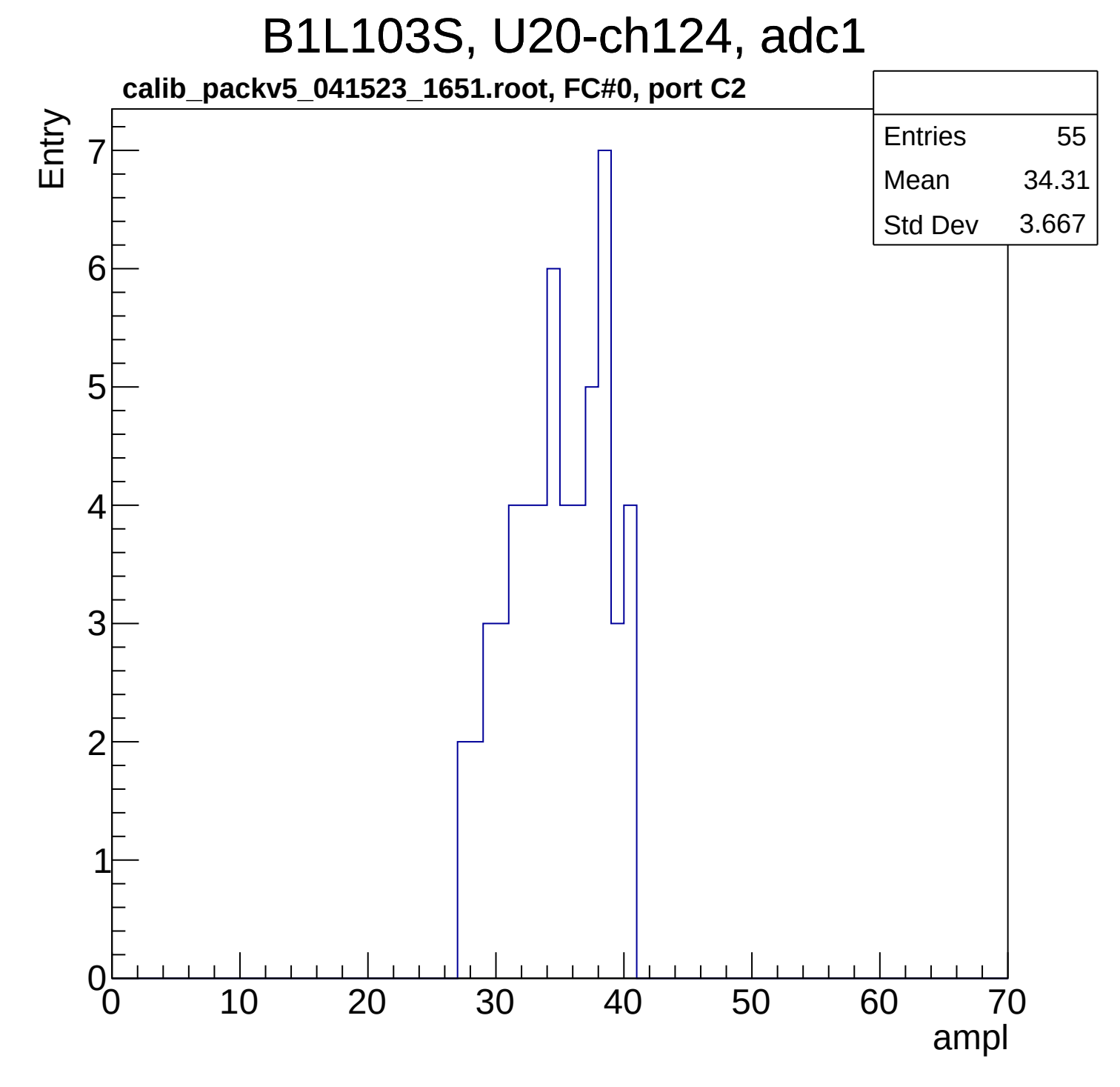
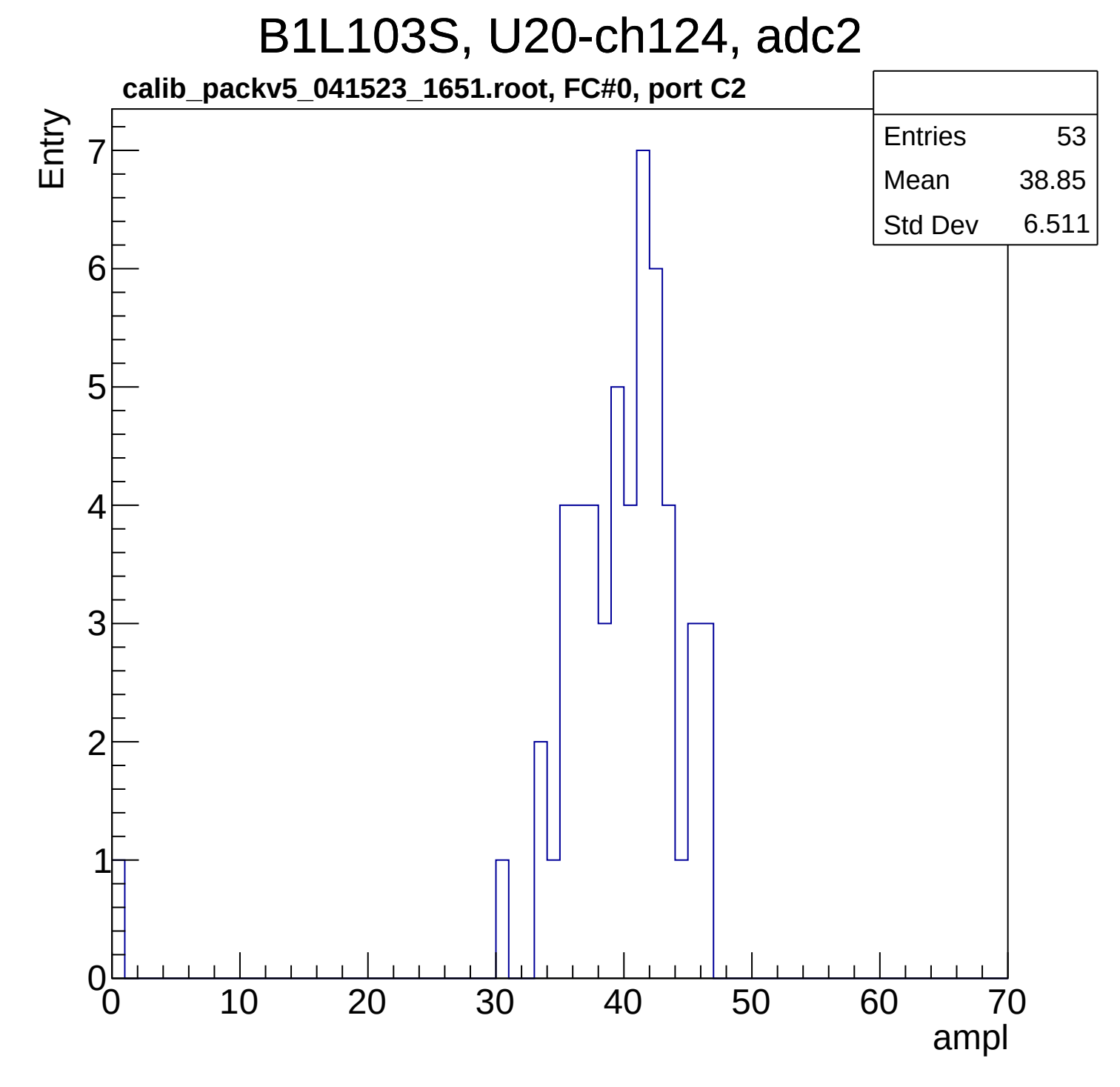
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U20-ch123, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch124, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 121
Mean 21.45
Std Dev 11.83
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch124, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 34.31
Std Dev 3.667
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U20-ch124, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 38.85
Std Dev 6.511
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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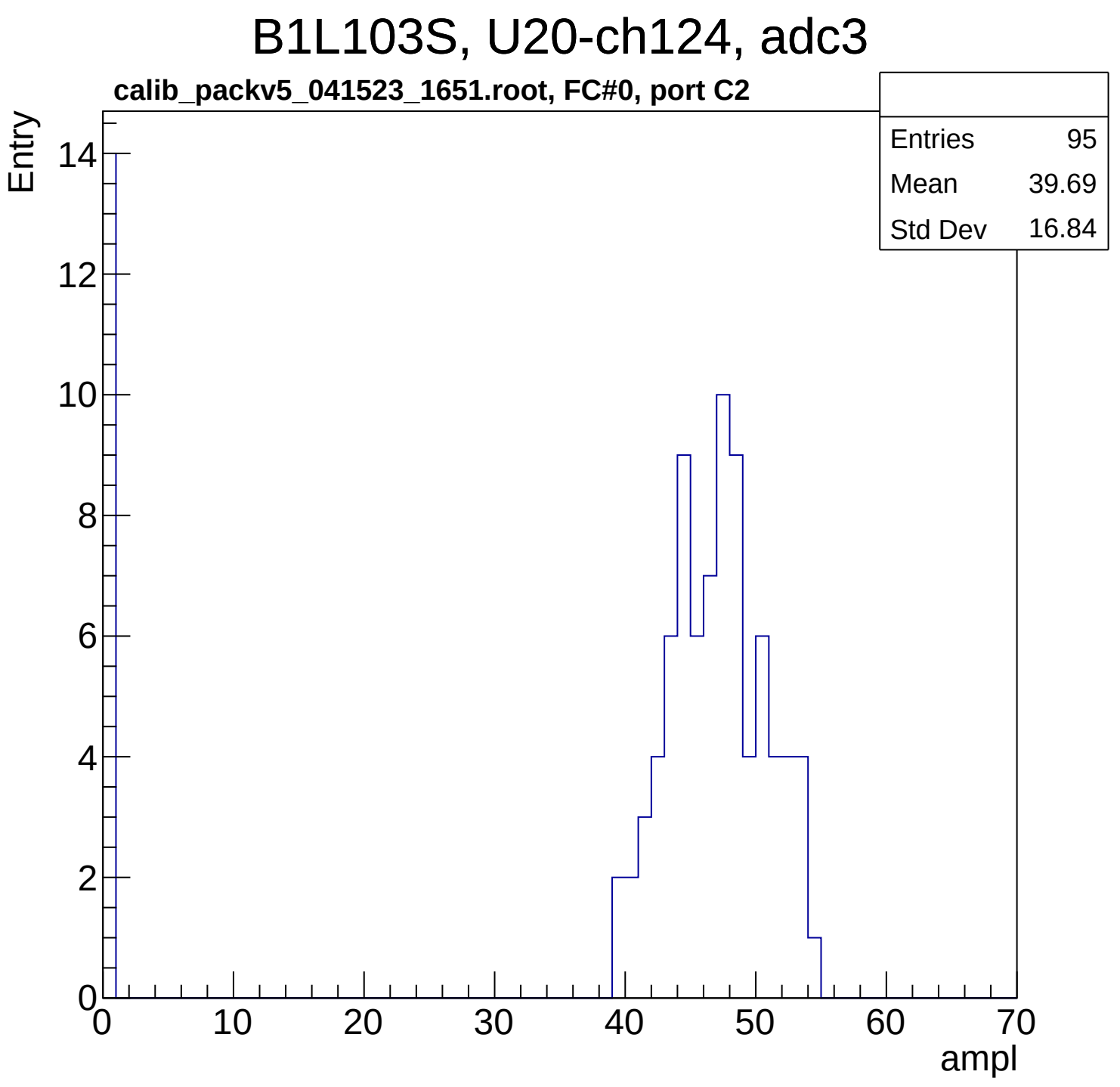
B1L103S, U20-ch124, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 39.69
Std Dev 16.84
Entry
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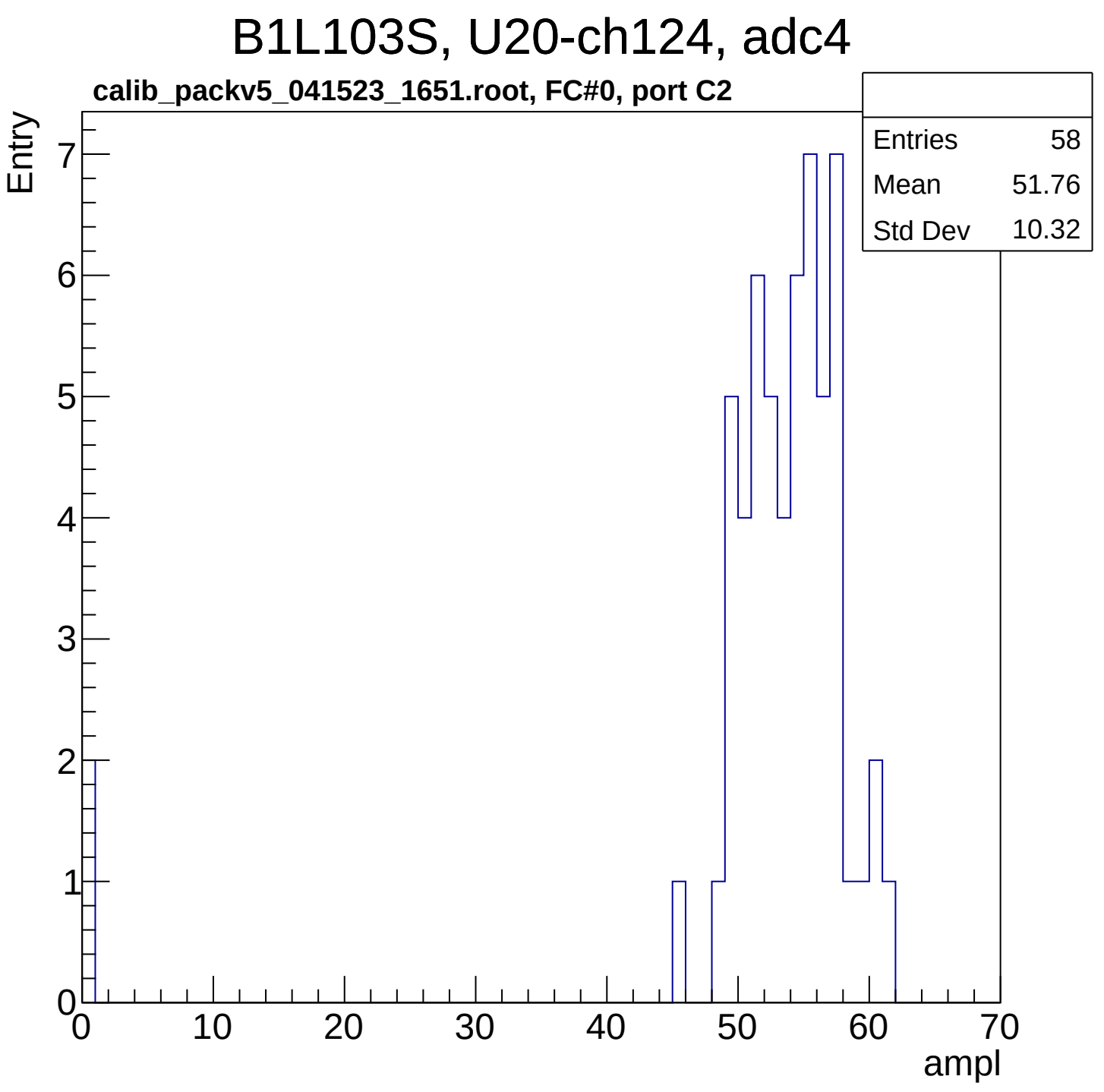
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch124, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 51.76
Std Dev 10.32
Entry
ampl
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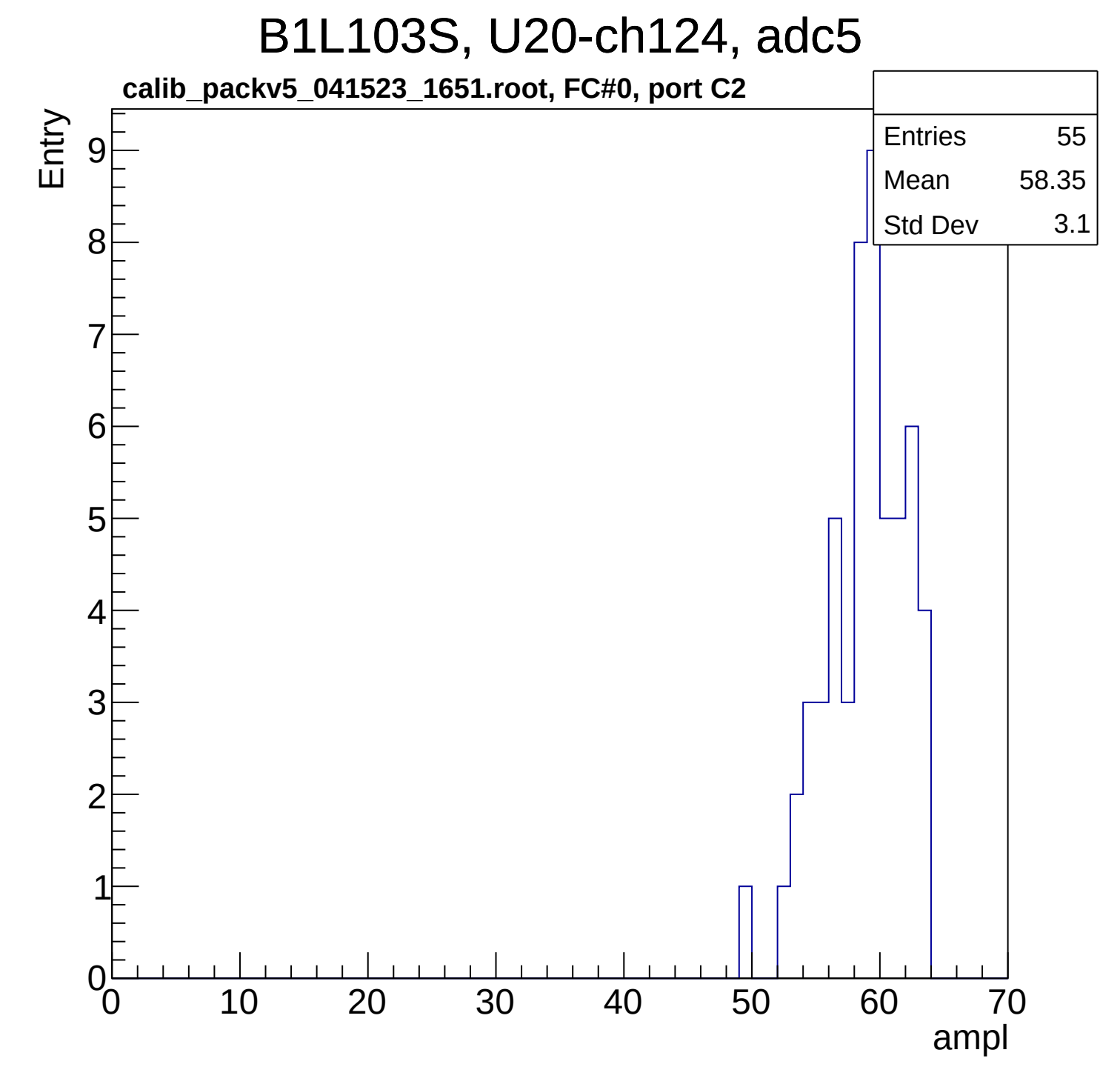
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U20-ch124, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 58.35
Std Dev 3.1
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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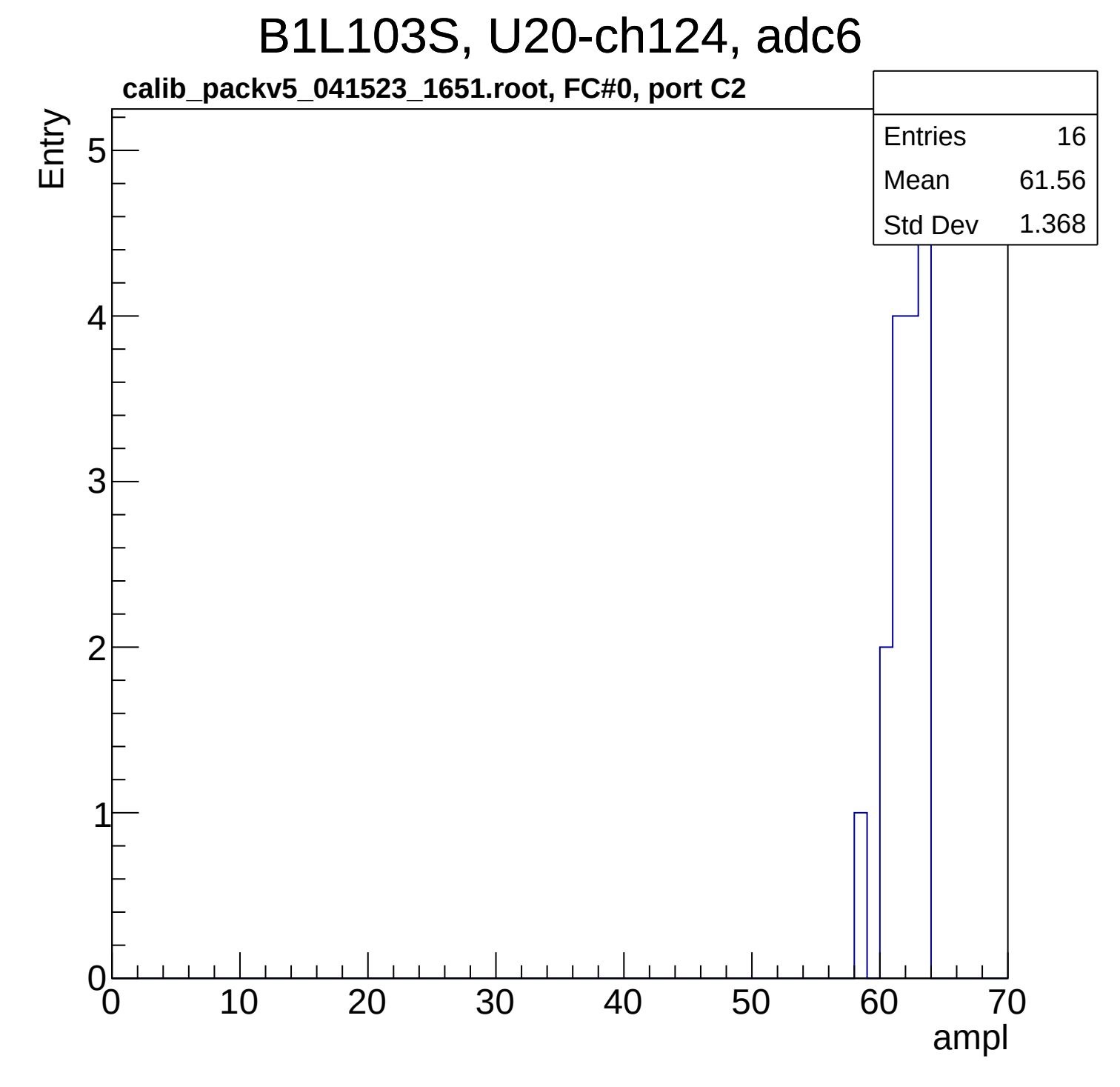
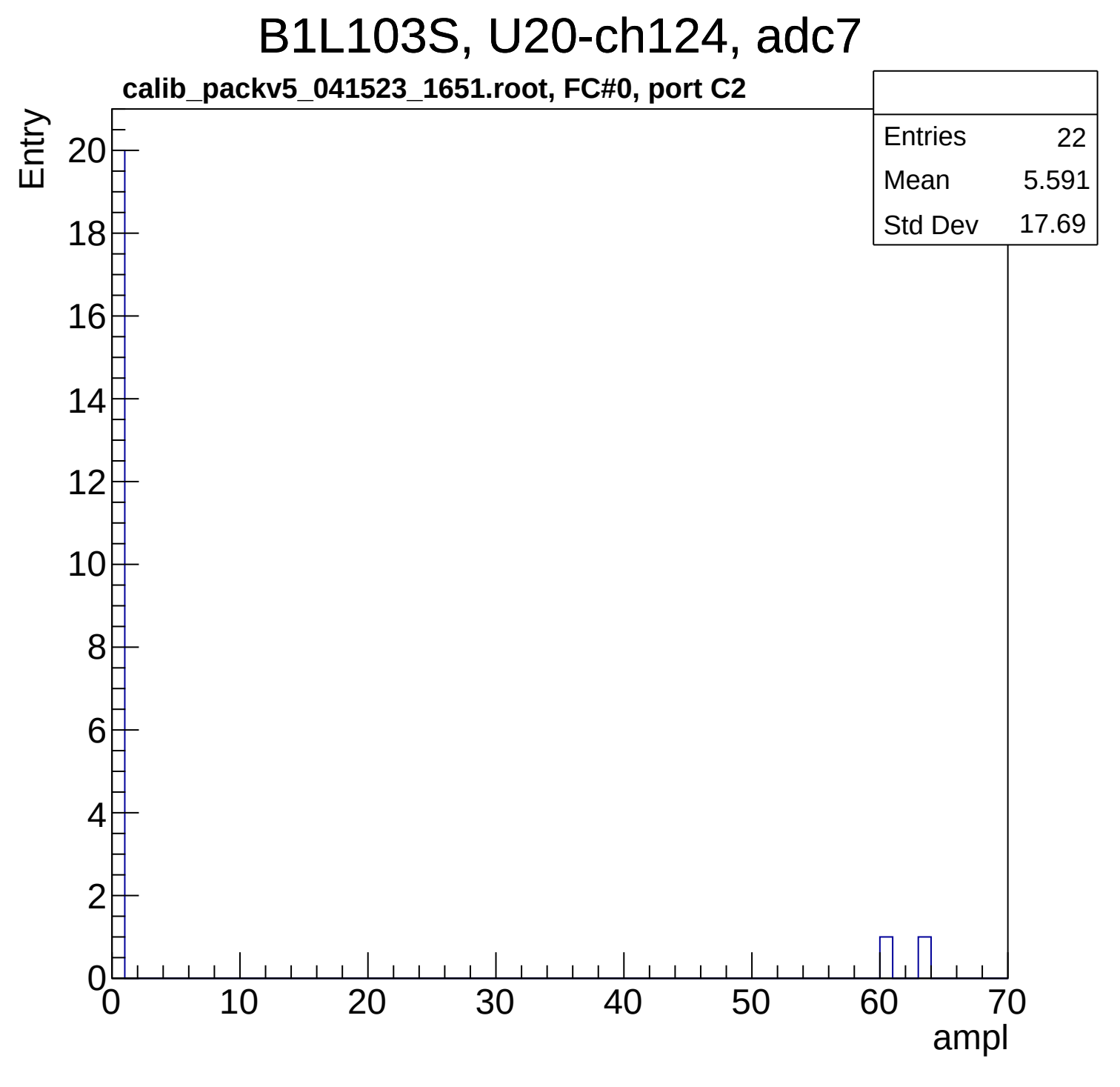
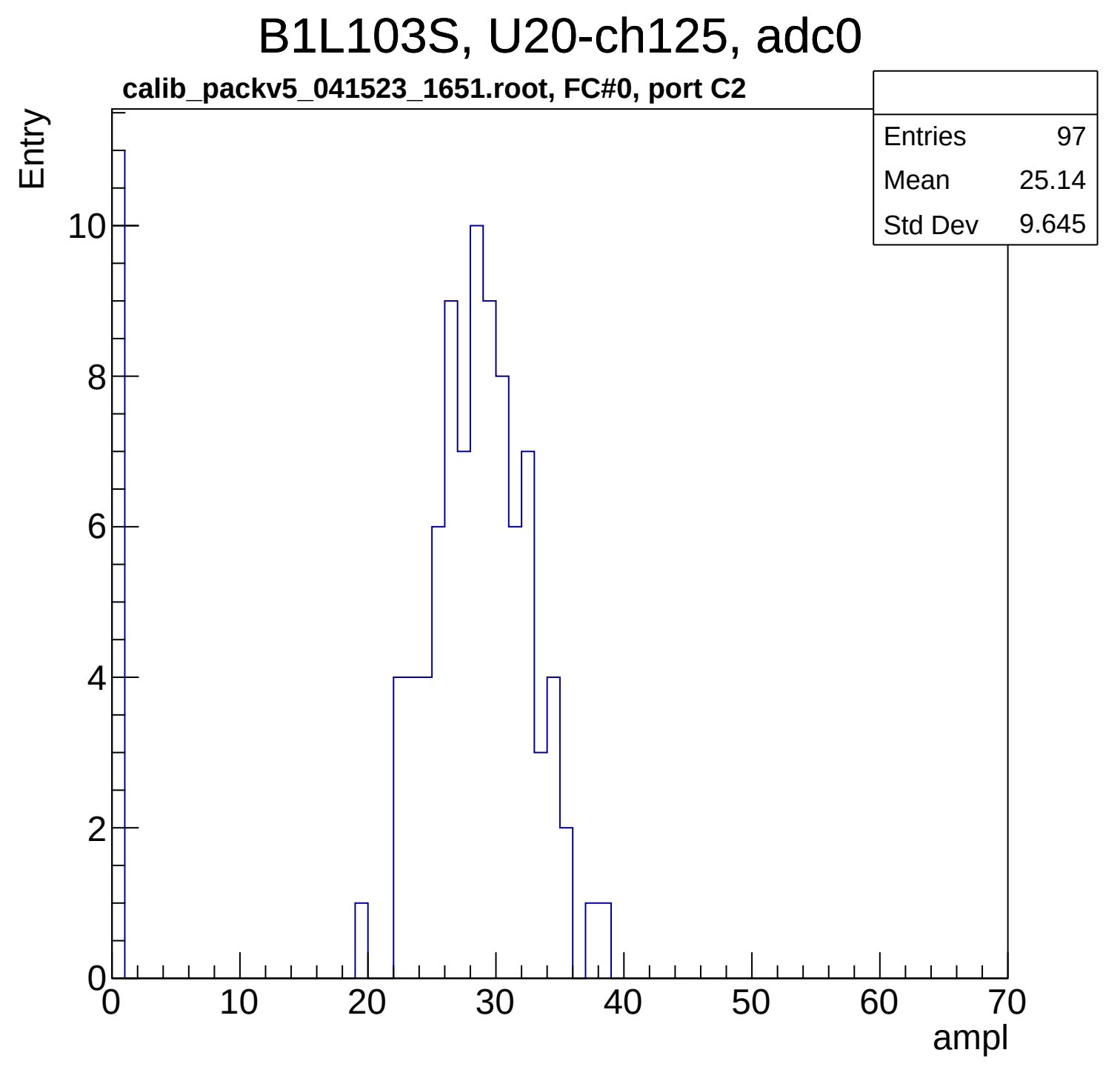
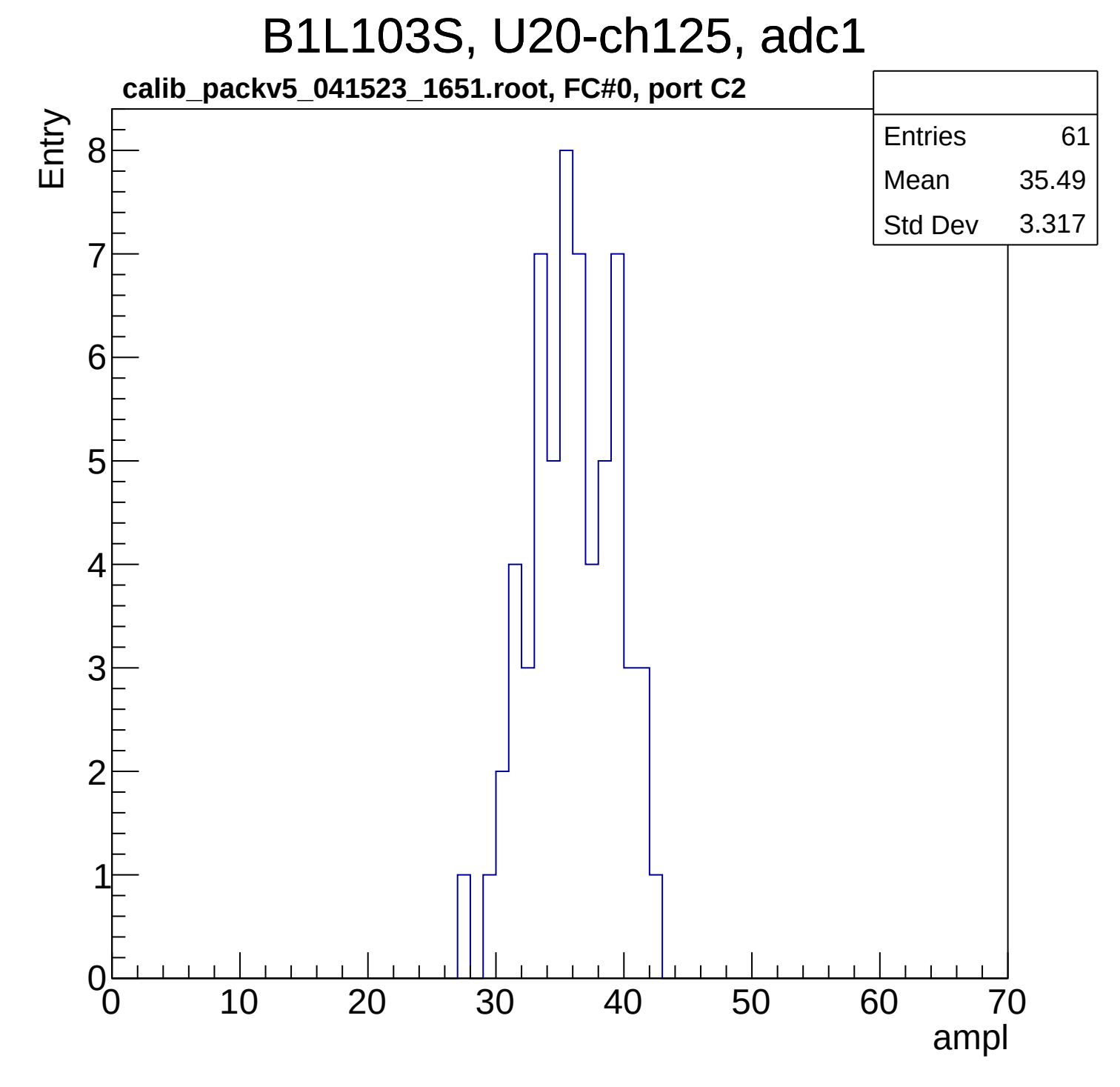
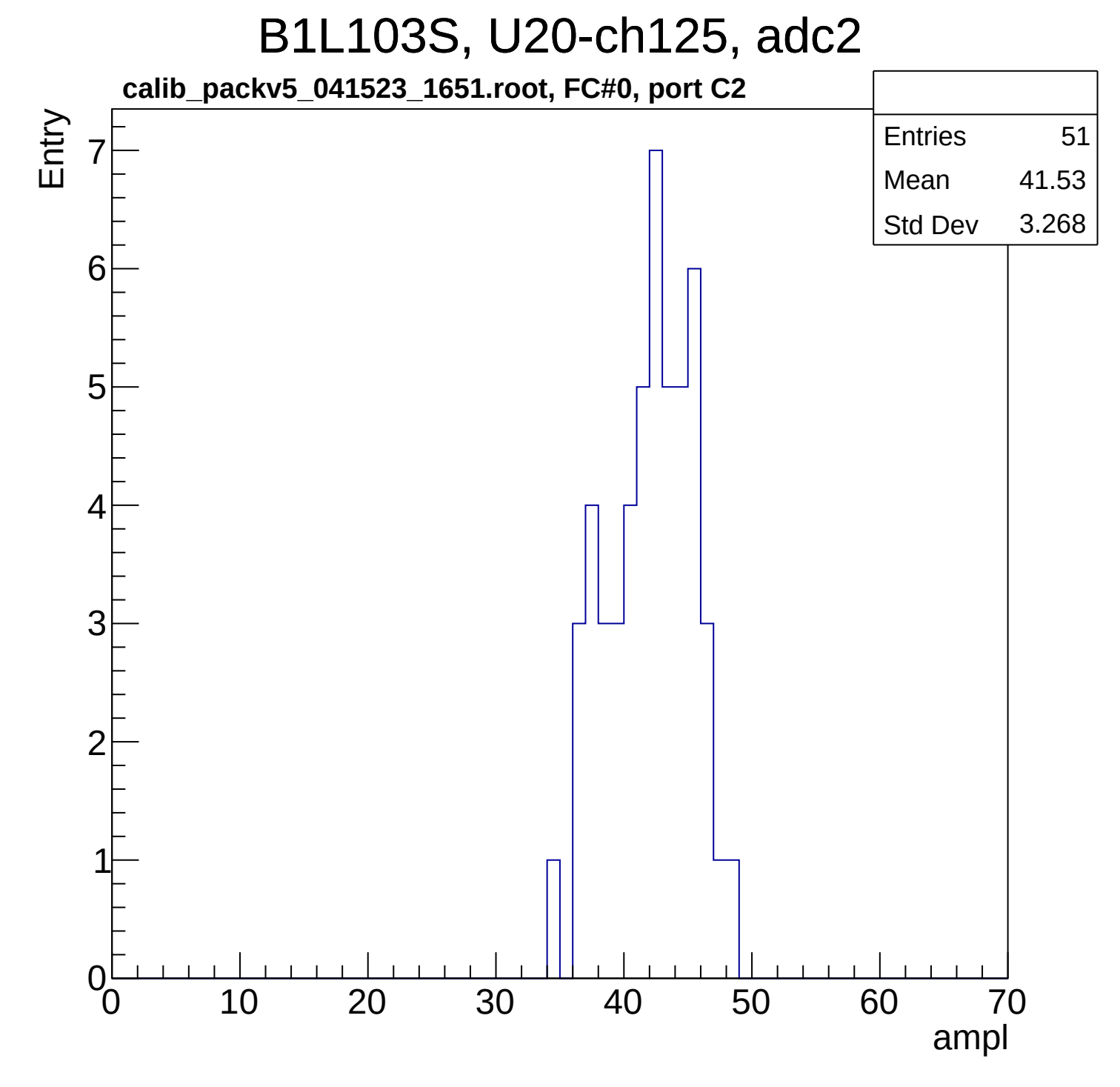
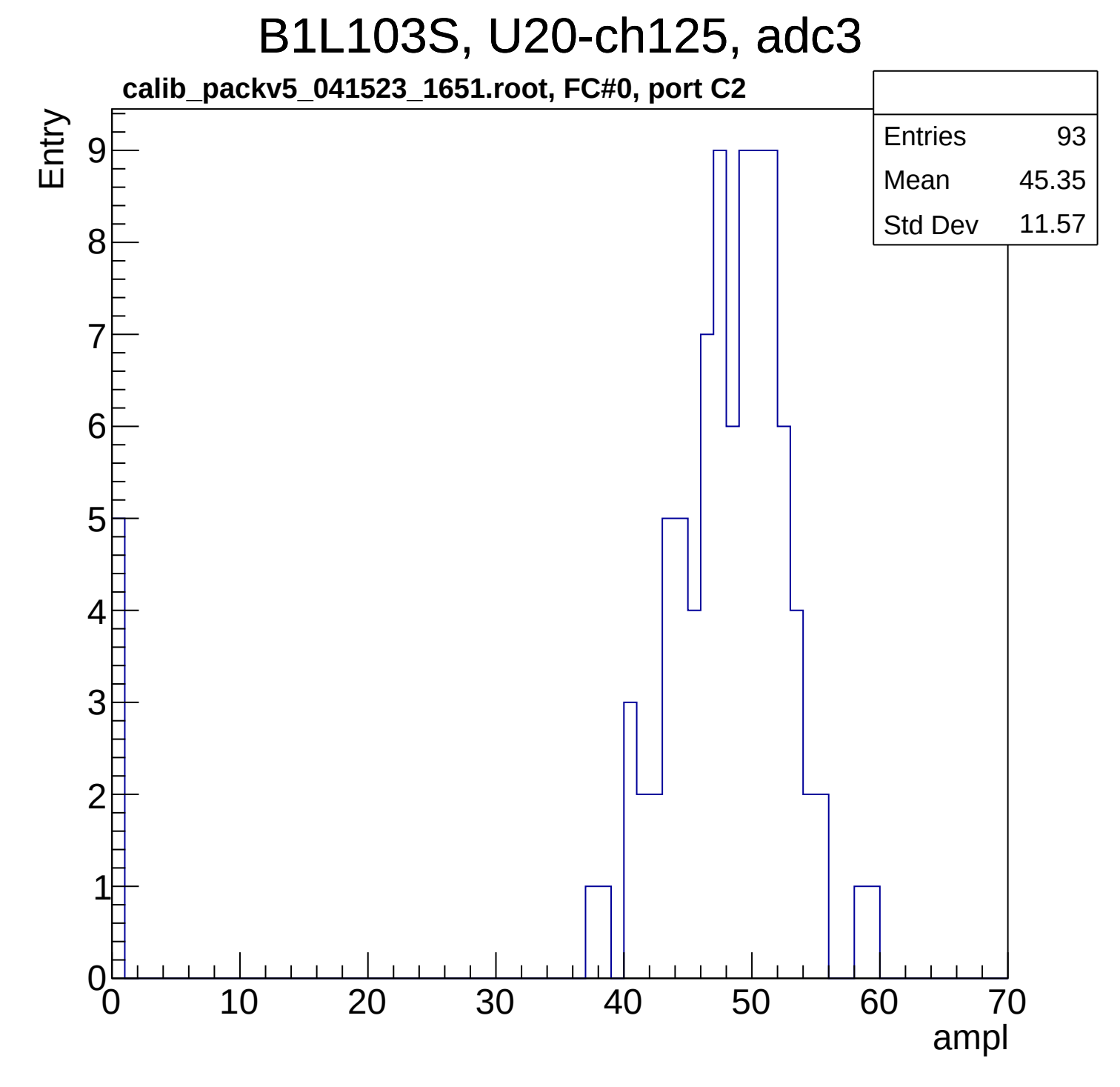

B1L103S, U20-ch124, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 61.56
Std Dev 1.368
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U20-ch124, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 5.591
Std Dev 17.69
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70


B1L103S, U20-ch125, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 25.14
Std Dev 9.645
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U20-ch125, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 35.49
Std Dev 3.317
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch125, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 41.53
Std Dev 3.268
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U20-ch125, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 45.35
Std Dev 11.57
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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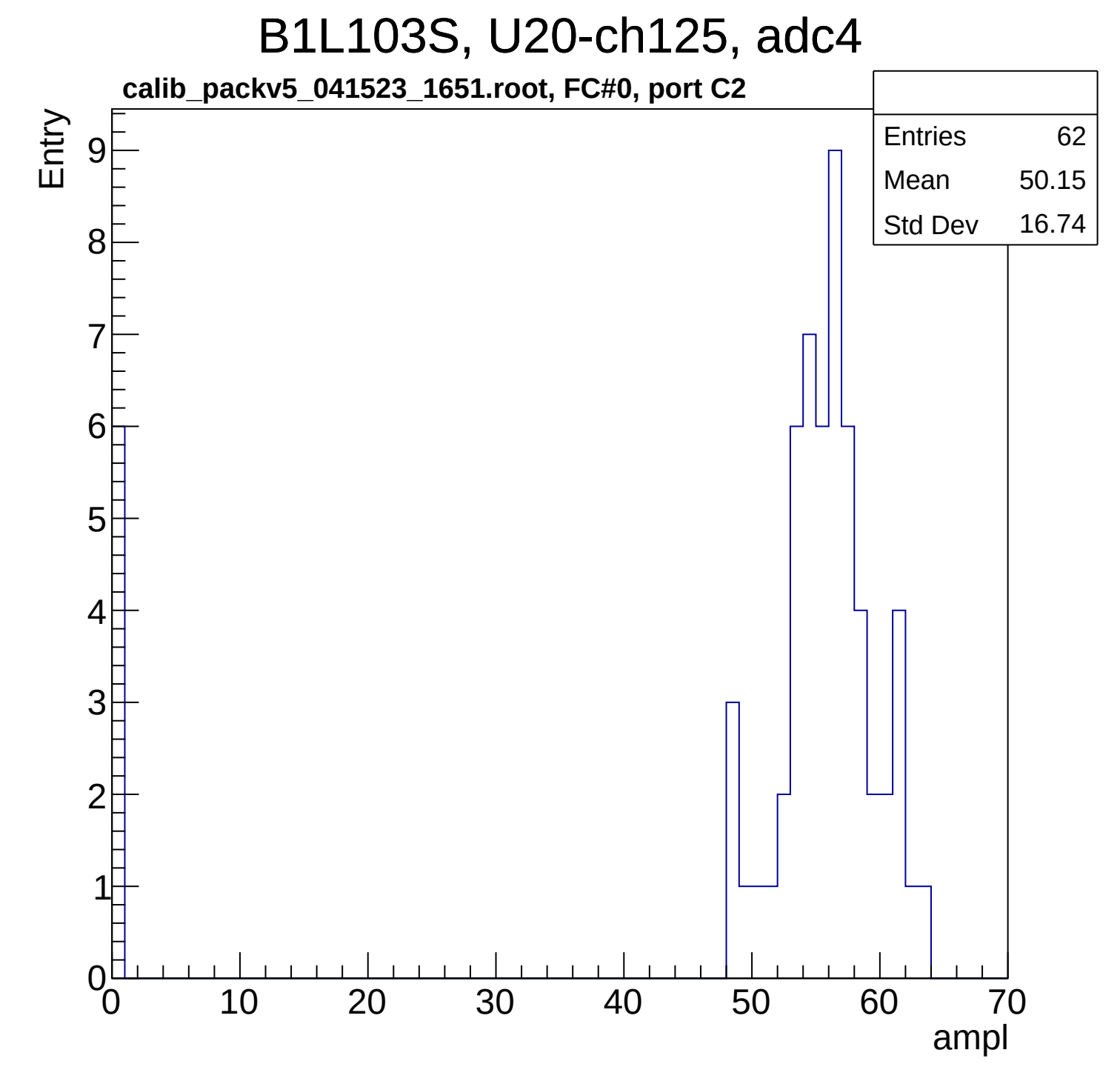
B1L103S, U20-ch125, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 50.15
Std Dev 16.74
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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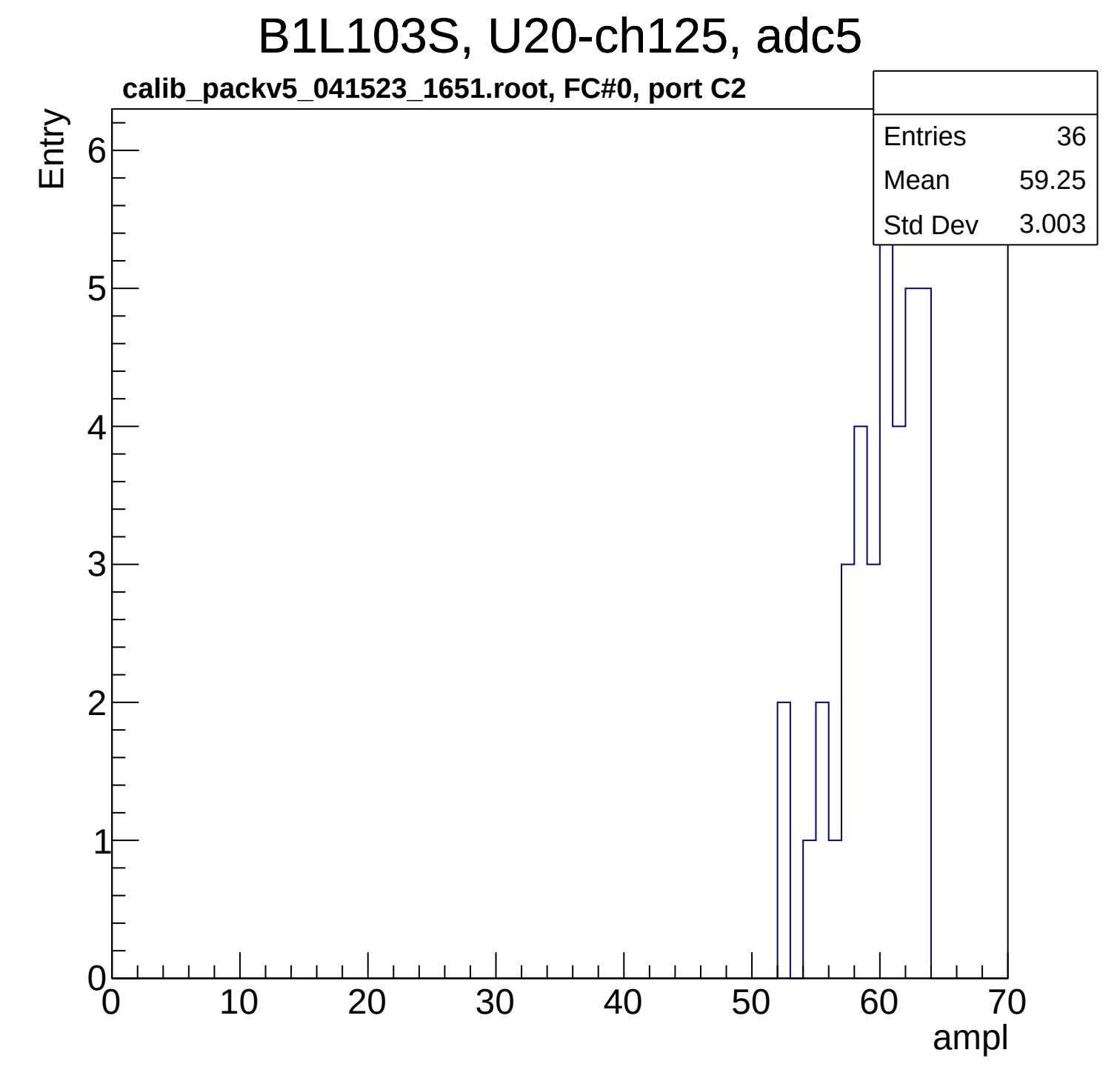
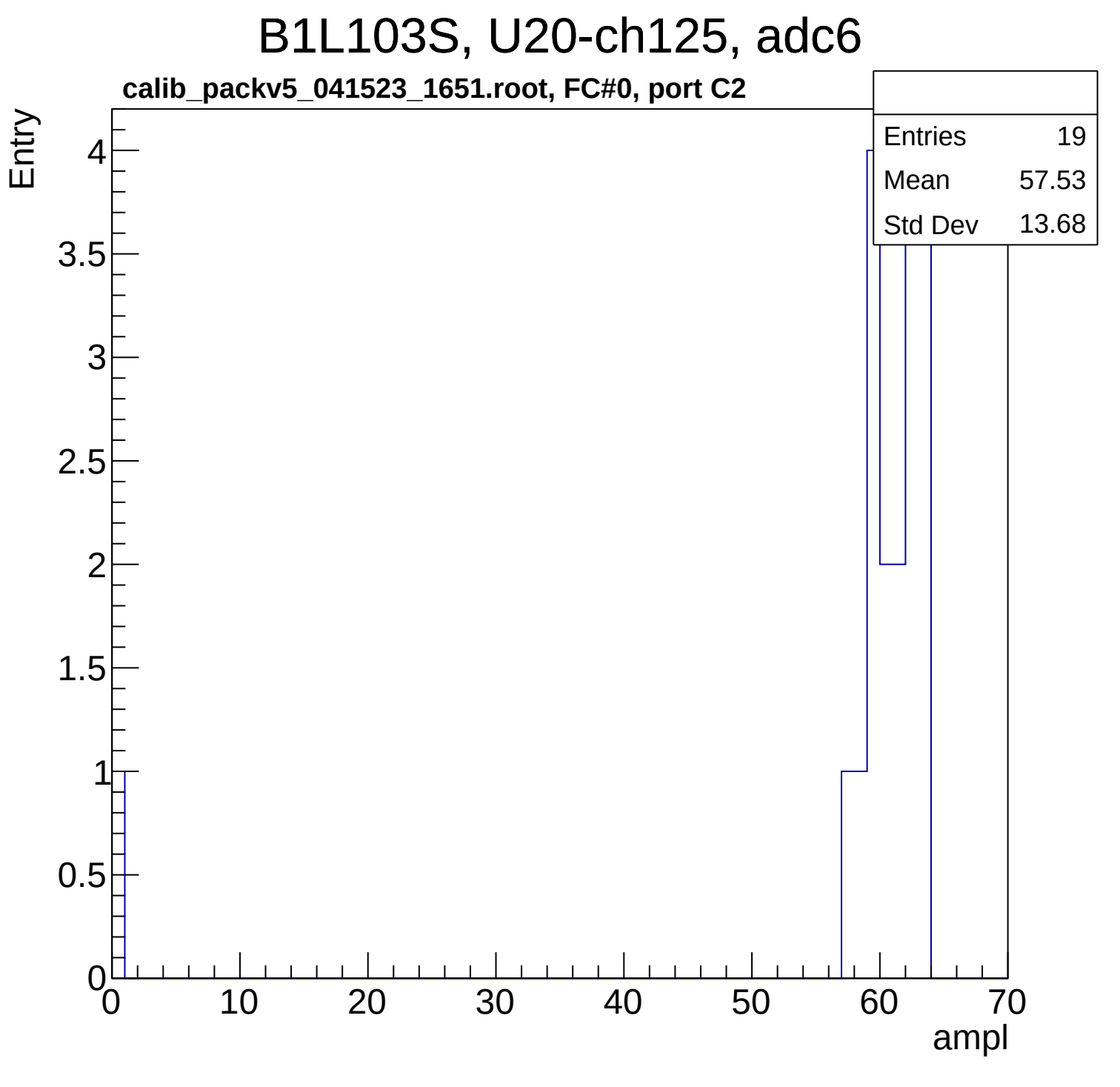
40
50
60
70


B1L103S, U20-ch125, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 59.25
Std Dev 3.003
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U20-ch125, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 57.53
Std Dev 13.68
Entry
ampl
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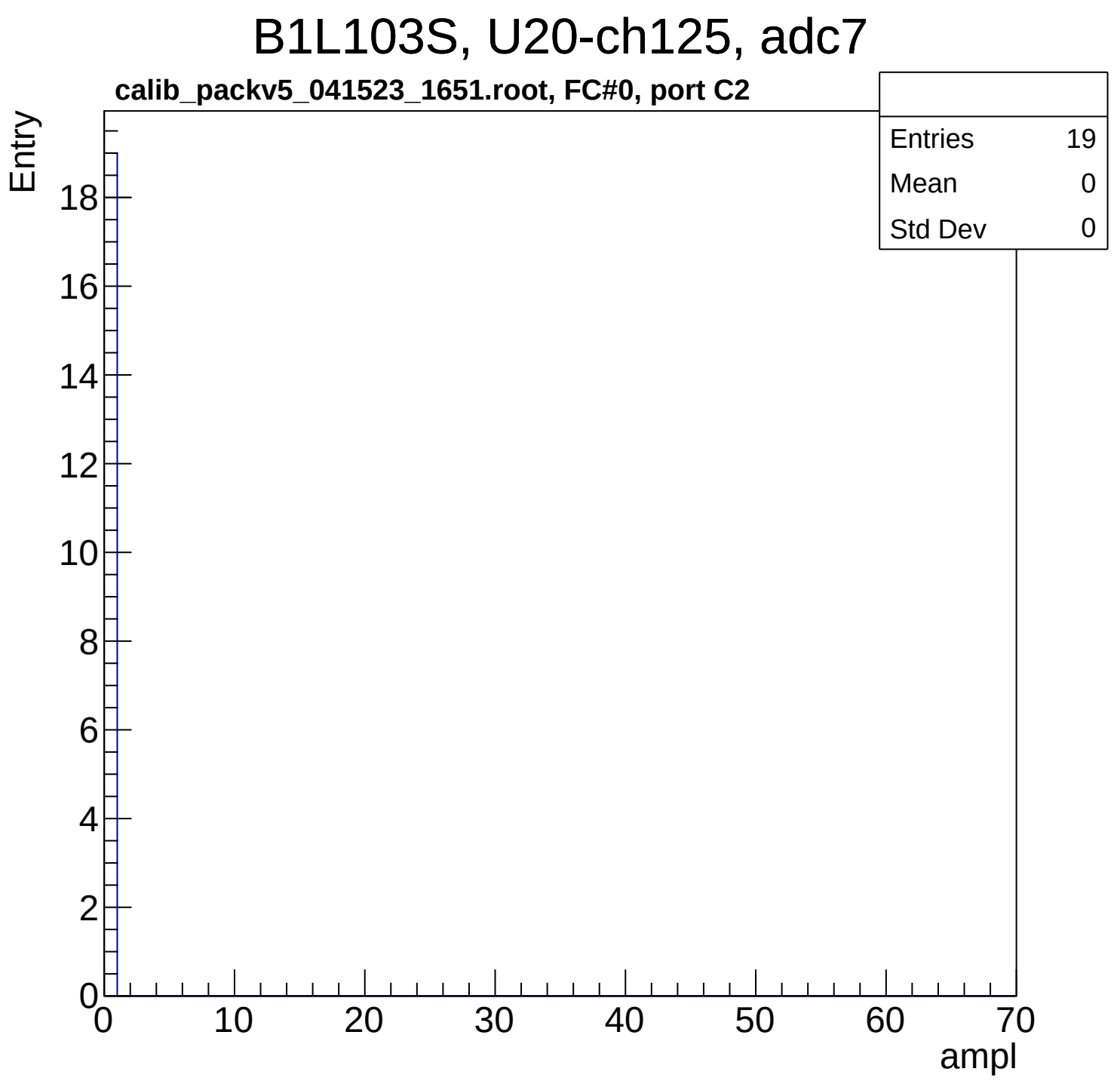
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U20-ch125, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
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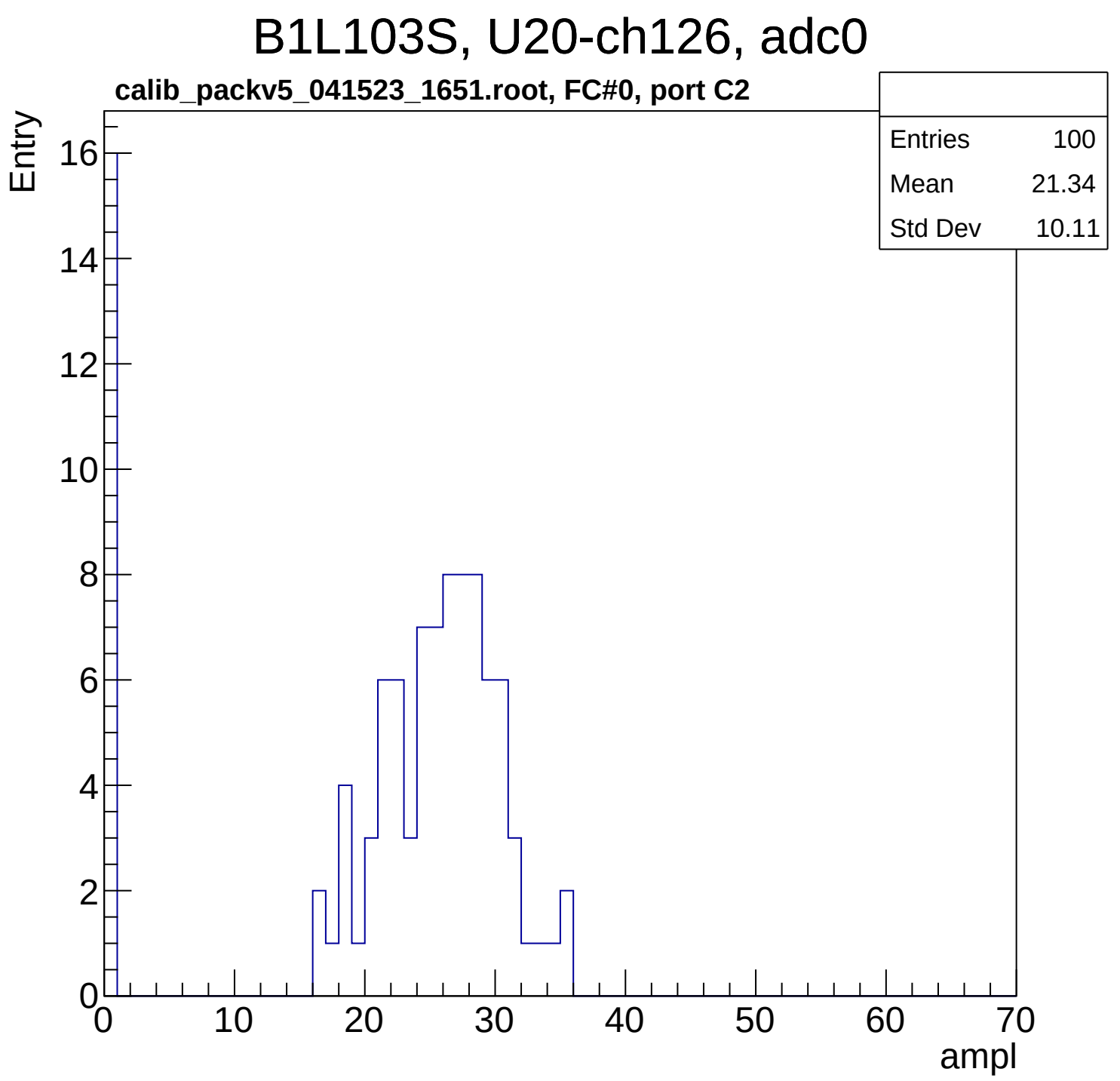
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch126, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 100
Mean 21.34
Std Dev 10.11
Entry
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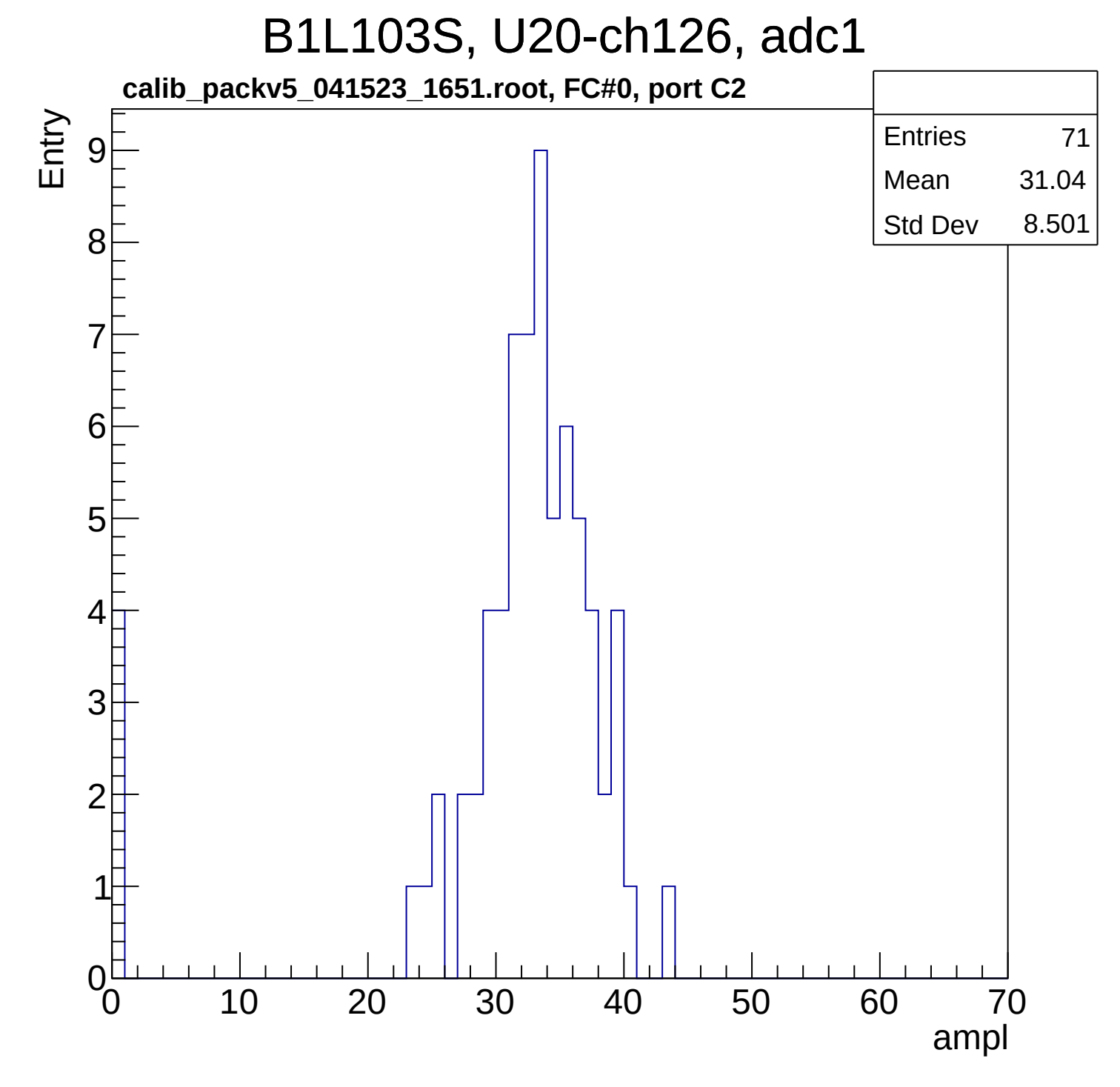
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch126, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 31.04
Std Dev 8.501
Entry
ampl
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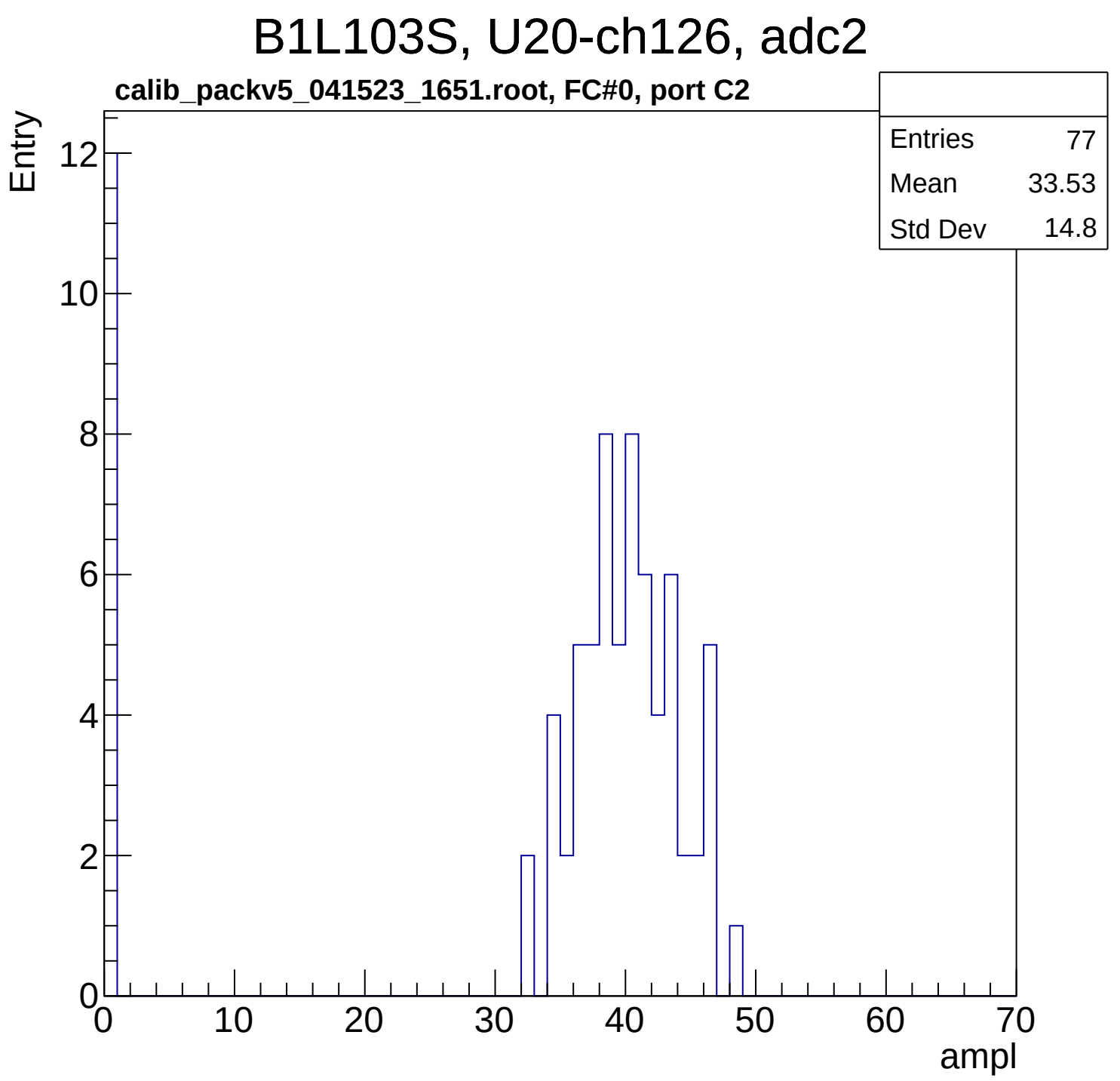
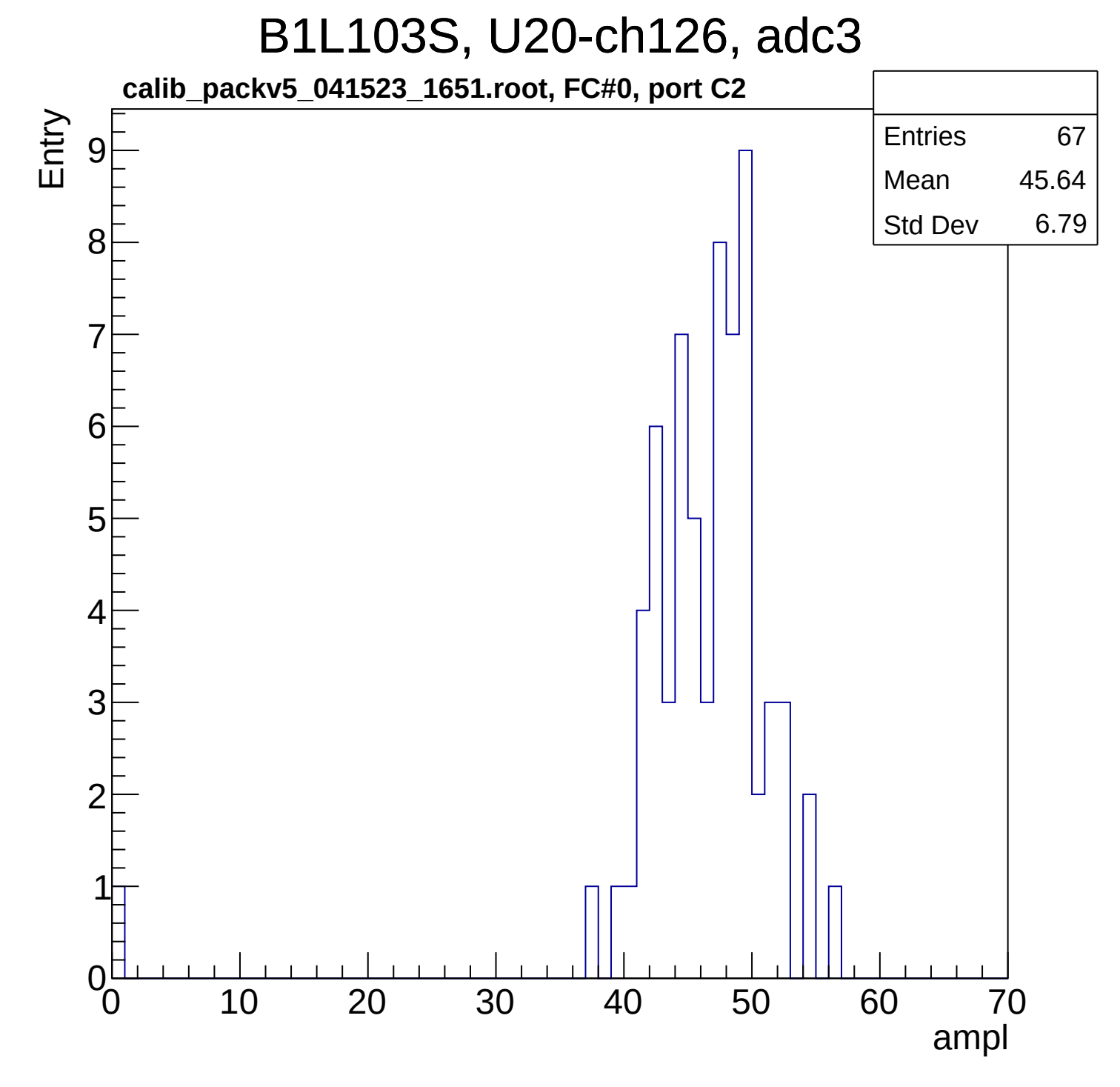
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch126, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 33.53
Std Dev 14.8
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch126, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 45.64
Std Dev 6.79
Entry
ampl
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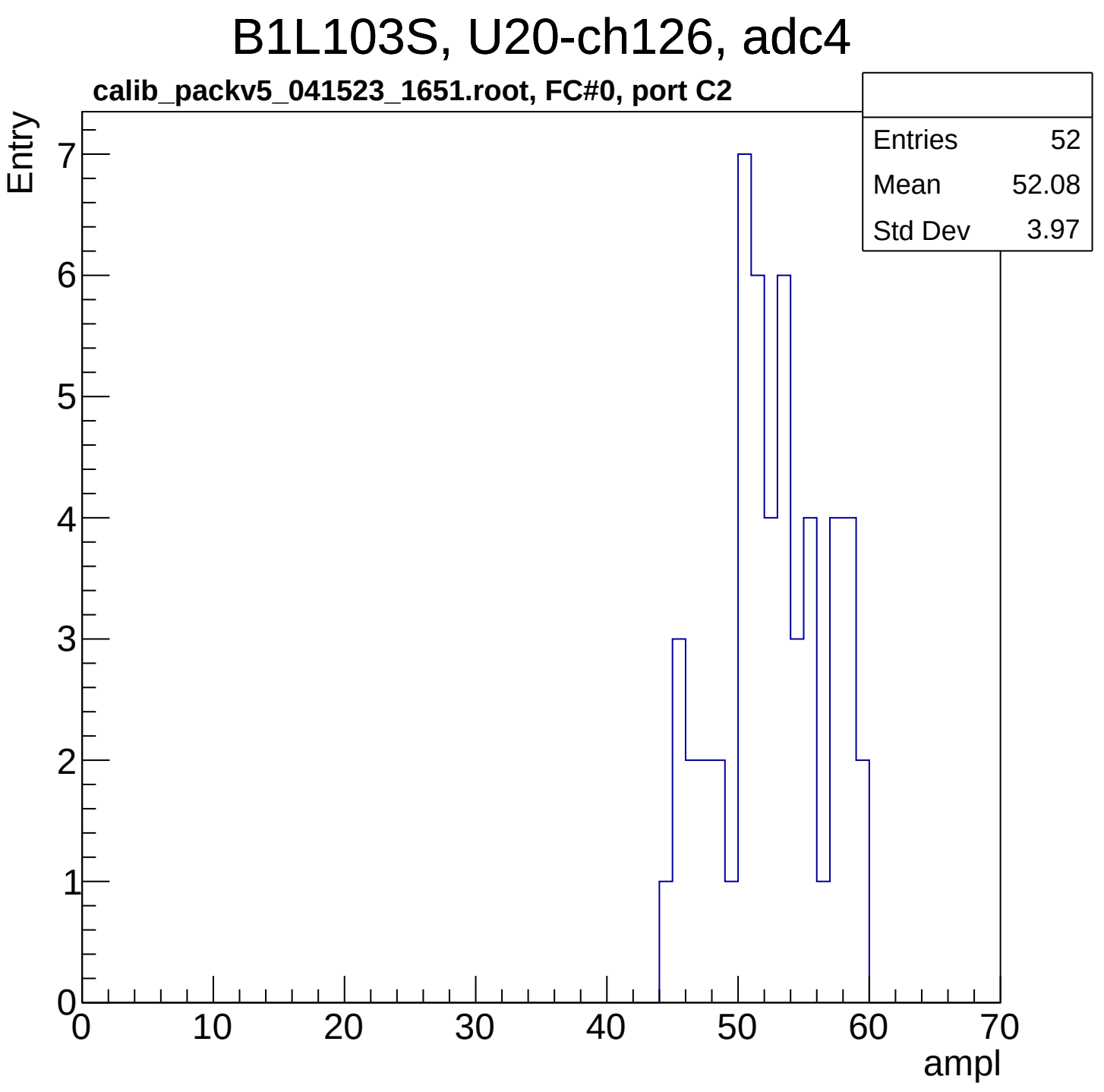
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U20-ch126, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 52.08
Std Dev 3.97
Entry
ampl
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1
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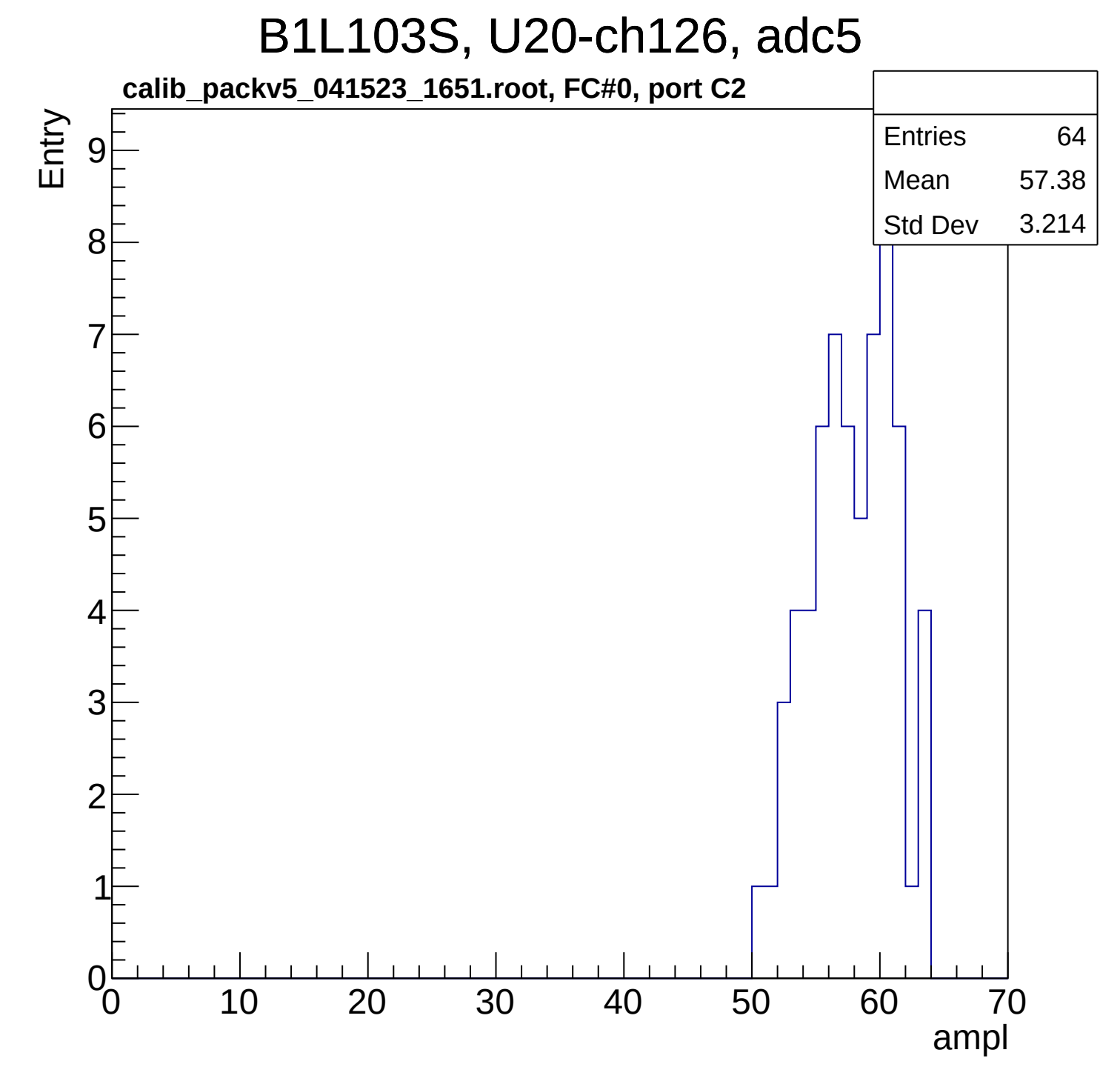
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U20-ch126, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 57.38
Std Dev 3.214
Entry
ampl
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3
4
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6
7
8
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0
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60
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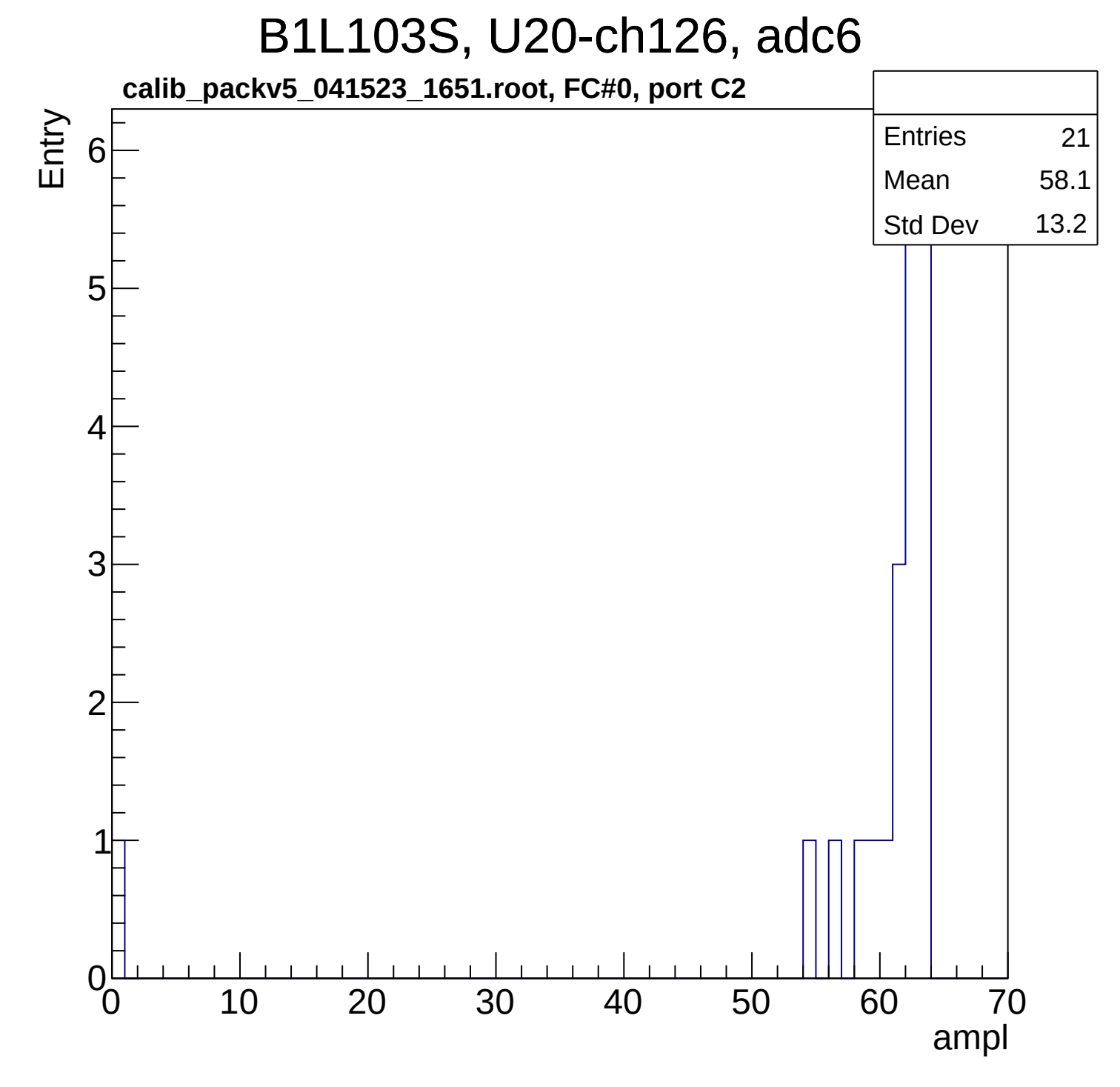
B1L103S, U20-ch126, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 58.1
Std Dev 13.2
Entry
ampl
0
1
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4
5
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0
10
20
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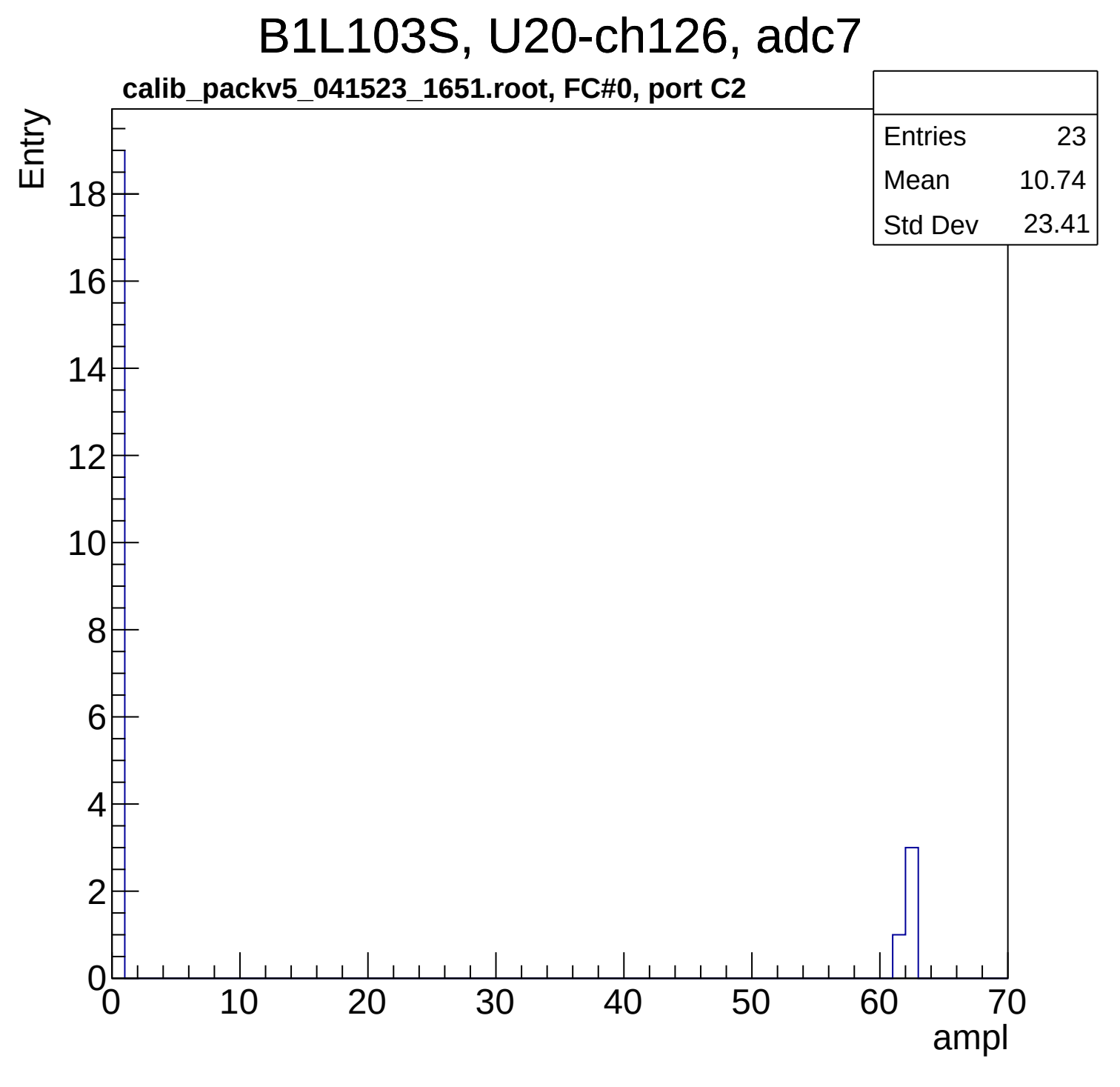
40
50
60
70


B1L103S, U20-ch126, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 10.74
Std Dev 23.41
Entry
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8
10
12
14
16
18
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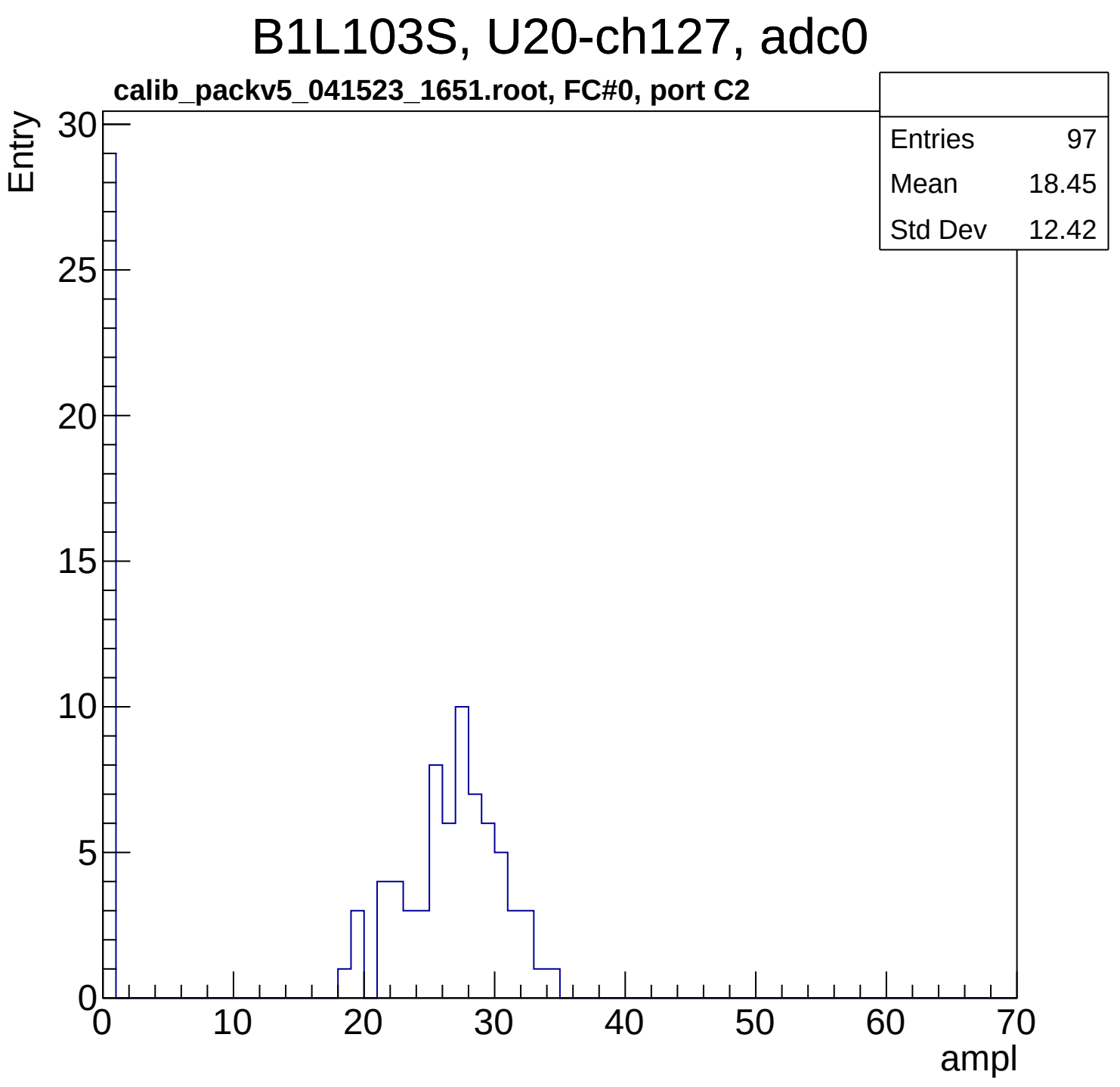
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch127, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 18.45
Std Dev 12.42
Entry
ampl
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5
10
15
20
25
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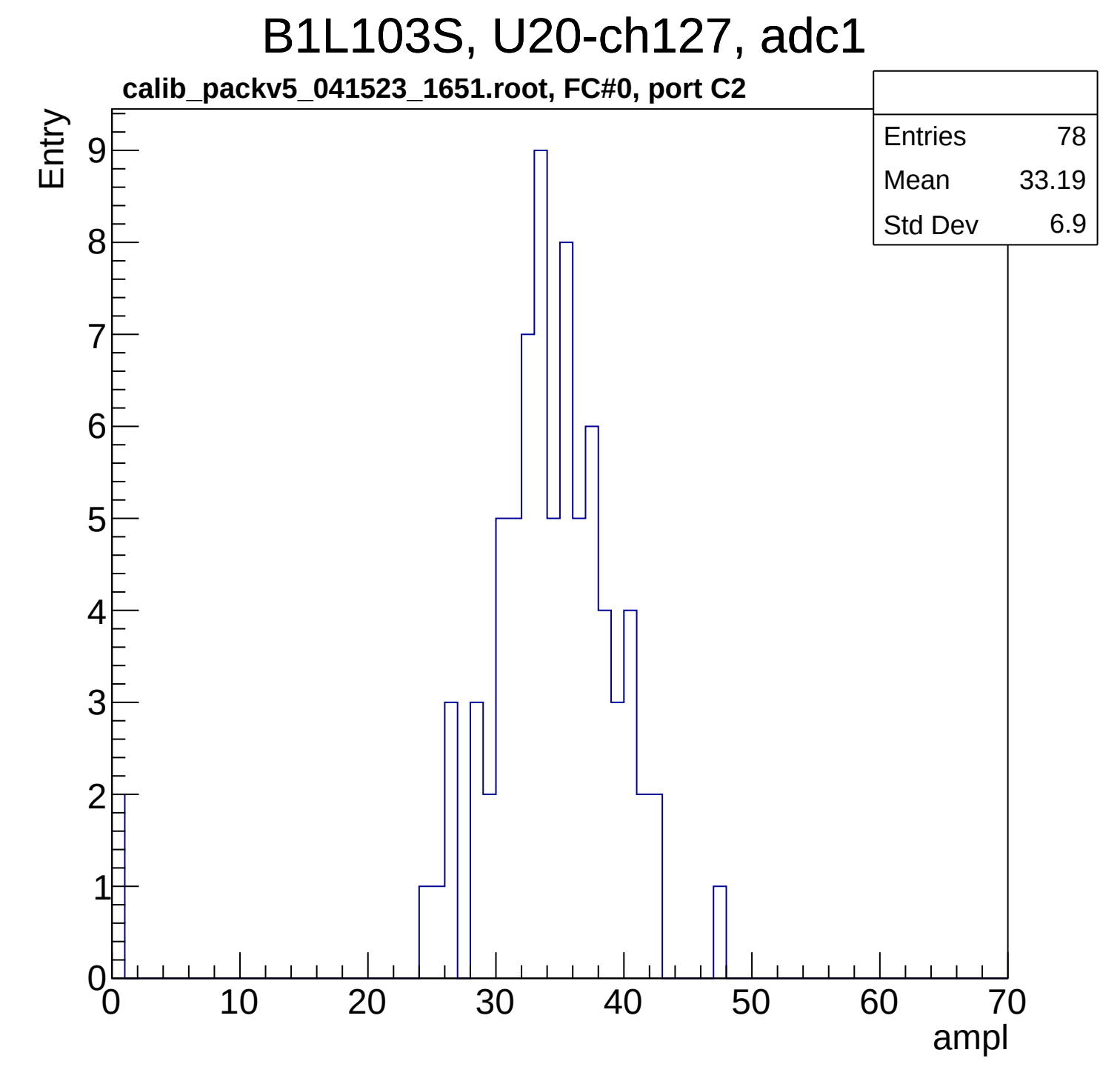
0
10
20
30
40
50
60
70


B1L103S, U20-ch127, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 33.19
Std Dev 6.9
Entry
ampl
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2
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6
7
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60
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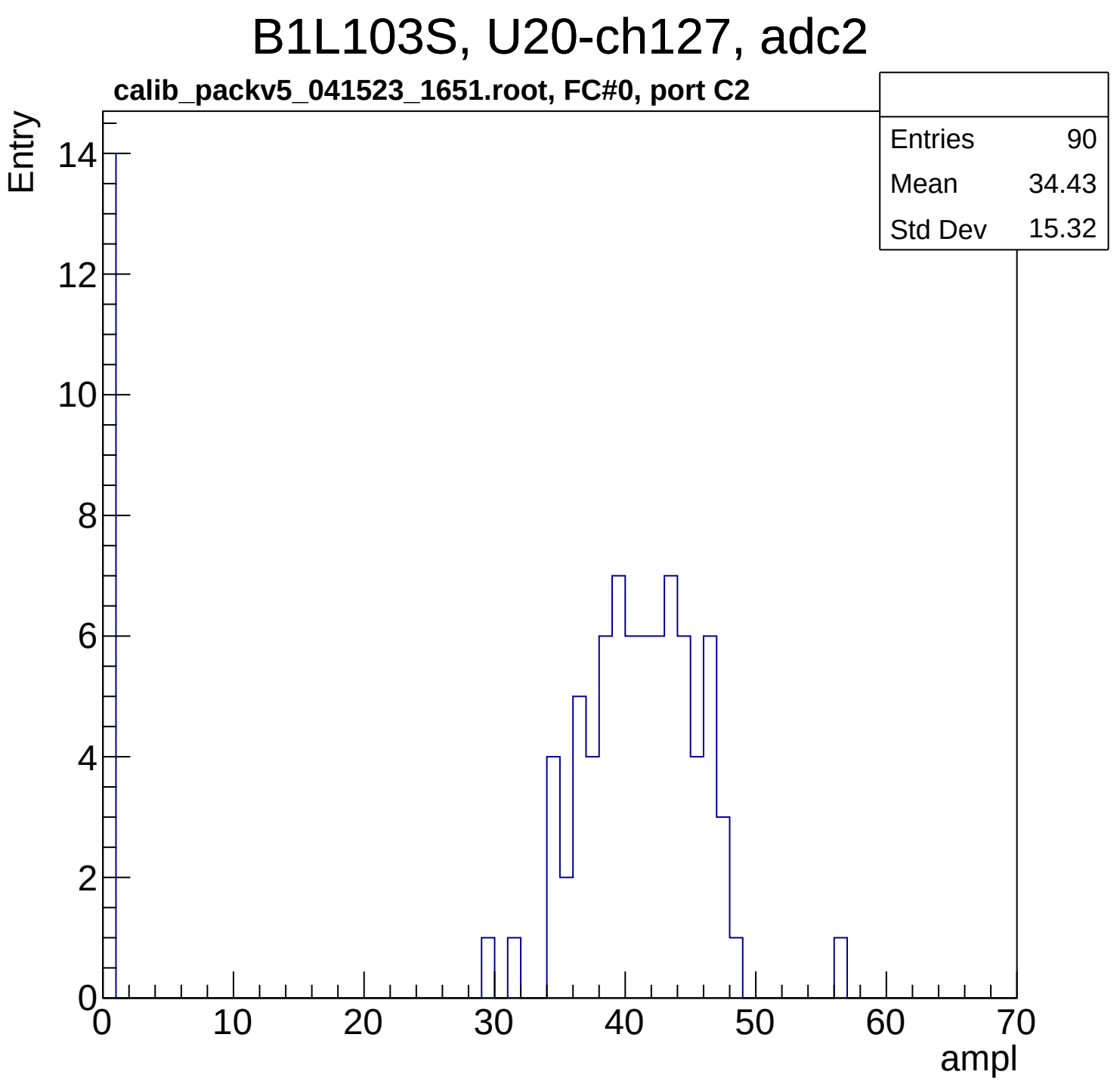
B1L103S, U20-ch127, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 34.43
Std Dev 15.32
Entry
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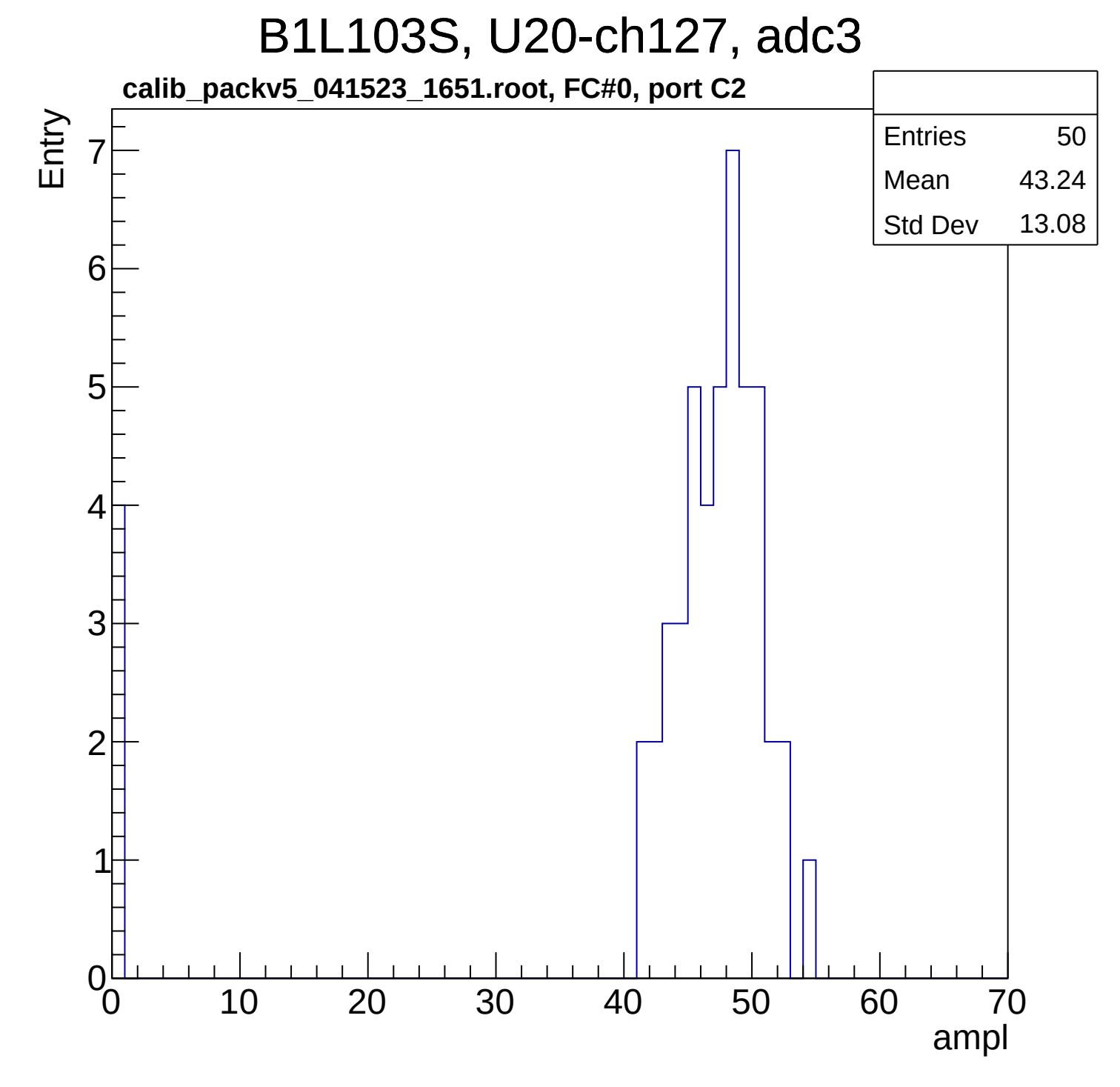
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch127, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 43.24
Std Dev 13.08
Entry
ampl
0
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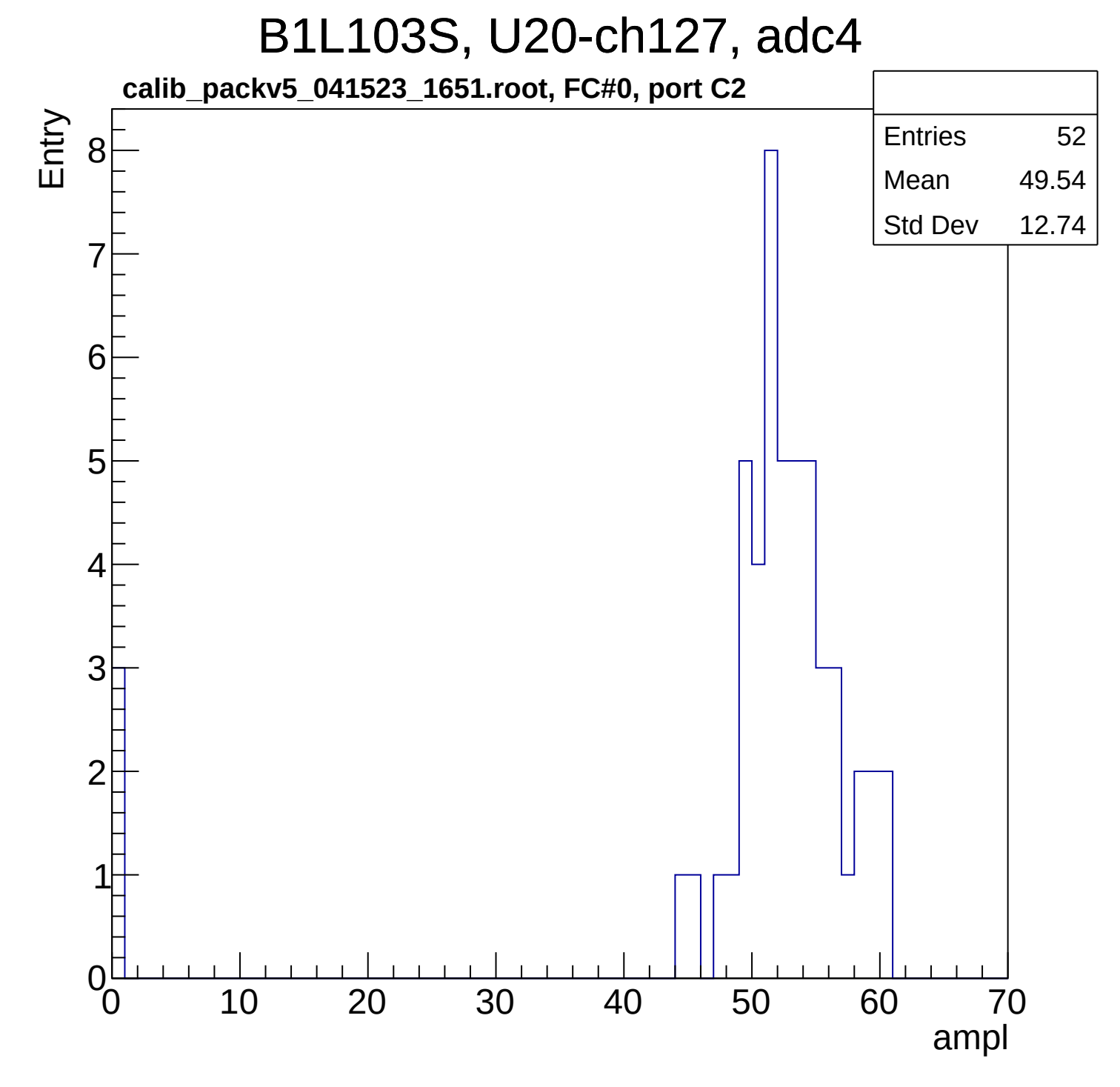
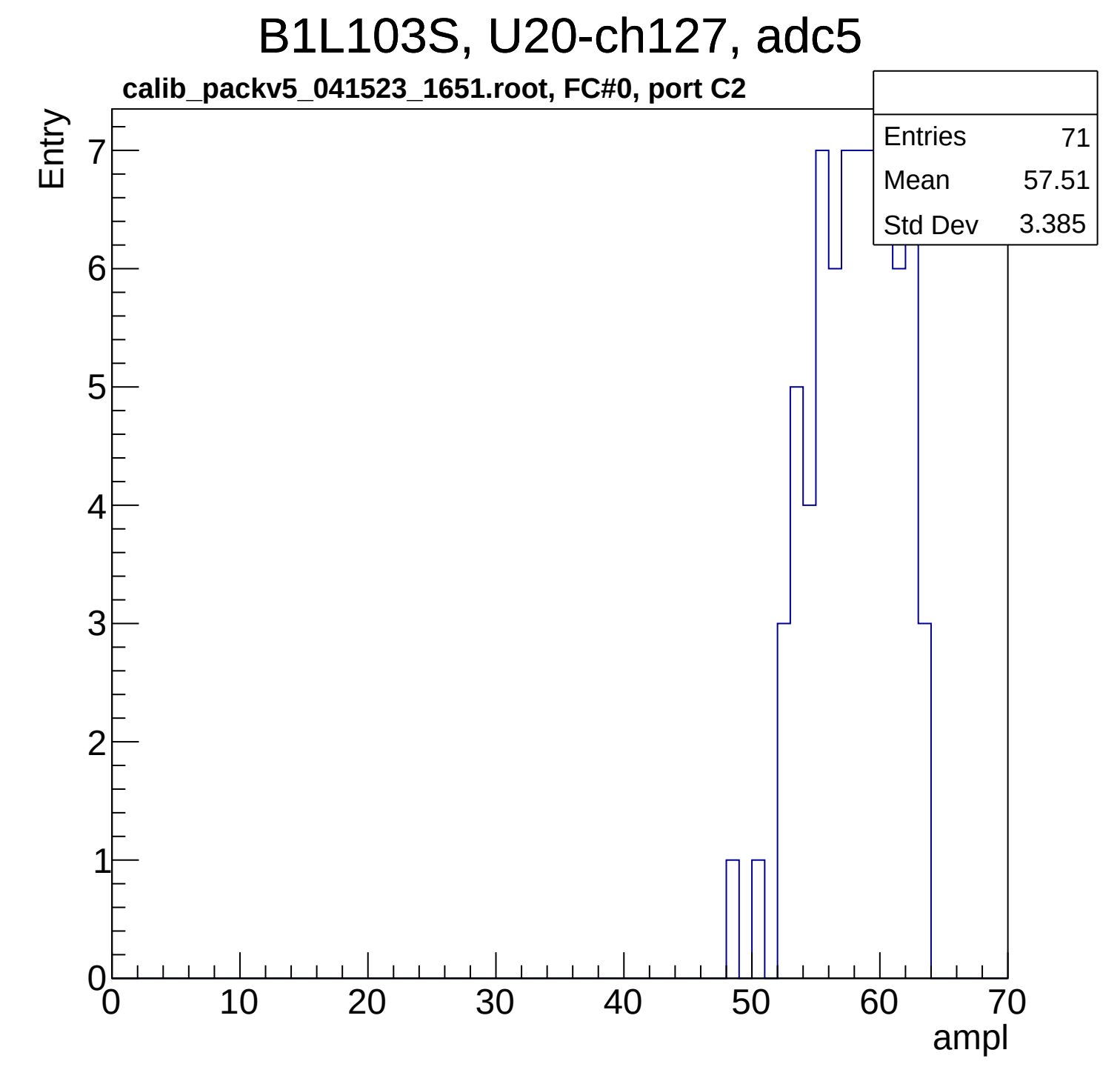
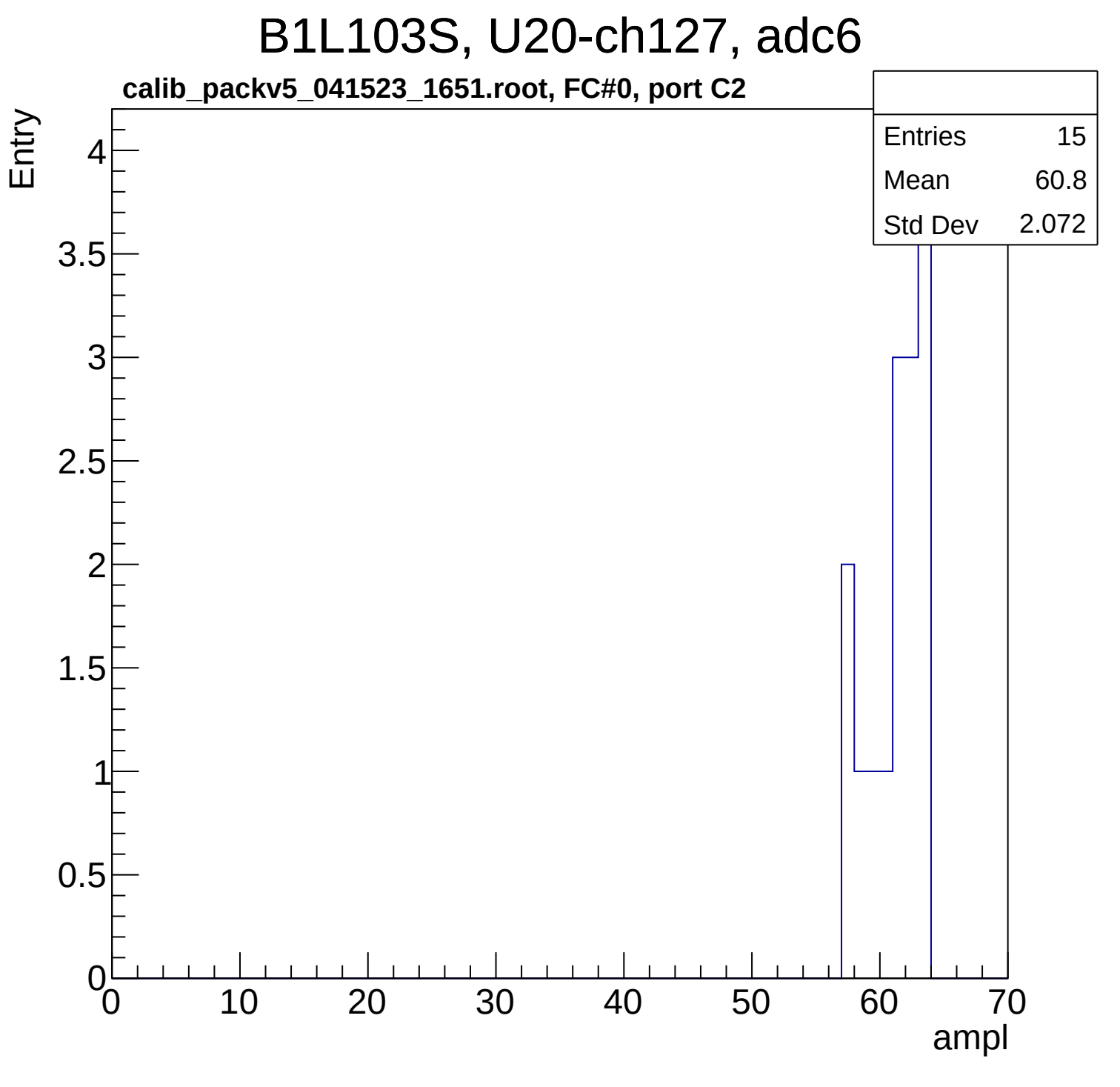
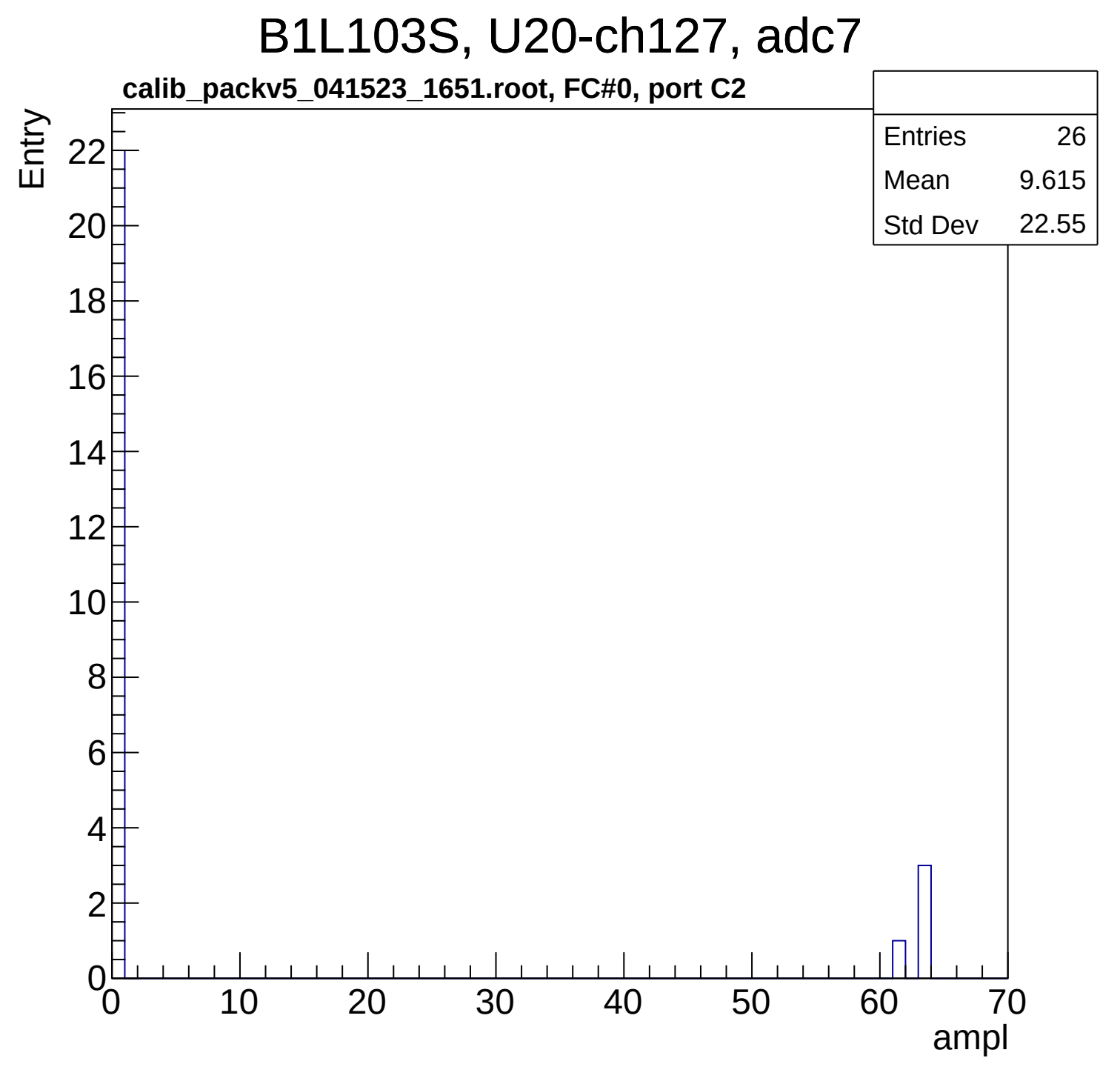
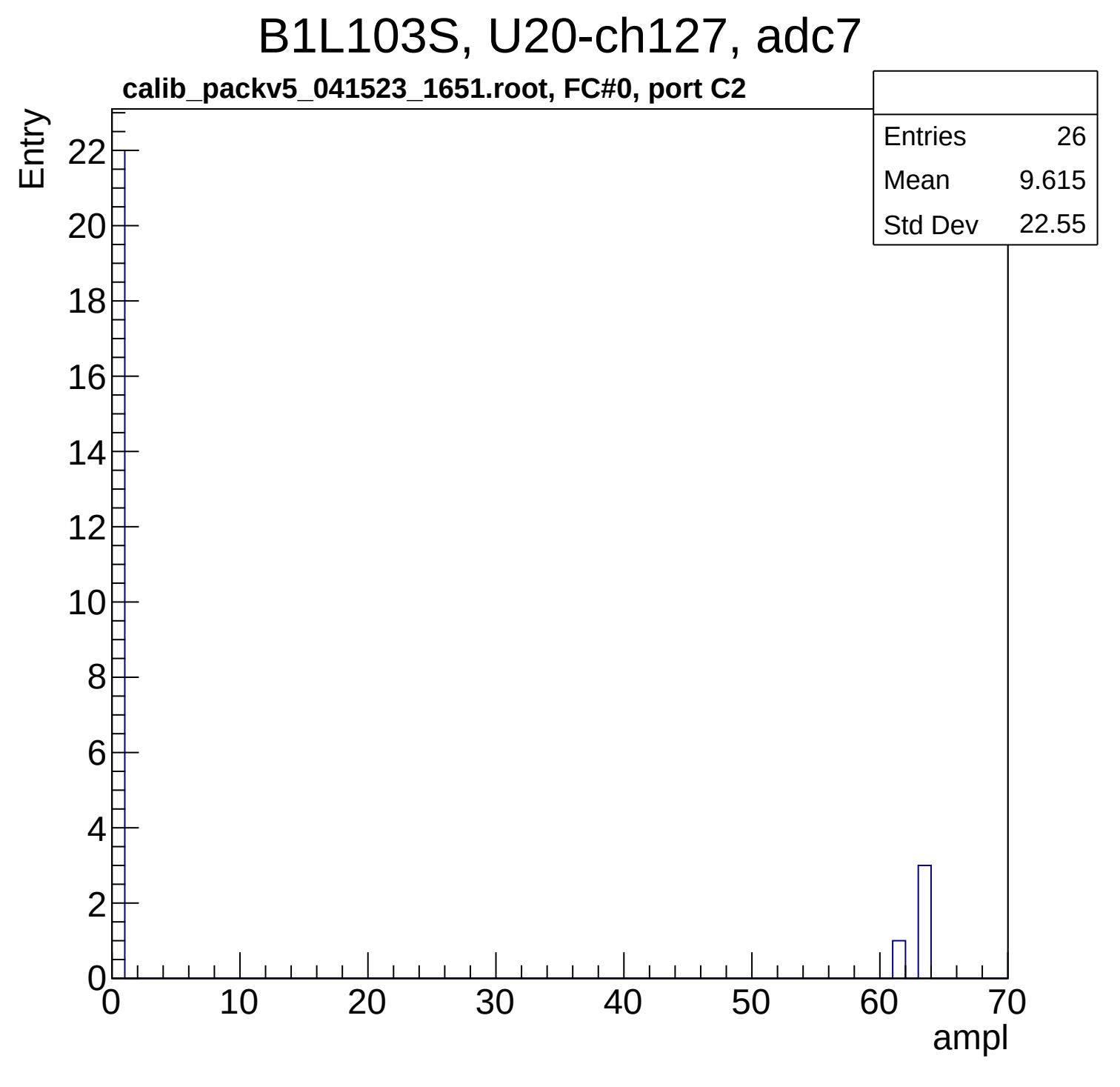
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U20-ch127, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 49.54
Std Dev 12.74
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U20-ch127, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 57.51
Std Dev 3.385
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U20-ch127, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 60.8
Std Dev 2.072
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U20-ch127, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 9.615
Std Dev 22.55
Entry
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70
ampl


B1L103S, U20-ch127, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 9.615
Std Dev 22.55
Entry
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70
ampl