



# B1L103S, U1-ch82

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 554   |
| Mean    | 32.39 |
| Std Dev | 20.69 |

Turn on : 22.2209

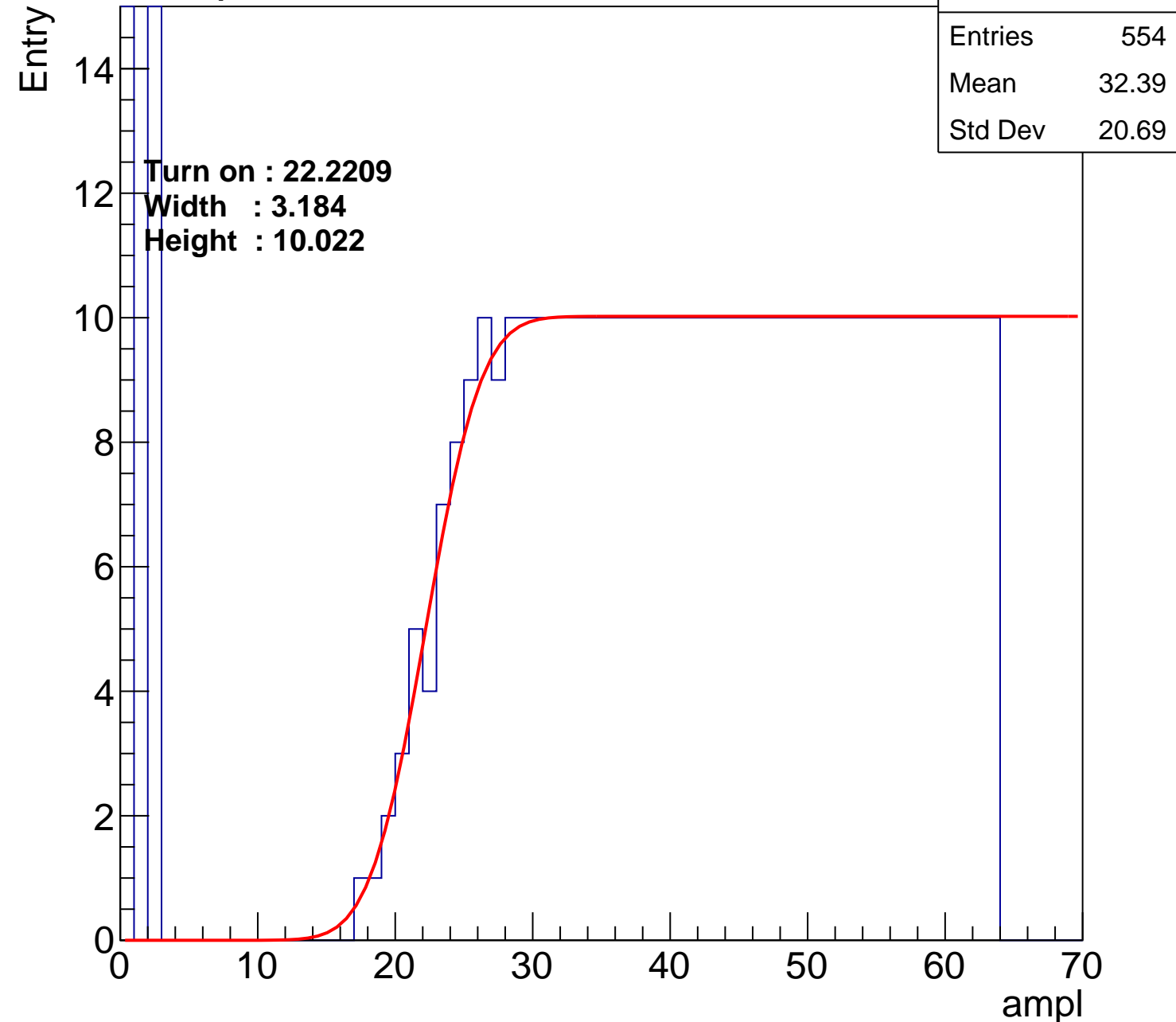
Width : 3.184

Height : 10.022

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U2-ch82

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 521   |
| Mean    | 33.38 |
| Std Dev | 20.85 |

Turn on : 24.7664

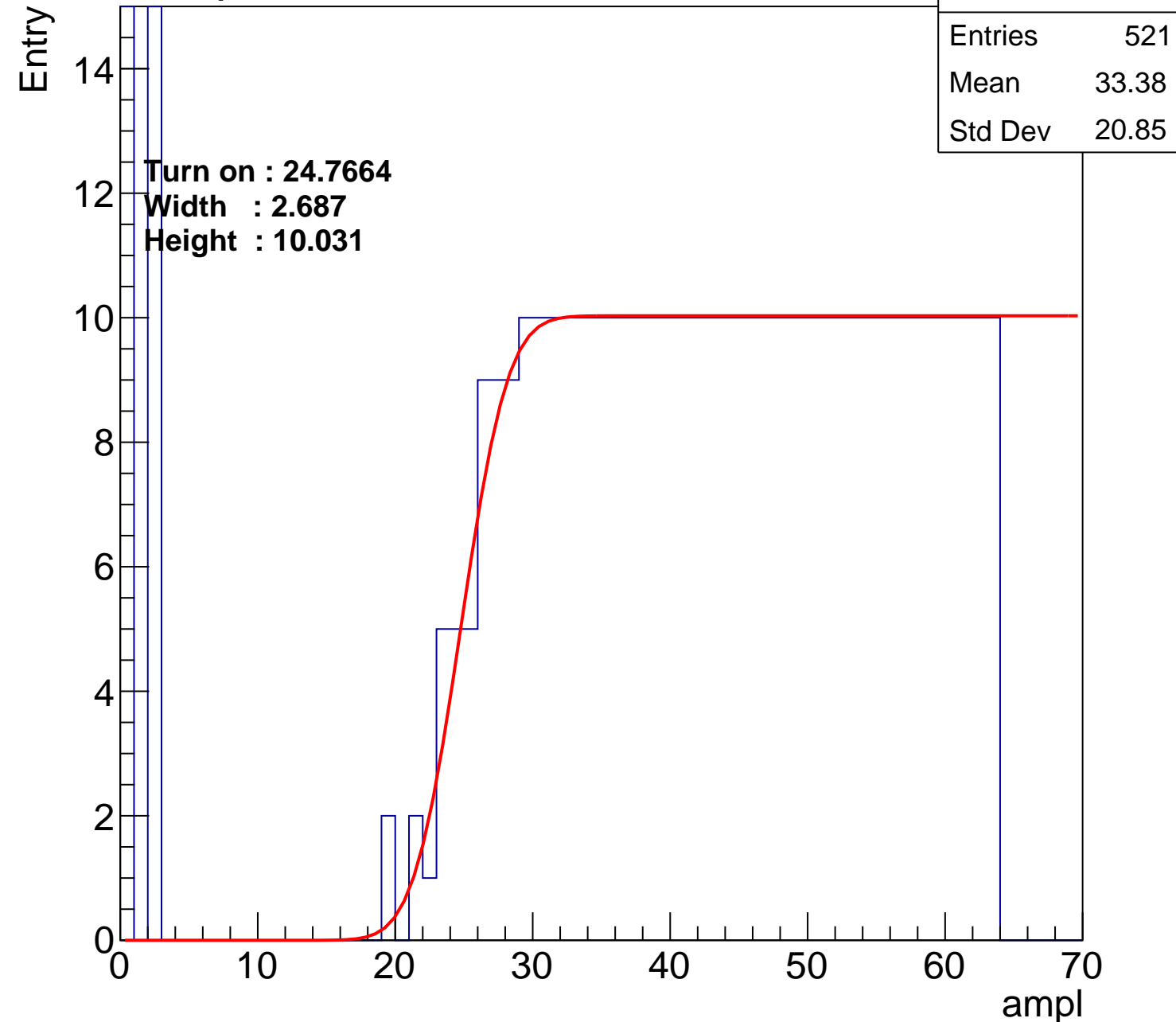
Width : 2.687

Height : 10.031

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U3-ch82

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 577   |
| Mean    | 30.78 |
| Std Dev | 21.5  |

Turn on : 23.3584

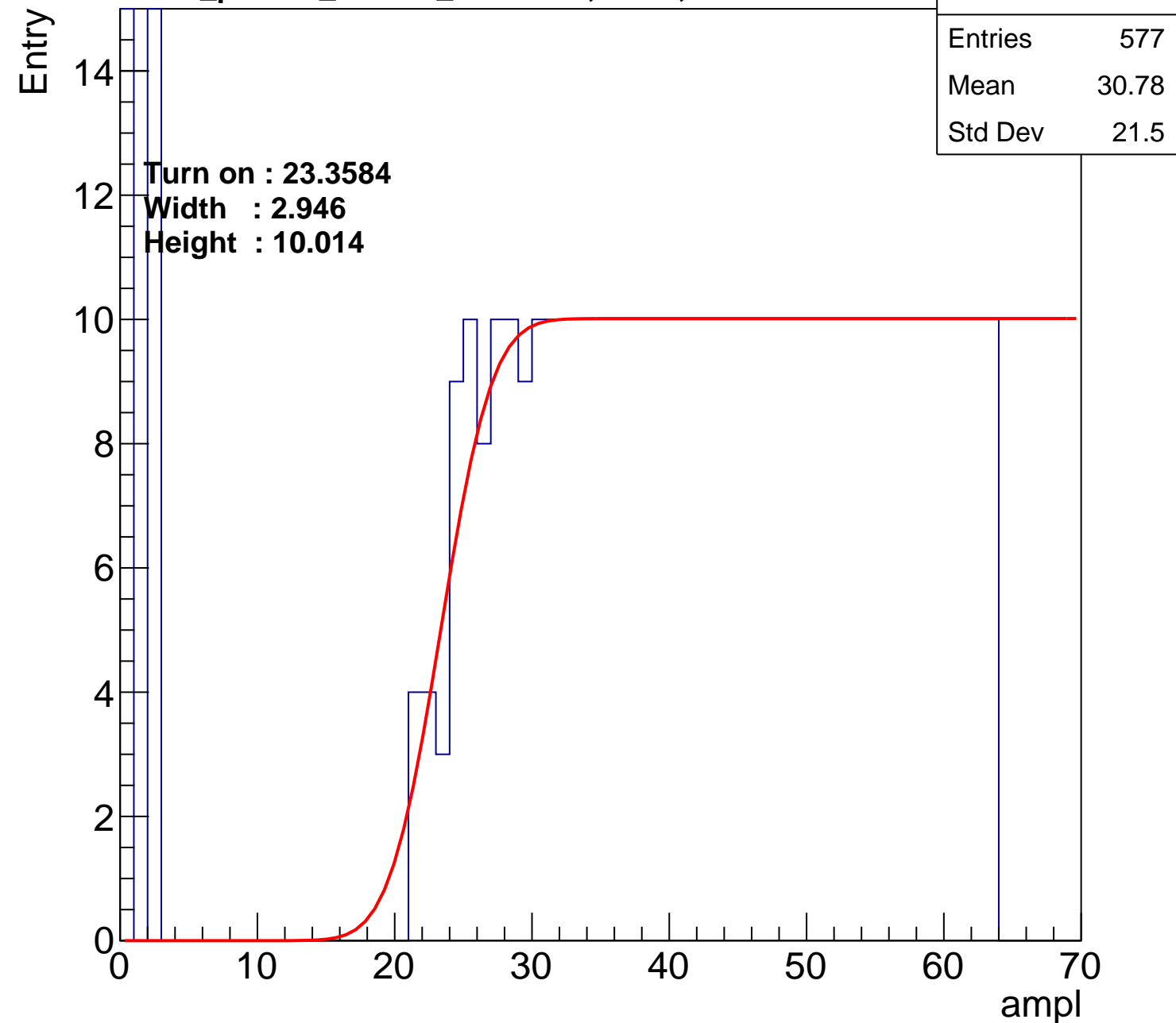
Width : 2.946

Height : 10.014

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U4-ch82

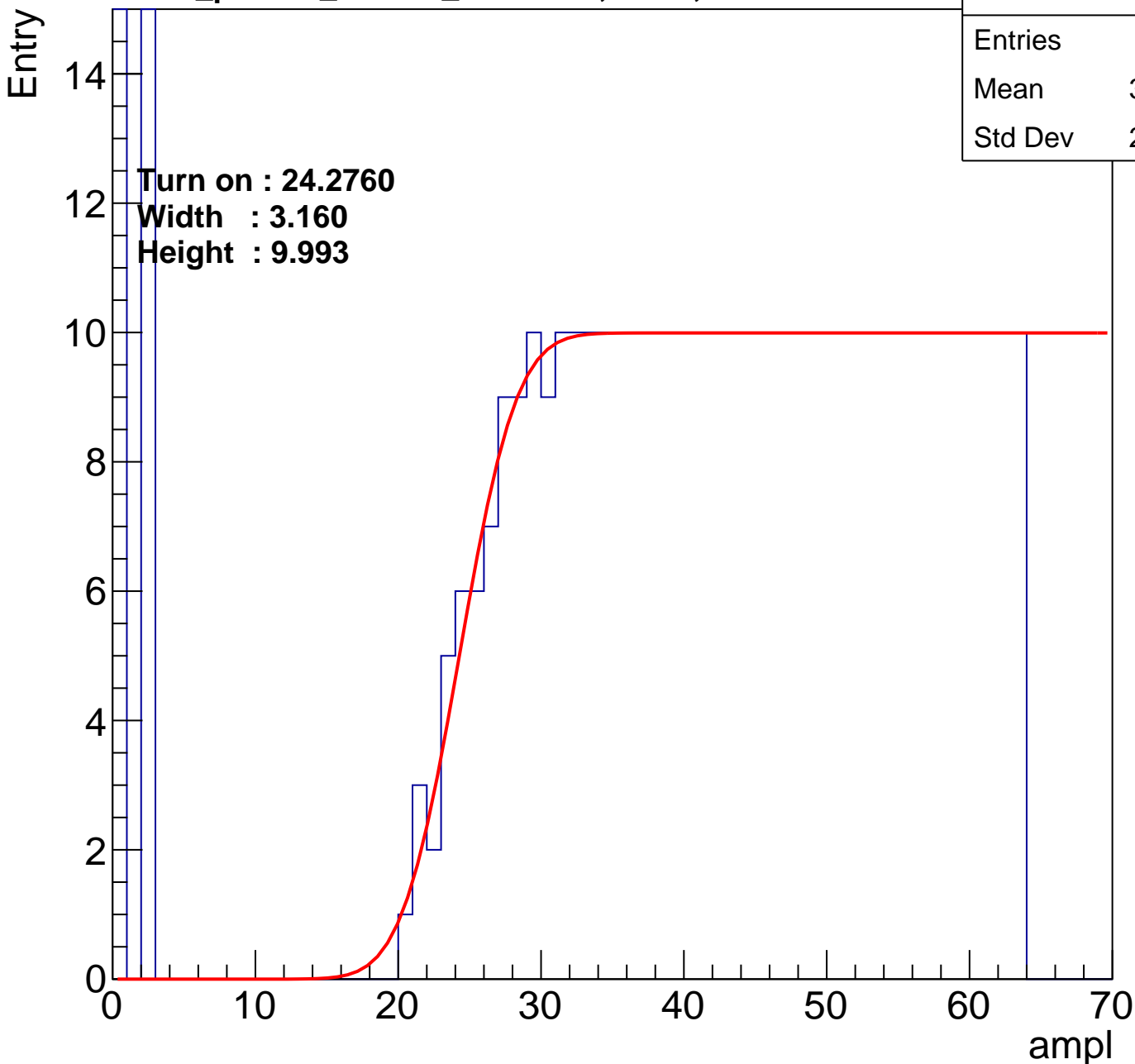
calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 537   |
| Mean    | 32.47 |
| Std Dev | 21.16 |

Turn on : 24.2760

Width : 3.160

Height : 9.993



# B1L103S, U10-ch82

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 525   |
| Mean    | 33.48 |
| Std Dev | 20.55 |

Turn on : 24.4350

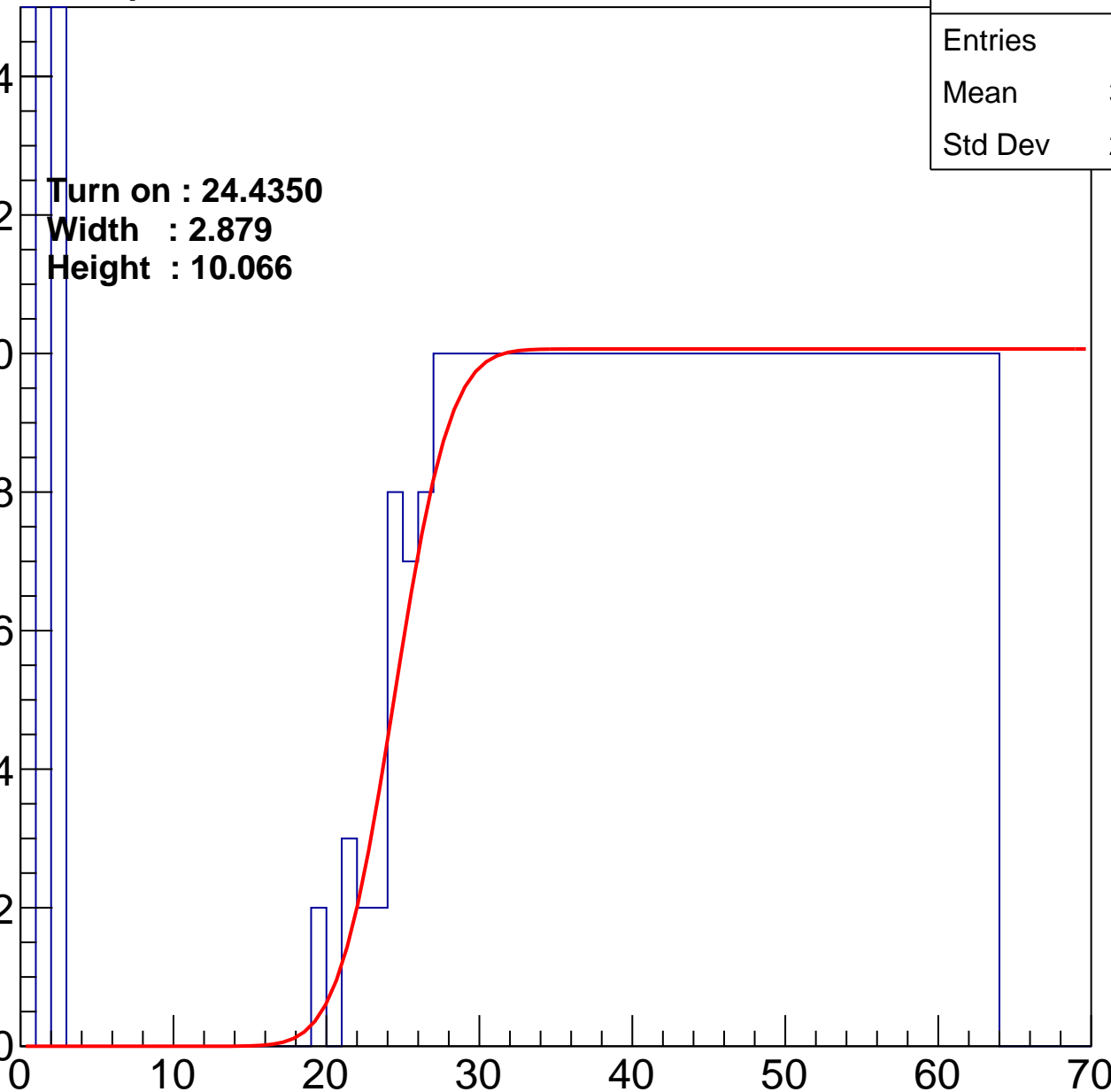
Width : 2.879

Height : 10.066

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U11-ch82

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 535   |
| Mean    | 32.25 |
| Std Dev | 21.43 |

Turn on : 25.4286

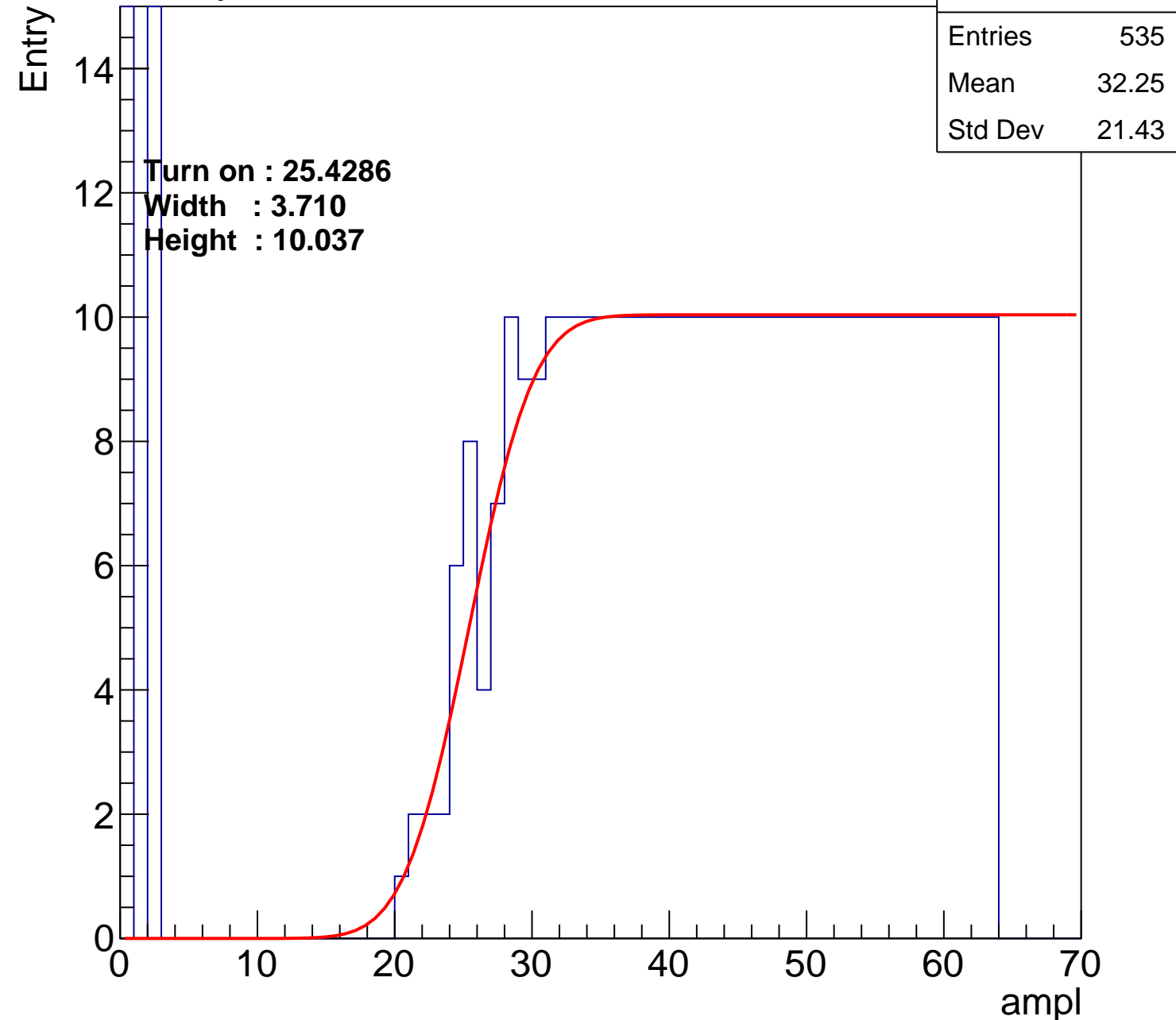
Width : 3.710

Height : 10.037

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U12-ch82

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 532   |
| Mean    | 32.37 |
| Std Dev | 21.4  |

Turn on : 25.4619

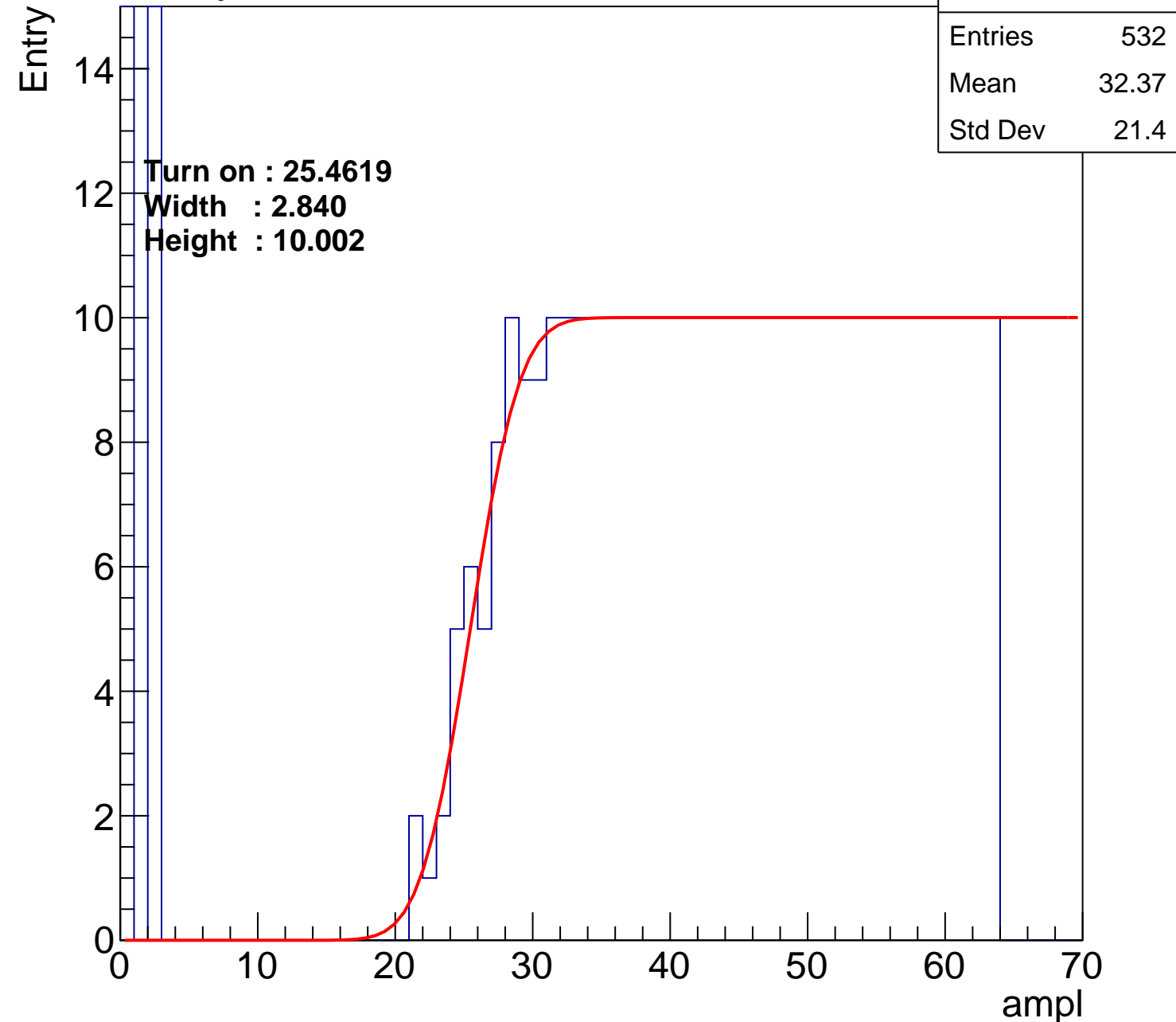
Width : 2.840

Height : 10.002

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L103S, U14-ch0

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 225   |
| Mean    | 38.11 |
| Std Dev | 18.2  |

**Turn on : 24.5503**  
**Width : 4.289**  
**Height : 5.019**

Entry

25

20

15

10

5

0

0

10

20

30

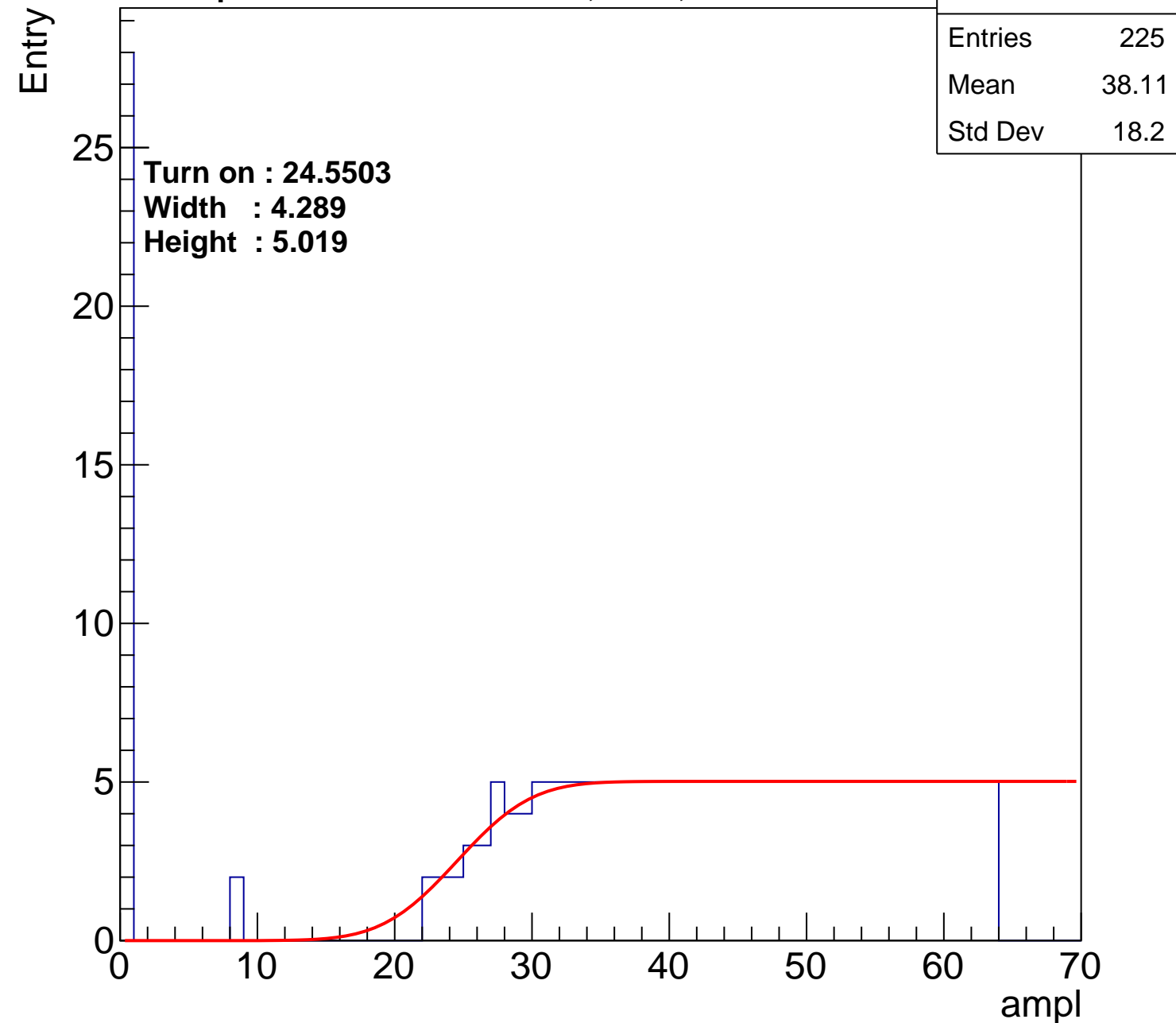
40

50

60

70

ampl



# B1L103S, U14-ch1

calib\_packv5\_041523\_1651.root, FC#0, Port C2

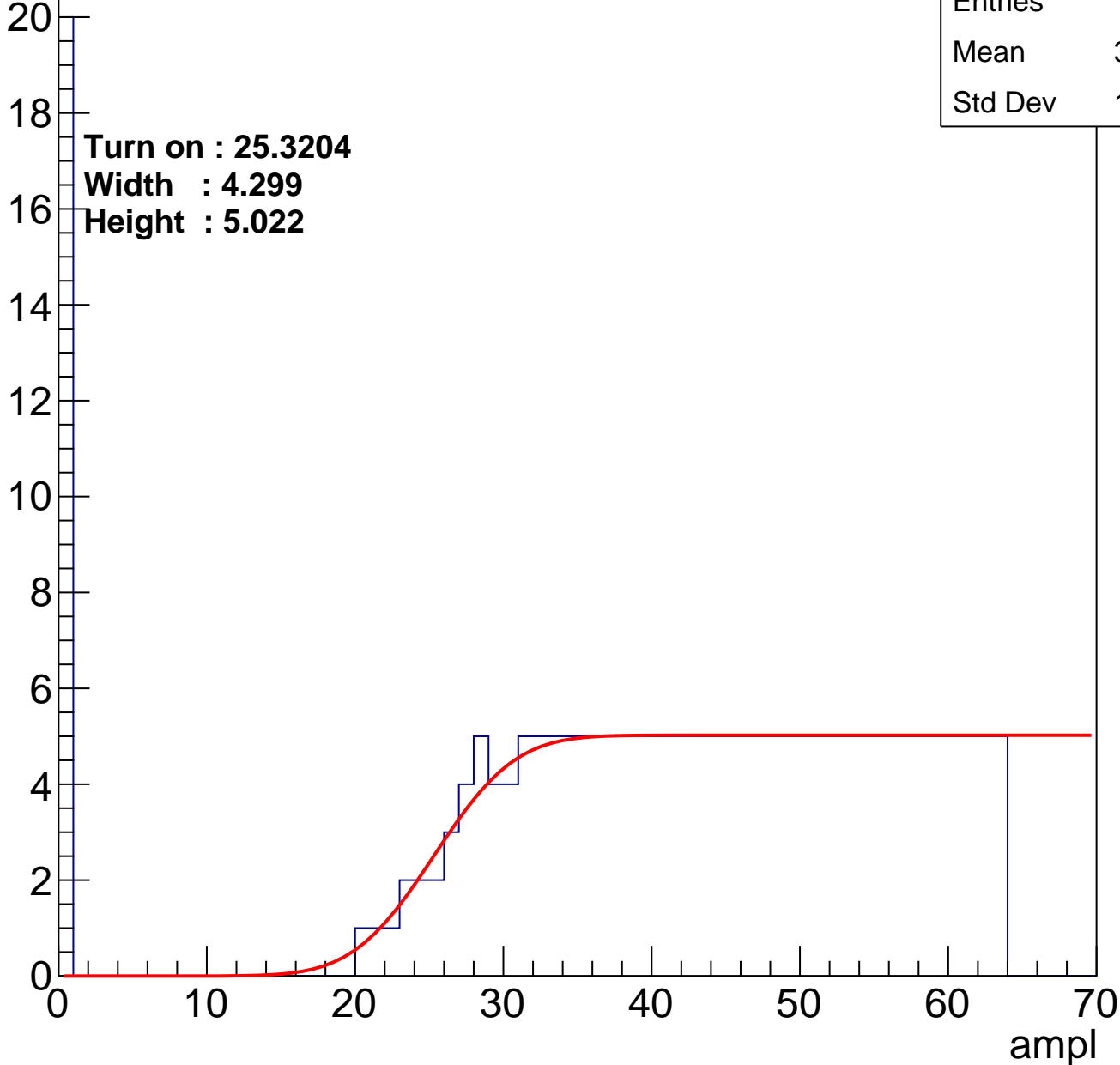
|         |       |
|---------|-------|
| Entries | 214   |
| Mean    | 39.83 |
| Std Dev | 16.82 |

**Turn on : 25.3204**

**Width : 4.299**

**Height : 5.022**

Entry



# B1L103S, U14-ch2

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 220   |
| Mean    | 38.75 |
| Std Dev | 17.81 |

**Turn on : 25.7108**

**Width : 4.097**

**Height : 5.030**

Entry

25

20

15

10

5

0

ampl

0

10

20

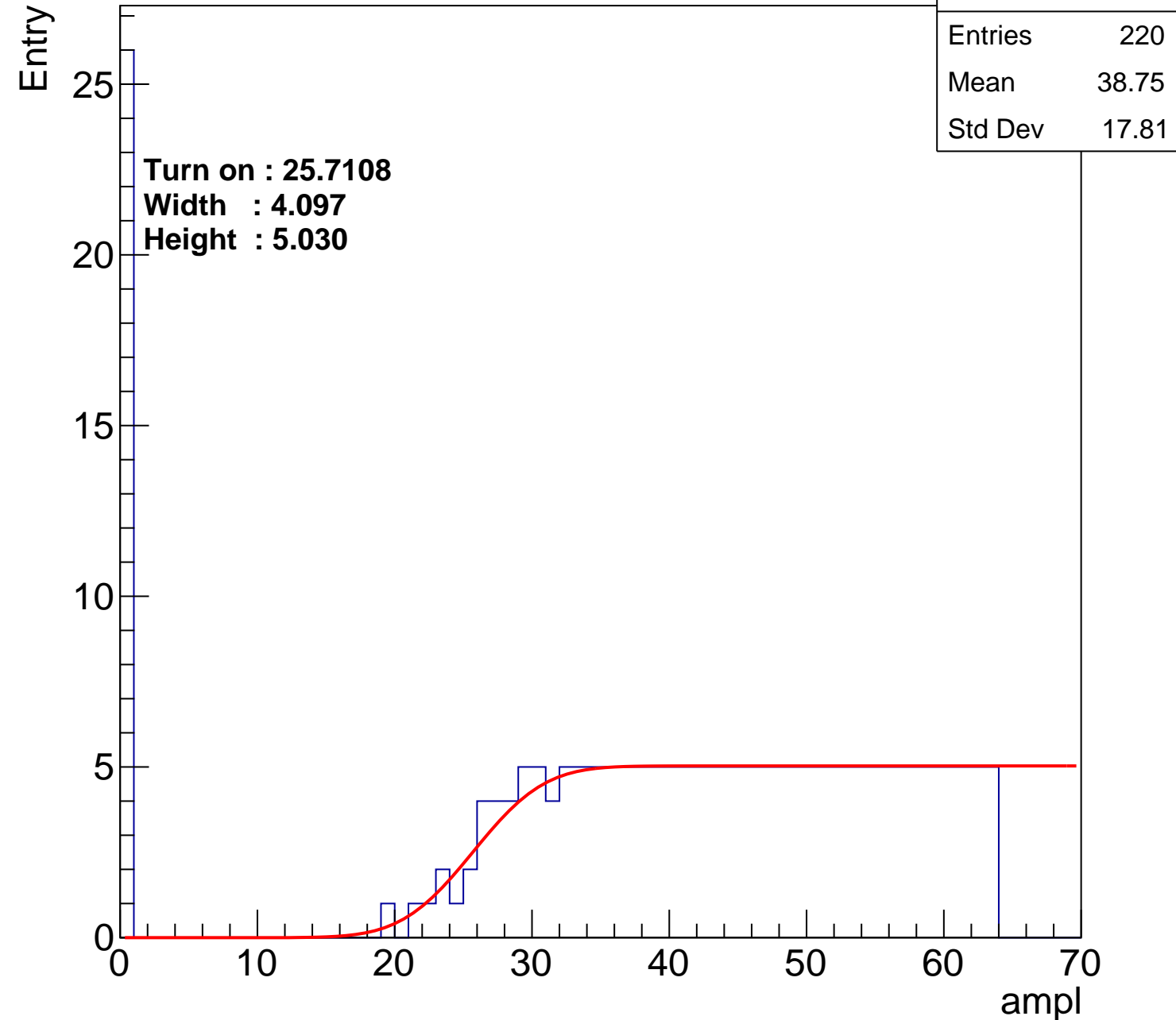
30

40

50

60

70



# B1L103S, U14-ch3

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 223   |
| Mean    | 38.73 |
| Std Dev | 17.55 |

Turn on : 24.9967

Width : 3.366

Height : 5.035

Entry

25

20

15

10

5

0

0

10

20

30

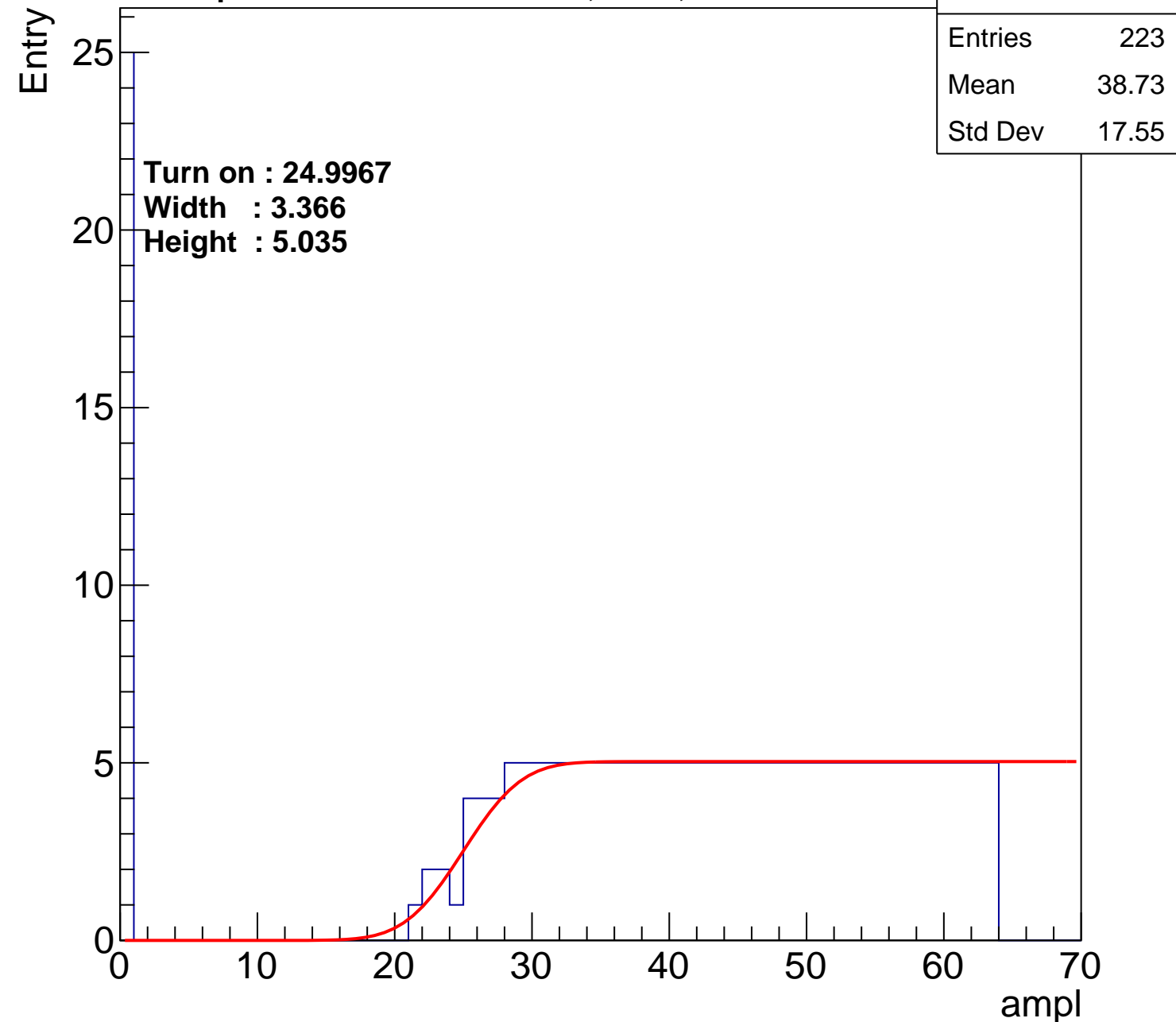
40

50

60

70

ampl



# B1L103S, U14-ch4

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 217   |
| Mean    | 38.99 |
| Std Dev | 17.81 |

**Turn on : 25.9846**

**Width : 3.342**

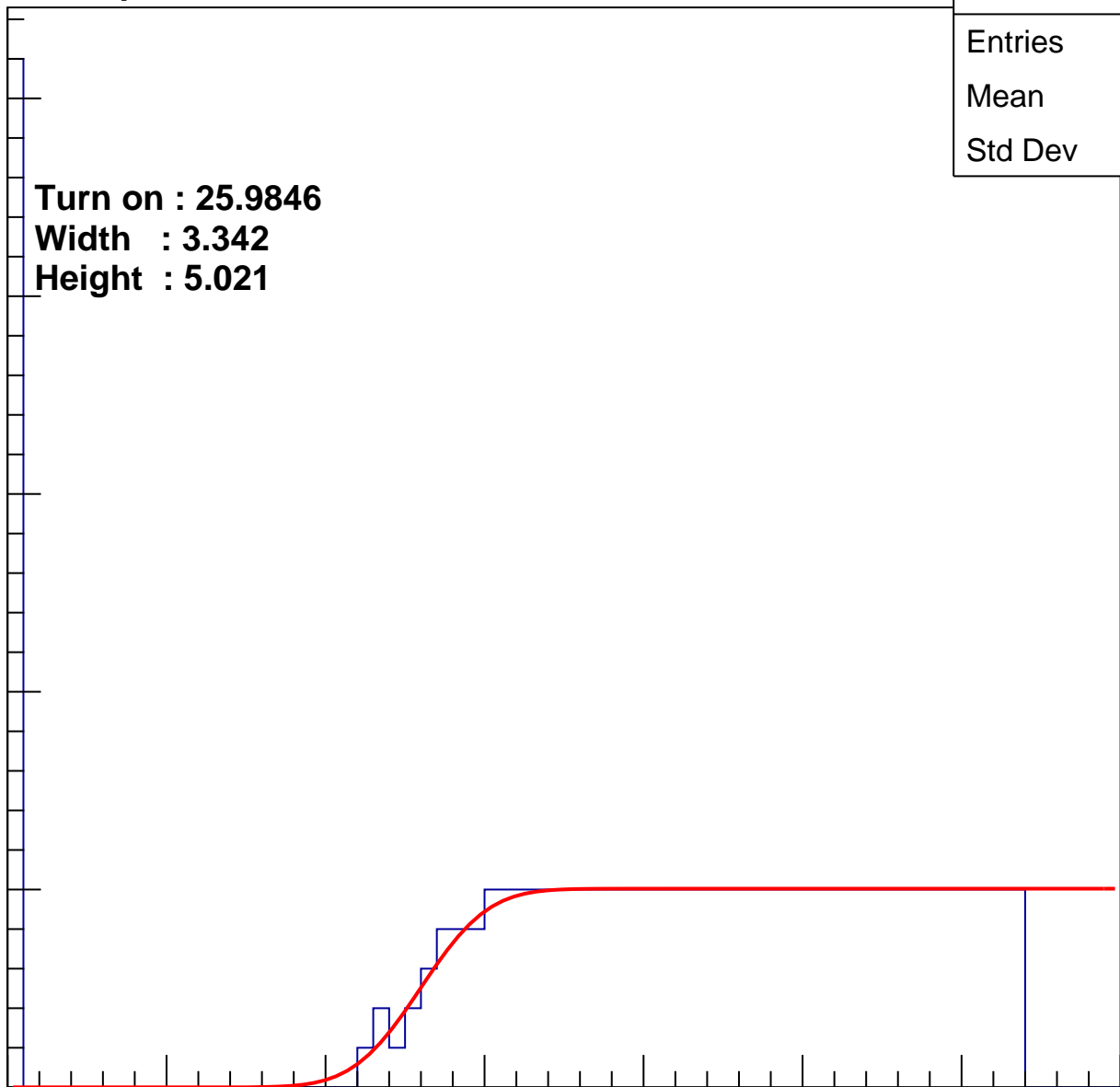
**Height : 5.021**

Entry

25  
20  
15  
10  
5  
0

0 10 20 30 40 50 60 70

ampl



# B1L103S, U14-ch5

calib\_packv5\_041523\_1651.root, FC#0, Port C2

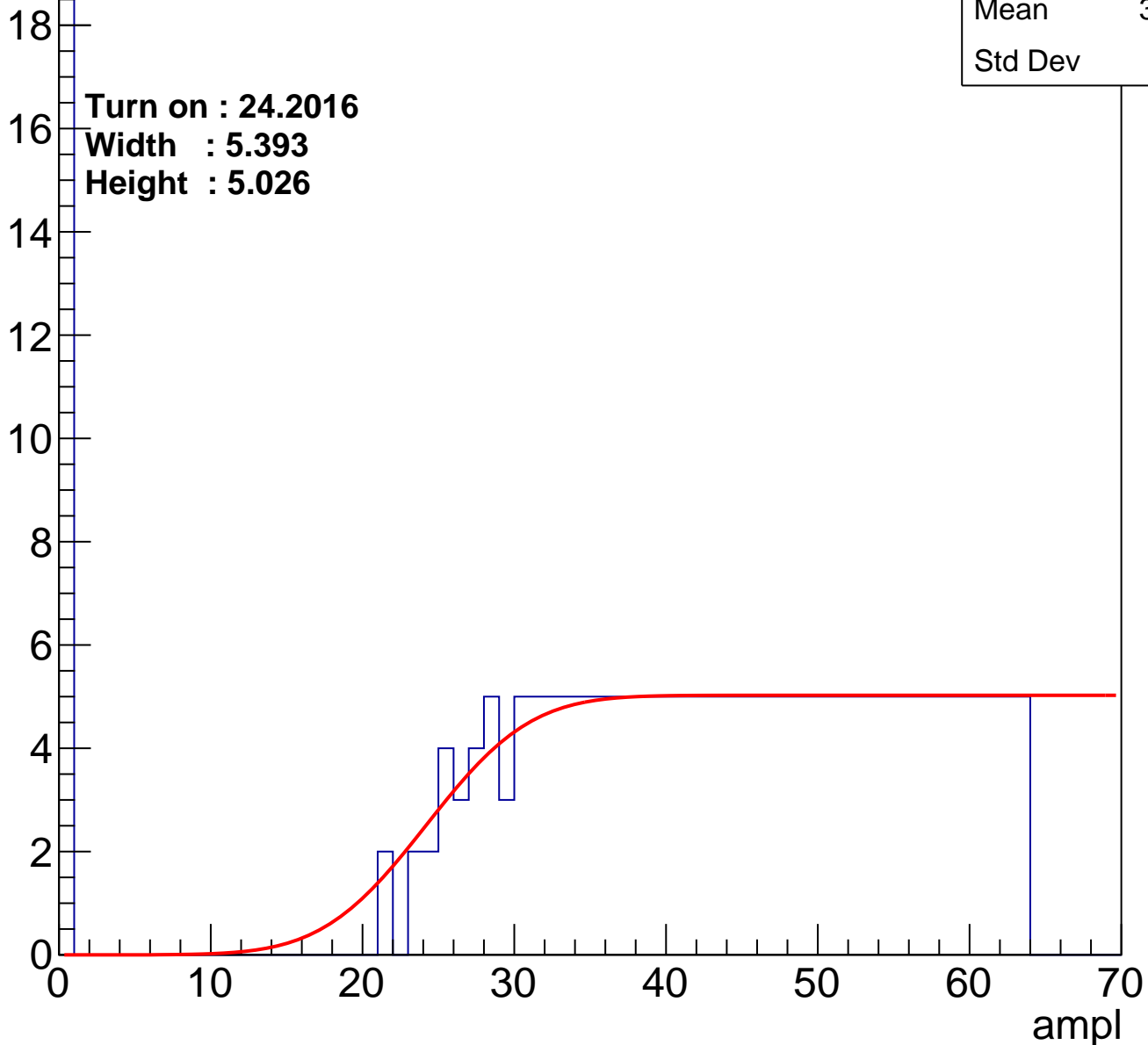
|         |       |
|---------|-------|
| Entries | 214   |
| Mean    | 39.97 |
| Std Dev | 16.6  |

Turn on : 24.2016

Width : 5.393

Height : 5.026

Entry



# B1L103S, U14-ch6

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 217   |
| Mean    | 38.81 |
| Std Dev | 18.11 |

**Turn on : 26.0677**  
**Width : 1.955**  
**Height : 4.999**

Entry

25

20

15

10

5

0

ampl

0

10

20

30

40

50

60

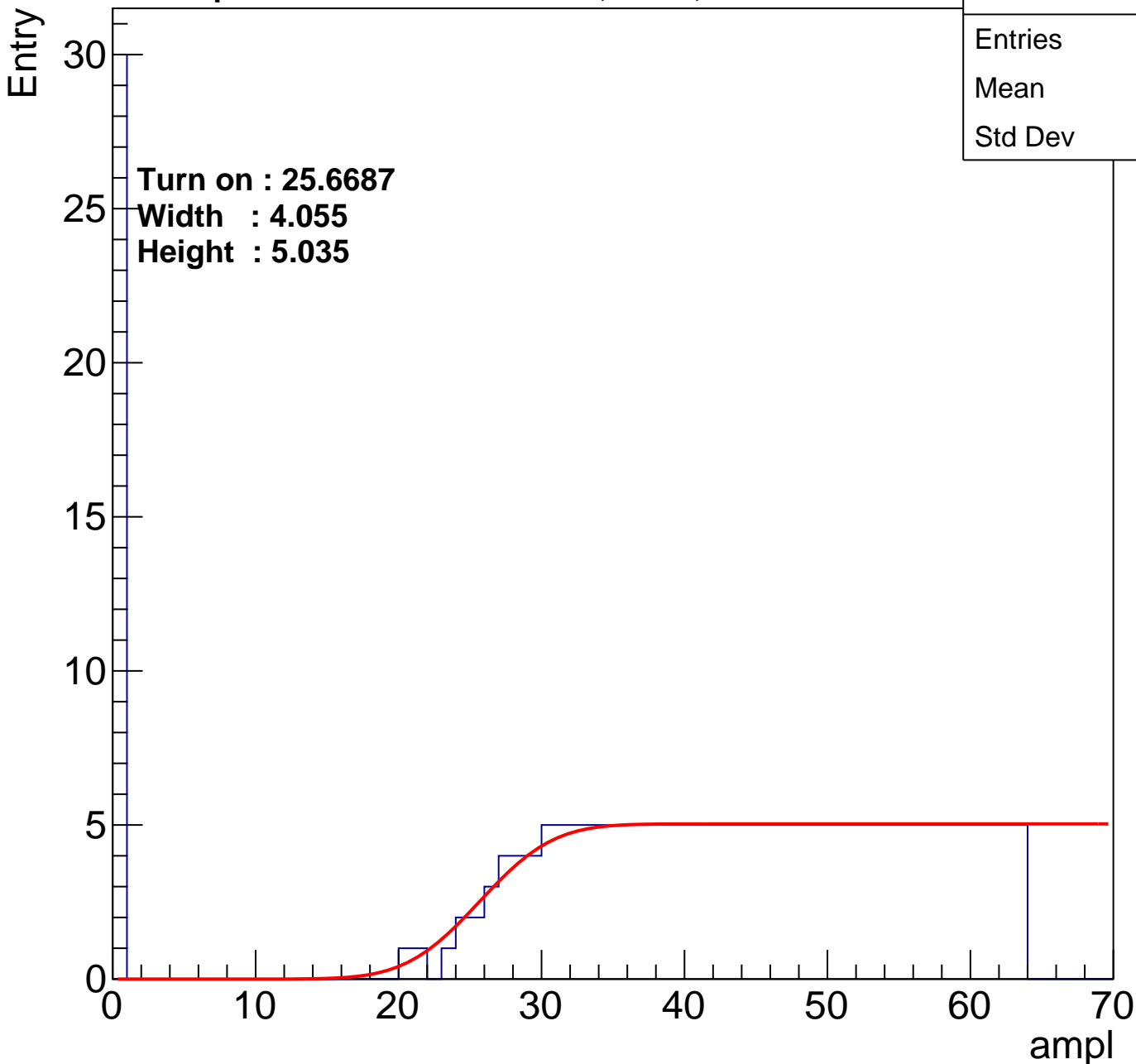
70

# B1L103S, U14-ch7

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |      |
|---------|------|
| Entries | 222  |
| Mean    | 38.2 |
| Std Dev | 18.4 |

**Turn on : 25.6687**  
**Width : 4.055**  
**Height : 5.035**





# B1L103S, U14-ch8

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 220   |
| Mean    | 38.79 |
| Std Dev | 17.78 |

**Turn on : 25.3442**

**Width : 3.393**

**Height : 5.016**

Entry

25

20

15

10

5

0

0

10

20

30

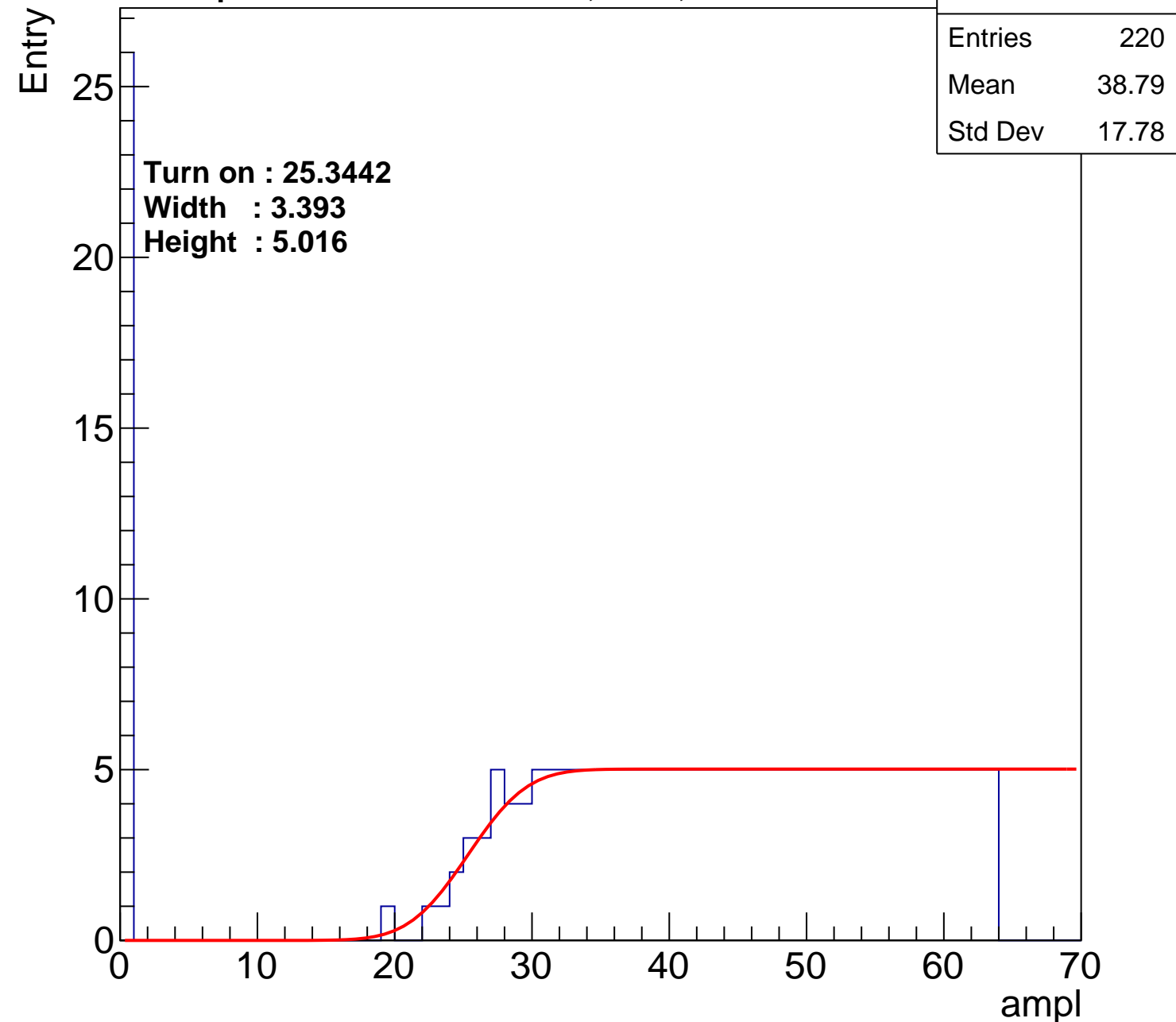
40

50

60

70

ampl



# B1L103S, U14-ch9

calib\_packv5\_041523\_1651.root, FC#0, Port C2

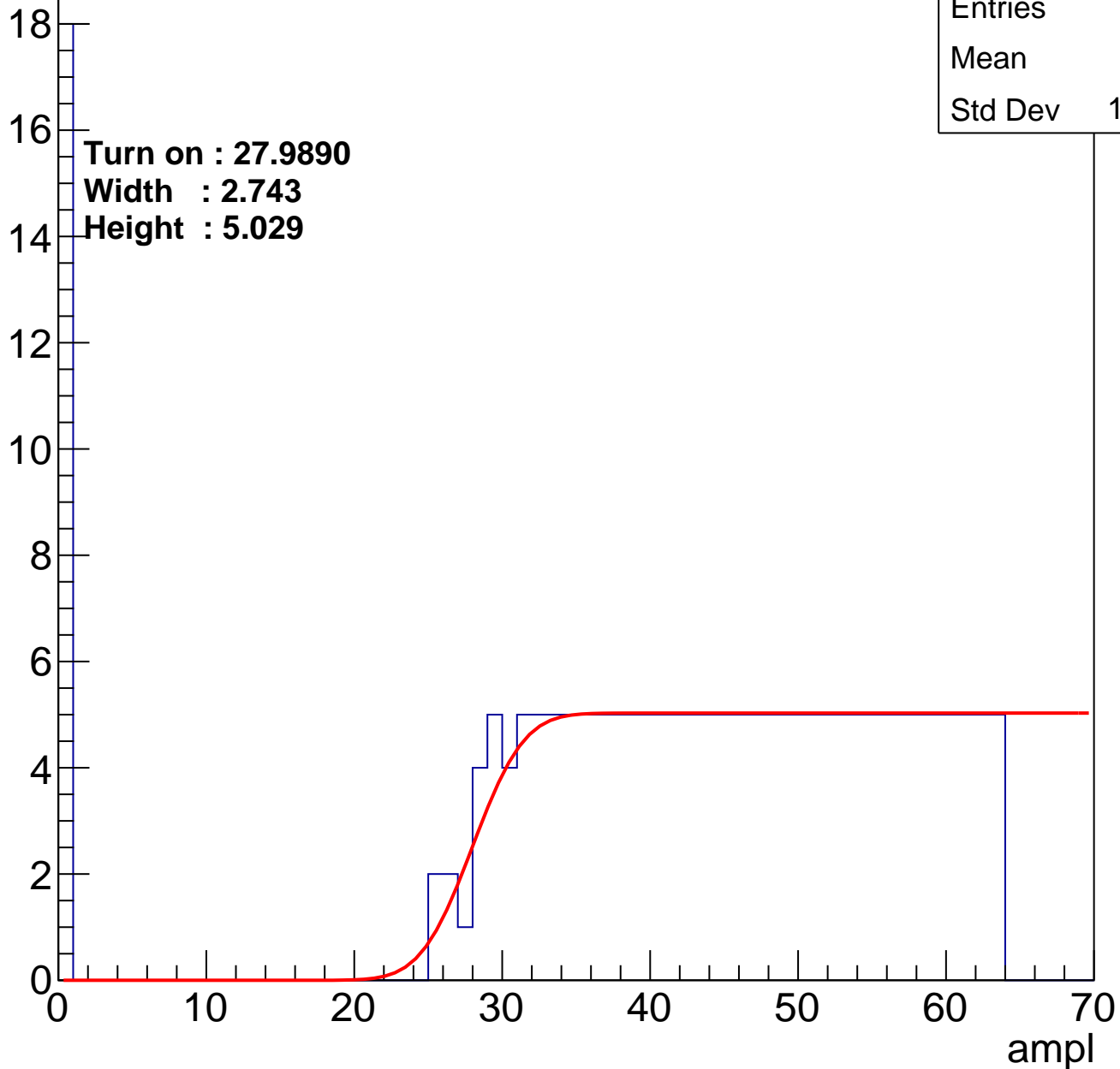
|         |       |
|---------|-------|
| Entries | 201   |
| Mean    | 41.1  |
| Std Dev | 16.42 |

Turn on : 27.9890

Width : 2.743

Height : 5.029

Entry



# B1L103S, U14-ch10

calib\_packv5\_041523\_1651.root, FC#0, Port C2

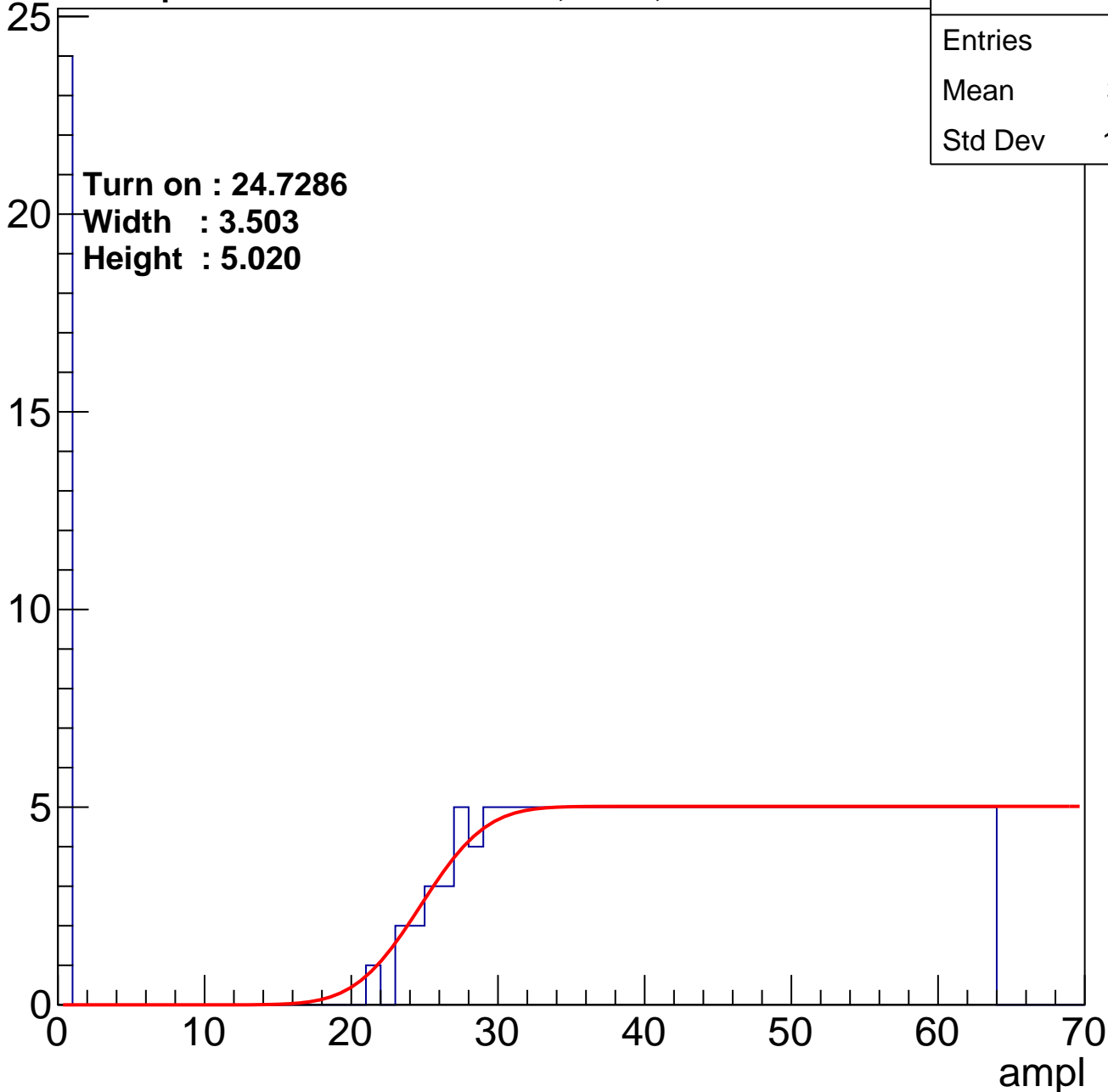
|         |       |
|---------|-------|
| Entries | 219   |
| Mean    | 39.11 |
| Std Dev | 17.43 |

Turn on : 24.7286

Width : 3.503

Height : 5.020

Entry

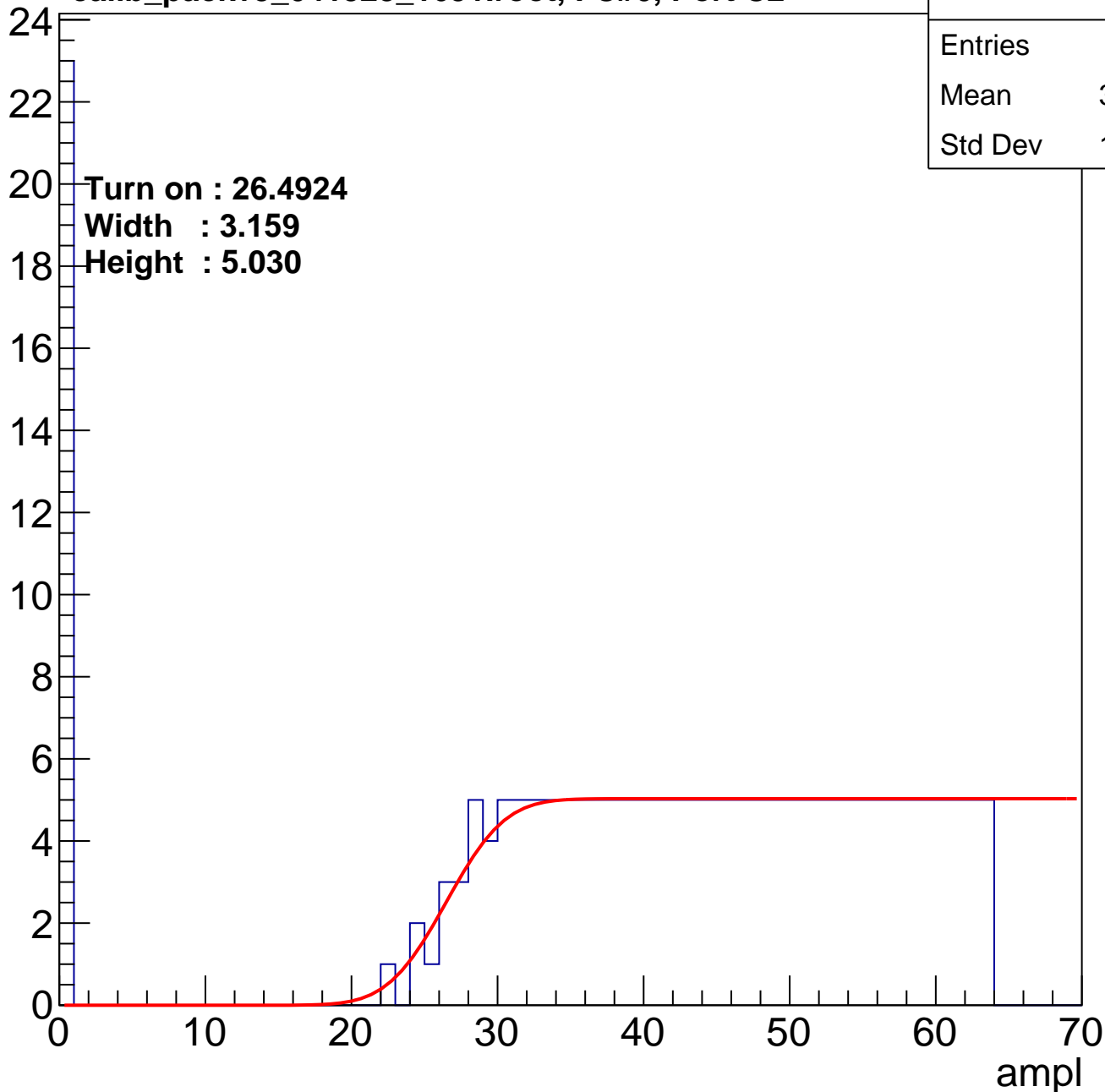


# B1L103S, U14-ch11

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 212   |
| Mean    | 39.69 |
| Std Dev | 17.33 |

Entry



# B1L103S, U14-ch12

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 218   |
| Mean    | 38.44 |
| Std Dev | 18.47 |

**Turn on : 27.4825**

**Width : 4.196**

**Height : 5.046**

Entry

30

25

20

15

10

5

0

0

10

20

30

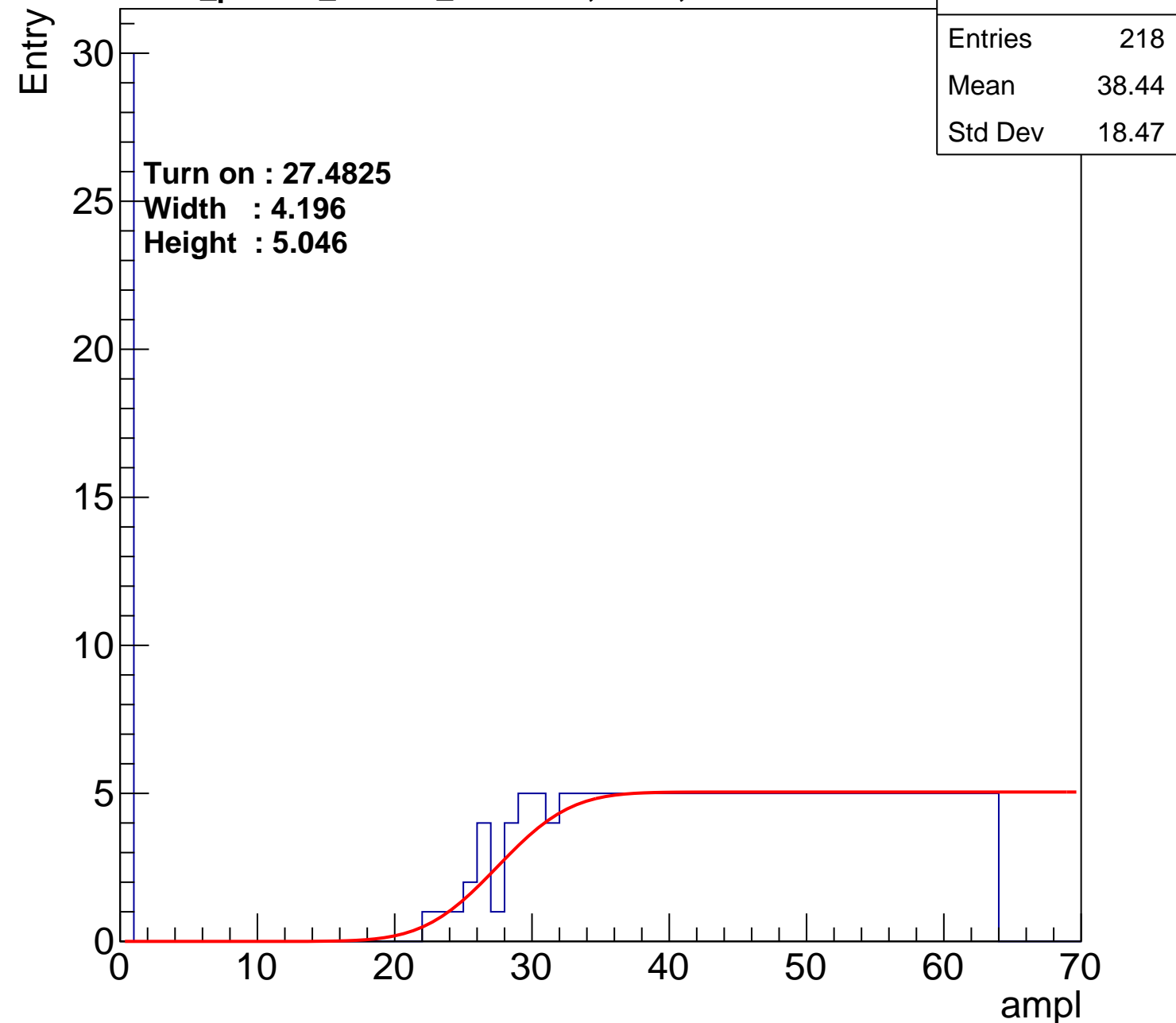
40

50

60

70

ampl



# B1L103S, U14-ch13

calib\_packv5\_041523\_1651.root, FC#0, Port C2

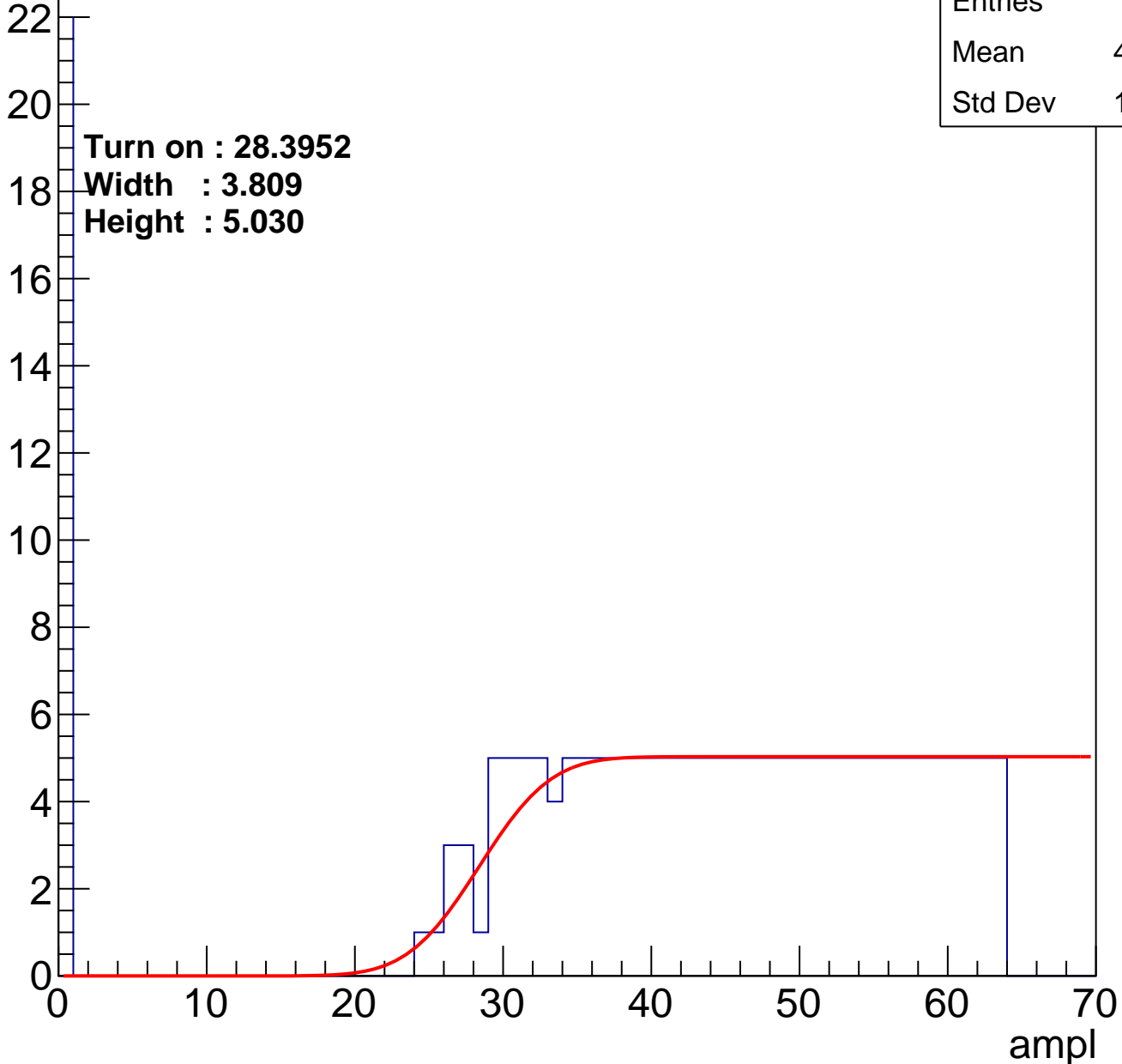
|         |       |
|---------|-------|
| Entries | 205   |
| Mean    | 40.26 |
| Std Dev | 17.25 |

**Turn on : 28.3952**

**Width : 3.809**

**Height : 5.030**

Entry



# B1L103S, U14-ch14

calib\_packv5\_041523\_1651.root, FC#0, Port C2

Entry

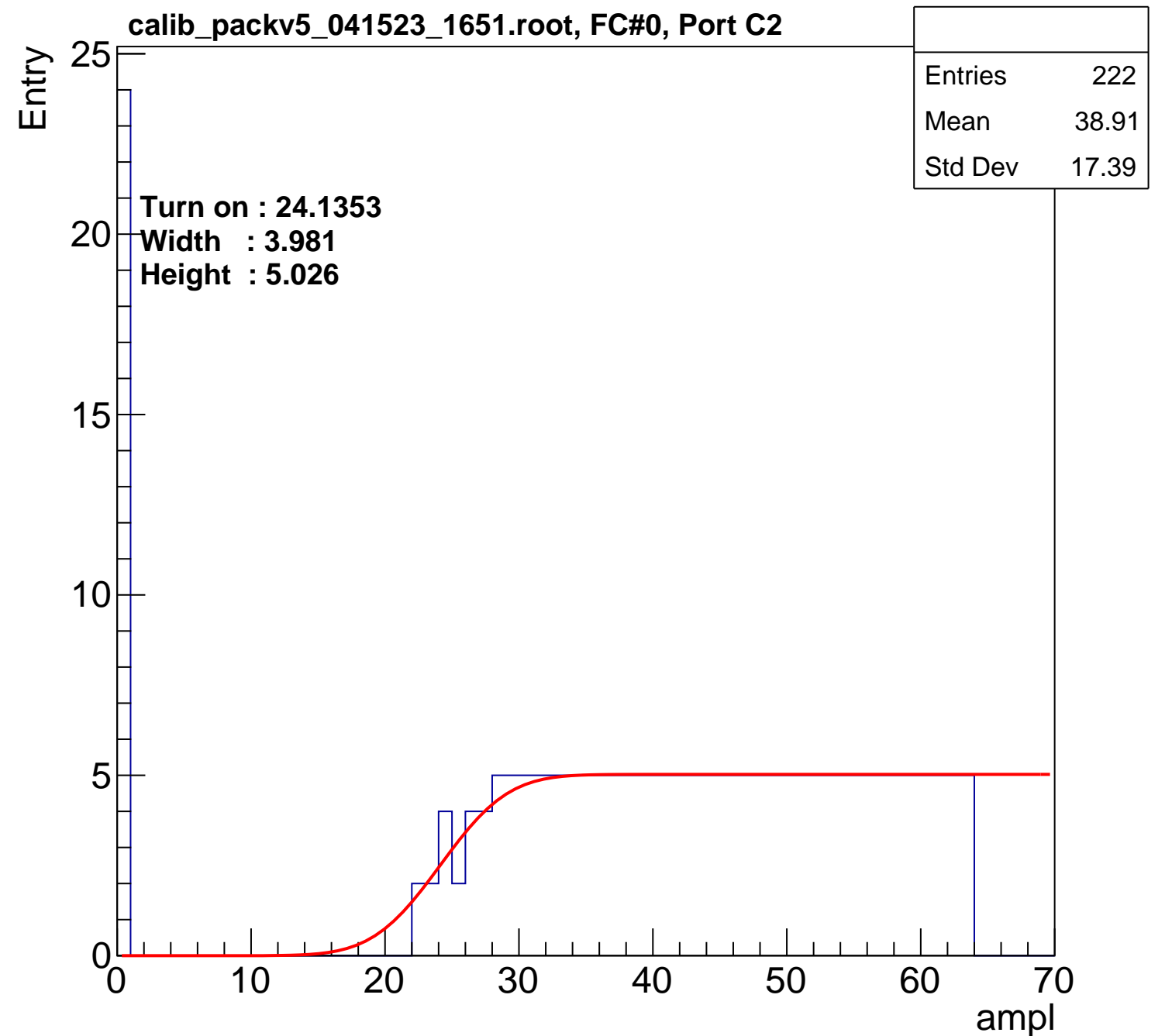
25  
20  
15  
10  
5  
0

**Turn on : 24.1353**  
**Width : 3.981**  
**Height : 5.026**

|         |       |
|---------|-------|
| Entries | 222   |
| Mean    | 38.91 |
| Std Dev | 17.39 |

ampl

0 10 20 30 40 50 60 70



# B1L103S, U14-ch15

calib\_packv5\_041523\_1651.root, FC#0, Port C2

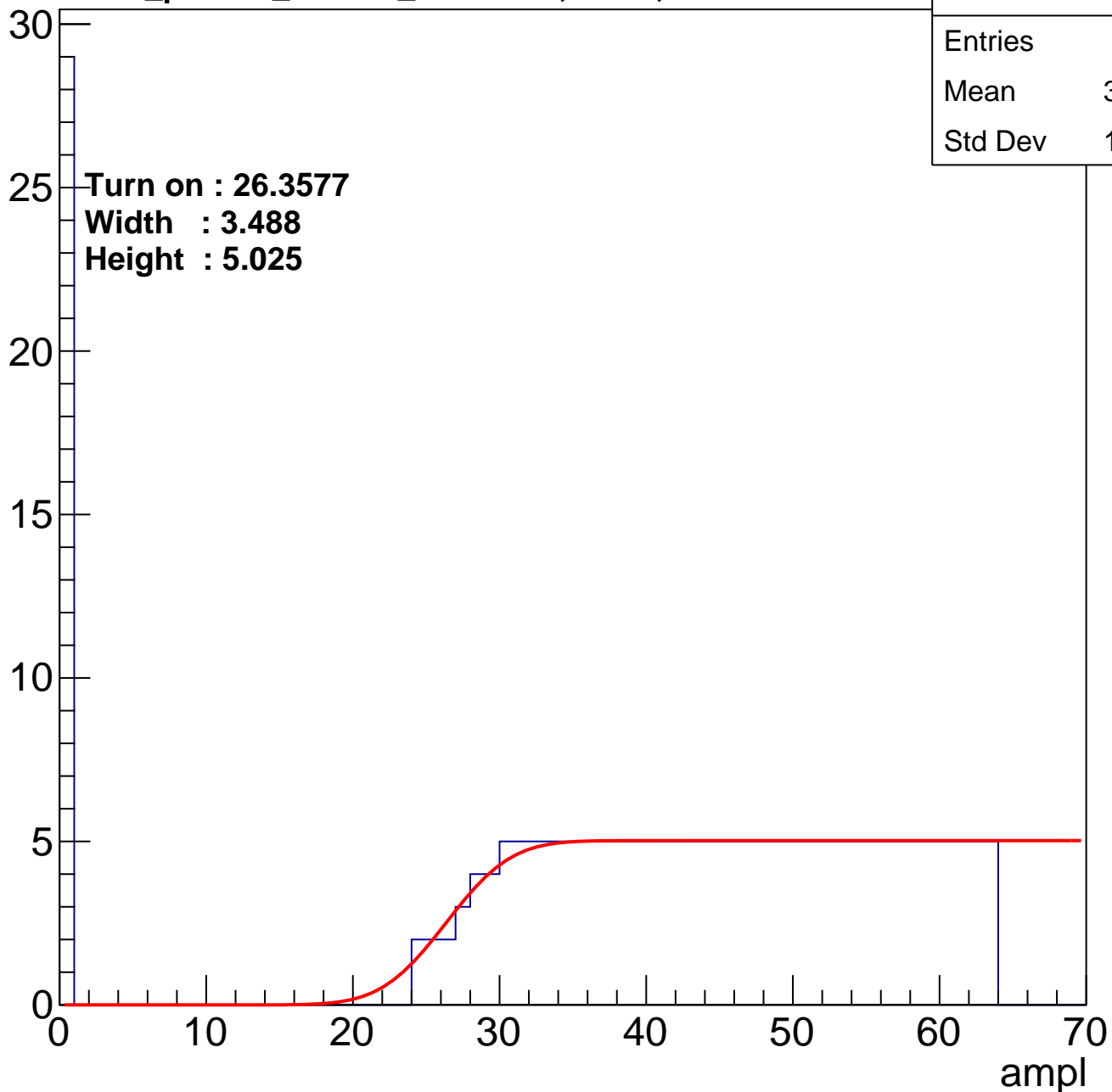
|         |       |
|---------|-------|
| Entries | 216   |
| Mean    | 38.72 |
| Std Dev | 18.32 |

Turn on : 26.3577

Width : 3.488

Height : 5.025

Entry





# B1L103S, U14-ch16

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 224   |
| Mean    | 38.61 |
| Std Dev | 17.69 |

**Turn on : 25.3404**

**Width : 3.962**

**Height : 5.079**

Entry

25

20

15

10

5

0

0

10

20

30

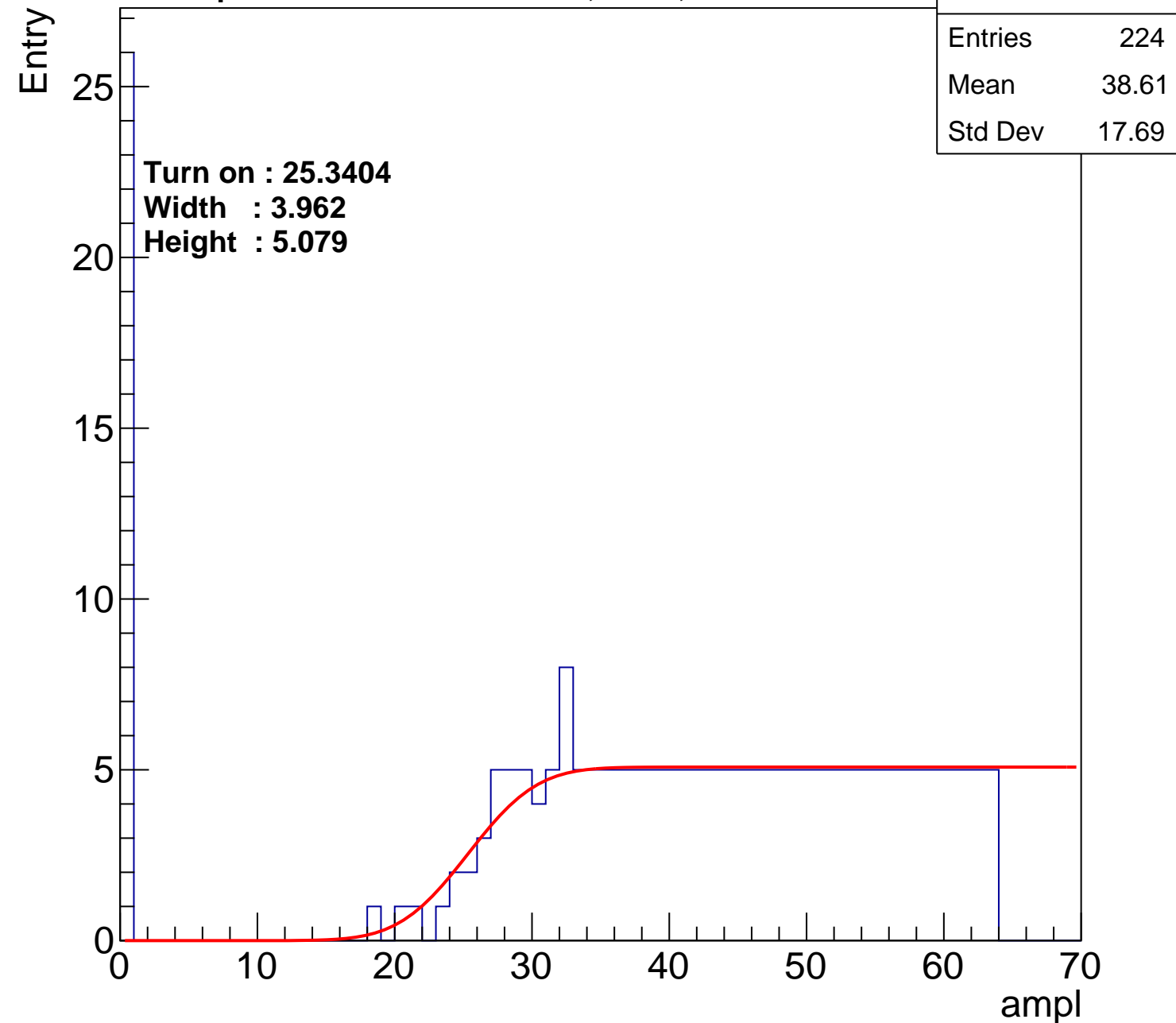
40

50

60

70

ampl



# B1L103S, U14-ch17

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 200   |
| Mean    | 41.57 |
| Std Dev | 15.73 |

**Turn on : 27.0793**

**Width : 2.482**

**Height : 5.010**

Entry

14

12

10

8

6

4

2

0

0

10

20

30

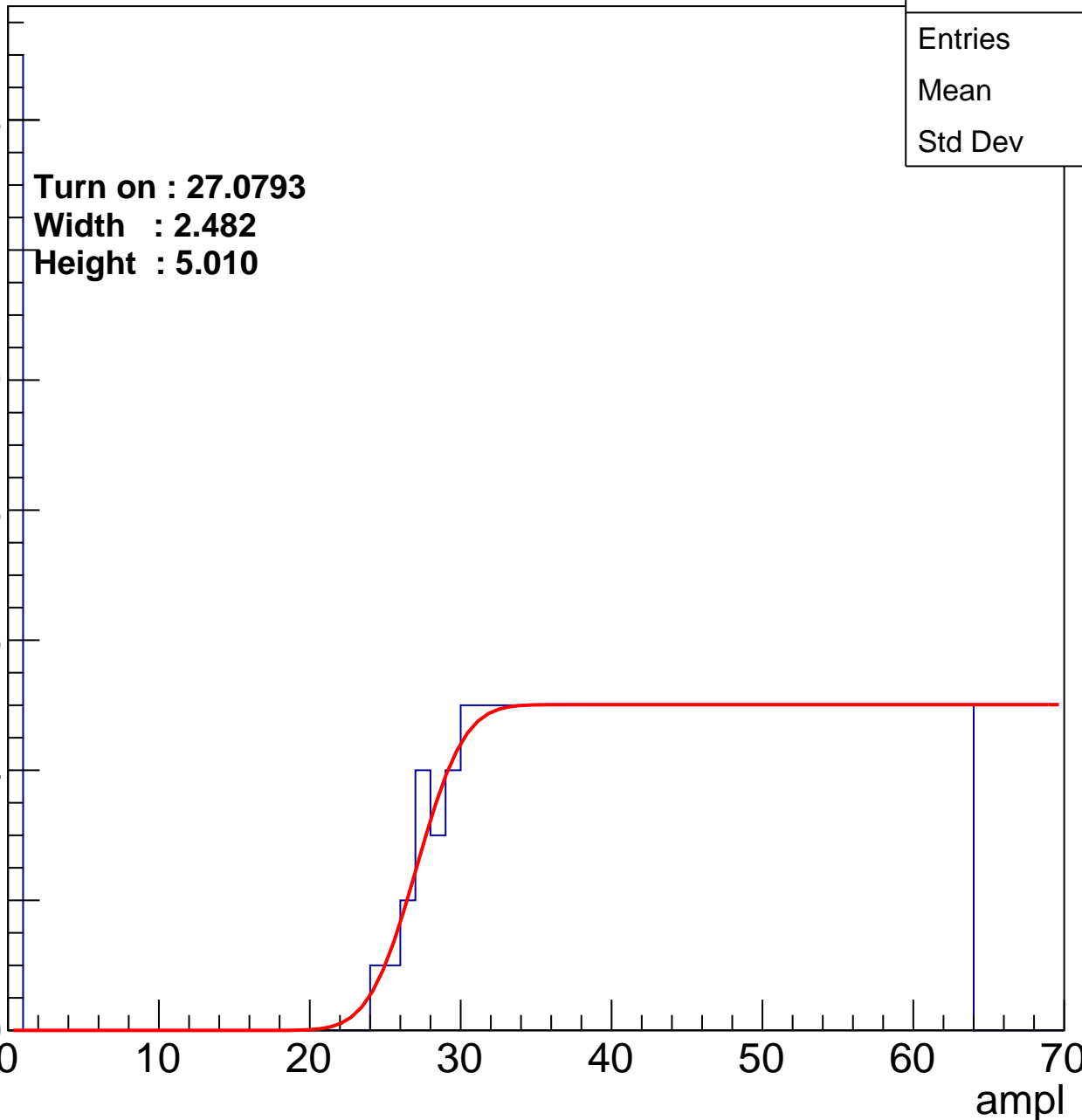
40

50

60

70

ampl



# B1L103S, U14-ch18

calib\_packv5\_041523\_1651.root, FC#0, Port C2

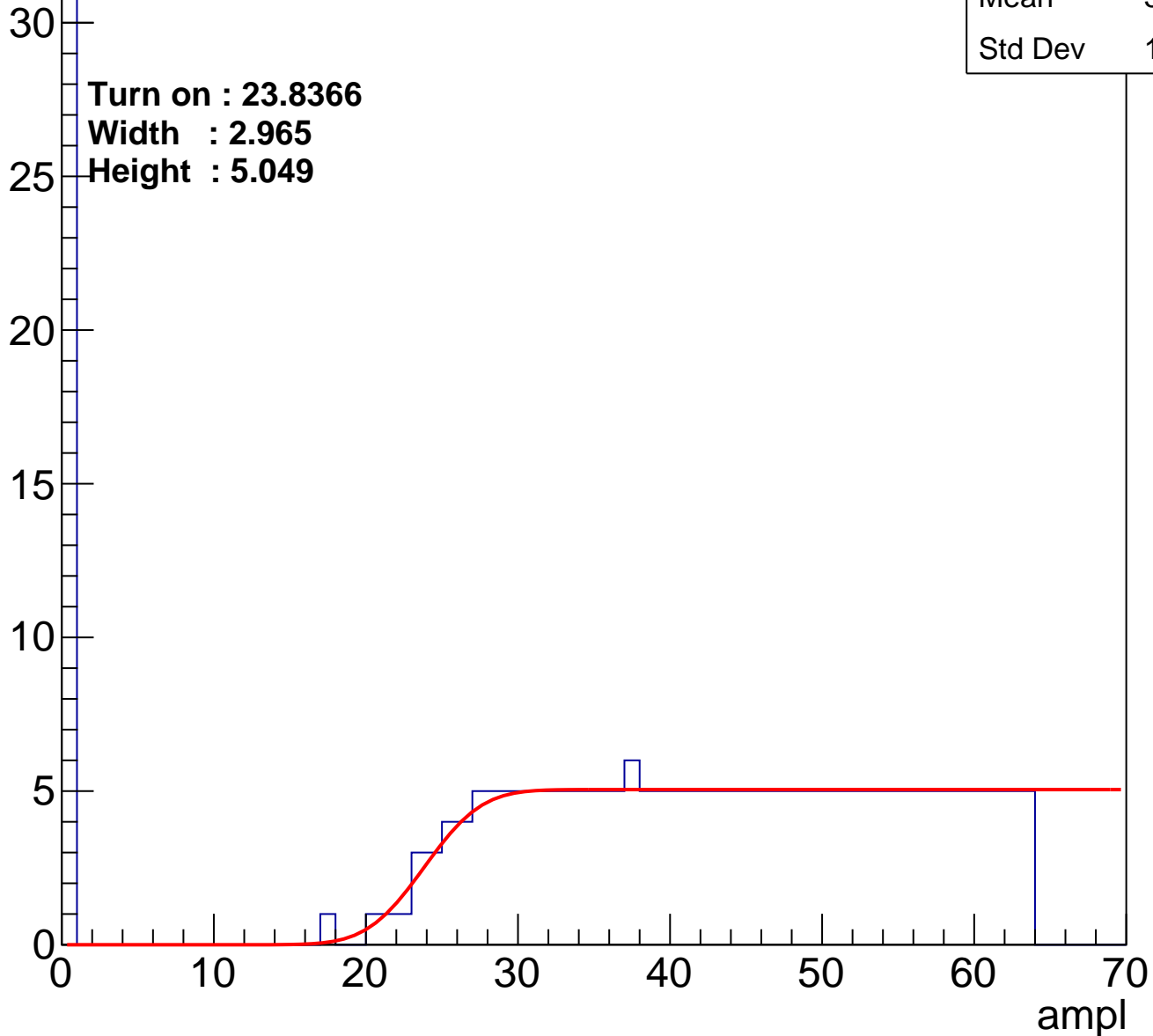
|         |       |
|---------|-------|
| Entries | 236   |
| Mean    | 37.23 |
| Std Dev | 18.42 |

**Turn on : 23.8366**

**Width : 2.965**

**Height : 5.049**

Entry



# B1L103S, U14-ch19

calib\_packv5\_041523\_1651.root, FC#0, Port C2

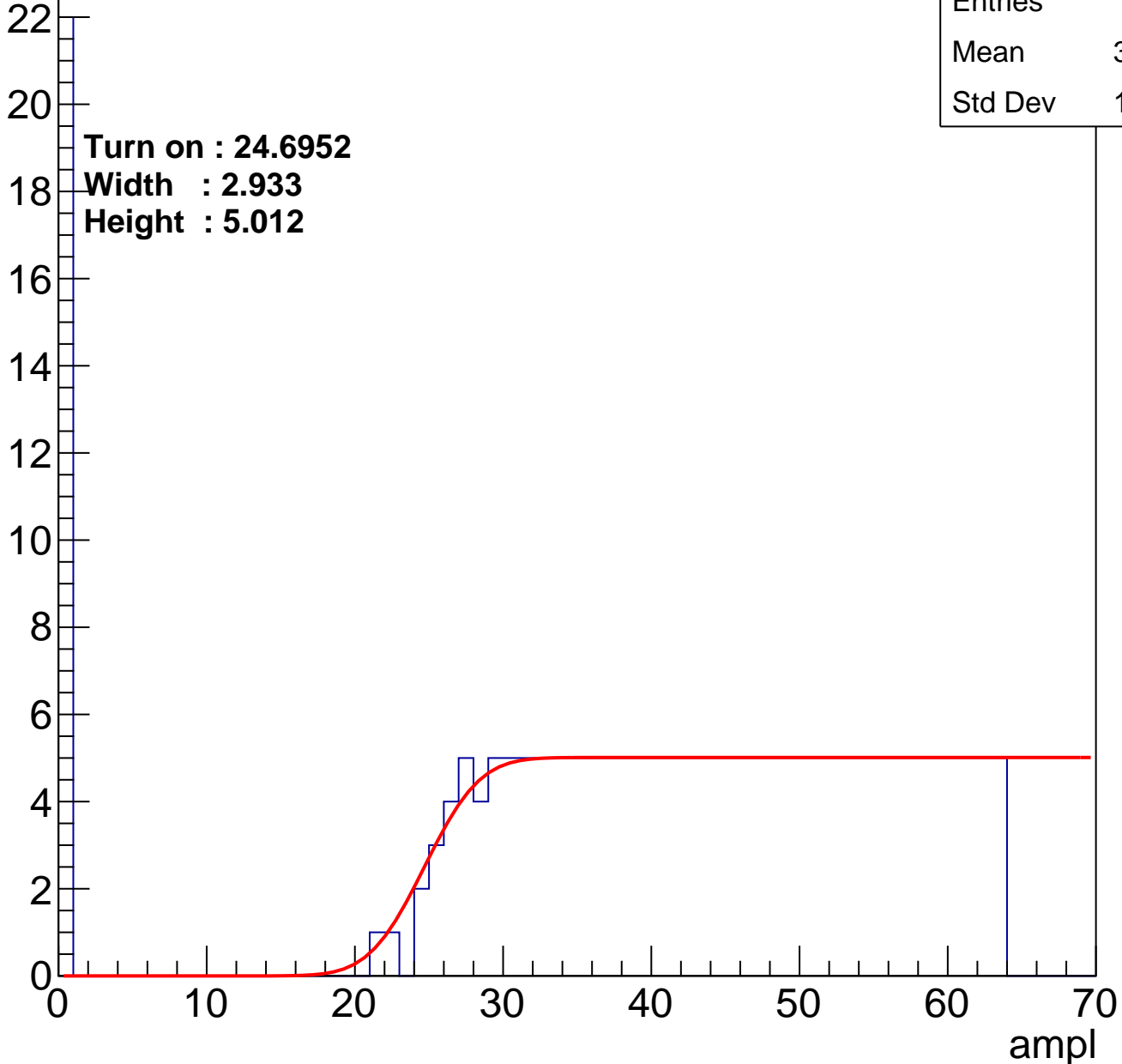
|         |       |
|---------|-------|
| Entries | 217   |
| Mean    | 39.48 |
| Std Dev | 17.09 |

**Turn on : 24.6952**

**Width : 2.933**

**Height : 5.012**

Entry



# B1L103S, U14-ch20

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 215   |
| Mean    | 38.94 |
| Std Dev | 18.06 |

**Turn on : 26.9306**

**Width : 4.528**

**Height : 5.039**

Entry

25

20

15

10

5

0

0

10

20

30

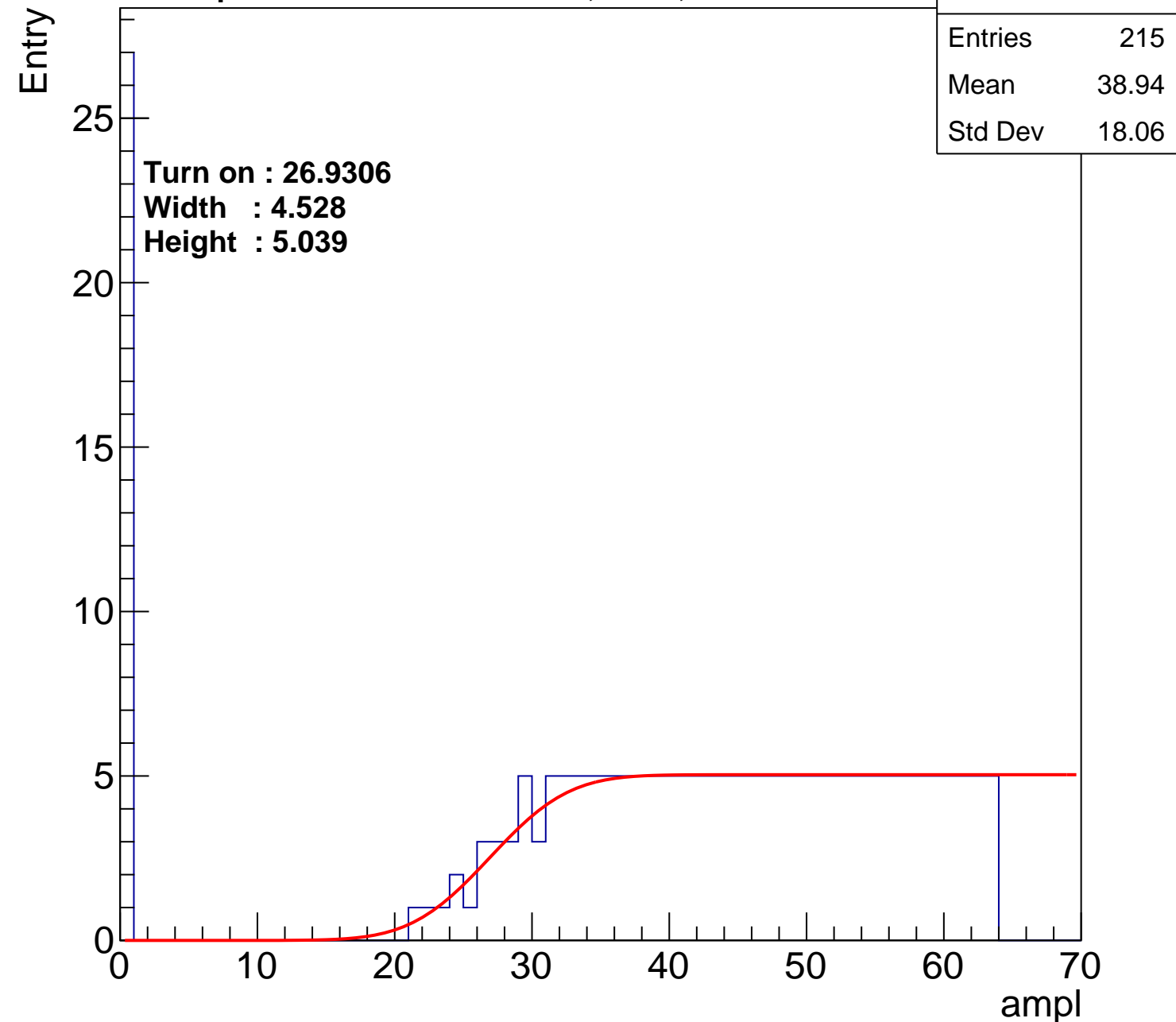
40

50

60

70

ampl



# B1L103S, U14-ch21

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 221   |
| Mean    | 37.95 |
| Std Dev | 18.87 |

**Turn on : 26.9364**

**Width : 3.741**

**Height : 5.039**

Entry

30

25

20

15

10

5

0

0

10

20

30

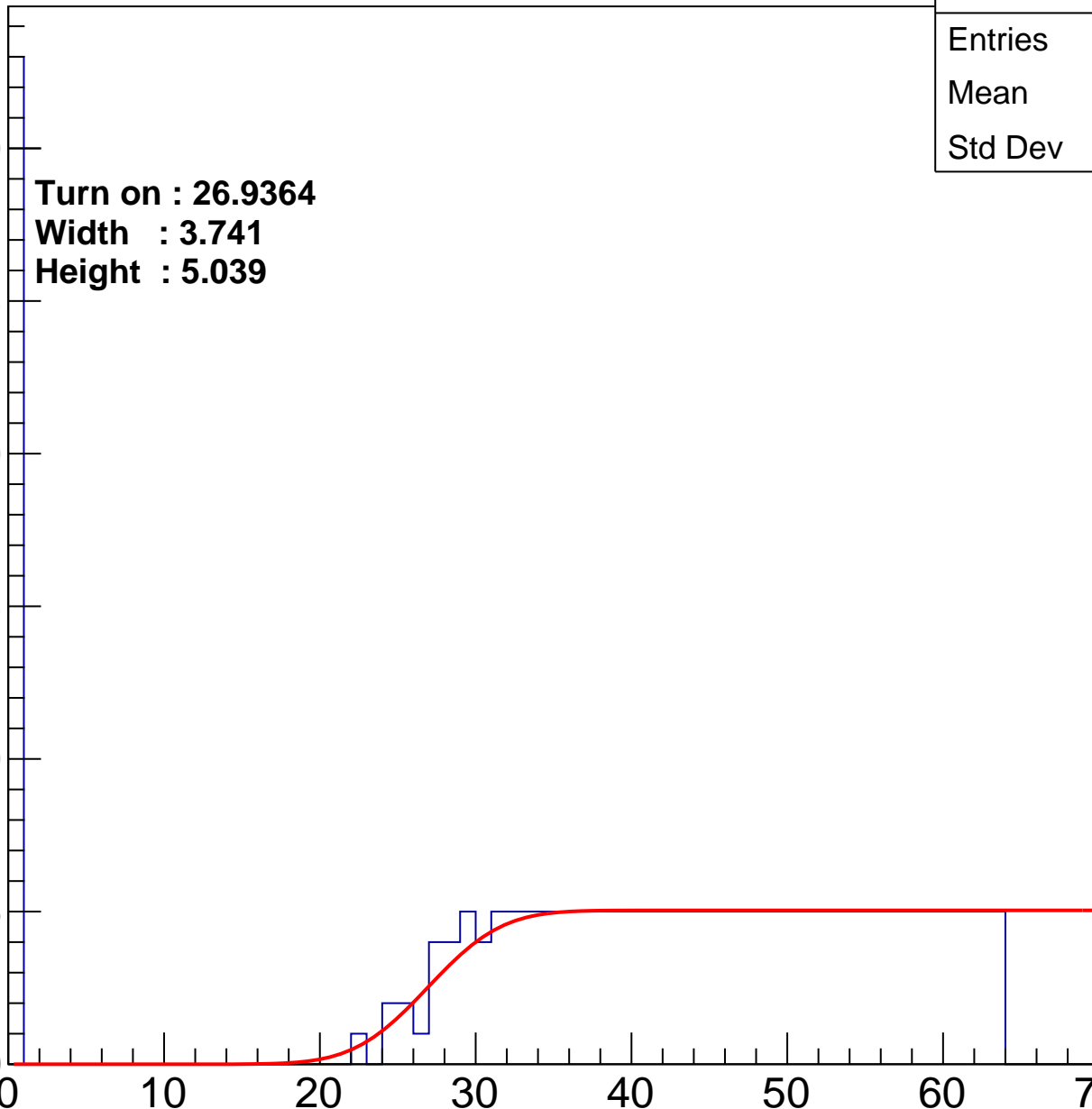
40

50

60

70

ampl



# B1L103S, U14-ch22

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 217   |
| Mean    | 38.99 |
| Std Dev | 17.82 |

**Turn on : 25.9442**

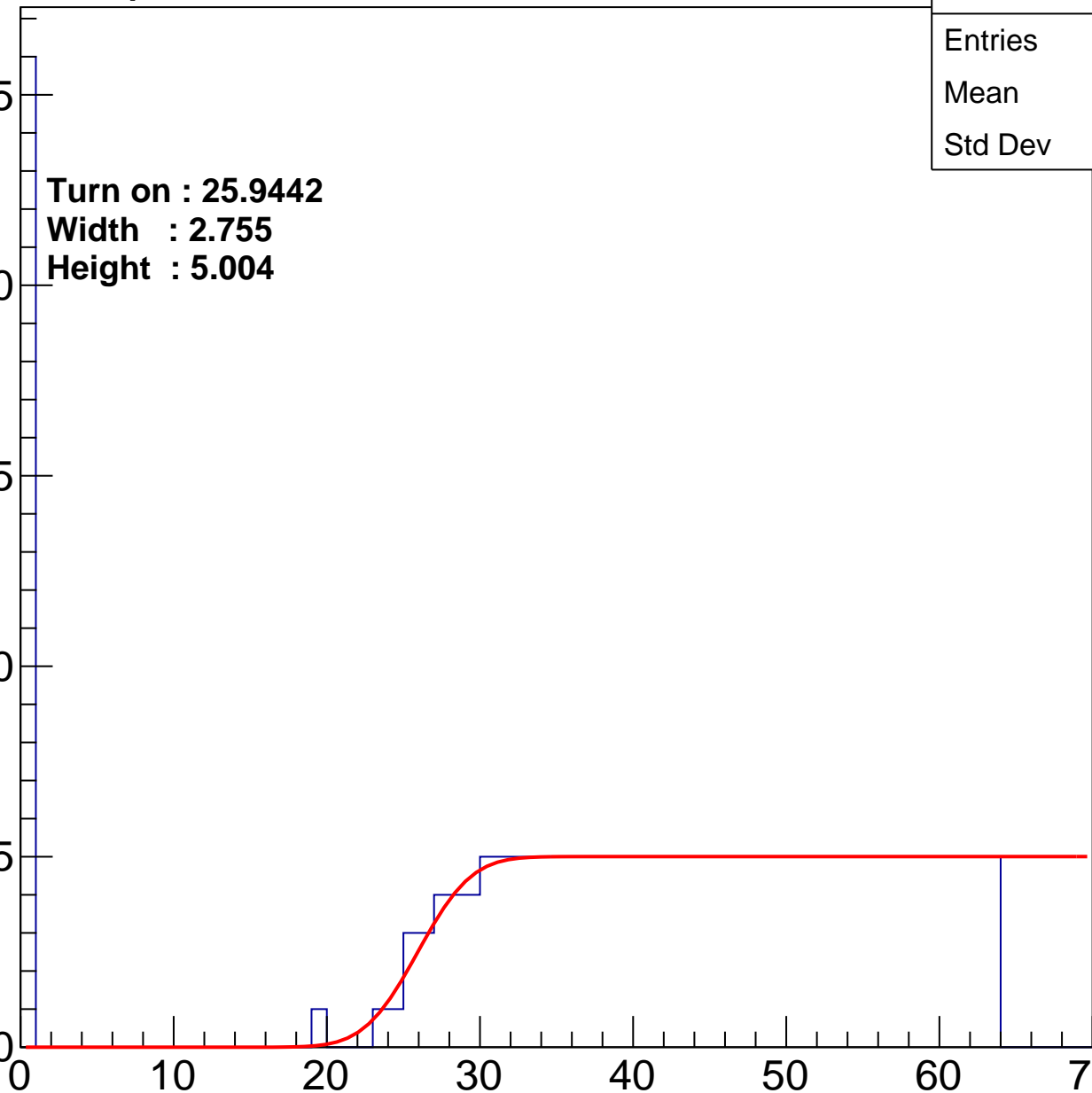
**Width : 2.755**

**Height : 5.004**

Entry

25  
20  
15  
10  
5  
0

ampl

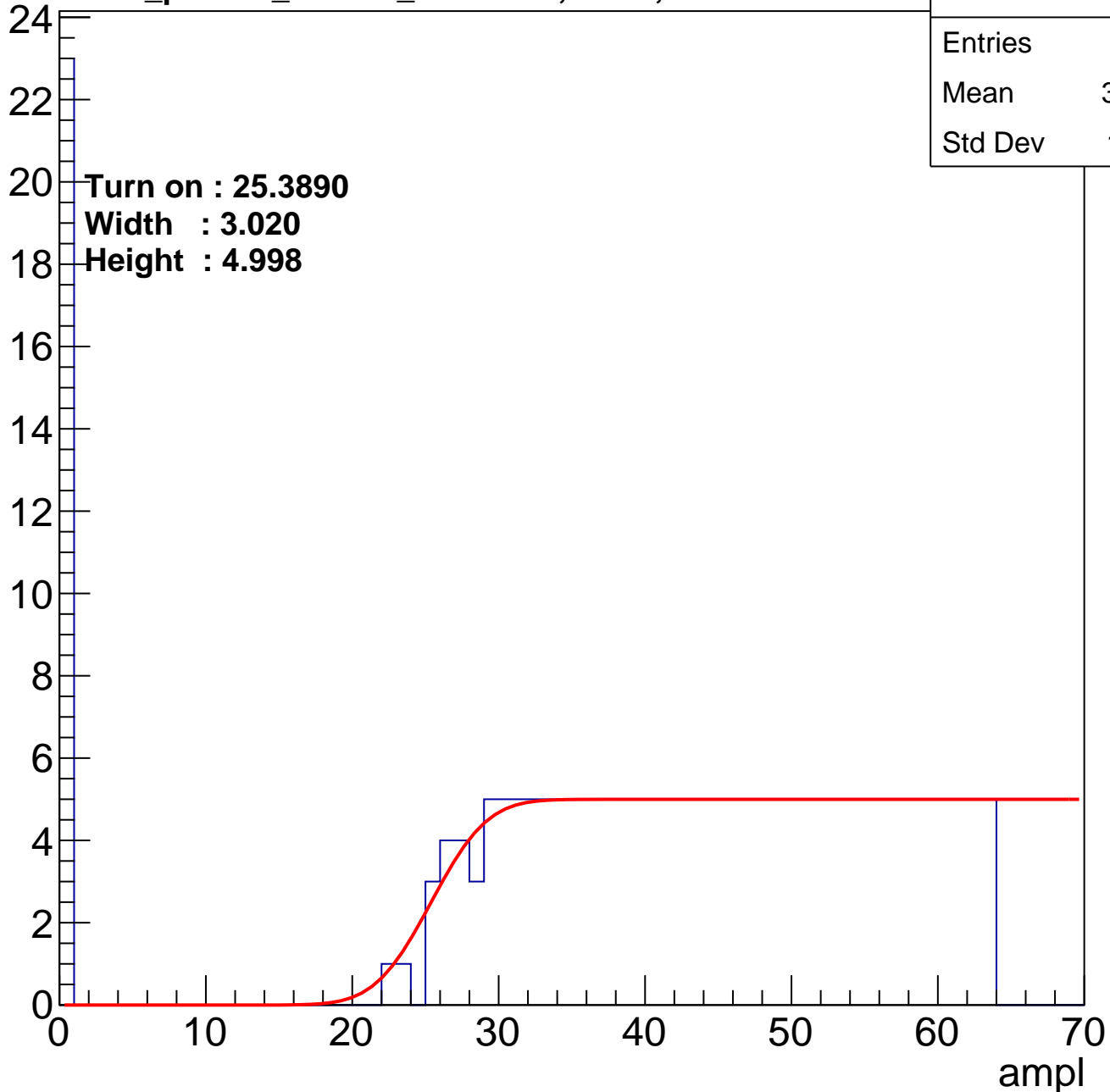


# B1L103S, U14-ch23

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 214   |
| Mean    | 39.56 |
| Std Dev | 17.31 |

Entry





# B1L103S, U14-ch24

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 218   |
| Mean    | 38.82 |
| Std Dev | 17.96 |

**Turn on : 25.8456**

**Width : 3.293**

**Height : 5.017**

Entry

25

20

15

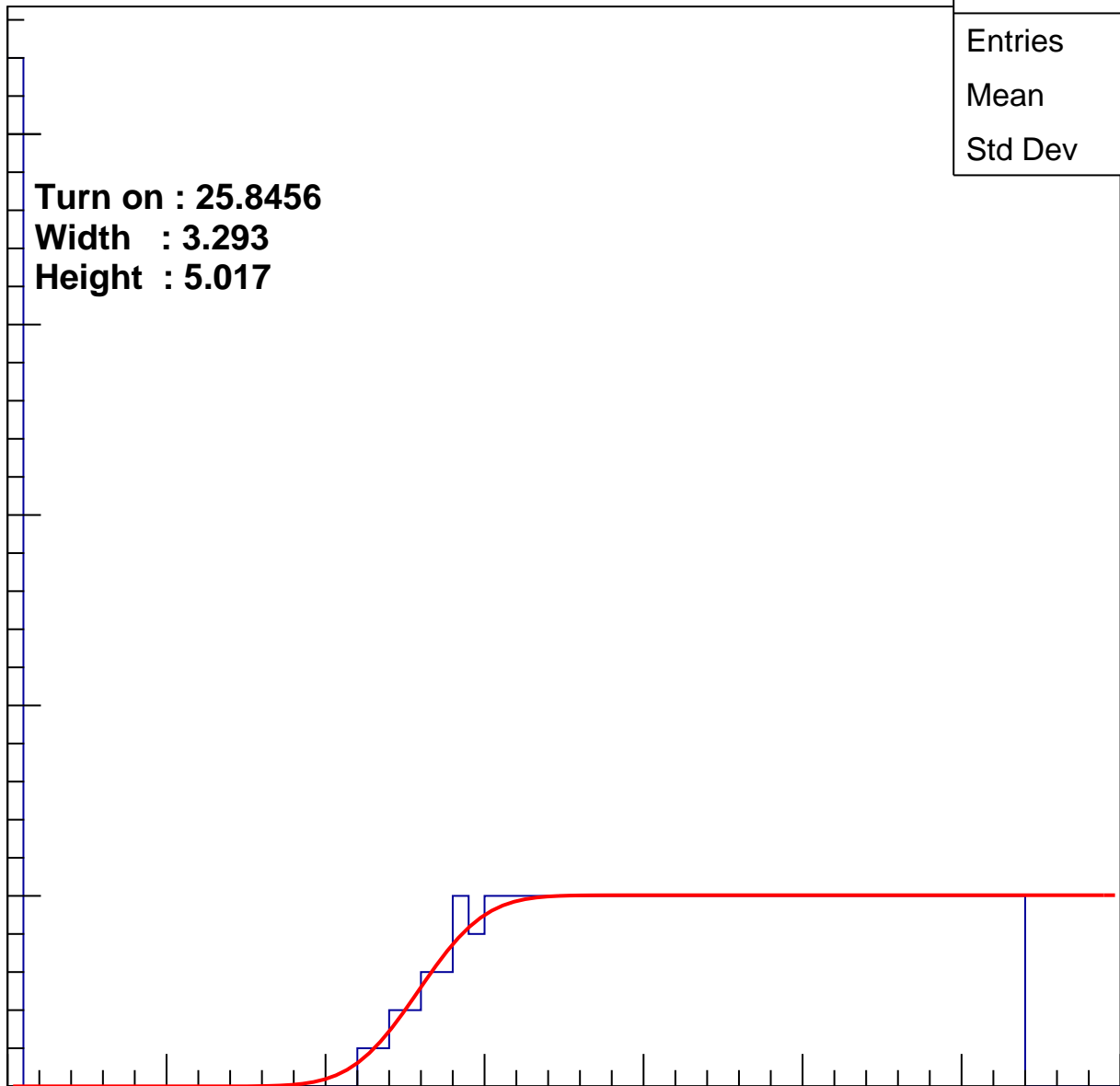
10

5

0

0 10 20 30 40 50 60 70

ampl



# B1L103S, U14-ch25

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 210   |
| Mean    | 39.4  |
| Std Dev | 17.97 |

**Turn on : 27.6974**

**Width : 2.334**

**Height : 5.004**

Entry

25

20

15

10

5

0

0

10

20

30

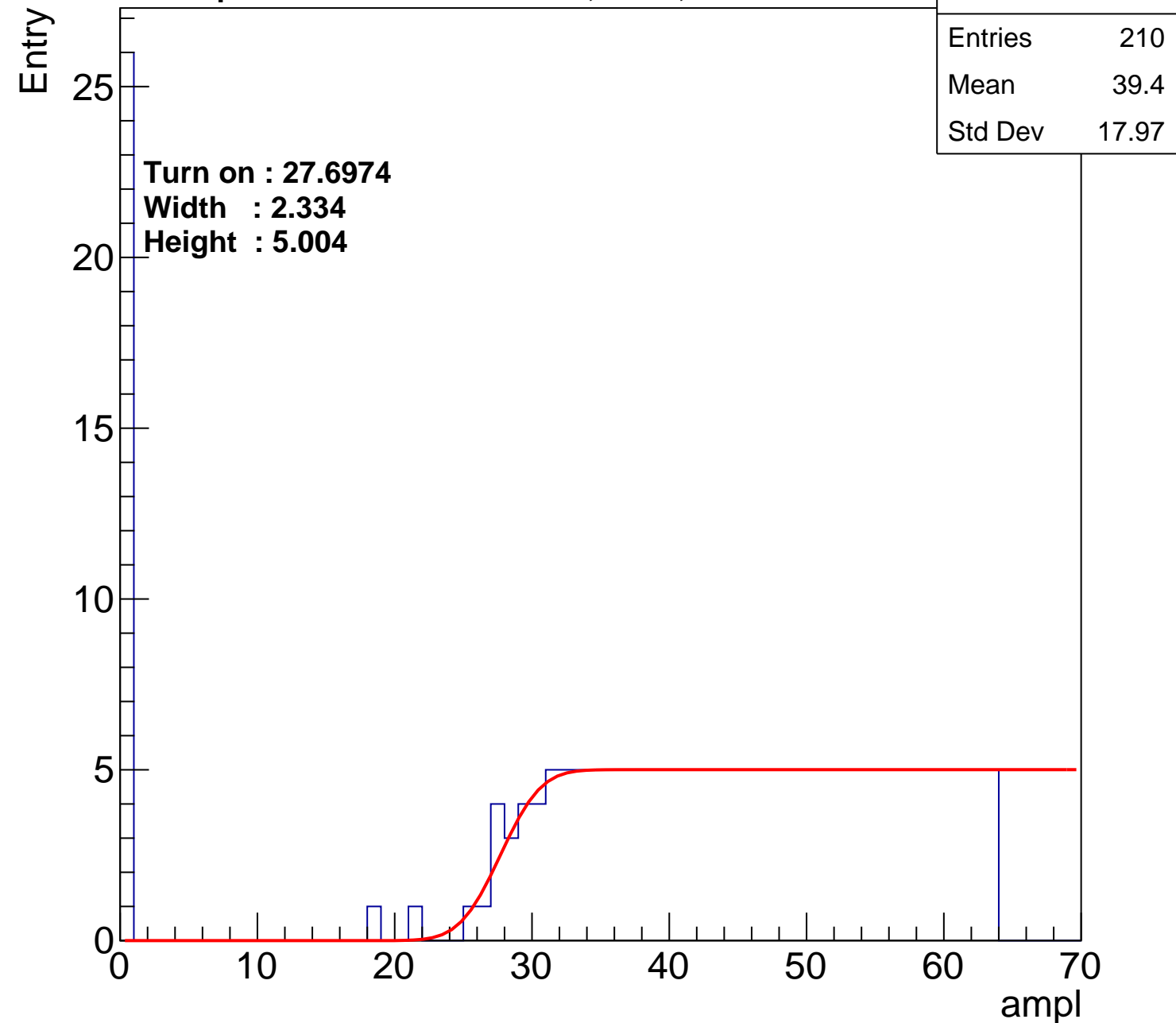
40

50

60

70

ampl



# B1L103S, U14-ch26

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 220   |
| Mean    | 38.23 |
| Std Dev | 18.58 |

**Turn on : 26.3271**

**Width : 3.213**

**Height : 5.021**

Entry

30

25

20

15

10

5

0

0

10

20

30

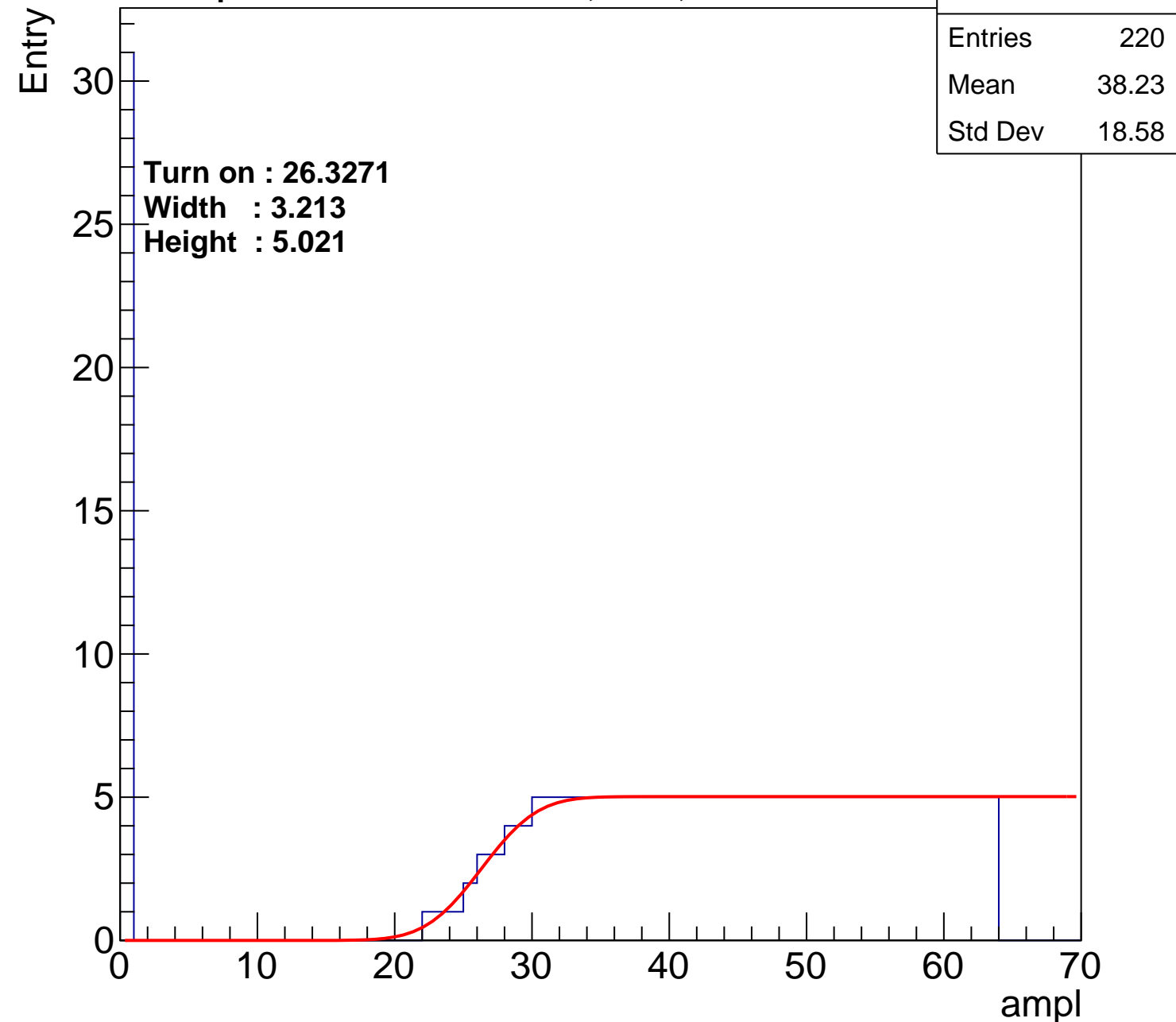
40

50

60

70

ampl



# B1L103S, U14-ch27

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 215   |
| Mean    | 39.26 |
| Std Dev | 17.65 |

Turn on : 25.9071

Width : 3.451

Height : 5.025

Entry

25

20

15

10

5

0

ampl

0

10

20

30

40

50

60

70

# B1L103S, U14-ch28

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 224   |
| Mean    | 37.77 |
| Std Dev | 18.8  |

**Turn on : 26.0236**

**Width : 3.234**

**Height : 5.000**

Entry

30

25

20

15

10

5

0

0

10

20

30

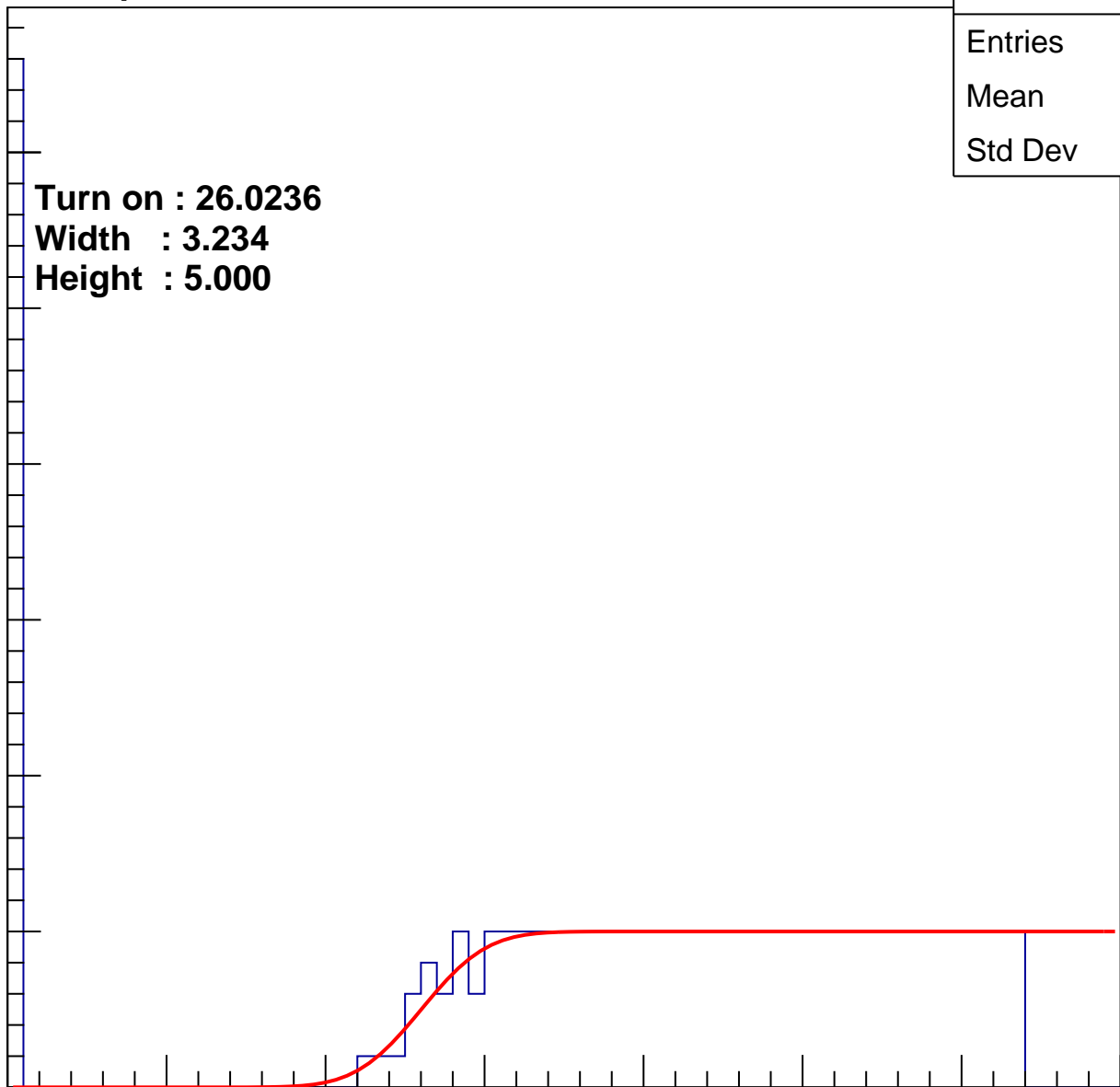
40

50

60

70

ampl



# B1L103S, U14-ch29

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 208   |
| Mean    | 39.56 |
| Std Dev | 17.97 |

**Turn on : 28.2164**

**Width : 3.465**

**Height : 5.045**

Entry

25

20

15

10

5

0

0

10

20

30

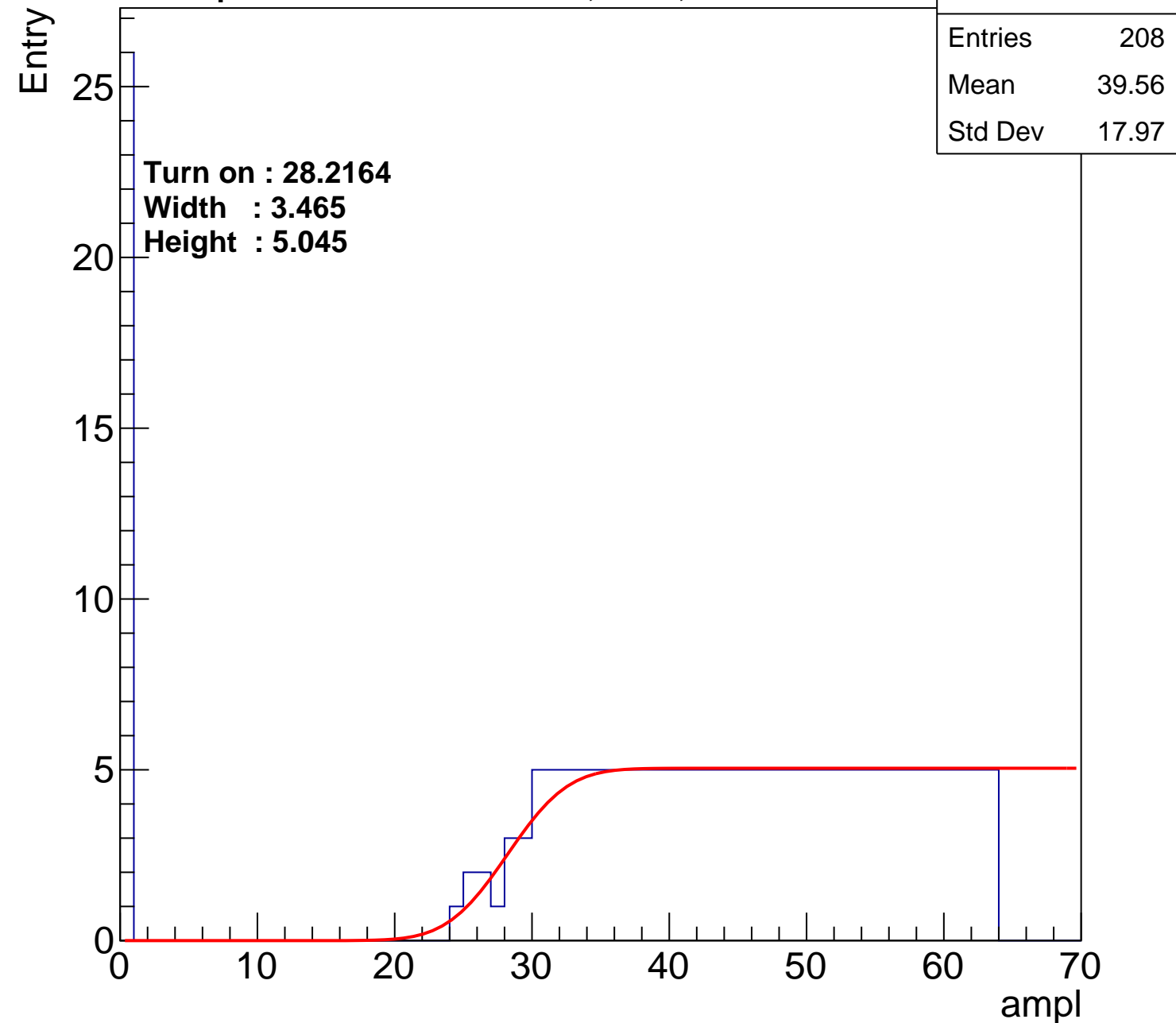
40

50

60

70

ampl



# B1L103S, U14-ch30

calib\_packv5\_041523\_1651.root, FC#0, Port C2

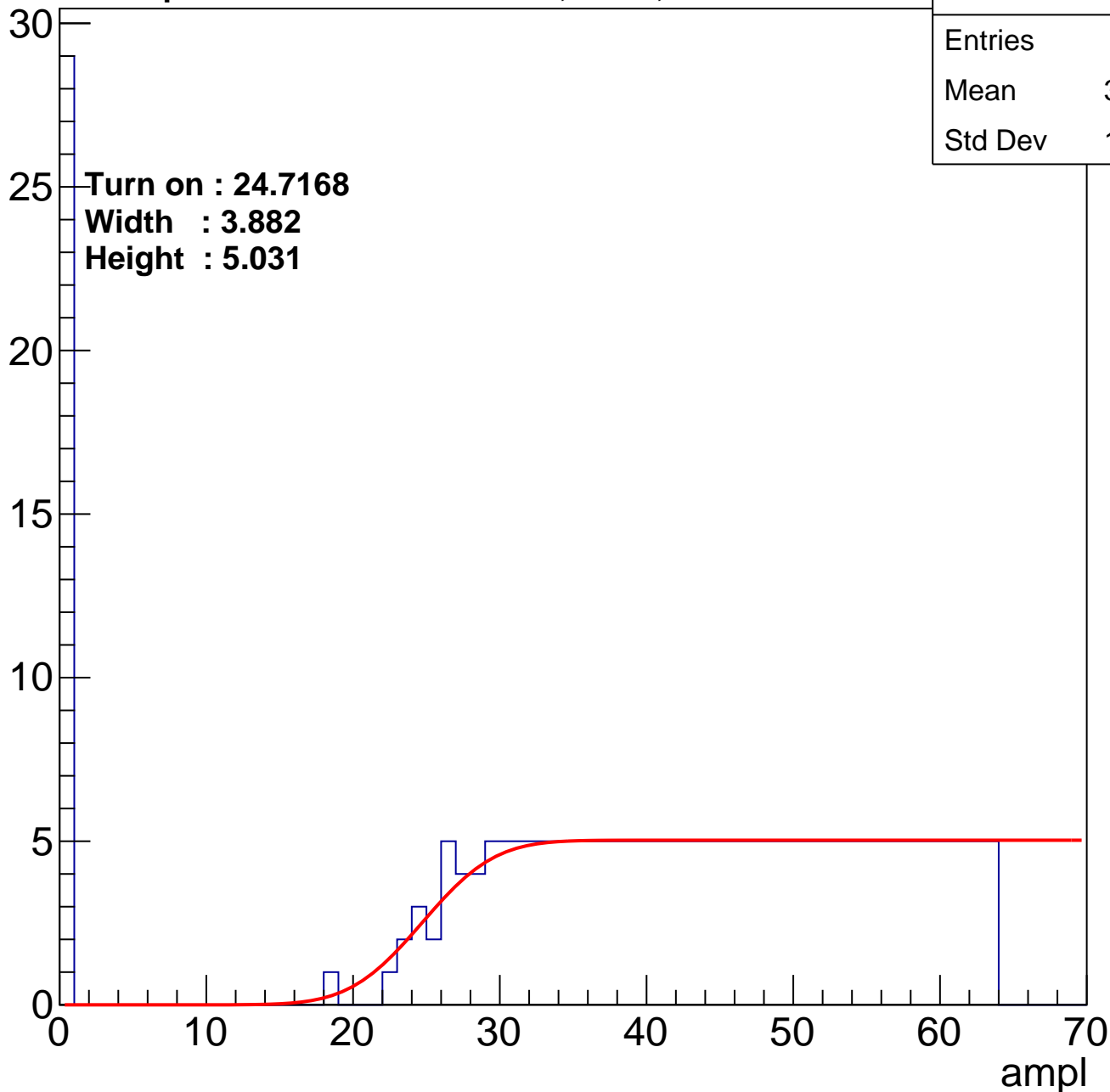
|         |       |
|---------|-------|
| Entries | 226   |
| Mean    | 38.09 |
| Std Dev | 18.16 |

Turn on : 24.7168

Width : 3.882

Height : 5.031

Entry



# B1L103S, U14-ch31

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 220   |
| Mean    | 37.99 |
| Std Dev | 18.9  |

**Turn on : 25.2953**

**Width : 4.277**

**Height : 5.035**

Entry

30

25

20

15

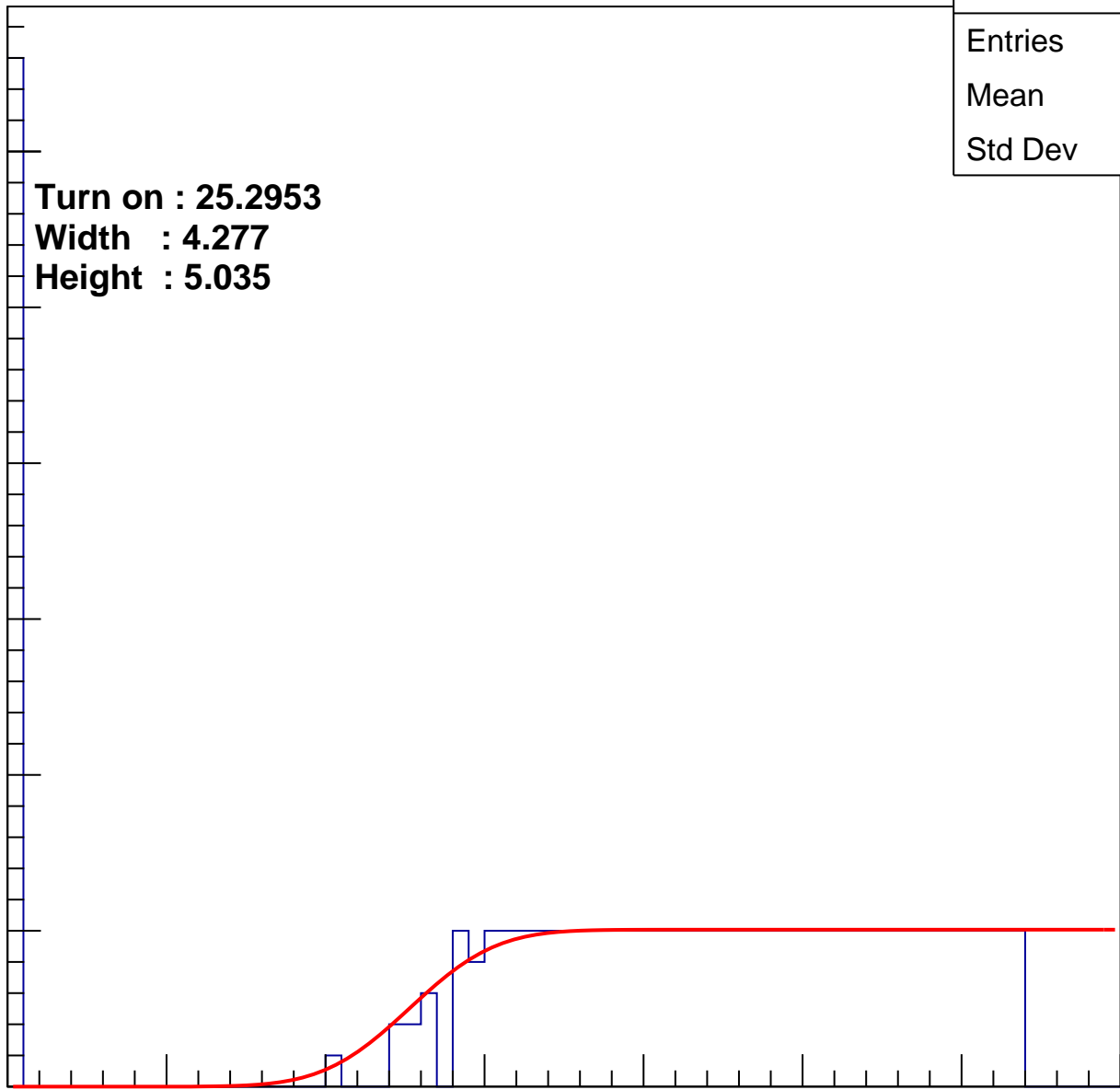
10

5

0

ampl

0 10 20 30 40 50 60 70





# B1L103S, U14-ch32

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 215   |
| Mean    | 39.27 |
| Std Dev | 17.65 |

**Turn on : 25.9151**

**Width : 2.304**

**Height : 4.987**

Entry

25

20

15

10

5

0

ampl

0

10

20

30

40

50

60

70

# B1L103S, U14-ch33

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 215   |
| Mean    | 39    |
| Std Dev | 18.02 |

**Turn on : 27.0351**

**Width : 3.652**

**Height : 5.050**

Entry

25

20

15

10

5

0

0

10

20

30

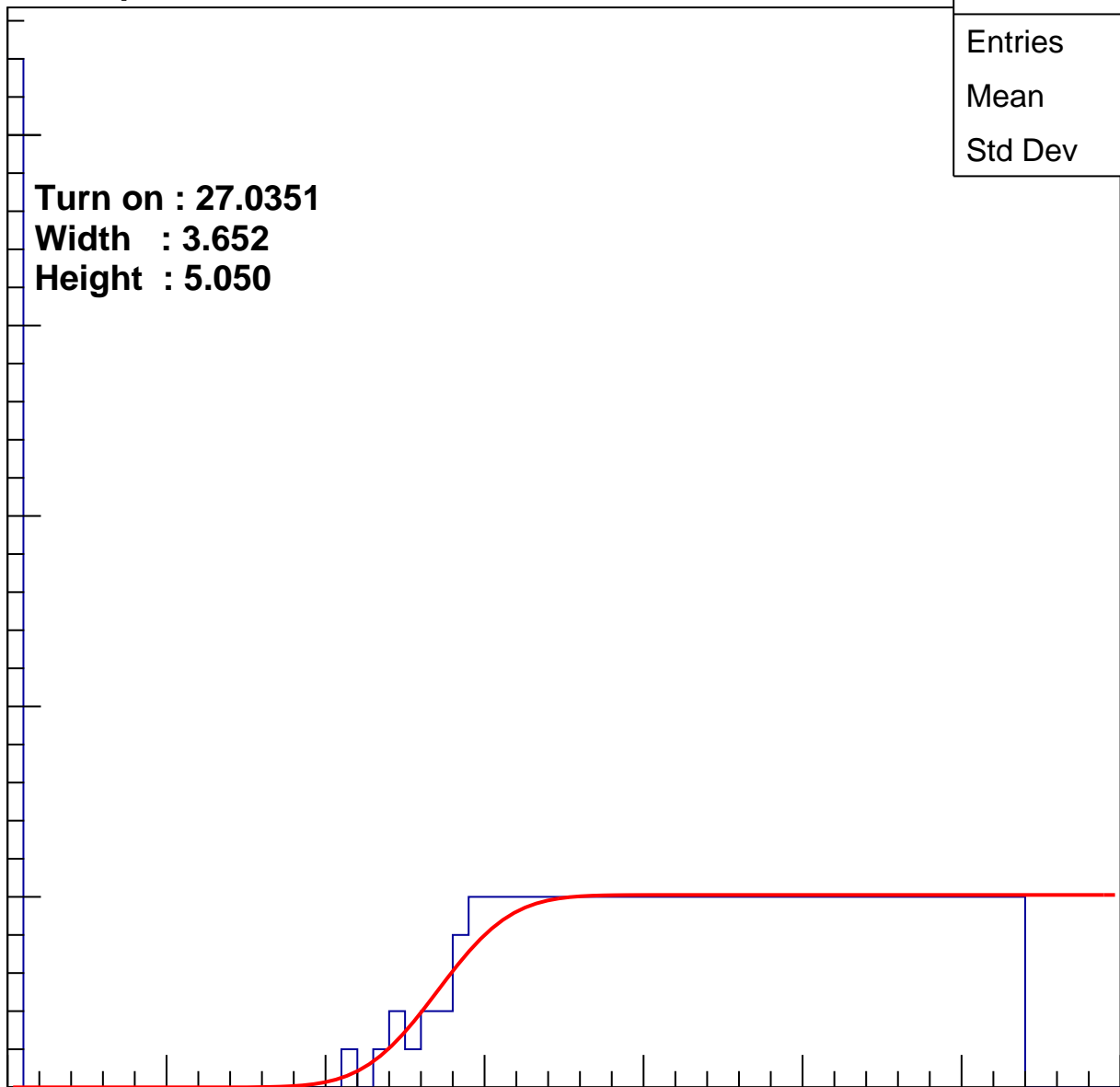
40

50

60

70

ampl



# B1L103S, U14-ch34

calib\_packv5\_041523\_1651.root, FC#0, Port C2

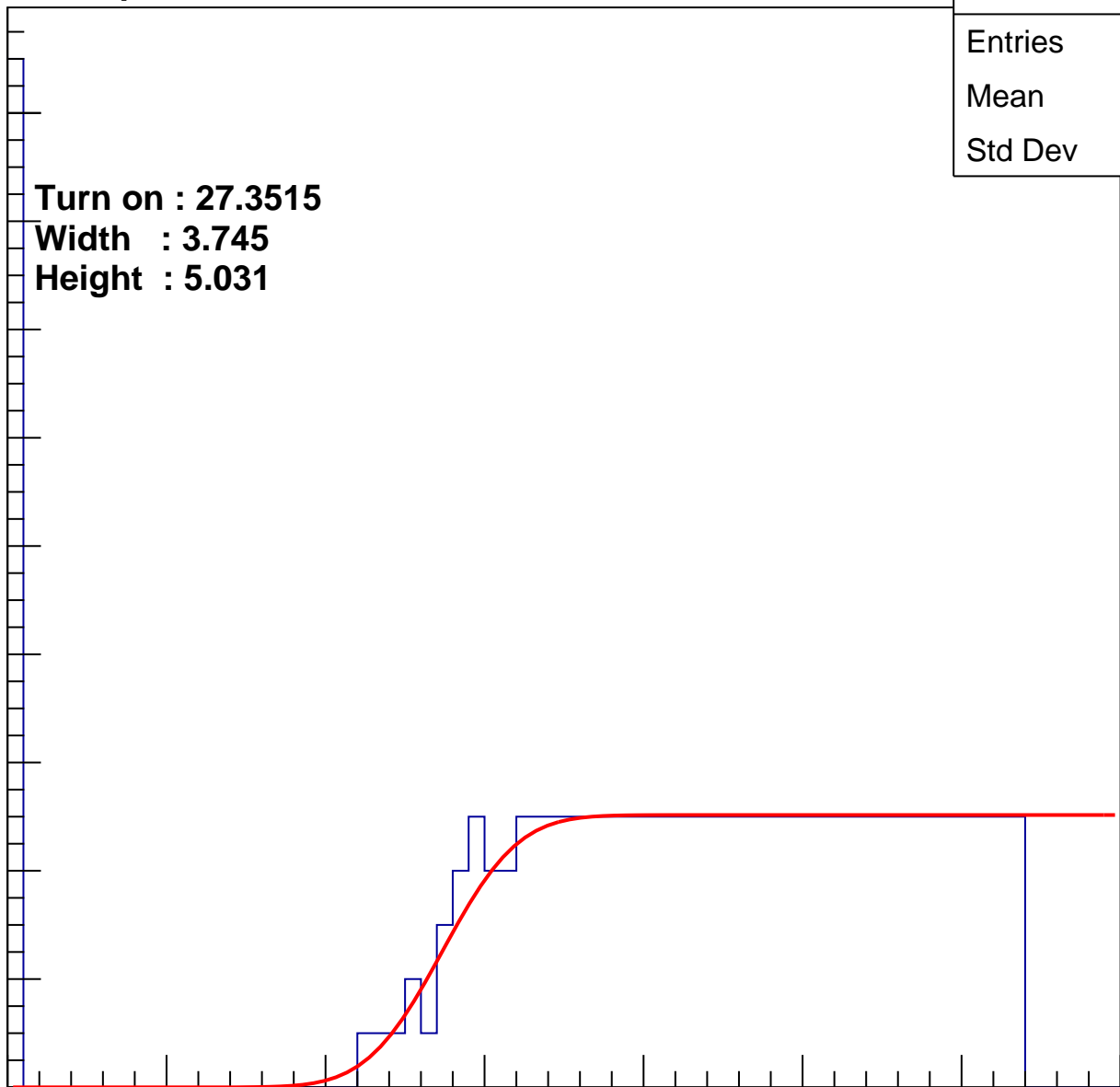
Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 27.3515**  
**Width : 3.745**  
**Height : 5.031**

|         |       |
|---------|-------|
| Entries | 205   |
| Mean    | 40.62 |
| Std Dev | 16.66 |

ampl



# B1L103S, U14-ch35

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 219   |
| Mean    | 38.73 |
| Std Dev | 17.96 |

**Turn on : 25.6081**

**Width : 3.491**

**Height : 5.003**

Entry

25

20

15

10

5

0

0

10

20

30

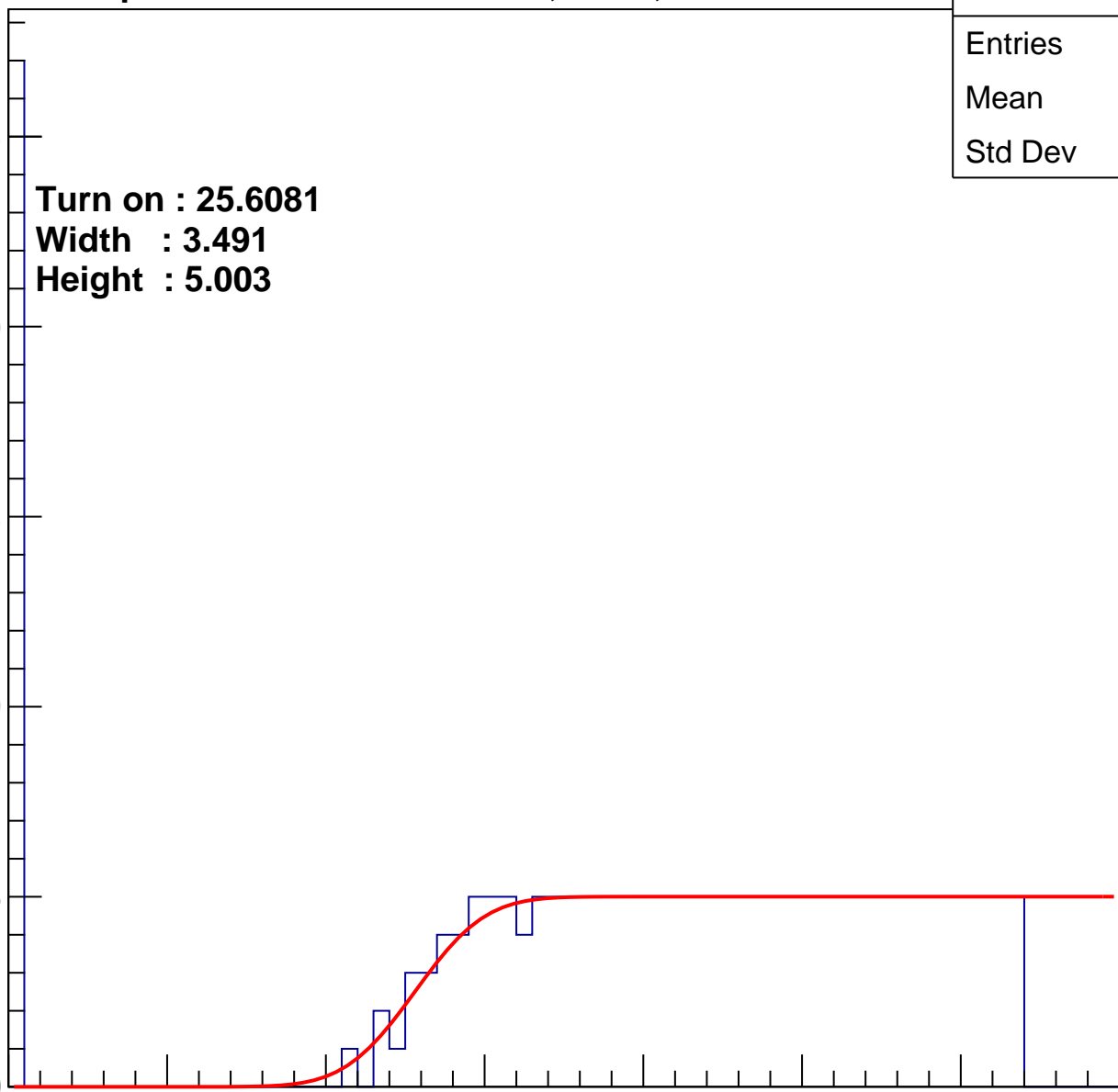
40

50

60

70

ampl



# B1L103S, U14-ch36

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 218   |
| Mean    | 38.67 |
| Std Dev | 18.15 |

**Turn on : 26.6298**

**Width : 4.044**

**Height : 5.046**

Entry

25

20

15

10

5

0

0

10

20

30

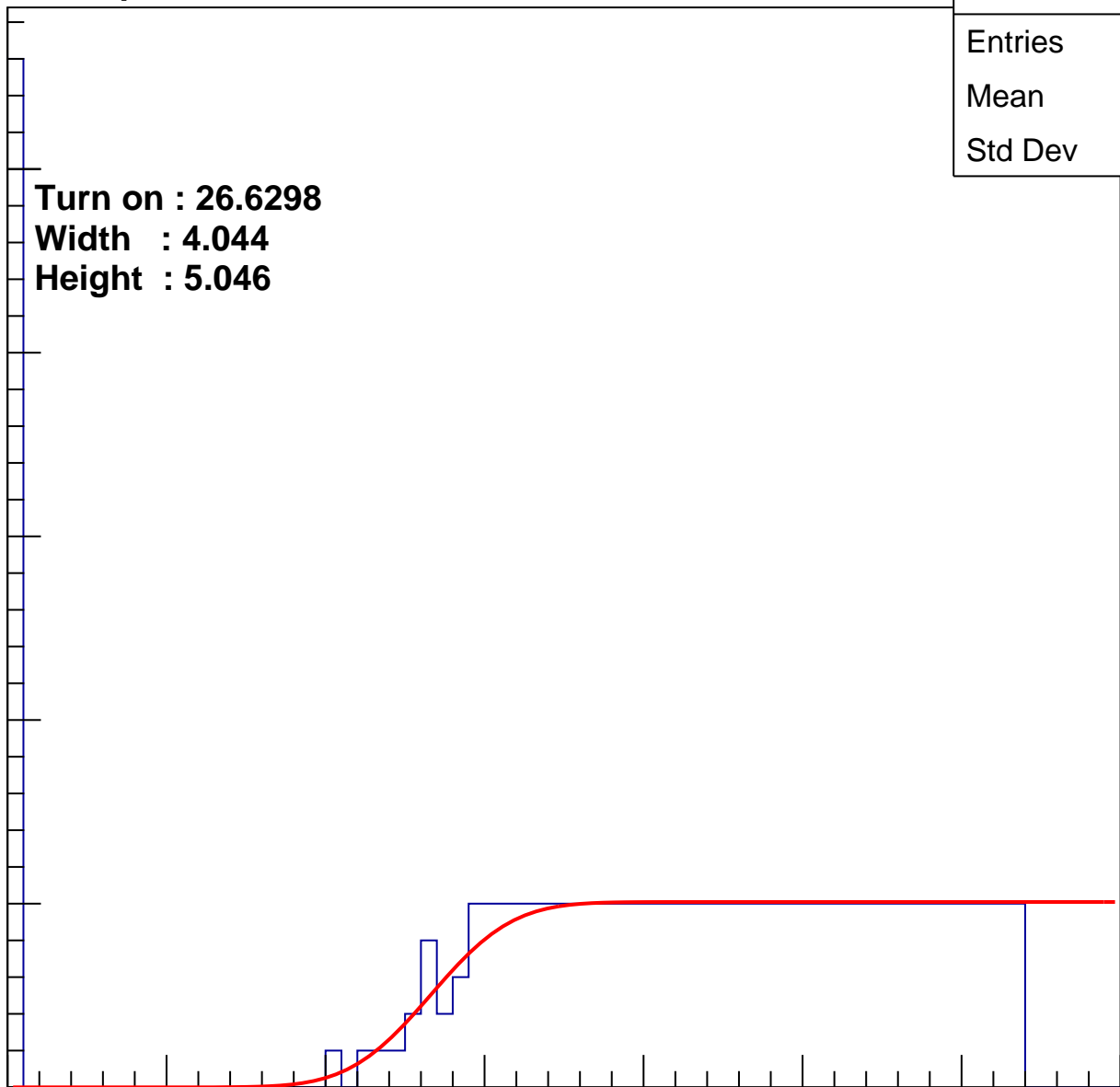
40

50

60

70

ampl



# B1L103S, U14-ch37

calib\_packv5\_041523\_1651.root, FC#0, Port C2

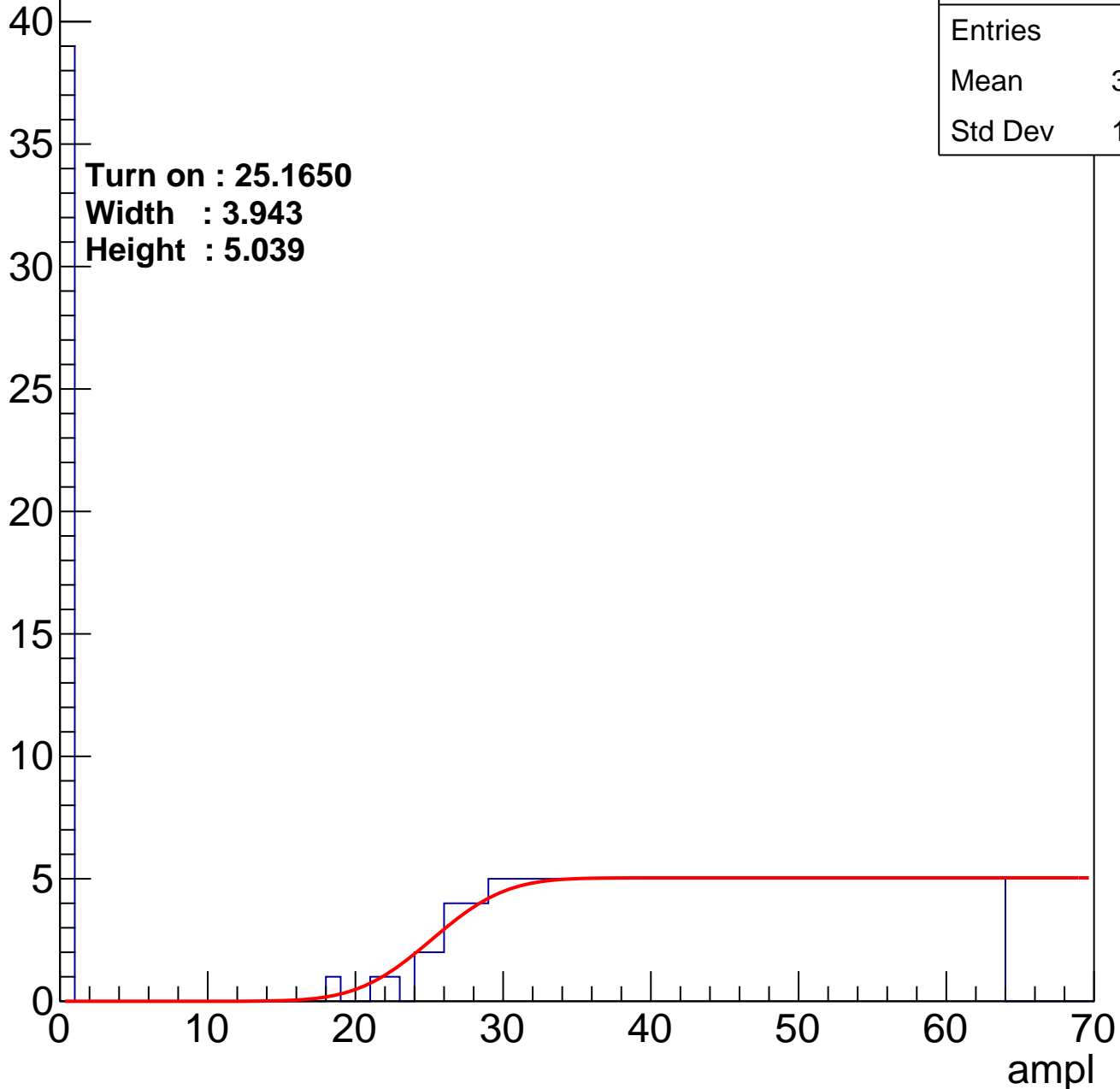
|         |       |
|---------|-------|
| Entries | 233   |
| Mean    | 36.62 |
| Std Dev | 19.44 |

**Turn on : 25.1650**

**Width : 3.943**

**Height : 5.039**

Entry



# B1L103S, U14-ch38

calib\_packv5\_041523\_1651.root, FC#0, Port C2

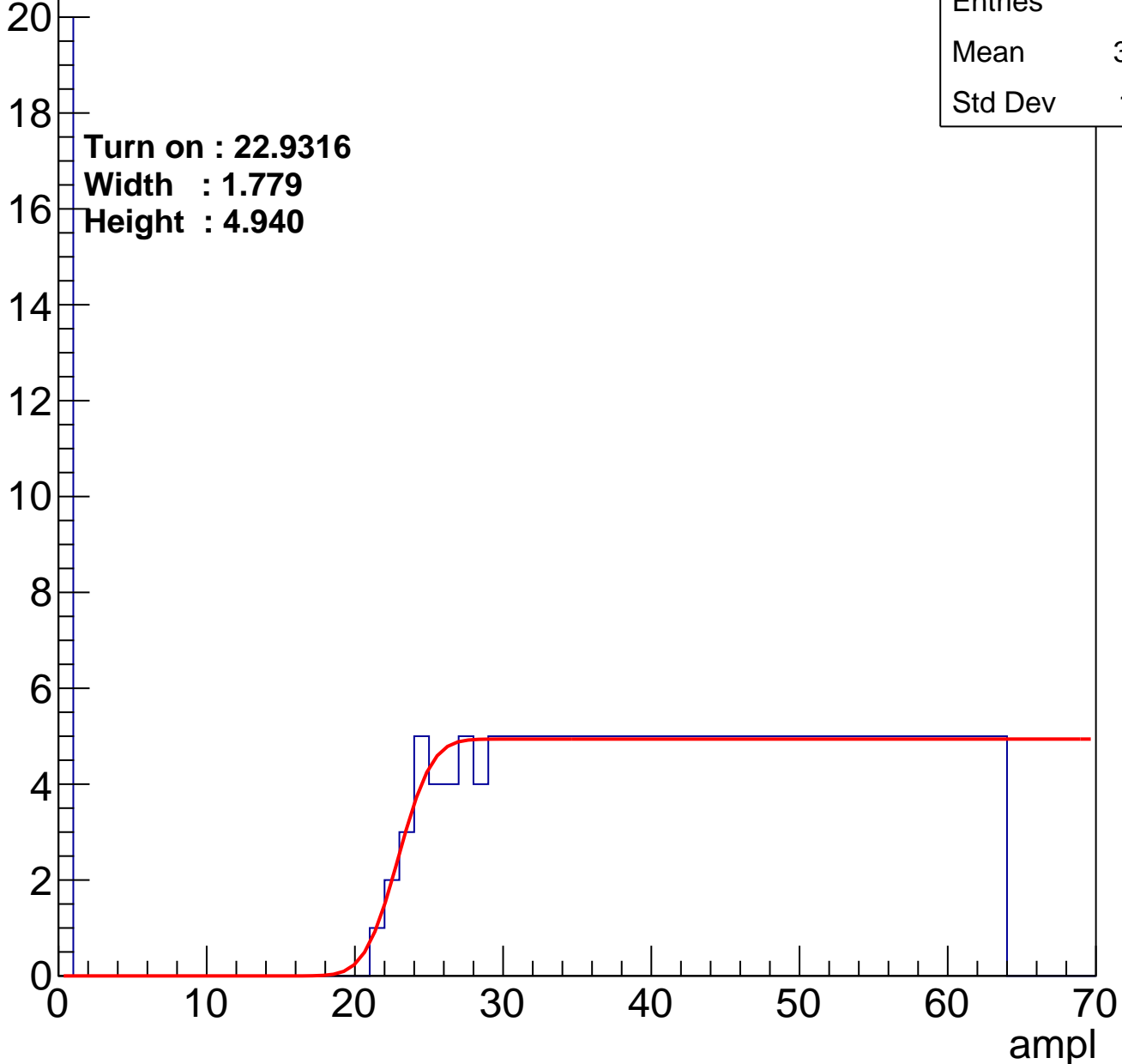
|         |       |
|---------|-------|
| Entries | 223   |
| Mean    | 39.26 |
| Std Dev | 16.71 |

**Turn on : 22.9316**

**Width : 1.779**

**Height : 4.940**

Entry



# B1L103S, U14-ch39

calib\_packv5\_041523\_1651.root, FC#0, Port C2

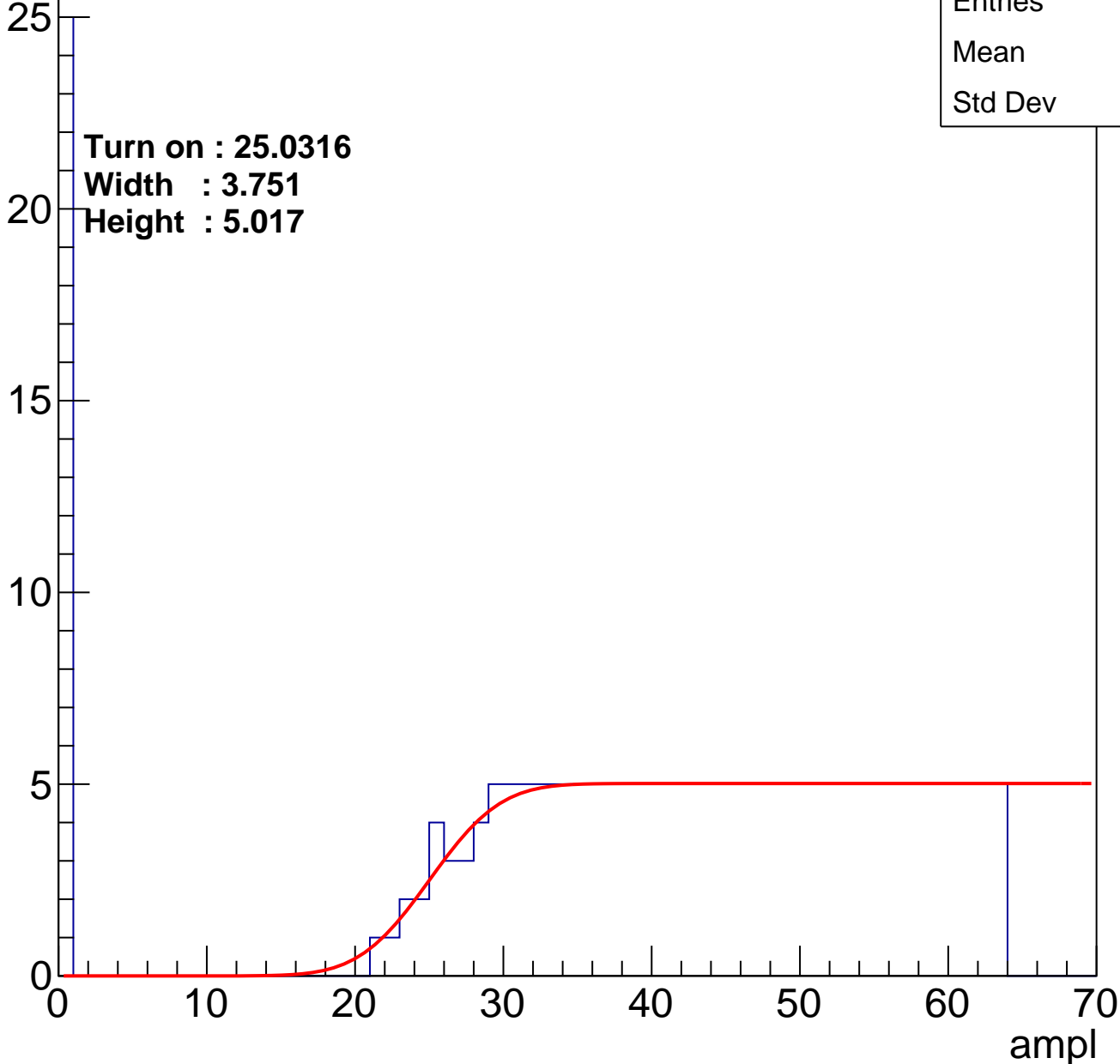
|         |       |
|---------|-------|
| Entries | 220   |
| Mean    | 38.9  |
| Std Dev | 17.61 |

Turn on : 25.0316

Width : 3.751

Height : 5.017

Entry





# B1L103S, U14-ch40

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 221   |
| Mean    | 38.83 |
| Std Dev | 17.77 |

**Turn on : 25.1515**

**Width : 3.307**

**Height : 5.007**

Entry

25

20

15

10

5

0

ampl

0

10

20

30

40

50

60

70

# B1L103S, U14-ch41

calib\_packv5\_041523\_1651.root, FC#0, Port C2

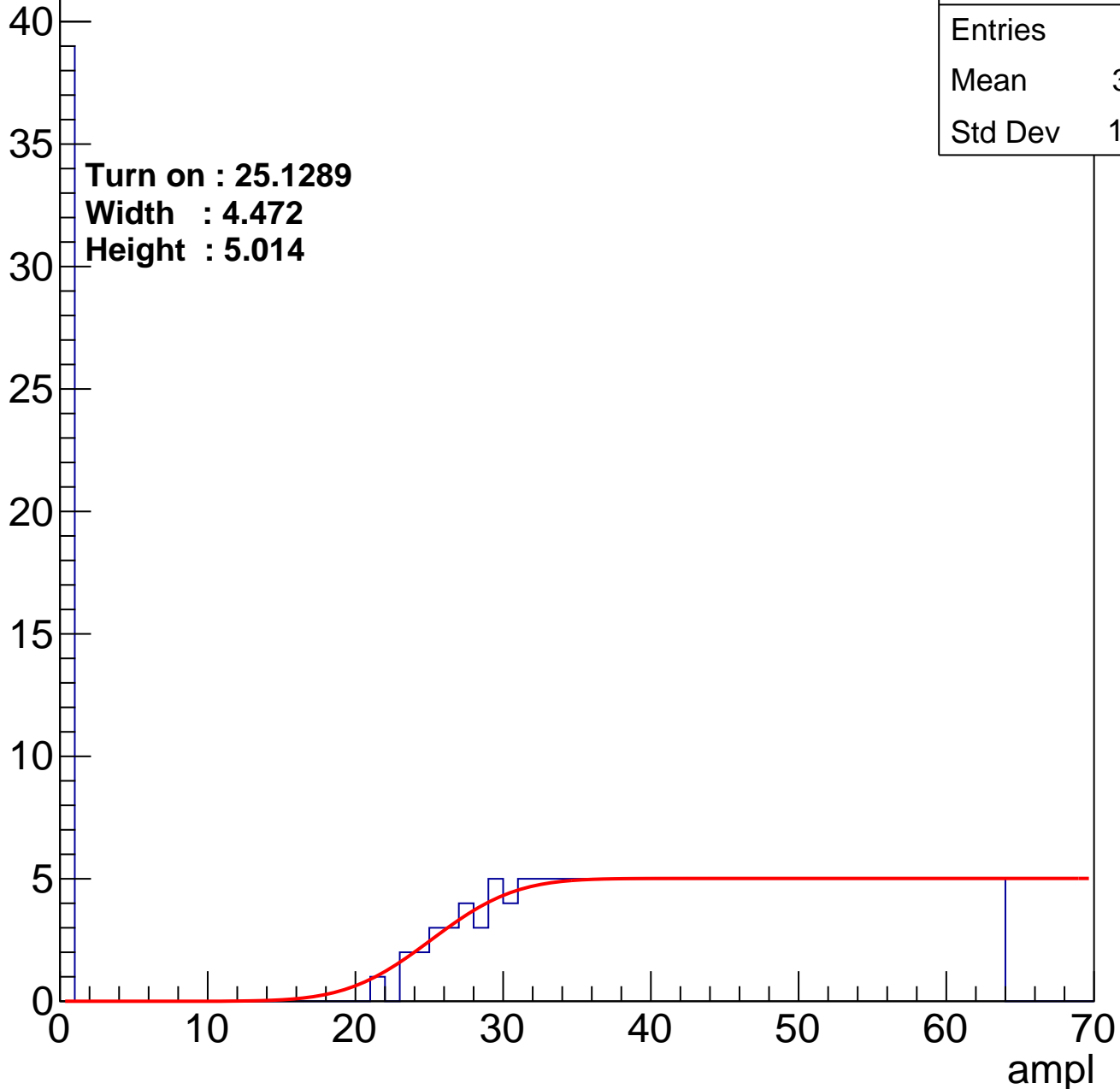
|         |       |
|---------|-------|
| Entries | 231   |
| Mean    | 36.71 |
| Std Dev | 19.49 |

**Turn on : 25.1289**

**Width : 4.472**

**Height : 5.014**

Entry



# B1L103S, U14-ch42

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 218   |
| Mean    | 38.8  |
| Std Dev | 17.98 |

**Turn on : 26.2056**

**Width : 3.453**

**Height : 5.034**

Entry

25

20

15

10

5

0

0

10

20

30

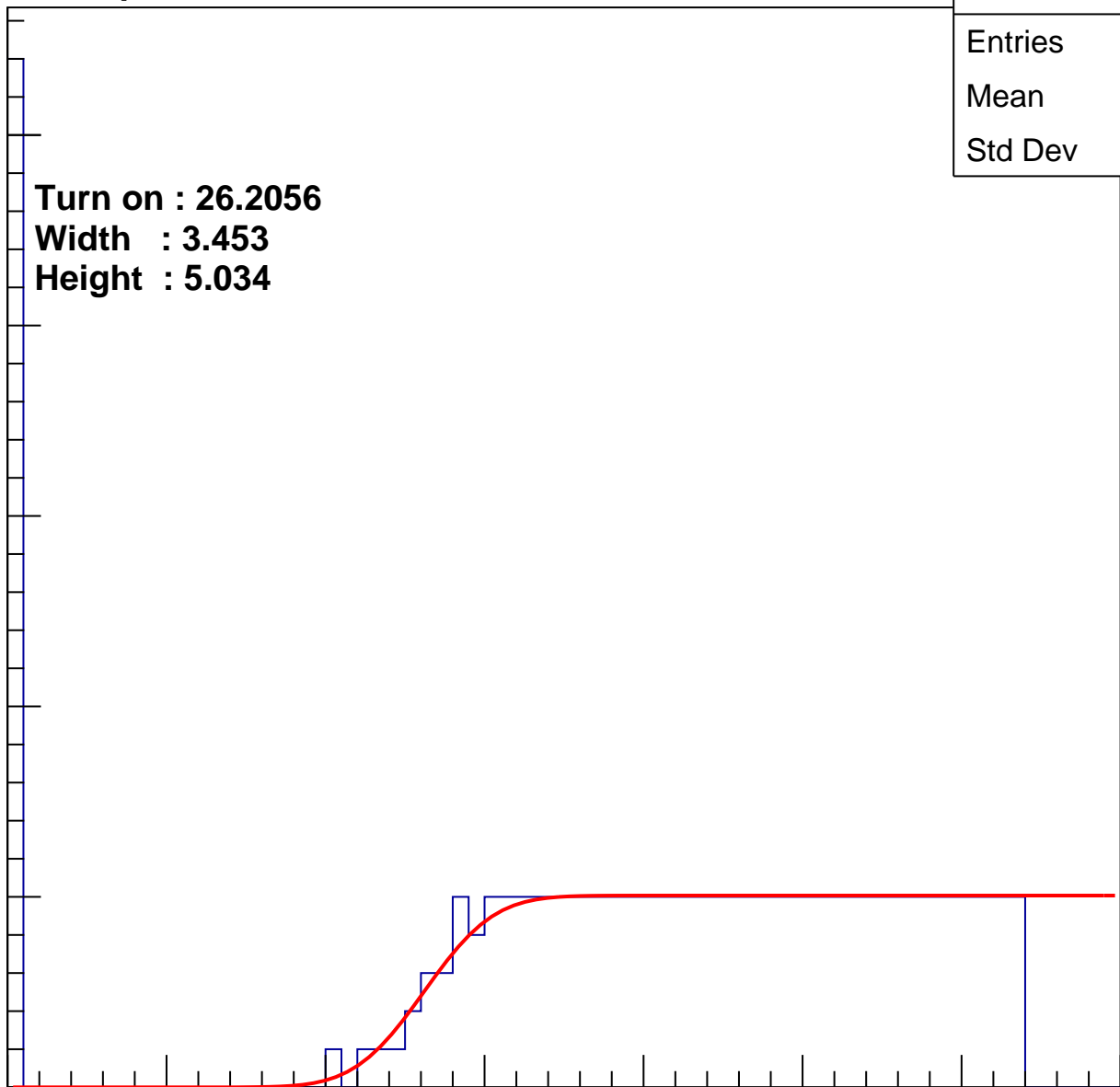
40

50

60

70

ampl



# B1L103S, U14-ch43

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 217   |
| Mean    | 39.02 |
| Std Dev | 17.79 |

**Turn on : 25.7068**

**Width : 2.843**

**Height : 5.002**

Entry

25

20

15

10

5

0

0

10

20

30

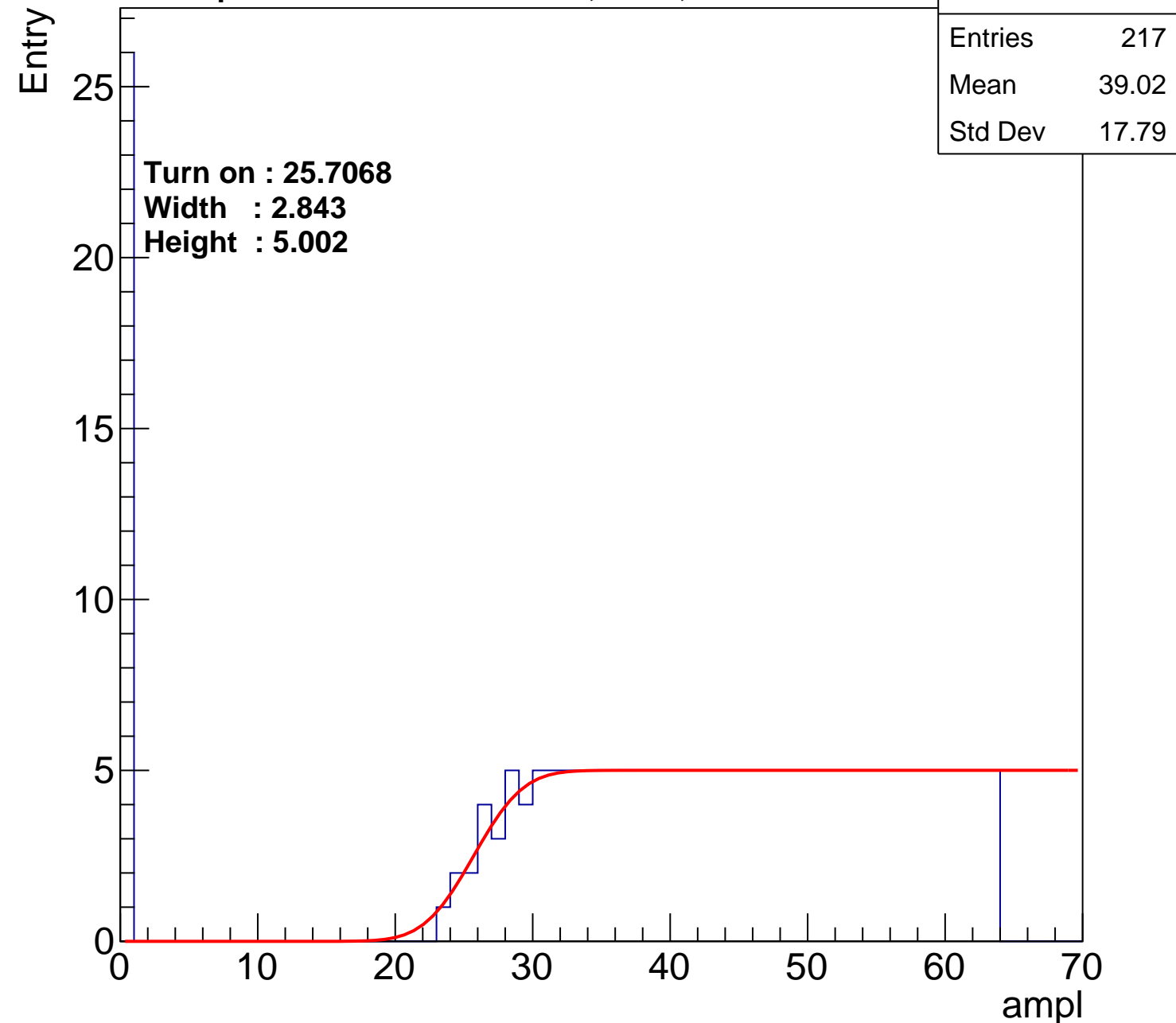
40

50

60

70

ampl



# B1L103S, U14-ch44

calib\_packv5\_041523\_1651.root, FC#0, Port C2

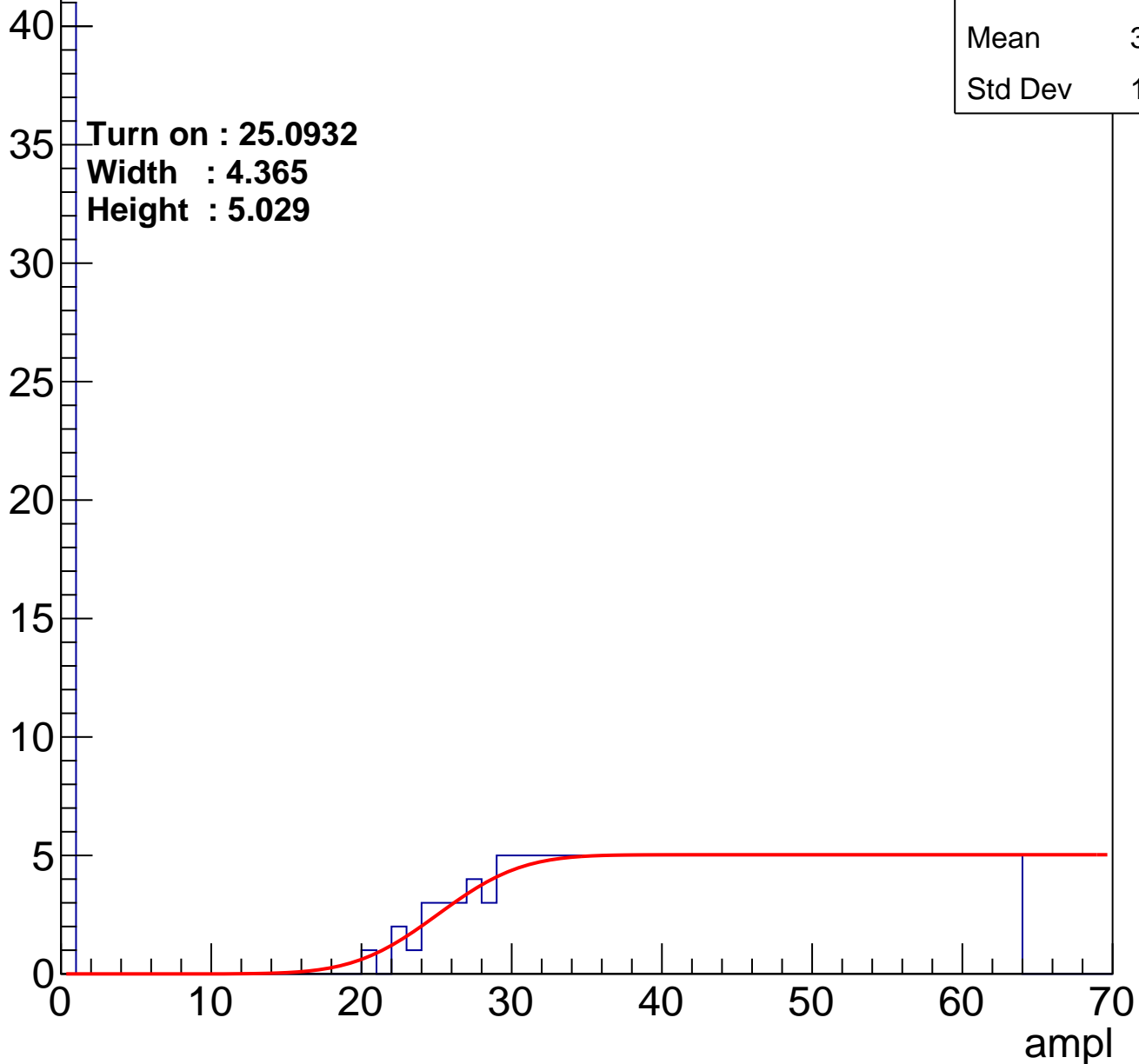
|         |       |
|---------|-------|
| Entries | 236   |
| Mean    | 36.25 |
| Std Dev | 19.63 |

Turn on : 25.0932

Width : 4.365

Height : 5.029

Entry



# B1L103S, U14-ch45

calib\_packv5\_041523\_1651.root, FC#0, Port C2

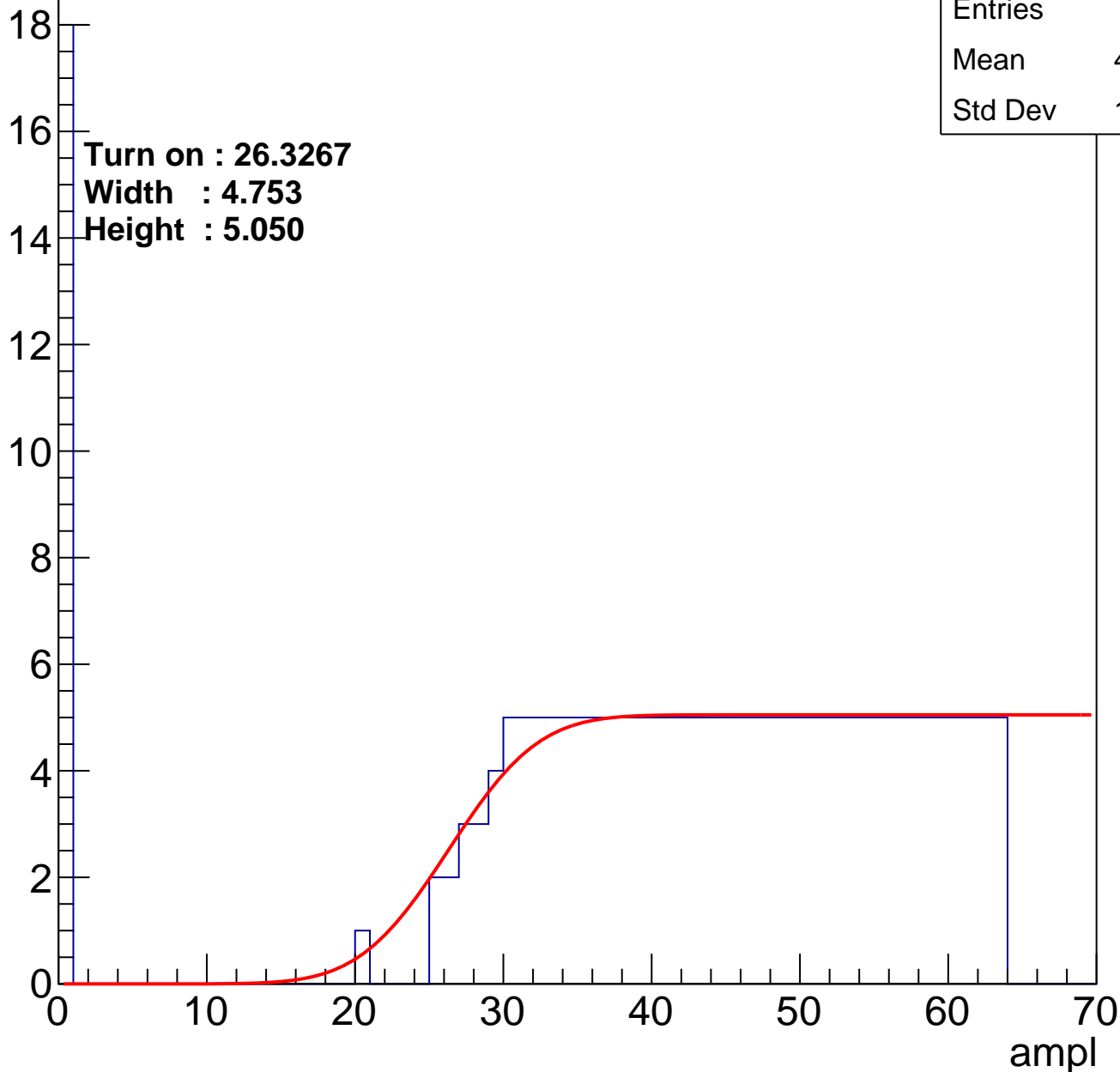
|         |       |
|---------|-------|
| Entries | 203   |
| Mean    | 40.93 |
| Std Dev | 16.44 |

**Turn on : 26.3267**

**Width : 4.753**

**Height : 5.050**

Entry



# B1L103S, U14-ch46

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 226   |
| Mean    | 37.86 |
| Std Dev | 18.48 |

**Turn on : 25.5206**

**Width : 4.263**

**Height : 5.051**

Entry

30

25

20

15

10

5

0

0

10

20

30

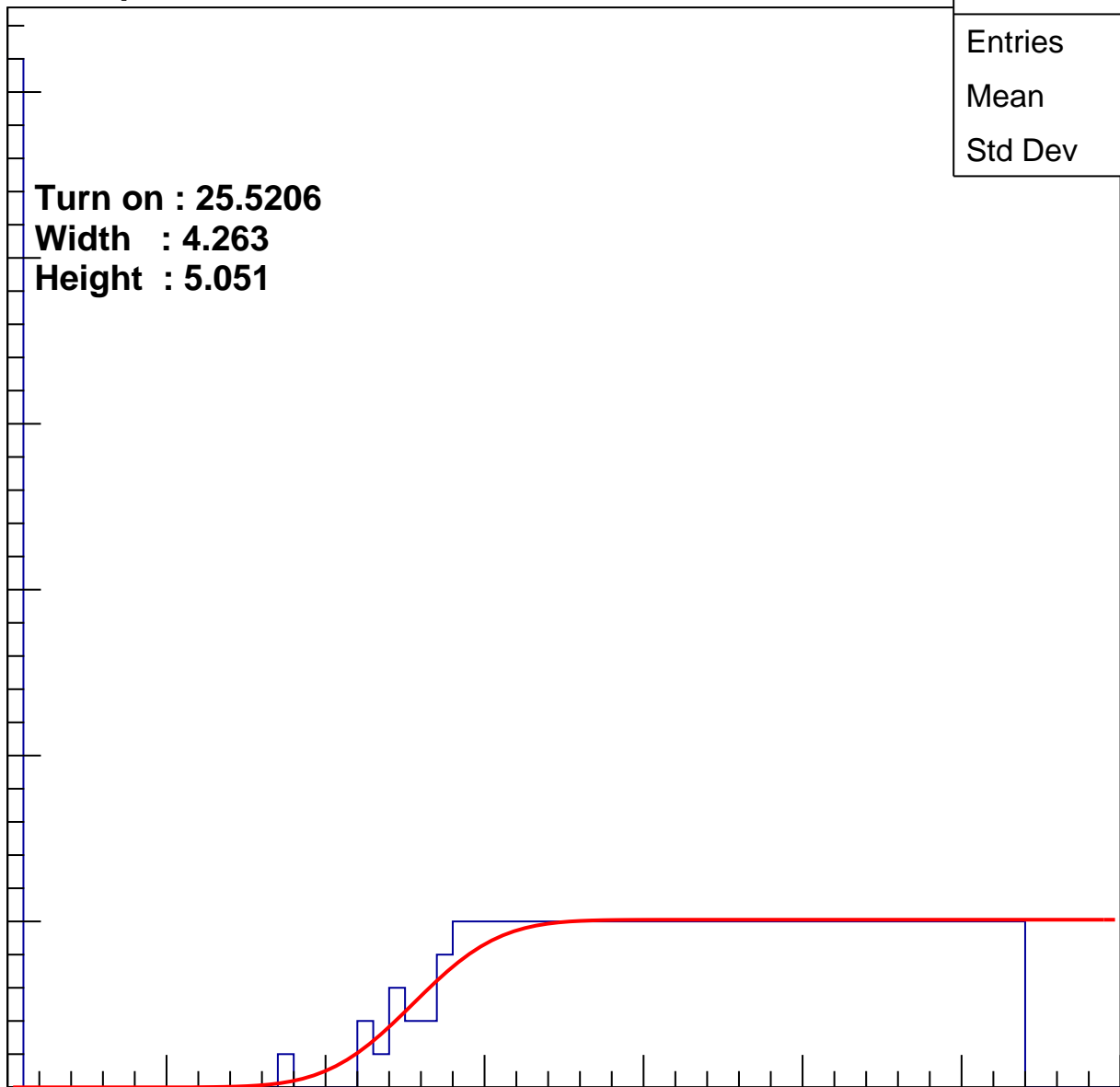
40

50

60

70

ampl



# B1L103S, U14-ch47

calib\_packv5\_041523\_1651.root, FC#0, Port C2

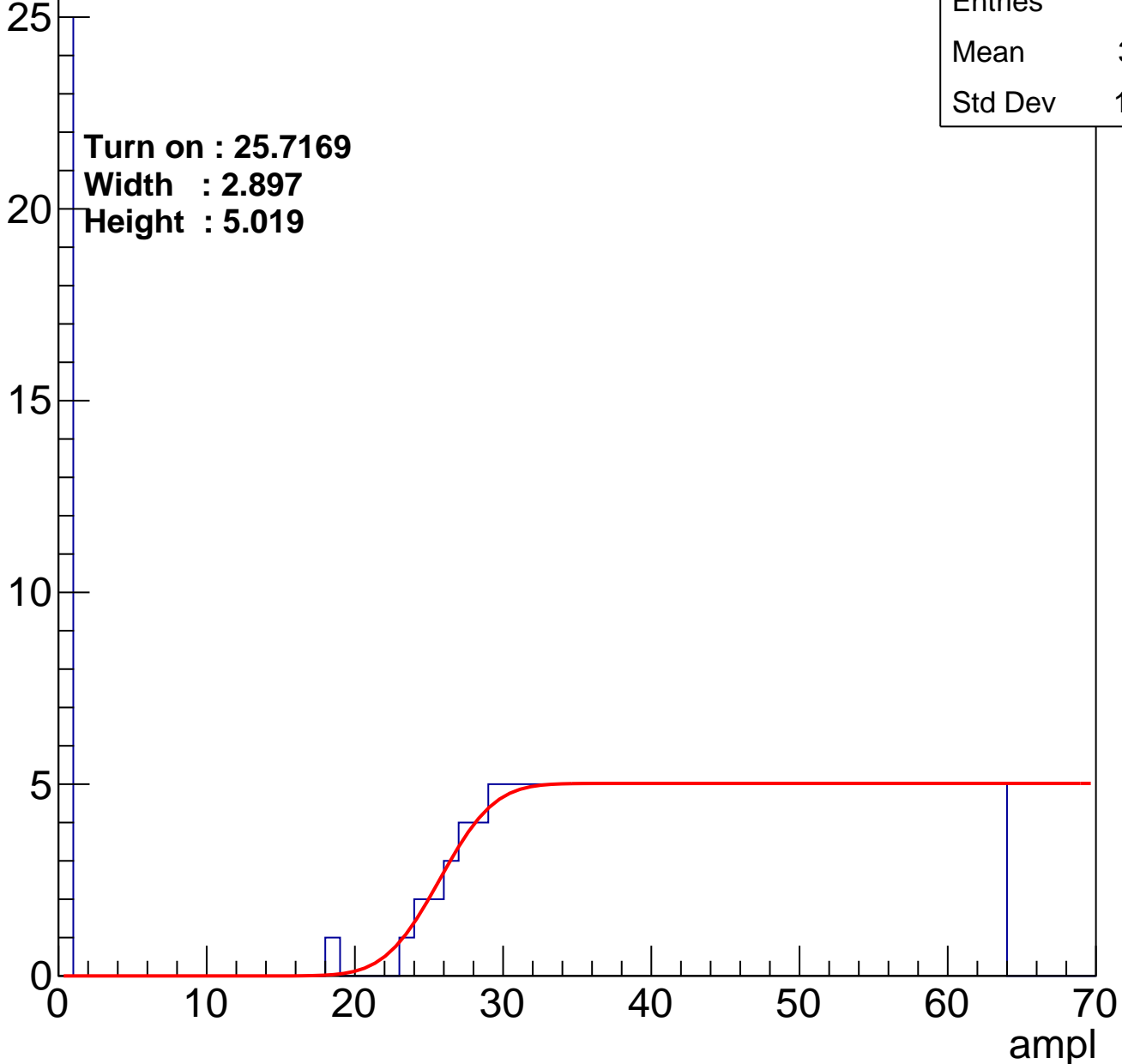
|         |       |
|---------|-------|
| Entries | 217   |
| Mean    | 39.11 |
| Std Dev | 17.64 |

Turn on : 25.7169

Width : 2.897

Height : 5.019

Entry





# B1L103S, U14-ch48

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 219   |
| Mean    | 38.84 |
| Std Dev | 17.81 |

**Turn on : 25.4524**

**Width : 4.458**

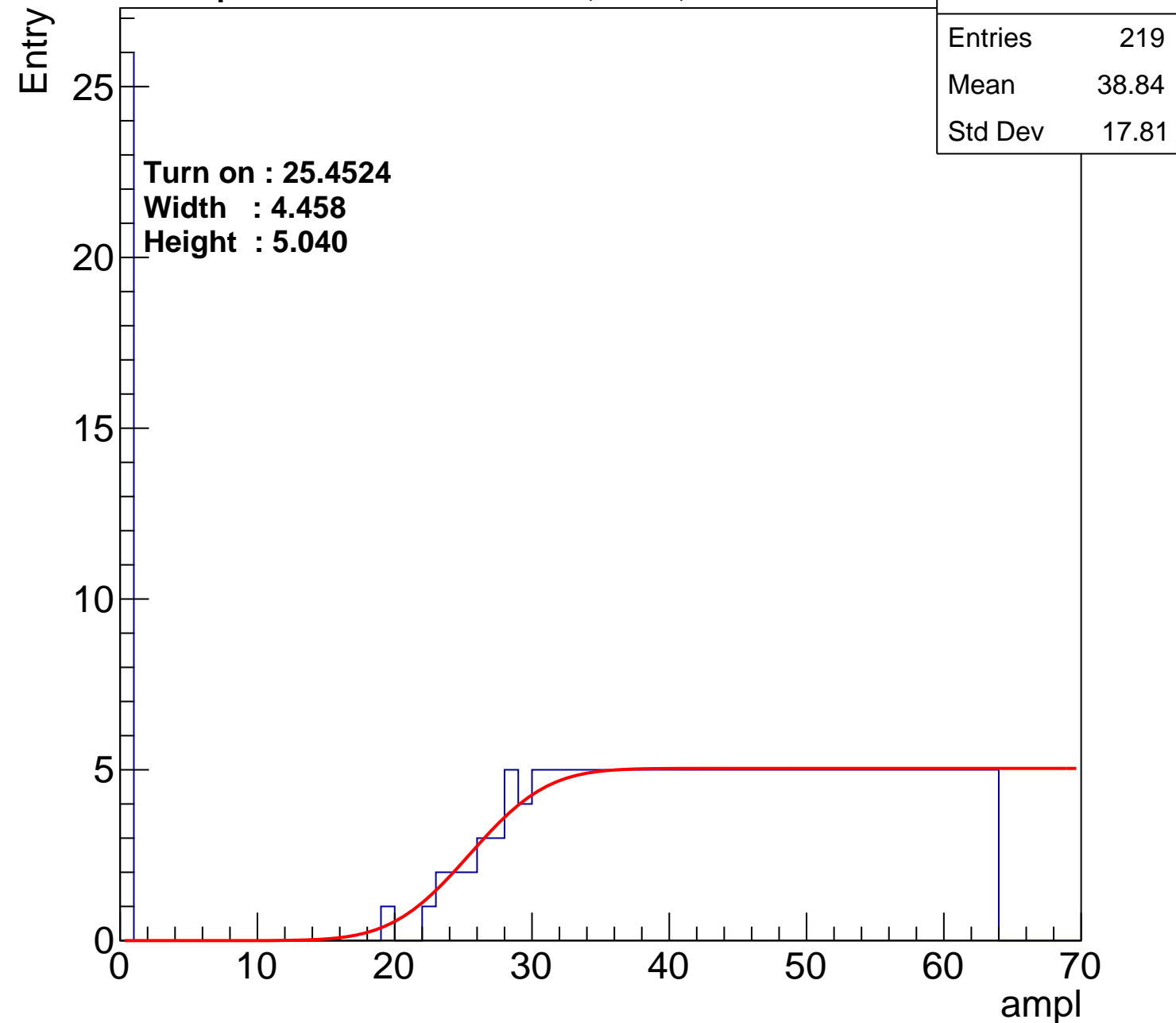
**Height : 5.040**

Entry

25  
20  
15  
10  
5  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U14-ch49

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 219   |
| Mean    | 38.74 |
| Std Dev | 17.95 |

**Turn on : 25.7022**

**Width : 3.256**

**Height : 5.006**

Entry

25

20

15

10

5

0

0

10

20

30

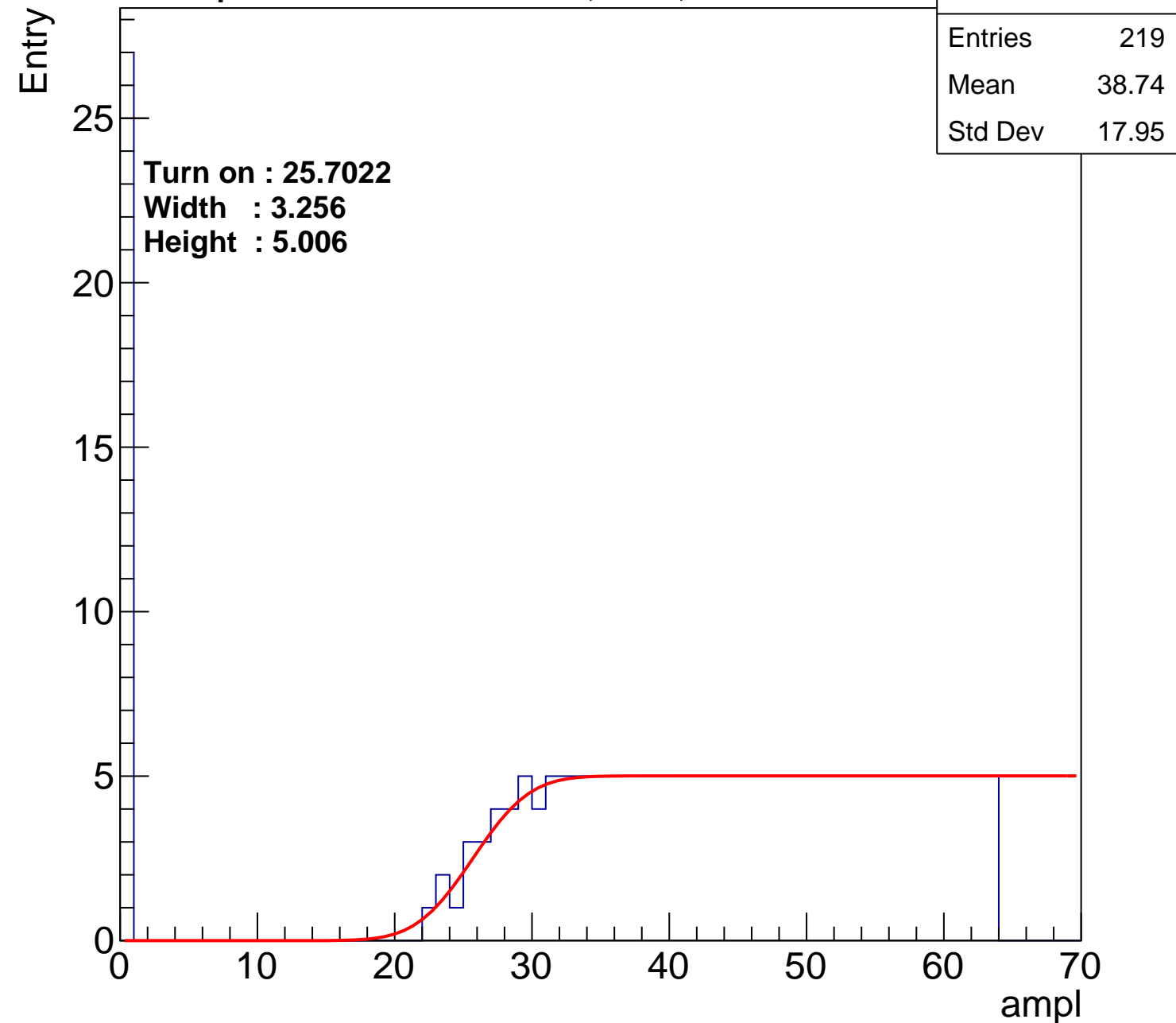
40

50

60

70

ampl



# B1L103S, U14-ch50

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 214   |
| Mean    | 39.14 |
| Std Dev | 17.89 |

**Turn on : 26.7423**

**Width : 4.705**

**Height : 5.048**

Entry

25

20

15

10

5

0

ampl

0

10

20

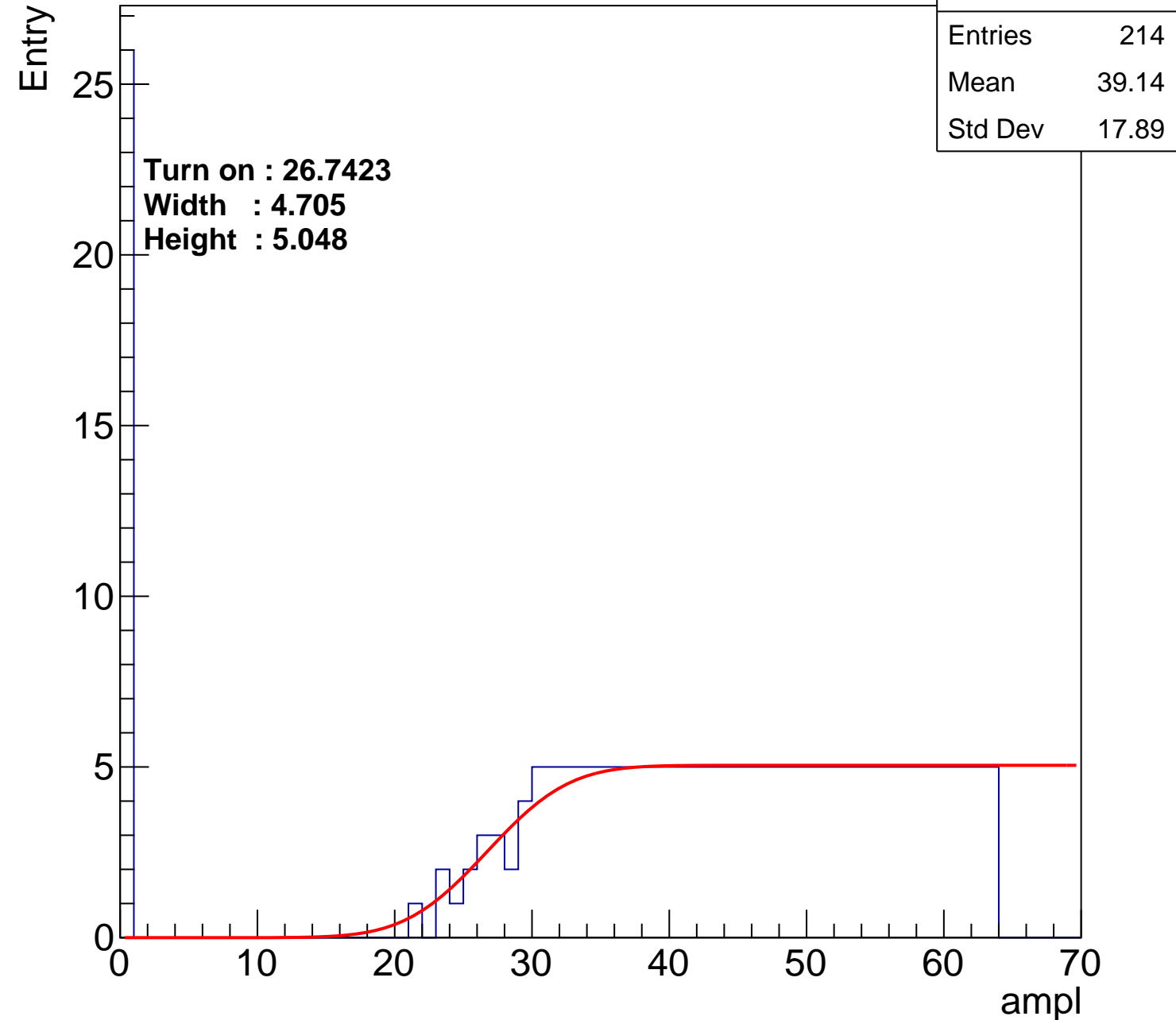
30

40

50

60

70



# B1L103S, U14-ch51

calib\_packv5\_041523\_1651.root, FC#0, Port C2

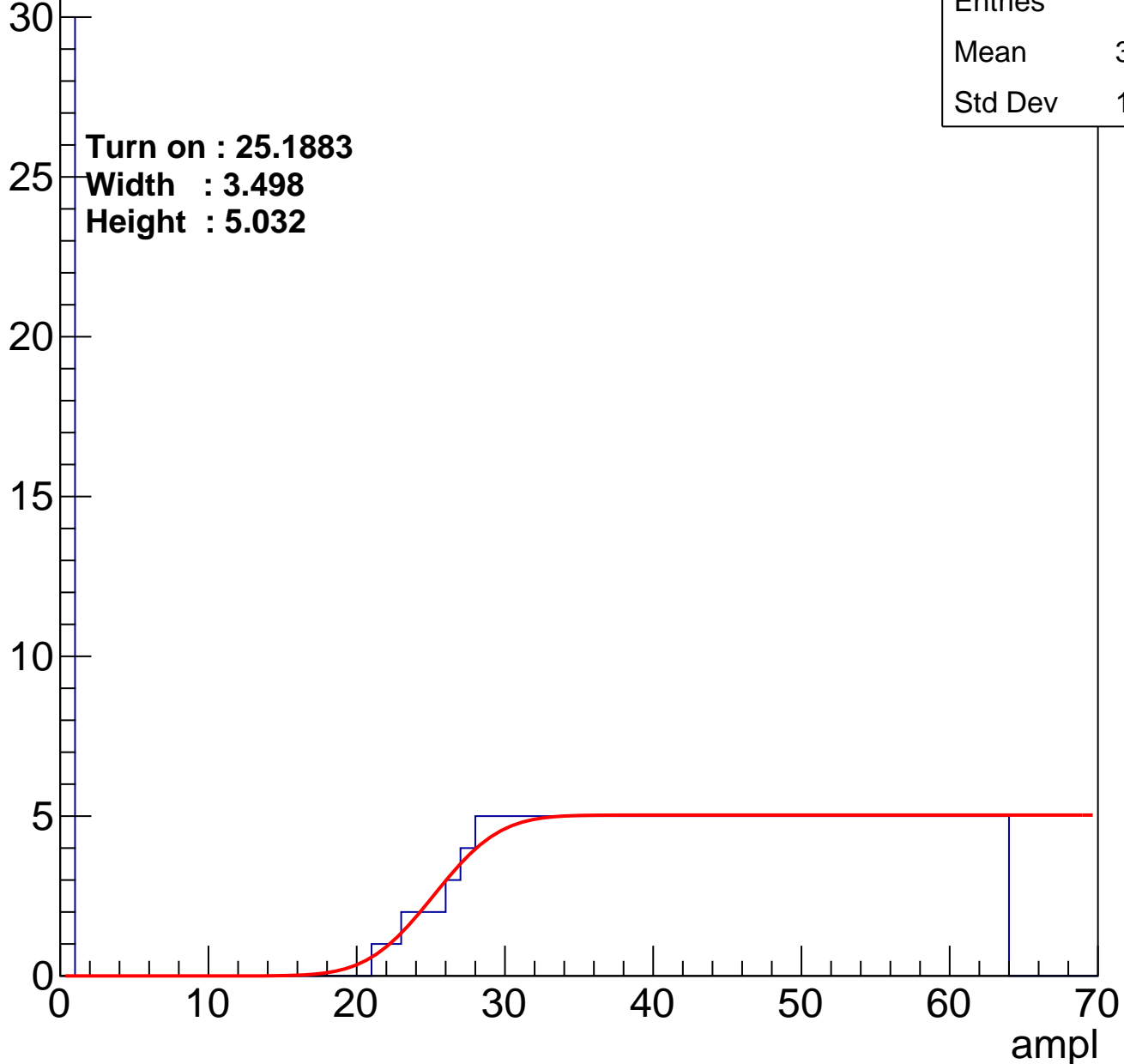
|         |       |
|---------|-------|
| Entries | 225   |
| Mean    | 38.06 |
| Std Dev | 18.32 |

**Turn on : 25.1883**

**Width : 3.498**

**Height : 5.032**

Entry

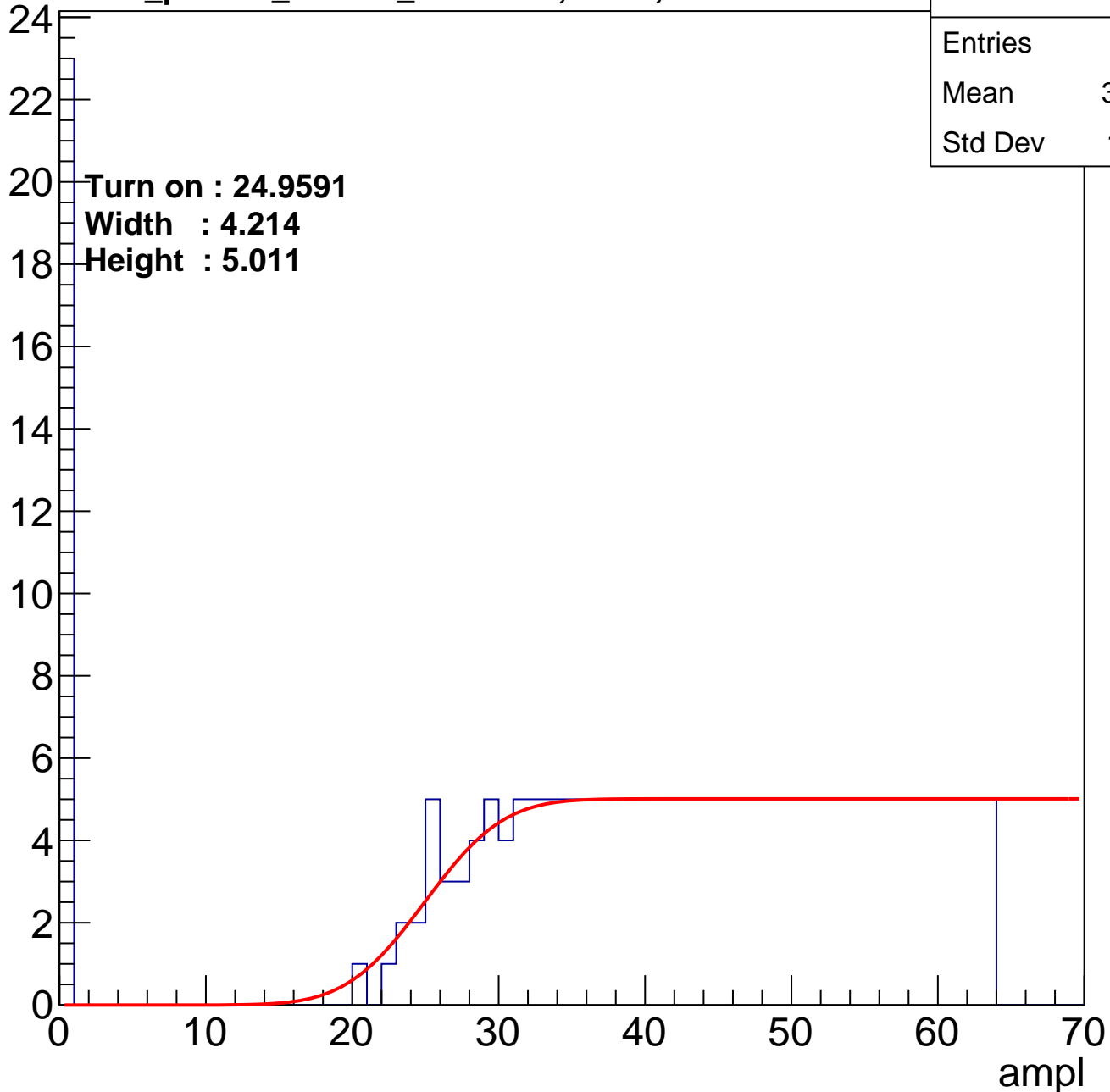


# B1L103S, U14-ch52

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 218   |
| Mean    | 39.23 |
| Std Dev | 17.31 |

Entry



# B1L103S, U14-ch53

calib\_packv5\_041523\_1651.root, FC#0, Port C2

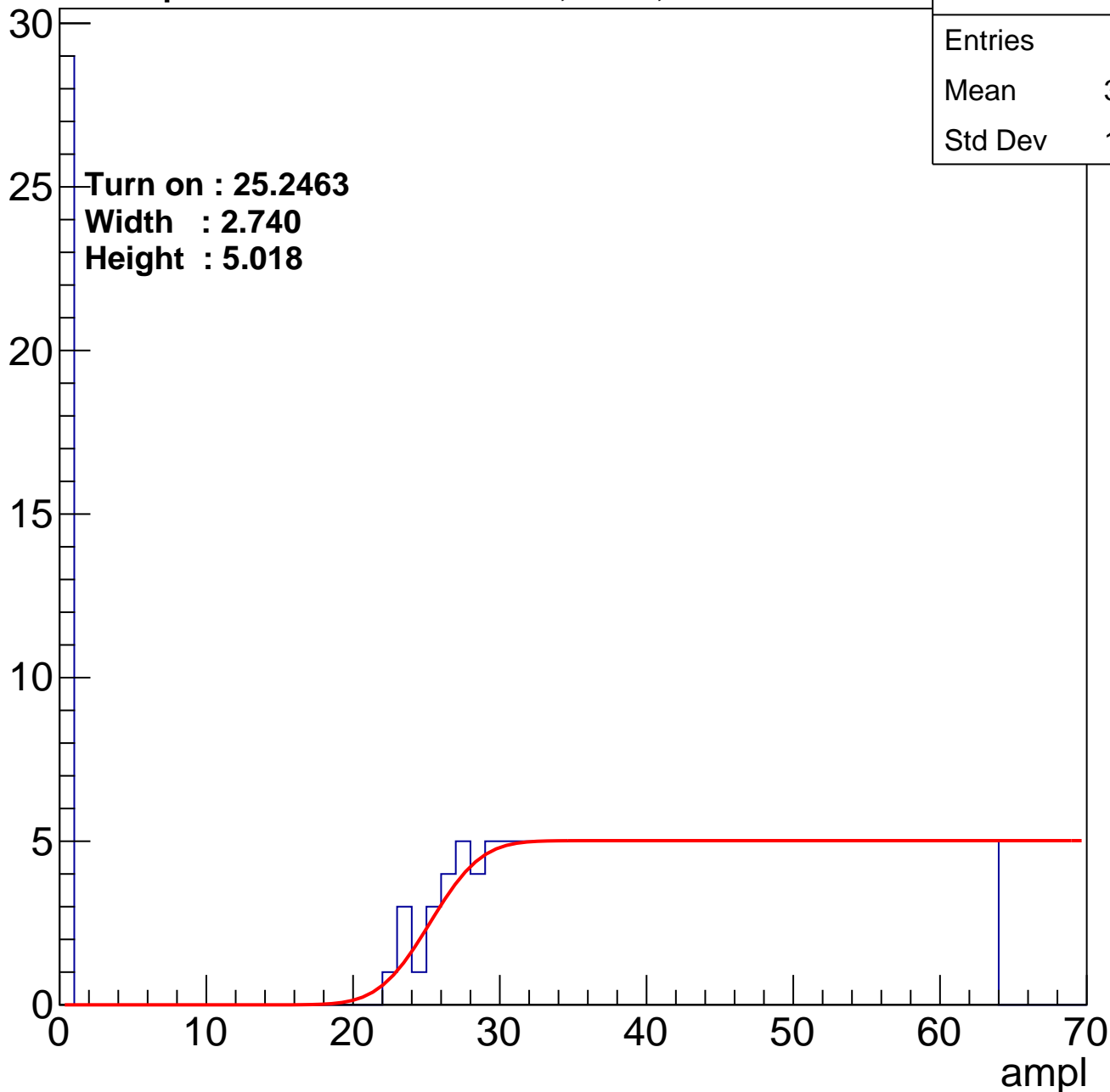
|         |       |
|---------|-------|
| Entries | 225   |
| Mean    | 38.18 |
| Std Dev | 18.15 |

Turn on : 25.2463

Width : 2.740

Height : 5.018

Entry



# B1L103S, U14-ch54

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 217   |
| Mean    | 38.82 |
| Std Dev | 18.03 |

**Turn on : 26.6269**

**Width : 4.824**

**Height : 5.059**

Entry

25

20

15

10

5

0

0

10

20

30

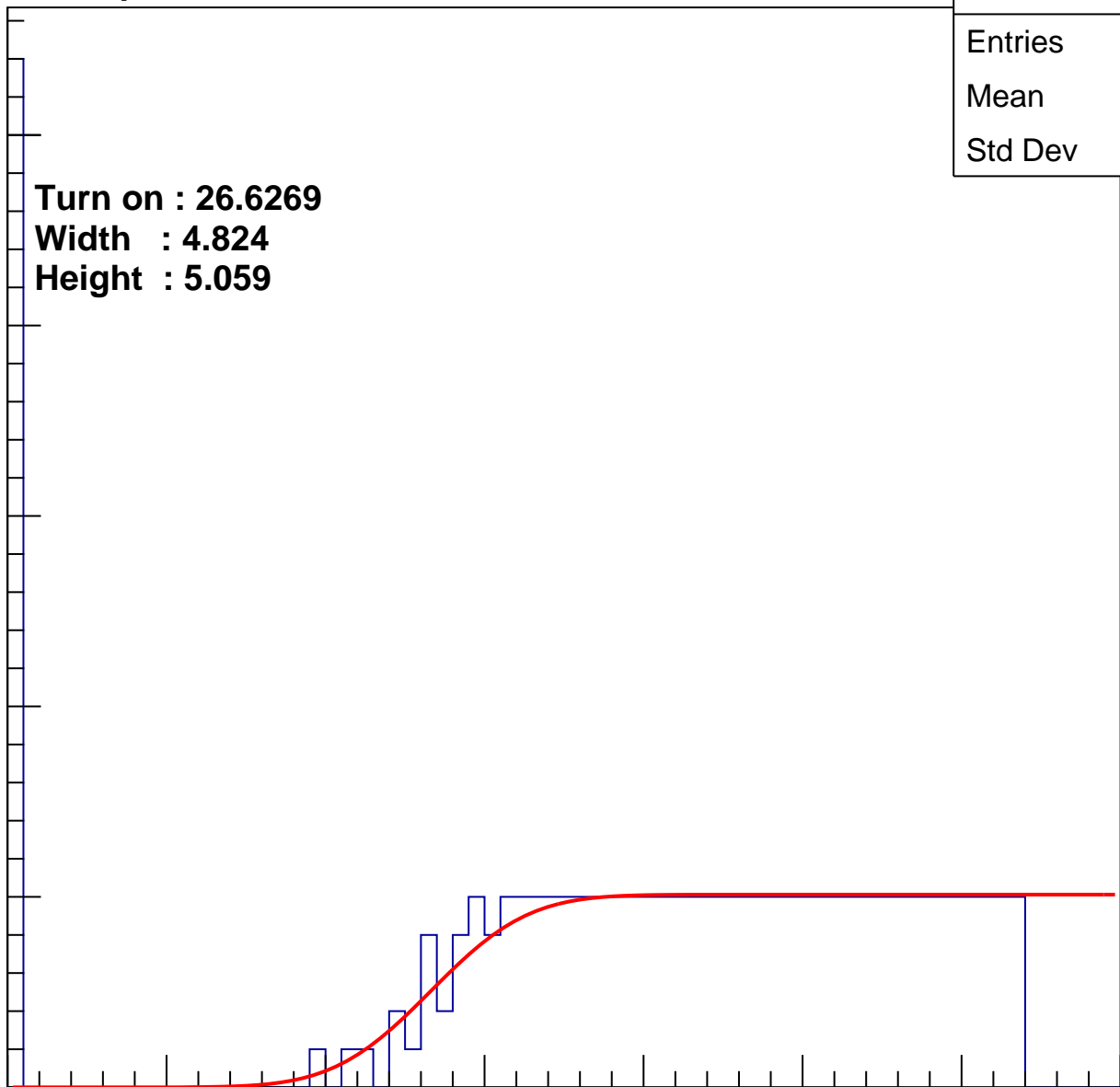
40

50

60

70

ampl

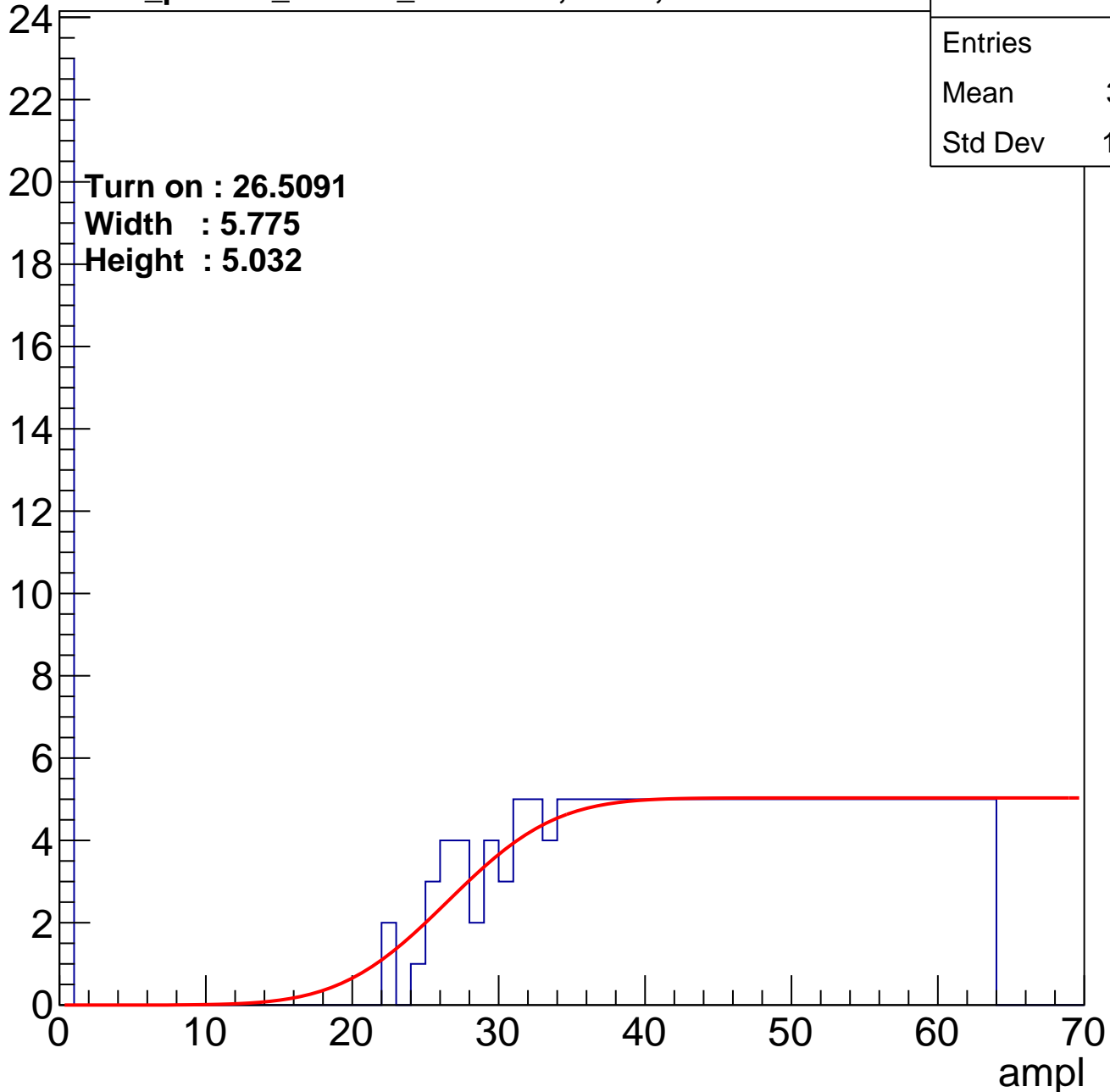


# B1L103S, U14-ch55

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 210   |
| Mean    | 39.71 |
| Std Dev | 17.44 |

Entry





# B1L103S, U14-ch56

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 227   |
| Mean    | 37.63 |
| Std Dev | 18.72 |

**Turn on : 25.0341**

**Width : 2.983**

**Height : 5.024**

Entry

30

25

20

15

10

5

0

0

10

20

30

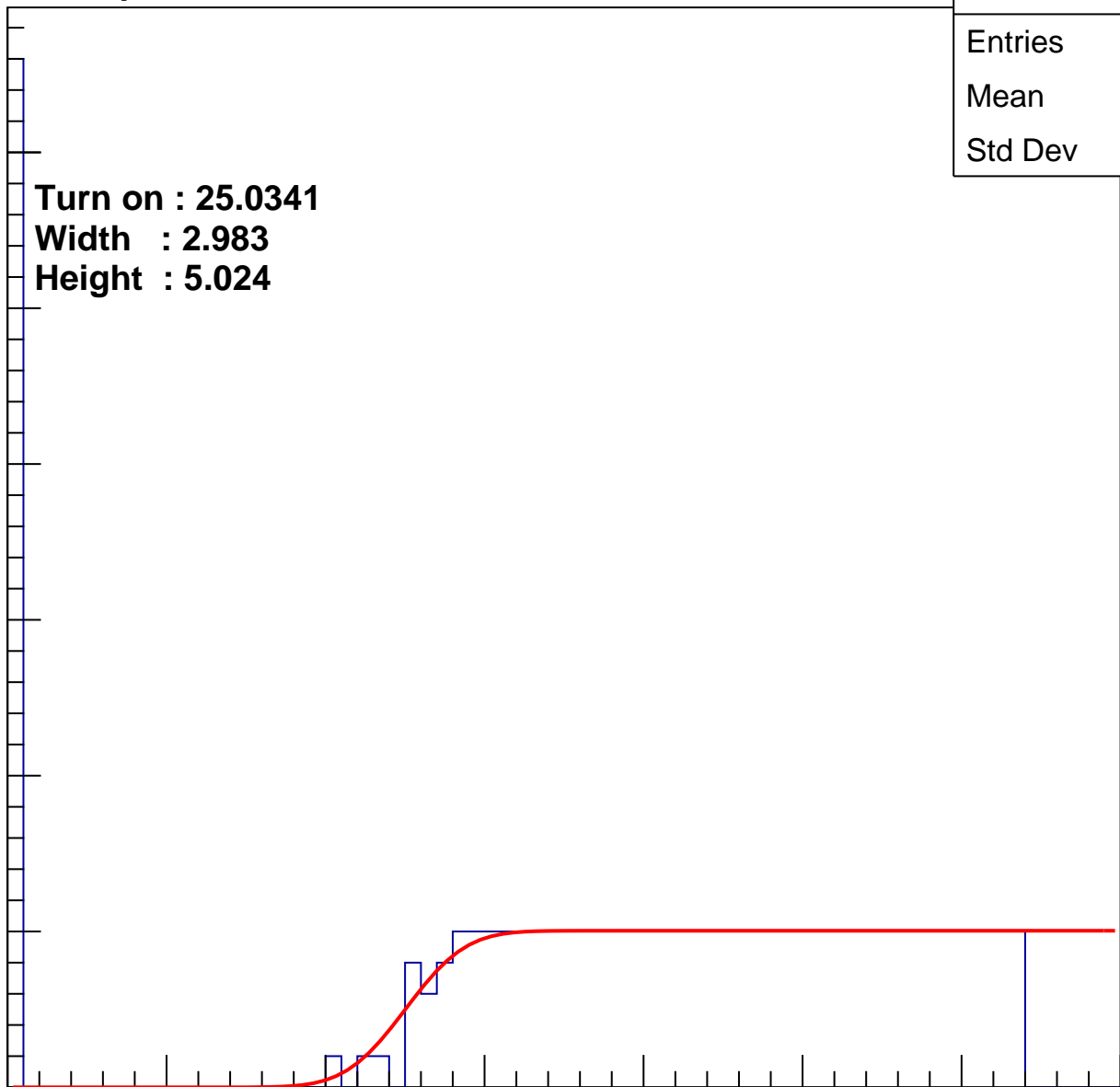
40

50

60

70

ampl

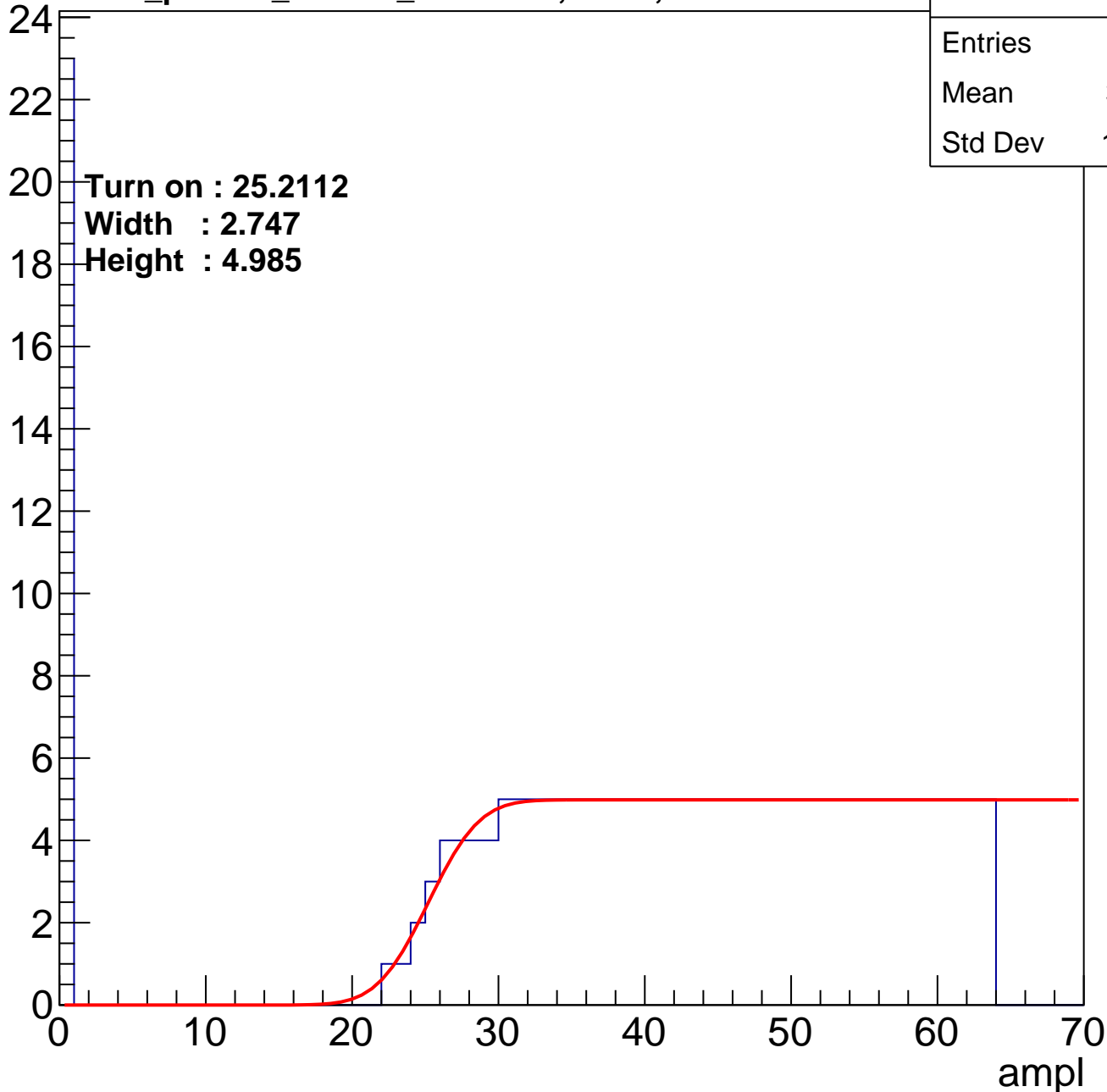


# B1L103S, U14-ch57

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 216   |
| Mean    | 39.41 |
| Std Dev | 17.29 |

Entry



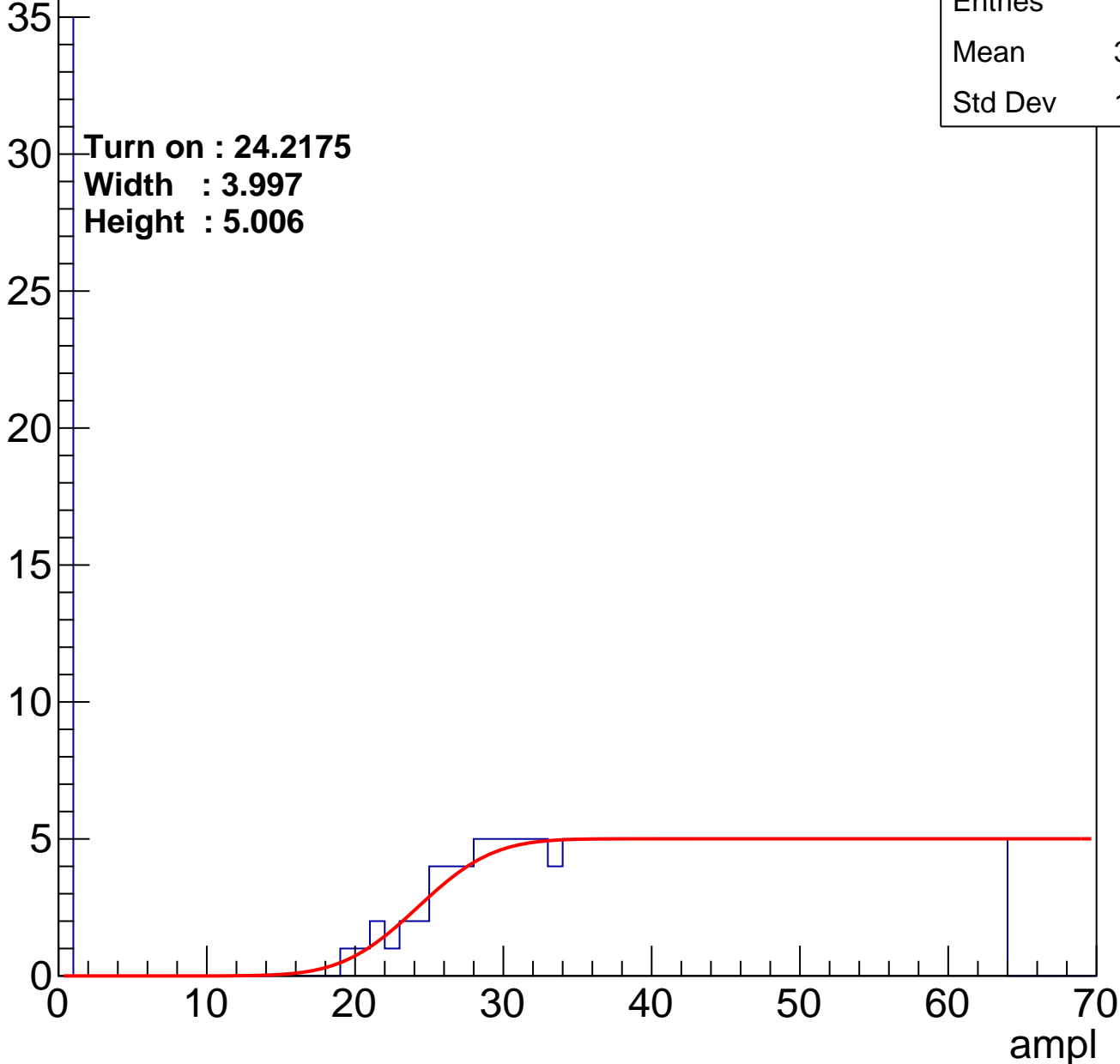
# B1L103S, U14-ch58

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 235   |
| Mean    | 36.88 |
| Std Dev | 18.89 |

Turn on : 24.2175  
Width : 3.997  
Height : 5.006

Entry



# B1L103S, U14-ch59

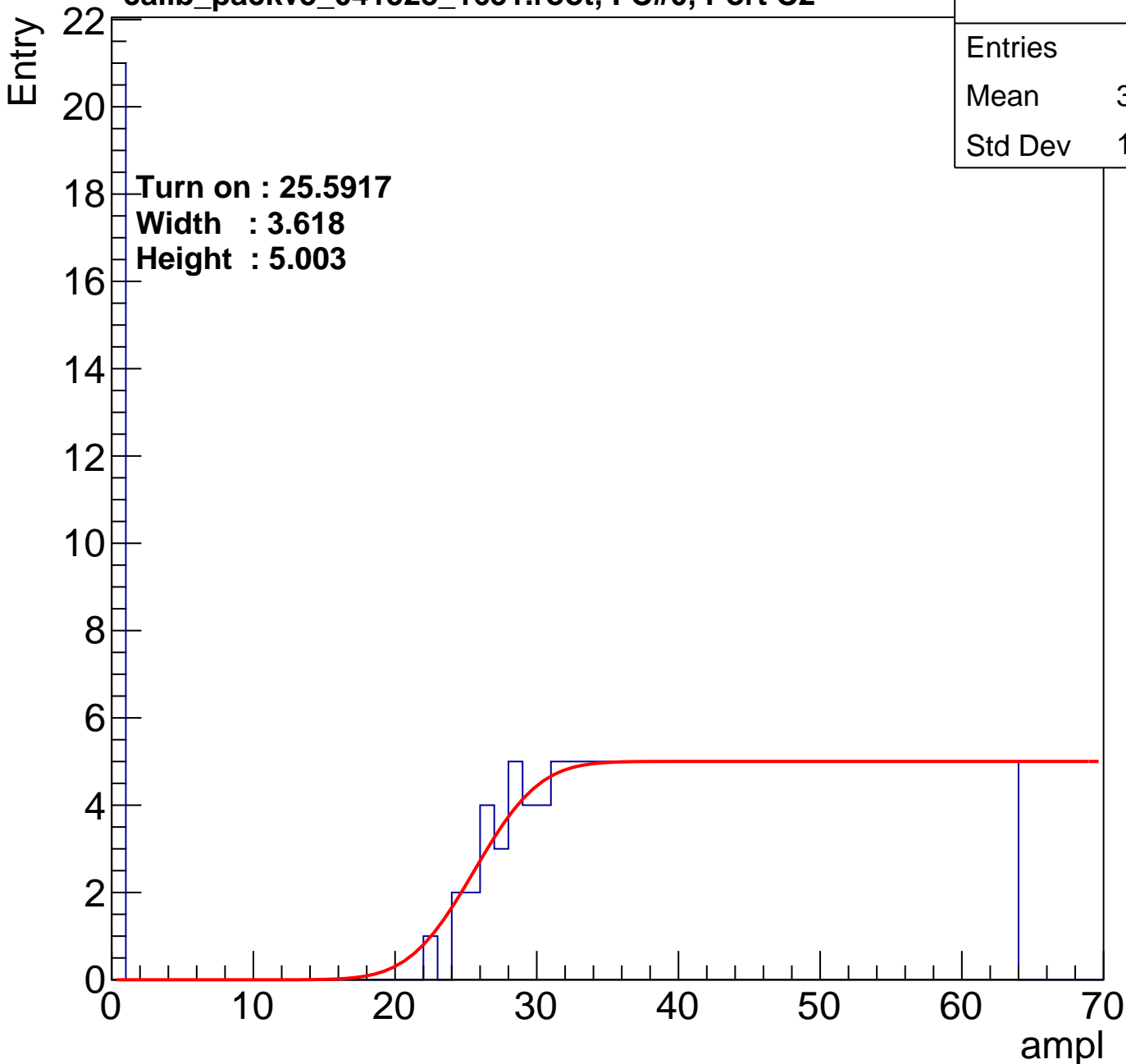
calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 211   |
| Mean    | 39.98 |
| Std Dev | 16.98 |

Turn on : 25.5917

Width : 3.618

Height : 5.003



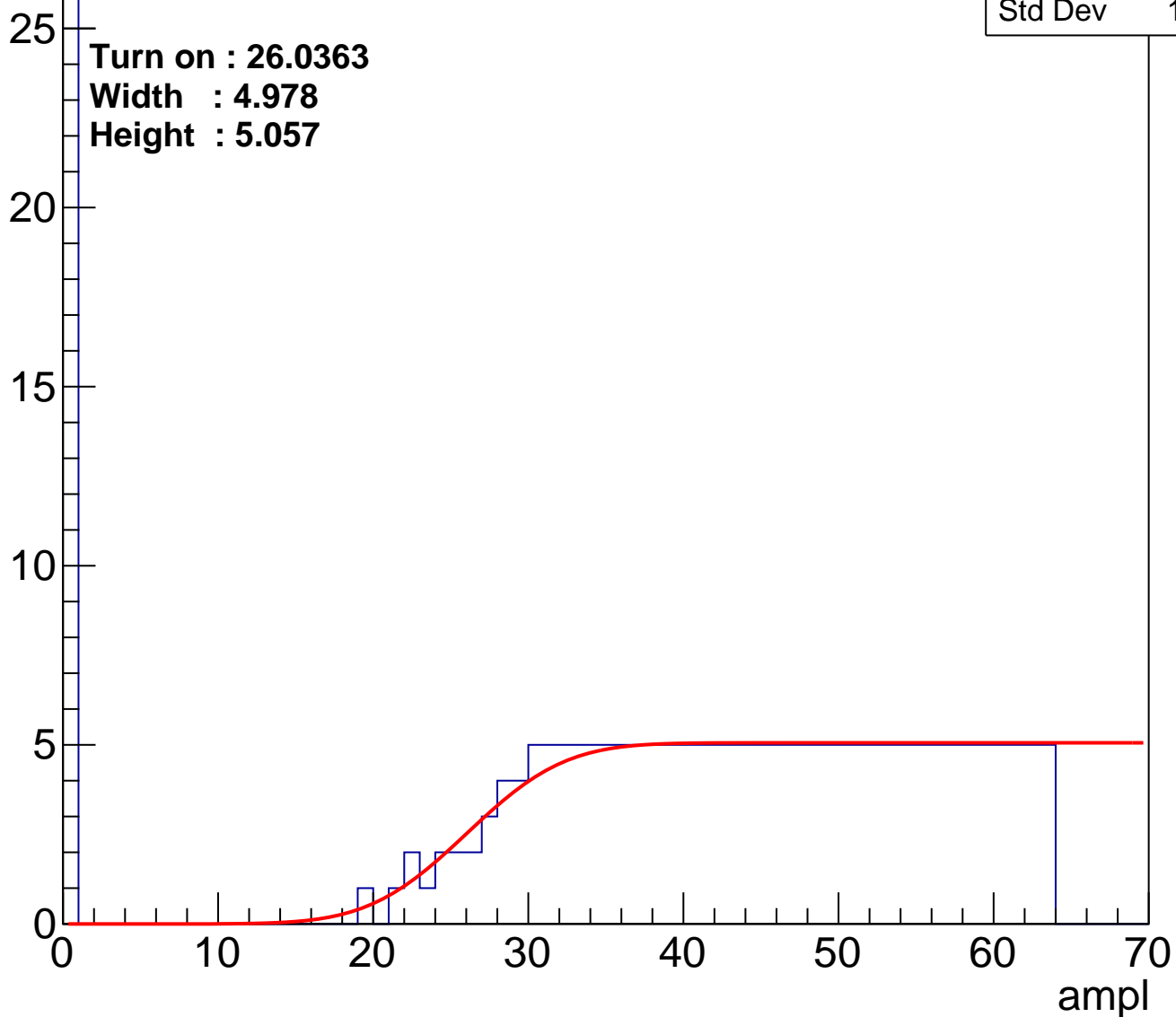
# B1L103S, U14-ch60

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 220   |
| Mean    | 38.5  |
| Std Dev | 18.16 |

**Turn on : 26.0363**  
**Width : 4.978**  
**Height : 5.057**

Entry



# B1L103S, U14-ch61

calib\_packv5\_041523\_1651.root, FC#0, Port C2

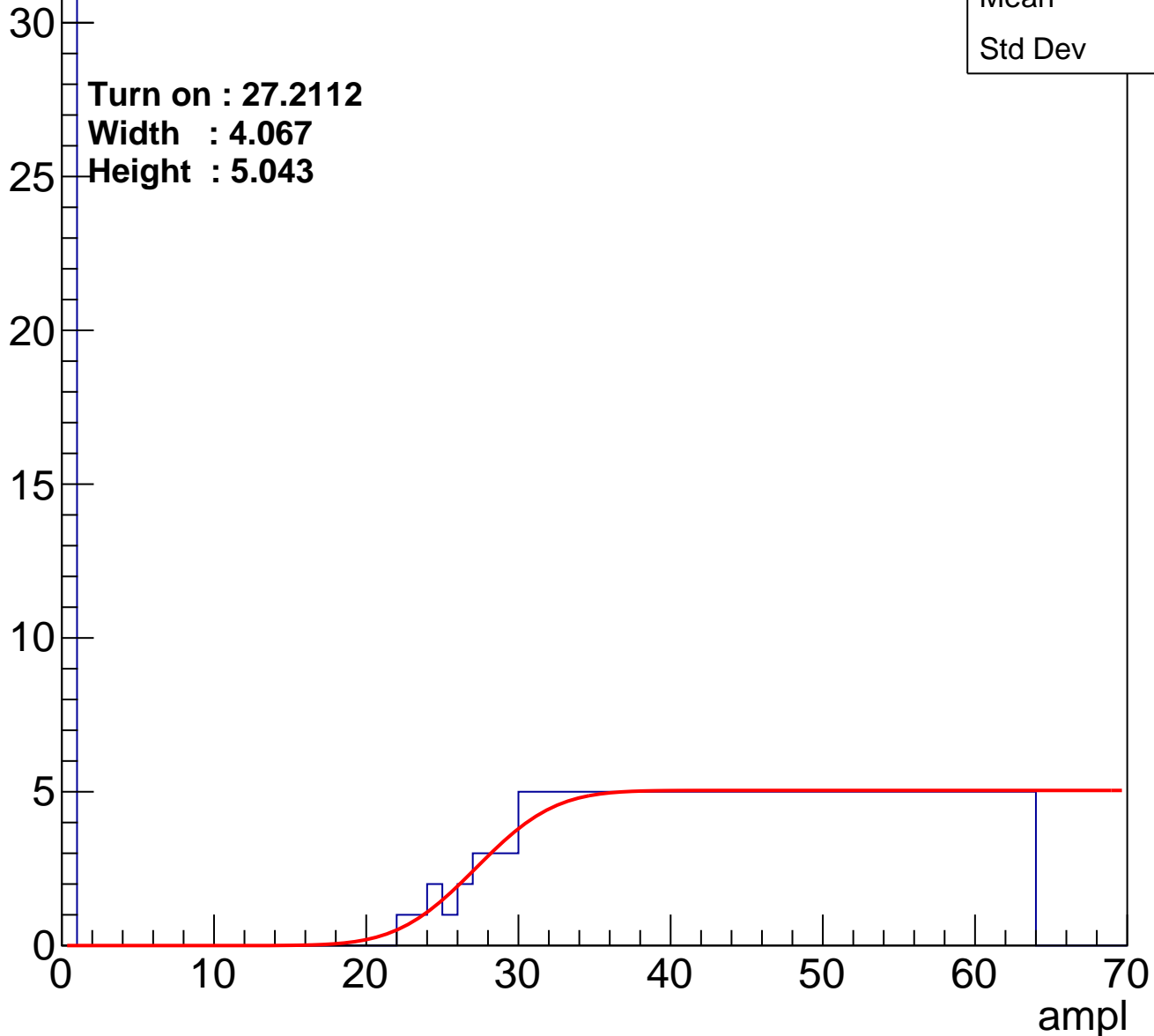
|         |      |
|---------|------|
| Entries | 218  |
| Mean    | 38.2 |
| Std Dev | 18.8 |

Turn on : 27.2112

Width : 4.067

Height : 5.043

Entry



# B1L103S, U14-ch62

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 218   |
| Mean    | 38.9  |
| Std Dev | 17.82 |

**Turn on : 25.9028**

**Width : 3.888**

**Height : 5.036**

Entry

25

20

15

10

5

0

0

10

20

30

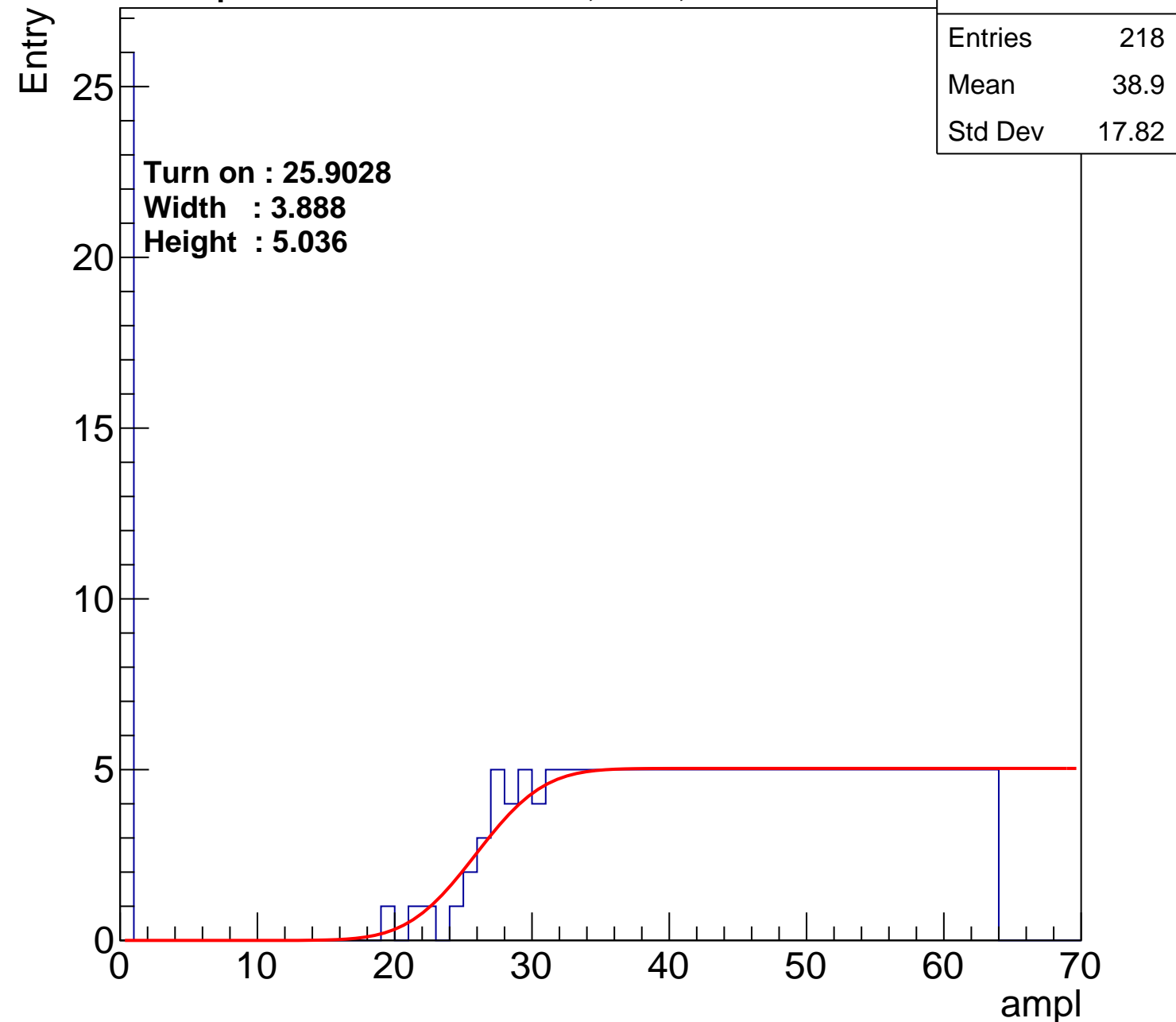
40

50

60

ampl

70



# B1L103S, U14-ch63

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 229   |
| Mean    | 37.44 |
| Std Dev | 18.73 |

**Turn on : 24.5286**

**Width : 5.195**

**Height : 5.034**

Entry

30

25

20

15

10

5

0

0

10

20

30

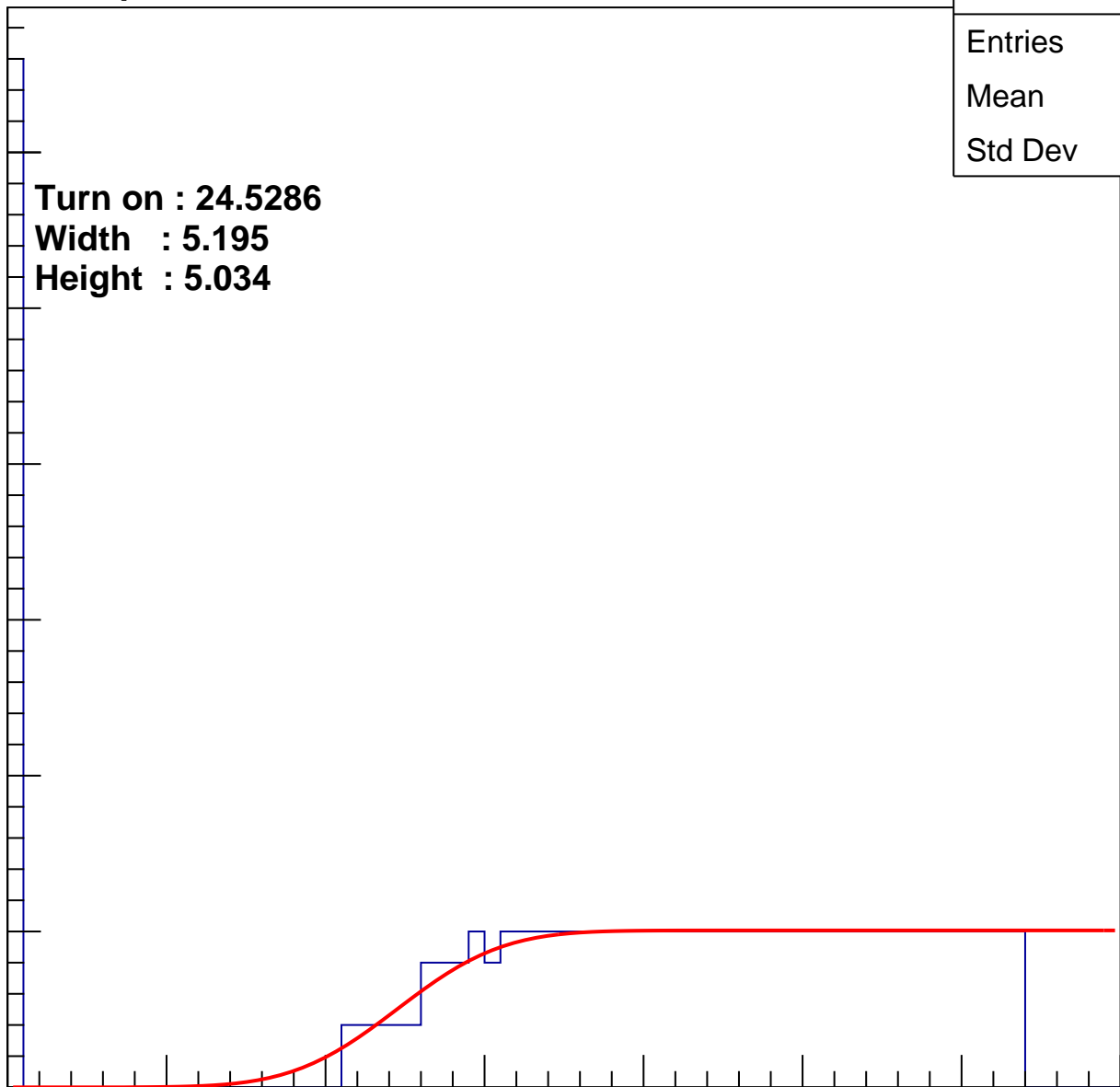
40

50

60

70

ampl





# B1L103S, U14-ch64

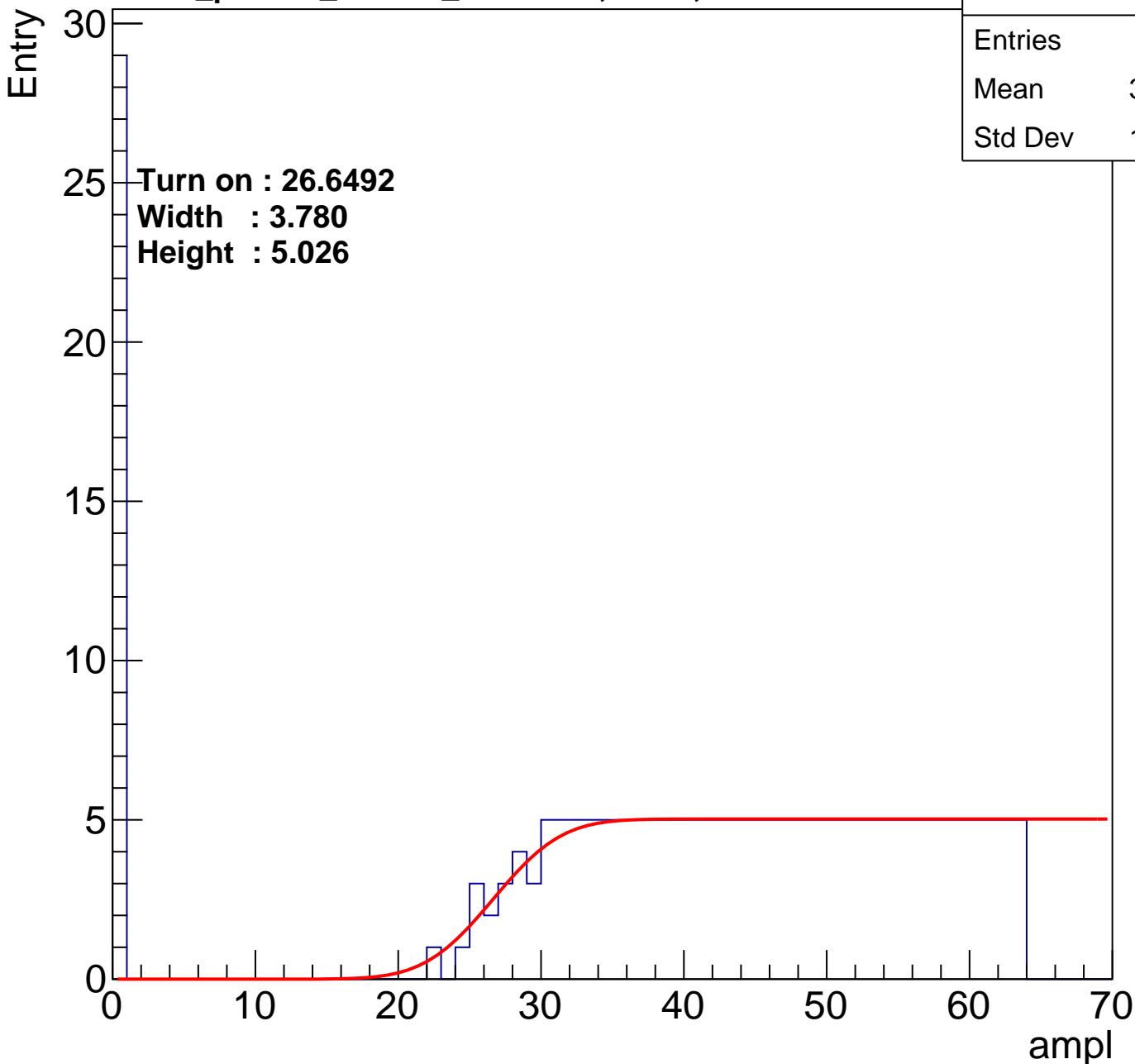
calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 216   |
| Mean    | 38.69 |
| Std Dev | 18.34 |

Turn on : 26.6492

Width : 3.780

Height : 5.026



# B1L103S, U14-ch65

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 227   |
| Mean    | 37.61 |
| Std Dev | 18.72 |

**Turn on : 24.1508**

**Width : 4.117**

**Height : 5.004**

Entry

30

25

20

15

10

5

0

ampl

0

10

20

30

40

50

60

70

# B1L103S, U14-ch66

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 226   |
| Mean    | 37.63 |
| Std Dev | 18.77 |

**Turn on : 25.3813**

**Width : 3.935**

**Height : 5.017**

Entry

30

25

20

15

10

5

0

0

10

20

30

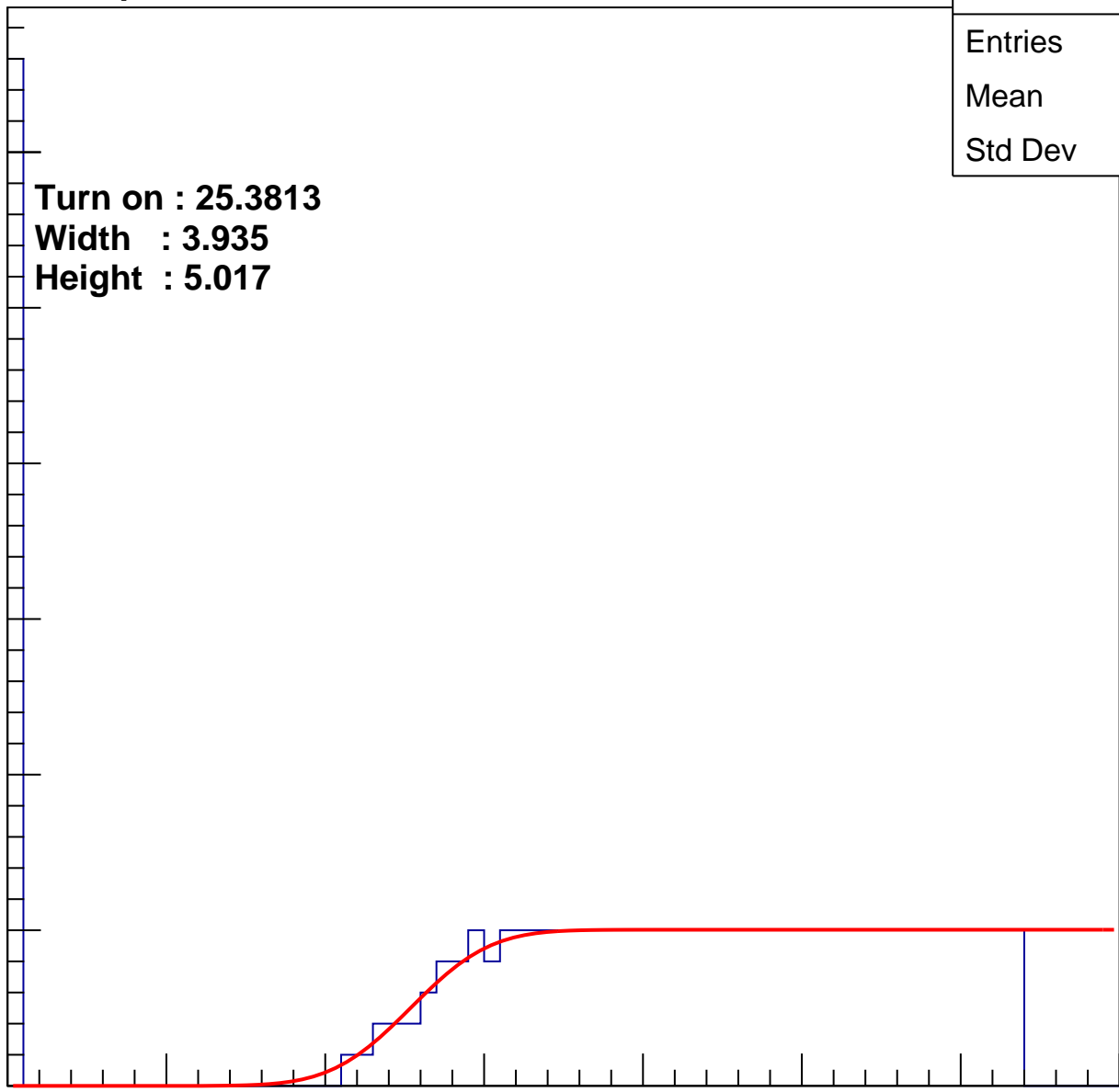
40

50

60

70

ampl



# B1L103S, U14-ch67

calib\_packv5\_041523\_1651.root, FC#0, Port C2

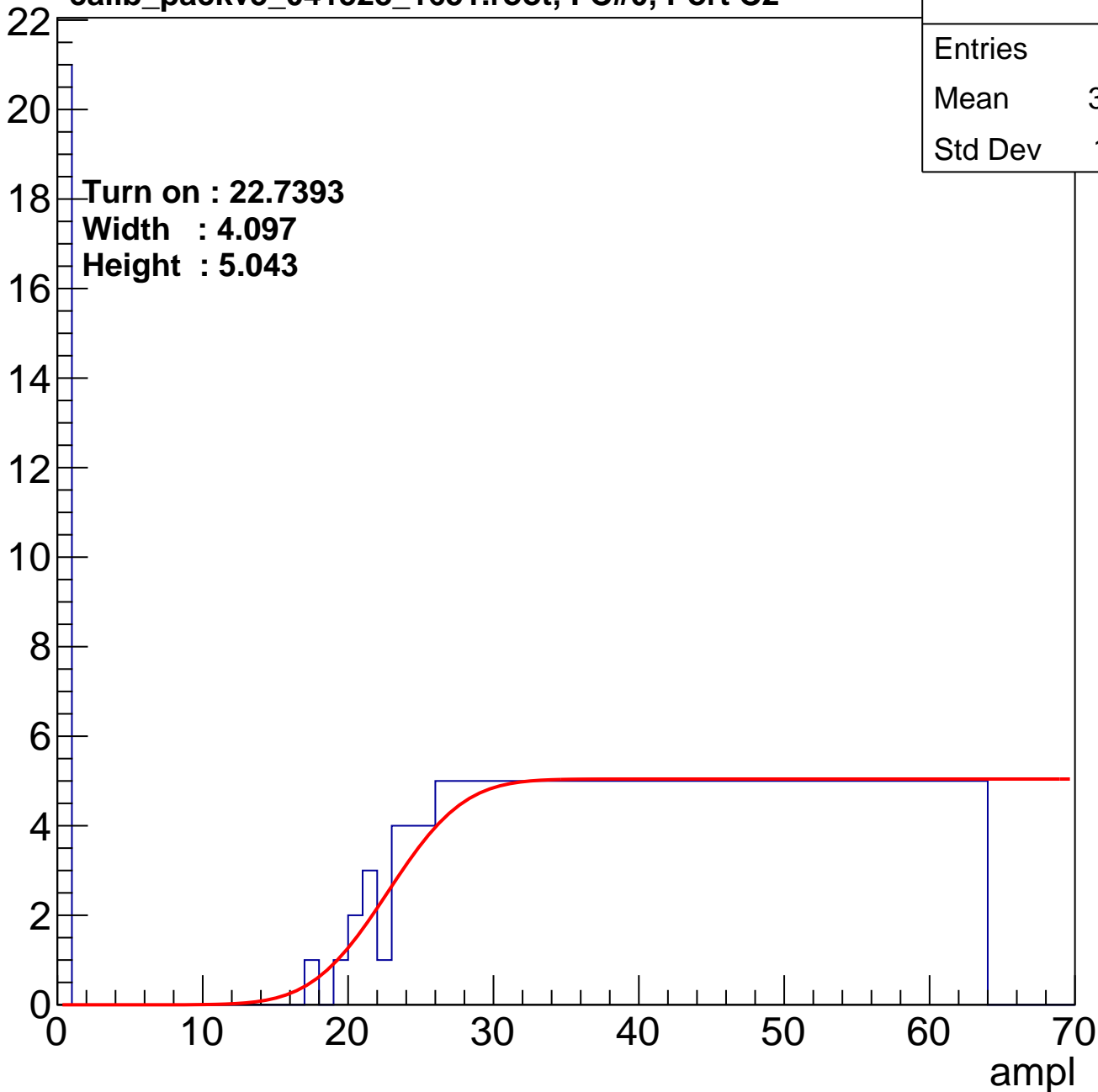
|         |       |
|---------|-------|
| Entries | 231   |
| Mean    | 38.55 |
| Std Dev | 16.91 |

Turn on : 22.7393

Width : 4.097

Height : 5.043

Entry



# B1L103S, U14-ch68

calib\_packv5\_041523\_1651.root, FC#0, Port C2

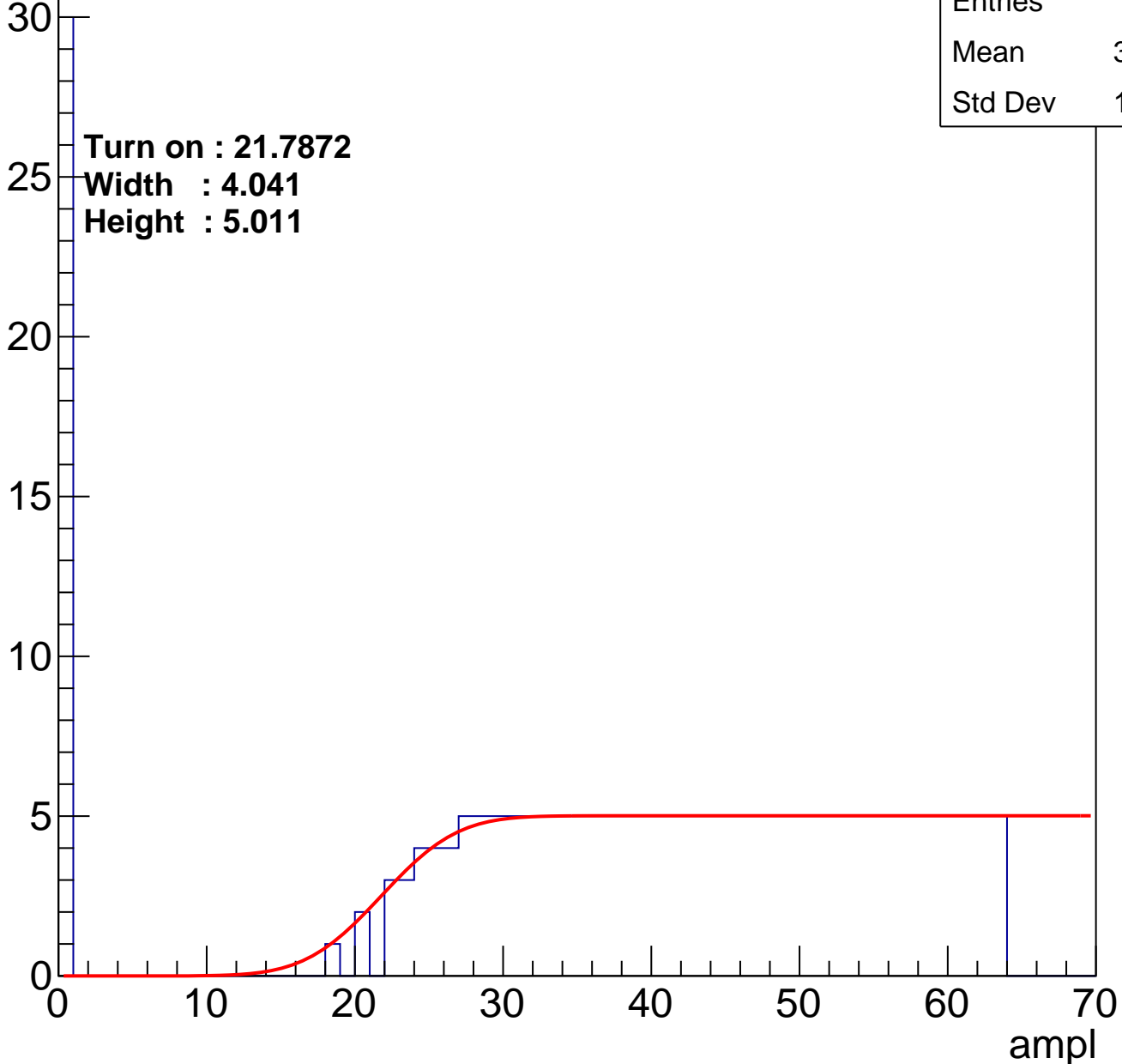
|         |       |
|---------|-------|
| Entries | 236   |
| Mean    | 37.36 |
| Std Dev | 18.17 |

**Turn on : 21.7872**

**Width : 4.041**

**Height : 5.011**

Entry



# B1L103S, U14-ch69

calib\_packv5\_041523\_1651.root, FC#0, Port C2

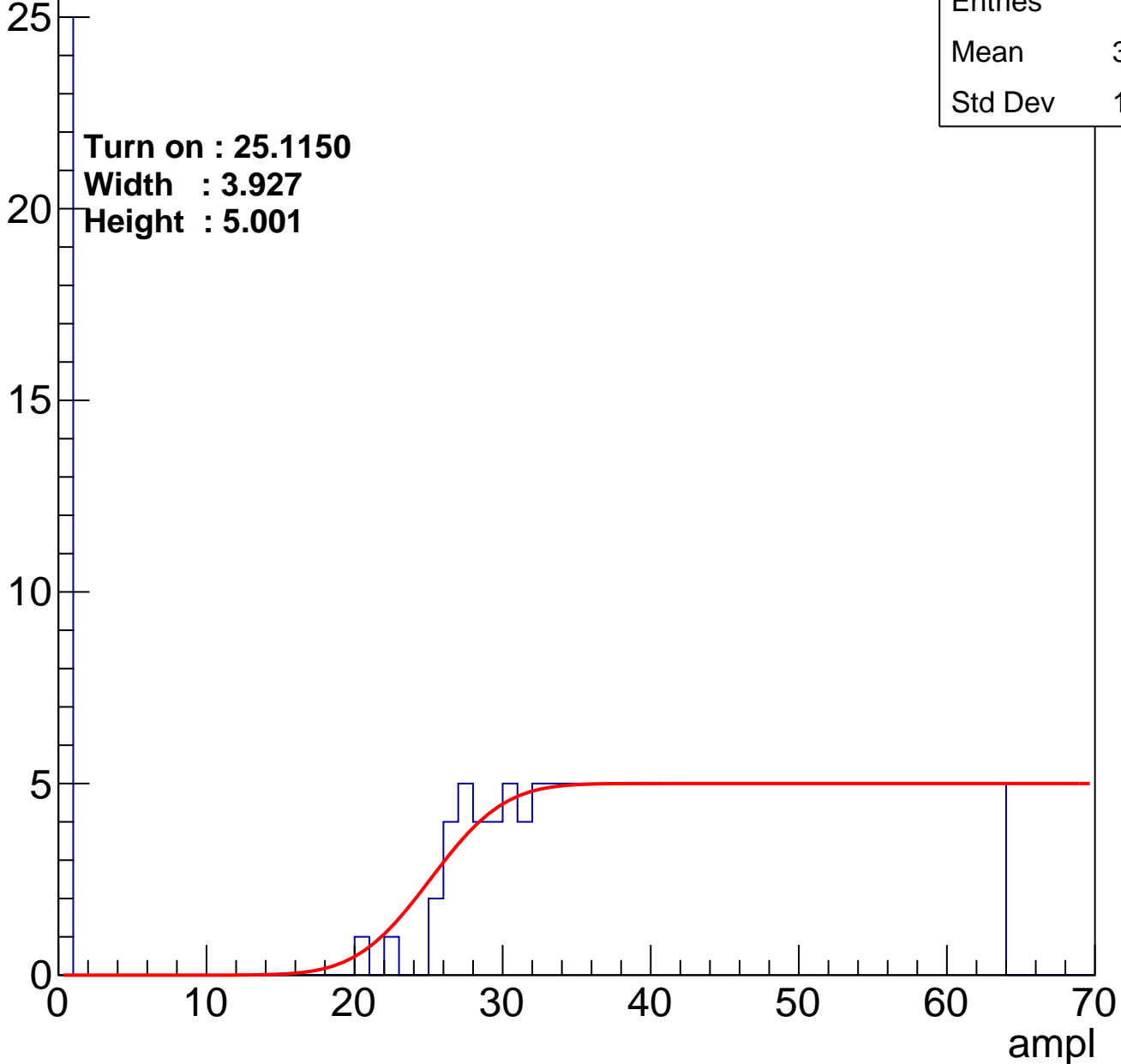
|         |       |
|---------|-------|
| Entries | 215   |
| Mean    | 39.22 |
| Std Dev | 17.68 |

Turn on : 25.1150

Width : 3.927

Height : 5.001

Entry



# B1L103S, U14-ch70

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 226   |
| Mean    | 38.4  |
| Std Dev | 17.71 |

**Turn on : 24.1367**

**Width : 3.130**

**Height : 5.020**

Entry

25

20

15

10

5

0

0

10

20

30

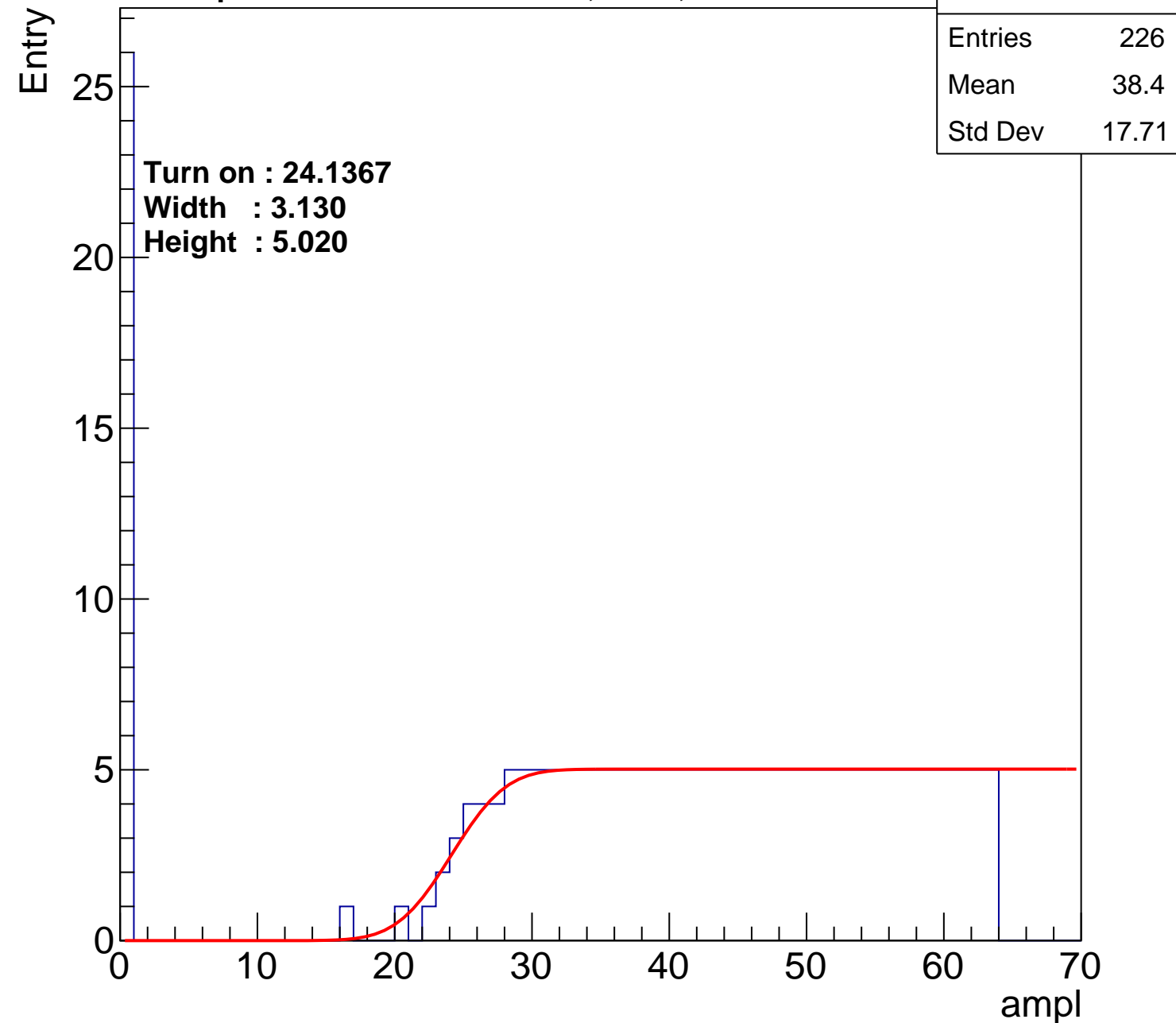
40

50

60

70

ampl



# B1L103S, U14-ch71

calib\_packv5\_041523\_1651.root, FC#0, Port C2

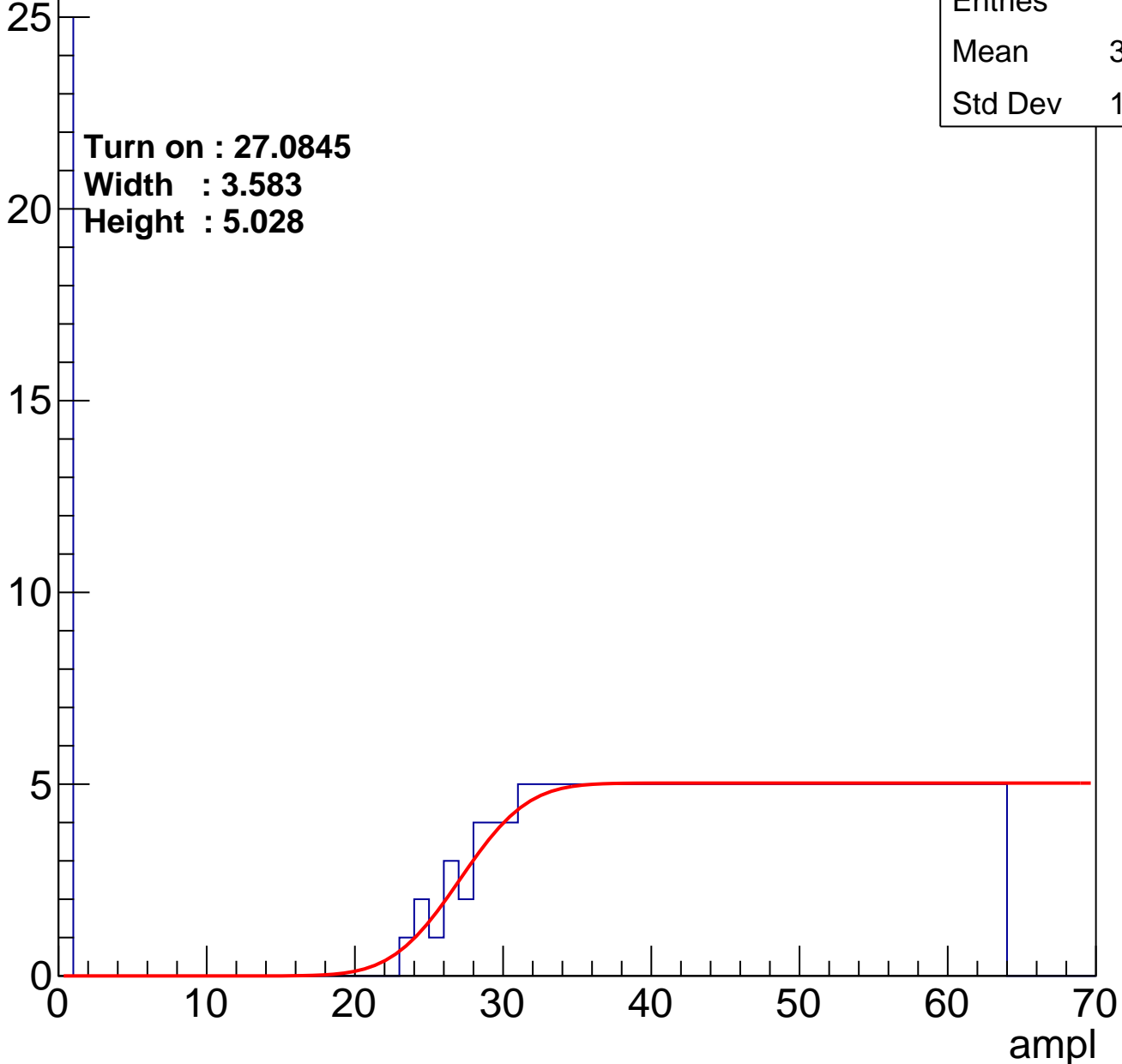
|         |       |
|---------|-------|
| Entries | 211   |
| Mean    | 39.48 |
| Std Dev | 17.74 |

**Turn on : 27.0845**

**Width : 3.583**

**Height : 5.028**

Entry



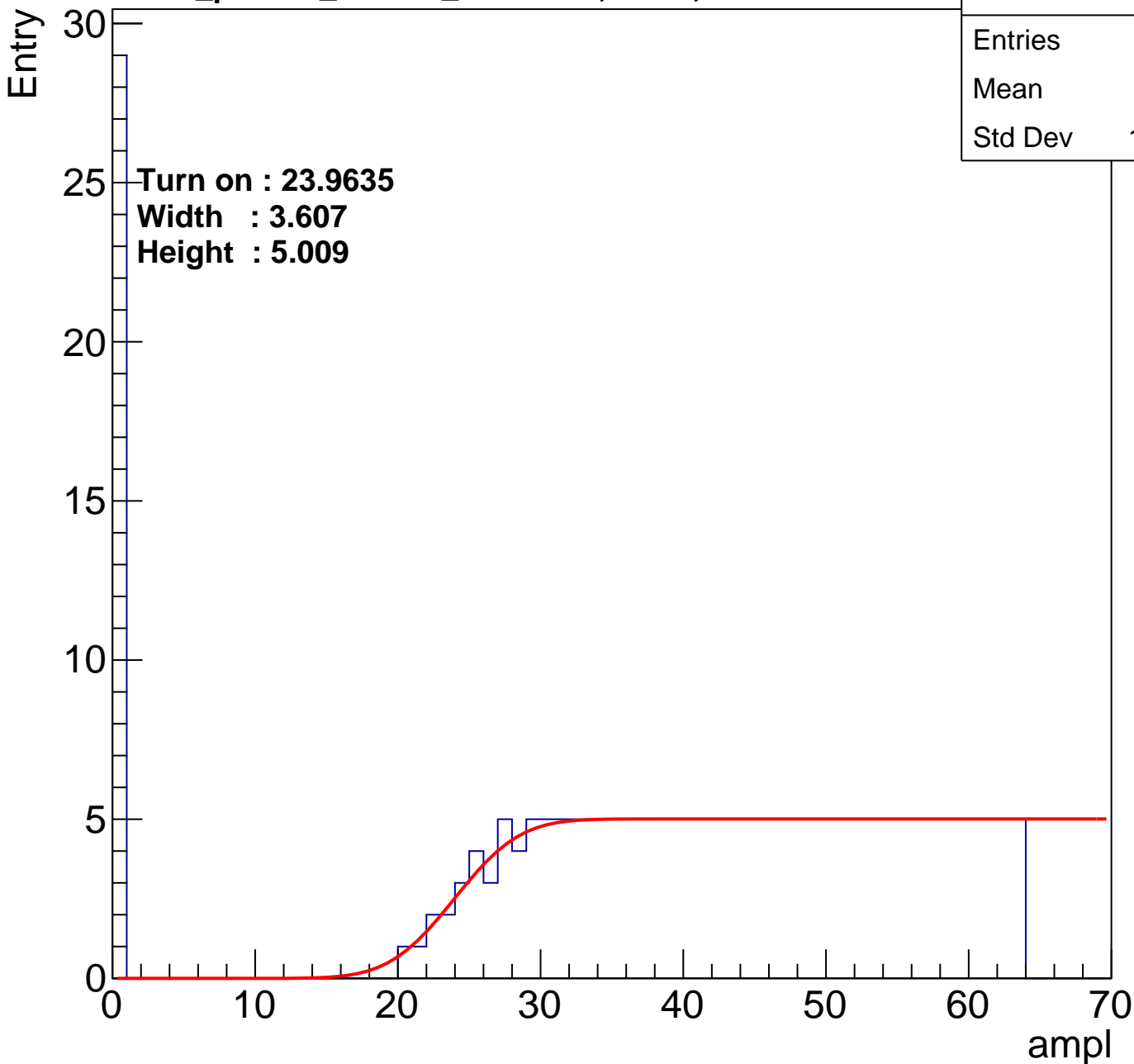


# B1L103S, U14-ch72

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 229   |
| Mean    | 37.9  |
| Std Dev | 18.12 |

Turn on : 23.9635  
Width : 3.607  
Height : 5.009



# B1L103S, U14-ch73

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 223   |
| Mean    | 38.49 |
| Std Dev | 17.9  |

**Turn on : 25.2121**

**Width : 3.416**

**Height : 5.037**

Entry

25

20

15

10

5

0

0

10

20

30

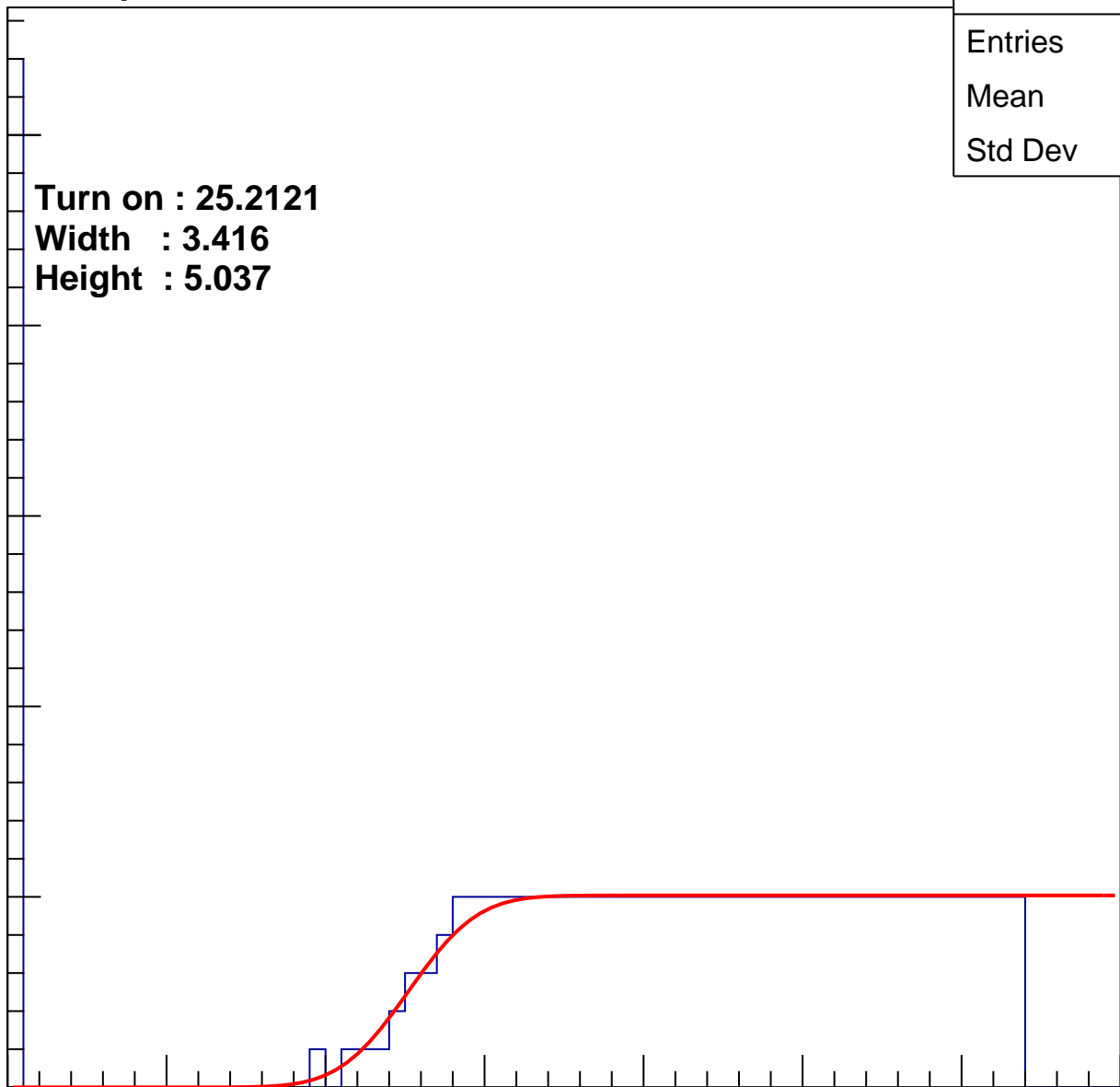
40

50

60

70

ampl



# B1L103S, U14-ch74

calib\_packv5\_041523\_1651.root, FC#0, Port C2

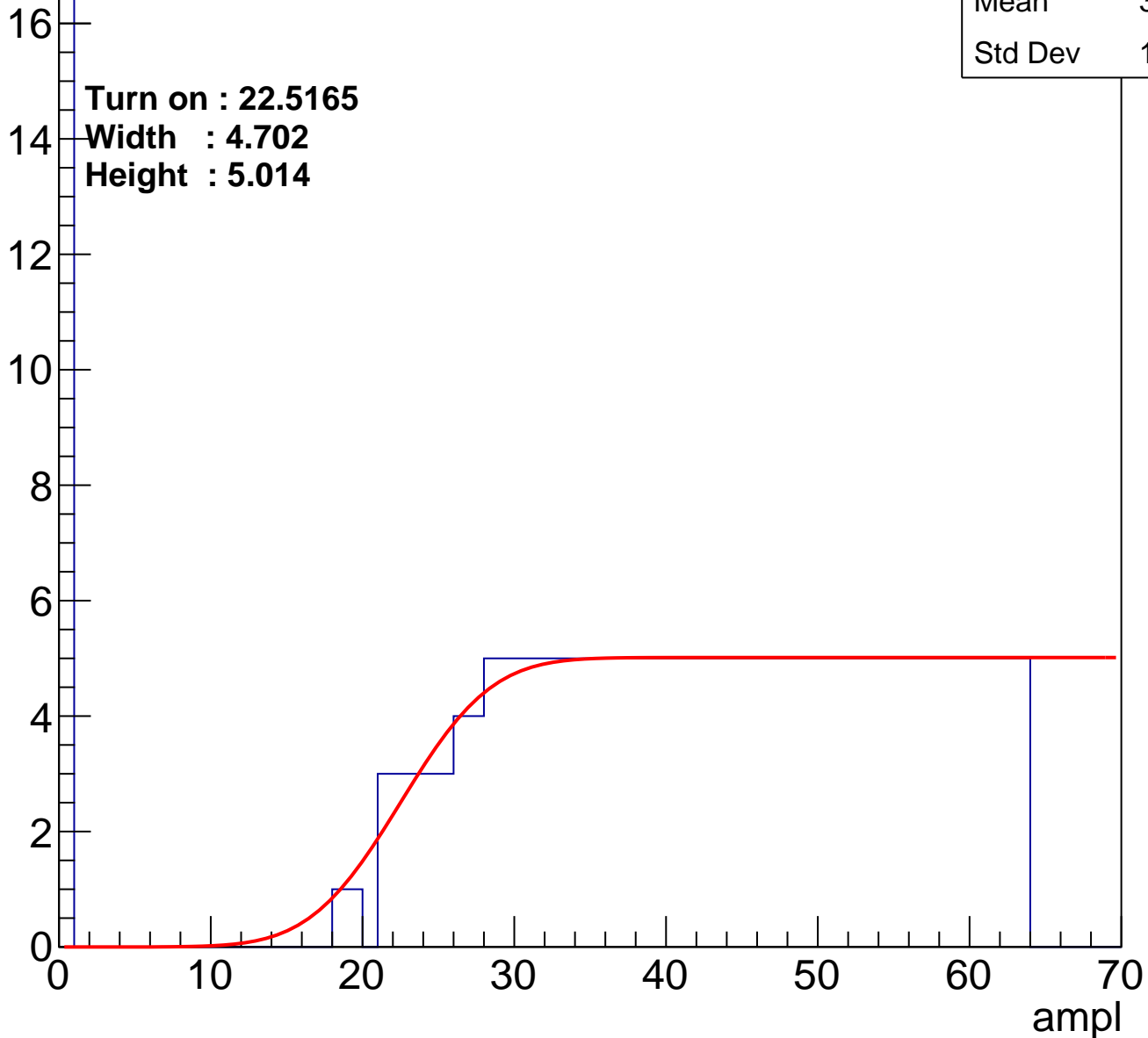
|         |       |
|---------|-------|
| Entries | 222   |
| Mean    | 39.57 |
| Std Dev | 16.27 |

Turn on : 22.5165

Width : 4.702

Height : 5.014

Entry



# B1L103S, U14-ch75

calib\_packv5\_041523\_1651.root, FC#0, Port C2

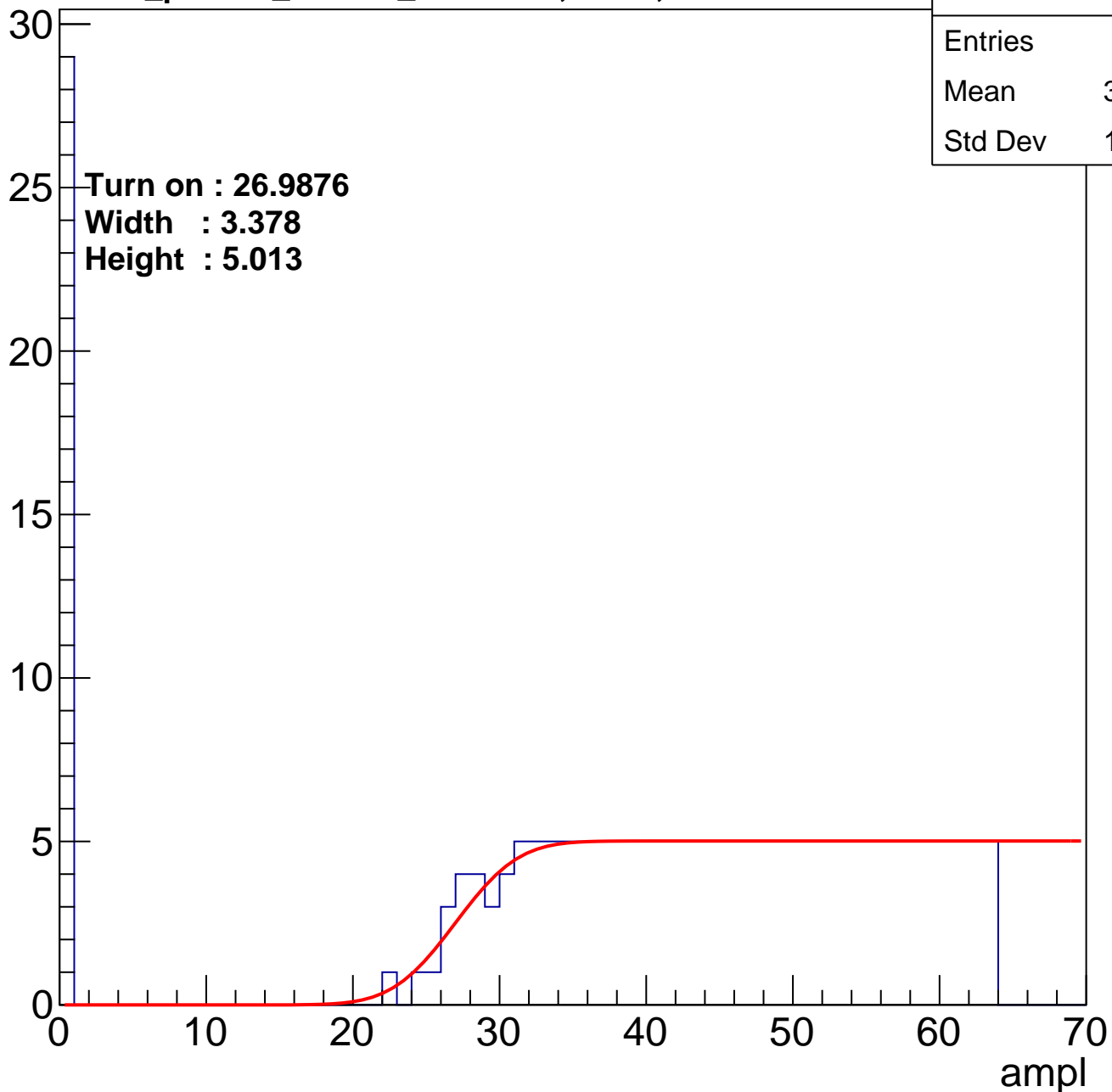
|         |       |
|---------|-------|
| Entries | 215   |
| Mean    | 38.75 |
| Std Dev | 18.37 |

Turn on : 26.9876

Width : 3.378

Height : 5.013

Entry



# B1L103S, U14-ch76

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 232   |
| Mean    | 37.59 |
| Std Dev | 18.24 |

**Turn on : 23.2337**

**Width : 4.182**

**Height : 5.006**

Entry

30

25

20

15

10

5

0

0

10

20

30

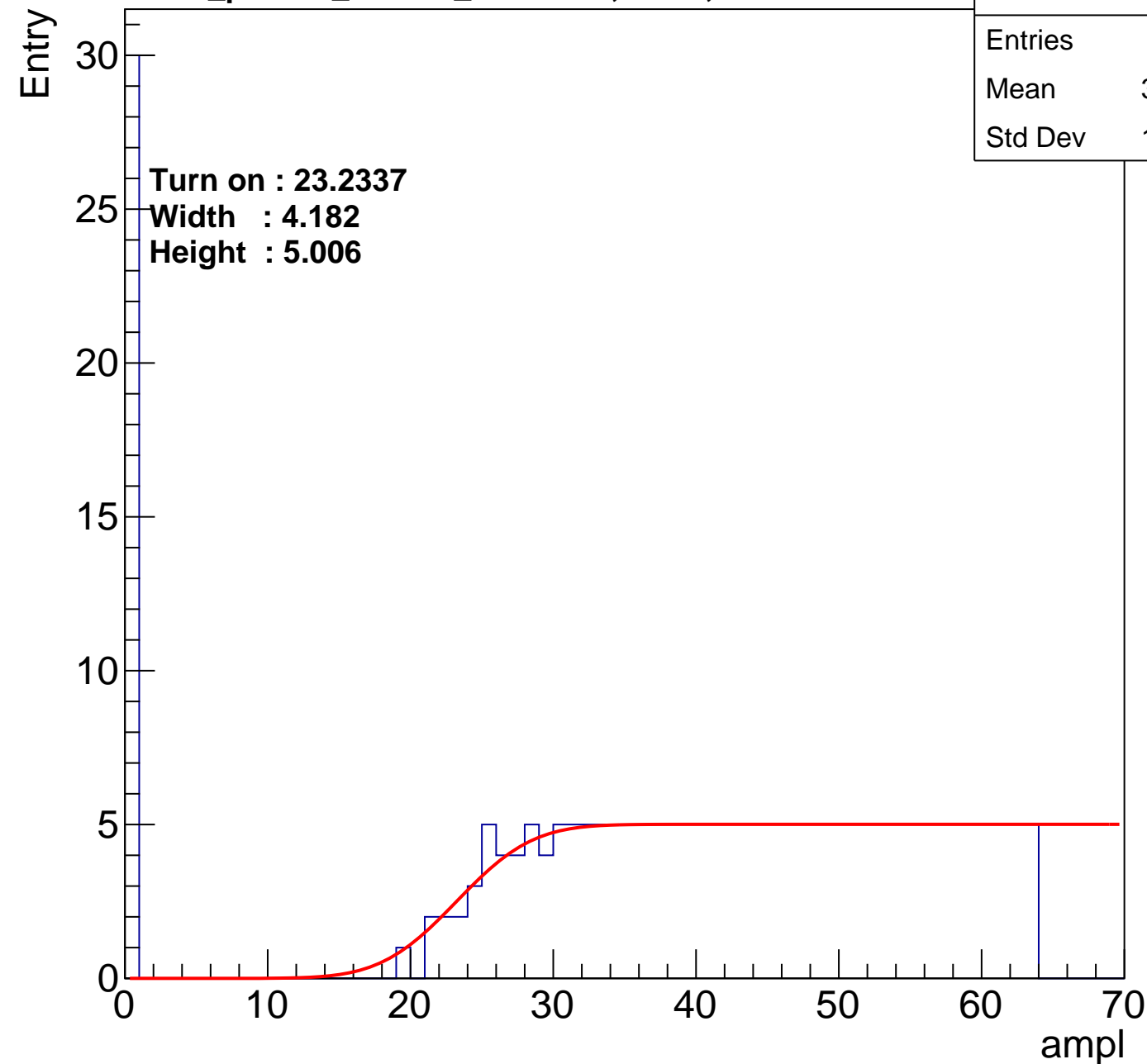
40

50

60

70

ampl



# B1L103S, U14-ch77

calib\_packv5\_041523\_1651.root, FC#0, Port C2

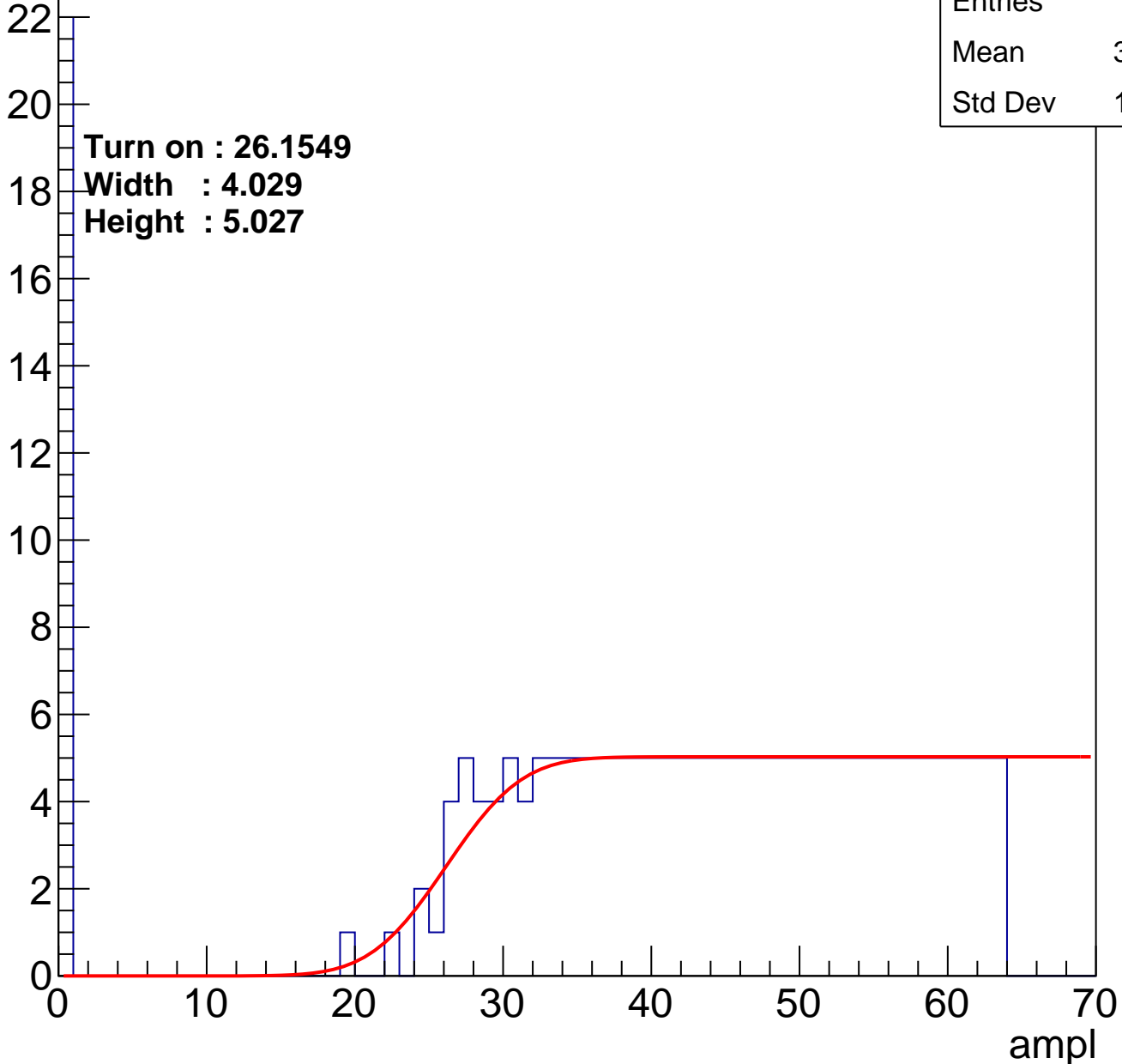
|         |       |
|---------|-------|
| Entries | 213   |
| Mean    | 39.69 |
| Std Dev | 17.18 |

**Turn on : 26.1549**

**Width : 4.029**

**Height : 5.027**

Entry



# B1L103S, U14-ch78

calib\_packv5\_041523\_1651.root, FC#0, Port C2

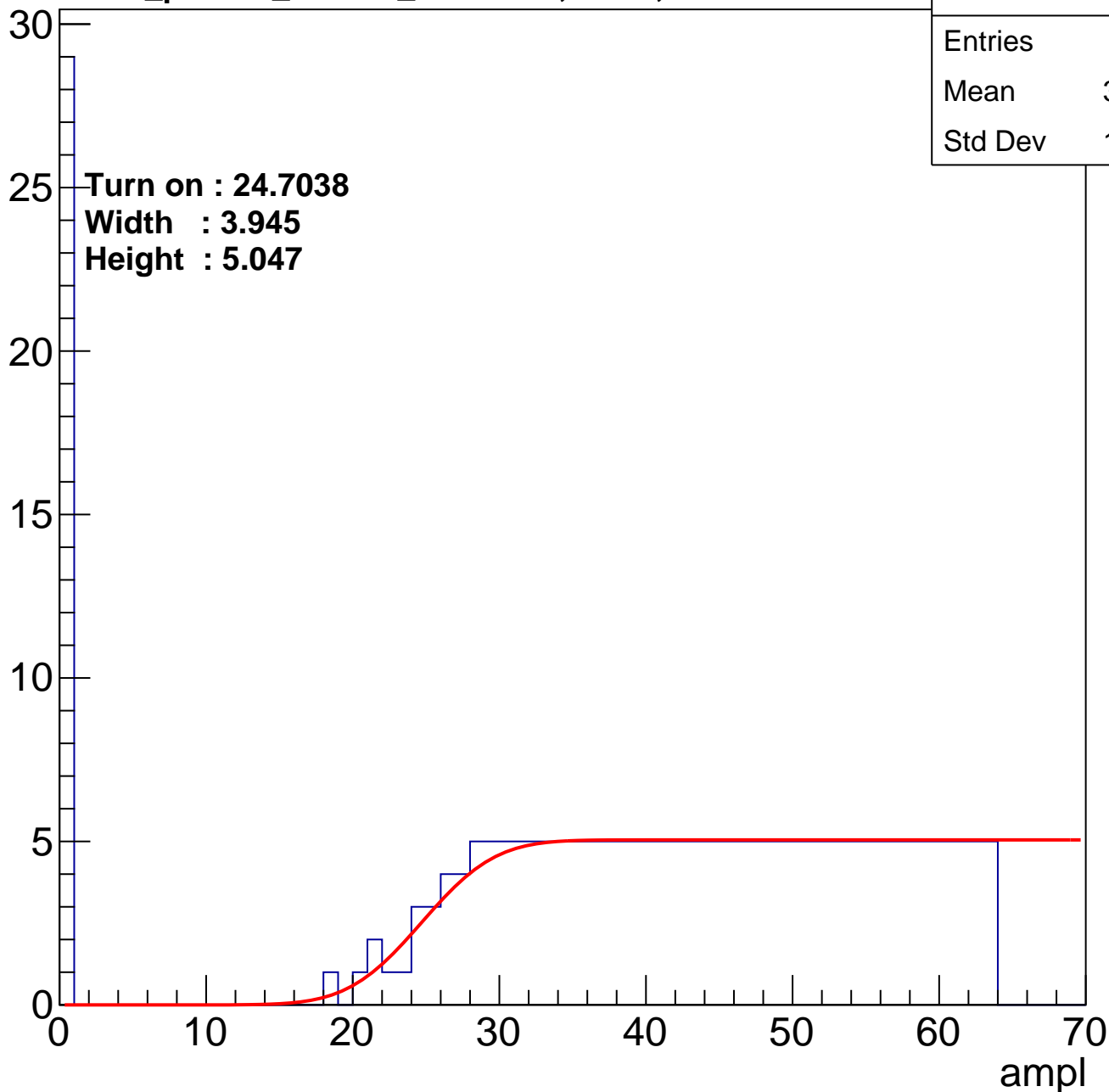
|         |       |
|---------|-------|
| Entries | 229   |
| Mean    | 37.88 |
| Std Dev | 18.14 |

Turn on : 24.7038

Width : 3.945

Height : 5.047

Entry



# B1L103S, U14-ch79

calib\_packv5\_041523\_1651.root, FC#0, Port C2

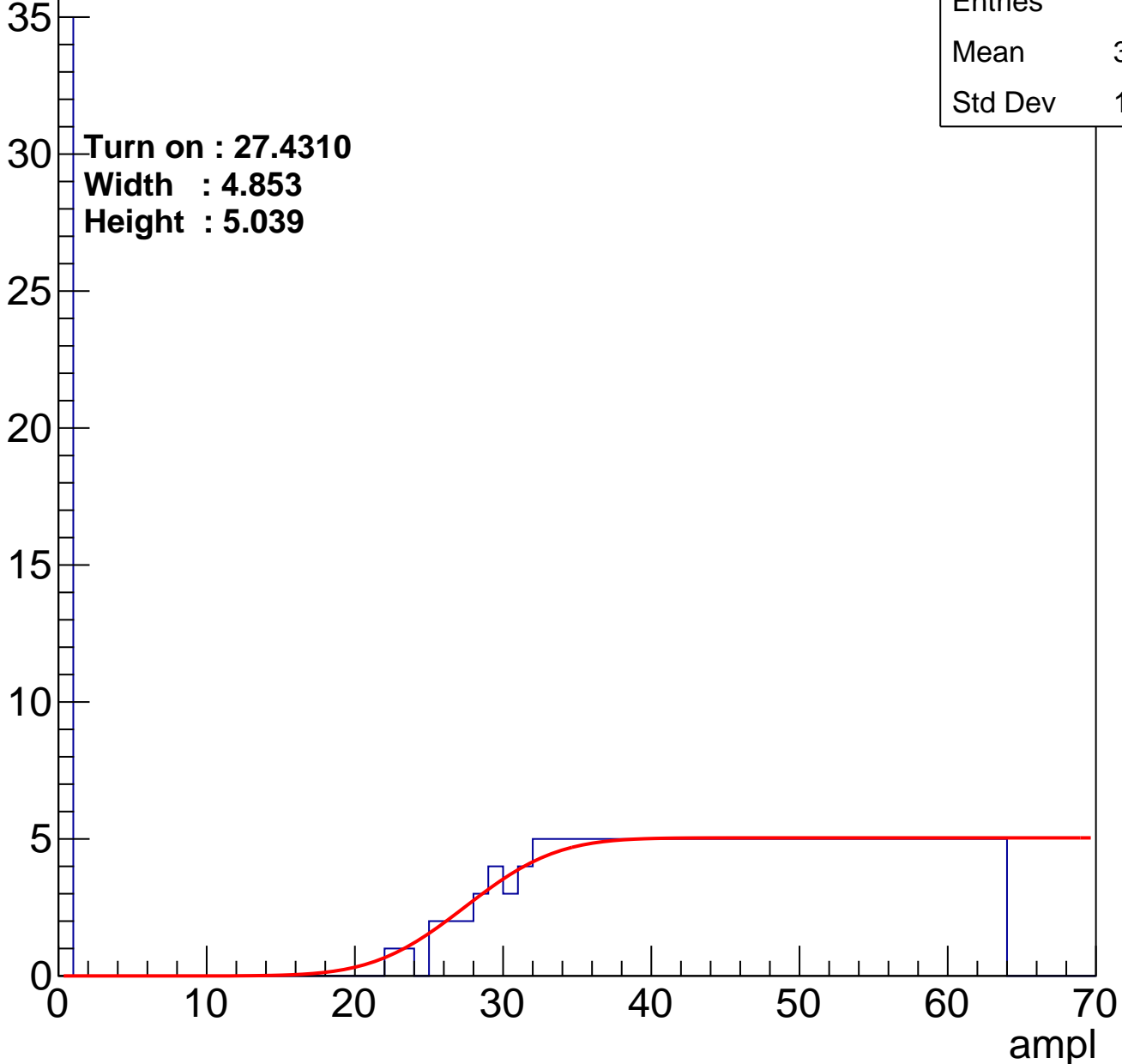
|         |       |
|---------|-------|
| Entries | 217   |
| Mean    | 37.86 |
| Std Dev | 19.32 |

Turn on : 27.4310

Width : 4.853

Height : 5.039

Entry





# B1L103S, U14-ch80

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 220   |
| Mean    | 38.81 |
| Std Dev | 17.76 |

**Turn on : 25.1382**

**Width : 2.934**

**Height : 4.991**

Entry

25

20

15

10

5

0

0

10

20

30

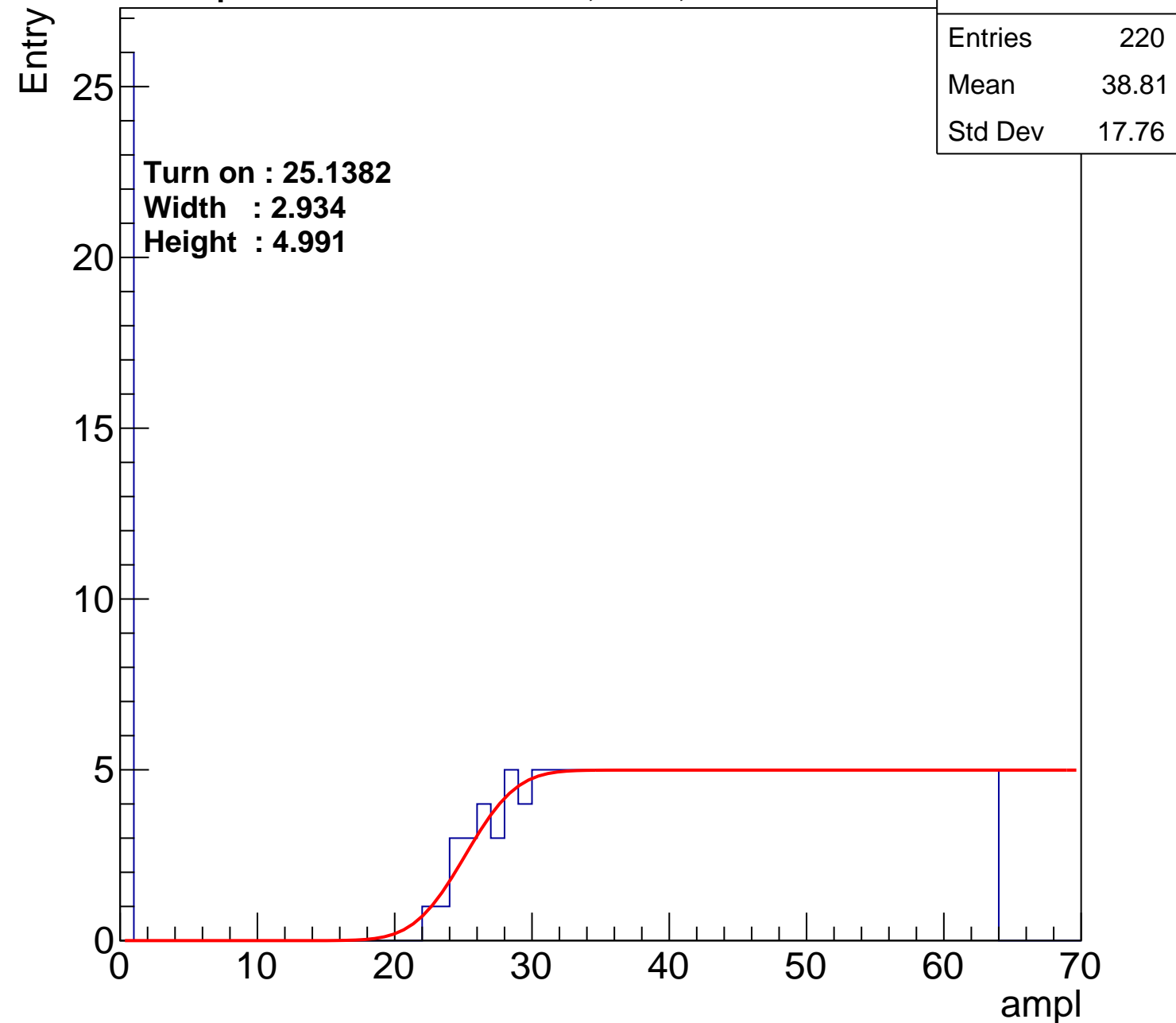
40

50

60

70

ampl



# B1L103S, U14-ch81

calib\_packv5\_041523\_1651.root, FC#0, Port C2

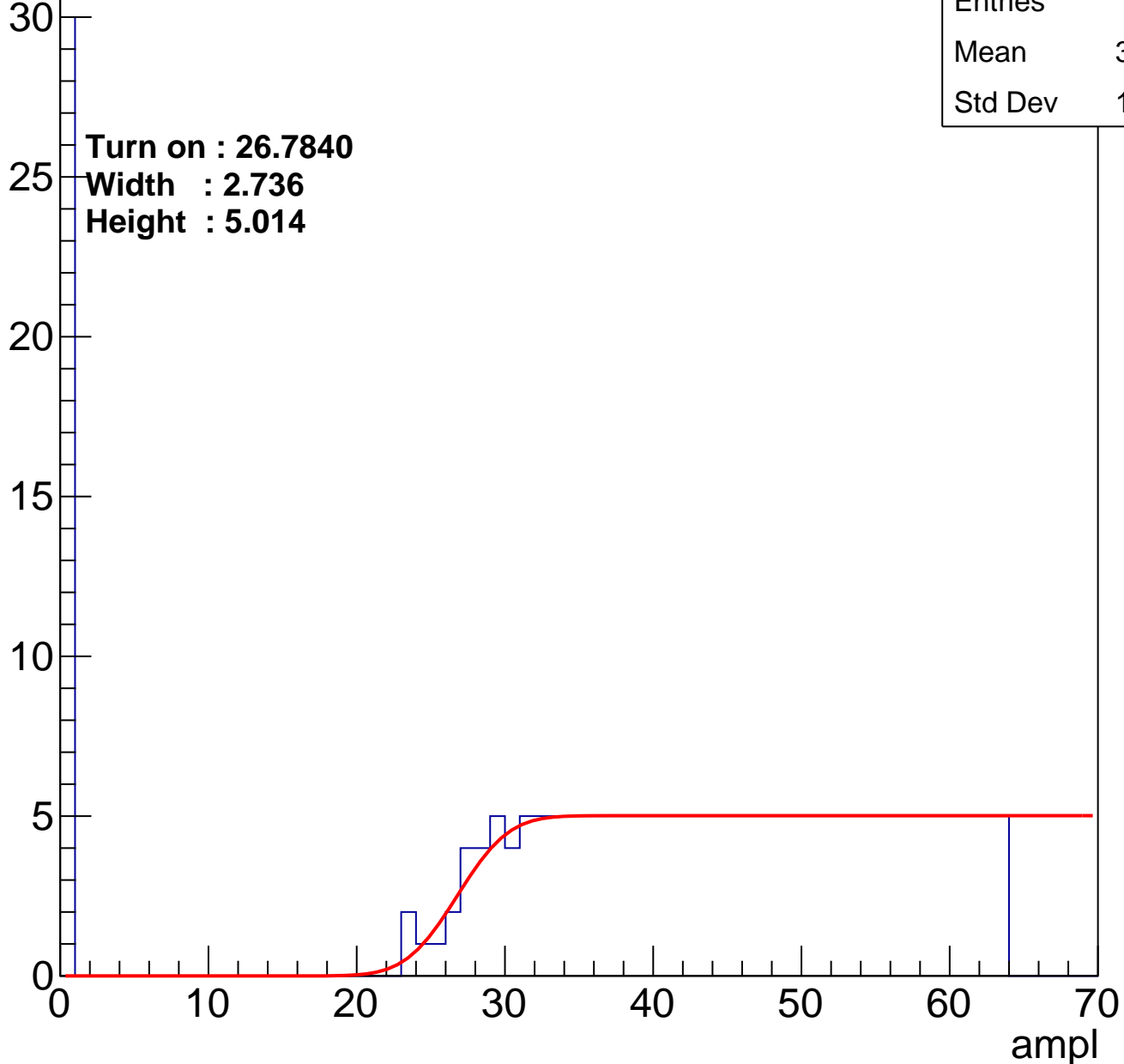
|         |       |
|---------|-------|
| Entries | 218   |
| Mean    | 38.47 |
| Std Dev | 18.45 |

**Turn on : 26.7840**

**Width : 2.736**

**Height : 5.014**

Entry

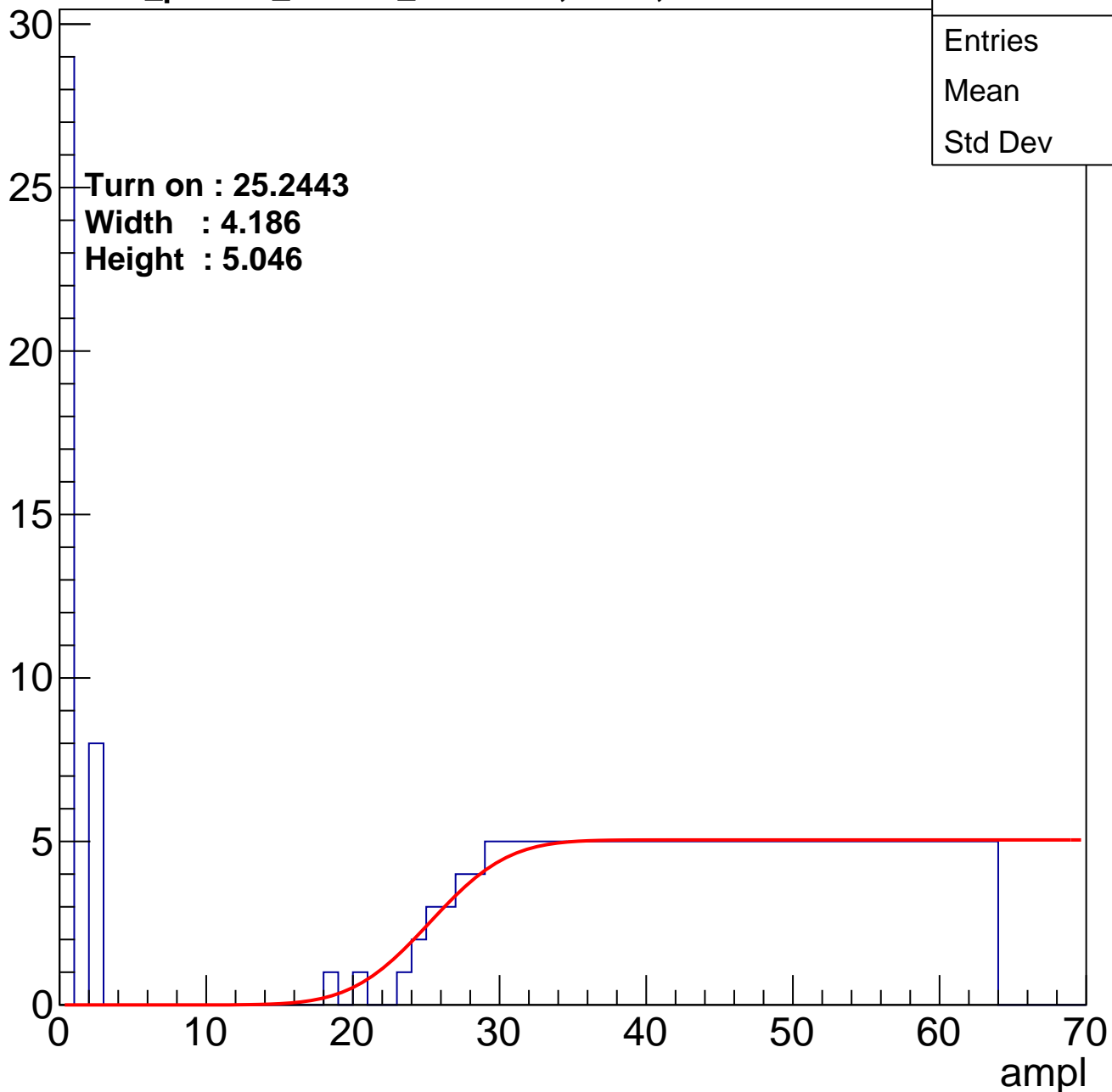


# B1L103S, U14-ch82

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |      |
|---------|------|
| Entries | 231  |
| Mean    | 37   |
| Std Dev | 19.1 |

Entry



# B1L103S, U14-ch83

calib\_packv5\_041523\_1651.root, FC#0, Port C2

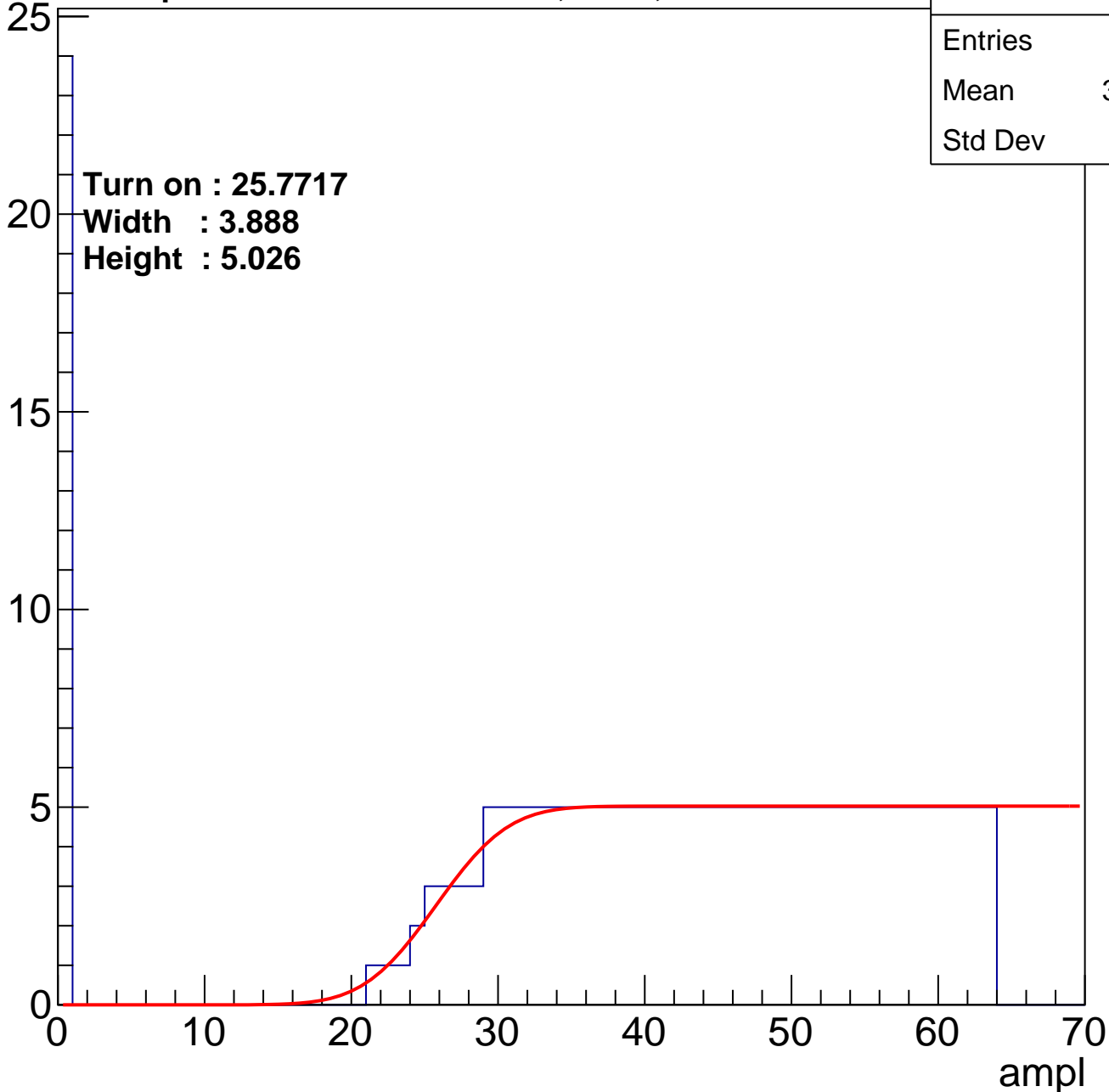
|         |       |
|---------|-------|
| Entries | 216   |
| Mean    | 39.27 |
| Std Dev | 17.5  |

Turn on : 25.7717

Width : 3.888

Height : 5.026

Entry



# B1L103S, U14-ch84

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 223   |
| Mean    | 38.17 |
| Std Dev | 18.35 |

**Turn on : 25.9625**

**Width : 2.955**

**Height : 5.008**

Entry

30

25

20

15

10

5

0

0

10

20

30

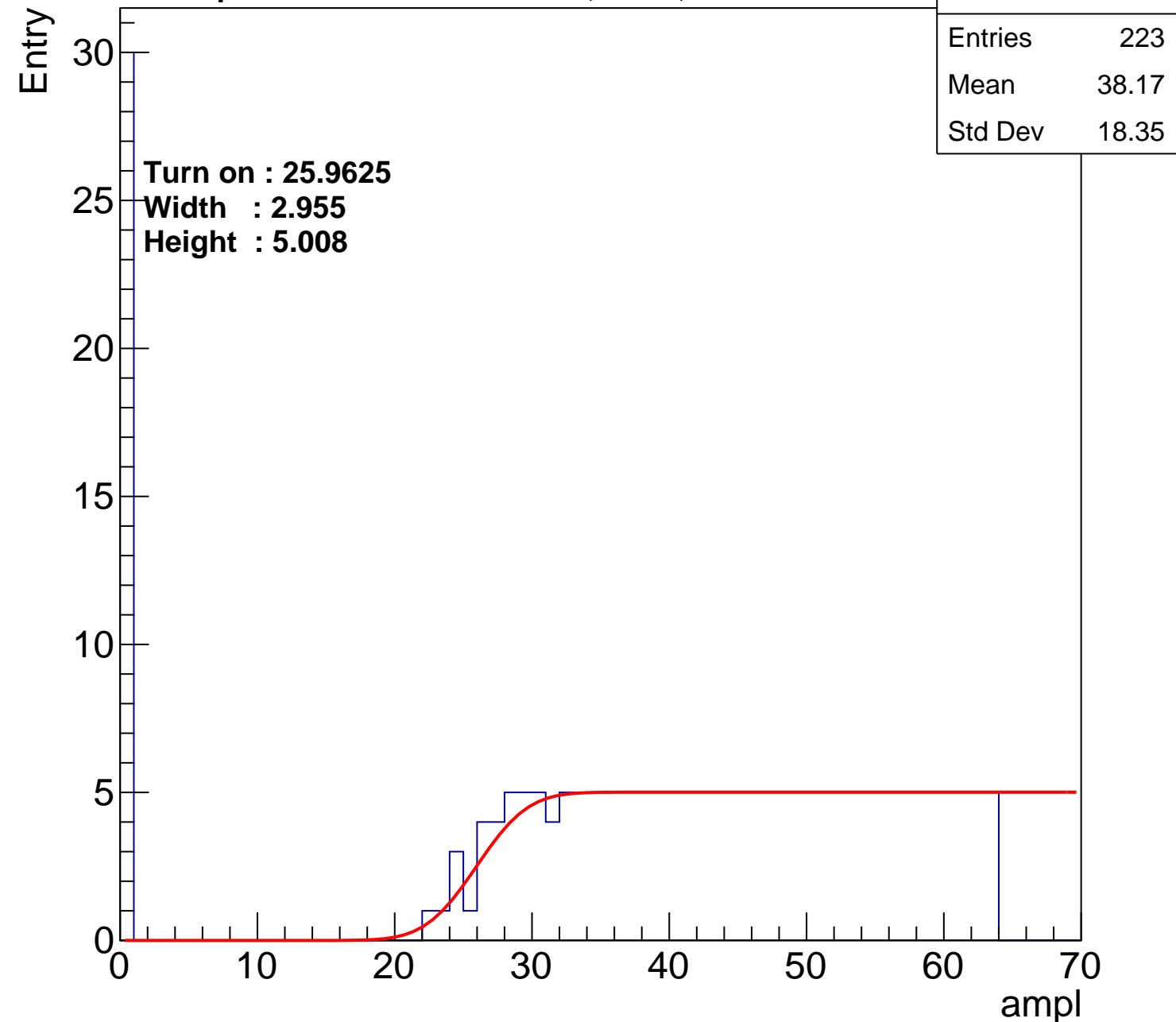
40

50

60

70

ampl



# B1L103S, U14-ch85

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 213   |
| Mean    | 39.19 |
| Std Dev | 17.92 |

**Turn on : 26.3502**

**Width : 4.527**

**Height : 5.020**

Entry

25

20

15

10

5

0

ampl

0

10

20

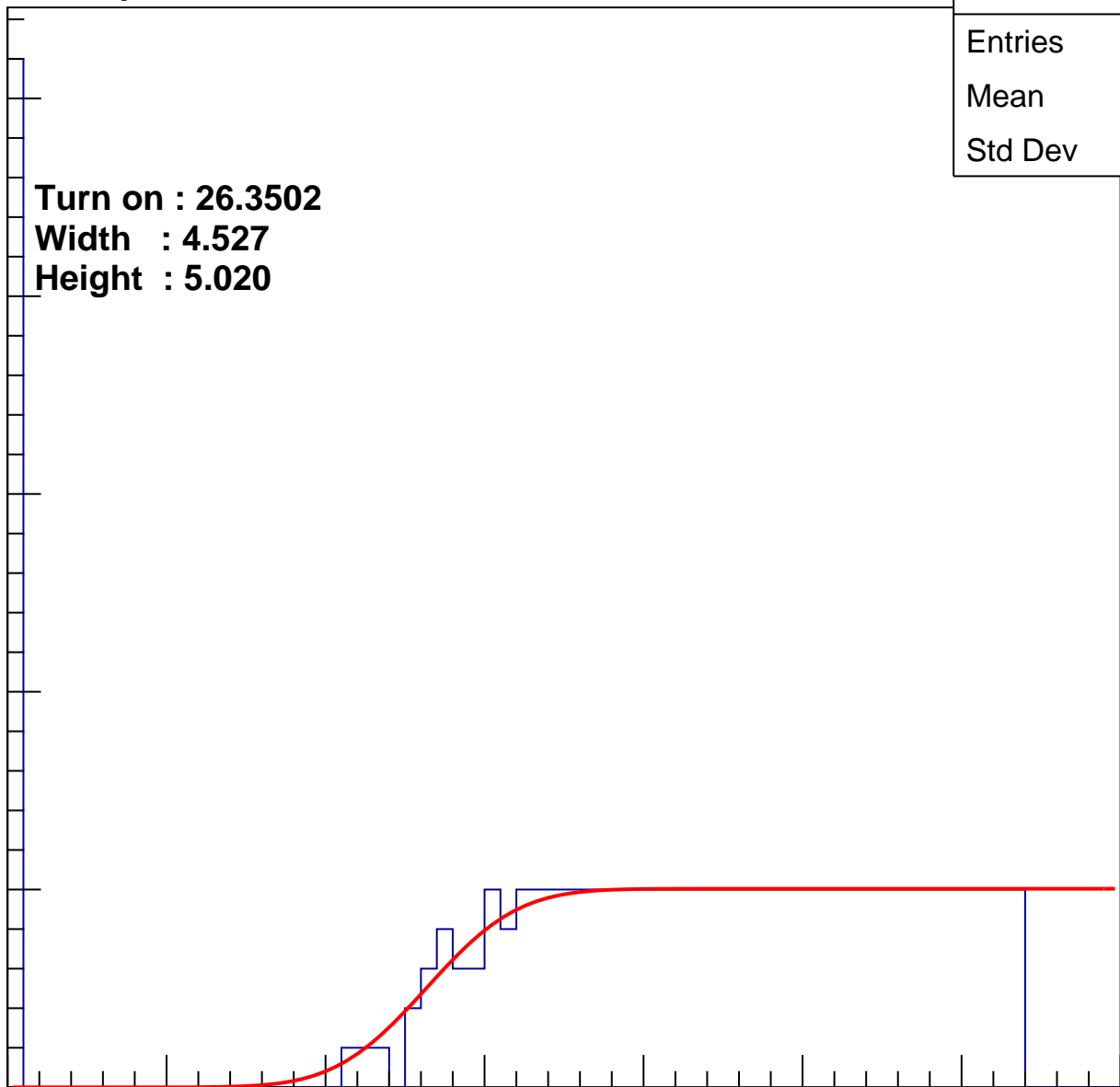
30

40

50

60

70



# B1L103S, U14-ch86

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 233   |
| Mean    | 37.44 |
| Std Dev | 18.35 |

**Turn on : 23.1874**

**Width : 3.884**

**Height : 5.005**

Entry

30

25

20

15

10

5

0

0

10

20

30

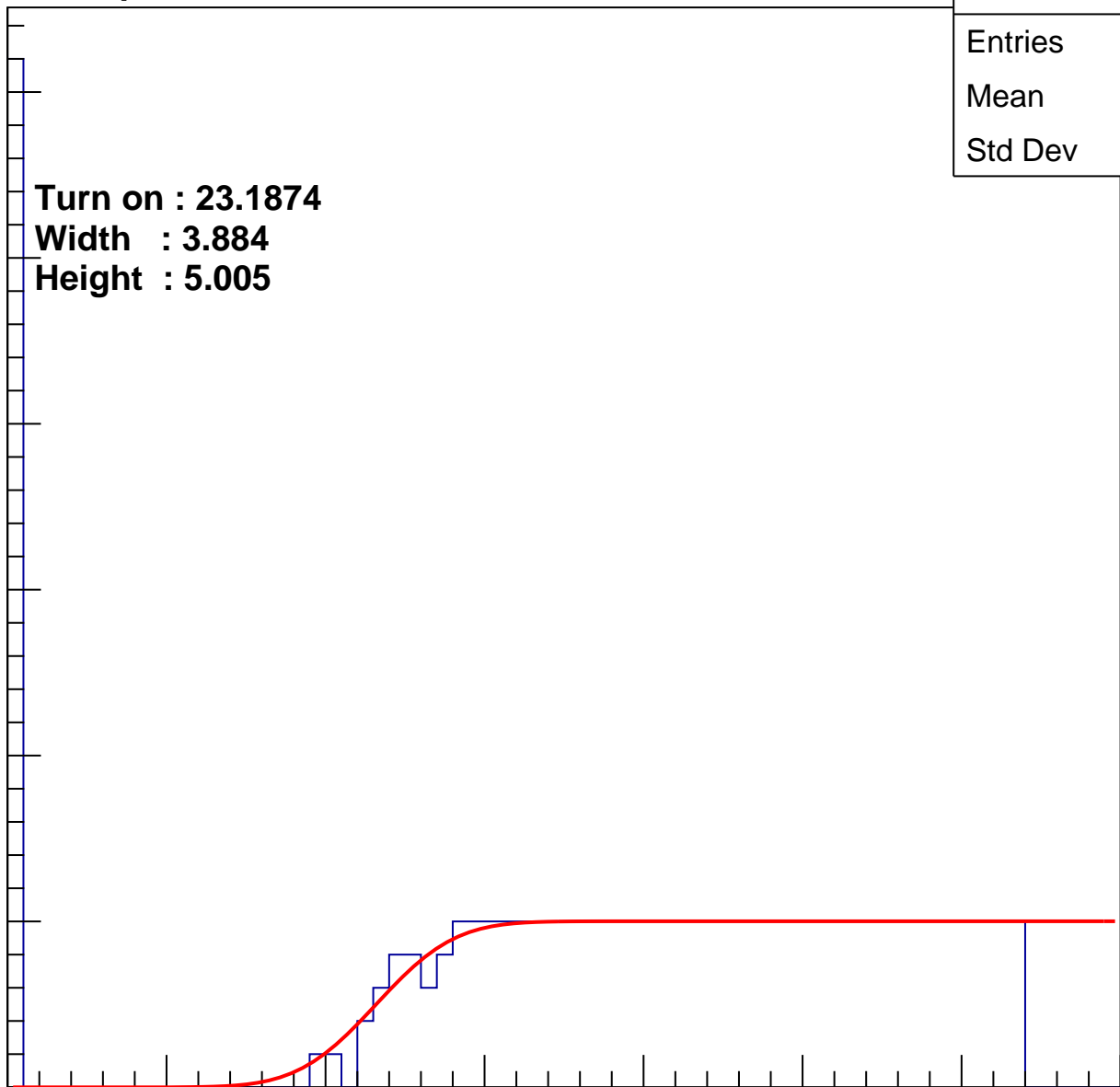
40

50

60

70

ampl



# B1L103S, U14-ch87

calib\_packv5\_041523\_1651.root, FC#0, Port C2

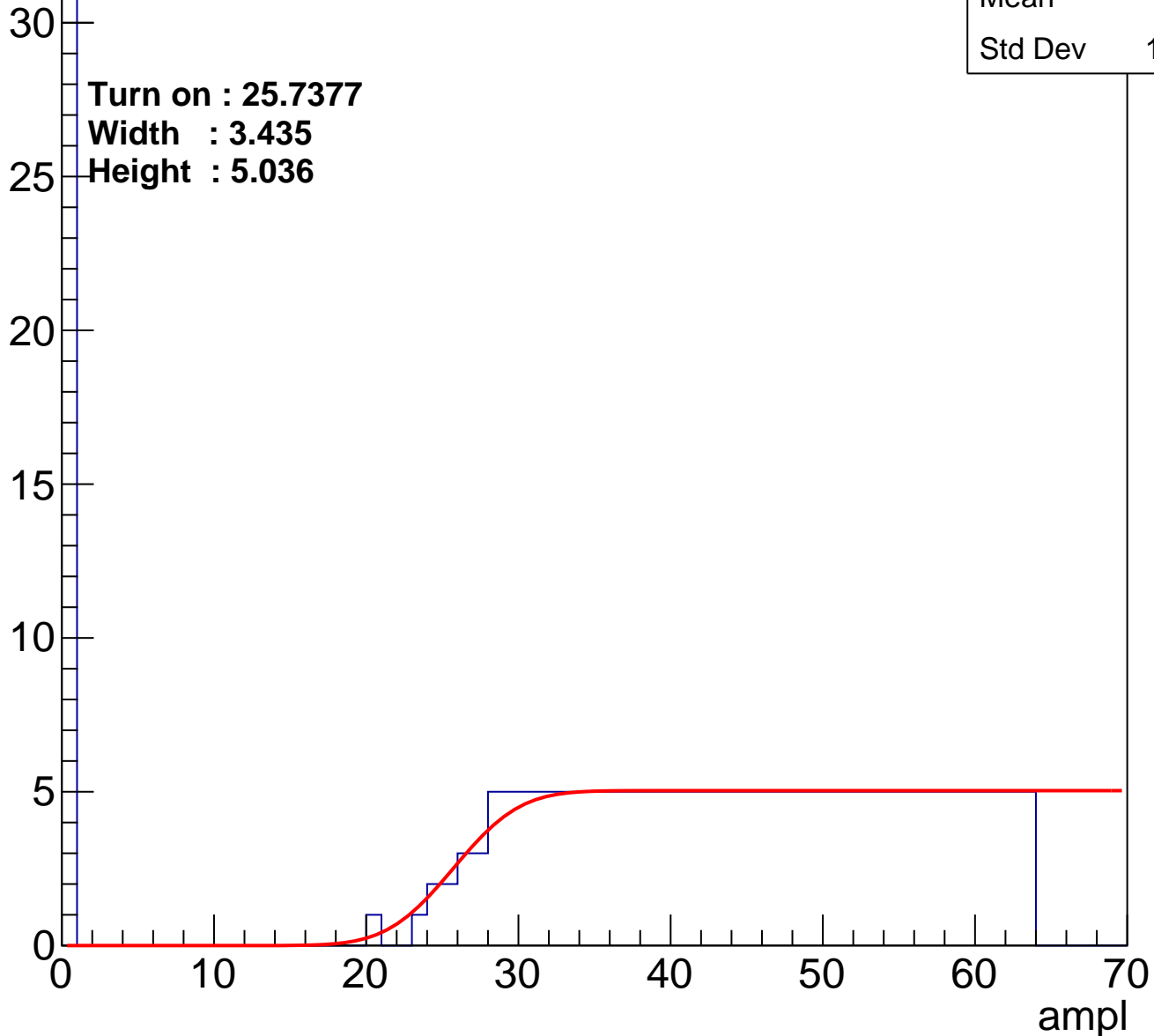
|         |       |
|---------|-------|
| Entries | 224   |
| Mean    | 37.9  |
| Std Dev | 18.64 |

**Turn on : 25.7377**

**Width : 3.435**

**Height : 5.036**

Entry





# B1L103S, U14-ch88

calib\_packv5\_041523\_1651.root, FC#0, Port C2

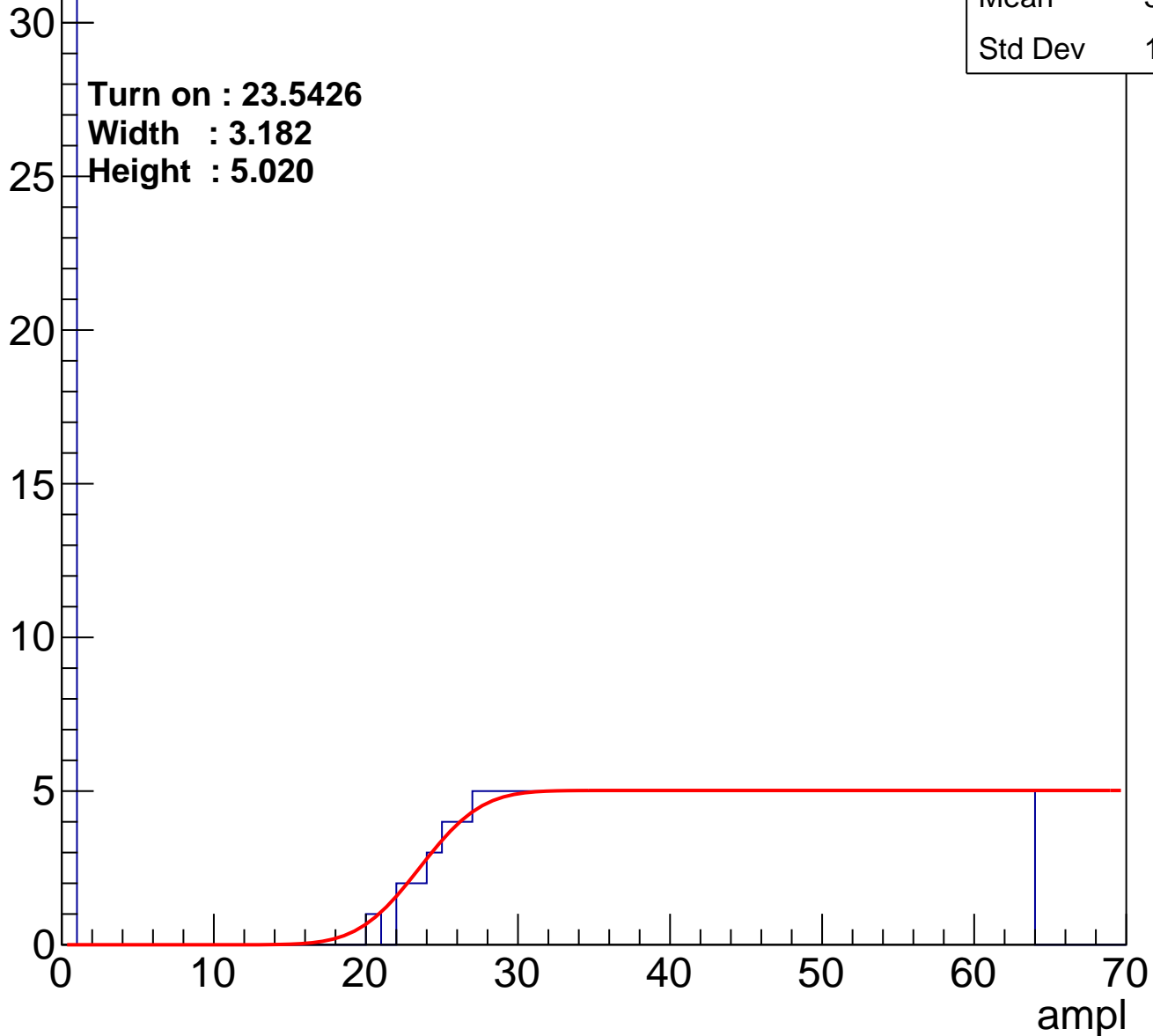
|         |       |
|---------|-------|
| Entries | 233   |
| Mean    | 37.39 |
| Std Dev | 18.46 |

**Turn on : 23.5426**

**Width : 3.182**

**Height : 5.020**

Entry



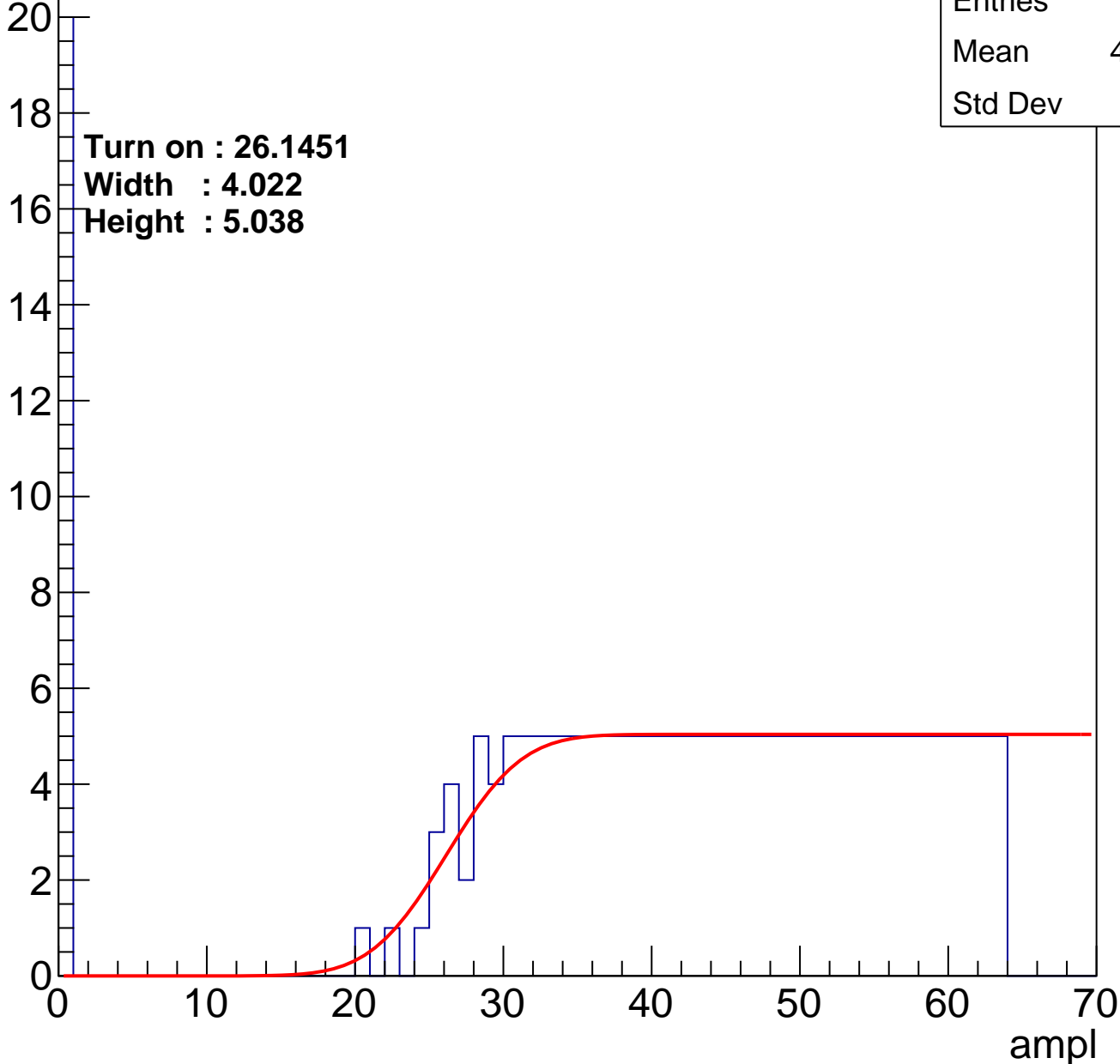
# B1L103S, U14-ch89

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 211   |
| Mean    | 40.09 |
| Std Dev | 16.8  |

**Turn on : 26.1451**  
**Width : 4.022**  
**Height : 5.038**

Entry



# B1L103S, U14-ch90

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 225   |
| Mean    | 38.59 |
| Std Dev | 17.54 |

Turn on : 24.3313

Width : 3.142

Height : 5.024

Entry

25

20

15

10

5

0

0

10

20

30

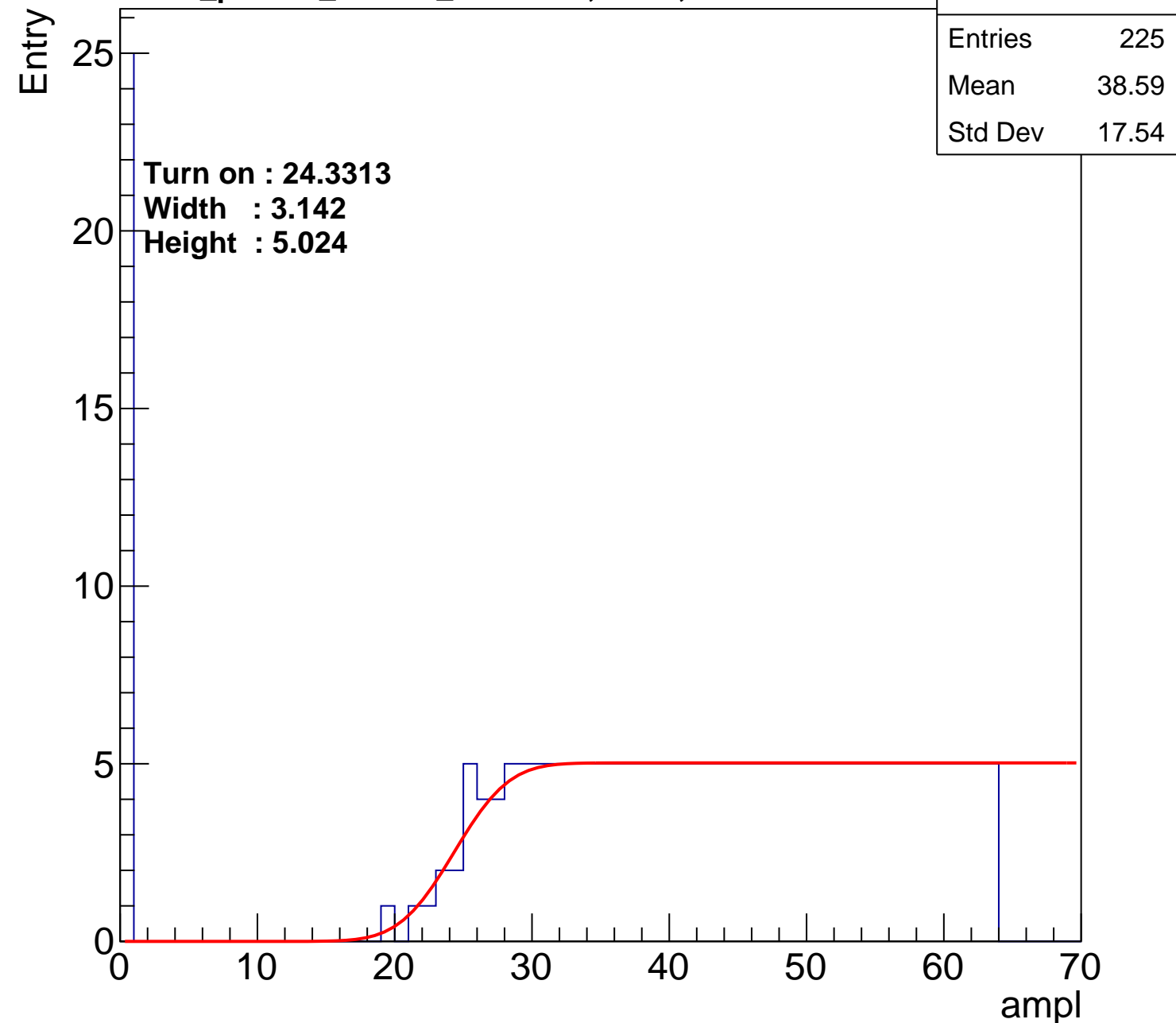
40

50

60

70

ampl



# B1L103S, U14-ch91

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 217   |
| Mean    | 38.85 |
| Std Dev | 18    |

**Turn on : 26.3270**

**Width : 4.058**

**Height : 5.029**

Entry

25

20

15

10

5

0

0

10

20

30

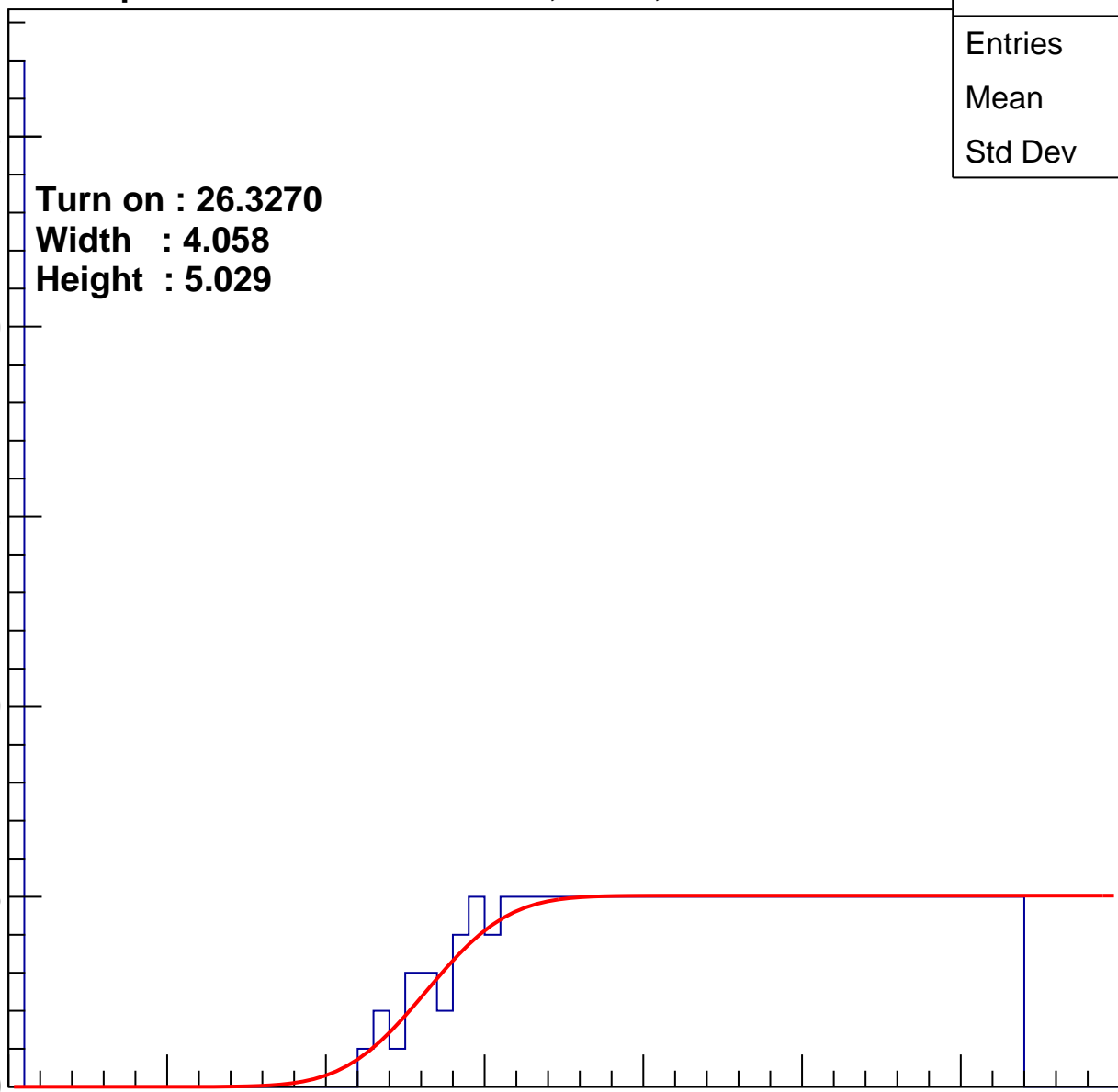
40

50

60

70

ampl



# B1L103S, U14-ch92

calib\_packv5\_041523\_1651.root, FC#0, Port C2

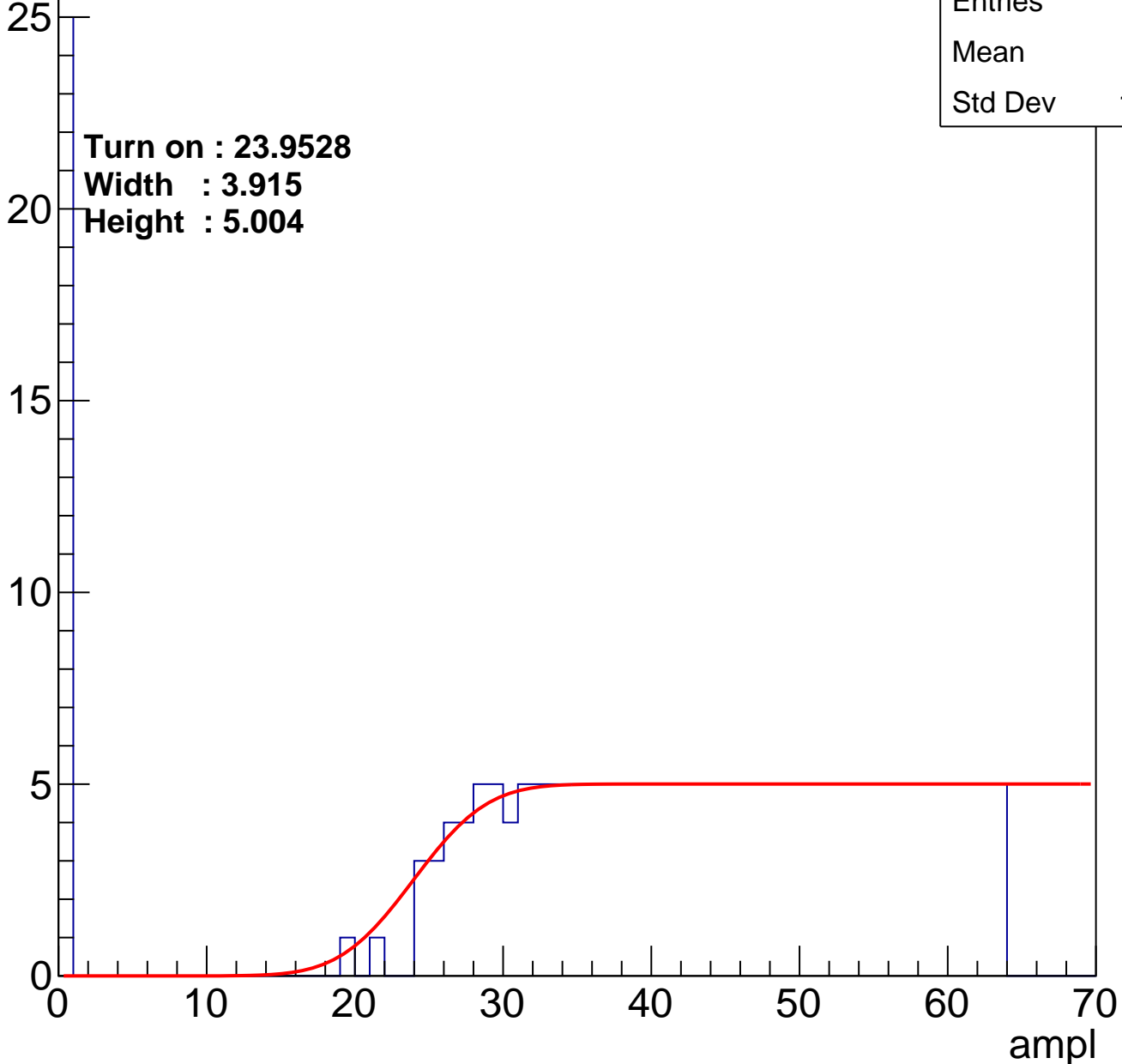
|         |       |
|---------|-------|
| Entries | 220   |
| Mean    | 38.9  |
| Std Dev | 17.61 |

**Turn on : 23.9528**

**Width : 3.915**

**Height : 5.004**

Entry



# B1L103S, U14-ch93

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 225   |
| Mean    | 38.33 |
| Std Dev | 17.89 |

**Turn on : 23.6026**

**Width : 4.960**

**Height : 5.021**

Entry

25

20

15

10

5

0

0

10

20

30

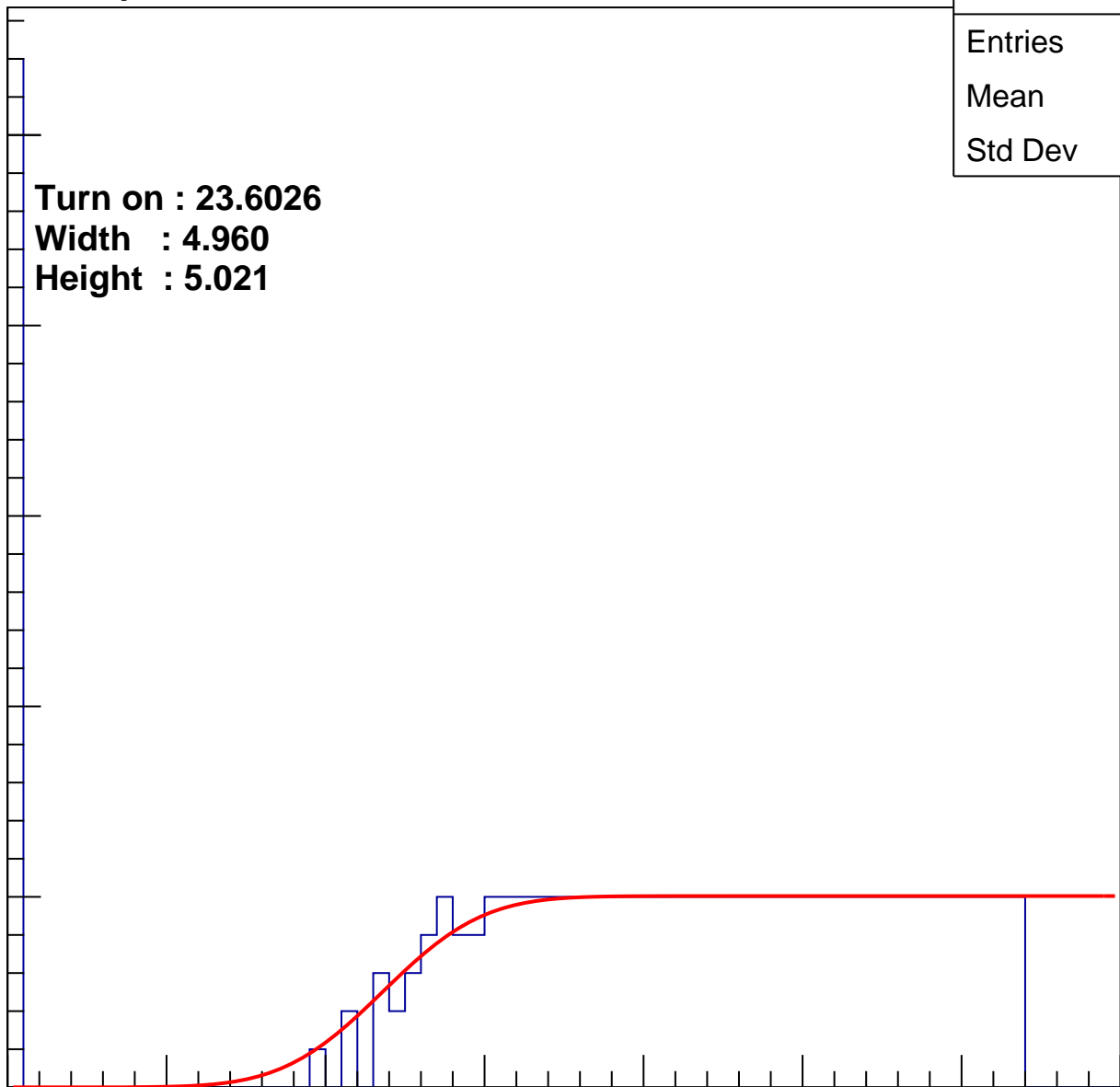
40

50

60

70

ampl



# B1L103S, U14-ch94

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 224   |
| Mean    | 38.46 |
| Std Dev | 17.78 |

**Turn on : 24.0824**

**Width : 5.035**

**Height : 5.017**

Entry

25

20

15

10

5

0

0

10

20

30

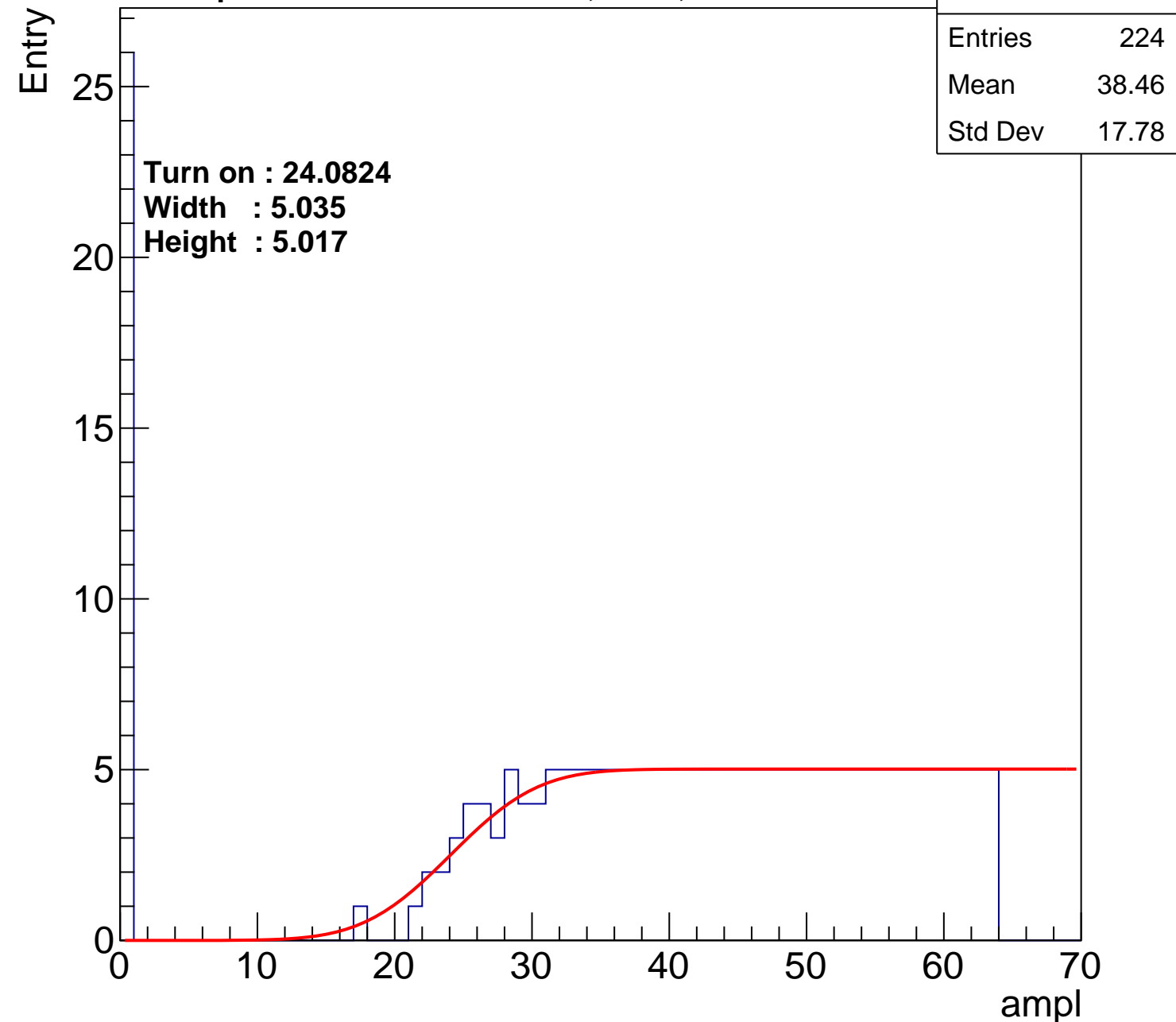
40

50

60

70

ampl



# B1L103S, U14-ch95

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 217   |
| Mean    | 38.98 |
| Std Dev | 17.82 |

**Turn on : 25.8455**

**Width : 2.354**

**Height : 4.978**

Entry

25

20

15

10

5

0

0

10

20

30

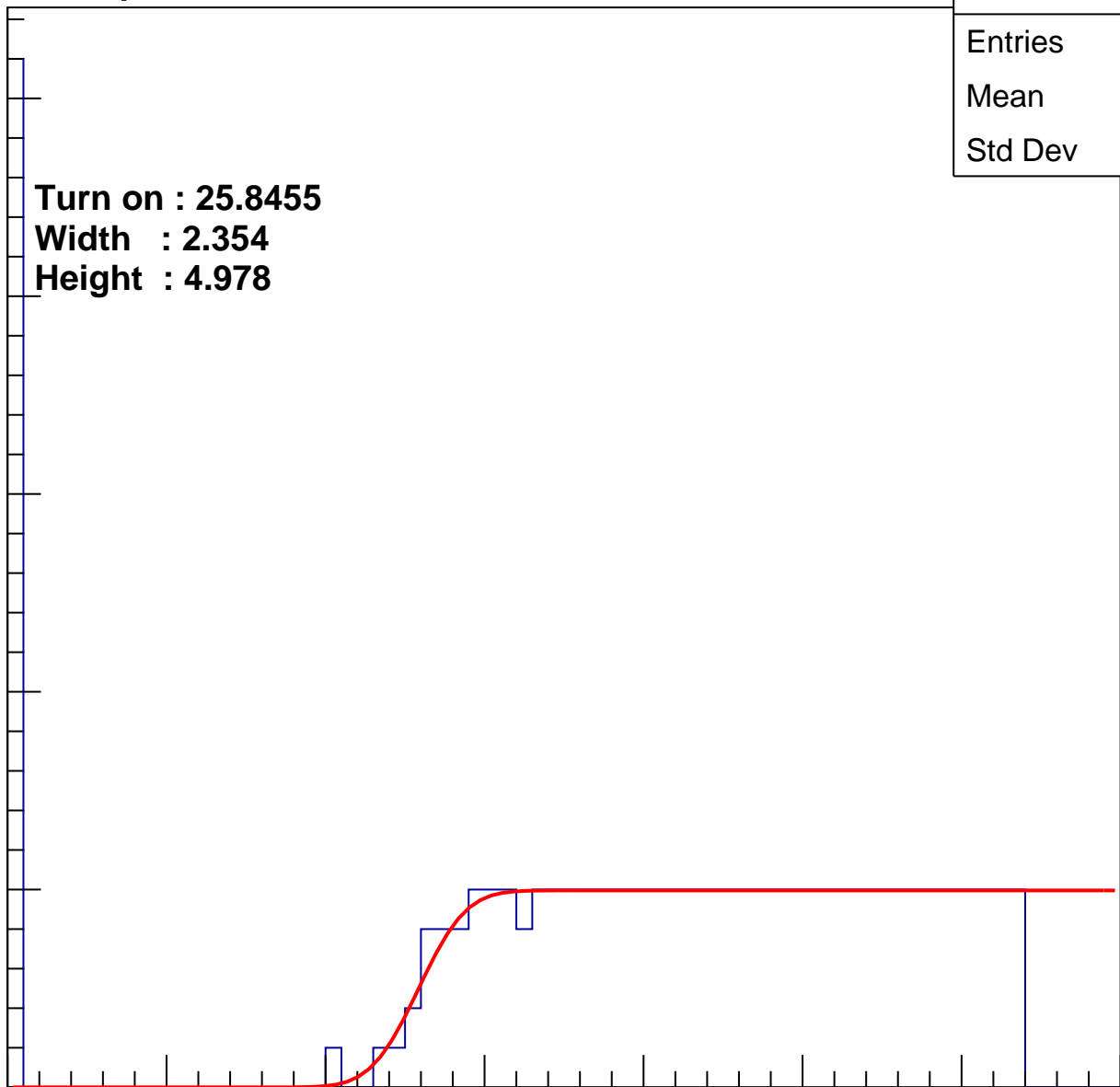
40

50

60

70

ampl





# B1L103S, U14-ch96

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 233   |
| Mean    | 37.23 |
| Std Dev | 18.64 |

**Turn on : 24.4650**

**Width : 4.261**

**Height : 5.039**

Entry

30

25

20

15

10

5

0

ampl

0

10

20

30

40

50

60

70

# B1L103S, U14-ch97

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 234   |
| Mean    | 36.67 |
| Std Dev | 19.28 |

Turn on : 25.1791

Width : 3.613

Height : 5.024

Entry

35

30

25

20

15

10

5

0

0

10

20

30

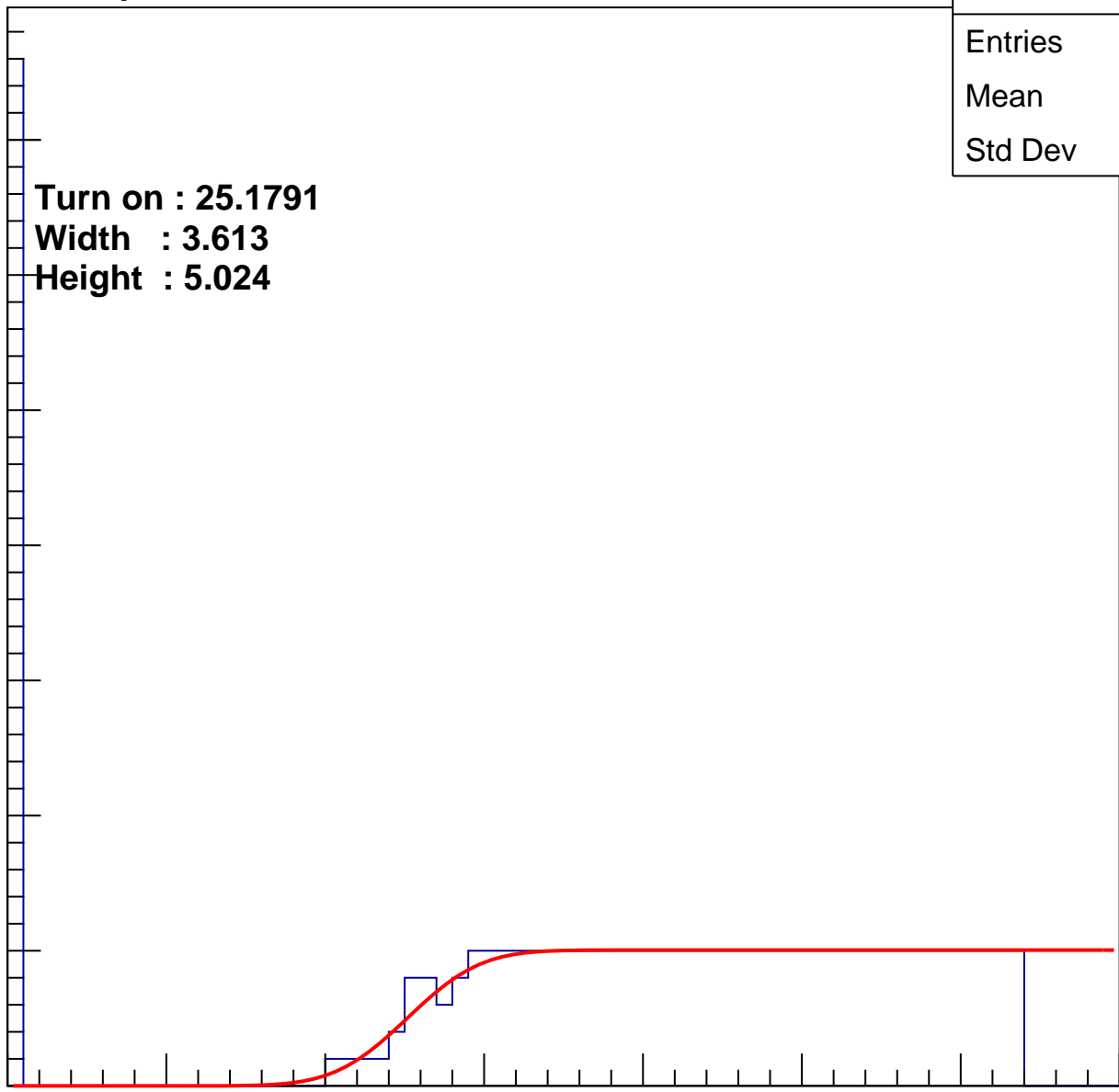
40

50

60

70

ampl



# B1L103S, U14-ch98

calib\_packv5\_041523\_1651.root, FC#0, Port C2

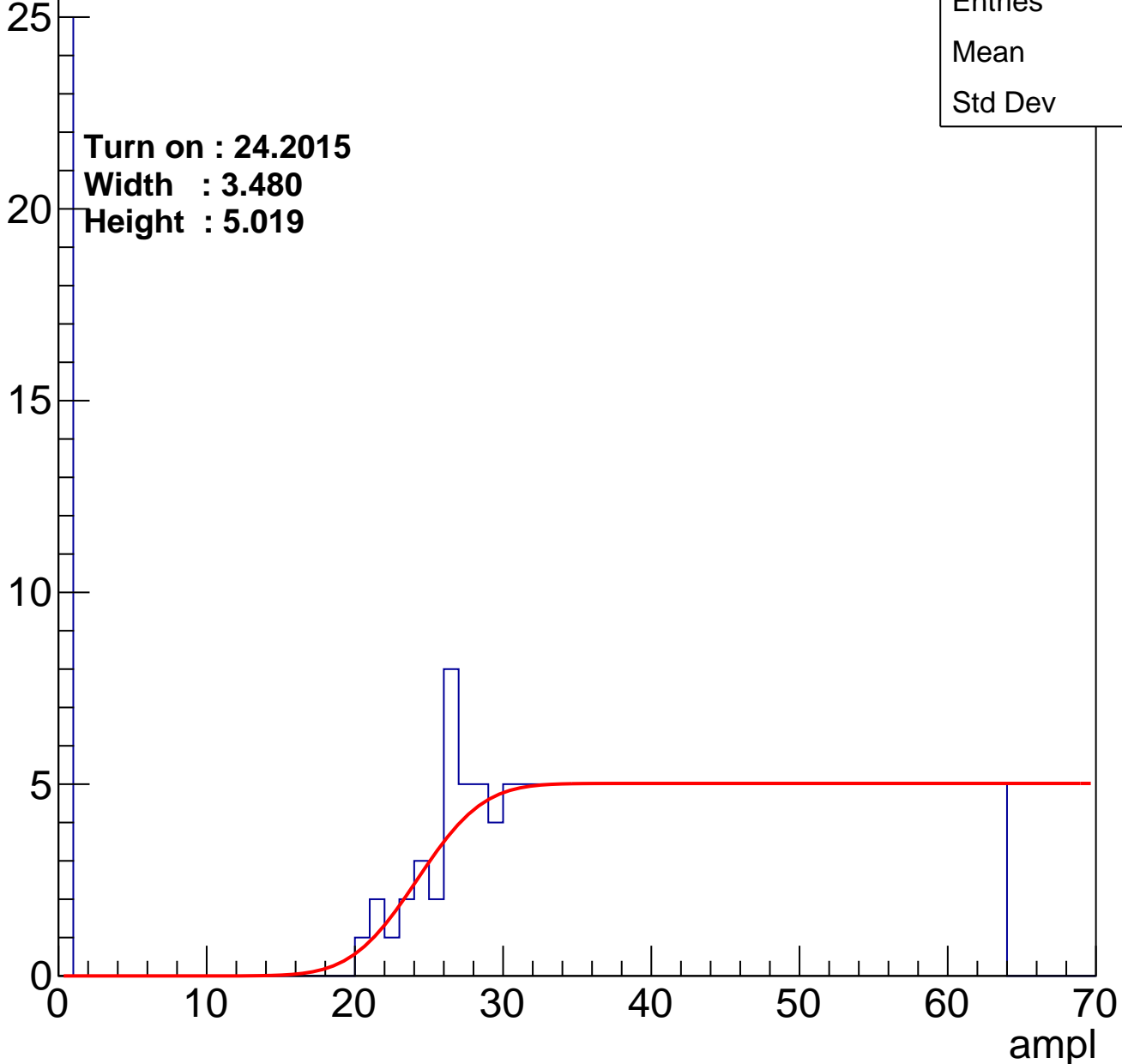
|         |      |
|---------|------|
| Entries | 228  |
| Mean    | 38.4 |
| Std Dev | 17.5 |

Turn on : 24.2015

Width : 3.480

Height : 5.019

Entry

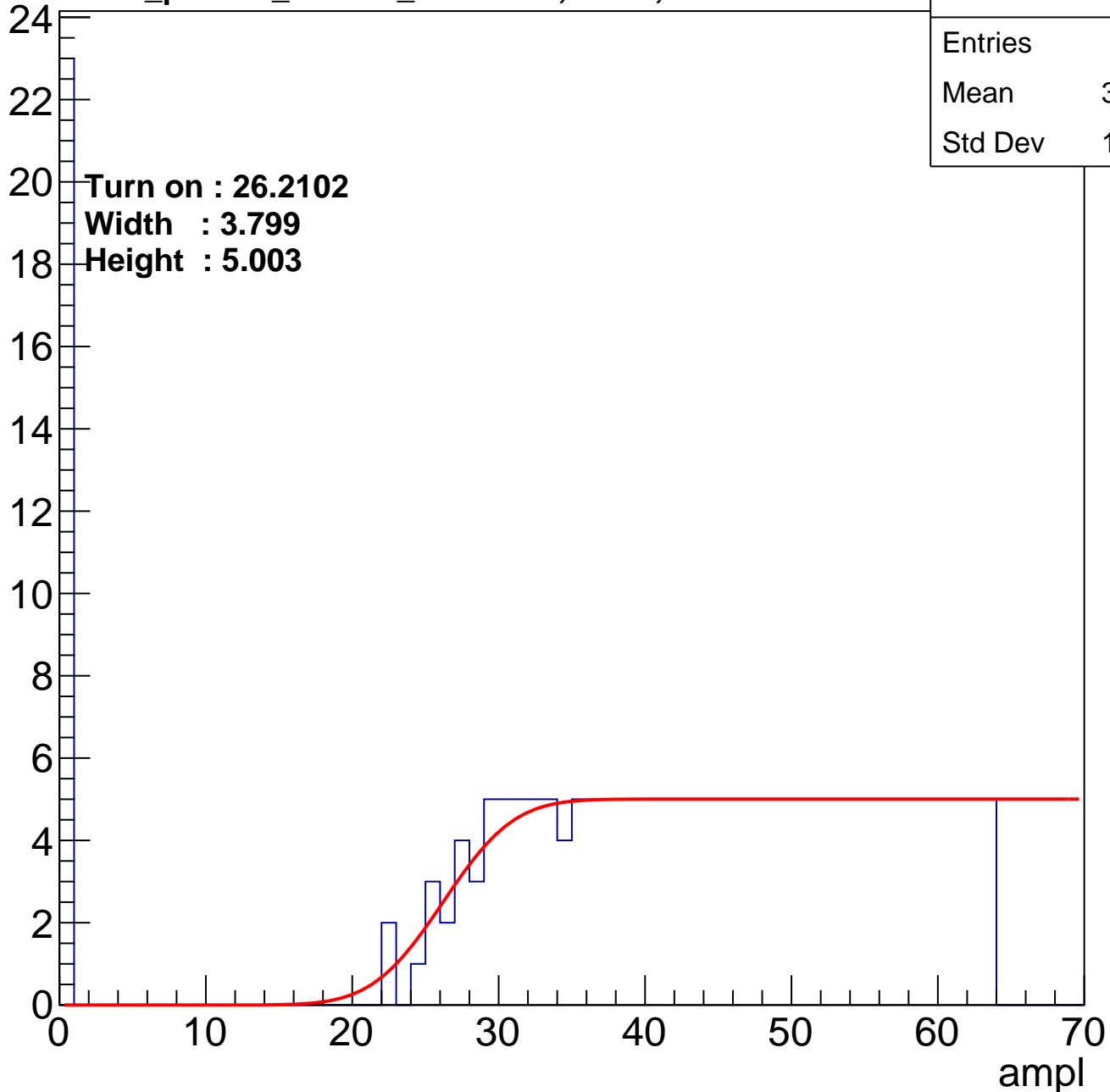


# B1L103S, U14-ch99

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 212   |
| Mean    | 39.64 |
| Std Dev | 17.37 |

Entry



# B1L103S, U14-ch100

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 223   |
| Mean    | 38.15 |
| Std Dev | 18.38 |

**Turn on : 25.7850**

**Width : 4.155**

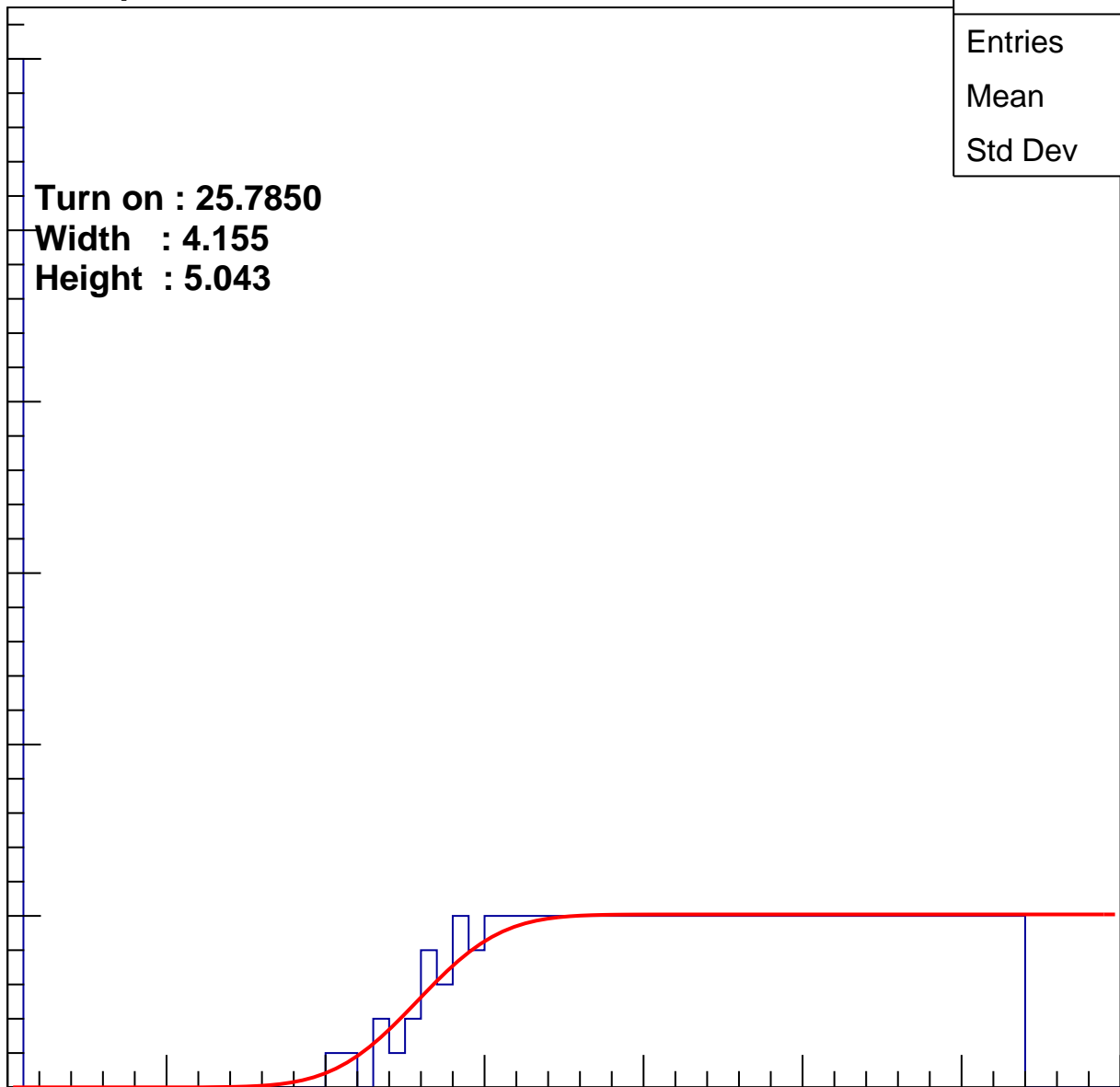
**Height : 5.043**

Entry

30  
25  
20  
15  
10  
5  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U14-ch101

calib\_packv5\_041523\_1651.root, FC#0, Port C2

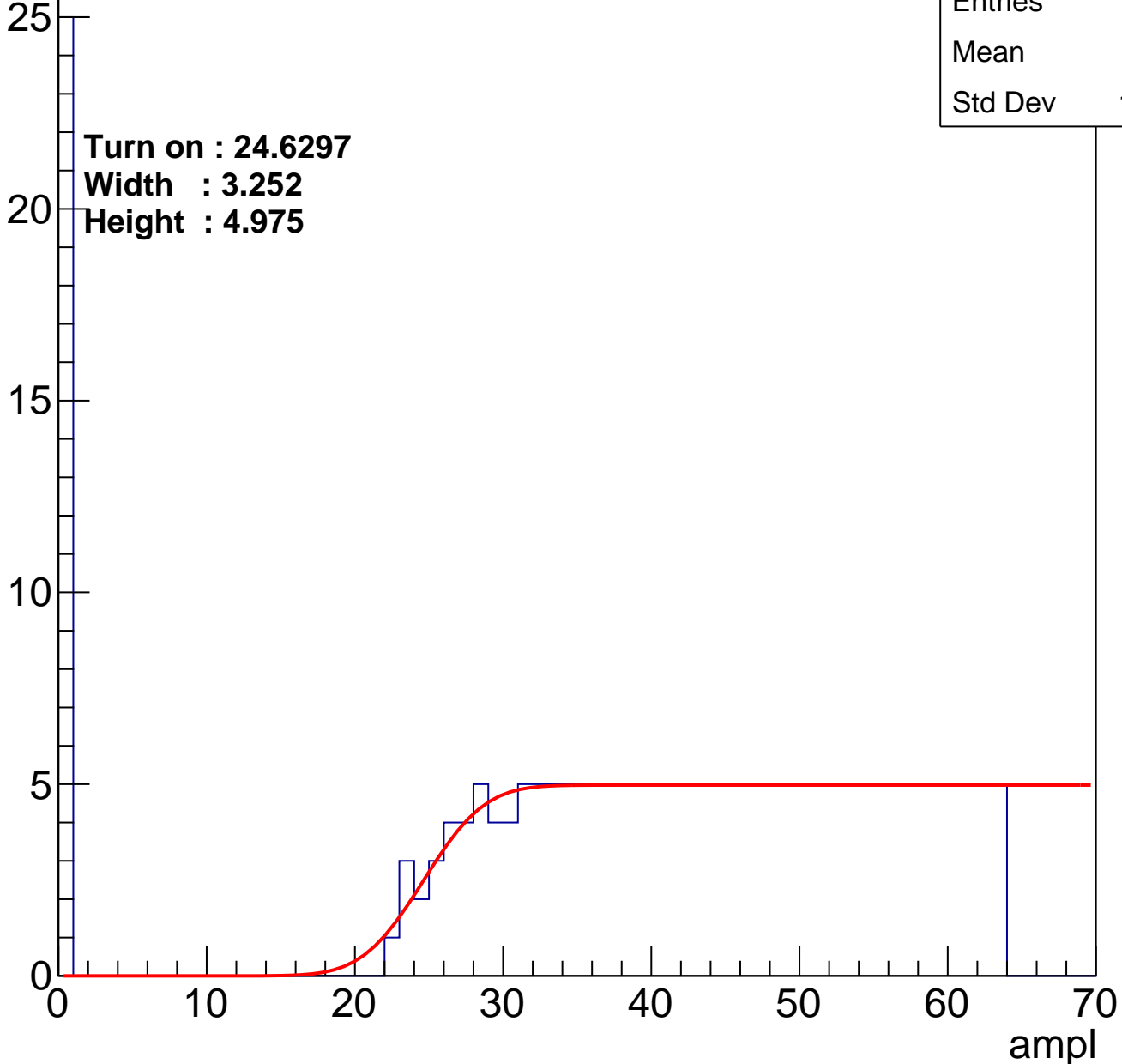
|         |       |
|---------|-------|
| Entries | 220   |
| Mean    | 38.9  |
| Std Dev | 17.61 |

**Turn on : 24.6297**

**Width : 3.252**

**Height : 4.975**

Entry



# B1L103S, U14-ch102

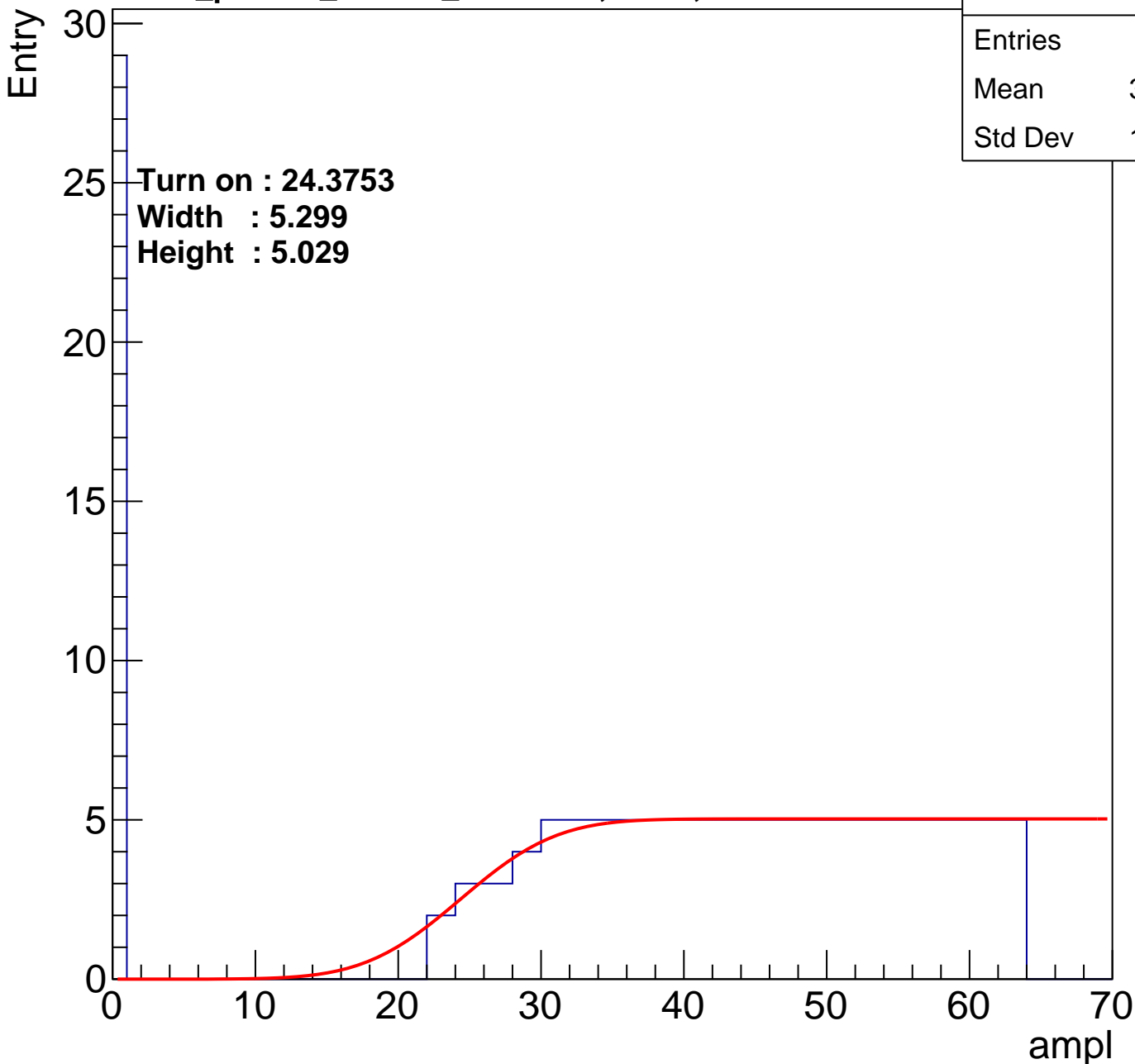
calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 223   |
| Mean    | 38.25 |
| Std Dev | 18.23 |

Turn on : 24.3753

Width : 5.299

Height : 5.029



# B1L103S, U14-ch103

calib\_packv5\_041523\_1651.root, FC#0, Port C2

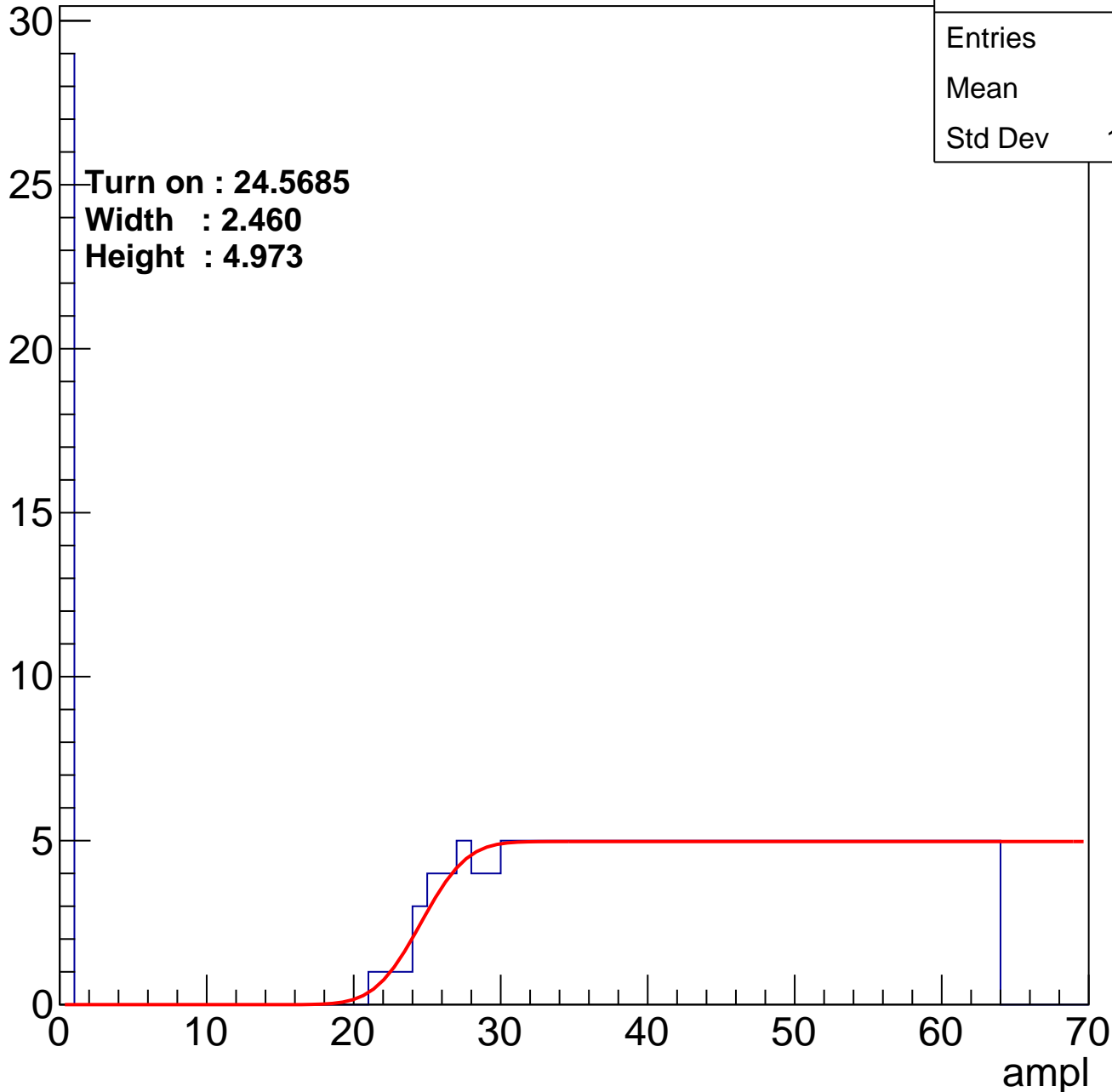
|         |       |
|---------|-------|
| Entries | 226   |
| Mean    | 38.1  |
| Std Dev | 18.15 |

Turn on : 24.5685

Width : 2.460

Height : 4.973

Entry





# B1L103S, U14-ch104

calib\_packv5\_041523\_1651.root, FC#0, Port C2

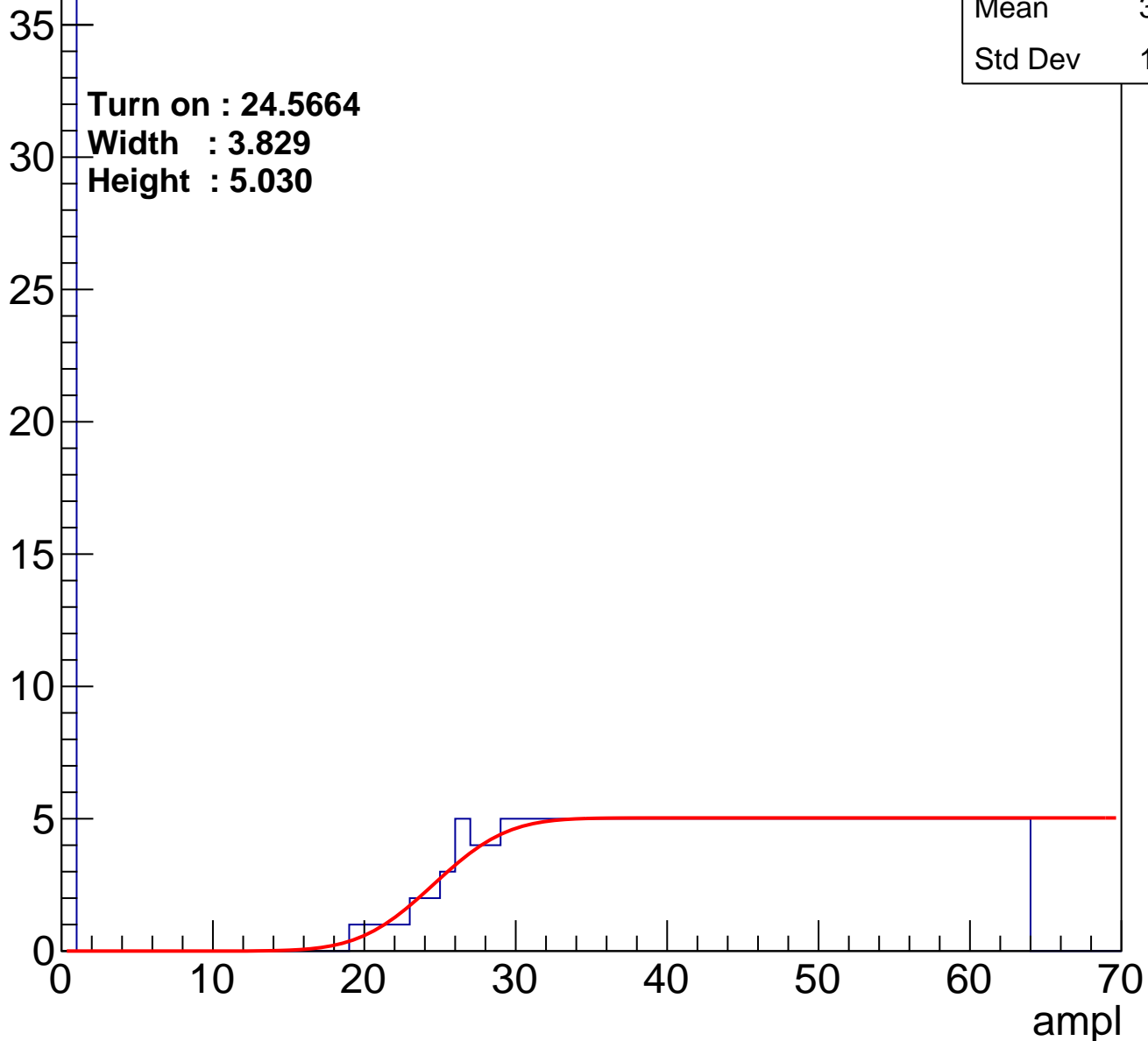
|         |       |
|---------|-------|
| Entries | 236   |
| Mean    | 36.66 |
| Std Dev | 19.12 |

**Turn on : 24.5664**

**Width : 3.829**

**Height : 5.030**

Entry



# B1L103S, U14-ch105

calib\_packv5\_041523\_1651.root, FC#0, Port C2

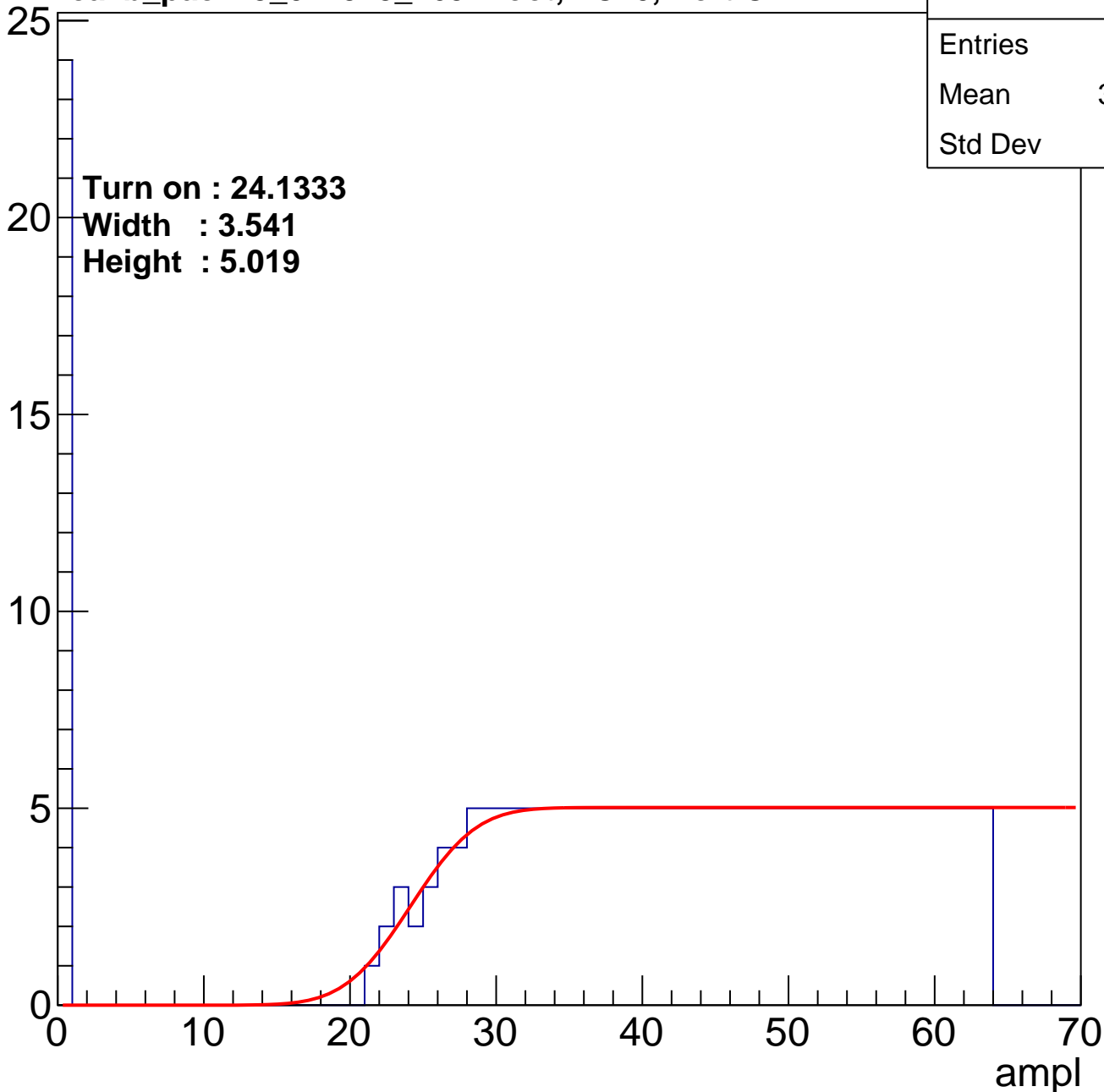
|         |       |
|---------|-------|
| Entries | 223   |
| Mean    | 38.83 |
| Std Dev | 17.4  |

Turn on : 24.1333

Width : 3.541

Height : 5.019

Entry

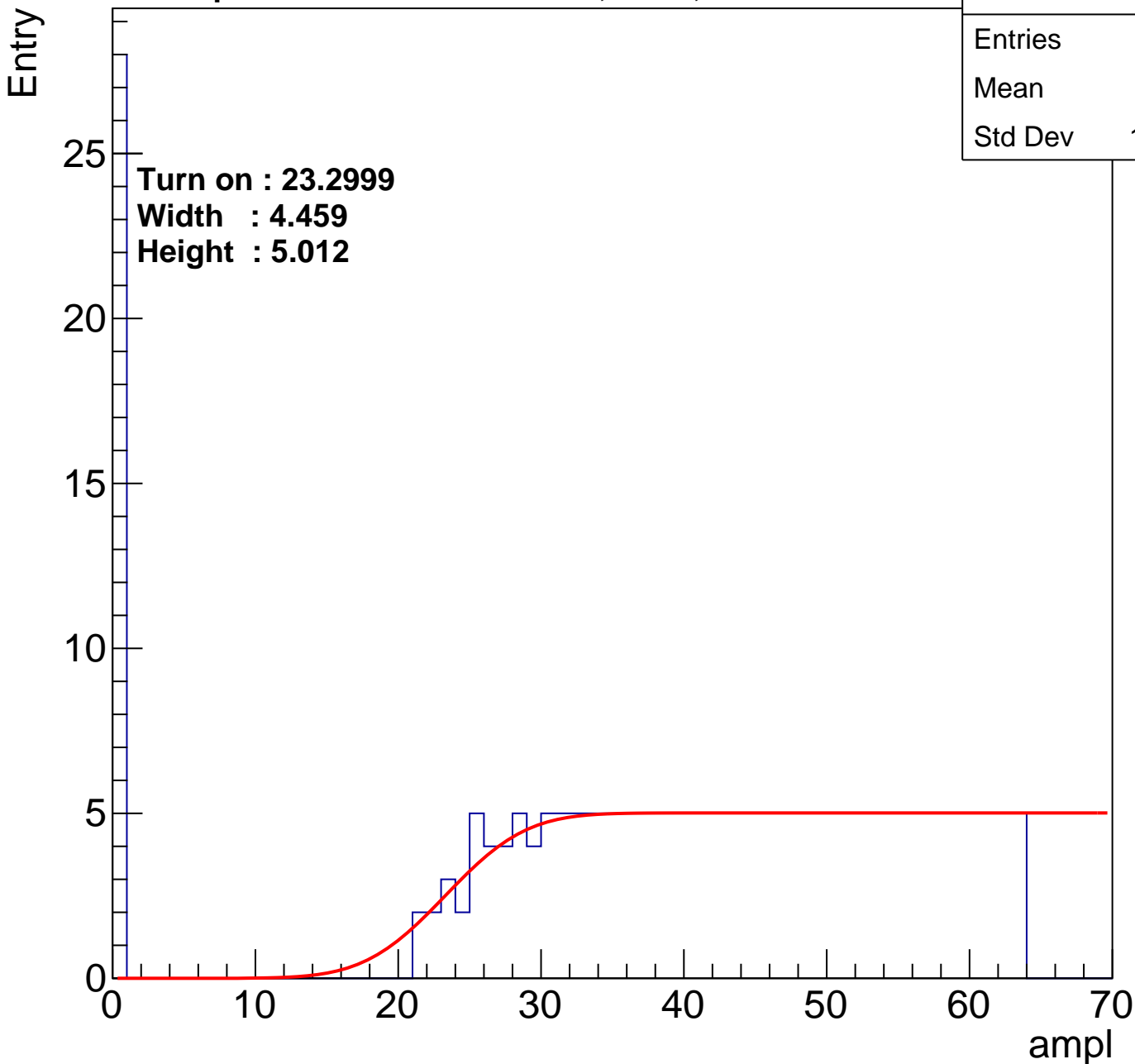


# B1L103S, U14-ch106

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 229   |
| Mean    | 38    |
| Std Dev | 17.97 |

**Turn on : 23.2999**  
**Width : 4.459**  
**Height : 5.012**



# B1L103S, U14-ch107

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 221   |
| Mean    | 38.52 |
| Std Dev | 18.08 |

**Turn on : 25.8430**  
**Width : 3.618**  
**Height : 5.040**

Entry

25

20

15

10

5

0

ampl

0

10

20

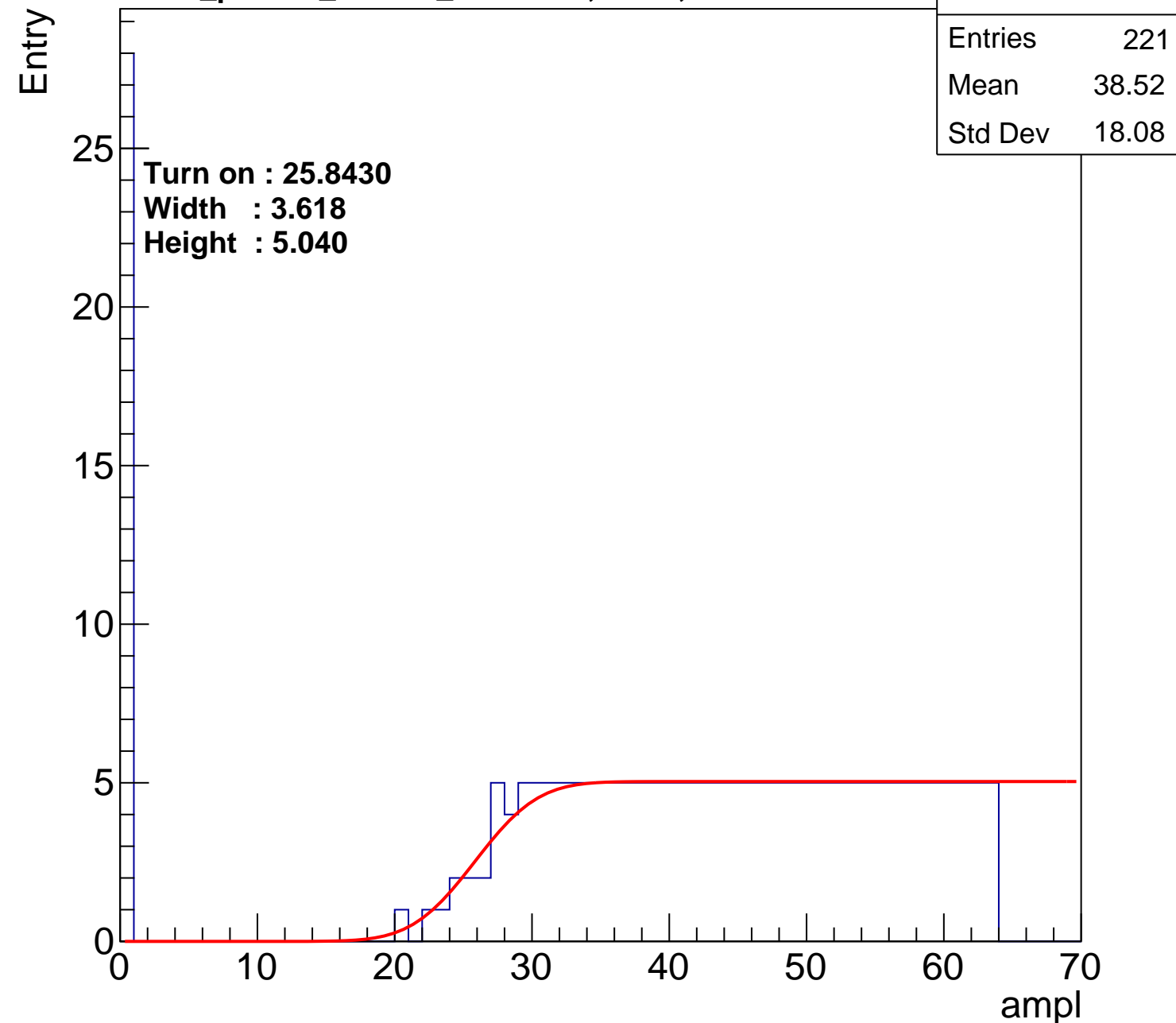
30

40

50

60

70



# B1L103S, U14-ch108

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 230   |
| Mean    | 38.14 |
| Std Dev | 17.65 |

**Turn on : 22.8541**

**Width : 2.078**

**Height : 4.943**

Entry

25

20

15

10

5

0

0

10

20

30

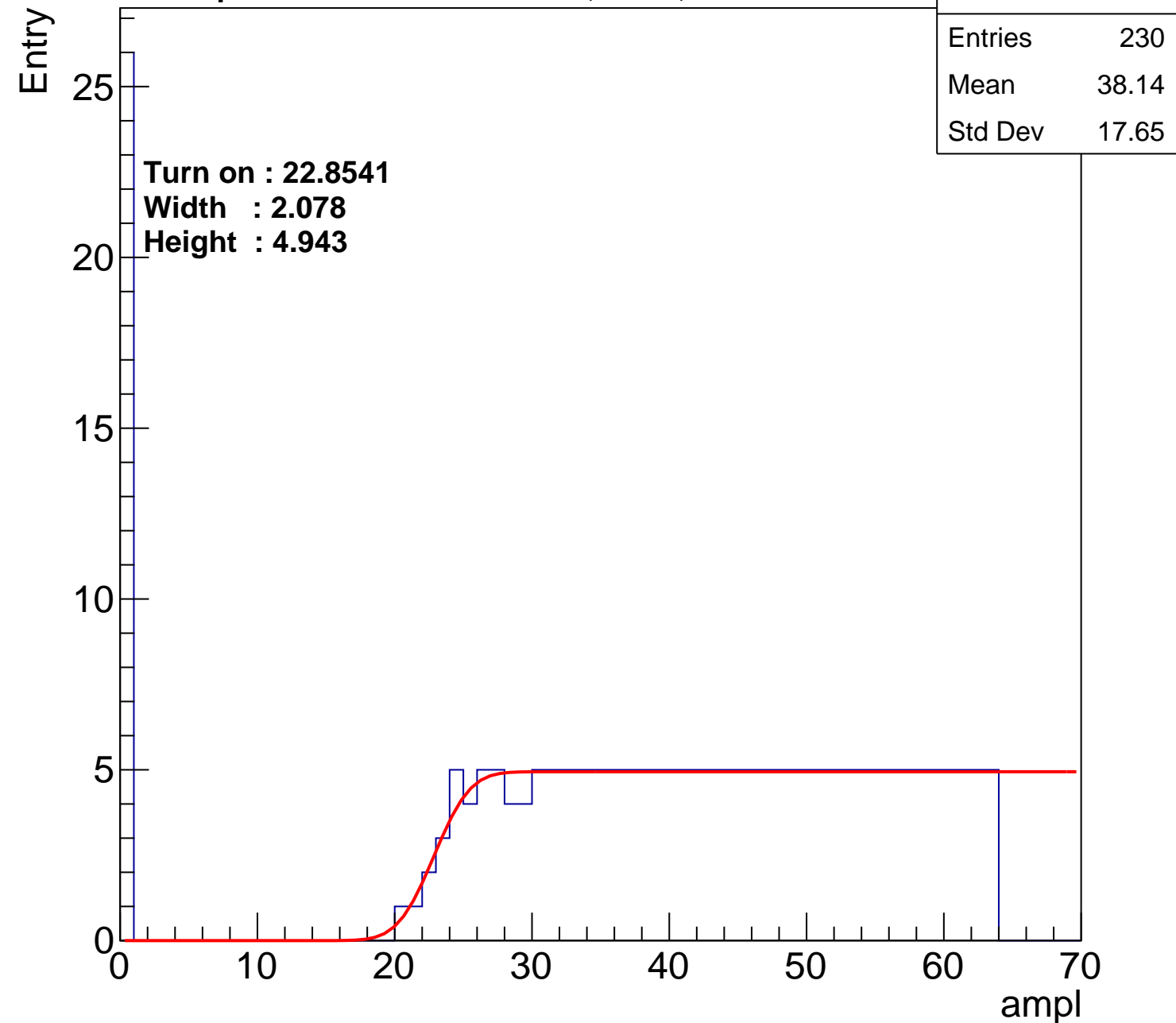
40

50

60

70

ampl



# B1L103S, U14-ch109

calib\_packv5\_041523\_1651.root, FC#0, Port C2

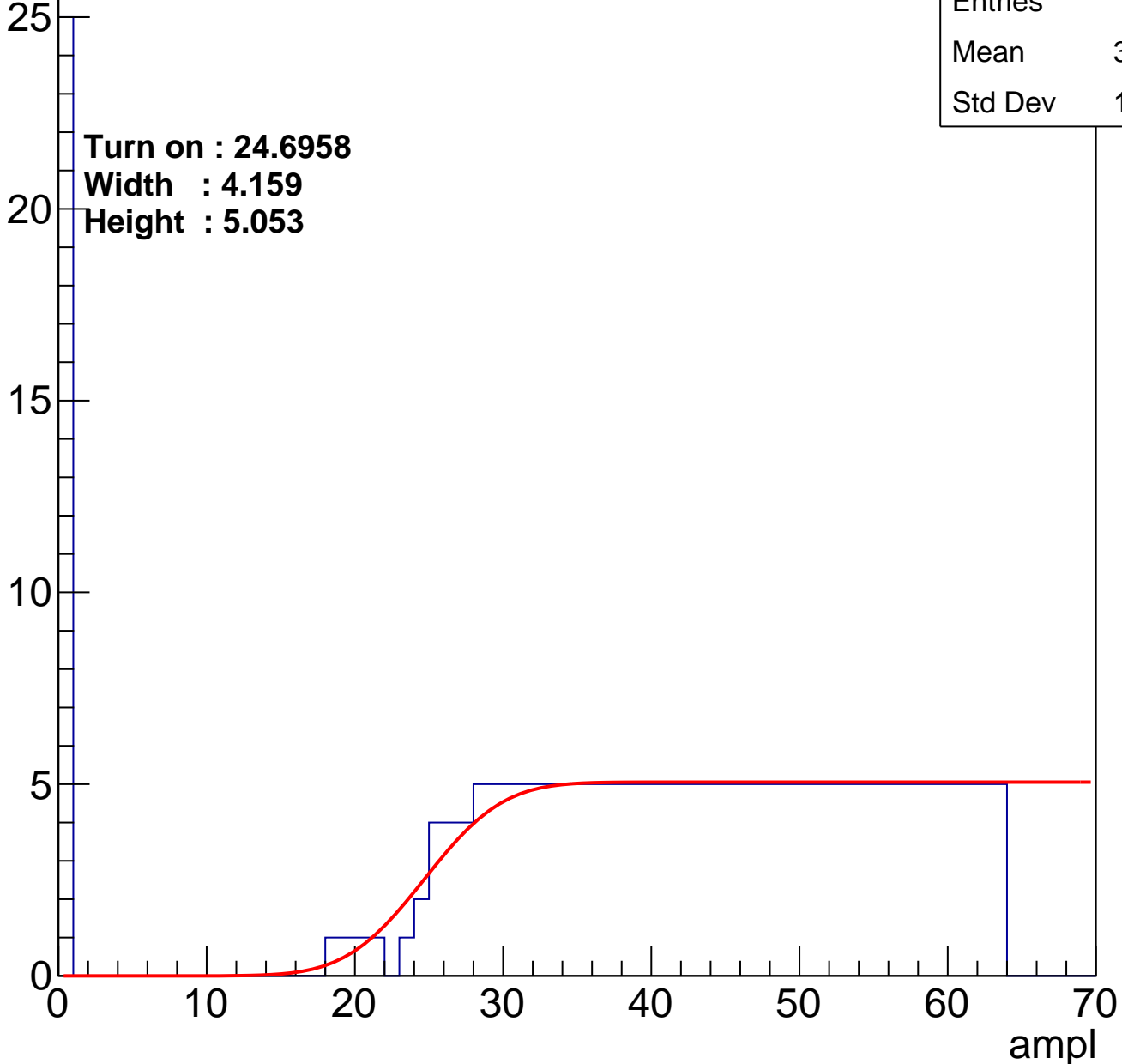
|         |       |
|---------|-------|
| Entries | 224   |
| Mean    | 38.62 |
| Std Dev | 17.59 |

**Turn on : 24.6958**

**Width : 4.159**

**Height : 5.053**

Entry

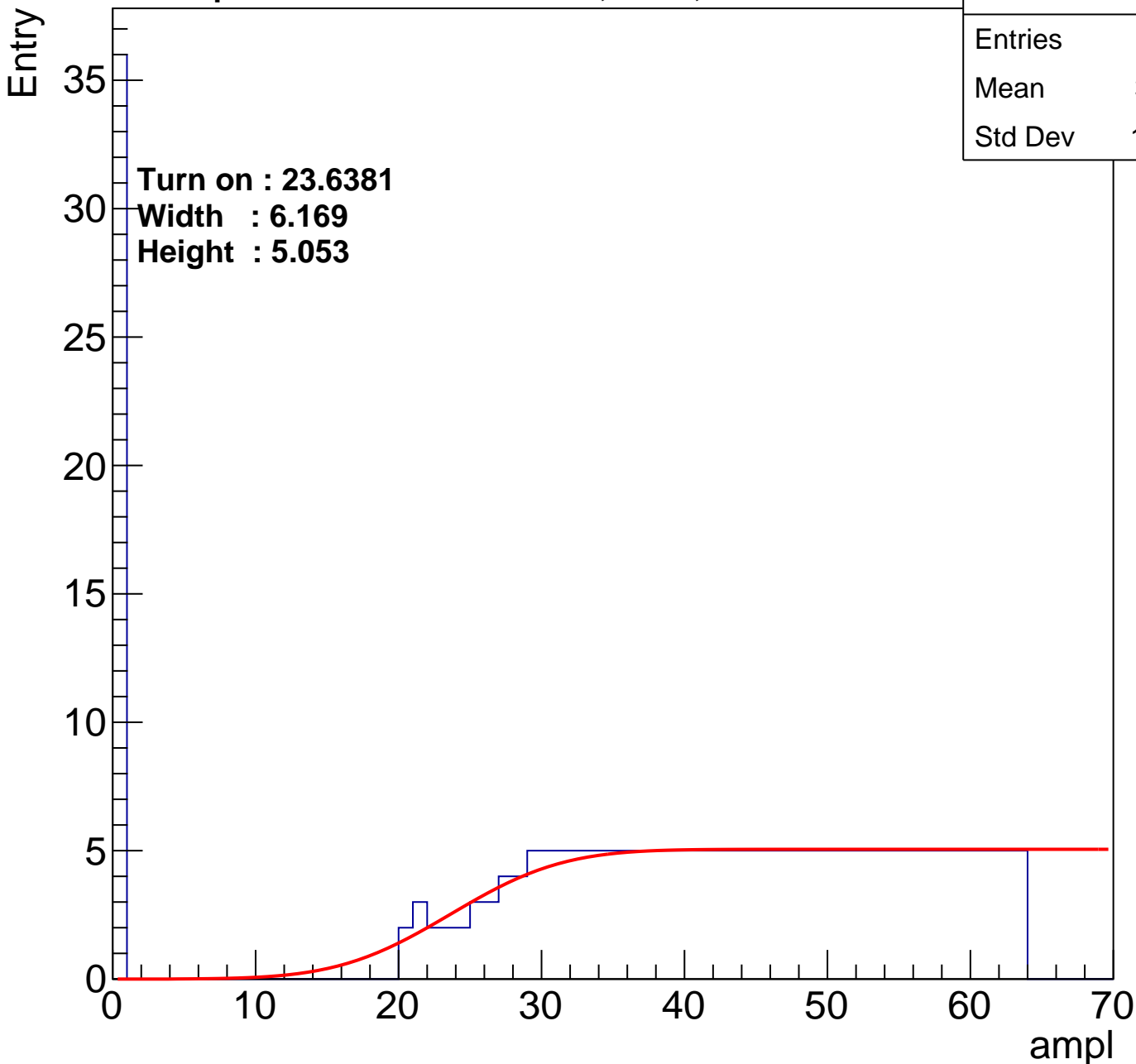


# B1L103S, U14-ch110

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 236   |
| Mean    | 36.71 |
| Std Dev | 19.02 |

Turn on : 23.6381  
Width : 6.169  
Height : 5.053



# B1L103S, U14-ch111

calib\_packv5\_041523\_1651.root, FC#0, Port C2

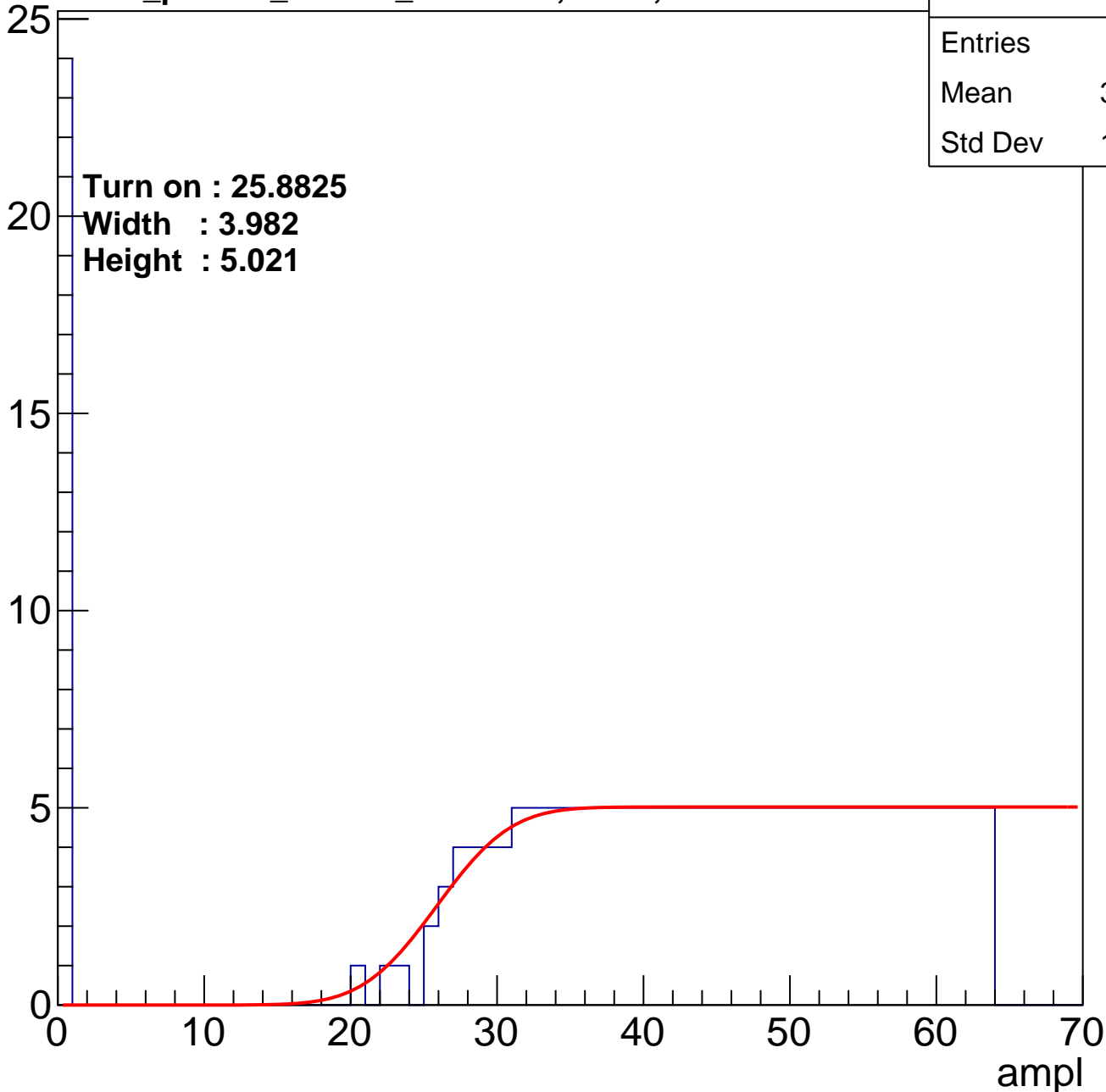
|         |       |
|---------|-------|
| Entries | 213   |
| Mean    | 39.46 |
| Std Dev | 17.55 |

Turn on : 25.8825

Width : 3.982

Height : 5.021

Entry





# B1L103S, U14-ch112

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 227   |
| Mean    | 38.37 |
| Std Dev | 17.89 |

**Turn on : 24.7522**

**Width : 4.135**

**Height : 5.060**

Entry

25

20

15

10

5

0

0

10

20

30

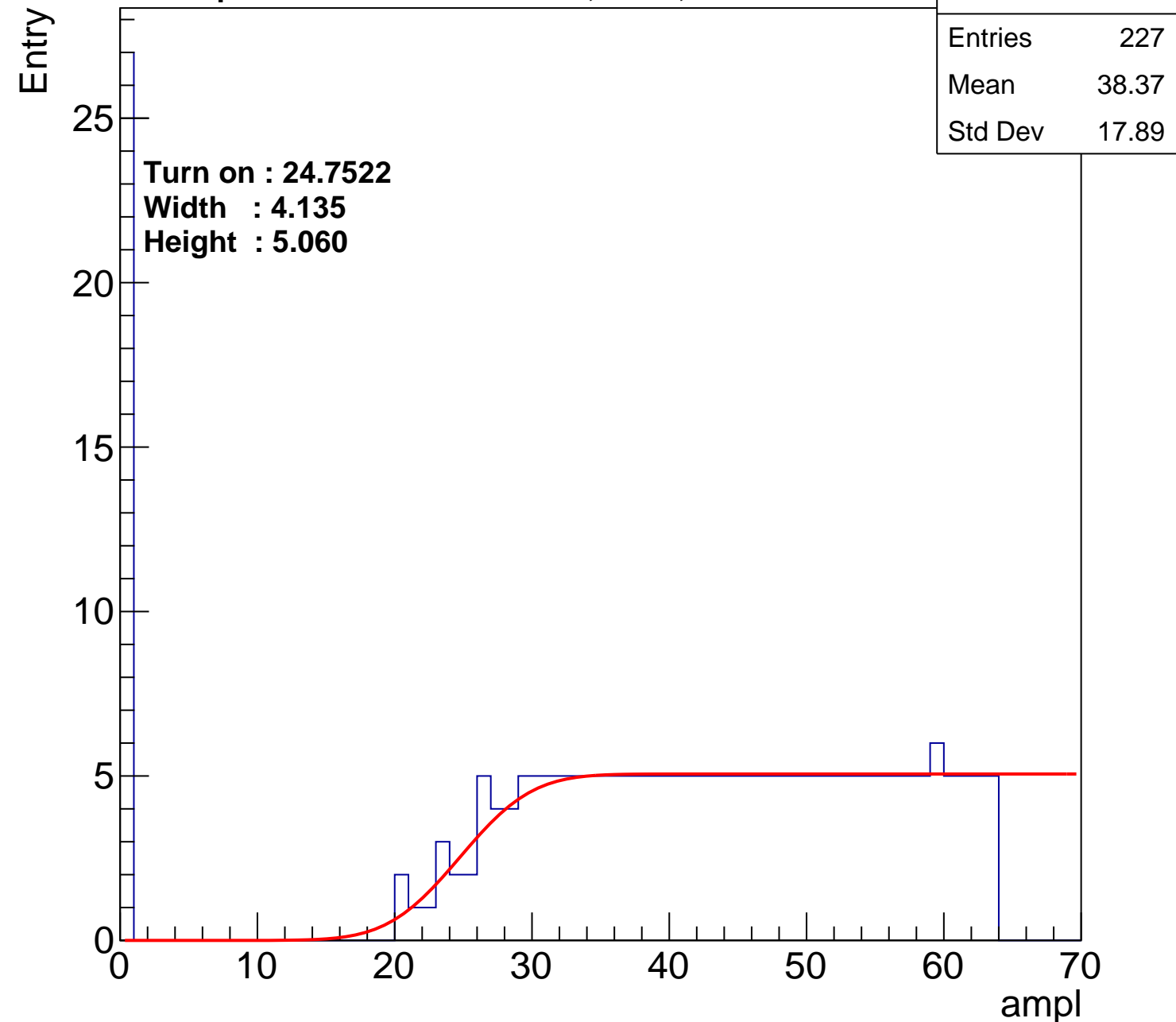
40

50

60

70

ampl



# B1L103S, U14-ch113

calib\_packv5\_041523\_1651.root, FC#0, Port C2

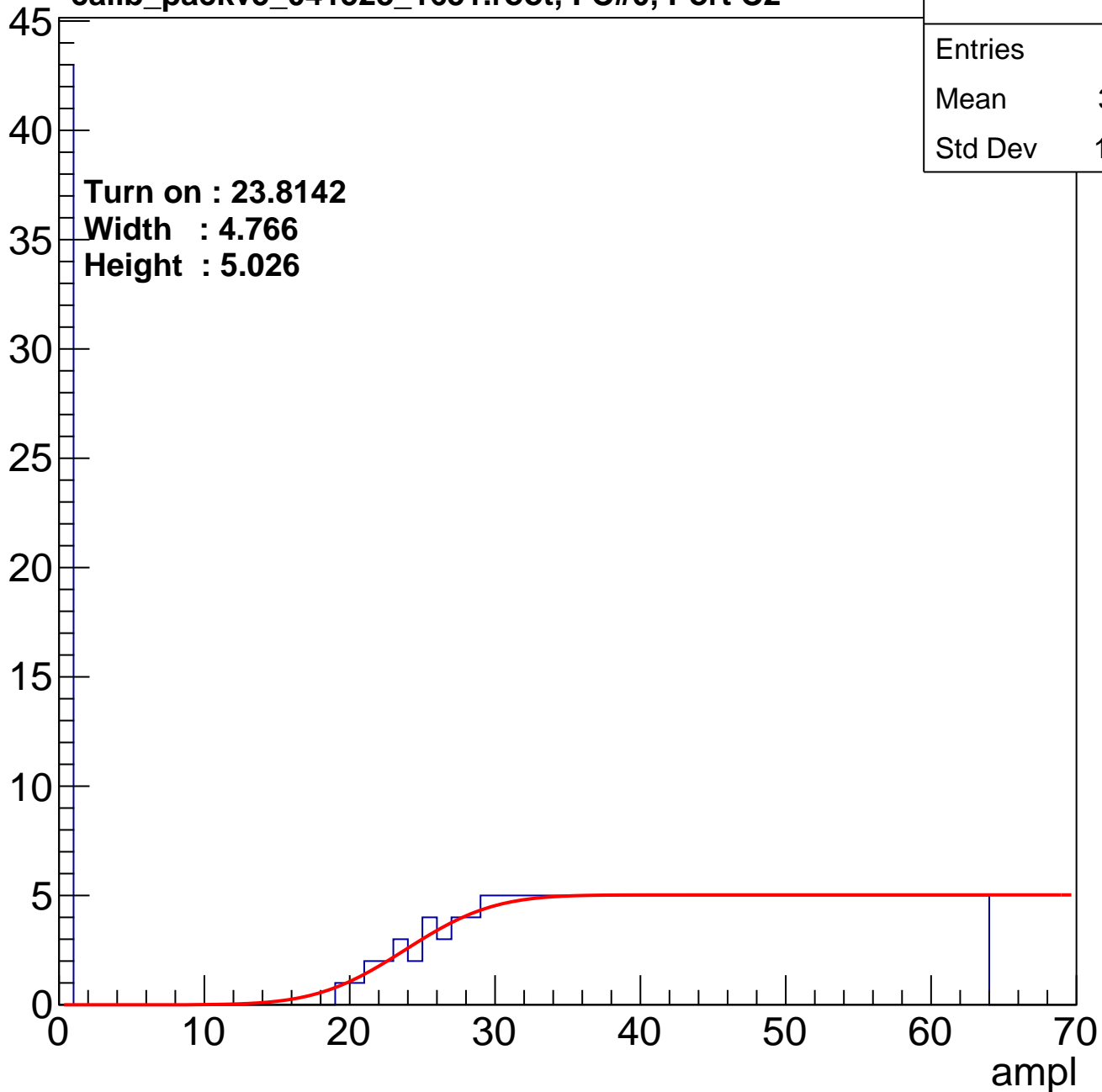
|         |       |
|---------|-------|
| Entries | 244   |
| Mean    | 35.61 |
| Std Dev | 19.69 |

**Turn on : 23.8142**

**Width : 4.766**

**Height : 5.026**

Entry



# B1L103S, U14-ch114

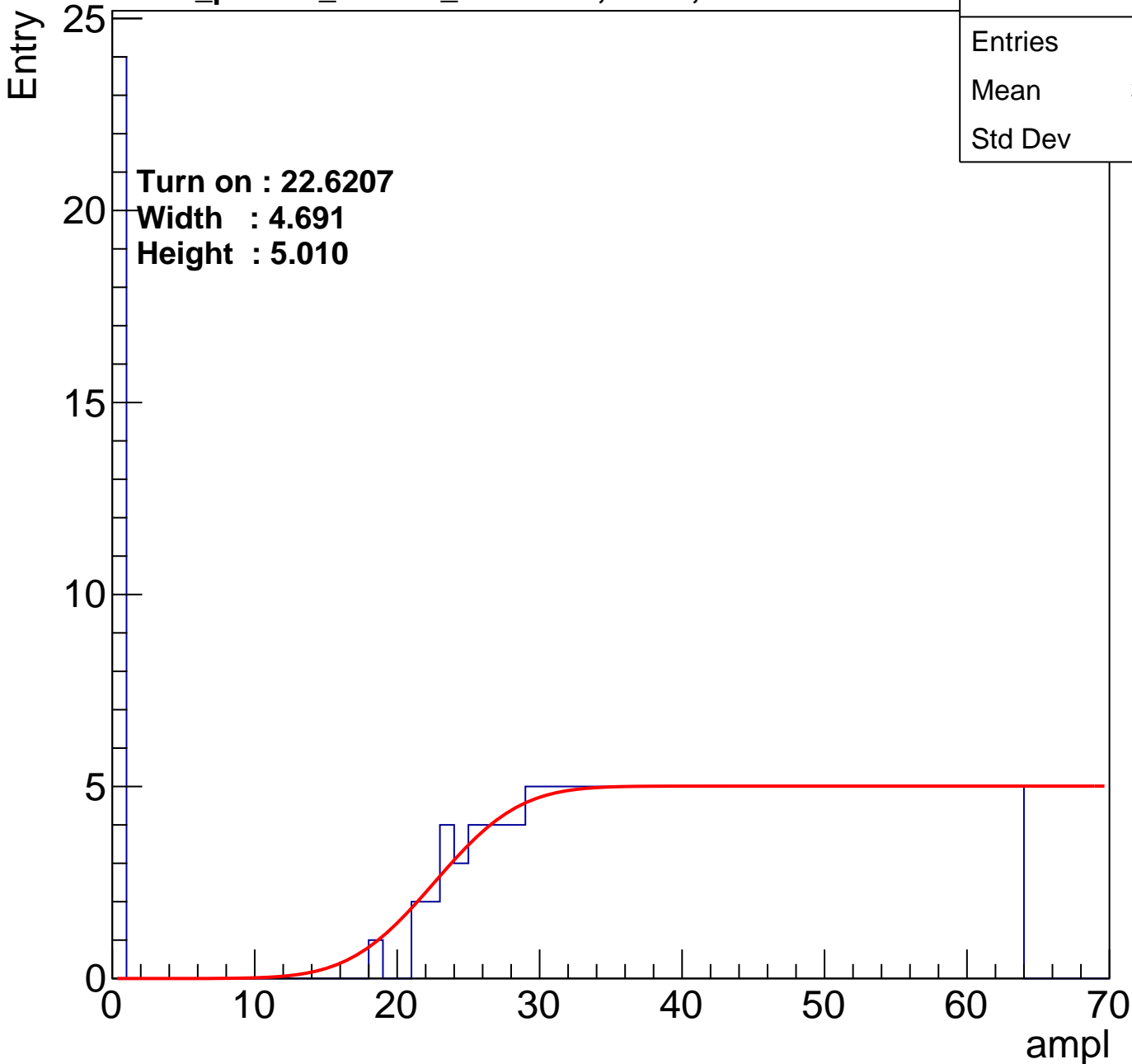
calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 227   |
| Mean    | 38.51 |
| Std Dev | 17.4  |

Turn on : 22.6207

Width : 4.691

Height : 5.010



# B1L103S, U14-ch115

calib\_packv5\_041523\_1651.root, FC#0, Port C2

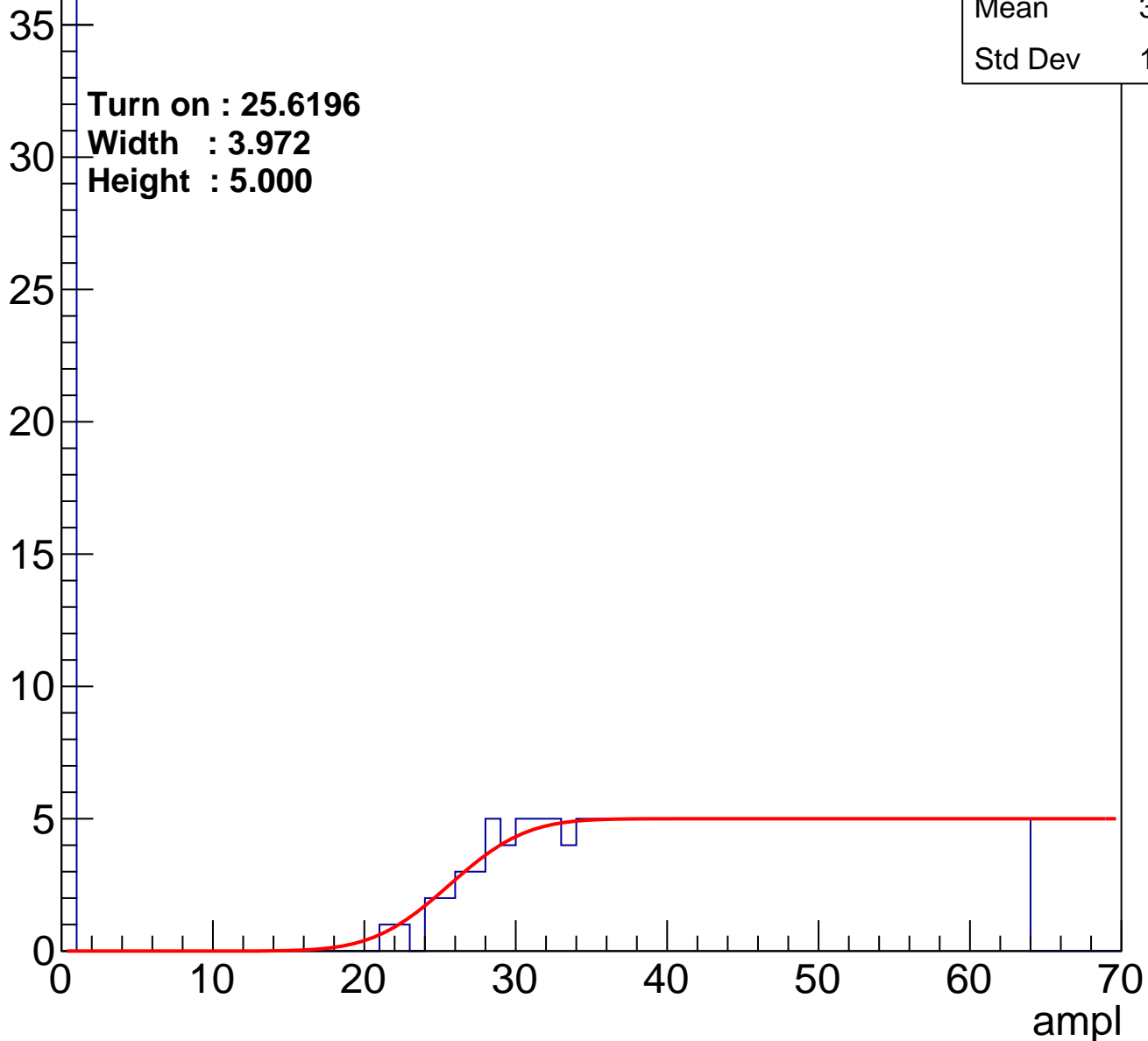
|         |       |
|---------|-------|
| Entries | 227   |
| Mean    | 37.13 |
| Std Dev | 19.32 |

**Turn on : 25.6196**

**Width : 3.972**

**Height : 5.000**

Entry



# B1L103S, U14-ch116

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 228   |
| Mean    | 37.78 |
| Std Dev | 18.41 |

**Turn on : 24.8199**

**Width : 2.787**

**Height : 5.021**

Entry

30

25

20

15

10

5

0

0

10

20

30

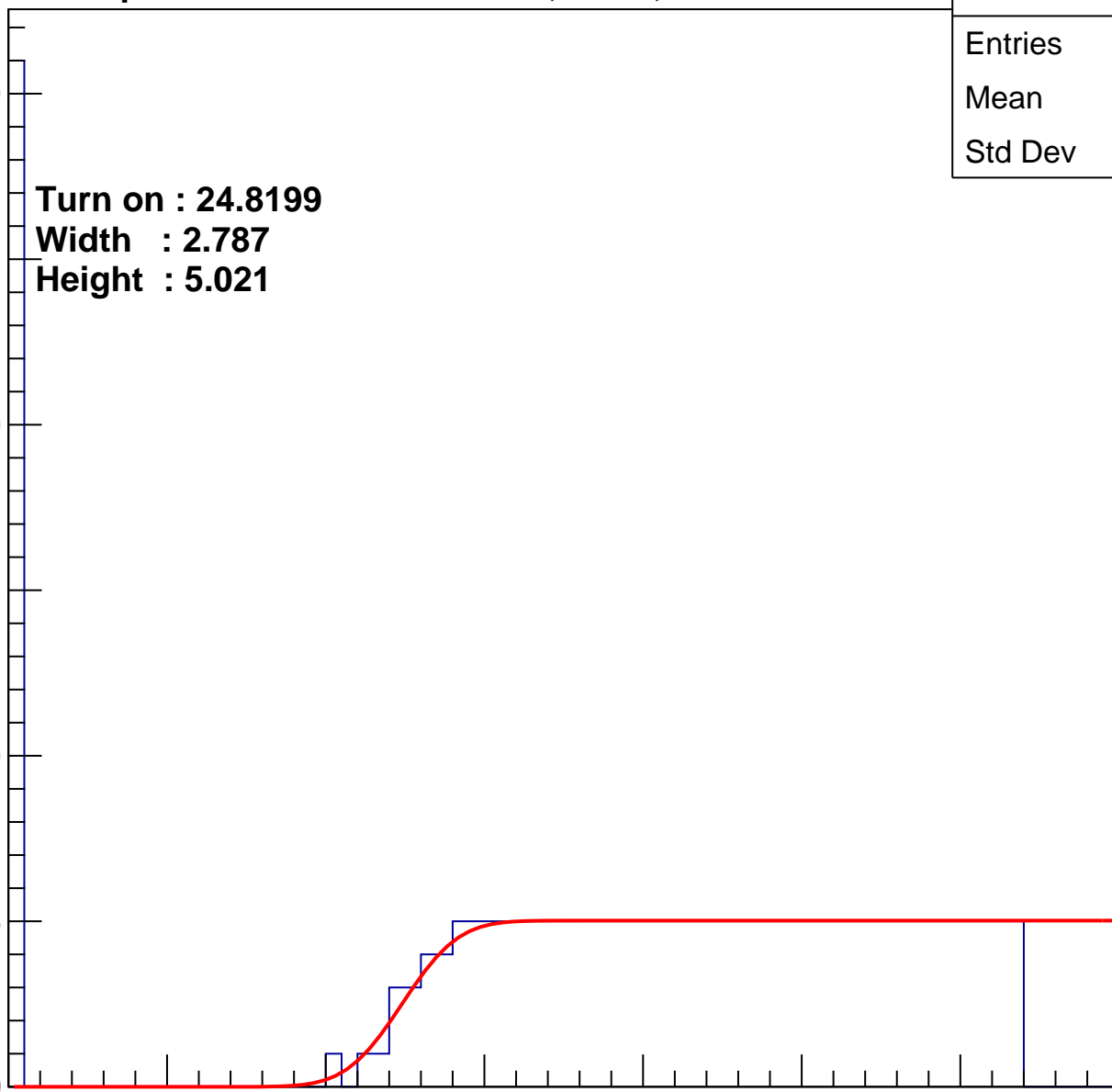
40

50

60

70

ampl



# B1L103S, U14-ch117

calib\_packv5\_041523\_1651.root, FC#0, Port C2

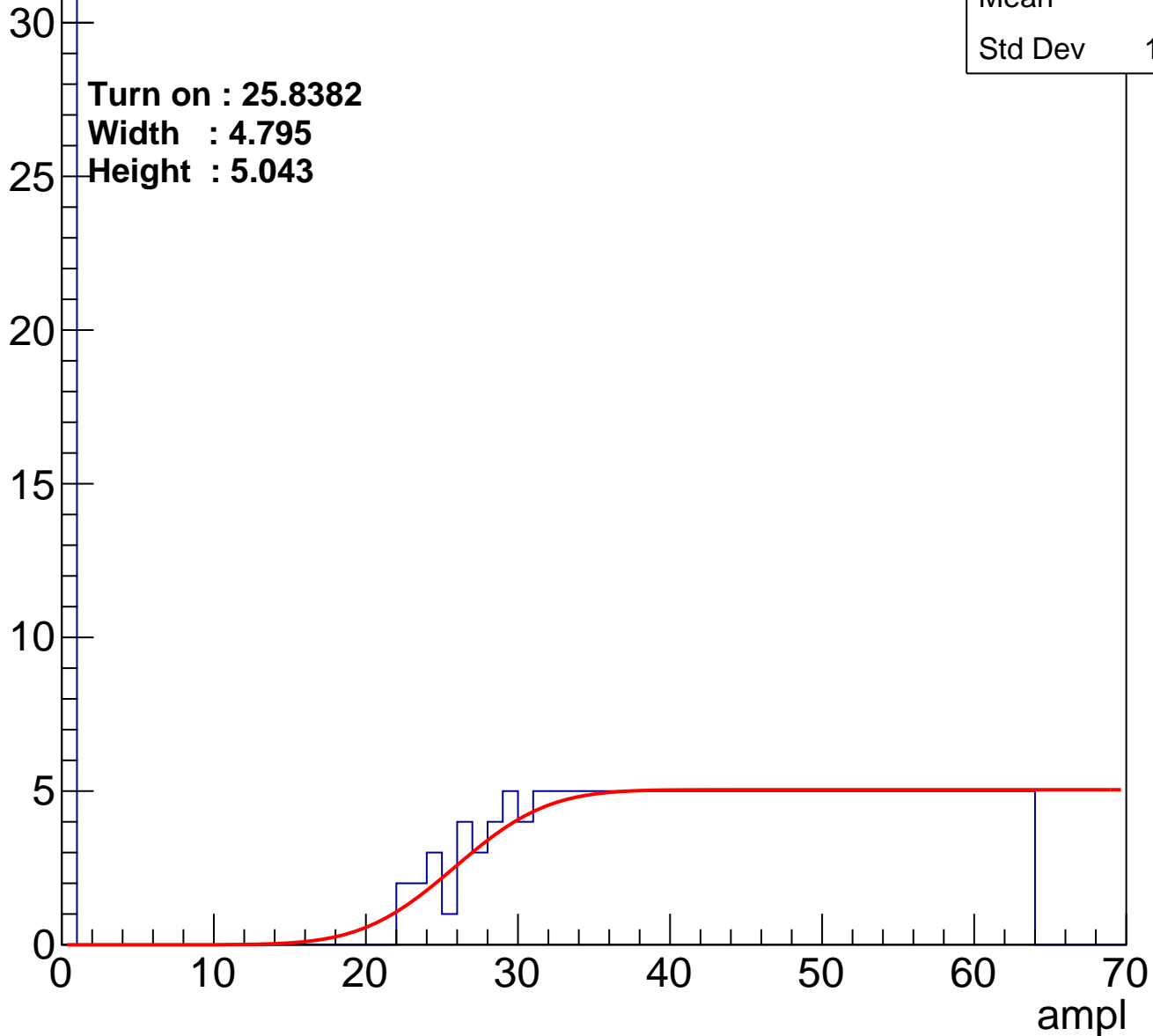
|         |       |
|---------|-------|
| Entries | 225   |
| Mean    | 37.8  |
| Std Dev | 18.65 |

**Turn on : 25.8382**

**Width : 4.795**

**Height : 5.043**

Entry



# B1L103S, U14-ch118

calib\_packv5\_041523\_1651.root, FC#0, Port C2

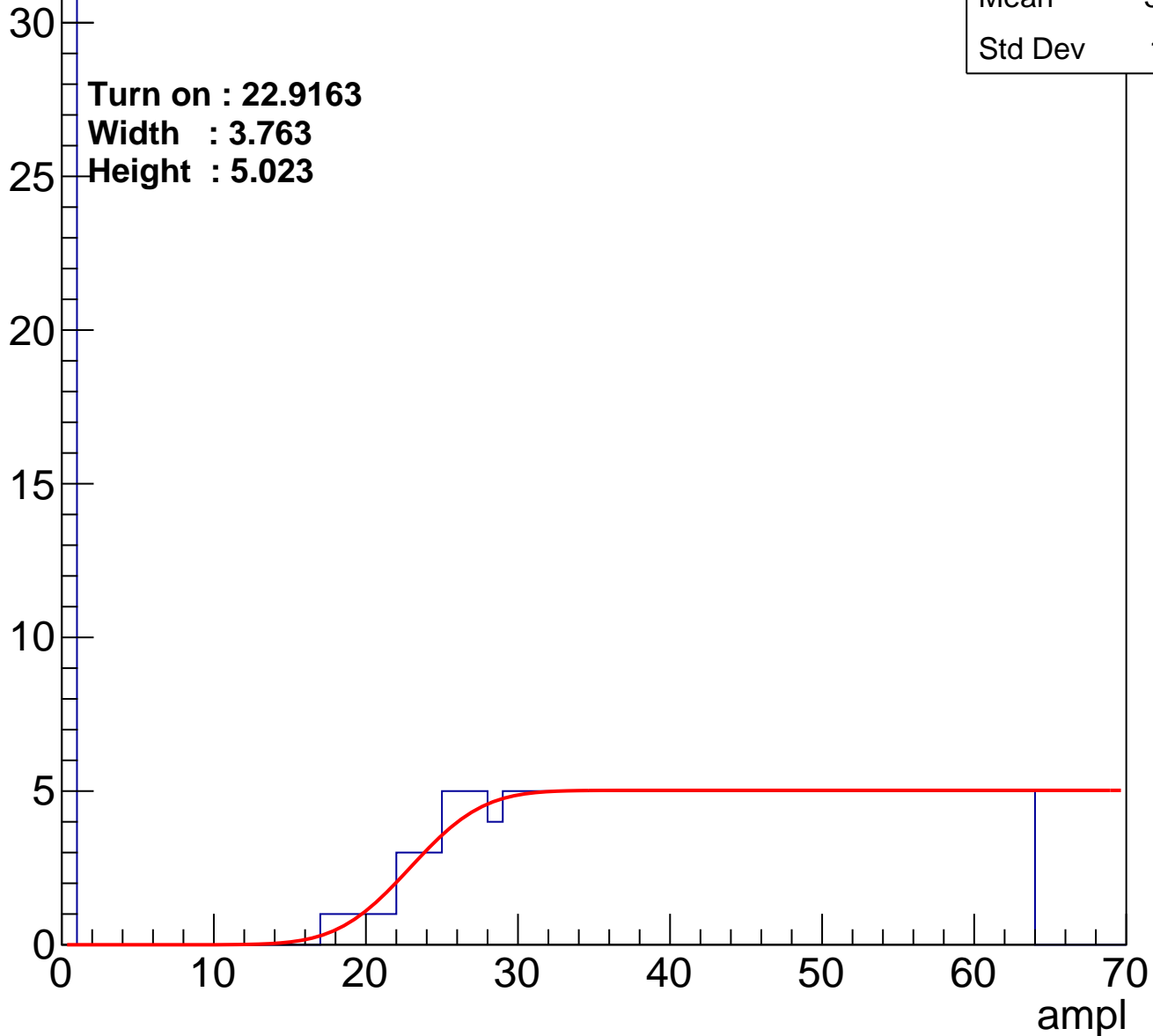
|         |       |
|---------|-------|
| Entries | 240   |
| Mean    | 36.89 |
| Std Dev | 18.41 |

**Turn on : 22.9163**

**Width : 3.763**

**Height : 5.023**

Entry



# B1L103S, U14-ch119

calib\_packv5\_041523\_1651.root, FC#0, Port C2

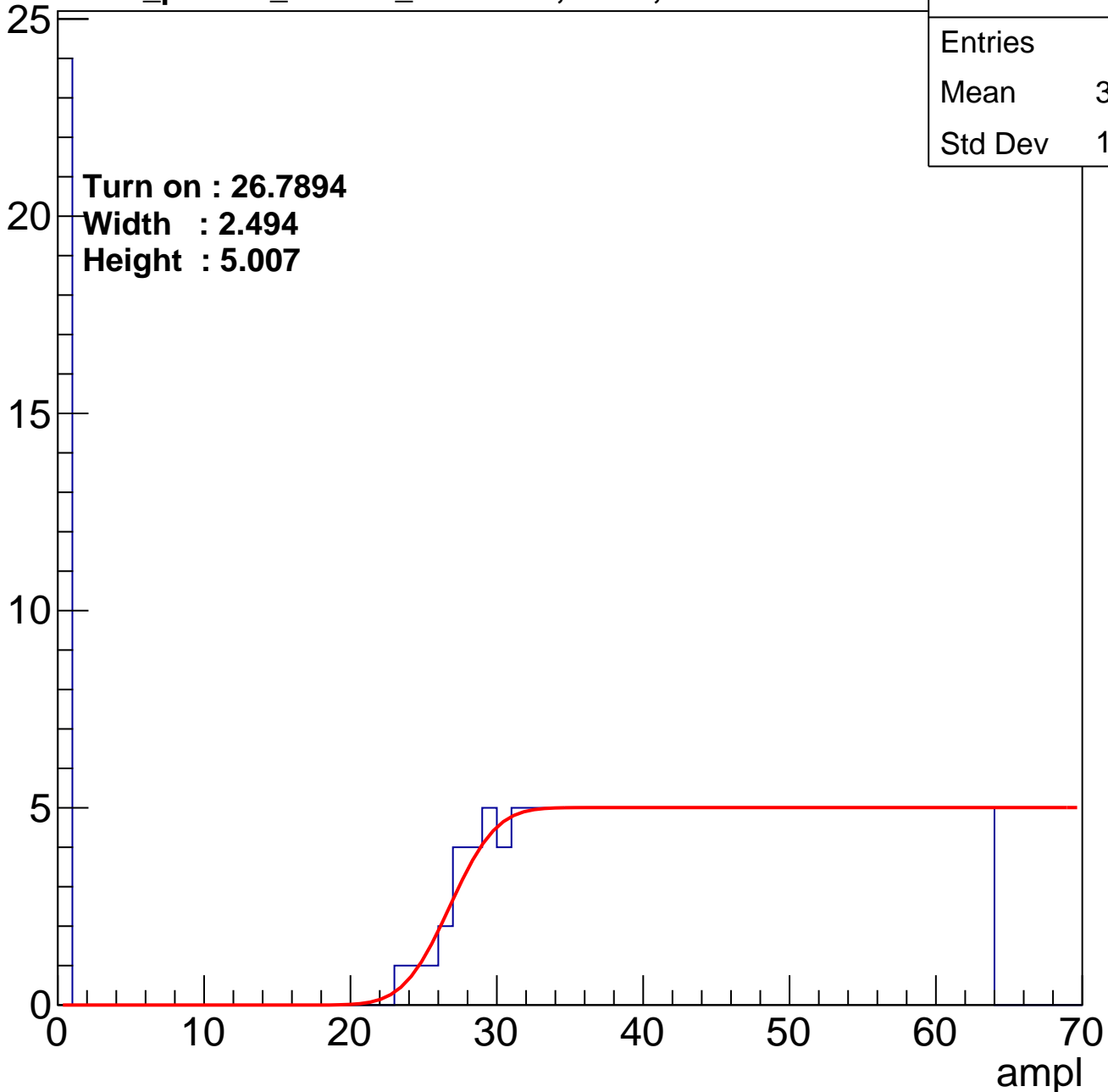
|         |       |
|---------|-------|
| Entries | 211   |
| Mean    | 39.64 |
| Std Dev | 17.53 |

Turn on : 26.7894

Width : 2.494

Height : 5.007

Entry





# B1L103S, U14-ch120

calib\_packv5\_041523\_1651.root, FC#0, Port C2

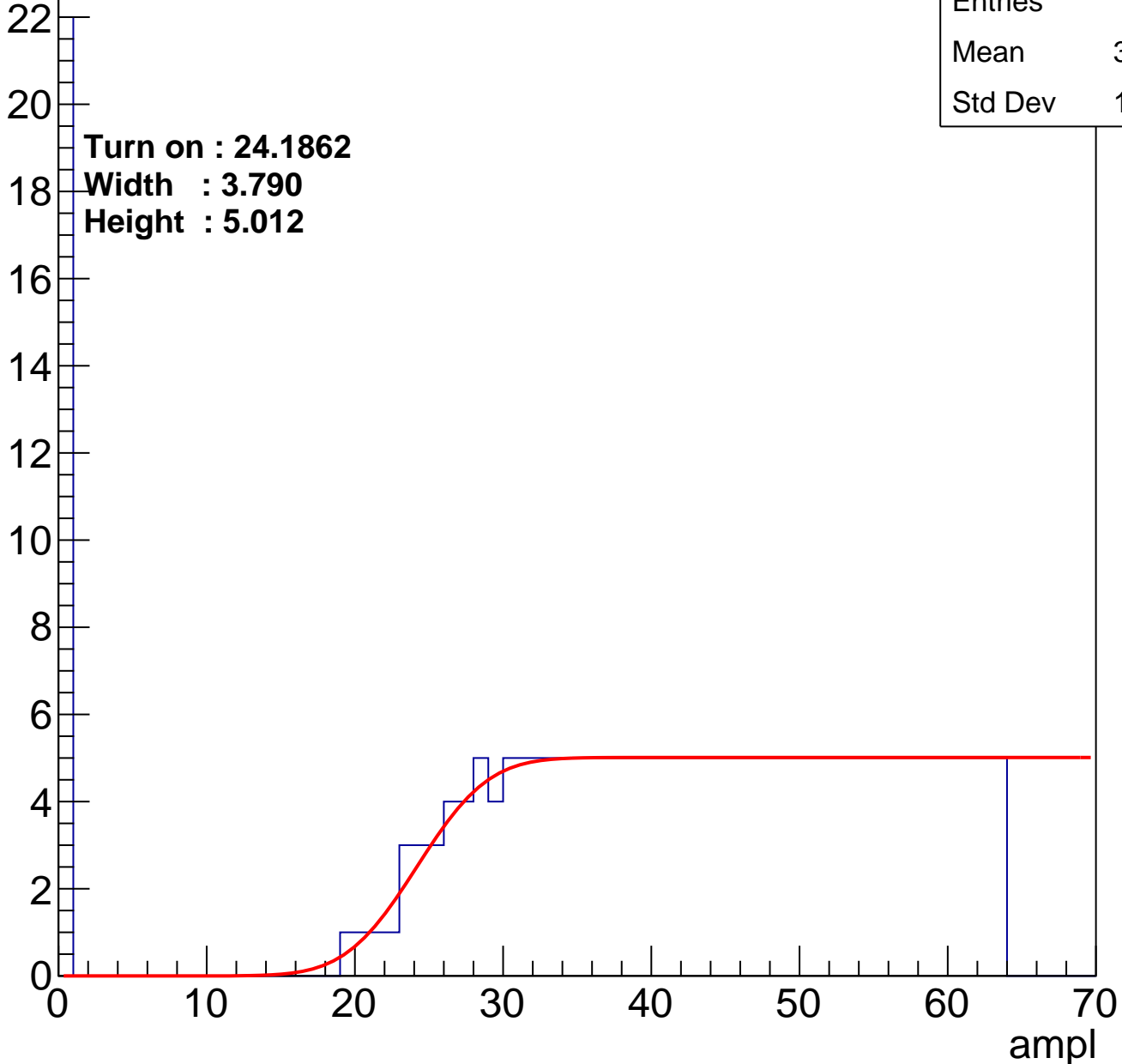
|         |       |
|---------|-------|
| Entries | 222   |
| Mean    | 39.06 |
| Std Dev | 17.12 |

**Turn on : 24.1862**

**Width : 3.790**

**Height : 5.012**

Entry



# B1L103S, U14-ch121

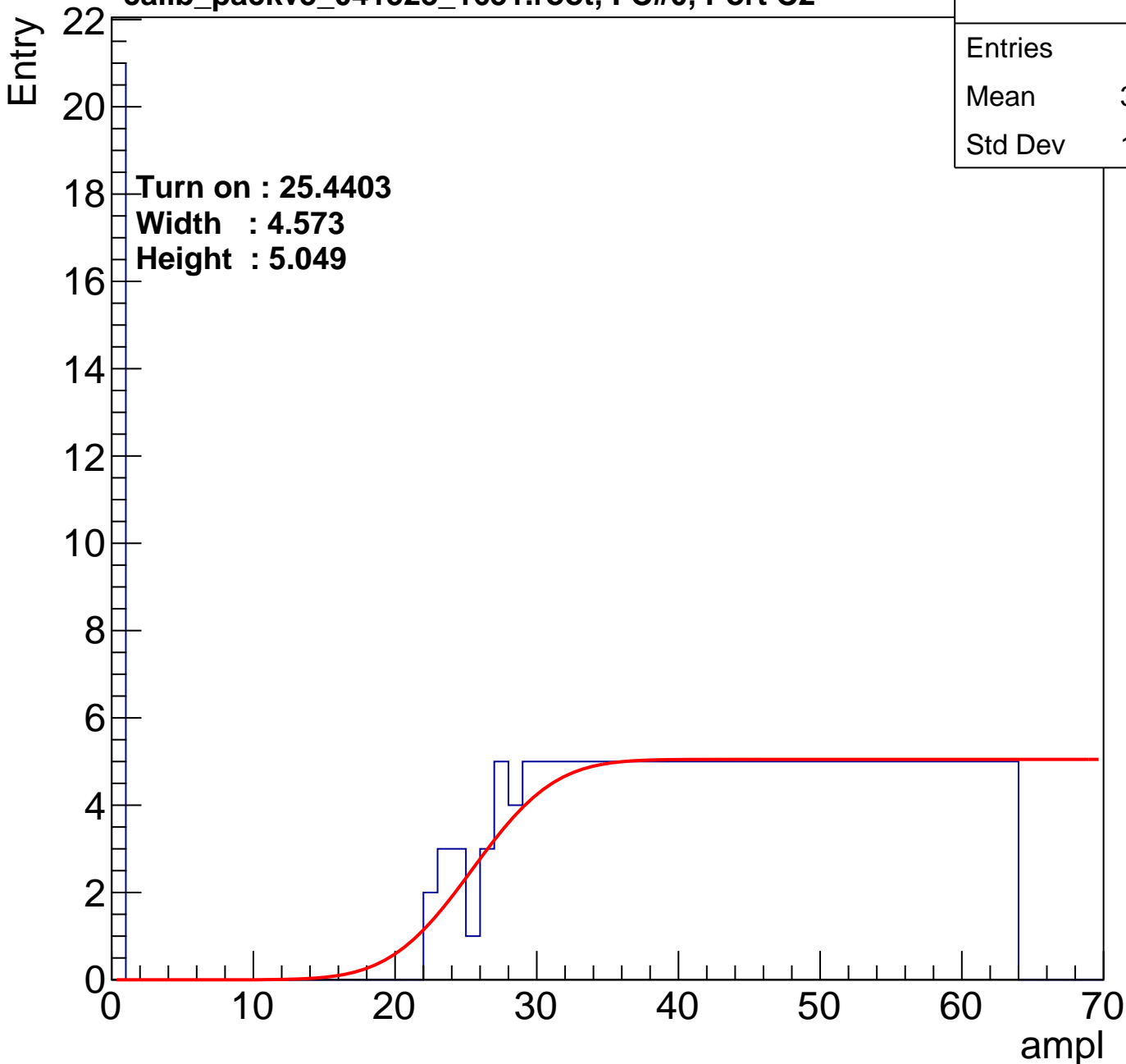
calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 217   |
| Mean    | 39.56 |
| Std Dev | 16.93 |

Turn on : 25.4403

Width : 4.573

Height : 5.049



# B1L103S, U14-ch122

calib\_packv5\_041523\_1651.root, FC#0, Port C2

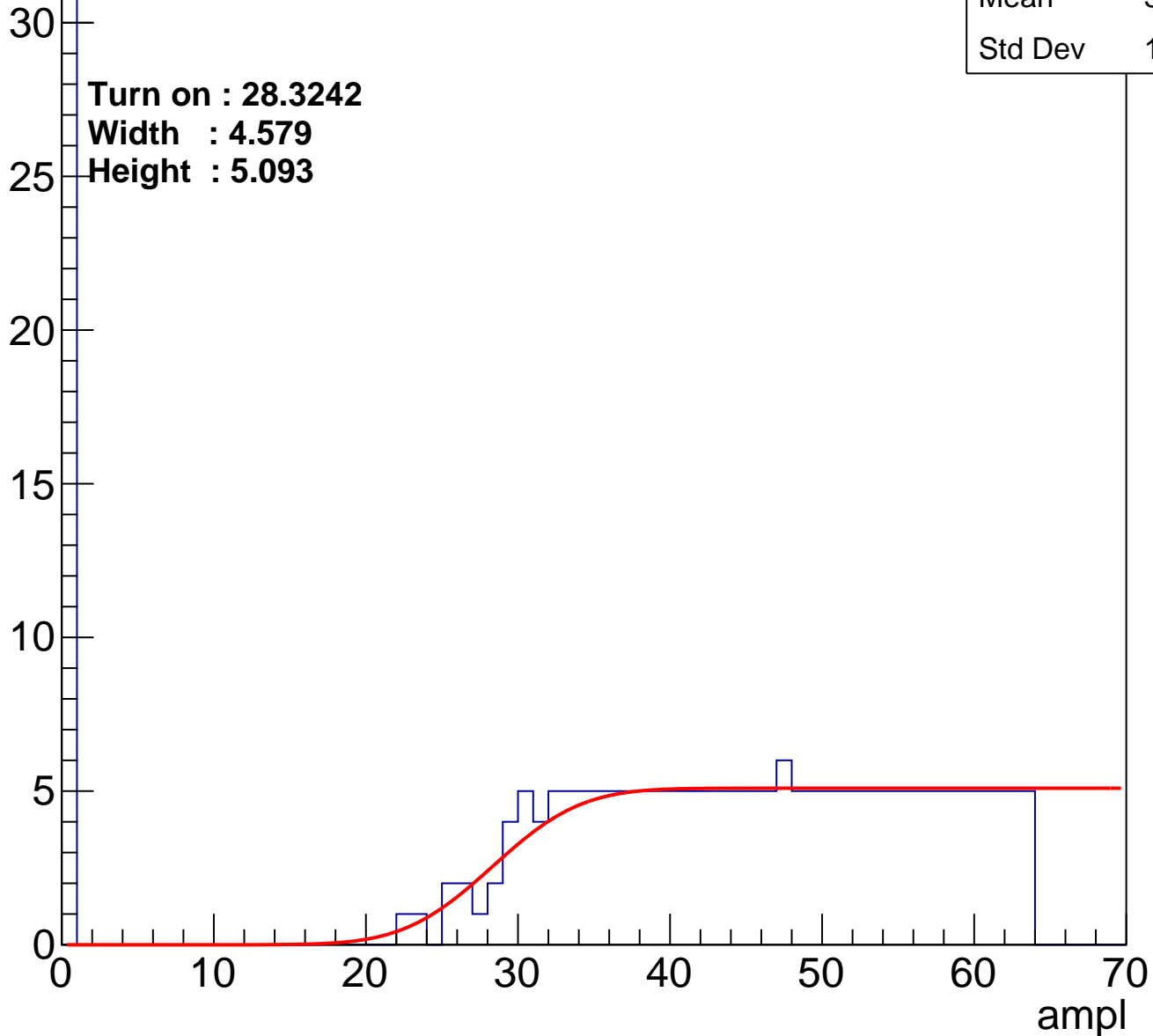
|         |       |
|---------|-------|
| Entries | 215   |
| Mean    | 38.45 |
| Std Dev | 18.87 |

**Turn on : 28.3242**

**Width : 4.579**

**Height : 5.093**

Entry



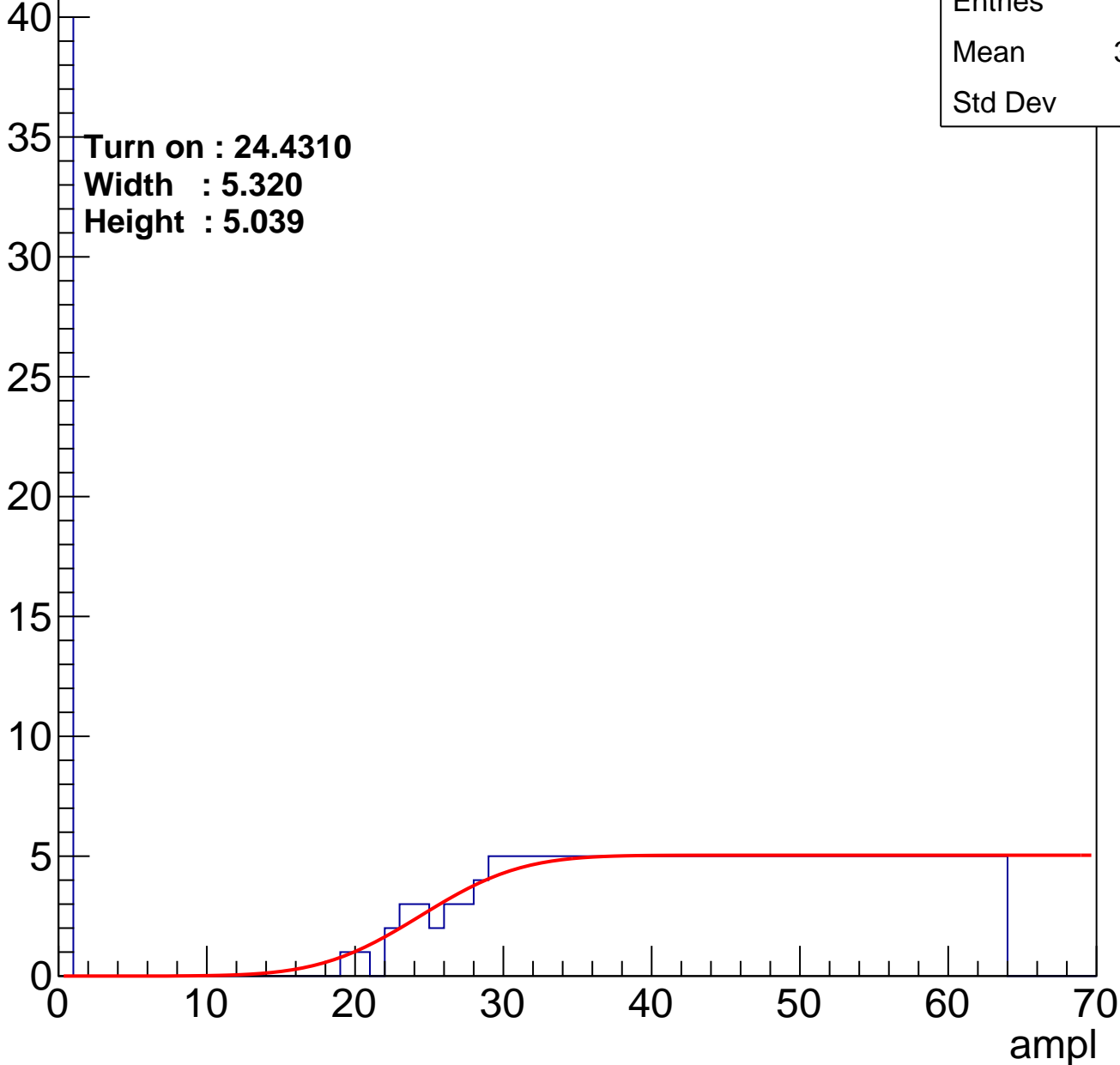
# B1L103S, U14-ch123

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 237   |
| Mean    | 36.27 |
| Std Dev | 19.5  |

Turn on : 24.4310  
Width : 5.320  
Height : 5.039

Entry



# B1L103S, U14-ch124

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 239   |
| Mean    | 36.39 |
| Std Dev | 19.18 |

**Turn on : 23.5743**

**Width : 4.756**

**Height : 5.032**

Entry

35

30

25

20

15

10

5

0

0

10

20

30

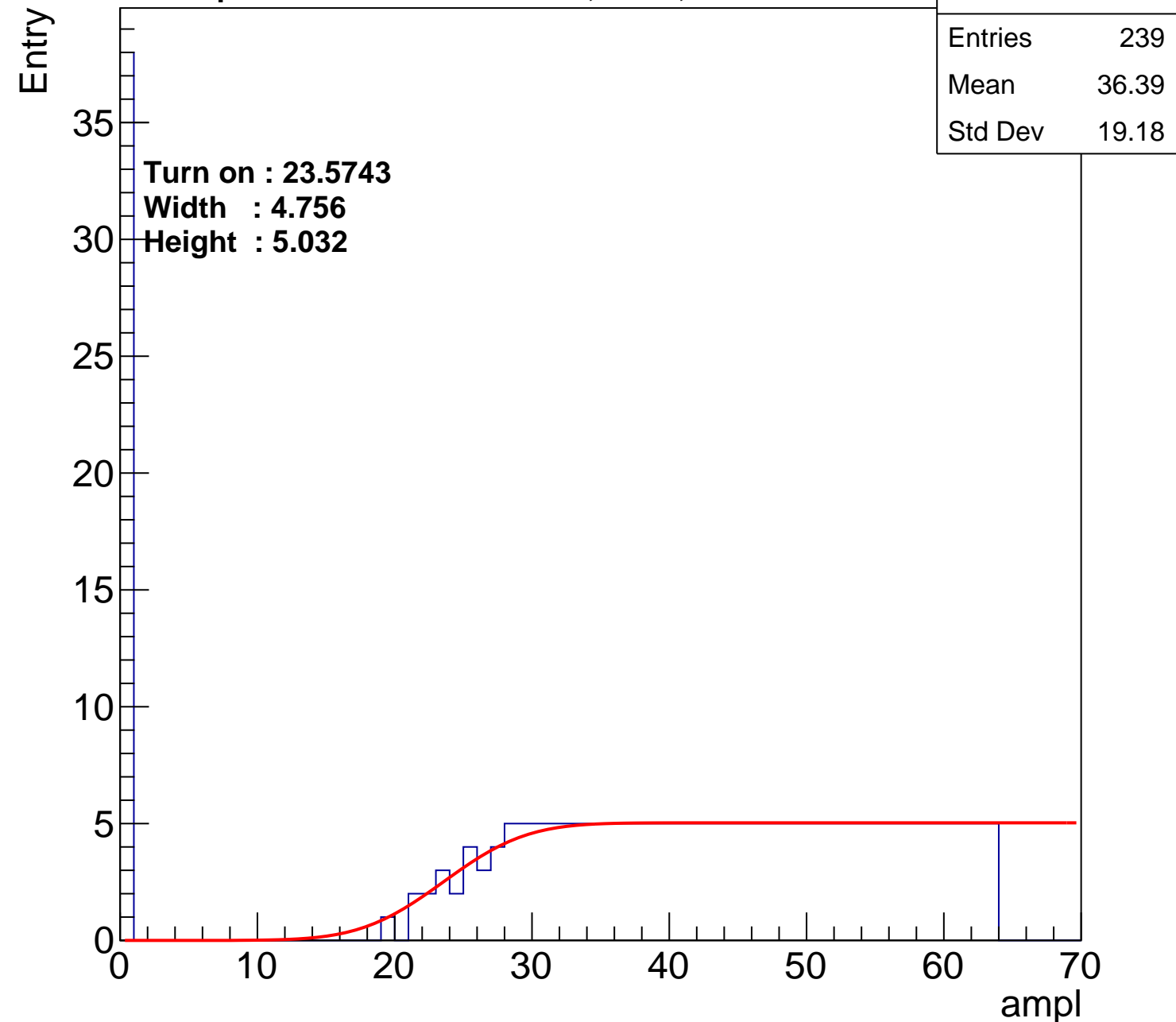
40

50

60

70

ampl



# B1L103S, U14-ch125

calib\_packv5\_041523\_1651.root, FC#0, Port C2

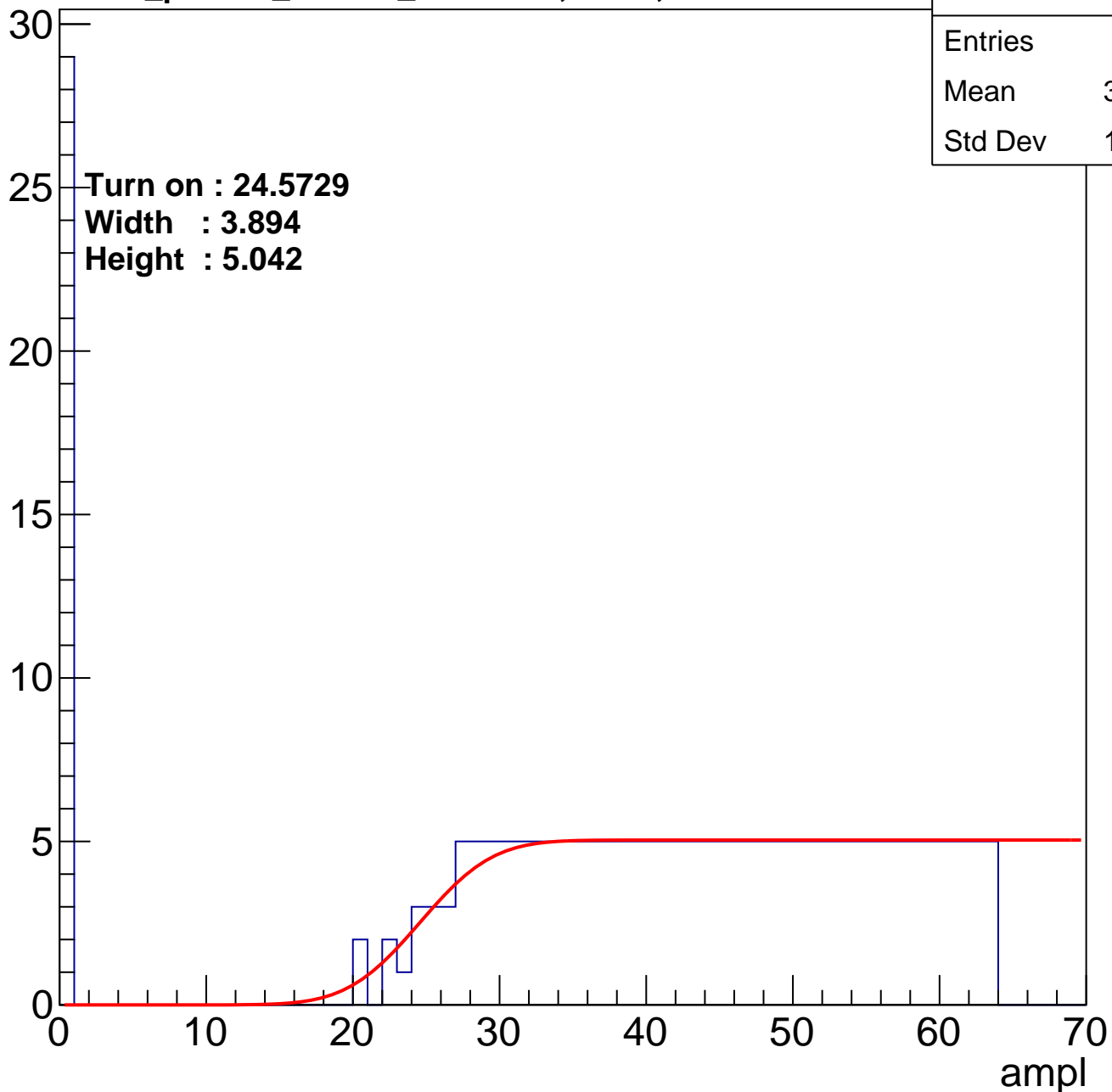
|         |       |
|---------|-------|
| Entries | 228   |
| Mean    | 37.97 |
| Std Dev | 18.13 |

Turn on : 24.5729

Width : 3.894

Height : 5.042

Entry



# B1L103S, U14-ch126

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 237   |
| Mean    | 36.76 |
| Std Dev | 18.86 |

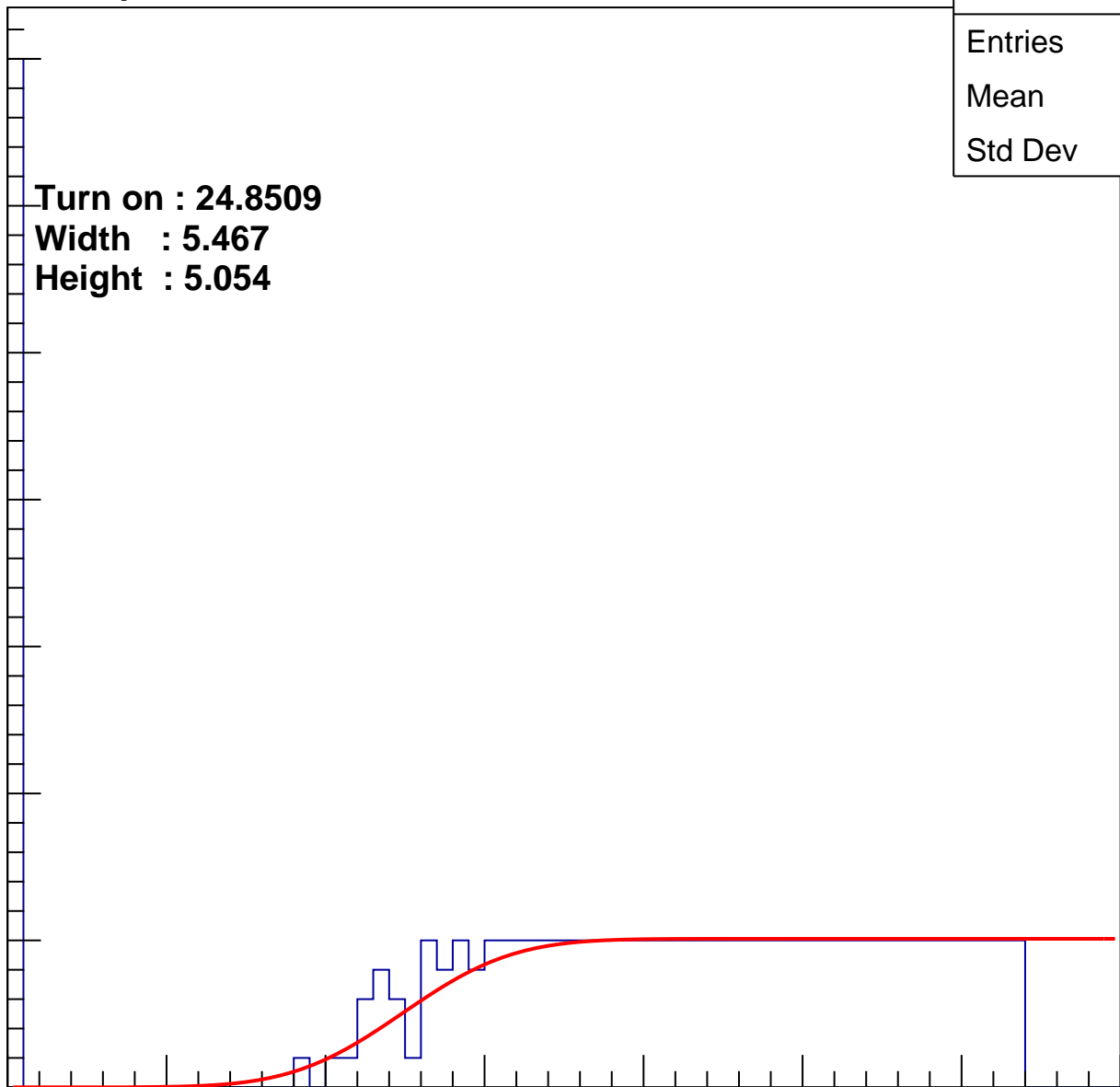
Entry

35  
30  
25  
20  
15  
10  
5  
0

Turn on : 24.8509  
Width : 5.467  
Height : 5.054

0 10 20 30 40 50 60 70

ampl

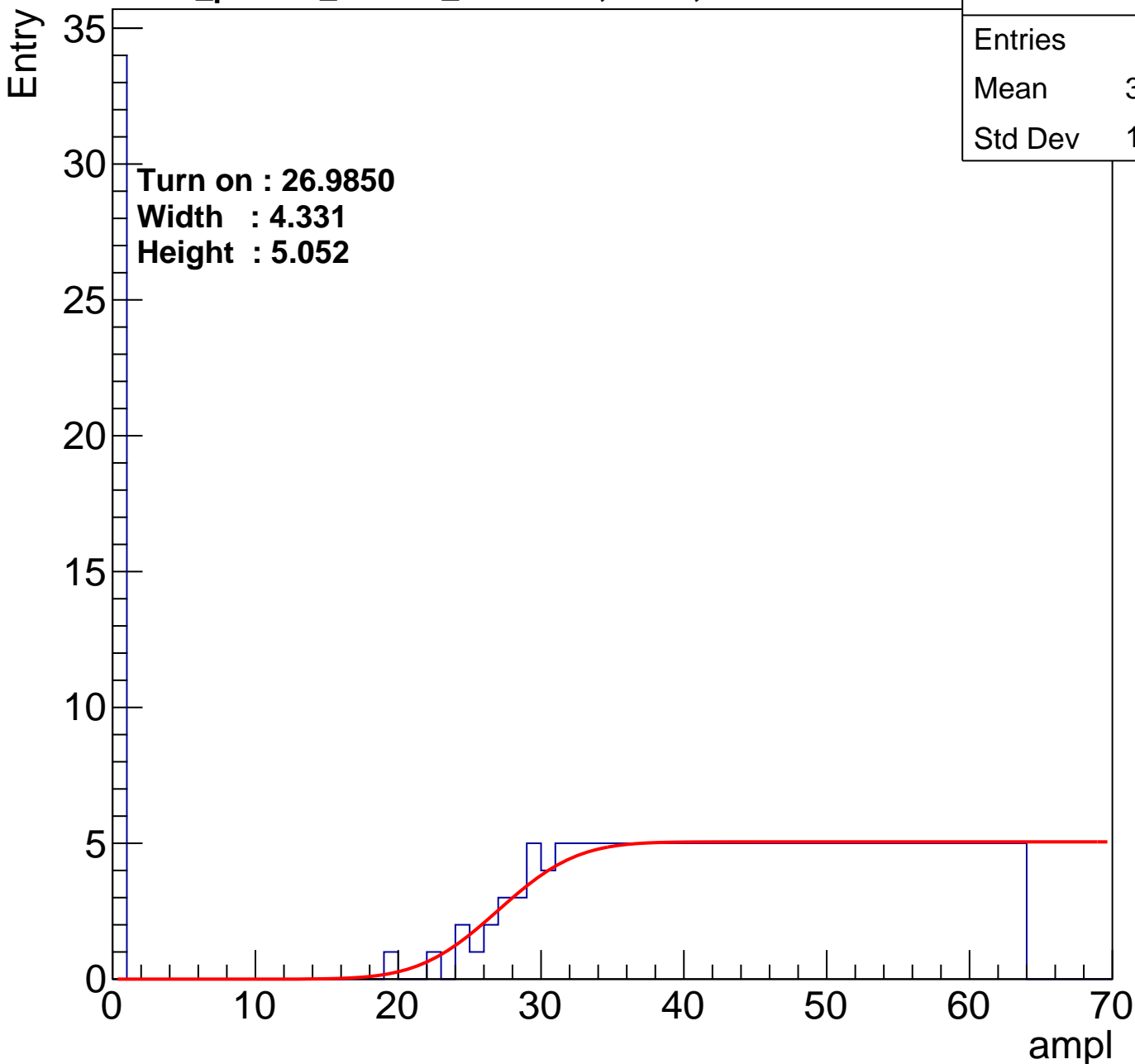


# B1L103S, U14-ch127

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 221   |
| Mean    | 37.79 |
| Std Dev | 19.05 |

Turn on : 26.9850  
Width : 4.331  
Height : 5.052





# B1L103S, U15-ch0

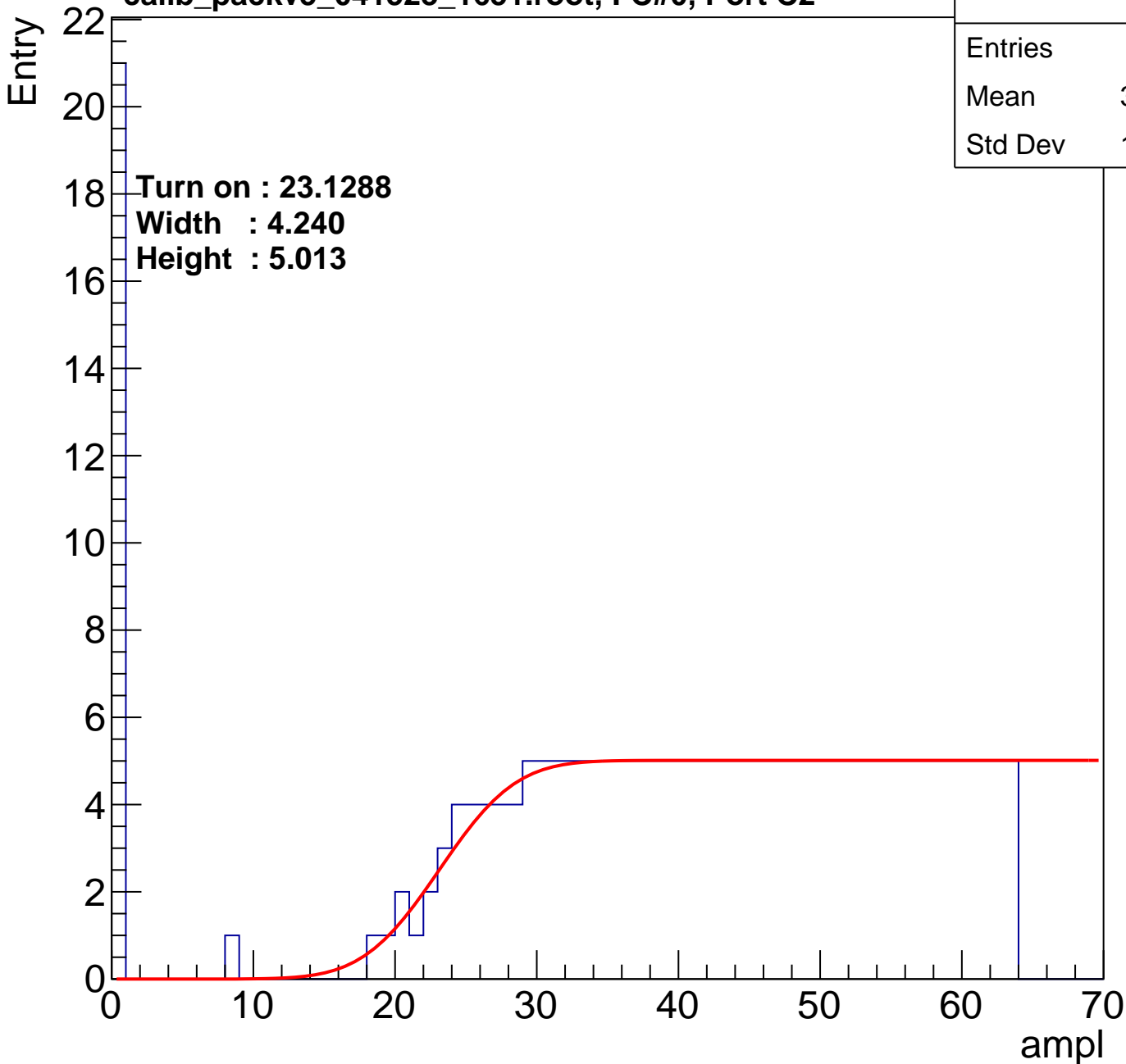
calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 227   |
| Mean    | 38.72 |
| Std Dev | 17.05 |

Turn on : 23.1288

Width : 4.240

Height : 5.013



# B1L103S, U15-ch1

calib\_packv5\_041523\_1651.root, FC#0, Port C2

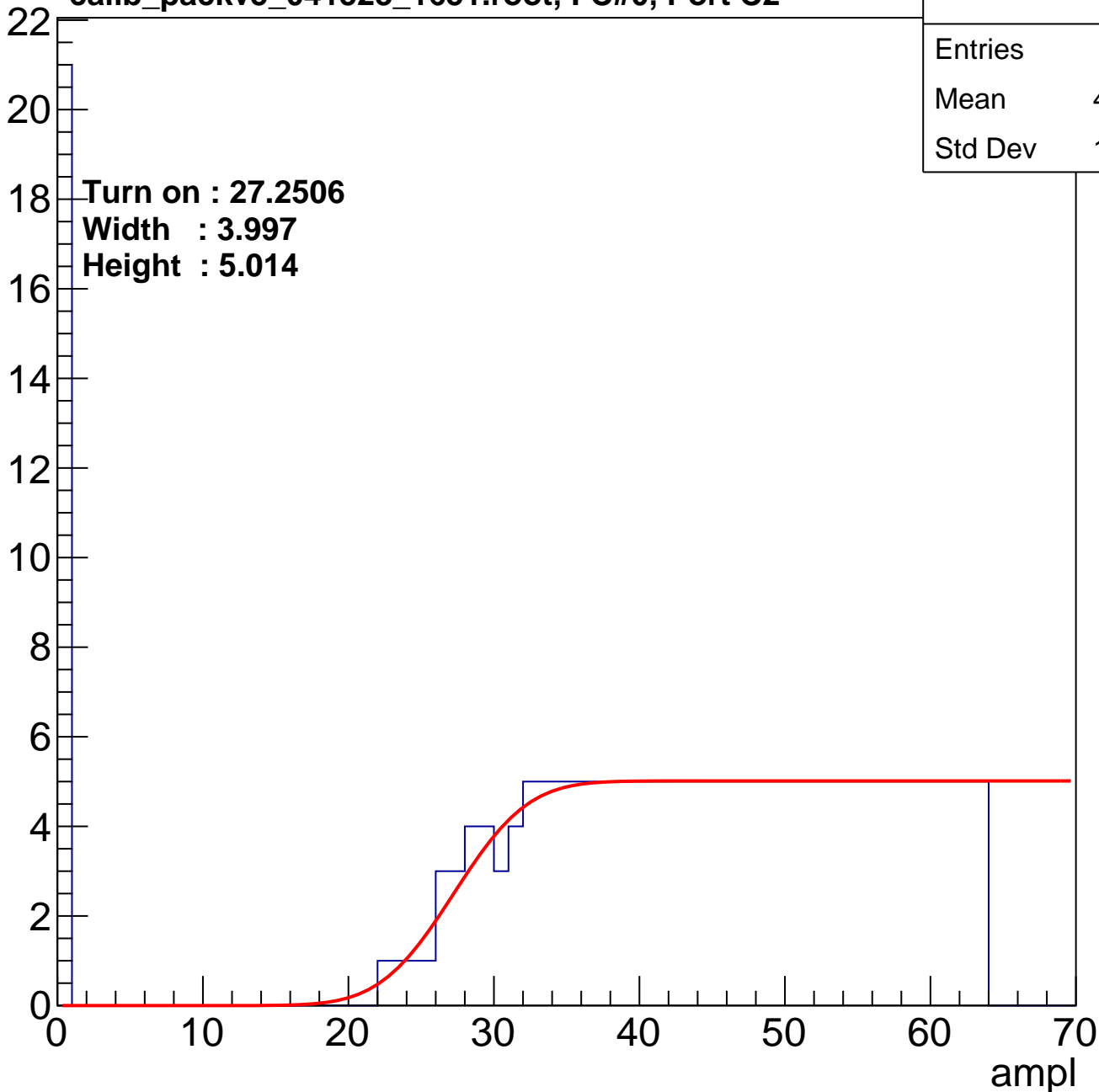
|         |       |
|---------|-------|
| Entries | 206   |
| Mean    | 40.27 |
| Std Dev | 17.08 |

Turn on : 27.2506

Width : 3.997

Height : 5.014

Entry



# B1L103S, U15-ch2

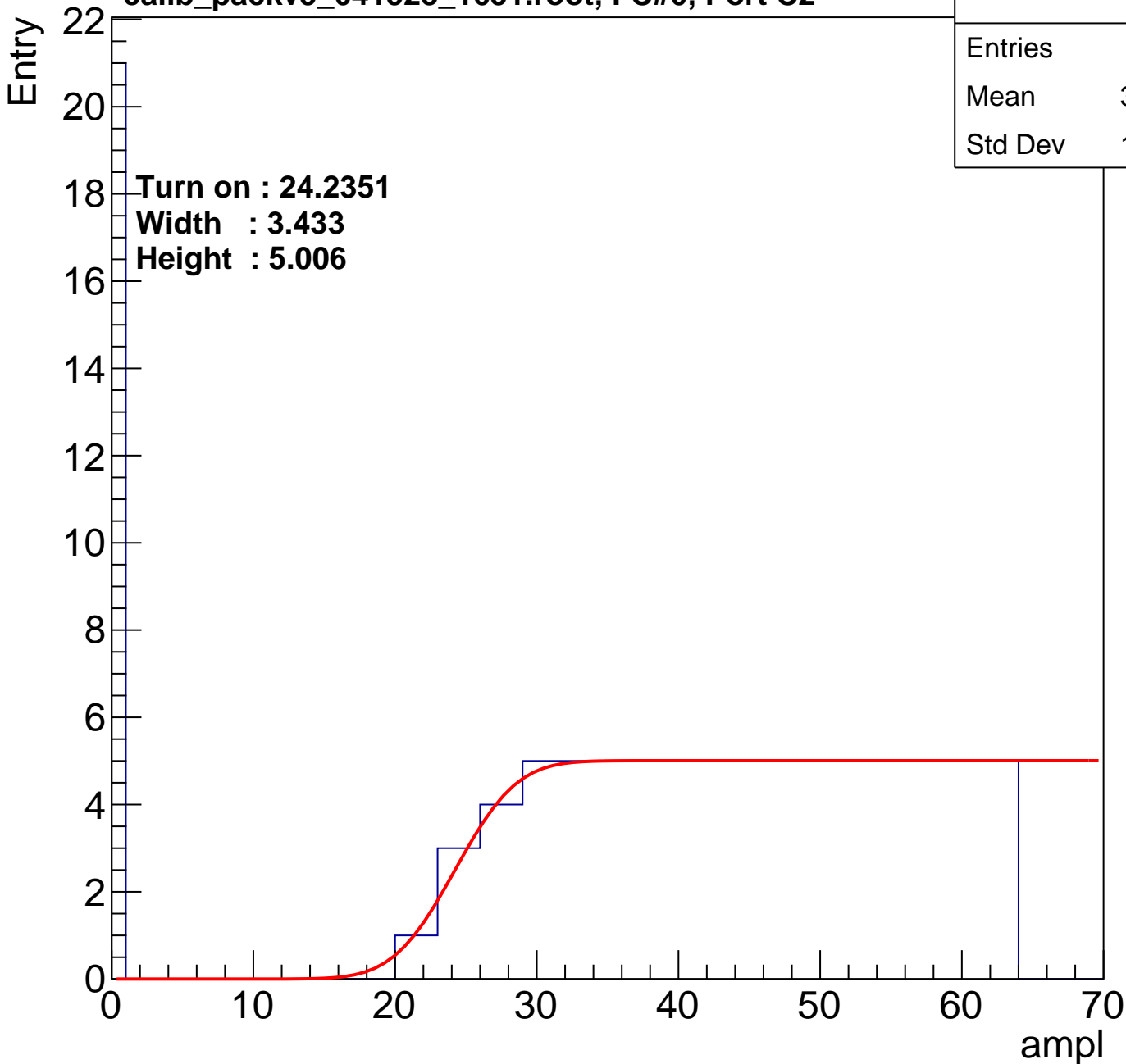
calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 220   |
| Mean    | 39.33 |
| Std Dev | 16.93 |

Turn on : 24.2351

Width : 3.433

Height : 5.006



# B1L103S, U15-ch3

calib\_packv5\_041523\_1651.root, FC#0, Port C2

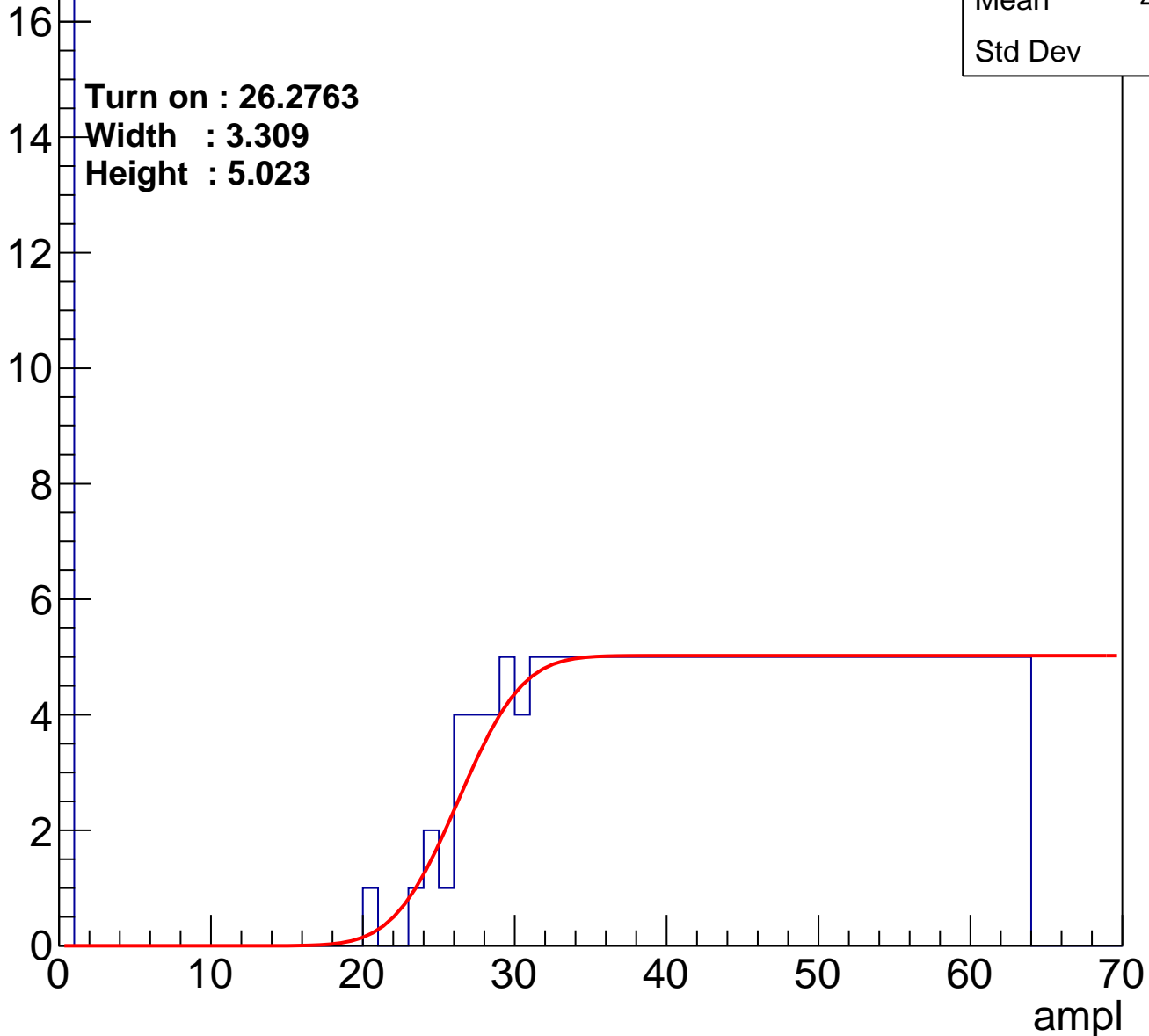
|         |       |
|---------|-------|
| Entries | 208   |
| Mean    | 40.67 |
| Std Dev | 16.2  |

**Turn on : 26.2763**

**Width : 3.309**

**Height : 5.023**

Entry



# B1L103S, U15-ch4

calib\_packv5\_041523\_1651.root, FC#0, Port C2

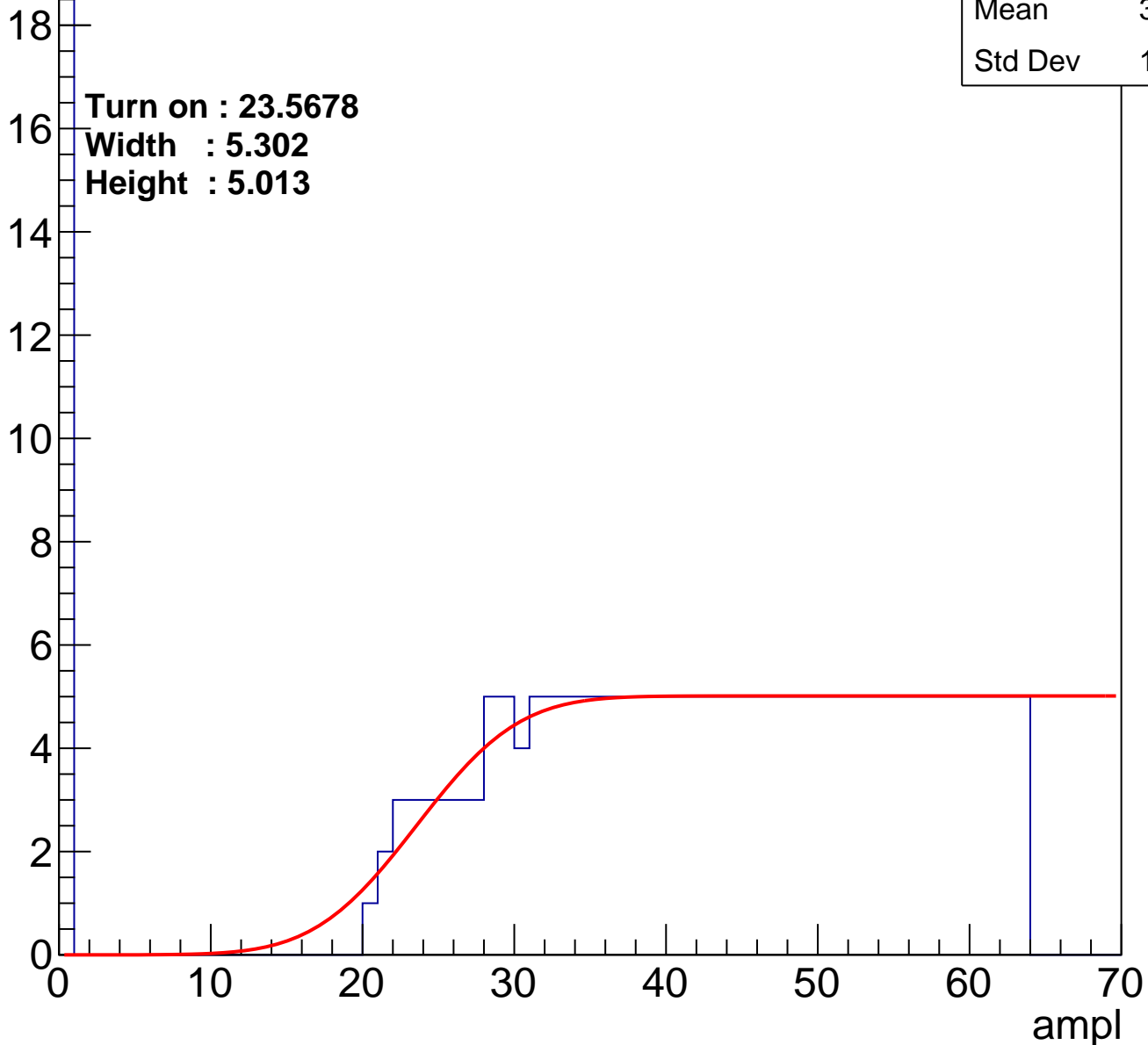
|         |       |
|---------|-------|
| Entries | 219   |
| Mean    | 39.56 |
| Std Dev | 16.64 |

**Turn on : 23.5678**

**Width : 5.302**

**Height : 5.013**

Entry



# B1L103S, U15-ch5

calib\_packv5\_041523\_1651.root, FC#0, Port C2

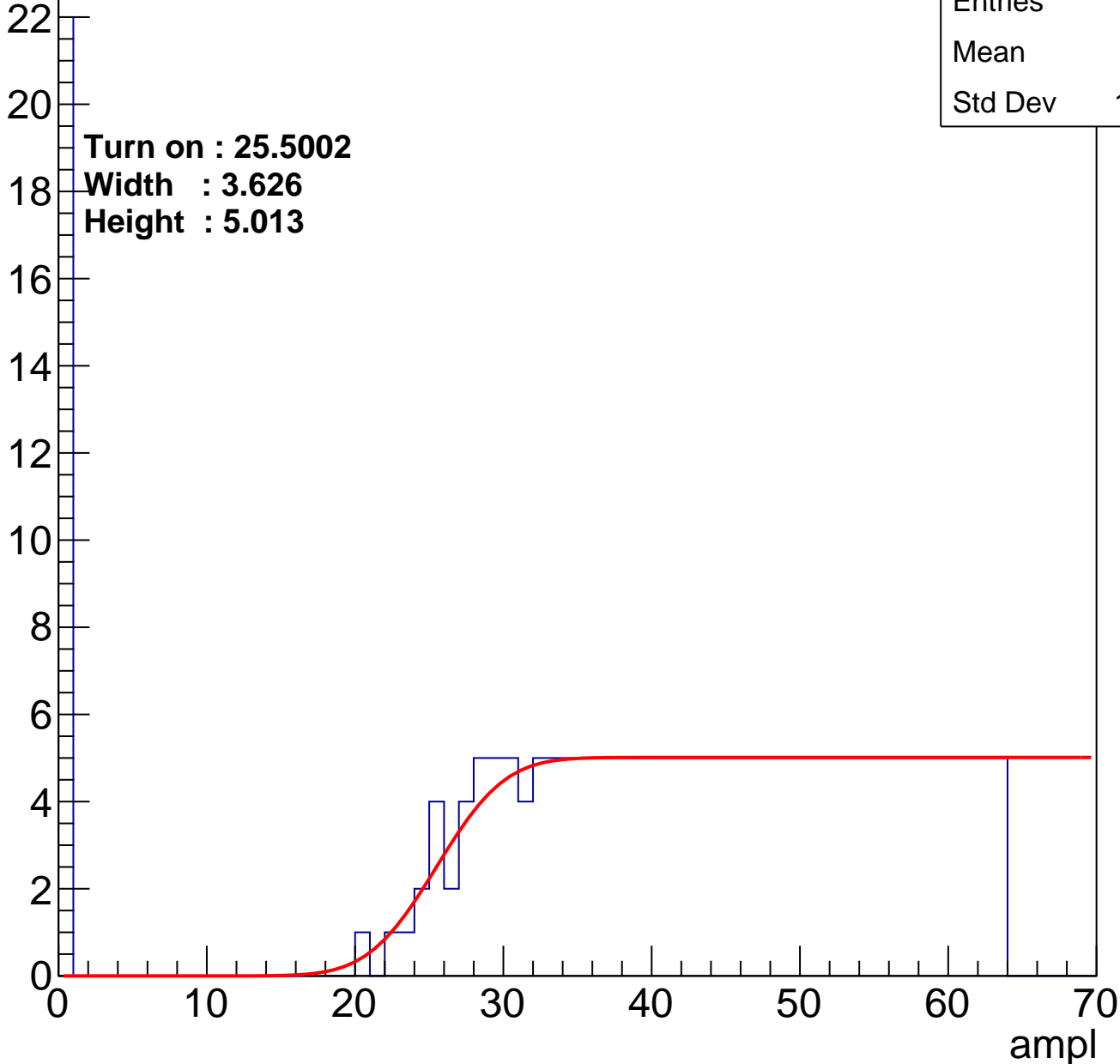
|         |       |
|---------|-------|
| Entries | 216   |
| Mean    | 39.5  |
| Std Dev | 17.14 |

**Turn on : 25.5002**

**Width : 3.626**

**Height : 5.013**

Entry



# B1L103S, U15-ch6

calib\_packv5\_041523\_1651.root, FC#0, Port C2

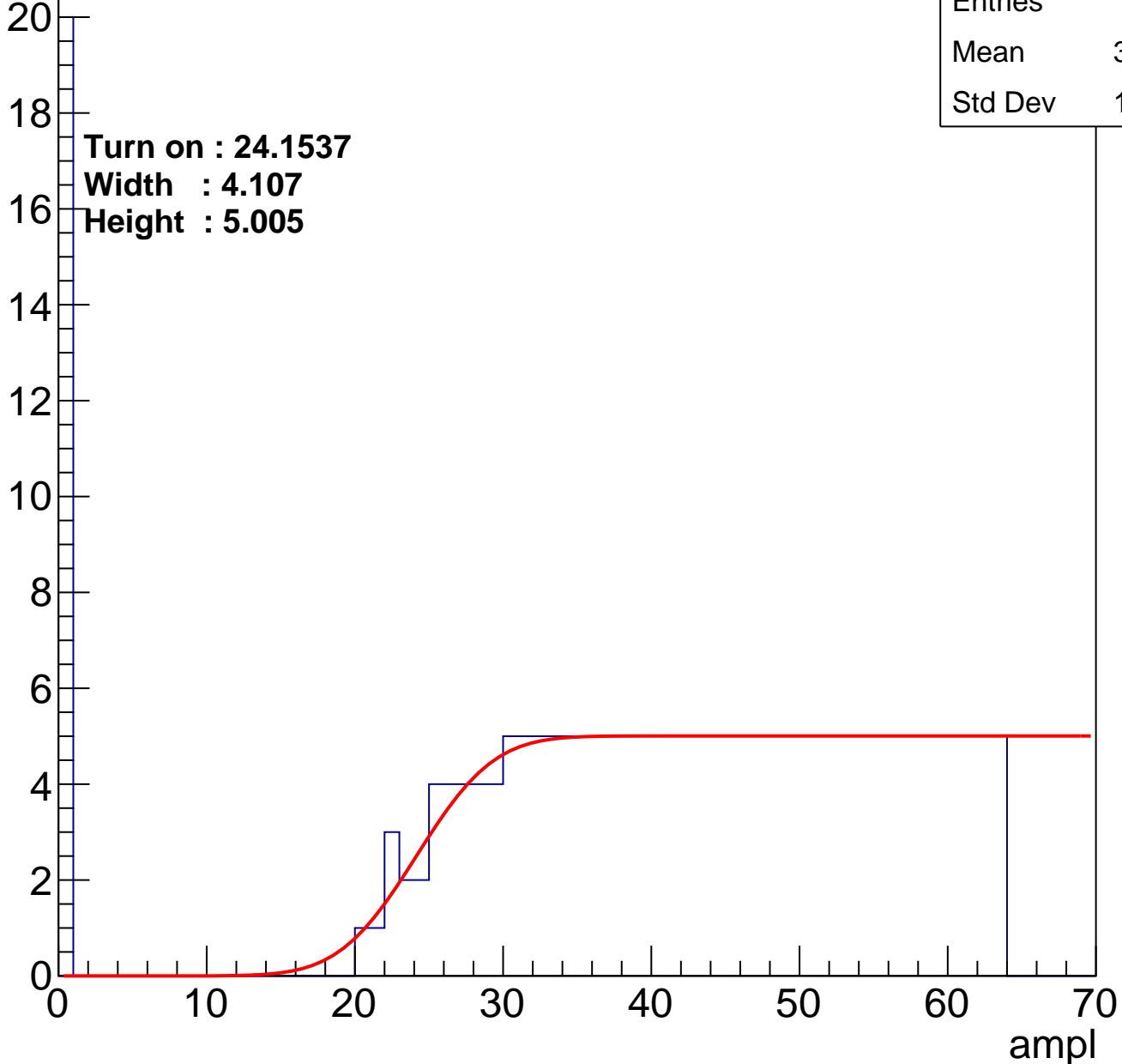
|         |       |
|---------|-------|
| Entries | 219   |
| Mean    | 39.48 |
| Std Dev | 16.79 |

**Turn on : 24.1537**

**Width : 4.107**

**Height : 5.005**

Entry



# B1L103S, U15-ch7

calib\_packv5\_041523\_1651.root, FC#0, Port C2

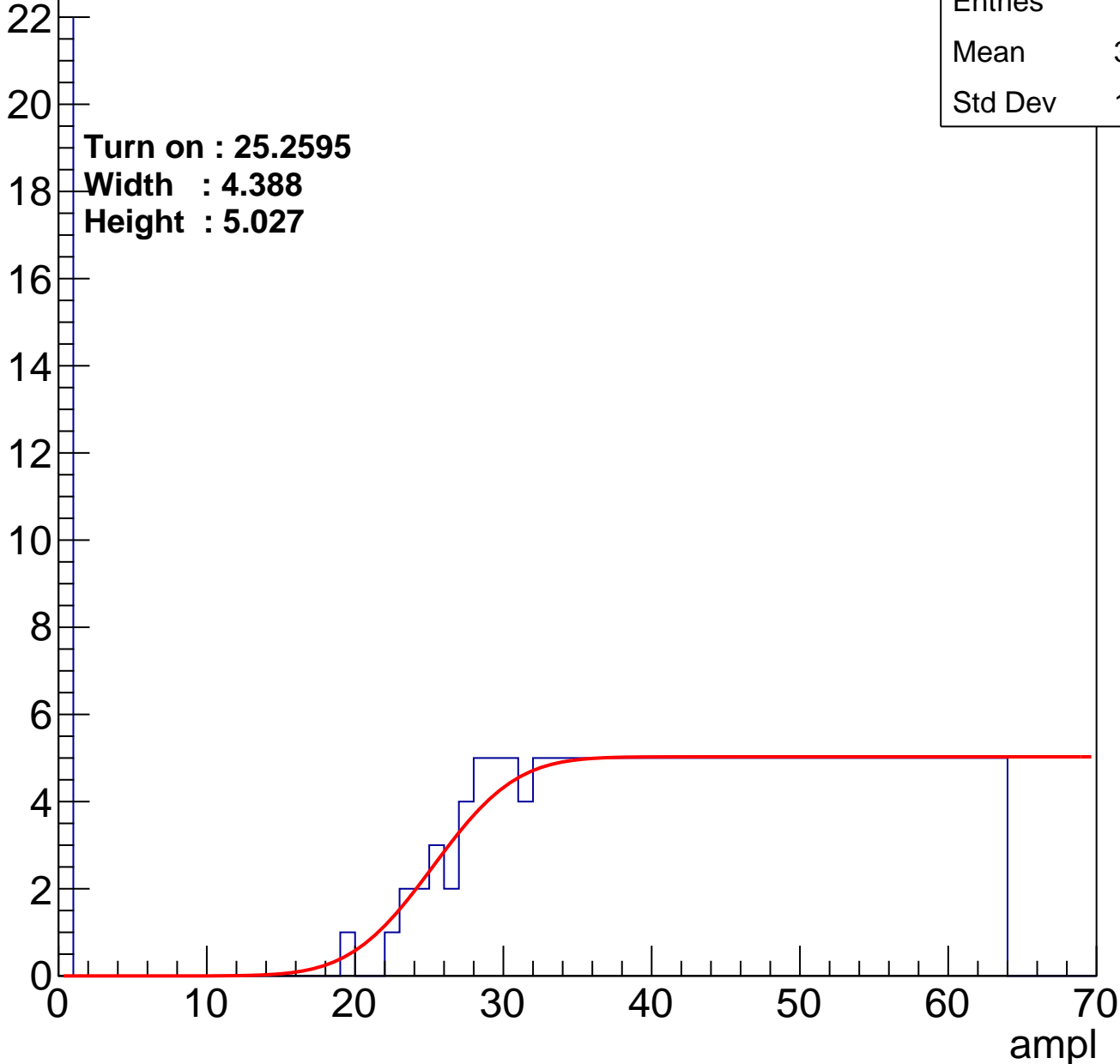
|         |       |
|---------|-------|
| Entries | 216   |
| Mean    | 39.49 |
| Std Dev | 17.15 |

**Turn on : 25.2595**

**Width : 4.388**

**Height : 5.027**

Entry





# B1L103S, U15-ch8

calib\_packv5\_041523\_1651.root, FC#0, Port C2

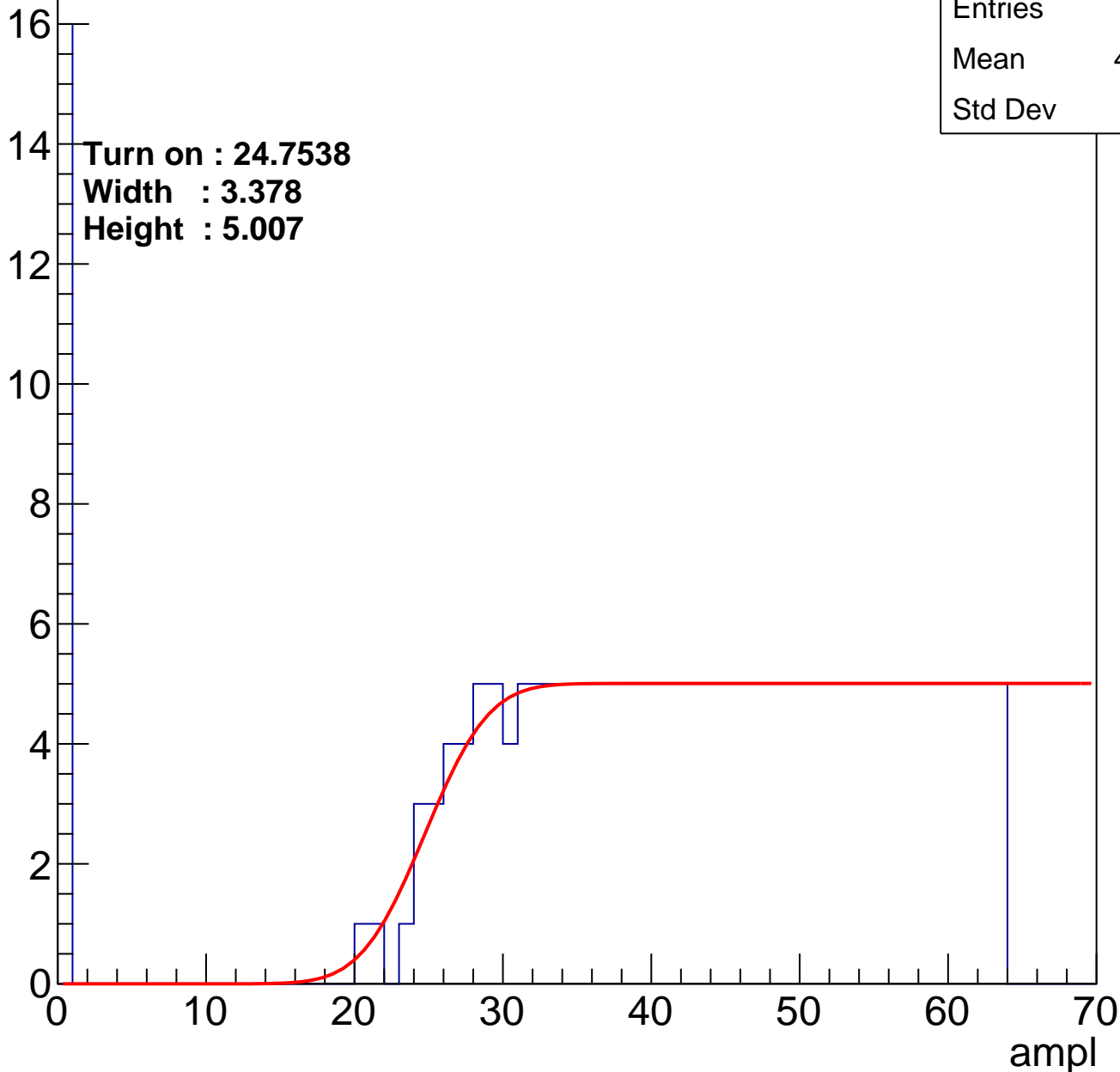
|         |       |
|---------|-------|
| Entries | 212   |
| Mean    | 40.49 |
| Std Dev | 16    |

Turn on : 24.7538

Width : 3.378

Height : 5.007

Entry



# B1L103S, U15-ch9

calib\_packv5\_041523\_1651.root, FC#0, Port C2

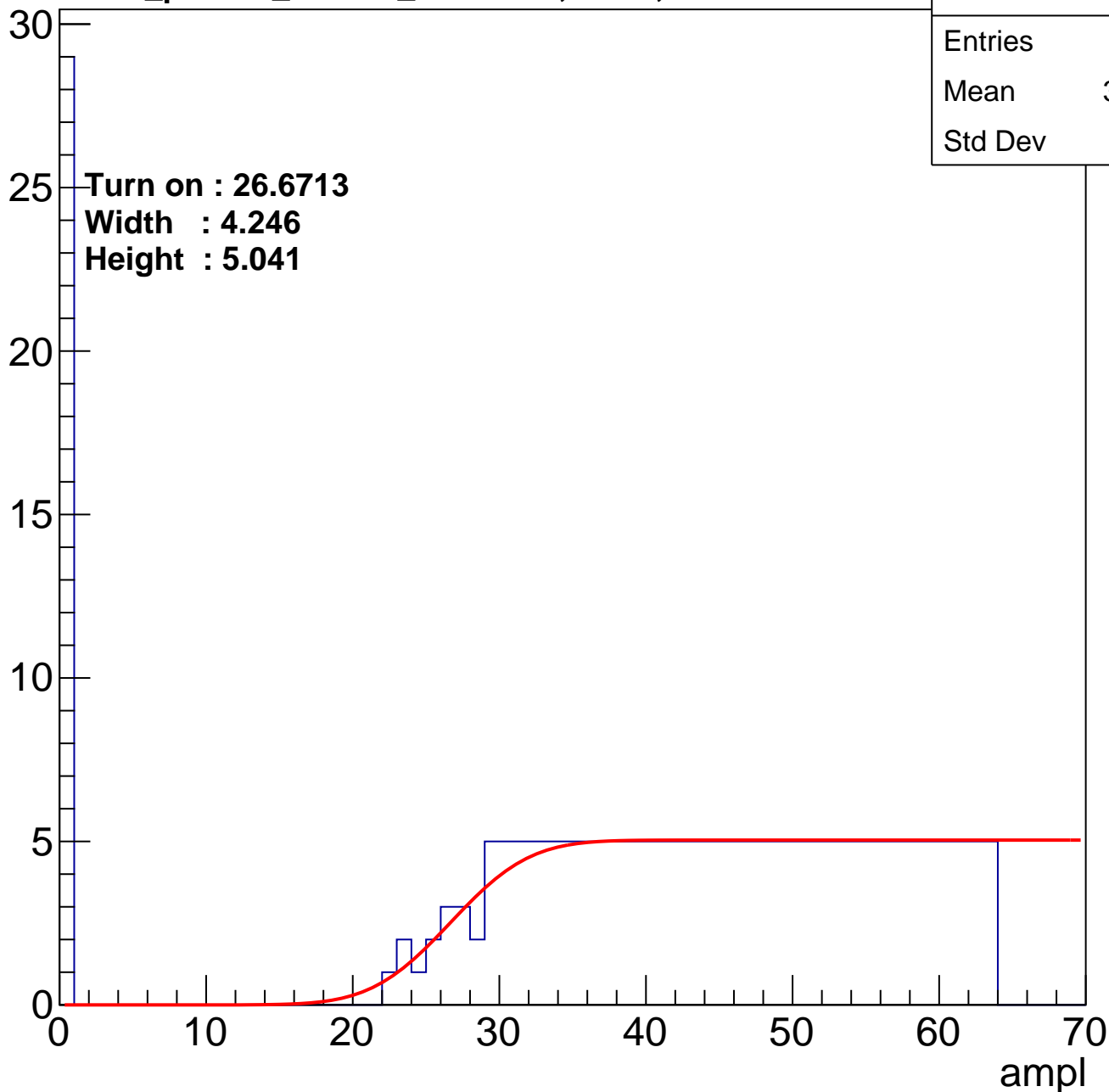
|         |       |
|---------|-------|
| Entries | 218   |
| Mean    | 38.56 |
| Std Dev | 18.31 |

Turn on : 26.6713

Width : 4.246

Height : 5.041

Entry



# B1L103S, U15-ch10

calib\_packv5\_041523\_1651.root, FC#0, Port C2

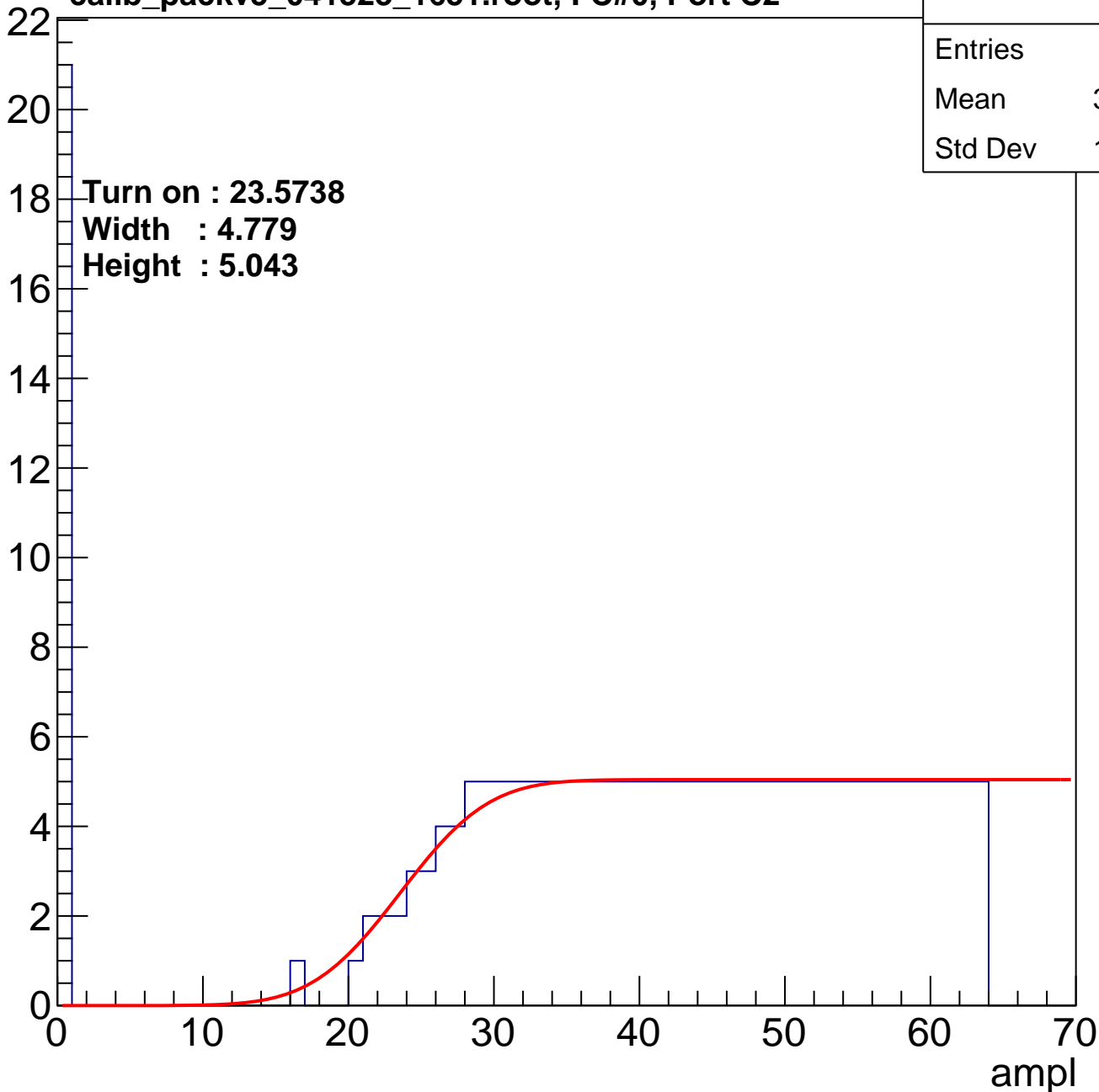
|         |       |
|---------|-------|
| Entries | 223   |
| Mean    | 39.09 |
| Std Dev | 16.96 |

Turn on : 23.5738

Width : 4.779

Height : 5.043

Entry

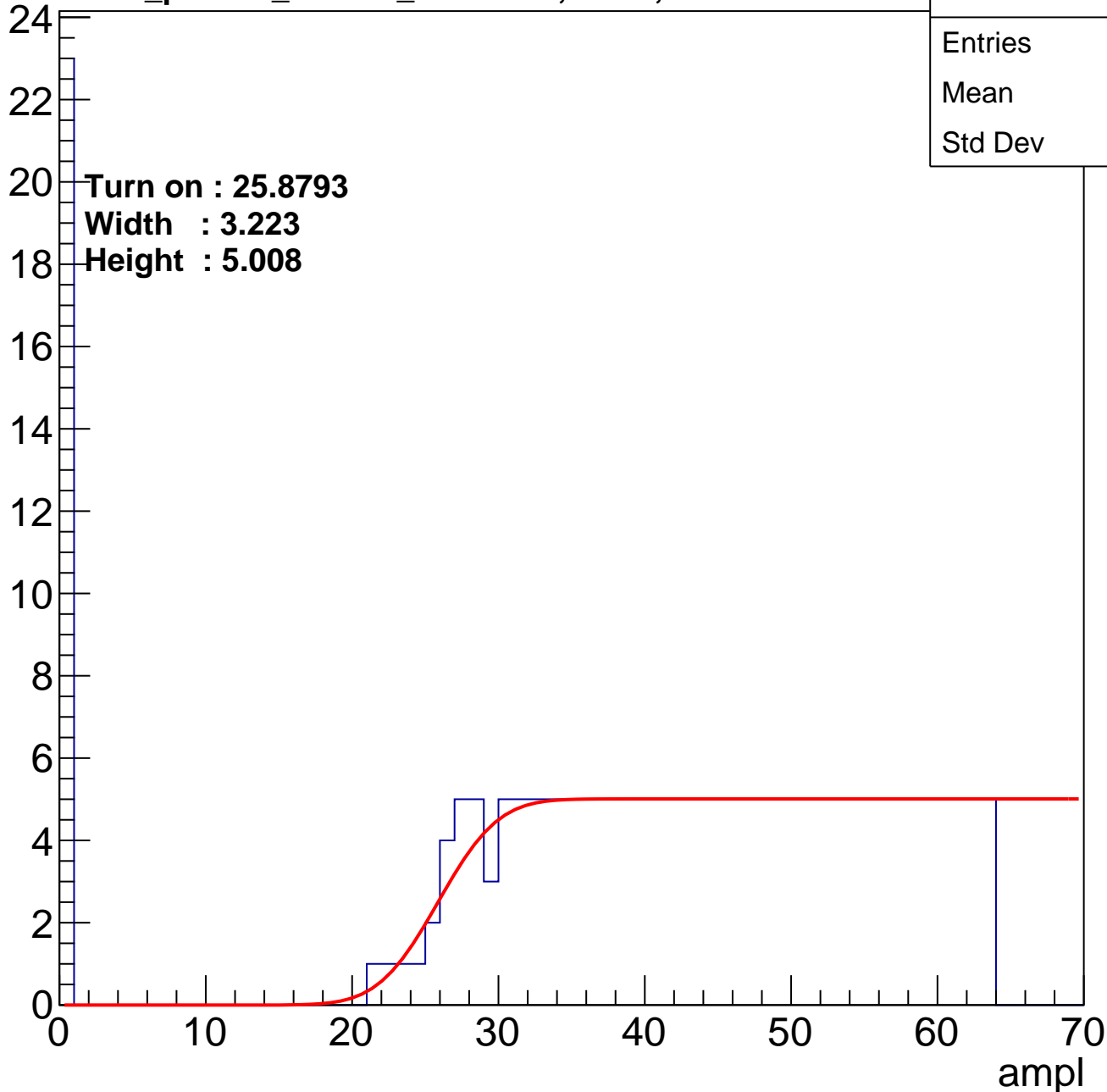


# B1L103S, U15-ch11

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |      |
|---------|------|
| Entries | 216  |
| Mean    | 39.4 |
| Std Dev | 17.3 |

Entry



# B1L103S, U15-ch12

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 216   |
| Mean    | 39.19 |
| Std Dev | 17.65 |

**Turn on : 26.4282**

**Width : 2.986**

**Height : 5.031**

Entry

25

20

15

10

5

0

0

10

20

30

40

50

60

70

ampl

0

# B1L103S, U15-ch13

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 218   |
| Mean    | 38.78 |
| Std Dev | 17.99 |

**Turn on : 26.8042**

**Width : 4.383**

**Height : 5.049**

Entry

25

20

15

10

5

0

0

10

20

30

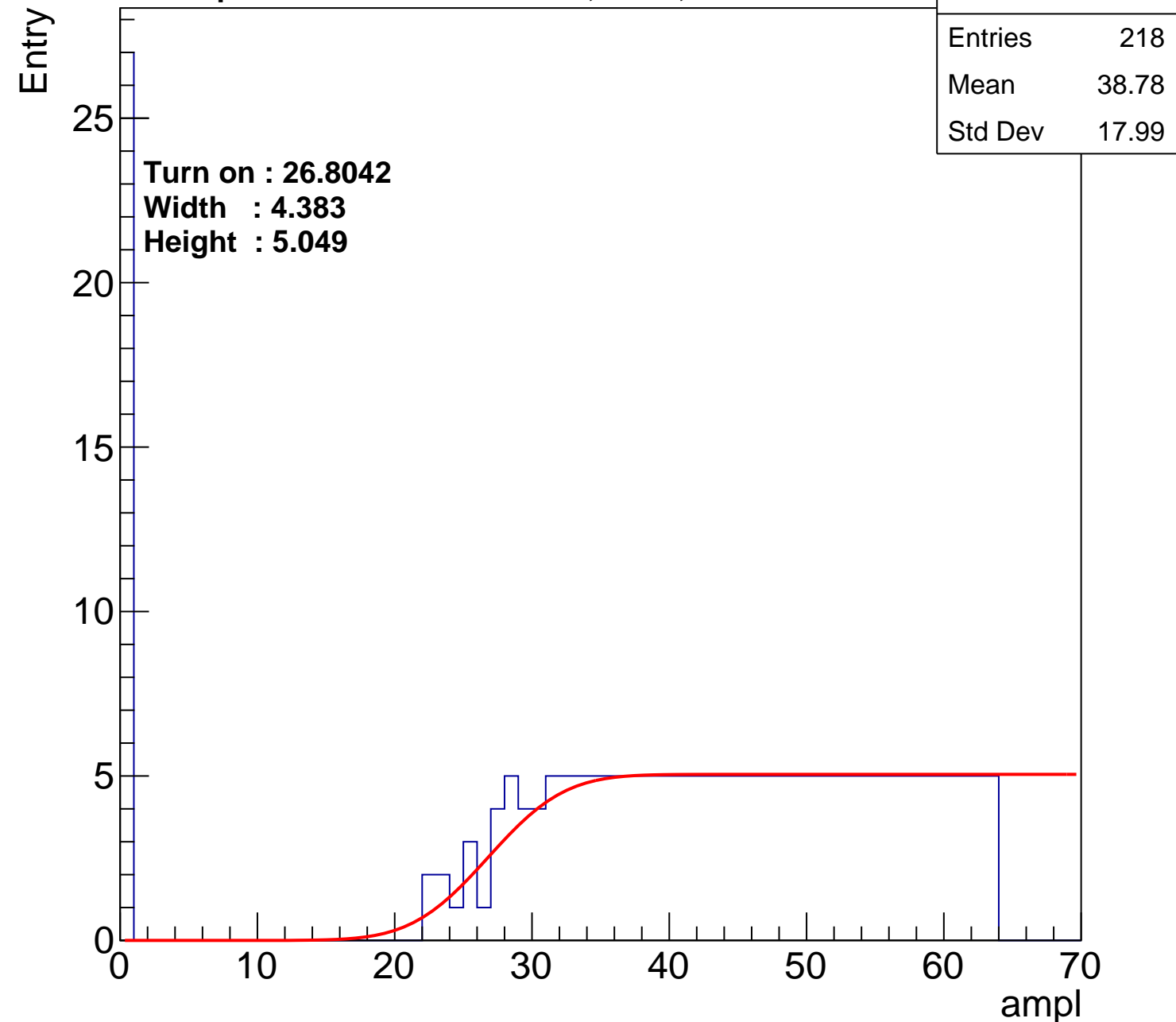
40

50

60

70

ampl



# B1L103S, U15-ch14

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 217   |
| Mean    | 38.96 |
| Std Dev | 17.83 |

**Turn on : 25.8480**

**Width : 4.483**

**Height : 5.028**

Entry

25

20

15

10

5

0

0

10

20

30

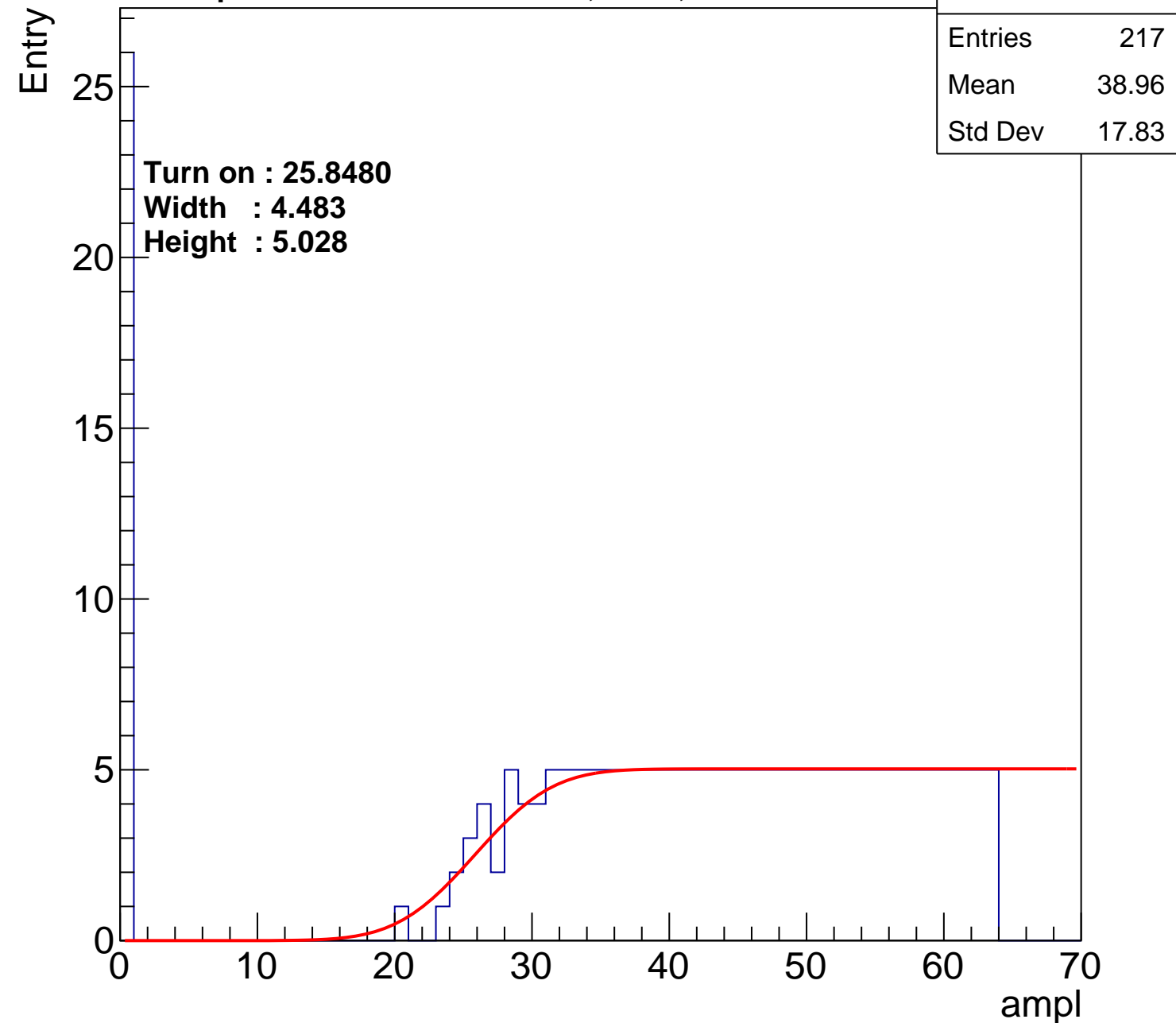
40

50

60

70

ampl



# B1L103S, U15-ch15

calib\_packv5\_041523\_1651.root, FC#0, Port C2

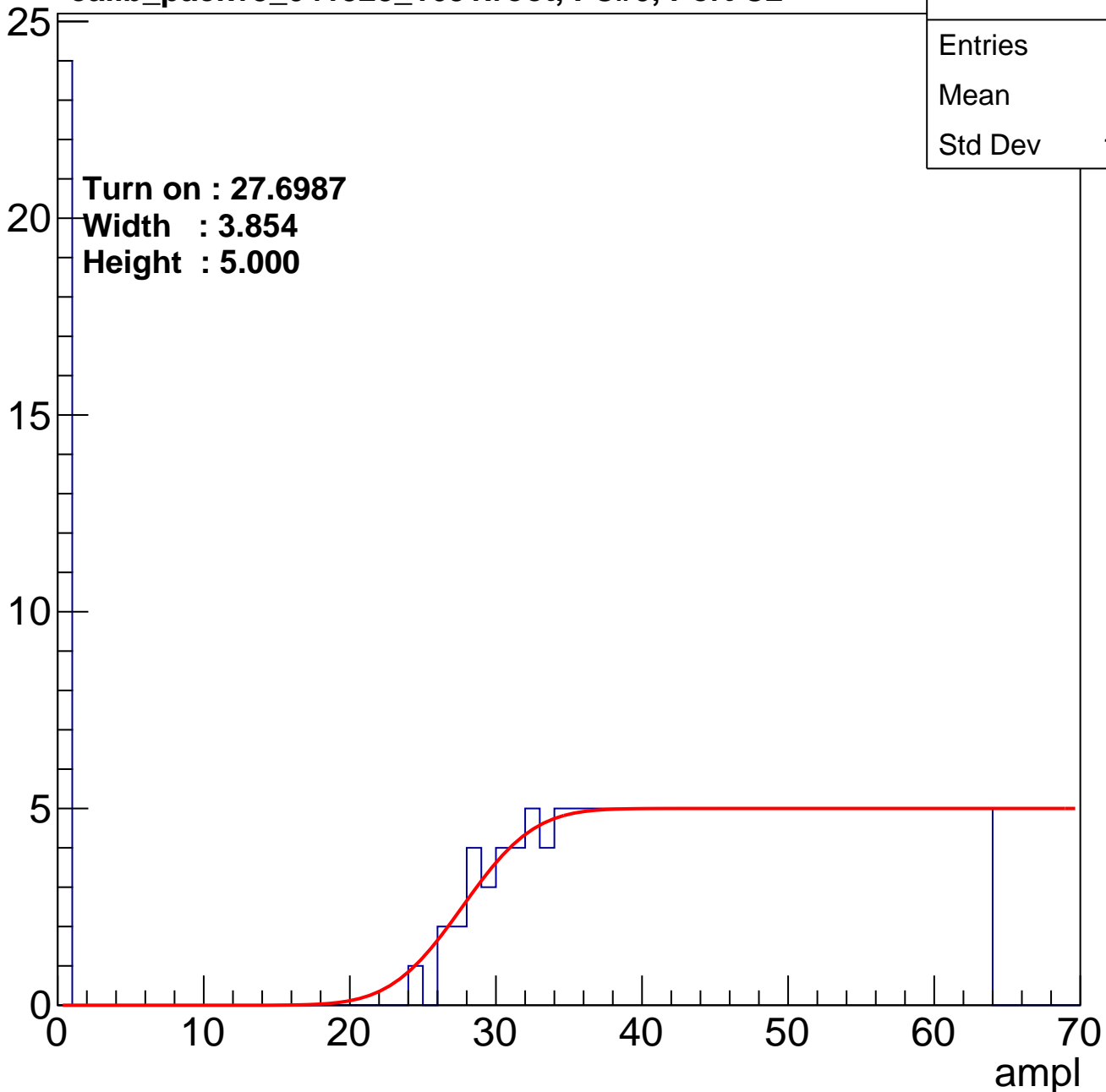
|         |       |
|---------|-------|
| Entries | 203   |
| Mean    | 40.1  |
| Std Dev | 17.71 |

Turn on : 27.6987

Width : 3.854

Height : 5.000

Entry





# B1L103S, U15-ch16

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 227   |
| Mean    | 38.46 |
| Std Dev | 17.61 |

**Turn on : 24.7078**

**Width : 3.332**

**Height : 5.069**

Entry

25

20

15

10

5

0

0

10

20

30

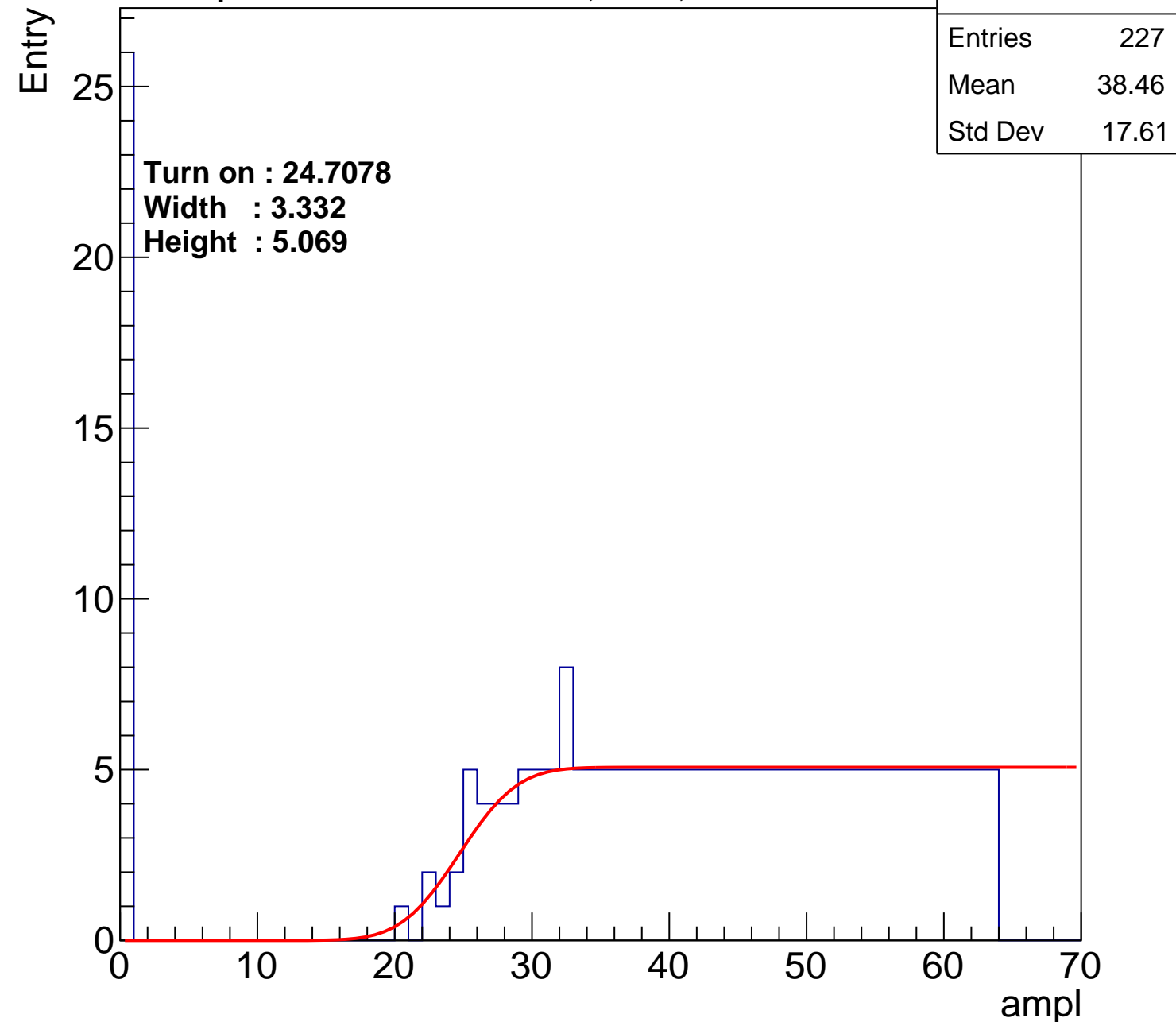
40

50

60

70

ampl

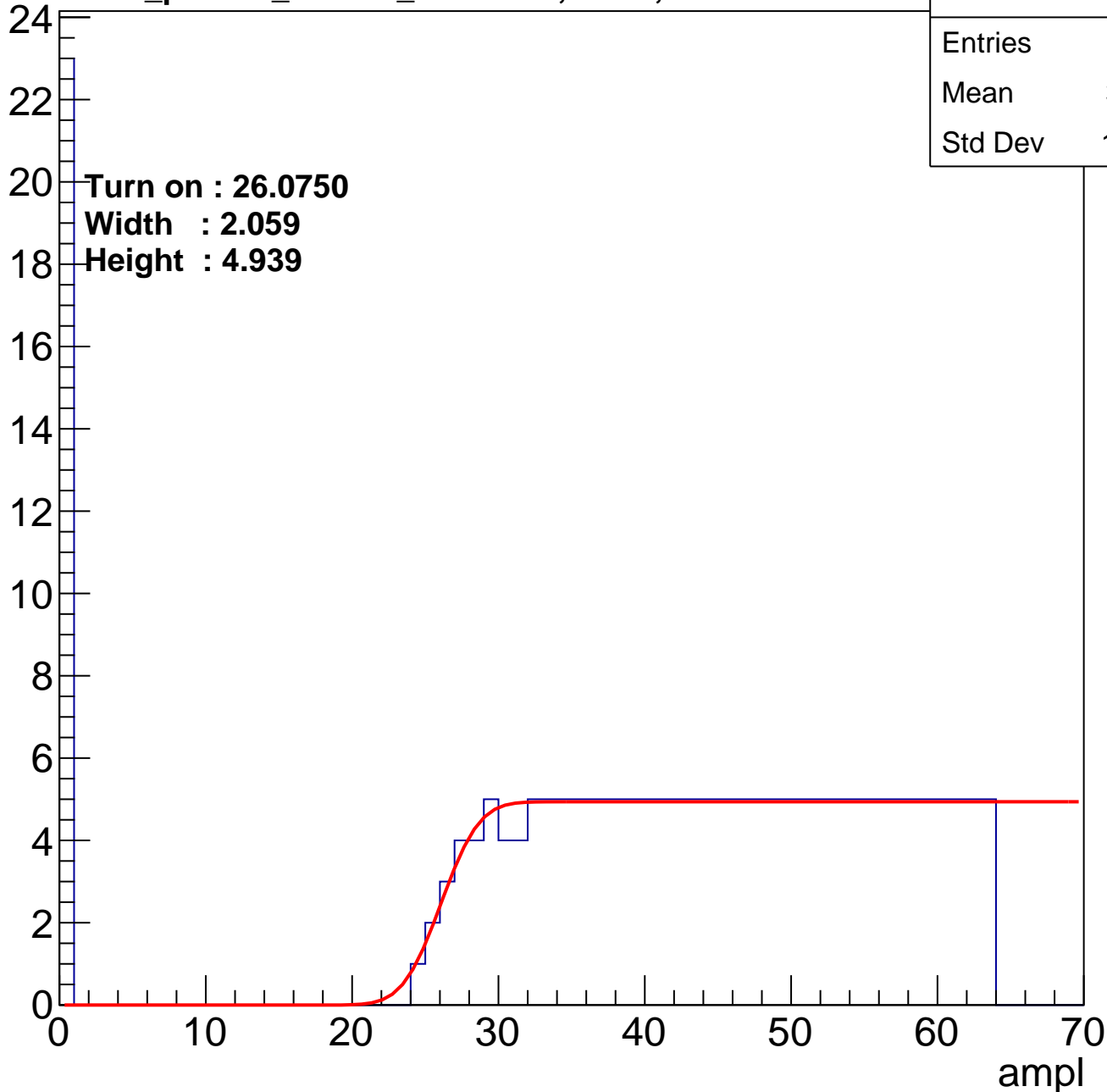


# B1L103S, U15-ch17

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 210   |
| Mean    | 39.81 |
| Std Dev | 17.36 |

Entry

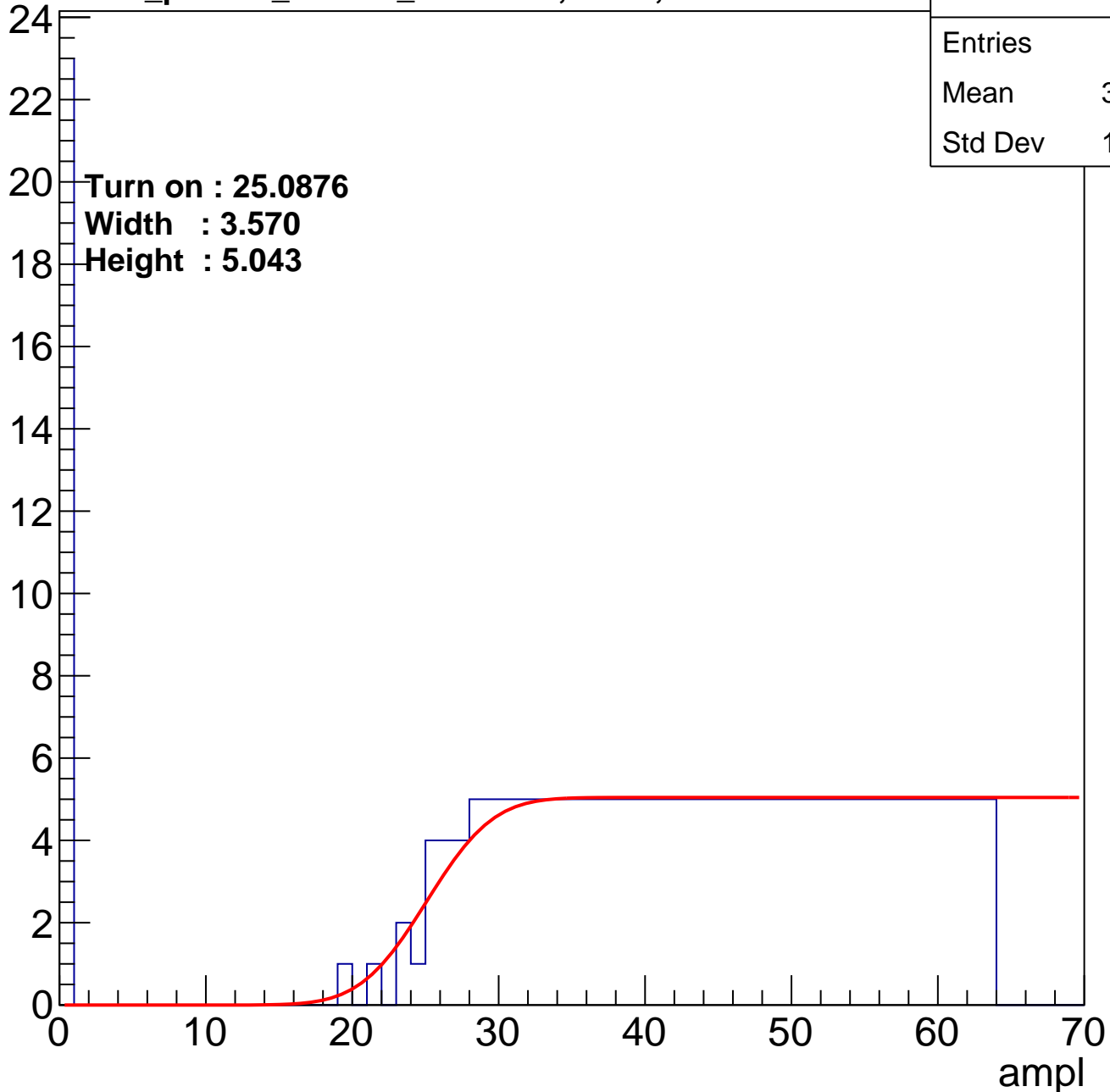


# B1L103S, U15-ch18

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 220   |
| Mean    | 39.15 |
| Std Dev | 17.26 |

Entry

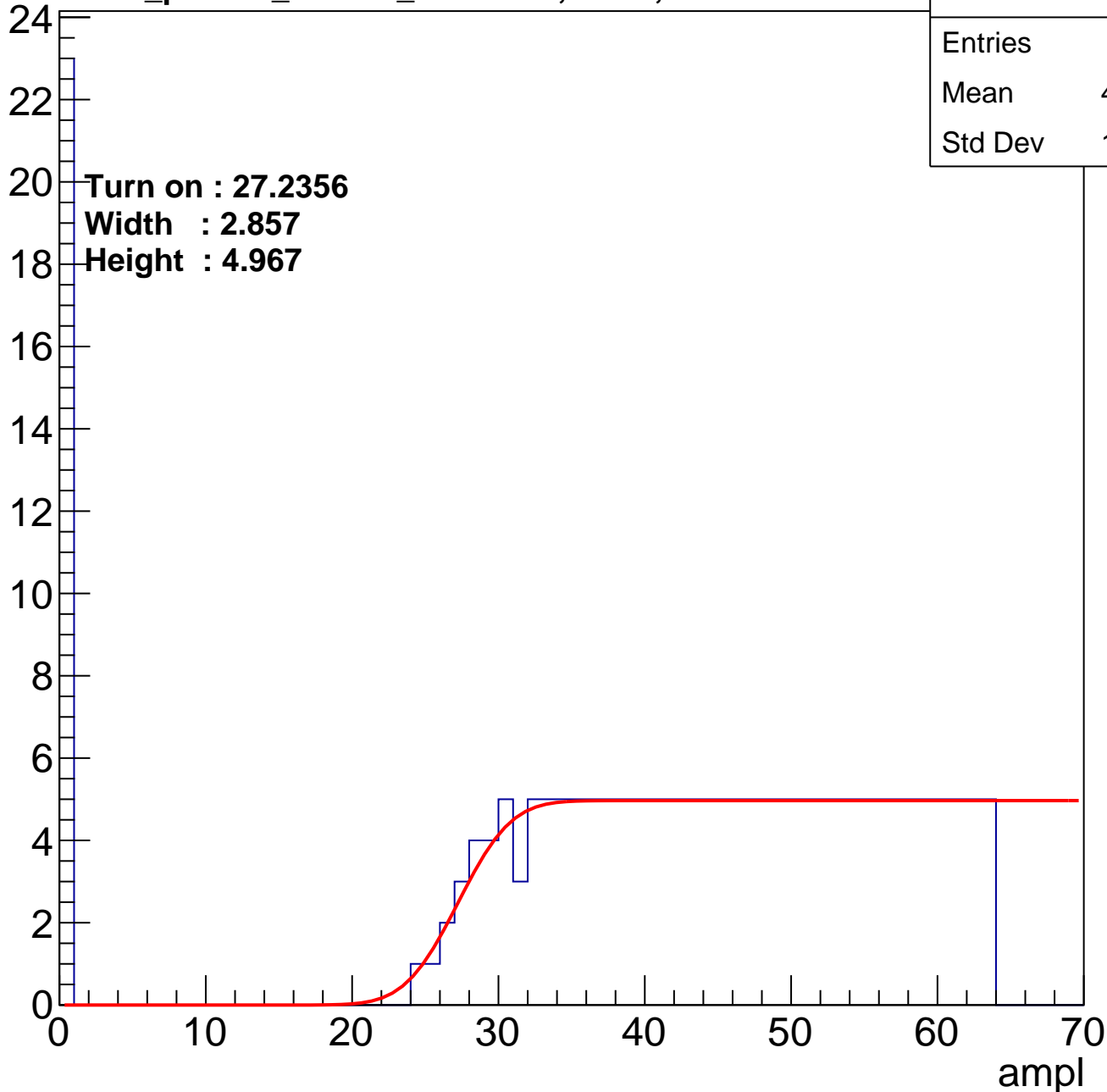


# B1L103S, U15-ch19

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 206   |
| Mean    | 40.06 |
| Std Dev | 17.44 |

Entry



# B1L103S, U15-ch20

calib\_packv5\_041523\_1651.root, FC#0, Port C2

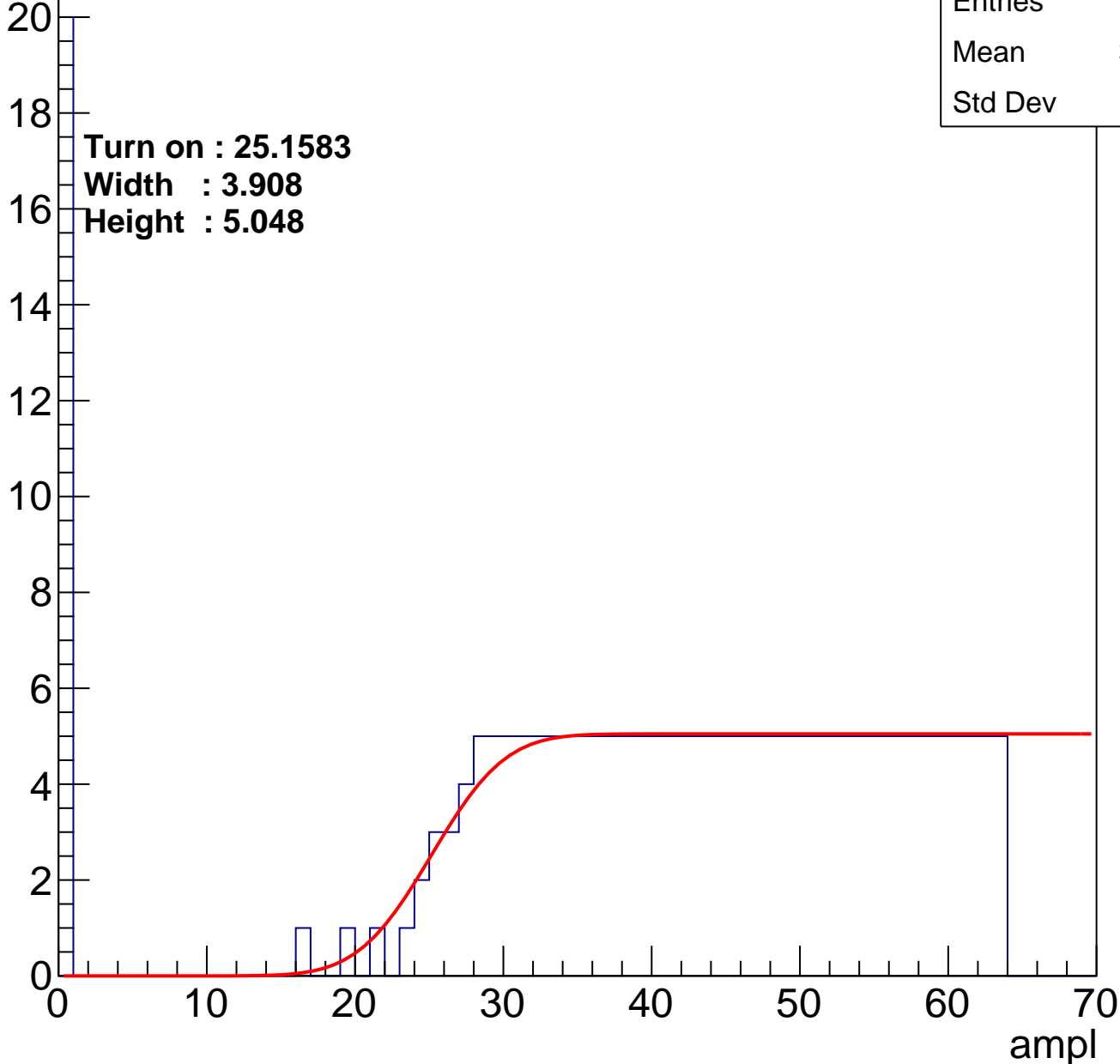
|         |       |
|---------|-------|
| Entries | 216   |
| Mean    | 39.71 |
| Std Dev | 16.8  |

**Turn on : 25.1583**

**Width : 3.908**

**Height : 5.048**

Entry



# B1L103S, U15-ch21

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 197   |
| Mean    | 41.81 |
| Std Dev | 15.73 |

**Turn on : 27.3215**

**Width : 2.090**

**Height : 4.982**

Entry

14

12

10

8

6

4

2

0

0

10

20

30

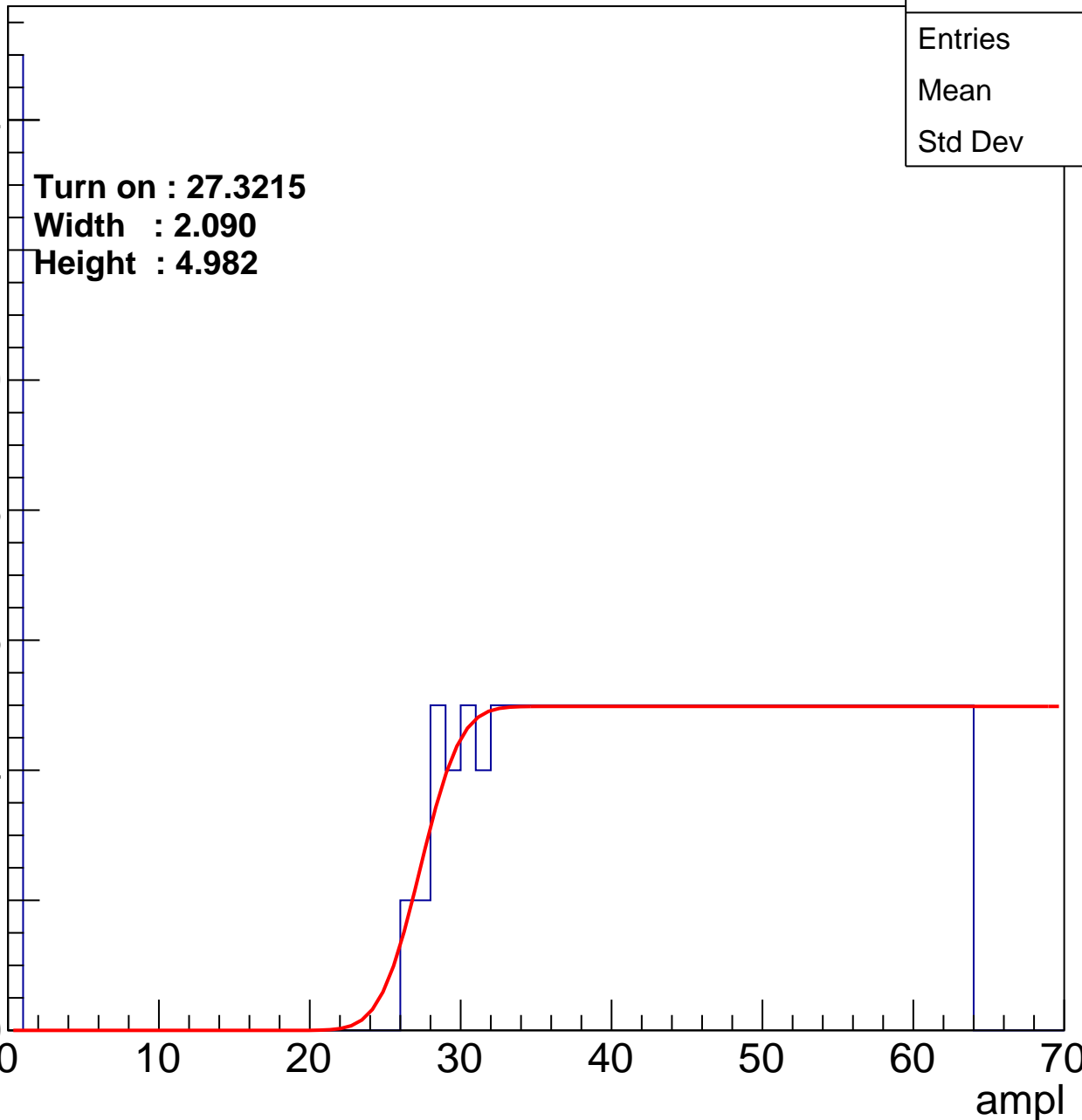
40

50

60

70

ampl

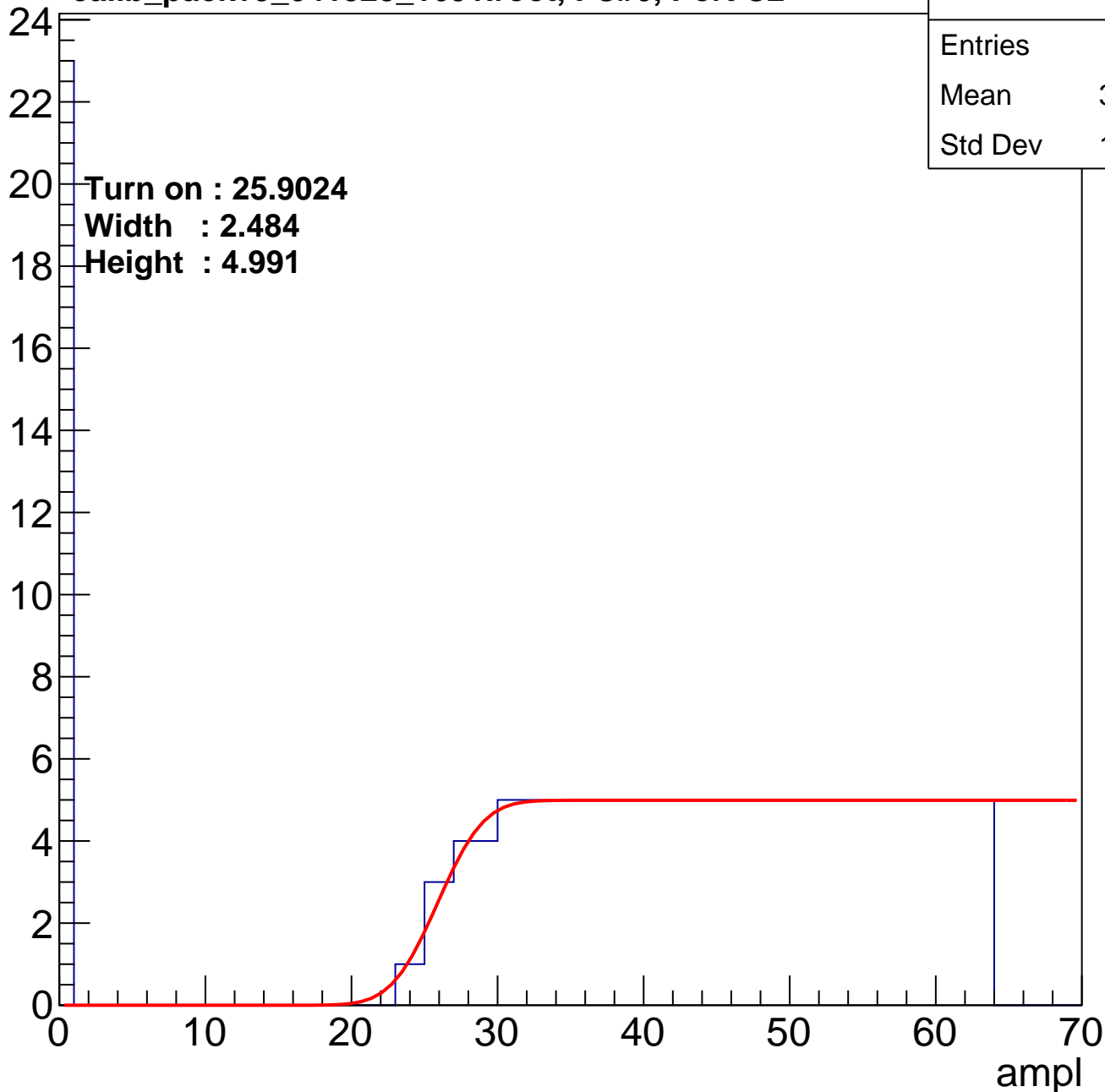


# B1L103S, U15-ch22

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 213   |
| Mean    | 39.63 |
| Std Dev | 17.32 |

Entry

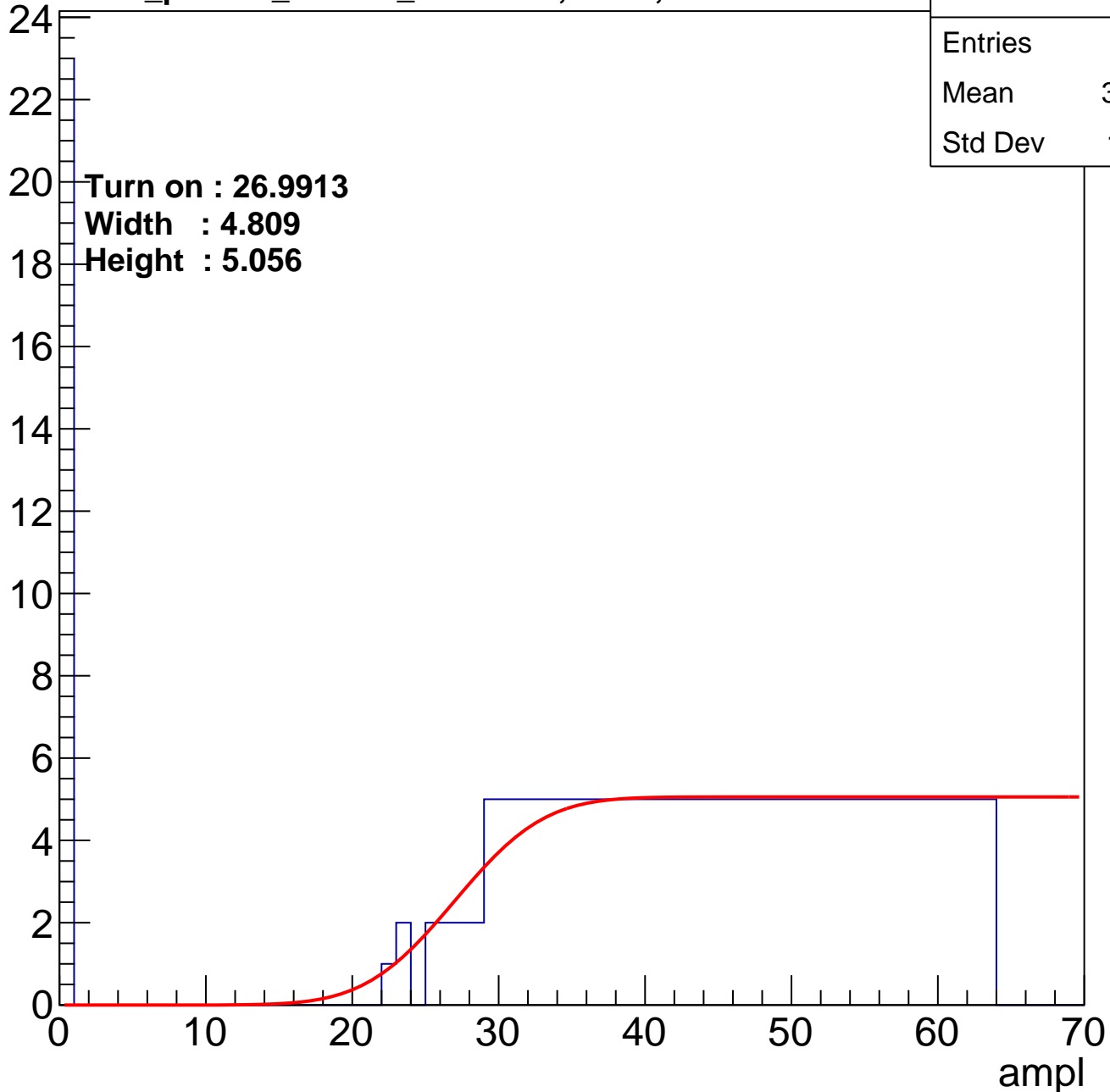


# B1L103S, U15-ch23

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 209   |
| Mean    | 39.86 |
| Std Dev | 17.41 |

Entry



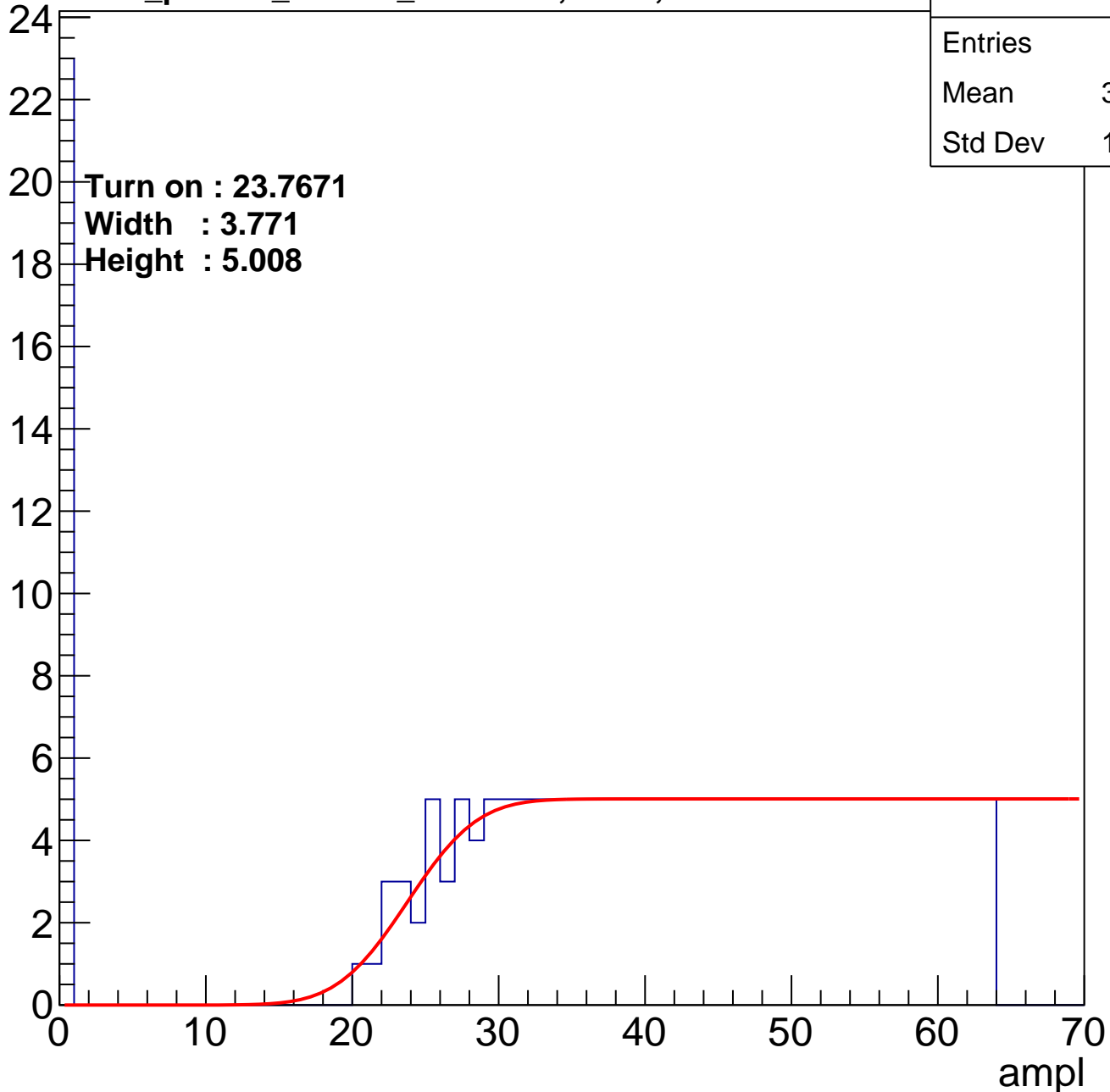


# B1L103S, U15-ch24

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 225   |
| Mean    | 38.77 |
| Std Dev | 17.24 |

Entry



# B1L103S, U15-ch25

calib\_packv5\_041523\_1651.root, FC#0, Port C2

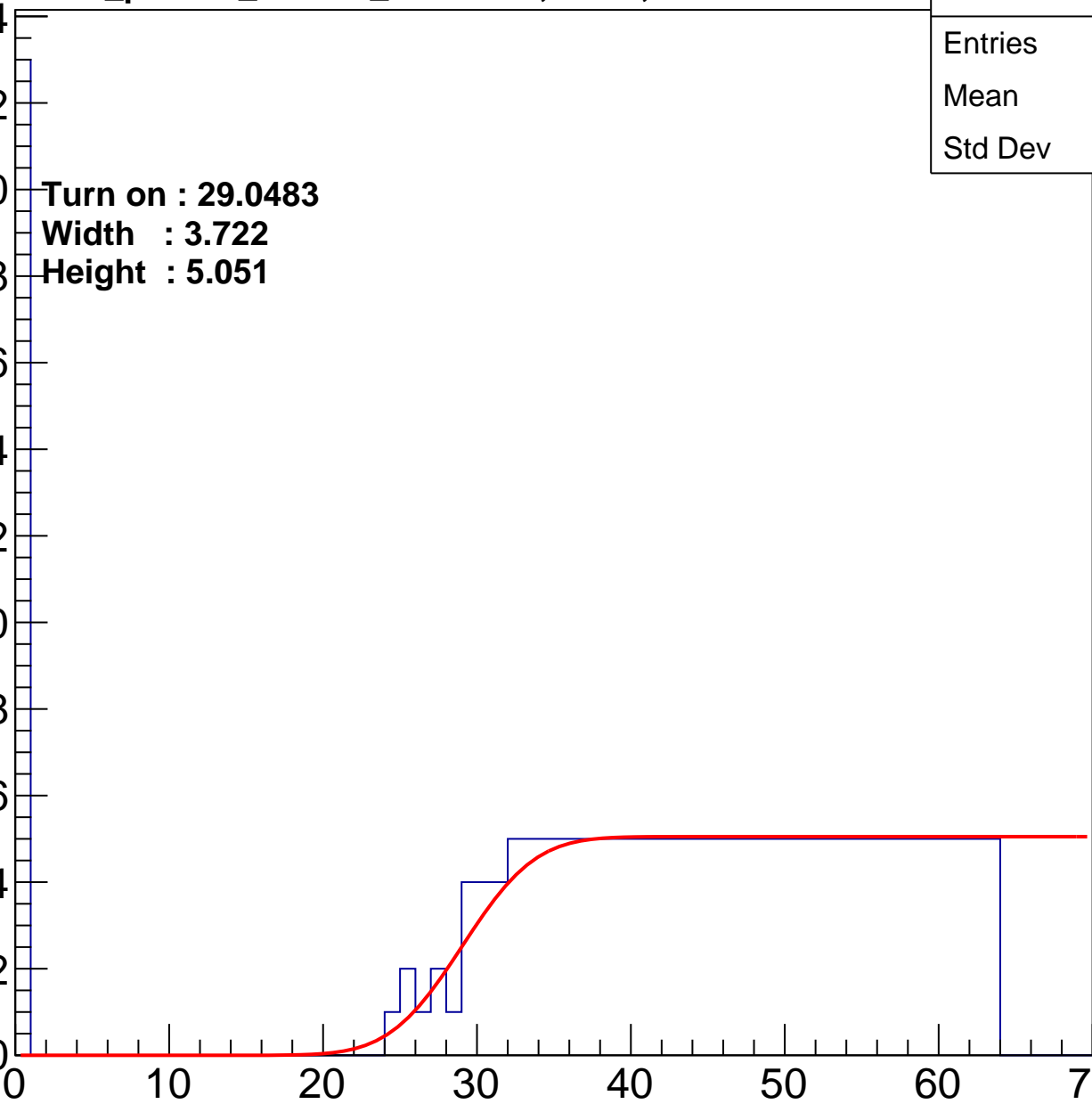
Entry

24  
22  
20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Turn on : 29.0483  
Width : 3.722  
Height : 5.051

|         |       |
|---------|-------|
| Entries | 202   |
| Mean    | 40.31 |
| Std Dev | 17.52 |

ampl



# B1L103S, U15-ch26

calib\_packv5\_041523\_1651.root, FC#0, Port C2

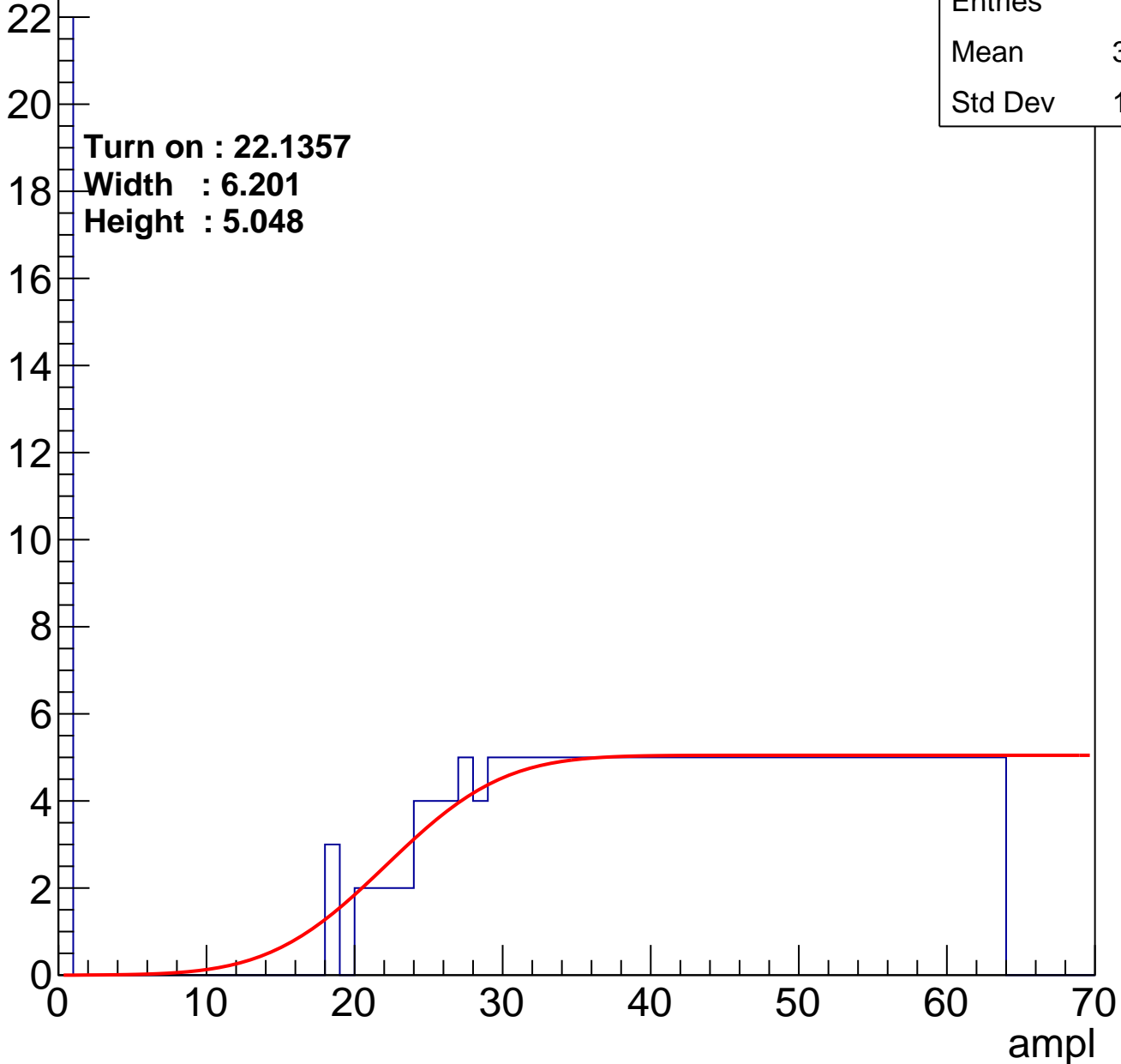
|         |       |
|---------|-------|
| Entries | 229   |
| Mean    | 38.53 |
| Std Dev | 17.13 |

**Turn on : 22.1357**

**Width : 6.201**

**Height : 5.048**

Entry



# B1L103S, U15-ch27

calib\_packv5\_041523\_1651.root, FC#0, Port C2

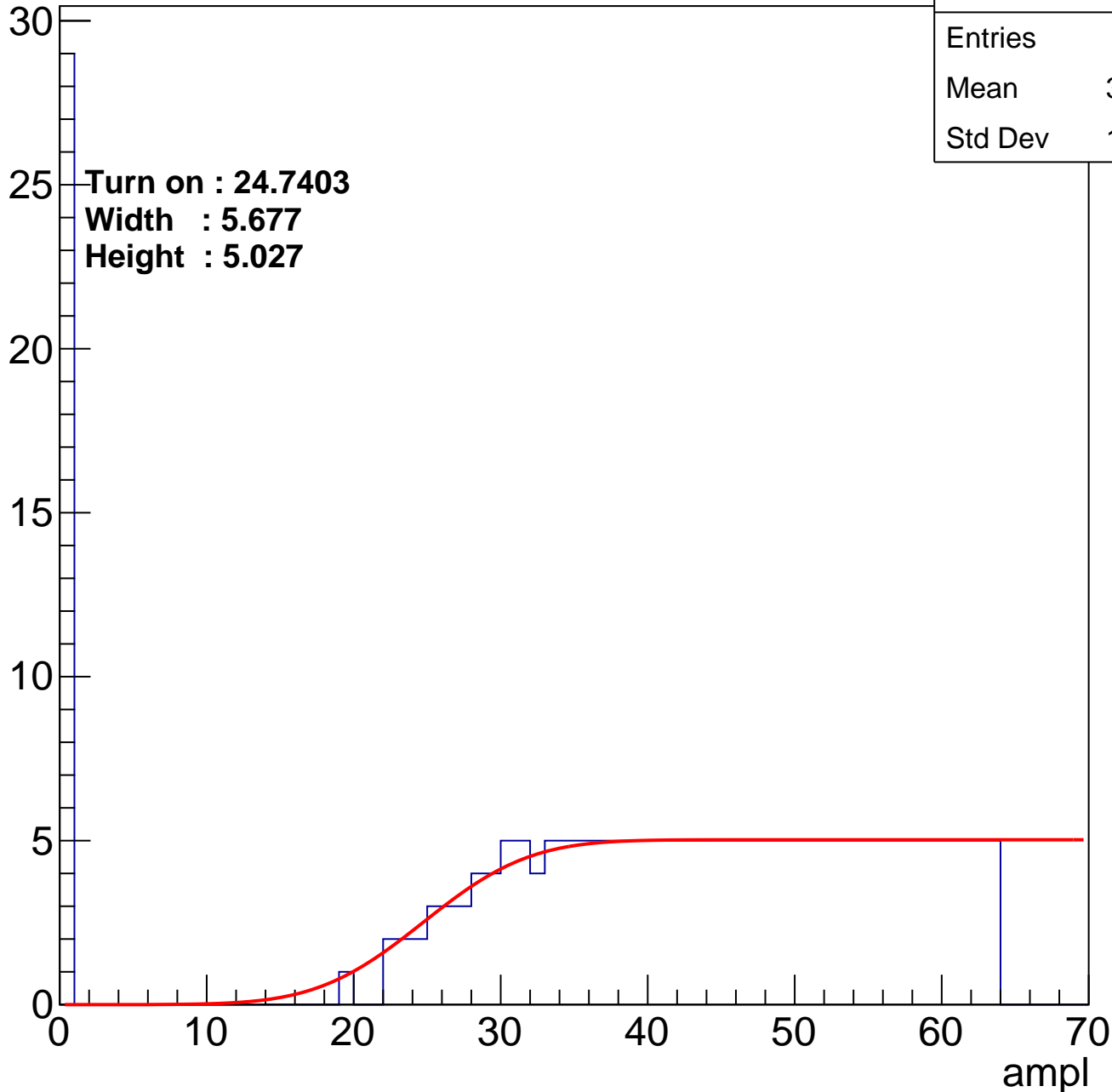
|         |       |
|---------|-------|
| Entries | 222   |
| Mean    | 38.25 |
| Std Dev | 18.28 |

Turn on : 24.7403

Width : 5.677

Height : 5.027

Entry



# B1L103S, U15-ch28

calib\_packv5\_041523\_1651.root, FC#0, Port C2

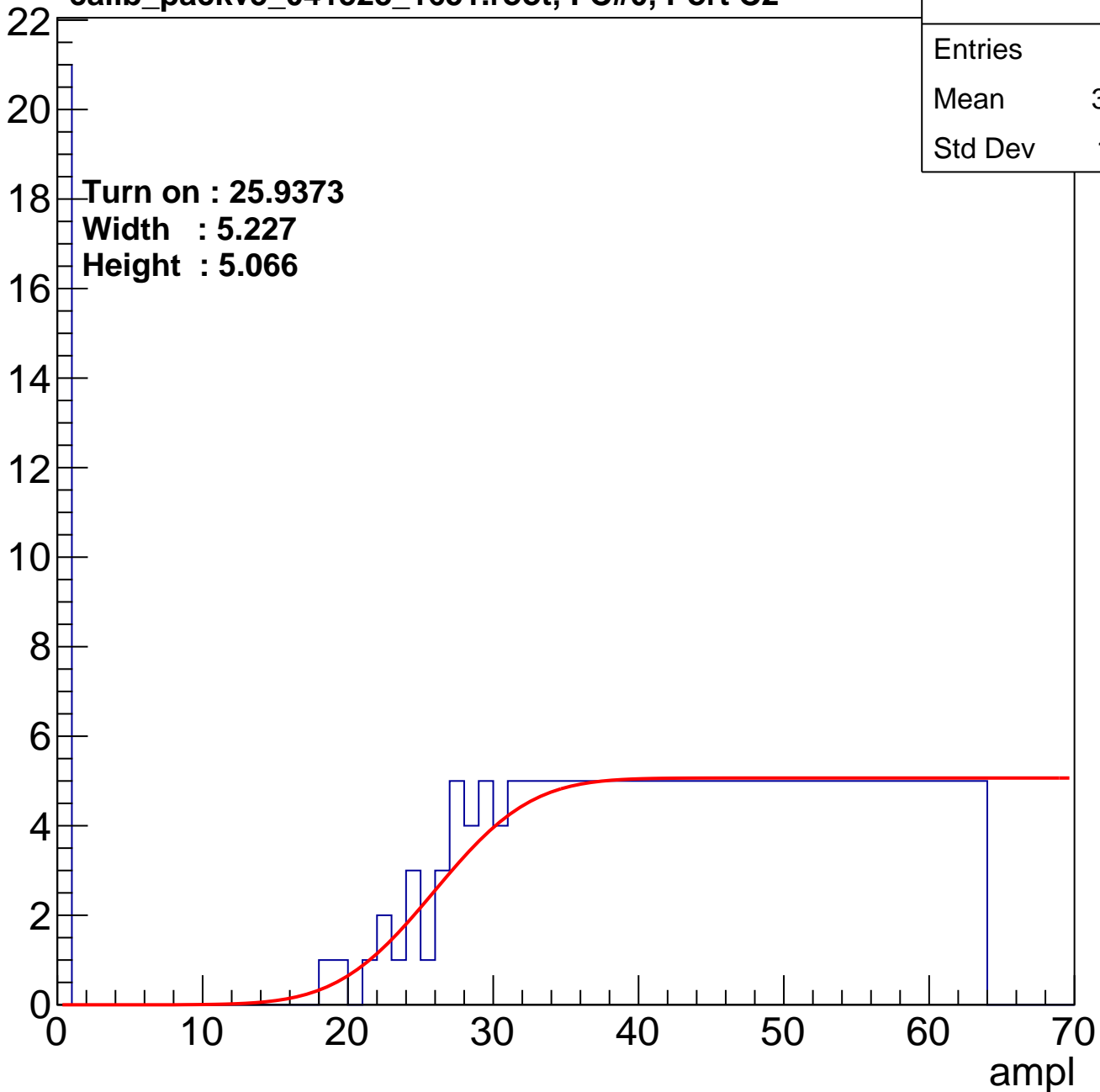
|         |       |
|---------|-------|
| Entries | 217   |
| Mean    | 39.48 |
| Std Dev | 17.01 |

Turn on : 25.9373

Width : 5.227

Height : 5.066

Entry



# B1L103S, U15-ch29

calib\_packv5\_041523\_1651.root, FC#0, Port C2

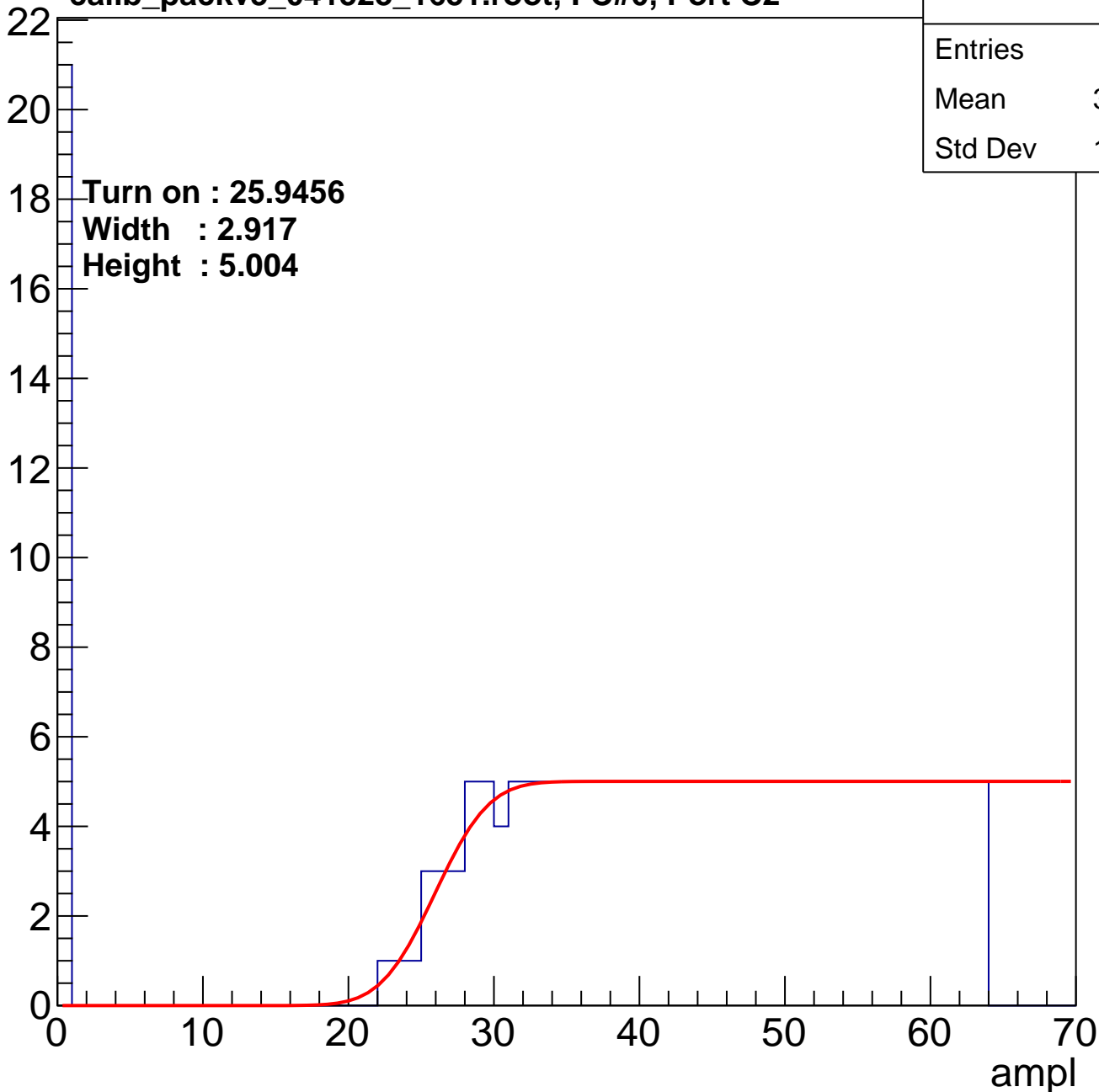
|         |       |
|---------|-------|
| Entries | 212   |
| Mean    | 39.92 |
| Std Dev | 16.96 |

**Turn on : 25.9456**

**Width : 2.917**

**Height : 5.004**

Entry



# B1L103S, U15-ch30

calib\_packv5\_041523\_1651.root, FC#0, Port C2

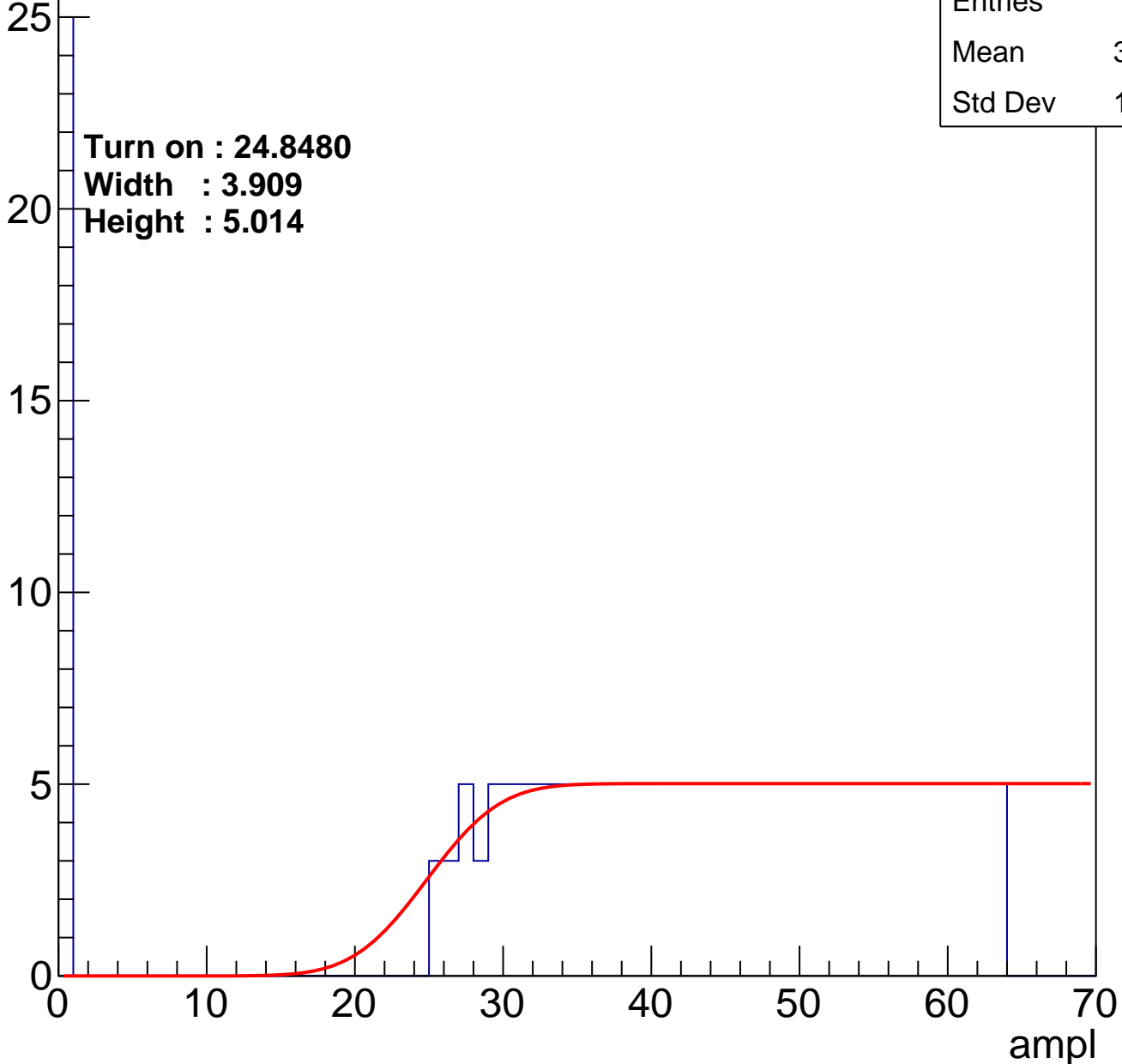
|         |       |
|---------|-------|
| Entries | 214   |
| Mean    | 39.36 |
| Std Dev | 17.64 |

**Turn on : 24.8480**

**Width : 3.909**

**Height : 5.014**

Entry



# B1L103S, U15-ch31

calib\_packv5\_041523\_1651.root, FC#0, Port C2

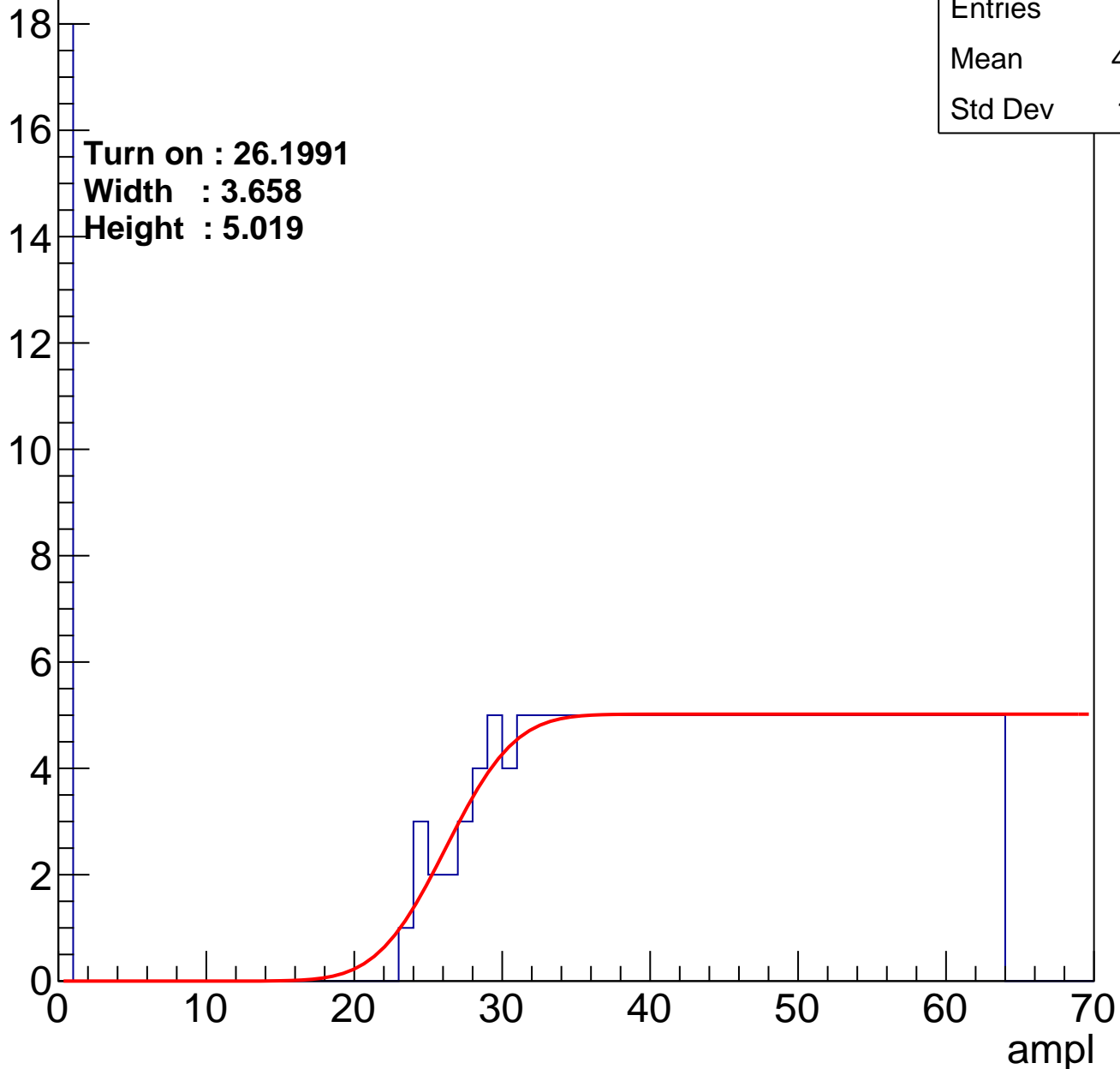
|         |       |
|---------|-------|
| Entries | 207   |
| Mean    | 40.63 |
| Std Dev | 16.41 |

**Turn on : 26.1991**

**Width : 3.658**

**Height : 5.019**

Entry





# B1L103S, U15-ch32

calib\_packv5\_041523\_1651.root, FC#0, Port C2

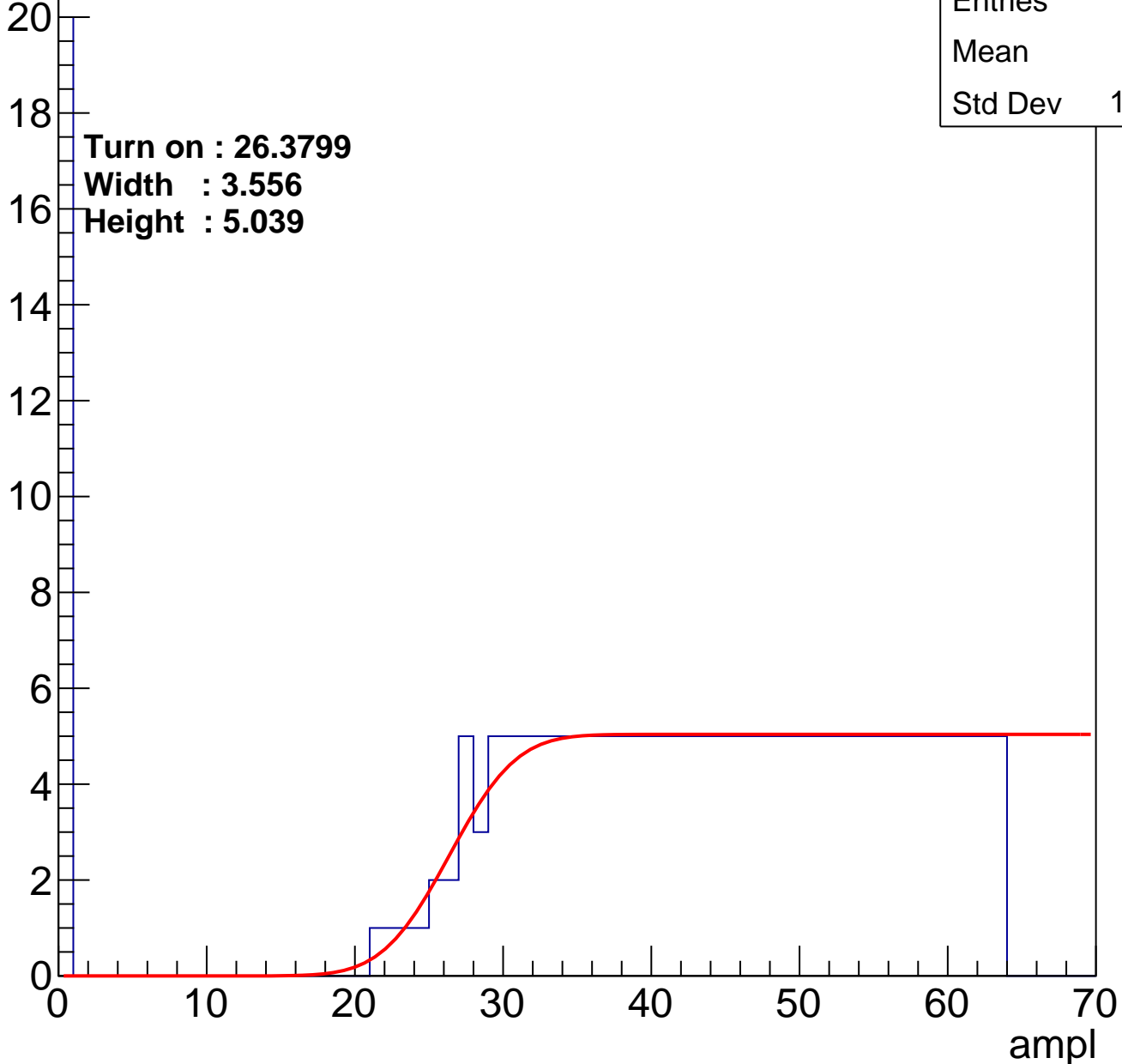
|         |       |
|---------|-------|
| Entries | 211   |
| Mean    | 40.1  |
| Std Dev | 16.79 |

**Turn on : 26.3799**

**Width : 3.556**

**Height : 5.039**

Entry



# B1L103S, U15-ch33

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 218   |
| Mean    | 38.88 |
| Std Dev | 17.83 |

**Turn on : 25.4925**

**Width : 4.494**

**Height : 5.025**

Entry

25

20

15

10

5

0

0

10

20

30

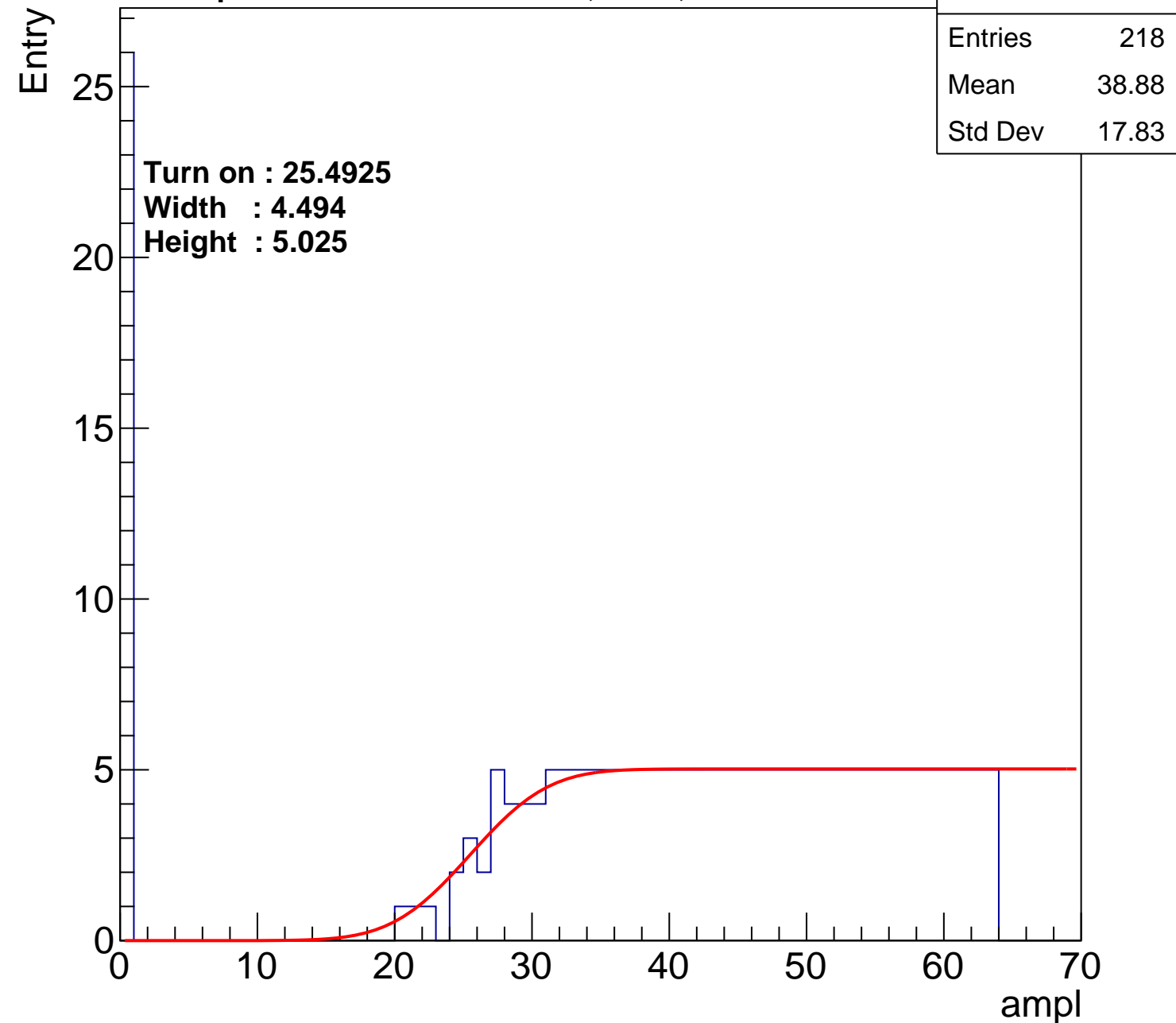
40

50

60

70

ampl

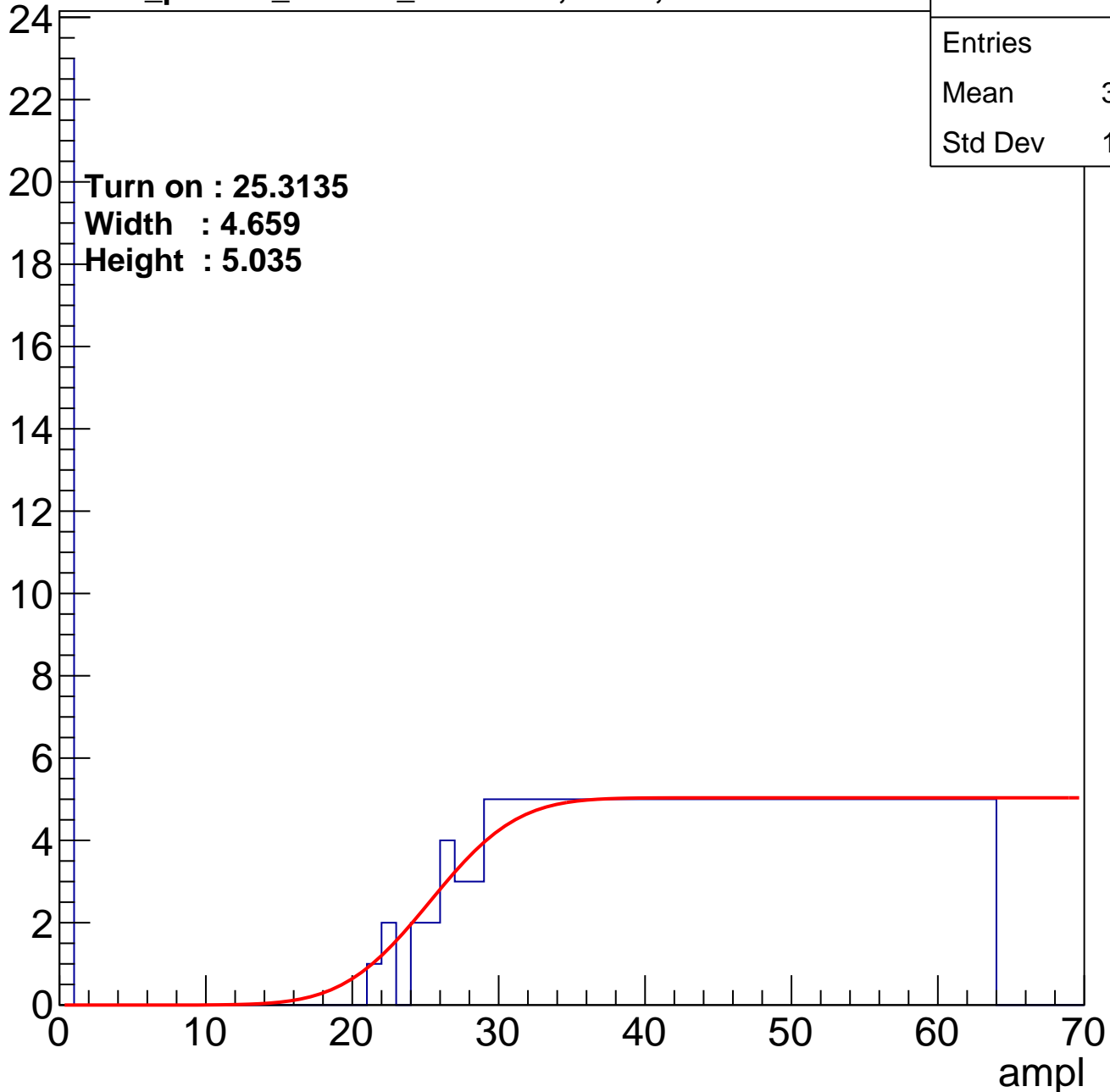


# B1L103S, U15-ch34

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 215   |
| Mean    | 39.45 |
| Std Dev | 17.33 |

Entry

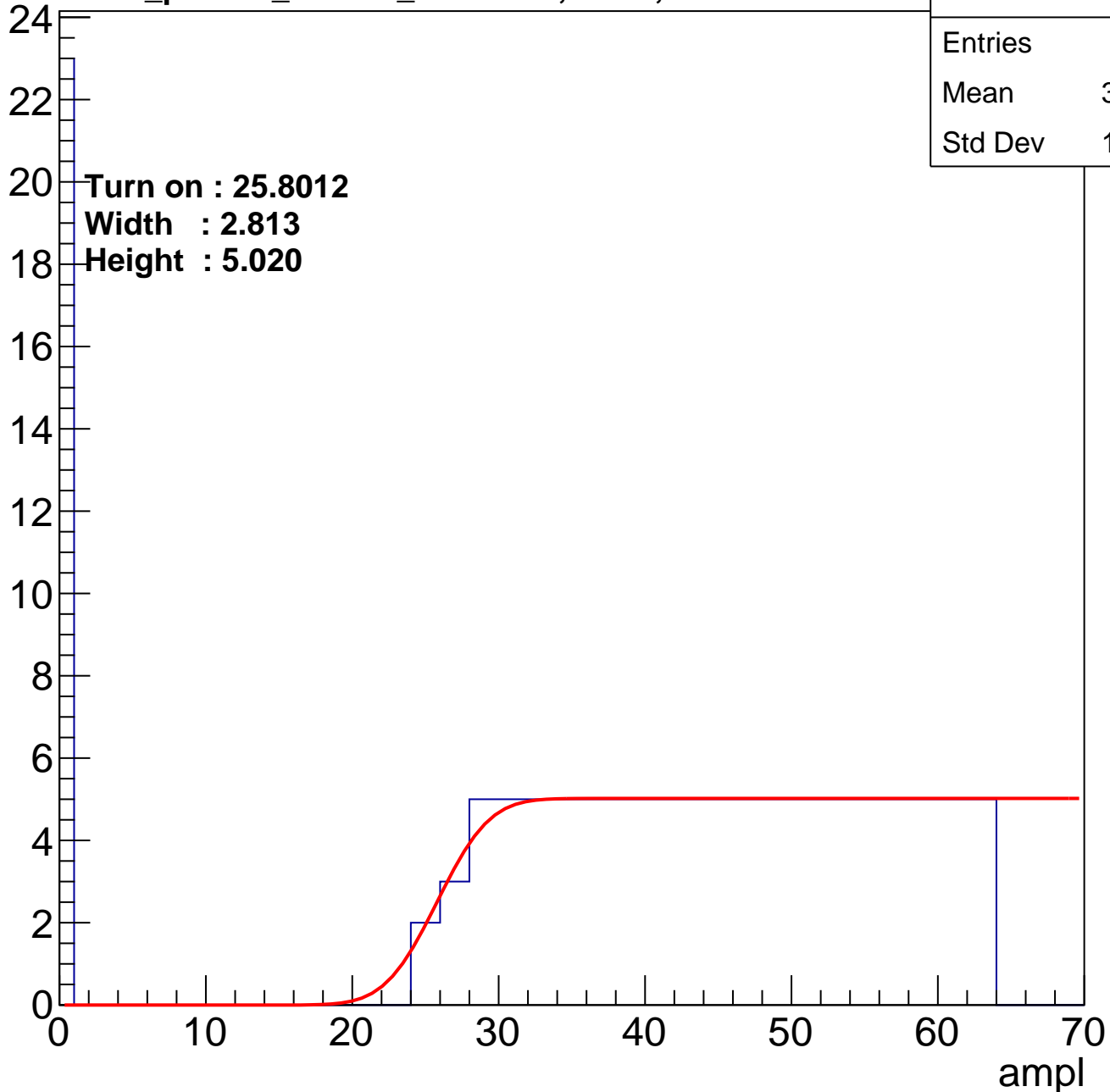


# B1L103S, U15-ch35

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 213   |
| Mean    | 39.66 |
| Std Dev | 17.29 |

Entry



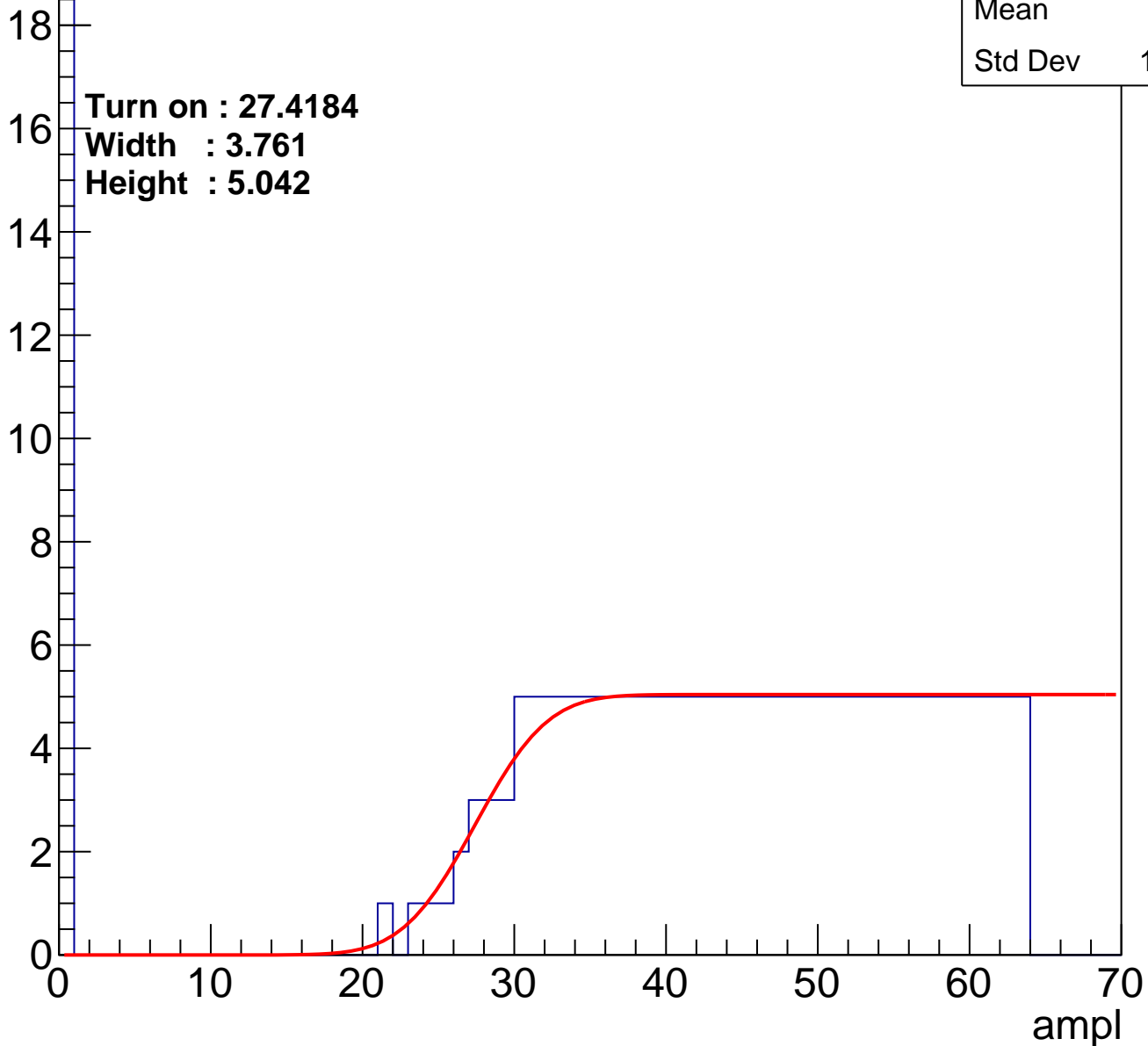
# B1L103S, U15-ch36

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 204   |
| Mean    | 40.7  |
| Std Dev | 16.67 |

**Turn on : 27.4184**  
**Width : 3.761**  
**Height : 5.042**

Entry



# B1L103S, U15-ch37

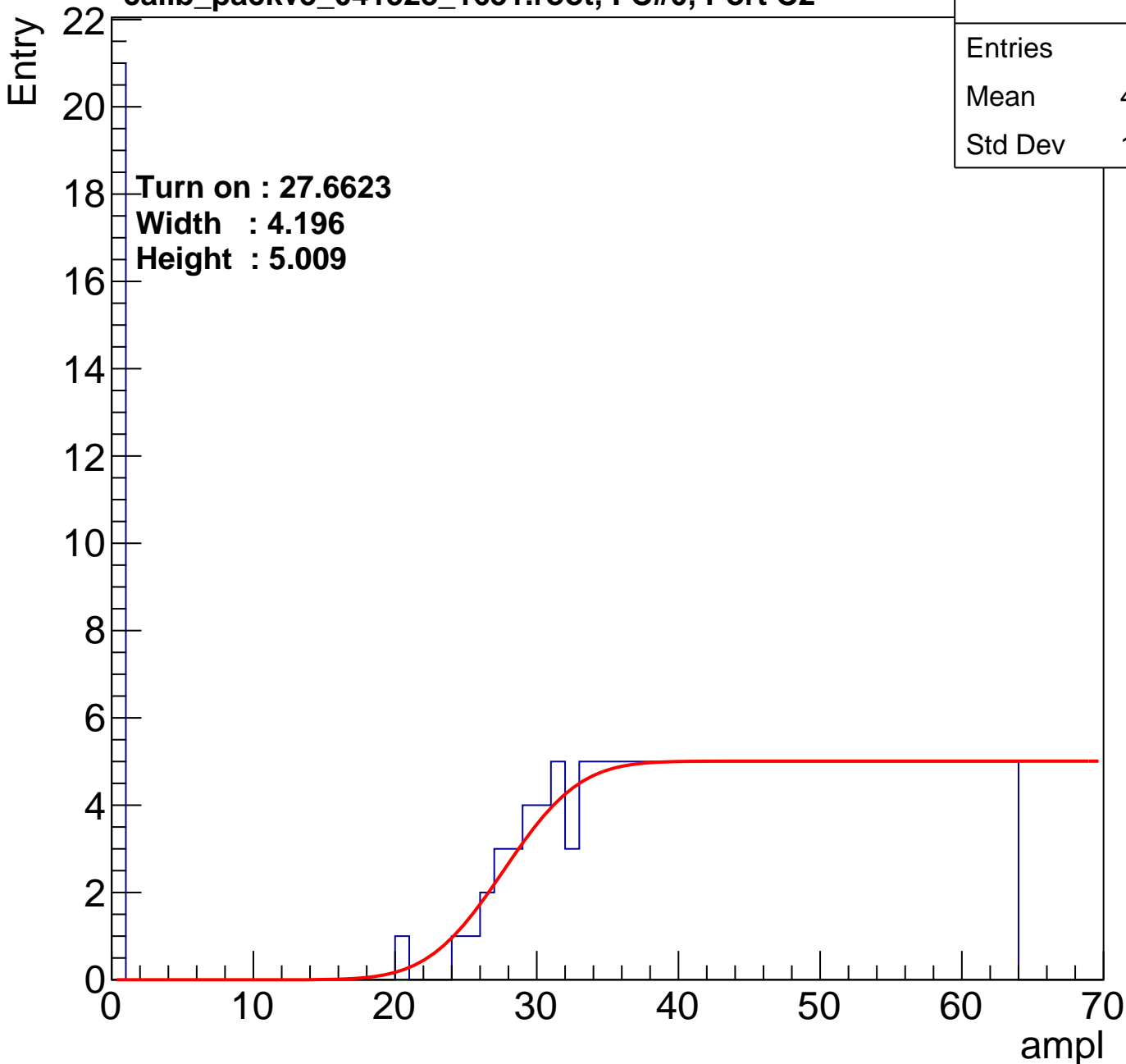
calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 203   |
| Mean    | 40.46 |
| Std Dev | 17.13 |

Turn on : 27.6623

Width : 4.196

Height : 5.009

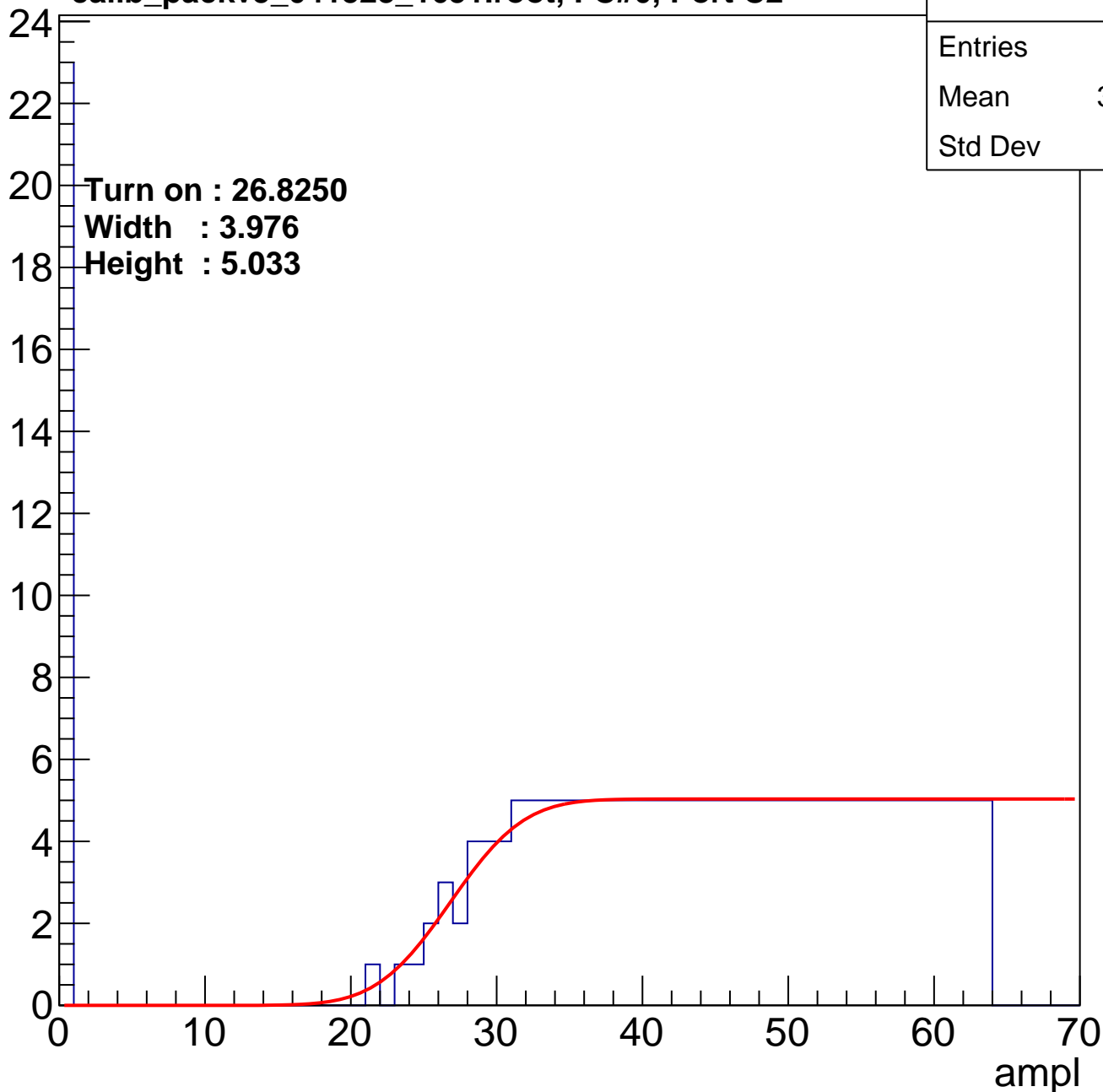


# B1L103S, U15-ch38

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 210   |
| Mean    | 39.78 |
| Std Dev | 17.4  |

Entry



# B1L103S, U15-ch39

calib\_packv5\_041523\_1651.root, FC#0, Port C2

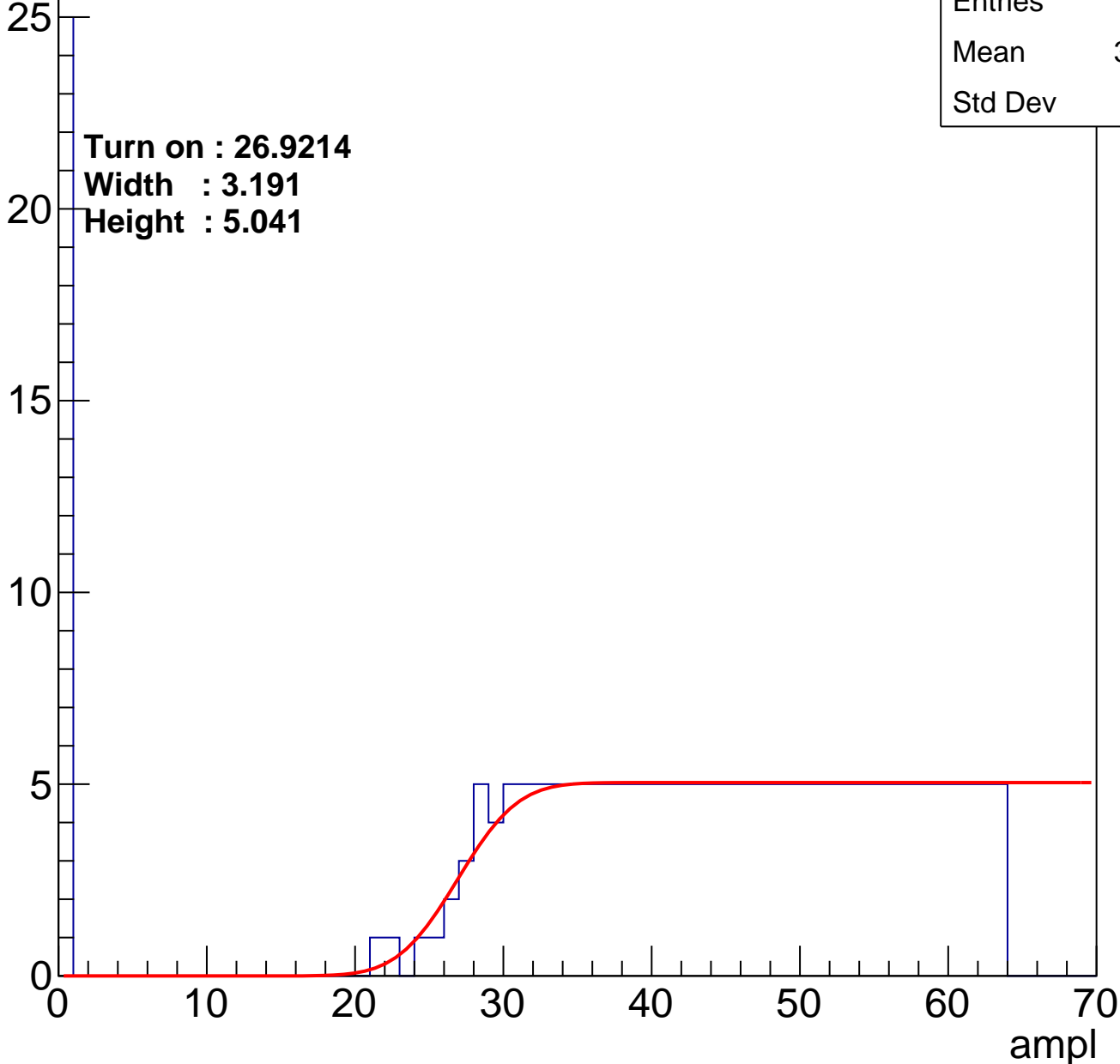
|         |       |
|---------|-------|
| Entries | 213   |
| Mean    | 39.37 |
| Std Dev | 17.7  |

Turn on : 26.9214

Width : 3.191

Height : 5.041

Entry





# B1L103S, U15-ch40

calib\_packv5\_041523\_1651.root, FC#0, Port C2

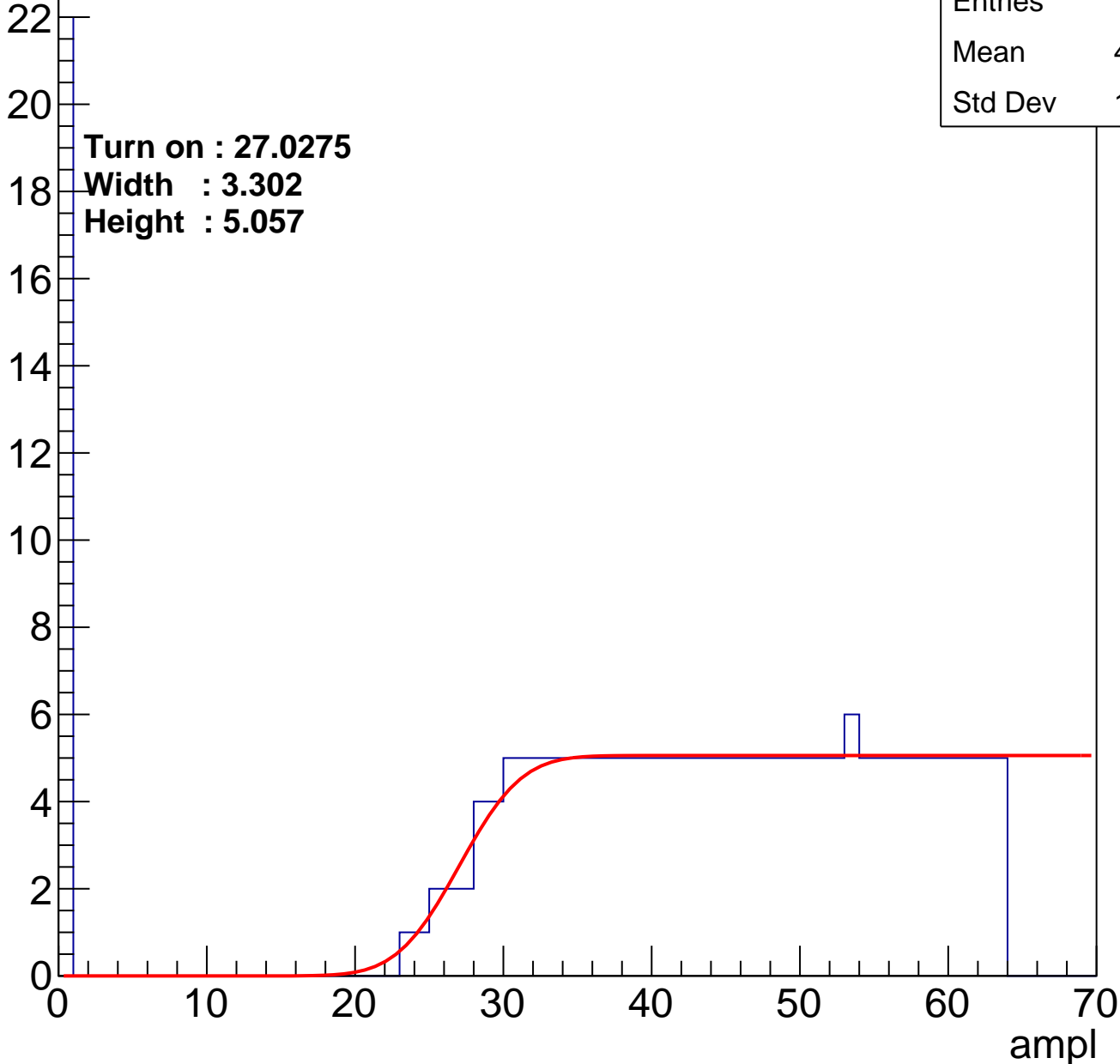
|         |       |
|---------|-------|
| Entries | 209   |
| Mean    | 40.14 |
| Std Dev | 17.18 |

**Turn on : 27.0275**

**Width : 3.302**

**Height : 5.057**

Entry



# B1L103S, U15-ch41

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 217   |
| Mean    | 39.01 |
| Std Dev | 17.8  |

**Turn on : 26.1277**

**Width : 2.960**

**Height : 5.026**

Entry

25

20

15

10

5

0

0

10

20

30

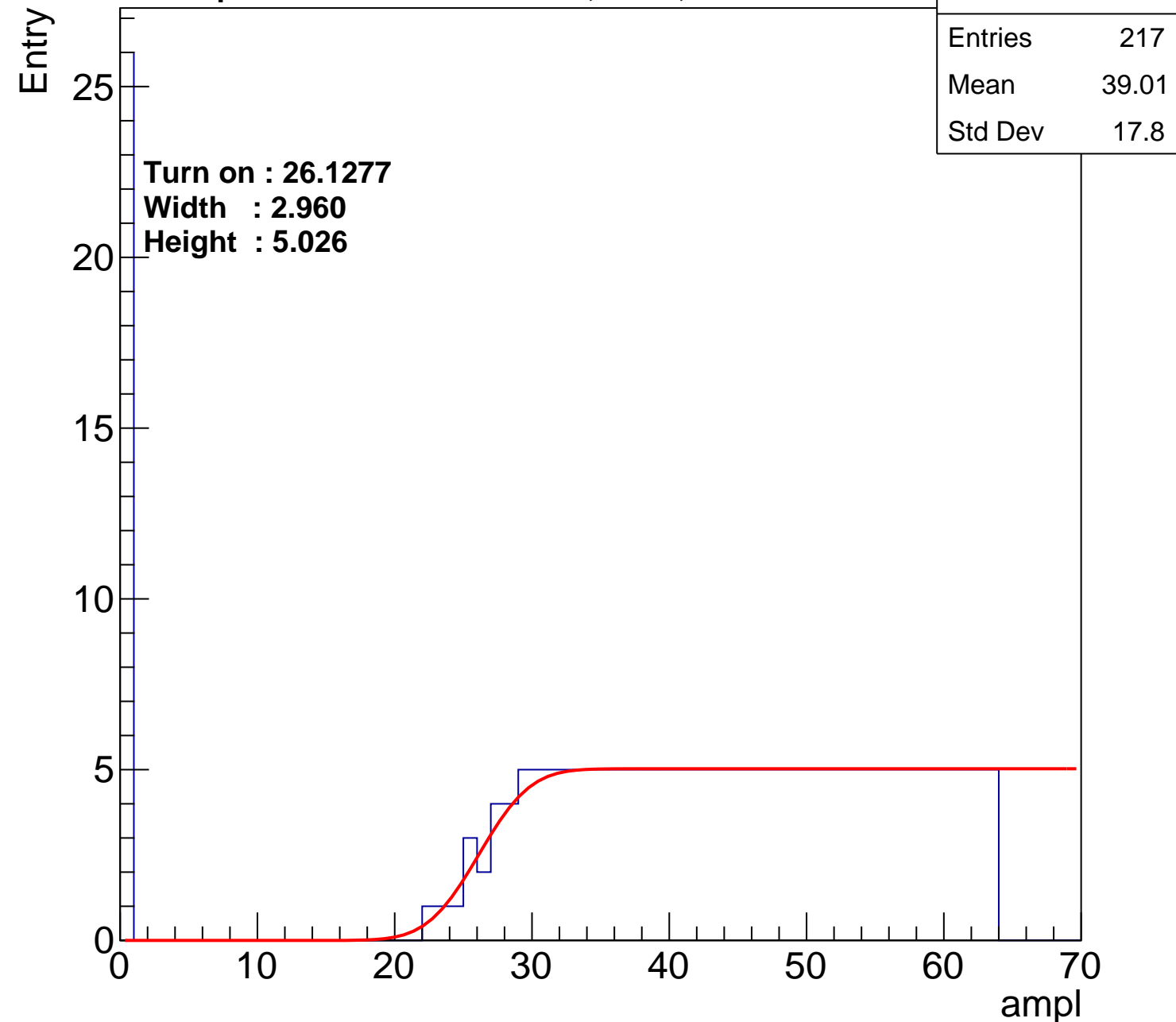
40

50

60

70

ampl



# B1L103S, U15-ch42

calib\_packv5\_041523\_1651.root, FC#0, Port C2

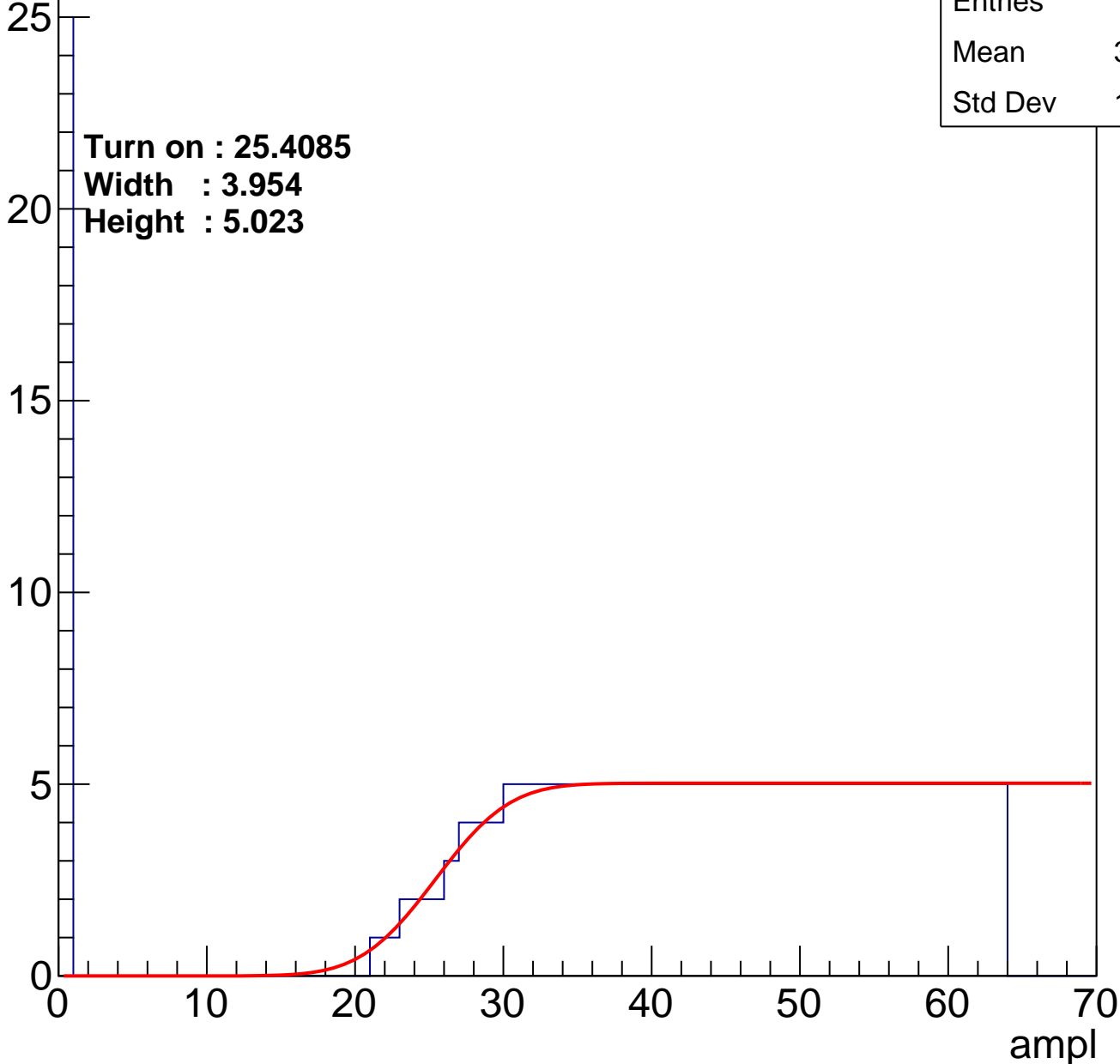
|         |       |
|---------|-------|
| Entries | 218   |
| Mean    | 39.02 |
| Std Dev | 17.65 |

**Turn on : 25.4085**

**Width : 3.954**

**Height : 5.023**

Entry



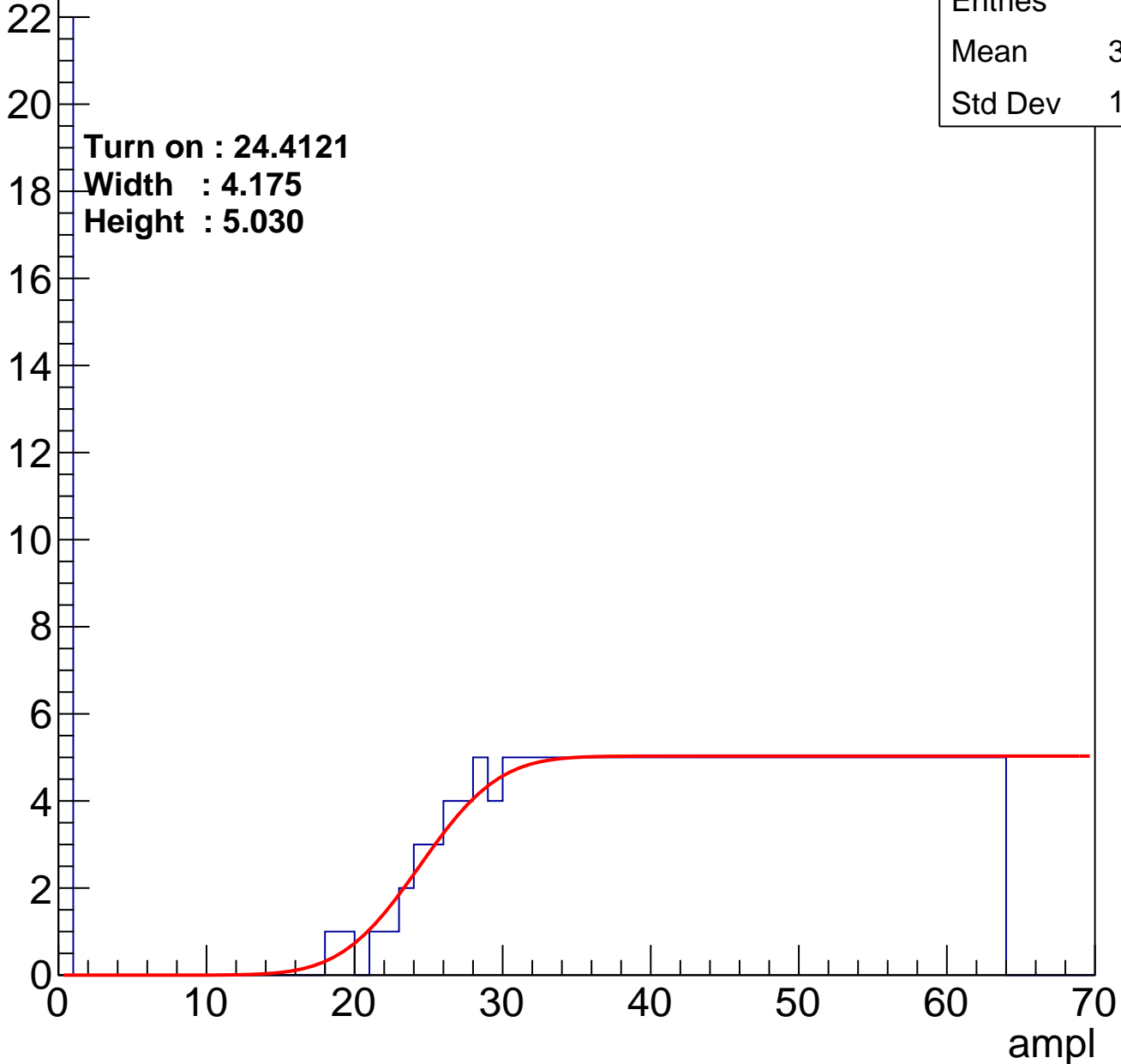
# B1L103S, U15-ch43

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 221   |
| Mean    | 39.12 |
| Std Dev | 17.13 |

**Turn on : 24.4121**  
**Width : 4.175**  
**Height : 5.030**

Entry



# B1L103S, U15-ch44

calib\_packv5\_041523\_1651.root, FC#0, Port C2

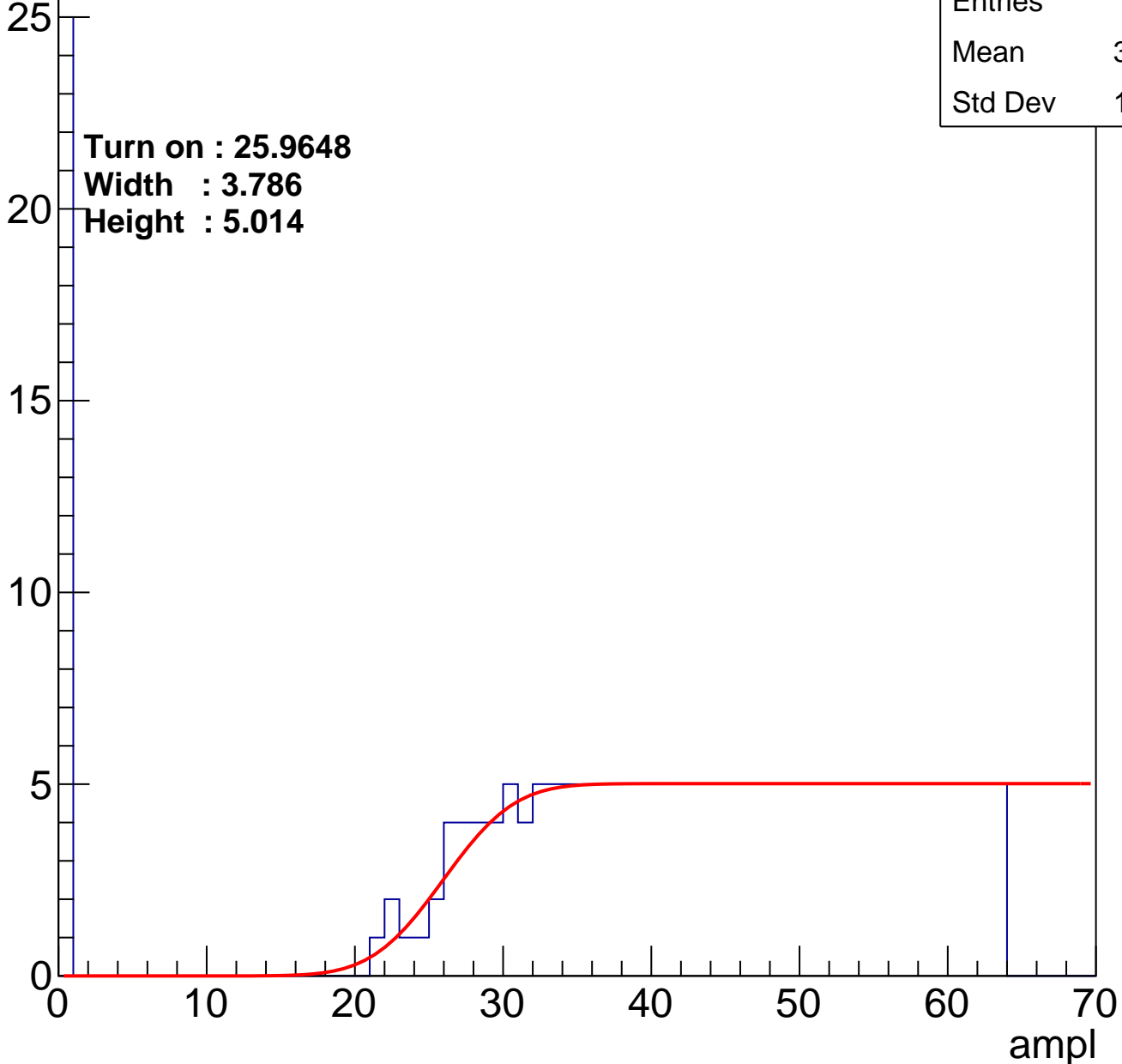
|         |       |
|---------|-------|
| Entries | 217   |
| Mean    | 39.06 |
| Std Dev | 17.68 |

**Turn on : 25.9648**

**Width : 3.786**

**Height : 5.014**

Entry



# B1L103S, U15-ch45

calib\_packv5\_041523\_1651.root, FC#0, Port C2

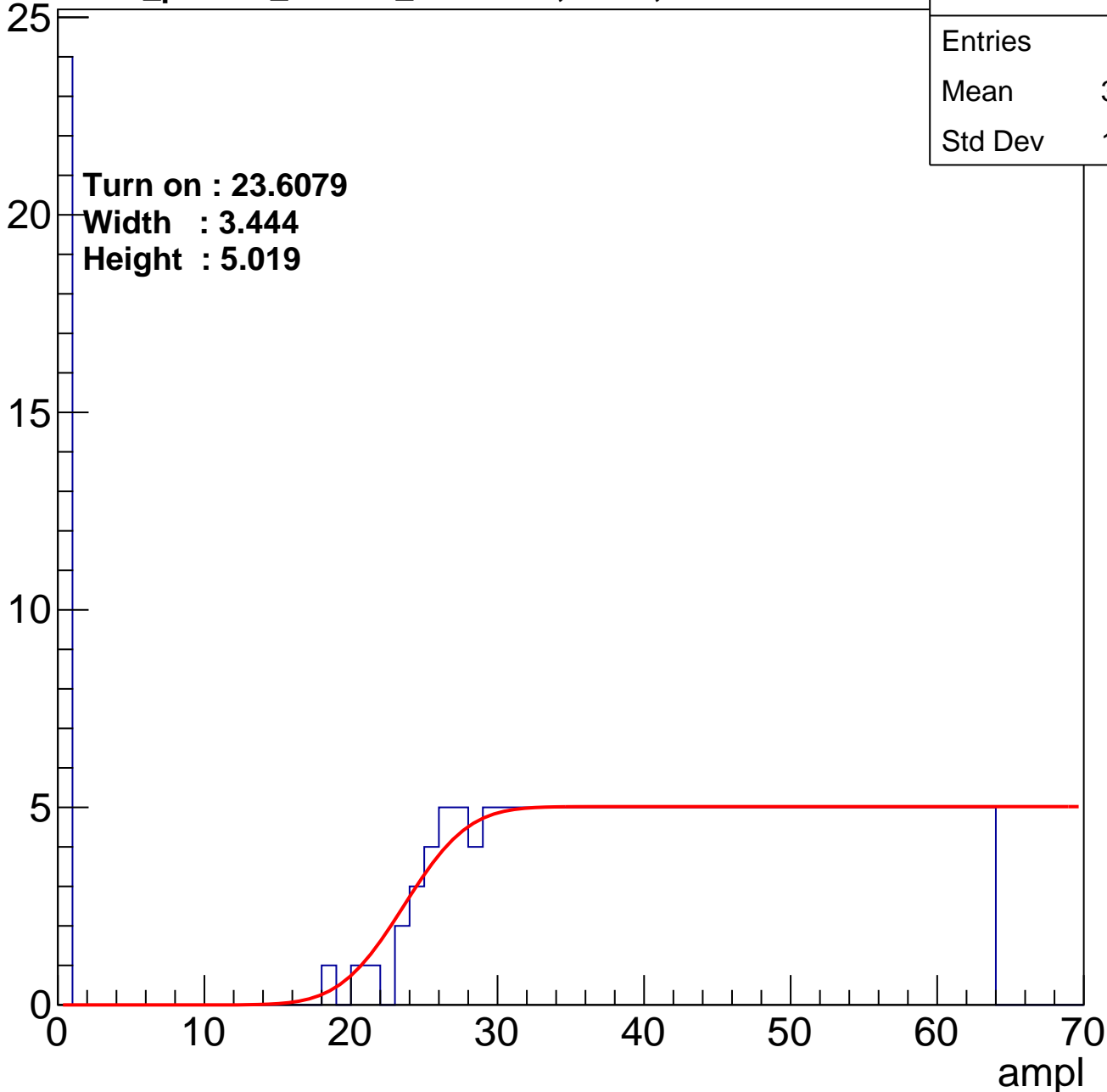
|         |       |
|---------|-------|
| Entries | 225   |
| Mean    | 38.68 |
| Std Dev | 17.39 |

Turn on : 23.6079

Width : 3.444

Height : 5.019

Entry



# B1L103S, U15-ch46

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 221   |
| Mean    | 38.71 |
| Std Dev | 17.77 |

**Turn on : 24.8973**

**Width : 3.621**

**Height : 4.990**

Entry

25

20

15

10

5

0

0

10

20

30

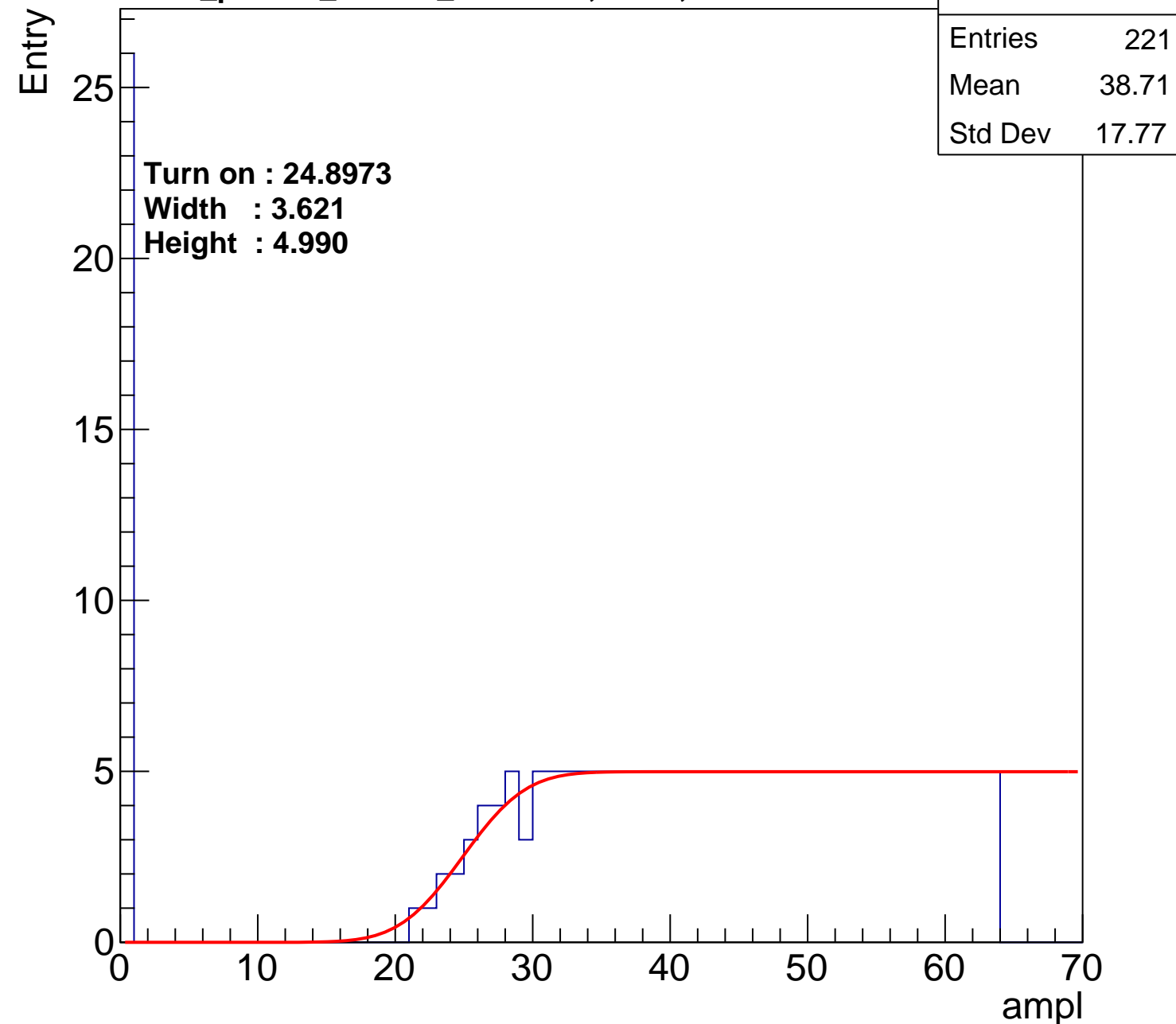
40

50

60

70

ampl



# B1L103S, U15-ch47

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 212   |
| Mean    | 39.31 |
| Std Dev | 17.9  |

**Turn on : 26.9223**

**Width : 3.491**

**Height : 5.034**

Entry

25

20

15

10

5

0

0

10

20

30

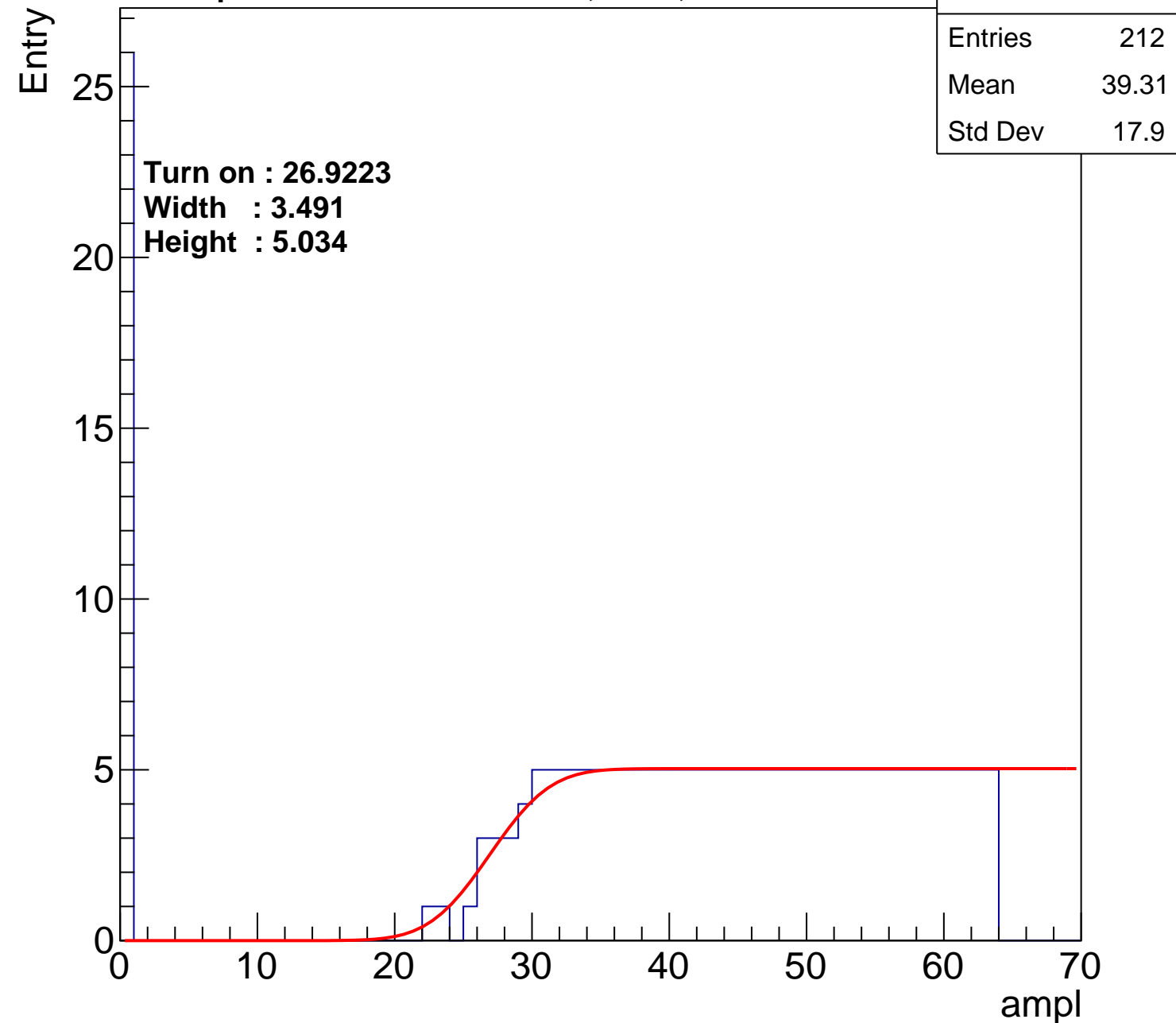
40

50

60

70

ampl





# B1L103S, U15-ch48

calib\_packv5\_041523\_1651.root, FC#0, Port C2

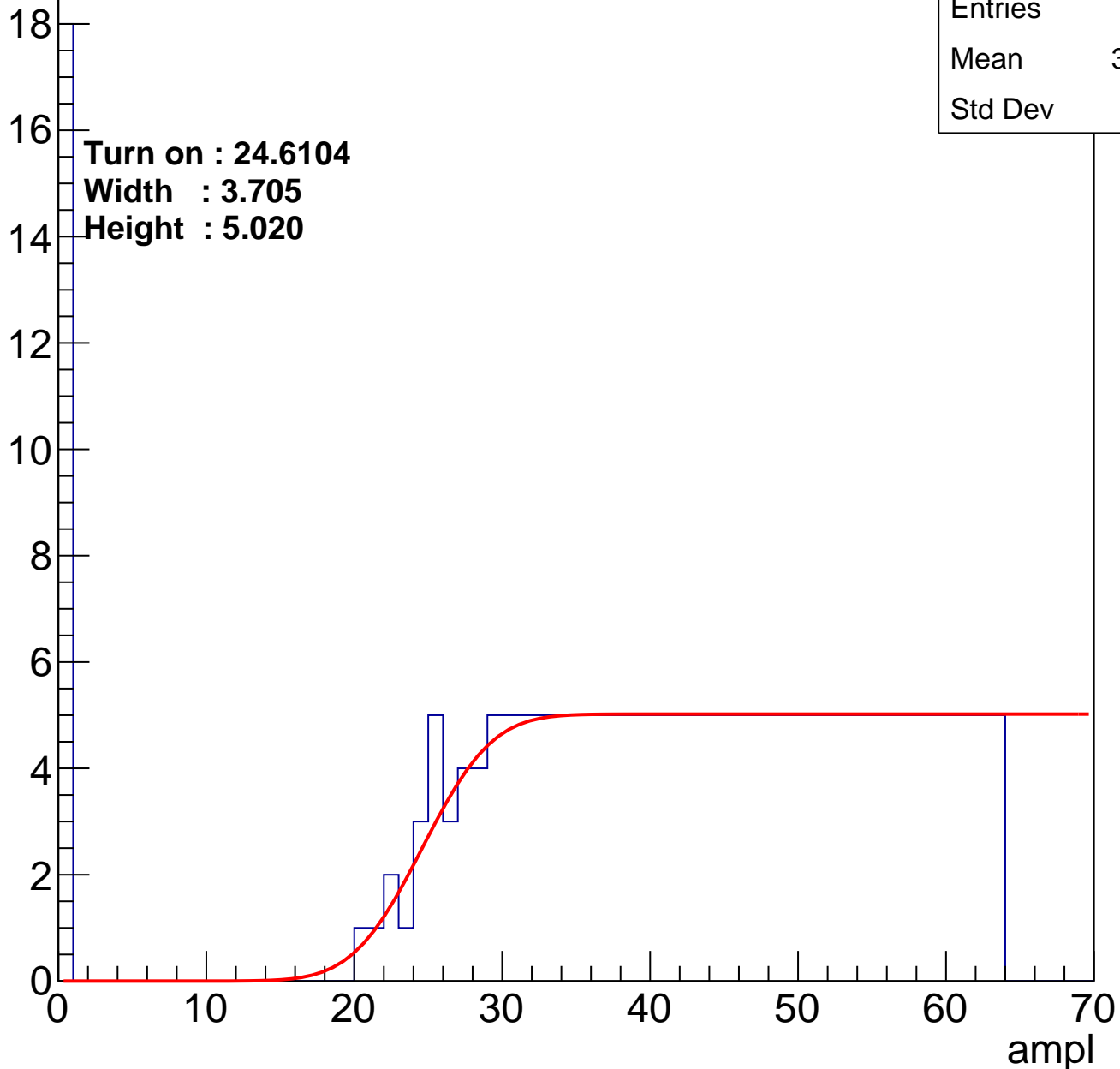
|         |       |
|---------|-------|
| Entries | 217   |
| Mean    | 39.88 |
| Std Dev | 16.4  |

Turn on : 24.6104

Width : 3.705

Height : 5.020

Entry



# B1L103S, U15-ch49

calib\_packv5\_041523\_1651.root, FC#0, Port C2

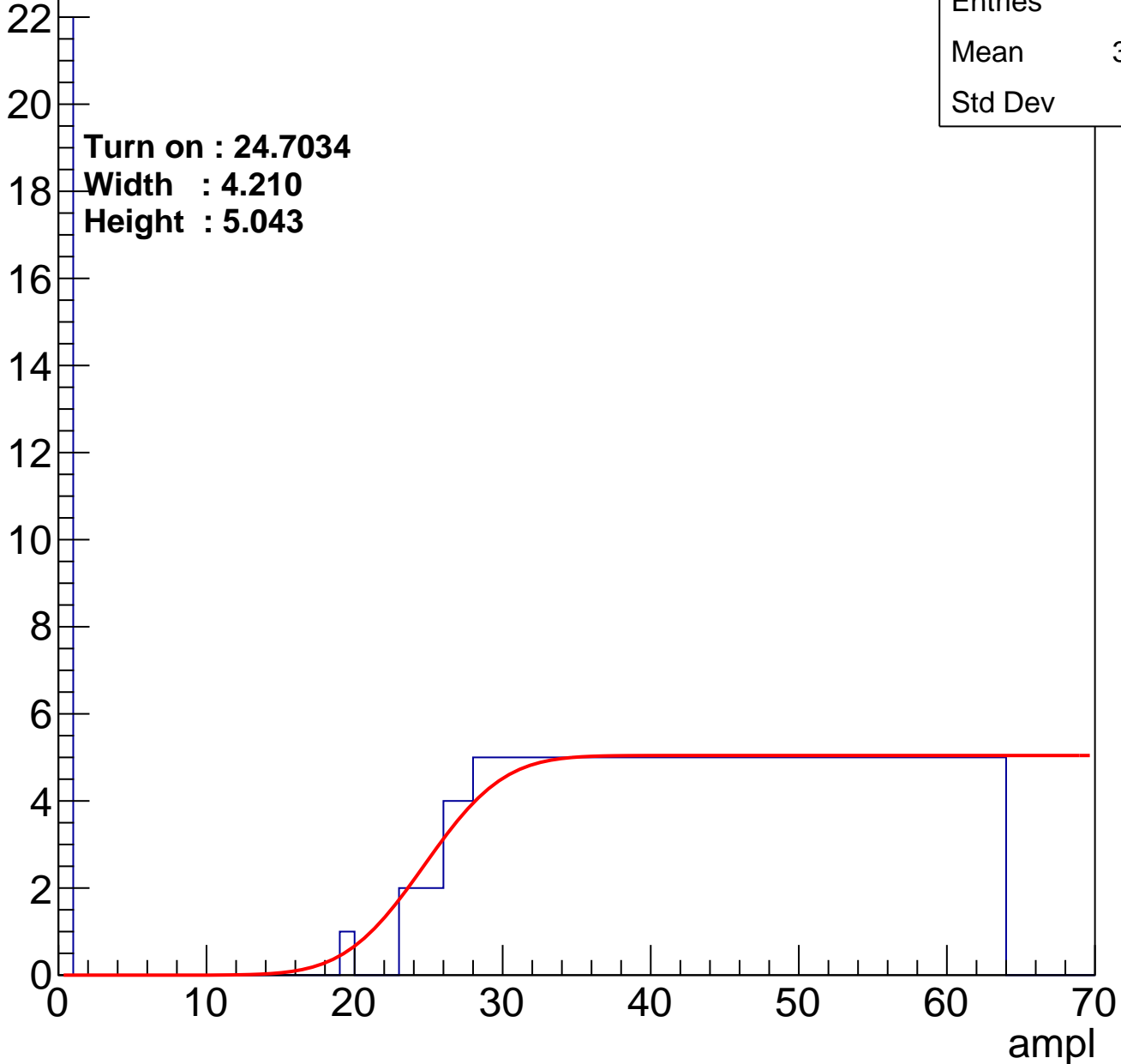
|         |       |
|---------|-------|
| Entries | 217   |
| Mean    | 39.47 |
| Std Dev | 17.1  |

**Turn on : 24.7034**

**Width : 4.210**

**Height : 5.043**

Entry



# B1L103S, U15-ch50

calib\_packv5\_041523\_1651.root, FC#0, Port C2

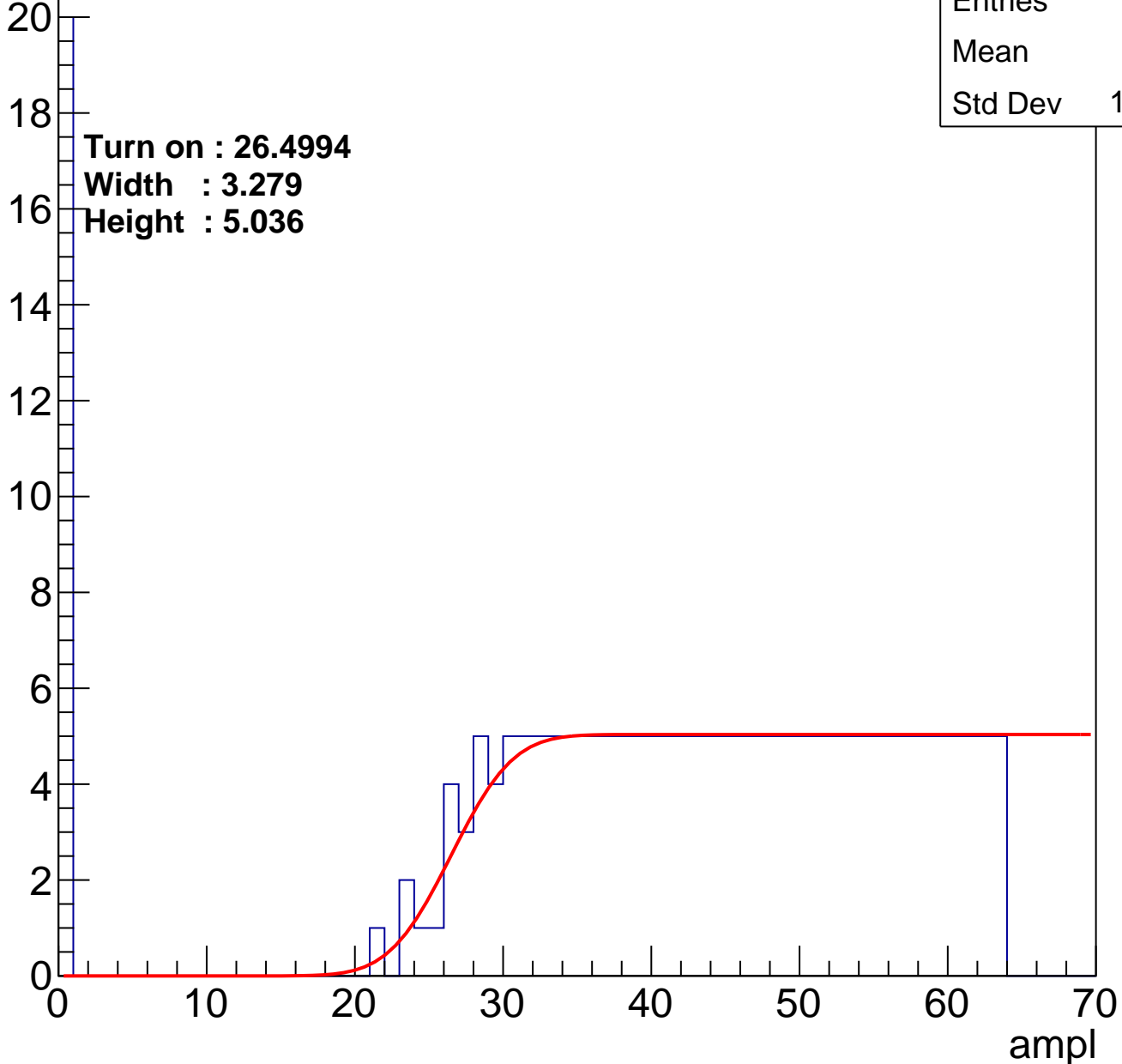
|         |       |
|---------|-------|
| Entries | 211   |
| Mean    | 40.1  |
| Std Dev | 16.79 |

**Turn on : 26.4994**

**Width : 3.279**

**Height : 5.036**

Entry



# B1L103S, U15-ch51

calib\_packv5\_041523\_1651.root, FC#0, Port C2

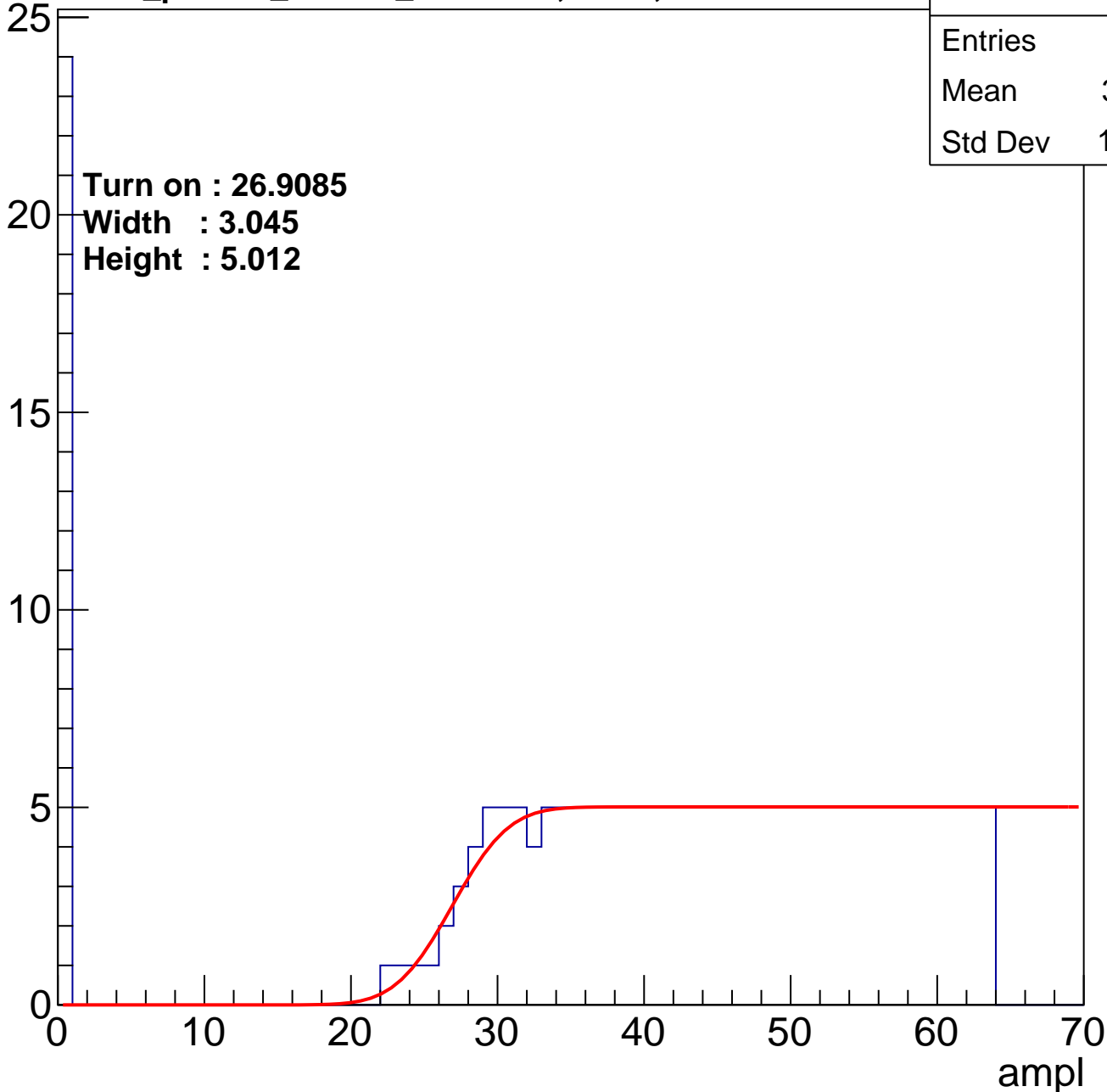
|         |       |
|---------|-------|
| Entries | 211   |
| Mean    | 39.61 |
| Std Dev | 17.55 |

Turn on : 26.9085

Width : 3.045

Height : 5.012

Entry



# B1L103S, U15-ch52

calib\_packv5\_041523\_1651.root, FC#0, Port C2

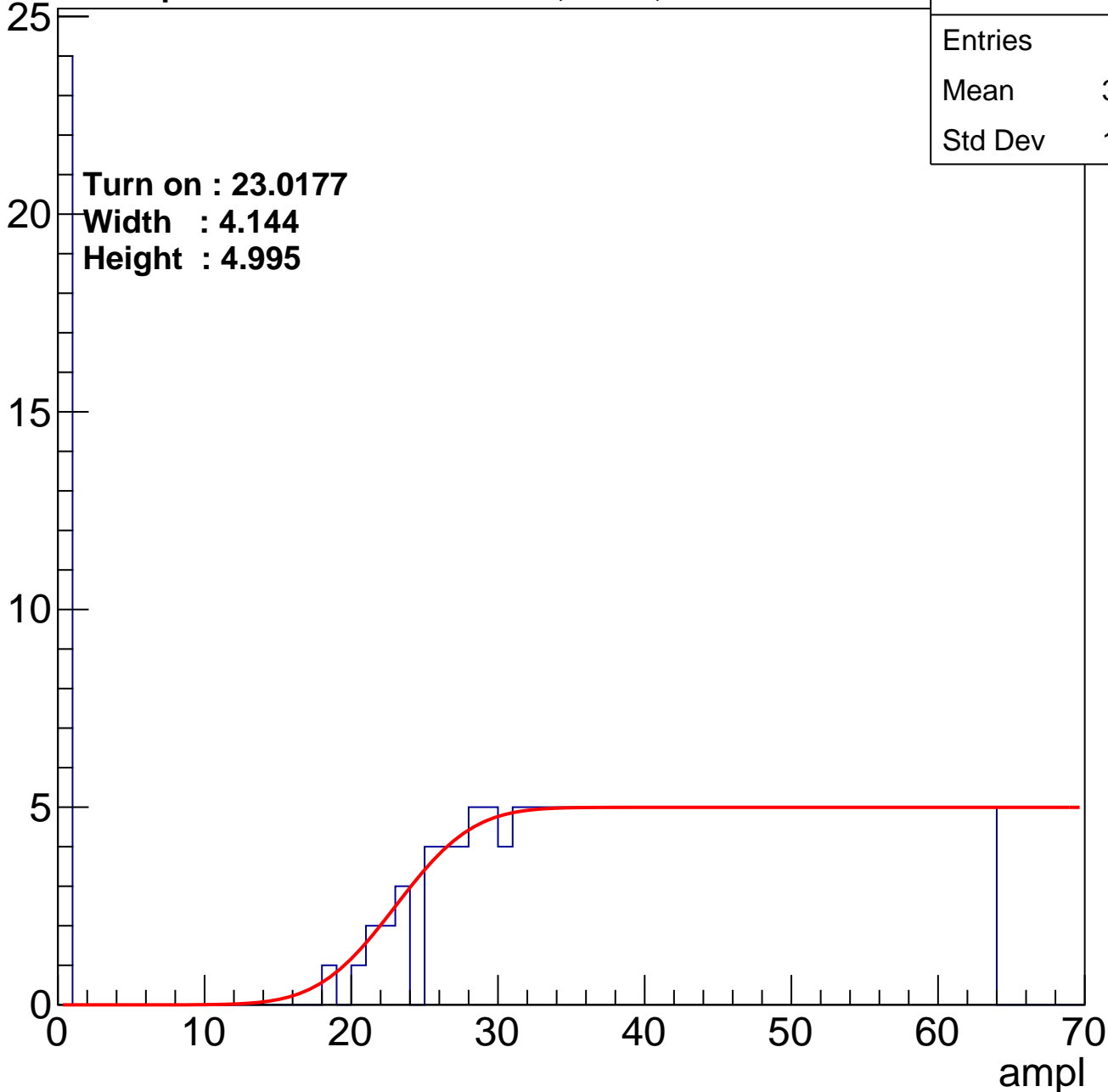
|         |       |
|---------|-------|
| Entries | 224   |
| Mean    | 38.68 |
| Std Dev | 17.46 |

Turn on : 23.0177

Width : 4.144

Height : 4.995

Entry



# B1L103S, U15-ch53

calib\_packv5\_041523\_1651.root, FC#0, Port C2

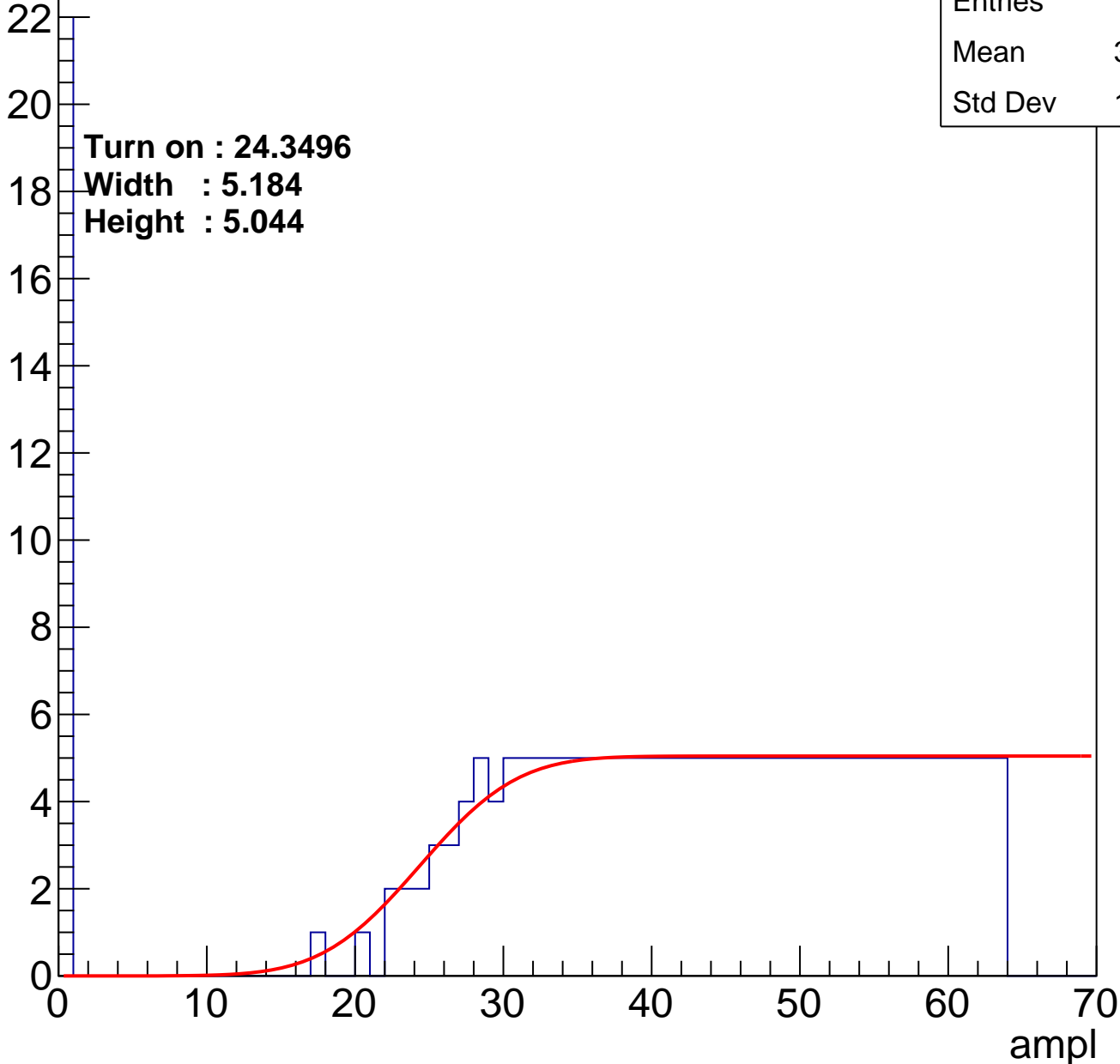
|         |       |
|---------|-------|
| Entries | 219   |
| Mean    | 39.26 |
| Std Dev | 17.15 |

**Turn on : 24.3496**

**Width : 5.184**

**Height : 5.044**

Entry

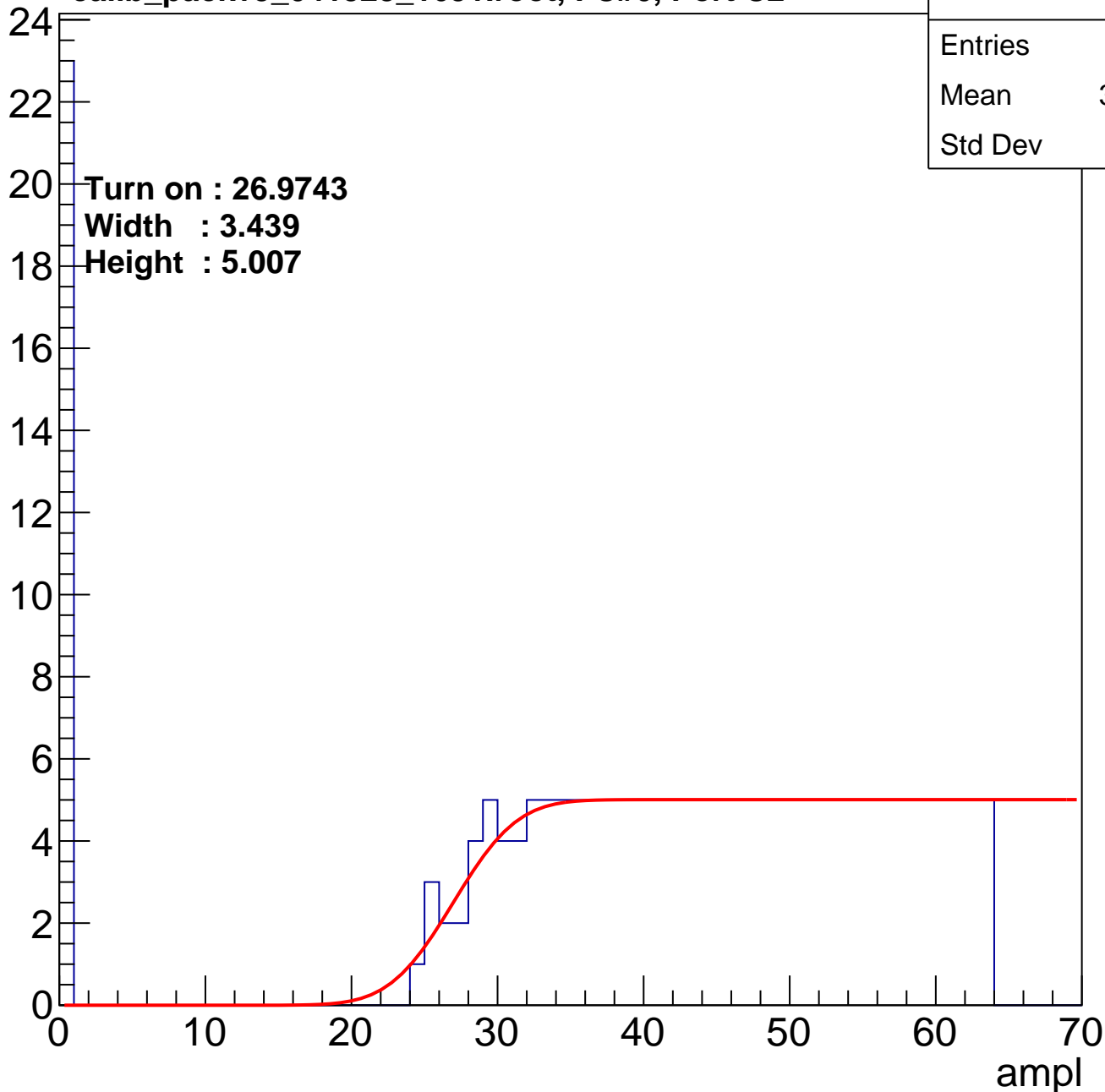


# B1L103S, U15-ch54

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 208   |
| Mean    | 39.93 |
| Std Dev | 17.4  |

Entry



# B1L103S, U15-ch55

calib\_packv5\_041523\_1651.root, FC#0, Port C2

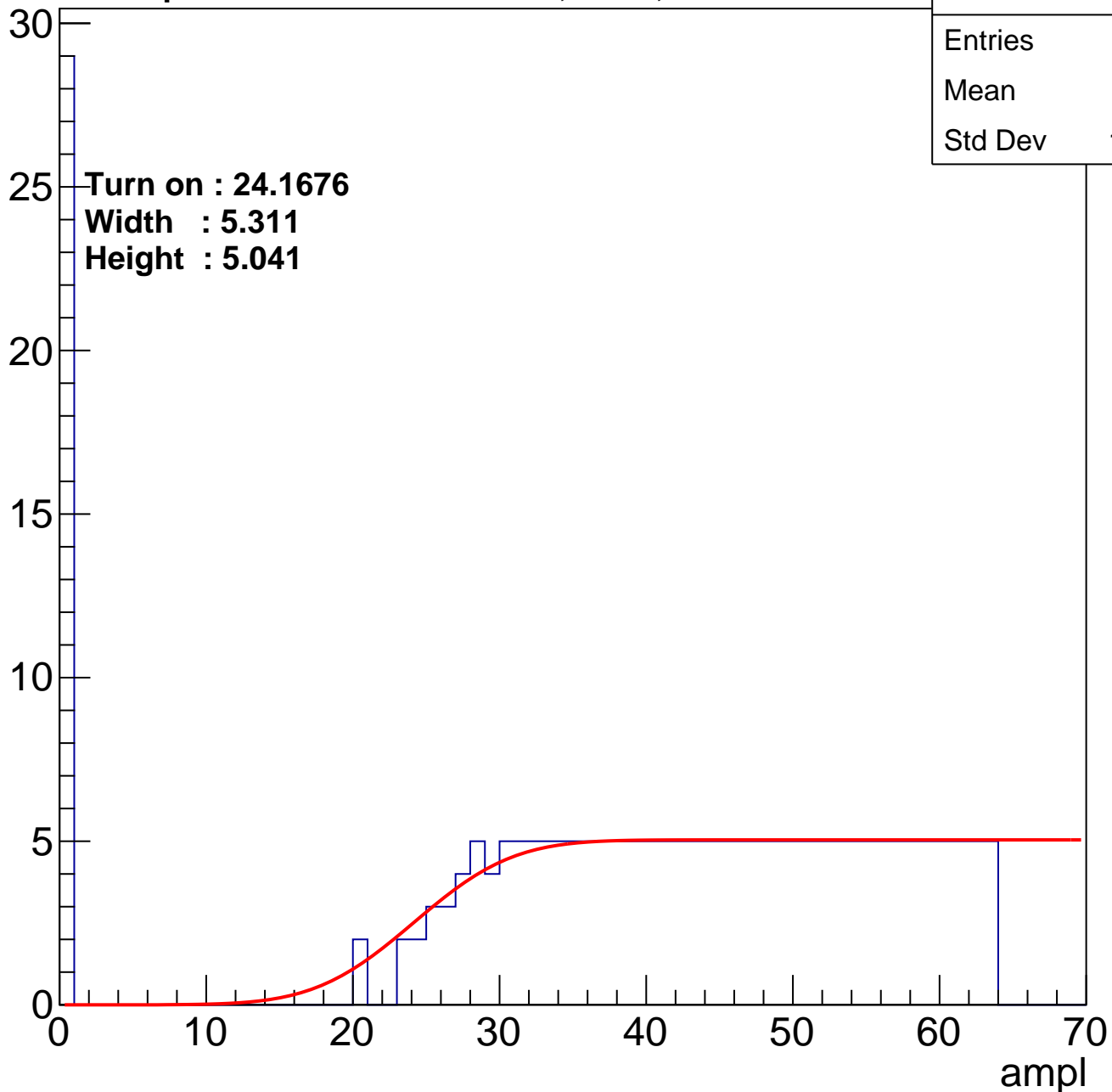
|         |       |
|---------|-------|
| Entries | 224   |
| Mean    | 38.2  |
| Std Dev | 18.21 |

Turn on : 24.1676

Width : 5.311

Height : 5.041

Entry





# B1L103S, U15-ch56

calib\_packv5\_041523\_1651.root, FC#0, Port C2

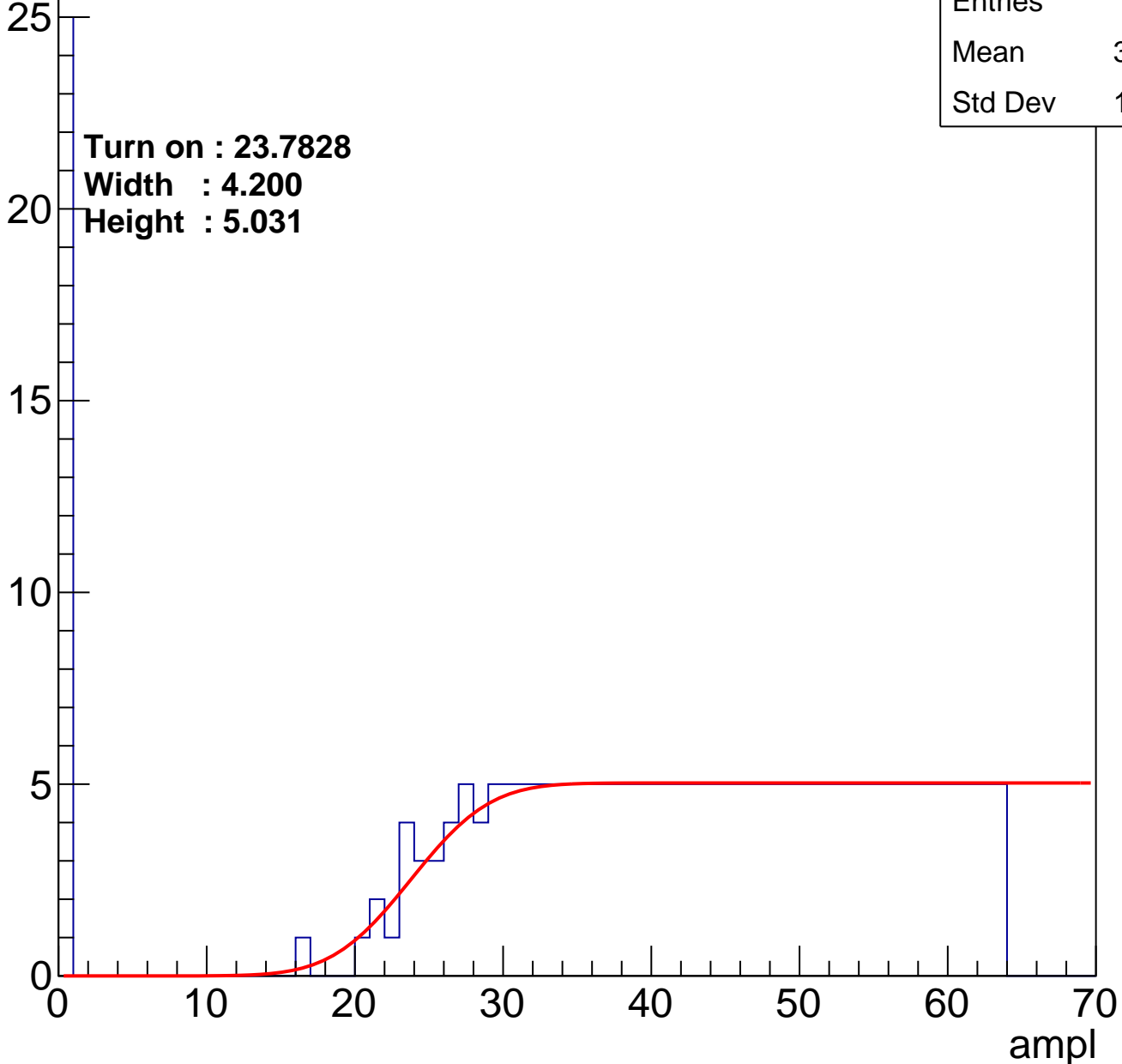
|         |       |
|---------|-------|
| Entries | 228   |
| Mean    | 38.33 |
| Std Dev | 17.56 |

**Turn on : 23.7828**

**Width : 4.200**

**Height : 5.031**

Entry



# B1L103S, U15-ch57

calib\_packv5\_041523\_1651.root, FC#0, Port C2

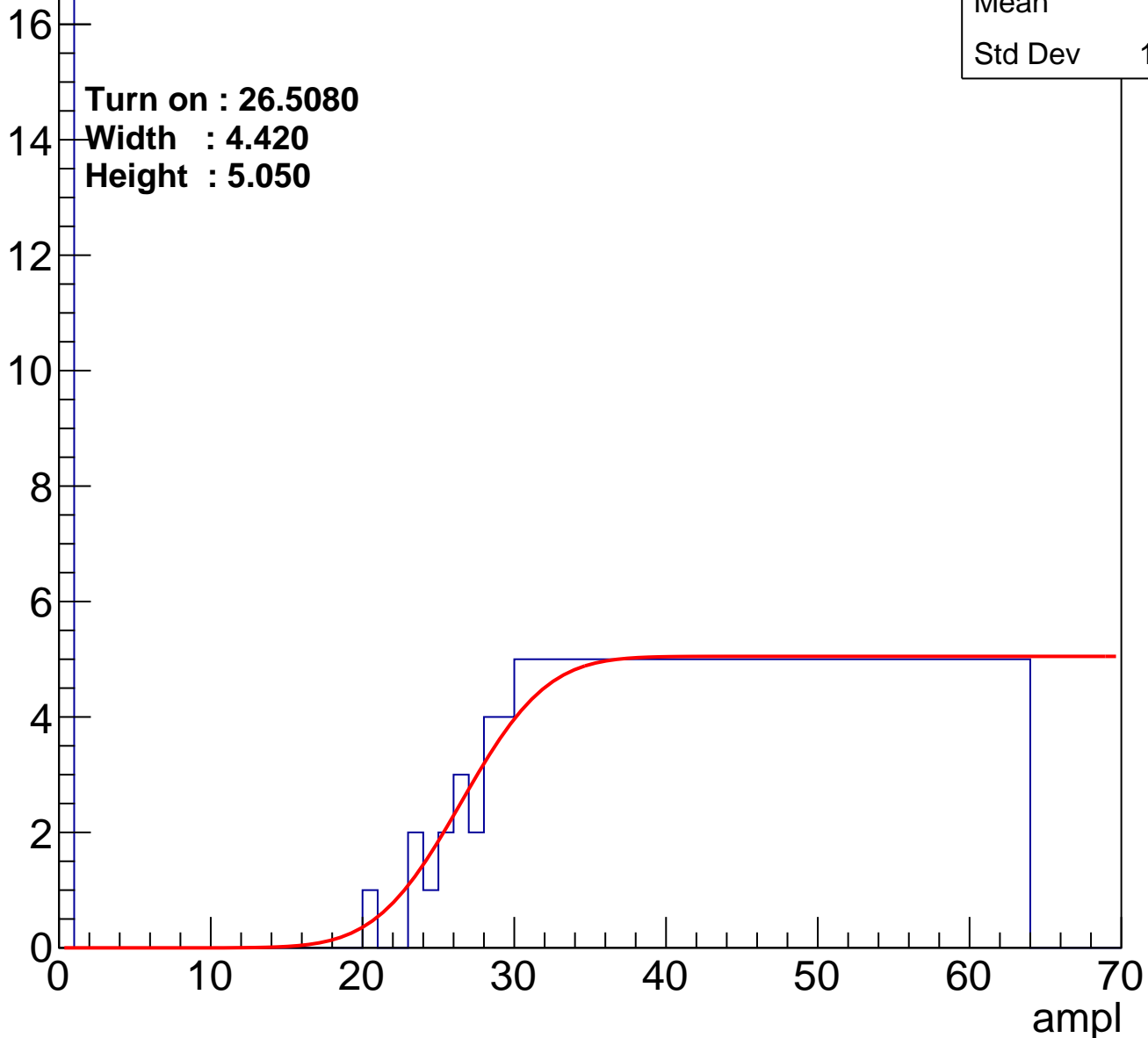
|         |       |
|---------|-------|
| Entries | 206   |
| Mean    | 40.8  |
| Std Dev | 16.23 |

Turn on : 26.5080

Width : 4.420

Height : 5.050

Entry

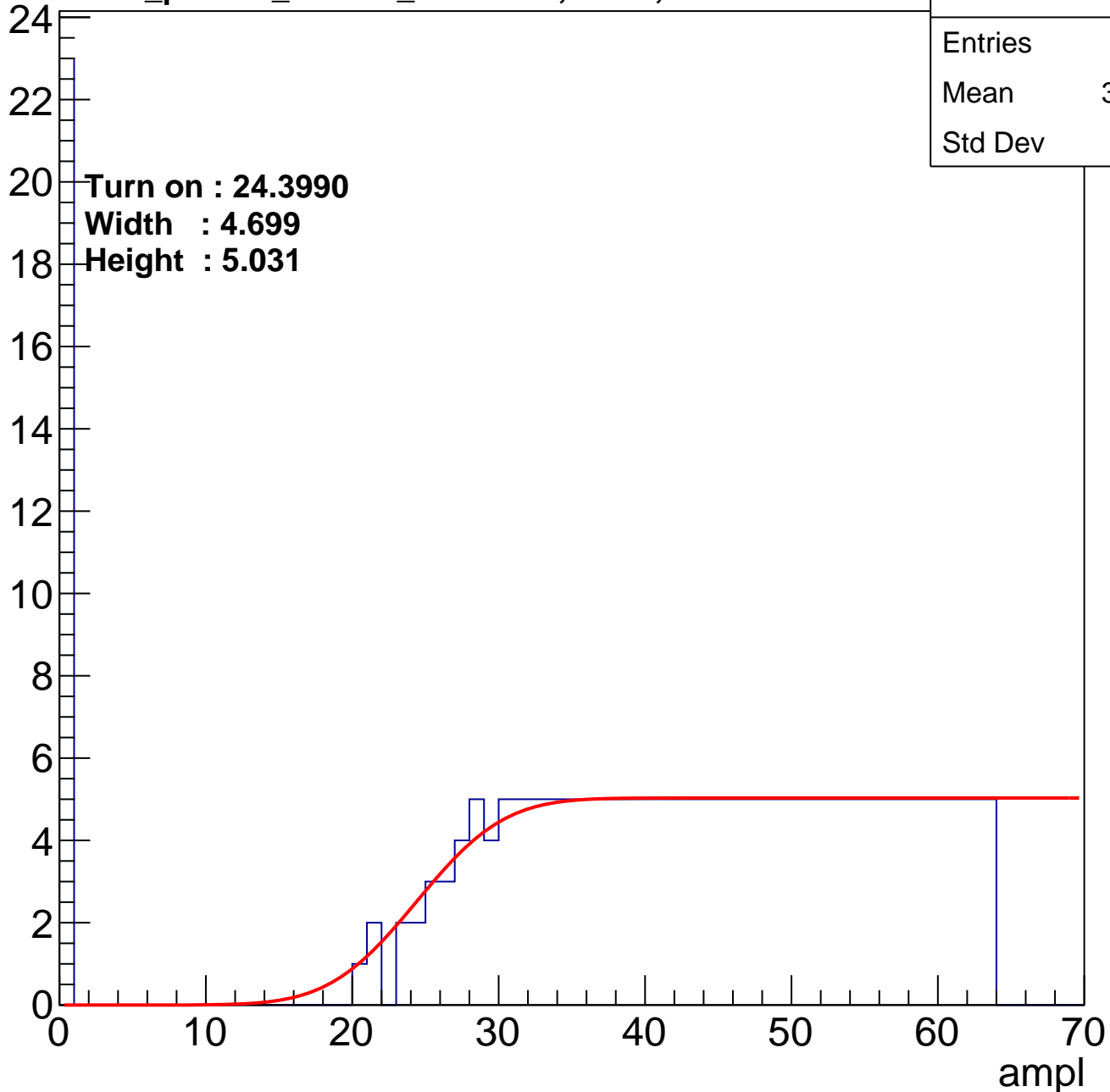


# B1L103S, U15-ch58

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 219   |
| Mean    | 39.17 |
| Std Dev | 17.3  |

Entry



# B1L103S, U15-ch59

calib\_packv5\_041523\_1651.root, FC#0, Port C2

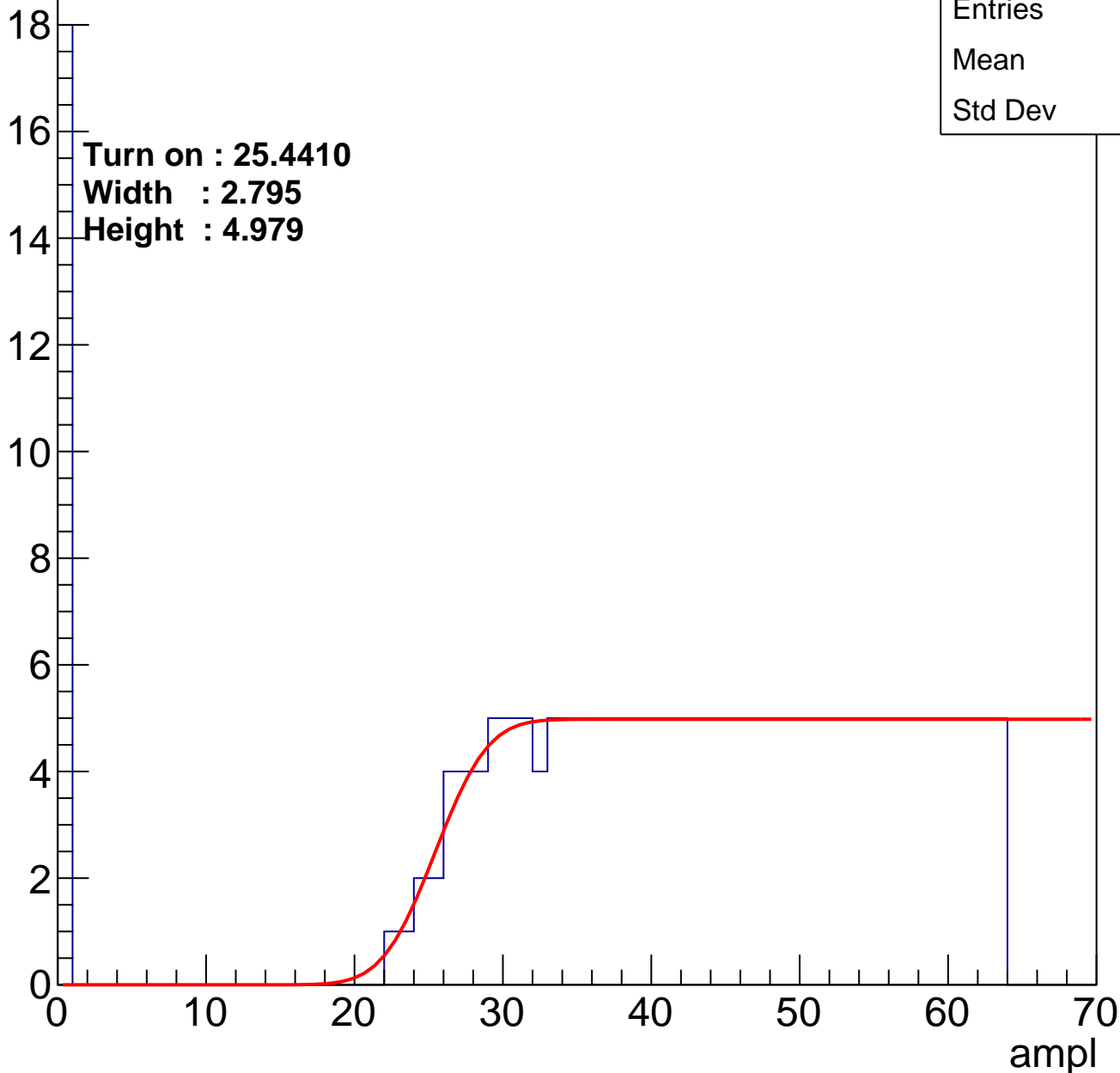
|         |      |
|---------|------|
| Entries | 210  |
| Mean    | 40.4 |
| Std Dev | 16.4 |

Turn on : 25.4410

Width : 2.795

Height : 4.979

Entry



# B1L103S, U15-ch60

calib\_packv5\_041523\_1651.root, FC#0, Port C2

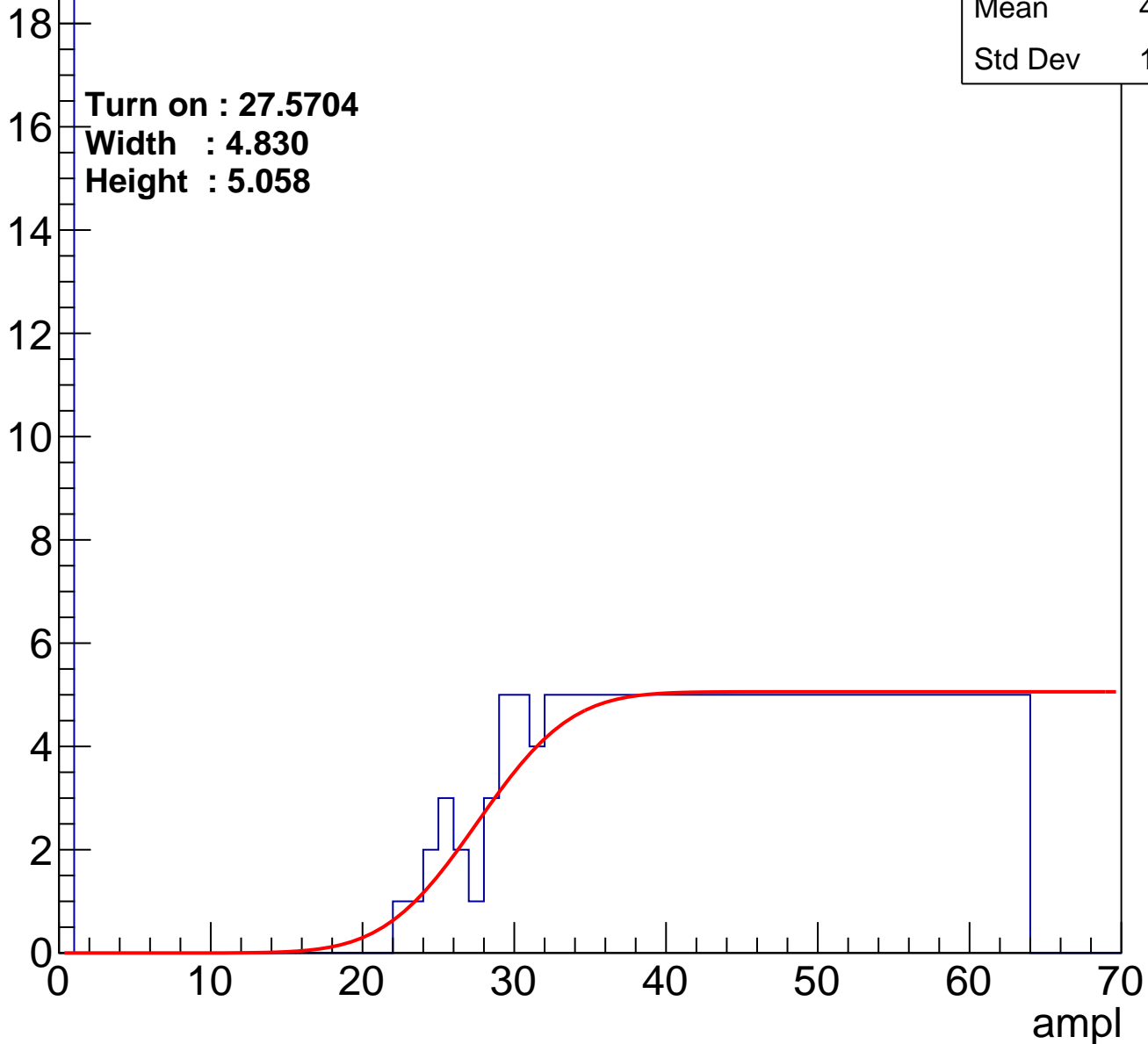
|         |       |
|---------|-------|
| Entries | 206   |
| Mean    | 40.53 |
| Std Dev | 16.66 |

**Turn on : 27.5704**

**Width : 4.830**

**Height : 5.058**

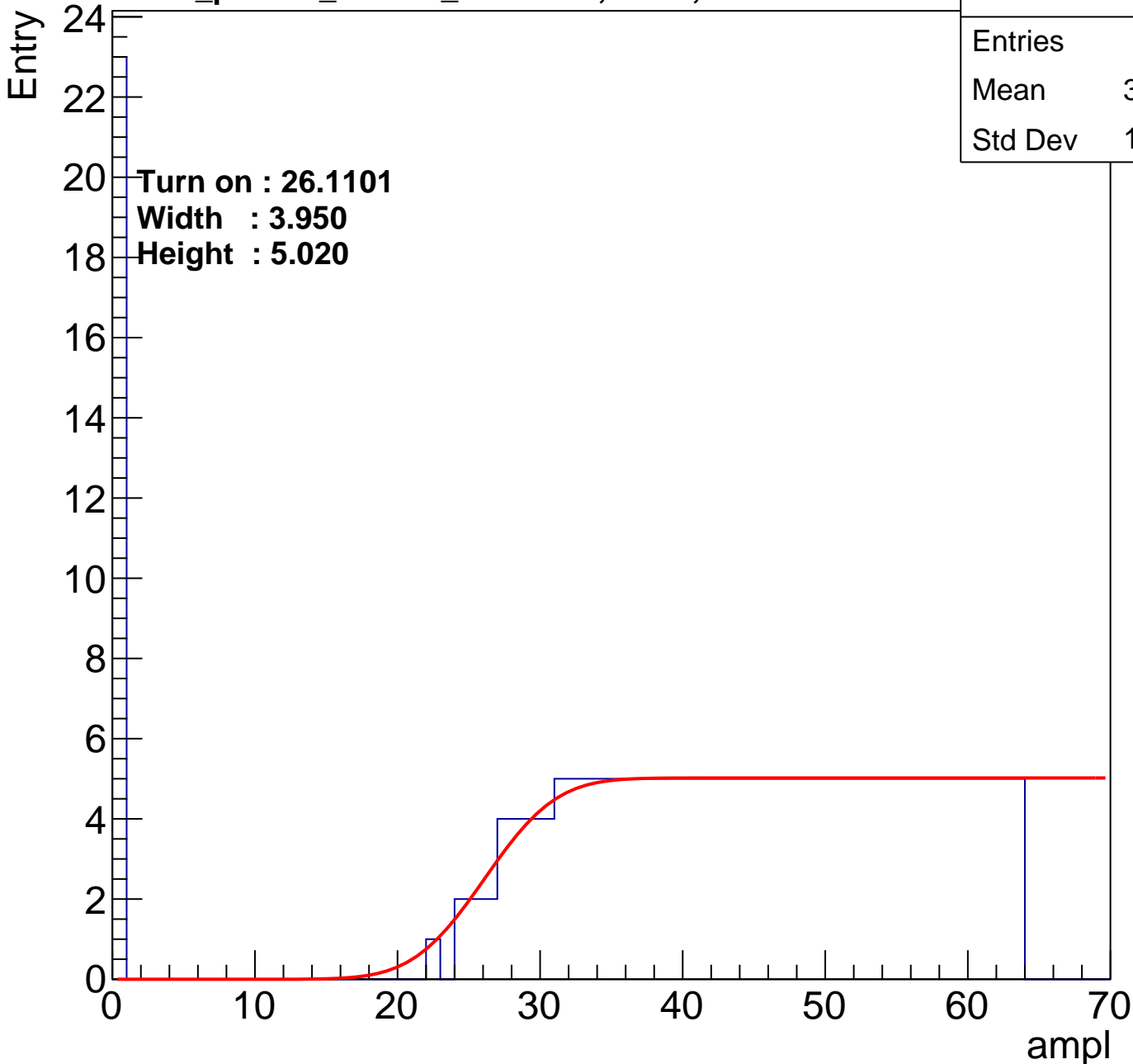
Entry



# B1L103S, U15-ch61

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 211   |
| Mean    | 39.73 |
| Std Dev | 17.37 |



# B1L103S, U15-ch62

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 231   |
| Mean    | 37.93 |
| Std Dev | 17.84 |

**Turn on : 22.7552**

**Width : 5.645**

**Height : 5.045**

Entry

25

20

15

10

5

0

0

10

20

30

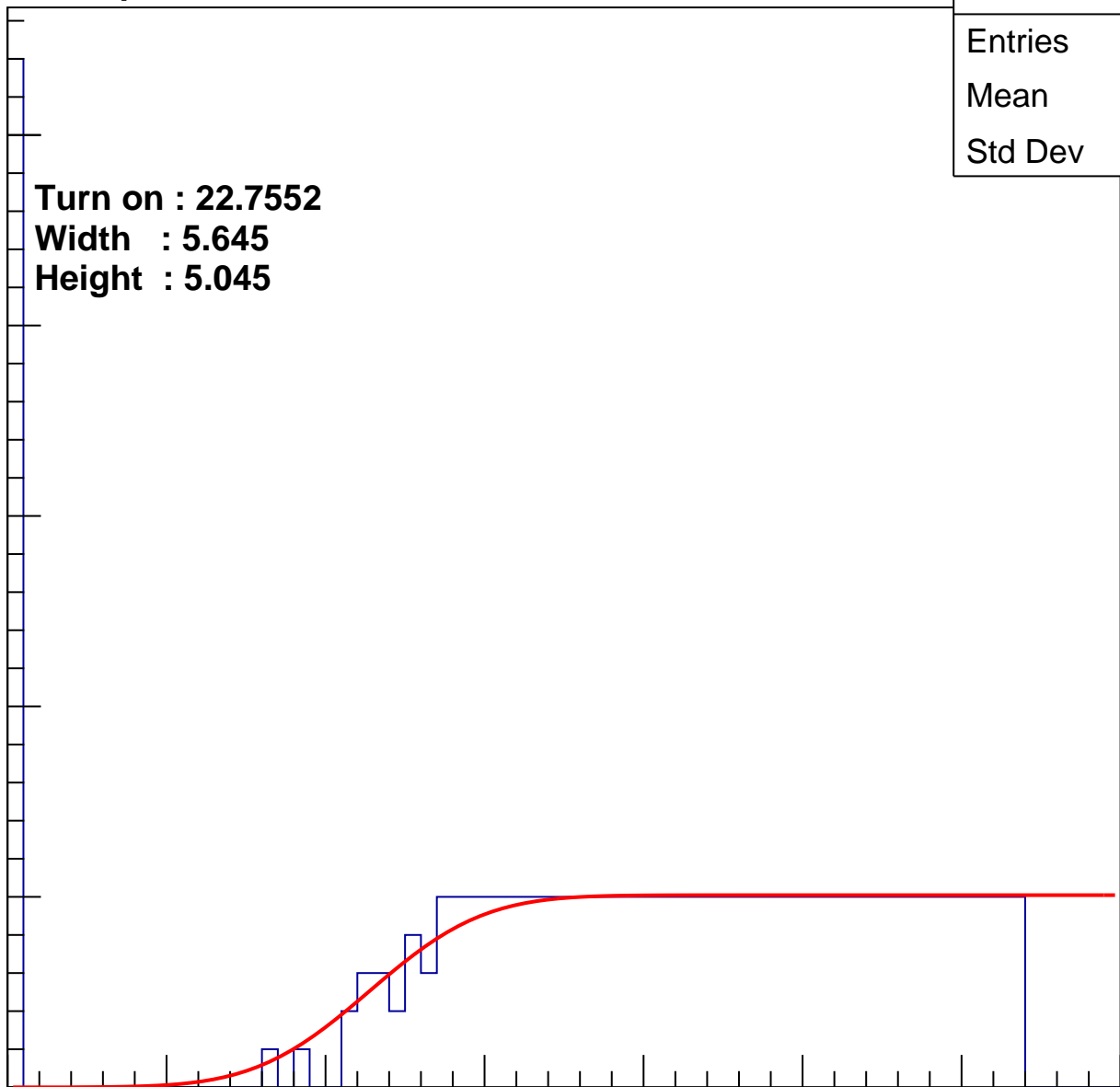
40

50

60

70

ampl



# B1L103S, U15-ch63

calib\_packv5\_041523\_1651.root, FC#0, Port C2

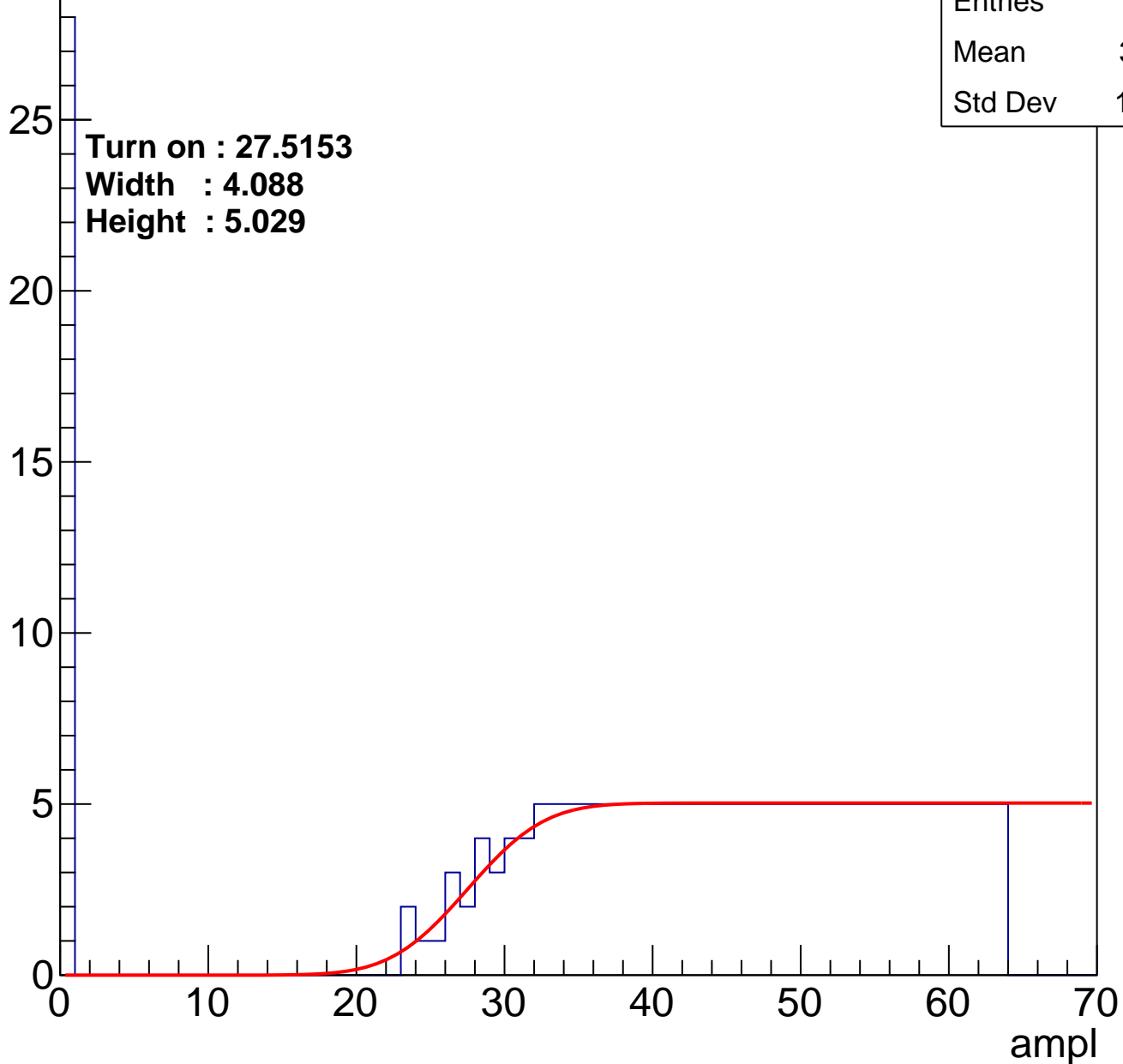
|         |       |
|---------|-------|
| Entries | 212   |
| Mean    | 39.01 |
| Std Dev | 18.28 |

**Turn on : 27.5153**

**Width : 4.088**

**Height : 5.029**

Entry



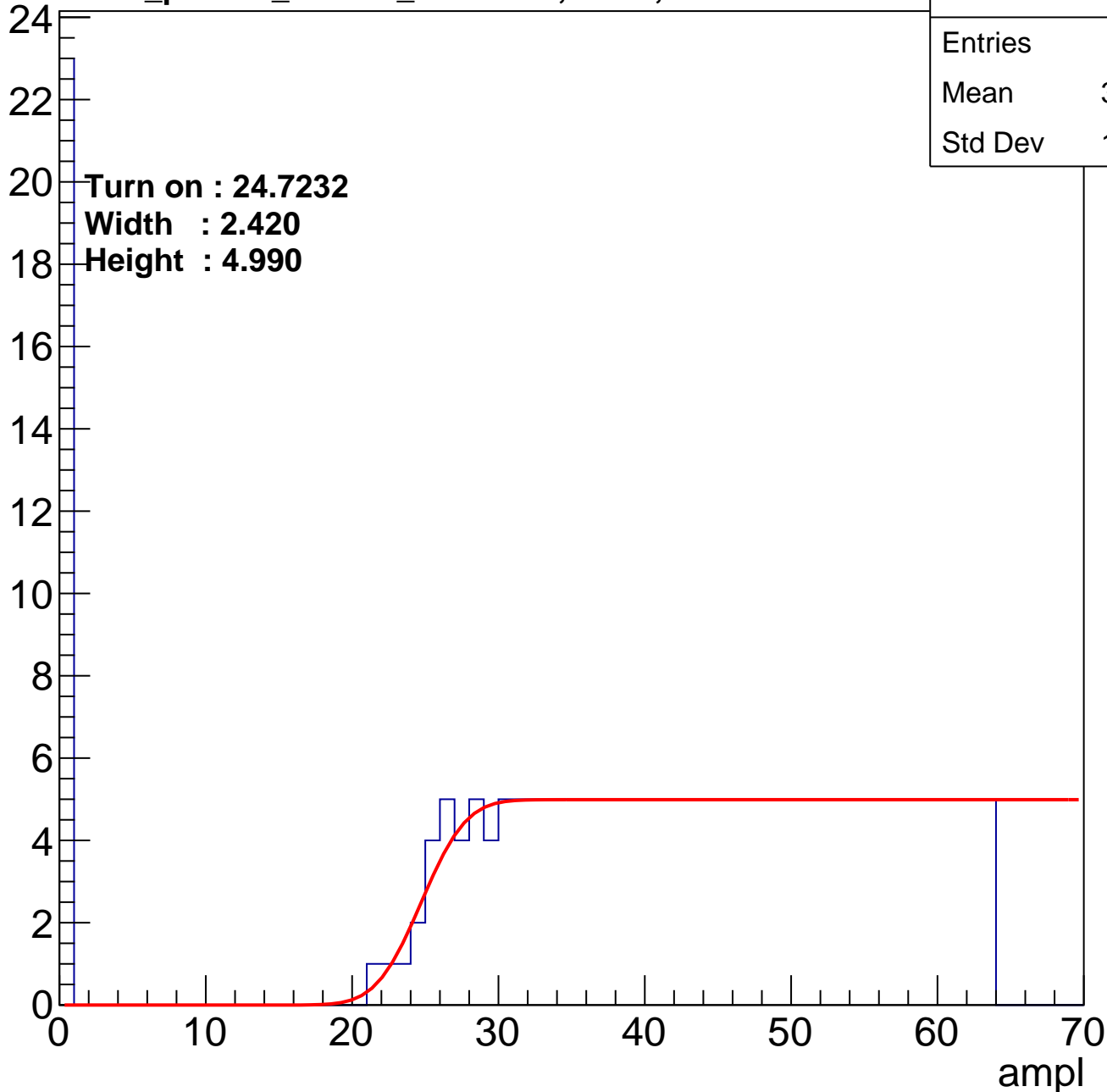


# B1L103S, U15-ch64

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 220   |
| Mean    | 39.15 |
| Std Dev | 17.25 |

Entry



# B1L103S, U15-ch65

calib\_packv5\_041523\_1651.root, FC#0, Port C2

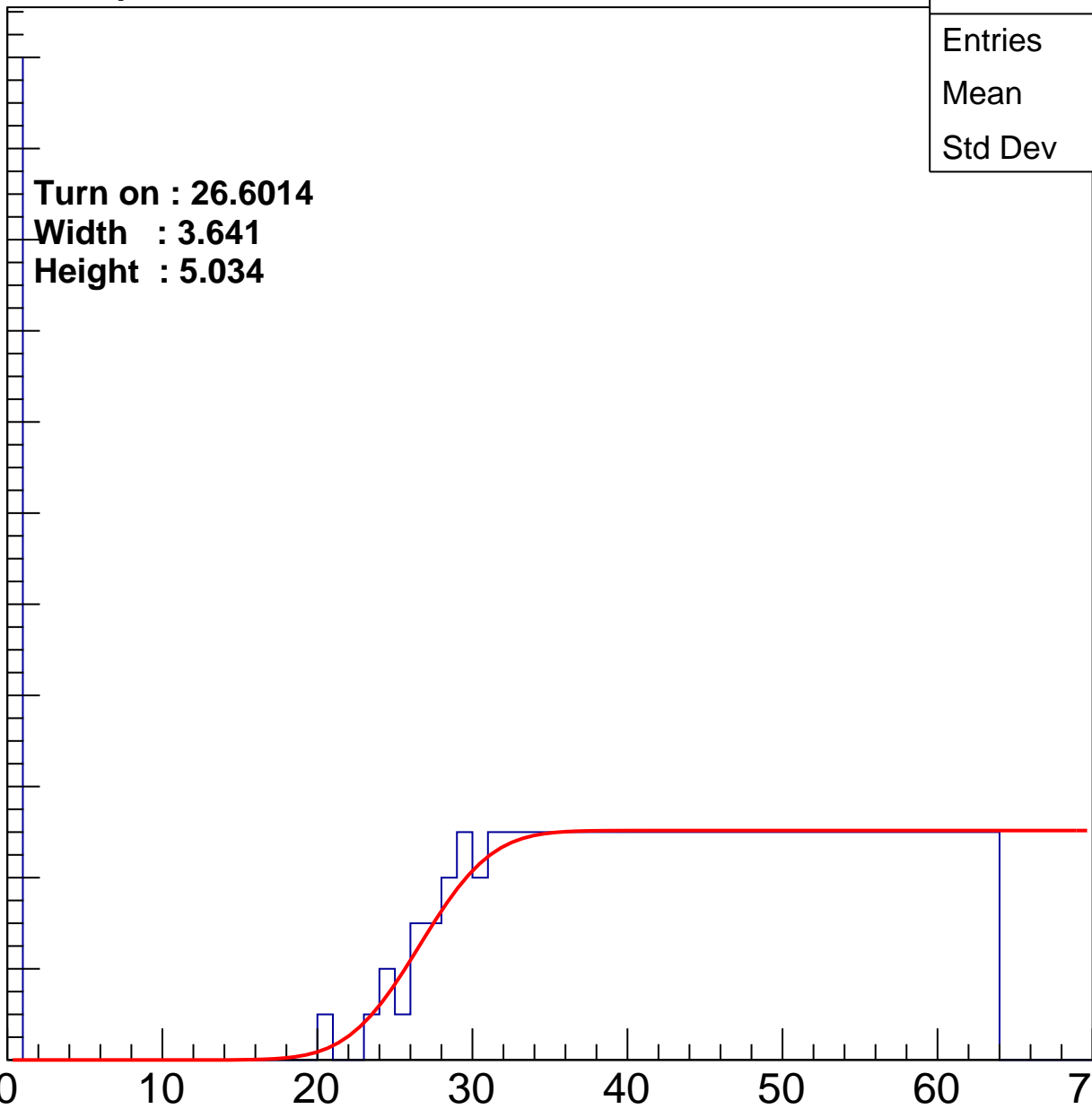
Entry

22  
20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 26.6014**  
**Width : 3.641**  
**Height : 5.034**

|         |       |
|---------|-------|
| Entries | 211   |
| Mean    | 39.84 |
| Std Dev | 17.19 |

ampl



# B1L103S, U15-ch66

calib\_packv5\_041523\_1651.root, FC#0, Port C2

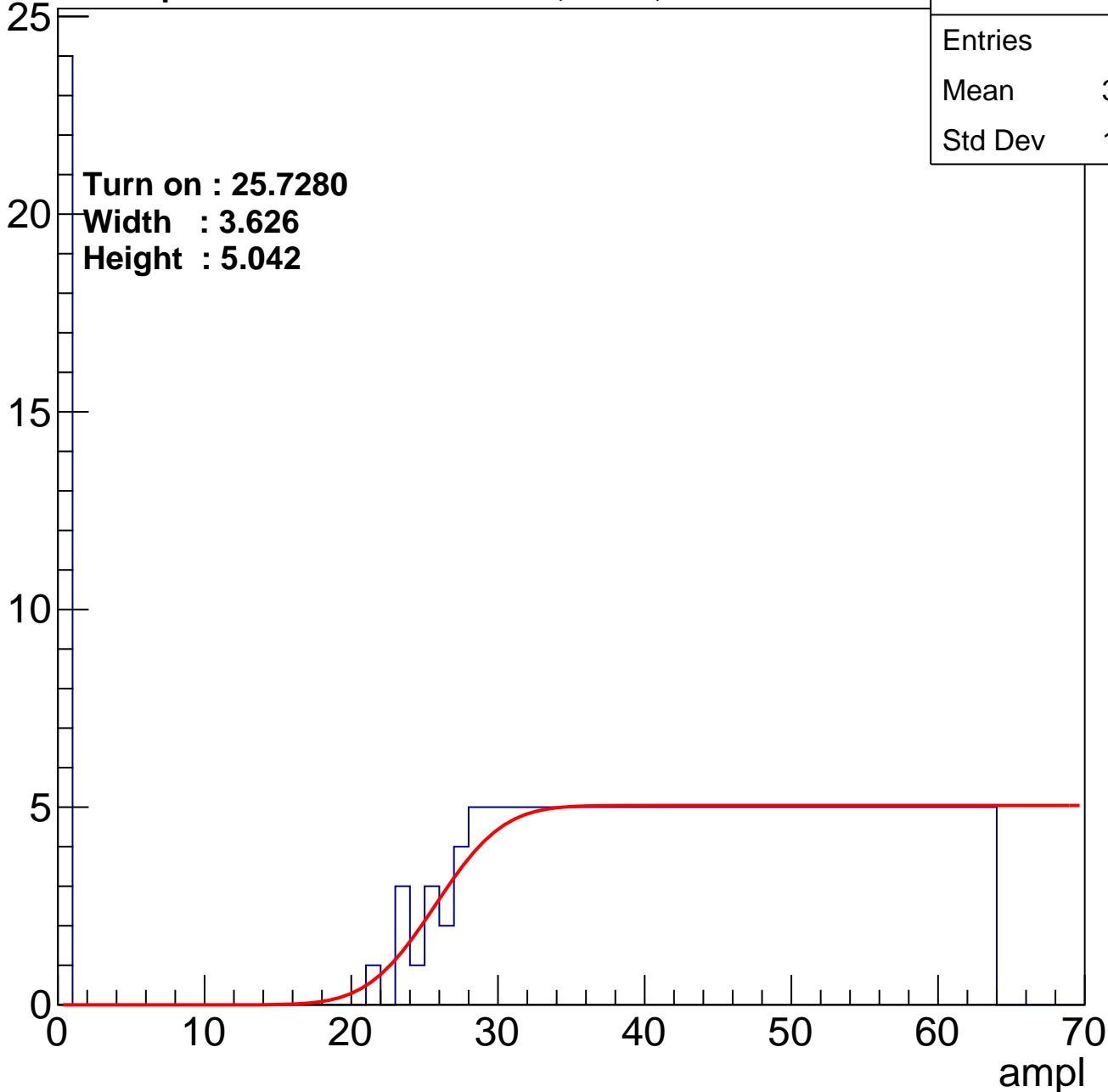
|         |       |
|---------|-------|
| Entries | 218   |
| Mean    | 39.17 |
| Std Dev | 17.45 |

Turn on : 25.7280

Width : 3.626

Height : 5.042

Entry



# B1L103S, U15-ch67

calib\_packv5\_041523\_1651.root, FC#0, Port C2

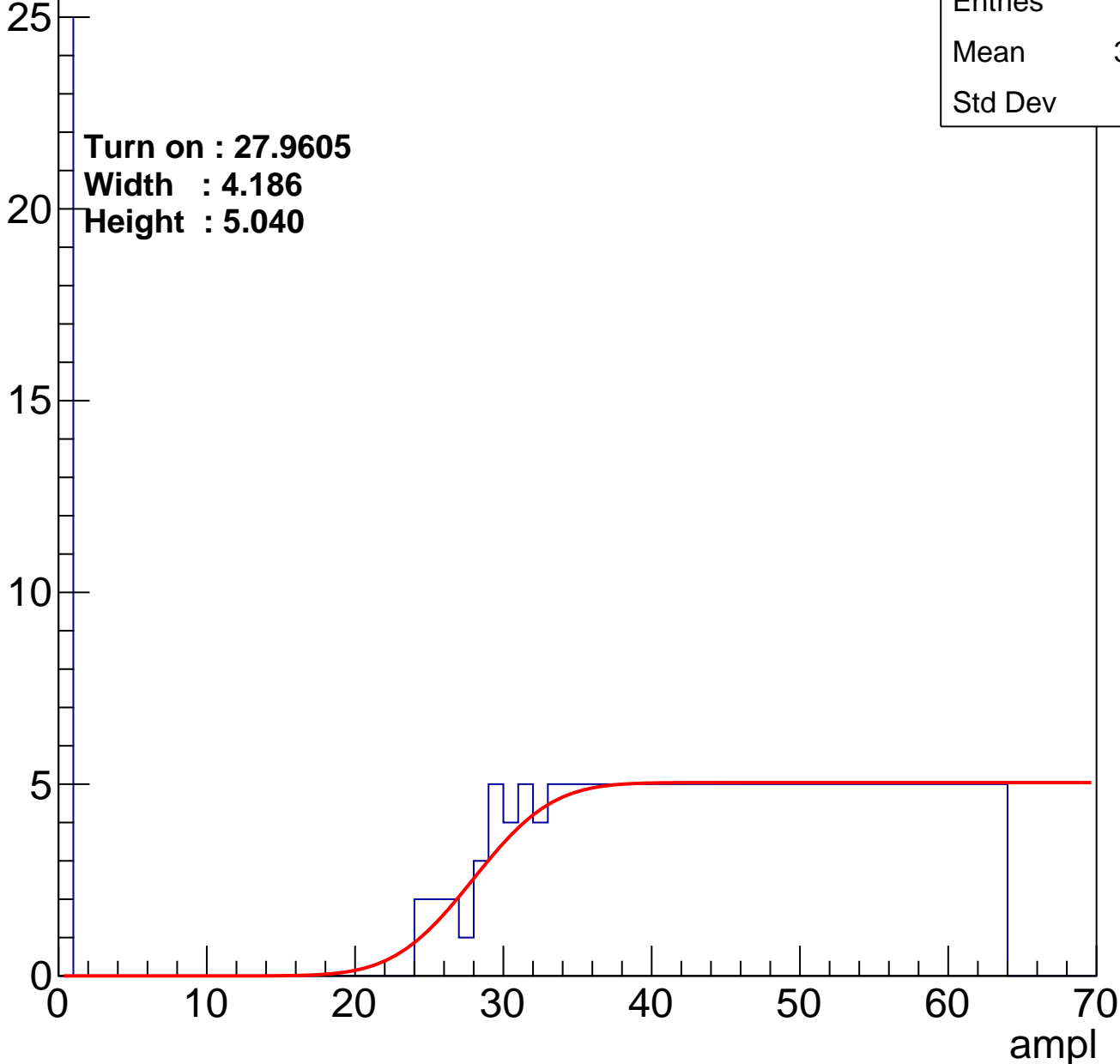
|         |       |
|---------|-------|
| Entries | 208   |
| Mean    | 39.66 |
| Std Dev | 17.8  |

**Turn on : 27.9605**

**Width : 4.186**

**Height : 5.040**

Entry



# B1L103S, U15-ch68

calib\_packv5\_041523\_1651.root, FC#0, Port C2

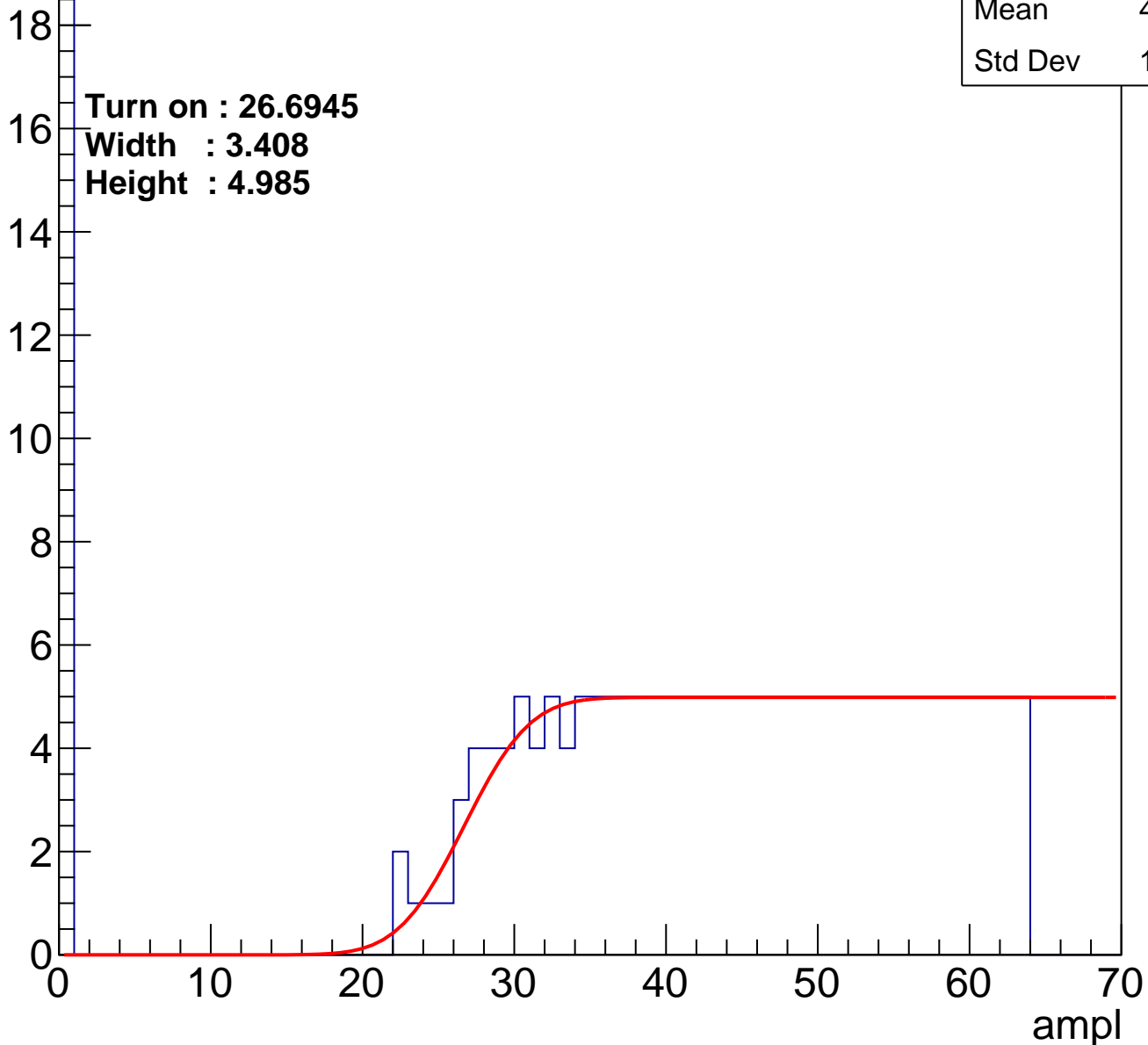
|         |       |
|---------|-------|
| Entries | 207   |
| Mean    | 40.44 |
| Std Dev | 16.67 |

**Turn on : 26.6945**

**Width : 3.408**

**Height : 4.985**

Entry



# B1L103S, U15-ch69

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 209   |
| Mean    | 38.8  |
| Std Dev | 18.88 |

**Turn on : 28.7089**

**Width : 3.220**

**Height : 4.997**

Entry

30

25

20

15

10

5

0

0

10

20

30

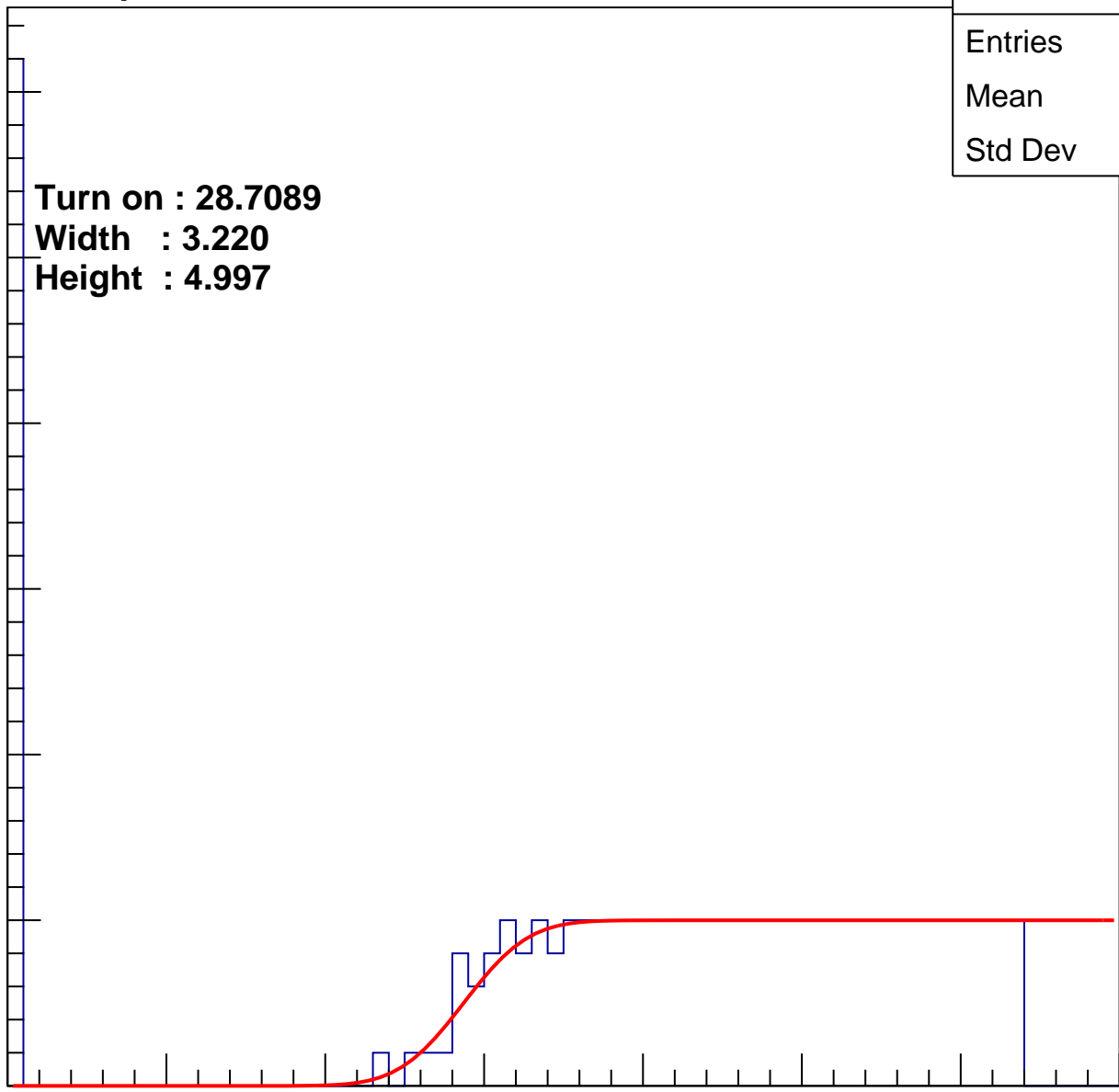
40

50

60

70

ampl



# B1L103S, U15-ch70

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 233   |
| Mean    | 37.73 |
| Std Dev | 17.94 |

**Turn on : 23.3500**  
**Width : 3.593**  
**Height : 5.017**

Entry

25

20

15

10

5

0

0

10

20

30

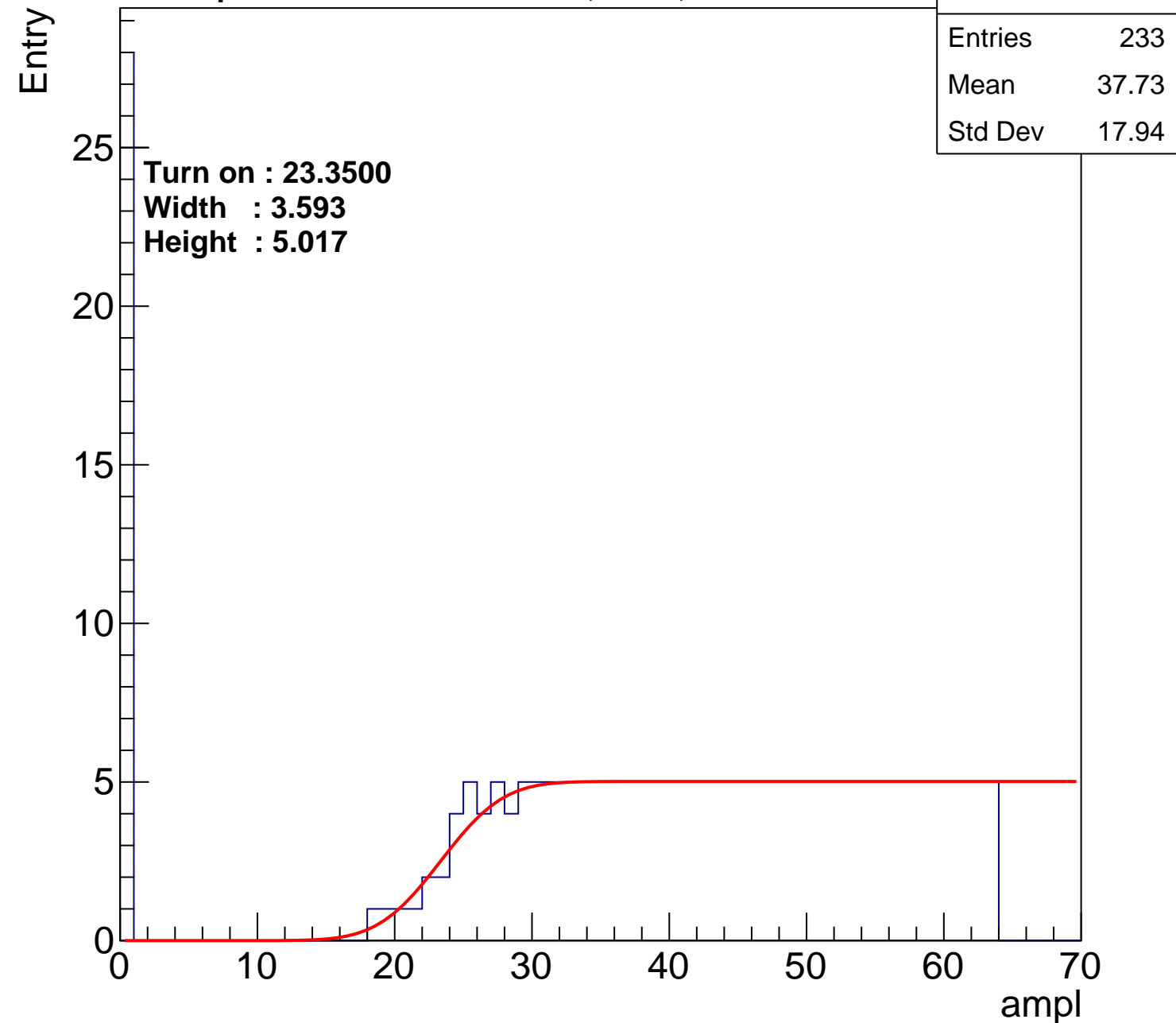
40

50

60

70

ampl



# B1L103S, U15-ch71

calib\_packv5\_041523\_1651.root, FC#0, Port C2

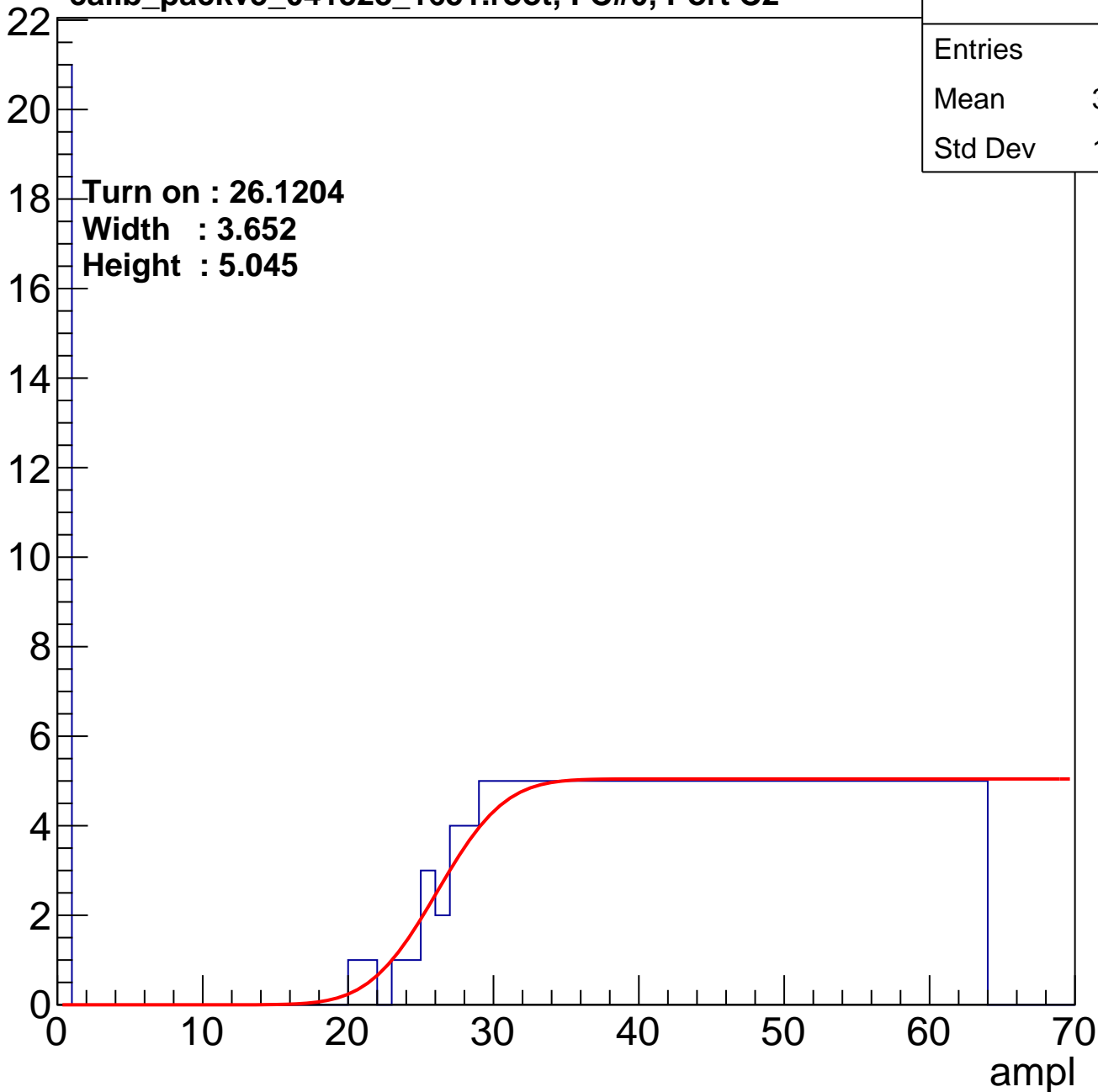
|         |       |
|---------|-------|
| Entries | 213   |
| Mean    | 39.84 |
| Std Dev | 16.97 |

Turn on : 26.1204

Width : 3.652

Height : 5.045

Entry





# B1L103S, U15-ch72

calib\_packv5\_041523\_1651.root, FC#0, Port C2

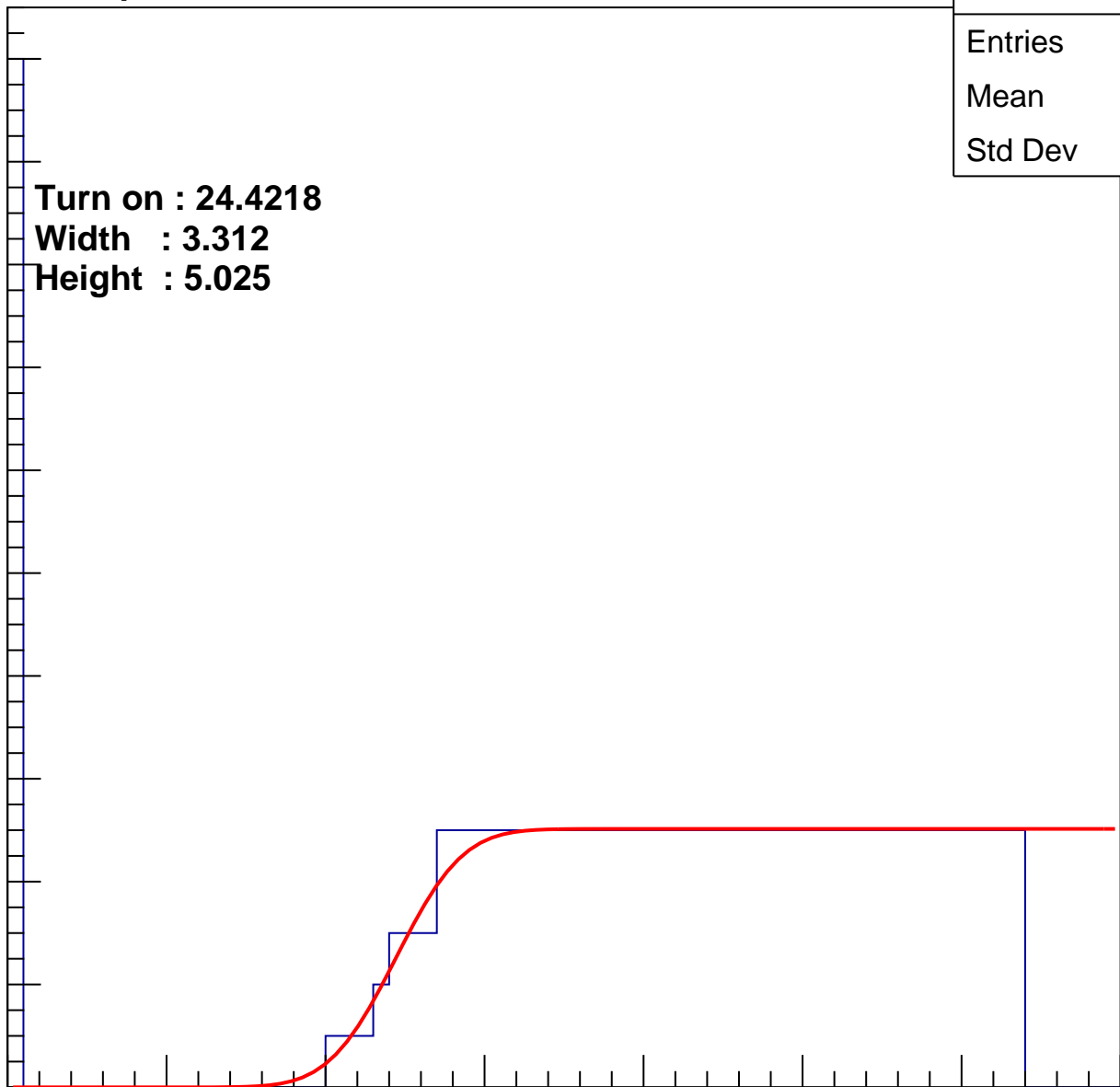
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Turn on : 24.4218  
Width : 3.312  
Height : 5.025

|         |       |
|---------|-------|
| Entries | 219   |
| Mean    | 39.54 |
| Std Dev | 16.74 |

ampl



# B1L103S, U15-ch73

calib\_packv5\_041523\_1651.root, FC#0, Port C2

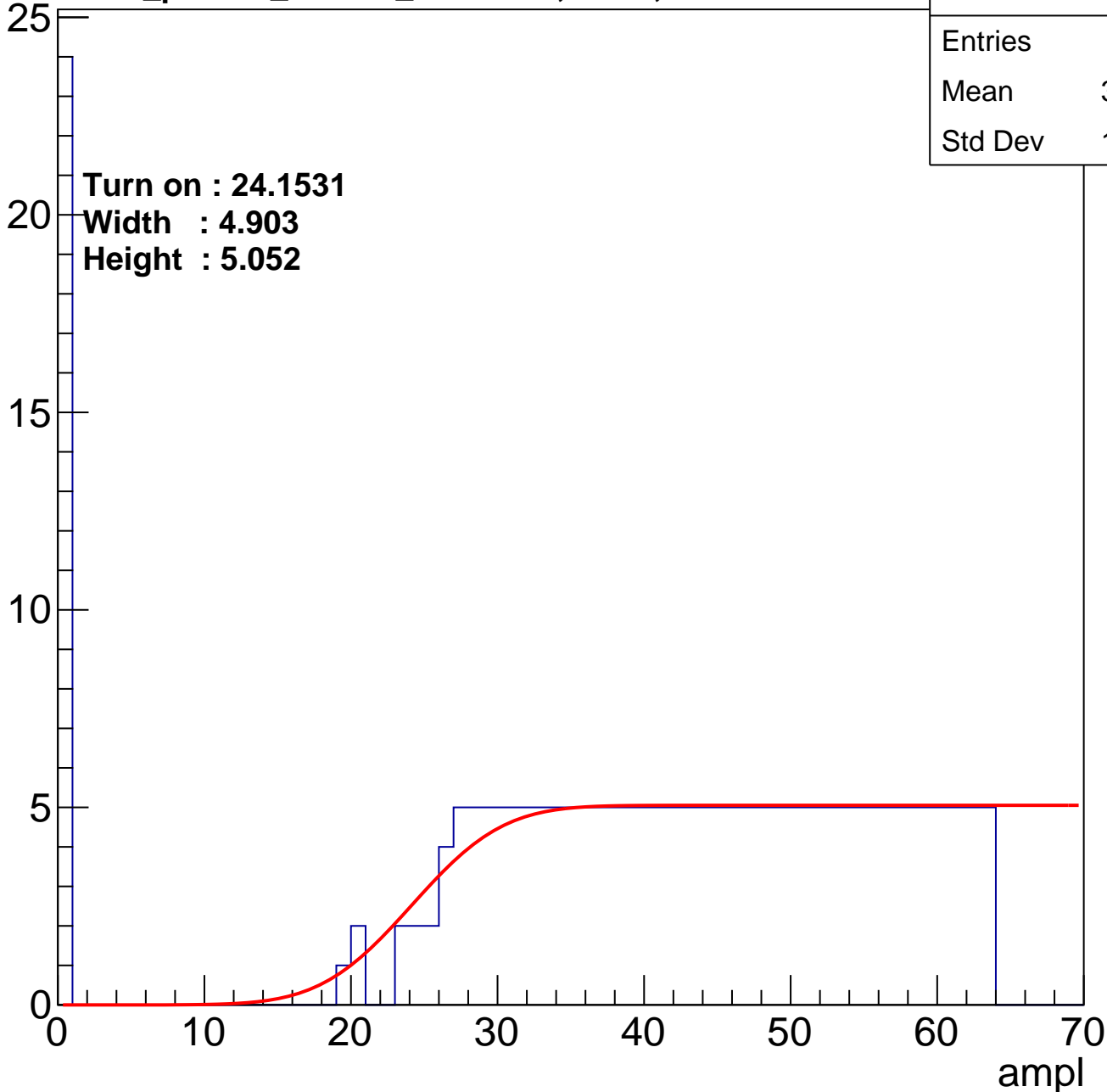
|         |       |
|---------|-------|
| Entries | 222   |
| Mean    | 38.88 |
| Std Dev | 17.42 |

Turn on : 24.1531

Width : 4.903

Height : 5.052

Entry



# B1L103S, U15-ch74

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 223   |
| Mean    | 38.42 |
| Std Dev | 17.95 |

**Turn on : 24.2572**

**Width : 4.556**

**Height : 5.006**

Entry

25

20

15

10

5

0

0

10

20

30

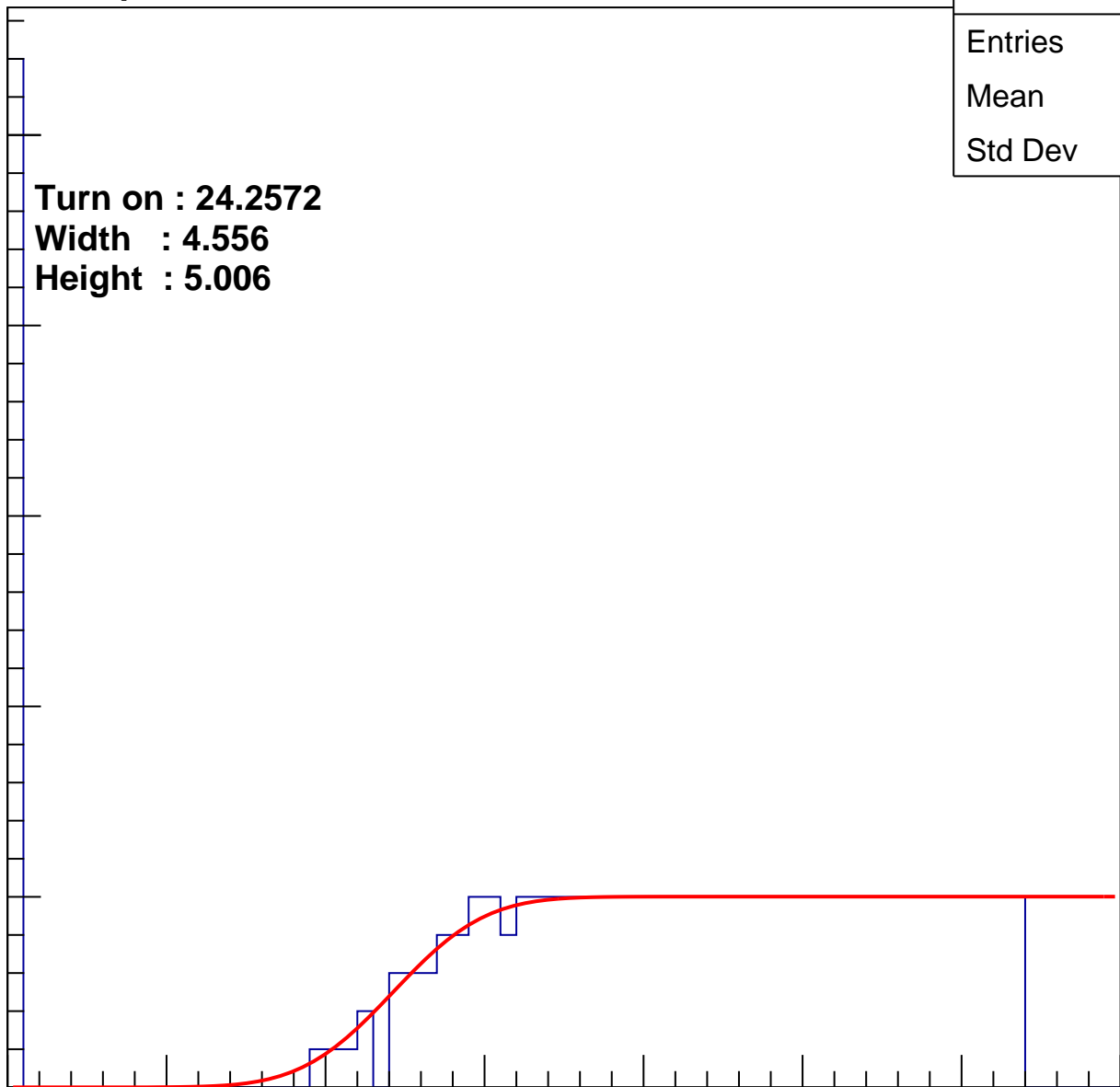
40

50

60

70

ampl



# B1L103S, U15-ch75

calib\_packv5\_041523\_1651.root, FC#0, Port C2

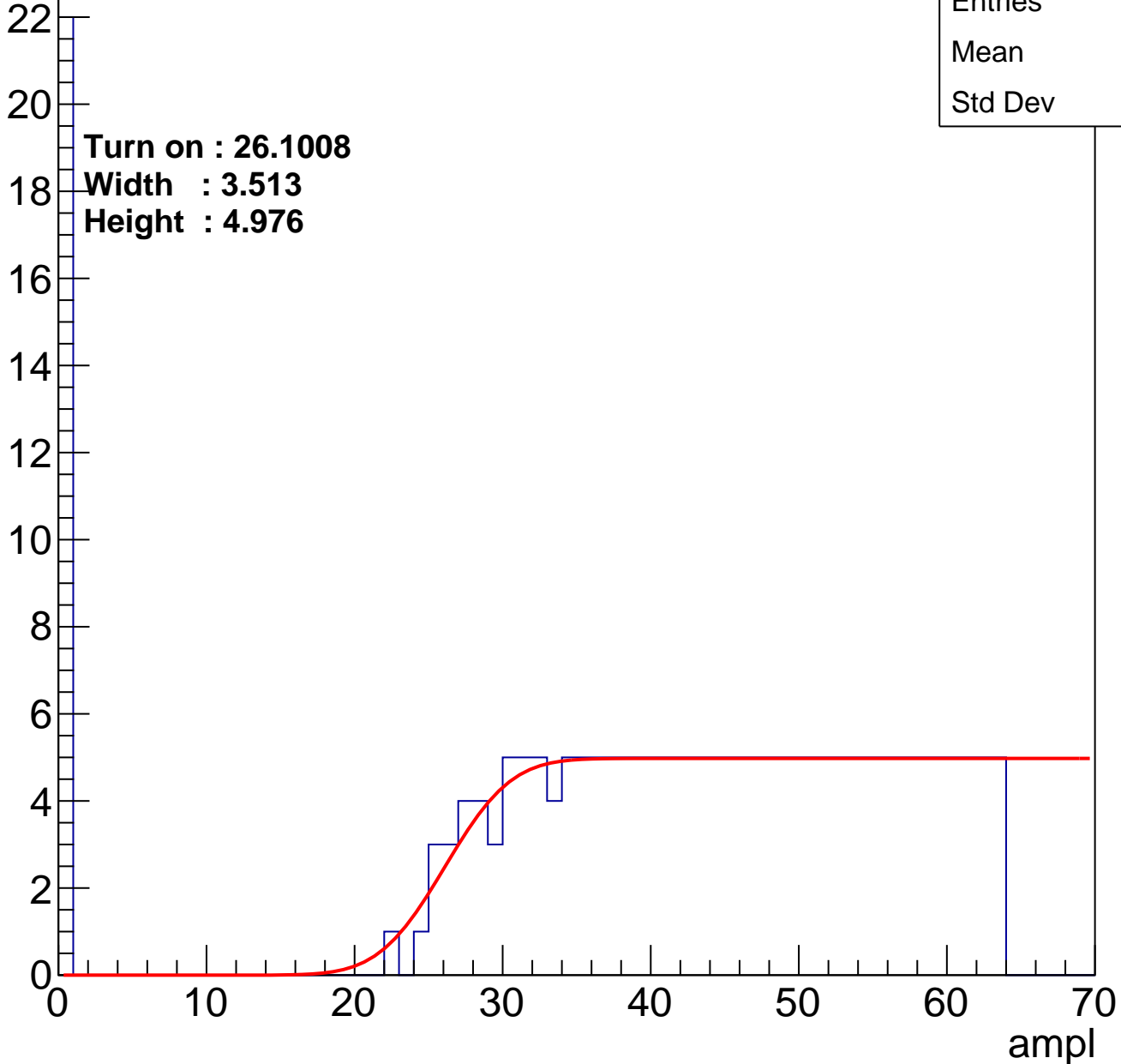
|         |      |
|---------|------|
| Entries | 210  |
| Mean    | 39.9 |
| Std Dev | 17.2 |

**Turn on : 26.1008**

**Width : 3.513**

**Height : 4.976**

Entry



# B1L103S, U15-ch76

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 209   |
| Mean    | 38.94 |
| Std Dev | 18.7  |

**Turn on : 28.7629**

**Width : 4.172**

**Height : 5.050**

Entry

30

25

20

15

10

5

0

0

10

20

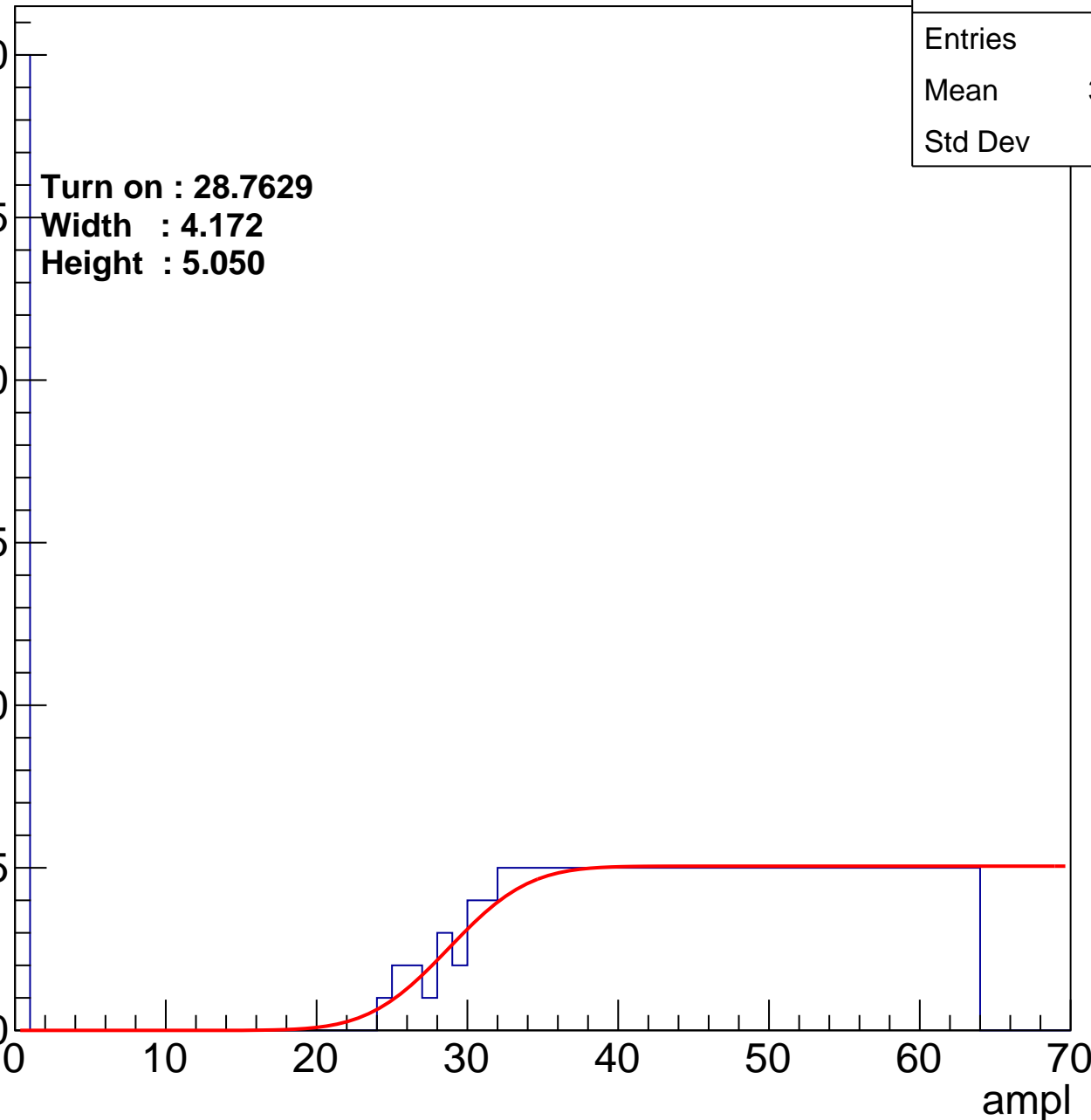
30

40

50

60

ampl



# B1L103S, U15-ch77

calib\_packv5\_041523\_1651.root, FC#0, Port C2

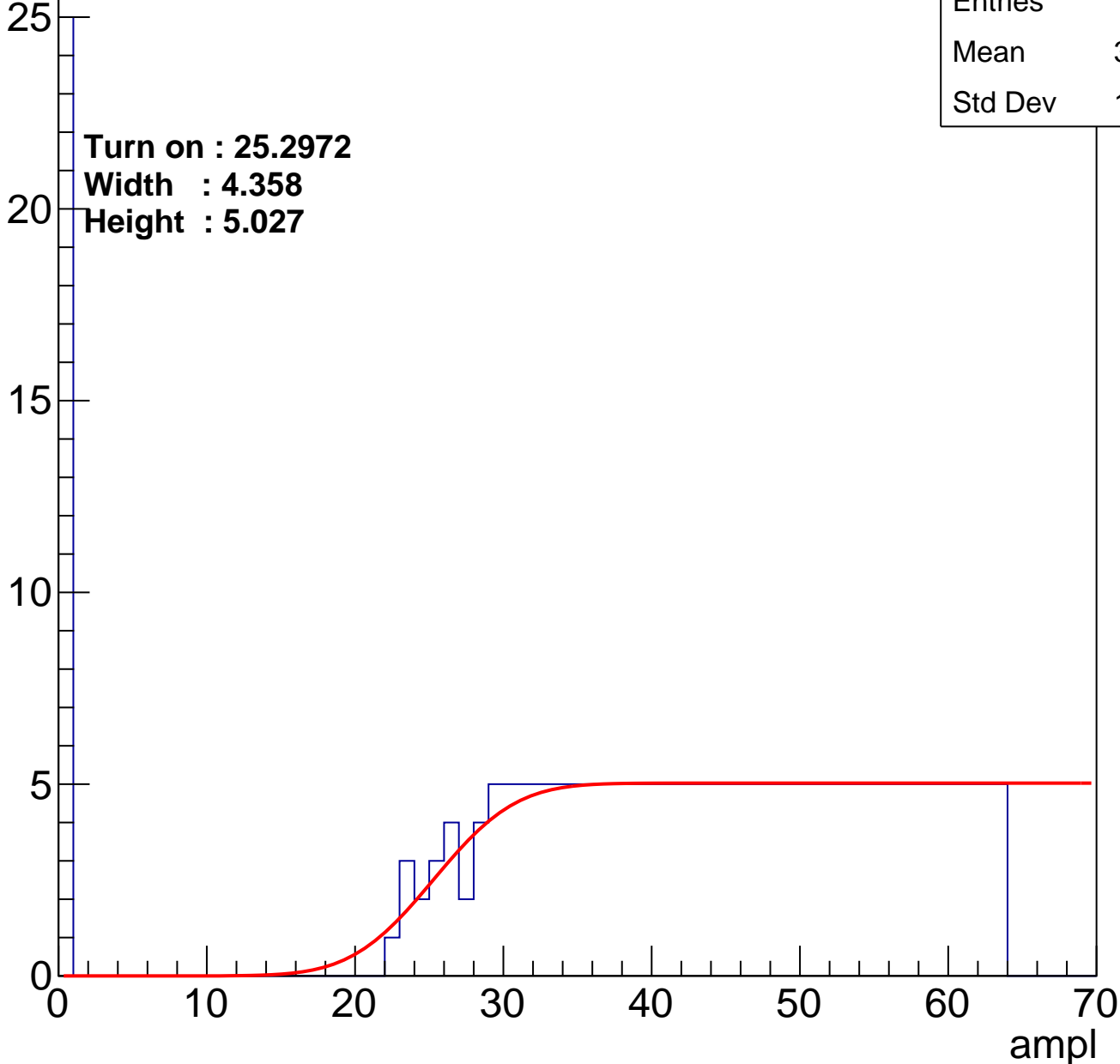
|         |       |
|---------|-------|
| Entries | 219   |
| Mean    | 38.97 |
| Std Dev | 17.62 |

Turn on : 25.2972

Width : 4.358

Height : 5.027

Entry



# B1L103S, U15-ch78

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 219   |
| Mean    | 38.73 |
| Std Dev | 17.97 |

**Turn on : 26.2549**

**Width : 4.178**

**Height : 5.047**

Entry

25

20

15

10

5

0

0

10

20

30

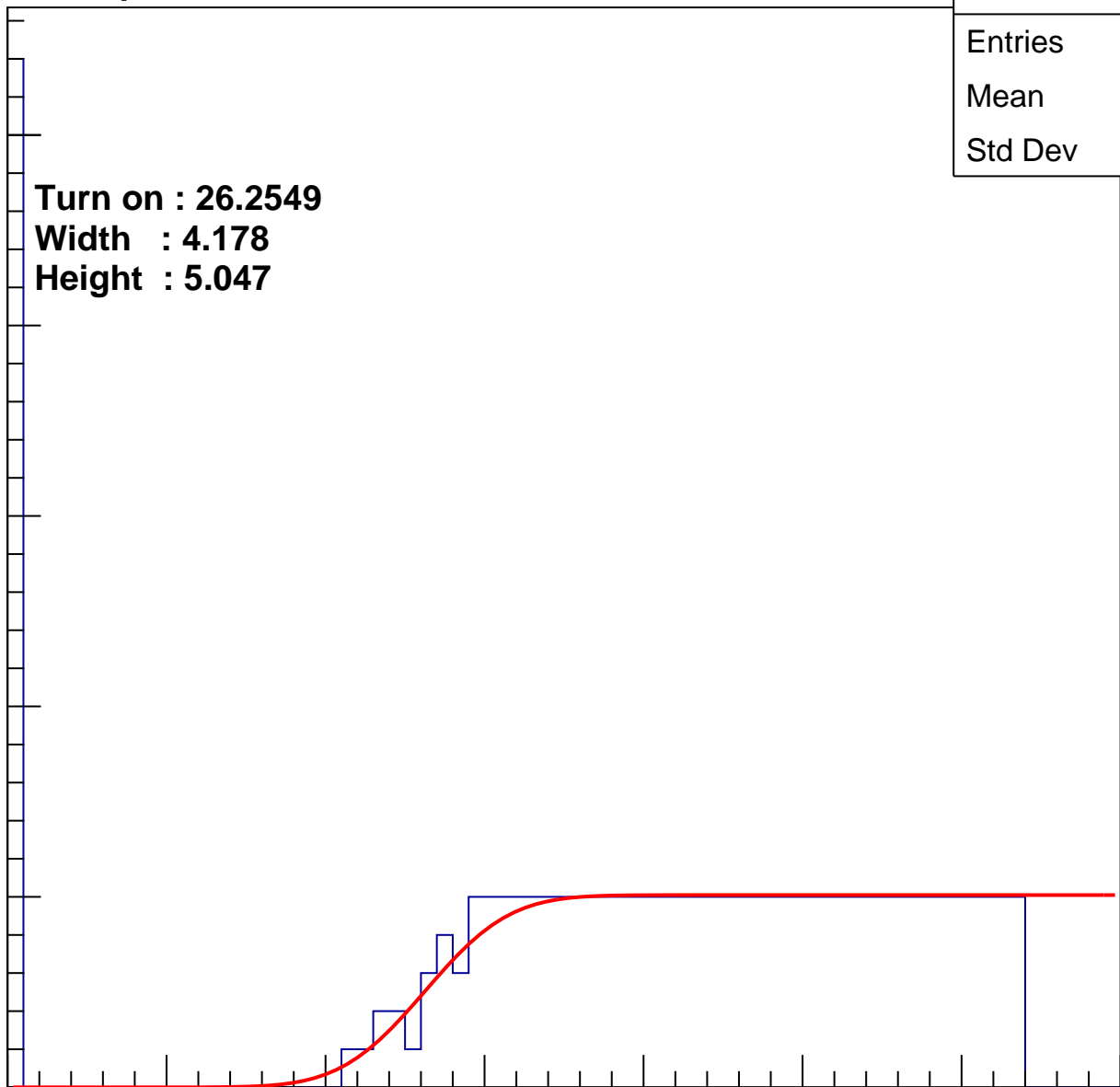
40

50

60

70

ampl



# B1L103S, U15-ch79

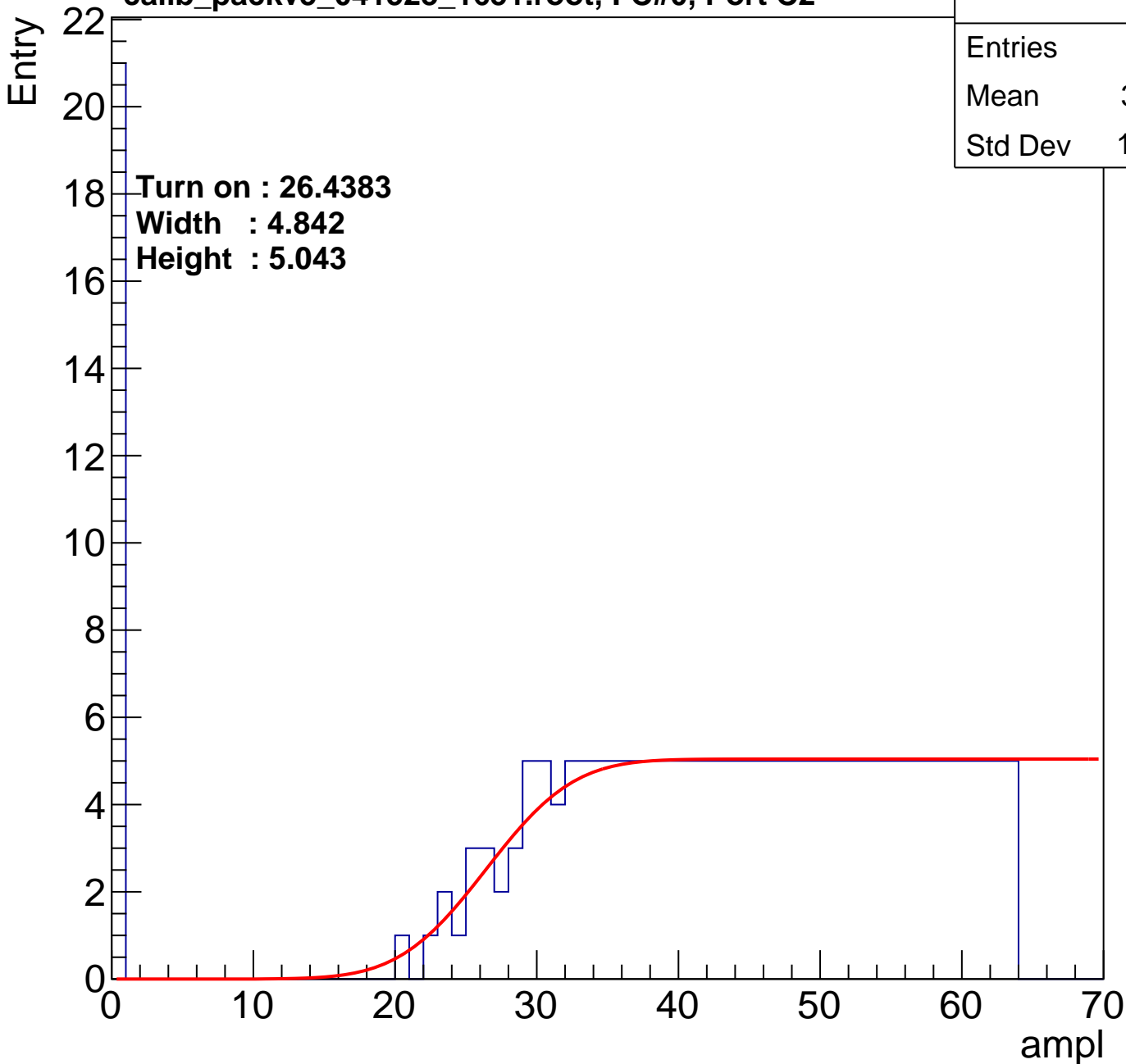
calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 211   |
| Mean    | 39.91 |
| Std Dev | 17.04 |

Turn on : 26.4383

Width : 4.842

Height : 5.043





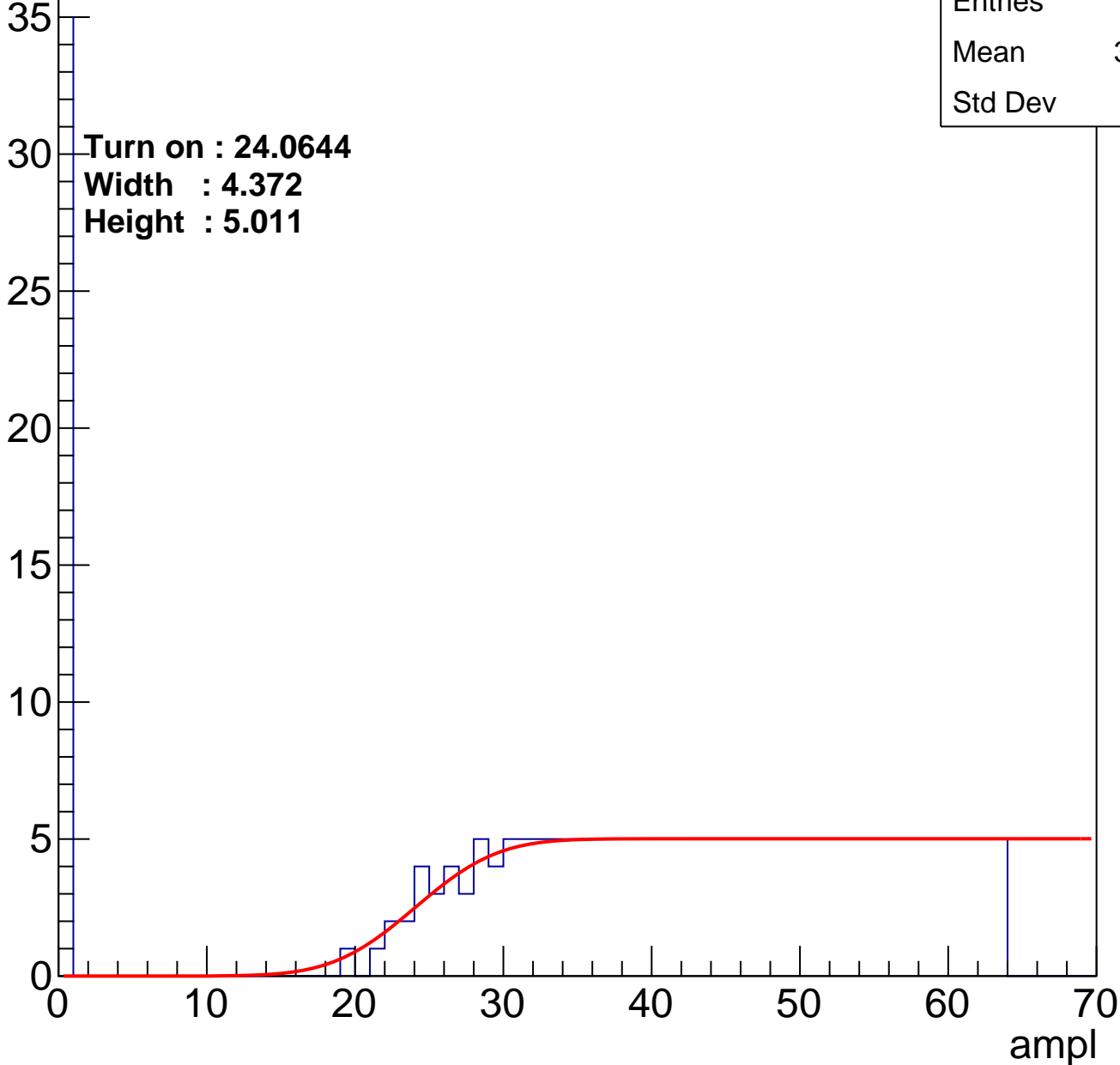
# B1L103S, U15-ch80

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 234   |
| Mean    | 36.95 |
| Std Dev | 18.9  |

Turn on : 24.0644  
Width : 4.372  
Height : 5.011

Entry



# B1L103S, U15-ch81

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 213   |
| Mean    | 39.27 |
| Std Dev | 17.86 |

**Turn on : 26.9496**

**Width : 3.111**

**Height : 5.032**

Entry

25

20

15

10

5

0

0

10

20

30

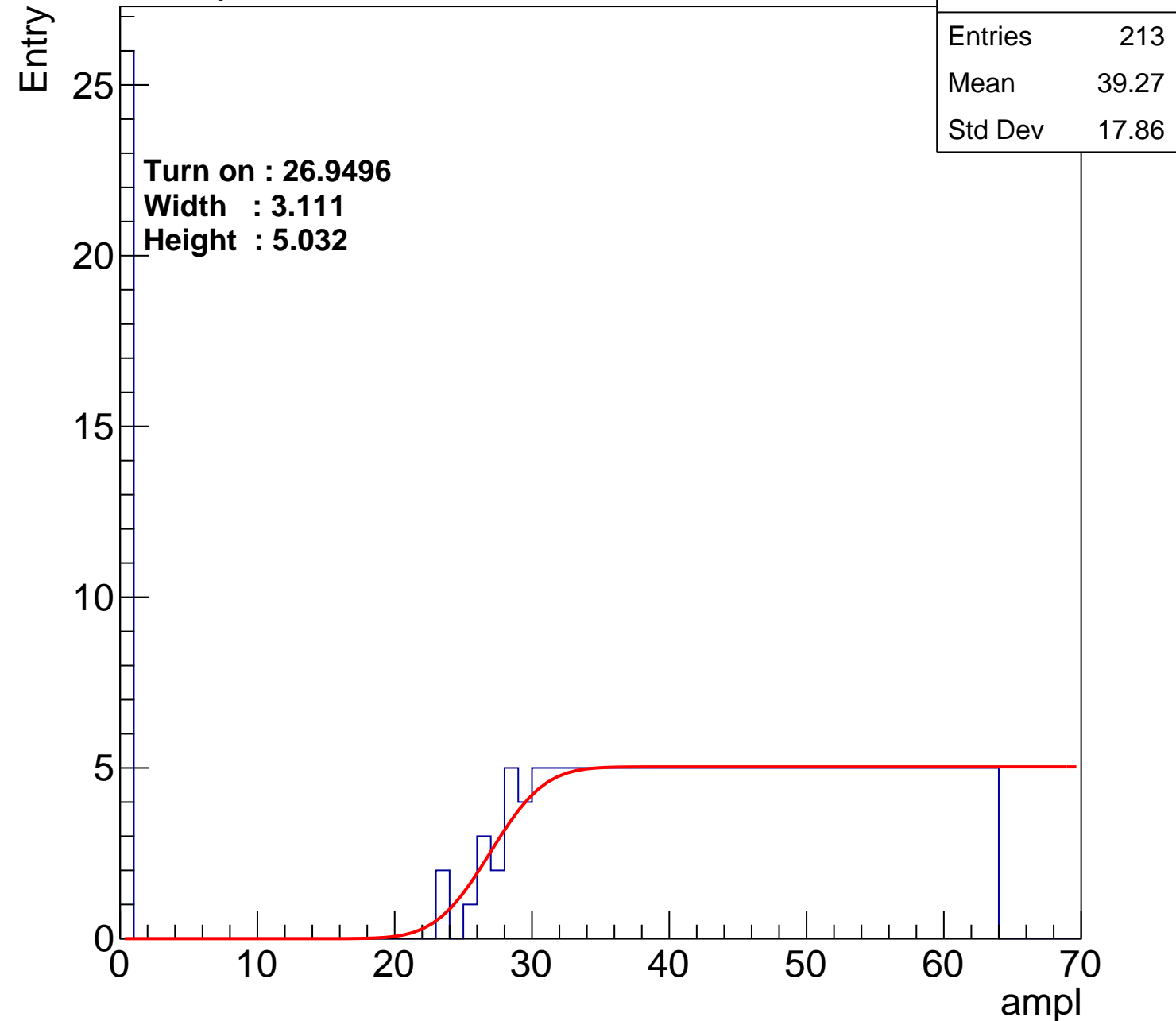
40

50

60

70

ampl



# B1L103S, U15-ch82

calib\_packv5\_041523\_1651.root, FC#0, Port C2

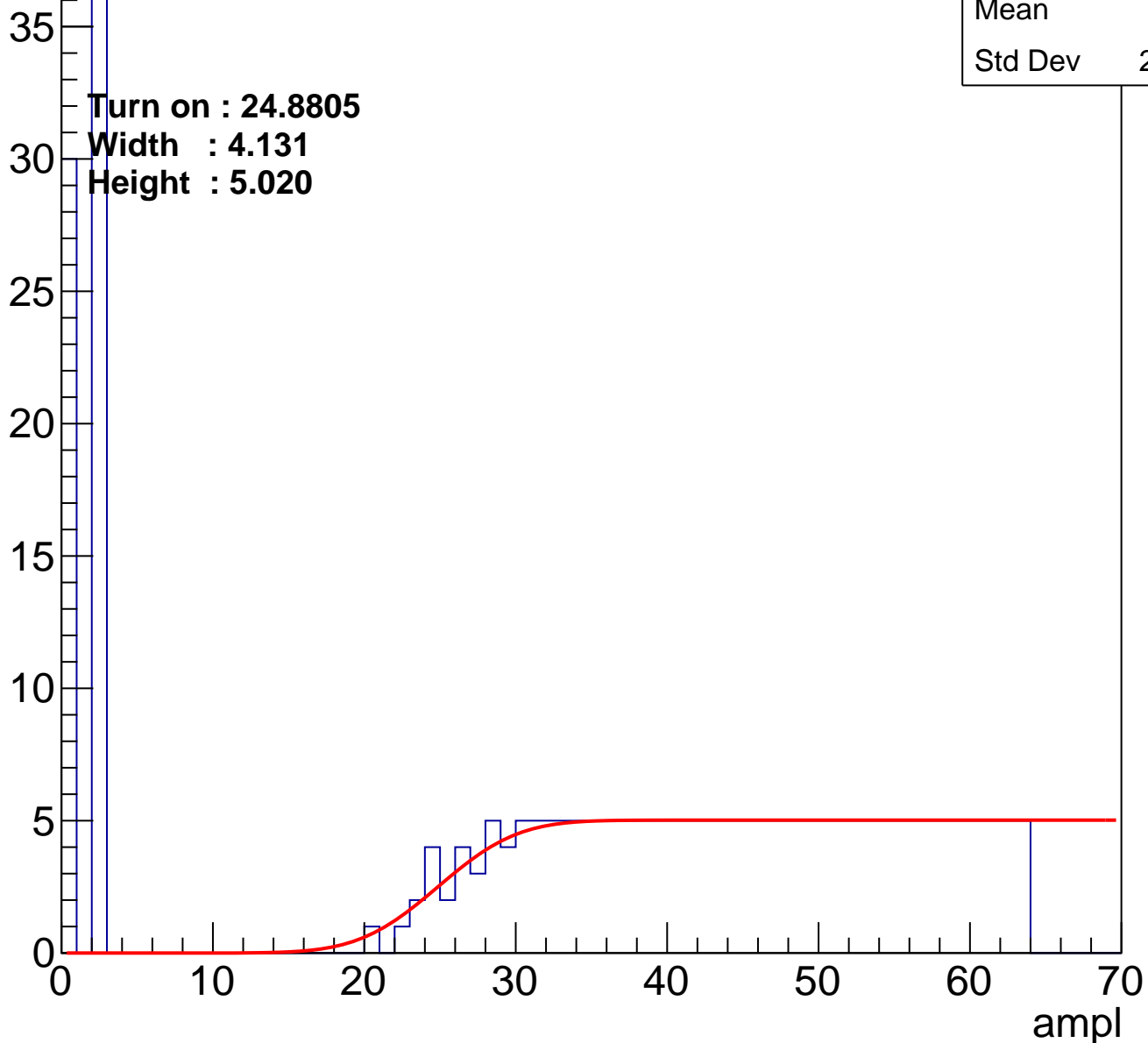
|         |       |
|---------|-------|
| Entries | 263   |
| Mean    | 32.9  |
| Std Dev | 21.09 |

Turn on : 24.8805

Width : 4.131

Height : 5.020

Entry

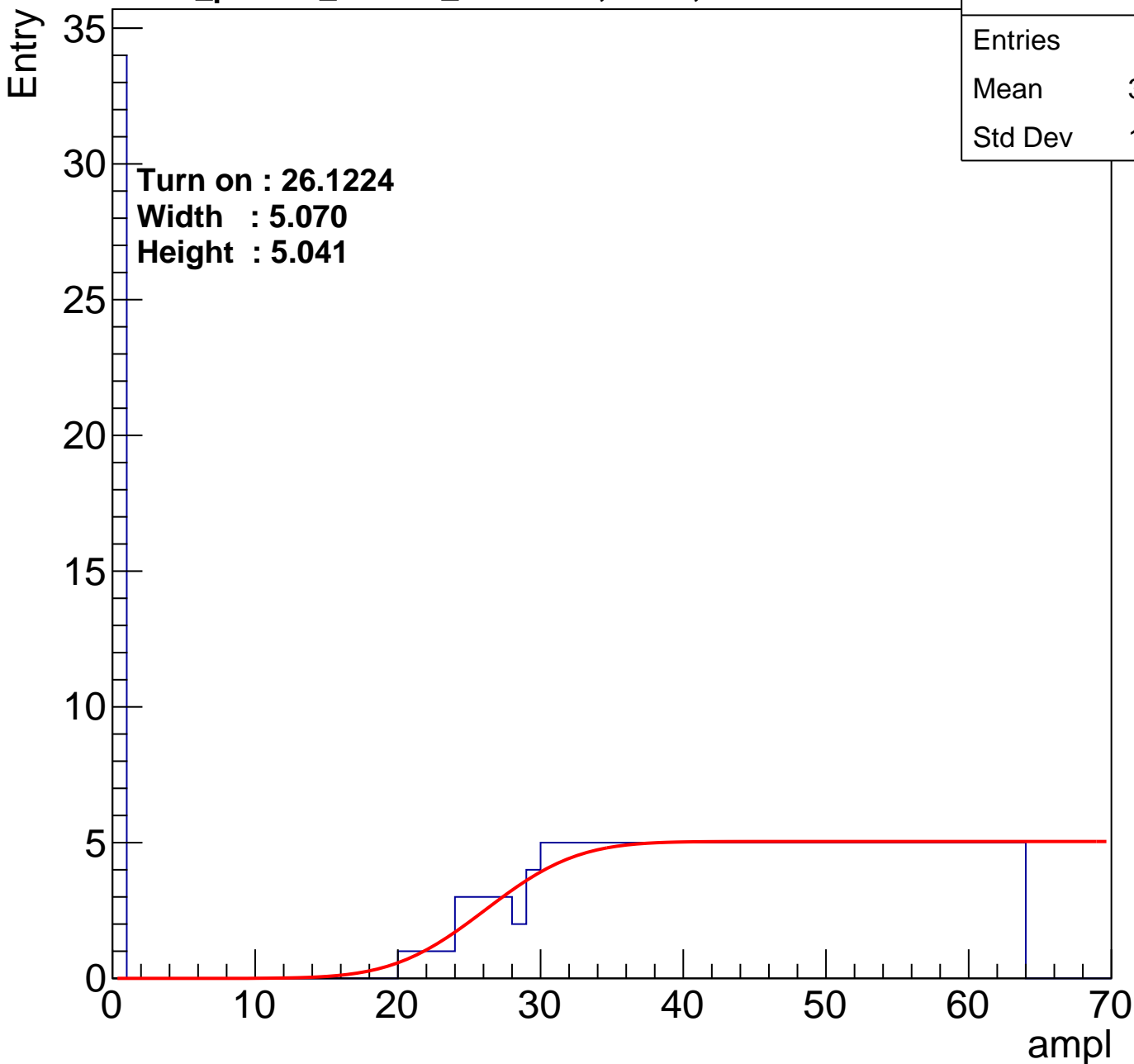


# B1L103S, U15-ch83

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 226   |
| Mean    | 37.47 |
| Std Dev | 18.95 |

Turn on : 26.1224  
Width : 5.070  
Height : 5.041



# B1L103S, U15-ch84

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 227   |
| Mean    | 37.79 |
| Std Dev | 18.46 |

**Turn on : 24.5465**

**Width : 3.941**

**Height : 5.003**

Entry

30

25

20

15

10

5

0

0

10

20

30

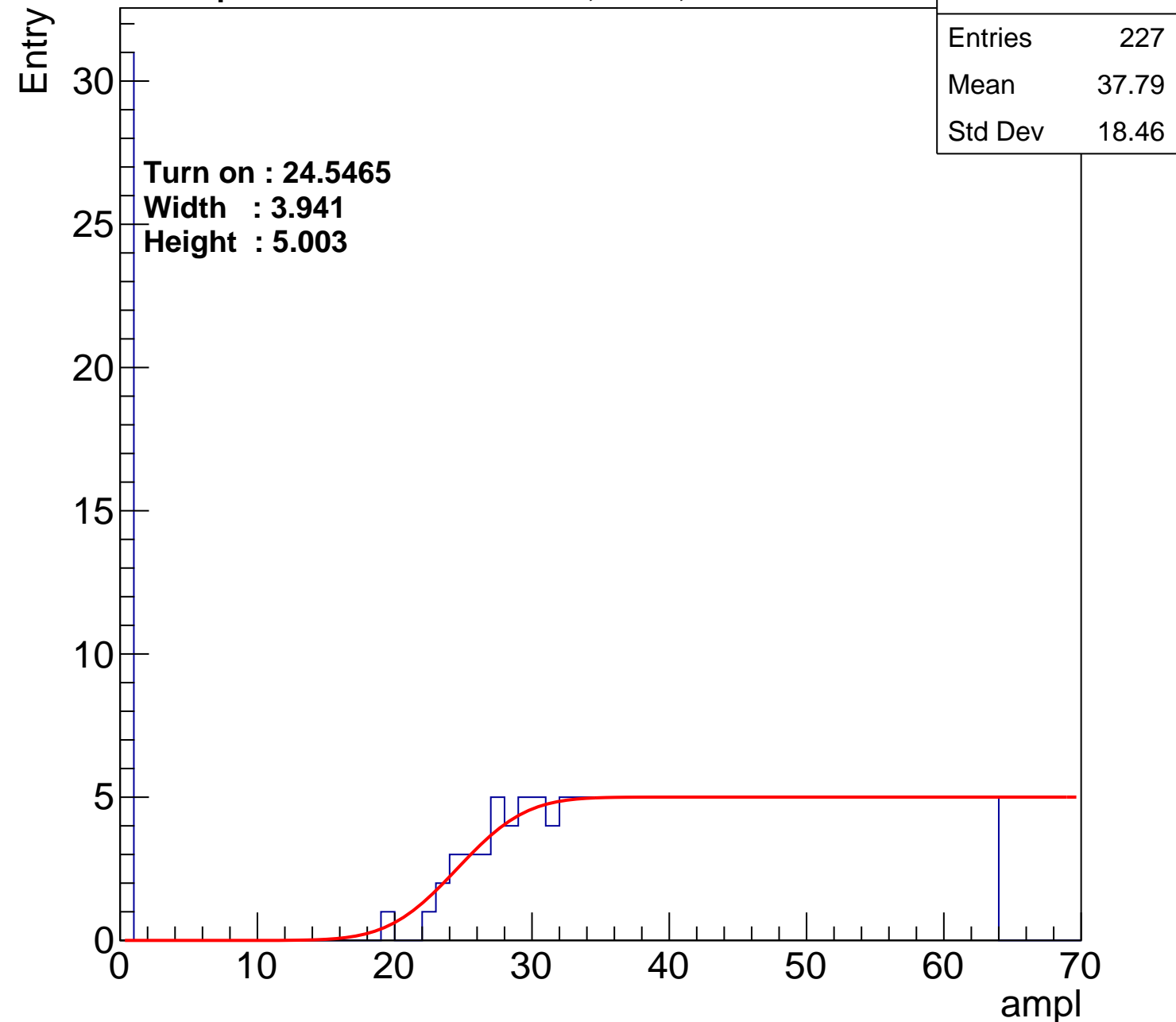
40

50

60

70

ampl



# B1L103S, U15-ch85

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 216   |
| Mean    | 39.09 |
| Std Dev | 17.81 |

**Turn on : 26.5453**

**Width : 2.646**

**Height : 5.035**

Entry

25

20

15

10

5

0

0

10

20

30

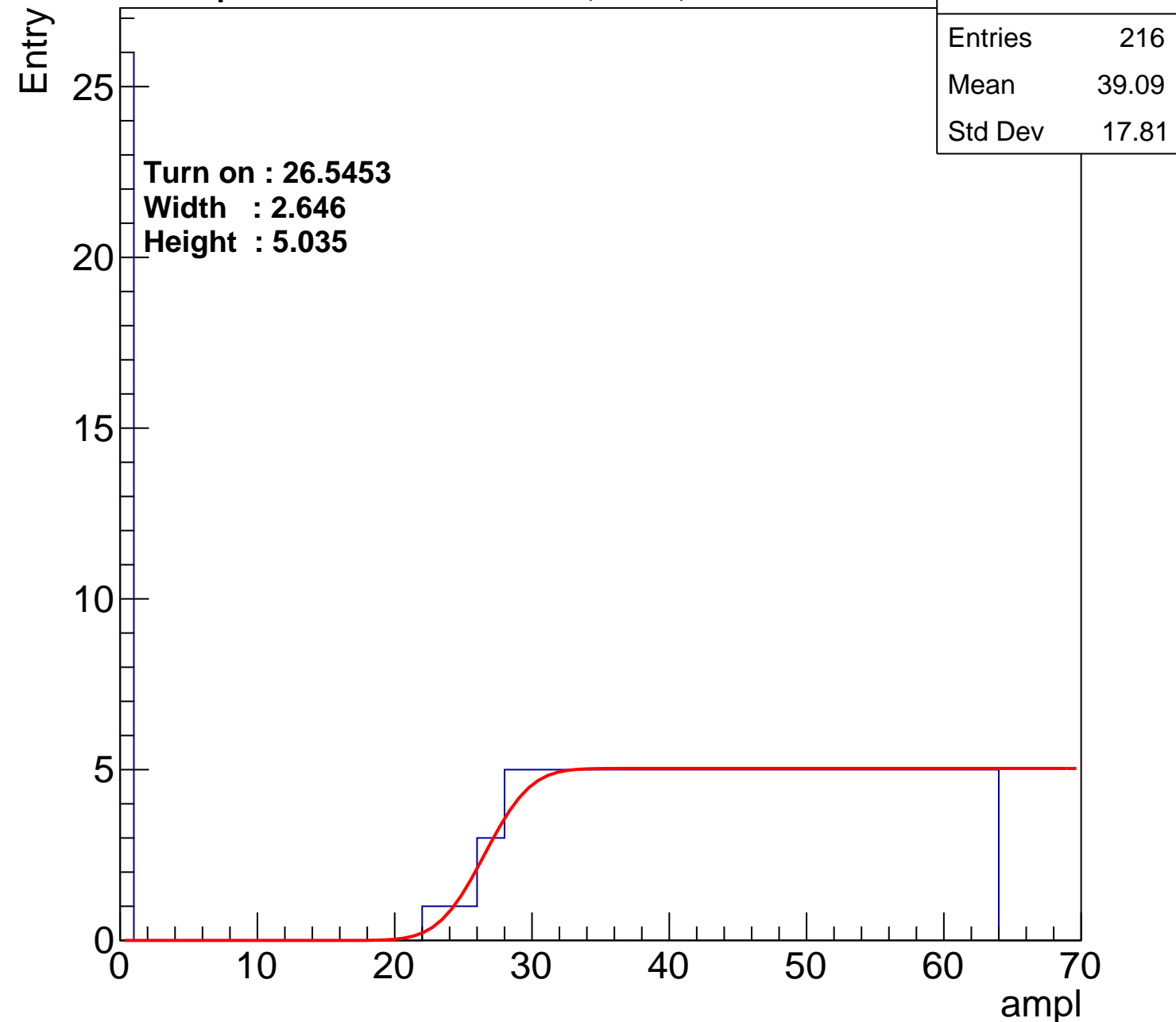
40

50

60

70

ampl

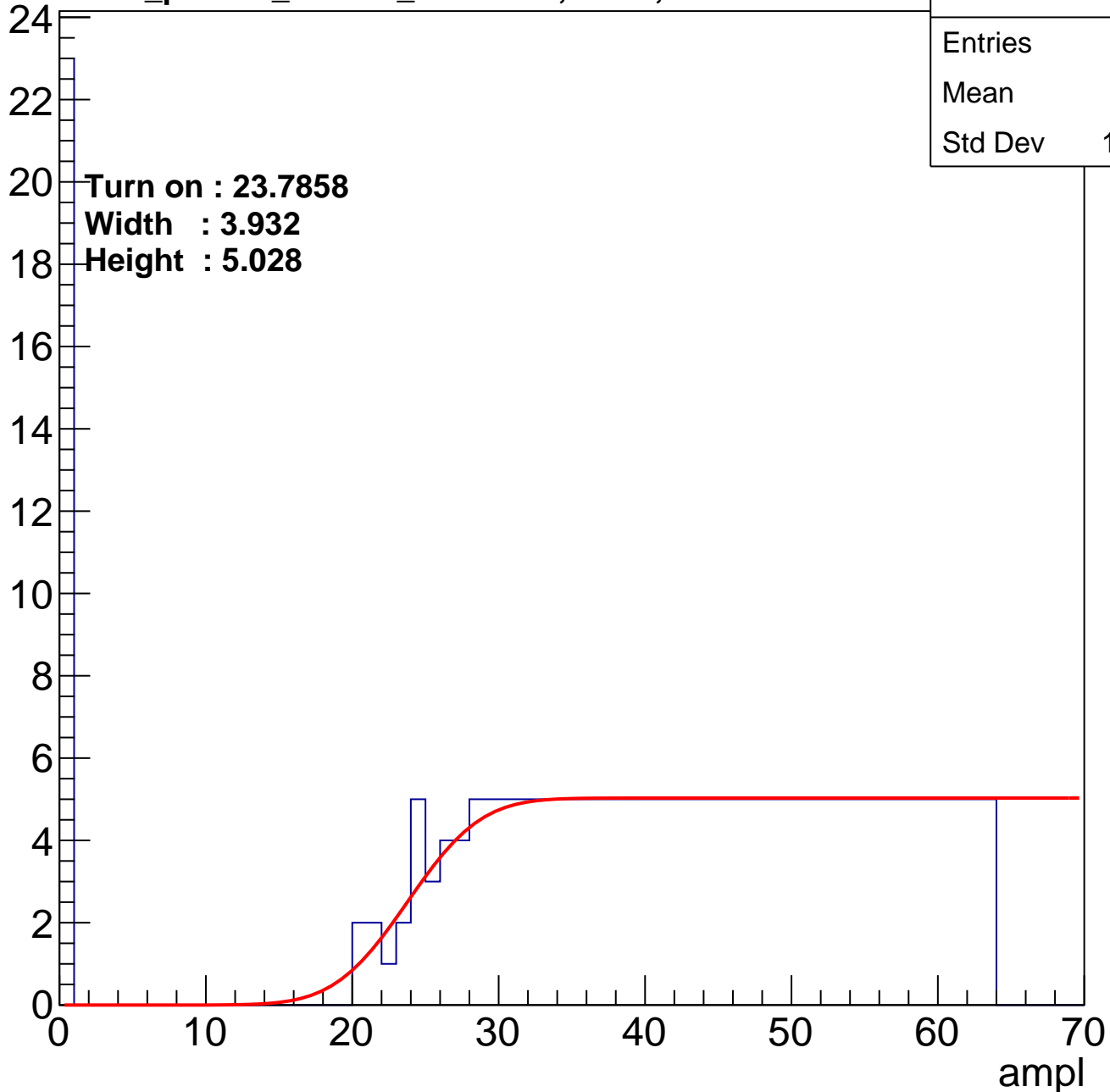


# B1L103S, U15-ch86

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 226   |
| Mean    | 38.7  |
| Std Dev | 17.23 |

Entry



# B1L103S, U15-ch87

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 215   |
| Mean    | 39.17 |
| Std Dev | 17.73 |

**Turn on : 26.9232**

**Width : 4.363**

**Height : 5.063**

Entry

25

20

15

10

5

0

0

10

20

30

40

50

60

70

ampl

0



# B1L103S, U15-ch88

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 226   |
| Mean    | 37.89 |
| Std Dev | 18.45 |

**Turn on : 24.4250**

**Width : 4.416**

**Height : 5.036**

Entry

30

25

20

15

10

5

0

0

10

20

30

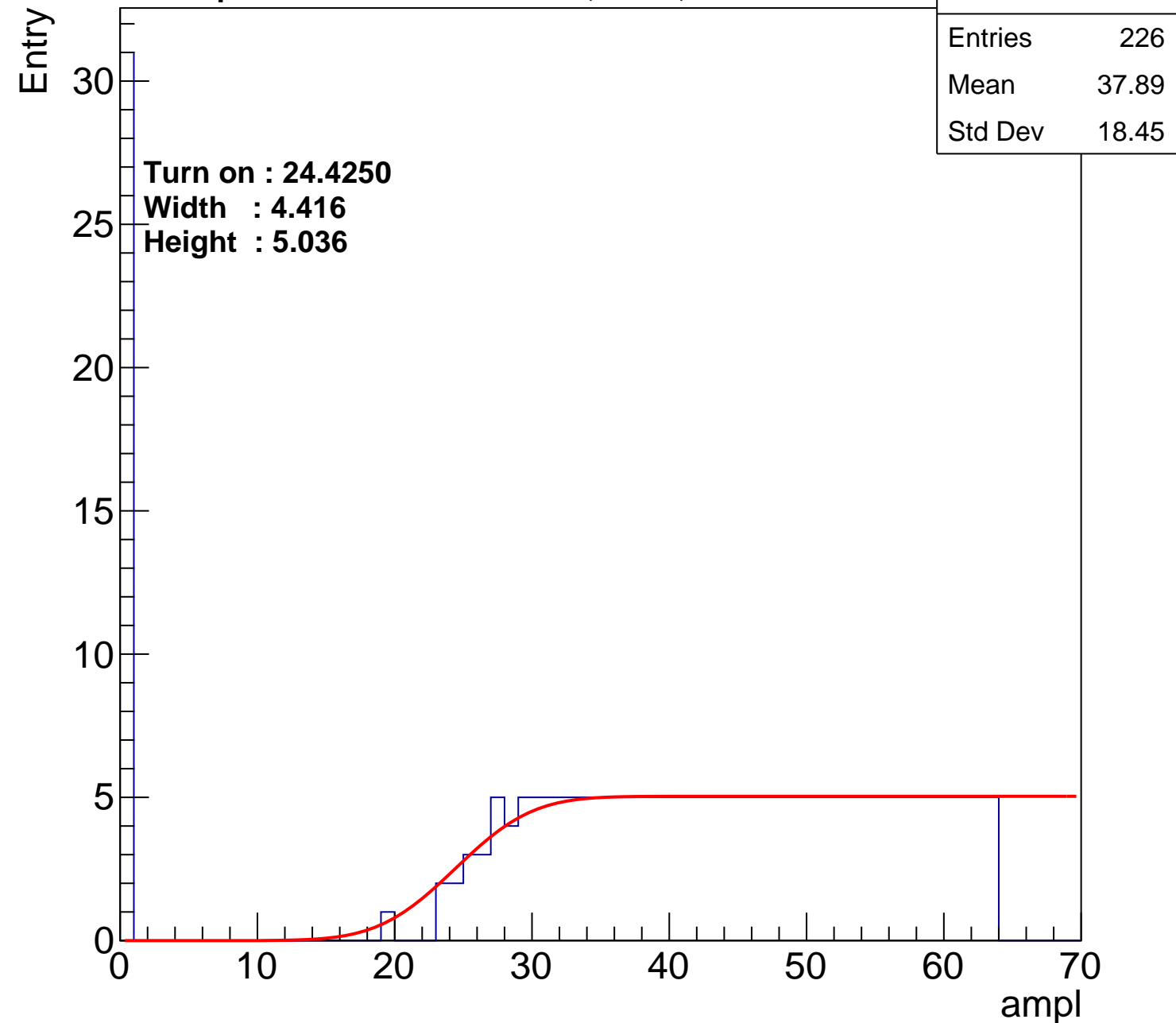
40

50

60

70

ampl



# B1L103S, U15-ch89

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 206   |
| Mean    | 40.46 |
| Std Dev | 16.82 |

**Turn on : 26.7704**

**Width : 2.620**

**Height : 4.981**

Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

ampl

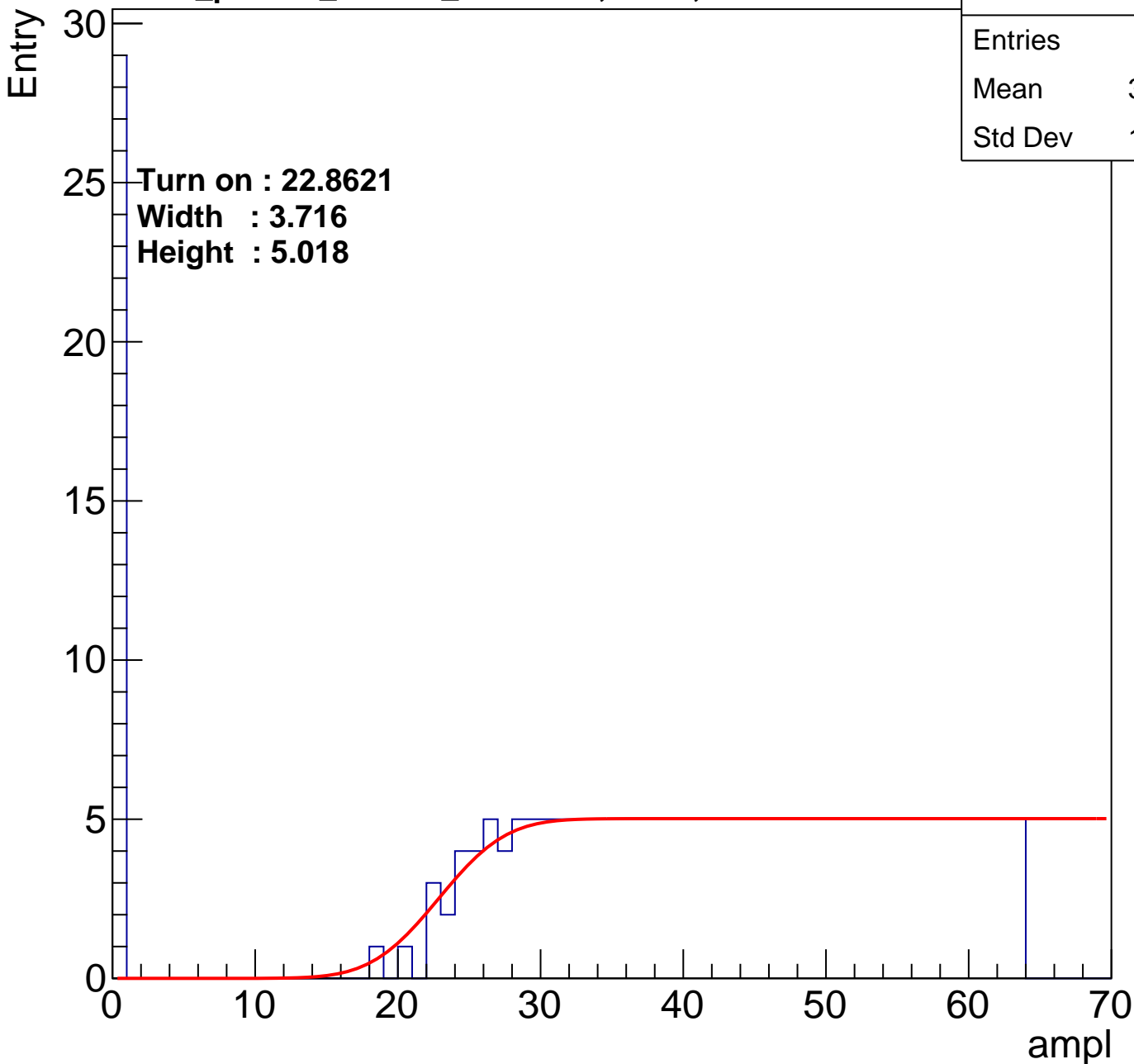
0 10 20 30 40 50 60 70

# B1L103S, U15-ch90

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 233   |
| Mean    | 37.66 |
| Std Dev | 18.06 |

Turn on : 22.8621  
Width : 3.716  
Height : 5.018



# B1L103S, U15-ch91

calib\_packv5\_041523\_1651.root, FC#0, Port C2

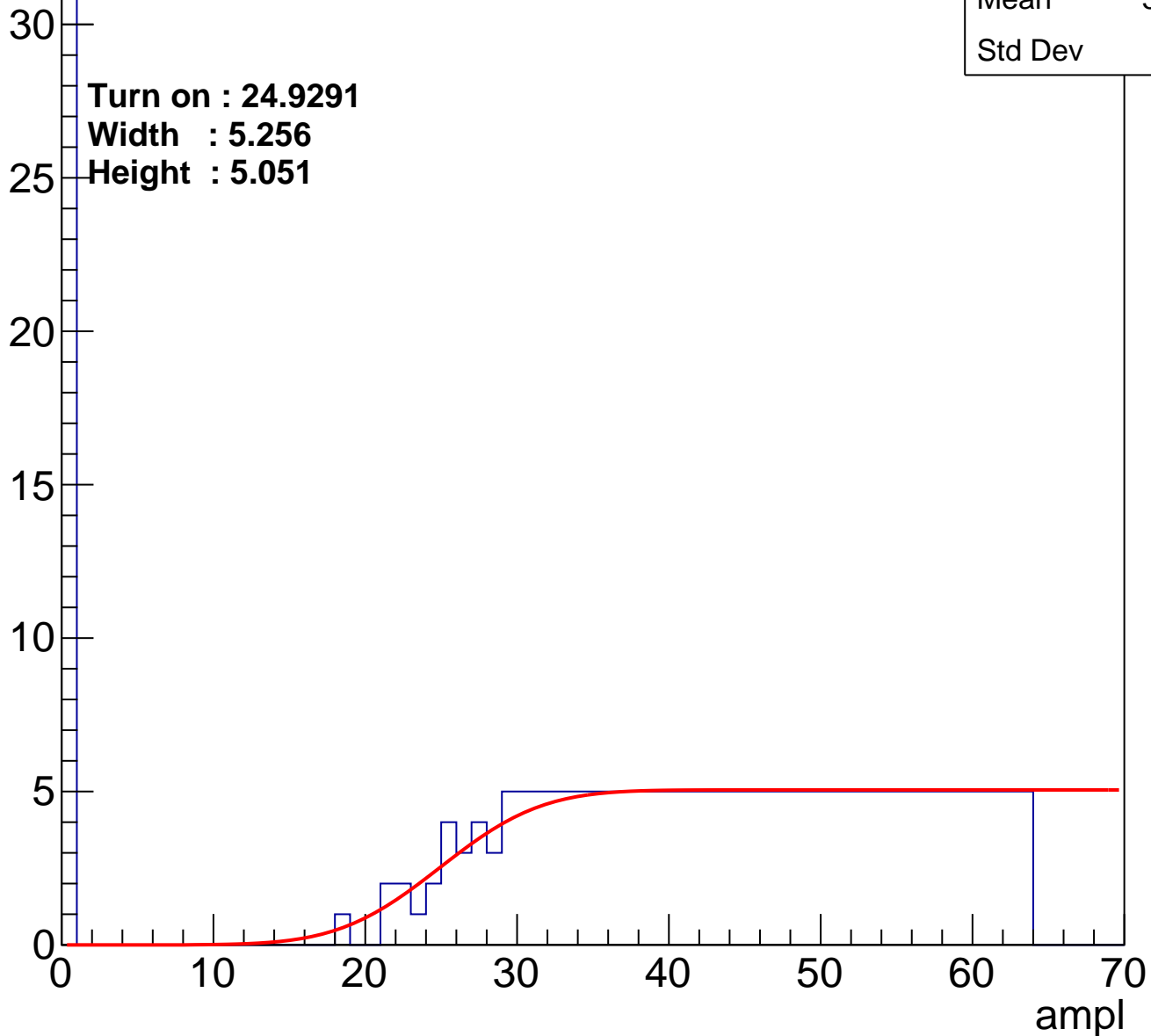
|         |       |
|---------|-------|
| Entries | 229   |
| Mean    | 37.53 |
| Std Dev | 18.6  |

**Turn on : 24.9291**

**Width : 5.256**

**Height : 5.051**

Entry



# B1L103S, U15-ch92

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 229   |
| Mean    | 37.97 |
| Std Dev | 18    |

**Turn on : 24.0759**

**Width : 4.003**

**Height : 5.020**

Entry

25

20

15

10

5

0

0

10

20

30

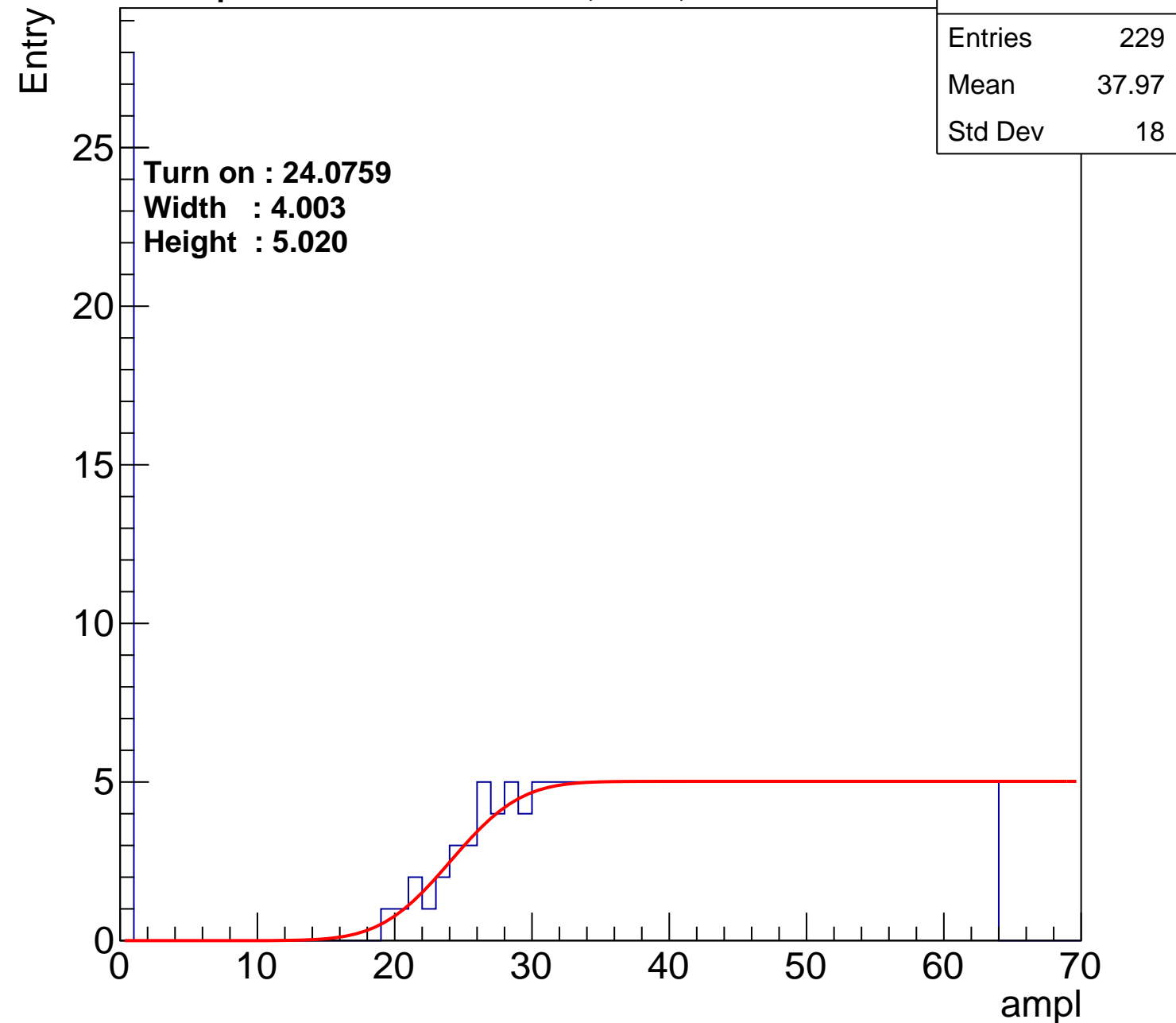
40

50

60

70

ampl

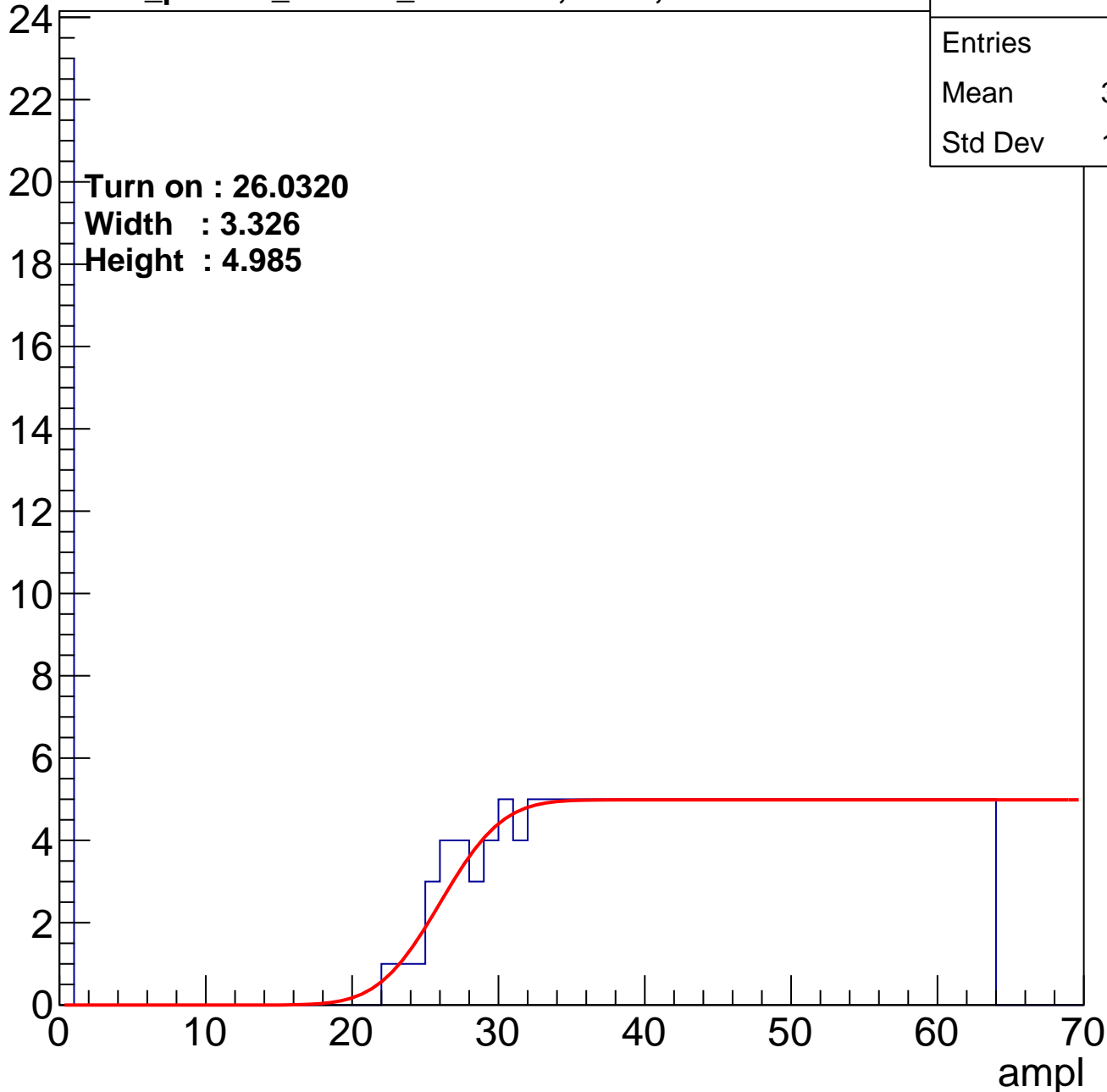


# B1L103S, U15-ch93

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 213   |
| Mean    | 39.58 |
| Std Dev | 17.35 |

Entry



# B1L103S, U15-ch94

calib\_packv5\_041523\_1651.root, FC#0, Port C2

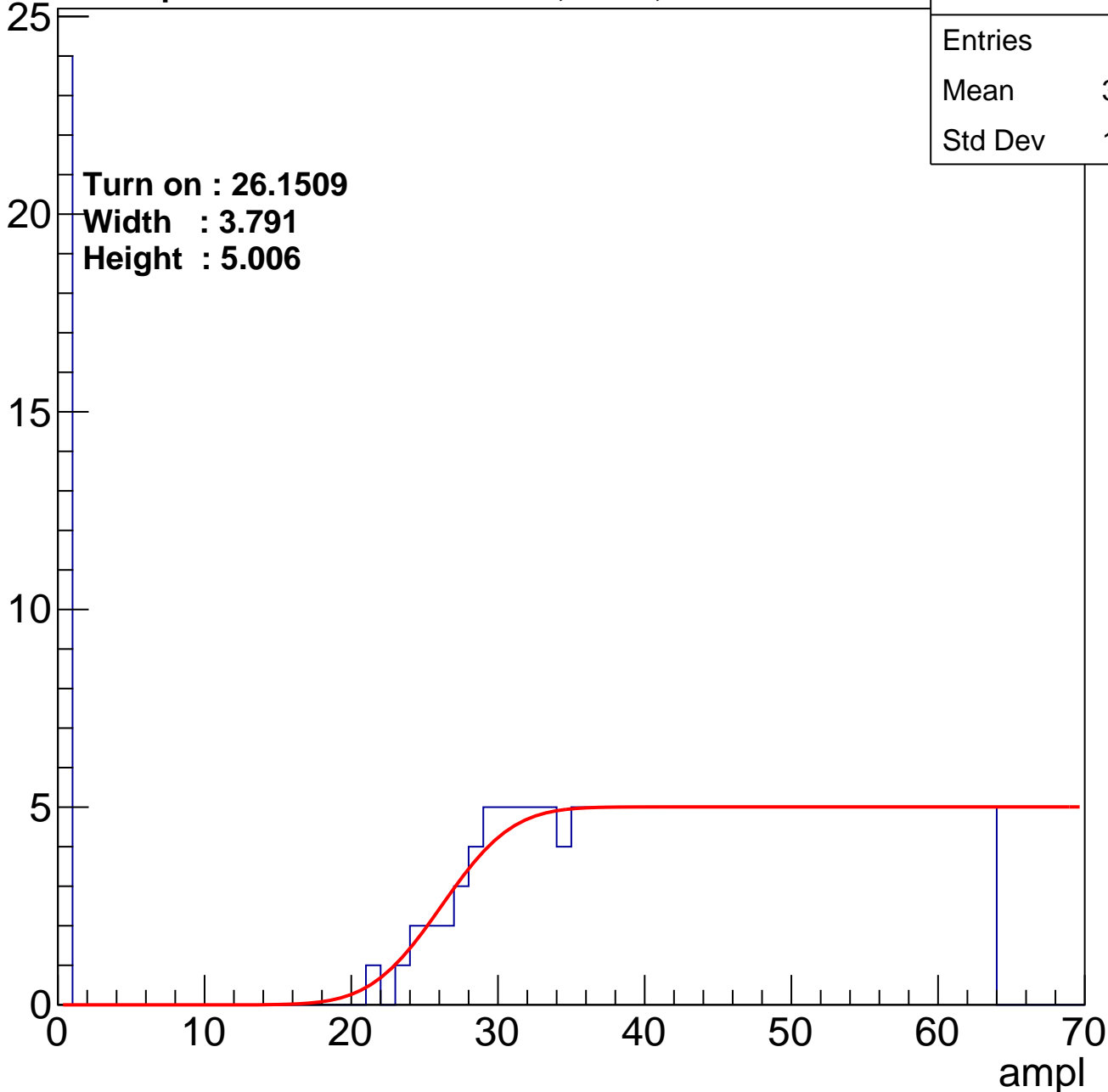
|         |       |
|---------|-------|
| Entries | 213   |
| Mean    | 39.45 |
| Std Dev | 17.54 |

Turn on : 26.1509

Width : 3.791

Height : 5.006

Entry



# B1L103S, U15-ch95

calib\_packv5\_041523\_1651.root, FC#0, Port C2

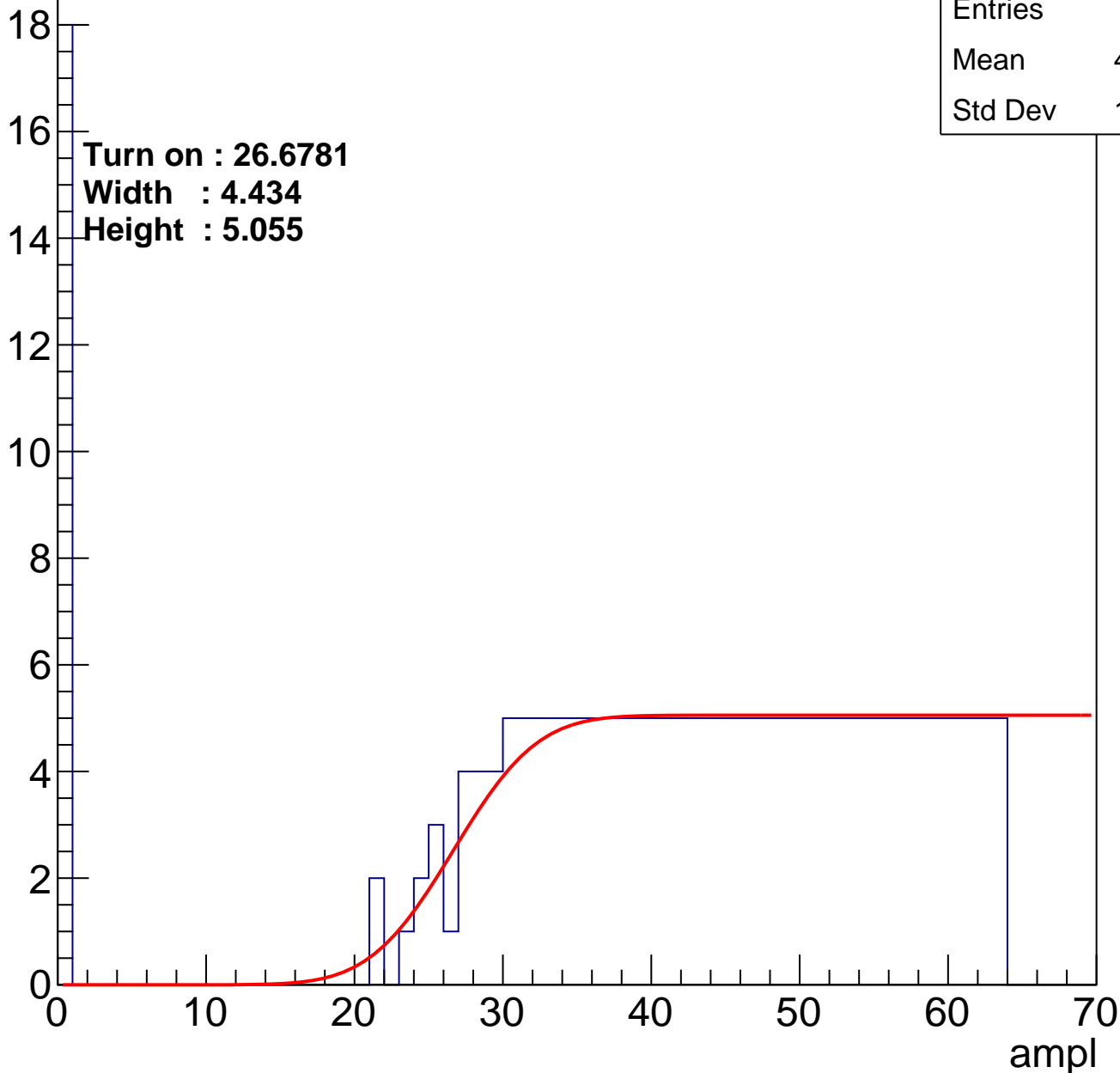
|         |       |
|---------|-------|
| Entries | 209   |
| Mean    | 40.45 |
| Std Dev | 16.43 |

Turn on : 26.6781

Width : 4.434

Height : 5.055

Entry





# B1L103S, U15-ch96

calib\_packv5\_041523\_1651.root, FC#0, Port C2

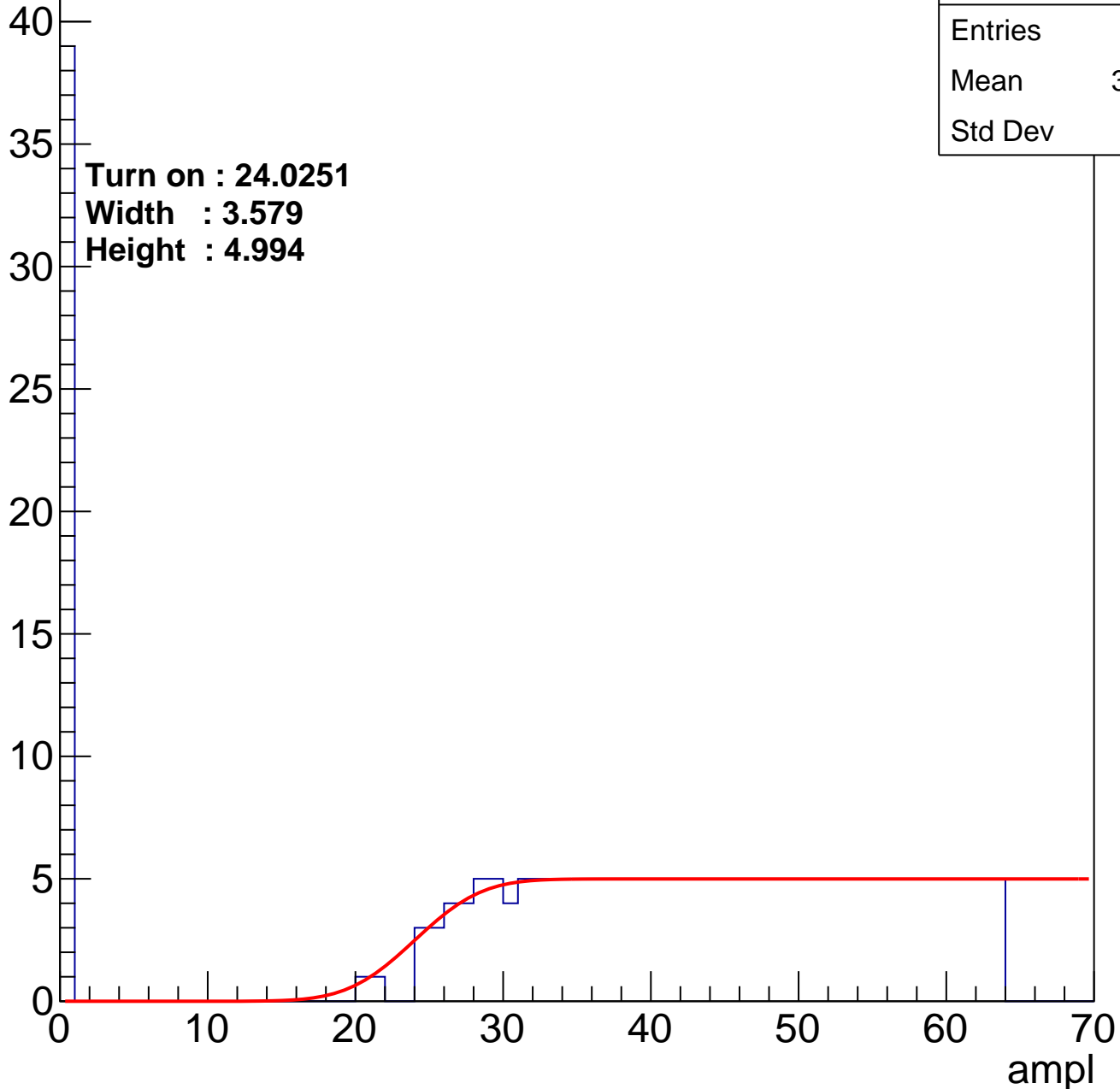
|         |       |
|---------|-------|
| Entries | 234   |
| Mean    | 36.58 |
| Std Dev | 19.4  |

**Turn on : 24.0251**

**Width : 3.579**

**Height : 4.994**

Entry



# B1L103S, U15-ch97

calib\_packv5\_041523\_1651.root, FC#0, Port C2

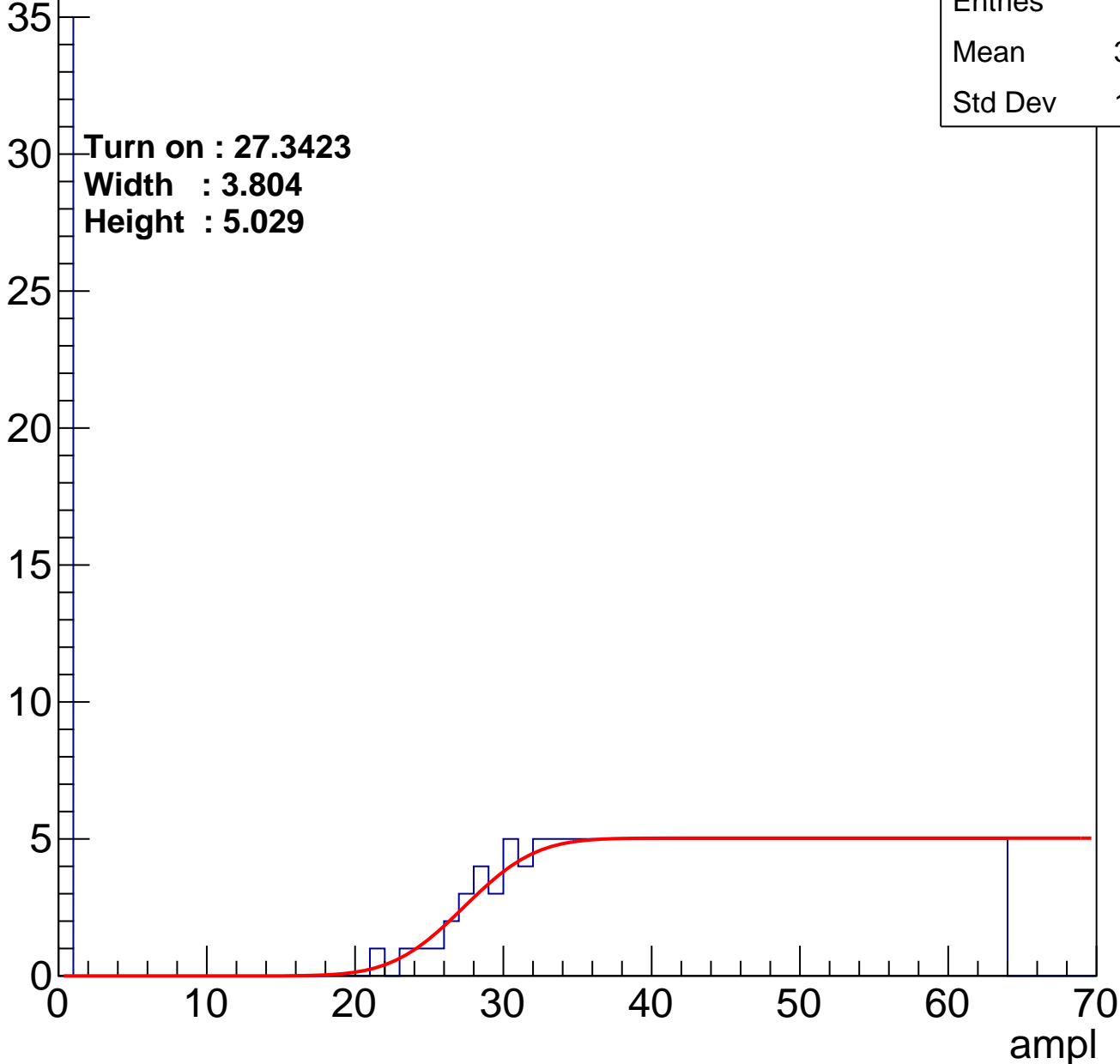
|         |       |
|---------|-------|
| Entries | 220   |
| Mean    | 37.72 |
| Std Dev | 19.22 |

Turn on : 27.3423

Width : 3.804

Height : 5.029

Entry



# B1L103S, U15-ch98

calib\_packv5\_041523\_1651.root, FC#0, Port C2

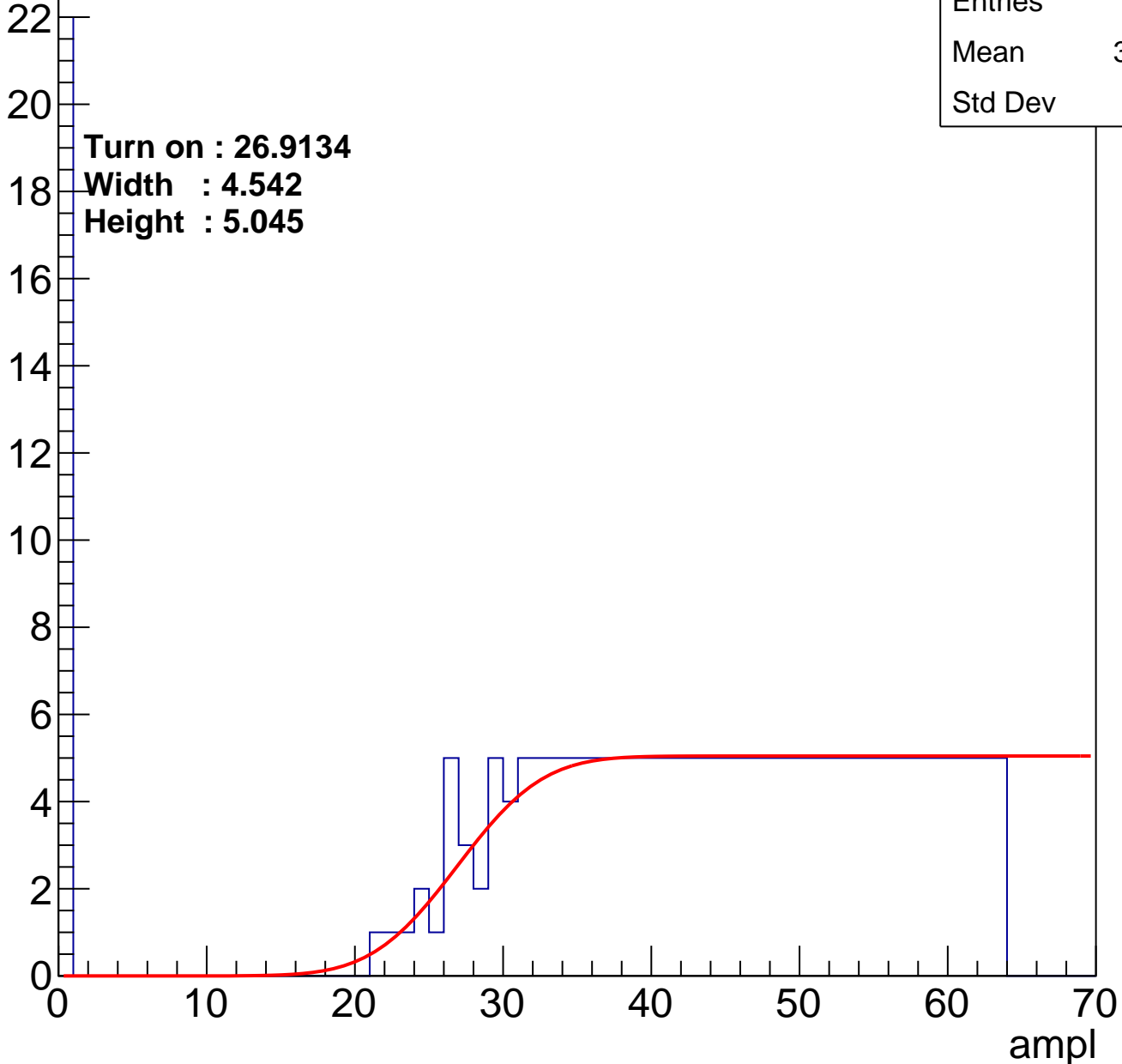
|         |       |
|---------|-------|
| Entries | 212   |
| Mean    | 39.75 |
| Std Dev | 17.2  |

**Turn on : 26.9134**

**Width : 4.542**

**Height : 5.045**

Entry

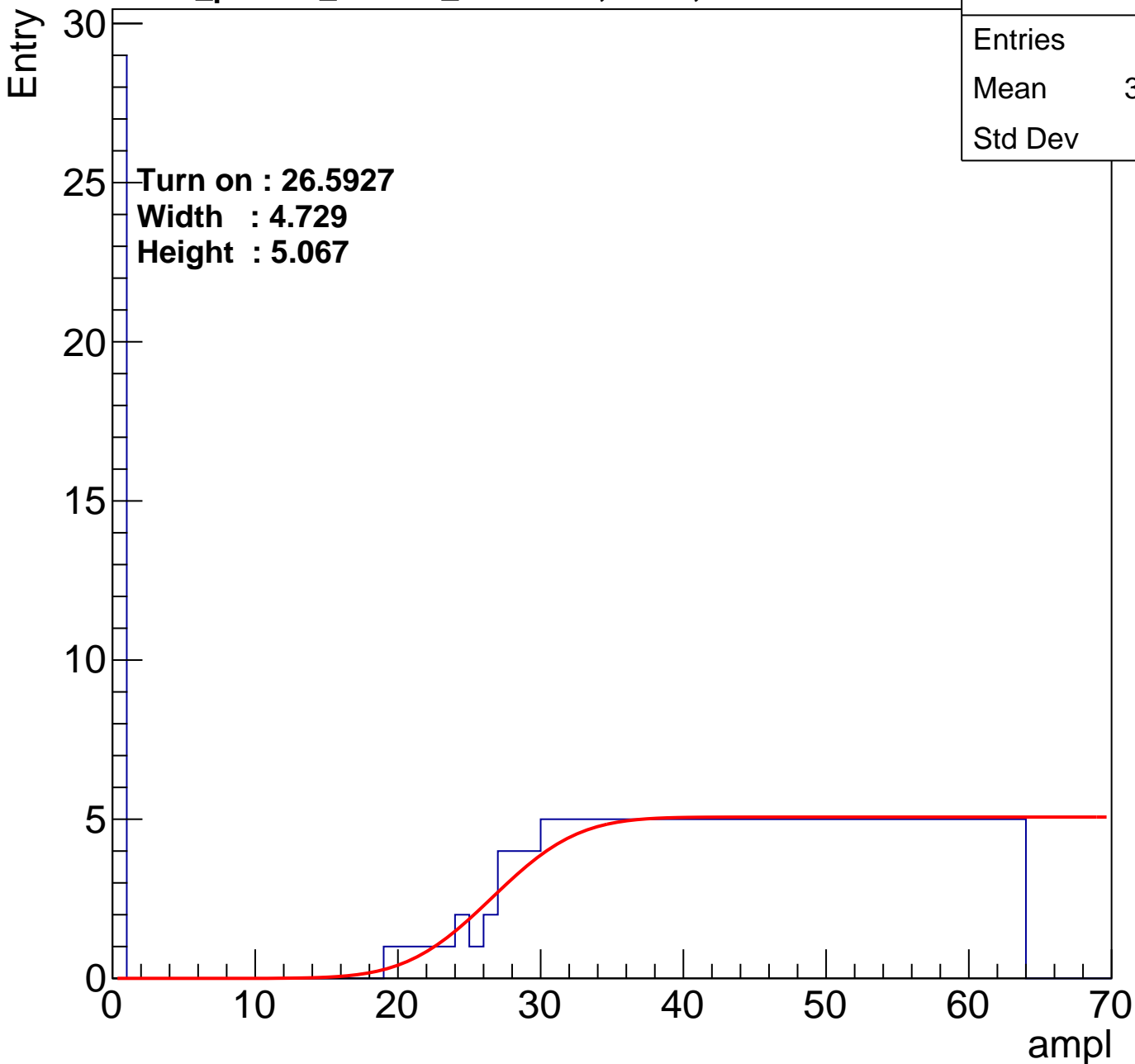


# B1L103S, U15-ch99

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 221   |
| Mean    | 38.33 |
| Std Dev | 18.3  |

Turn on : 26.5927  
Width : 4.729  
Height : 5.067



# B1L103S, U15-ch100

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 230   |
| Mean    | 37.63 |
| Std Dev | 18.39 |

**Turn on : 23.9247**

**Width : 3.081**

**Height : 4.986**

Entry

30

25

20

15

10

5

0

0

10

20

30

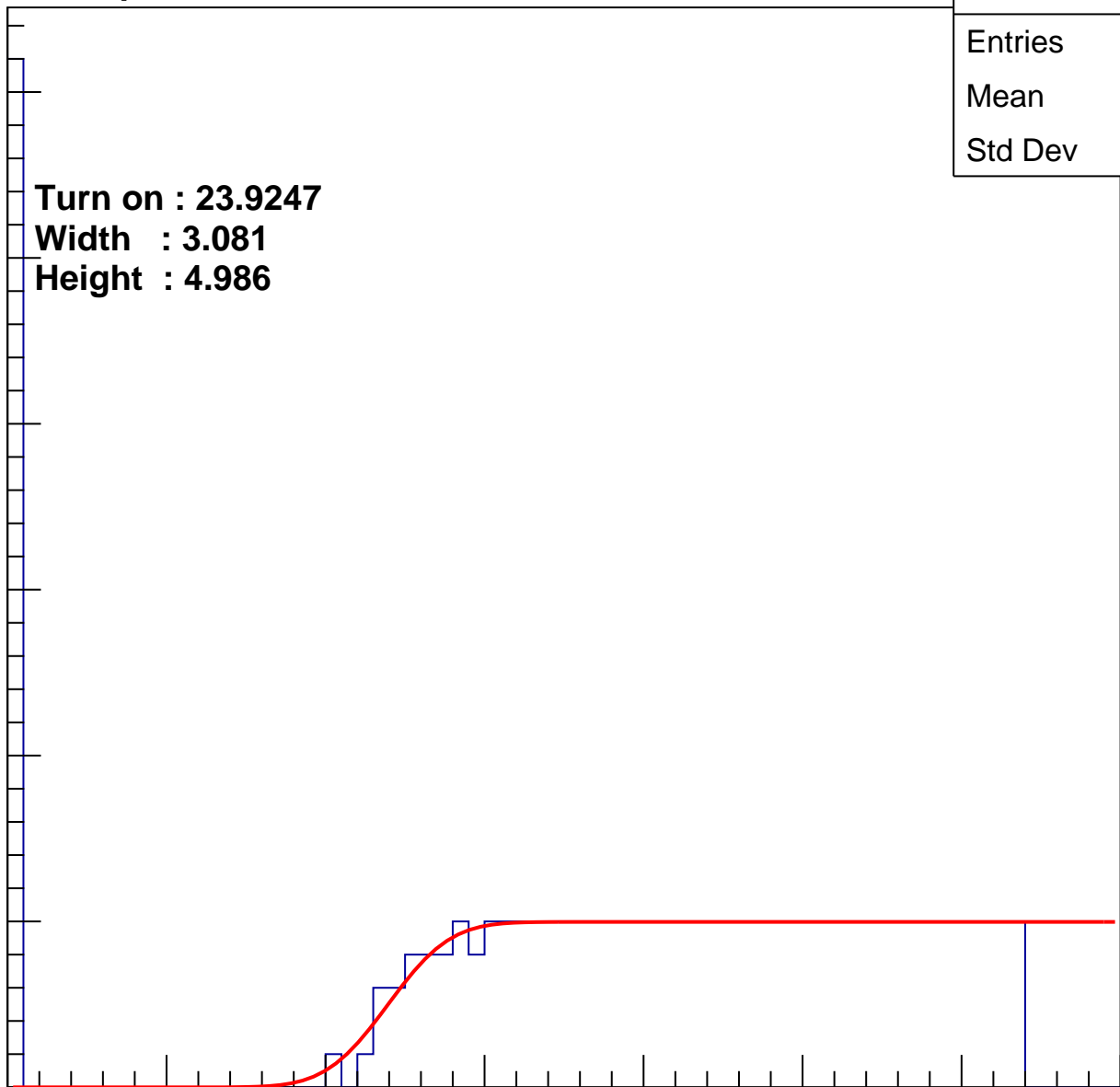
40

50

60

70

ampl



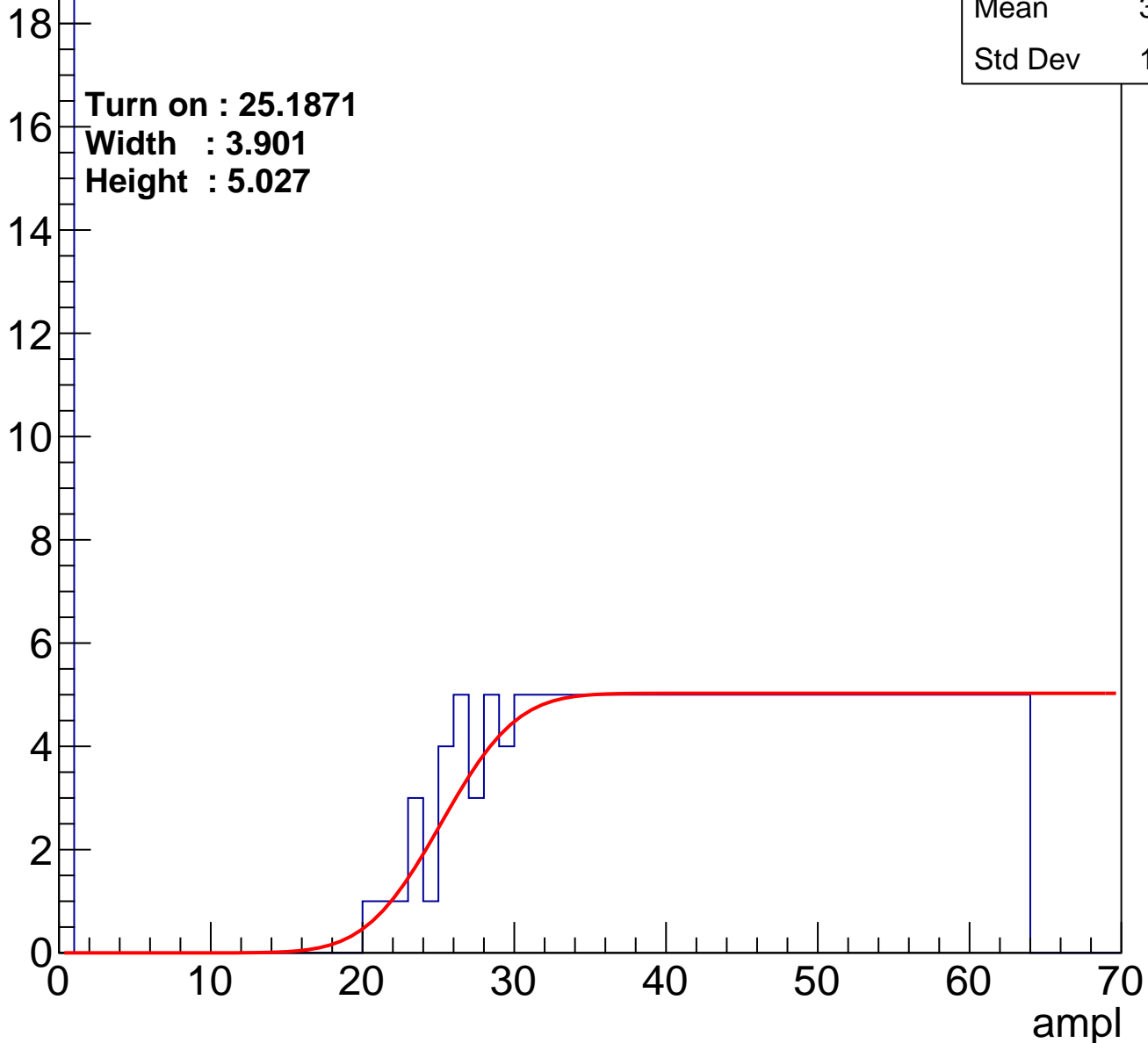
# B1L103S, U15-ch101

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 217   |
| Mean    | 39.76 |
| Std Dev | 16.59 |

**Turn on : 25.1871**  
**Width : 3.901**  
**Height : 5.027**

Entry



# B1L103S, U15-ch102

calib\_packv5\_041523\_1651.root, FC#0, Port C2

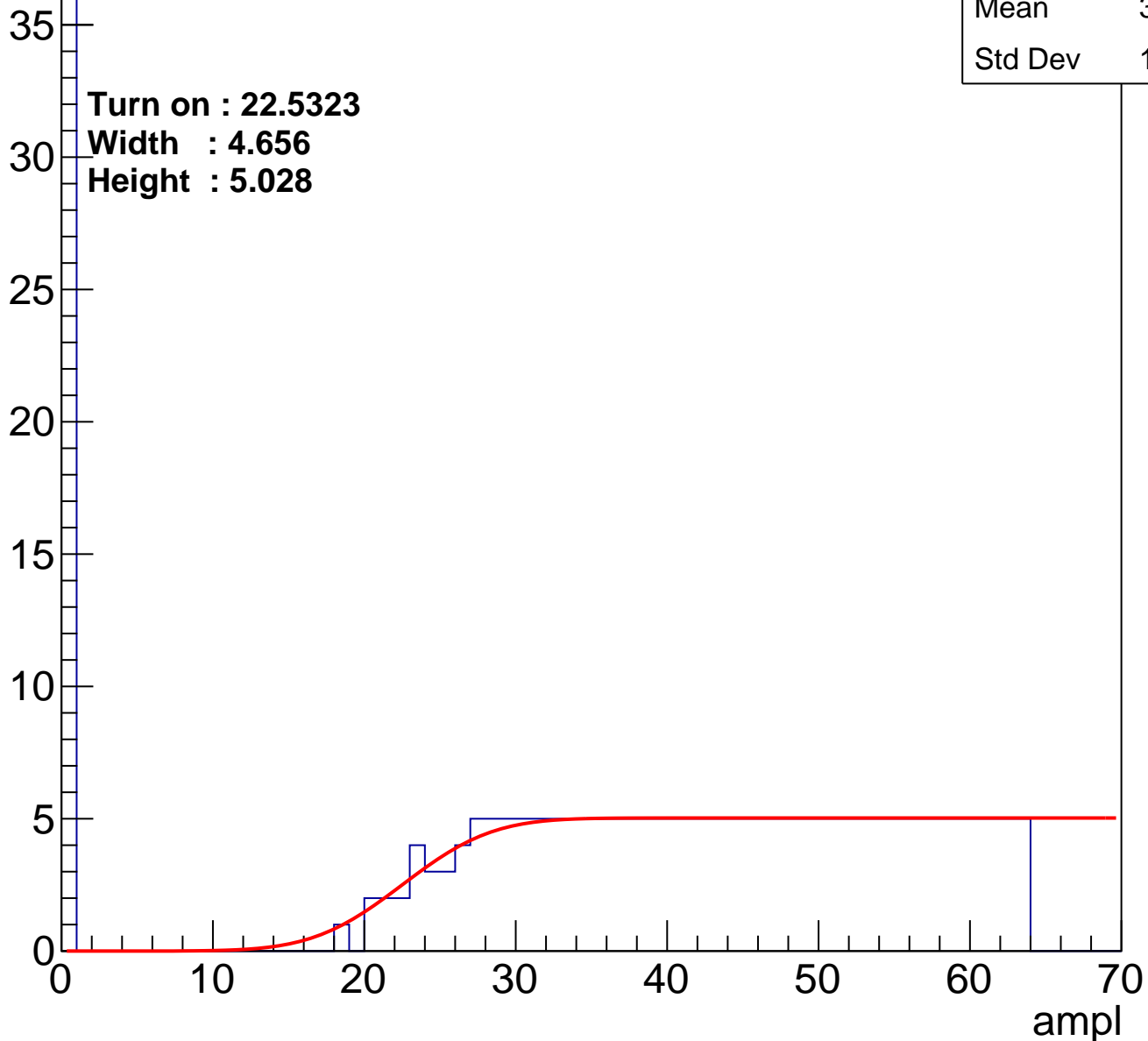
|         |       |
|---------|-------|
| Entries | 243   |
| Mean    | 36.26 |
| Std Dev | 18.98 |

**Turn on : 22.5323**

**Width : 4.656**

**Height : 5.028**

Entry



# B1L103S, U15-ch103

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 223   |
| Mean    | 38.37 |
| Std Dev | 18.07 |

**Turn on : 25.1746**  
**Width : 2.927**  
**Height : 5.007**

Entry

25

20

15

10

5

0

ampl

0

10

20

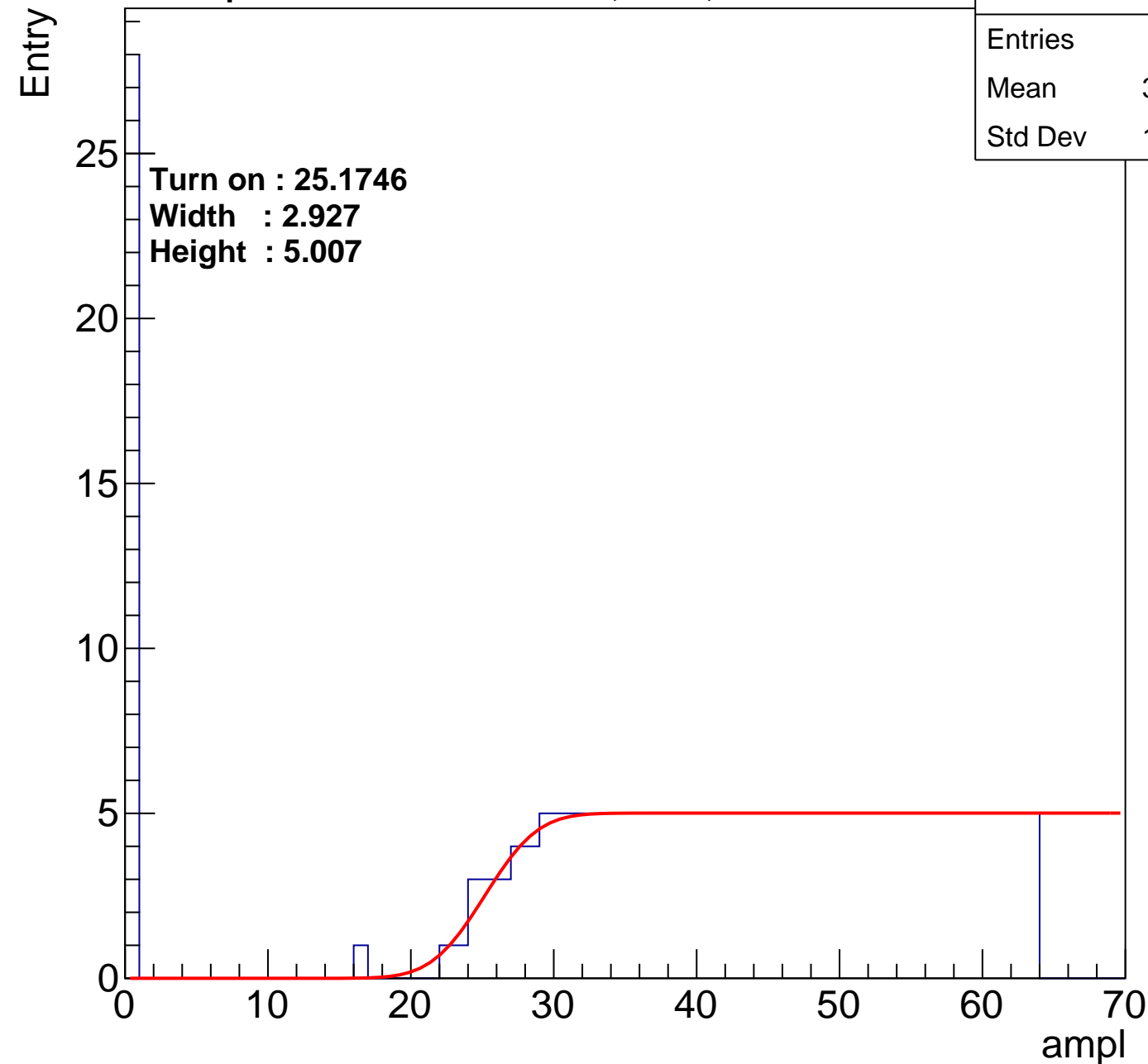
30

40

50

60

70





# B1L103S, U15-ch104

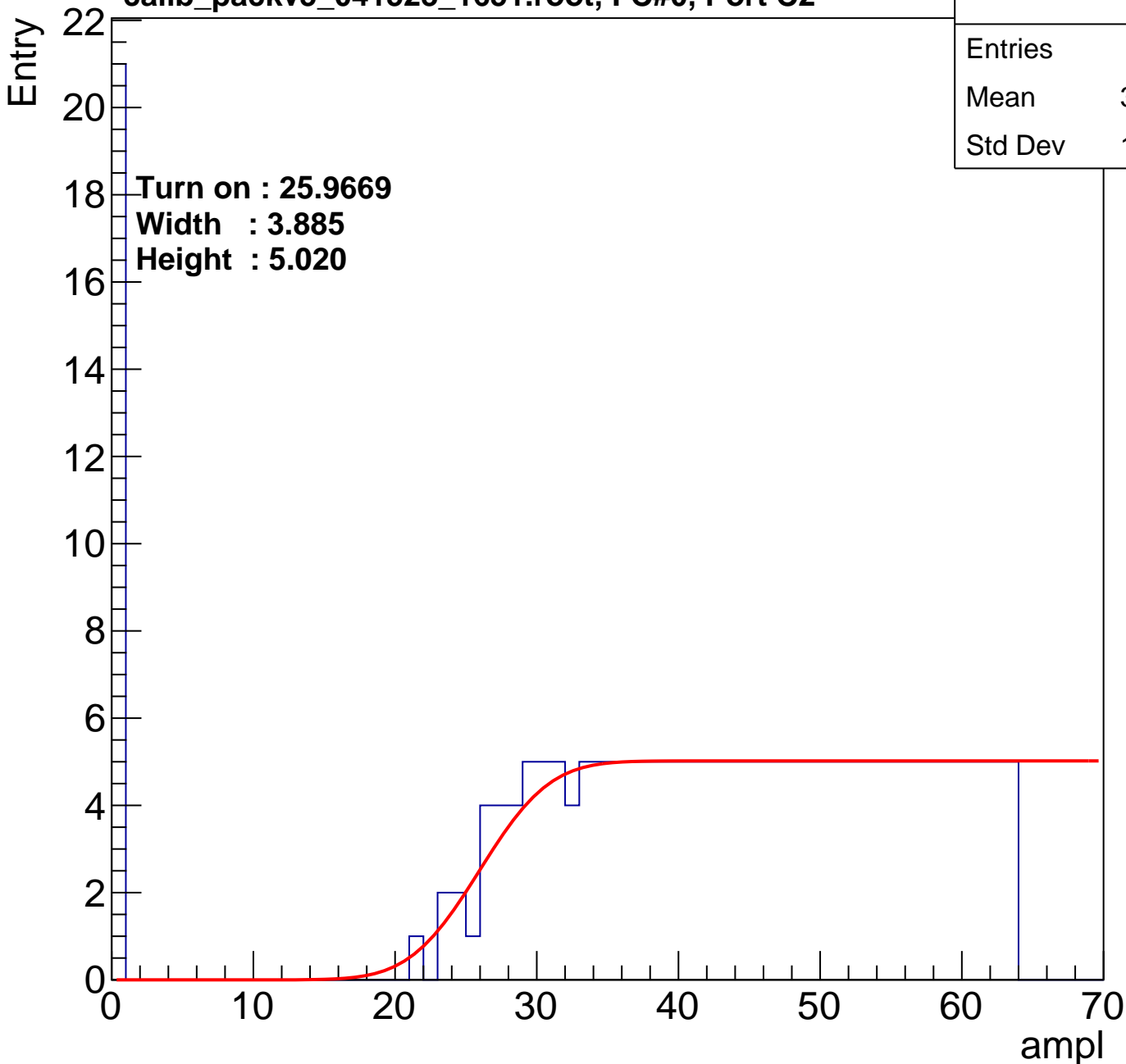
calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 213   |
| Mean    | 39.82 |
| Std Dev | 16.98 |

Turn on : 25.9669

Width : 3.885

Height : 5.020



# B1L103S, U15-ch105

calib\_packv5\_041523\_1651.root, FC#0, Port C2

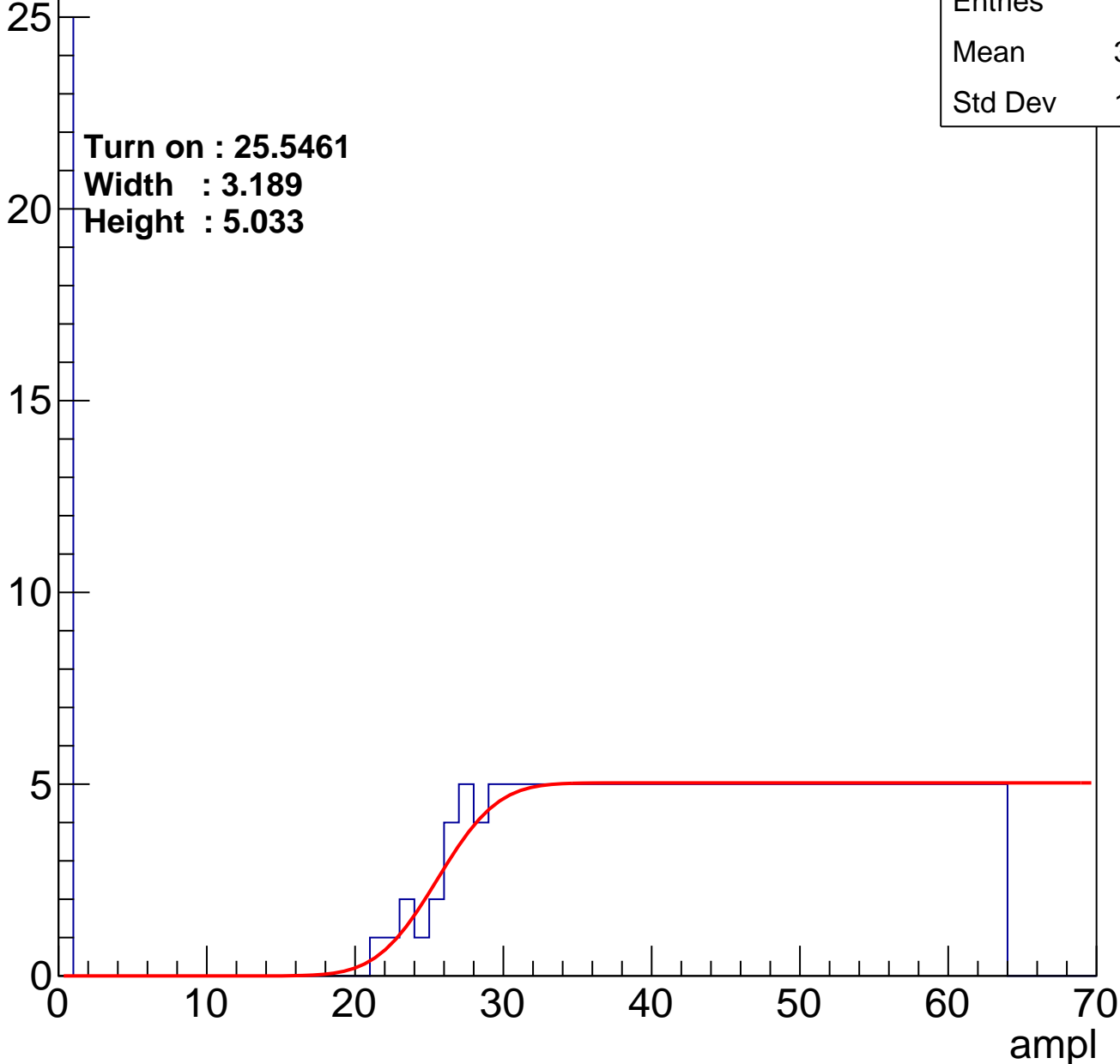
|         |       |
|---------|-------|
| Entries | 220   |
| Mean    | 38.93 |
| Std Dev | 17.59 |

Turn on : 25.5461

Width : 3.189

Height : 5.033

Entry



# B1L103S, U15-ch106

calib\_packv5\_041523\_1651.root, FC#0, Port C2

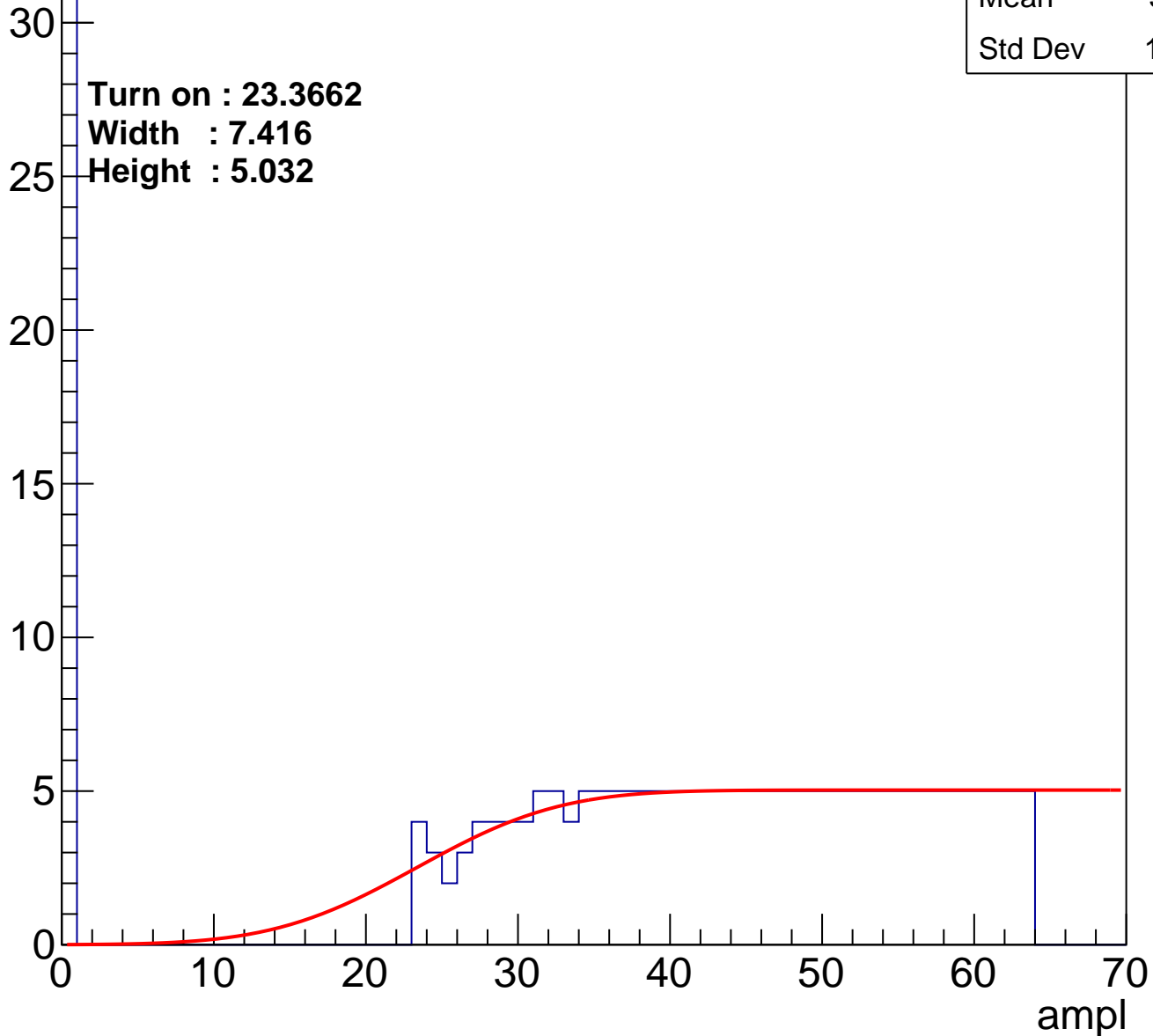
|         |       |
|---------|-------|
| Entries | 224   |
| Mean    | 37.81 |
| Std Dev | 18.69 |

**Turn on : 23.3662**

**Width : 7.416**

**Height : 5.032**

Entry



# B1L103S, U15-ch107

calib\_packv5\_041523\_1651.root, FC#0, Port C2

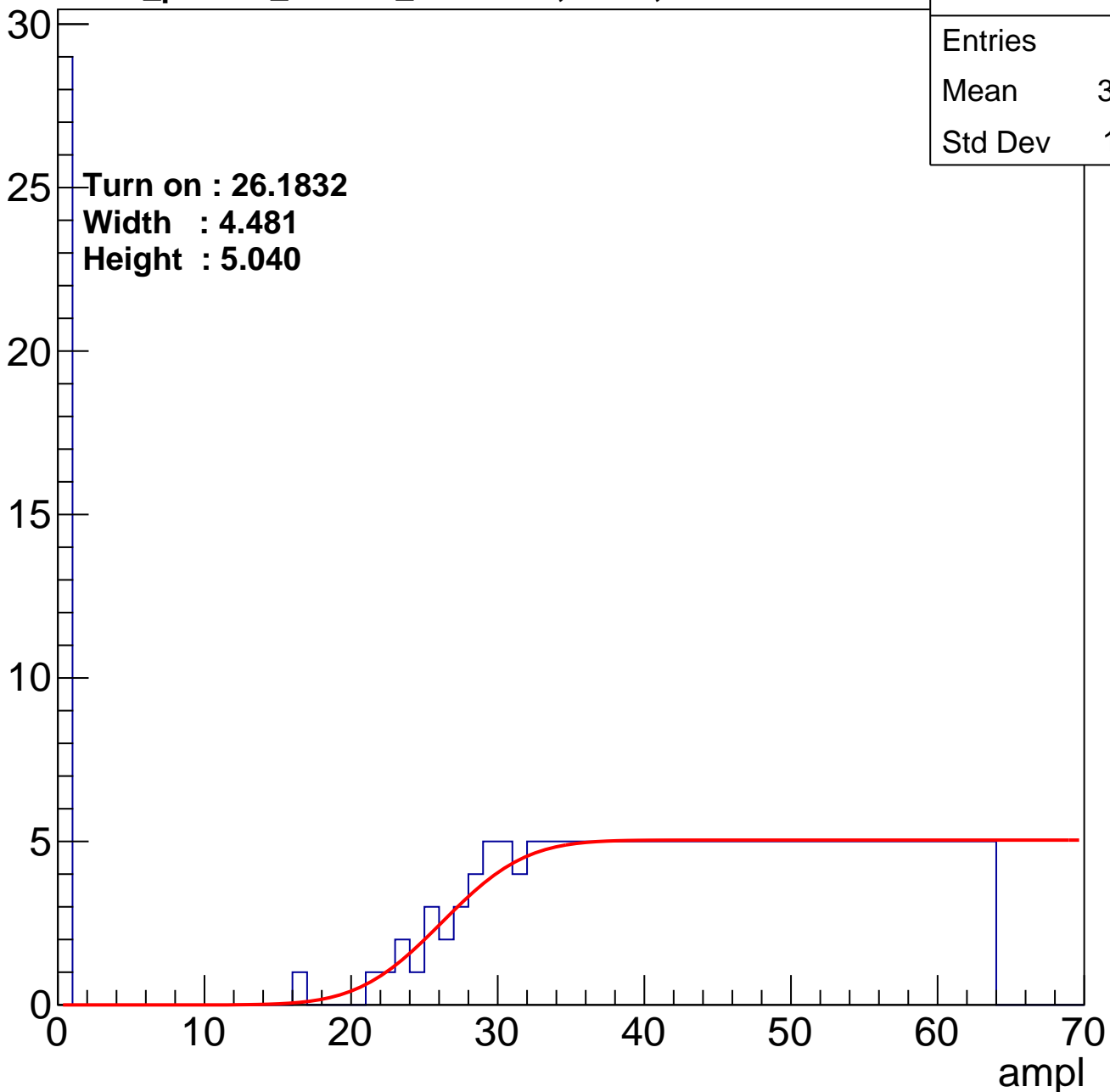
|         |       |
|---------|-------|
| Entries | 221   |
| Mean    | 38.32 |
| Std Dev | 18.31 |

Turn on : 26.1832

Width : 4.481

Height : 5.040

Entry



# B1L103S, U15-ch108

calib\_packv5\_041523\_1651.root, FC#0, Port C2

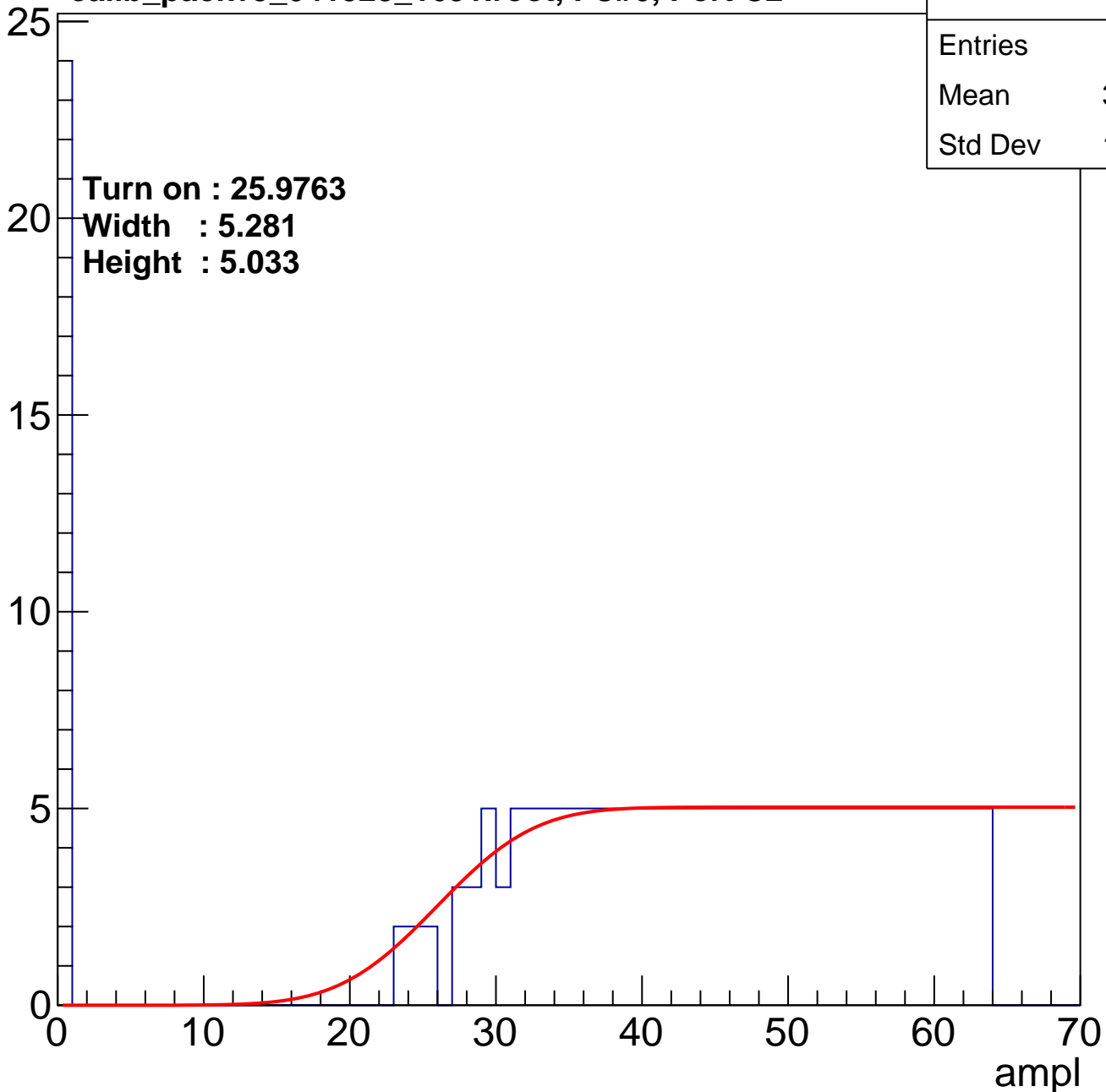
|         |       |
|---------|-------|
| Entries | 209   |
| Mean    | 39.71 |
| Std Dev | 17.61 |

Turn on : 25.9763

Width : 5.281

Height : 5.033

Entry



# B1L103S, U15-ch109

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 220   |
| Mean    | 38.81 |
| Std Dev | 17.76 |

**Turn on : 25.5128**

**Width : 3.263**

**Height : 5.029**

Entry

25

20

15

10

5

0

0

10

20

30

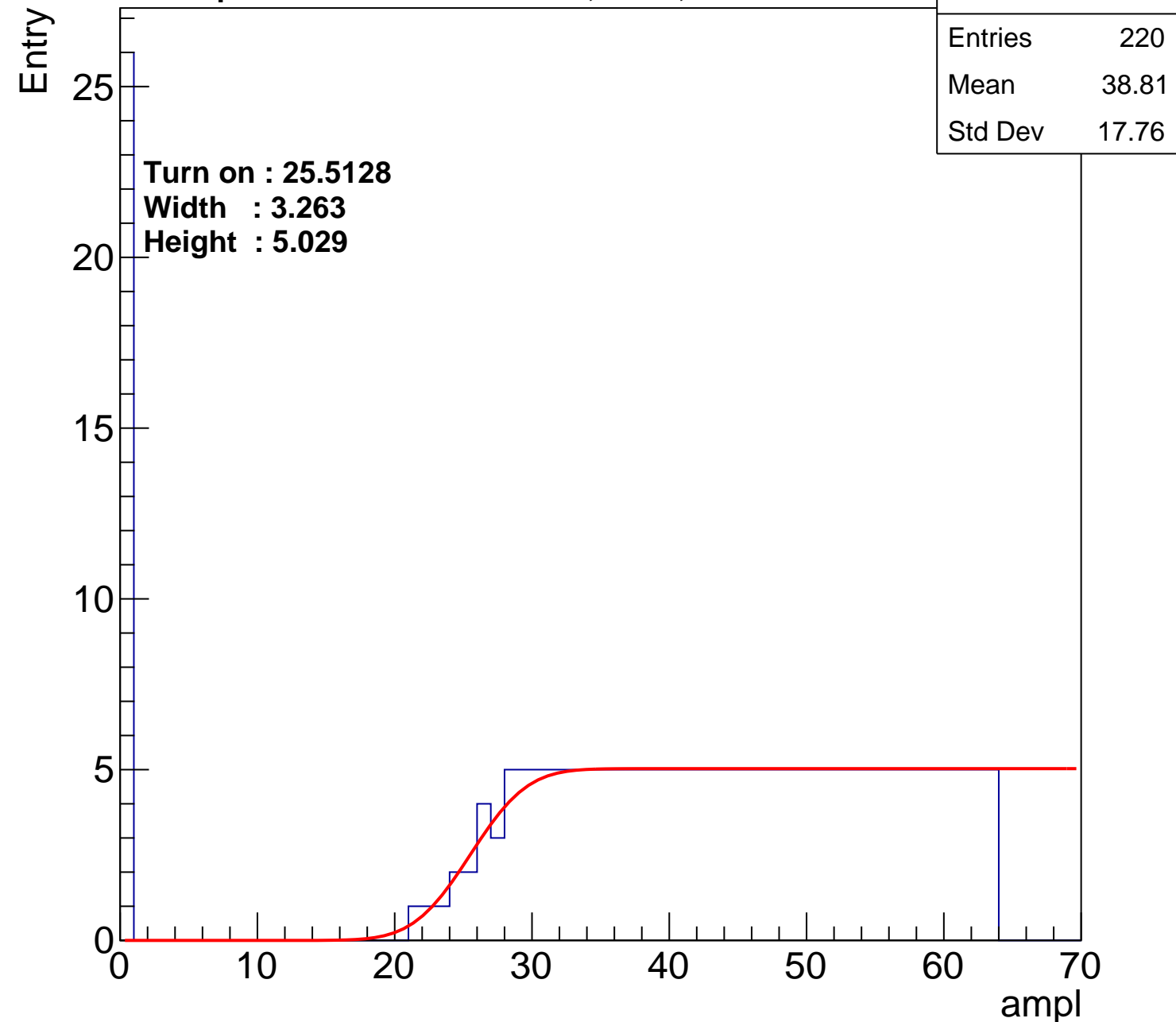
40

50

60

70

ampl



# B1L103S, U15-ch110

calib\_packv5\_041523\_1651.root, FC#0, Port C2

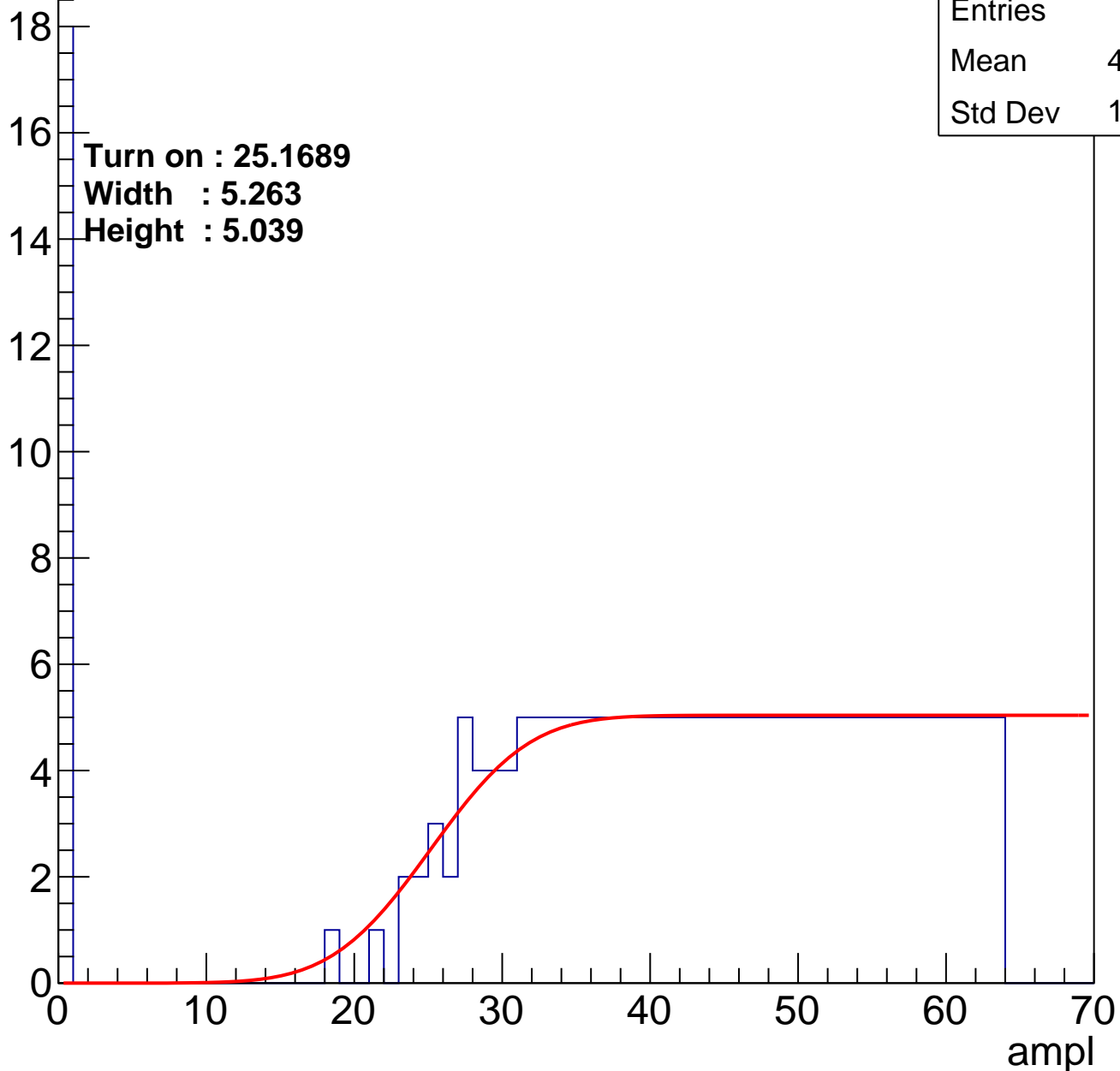
|         |       |
|---------|-------|
| Entries | 211   |
| Mean    | 40.27 |
| Std Dev | 16.46 |

Turn on : 25.1689

Width : 5.263

Height : 5.039

Entry



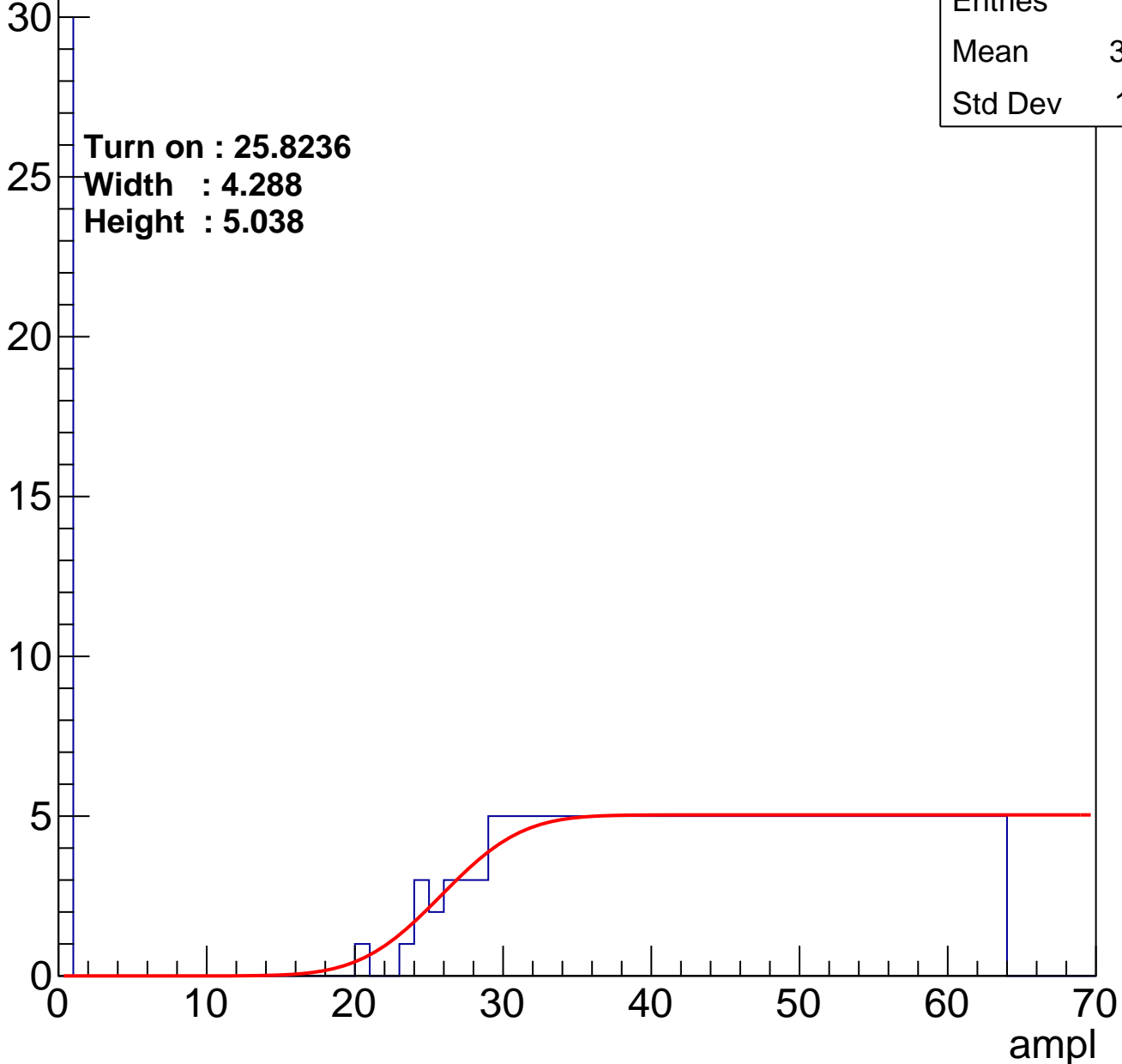
# B1L103S, U15-ch111

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 221   |
| Mean    | 38.27 |
| Std Dev | 18.41 |

**Turn on : 25.8236**  
**Width : 4.288**  
**Height : 5.038**

Entry





# B1L103S, U15-ch112

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 223   |
| Mean    | 38.35 |
| Std Dev | 18.07 |

**Turn on : 24.1279**

**Width : 4.974**

**Height : 5.015**

Entry

25

20

15

10

5

0

0

10

20

30

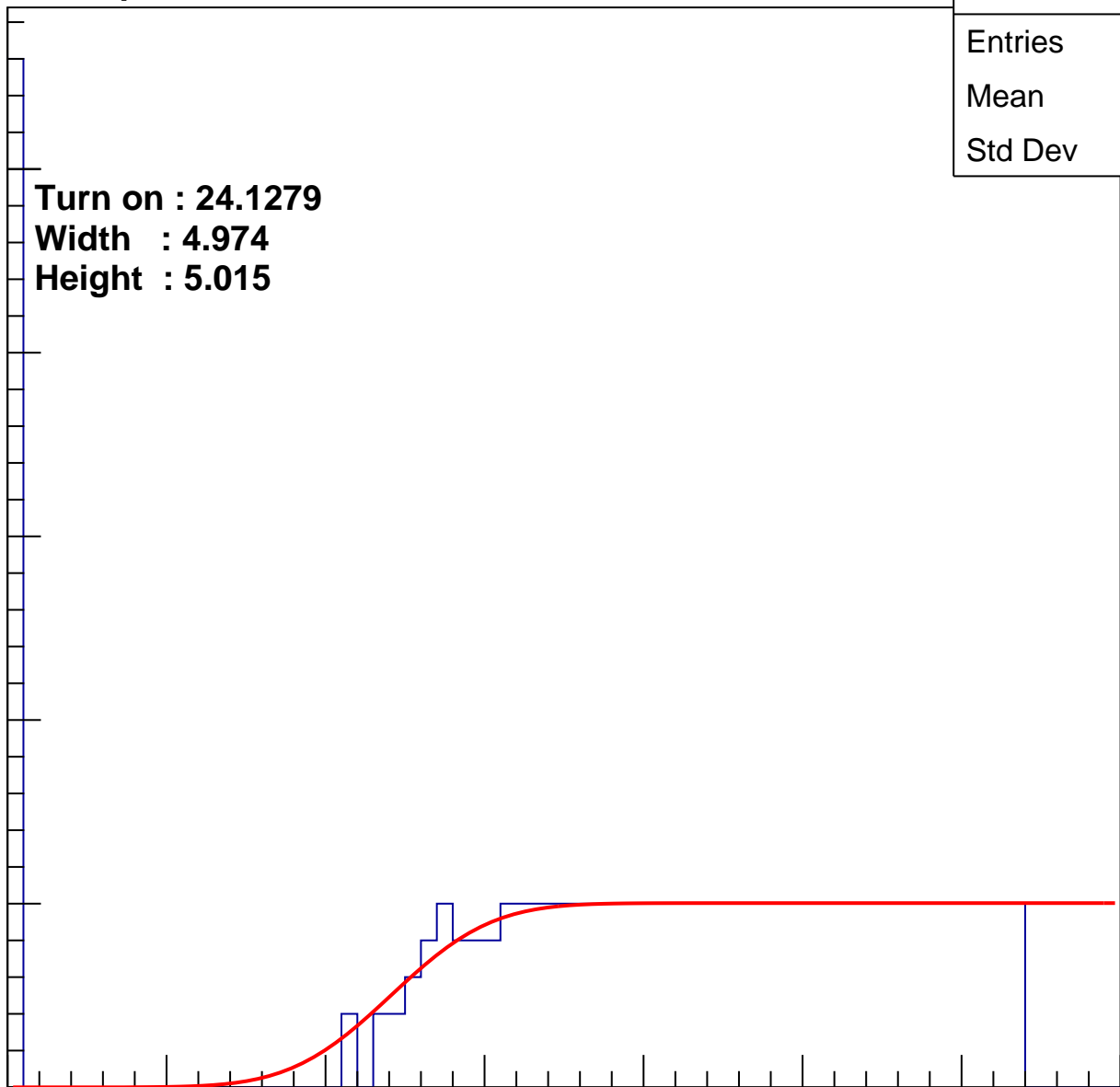
40

50

60

70

ampl



# B1L103S, U15-ch113

calib\_packv5\_041523\_1651.root, FC#0, Port C2

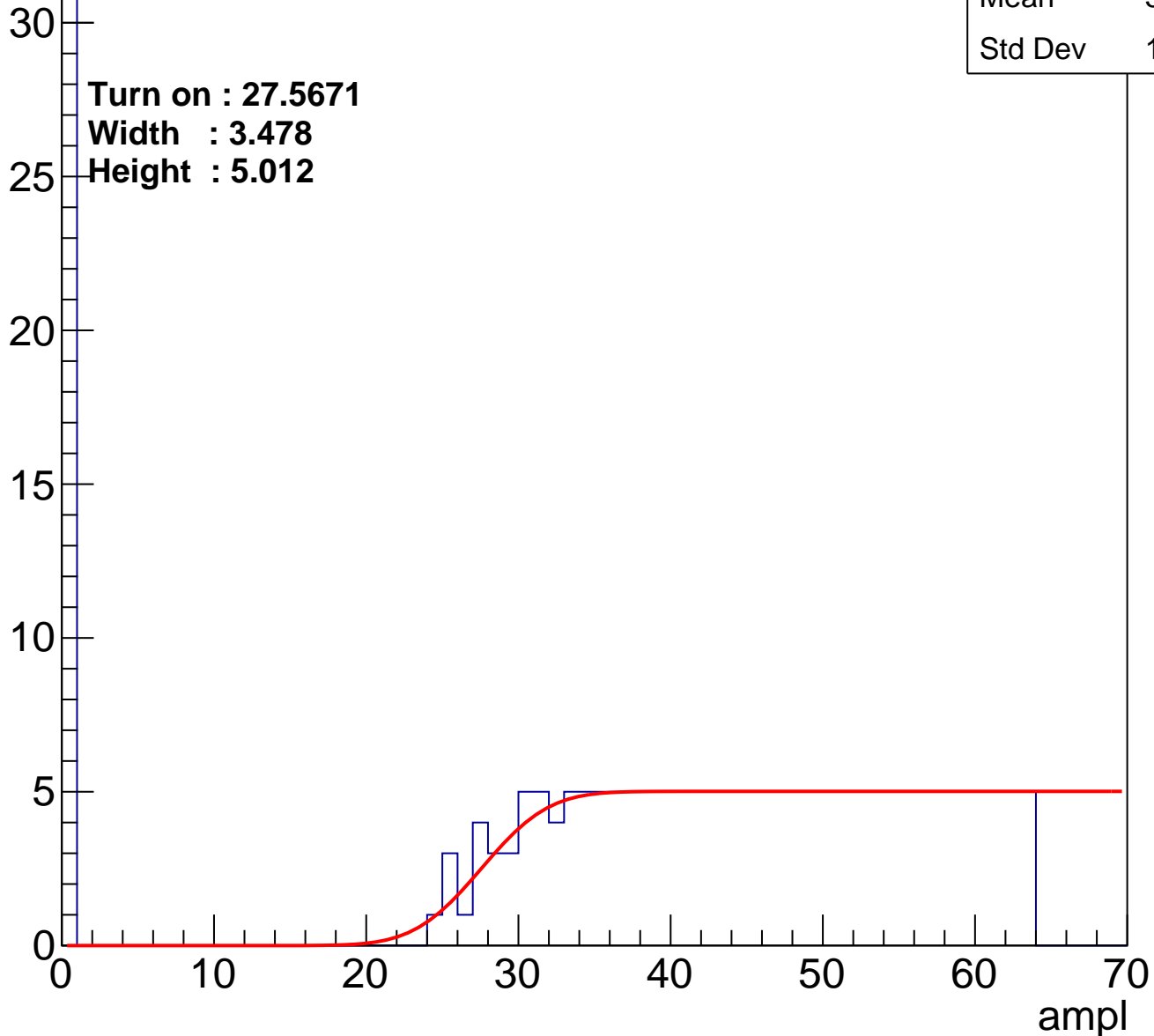
|         |       |
|---------|-------|
| Entries | 216   |
| Mean    | 38.32 |
| Std Dev | 18.84 |

**Turn on : 27.5671**

**Width : 3.478**

**Height : 5.012**

Entry



# B1L103S, U15-ch114

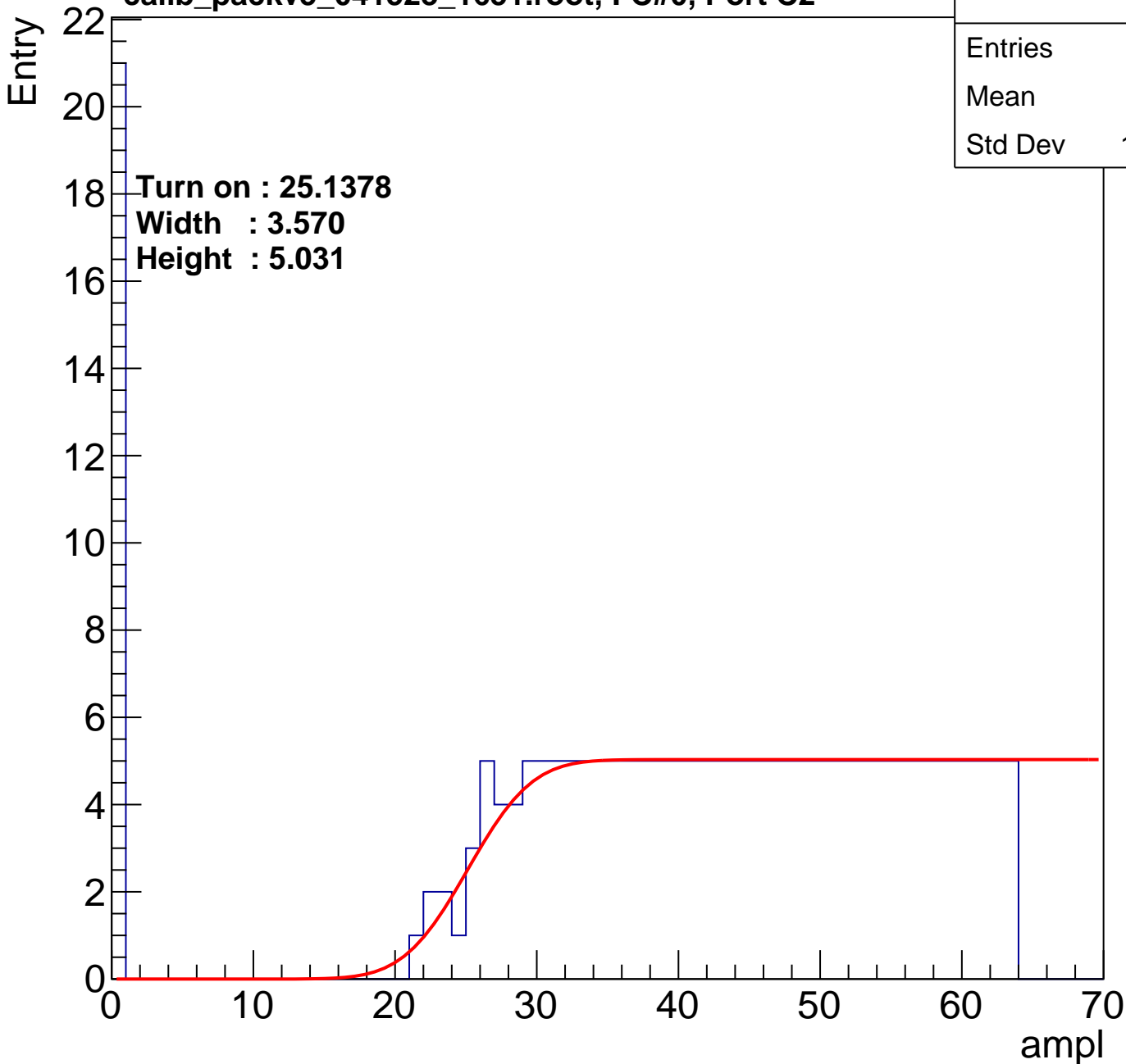
calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 218   |
| Mean    | 39.5  |
| Std Dev | 16.92 |

Turn on : 25.1378

Width : 3.570

Height : 5.031



# B1L103S, U15-ch115

calib\_packv5\_041523\_1651.root, FC#0, Port C2

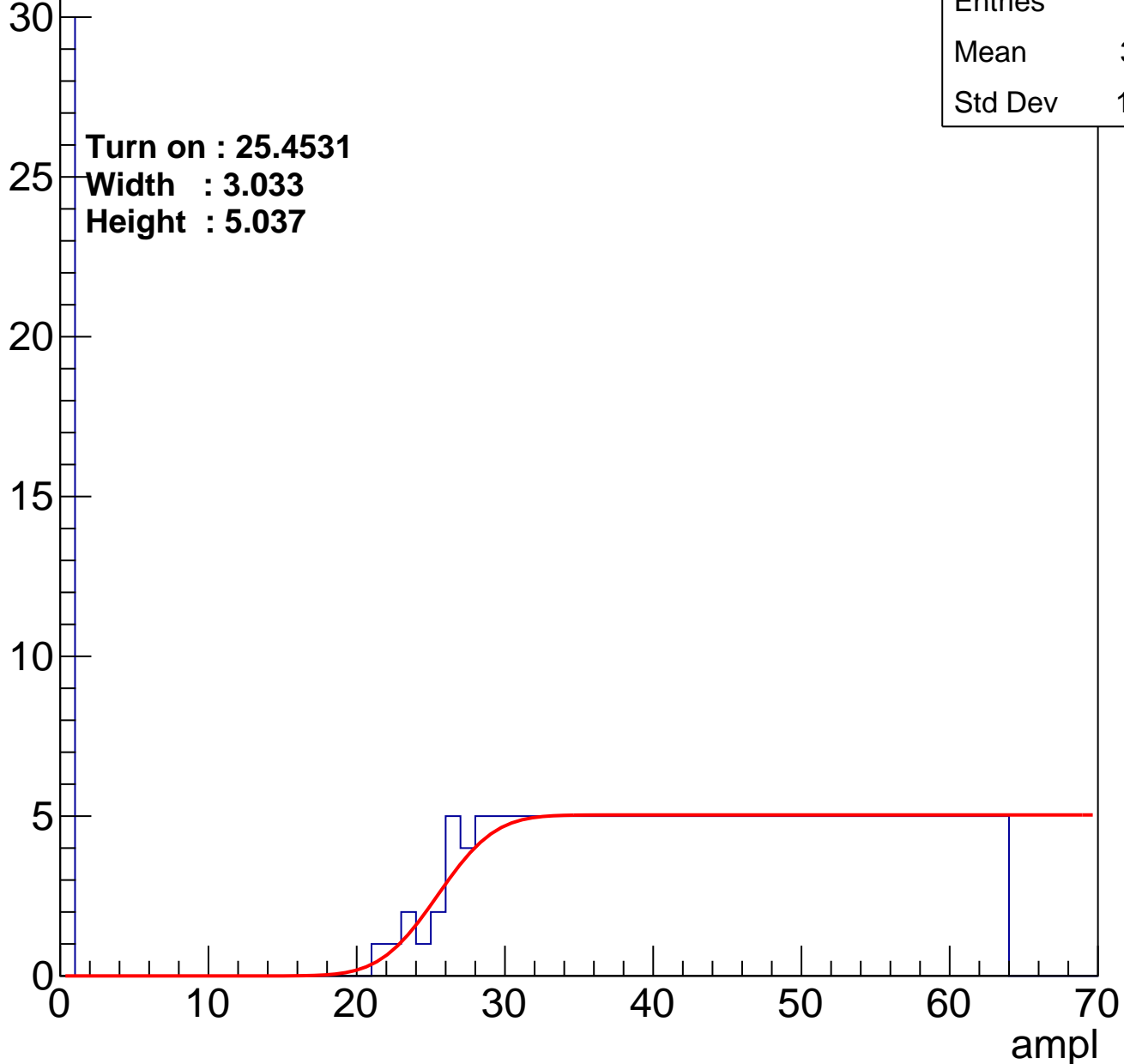
|         |       |
|---------|-------|
| Entries | 226   |
| Mean    | 38.01 |
| Std Dev | 18.29 |

Turn on : 25.4531

Width : 3.033

Height : 5.037

Entry



# B1L103S, U15-ch116

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 225   |
| Mean    | 38.47 |
| Std Dev | 17.71 |

**Turn on : 24.5202**

**Width : 3.592**

**Height : 5.020**

Entry

25

20

15

10

5

0

ampl

0

10

20

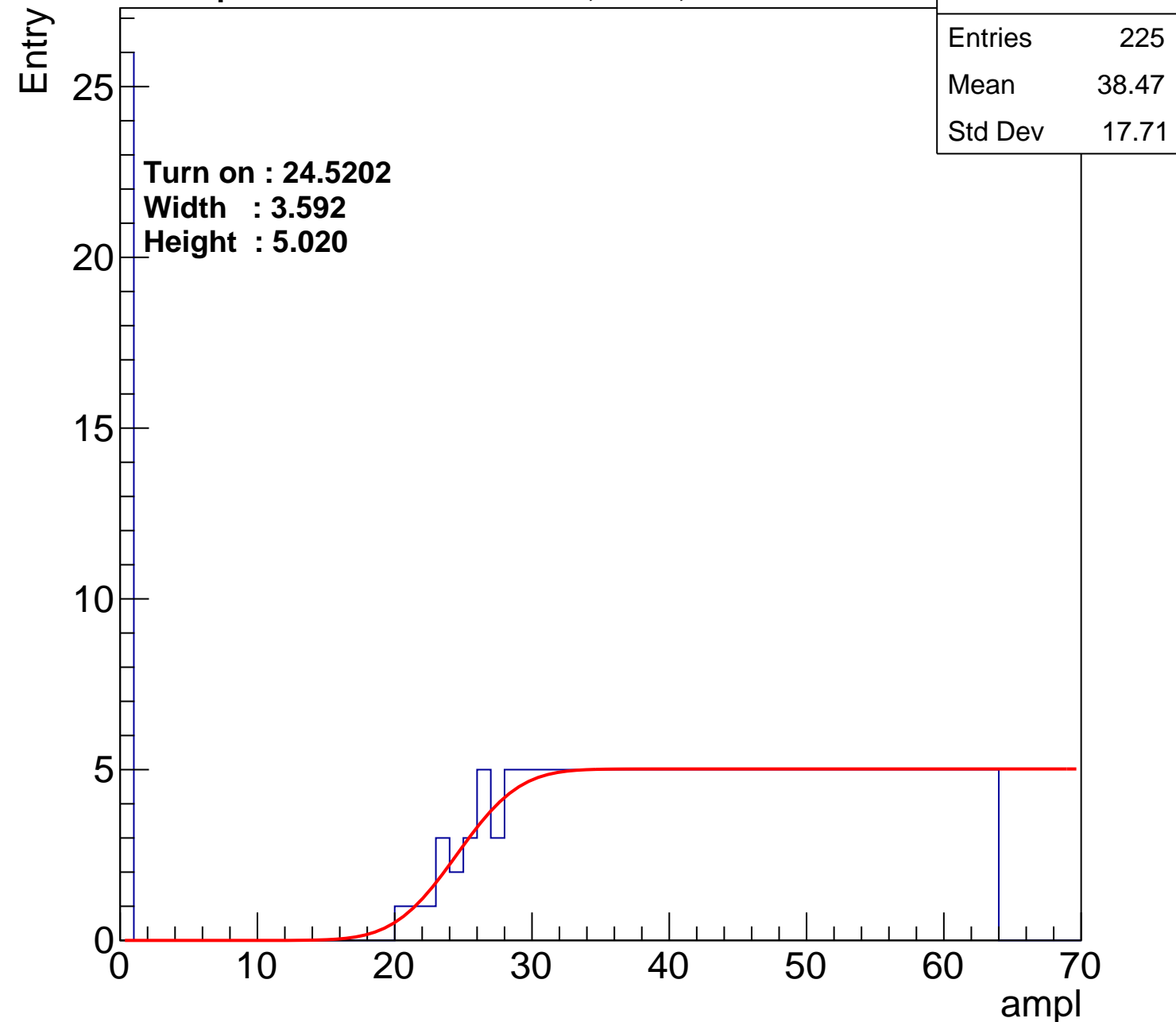
30

40

50

60

70



# B1L103S, U15-ch117

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 214   |
| Mean    | 38.56 |
| Std Dev | 18.73 |

**Turn on : 27.0462**

**Width : 4.113**

**Height : 5.022**

Entry

30

25

20

15

10

5

0

ampl

0

10

20

30

40

50

60

70

# B1L103S, U15-ch118

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 225   |
| Mean    | 38.59 |
| Std Dev | 17.55 |

Turn on : 24.1445

Width : 3.499

Height : 5.031

Entry

25

20

15

10

5

0

0

10

20

30

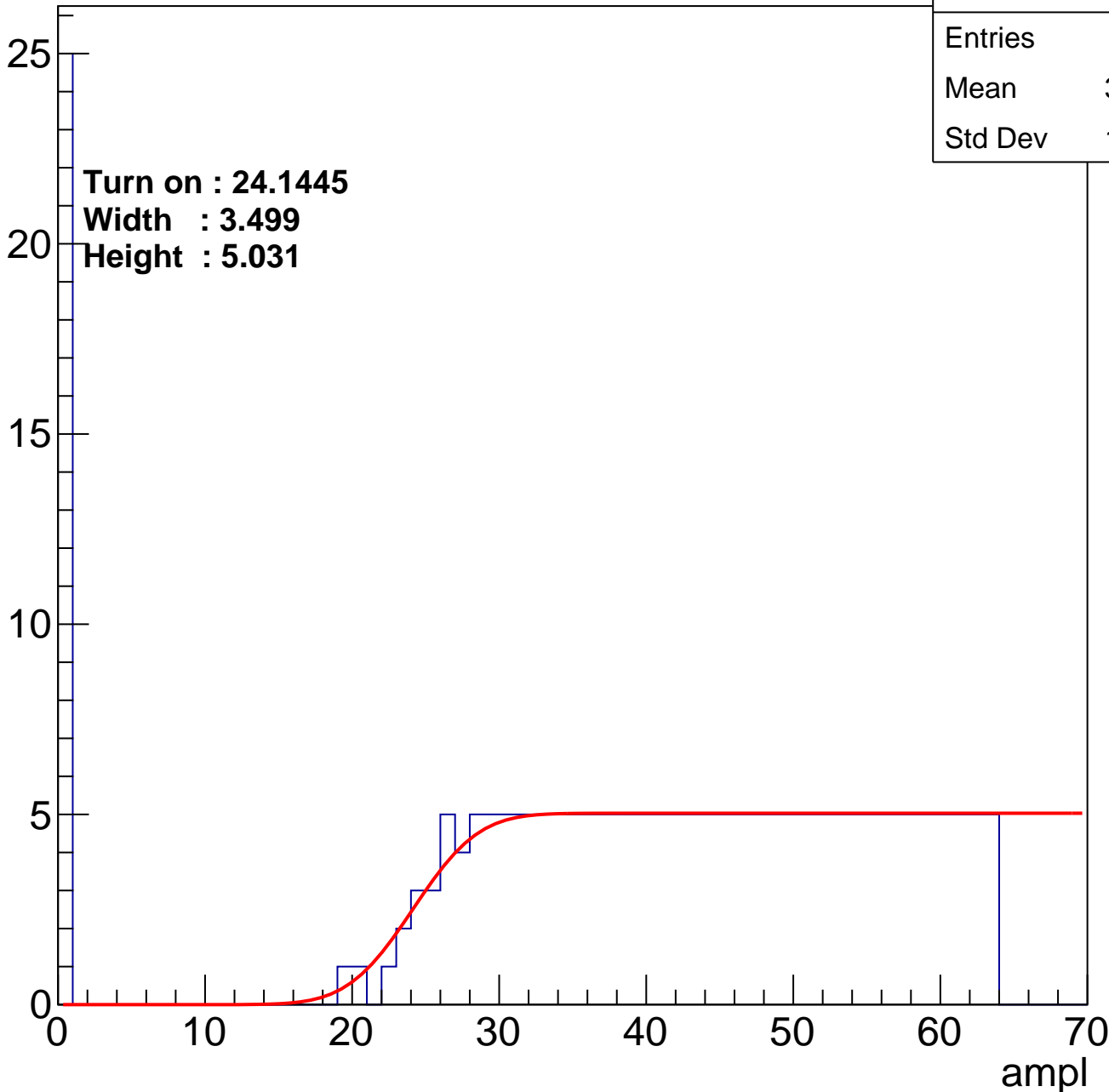
40

50

60

70

ampl

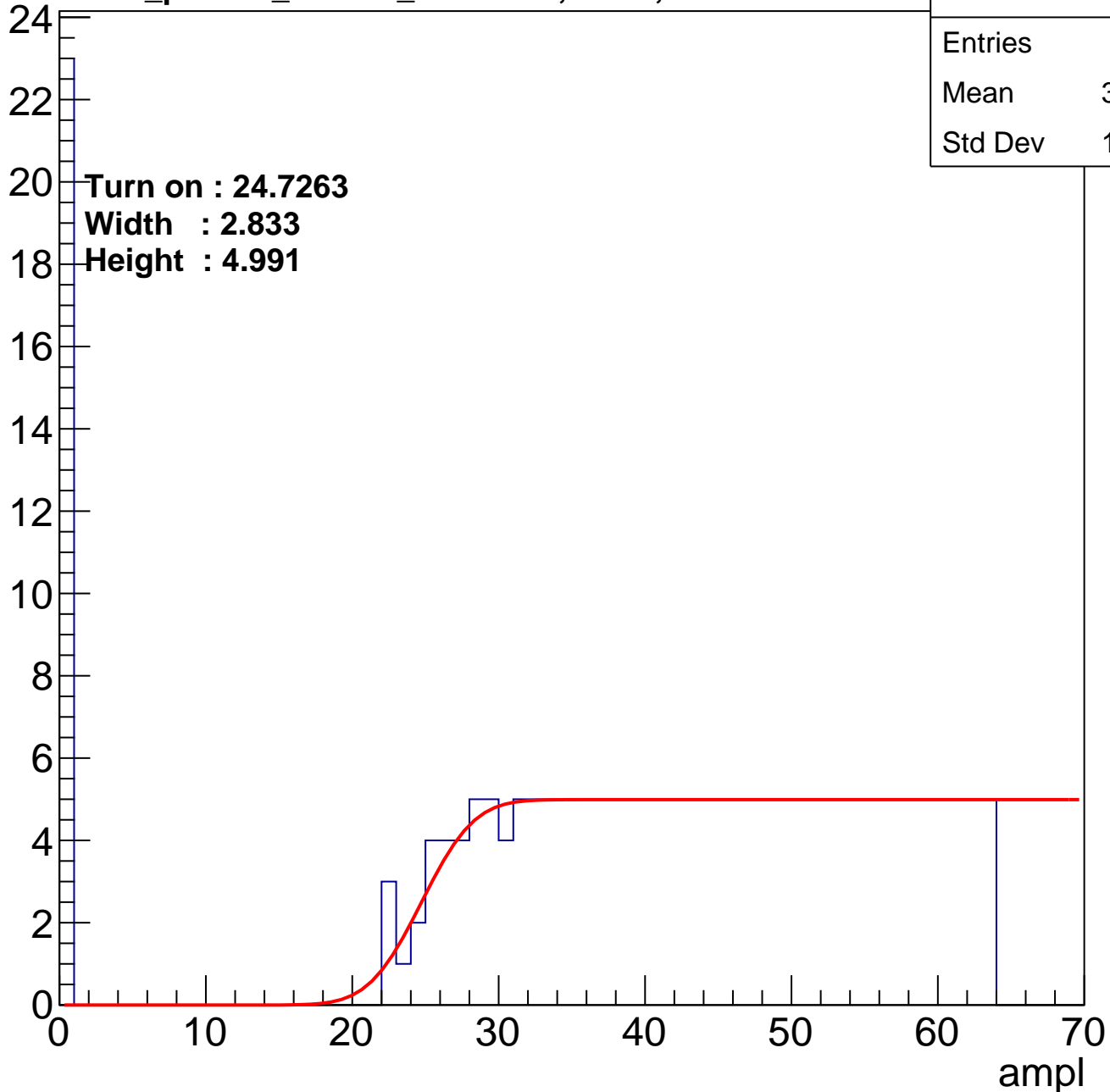


# B1L103S, U15-ch119

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 220   |
| Mean    | 39.13 |
| Std Dev | 17.26 |

Entry





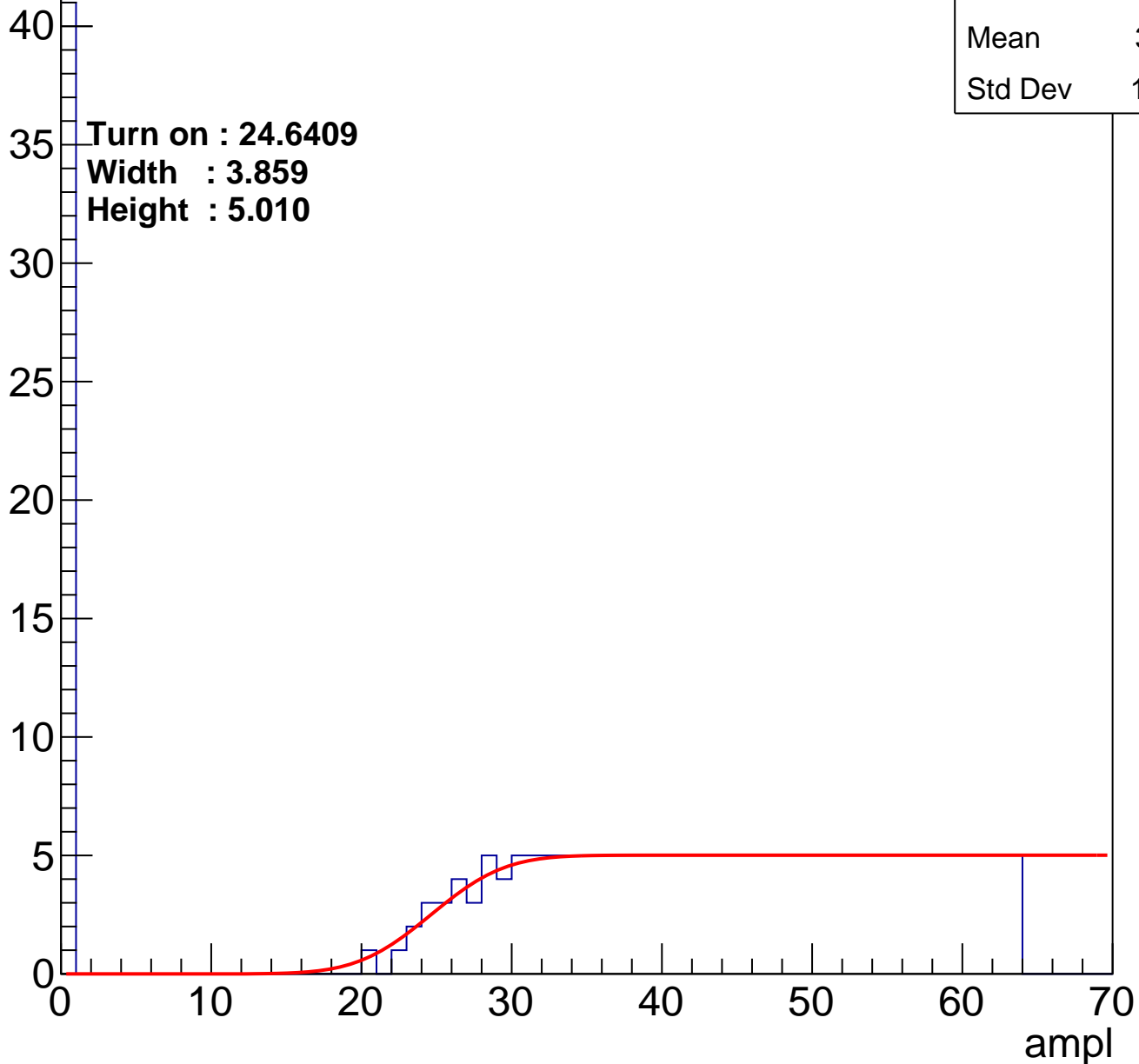
# B1L103S, U15-ch120

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 237   |
| Mean    | 36.21 |
| Std Dev | 19.59 |

Turn on : 24.6409  
Width : 3.859  
Height : 5.010

Entry



# B1L103S, U15-ch121

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 228   |
| Mean    | 37.47 |
| Std Dev | 18.76 |

**Turn on : 25.1032**

**Width : 4.158**

**Height : 4.994**

Entry

30

25

20

15

10

5

0

0

10

20

30

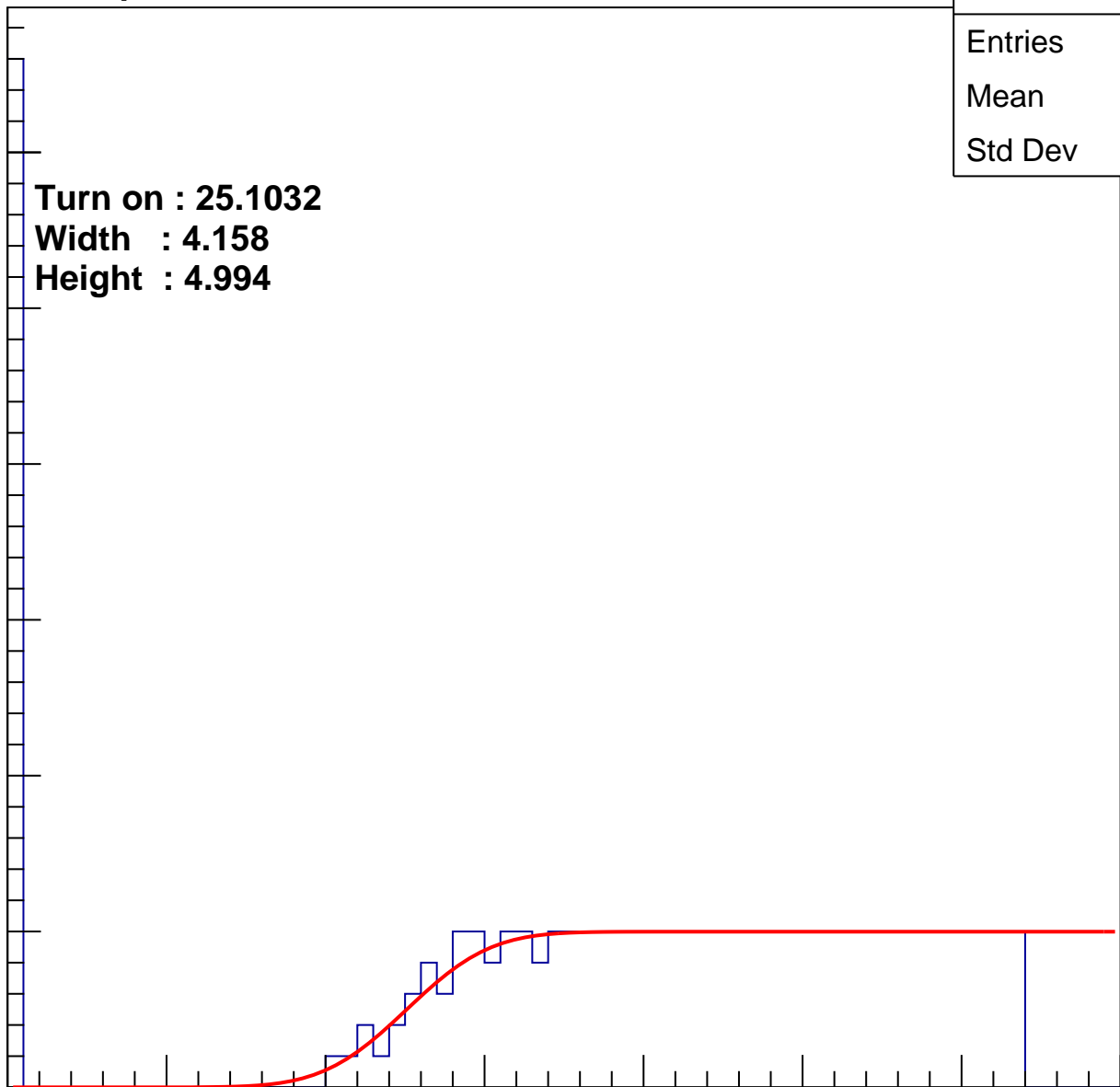
40

50

60

70

ampl



# B1L103S, U15-ch122

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 221   |
| Mean    | 38.14 |
| Std Dev | 18.58 |

**Turn on : 25.6477**

**Width : 4.515**

**Height : 5.030**

Entry

30

25

20

15

10

5

0

ampl

0

10

20

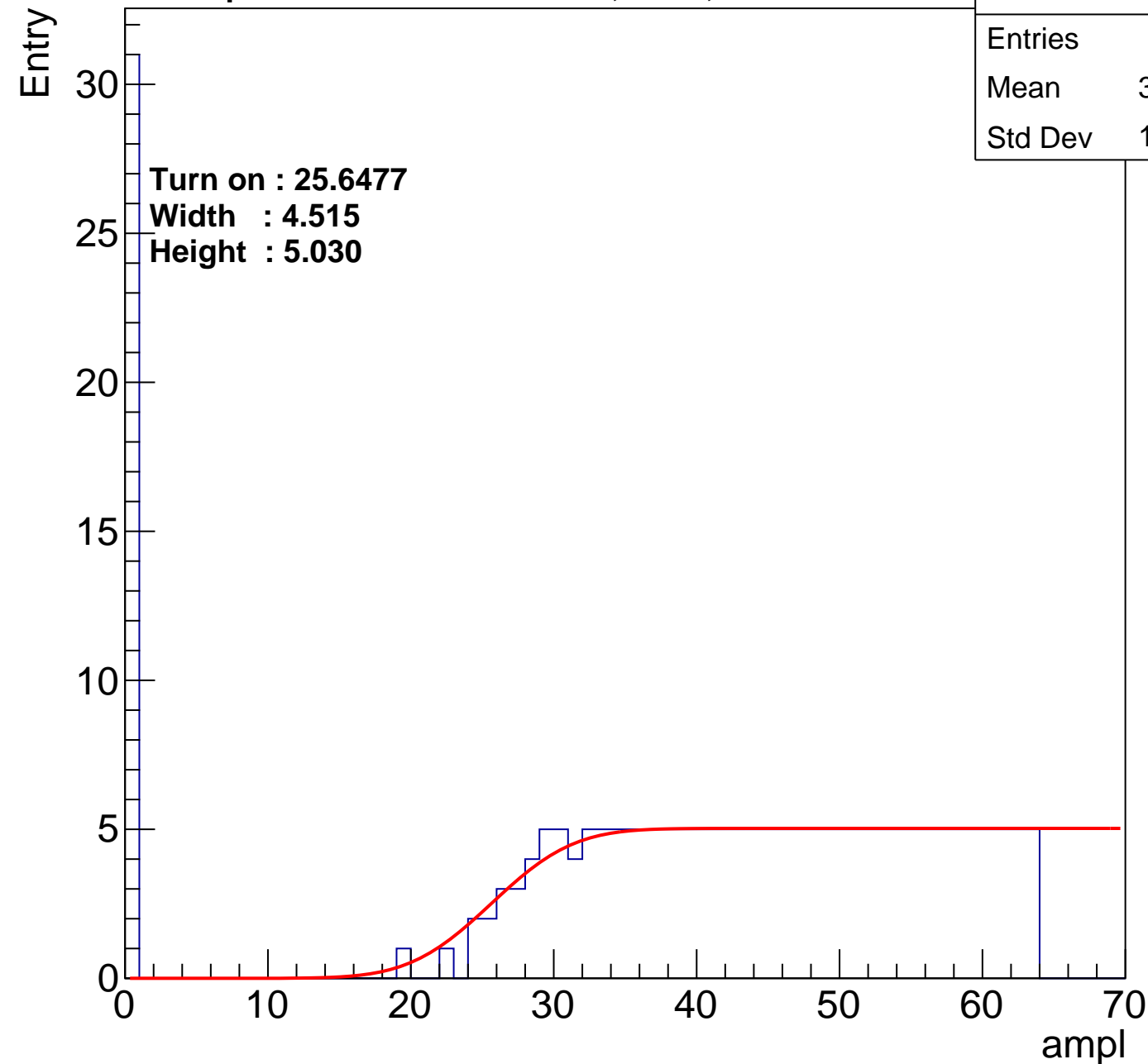
30

40

50

60

70



# B1L103S, U15-ch123

calib\_packv5\_041523\_1651.root, FC#0, Port C2

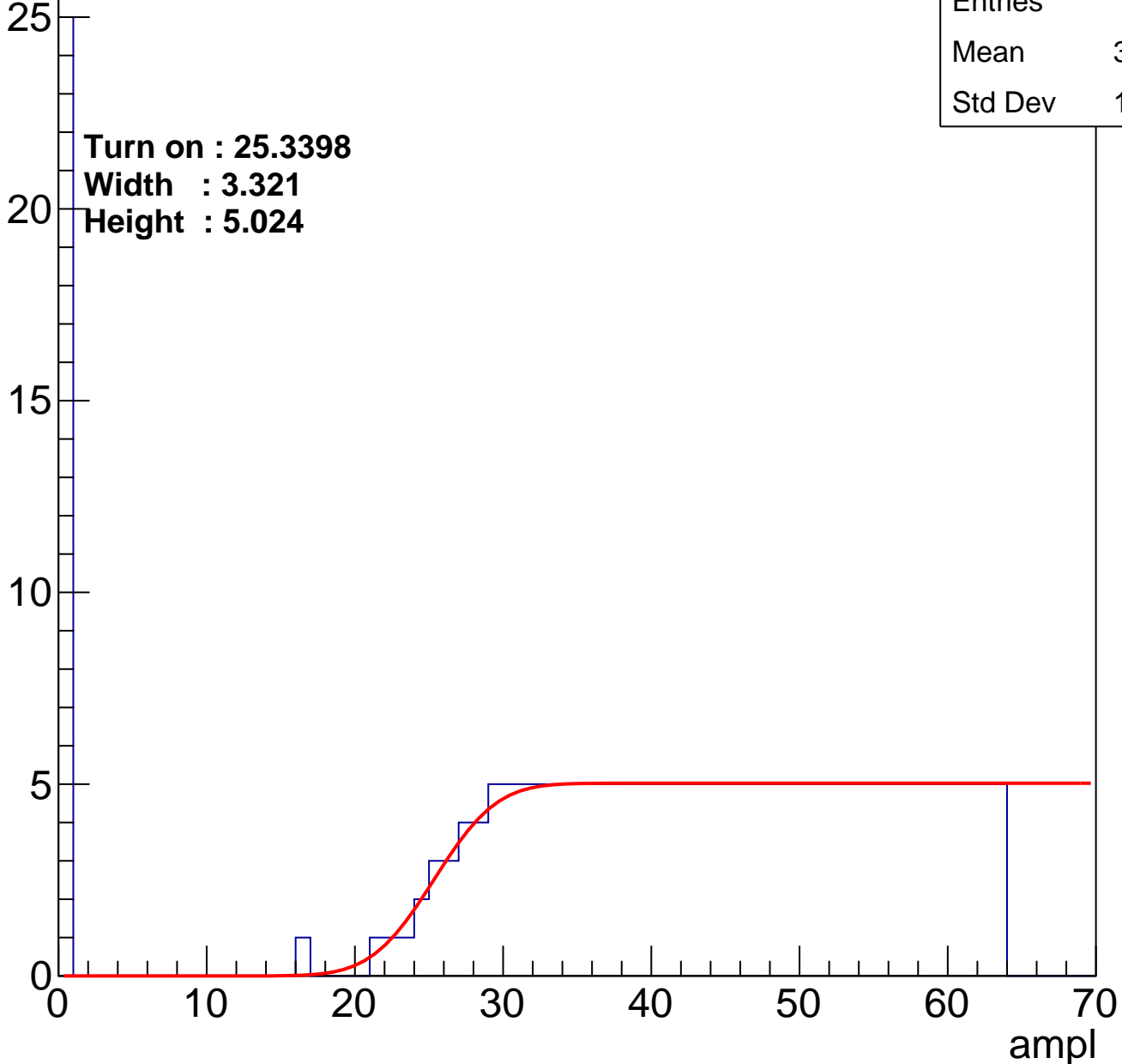
|         |       |
|---------|-------|
| Entries | 220   |
| Mean    | 38.88 |
| Std Dev | 17.64 |

Turn on : 25.3398

Width : 3.321

Height : 5.024

Entry



# B1L103S, U15-ch124

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 220   |
| Mean    | 38.73 |
| Std Dev | 17.83 |

**Turn on : 25.9864**

**Width : 4.880**

**Height : 5.064**

Entry

25

20

15

10

5

0

0

10

20

30

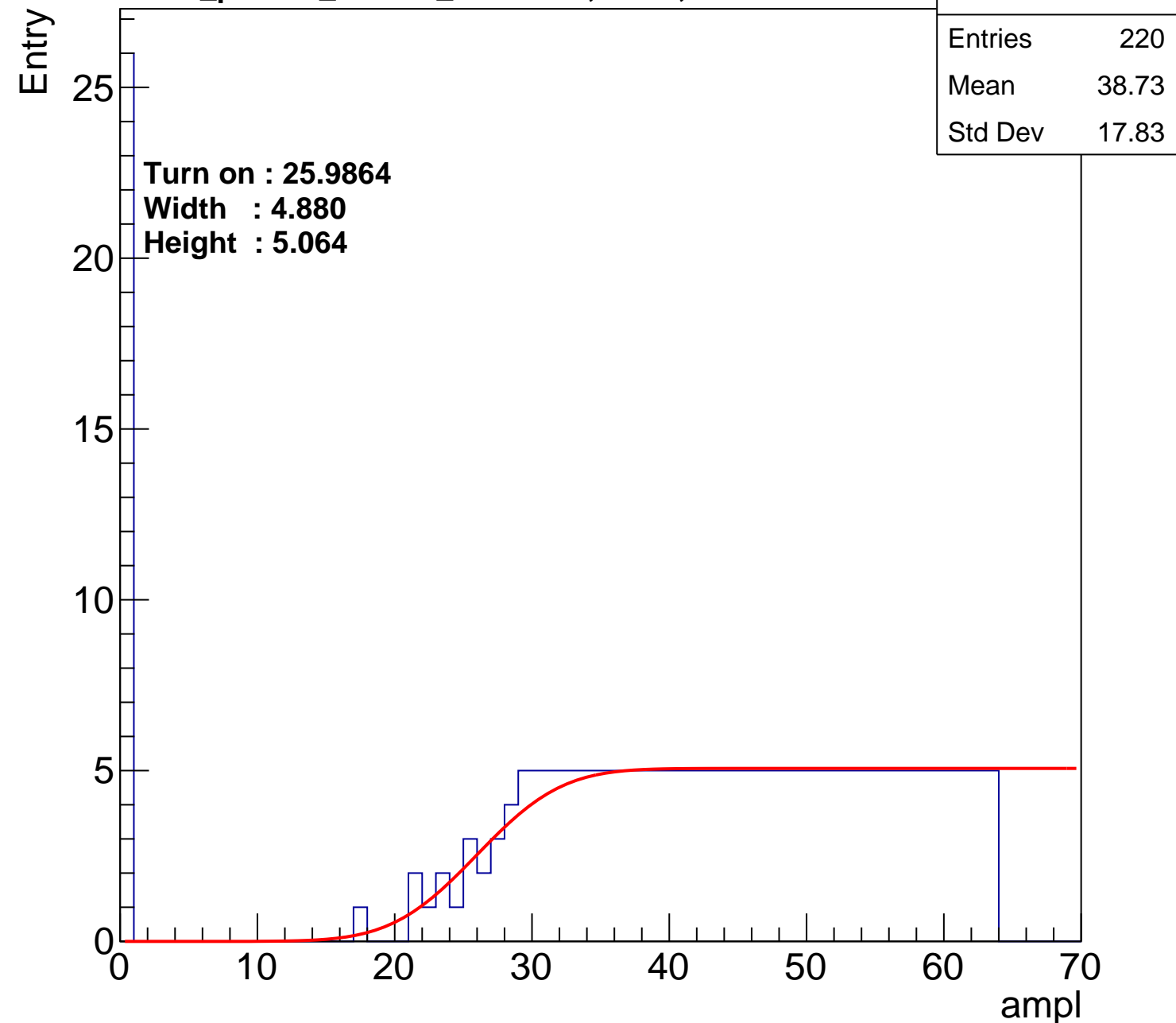
40

50

60

70

ampl



# B1L103S, U15-ch125

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 209   |
| Mean    | 39.45 |
| Std Dev | 17.98 |

**Turn on : 27.7456**

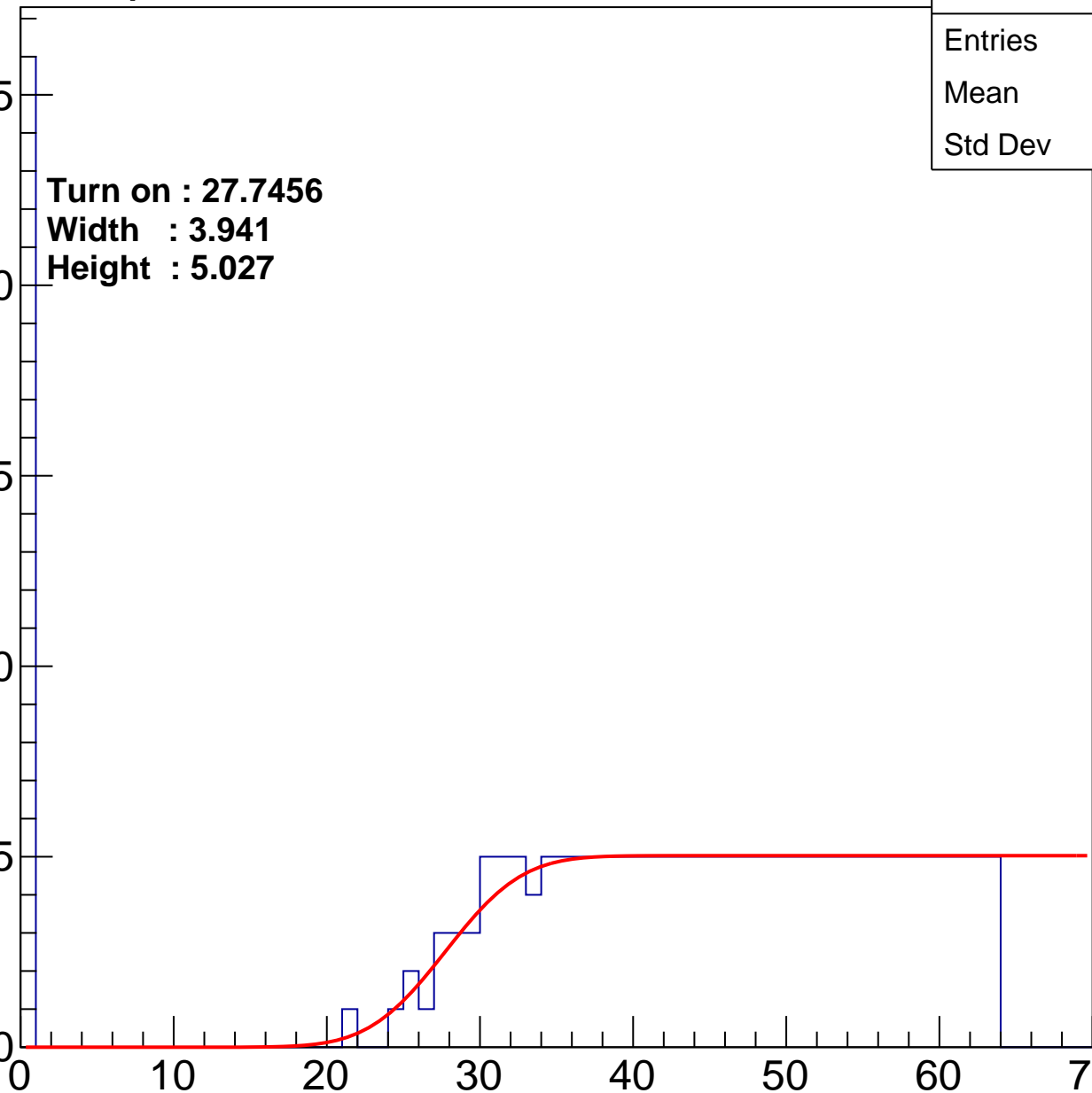
**Width : 3.941**

**Height : 5.027**

Entry

25  
20  
15  
10  
5  
0

ampl

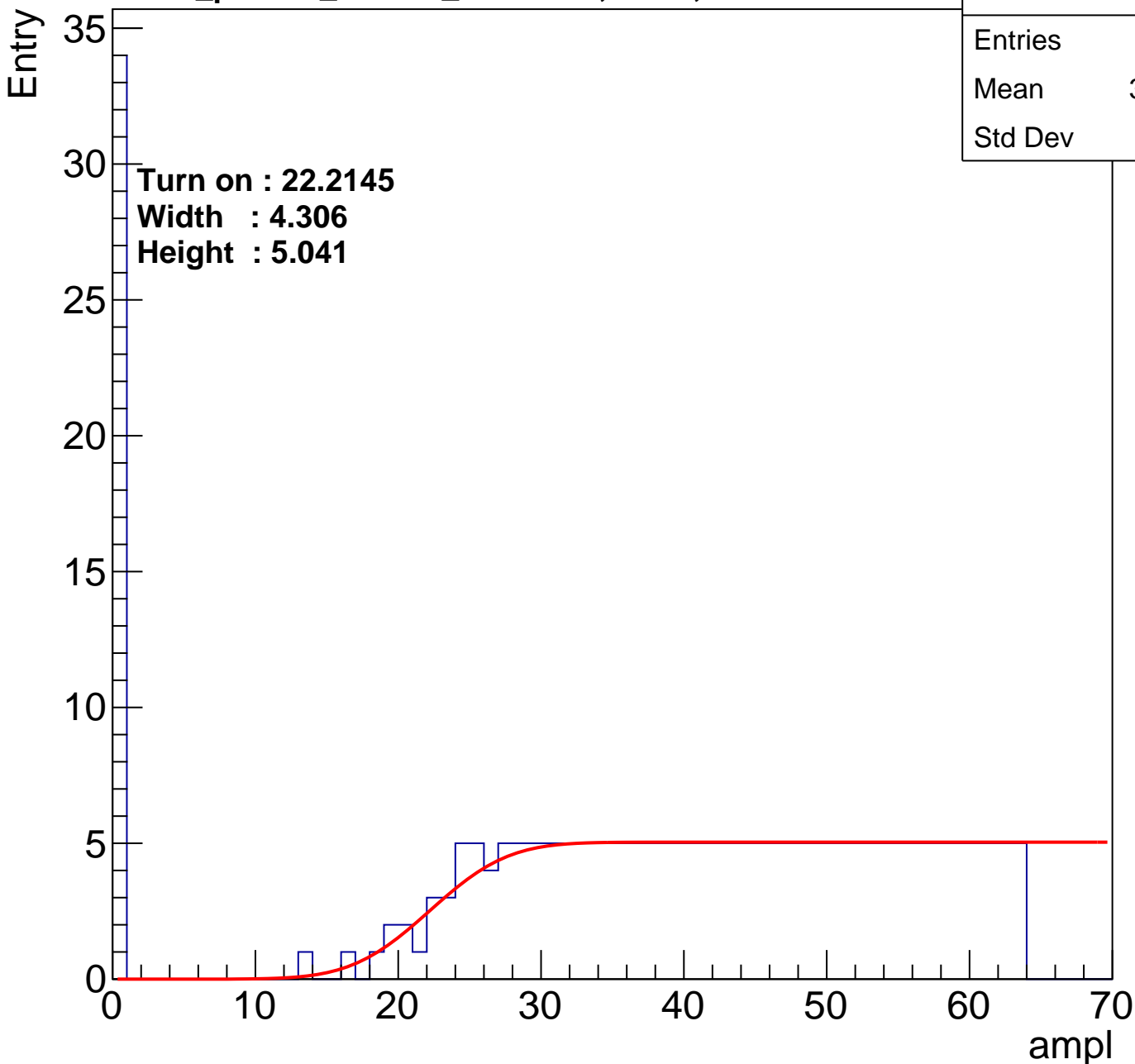


# B1L103S, U15-ch126

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 247   |
| Mean    | 36.26 |
| Std Dev | 18.61 |

Turn on : 22.2145  
Width : 4.306  
Height : 5.041



# B1L103S, U15-ch127

calib\_packv5\_041523\_1651.root, FC#0, Port C2

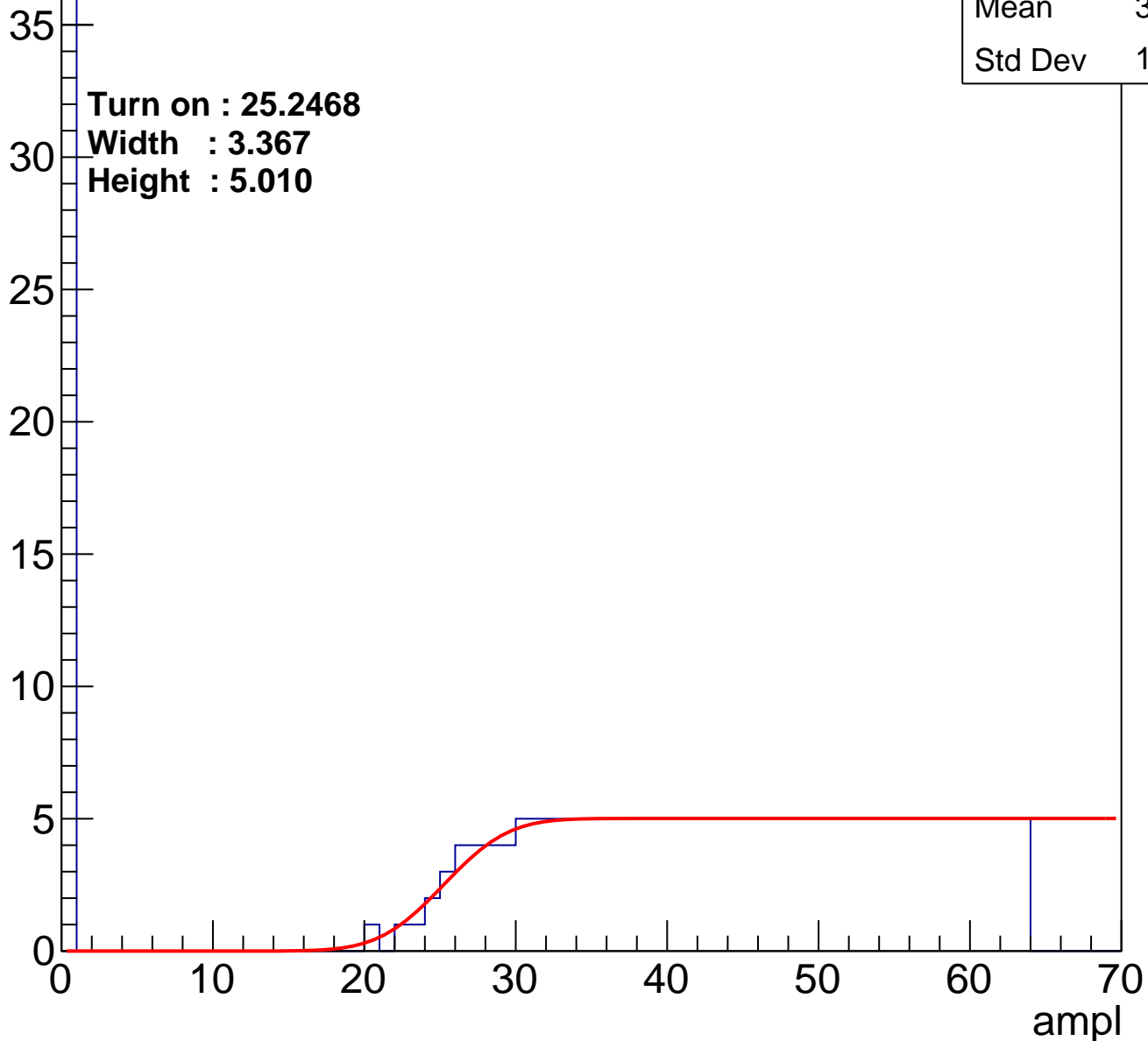
|         |       |
|---------|-------|
| Entries | 231   |
| Mean    | 36.94 |
| Std Dev | 19.22 |

**Turn on : 25.2468**

**Width : 3.367**

**Height : 5.010**

Entry





# B1L103S, U17-ch82

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 545   |
| Mean    | 32.03 |
| Std Dev | 21.3  |

Turn on : 24.7181

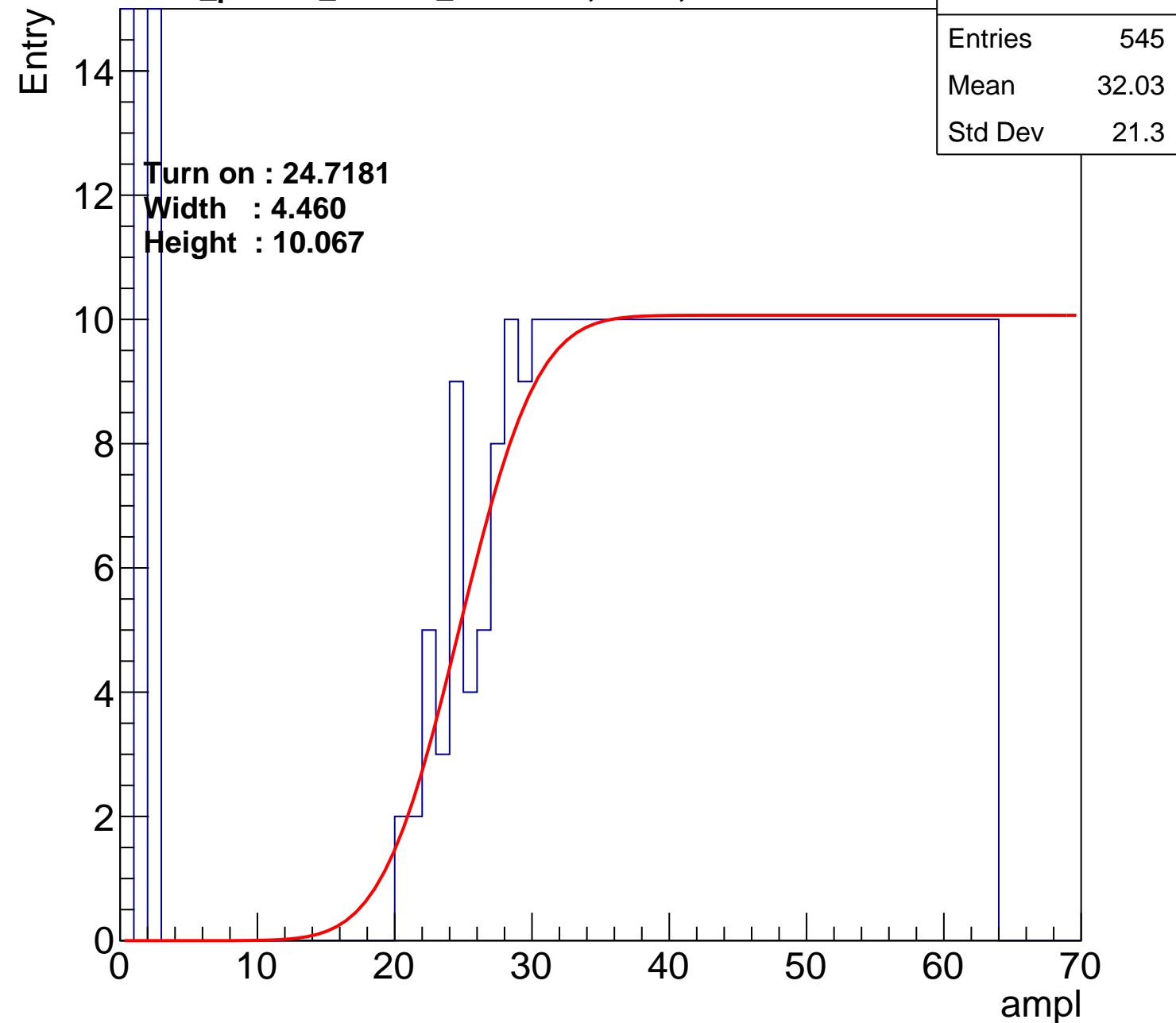
Width : 4.460

Height : 10.067

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U18-ch82

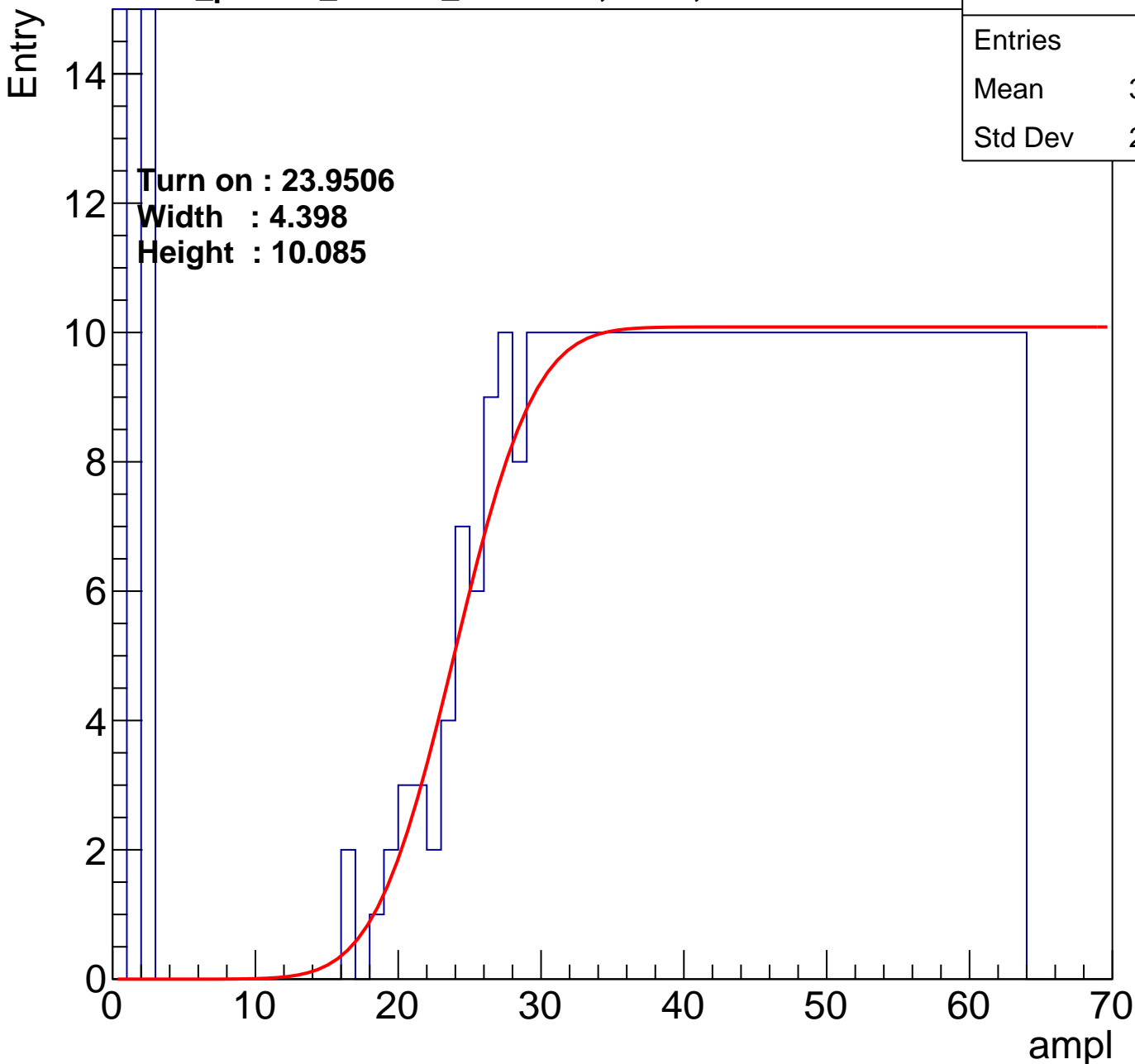
calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 570   |
| Mean    | 31.03 |
| Std Dev | 21.46 |

Turn on : 23.9506

Width : 4.398

Height : 10.085



# B1L103S, U23-ch82

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 543   |
| Mean    | 33.35 |
| Std Dev | 20.12 |

Turn on : 21.4562

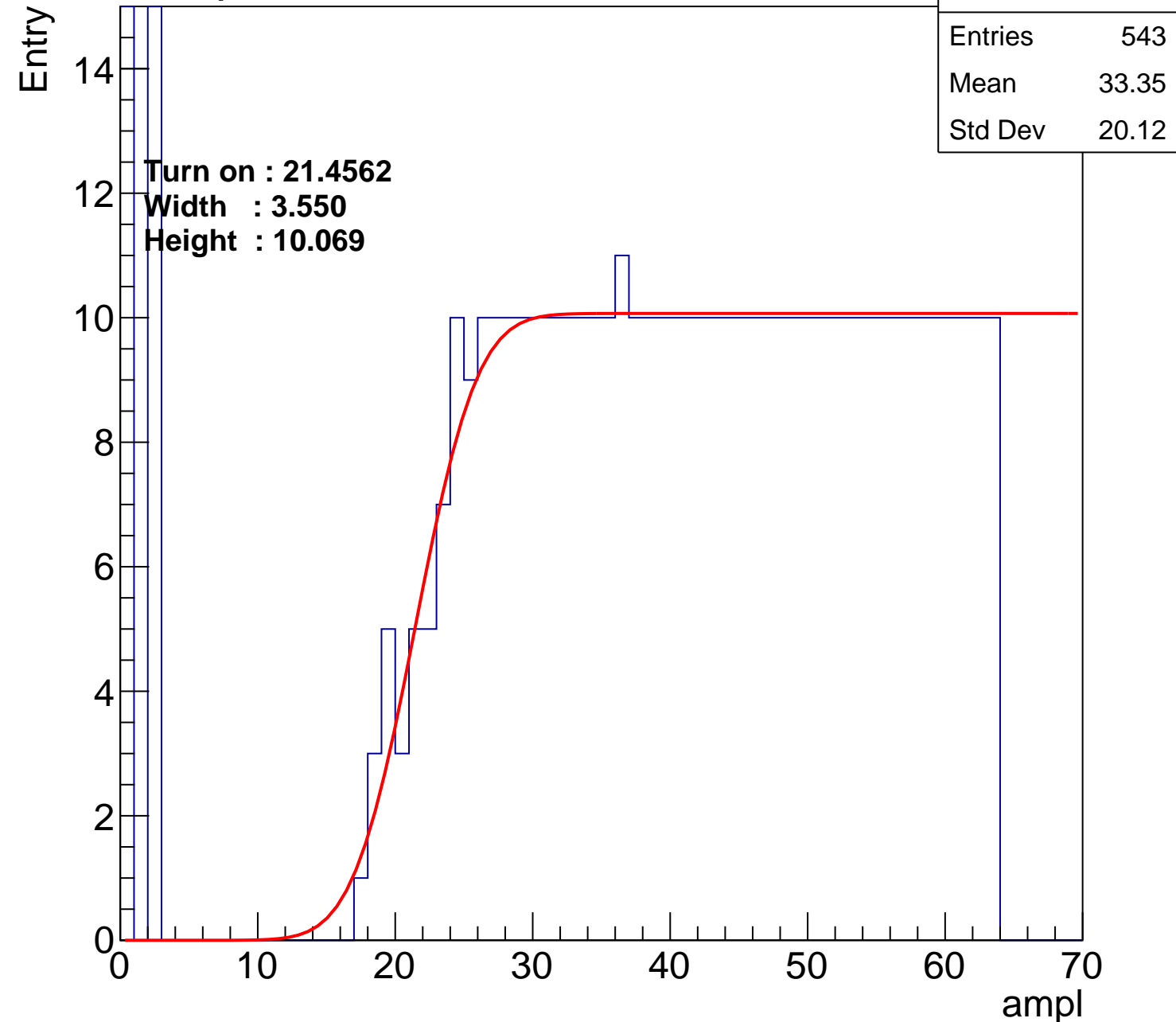
Width : 3.550

Height : 10.069

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U25-ch82

calib\_packv5\_041523\_1651.root, FC#0, Port C2

|         |       |
|---------|-------|
| Entries | 524   |
| Mean    | 33.73 |
| Std Dev | 20.34 |

Turn on : 23.4408

Width : 3.123

Height : 10.023

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl

