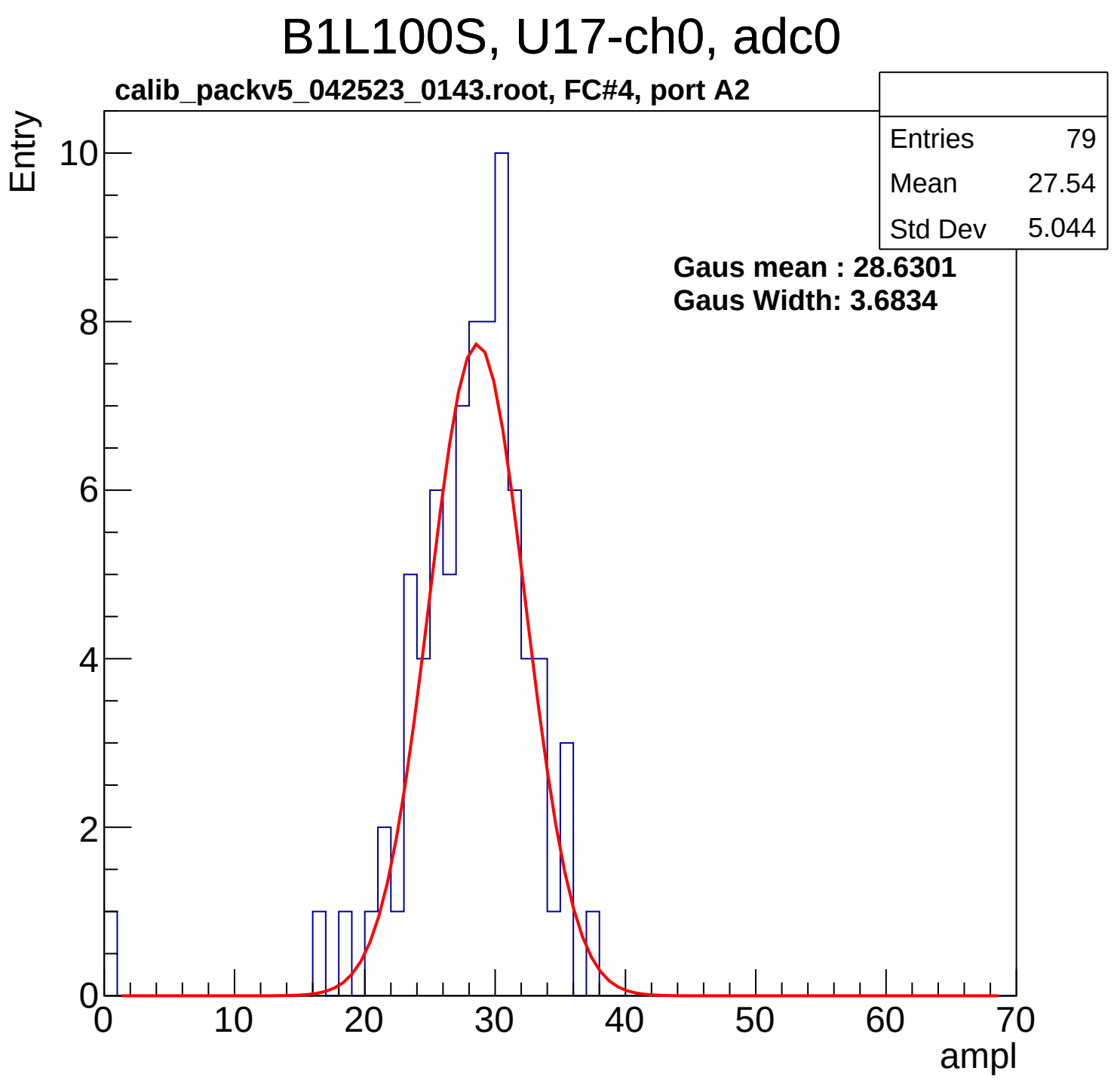
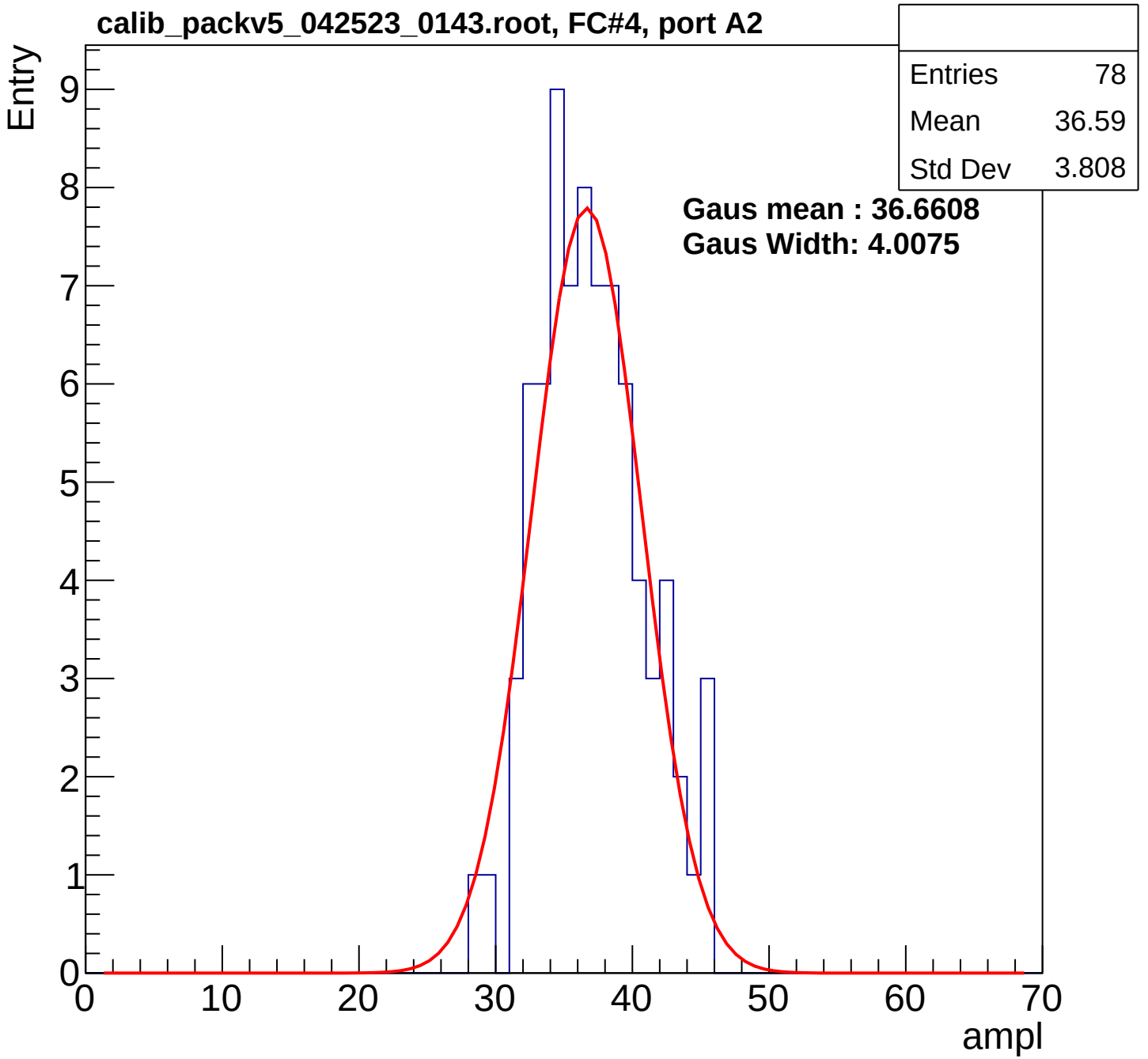

B1L100S, U17-ch0, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 79
Mean 27.54
Std Dev 5.044
Gaus mean : 28.6301
Gaus Width: 3.6834
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U17-ch0, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 78
Mean 36.59
Std Dev 3.808
Gaus mean : 36.6608
Gaus Width: 4.0075
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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40
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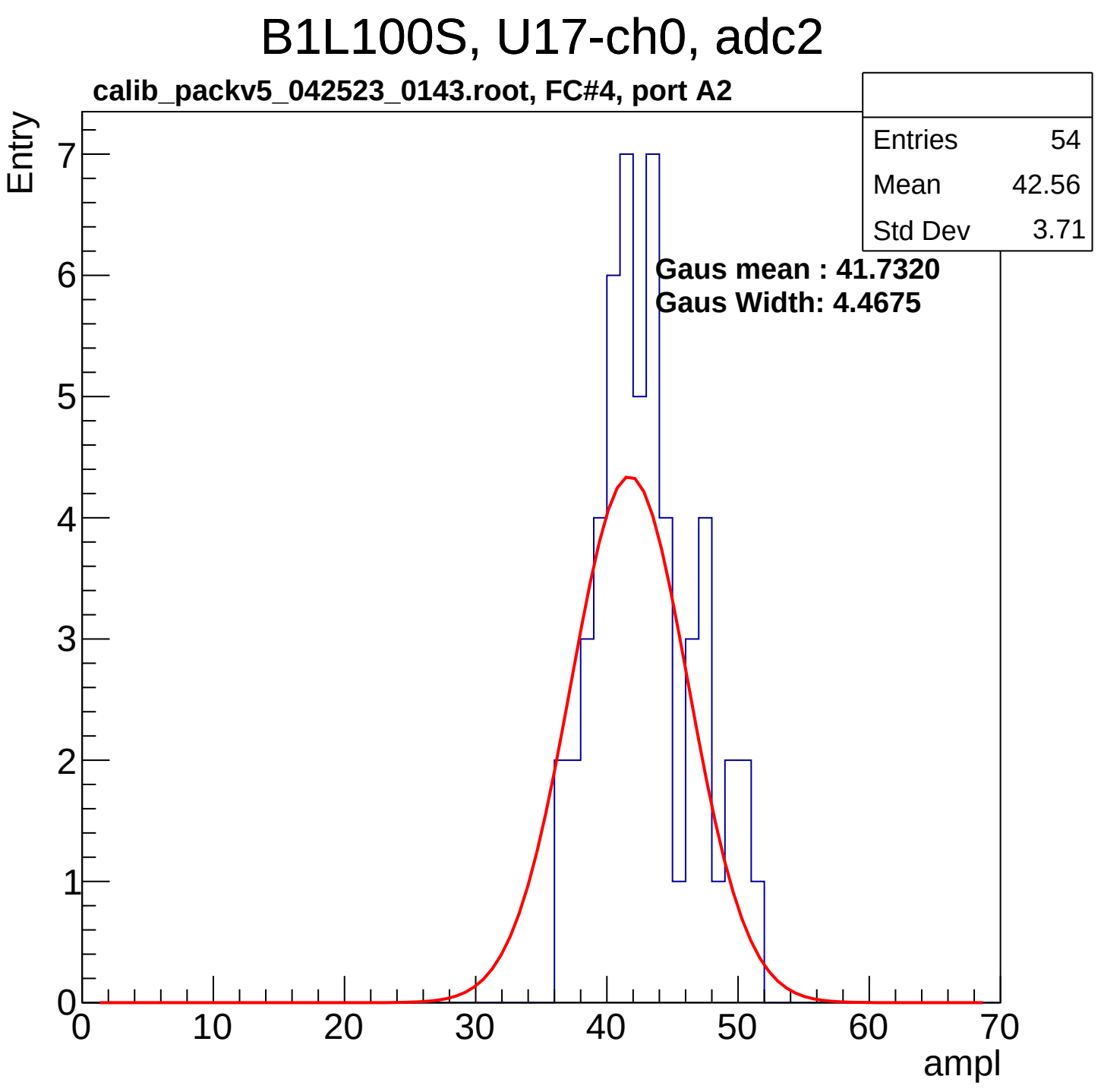
B1L100S, U17-ch0, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 42.56
Std Dev 3.71
Gaus mean : 41.7320
Gaus Width: 4.4675
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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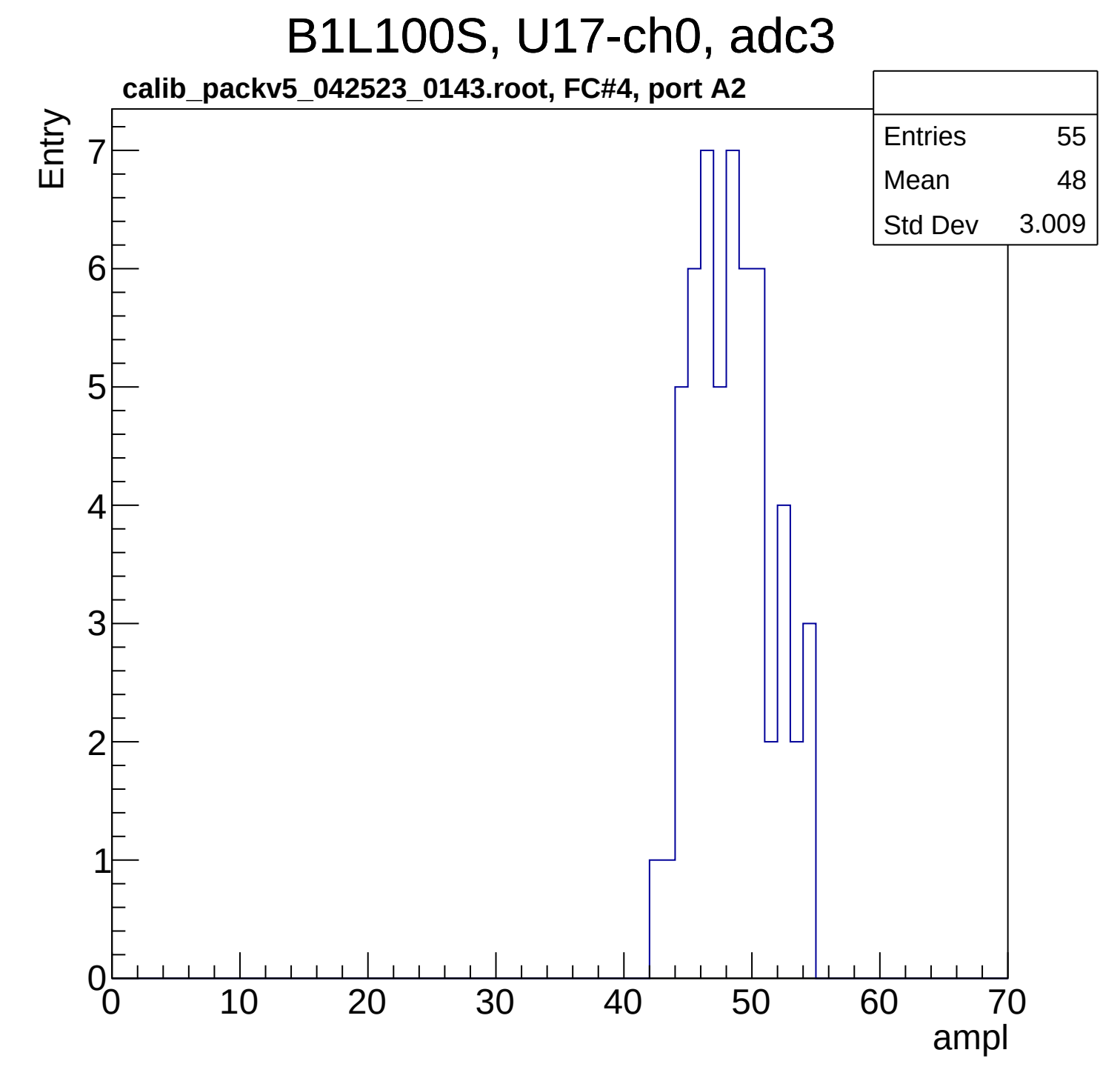
B1L100S, U17-ch0, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 48
Std Dev 3.009
Entry
ampl
0
1
2
3
4
5
6
7
0
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40
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60
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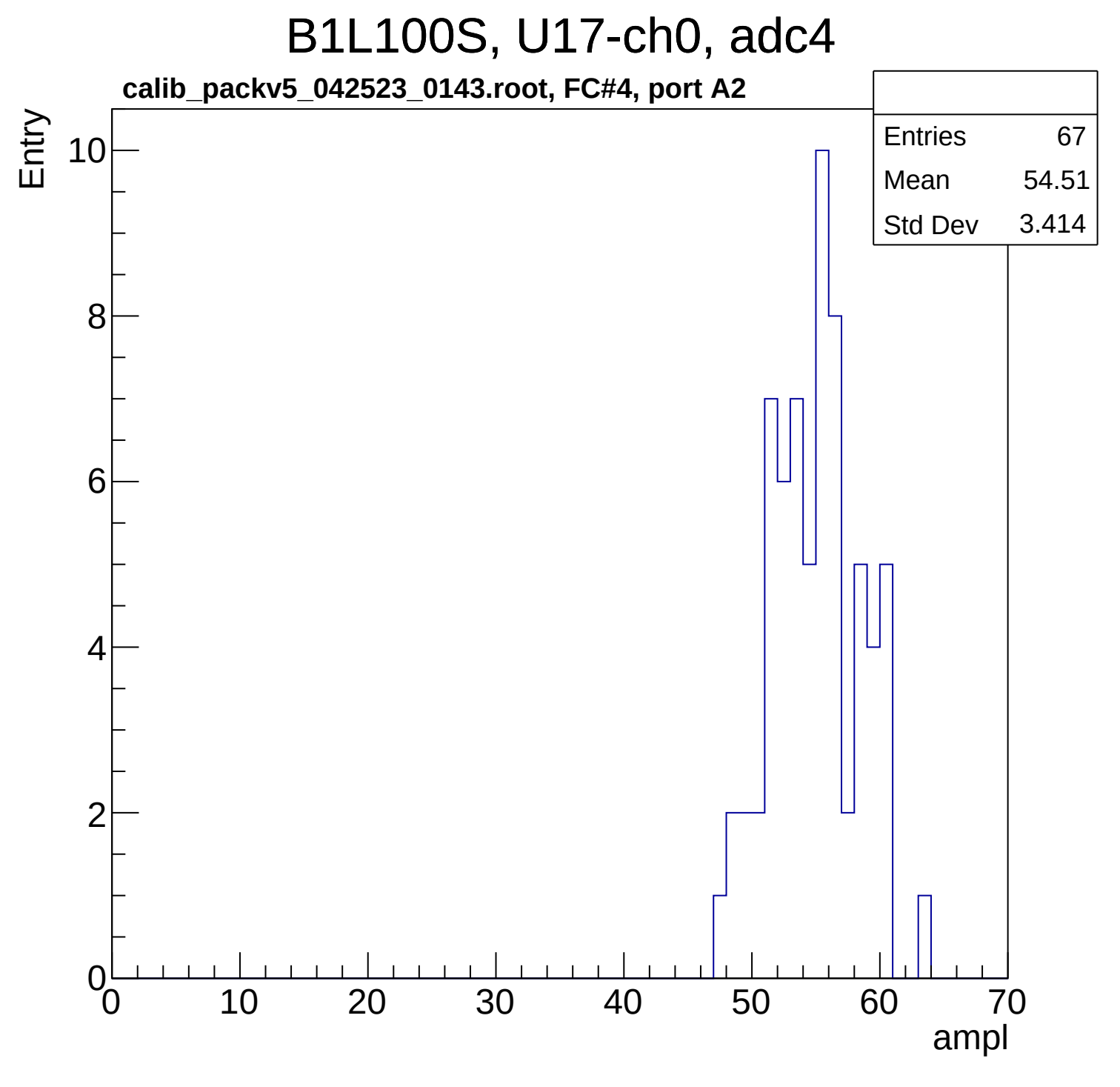
B1L100S, U17-ch0, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 54.51
Std Dev 3.414
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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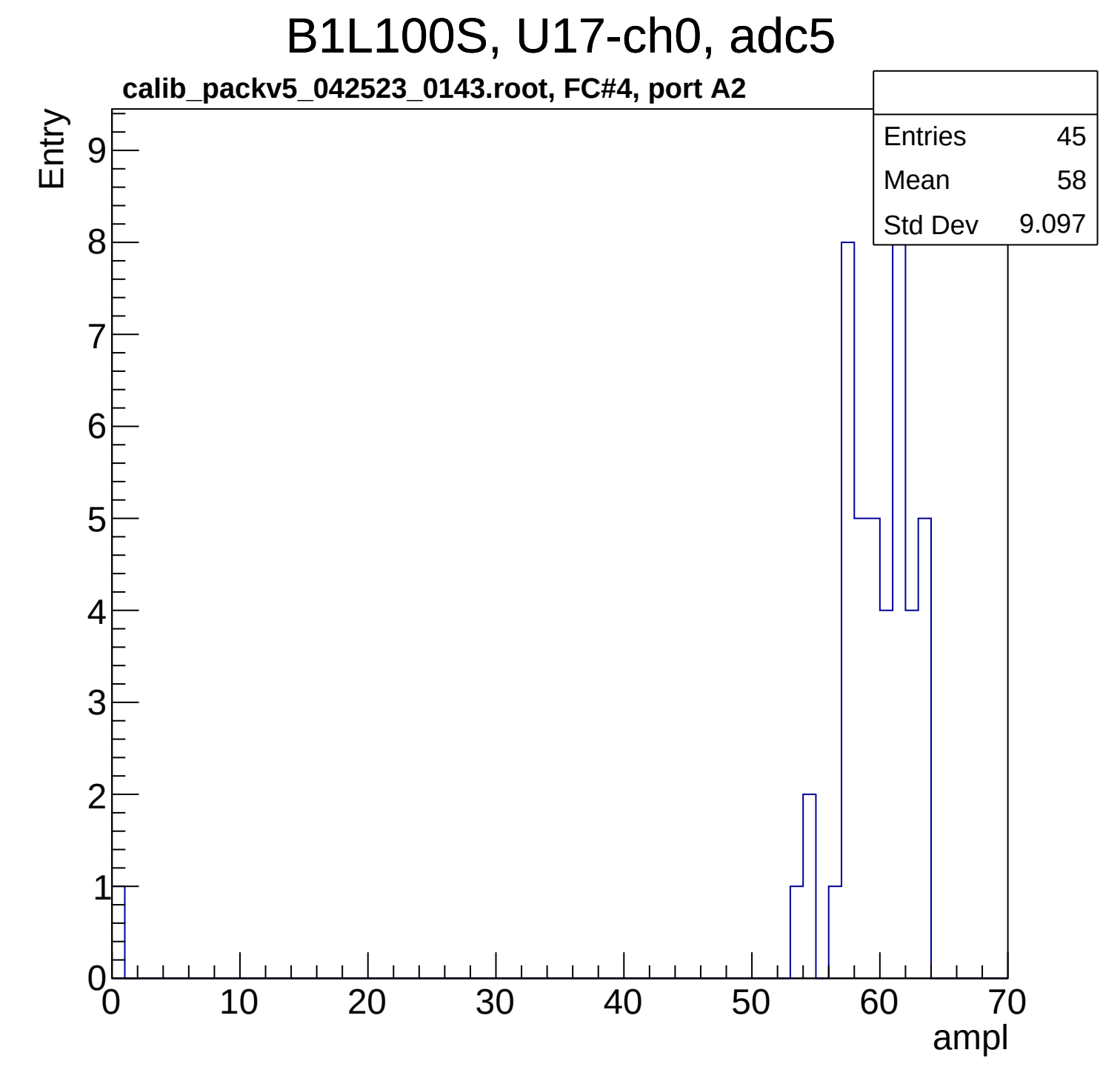
B1L100S, U17-ch0, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 45
Mean 58
Std Dev 9.097
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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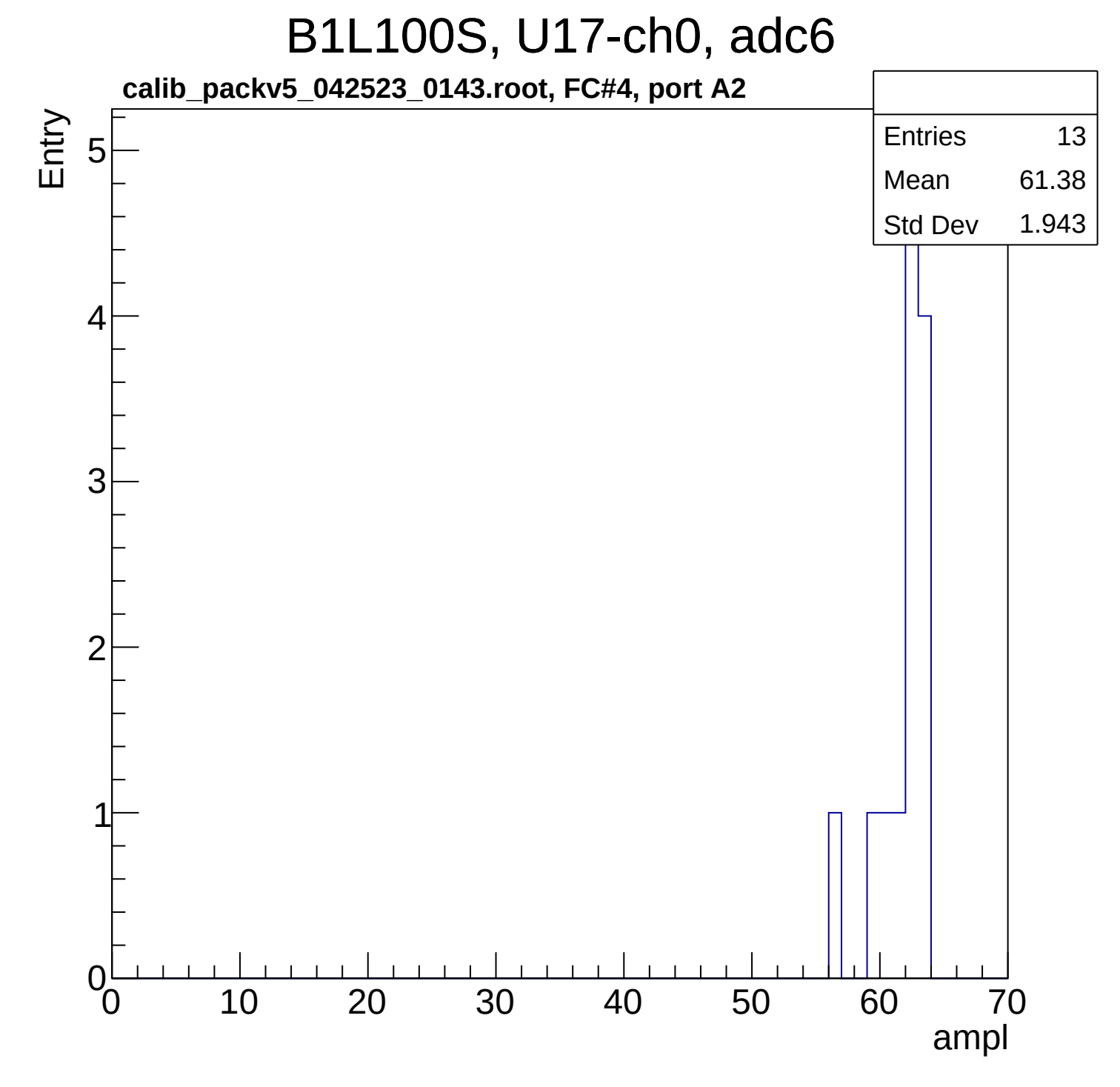
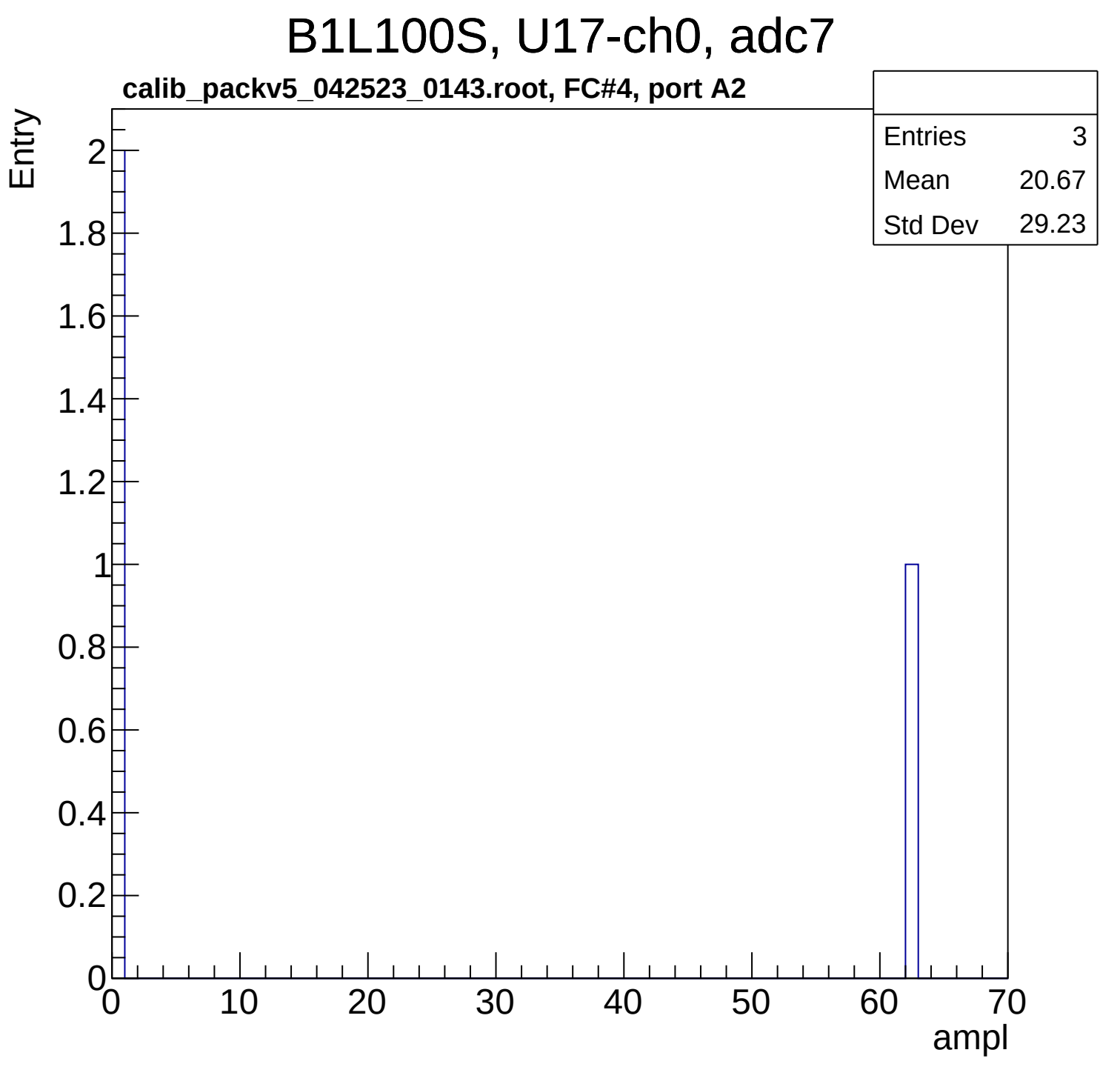

B1L100S, U17-ch0, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 13
Mean 61.38
Std Dev 1.943
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L100S, U17-ch0, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 20.67
Std Dev 29.23
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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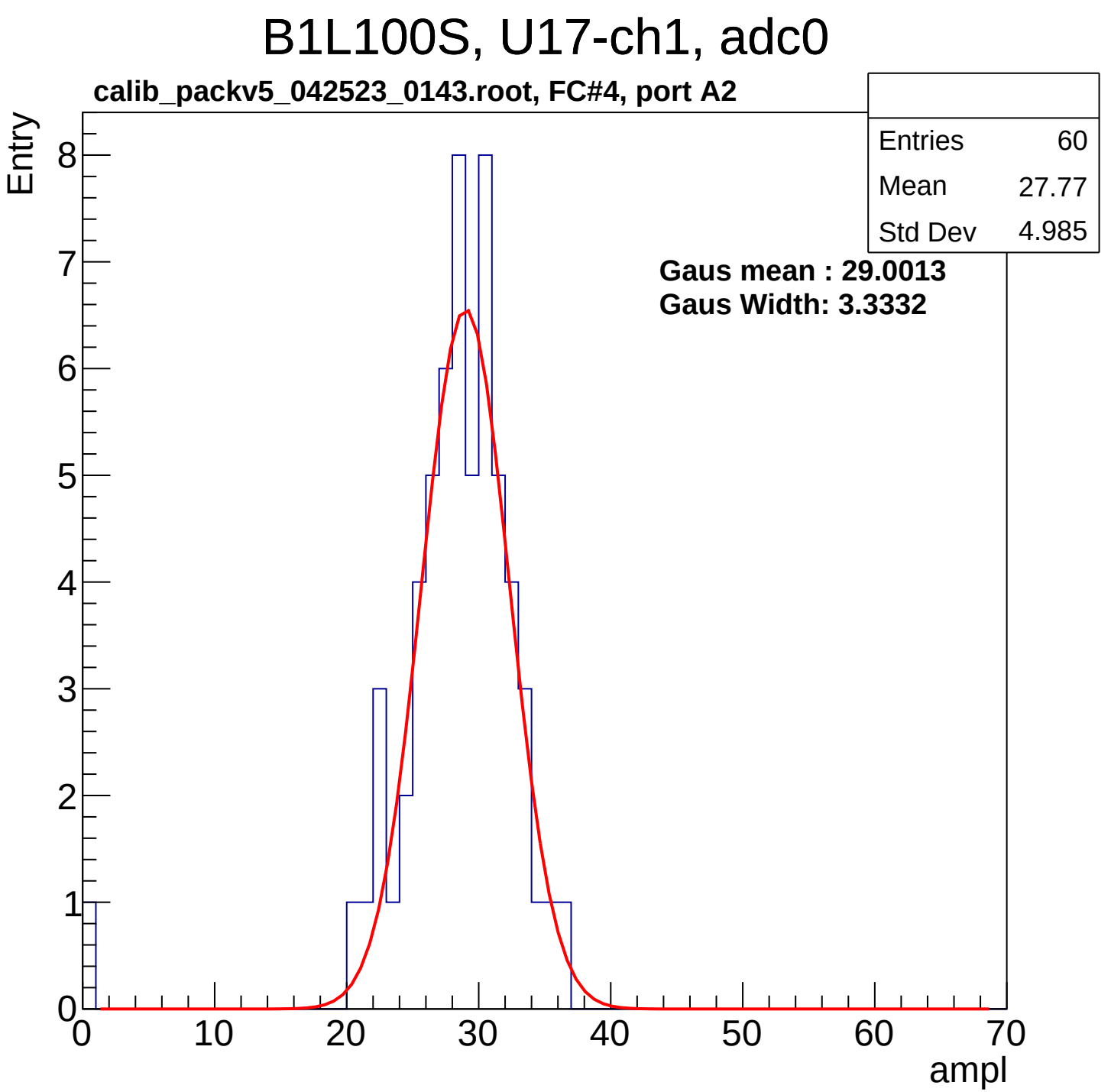
B1L100S, U17-ch1, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 27.77
Std Dev 4.985
Gaus mean : 29.0013
Gaus Width: 3.3332
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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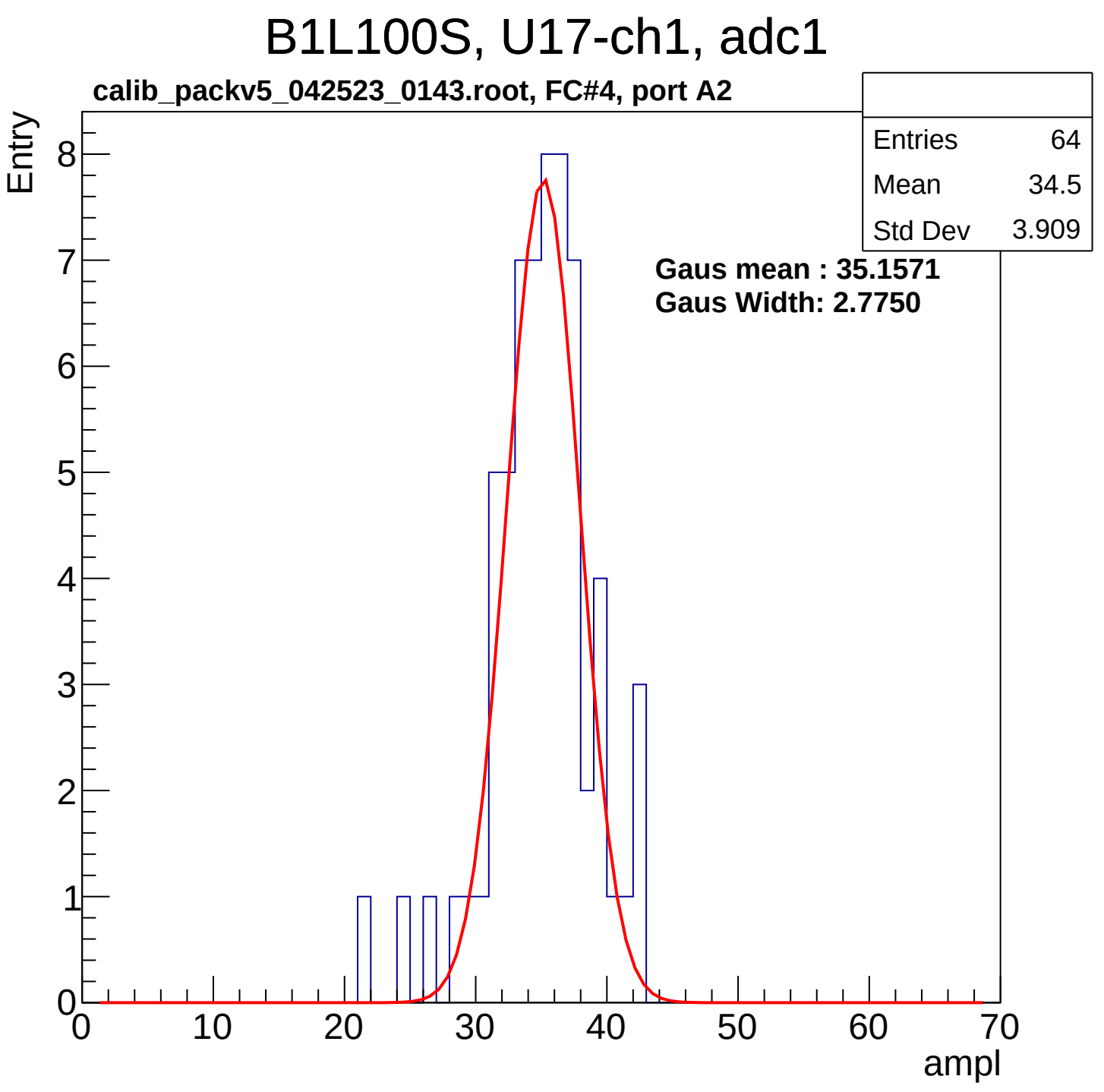
B1L100S, U17-ch1, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 34.5
Std Dev 3.909
Gaus mean : 35.1571
Gaus Width: 2.7750
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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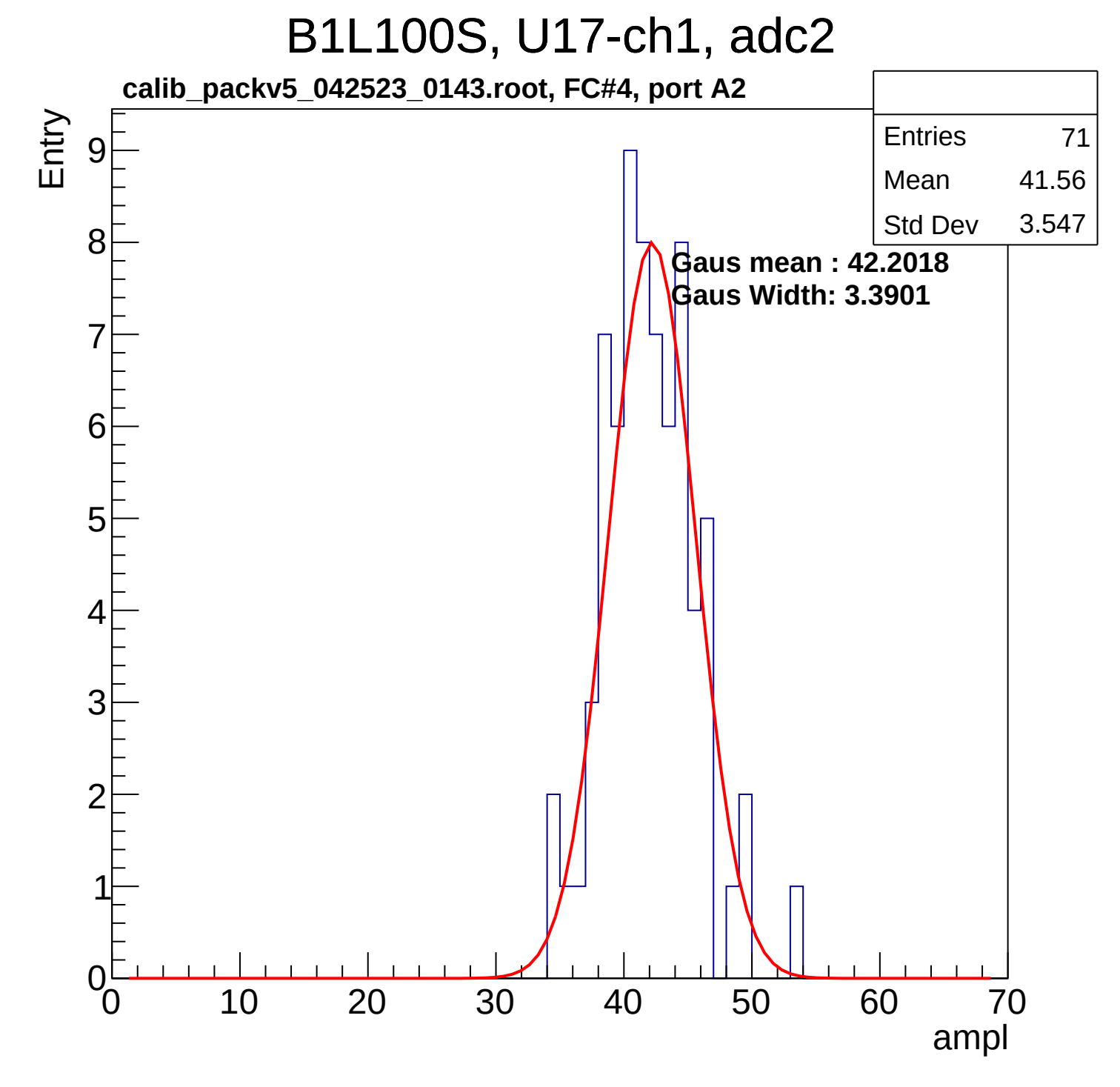
B1L100S, U17-ch1, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 41.56
Std Dev 3.547
Gaus mean : 42.2018
Gaus Width: 3.3901
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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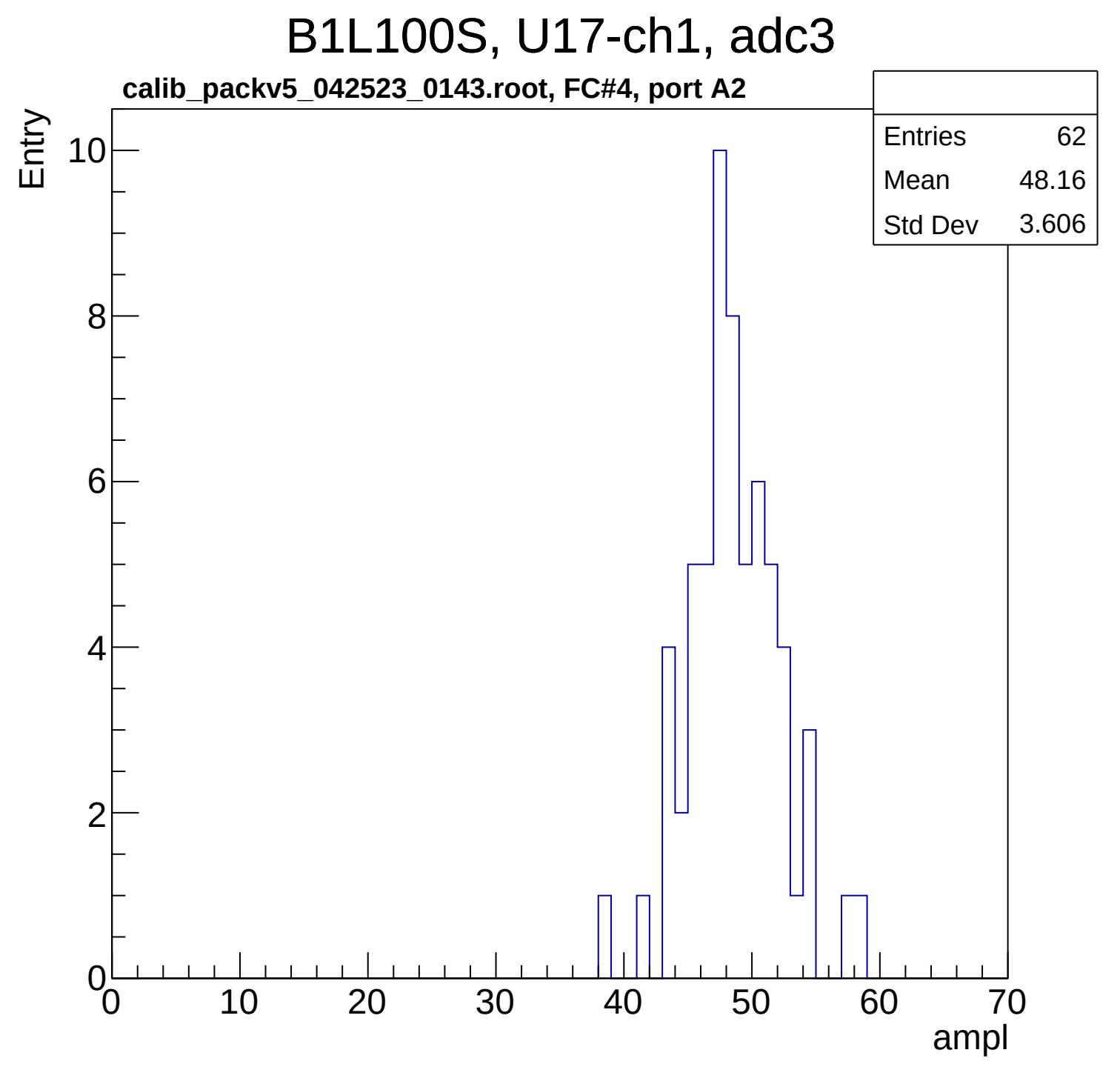
B1L100S, U17-ch1, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 48.16
Std Dev 3.606
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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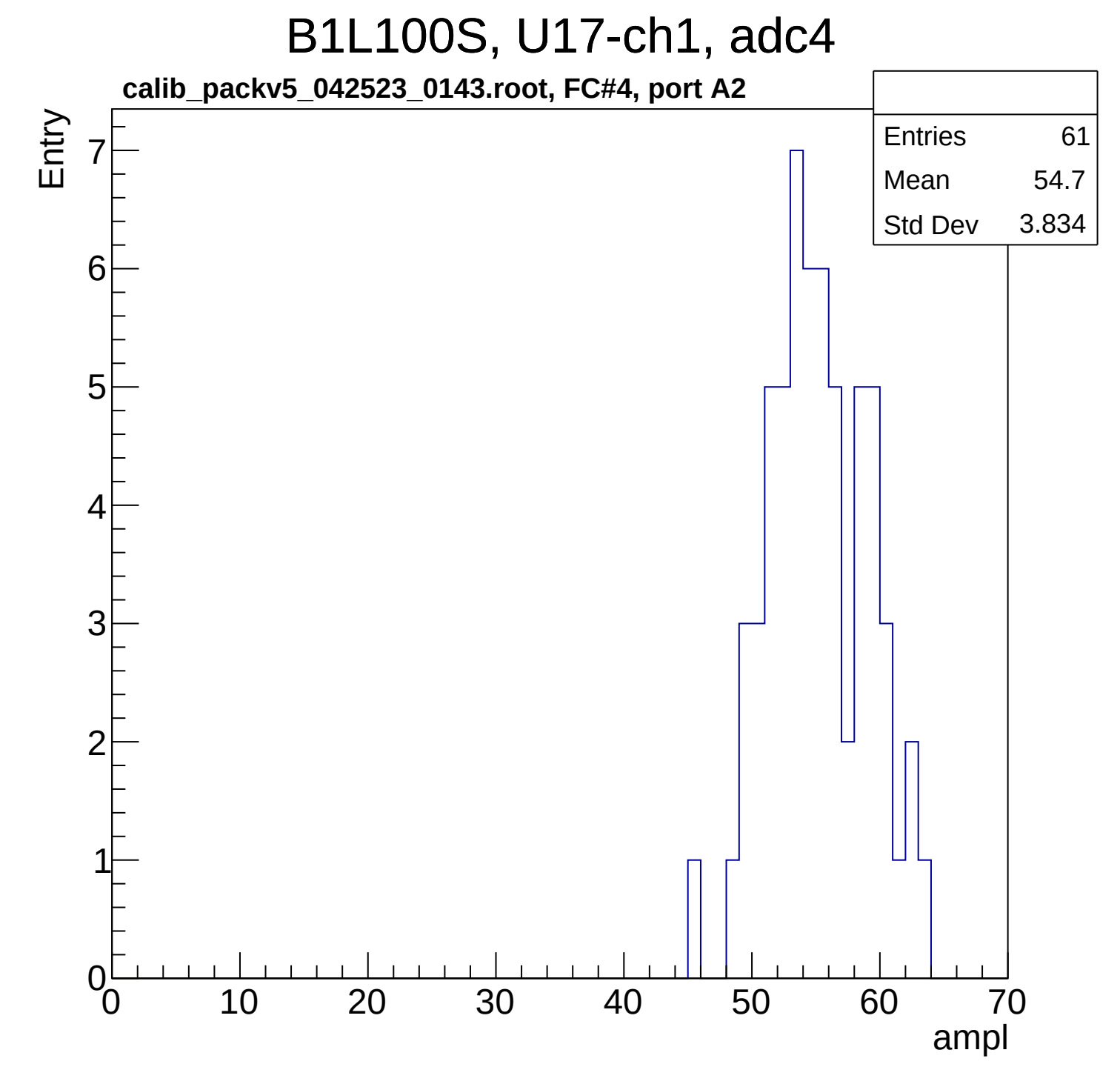
B1L100S, U17-ch1, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 54.7
Std Dev 3.834
Entry
ampl
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1
2
3
4
5
6
7
0
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20
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40
50
60
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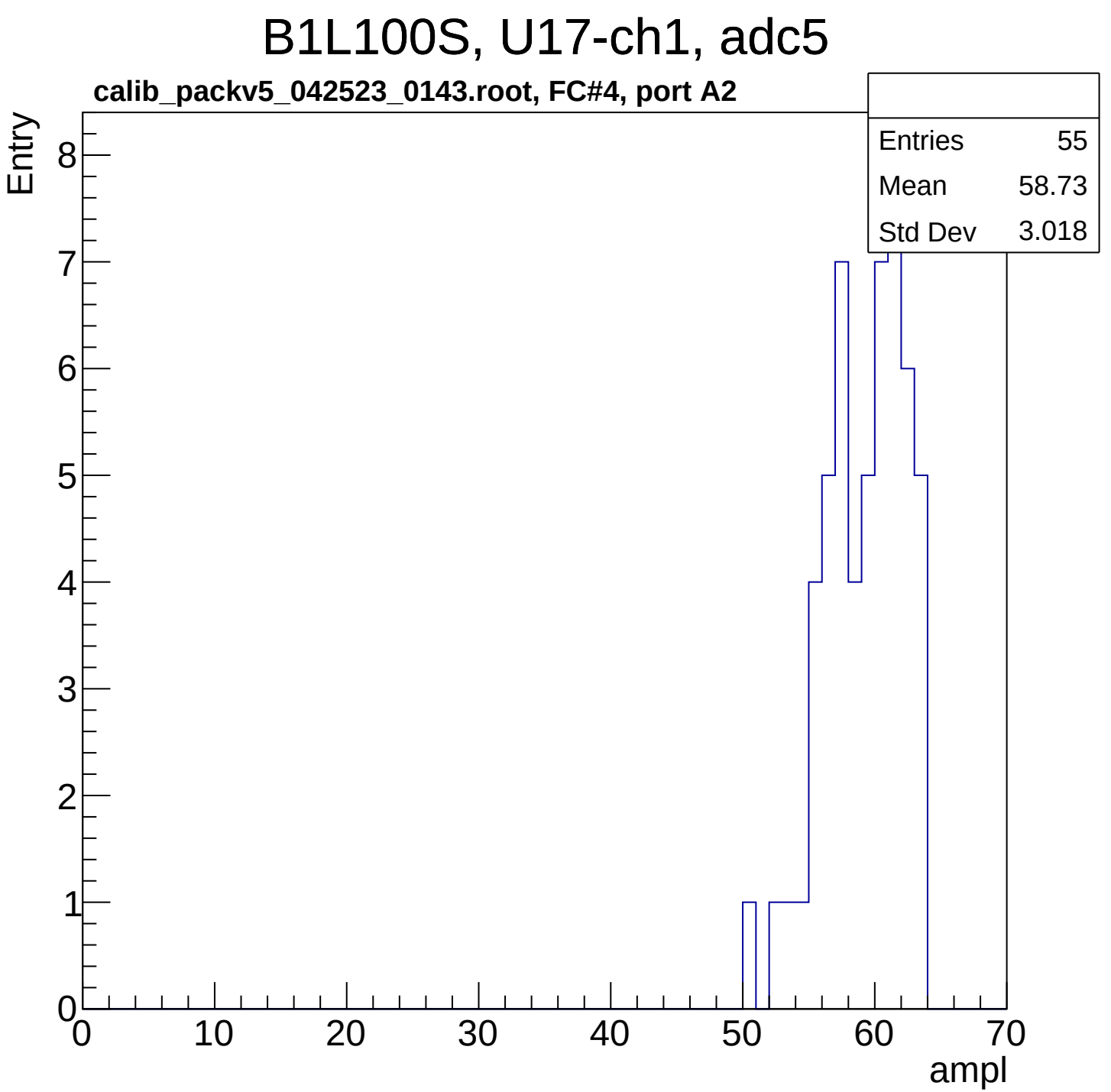
B1L100S, U17-ch1, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 58.73
Std Dev 3.018
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
50
60
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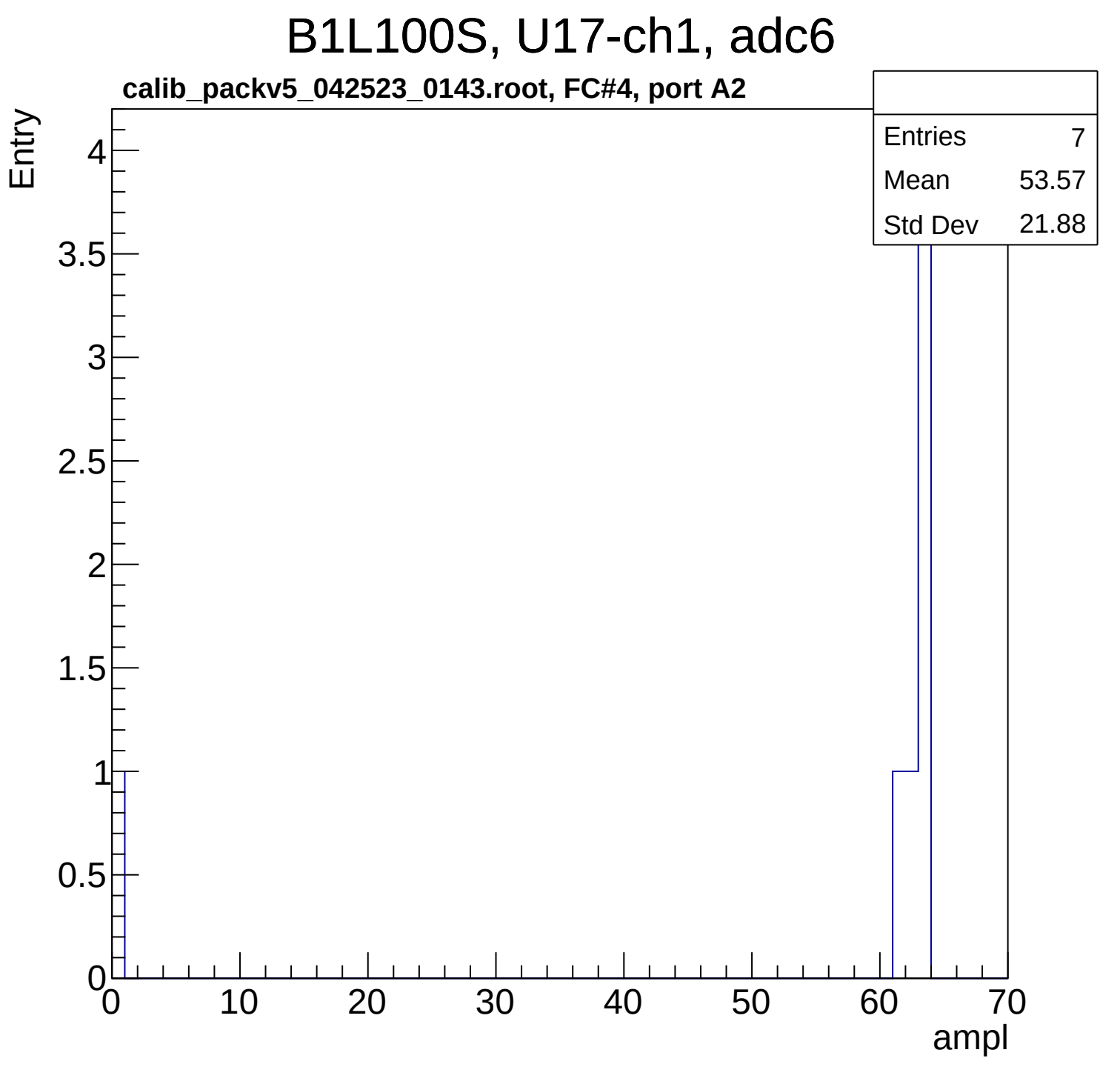
B1L100S, U17-ch1, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 7
Mean 53.57
Std Dev 21.88
Entry
ampl
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0.5
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1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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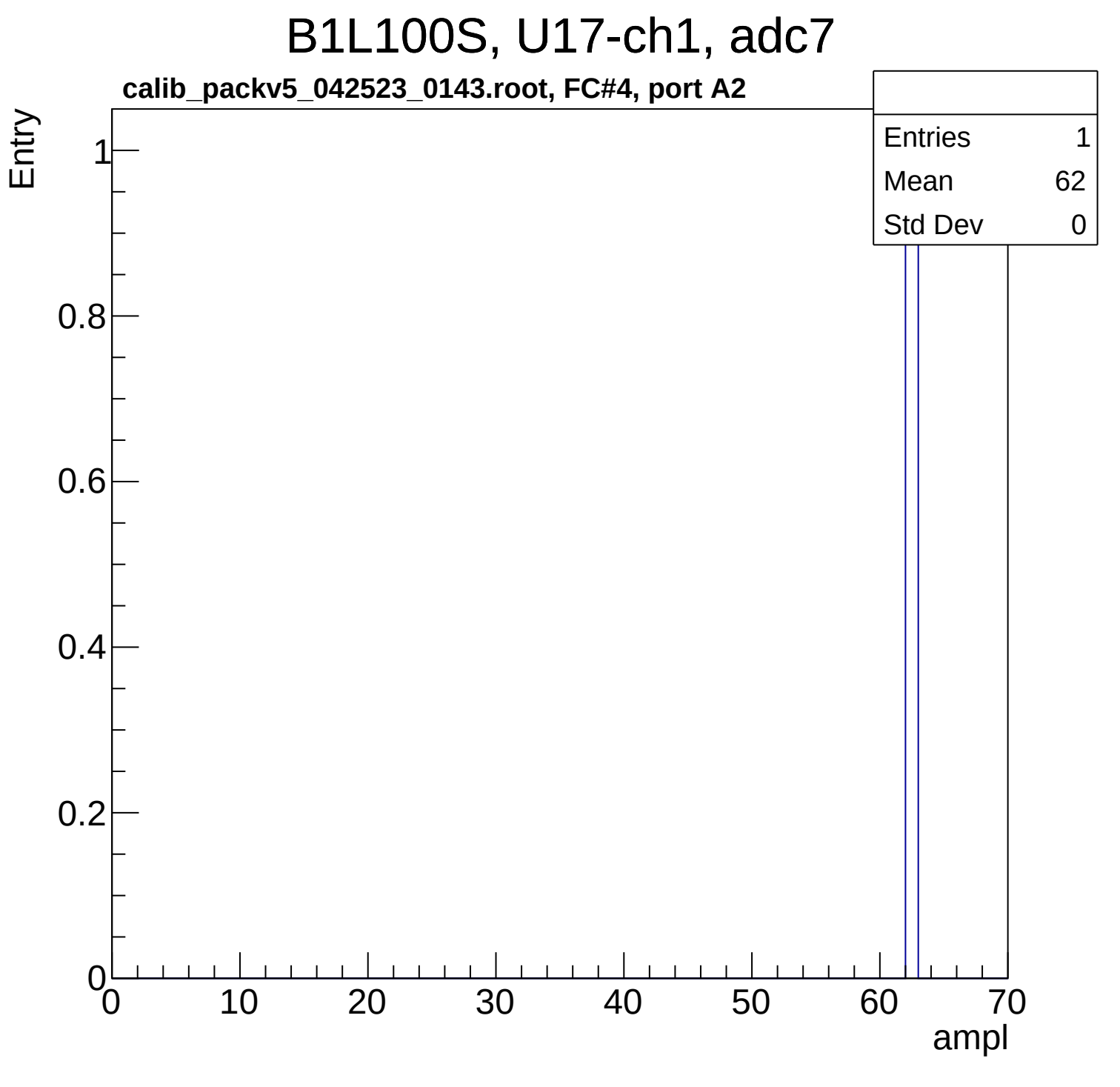
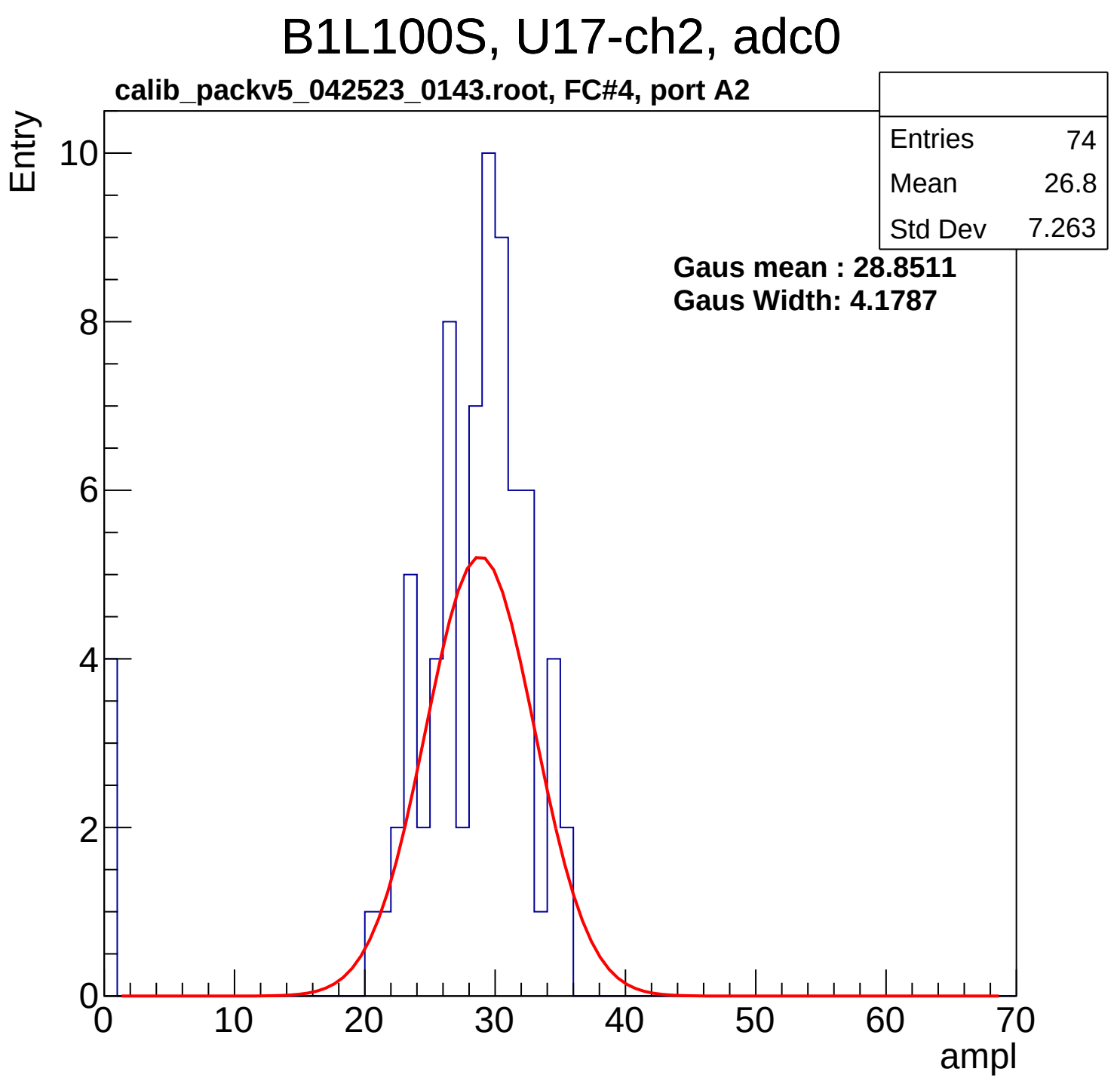

B1L100S, U17-ch1, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 62
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch2, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 74
Mean 26.8
Std Dev 7.263
Gaus mean : 28.8511
Gaus Width: 4.1787
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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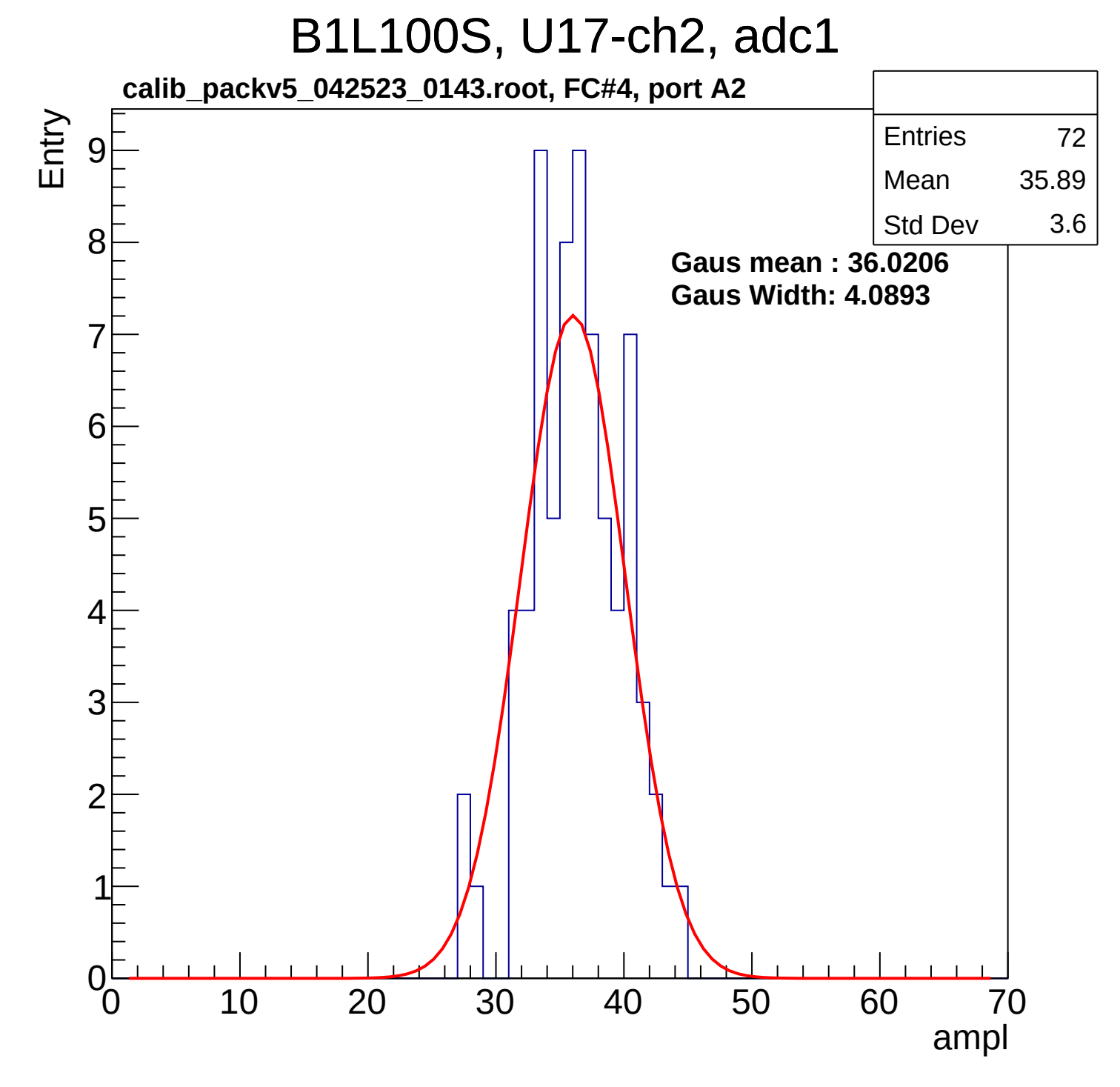
B1L100S, U17-ch2, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 35.89
Std Dev 3.6
Gaus mean : 36.0206
Gaus Width: 4.0893
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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20
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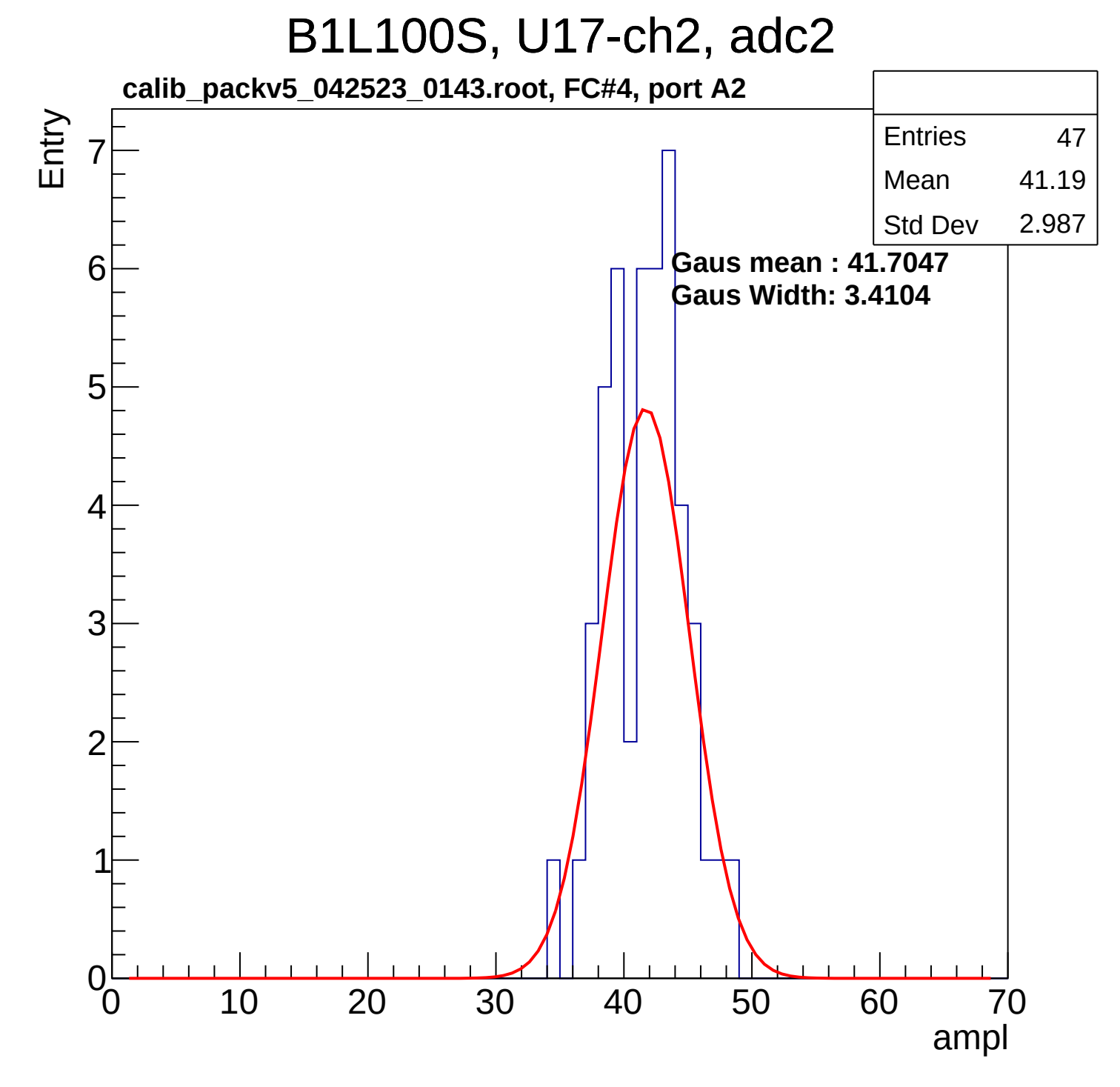
B1L100S, U17-ch2, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 47
Mean 41.19
Std Dev 2.987
Gaus mean : 41.7047
Gaus Width: 3.4104
Entry
ampl
0
1
2
3
4
5
6
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0
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60
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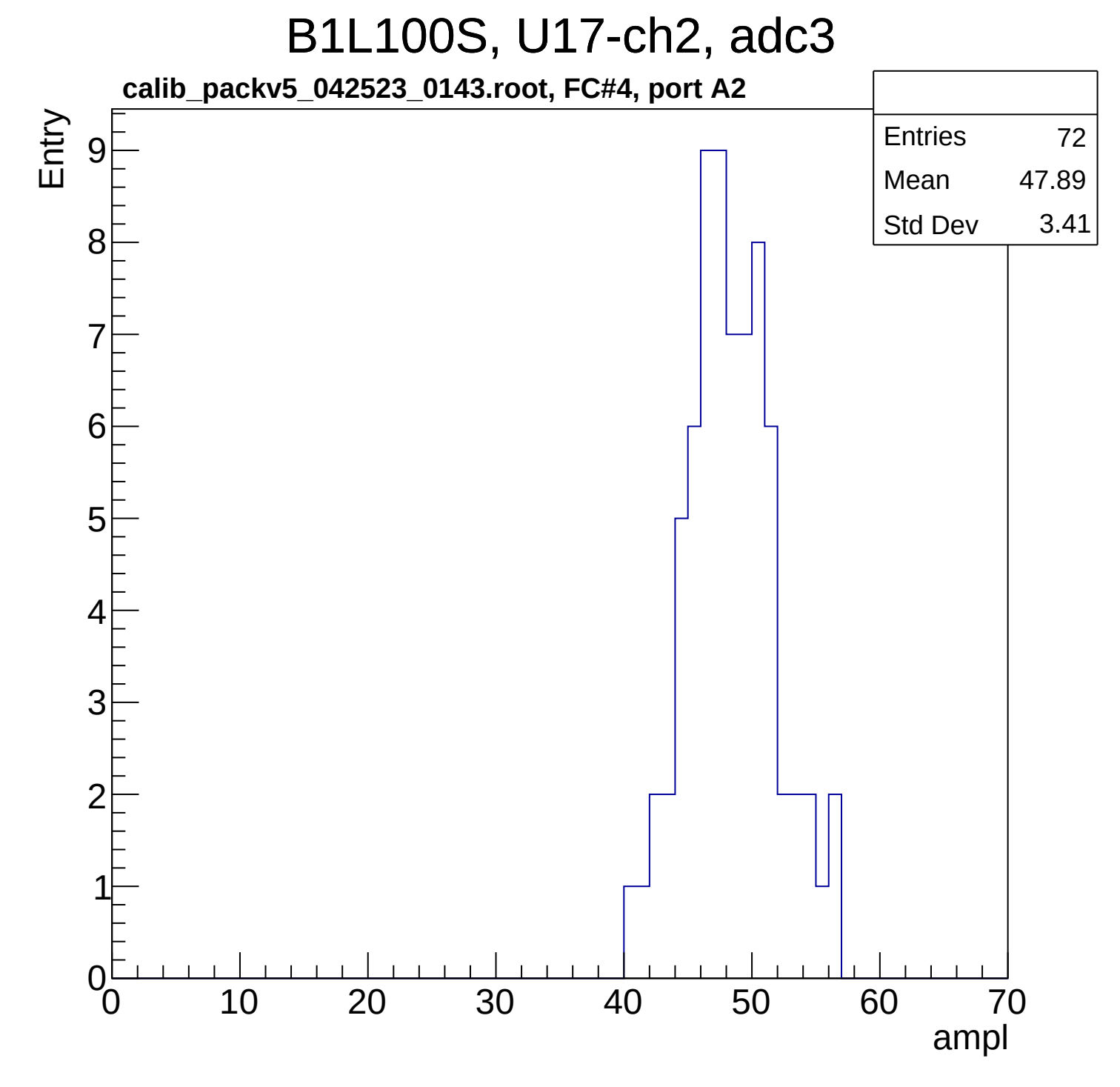
B1L100S, U17-ch2, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 47.89
Std Dev 3.41
Entry
ampl
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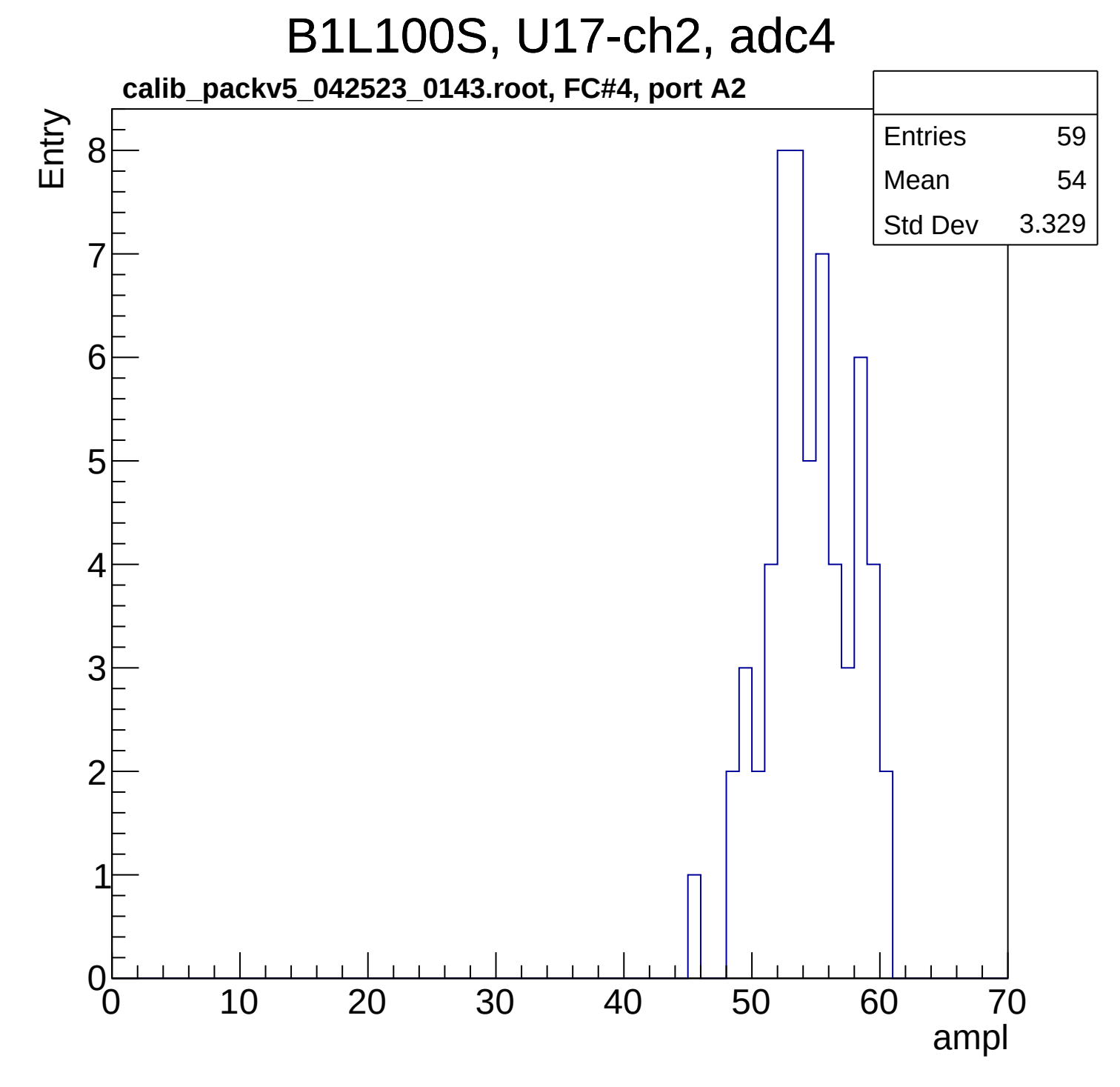
B1L100S, U17-ch2, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 54
Std Dev 3.329
Entry
ampl
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1
2
3
4
5
6
7
8
0
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40
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60
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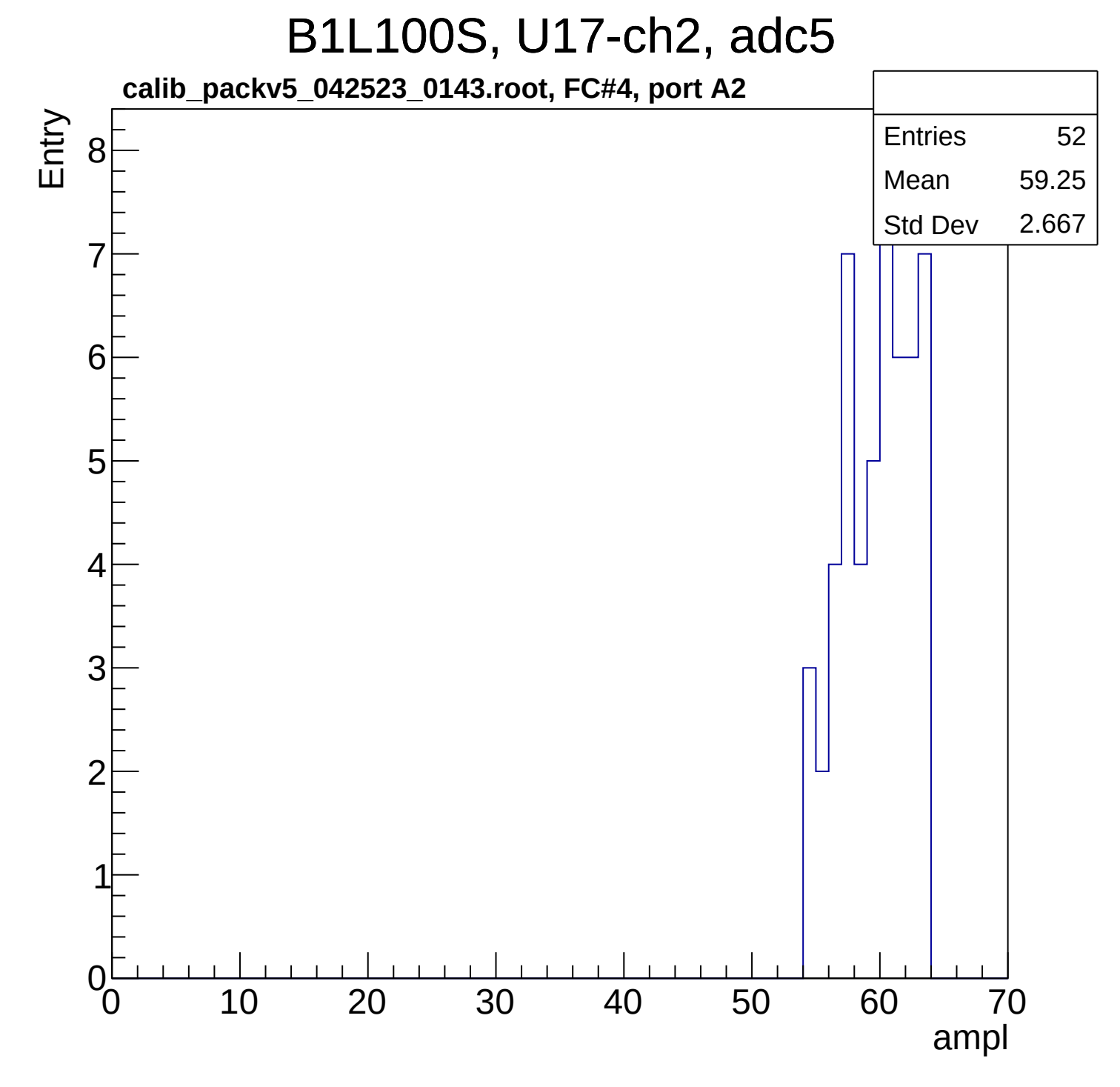
B1L100S, U17-ch2, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 52
Mean 59.25
Std Dev 2.667
Entry
ampl
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2
3
4
5
6
7
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0
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60
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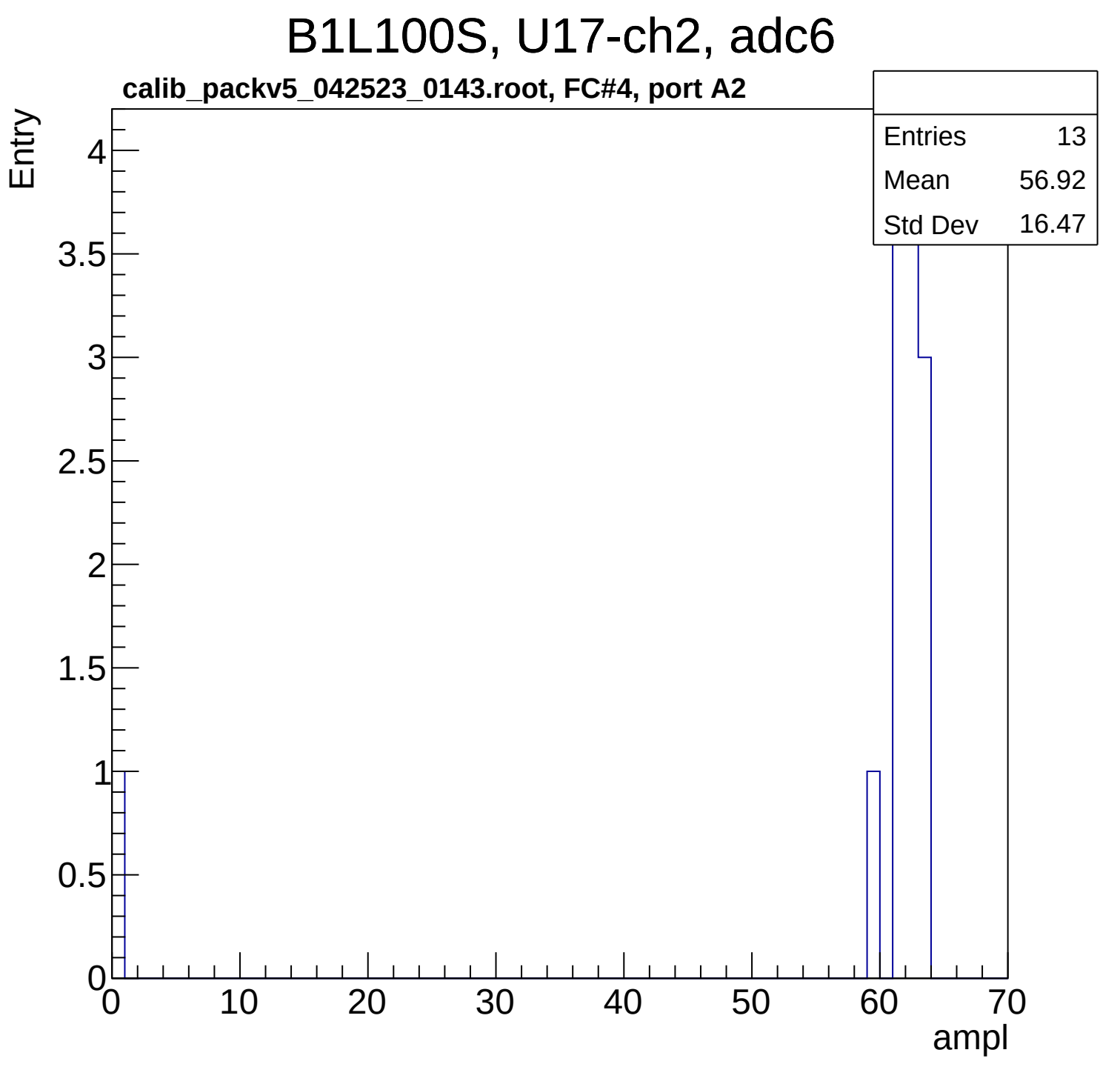
B1L100S, U17-ch2, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 13
Mean 56.92
Std Dev 16.47
Entry
ampl
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1
1.5
2
2.5
3
3.5
4
0
10
20
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40
50
60
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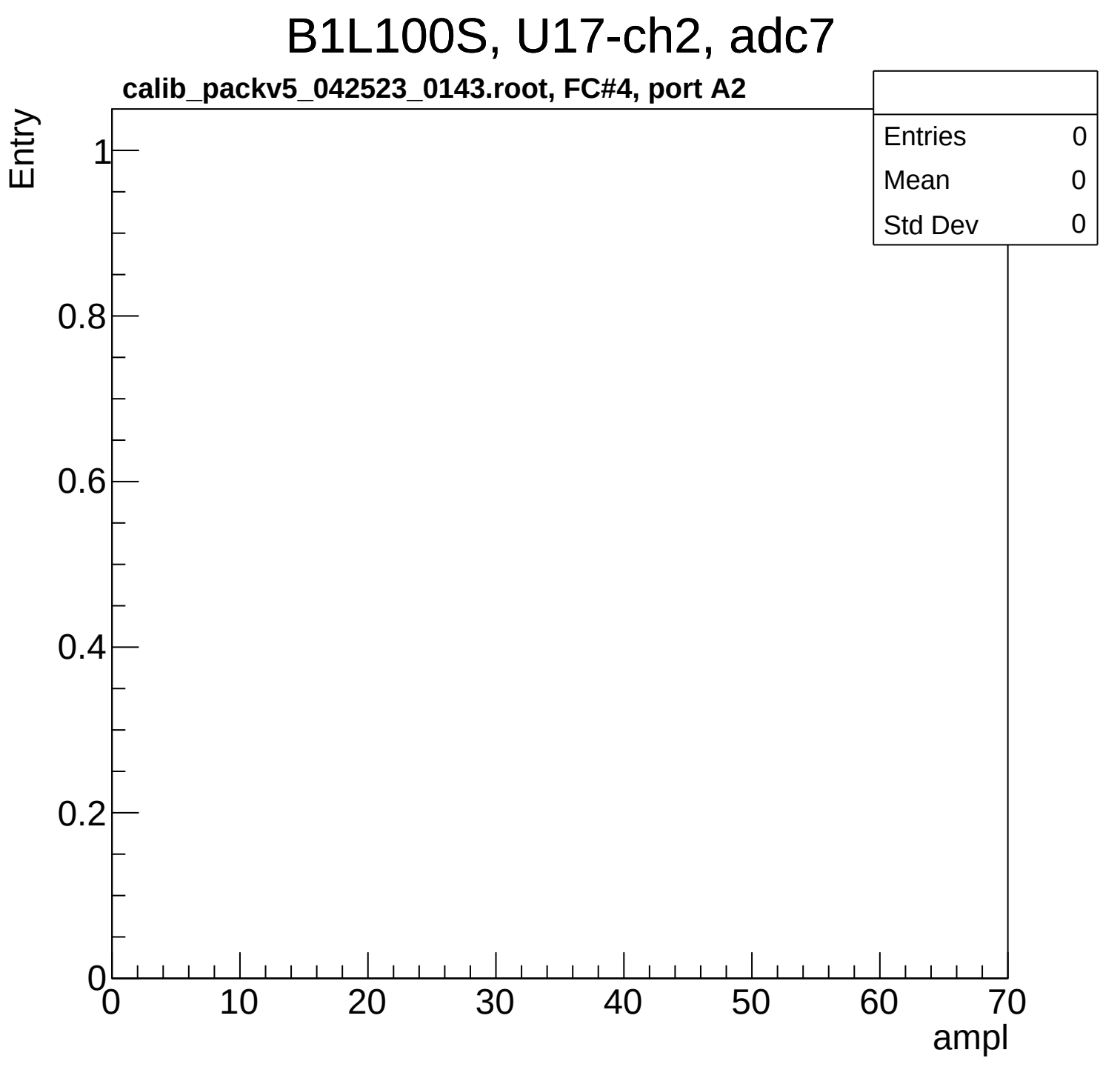
B1L100S, U17-ch2, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
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0.6
0.4
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10
20
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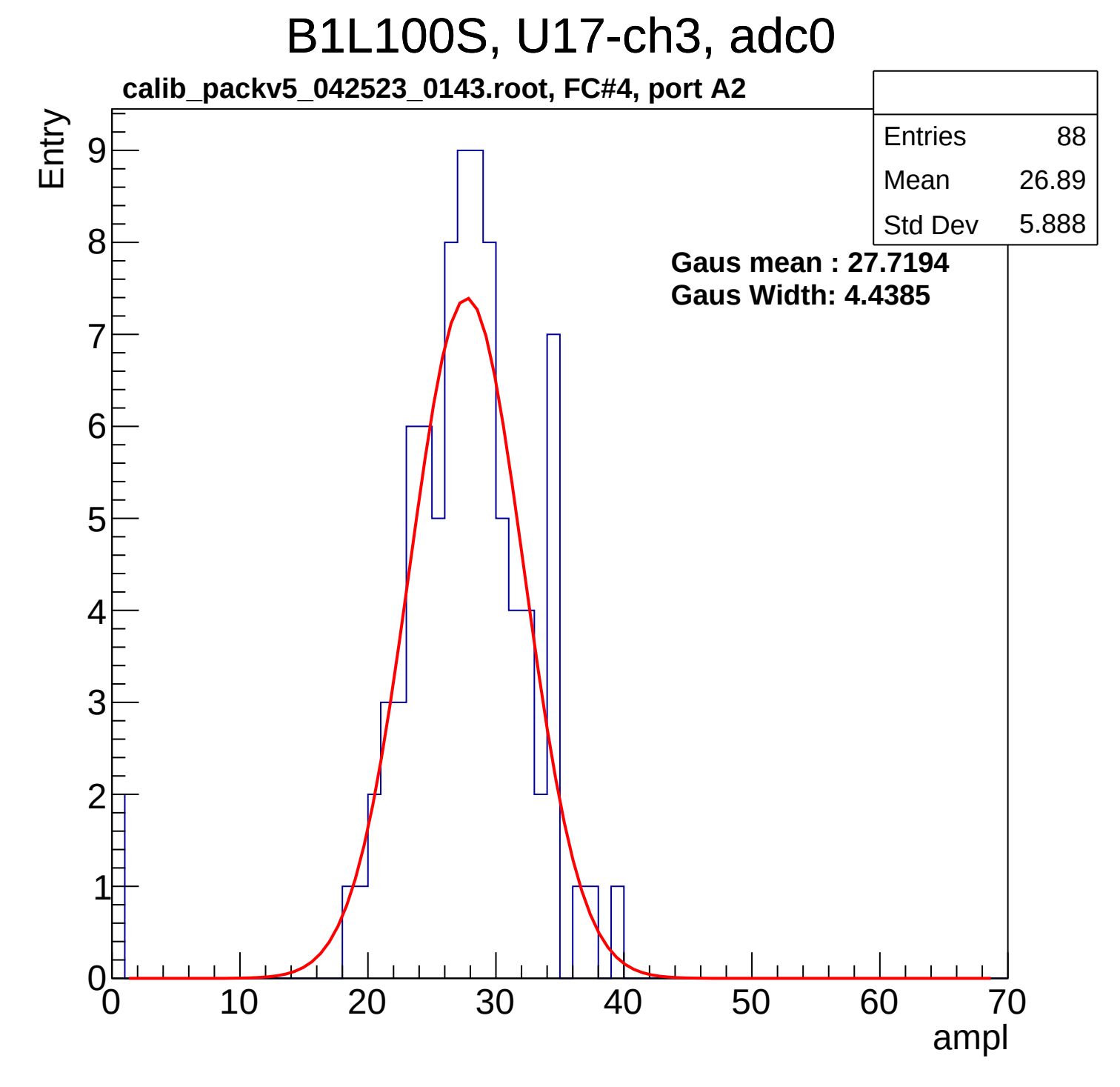
40
50
60
70
ampl


B1L100S, U17-ch3, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 88
Mean 26.89
Std Dev 5.888
Gaus mean : 27.7194
Gaus Width: 4.4385
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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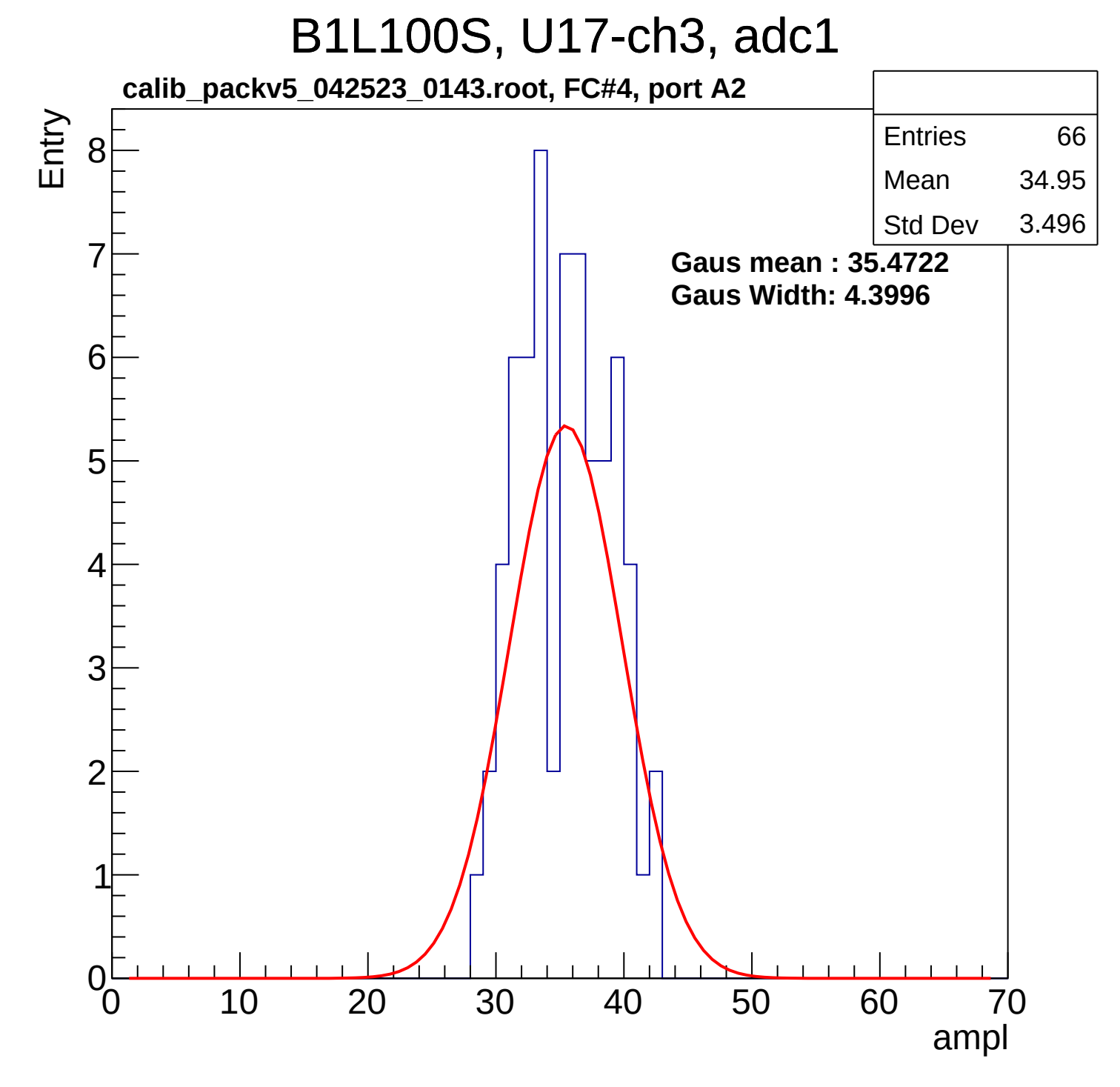
B1L100S, U17-ch3, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 34.95
Std Dev 3.496
Gaus mean : 35.4722
Gaus Width: 4.3996
Entry
ampl
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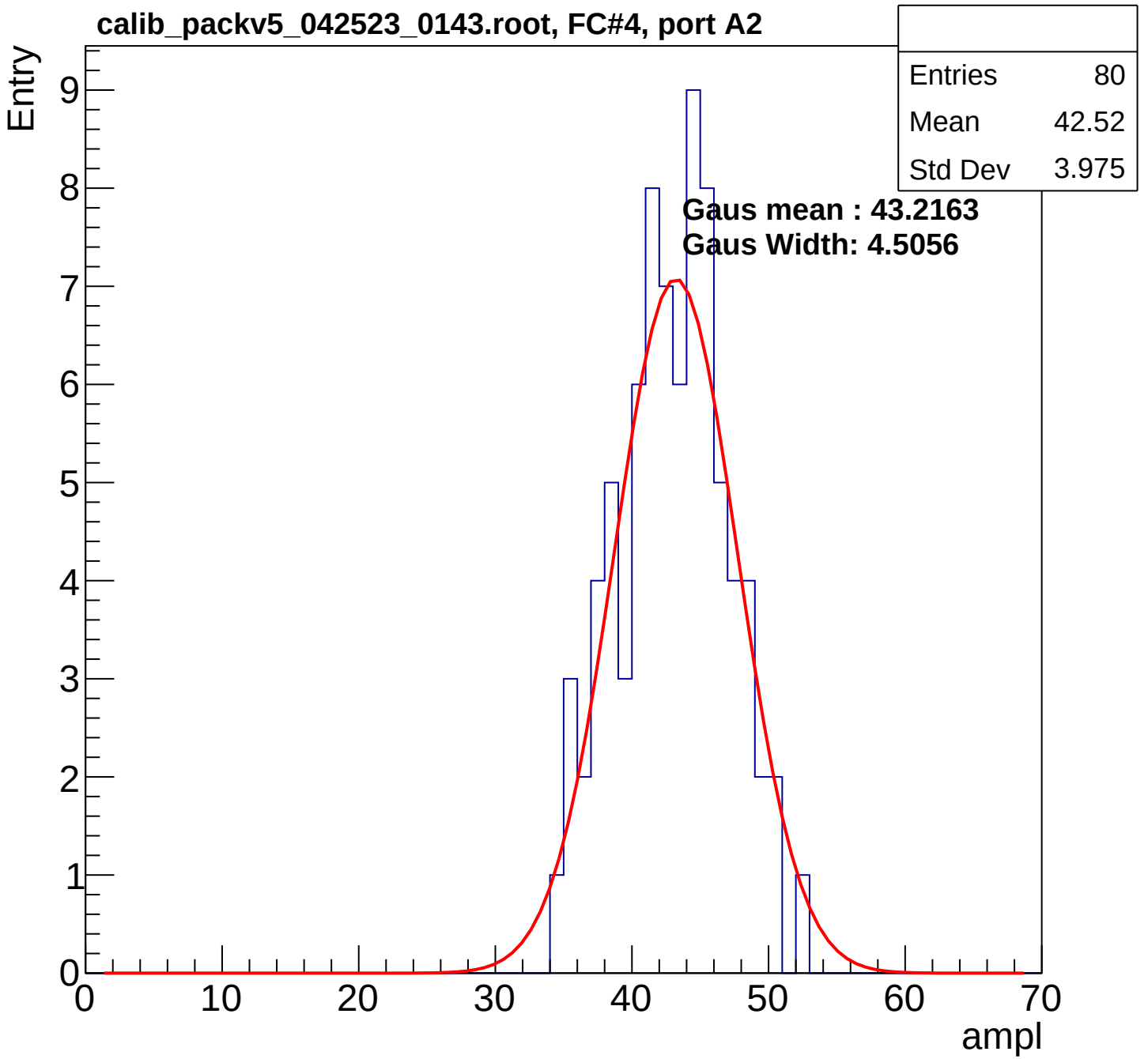
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch3, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 80
Mean 42.52
Std Dev 3.975
Gaus mean : 43.2163
Gaus Width: 4.5056
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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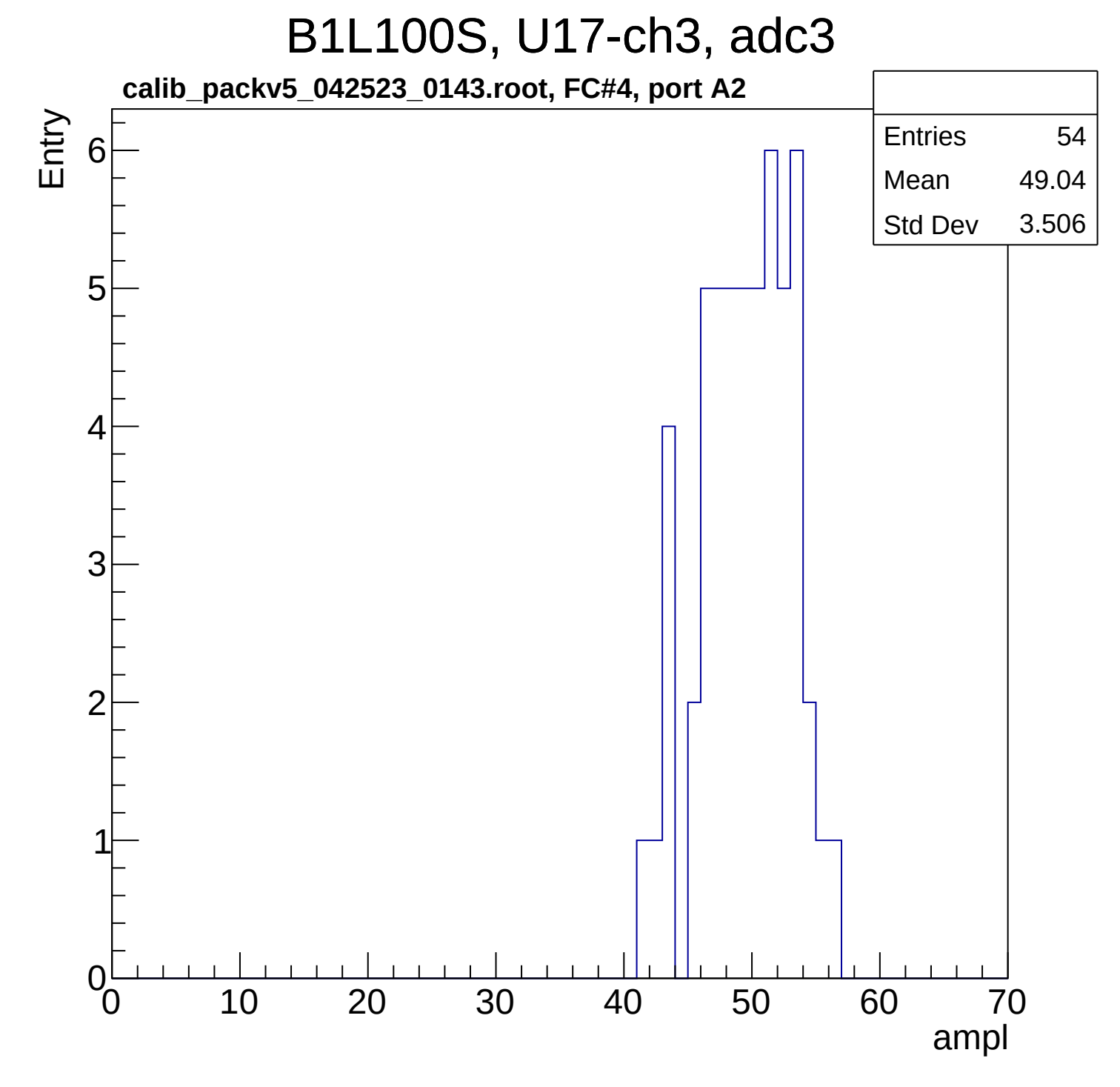
B1L100S, U17-ch3, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 49.04
Std Dev 3.506
Entry
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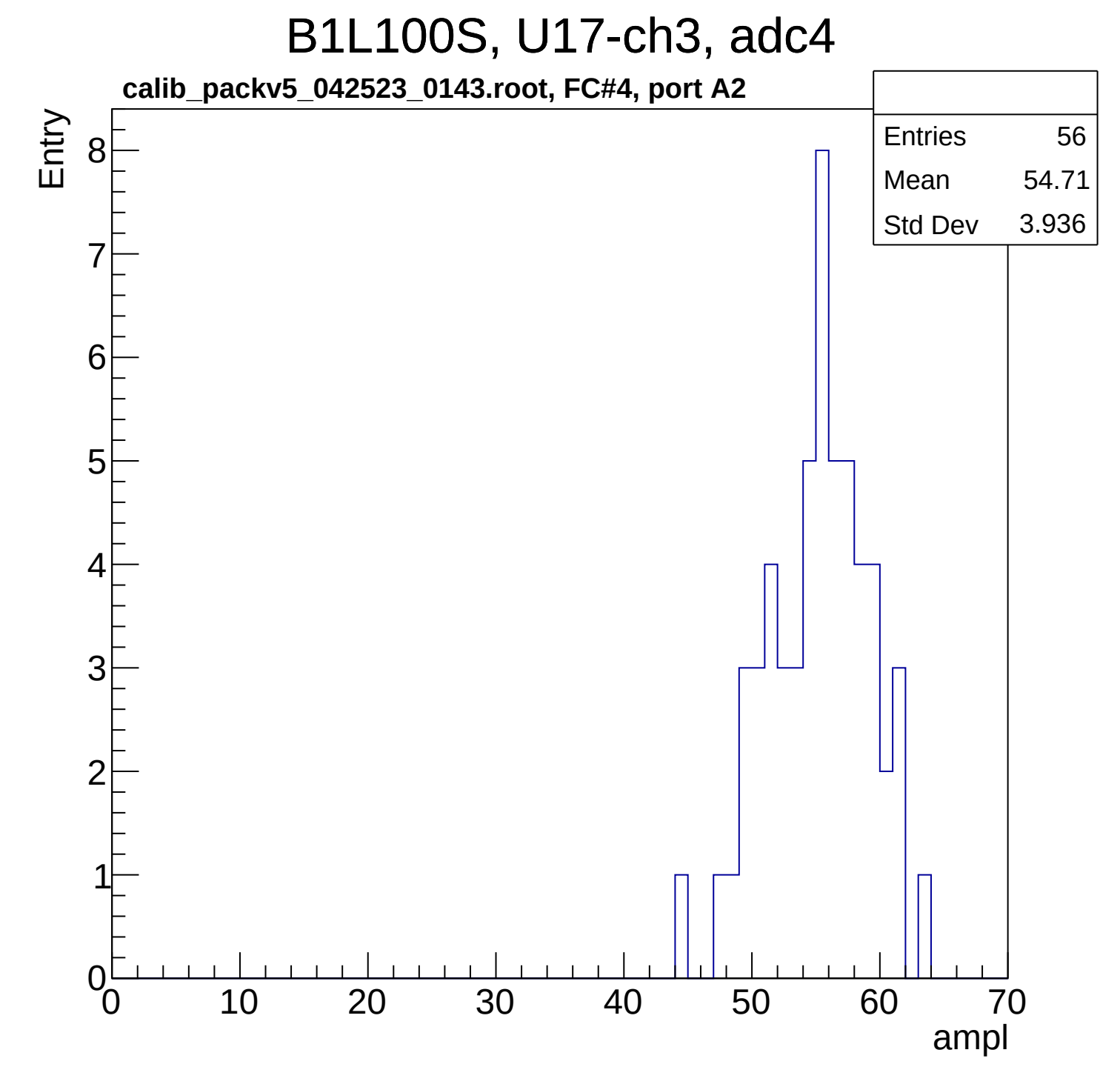
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch3, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 54.71
Std Dev 3.936
Entry
ampl
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2
3
4
5
6
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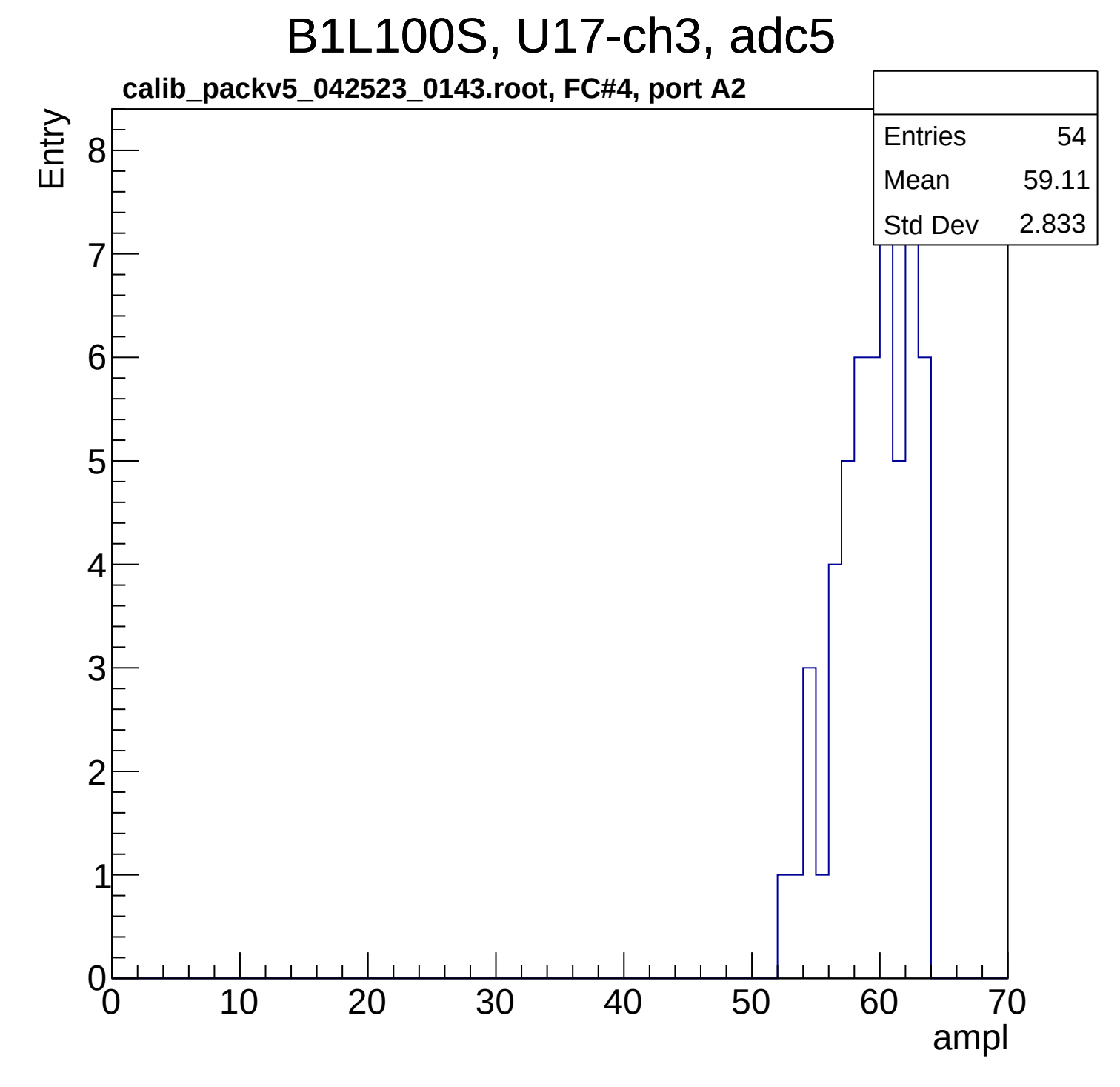
B1L100S, U17-ch3, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 59.11
Std Dev 2.833
Entry
ampl
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2
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4
5
6
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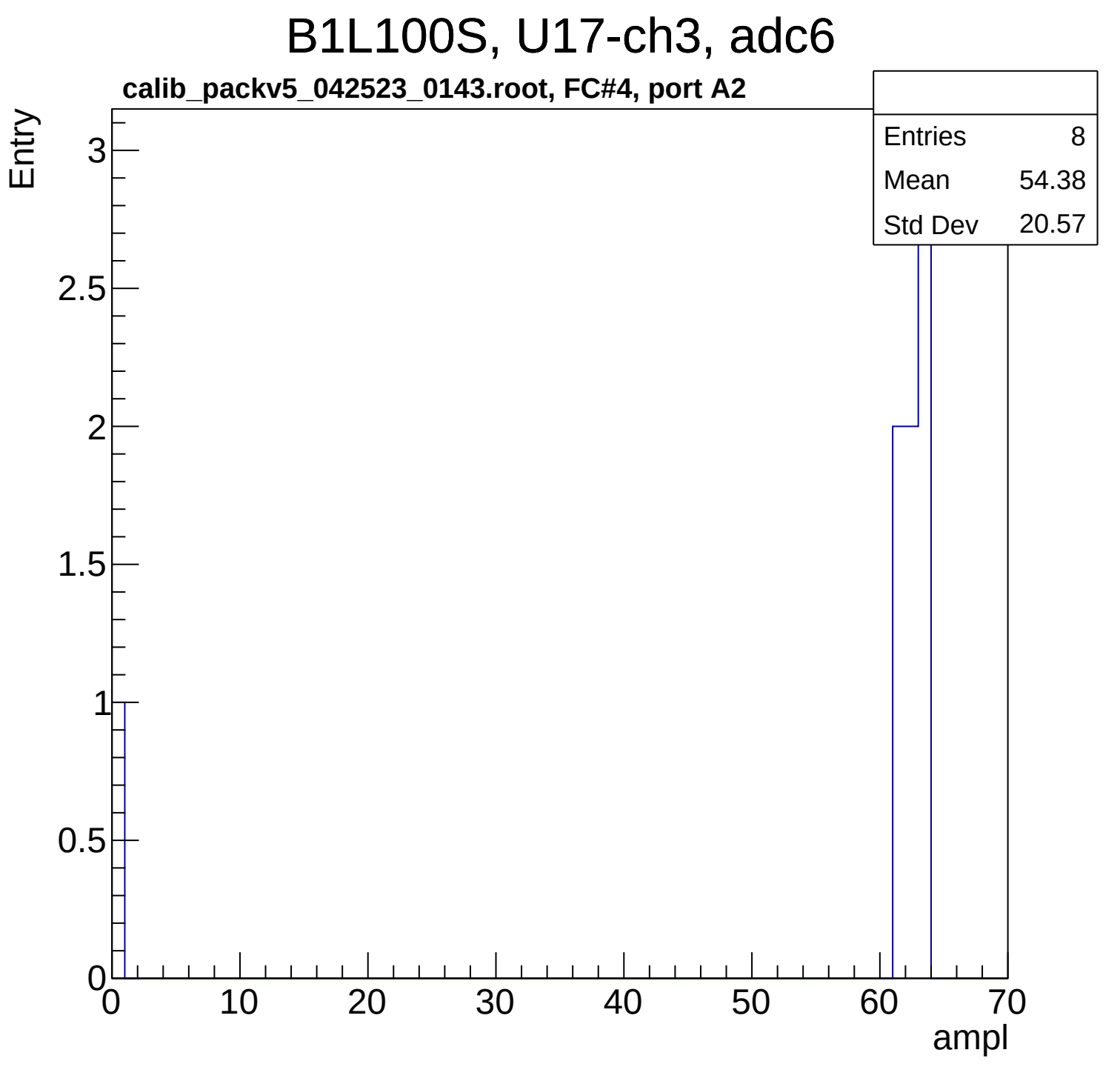
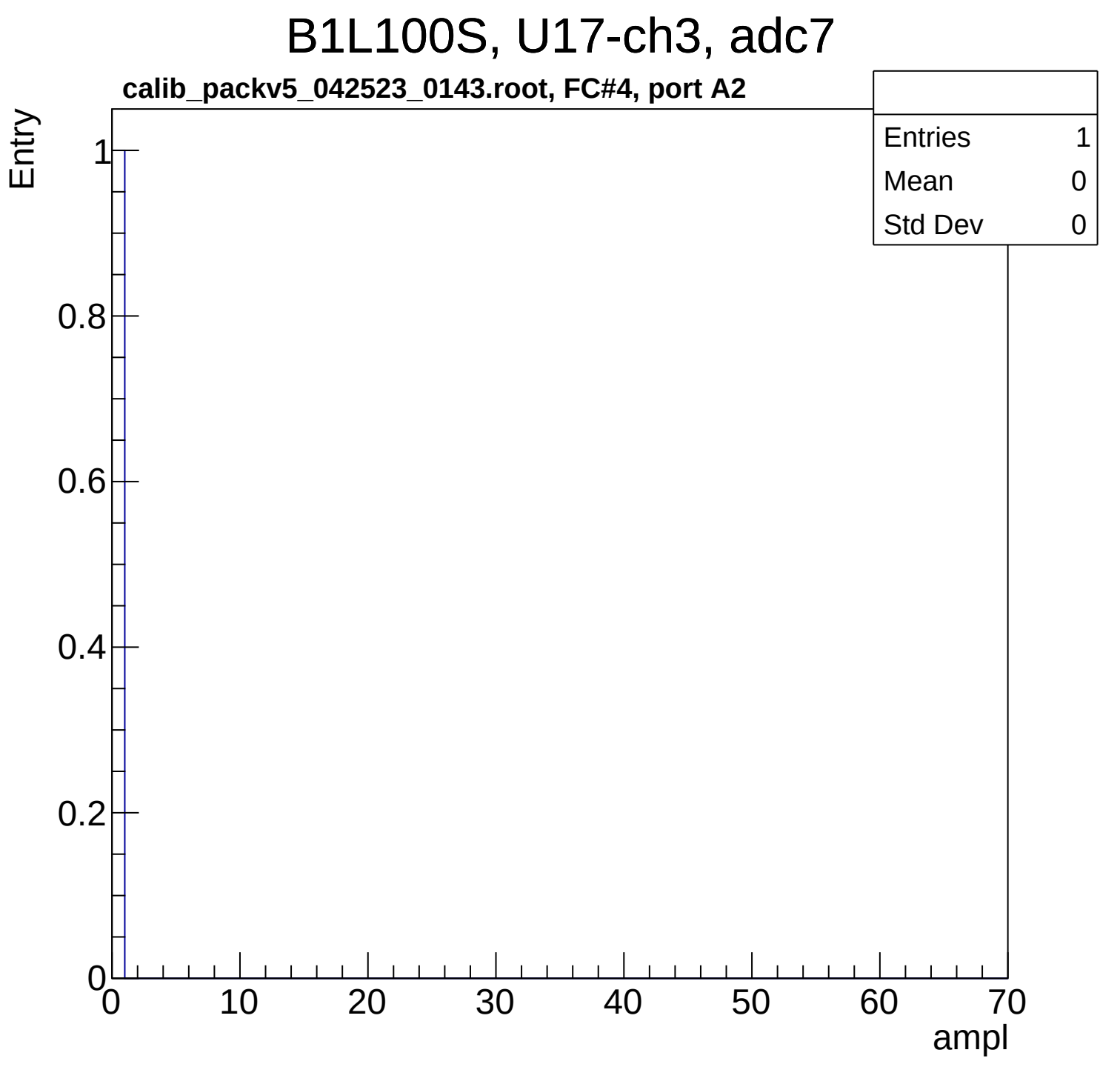

B1L100S, U17-ch3, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 8
Mean 54.38
Std Dev 20.57
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L100S, U17-ch3, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
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10
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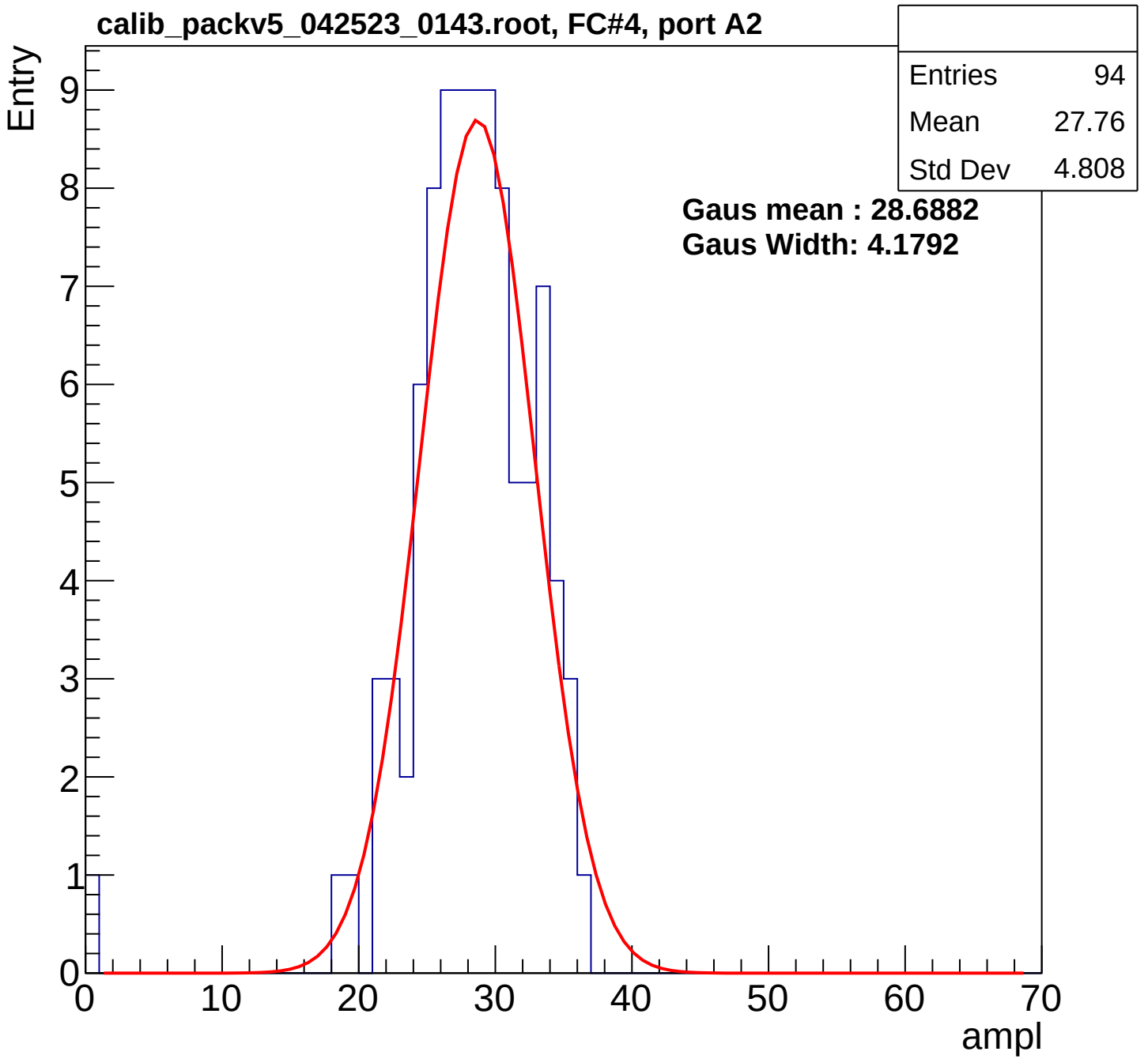
60
70
ampl


B1L100S, U17-ch4, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 94
Mean 27.76
Std Dev 4.808
Gaus mean : 28.6882
Gaus Width: 4.1792
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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60
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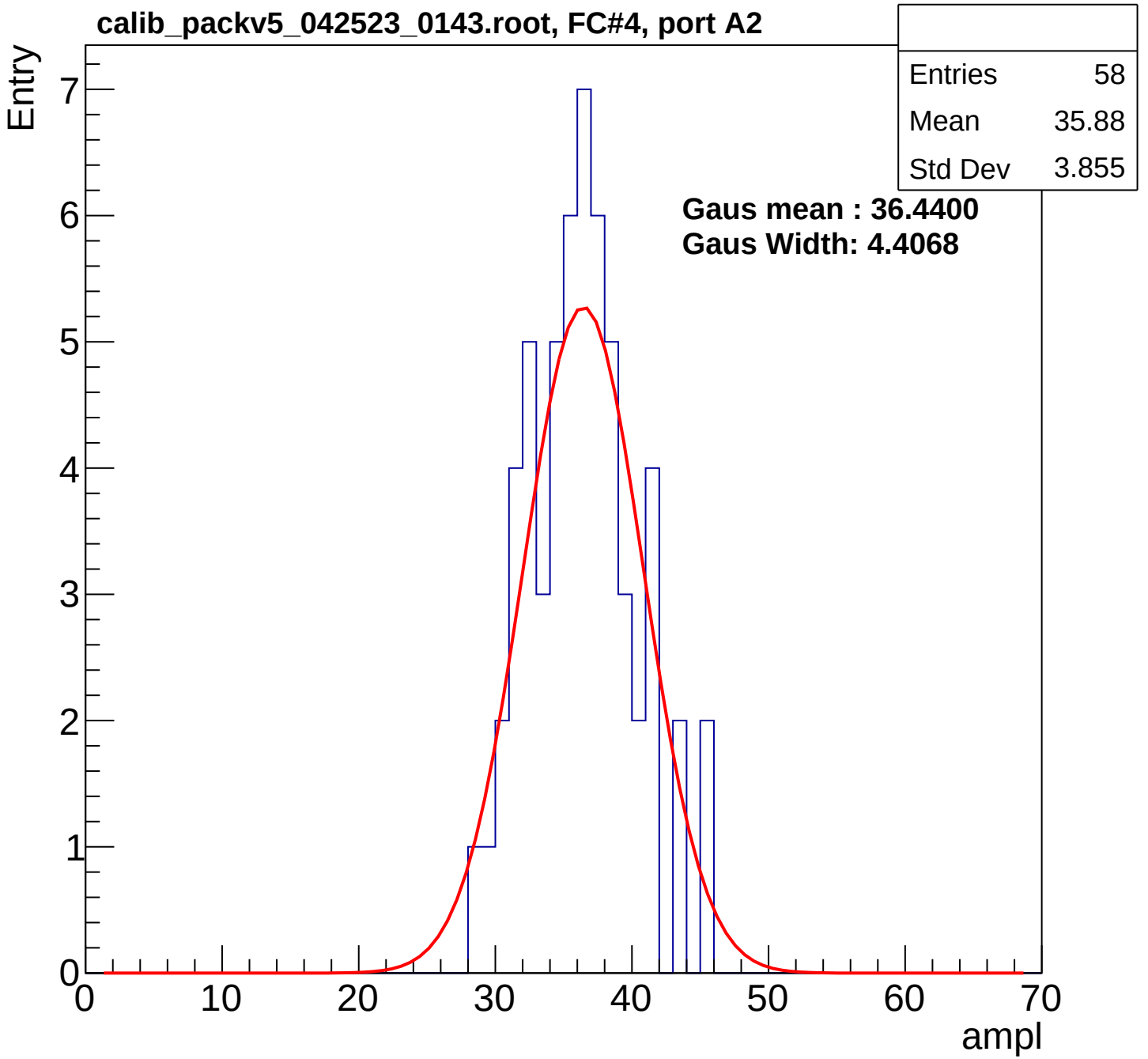
B1L100S, U17-ch4, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 35.88
Std Dev 3.855
Gaus mean : 36.4400
Gaus Width: 4.4068
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
50
60
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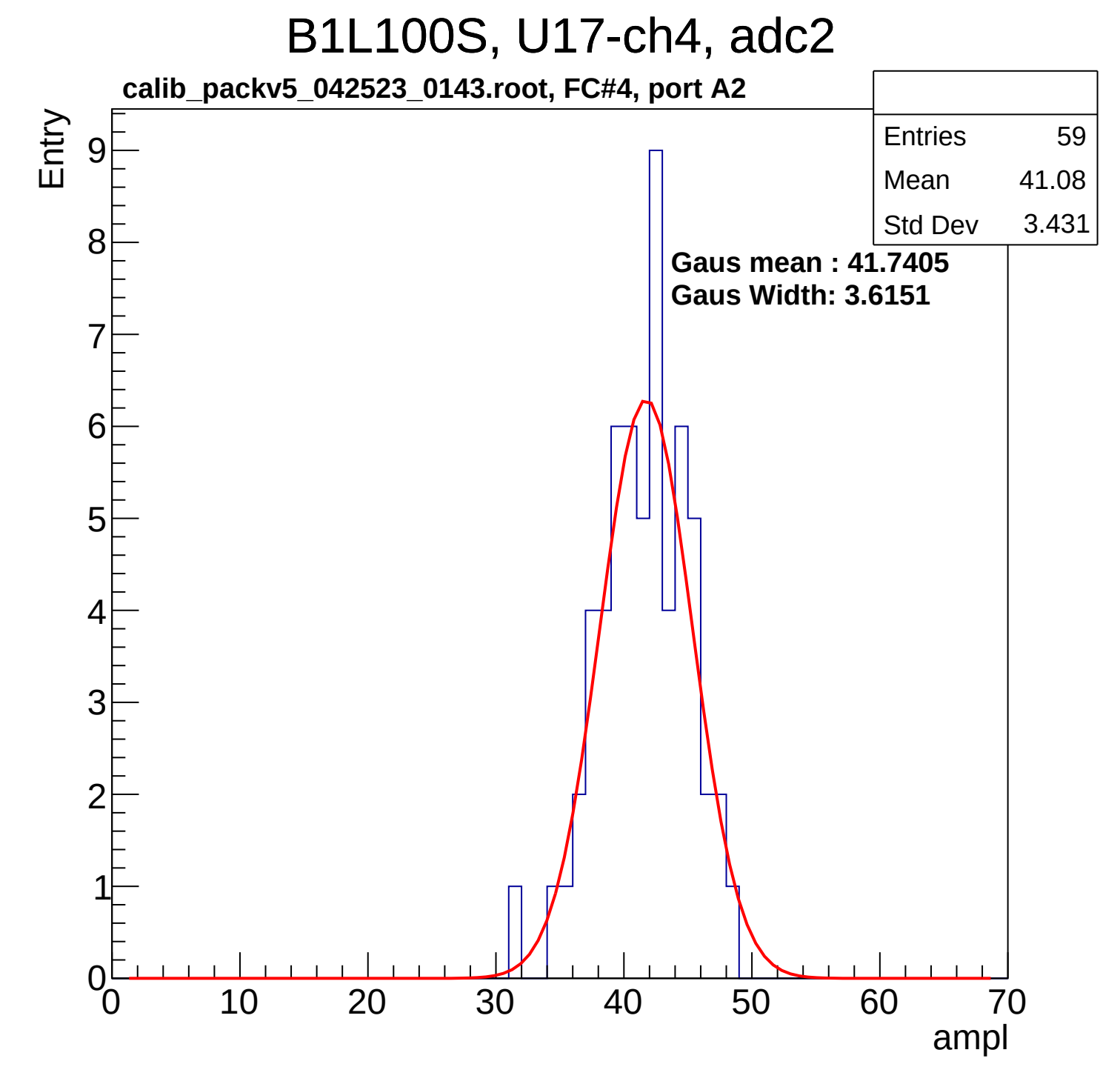
B1L100S, U17-ch4, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 41.08
Std Dev 3.431
Gaus mean : 41.7405
Gaus Width: 3.6151
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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40
50
60
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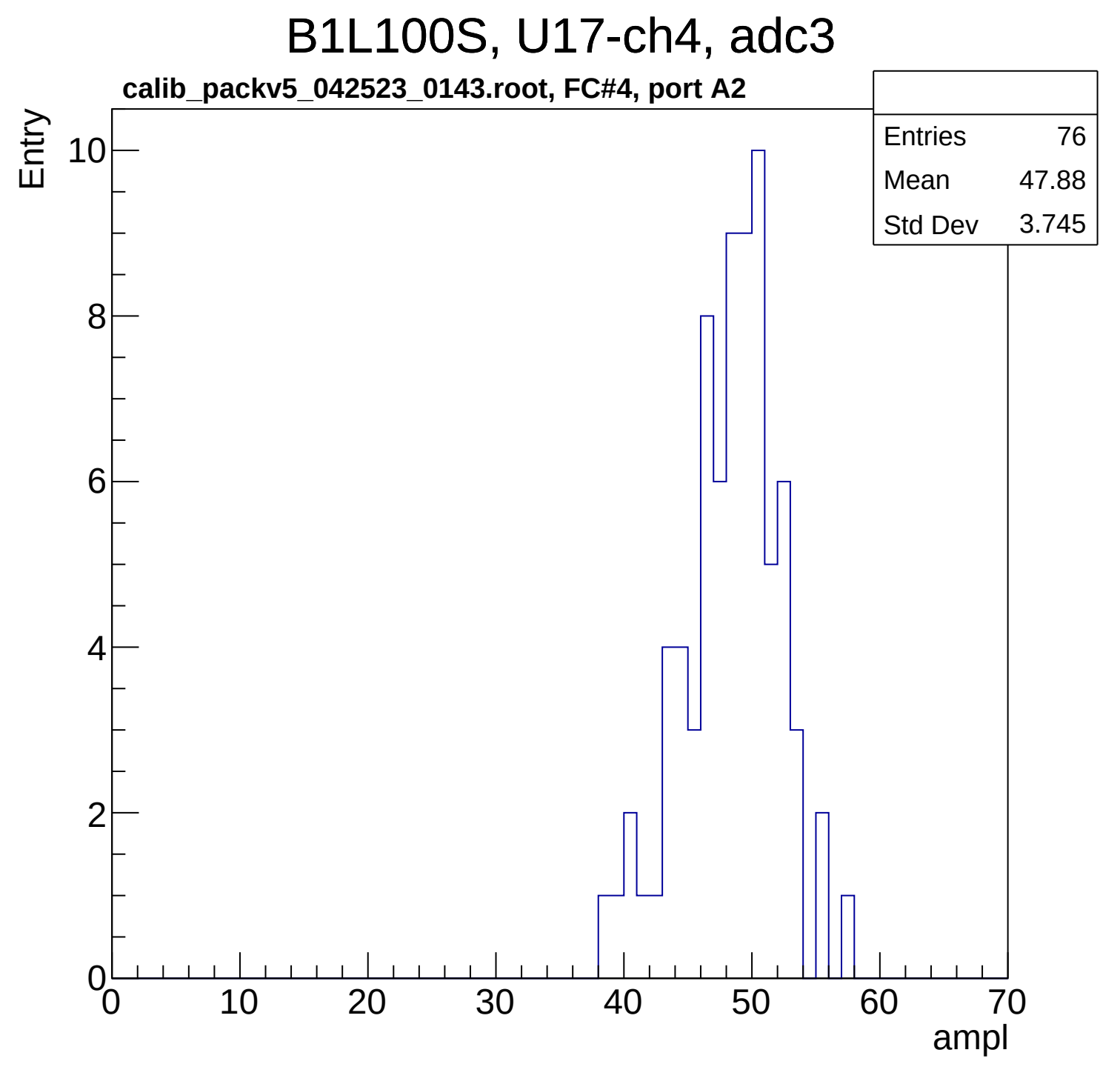
B1L100S, U17-ch4, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 76
Mean 47.88
Std Dev 3.745
Entry
ampl
0
2
4
6
8
10
0
10
20
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40
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60
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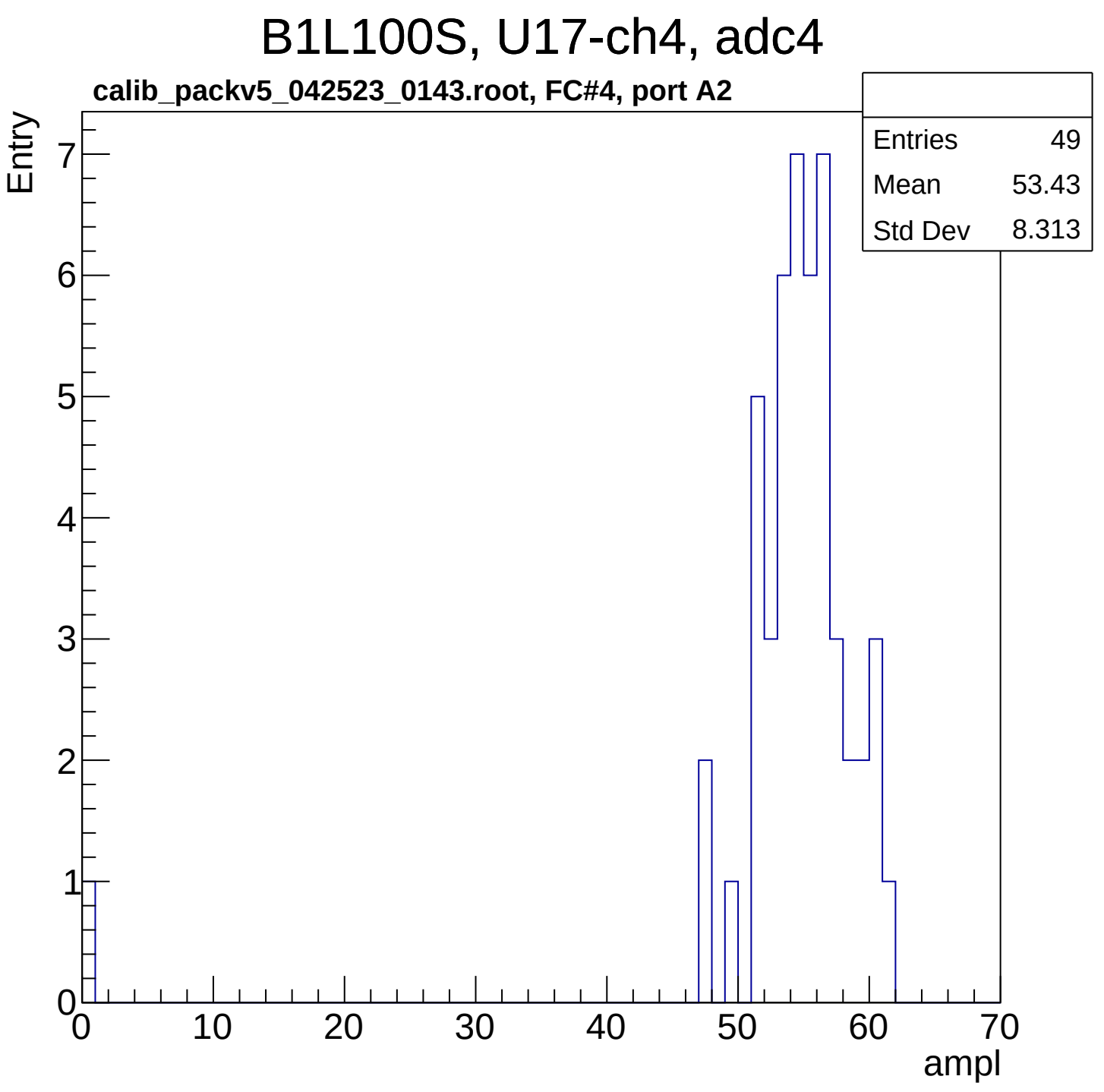
B1L100S, U17-ch4, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 49
Mean 53.43
Std Dev 8.313
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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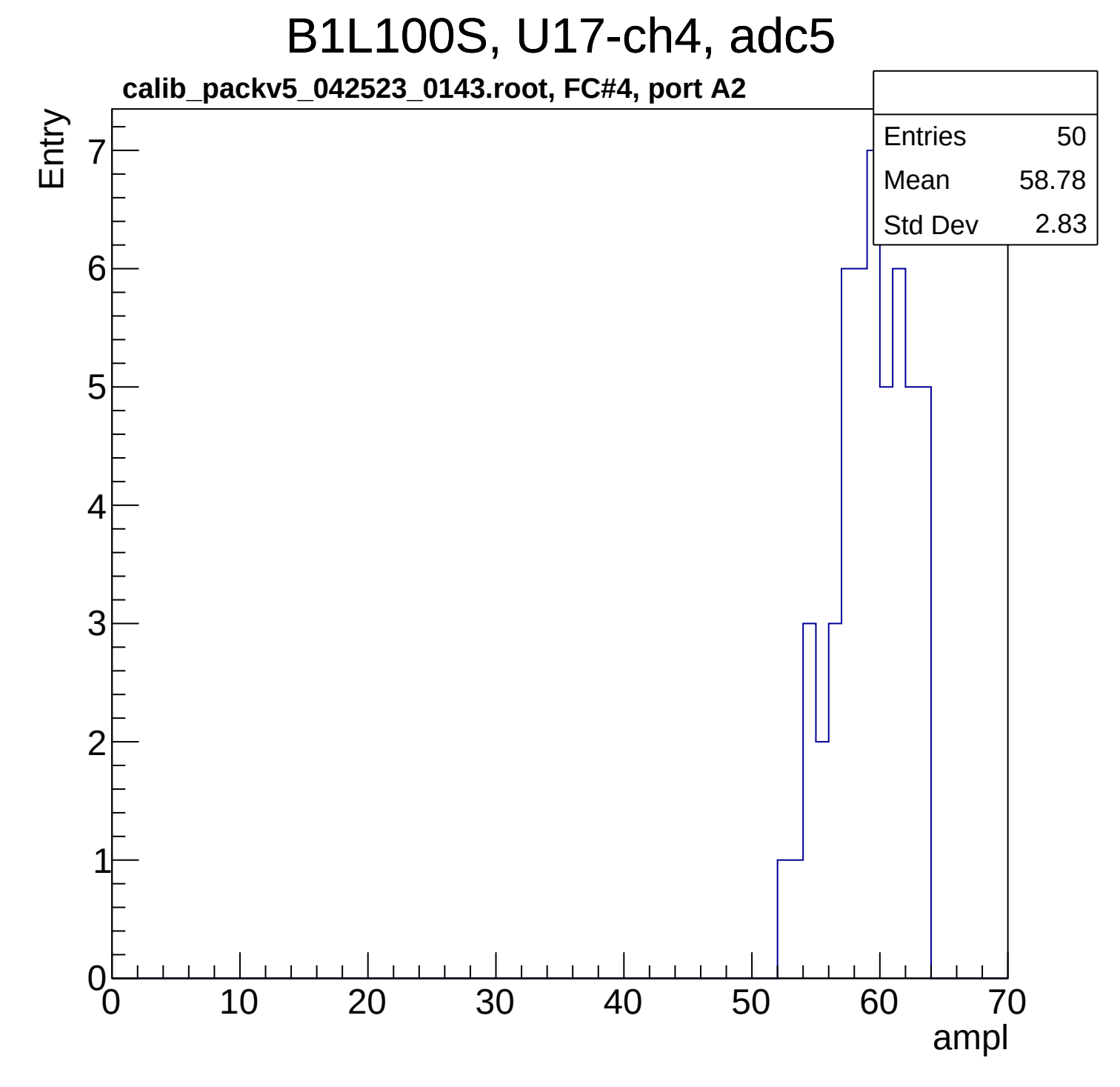
B1L100S, U17-ch4, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 58.78
Std Dev 2.83
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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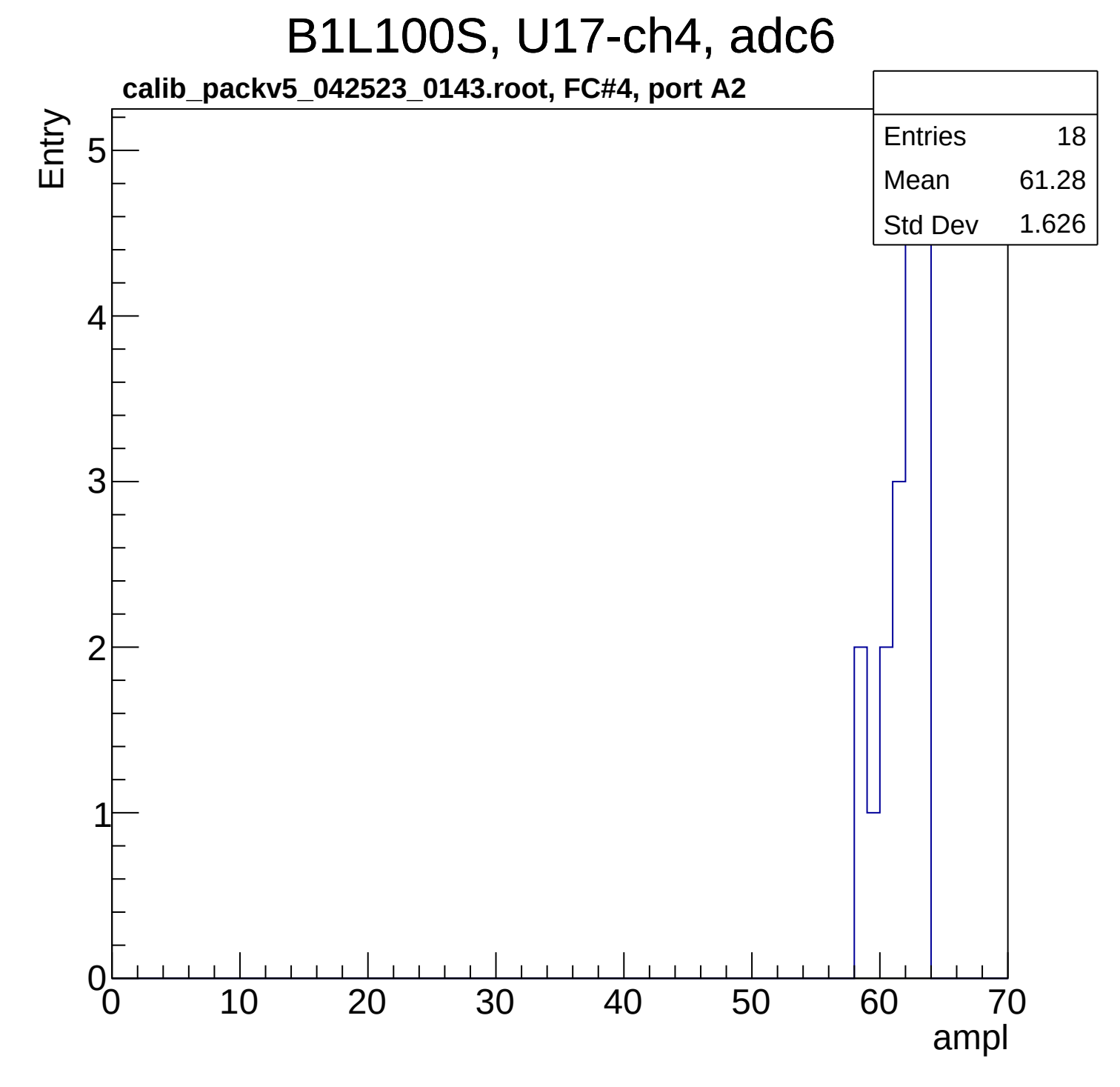
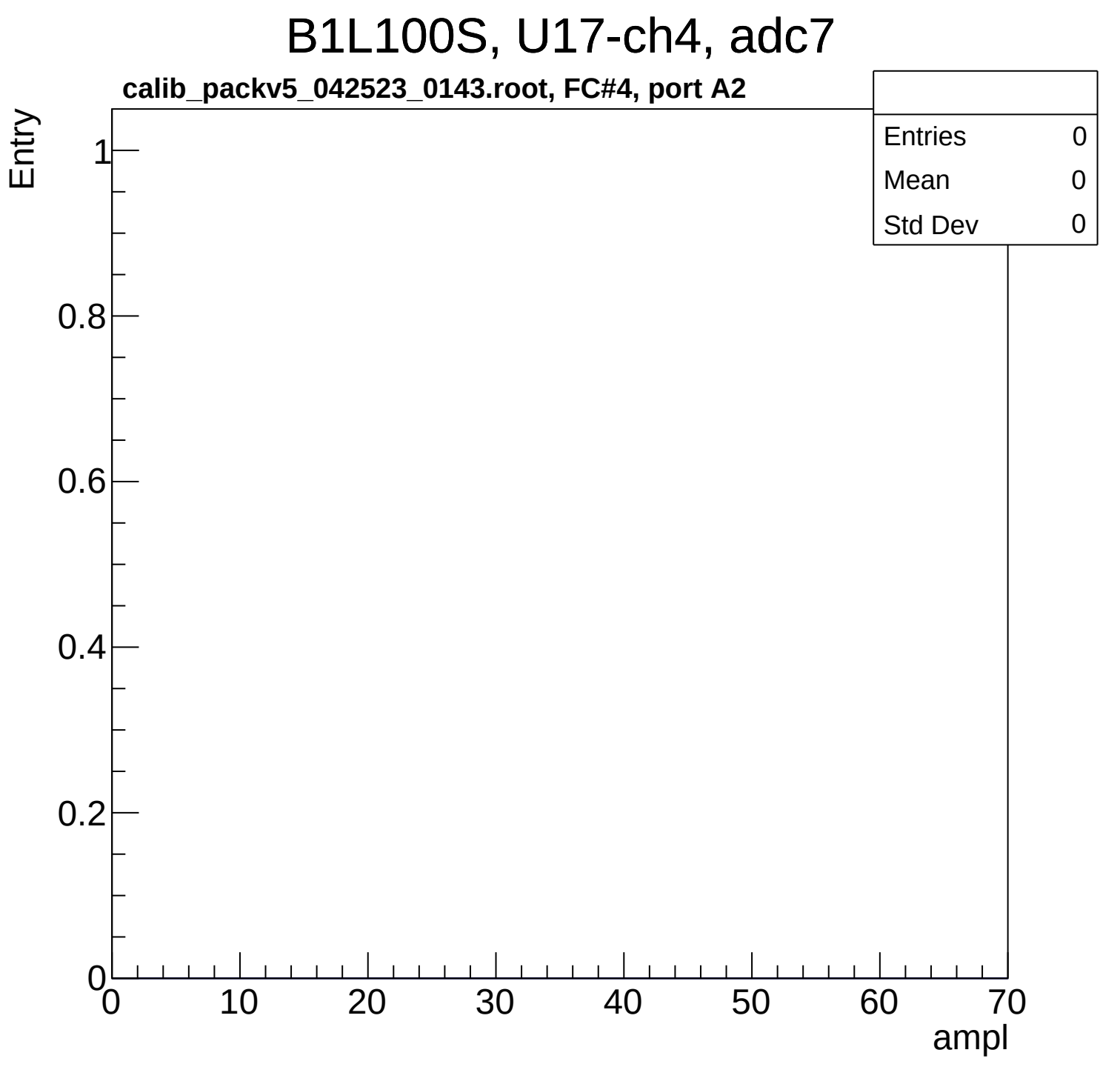

B1L100S, U17-ch4, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 18
Mean 61.28
Std Dev 1.626
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L100S, U17-ch4, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
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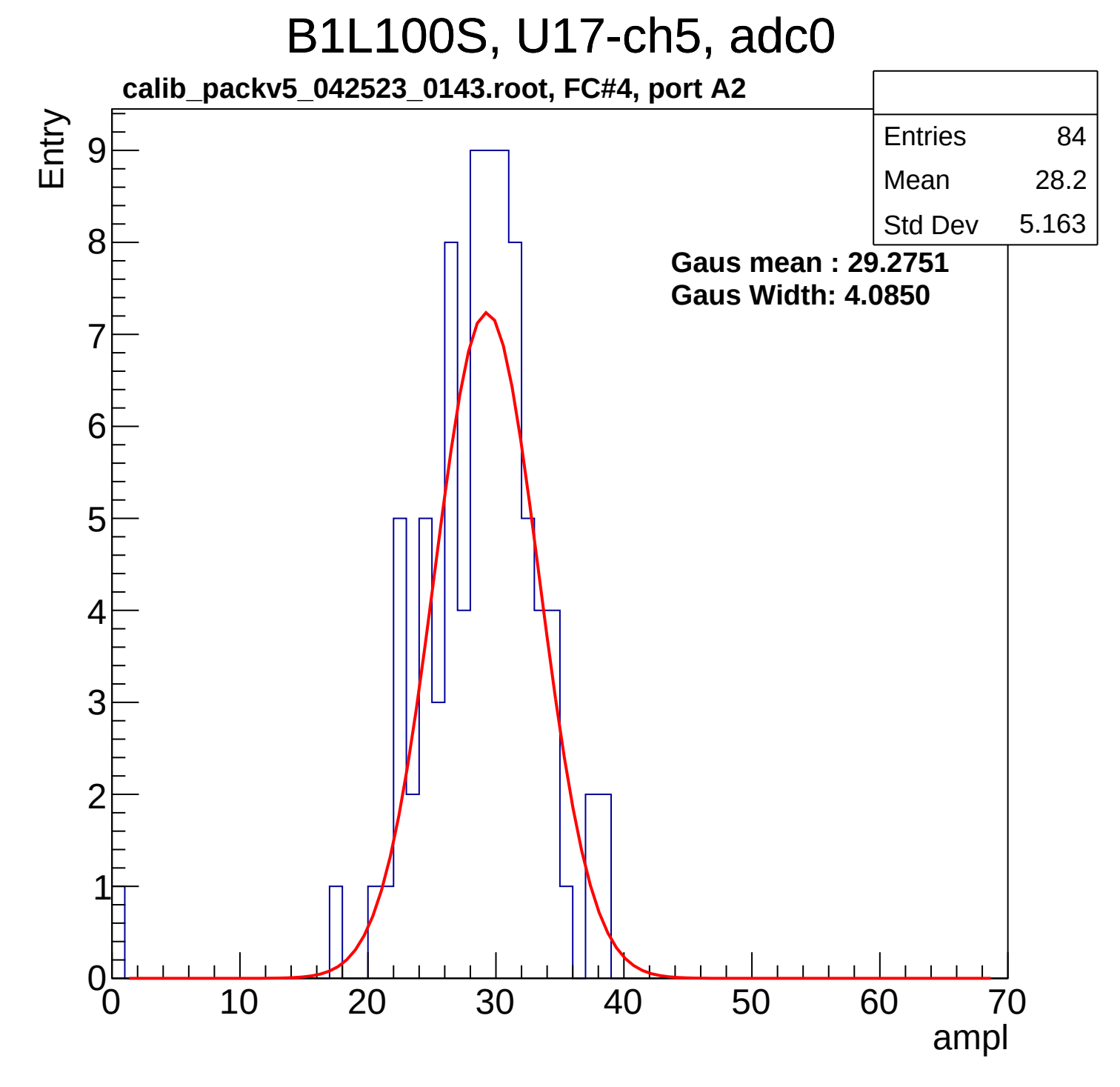
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch5, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 84
Mean 28.2
Std Dev 5.163
Gaus mean : 29.2751
Gaus Width: 4.0850
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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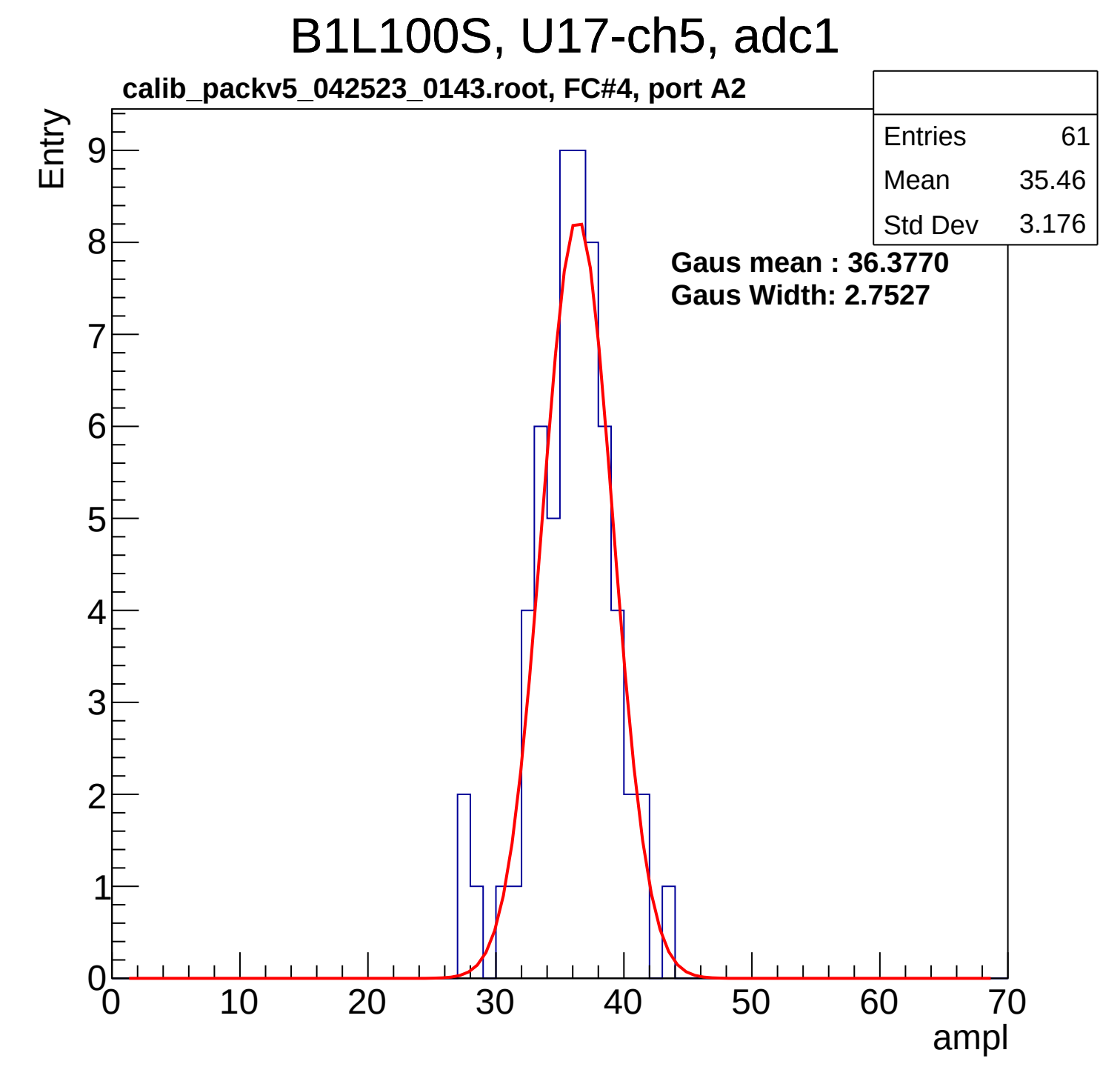
B1L100S, U17-ch5, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 35.46
Std Dev 3.176
Gaus mean : 36.3770
Gaus Width: 2.7527
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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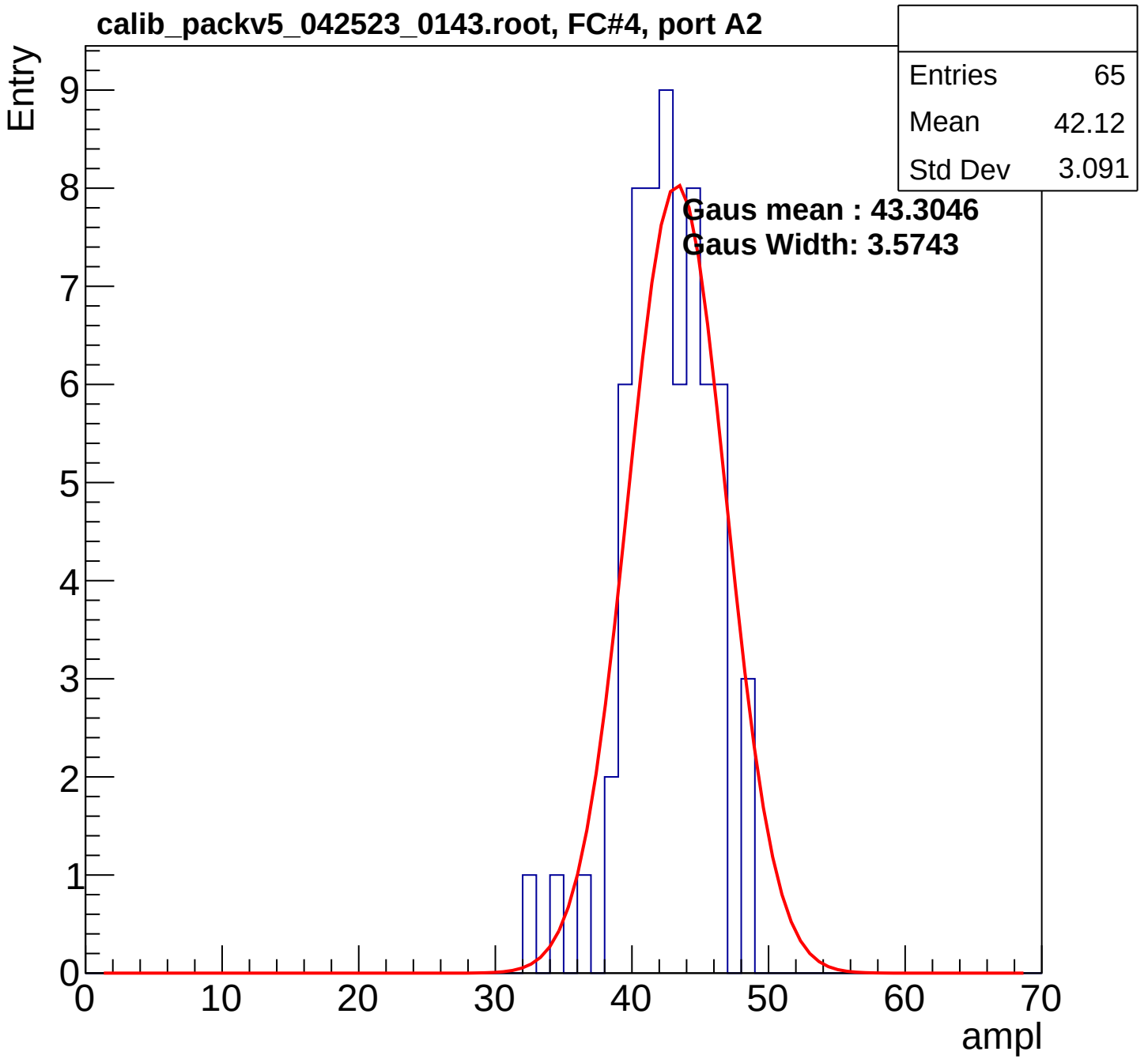
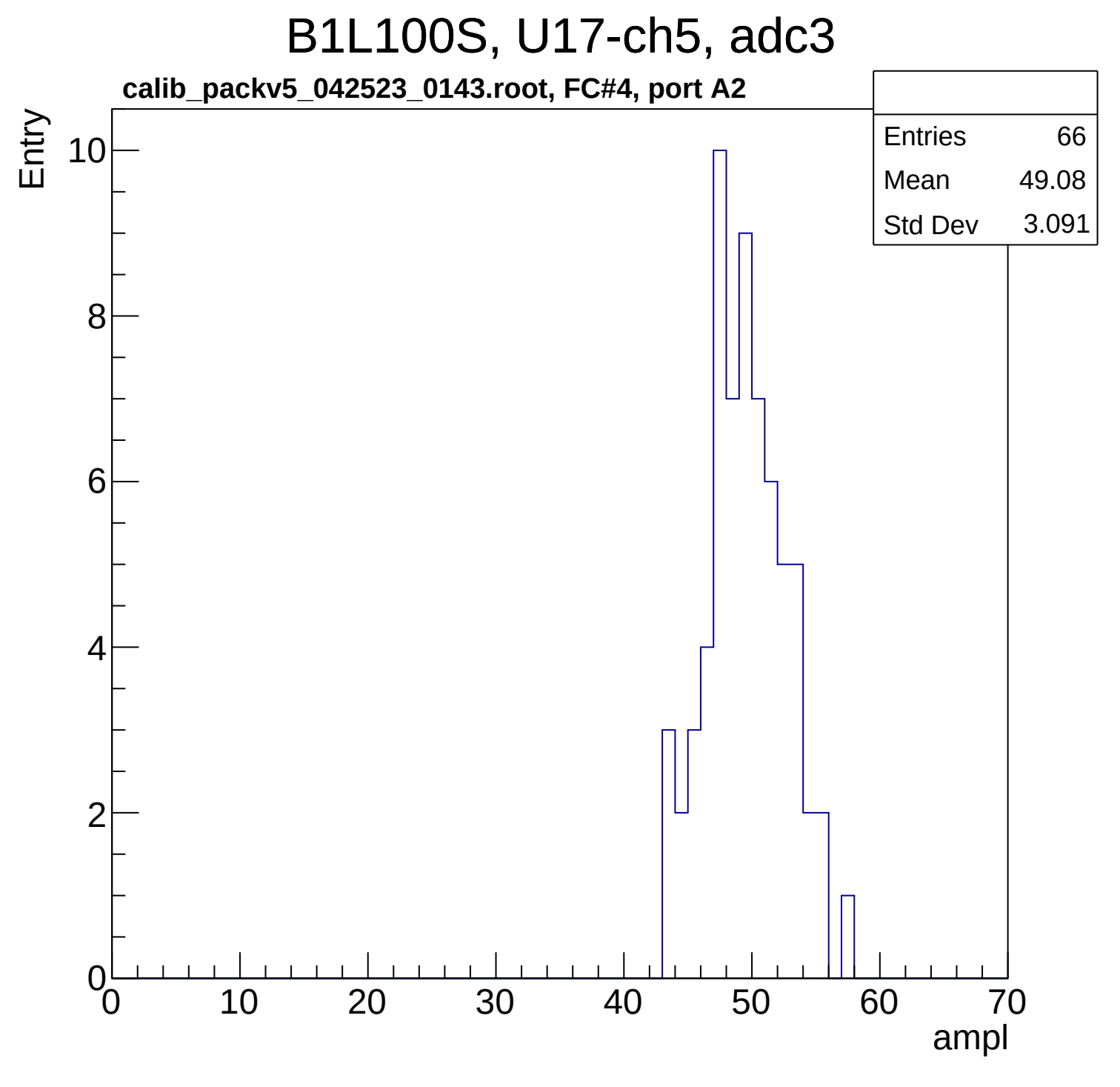
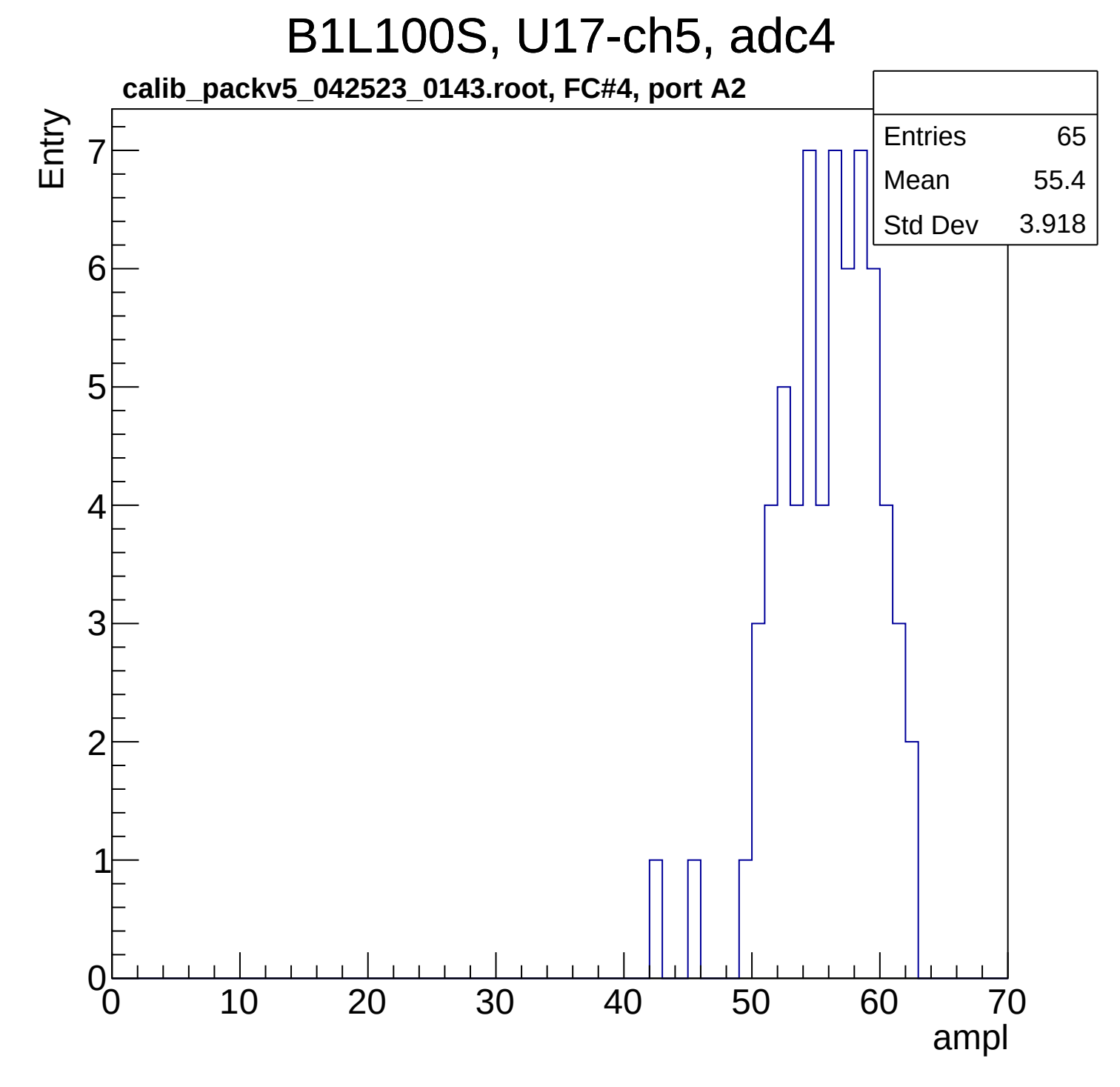
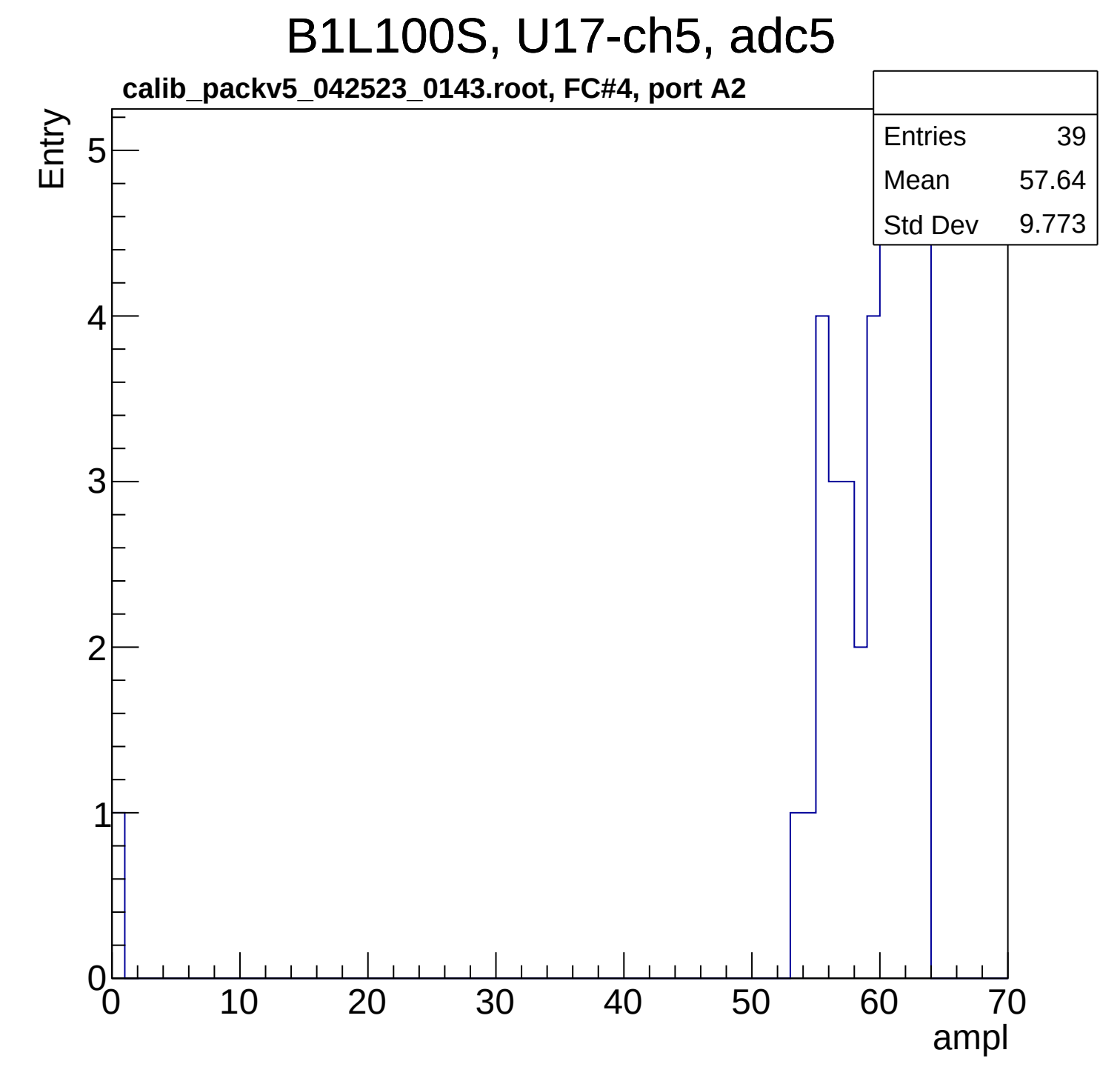
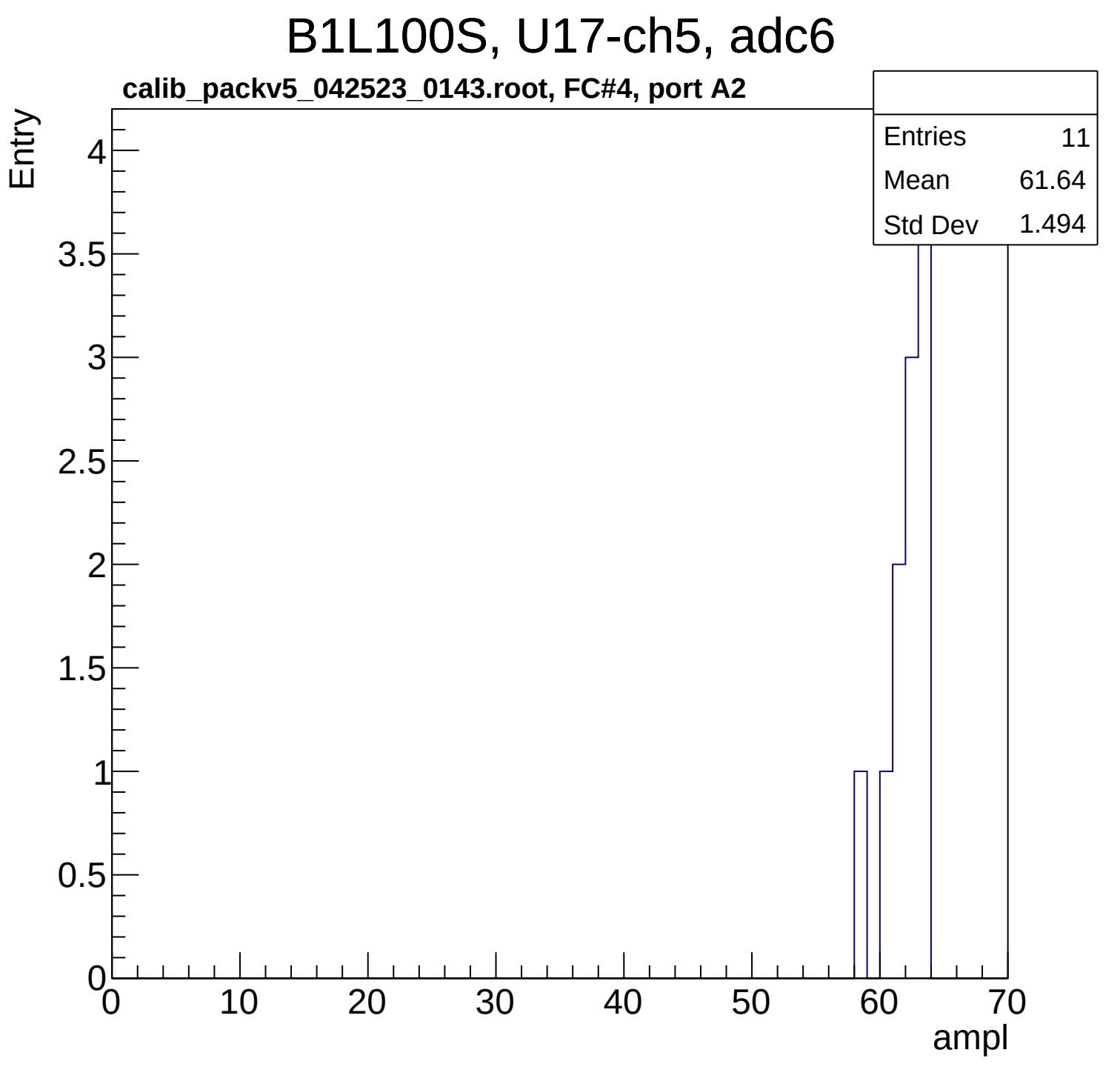

B1L100S, U17-ch5, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 42.12
Std Dev 3.091
Gaus mean : 43.3046
Gaus Width: 3.5743
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch5, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 49.08
Std Dev 3.091
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U17-ch5, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 55.4
Std Dev 3.918
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U17-ch5, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 39
Mean 57.64
Std Dev 9.773
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L100S, U17-ch5, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 11
Mean 61.64
Std Dev 1.494
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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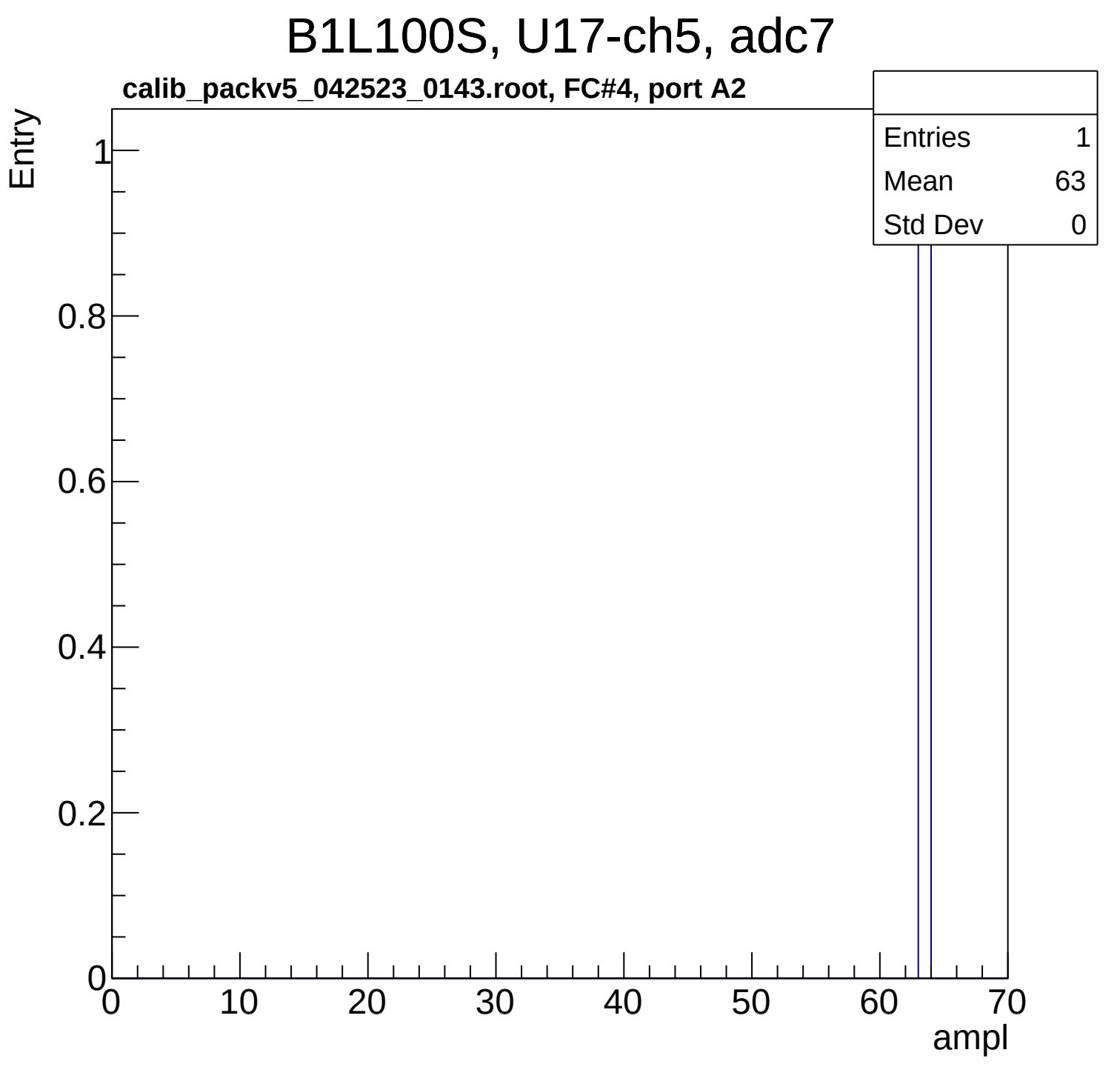
40
50
60
70


B1L100S, U17-ch5, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 63
Std Dev 0
Entry
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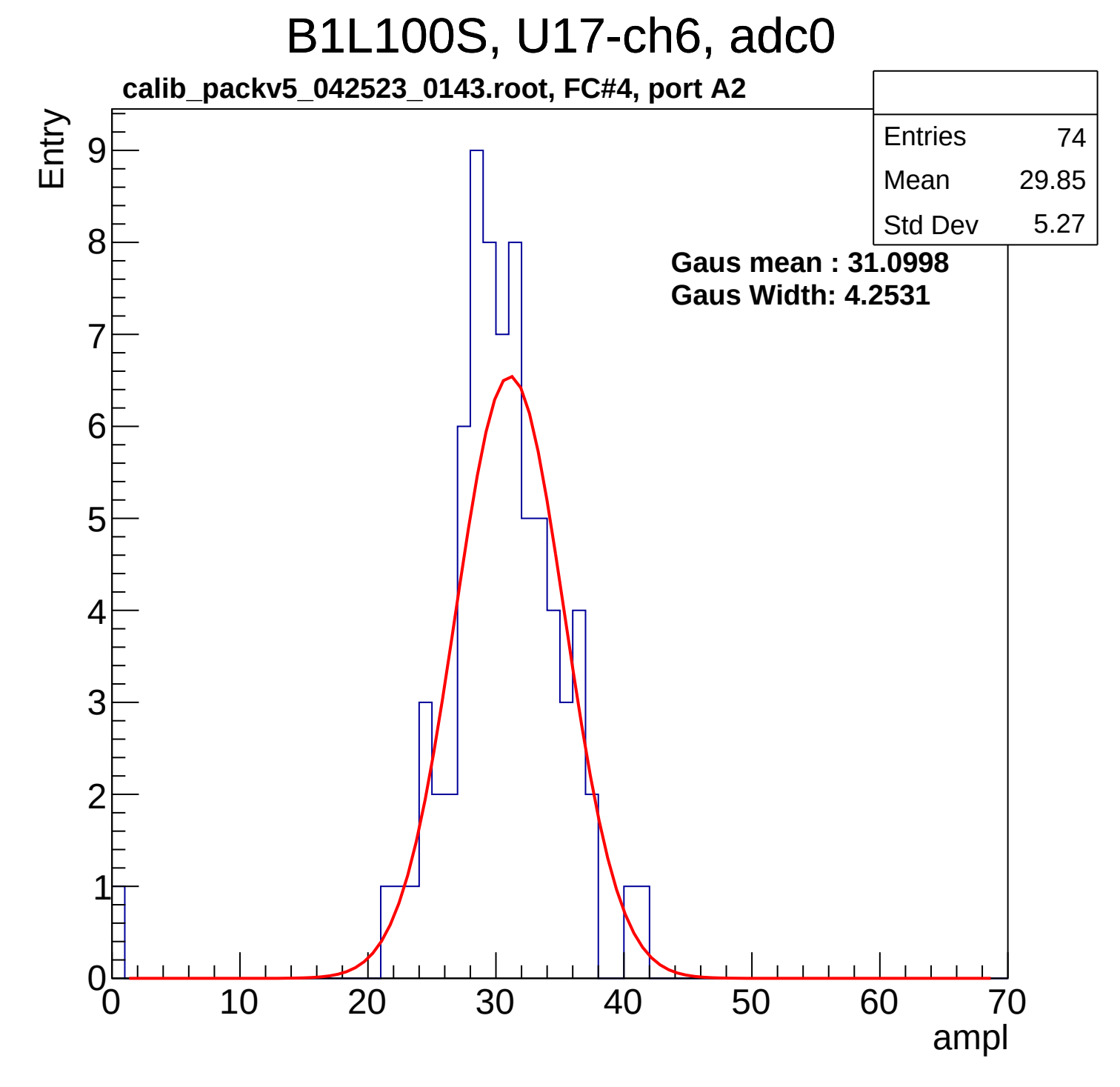
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch6, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 74
Mean 29.85
Std Dev 5.27
Gaus mean : 31.0998
Gaus Width: 4.2531
Entry
ampl
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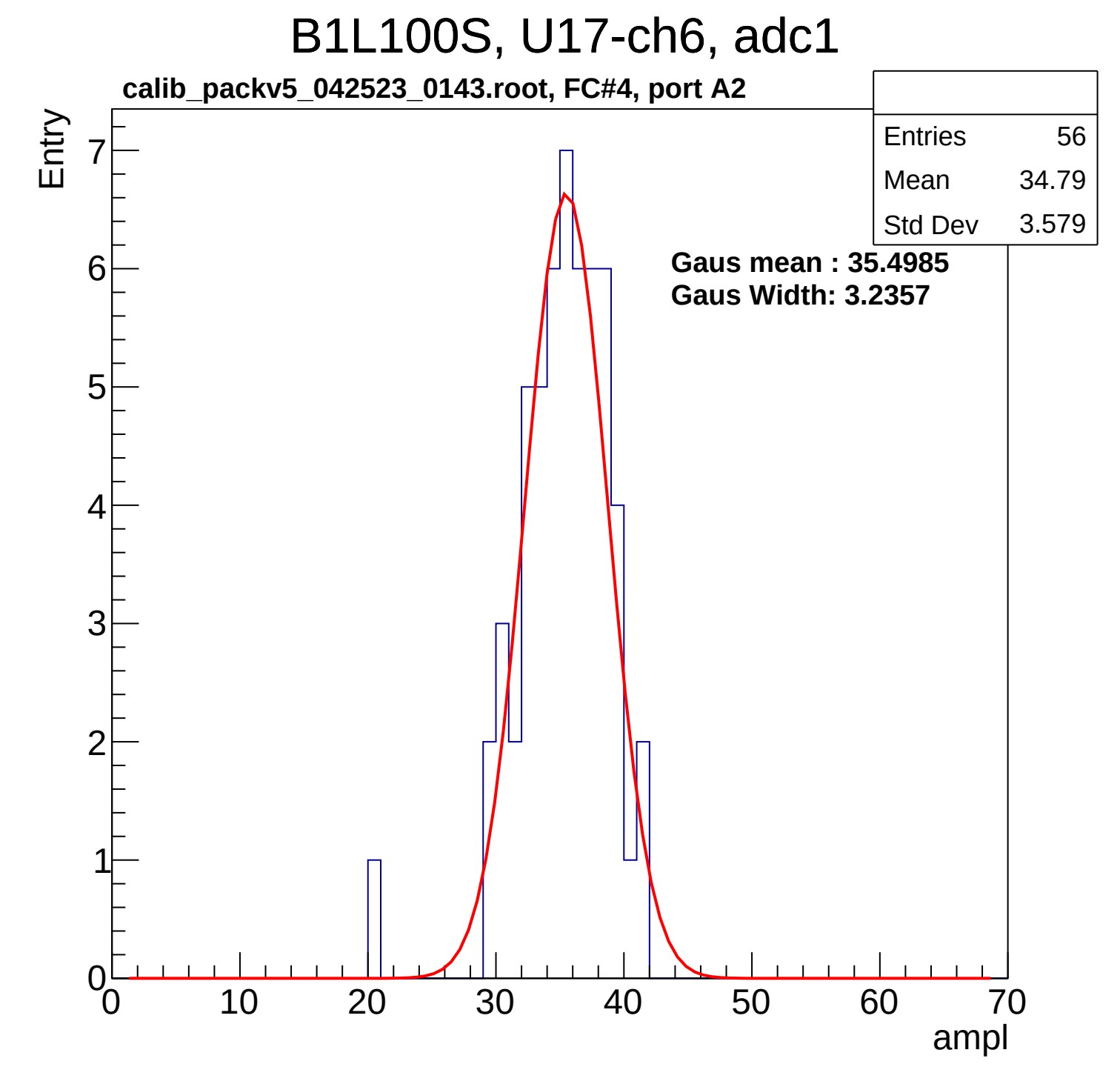
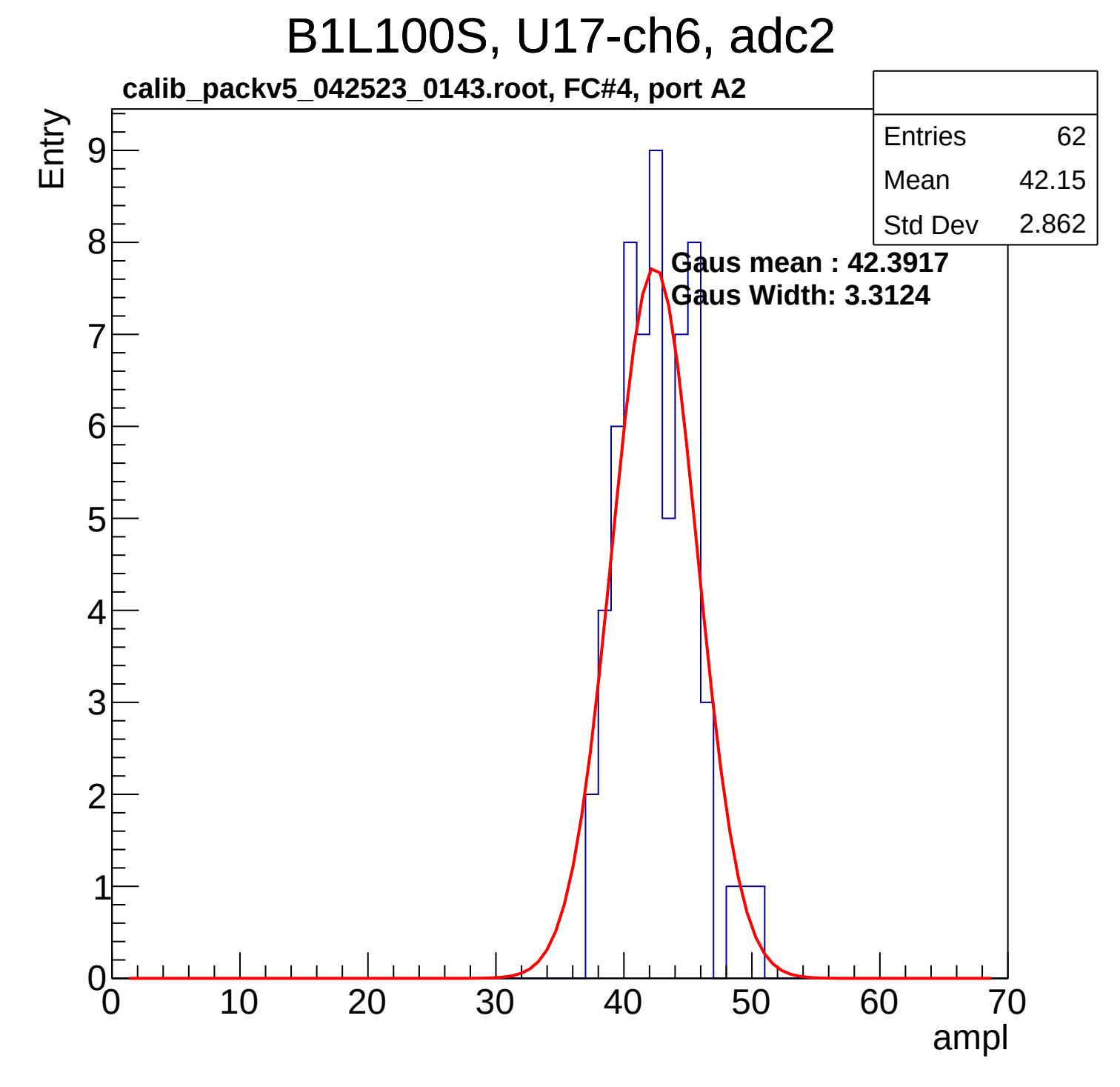
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch6, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 34.79
Std Dev 3.579
Gaus mean : 35.4985
Gaus Width: 3.2357
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U17-ch6, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 42.15
Std Dev 2.862
Gaus mean : 42.3917
Gaus Width: 3.3124
Entry
ampl
0
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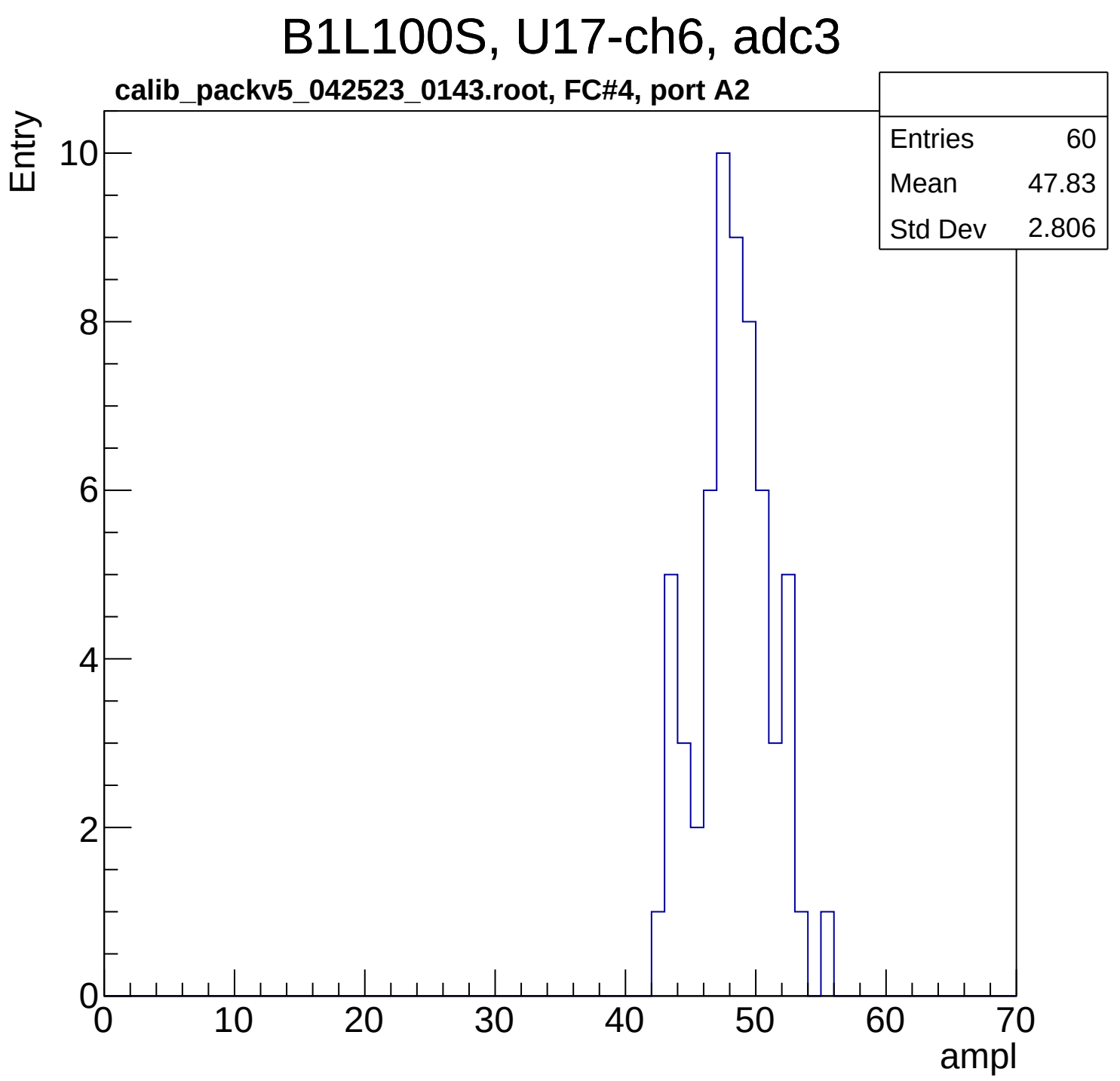
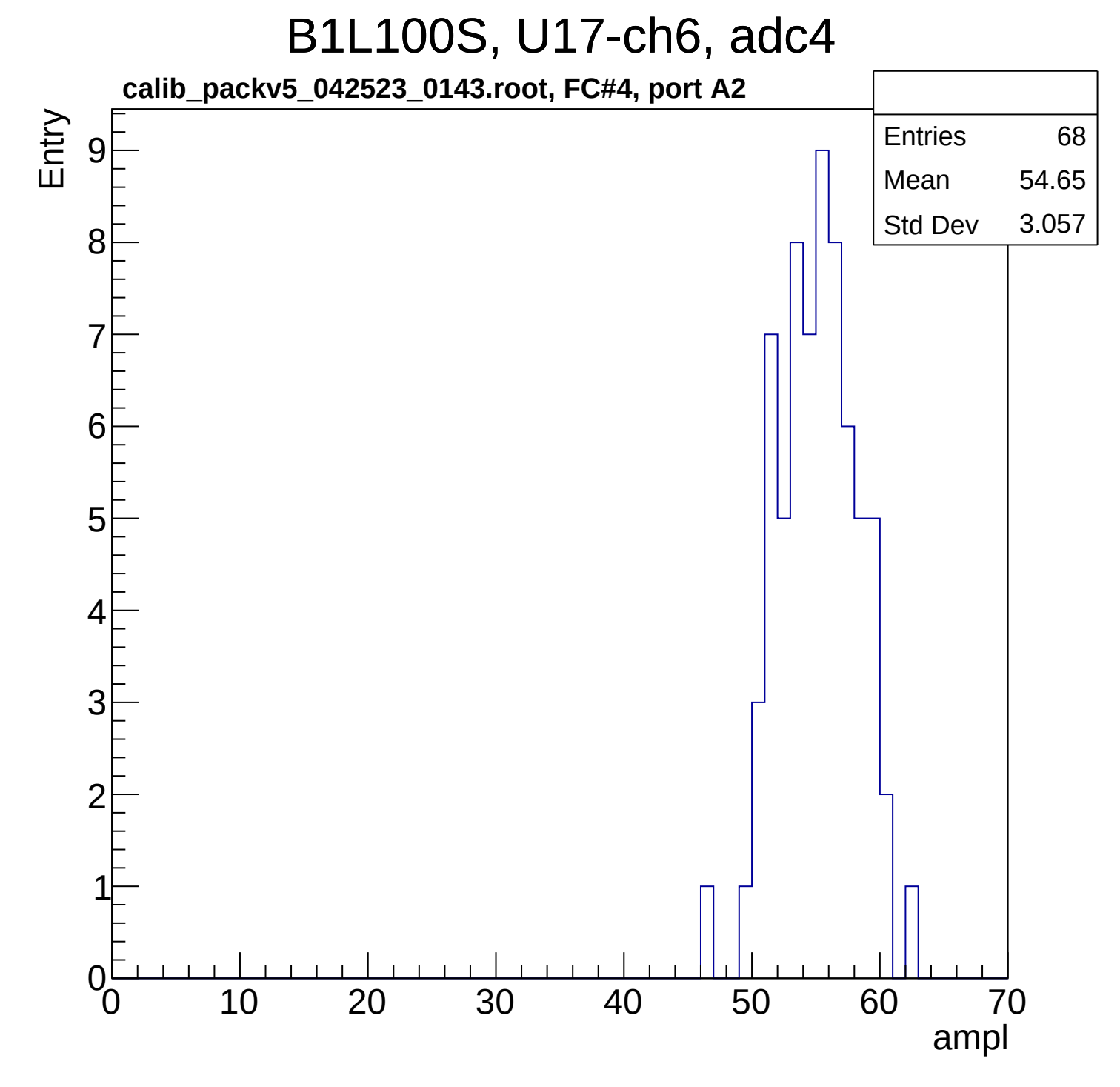
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch6, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 47.83
Std Dev 2.806
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch6, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 54.65
Std Dev 3.057
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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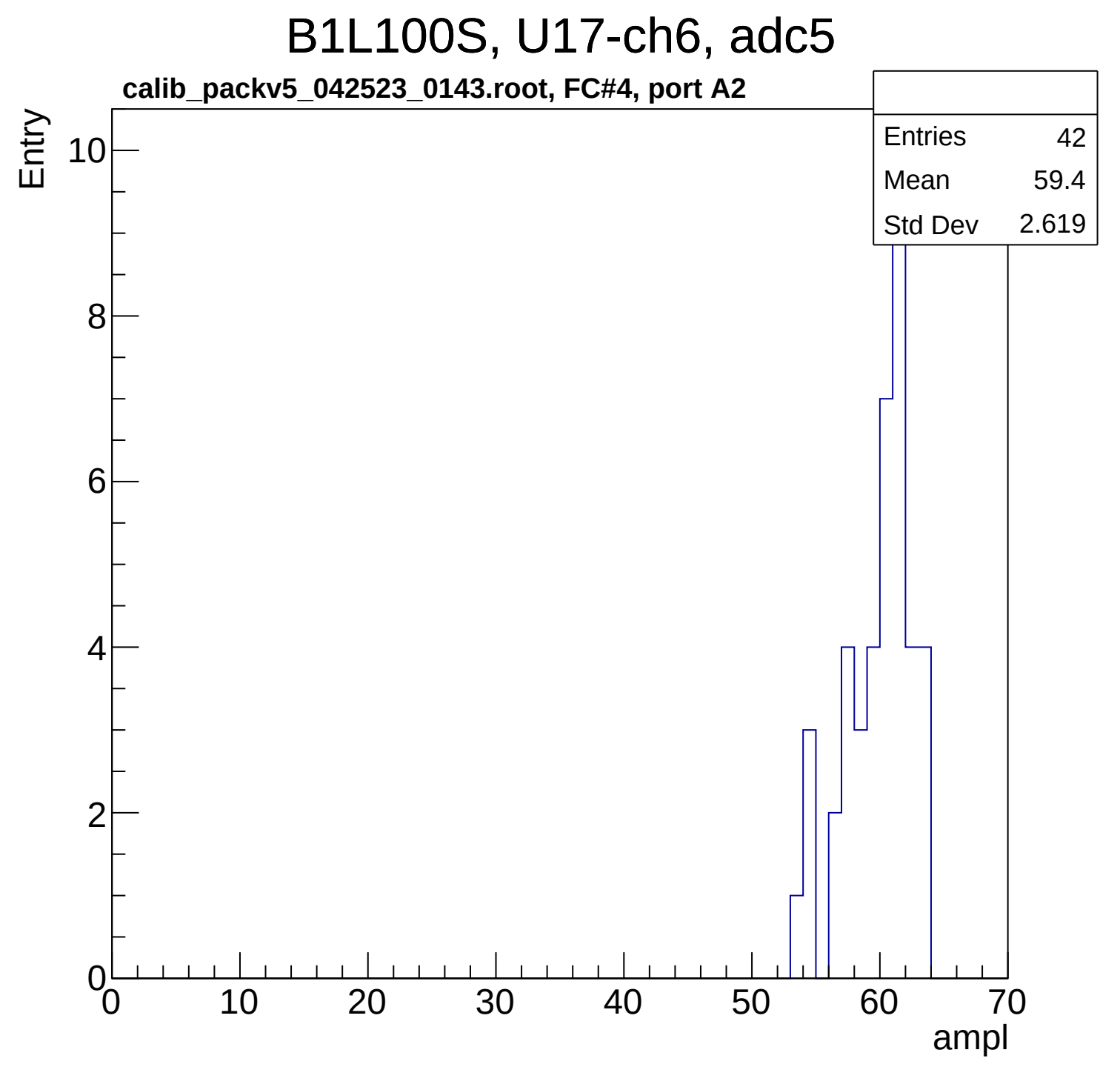
40
50
60
70


B1L100S, U17-ch6, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 42
Mean 59.4
Std Dev 2.619
Entry
ampl
0
2
4
6
8
10
0
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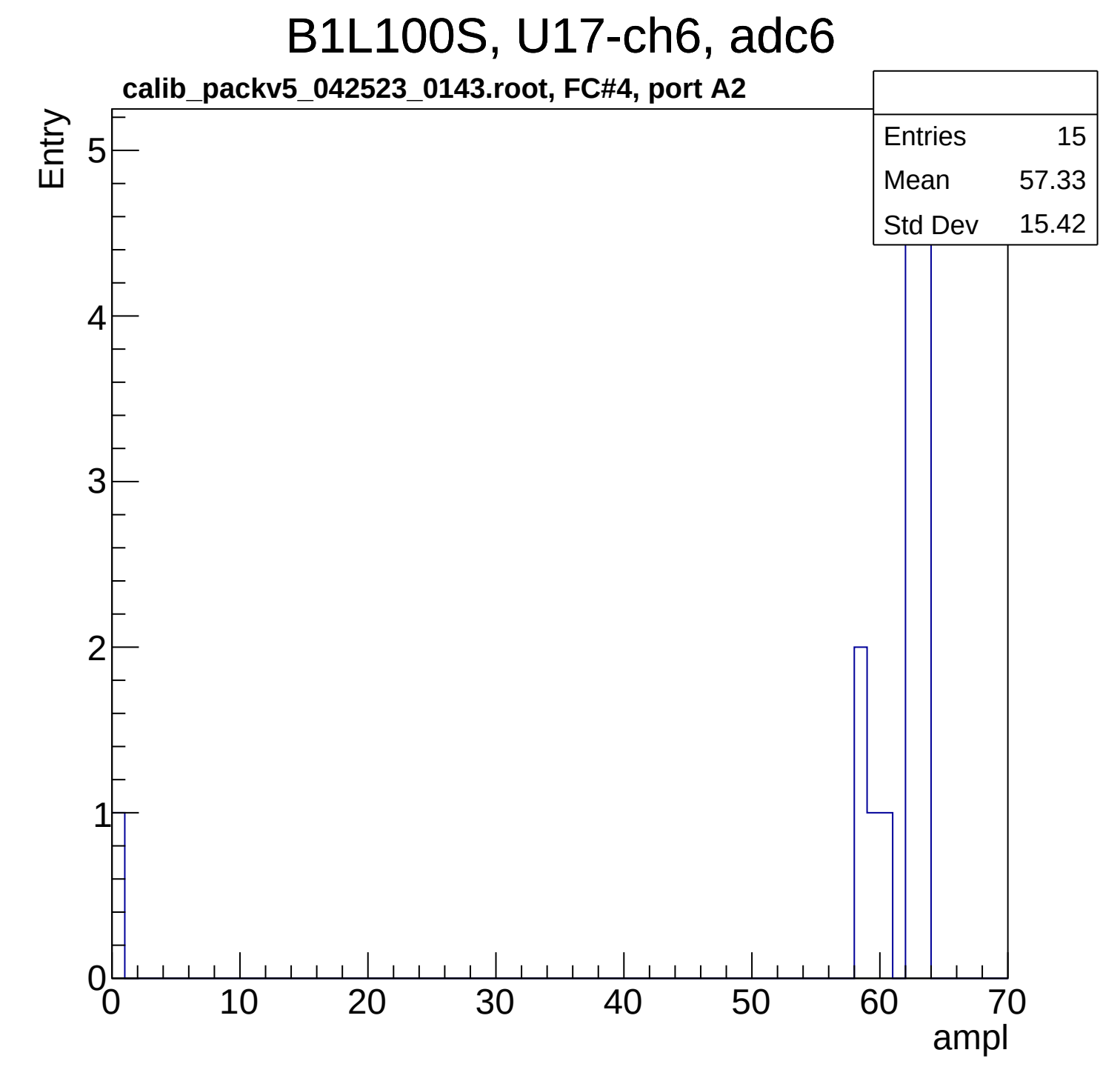
20
30
40
50
60
70


B1L100S, U17-ch6, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 15
Mean 57.33
Std Dev 15.42
Entry
ampl
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4
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0
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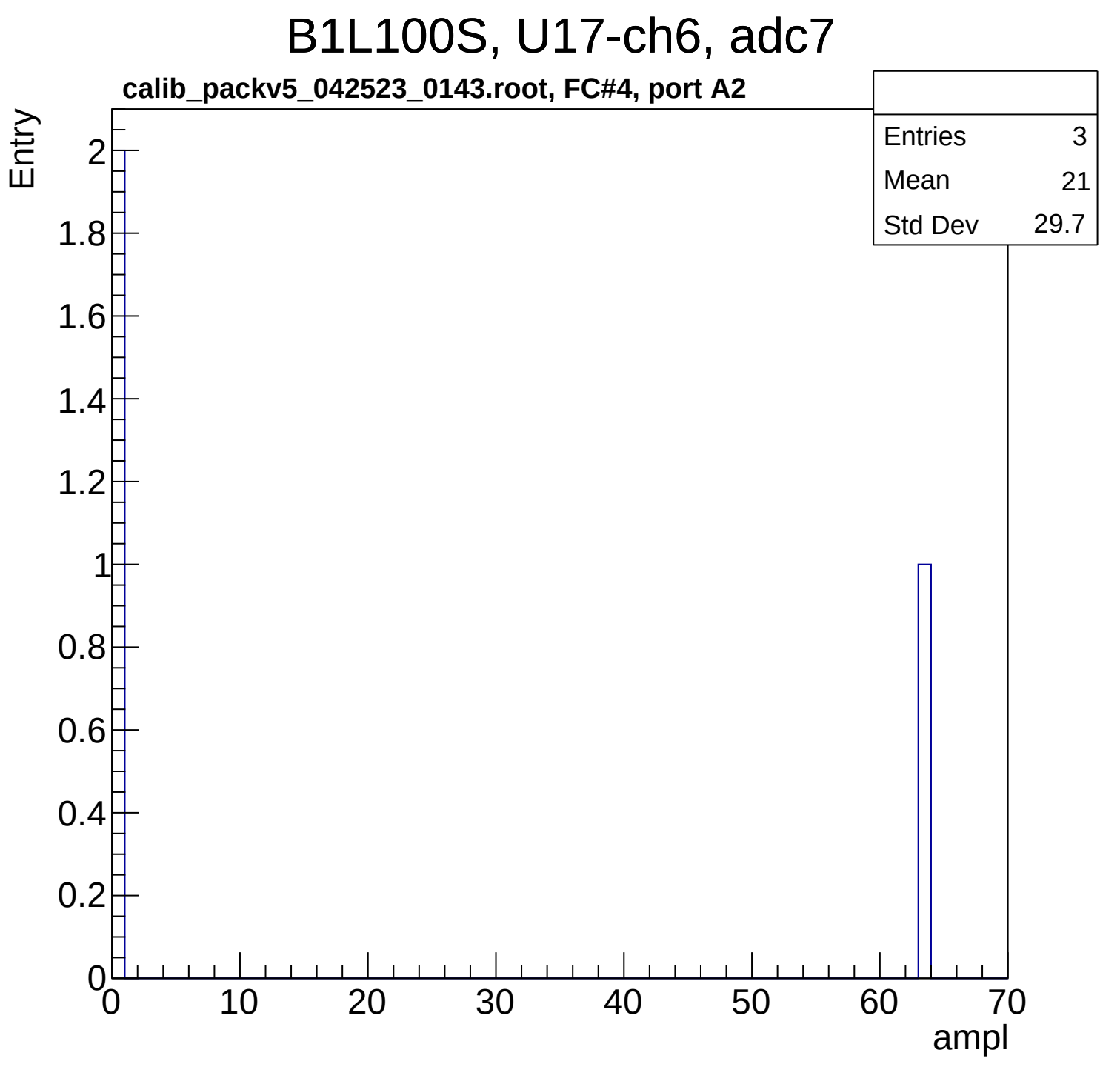
50
60
70


B1L100S, U17-ch6, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 21
Std Dev 29.7
Entry
ampl
0
0.2
0.4
0.6
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1.2
1.4
1.6
1.8
2
0
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20
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60
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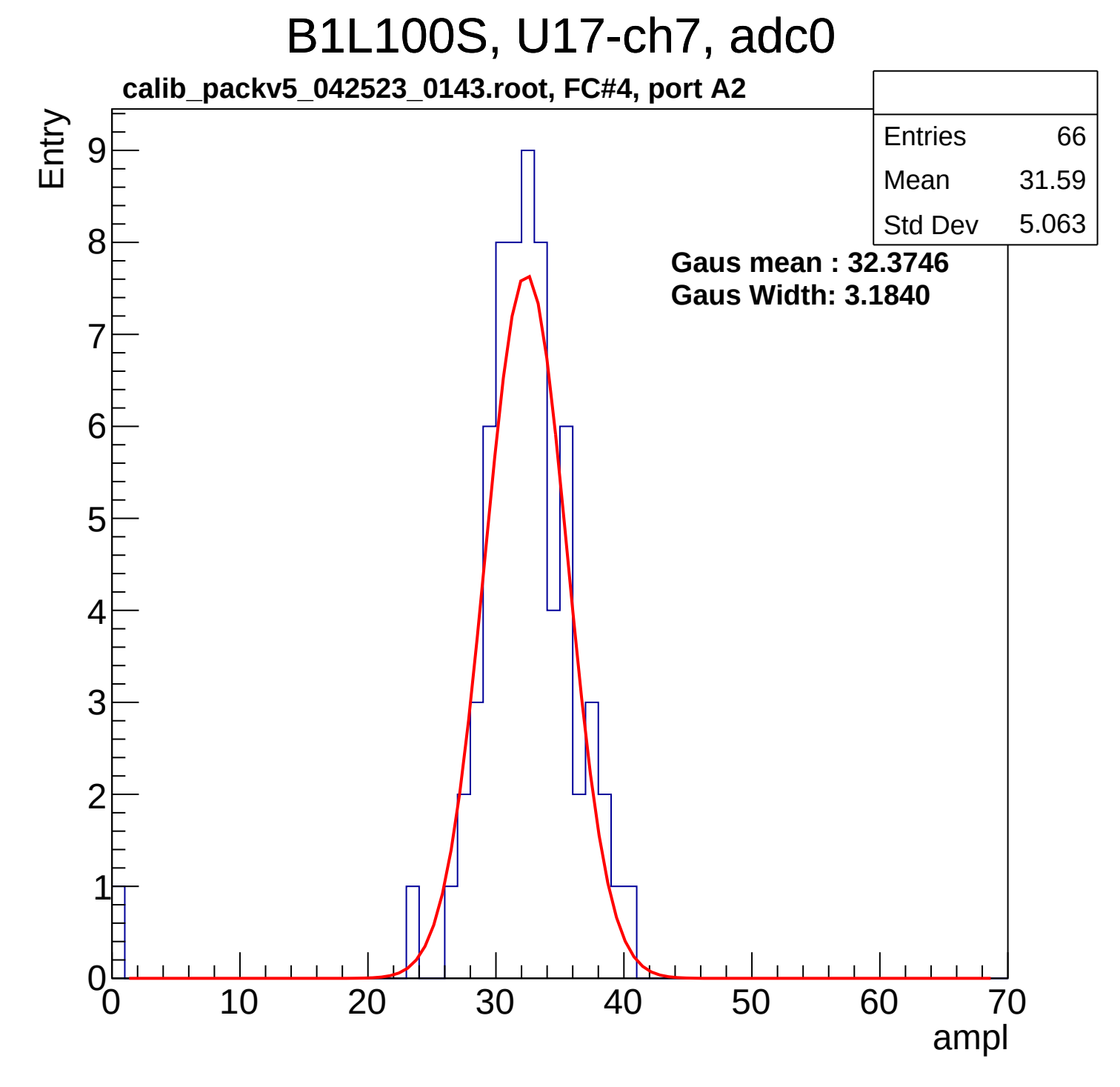
B1L100S, U17-ch7, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 31.59
Std Dev 5.063
Gaus mean : 32.3746
Gaus Width: 3.1840
Entry
ampl
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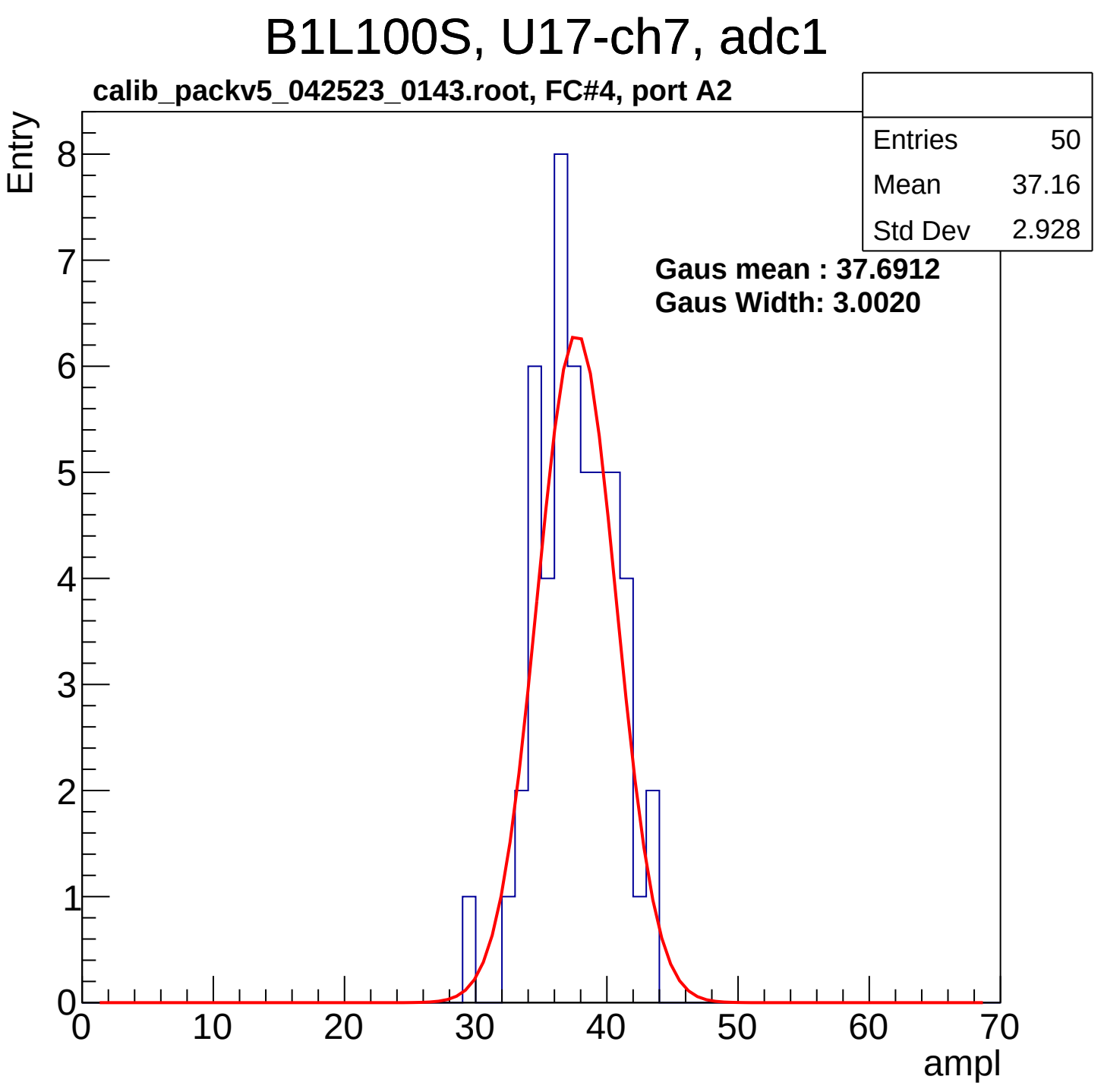
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch7, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 37.16
Std Dev 2.928
Gaus mean : 37.6912
Gaus Width: 3.0020
Entry
ampl
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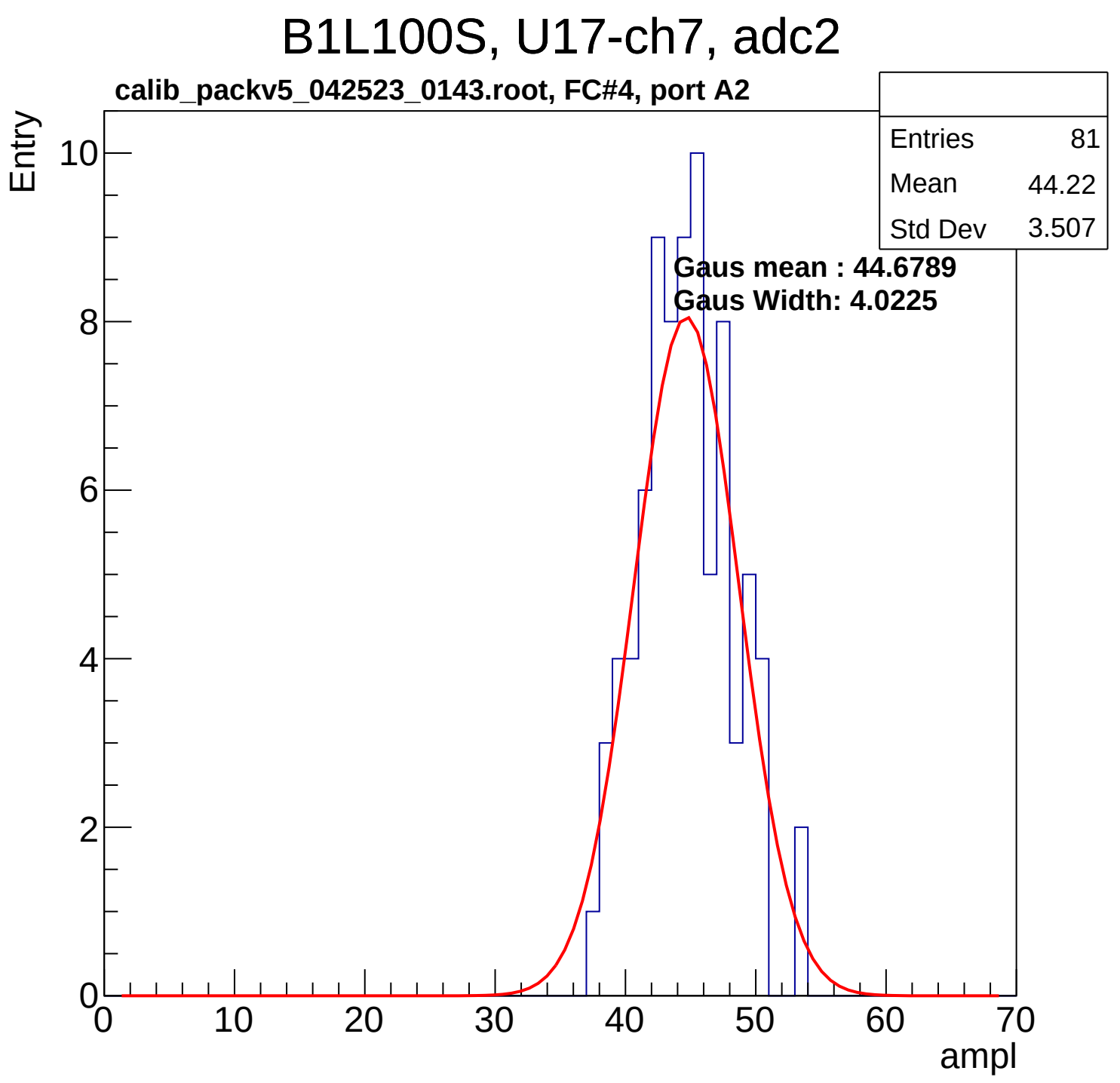
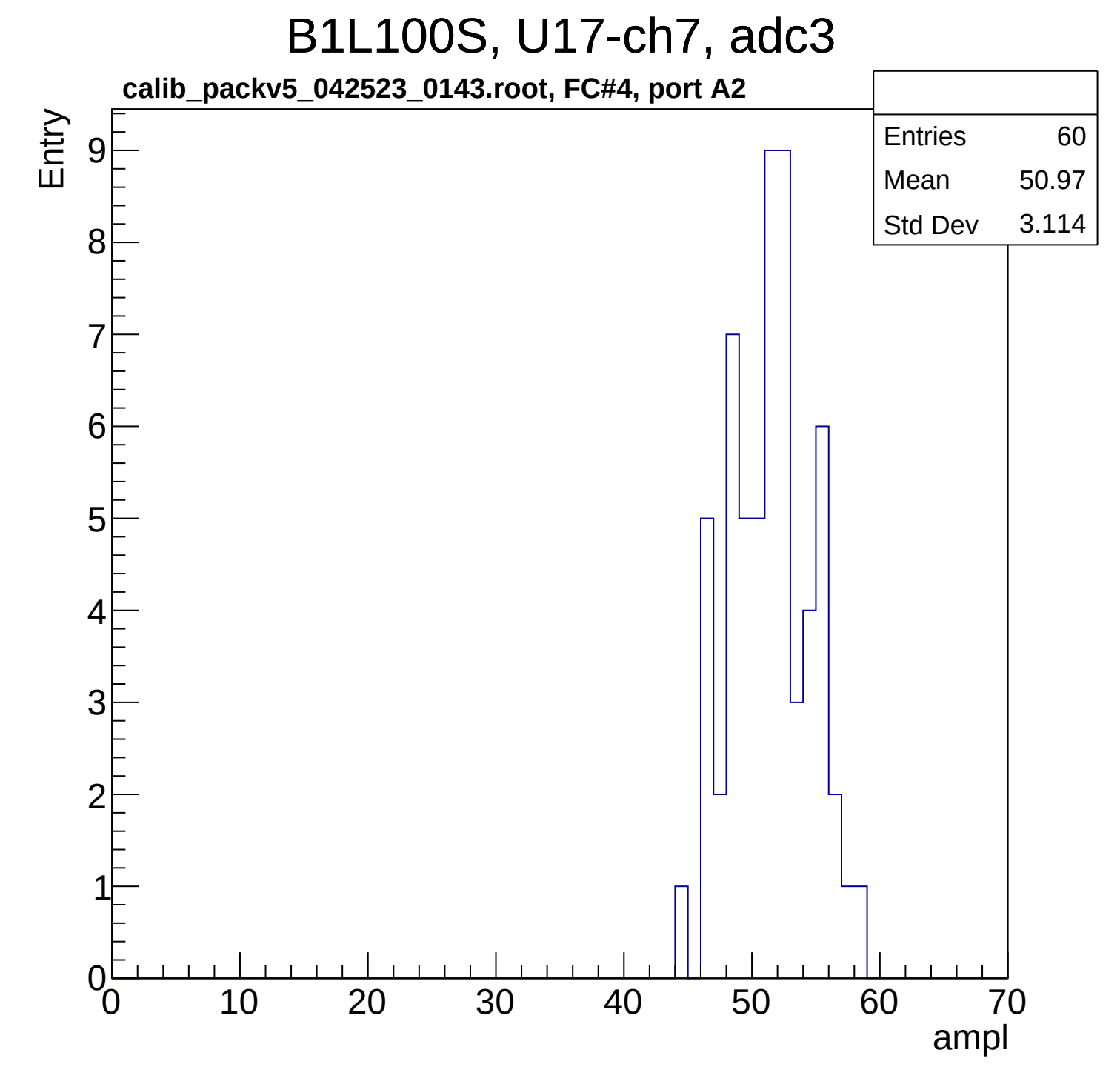
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch7, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 81
Mean 44.22
Std Dev 3.507
Gaus mean : 44.6789
Gaus Width: 4.0225
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U17-ch7, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 50.97
Std Dev 3.114
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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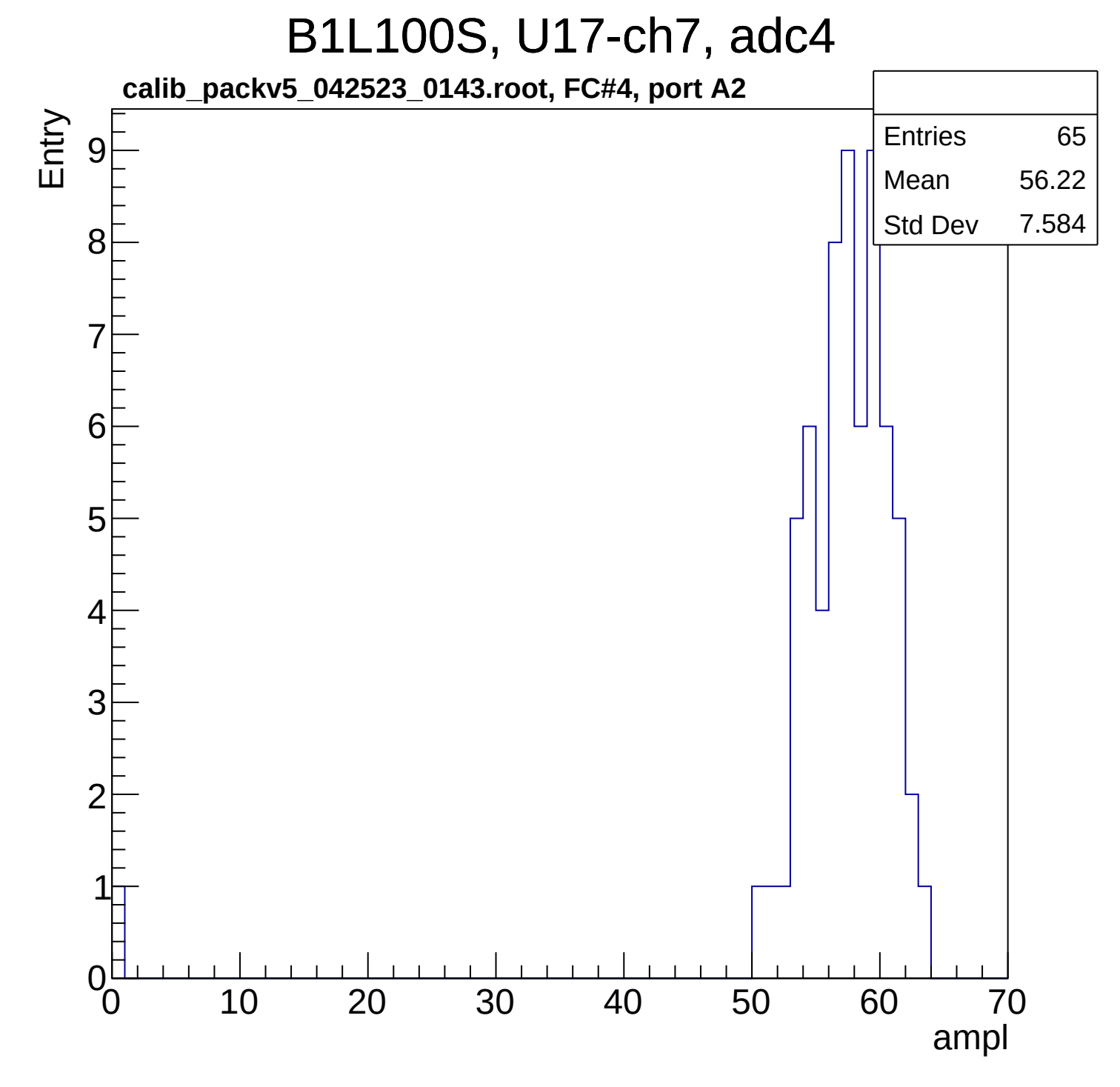
B1L100S, U17-ch7, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 56.22
Std Dev 7.584
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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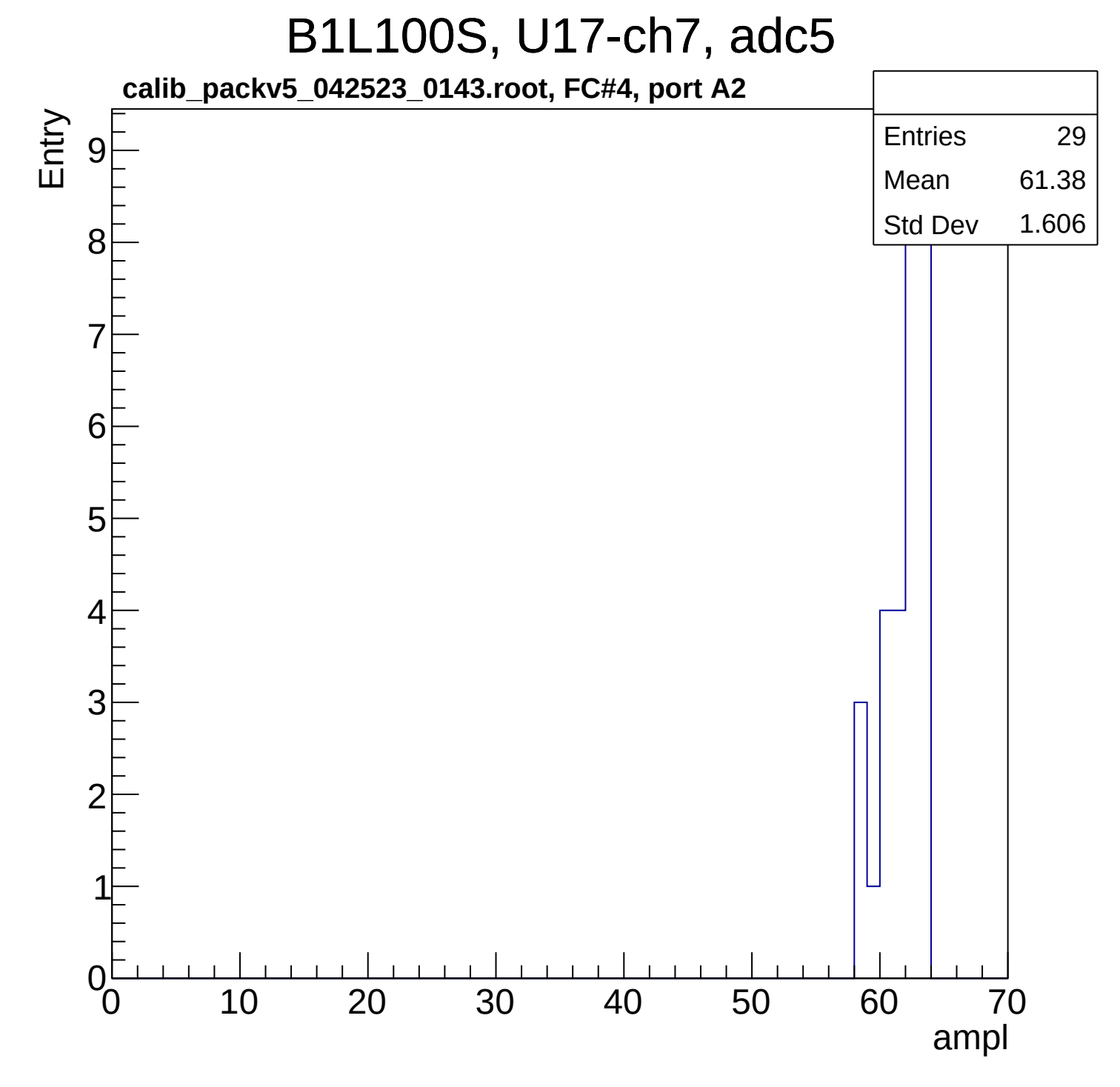
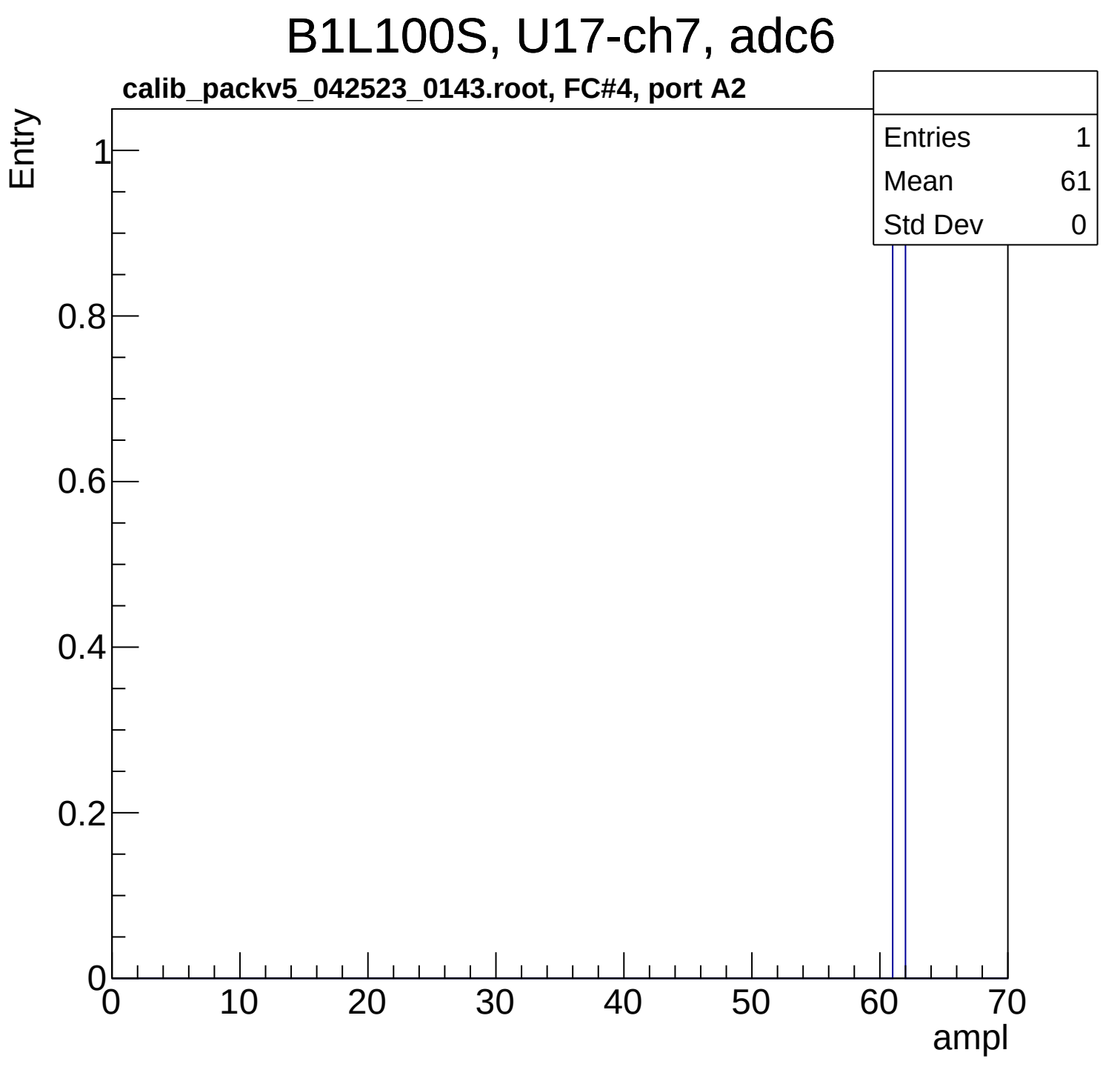

B1L100S, U17-ch7, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 29
Mean 61.38
Std Dev 1.606
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch7, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 61
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
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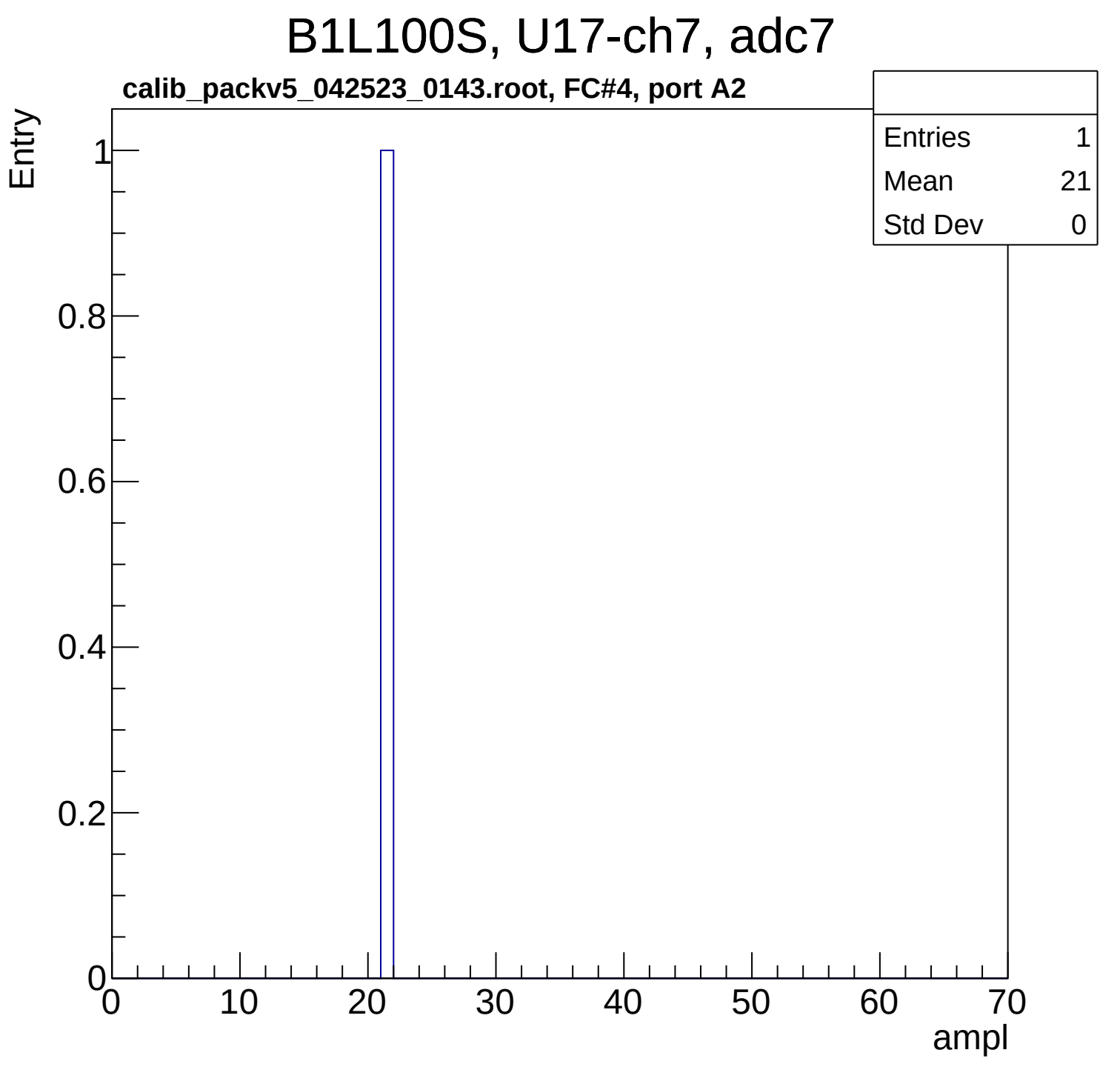
50
60
70
ampl


B1L100S, U17-ch7, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 21
Std Dev 0
Entry
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0.6
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0.2
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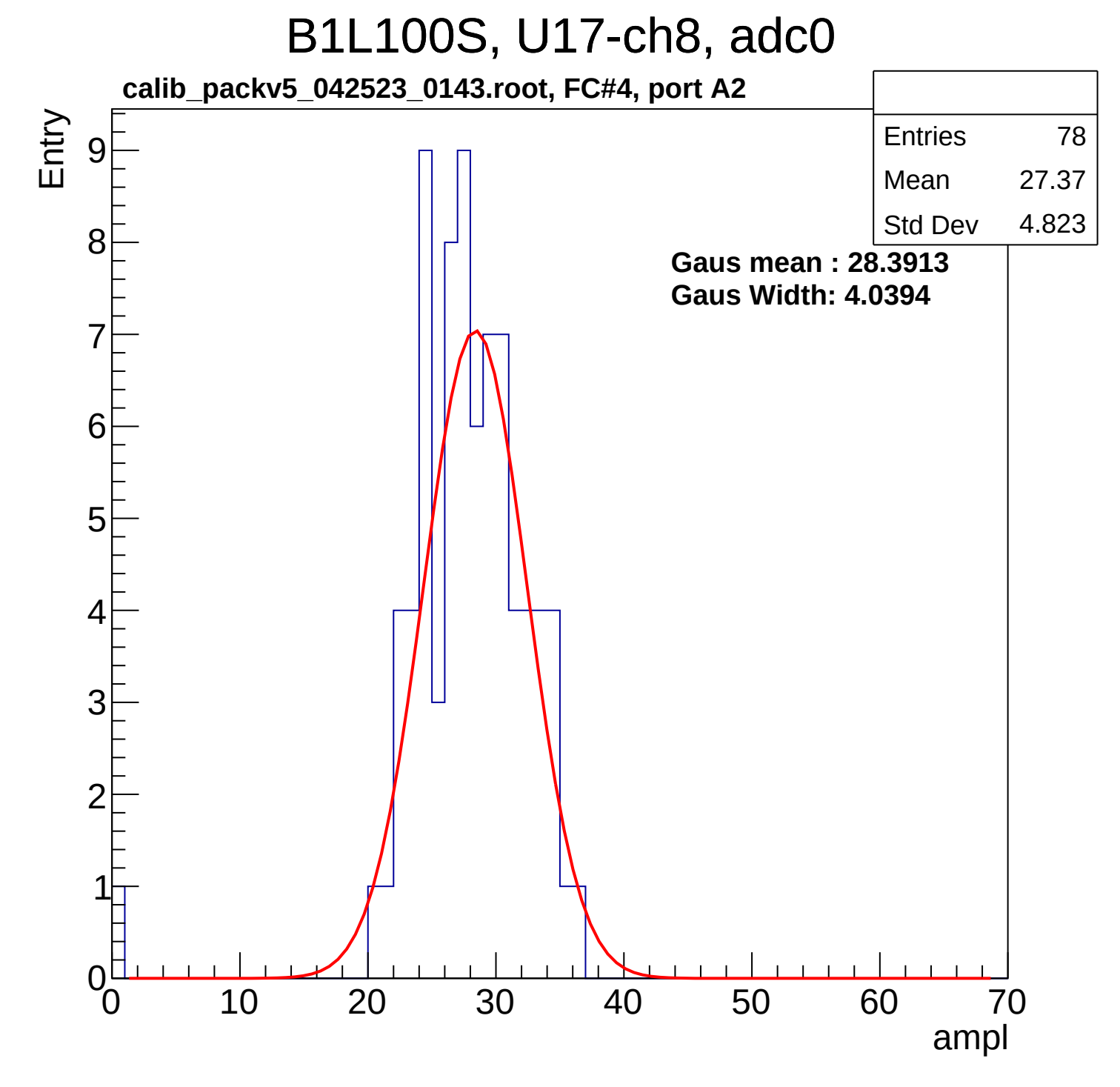
70
ampl


B1L100S, U17-ch8, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 78
Mean 27.37
Std Dev 4.823
Gaus mean : 28.3913
Gaus Width: 4.0394
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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40
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60
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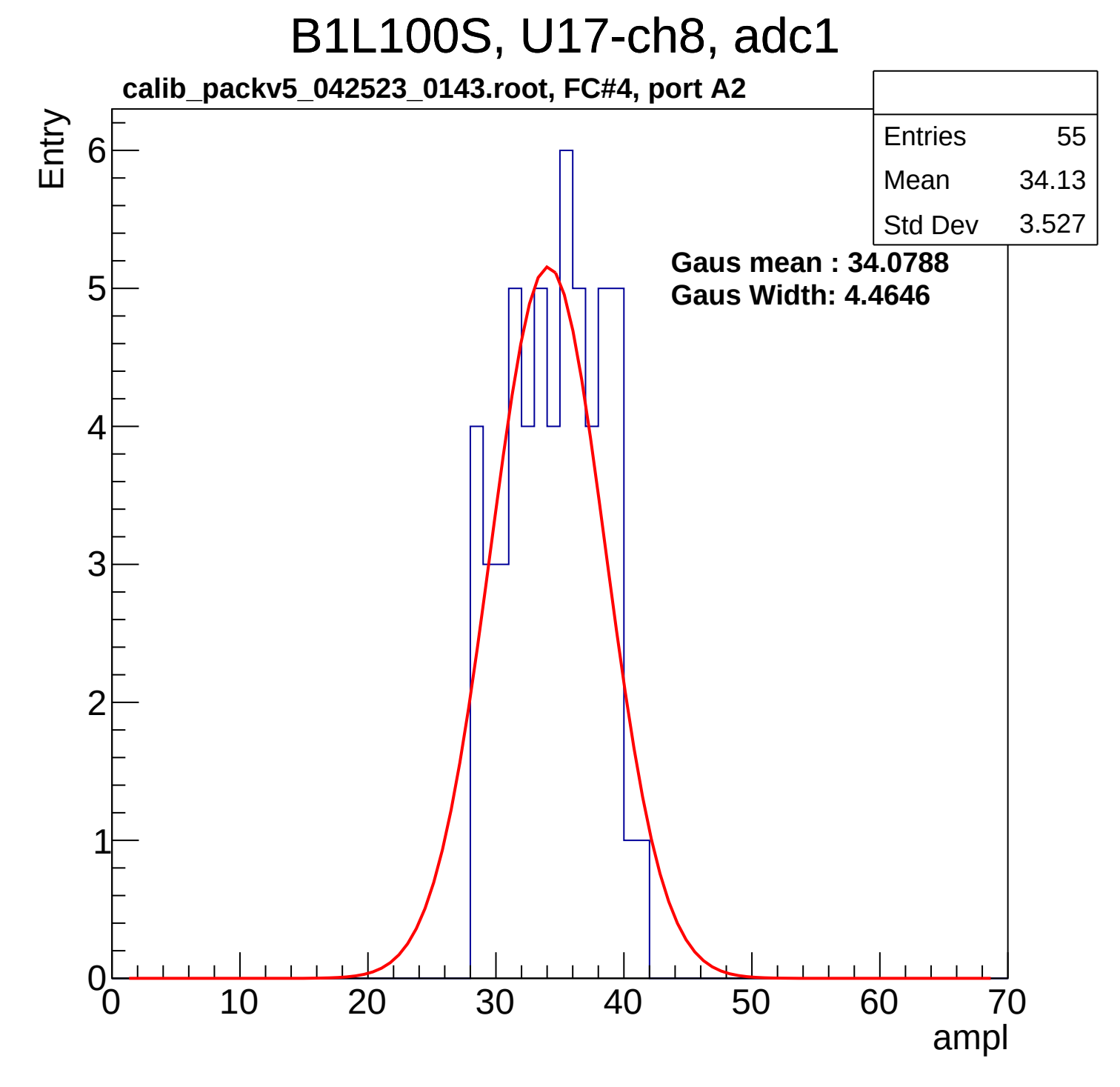
B1L100S, U17-ch8, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 34.13
Std Dev 3.527
Gaus mean : 34.0788
Gaus Width: 4.4646
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
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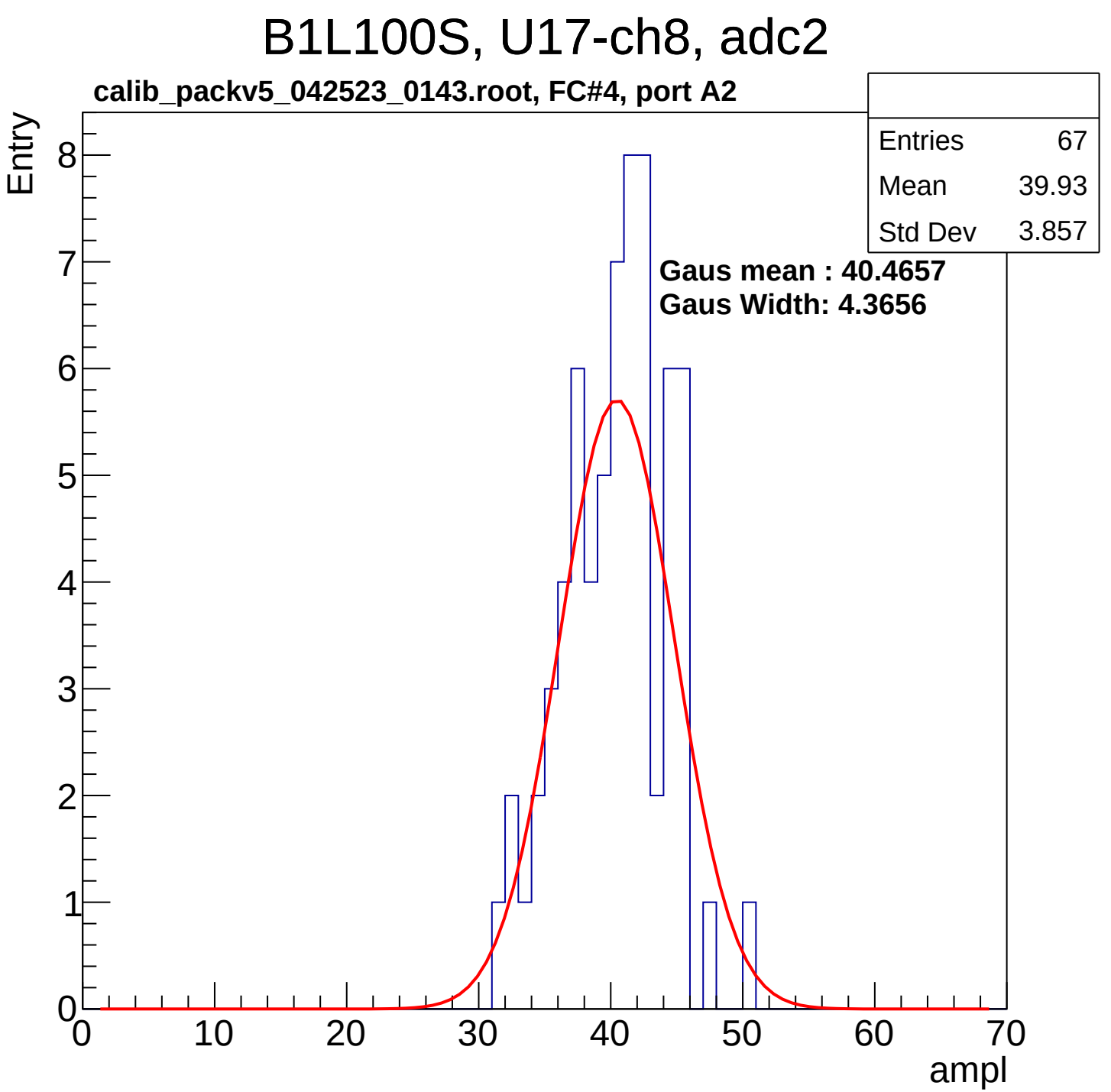
60
70


B1L100S, U17-ch8, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 39.93
Std Dev 3.857
Gaus mean : 40.4657
Gaus Width: 4.3656
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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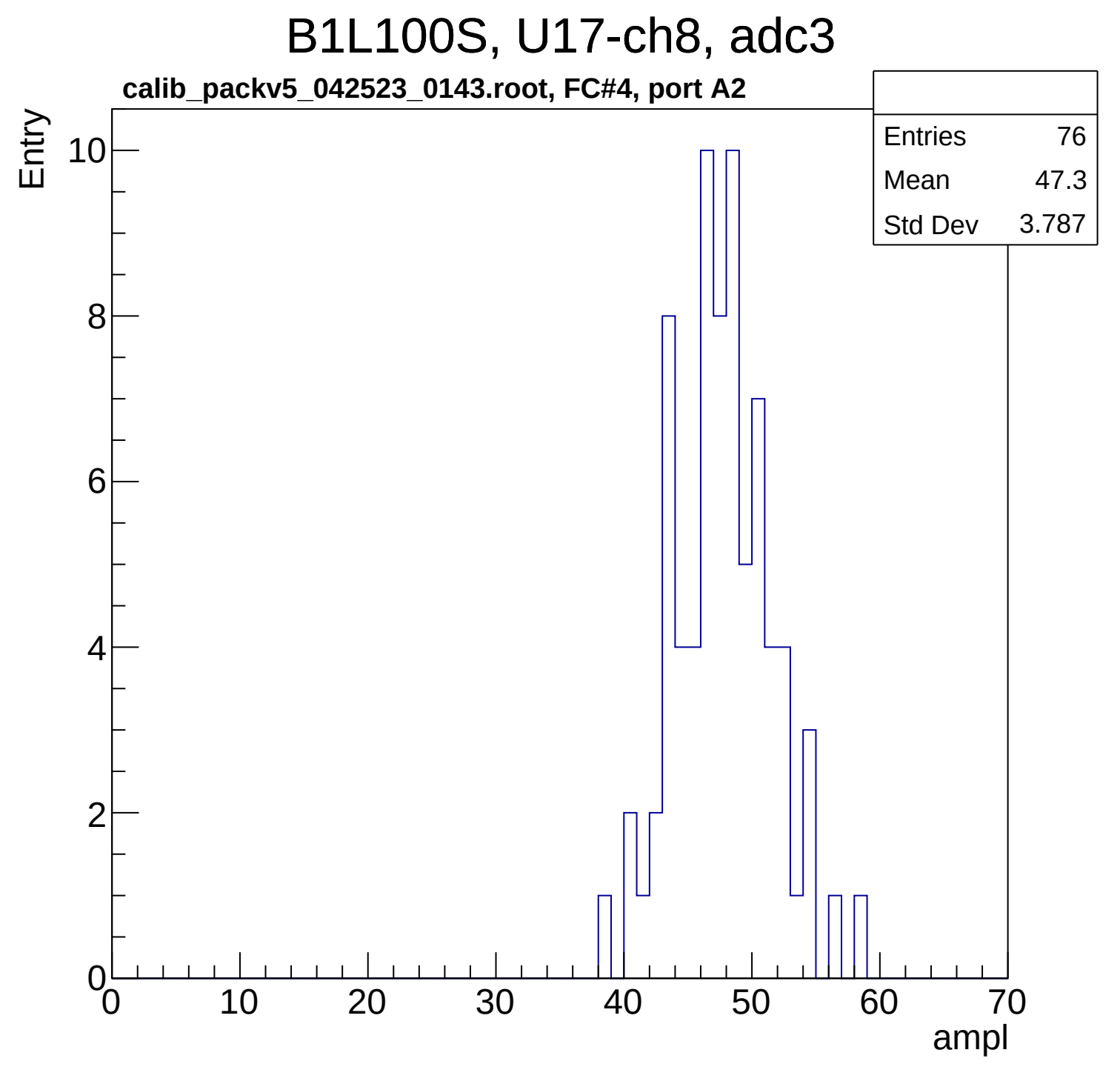
B1L100S, U17-ch8, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 76
Mean 47.3
Std Dev 3.787
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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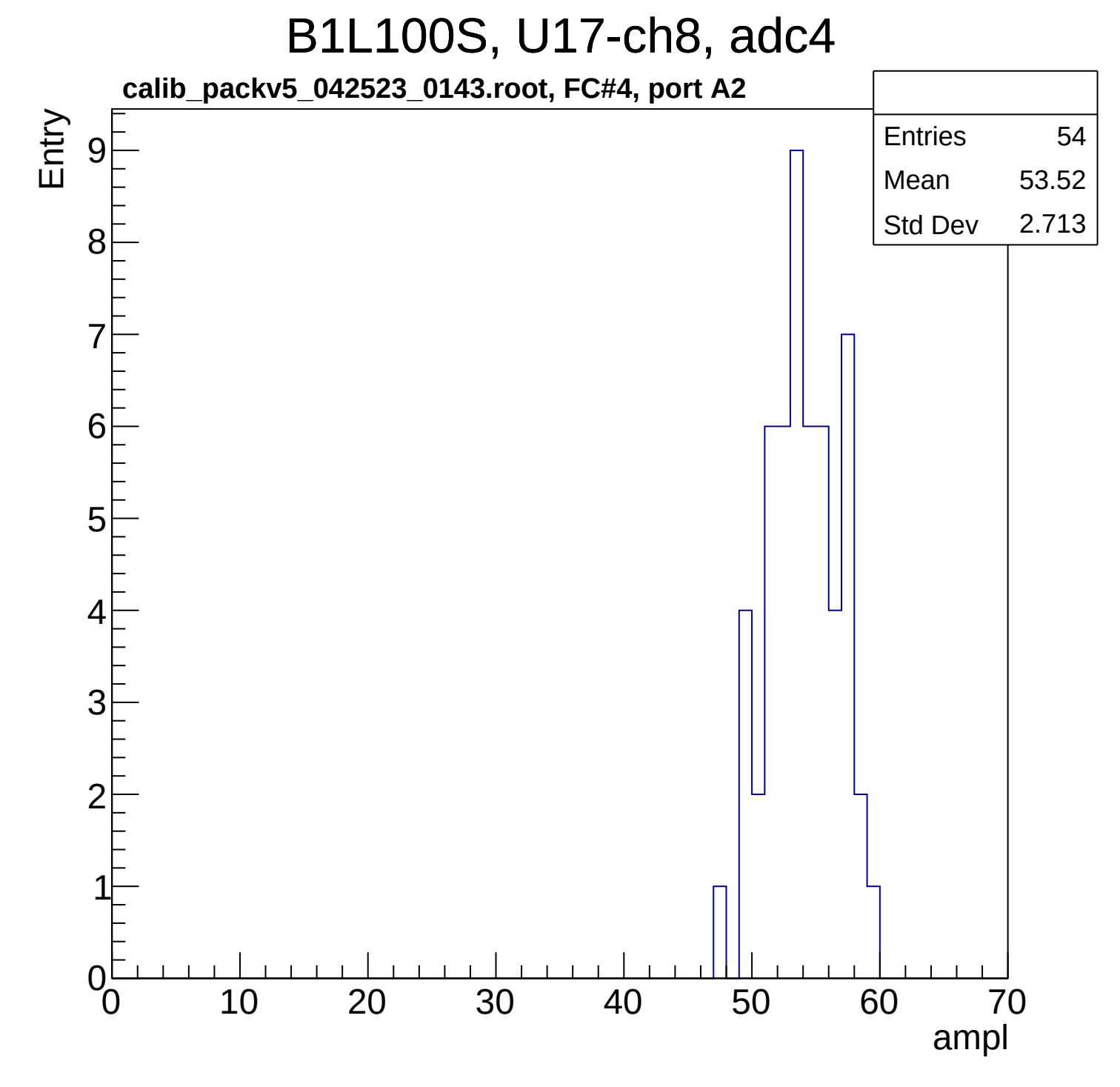
B1L100S, U17-ch8, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 53.52
Std Dev 2.713
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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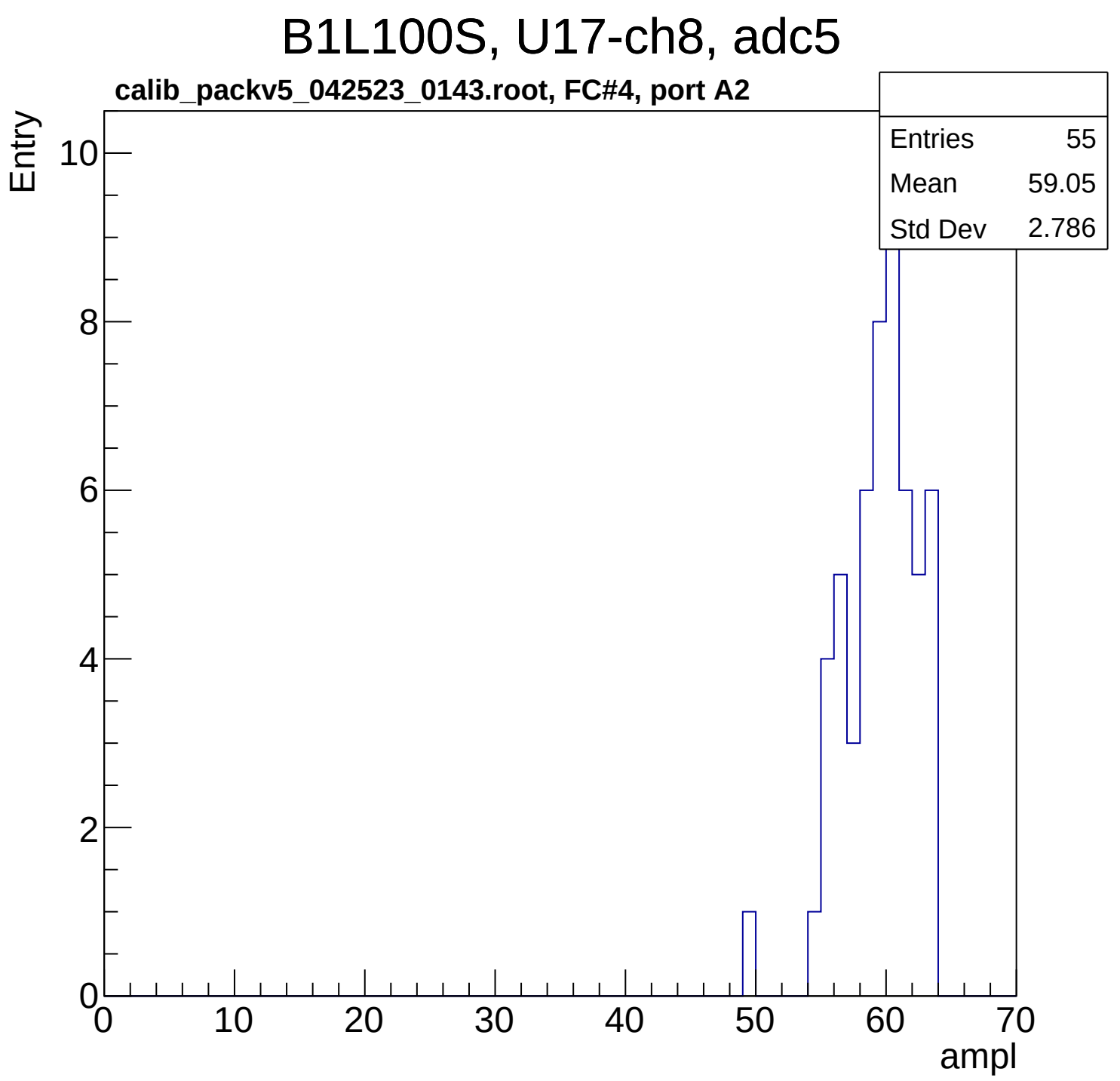
B1L100S, U17-ch8, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 59.05
Std Dev 2.786
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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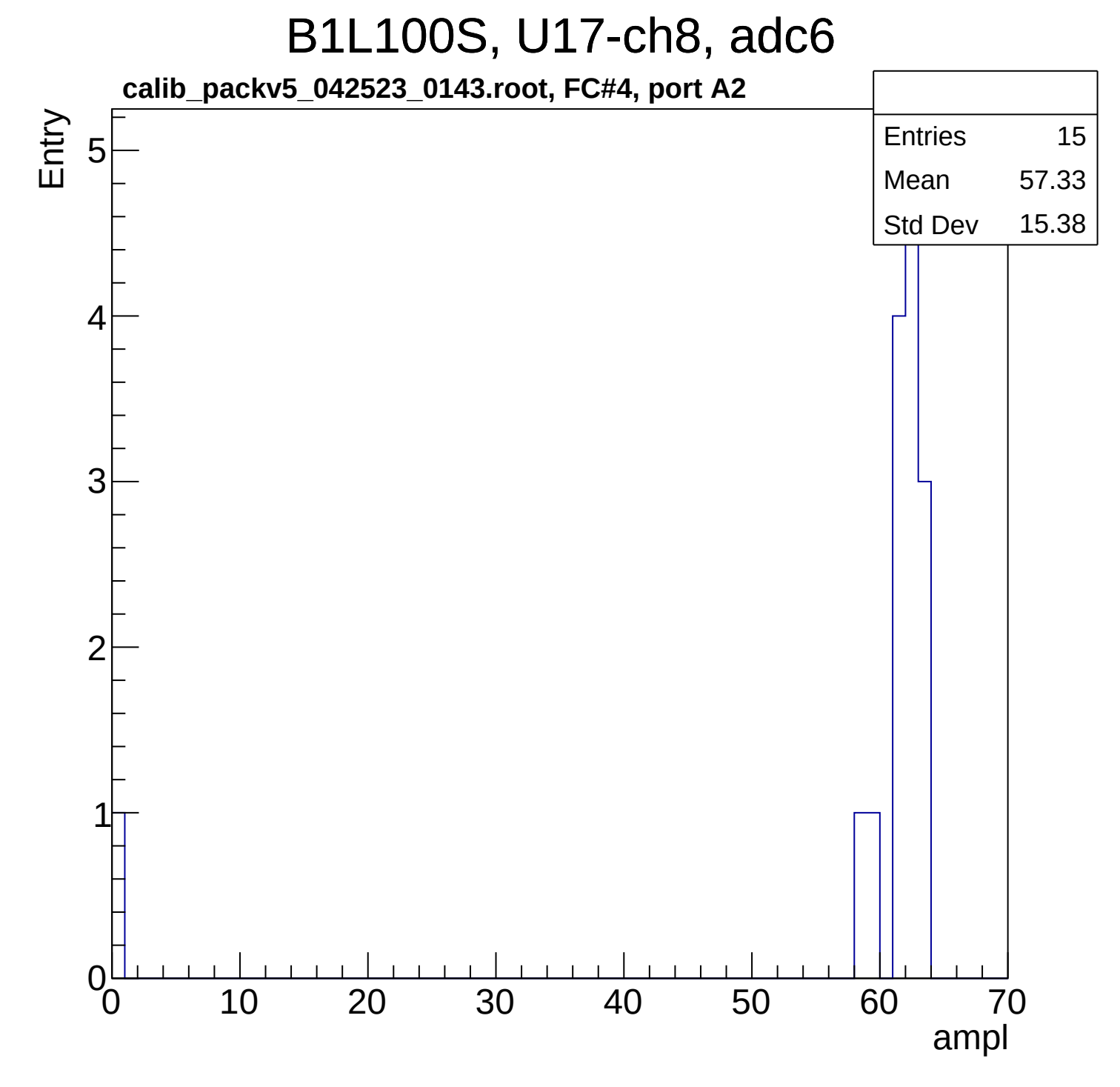
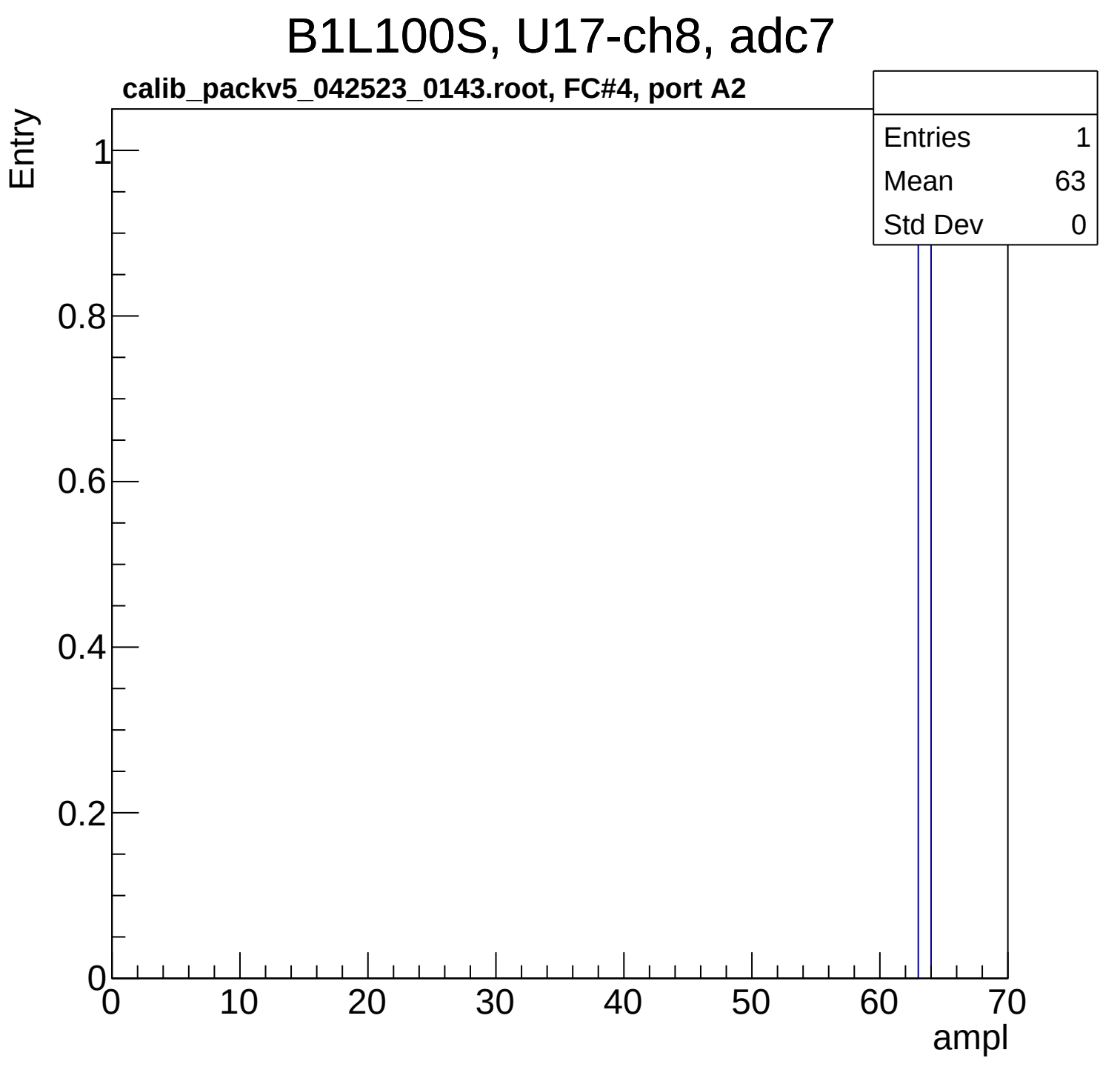
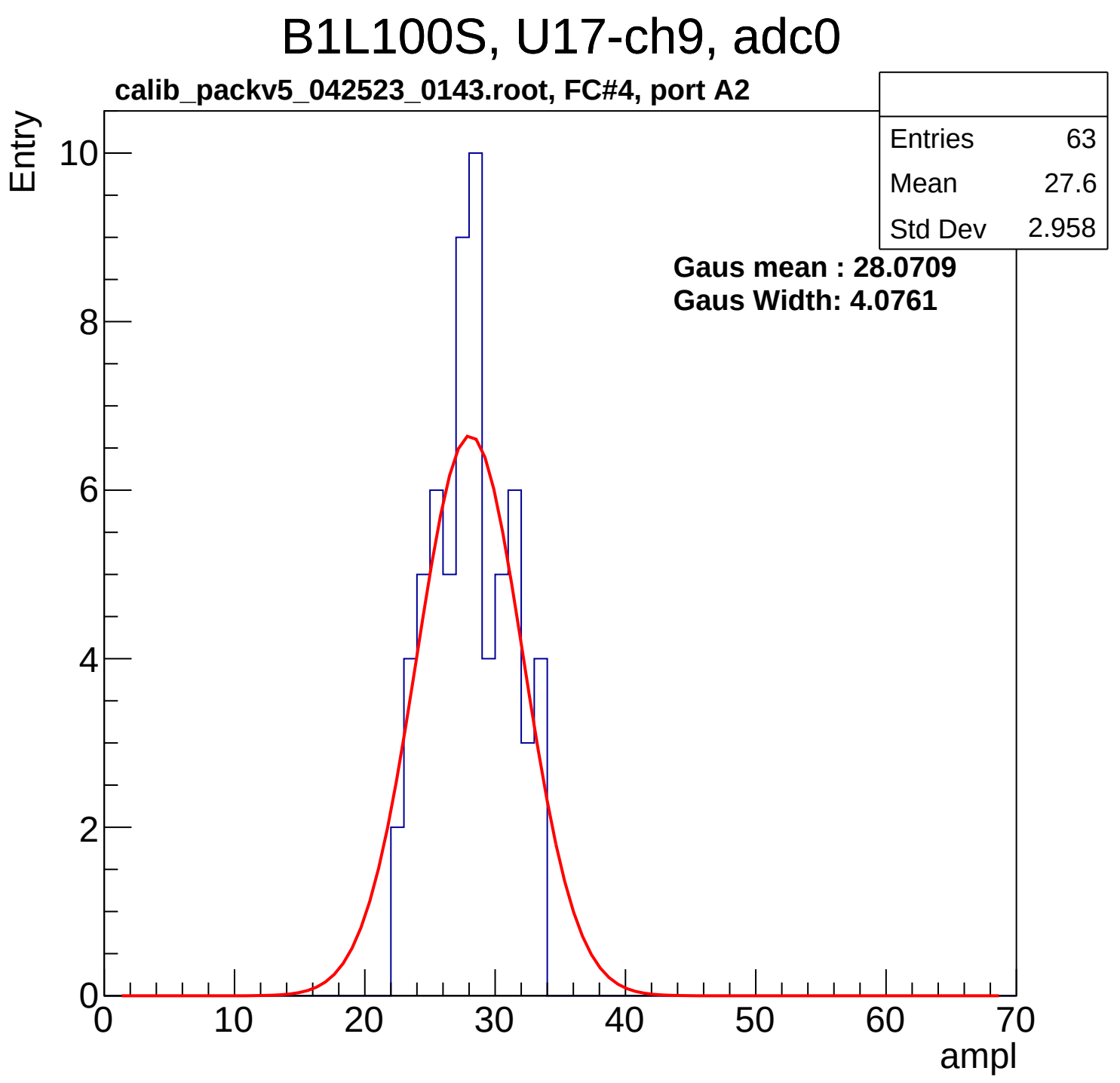

B1L100S, U17-ch8, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 15
Mean 57.33
Std Dev 15.38
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch8, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch9, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 27.6
Std Dev 2.958
Gaus mean : 28.0709
Gaus Width: 4.0761
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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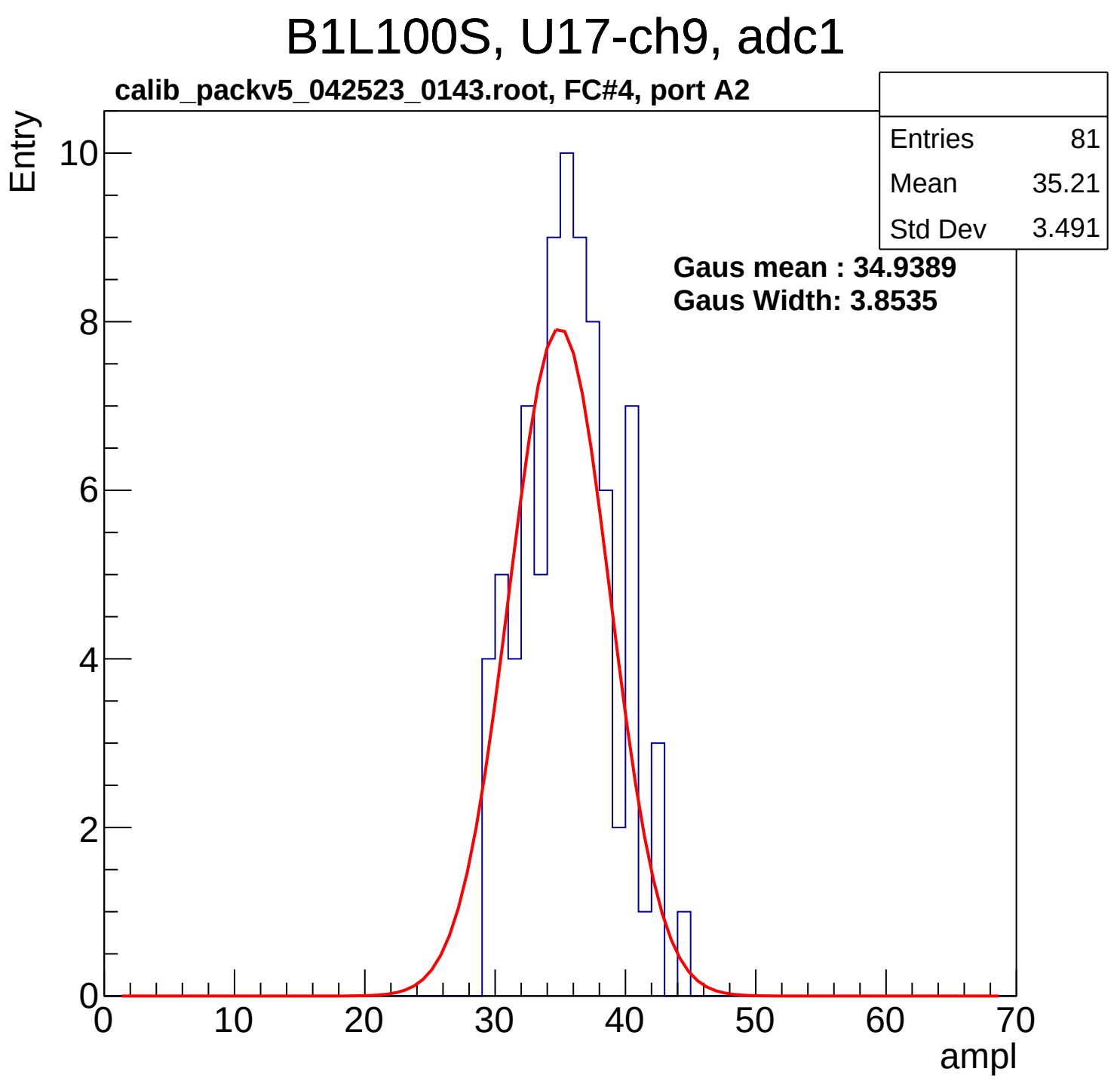
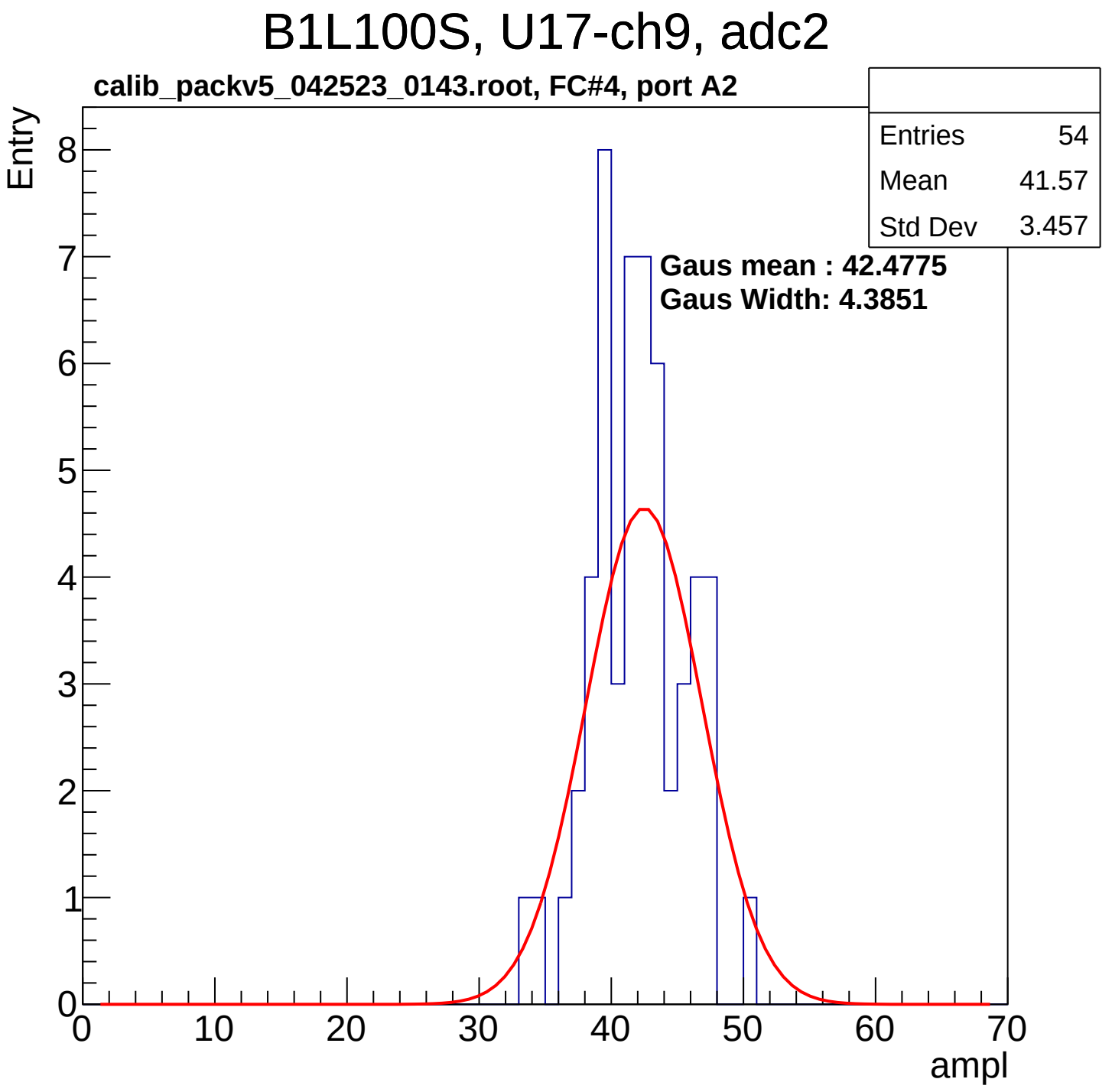
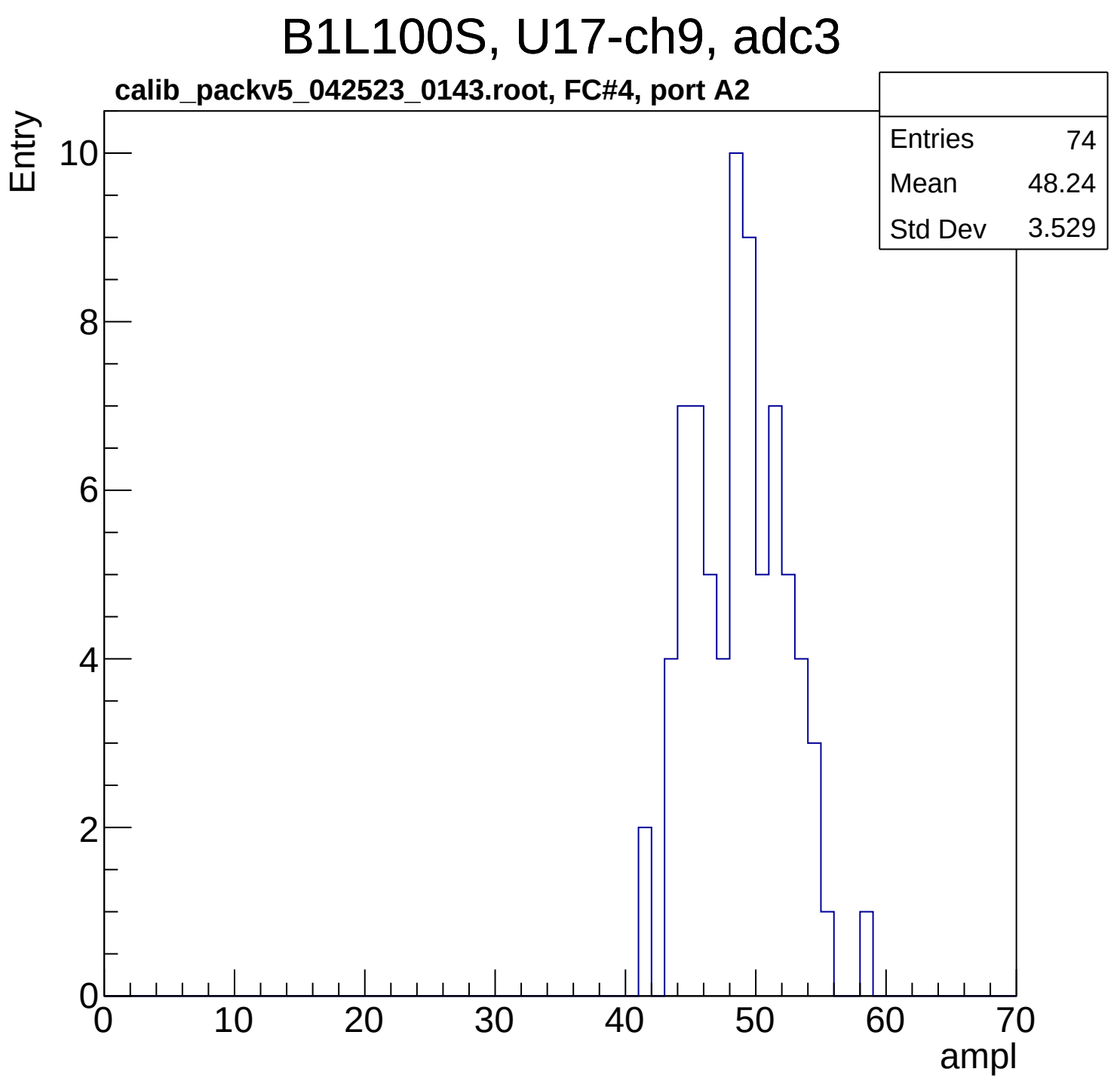
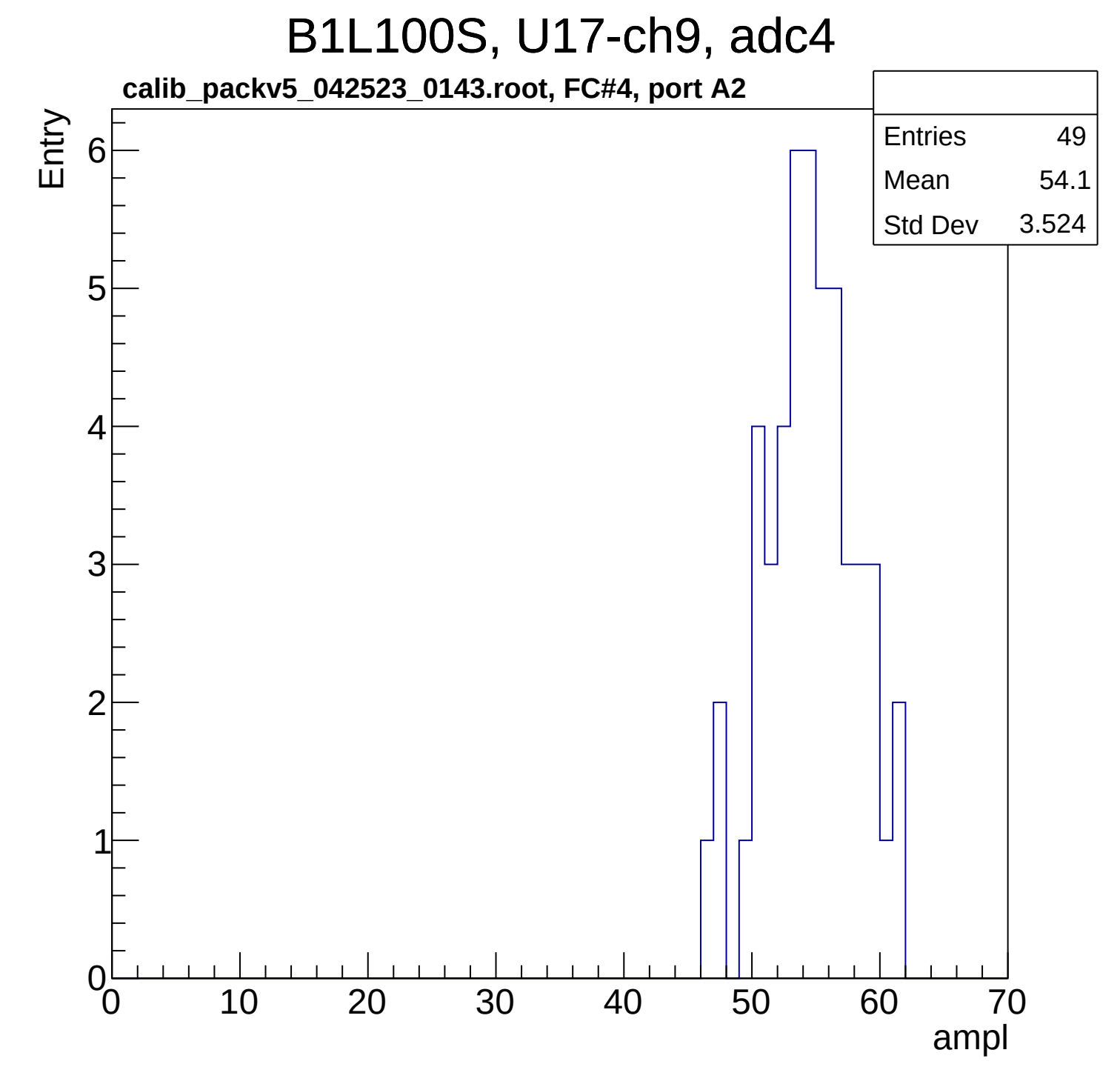
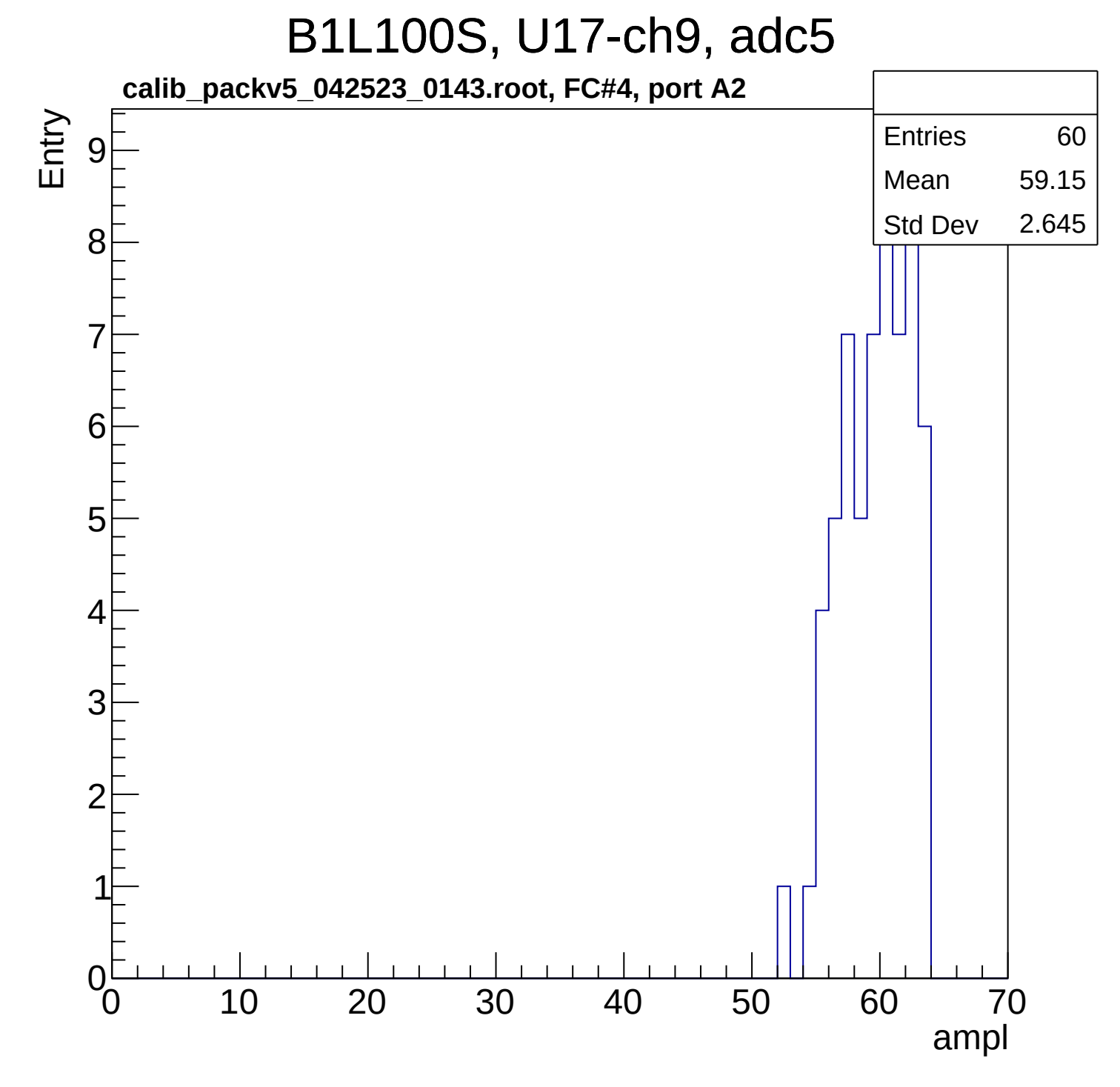

B1L100S, U17-ch9, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 81
Mean 35.21
Std Dev 3.491
Gaus mean : 34.9389
Gaus Width: 3.8535
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U17-ch9, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 41.57
Std Dev 3.457
Gaus mean : 42.4775
Gaus Width: 4.3851
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch9, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 74
Mean 48.24
Std Dev 3.529
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U17-ch9, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 49
Mean 54.1
Std Dev 3.524
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L100S, U17-ch9, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 59.15
Std Dev 2.645
Entry
ampl
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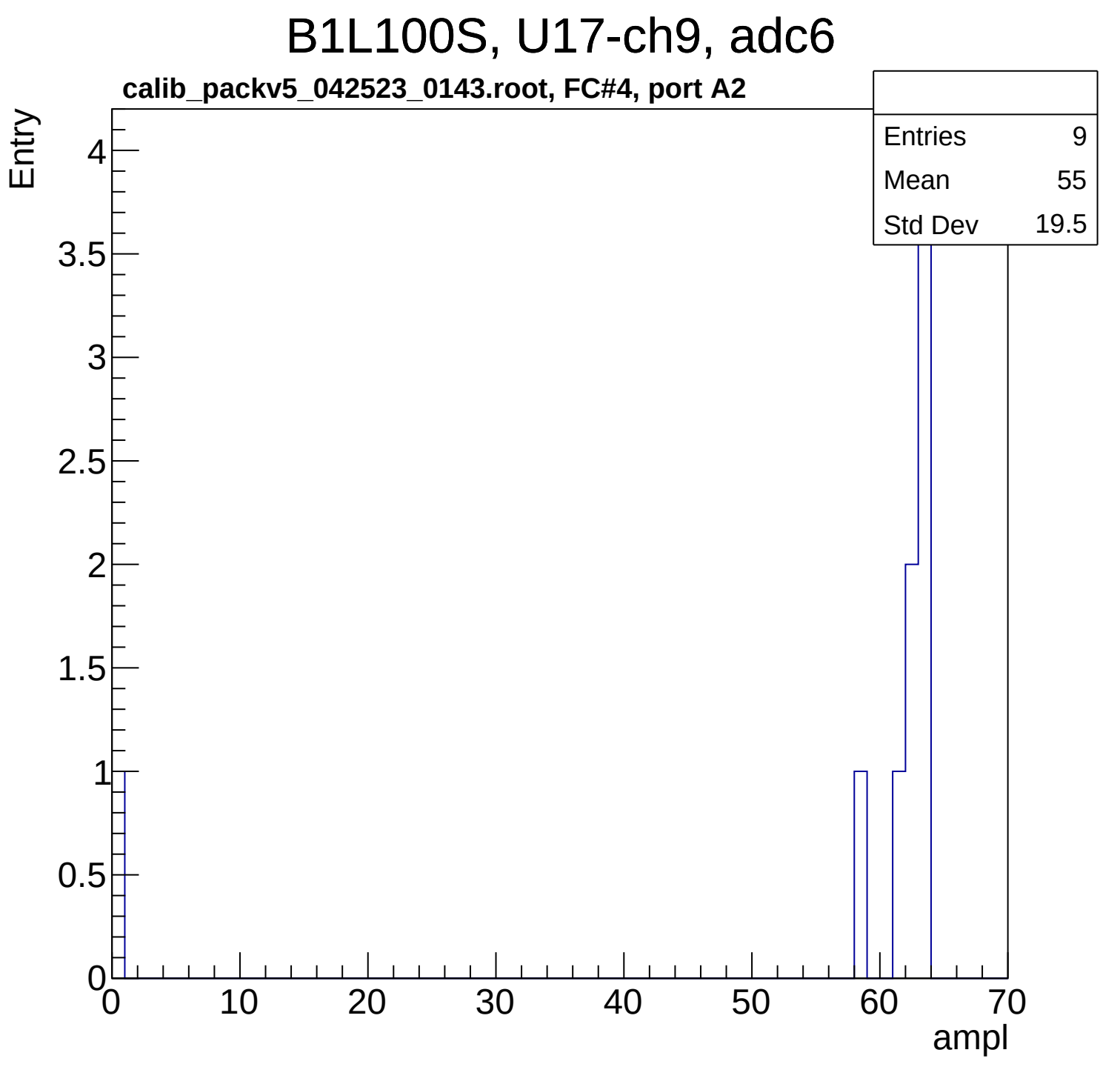
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch9, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 9
Mean 55
Std Dev 19.5
Entry
ampl
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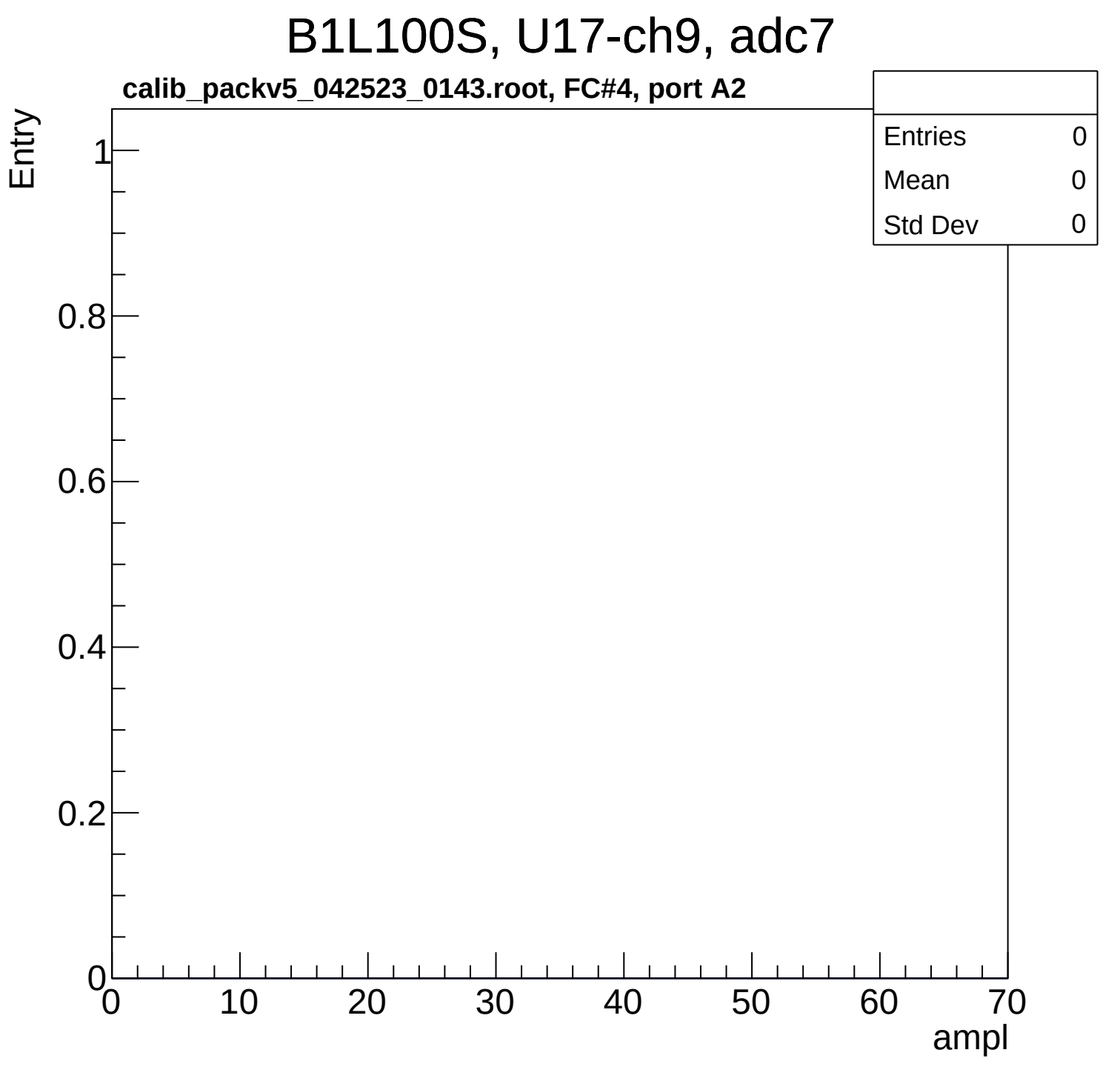
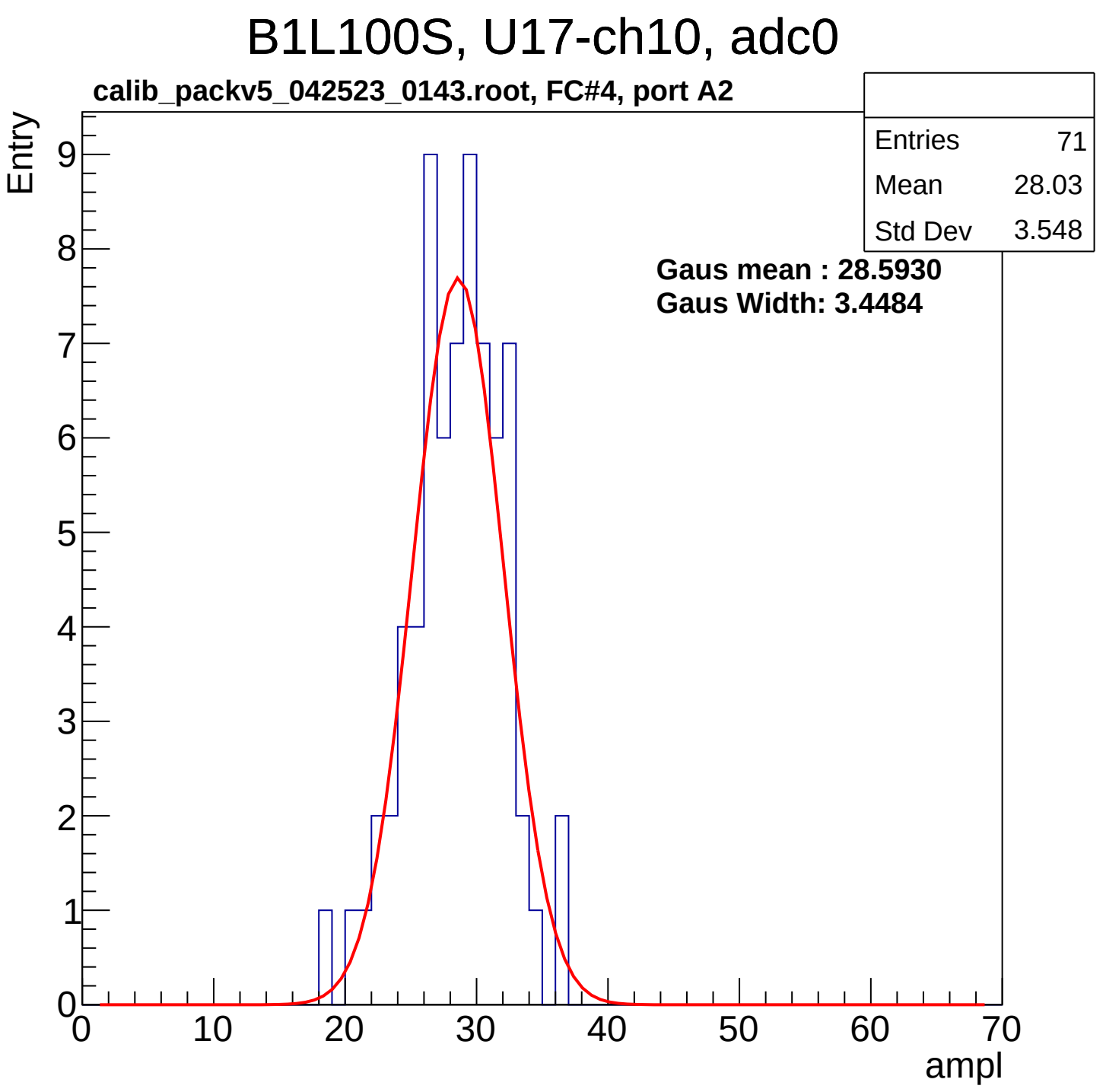
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L100S, U17-ch9, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch10, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 28.03
Std Dev 3.548
Gaus mean : 28.5930
Gaus Width: 3.4484
Entry
ampl
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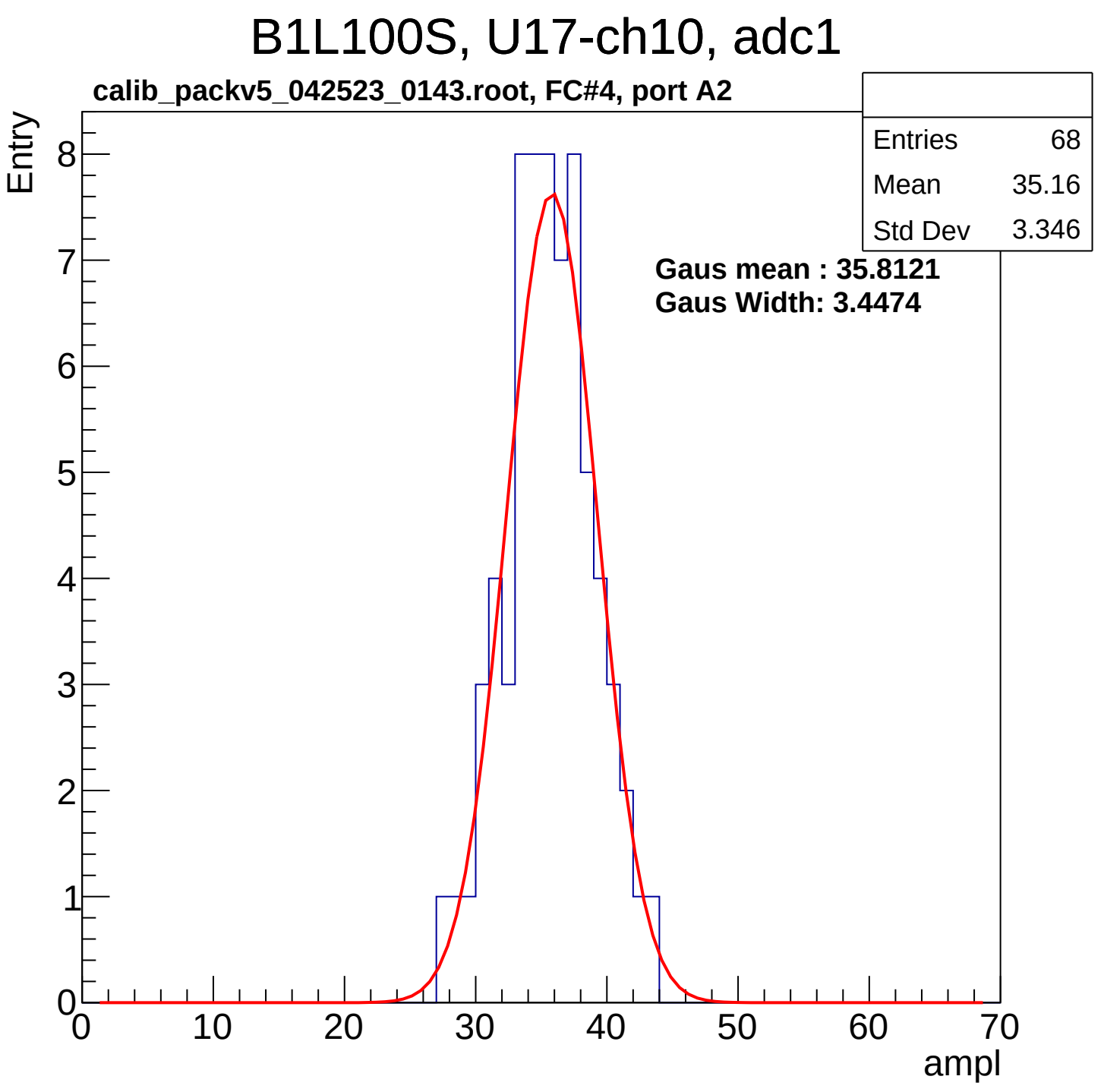
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch10, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 35.16
Std Dev 3.346
Gaus mean : 35.8121
Gaus Width: 3.4474
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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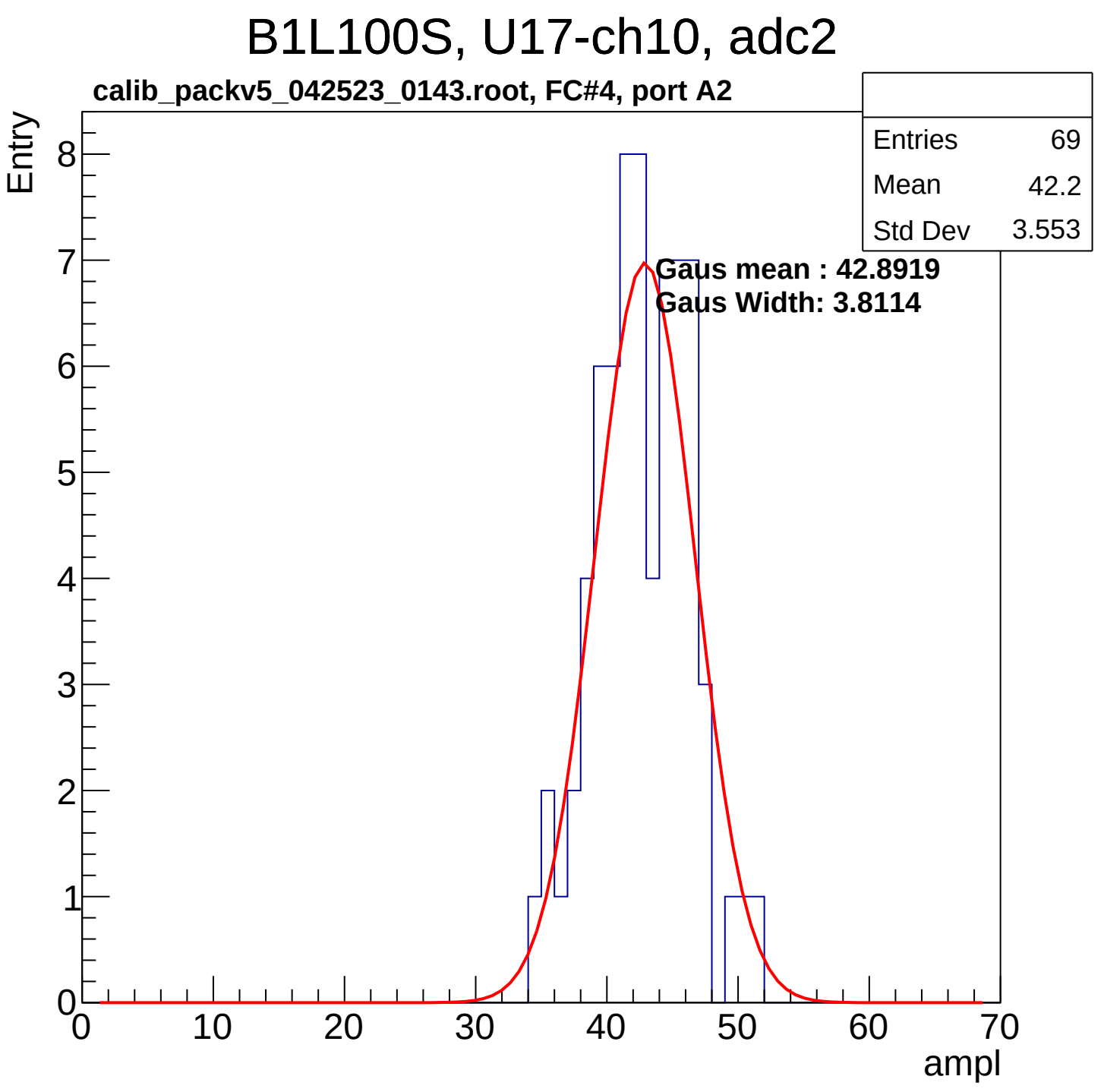
40
50
60
70


B1L100S, U17-ch10, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 42.2
Std Dev 3.553
Gaus mean : 42.8919
Gaus Width: 3.8114
Entry
ampl
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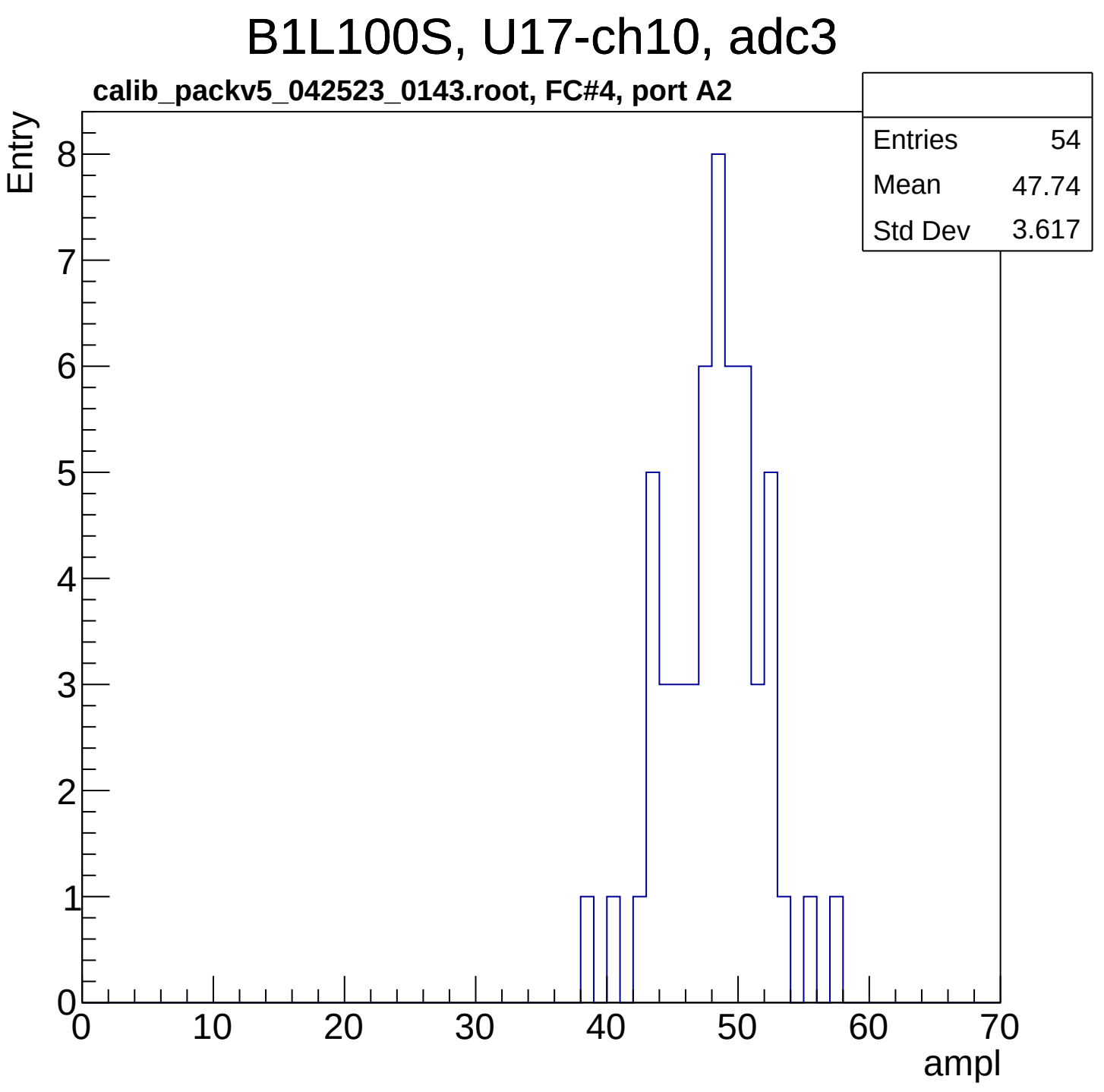
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch10, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 47.74
Std Dev 3.617
Entry
ampl
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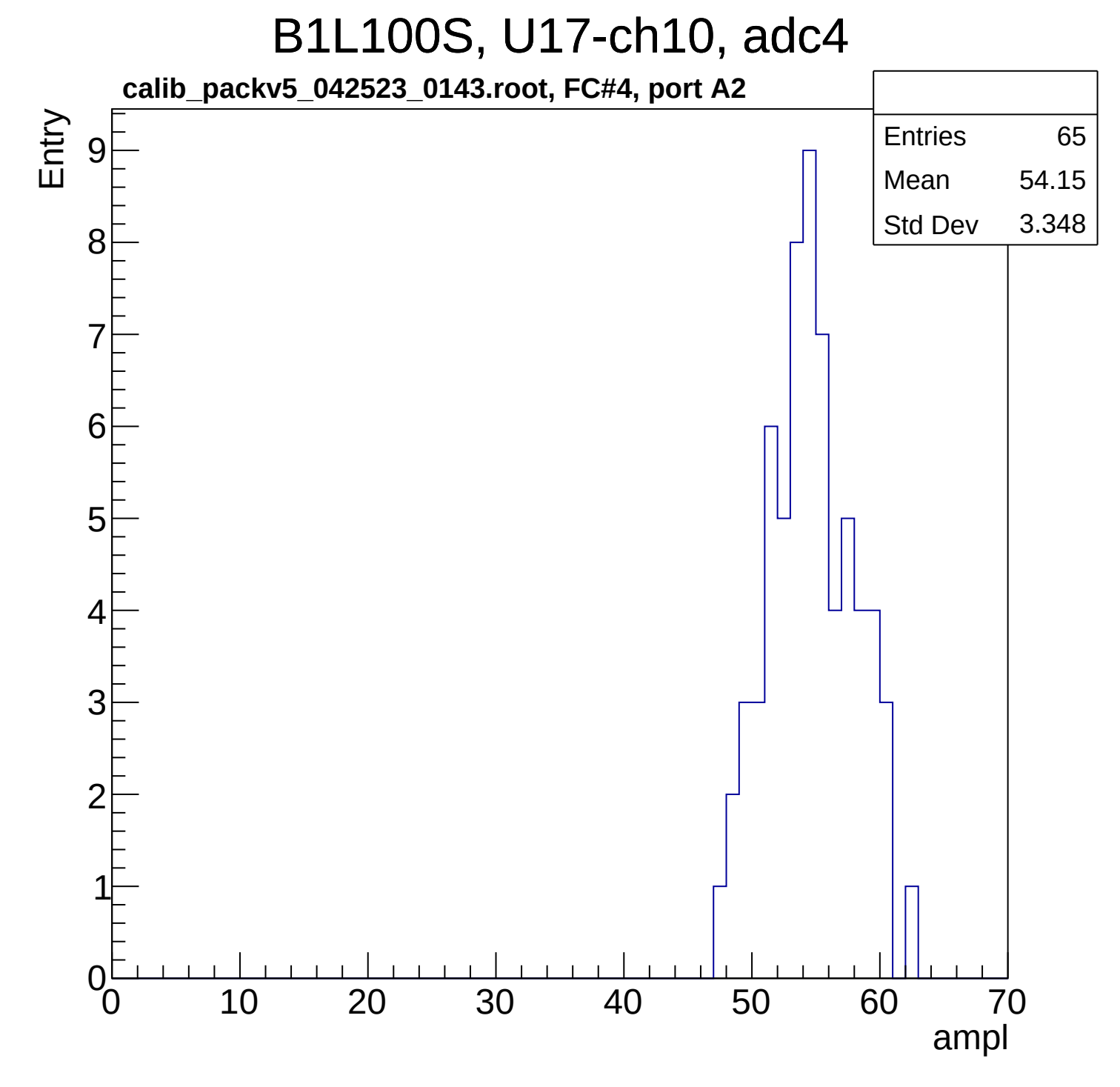
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch10, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 54.15
Std Dev 3.348
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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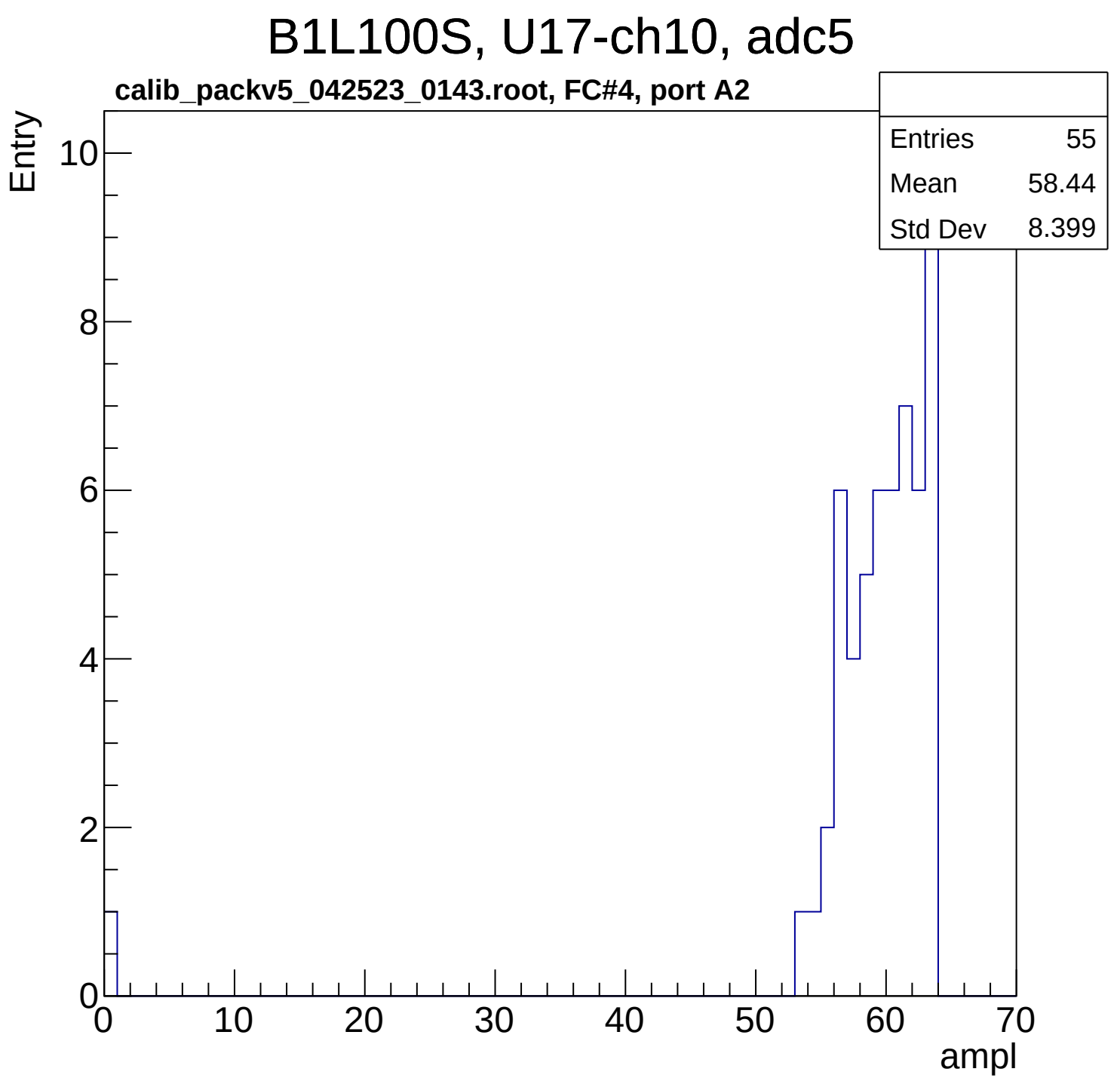
60
70


B1L100S, U17-ch10, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 58.44
Std Dev 8.399
Entry
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10
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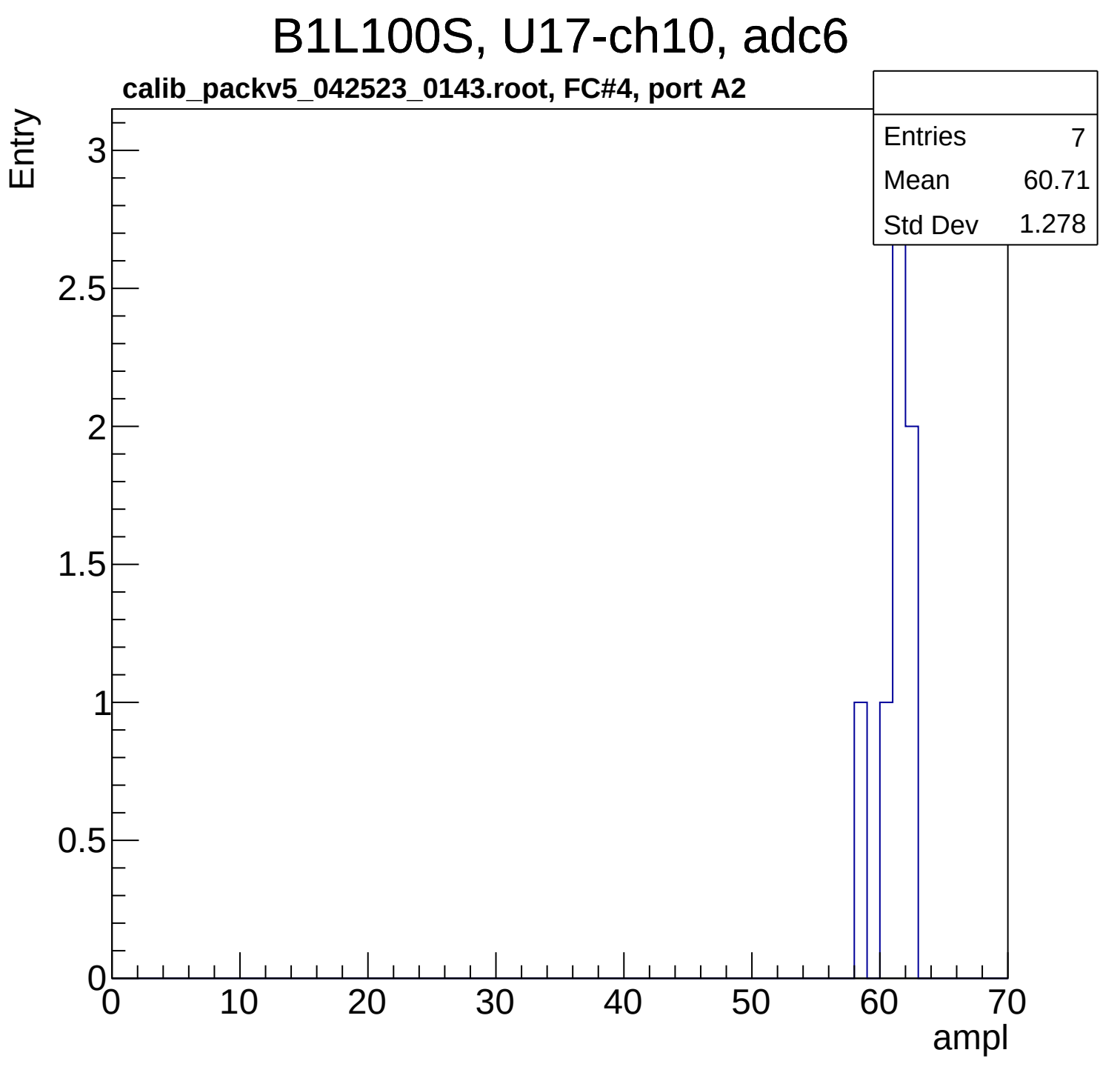
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch10, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 7
Mean 60.71
Std Dev 1.278
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
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40
50
60
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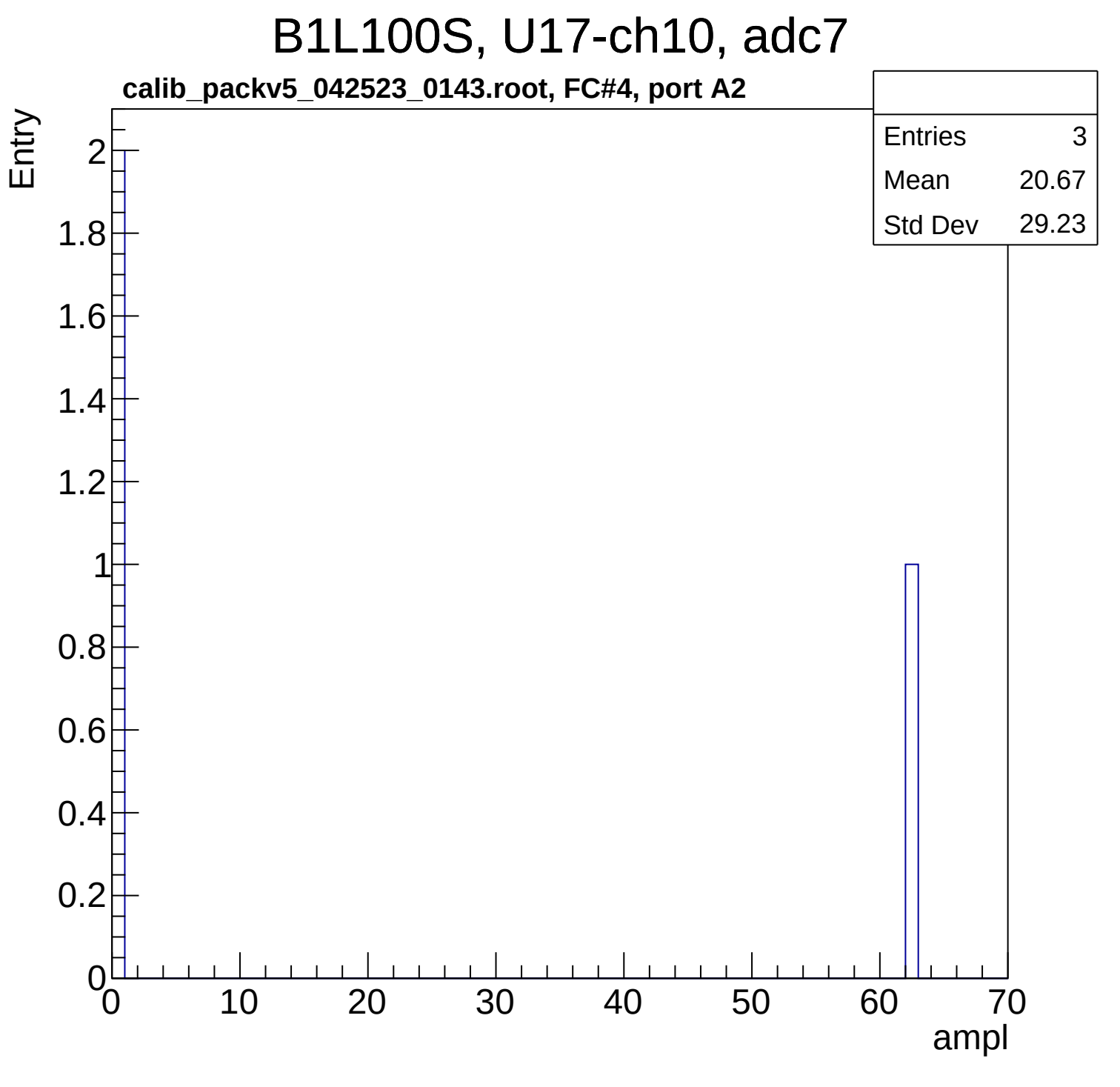
B1L100S, U17-ch10, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 20.67
Std Dev 29.23
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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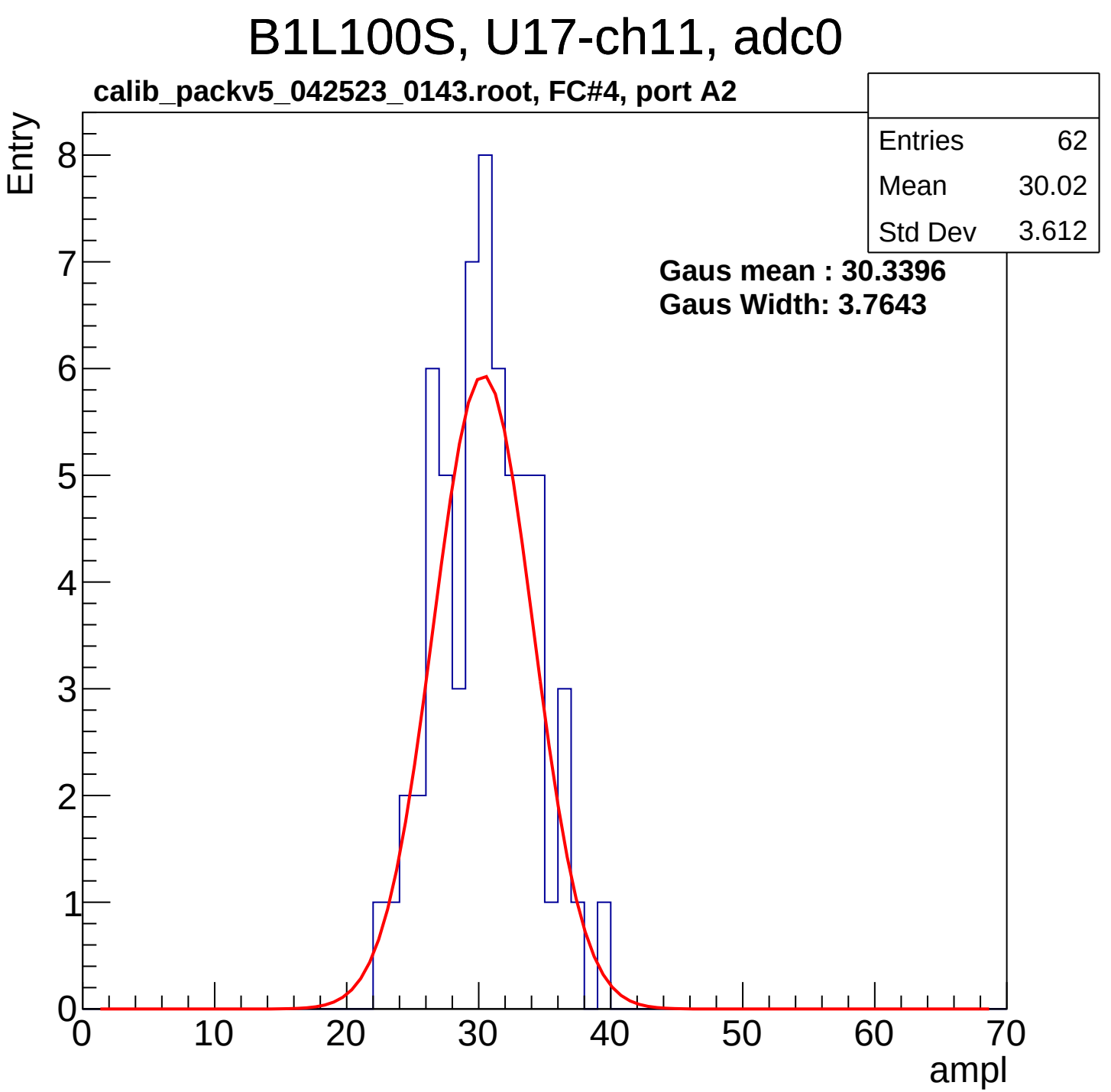
B1L100S, U17-ch11, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 30.02
Std Dev 3.612
Gaus mean : 30.3396
Gaus Width: 3.7643
Entry
ampl
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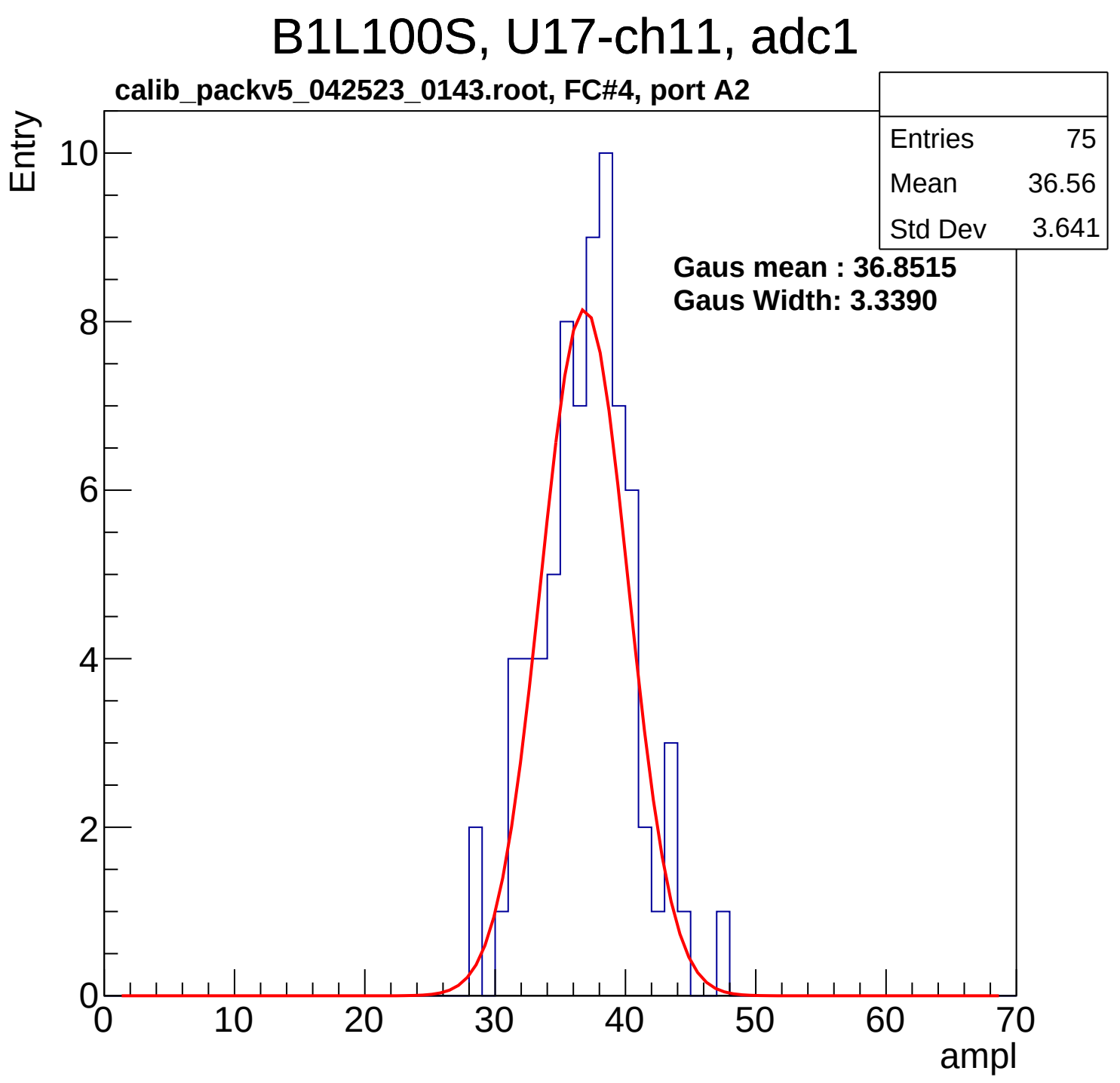
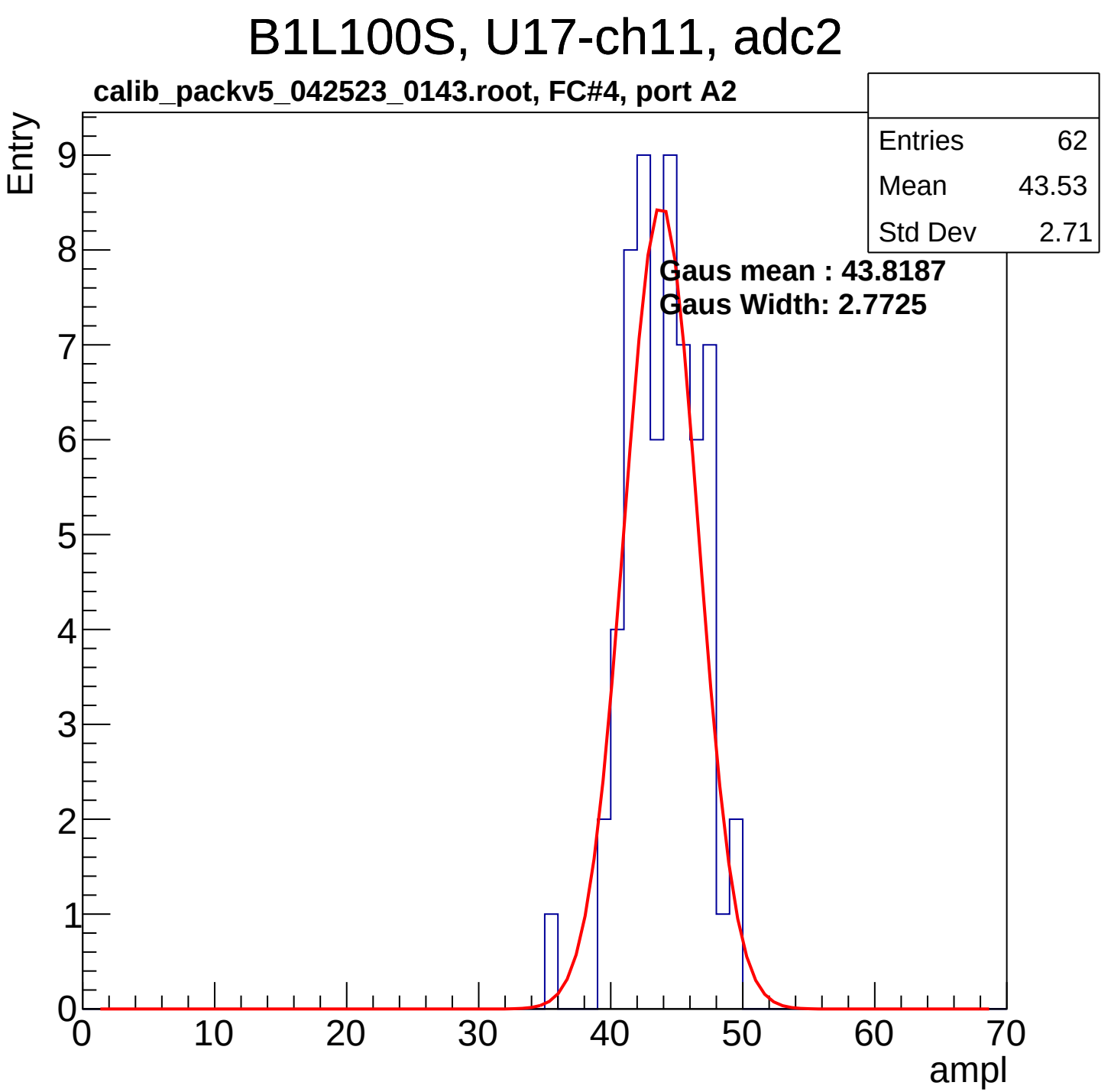
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch11, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 75
Mean 36.56
Std Dev 3.641
Gaus mean : 36.8515
Gaus Width: 3.3390
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U17-ch11, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 43.53
Std Dev 2.71
Gaus mean : 43.8187
Gaus Width: 2.7725
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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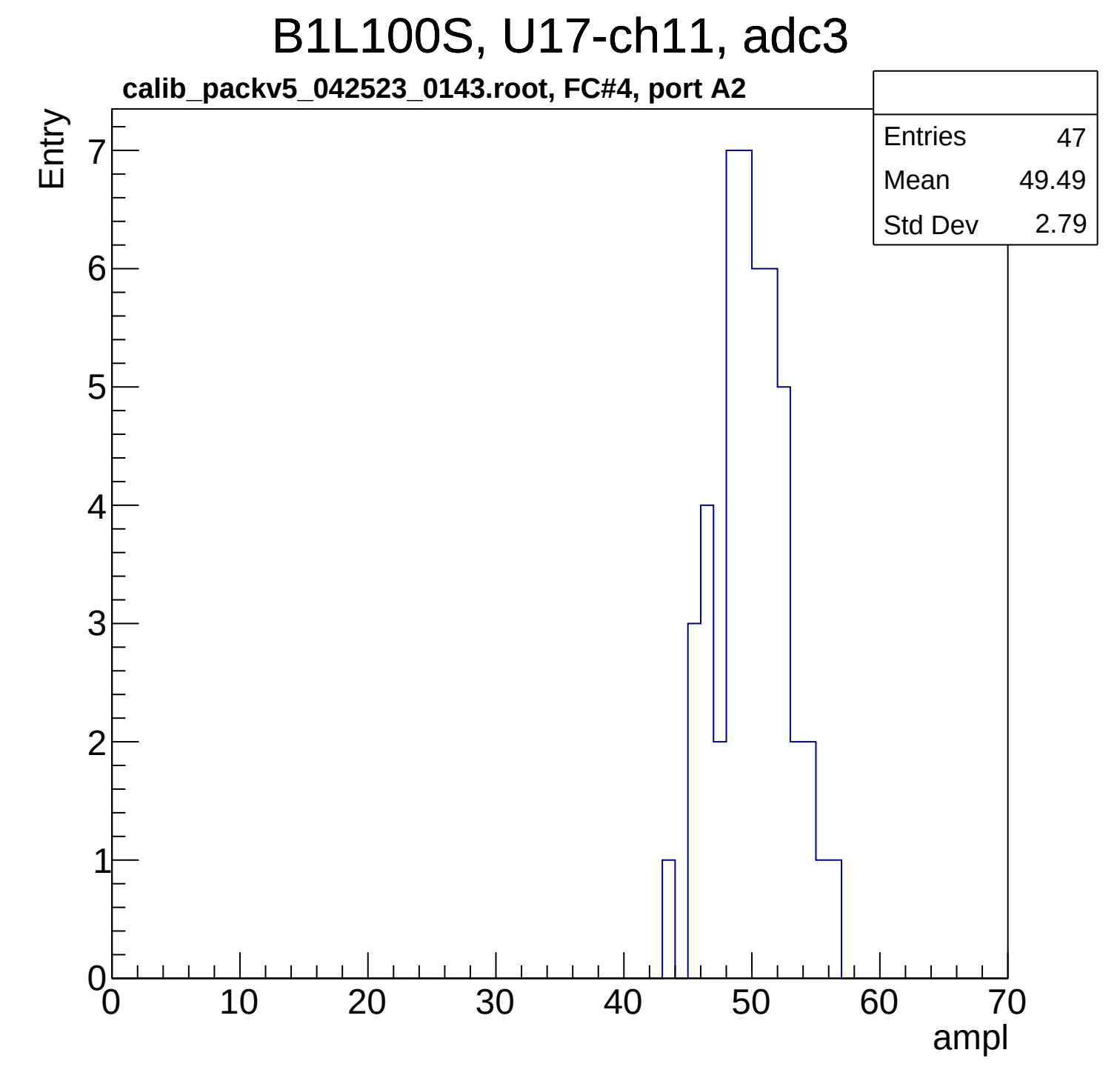
B1L100S, U17-ch11, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 47
Mean 49.49
Std Dev 2.79
Entry
ampl
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2
3
4
5
6
7
0
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20
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40
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60
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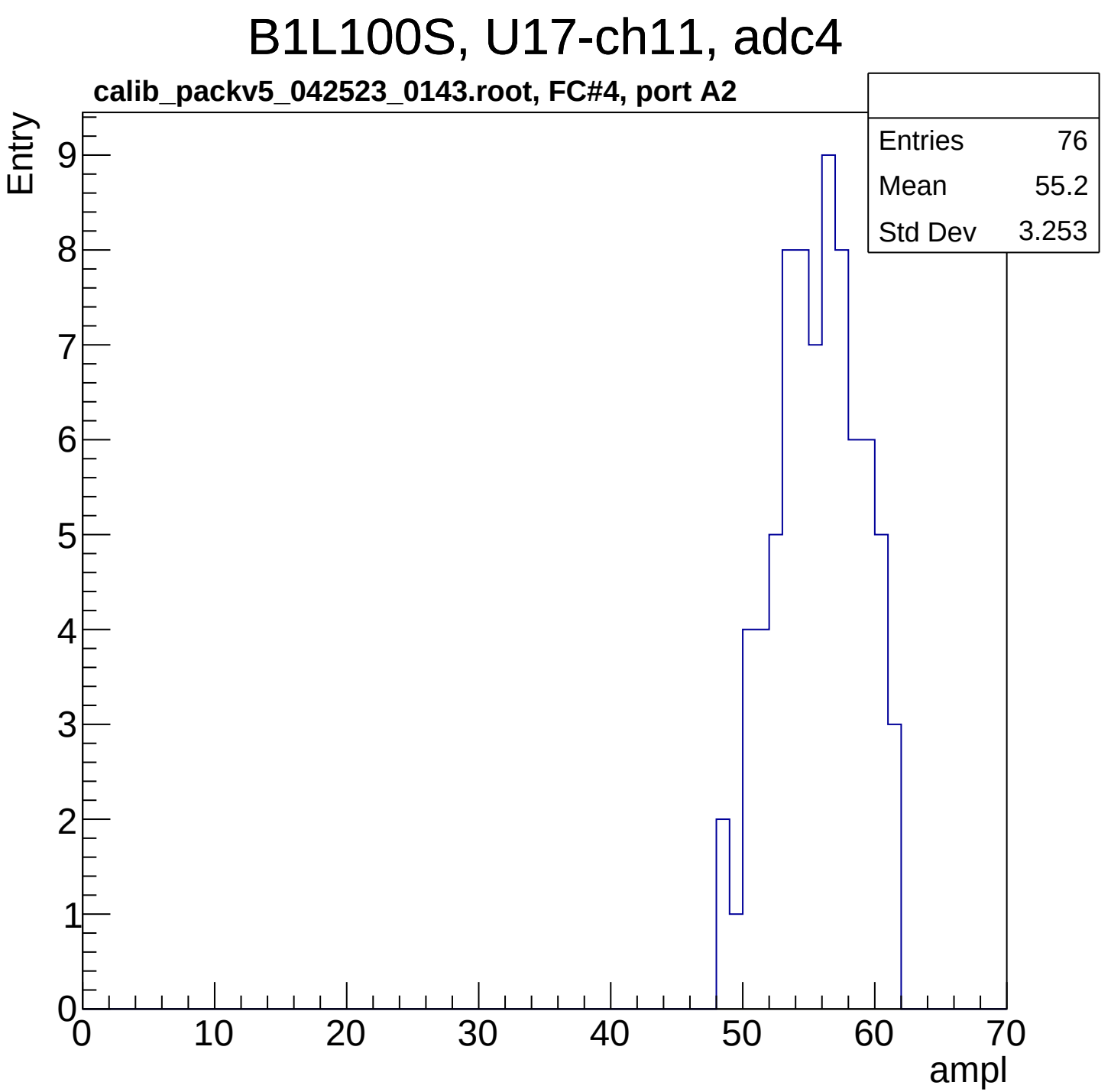
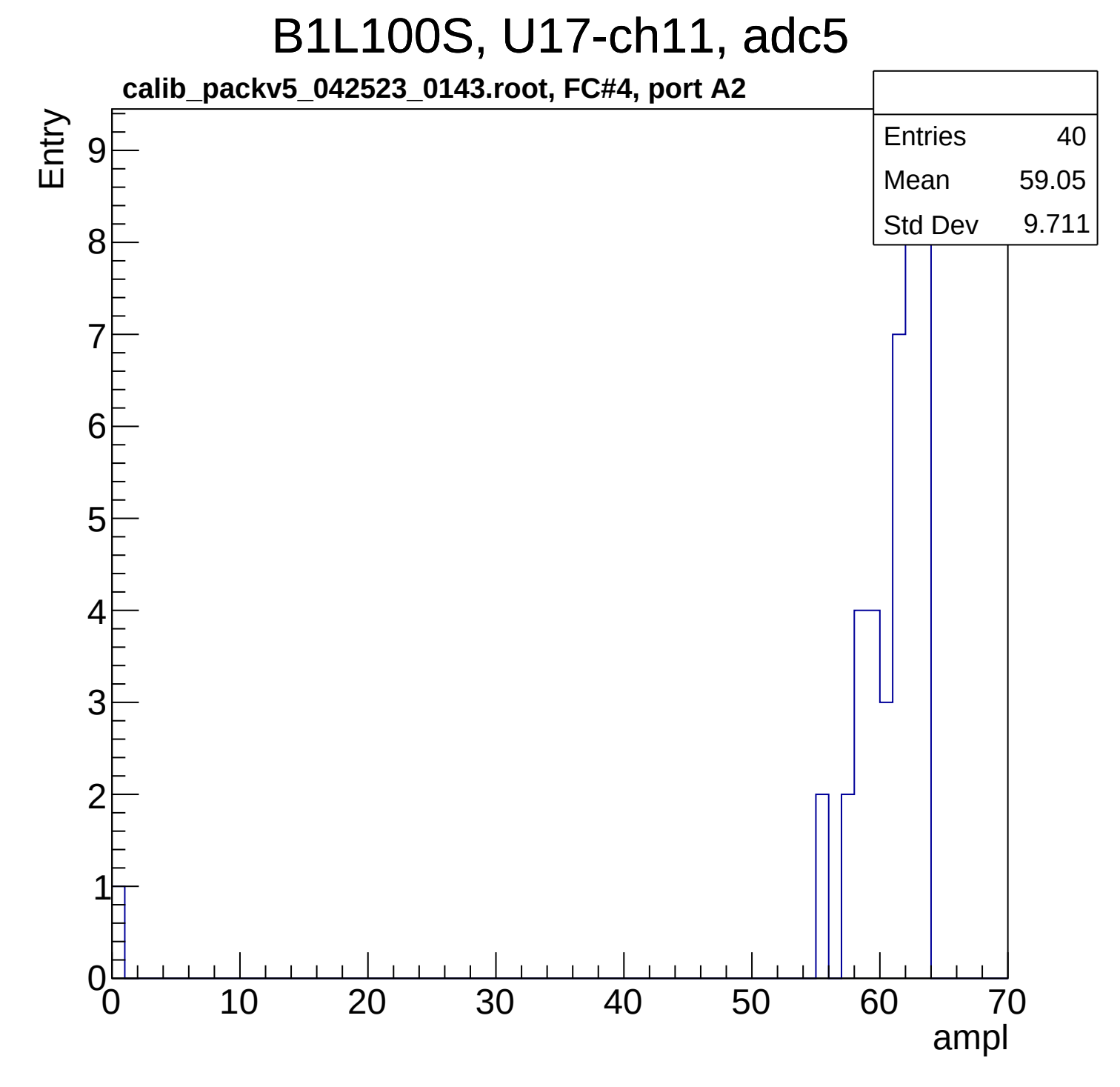

B1L100S, U17-ch11, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 76
Mean 55.2
Std Dev 3.253
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch11, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 40
Mean 59.05
Std Dev 9.711
Entry
ampl
0
1
2
3
4
5
6
7
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0
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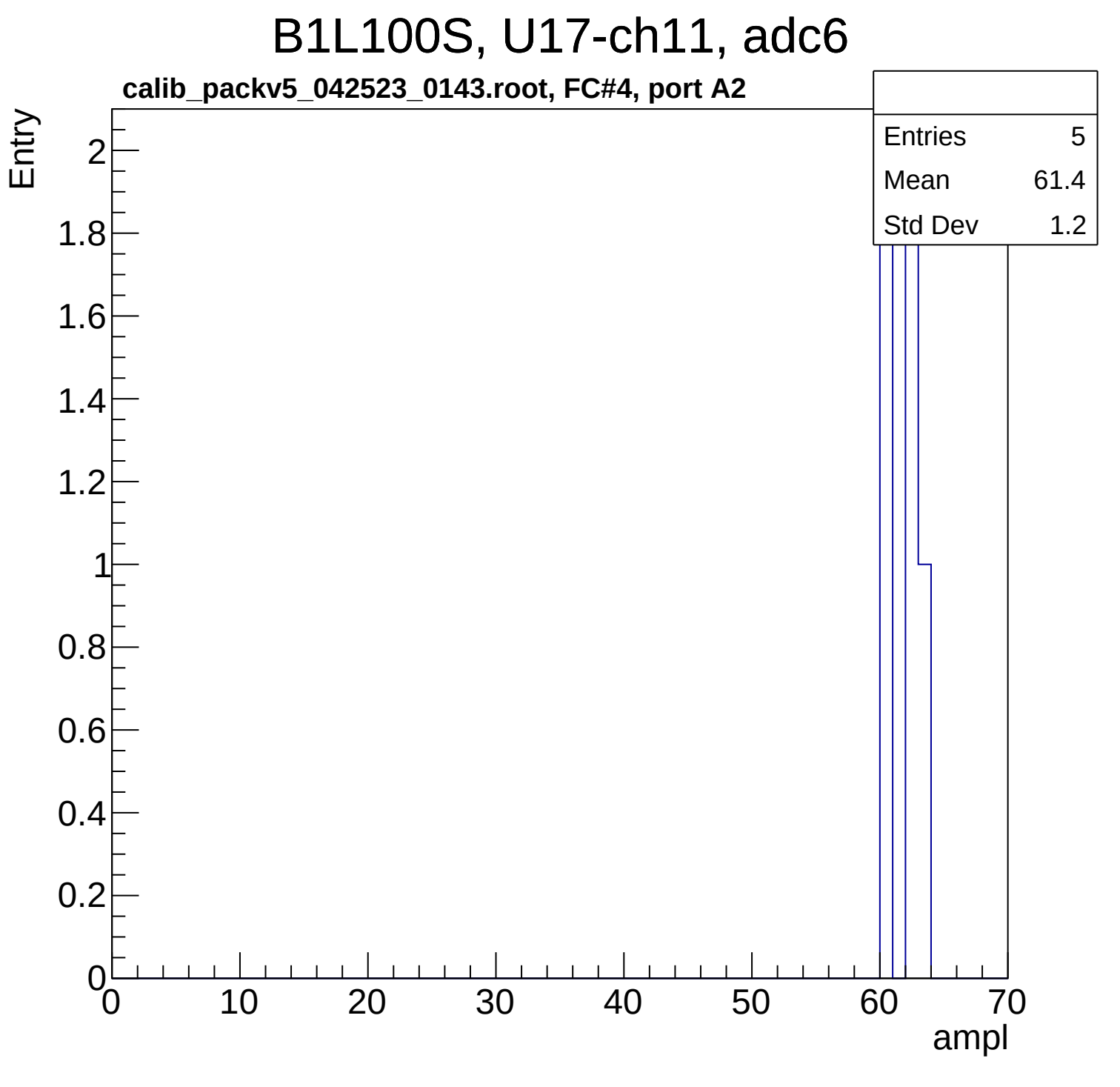
B1L100S, U17-ch11, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 5
Mean 61.4
Std Dev 1.2
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
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30
40
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60
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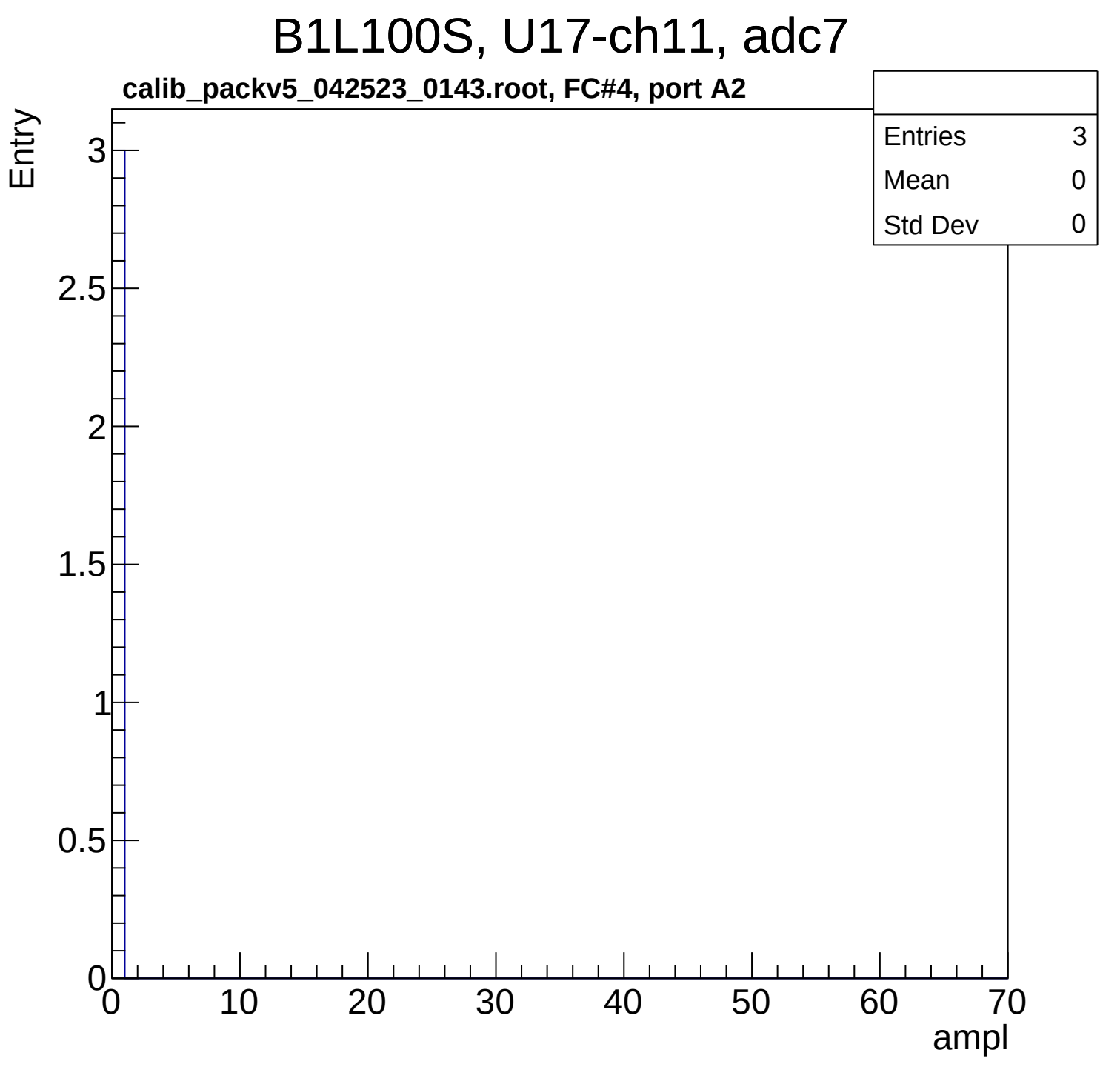
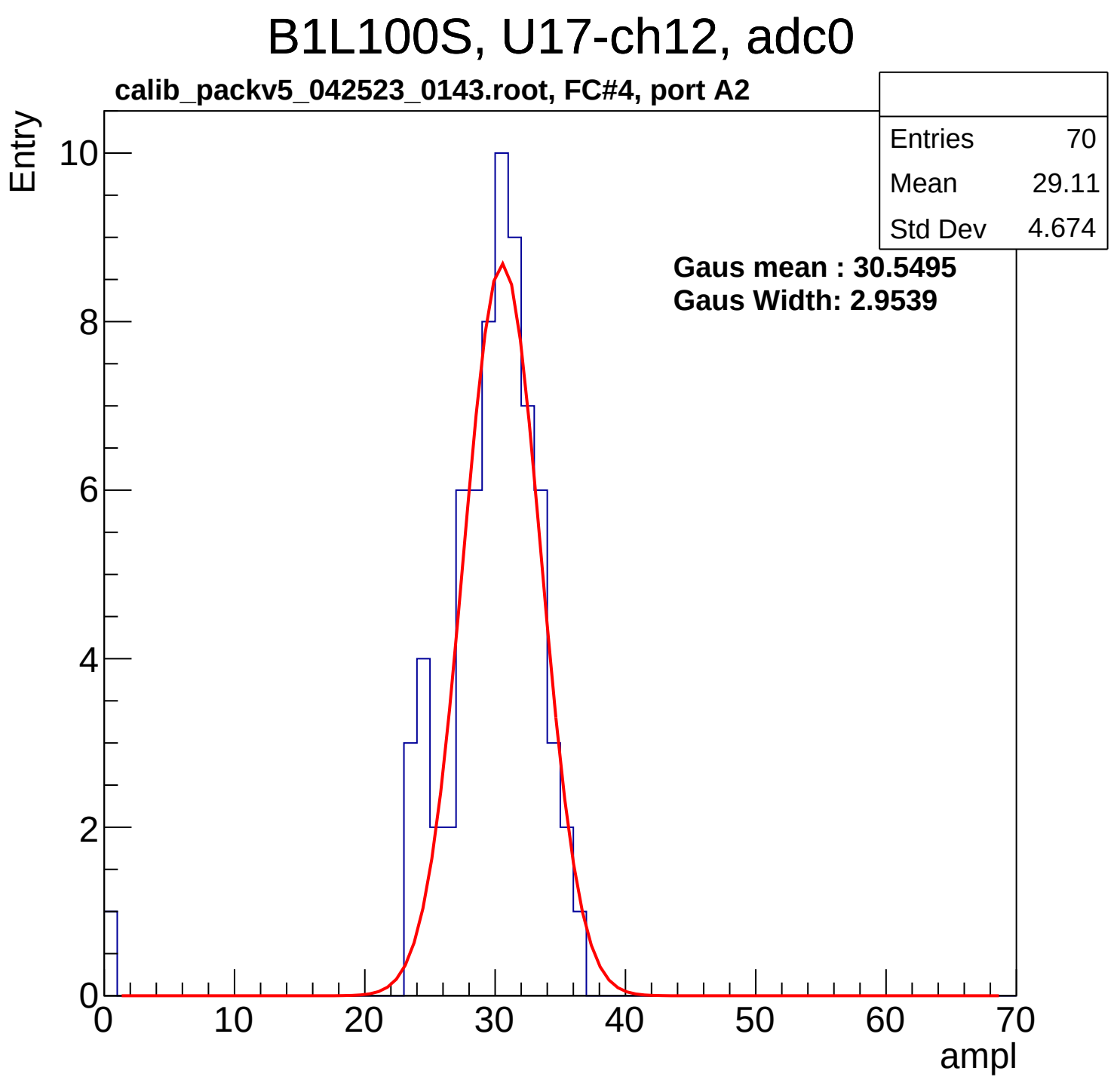
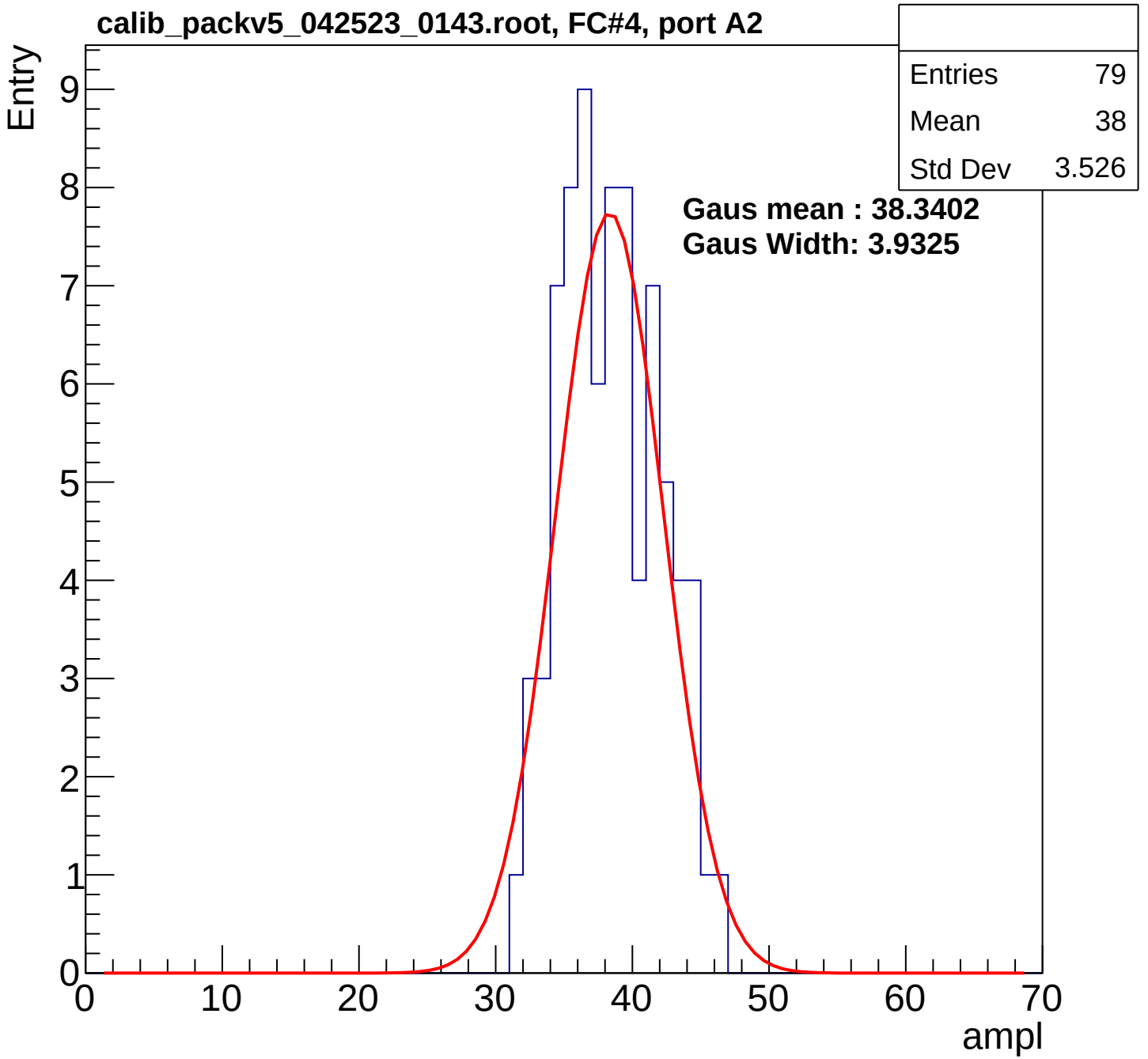

B1L100S, U17-ch11, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 0
Std Dev 0
Entry
3
2.5
2
1.5
1
0.5
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch12, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 29.11
Std Dev 4.674
Gaus mean : 30.5495
Gaus Width: 2.9539
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U17-ch12, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 79
Mean 38
Std Dev 3.526
Gaus mean : 38.3402
Gaus Width: 3.9325
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
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30
40
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60
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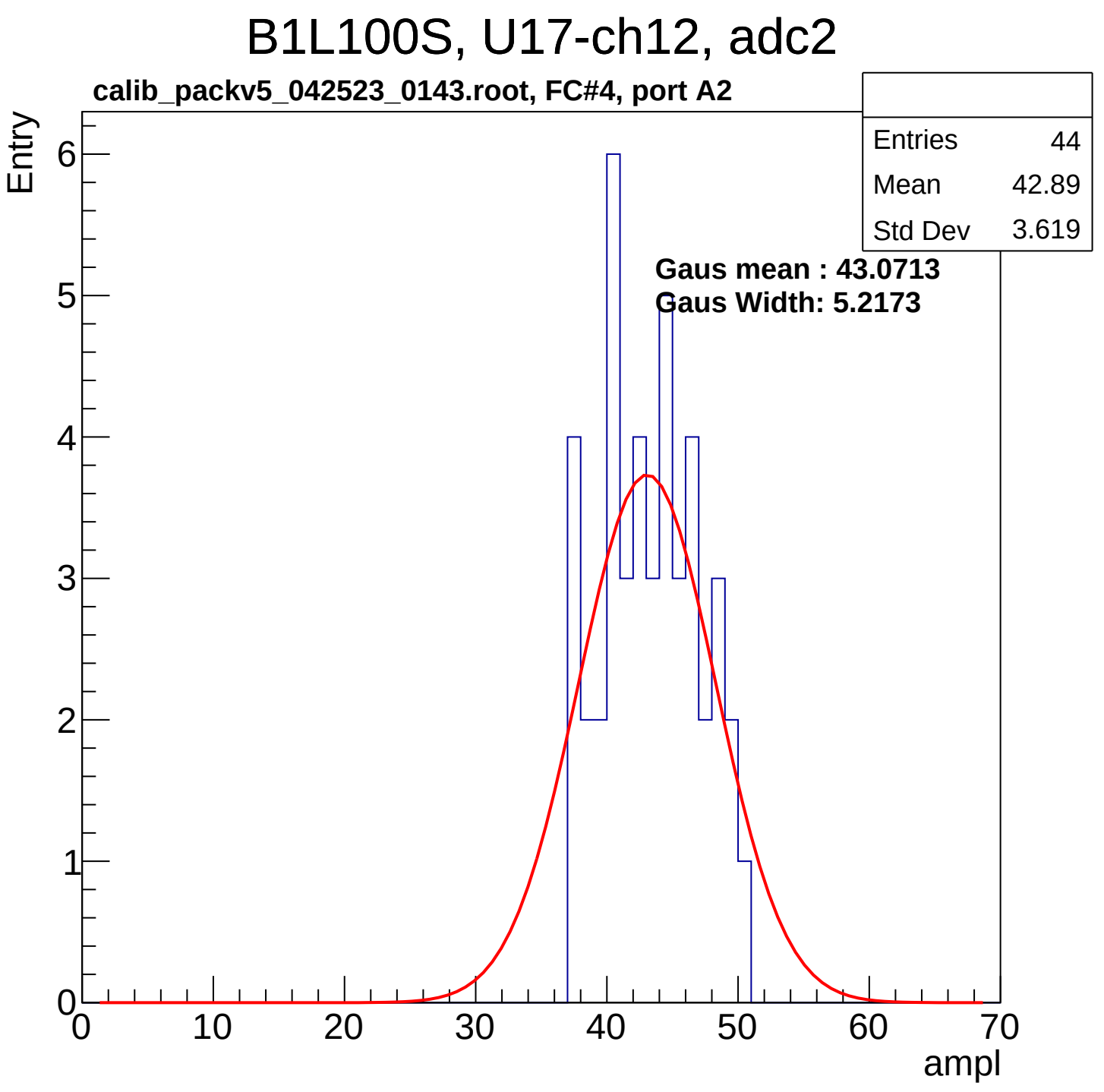
B1L100S, U17-ch12, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 44
Mean 42.89
Std Dev 3.619
Gaus mean : 43.0713
Gaus Width: 5.2173
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
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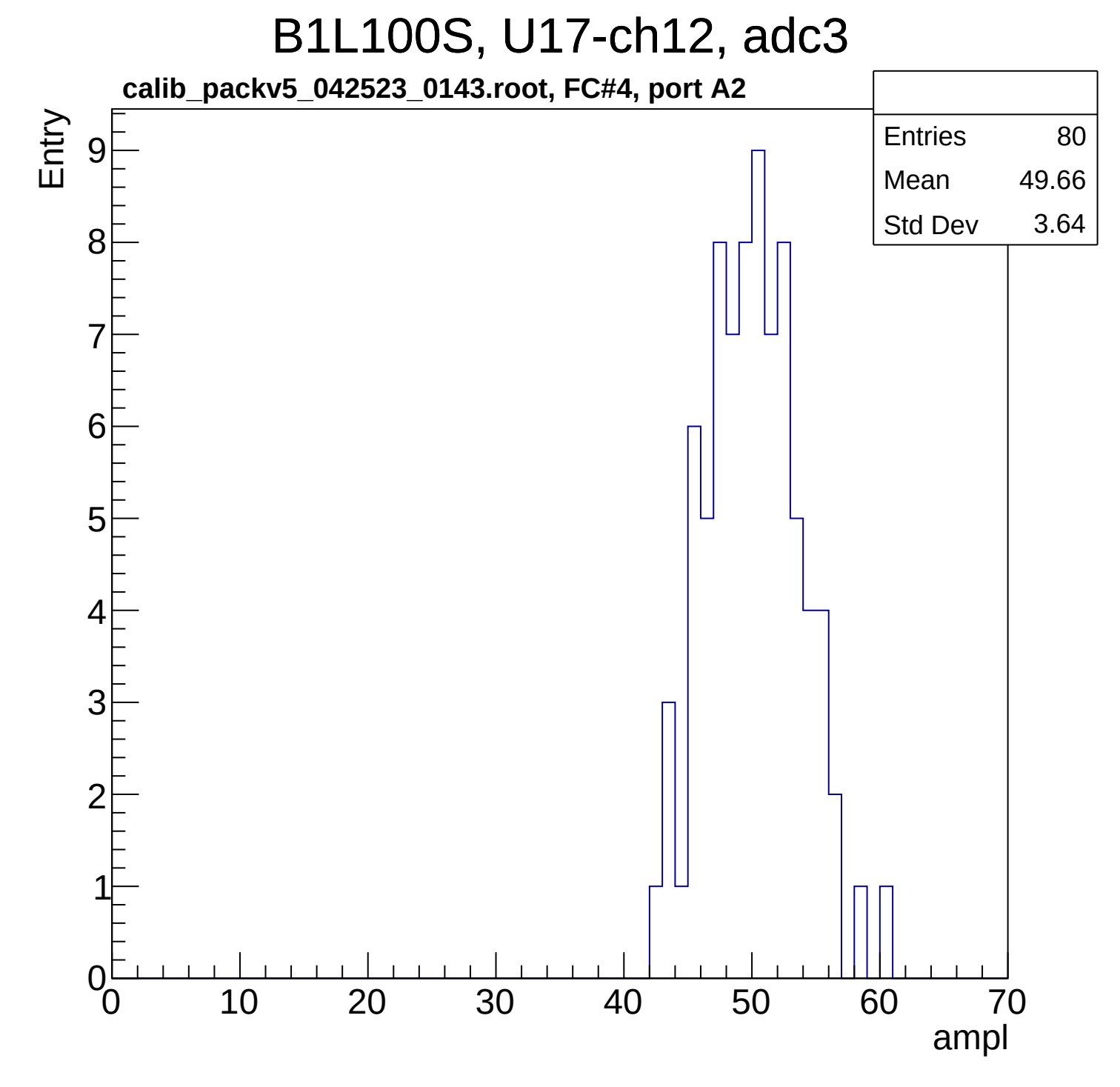
B1L100S, U17-ch12, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 80
Mean 49.66
Std Dev 3.64
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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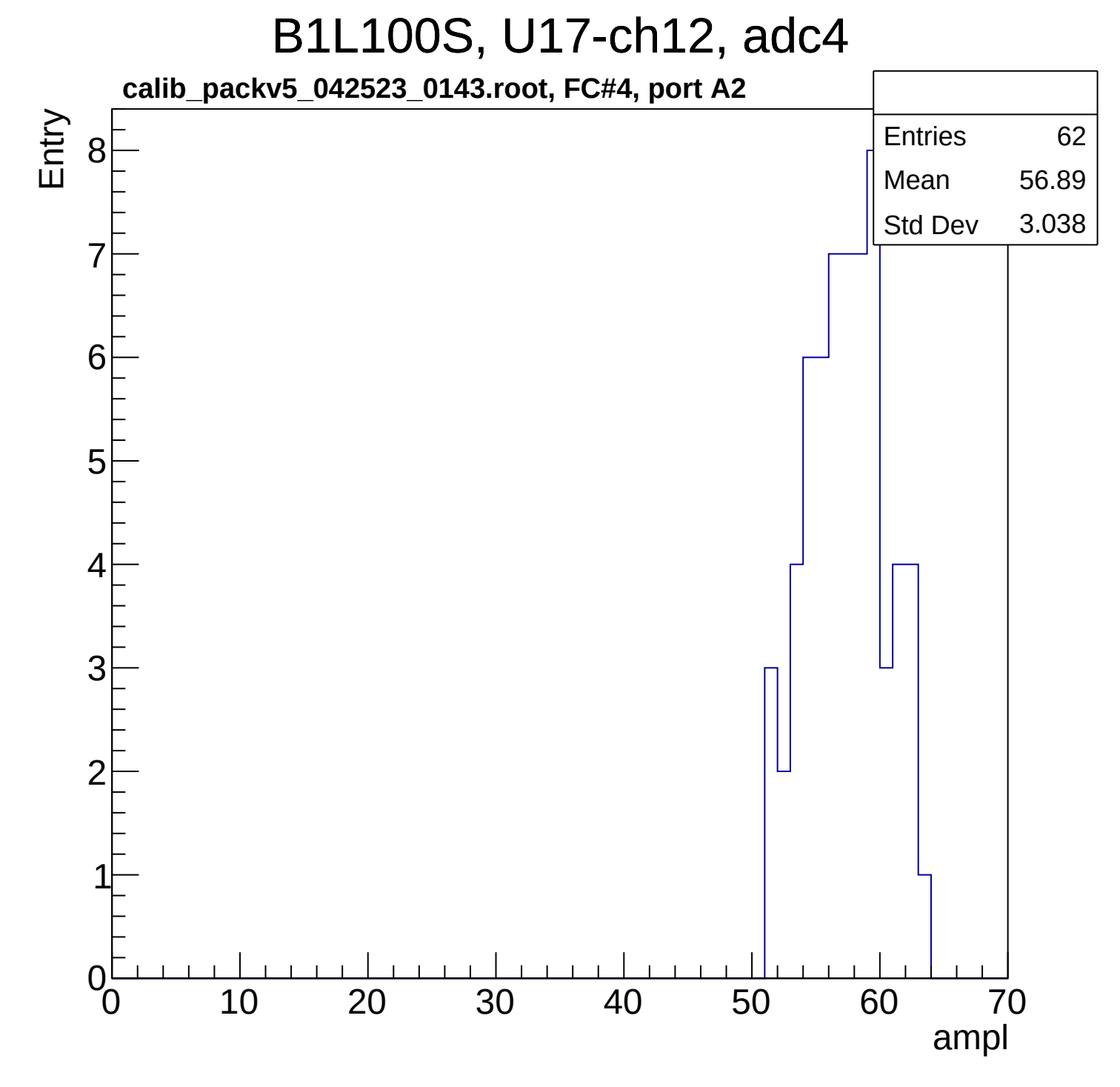
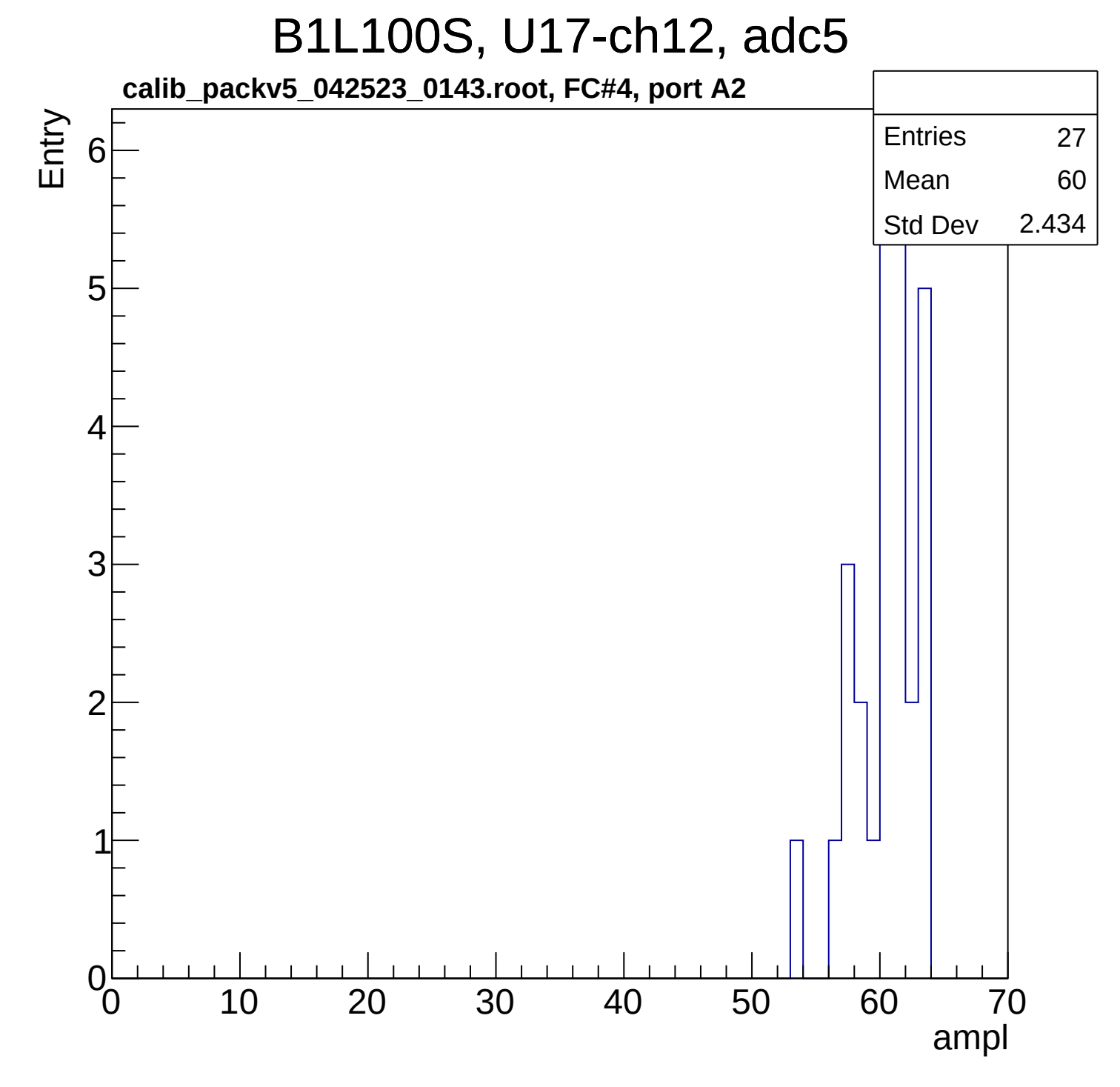
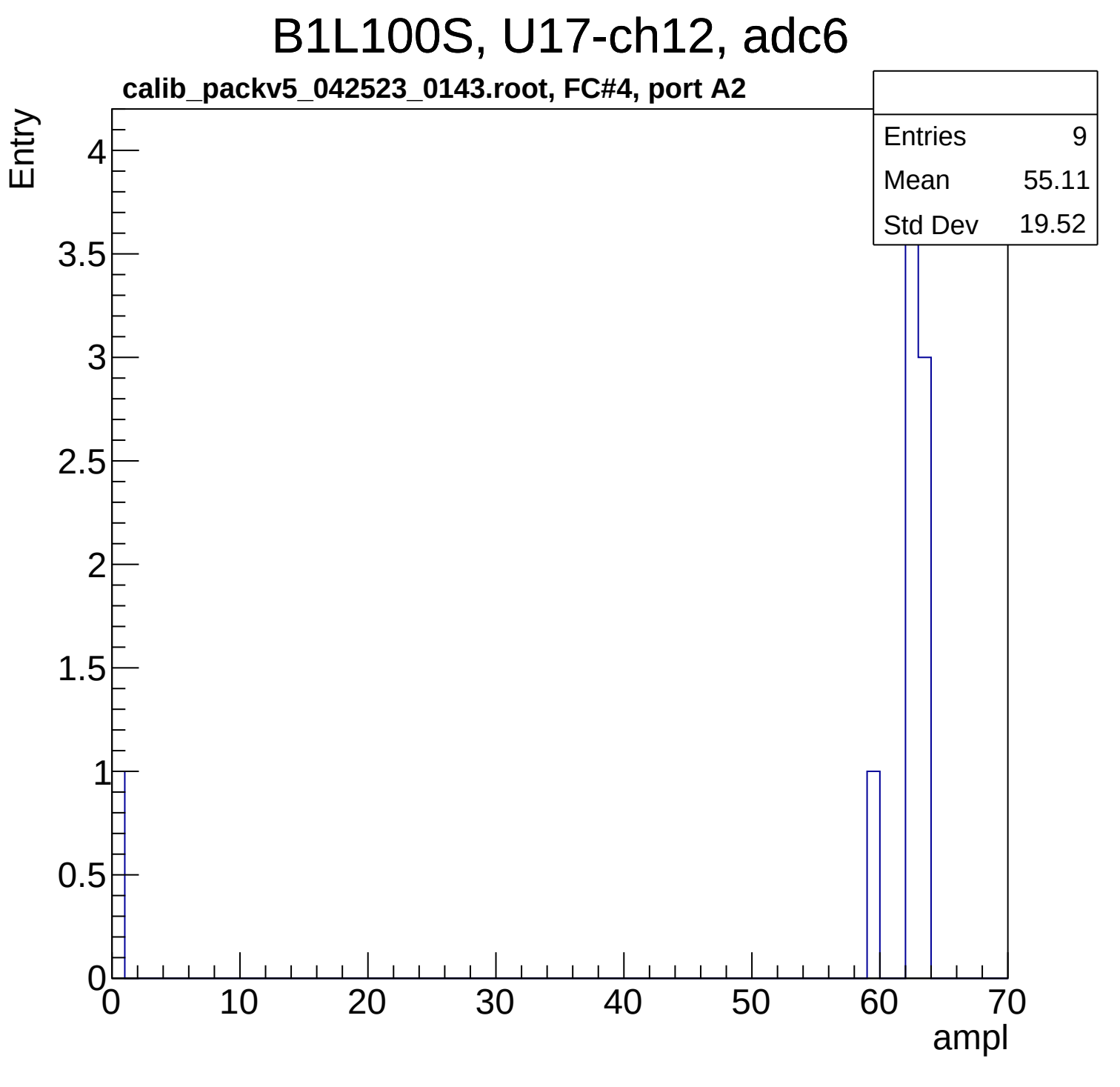
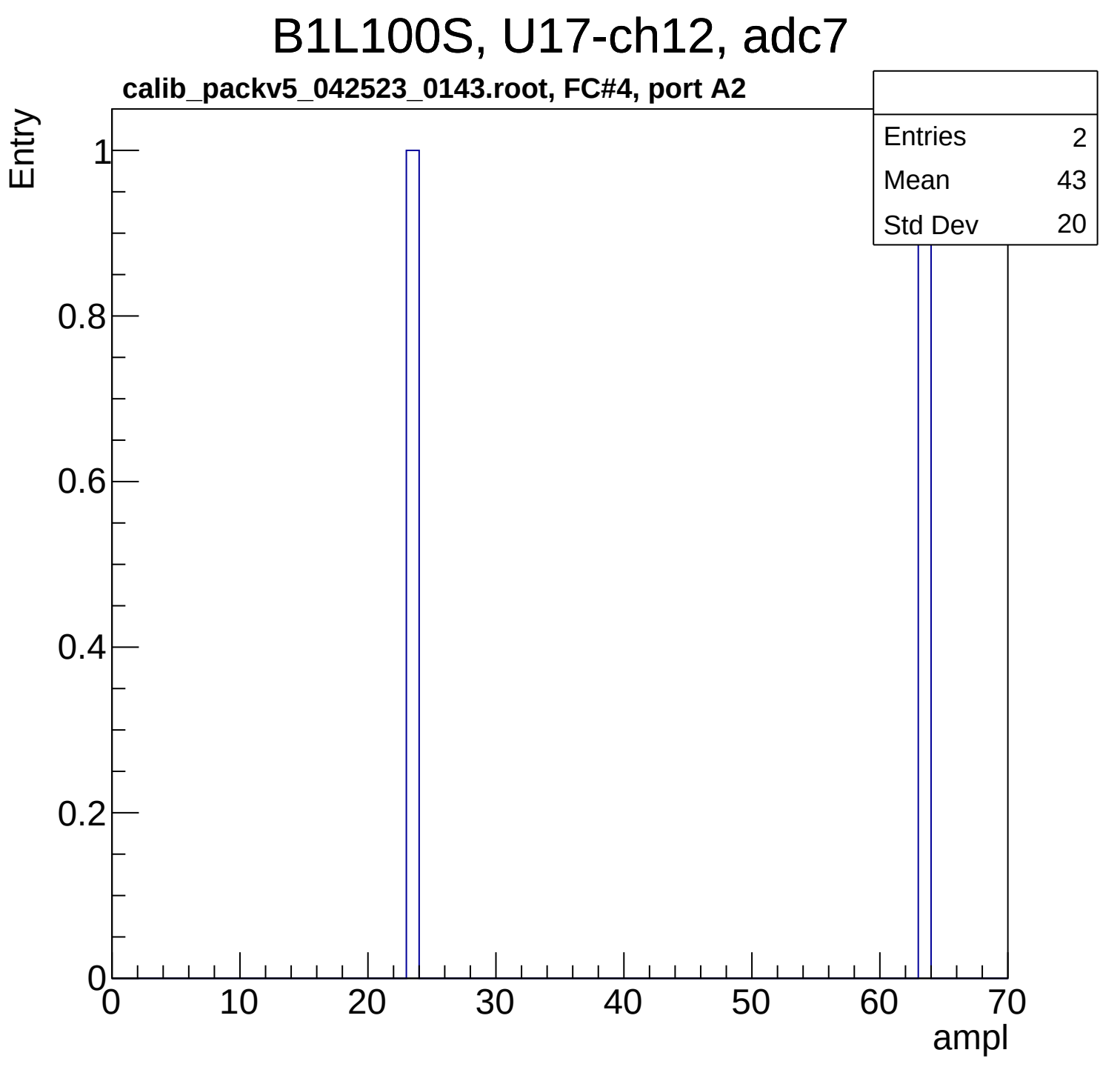
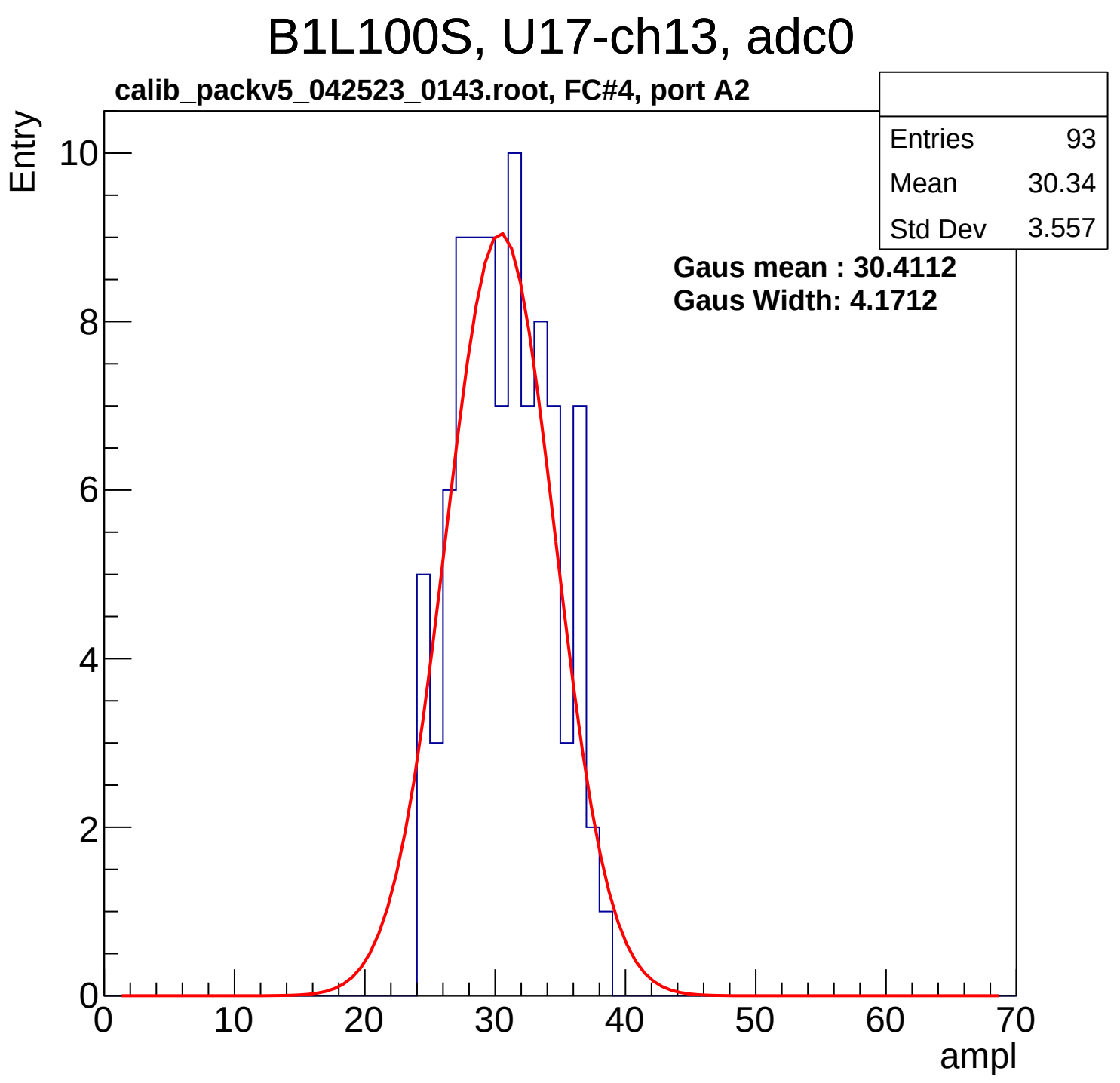
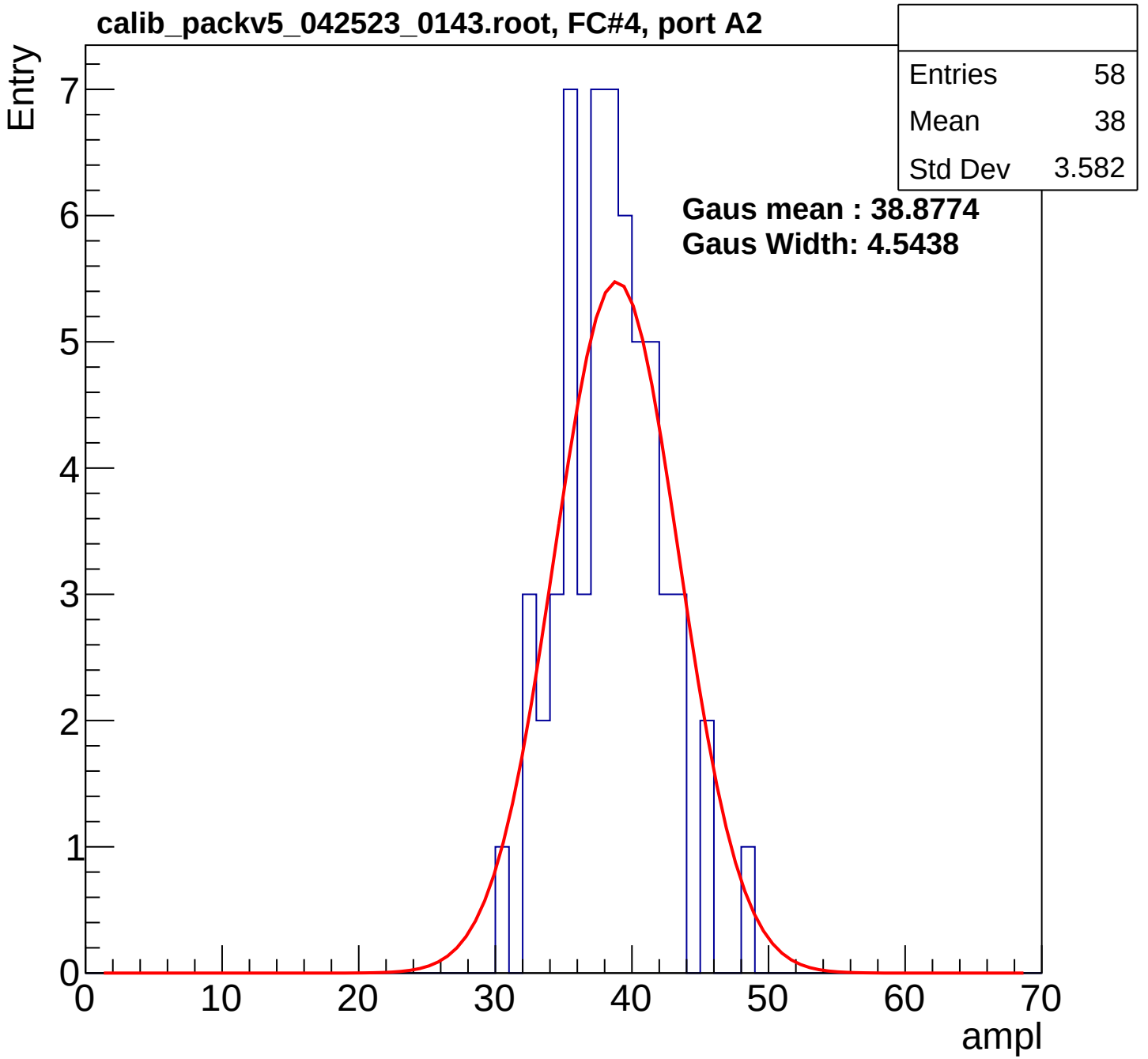

B1L100S, U17-ch12, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 56.89
Std Dev 3.038
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

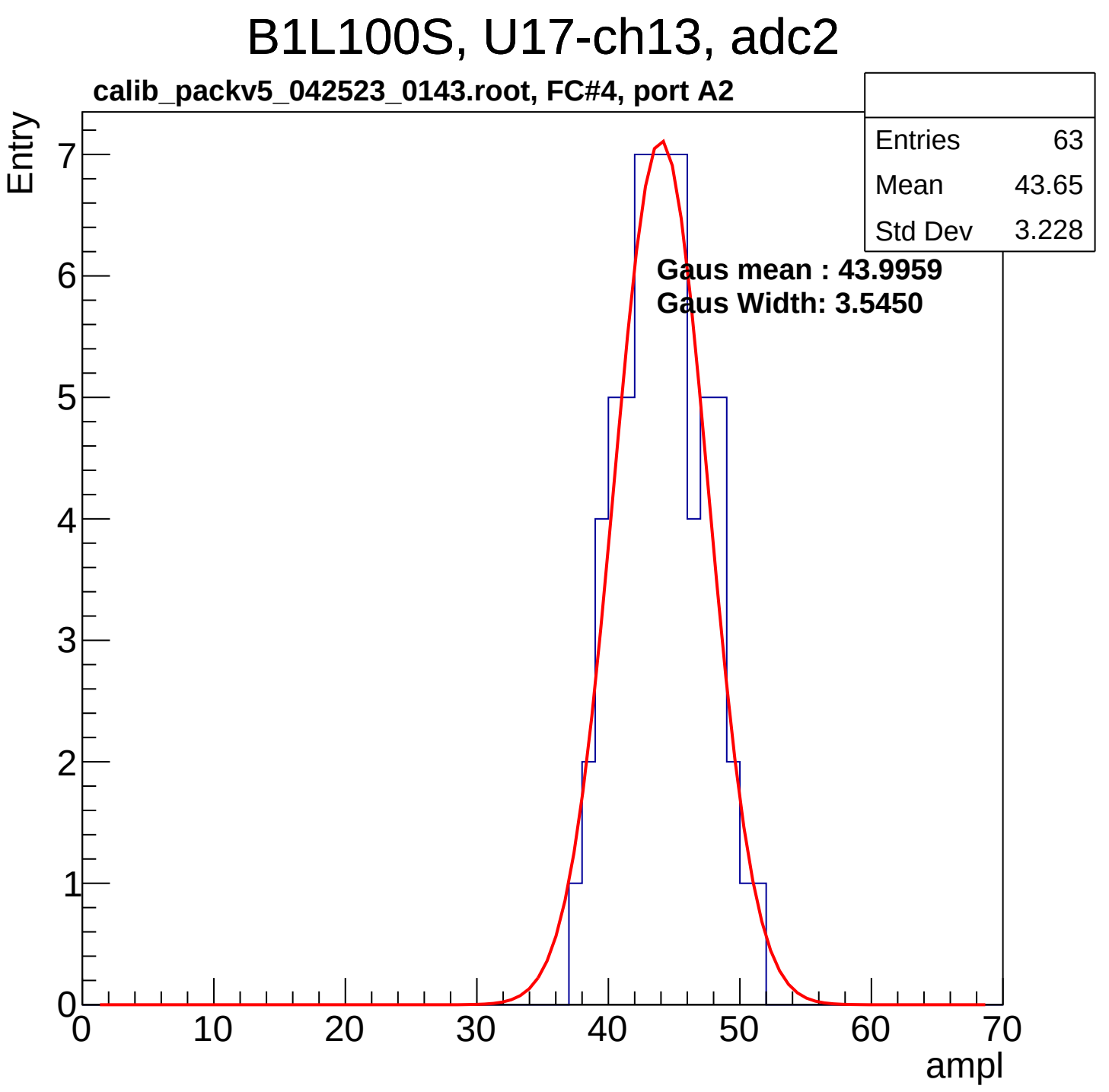

B1L100S, U17-ch12, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 27
Mean 60
Std Dev 2.434
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

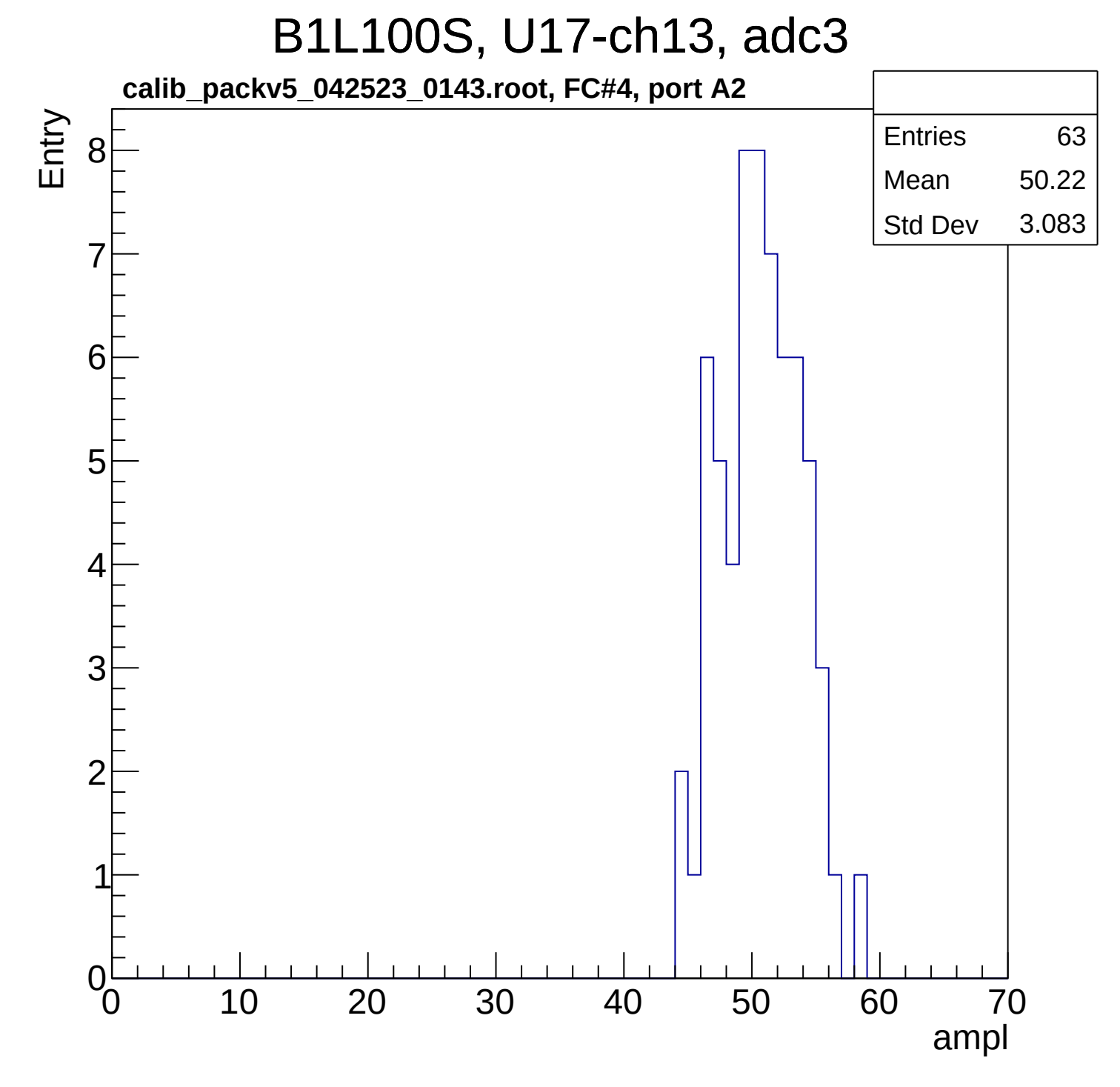

B1L100S, U17-ch12, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 9
Mean 55.11
Std Dev 19.52
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

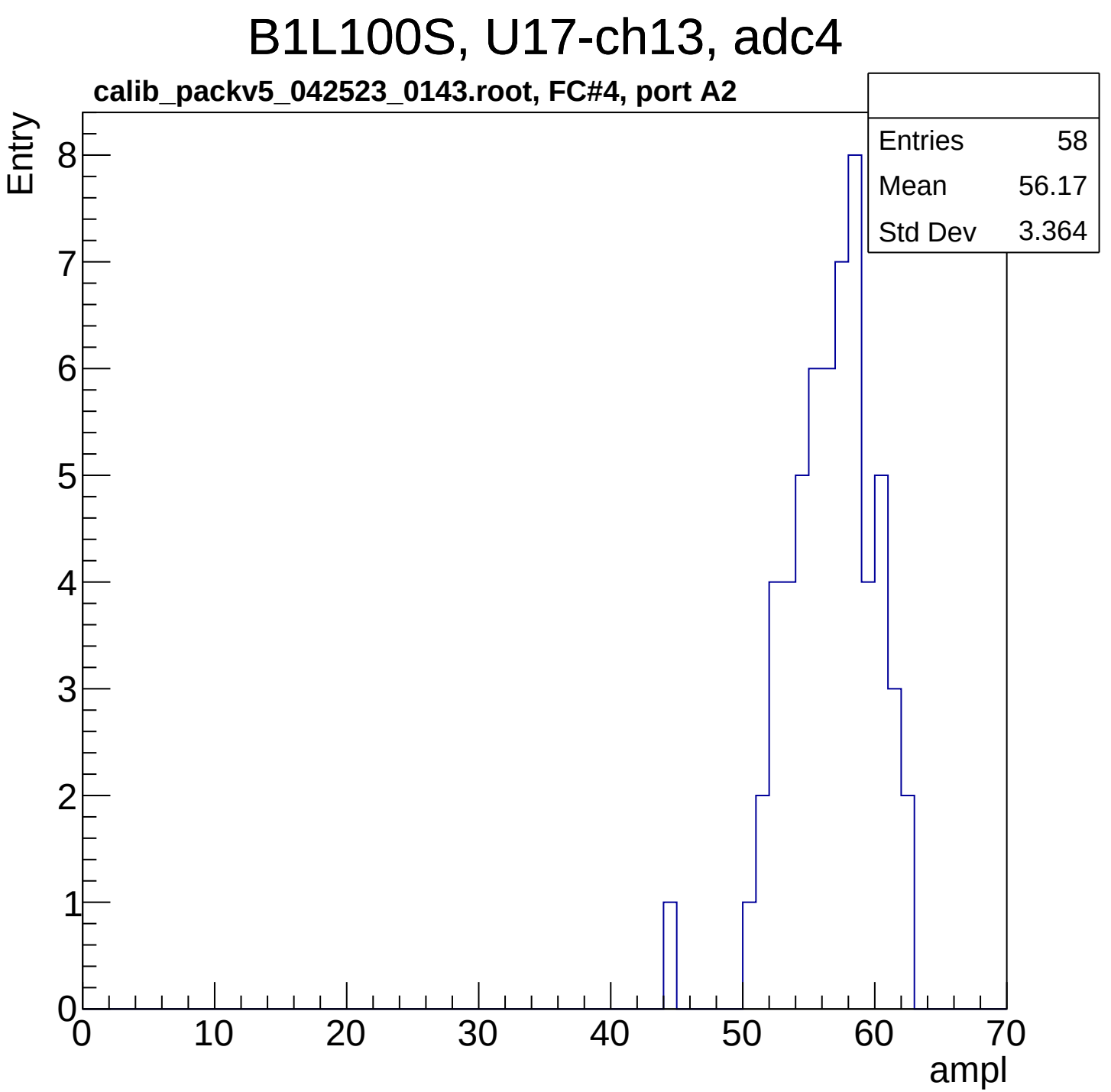

B1L100S, U17-ch12, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 43
Std Dev 20
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

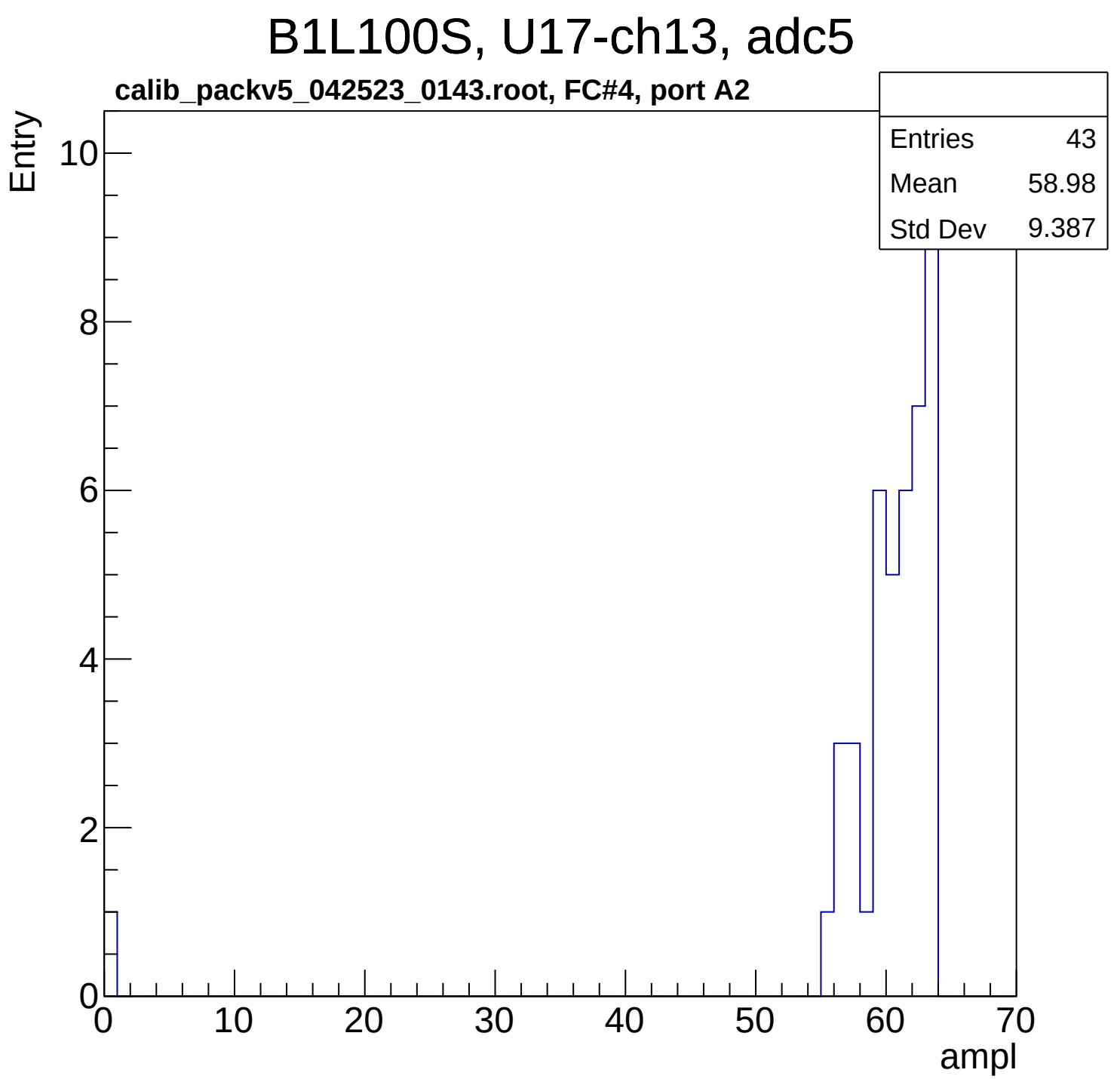

B1L100S, U17-ch13, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 93
Mean 30.34
Std Dev 3.557
Gaus mean : 30.4112
Gaus Width: 4.1712
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

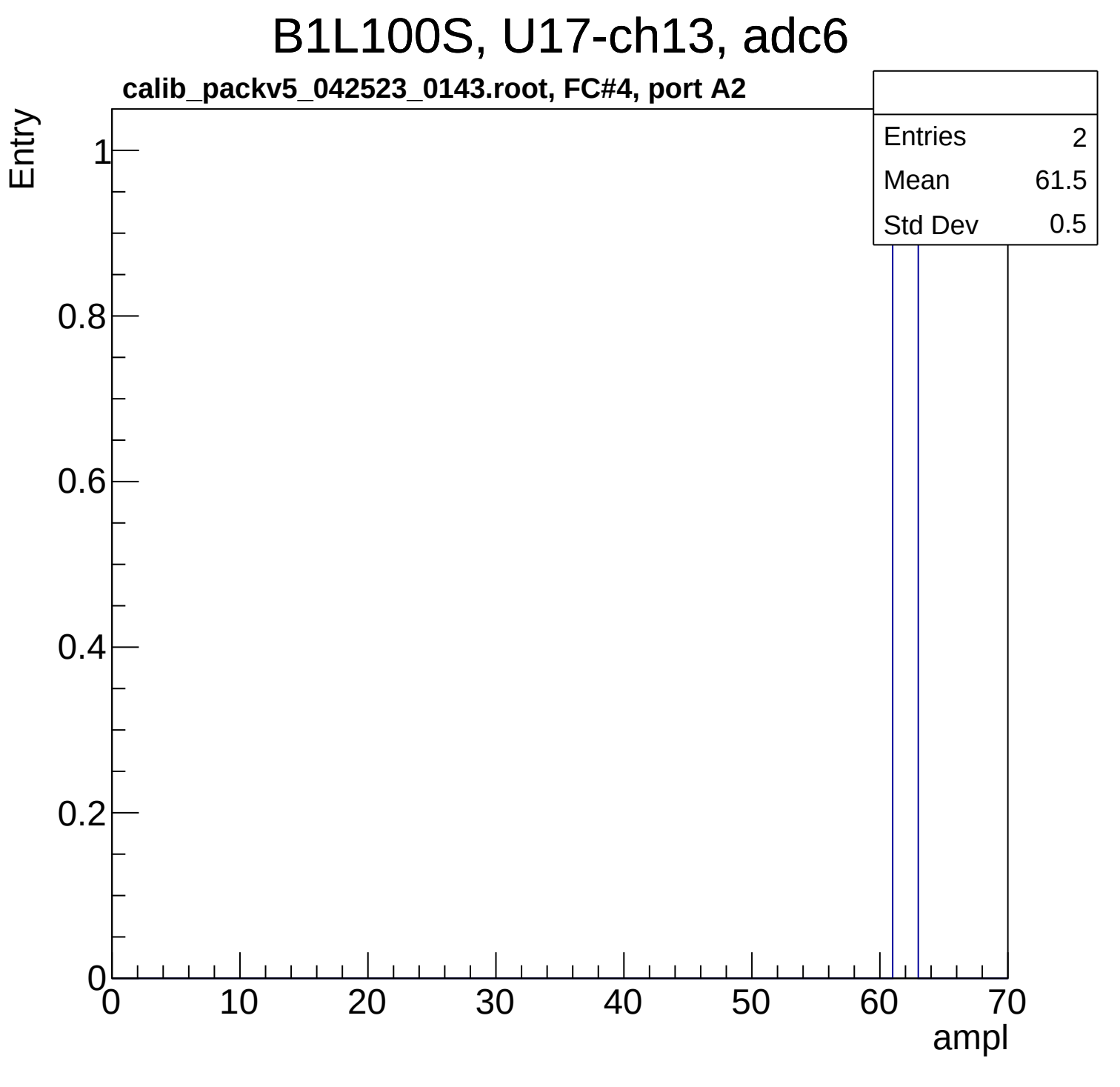

B1L100S, U17-ch13, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 38
Std Dev 3.582
Gaus mean : 38.8774
Gaus Width: 4.5438
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

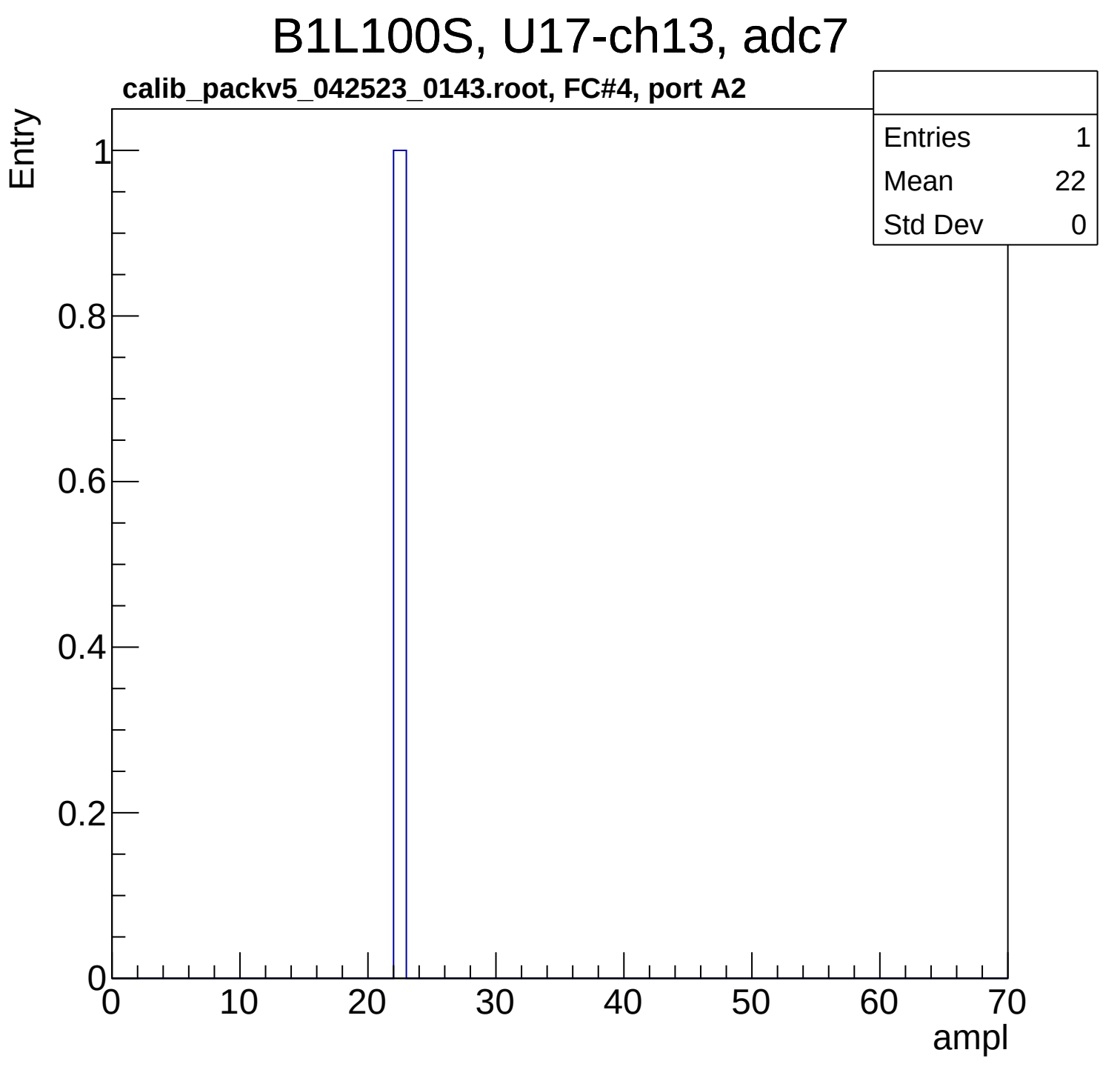

B1L100S, U17-ch13, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 43.65
Std Dev 3.228
Gaus mean : 43.9959
Gaus Width: 3.5450
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

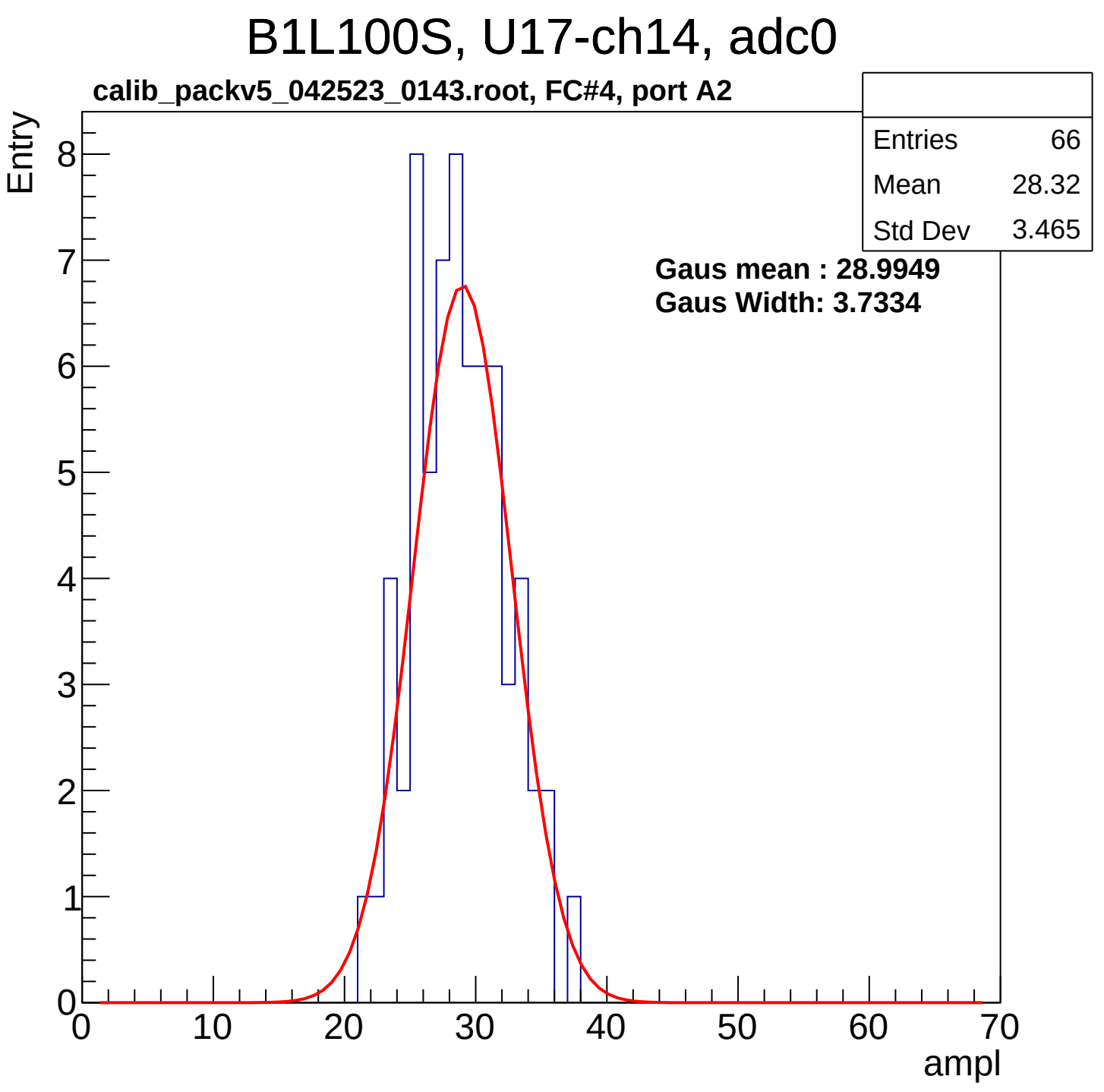

B1L100S, U17-ch13, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 50.22
Std Dev 3.083
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

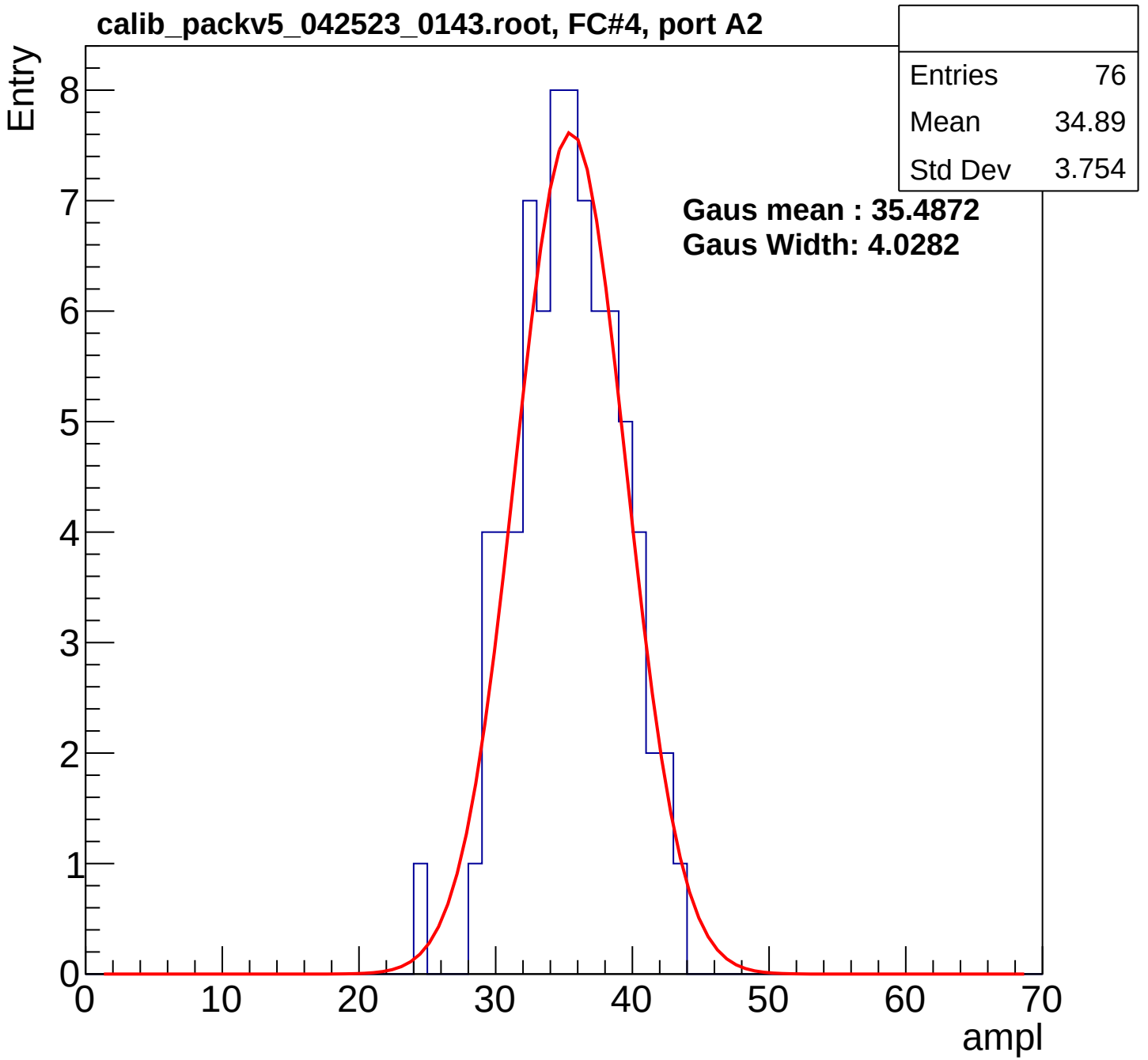

B1L100S, U17-ch13, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 56.17
Std Dev 3.364
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

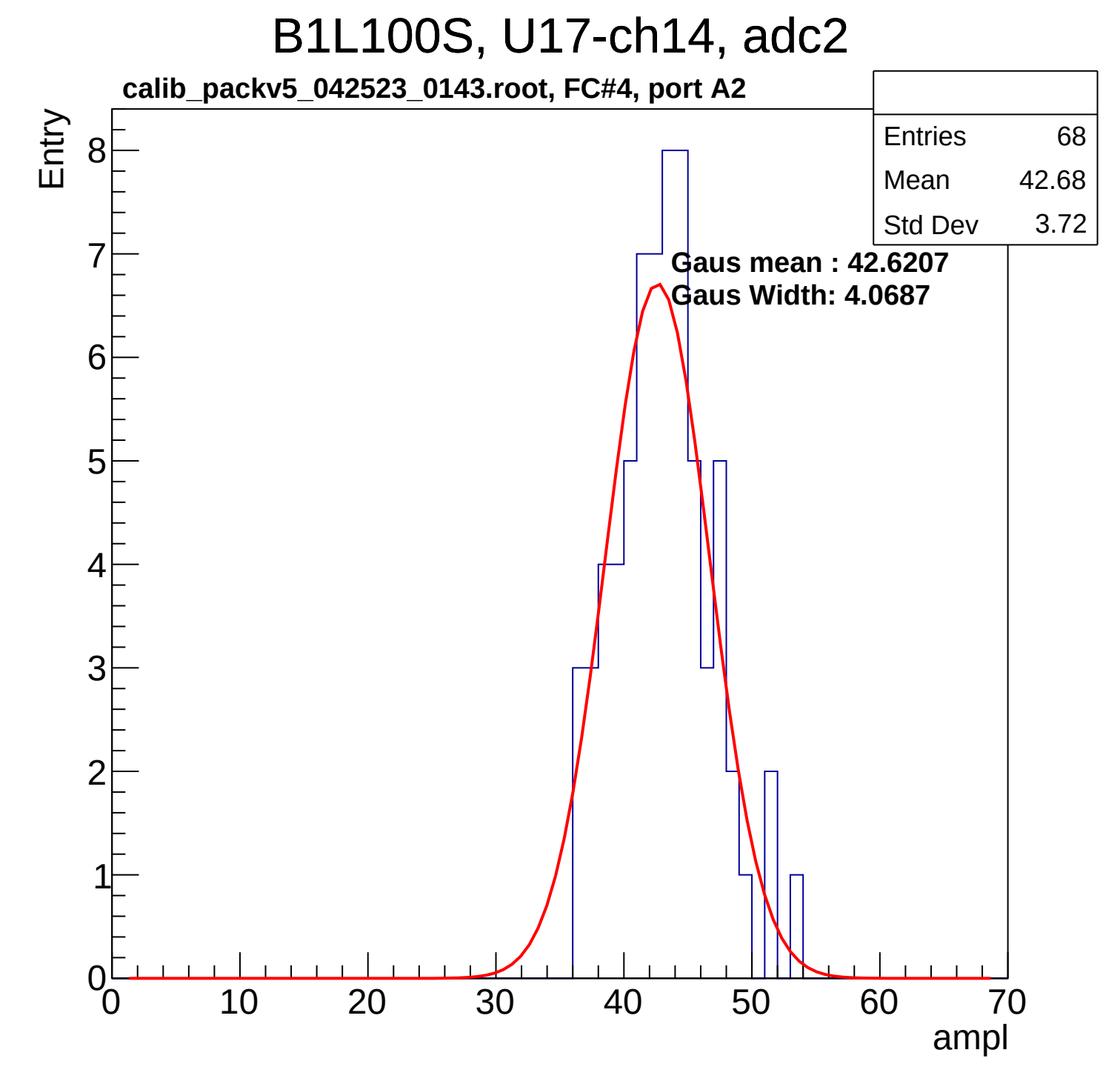

B1L100S, U17-ch13, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 43
Mean 58.98
Std Dev 9.387
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

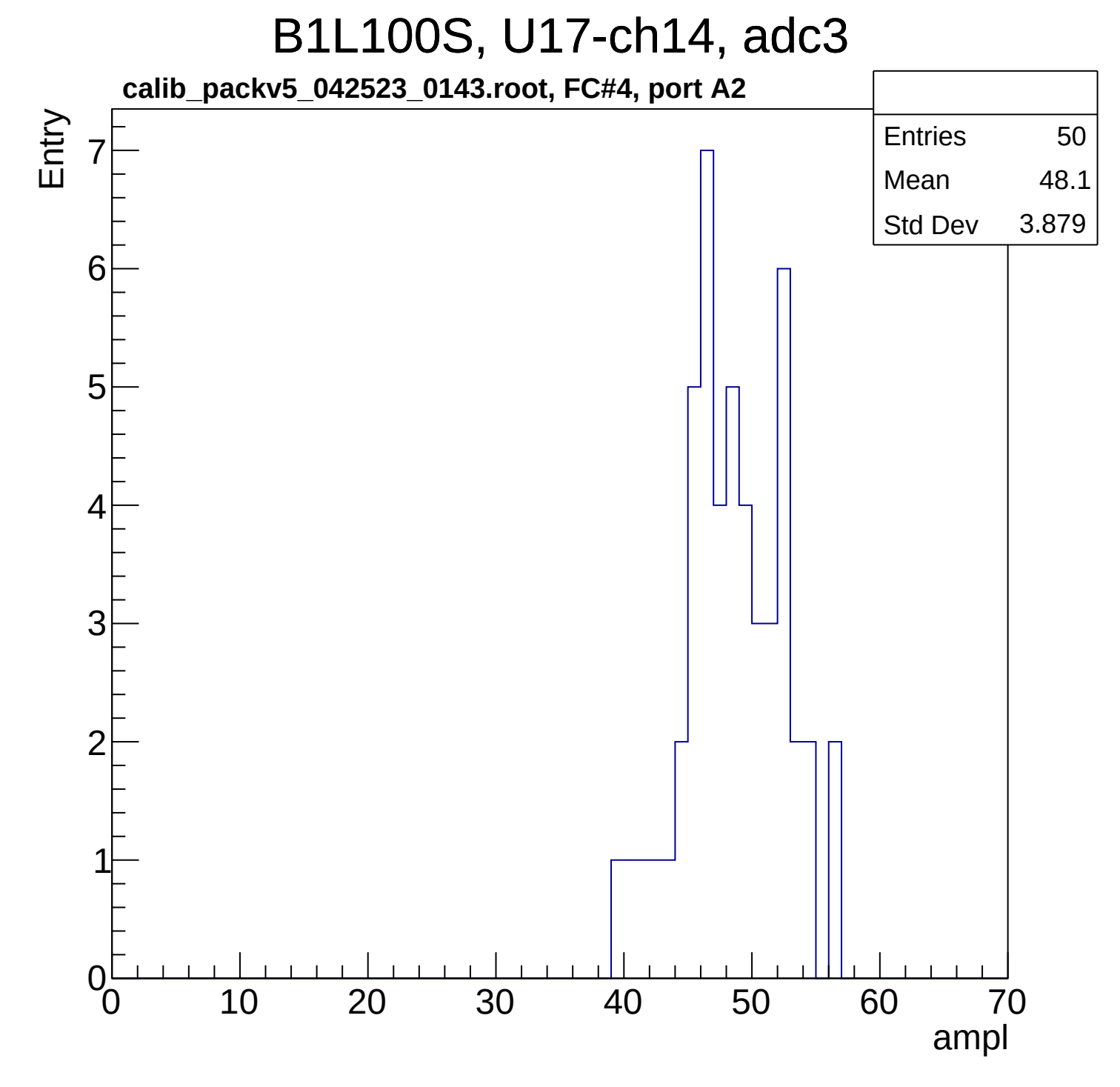

B1L100S, U17-ch13, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 61.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch13, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 22
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch14, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 28.32
Std Dev 3.465
Gaus mean : 28.9949
Gaus Width: 3.7334
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch14, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 76
Mean 34.89
Std Dev 3.754
Gaus mean : 35.4872
Gaus Width: 4.0282
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch14, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 42.68
Std Dev 3.72
Gaus mean : 42.6207
Gaus Width: 4.0687
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch14, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 48.1
Std Dev 3.879
Entry
ampl
0
1
2
3
4
5
6
7
0
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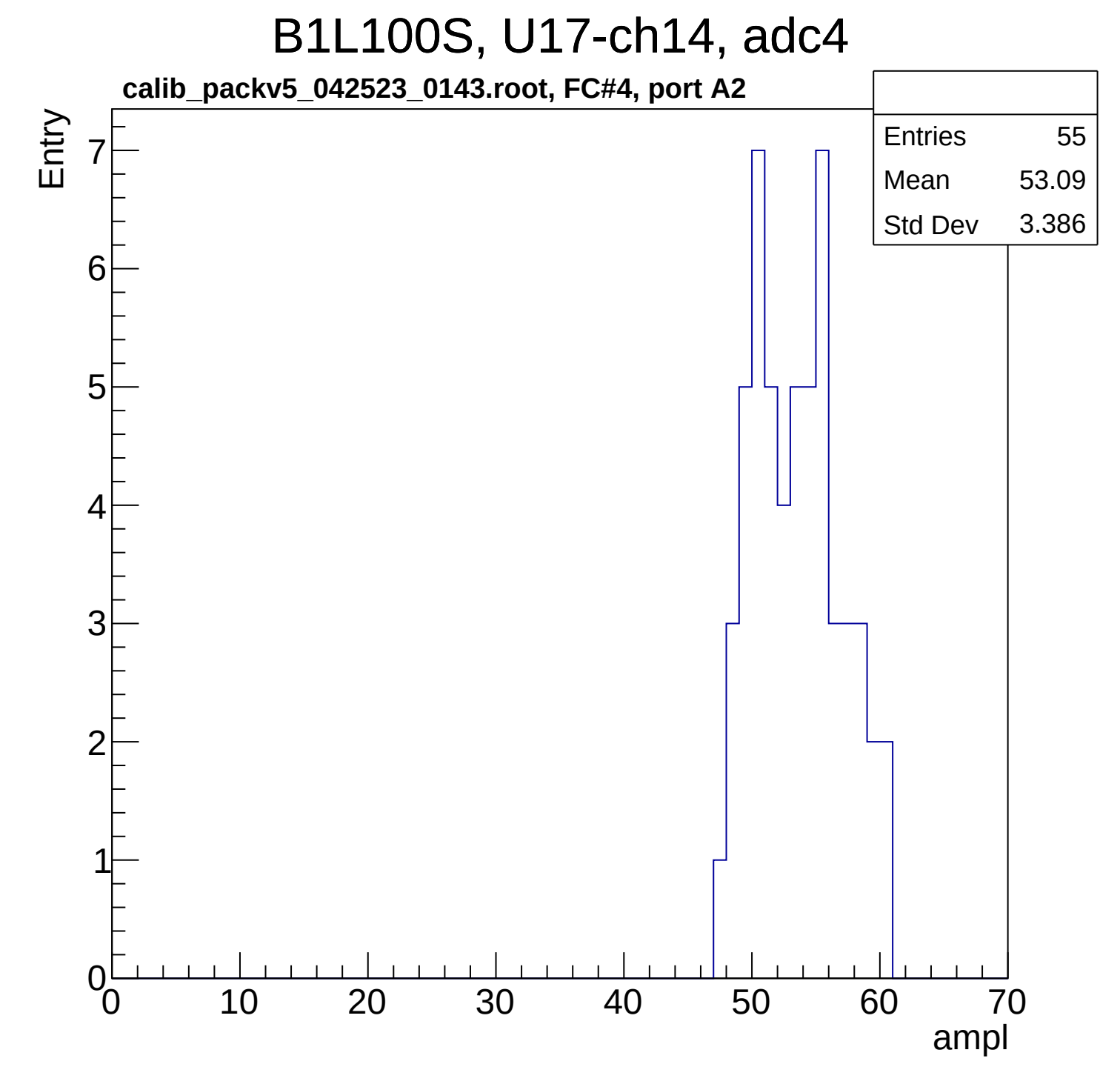
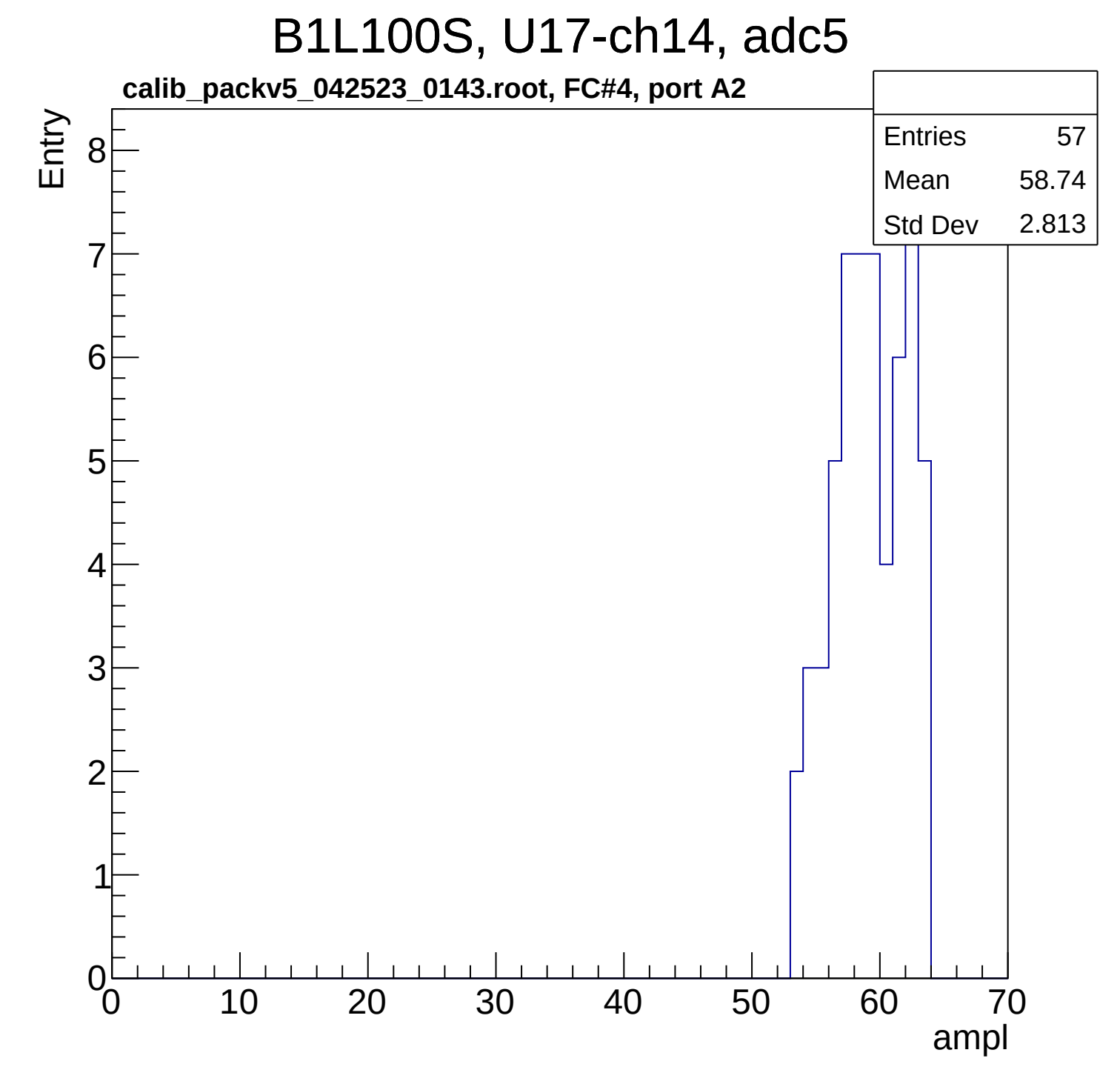
20
30
40
50
60
70


B1L100S, U17-ch14, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 53.09
Std Dev 3.386
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U17-ch14, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 58.74
Std Dev 2.813
Entry
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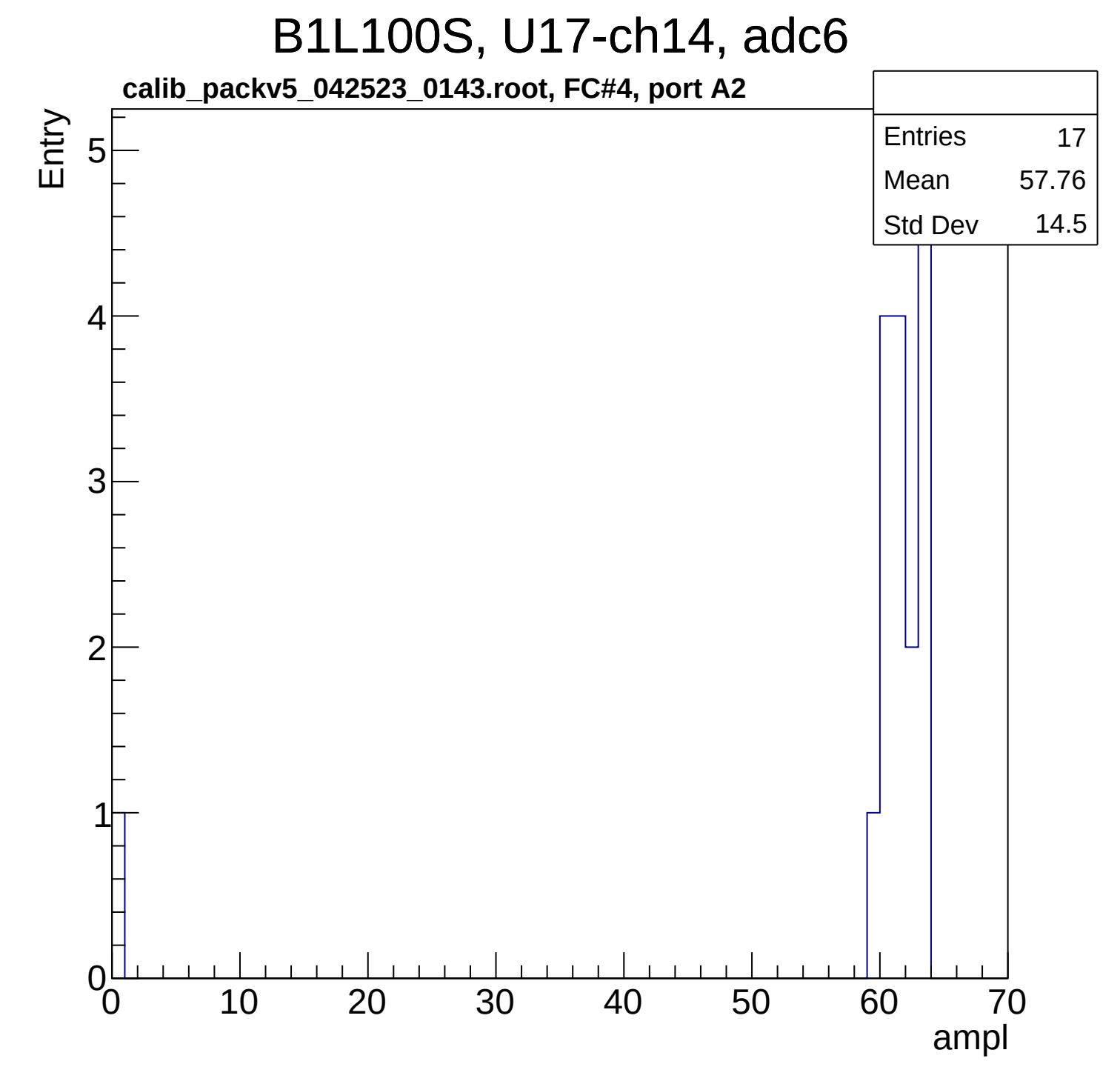
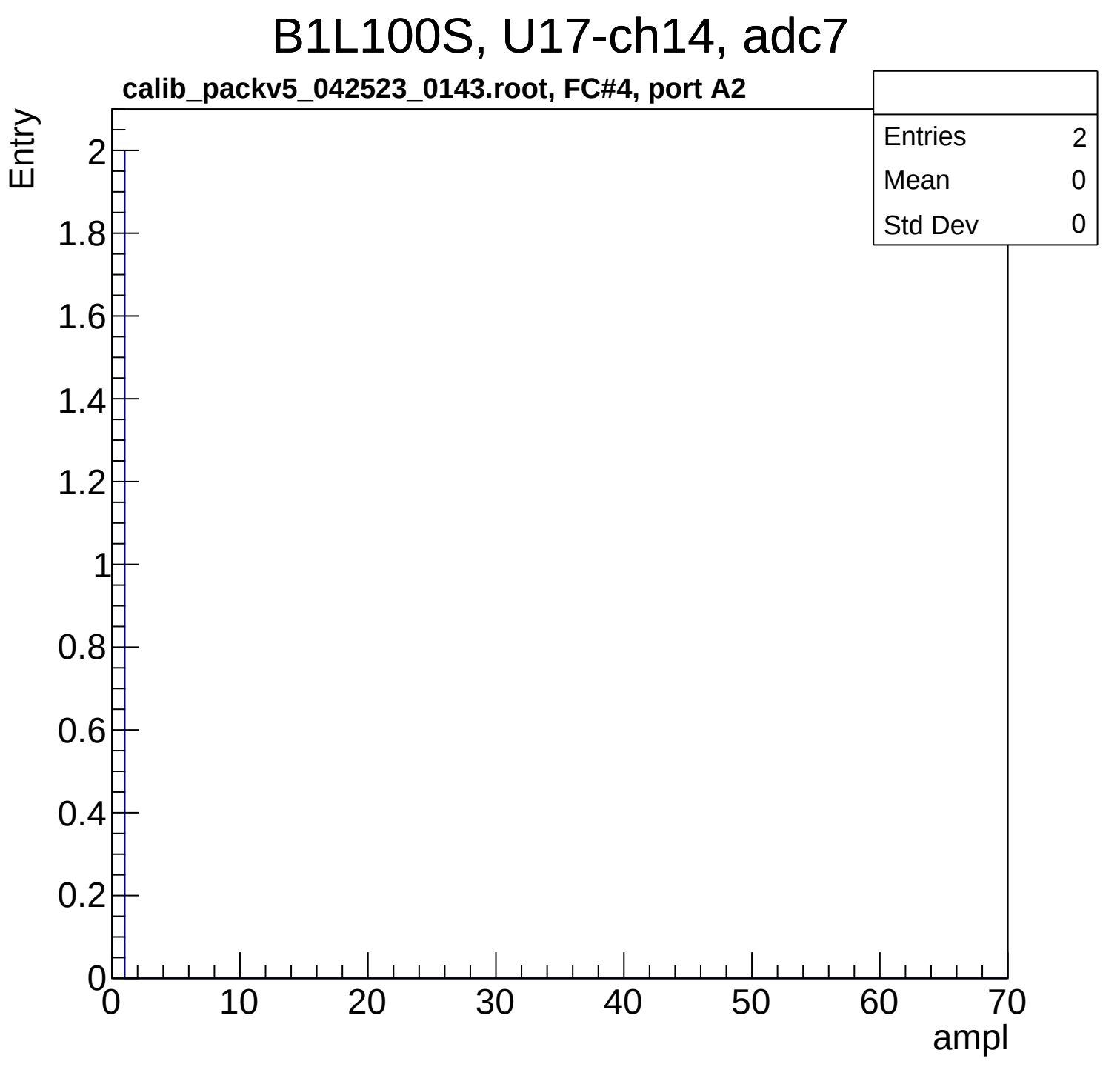
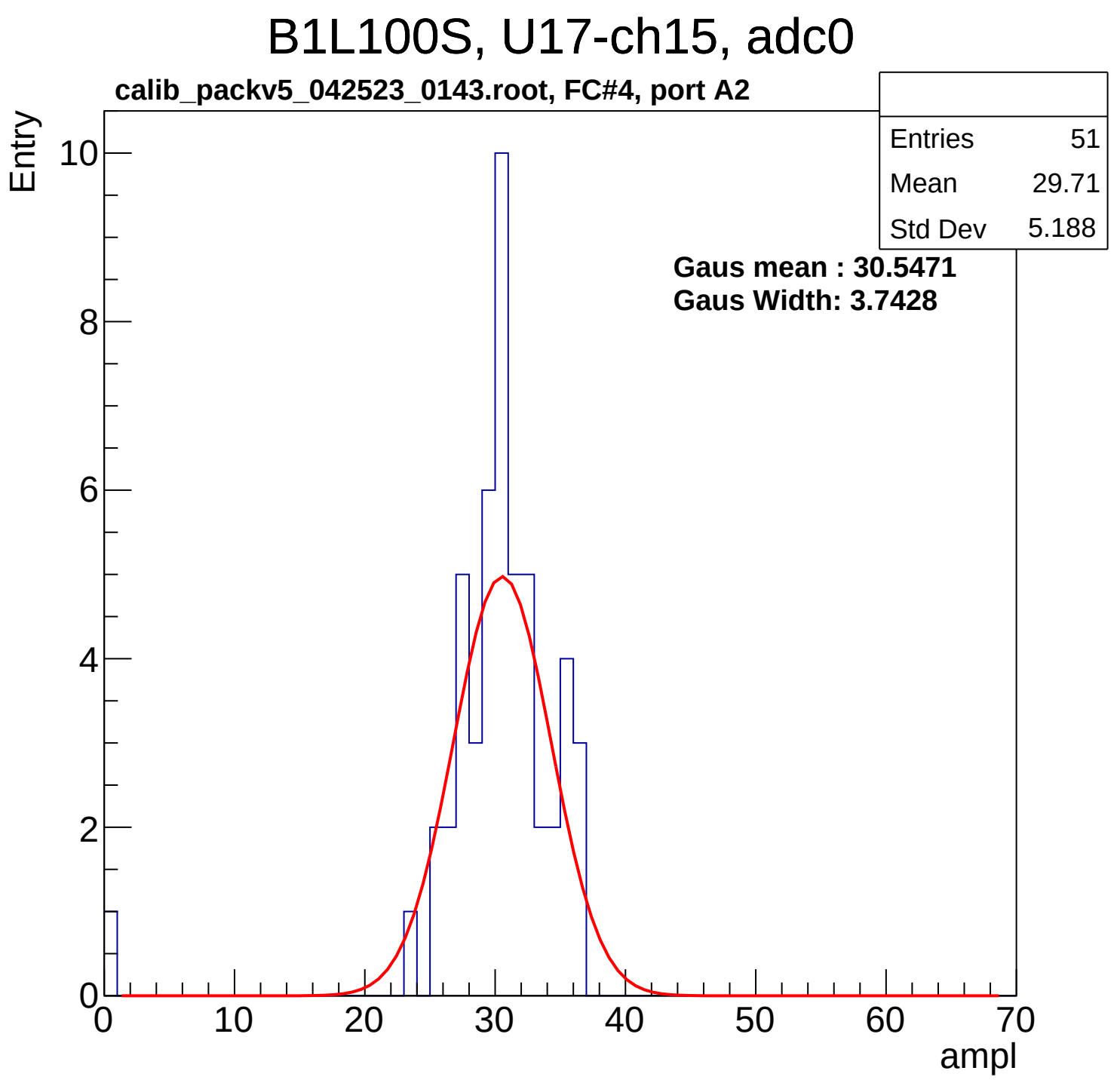
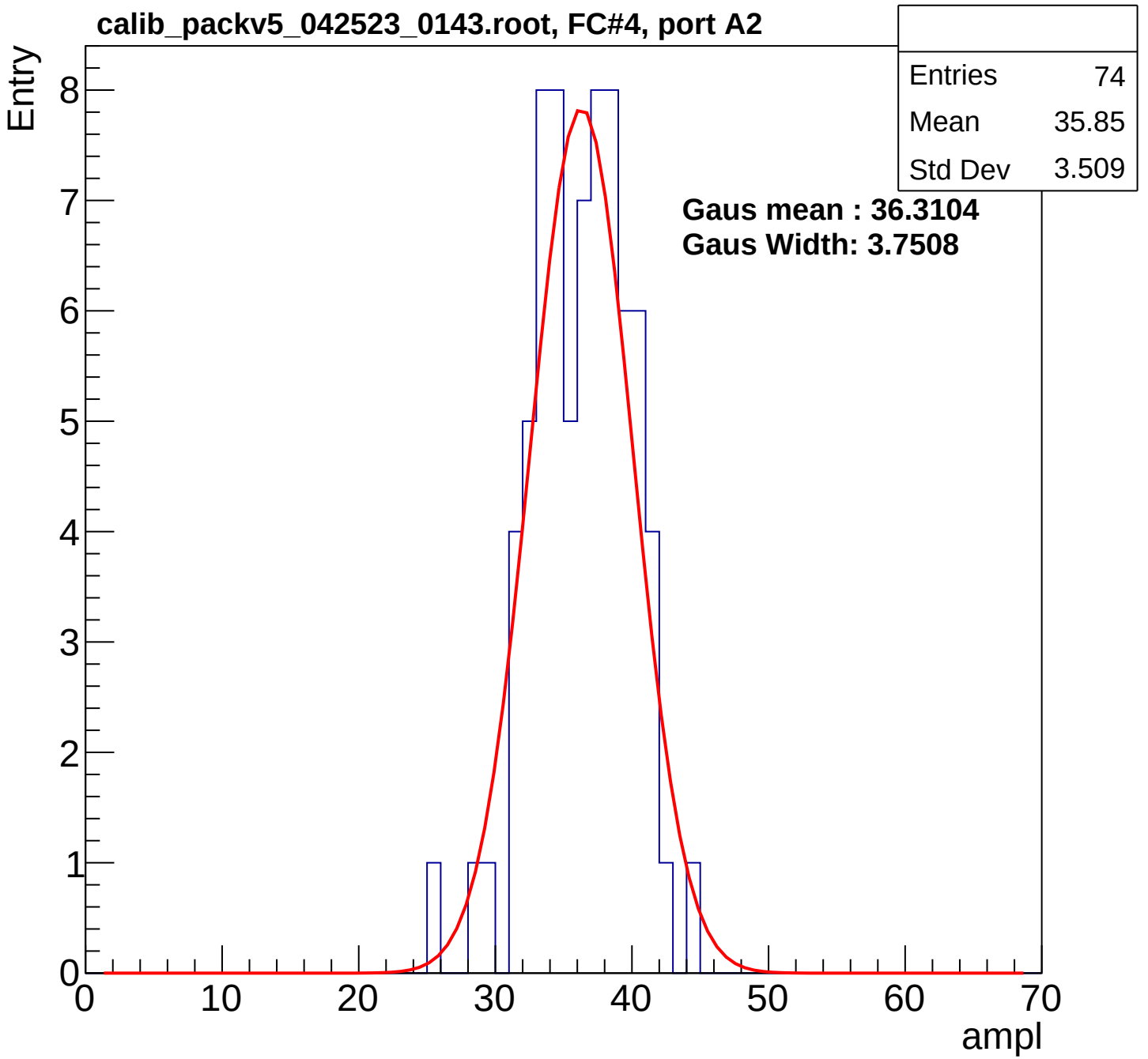
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch14, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 17
Mean 57.76
Std Dev 14.5
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L100S, U17-ch14, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch15, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 29.71
Std Dev 5.188
Gaus mean : 30.5471
Gaus Width: 3.7428
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U17-ch15, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 74
Mean 35.85
Std Dev 3.509
Gaus mean : 36.3104
Gaus Width: 3.7508
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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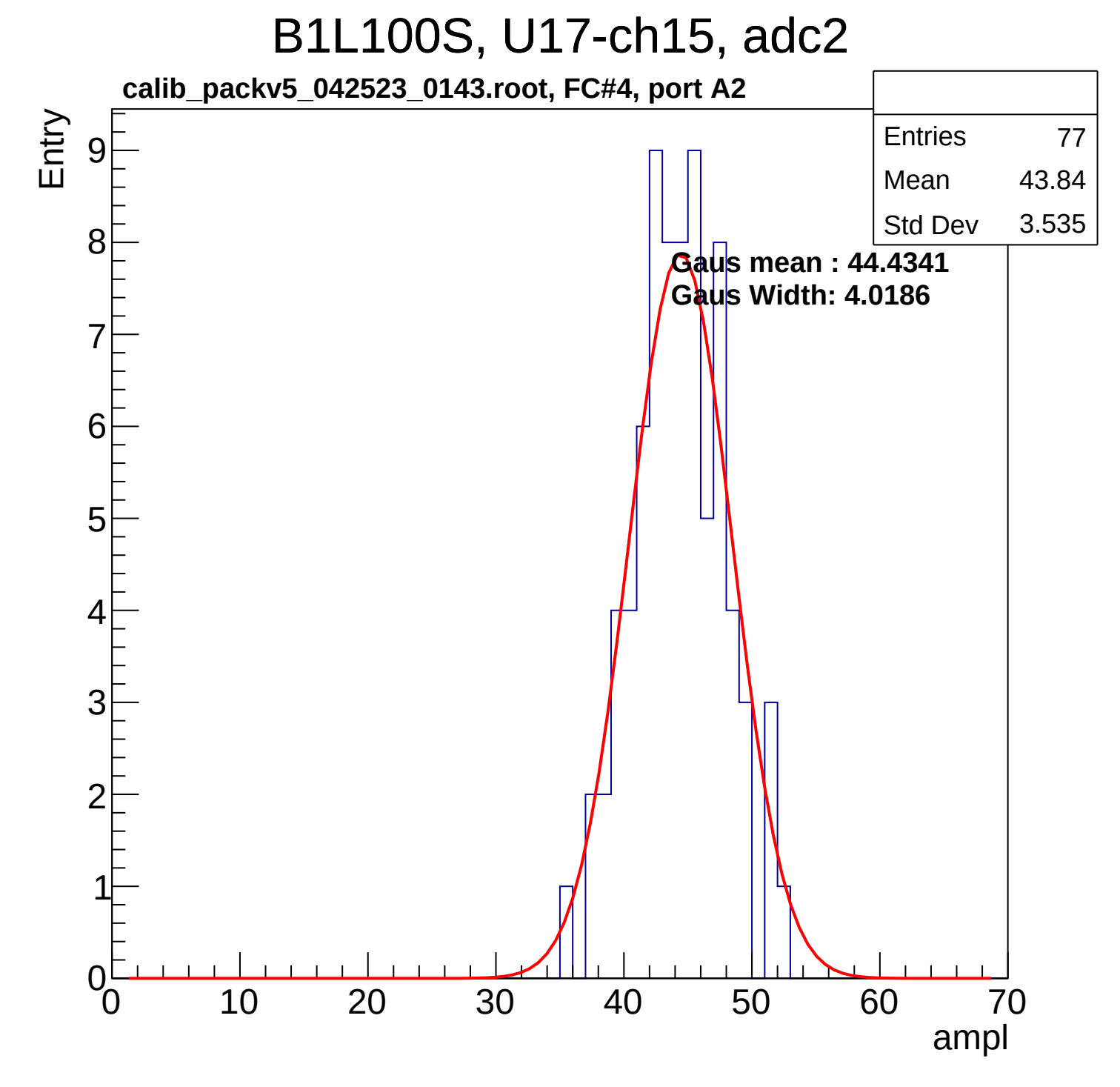
B1L100S, U17-ch15, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 77
Mean 43.84
Std Dev 3.535
Gaus mean : 44.4341
Gaus Width: 4.0186
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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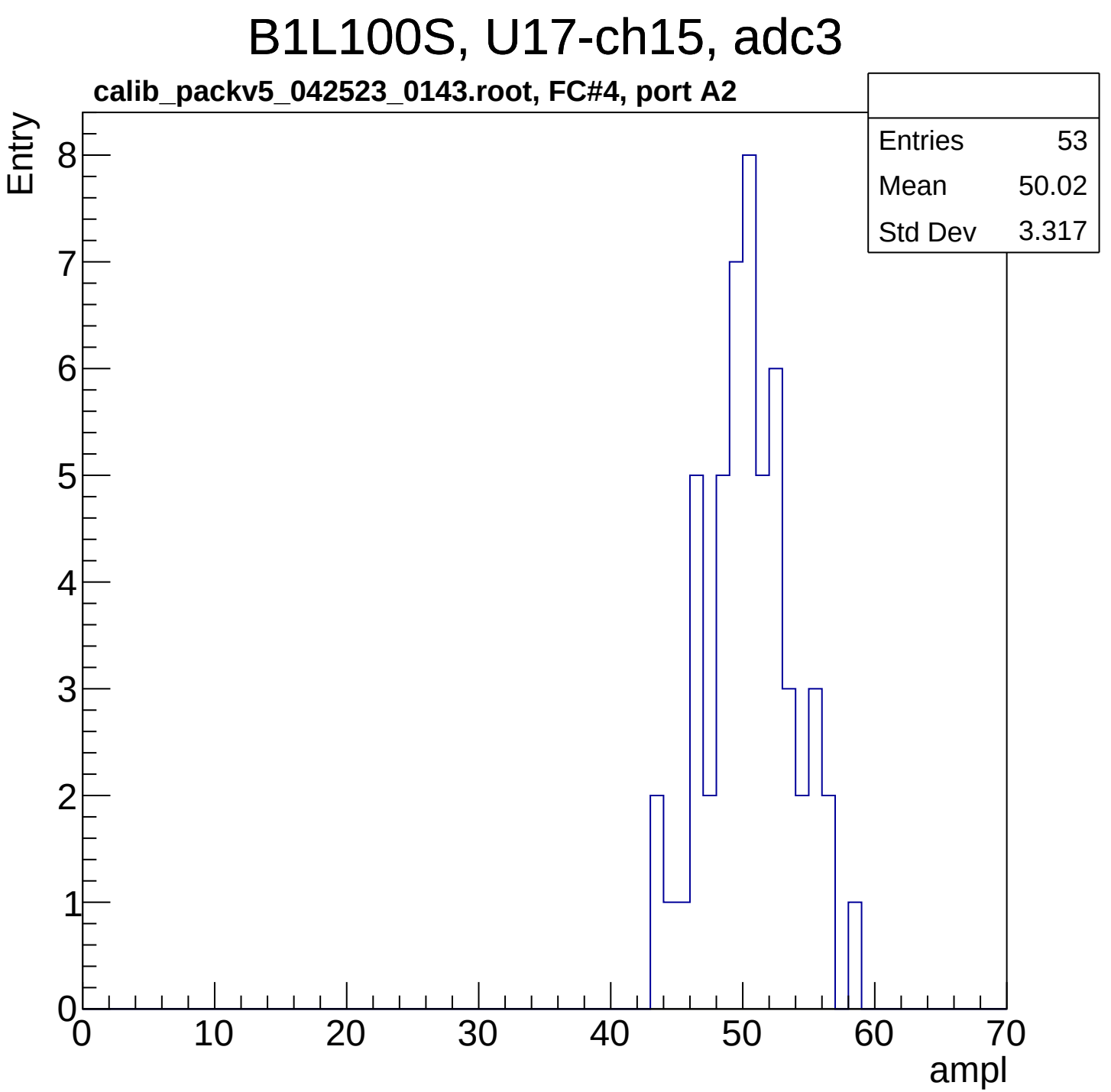
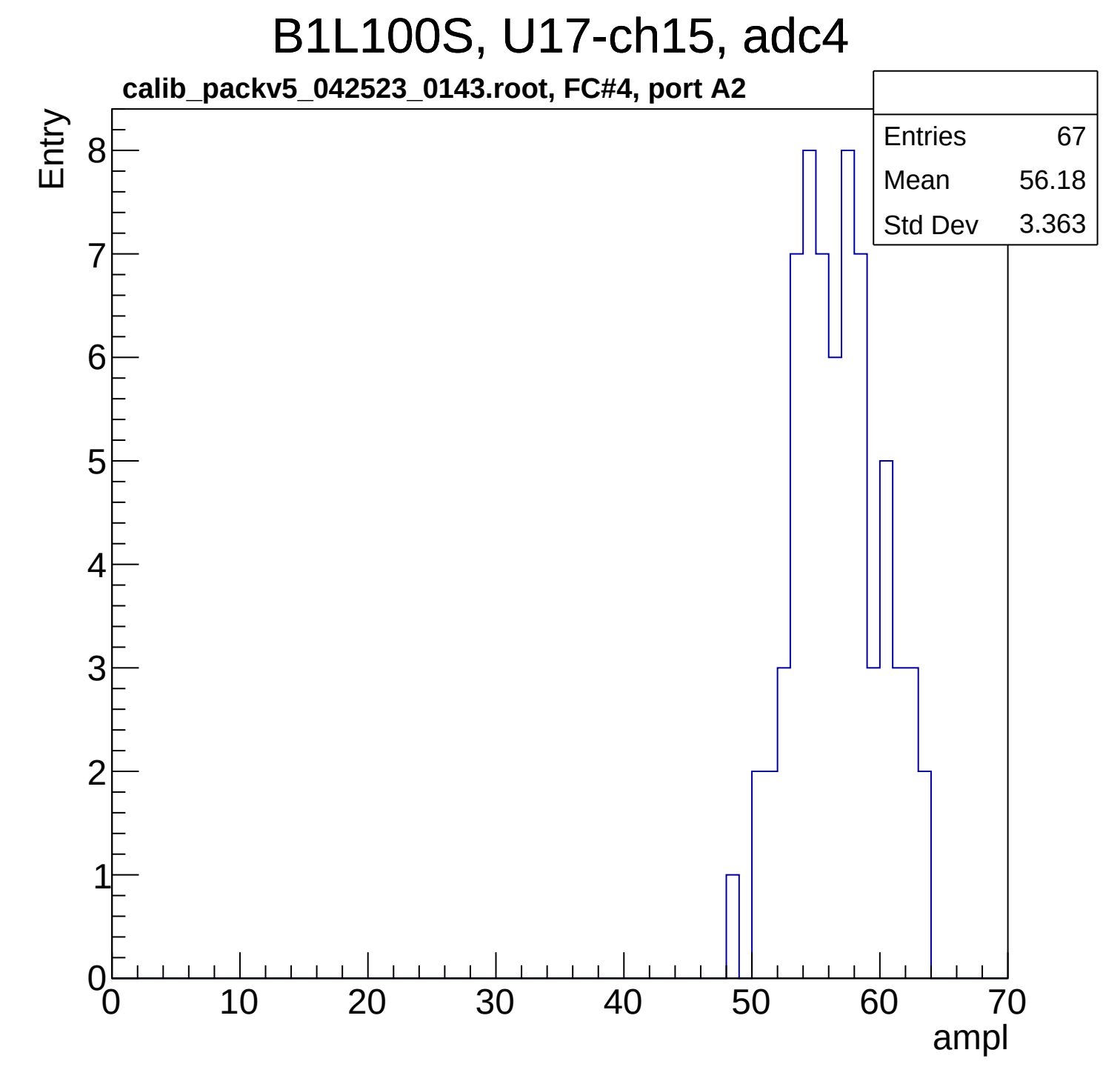

B1L100S, U17-ch15, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 50.02
Std Dev 3.317
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch15, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 56.18
Std Dev 3.363
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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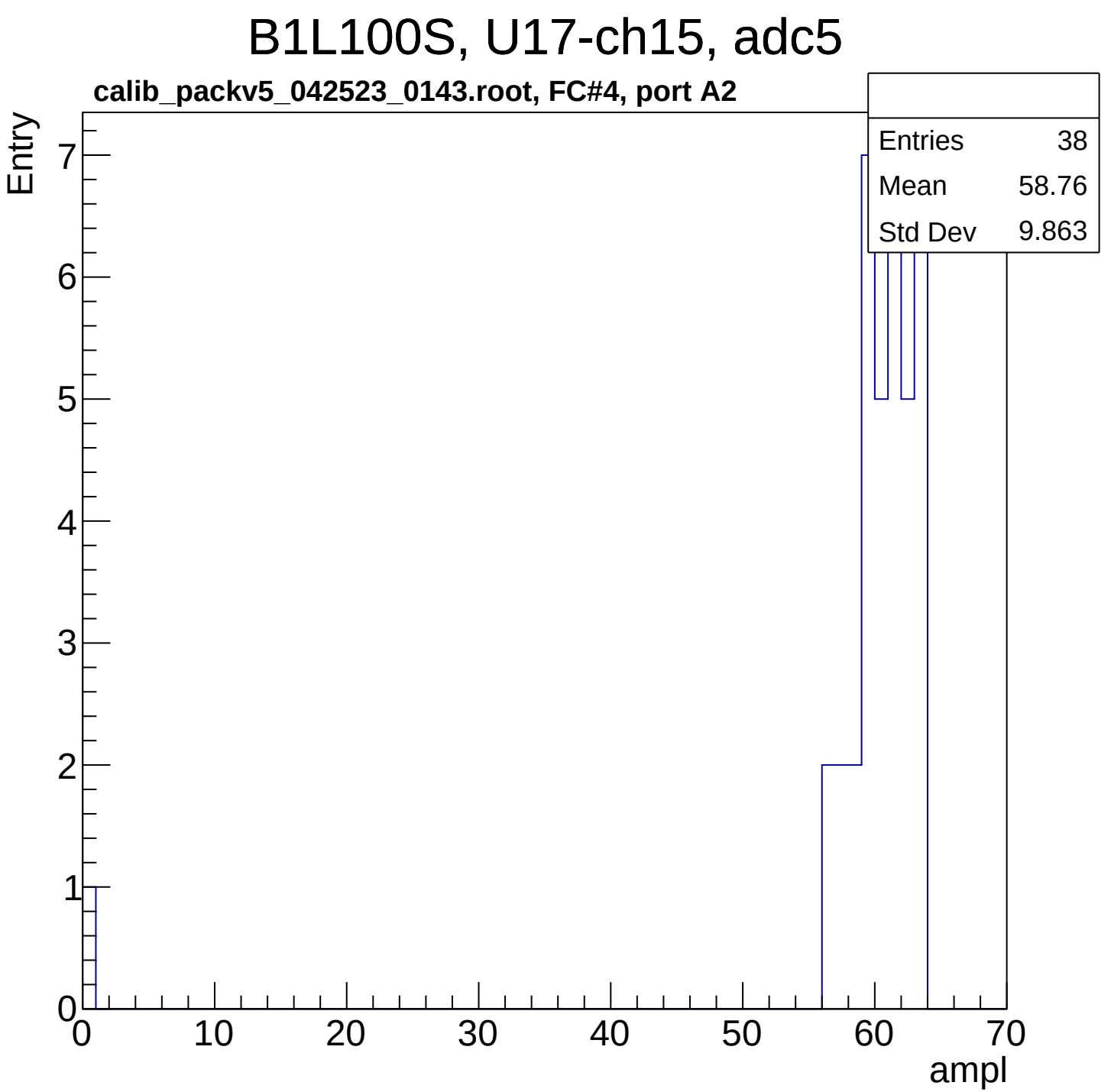
40
50
60
70


B1L100S, U17-ch15, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 38
Mean 58.76
Std Dev 9.863
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
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60
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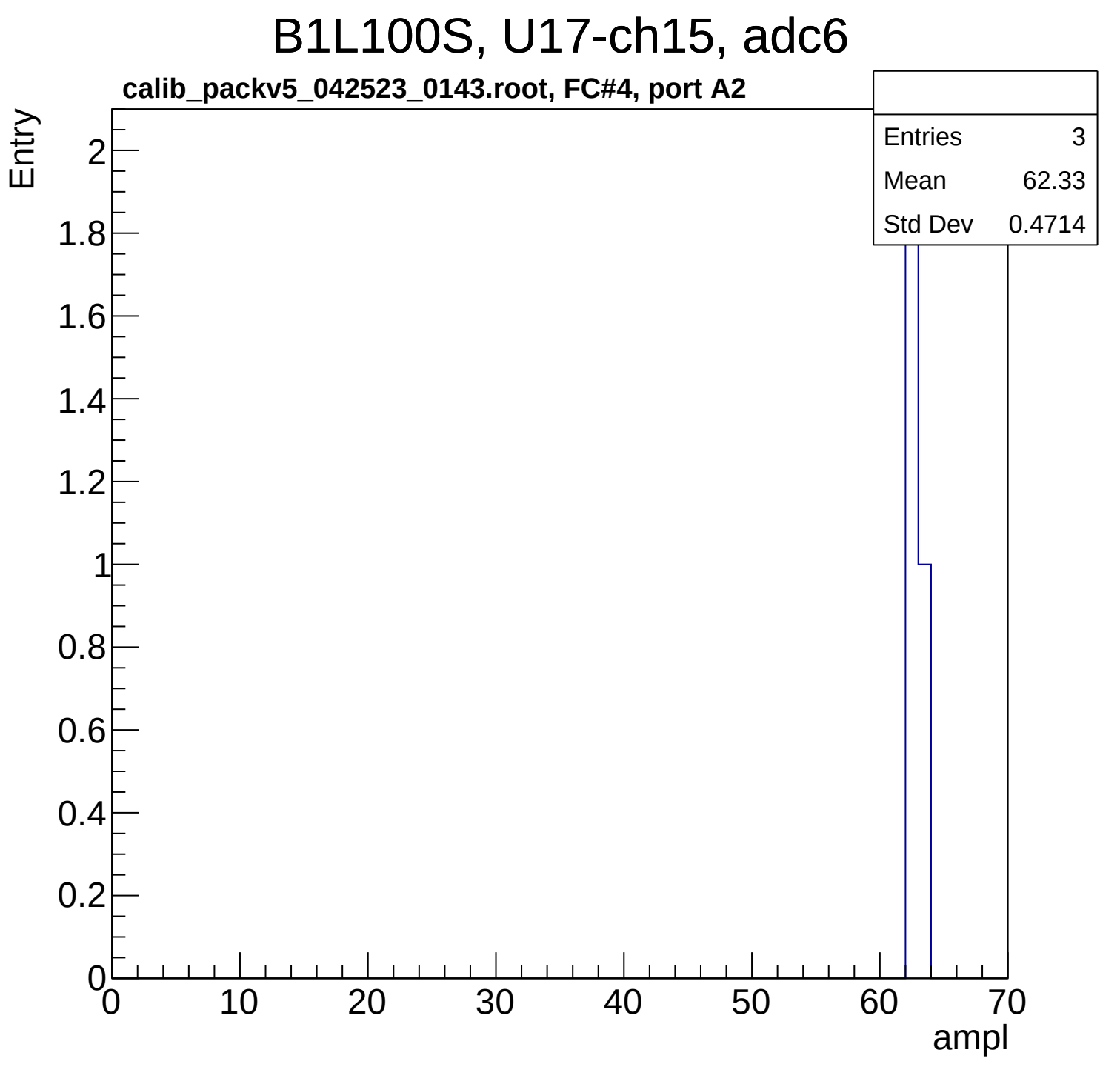
B1L100S, U17-ch15, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 62.33
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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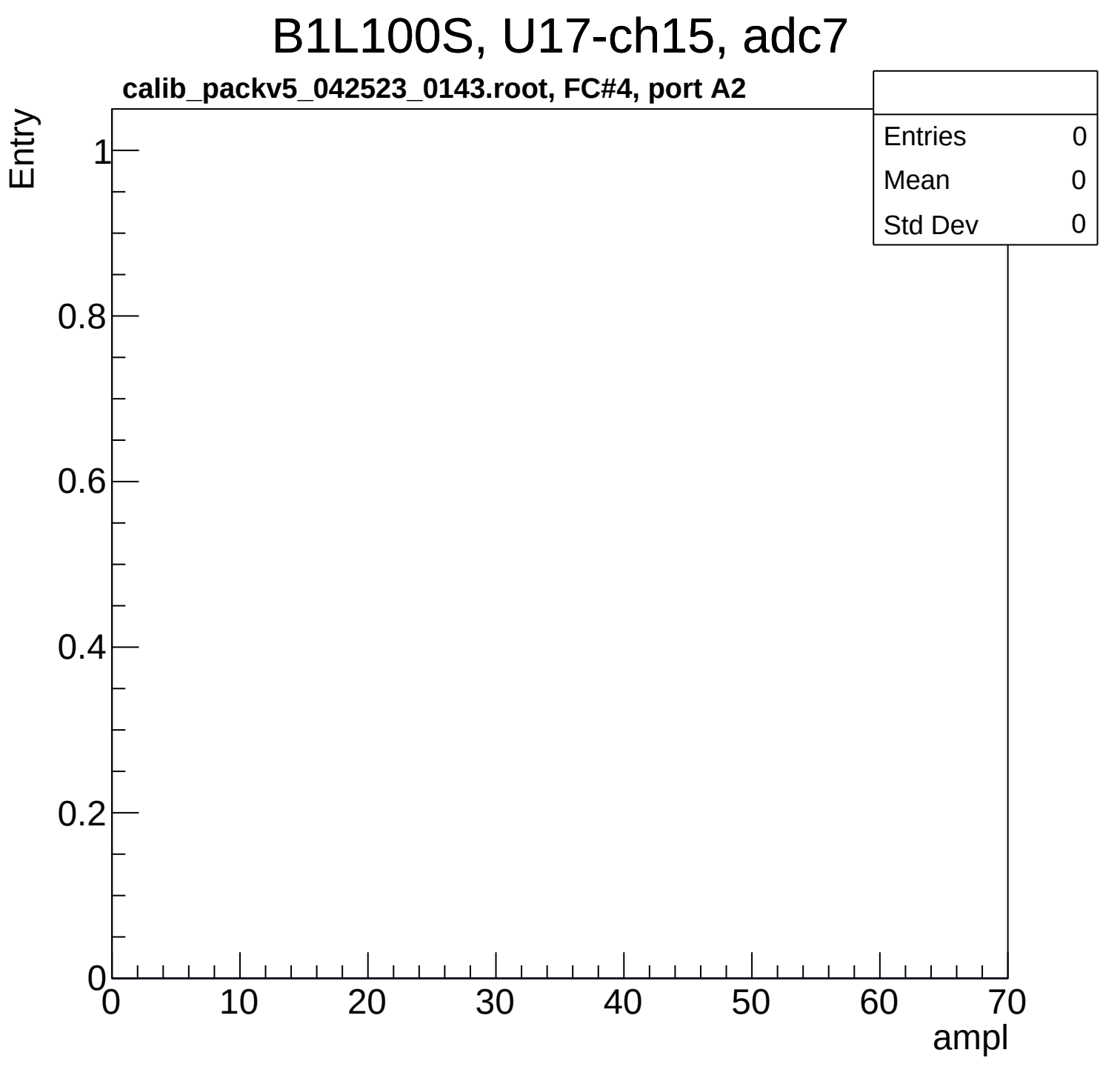
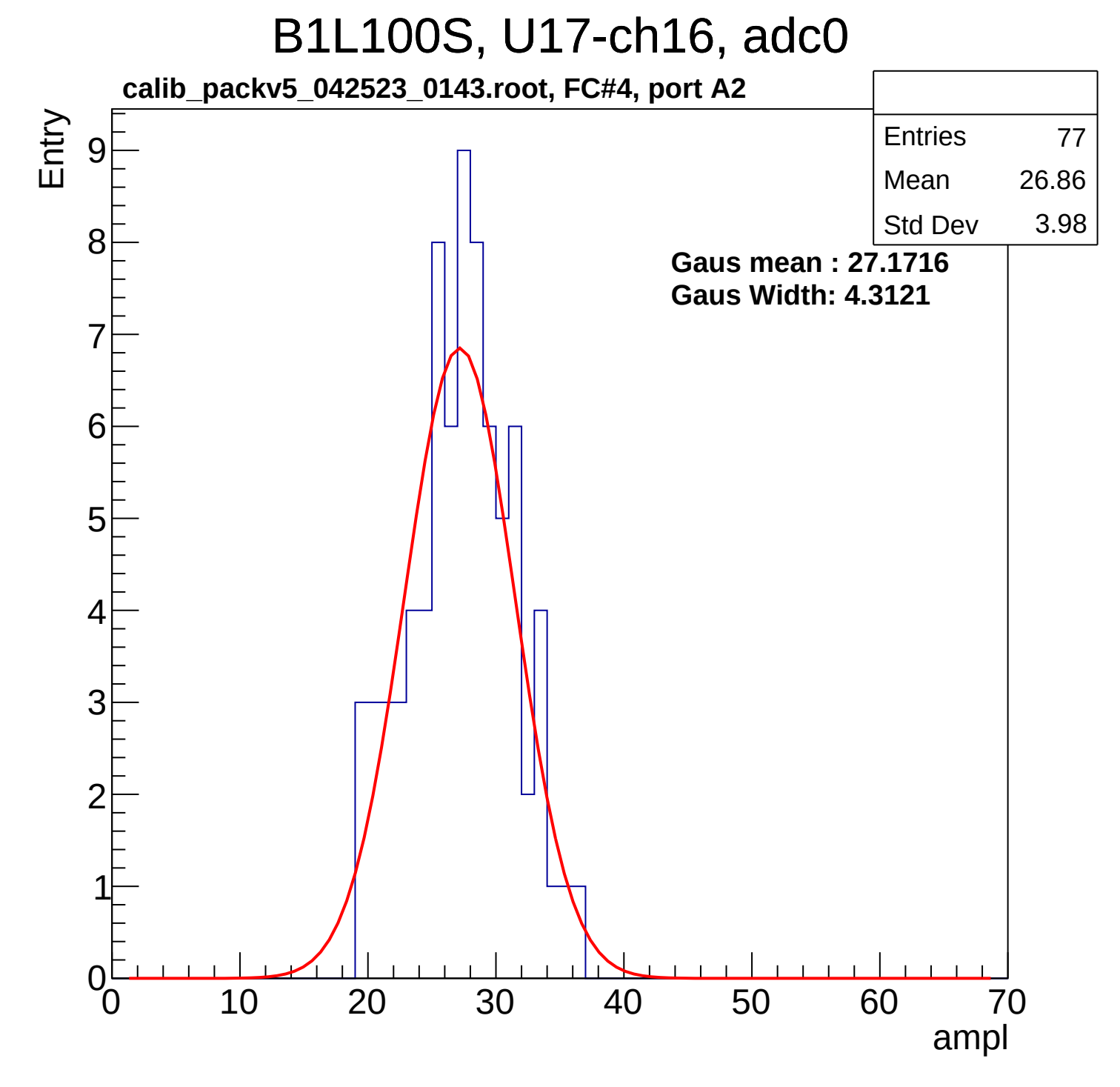
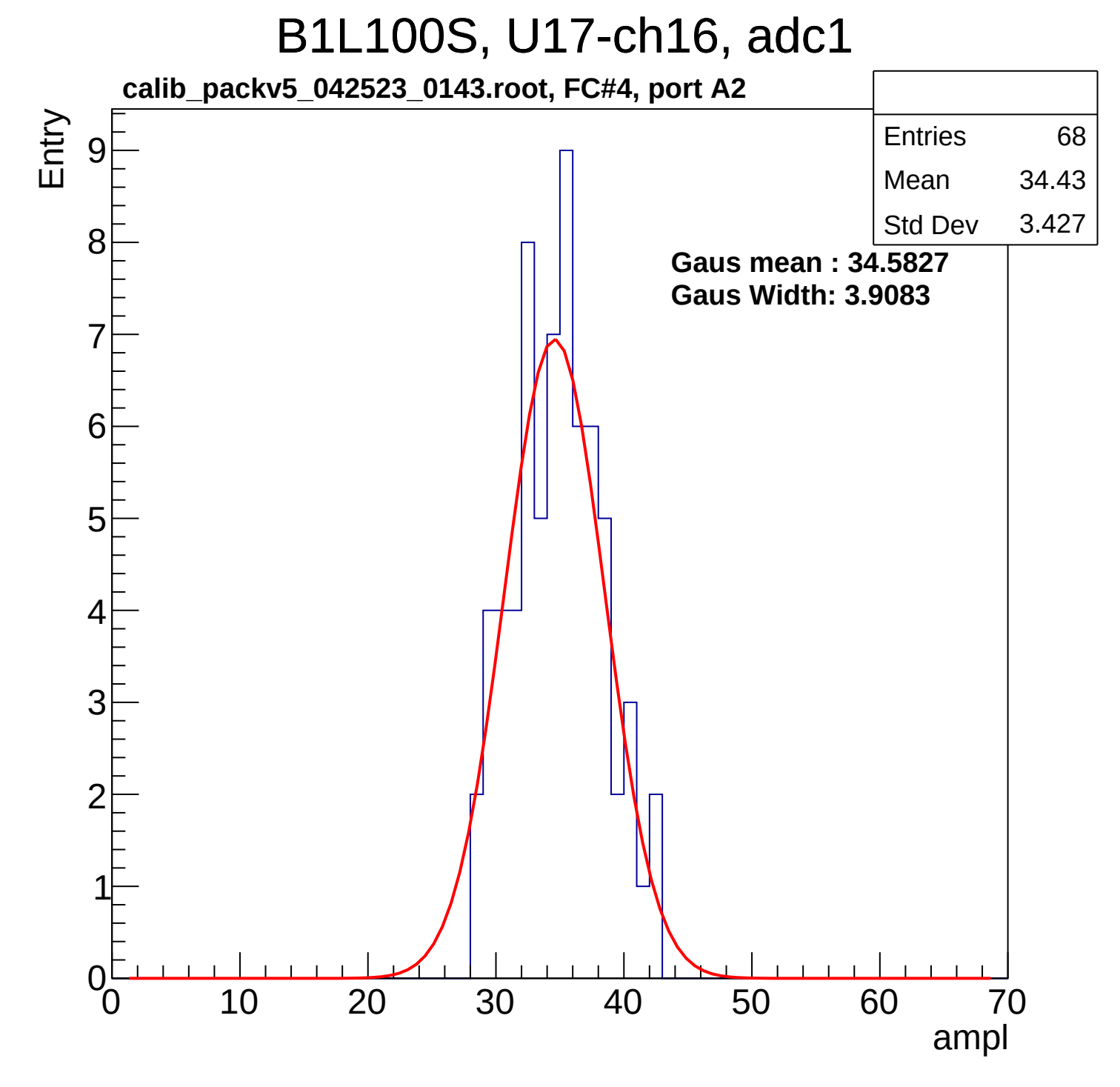
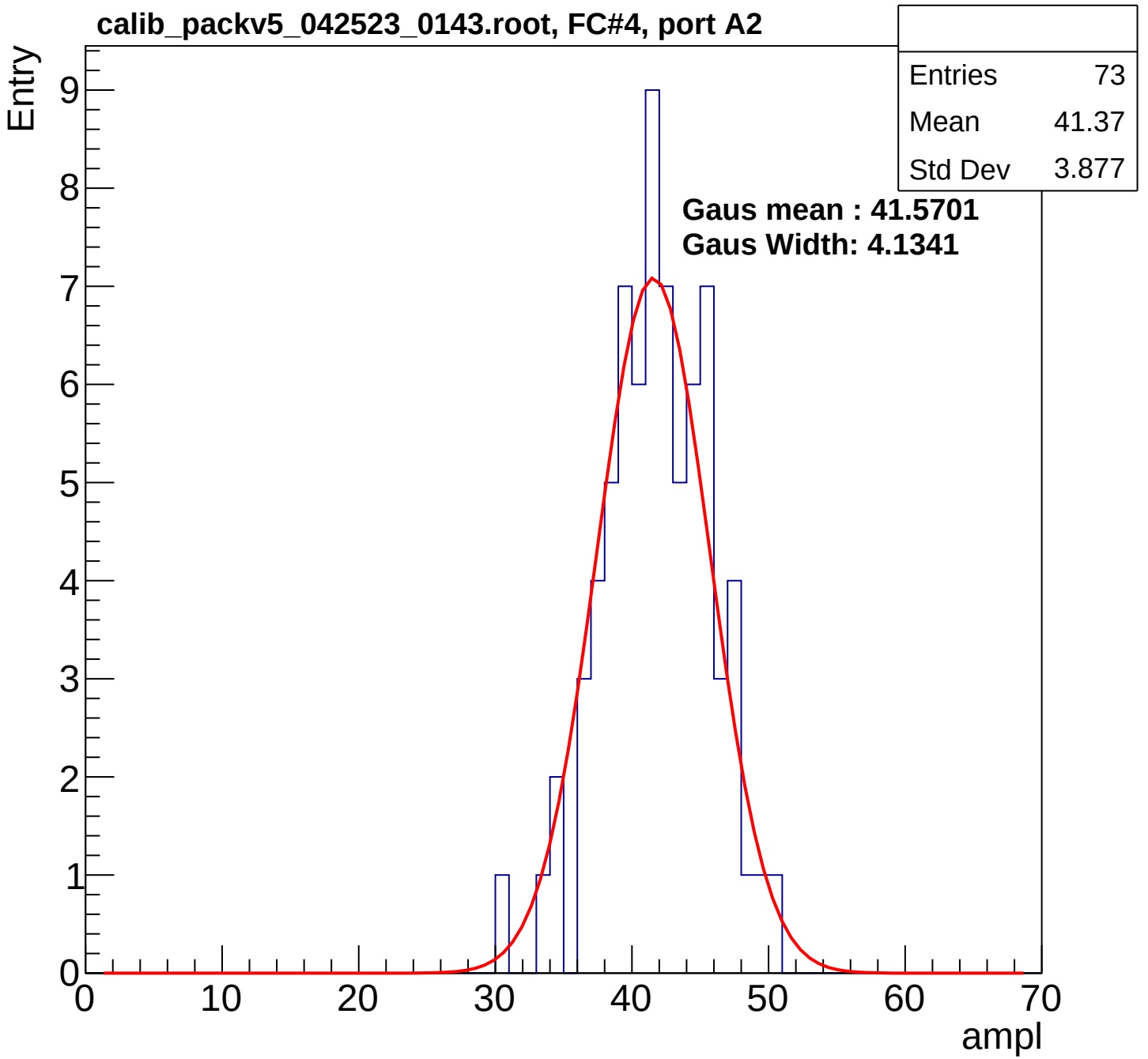
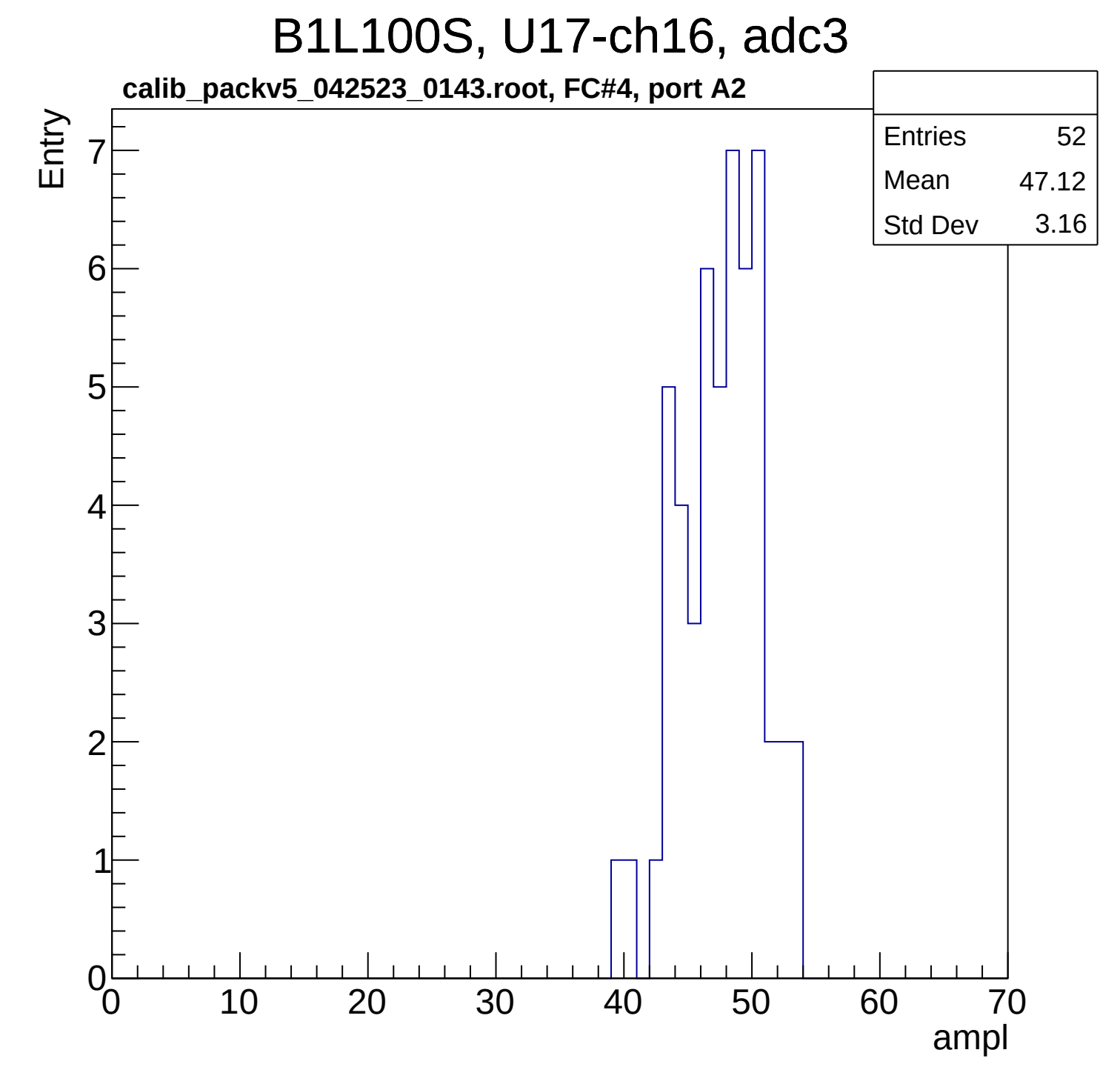
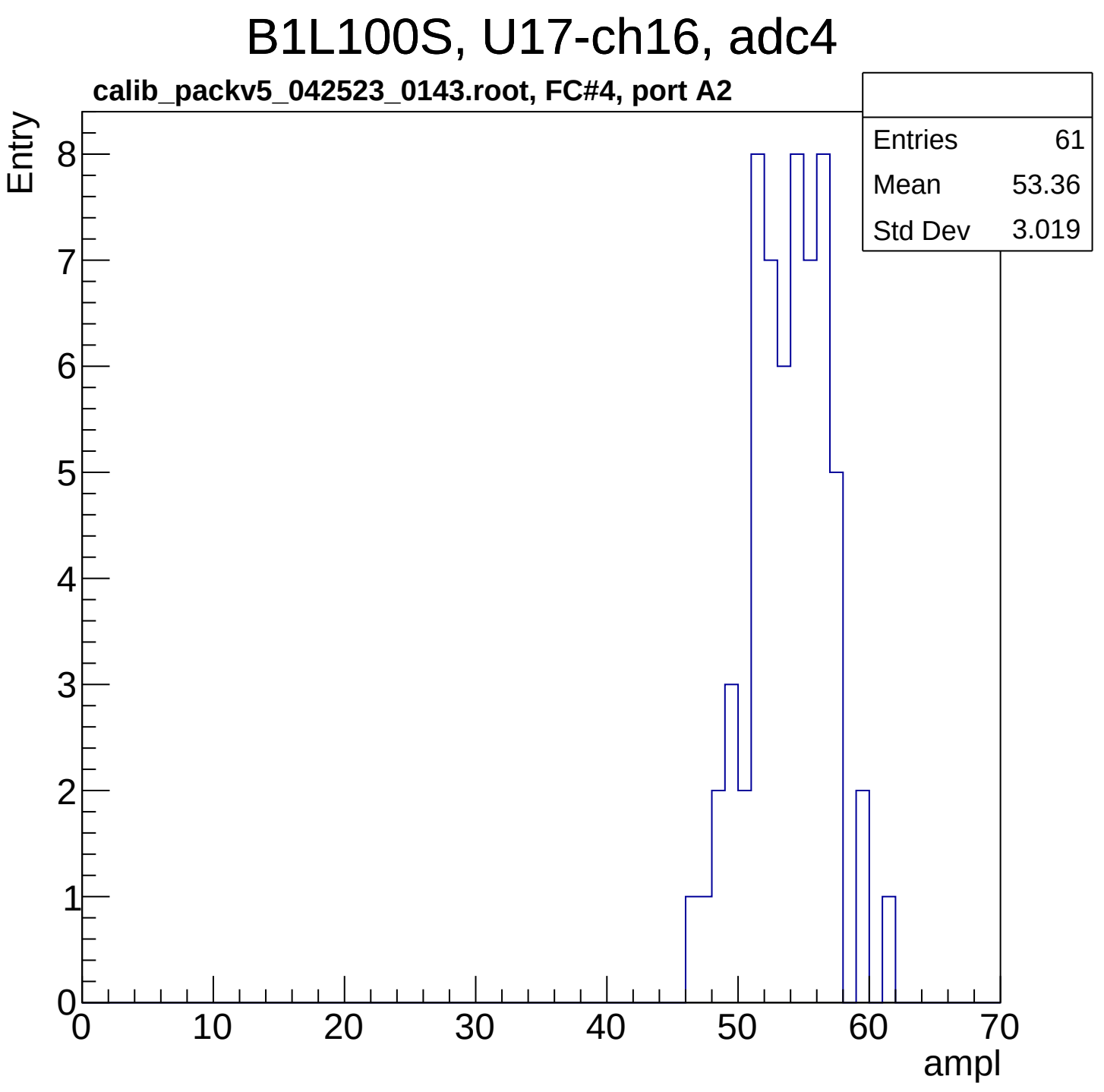

B1L100S, U17-ch15, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

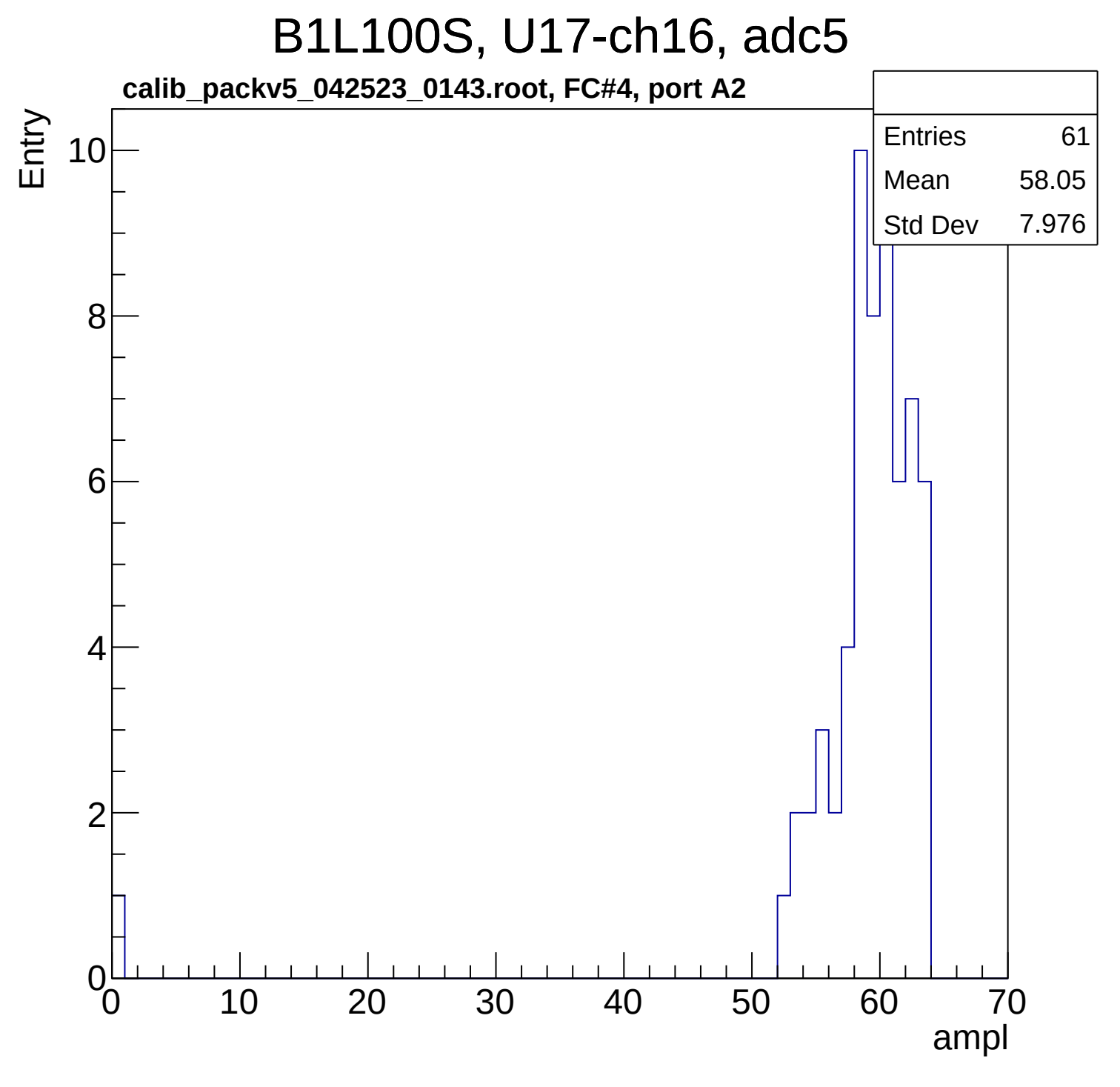

B1L100S, U17-ch16, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 77
Mean 26.86
Std Dev 3.98
Gaus mean : 27.1716
Gaus Width: 4.3121
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

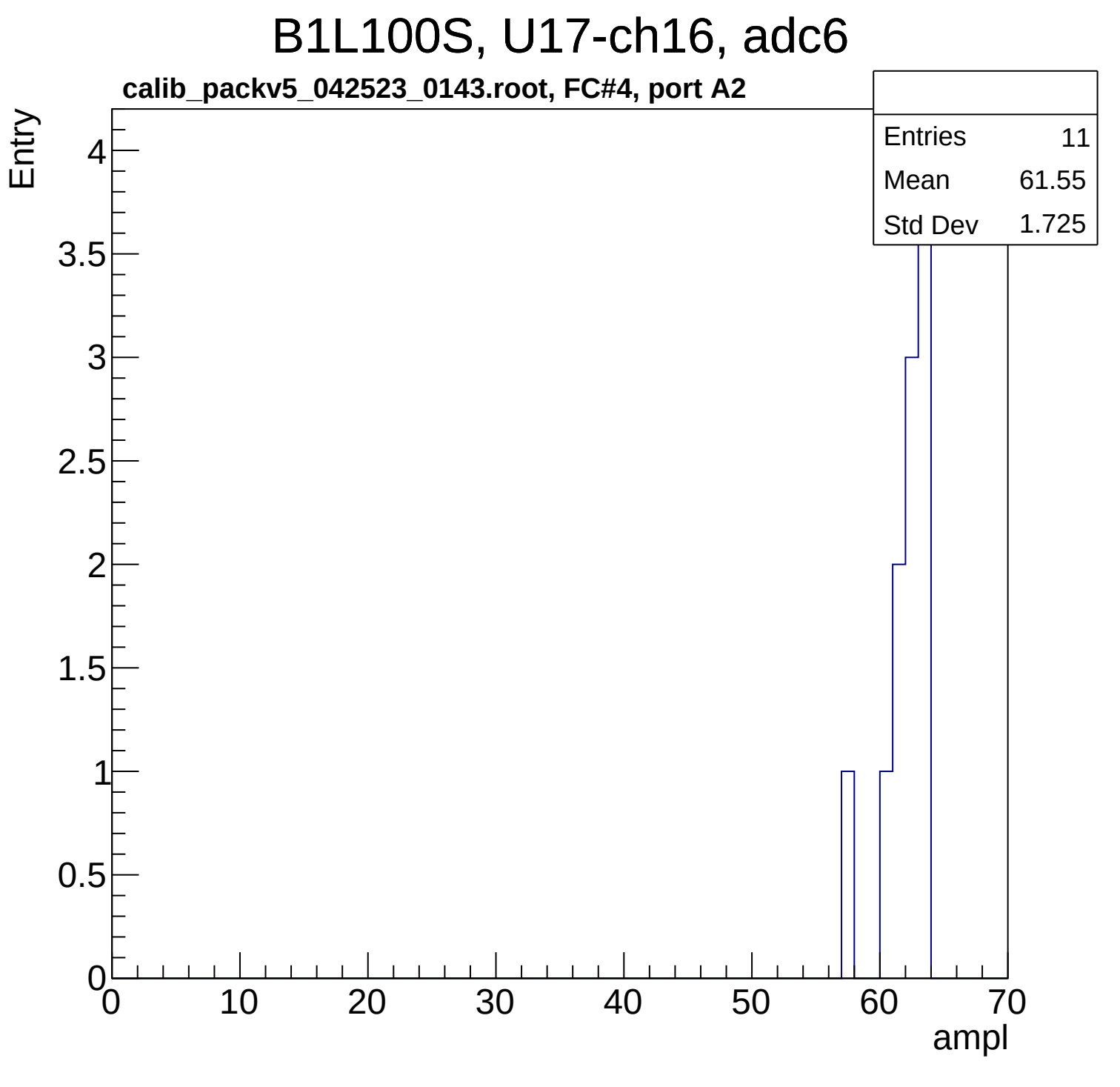

B1L100S, U17-ch16, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 34.43
Std Dev 3.427
Gaus mean : 34.5827
Gaus Width: 3.9083
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

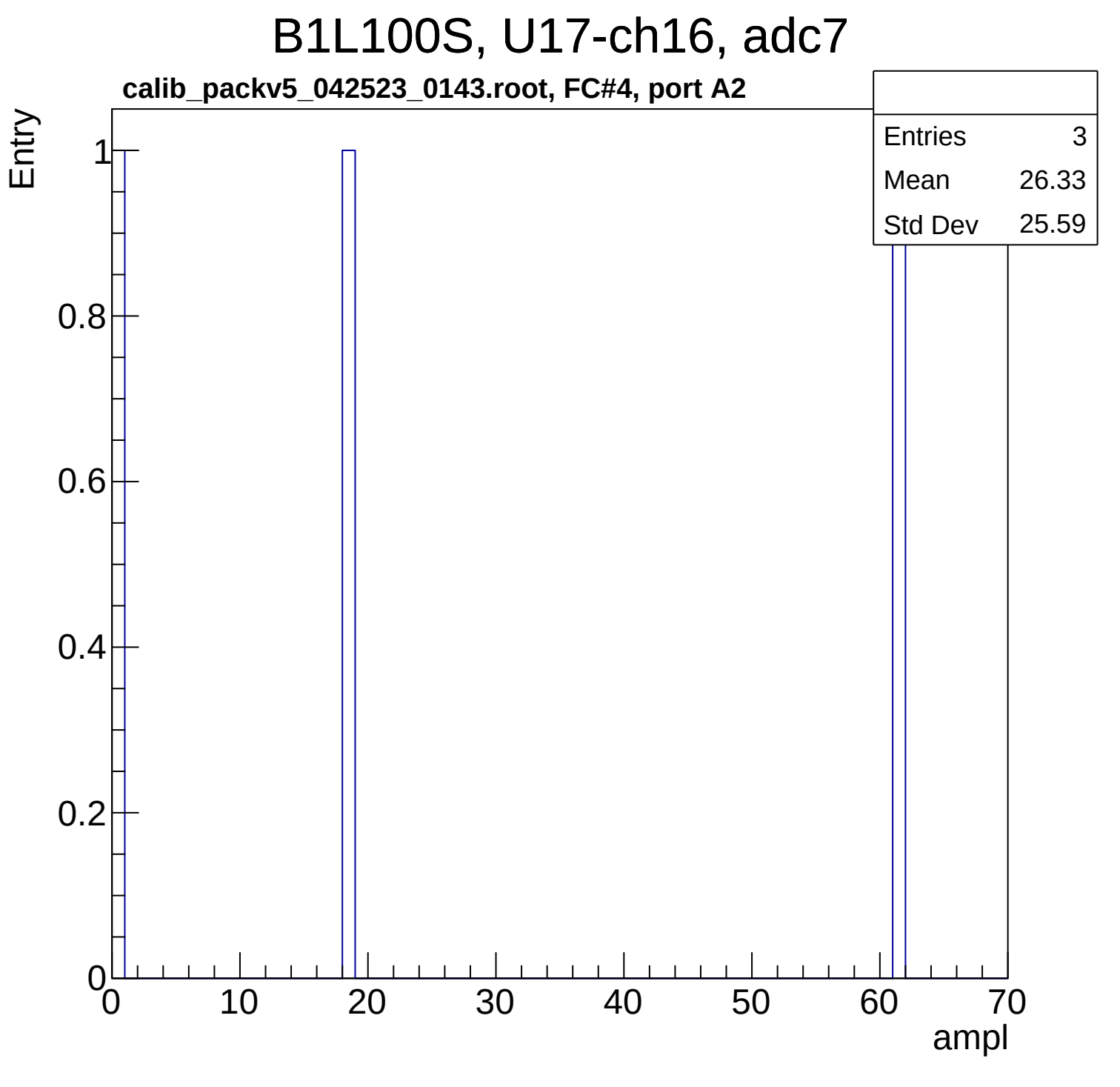

B1L100S, U17-ch16, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 41.37
Std Dev 3.877
Gaus mean : 41.5701
Gaus Width: 4.1341
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

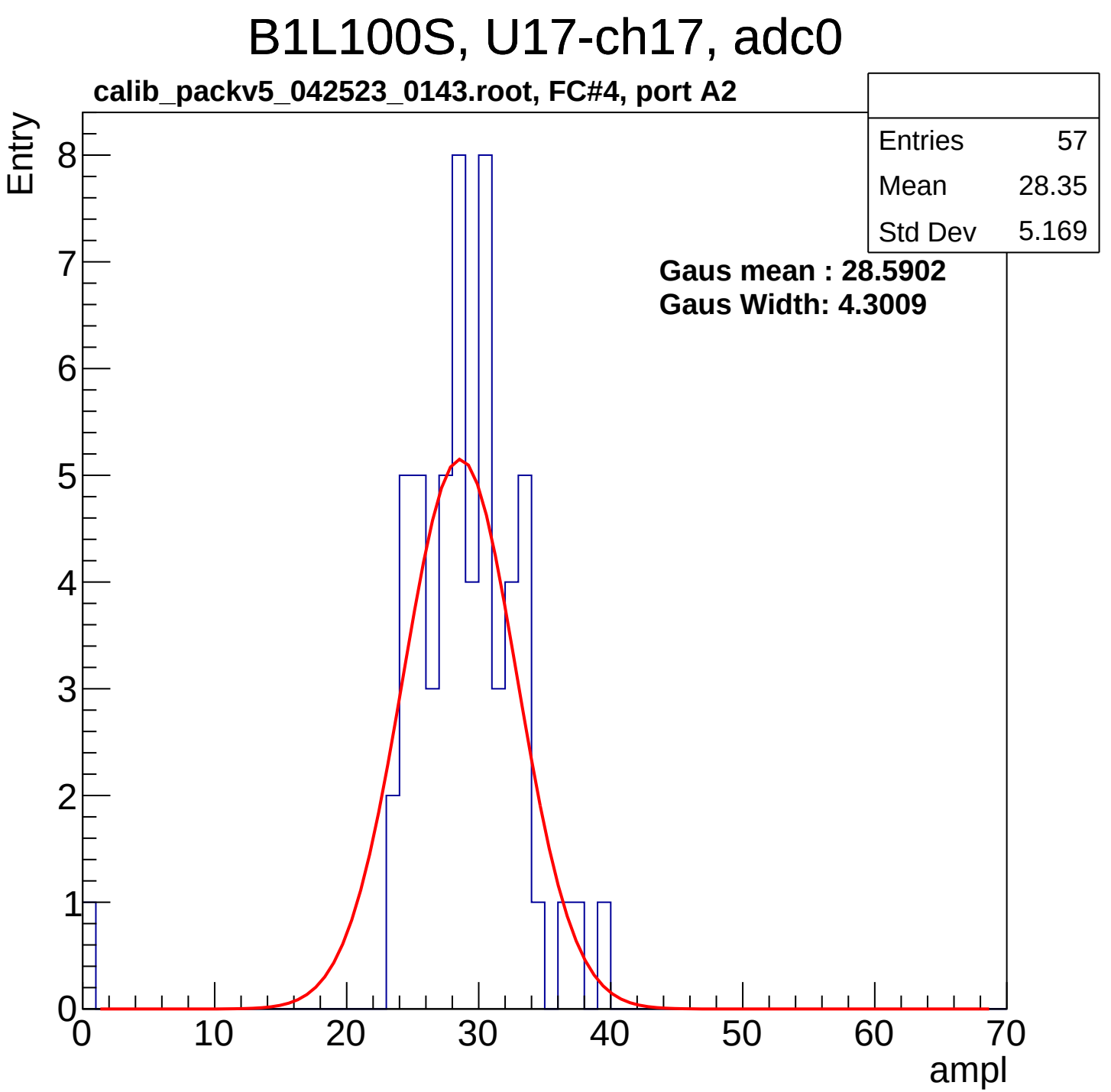

B1L100S, U17-ch16, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 52
Mean 47.12
Std Dev 3.16
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

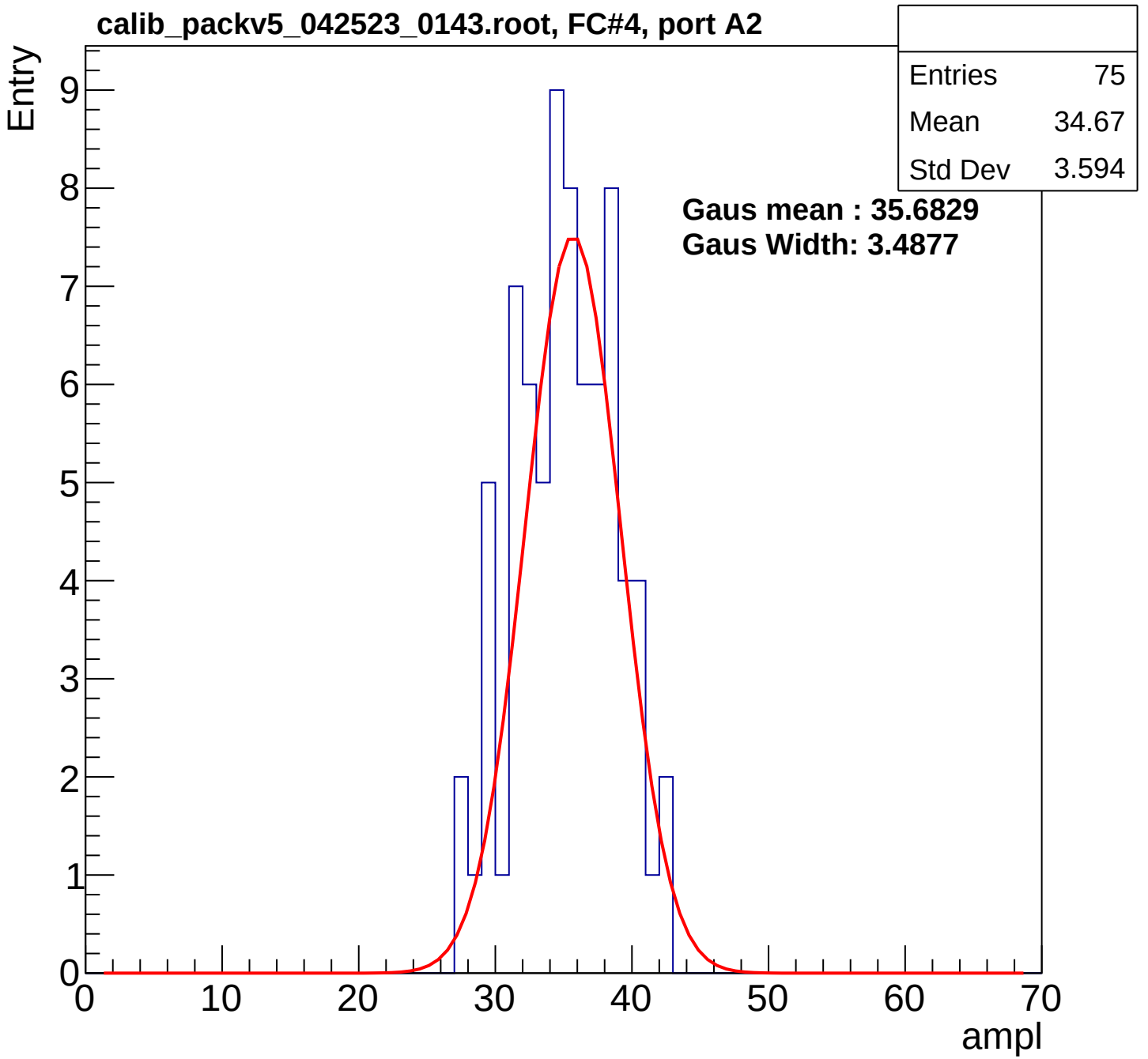

B1L100S, U17-ch16, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 53.36
Std Dev 3.019
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

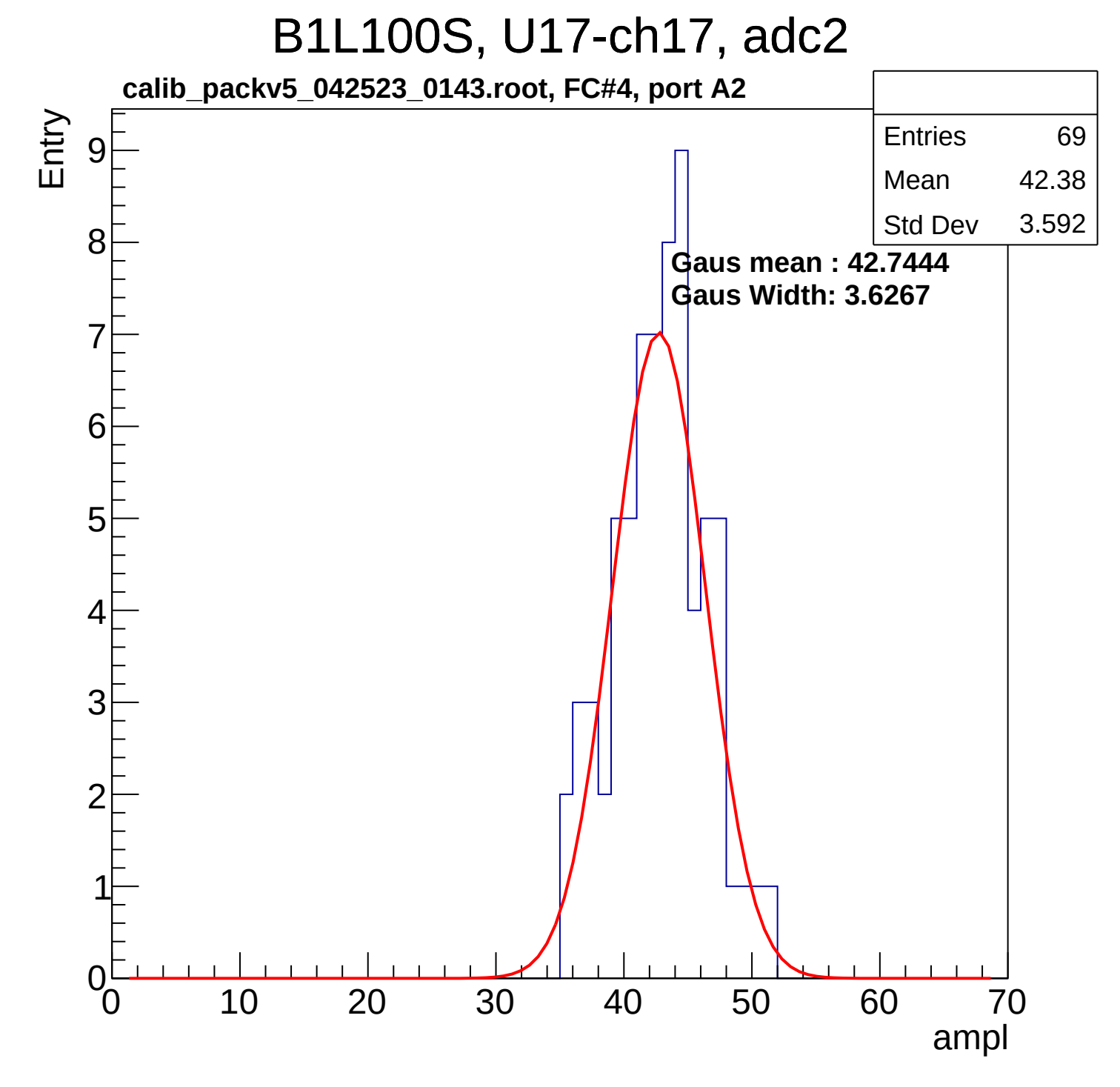

B1L100S, U17-ch16, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 58.05
Std Dev 7.976
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

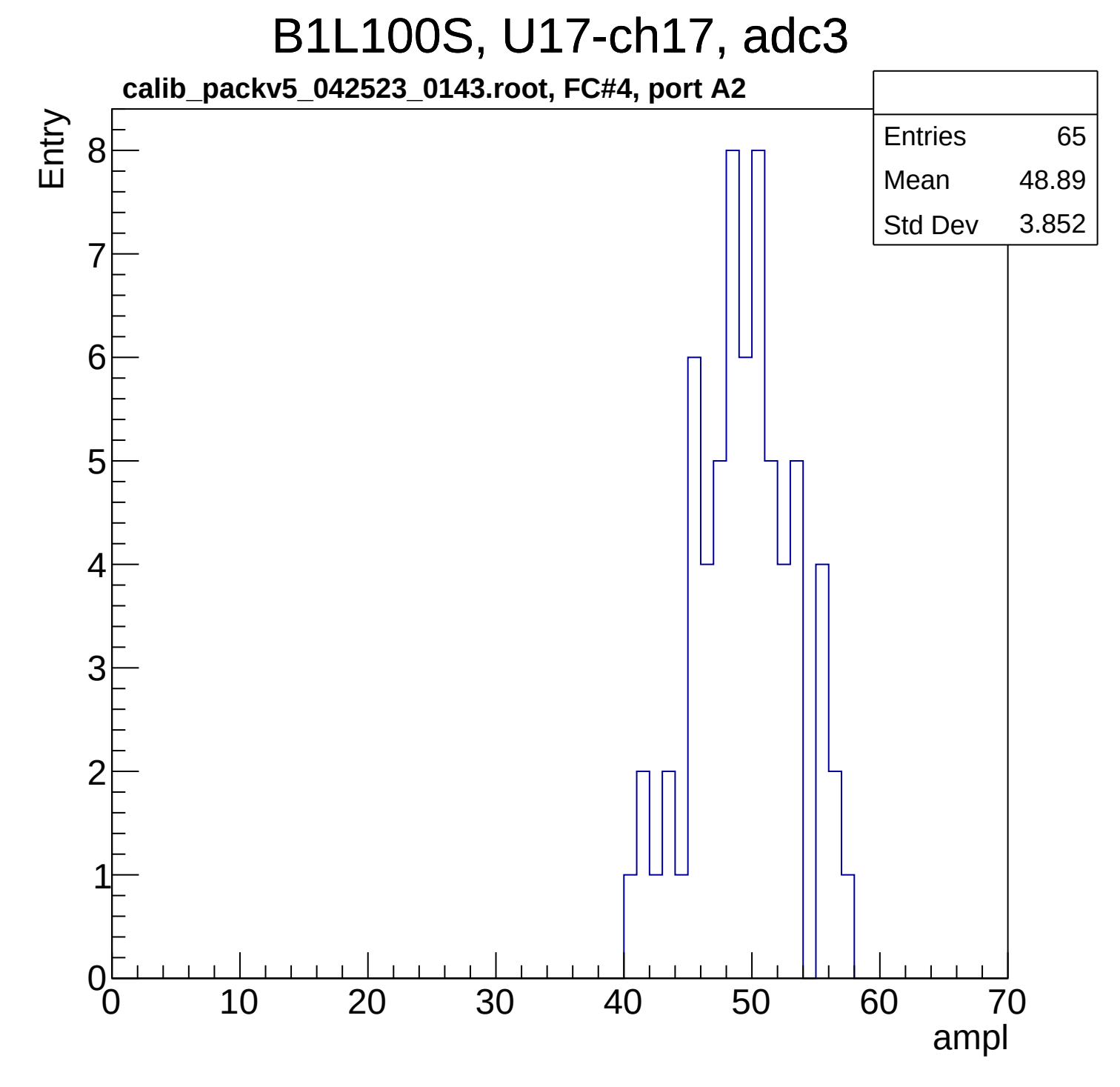

B1L100S, U17-ch16, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 11
Mean 61.55
Std Dev 1.725
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

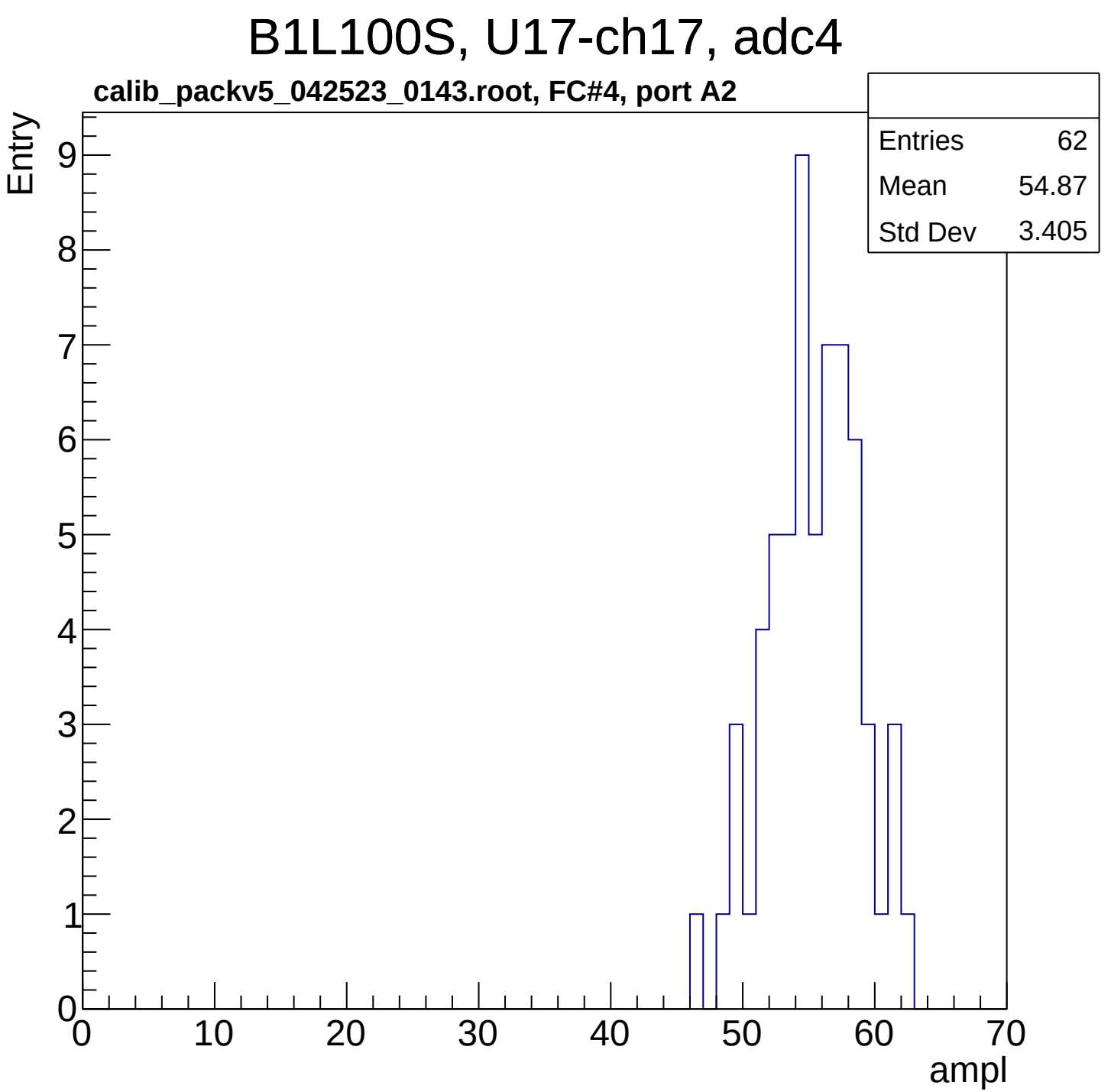

B1L100S, U17-ch16, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 26.33
Std Dev 25.59
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

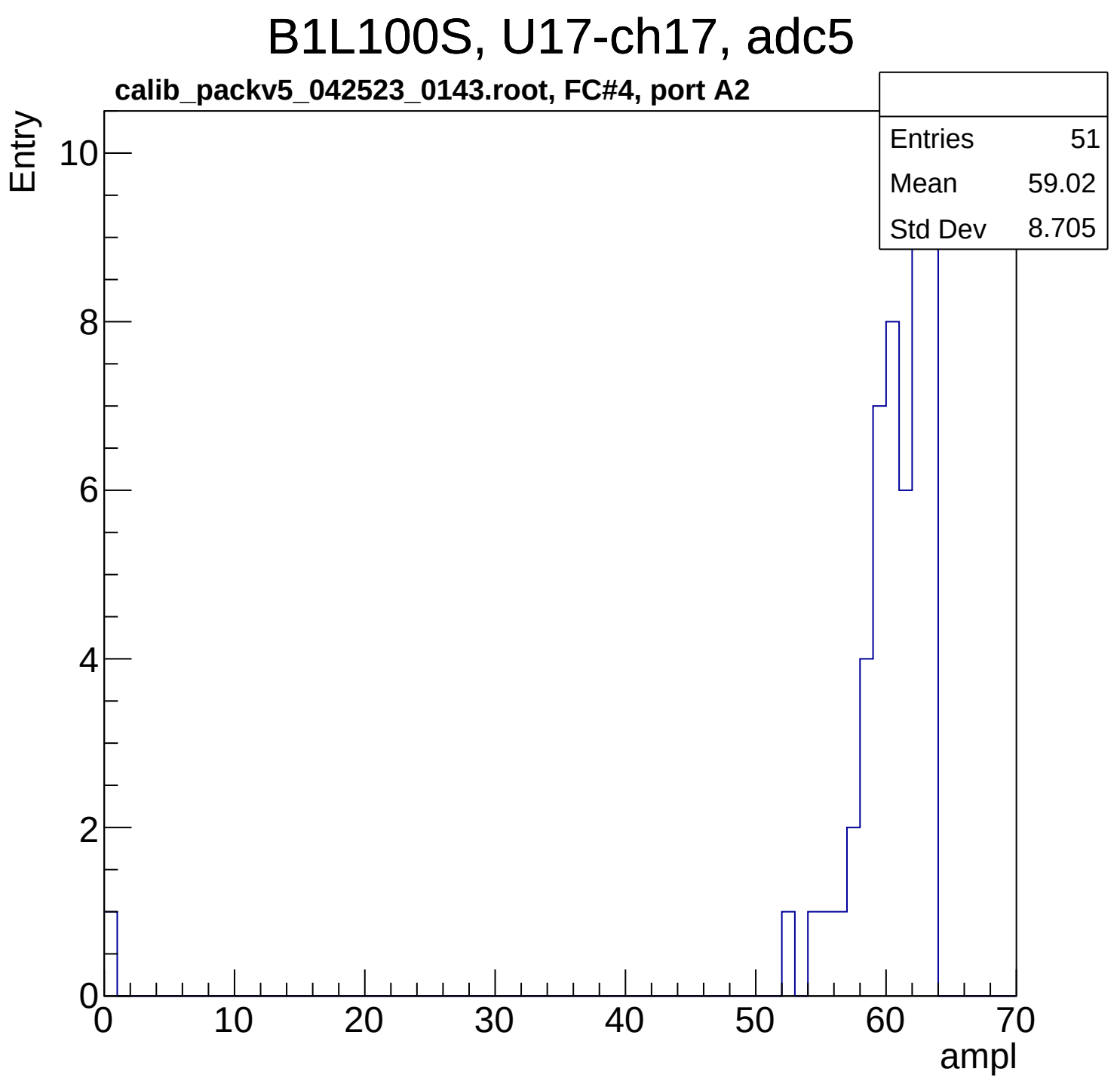

B1L100S, U17-ch17, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 28.35
Std Dev 5.169
Gaus mean : 28.5902
Gaus Width: 4.3009
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

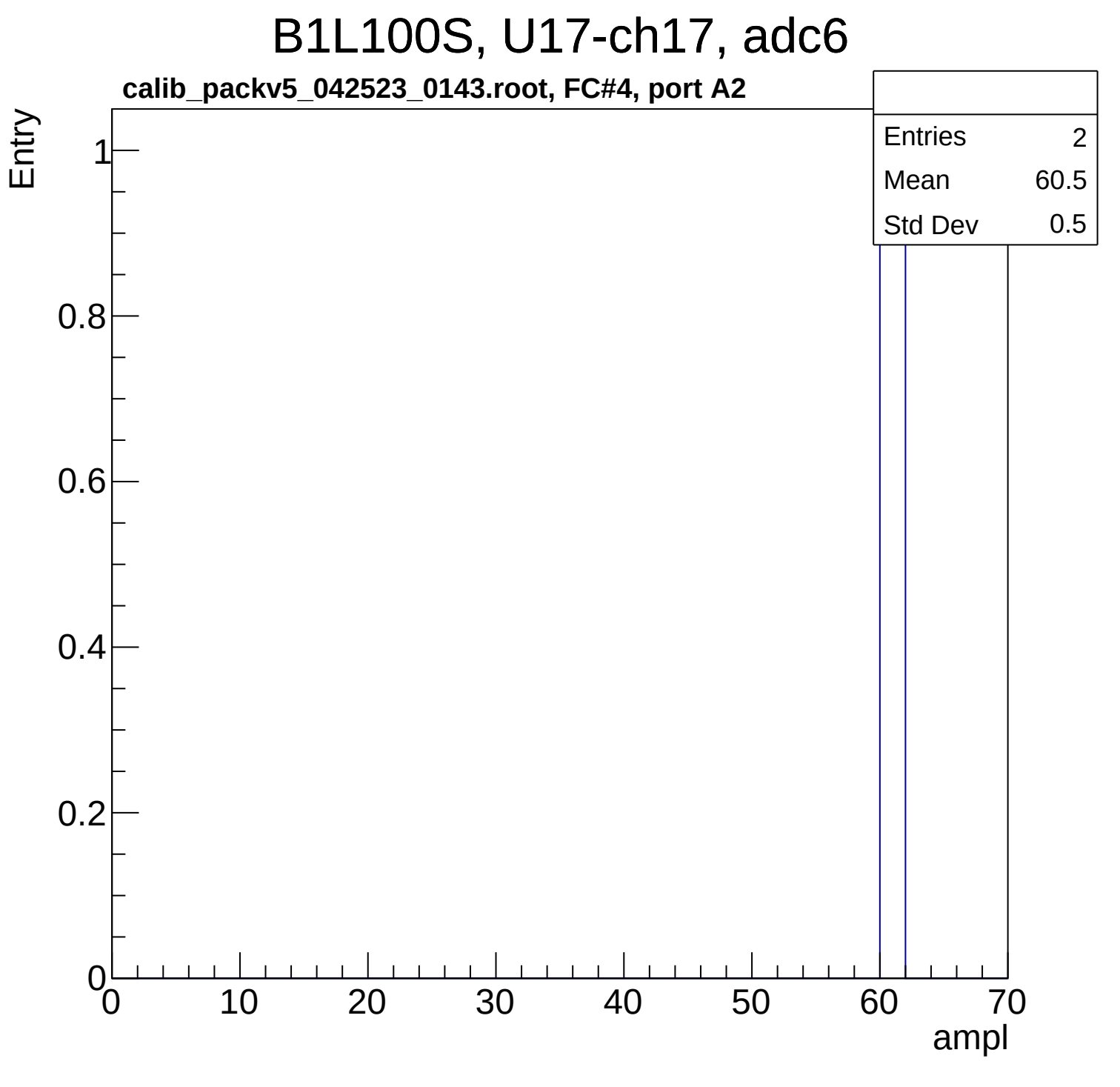

B1L100S, U17-ch17, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 75
Mean 34.67
Std Dev 3.594
Gaus mean : 35.6829
Gaus Width: 3.4877
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

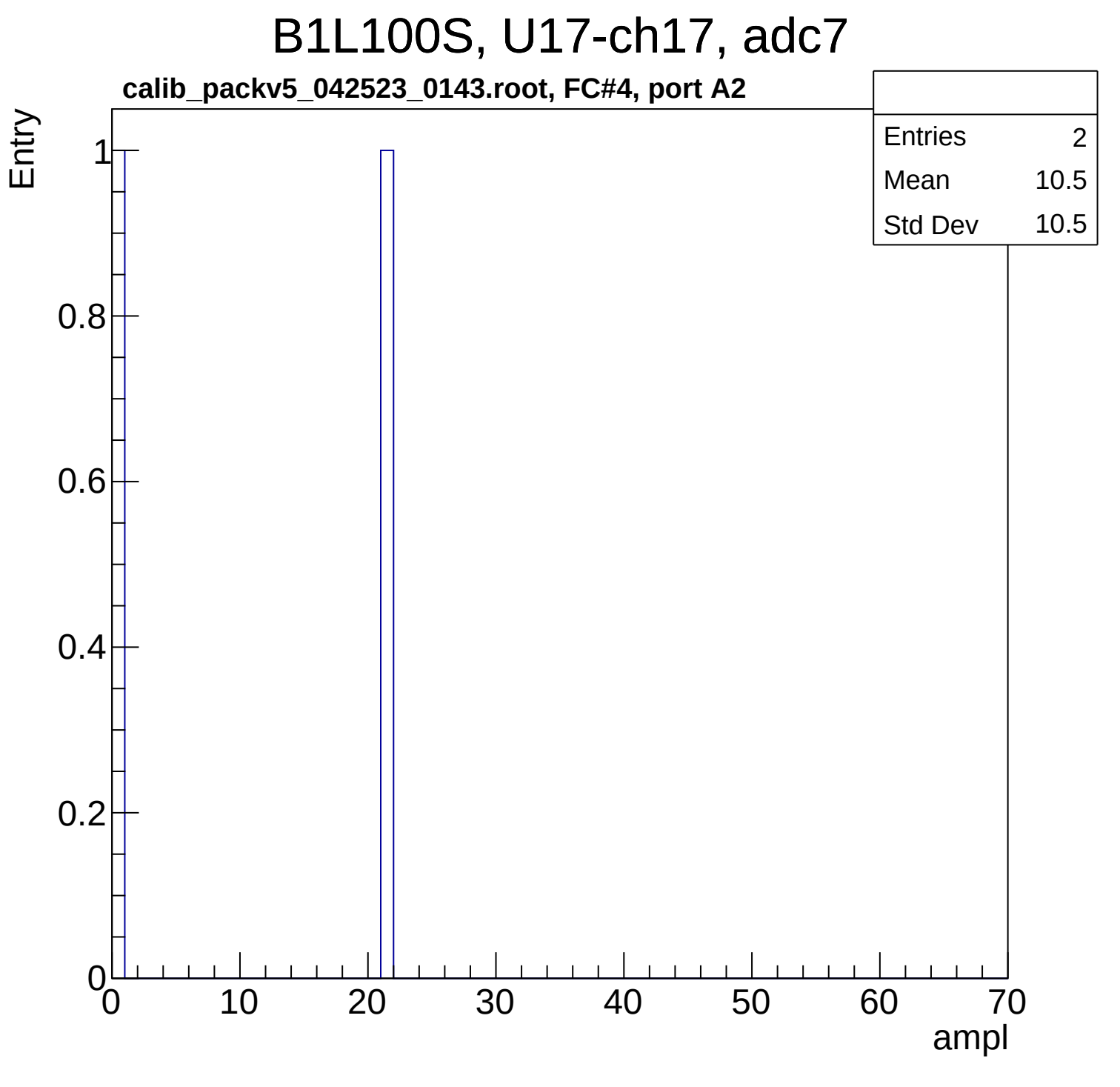

B1L100S, U17-ch17, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 42.38
Std Dev 3.592
Gaus mean : 42.7444
Gaus Width: 3.6267
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

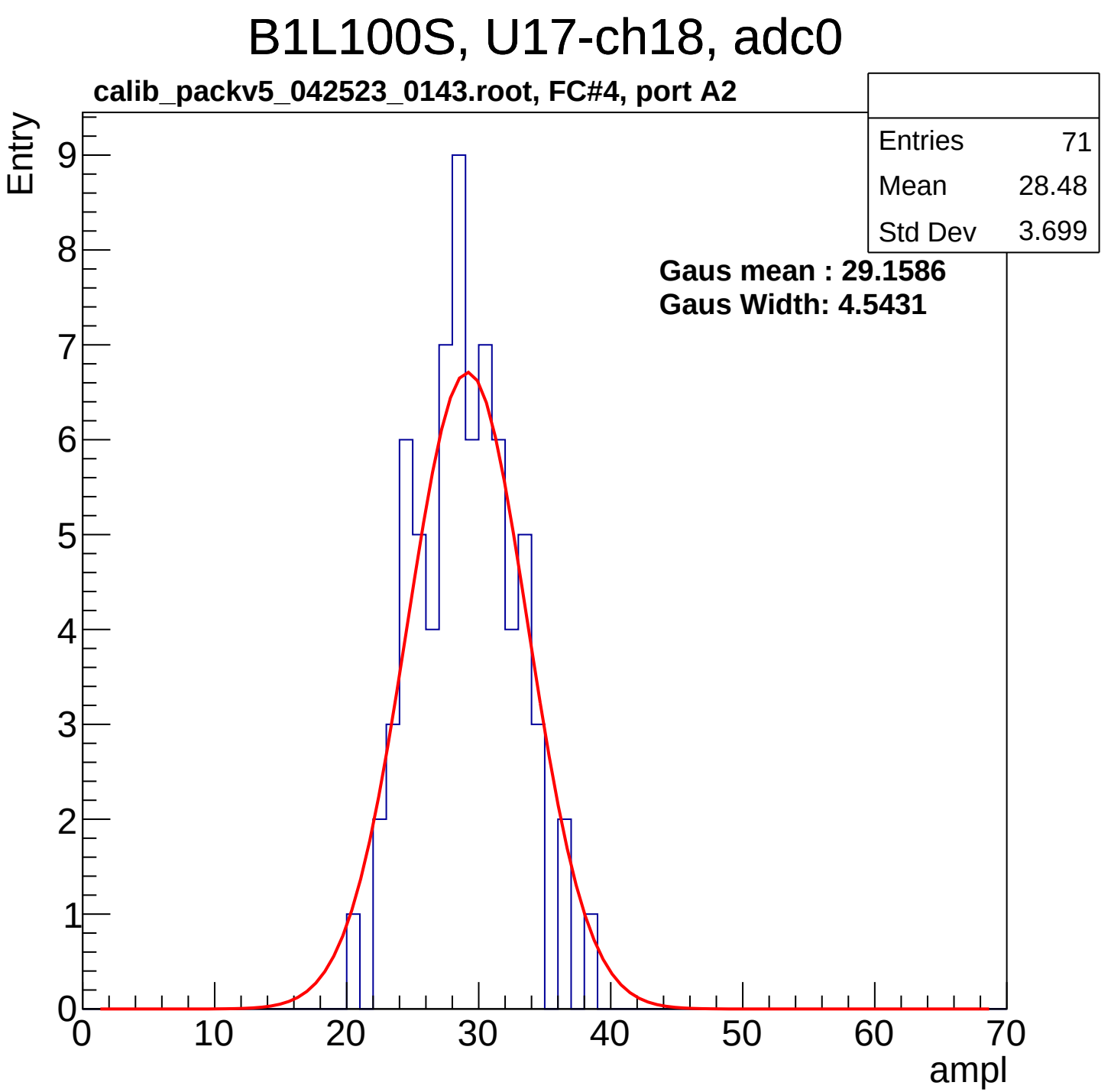

B1L100S, U17-ch17, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 48.89
Std Dev 3.852
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch17, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 54.87
Std Dev 3.405
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch17, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 59.02
Std Dev 8.705
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U17-ch17, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 60.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch17, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 10.5
Std Dev 10.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch18, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 28.48
Std Dev 3.699
Gaus mean : 29.1586
Gaus Width: 4.5431
Entry
ampl
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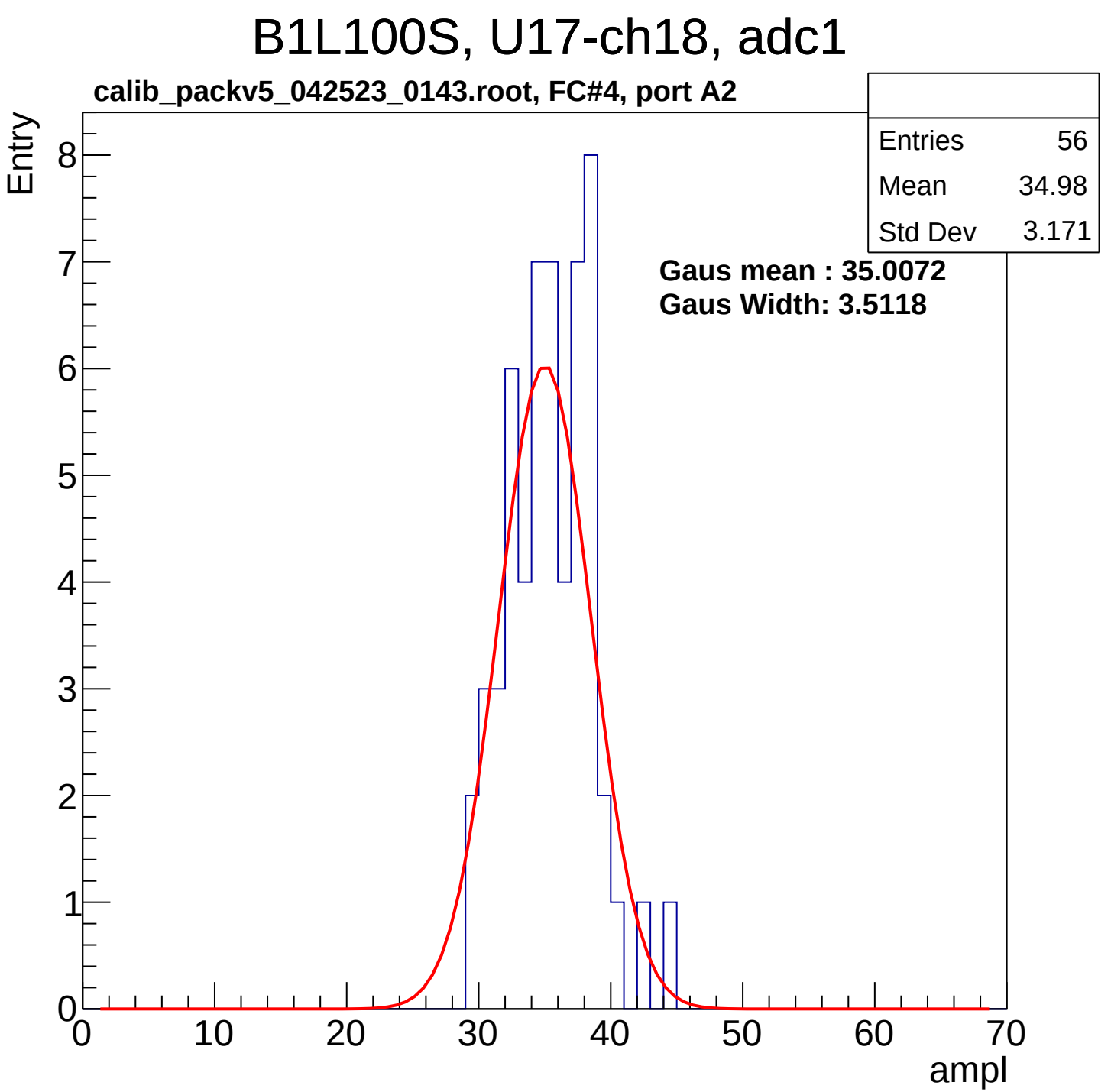
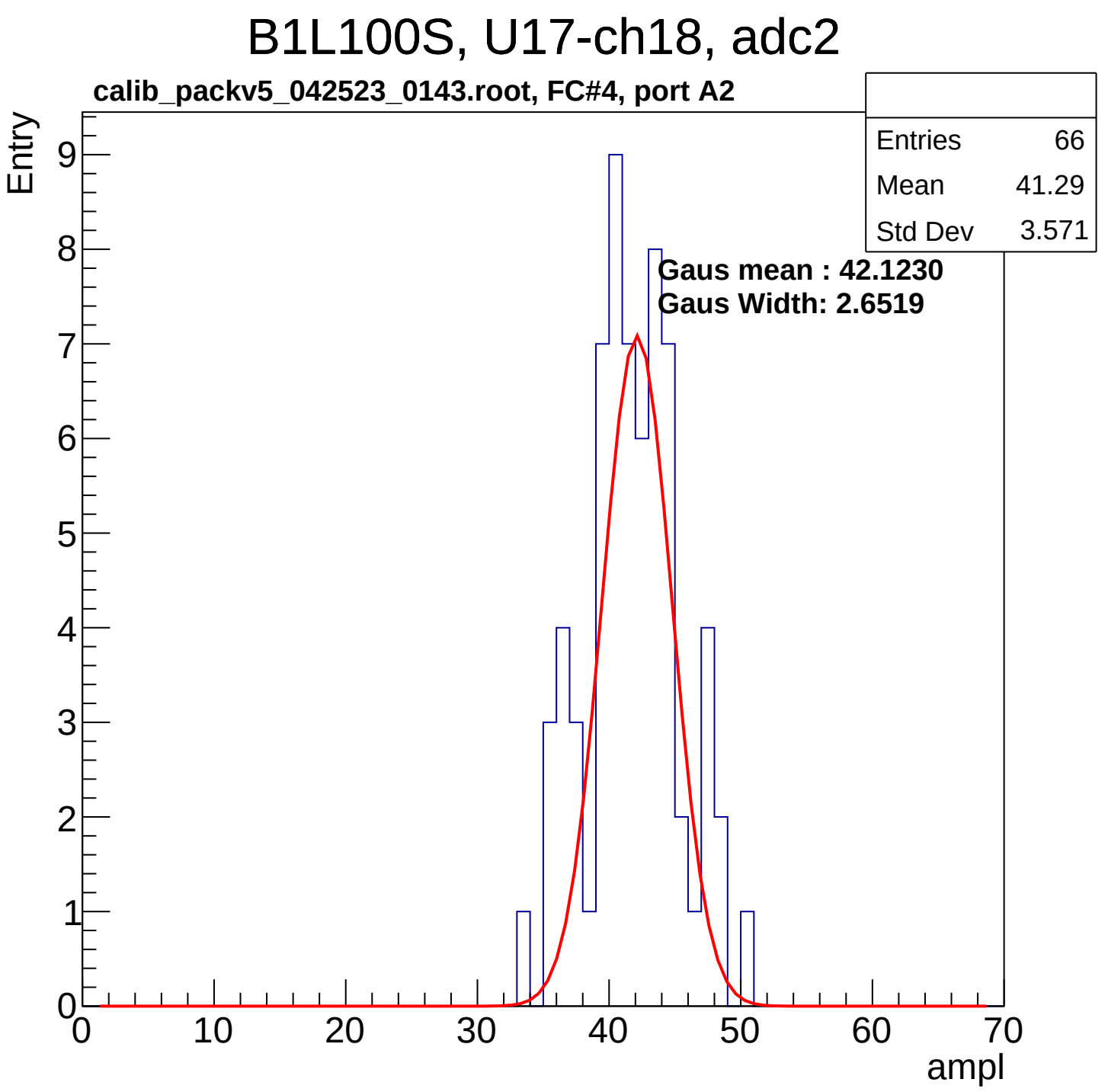
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch18, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 34.98
Std Dev 3.171
Gaus mean : 35.0072
Gaus Width: 3.5118
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch18, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 41.29
Std Dev 3.571
Gaus mean : 42.1230
Gaus Width: 2.6519
Entry
ampl
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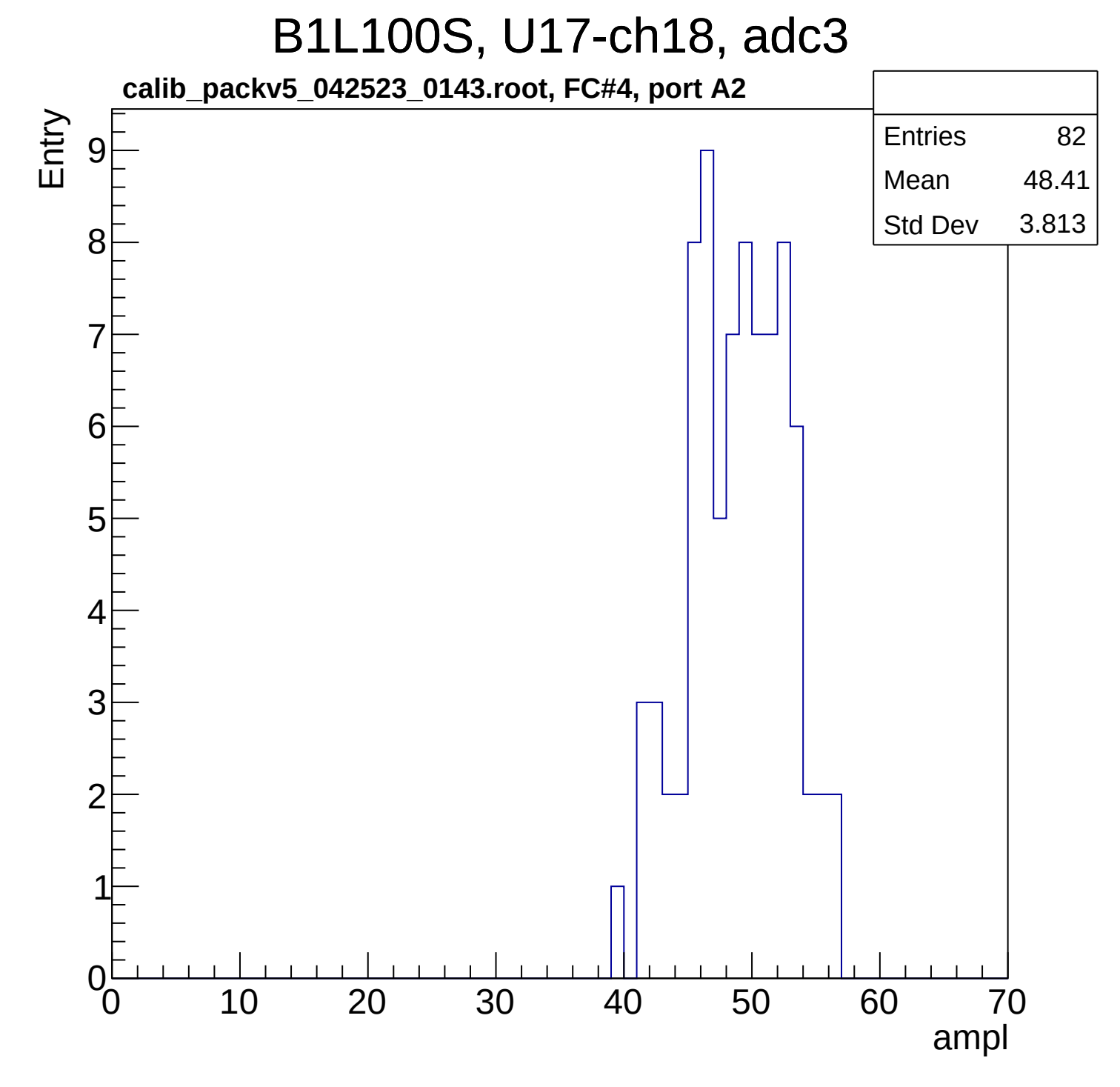
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch18, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 82
Mean 48.41
Std Dev 3.813
Entry
ampl
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3
4
5
6
7
8
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0
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40
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60
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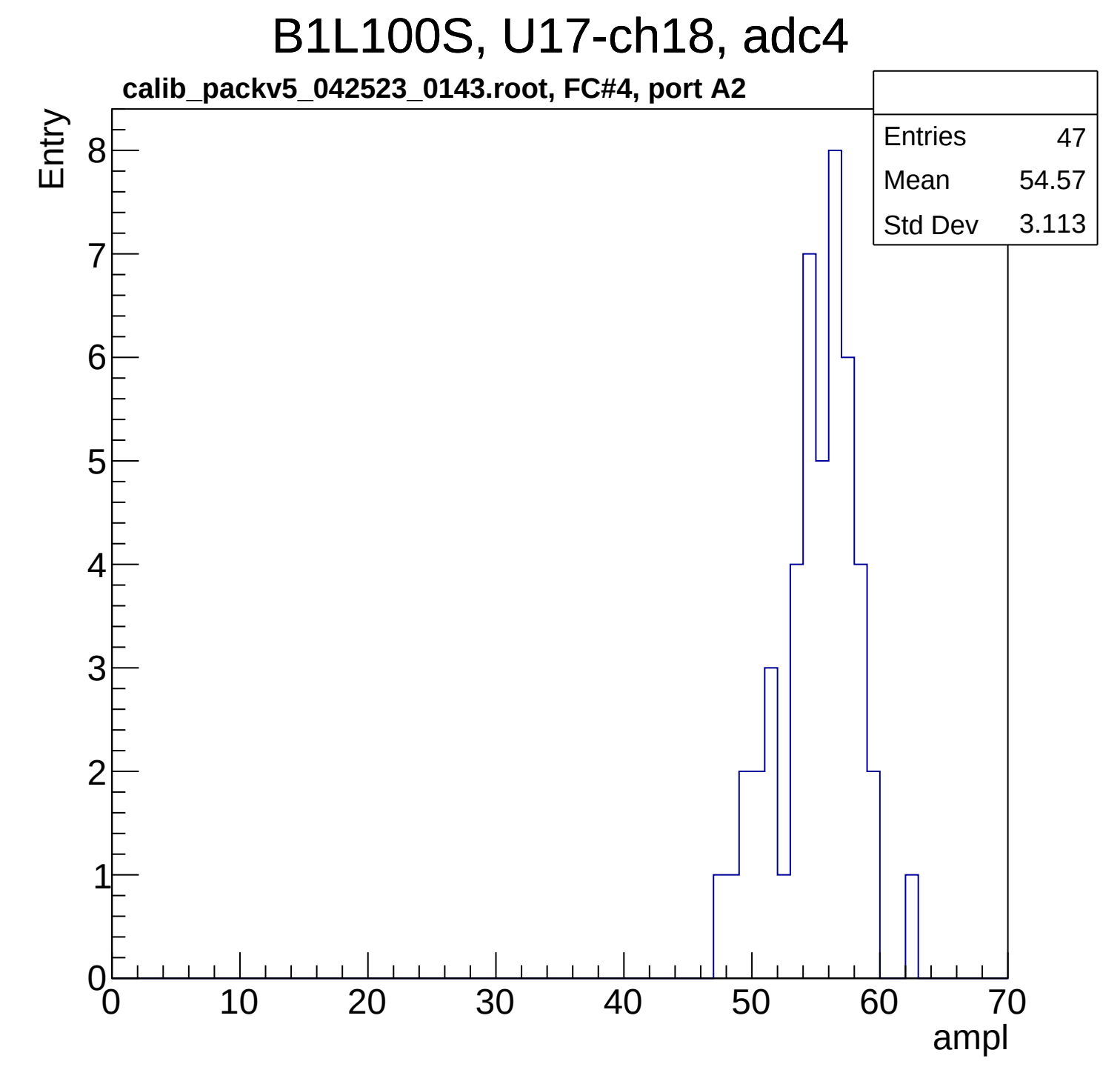
B1L100S, U17-ch18, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 47
Mean 54.57
Std Dev 3.113
Entry
ampl
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1
2
3
4
5
6
7
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0
10
20
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40
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60
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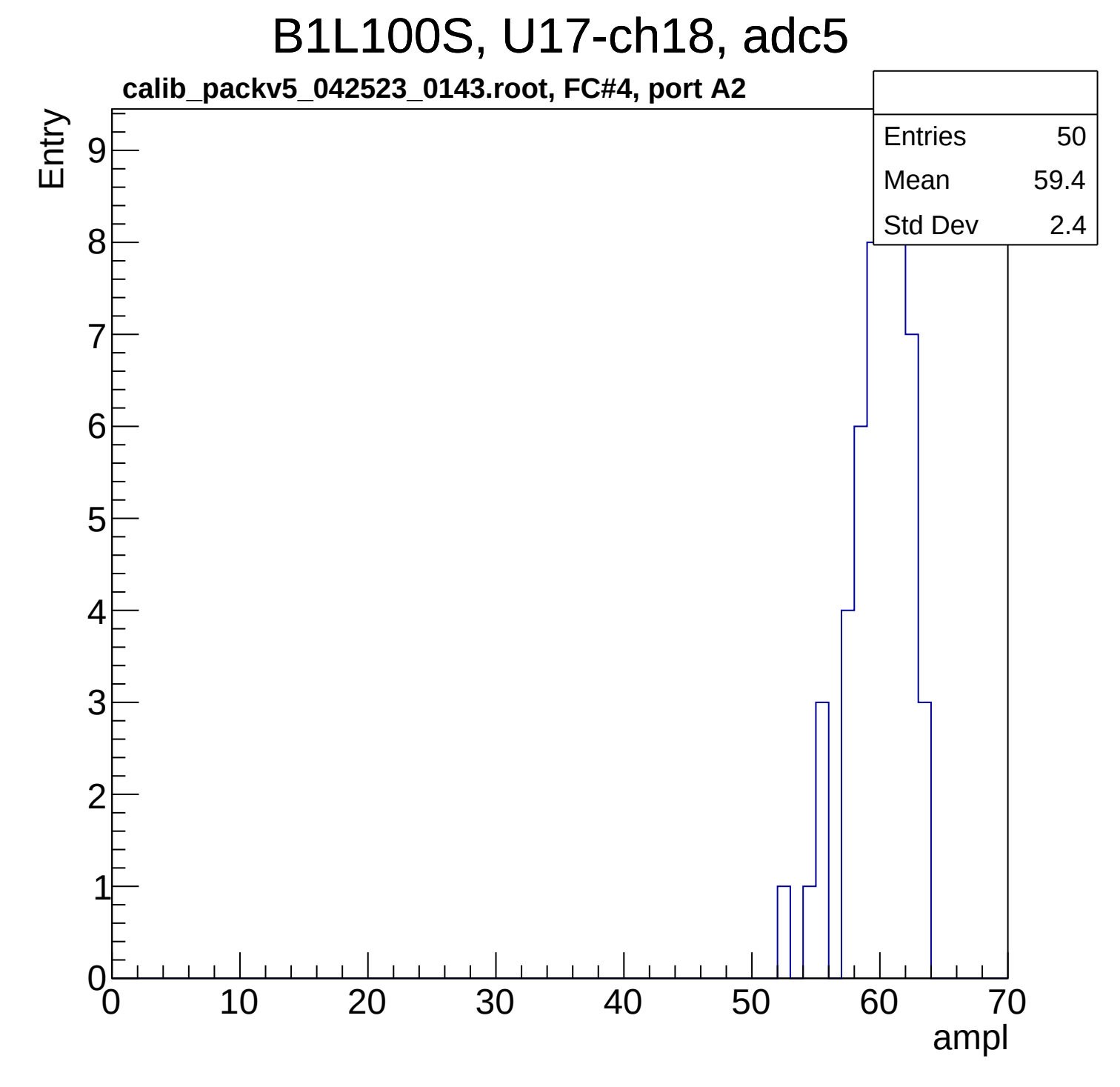
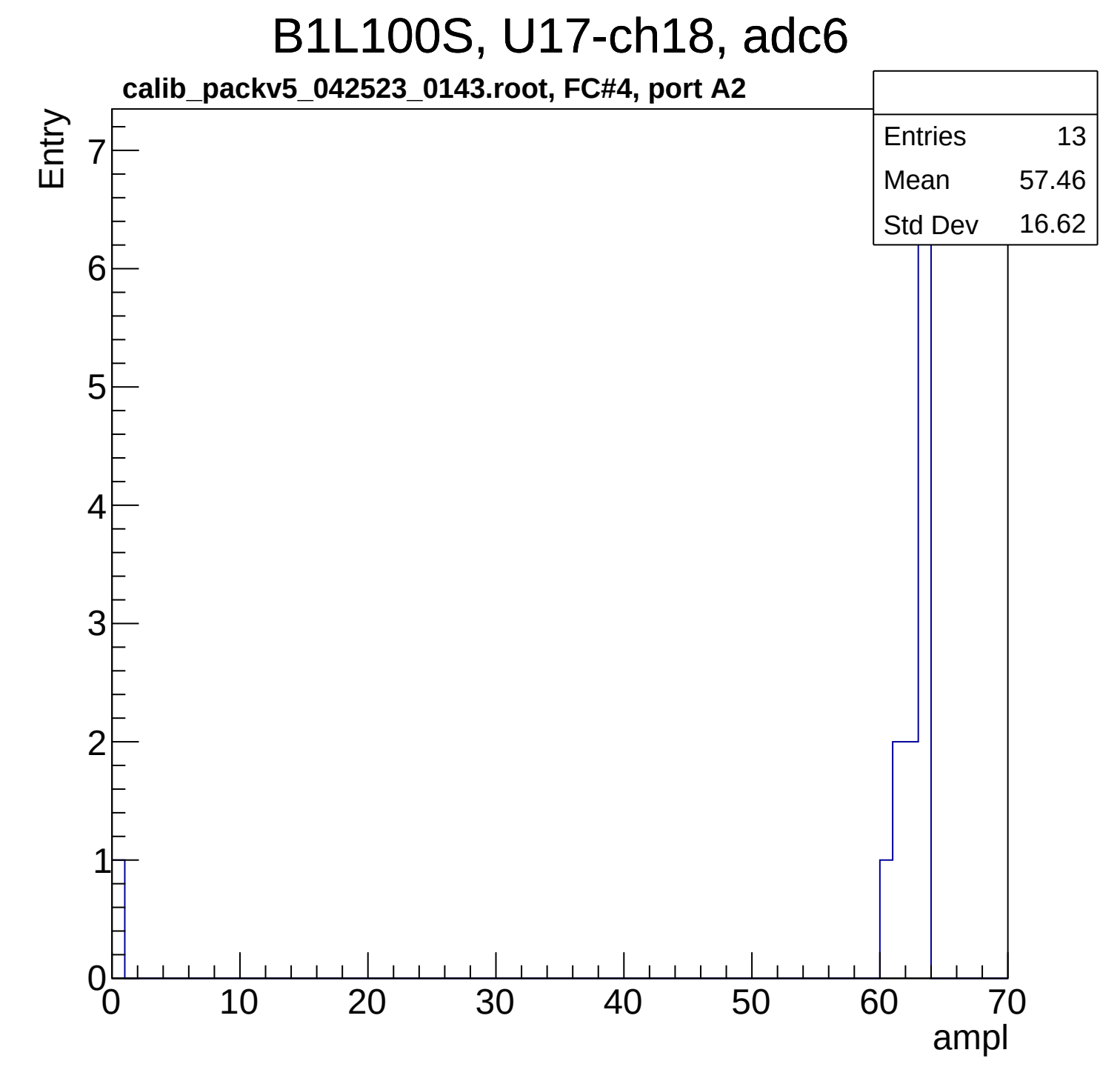
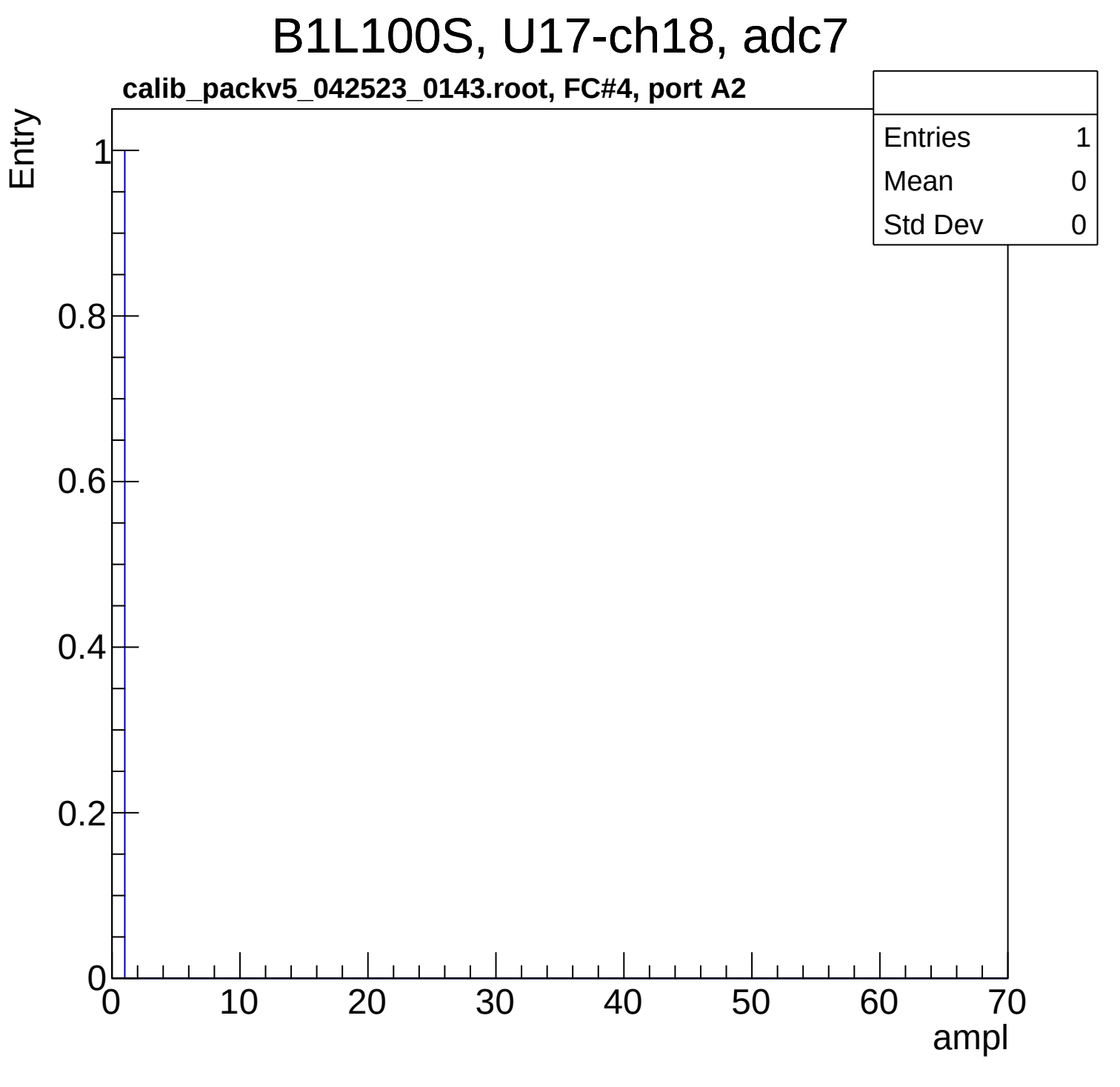
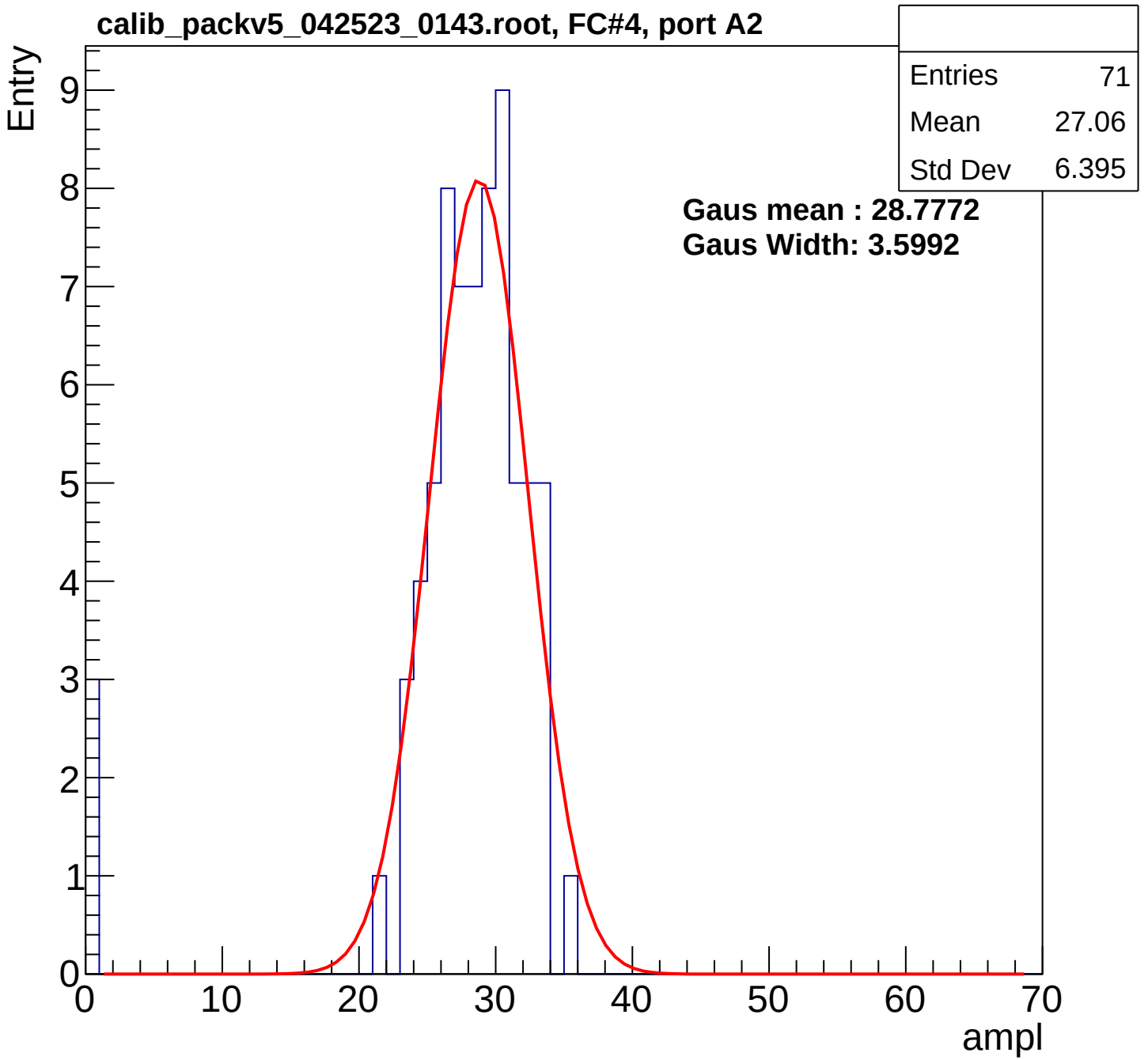

B1L100S, U17-ch18, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 59.4
Std Dev 2.4
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch18, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 13
Mean 57.46
Std Dev 16.62
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U17-ch18, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch19, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 27.06
Std Dev 6.395
Gaus mean : 28.7772
Gaus Width: 3.5992
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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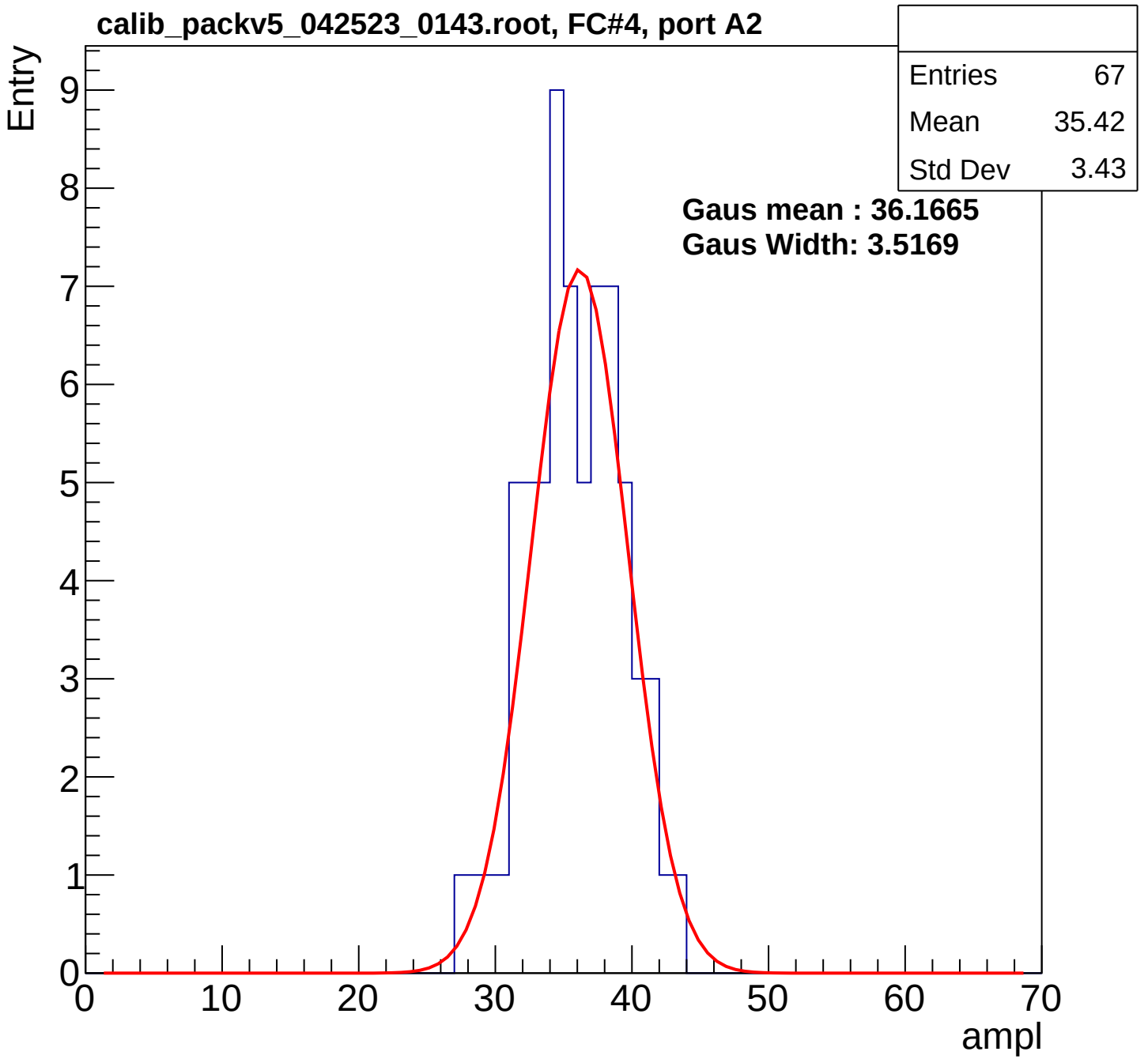
B1L100S, U17-ch19, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 35.42
Std Dev 3.43
Gaus mean : 36.1665
Gaus Width: 3.5169
Entry
ampl
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1
2
3
4
5
6
7
8
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0
10
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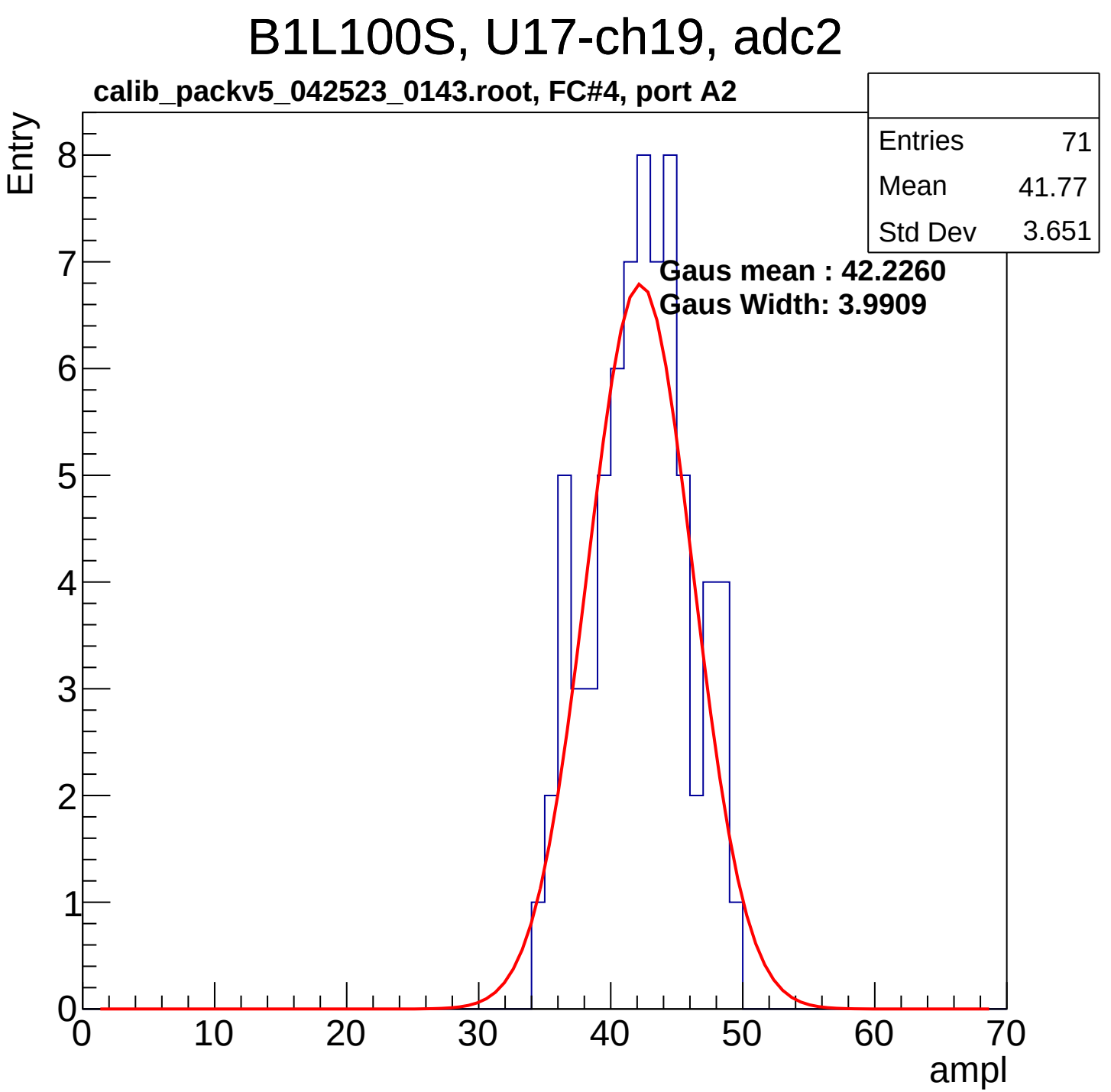
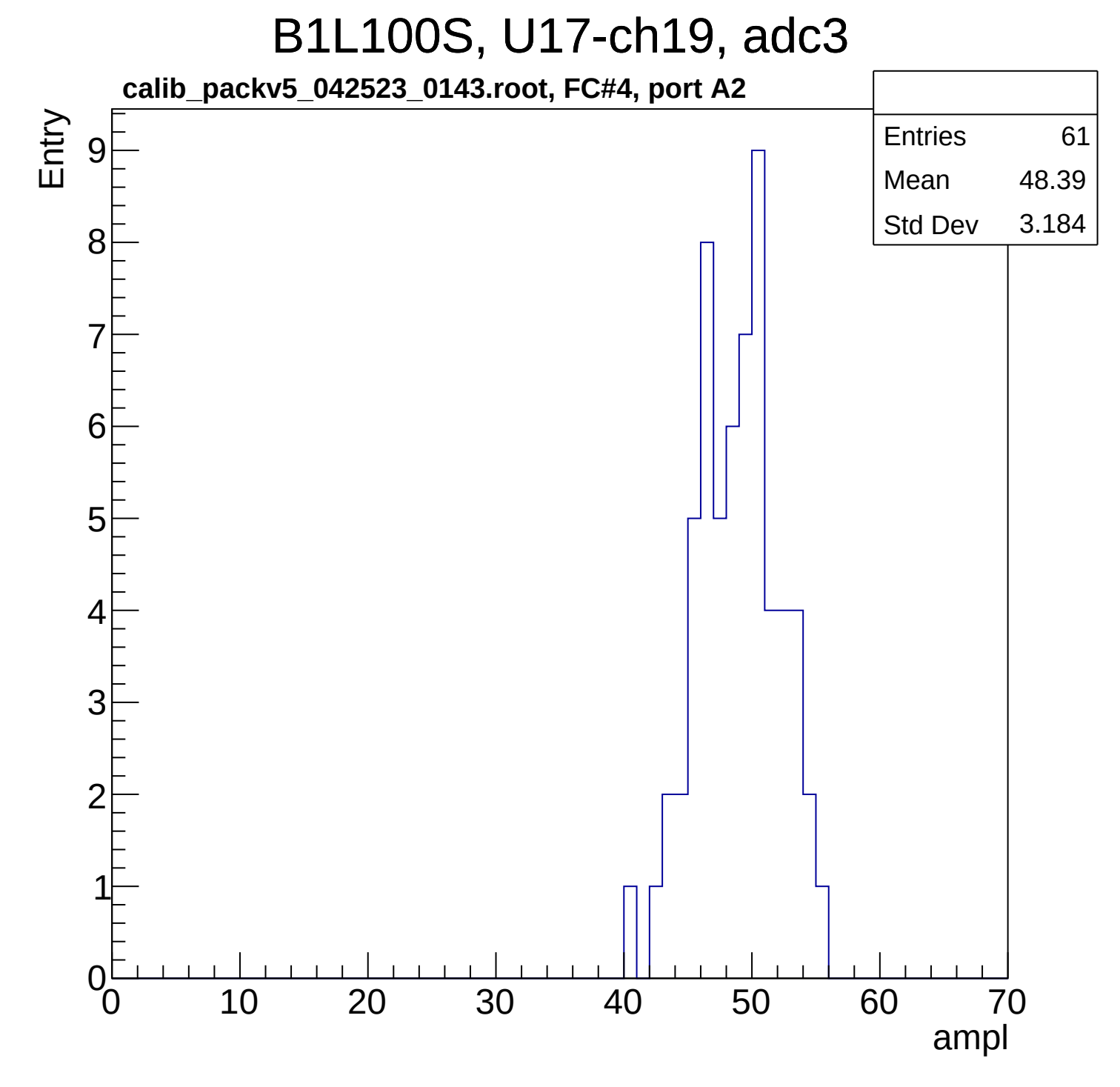
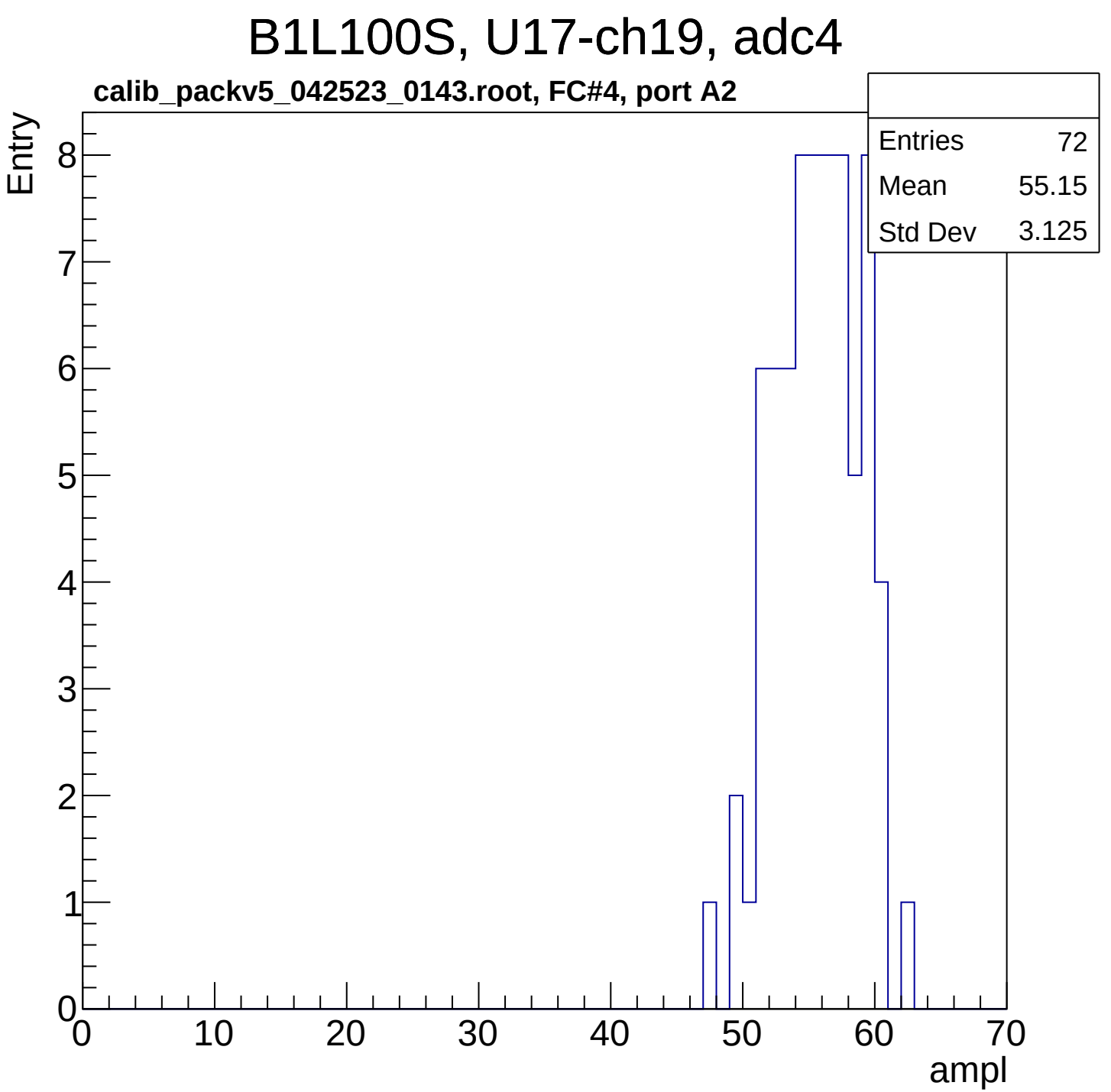
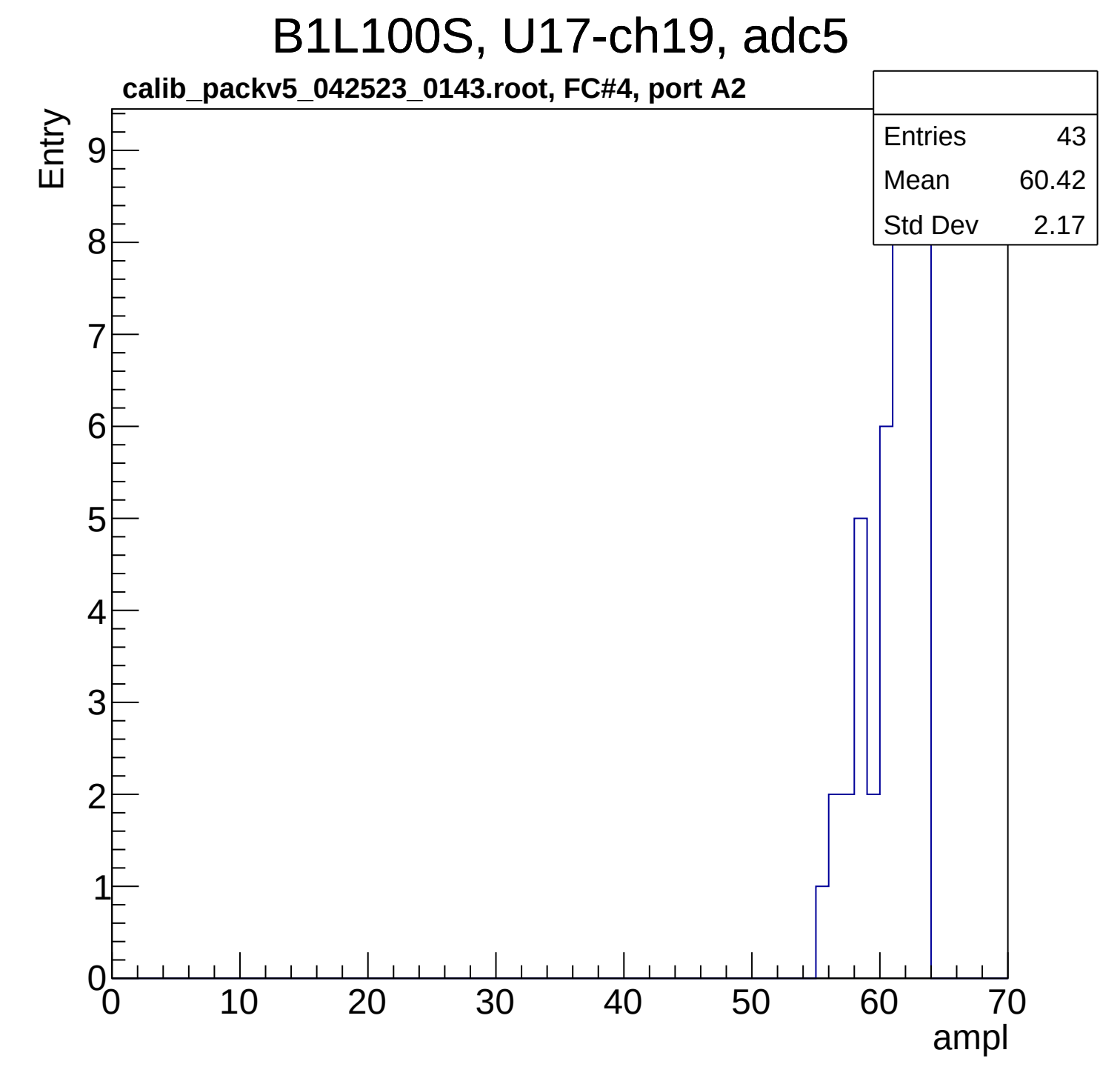
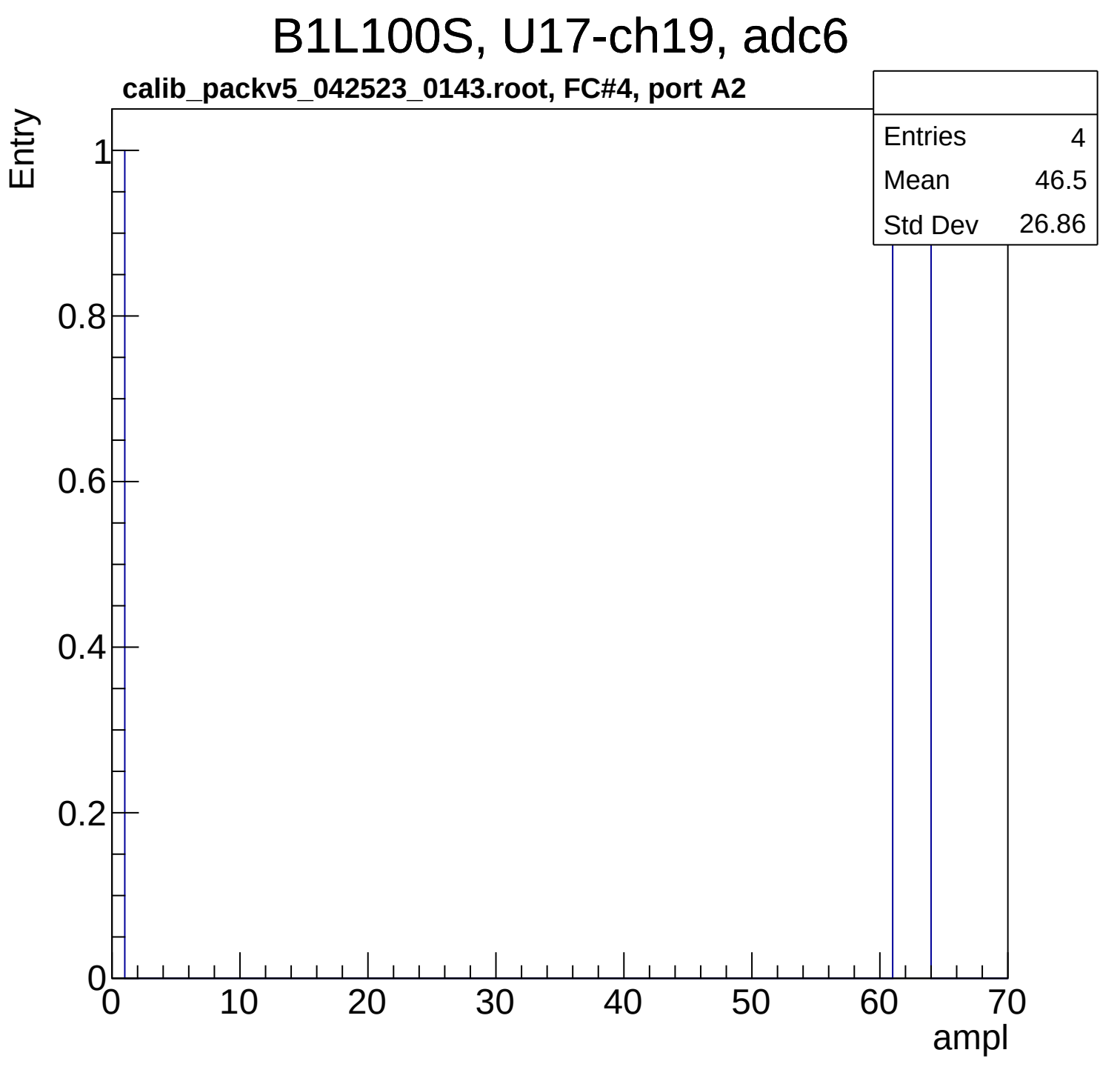
60
70

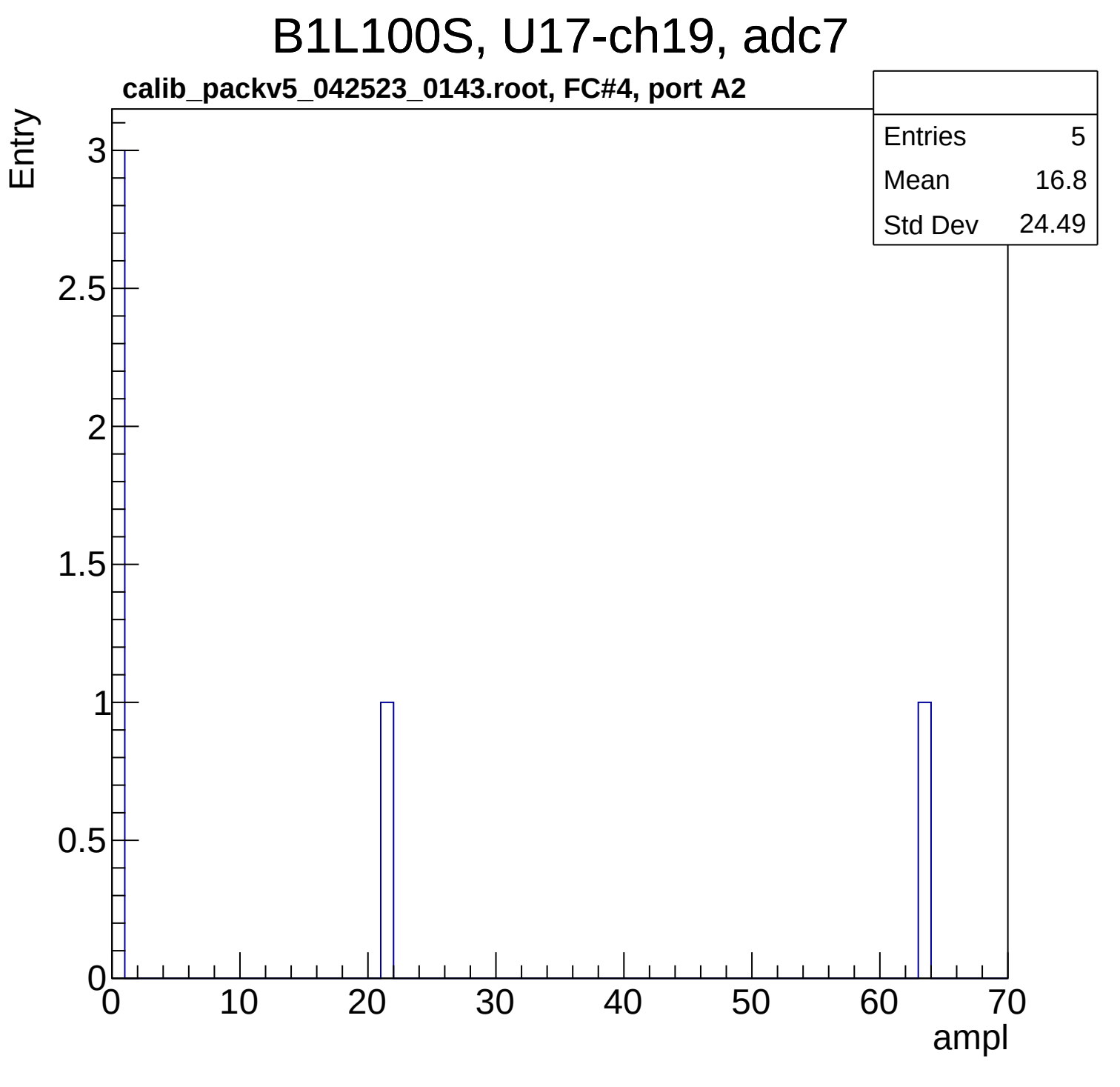

B1L100S, U17-ch19, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 41.77
Std Dev 3.651
Gaus mean : 42.2260
Gaus Width: 3.9909
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

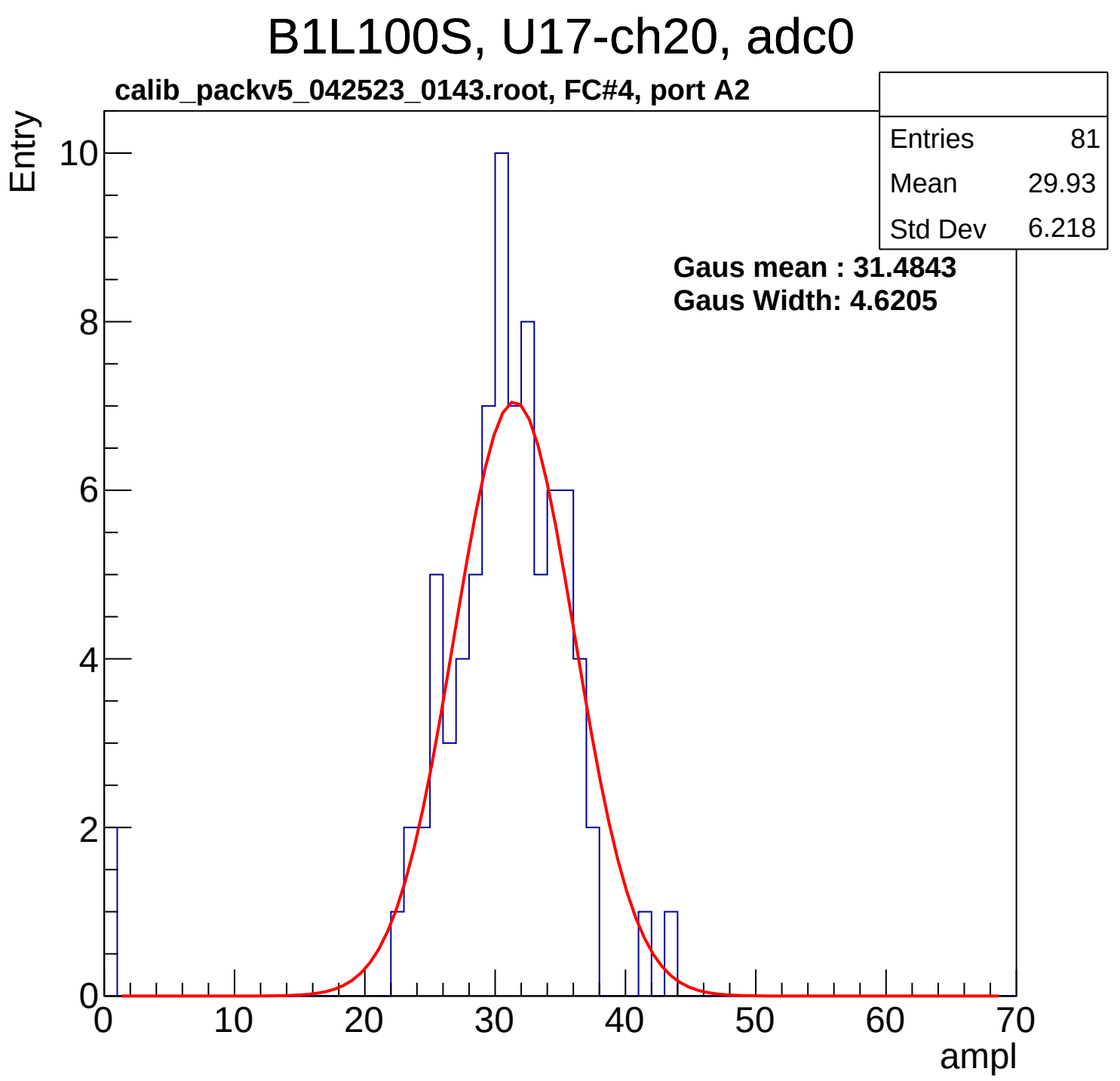

B1L100S, U17-ch19, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 48.39
Std Dev 3.184
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

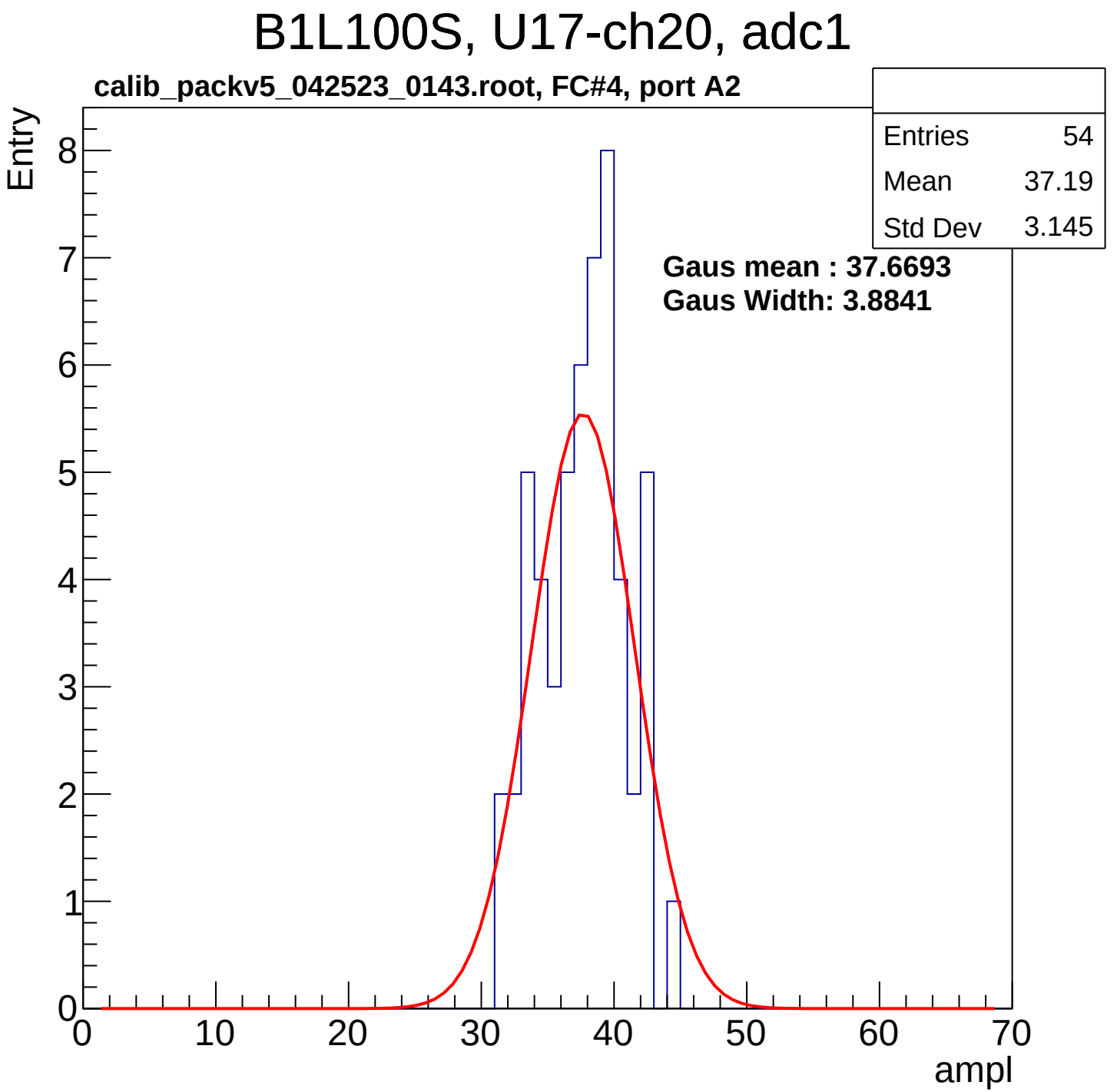

B1L100S, U17-ch19, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 55.15
Std Dev 3.125
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

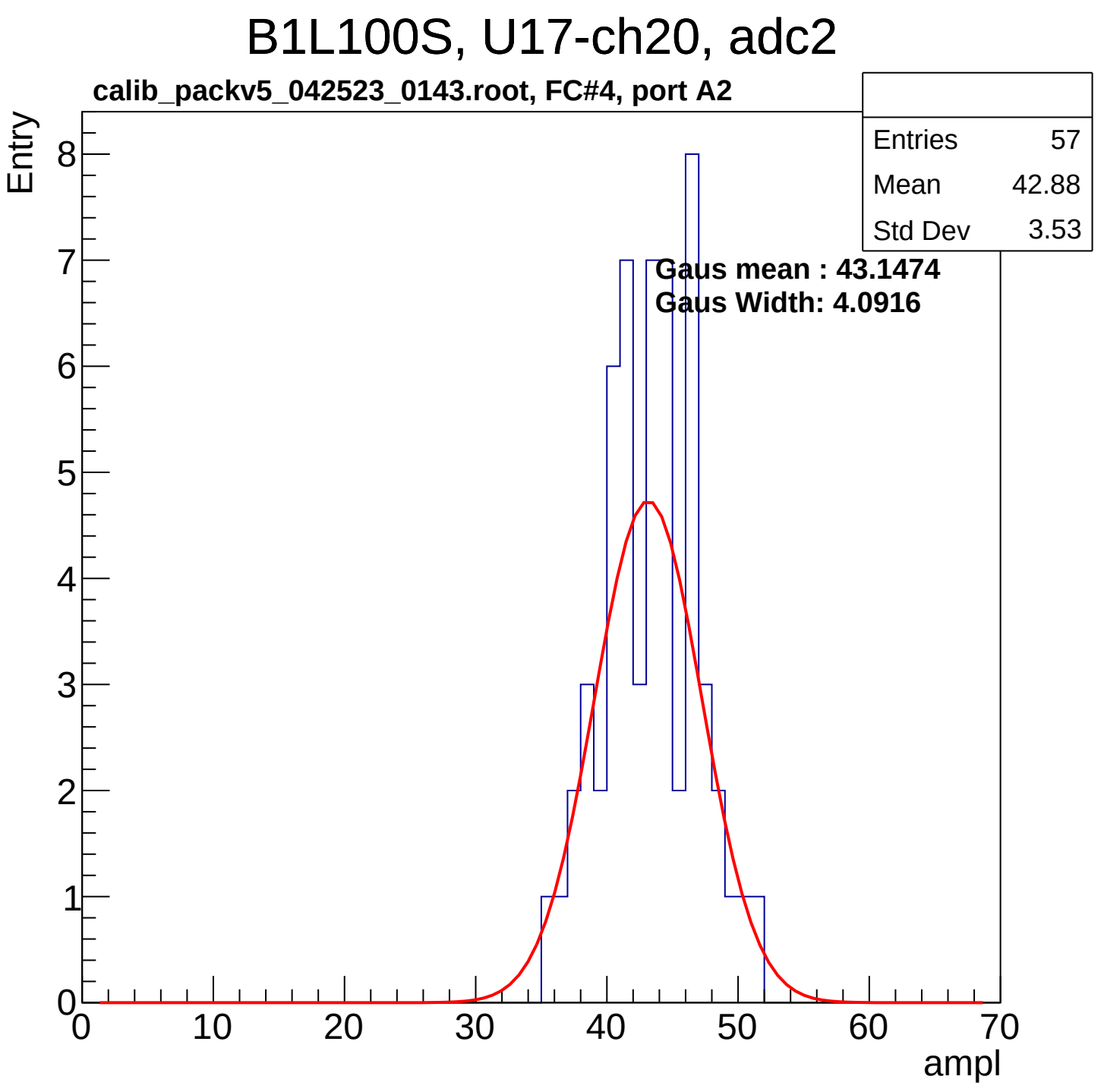

B1L100S, U17-ch19, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 43
Mean 60.42
Std Dev 2.17
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

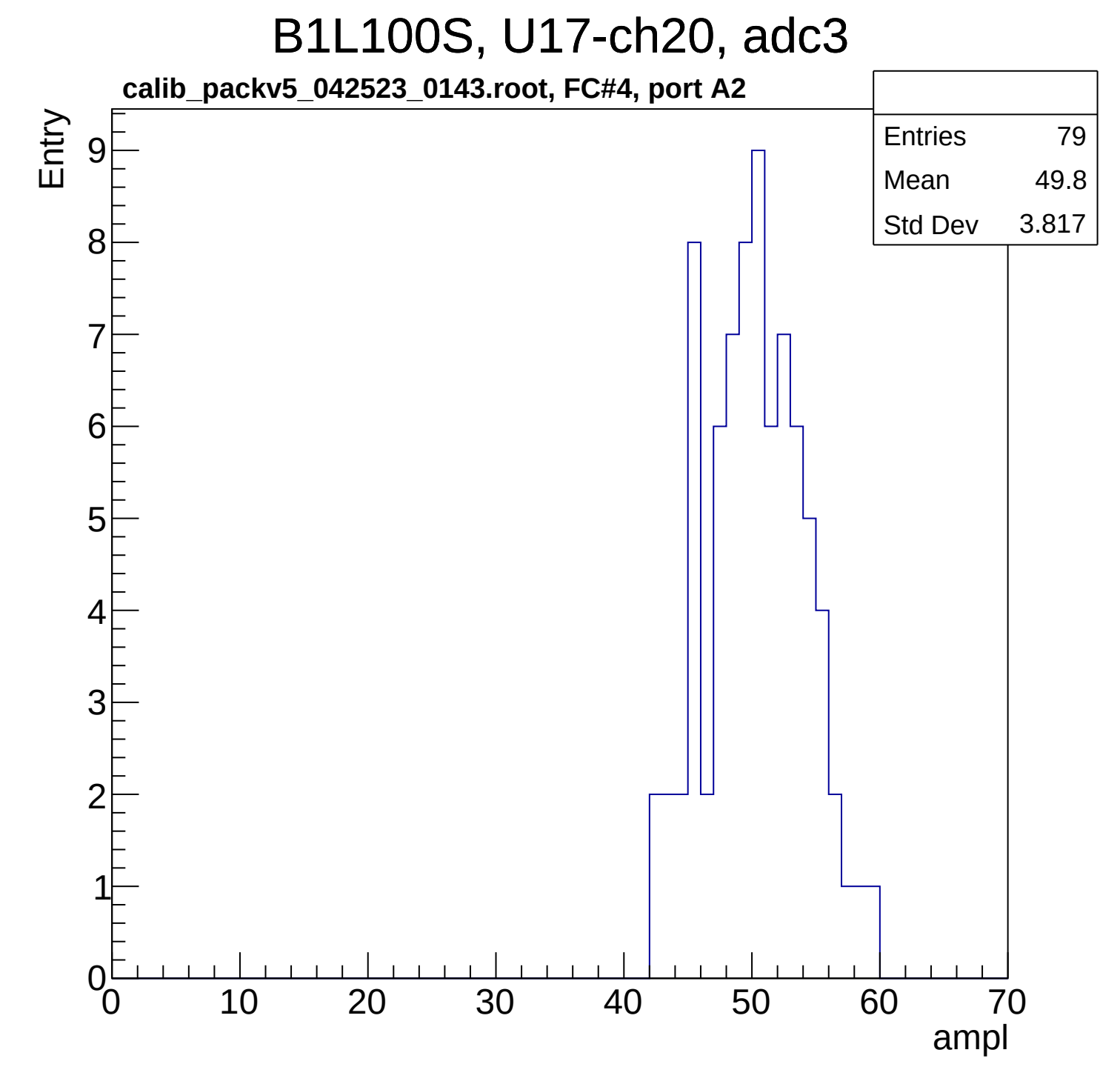

B1L100S, U17-ch19, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 4
Mean 46.5
Std Dev 26.86
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

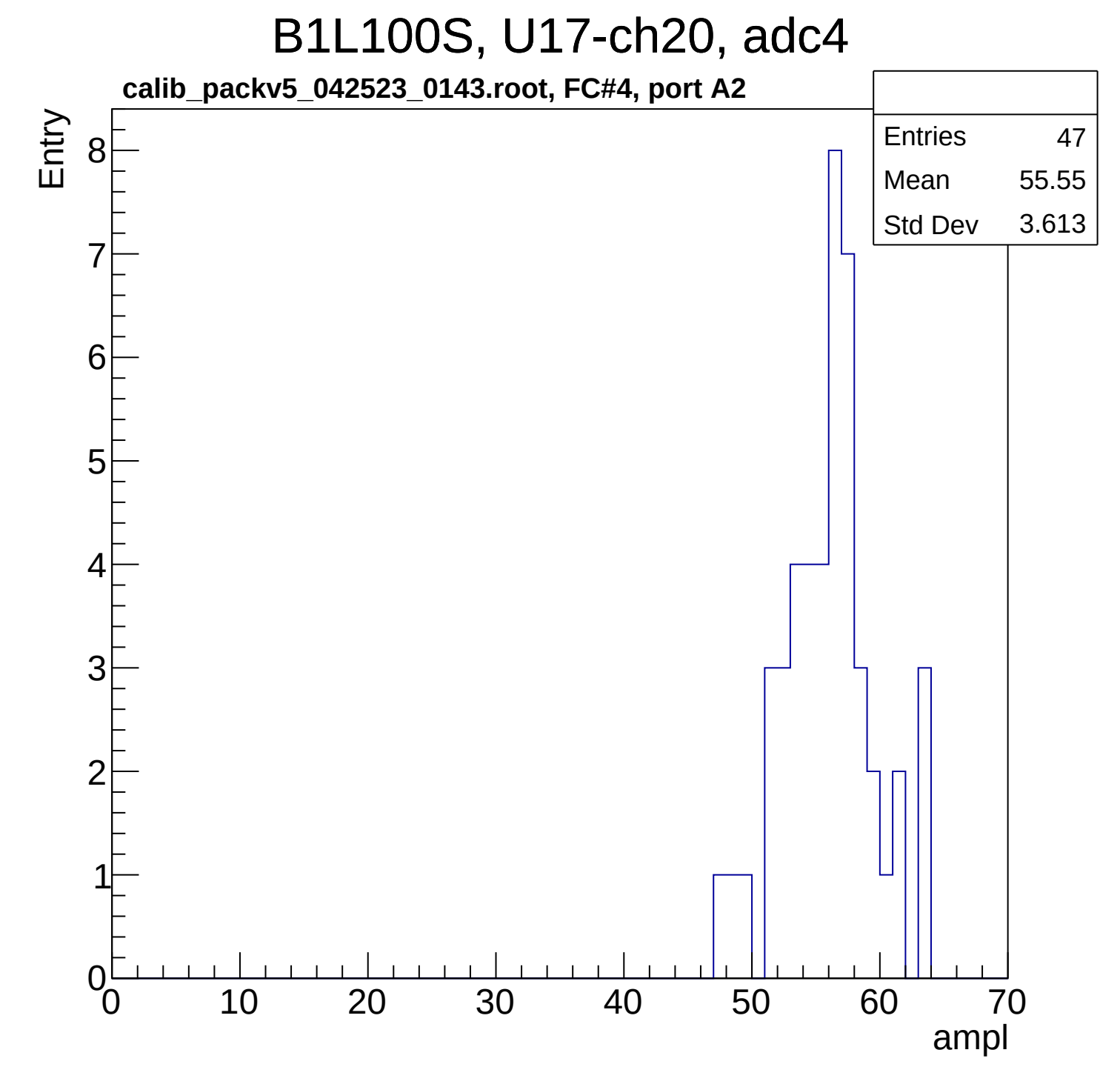

B1L100S, U17-ch19, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 5
Mean 16.8
Std Dev 24.49
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

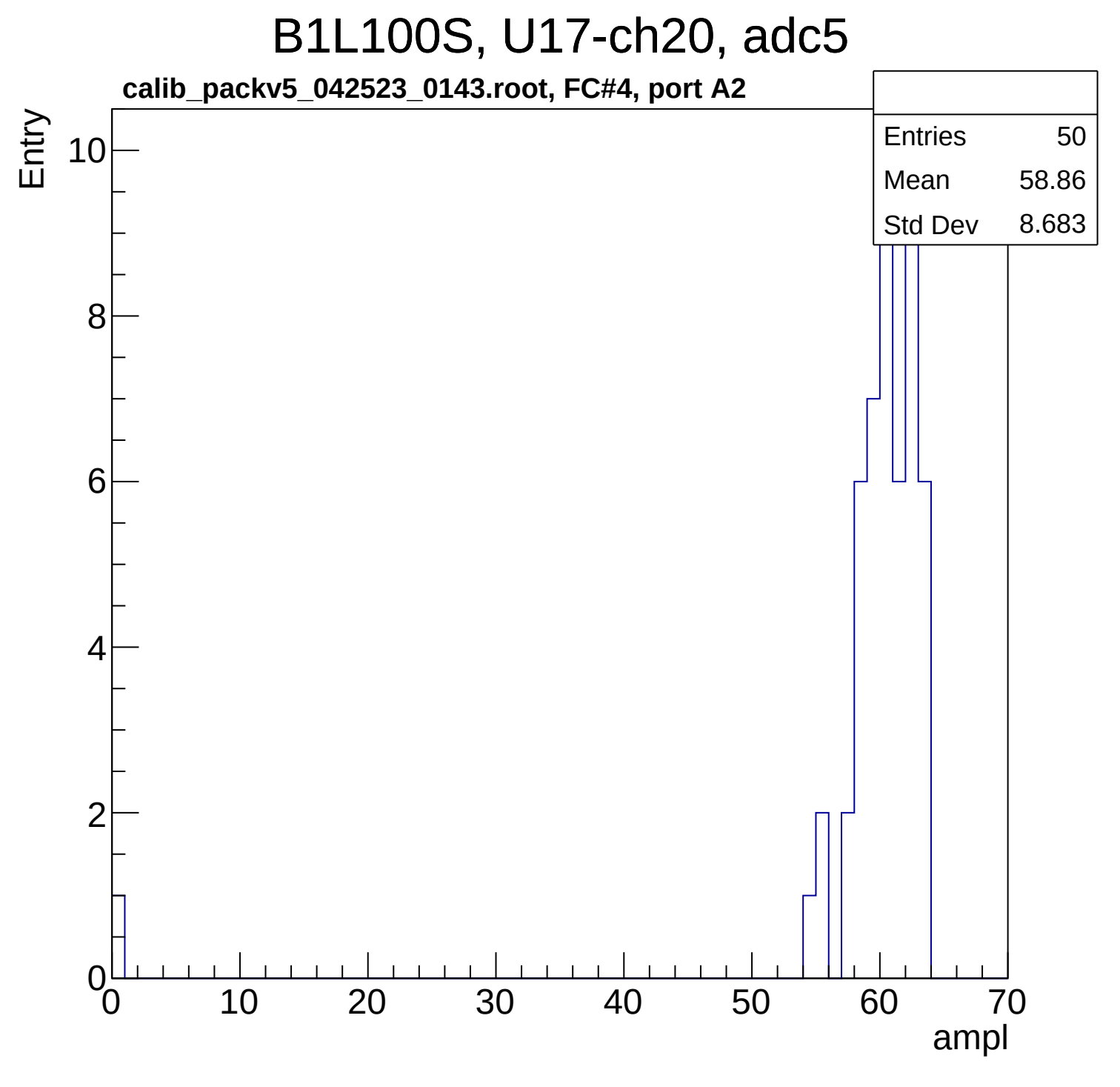

B1L100S, U17-ch20, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 81
Mean 29.93
Std Dev 6.218
Gaus mean : 31.4843
Gaus Width: 4.6205
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

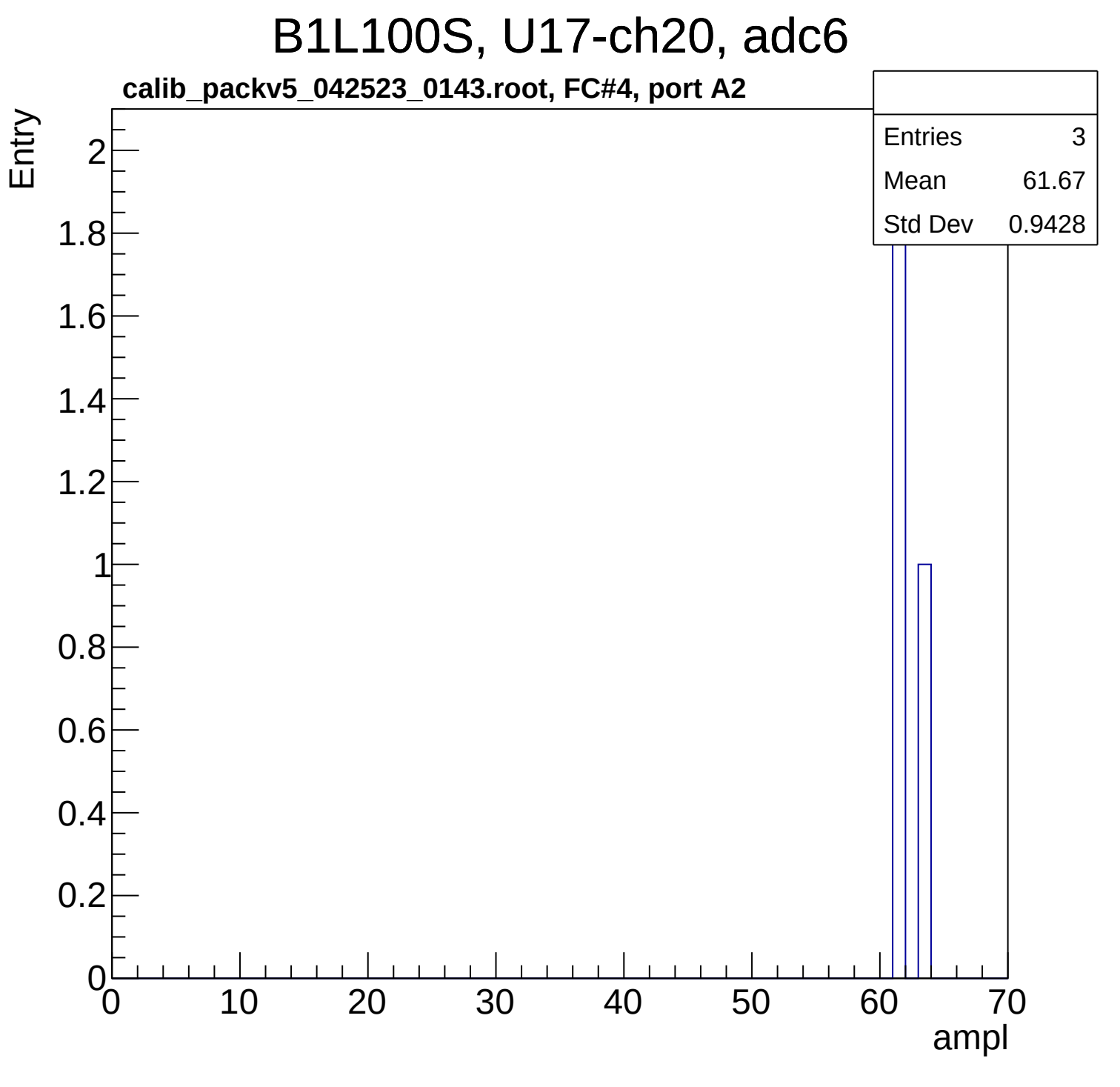

B1L100S, U17-ch20, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 37.19
Std Dev 3.145
Gaus mean : 37.6693
Gaus Width: 3.8841
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

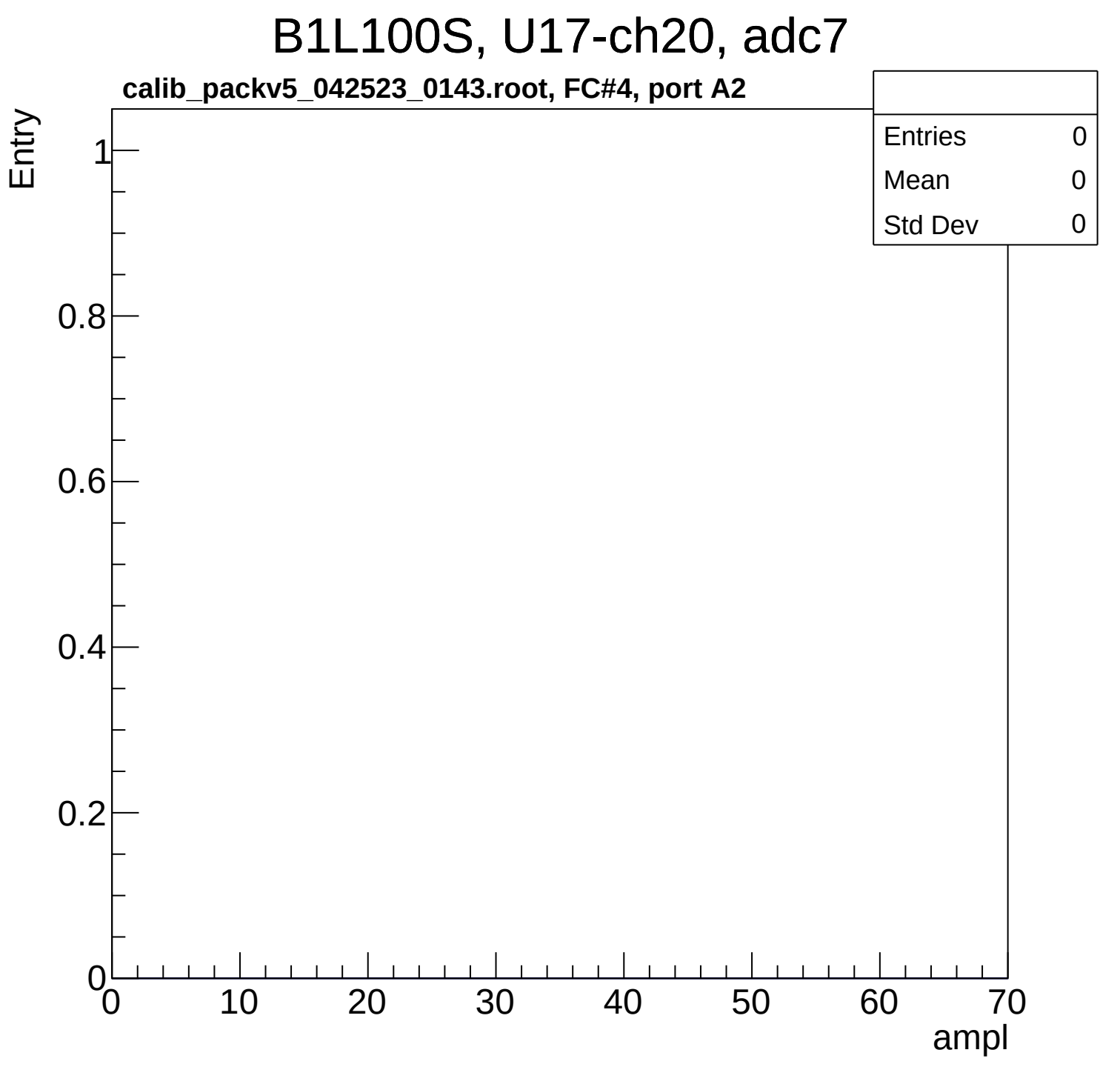

B1L100S, U17-ch20, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 42.88
Std Dev 3.53
Gaus mean : 43.1474
Gaus Width: 4.0916
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

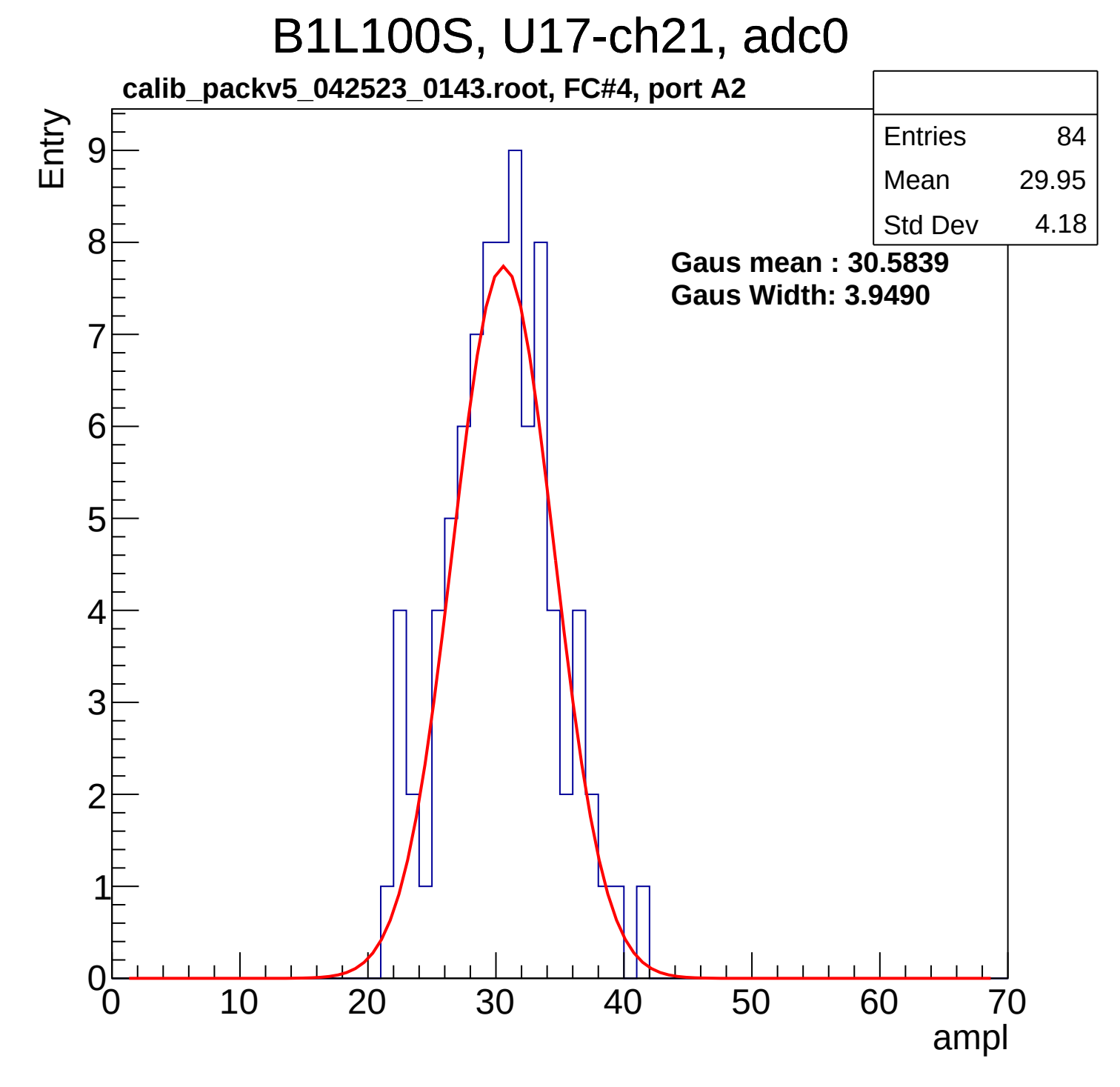

B1L100S, U17-ch20, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 79
Mean 49.8
Std Dev 3.817
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

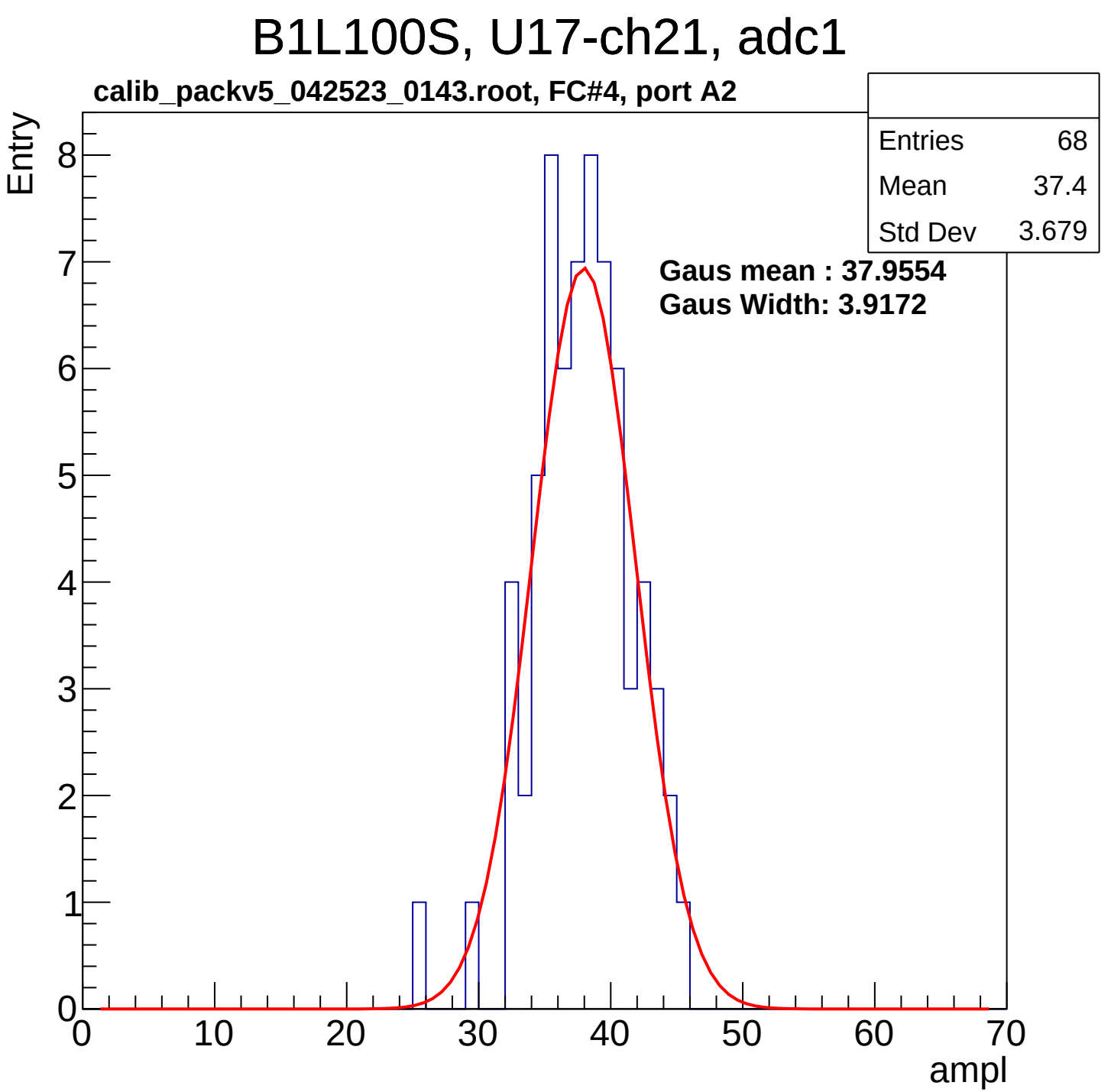

B1L100S, U17-ch20, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 47
Mean 55.55
Std Dev 3.613
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

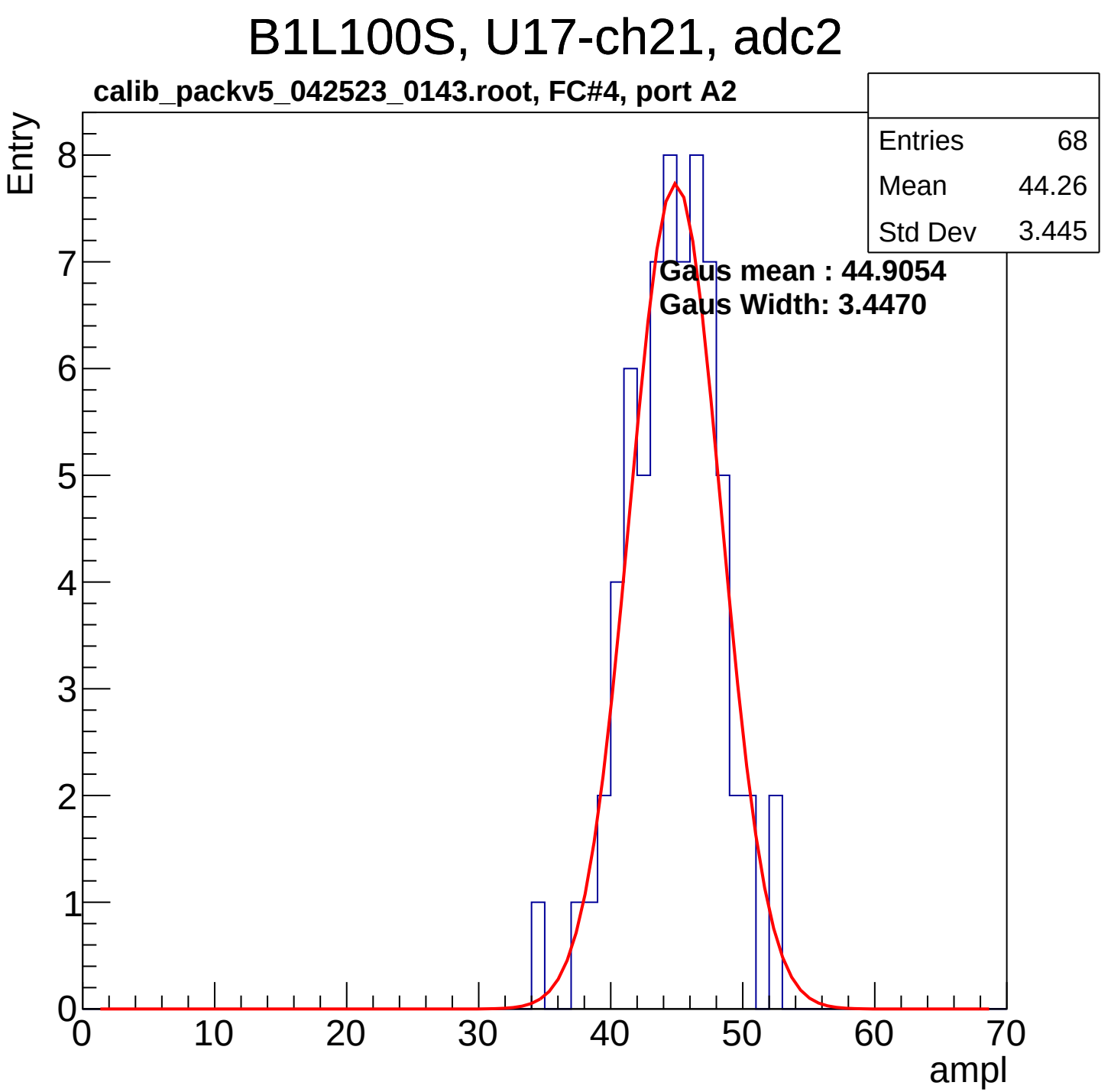

B1L100S, U17-ch20, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 58.86
Std Dev 8.683
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

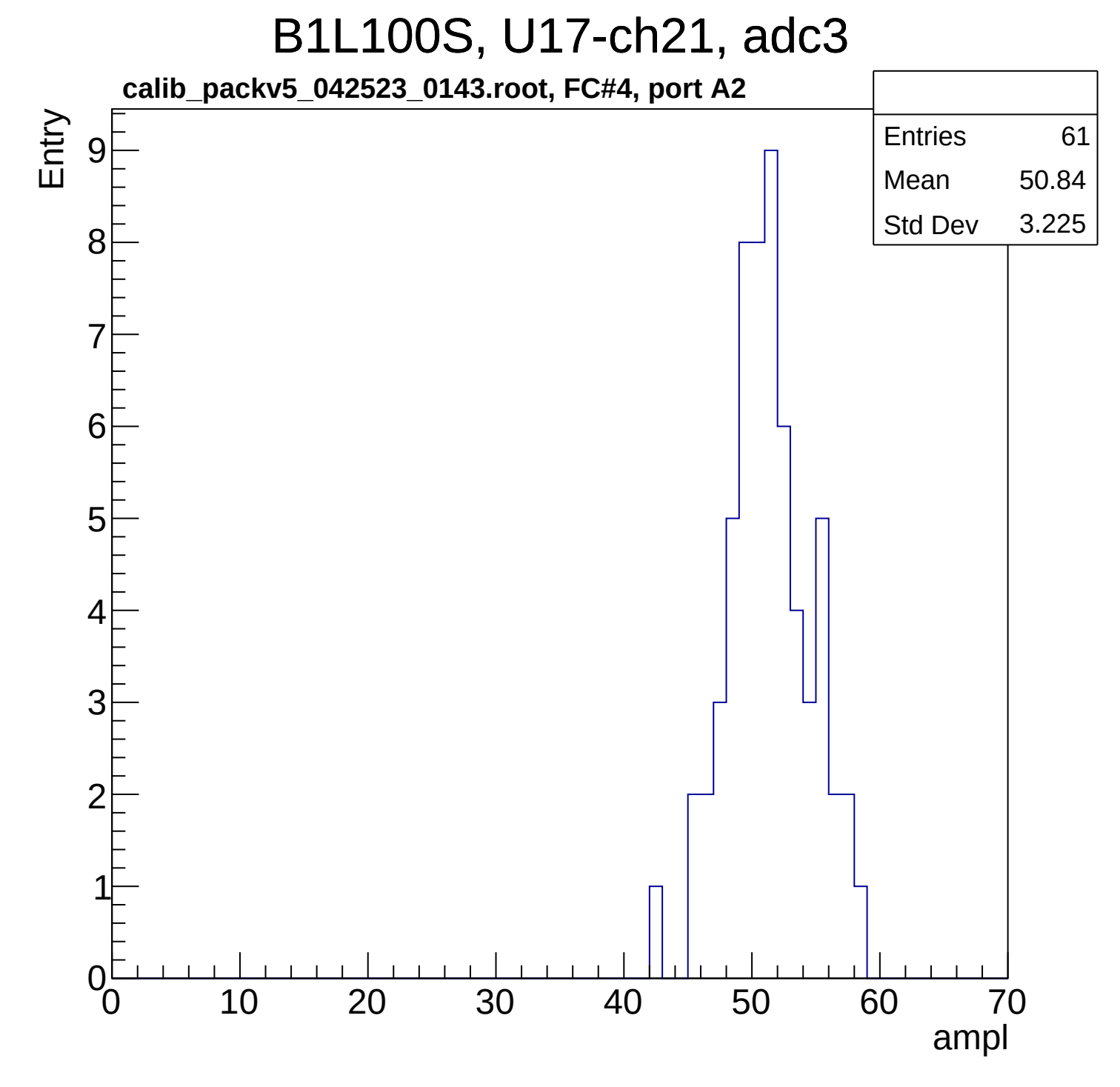

B1L100S, U17-ch20, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 61.67
Std Dev 0.9428
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

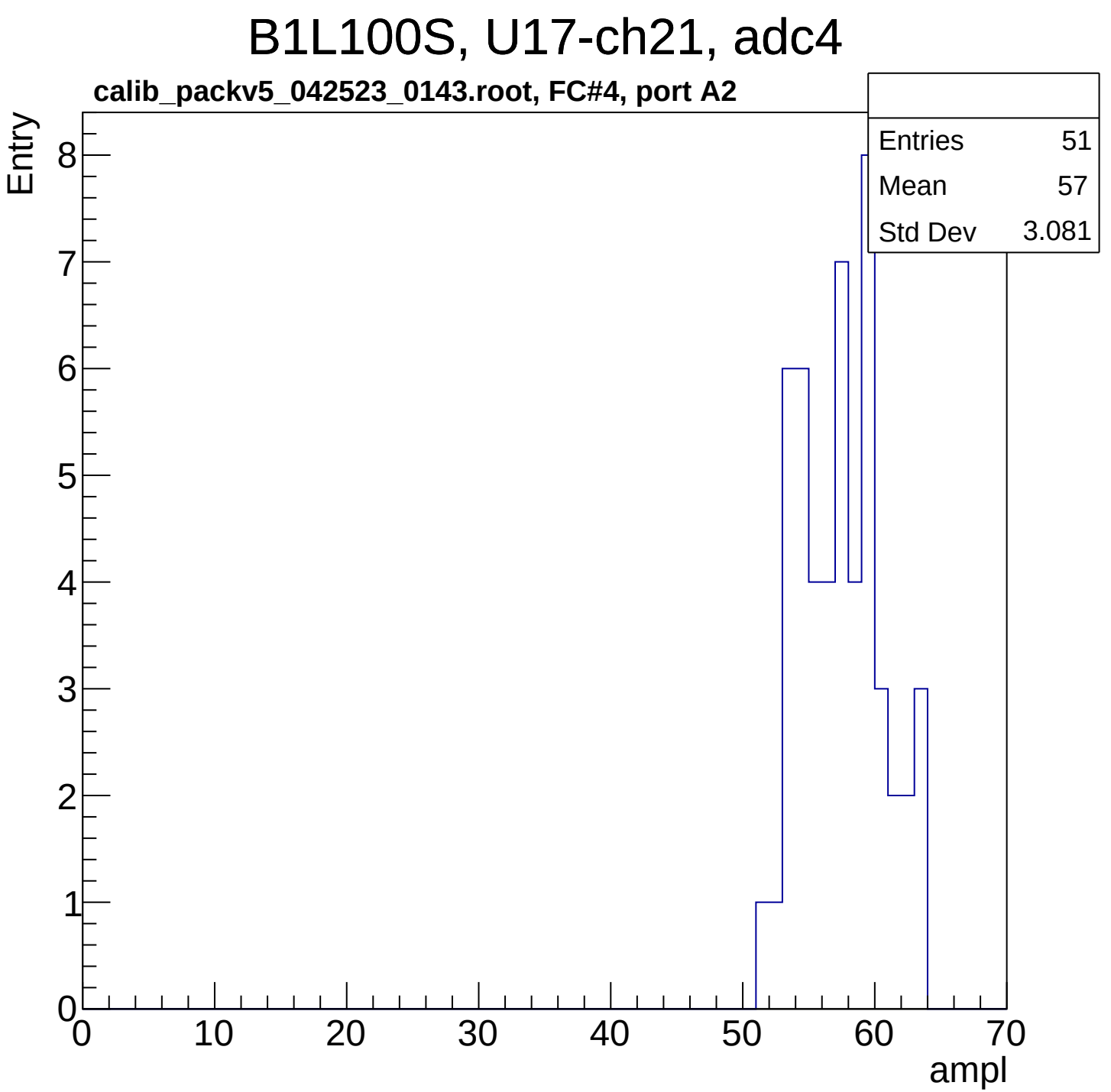

B1L100S, U17-ch20, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch21, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 84
Mean 29.95
Std Dev 4.18
Gaus mean : 30.5839
Gaus Width: 3.9490
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch21, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 37.4
Std Dev 3.679
Gaus mean : 37.9554
Gaus Width: 3.9172
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch21, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 44.26
Std Dev 3.445
Gaus mean : 44.9054
Gaus Width: 3.4470
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch21, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 50.84
Std Dev 3.225
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch21, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 57
Std Dev 3.081
Entry
ampl
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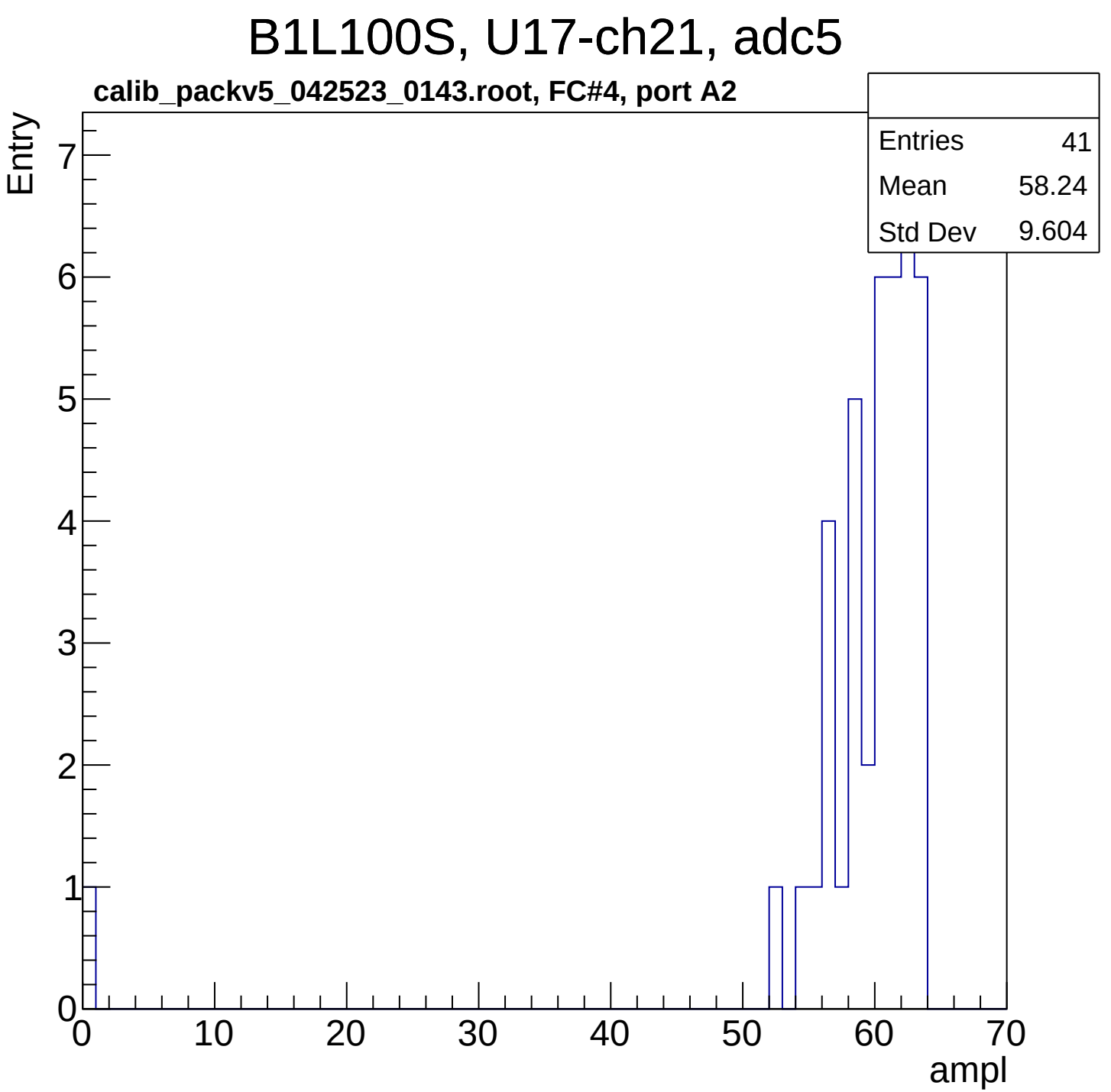
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch21, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 41
Mean 58.24
Std Dev 9.604
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
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40
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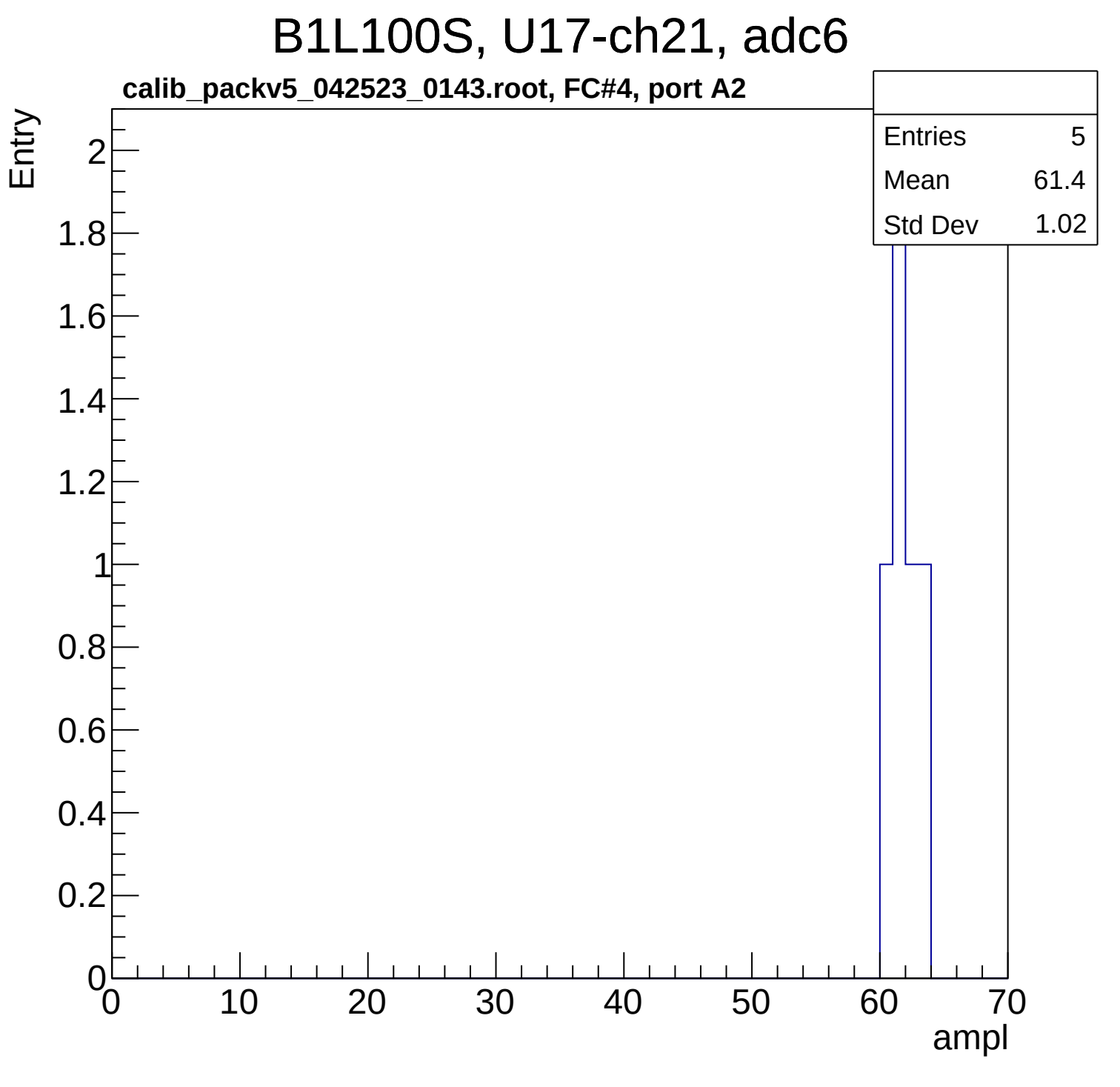
60
70


B1L100S, U17-ch21, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 5
Mean 61.4
Std Dev 1.02
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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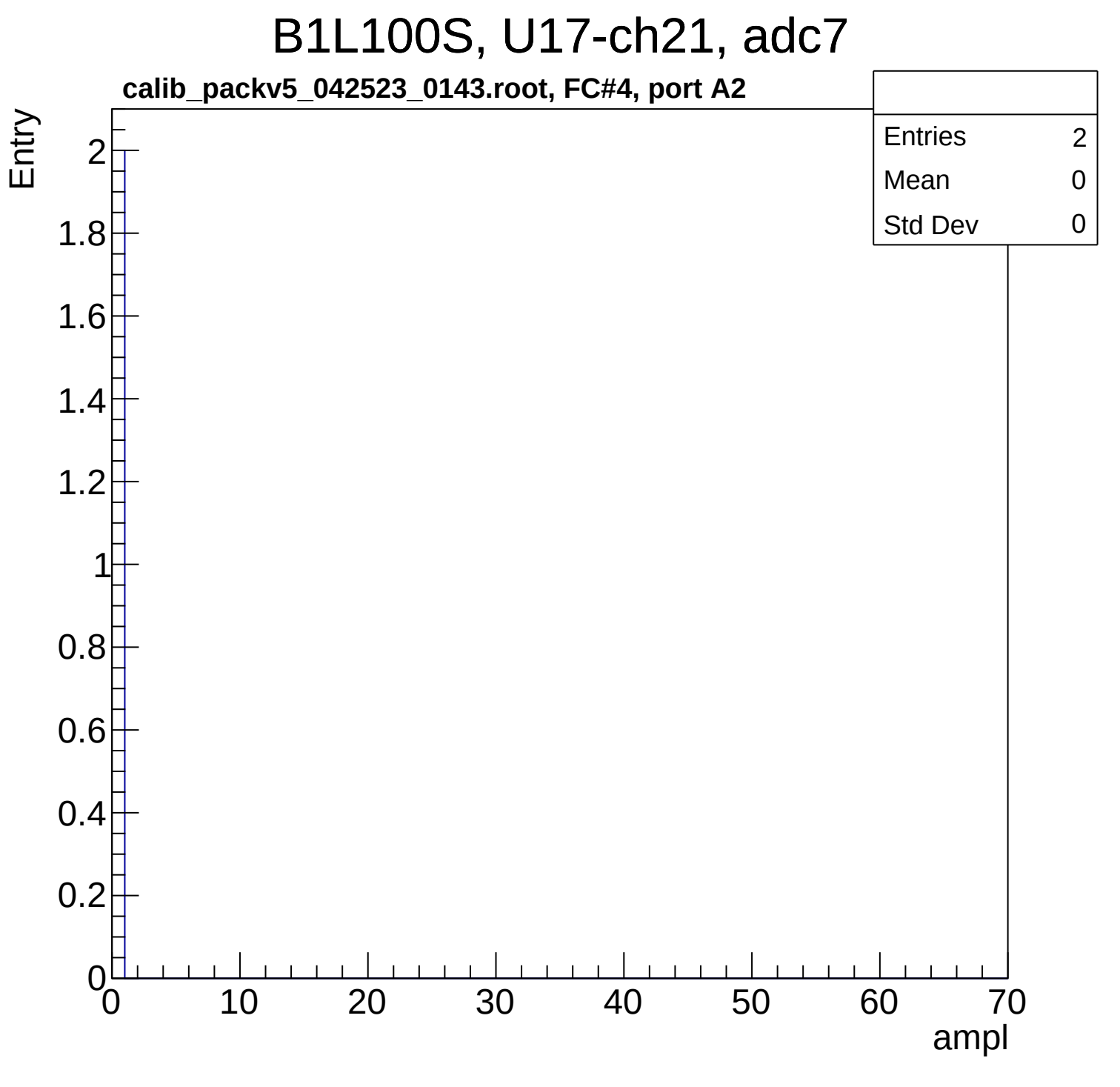
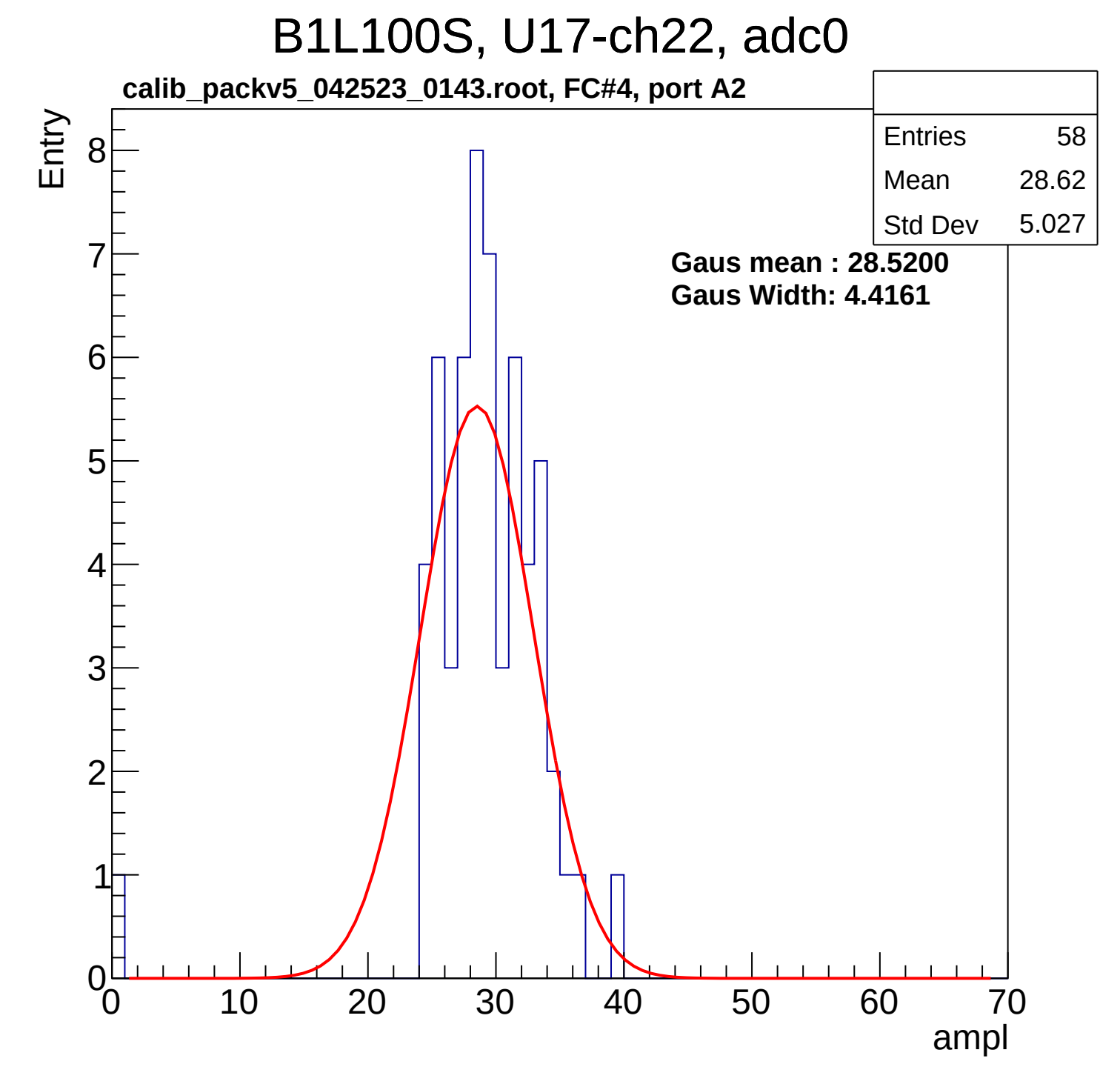
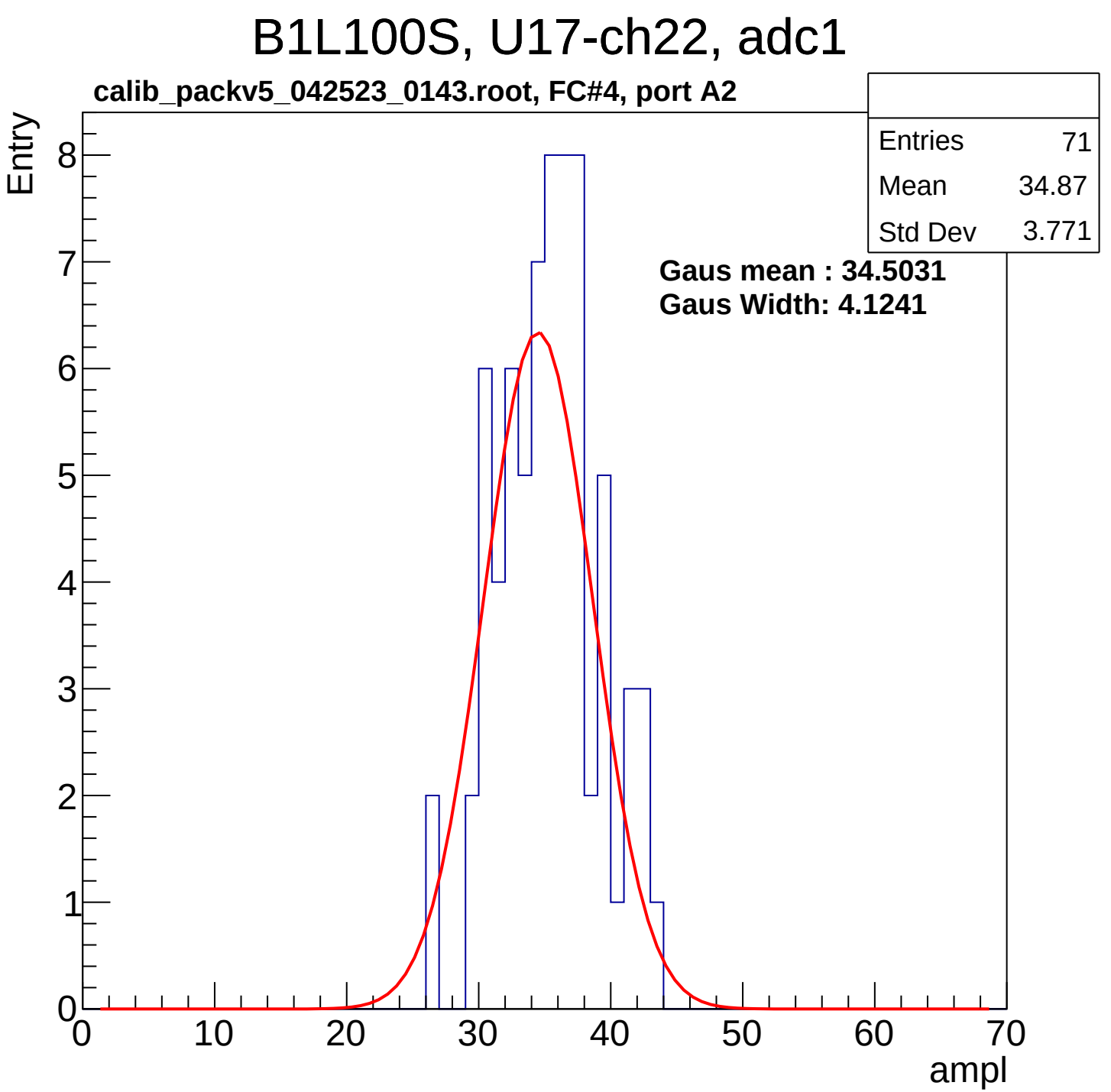
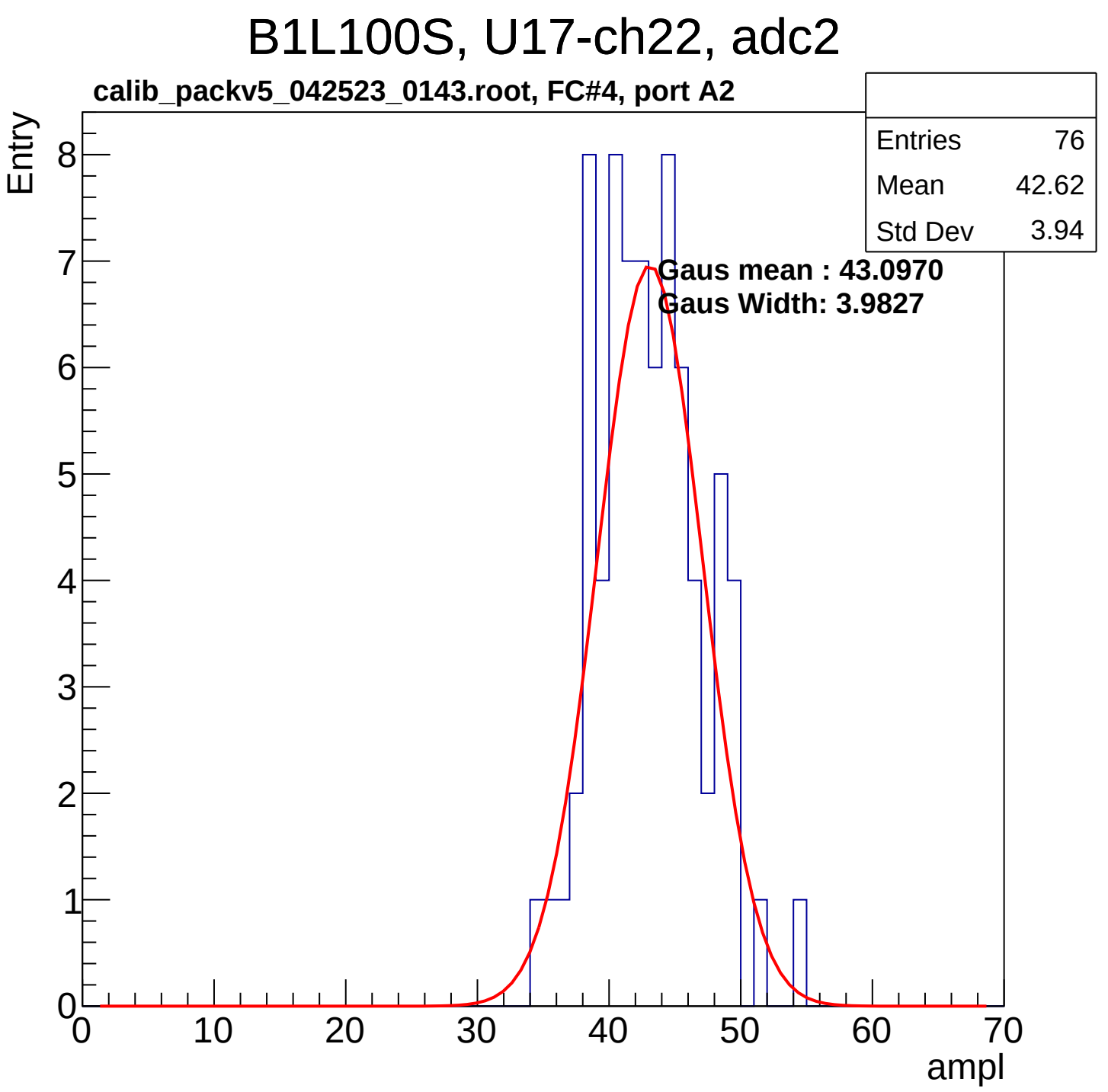
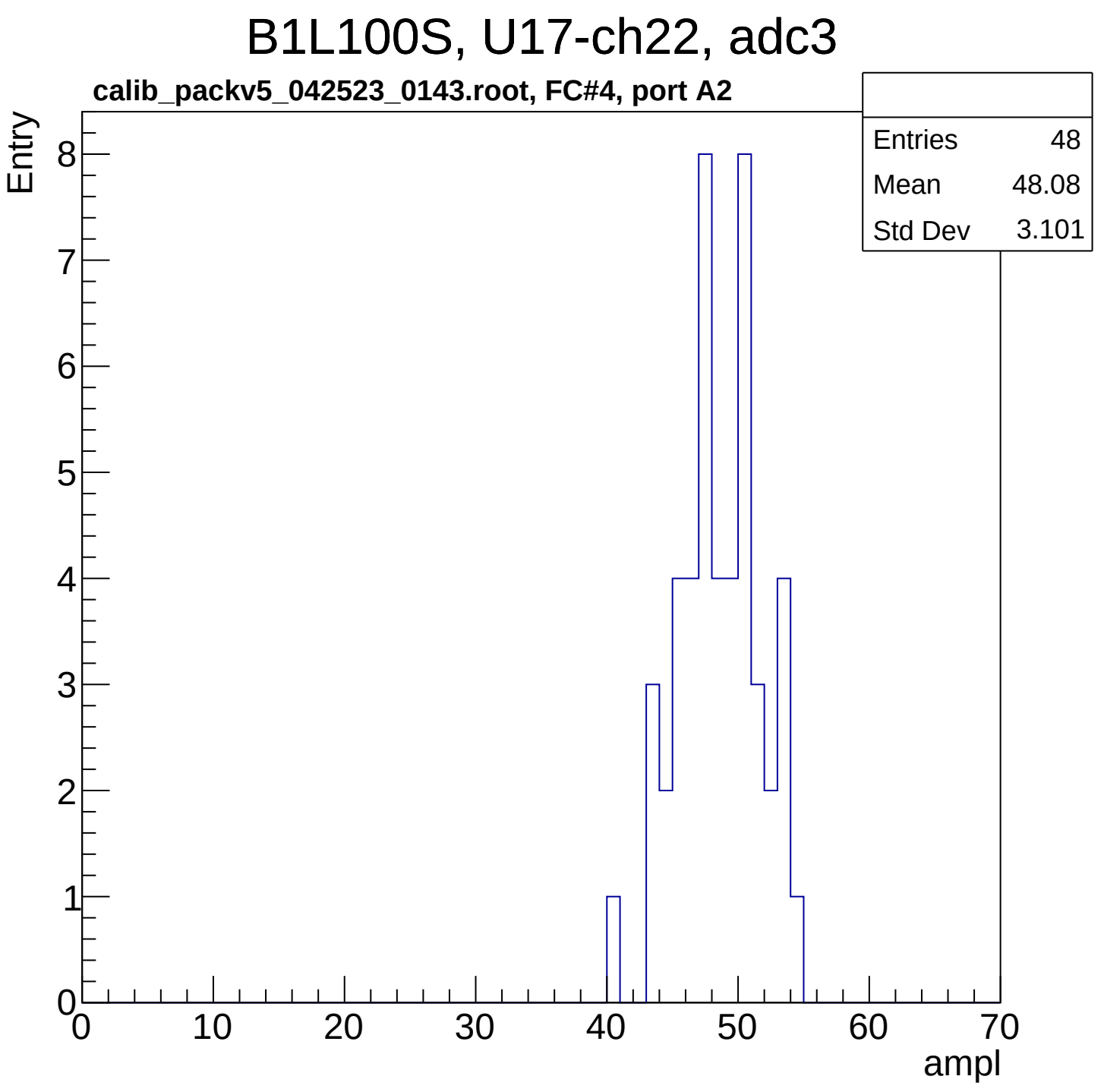
40
50
60
70


B1L100S, U17-ch21, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch22, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 28.62
Std Dev 5.027
Gaus mean : 28.5200
Gaus Width: 4.4161
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch22, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 34.87
Std Dev 3.771
Gaus mean : 34.5031
Gaus Width: 4.1241
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch22, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 76
Mean 42.62
Std Dev 3.94
Gaus mean : 43.0970
Gaus Width: 3.9827
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch22, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 48
Mean 48.08
Std Dev 3.101
Entry
ampl
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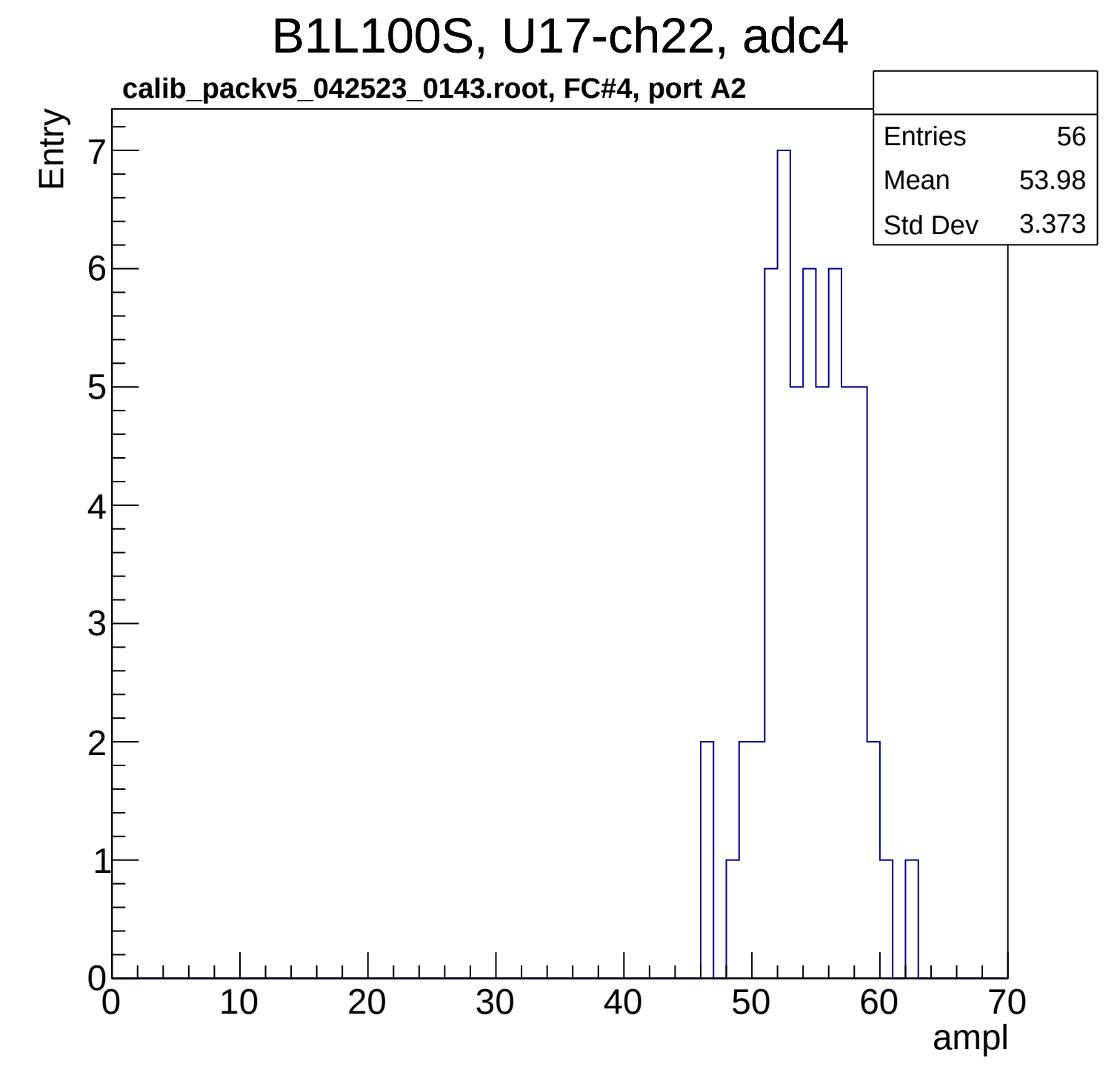
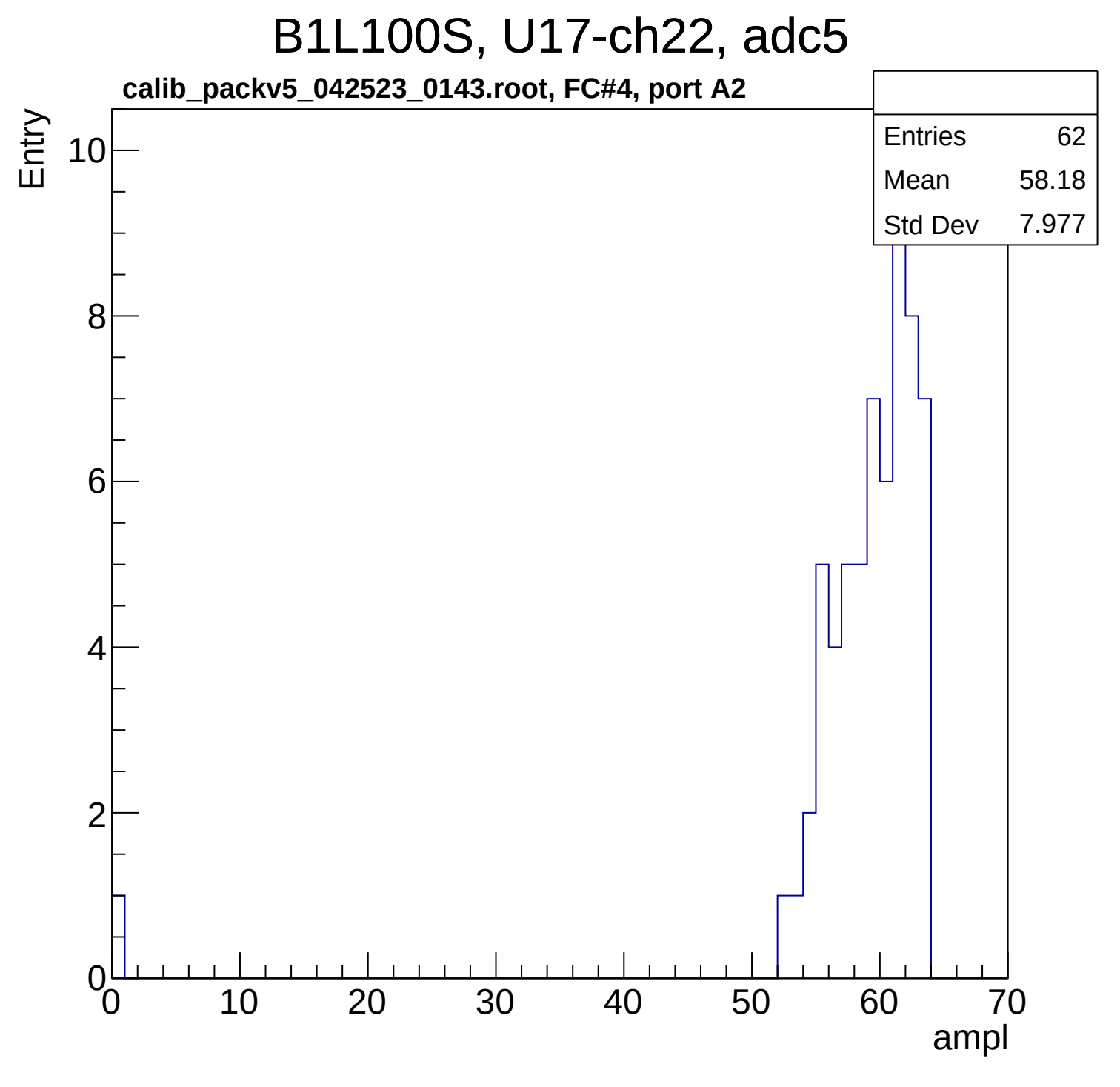
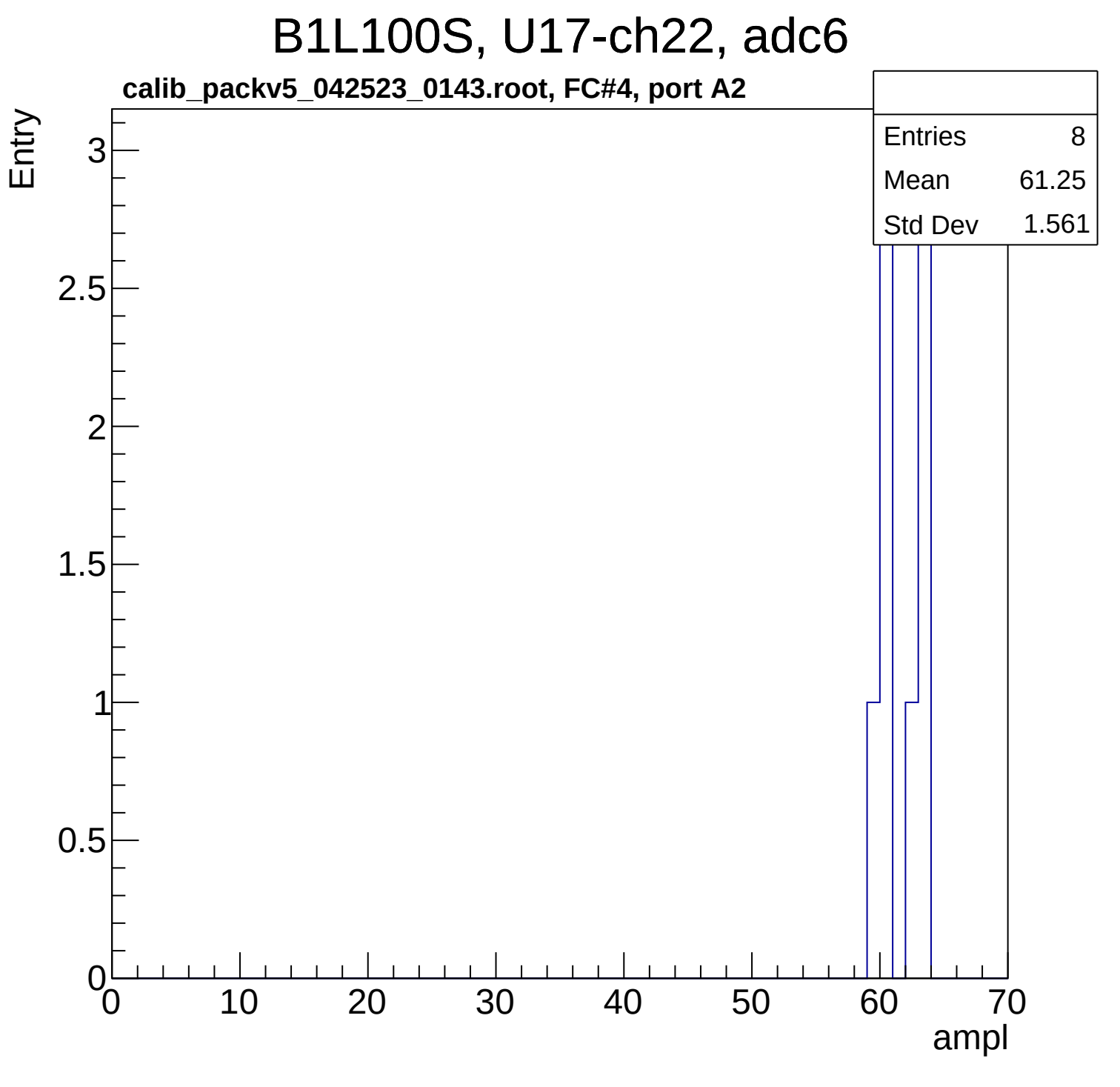
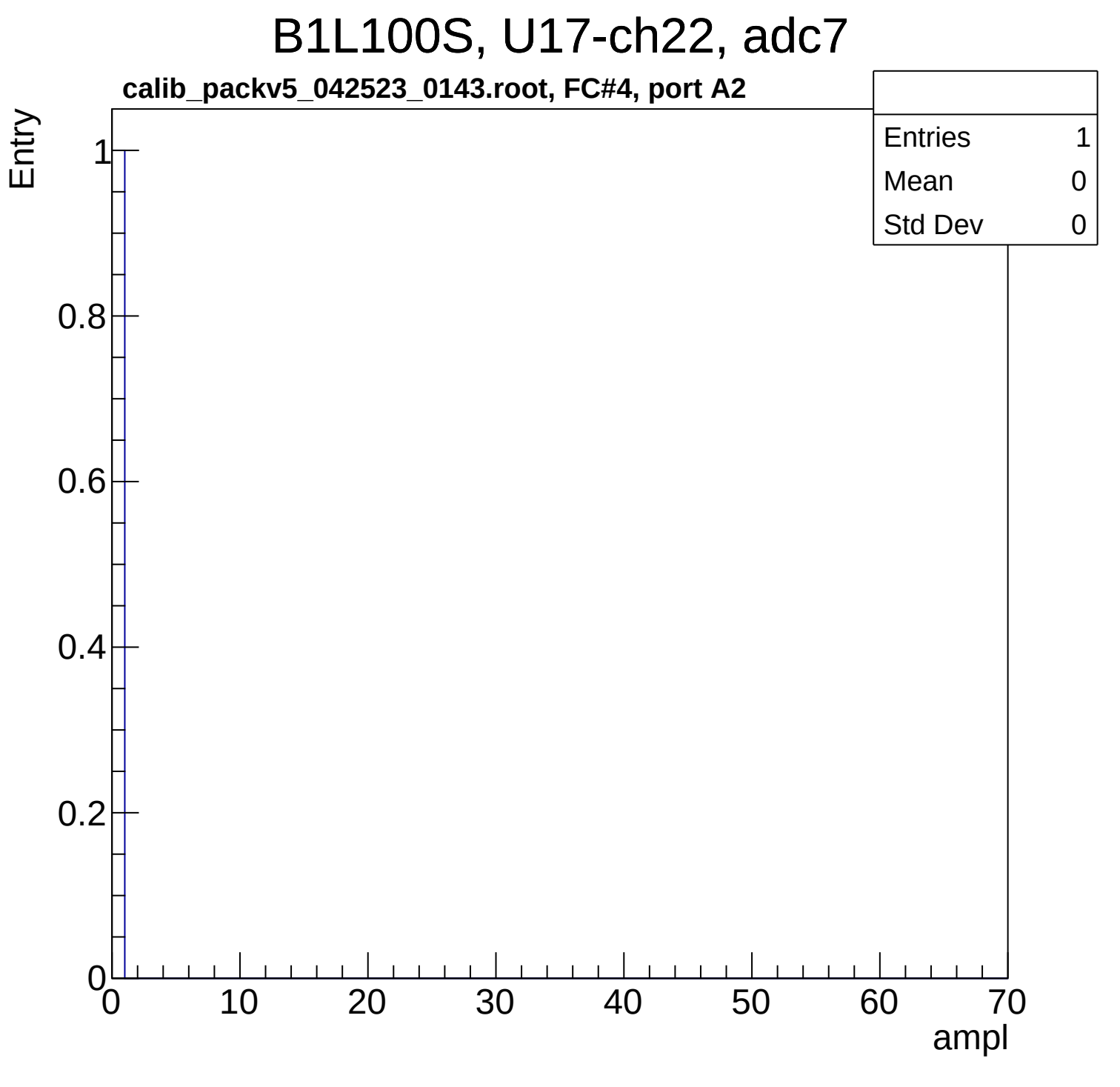
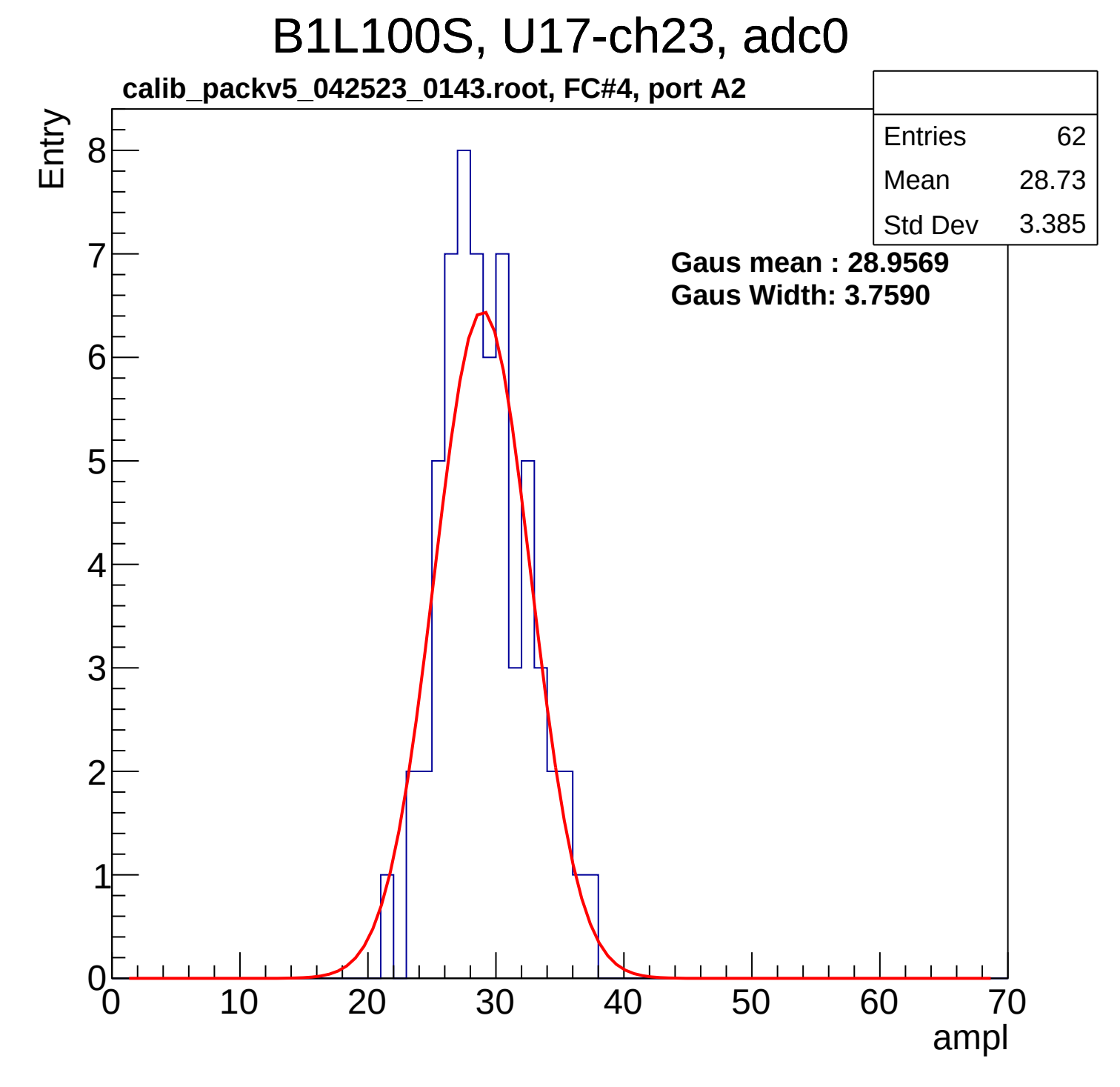
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch22, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 53.98
Std Dev 3.373
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U17-ch22, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 58.18
Std Dev 7.977
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch22, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 8
Mean 61.25
Std Dev 1.561
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L100S, U17-ch22, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch23, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 28.73
Std Dev 3.385
Gaus mean : 28.9569
Gaus Width: 3.7590
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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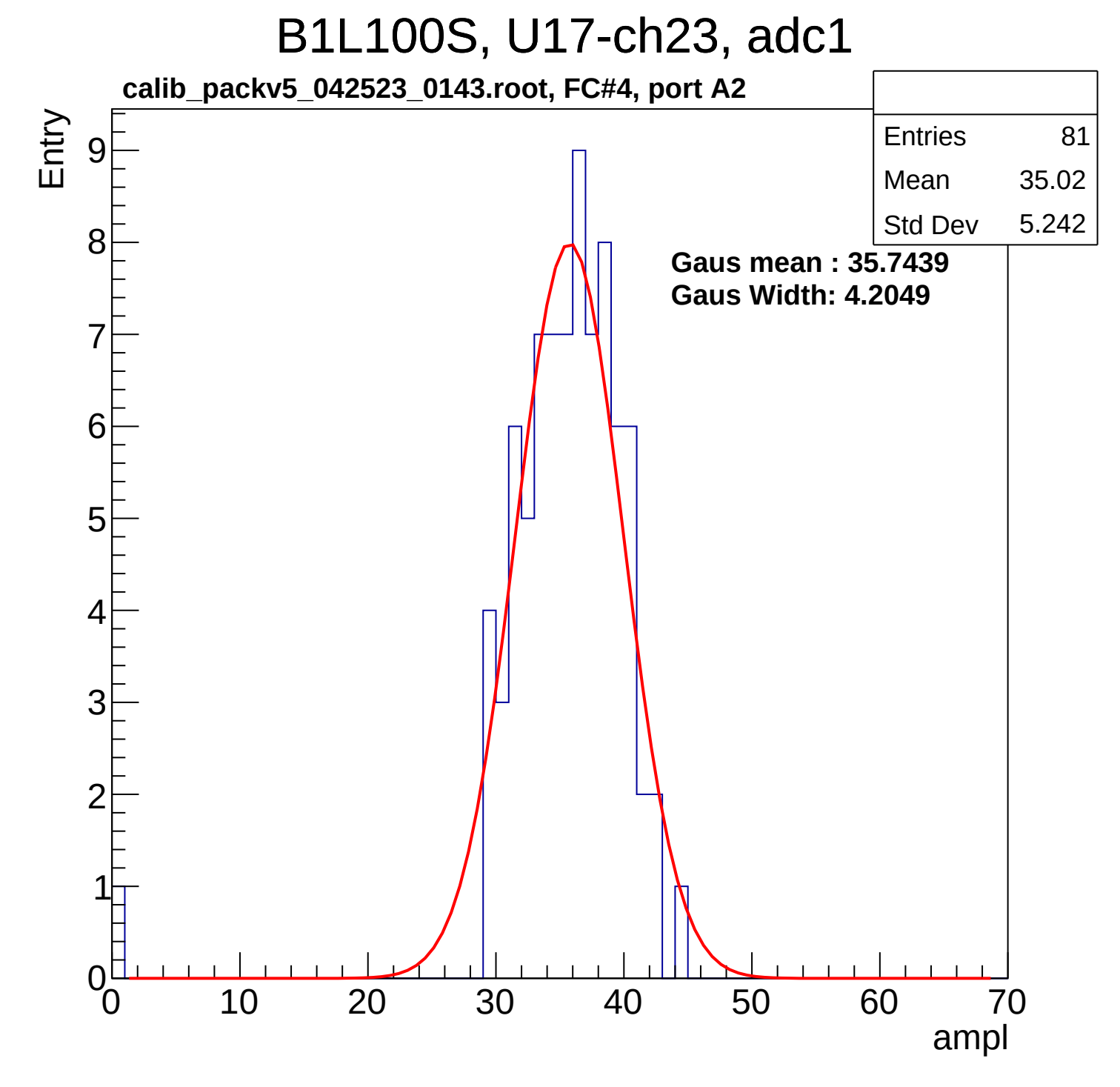
40
50
60
70


B1L100S, U17-ch23, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 81
Mean 35.02
Std Dev 5.242
Gaus mean : 35.7439
Gaus Width: 4.2049
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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20
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40
50
60
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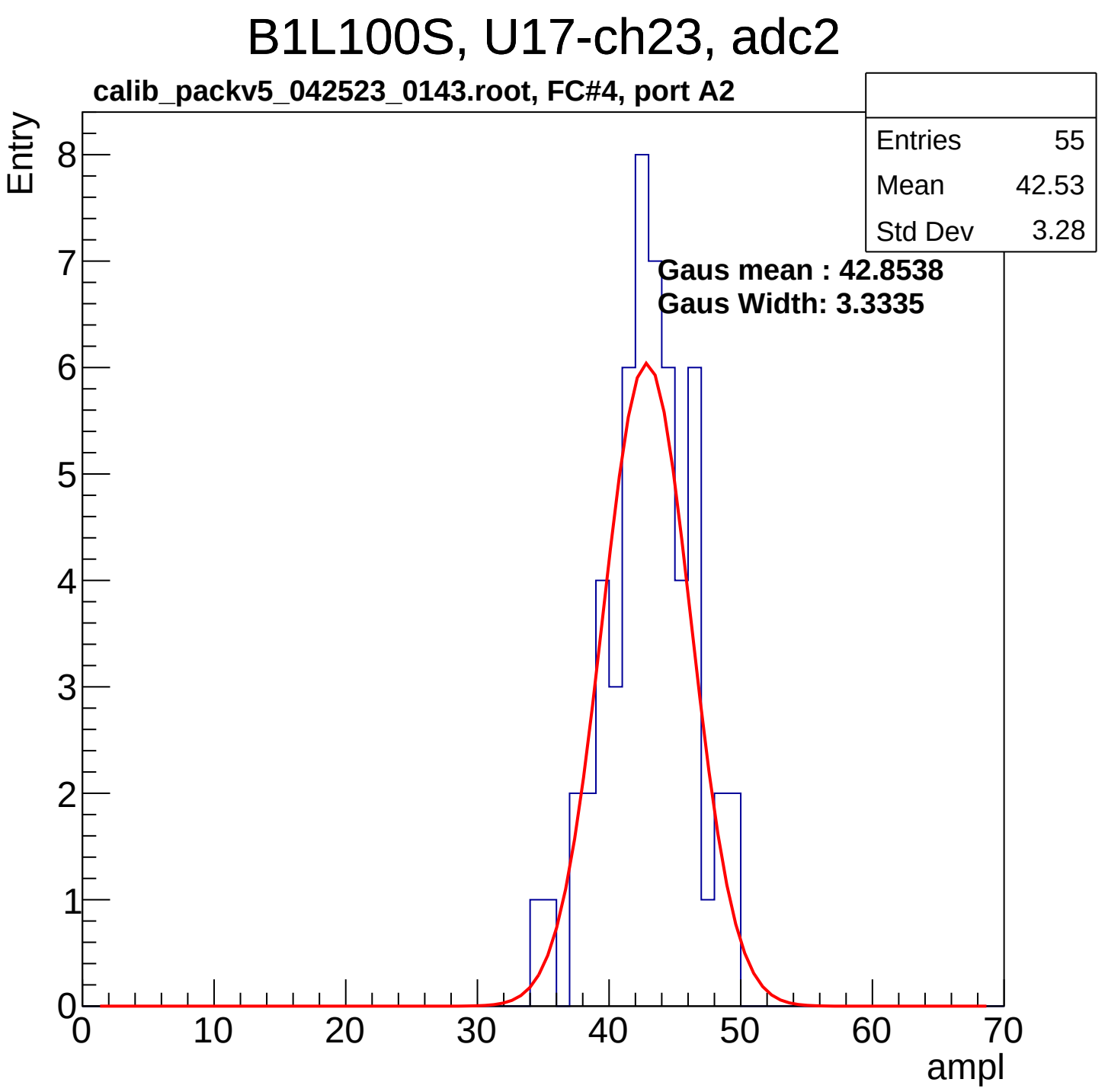
B1L100S, U17-ch23, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 42.53
Std Dev 3.28
Gaus mean : 42.8538
Gaus Width: 3.3335
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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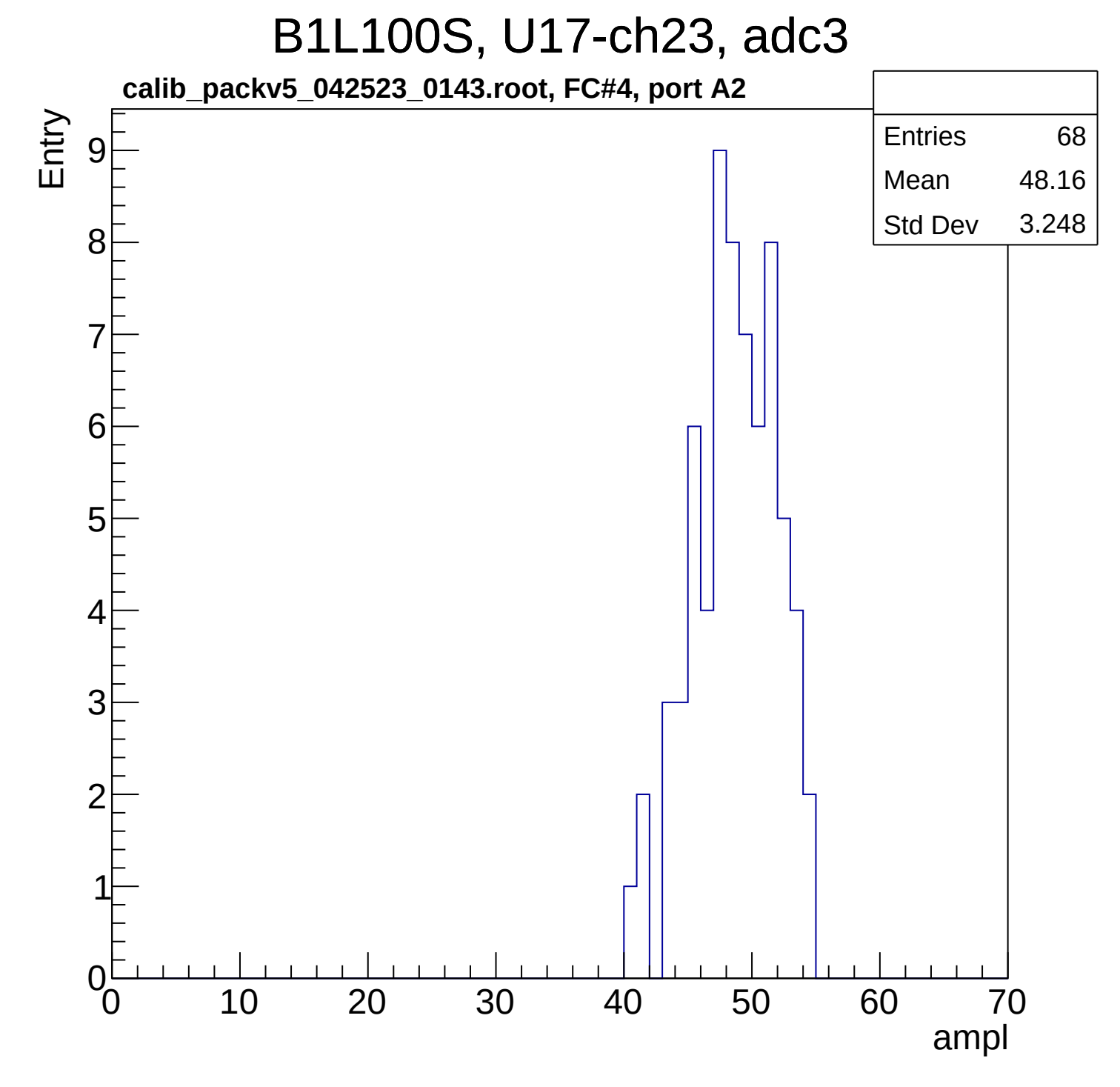
B1L100S, U17-ch23, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 48.16
Std Dev 3.248
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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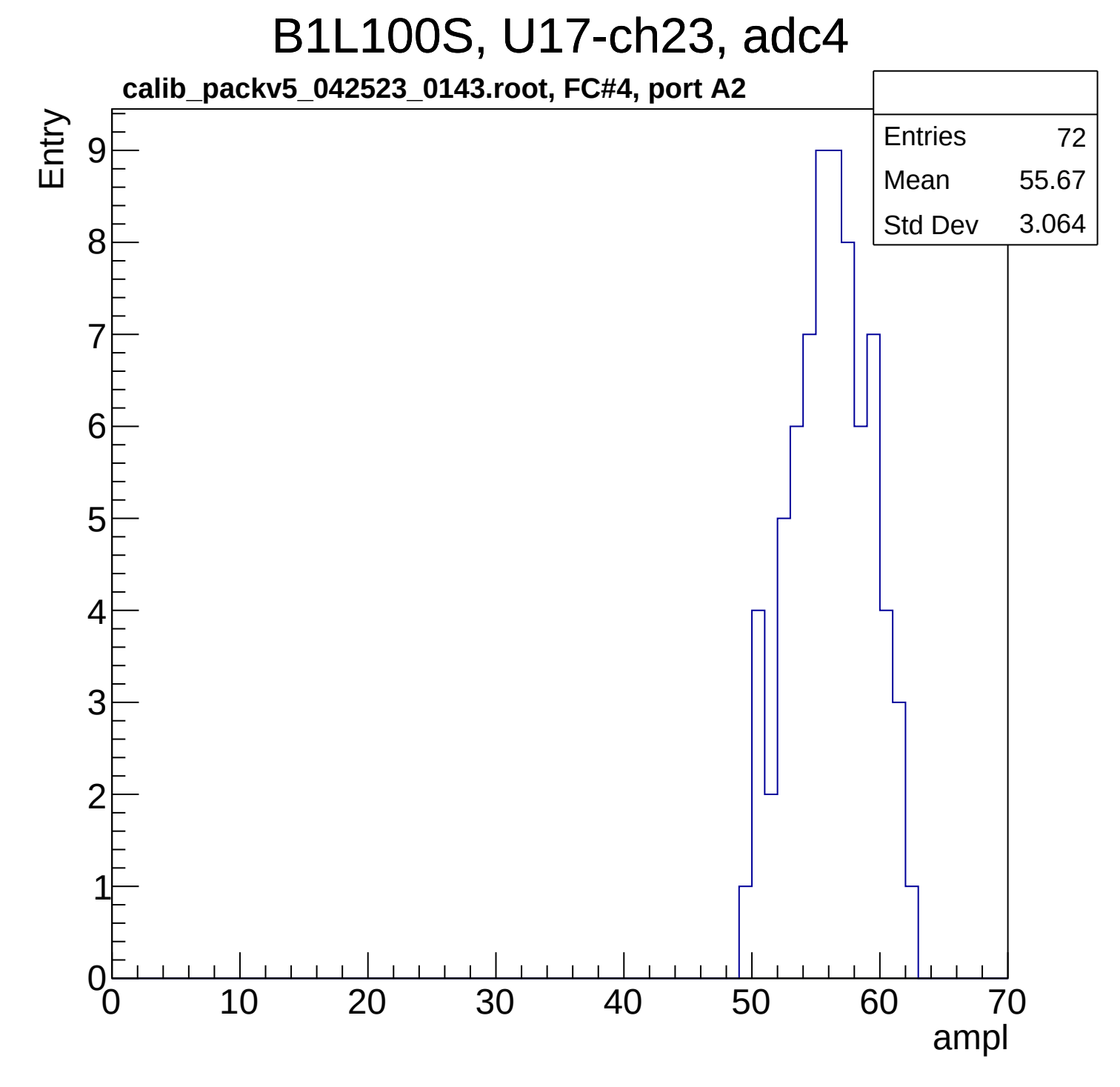
B1L100S, U17-ch23, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 55.67
Std Dev 3.064
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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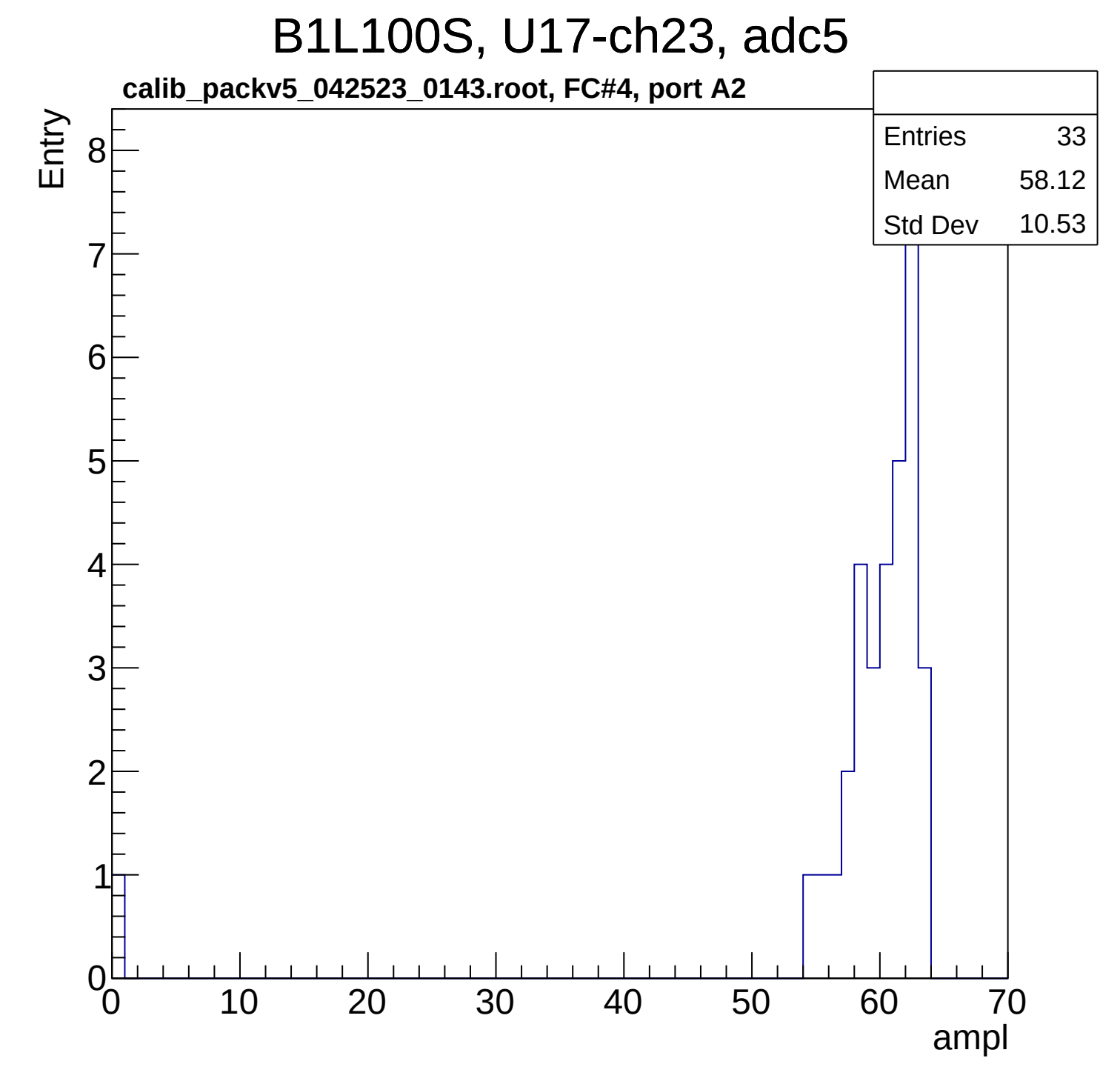
B1L100S, U17-ch23, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 33
Mean 58.12
Std Dev 10.53
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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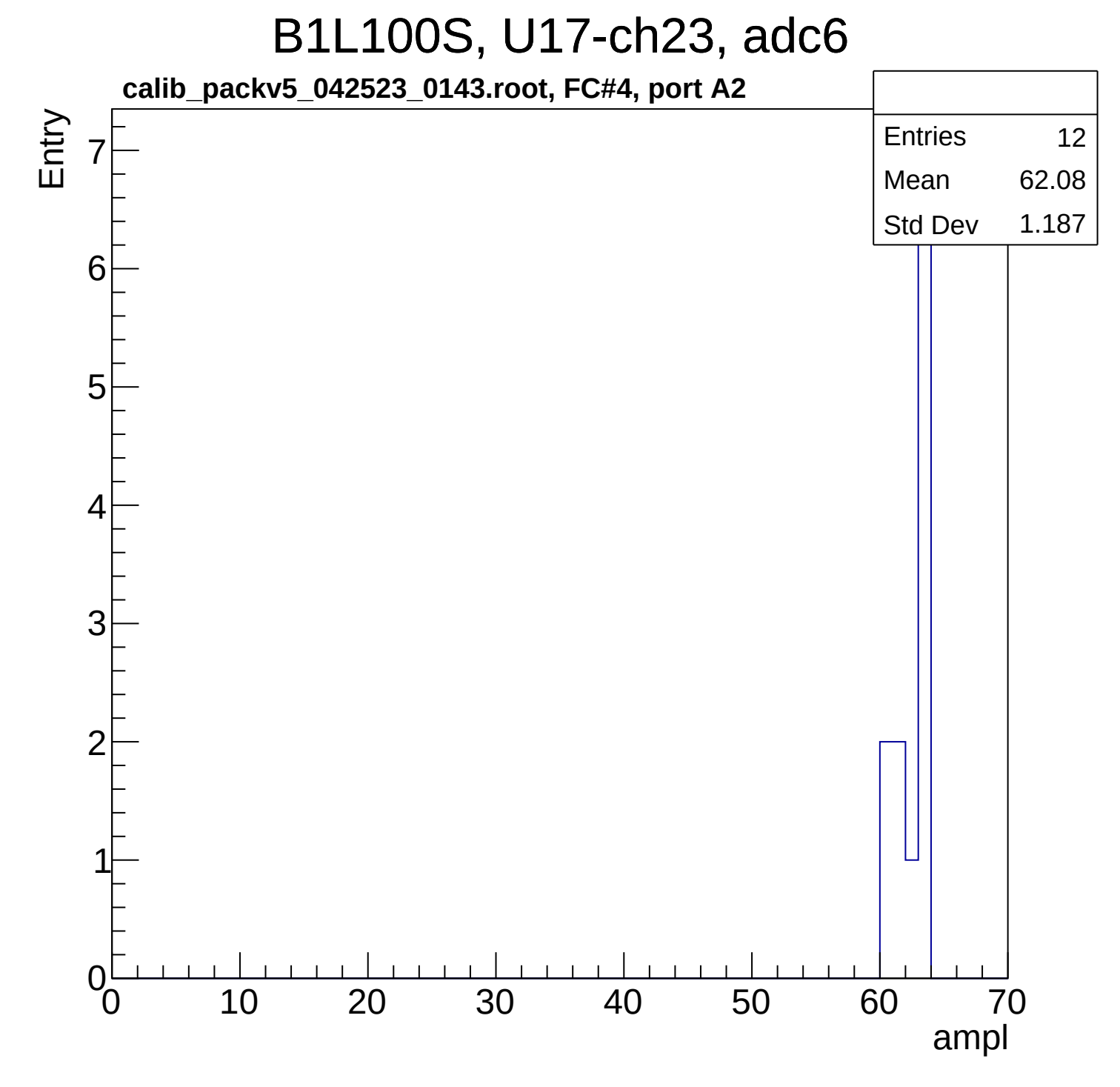
B1L100S, U17-ch23, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 12
Mean 62.08
Std Dev 1.187
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
50
60
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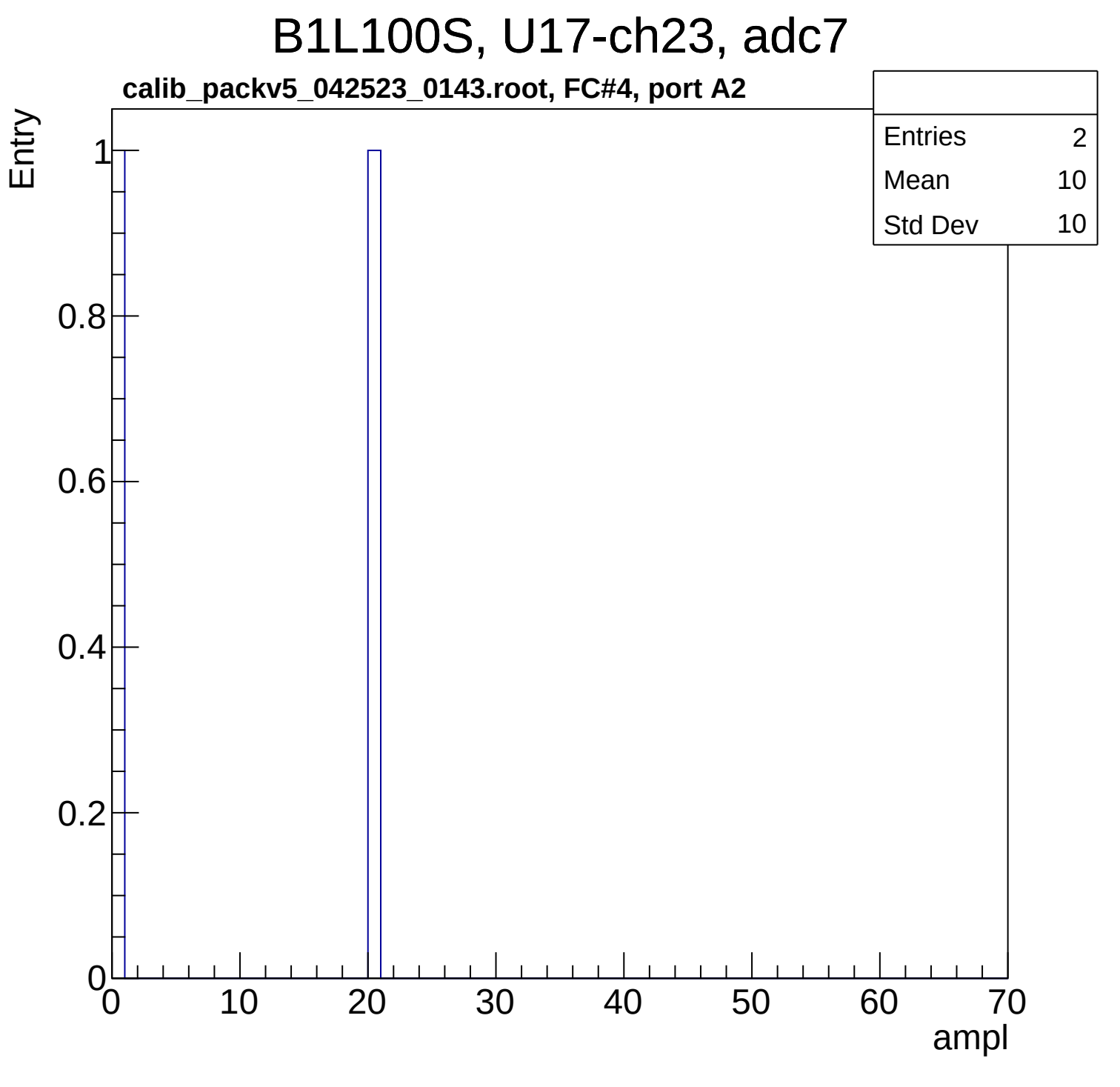
B1L100S, U17-ch23, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 10
Std Dev 10
Entry
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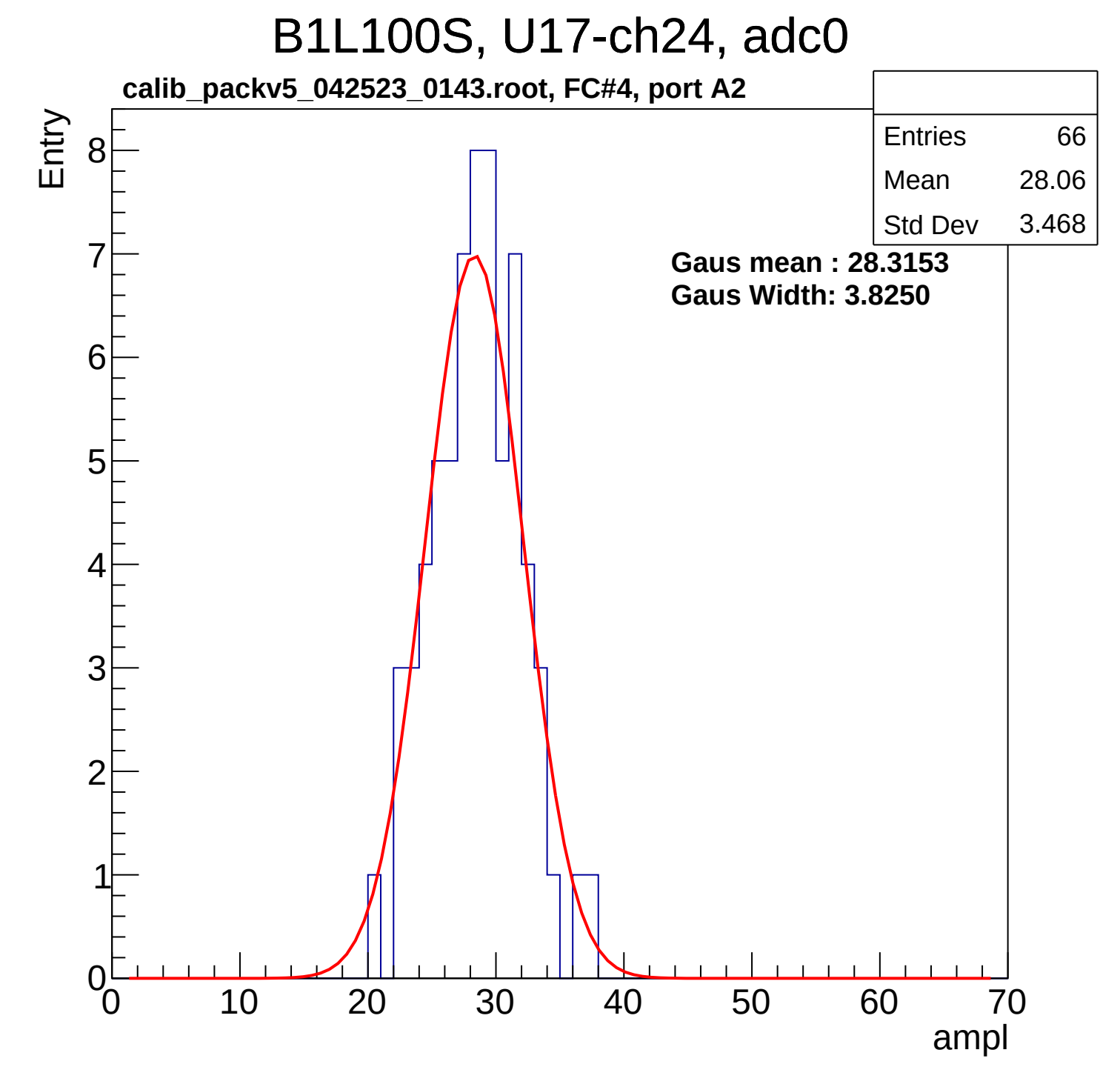
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch24, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 28.06
Std Dev 3.468
Gaus mean : 28.3153
Gaus Width: 3.8250
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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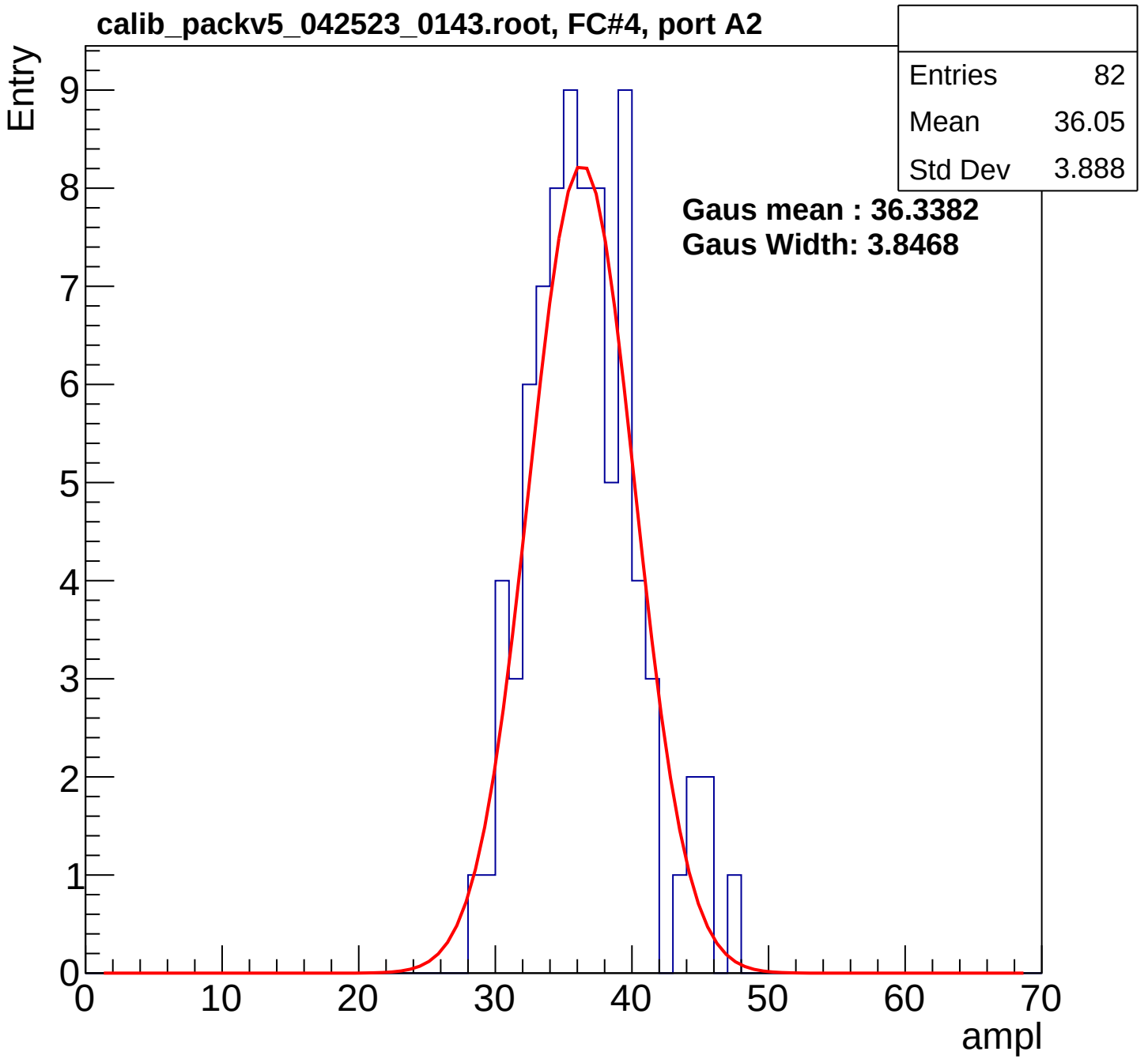
B1L100S, U17-ch24, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 82
Mean 36.05
Std Dev 3.888
Gaus mean : 36.3382
Gaus Width: 3.8468
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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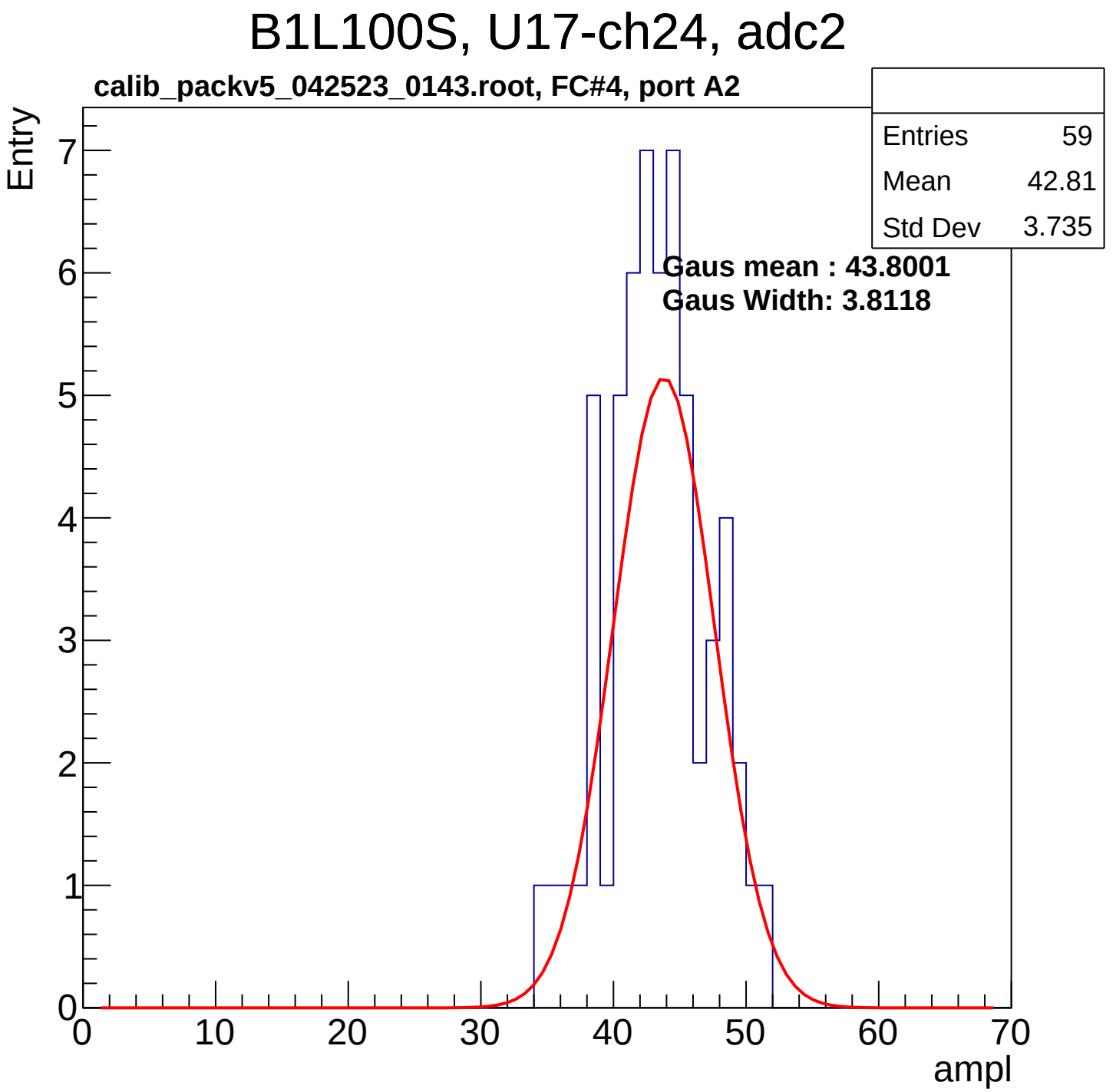
B1L100S, U17-ch24, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 42.81
Std Dev 3.735
Gaus mean : 43.8001
Gaus Width: 3.8118
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
50
60
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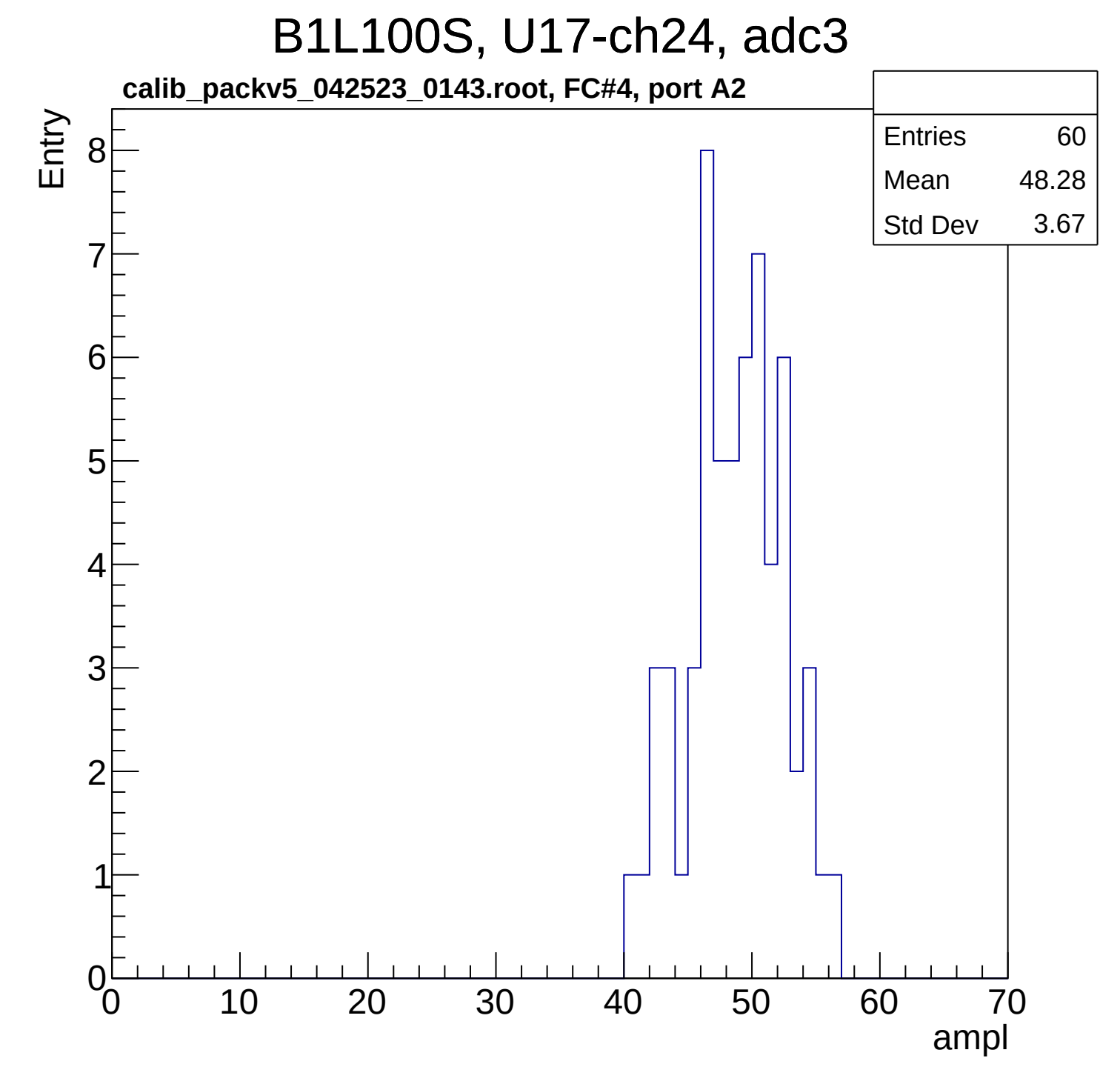
B1L100S, U17-ch24, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 48.28
Std Dev 3.67
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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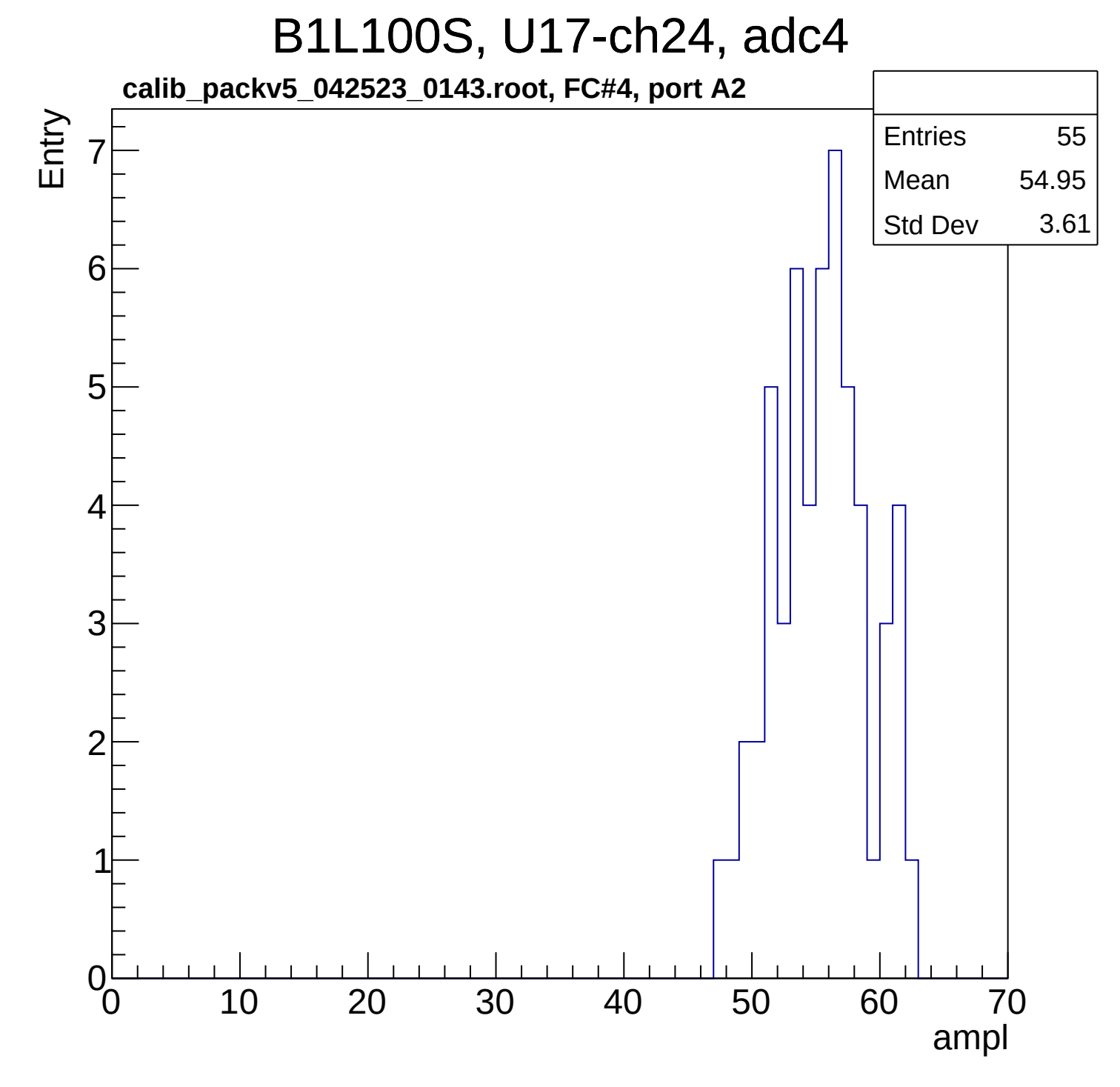
B1L100S, U17-ch24, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 54.95
Std Dev 3.61
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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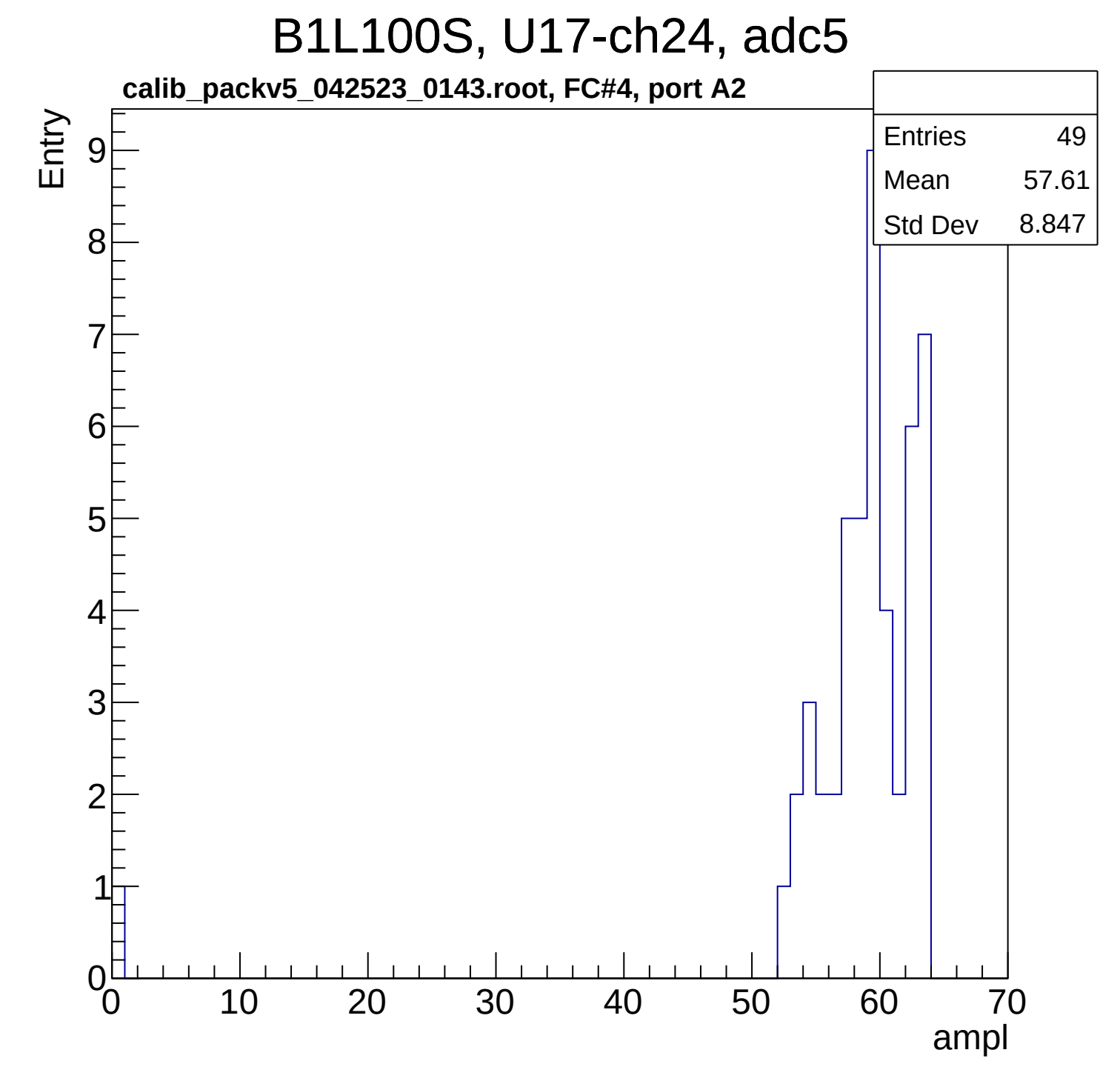
B1L100S, U17-ch24, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 49
Mean 57.61
Std Dev 8.847
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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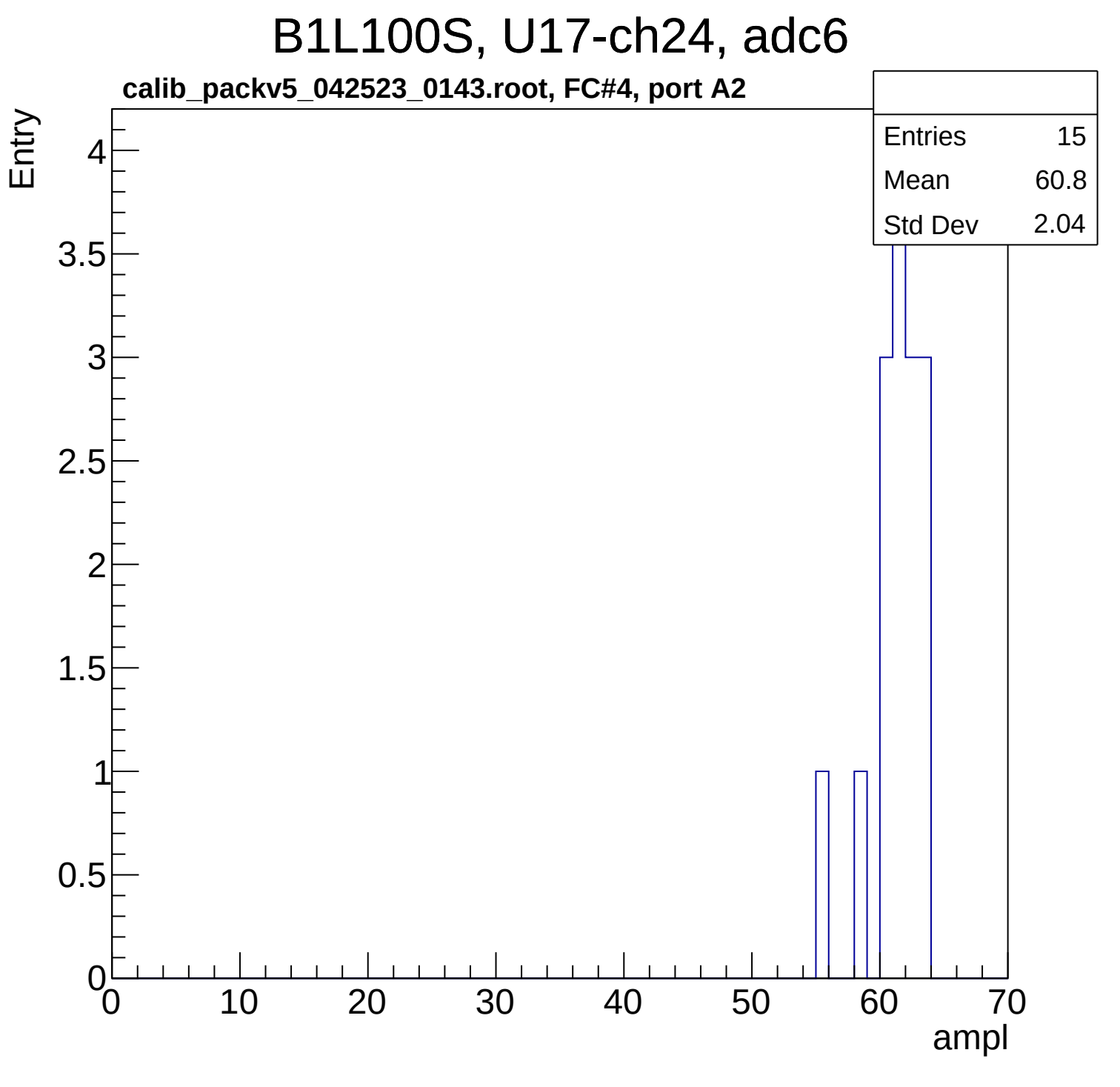
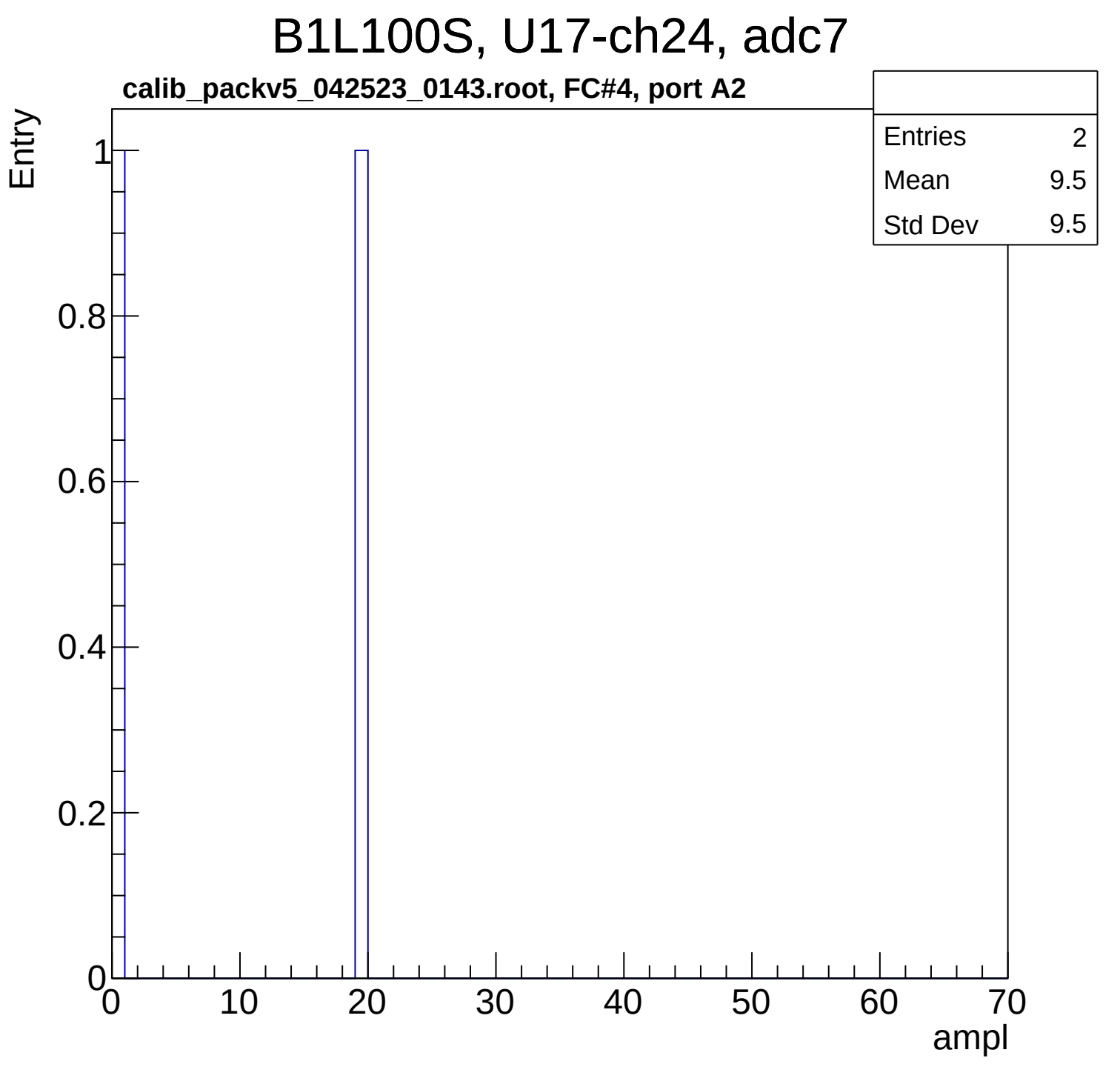
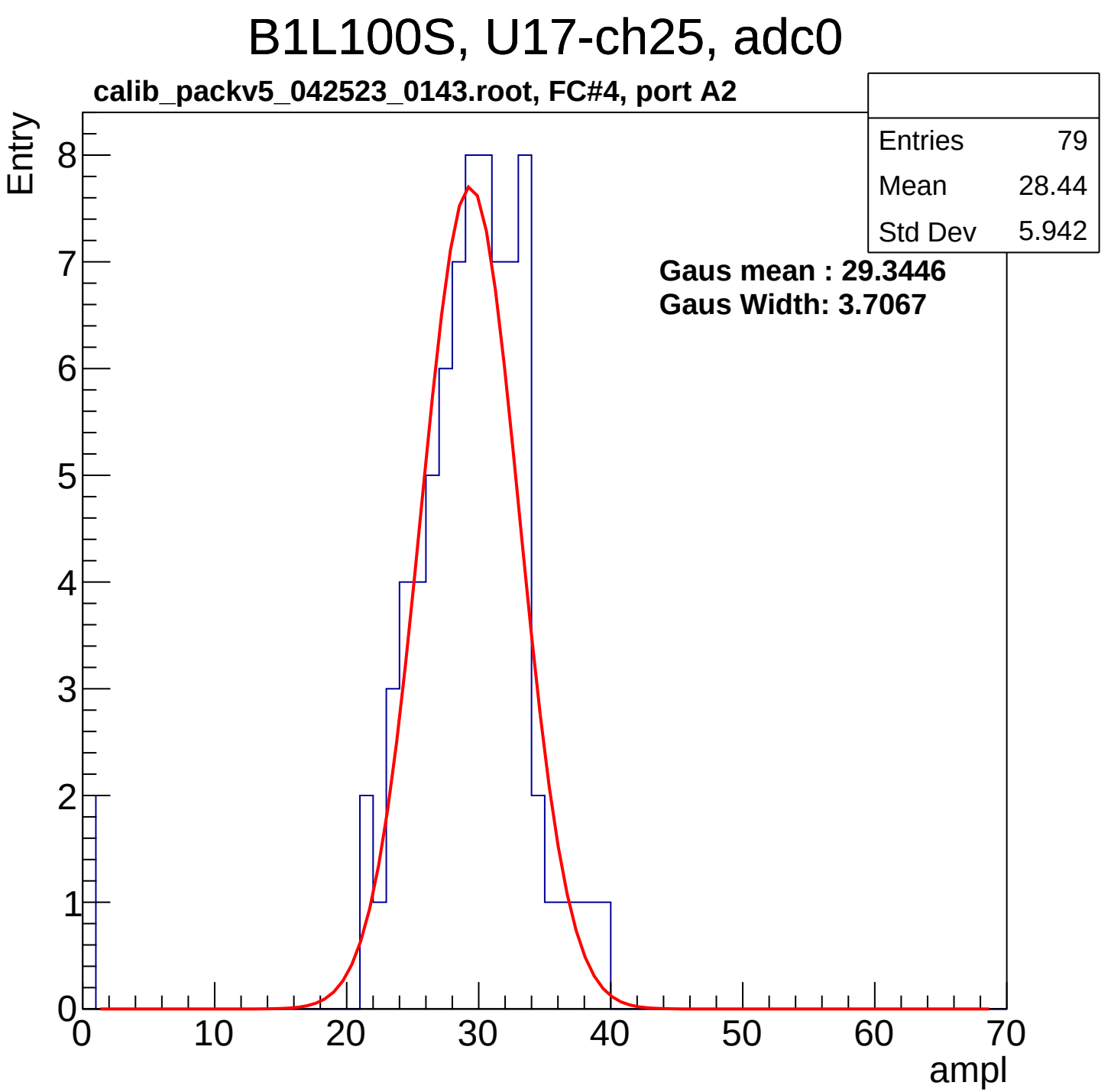
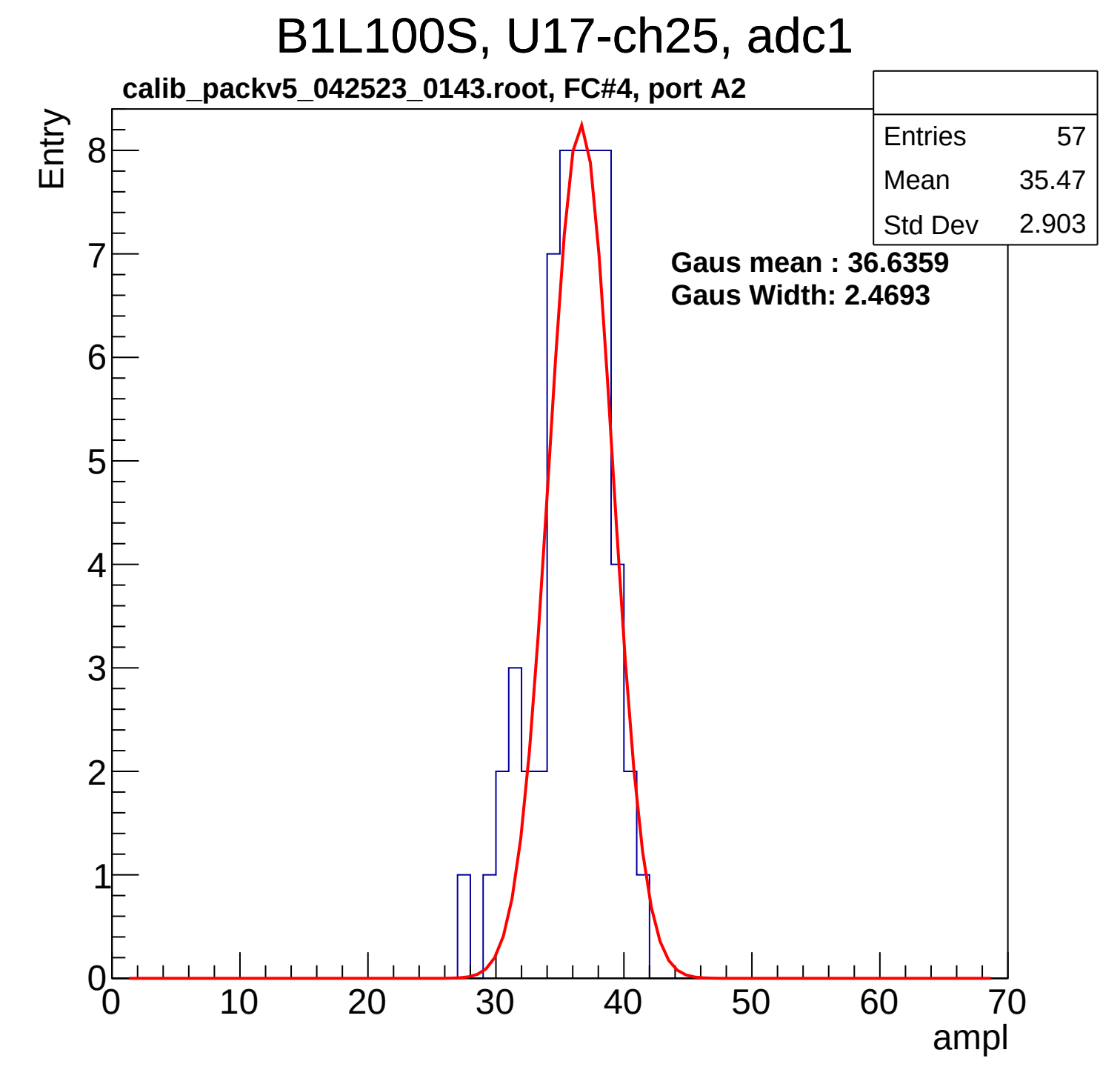
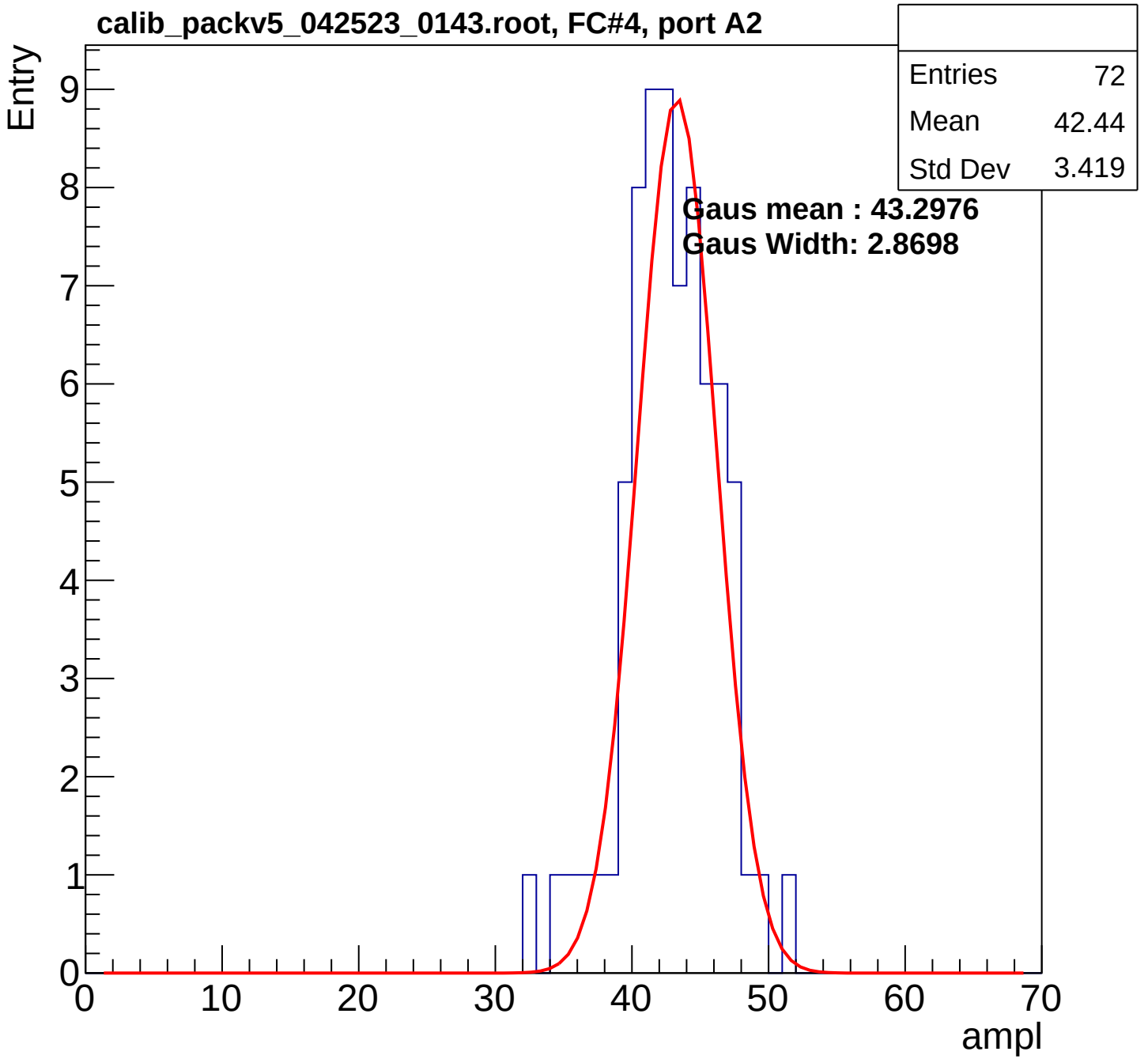

B1L100S, U17-ch24, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 15
Mean 60.8
Std Dev 2.04
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L100S, U17-ch24, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 9.5
Std Dev 9.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch25, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 79
Mean 28.44
Std Dev 5.942
Gaus mean : 29.3446
Gaus Width: 3.7067
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch25, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 35.47
Std Dev 2.903
Gaus mean : 36.6359
Gaus Width: 2.4693
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch25, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 42.44
Std Dev 3.419
Gaus mean : 43.2976
Gaus Width: 2.8698
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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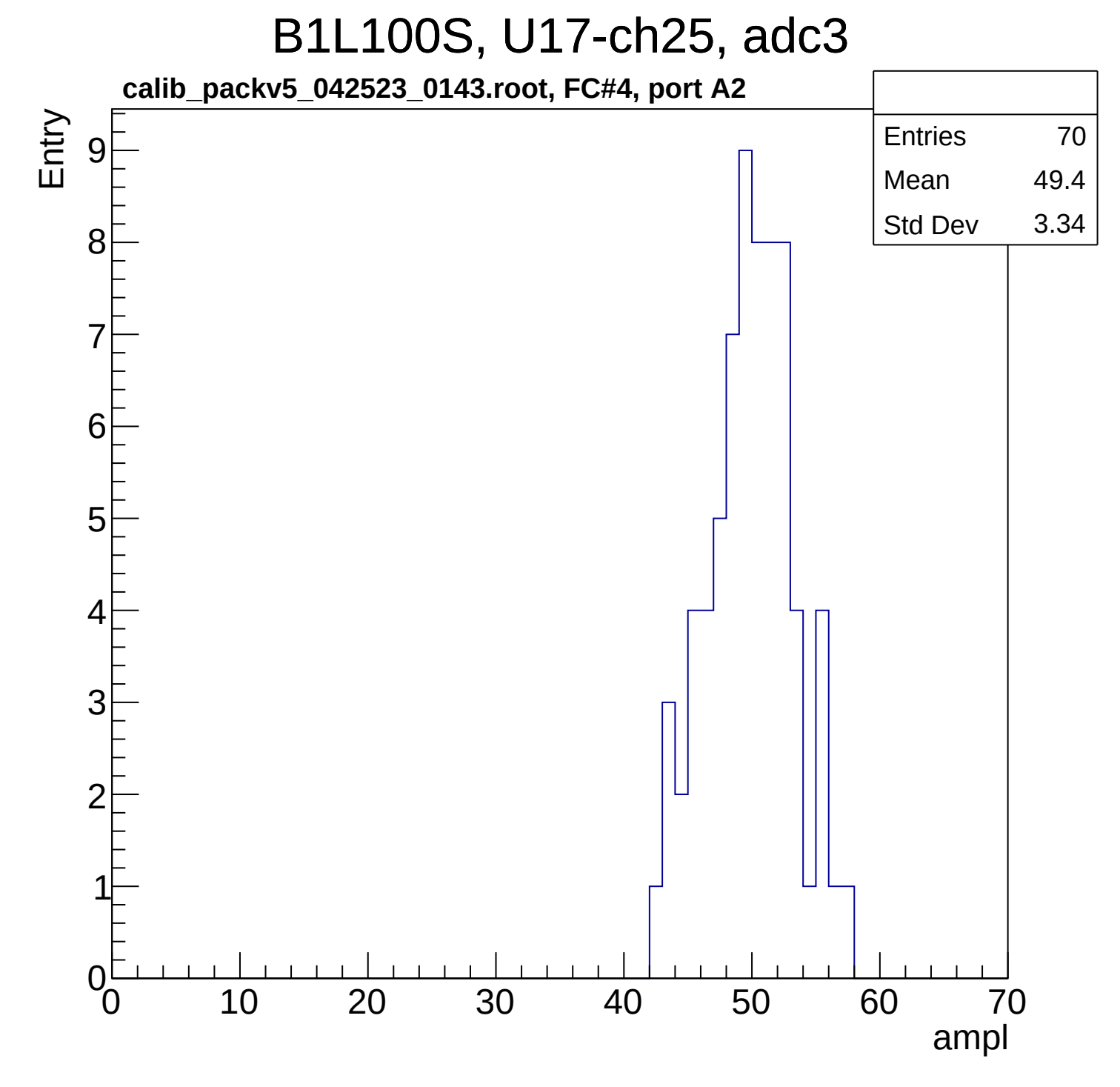
B1L100S, U17-ch25, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 49.4
Std Dev 3.34
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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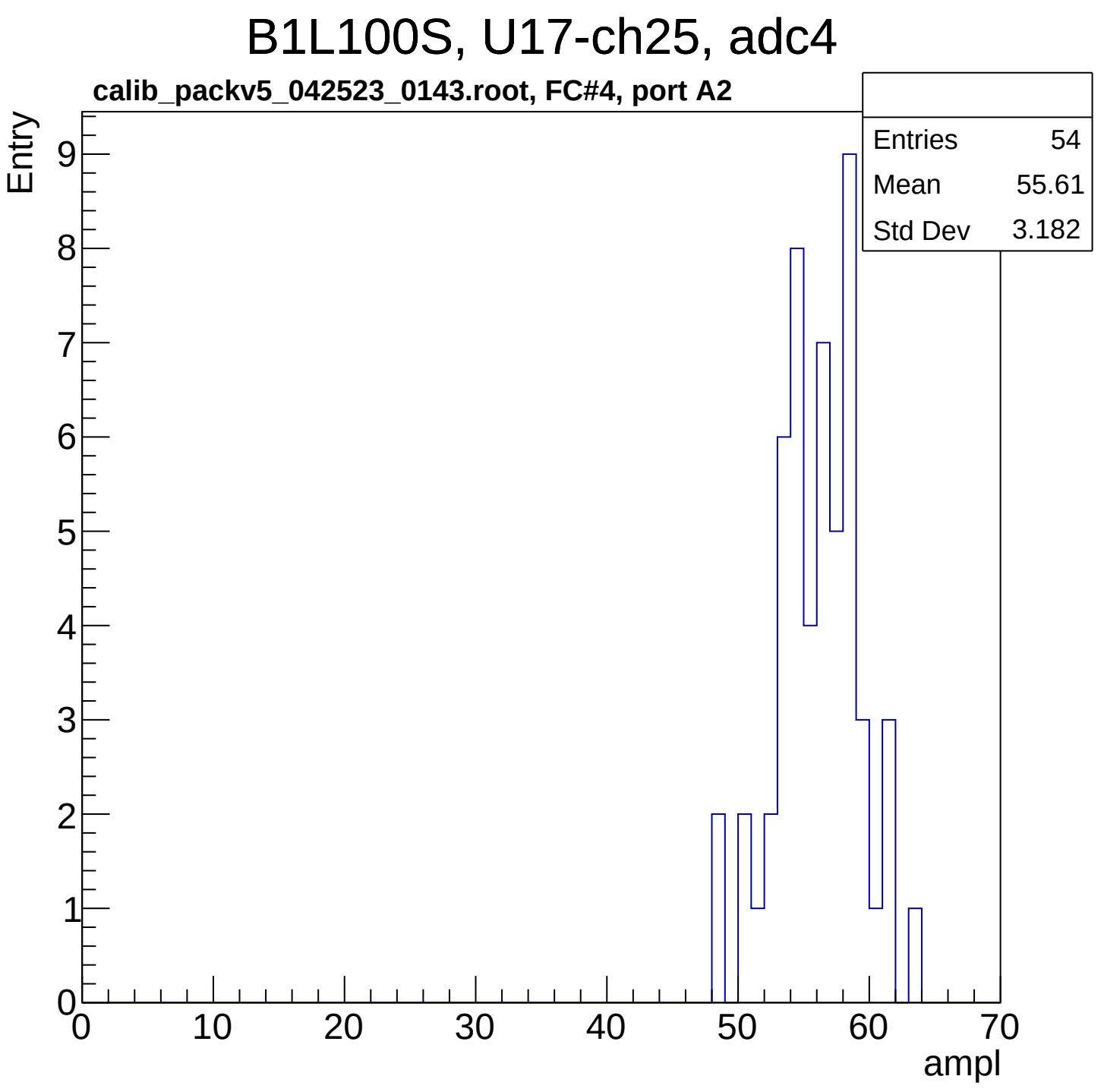
B1L100S, U17-ch25, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 55.61
Std Dev 3.182
Entry
ampl
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3
4
5
6
7
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0
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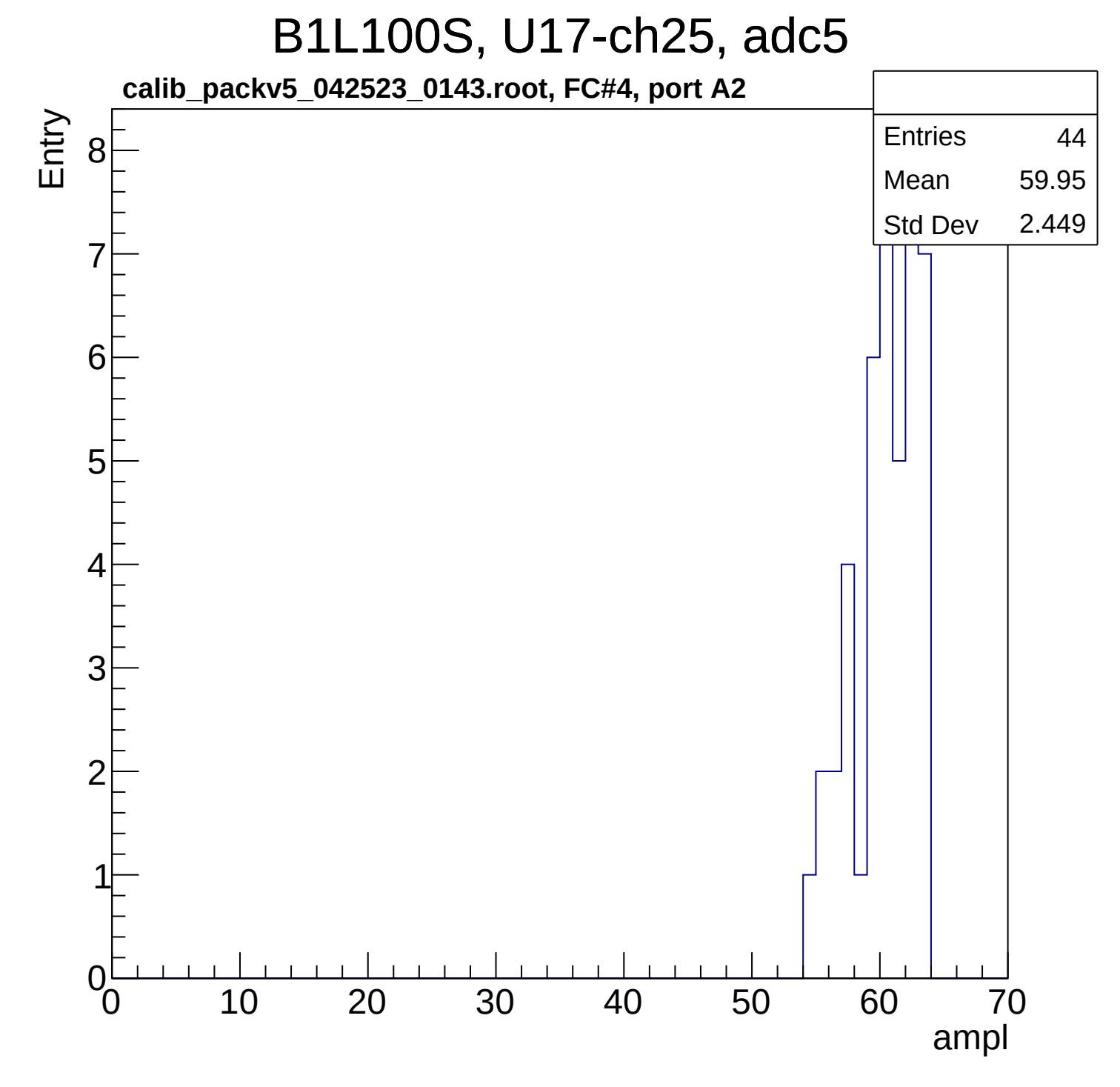
B1L100S, U17-ch25, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 44
Mean 59.95
Std Dev 2.449
Entry
ampl
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1
2
3
4
5
6
7
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0
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60
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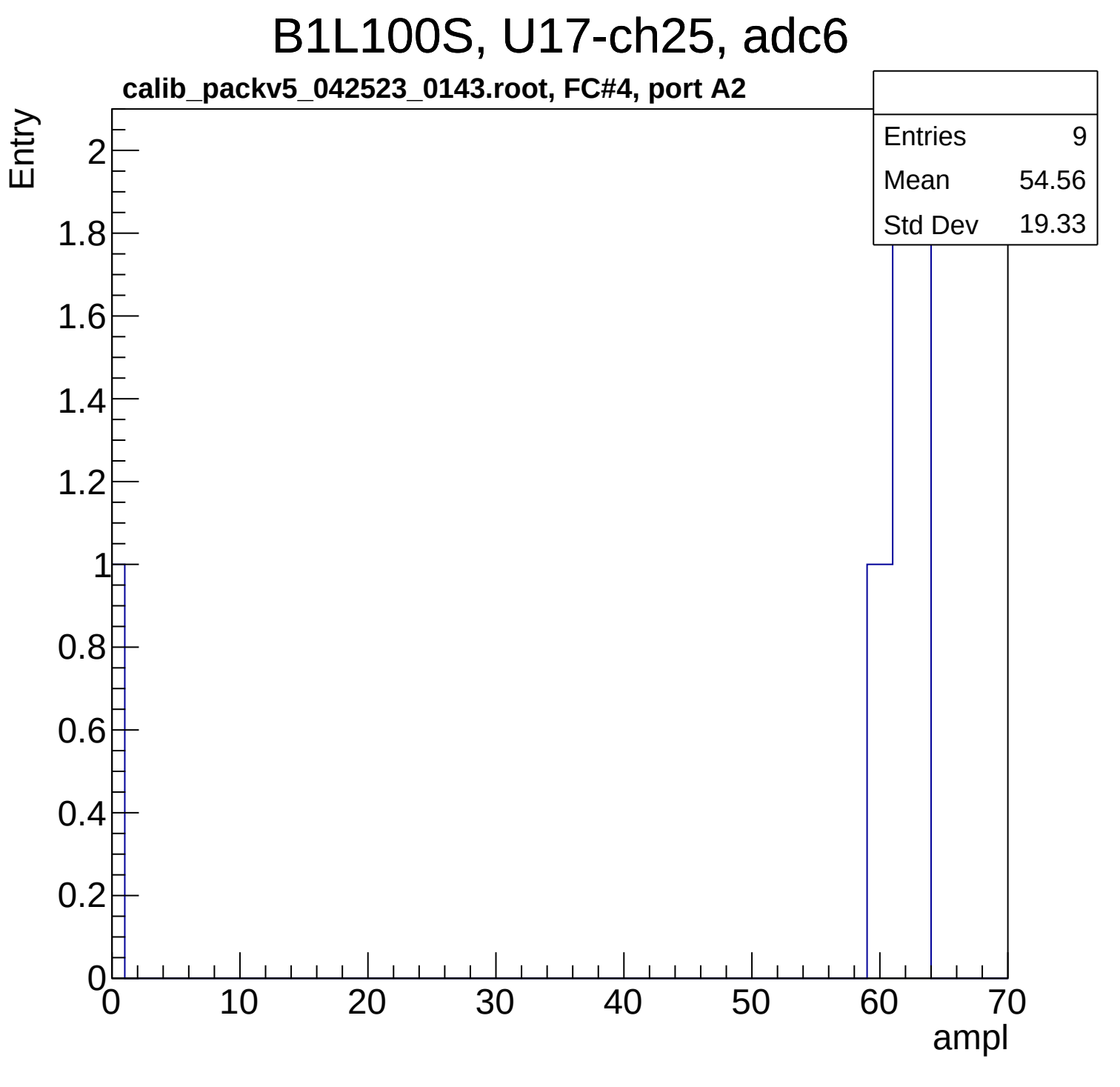
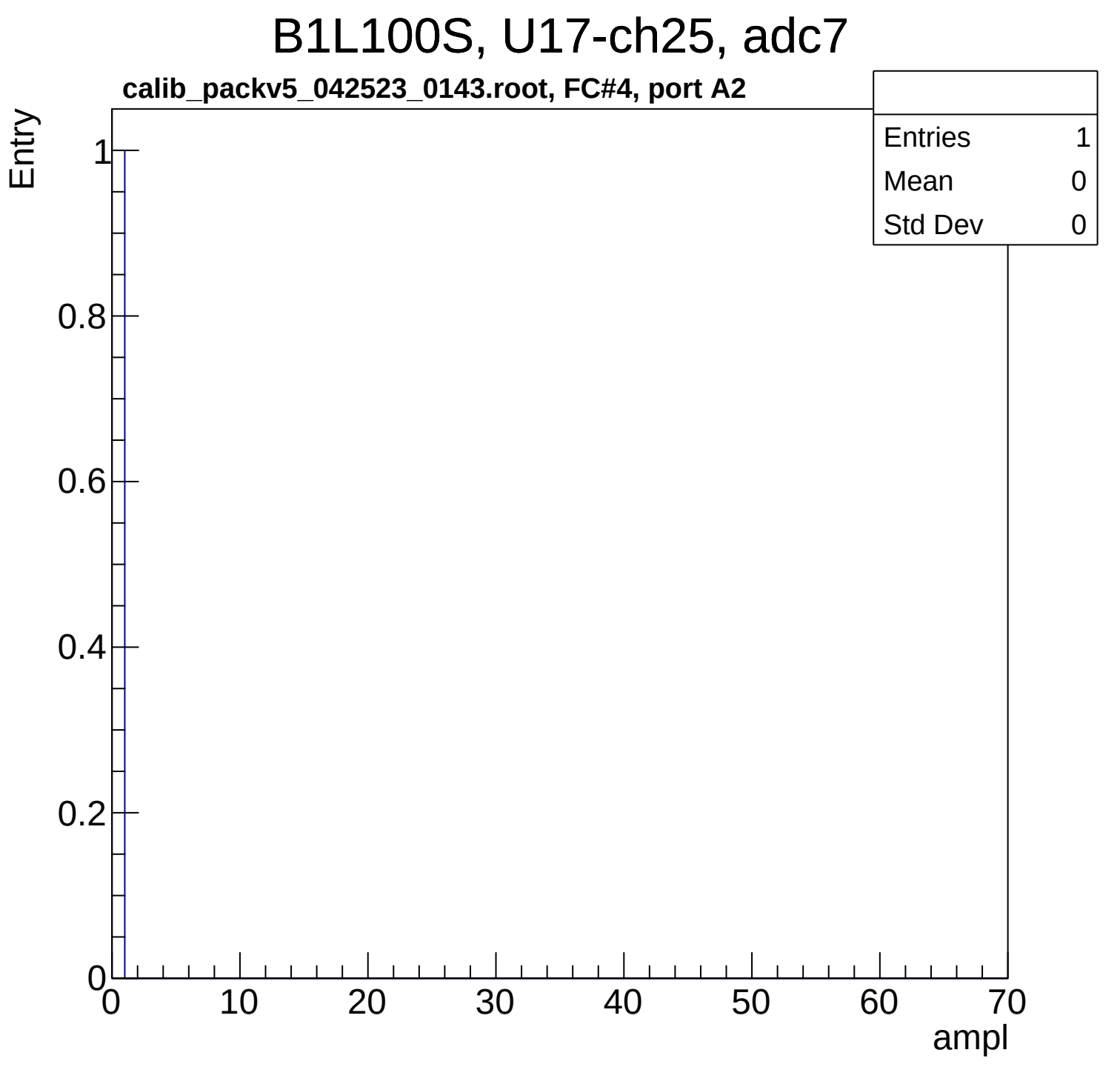

B1L100S, U17-ch25, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 9
Mean 54.56
Std Dev 19.33
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L100S, U17-ch25, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
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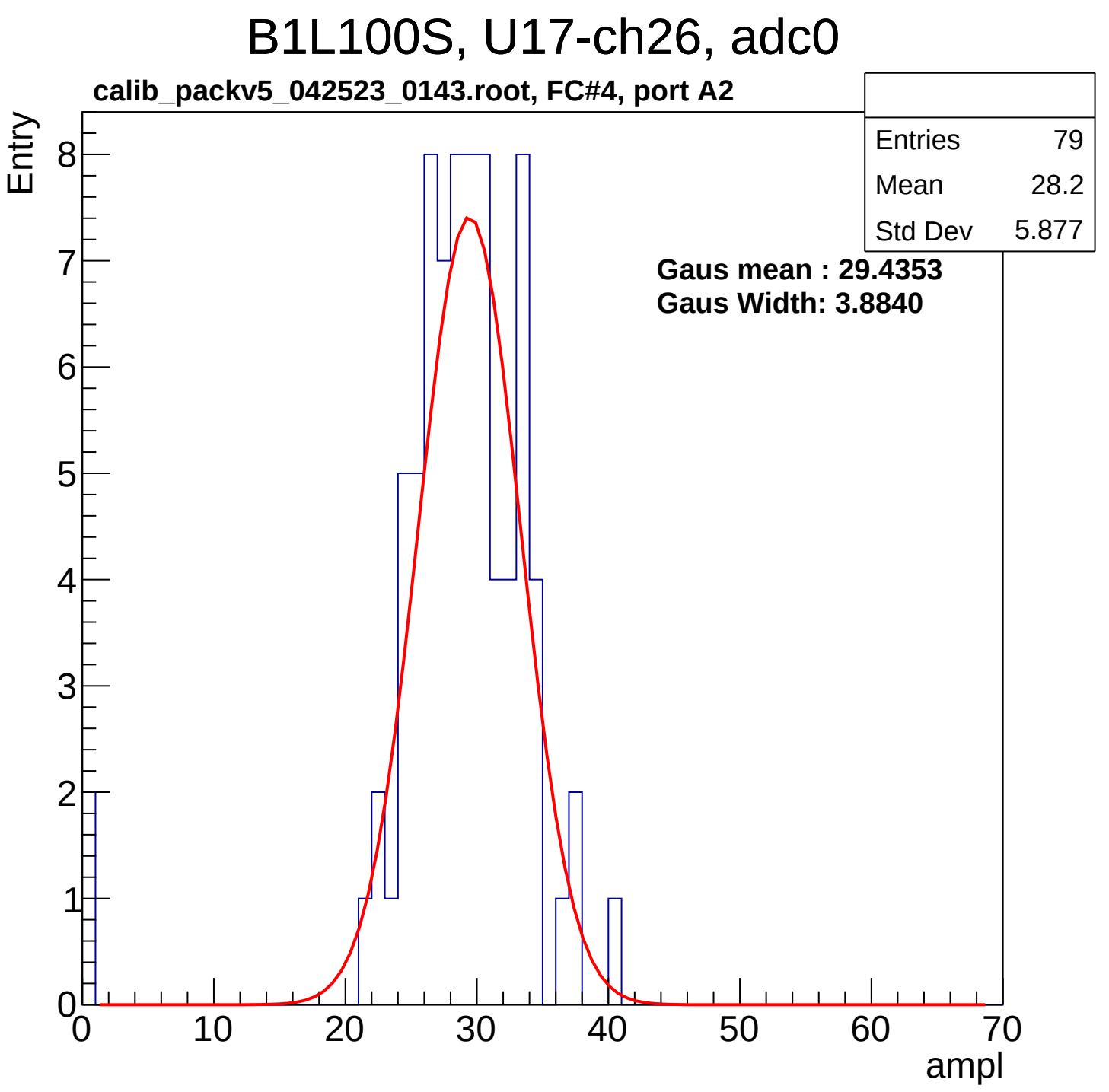
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch26, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 79
Mean 28.2
Std Dev 5.877
Gaus mean : 29.4353
Gaus Width: 3.8840
Entry
ampl
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2
3
4
5
6
7
8
0
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40
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60
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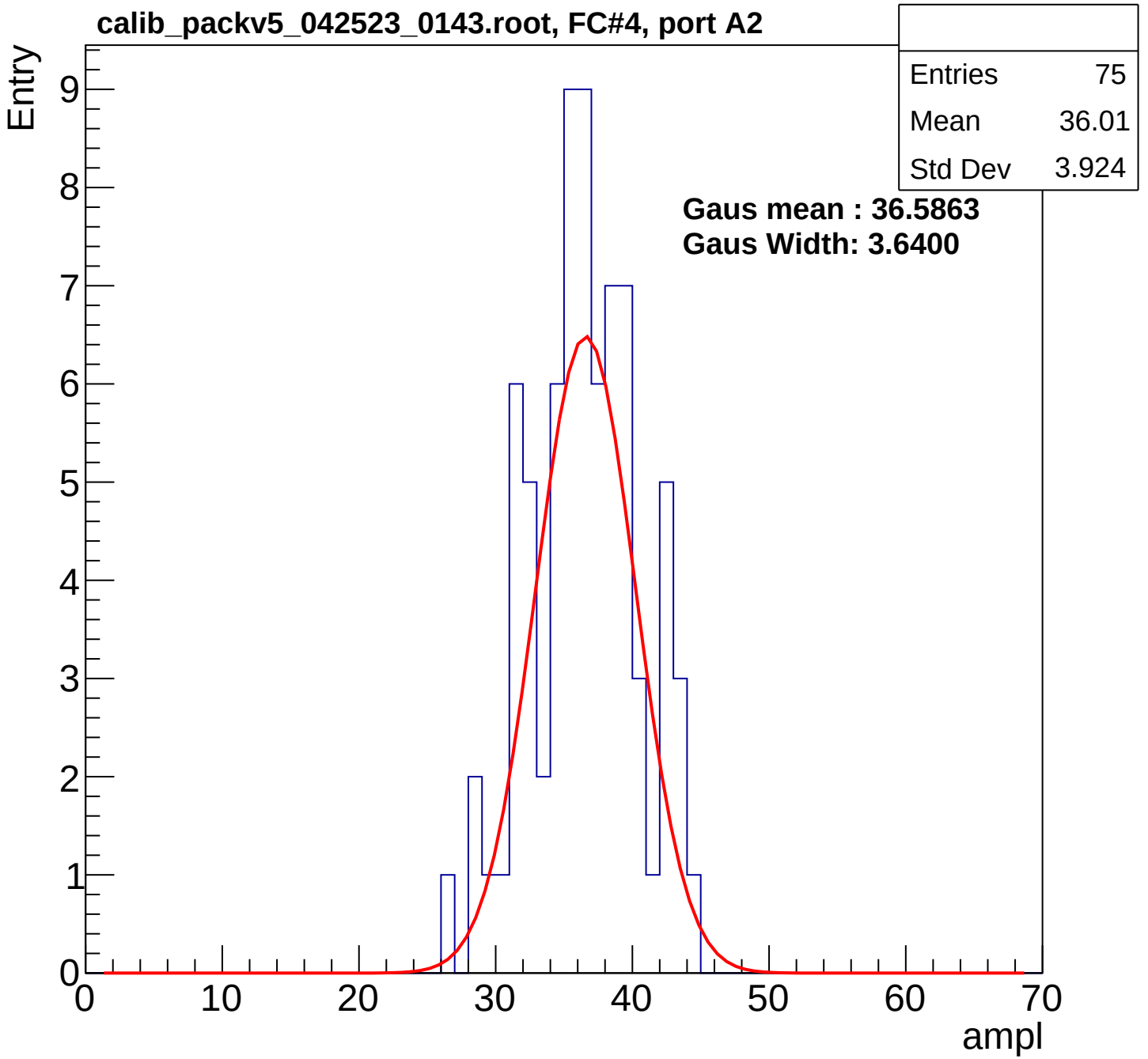
B1L100S, U17-ch26, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 75
Mean 36.01
Std Dev 3.924
Gaus mean : 36.5863
Gaus Width: 3.6400
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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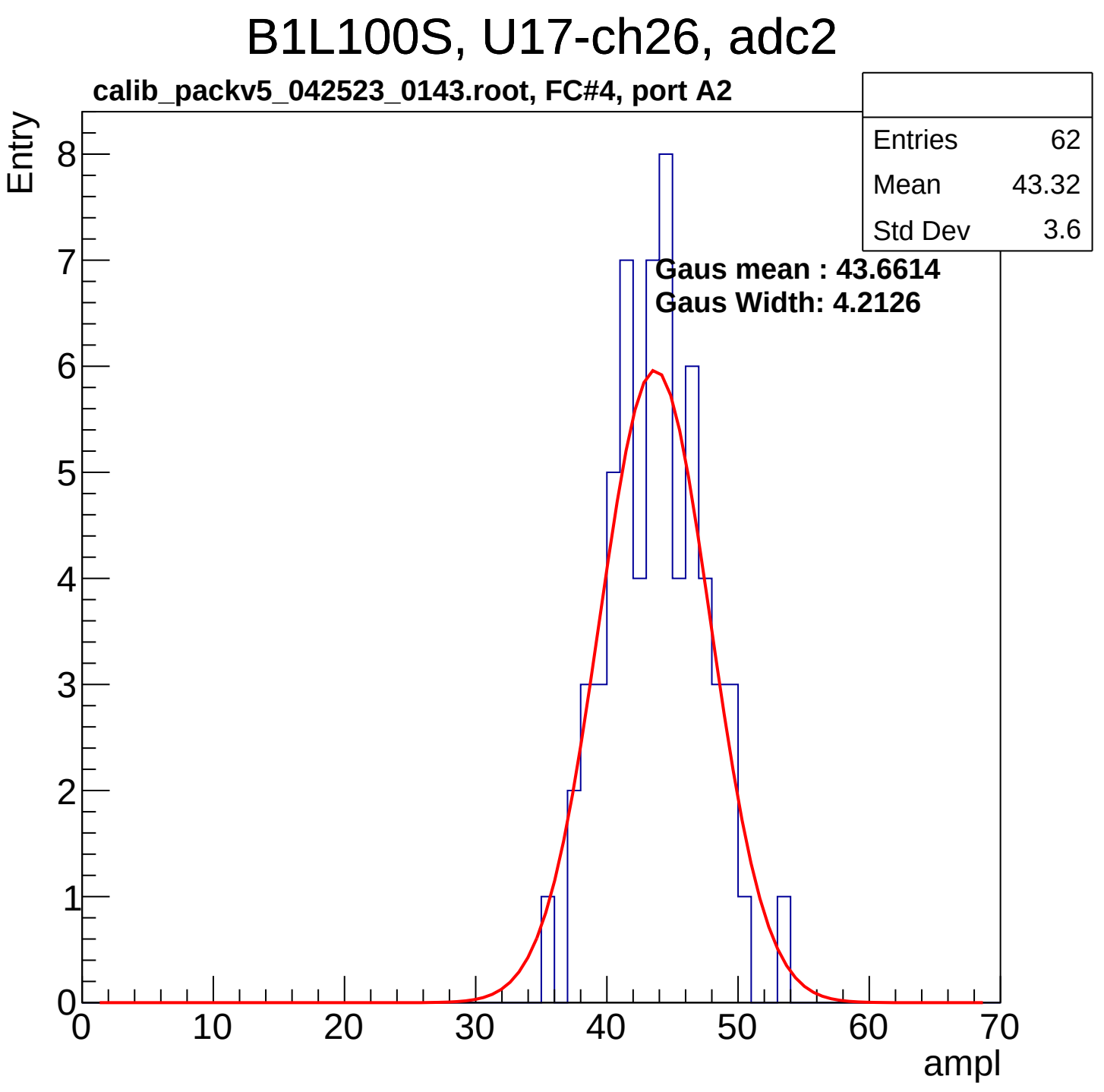
B1L100S, U17-ch26, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 43.32
Std Dev 3.6
Gaus mean : 43.6614
Gaus Width: 4.2126
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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60
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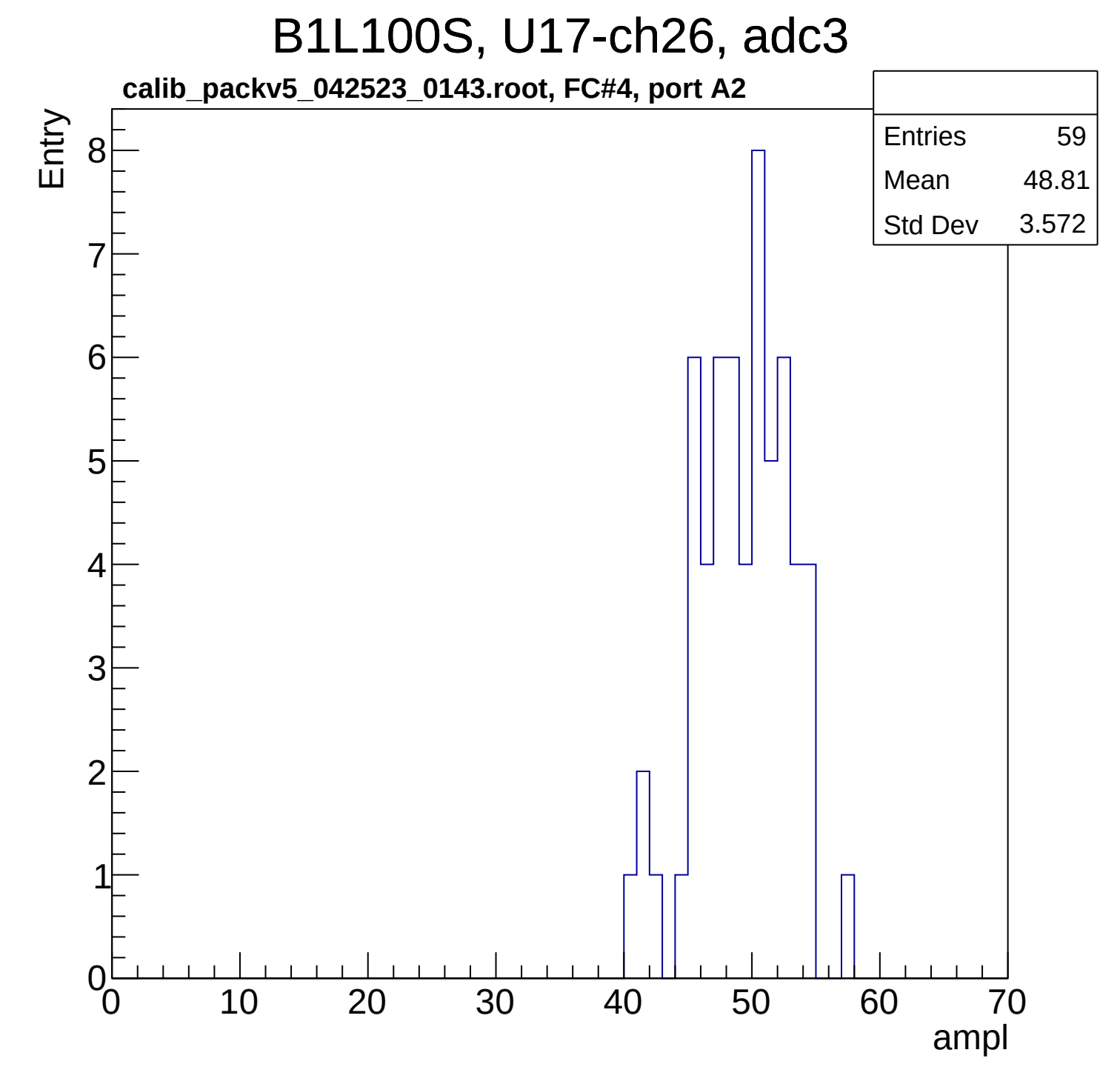
B1L100S, U17-ch26, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 48.81
Std Dev 3.572
Entry
ampl
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2
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4
5
6
7
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0
10
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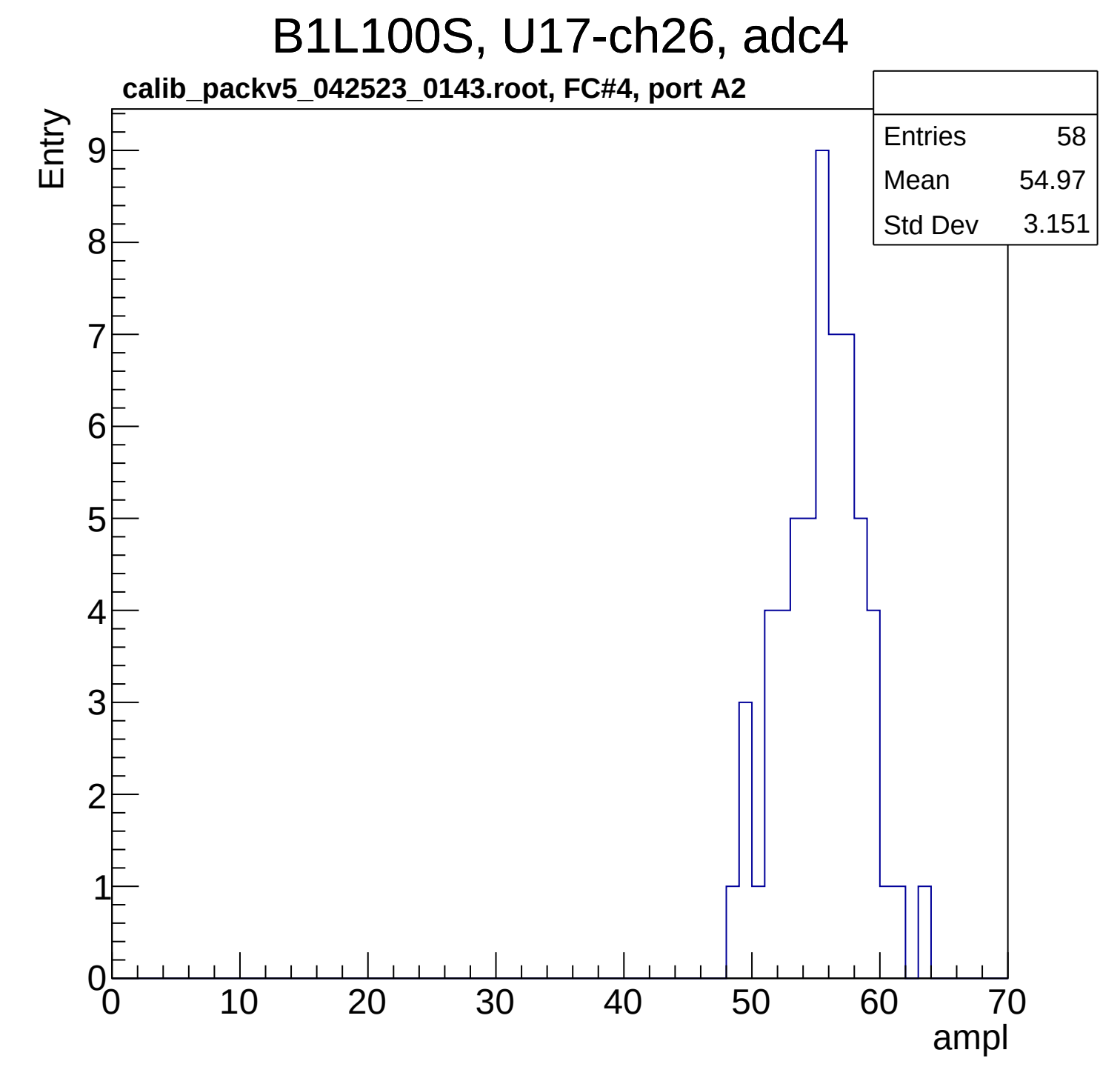
B1L100S, U17-ch26, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 54.97
Std Dev 3.151
Entry
ampl
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3
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6
7
8
9
0
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20
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40
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60
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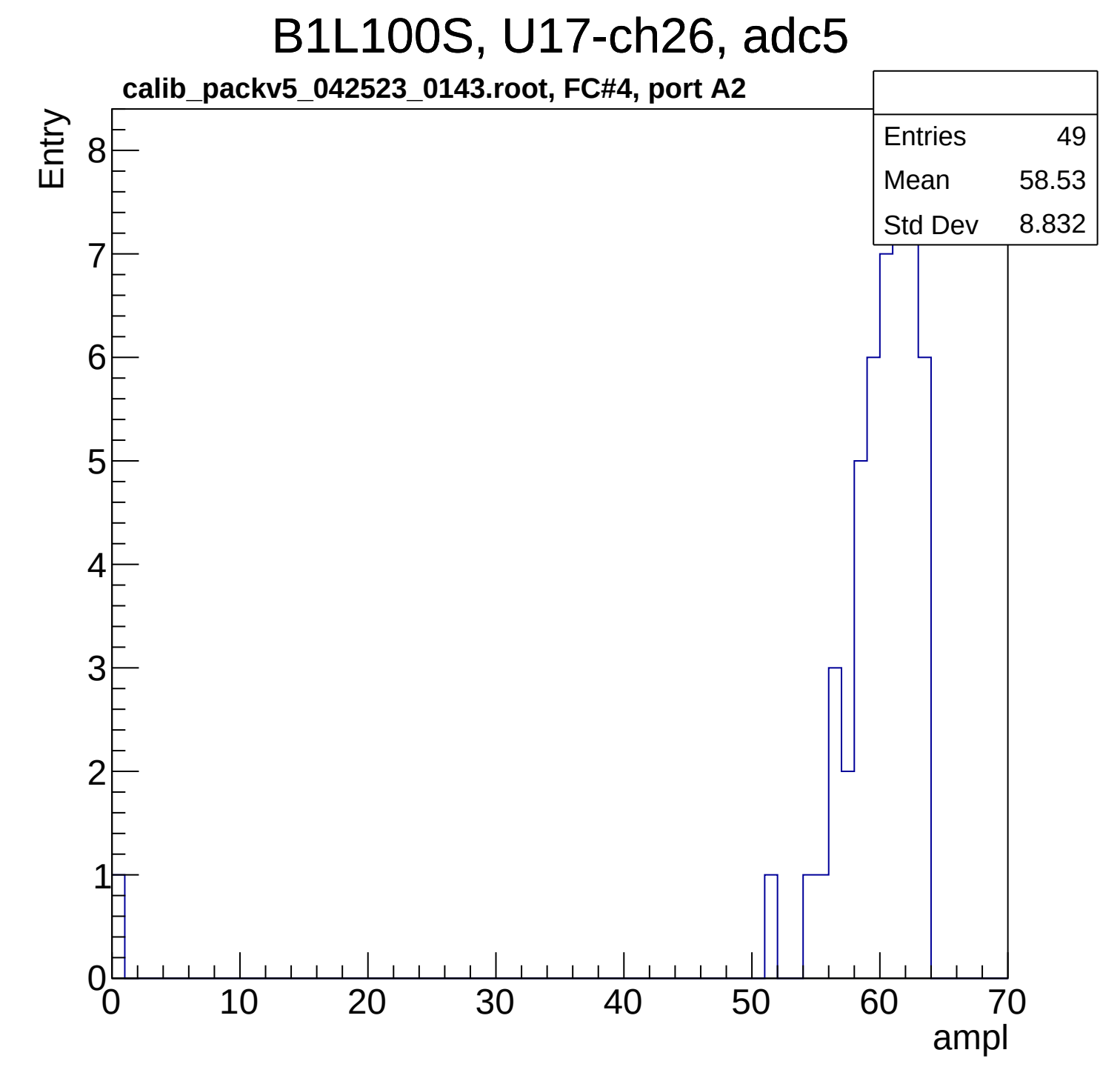
B1L100S, U17-ch26, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 49
Mean 58.53
Std Dev 8.832
Entry
ampl
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1
2
3
4
5
6
7
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0
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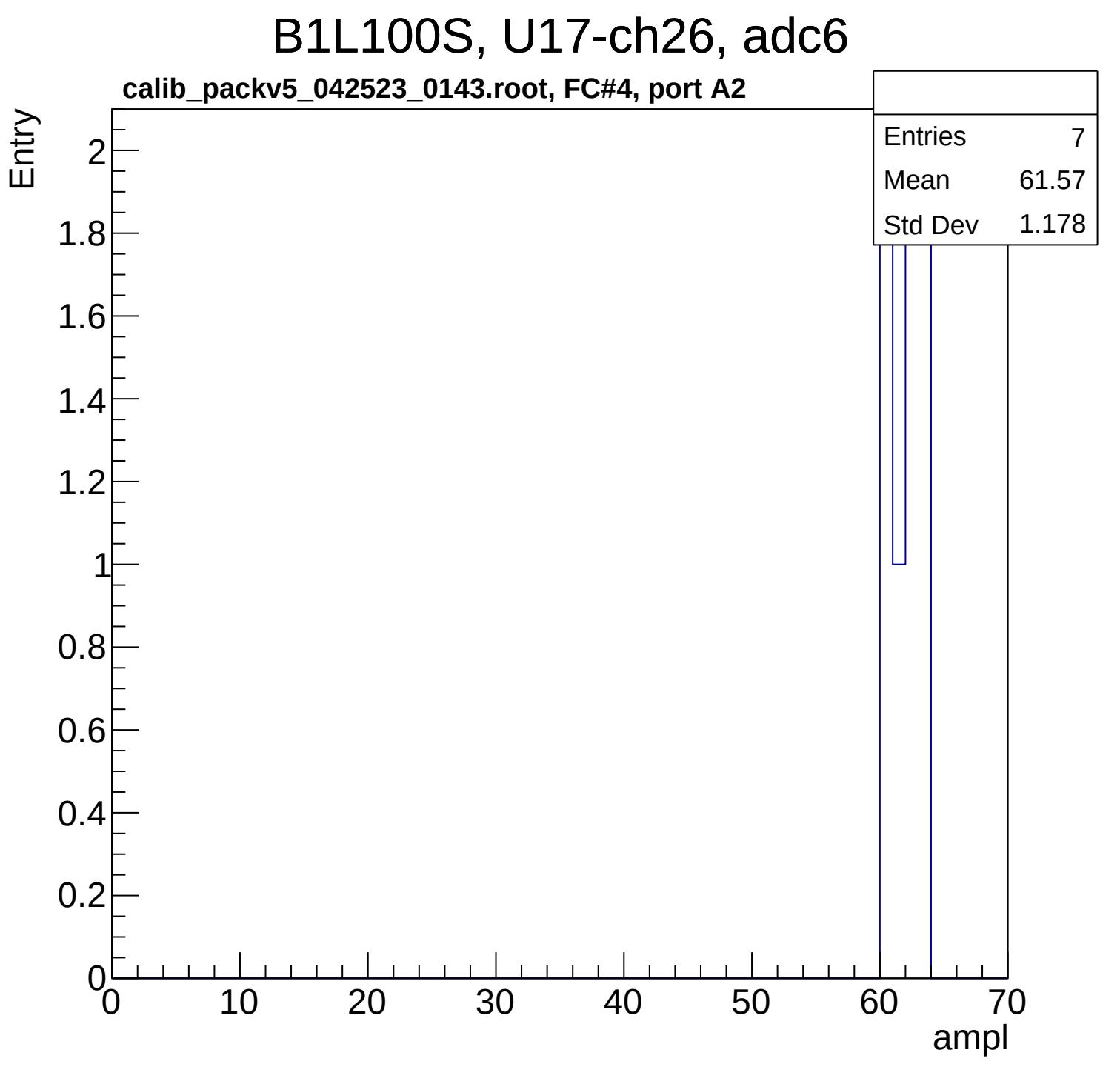
B1L100S, U17-ch26, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 7
Mean 61.57
Std Dev 1.178
Entry
ampl
0
0.2
0.4
0.6
0.8
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1.2
1.4
1.6
1.8
2
0
10
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40
50
60
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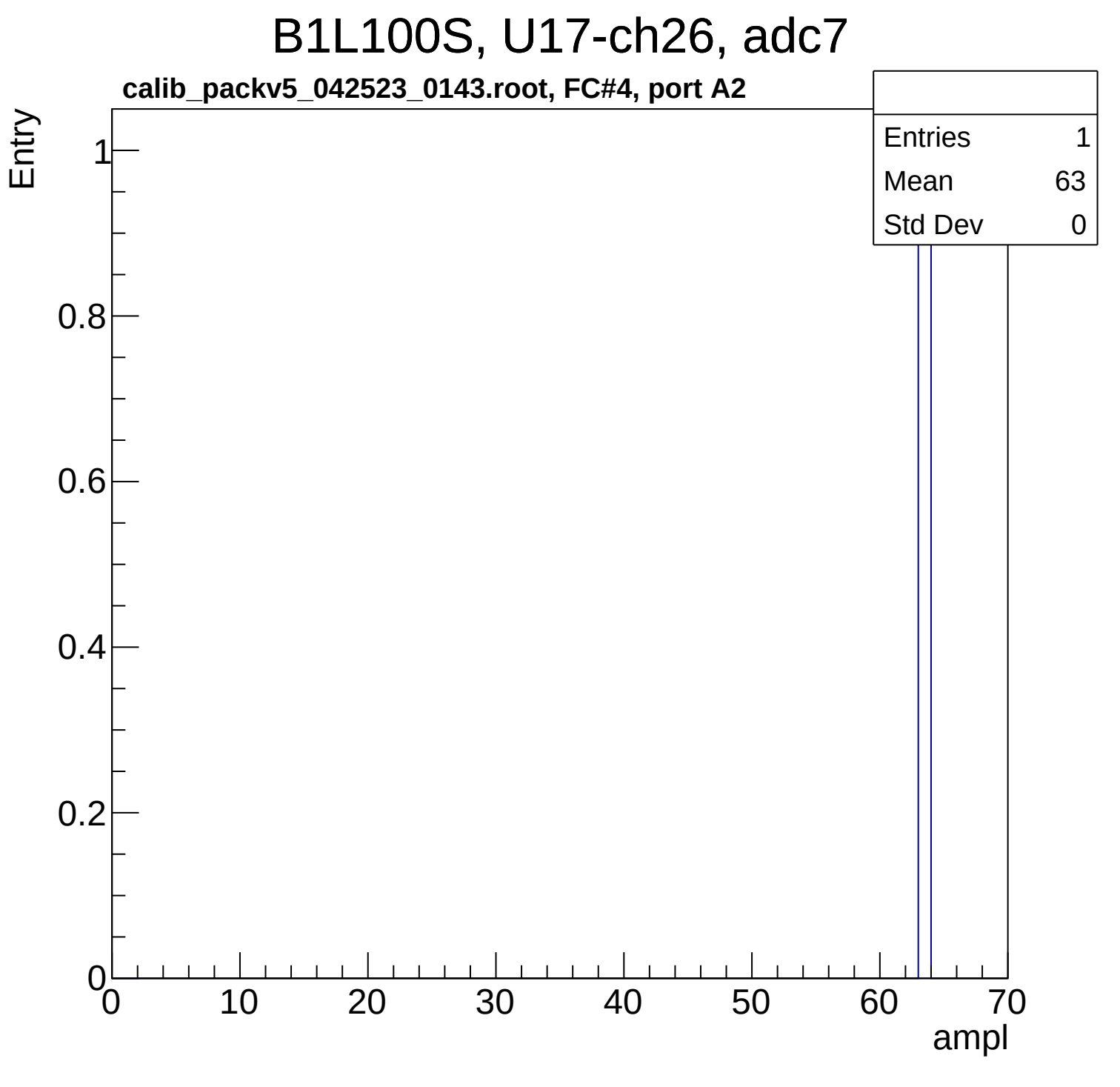
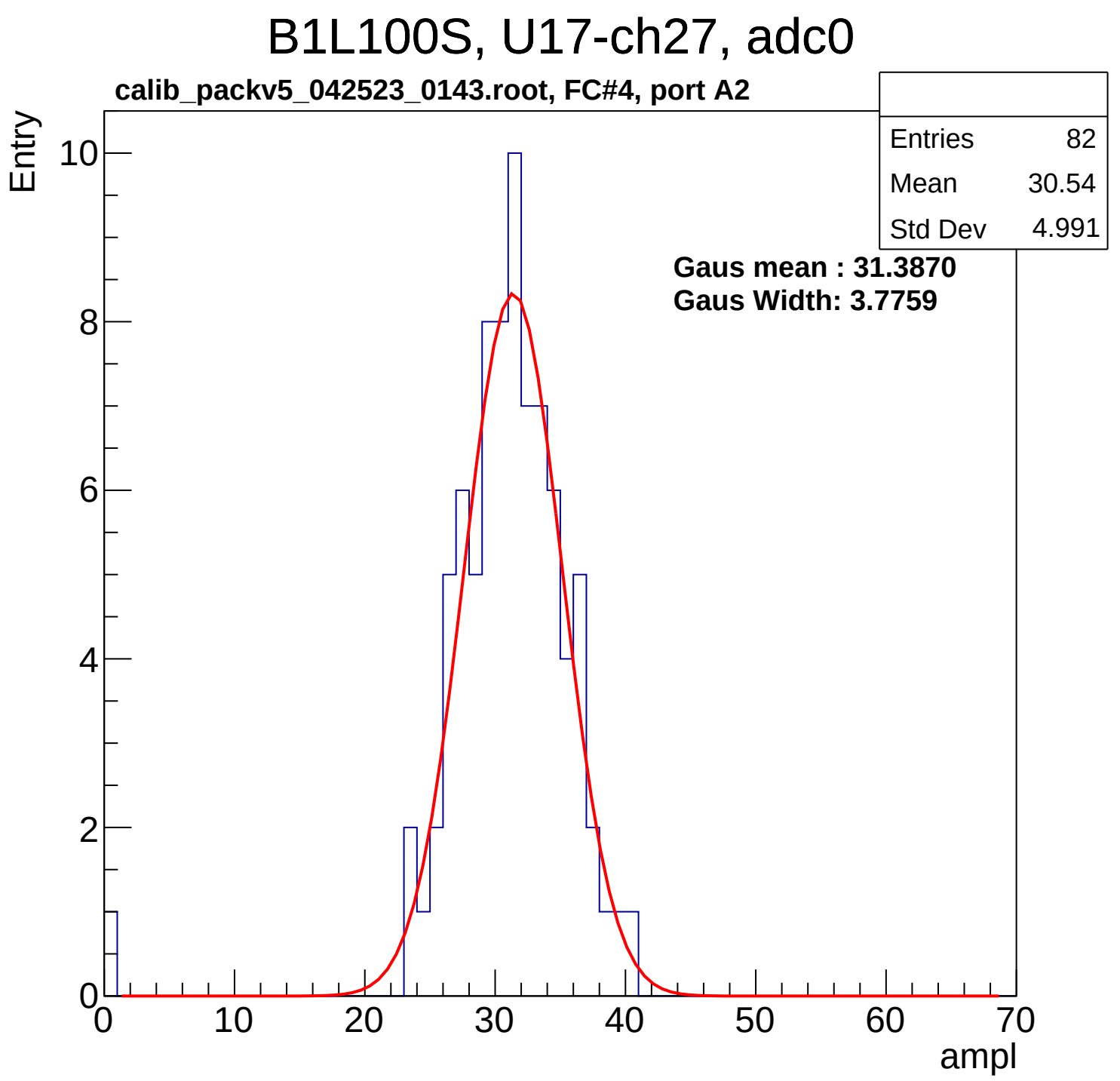

B1L100S, U17-ch26, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch27, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 82
Mean 30.54
Std Dev 4.991
Gaus mean : 31.3870
Gaus Width: 3.7759
Entry
ampl
0
2
4
6
8
10
0
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20
30
40
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60
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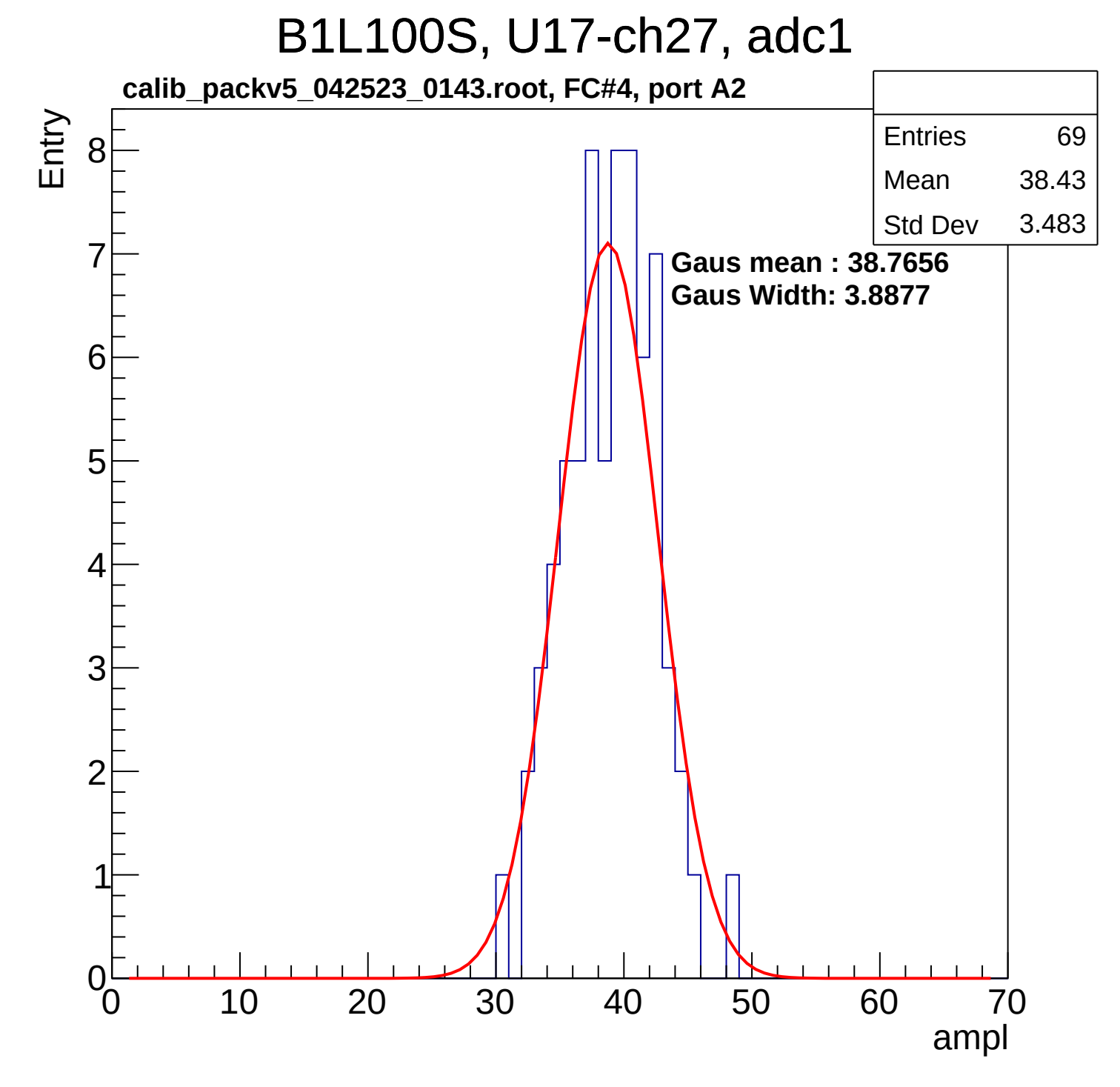
B1L100S, U17-ch27, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 38.43
Std Dev 3.483
Gaus mean : 38.7656
Gaus Width: 3.8877
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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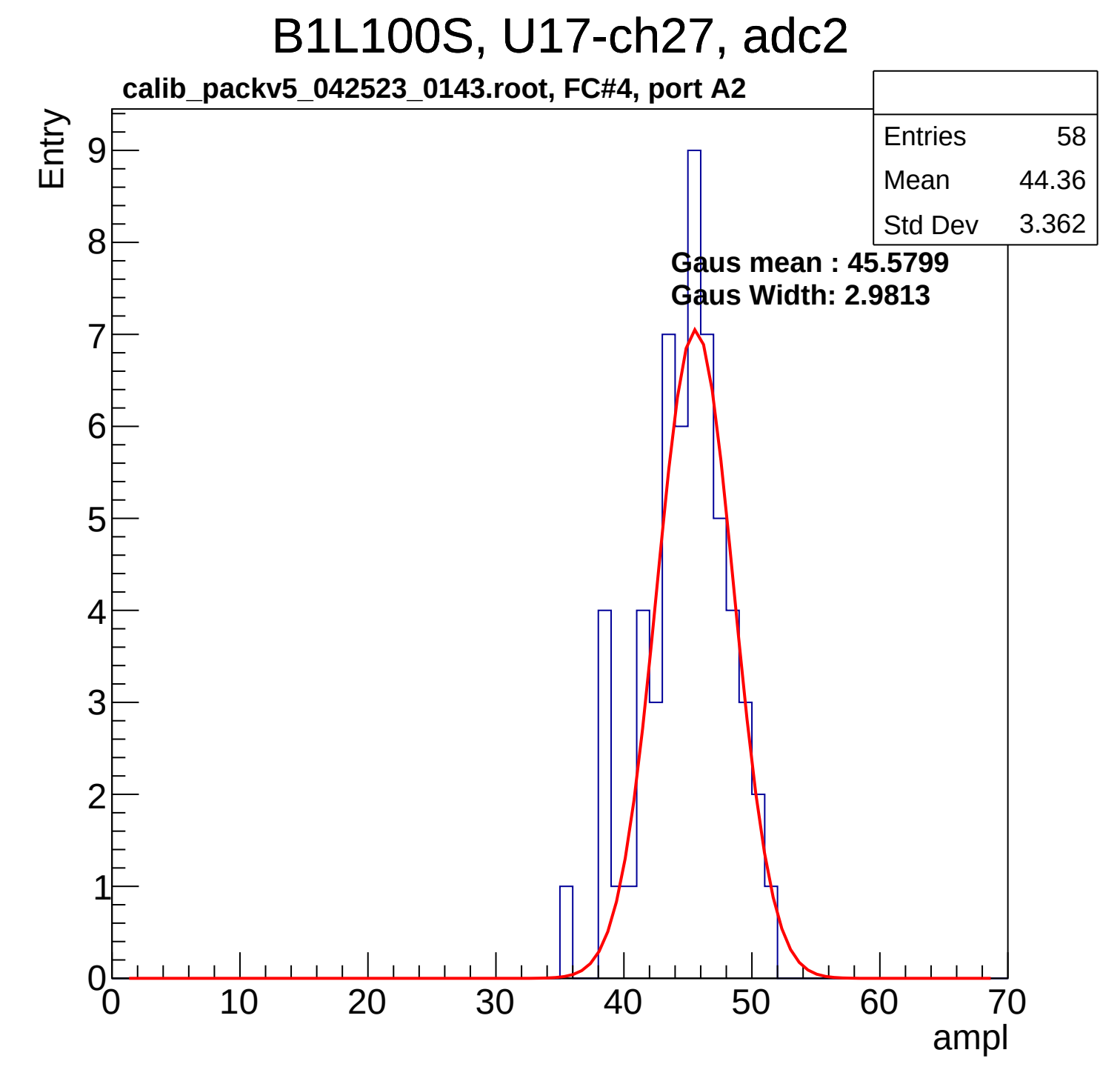
B1L100S, U17-ch27, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 44.36
Std Dev 3.362
Gaus mean : 45.5799
Gaus Width: 2.9813
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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40
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60
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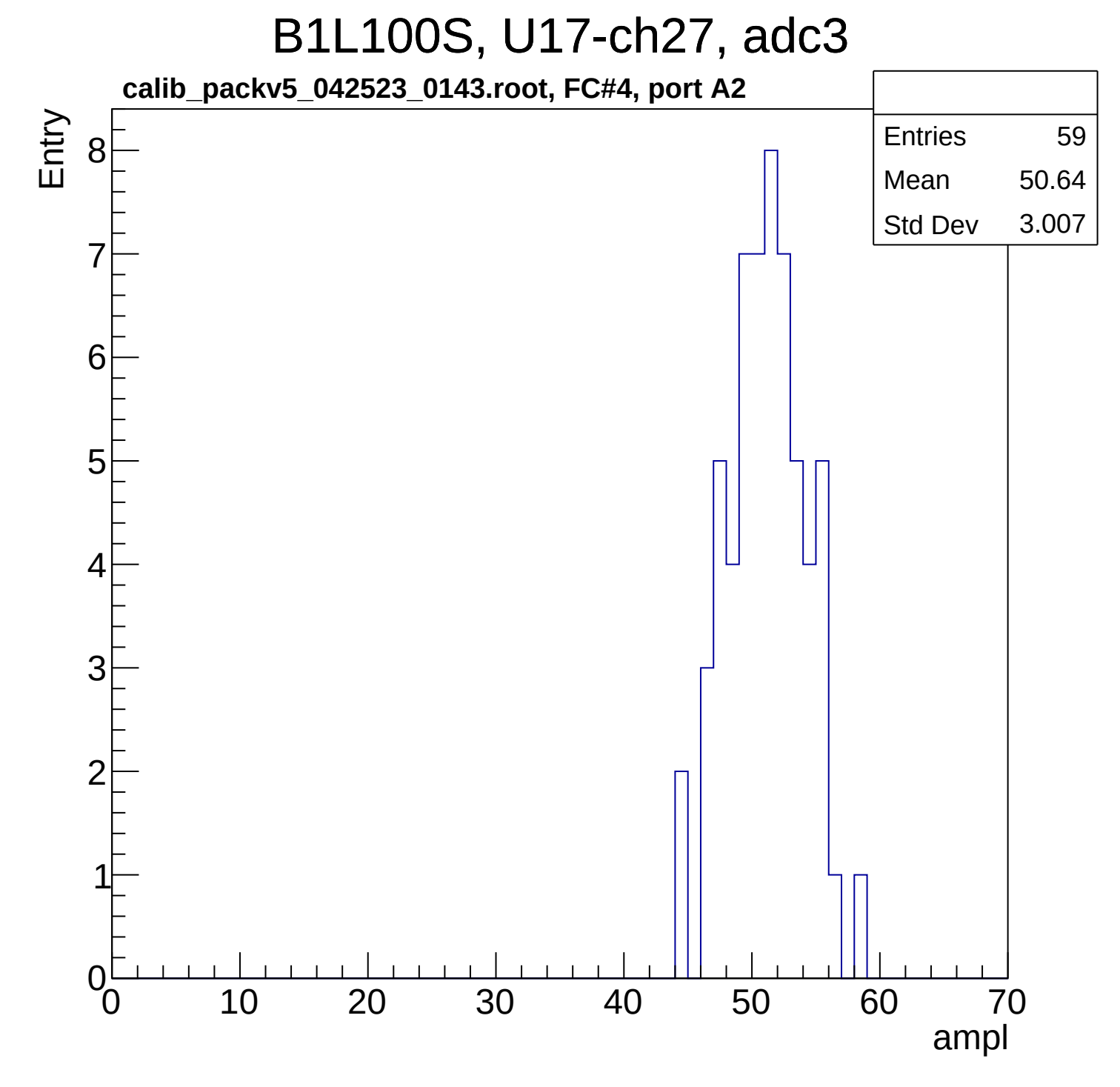
B1L100S, U17-ch27, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 50.64
Std Dev 3.007
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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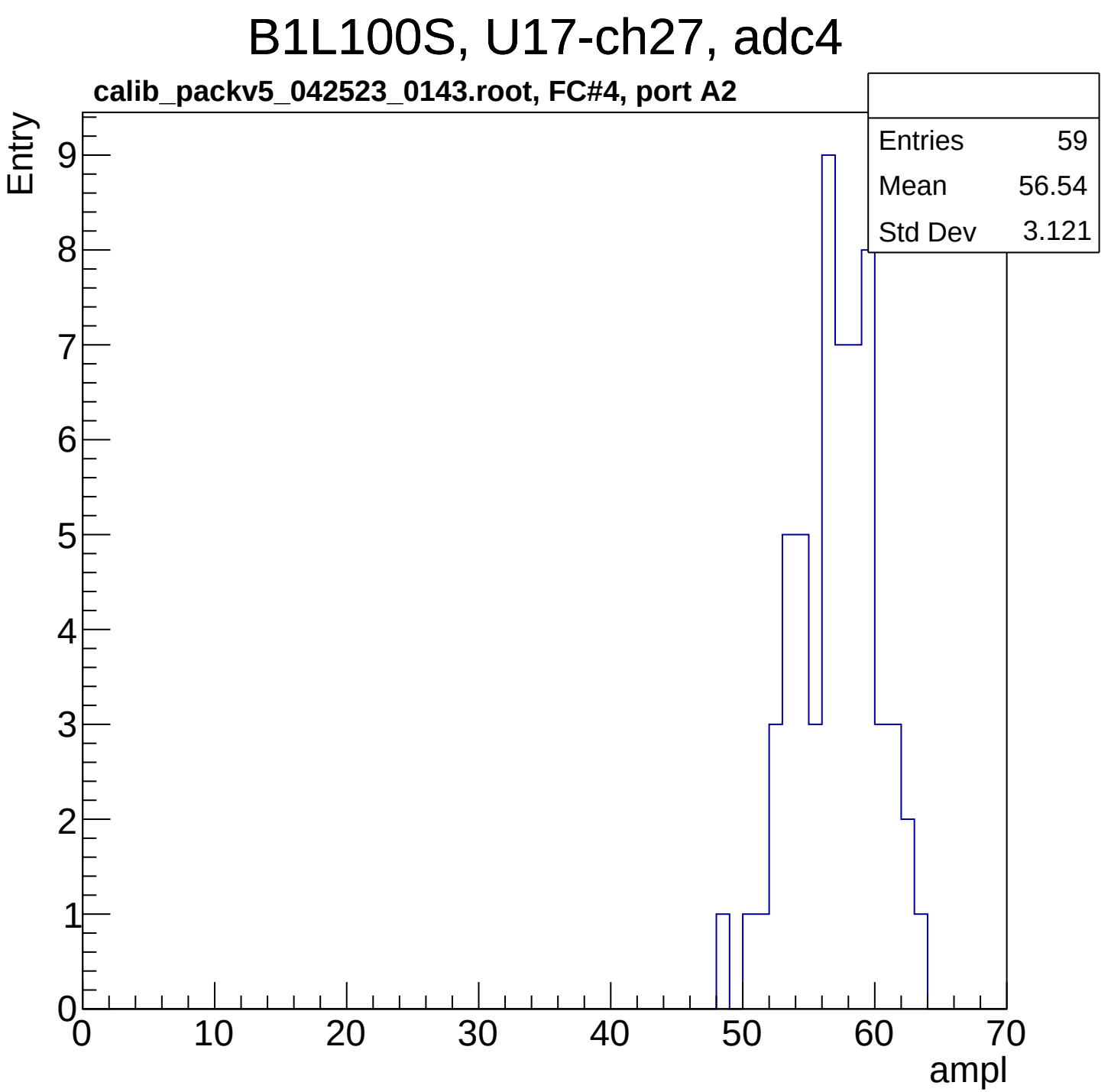
B1L100S, U17-ch27, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 56.54
Std Dev 3.121
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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60
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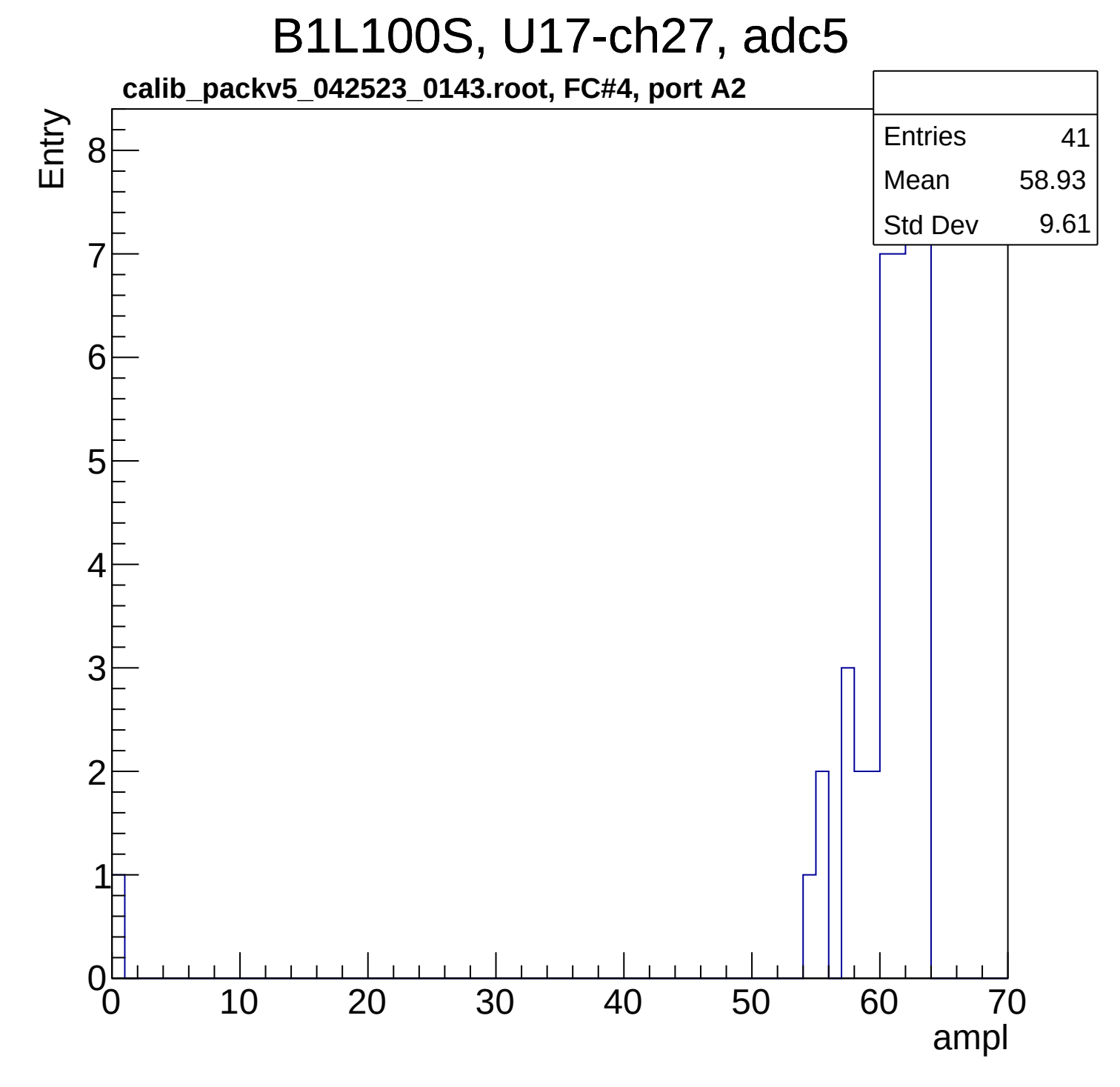
B1L100S, U17-ch27, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 41
Mean 58.93
Std Dev 9.61
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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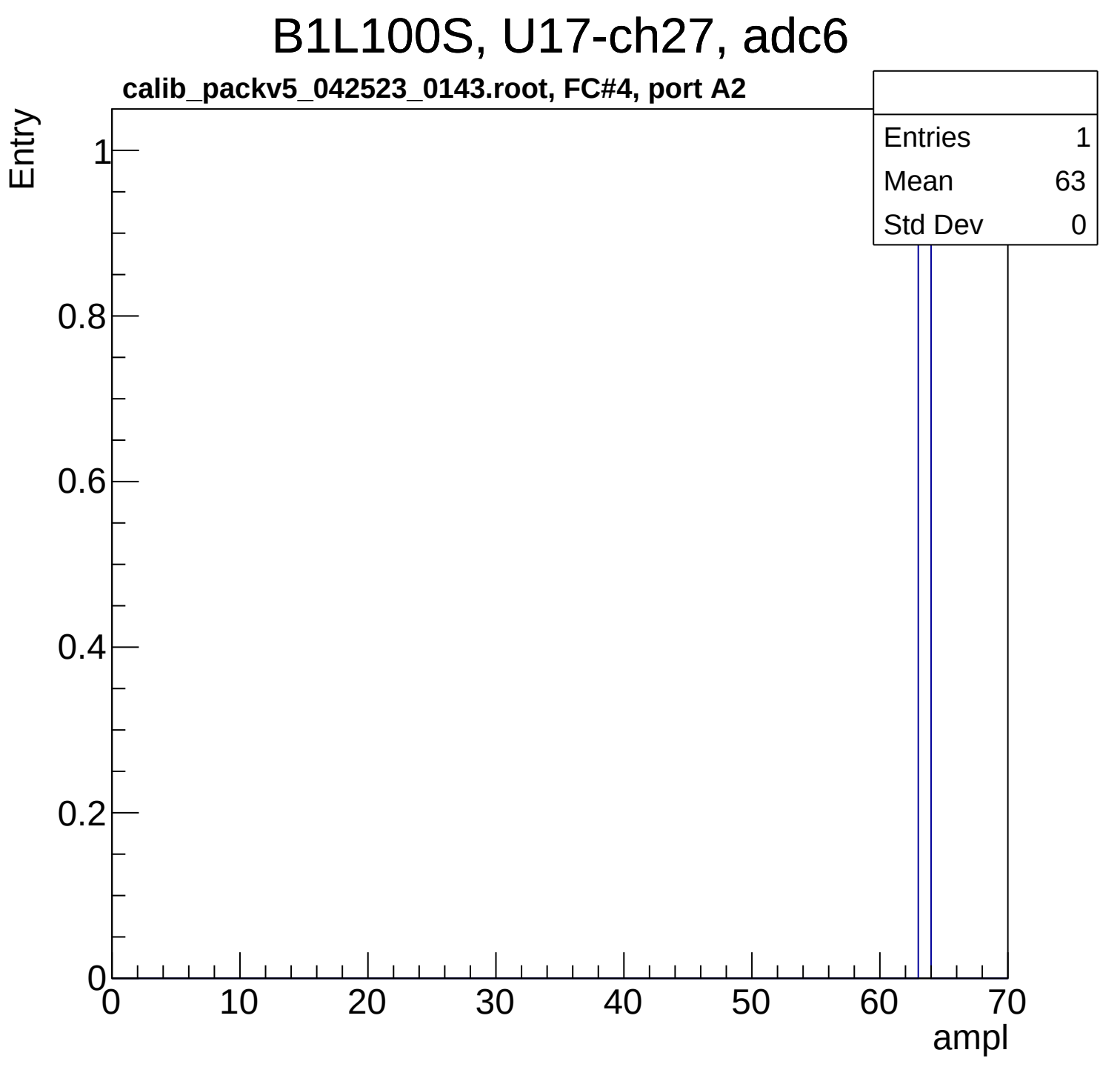
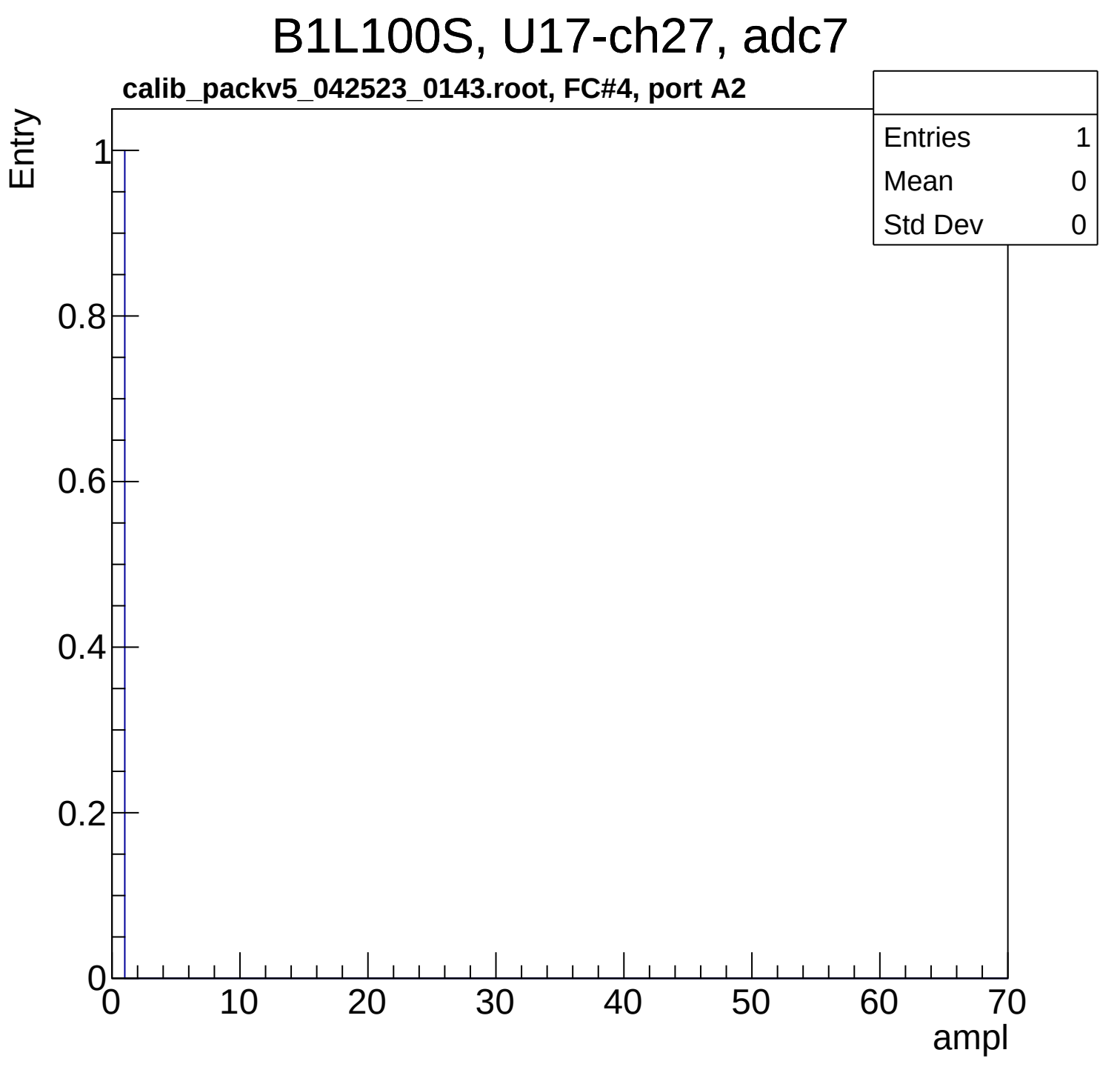
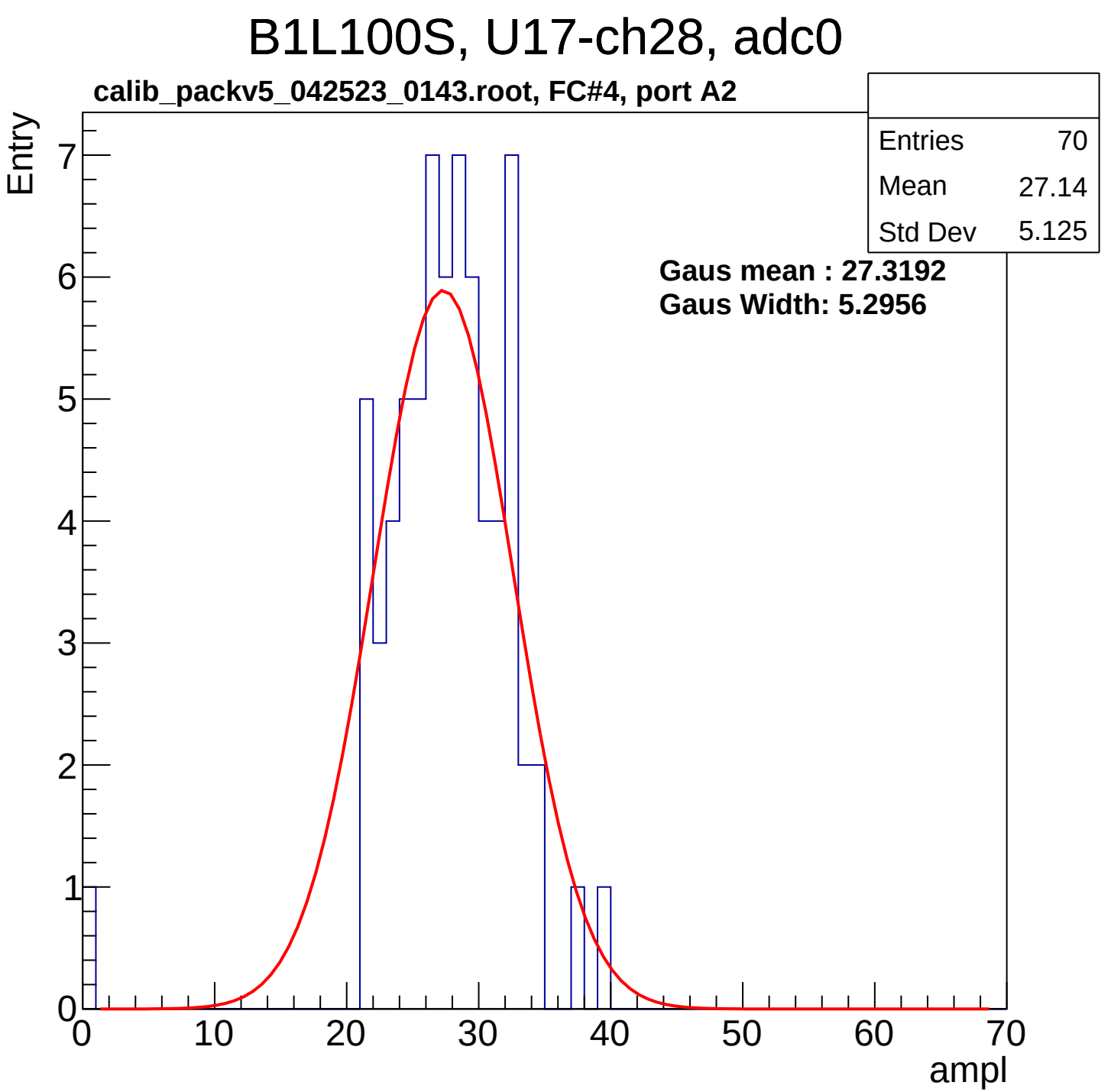
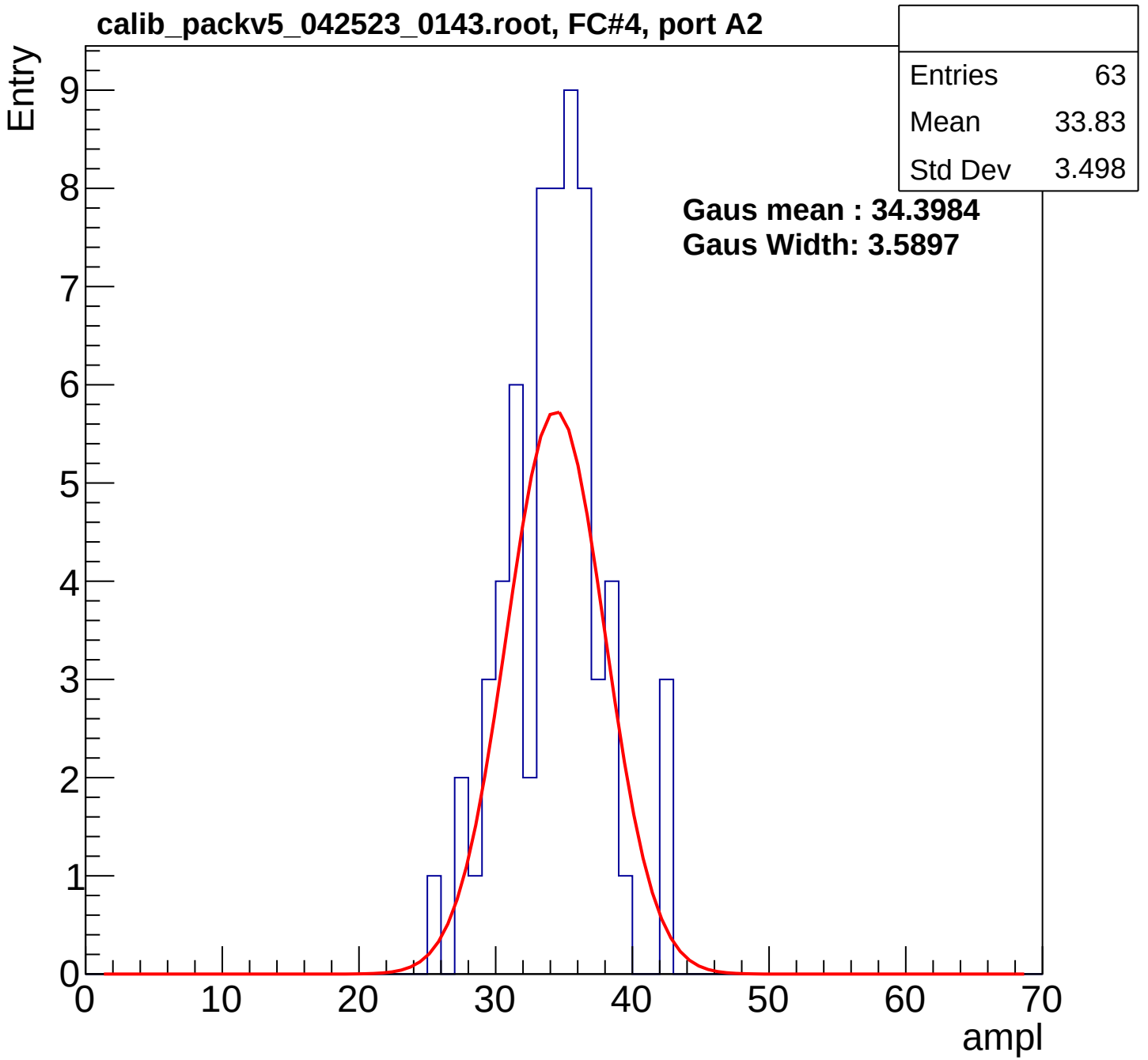

B1L100S, U17-ch27, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch27, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch28, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 27.14
Std Dev 5.125
Gaus mean : 27.3192
Gaus Width: 5.2956
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U17-ch28, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 33.83
Std Dev 3.498
Gaus mean : 34.3984
Gaus Width: 3.5897
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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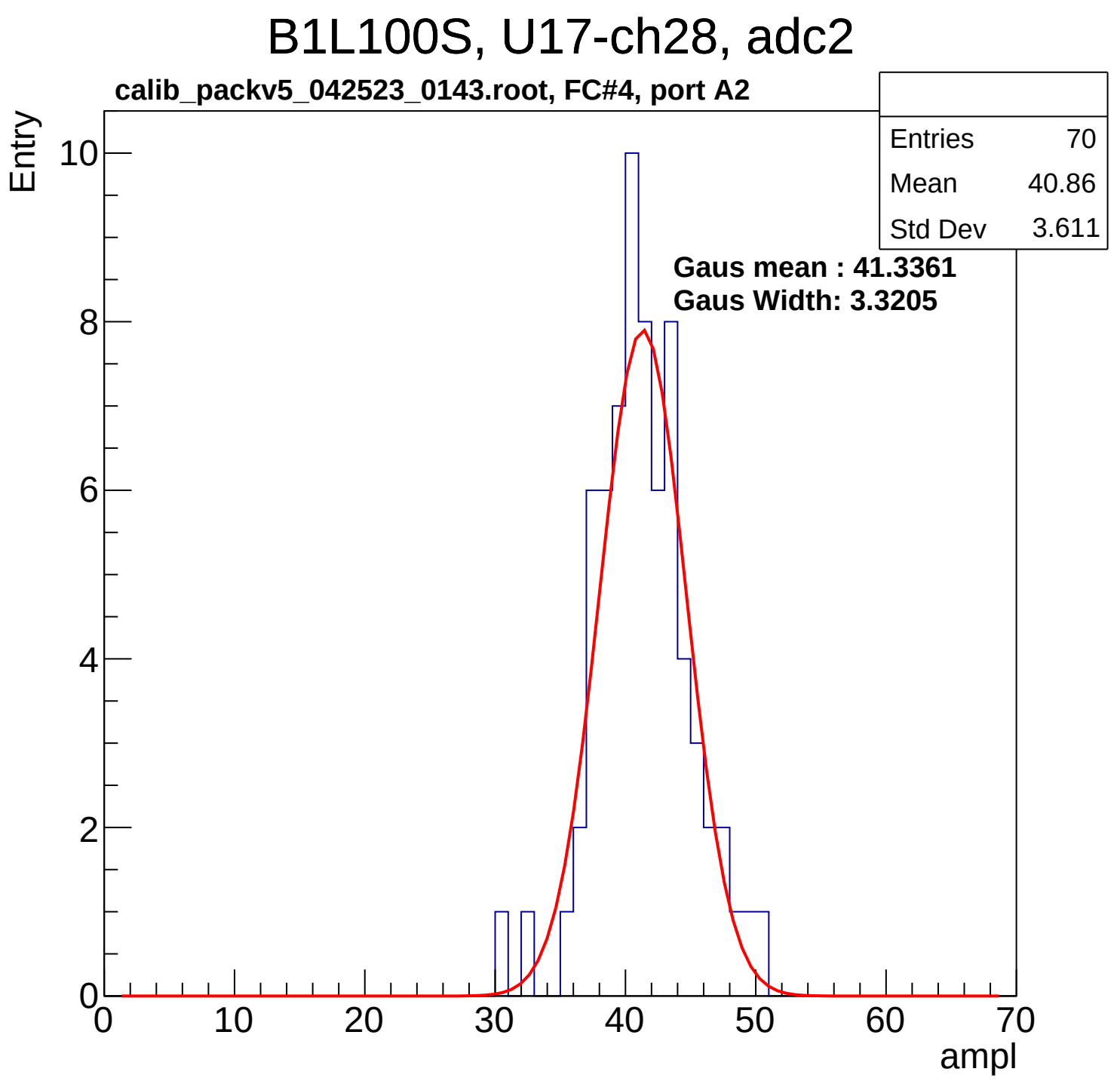
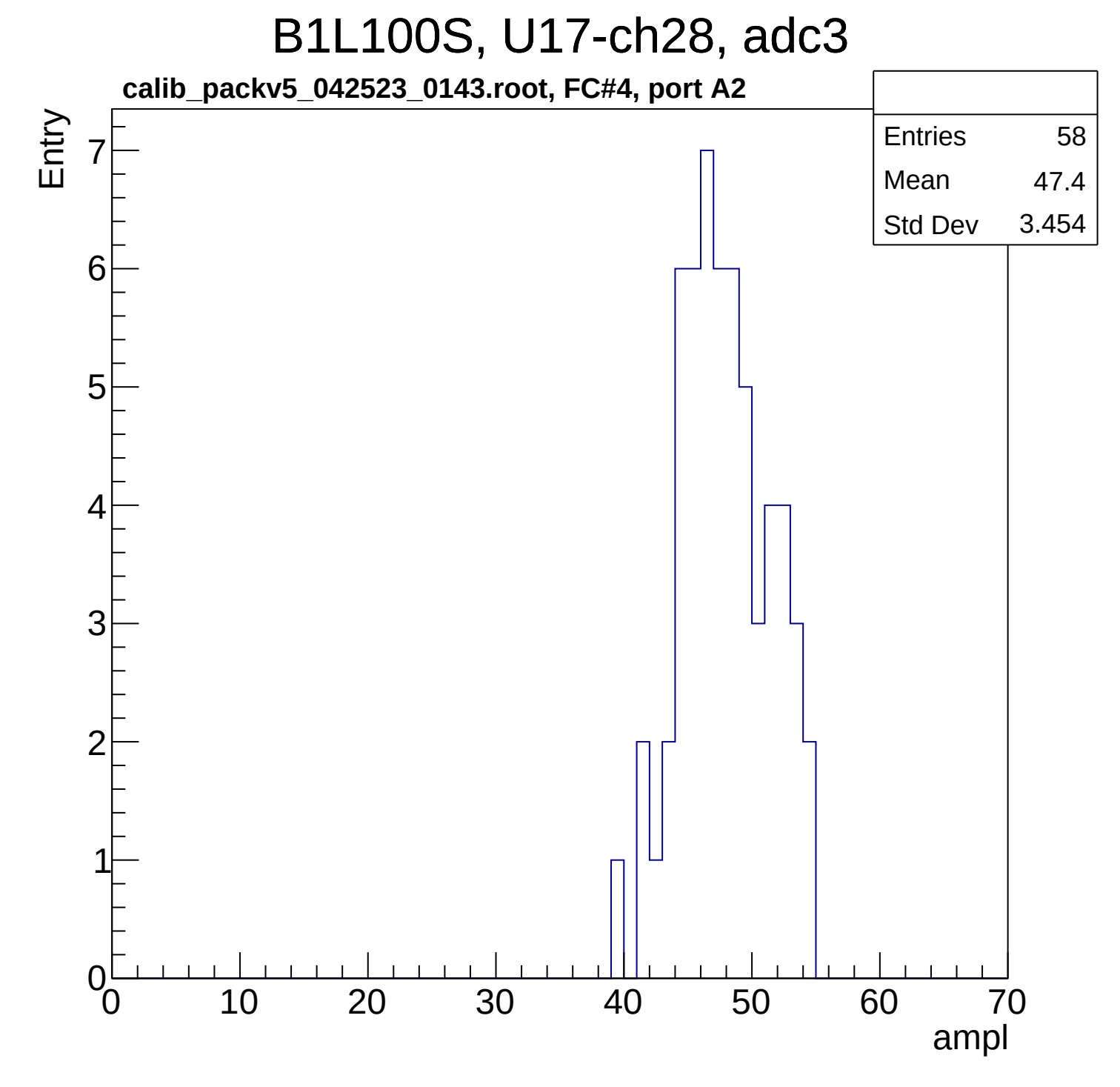

B1L100S, U17-ch28, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 40.86
Std Dev 3.611
Gaus mean : 41.3361
Gaus Width: 3.3205
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U17-ch28, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 47.4
Std Dev 3.454
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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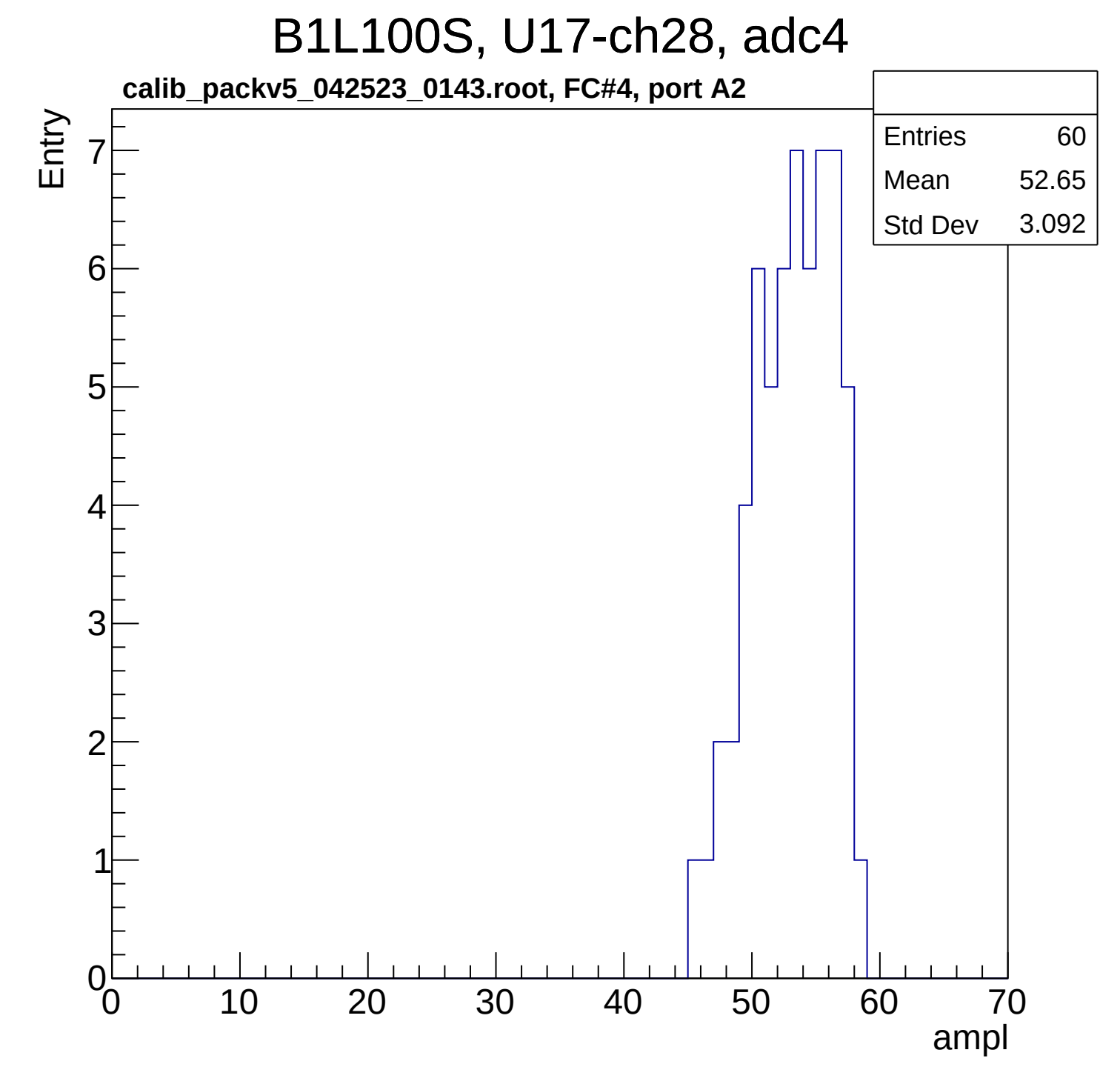
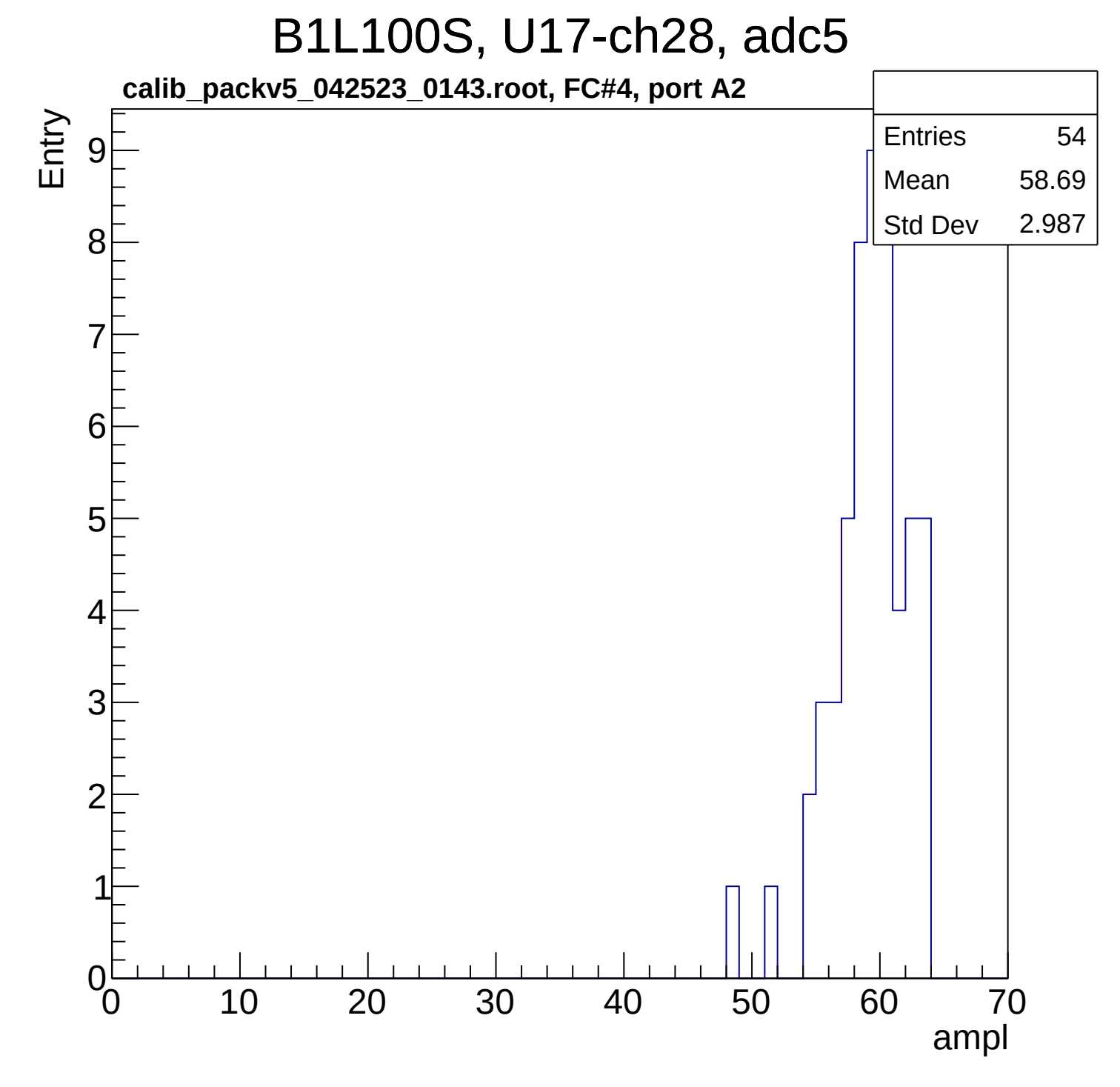
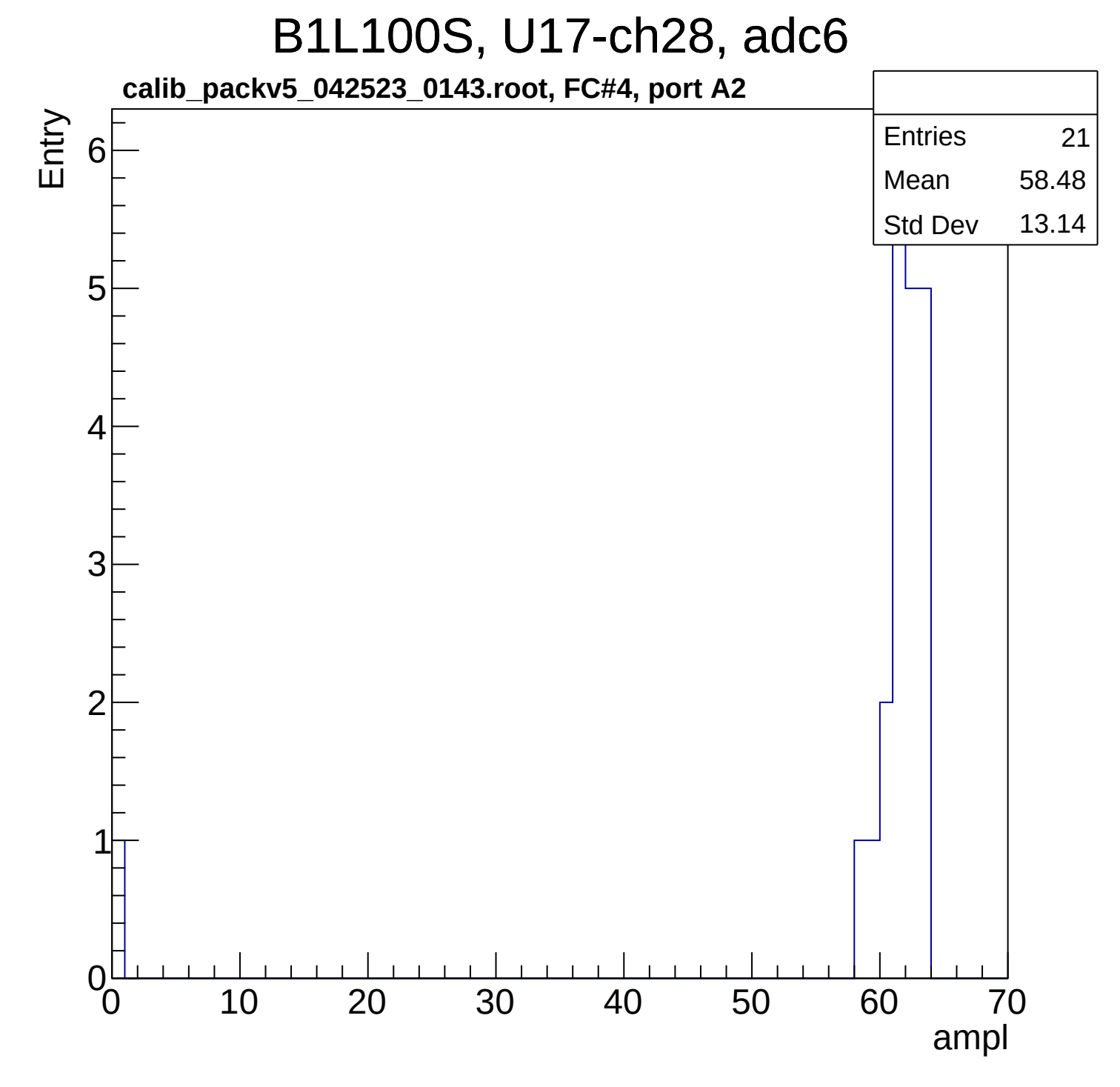
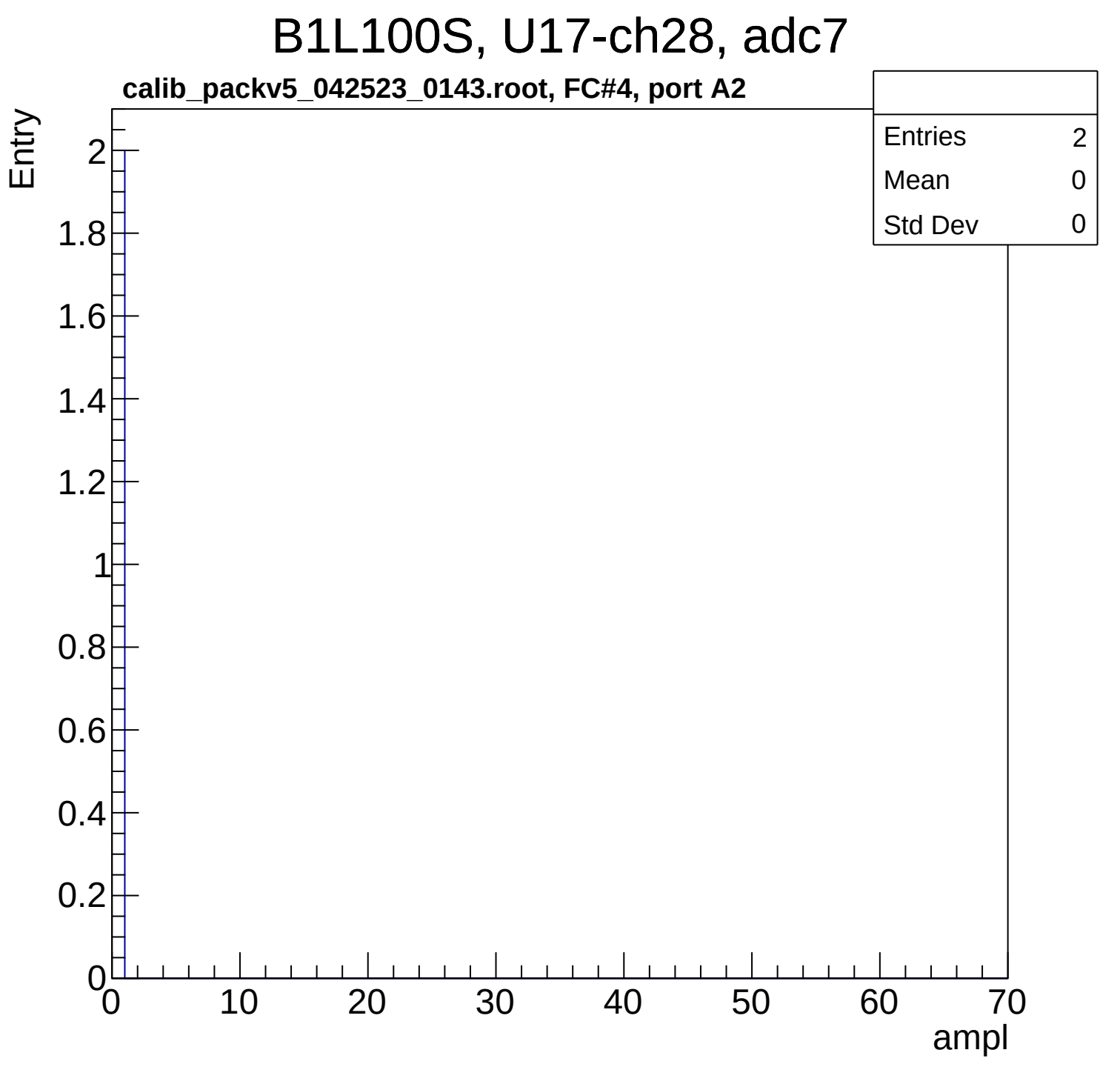
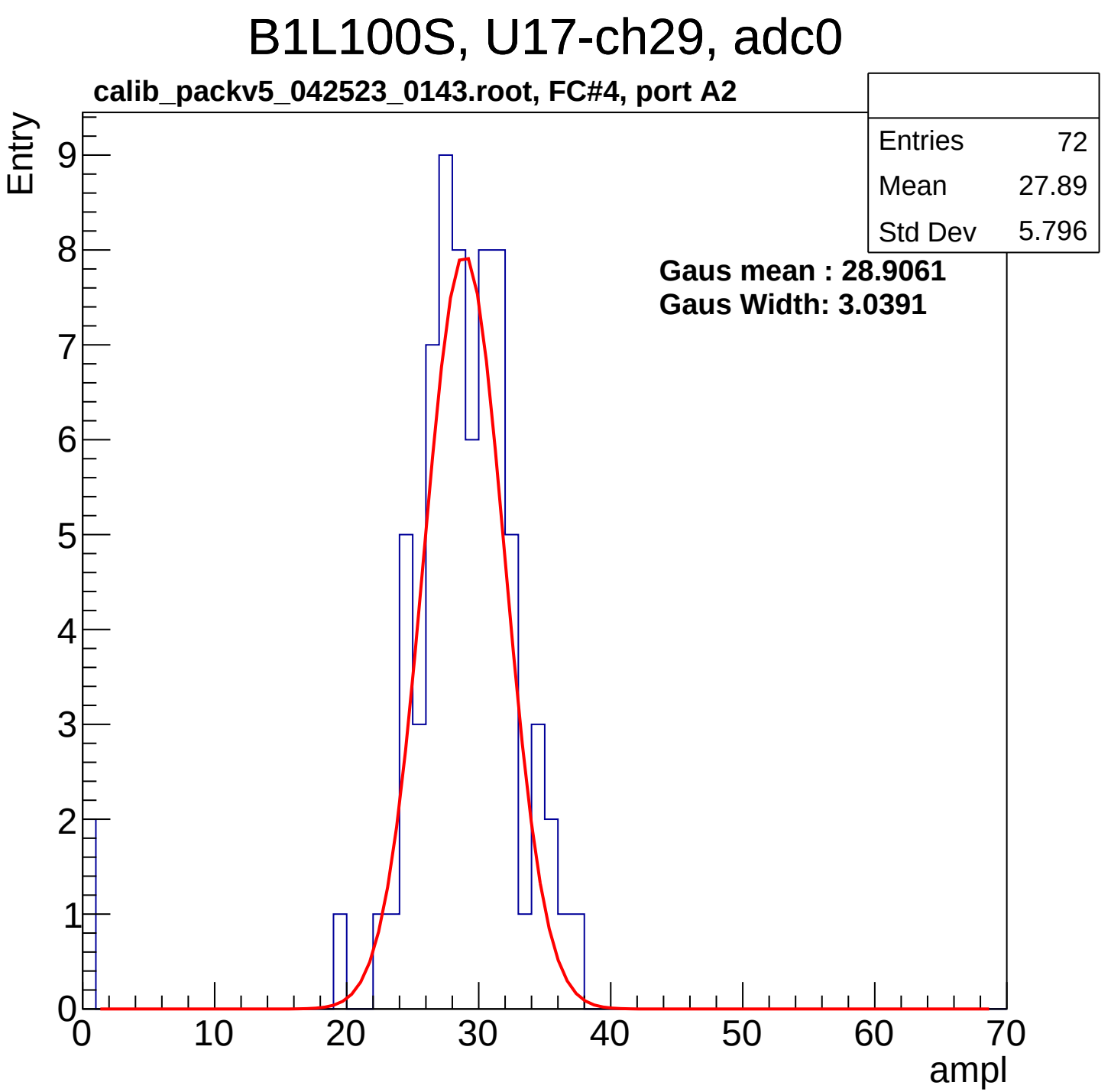
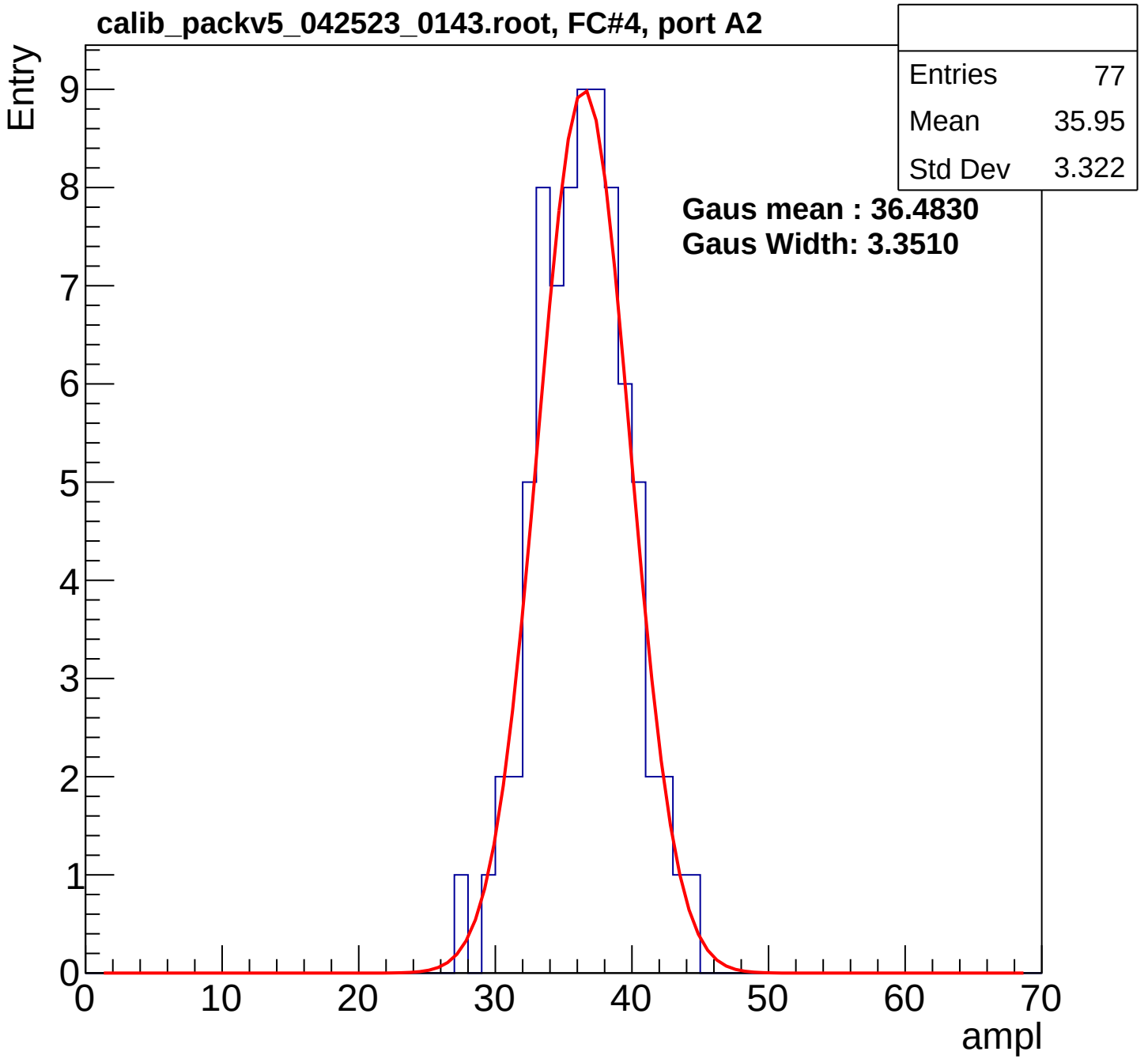

B1L100S, U17-ch28, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 52.65
Std Dev 3.092
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

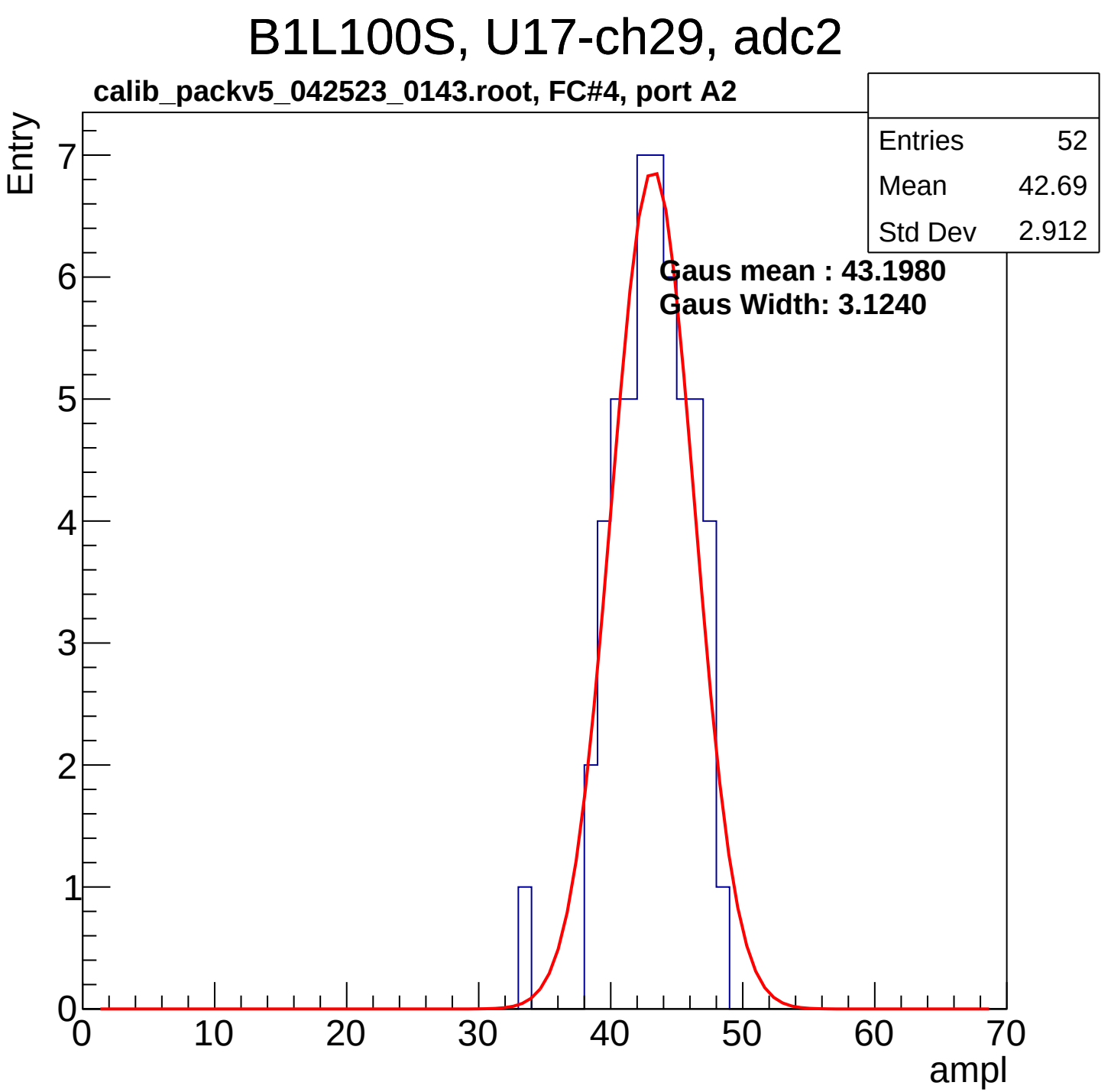

B1L100S, U17-ch28, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 58.69
Std Dev 2.987
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

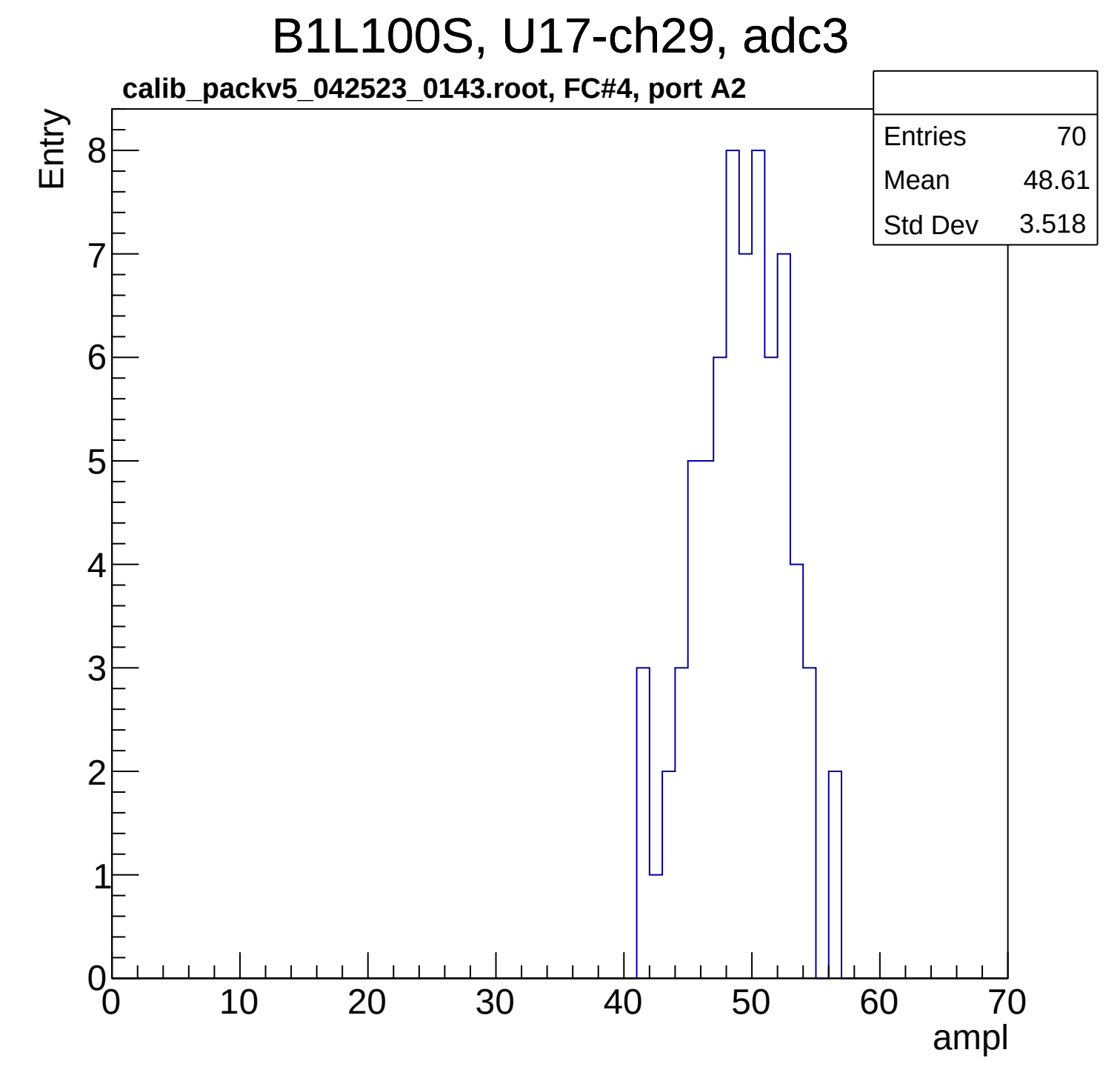

B1L100S, U17-ch28, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 21
Mean 58.48
Std Dev 13.14
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch28, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch29, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 27.89
Std Dev 5.796
Gaus mean : 28.9061
Gaus Width: 3.0391
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch29, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 77
Mean 35.95
Std Dev 3.322
Gaus mean : 36.4830
Gaus Width: 3.3510
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch29, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 52
Mean 42.69
Std Dev 2.912
Gaus mean : 43.1980
Gaus Width: 3.1240
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U17-ch29, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 48.61
Std Dev 3.518
Entry
ampl
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2
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60
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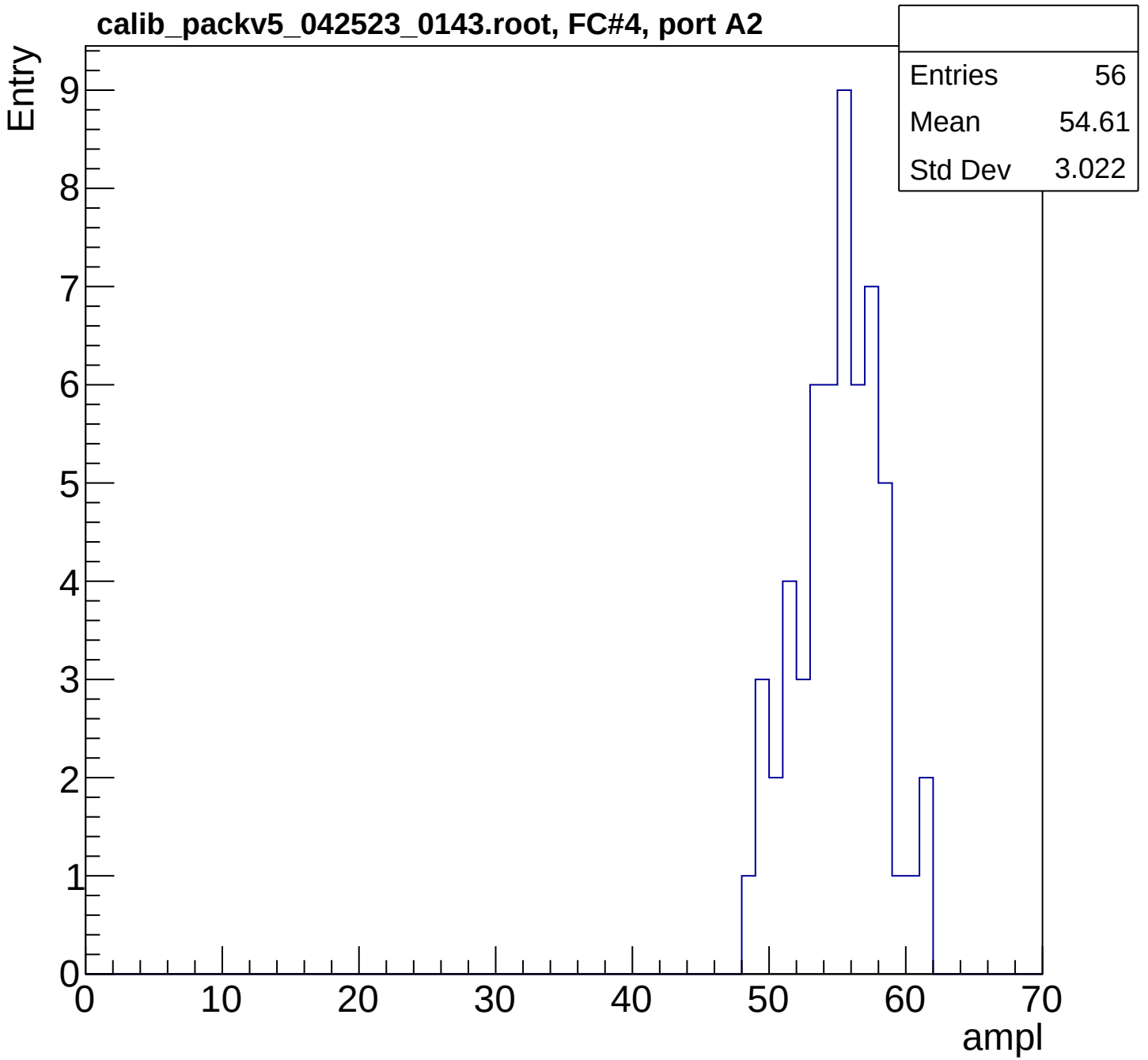
B1L100S, U17-ch29, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 54.61
Std Dev 3.022
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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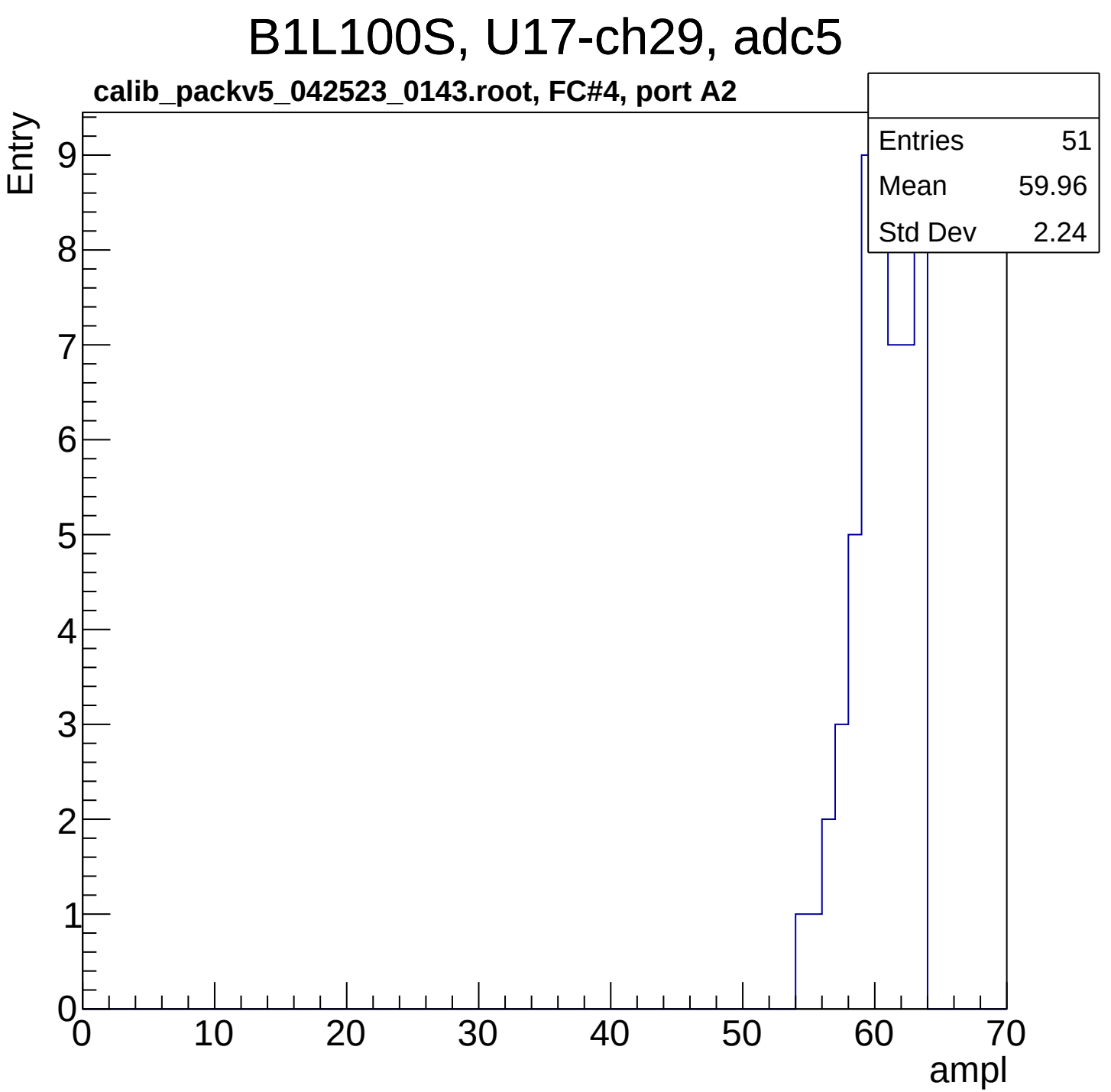
B1L100S, U17-ch29, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 59.96
Std Dev 2.24
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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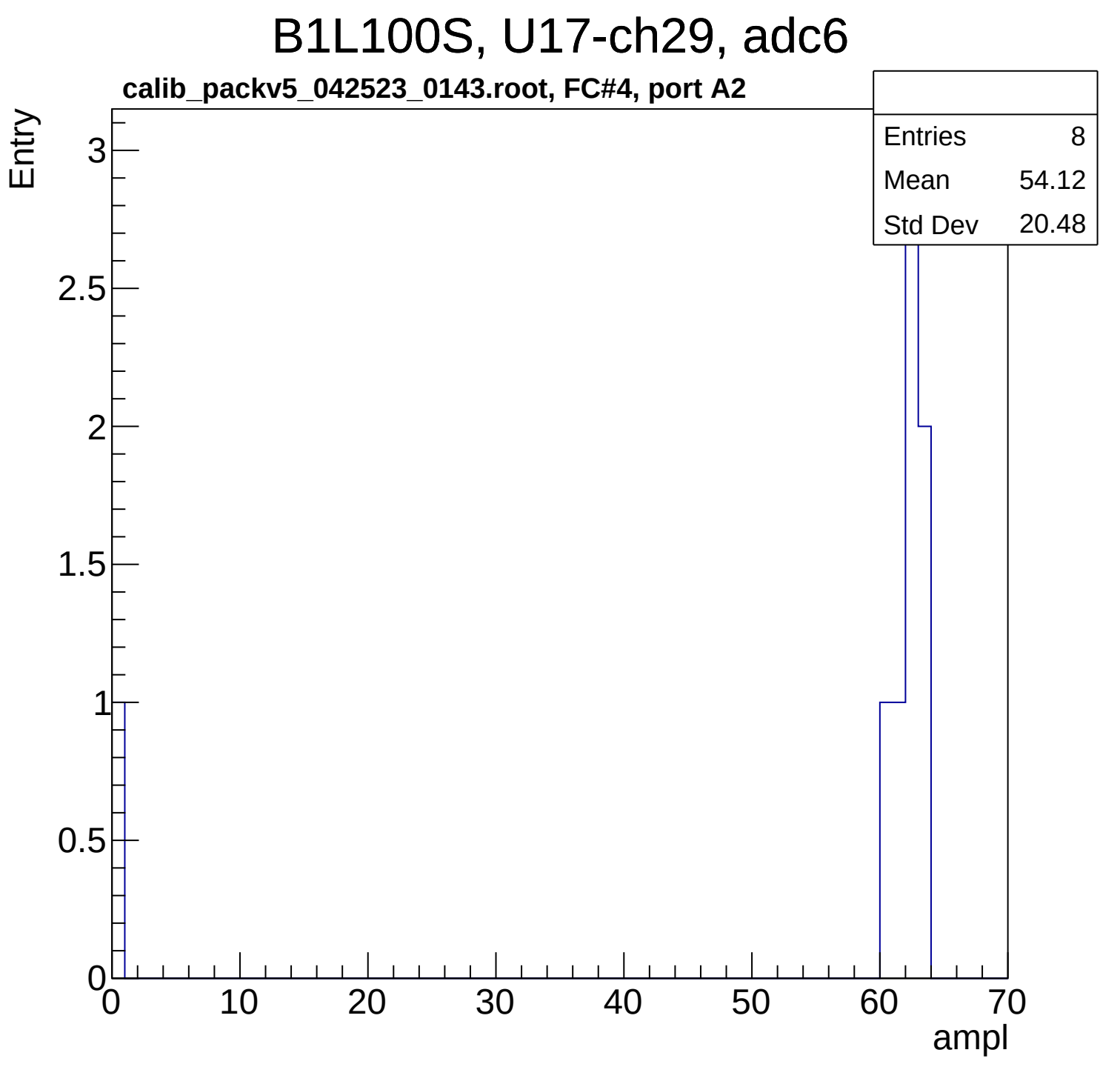
B1L100S, U17-ch29, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 8
Mean 54.12
Std Dev 20.48
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
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40
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60
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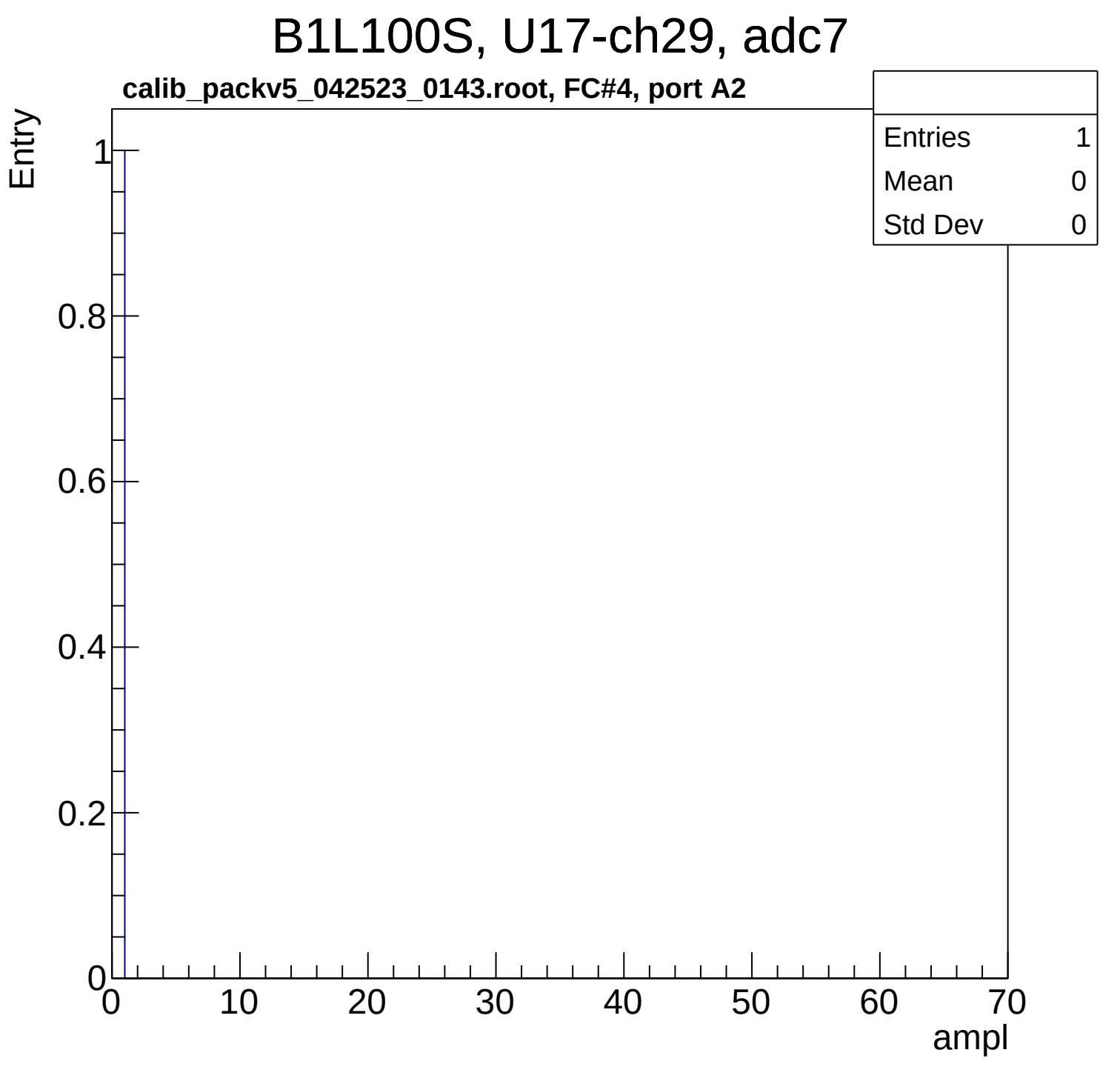
B1L100S, U17-ch29, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
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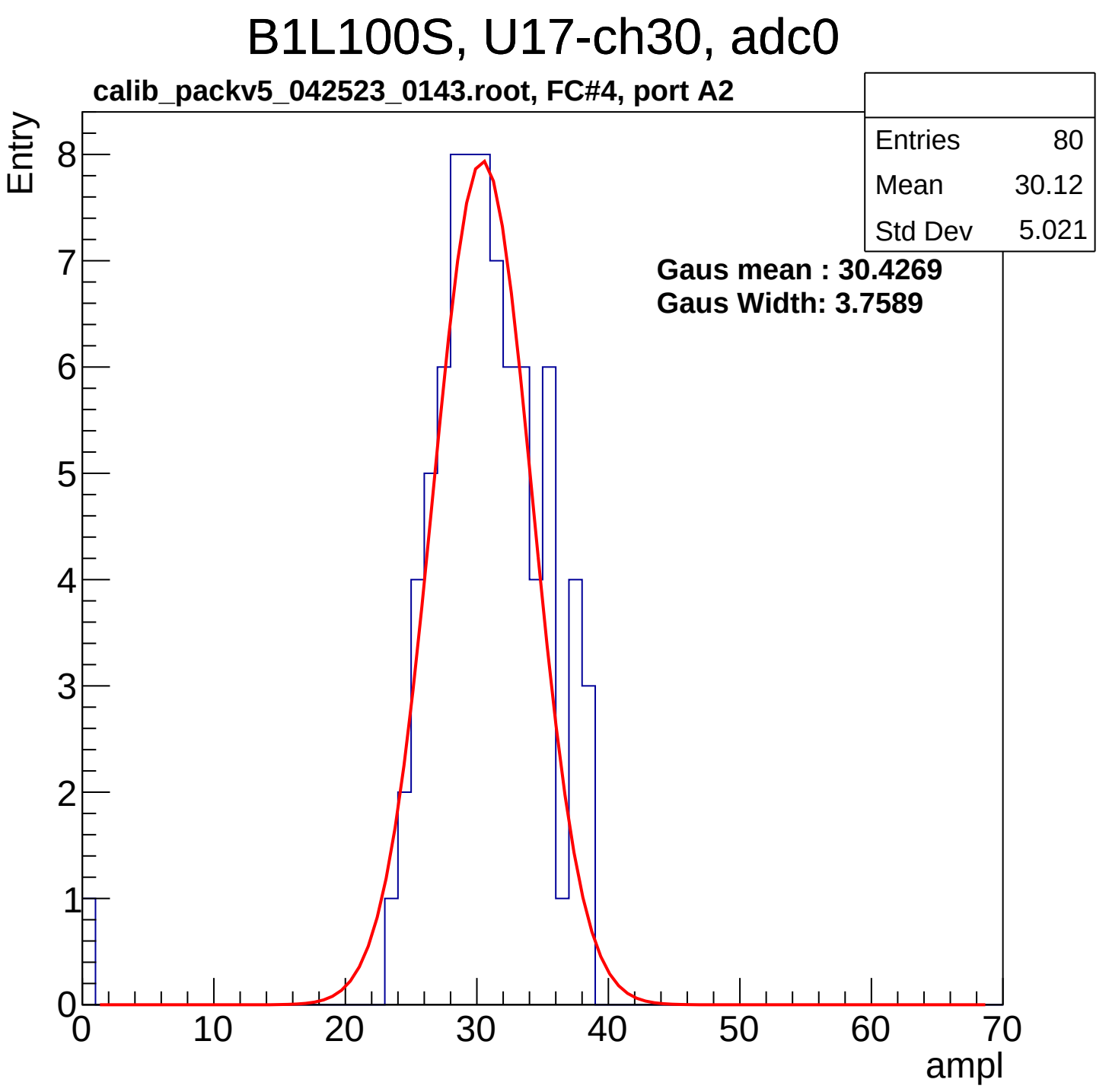
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch30, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 80
Mean 30.12
Std Dev 5.021
Gaus mean : 30.4269
Gaus Width: 3.7589
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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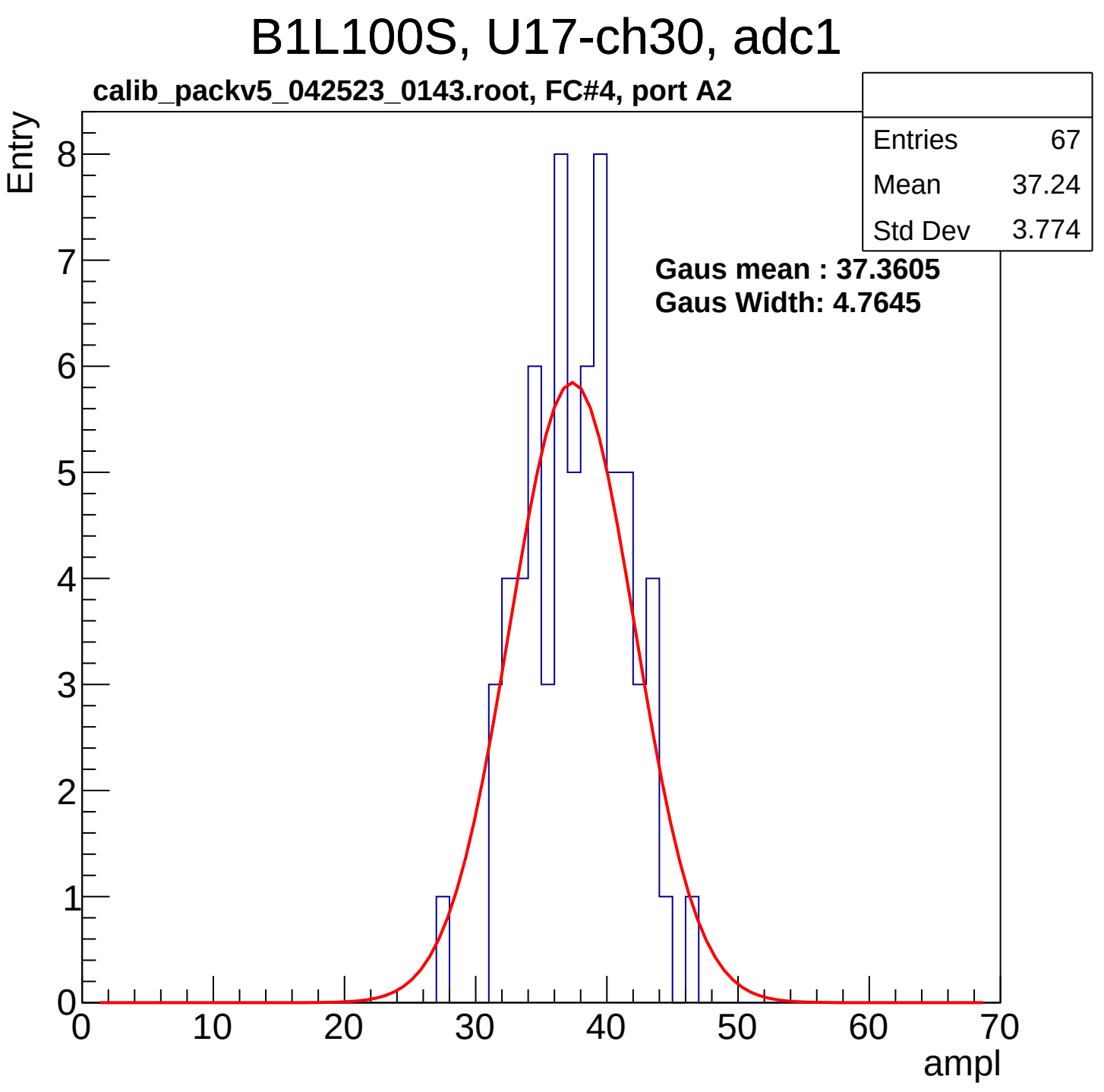
40
50
60
70


B1L100S, U17-ch30, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 37.24
Std Dev 3.774
Gaus mean : 37.3605
Gaus Width: 4.7645
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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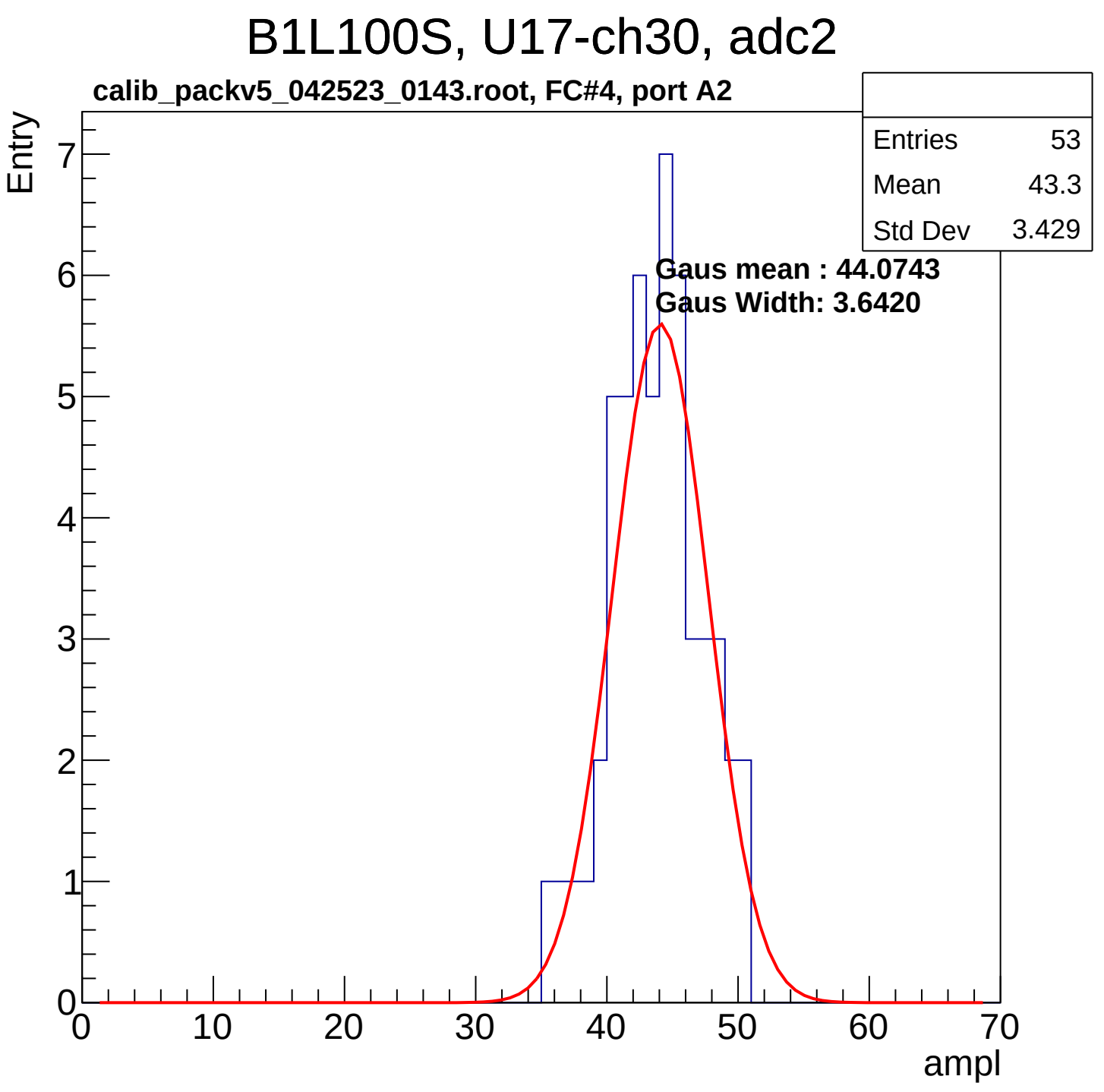
B1L100S, U17-ch30, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 43.3
Std Dev 3.429
Gaus mean : 44.0743
Gaus Width: 3.6420
Entry
ampl
0
1
2
3
4
5
6
7
0
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40
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60
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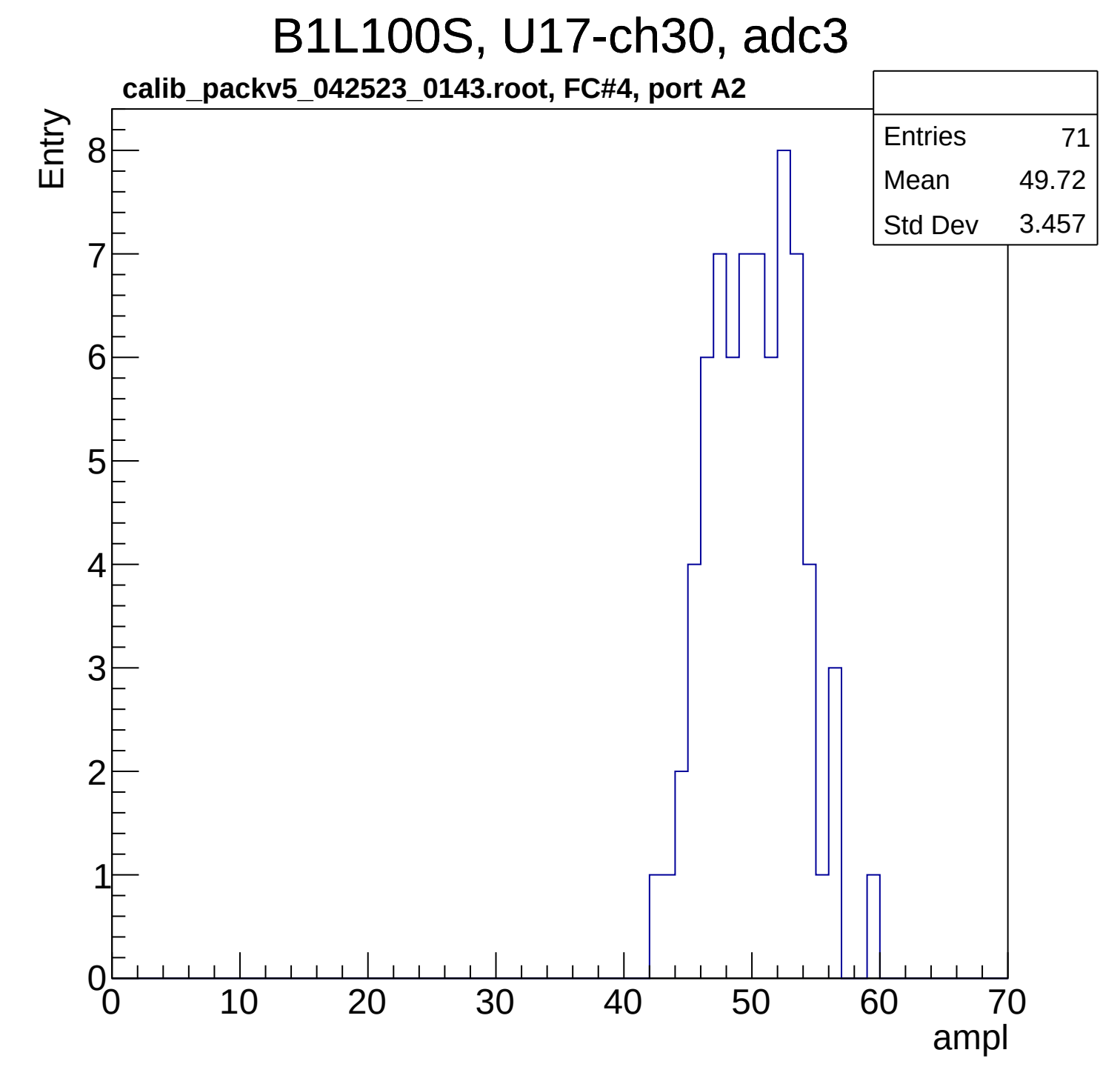
B1L100S, U17-ch30, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 49.72
Std Dev 3.457
Entry
ampl
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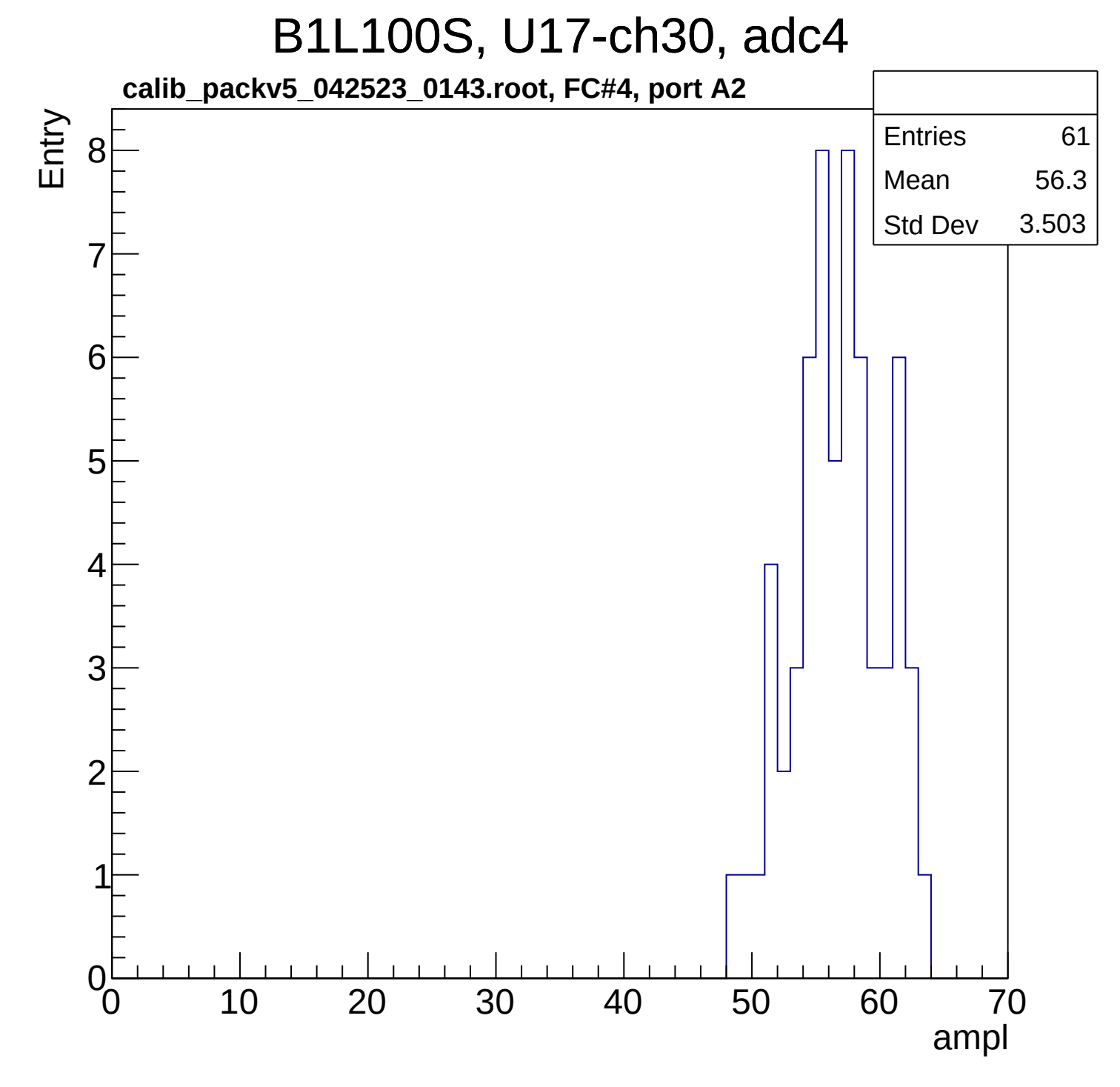
B1L100S, U17-ch30, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 56.3
Std Dev 3.503
Entry
ampl
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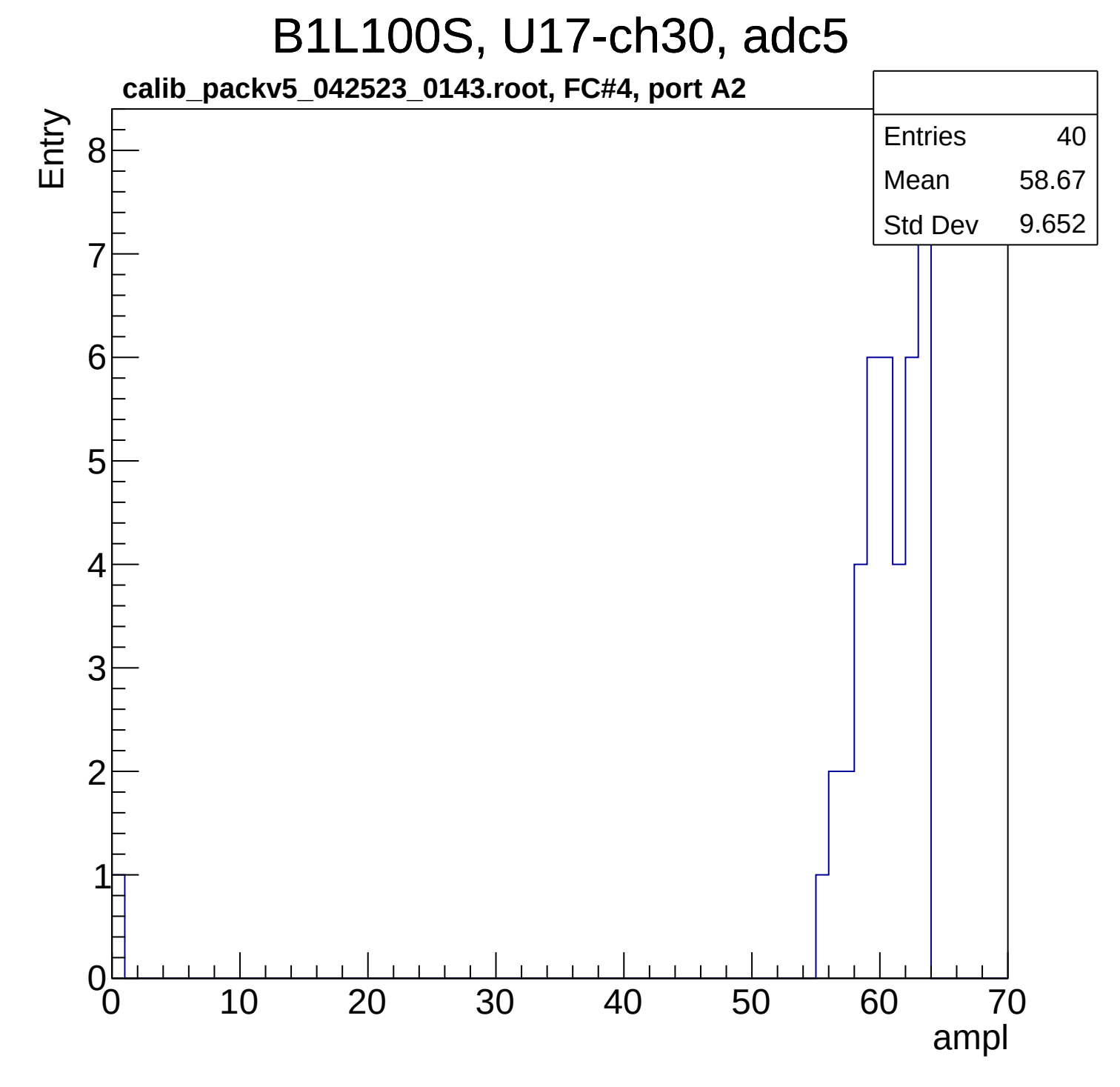
B1L100S, U17-ch30, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 40
Mean 58.67
Std Dev 9.652
Entry
ampl
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4
5
6
7
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50
60
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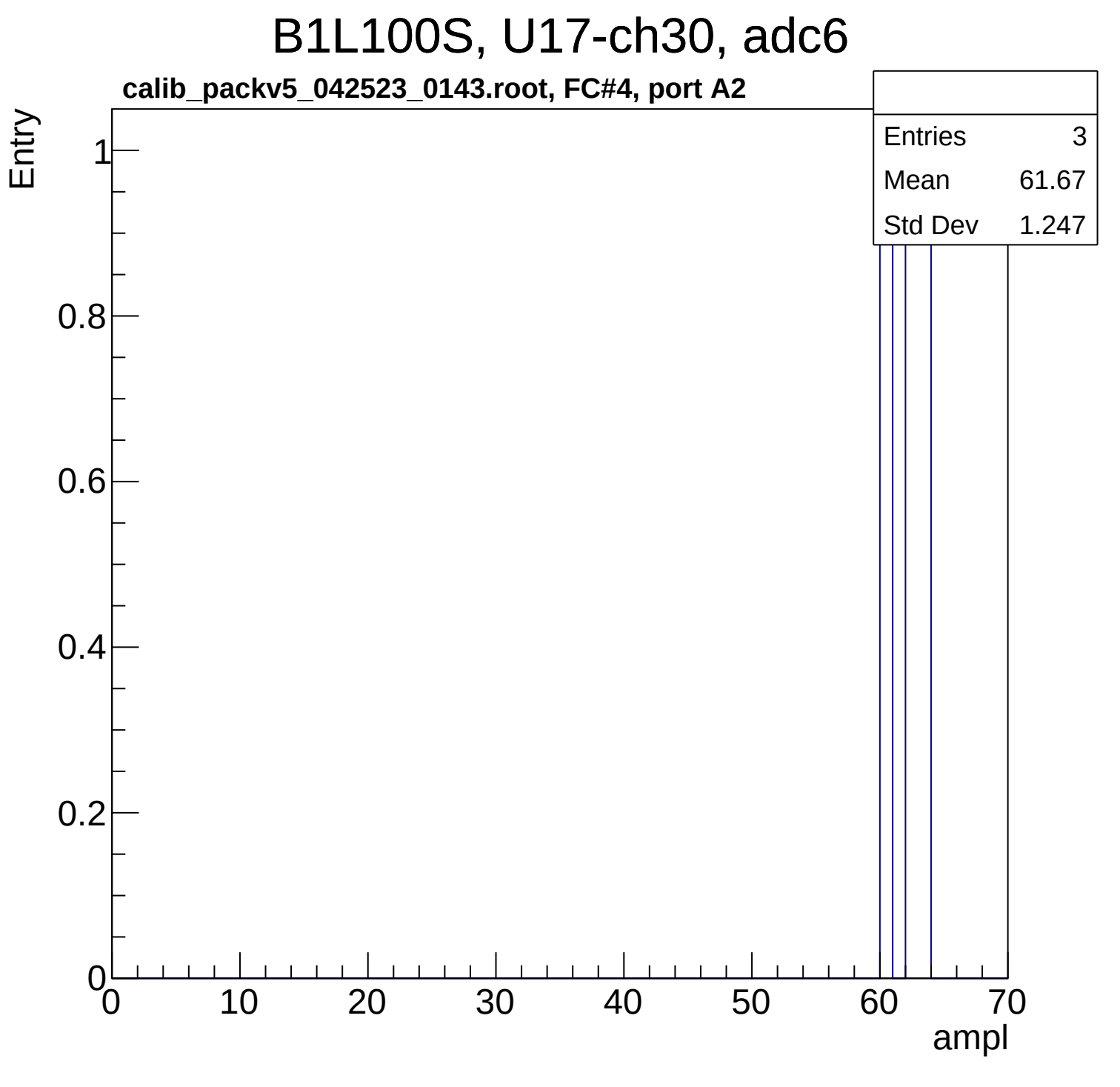
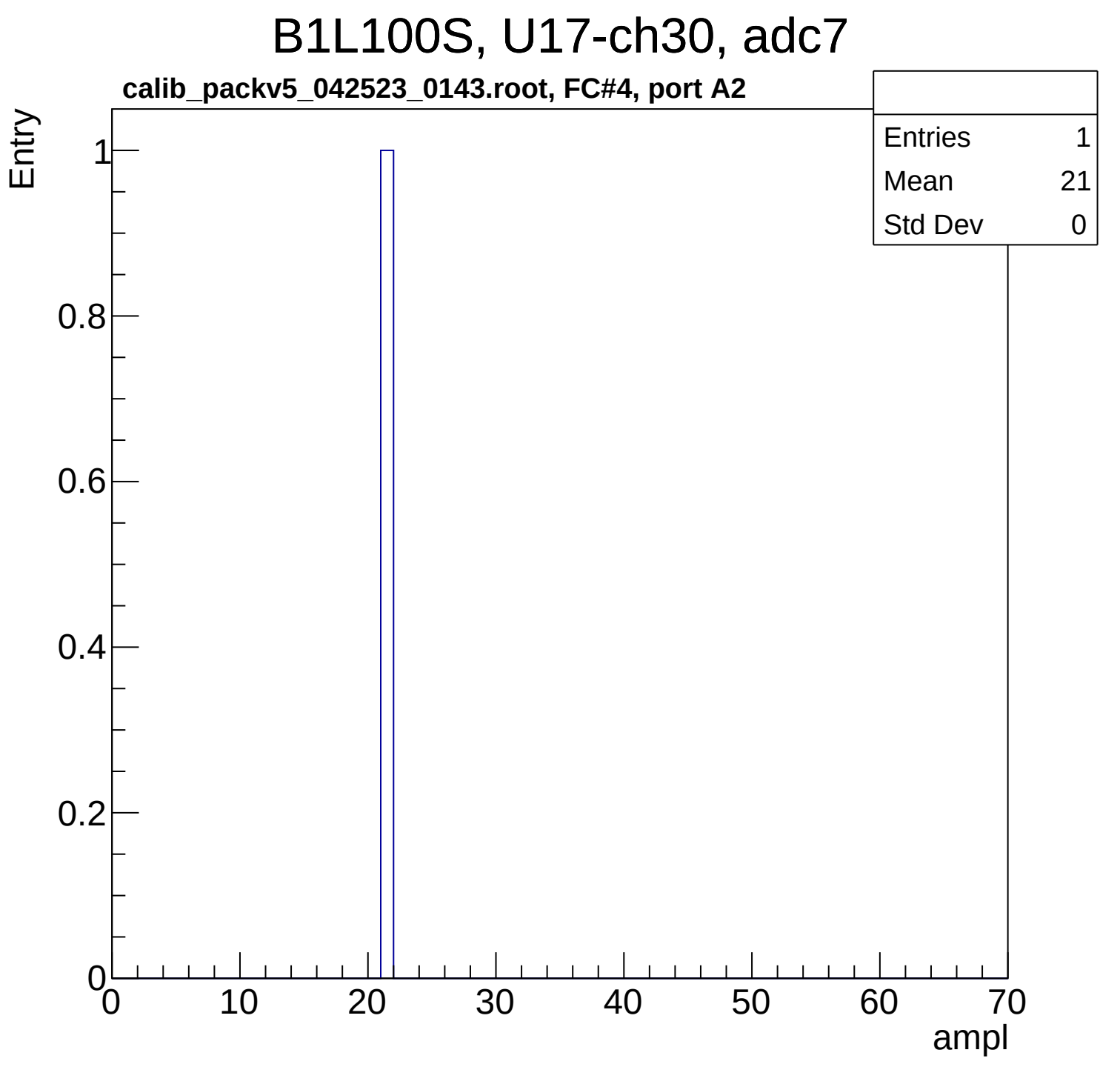

B1L100S, U17-ch30, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 61.67
Std Dev 1.247
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch30, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 21
Std Dev 0
Entry
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0.6
0.4
0.2
0
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10
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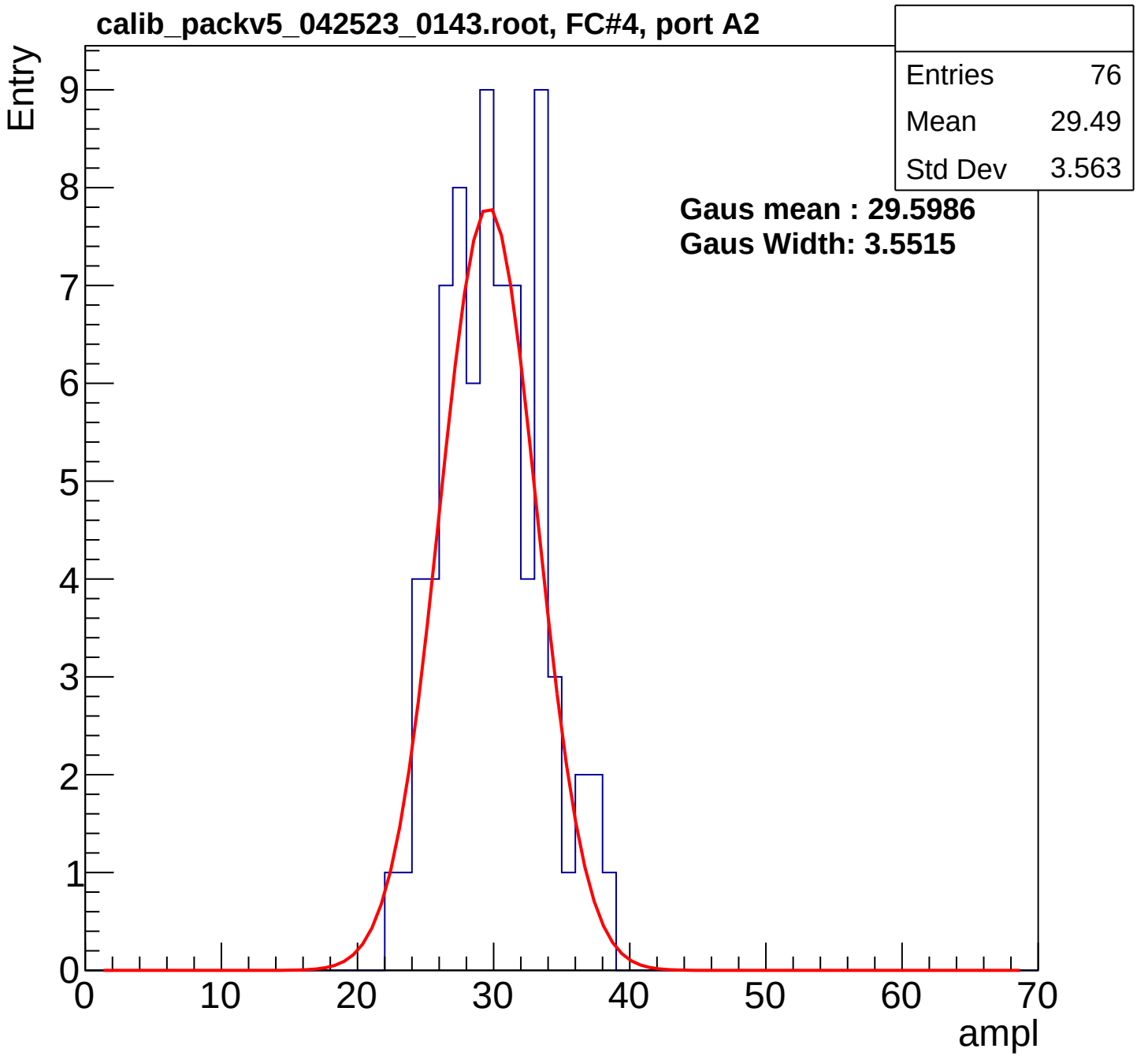
50
60
70
ampl


B1L100S, U17-ch31, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 76
Mean 29.49
Std Dev 3.563
Gaus mean : 29.5986
Gaus Width: 3.5515
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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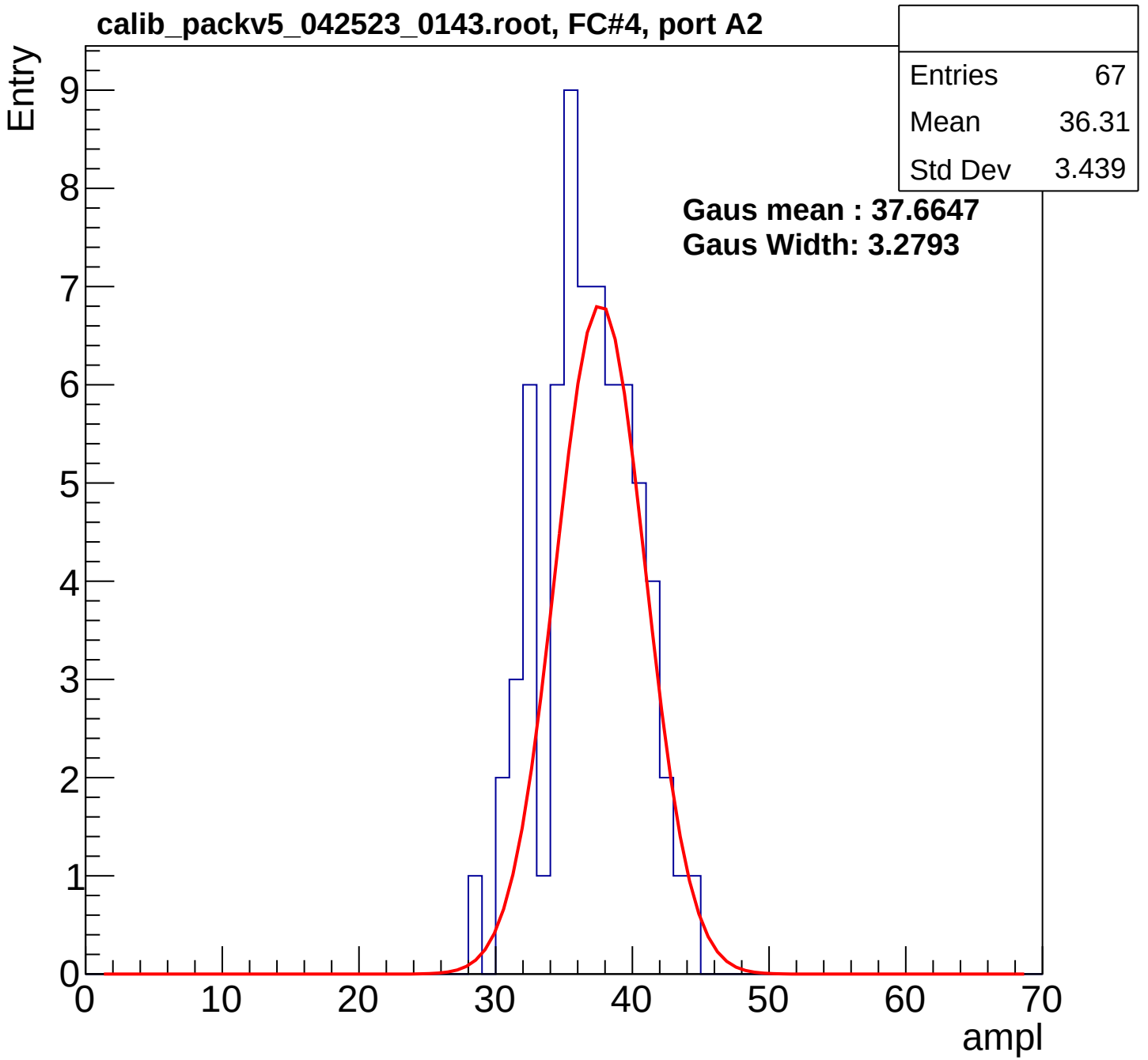
B1L100S, U17-ch31, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 36.31
Std Dev 3.439
Gaus mean : 37.6647
Gaus Width: 3.2793
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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30
40
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60
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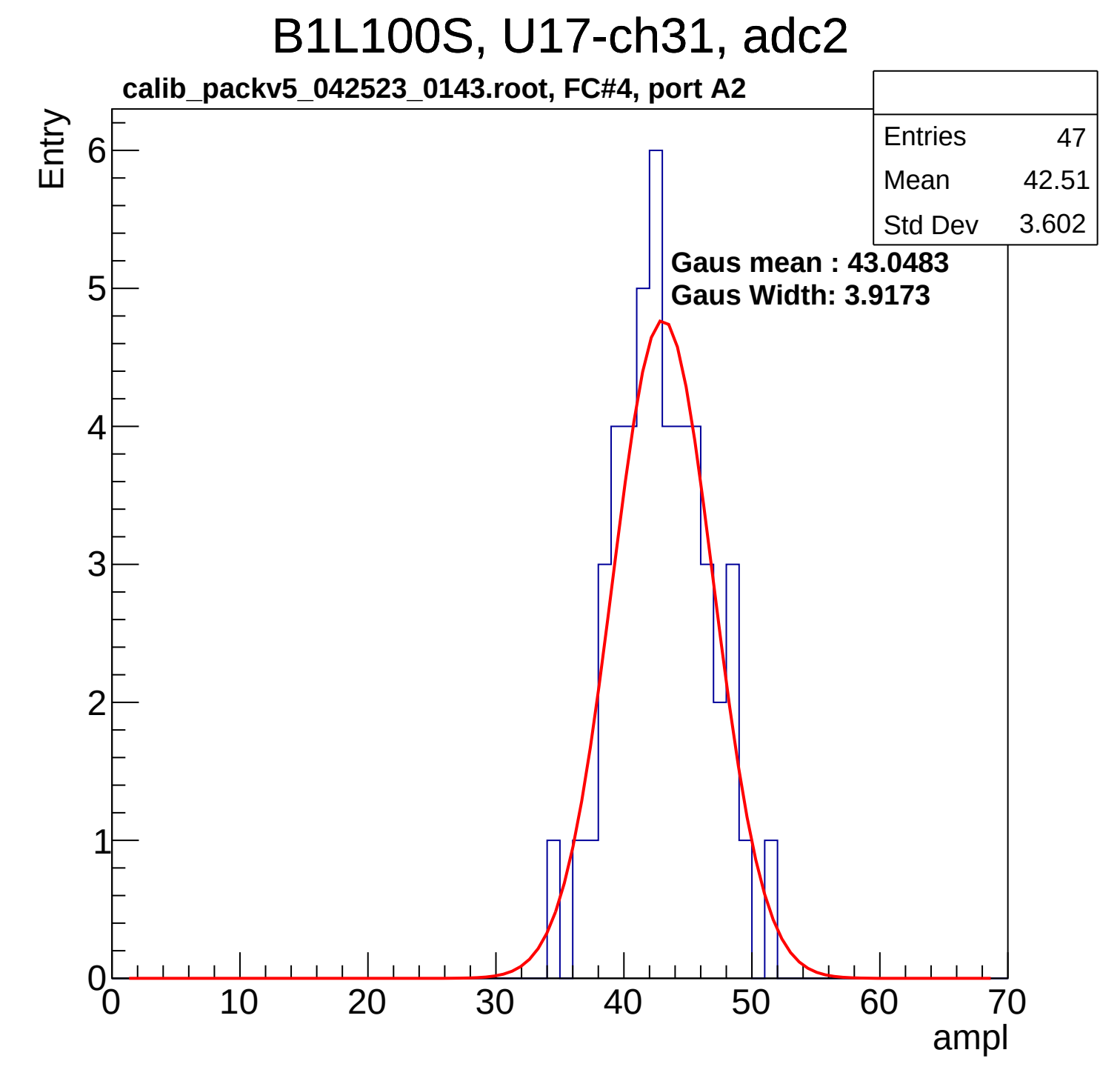
B1L100S, U17-ch31, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 47
Mean 42.51
Std Dev 3.602
Gaus mean : 43.0483
Gaus Width: 3.9173
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
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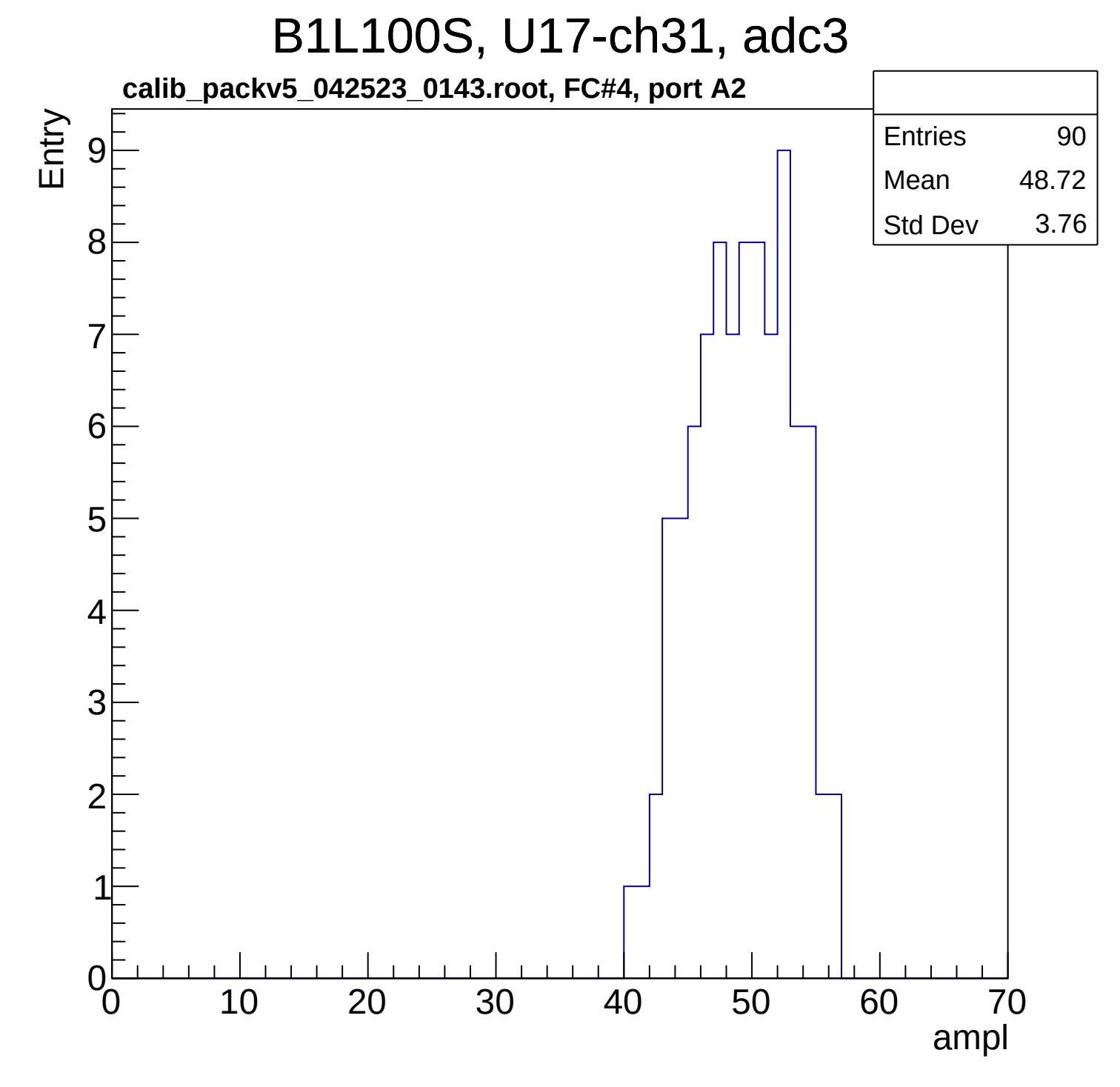
B1L100S, U17-ch31, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 90
Mean 48.72
Std Dev 3.76
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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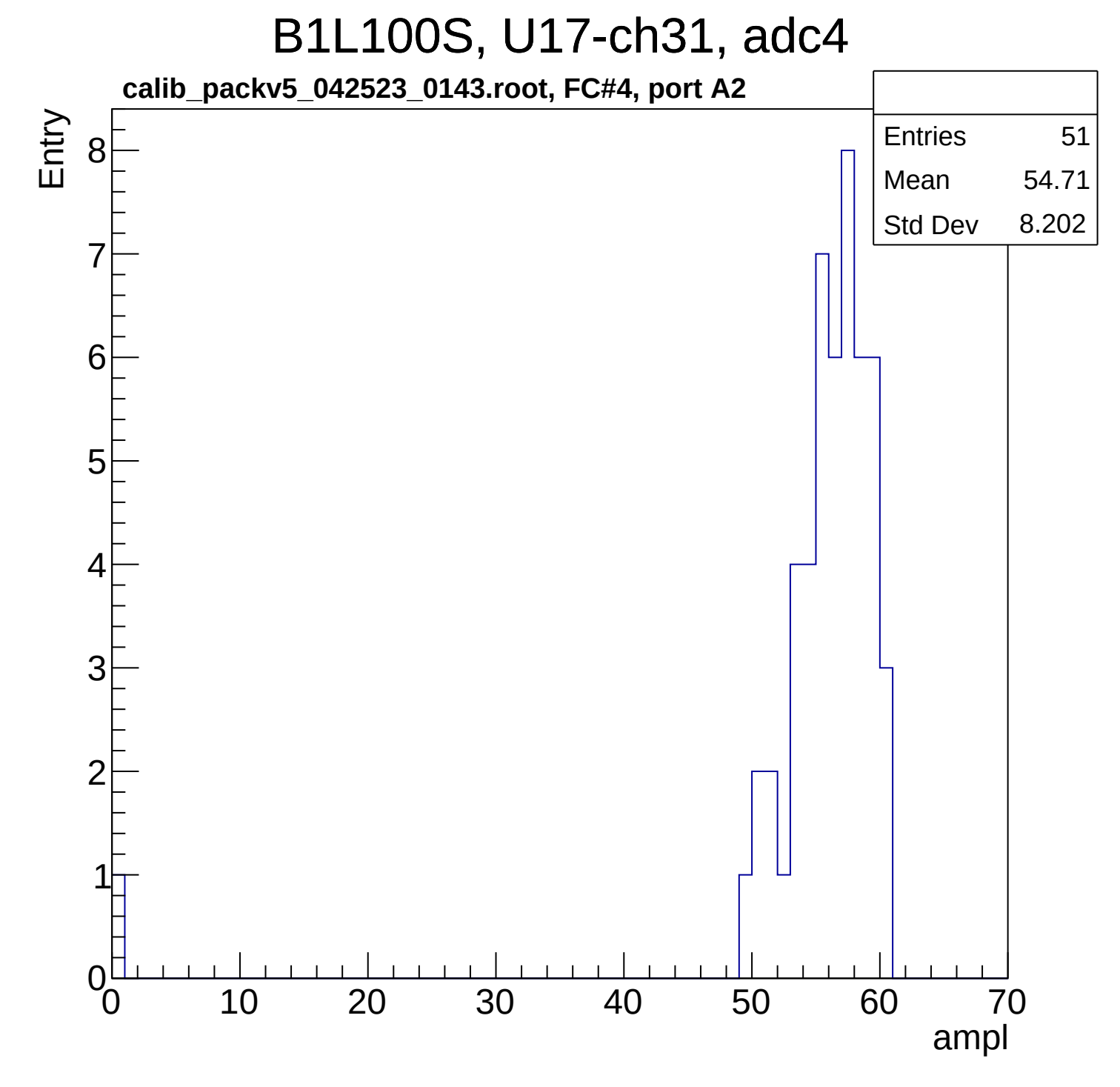
B1L100S, U17-ch31, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 54.71
Std Dev 8.202
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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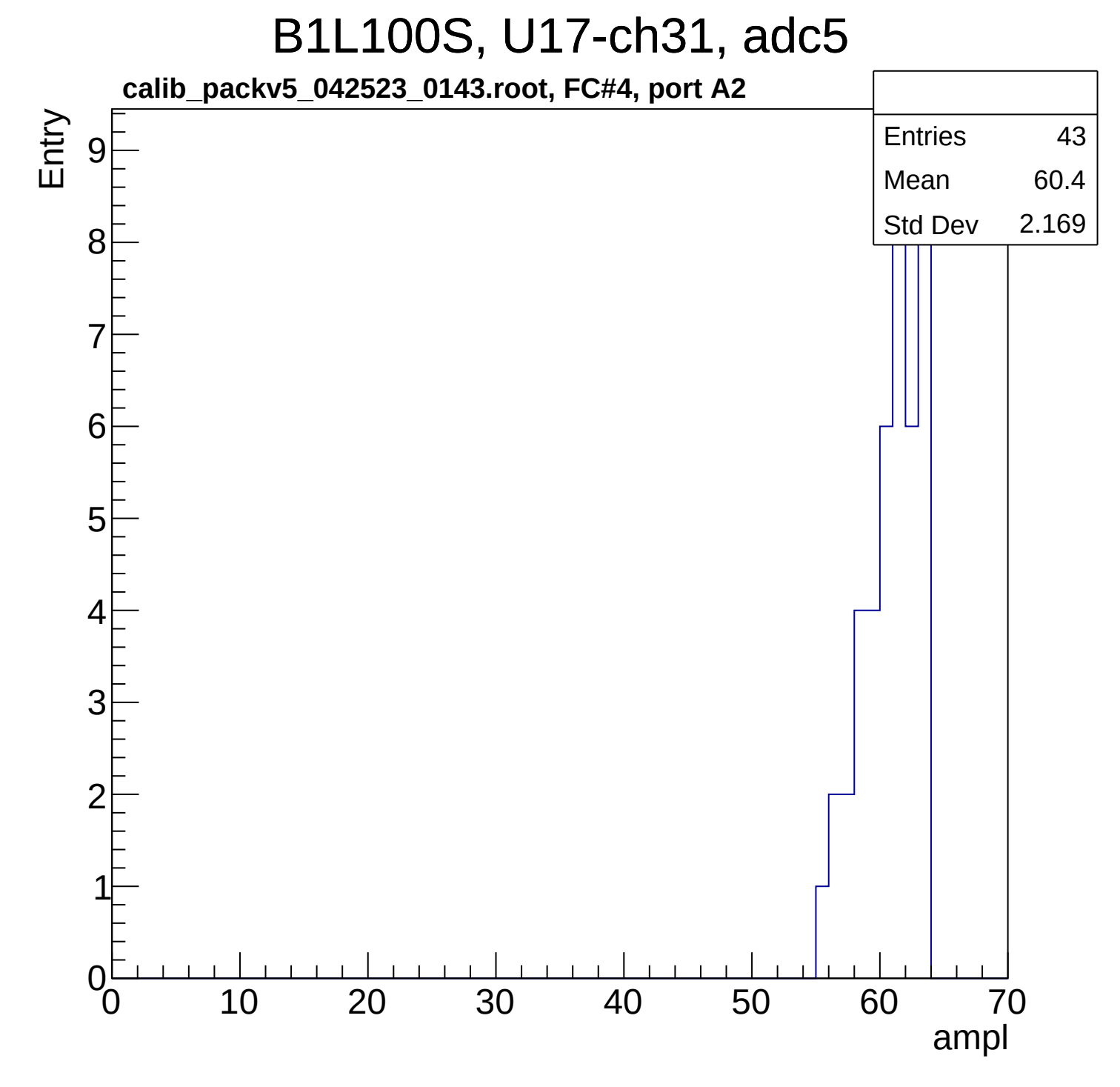
B1L100S, U17-ch31, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 43
Mean 60.4
Std Dev 2.169
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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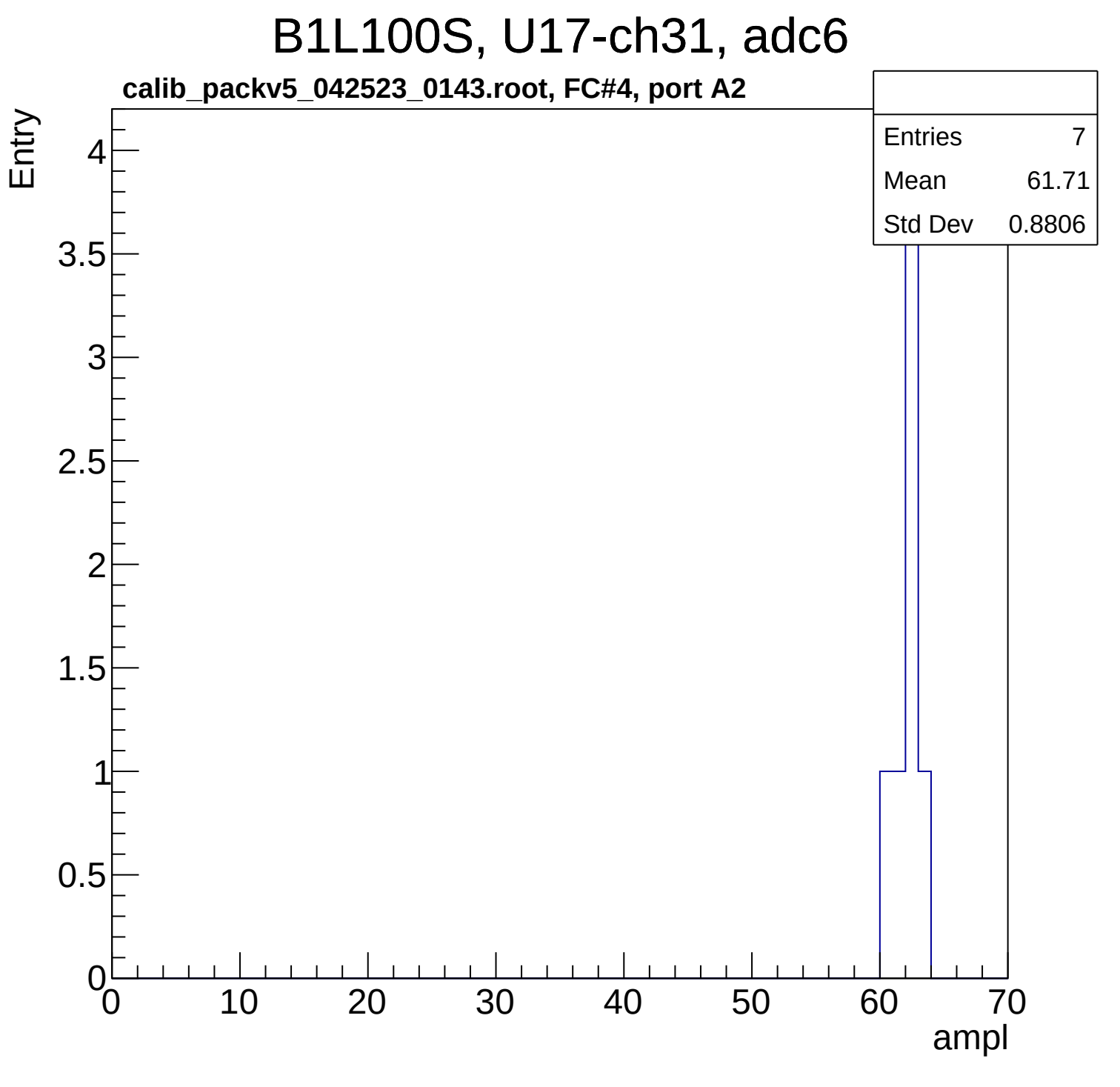
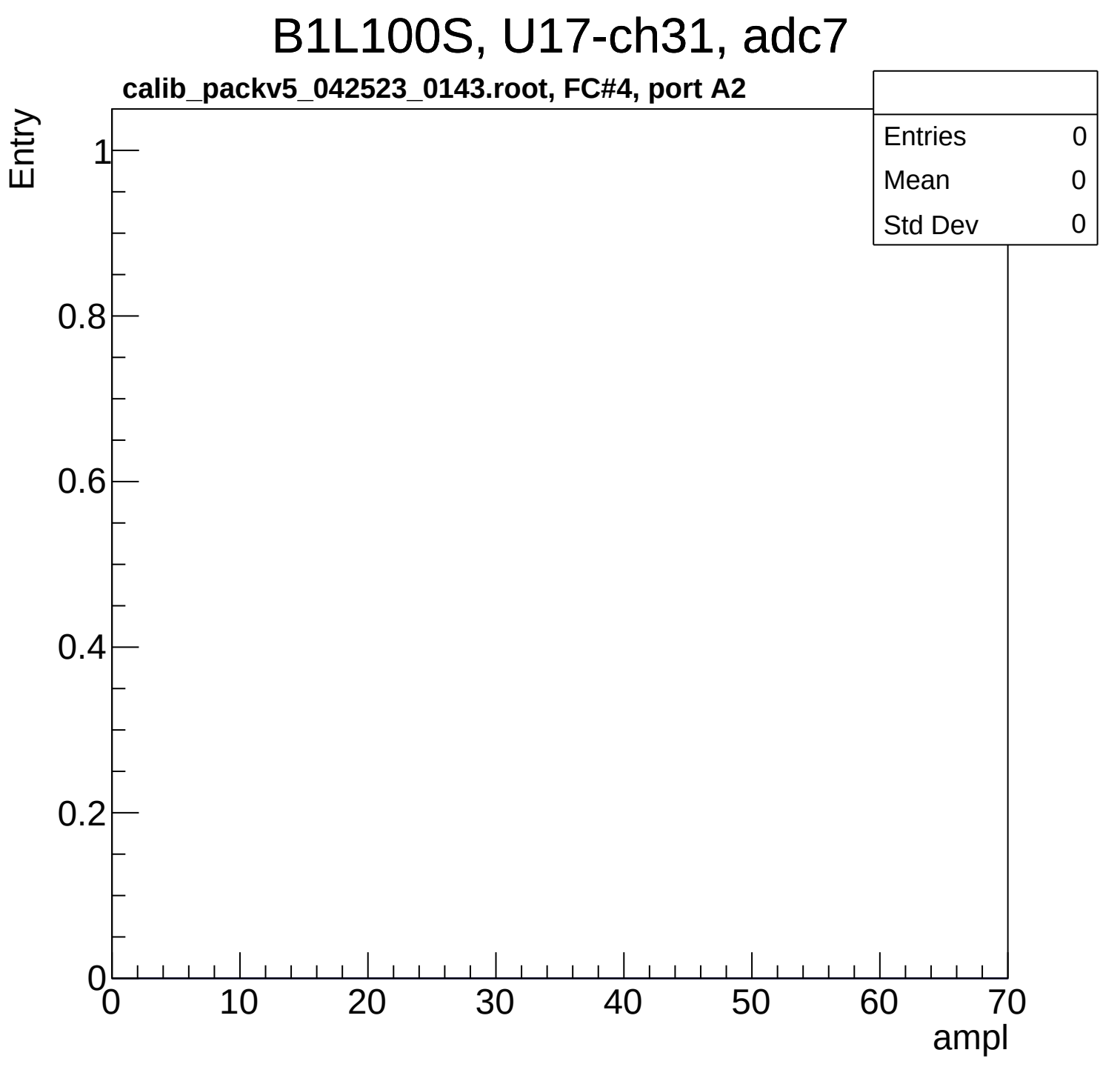
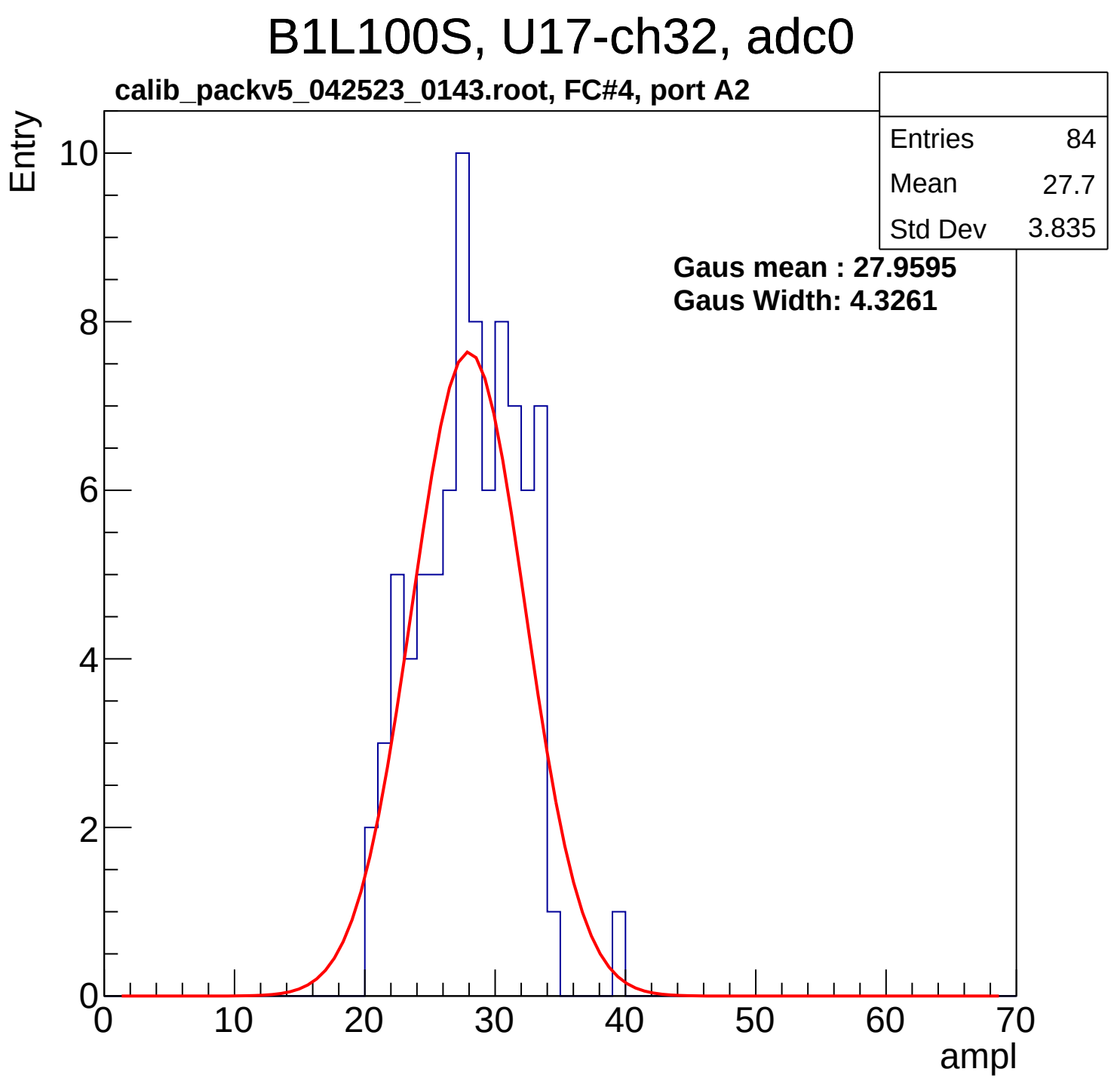
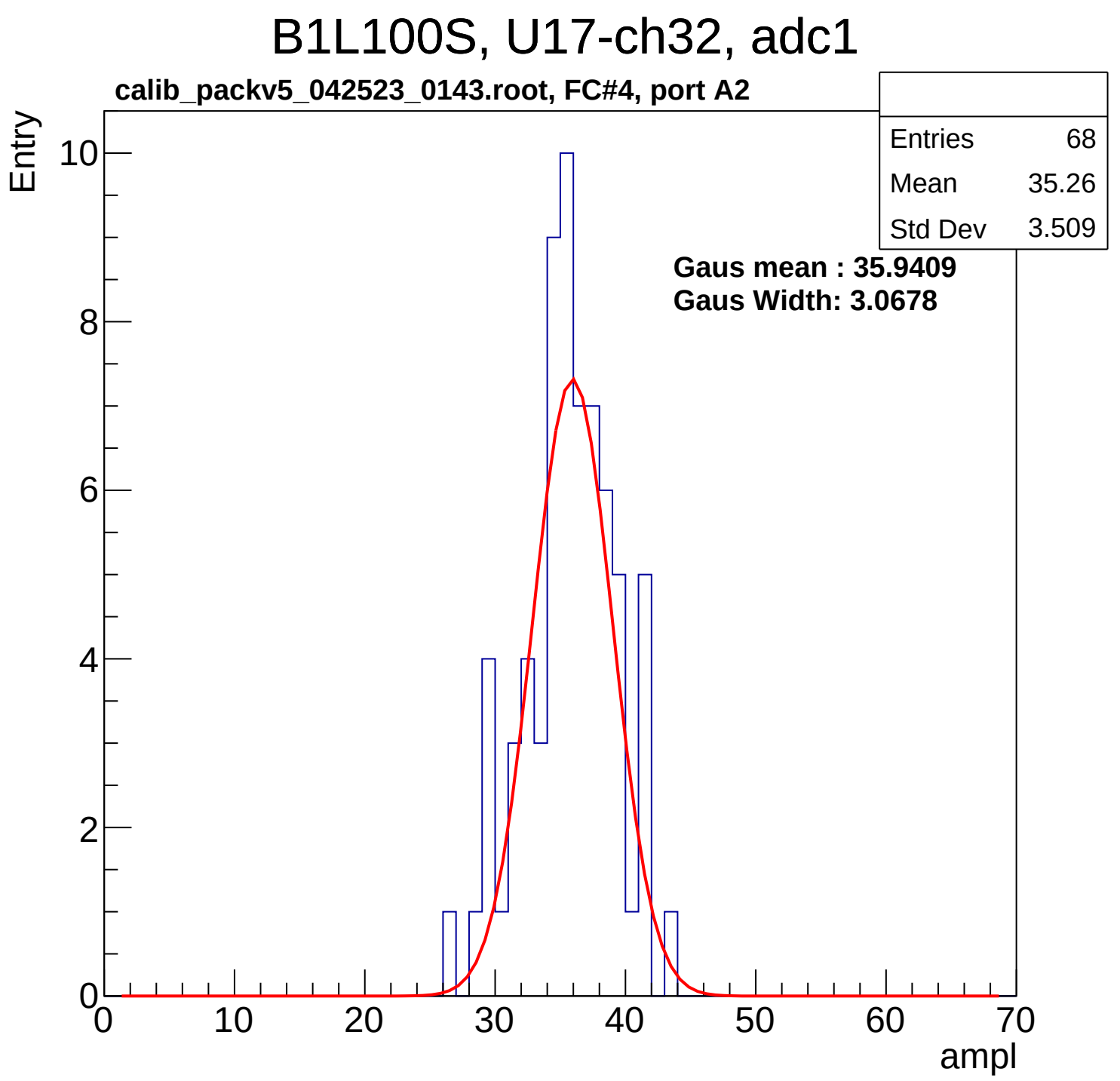
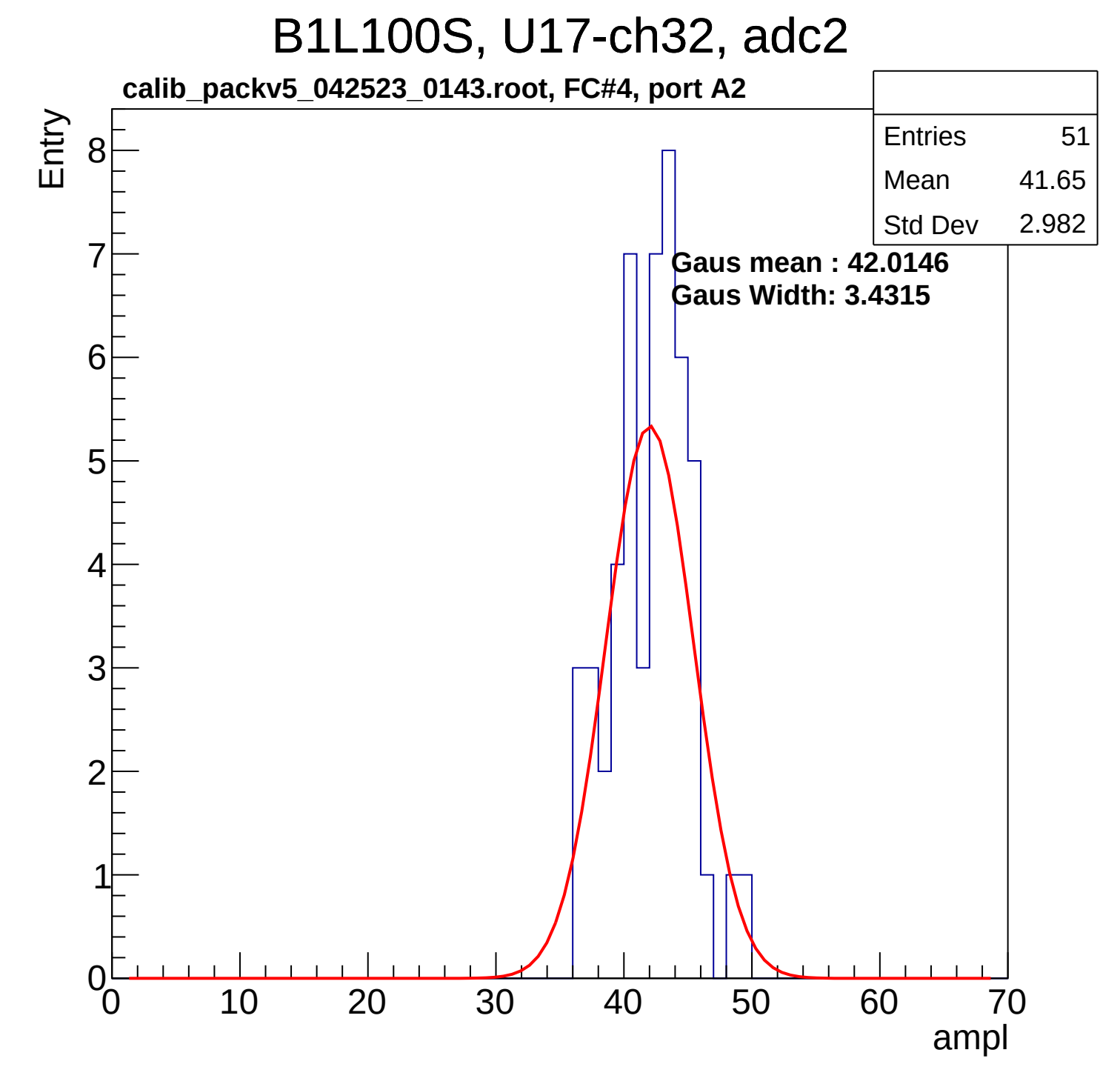
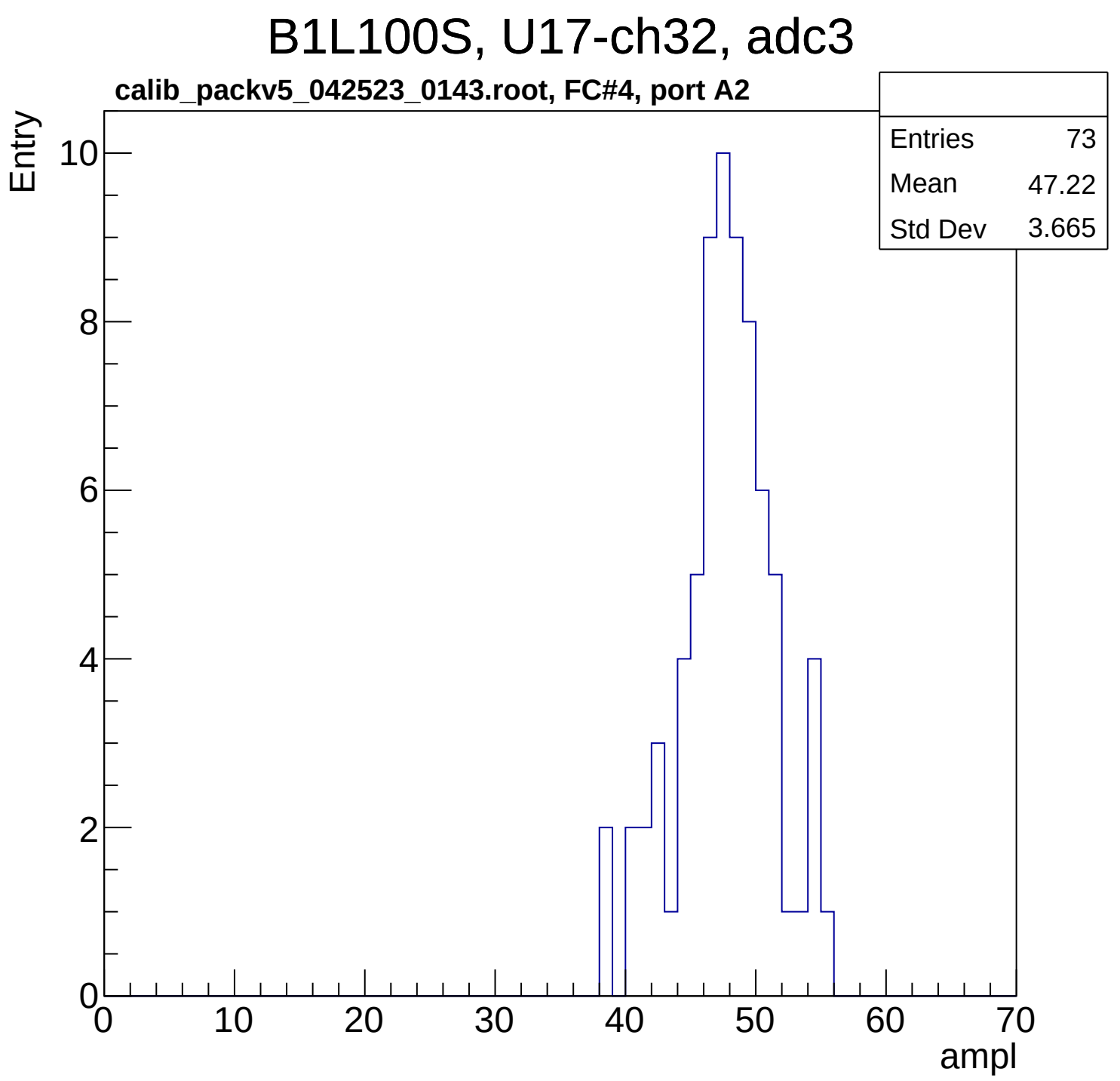

B1L100S, U17-ch31, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 7
Mean 61.71
Std Dev 0.8806
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

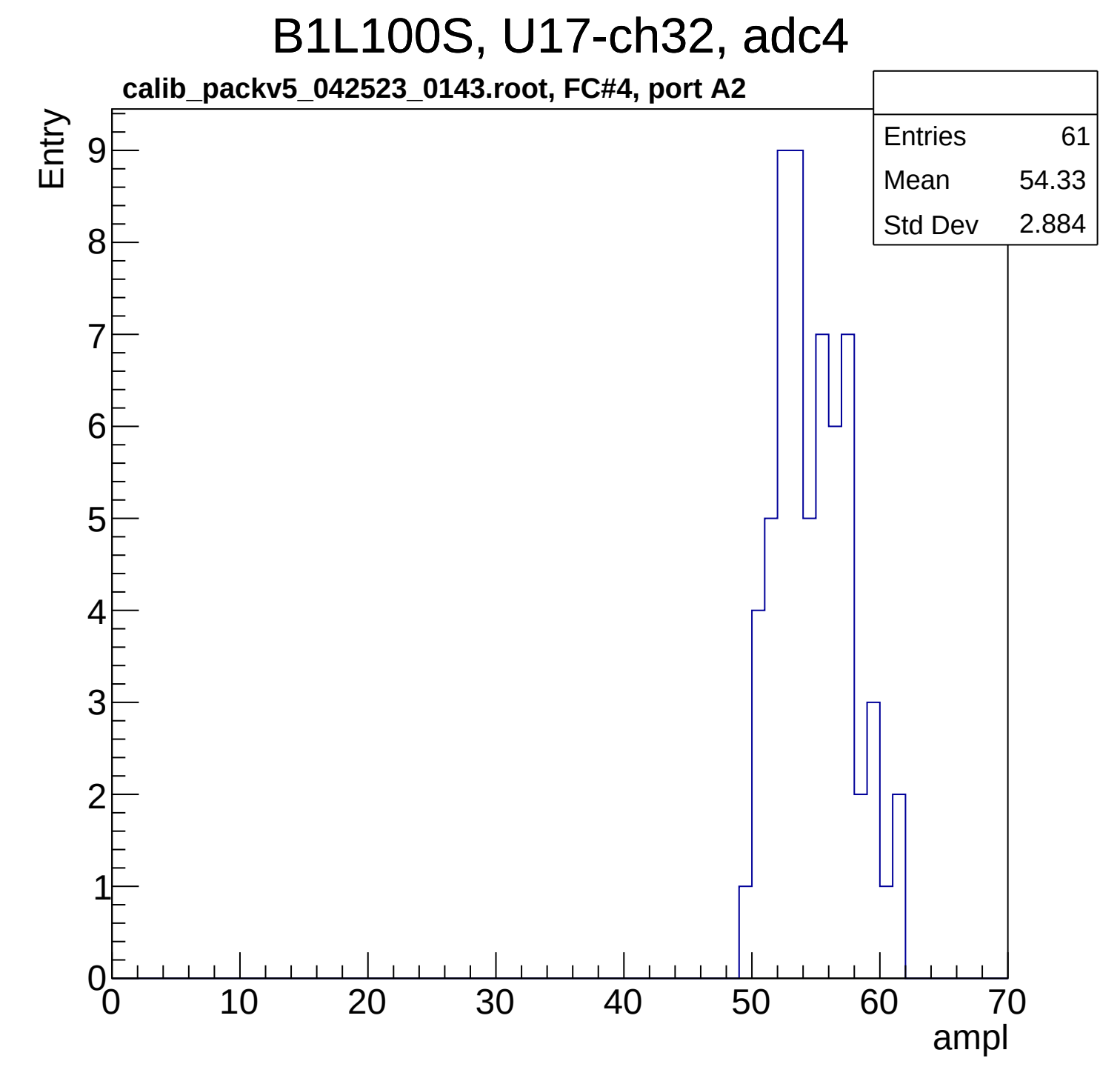

B1L100S, U17-ch31, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

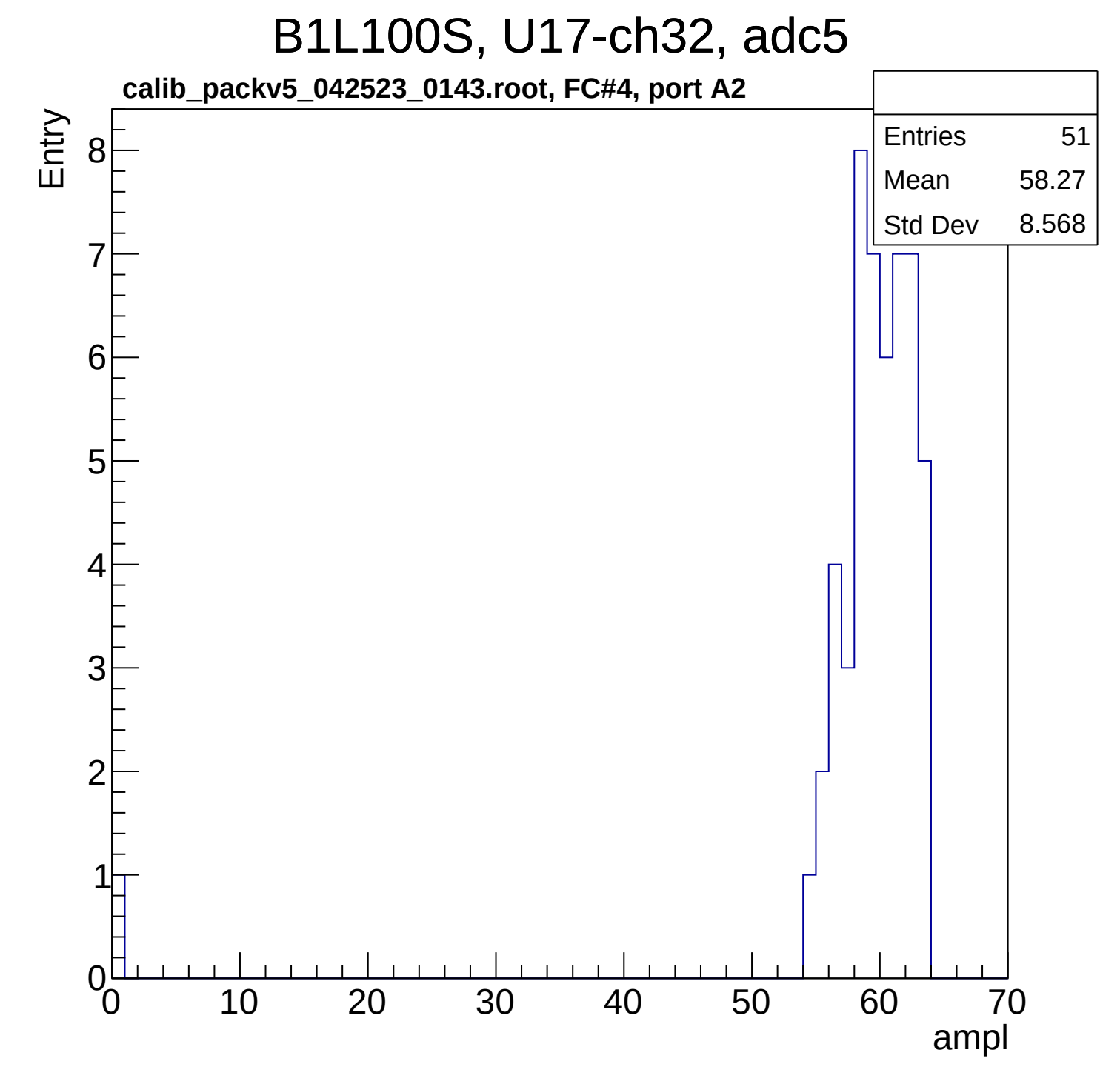

B1L100S, U17-ch32, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 84
Mean 27.7
Std Dev 3.835
Gaus mean : 27.9595
Gaus Width: 4.3261
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

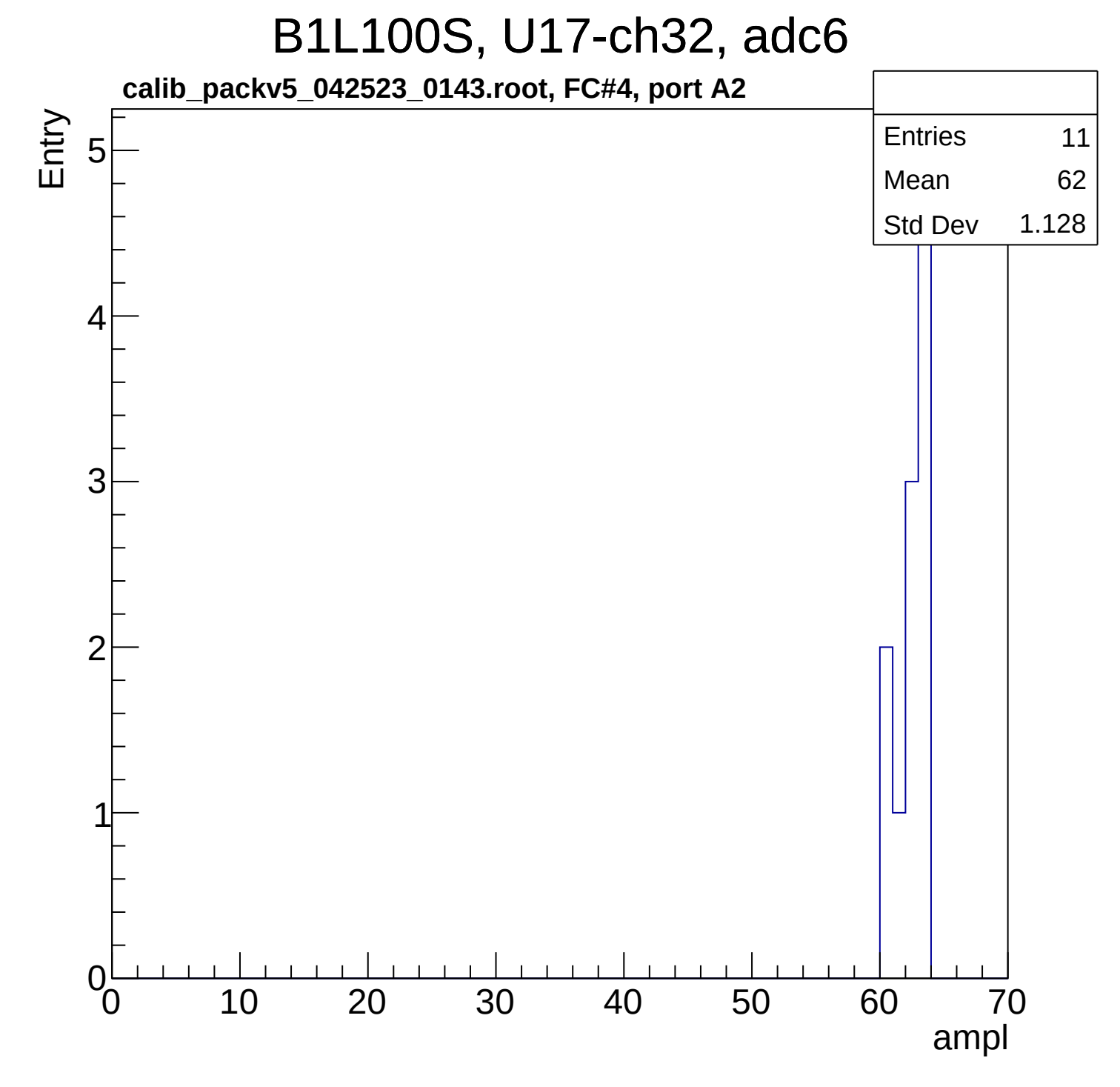

B1L100S, U17-ch32, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 35.26
Std Dev 3.509
Gaus mean : 35.9409
Gaus Width: 3.0678
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

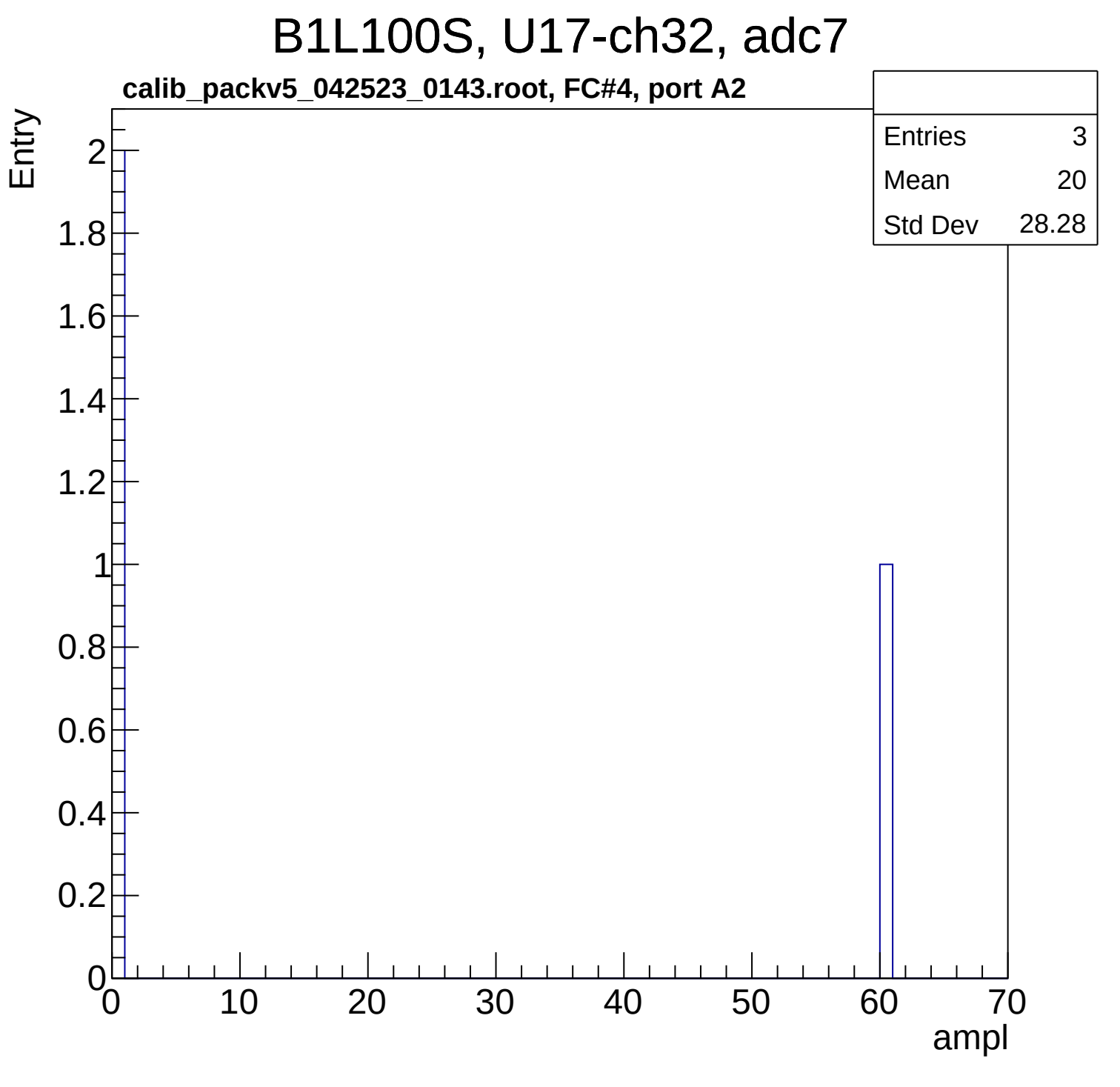

B1L100S, U17-ch32, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 41.65
Std Dev 2.982
Gaus mean : 42.0146
Gaus Width: 3.4315
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

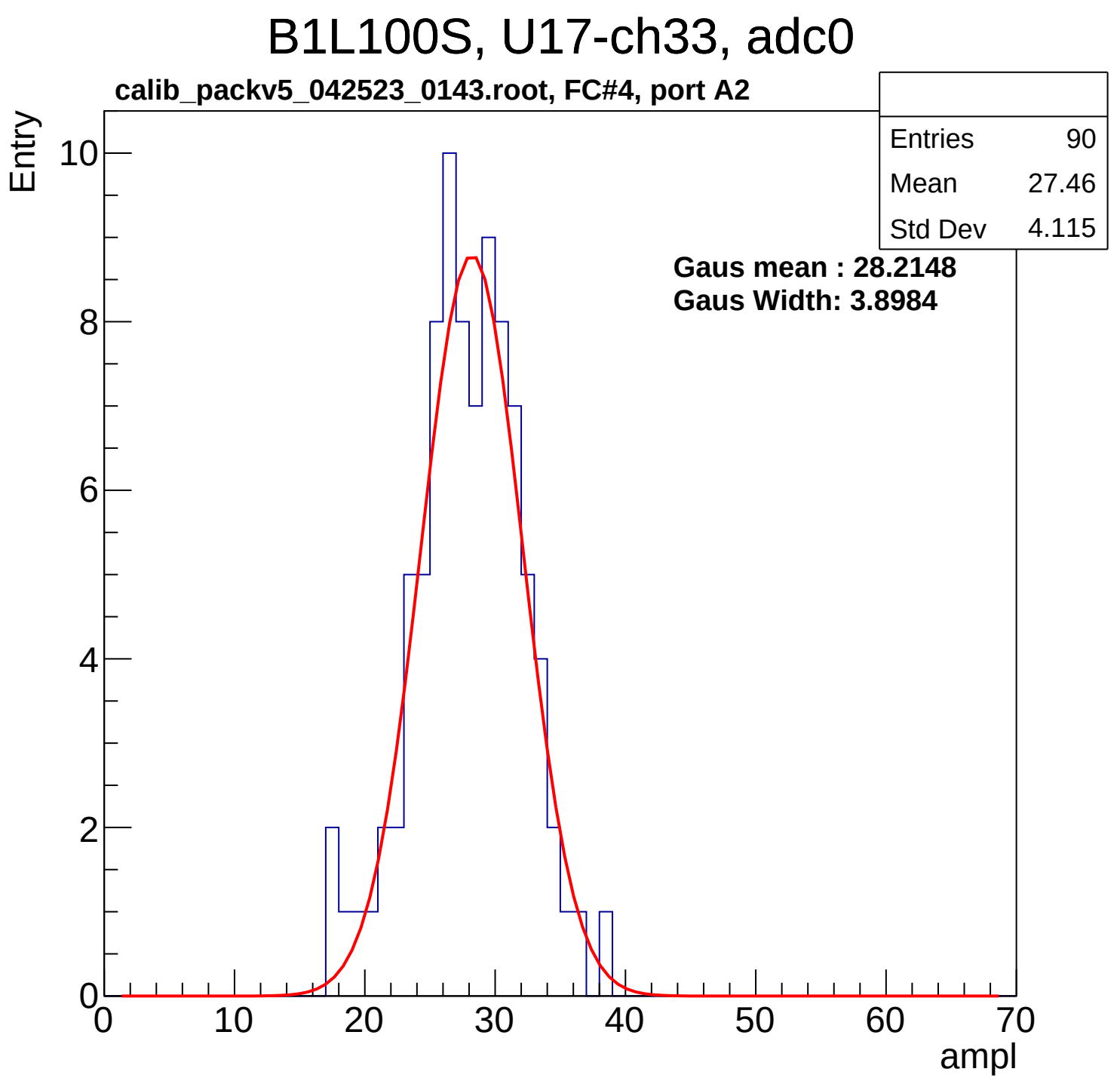

B1L100S, U17-ch32, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 47.22
Std Dev 3.665
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

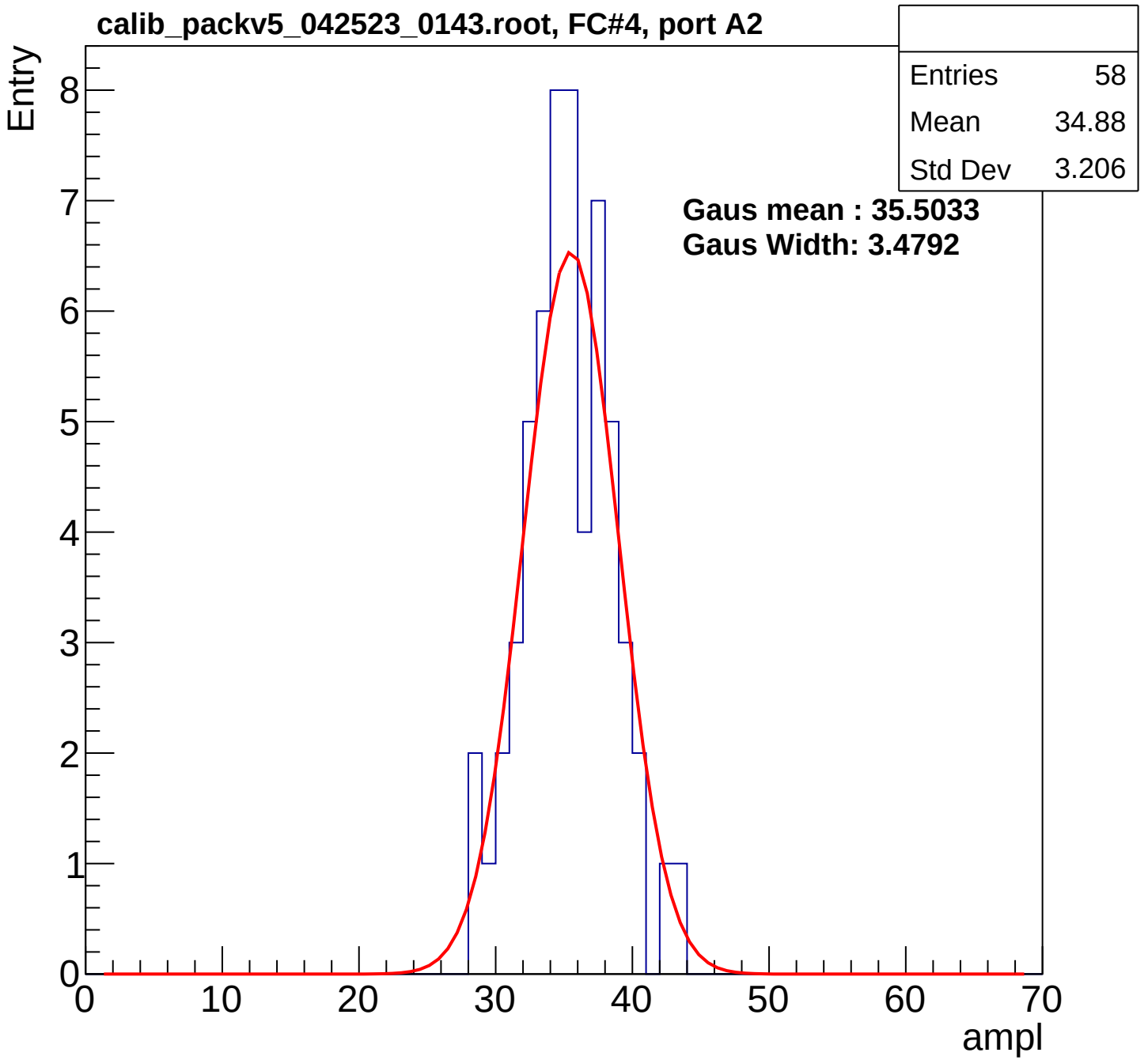

B1L100S, U17-ch32, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 54.33
Std Dev 2.884
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

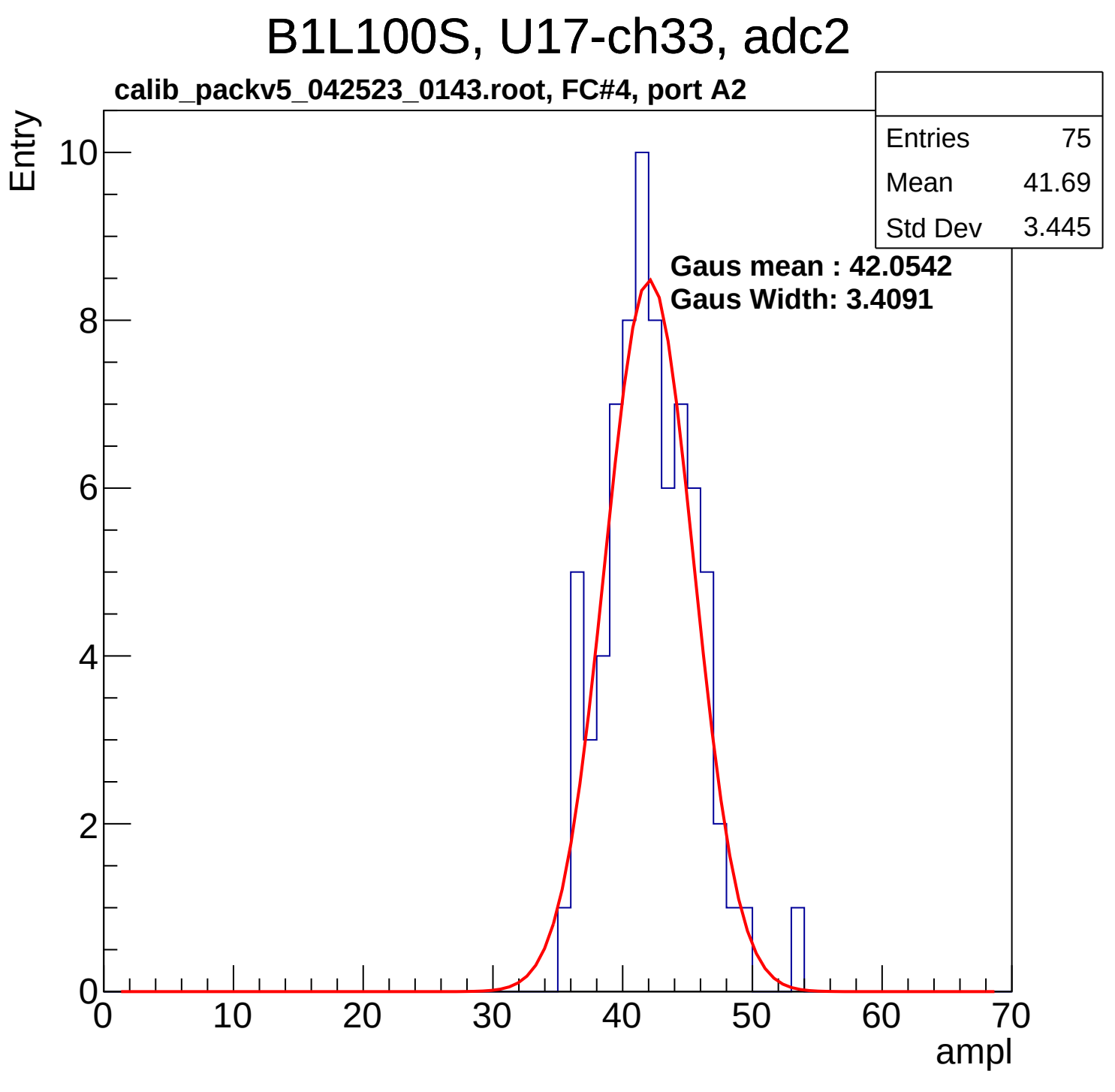

B1L100S, U17-ch32, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 58.27
Std Dev 8.568
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

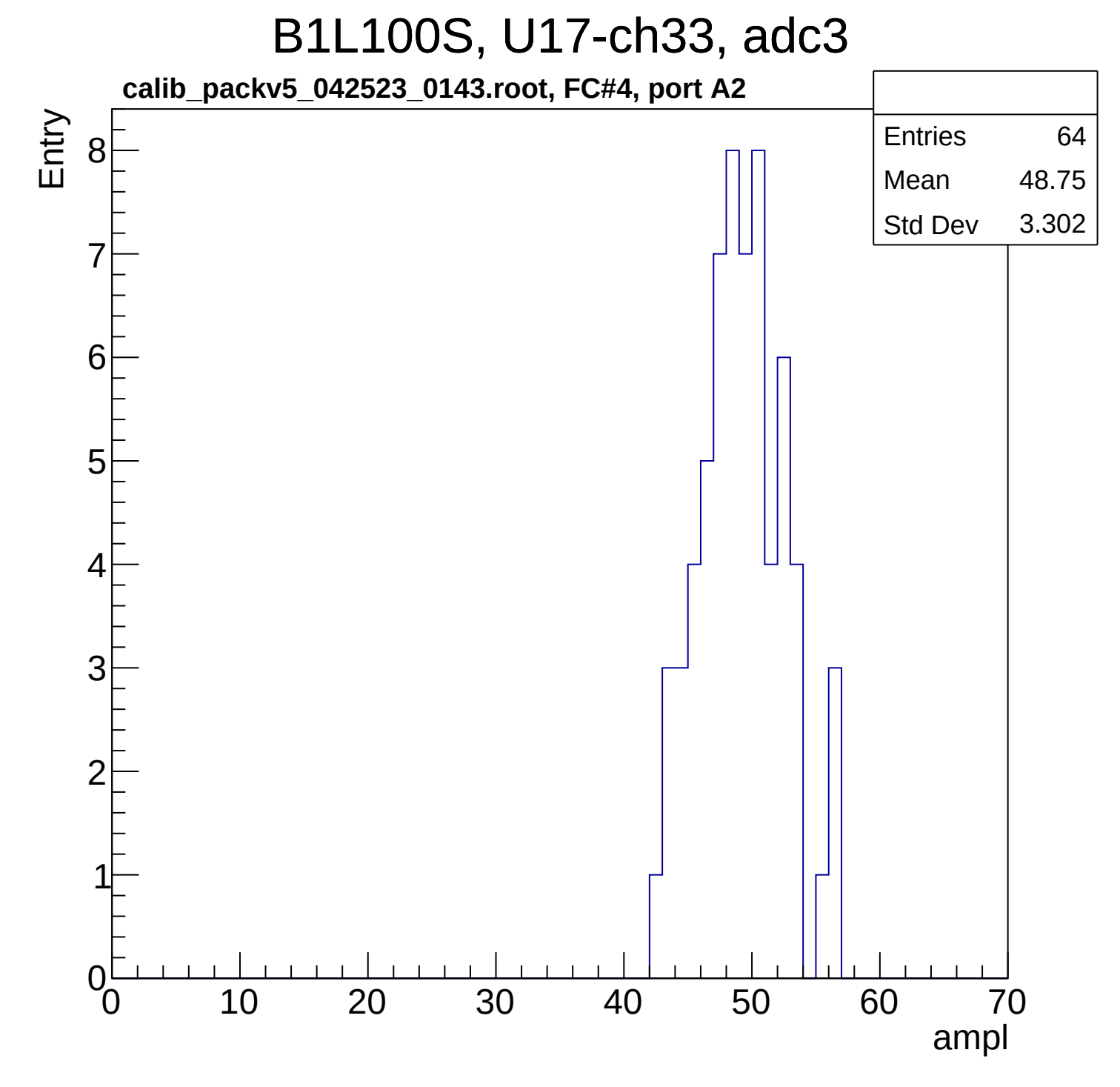

B1L100S, U17-ch32, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 11
Mean 62
Std Dev 1.128
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L100S, U17-ch32, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 20
Std Dev 28.28
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L100S, U17-ch33, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 90
Mean 27.46
Std Dev 4.115
Gaus mean : 28.2148
Gaus Width: 3.8984
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U17-ch33, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 34.88
Std Dev 3.206
Gaus mean : 35.5033
Gaus Width: 3.4792
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch33, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 75
Mean 41.69
Std Dev 3.445
Gaus mean : 42.0542
Gaus Width: 3.4091
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U17-ch33, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 48.75
Std Dev 3.302
Entry
ampl
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2
3
4
5
6
7
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0
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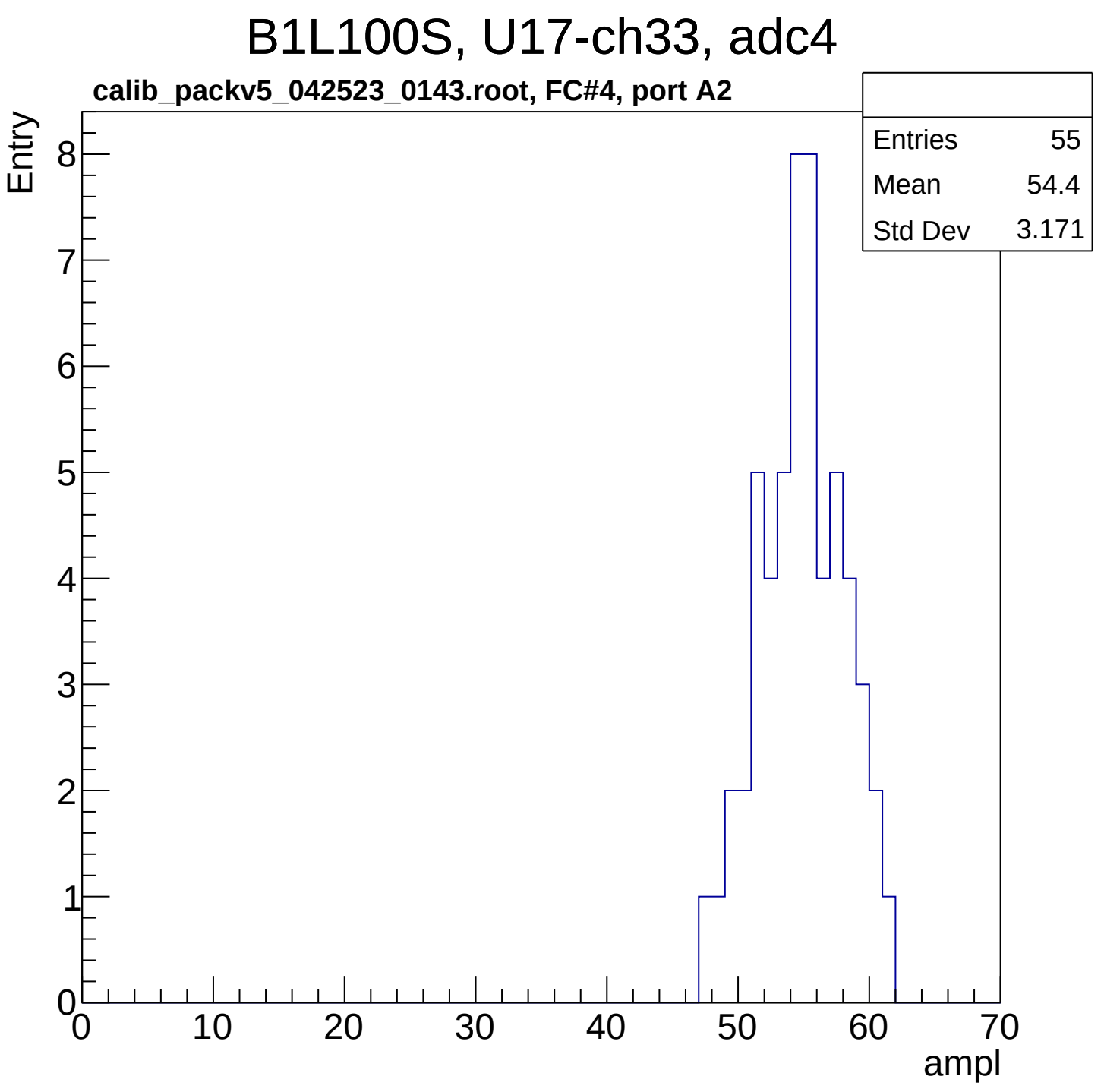
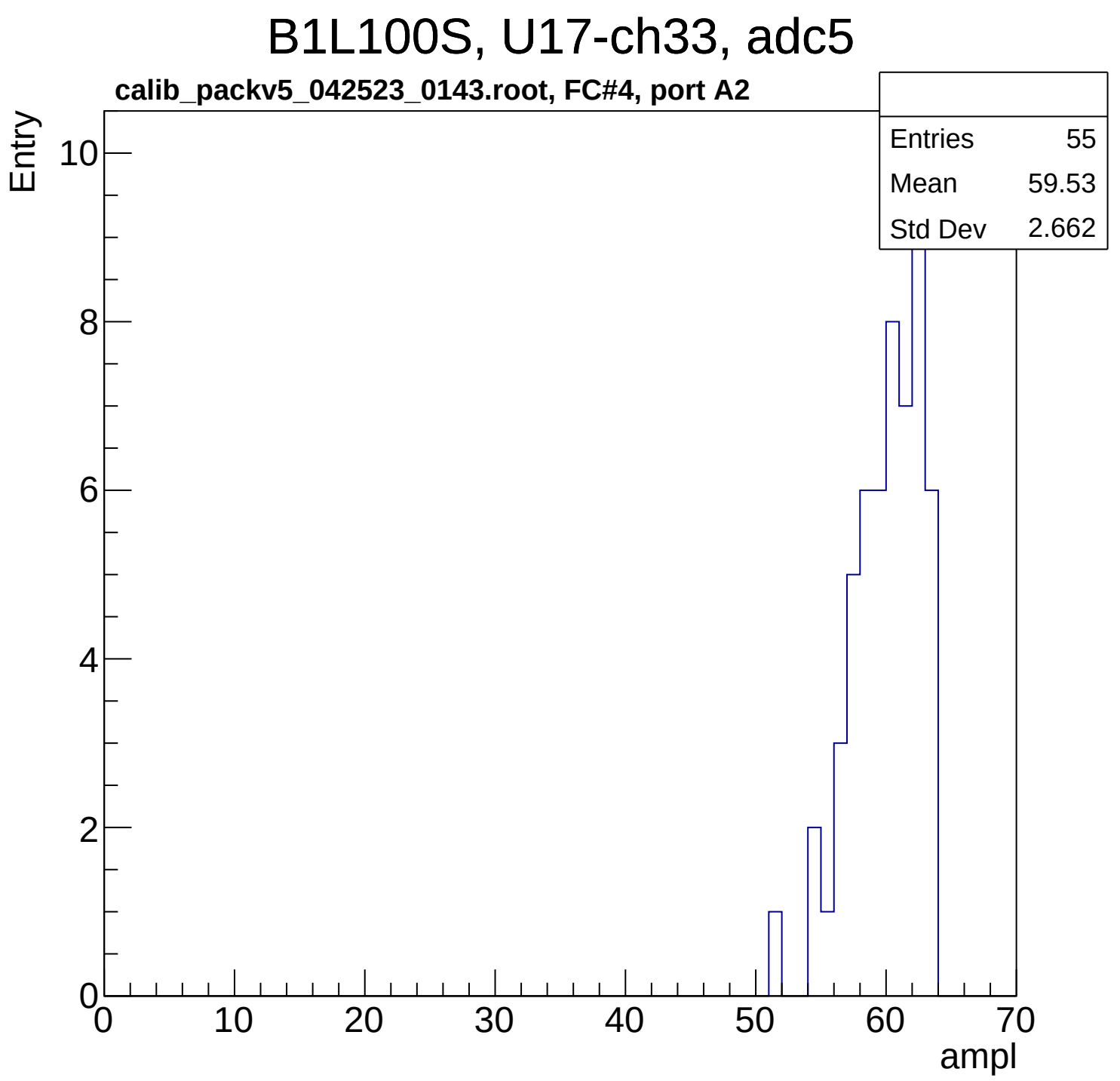
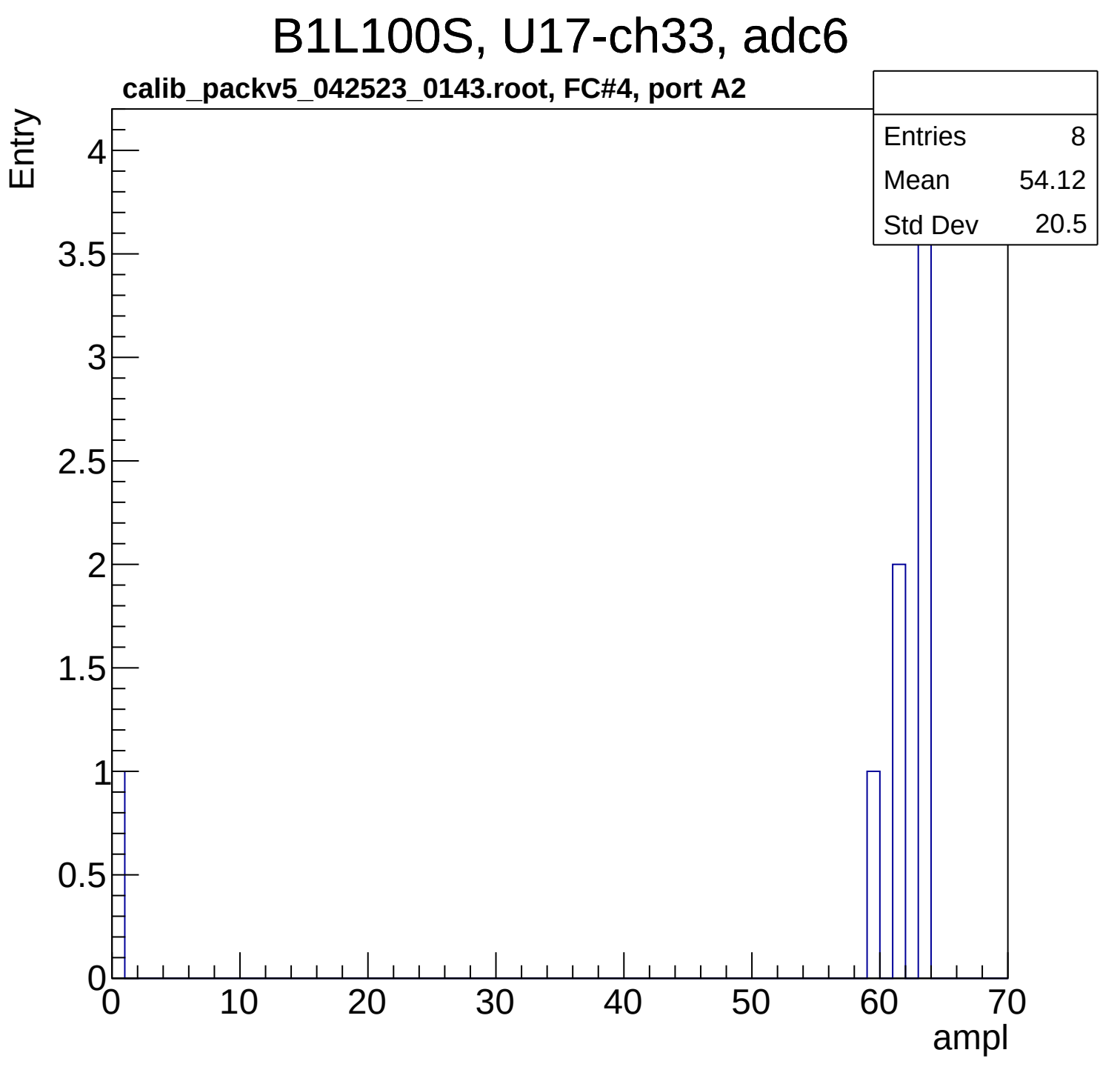
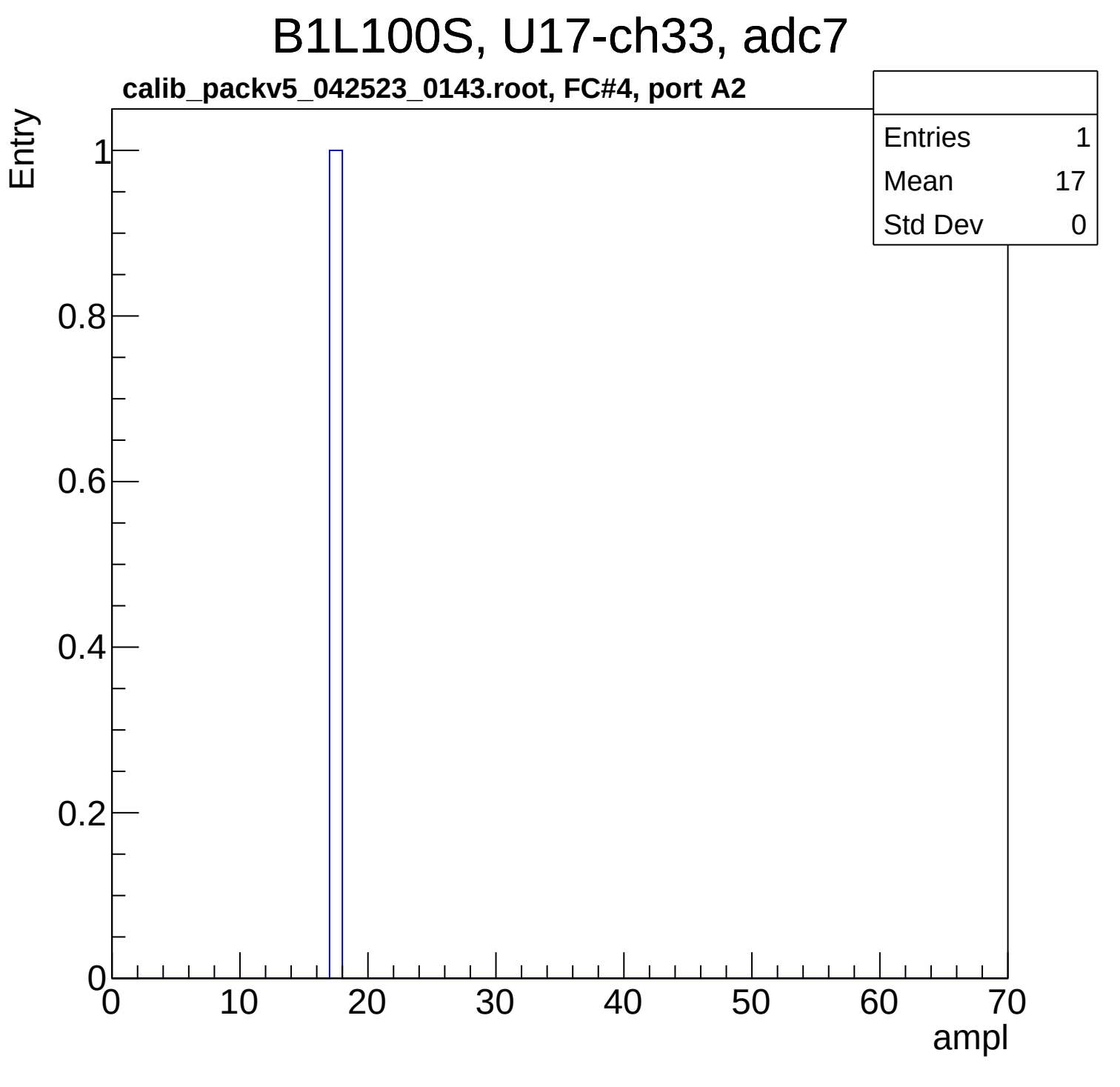
40
50
60
70


B1L100S, U17-ch33, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 54.4
Std Dev 3.171
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch33, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 59.53
Std Dev 2.662
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch33, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 8
Mean 54.12
Std Dev 20.5
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L100S, U17-ch33, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 17
Std Dev 0
Entry
1
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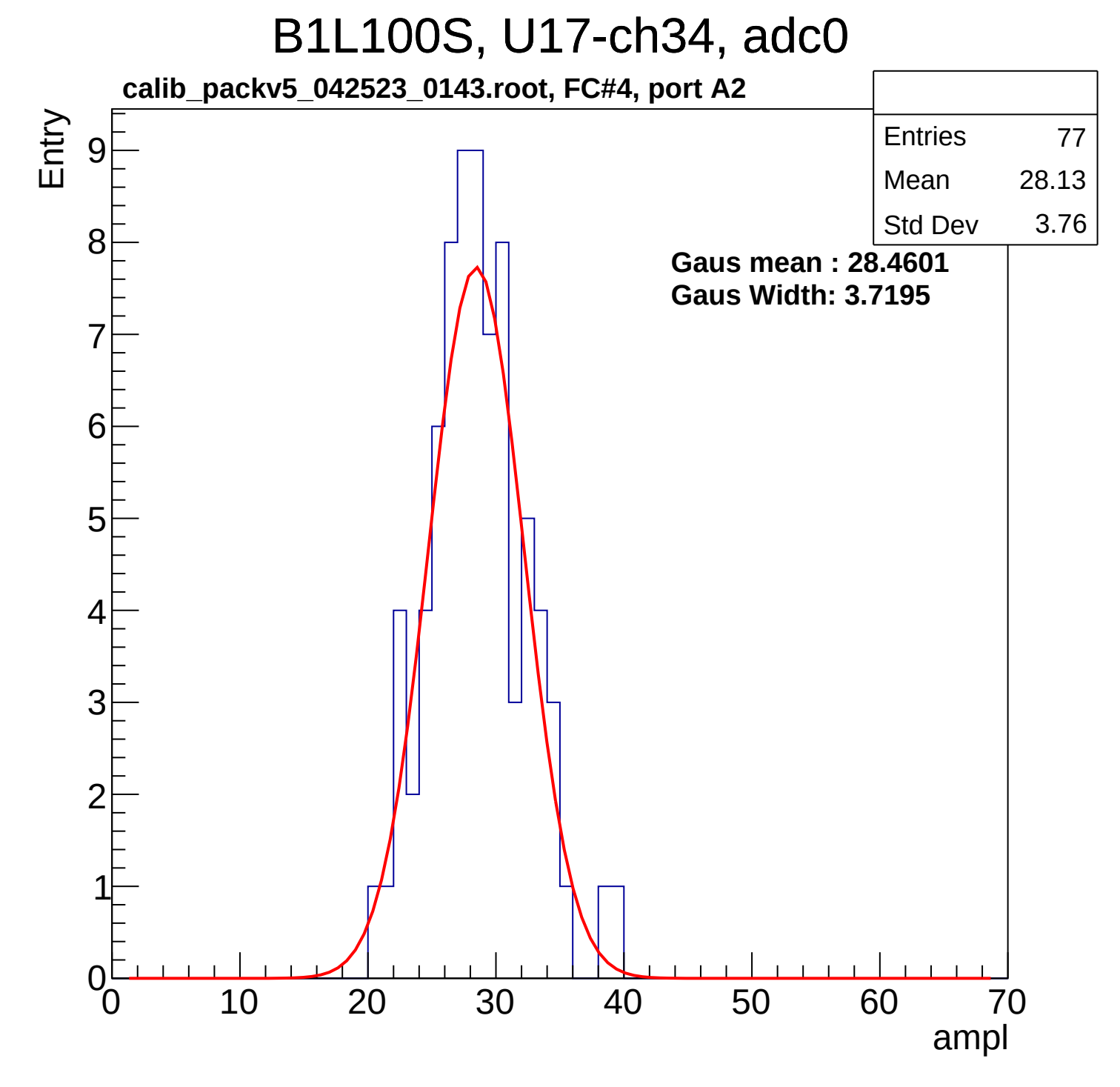
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch34, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 77
Mean 28.13
Std Dev 3.76
Gaus mean : 28.4601
Gaus Width: 3.7195
Entry
ampl
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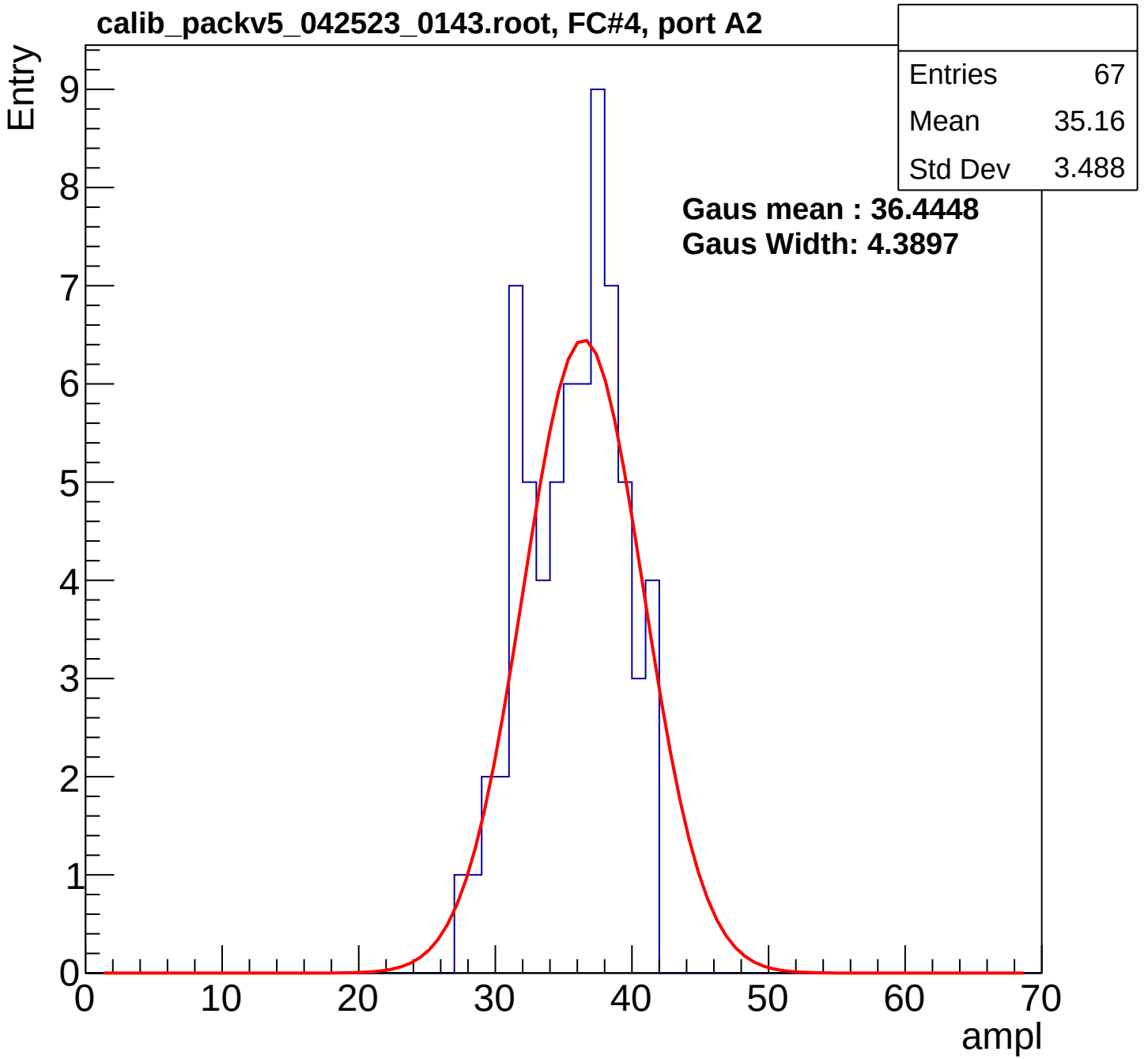
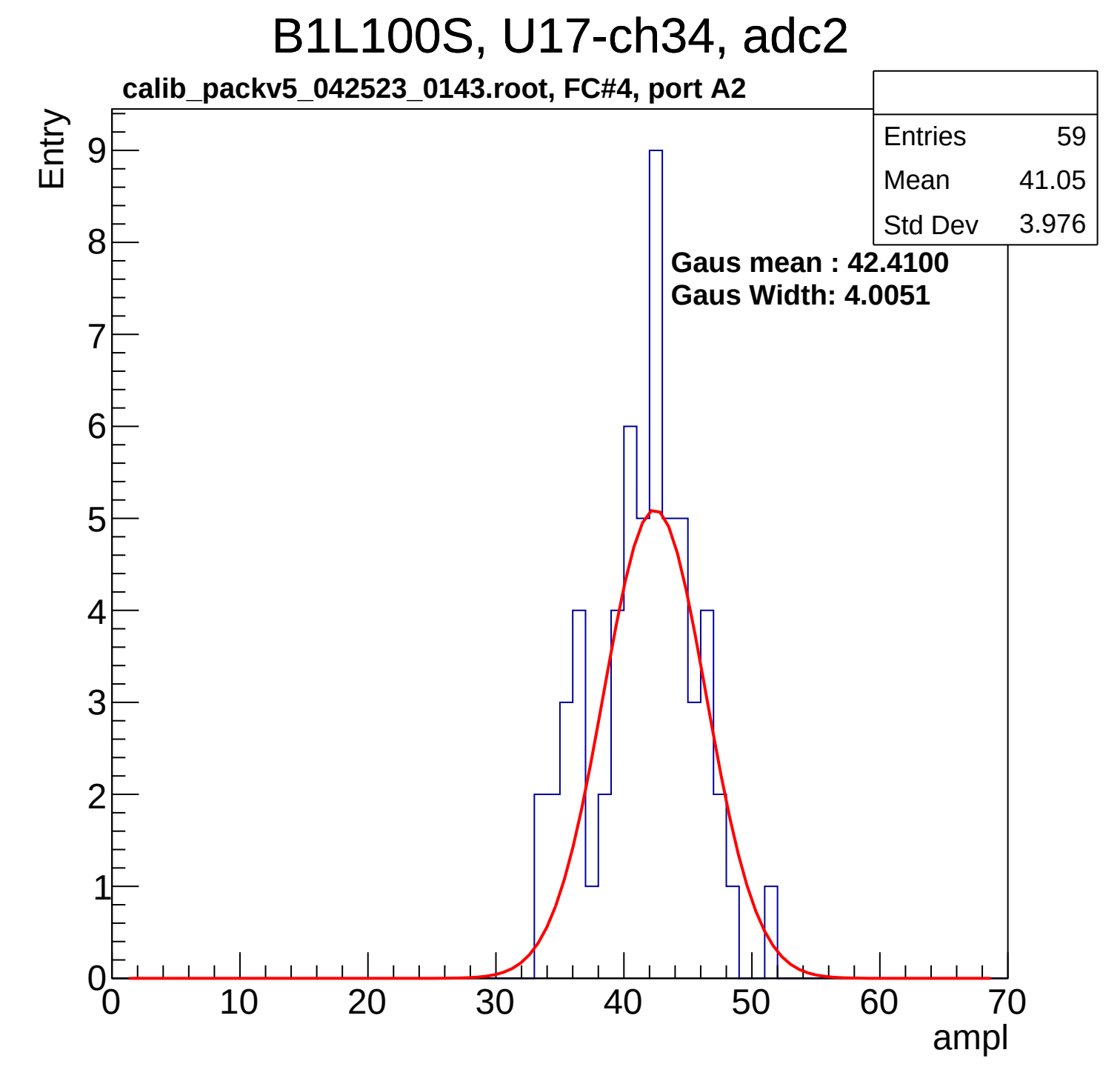
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch34, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 35.16
Std Dev 3.488
Gaus mean : 36.4448
Gaus Width: 4.3897
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch34, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 41.05
Std Dev 3.976
Gaus mean : 42.4100
Gaus Width: 4.0051
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
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60
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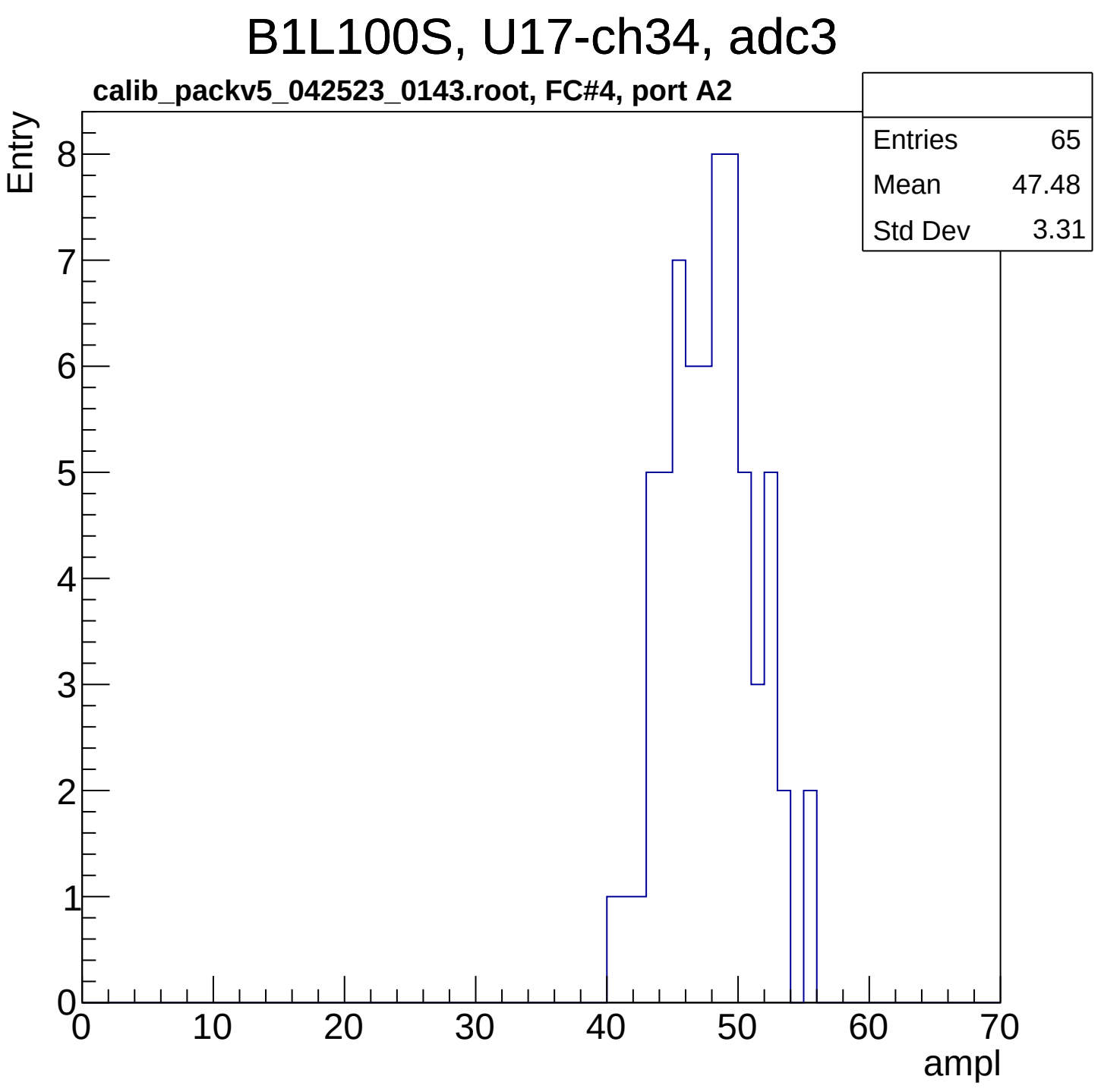
B1L100S, U17-ch34, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 47.48
Std Dev 3.31
Entry
ampl
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1
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3
4
5
6
7
8
0
10
20
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40
50
60
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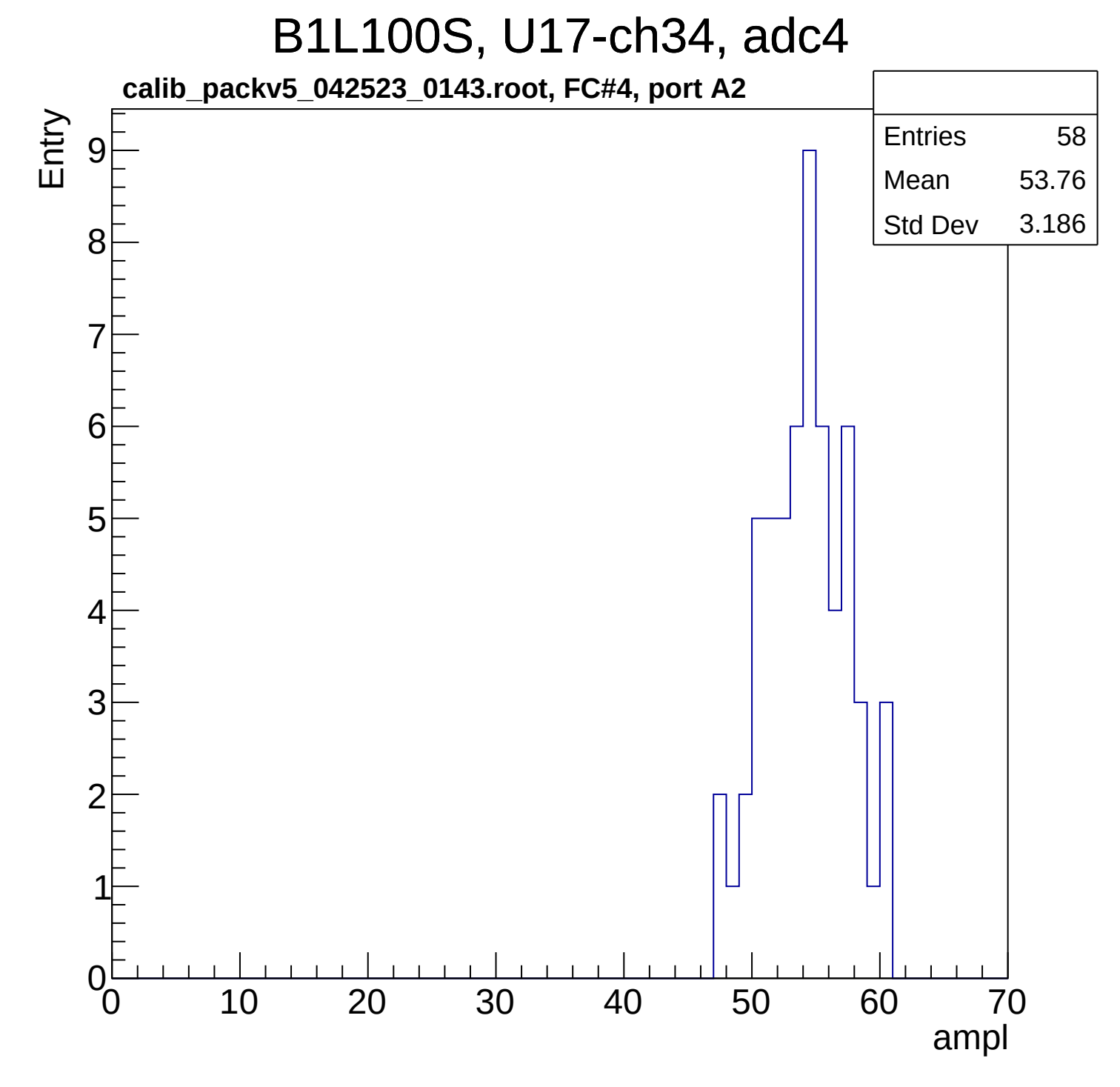
B1L100S, U17-ch34, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 53.76
Std Dev 3.186
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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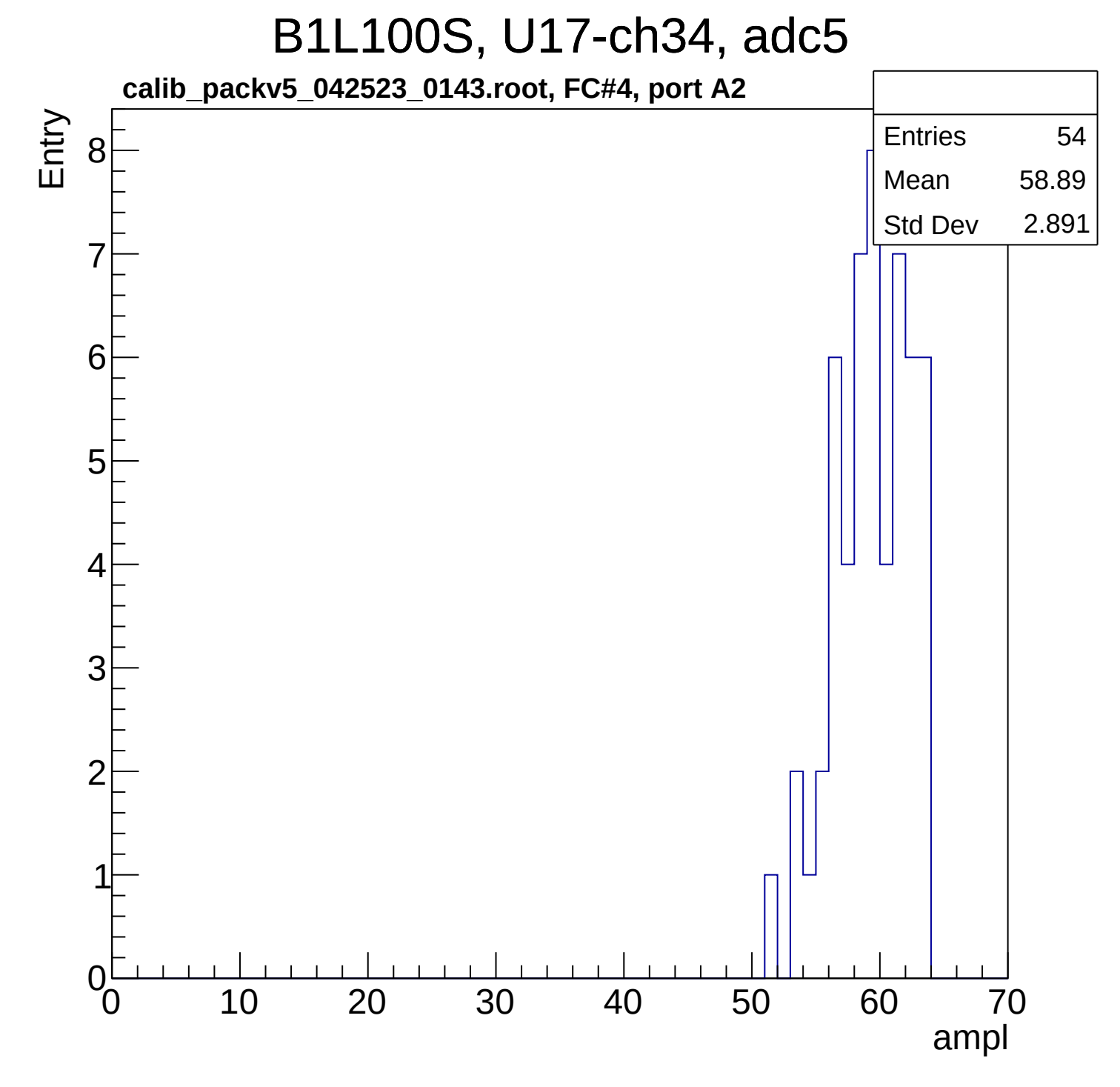
B1L100S, U17-ch34, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 58.89
Std Dev 2.891
Entry
ampl
0
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2
3
4
5
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7
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0
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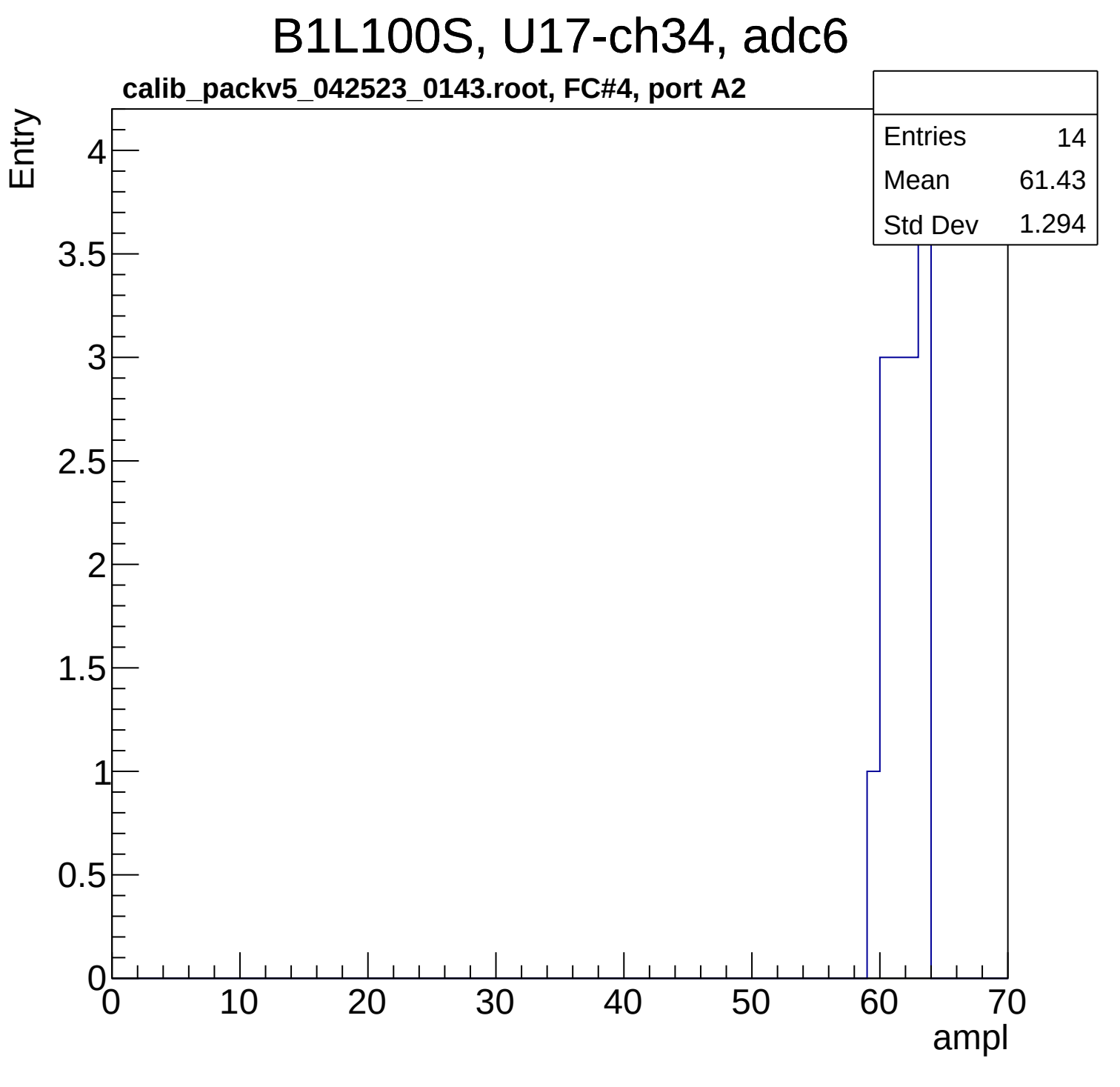
40
50
60
70


B1L100S, U17-ch34, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 14
Mean 61.43
Std Dev 1.294
Entry
ampl
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0.5
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1.5
2
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3.5
4
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60
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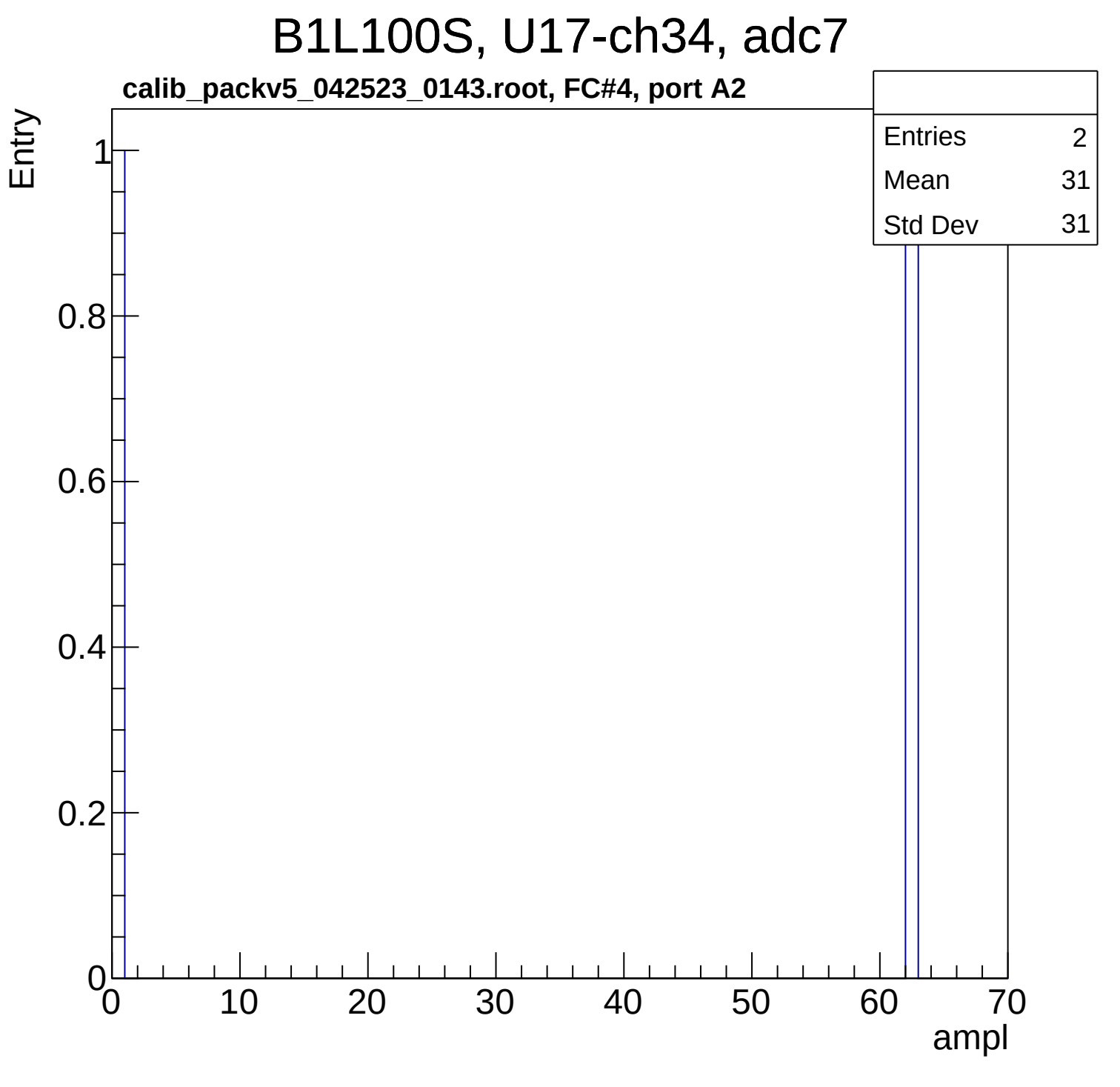
B1L100S, U17-ch34, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 31
Std Dev 31
Entry
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0.6
0.4
0.2
0
0
10
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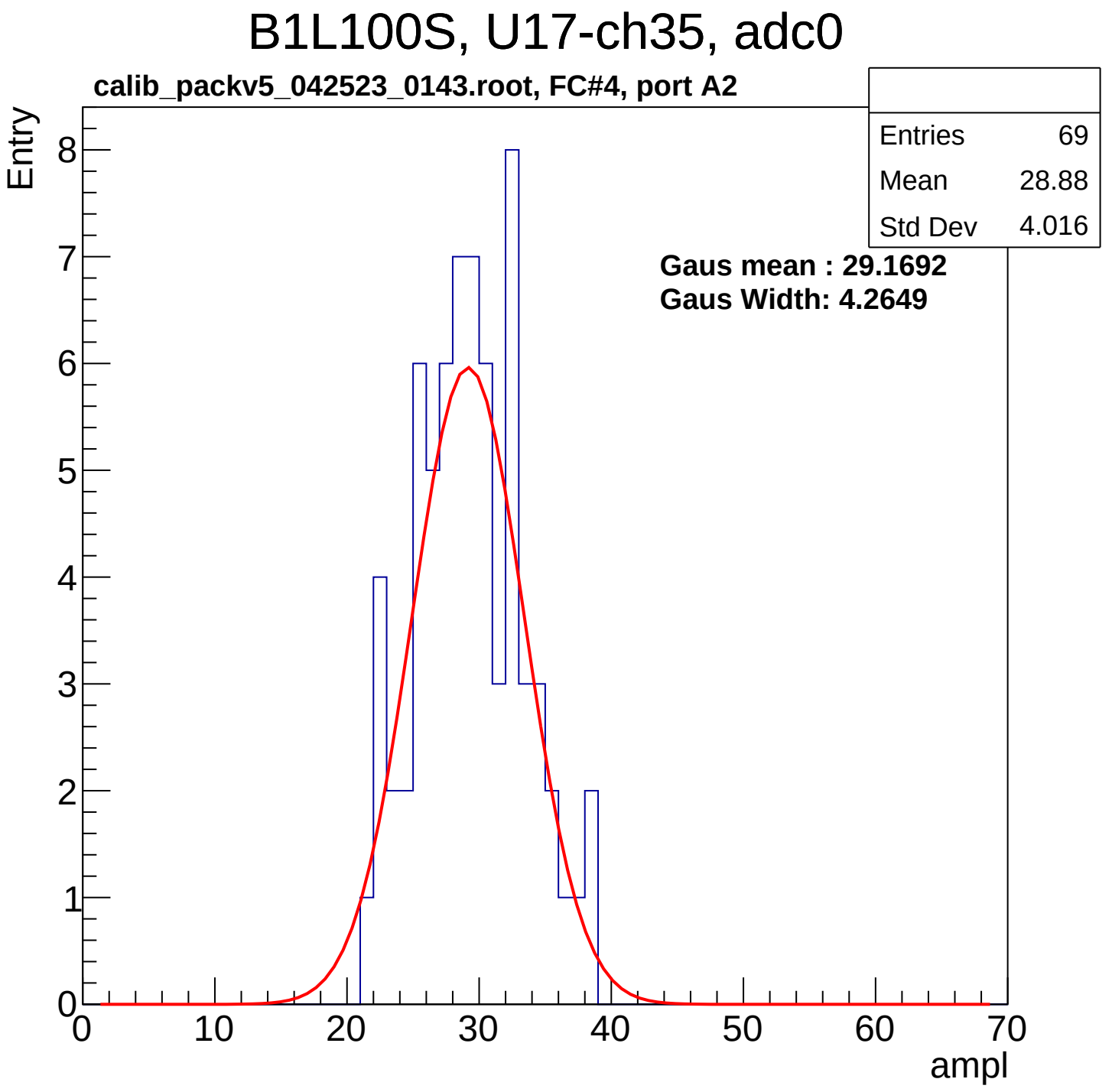
50
60
70
ampl


B1L100S, U17-ch35, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 28.88
Std Dev 4.016
Gaus mean : 29.1692
Gaus Width: 4.2649
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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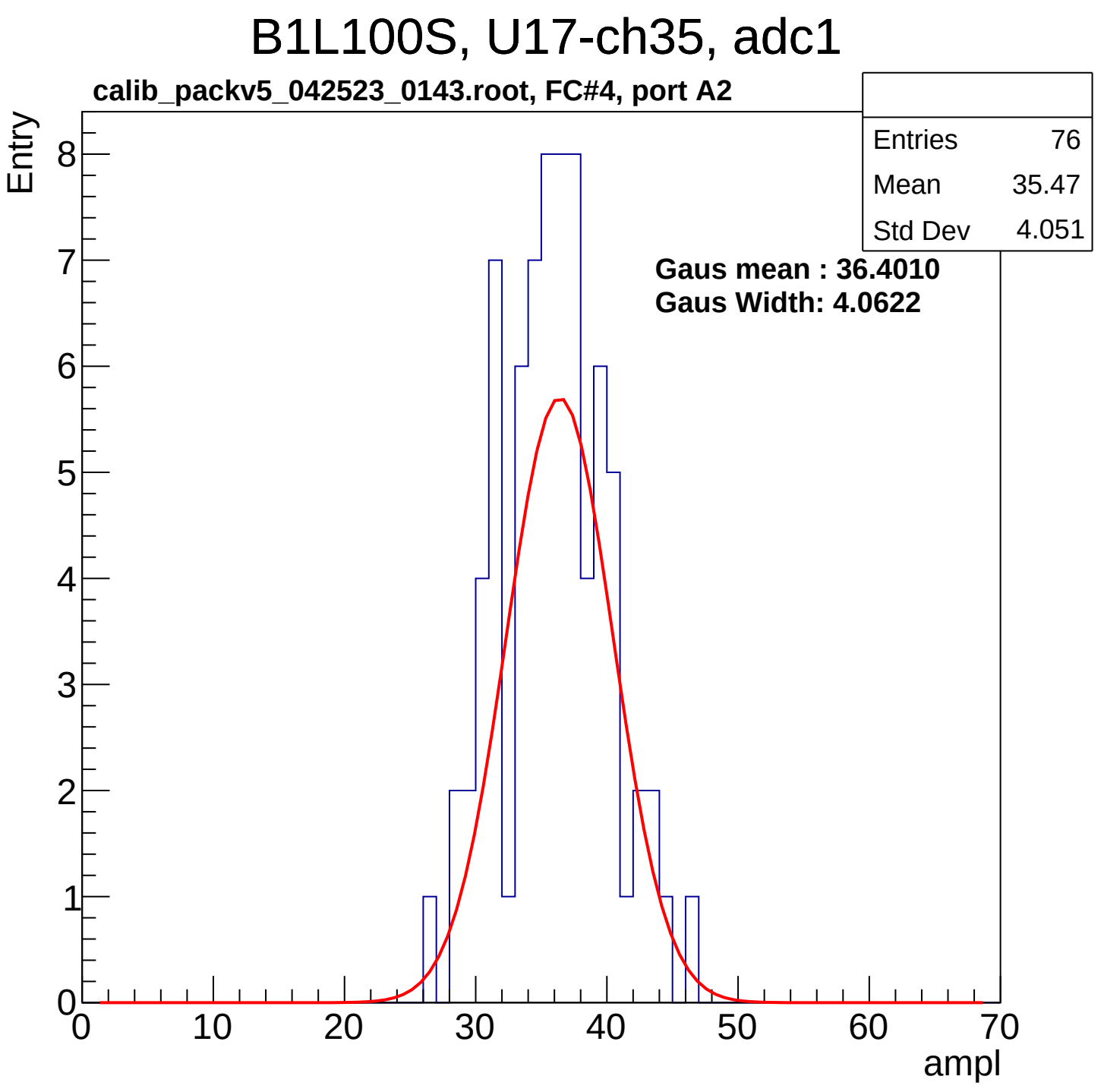
B1L100S, U17-ch35, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 76
Mean 35.47
Std Dev 4.051
Gaus mean : 36.4010
Gaus Width: 4.0622
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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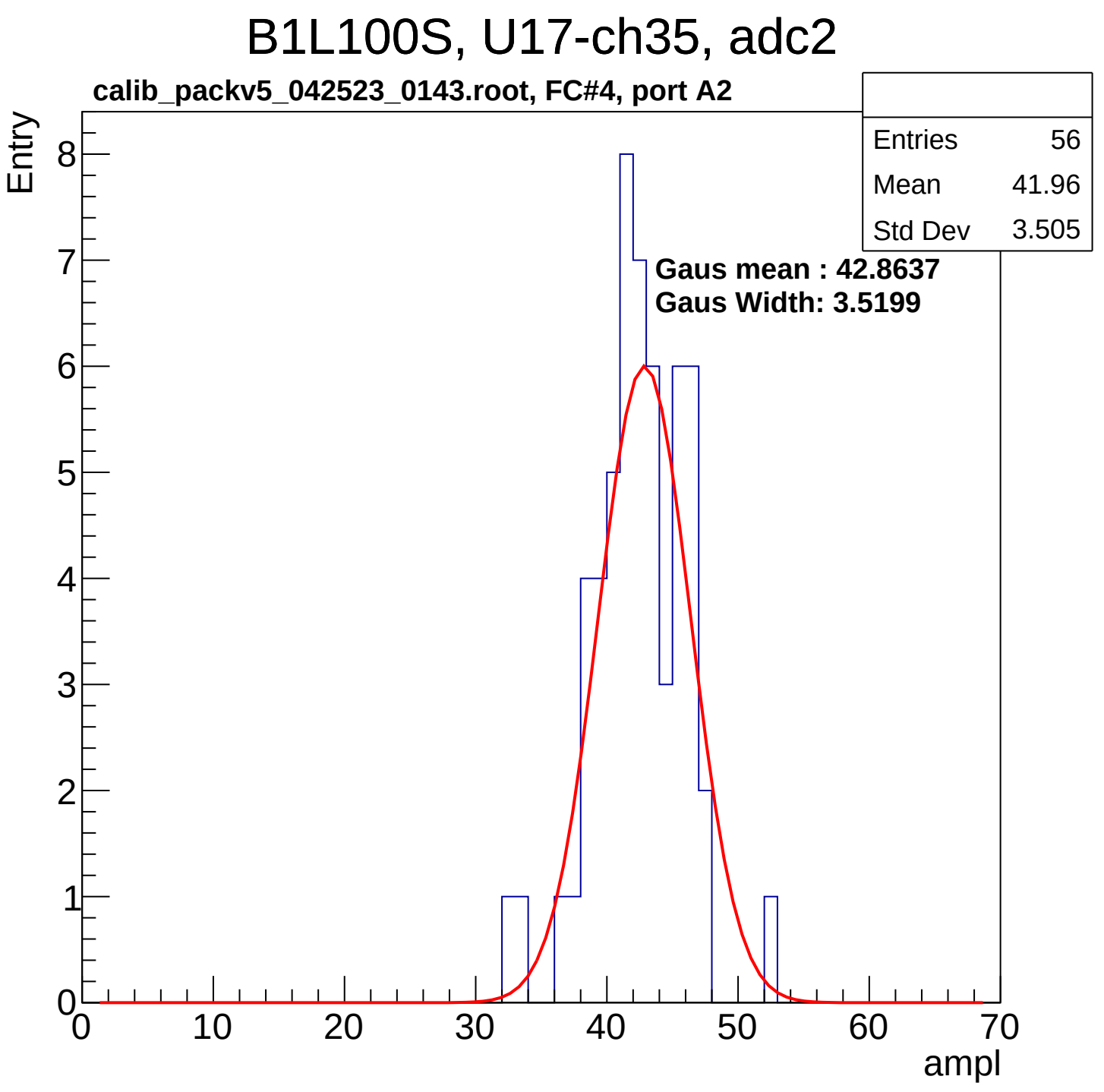
B1L100S, U17-ch35, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 41.96
Std Dev 3.505
Gaus mean : 42.8637
Gaus Width: 3.5199
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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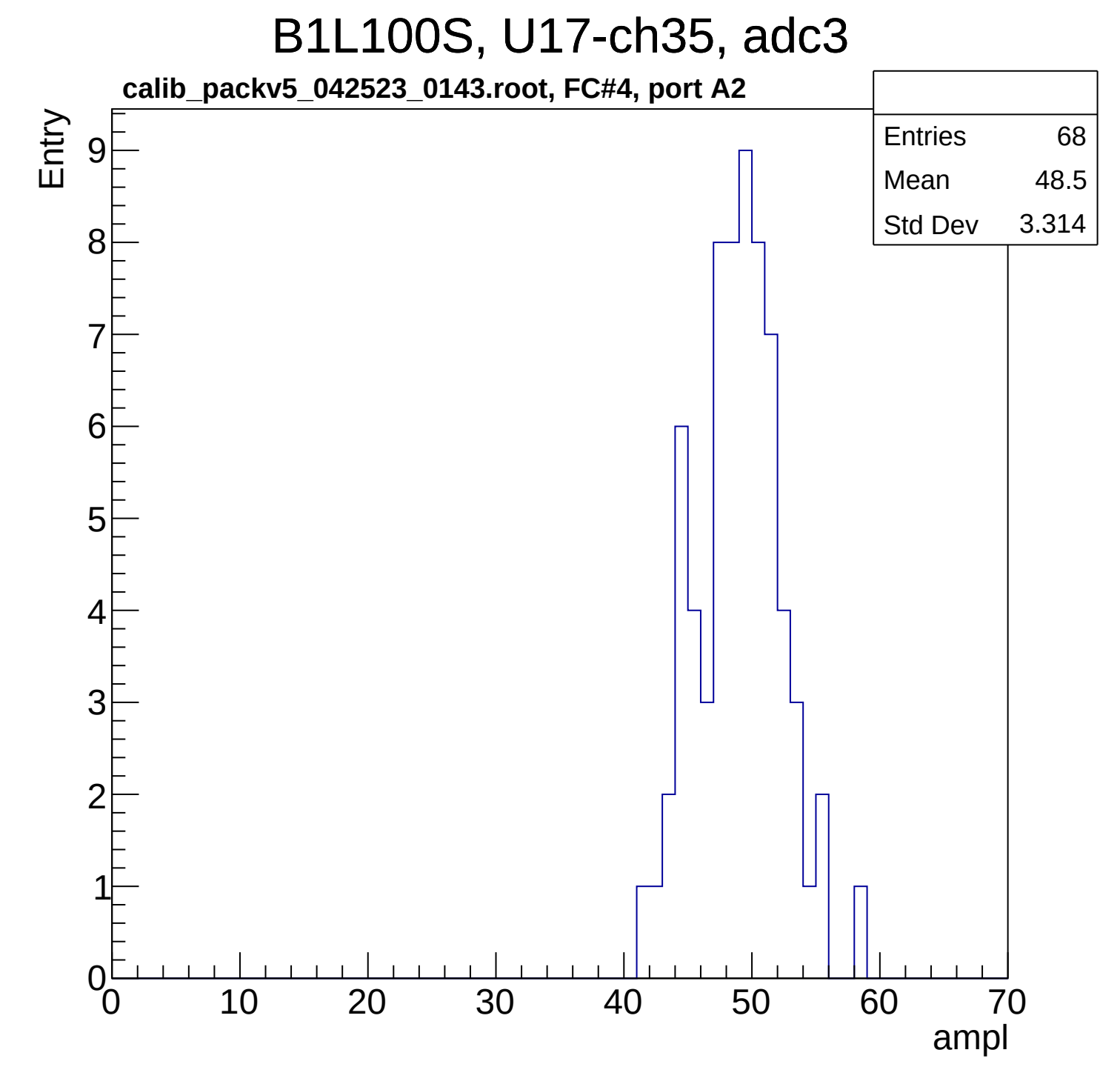
B1L100S, U17-ch35, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 48.5
Std Dev 3.314
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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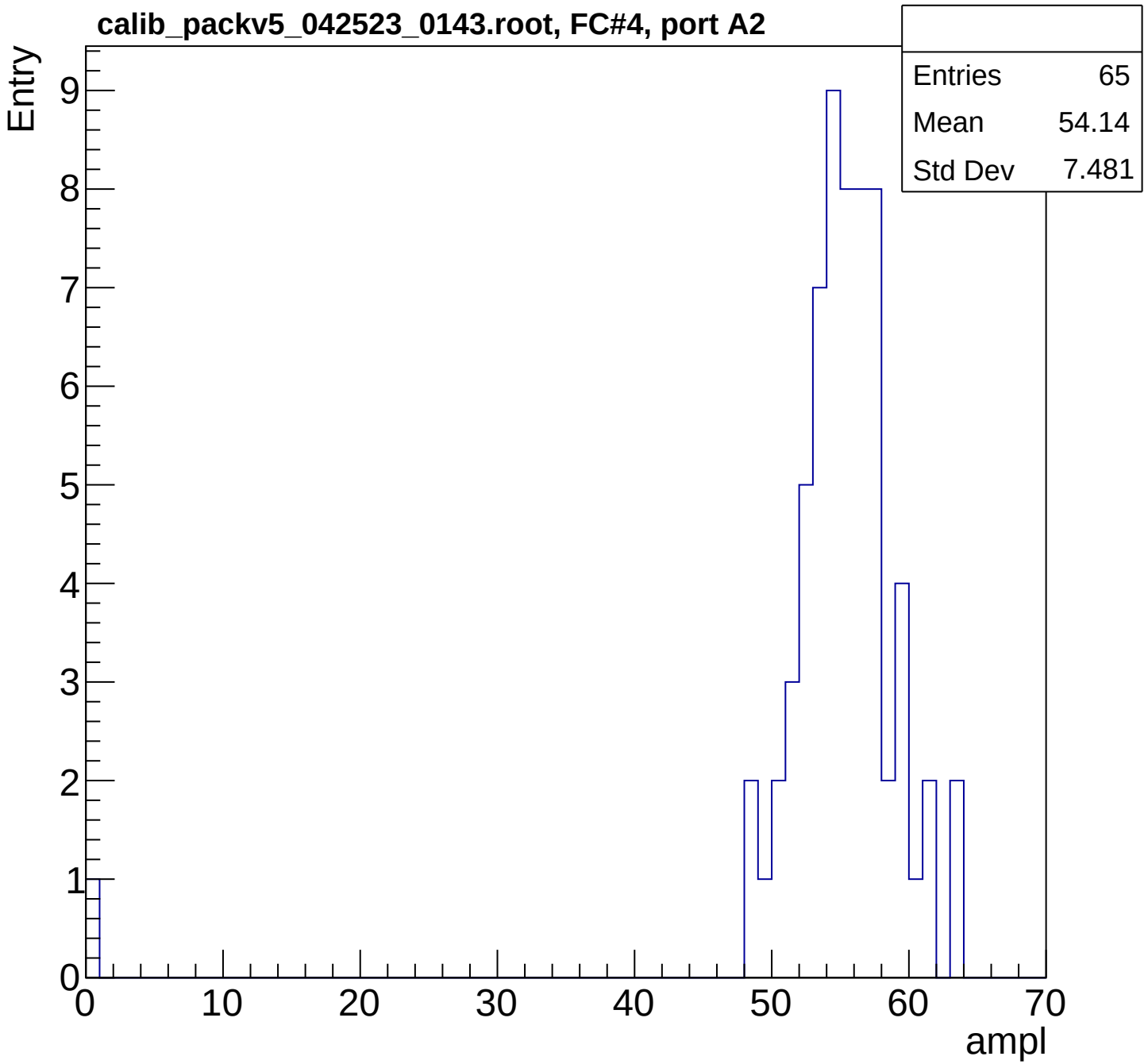
B1L100S, U17-ch35, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 54.14
Std Dev 7.481
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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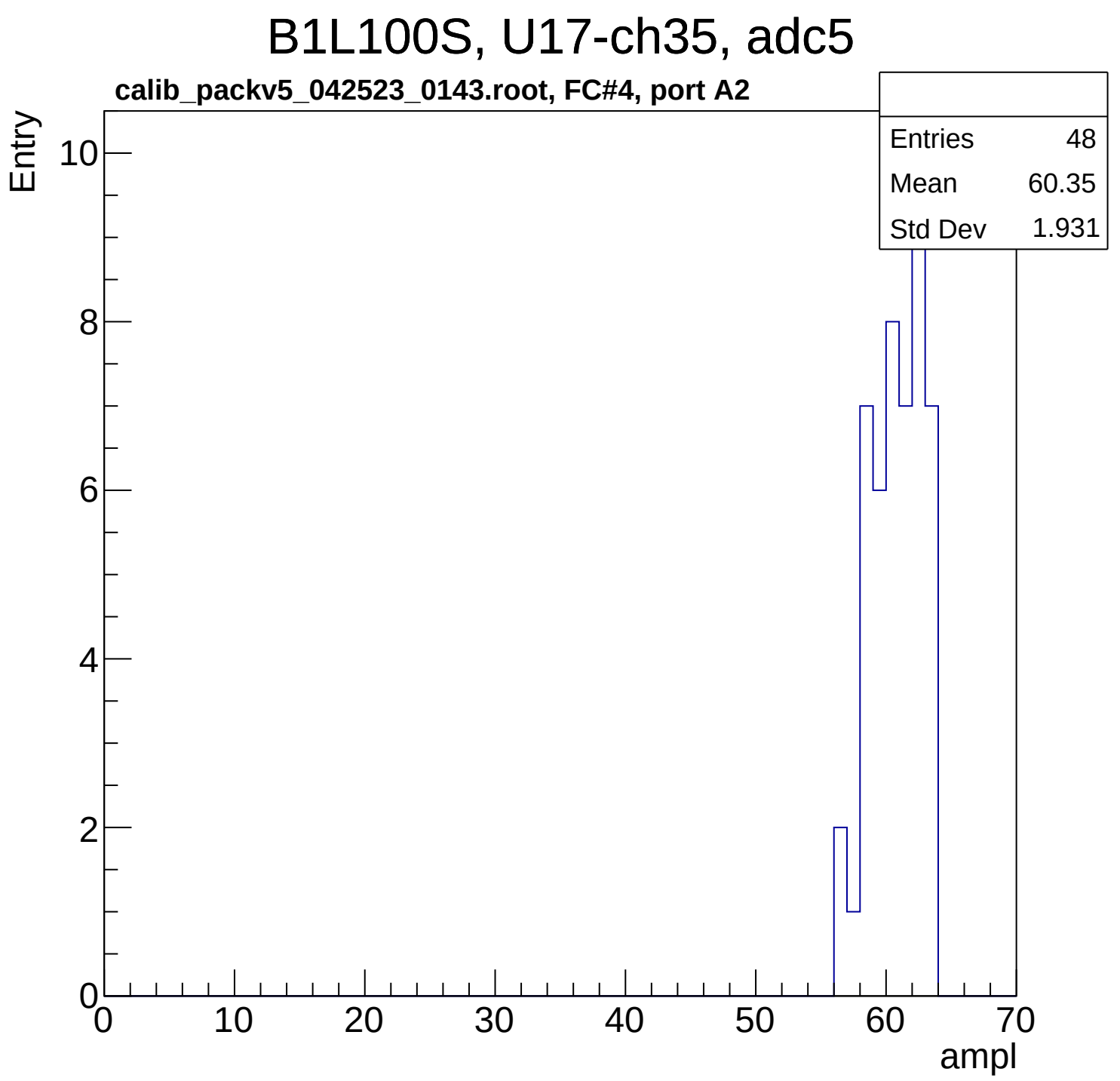
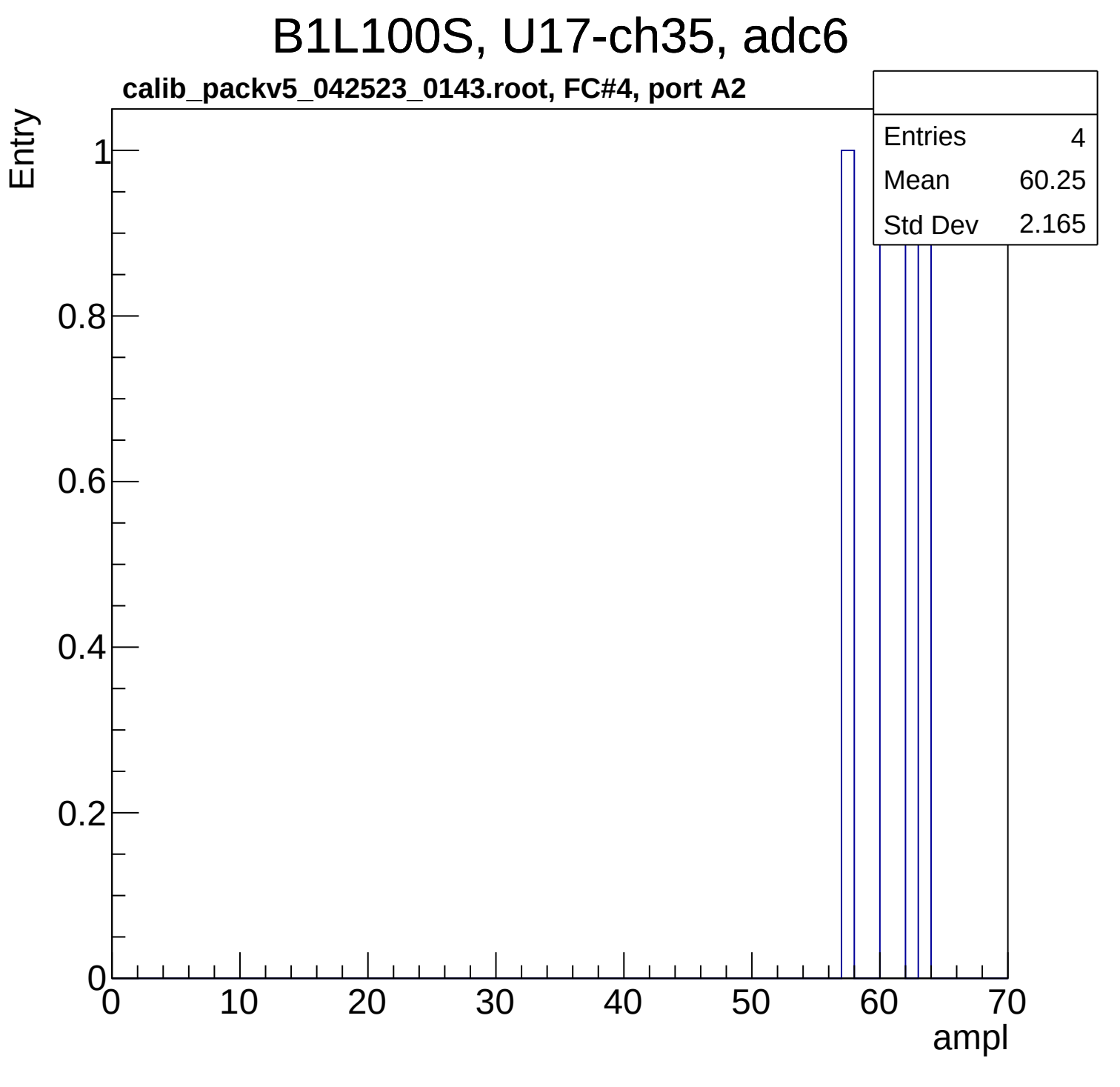
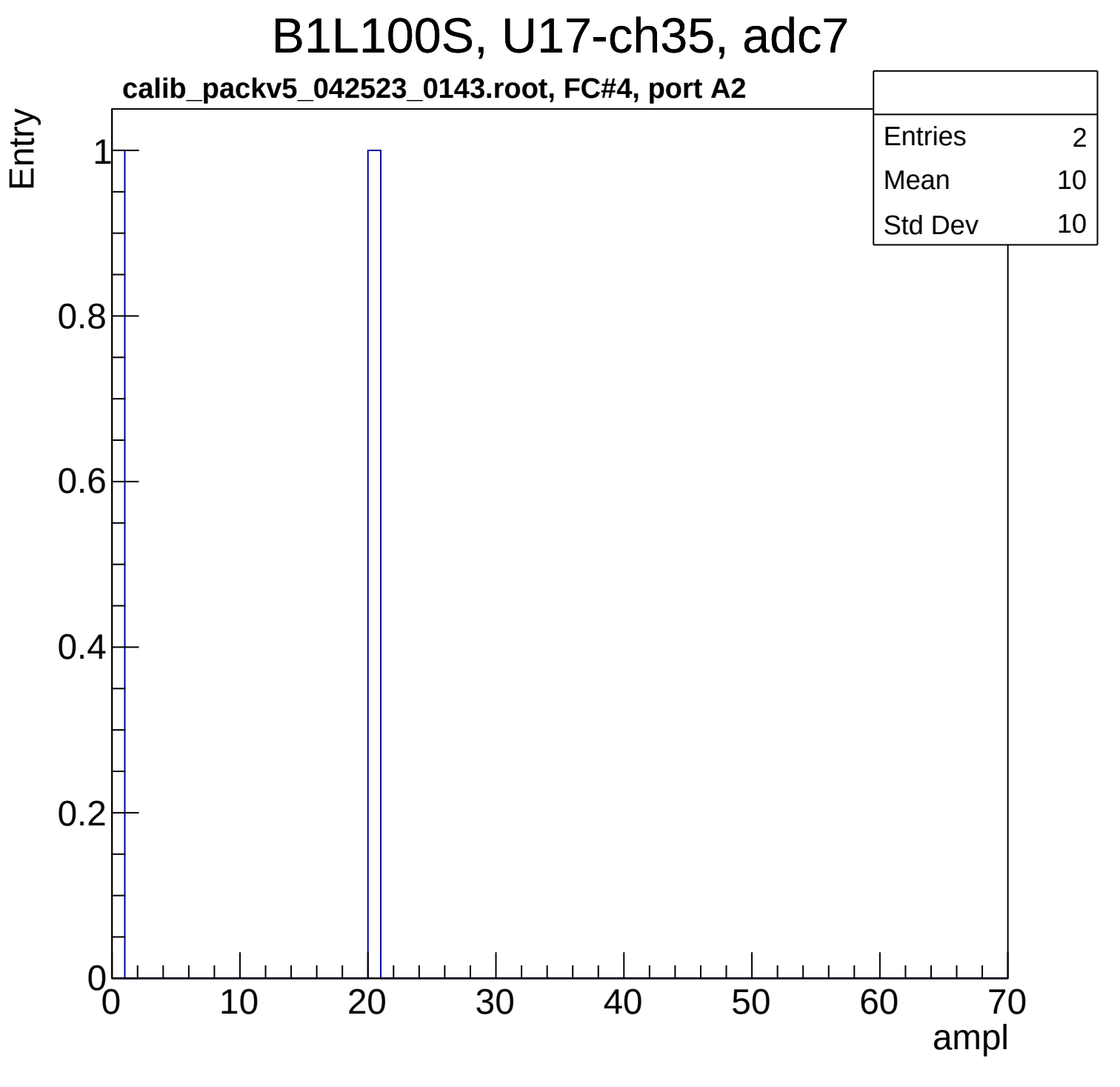

B1L100S, U17-ch35, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 48
Mean 60.35
Std Dev 1.931
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch35, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 4
Mean 60.25
Std Dev 2.165
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B1L100S, U17-ch35, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 10
Std Dev 10
Entry
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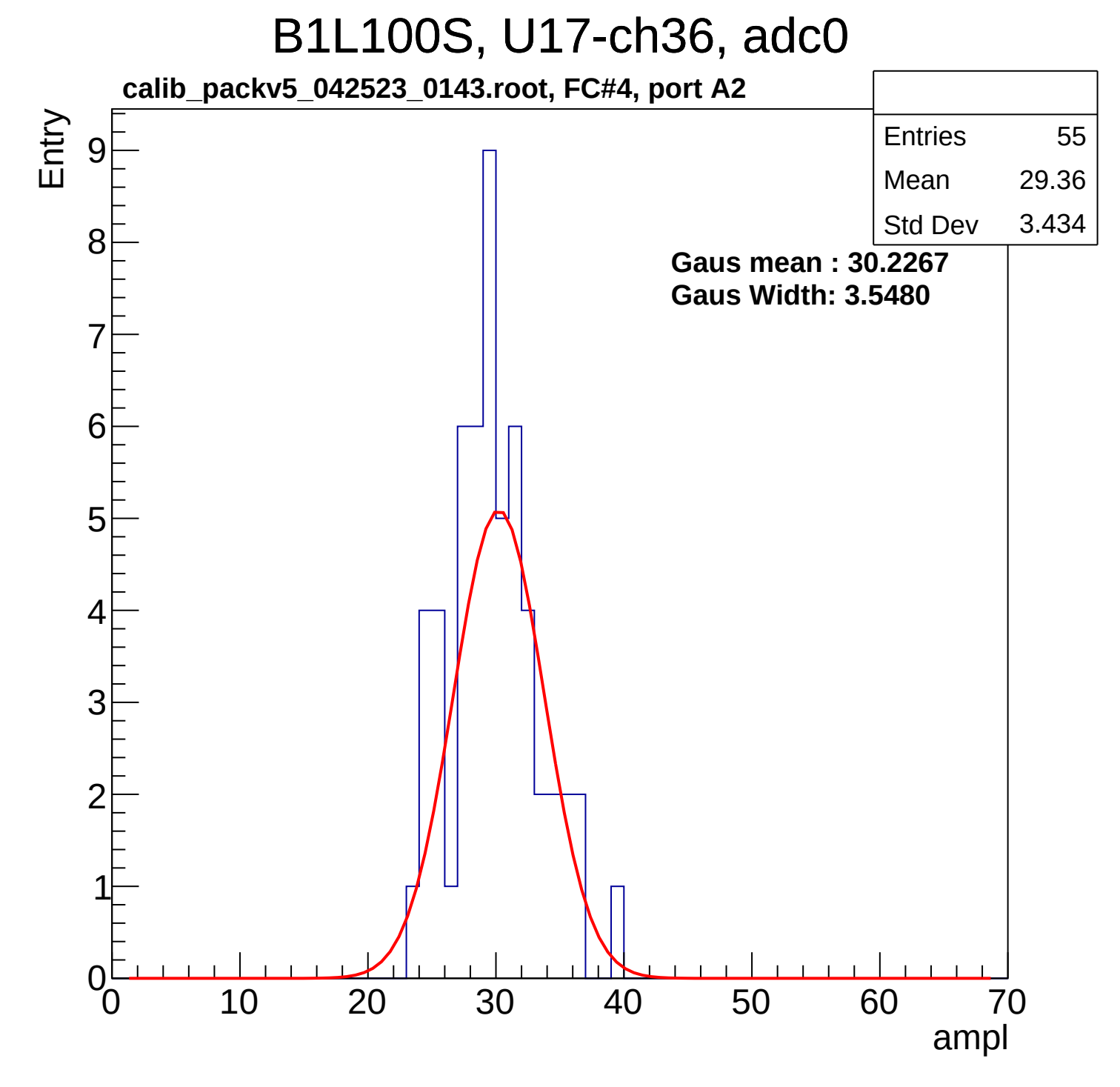
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch36, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 29.36
Std Dev 3.434
Gaus mean : 30.2267
Gaus Width: 3.5480
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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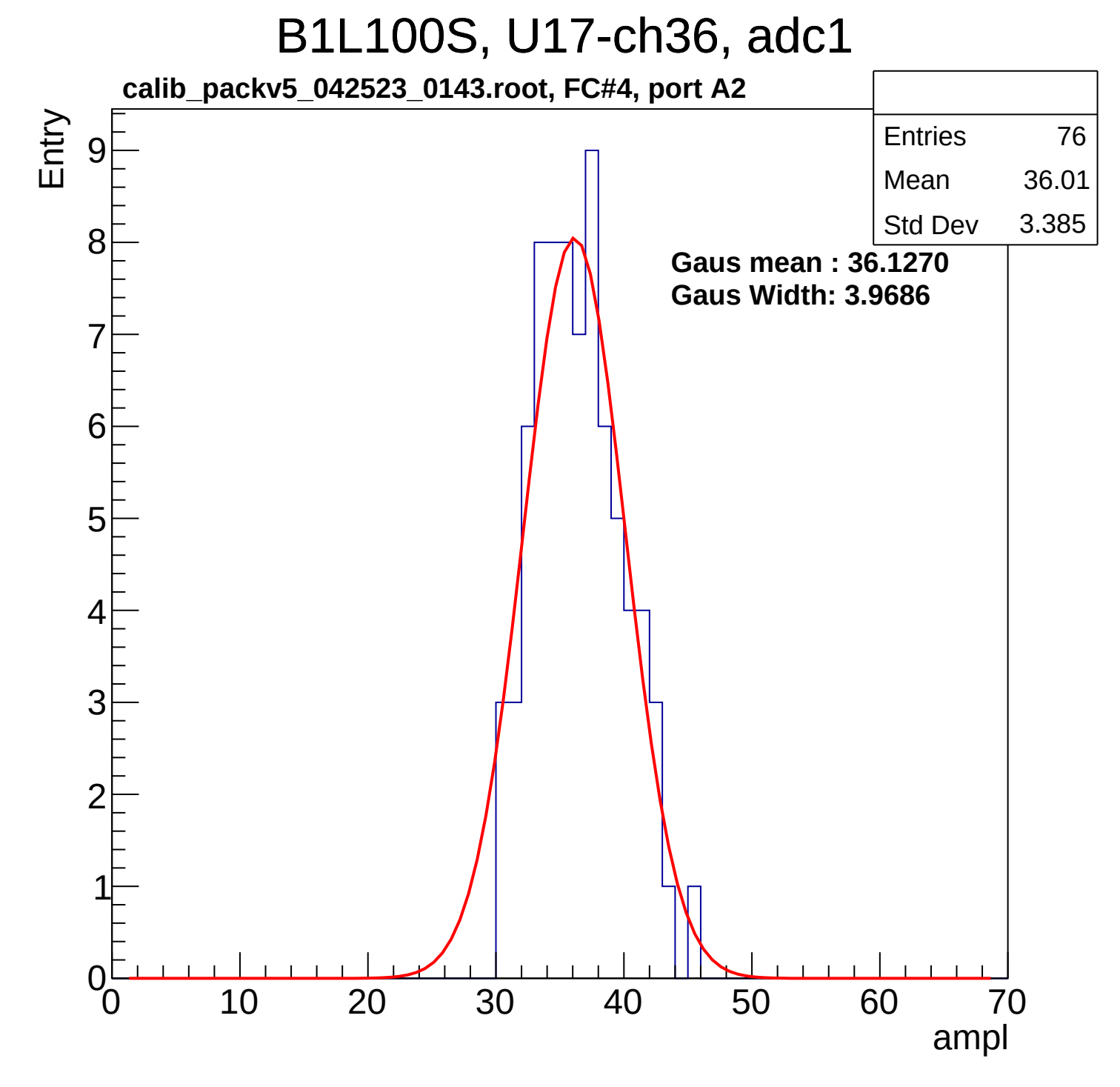
B1L100S, U17-ch36, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 76
Mean 36.01
Std Dev 3.385
Gaus mean : 36.1270
Gaus Width: 3.9686
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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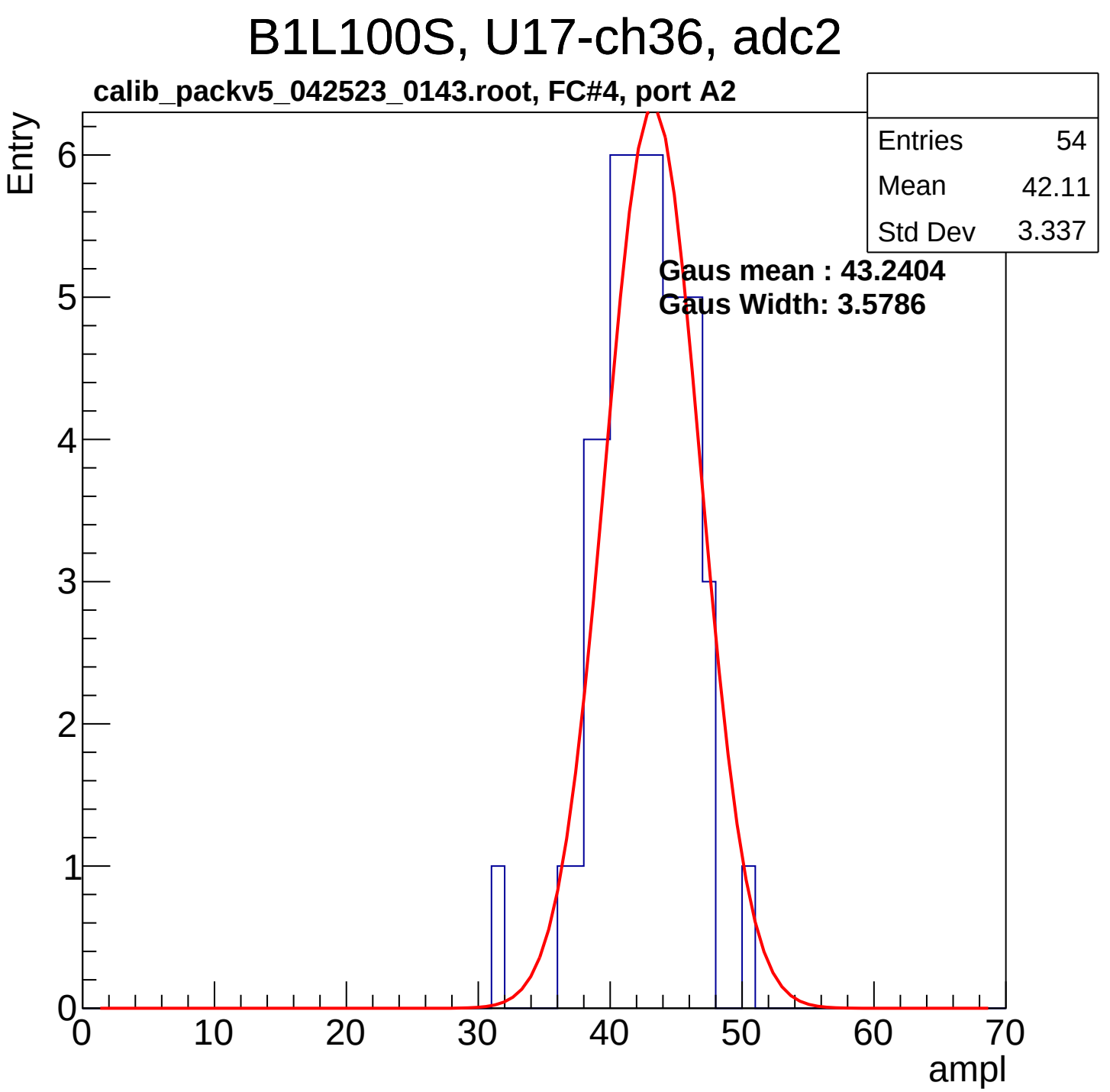
B1L100S, U17-ch36, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 42.11
Std Dev 3.337
Gaus mean : 43.2404
Gaus Width: 3.5786
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
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60
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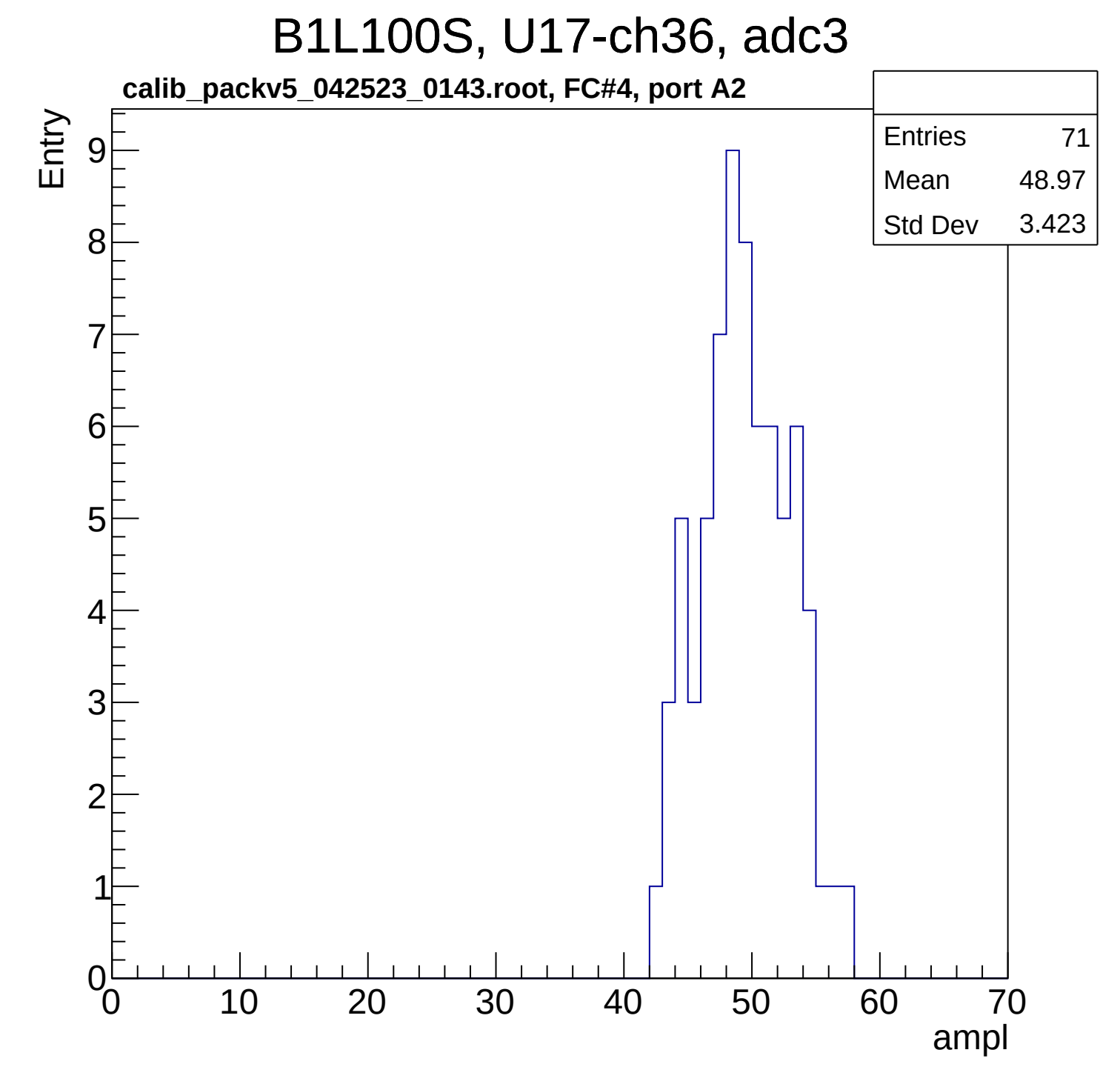
B1L100S, U17-ch36, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 48.97
Std Dev 3.423
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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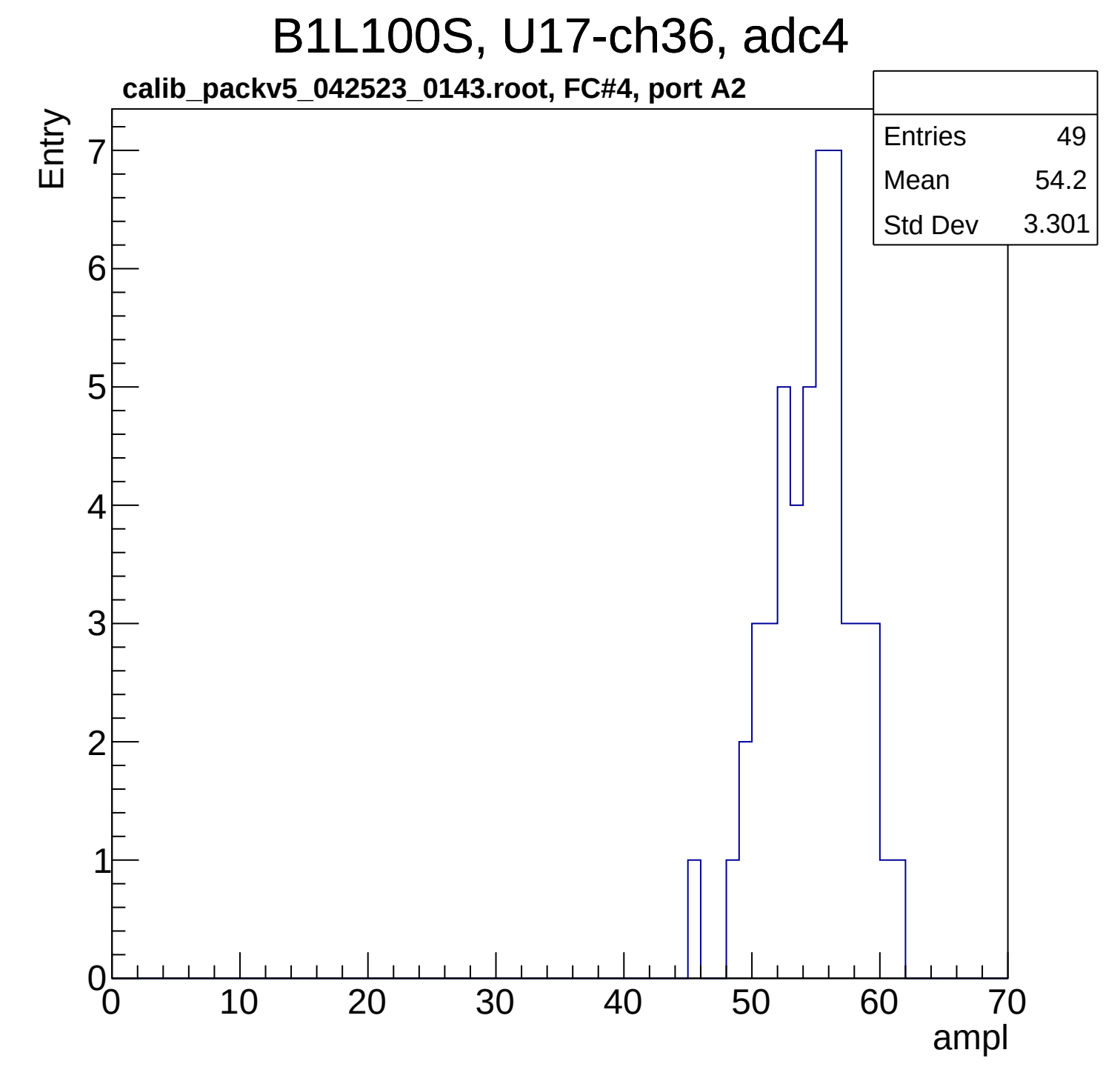
B1L100S, U17-ch36, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 49
Mean 54.2
Std Dev 3.301
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
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60
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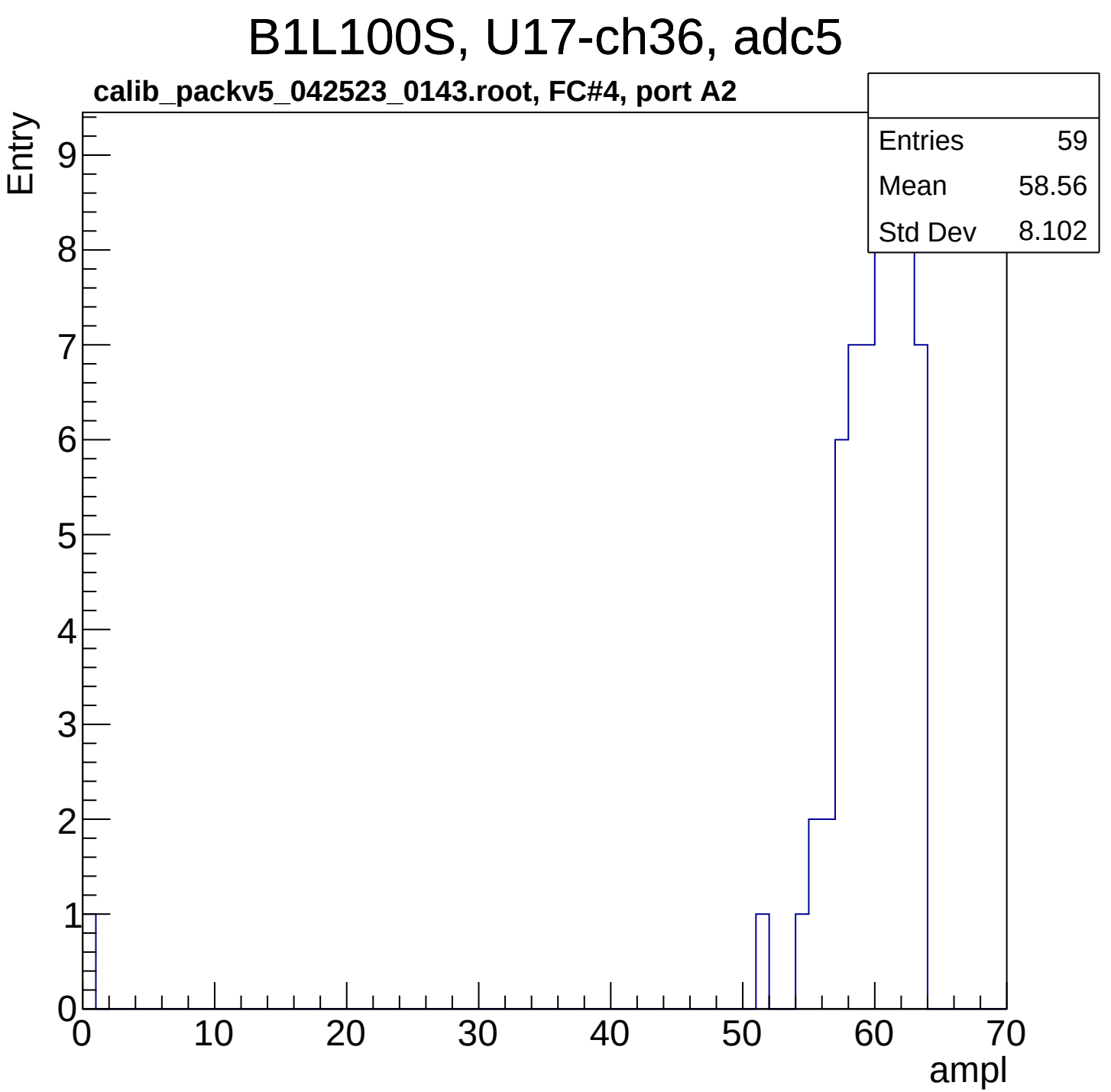
B1L100S, U17-ch36, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 58.56
Std Dev 8.102
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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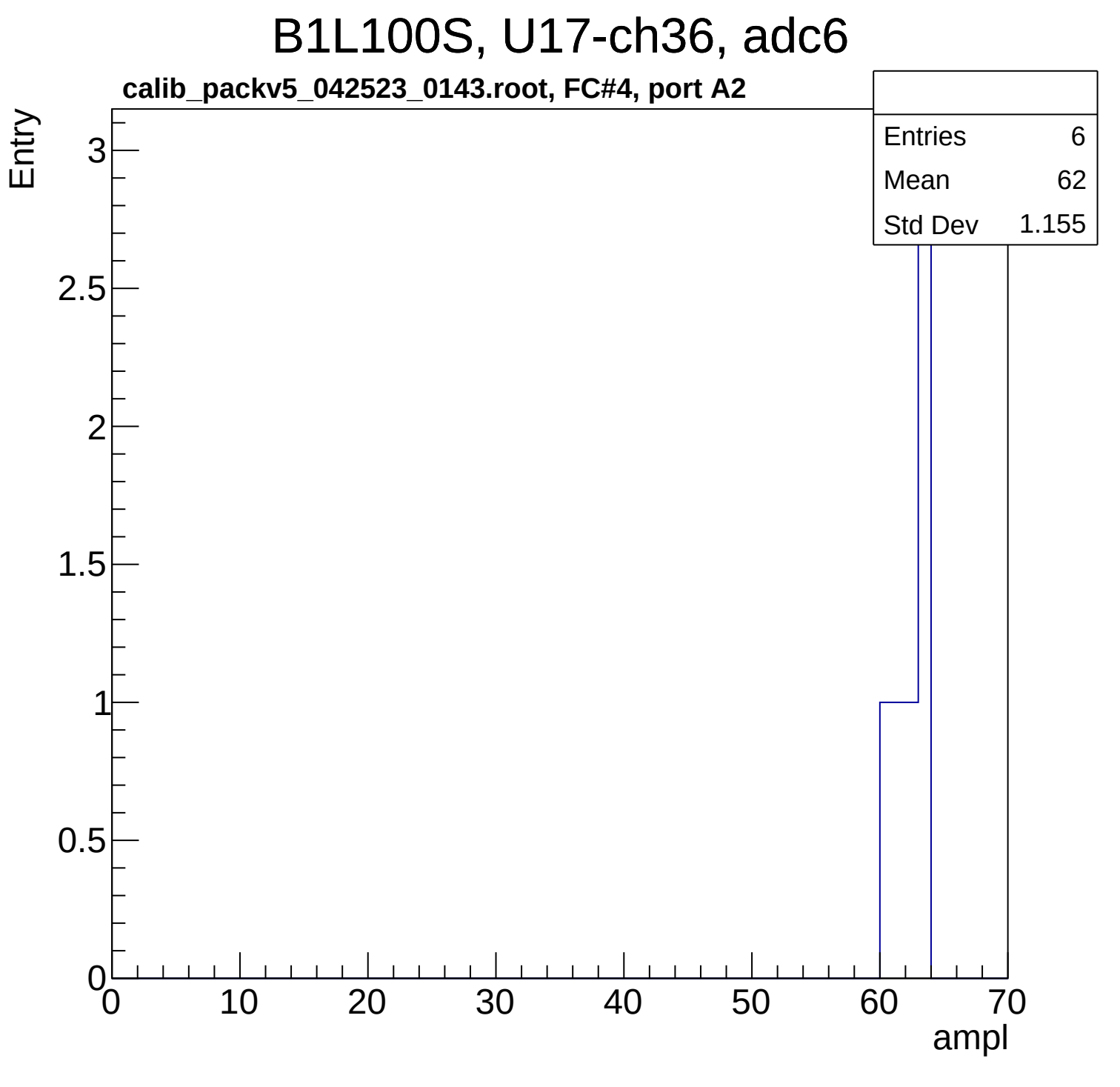
B1L100S, U17-ch36, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 6
Mean 62
Std Dev 1.155
Entry
ampl
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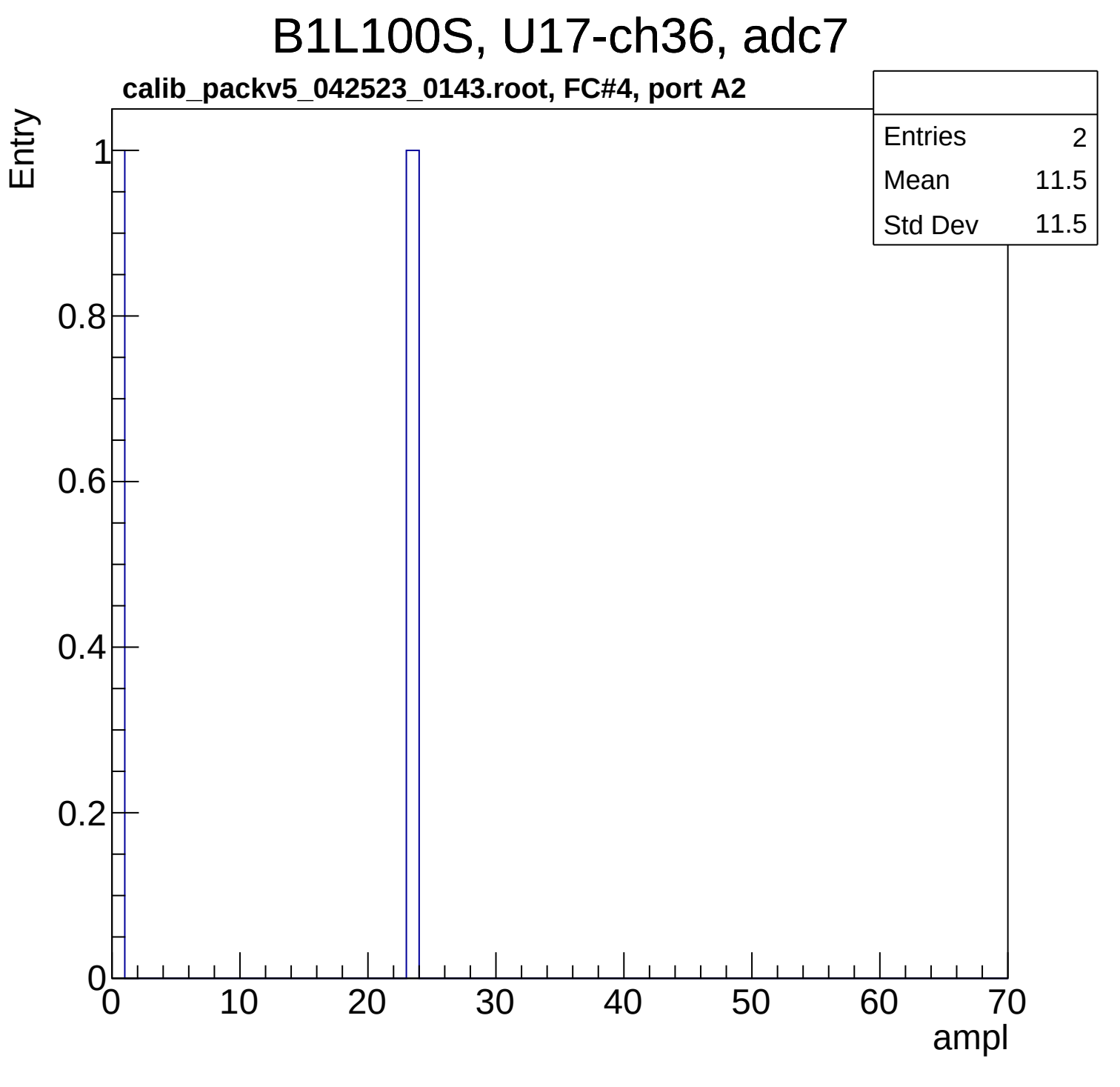
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L100S, U17-ch36, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 11.5
Std Dev 11.5
Entry
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0.6
0.4
0.2
0
0
10
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30
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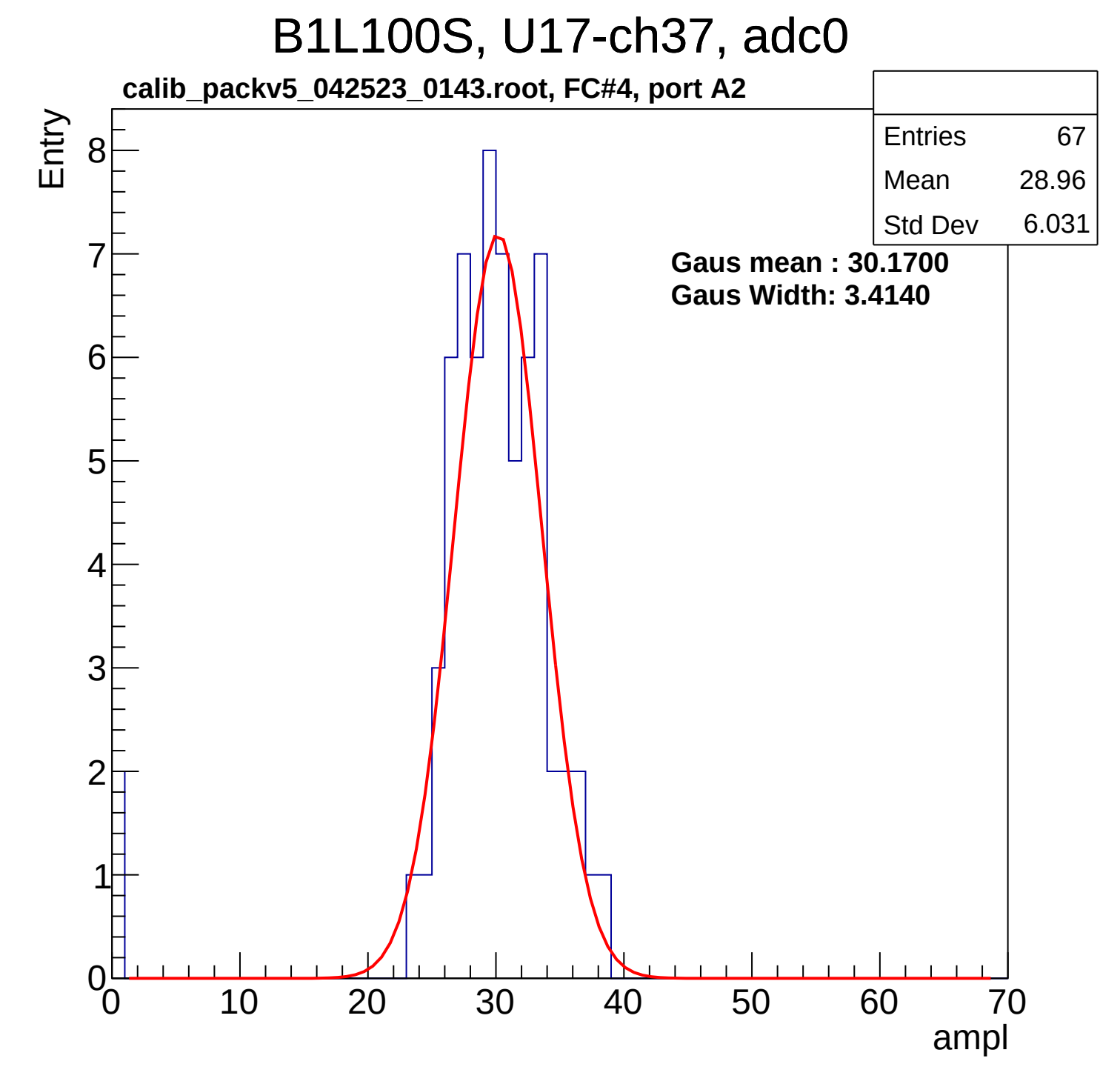
50
60
70
ampl


B1L100S, U17-ch37, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 28.96
Std Dev 6.031
Gaus mean : 30.1700
Gaus Width: 3.4140
Entry
ampl
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1
2
3
4
5
6
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8
0
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40
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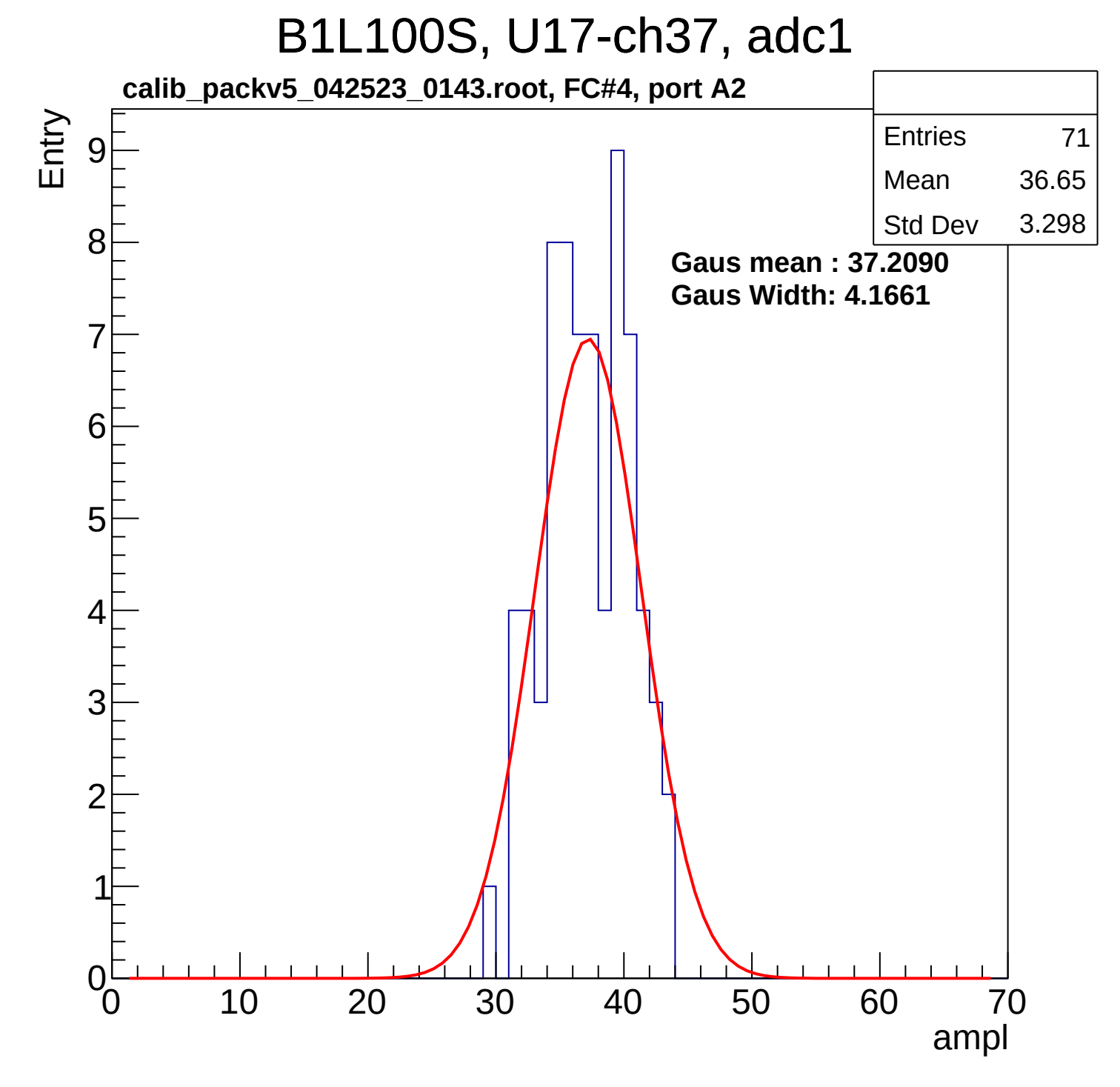
60
70


B1L100S, U17-ch37, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 36.65
Std Dev 3.298
Gaus mean : 37.2090
Gaus Width: 4.1661
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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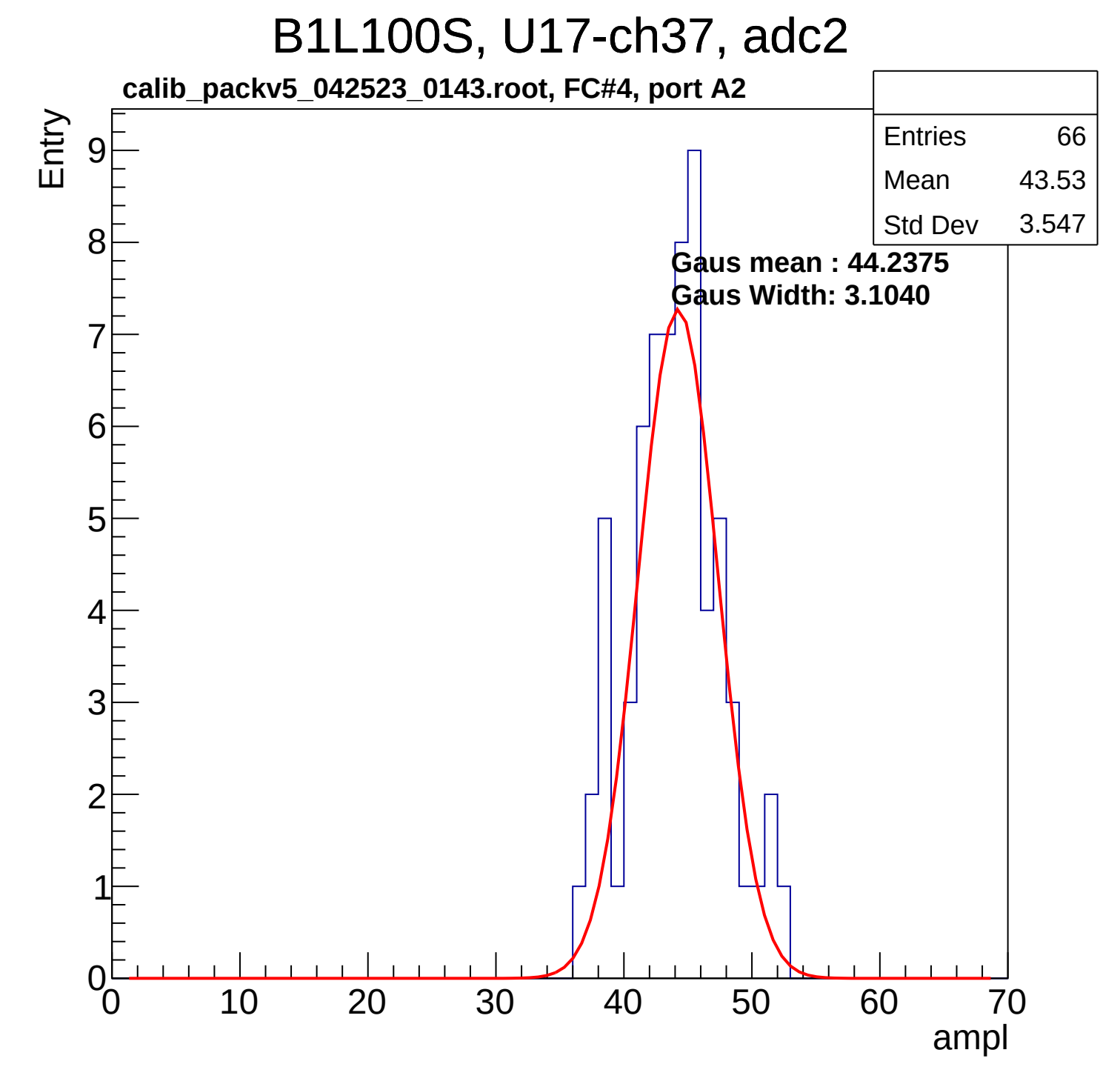
B1L100S, U17-ch37, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 43.53
Std Dev 3.547
Gaus mean : 44.2375
Gaus Width: 3.1040
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
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60
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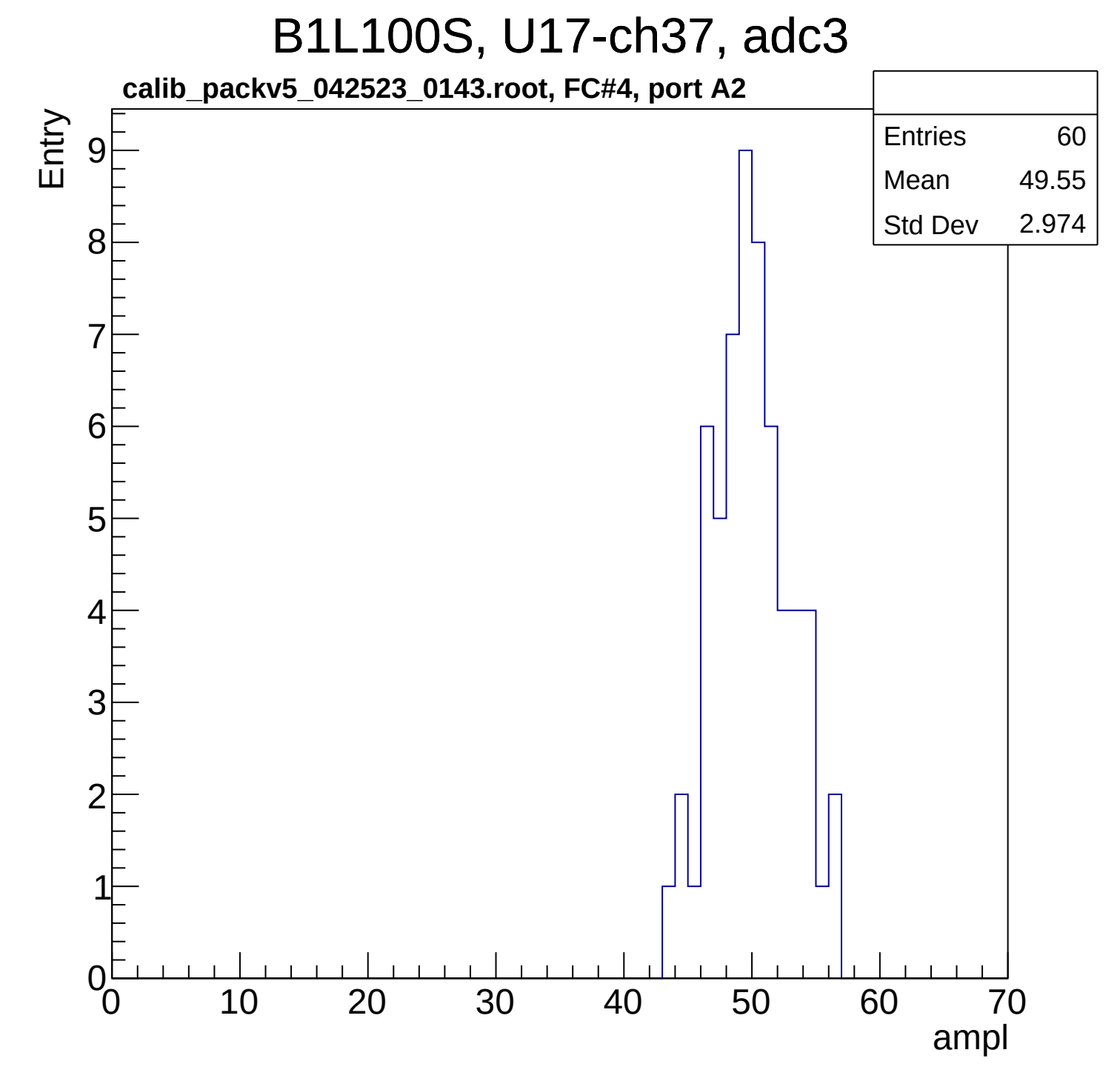
B1L100S, U17-ch37, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 49.55
Std Dev 2.974
Entry
ampl
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6
7
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0
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60
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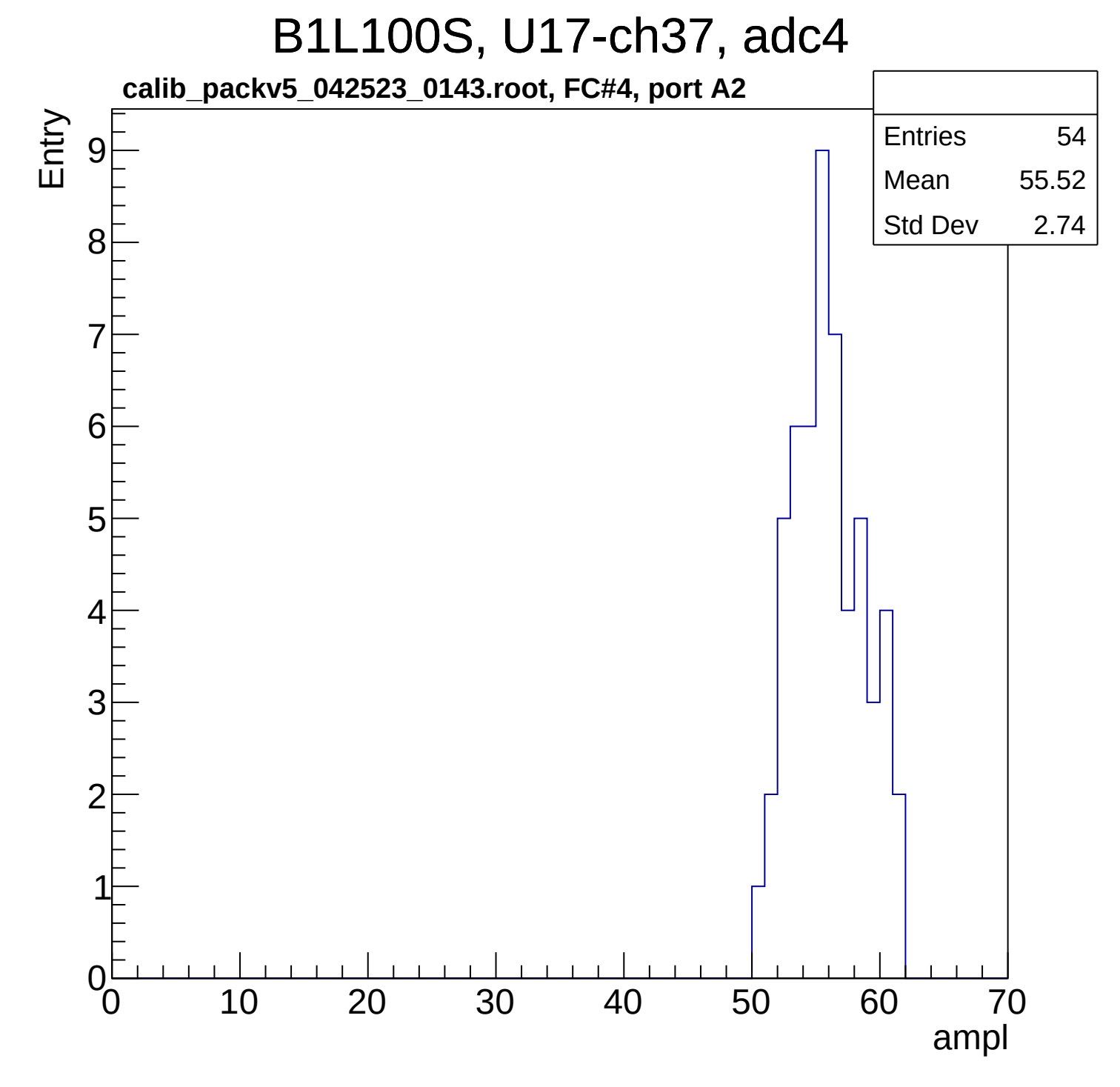
B1L100S, U17-ch37, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 55.52
Std Dev 2.74
Entry
ampl
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6
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0
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40
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60
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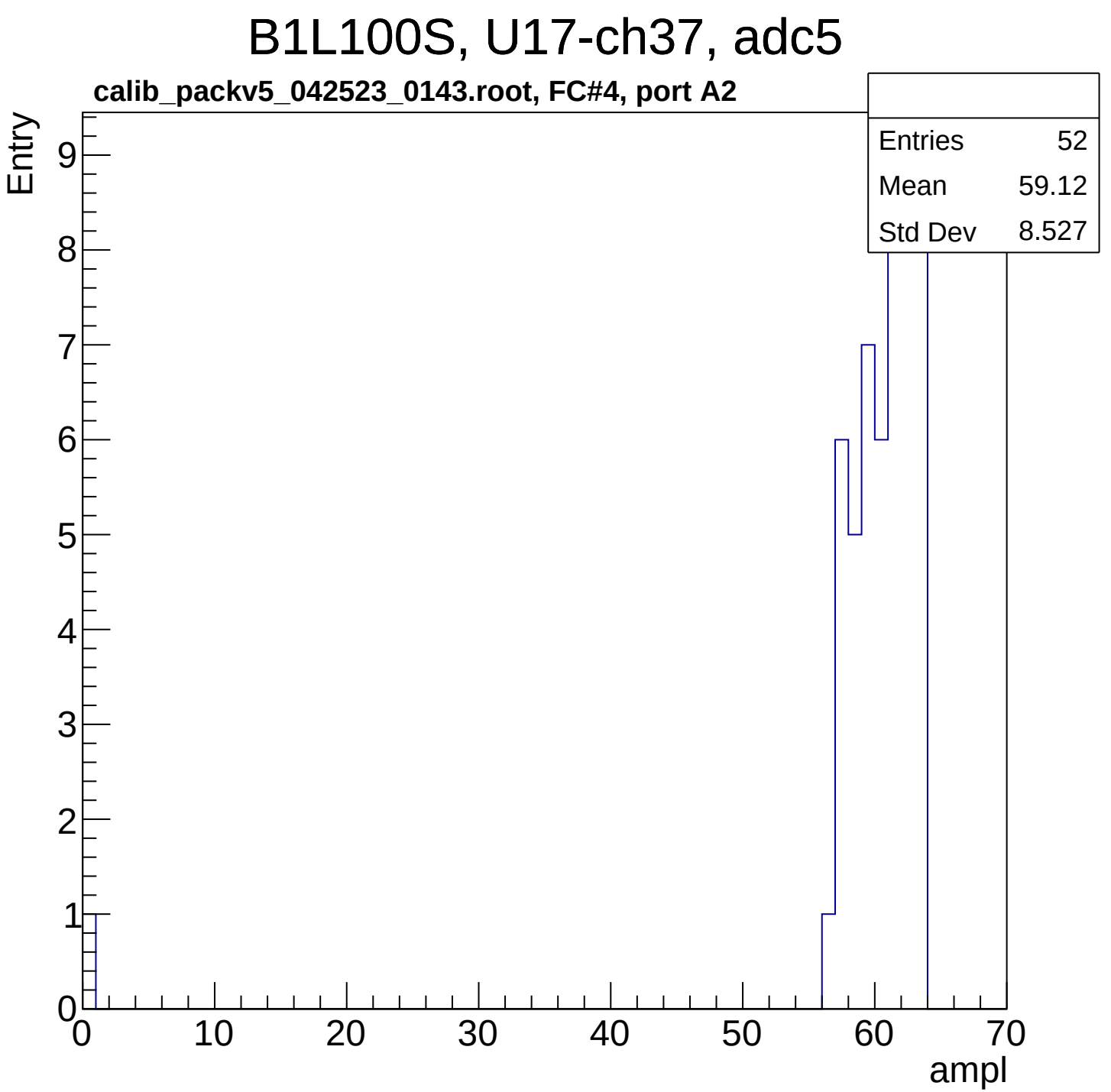
B1L100S, U17-ch37, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 52
Mean 59.12
Std Dev 8.527
Entry
ampl
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3
4
5
6
7
8
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0
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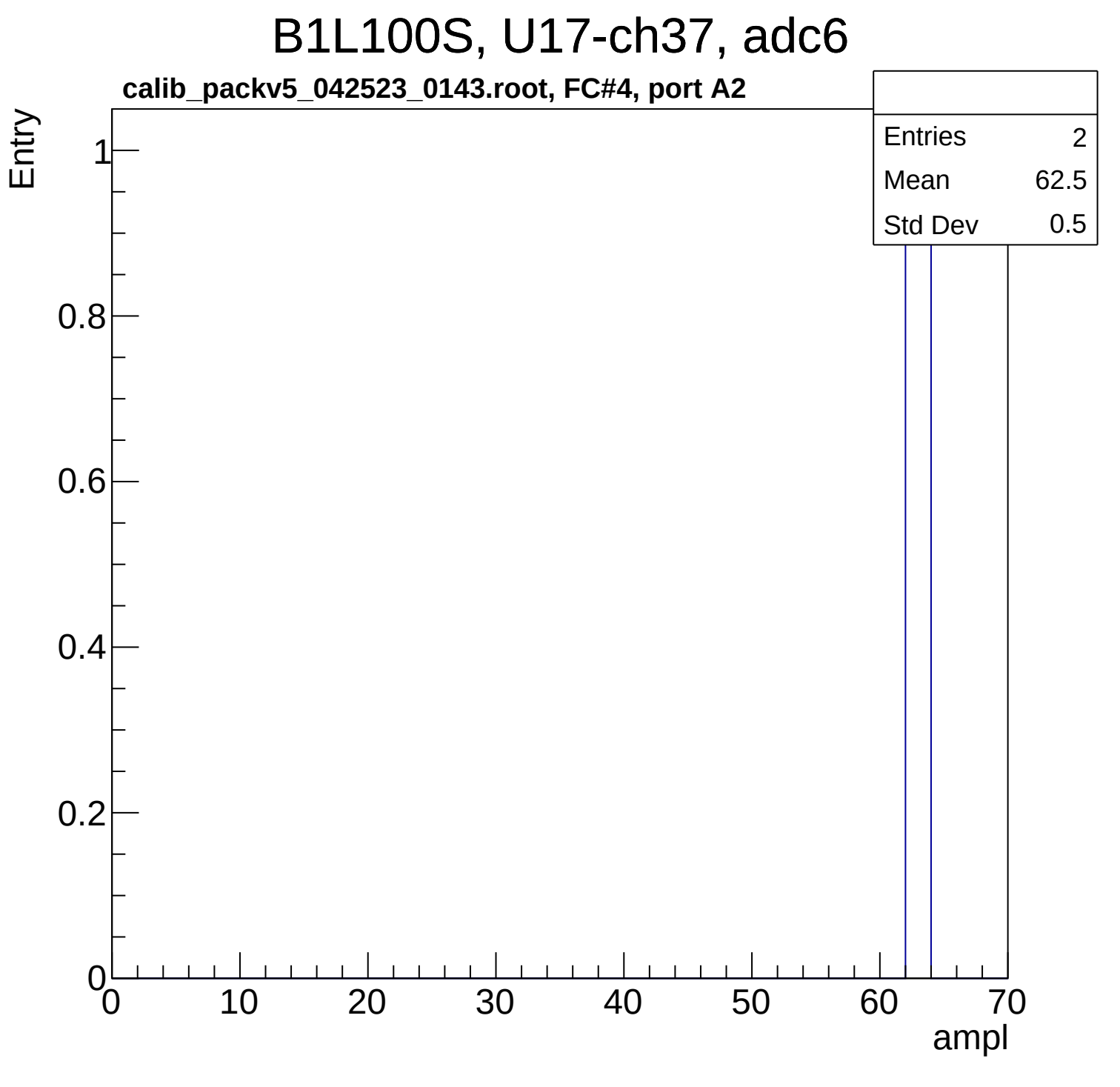
B1L100S, U17-ch37, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
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0.6
0.4
0.2
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0
10
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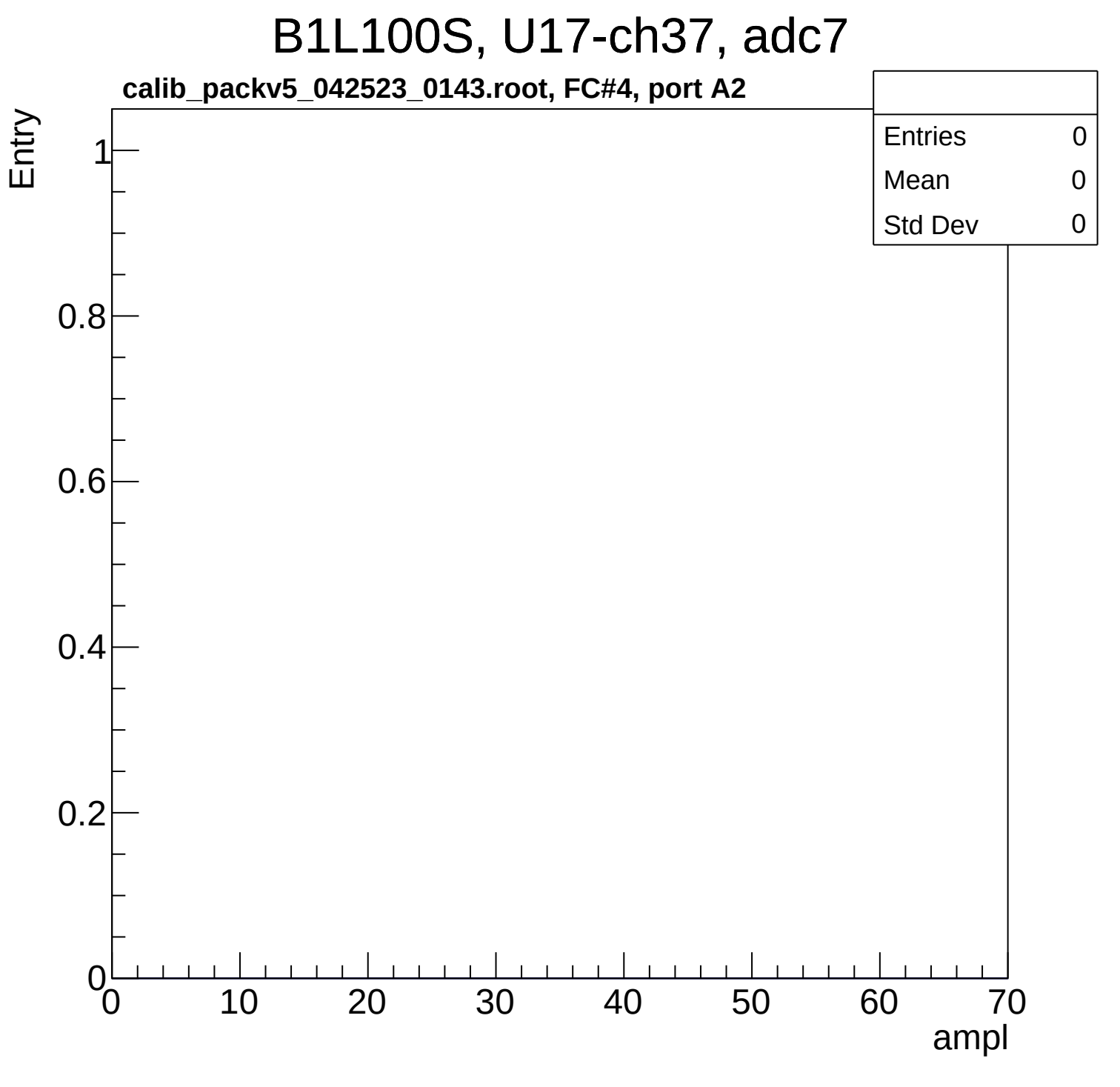
50
60
70
ampl


B1L100S, U17-ch37, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
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0.6
0.4
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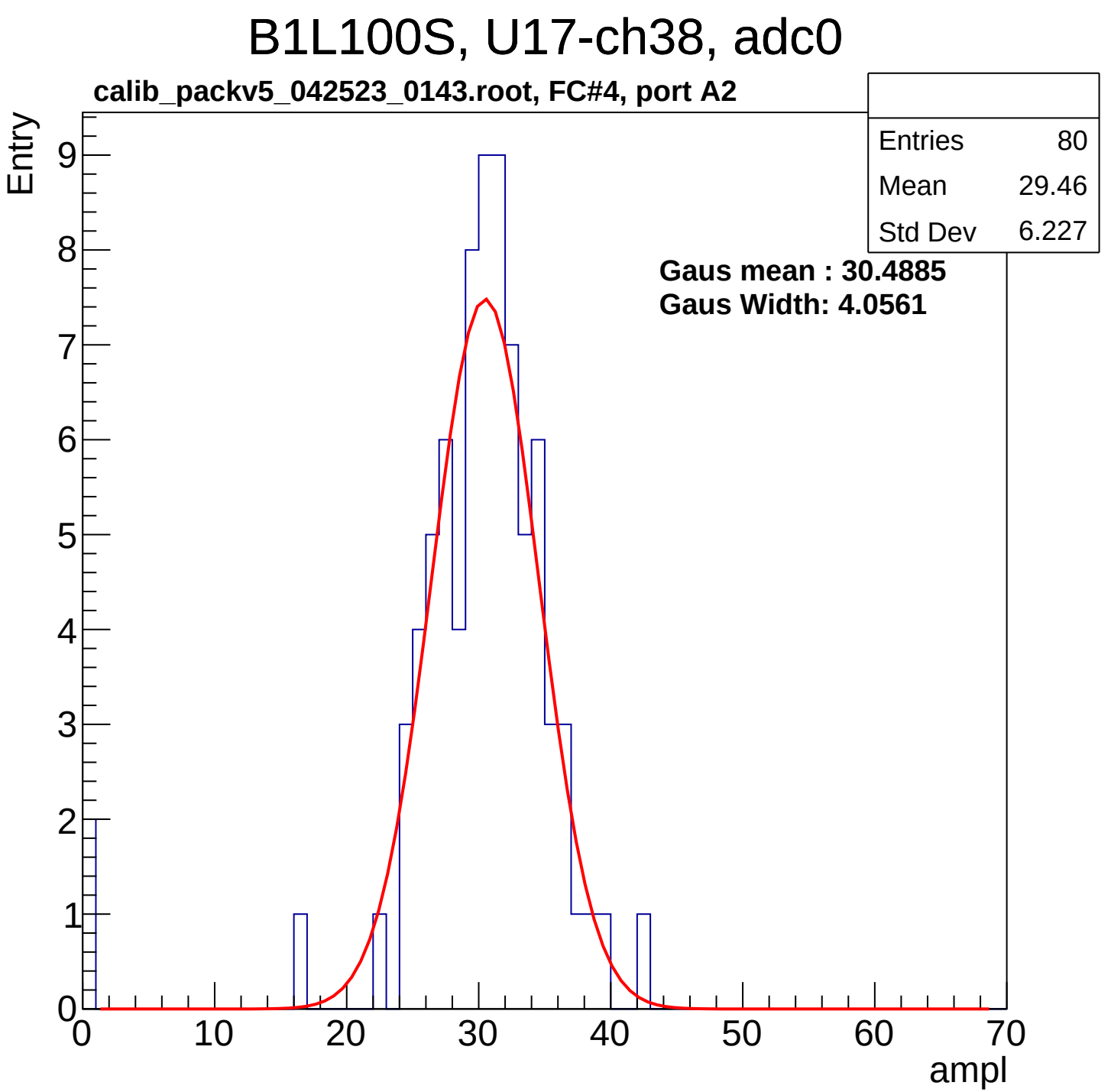
50
60
70
ampl


B1L100S, U17-ch38, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 80
Mean 29.46
Std Dev 6.227
Gaus mean : 30.4885
Gaus Width: 4.0561
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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60
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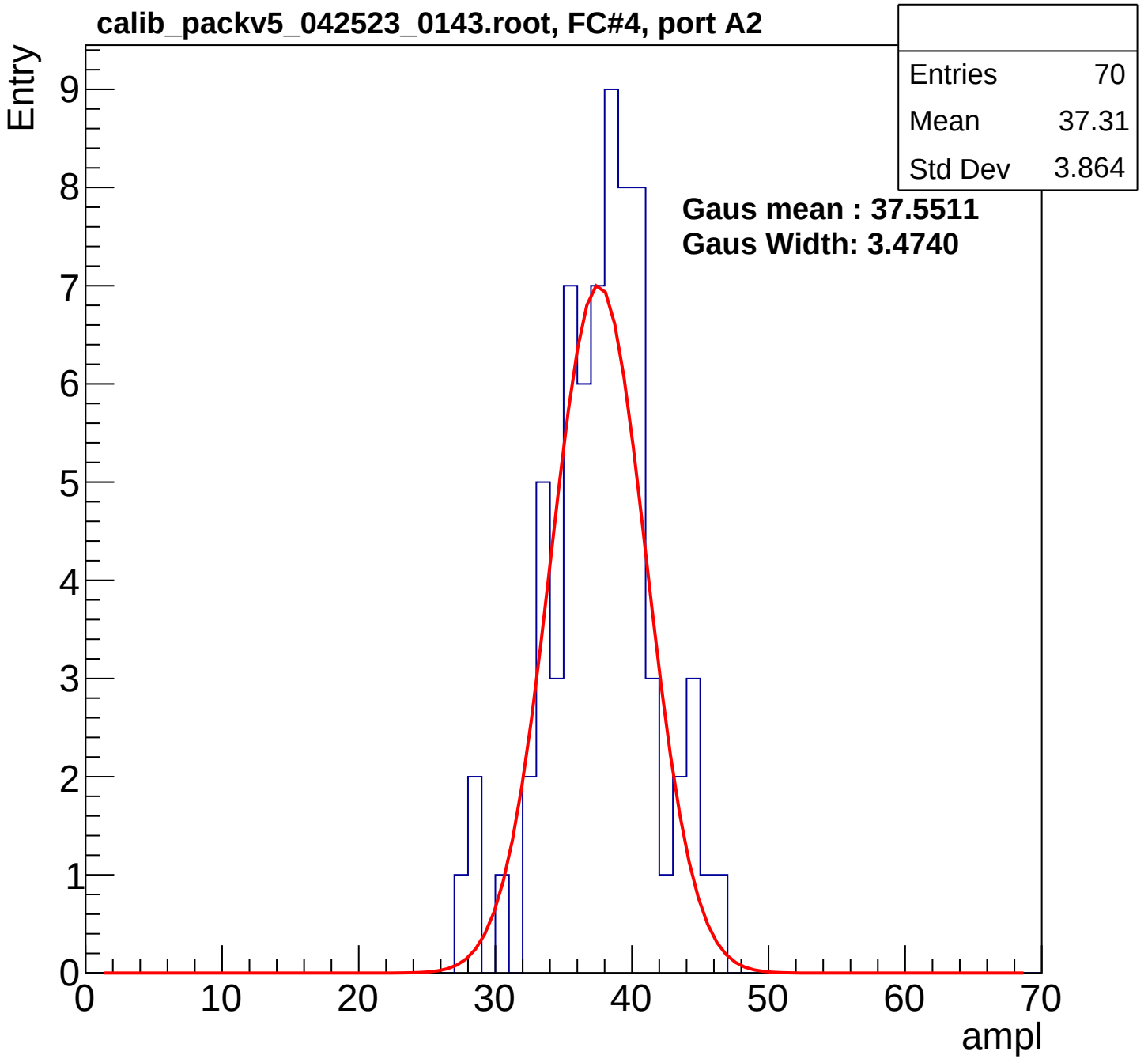
B1L100S, U17-ch38, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 37.31
Std Dev 3.864
Gaus mean : 37.5511
Gaus Width: 3.4740
Entry
ampl
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3
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7
8
9
0
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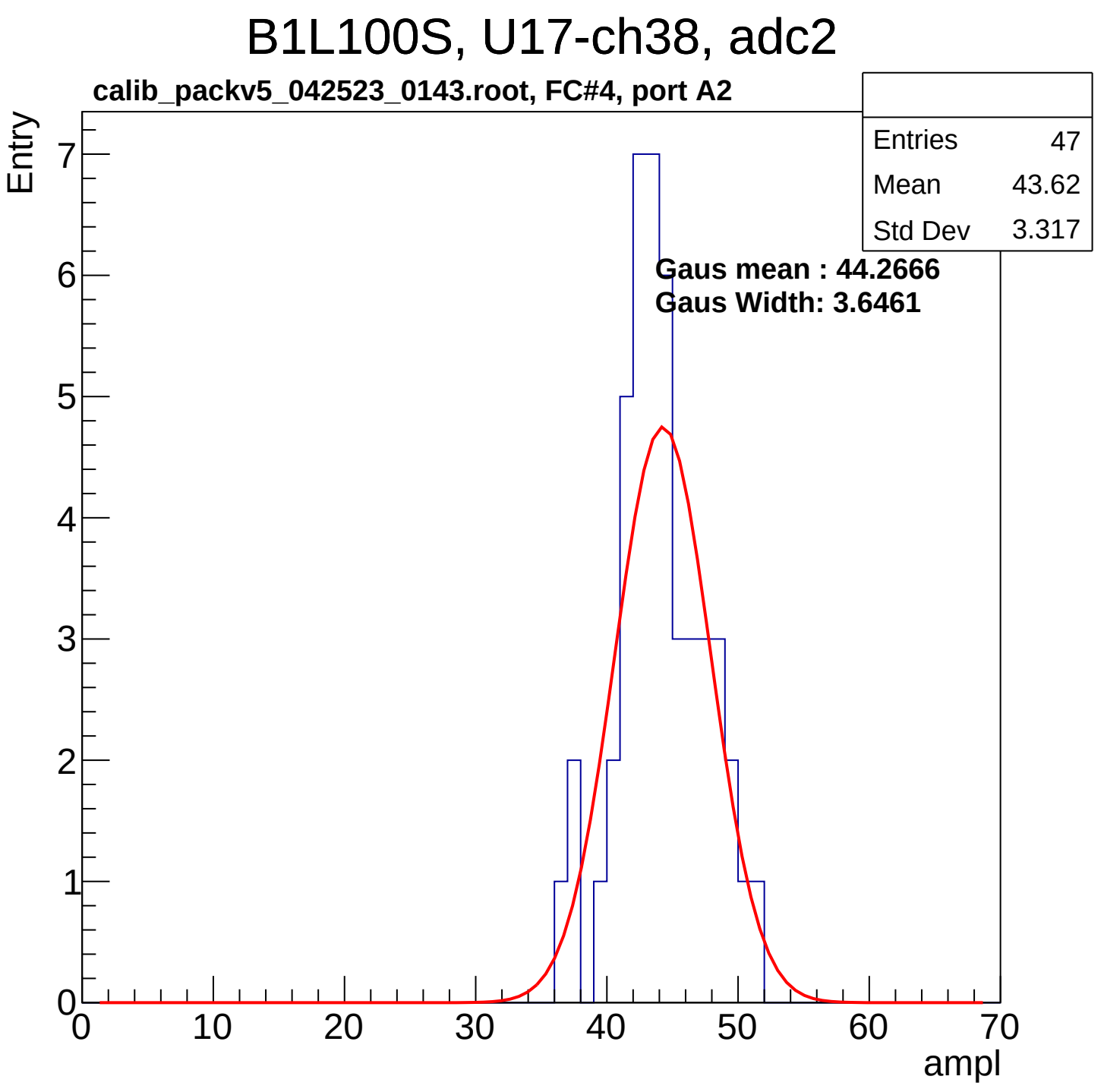
B1L100S, U17-ch38, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 47
Mean 43.62
Std Dev 3.317
Gaus mean : 44.2666
Gaus Width: 3.6461
Entry
ampl
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2
3
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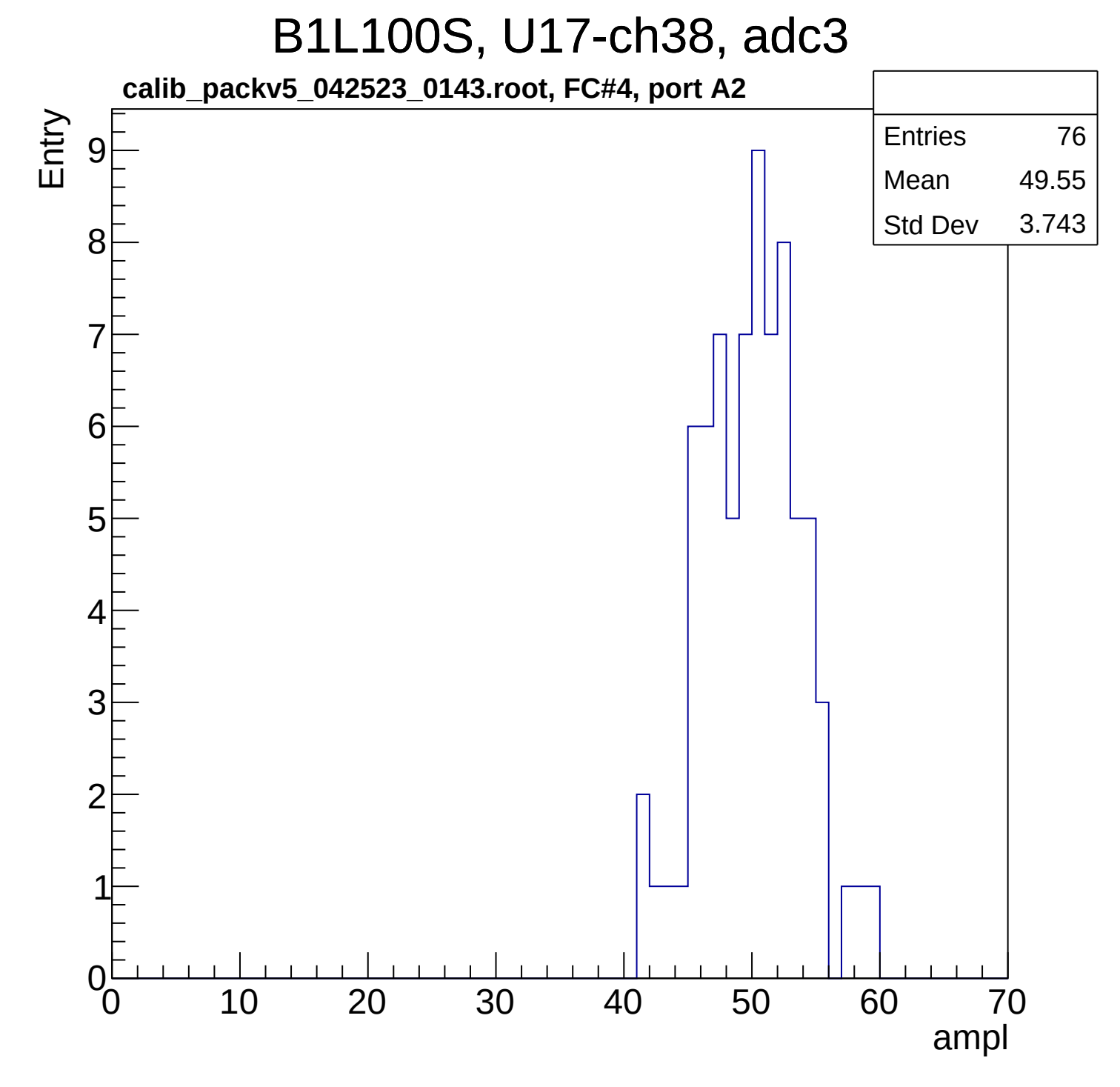
B1L100S, U17-ch38, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 76
Mean 49.55
Std Dev 3.743
Entry
ampl
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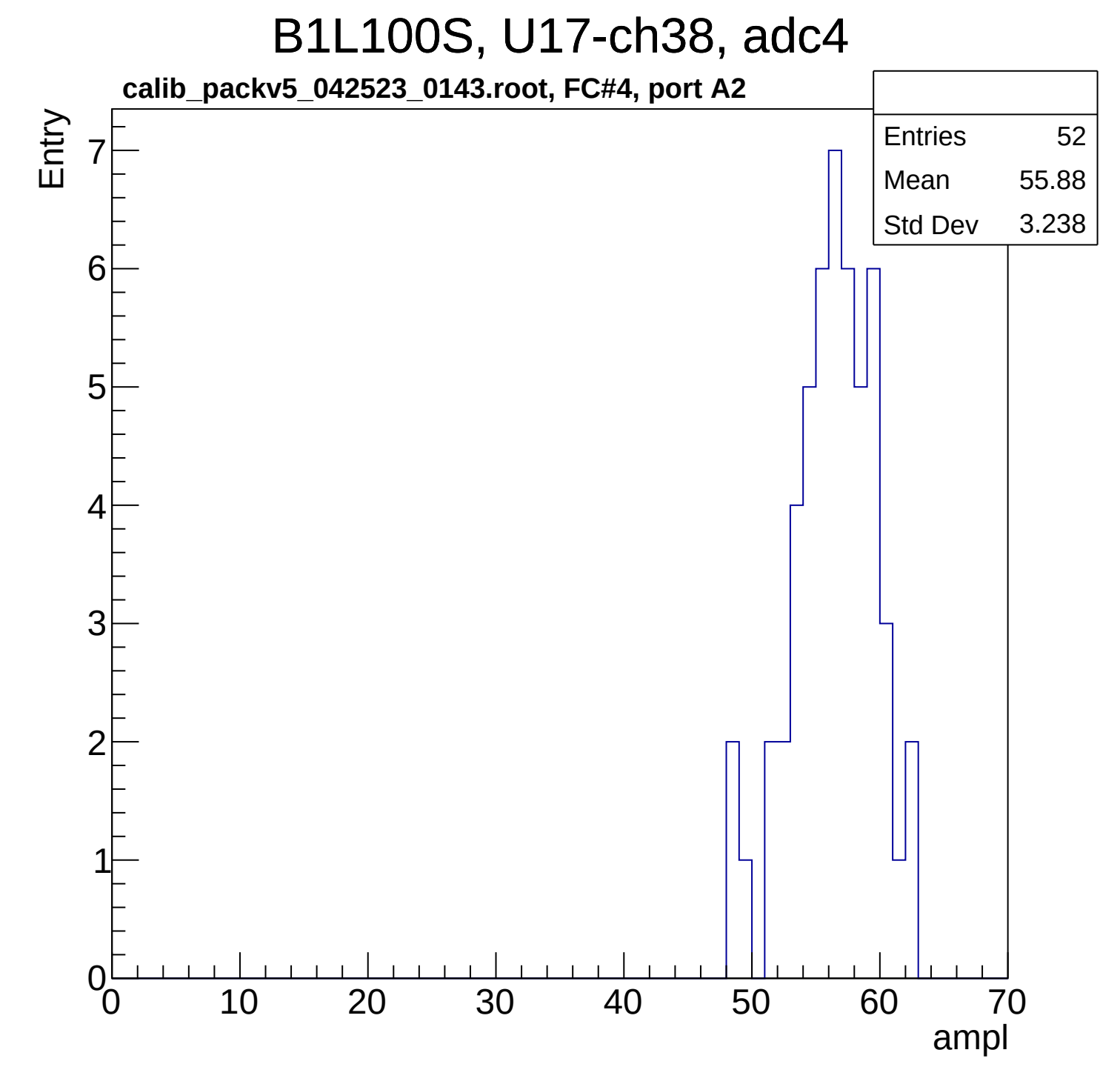
B1L100S, U17-ch38, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 52
Mean 55.88
Std Dev 3.238
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
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50
60
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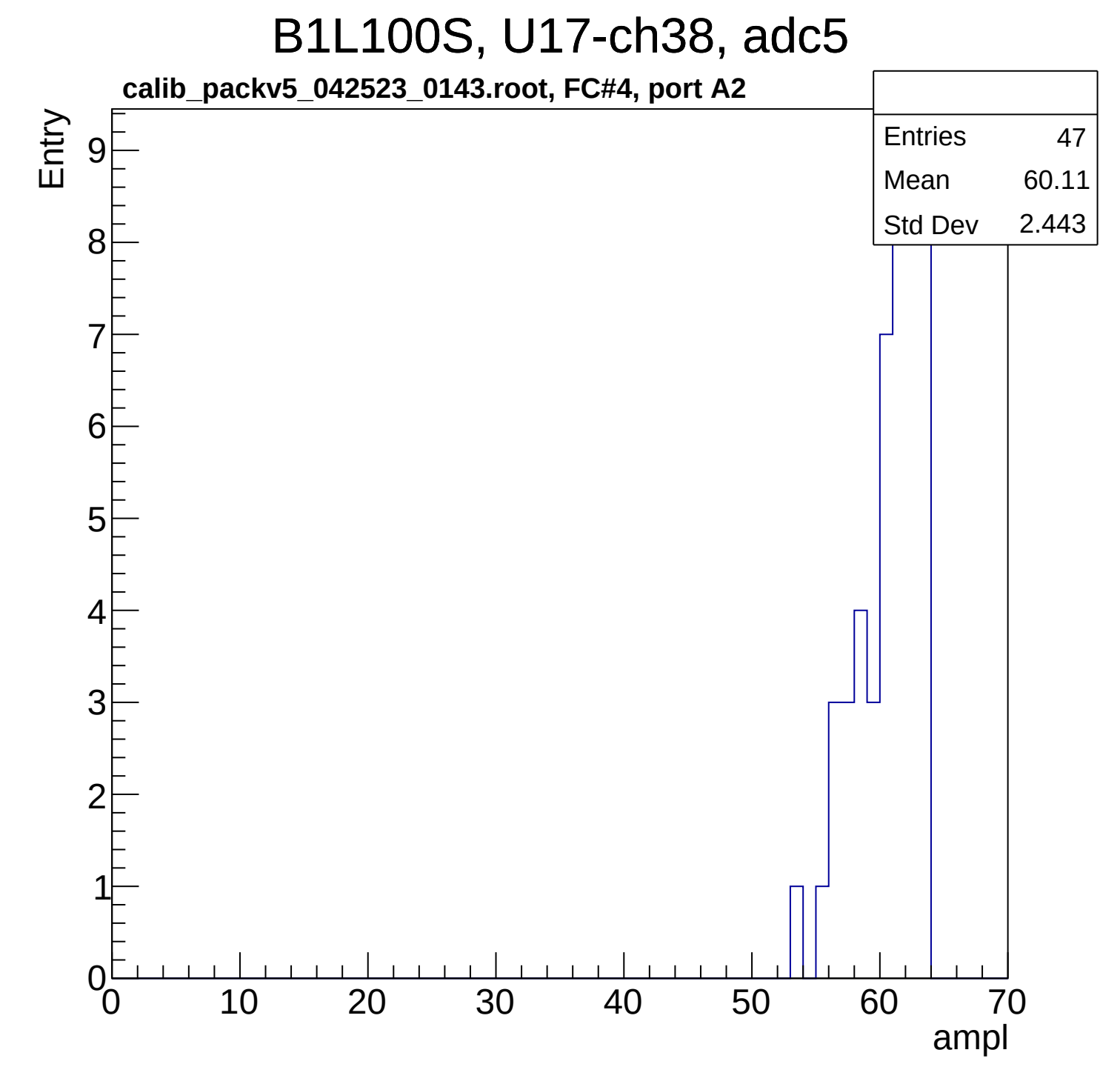
B1L100S, U17-ch38, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 47
Mean 60.11
Std Dev 2.443
Entry
ampl
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2
3
4
5
6
7
8
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0
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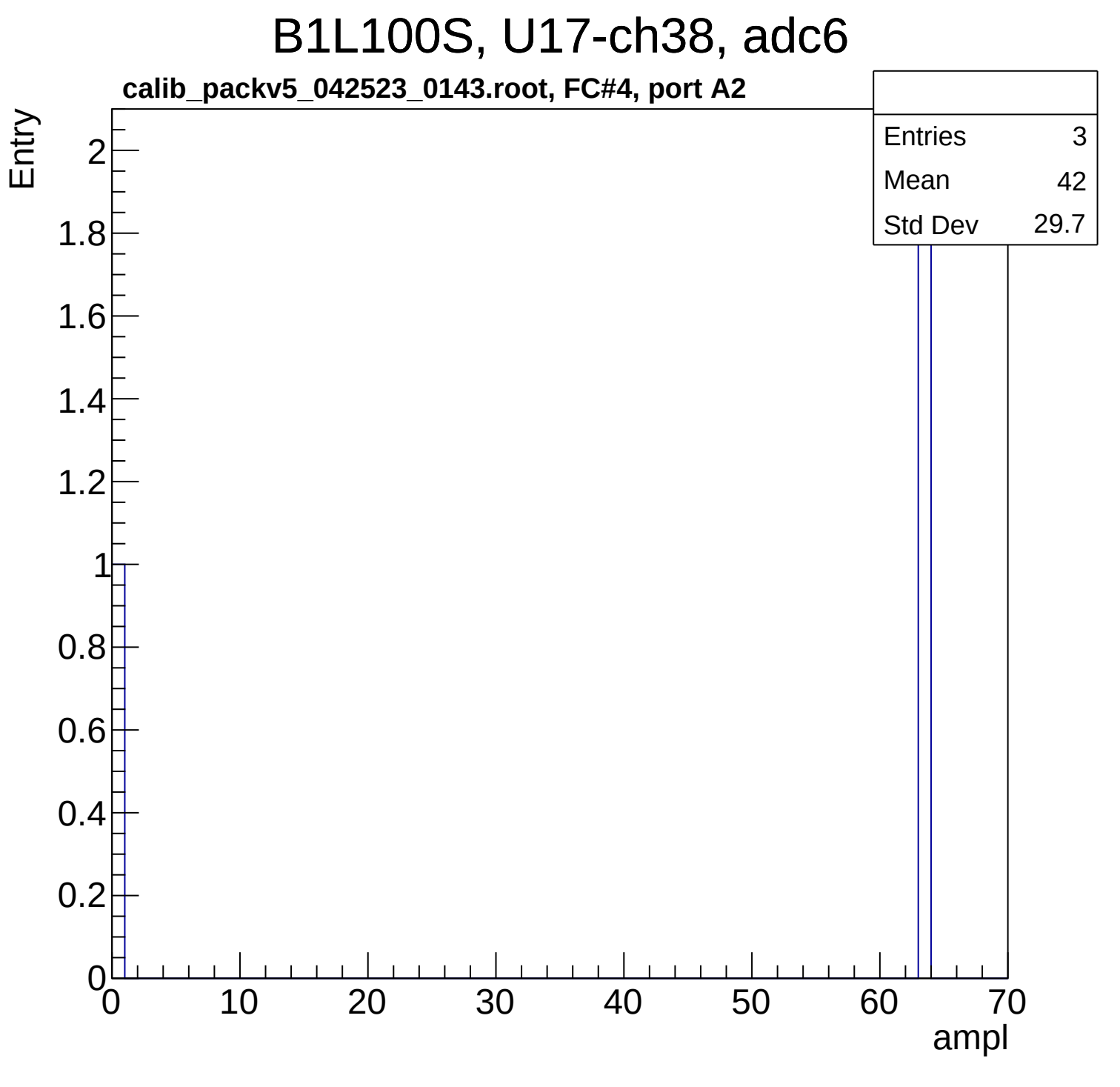
B1L100S, U17-ch38, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 42
Std Dev 29.7
Entry
ampl
0
0.2
0.4
0.6
0.8
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1.2
1.4
1.6
1.8
2
0
10
20
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40
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60
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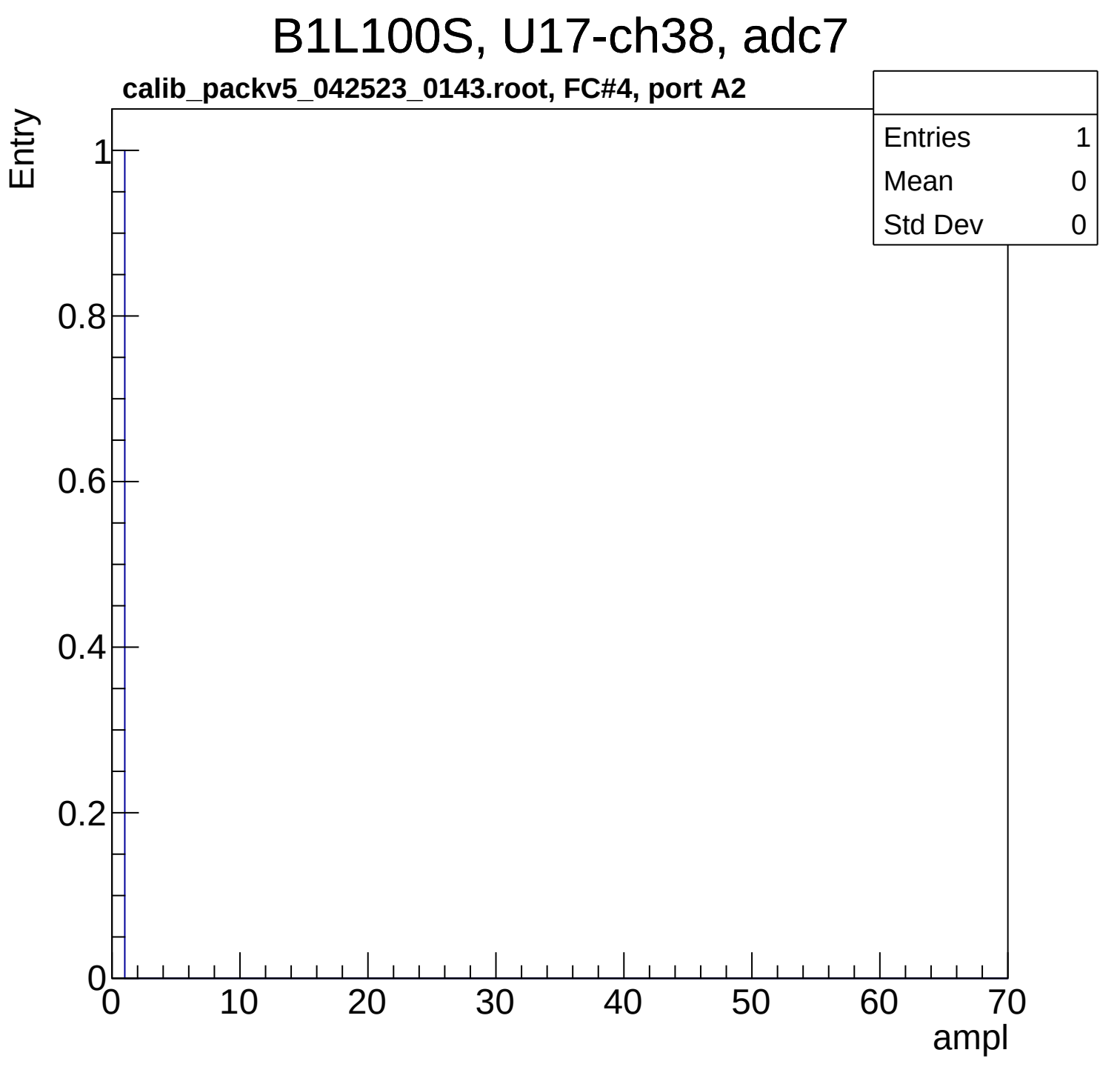
B1L100S, U17-ch38, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
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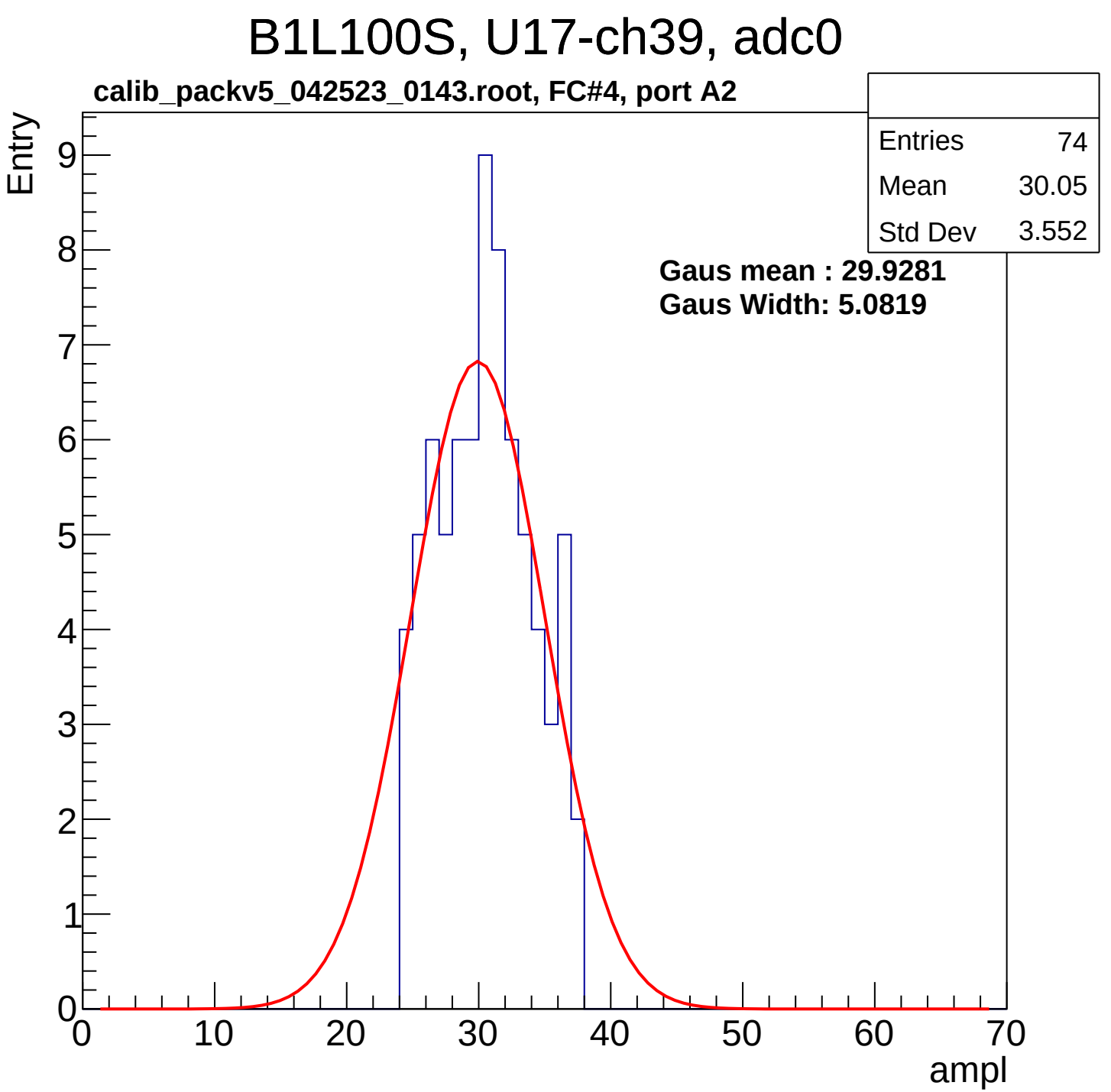
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch39, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 74
Mean 30.05
Std Dev 3.552
Gaus mean : 29.9281
Gaus Width: 5.0819
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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60
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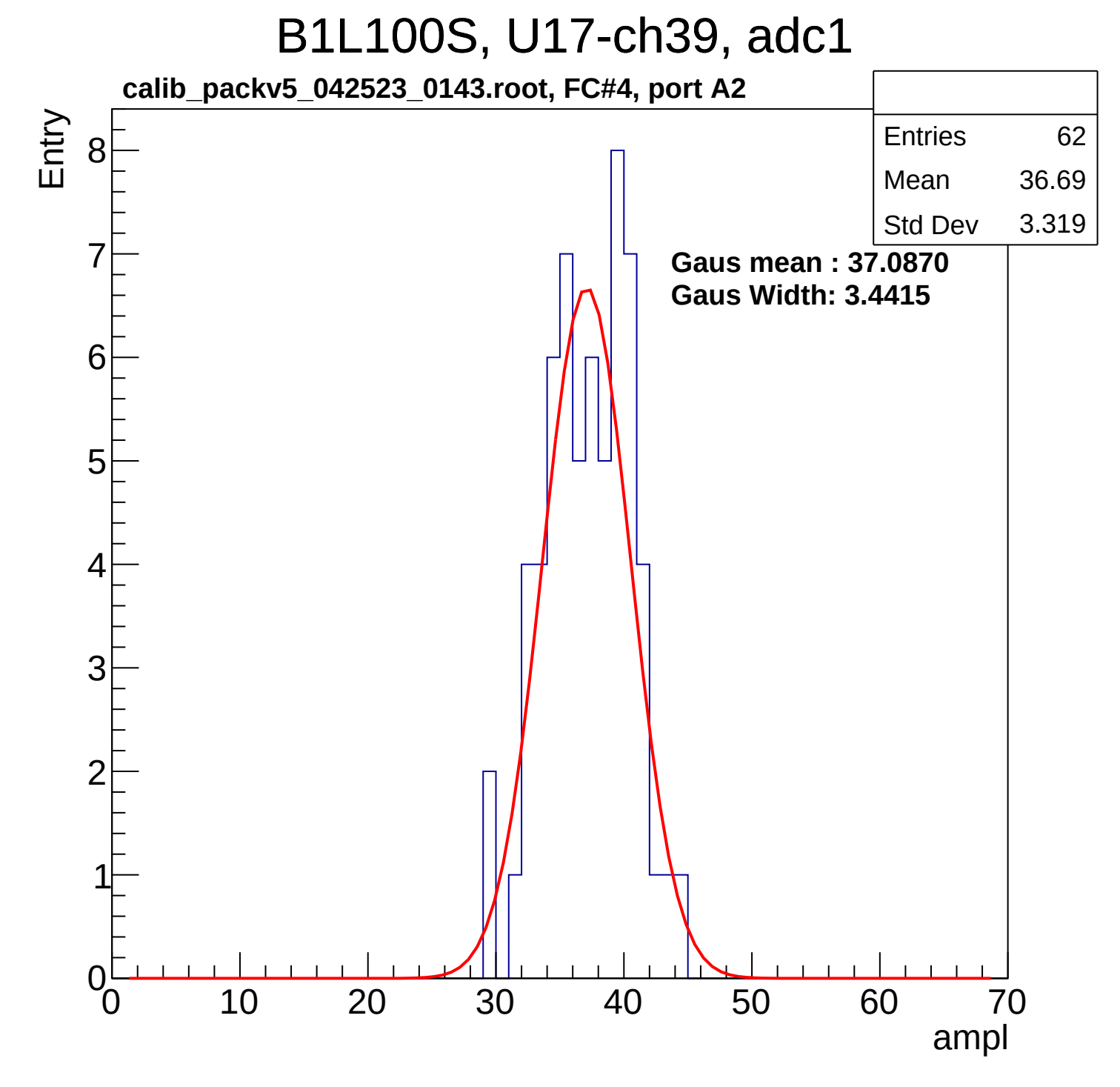
B1L100S, U17-ch39, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 36.69
Std Dev 3.319
Gaus mean : 37.0870
Gaus Width: 3.4415
Entry
ampl
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1
2
3
4
5
6
7
8
0
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40
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60
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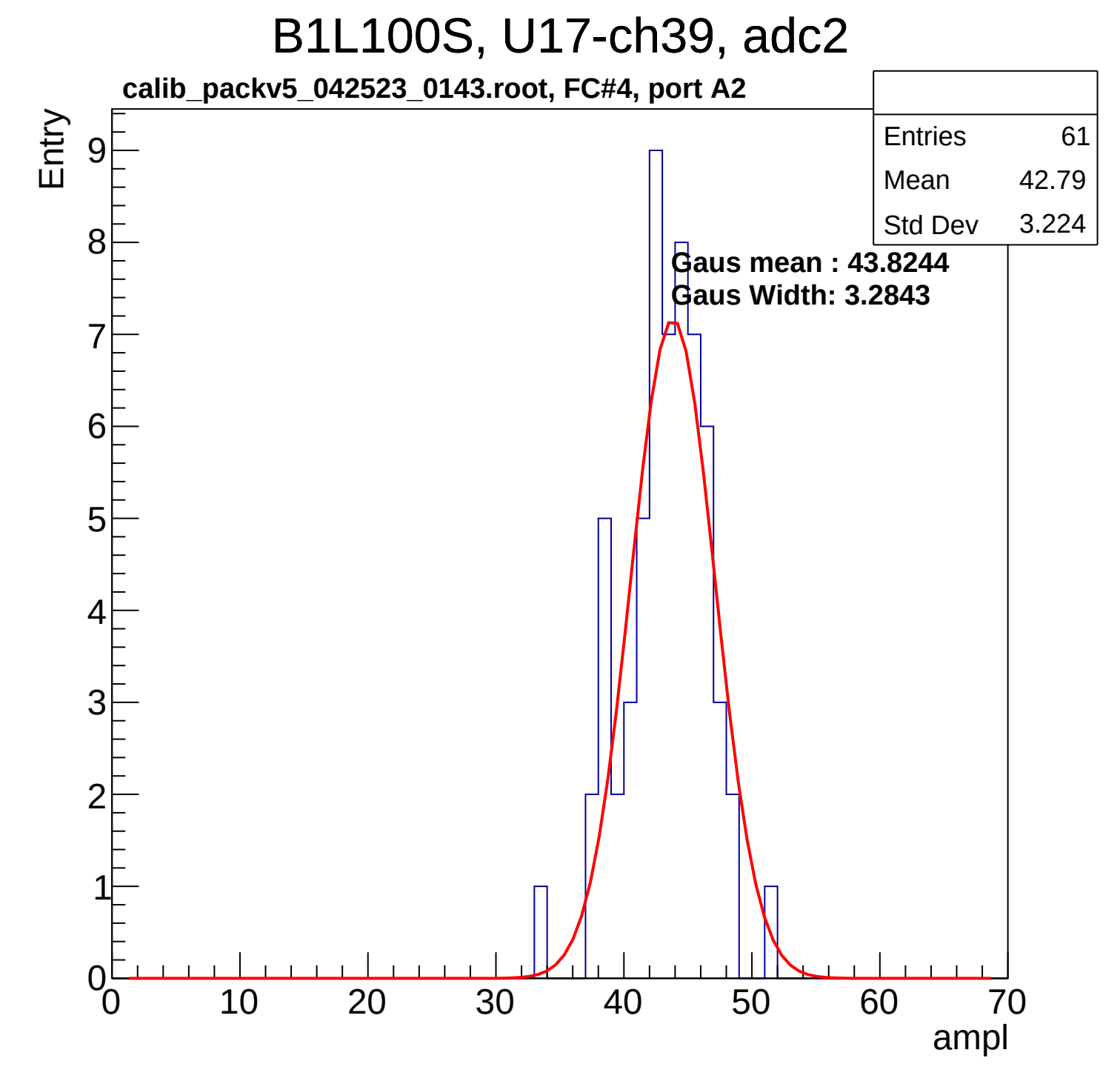
B1L100S, U17-ch39, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 42.79
Std Dev 3.224
Gaus mean : 43.8244
Gaus Width: 3.2843
Entry
ampl
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2
3
4
5
6
7
8
9
0
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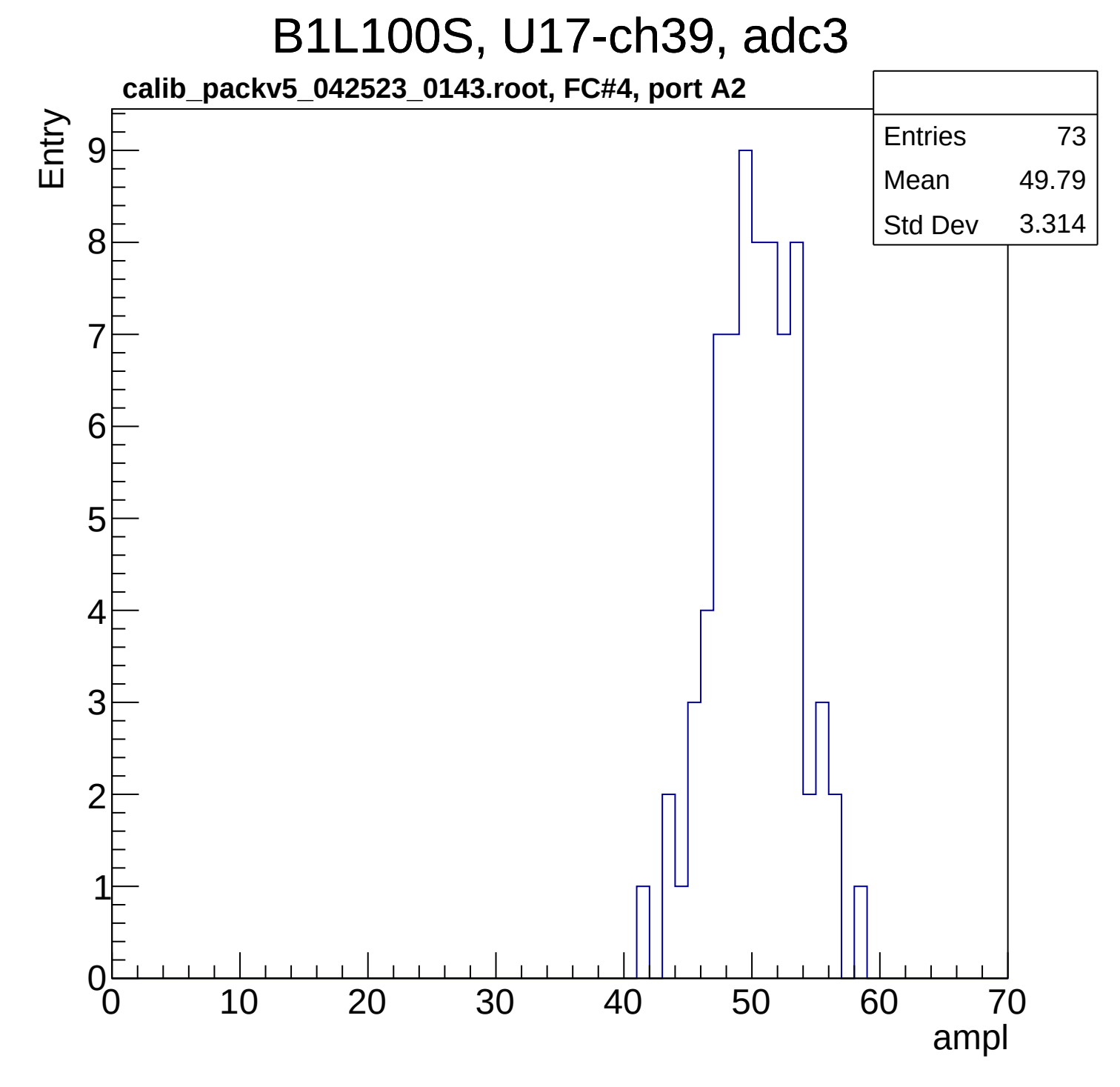
B1L100S, U17-ch39, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 49.79
Std Dev 3.314
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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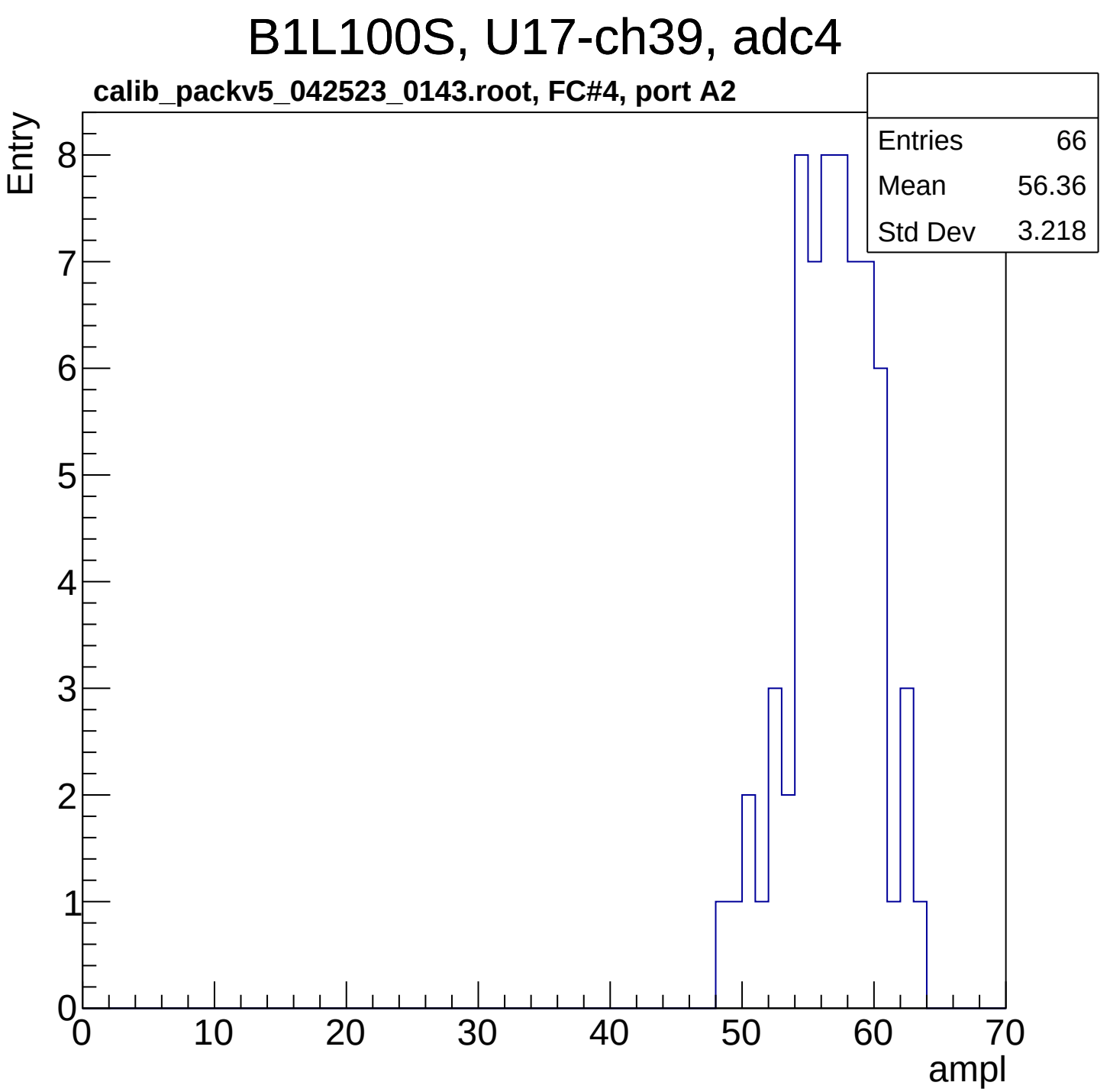
B1L100S, U17-ch39, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 56.36
Std Dev 3.218
Entry
ampl
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1
2
3
4
5
6
7
8
0
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40
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60
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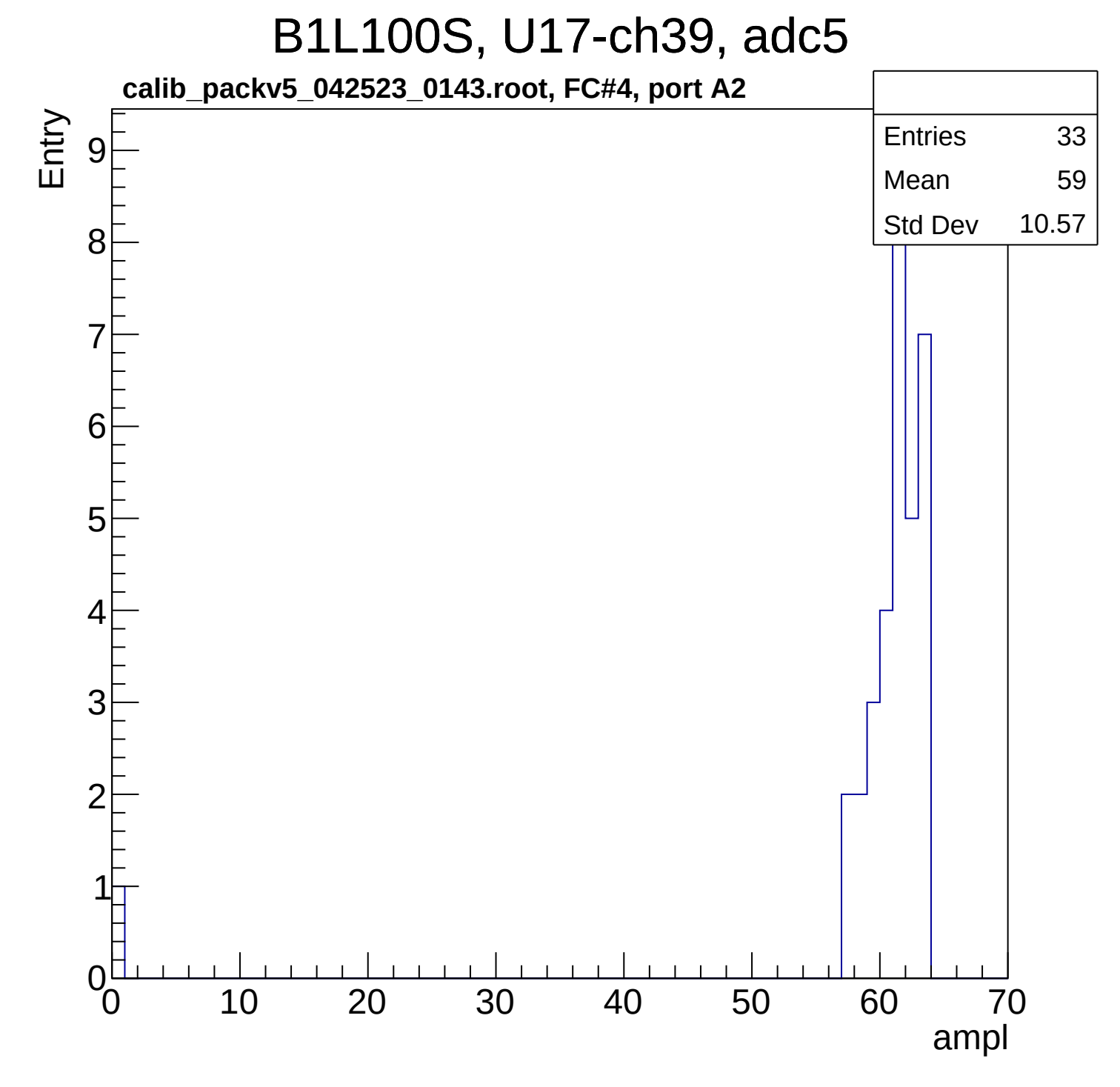
B1L100S, U17-ch39, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 33
Mean 59
Std Dev 10.57
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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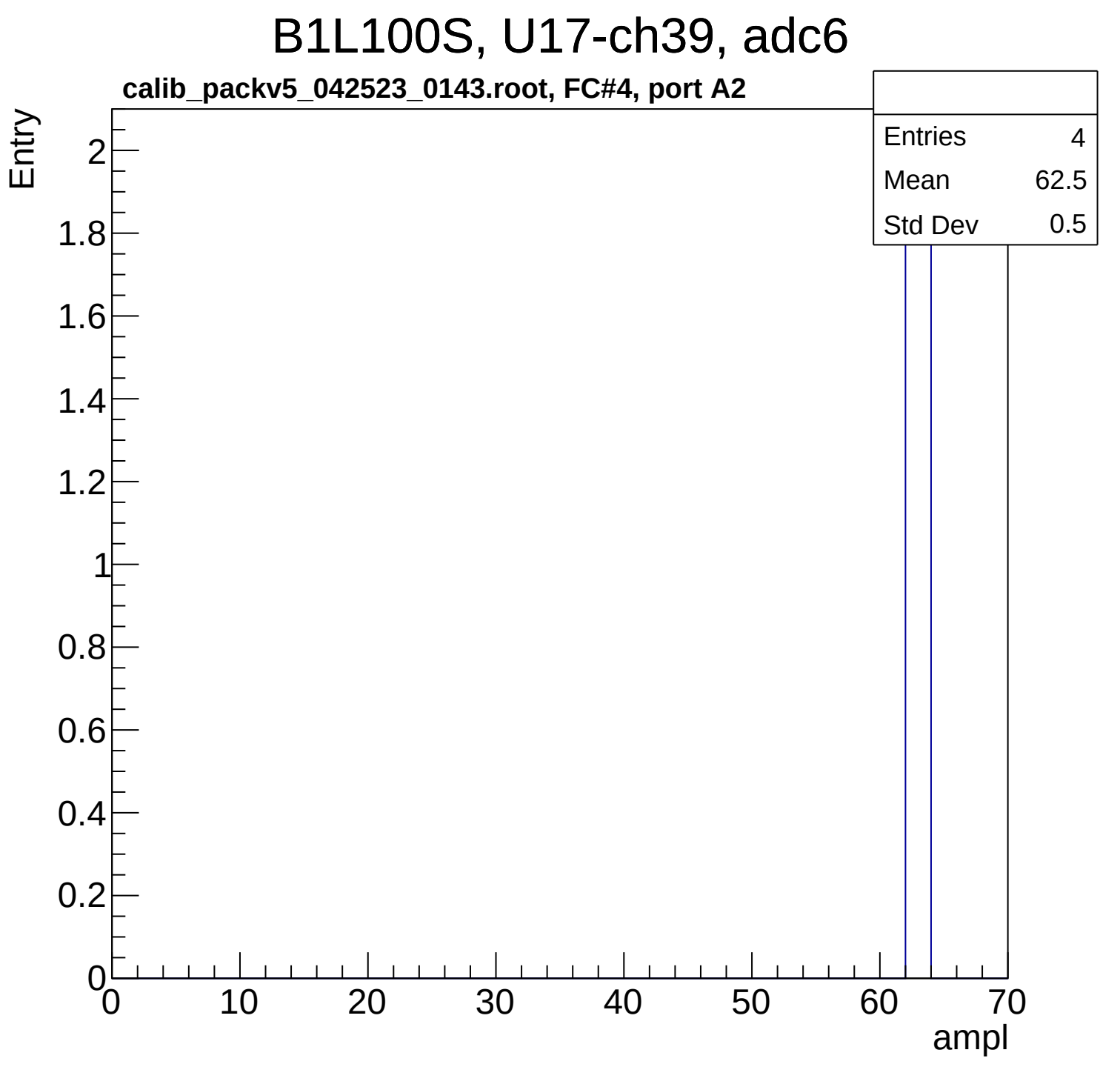
B1L100S, U17-ch39, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 4
Mean 62.5
Std Dev 0.5
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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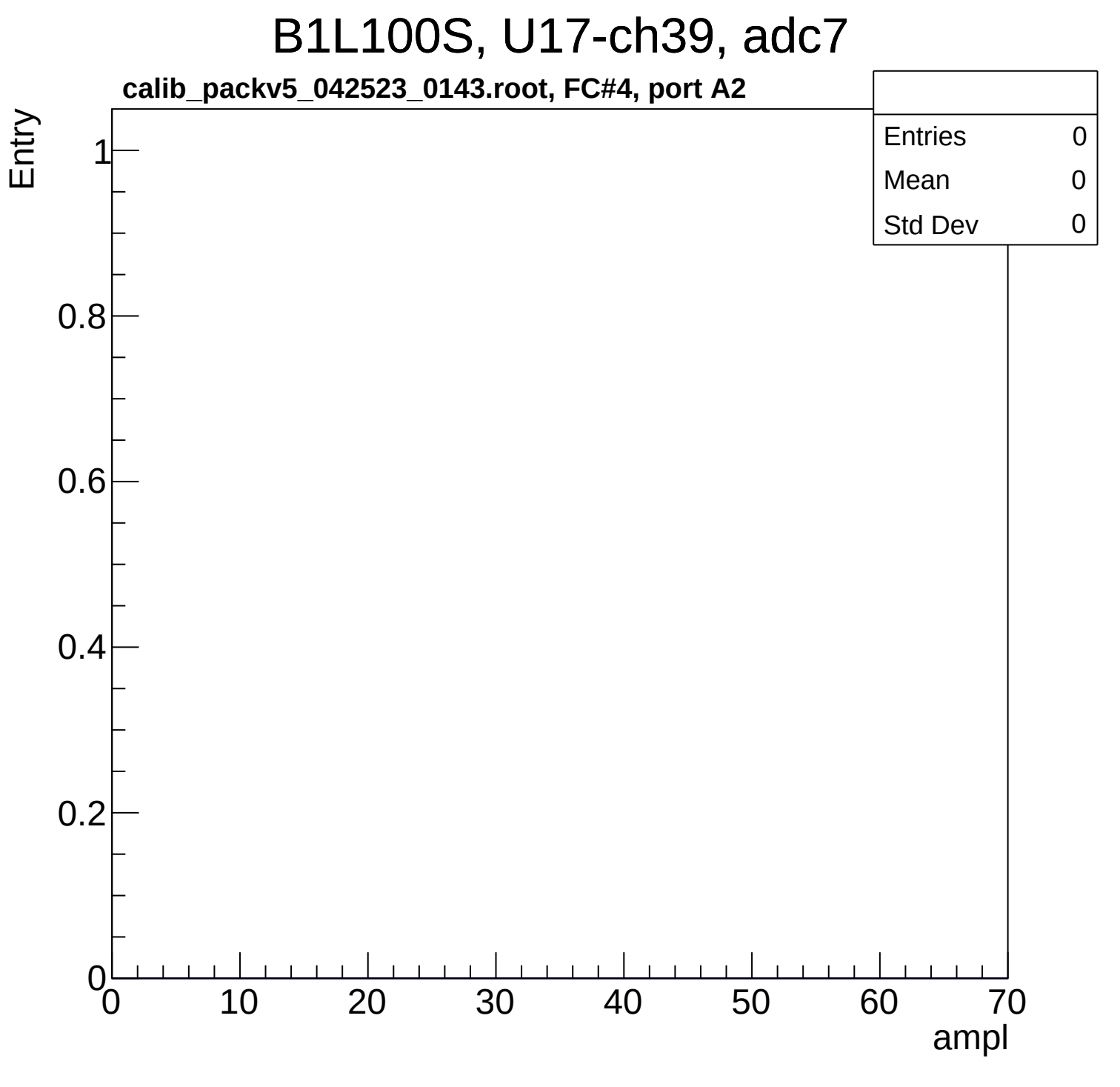
B1L100S, U17-ch39, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
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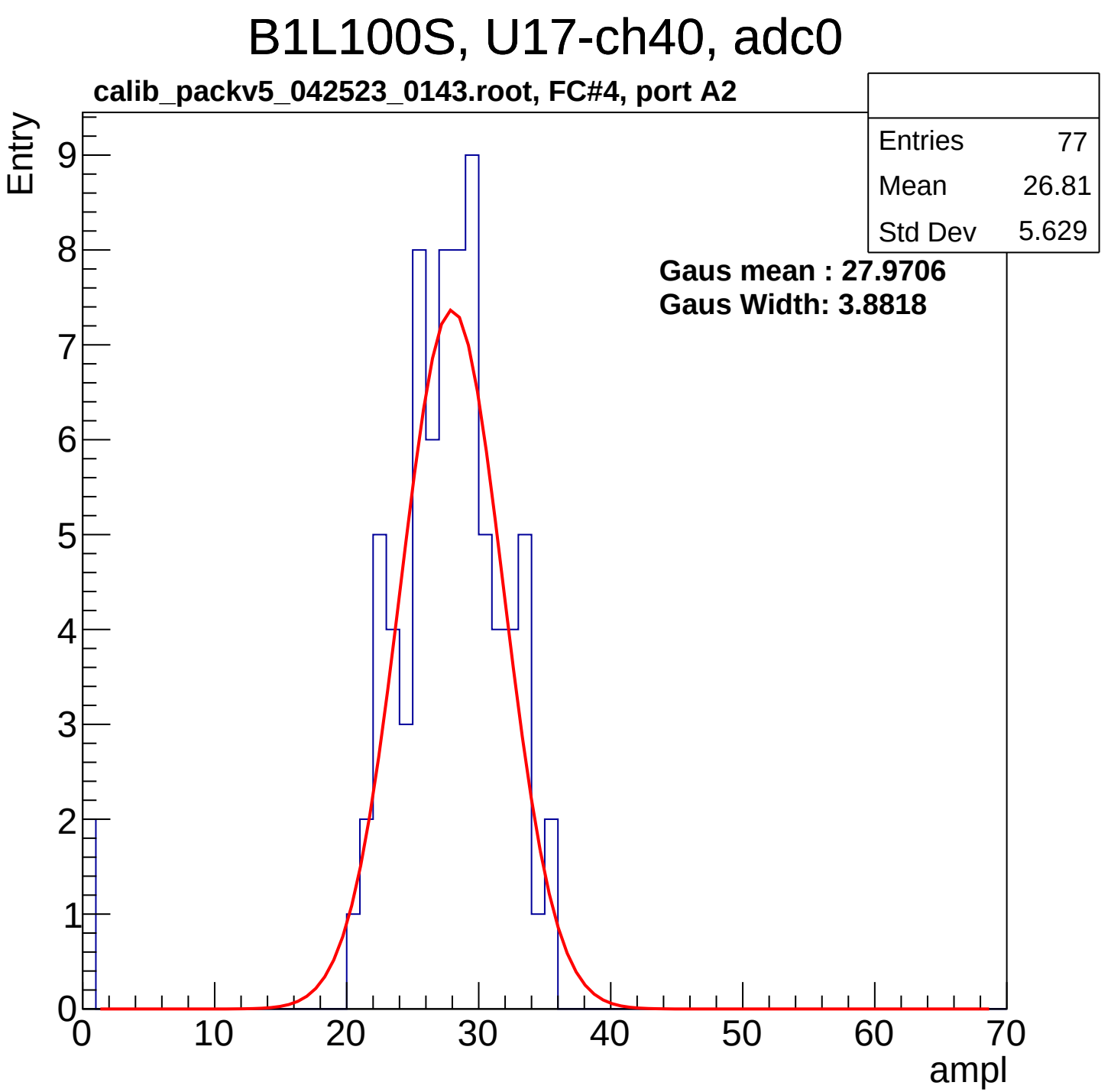
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch40, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 77
Mean 26.81
Std Dev 5.629
Gaus mean : 27.9706
Gaus Width: 3.8818
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
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40
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60
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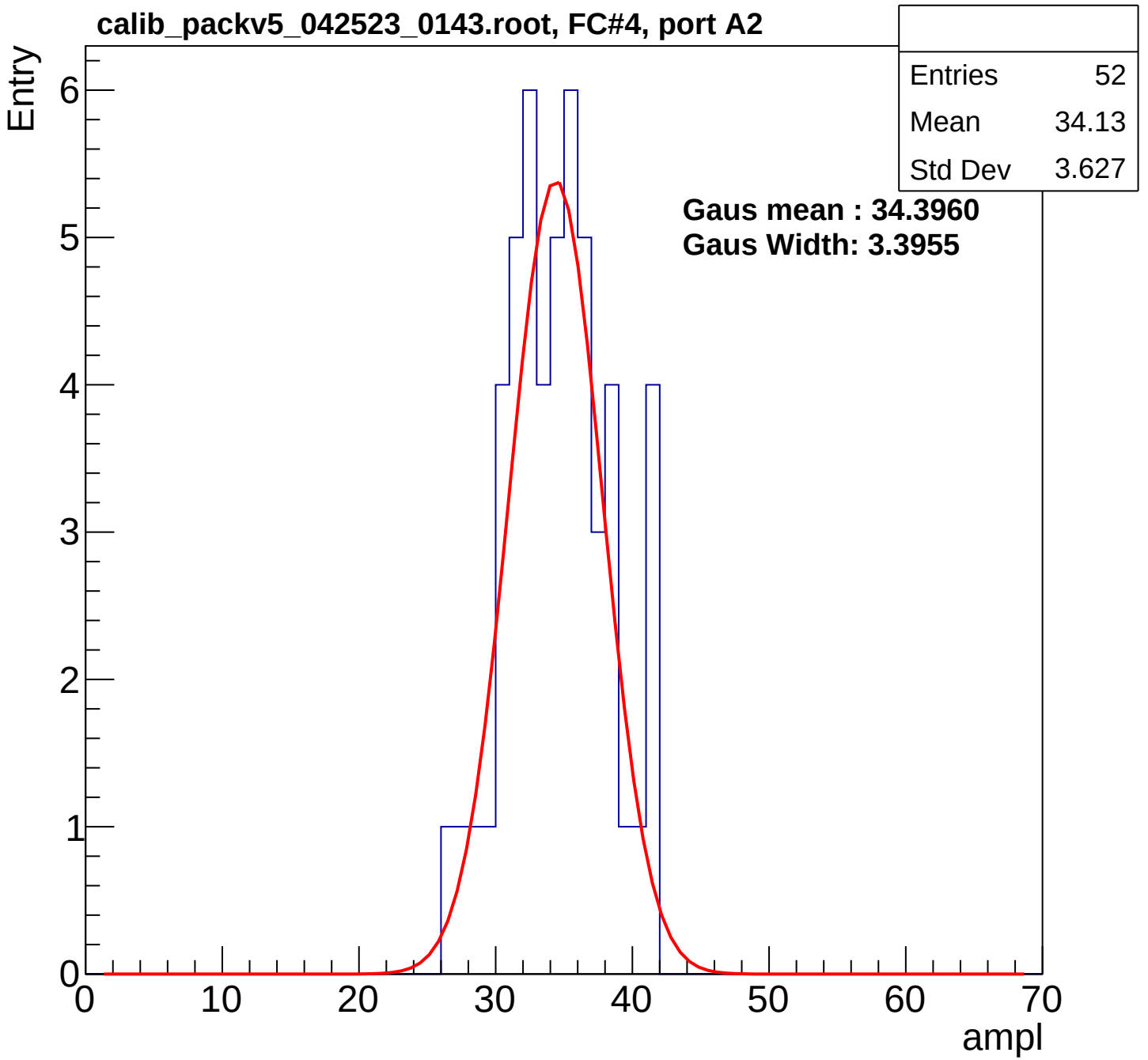
B1L100S, U17-ch40, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 52
Mean 34.13
Std Dev 3.627
Gaus mean : 34.3960
Gaus Width: 3.3955
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
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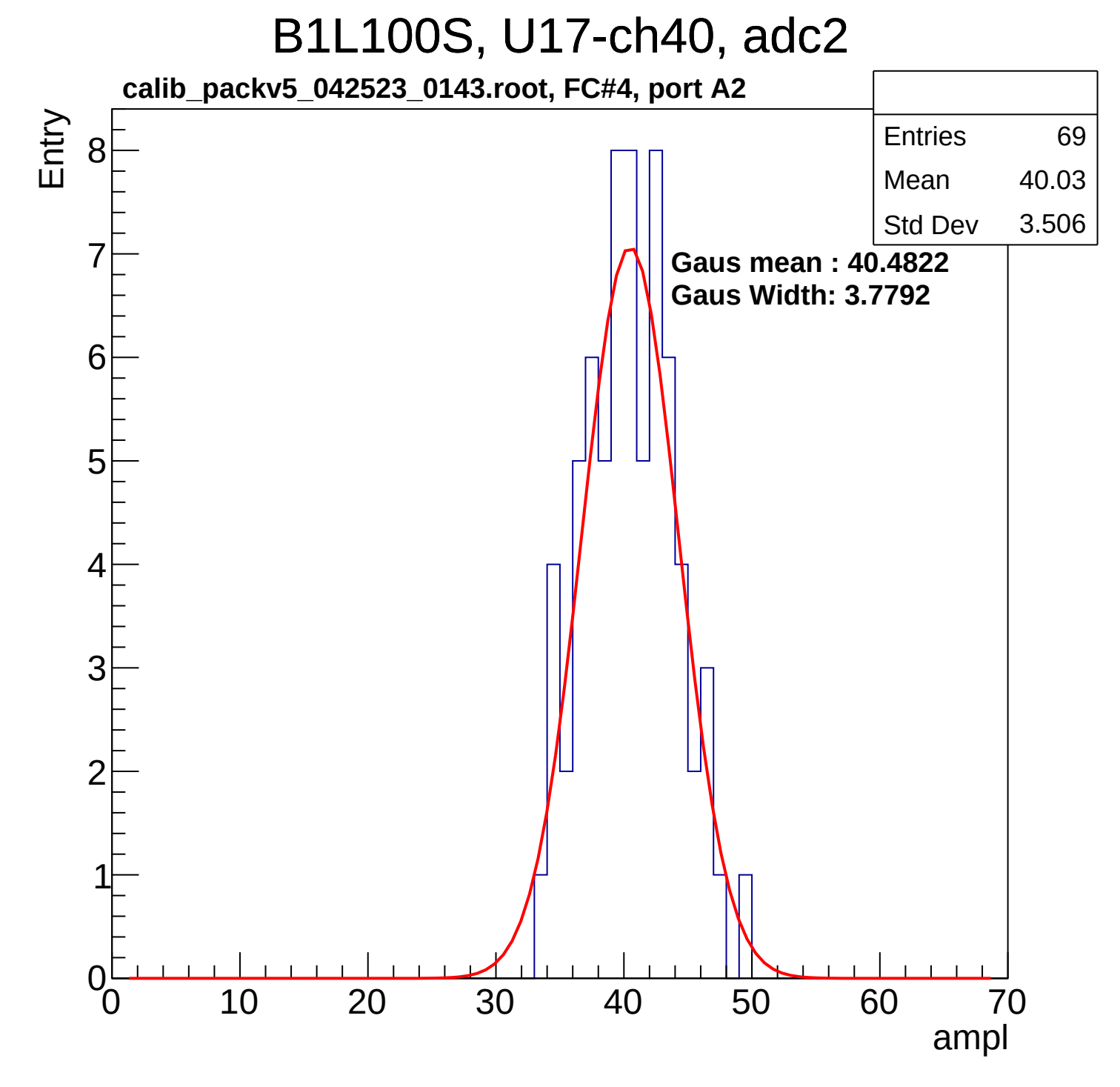
B1L100S, U17-ch40, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 40.03
Std Dev 3.506
Gaus mean : 40.4822
Gaus Width: 3.7792
Entry
ampl
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2
3
4
5
6
7
8
0
10
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40
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60
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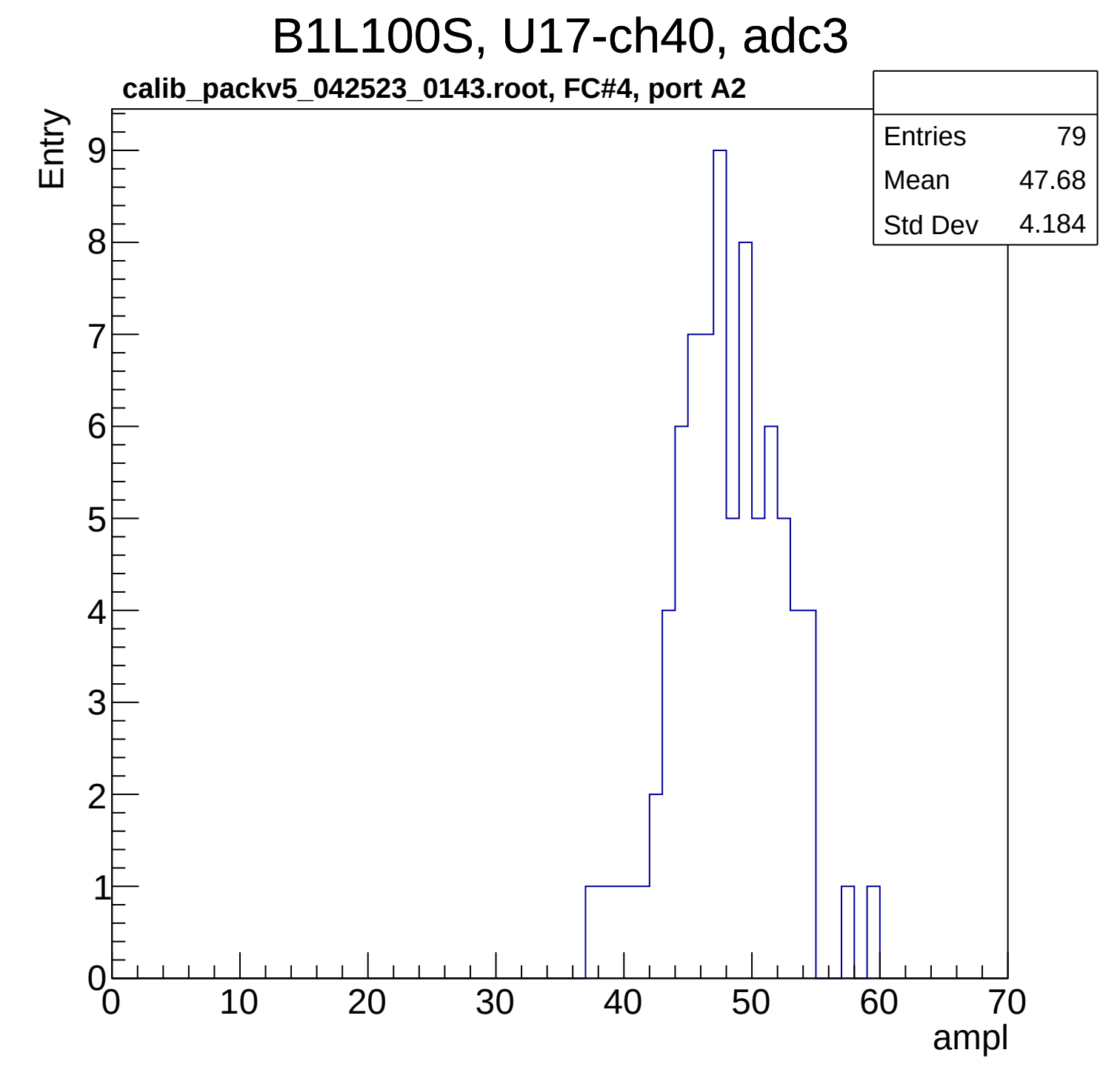
B1L100S, U17-ch40, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 79
Mean 47.68
Std Dev 4.184
Entry
ampl
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3
4
5
6
7
8
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0
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60
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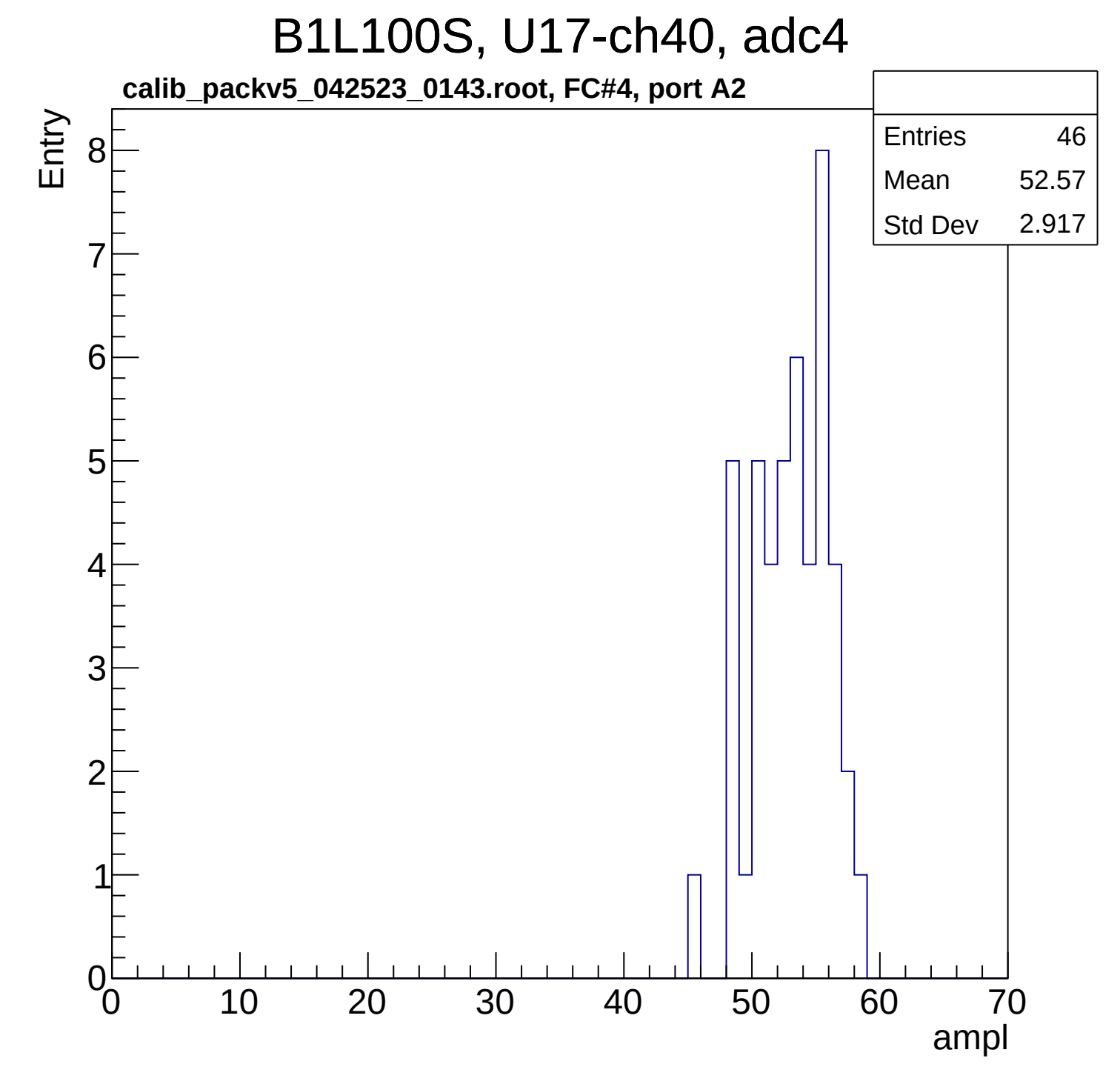
B1L100S, U17-ch40, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 46
Mean 52.57
Std Dev 2.917
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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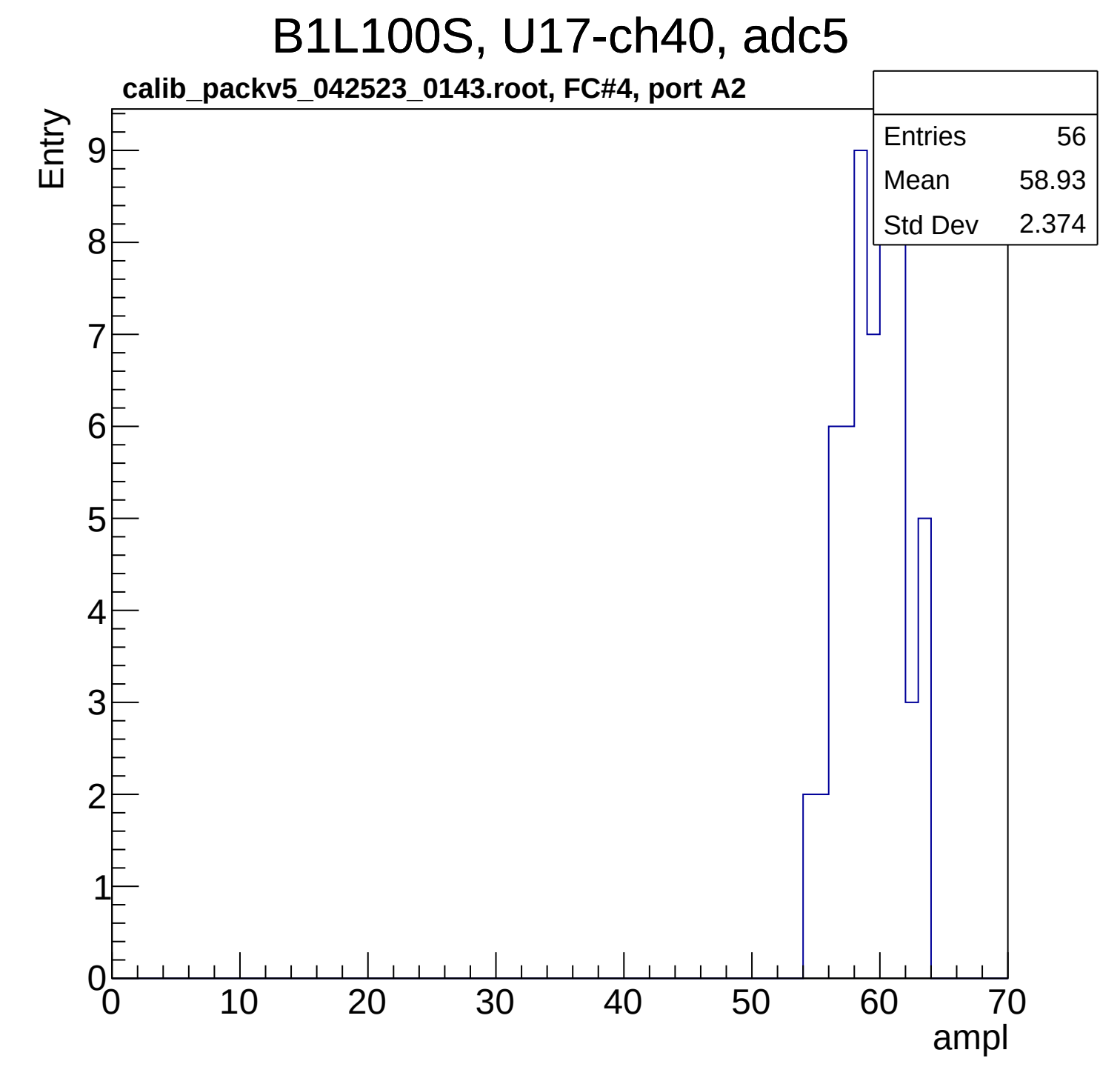
B1L100S, U17-ch40, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 58.93
Std Dev 2.374
Entry
ampl
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3
4
5
6
7
8
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0
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60
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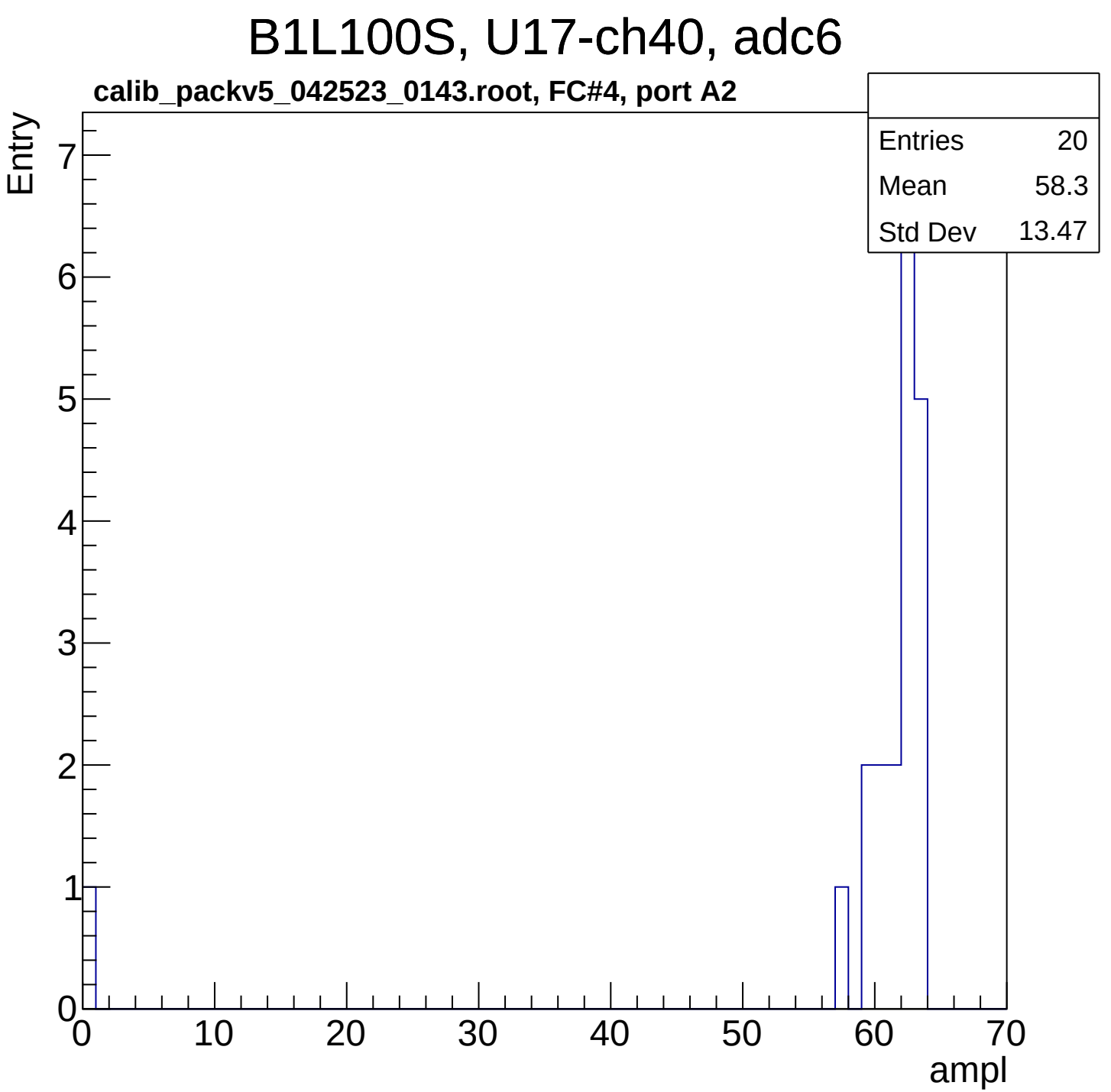
B1L100S, U17-ch40, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 20
Mean 58.3
Std Dev 13.47
Entry
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1
2
3
4
5
6
7
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10
20
30
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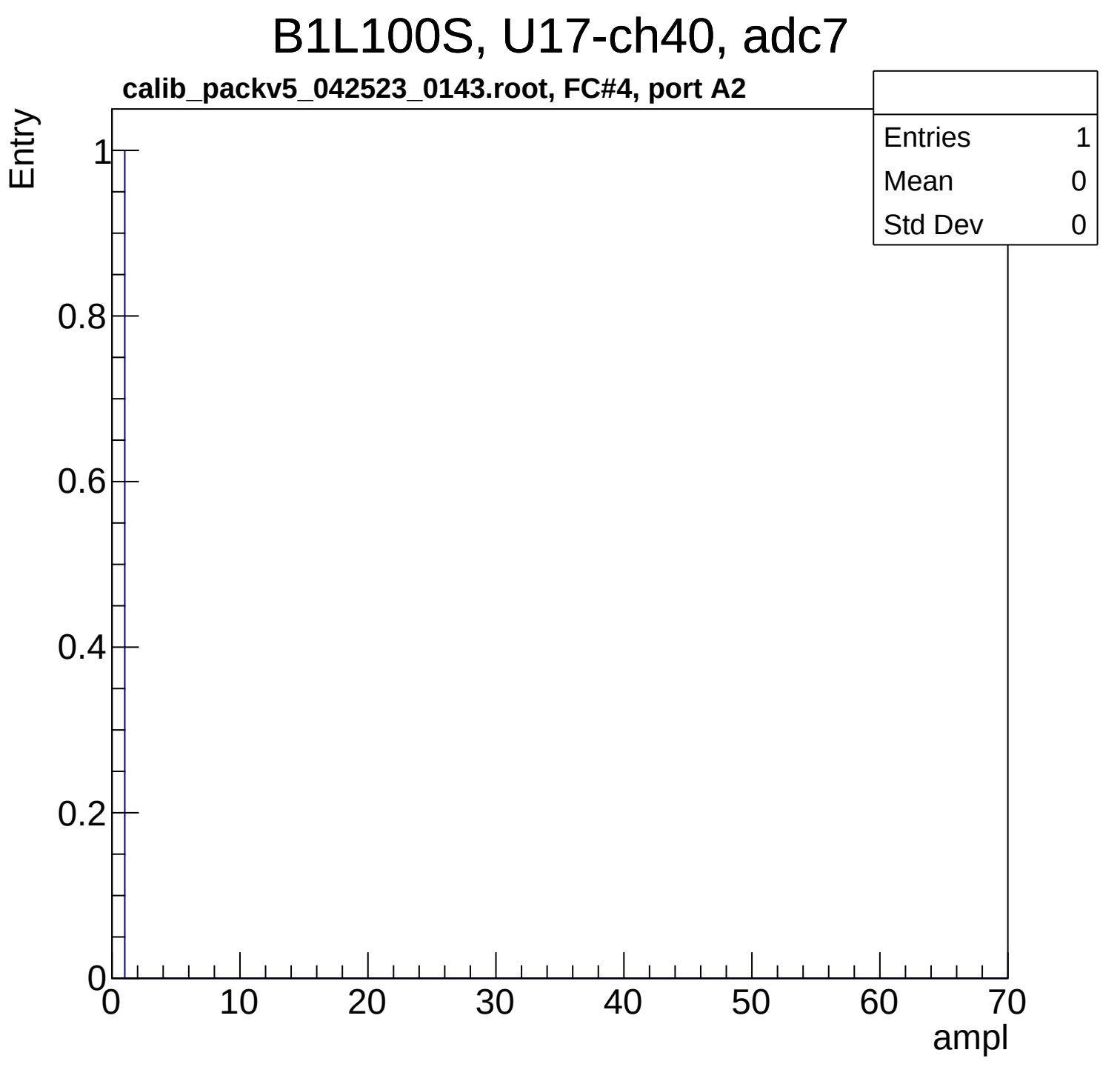
50
60
70
ampl


B1L100S, U17-ch40, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
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0.6
0.4
0.2
0
0
10
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30
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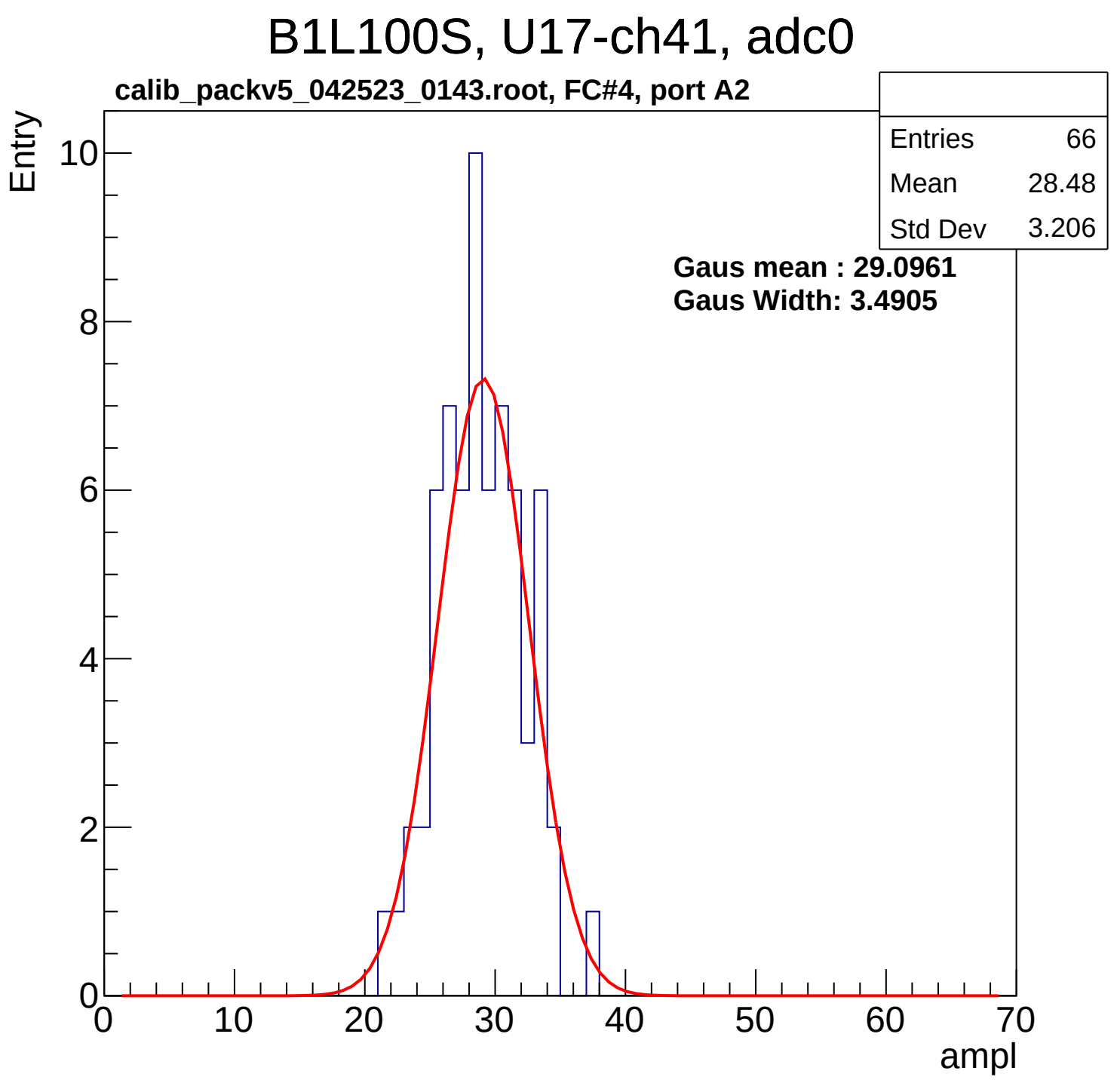
50
60
70
ampl


B1L100S, U17-ch41, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 28.48
Std Dev 3.206
Gaus mean : 29.0961
Gaus Width: 3.4905
Entry
ampl
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8
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0
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60
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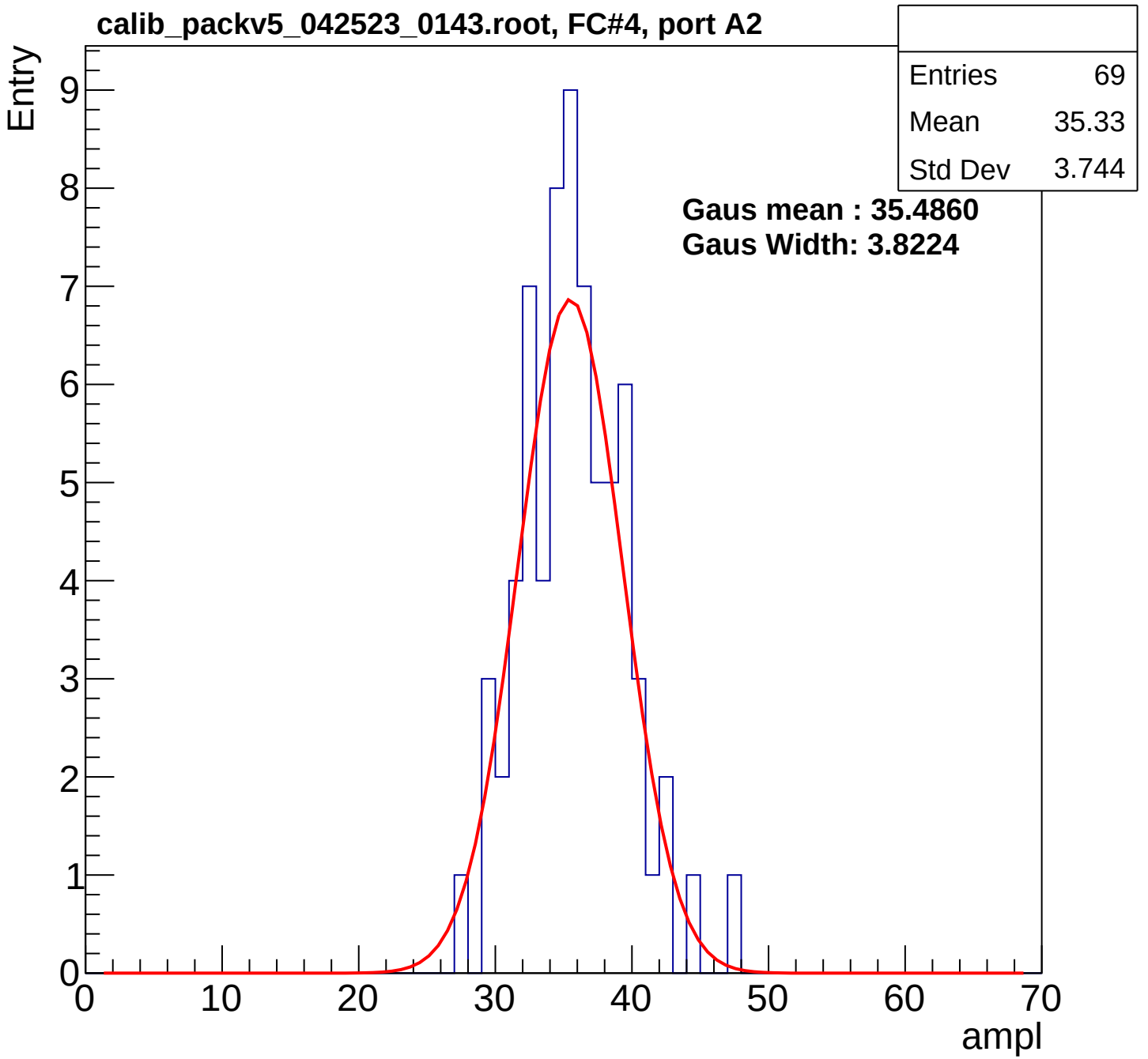
B1L100S, U17-ch41, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 35.33
Std Dev 3.744
Gaus mean : 35.4860
Gaus Width: 3.8224
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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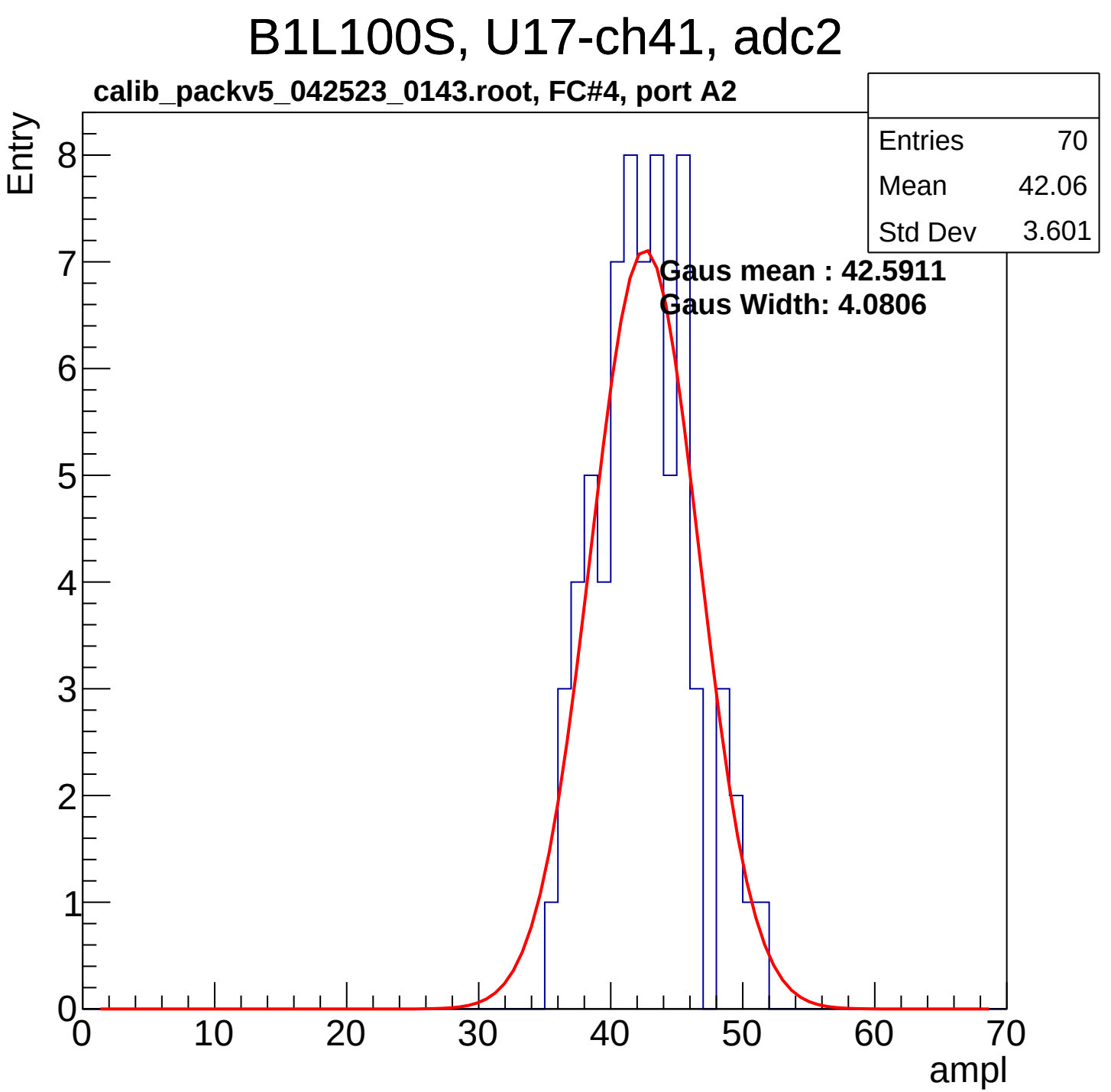
B1L100S, U17-ch41, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 42.06
Std Dev 3.601
Gaus mean : 42.5911
Gaus Width: 4.0806
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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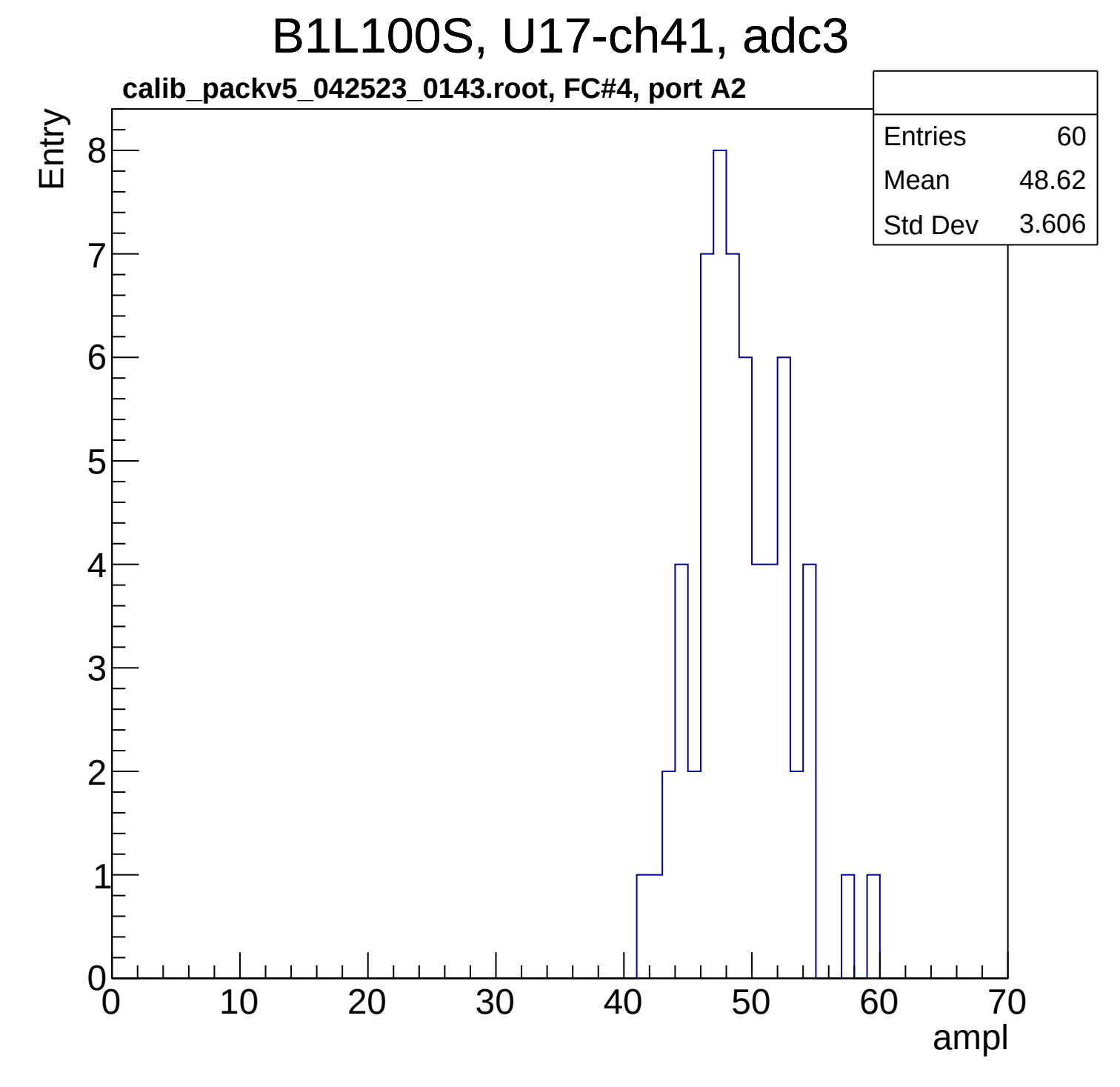
B1L100S, U17-ch41, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 48.62
Std Dev 3.606
Entry
ampl
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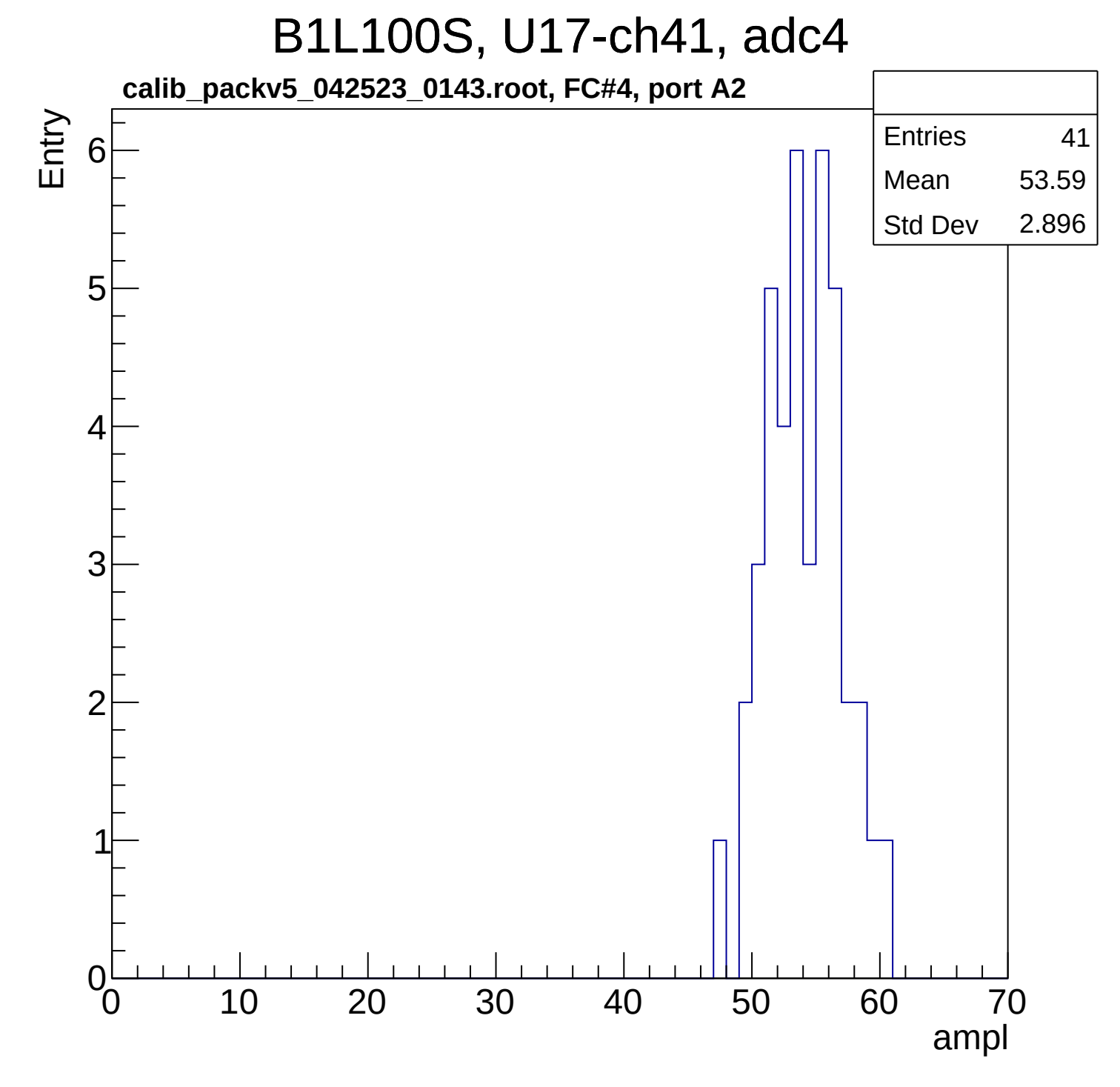
B1L100S, U17-ch41, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 41
Mean 53.59
Std Dev 2.896
Entry
ampl
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3
4
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0
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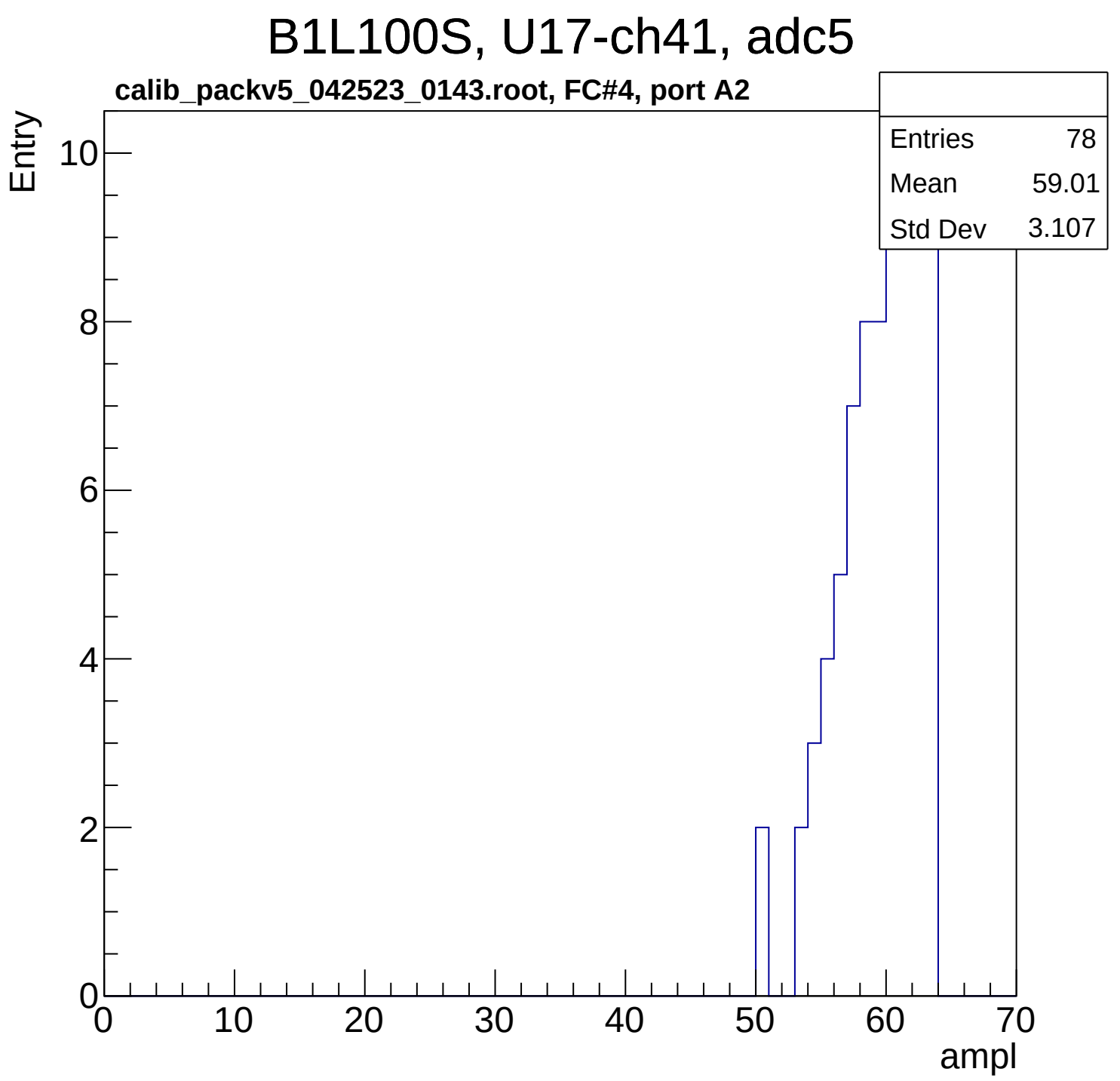
B1L100S, U17-ch41, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 78
Mean 59.01
Std Dev 3.107
Entry
ampl
0
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4
6
8
10
0
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20
30
40
50
60
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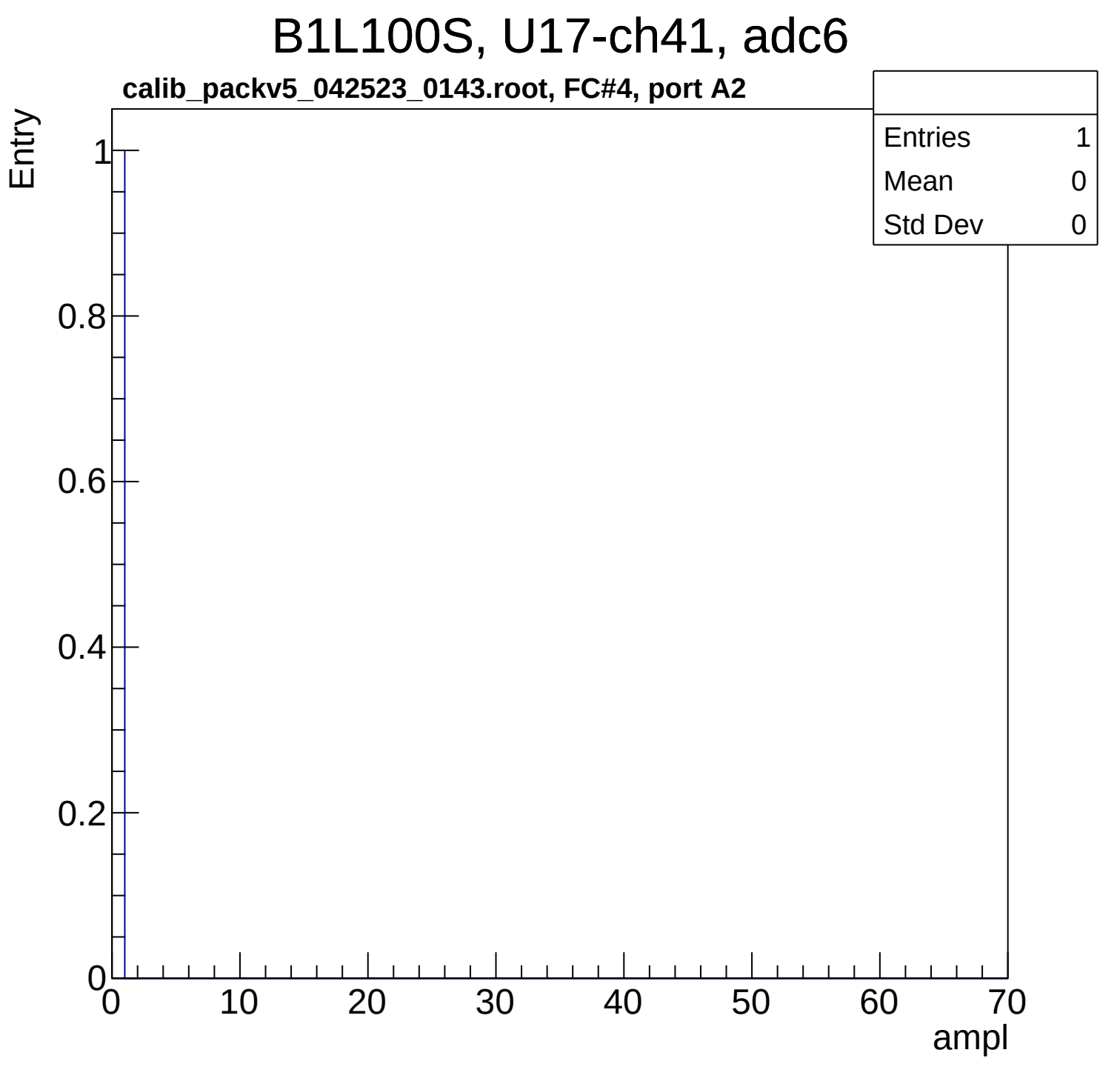
B1L100S, U17-ch41, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
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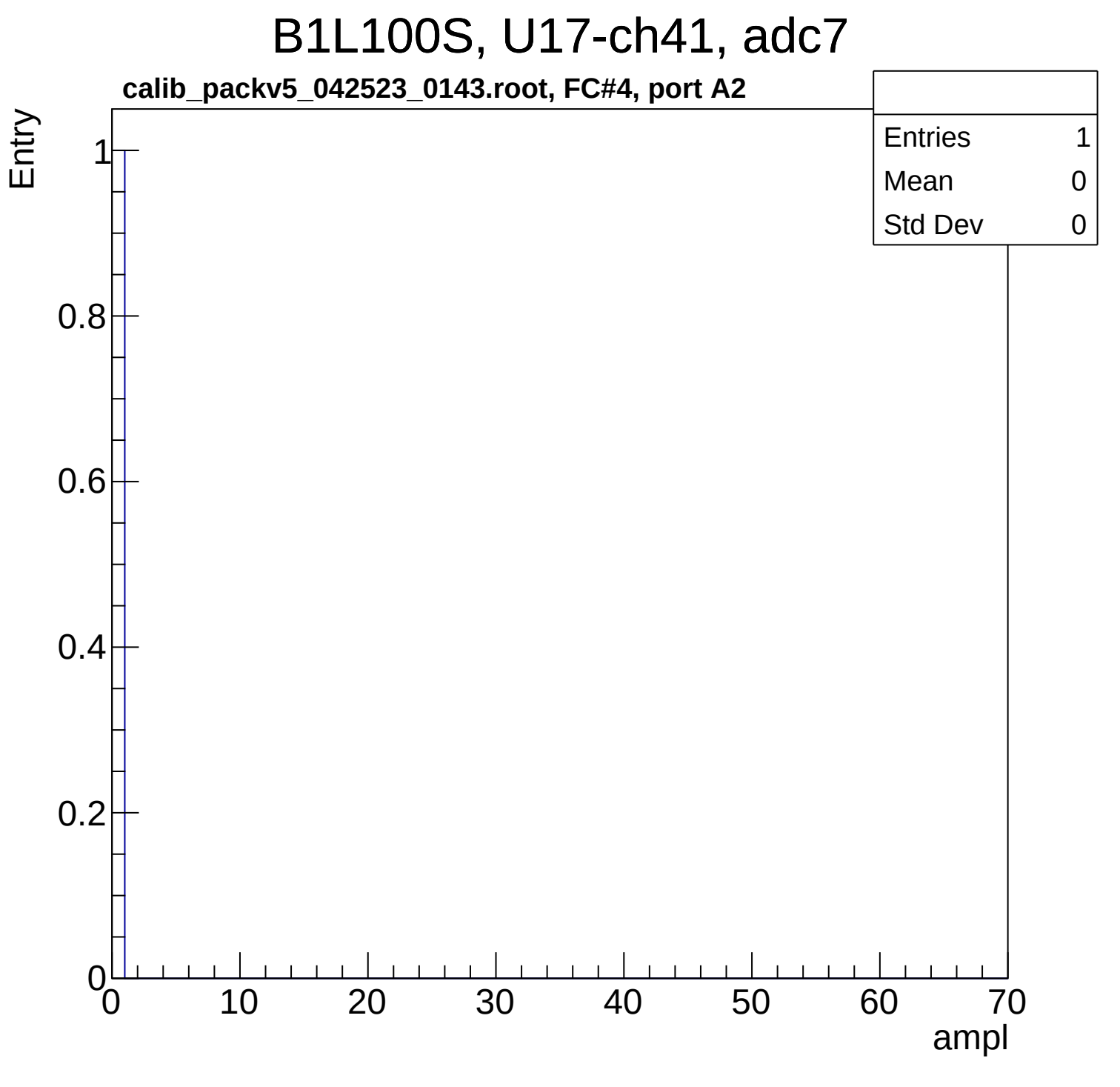
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch41, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
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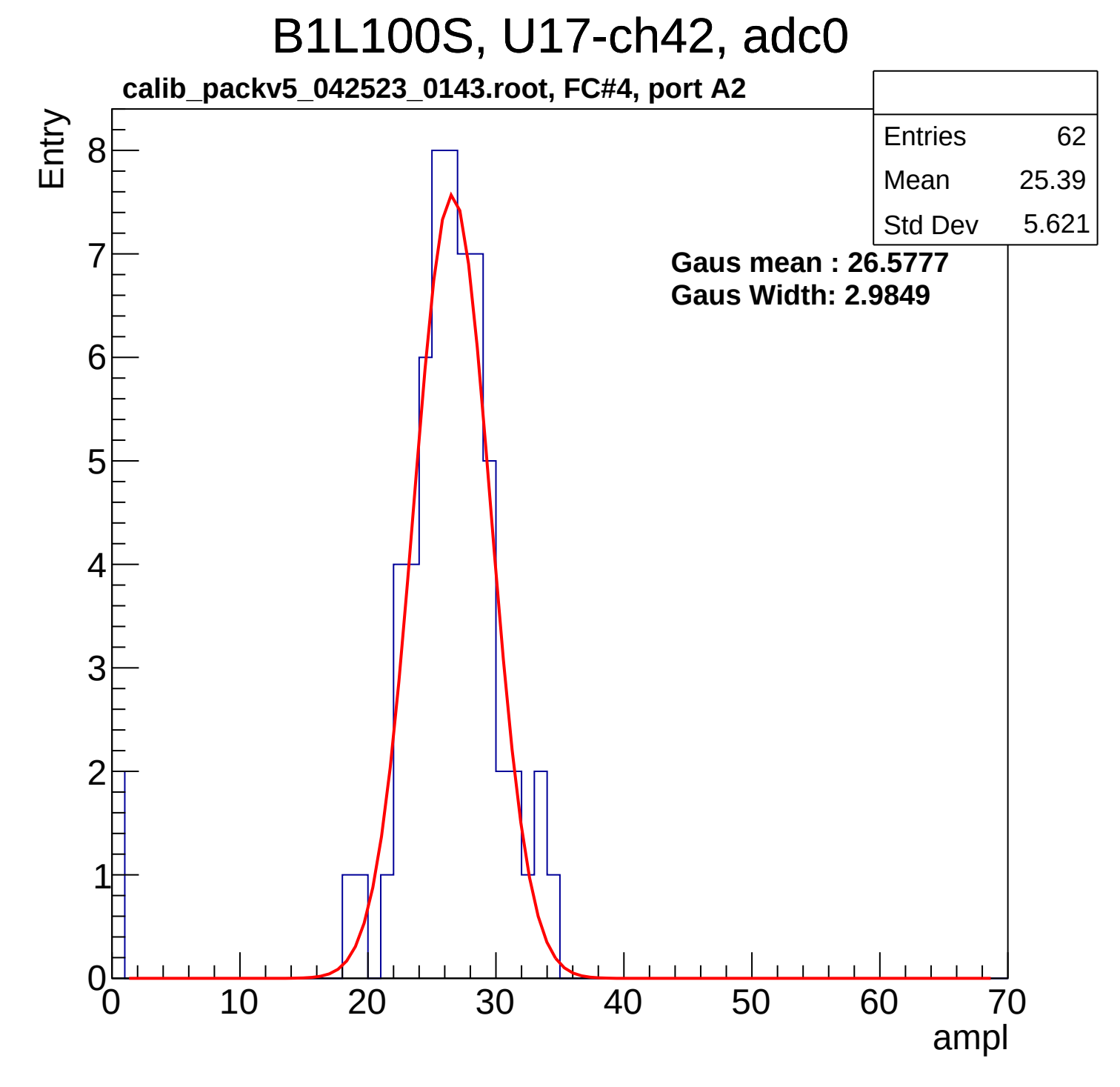
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch42, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 25.39
Std Dev 5.621
Gaus mean : 26.5777
Gaus Width: 2.9849
Entry
ampl
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1
2
3
4
5
6
7
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0
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20
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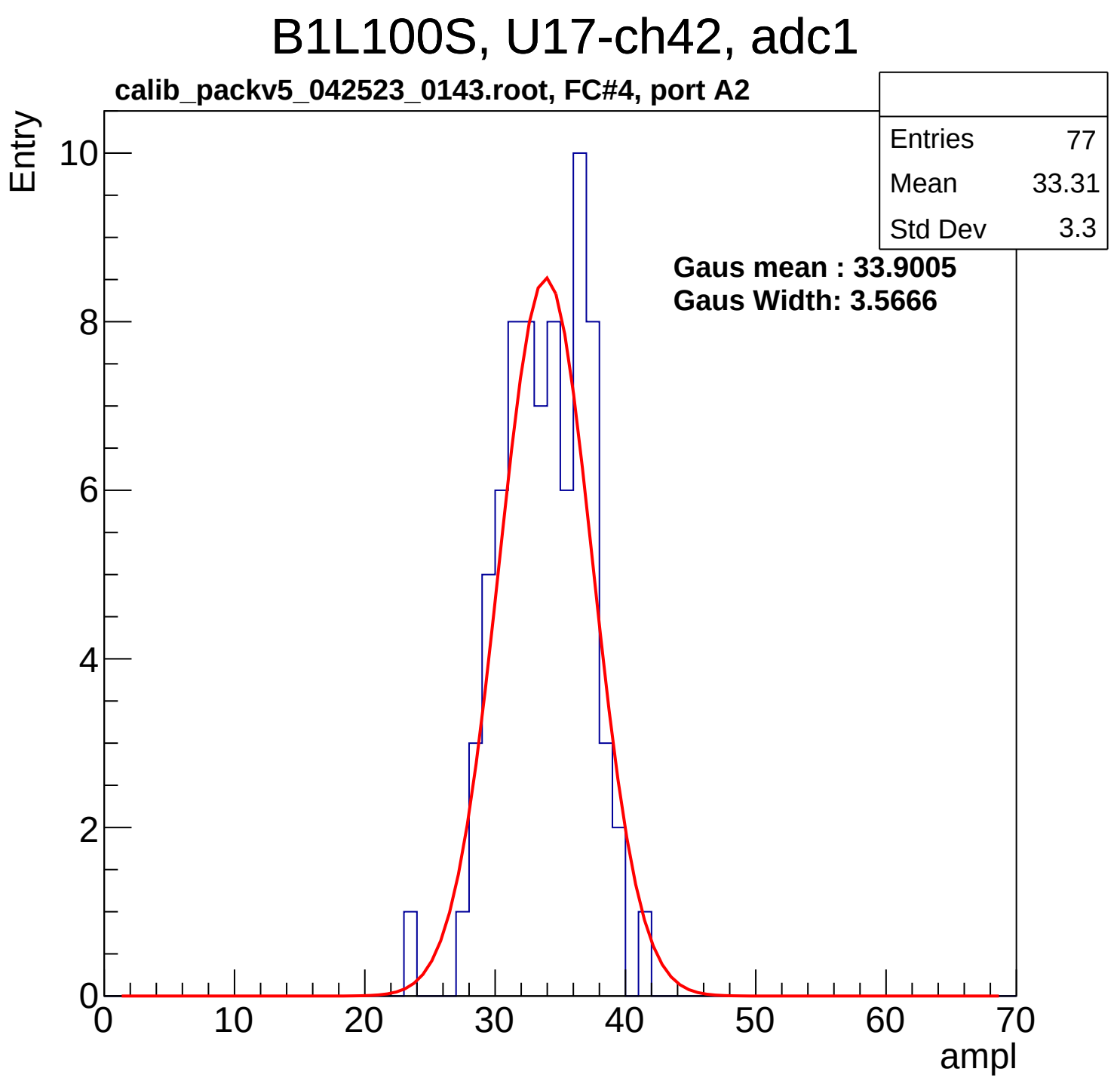
B1L100S, U17-ch42, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 77
Mean 33.31
Std Dev 3.3
Gaus mean : 33.9005
Gaus Width: 3.5666
Entry
ampl
0
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4
6
8
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0
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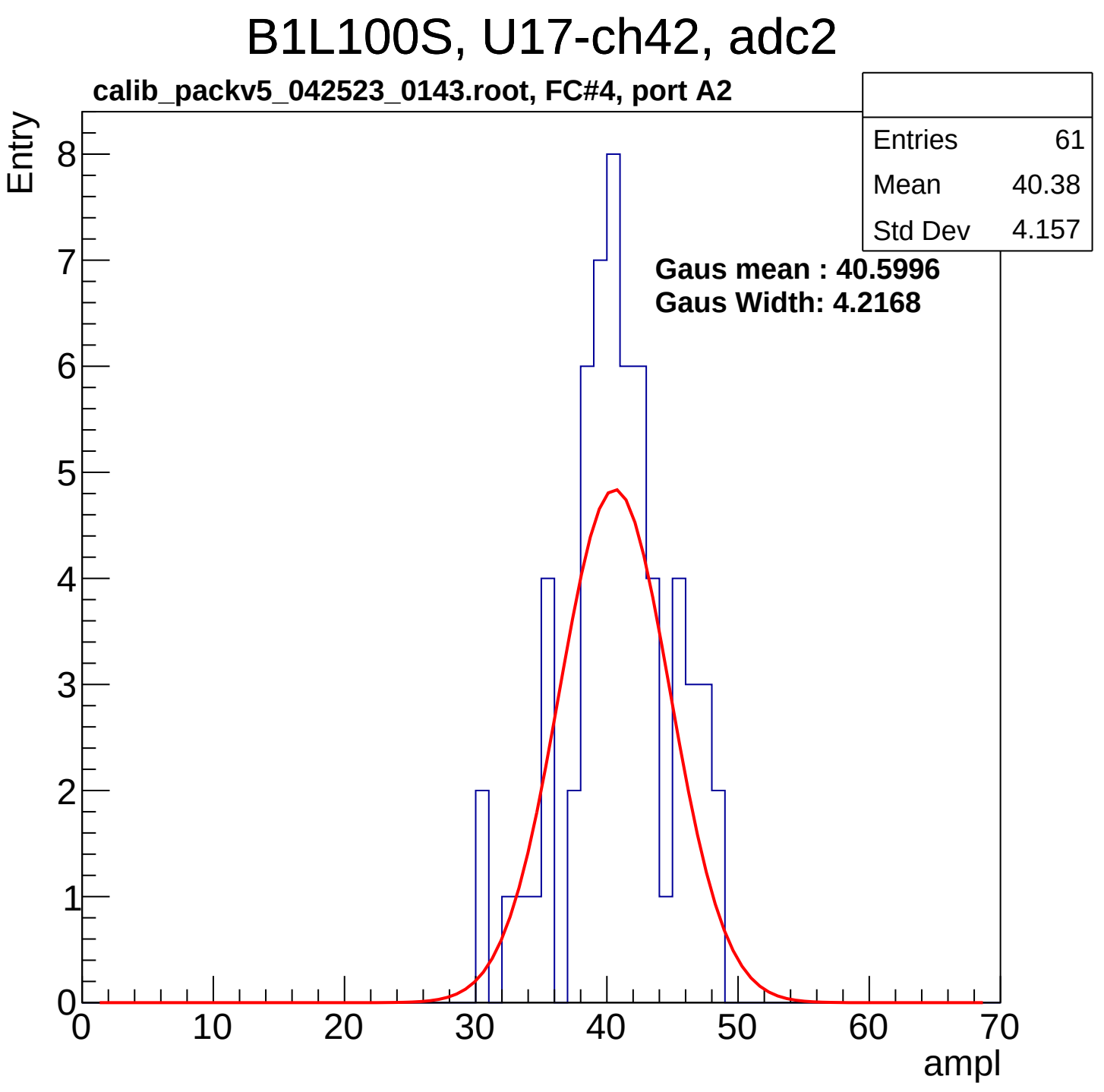
B1L100S, U17-ch42, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 40.38
Std Dev 4.157
Gaus mean : 40.5996
Gaus Width: 4.2168
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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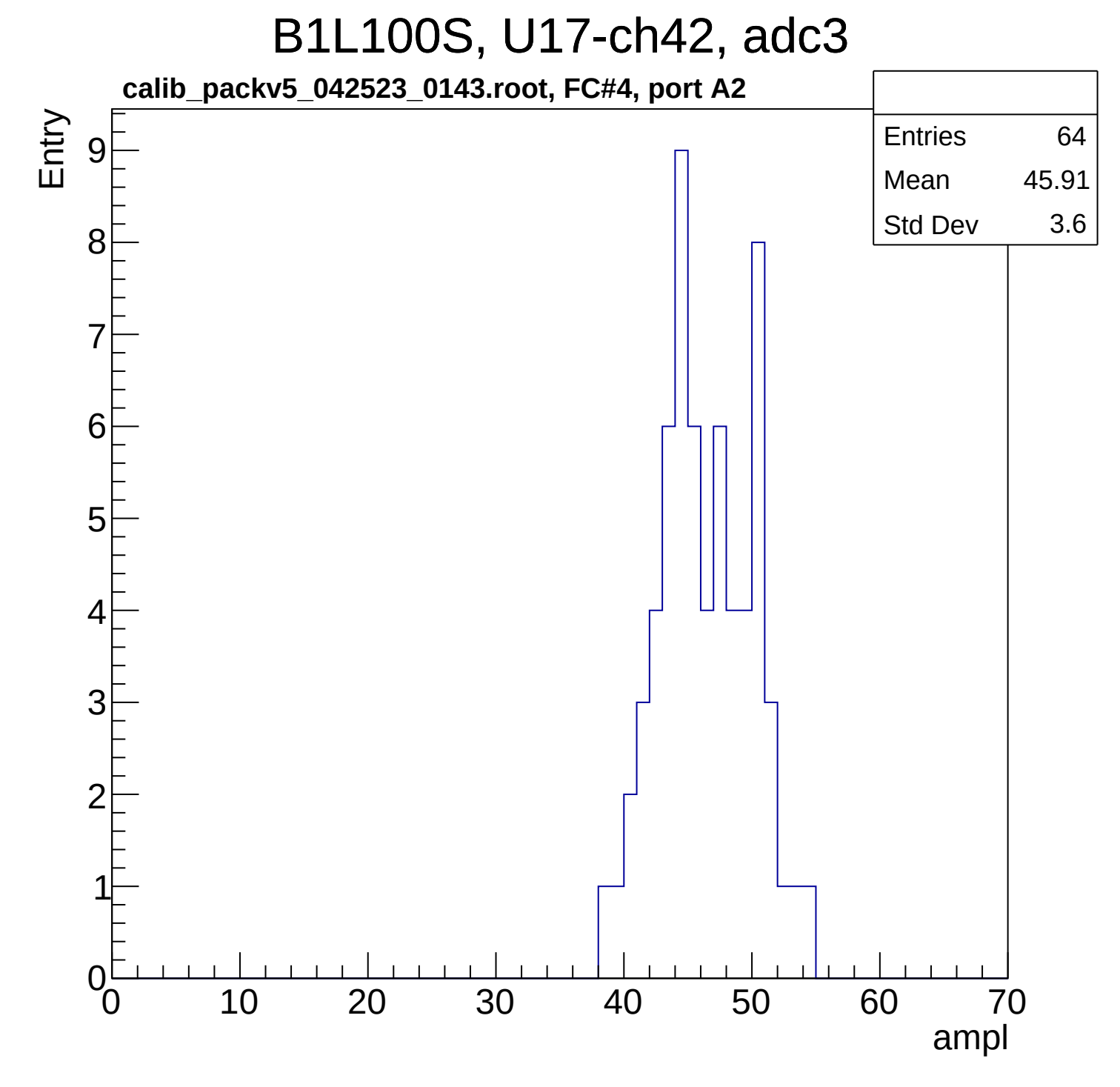
B1L100S, U17-ch42, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 45.91
Std Dev 3.6
Entry
ampl
0
1
2
3
4
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6
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0
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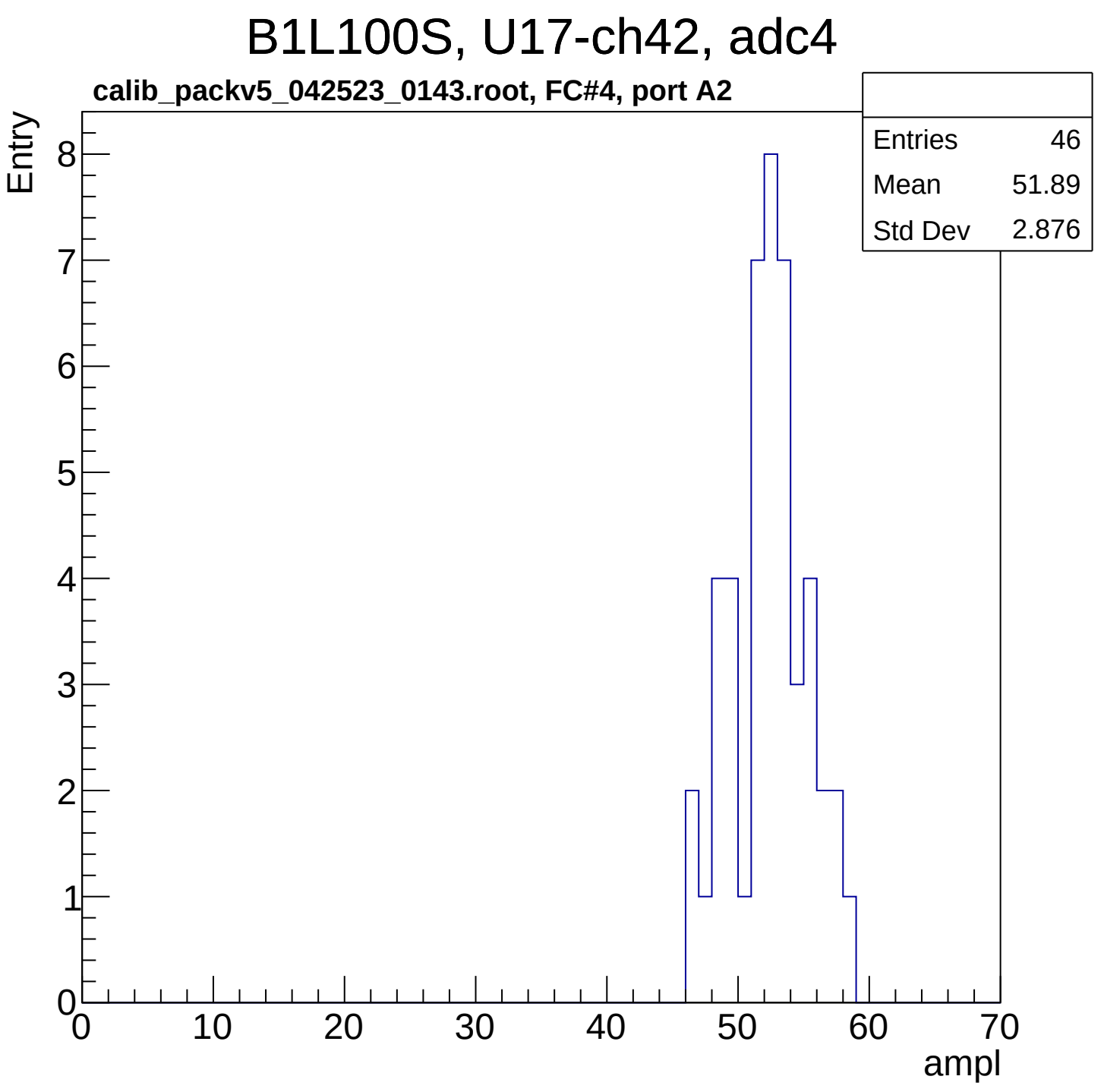
B1L100S, U17-ch42, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 46
Mean 51.89
Std Dev 2.876
Entry
ampl
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2
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4
5
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7
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0
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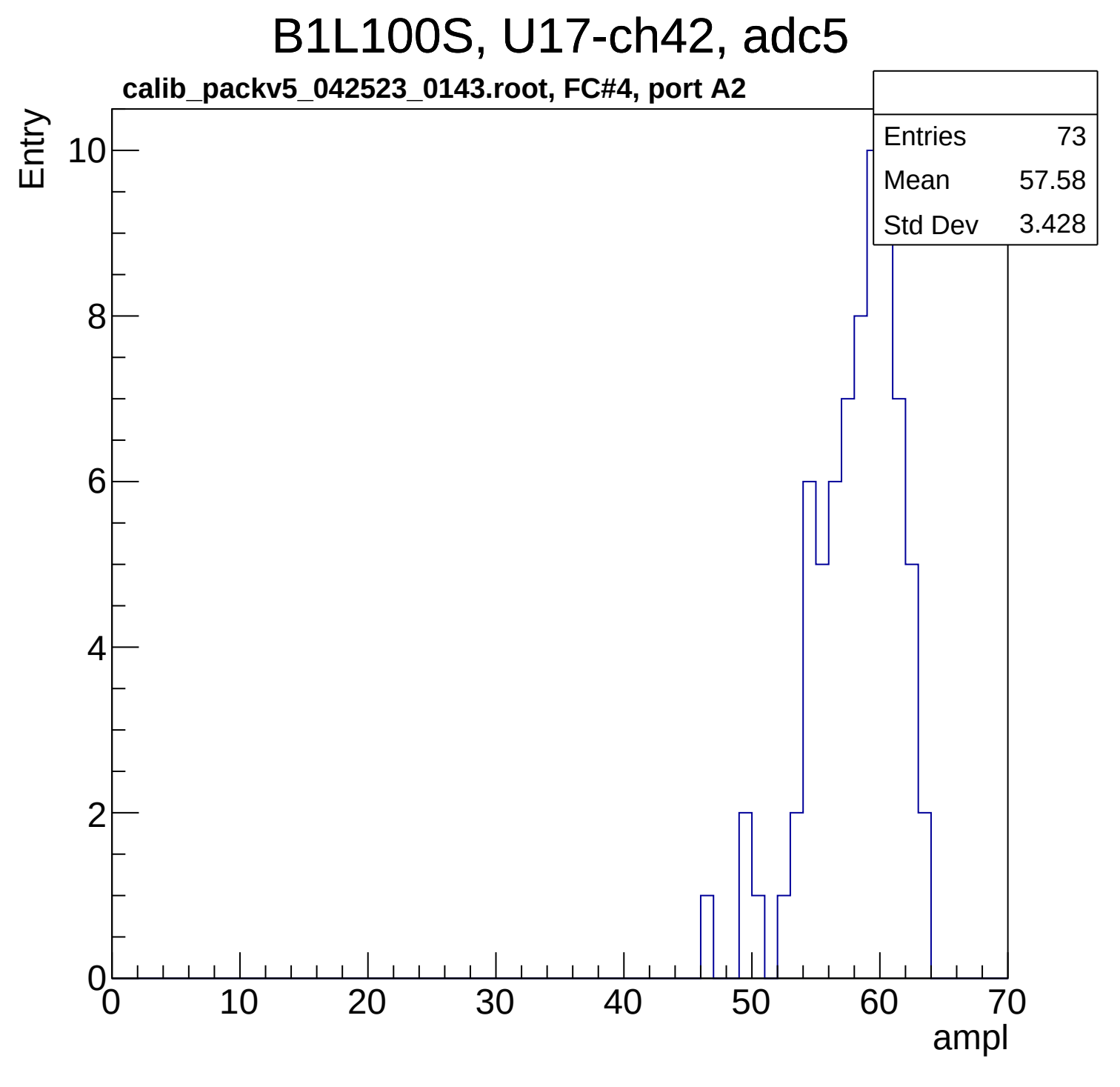
B1L100S, U17-ch42, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 57.58
Std Dev 3.428
Entry
ampl
0
2
4
6
8
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0
10
20
30
40
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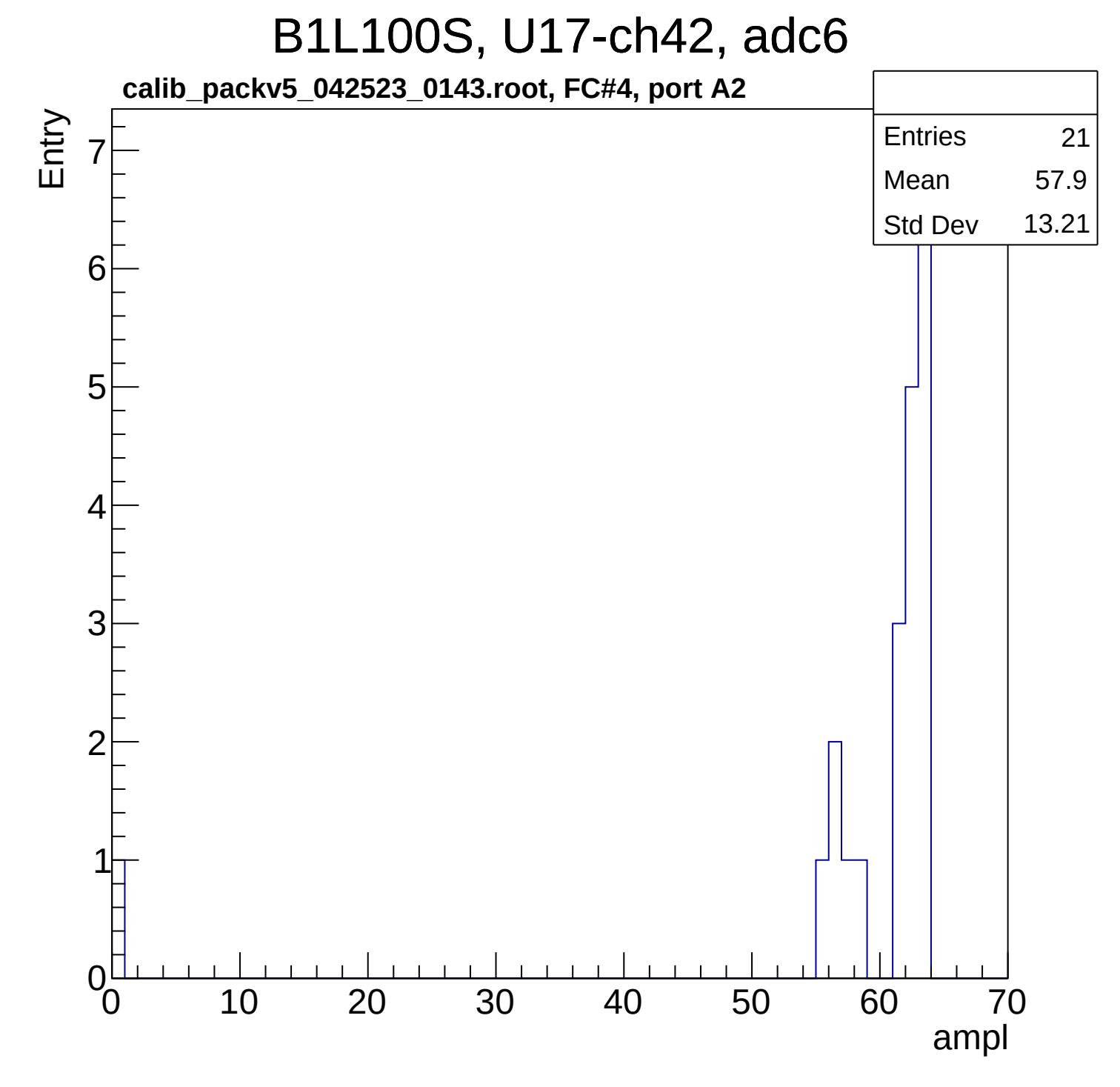
B1L100S, U17-ch42, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 21
Mean 57.9
Std Dev 13.21
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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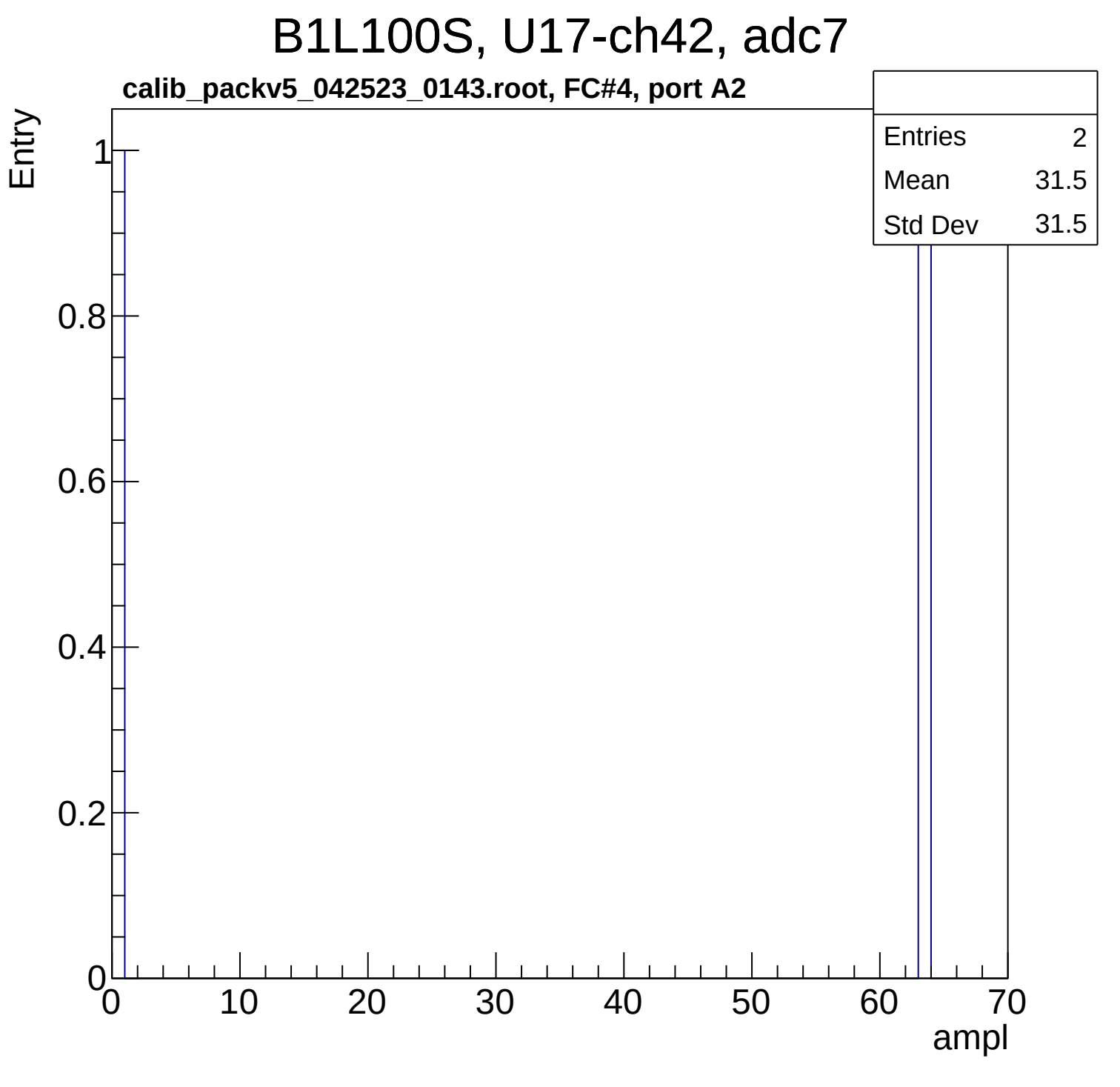
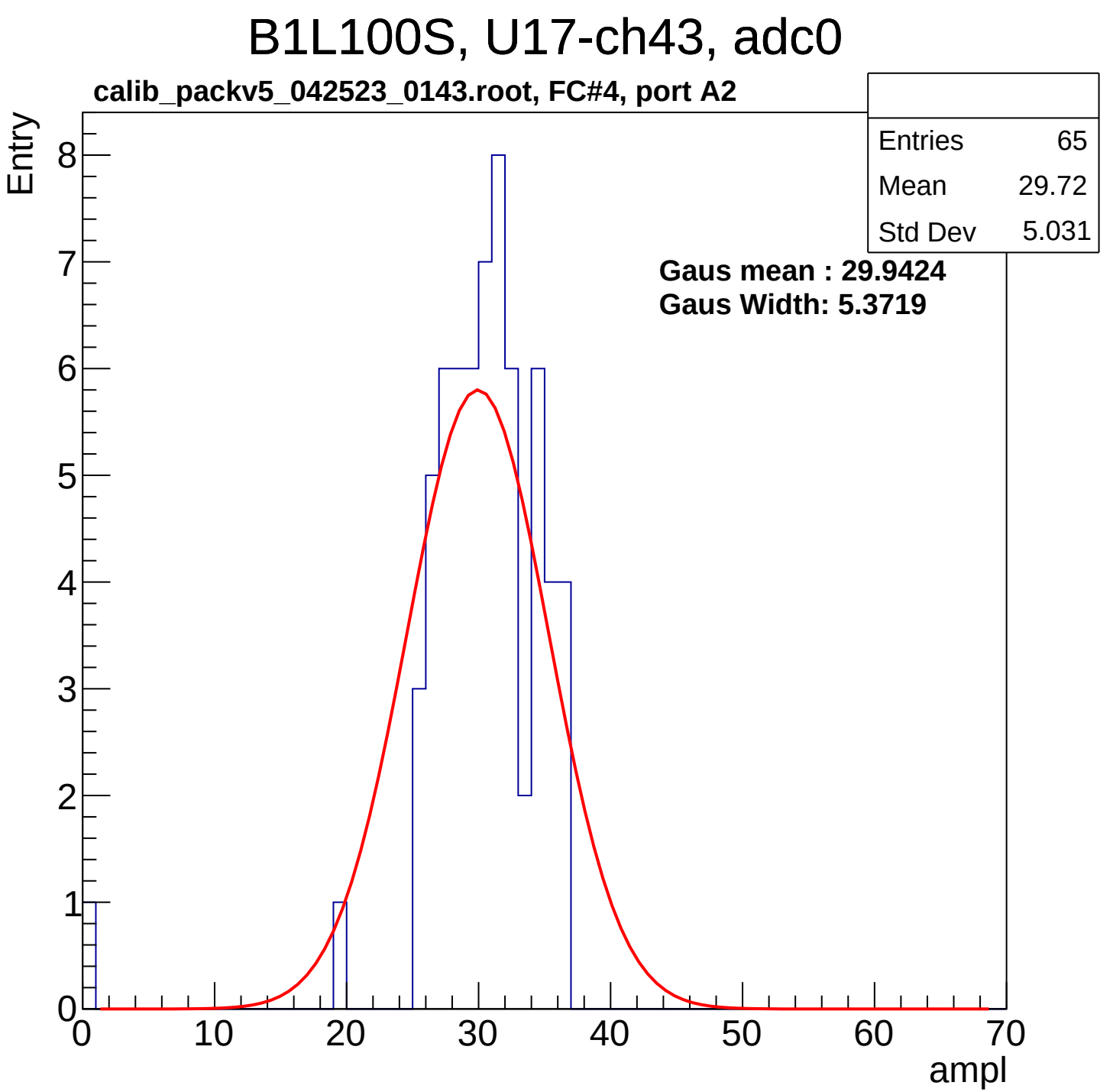
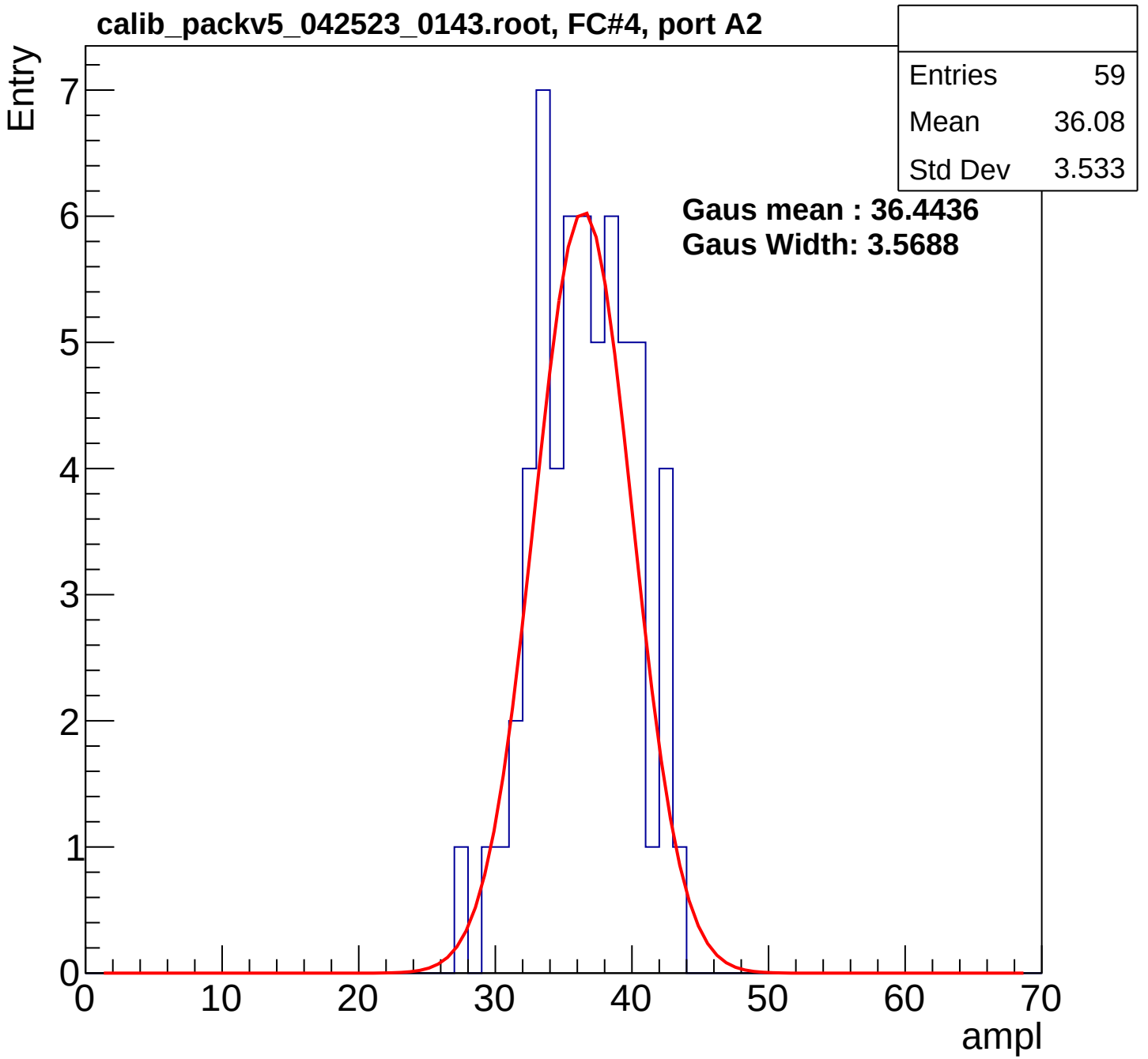
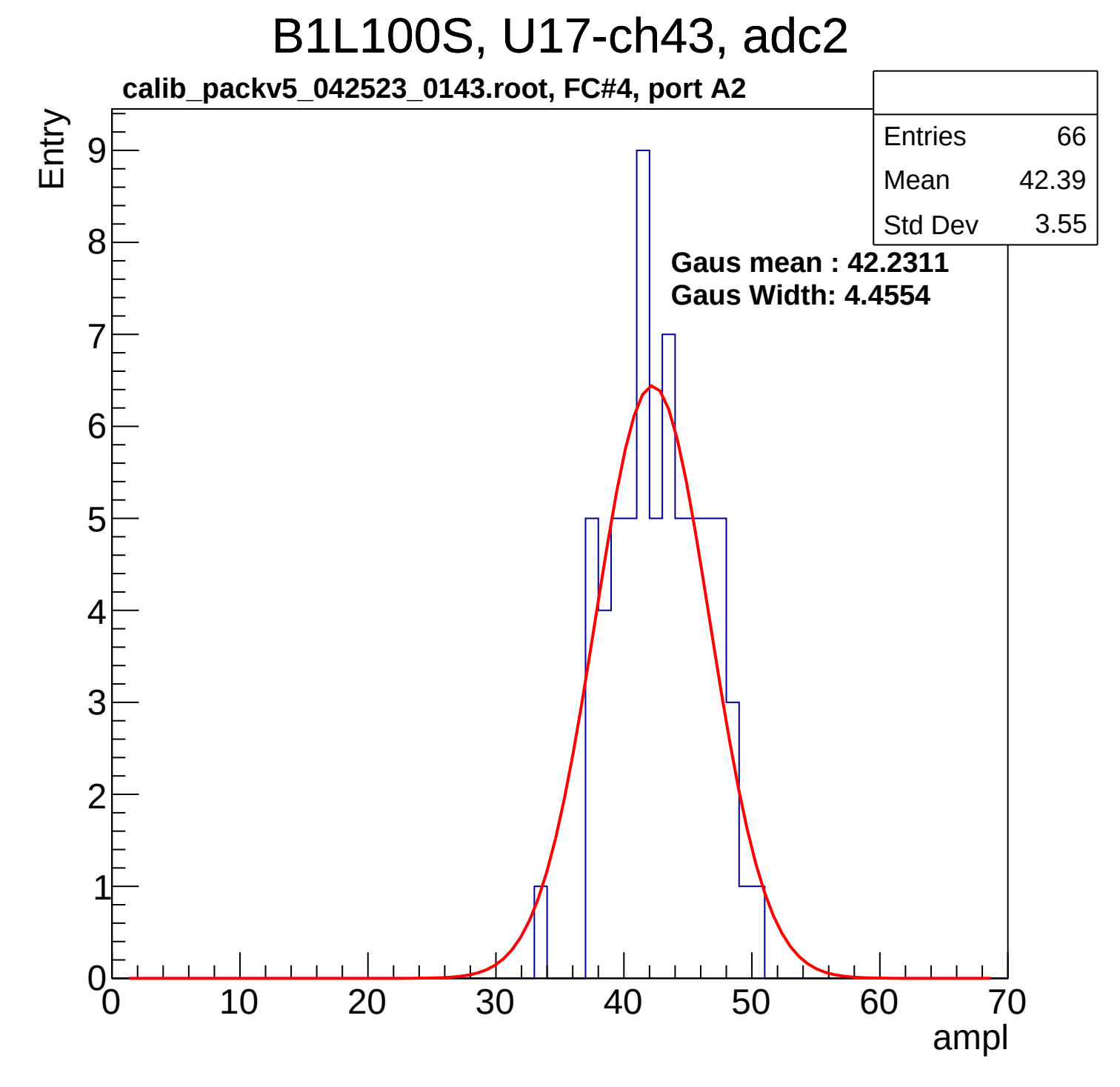

B1L100S, U17-ch42, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 31.5
Std Dev 31.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch43, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 29.72
Std Dev 5.031
Gaus mean : 29.9424
Gaus Width: 5.3719
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch43, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 36.08
Std Dev 3.533
Gaus mean : 36.4436
Gaus Width: 3.5688
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U17-ch43, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 42.39
Std Dev 3.55
Gaus mean : 42.2311
Gaus Width: 4.4554
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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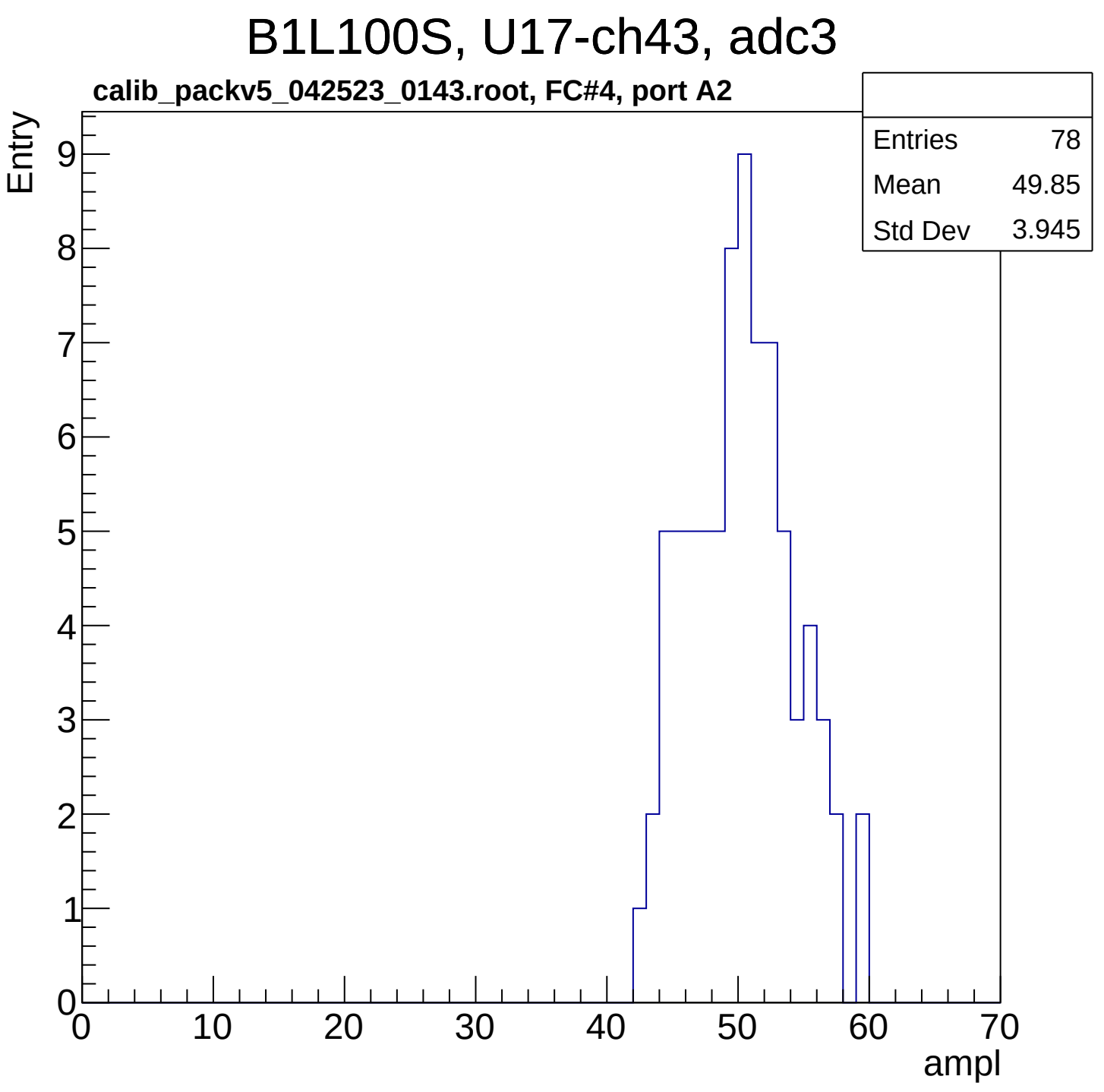
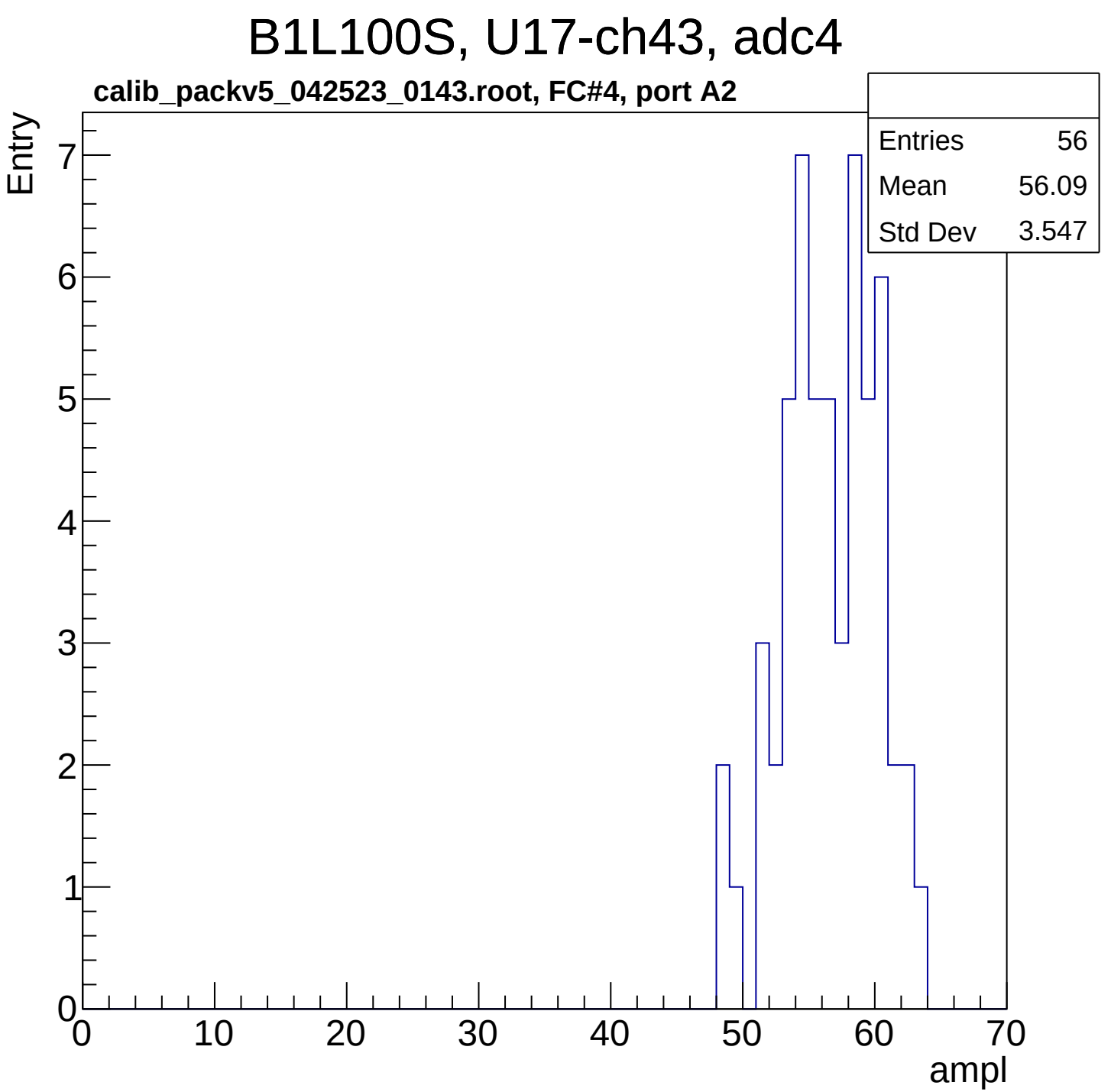

B1L100S, U17-ch43, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 78
Mean 49.85
Std Dev 3.945
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch43, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 56.09
Std Dev 3.547
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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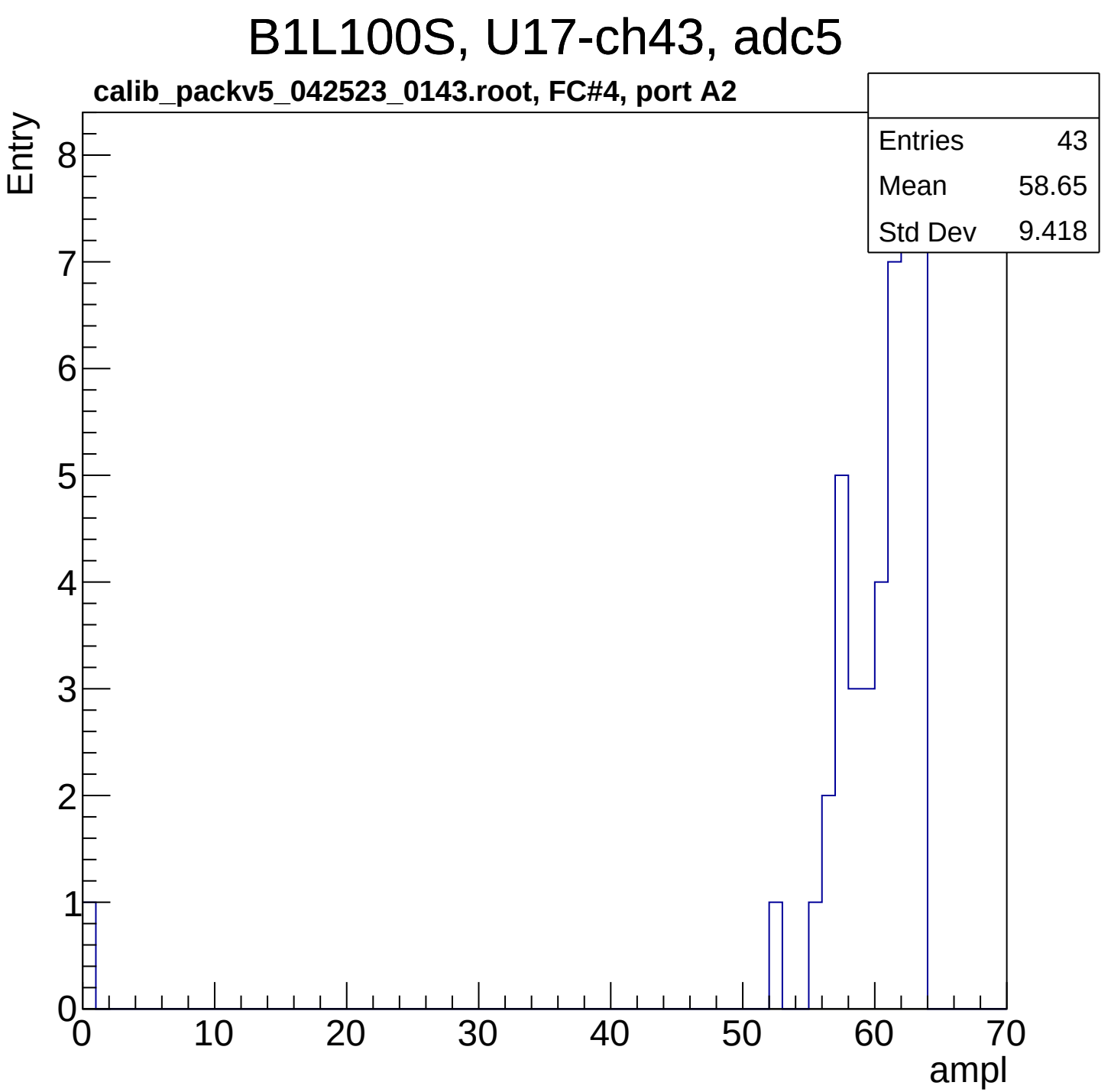
B1L100S, U17-ch43, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 43
Mean 58.65
Std Dev 9.418
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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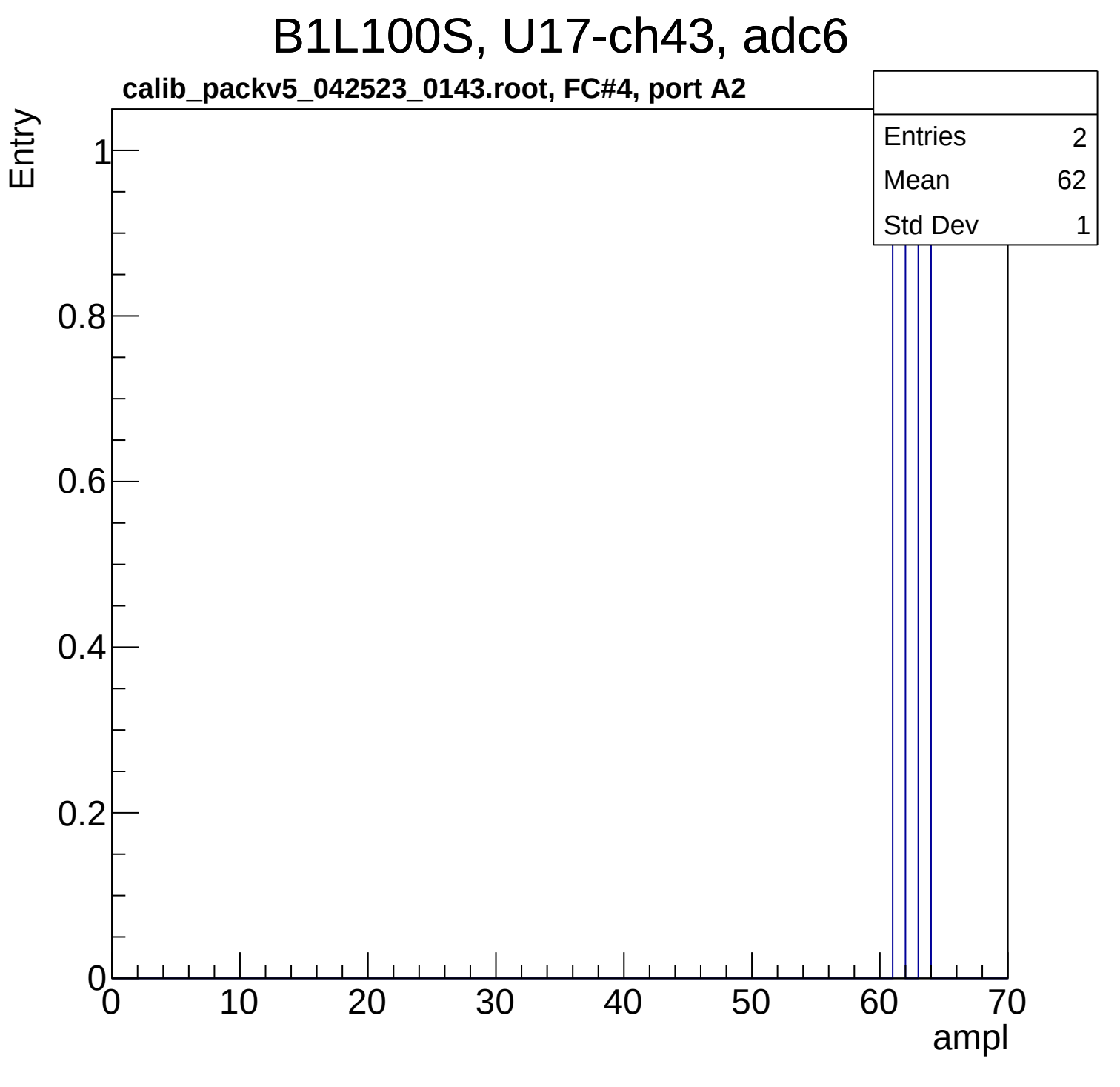
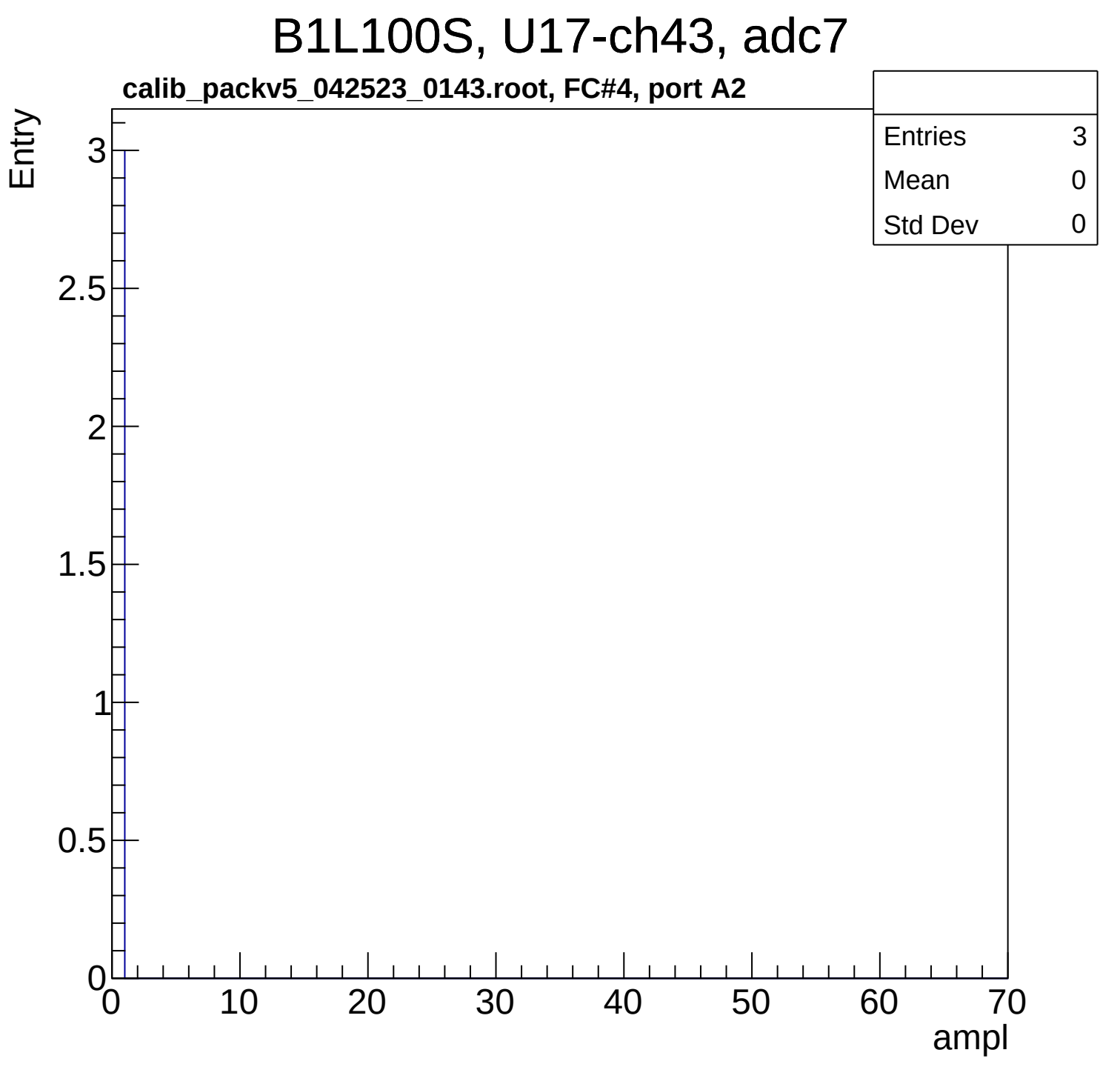
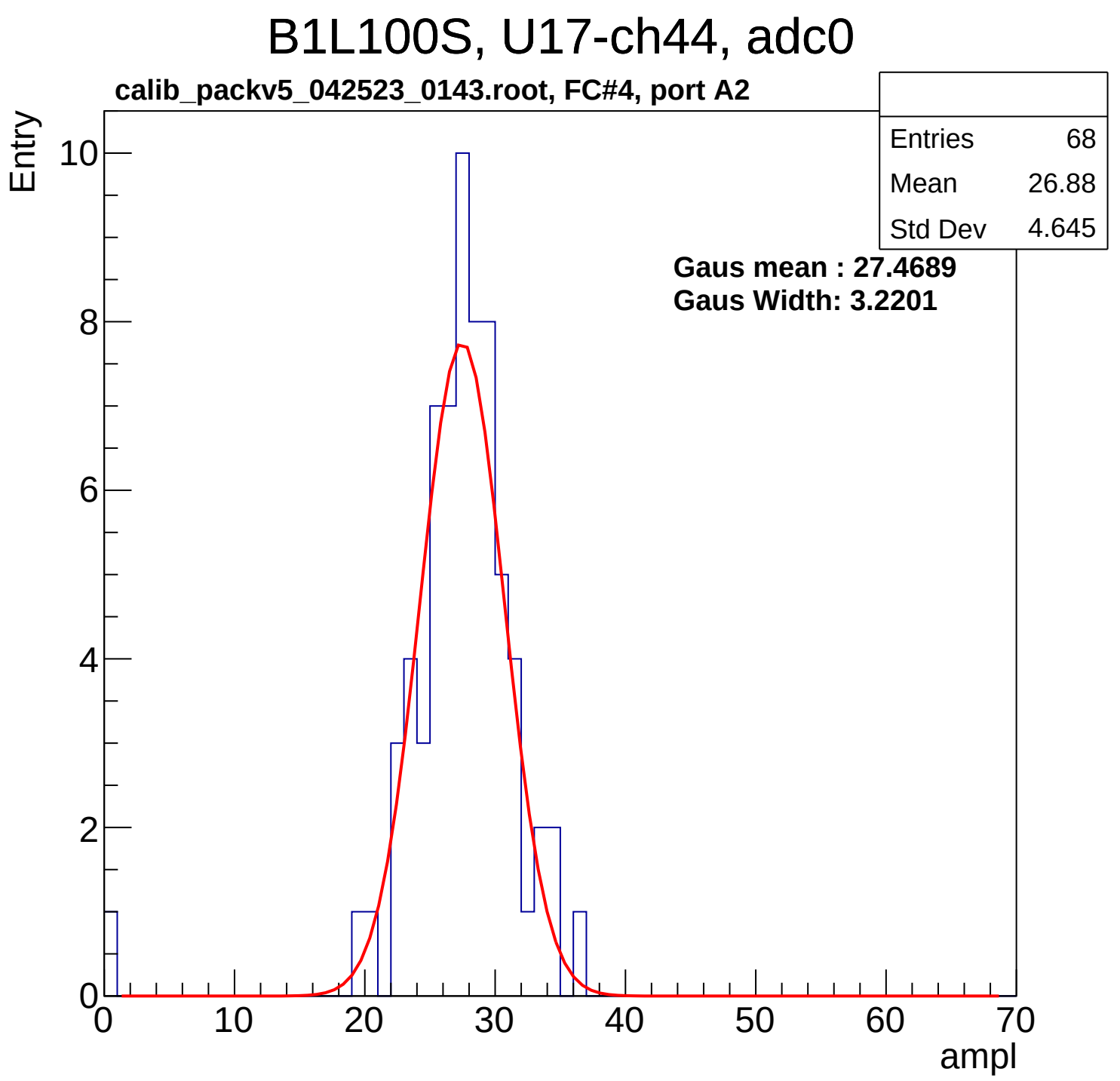
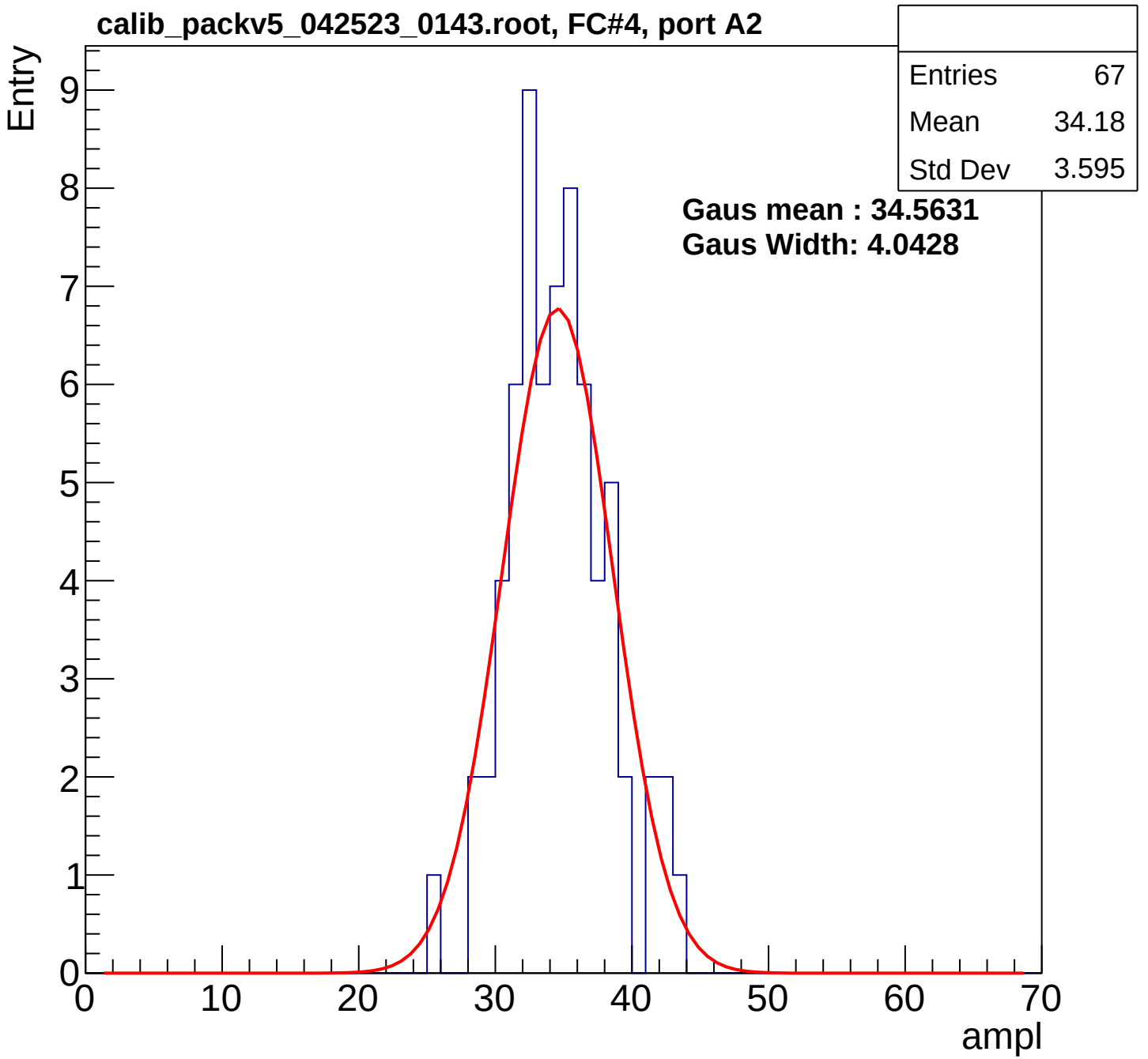
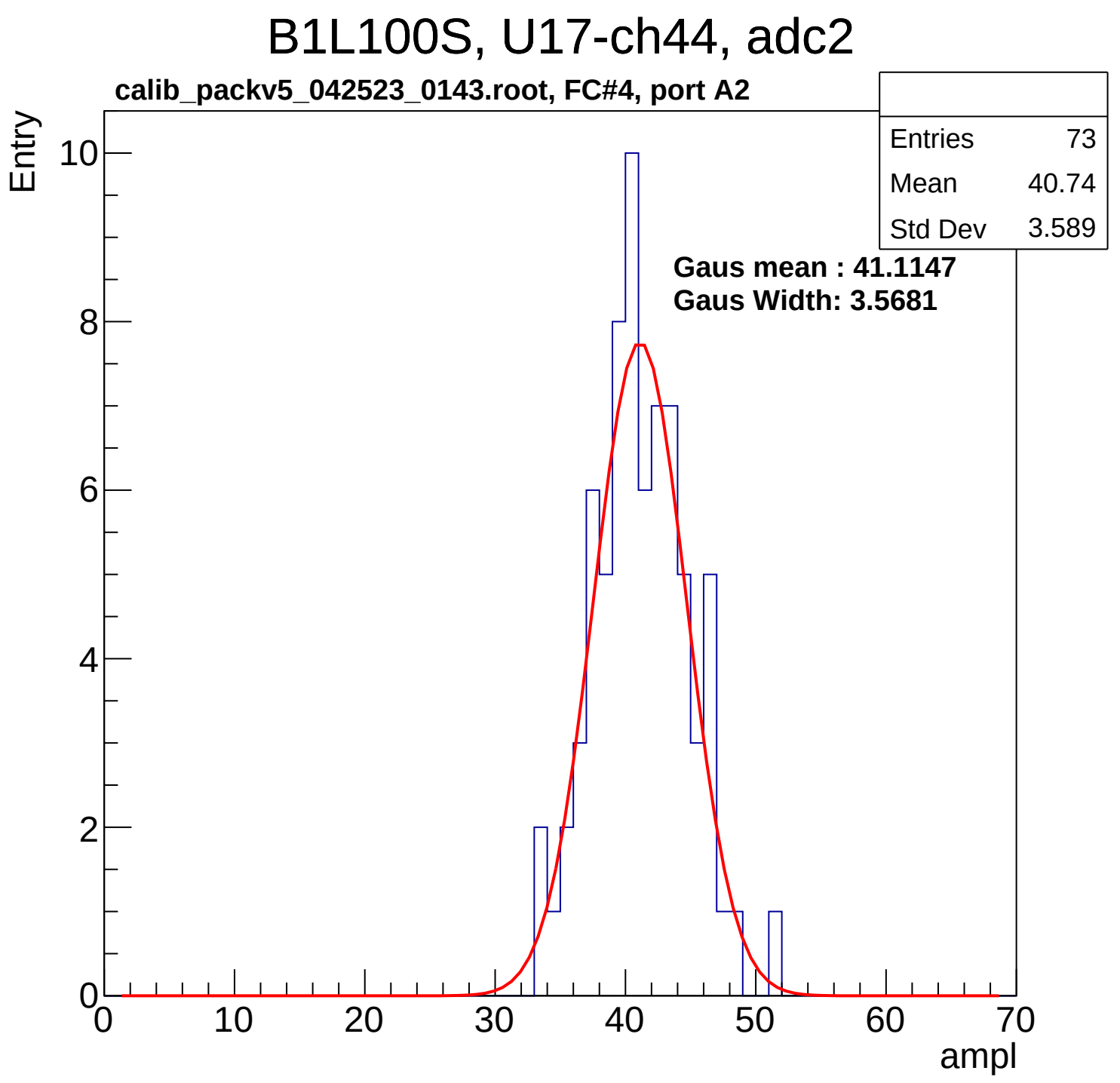
40
50
60
70

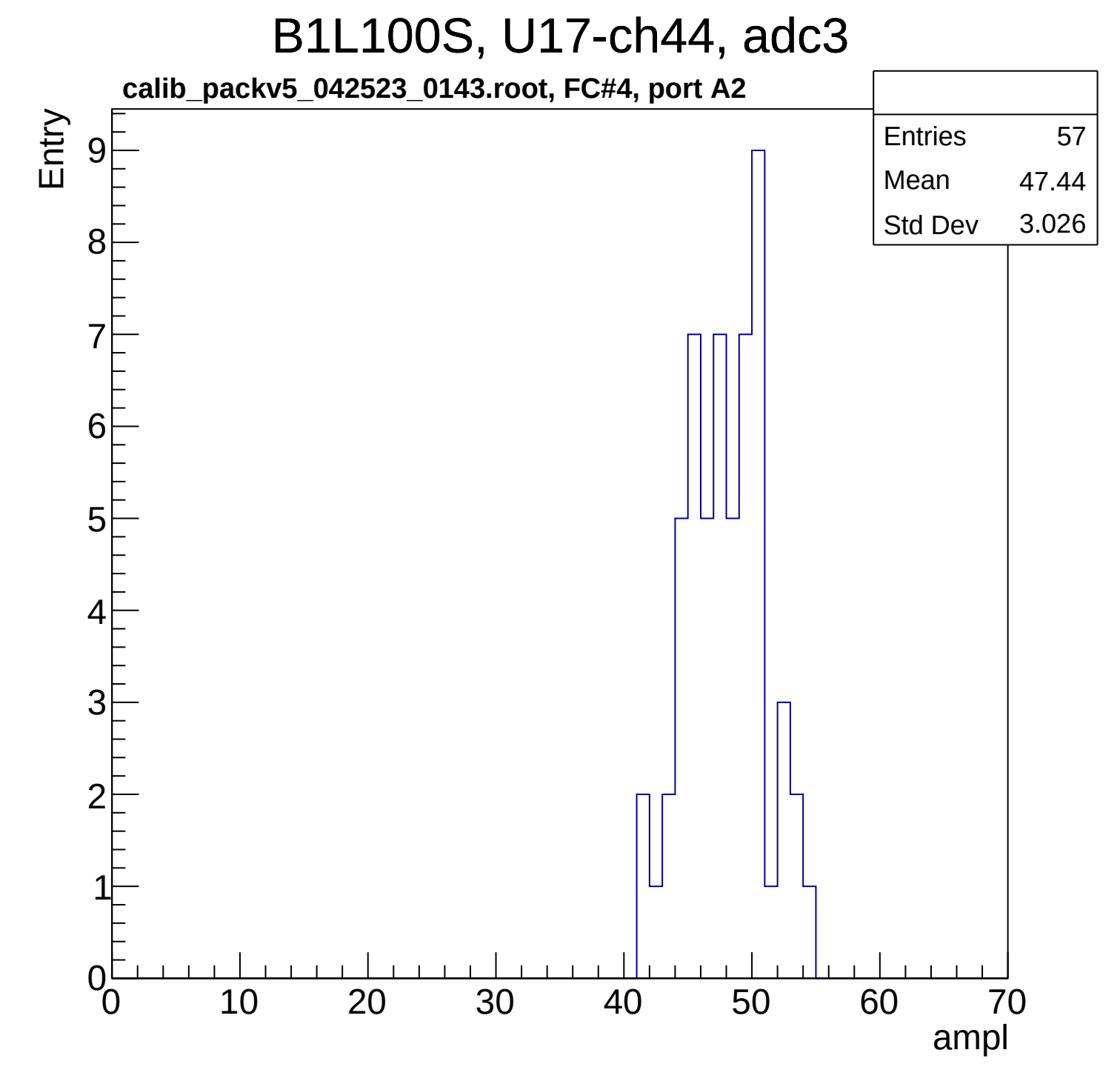

B1L100S, U17-ch43, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 62
Std Dev 1
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

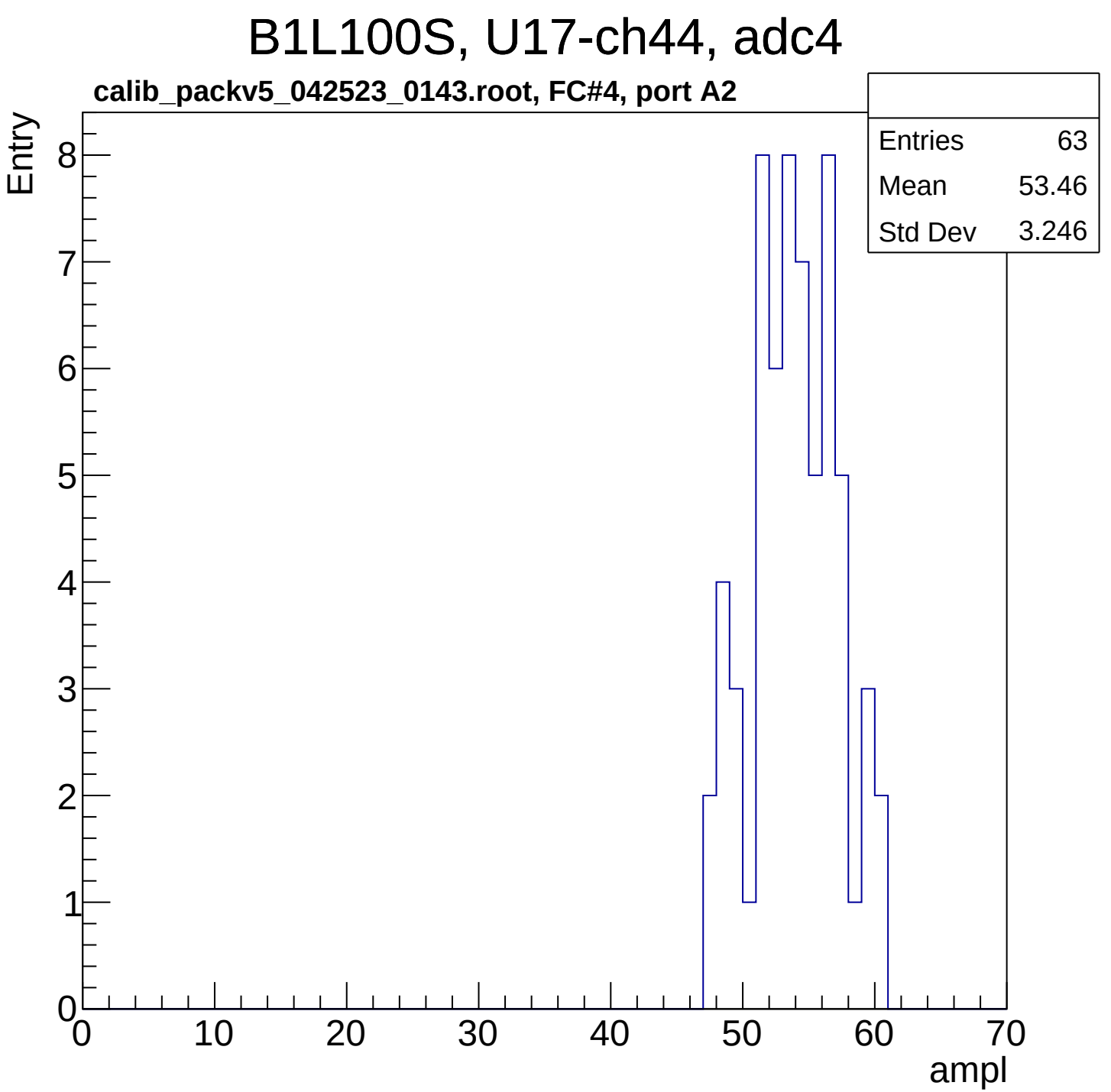

B1L100S, U17-ch43, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 0
Std Dev 0
Entry
3
2.5
2
1.5
1
0.5
0
0
10
20
30
40
50
60
70
ampl

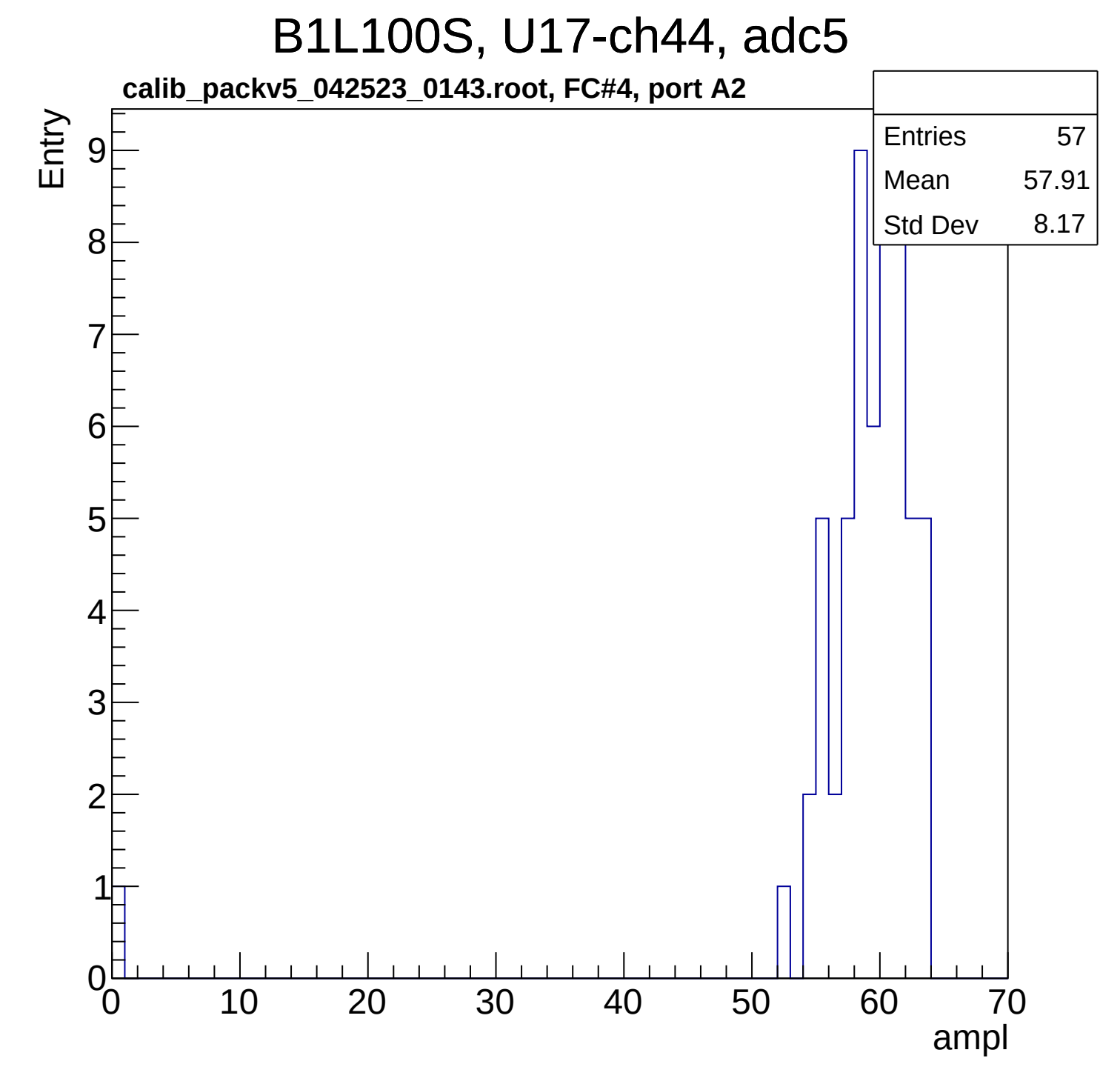

B1L100S, U17-ch44, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 26.88
Std Dev 4.645
Gaus mean : 27.4689
Gaus Width: 3.2201
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U17-ch44, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 34.18
Std Dev 3.595
Gaus mean : 34.5631
Gaus Width: 4.0428
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch44, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 40.74
Std Dev 3.589
Gaus mean : 41.1147
Gaus Width: 3.5681
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U17-ch44, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 47.44
Std Dev 3.026
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch44, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 53.46
Std Dev 3.246
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch44, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 57.91
Std Dev 8.17
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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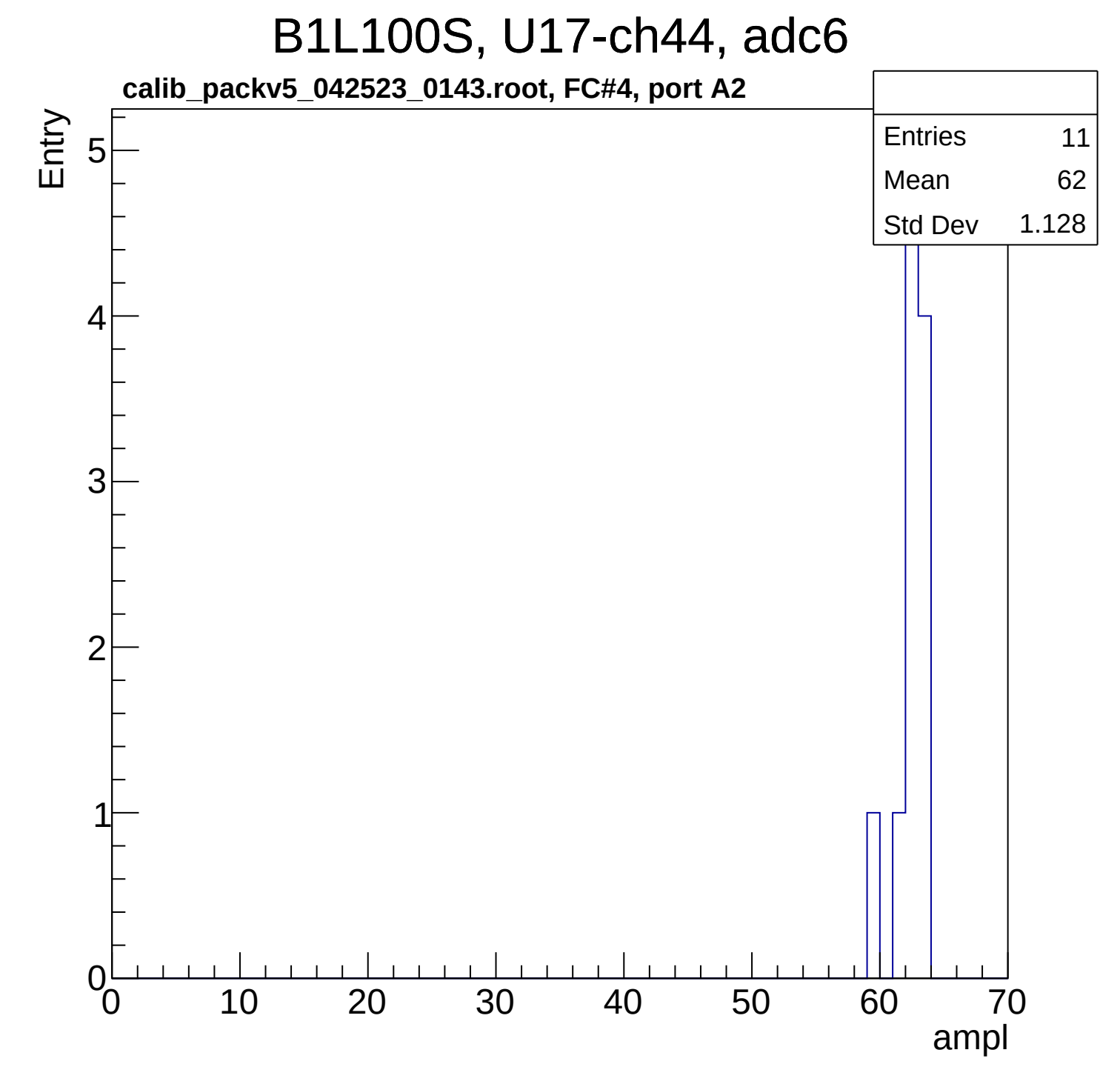
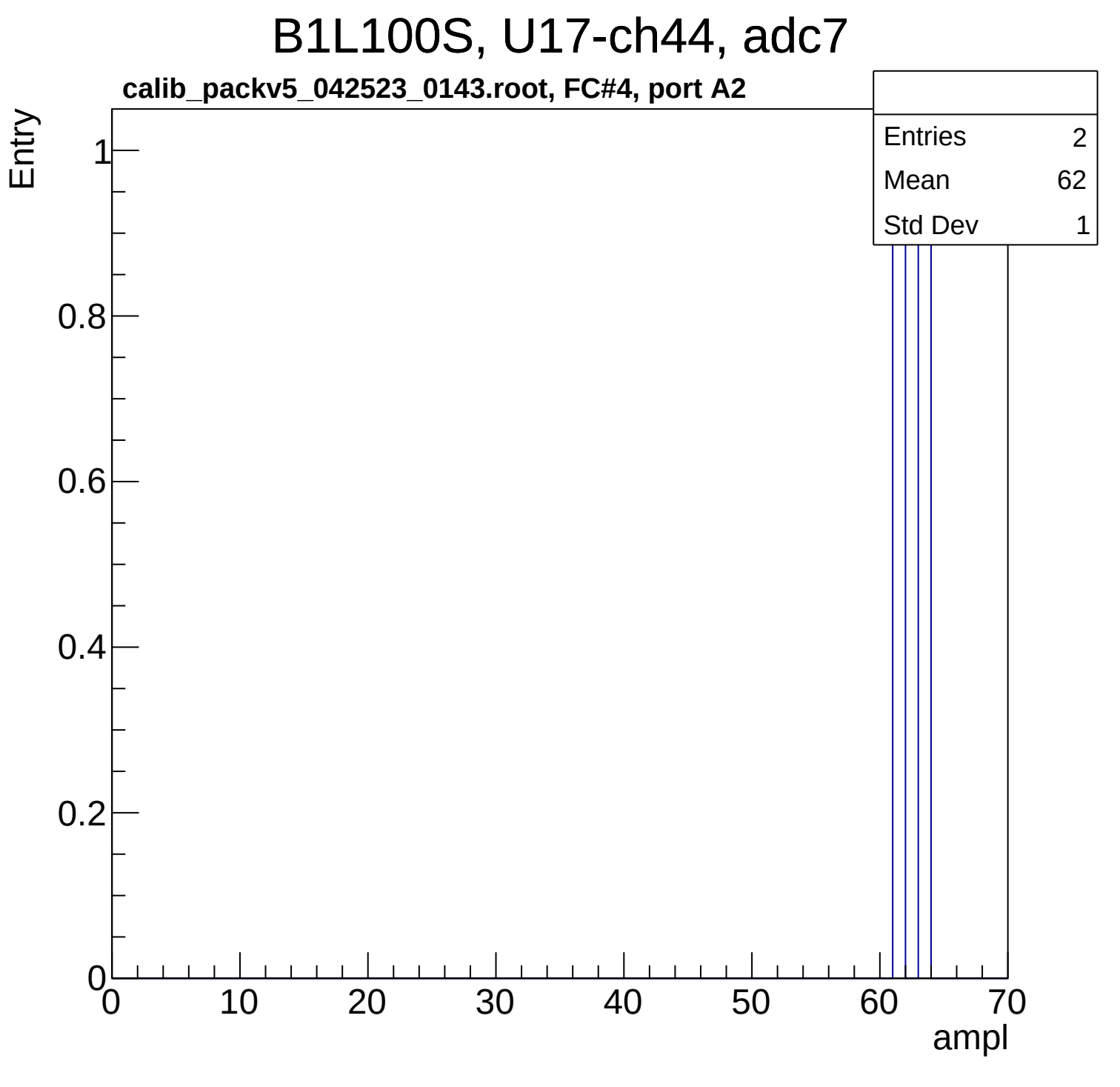
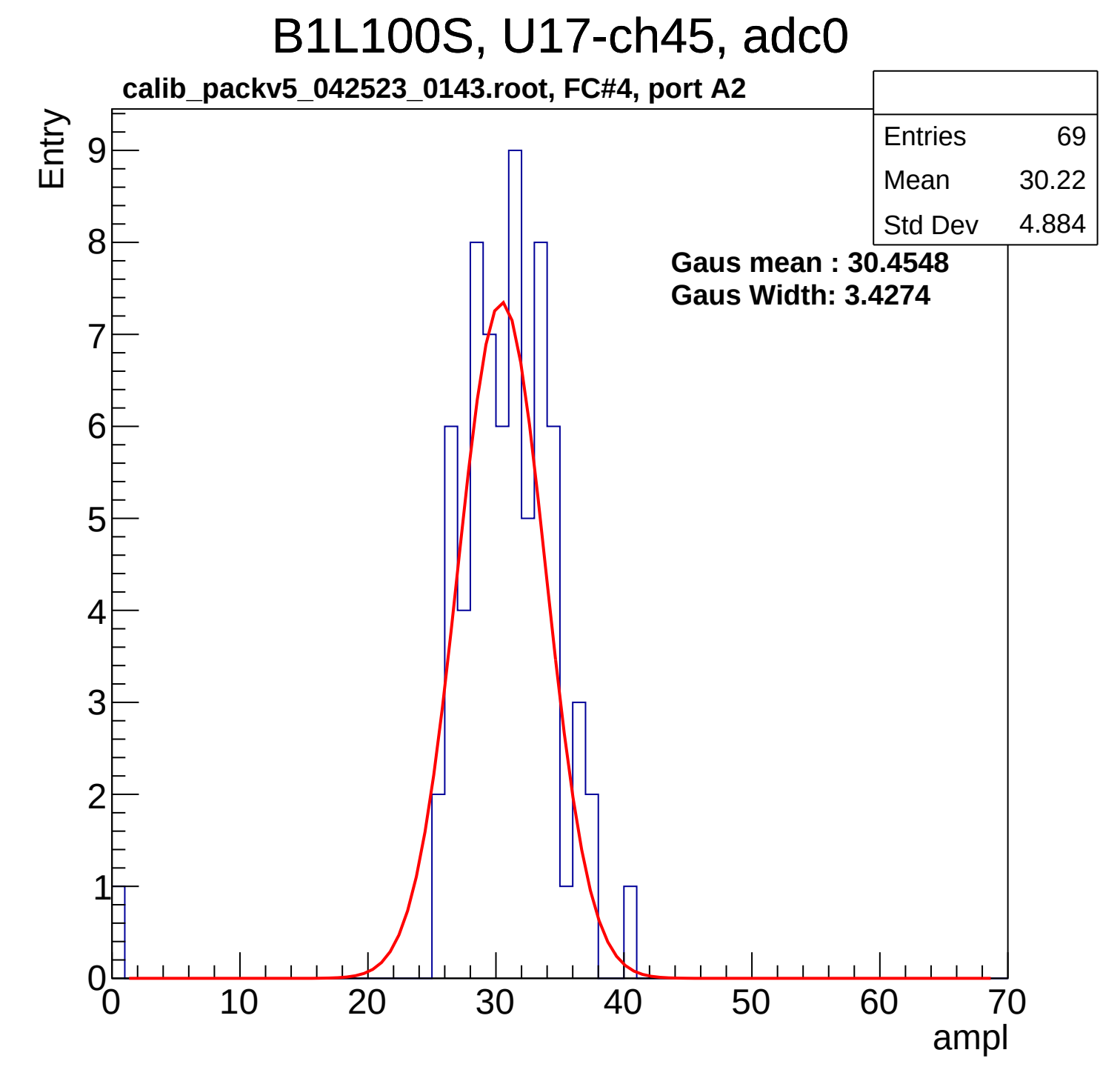
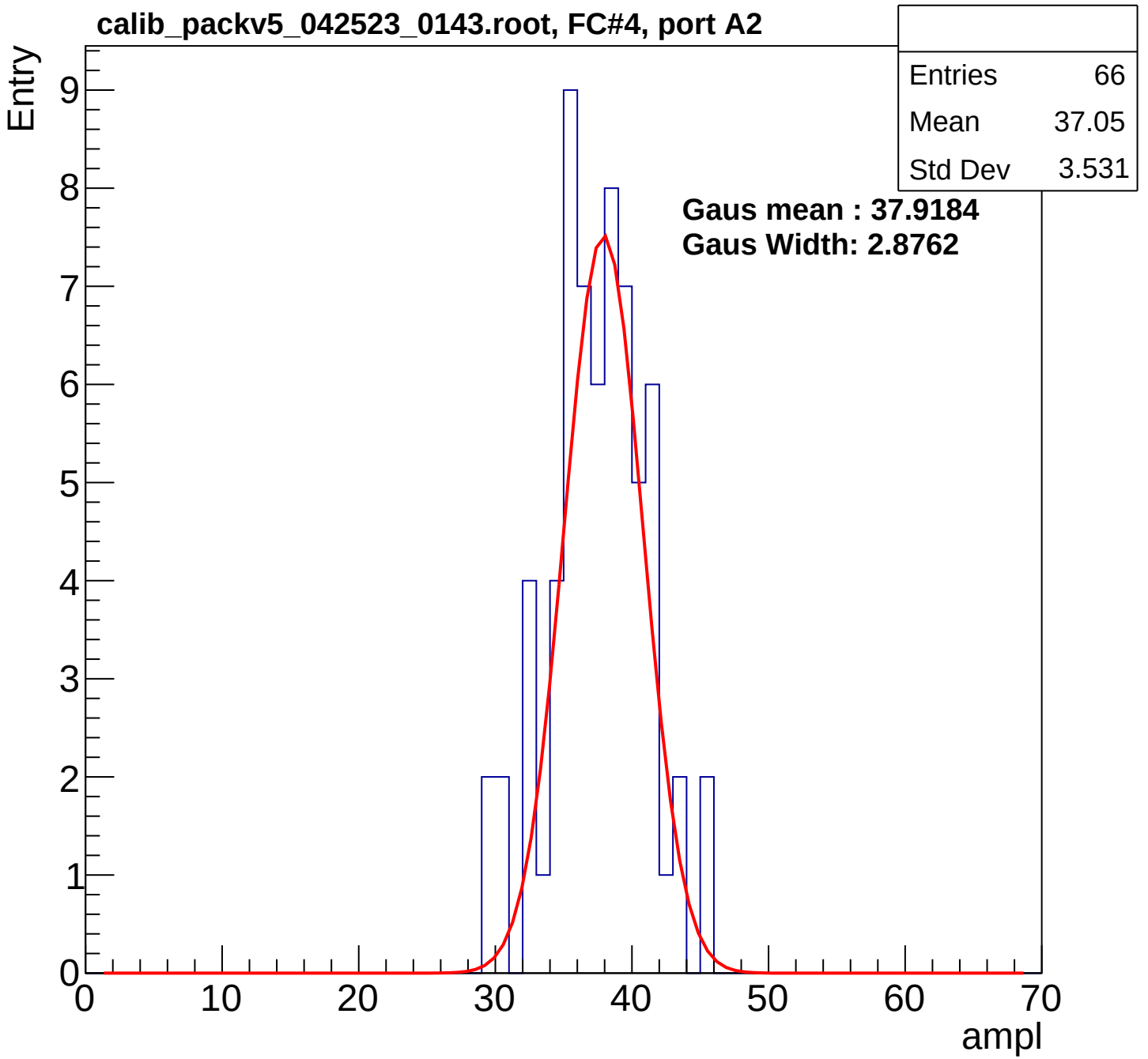
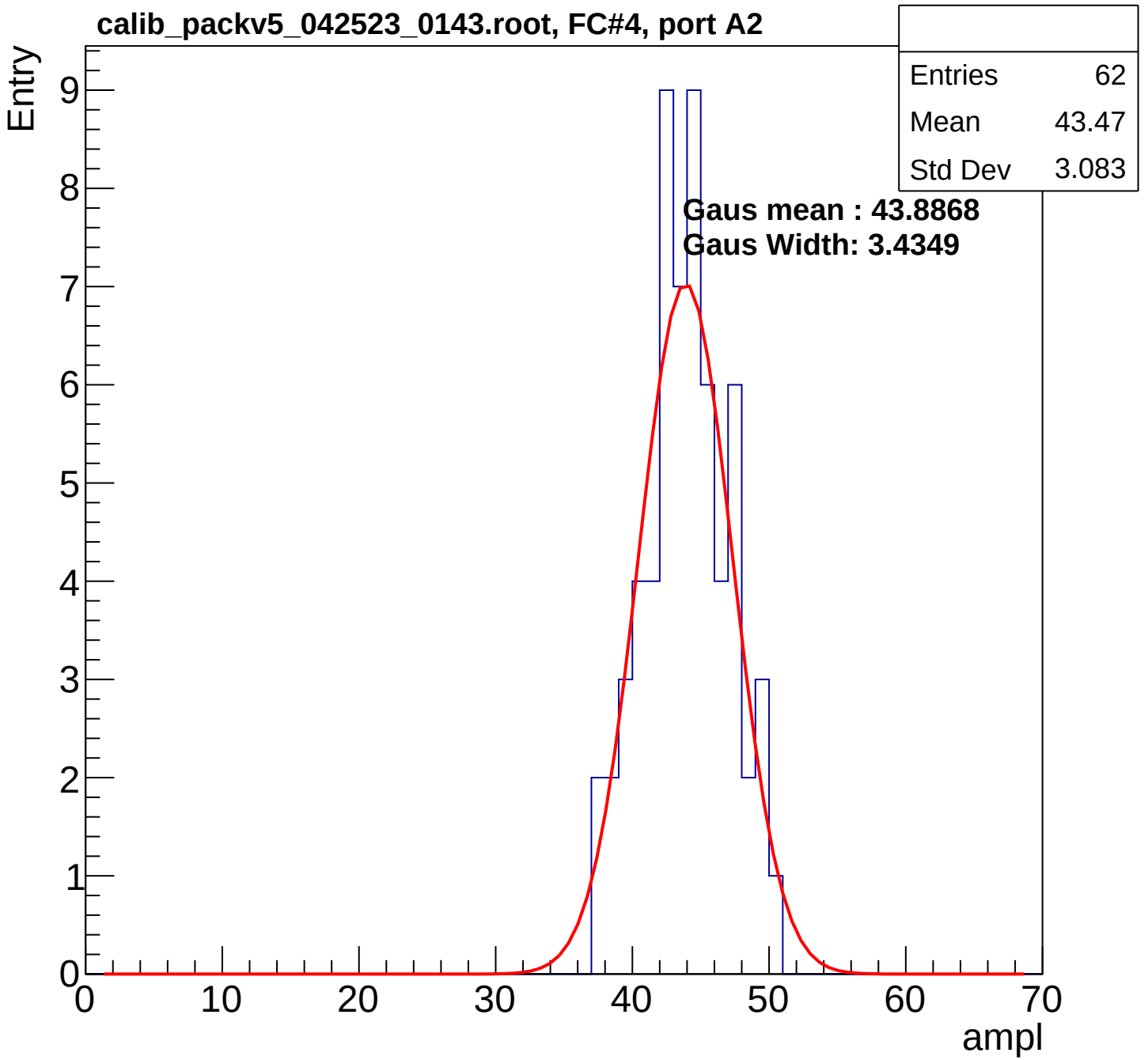
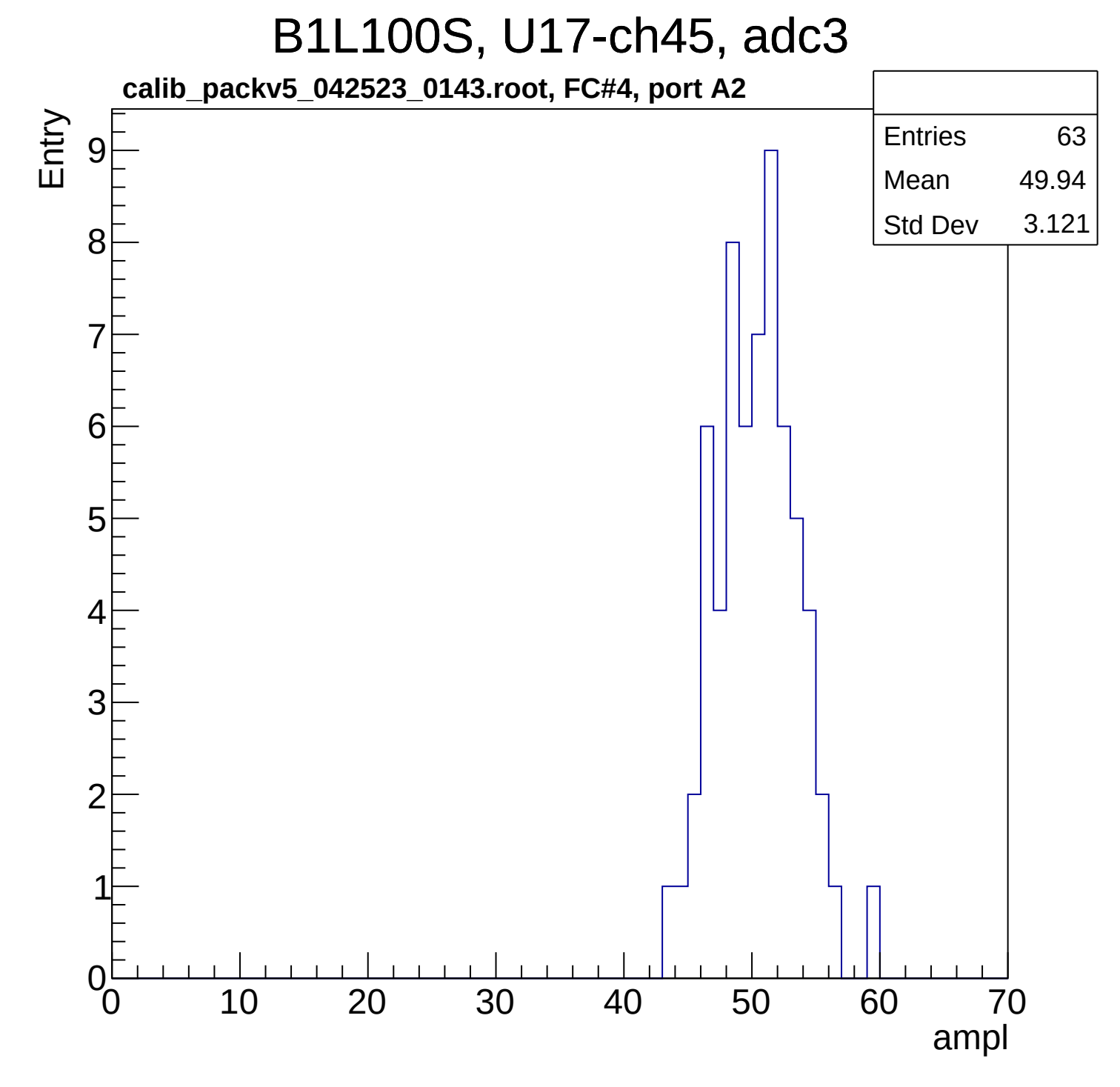

B1L100S, U17-ch44, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 11
Mean 62
Std Dev 1.128
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch44, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 62
Std Dev 1
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch45, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 30.22
Std Dev 4.884
Gaus mean : 30.4548
Gaus Width: 3.4274
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch45, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 37.05
Std Dev 3.531
Gaus mean : 37.9184
Gaus Width: 2.8762
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch45, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 43.47
Std Dev 3.083
Gaus mean : 43.8868
Gaus Width: 3.4349
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch45, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 49.94
Std Dev 3.121
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
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40
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60
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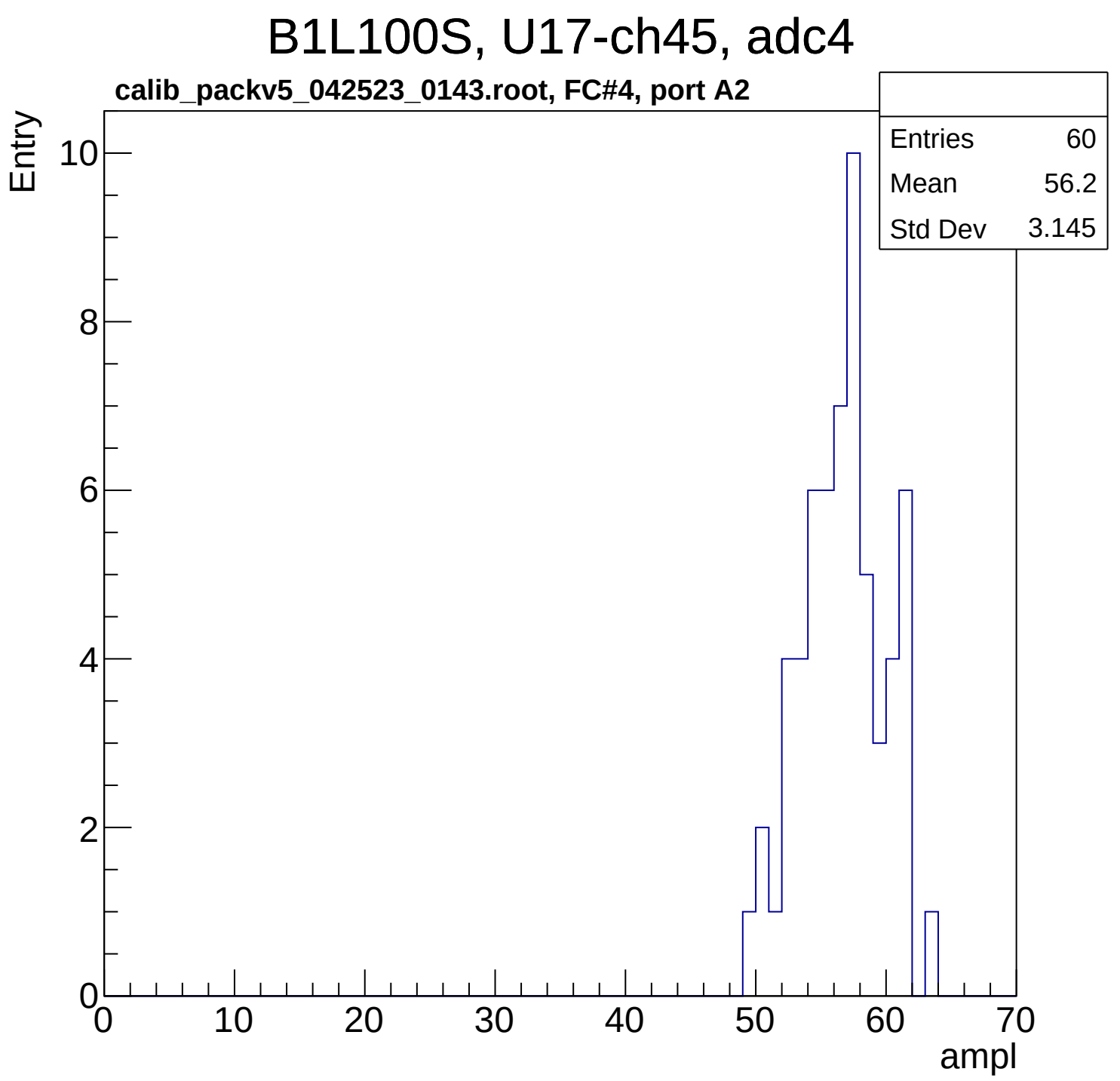
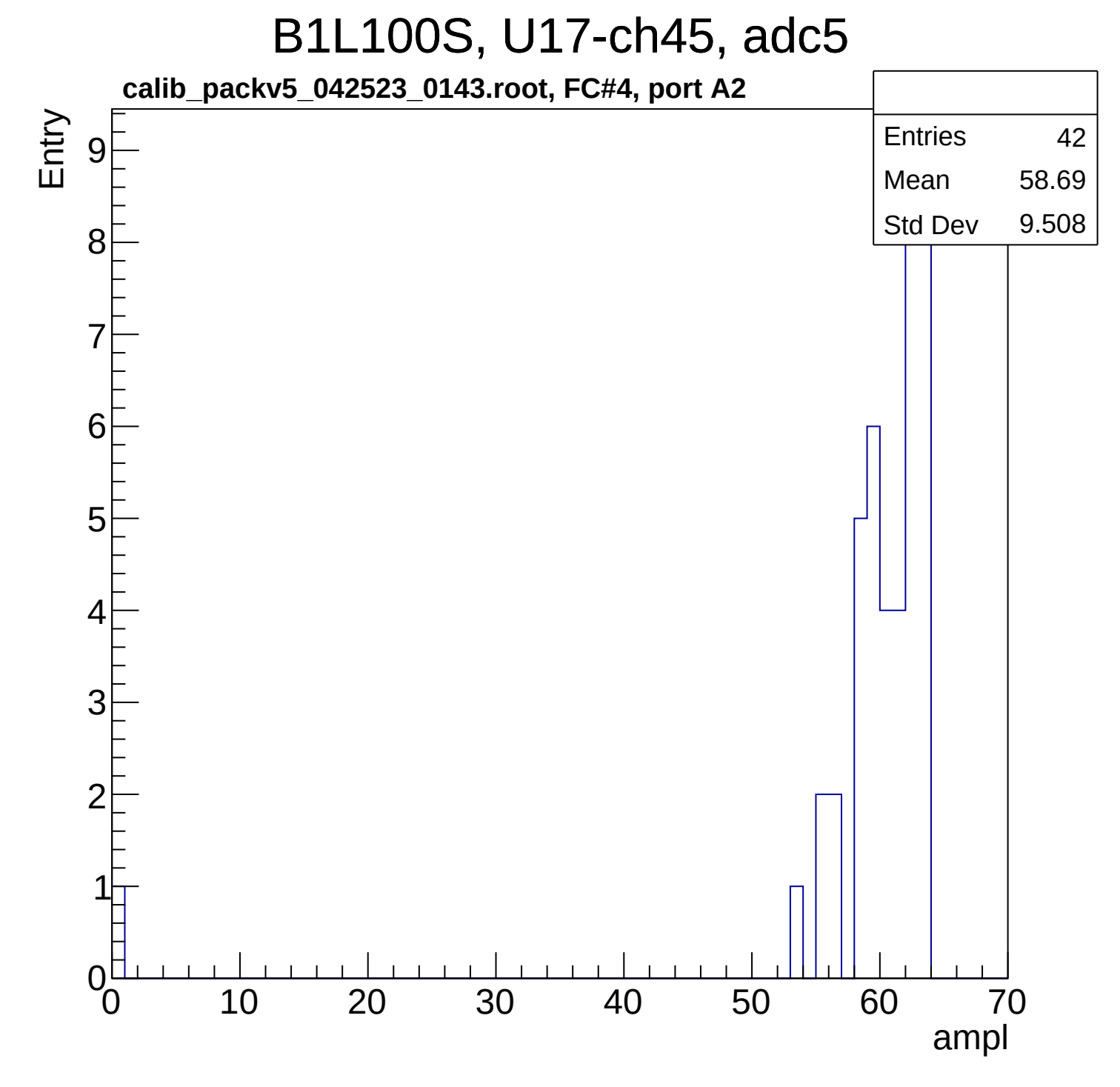

B1L100S, U17-ch45, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 56.2
Std Dev 3.145
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch45, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 42
Mean 58.69
Std Dev 9.508
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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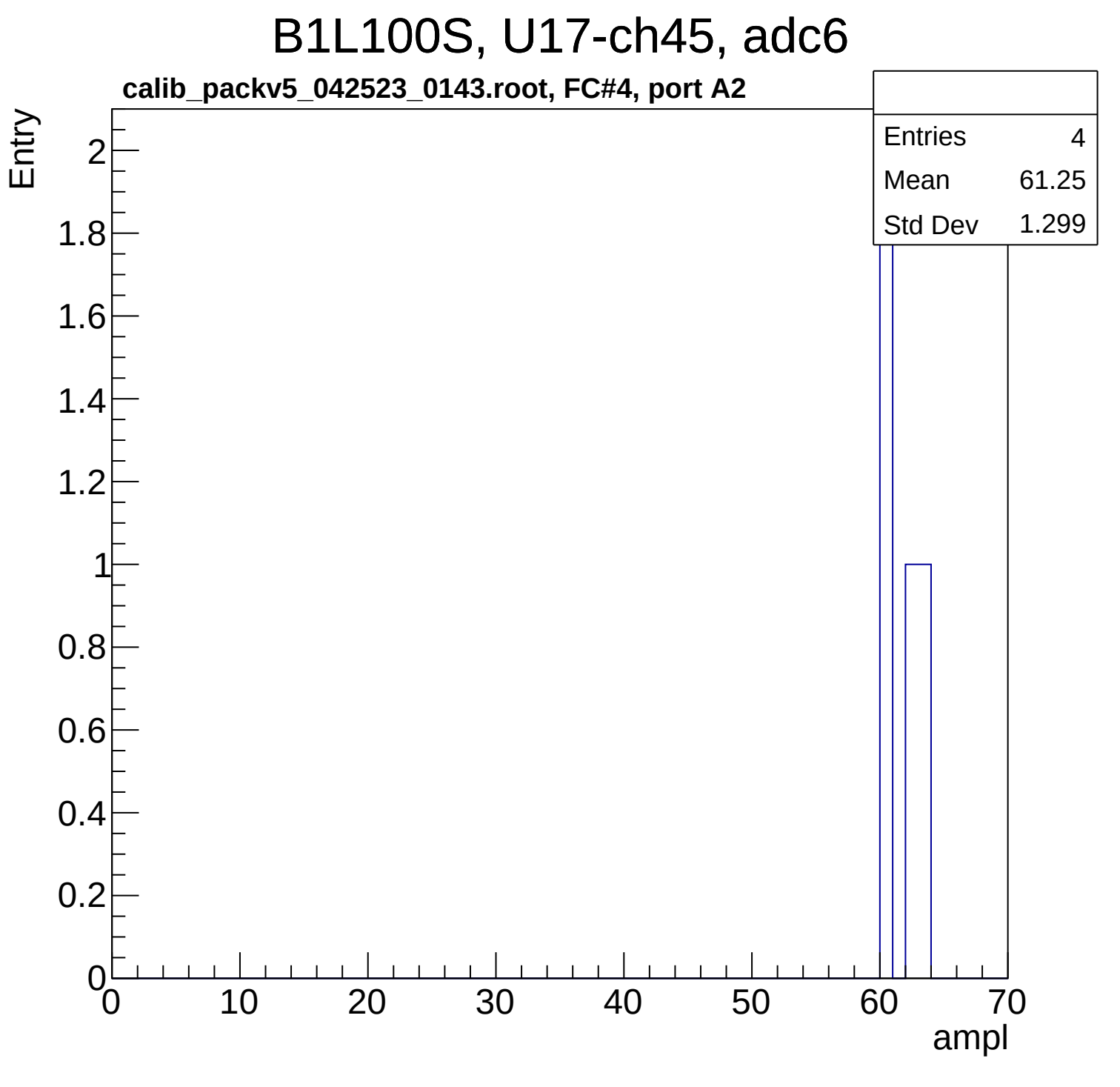
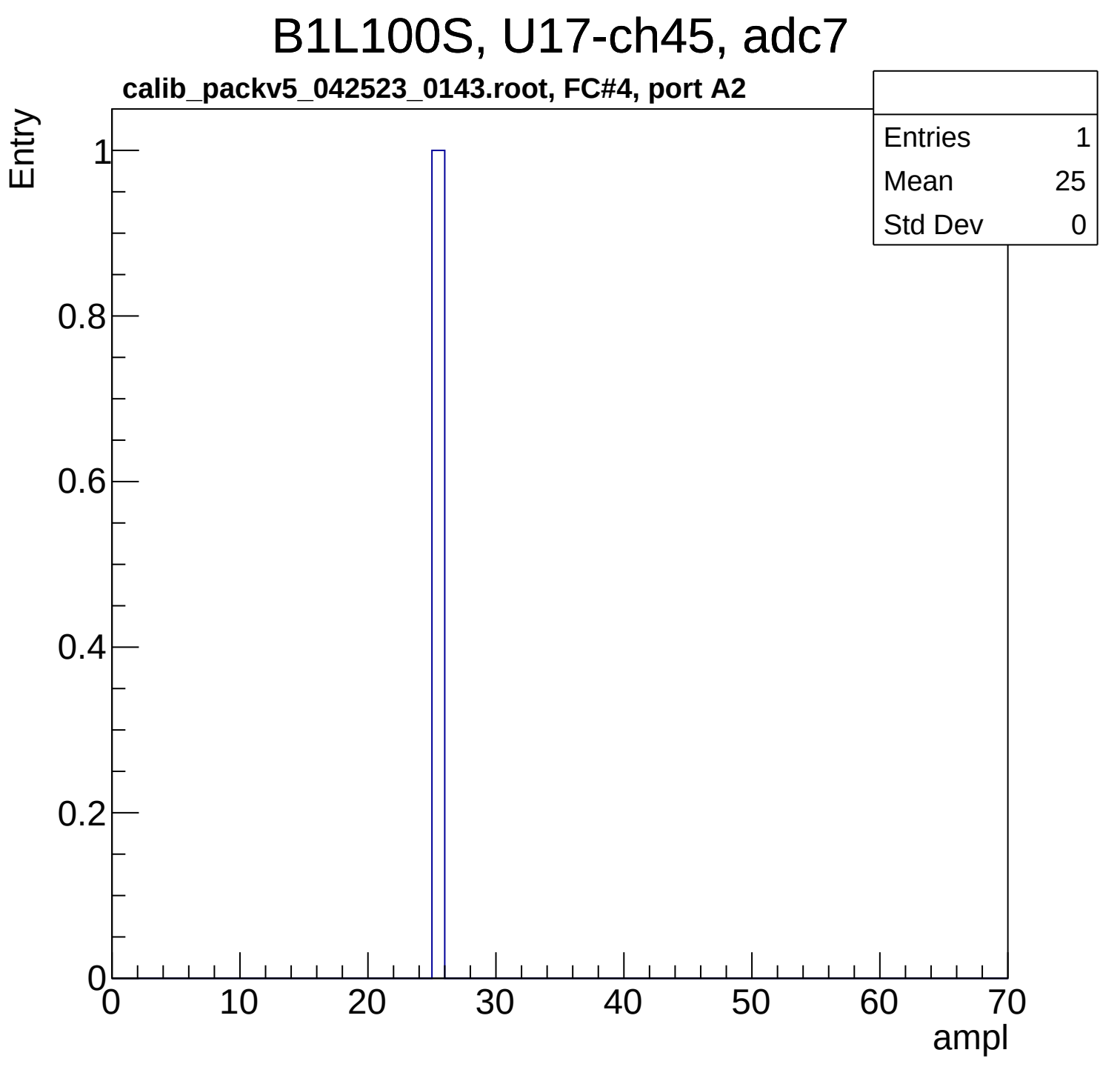

B1L100S, U17-ch45, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 4
Mean 61.25
Std Dev 1.299
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L100S, U17-ch45, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 25
Std Dev 0
Entry
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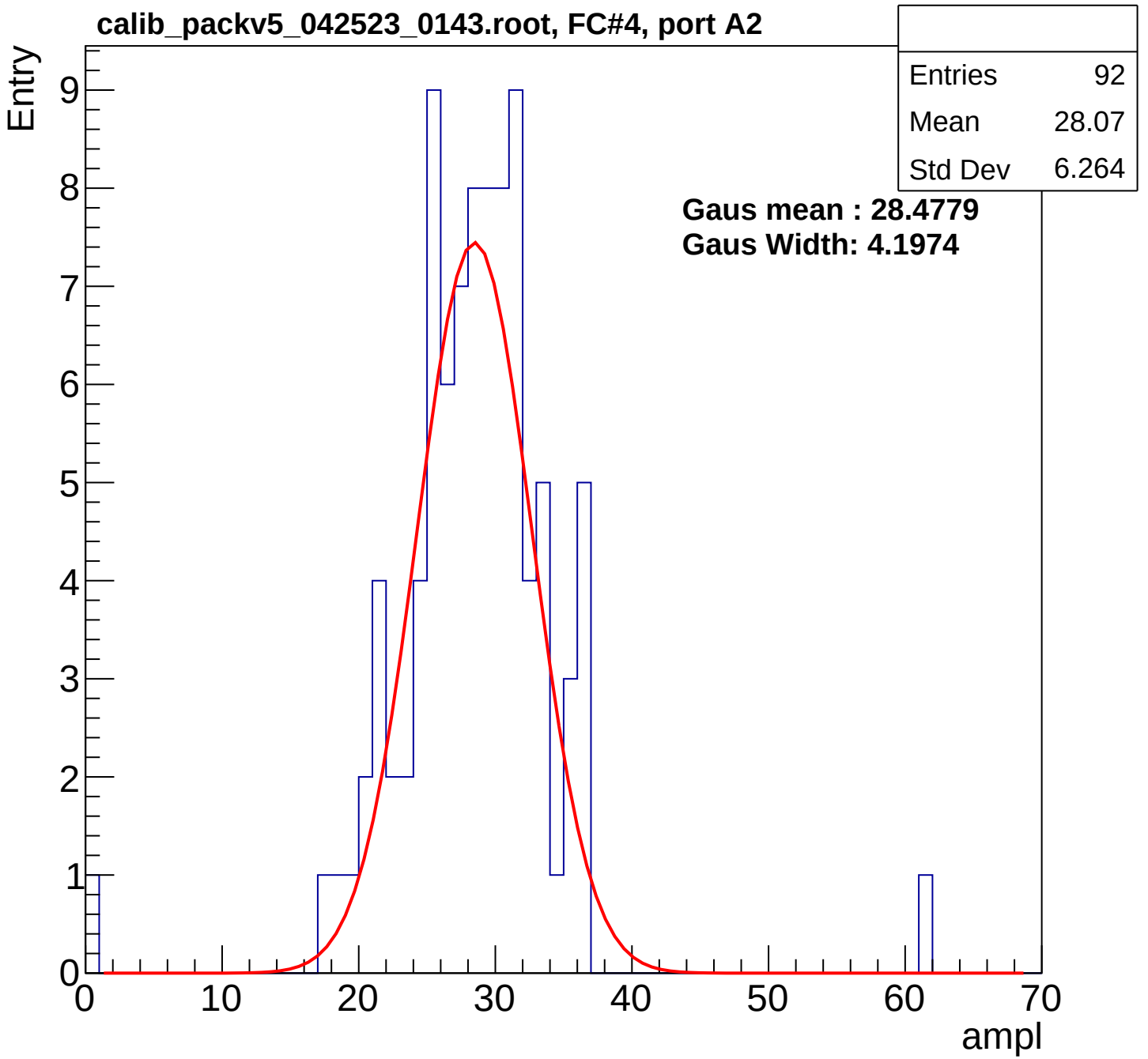
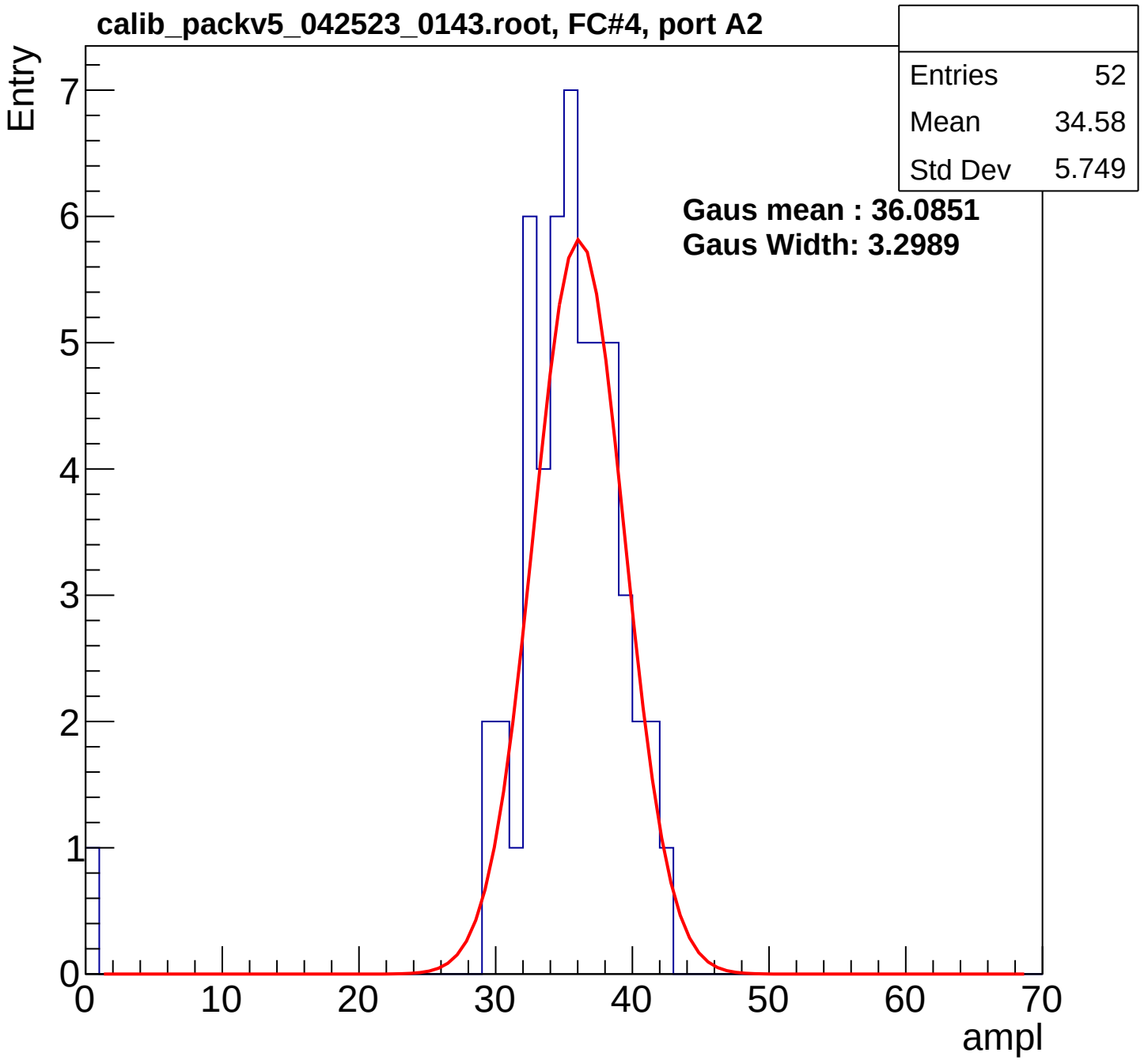
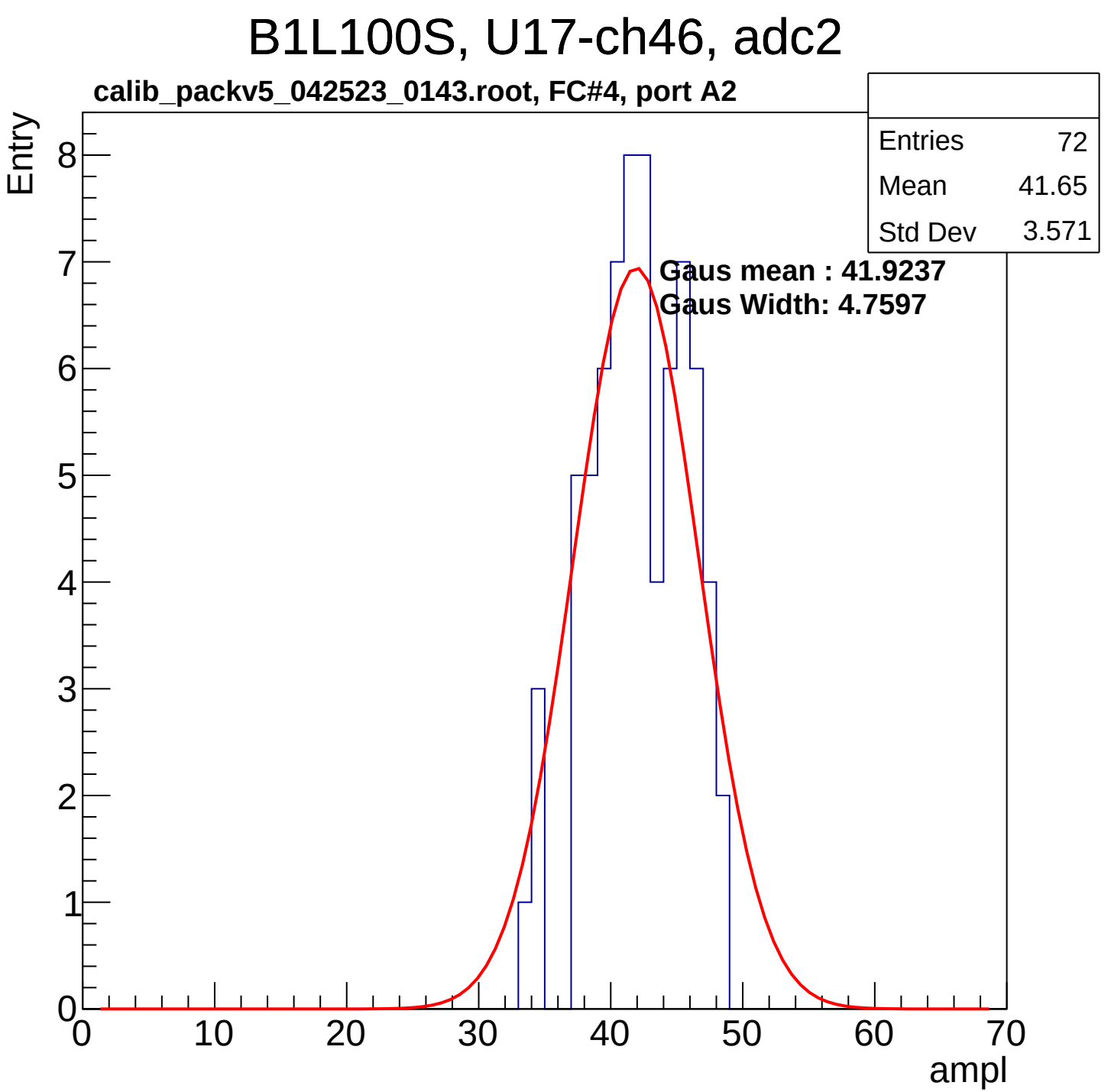
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch46, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 92
Mean 28.07
Std Dev 6.264
Gaus mean : 28.4779
Gaus Width: 4.1974
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch46, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 52
Mean 34.58
Std Dev 5.749
Gaus mean : 36.0851
Gaus Width: 3.2989
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U17-ch46, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 41.65
Std Dev 3.571
Gaus mean : 41.9237
Gaus Width: 4.7597
Entry
ampl
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1
2
3
4
5
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0
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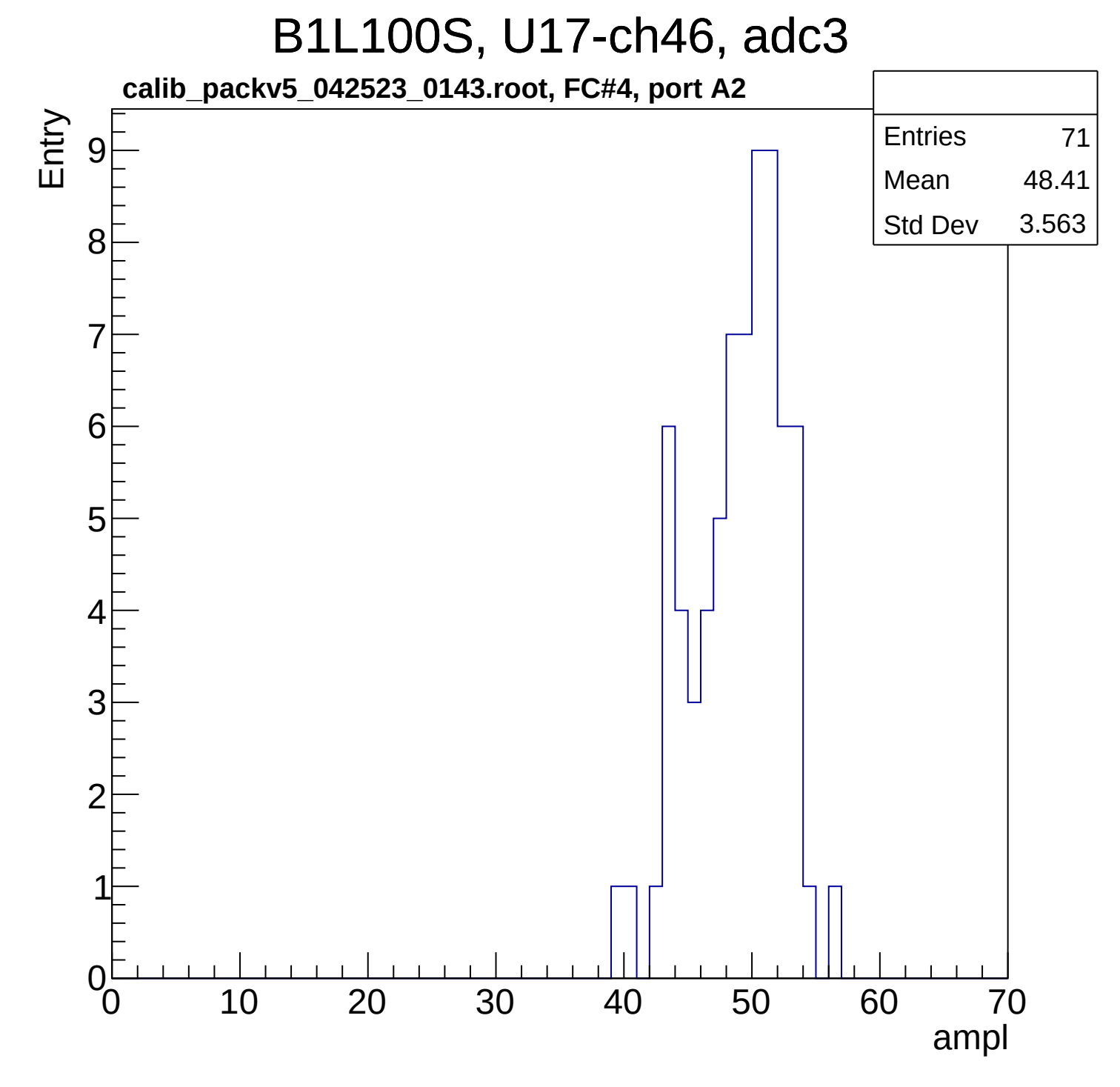
B1L100S, U17-ch46, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 48.41
Std Dev 3.563
Entry
ampl
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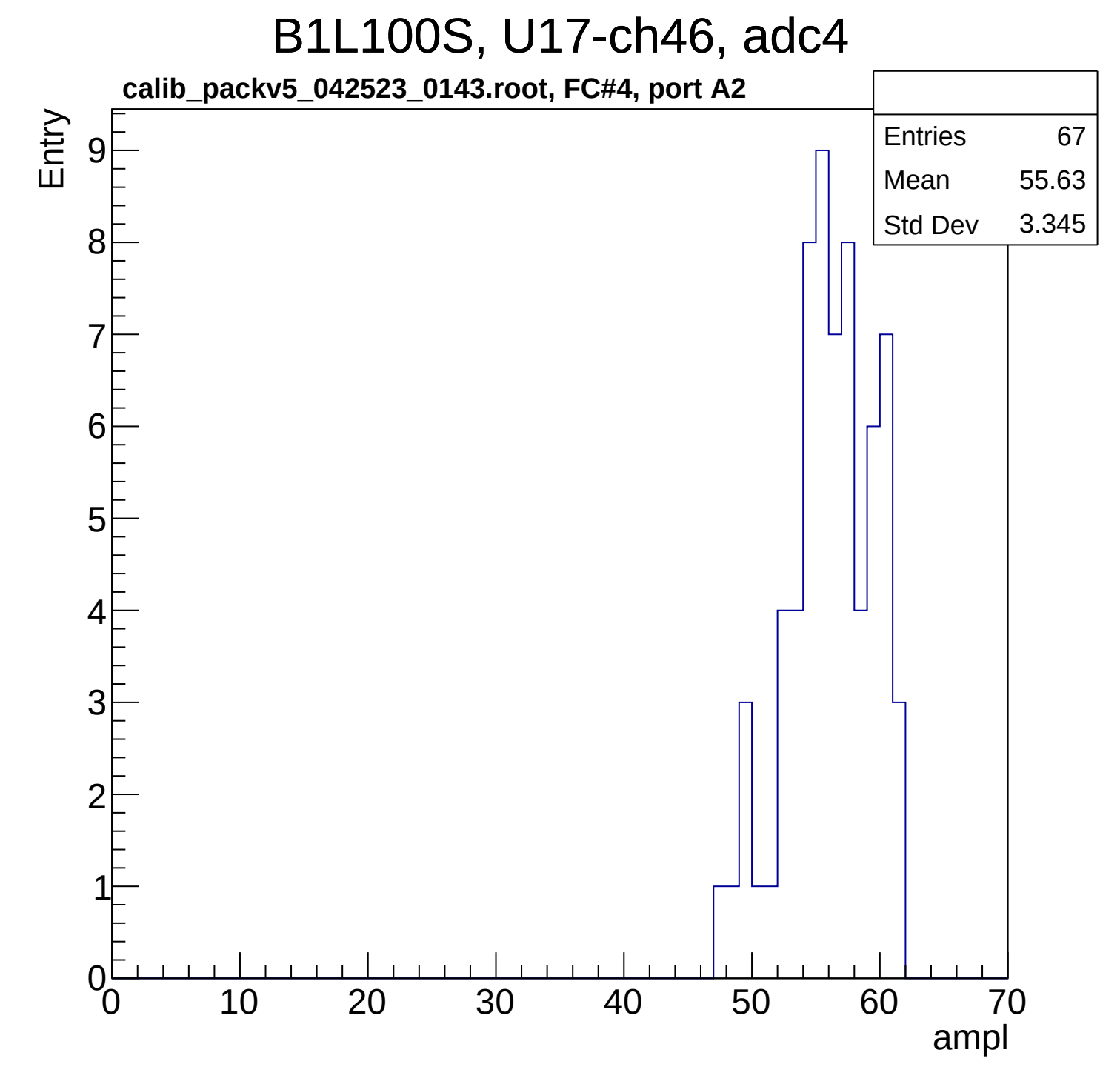
B1L100S, U17-ch46, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 55.63
Std Dev 3.345
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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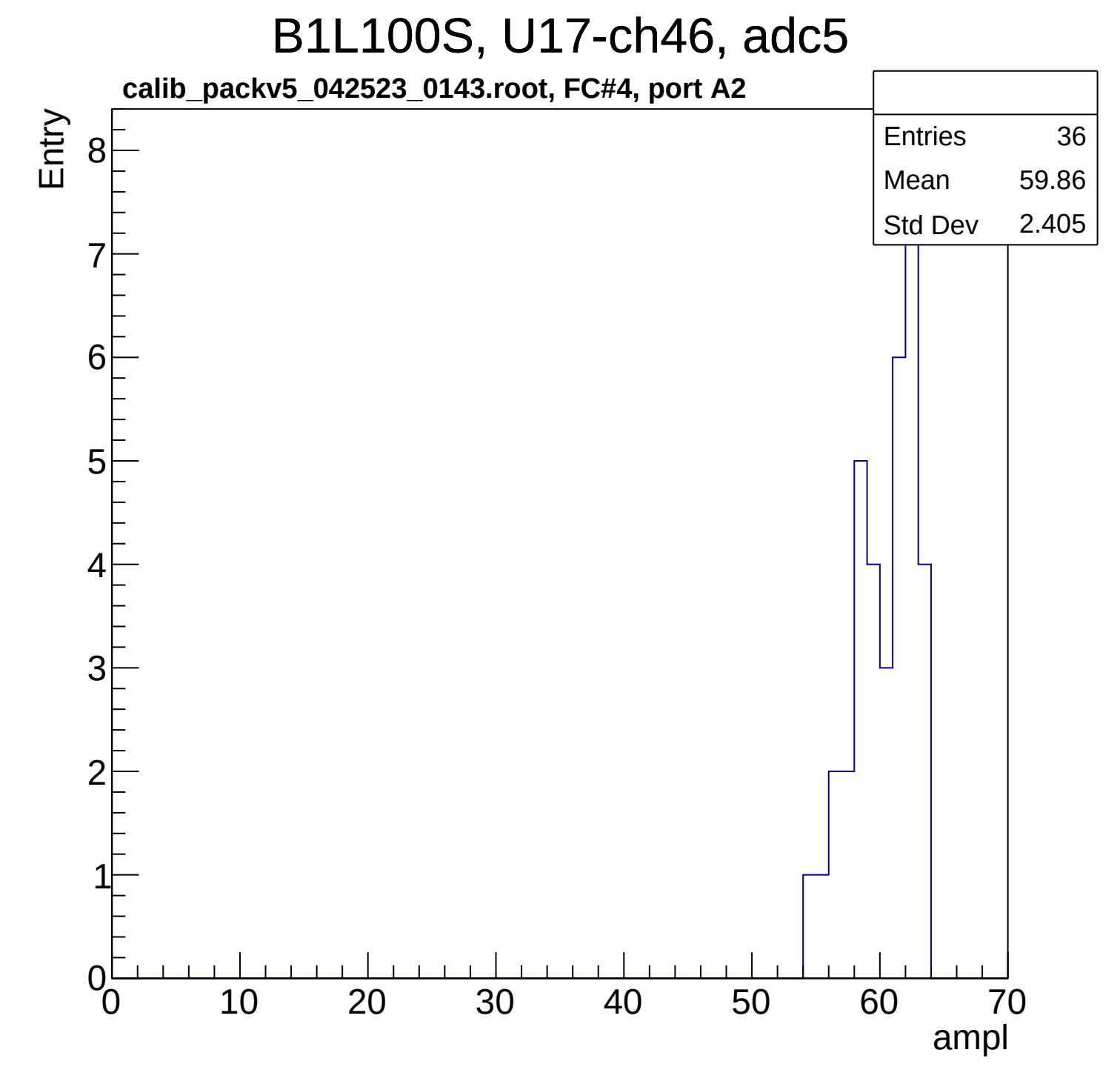
B1L100S, U17-ch46, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 36
Mean 59.86
Std Dev 2.405
Entry
ampl
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1
2
3
4
5
6
7
8
0
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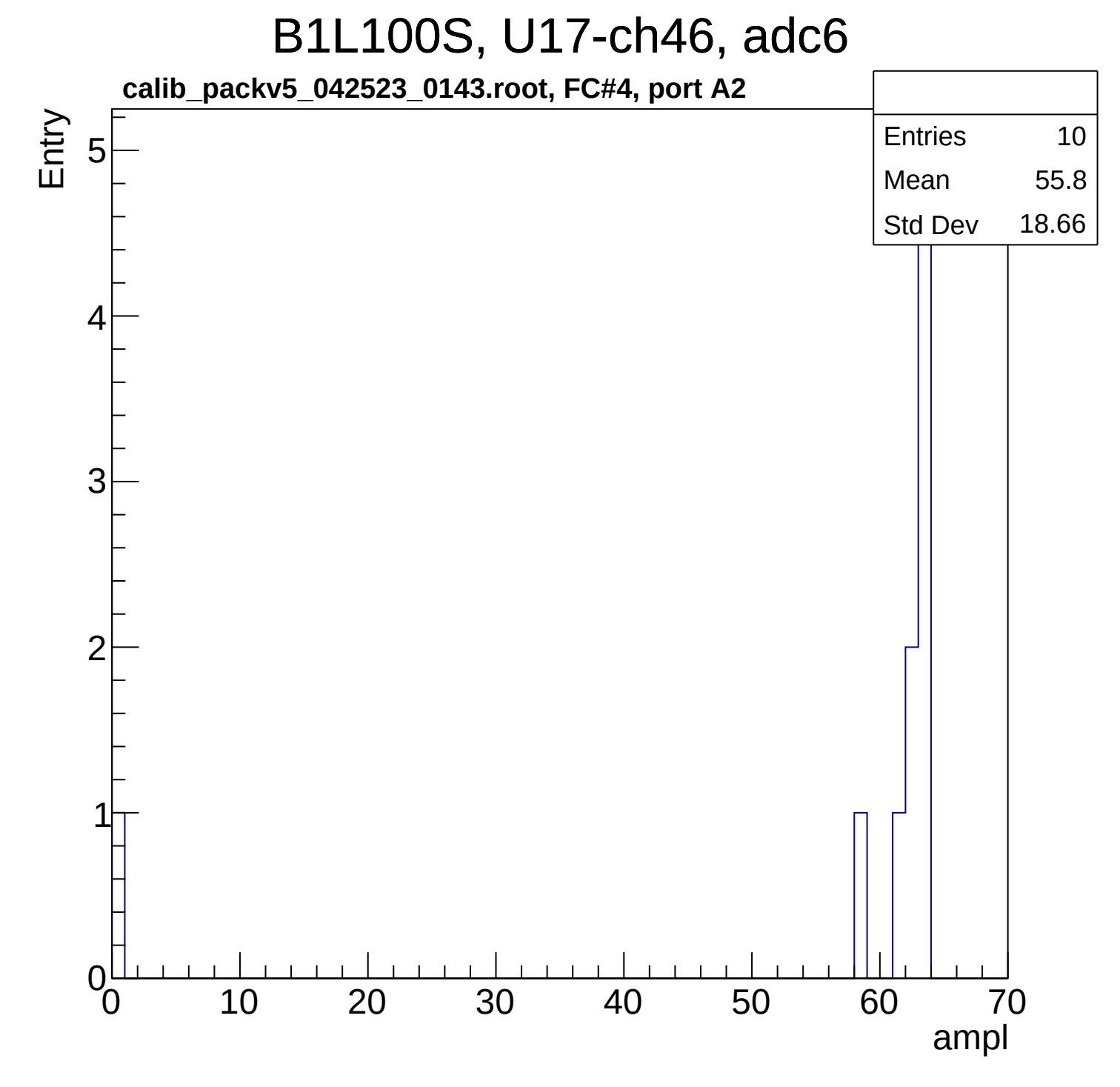
B1L100S, U17-ch46, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 10
Mean 55.8
Std Dev 18.66
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
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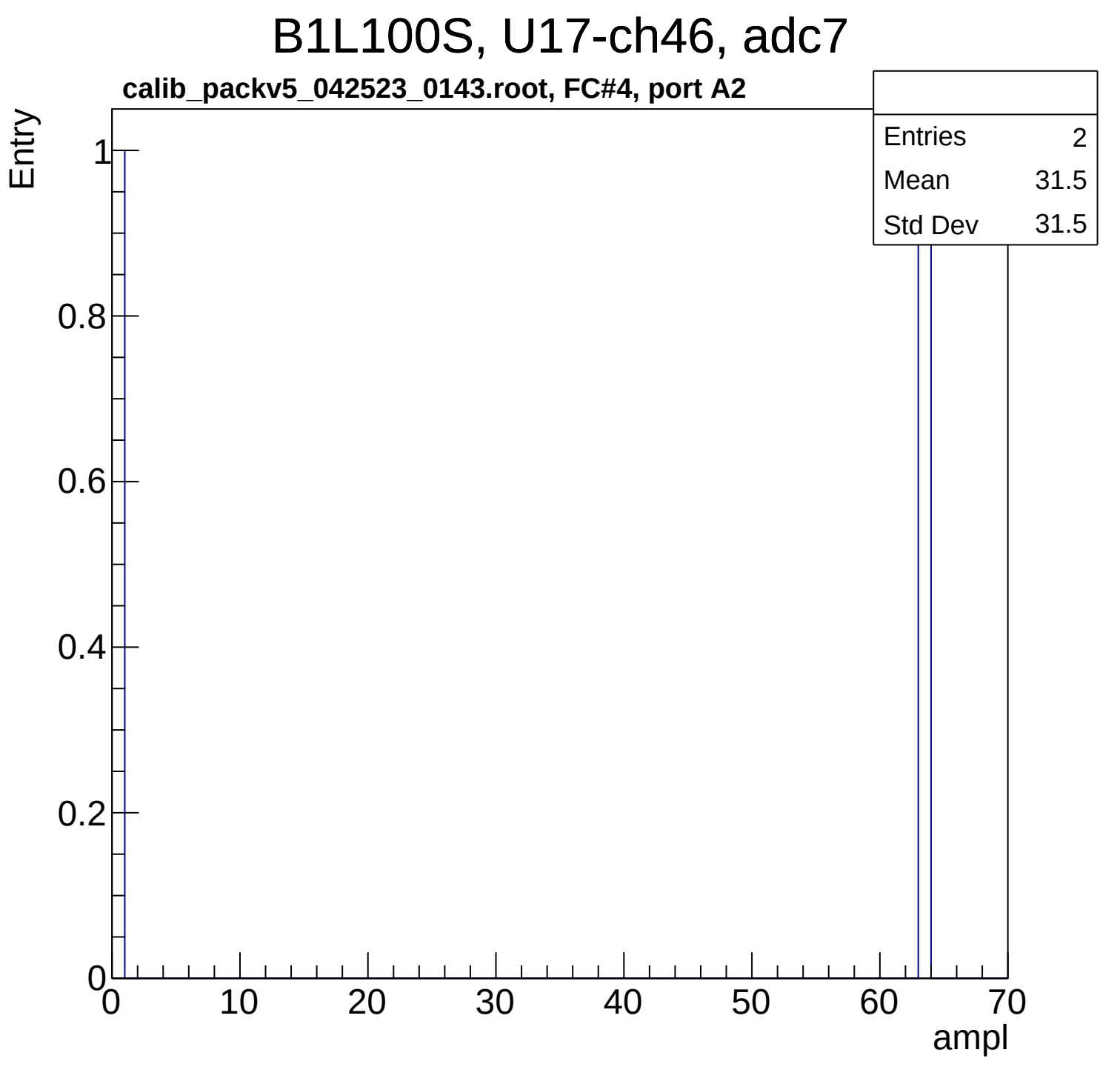
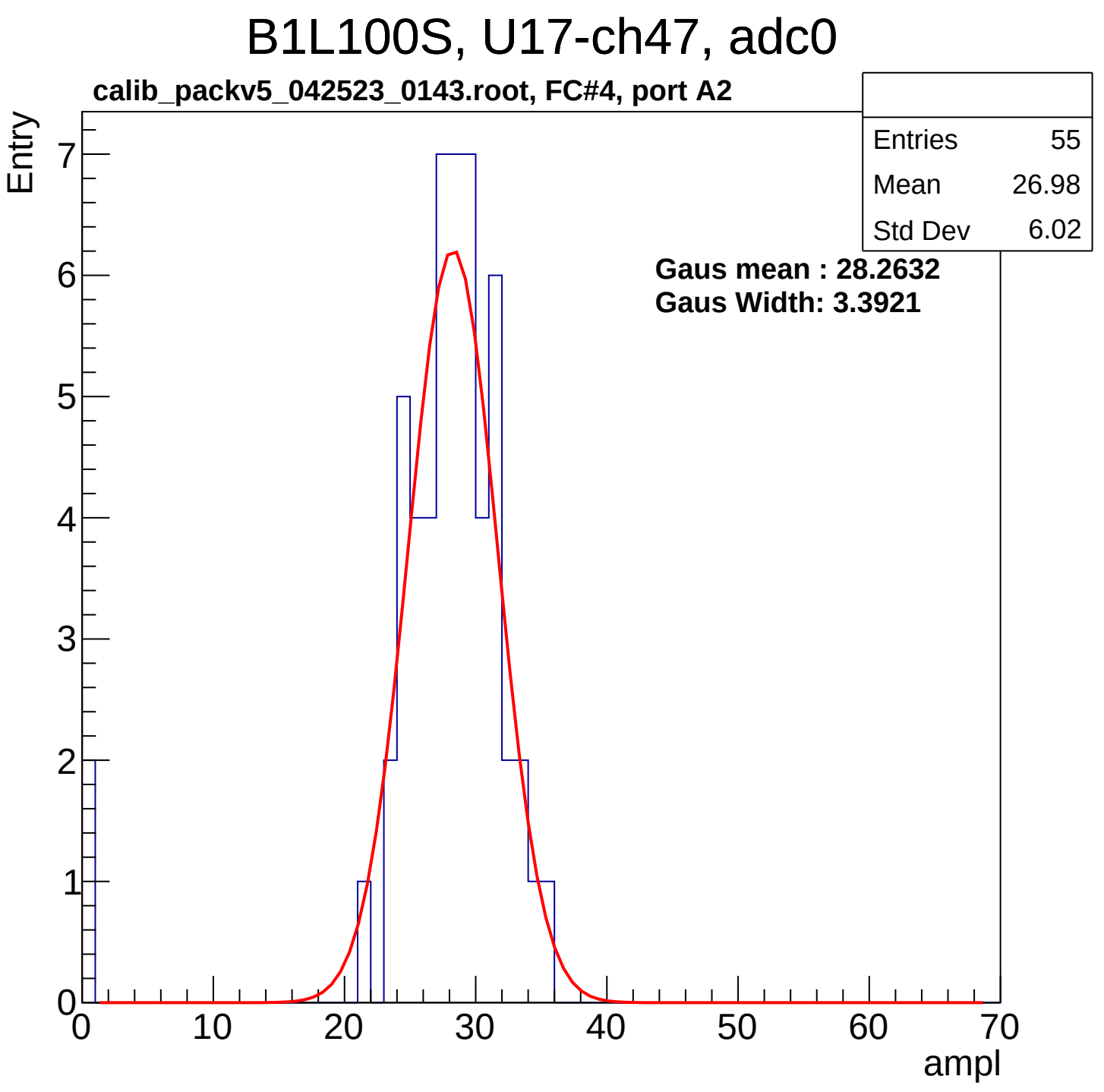
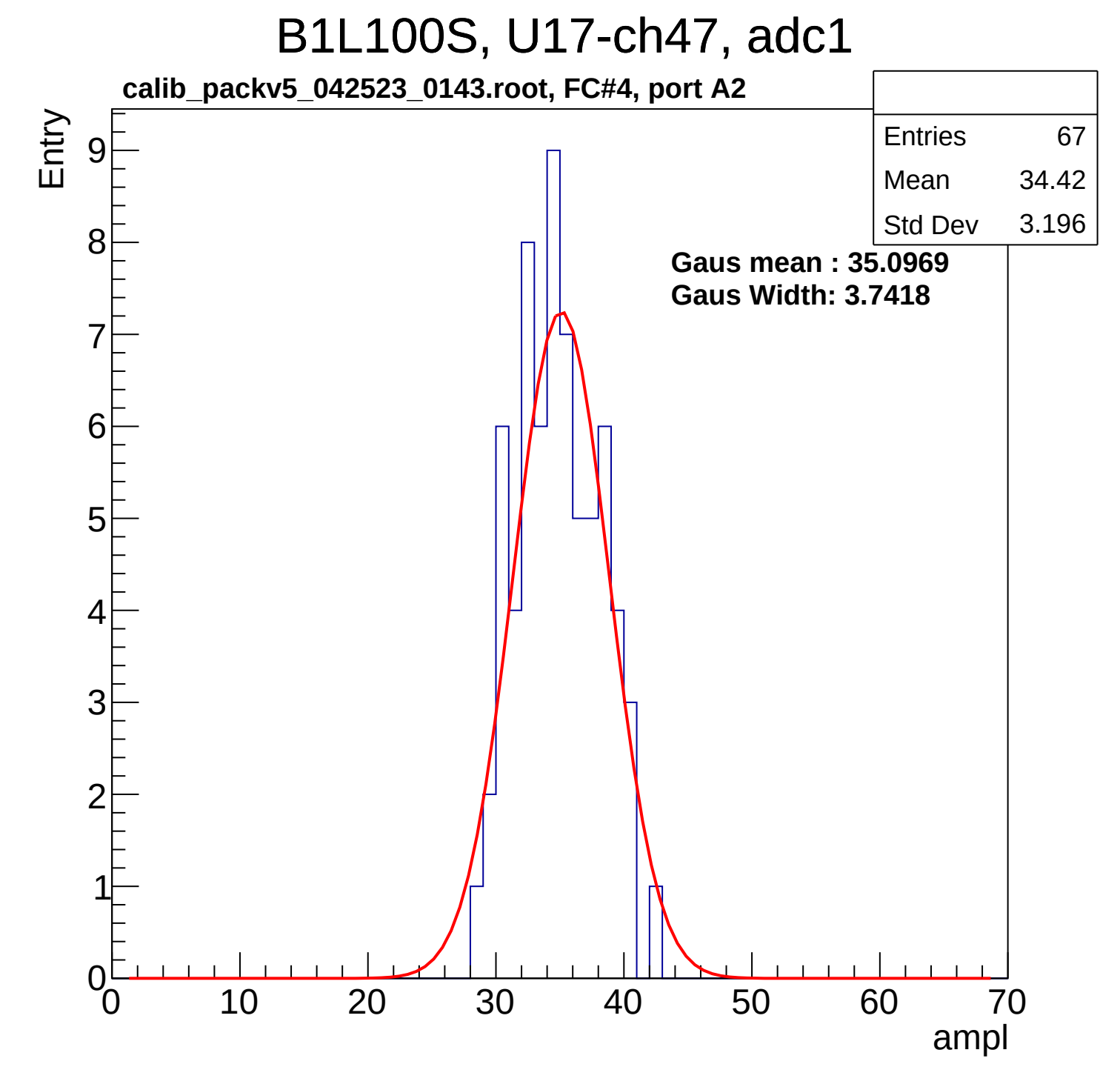

B1L100S, U17-ch46, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 31.5
Std Dev 31.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch47, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 26.98
Std Dev 6.02
Gaus mean : 28.2632
Gaus Width: 3.3921
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U17-ch47, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 34.42
Std Dev 3.196
Gaus mean : 35.0969
Gaus Width: 3.7418
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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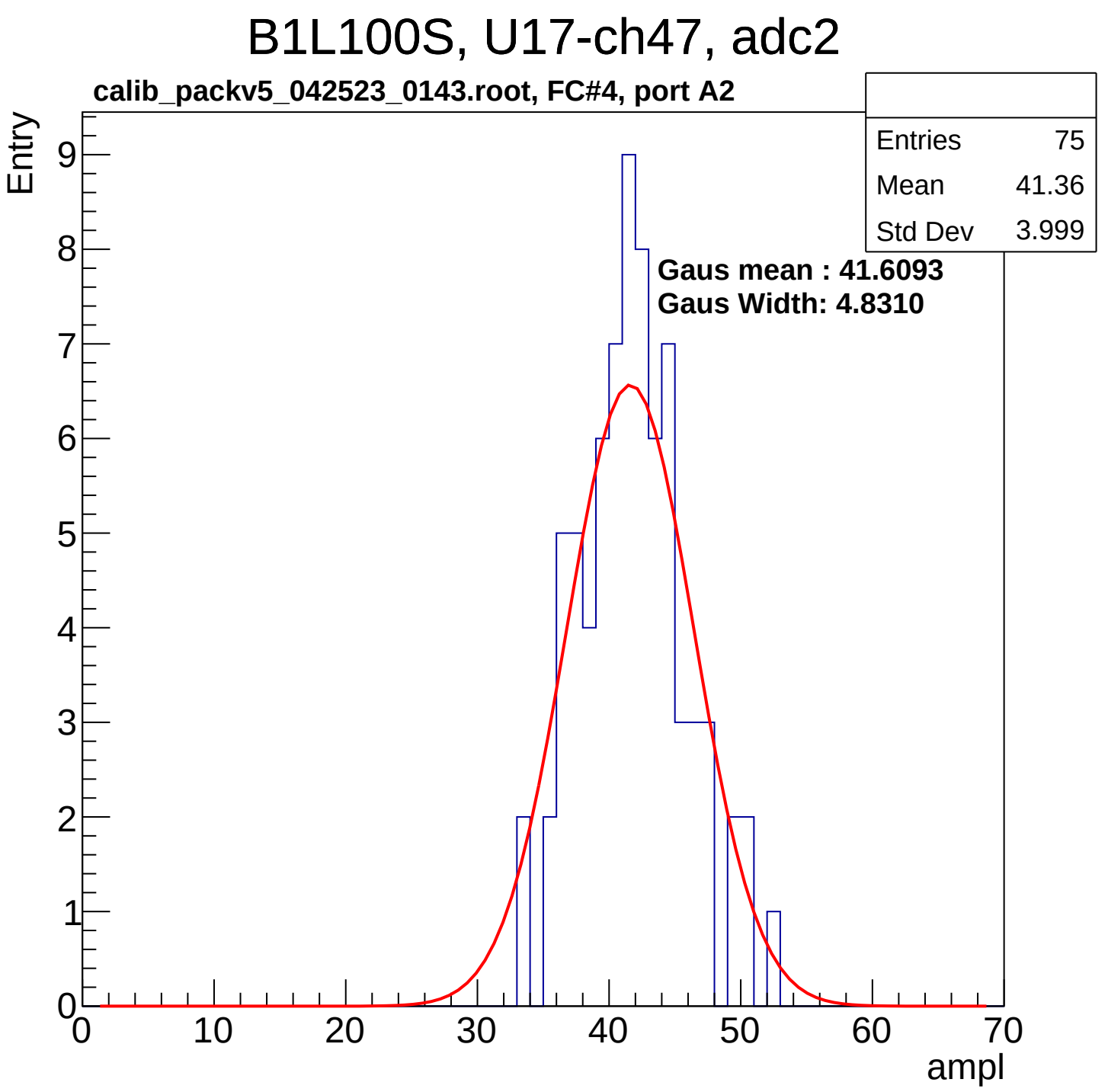
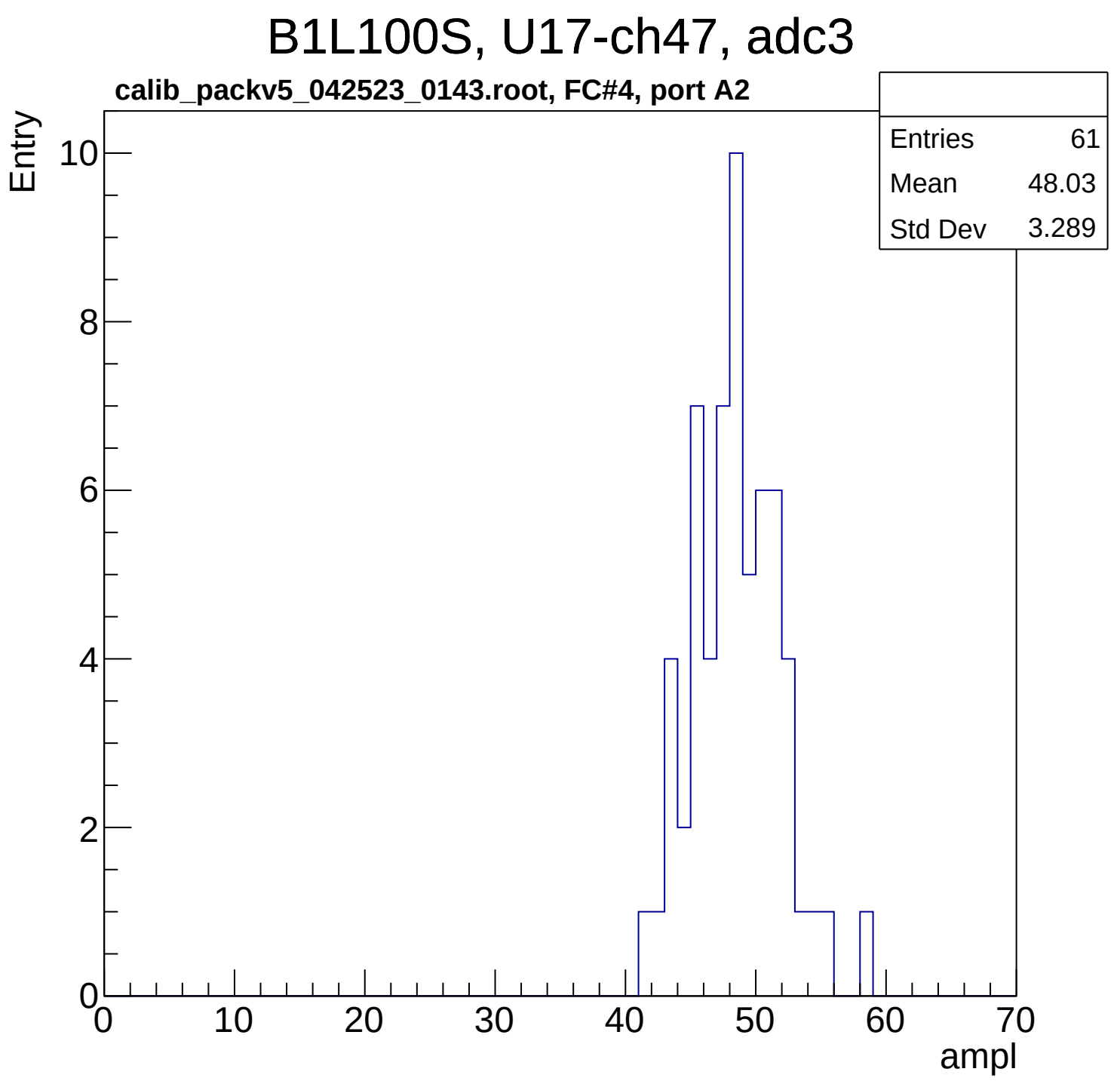
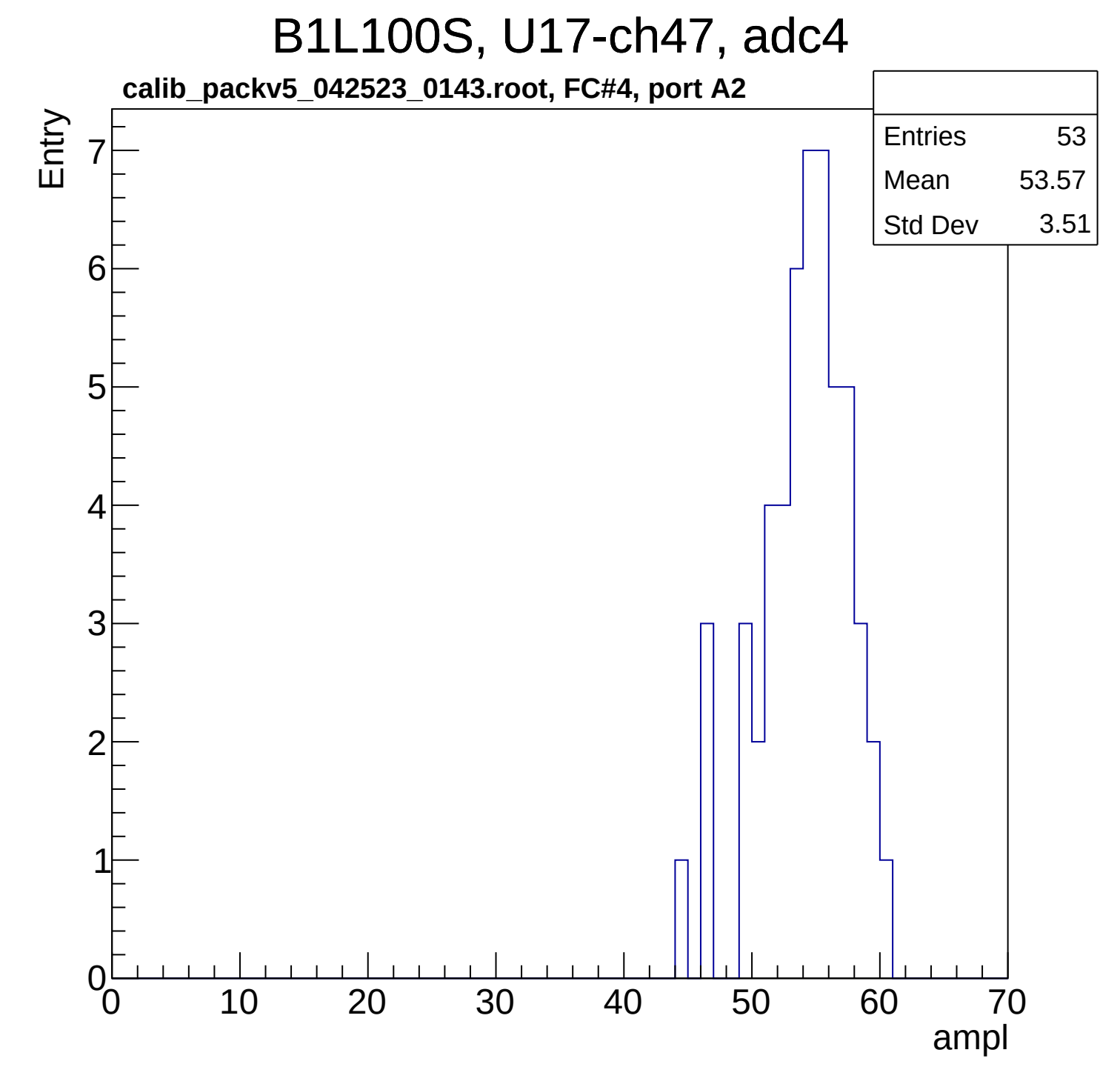
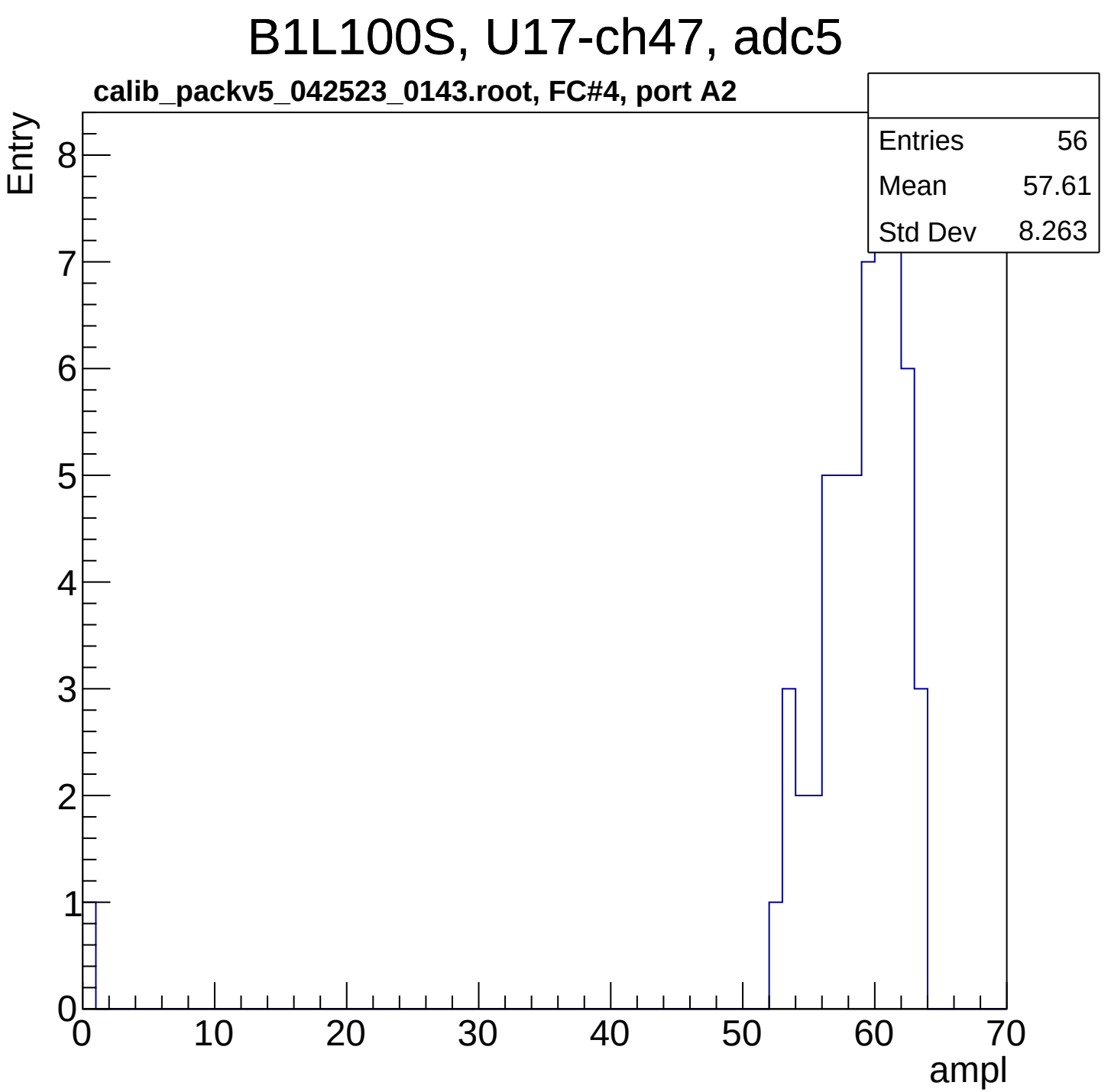
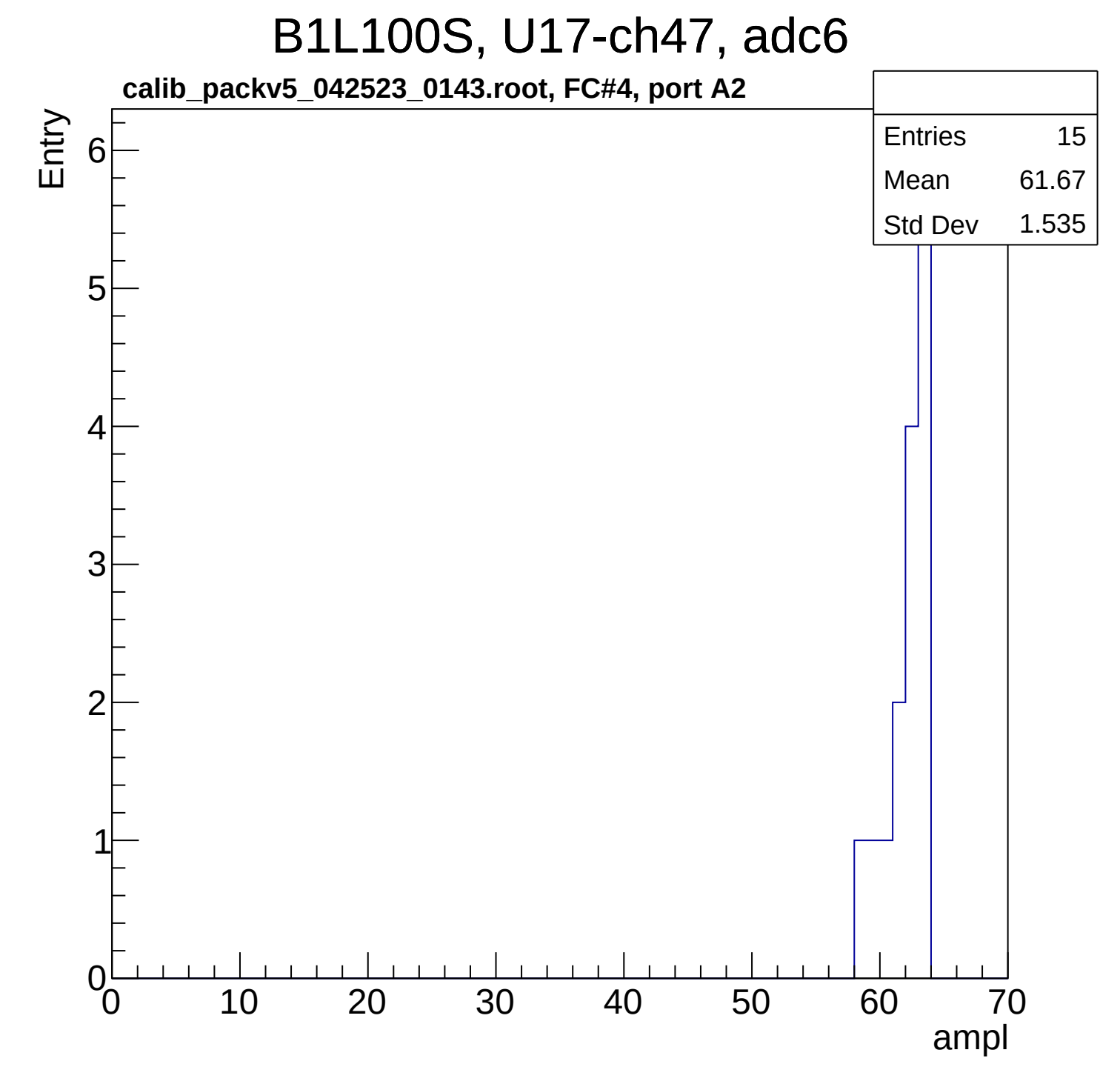
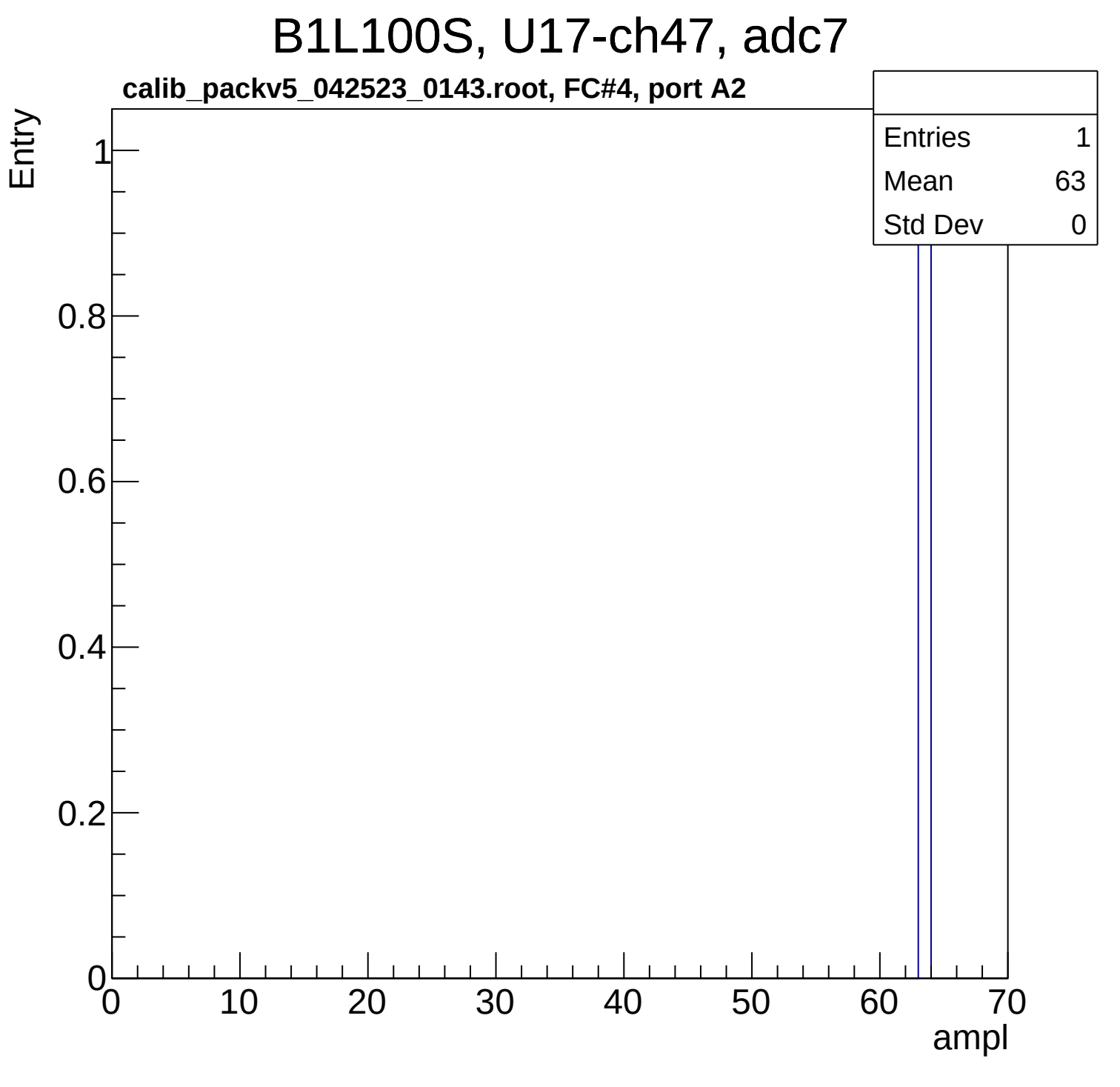

B1L100S, U17-ch47, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 75
Mean 41.36
Std Dev 3.999
Gaus mean : 41.6093
Gaus Width: 4.8310
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

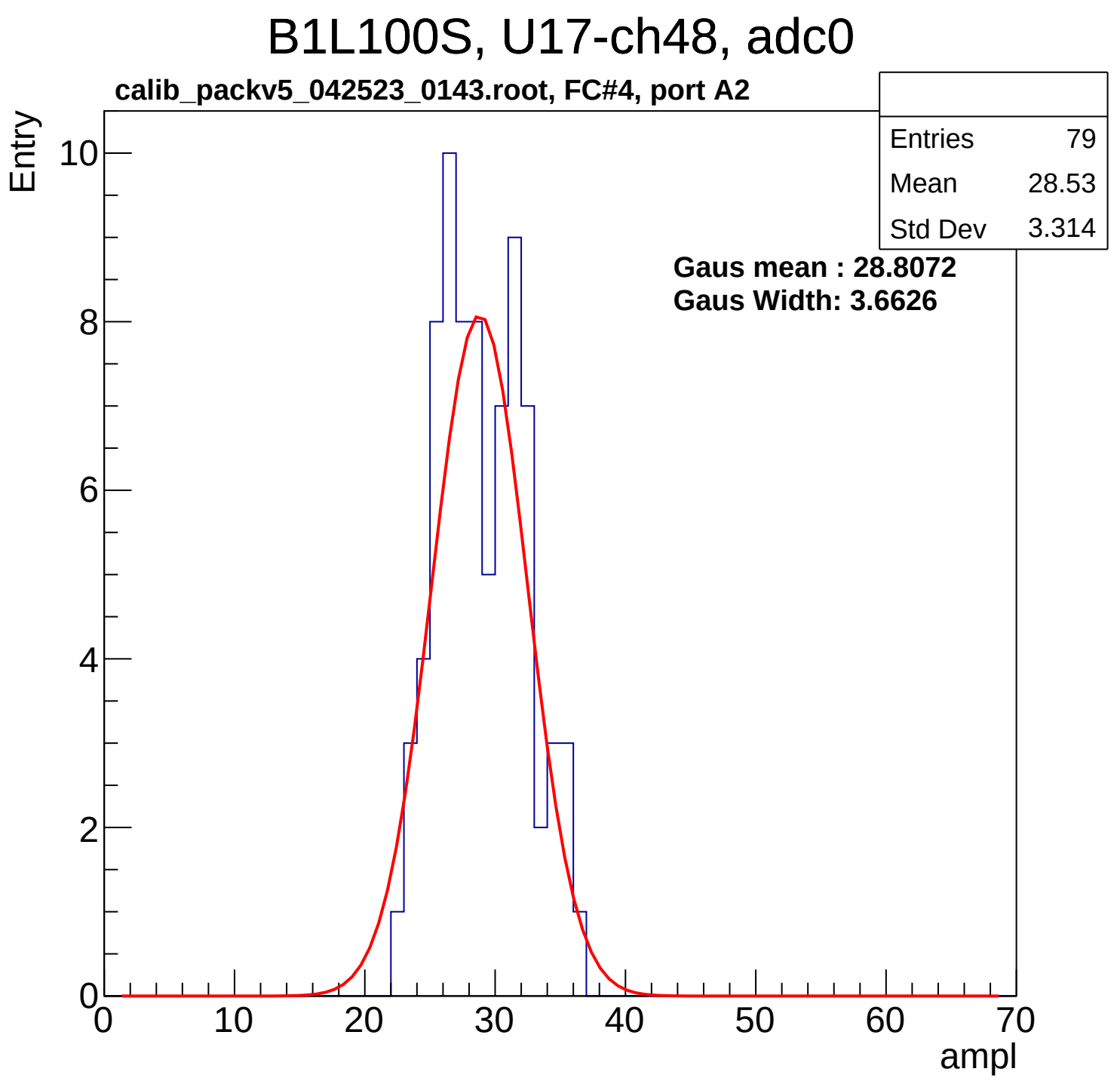

B1L100S, U17-ch47, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 48.03
Std Dev 3.289
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

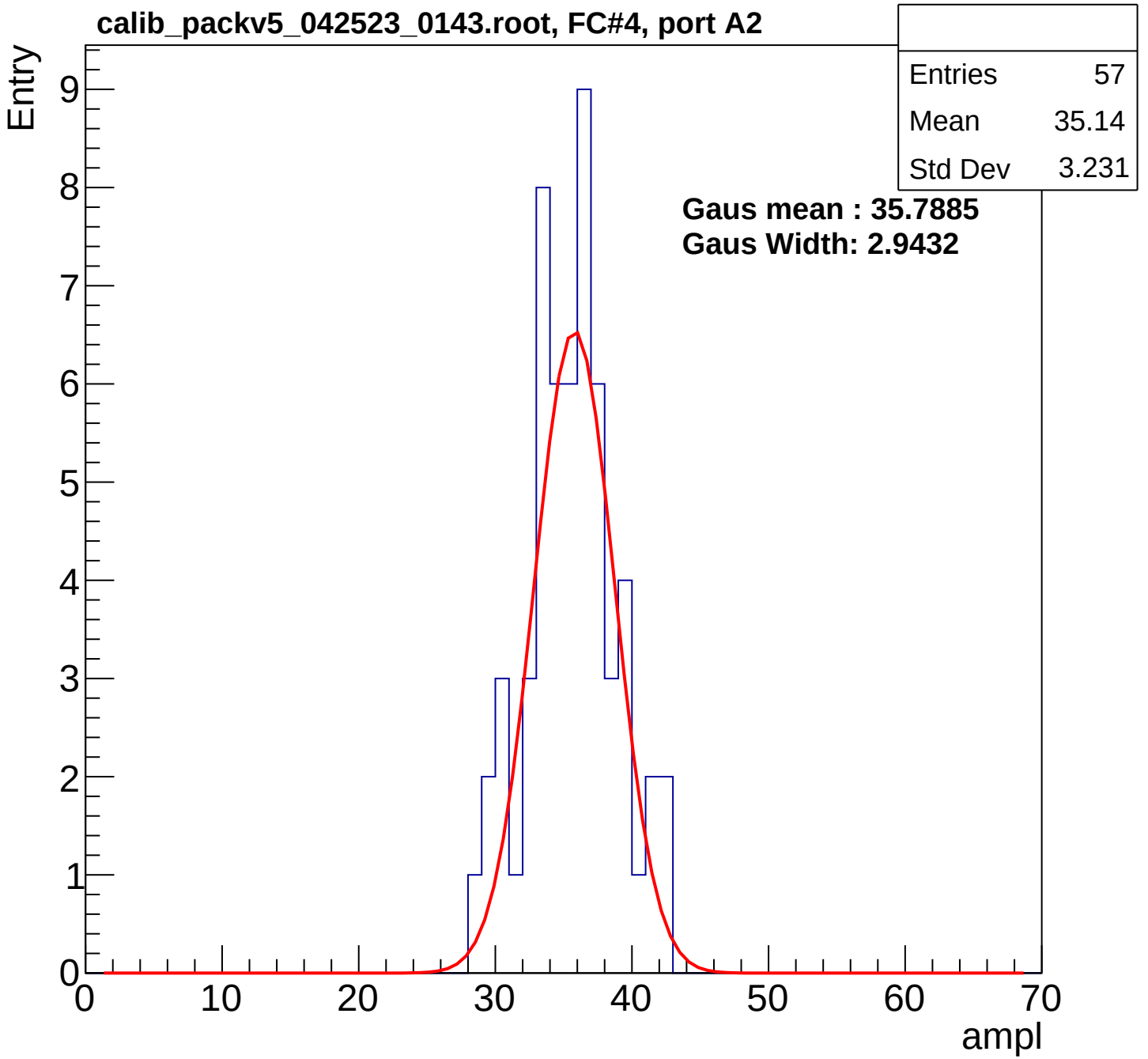

B1L100S, U17-ch47, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 53.57
Std Dev 3.51
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

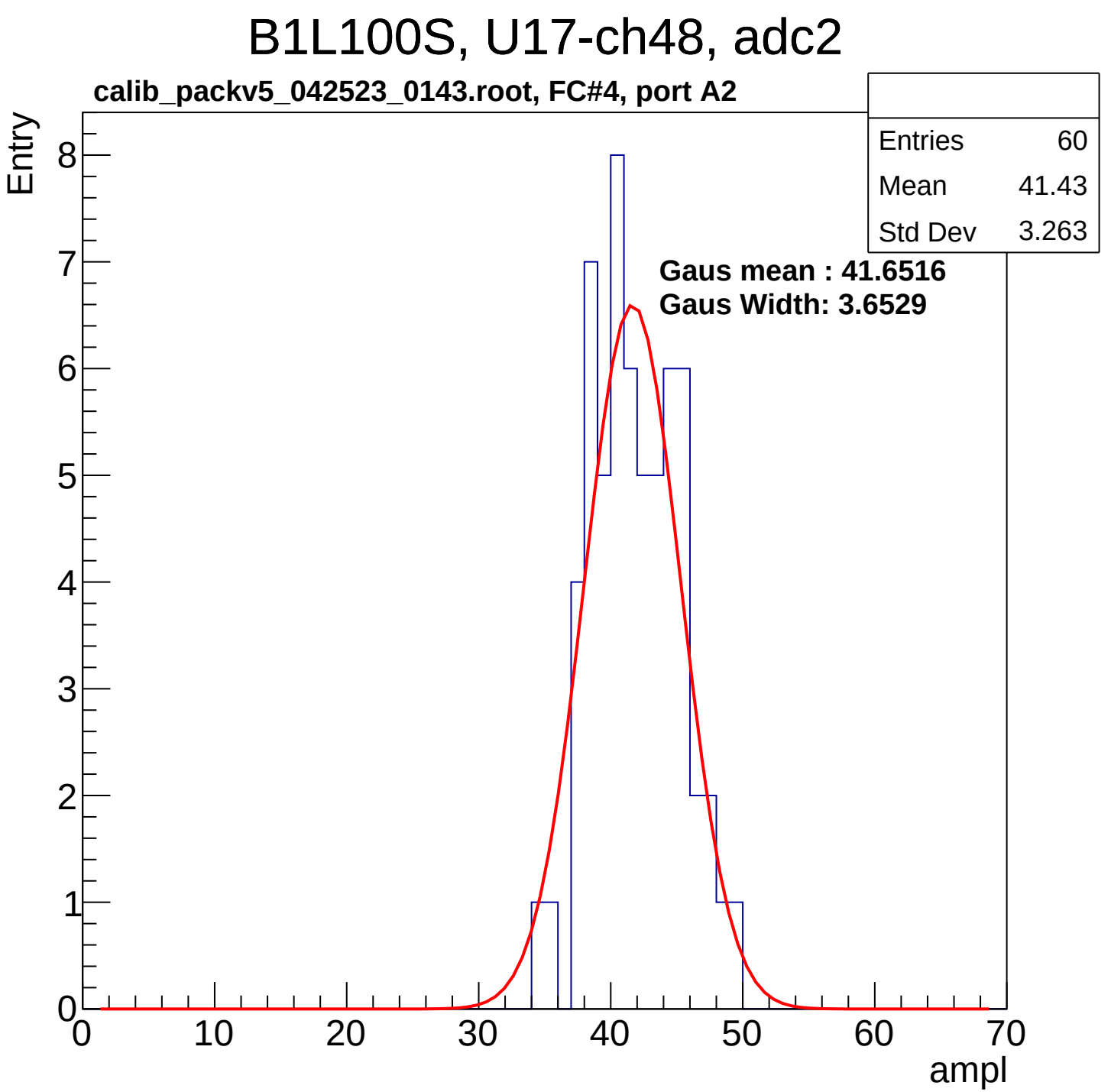

B1L100S, U17-ch47, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 57.61
Std Dev 8.263
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

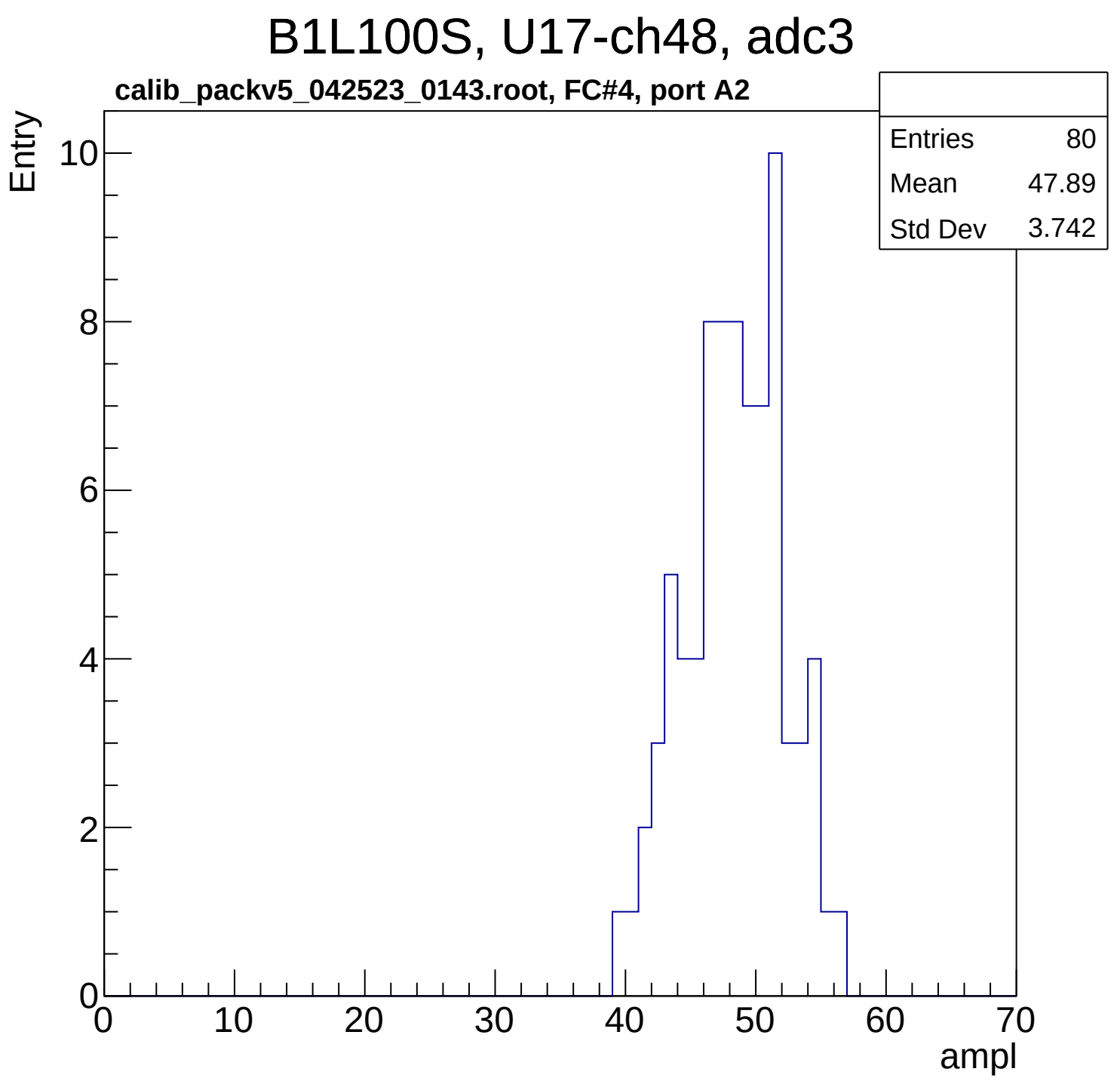

B1L100S, U17-ch47, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 15
Mean 61.67
Std Dev 1.535
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

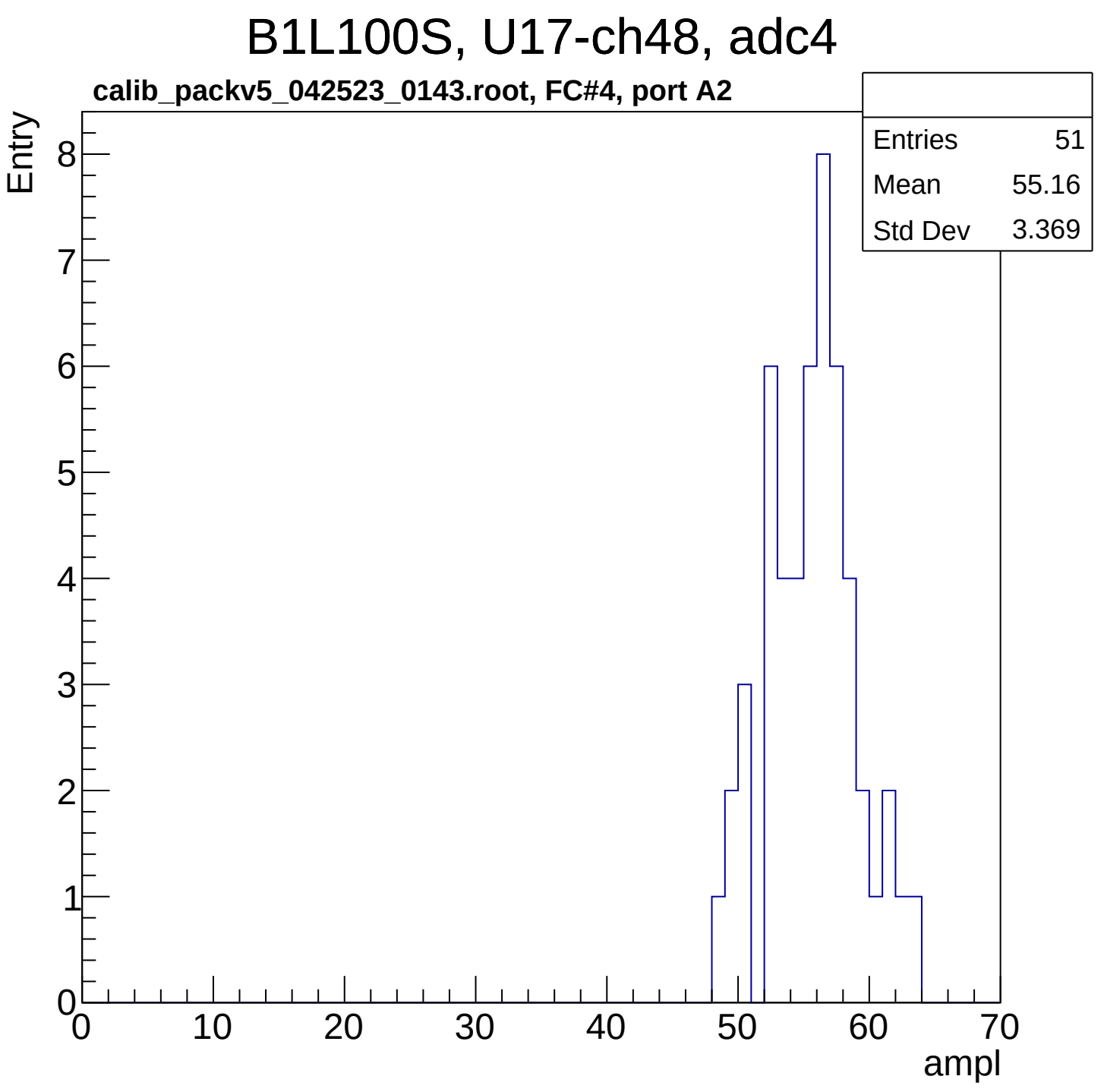

B1L100S, U17-ch47, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch48, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 79
Mean 28.53
Std Dev 3.314
Gaus mean : 28.8072
Gaus Width: 3.6626
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U17-ch48, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 35.14
Std Dev 3.231
Gaus mean : 35.7885
Gaus Width: 2.9432
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L100S, U17-ch48, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 41.43
Std Dev 3.263
Gaus mean : 41.6516
Gaus Width: 3.6529
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch48, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 80
Mean 47.89
Std Dev 3.742
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U17-ch48, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 55.16
Std Dev 3.369
Entry
ampl
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1
2
3
4
5
6
7
8
0
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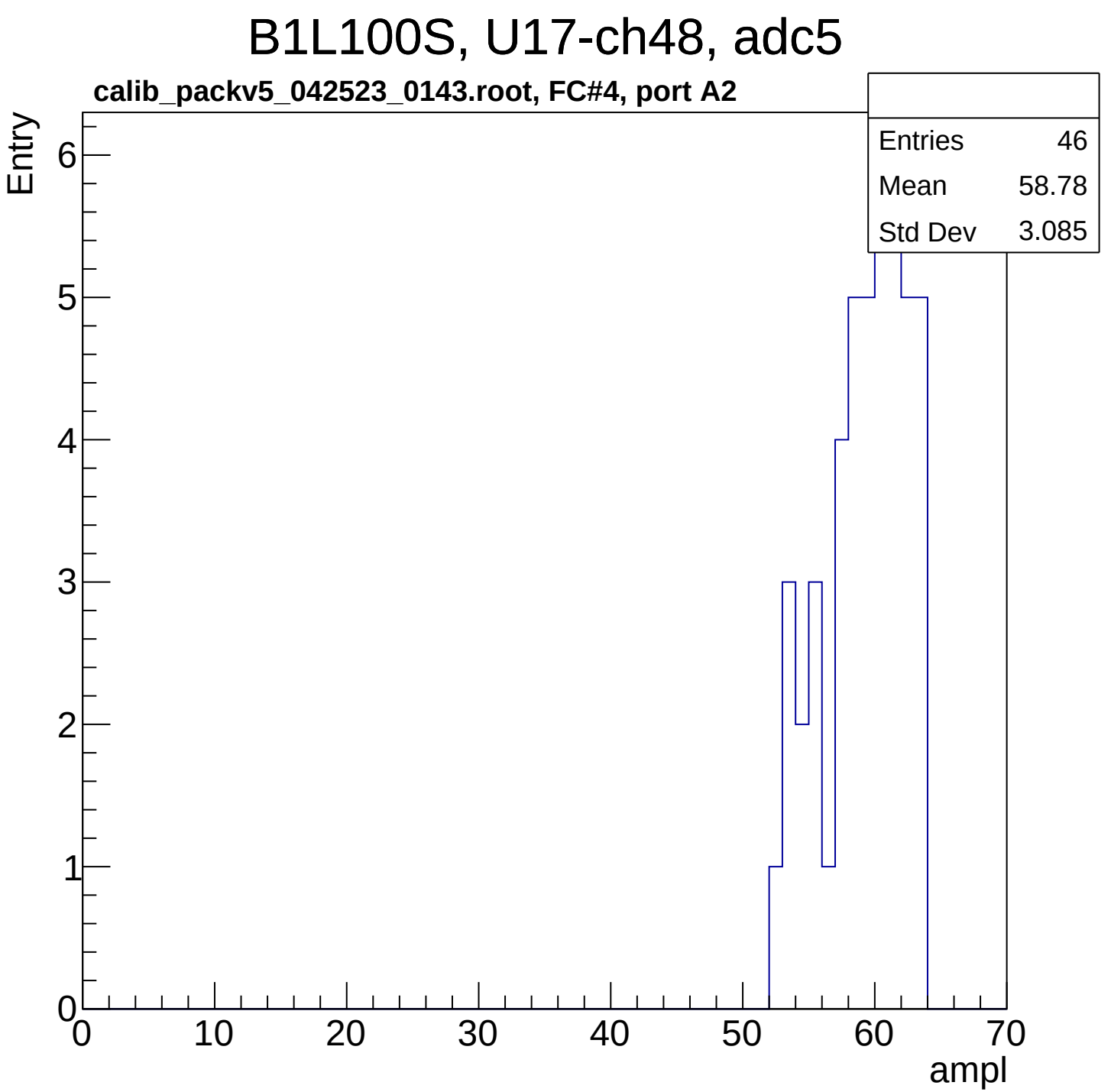
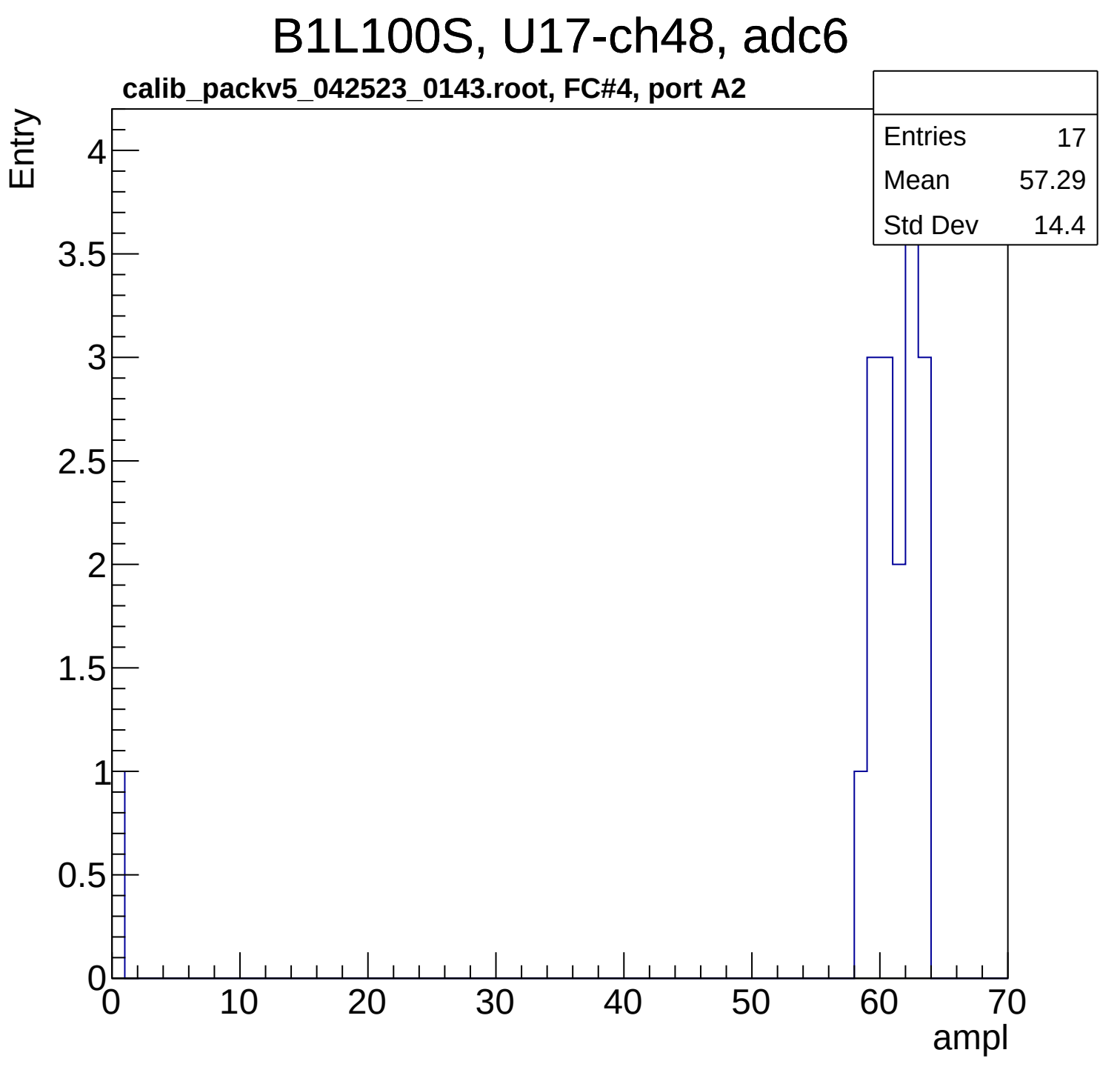
20
30
40
50
60
70


B1L100S, U17-ch48, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 46
Mean 58.78
Std Dev 3.085
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch48, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 17
Mean 57.29
Std Dev 14.4
Entry
ampl
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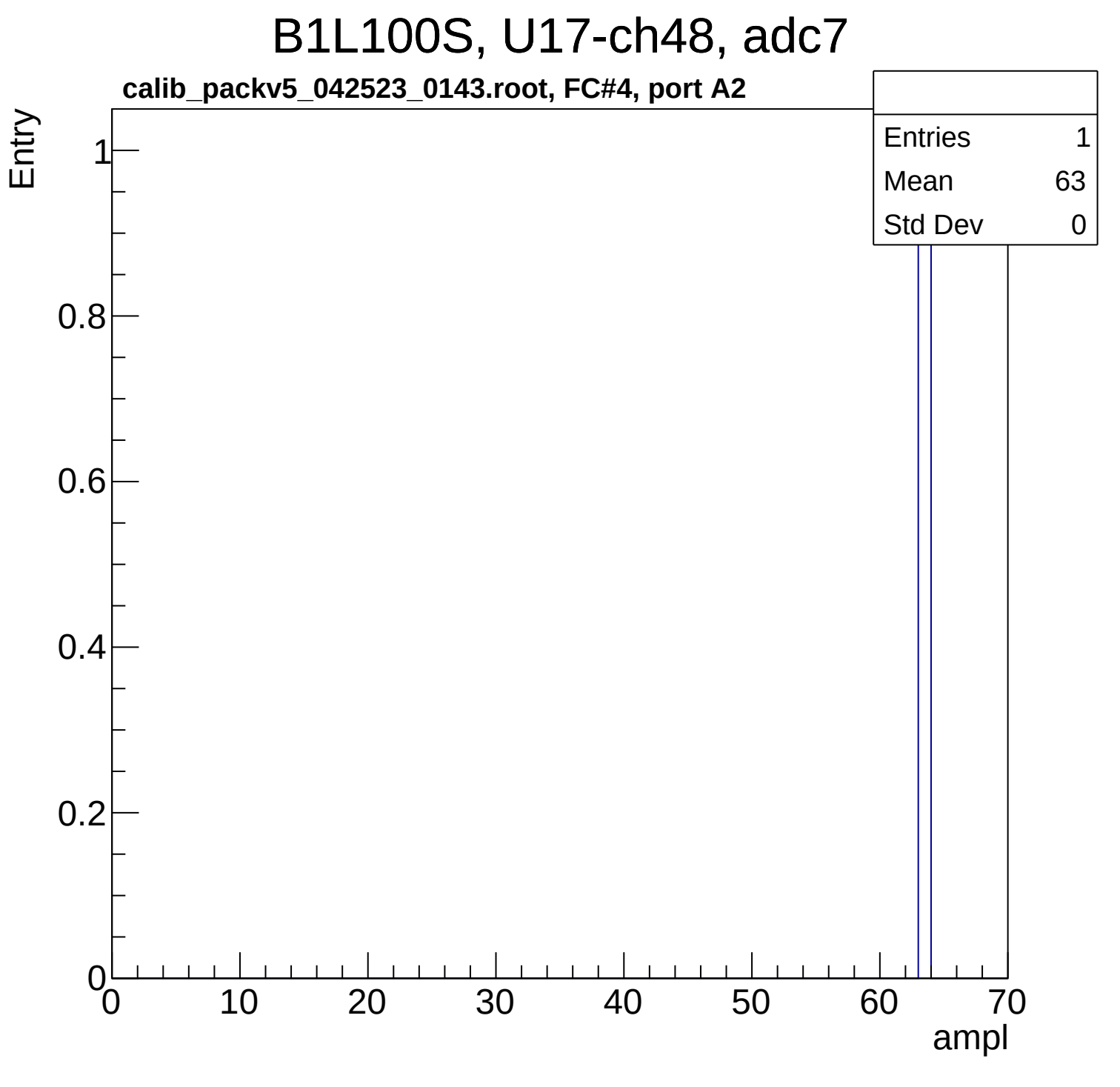
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L100S, U17-ch48, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 63
Std Dev 0
Entry
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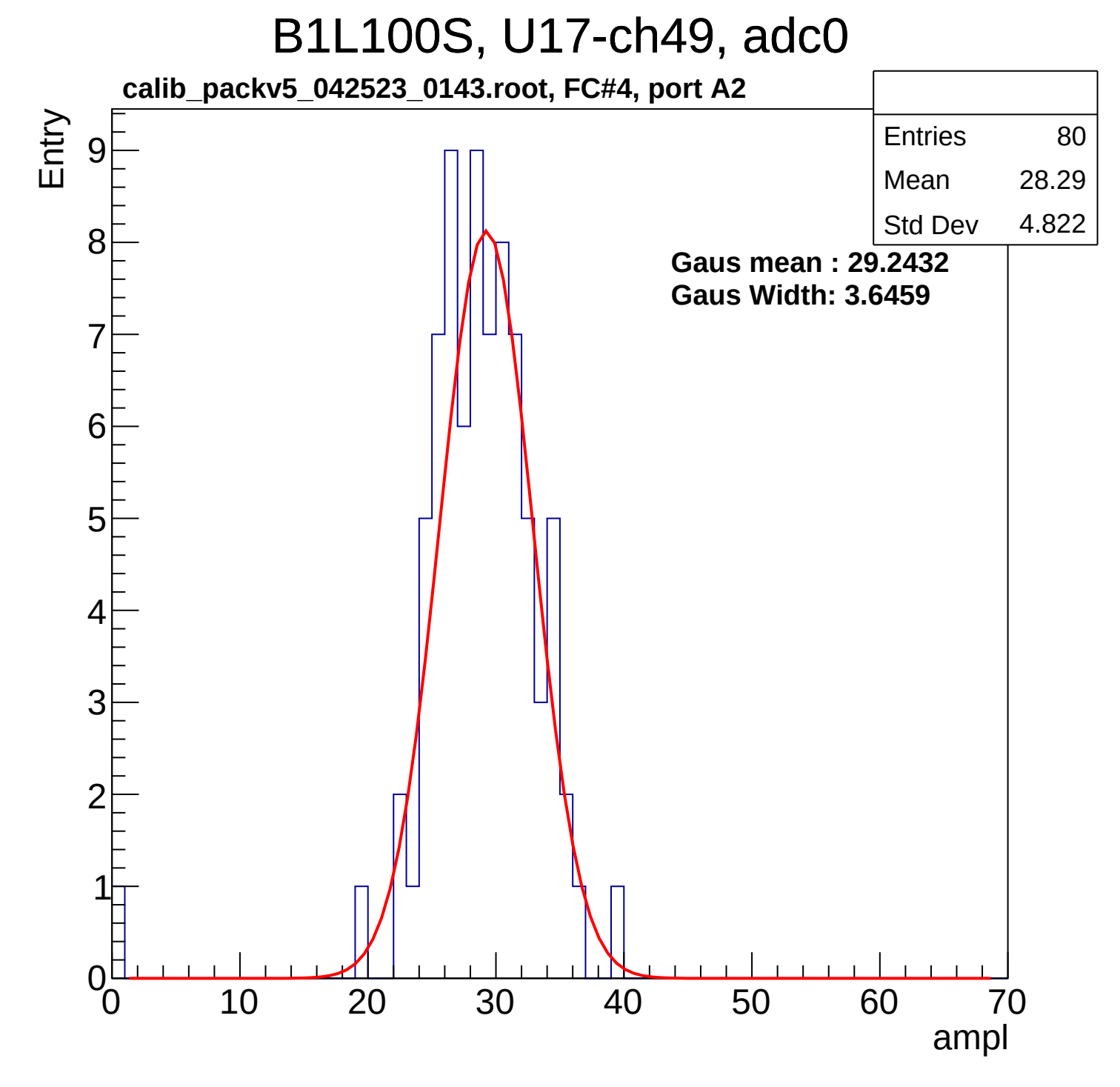
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch49, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 80
Mean 28.29
Std Dev 4.822
Gaus mean : 29.2432
Gaus Width: 3.6459
Entry
ampl
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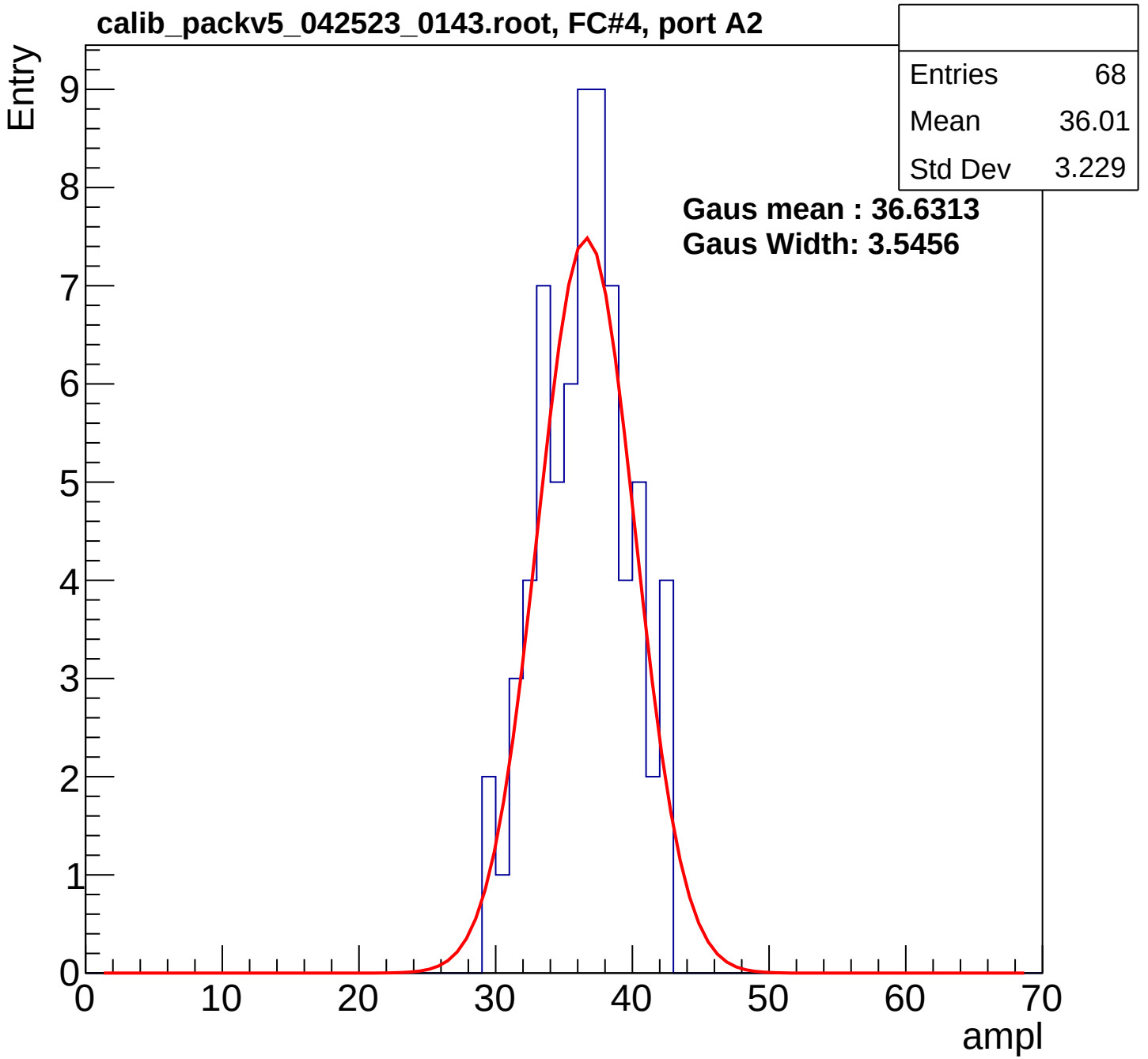
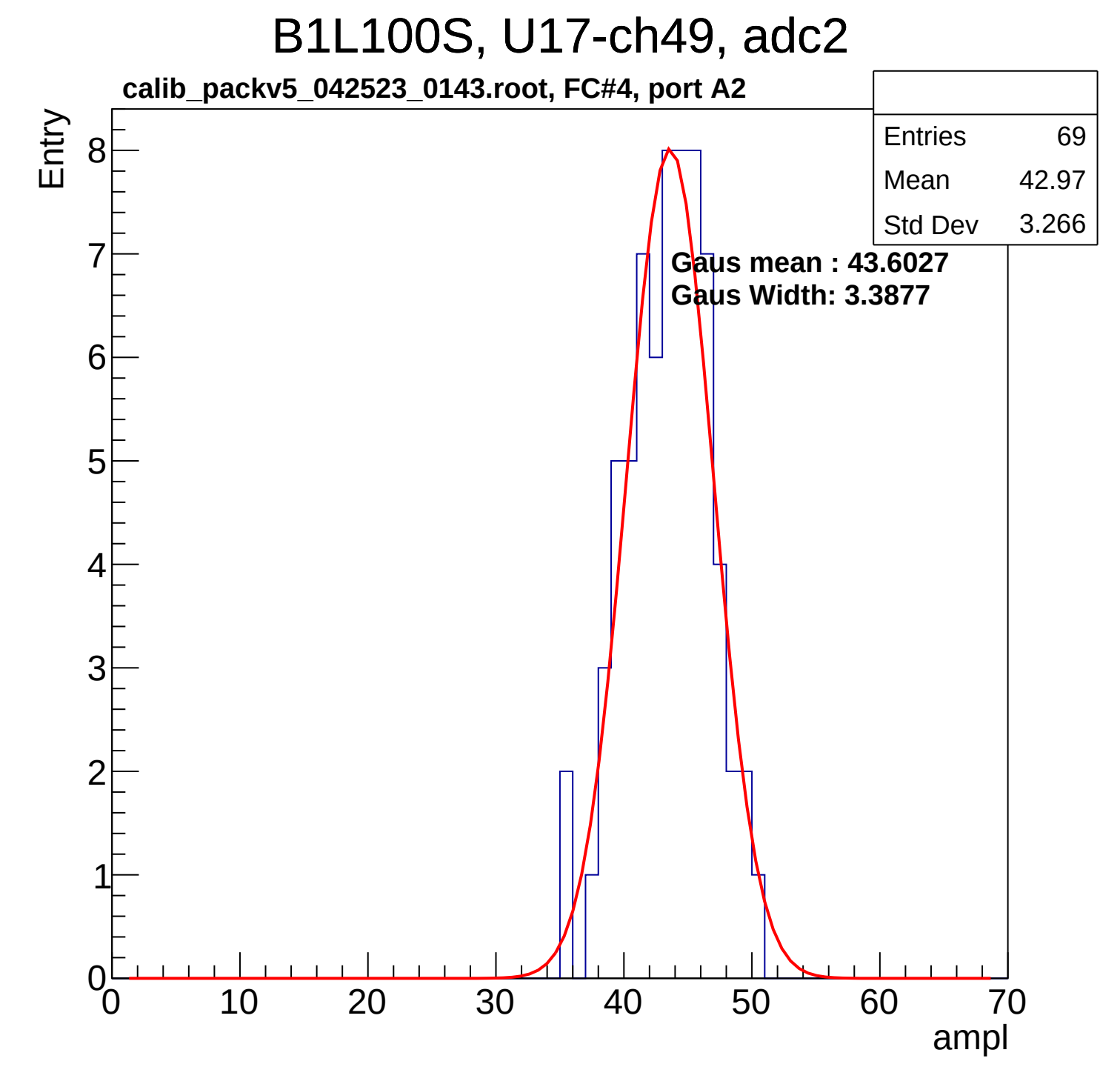
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch49, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 36.01
Std Dev 3.229
Gaus mean : 36.6313
Gaus Width: 3.5456
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch49, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 42.97
Std Dev 3.266
Gaus mean : 43.6027
Gaus Width: 3.3877
Entry
ampl
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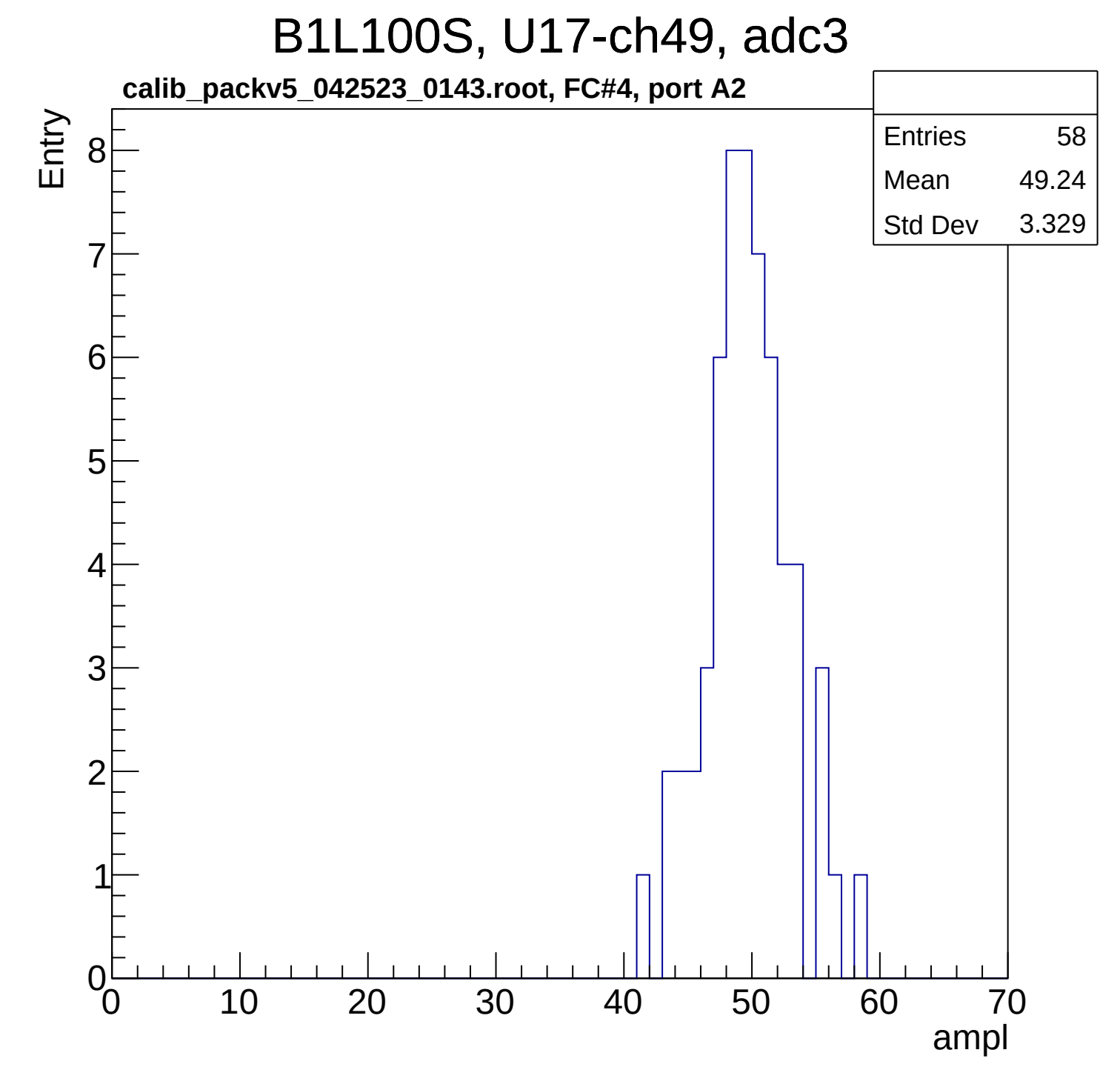
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch49, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 49.24
Std Dev 3.329
Entry
ampl
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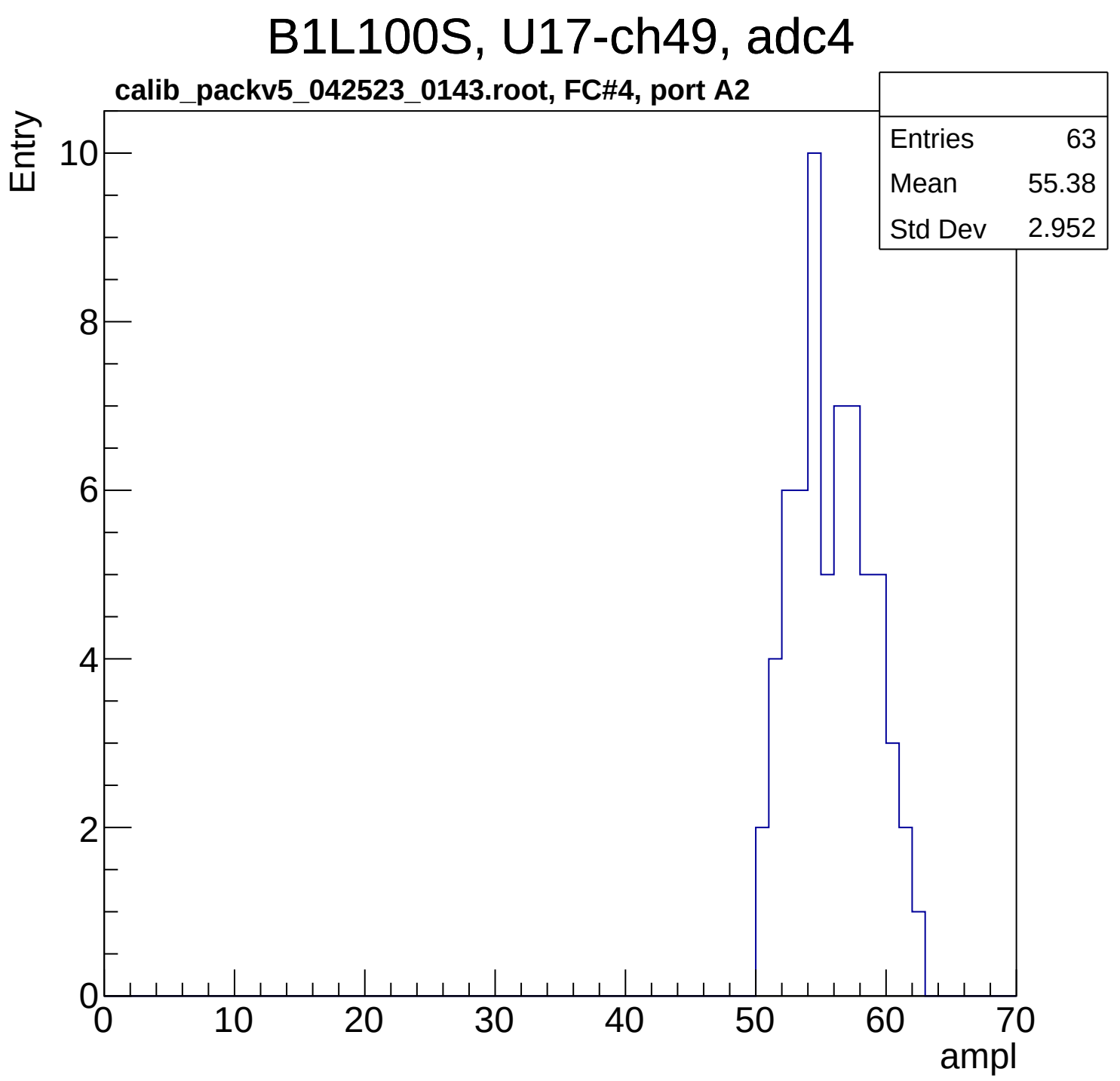
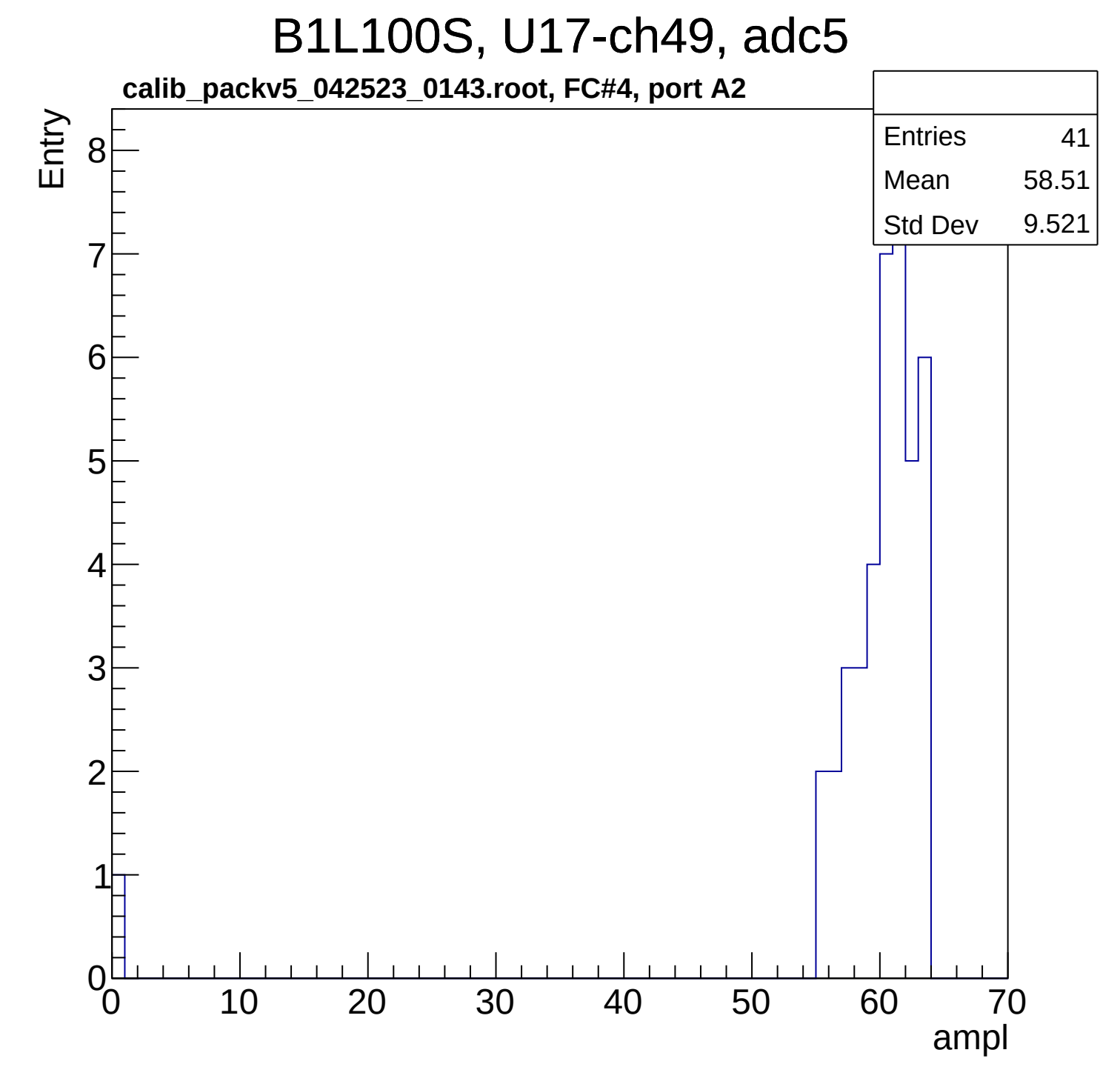
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch49, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 55.38
Std Dev 2.952
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch49, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 41
Mean 58.51
Std Dev 9.521
Entry
ampl
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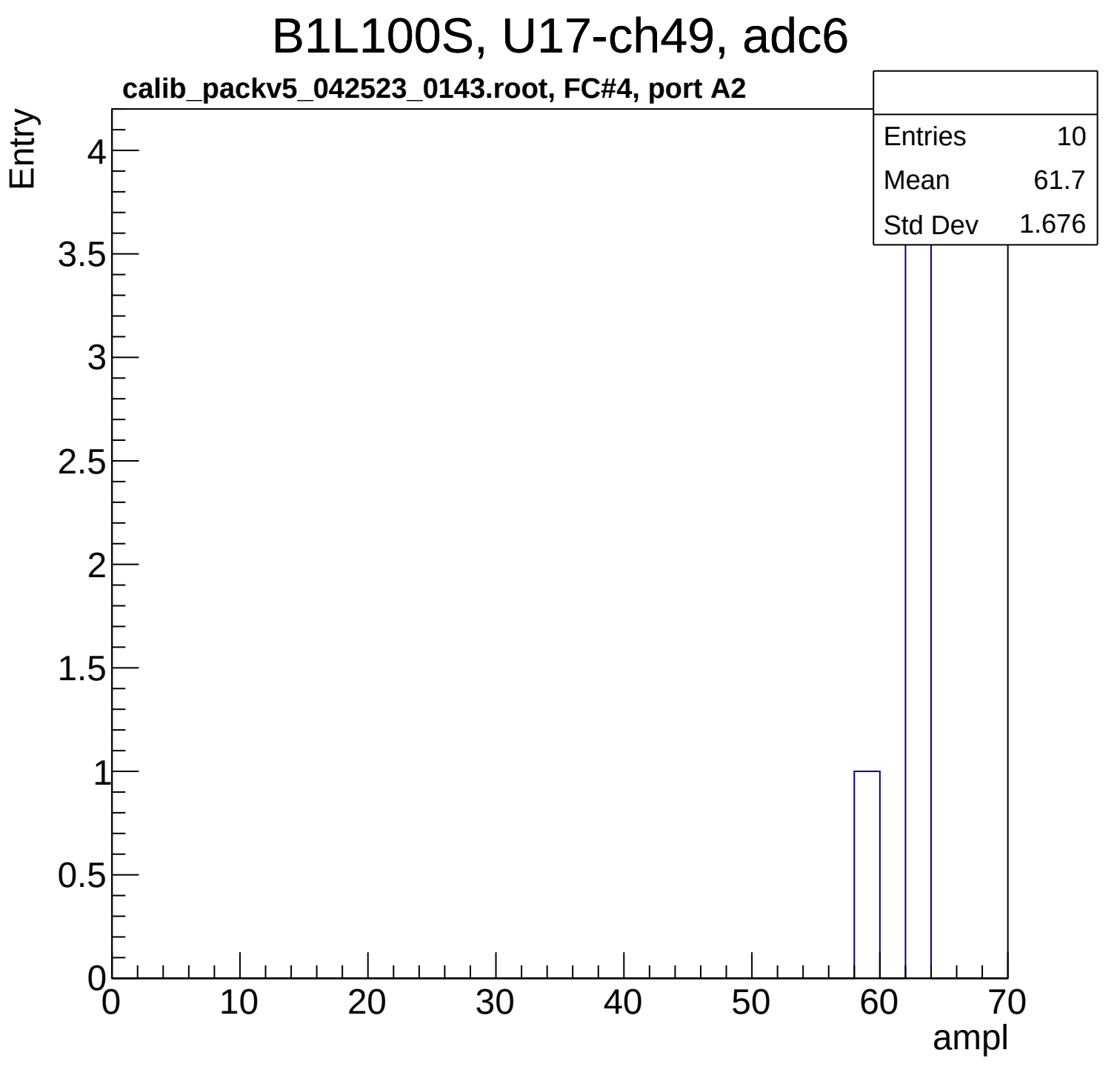
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch49, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 10
Mean 61.7
Std Dev 1.676
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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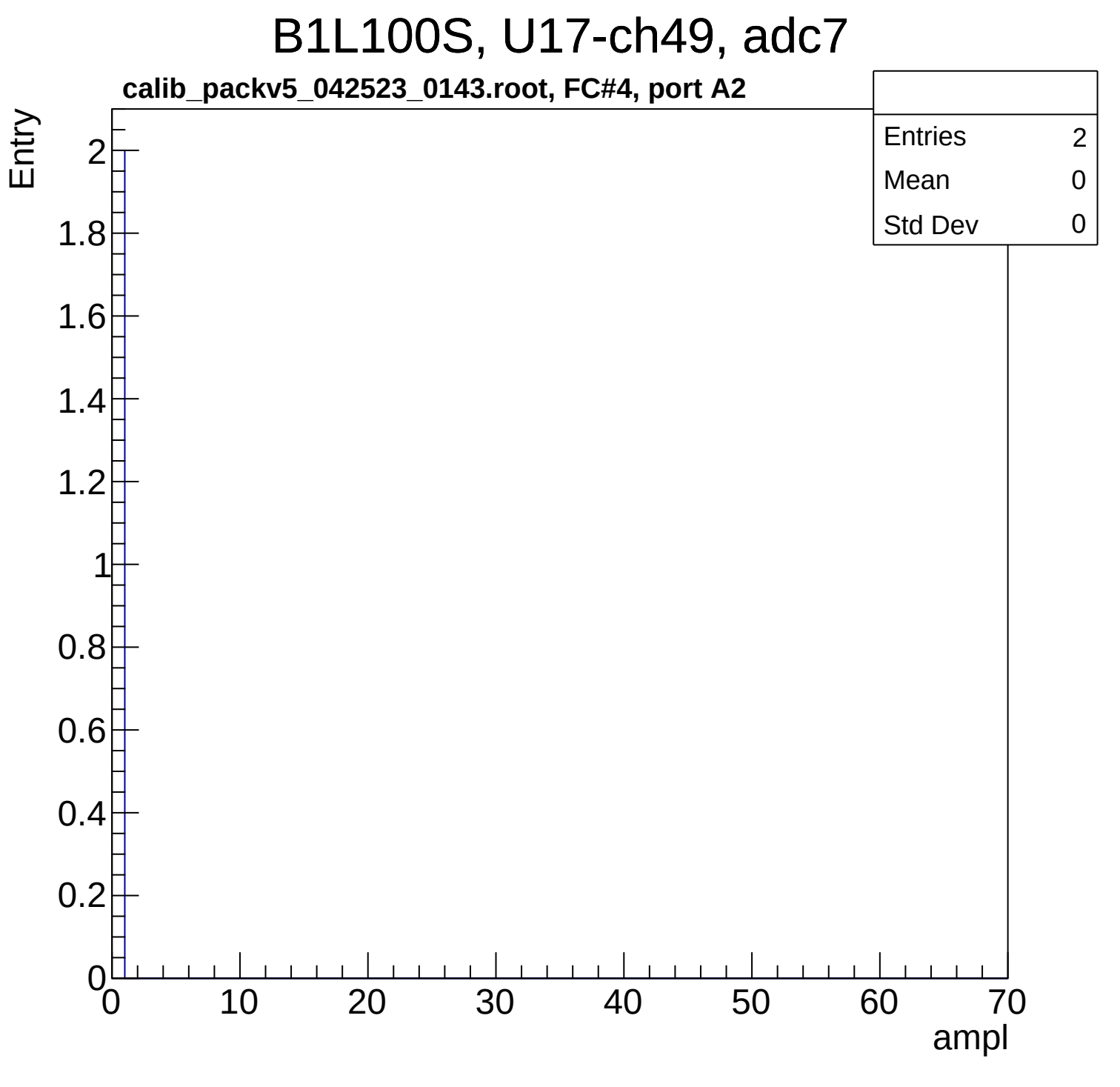
B1L100S, U17-ch49, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
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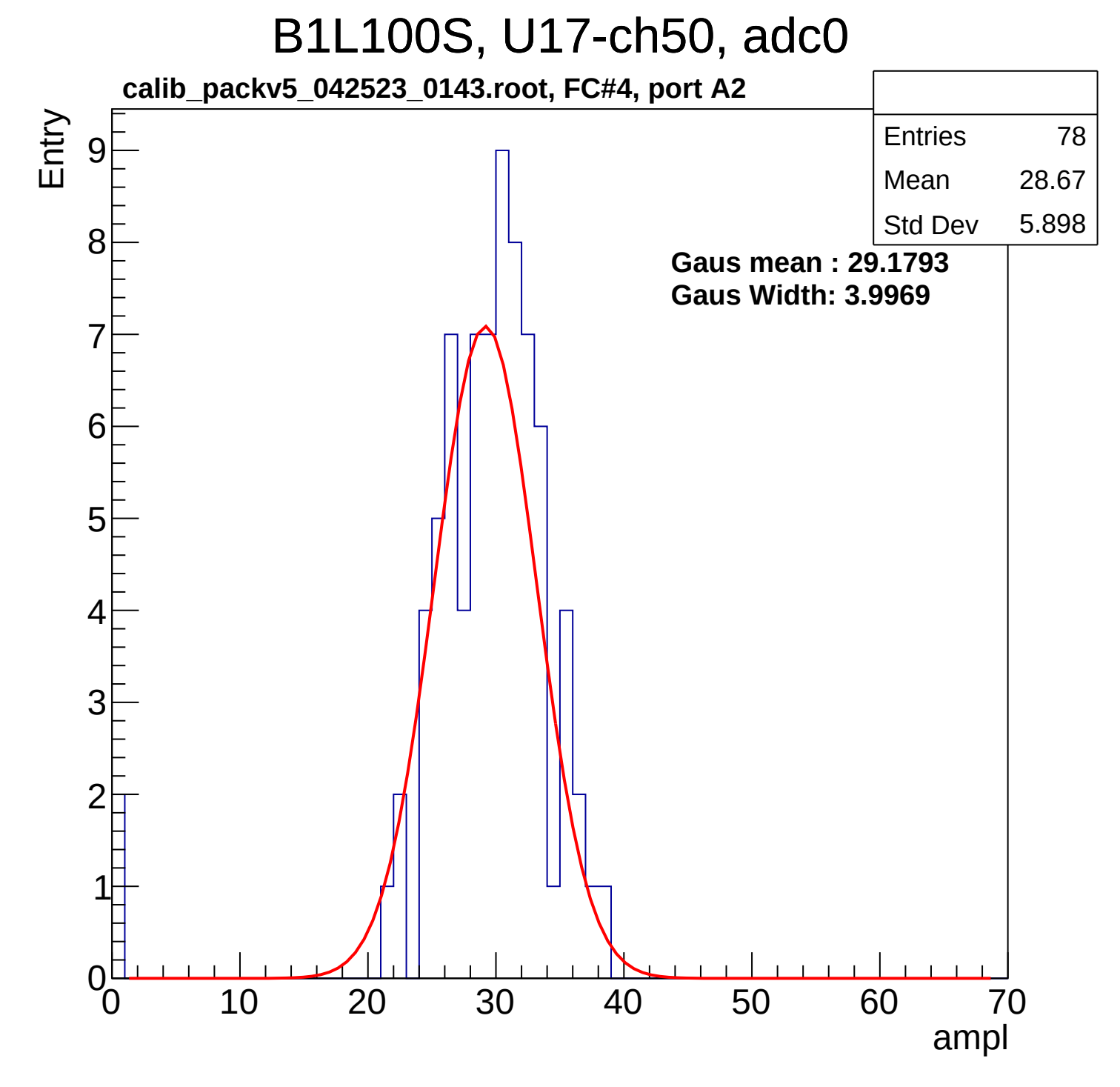
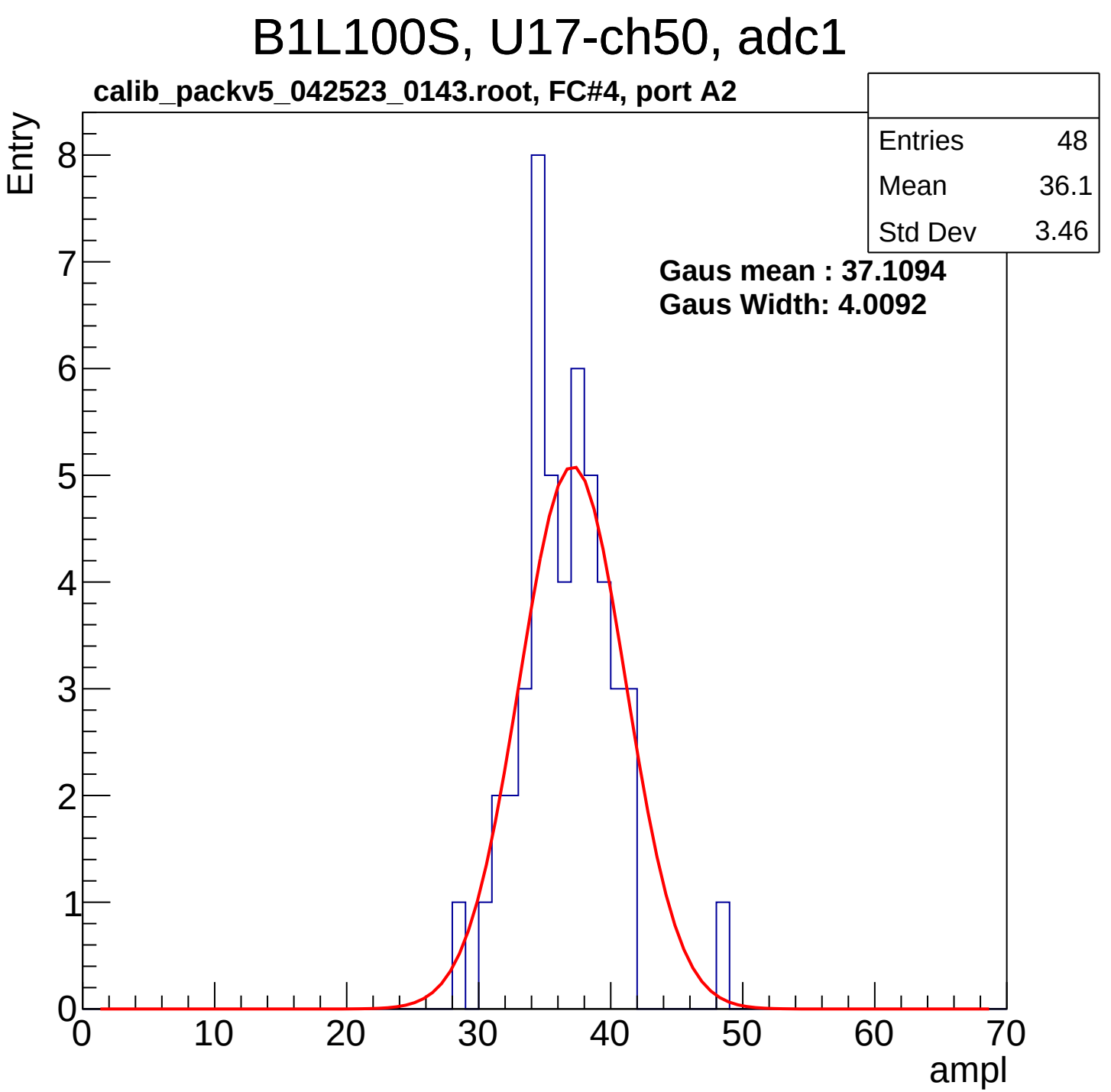
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch50, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 78
Mean 28.67
Std Dev 5.898
Gaus mean : 29.1793
Gaus Width: 3.9969
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch50, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 48
Mean 36.1
Std Dev 3.46
Gaus mean : 37.1094
Gaus Width: 4.0092
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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40
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60
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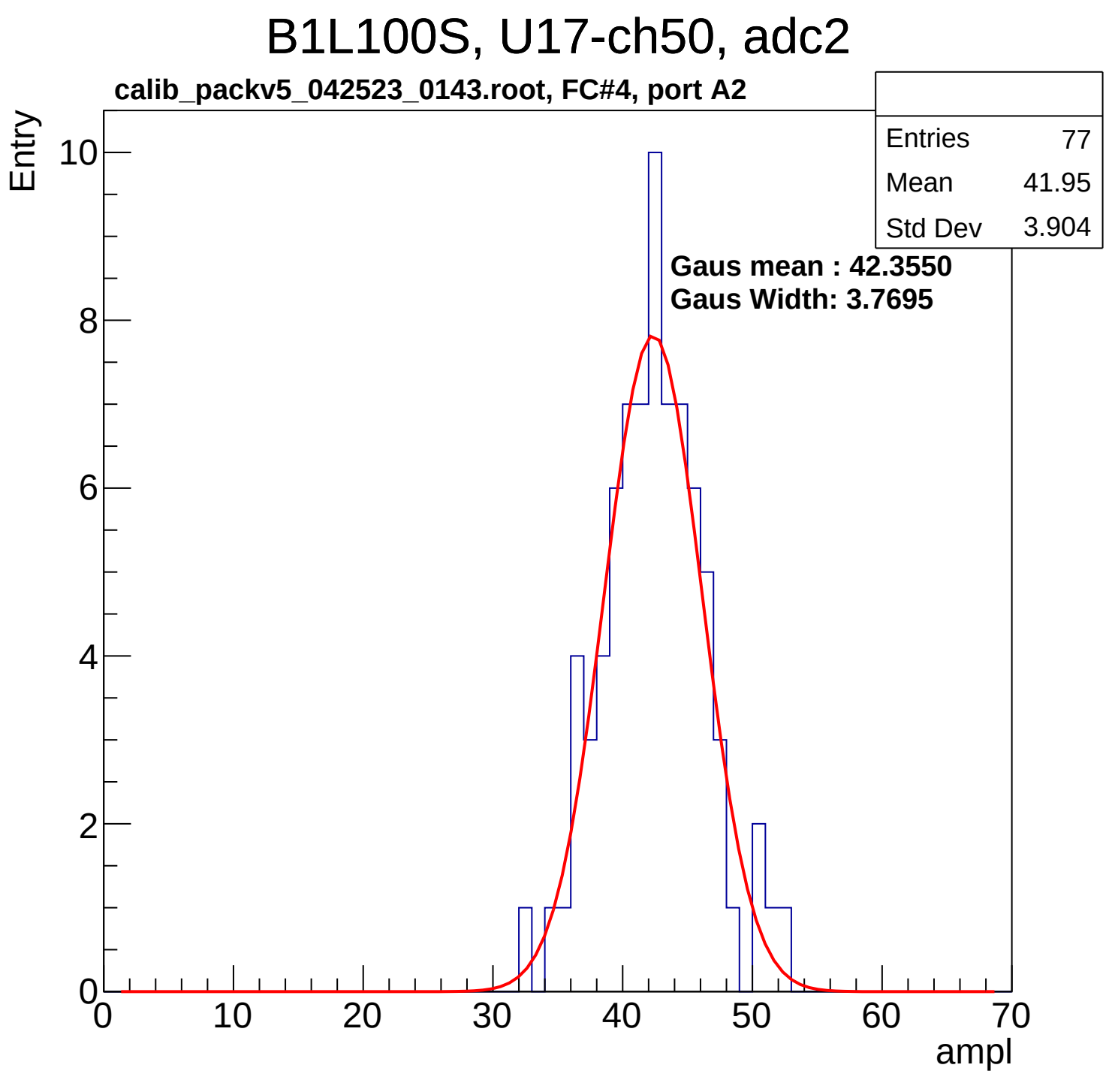
B1L100S, U17-ch50, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 77
Mean 41.95
Std Dev 3.904
Gaus mean : 42.3550
Gaus Width: 3.7695
Entry
ampl
0
2
4
6
8
10
0
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60
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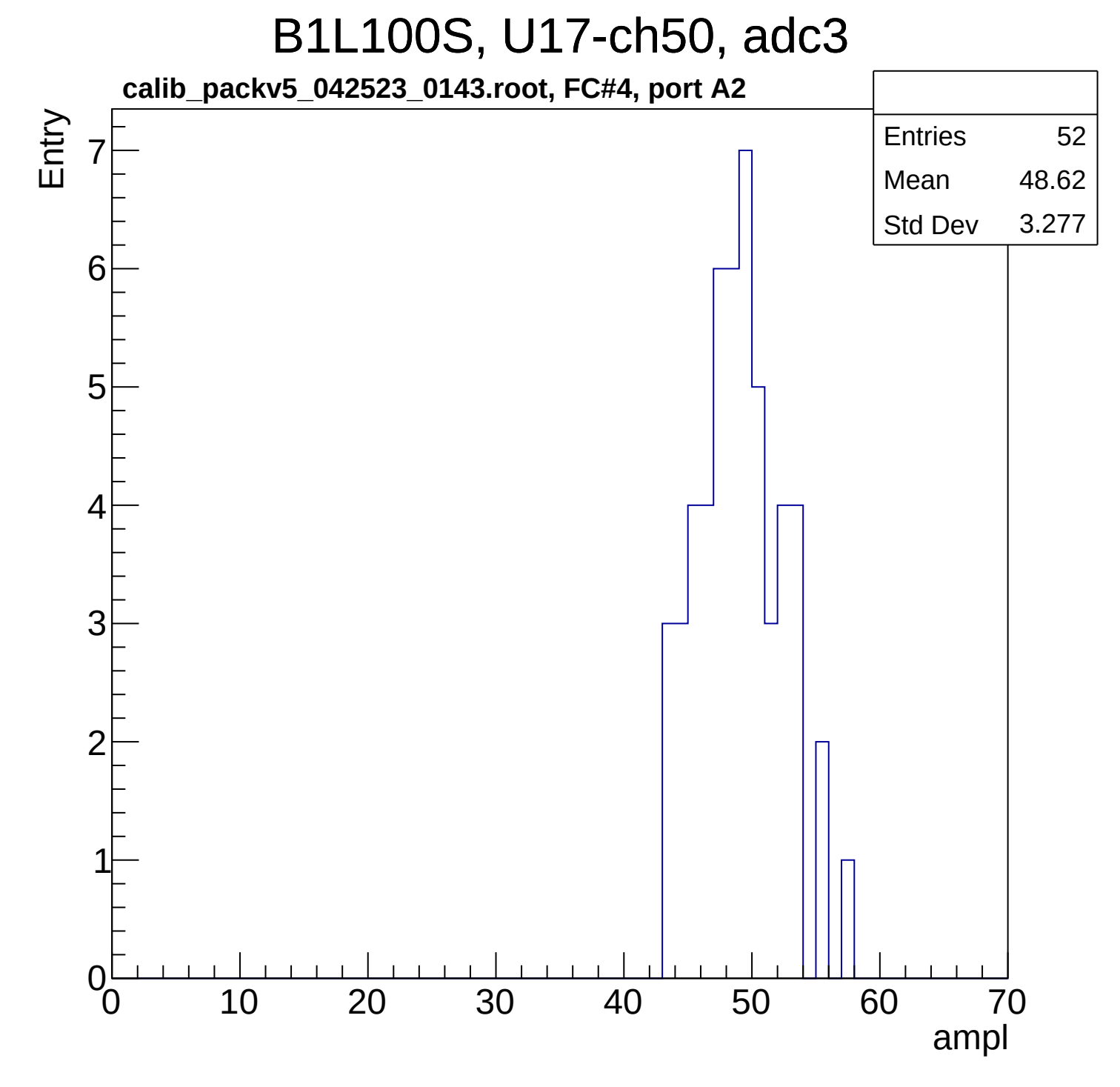
B1L100S, U17-ch50, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 52
Mean 48.62
Std Dev 3.277
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
50
60
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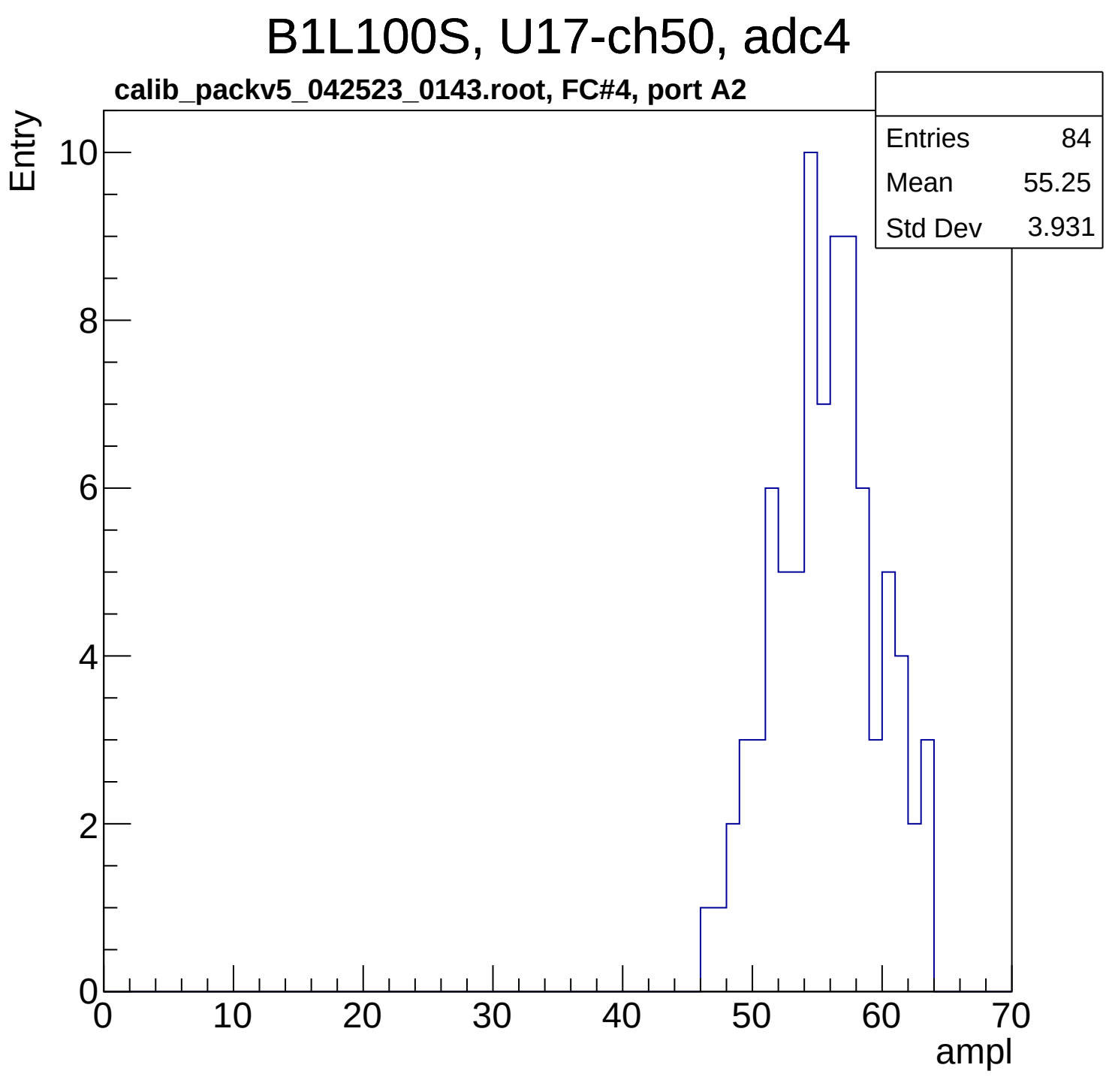
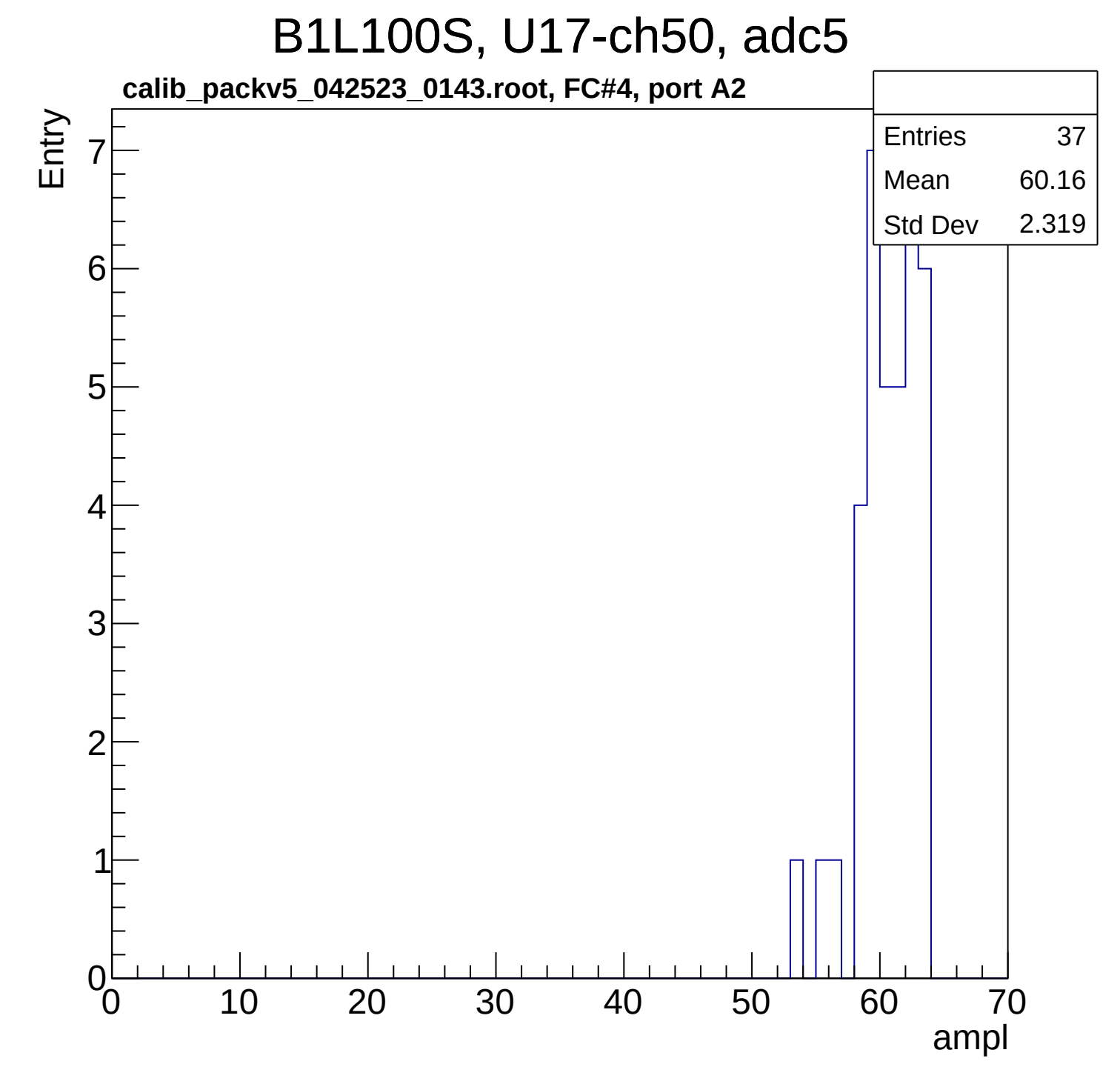

B1L100S, U17-ch50, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 84
Mean 55.25
Std Dev 3.931
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch50, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 37
Mean 60.16
Std Dev 2.319
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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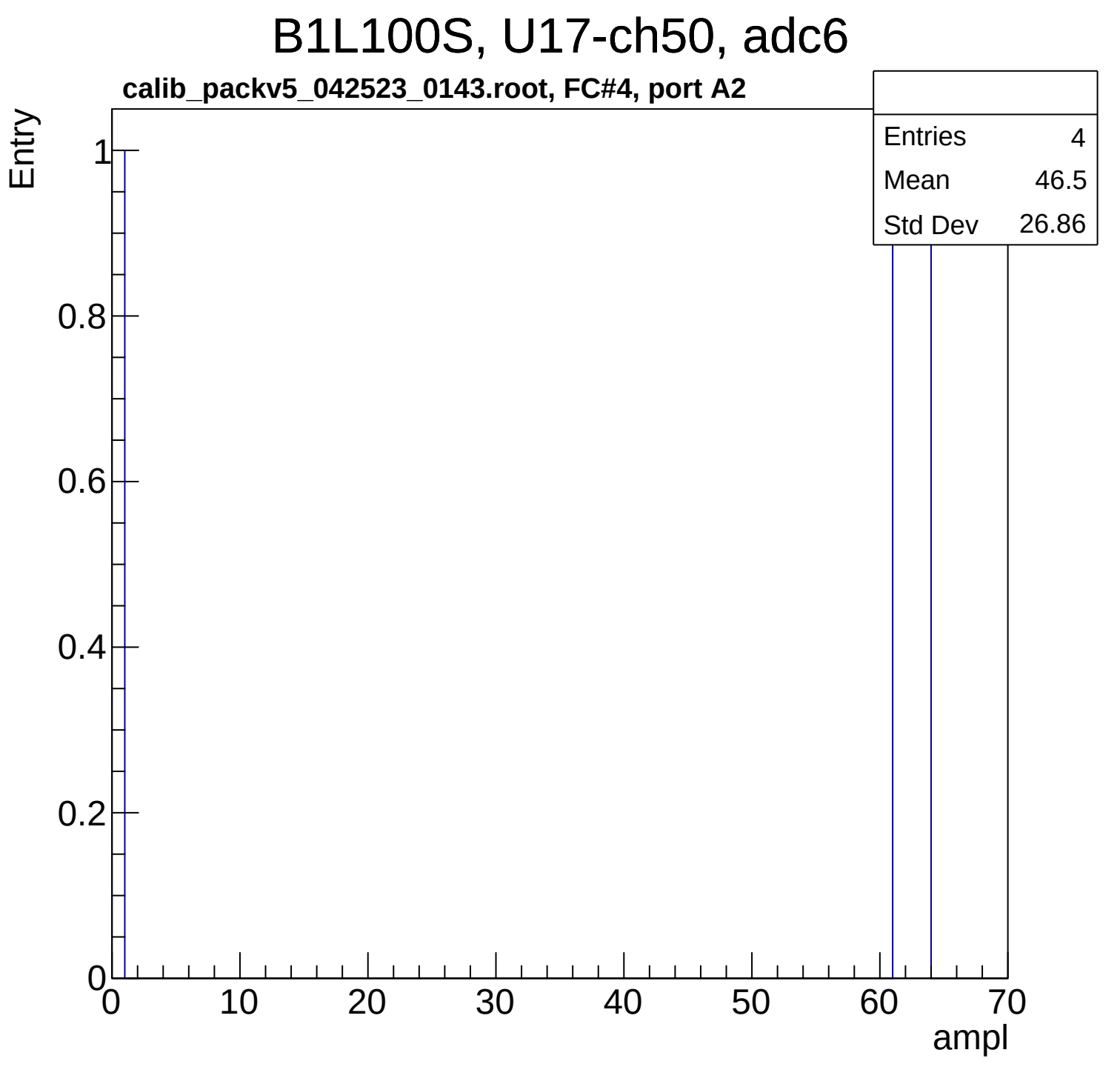
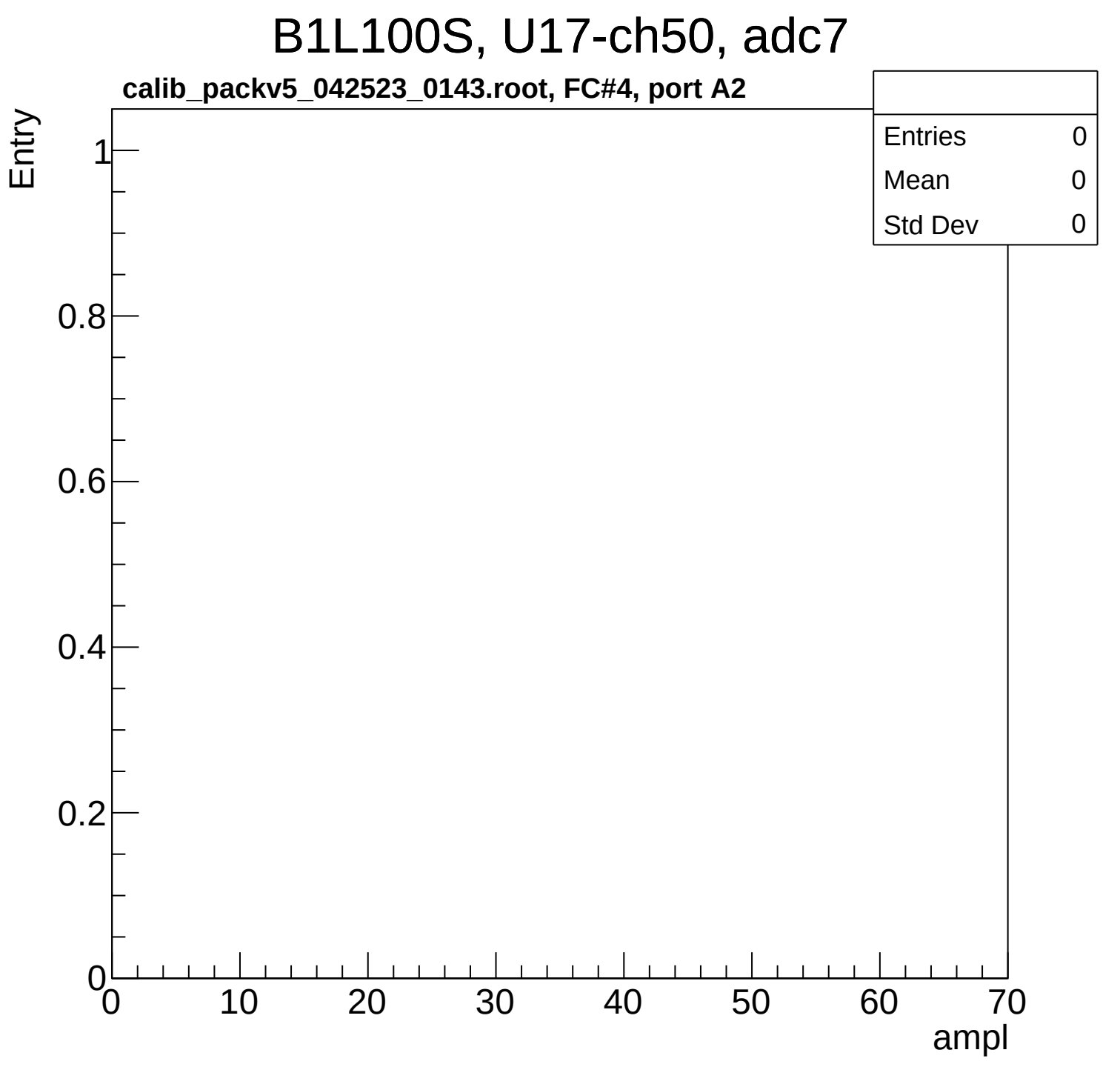
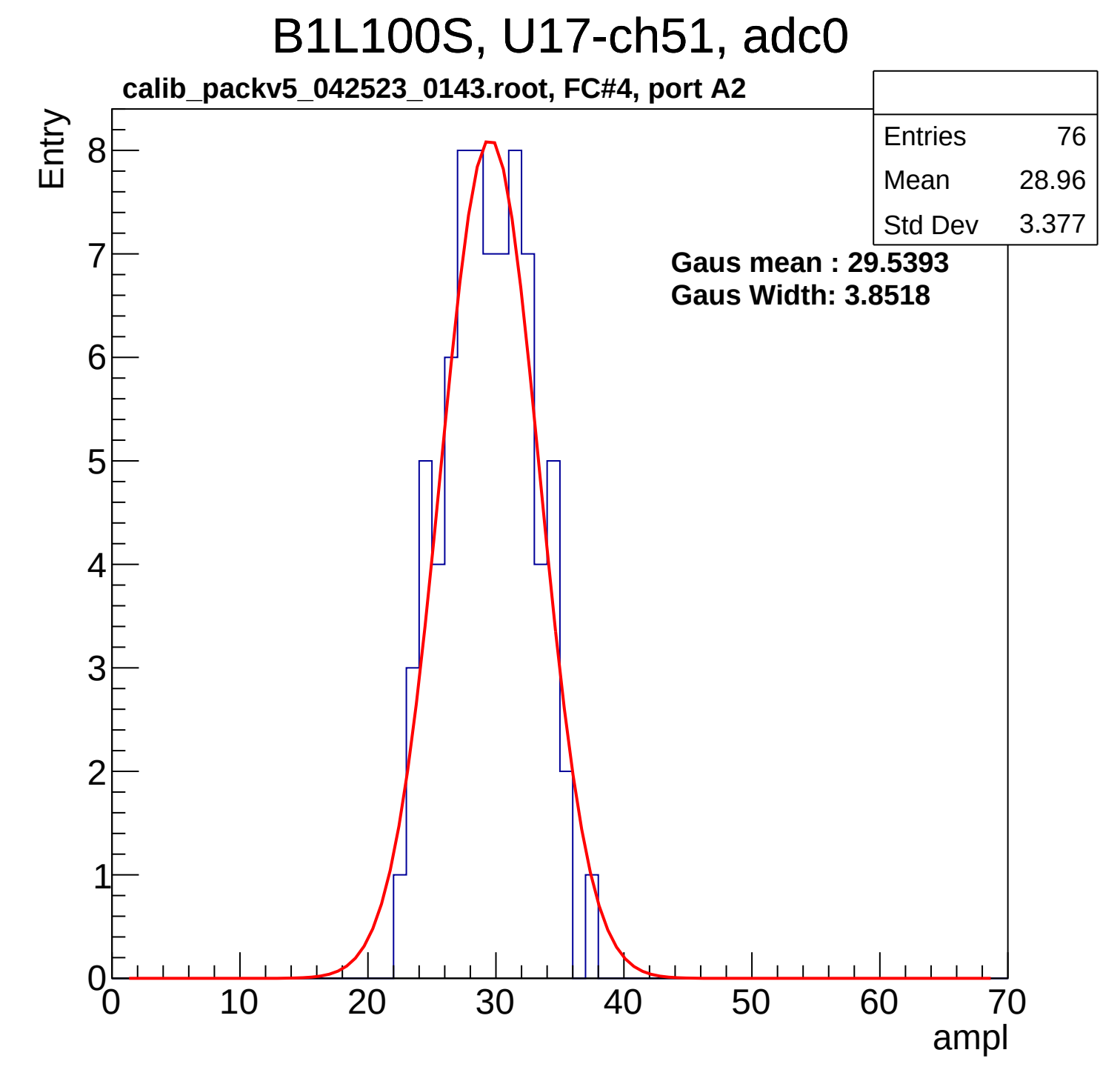
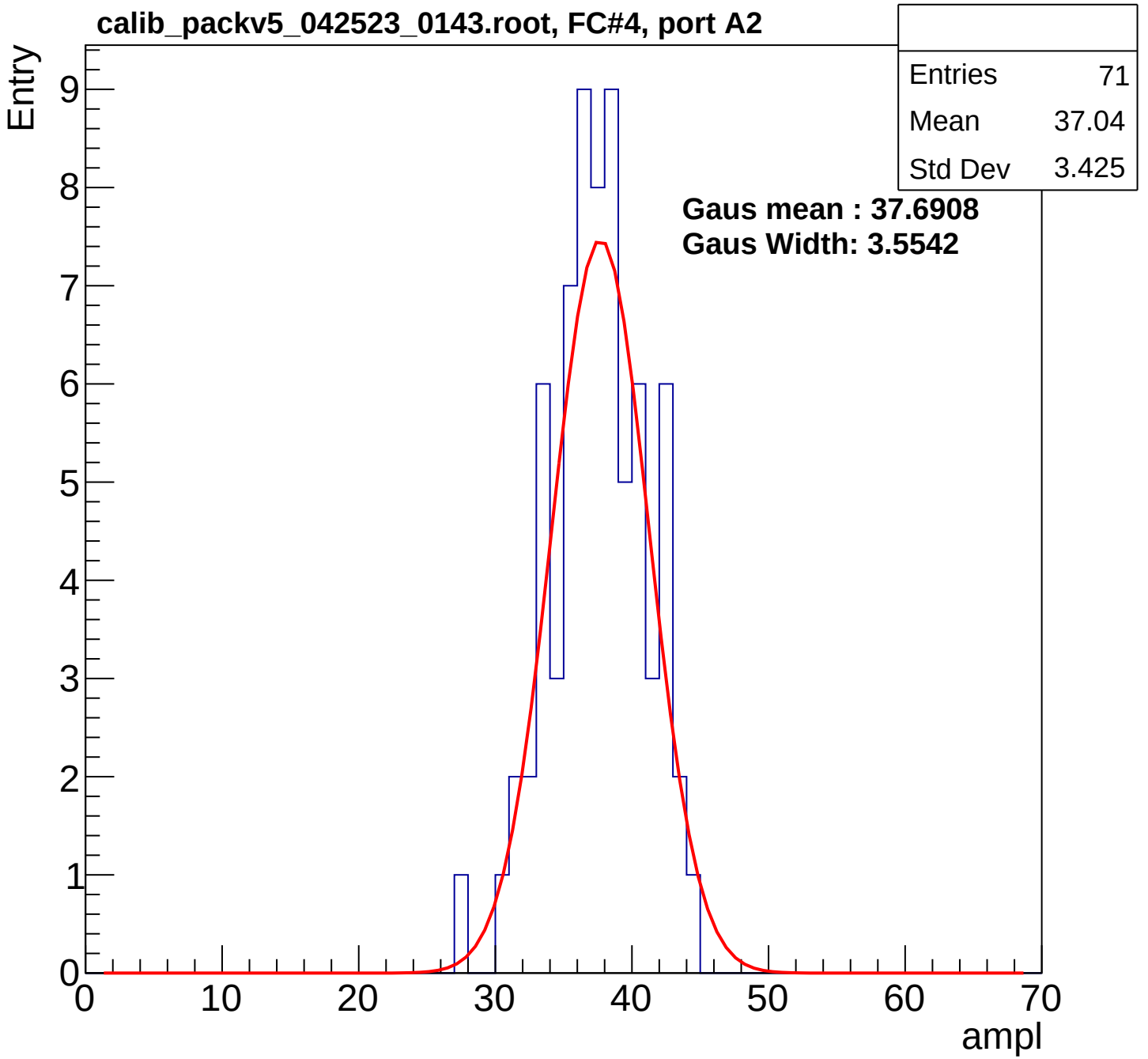
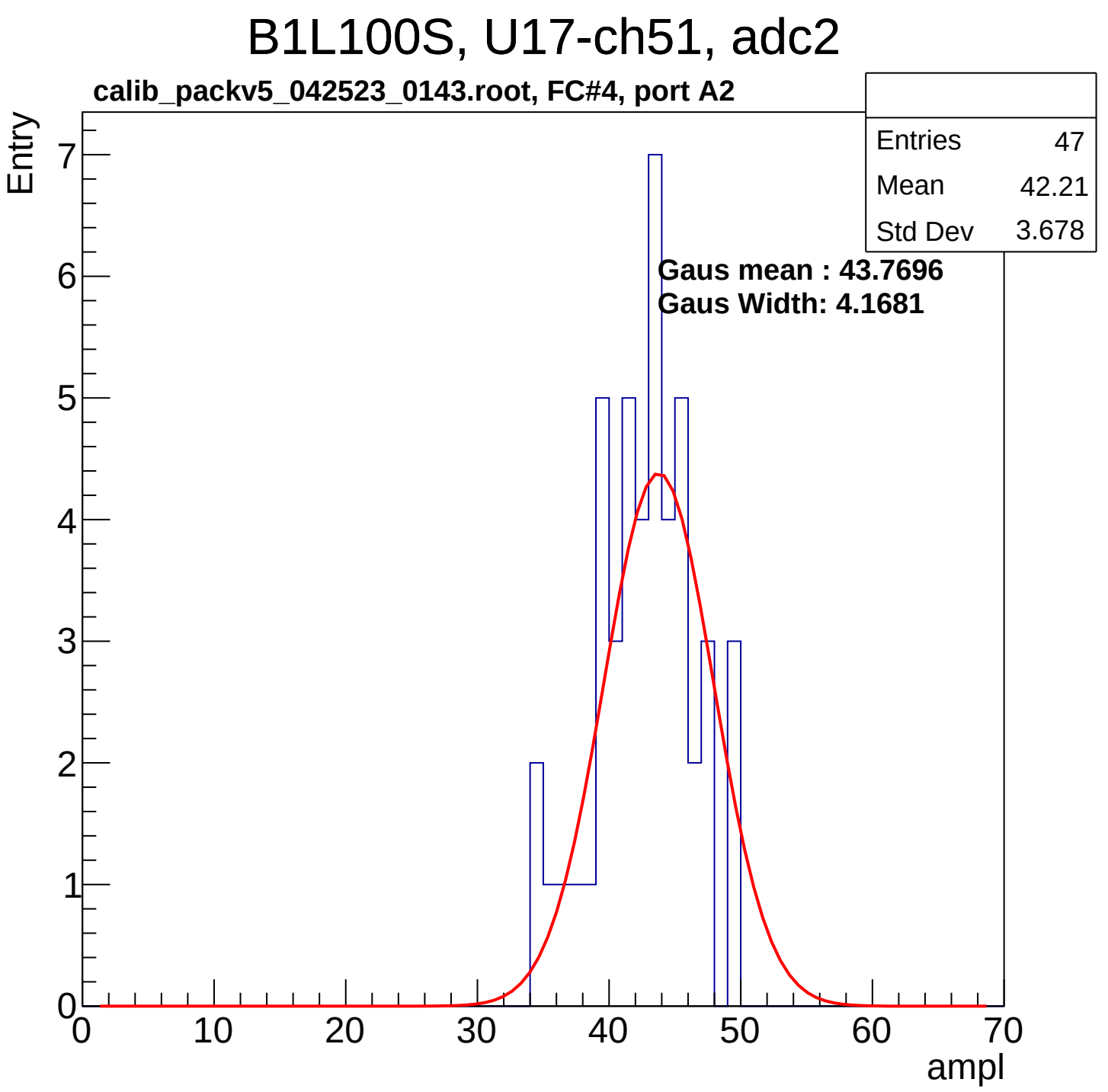
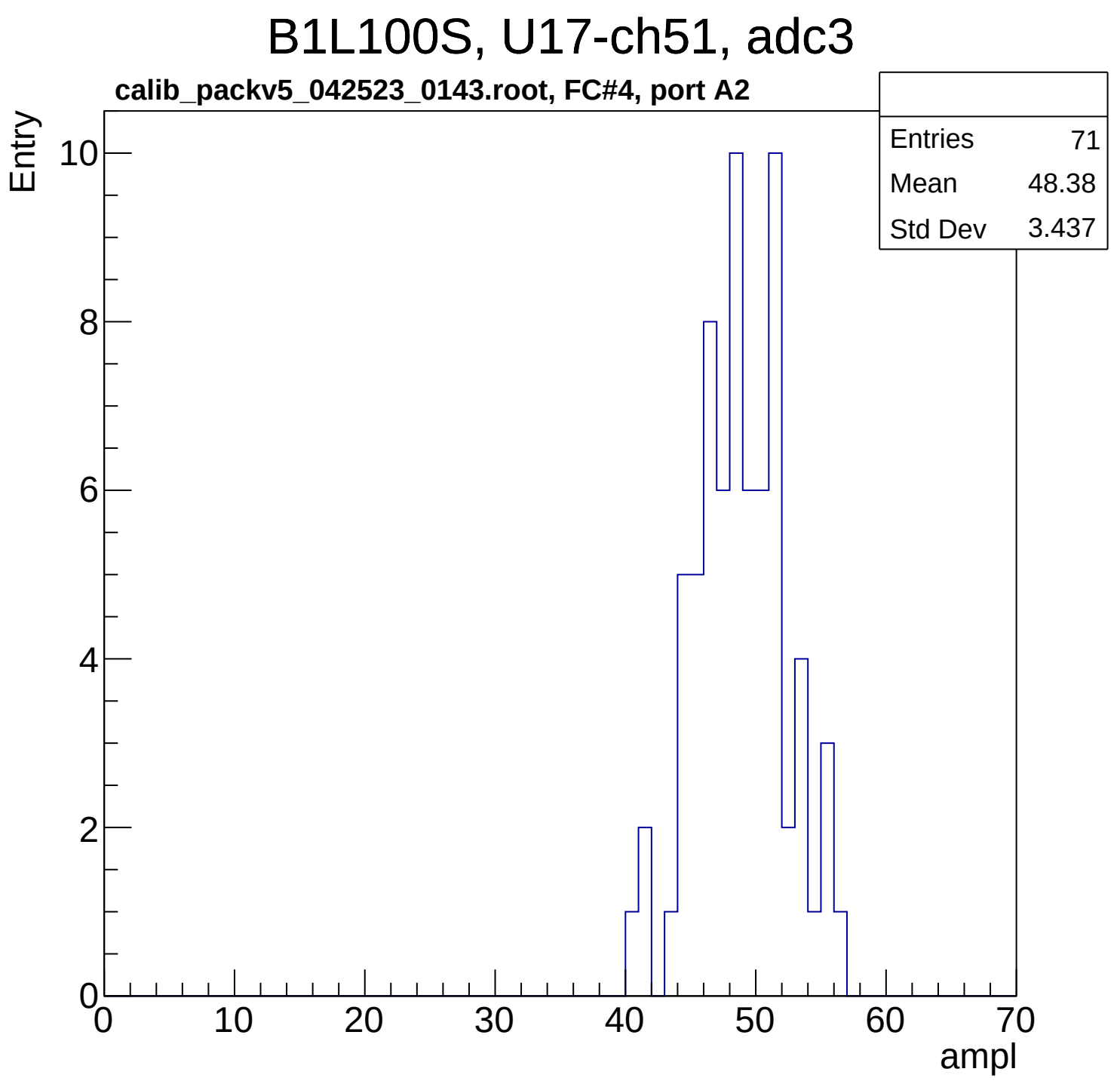

B1L100S, U17-ch50, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 4
Mean 46.5
Std Dev 26.86
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

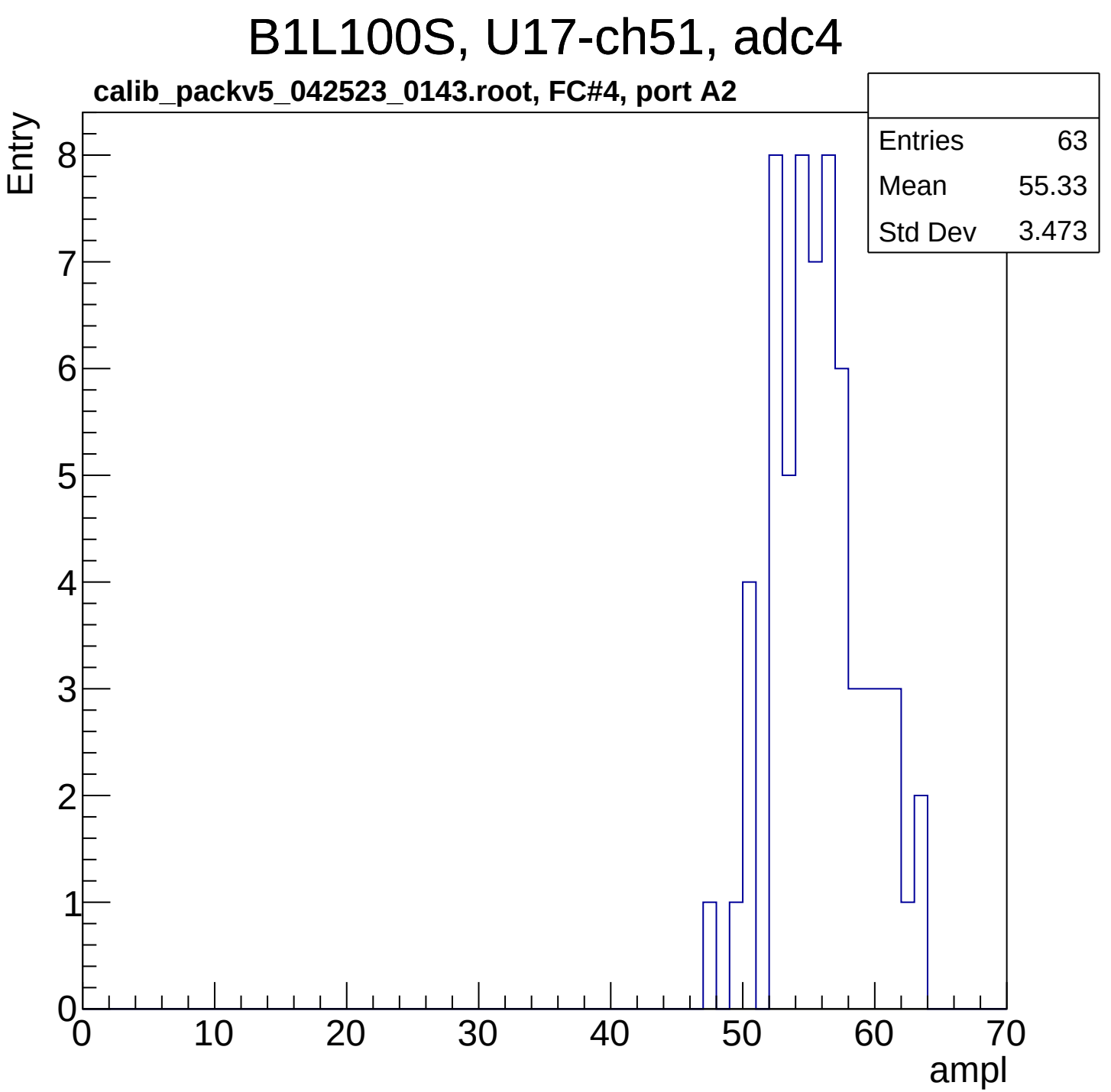

B1L100S, U17-ch50, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch51, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 76
Mean 28.96
Std Dev 3.377
Gaus mean : 29.5393
Gaus Width: 3.8518
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch51, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 37.04
Std Dev 3.425
Gaus mean : 37.6908
Gaus Width: 3.5542
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch51, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 47
Mean 42.21
Std Dev 3.678
Gaus mean : 43.7696
Gaus Width: 4.1681
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U17-ch51, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 48.38
Std Dev 3.437
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch51, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 55.33
Std Dev 3.473
Entry
ampl
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1
2
3
4
5
6
7
8
0
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40
50
60
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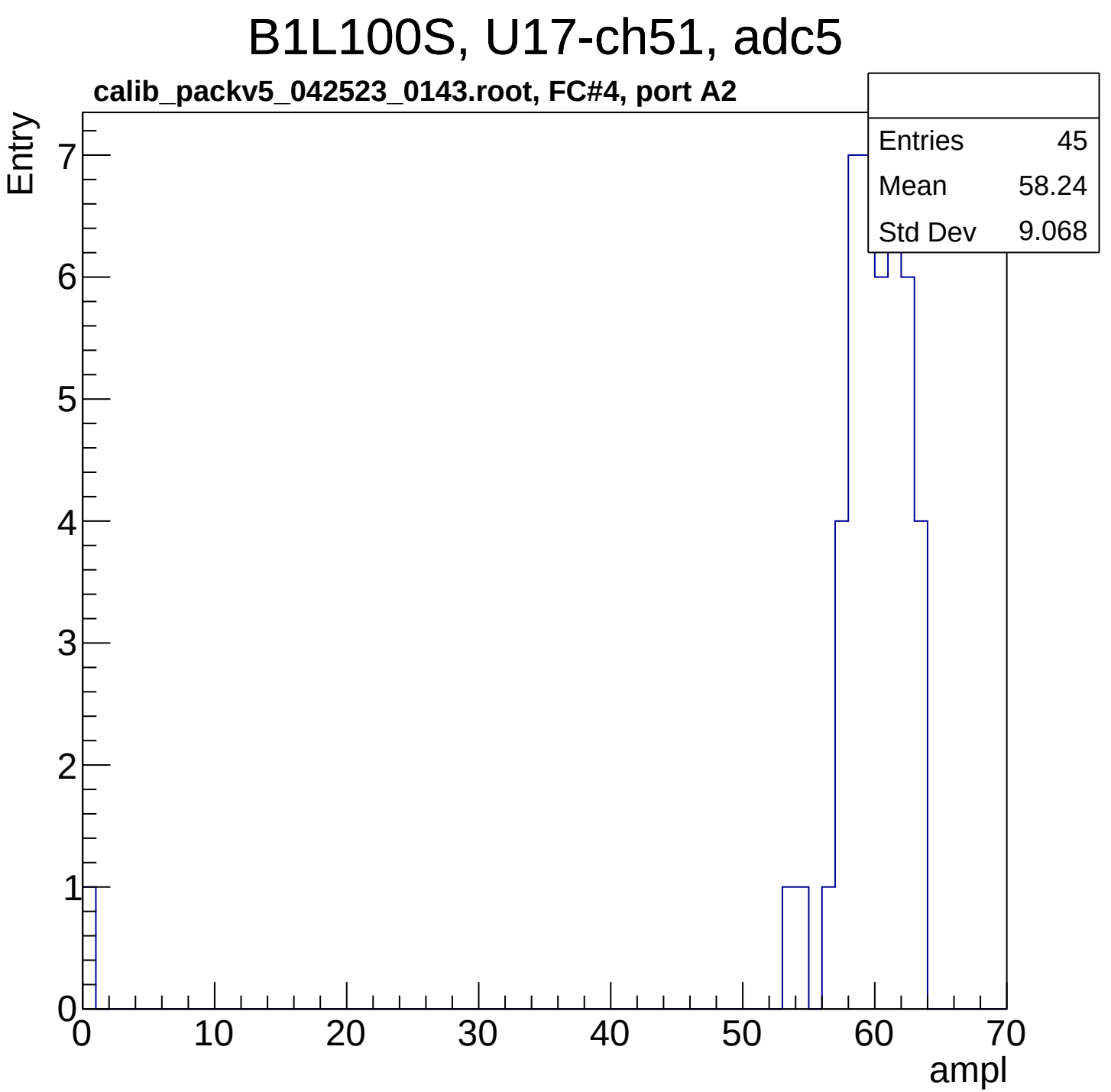
B1L100S, U17-ch51, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 45
Mean 58.24
Std Dev 9.068
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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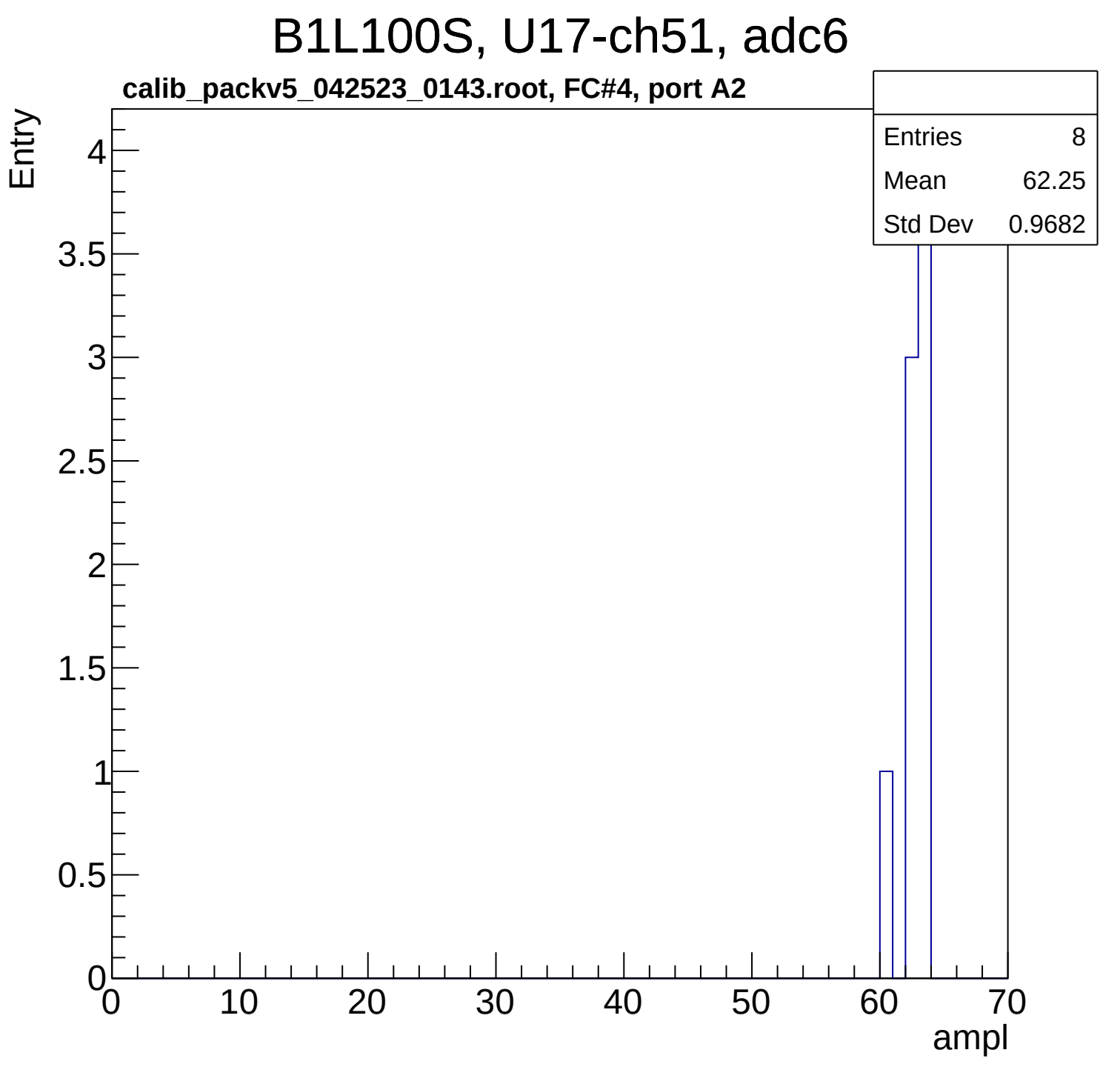
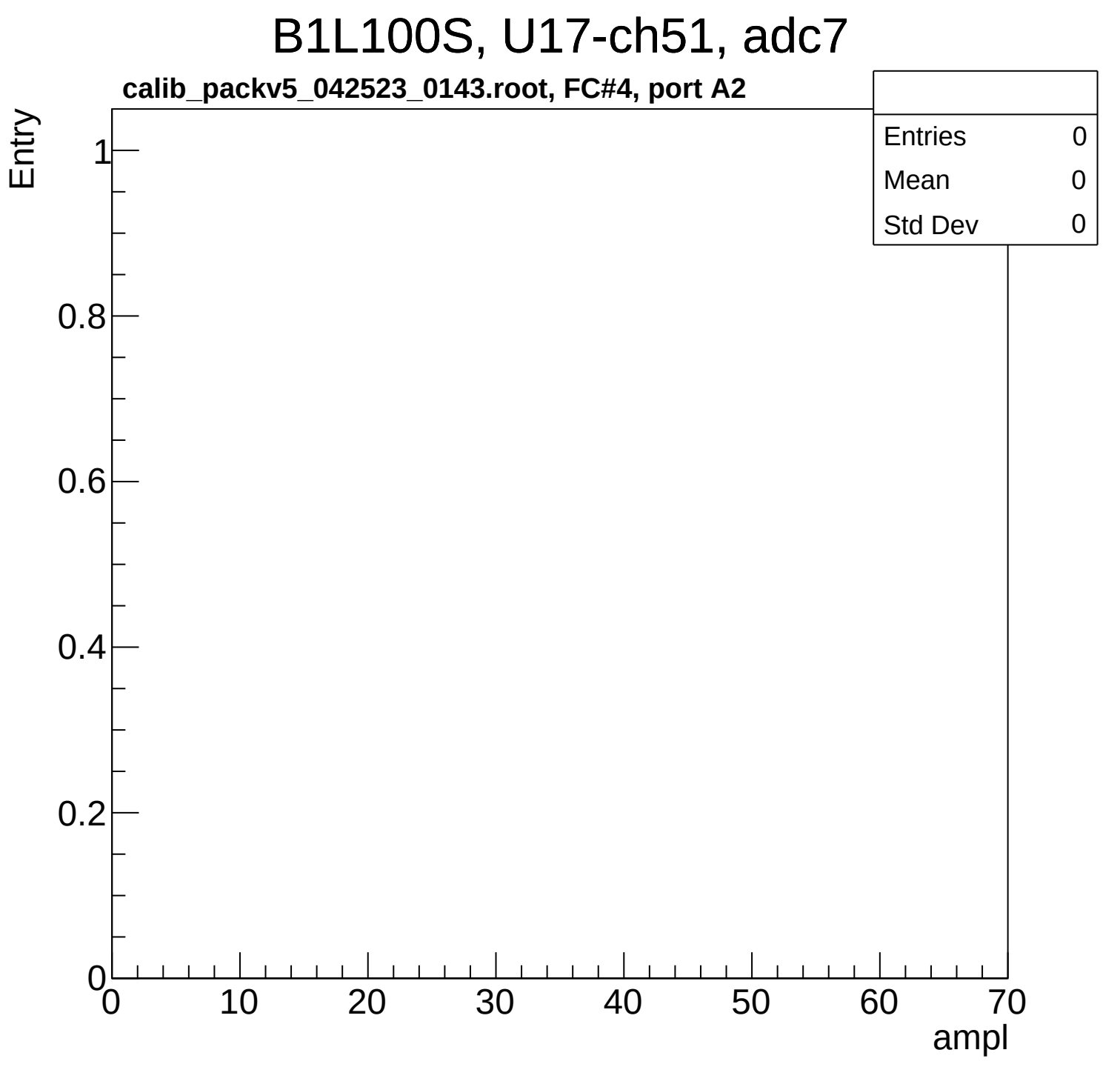
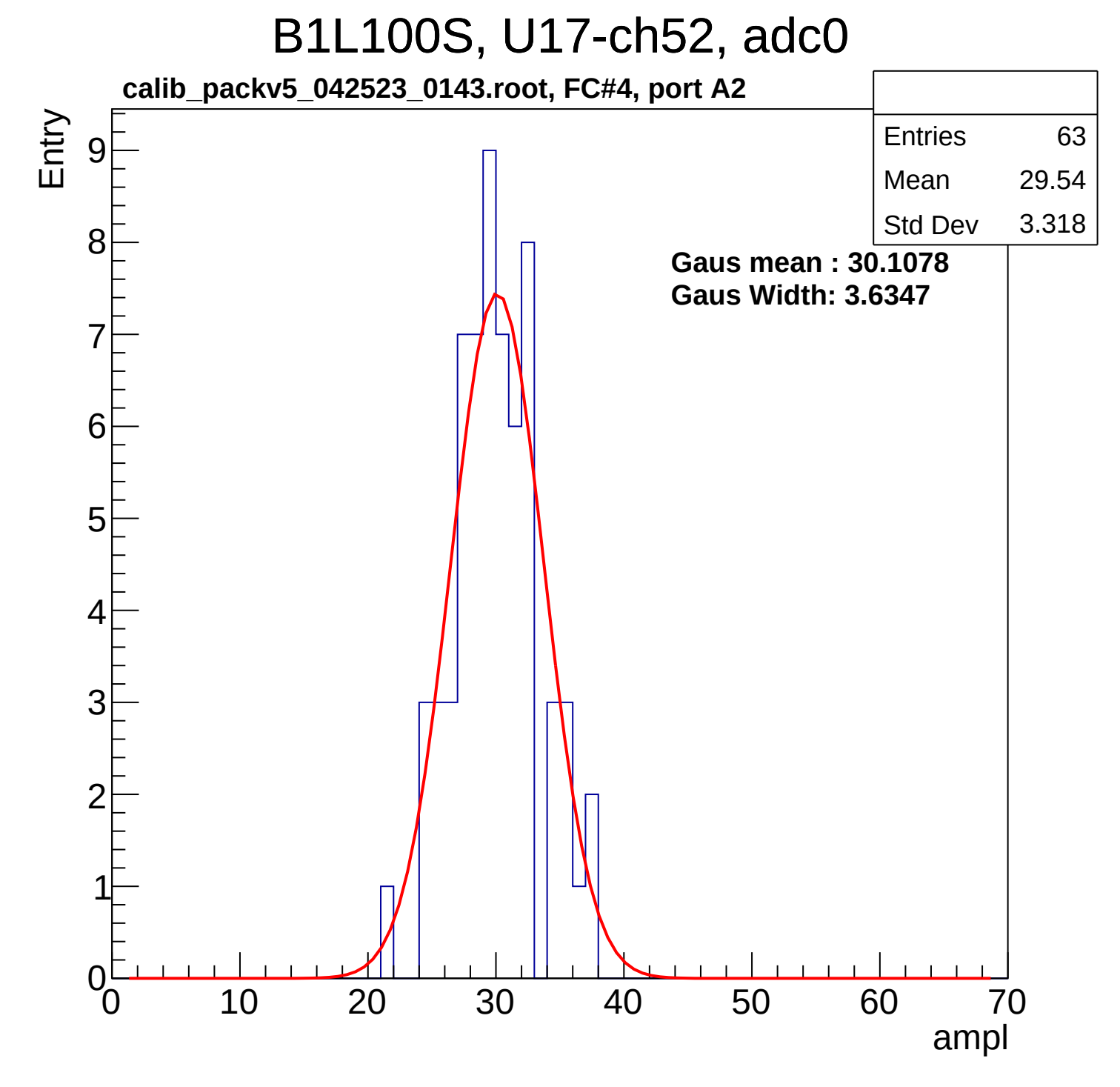
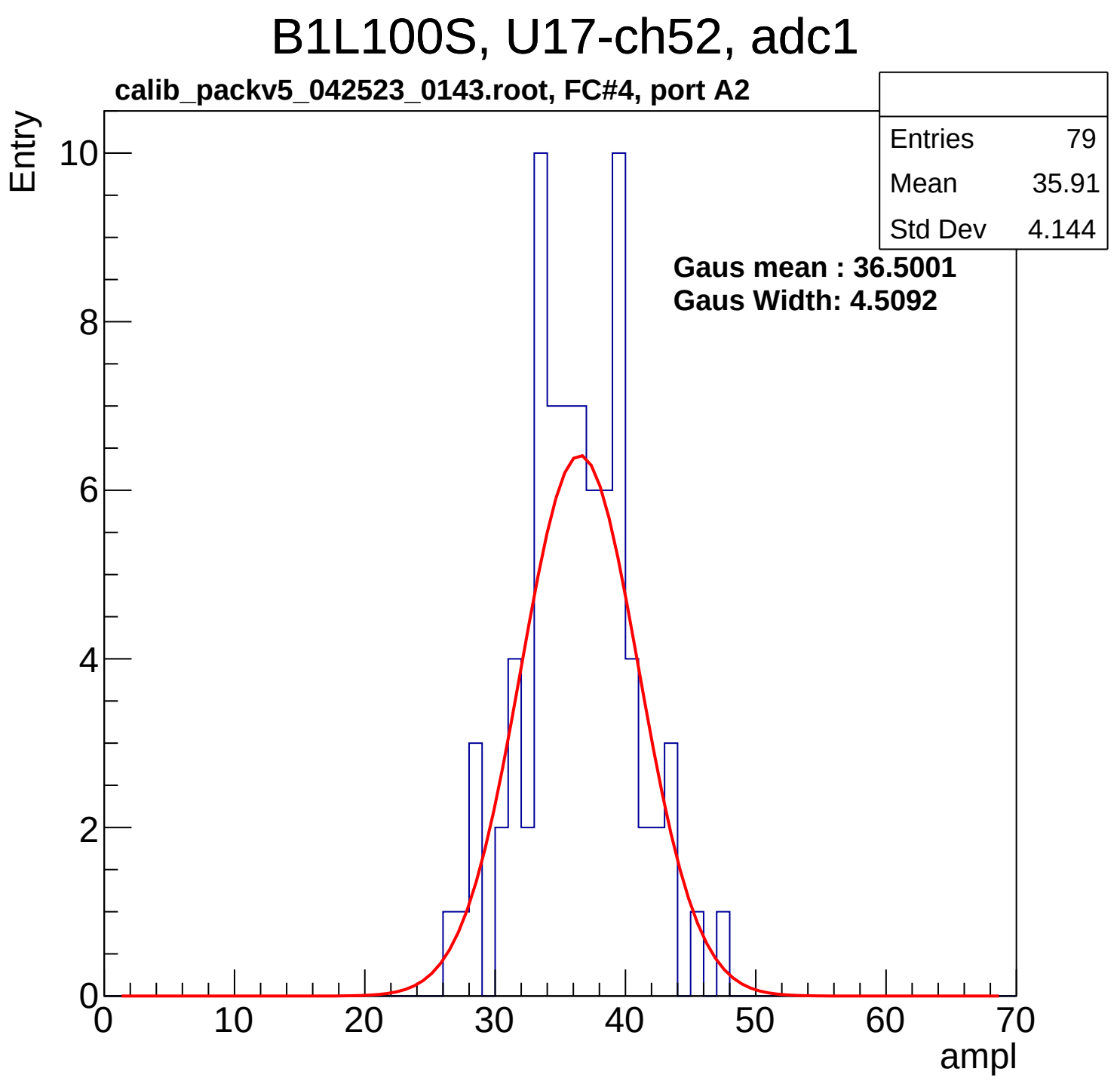
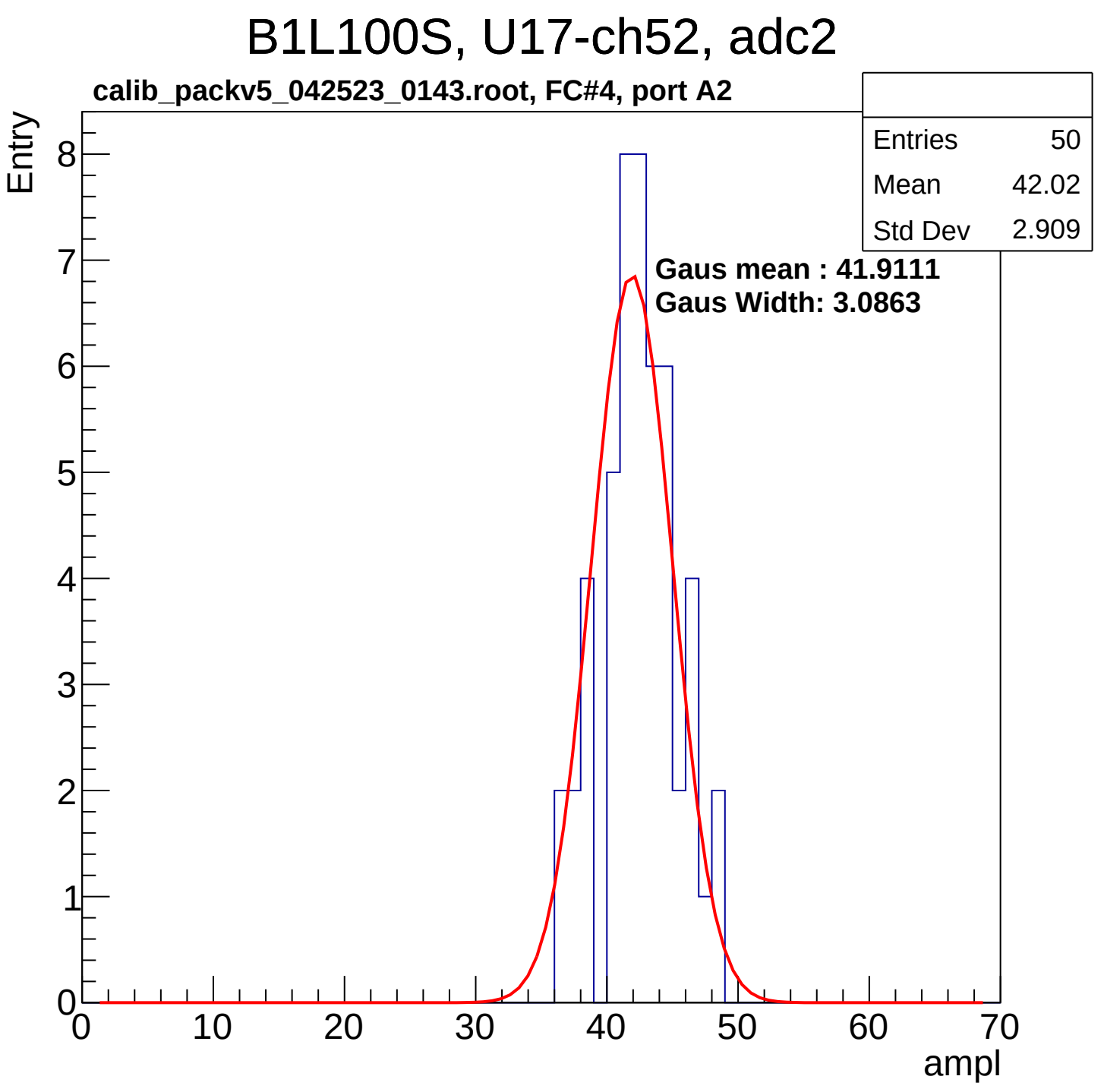
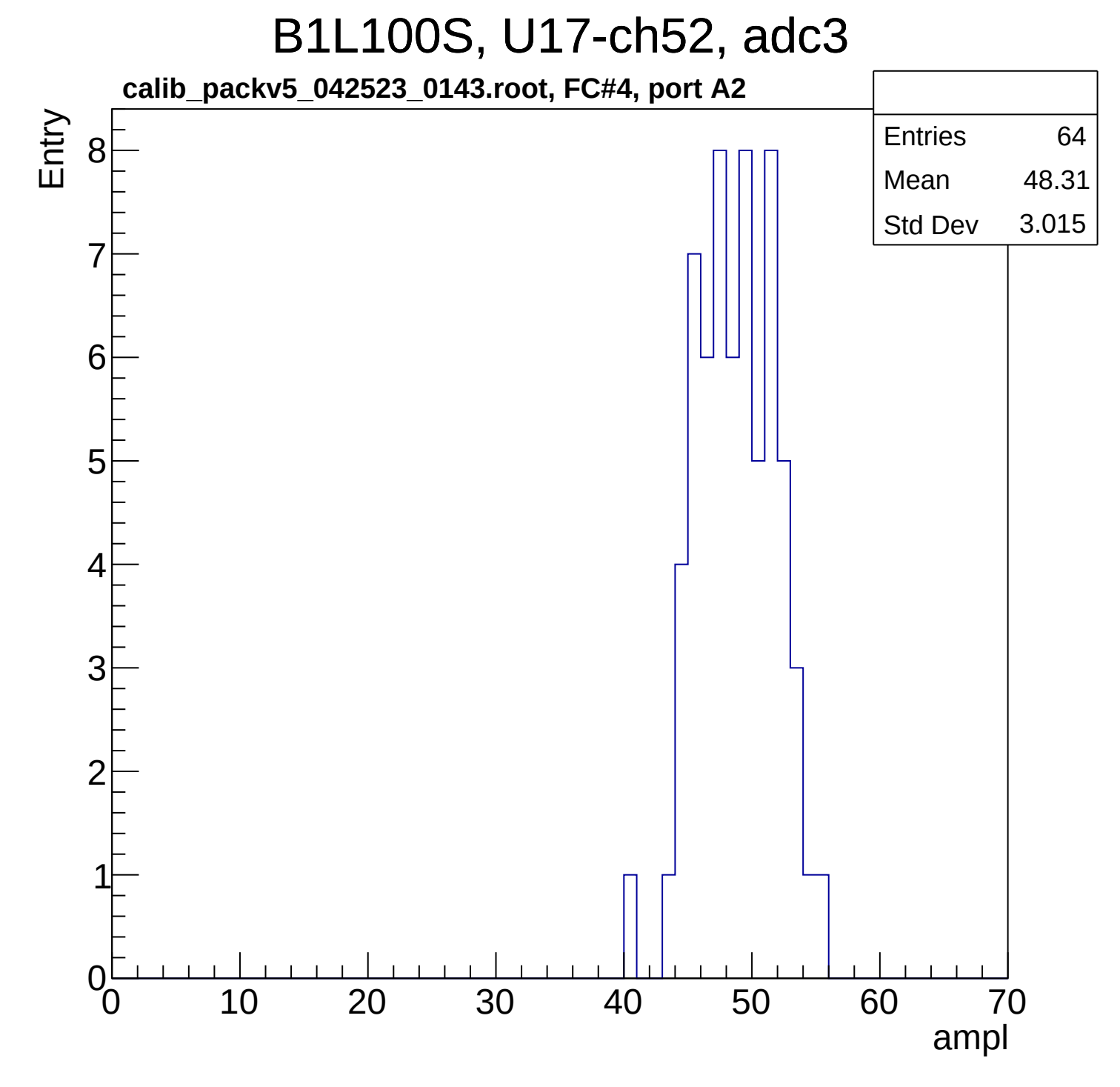

B1L100S, U17-ch51, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 8
Mean 62.25
Std Dev 0.9682
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L100S, U17-ch51, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch52, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 29.54
Std Dev 3.318
Gaus mean : 30.1078
Gaus Width: 3.6347
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch52, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 79
Mean 35.91
Std Dev 4.144
Gaus mean : 36.5001
Gaus Width: 4.5092
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U17-ch52, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 42.02
Std Dev 2.909
Gaus mean : 41.9111
Gaus Width: 3.0863
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch52, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 48.31
Std Dev 3.015
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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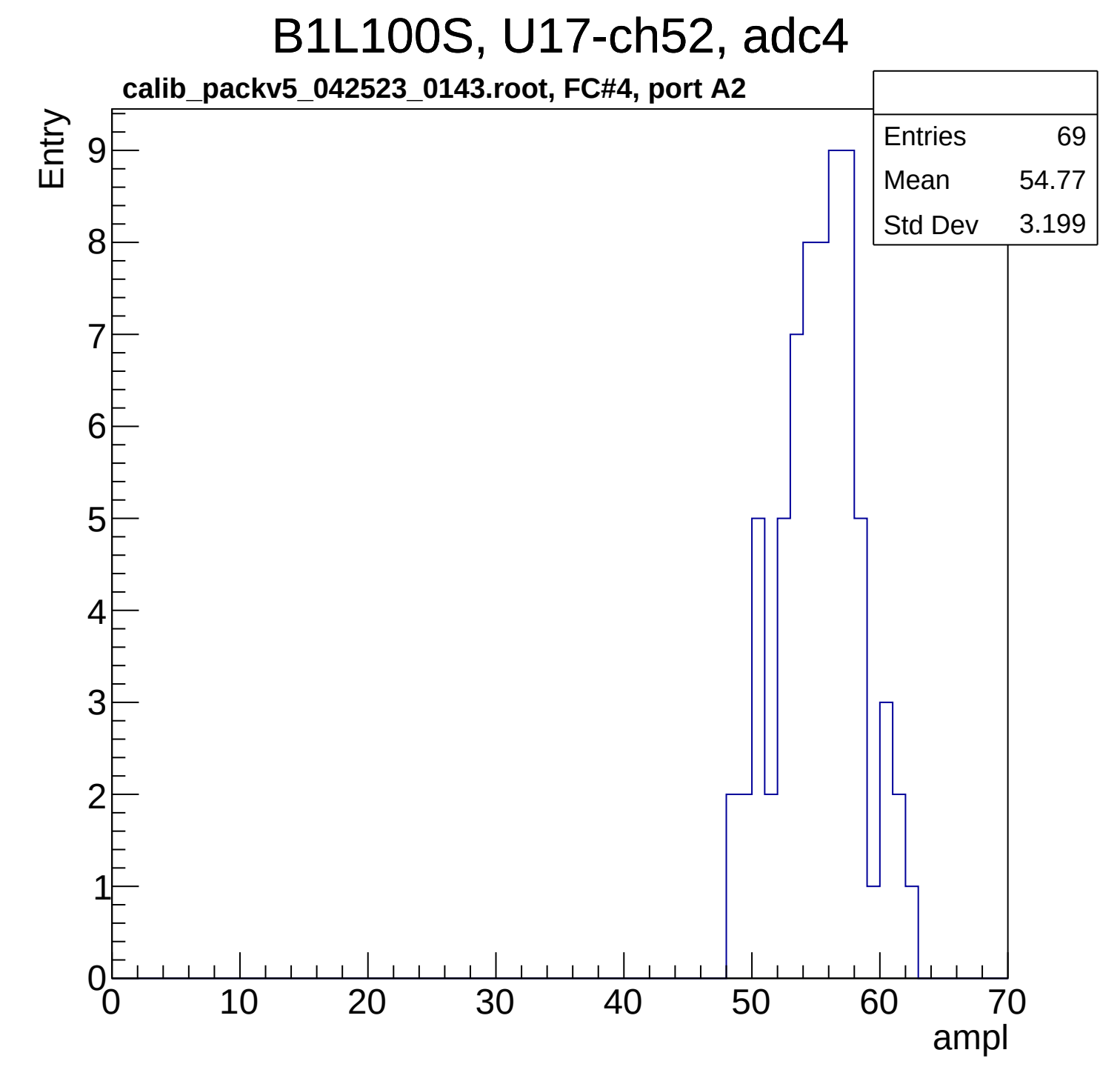
B1L100S, U17-ch52, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 54.77
Std Dev 3.199
Entry
ampl
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3
4
5
6
7
8
9
0
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20
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60
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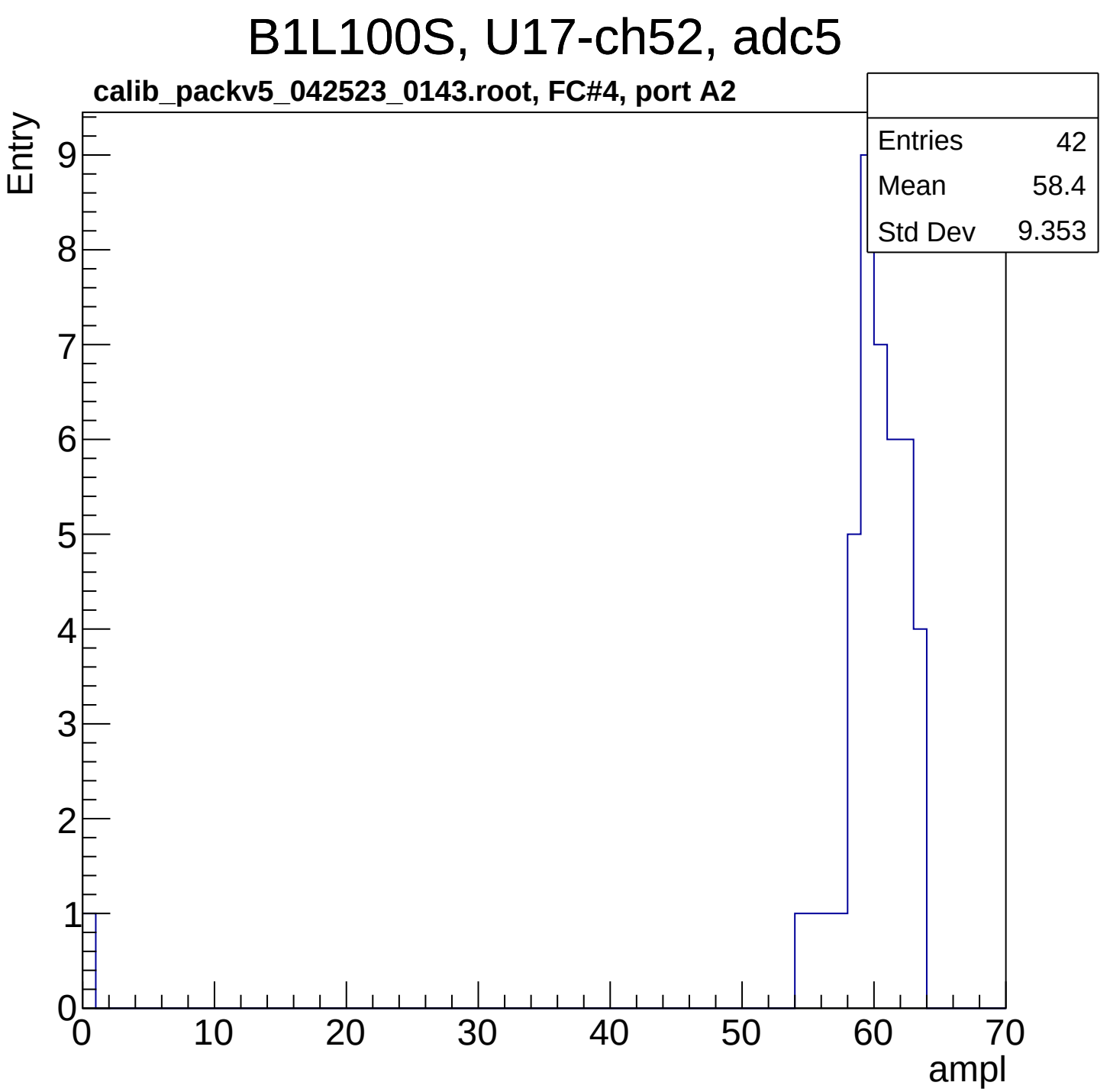
B1L100S, U17-ch52, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 42
Mean 58.4
Std Dev 9.353
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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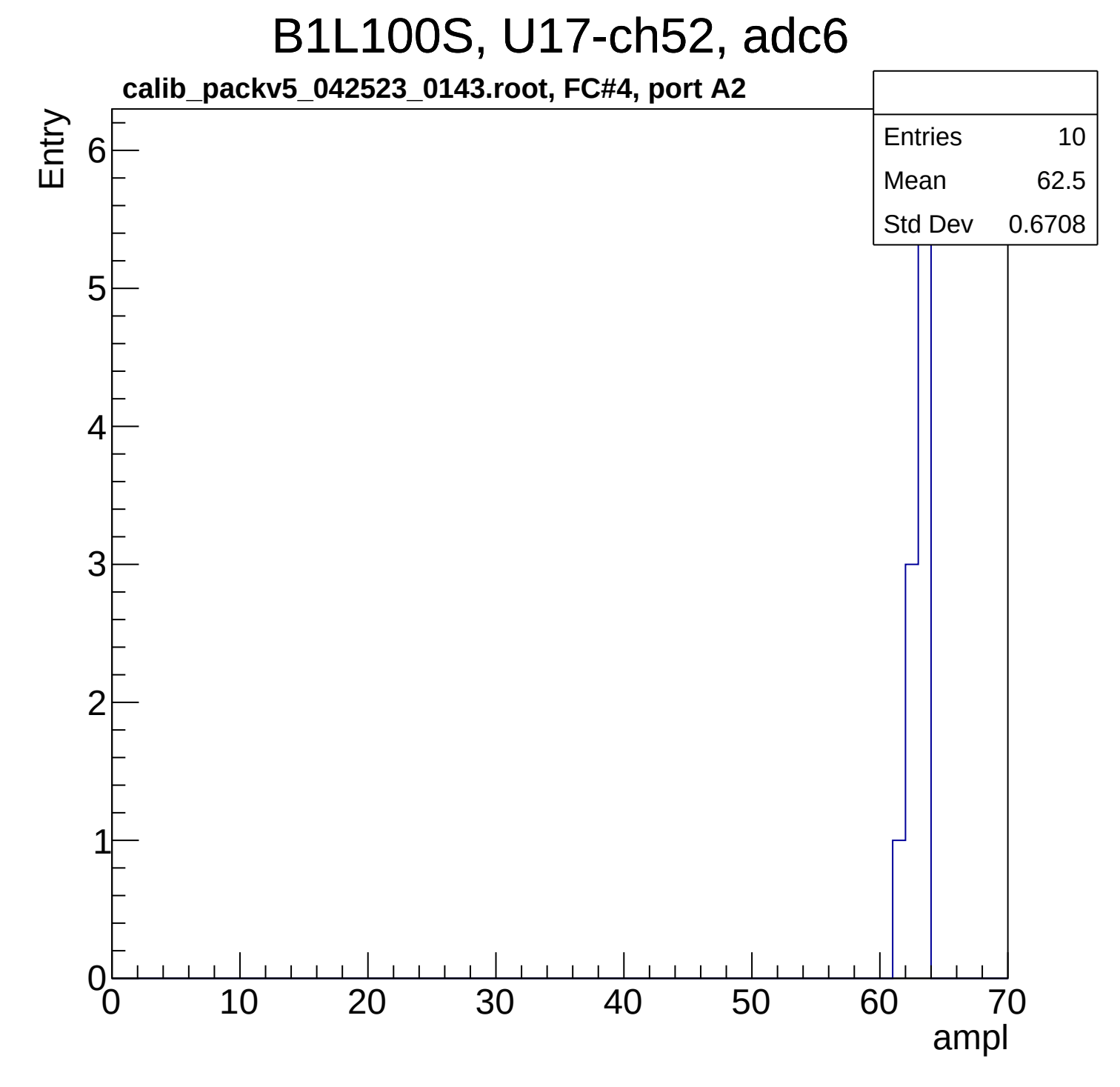
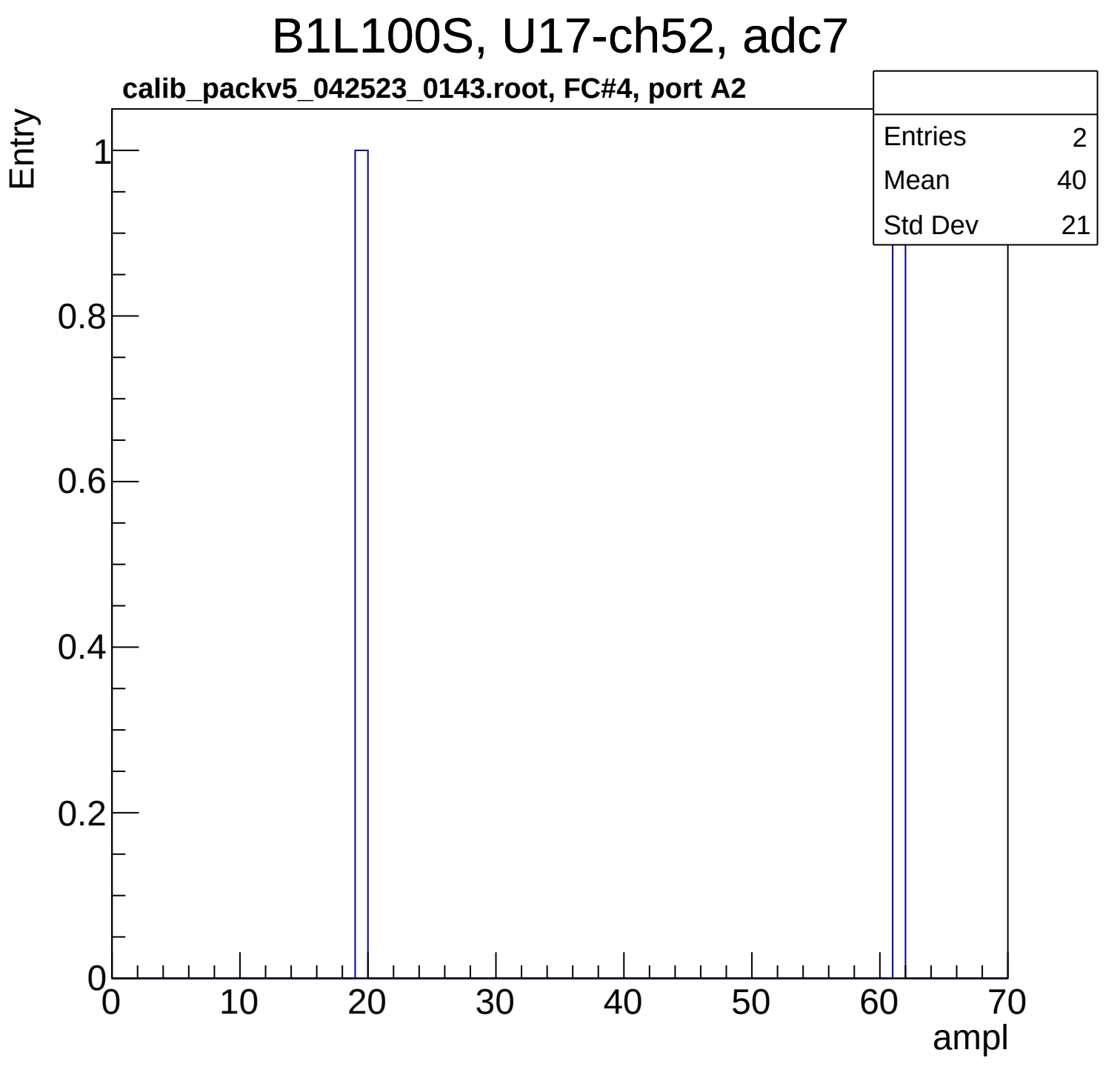
50
60
70


B1L100S, U17-ch52, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 10
Mean 62.5
Std Dev 0.6708
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch52, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 40
Std Dev 21
Entry
ampl
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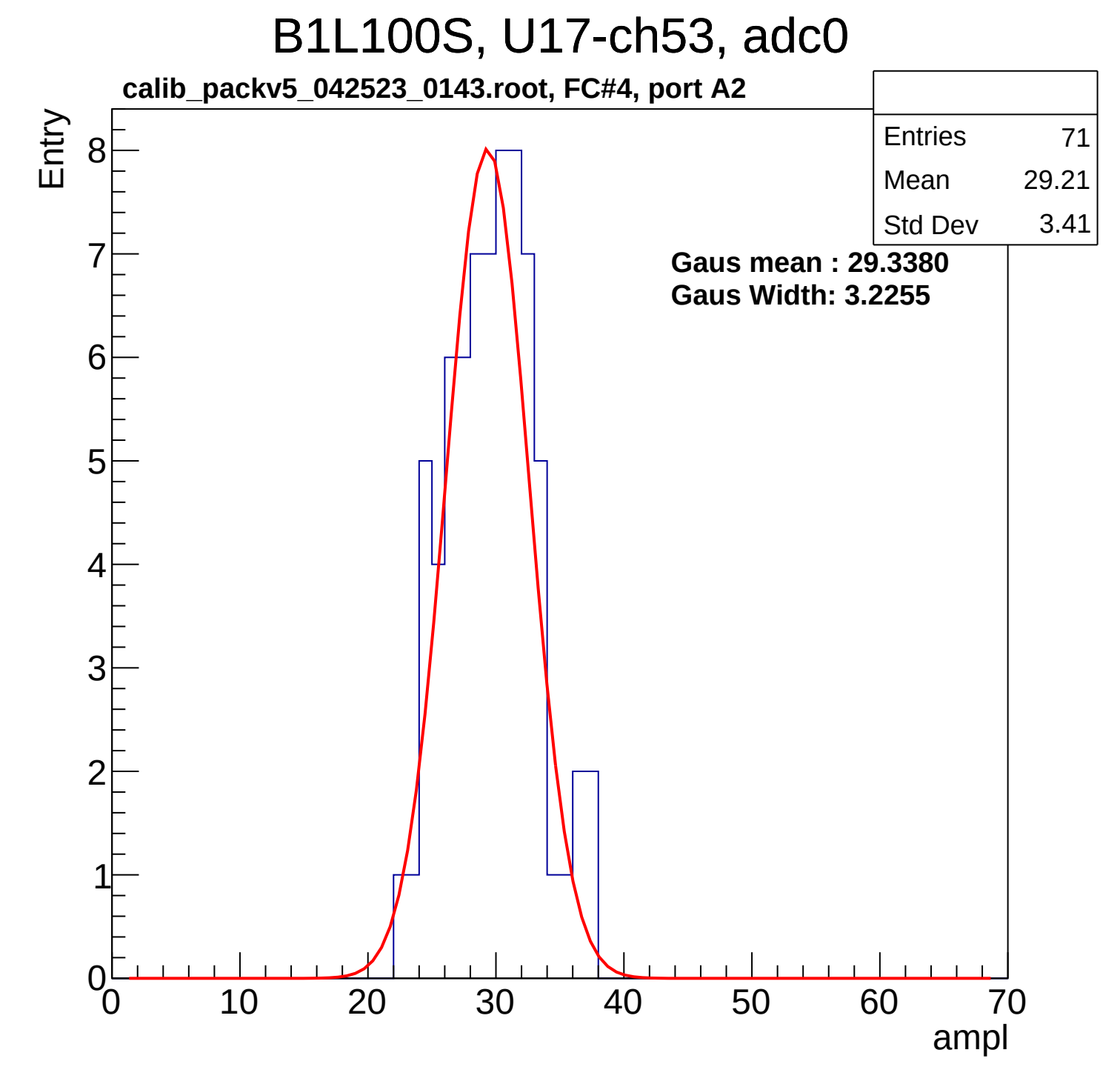
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B1L100S, U17-ch53, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 29.21
Std Dev 3.41
Gaus mean : 29.3380
Gaus Width: 3.2255
Entry
ampl
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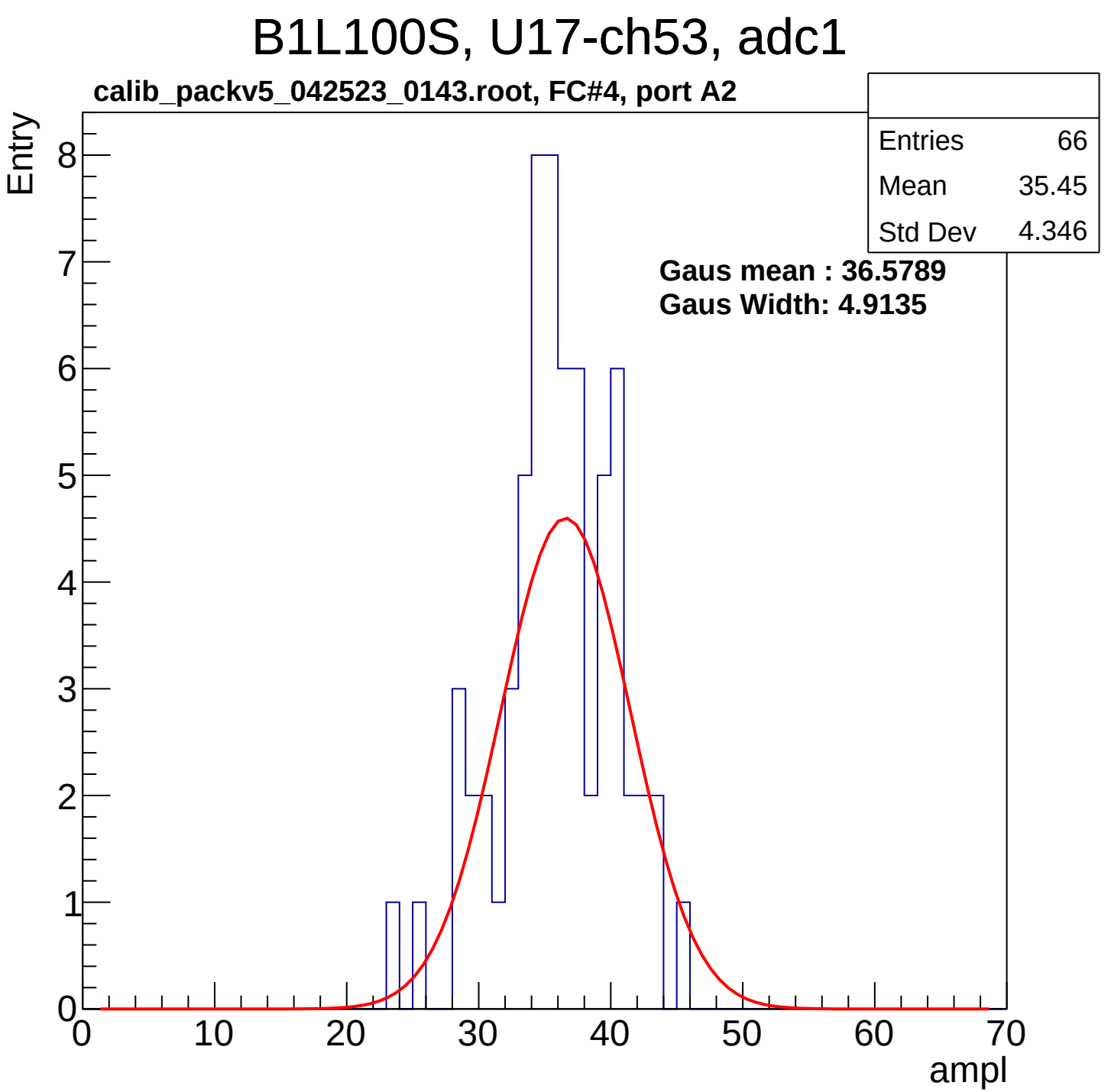
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch53, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 35.45
Std Dev 4.346
Gaus mean : 36.5789
Gaus Width: 4.9135
Entry
ampl
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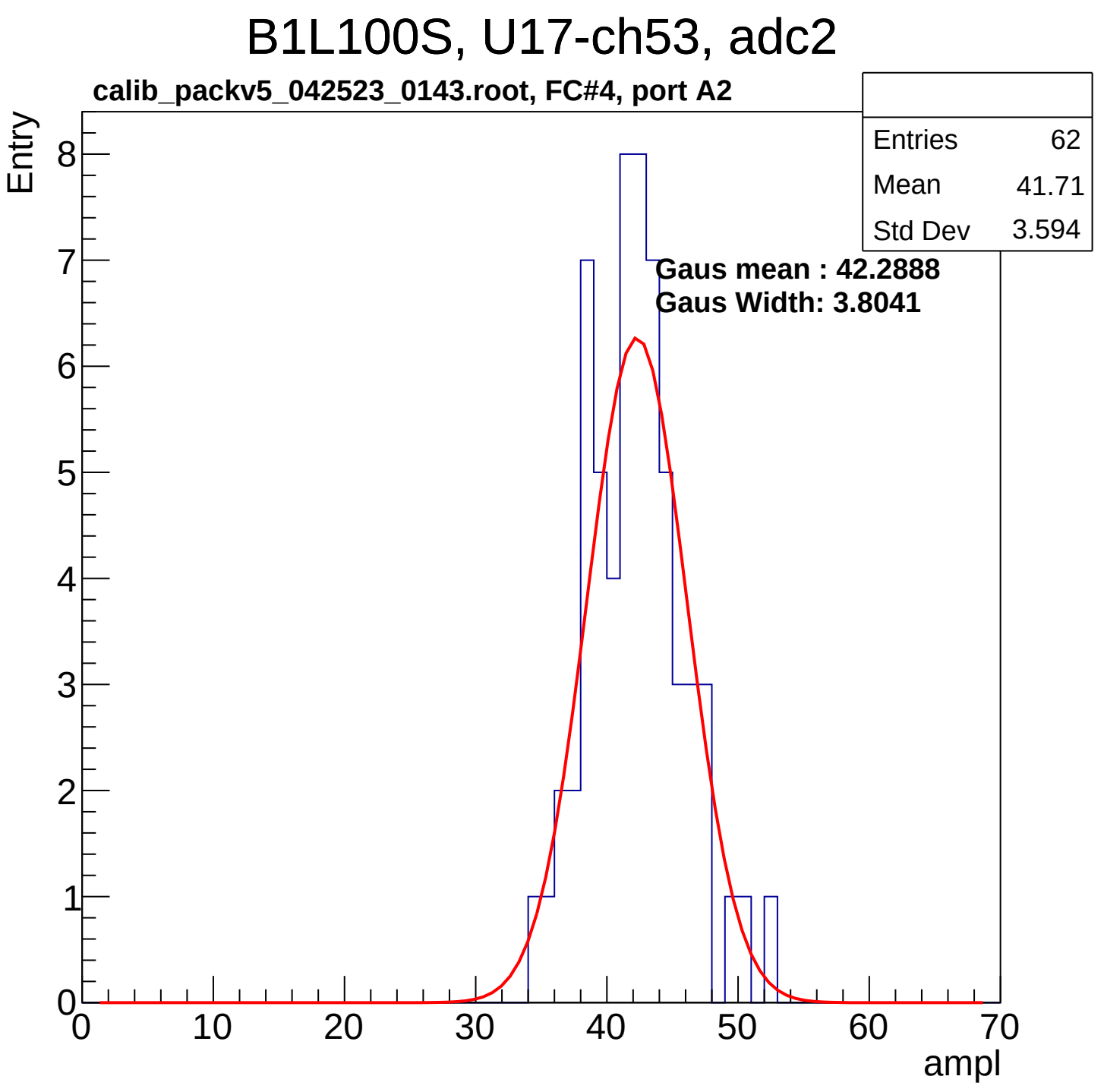
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch53, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 41.71
Std Dev 3.594
Gaus mean : 42.2888
Gaus Width: 3.8041
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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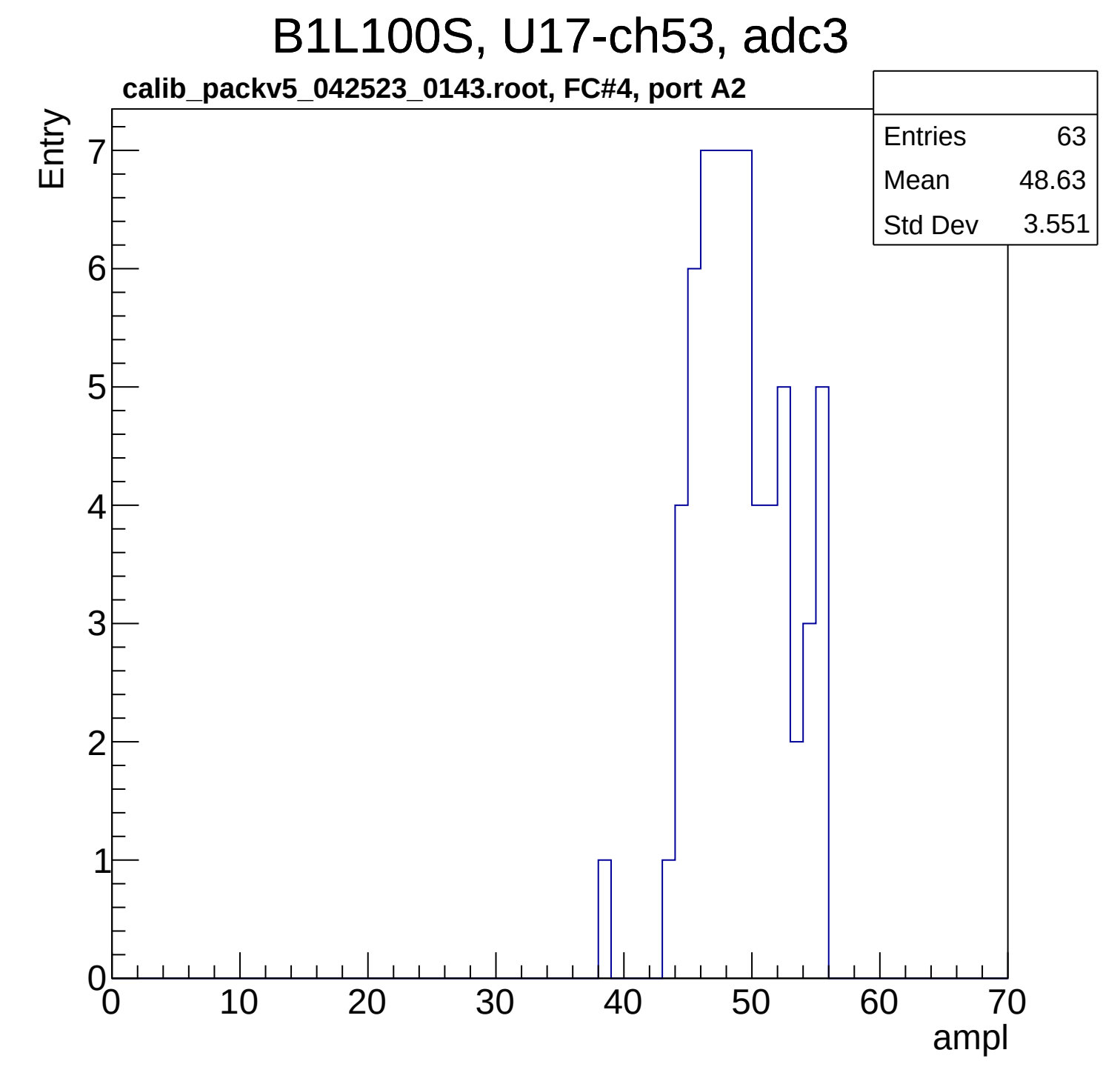
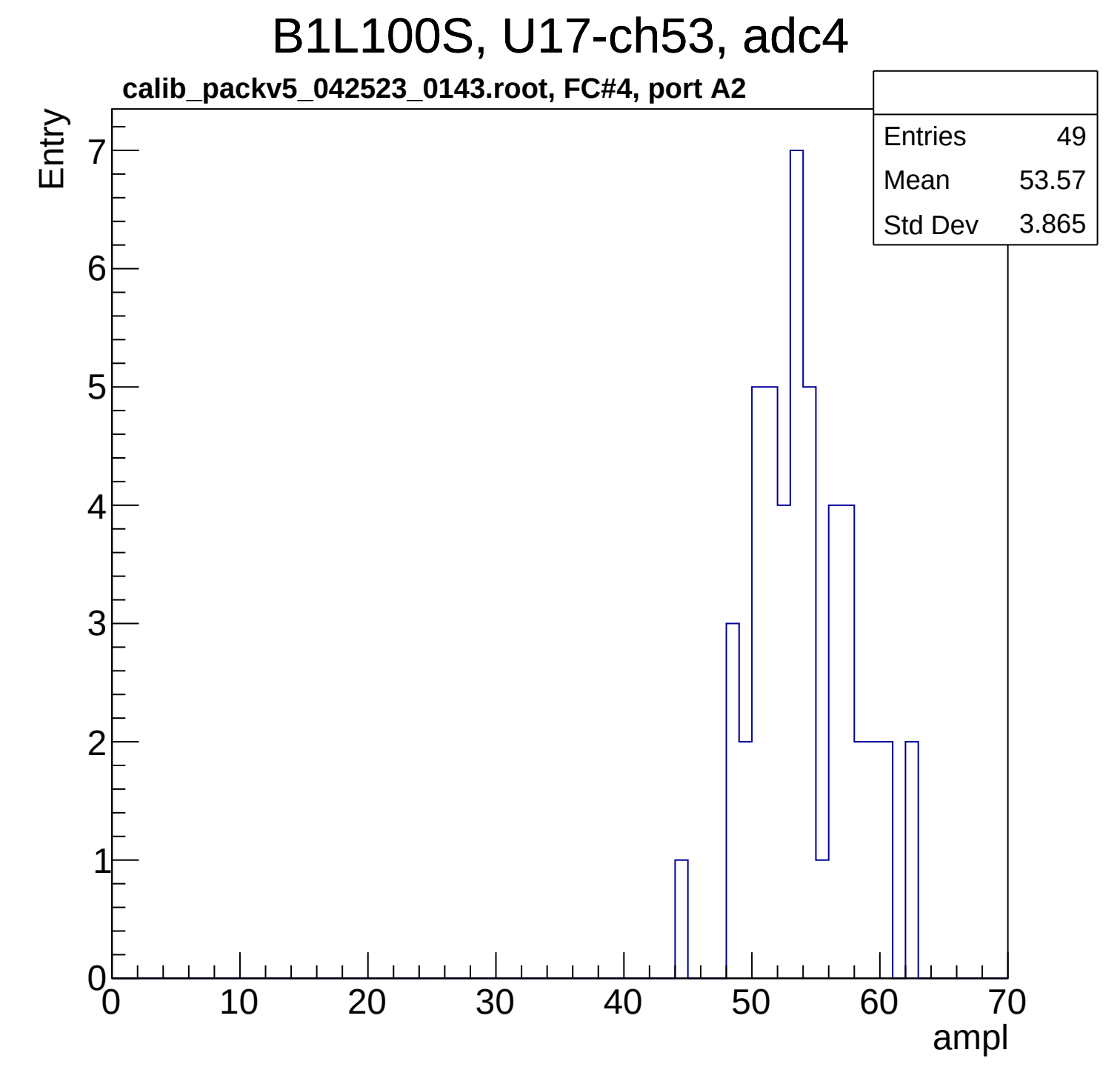

B1L100S, U17-ch53, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 48.63
Std Dev 3.551
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U17-ch53, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 49
Mean 53.57
Std Dev 3.865
Entry
ampl
0
1
2
3
4
5
6
7
0
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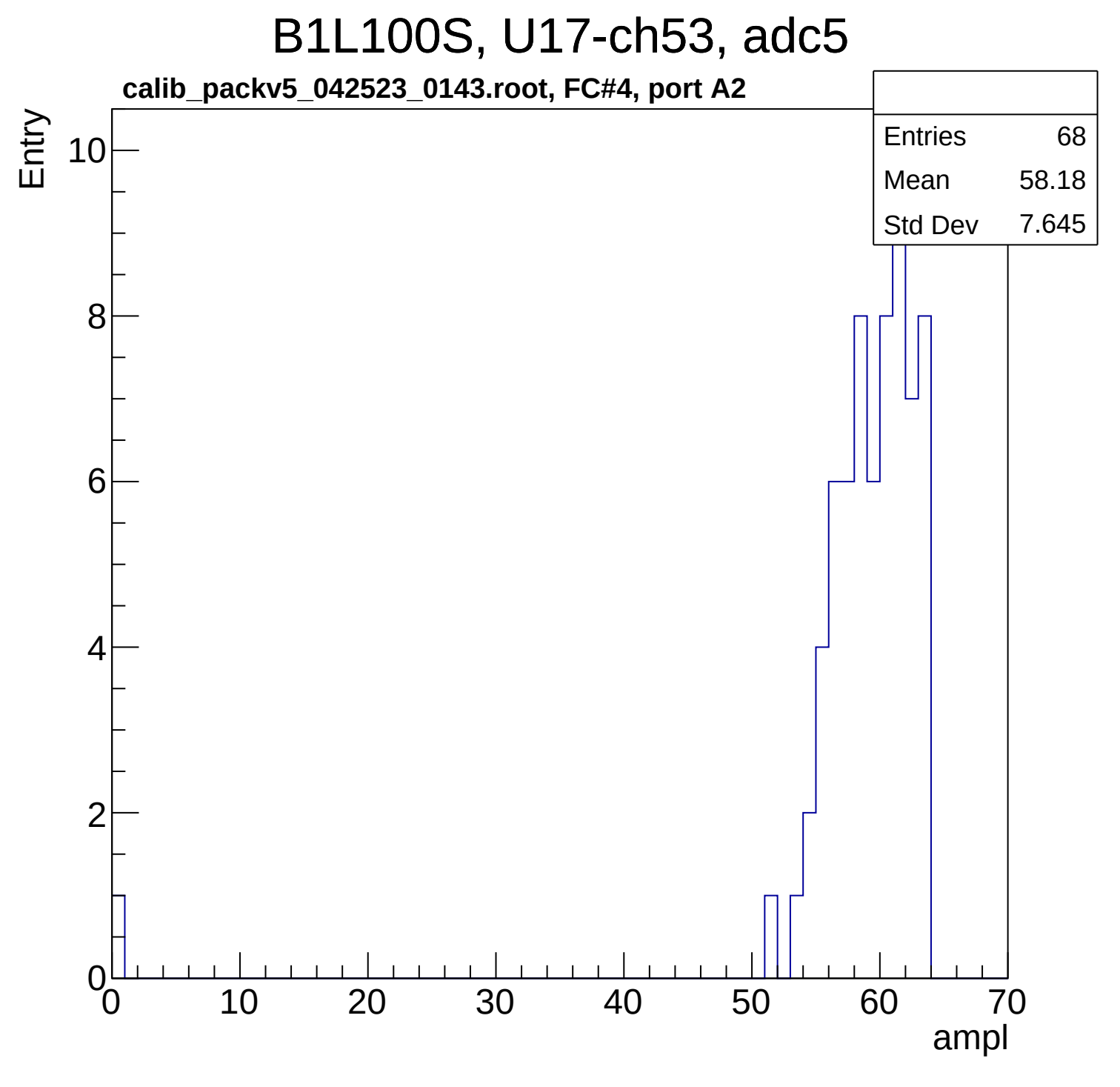
20
30
40
50
60
70


B1L100S, U17-ch53, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 58.18
Std Dev 7.645
Entry
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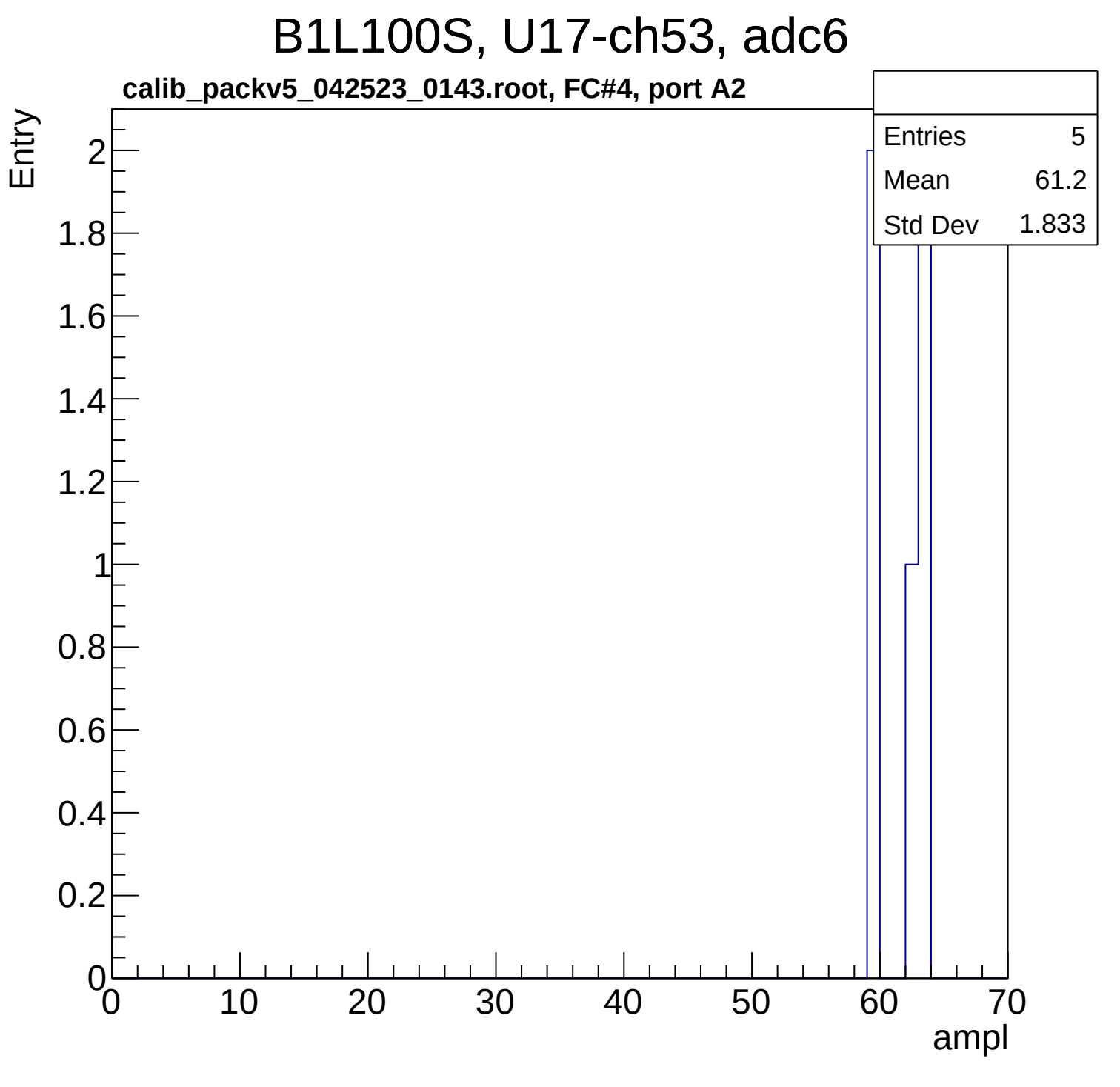
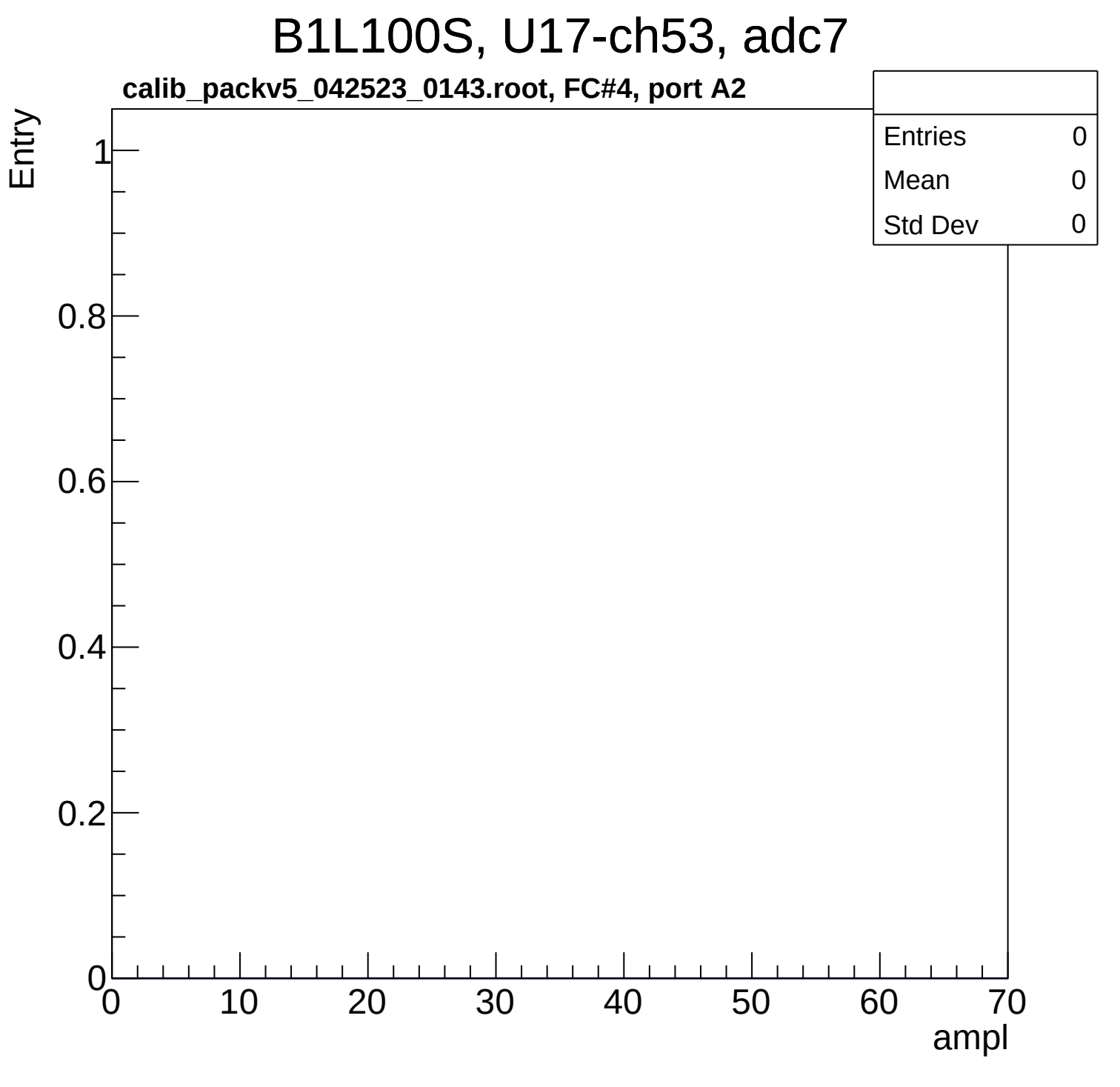
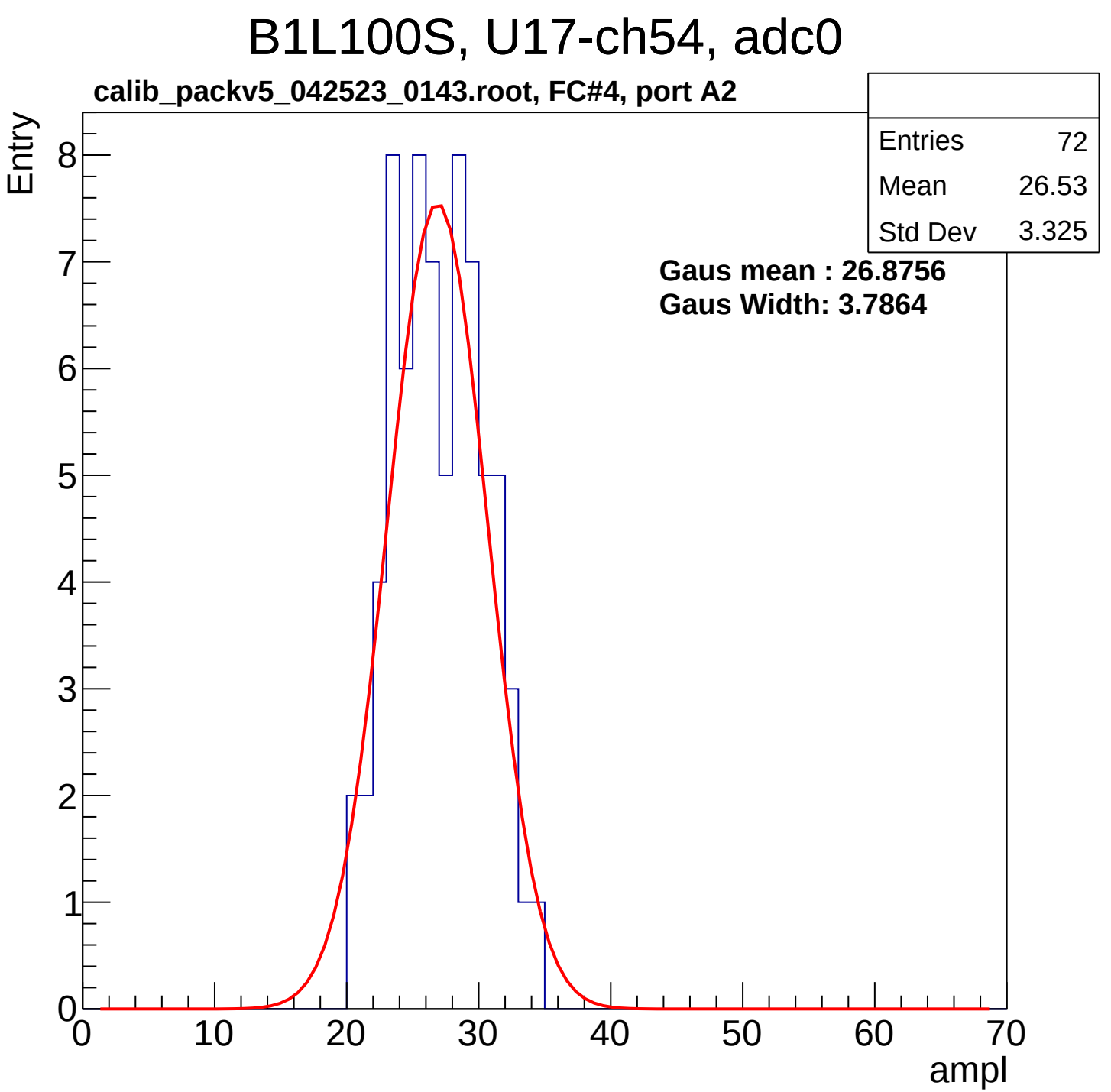
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch53, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 5
Mean 61.2
Std Dev 1.833
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L100S, U17-ch53, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch54, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 26.53
Std Dev 3.325
Gaus mean : 26.8756
Gaus Width: 3.7864
Entry
ampl
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1
2
3
4
5
6
7
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0
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40
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60
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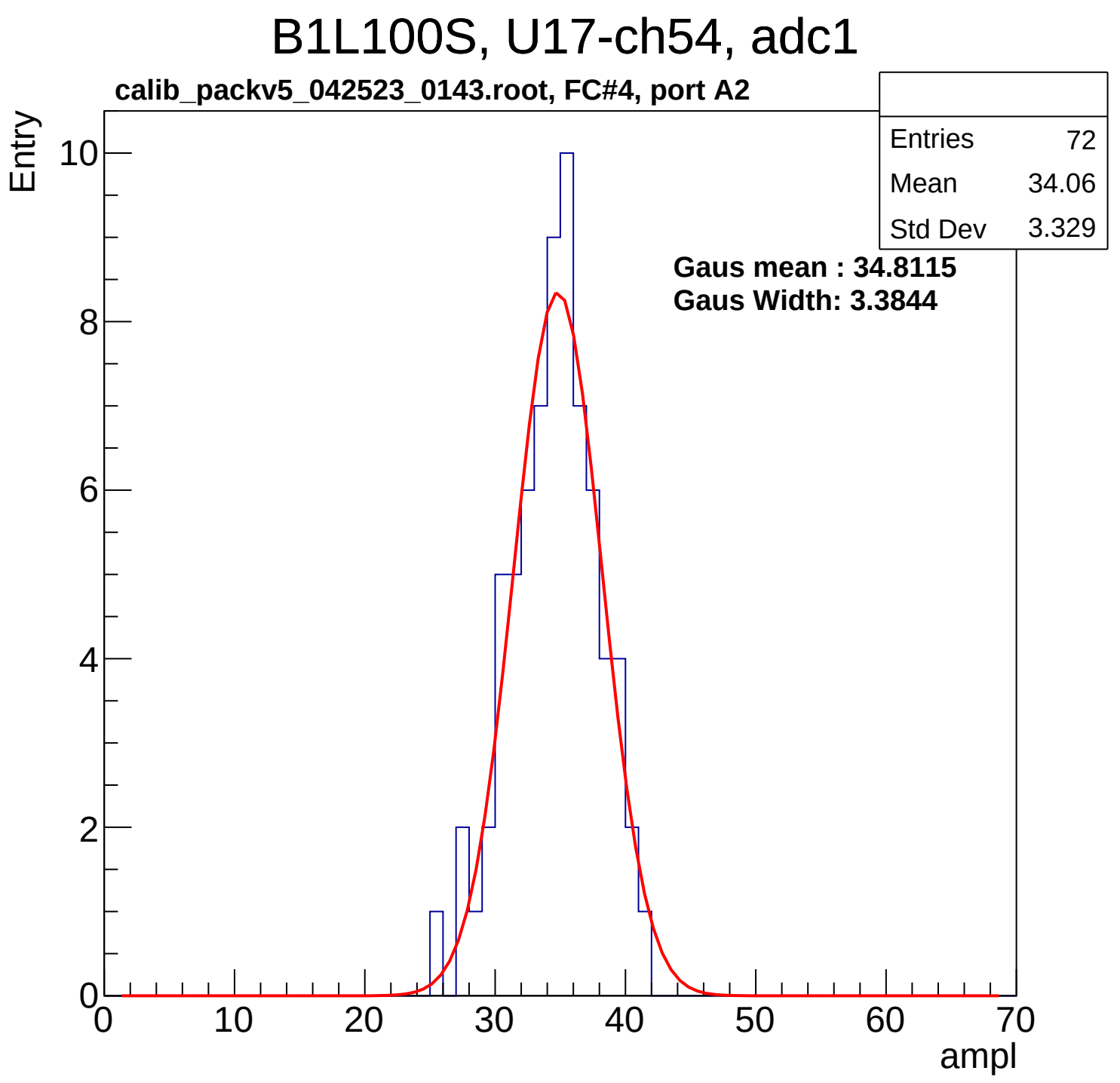
B1L100S, U17-ch54, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 34.06
Std Dev 3.329
Gaus mean : 34.8115
Gaus Width: 3.3844
Entry
ampl
0
2
4
6
8
10
0
10
20
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40
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60
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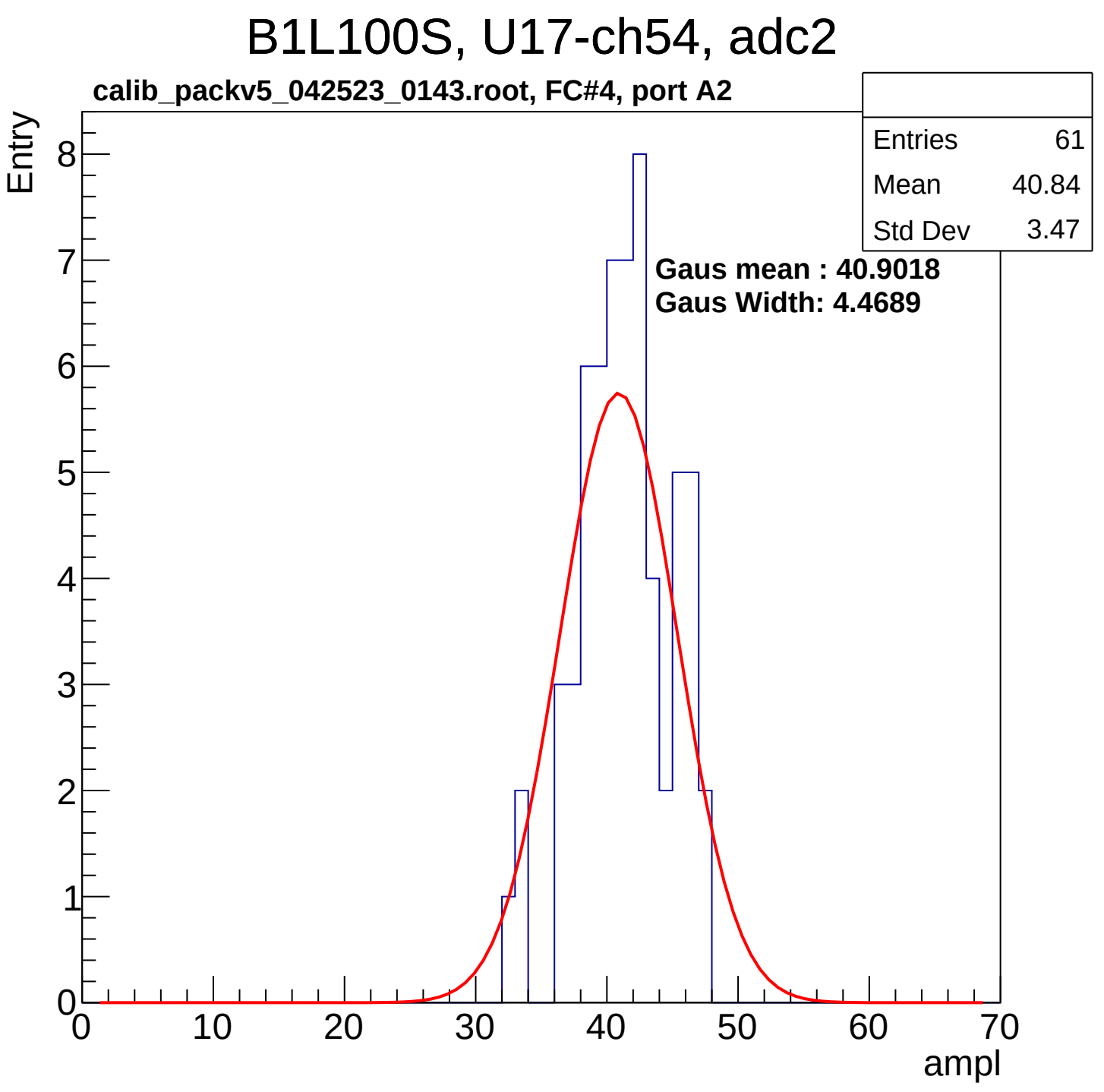
B1L100S, U17-ch54, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 40.84
Std Dev 3.47
Gaus mean : 40.9018
Gaus Width: 4.4689
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
30
40
50
60
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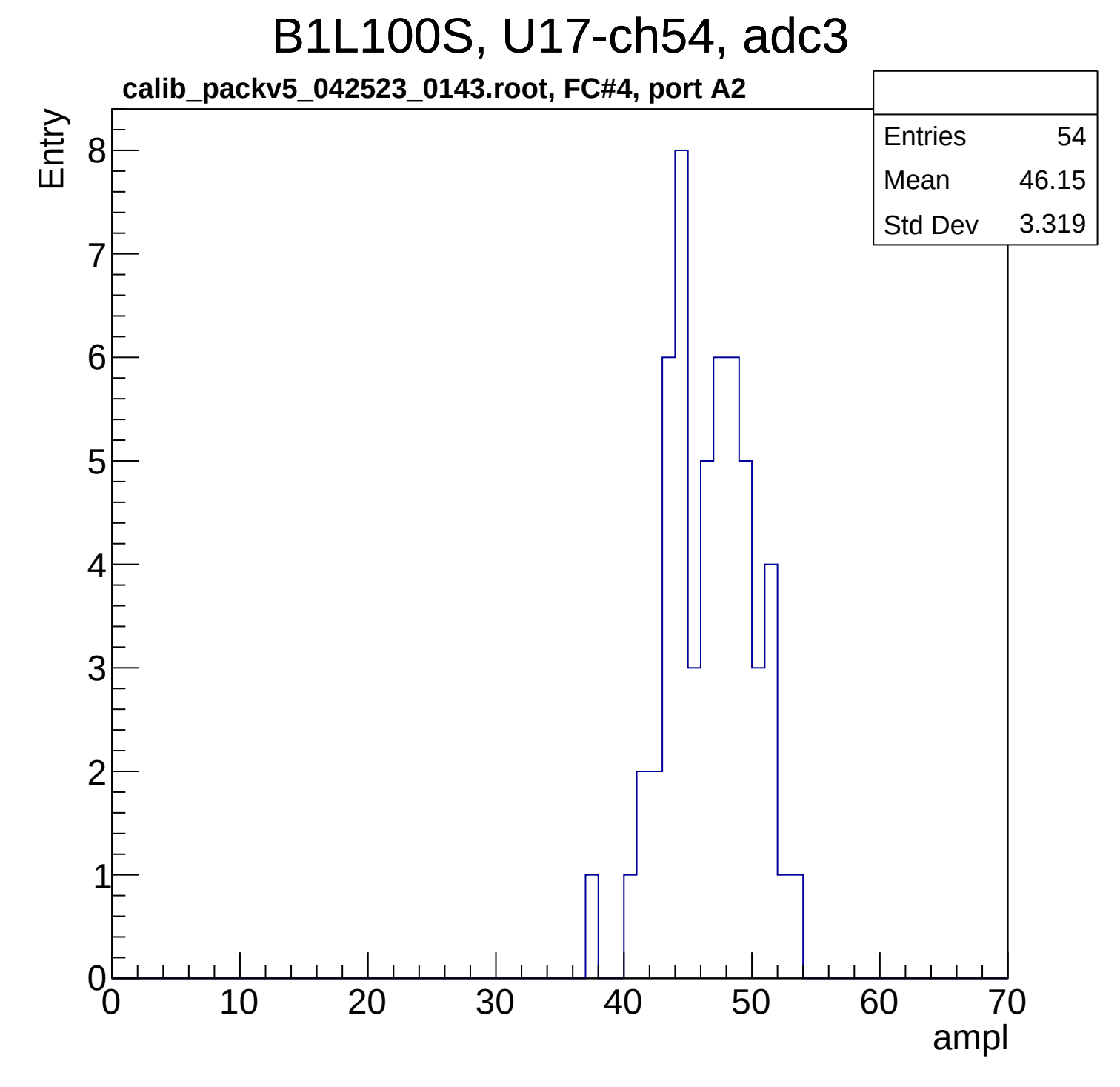
B1L100S, U17-ch54, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 46.15
Std Dev 3.319
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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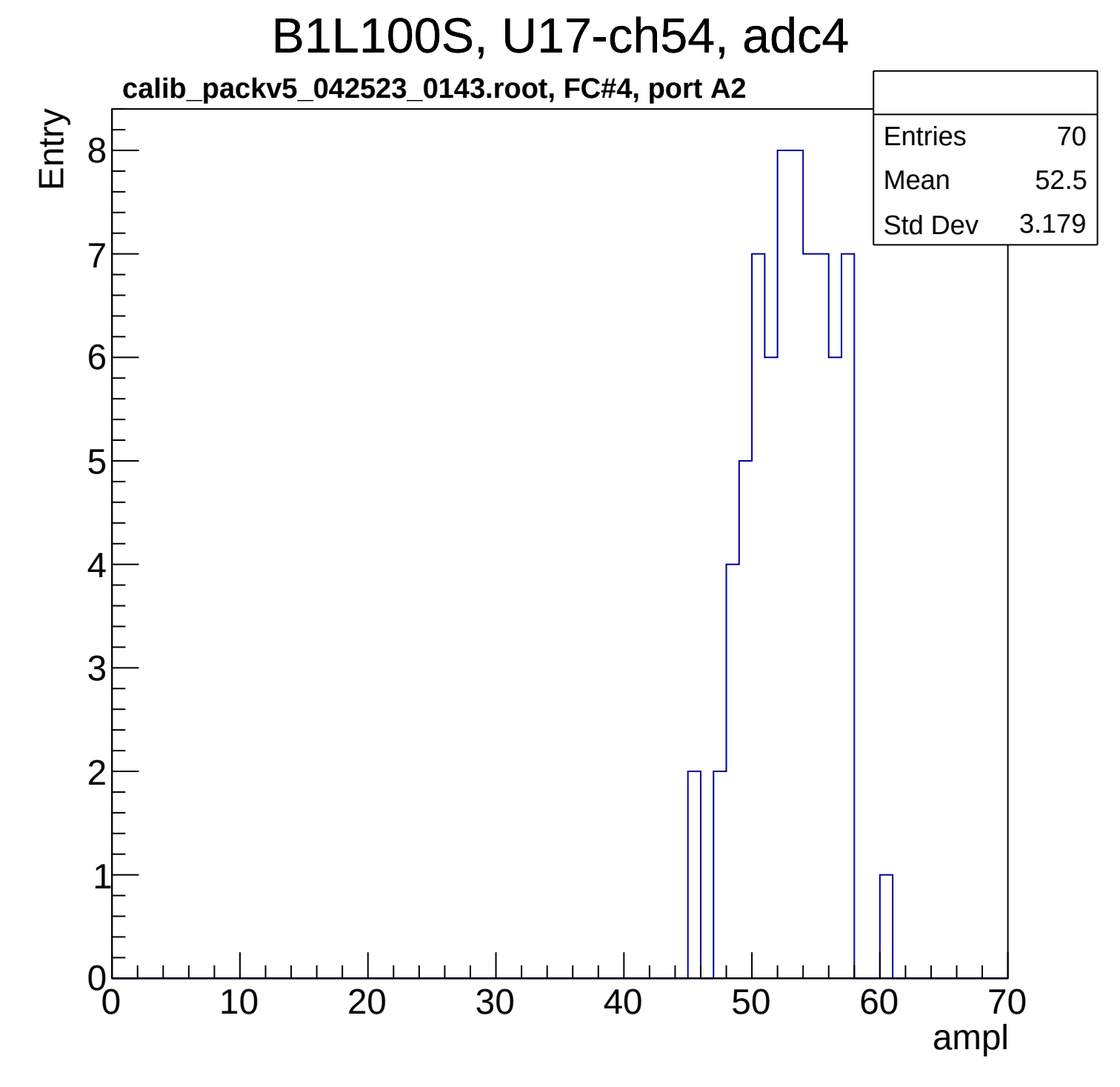
B1L100S, U17-ch54, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 52.5
Std Dev 3.179
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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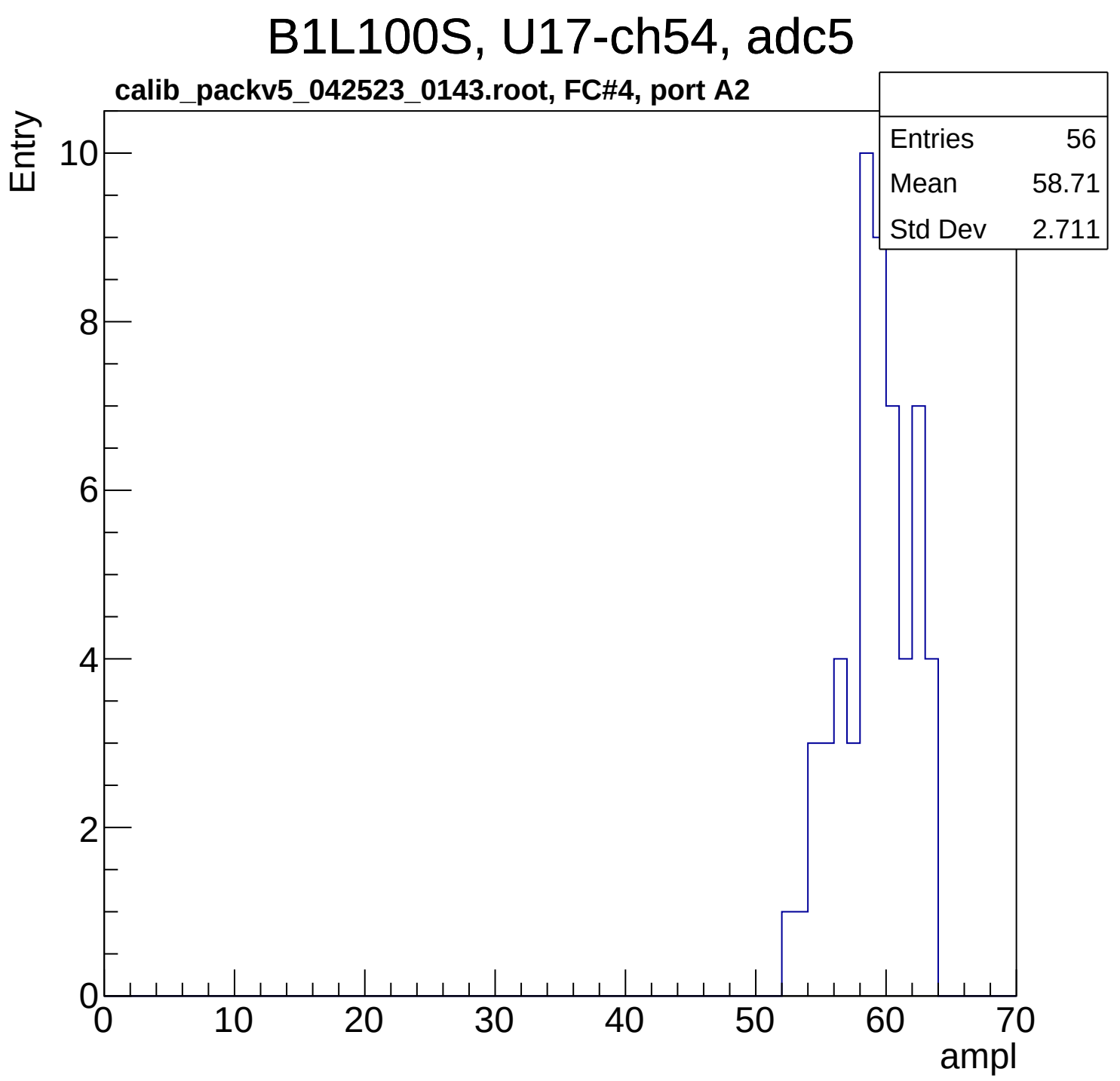
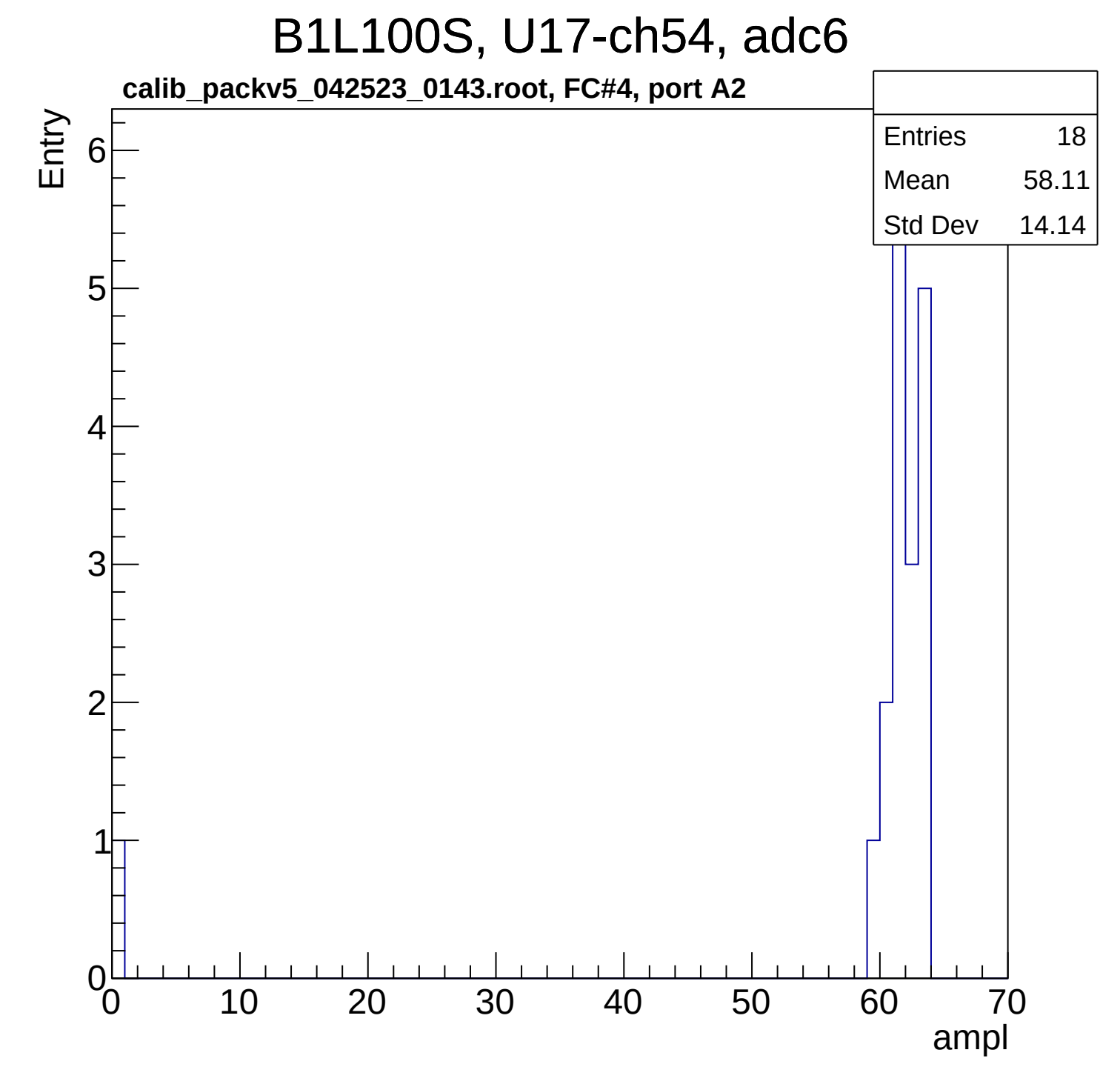
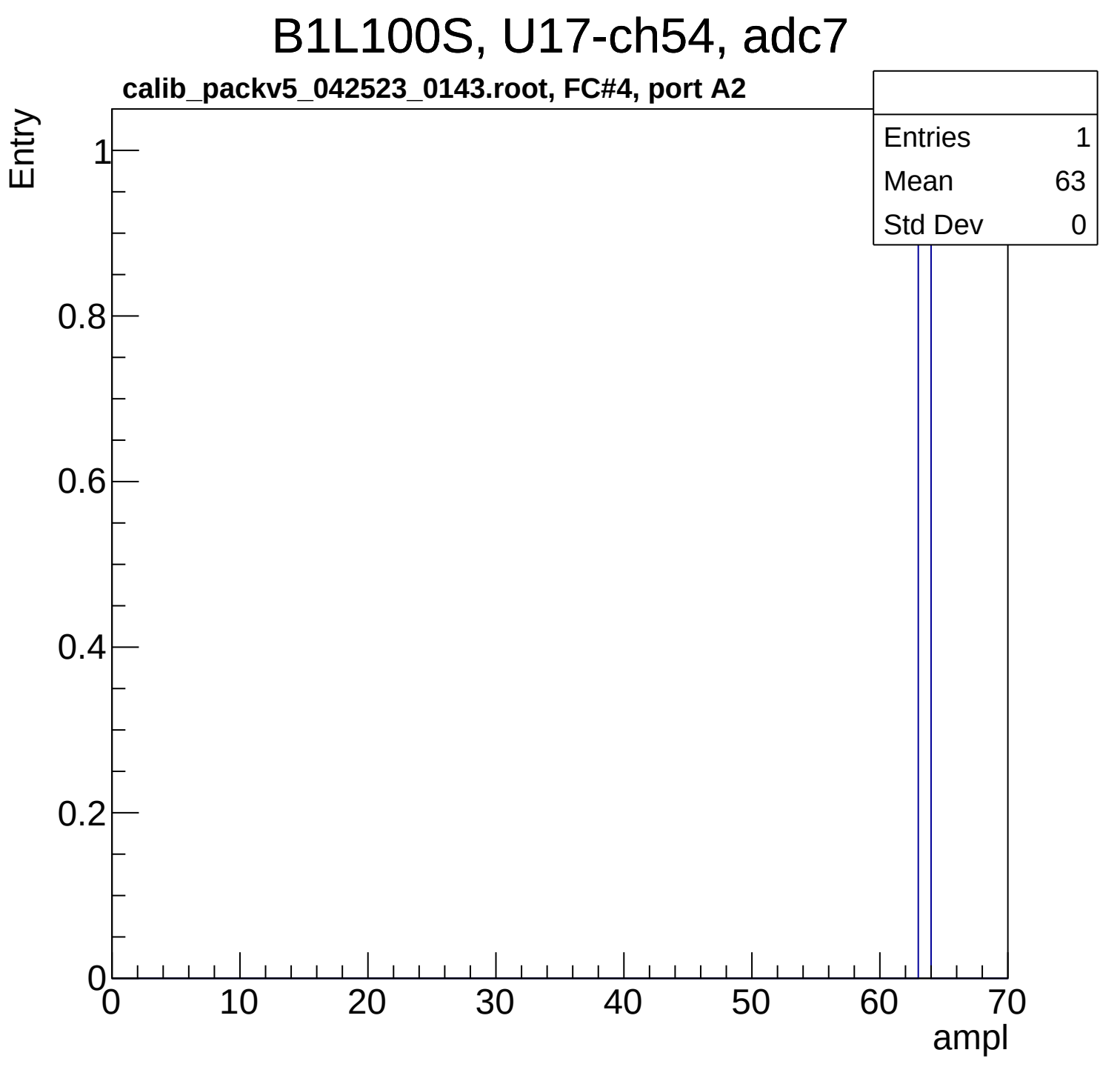
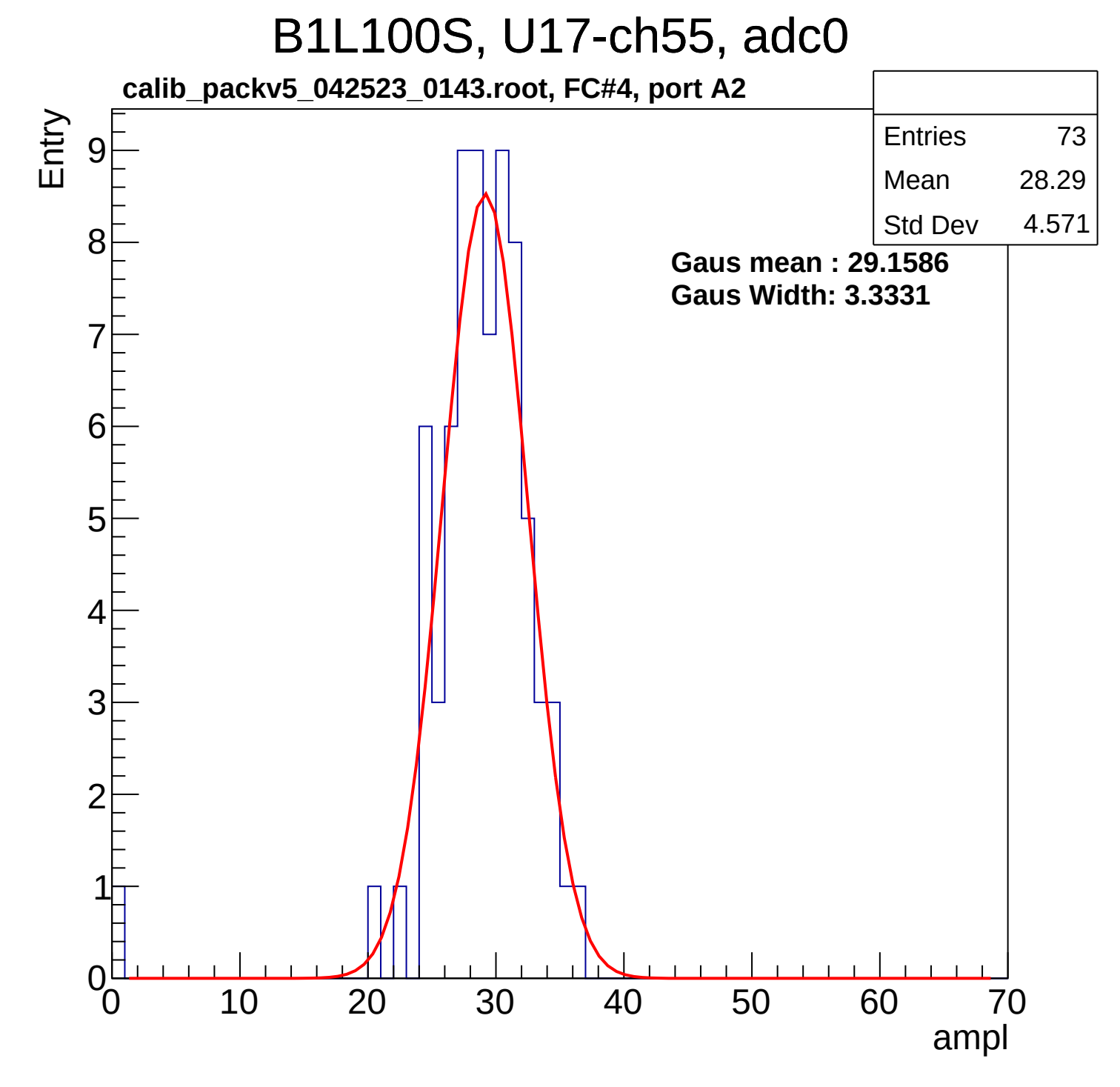
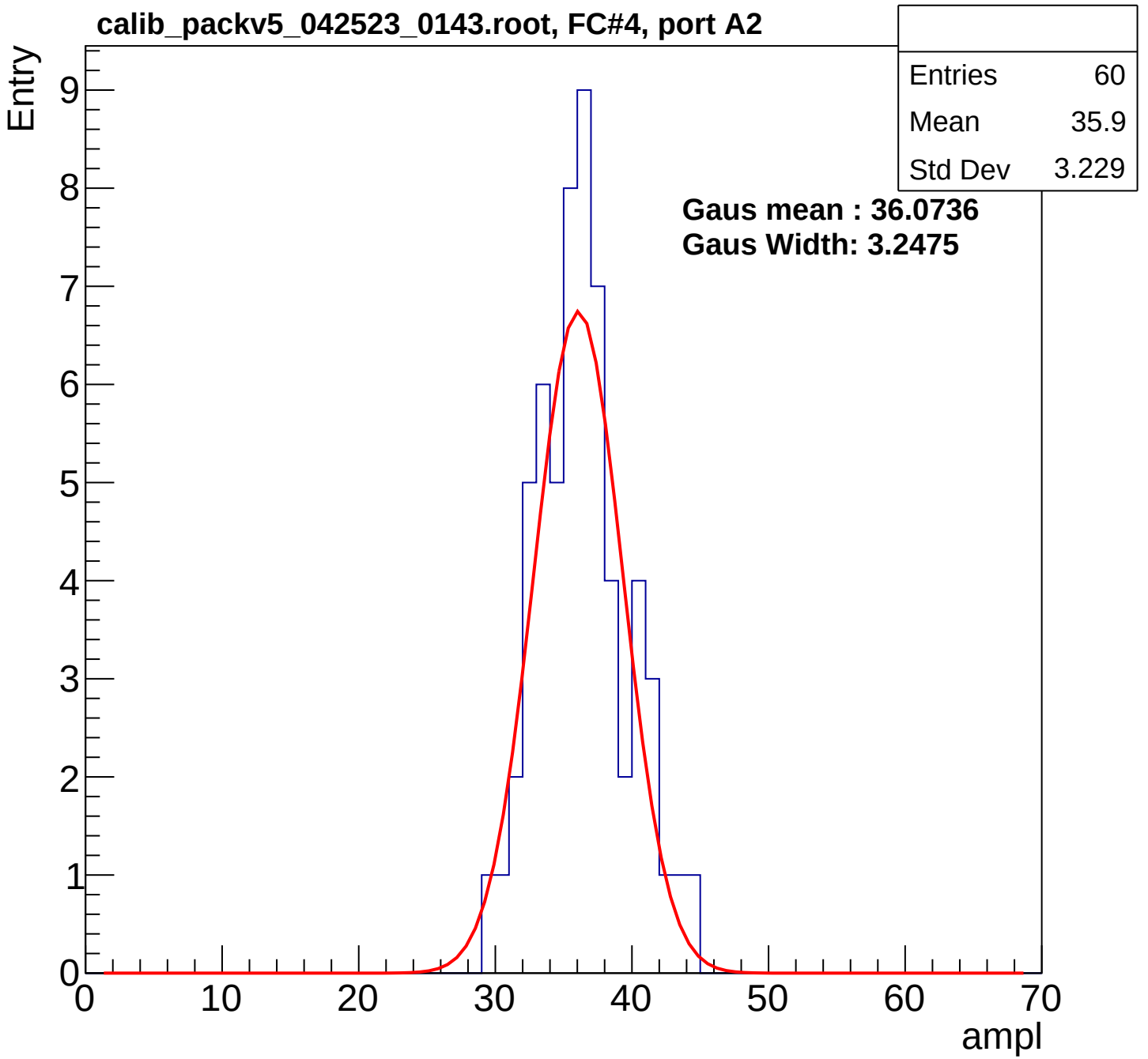
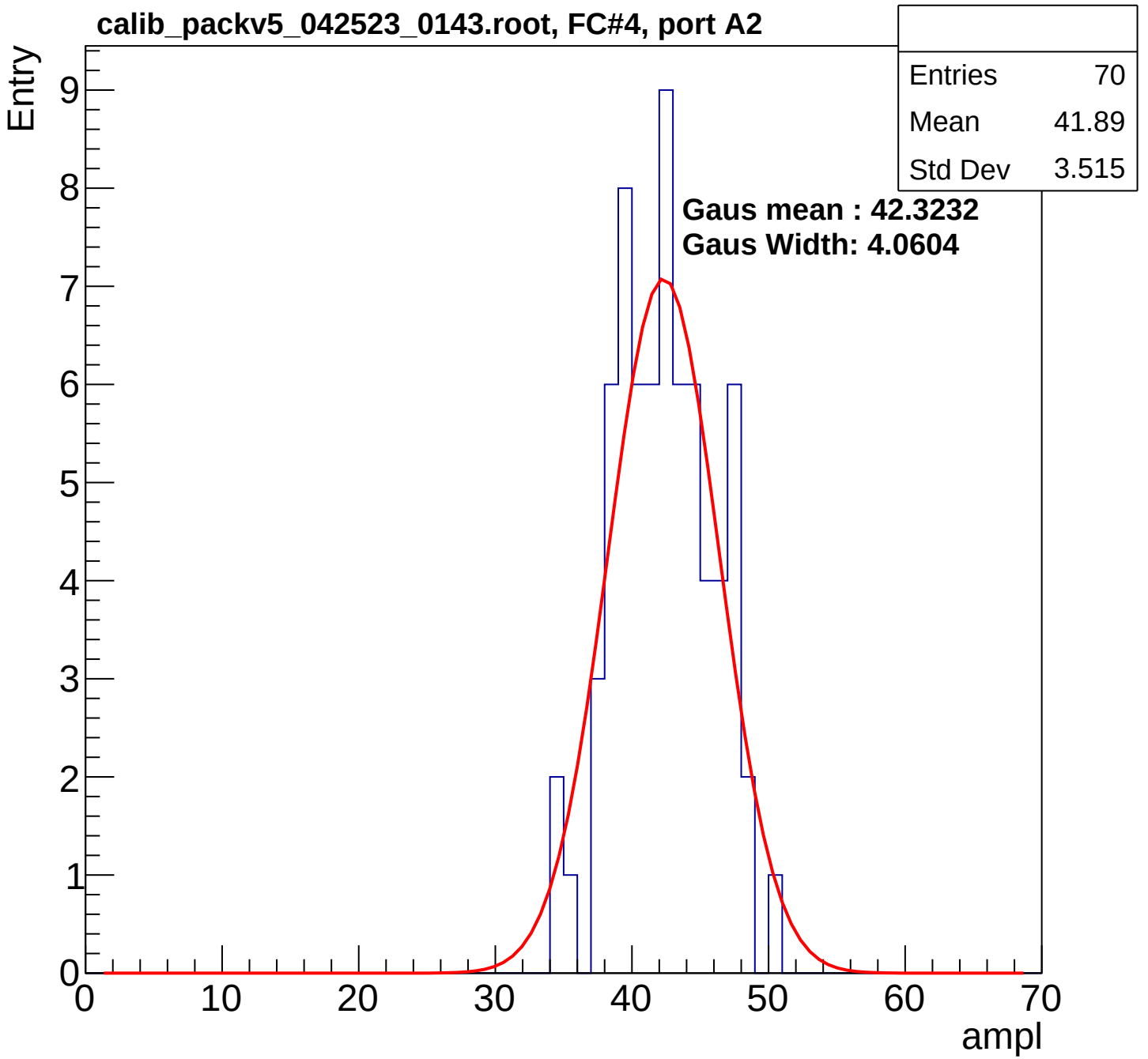

B1L100S, U17-ch54, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 58.71
Std Dev 2.711
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

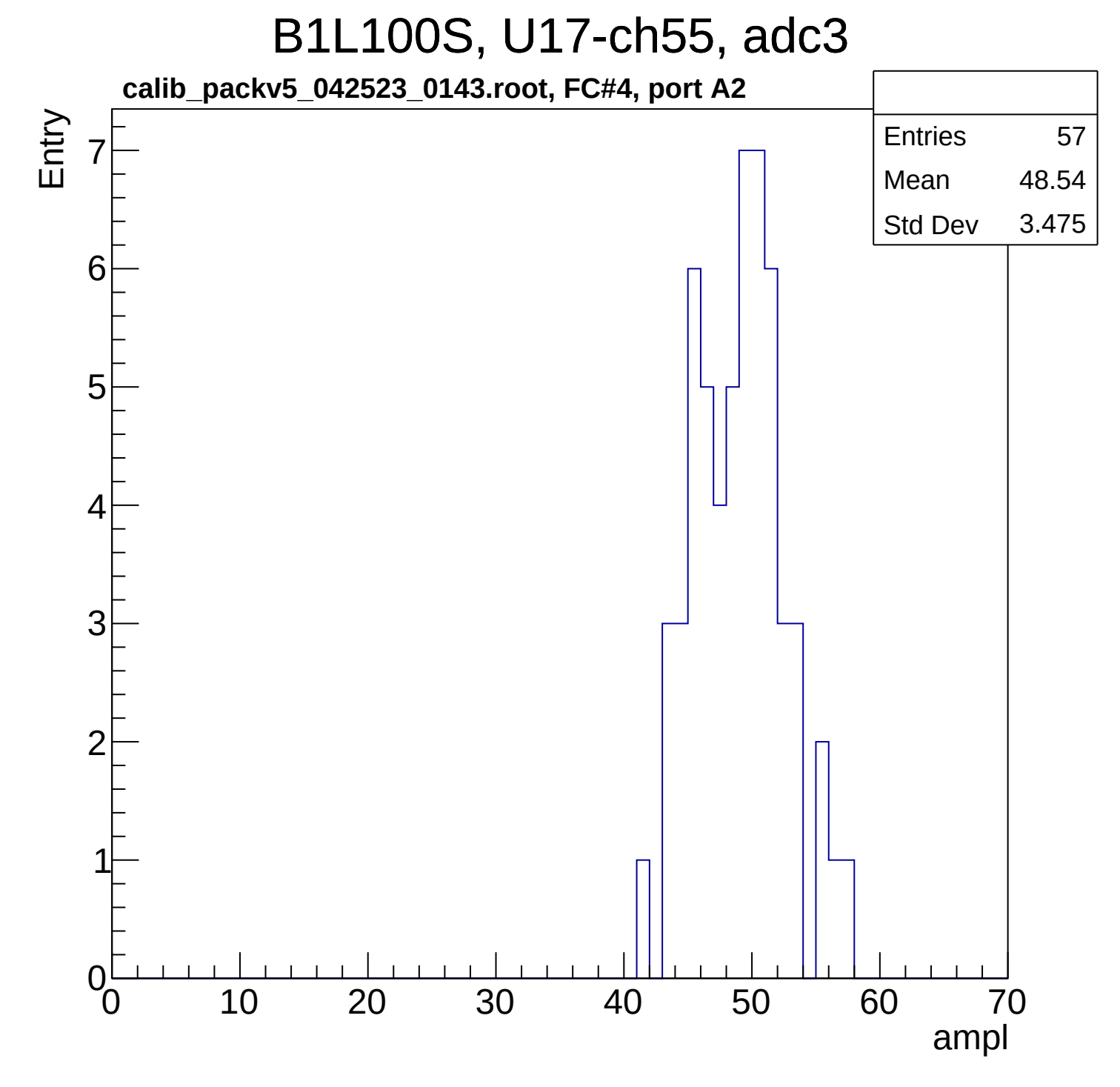

B1L100S, U17-ch54, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 18
Mean 58.11
Std Dev 14.14
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

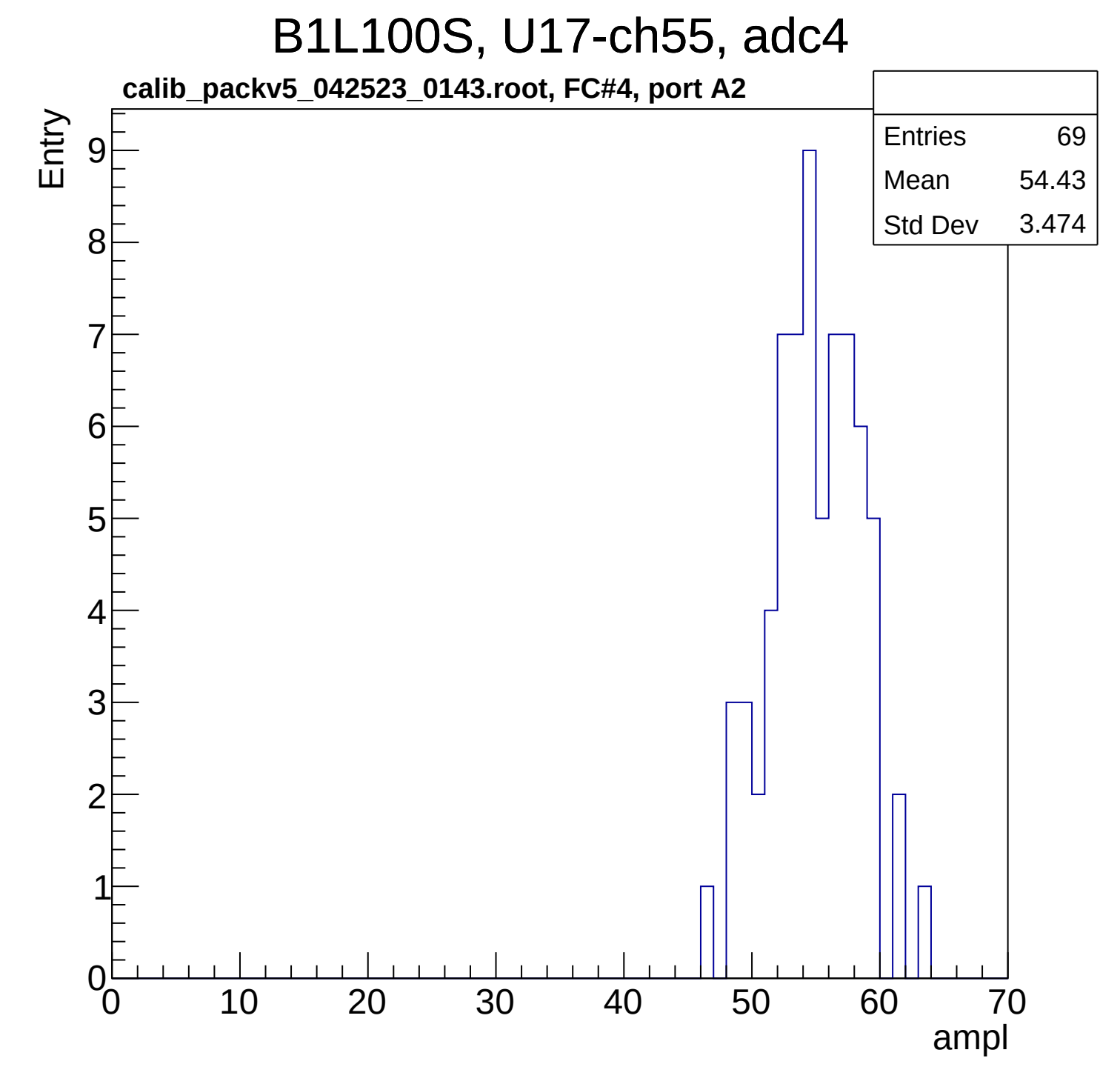

B1L100S, U17-ch54, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

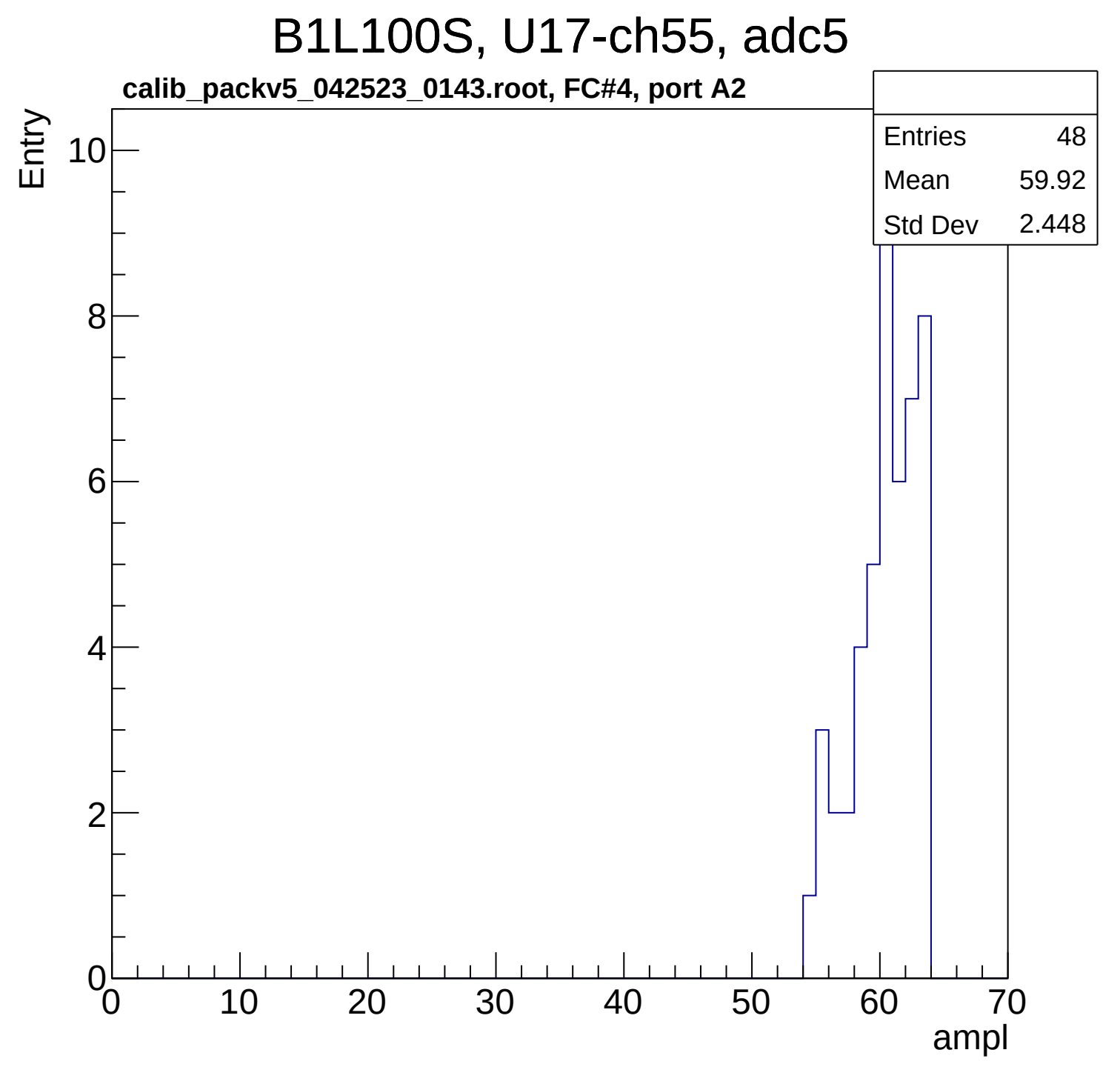

B1L100S, U17-ch55, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 28.29
Std Dev 4.571
Gaus mean : 29.1586
Gaus Width: 3.3331
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

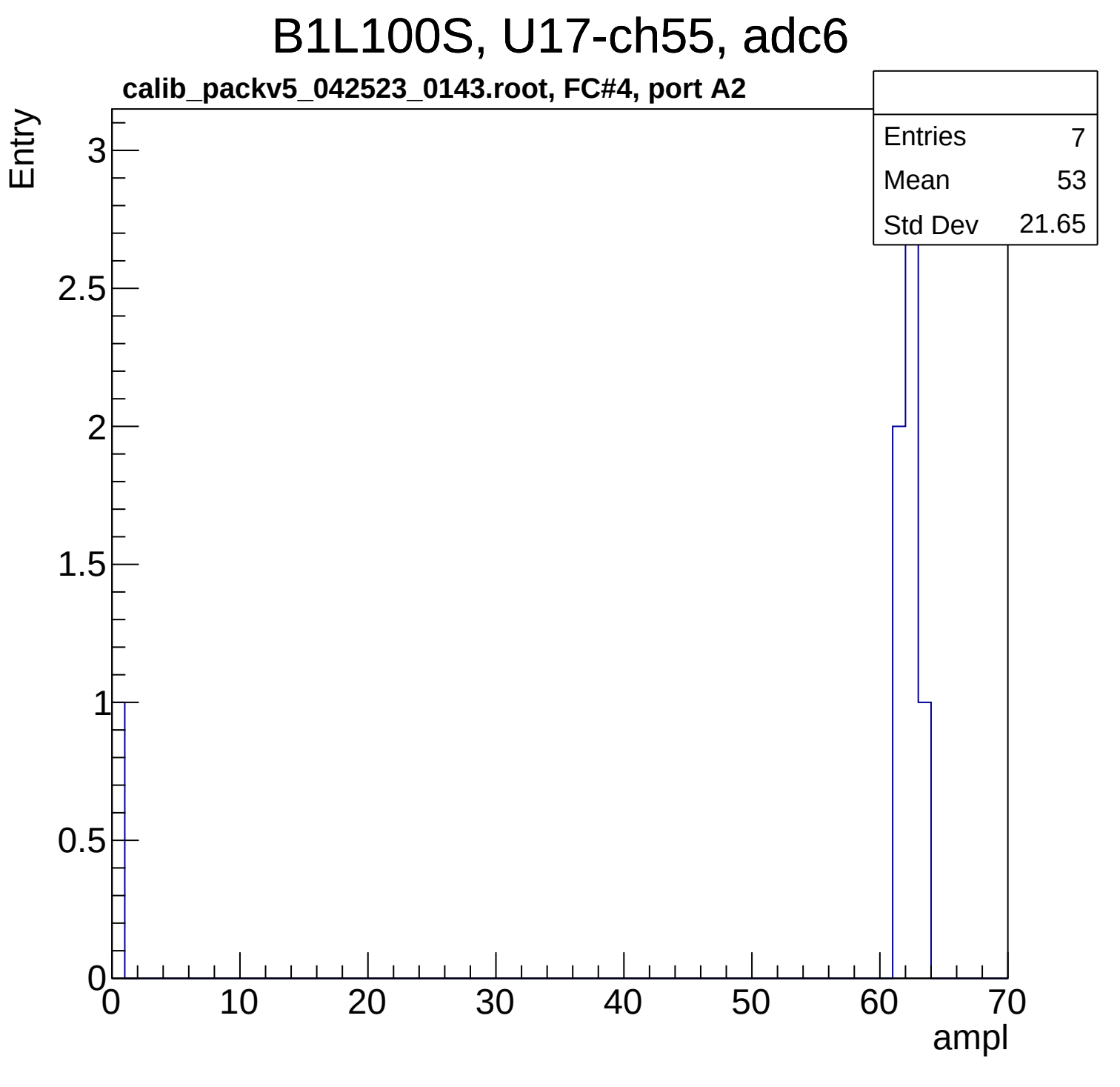

B1L100S, U17-ch55, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 35.9
Std Dev 3.229
Gaus mean : 36.0736
Gaus Width: 3.2475
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

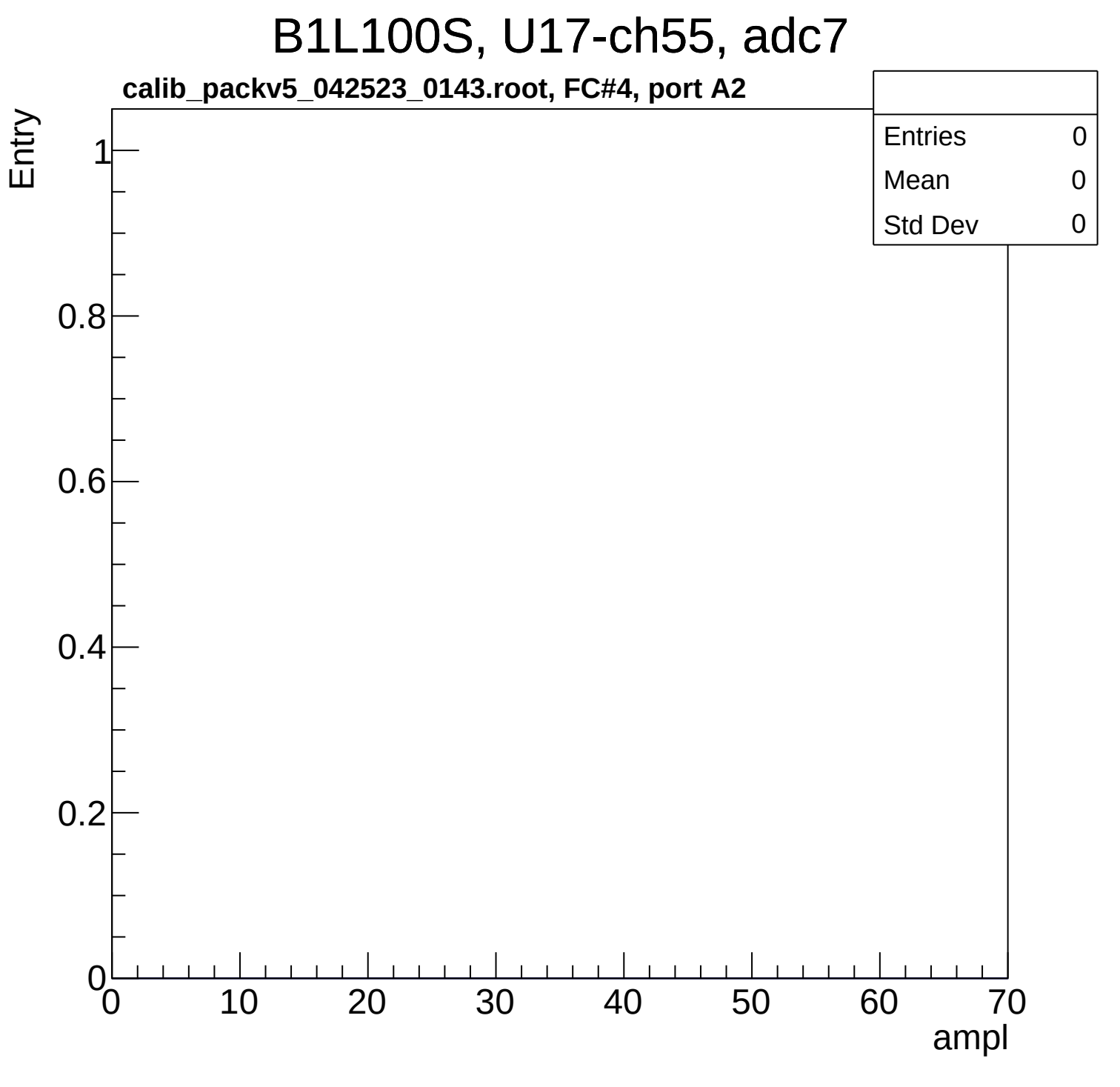

B1L100S, U17-ch55, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 41.89
Std Dev 3.515
Gaus mean : 42.3232
Gaus Width: 4.0604
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

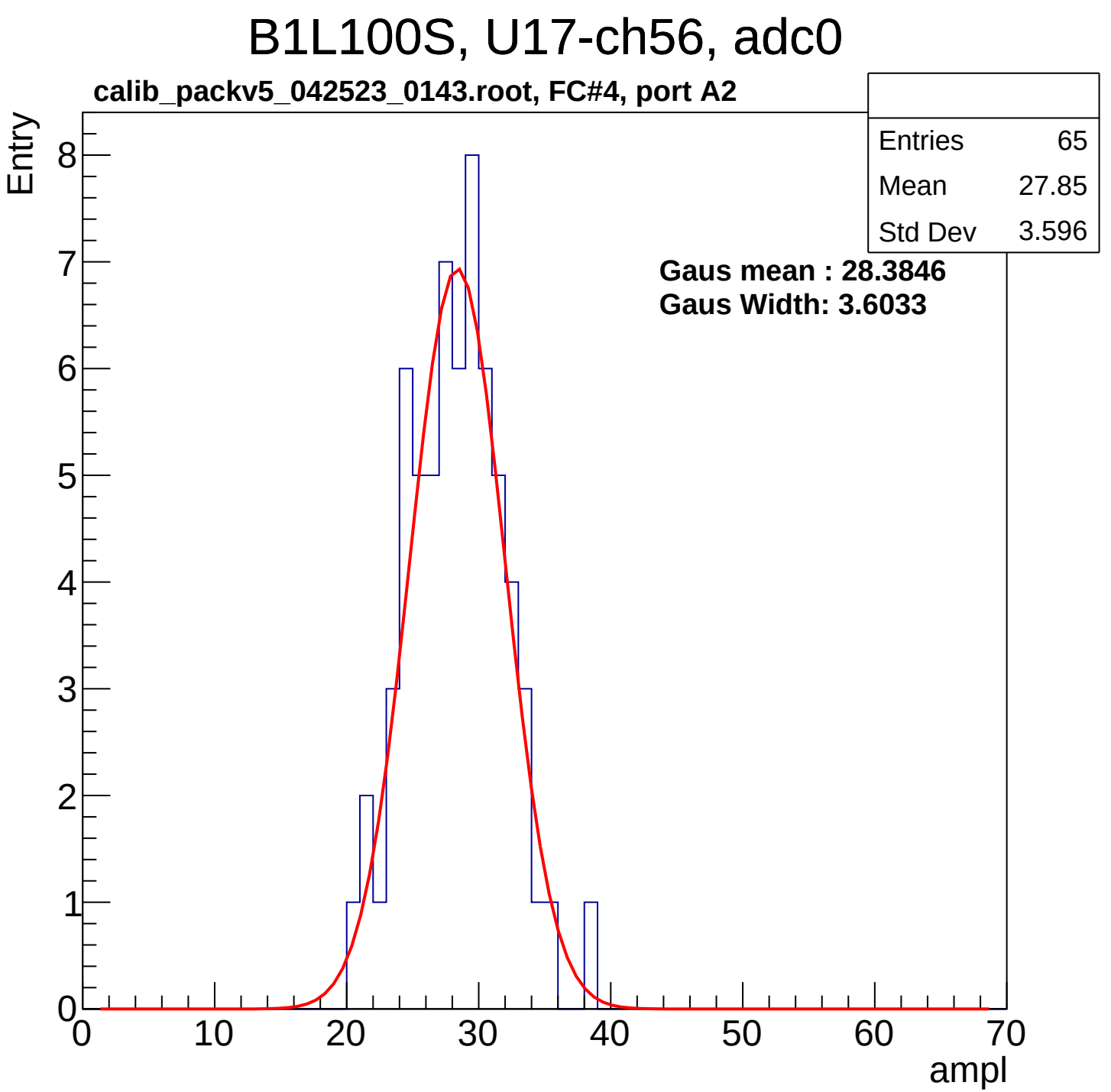

B1L100S, U17-ch55, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 48.54
Std Dev 3.475
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

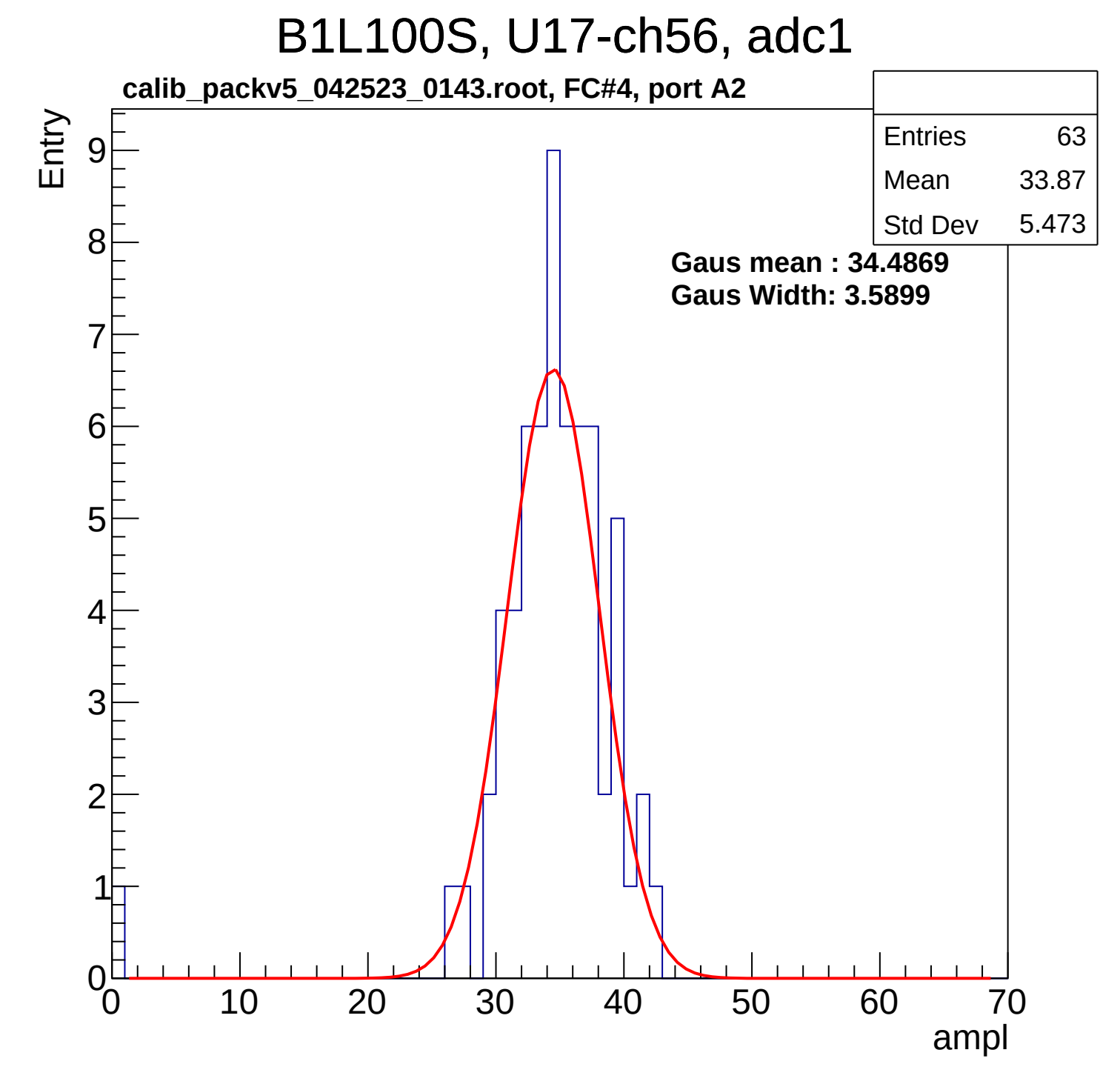

B1L100S, U17-ch55, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 54.43
Std Dev 3.474
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

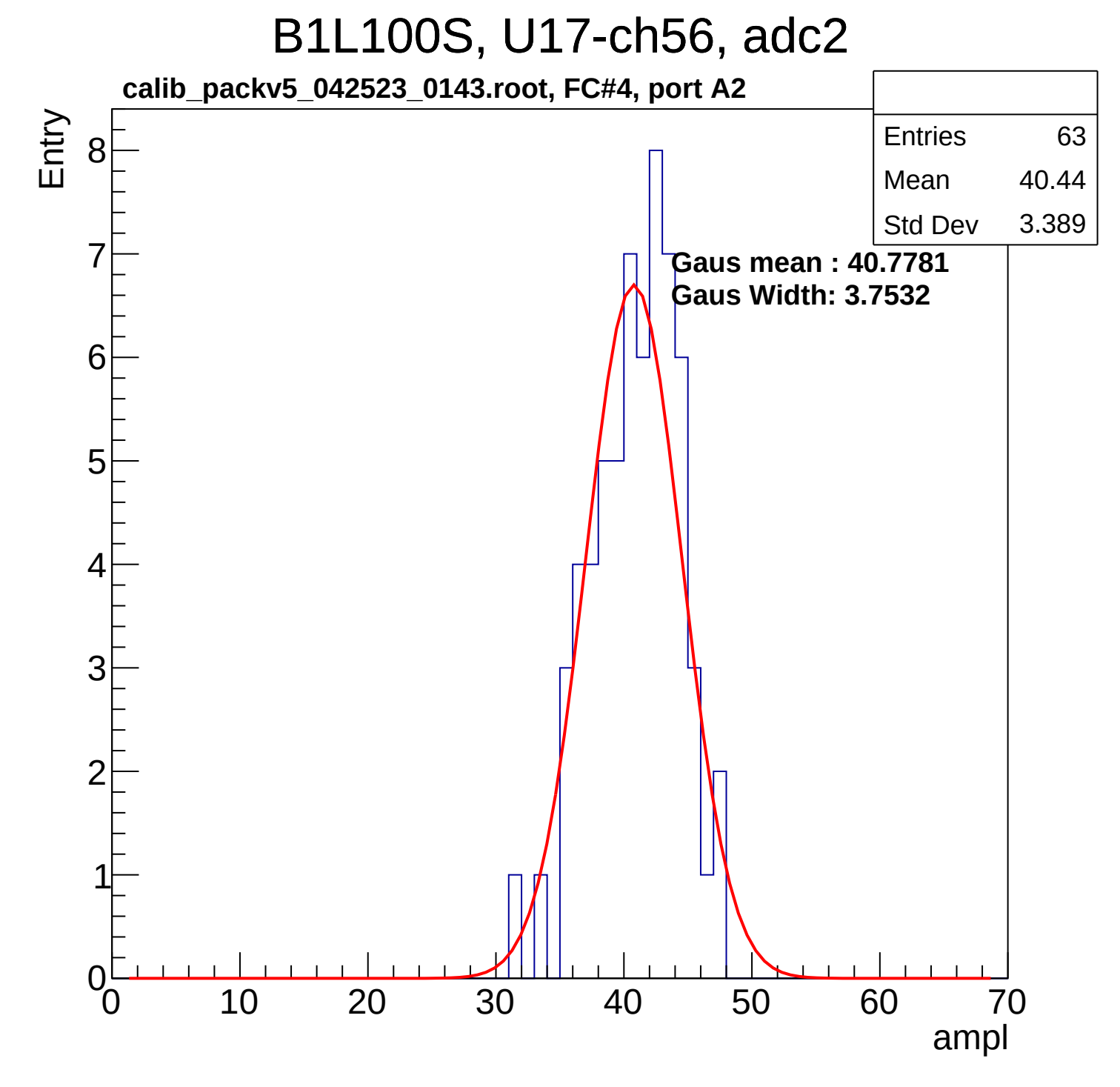

B1L100S, U17-ch55, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 48
Mean 59.92
Std Dev 2.448
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

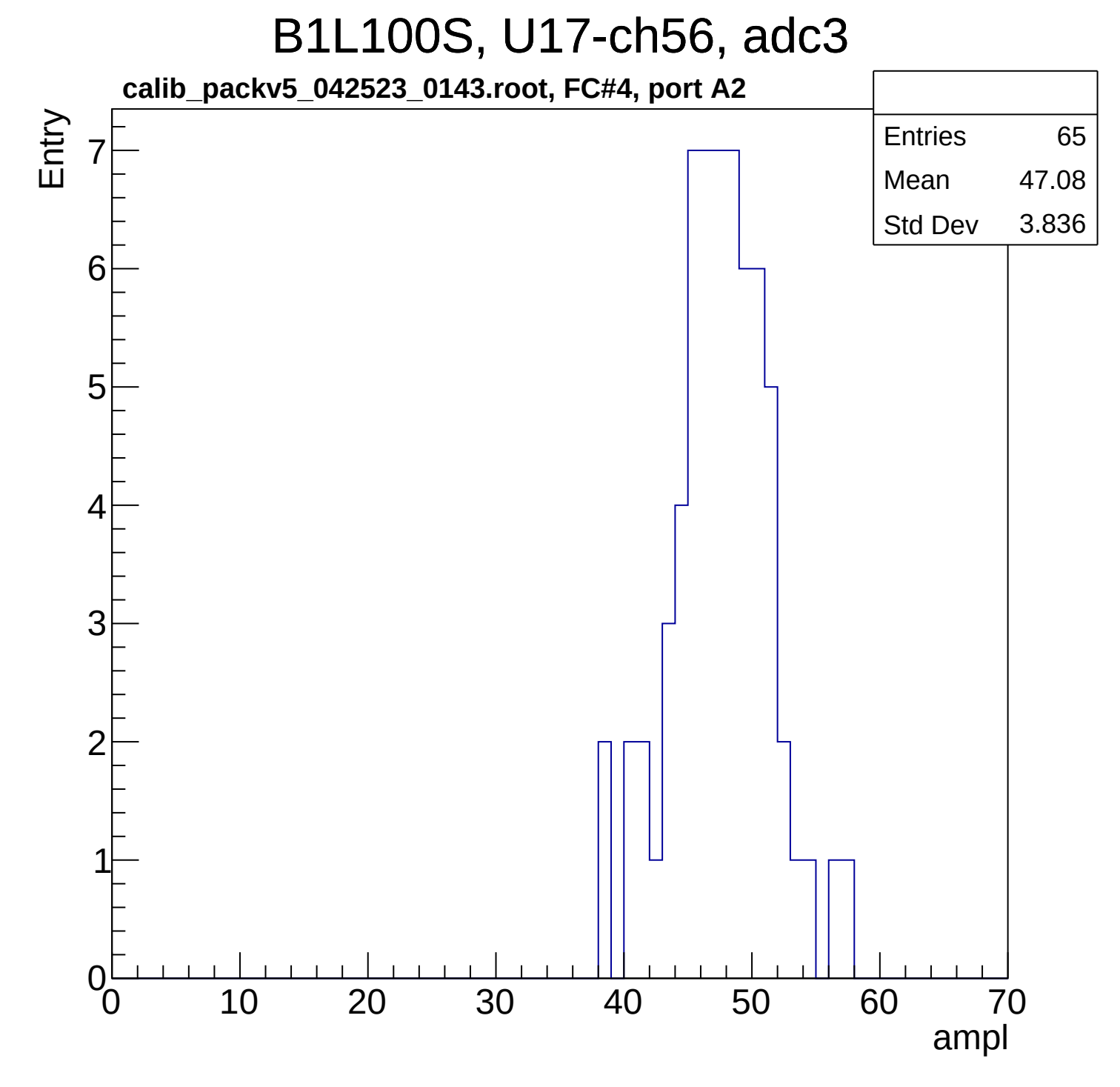

B1L100S, U17-ch55, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 7
Mean 53
Std Dev 21.65
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

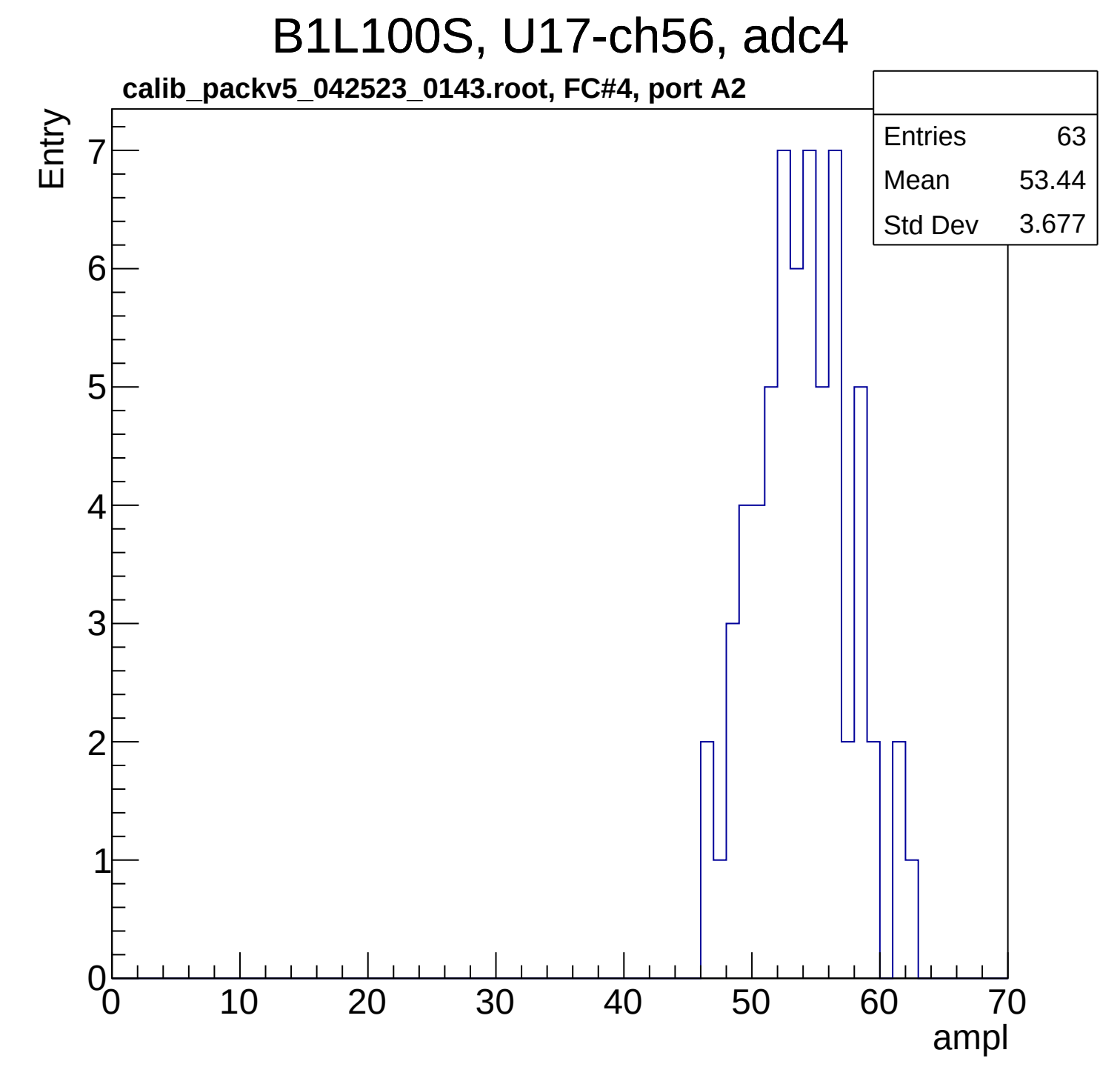

B1L100S, U17-ch55, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

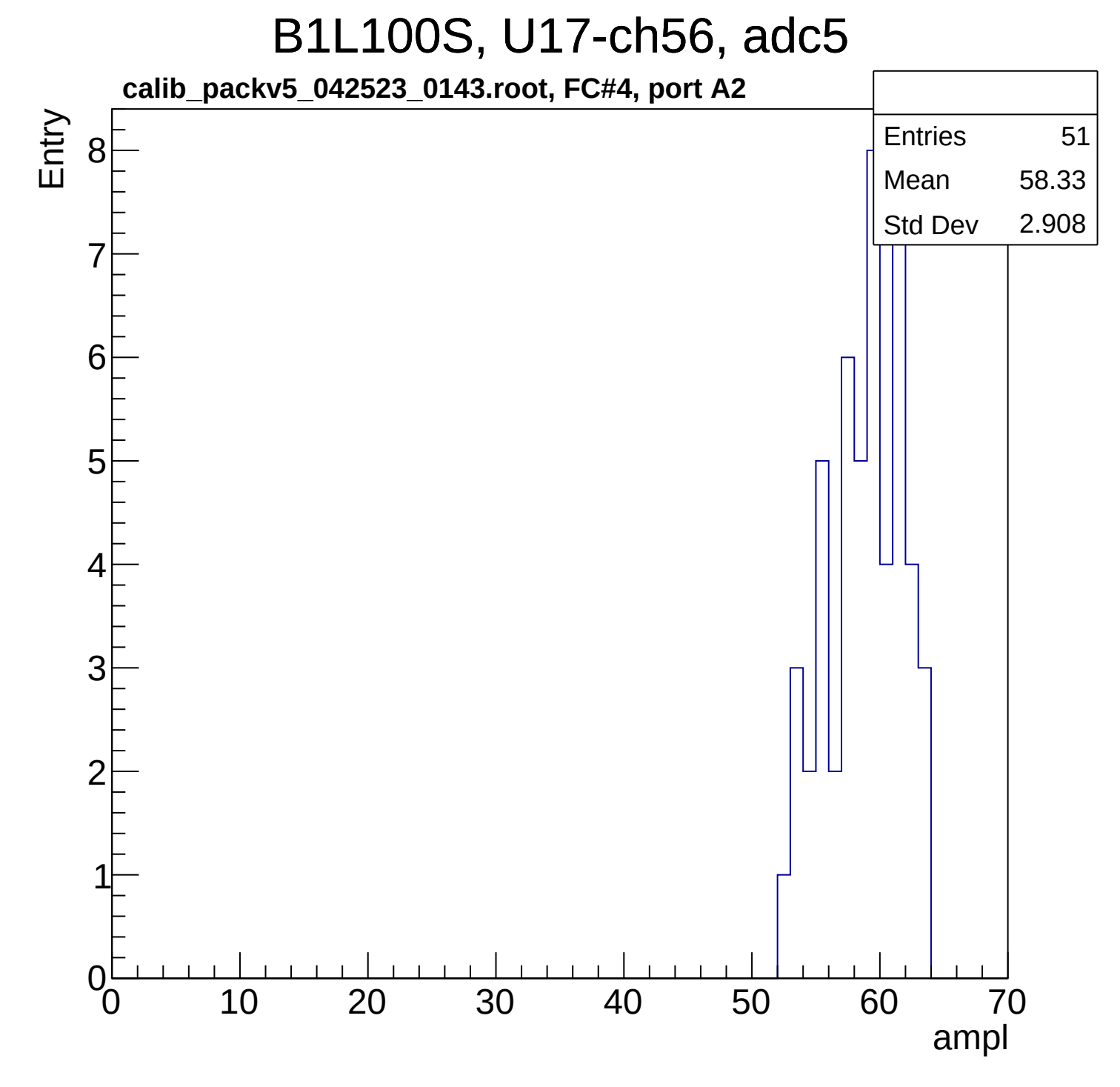

B1L100S, U17-ch56, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 27.85
Std Dev 3.596
Gaus mean : 28.3846
Gaus Width: 3.6033
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch56, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 33.87
Std Dev 5.473
Gaus mean : 34.4869
Gaus Width: 3.5899
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch56, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 40.44
Std Dev 3.389
Gaus mean : 40.7781
Gaus Width: 3.7532
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch56, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 47.08
Std Dev 3.836
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U17-ch56, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 53.44
Std Dev 3.677
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U17-ch56, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 58.33
Std Dev 2.908
Entry
ampl
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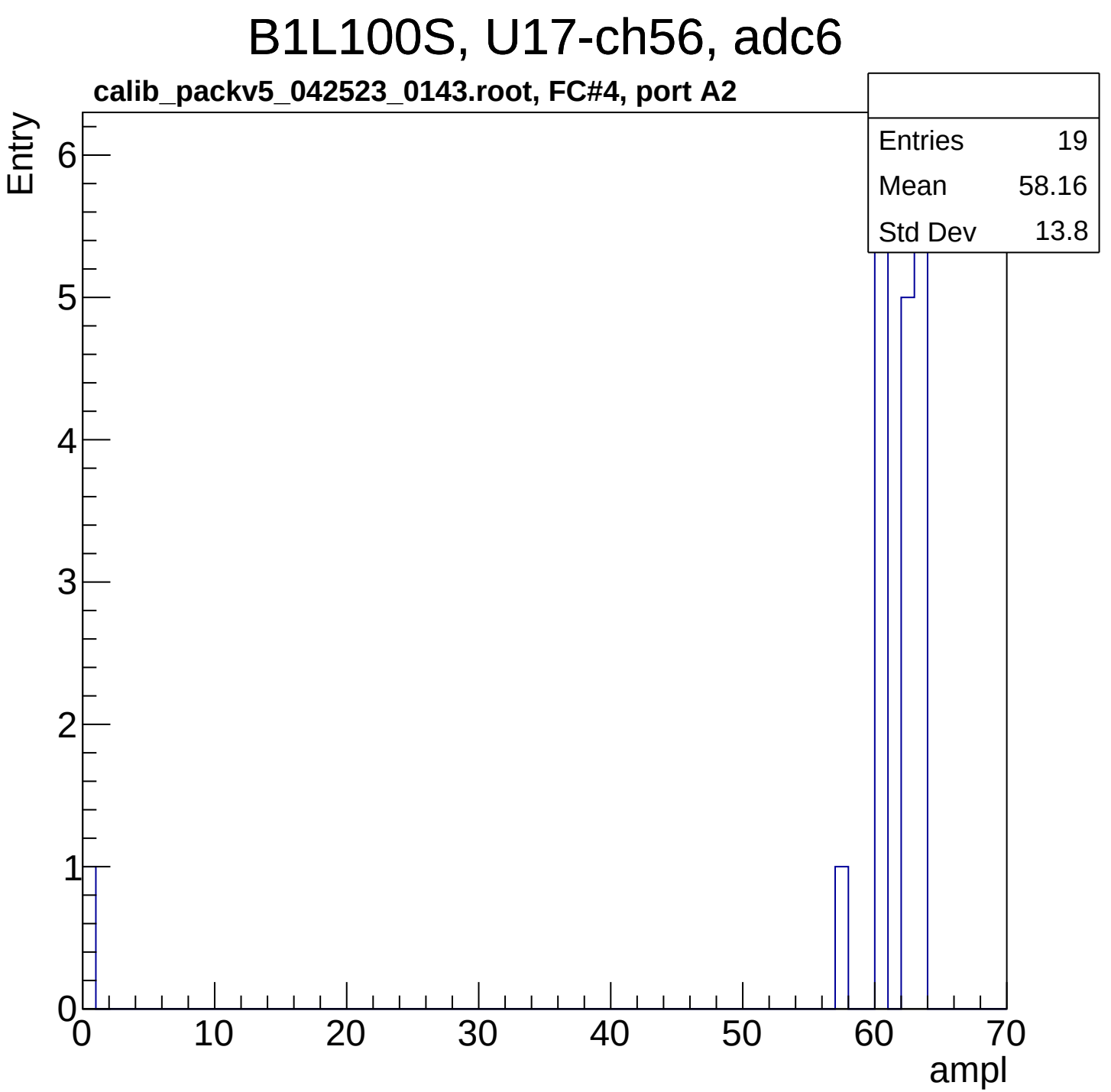
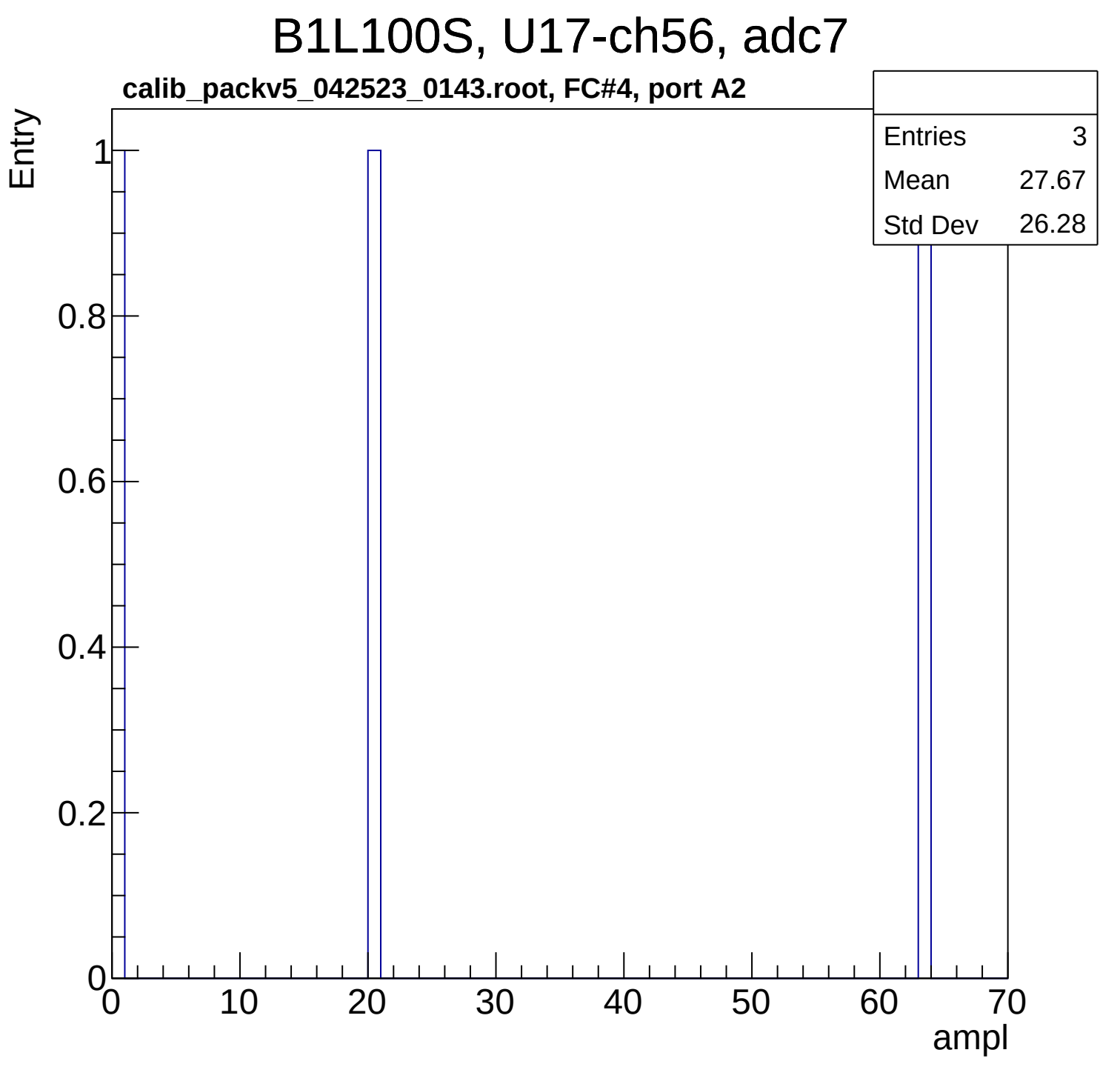
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch56, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 19
Mean 58.16
Std Dev 13.8
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch56, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 27.67
Std Dev 26.28
Entry
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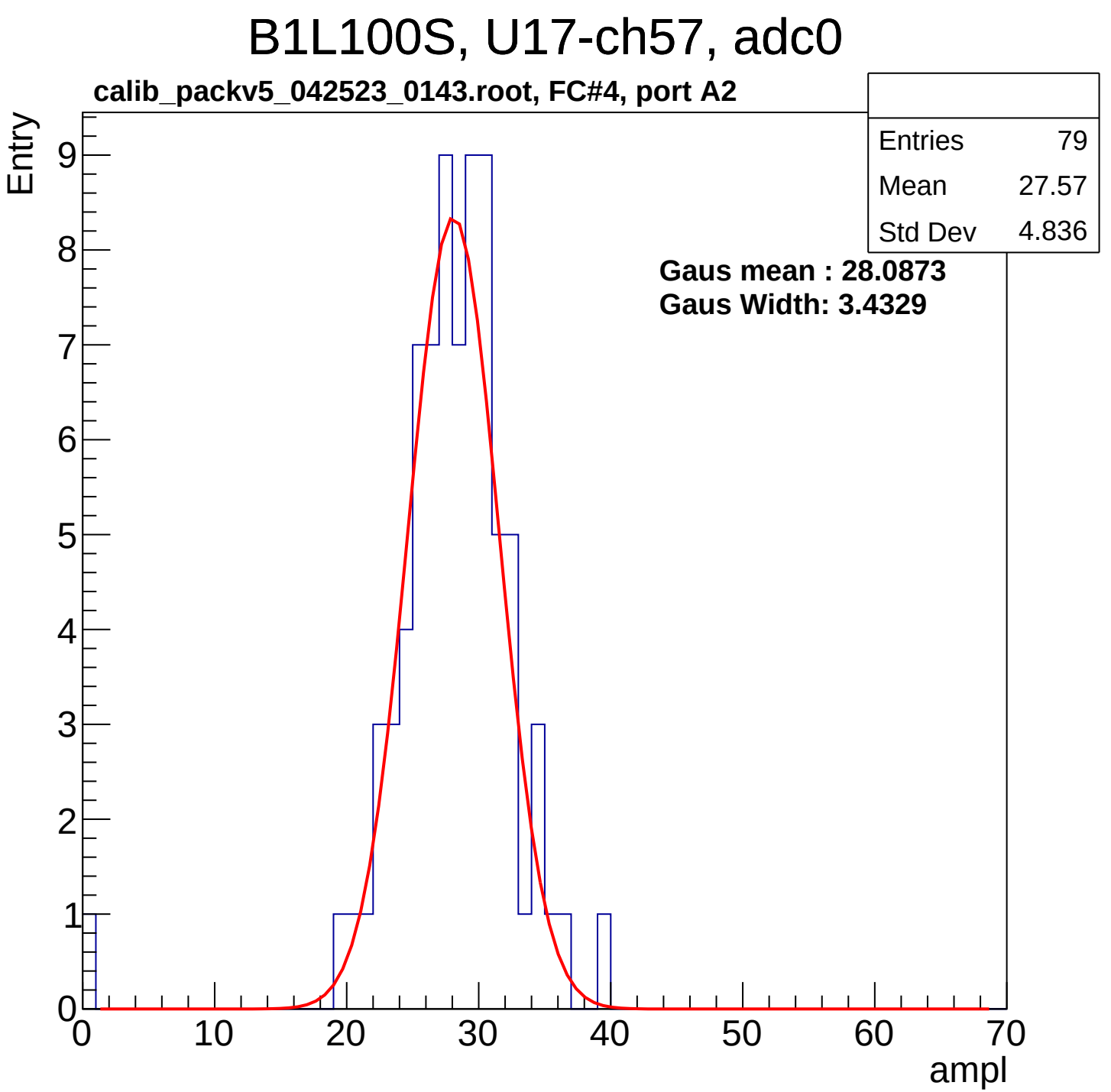
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch57, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 79
Mean 27.57
Std Dev 4.836
Gaus mean : 28.0873
Gaus Width: 3.4329
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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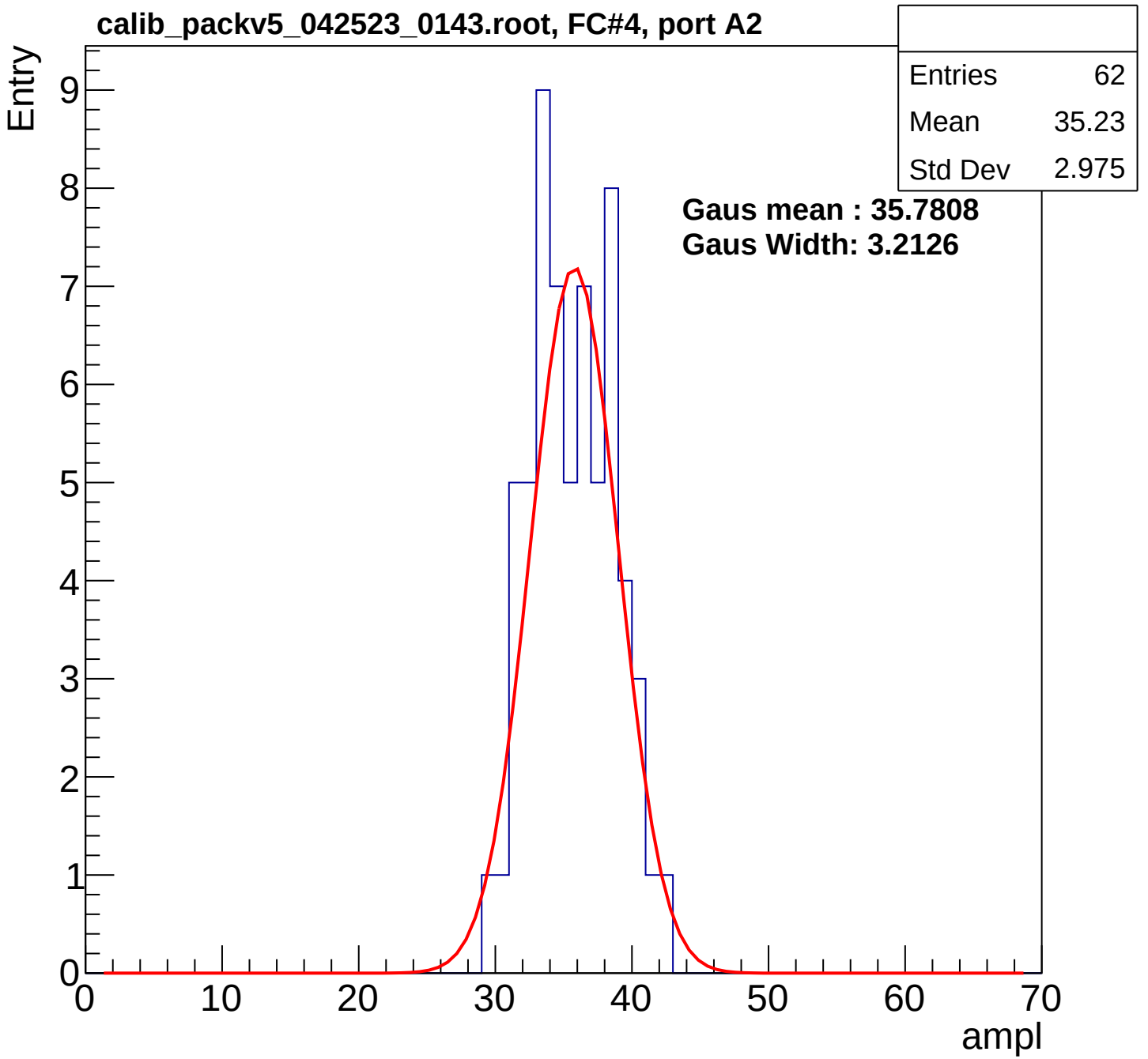
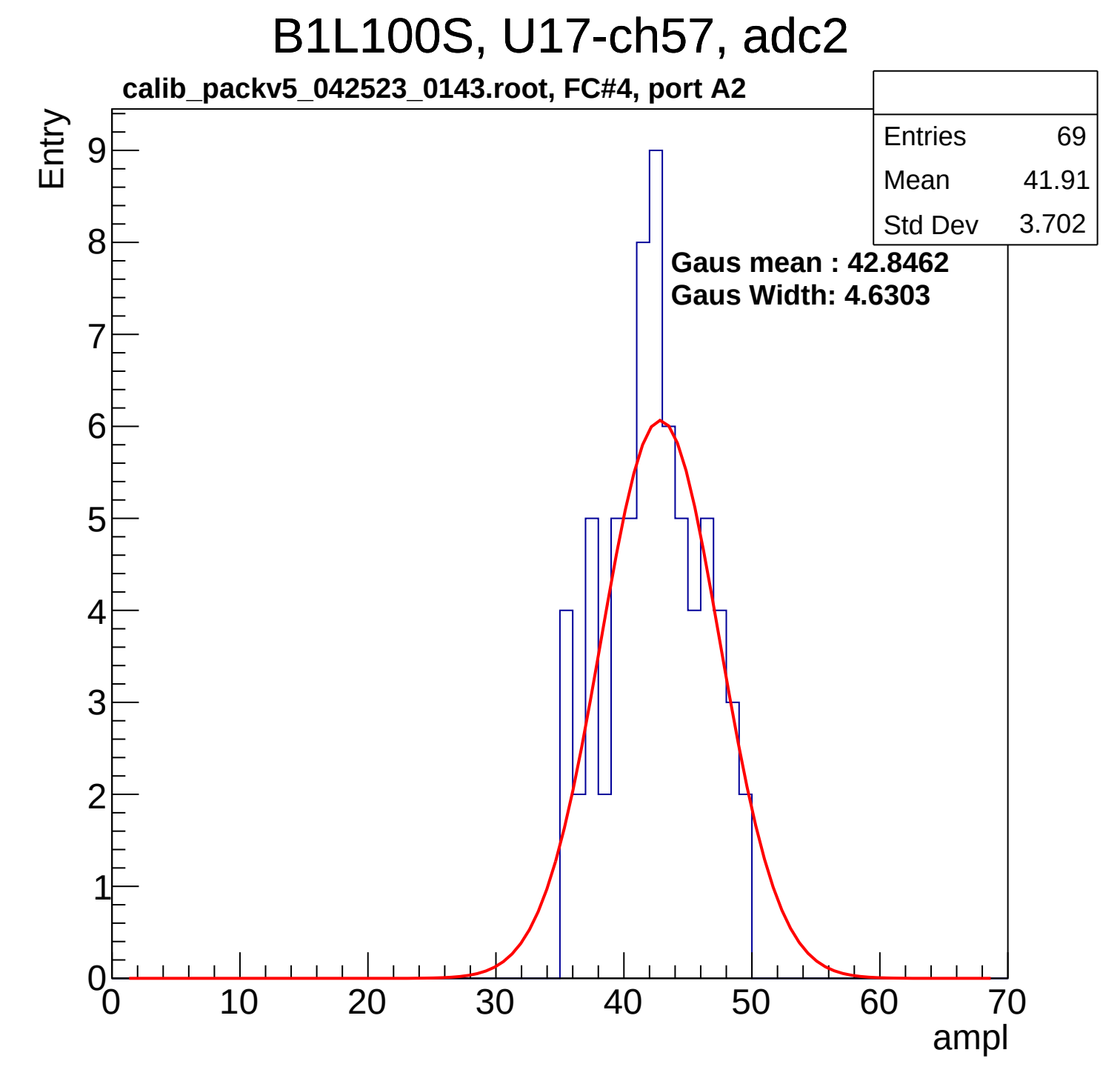
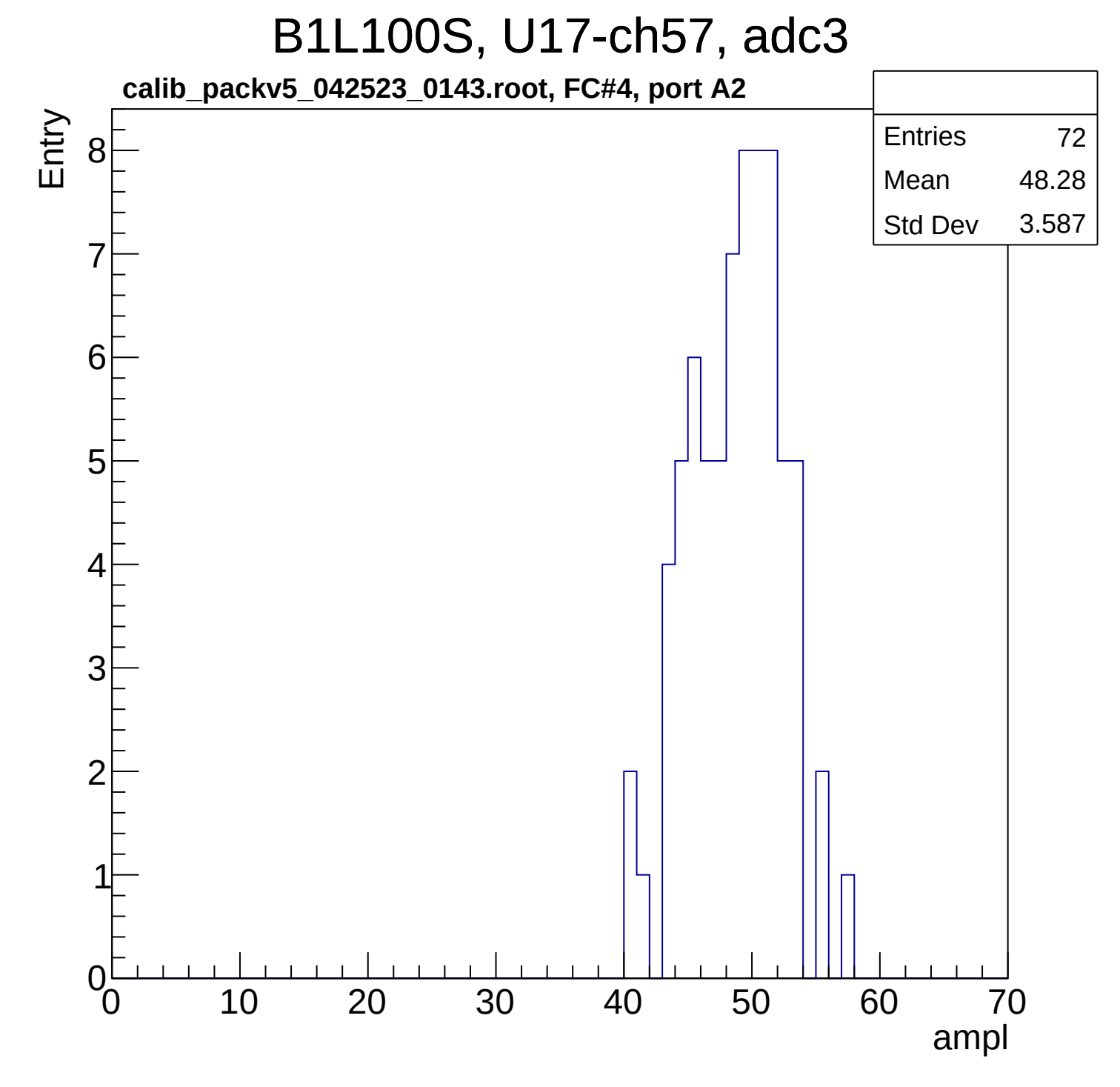
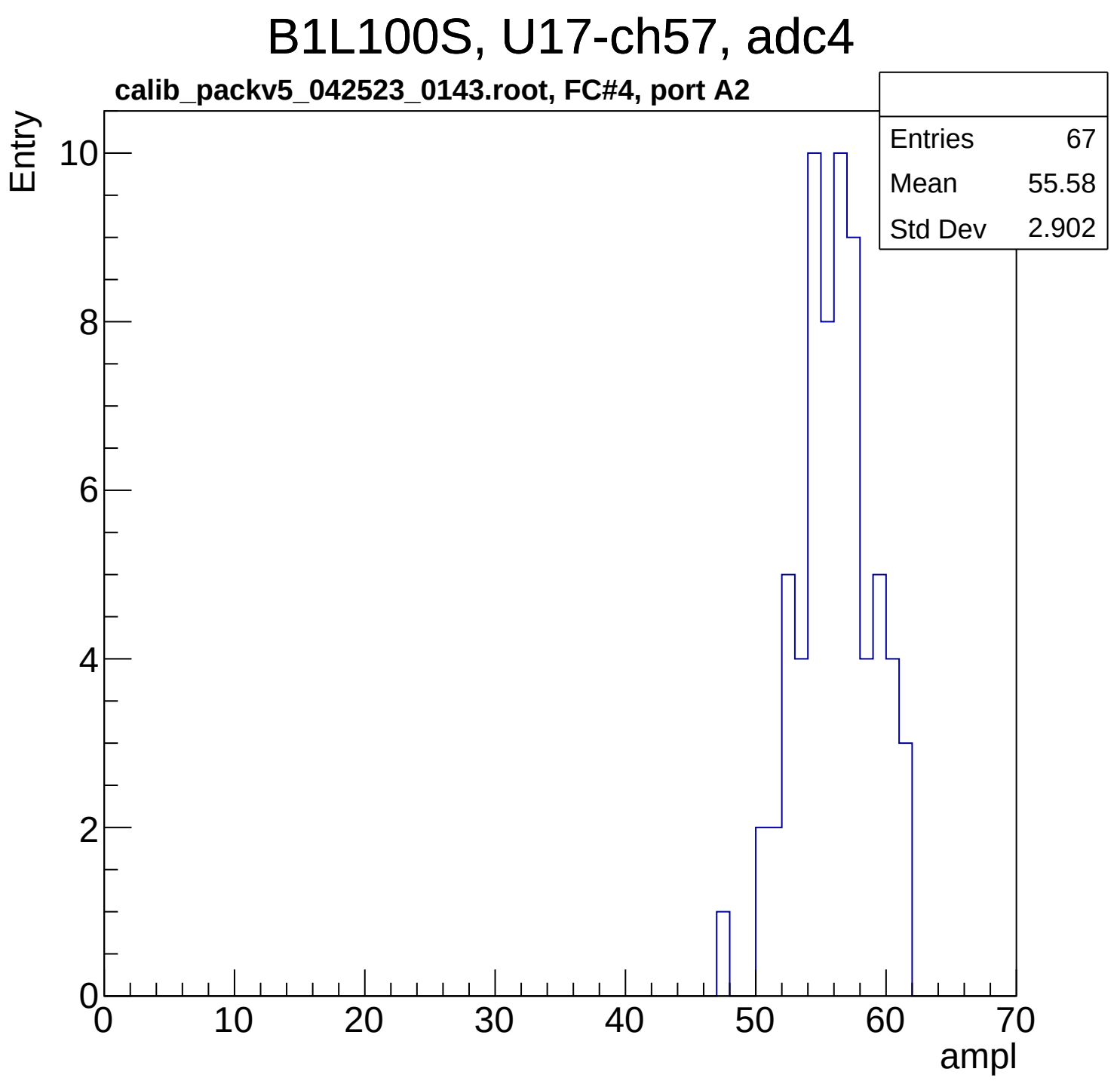
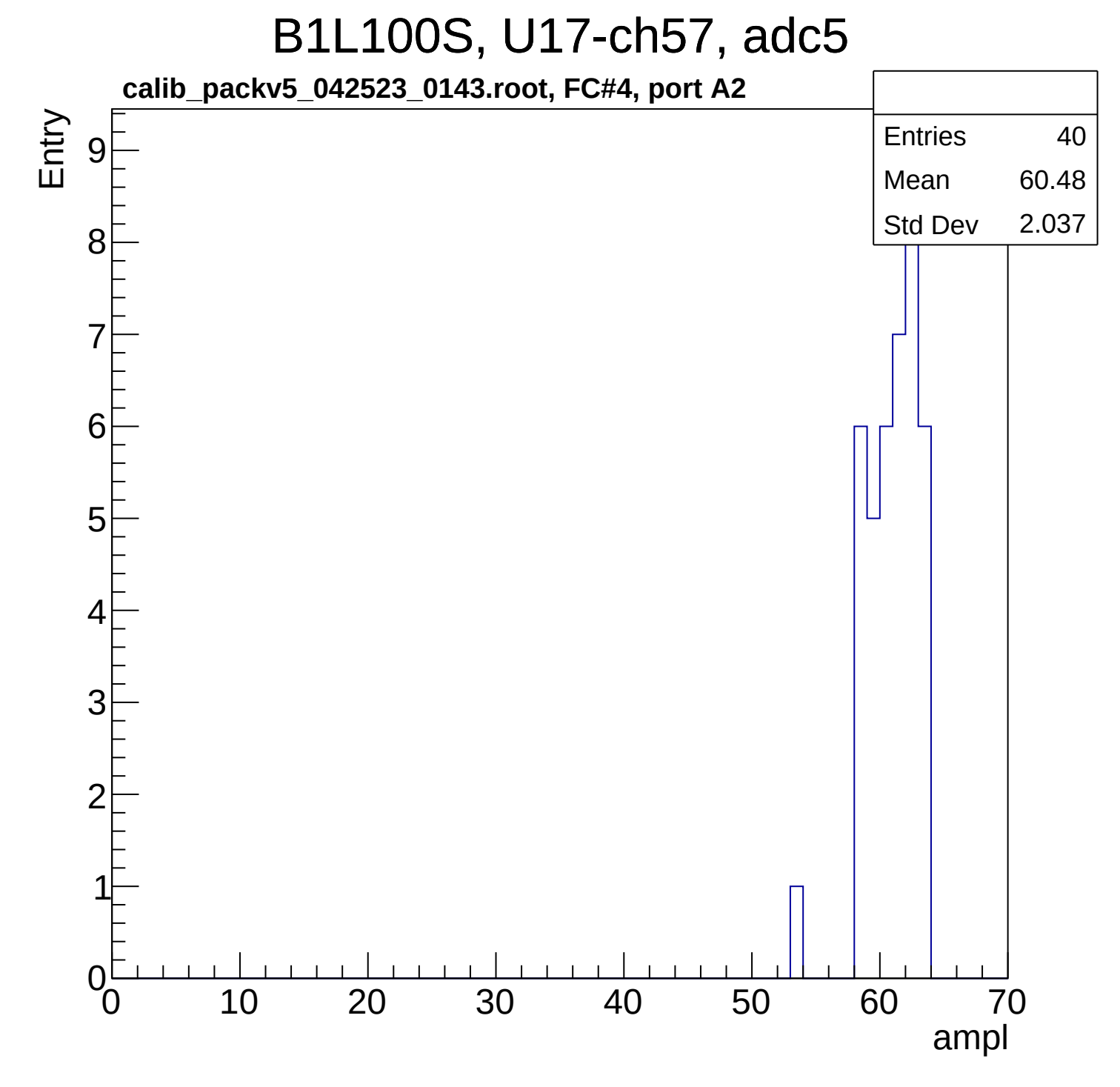

B1L100S, U17-ch57, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 35.23
Std Dev 2.975
Gaus mean : 35.7808
Gaus Width: 3.2126
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch57, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 41.91
Std Dev 3.702
Gaus mean : 42.8462
Gaus Width: 4.6303
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch57, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 48.28
Std Dev 3.587
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch57, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 55.58
Std Dev 2.902
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U17-ch57, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 40
Mean 60.48
Std Dev 2.037
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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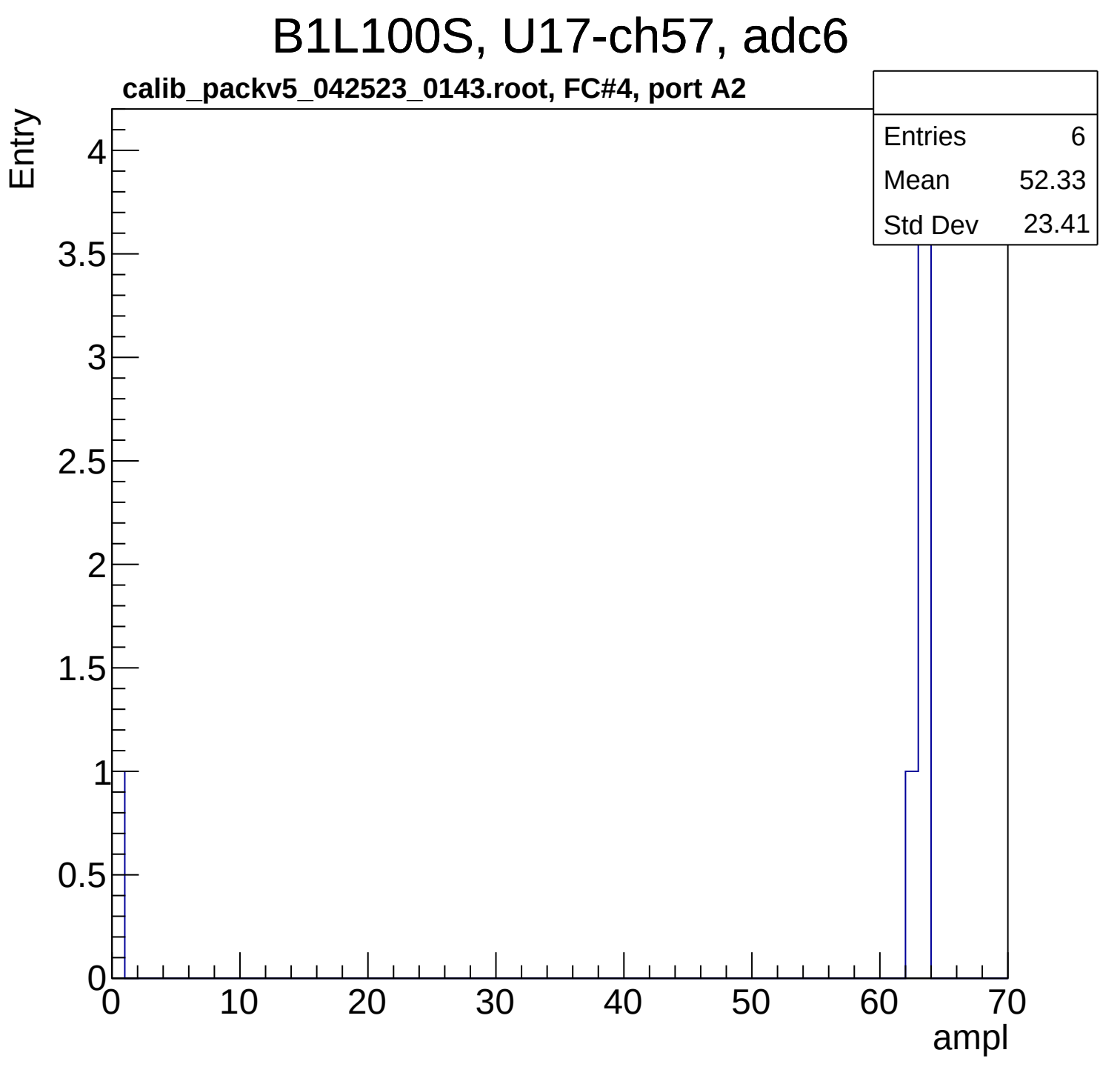
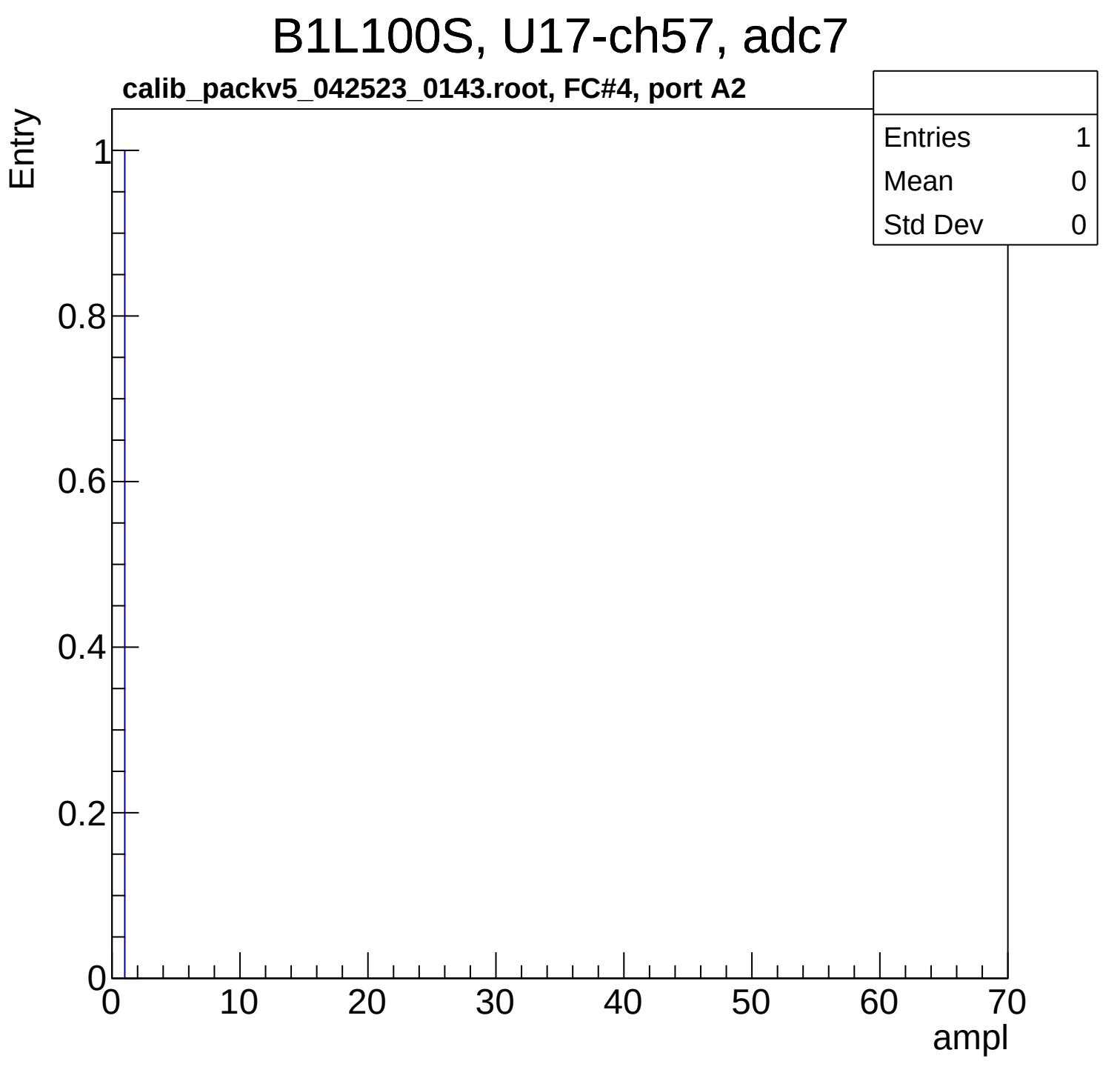

B1L100S, U17-ch57, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 6
Mean 52.33
Std Dev 23.41
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L100S, U17-ch57, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
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0.8
0.6
0.4
0.2
0
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10
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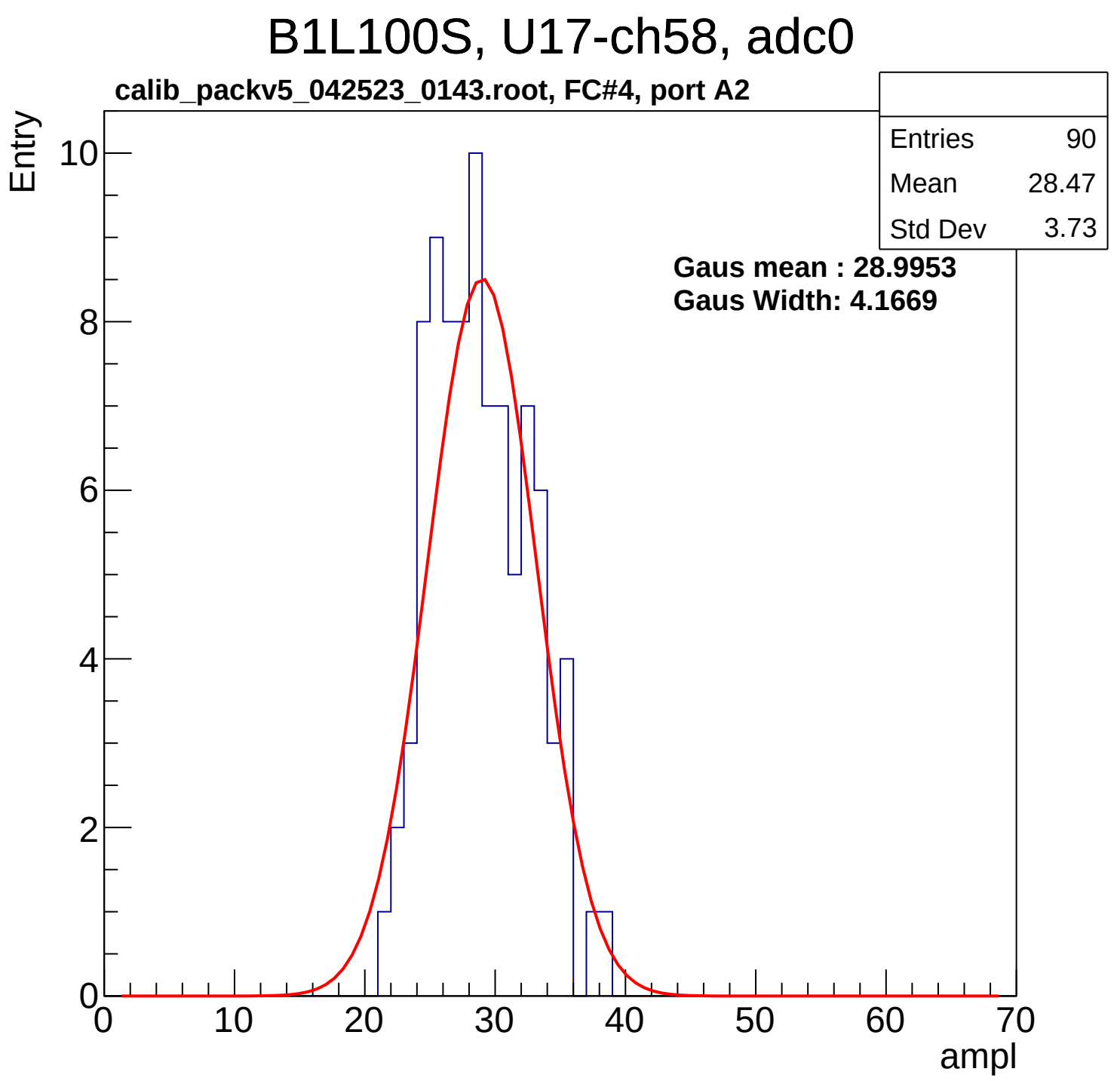
70
ampl


B1L100S, U17-ch58, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 90
Mean 28.47
Std Dev 3.73
Gaus mean : 28.9953
Gaus Width: 4.1669
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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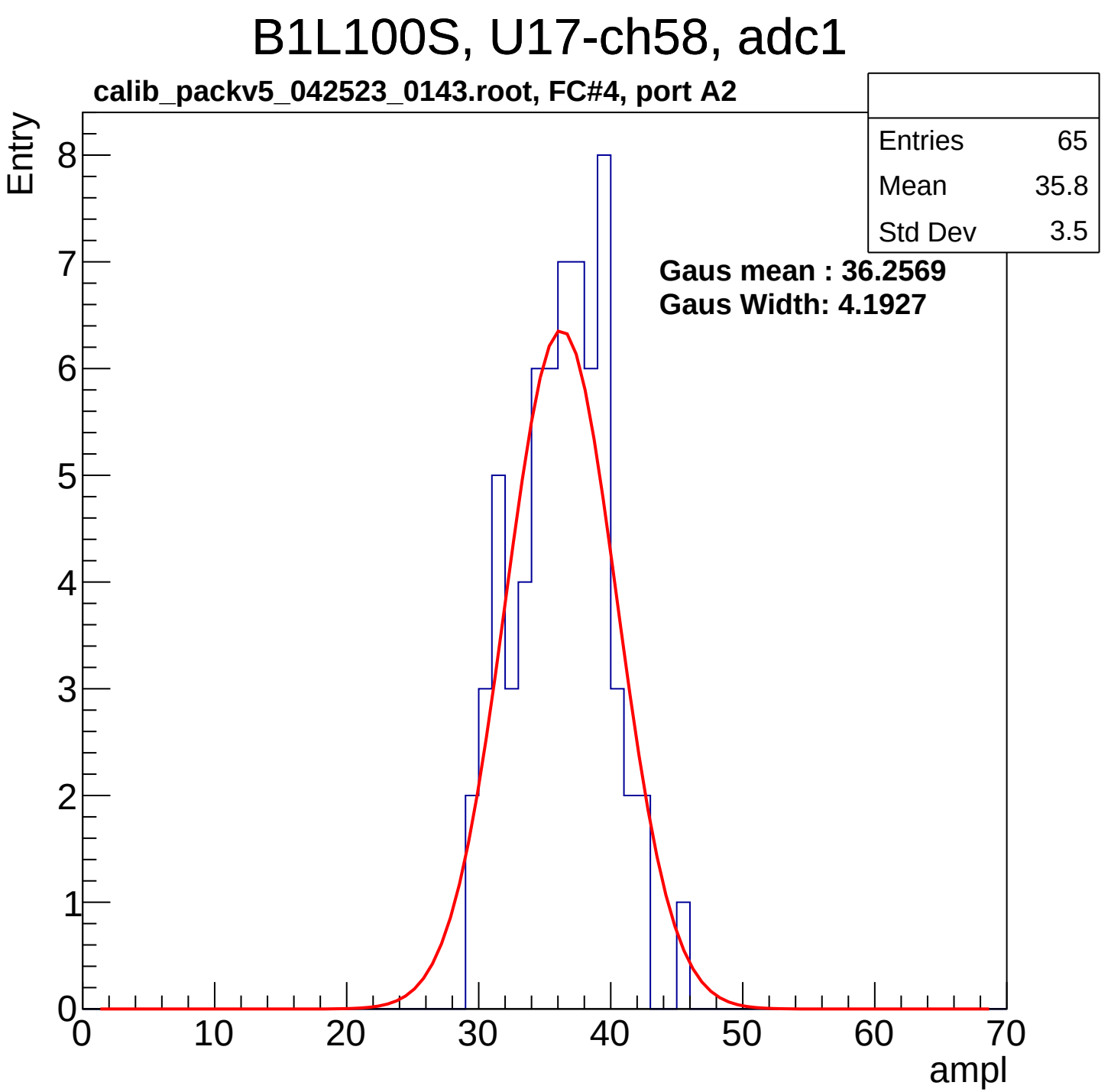
B1L100S, U17-ch58, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 35.8
Std Dev 3.5
Gaus mean : 36.2569
Gaus Width: 4.1927
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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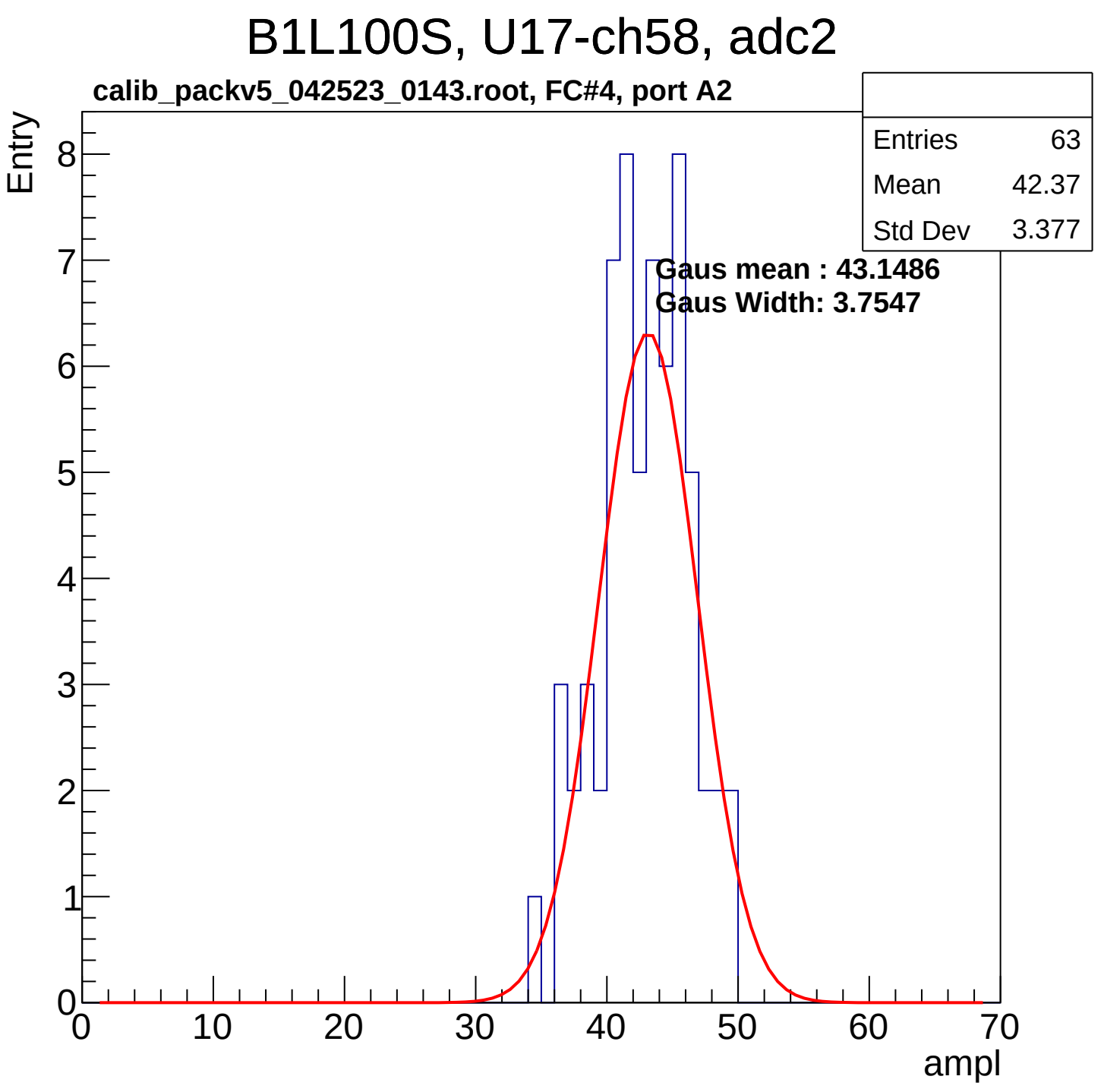
B1L100S, U17-ch58, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 42.37
Std Dev 3.377
Gaus mean : 43.1486
Gaus Width: 3.7547
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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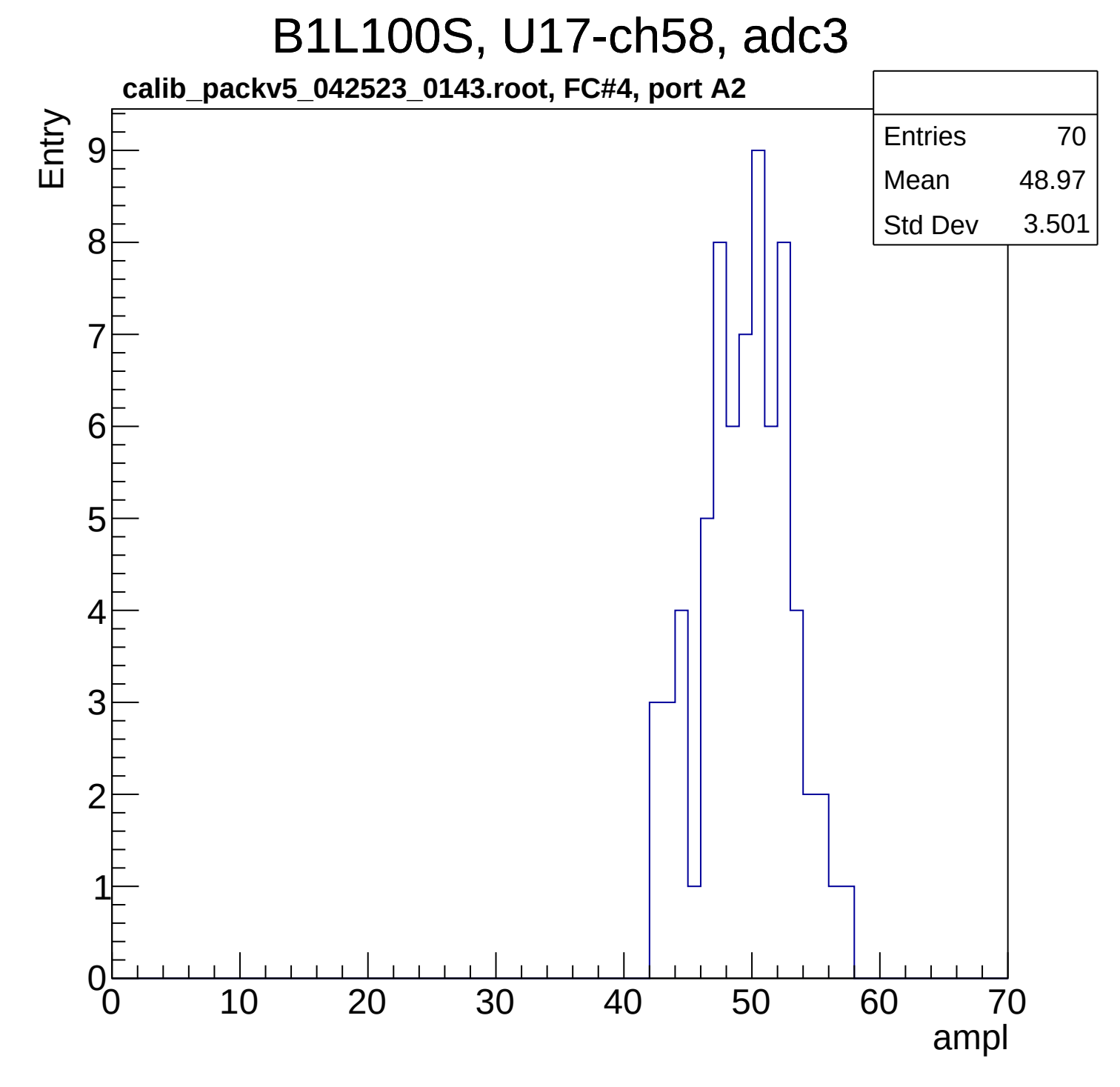
B1L100S, U17-ch58, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 48.97
Std Dev 3.501
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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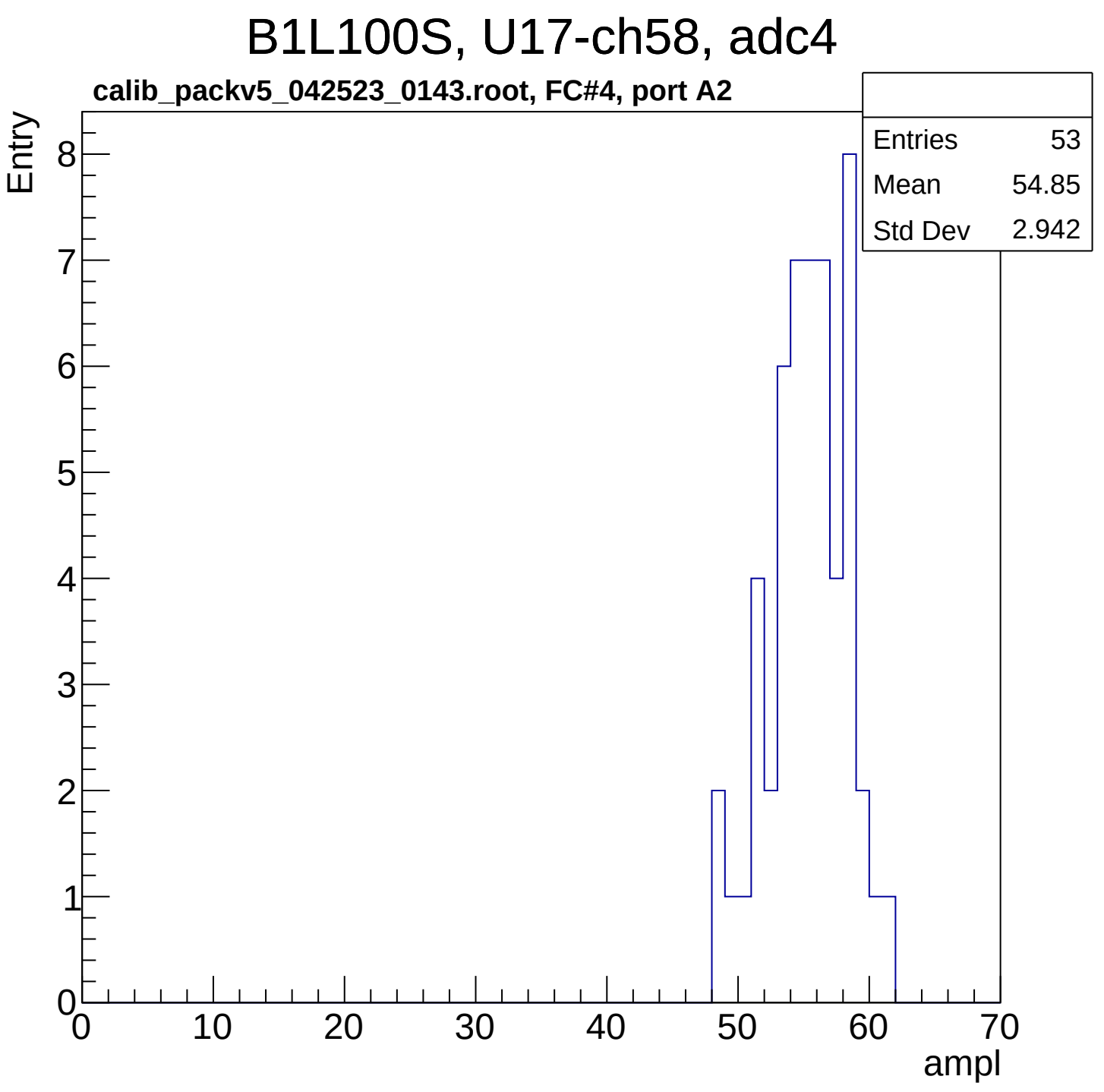
B1L100S, U17-ch58, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 54.85
Std Dev 2.942
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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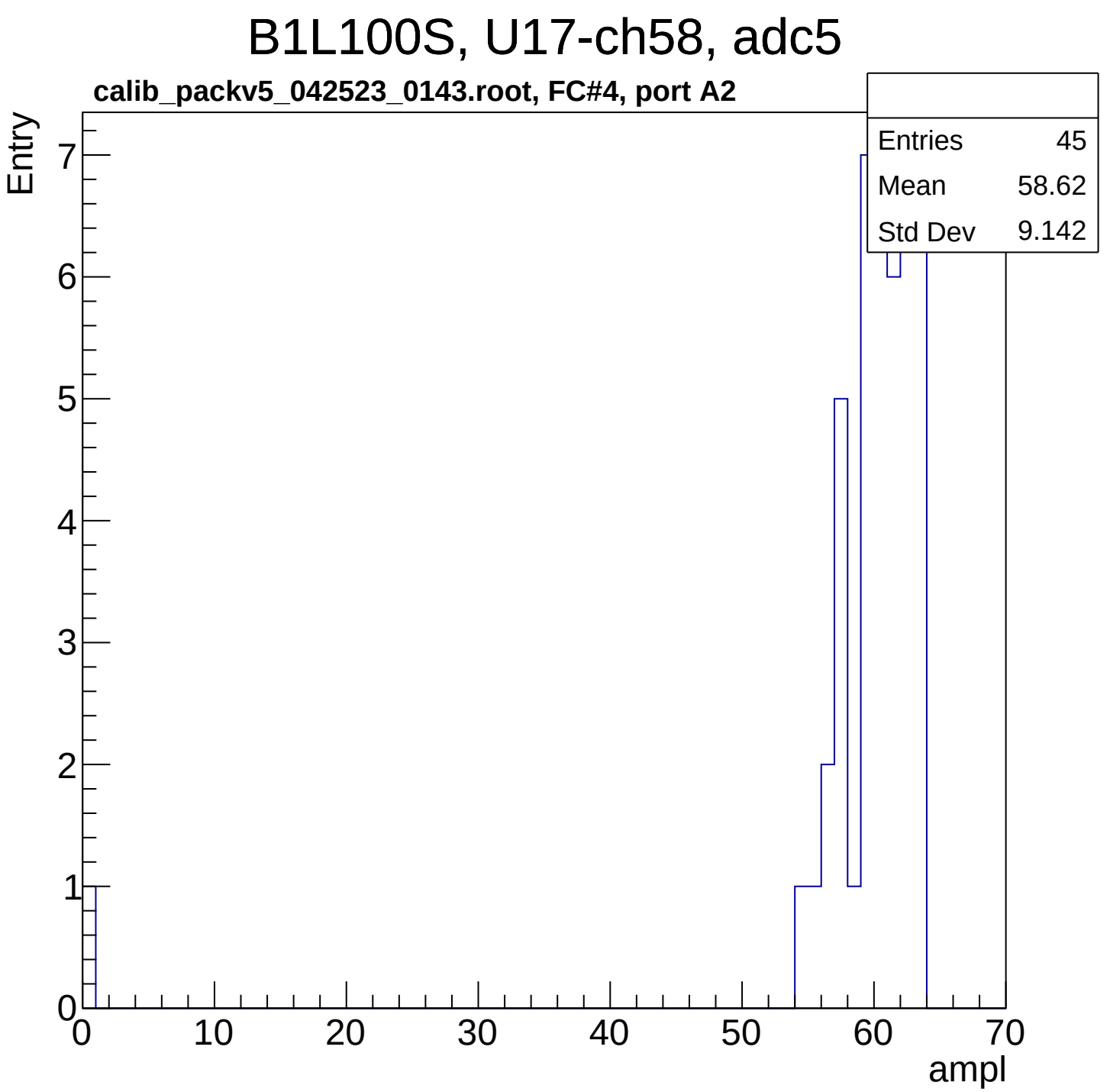
B1L100S, U17-ch58, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 45
Mean 58.62
Std Dev 9.142
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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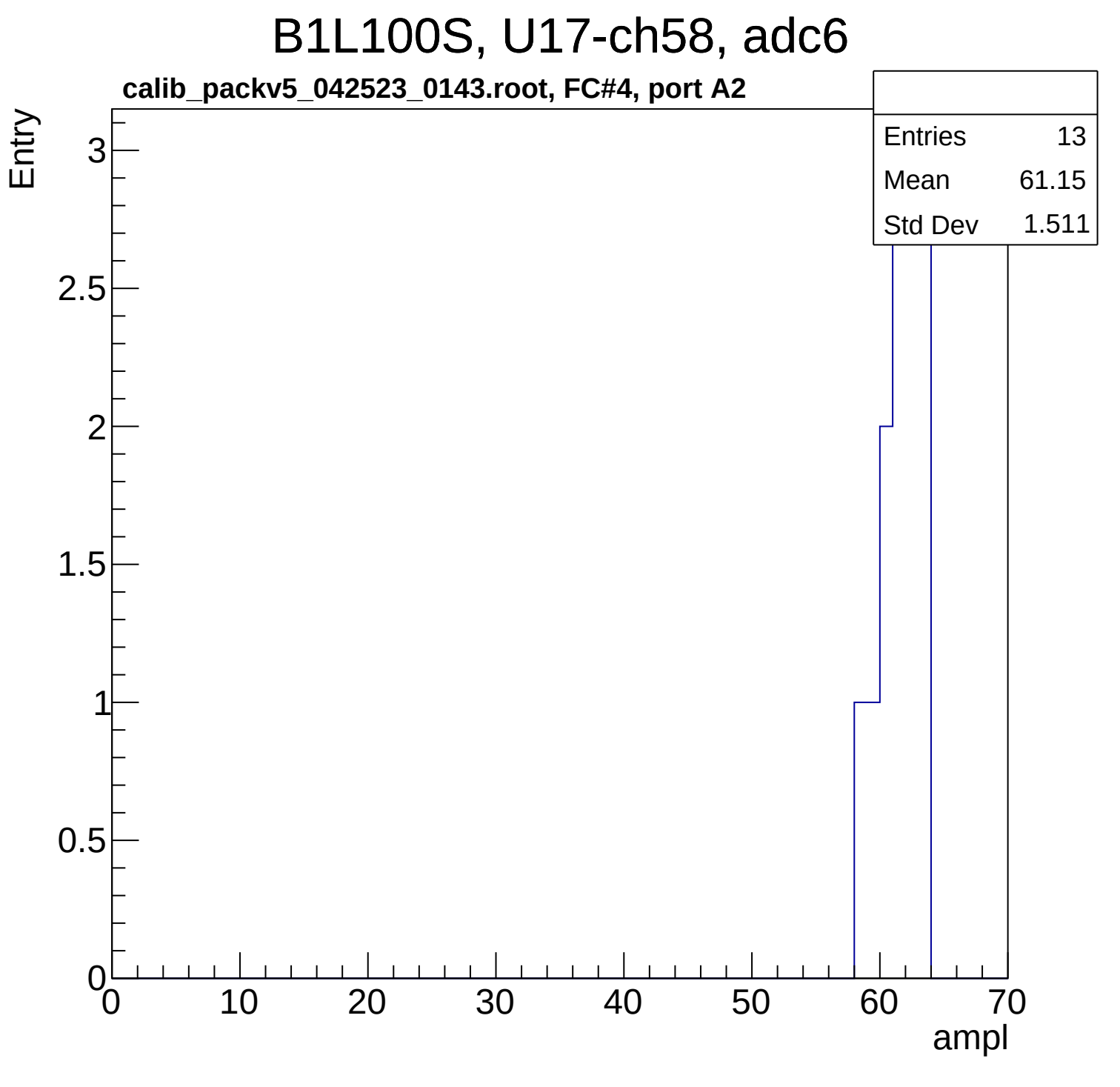
B1L100S, U17-ch58, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 13
Mean 61.15
Std Dev 1.511
Entry
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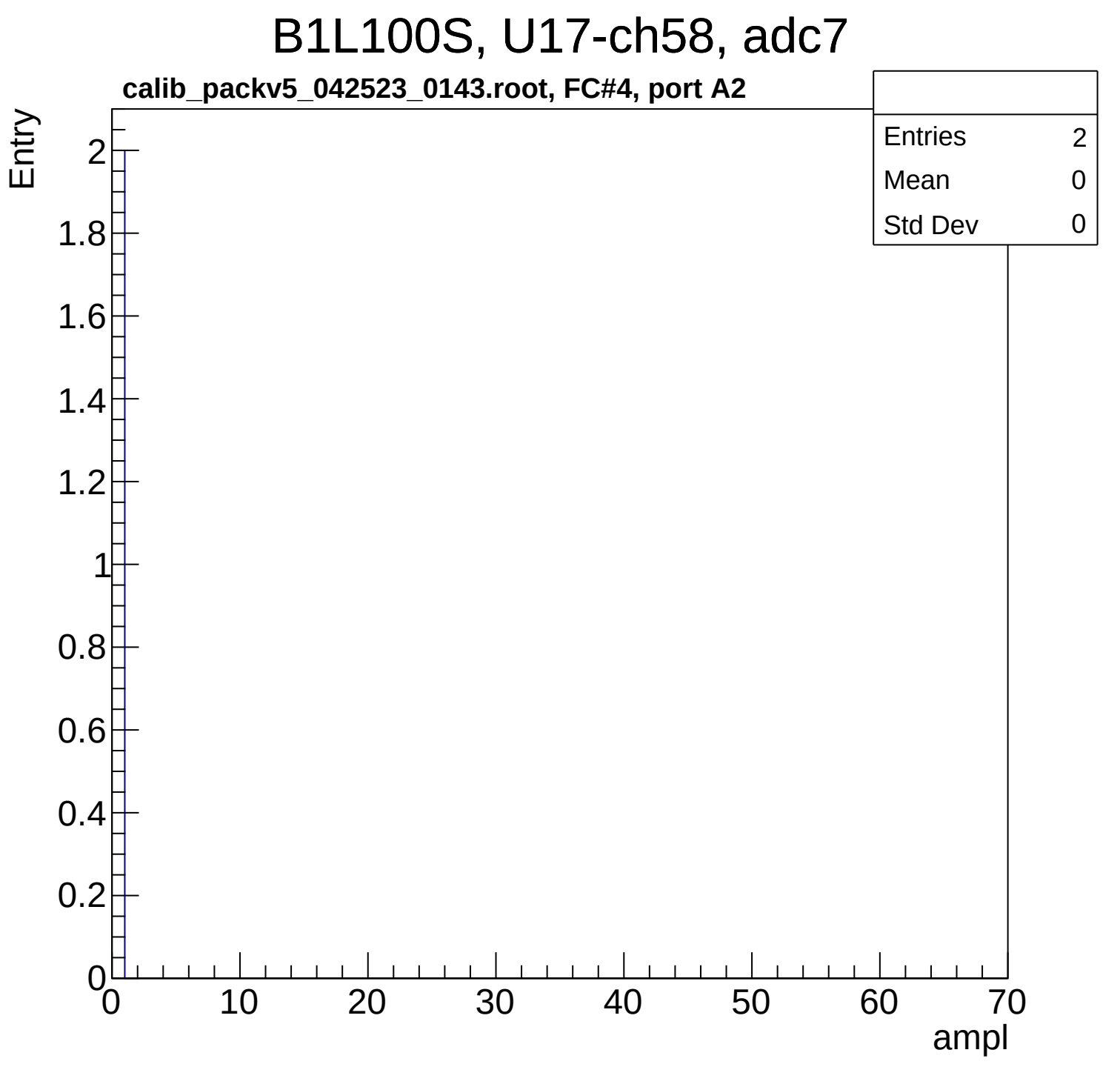
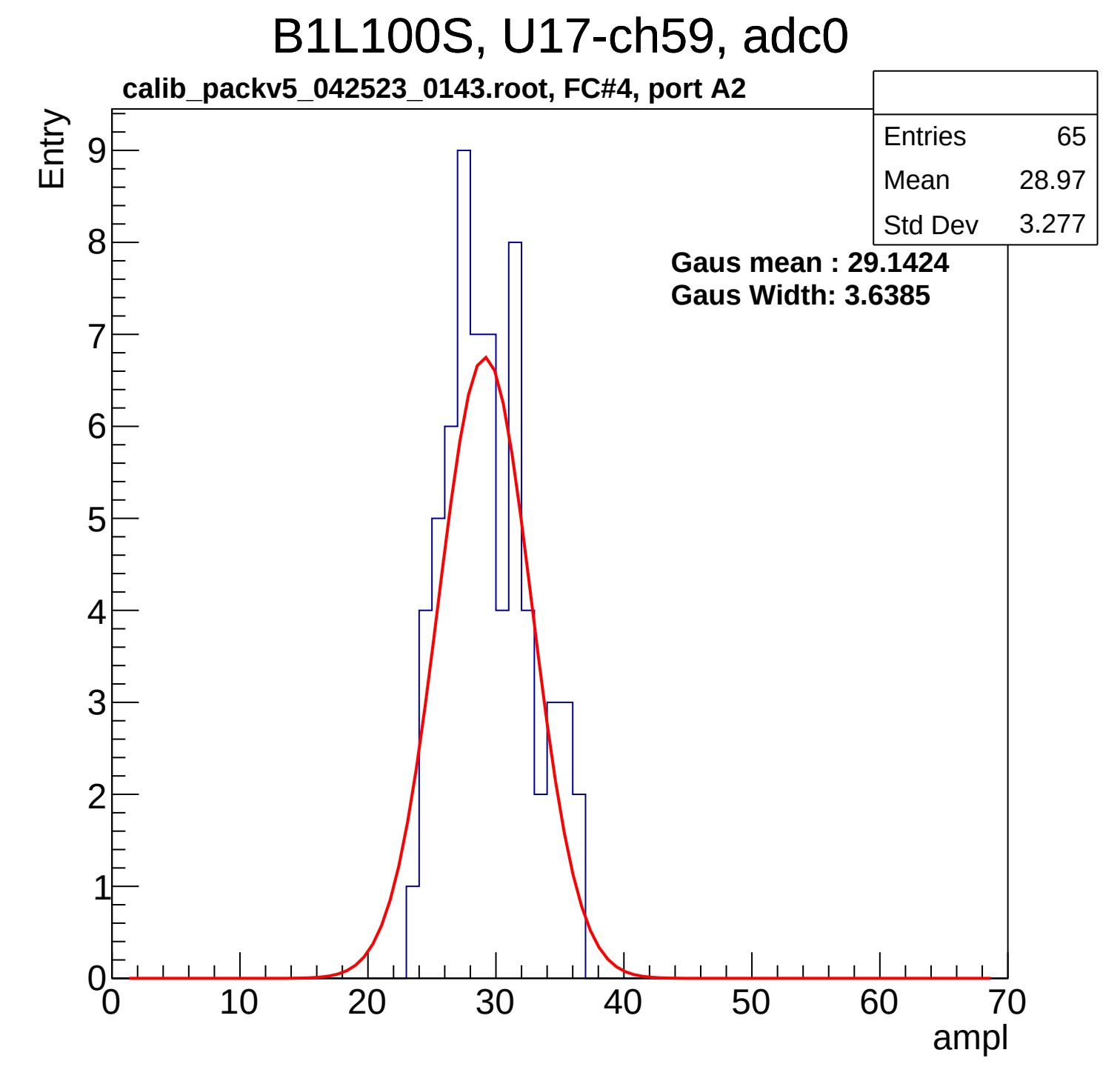
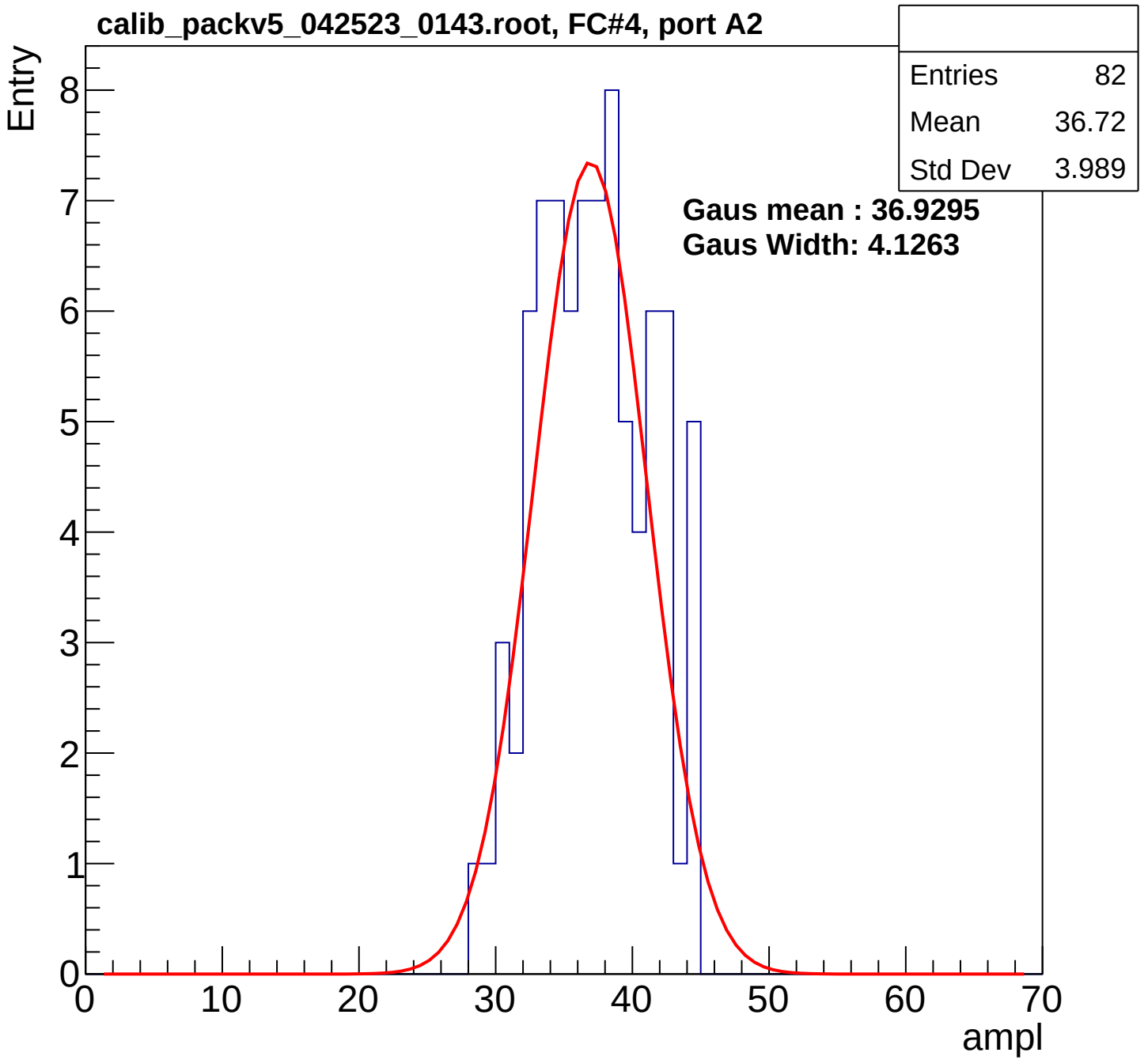
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch58, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch59, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 28.97
Std Dev 3.277
Gaus mean : 29.1424
Gaus Width: 3.6385
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch59, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 82
Mean 36.72
Std Dev 3.989
Gaus mean : 36.9295
Gaus Width: 4.1263
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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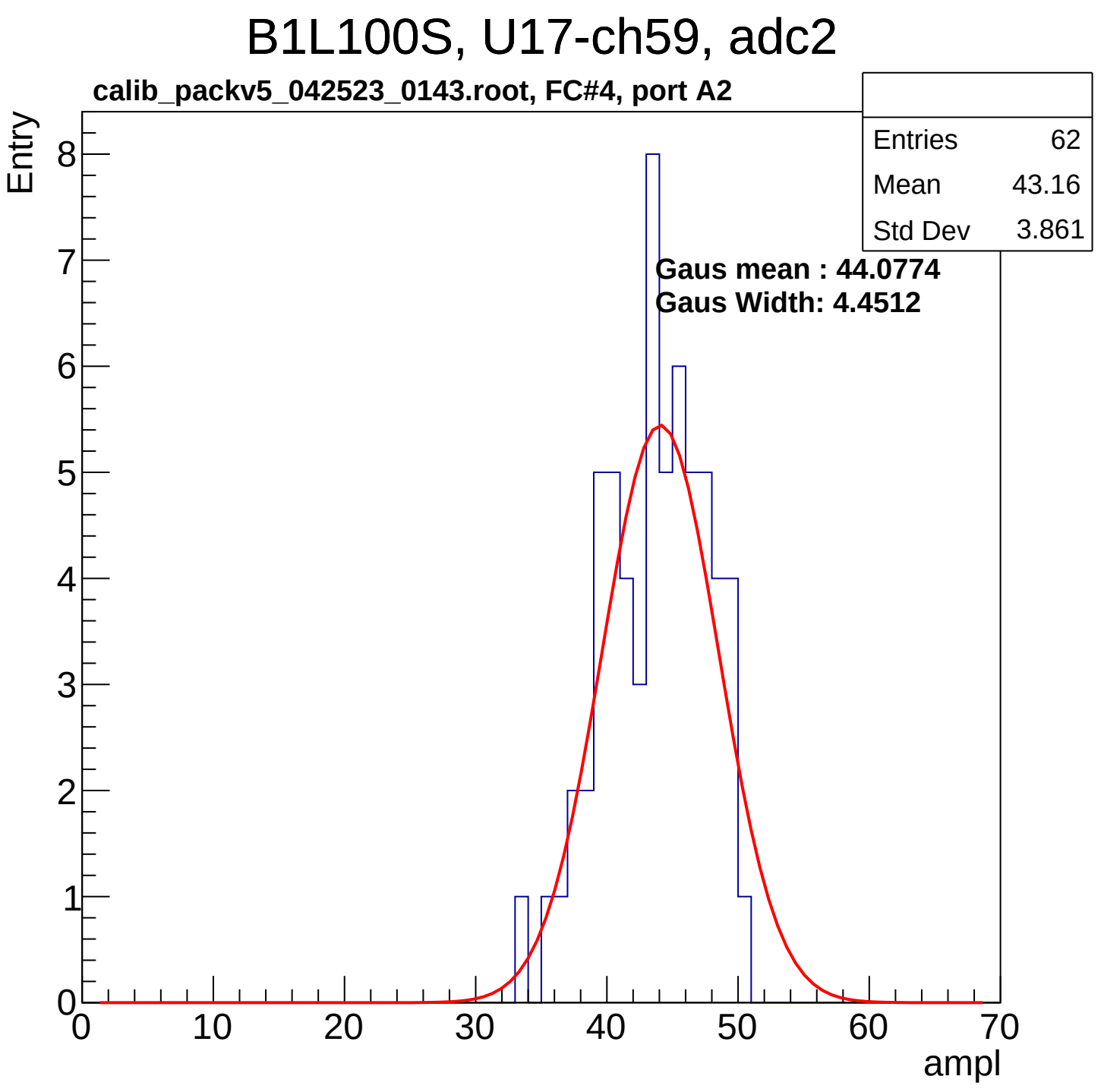
B1L100S, U17-ch59, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 43.16
Std Dev 3.861
Gaus mean : 44.0774
Gaus Width: 4.4512
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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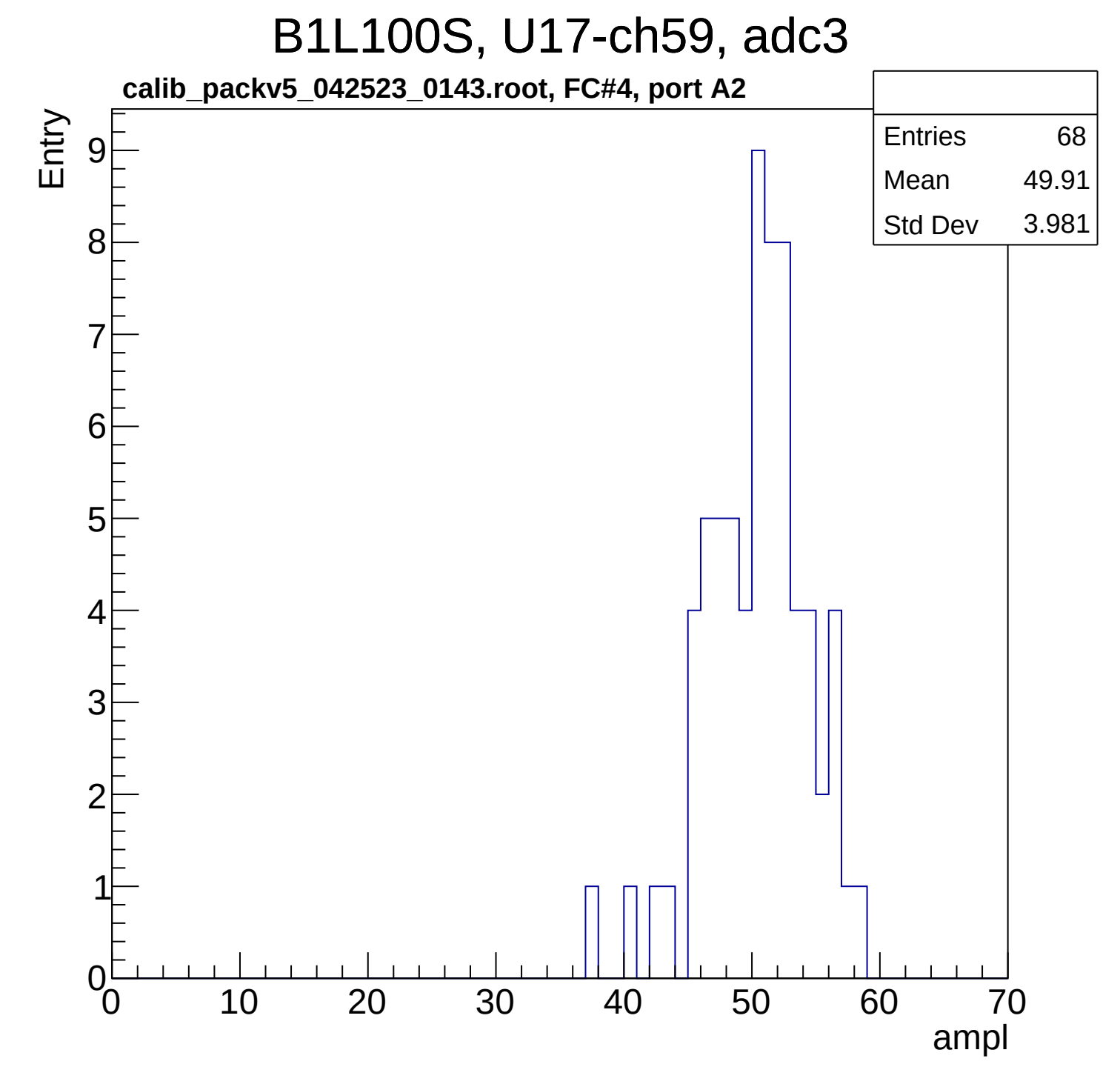
B1L100S, U17-ch59, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 49.91
Std Dev 3.981
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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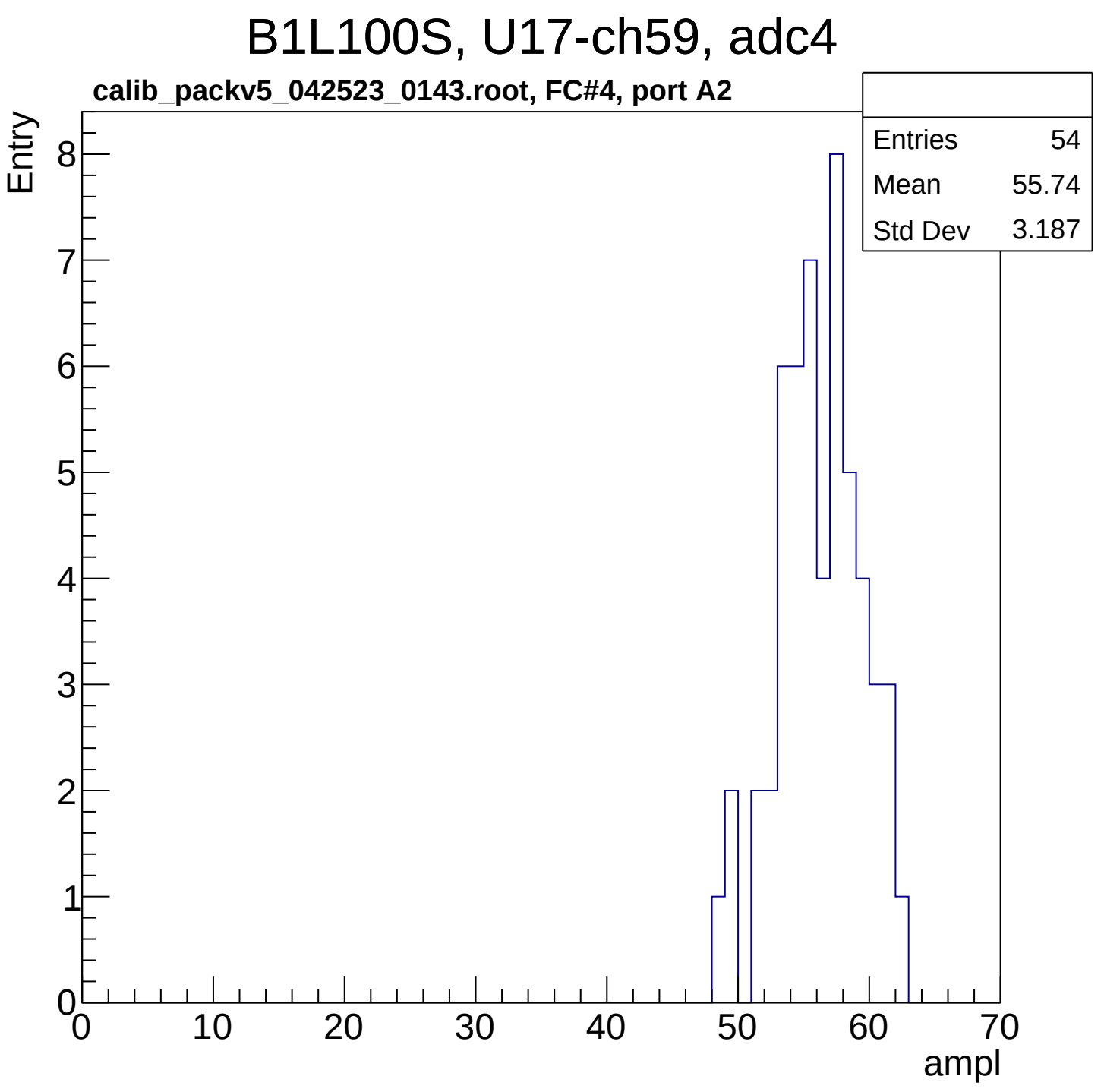
40
50
60
70


B1L100S, U17-ch59, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 55.74
Std Dev 3.187
Entry
ampl
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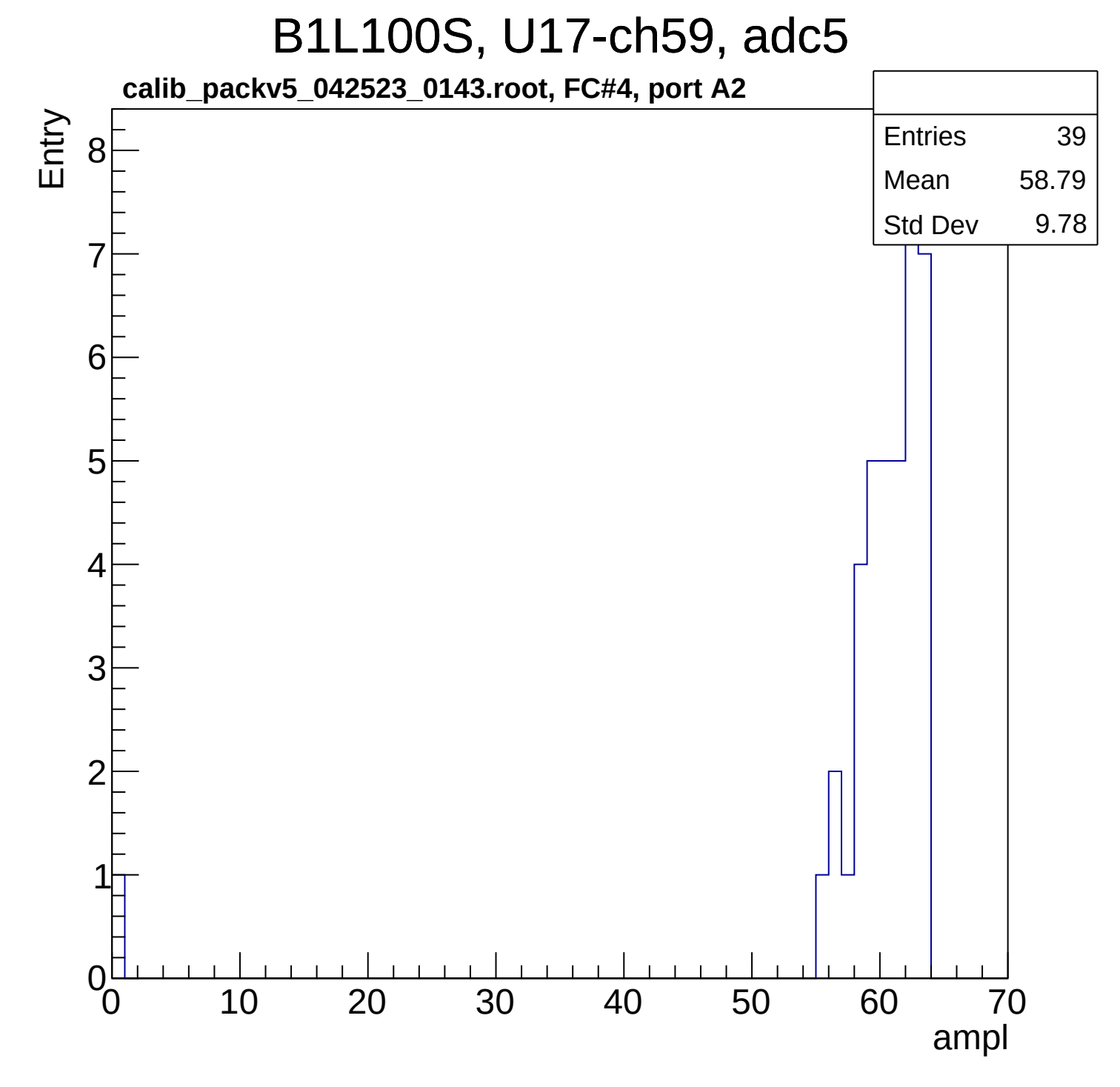
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch59, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 39
Mean 58.79
Std Dev 9.78
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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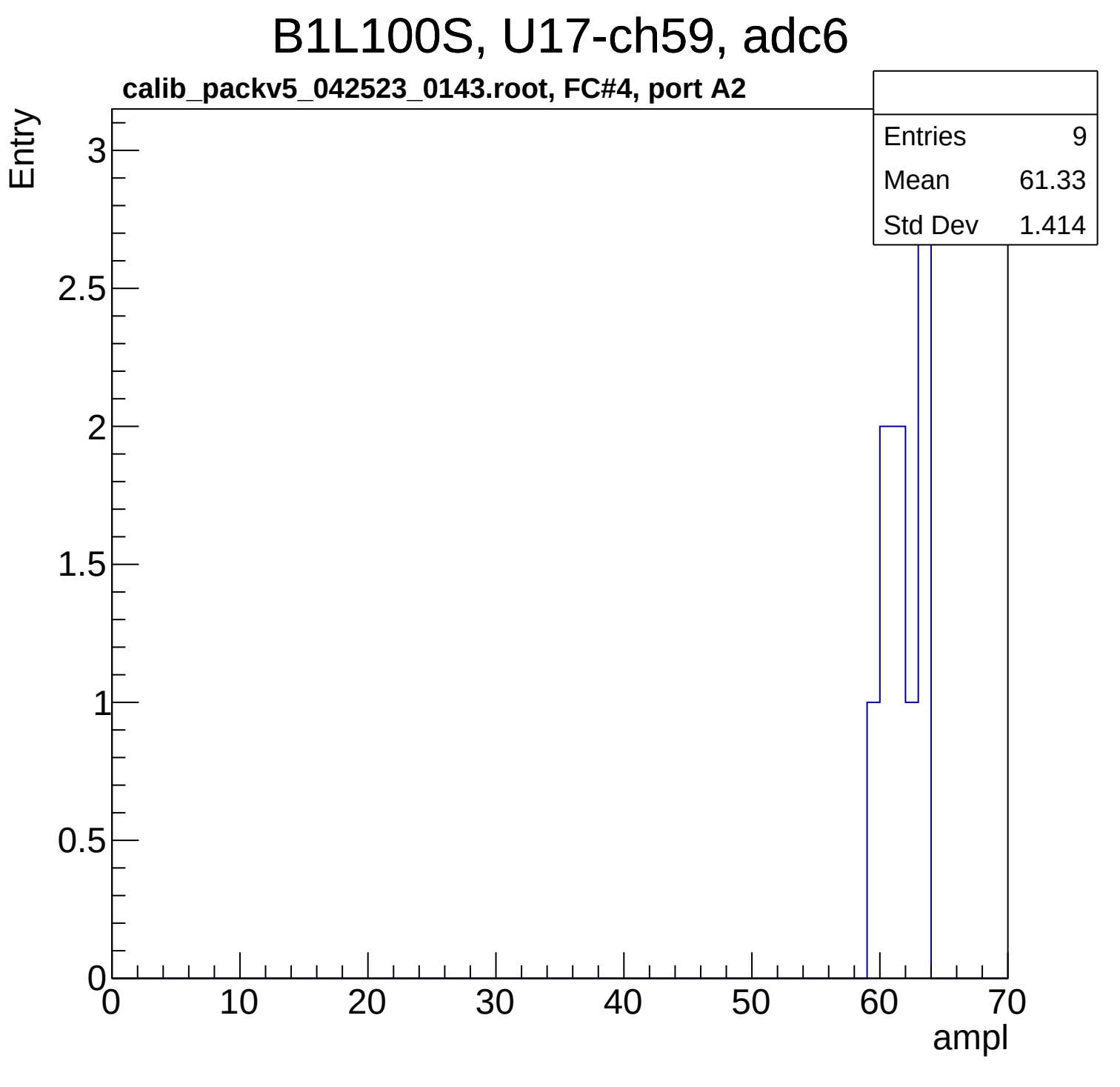
B1L100S, U17-ch59, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 9
Mean 61.33
Std Dev 1.414
Entry
ampl
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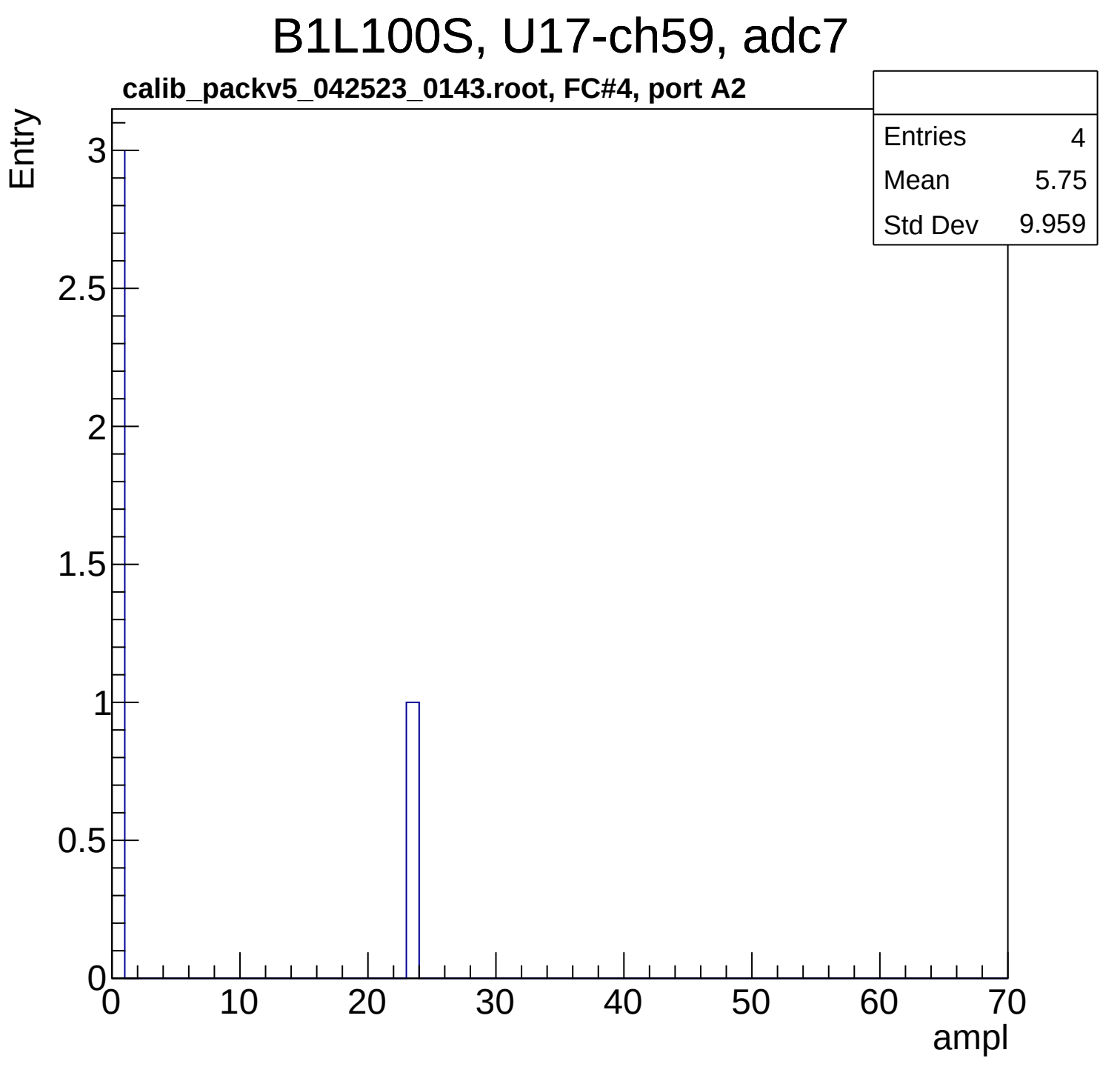
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L100S, U17-ch59, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 4
Mean 5.75
Std Dev 9.959
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
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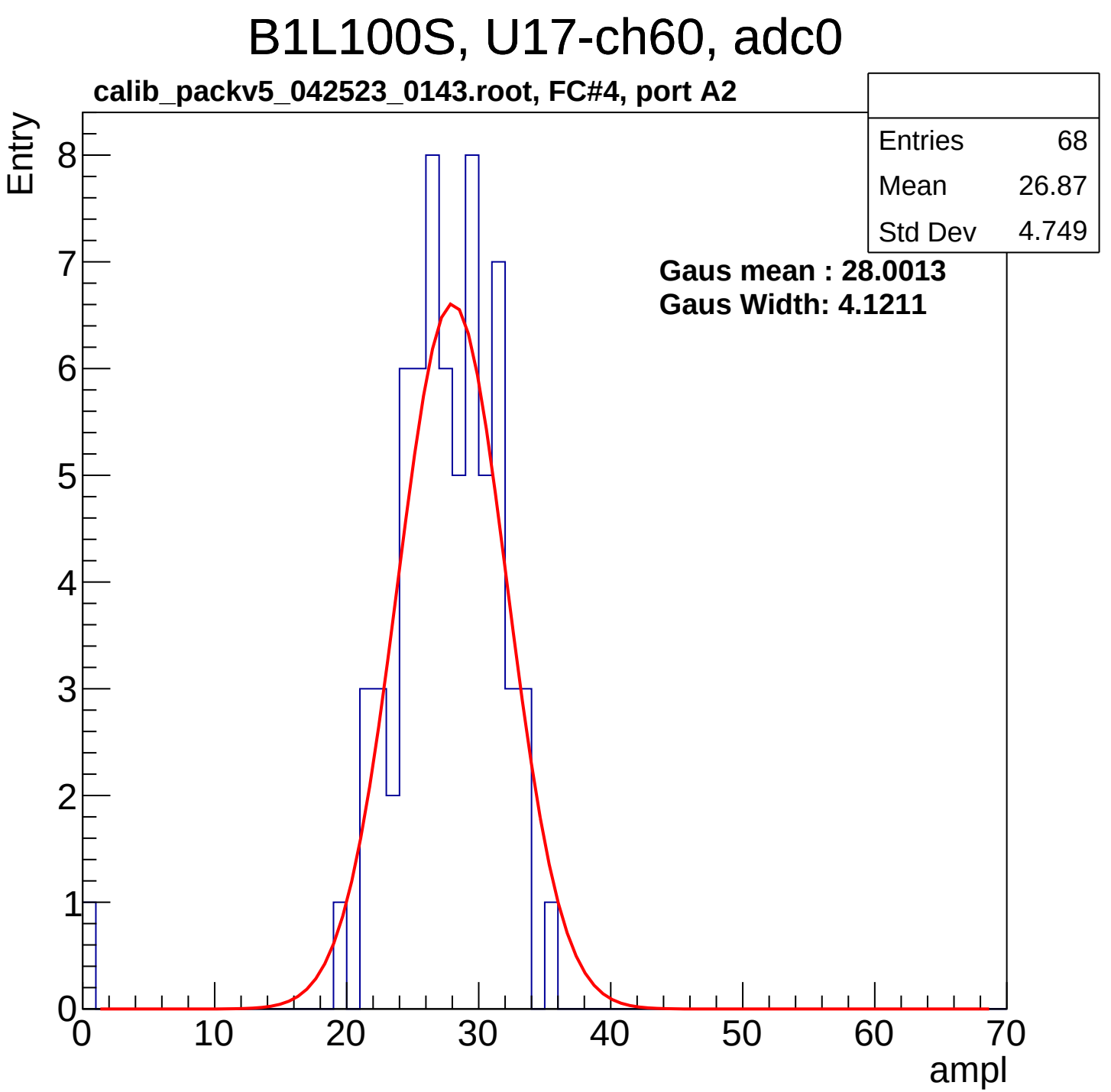
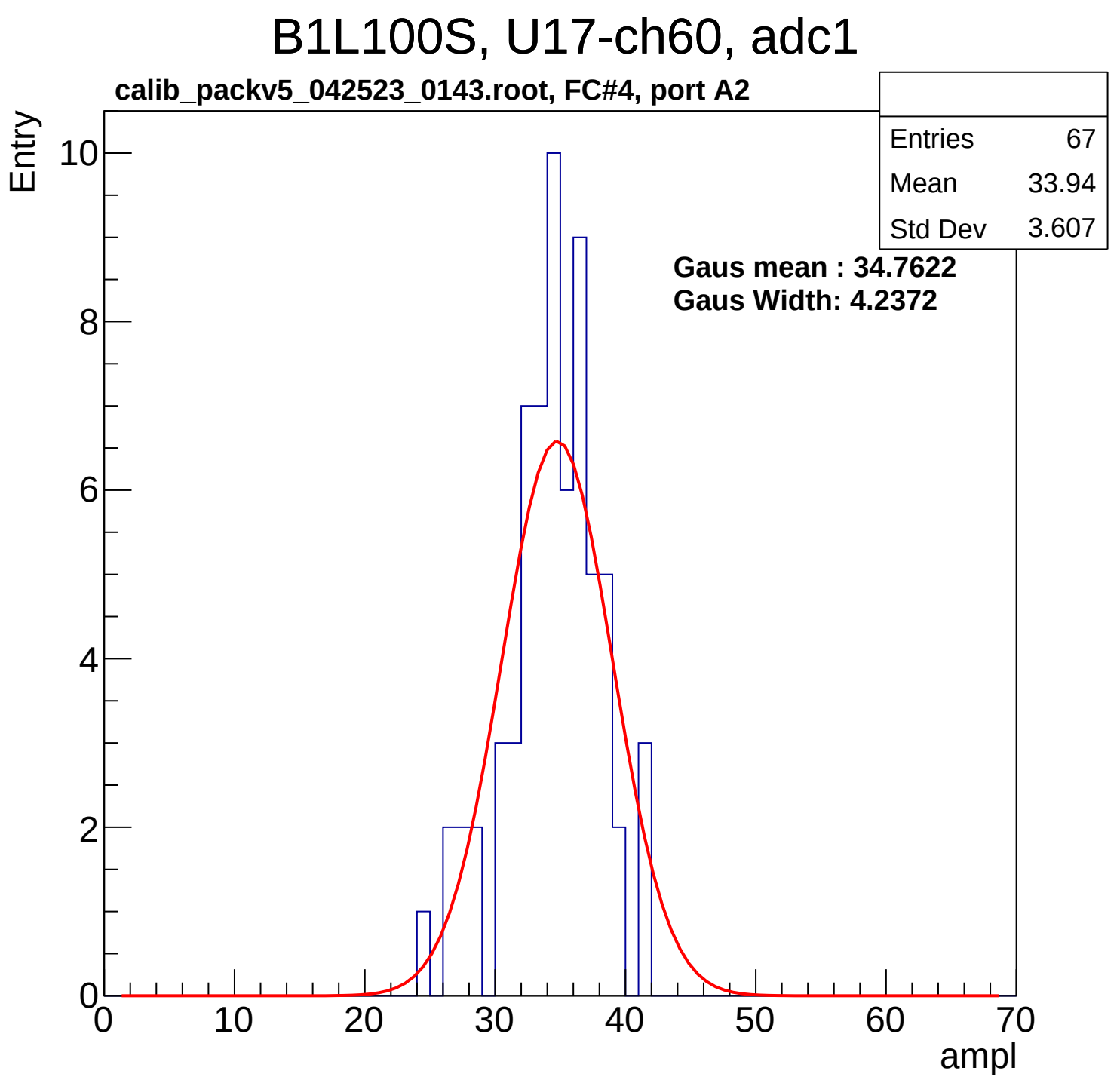
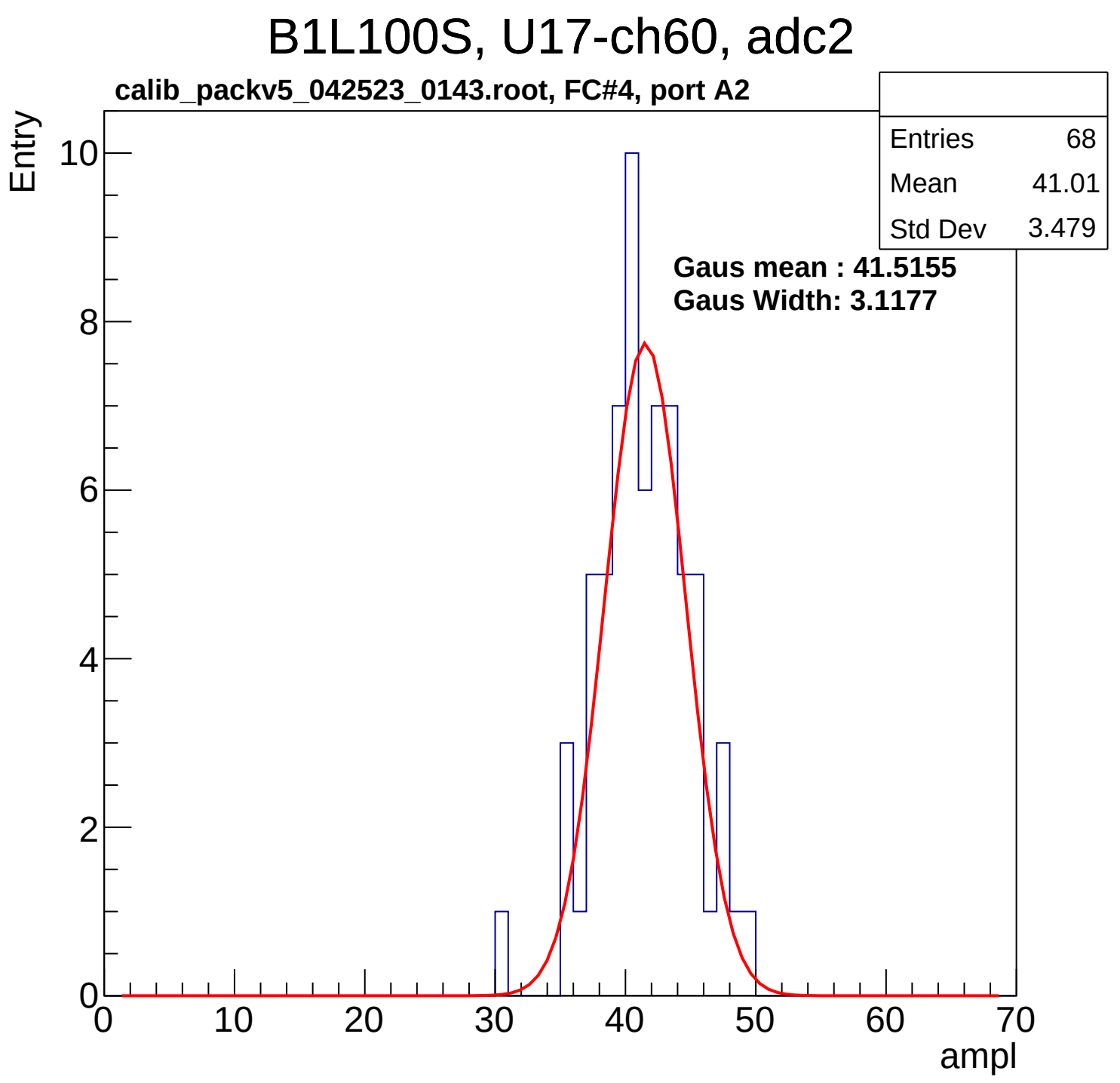

B1L100S, U17-ch60, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 26.87
Std Dev 4.749
Gaus mean : 28.0013
Gaus Width: 4.1211
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch60, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 33.94
Std Dev 3.607
Gaus mean : 34.7622
Gaus Width: 4.2372
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U17-ch60, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 41.01
Std Dev 3.479
Gaus mean : 41.5155
Gaus Width: 3.1177
Entry
ampl
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4
6
8
10
0
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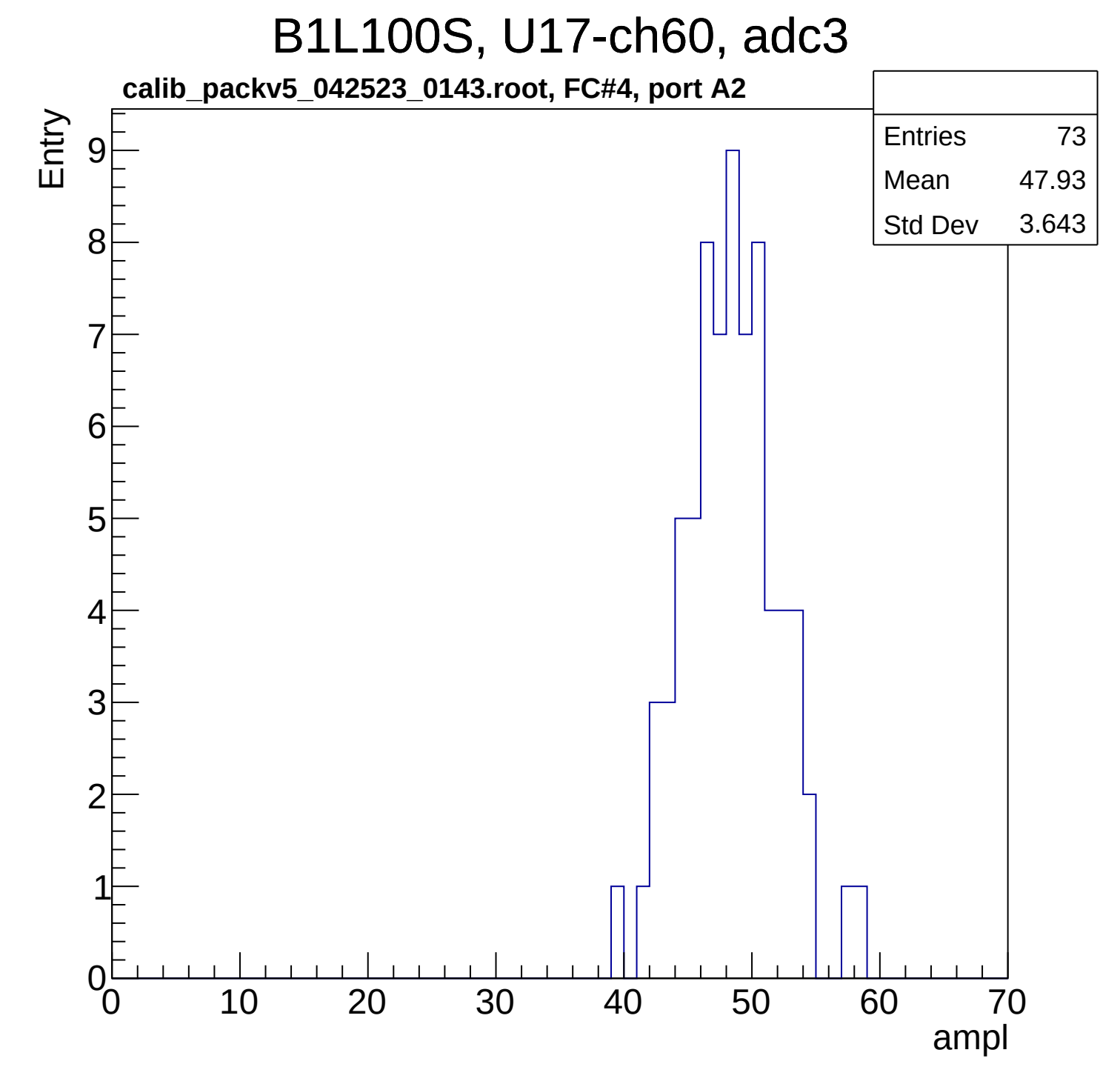
50
60
70


B1L100S, U17-ch60, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 47.93
Std Dev 3.643
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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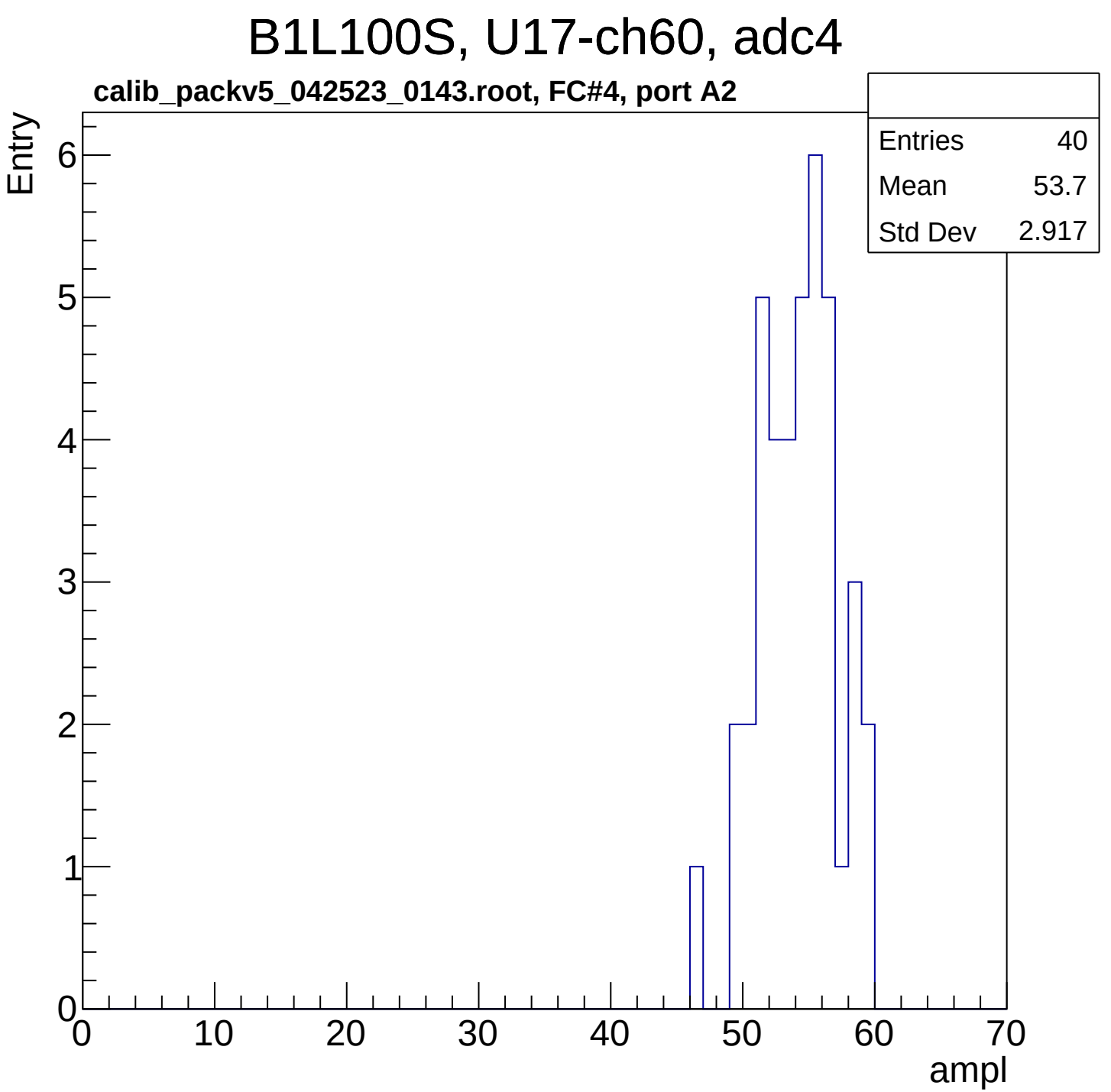
B1L100S, U17-ch60, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 40
Mean 53.7
Std Dev 2.917
Entry
ampl
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2
3
4
5
6
0
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20
30
40
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60
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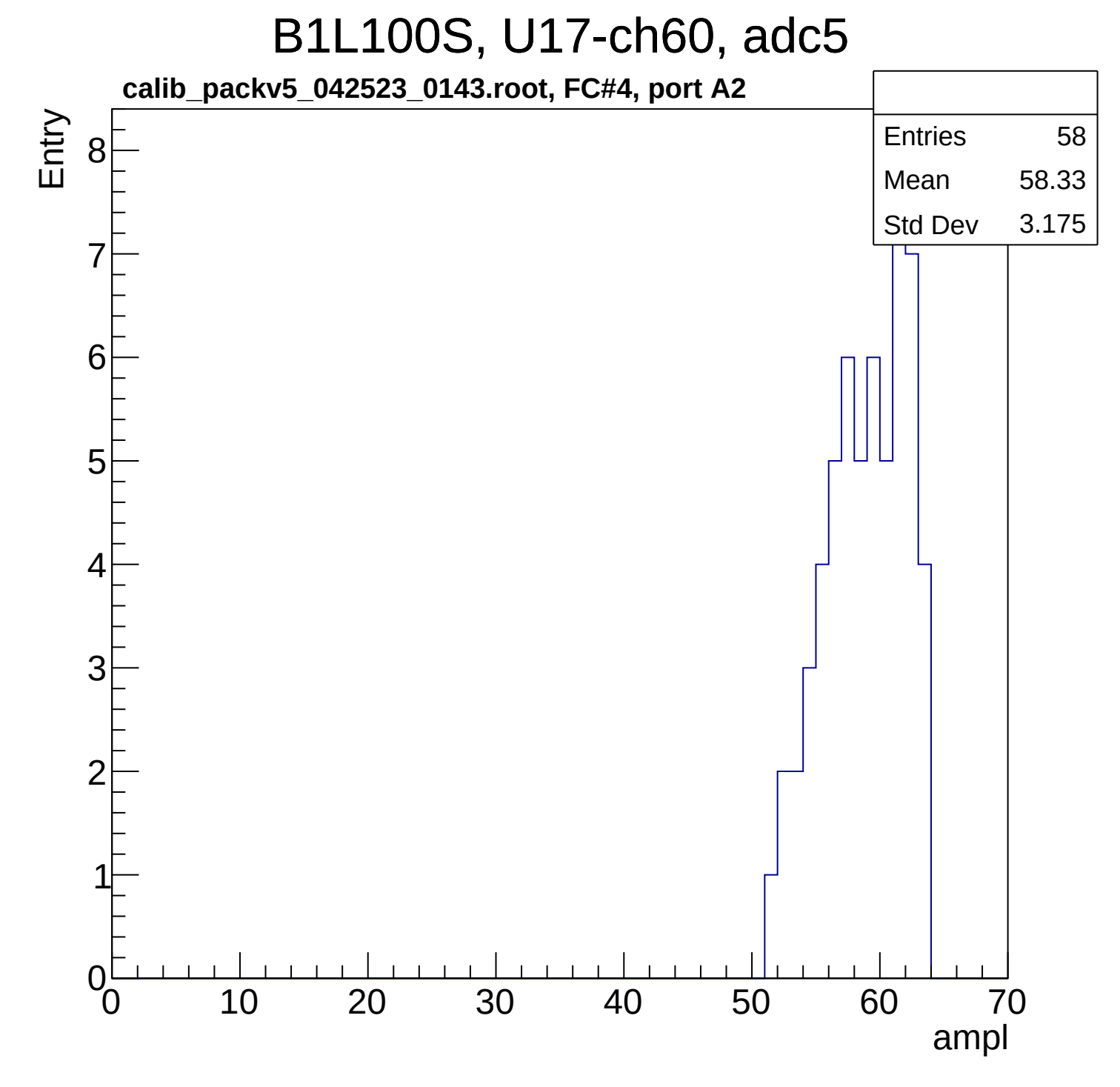
B1L100S, U17-ch60, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 58.33
Std Dev 3.175
Entry
ampl
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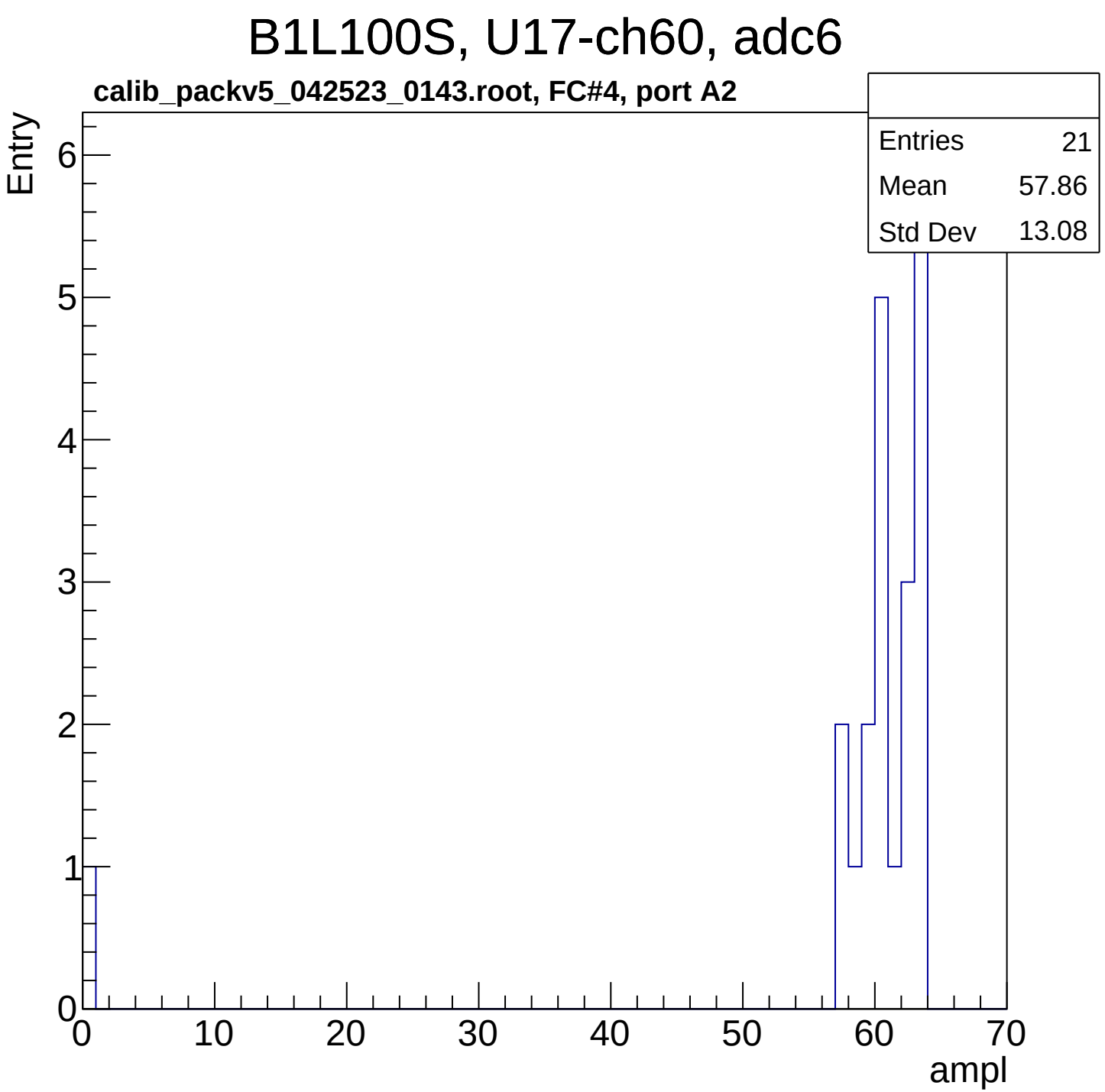
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch60, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 21
Mean 57.86
Std Dev 13.08
Entry
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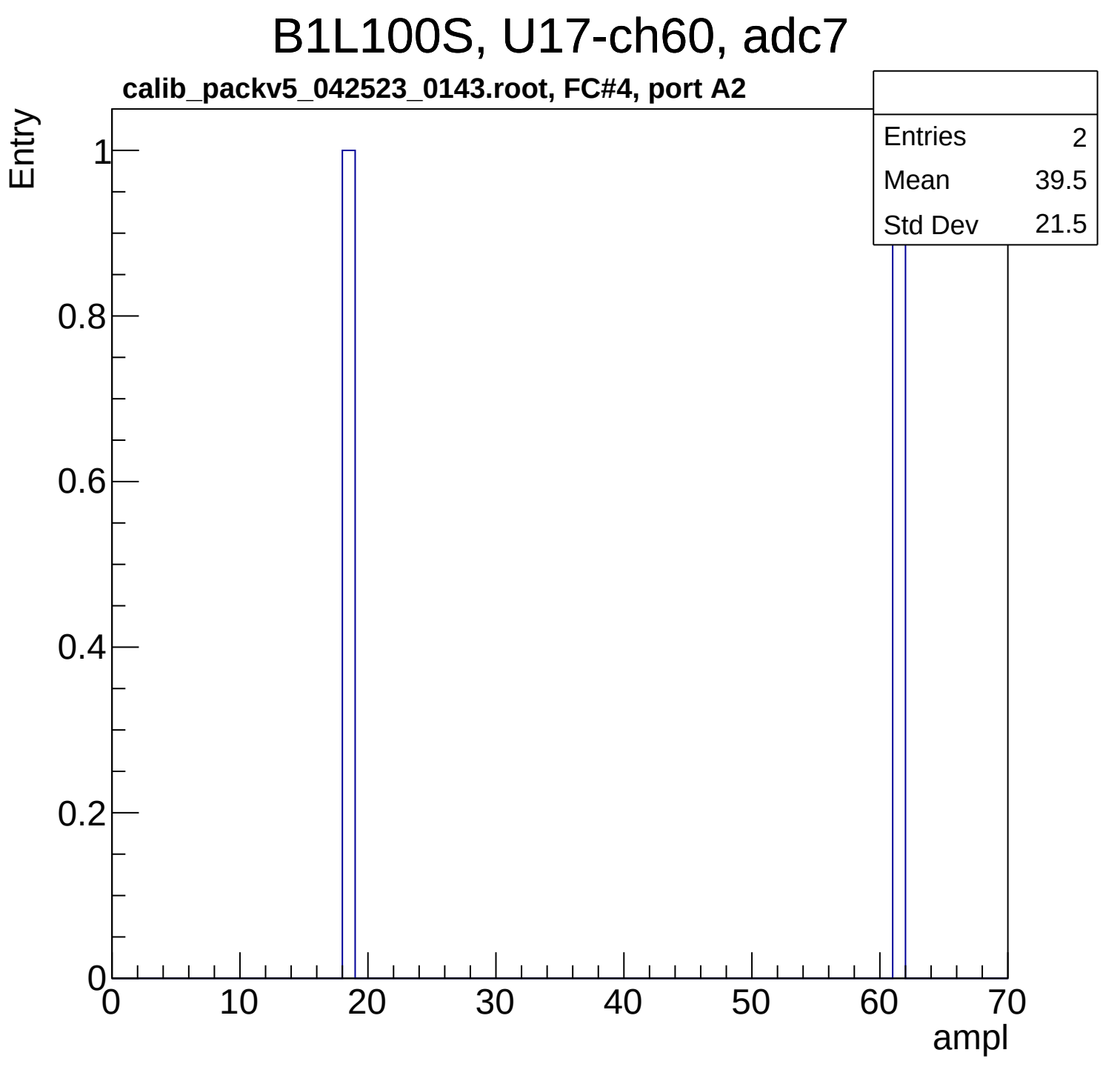
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch60, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 39.5
Std Dev 21.5
Entry
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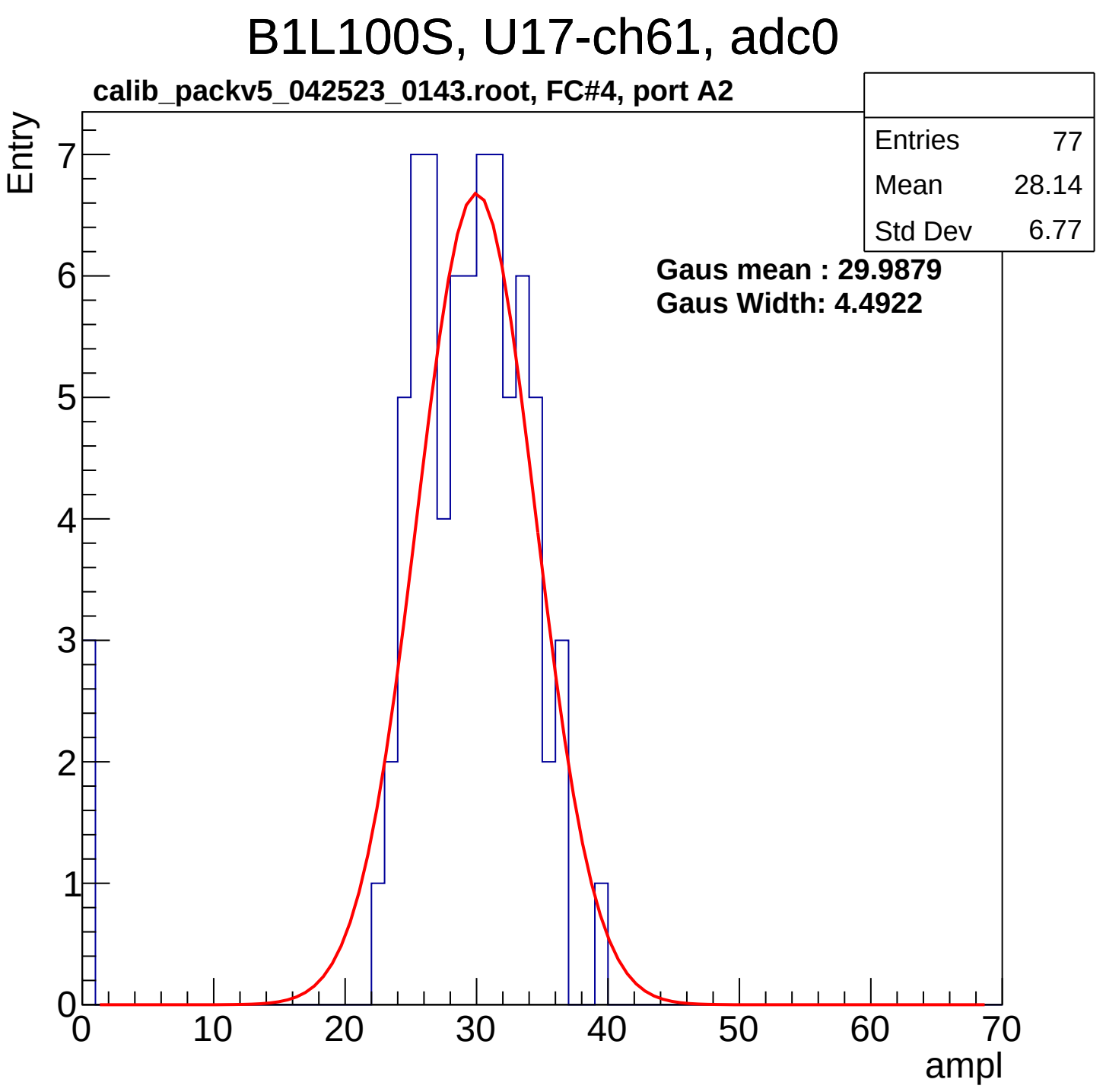
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch61, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 77
Mean 28.14
Std Dev 6.77
Gaus mean : 29.9879
Gaus Width: 4.4922
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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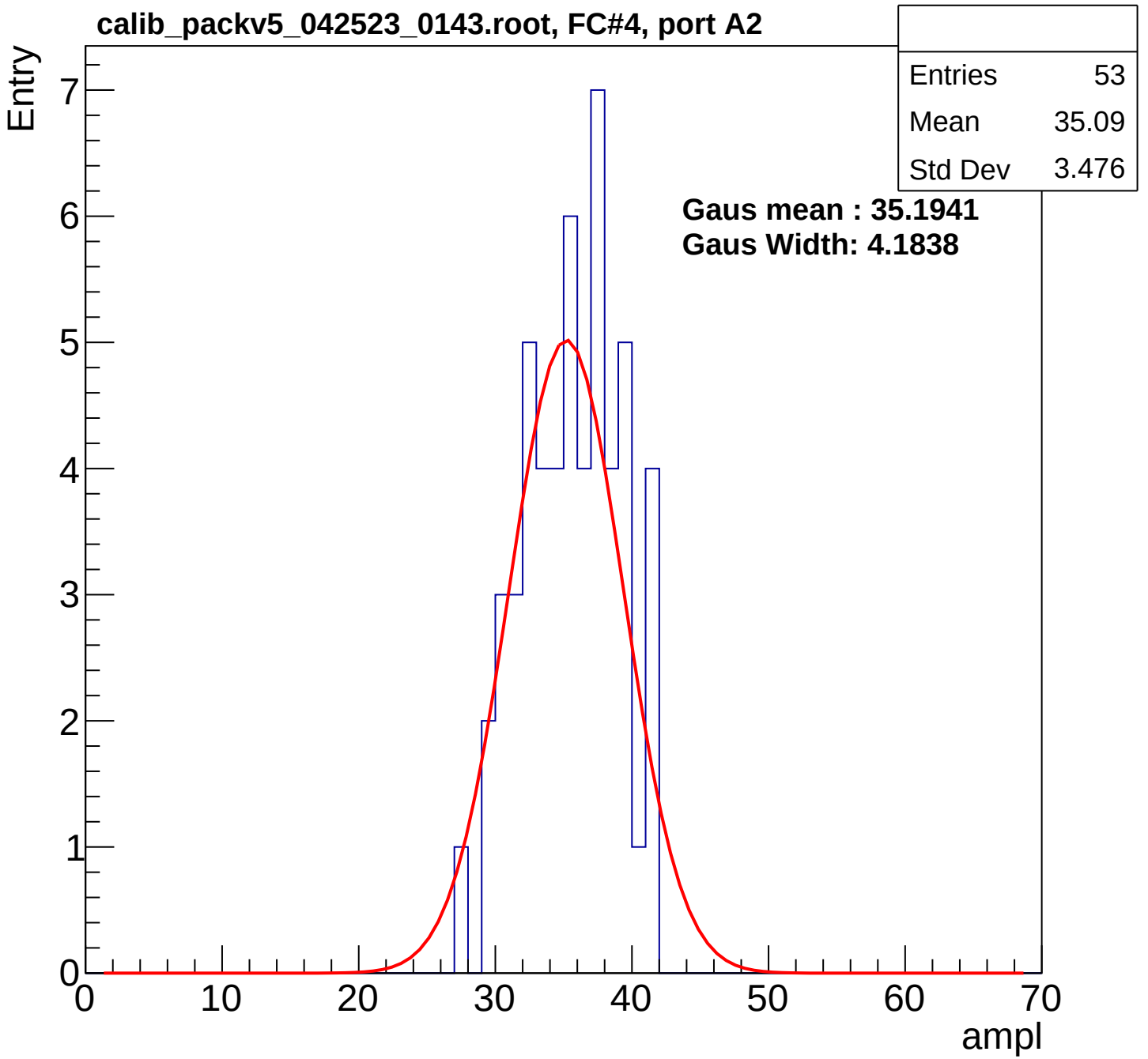
B1L100S, U17-ch61, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 35.09
Std Dev 3.476
Gaus mean : 35.1941
Gaus Width: 4.1838
Entry
ampl
0
1
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3
4
5
6
7
0
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20
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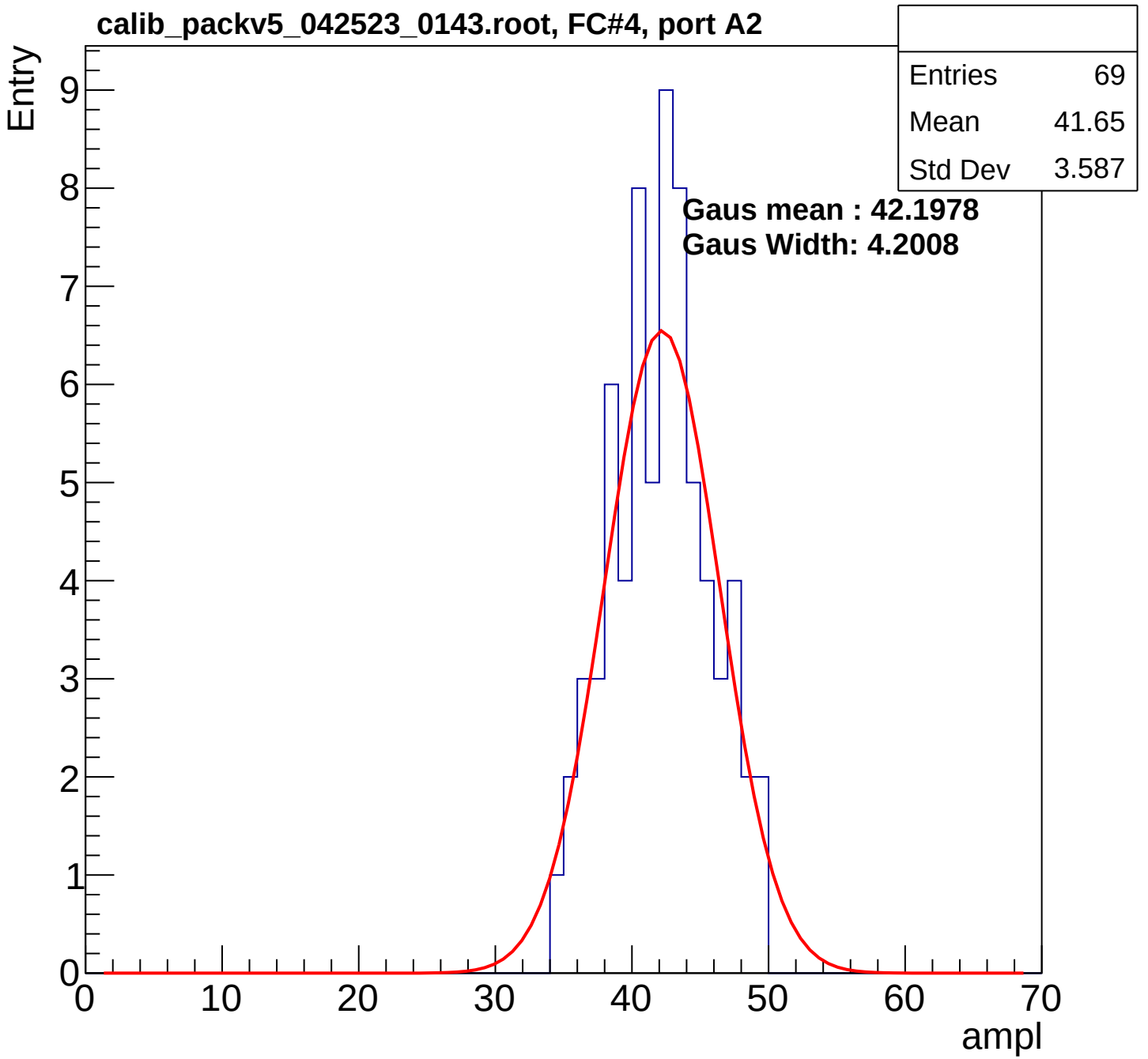
60
70


B1L100S, U17-ch61, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 41.65
Std Dev 3.587
Gaus mean : 42.1978
Gaus Width: 4.2008
Entry
ampl
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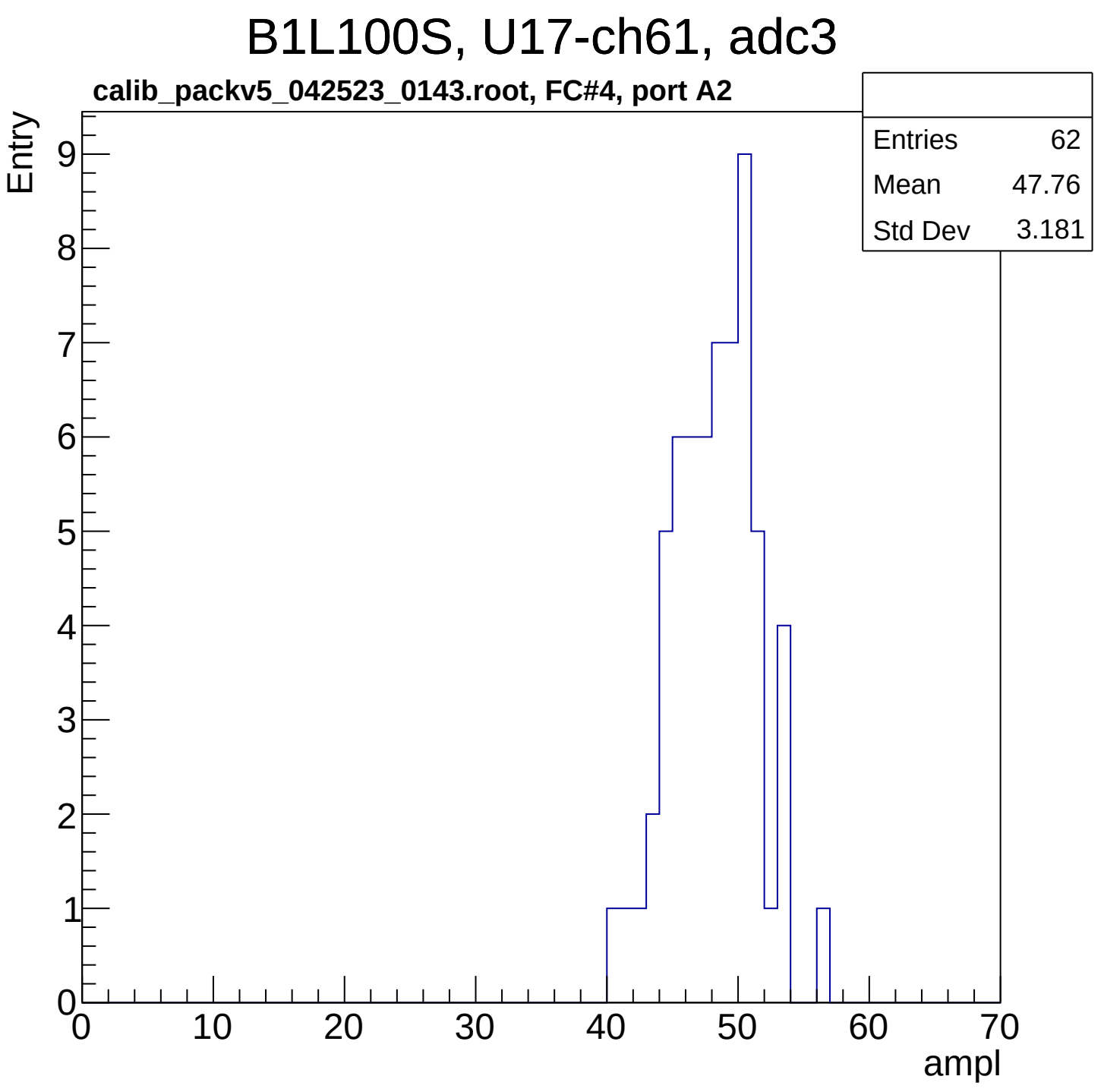
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch61, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 47.76
Std Dev 3.181
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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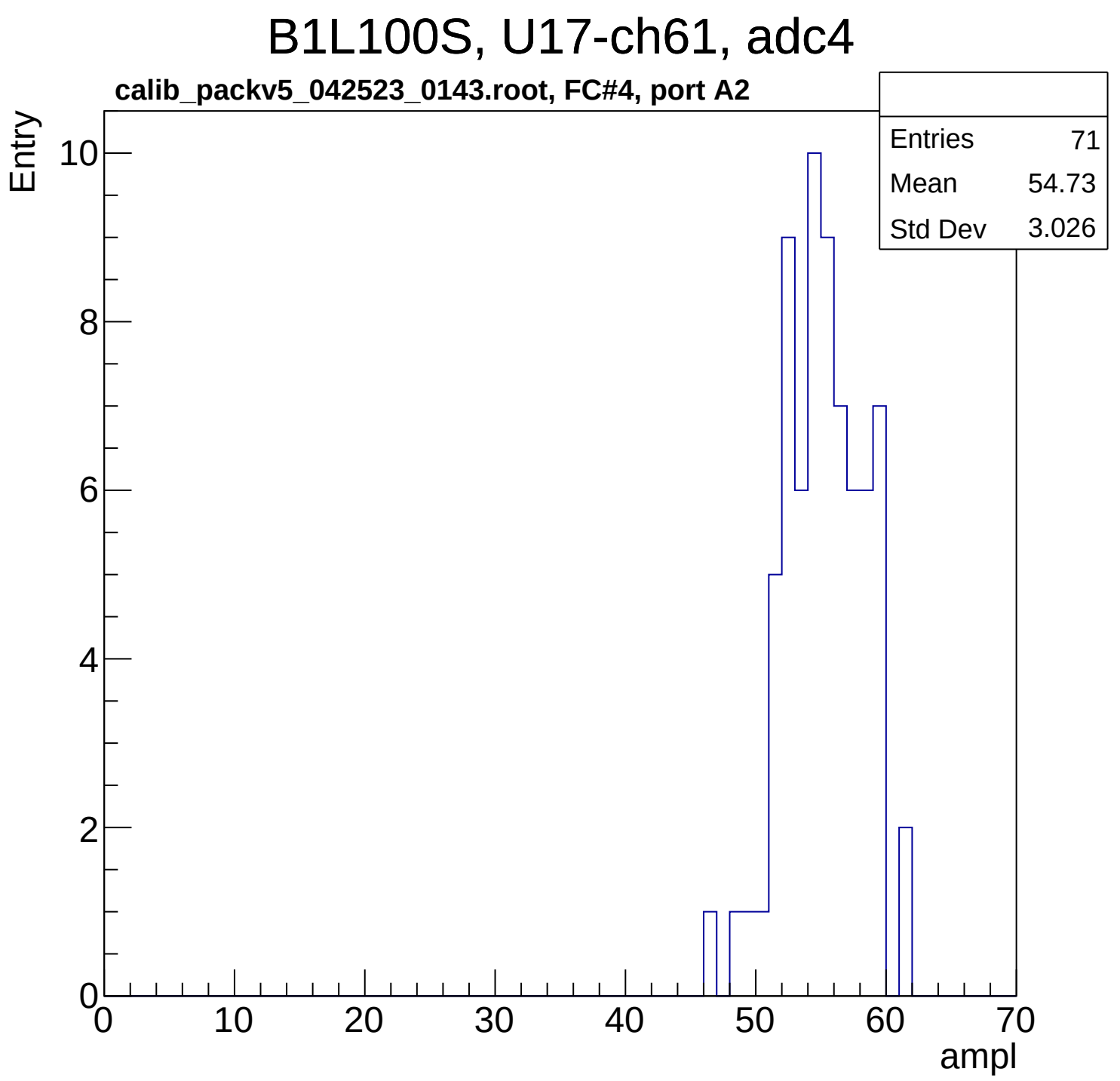
B1L100S, U17-ch61, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 54.73
Std Dev 3.026
Entry
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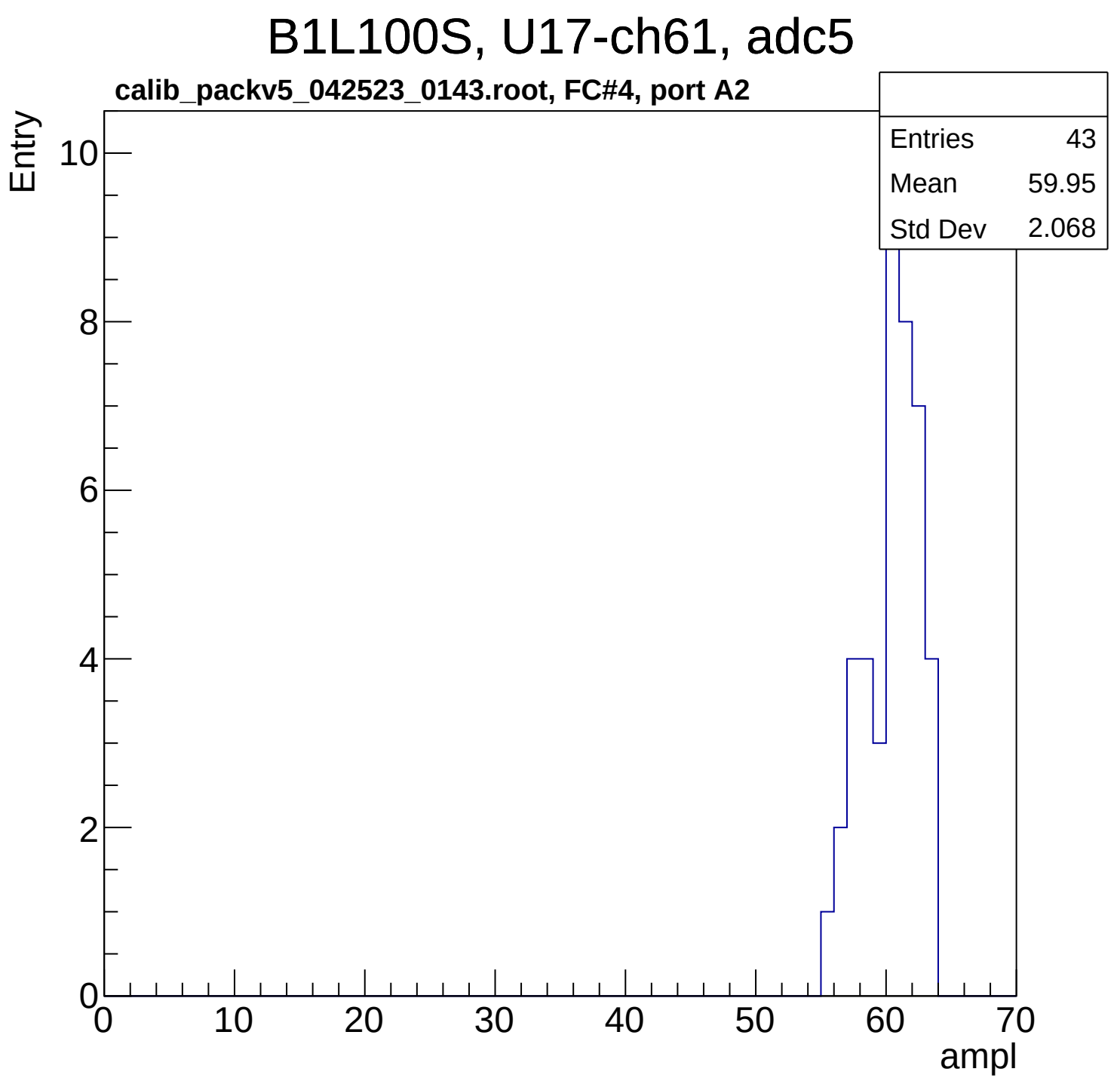
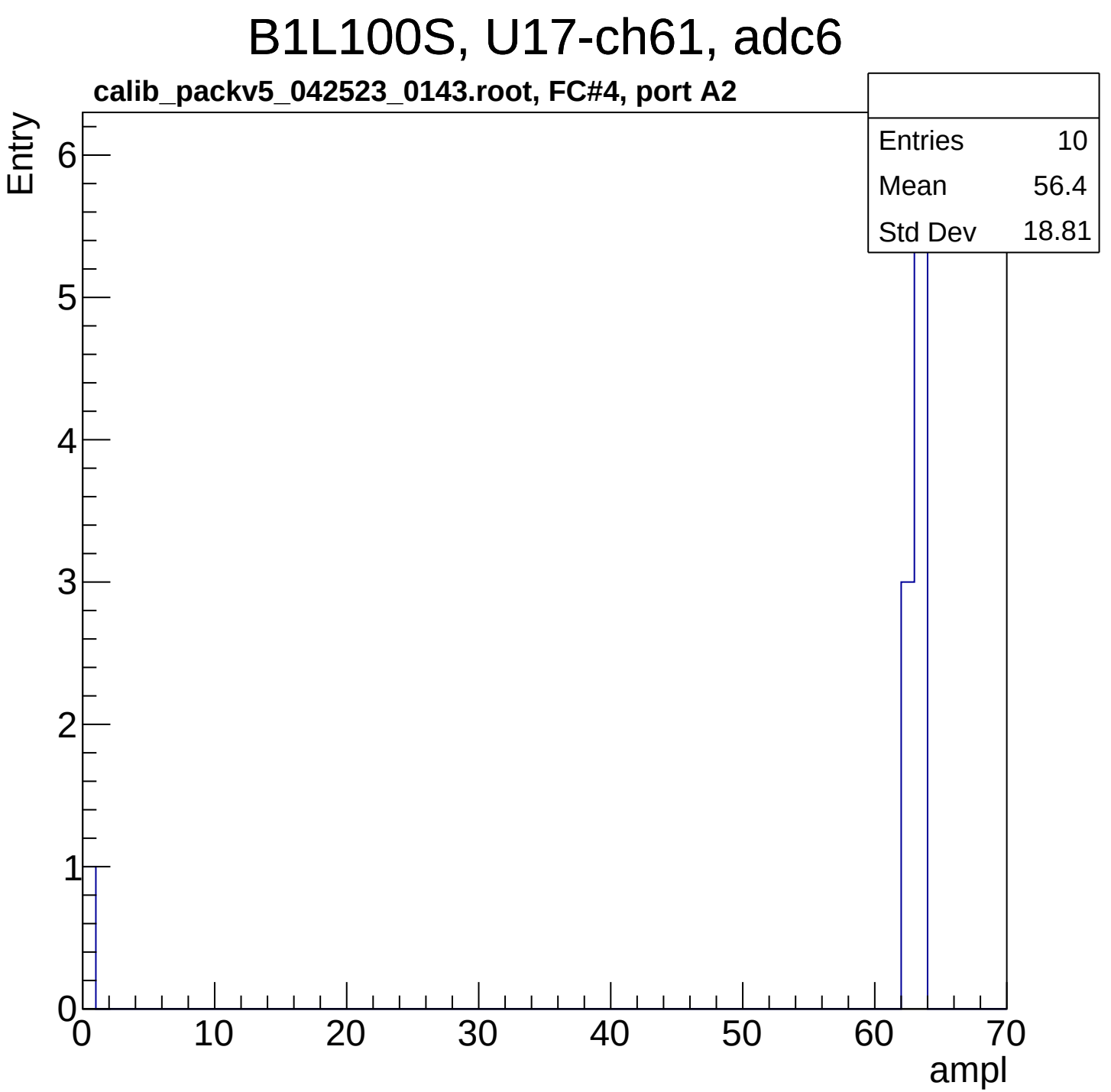
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch61, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 43
Mean 59.95
Std Dev 2.068
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch61, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 10
Mean 56.4
Std Dev 18.81
Entry
0
1
2
3
4
5
6
0
10
20
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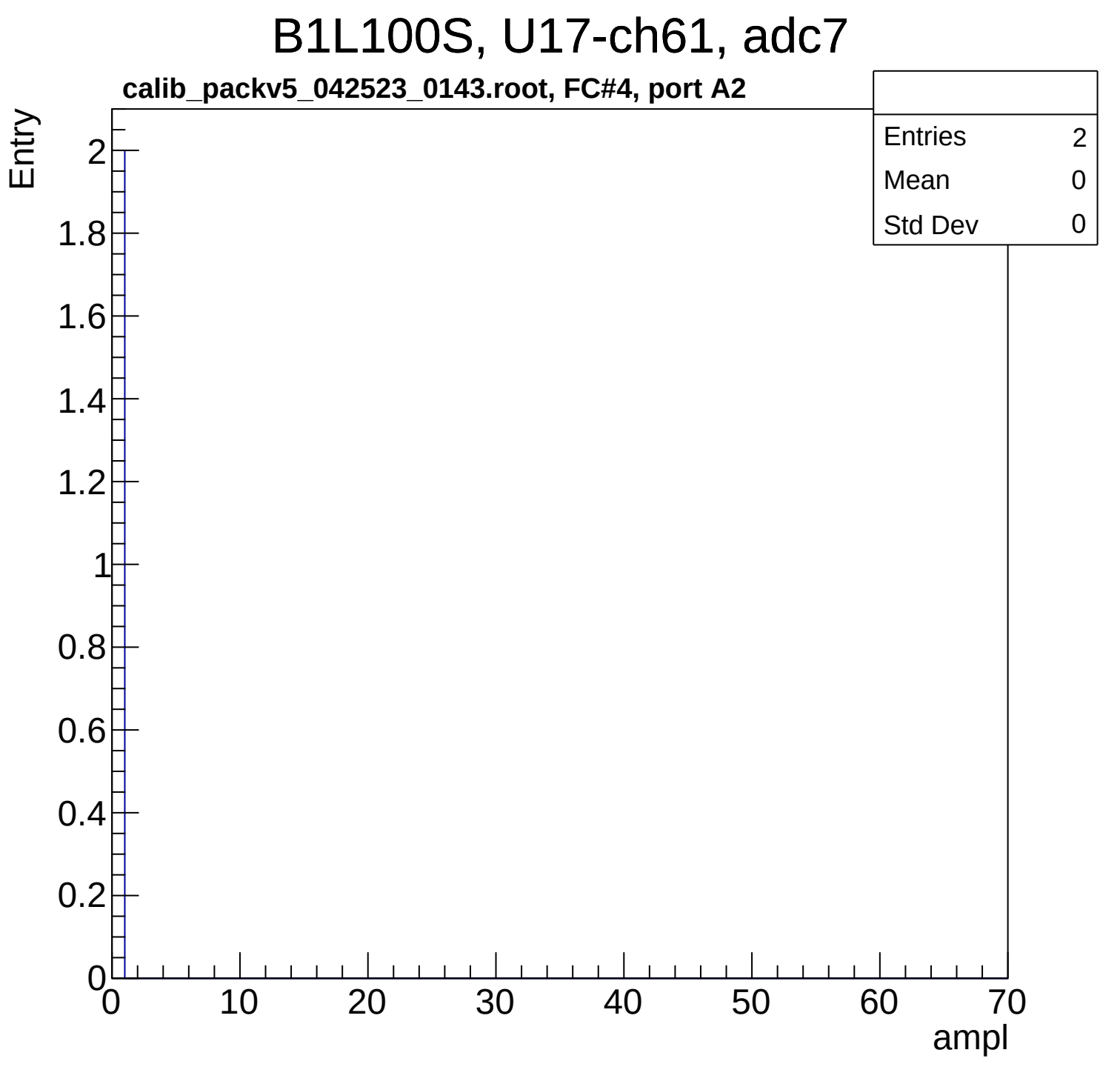
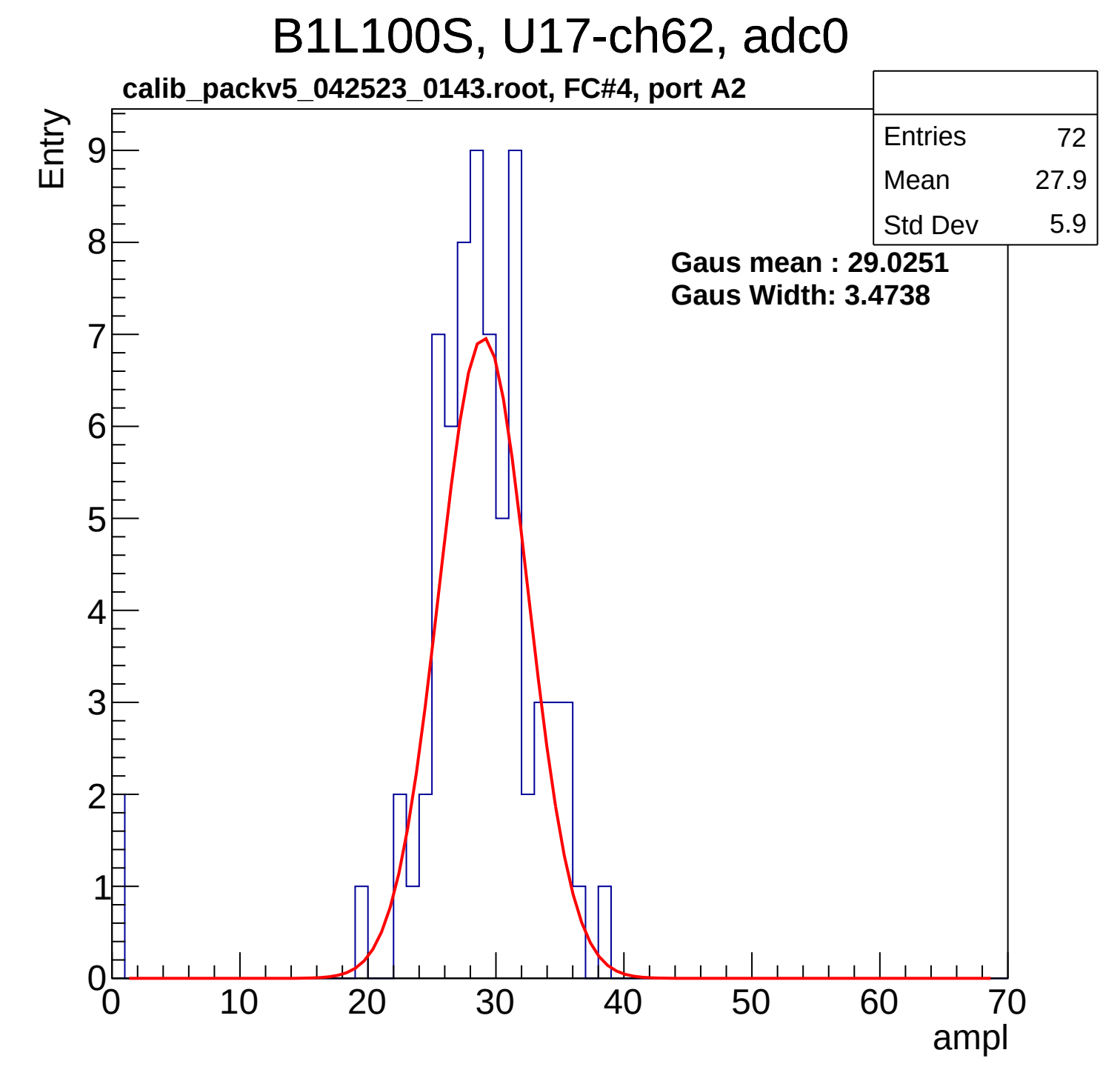
50
60
70
ampl


B1L100S, U17-ch61, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch62, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 27.9
Std Dev 5.9
Gaus mean : 29.0251
Gaus Width: 3.4738
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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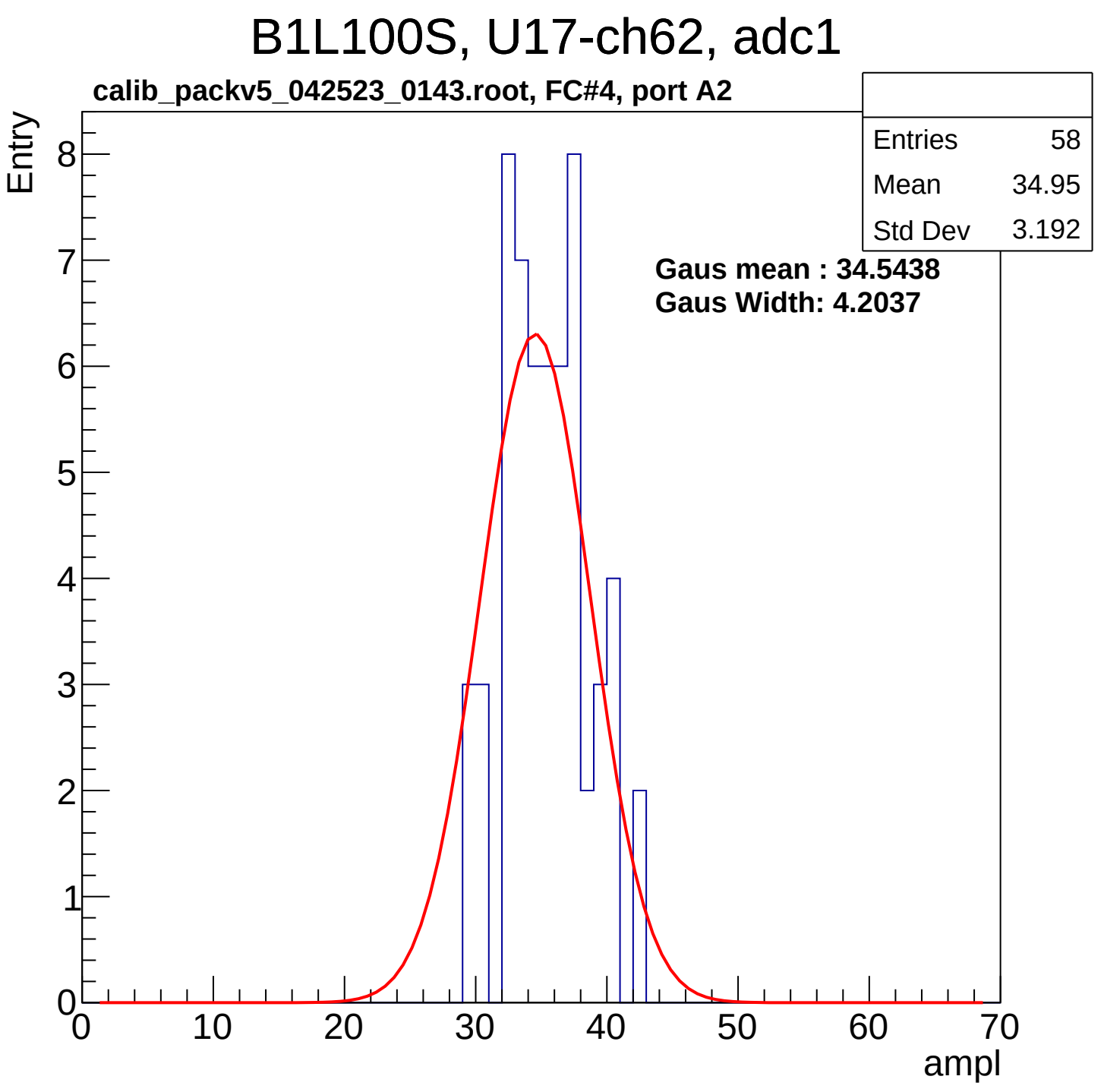
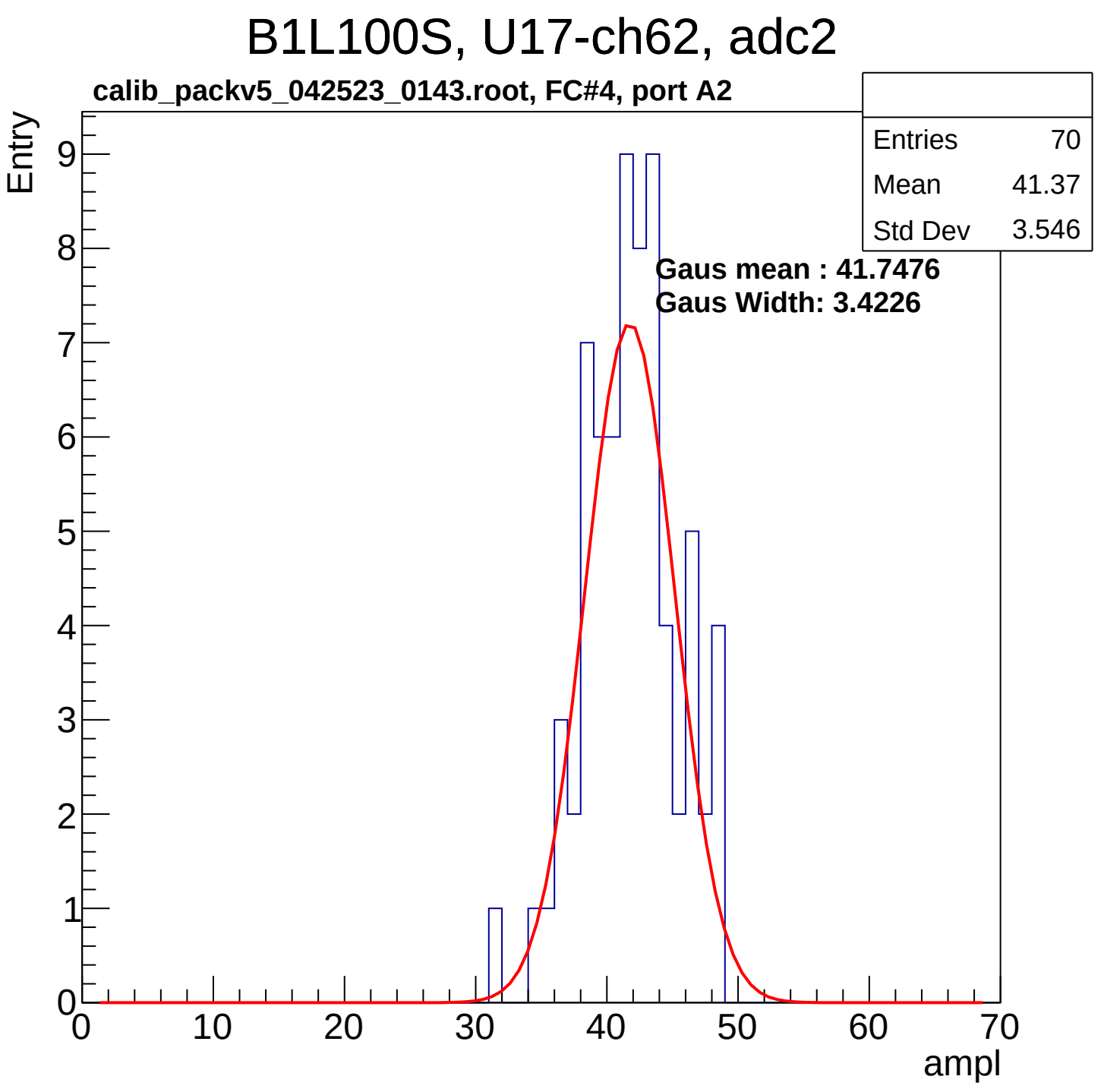

B1L100S, U17-ch62, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 34.95
Std Dev 3.192
Gaus mean : 34.5438
Gaus Width: 4.2037
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch62, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 41.37
Std Dev 3.546
Gaus mean : 41.7476
Gaus Width: 3.4226
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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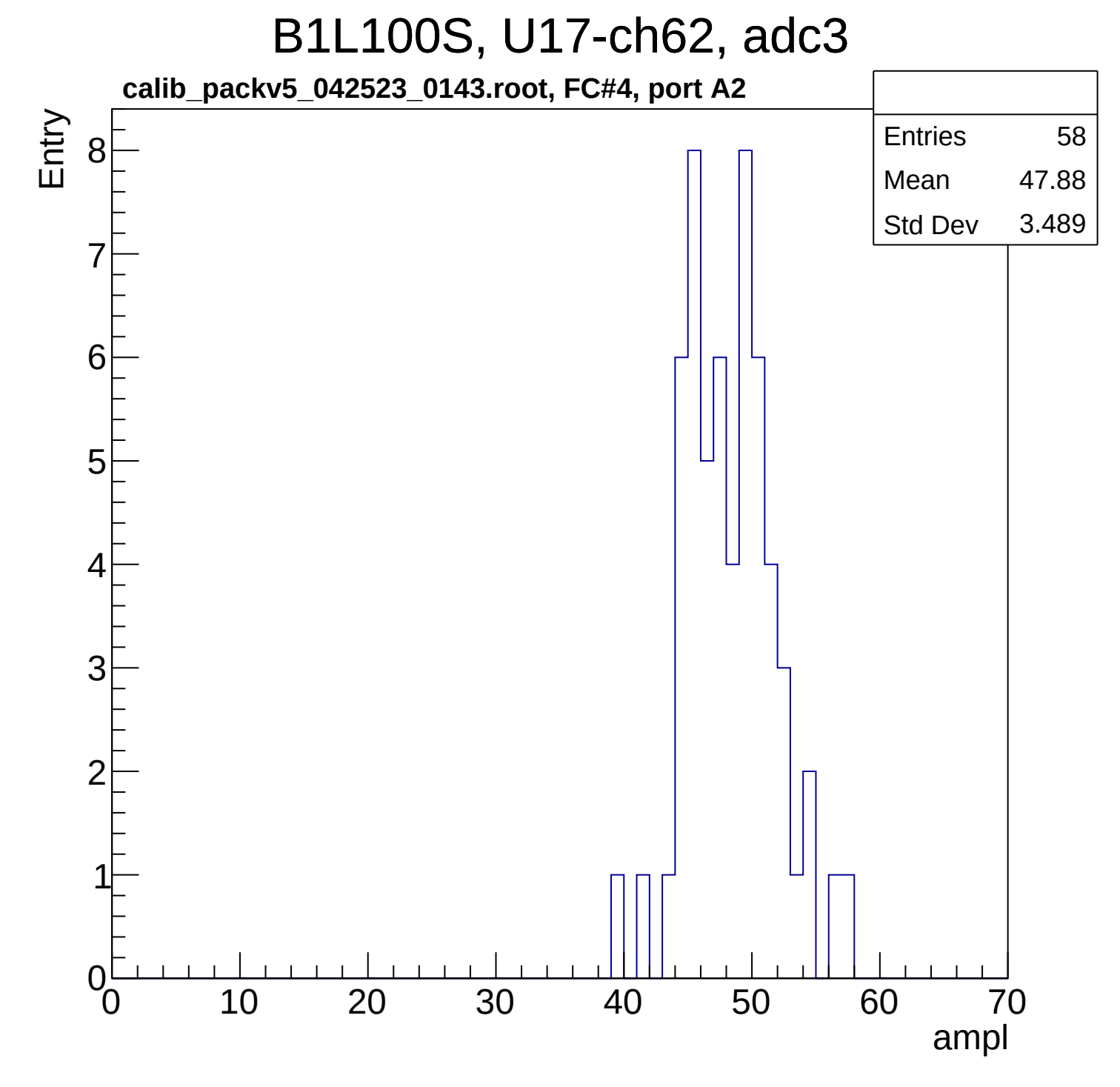
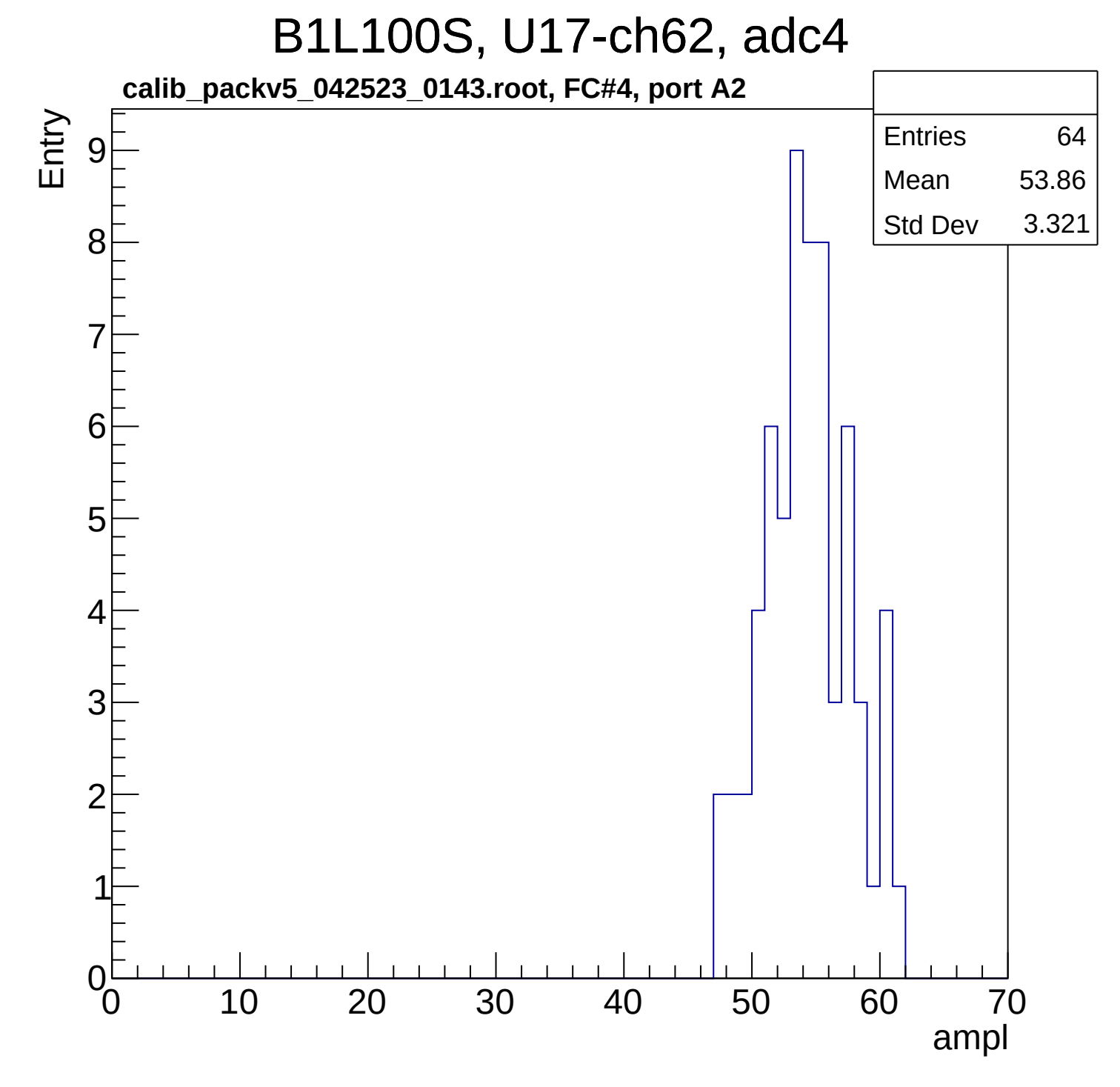

B1L100S, U17-ch62, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 47.88
Std Dev 3.489
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch62, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 53.86
Std Dev 3.321
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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20
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60
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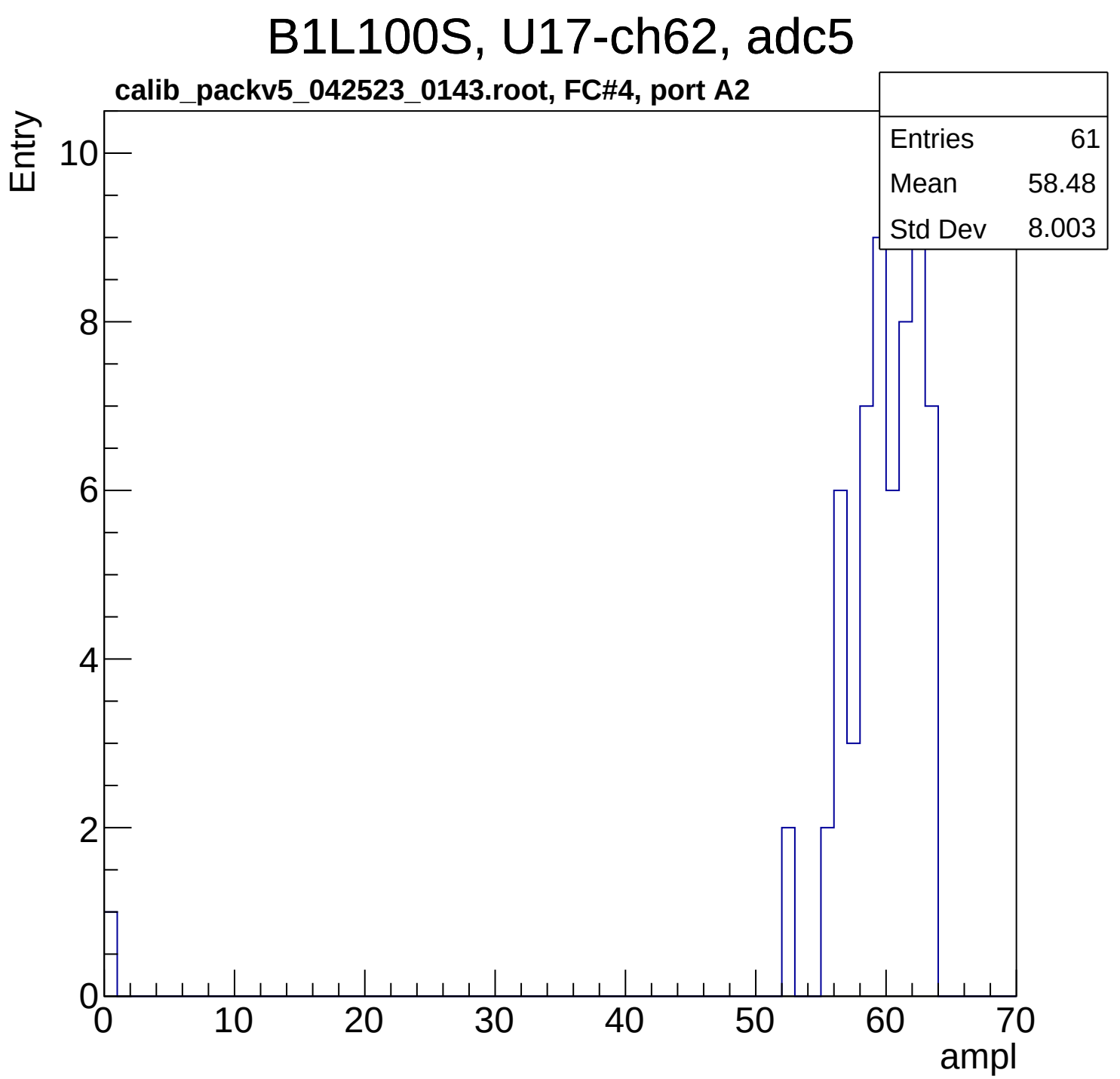
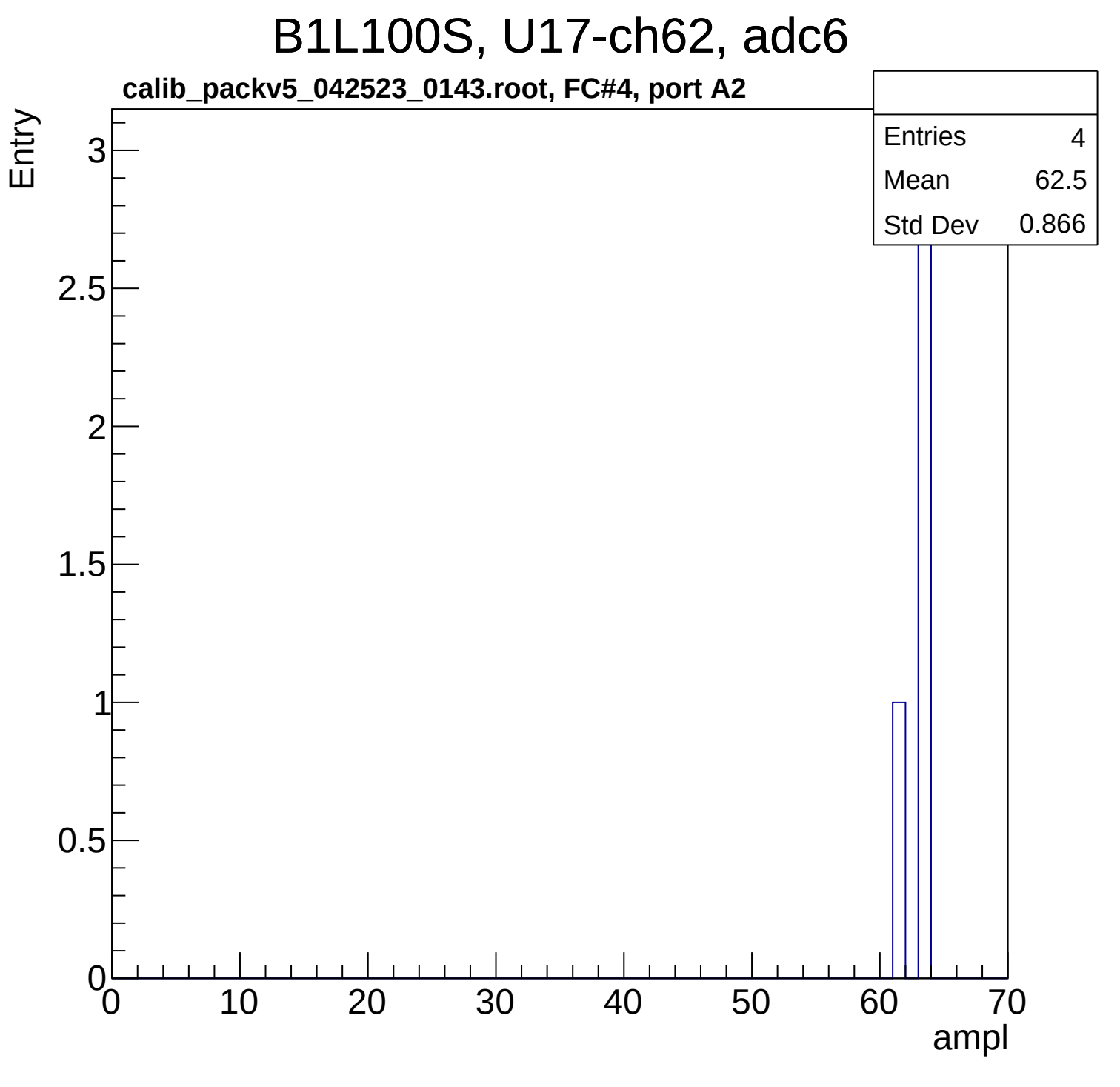
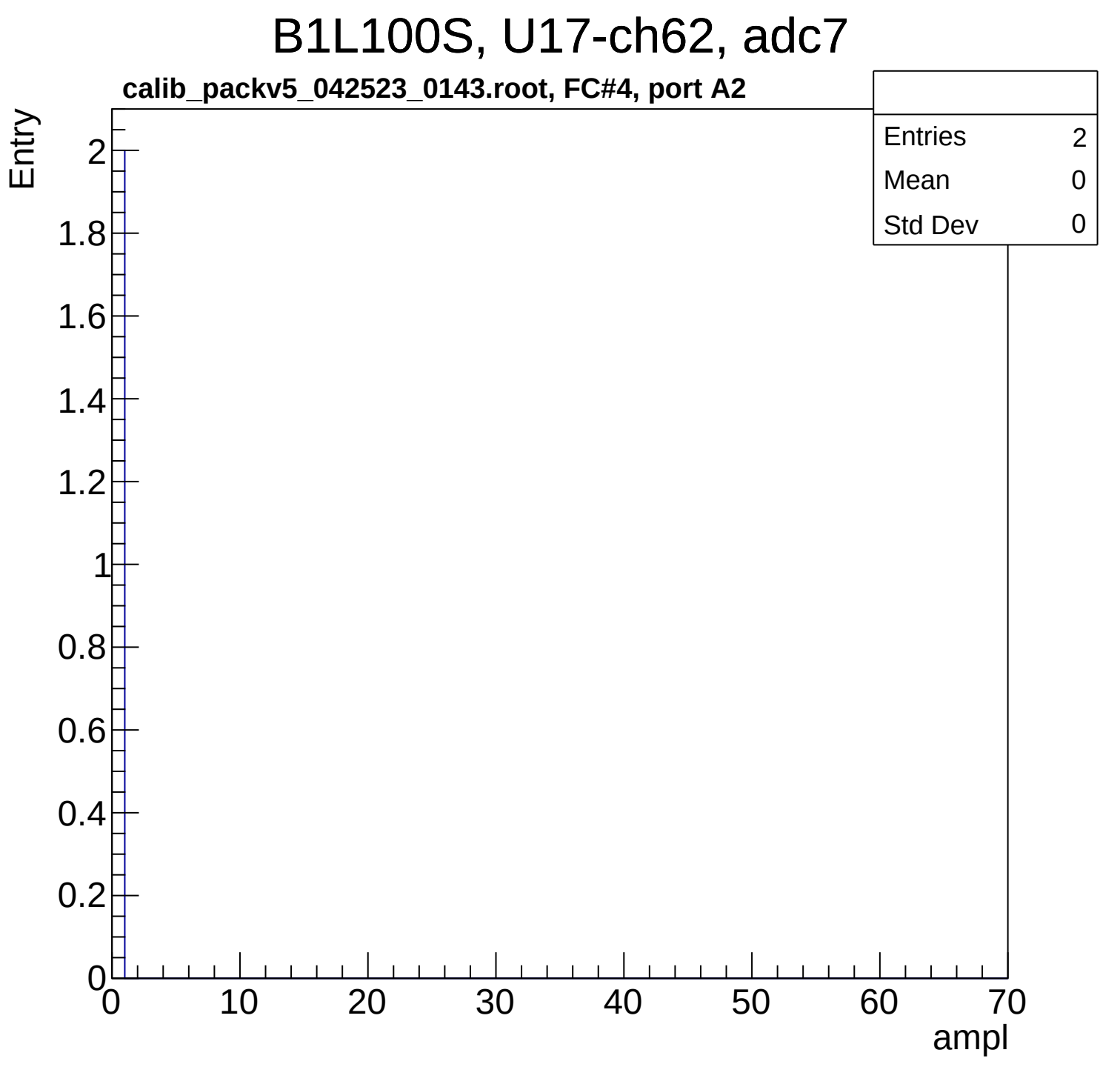
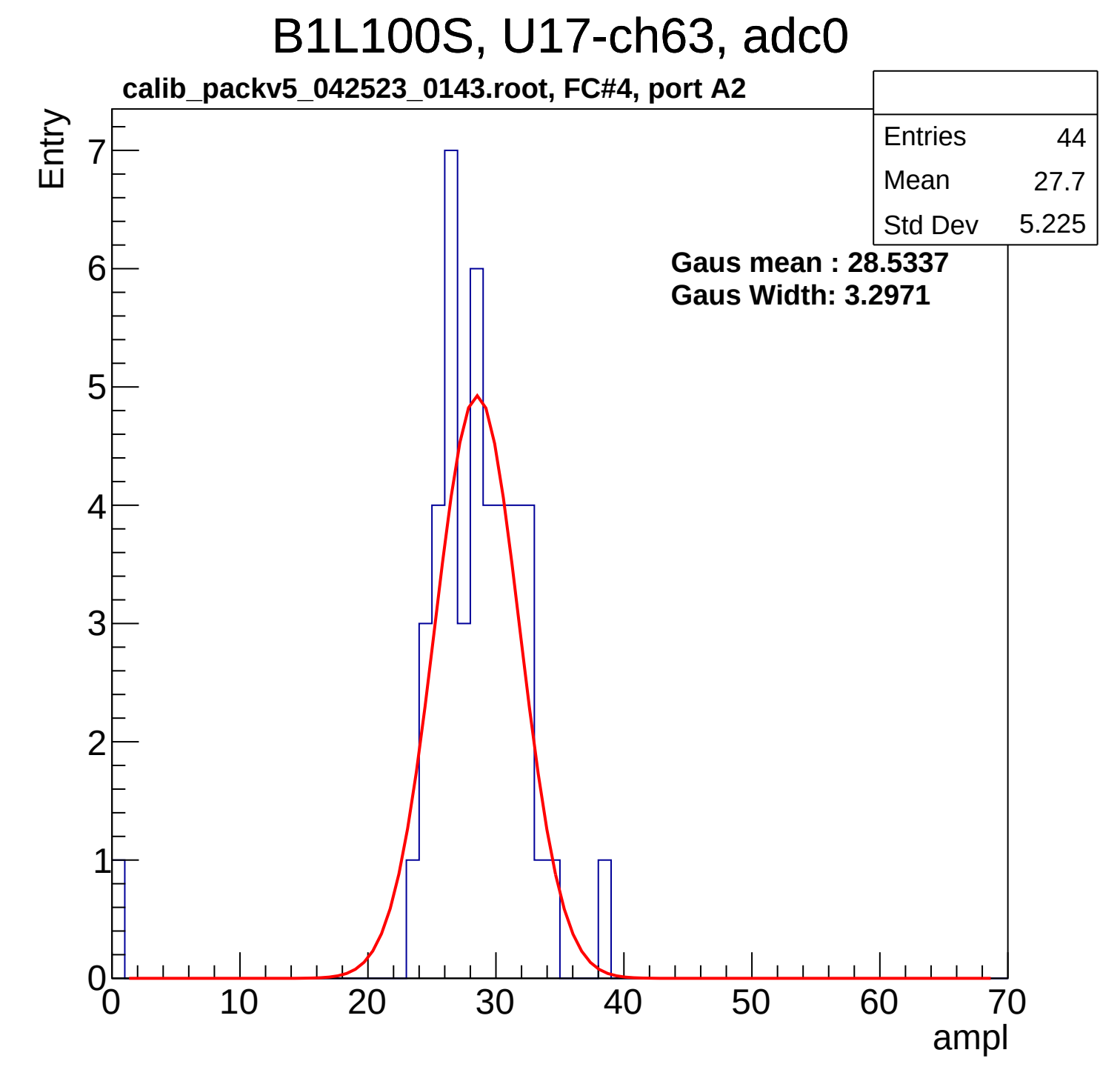
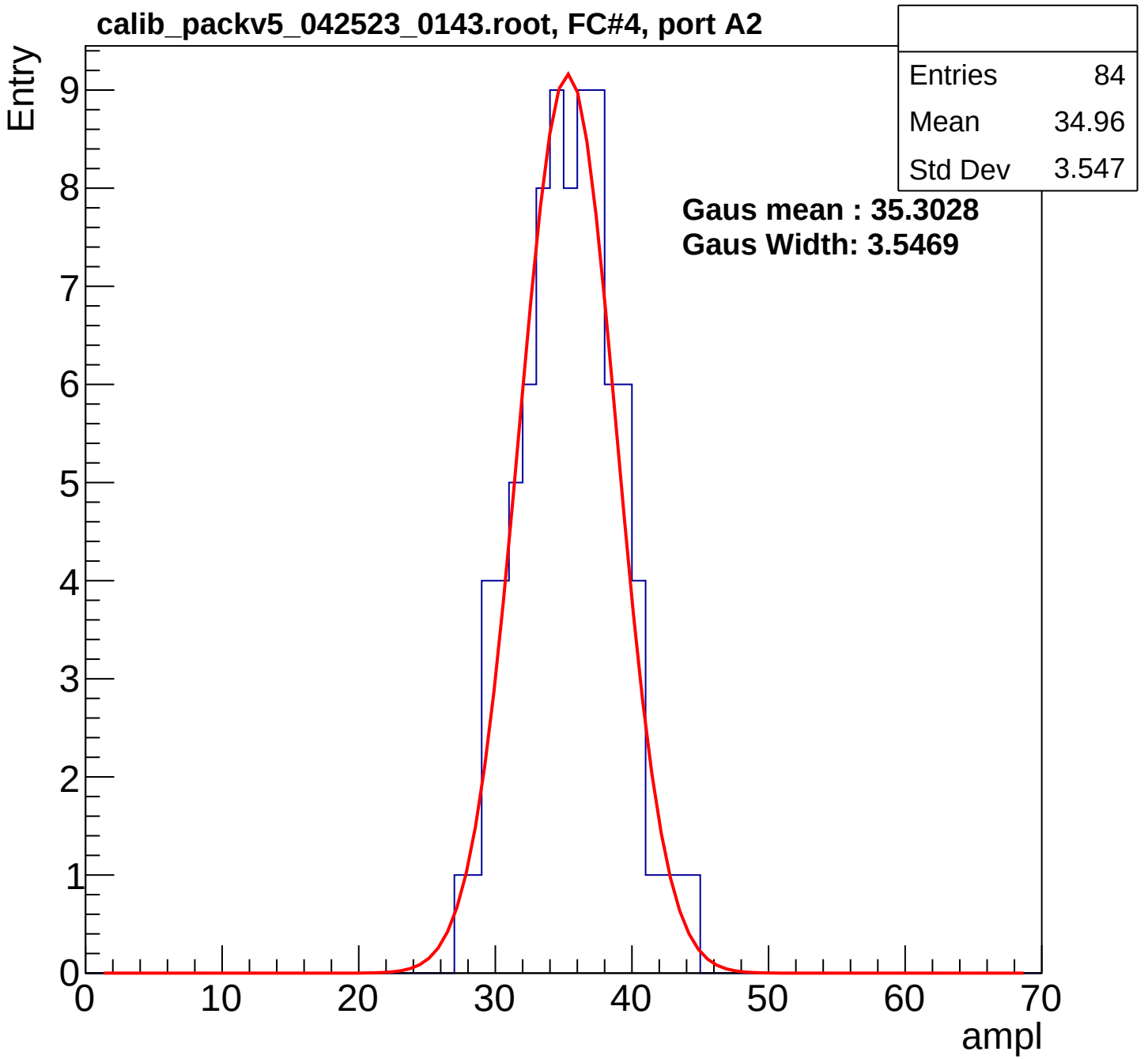

B1L100S, U17-ch62, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 58.48
Std Dev 8.003
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U17-ch62, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 4
Mean 62.5
Std Dev 0.866
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L100S, U17-ch62, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch63, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 44
Mean 27.7
Std Dev 5.225
Gaus mean : 28.5337
Gaus Width: 3.2971
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U17-ch63, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 84
Mean 34.96
Std Dev 3.547
Gaus mean : 35.3028
Gaus Width: 3.5469
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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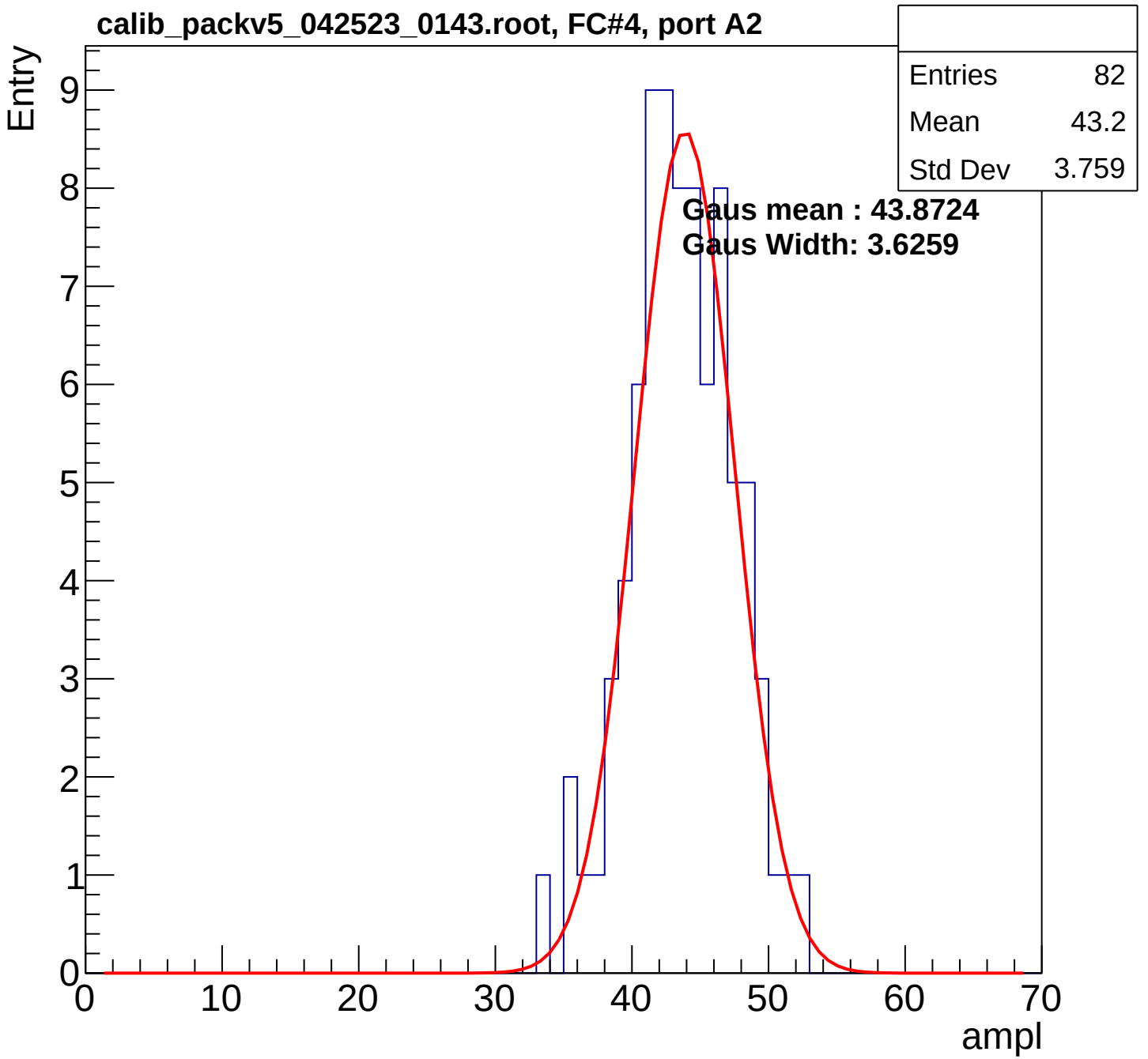
B1L100S, U17-ch63, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 82
Mean 43.2
Std Dev 3.759
Gaus mean : 43.8724
Gaus Width: 3.6259
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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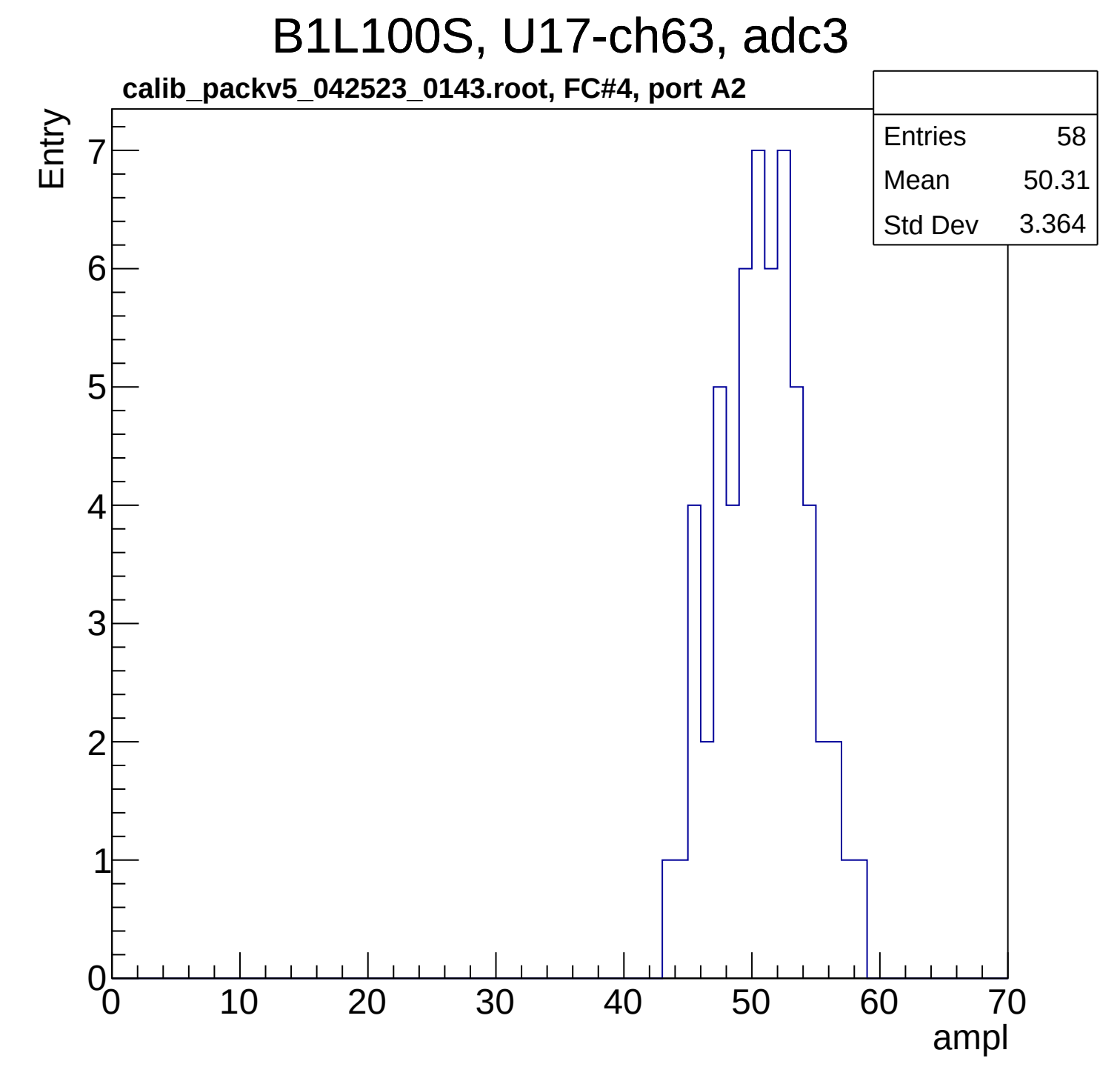
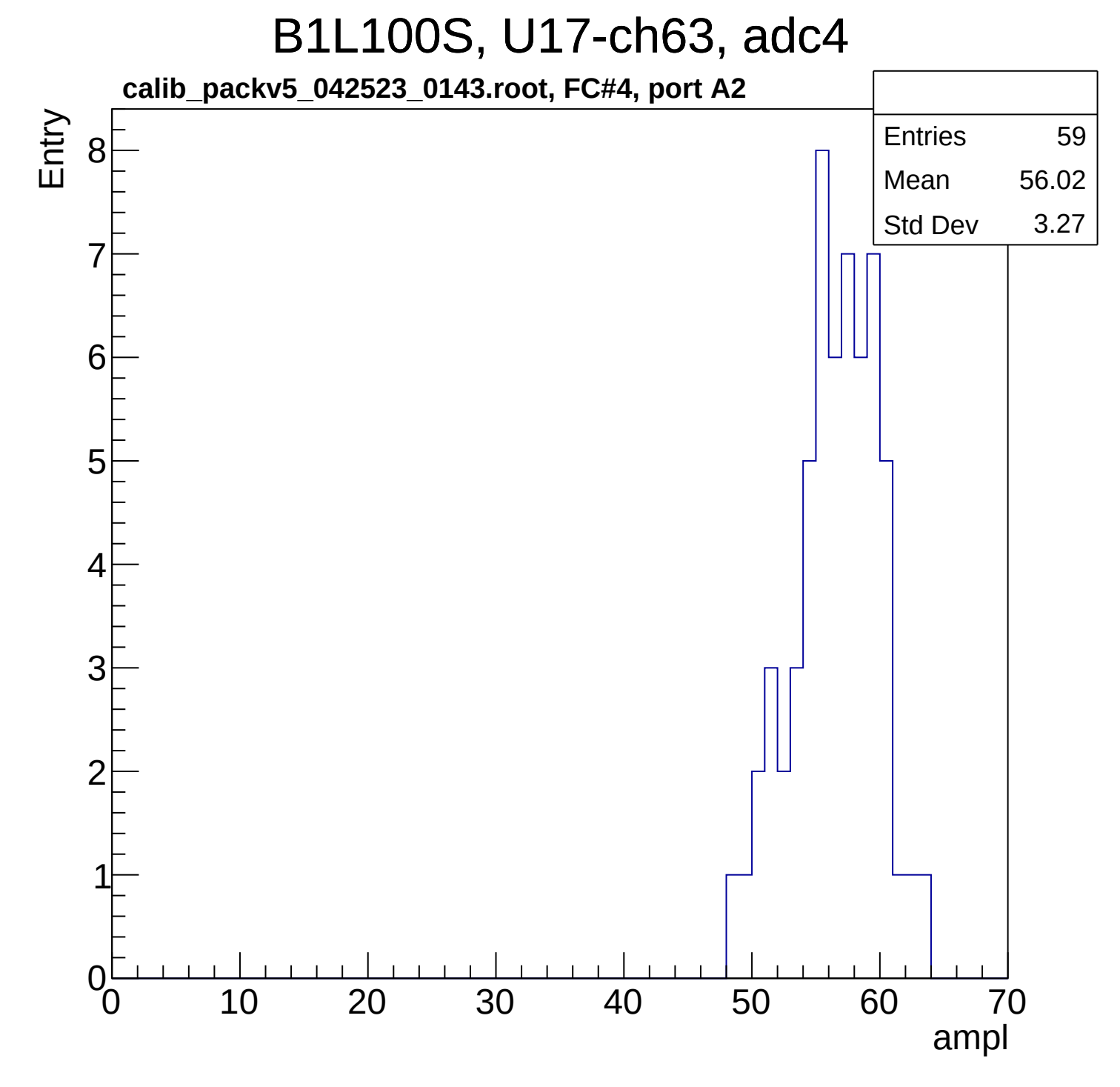
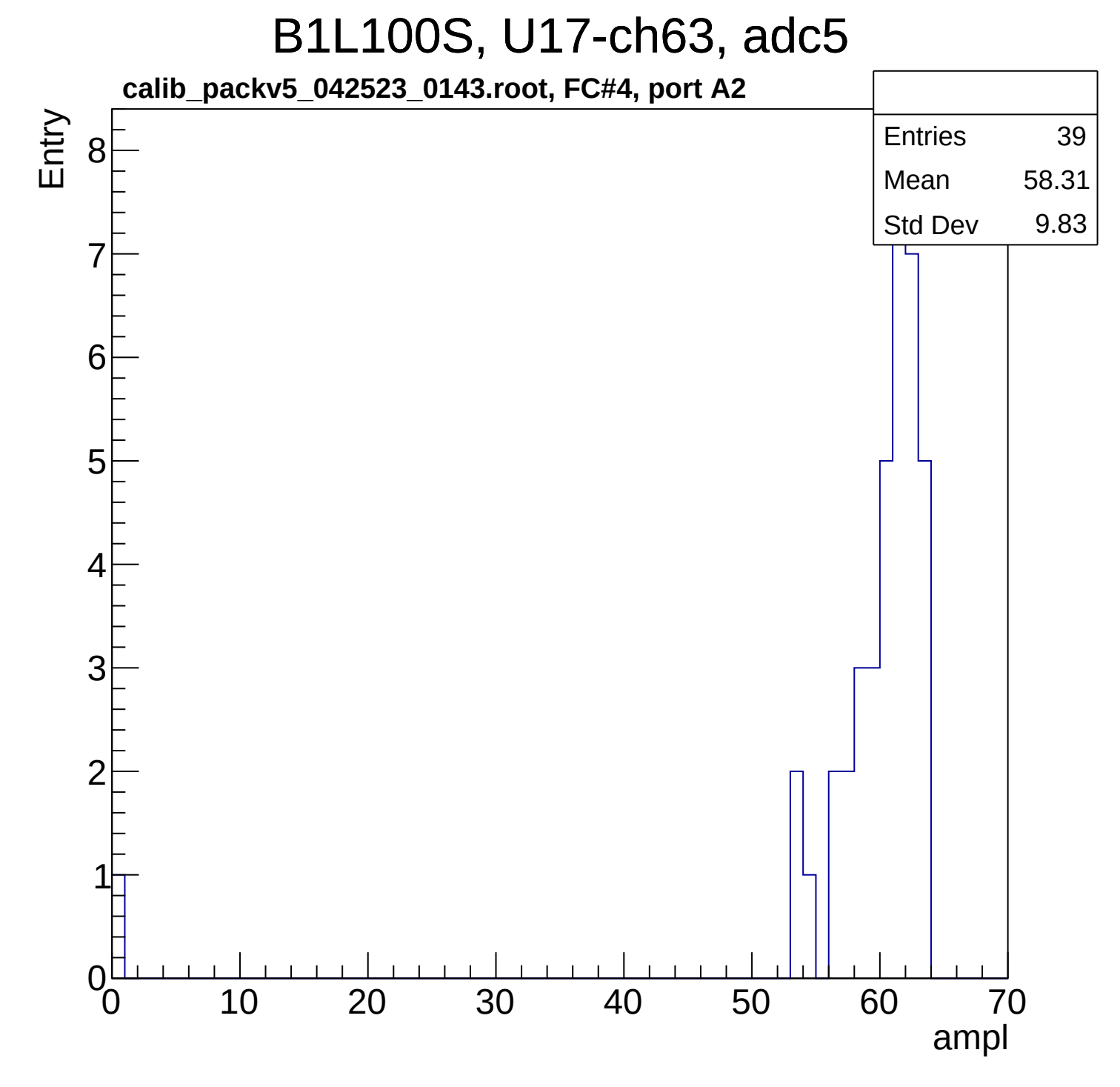

B1L100S, U17-ch63, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 50.31
Std Dev 3.364
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U17-ch63, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 56.02
Std Dev 3.27
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch63, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 39
Mean 58.31
Std Dev 9.83
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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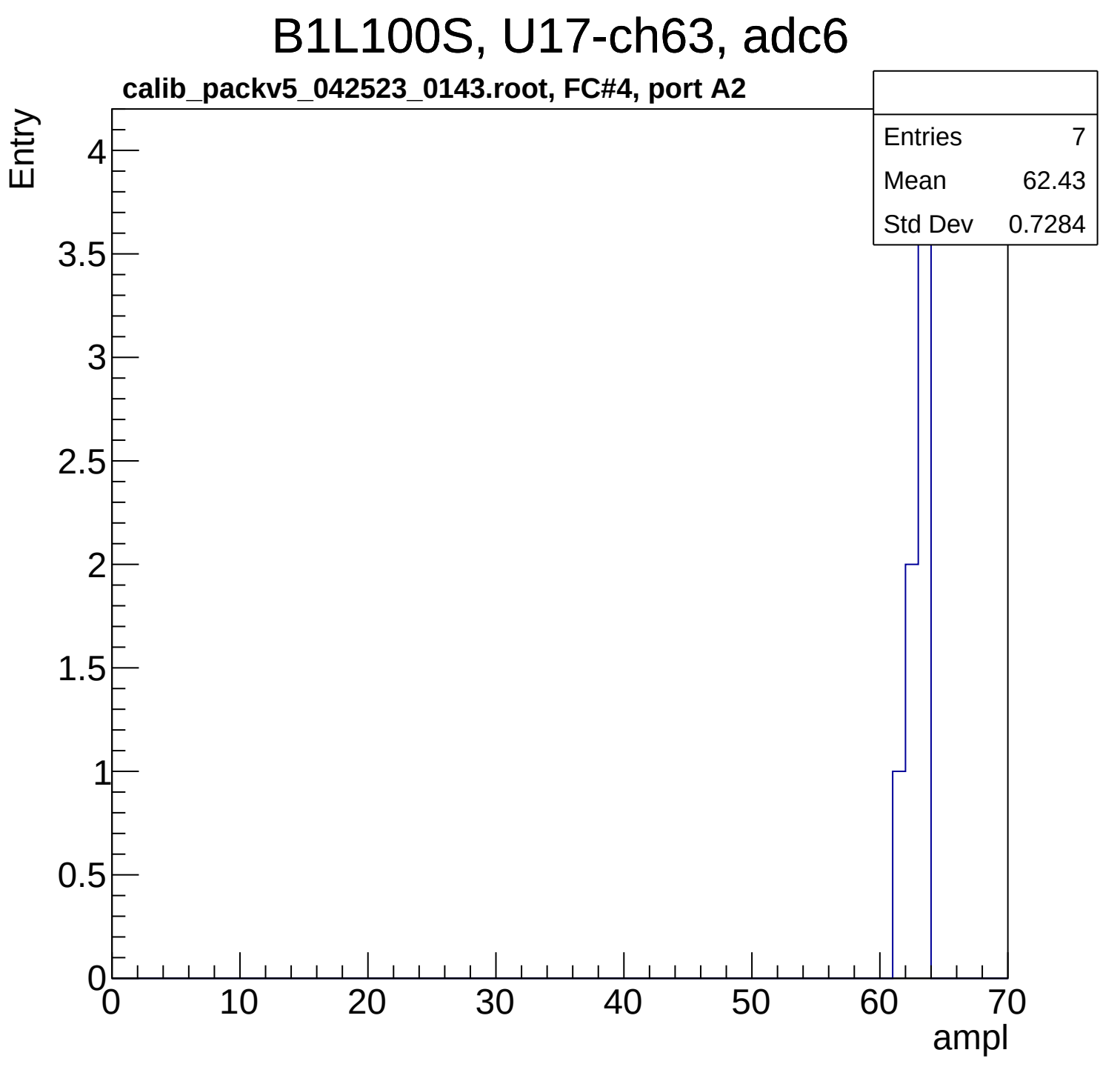
40
50
60
70


B1L100S, U17-ch63, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 7
Mean 62.43
Std Dev 0.7284
Entry
ampl
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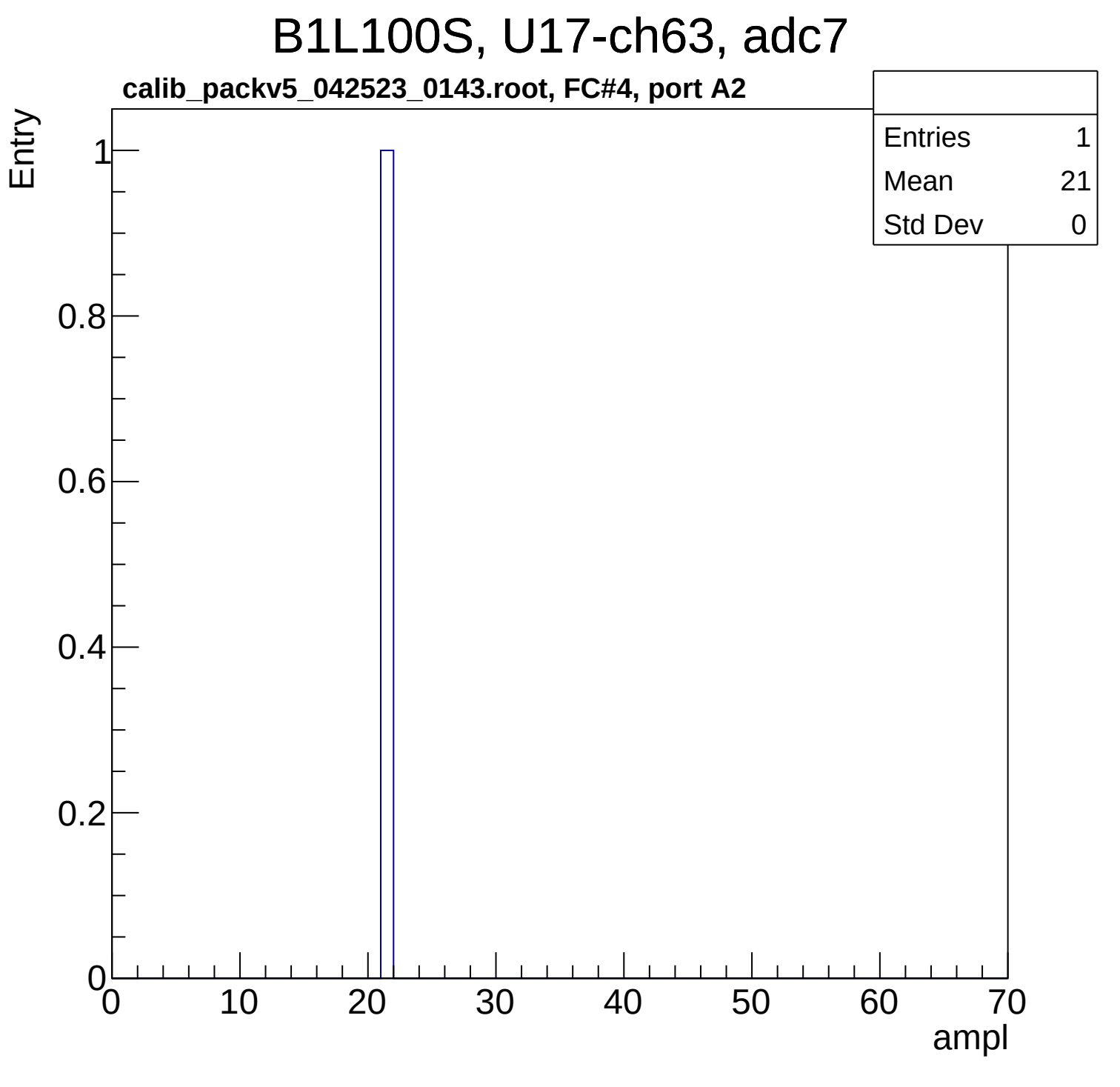
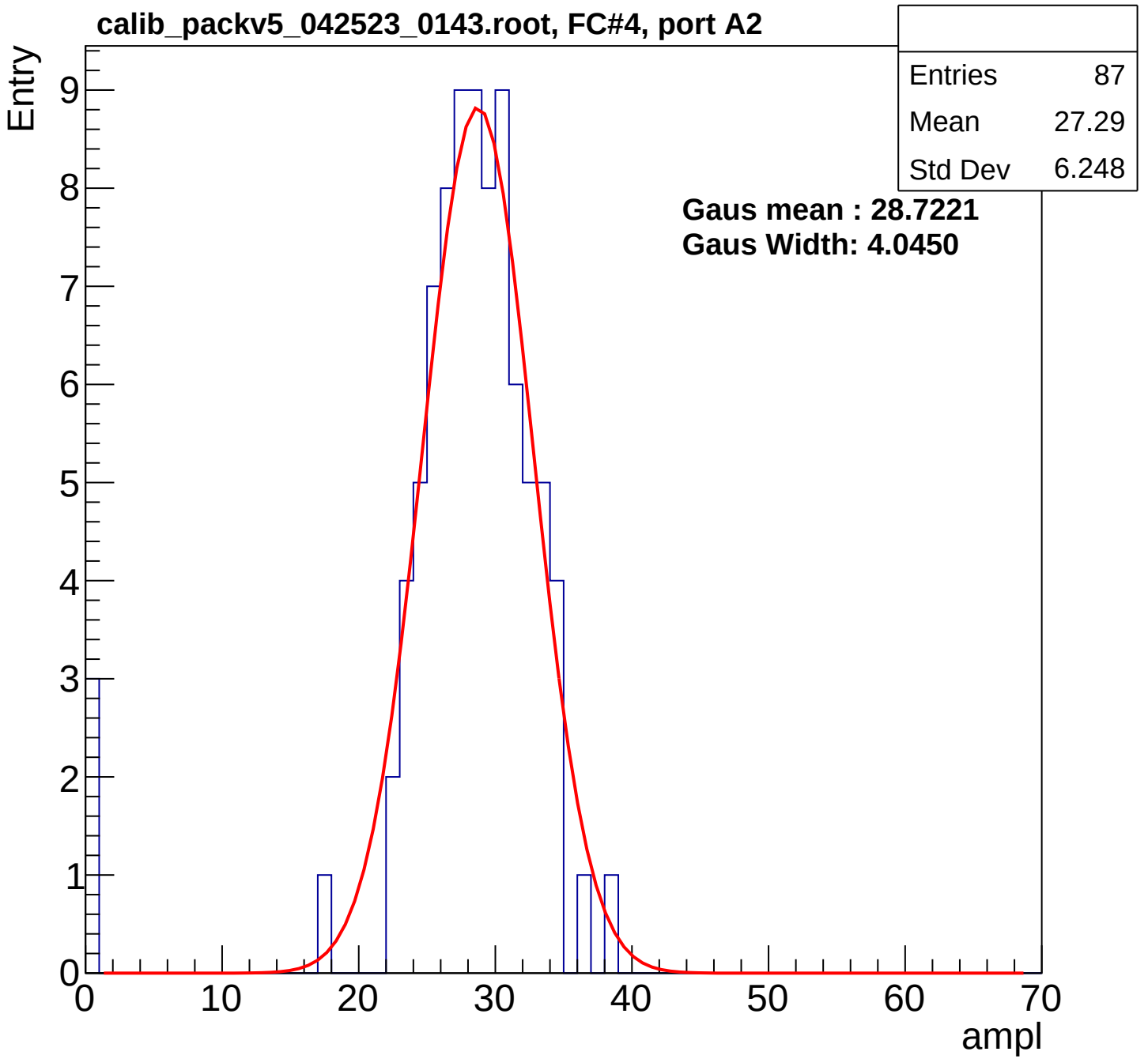
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L100S, U17-ch63, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 21
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch64, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 87
Mean 27.29
Std Dev 6.248
Gaus mean : 28.7221
Gaus Width: 4.0450
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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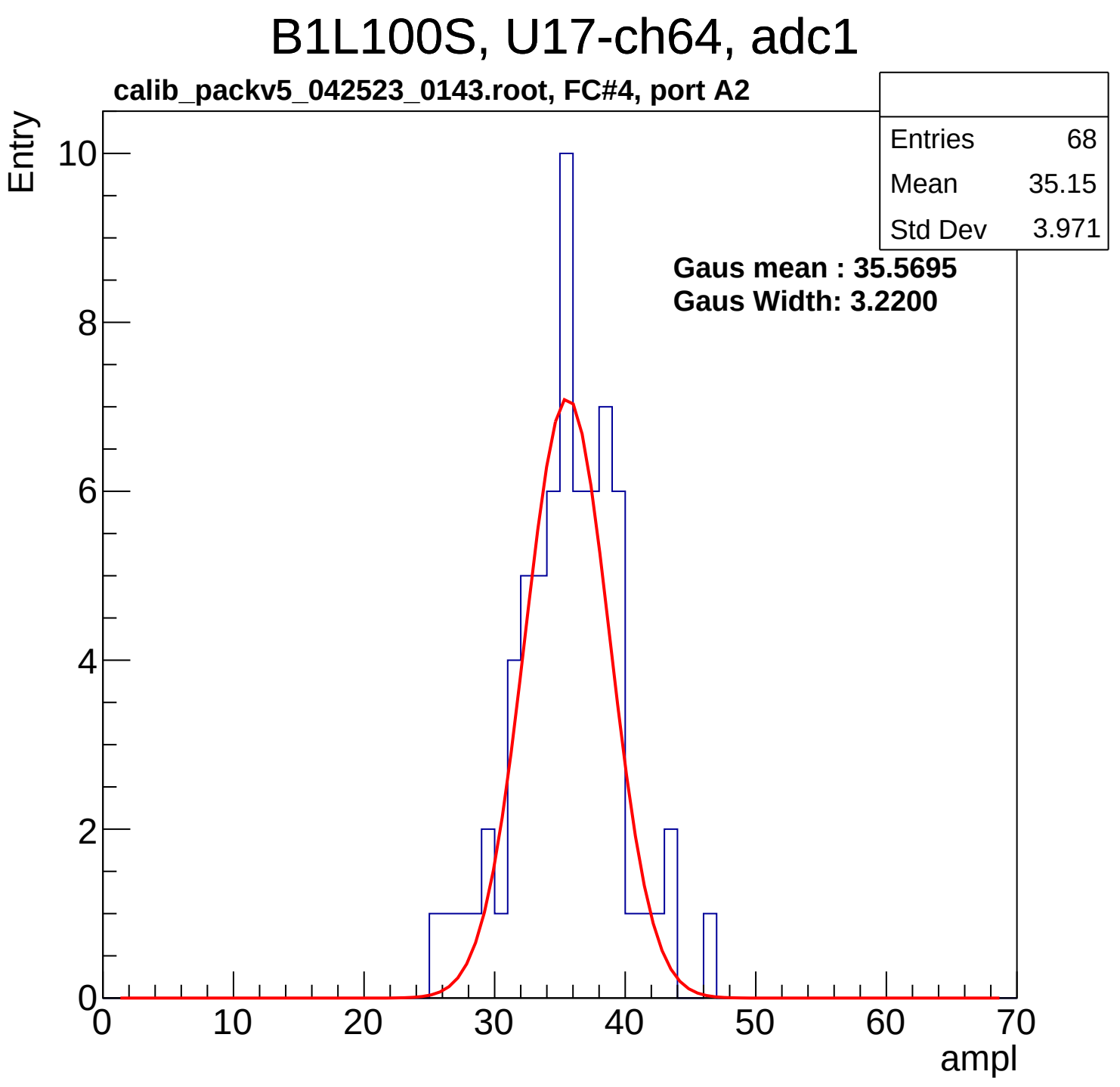
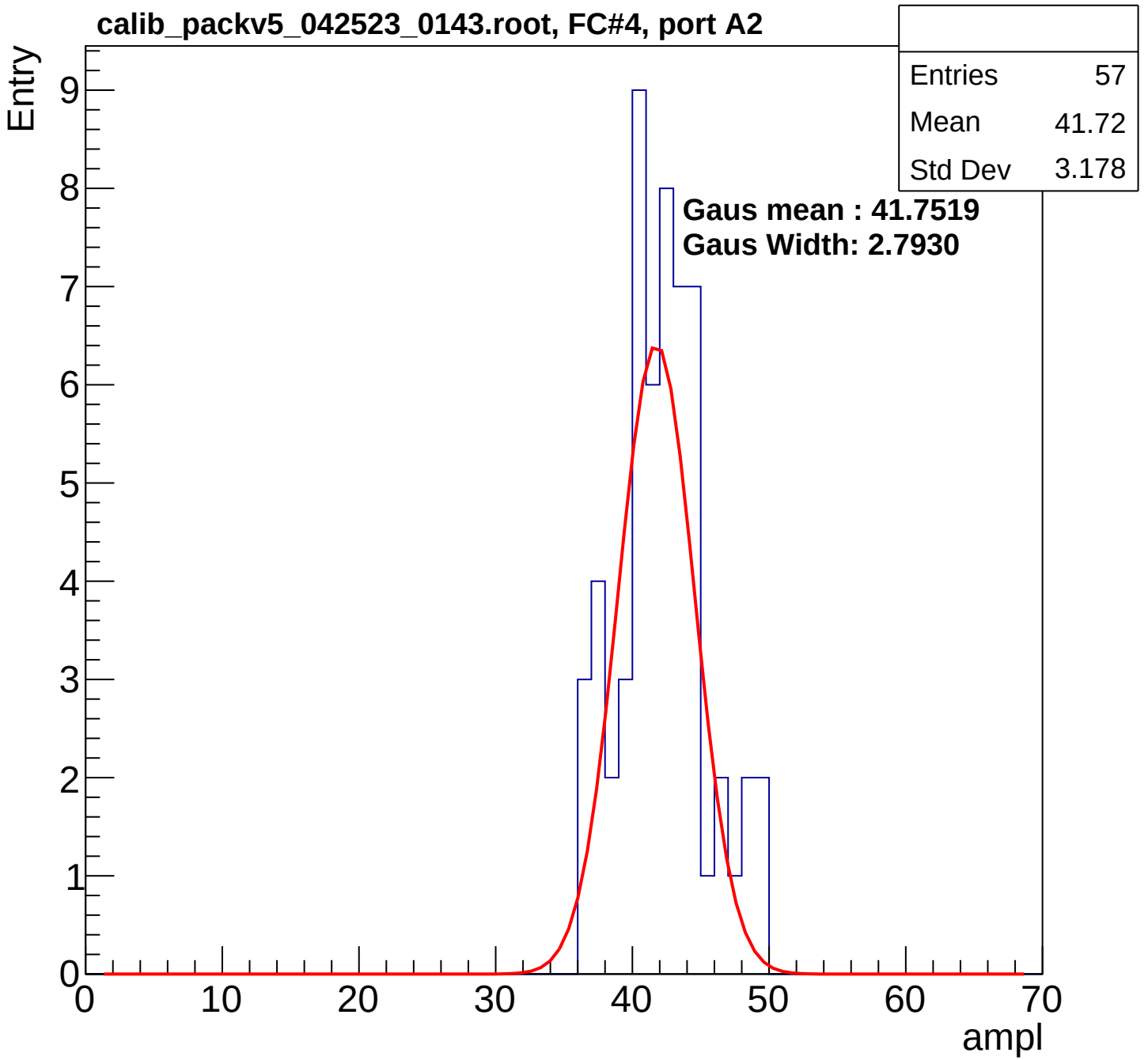
20
30
40
50
60
70


B1L100S, U17-ch64, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 35.15
Std Dev 3.971
Gaus mean : 35.5695
Gaus Width: 3.2200
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U17-ch64, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 41.72
Std Dev 3.178
Gaus mean : 41.7519
Gaus Width: 2.7930
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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20
30
40
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60
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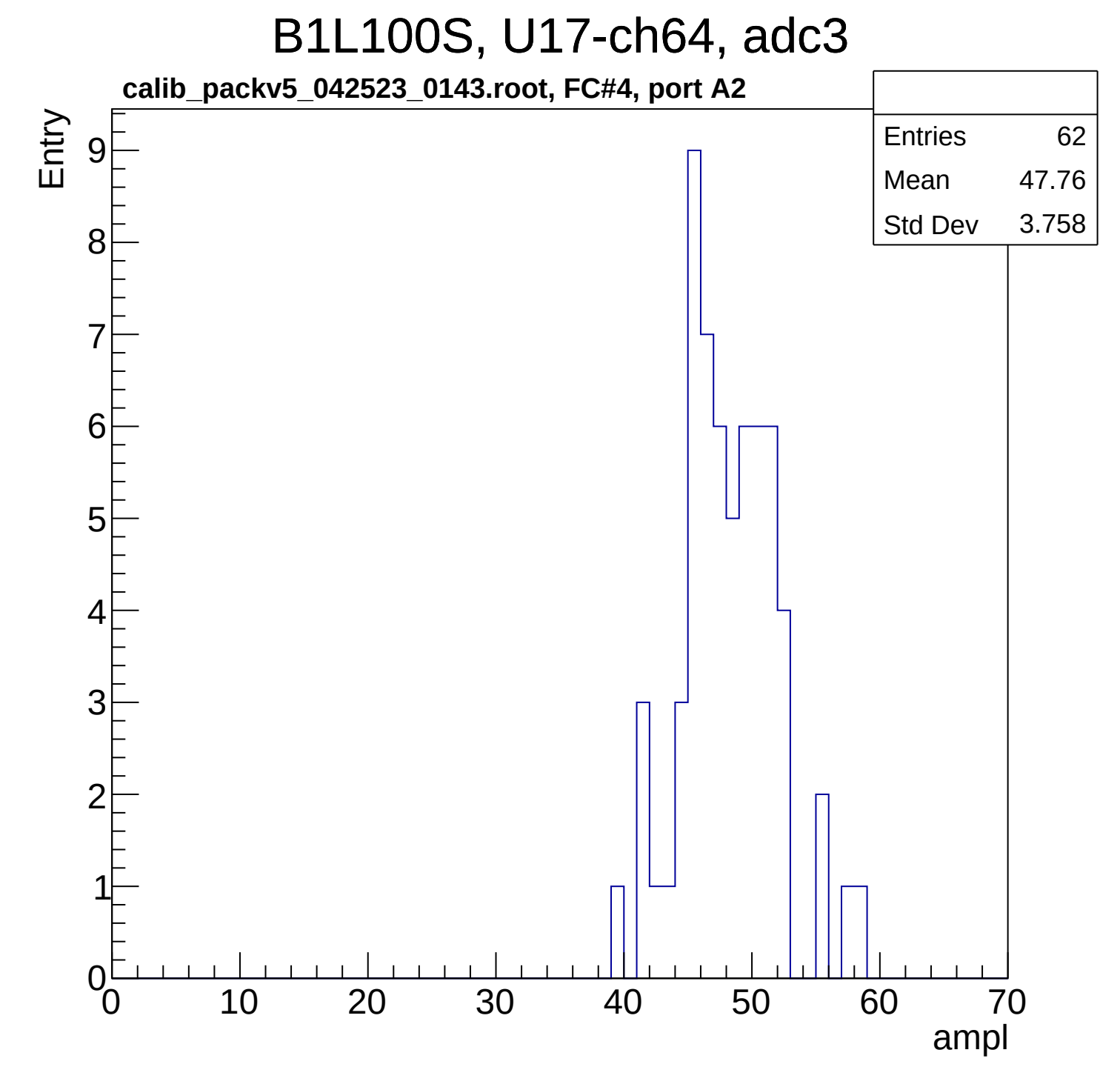
B1L100S, U17-ch64, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 47.76
Std Dev 3.758
Entry
ampl
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1
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3
4
5
6
7
8
9
0
10
20
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40
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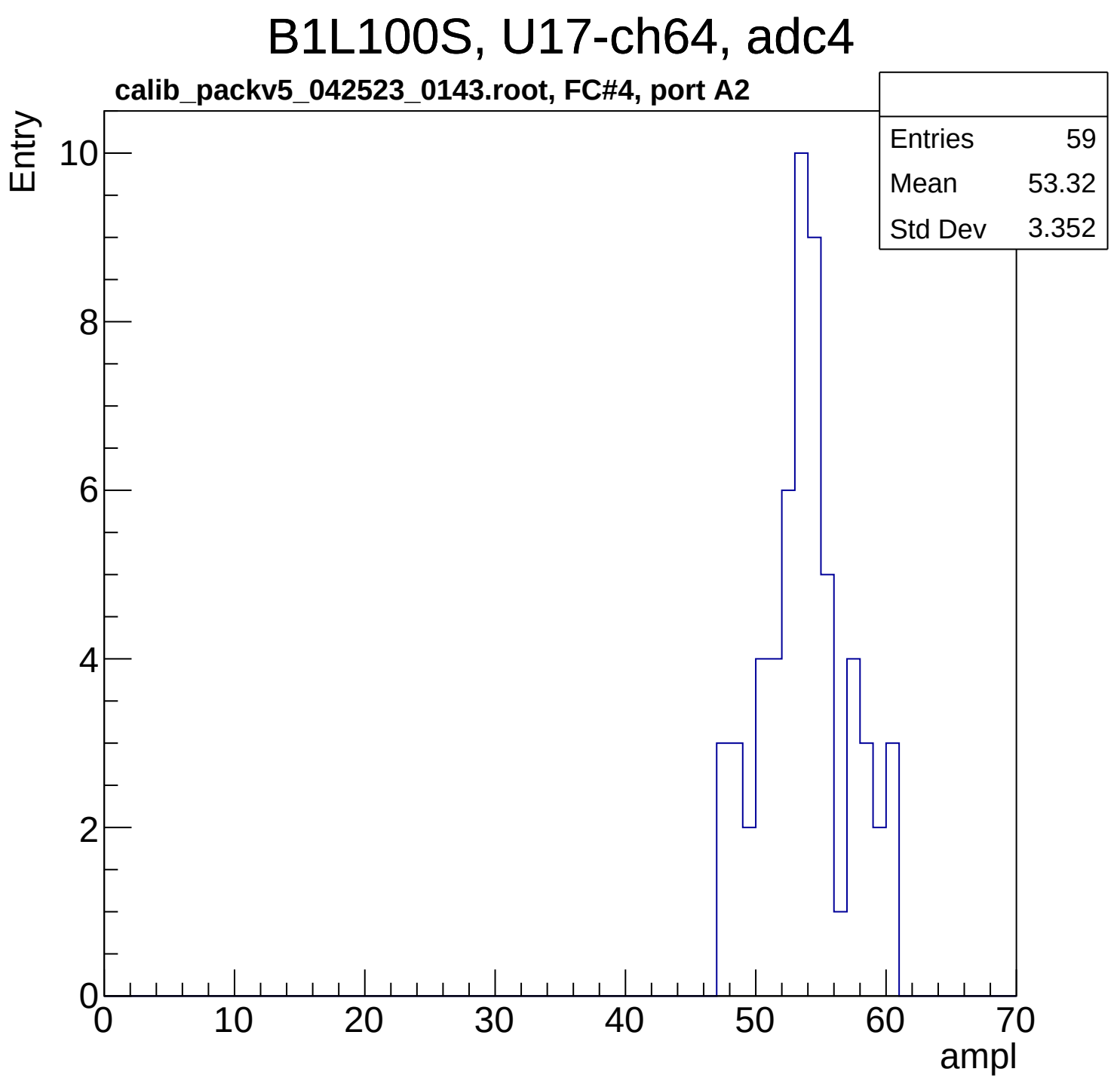
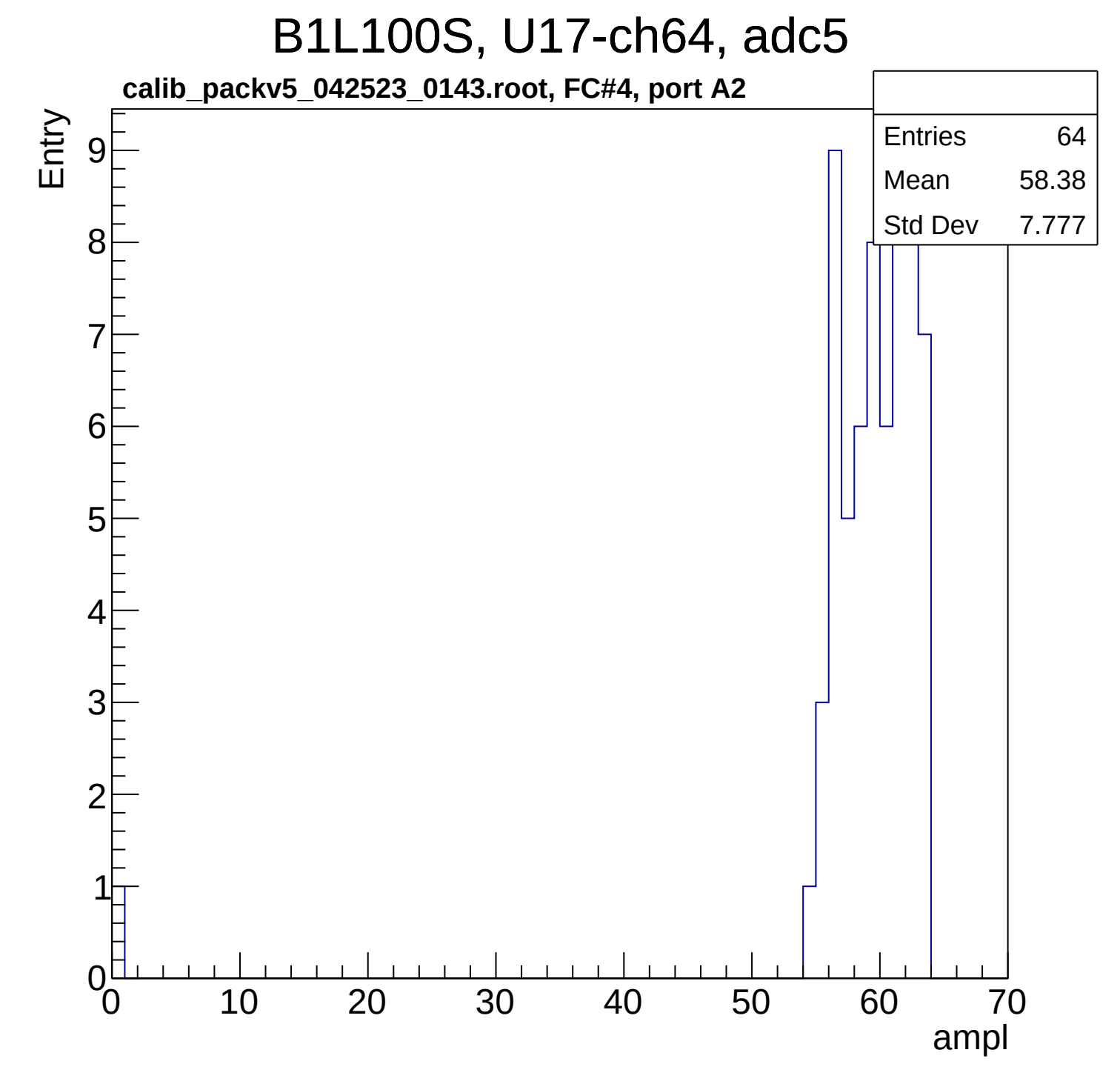
60
70


B1L100S, U17-ch64, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 53.32
Std Dev 3.352
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch64, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 58.38
Std Dev 7.777
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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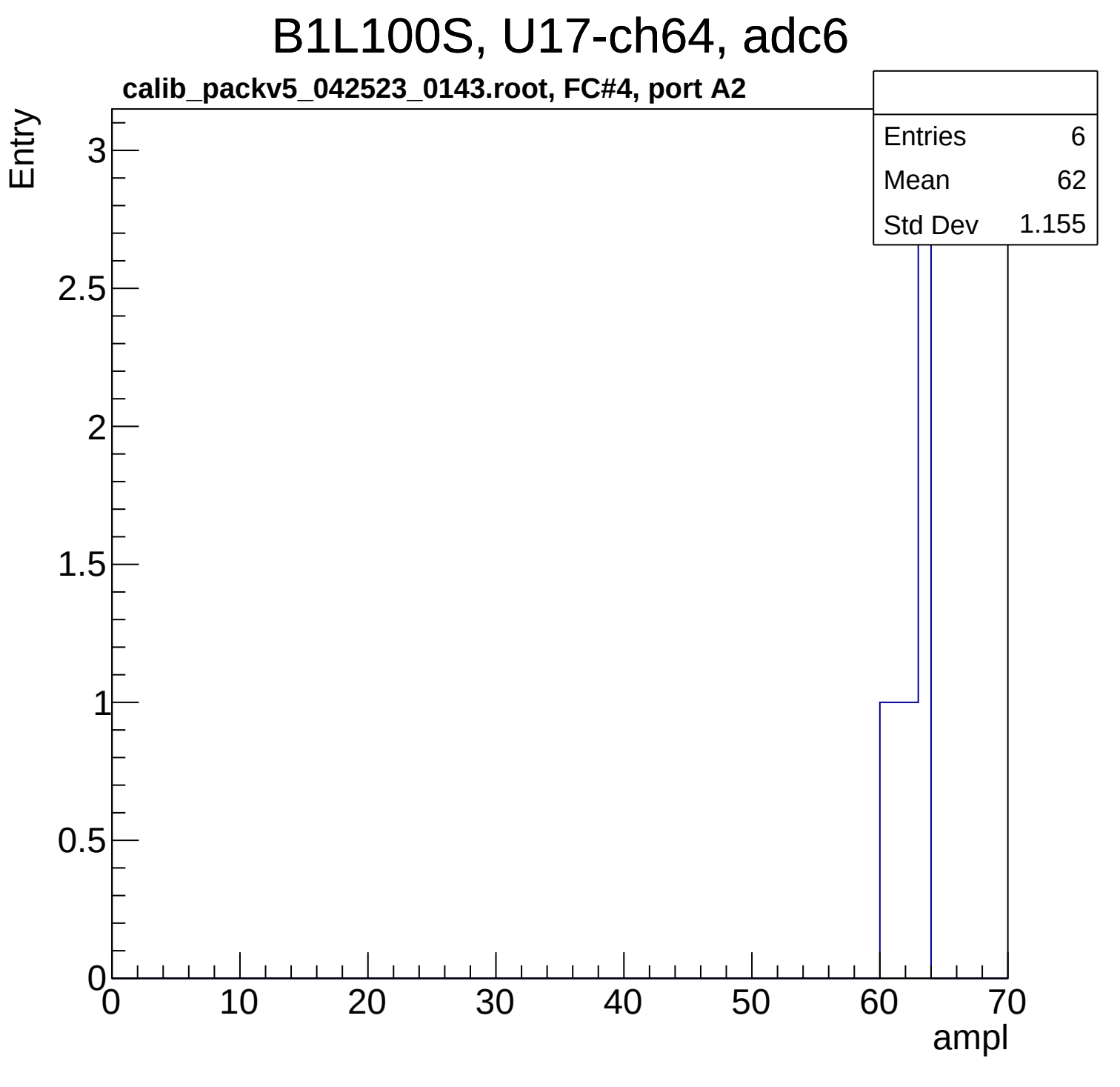
40
50
60
70


B1L100S, U17-ch64, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 6
Mean 62
Std Dev 1.155
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
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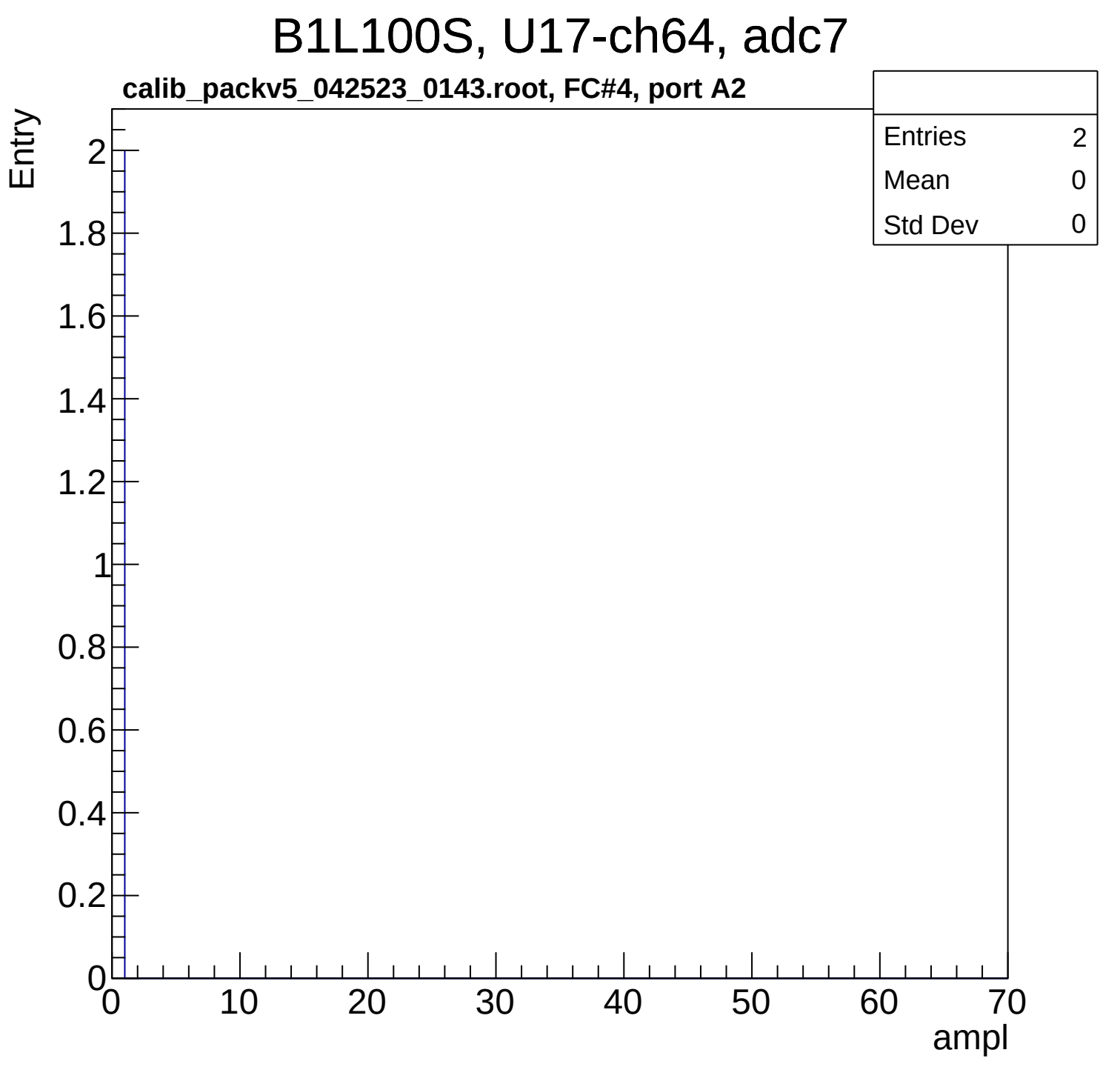
40
50
60
70


B1L100S, U17-ch64, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
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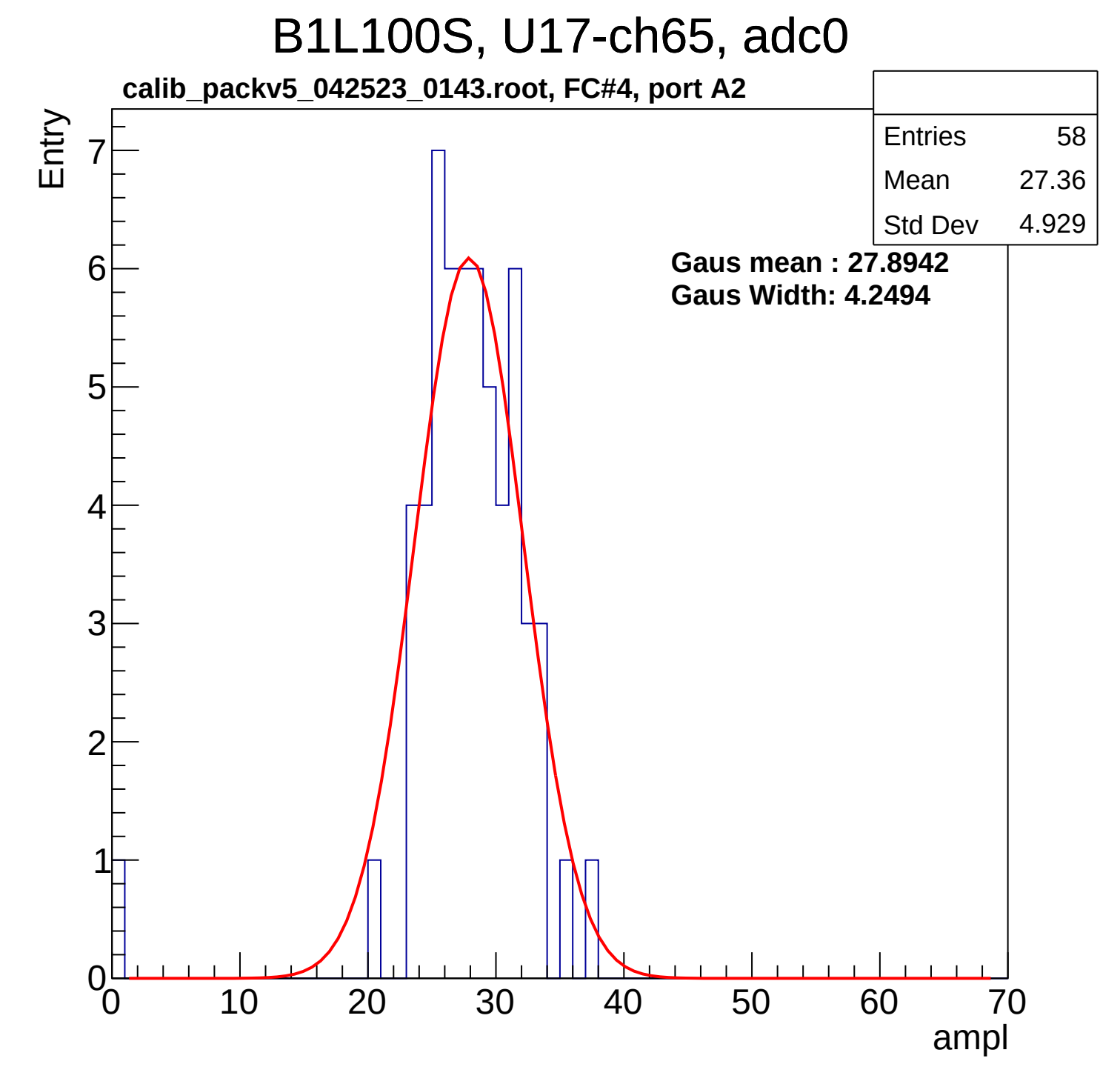
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch65, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 27.36
Std Dev 4.929
Gaus mean : 27.8942
Gaus Width: 4.2494
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
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60
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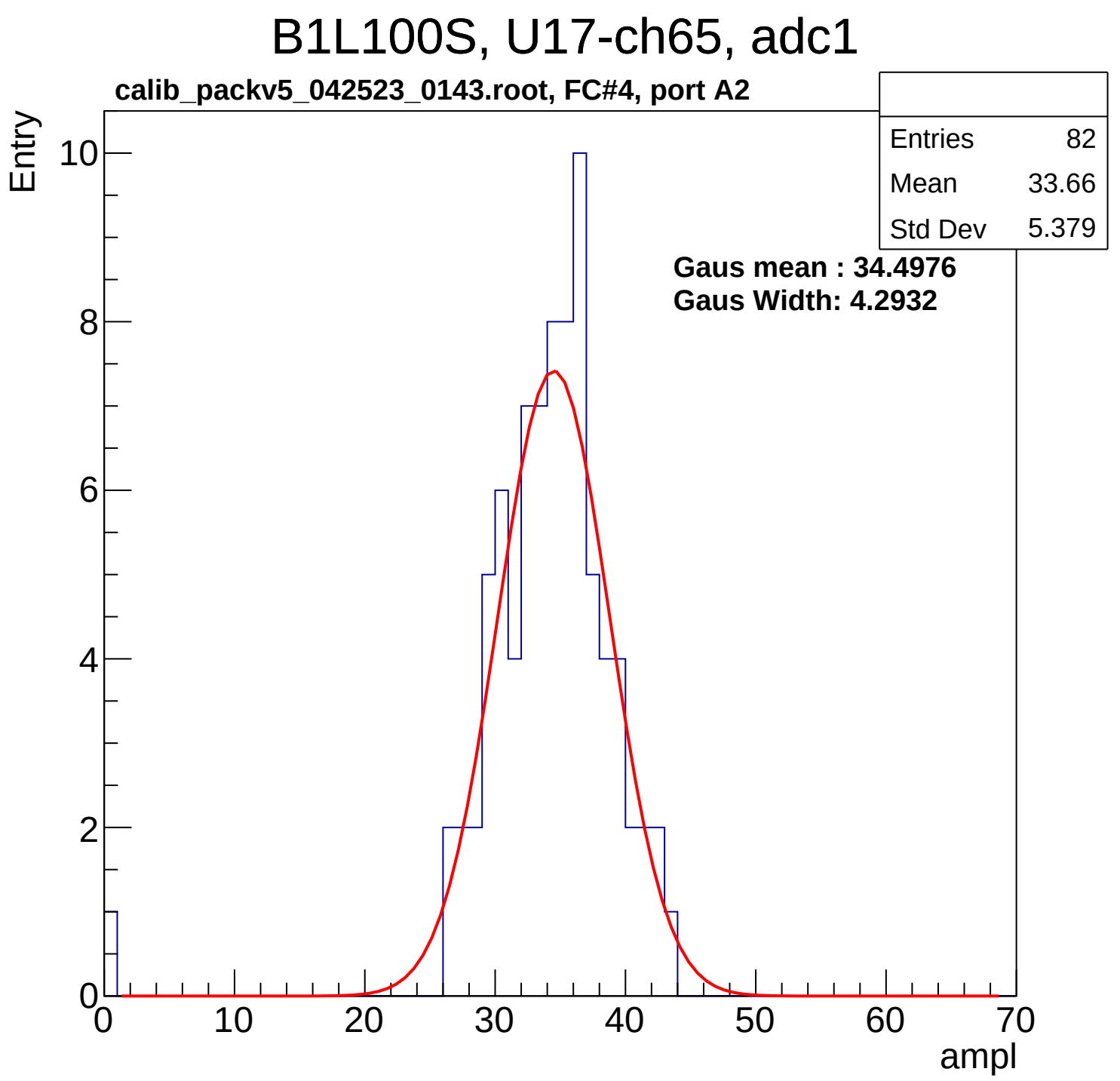
B1L100S, U17-ch65, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 82
Mean 33.66
Std Dev 5.379
Gaus mean : 34.4976
Gaus Width: 4.2932
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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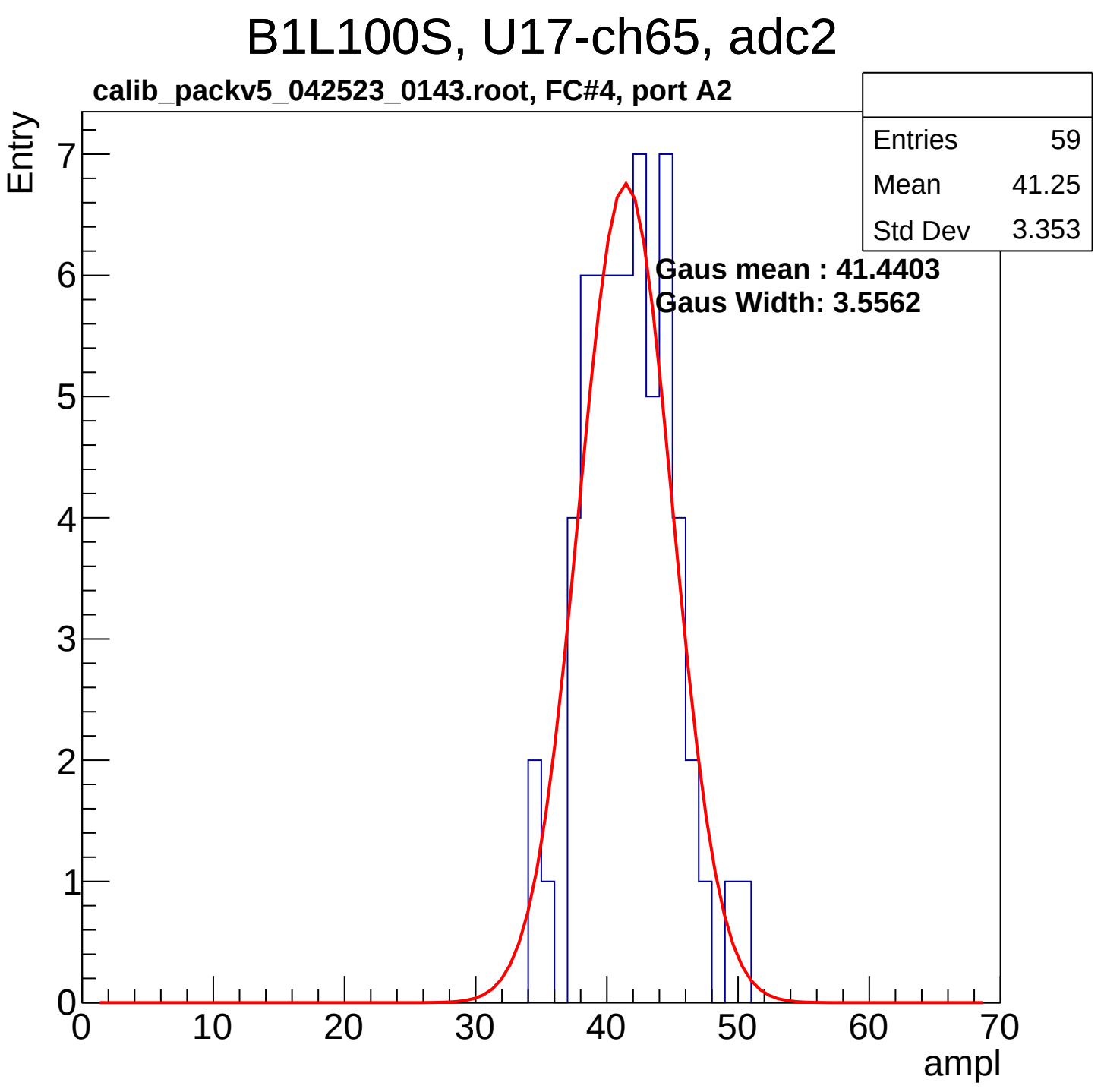
B1L100S, U17-ch65, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 41.25
Std Dev 3.353
Gaus mean : 41.4403
Gaus Width: 3.5562
Entry
ampl
0
1
2
3
4
5
6
7
0
10
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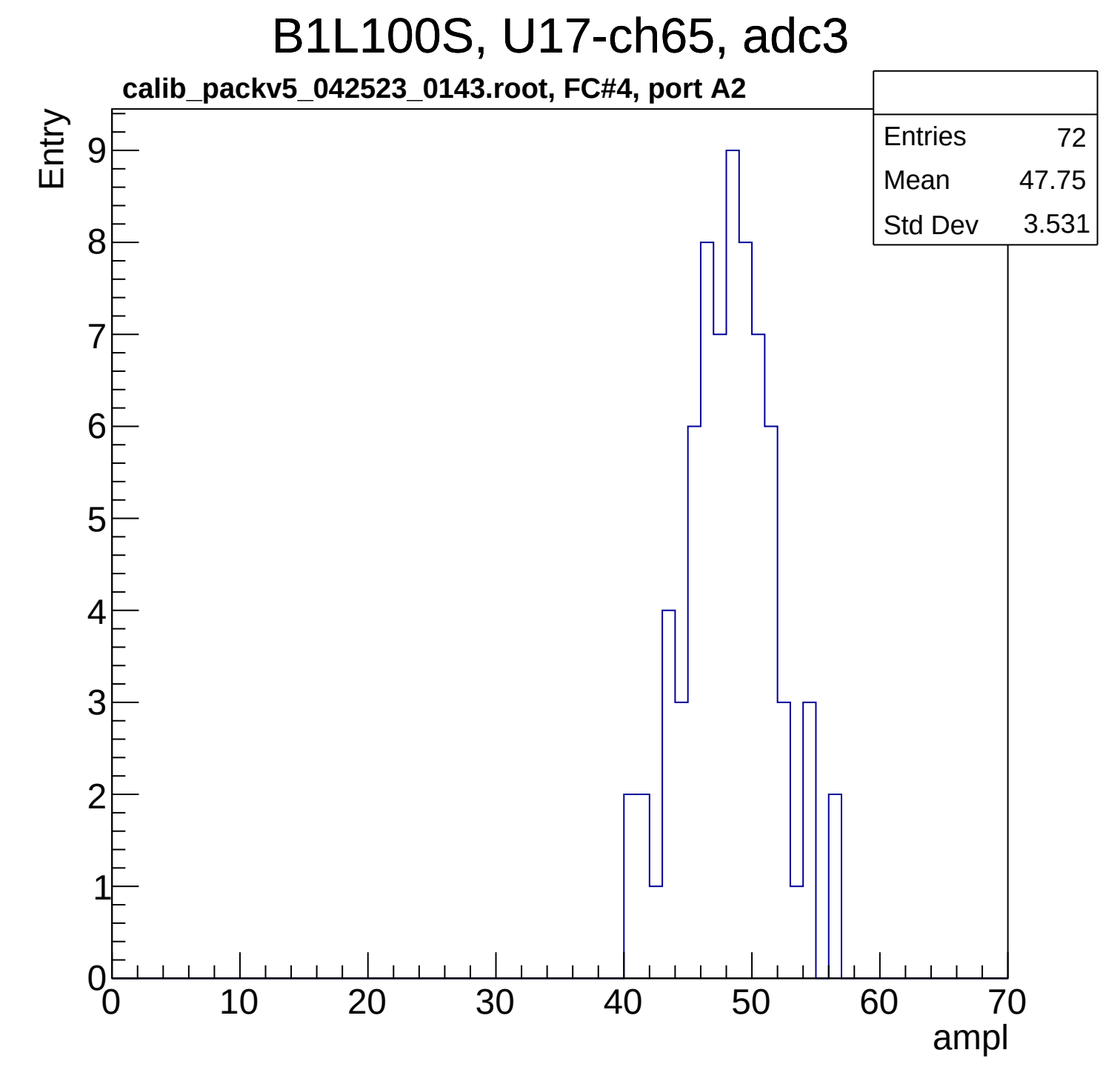
B1L100S, U17-ch65, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 47.75
Std Dev 3.531
Entry
ampl
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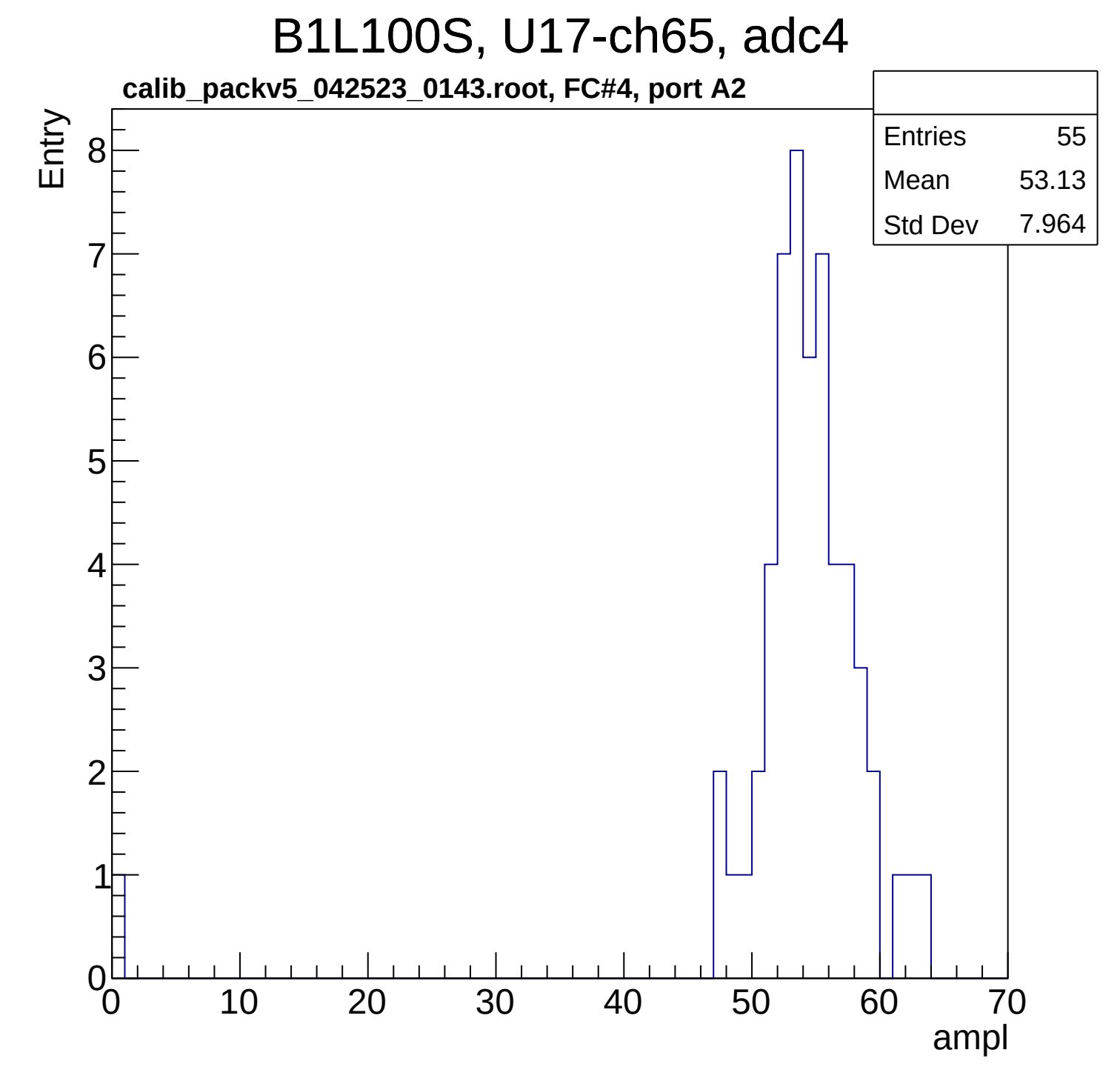
B1L100S, U17-ch65, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 53.13
Std Dev 7.964
Entry
ampl
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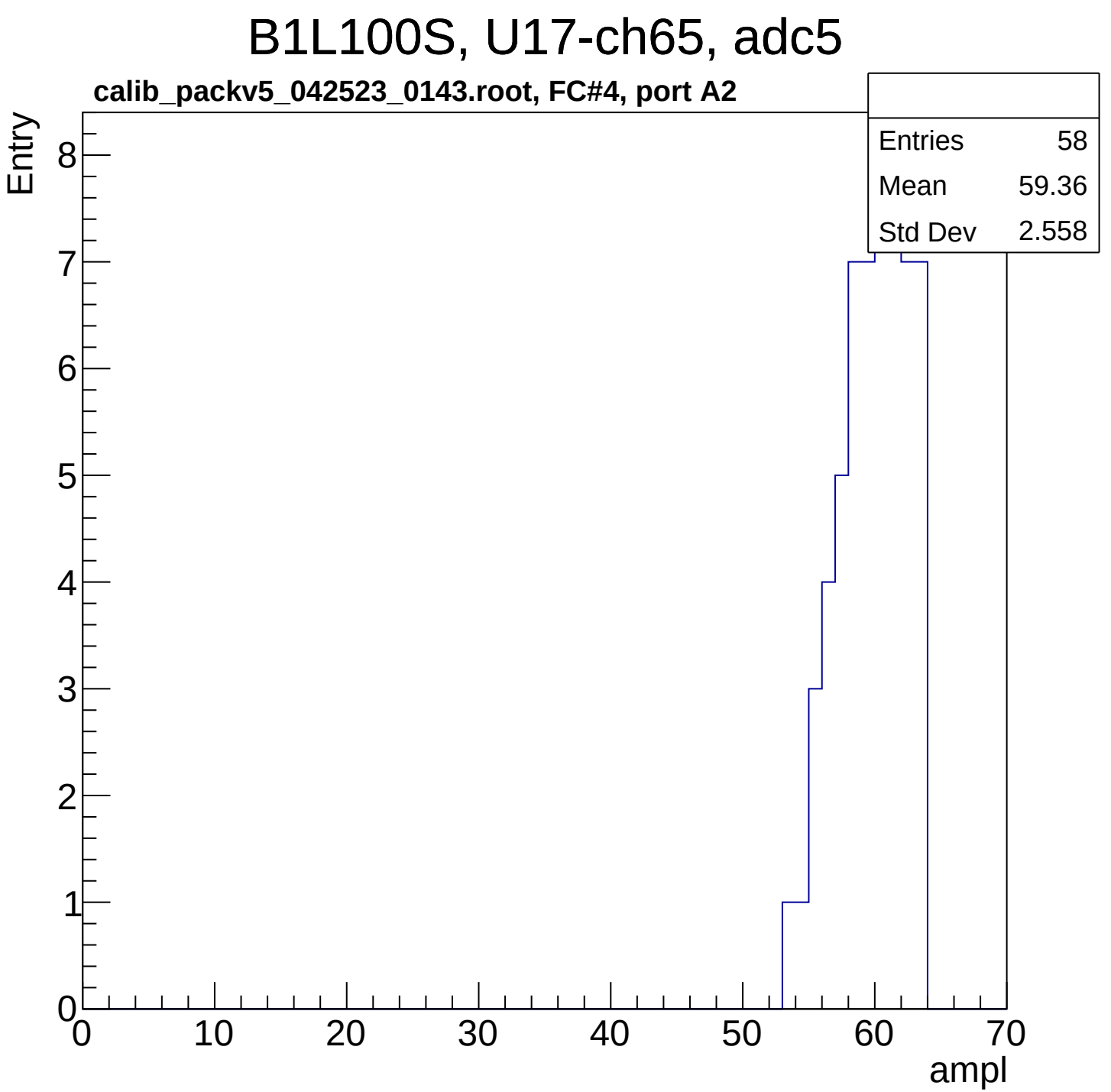
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch65, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 59.36
Std Dev 2.558
Entry
0
1
2
3
4
5
6
7
8
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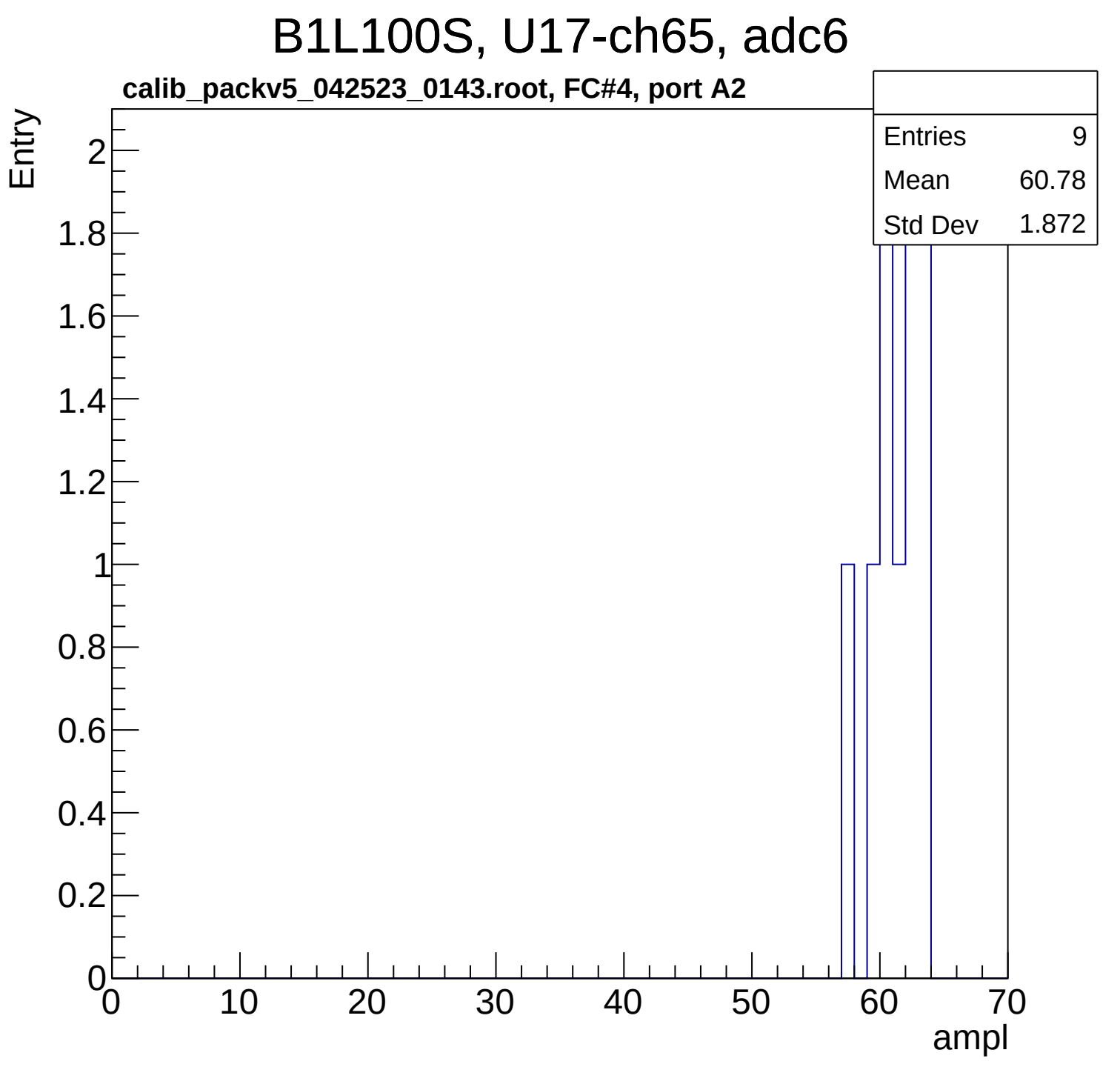
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch65, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 9
Mean 60.78
Std Dev 1.872
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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40
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60
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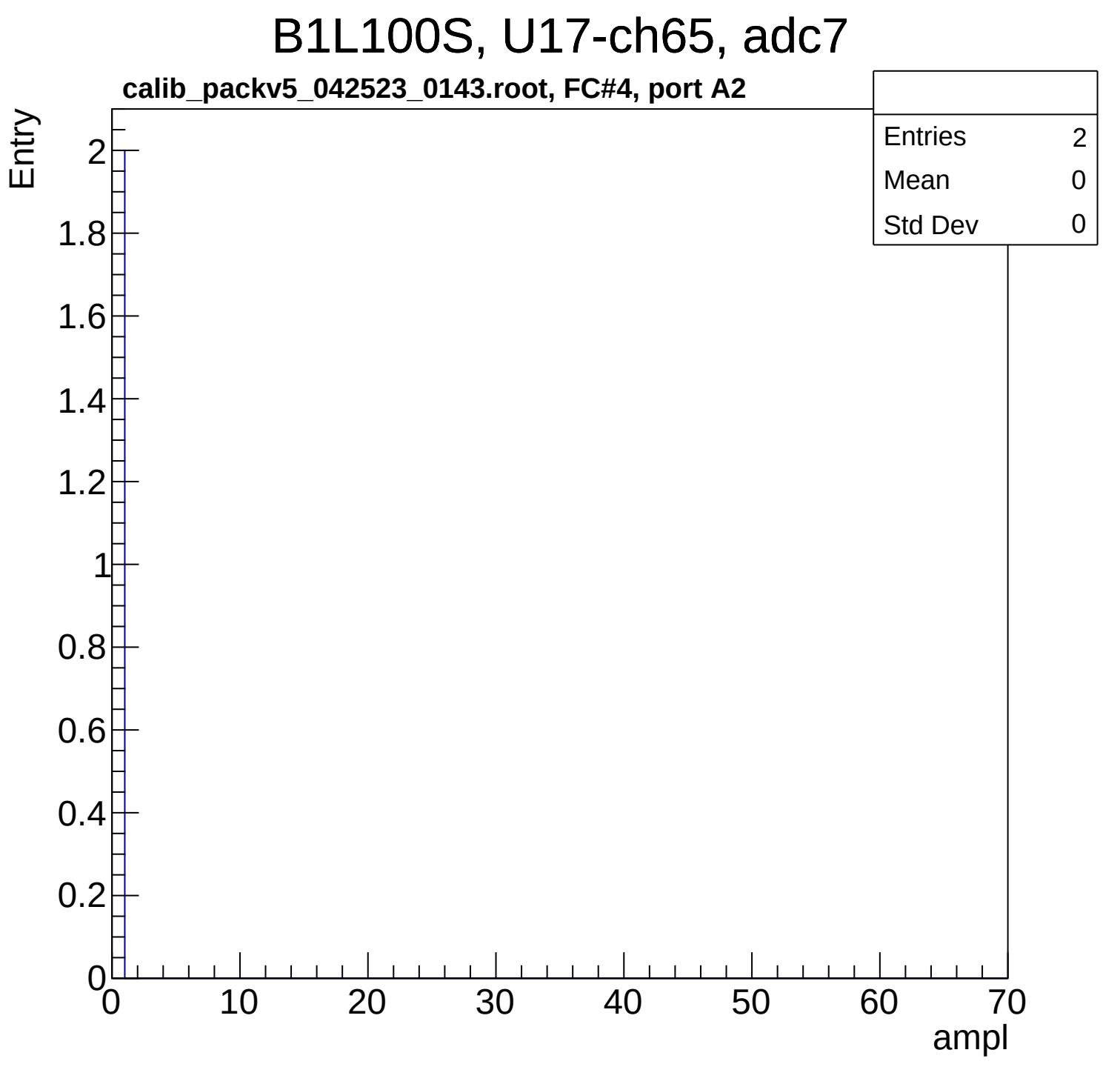
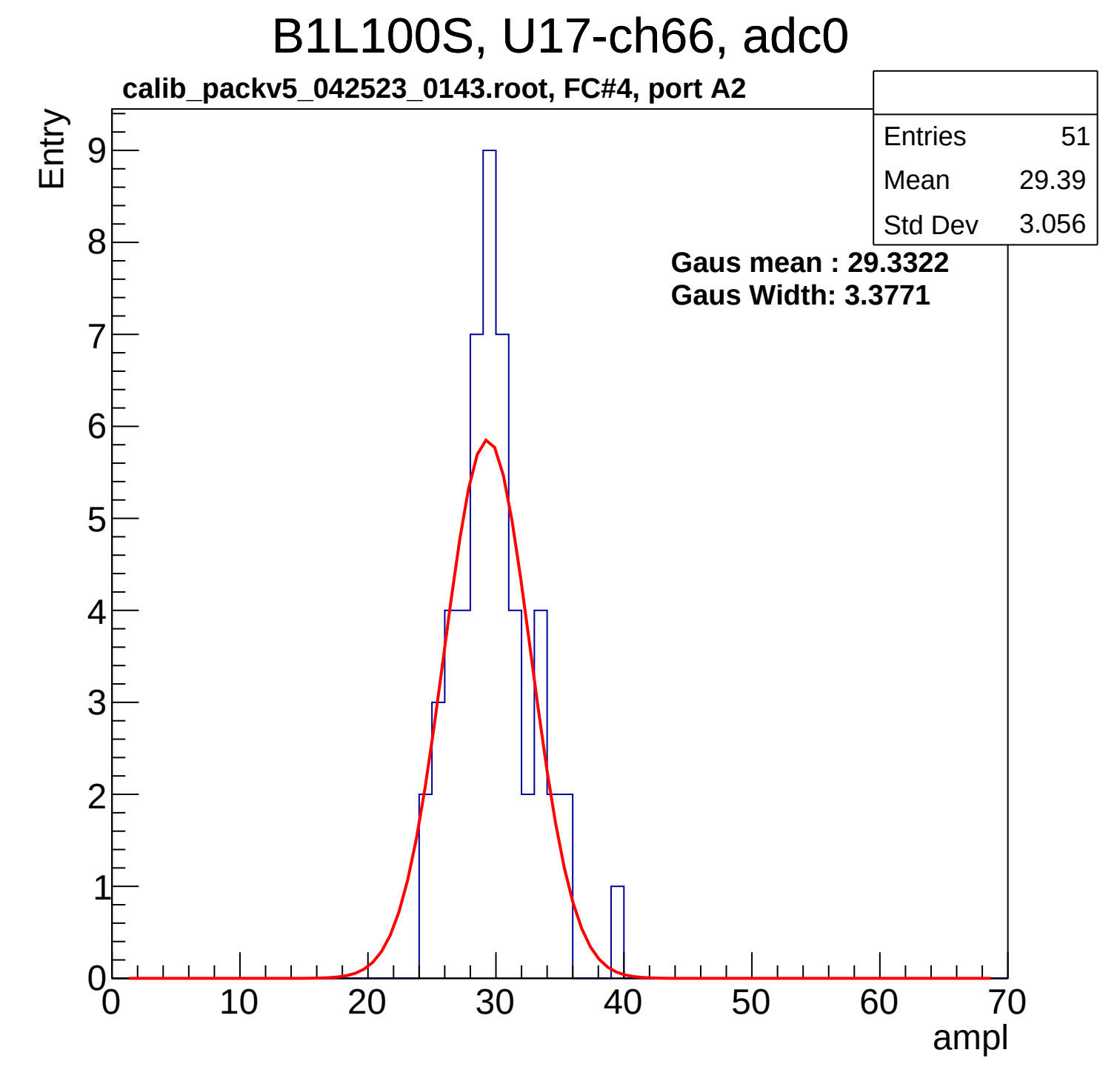

B1L100S, U17-ch65, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch66, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 29.39
Std Dev 3.056
Gaus mean : 29.3322
Gaus Width: 3.3771
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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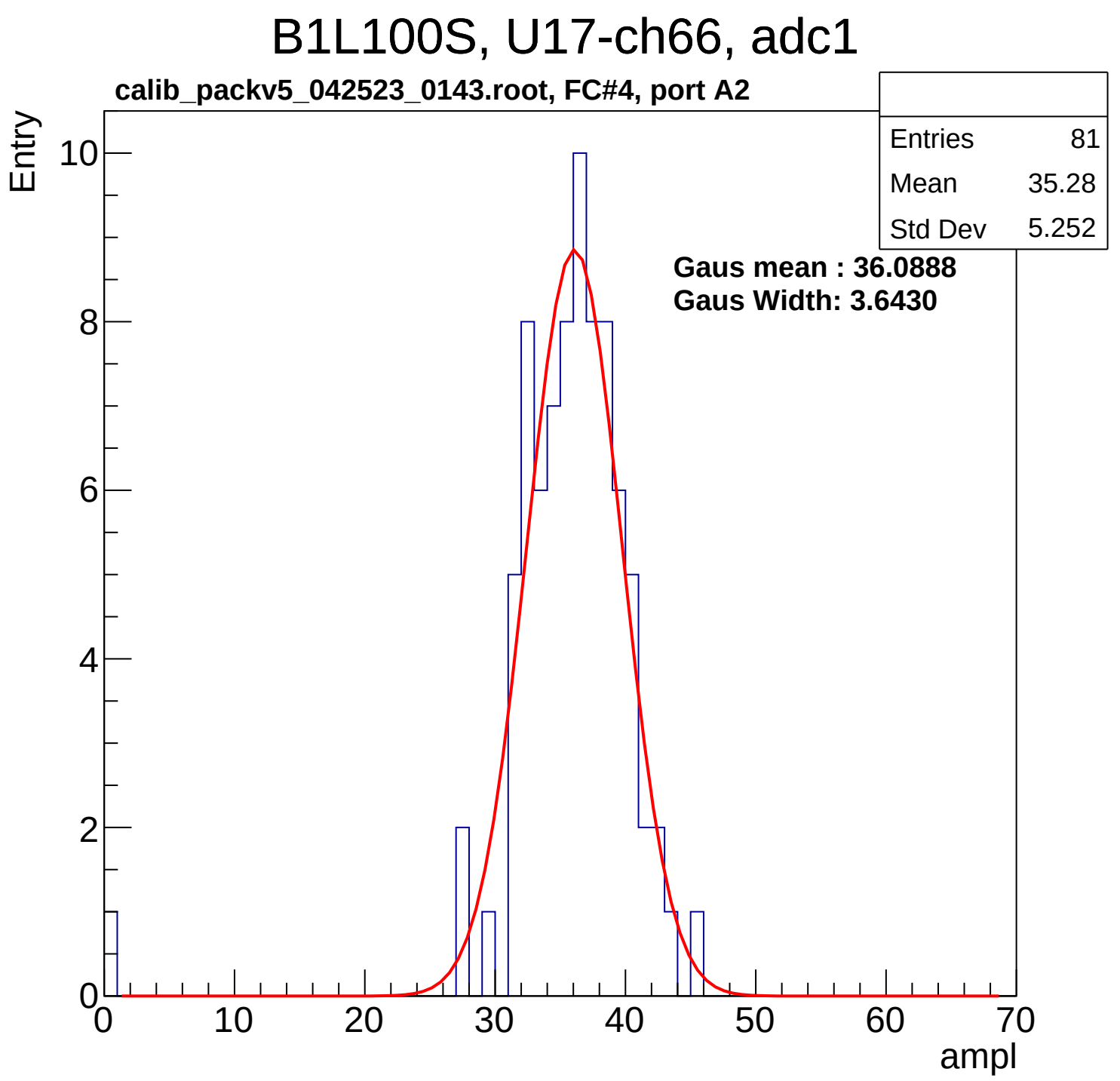
B1L100S, U17-ch66, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 81
Mean 35.28
Std Dev 5.252
Gaus mean : 36.0888
Gaus Width: 3.6430
Entry
ampl
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2
4
6
8
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0
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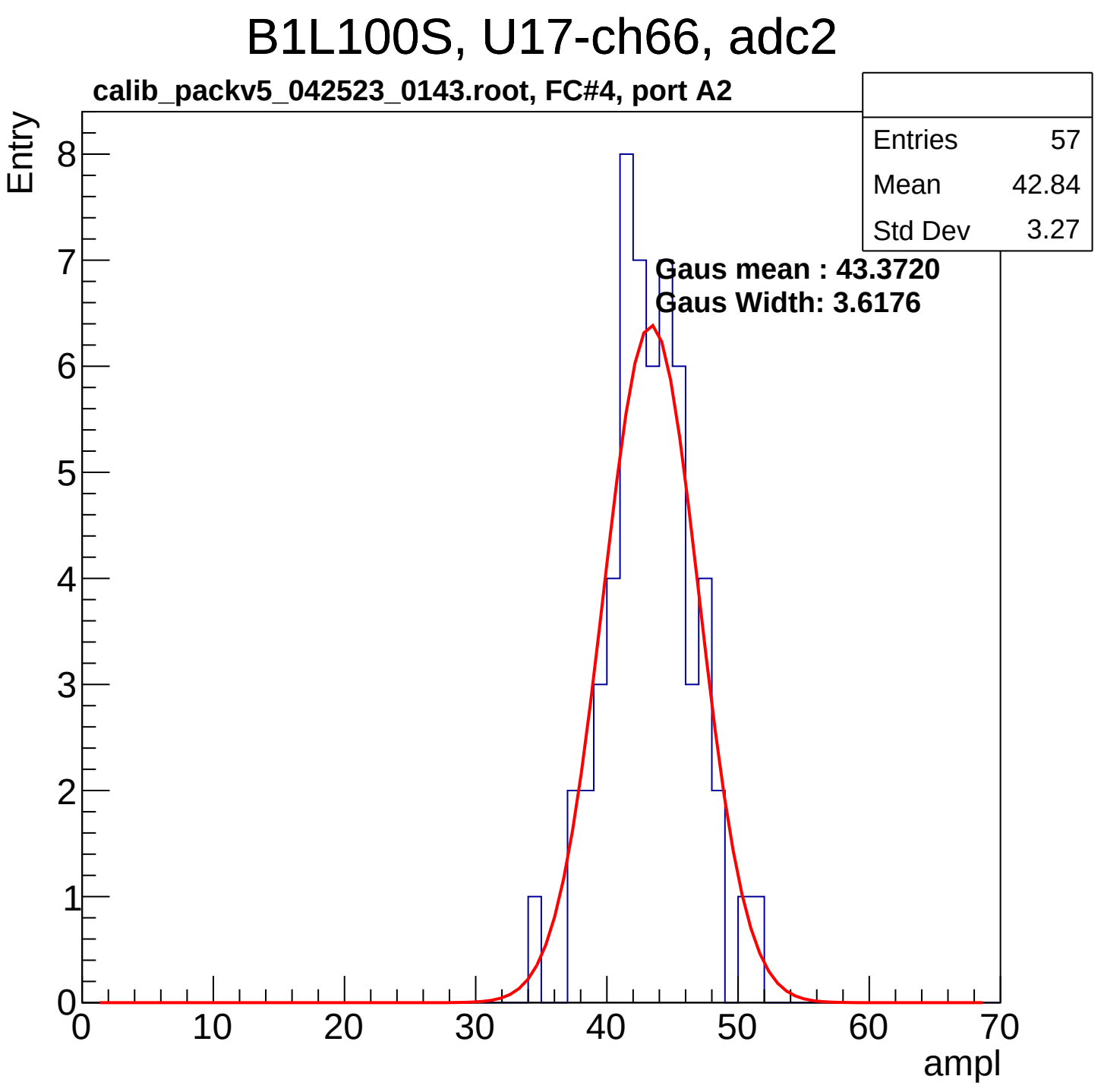
B1L100S, U17-ch66, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 42.84
Std Dev 3.27
Gaus mean : 43.3720
Gaus Width: 3.6176
Entry
ampl
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1
2
3
4
5
6
7
8
0
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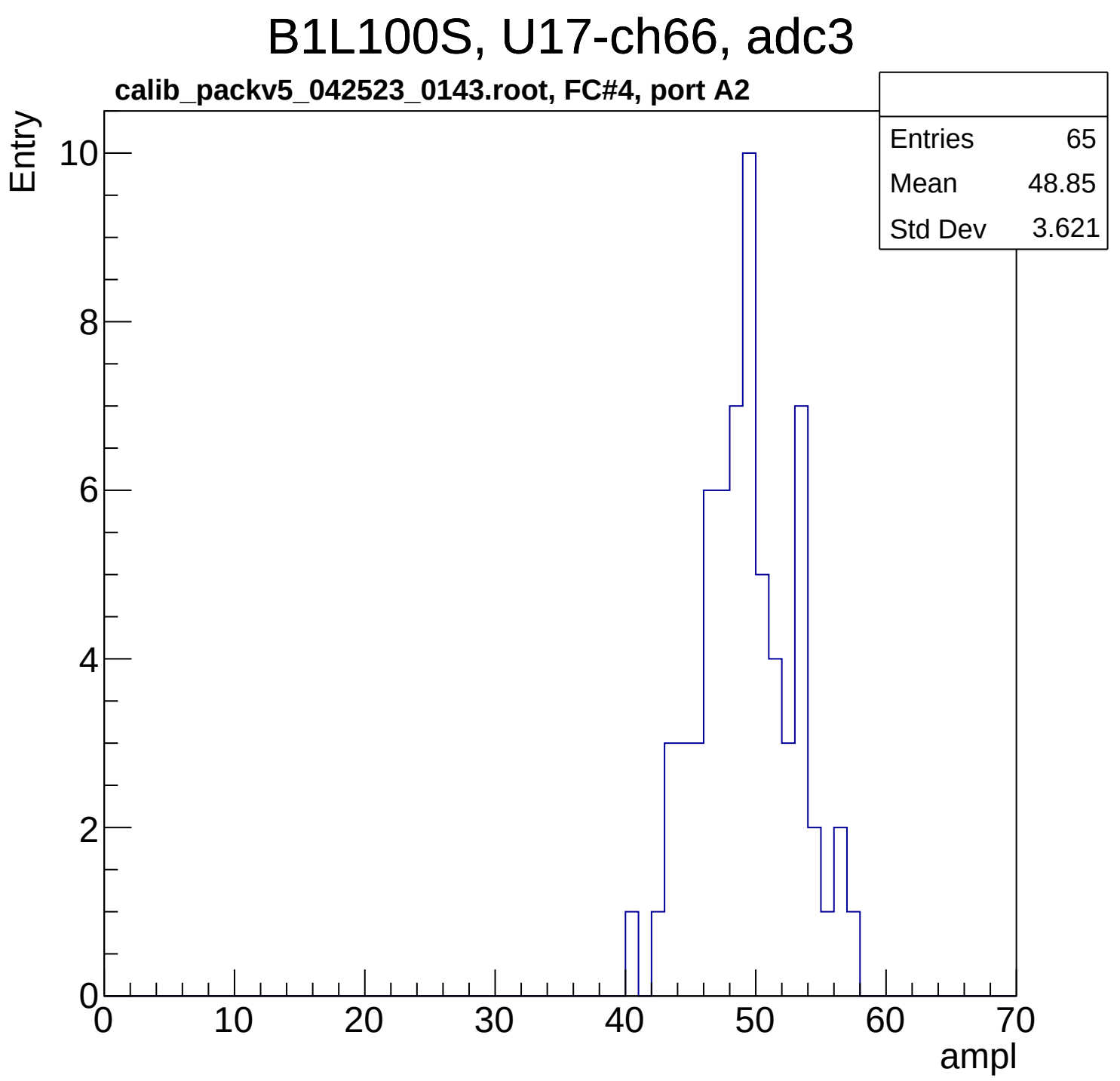
B1L100S, U17-ch66, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 48.85
Std Dev 3.621
Entry
ampl
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2
4
6
8
10
0
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40
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60
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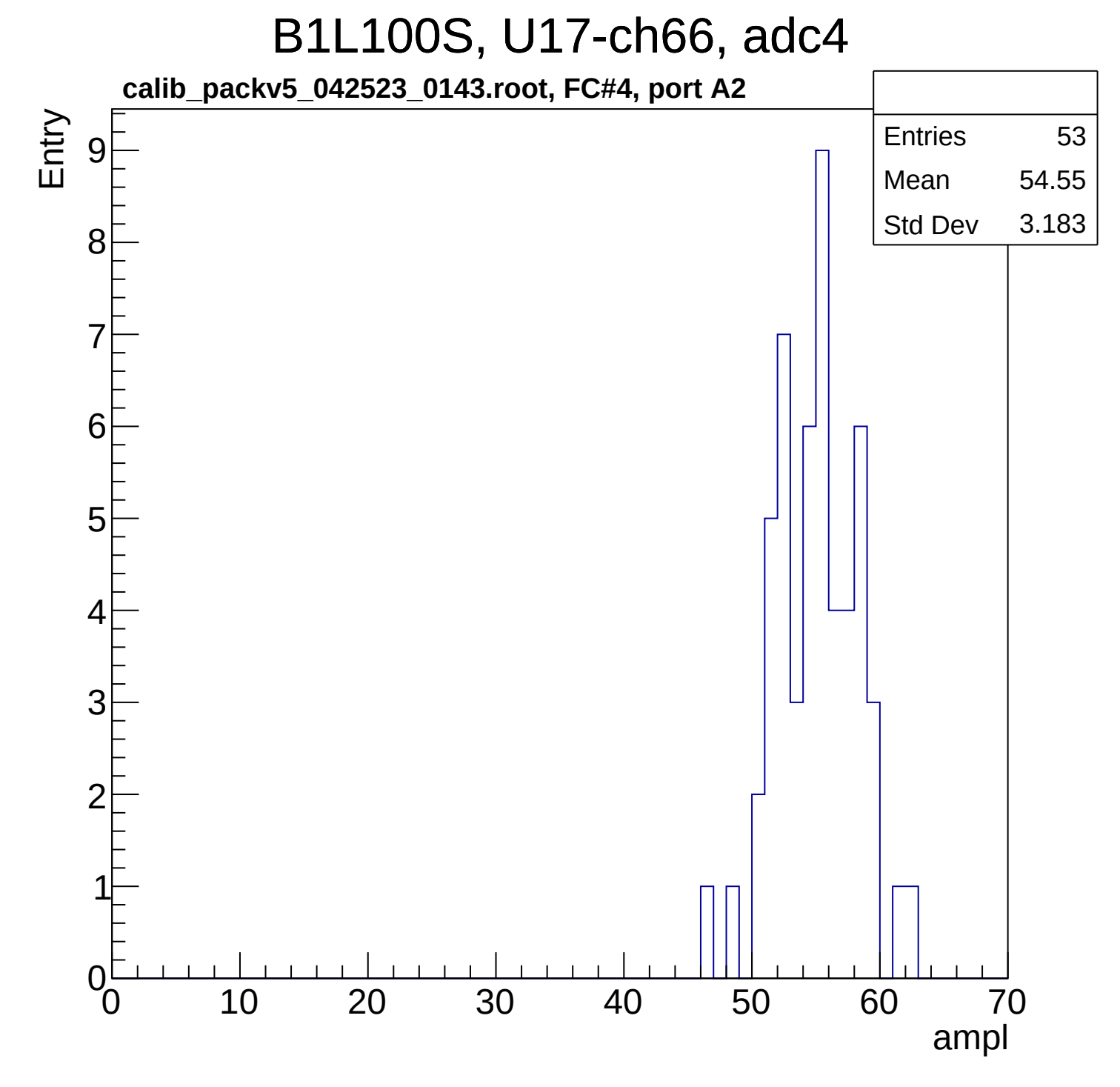
B1L100S, U17-ch66, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 54.55
Std Dev 3.183
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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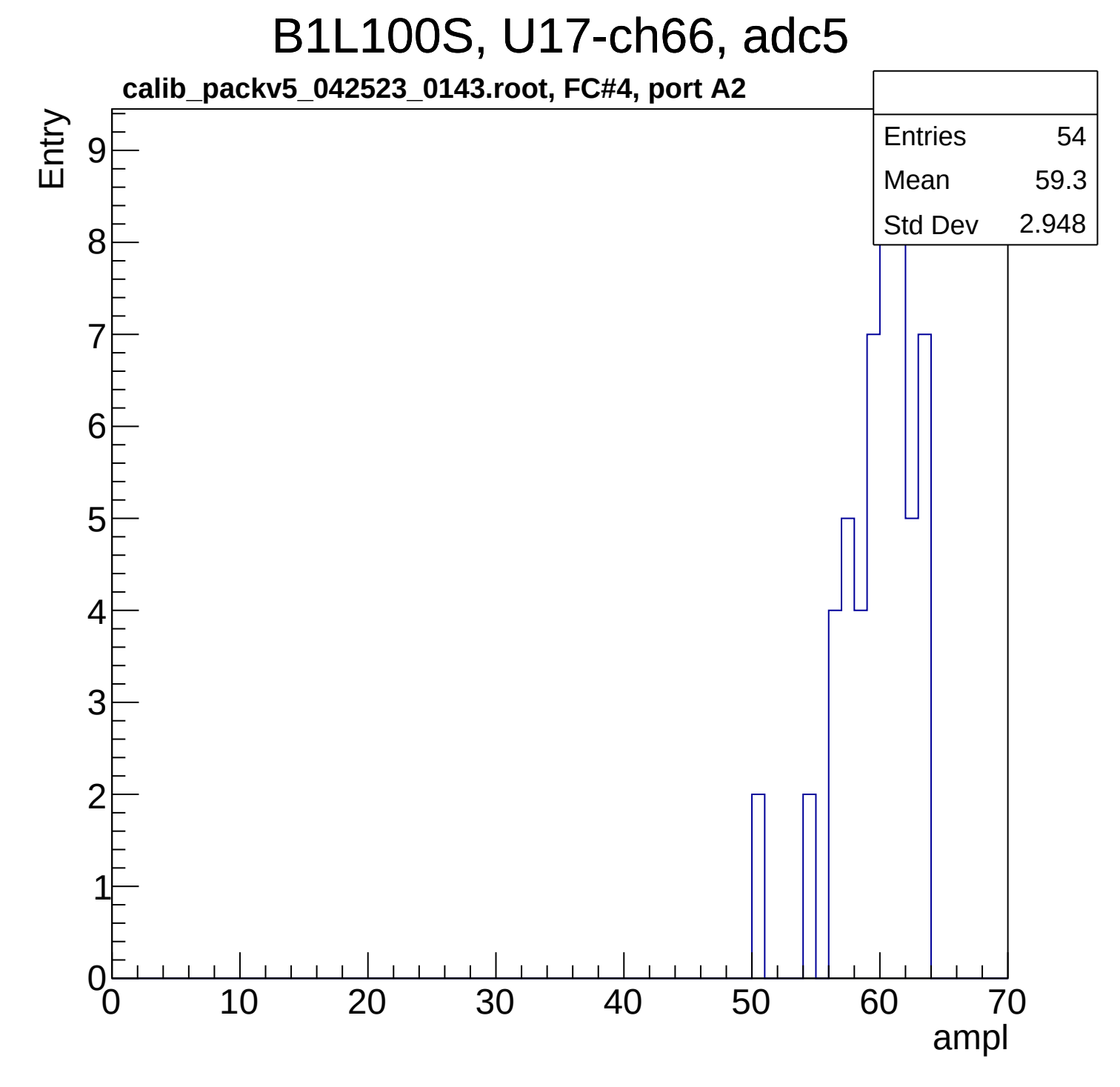
B1L100S, U17-ch66, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 59.3
Std Dev 2.948
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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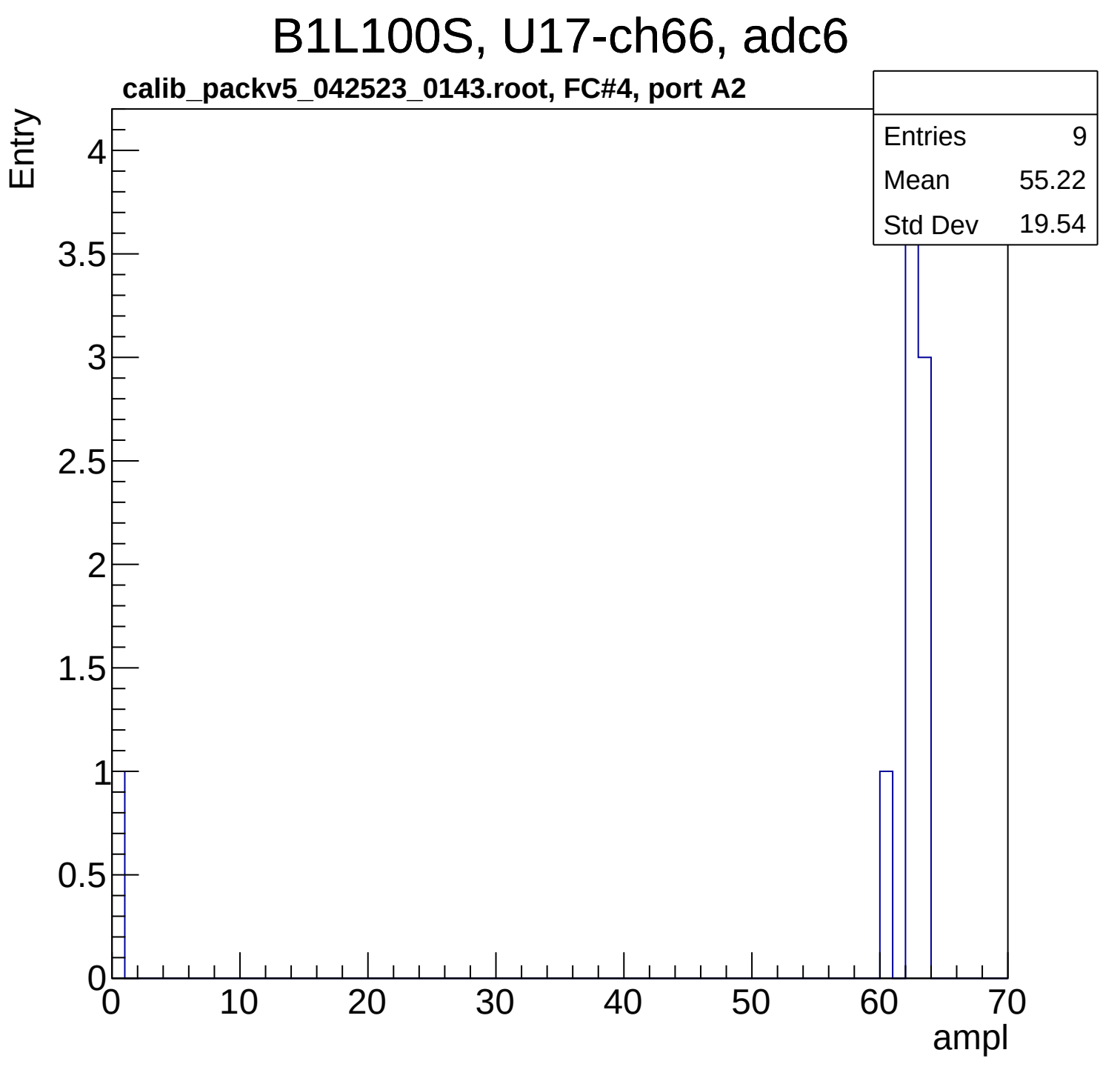
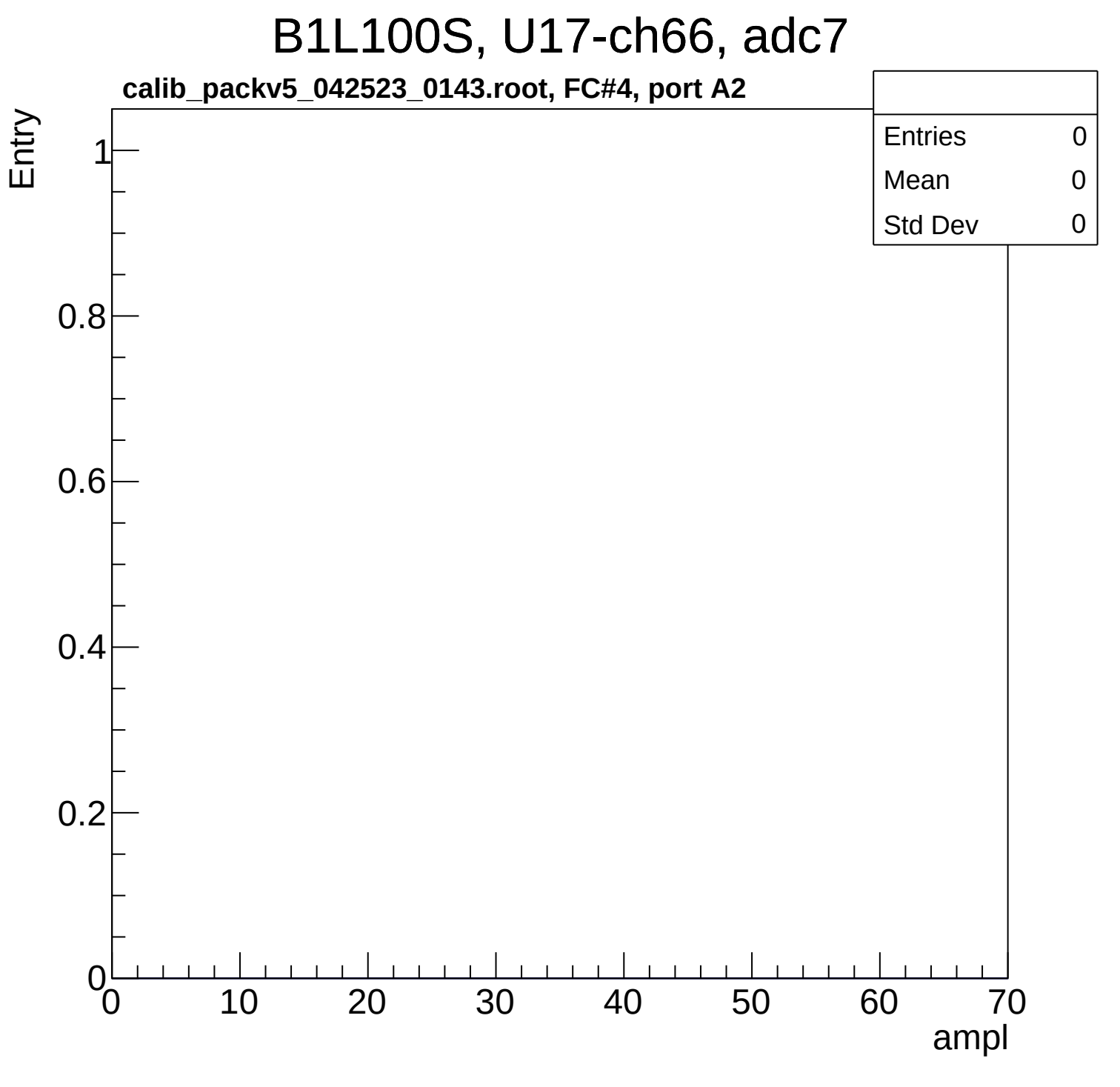

B1L100S, U17-ch66, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 9
Mean 55.22
Std Dev 19.54
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L100S, U17-ch66, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
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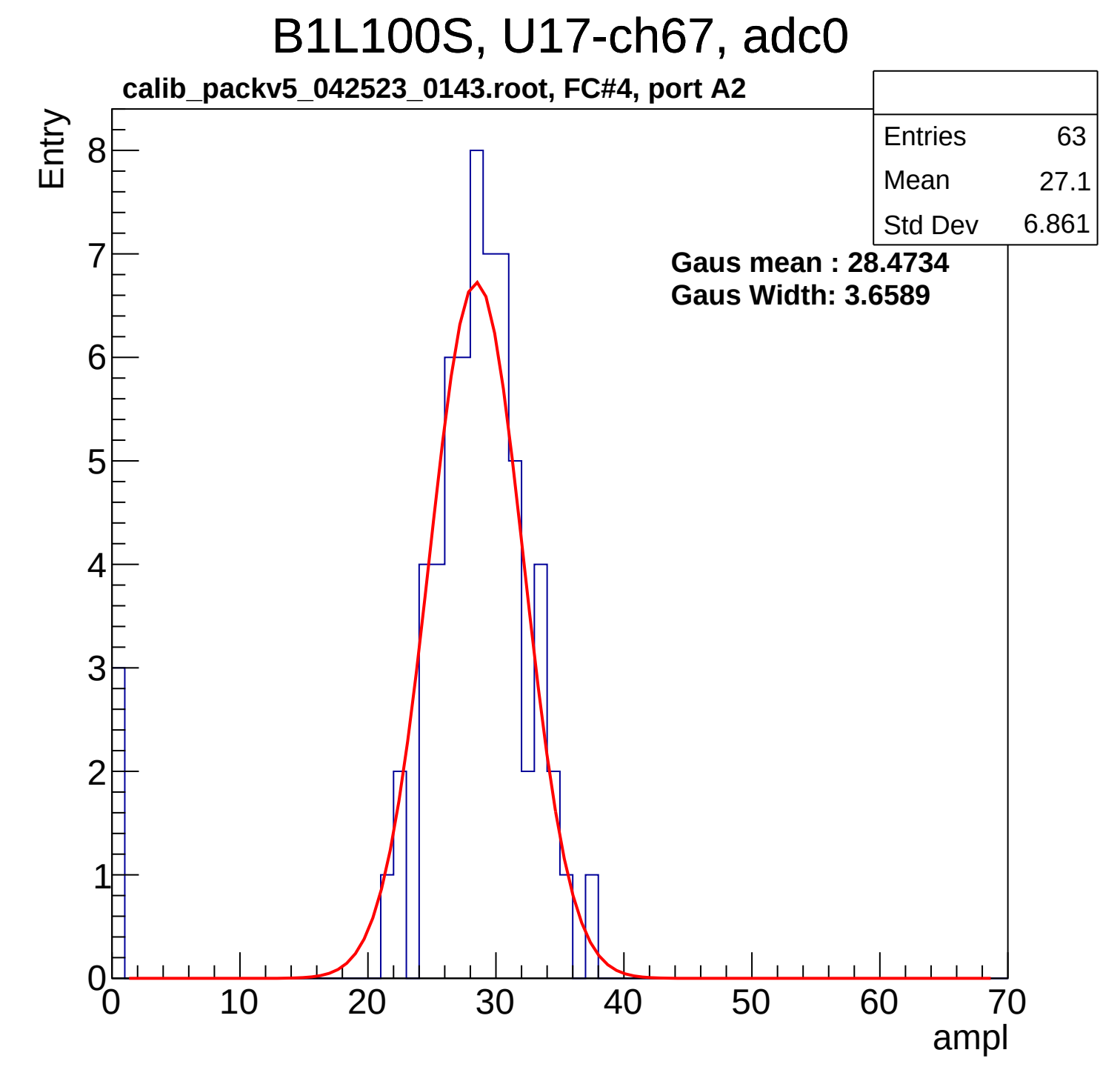
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch67, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 27.1
Std Dev 6.861
Gaus mean : 28.4734
Gaus Width: 3.6589
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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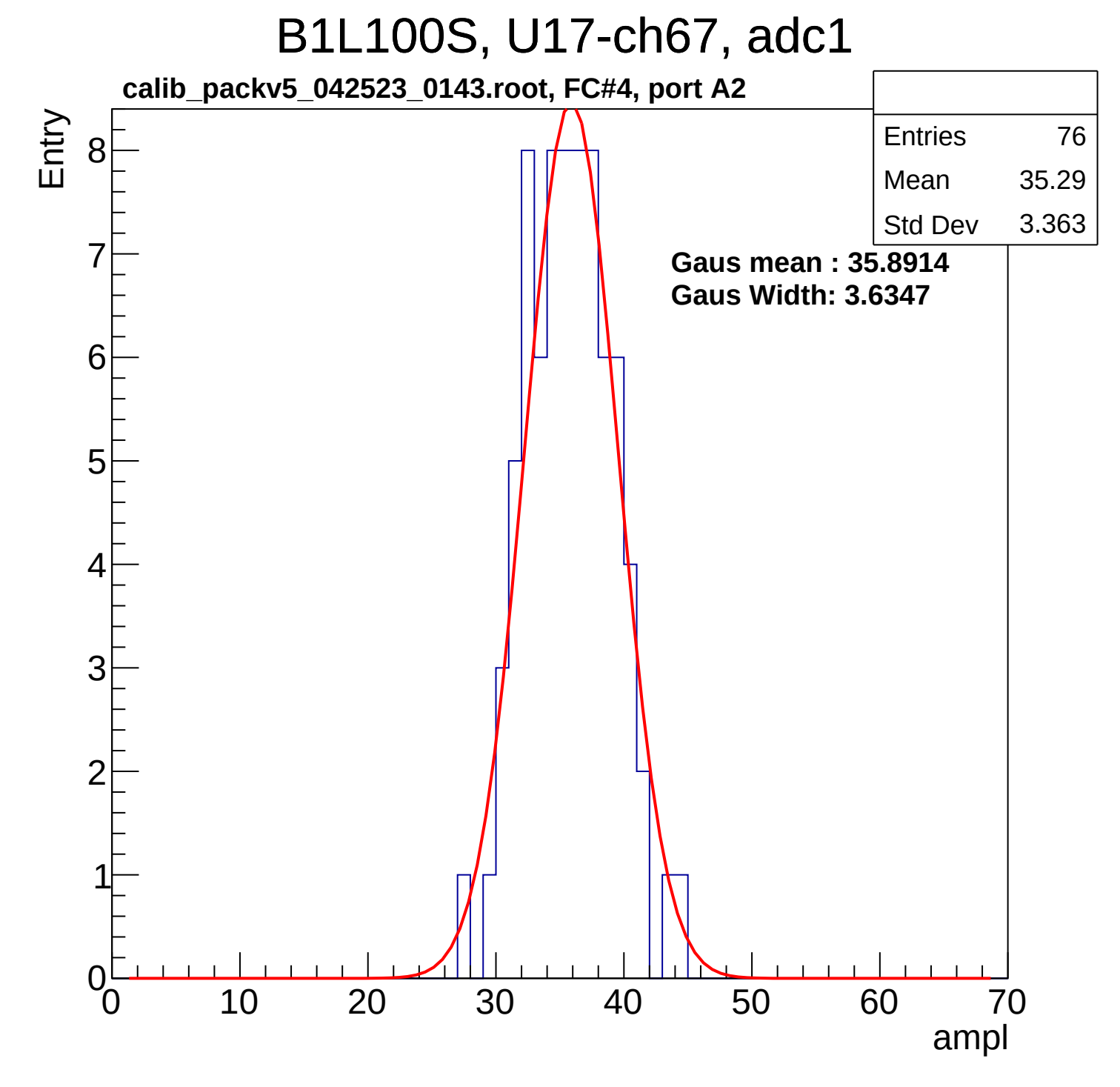
B1L100S, U17-ch67, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 76
Mean 35.29
Std Dev 3.363
Gaus mean : 35.8914
Gaus Width: 3.6347
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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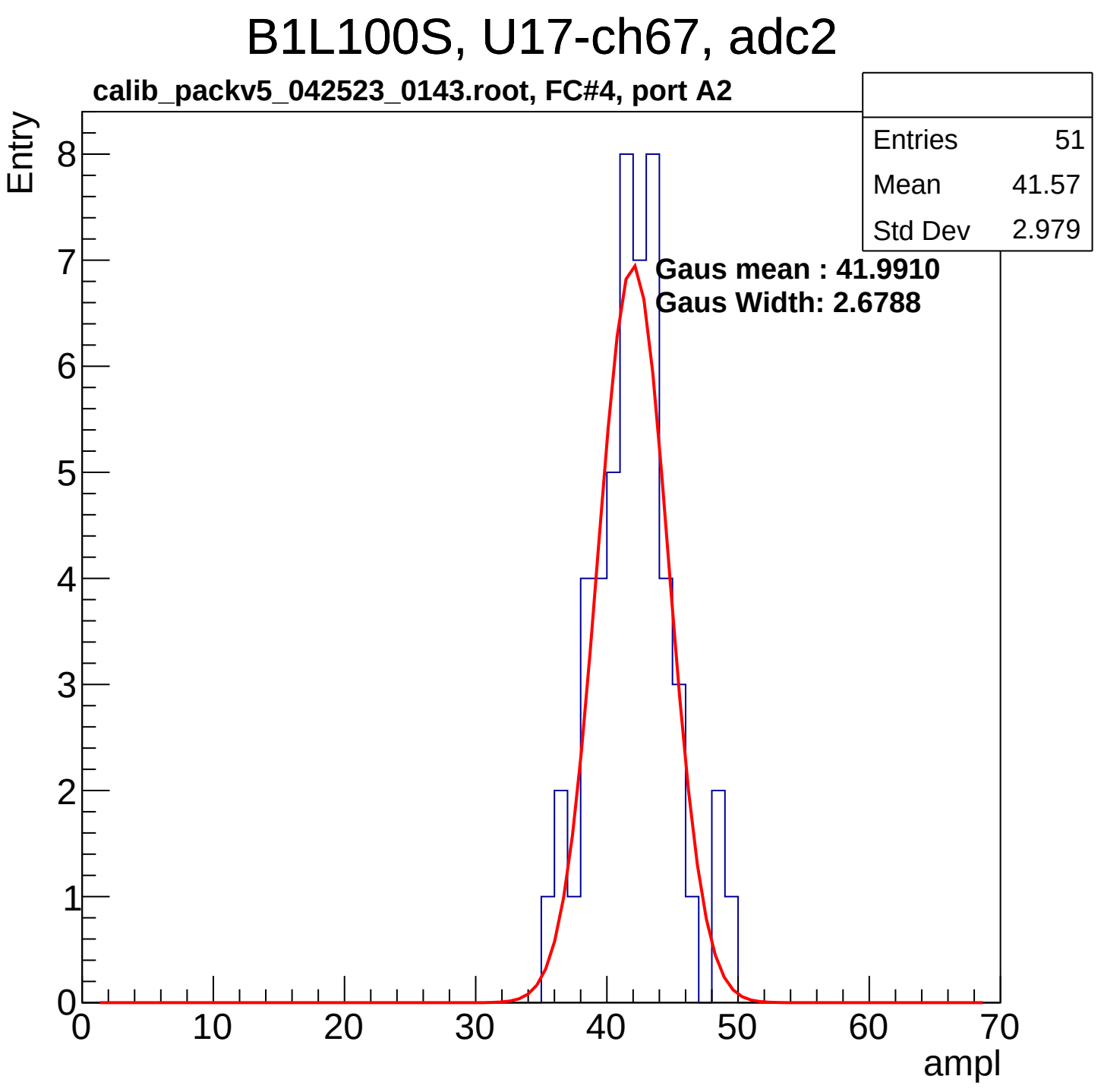
40
50
60
70


B1L100S, U17-ch67, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 41.57
Std Dev 2.979
Gaus mean : 41.9910
Gaus Width: 2.6788
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
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40
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60
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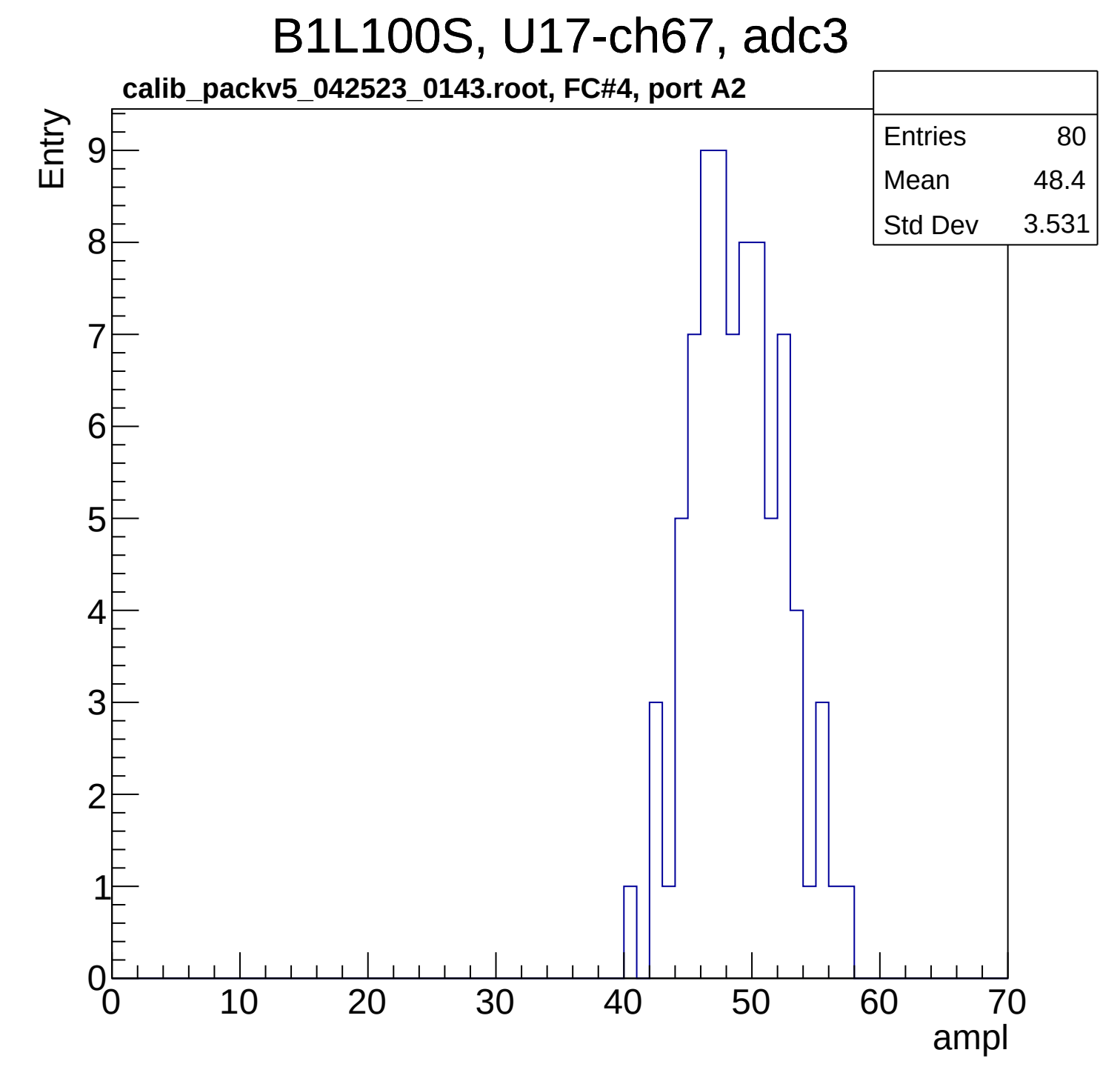
B1L100S, U17-ch67, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 80
Mean 48.4
Std Dev 3.531
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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60
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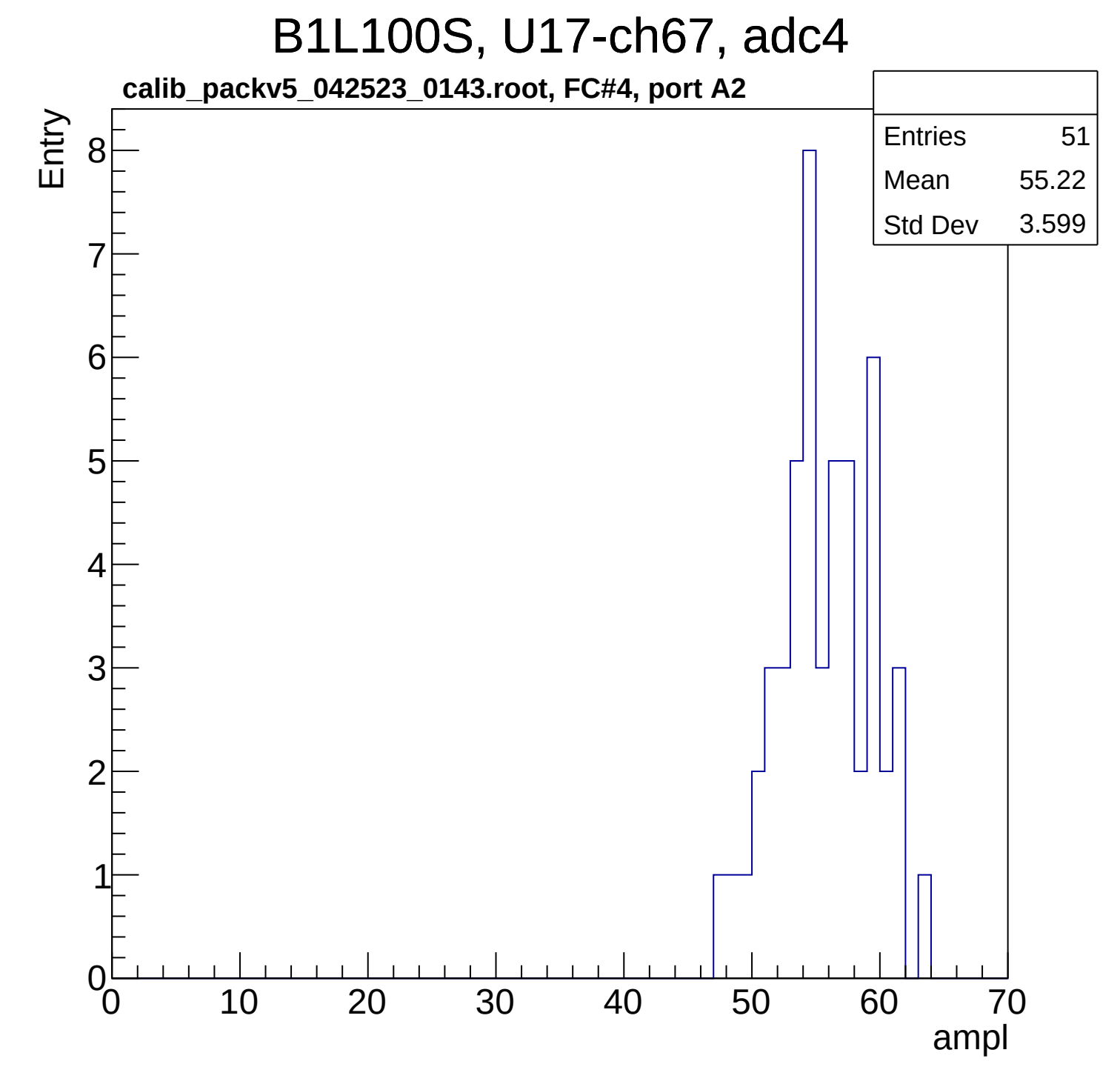
B1L100S, U17-ch67, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 55.22
Std Dev 3.599
Entry
ampl
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2
3
4
5
6
7
8
0
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20
30
40
50
60
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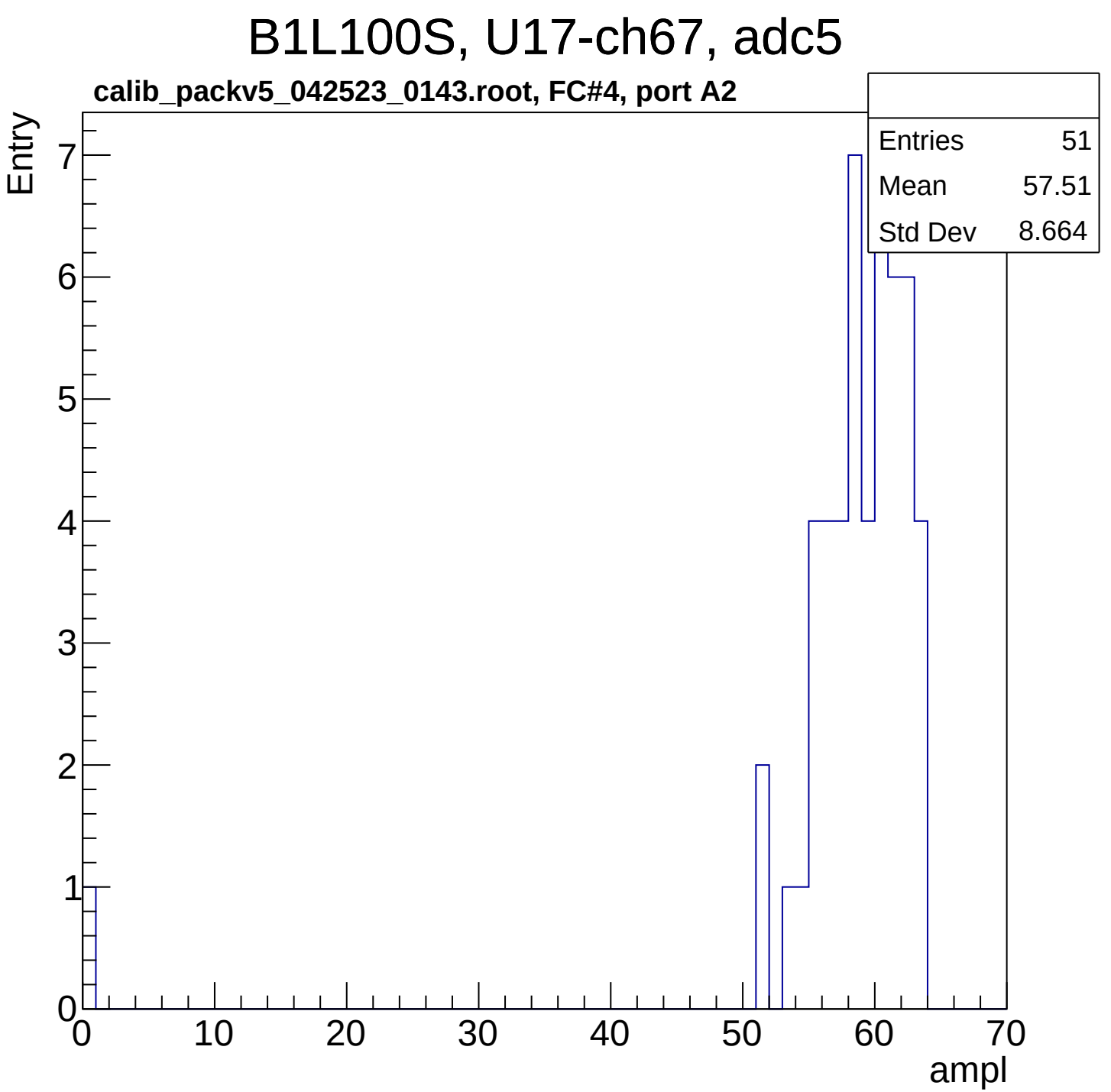
B1L100S, U17-ch67, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 57.51
Std Dev 8.664
Entry
ampl
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1
2
3
4
5
6
7
0
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20
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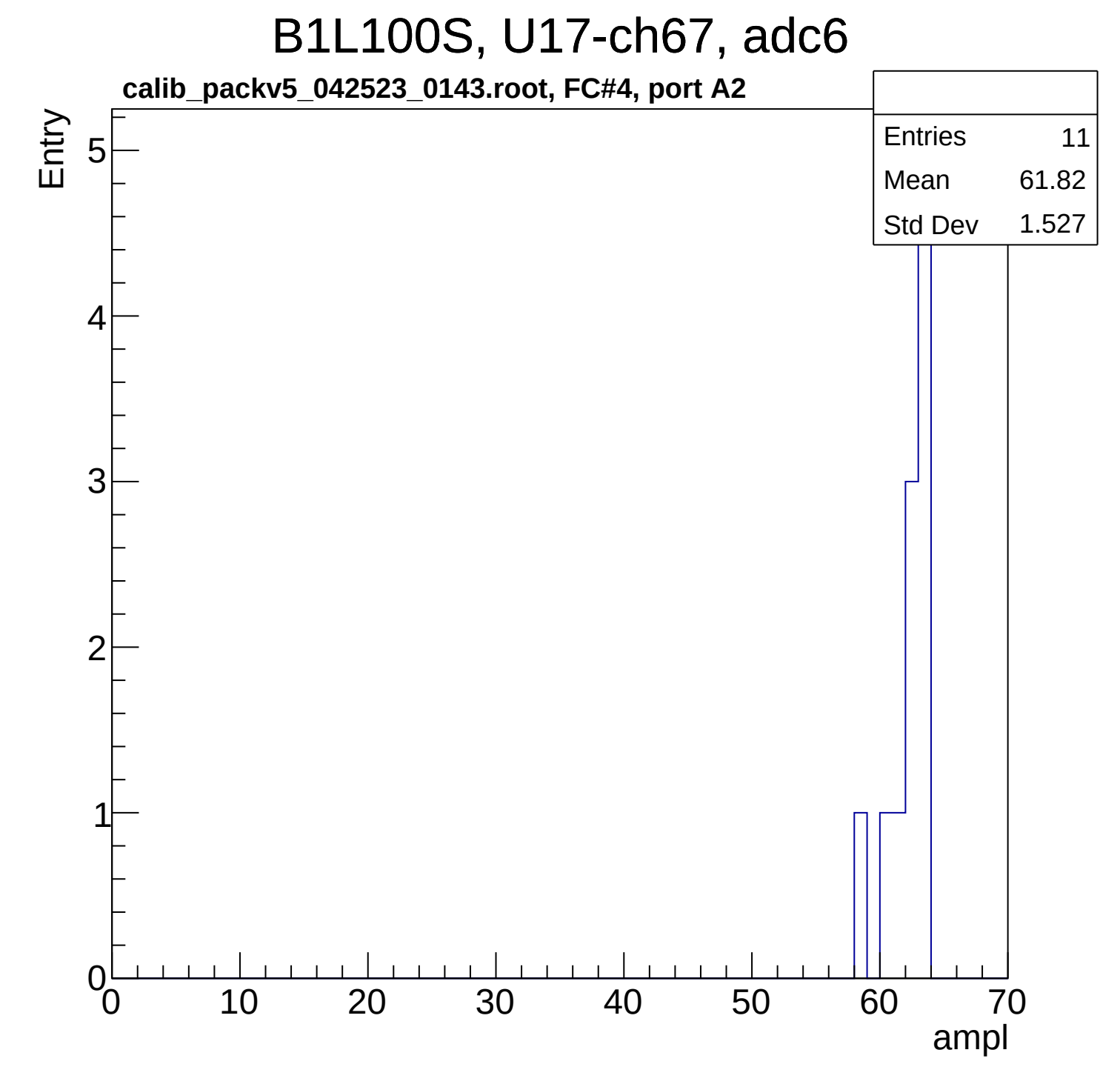
40
50
60
70


B1L100S, U17-ch67, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 11
Mean 61.82
Std Dev 1.527
Entry
0
1
2
3
4
5
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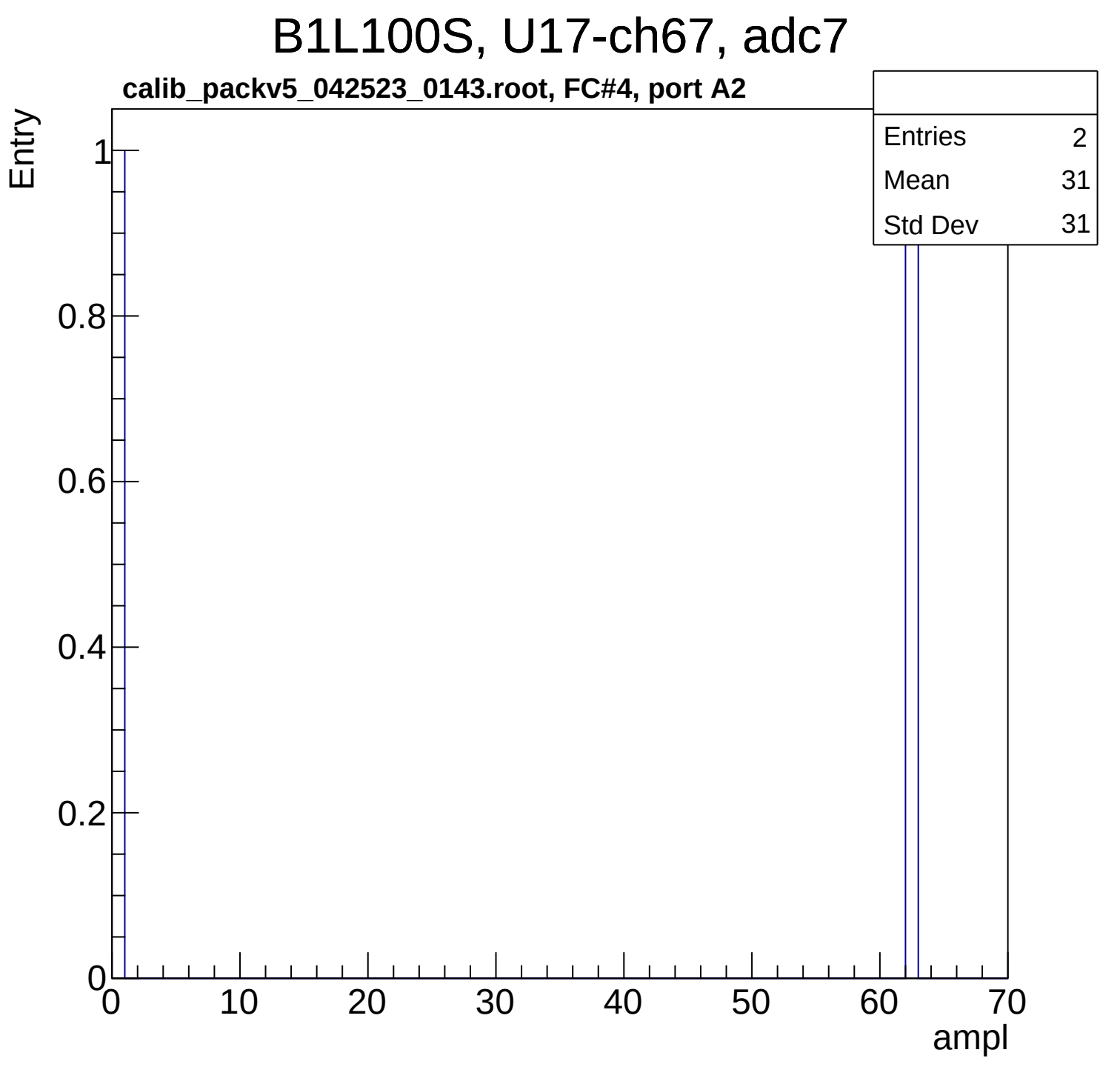
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch67, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 31
Std Dev 31
Entry
1
0.8
0.6
0.4
0.2
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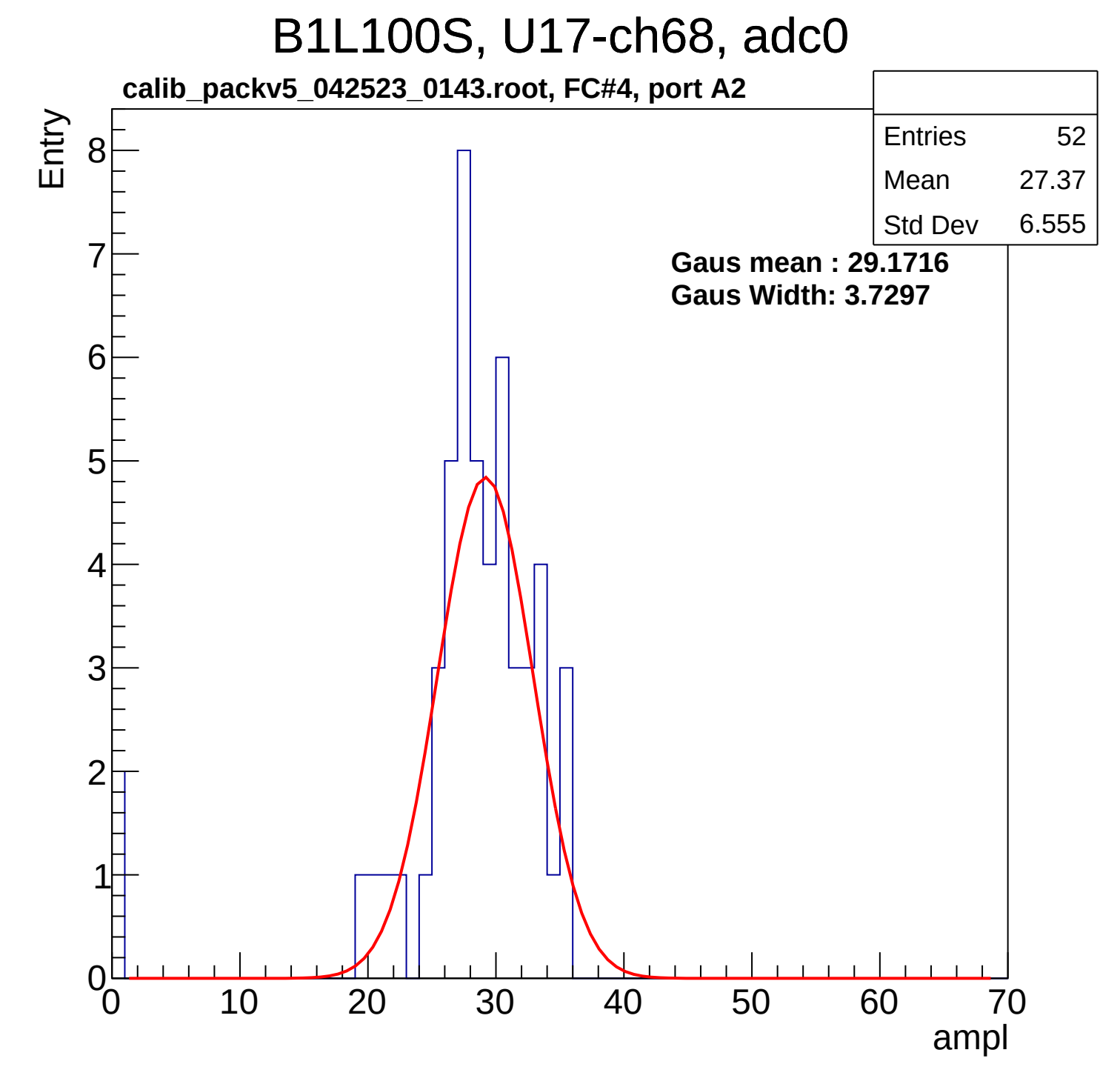
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch68, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 52
Mean 27.37
Std Dev 6.555
Gaus mean : 29.1716
Gaus Width: 3.7297
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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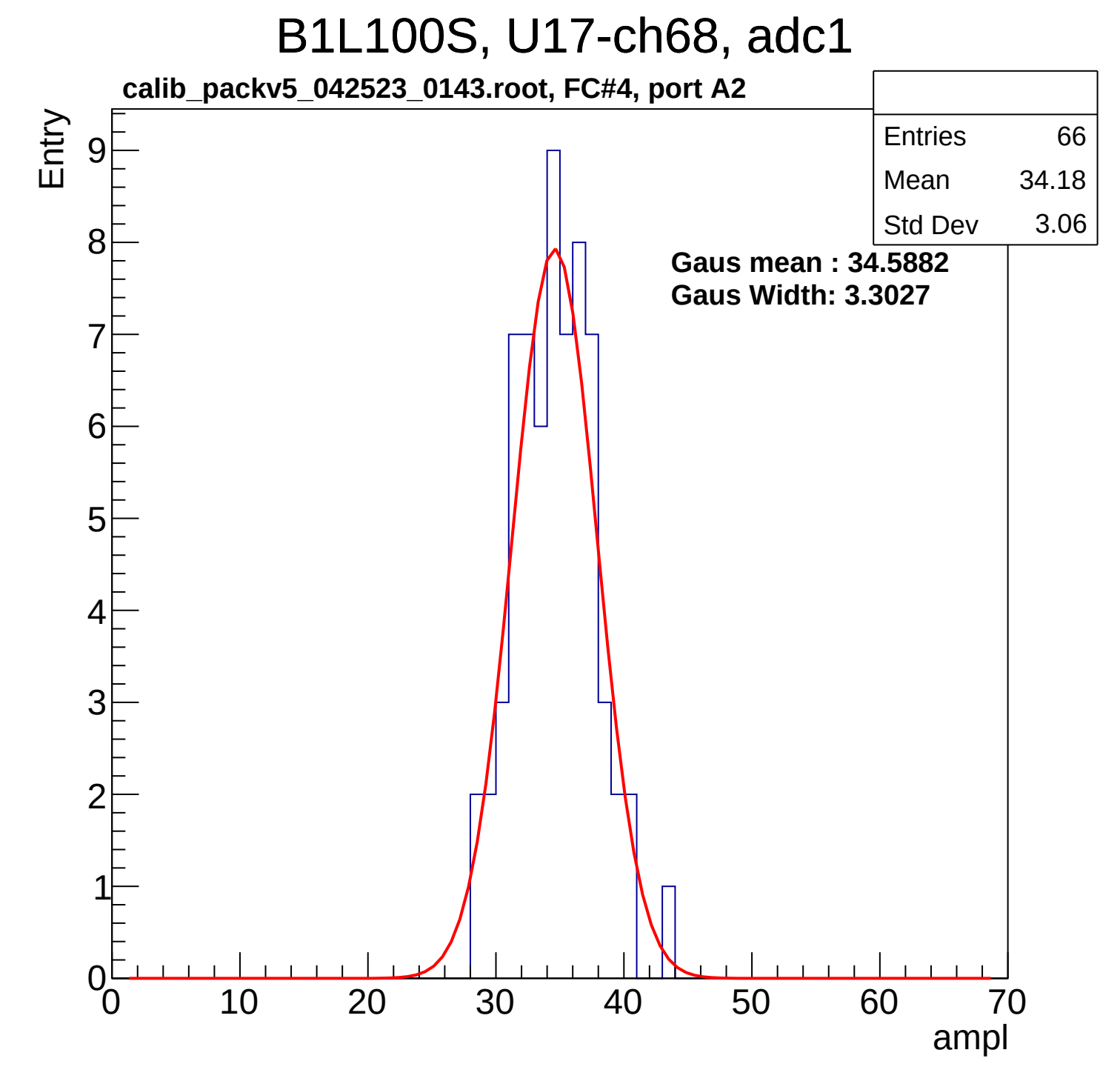
B1L100S, U17-ch68, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 34.18
Std Dev 3.06
Gaus mean : 34.5882
Gaus Width: 3.3027
Entry
ampl
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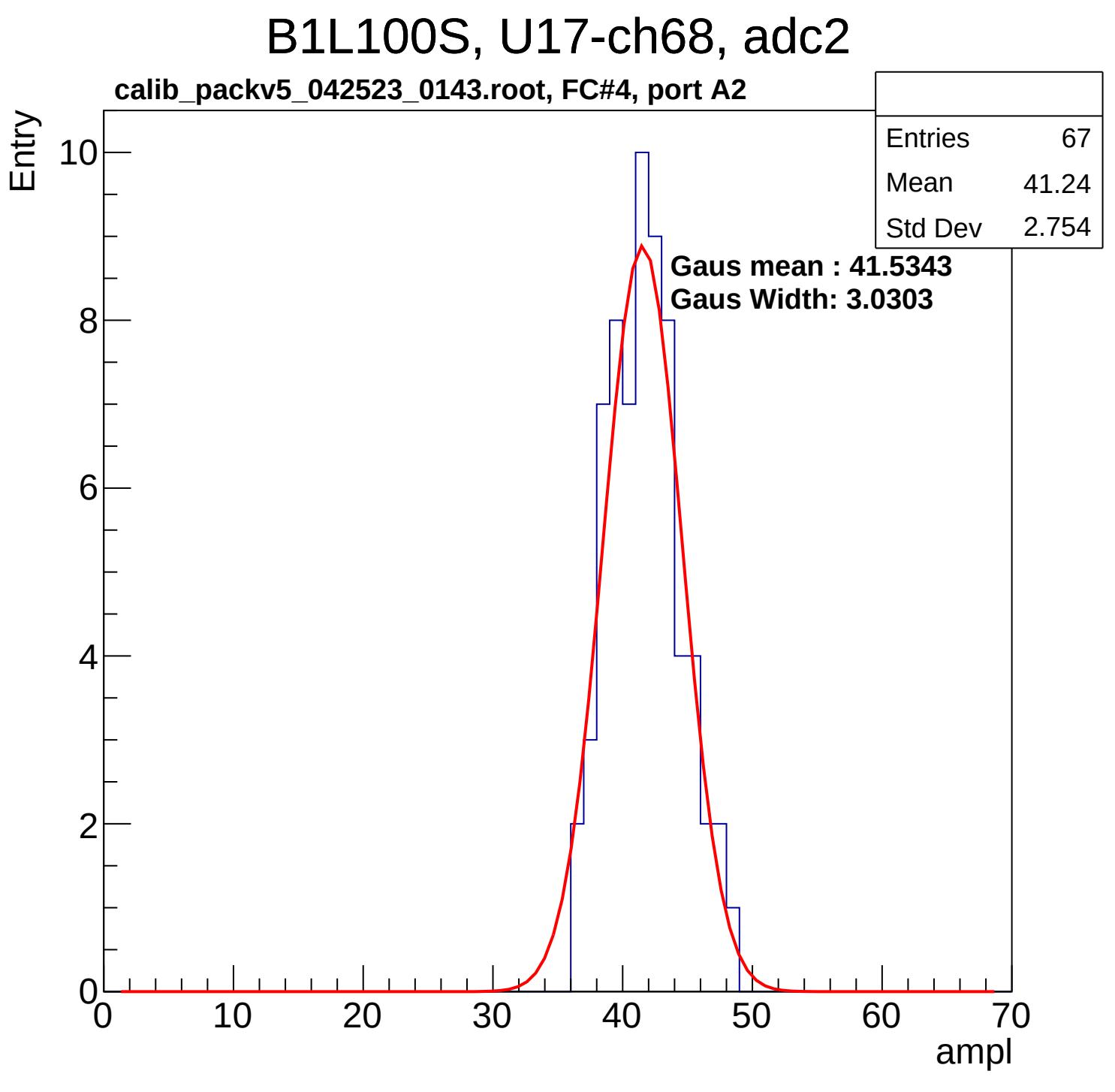
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch68, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 41.24
Std Dev 2.754
Gaus mean : 41.5343
Gaus Width: 3.0303
Entry
ampl
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2
4
6
8
10
0
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20
30
40
50
60
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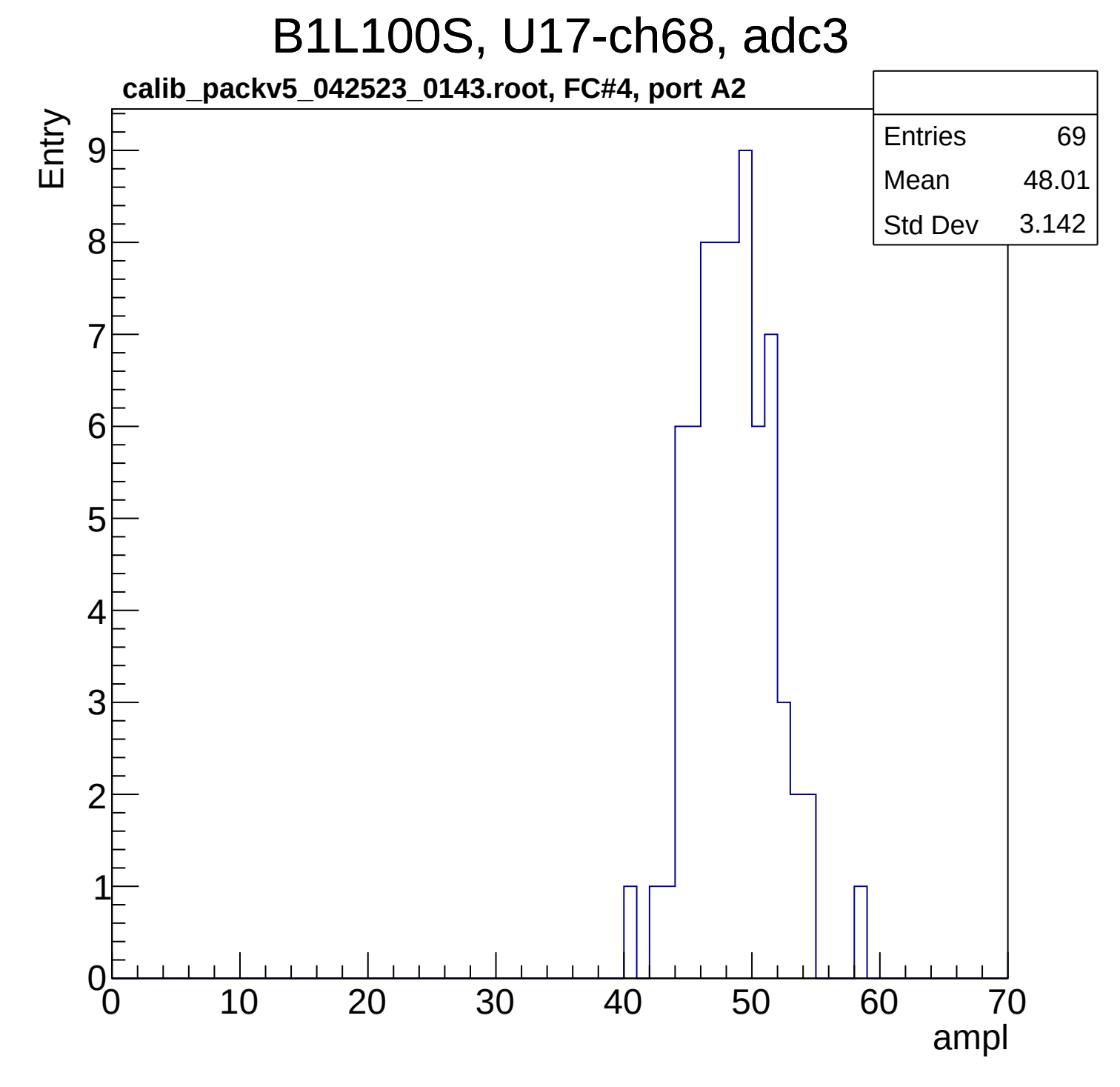
B1L100S, U17-ch68, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 48.01
Std Dev 3.142
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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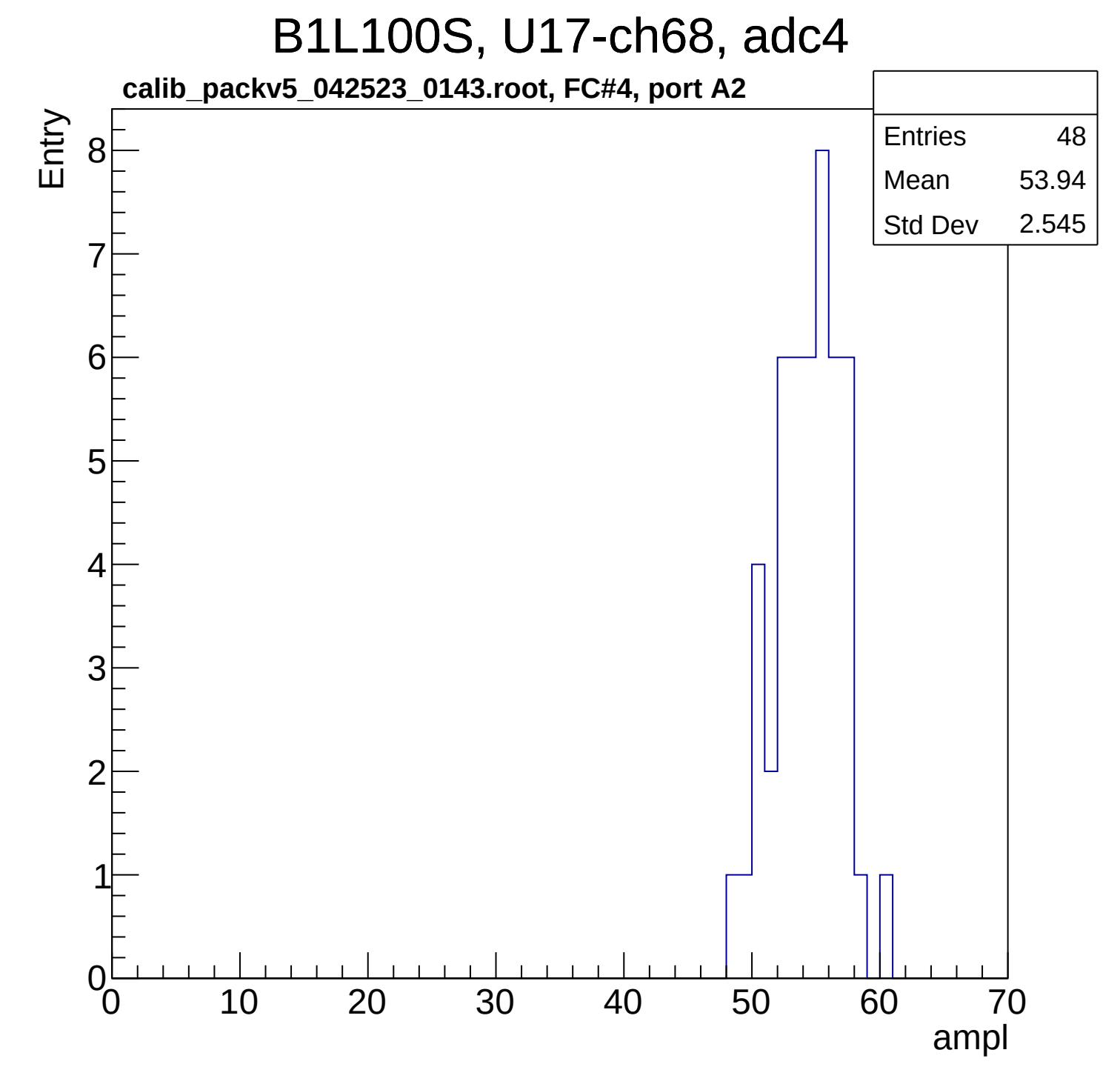
B1L100S, U17-ch68, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 48
Mean 53.94
Std Dev 2.545
Entry
ampl
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4
5
6
7
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0
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20
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40
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60
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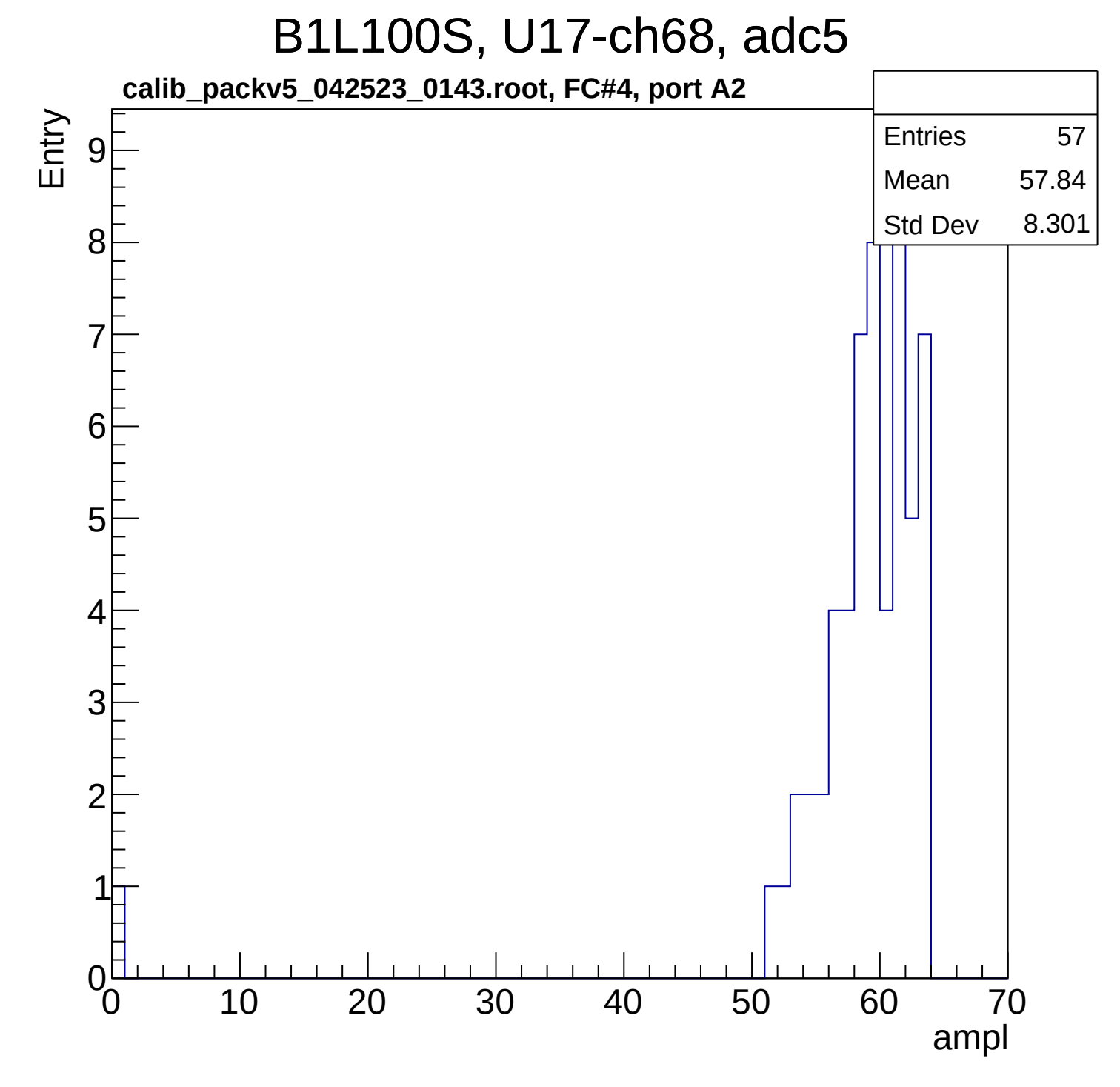
B1L100S, U17-ch68, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 57.84
Std Dev 8.301
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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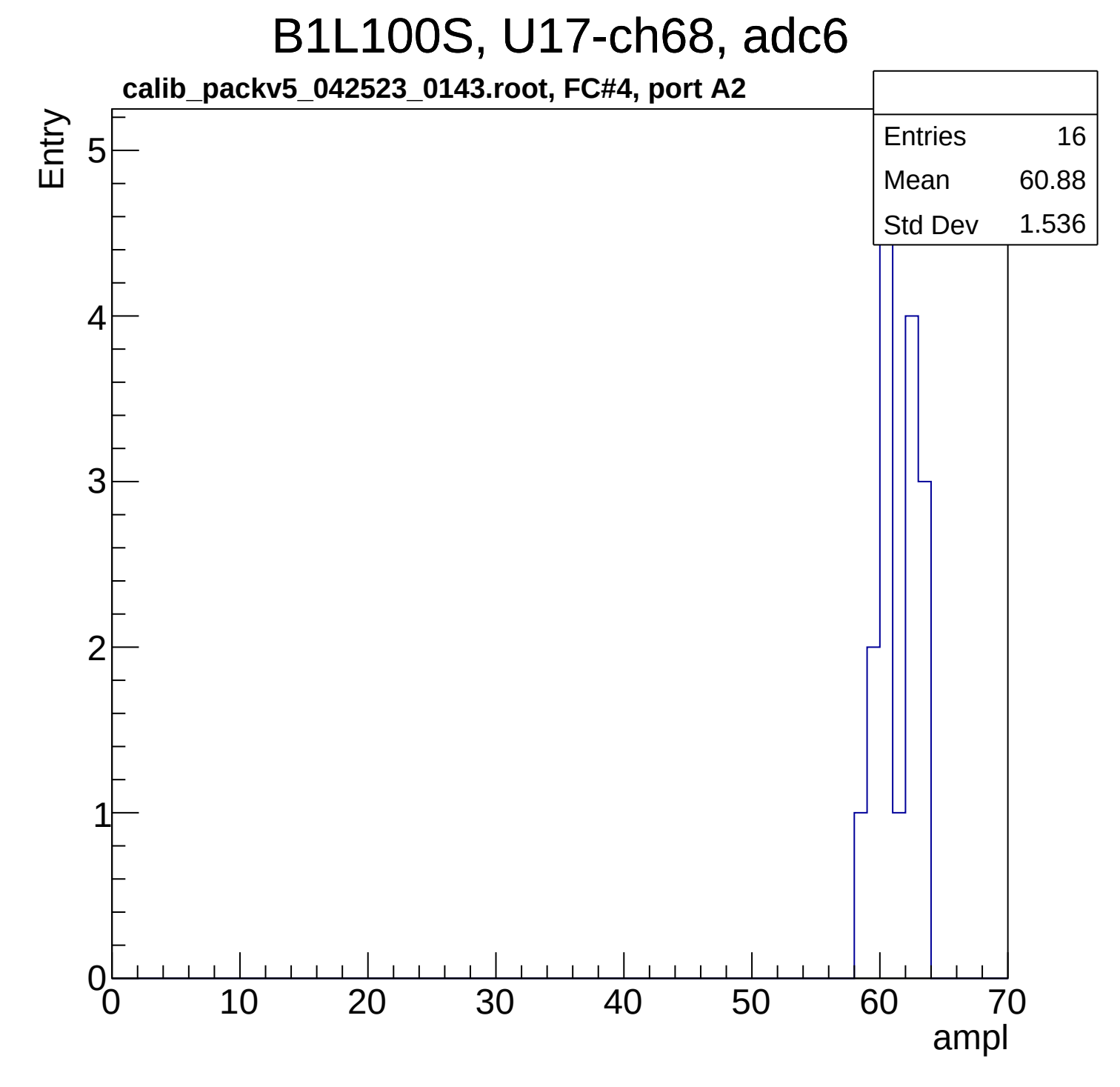
B1L100S, U17-ch68, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 16
Mean 60.88
Std Dev 1.536
Entry
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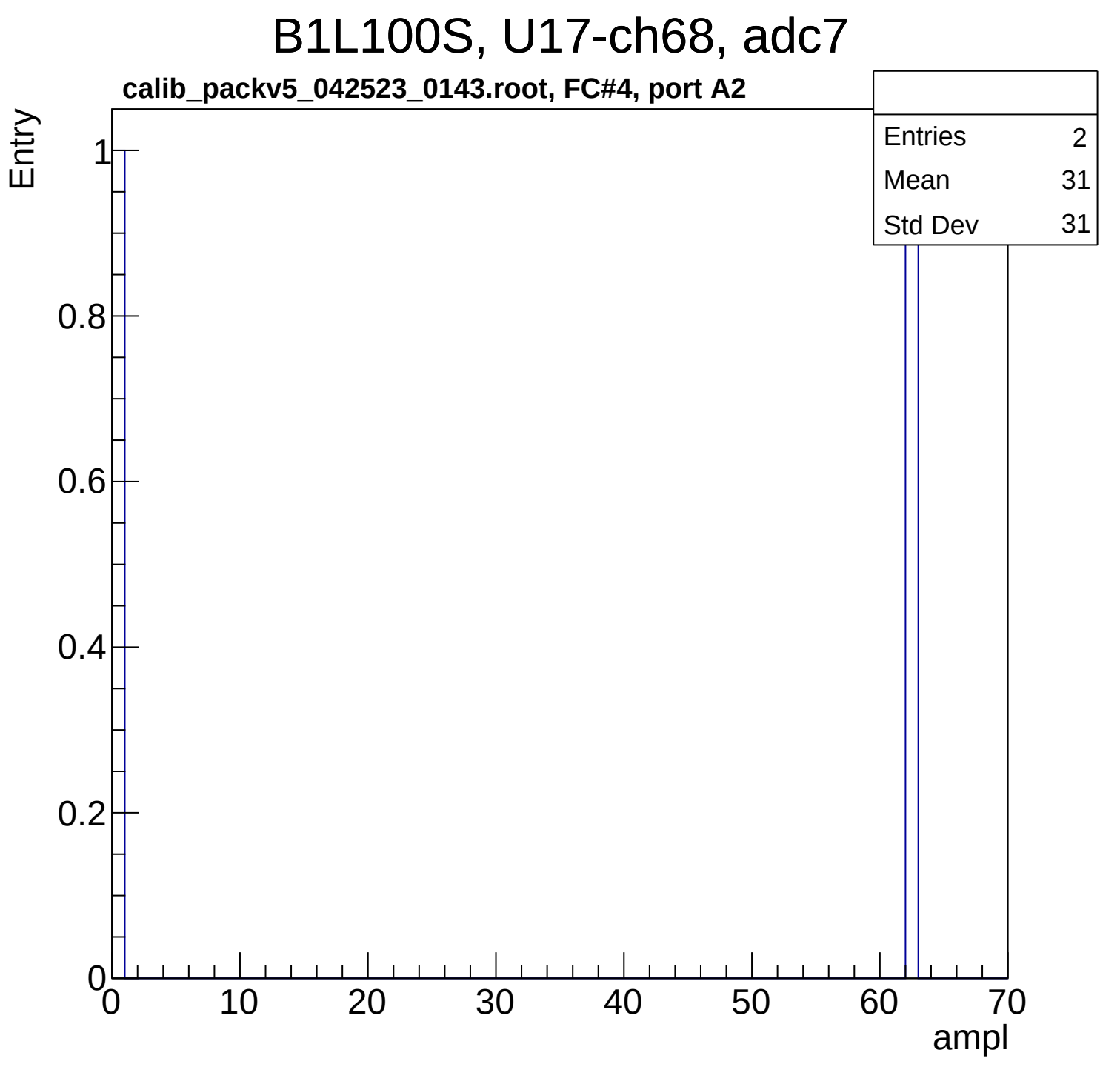
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch68, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 31
Std Dev 31
Entry
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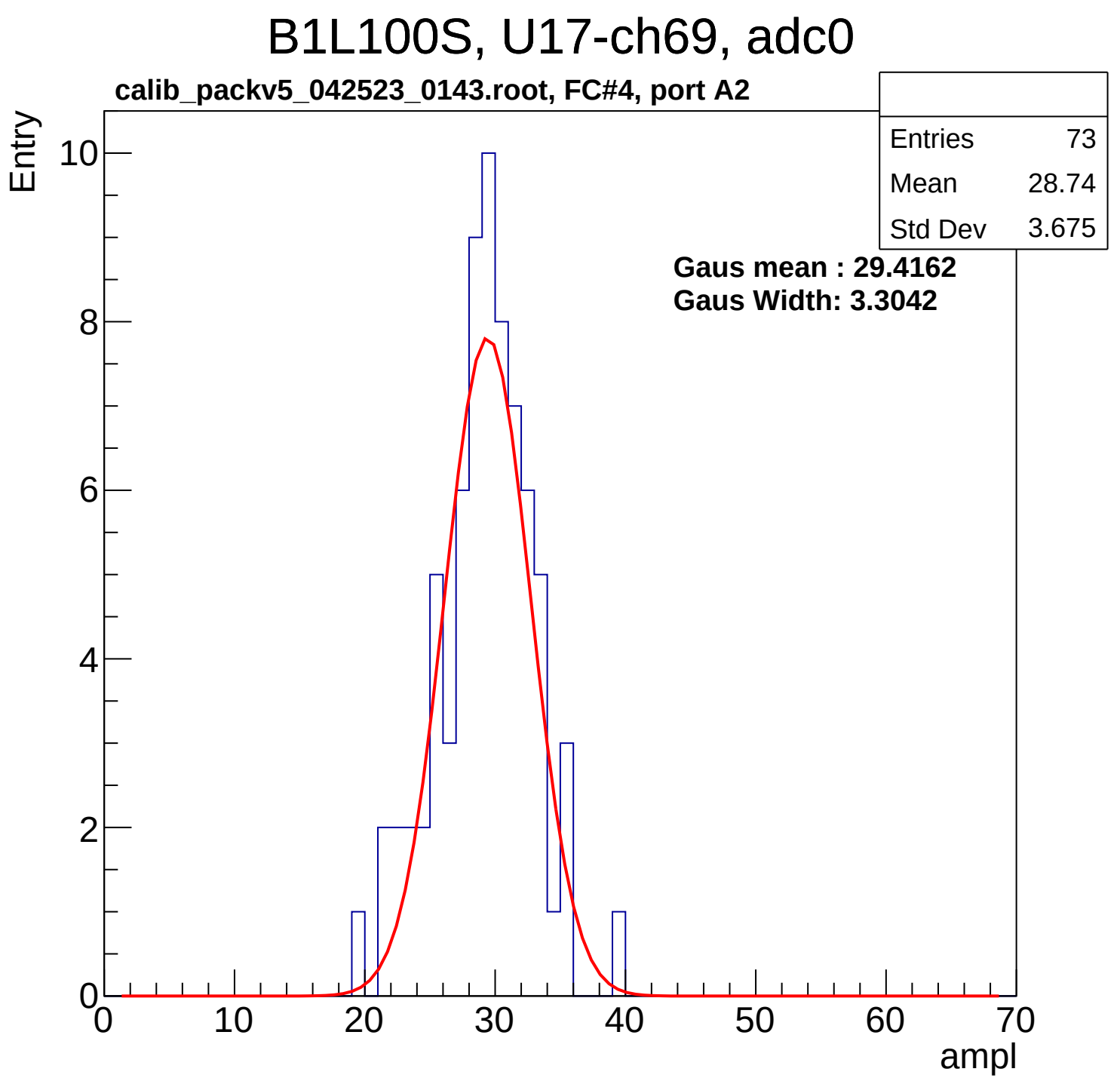
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch69, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 28.74
Std Dev 3.675
Gaus mean : 29.4162
Gaus Width: 3.3042
Entry
ampl
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6
8
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0
10
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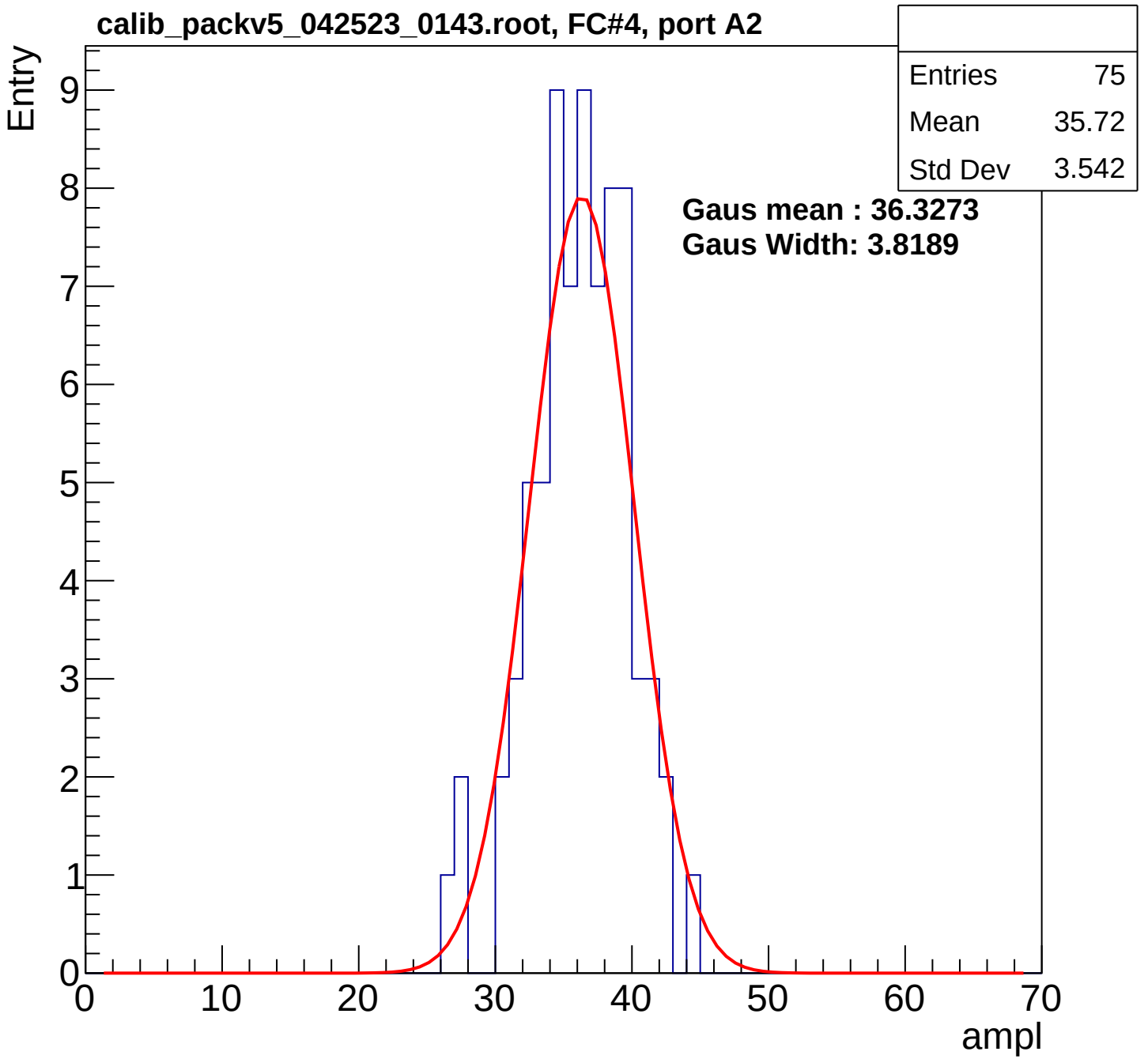
B1L100S, U17-ch69, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 75
Mean 35.72
Std Dev 3.542
Gaus mean : 36.3273
Gaus Width: 3.8189
Entry
ampl
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3
4
5
6
7
8
9
0
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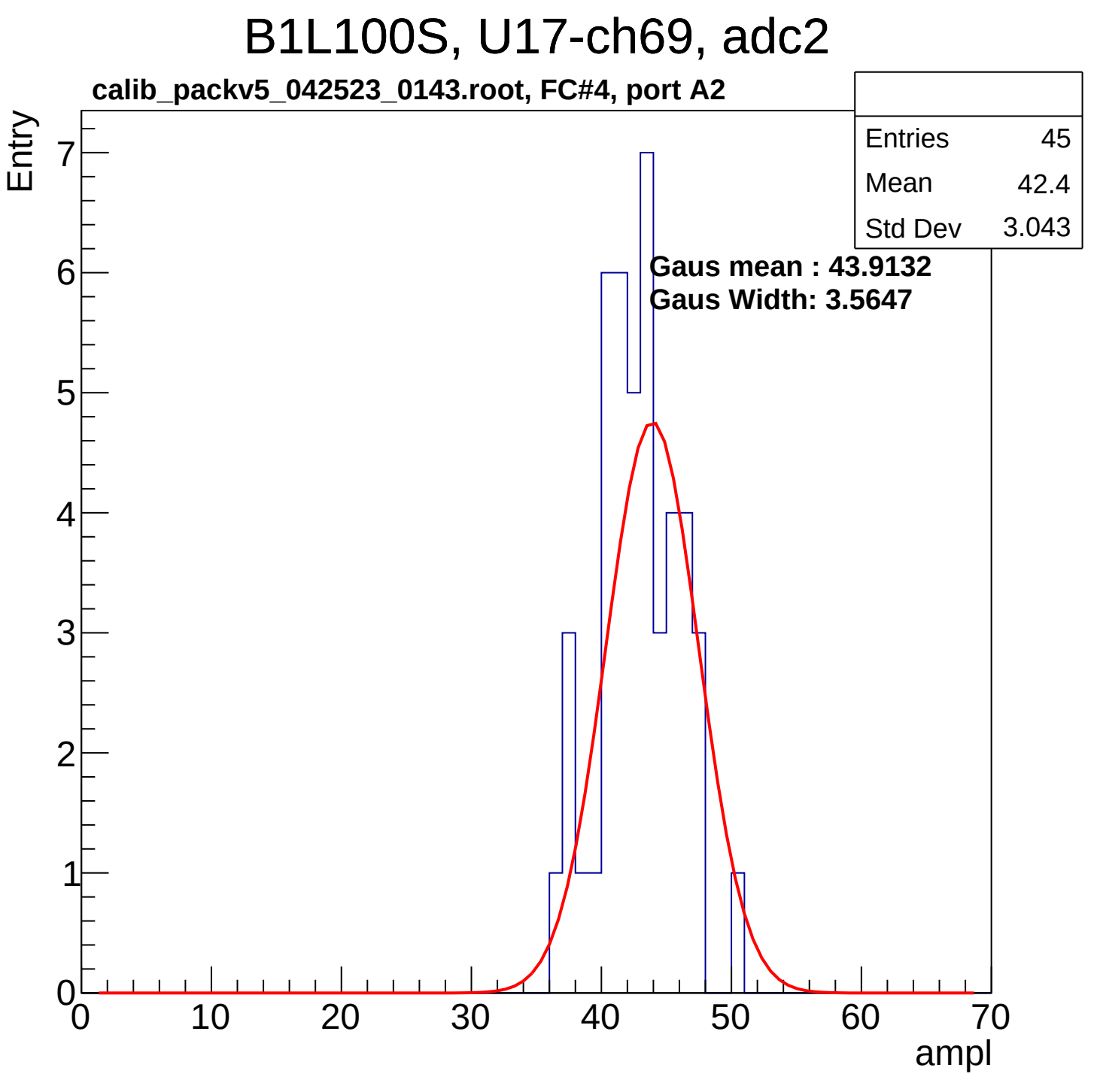
B1L100S, U17-ch69, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 45
Mean 42.4
Std Dev 3.043
Gaus mean : 43.9132
Gaus Width: 3.5647
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
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60
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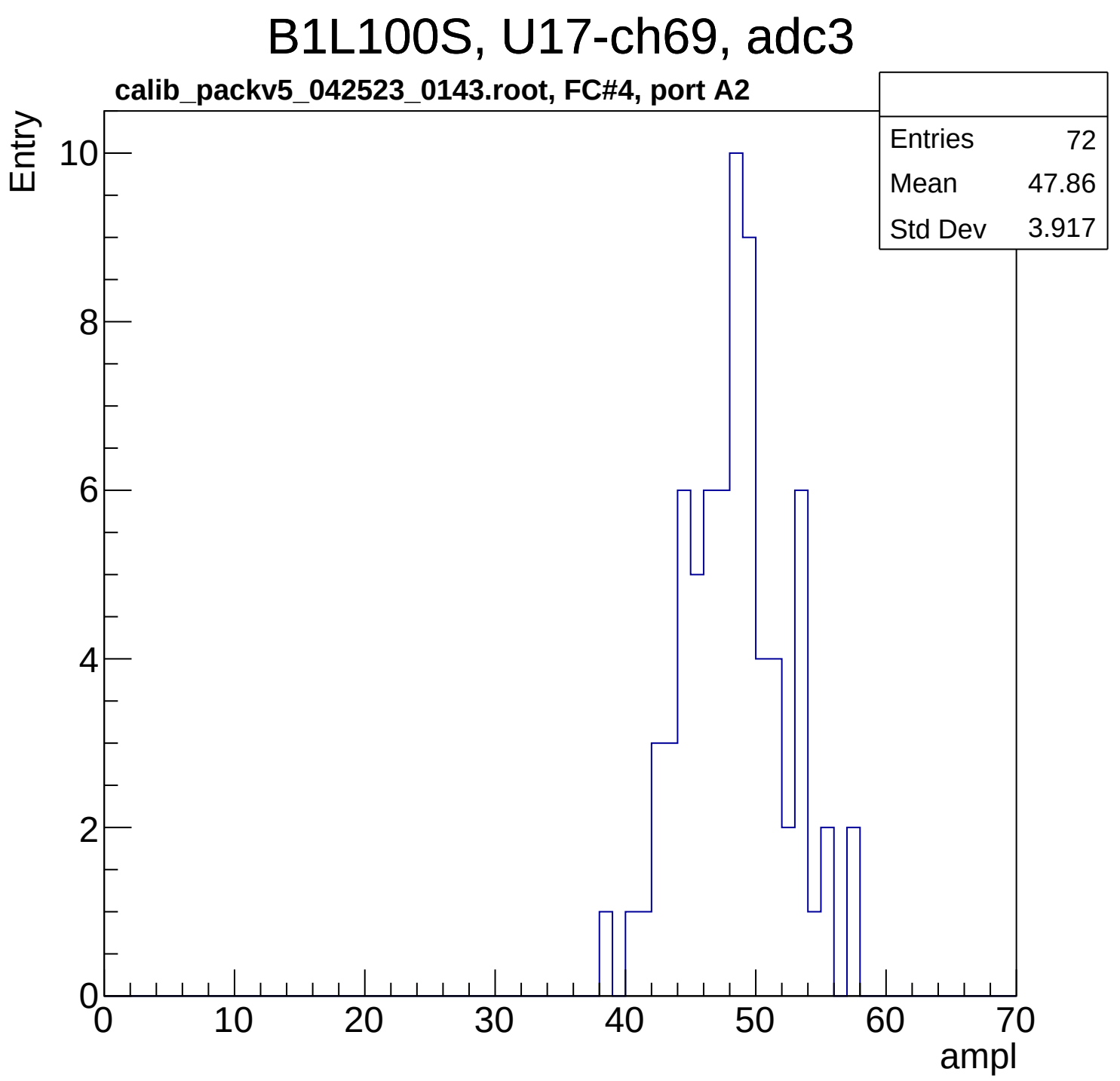
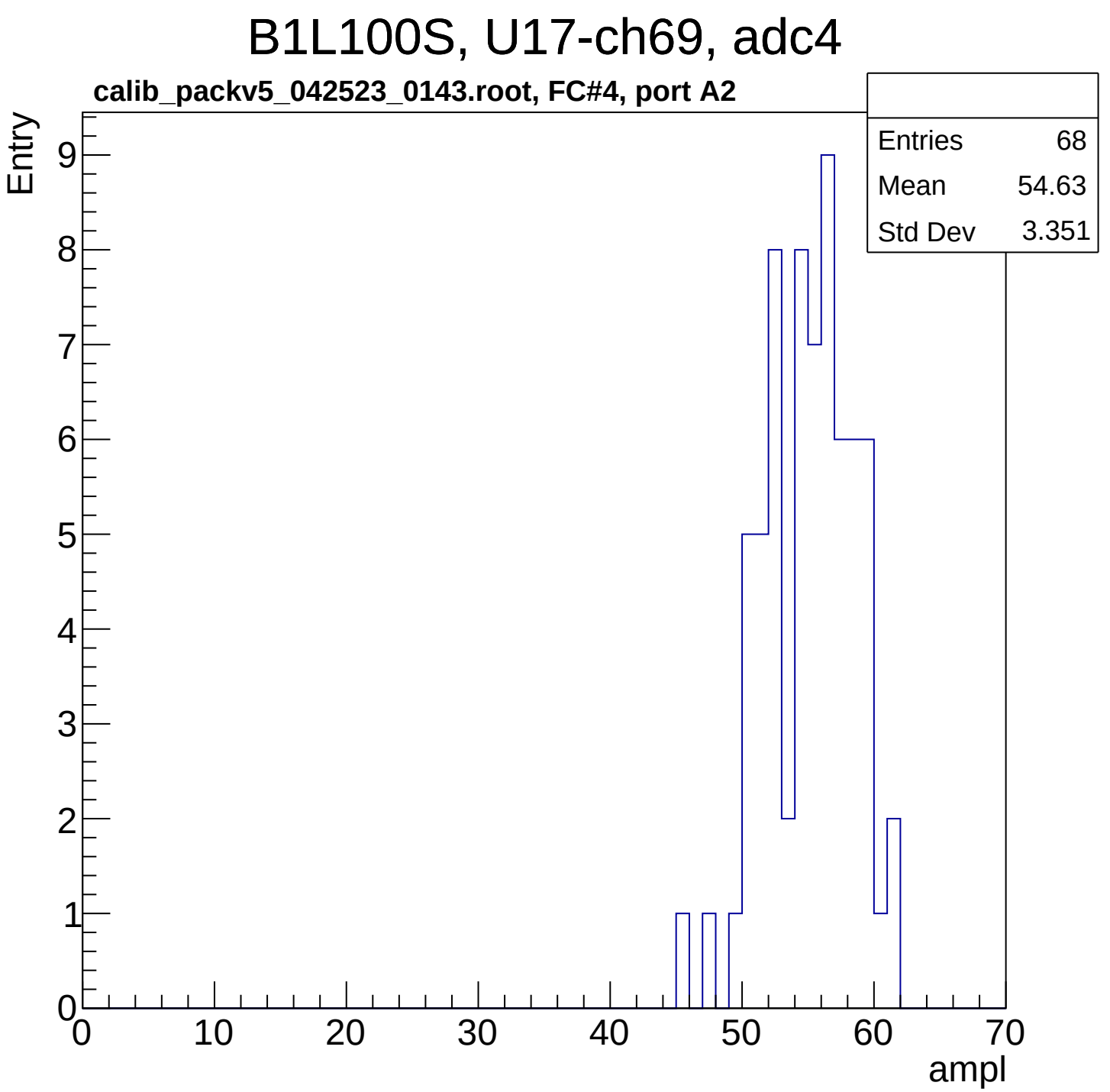
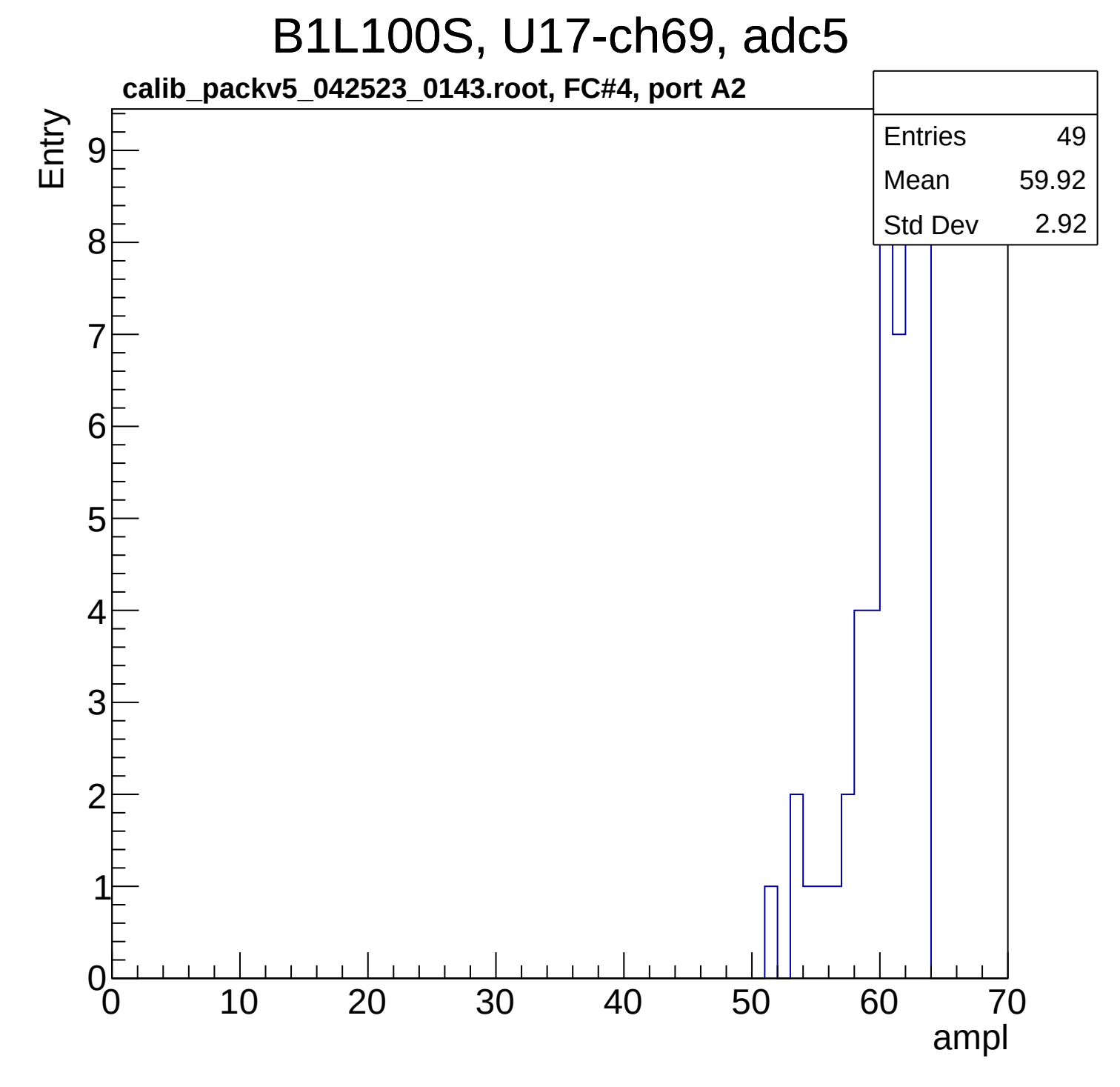
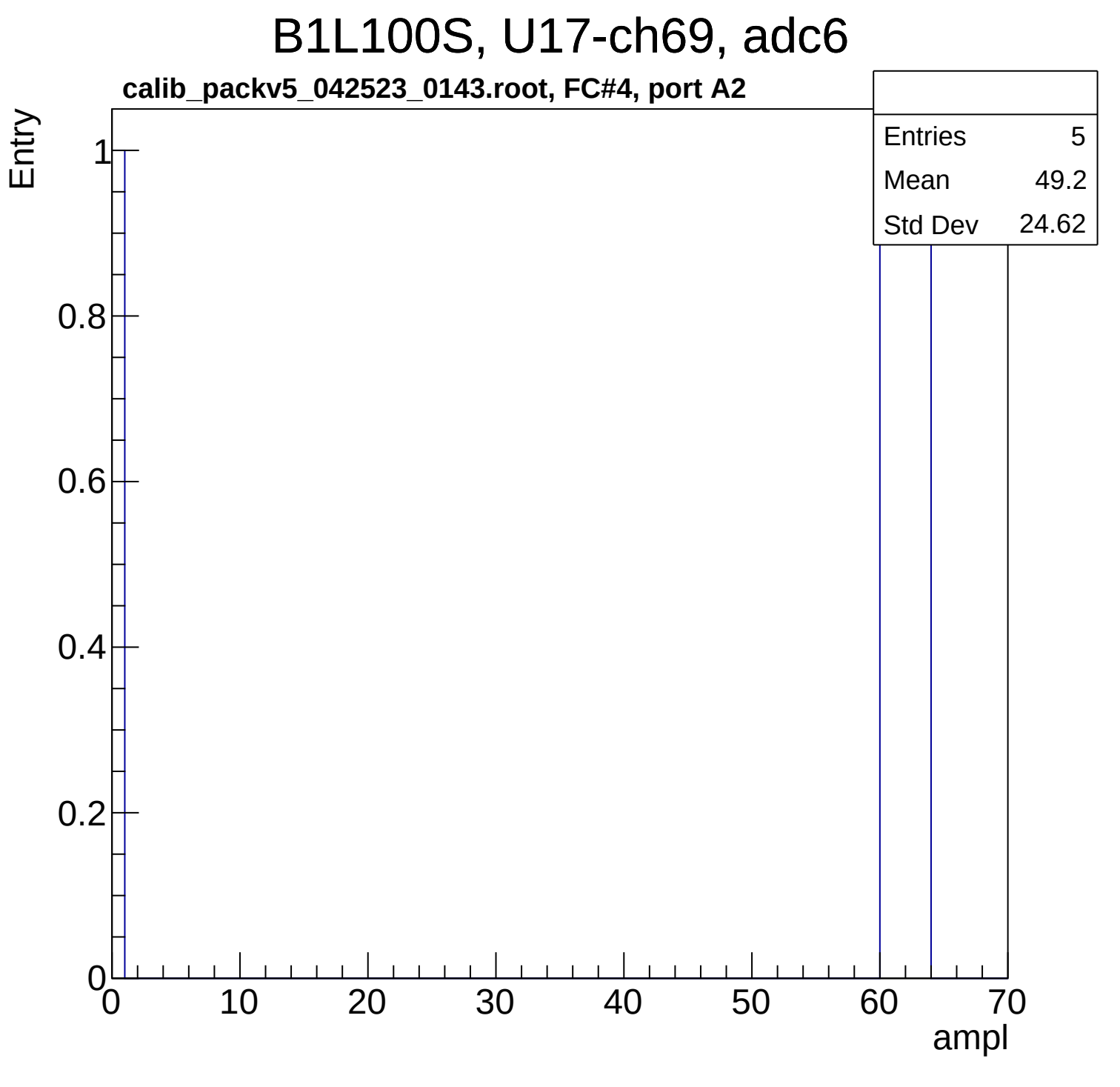
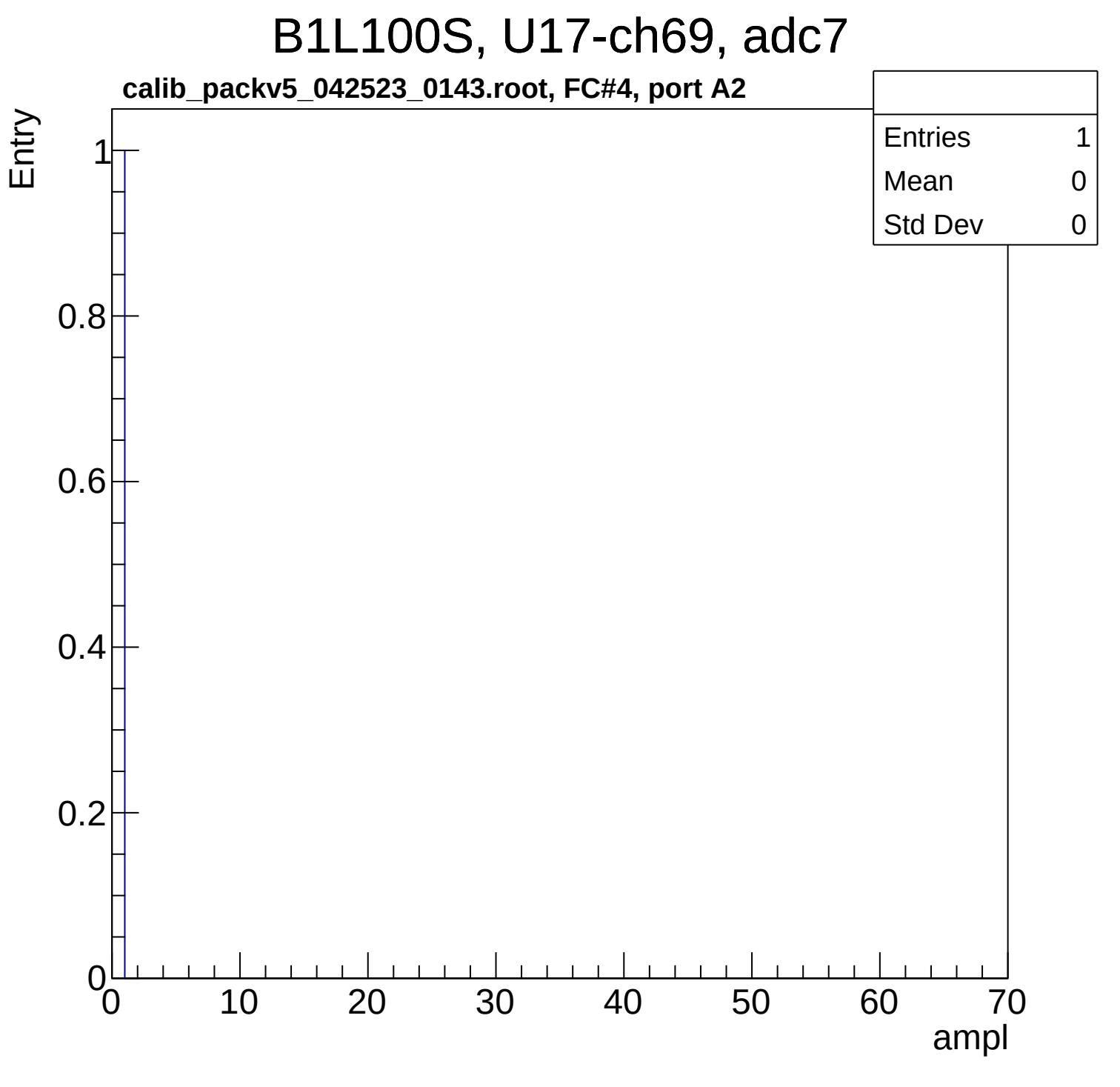
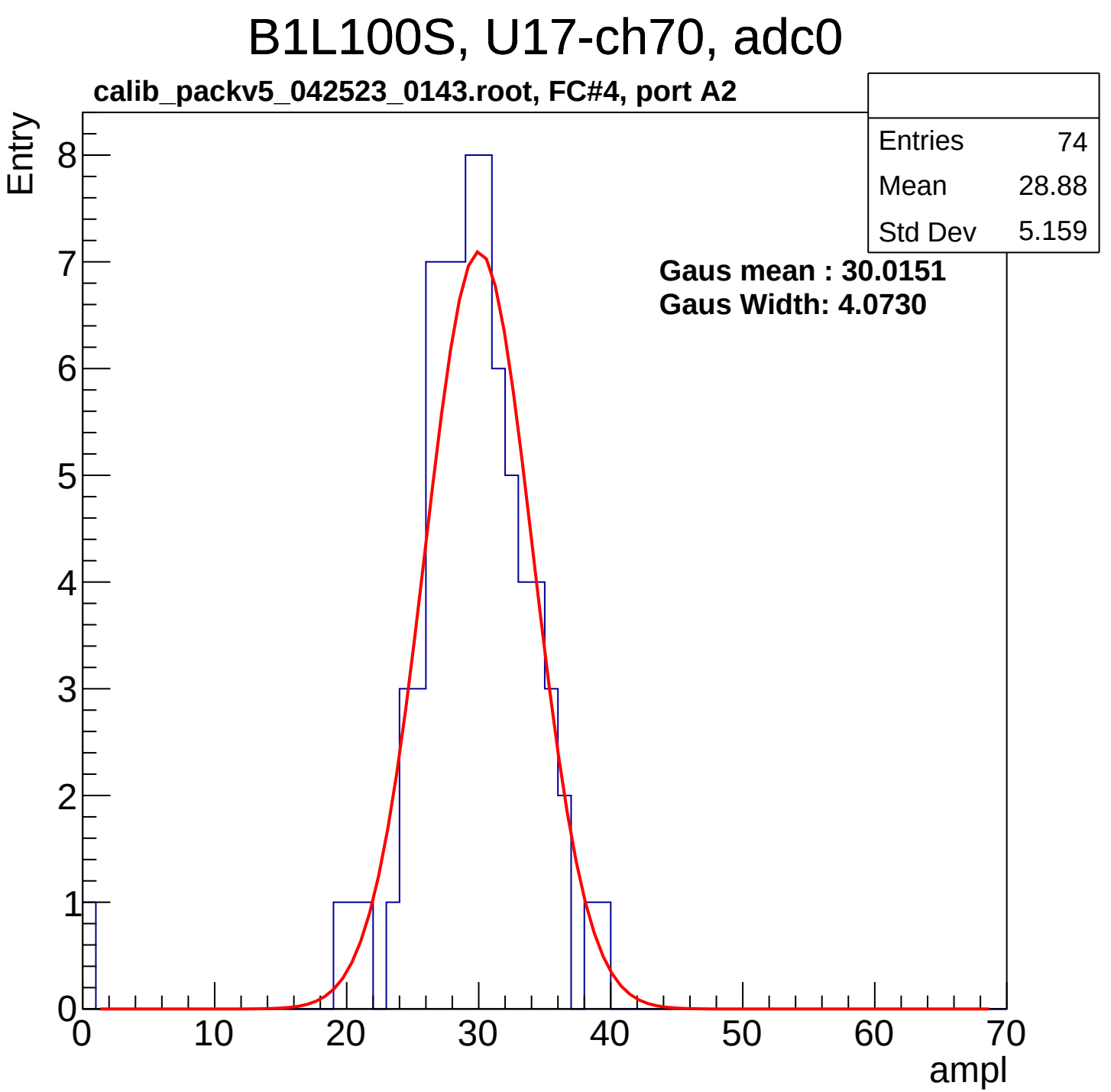

B1L100S, U17-ch69, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 47.86
Std Dev 3.917
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

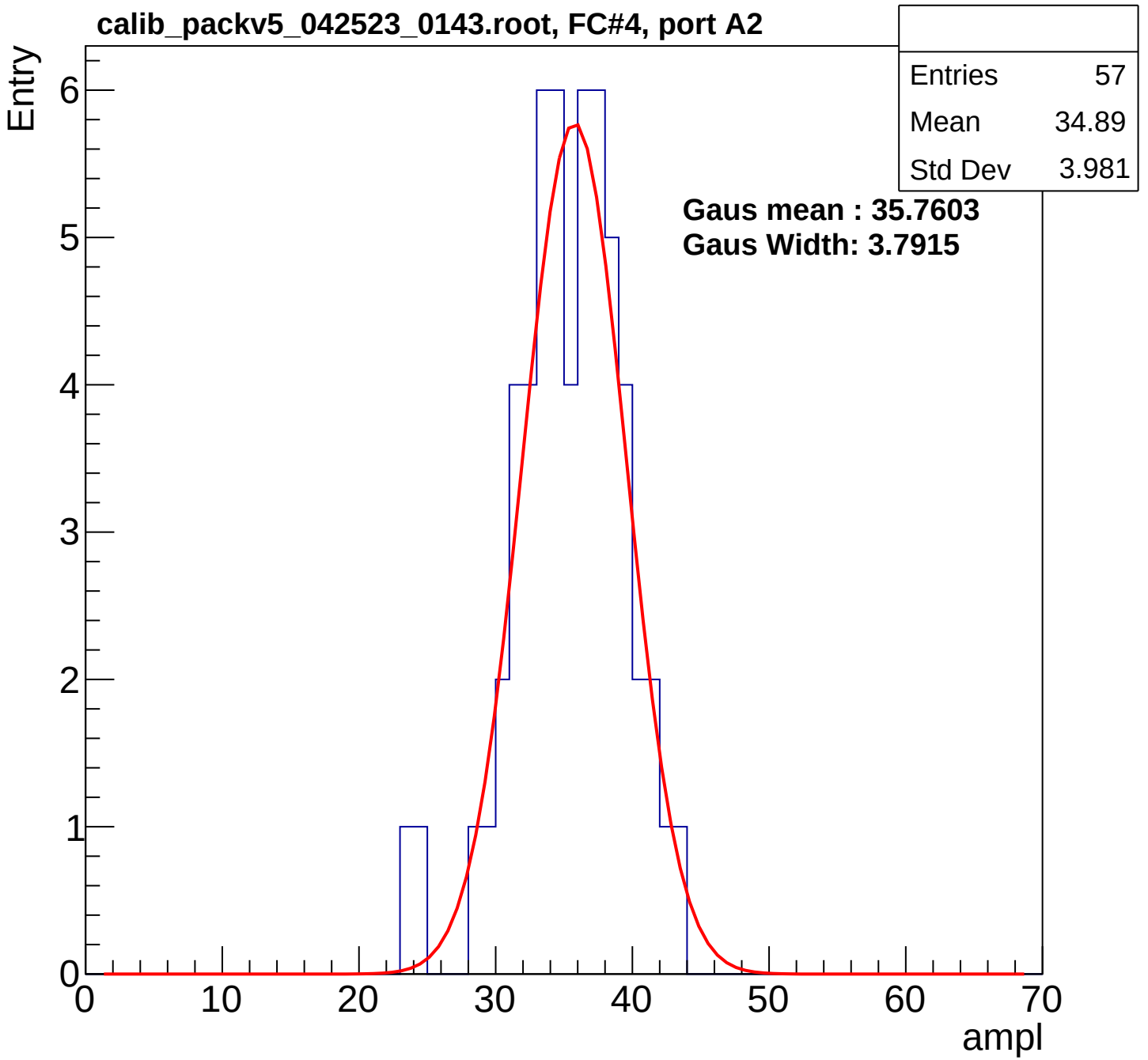

B1L100S, U17-ch69, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 54.63
Std Dev 3.351
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

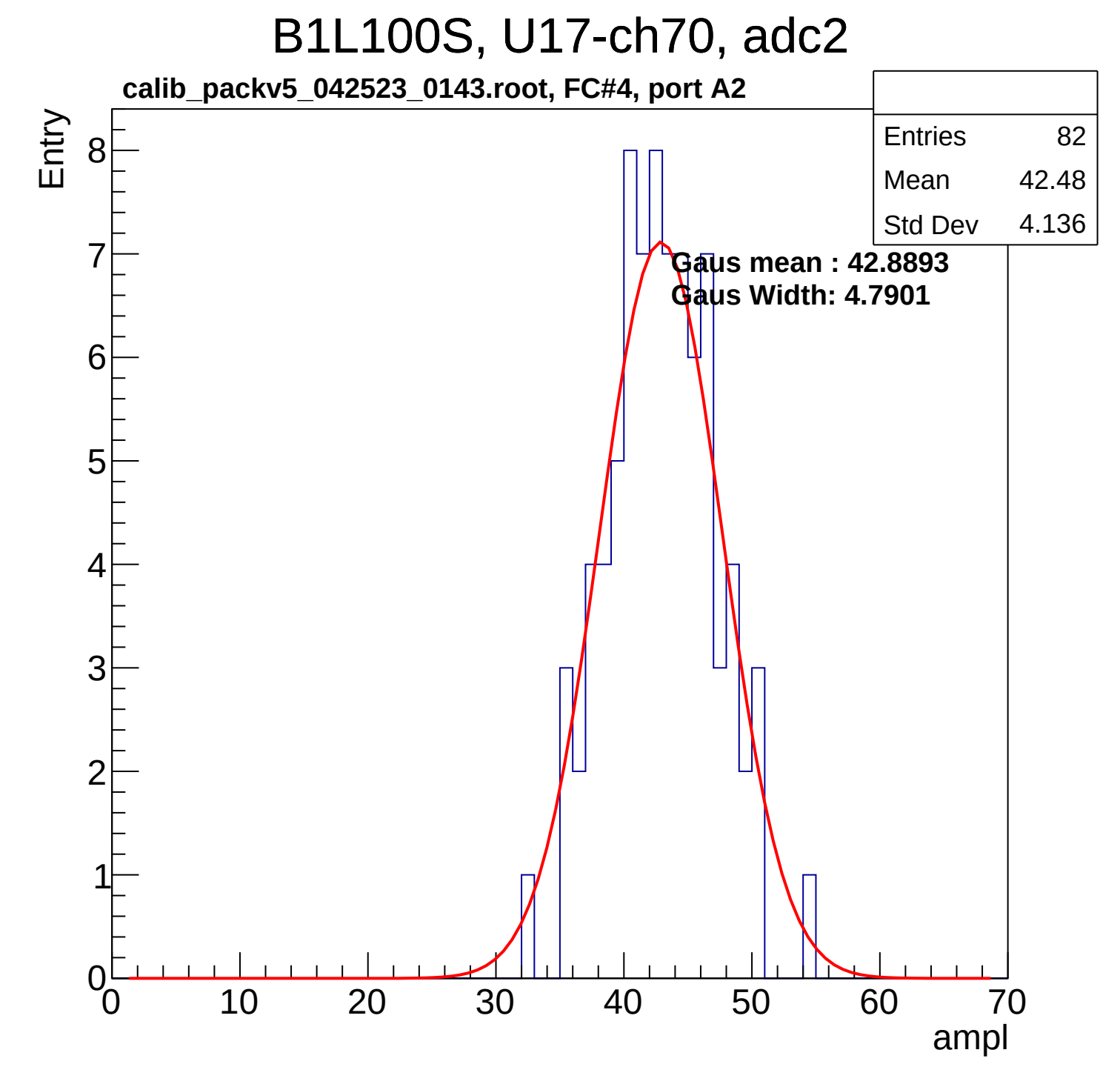

B1L100S, U17-ch69, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 49
Mean 59.92
Std Dev 2.92
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

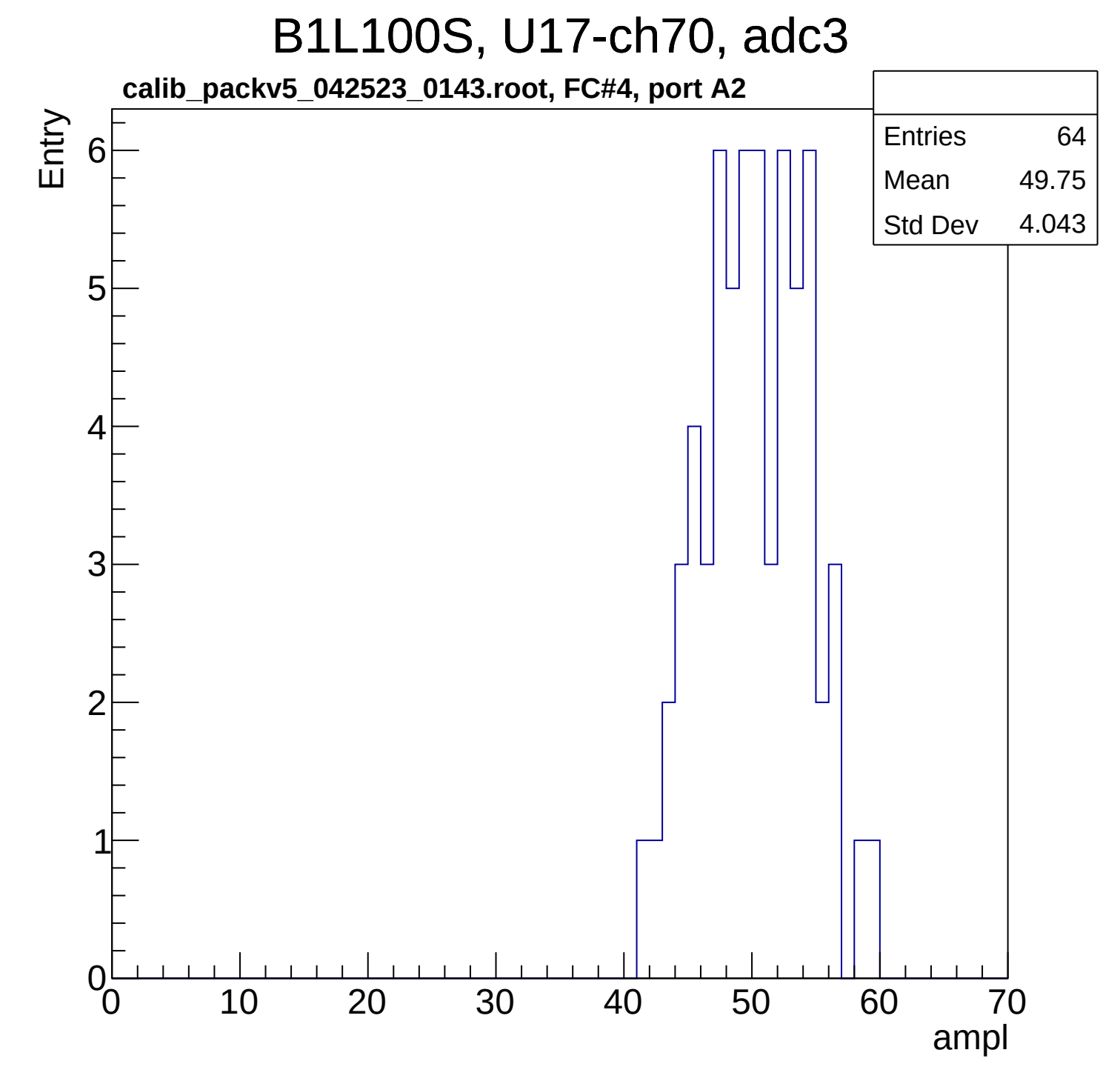

B1L100S, U17-ch69, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 5
Mean 49.2
Std Dev 24.62
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

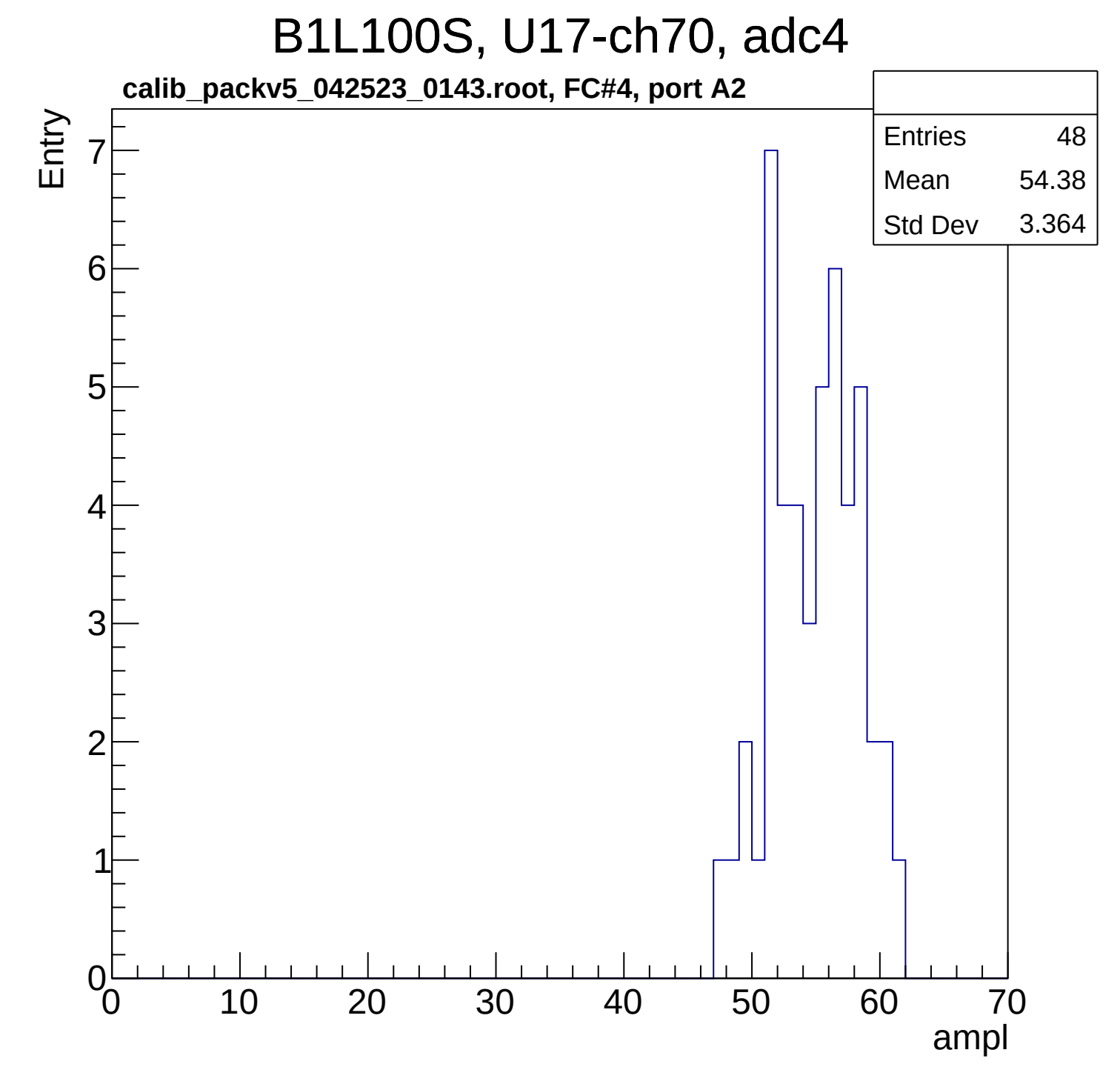

B1L100S, U17-ch69, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

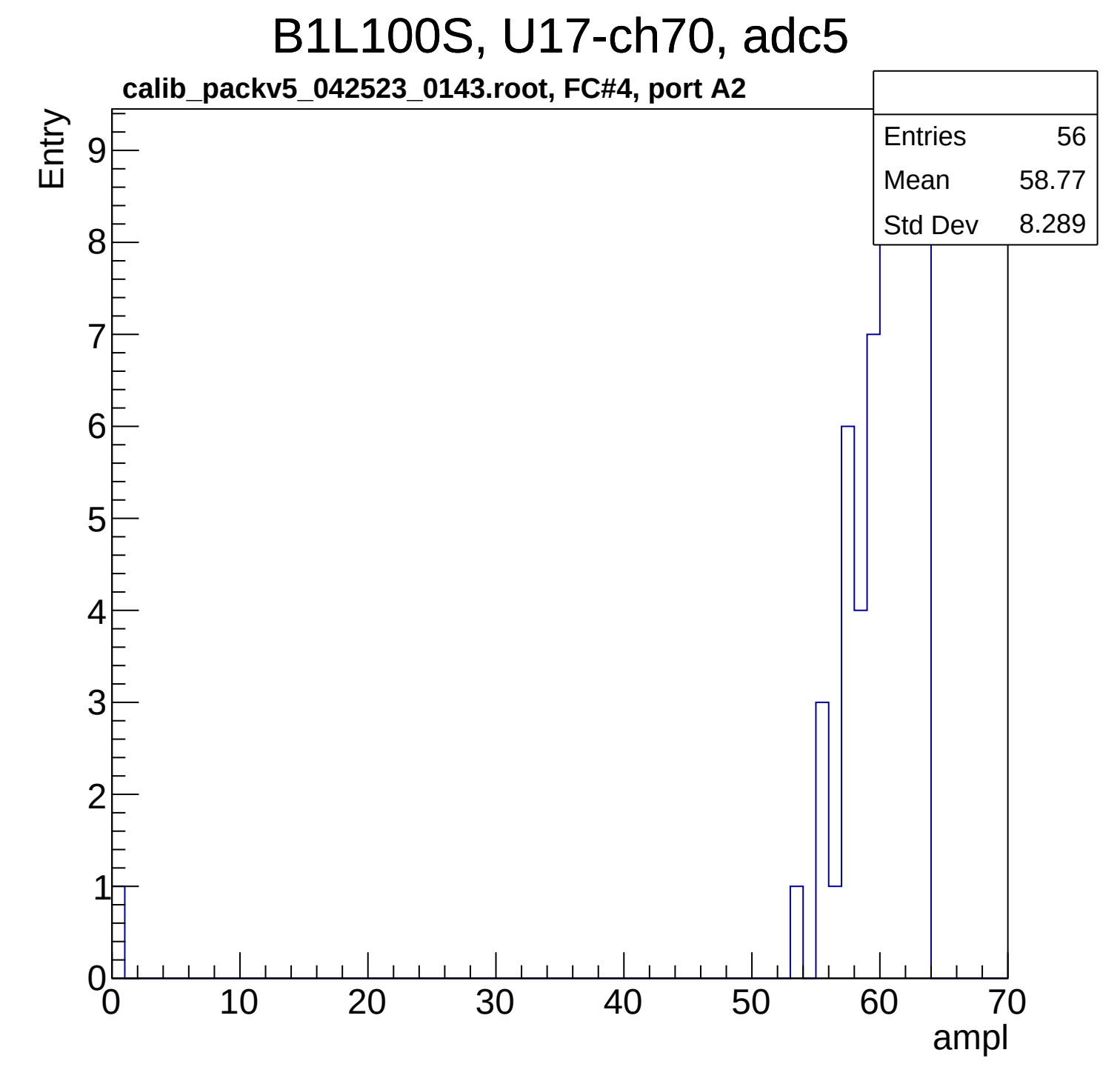

B1L100S, U17-ch70, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 74
Mean 28.88
Std Dev 5.159
Gaus mean : 30.0151
Gaus Width: 4.0730
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch70, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 34.89
Std Dev 3.981
Gaus mean : 35.7603
Gaus Width: 3.7915
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L100S, U17-ch70, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 82
Mean 42.48
Std Dev 4.136
Gaus mean : 42.8893
Gaus Width: 4.7901
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch70, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 49.75
Std Dev 4.043
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch70, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 48
Mean 54.38
Std Dev 3.364
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U17-ch70, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 58.77
Std Dev 8.289
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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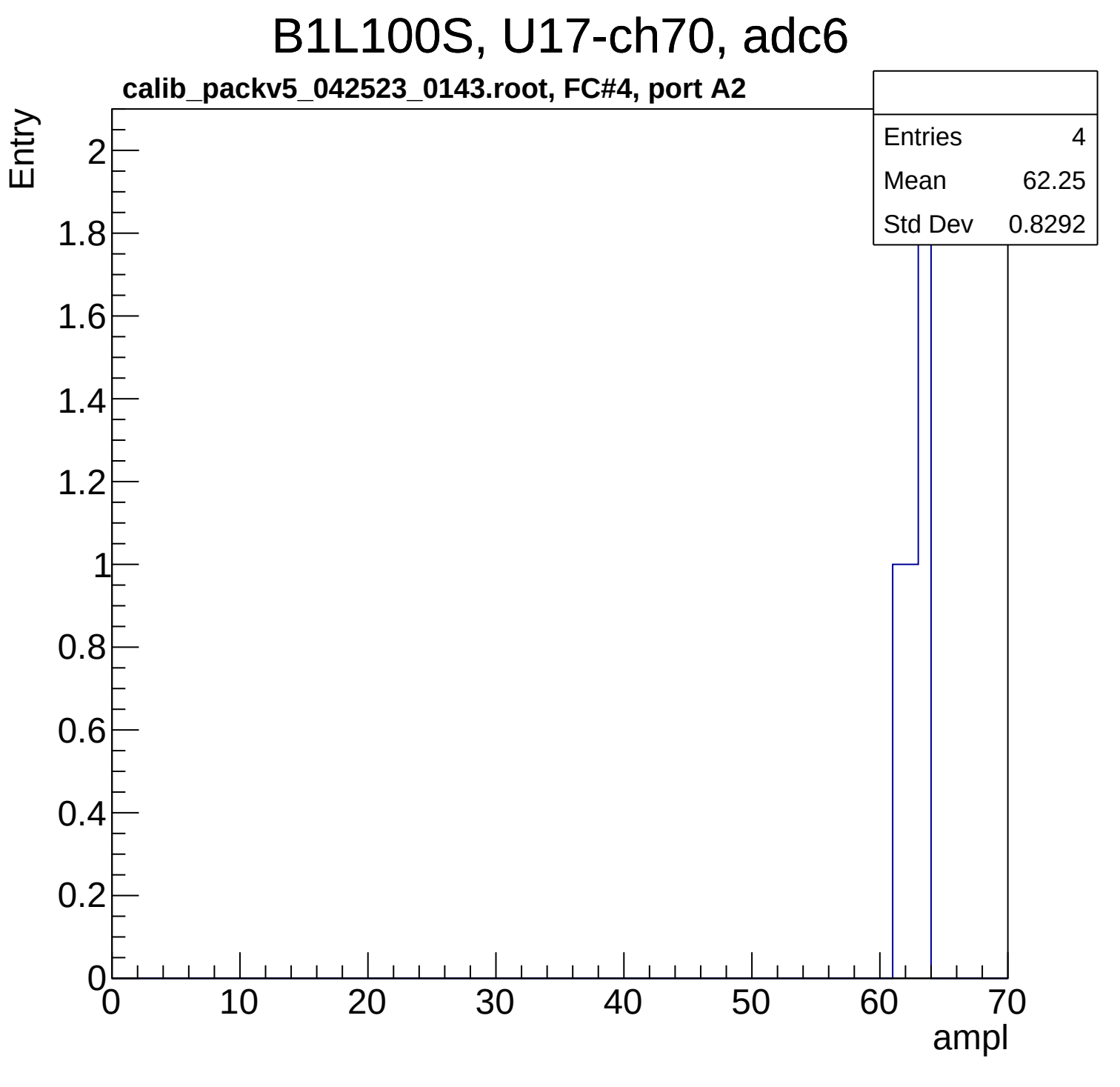
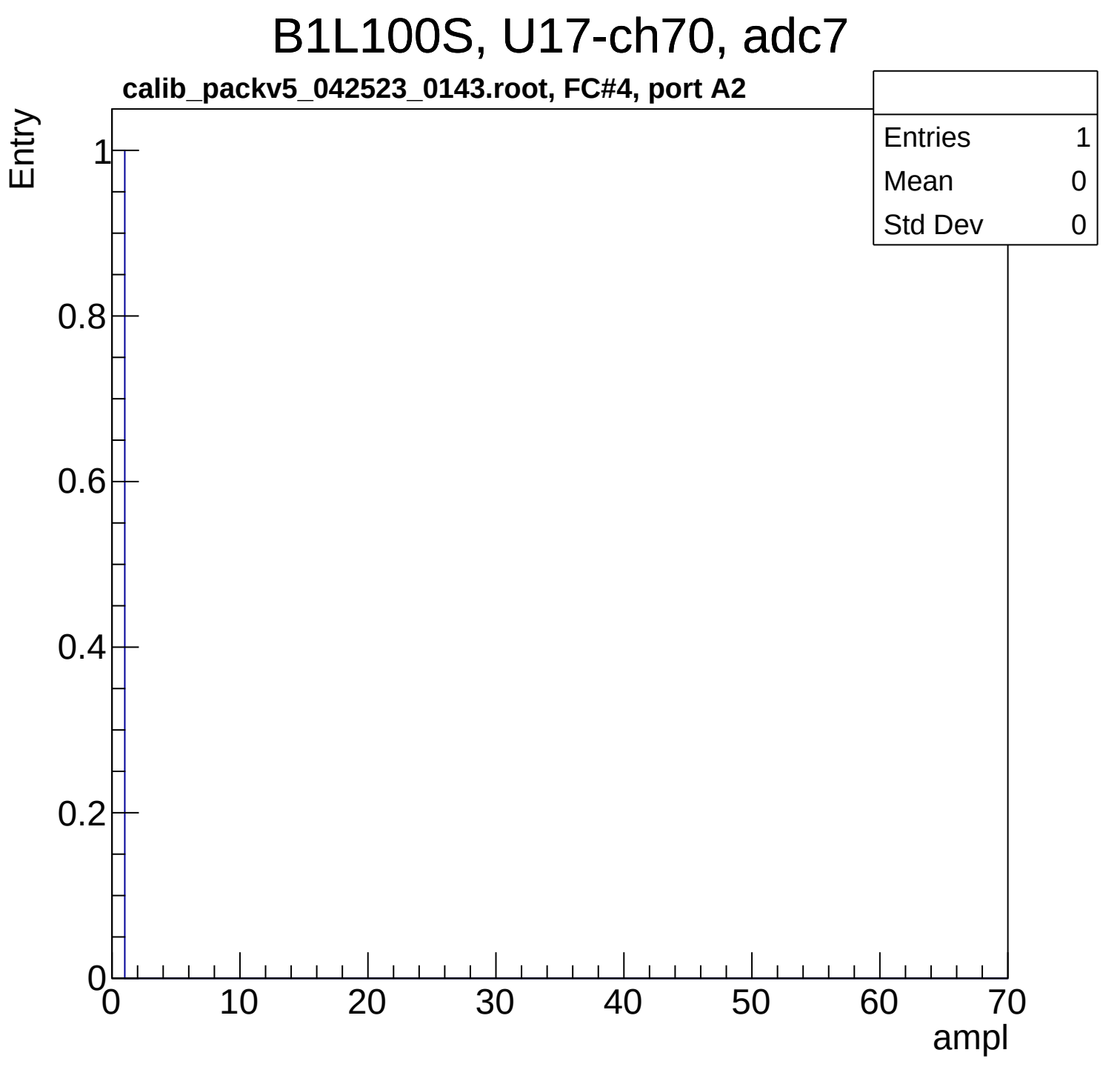
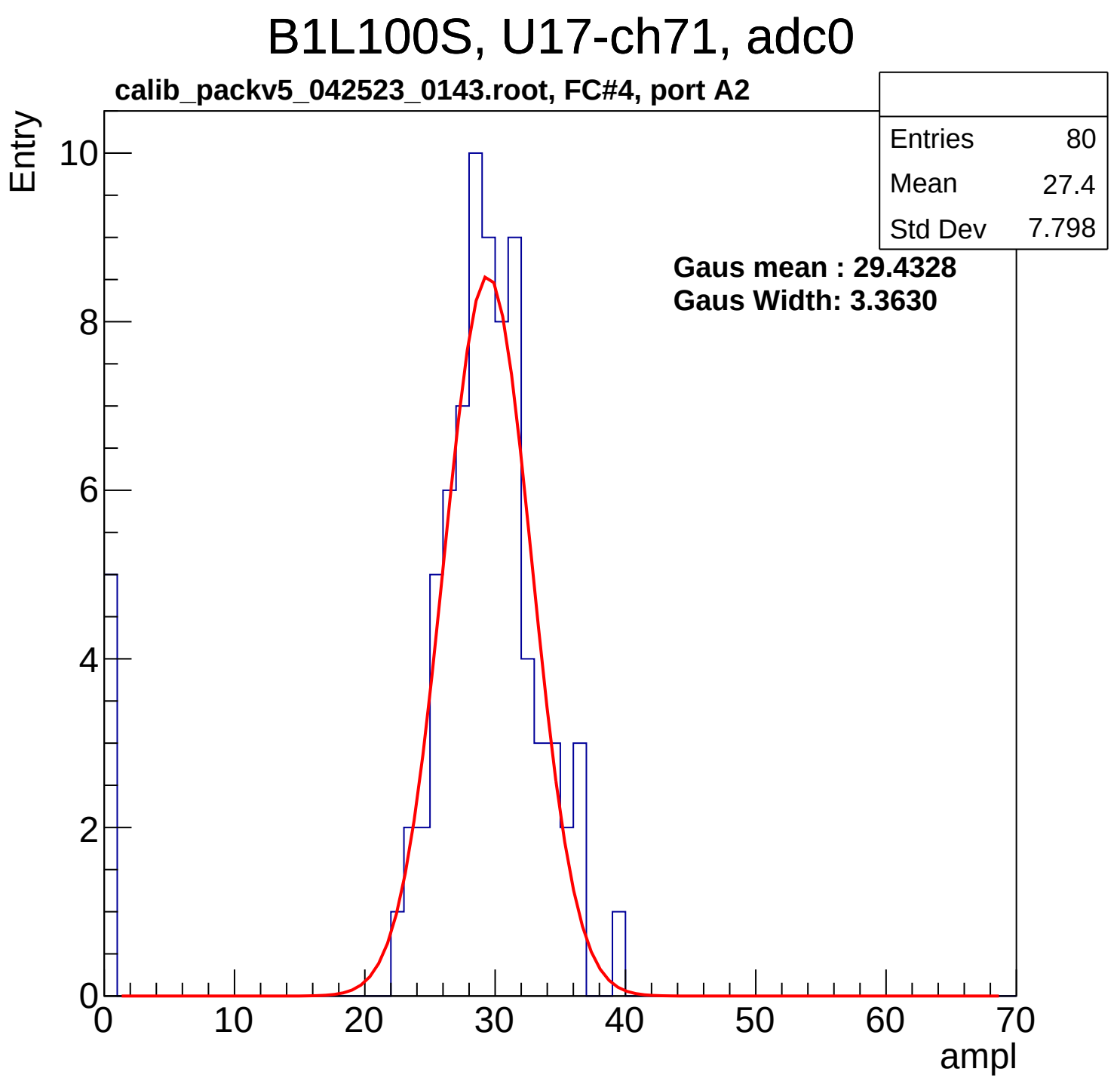
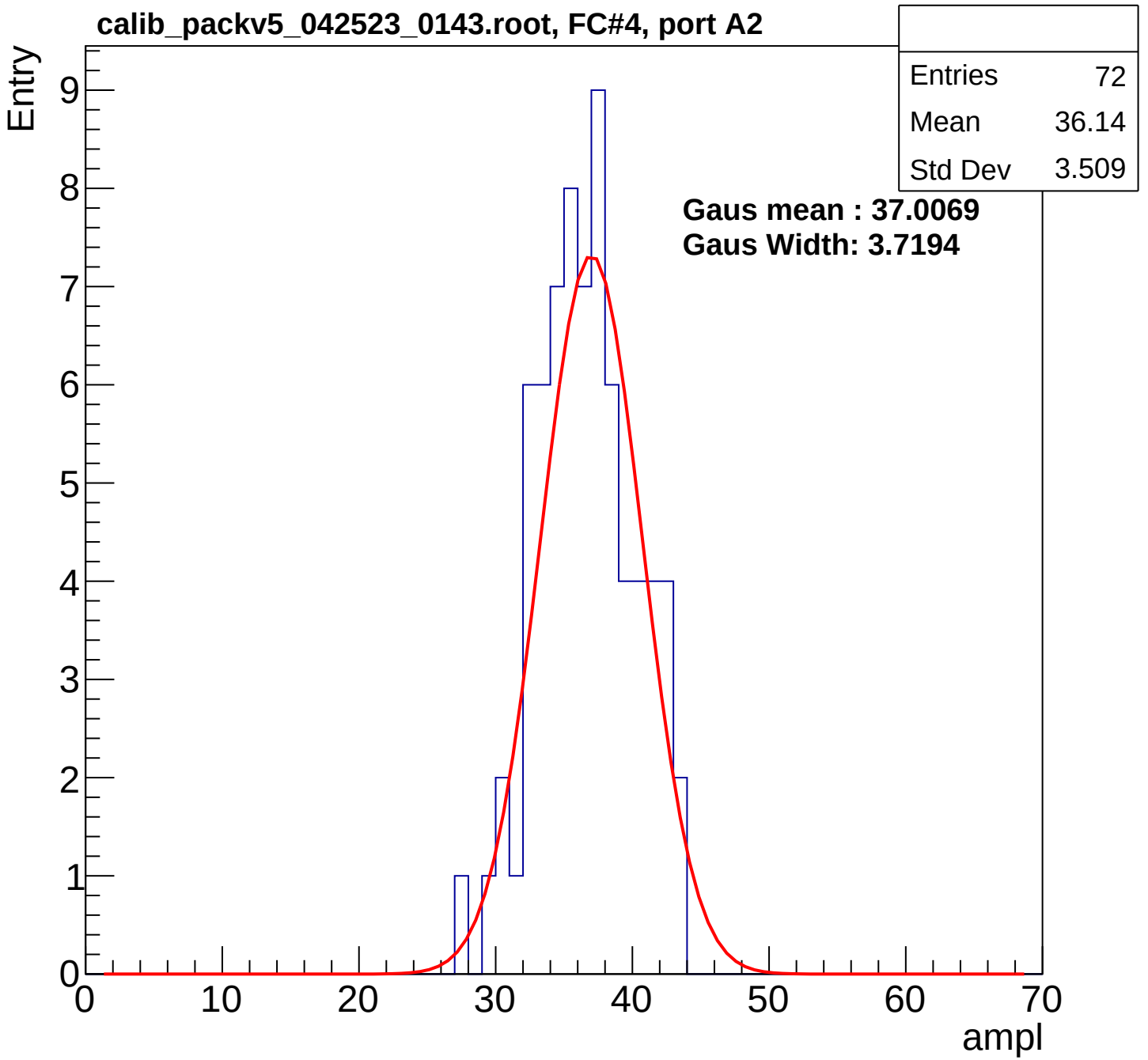
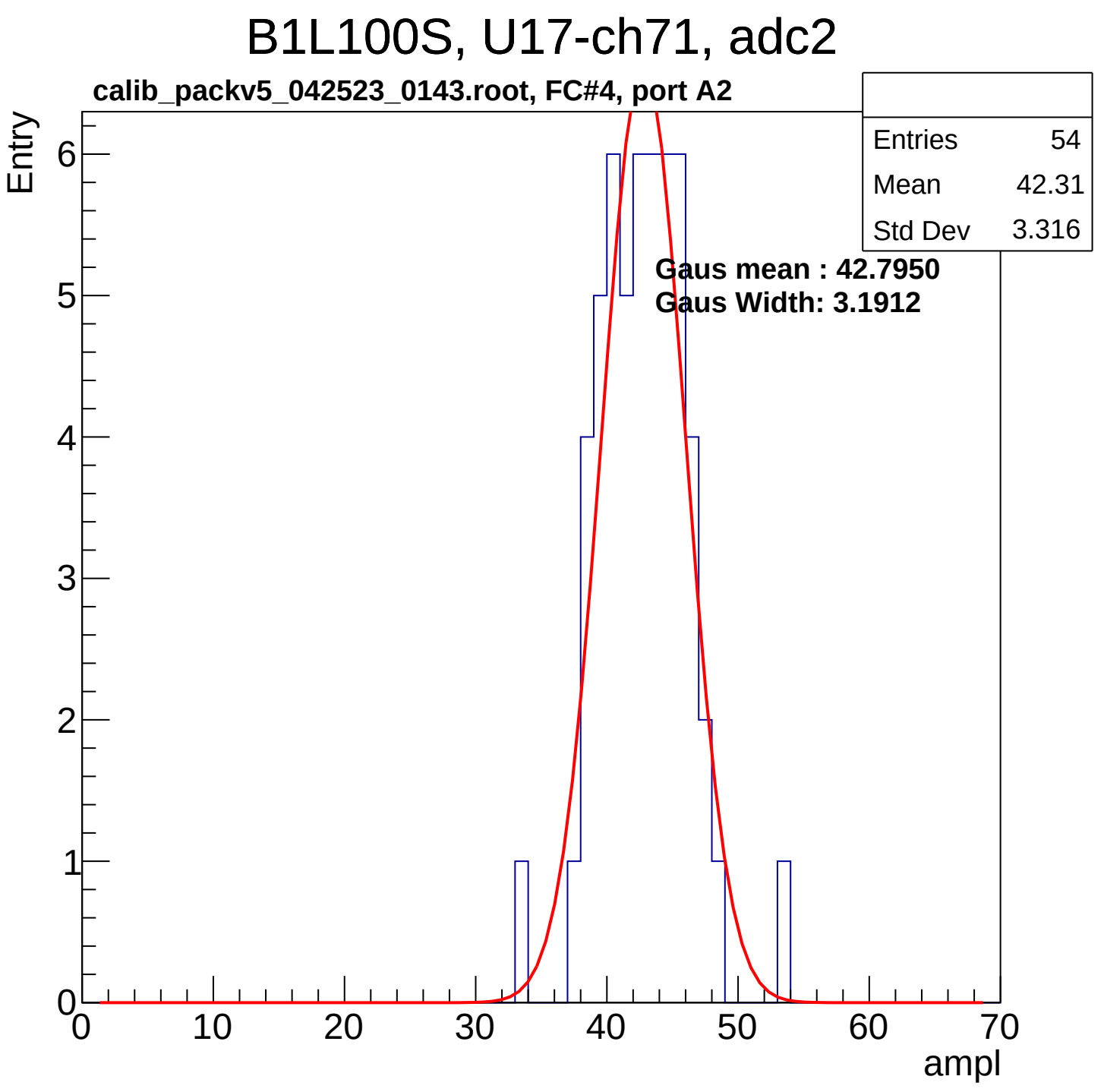
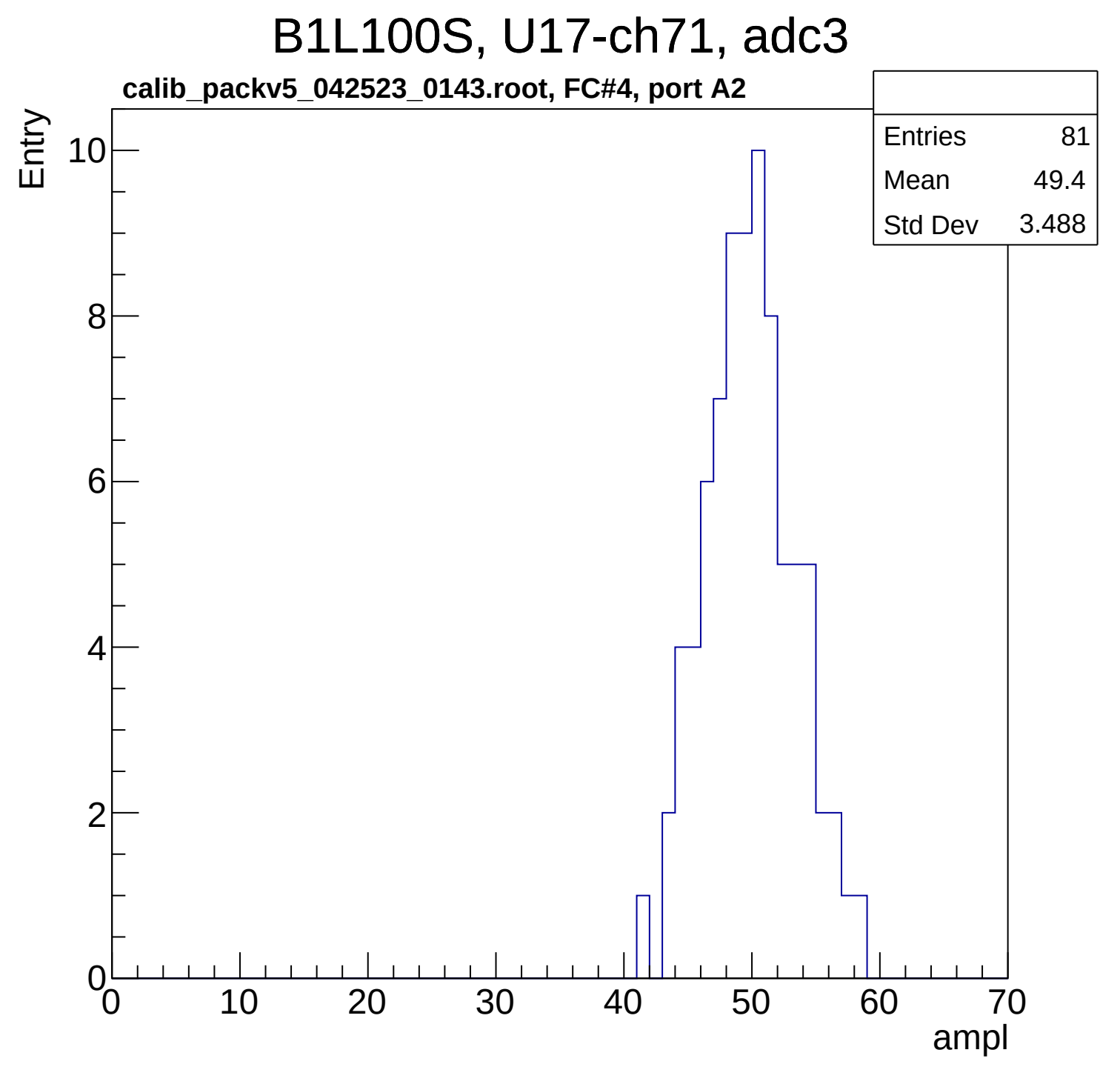

B1L100S, U17-ch70, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 4
Mean 62.25
Std Dev 0.8292
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

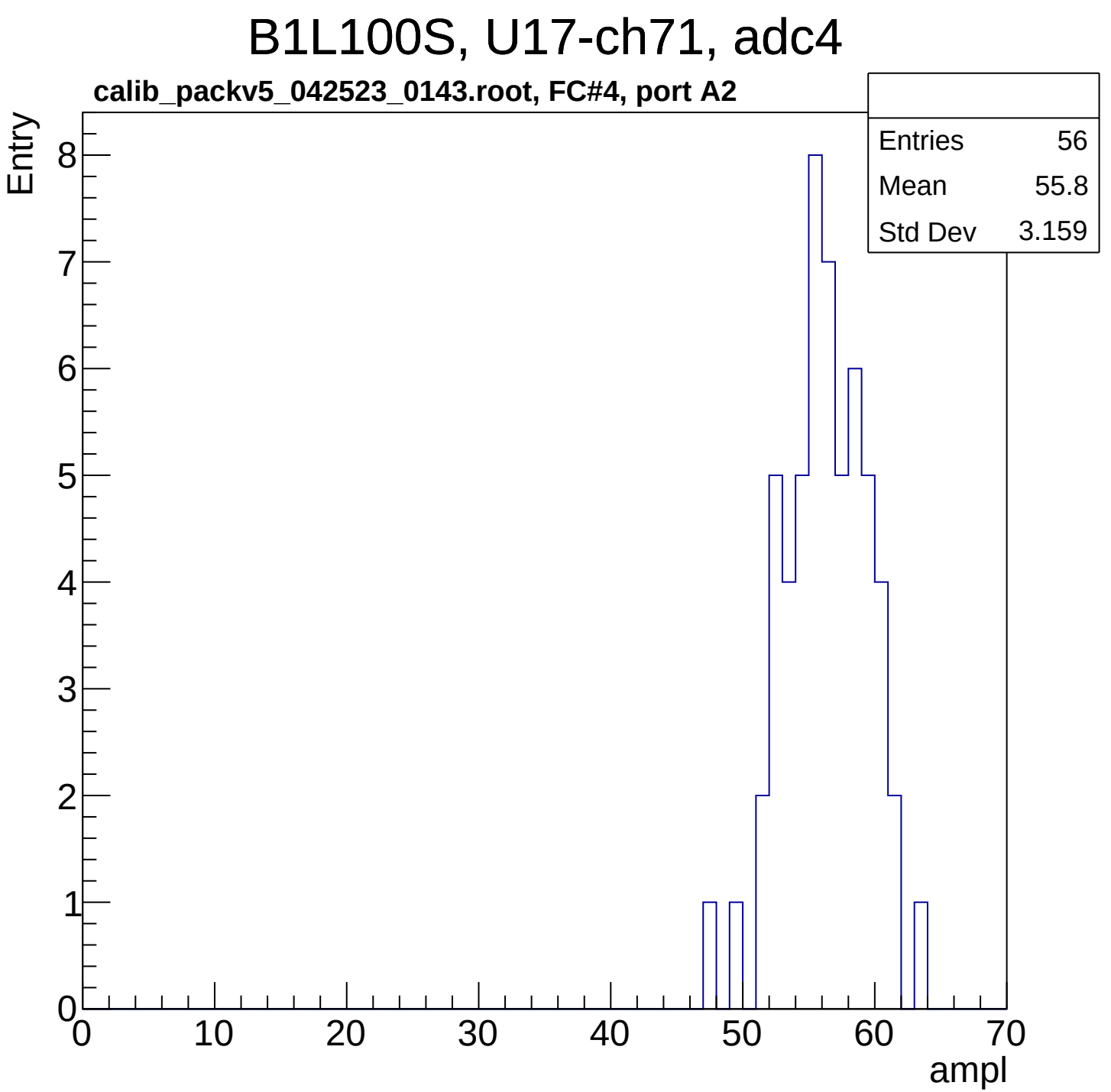

B1L100S, U17-ch70, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

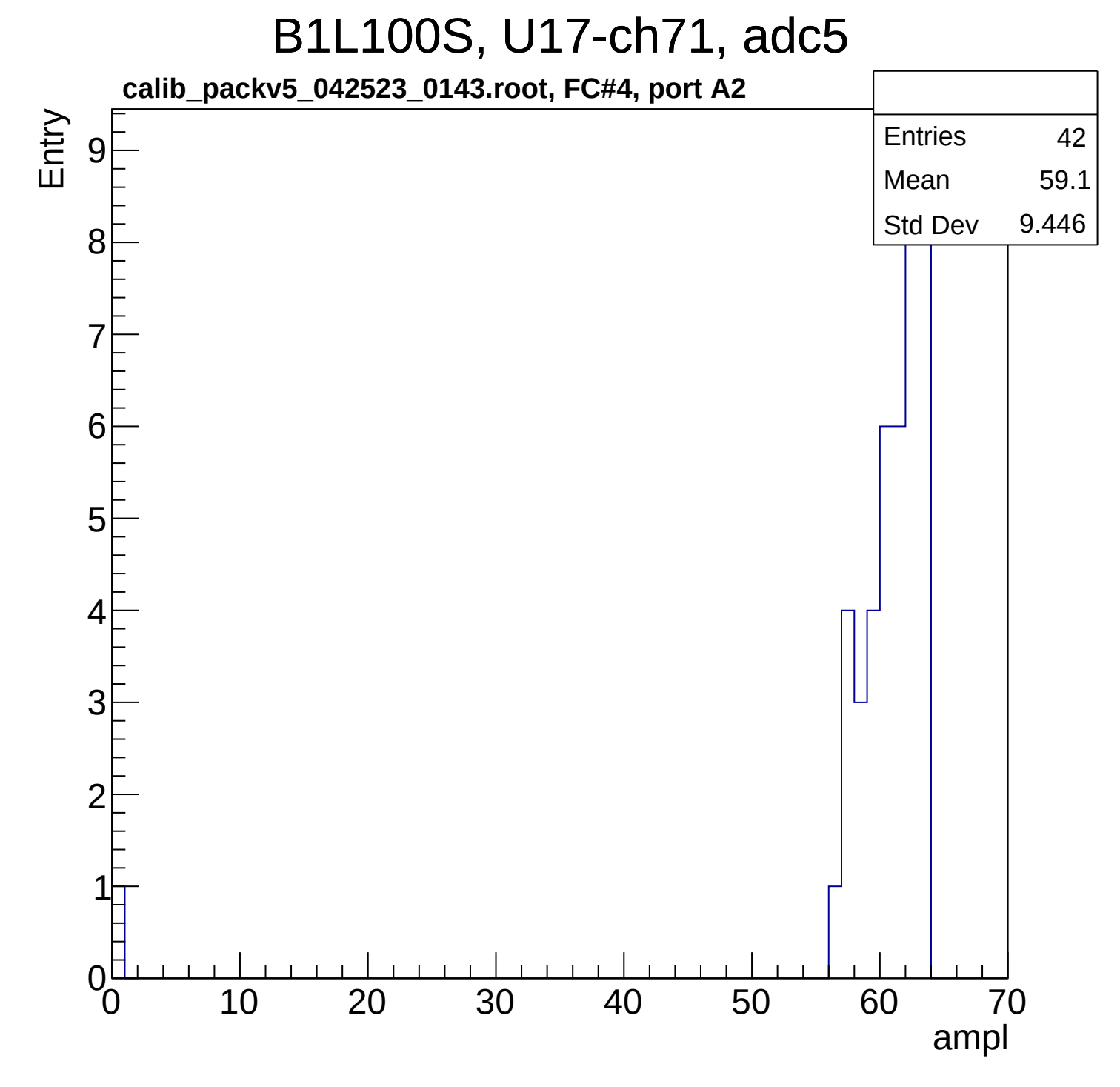

B1L100S, U17-ch71, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 80
Mean 27.4
Std Dev 7.798
Gaus mean : 29.4328
Gaus Width: 3.3630
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

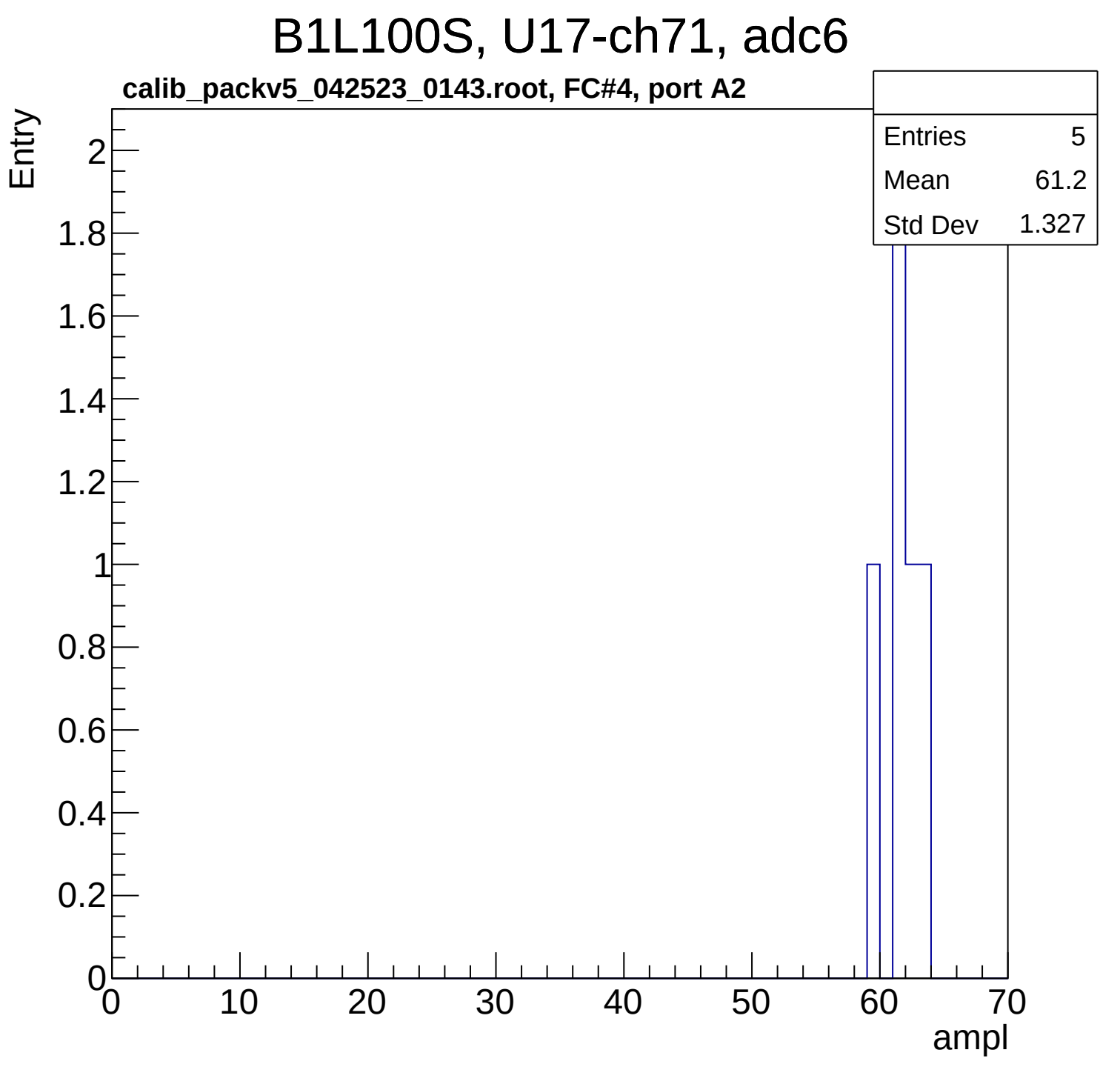

B1L100S, U17-ch71, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 36.14
Std Dev 3.509
Gaus mean : 37.0069
Gaus Width: 3.7194
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch71, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 42.31
Std Dev 3.316
Gaus mean : 42.7950
Gaus Width: 3.1912
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L100S, U17-ch71, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 81
Mean 49.4
Std Dev 3.488
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U17-ch71, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 55.8
Std Dev 3.159
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch71, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 42
Mean 59.1
Std Dev 9.446
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch71, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 5
Mean 61.2
Std Dev 1.327
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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20
30
40
50
60
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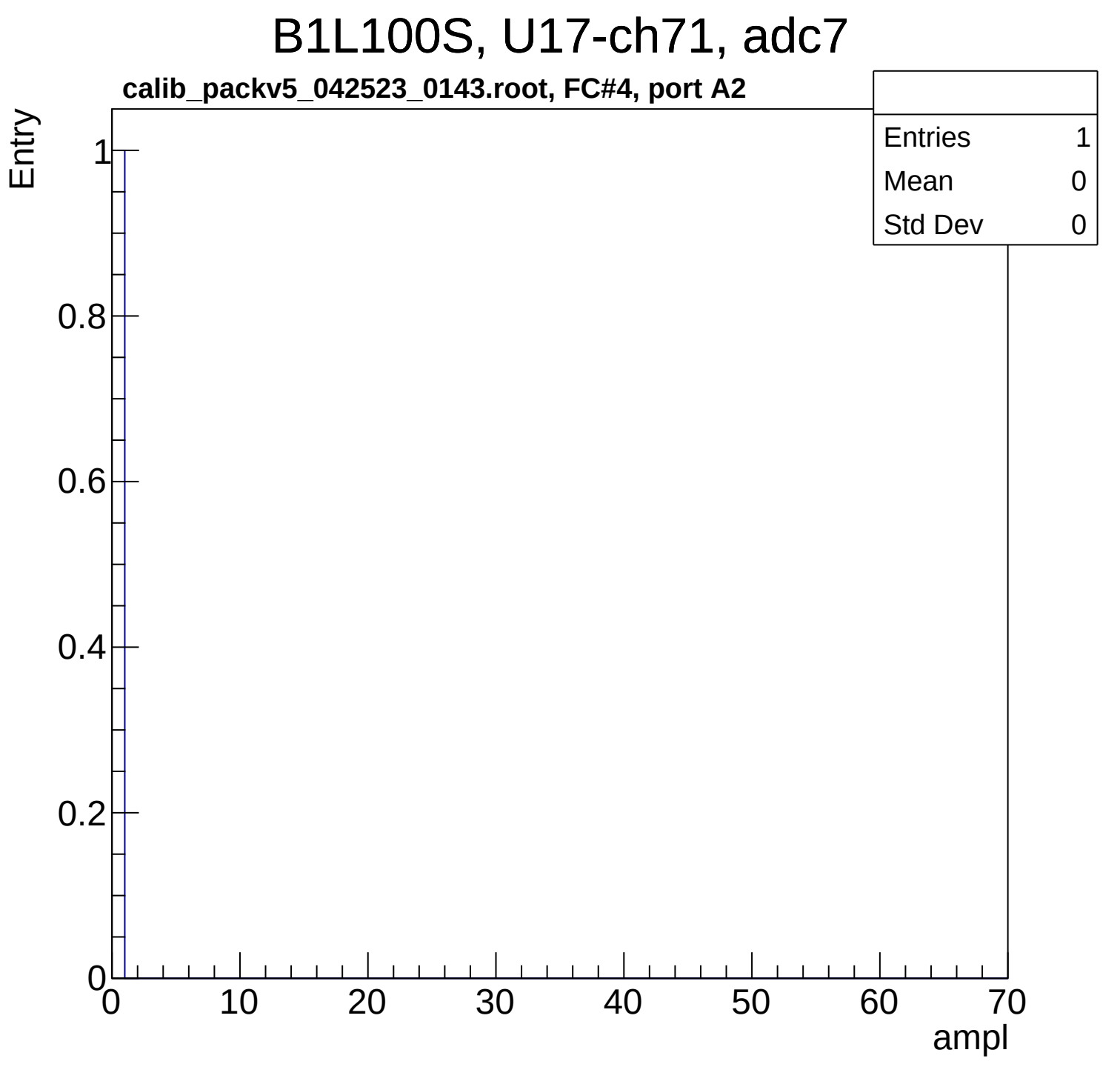
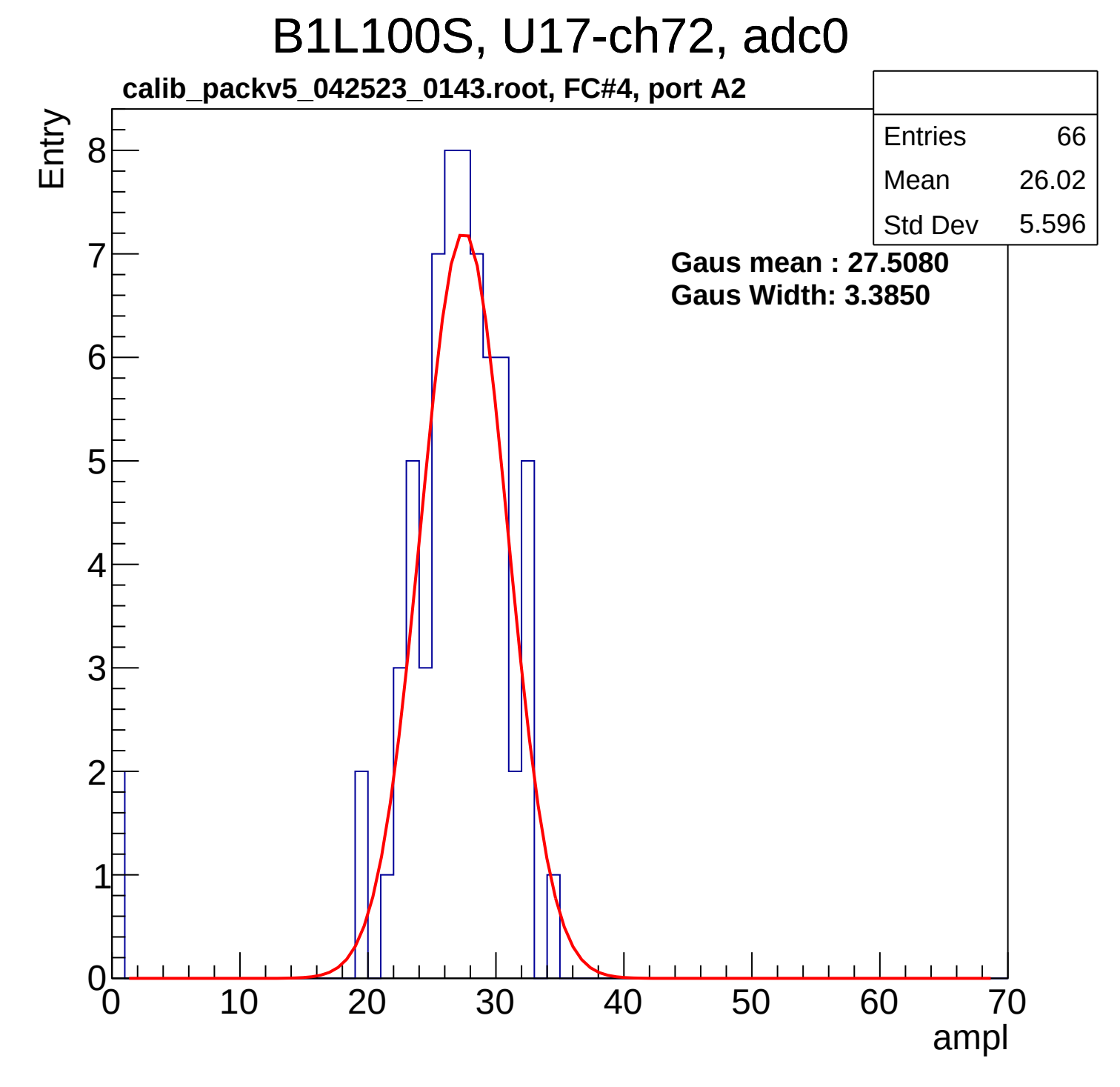
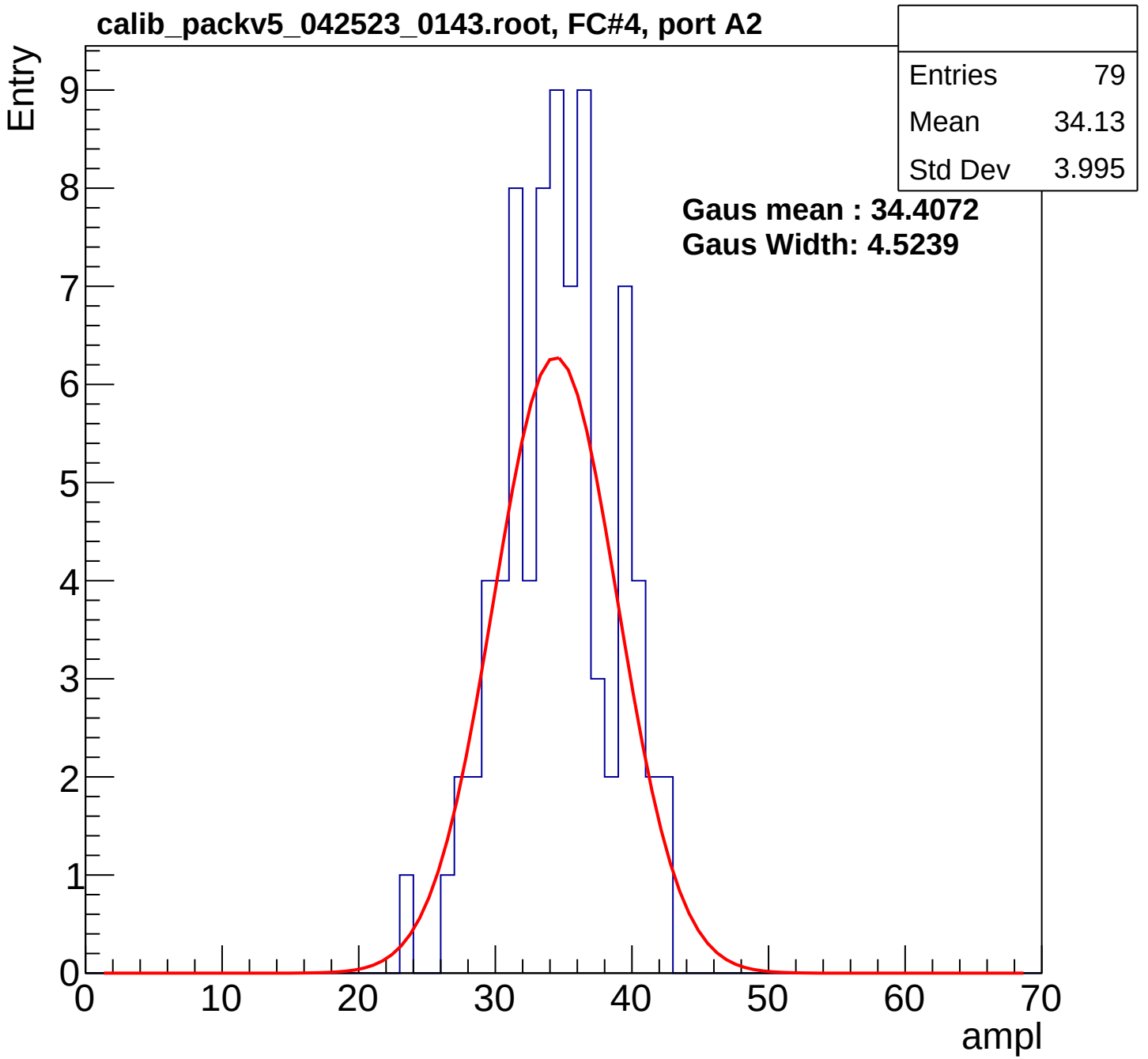
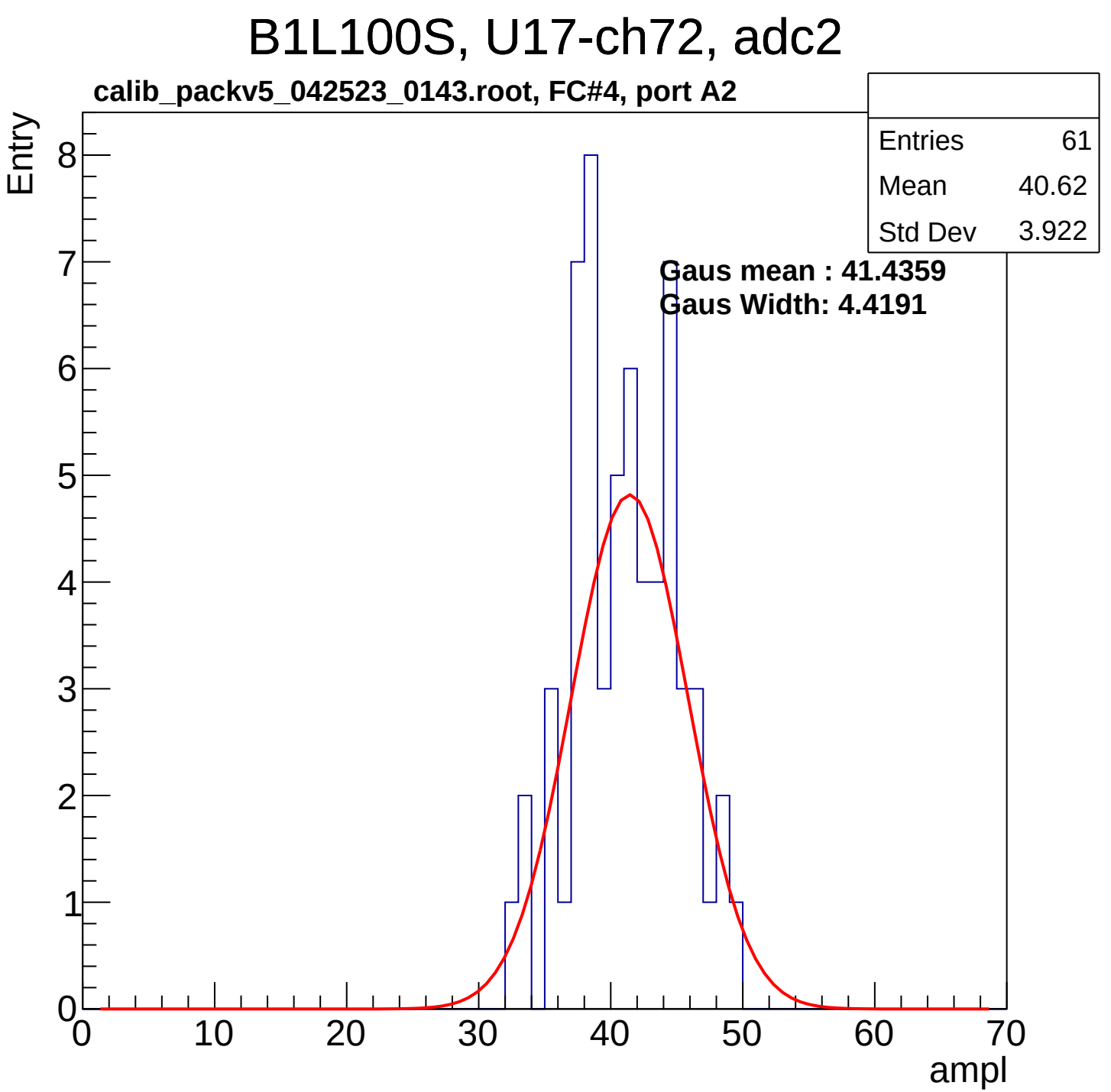

B1L100S, U17-ch71, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch72, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 26.02
Std Dev 5.596
Gaus mean : 27.5080
Gaus Width: 3.3850
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch72, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 79
Mean 34.13
Std Dev 3.995
Gaus mean : 34.4072
Gaus Width: 4.5239
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch72, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 40.62
Std Dev 3.922
Gaus mean : 41.4359
Gaus Width: 4.4191
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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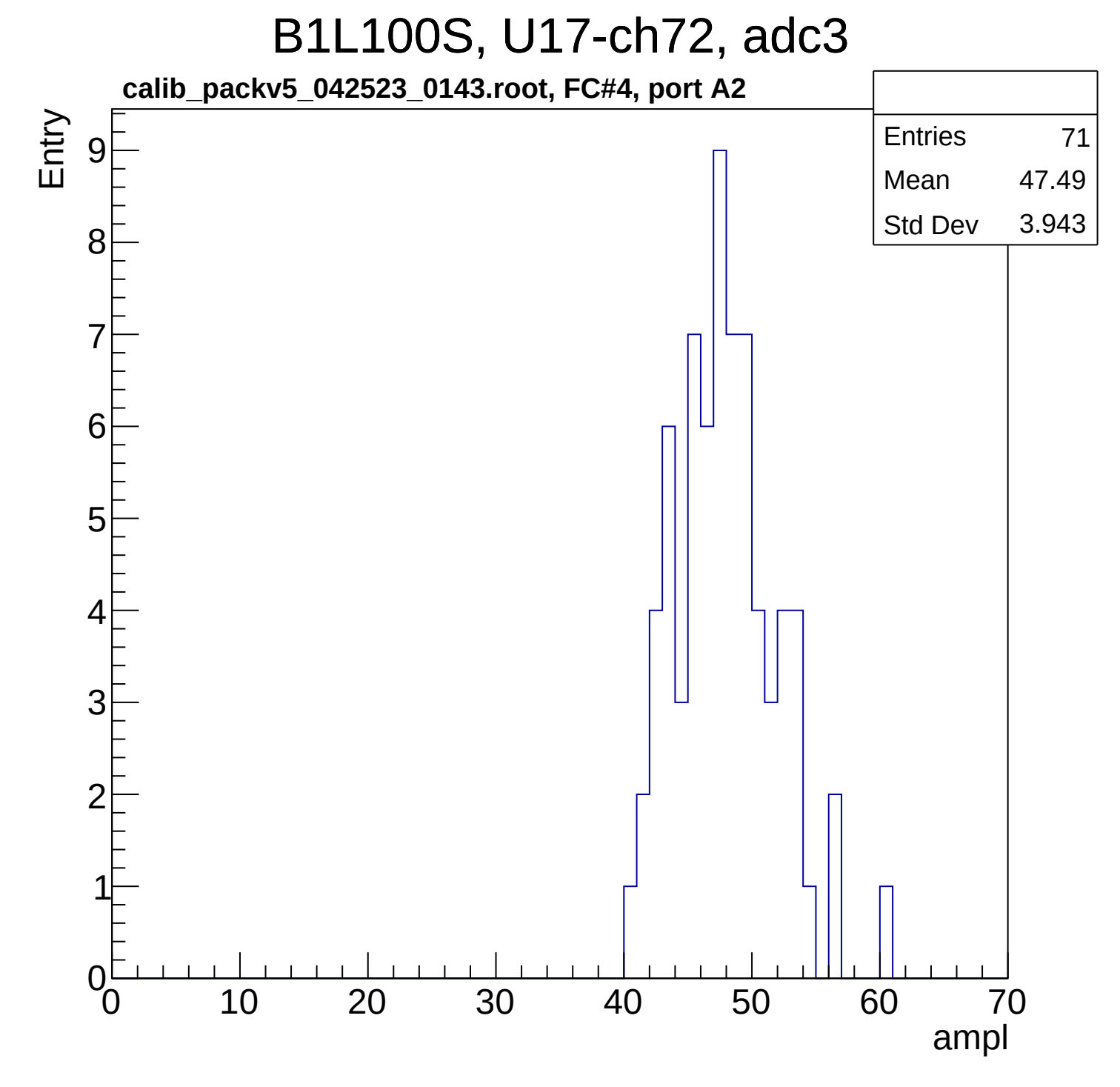
B1L100S, U17-ch72, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 47.49
Std Dev 3.943
Entry
ampl
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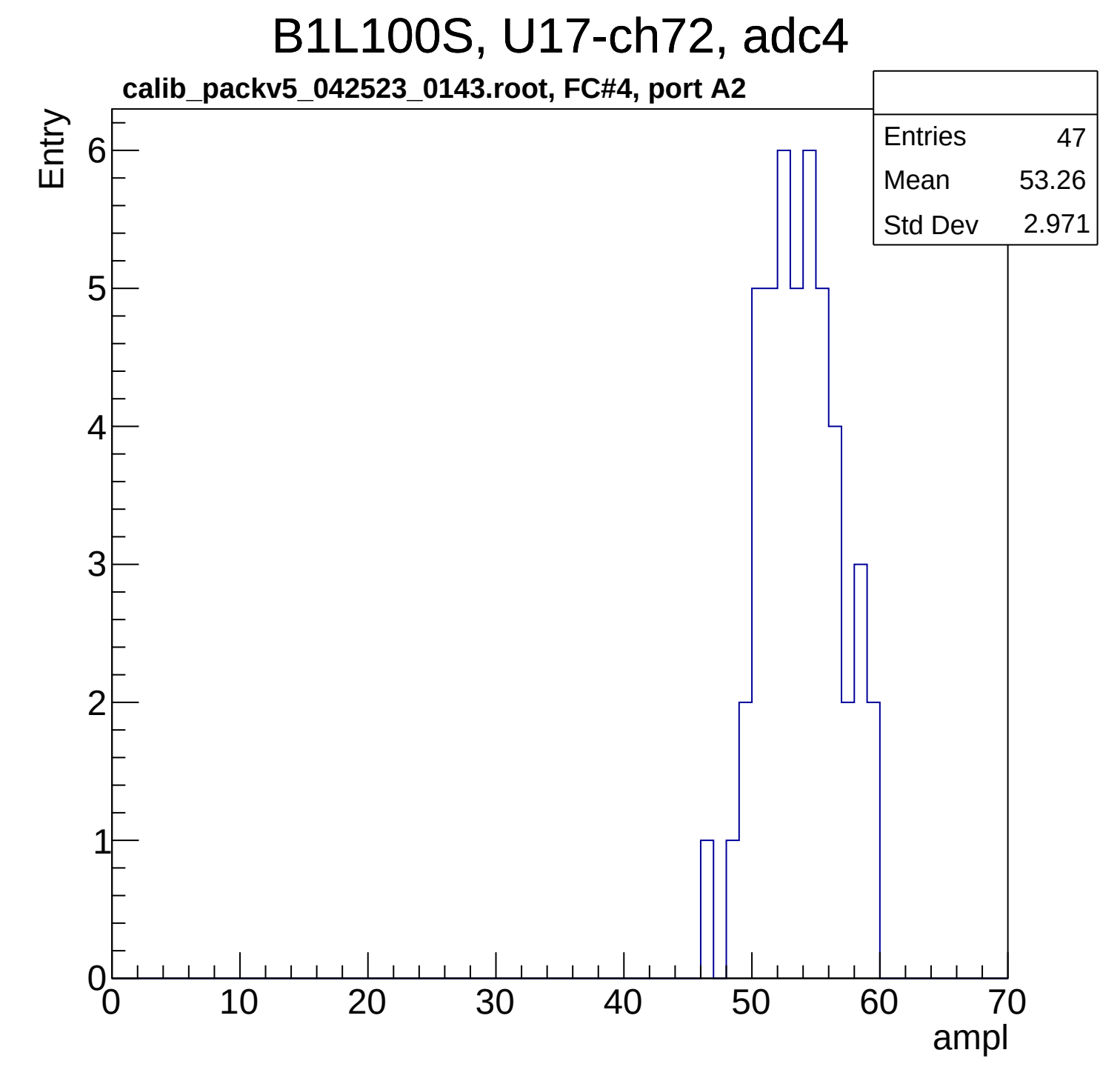
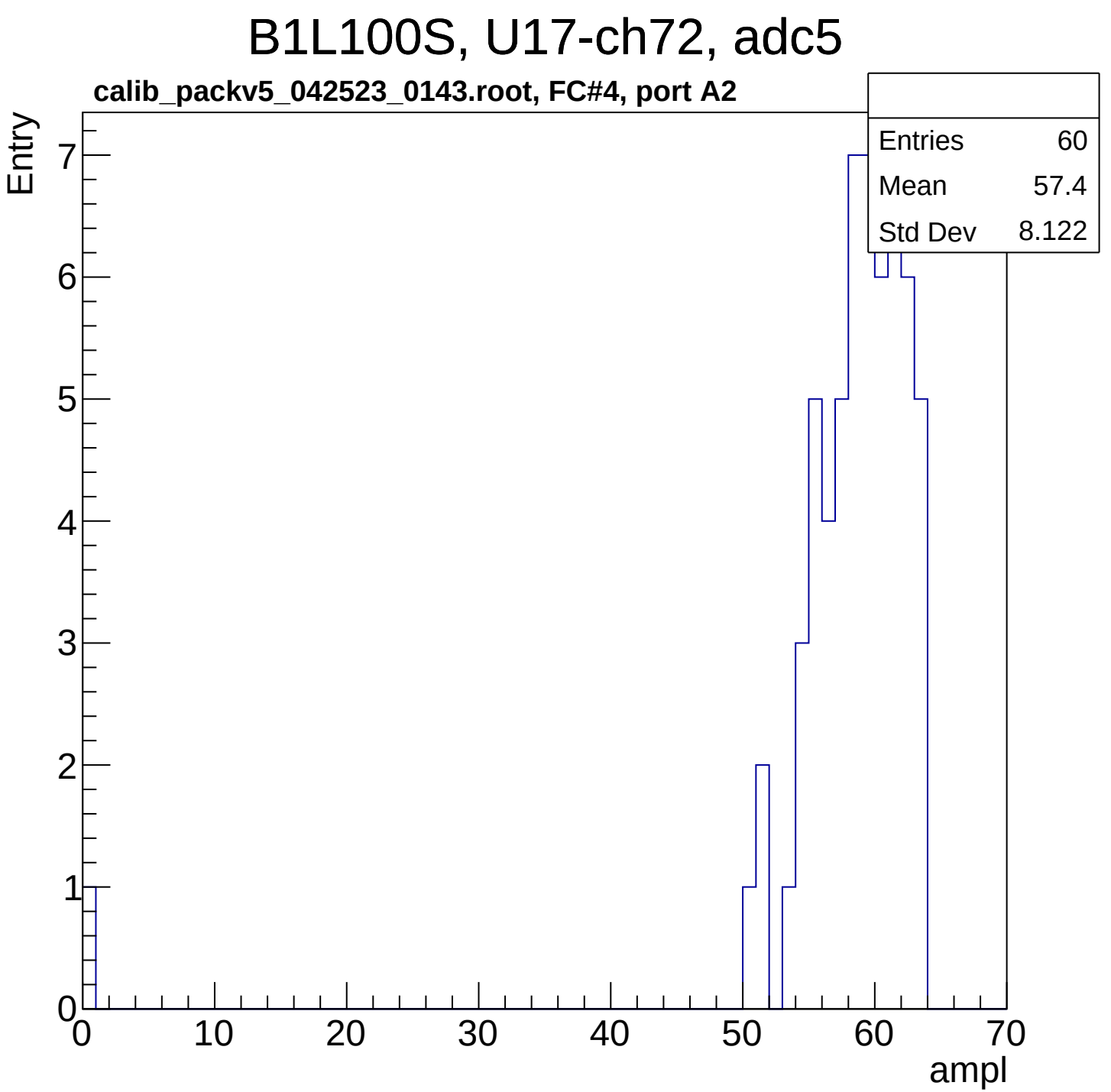
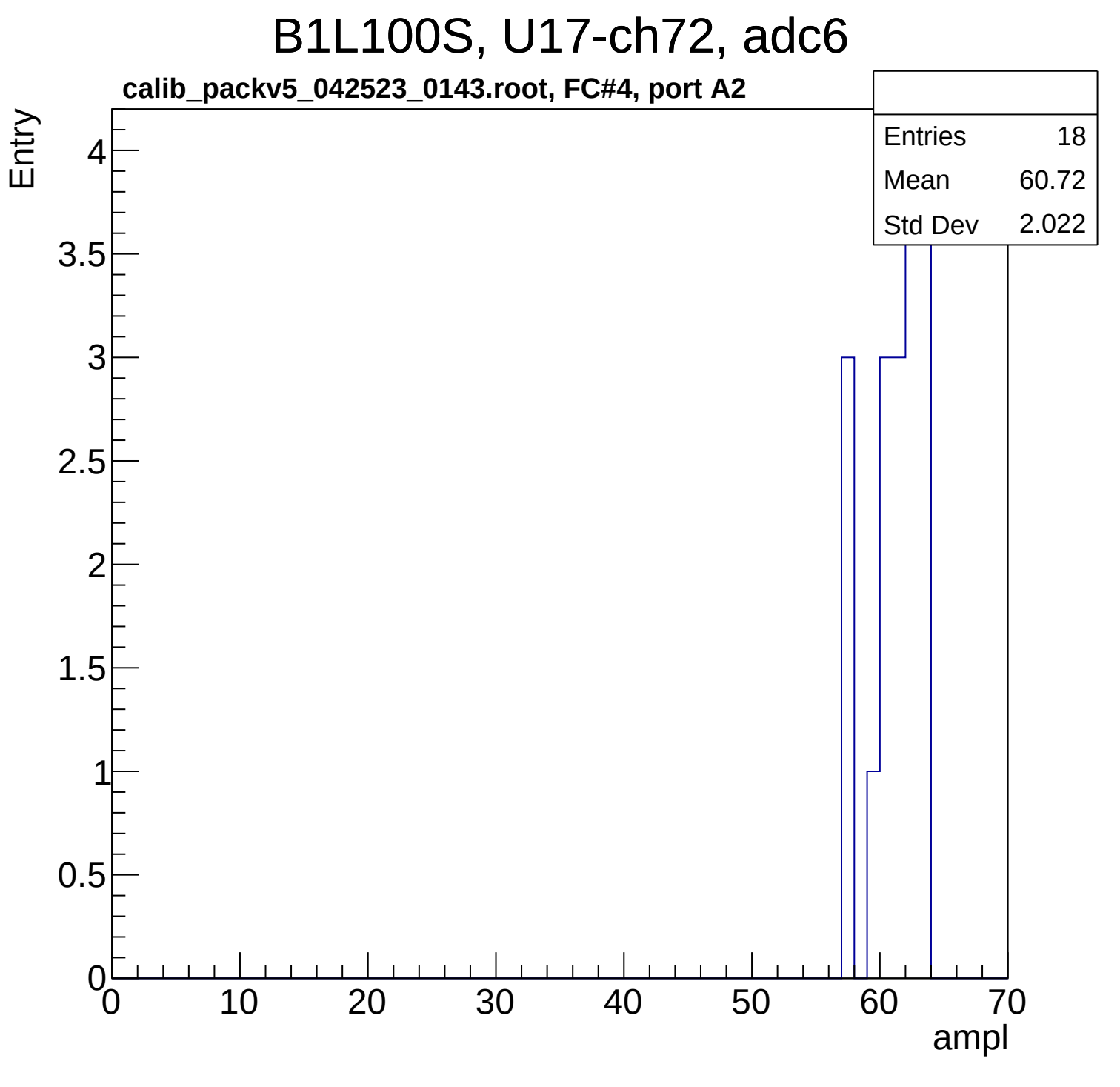
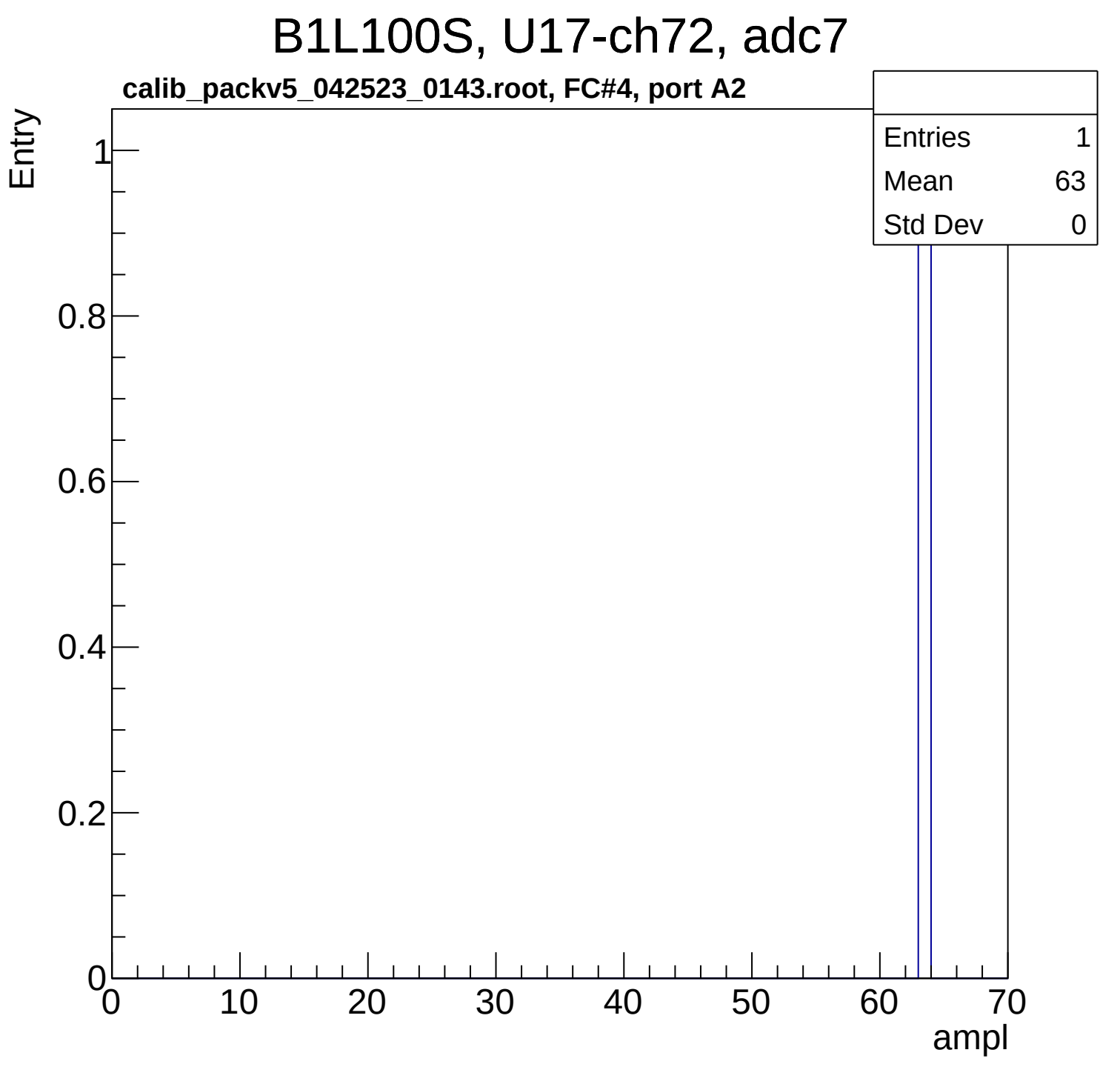
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch72, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 47
Mean 53.26
Std Dev 2.971
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L100S, U17-ch72, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 57.4
Std Dev 8.122
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U17-ch72, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 18
Mean 60.72
Std Dev 2.022
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L100S, U17-ch72, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 63
Std Dev 0
Entry
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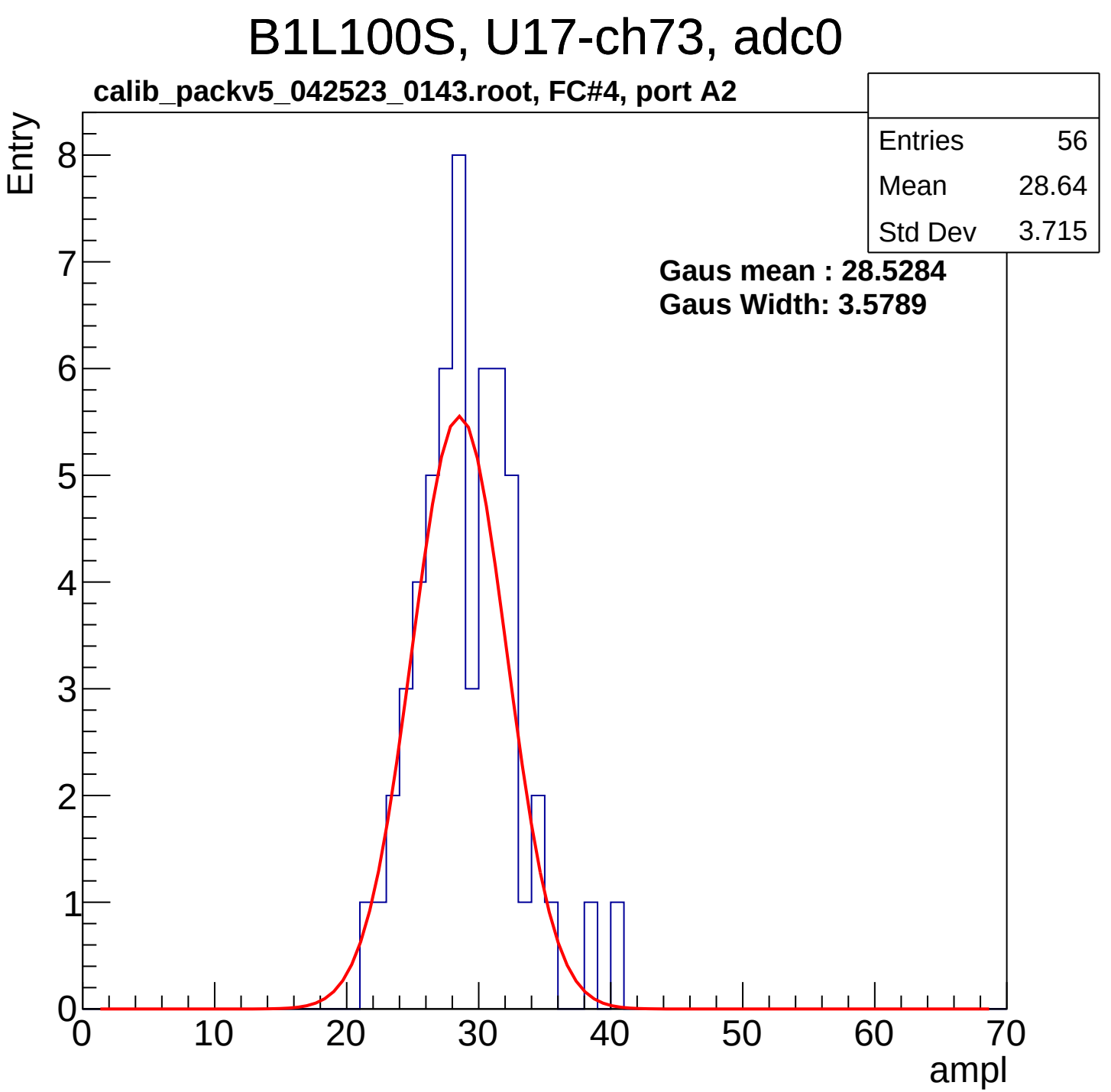
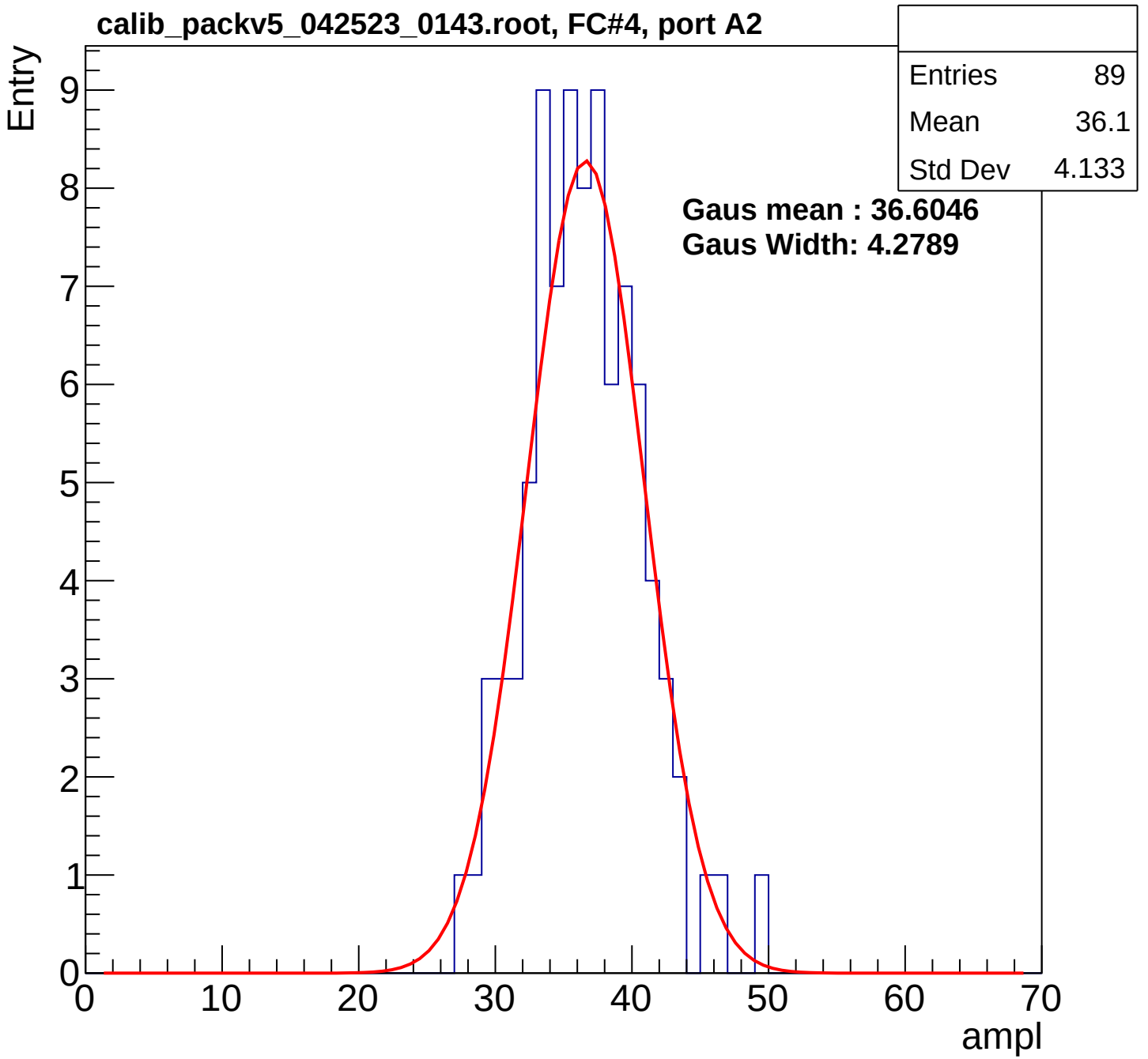
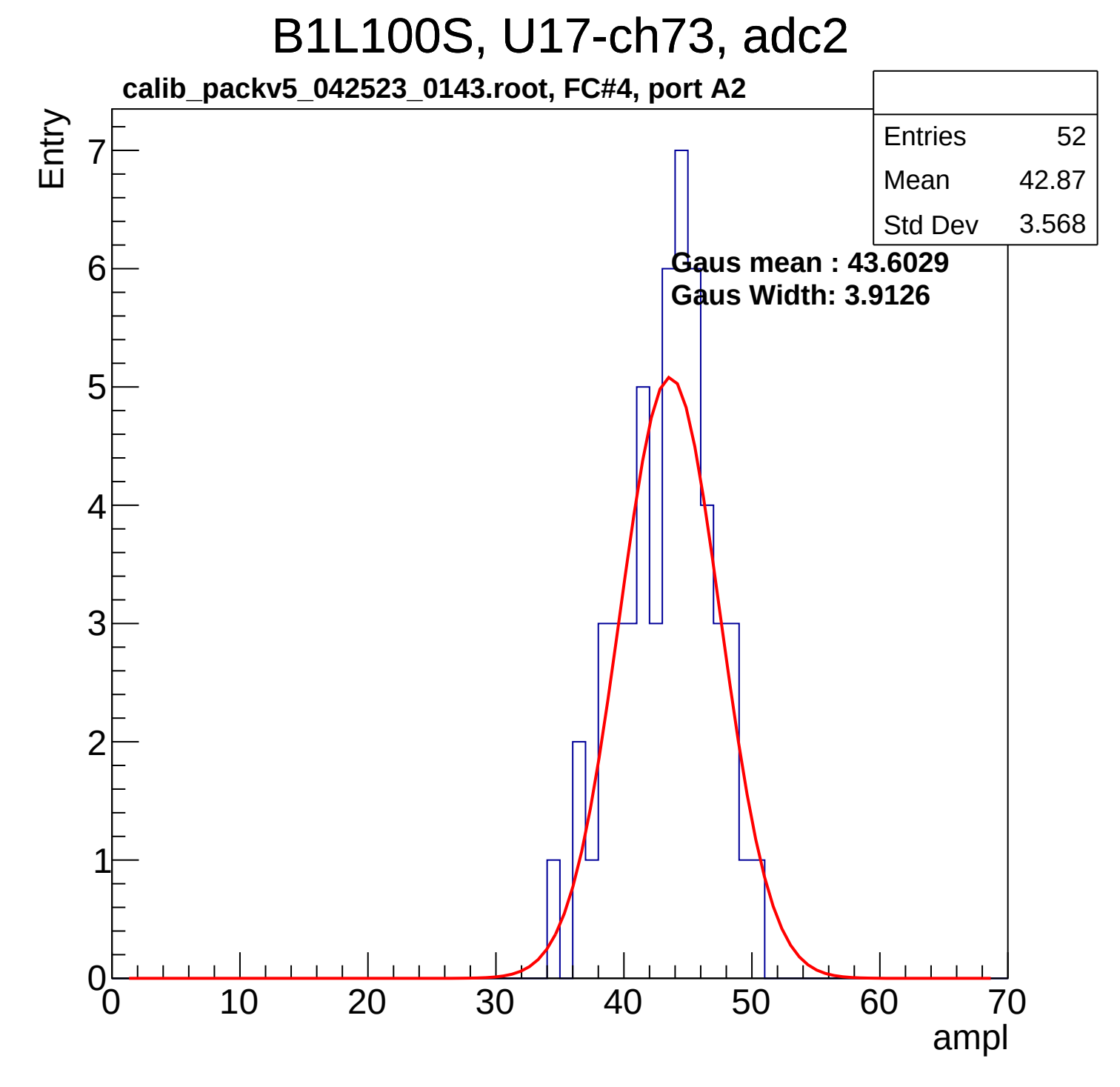
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch73, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 28.64
Std Dev 3.715
Gaus mean : 28.5284
Gaus Width: 3.5789
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch73, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 89
Mean 36.1
Std Dev 4.133
Gaus mean : 36.6046
Gaus Width: 4.2789
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch73, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 52
Mean 42.87
Std Dev 3.568
Gaus mean : 43.6029
Gaus Width: 3.9126
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
30
40
50
60
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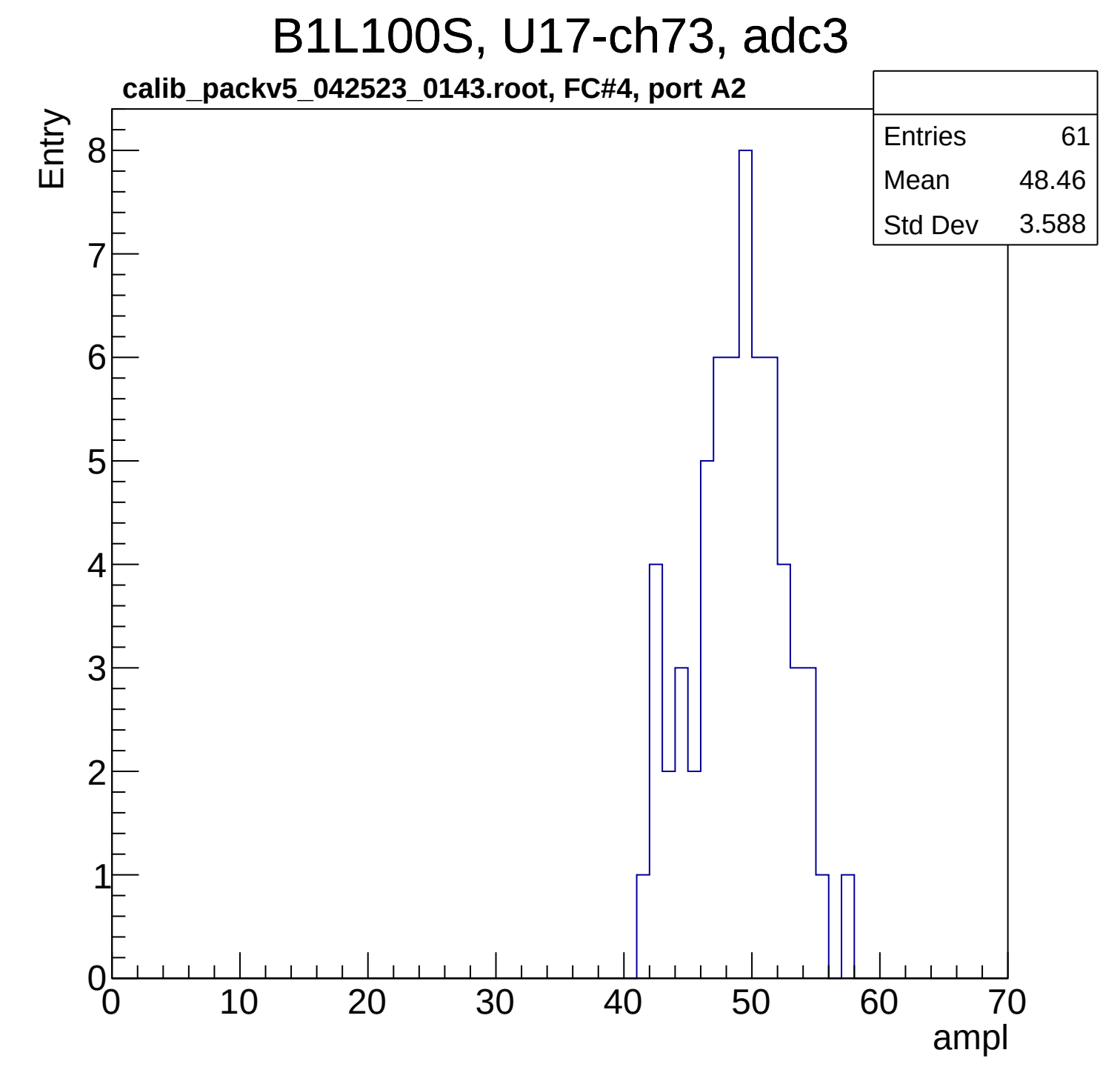
B1L100S, U17-ch73, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 48.46
Std Dev 3.588
Entry
ampl
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1
2
3
4
5
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7
8
0
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40
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60
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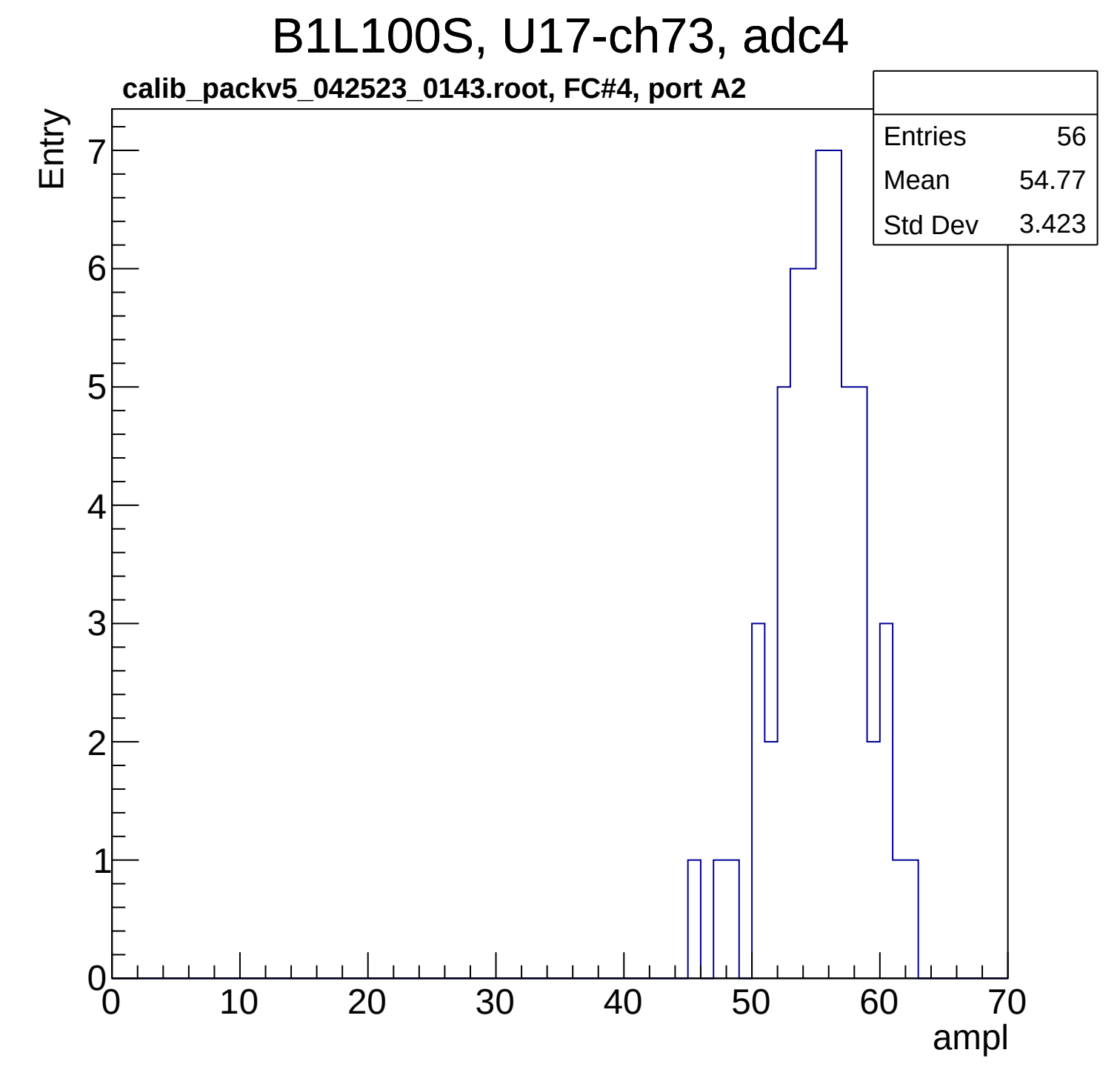
B1L100S, U17-ch73, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 54.77
Std Dev 3.423
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
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40
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60
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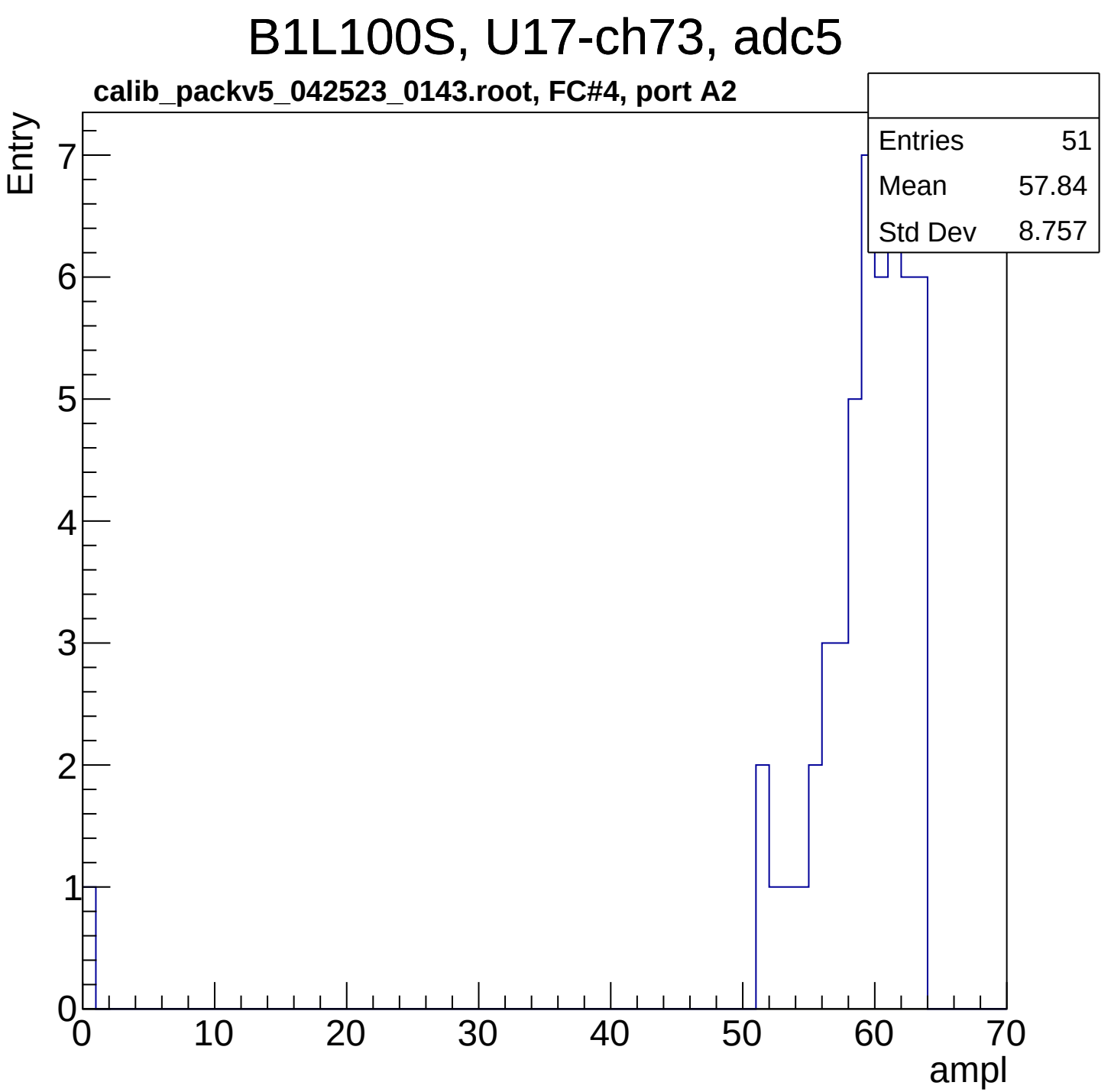
B1L100S, U17-ch73, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 57.84
Std Dev 8.757
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
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40
50
60
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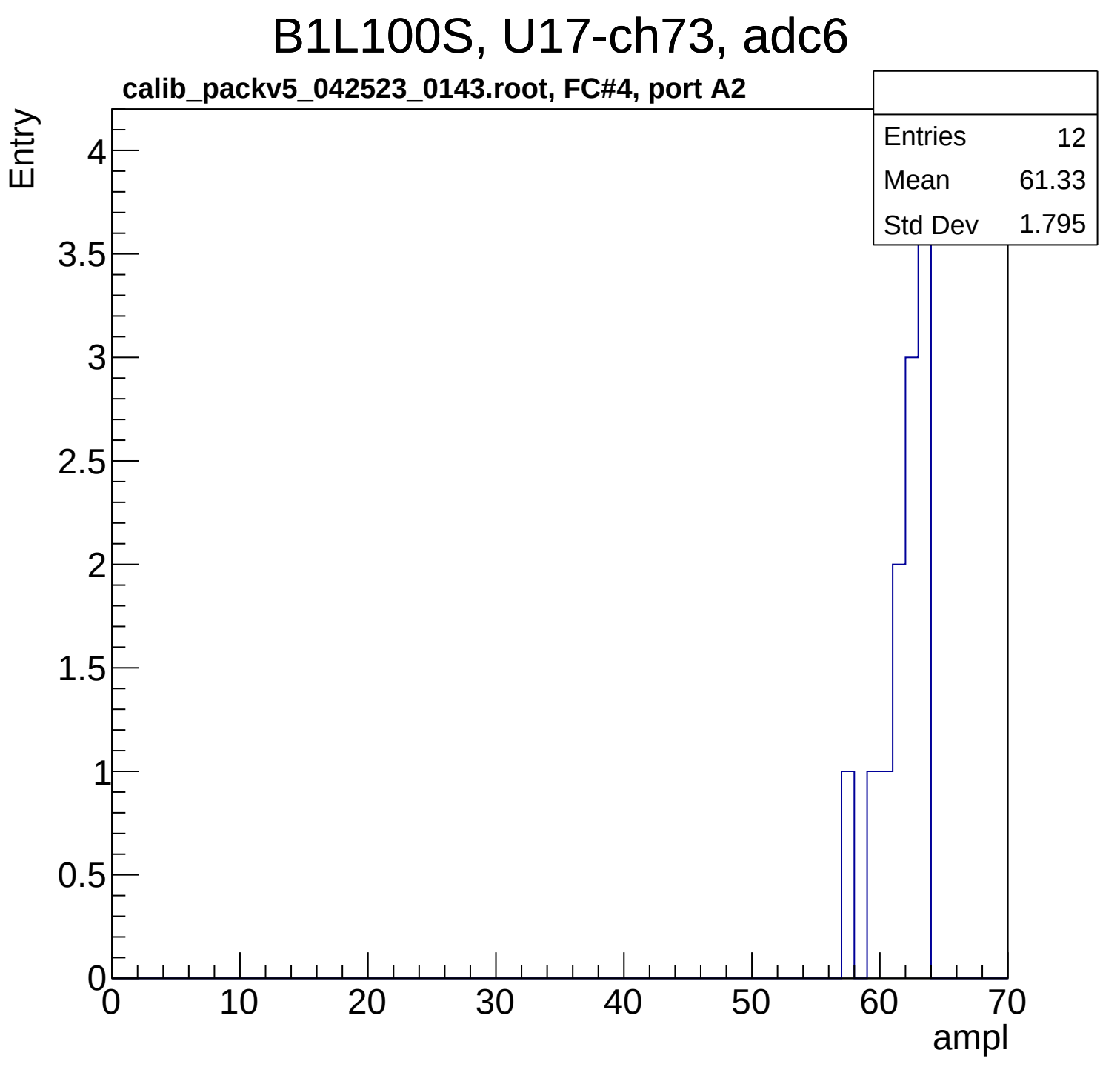
B1L100S, U17-ch73, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 12
Mean 61.33
Std Dev 1.795
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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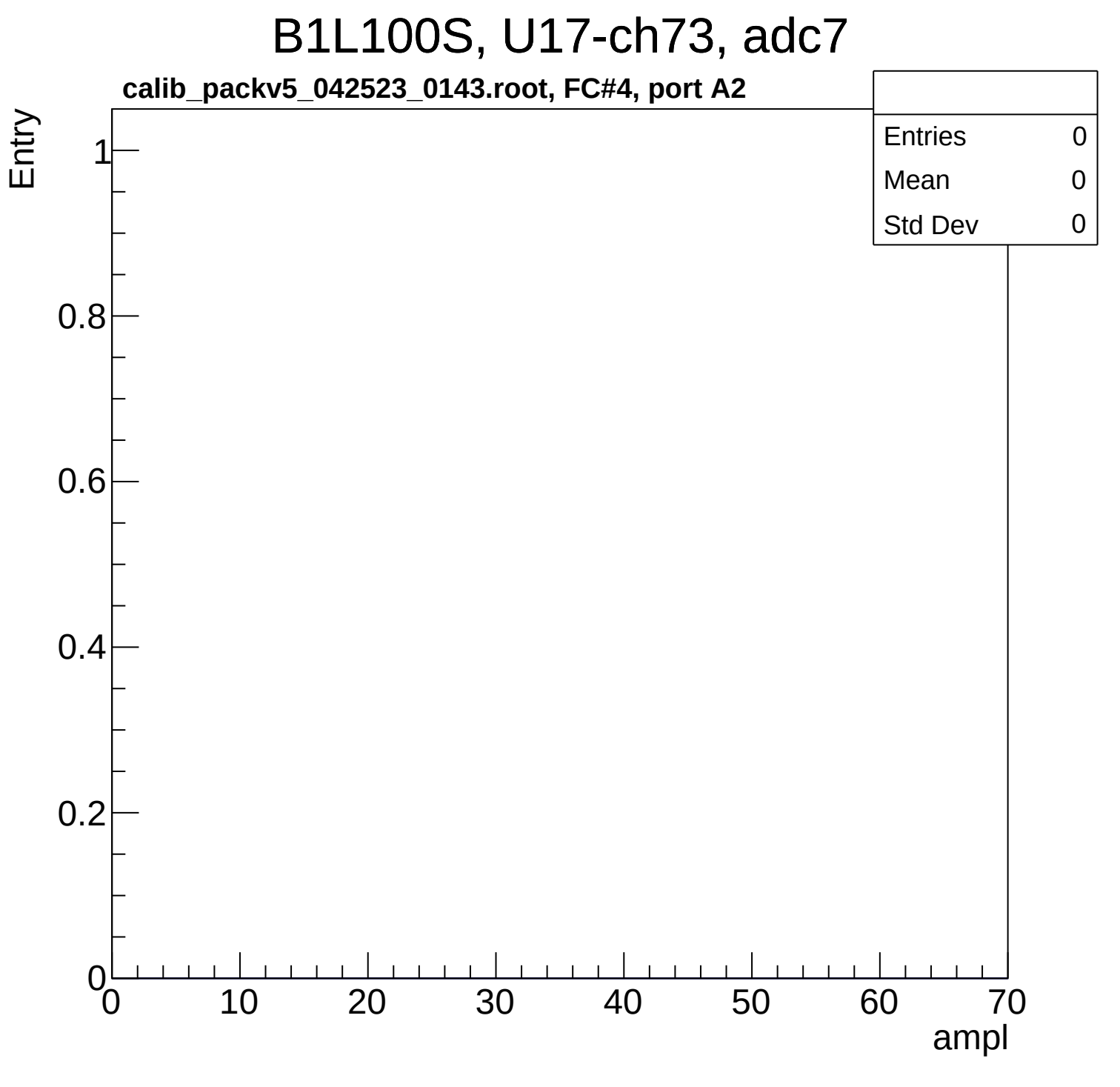
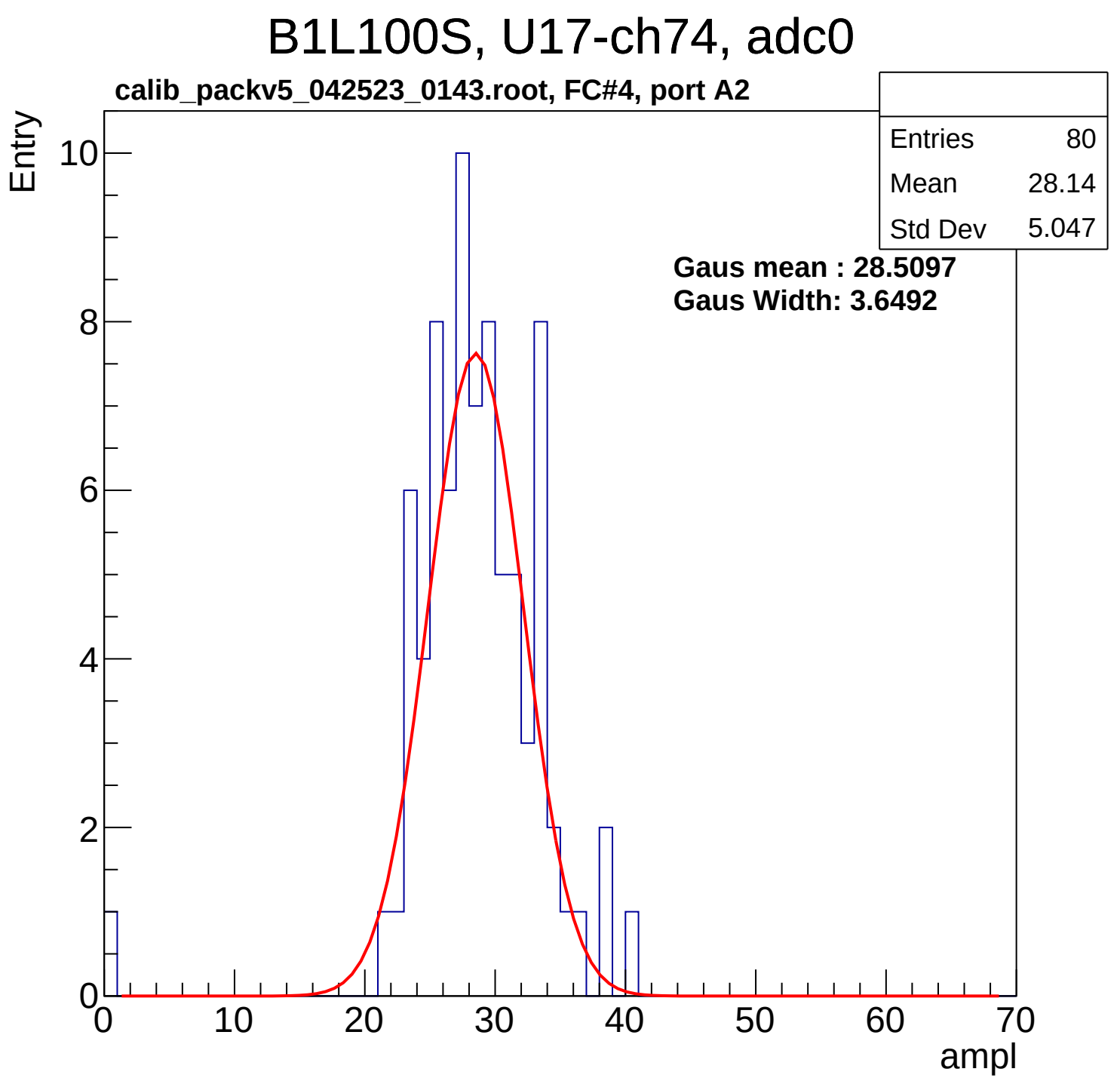
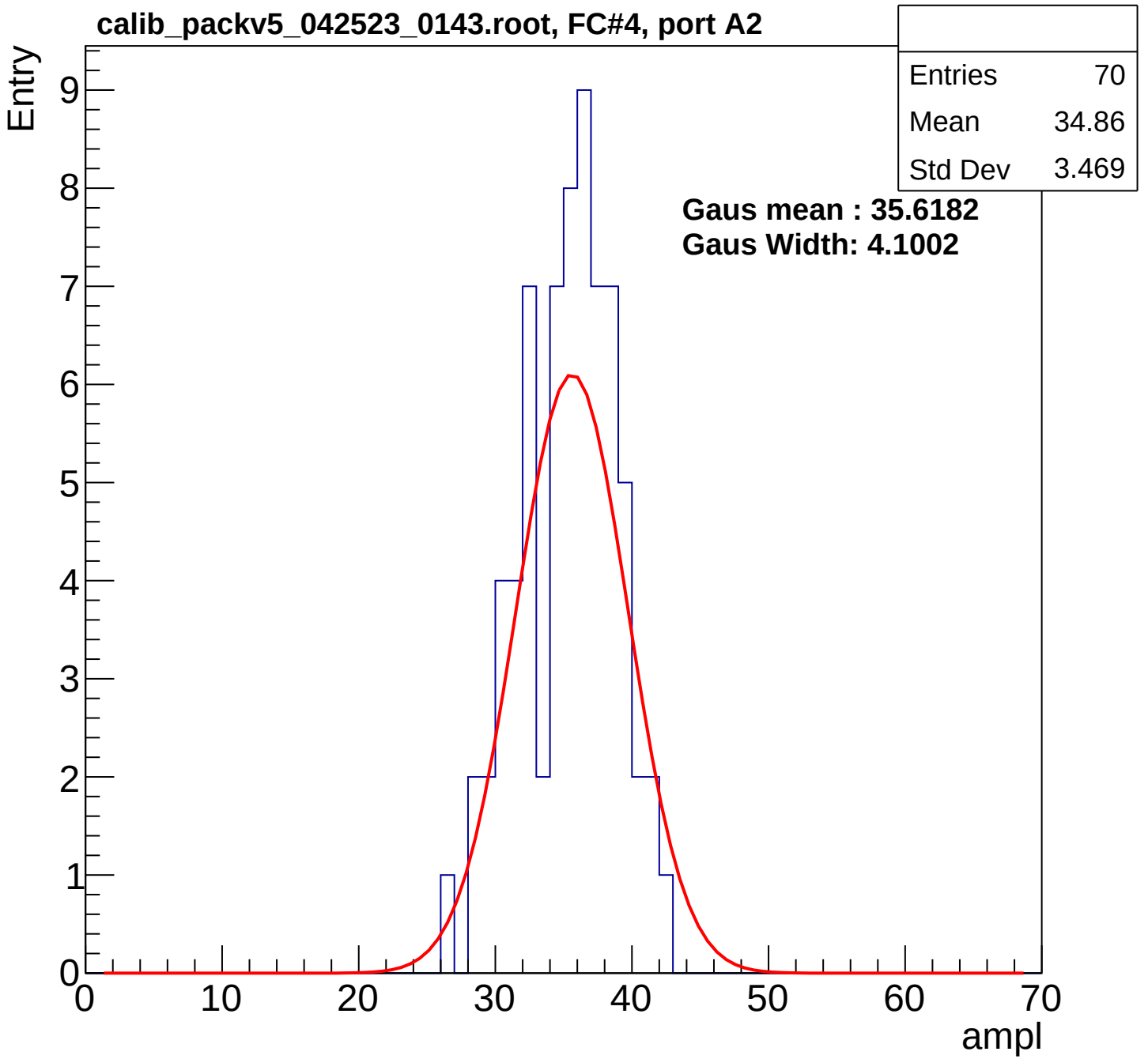

B1L100S, U17-ch73, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch74, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 80
Mean 28.14
Std Dev 5.047
Gaus mean : 28.5097
Gaus Width: 3.6492
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U17-ch74, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 34.86
Std Dev 3.469
Gaus mean : 35.6182
Gaus Width: 4.1002
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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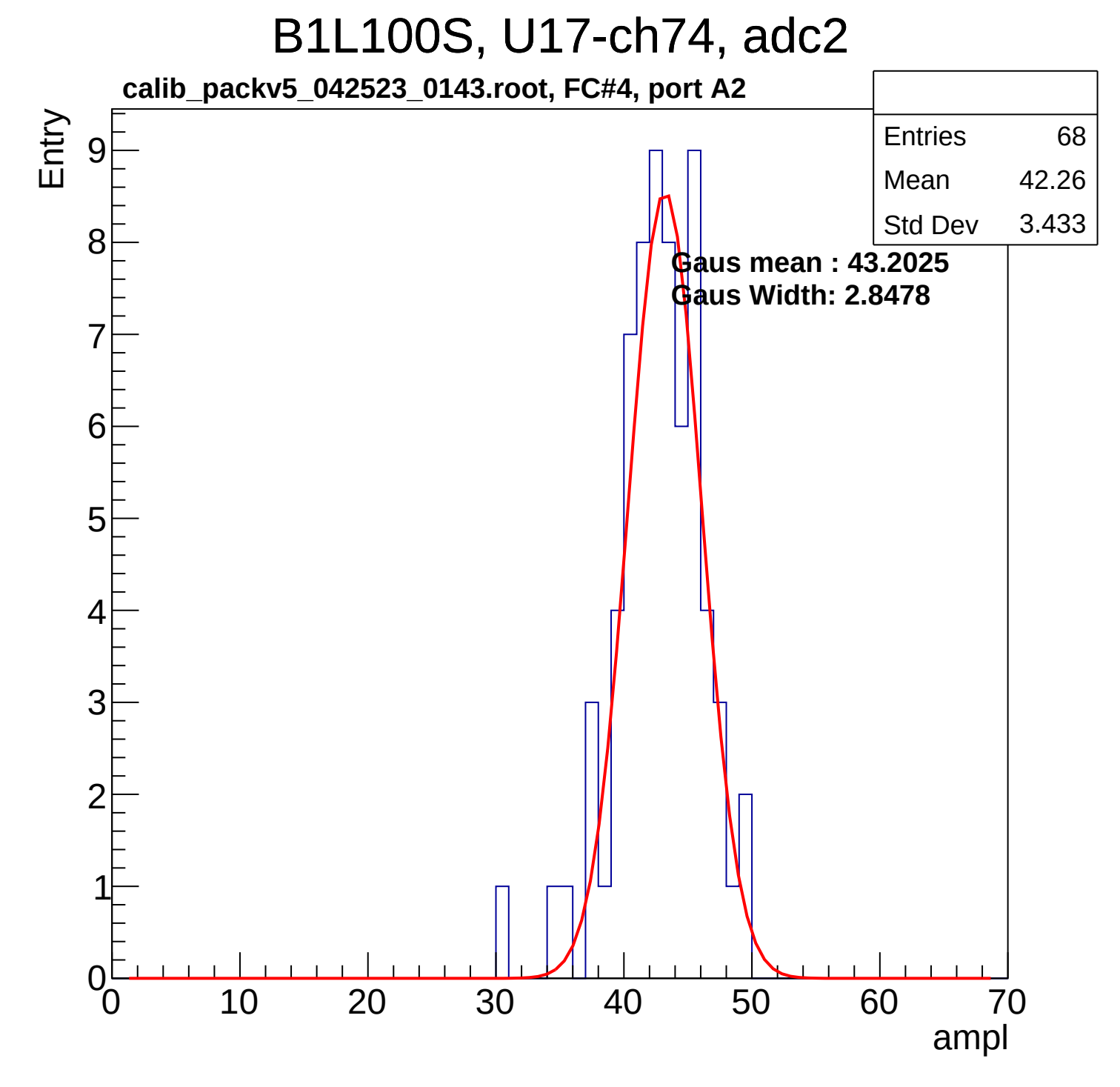
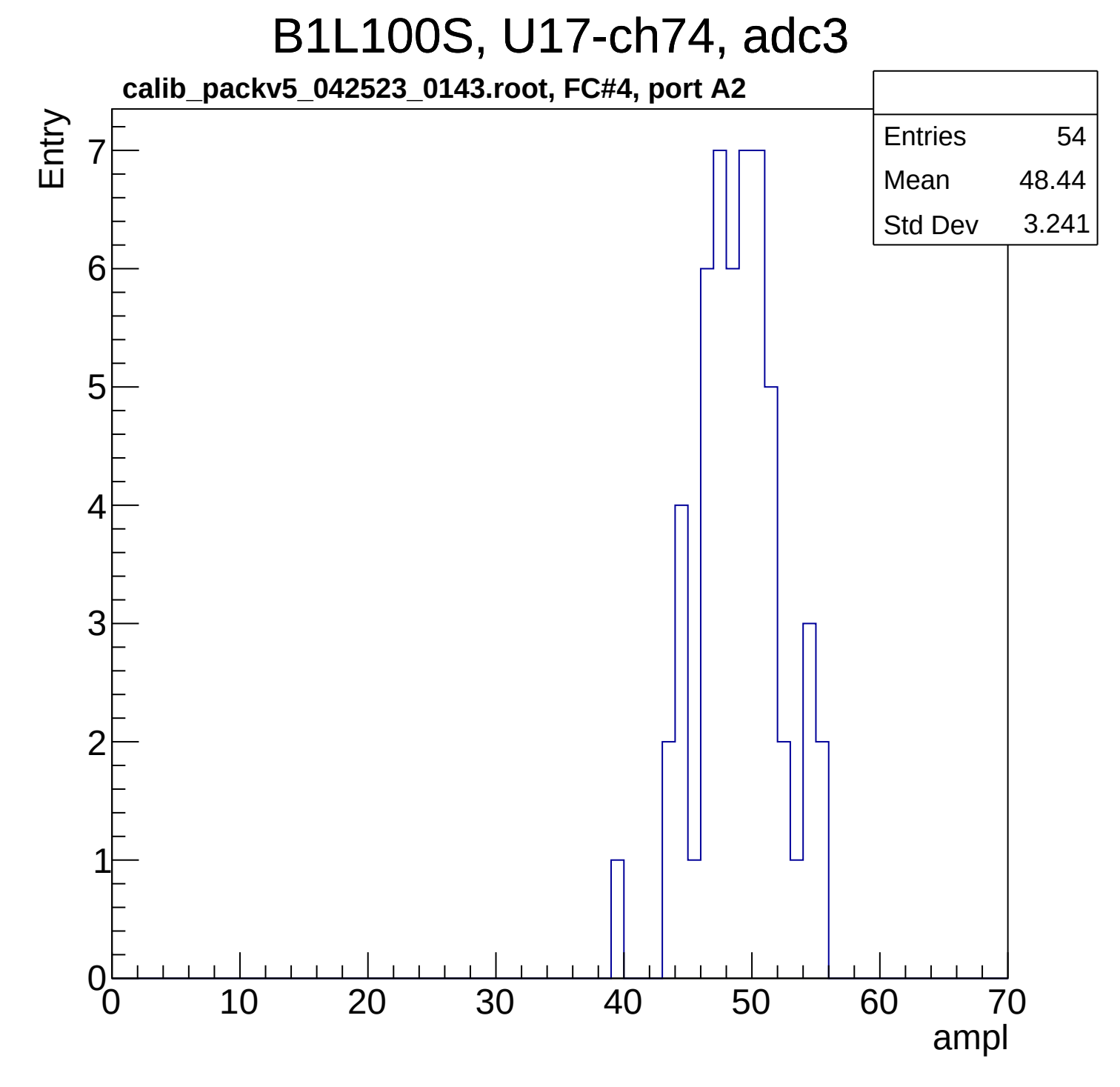
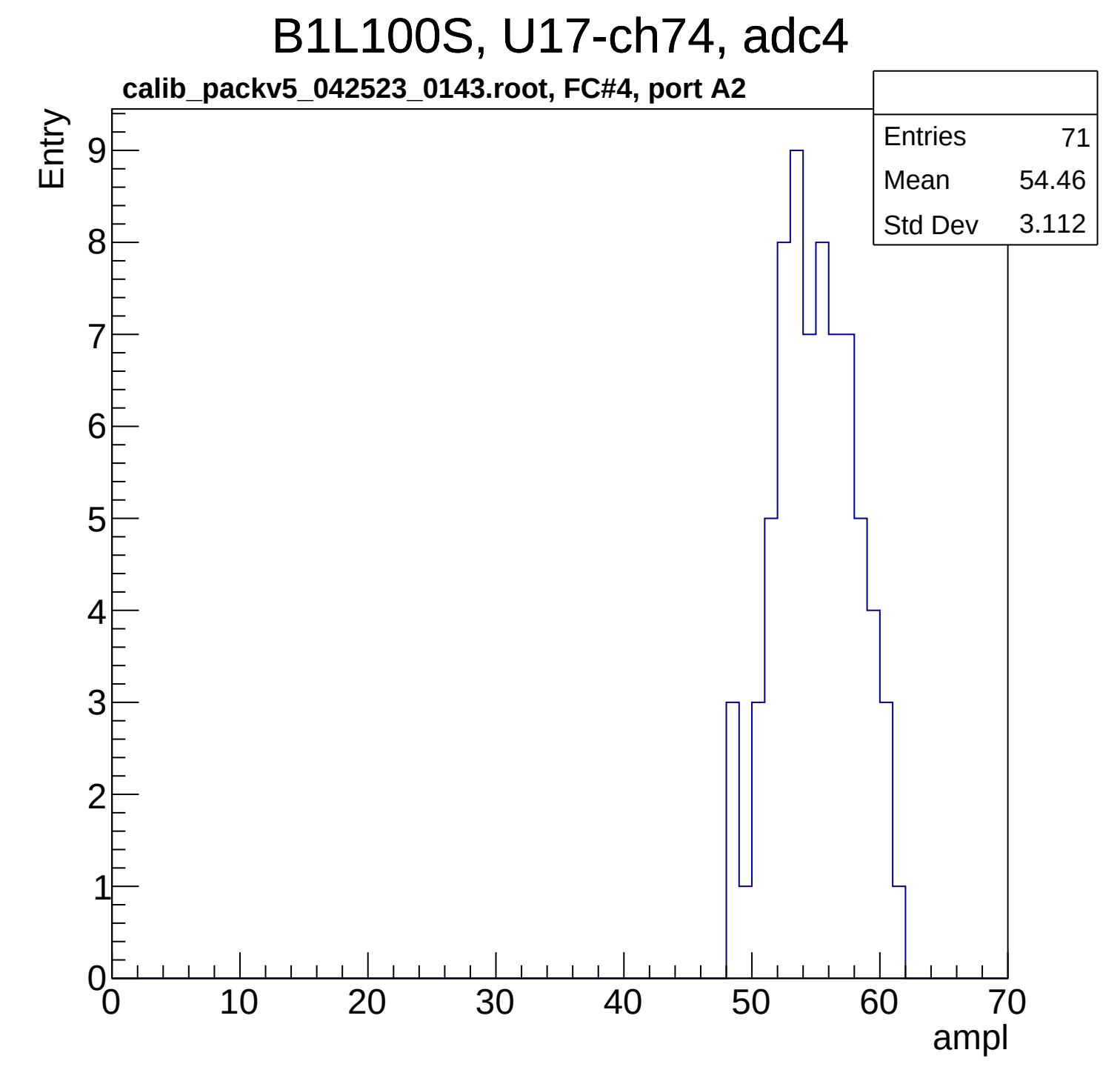
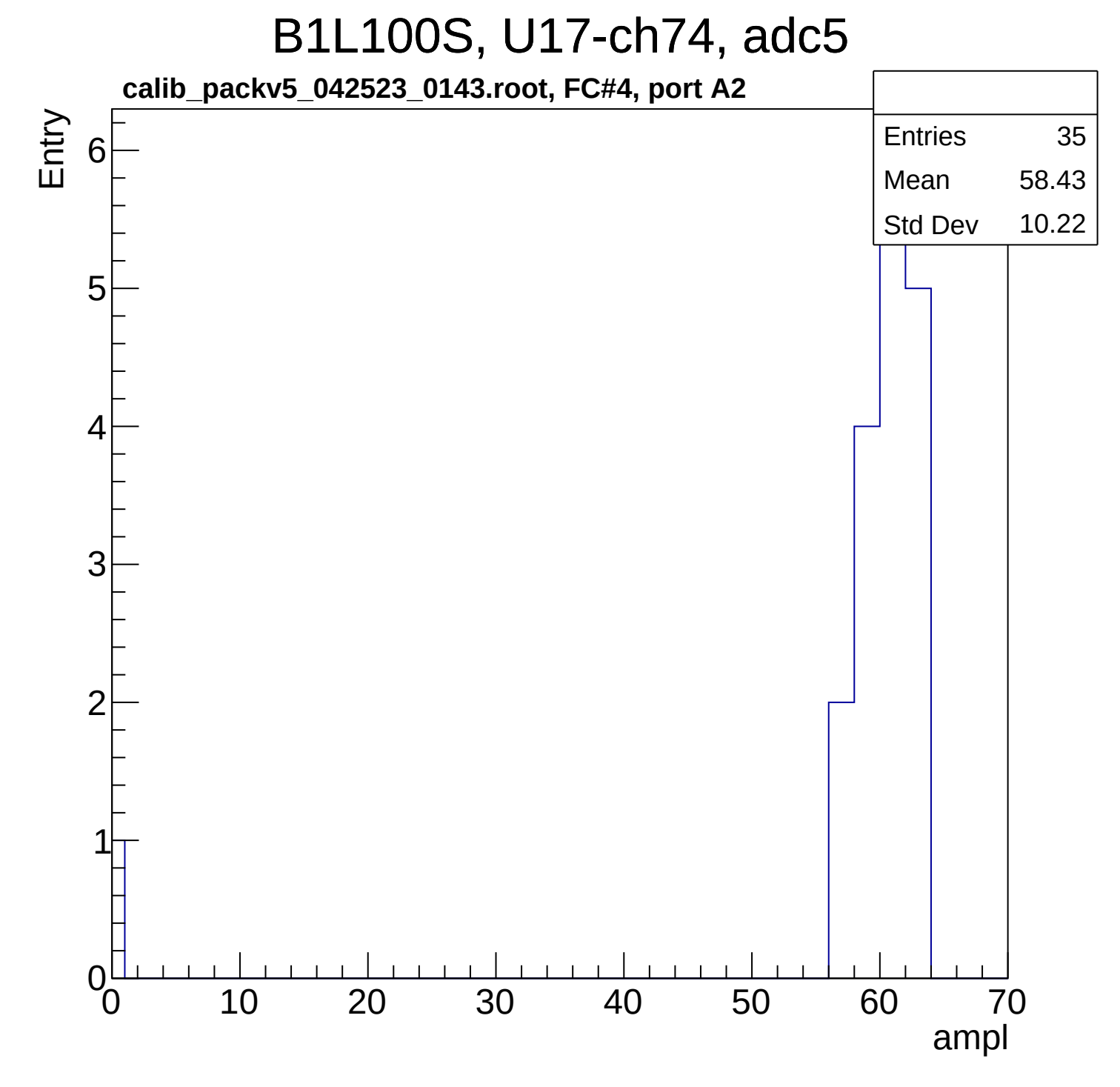
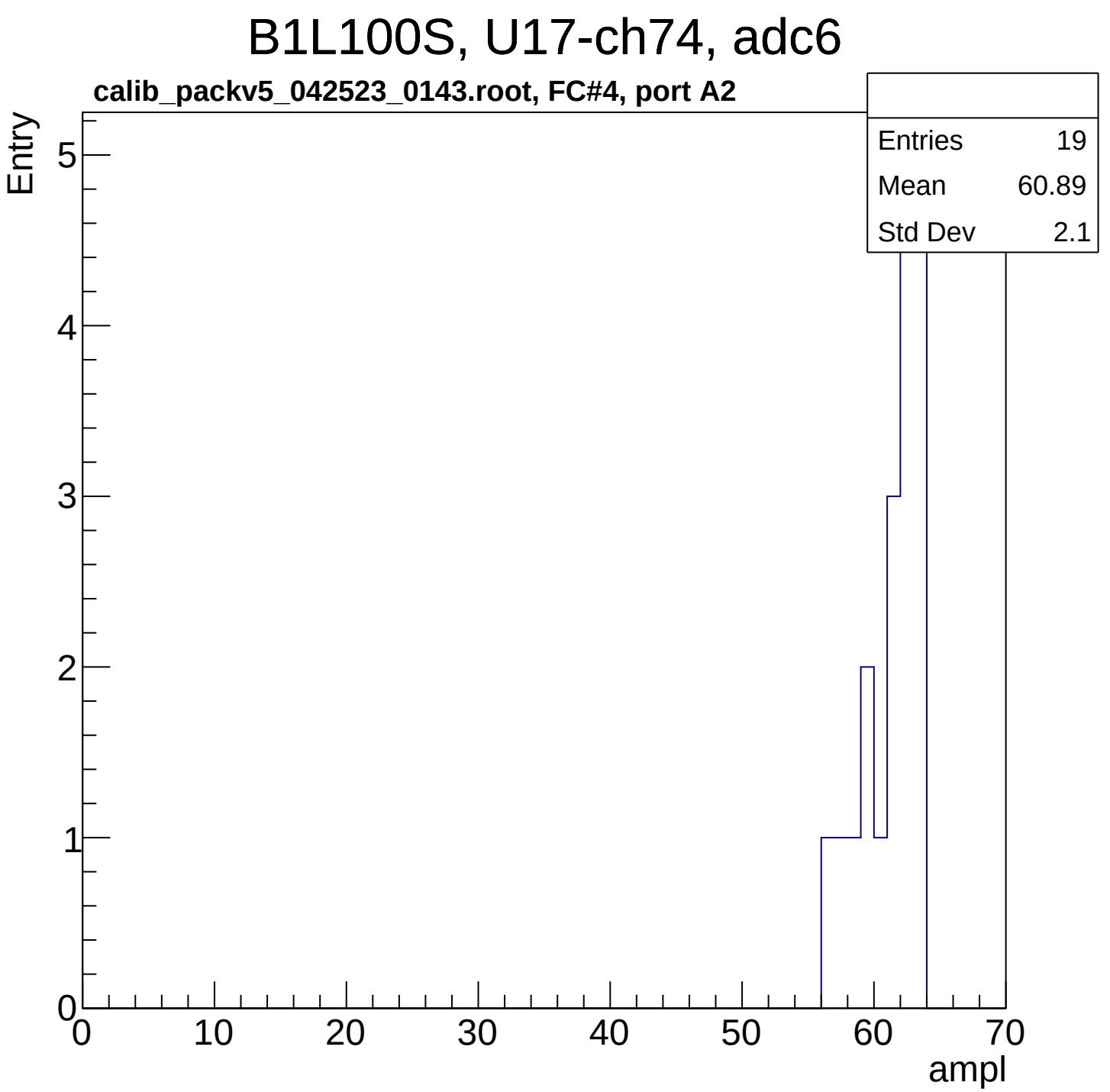
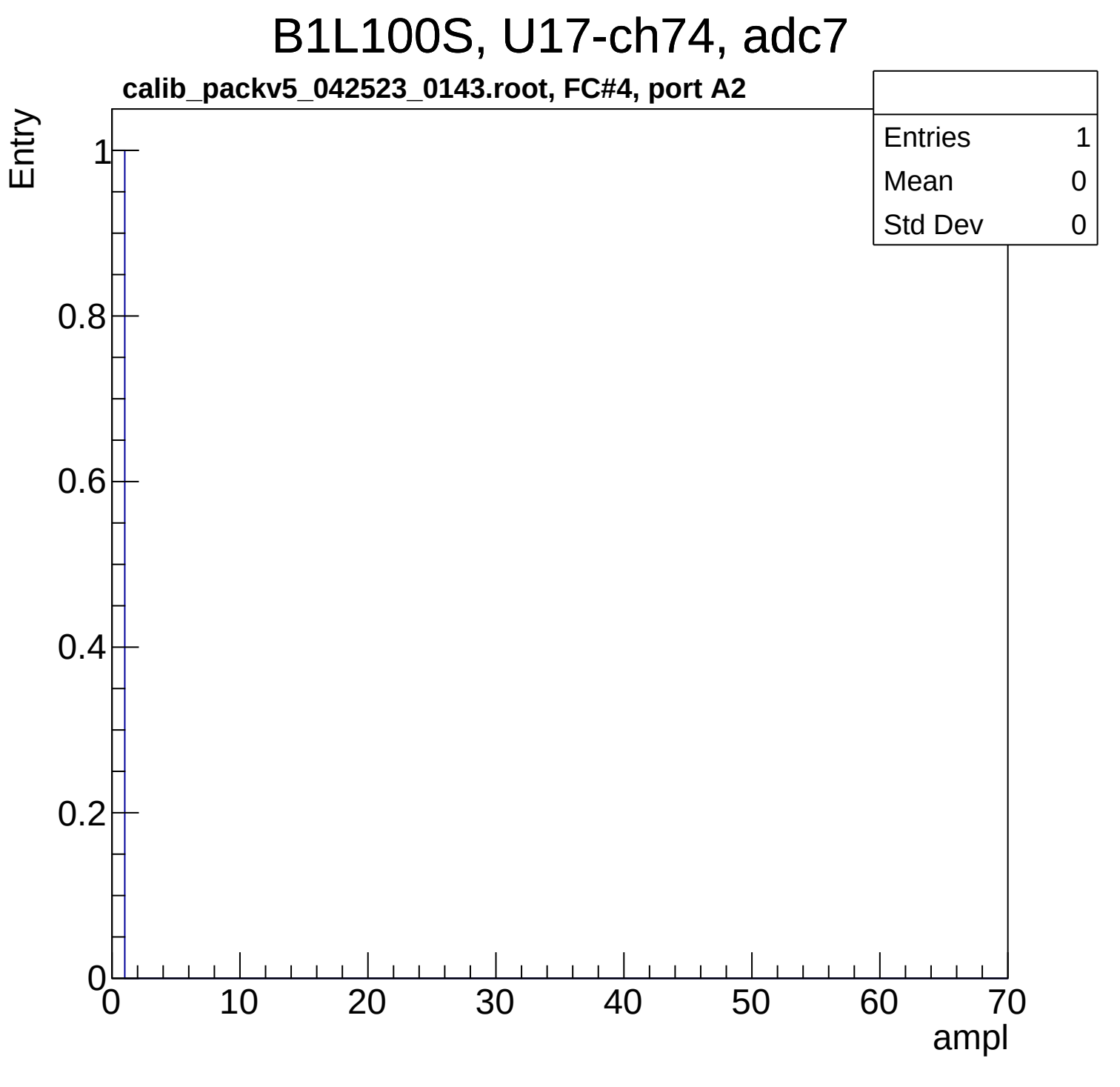

B1L100S, U17-ch74, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 42.26
Std Dev 3.433
Gaus mean : 43.2025
Gaus Width: 2.8478
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

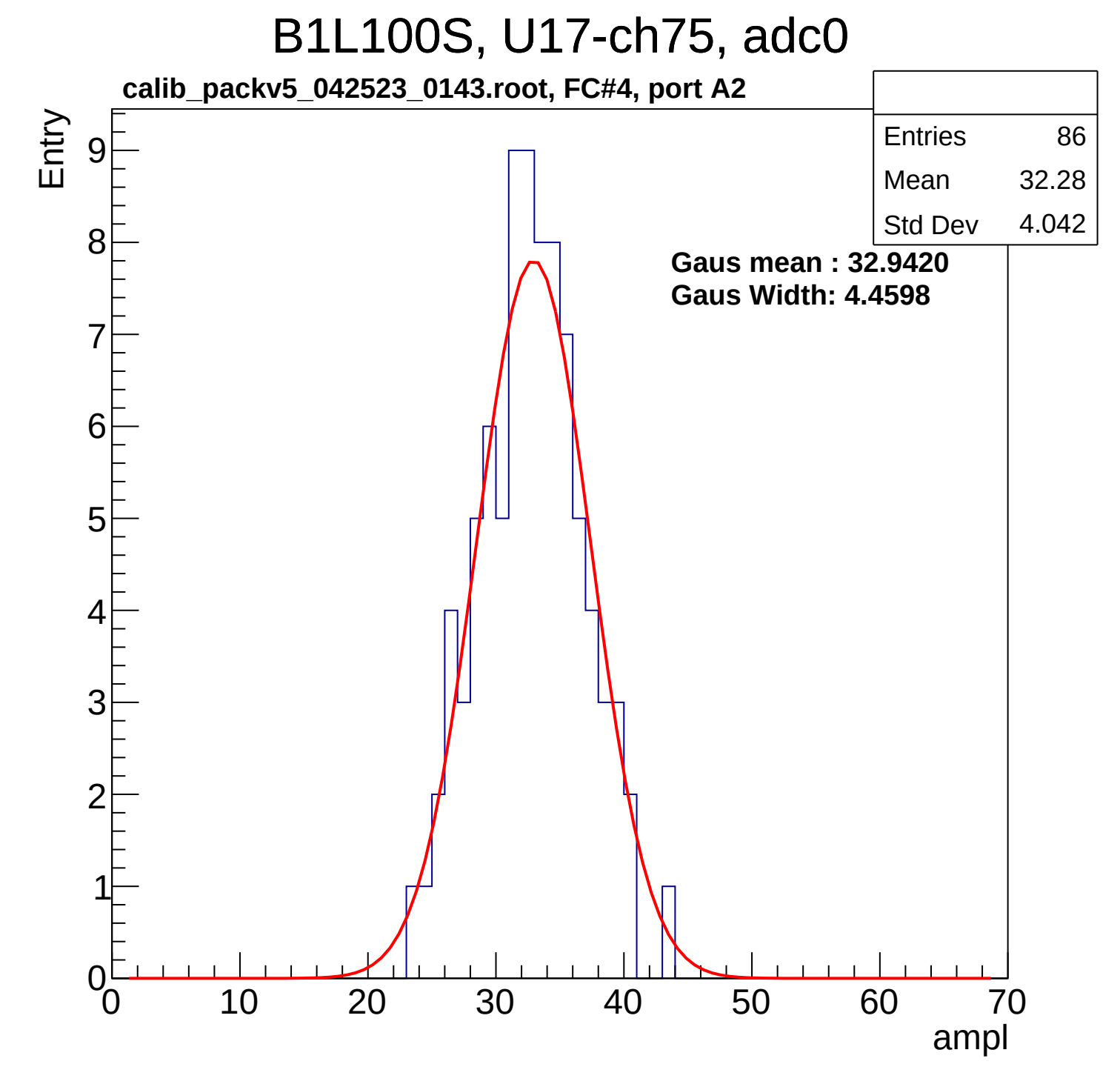

B1L100S, U17-ch74, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 48.44
Std Dev 3.241
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U17-ch74, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 54.46
Std Dev 3.112
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch74, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 35
Mean 58.43
Std Dev 10.22
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch74, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 19
Mean 60.89
Std Dev 2.1
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L100S, U17-ch74, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch75, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 86
Mean 32.28
Std Dev 4.042
Gaus mean : 32.9420
Gaus Width: 4.4598
Entry
ampl
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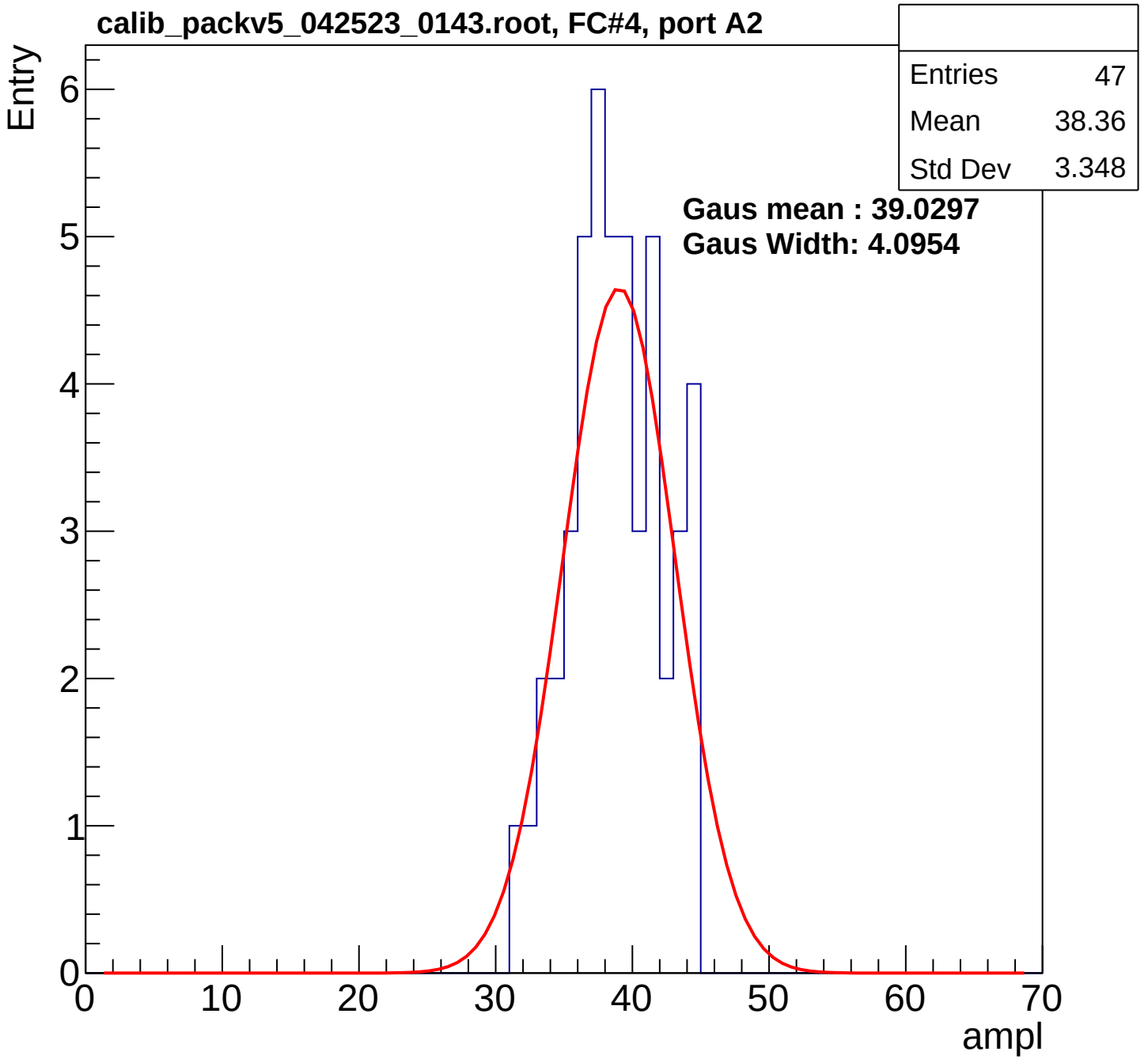
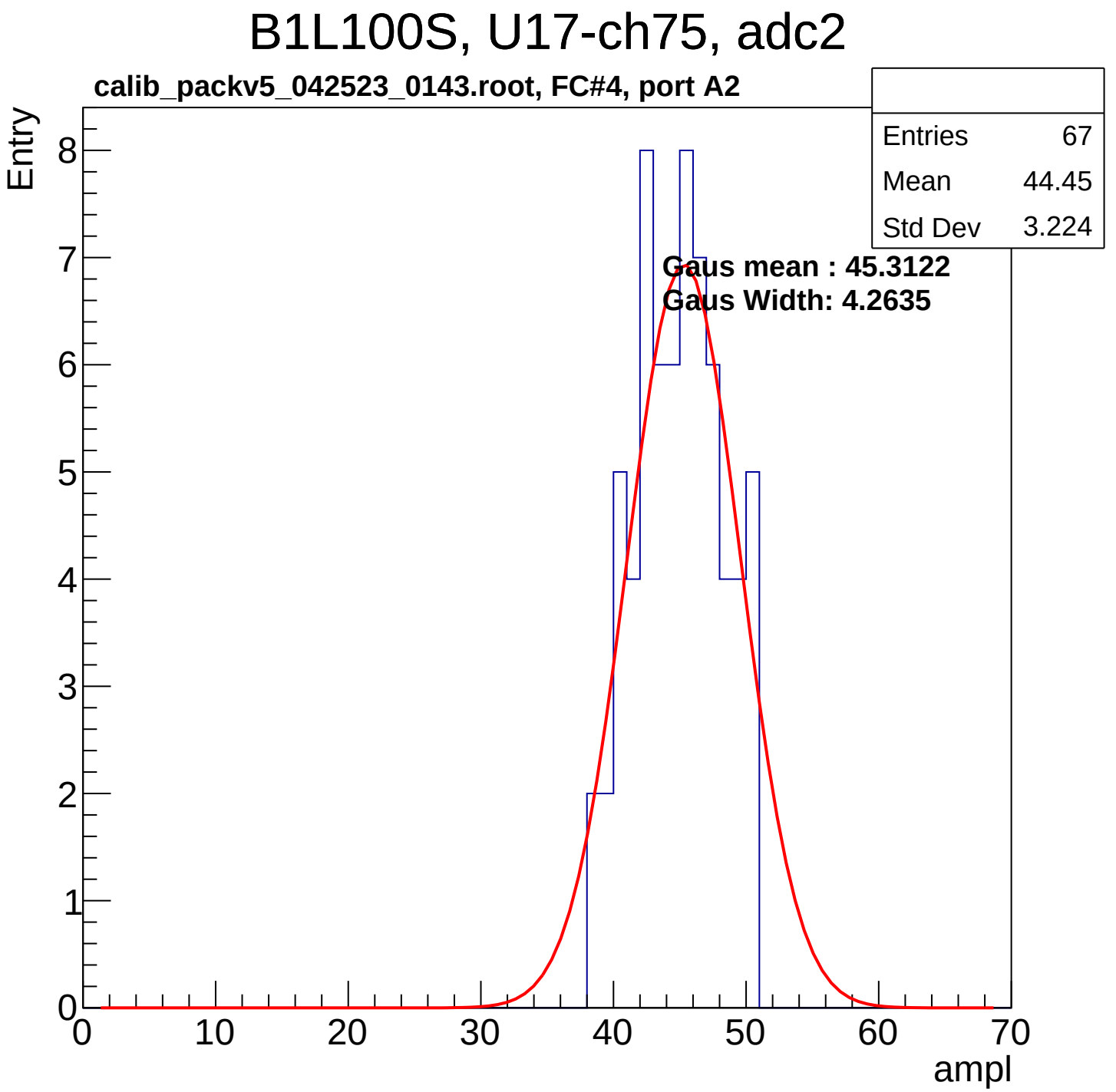
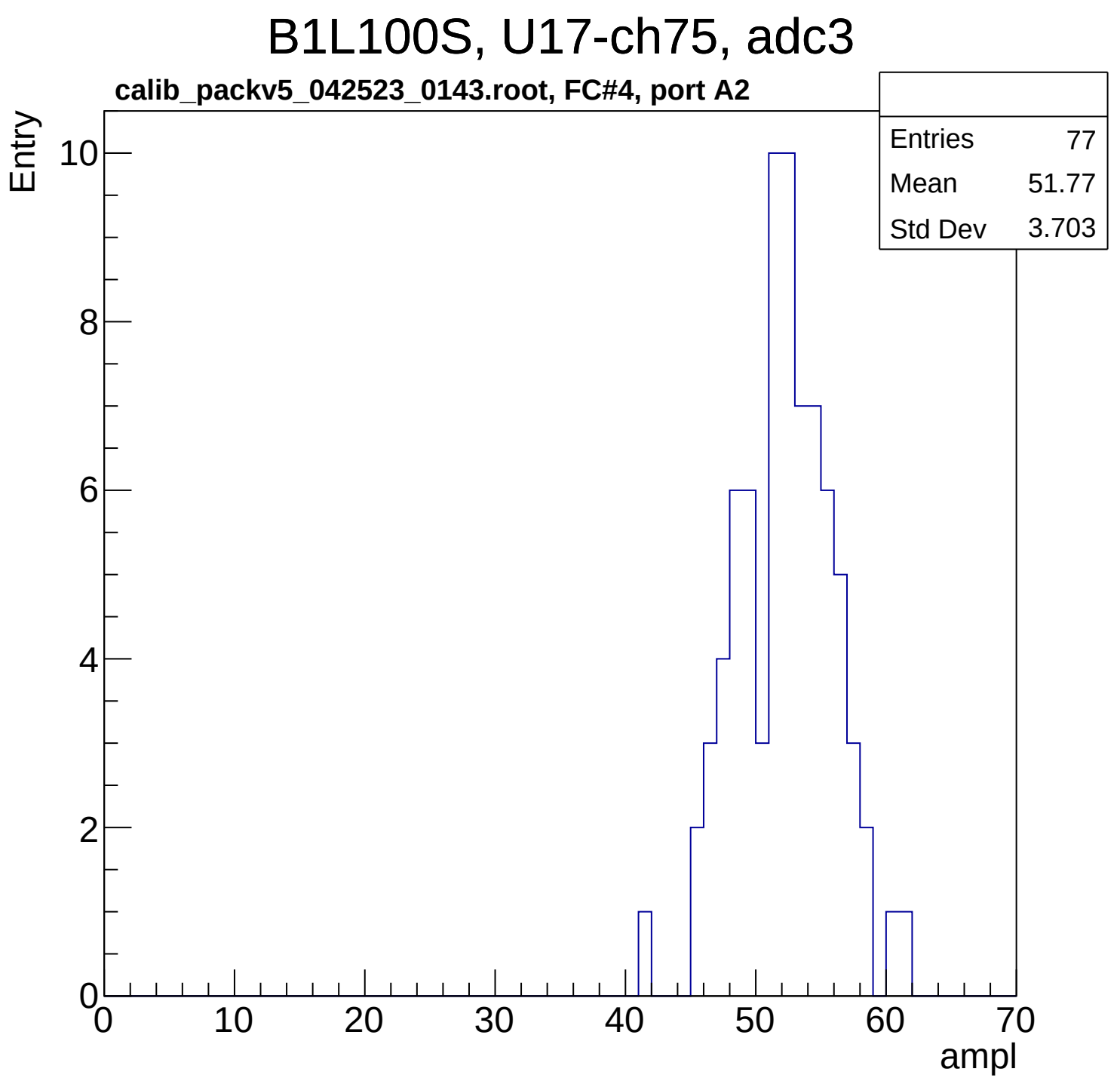
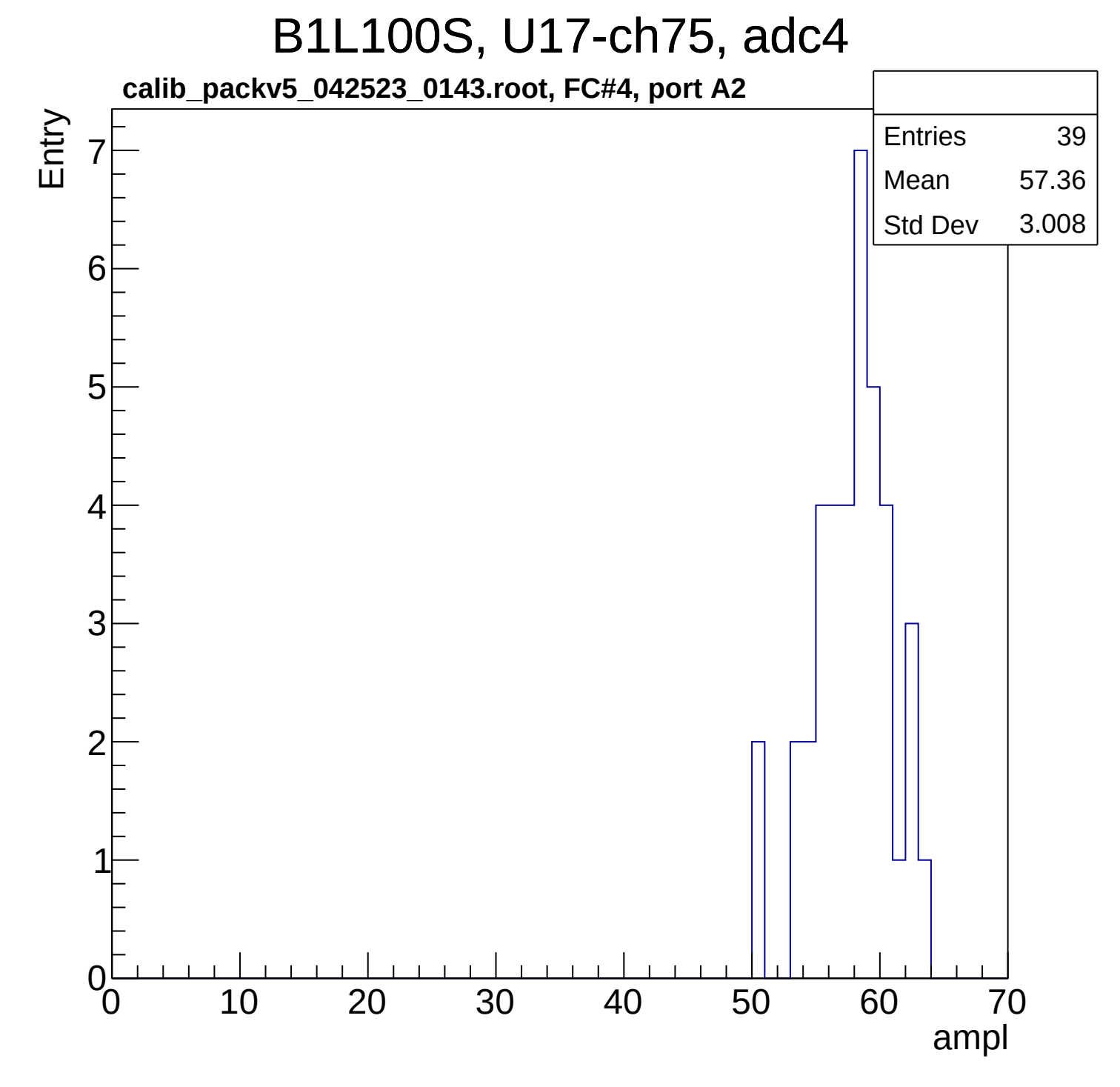
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch75, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 47
Mean 38.36
Std Dev 3.348
Gaus mean : 39.0297
Gaus Width: 4.0954
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L100S, U17-ch75, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 44.45
Std Dev 3.224
Gaus mean : 45.3122
Gaus Width: 4.2635
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch75, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 77
Mean 51.77
Std Dev 3.703
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U17-ch75, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 39
Mean 57.36
Std Dev 3.008
Entry
ampl
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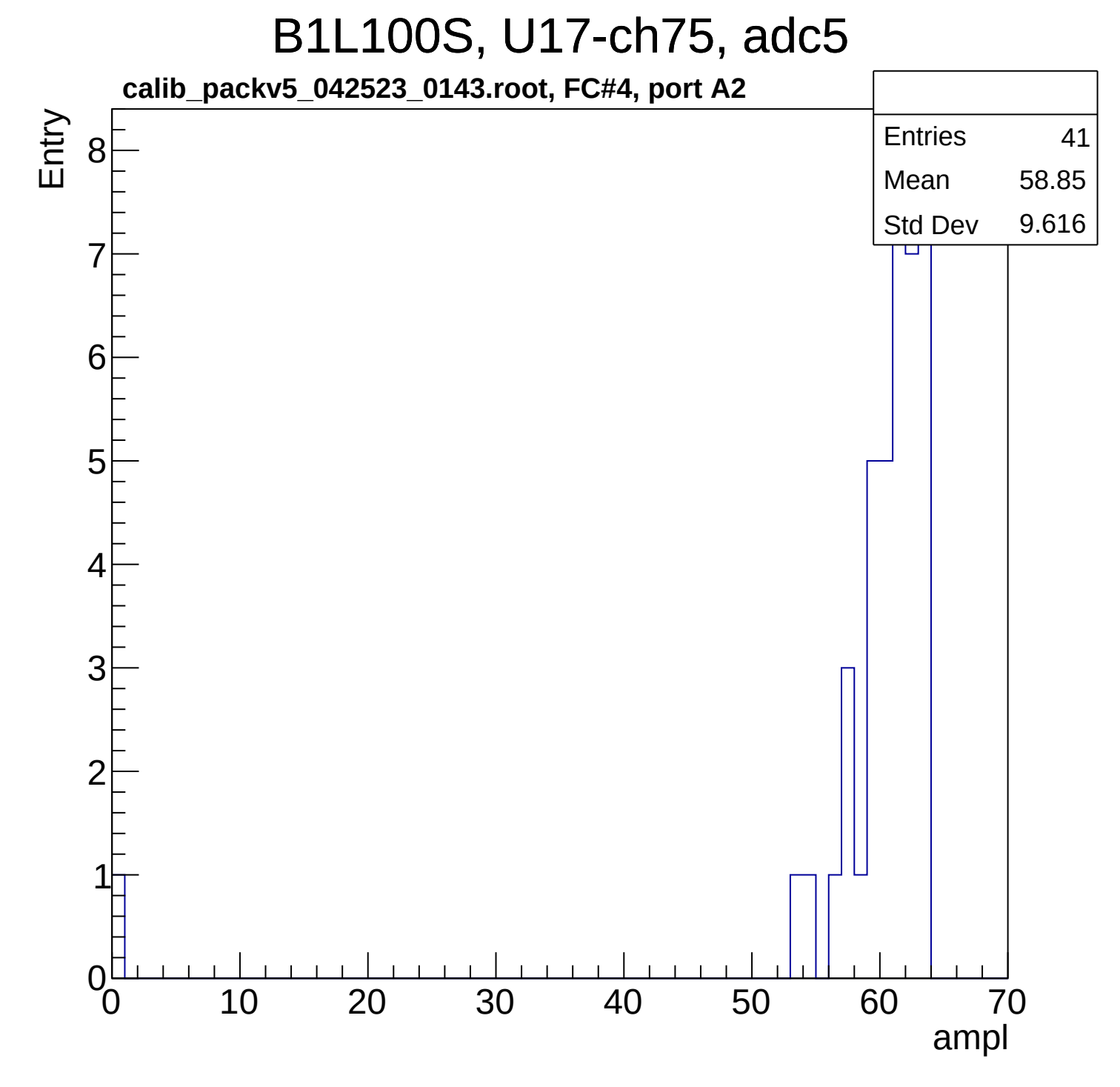
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U17-ch75, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 41
Mean 58.85
Std Dev 9.616
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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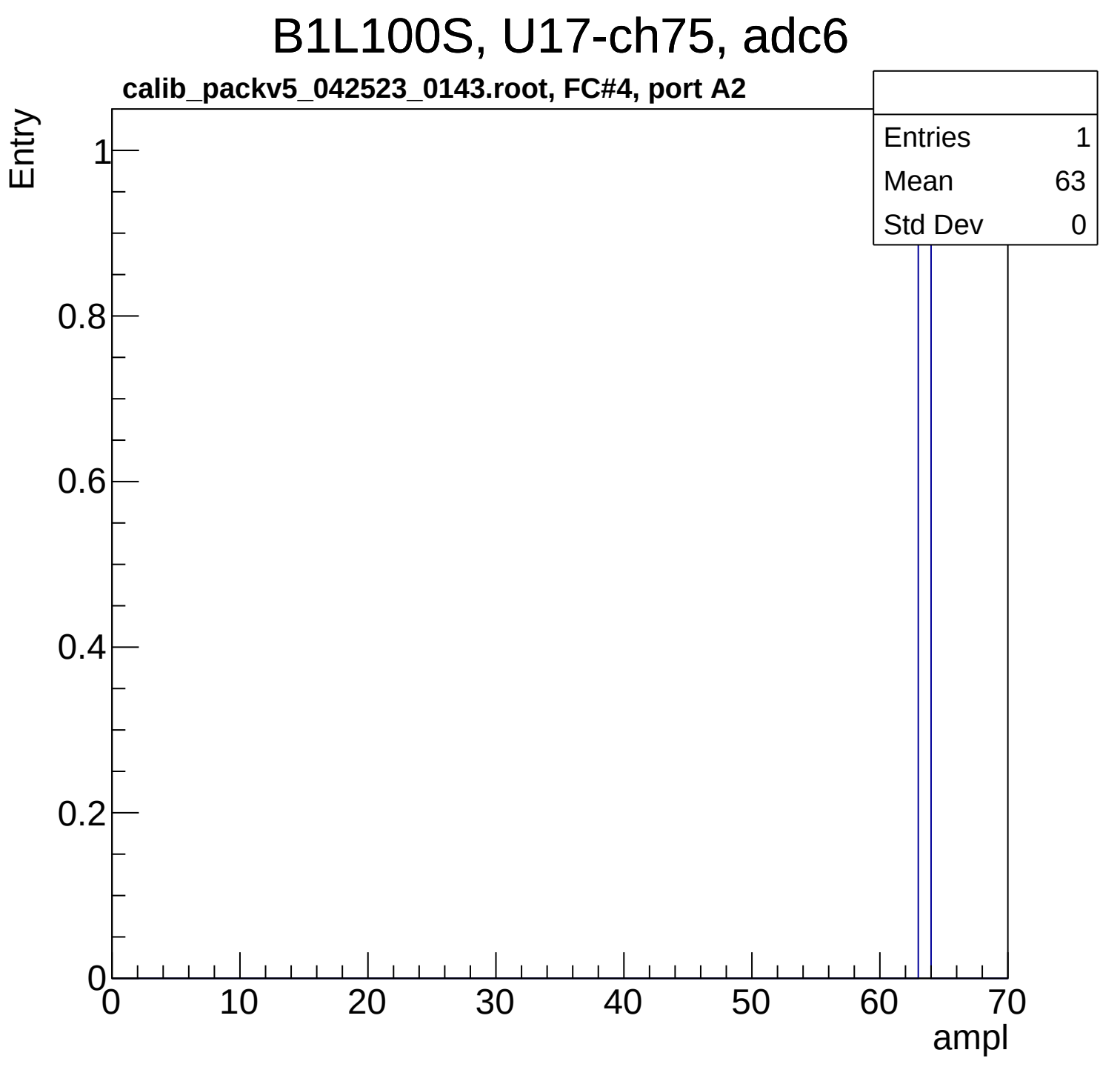
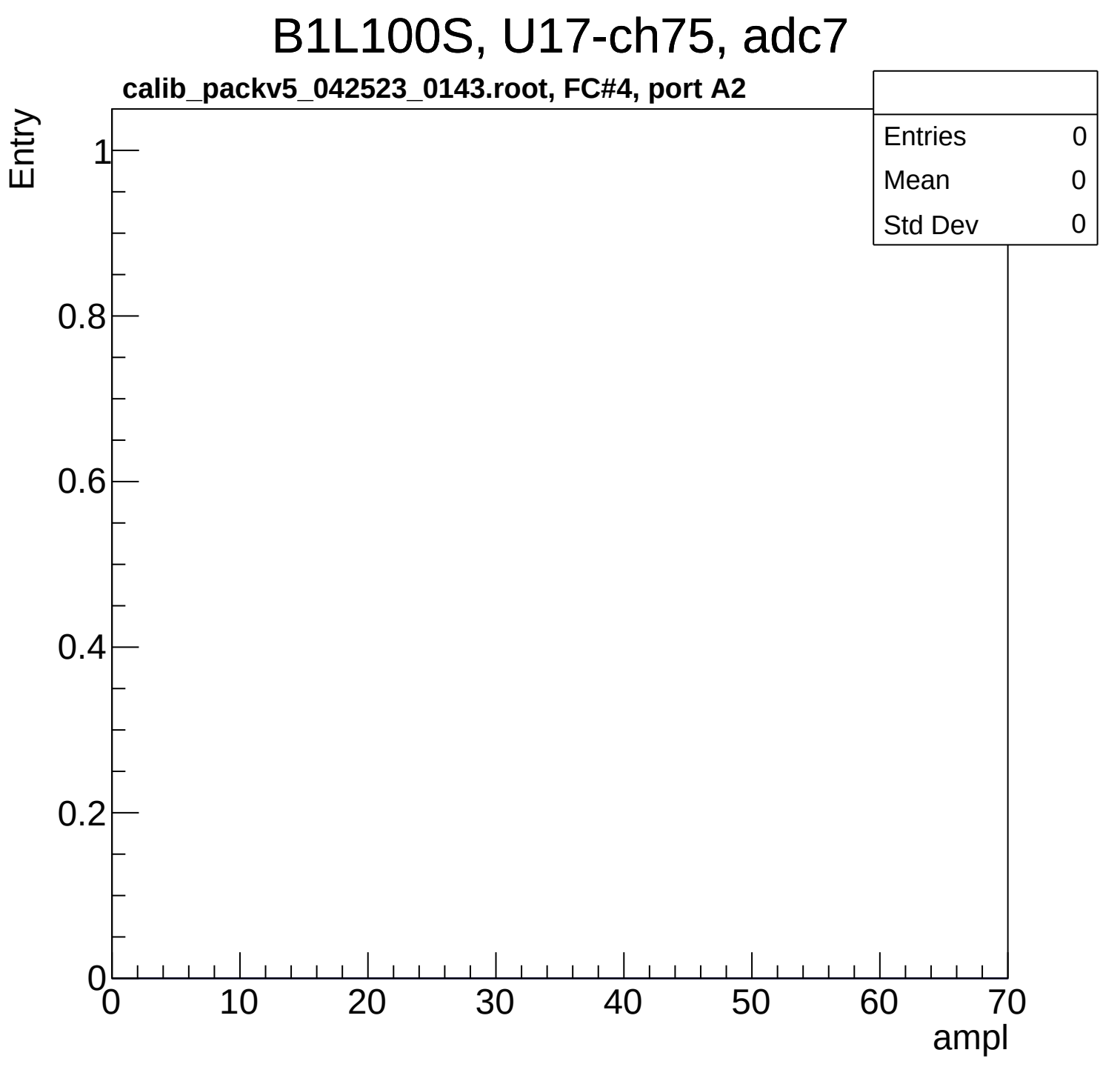

B1L100S, U17-ch75, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch75, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
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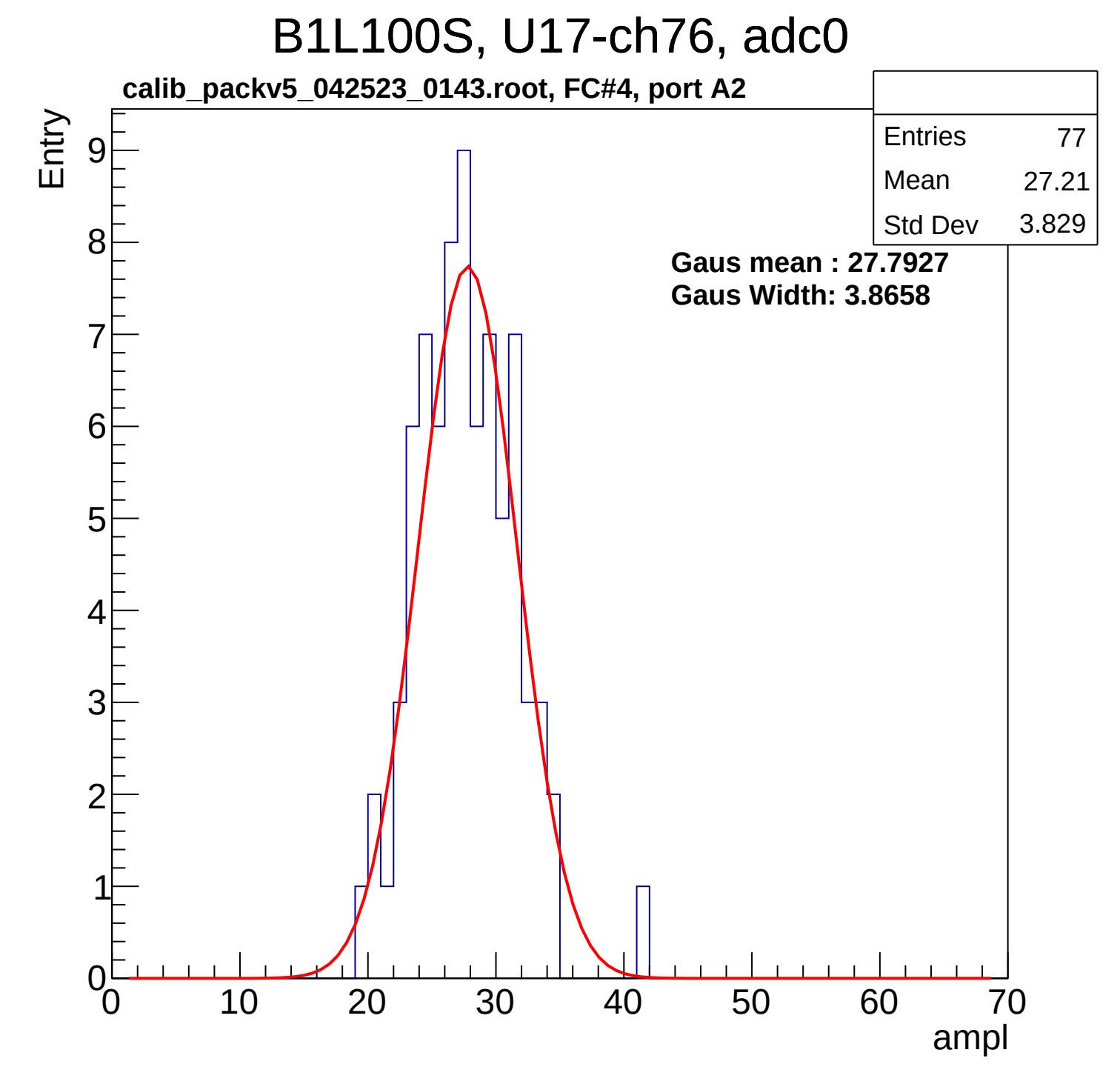
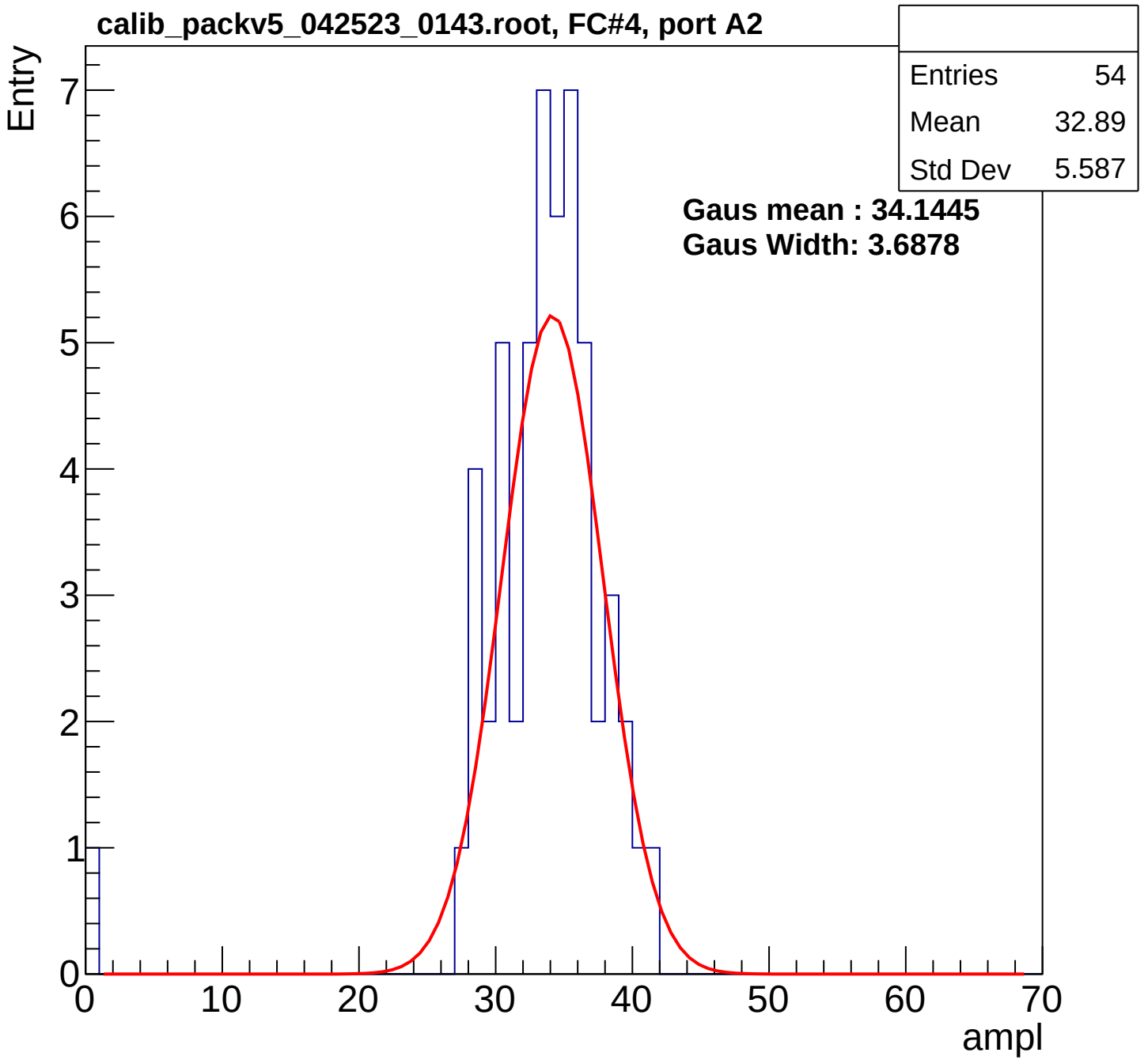
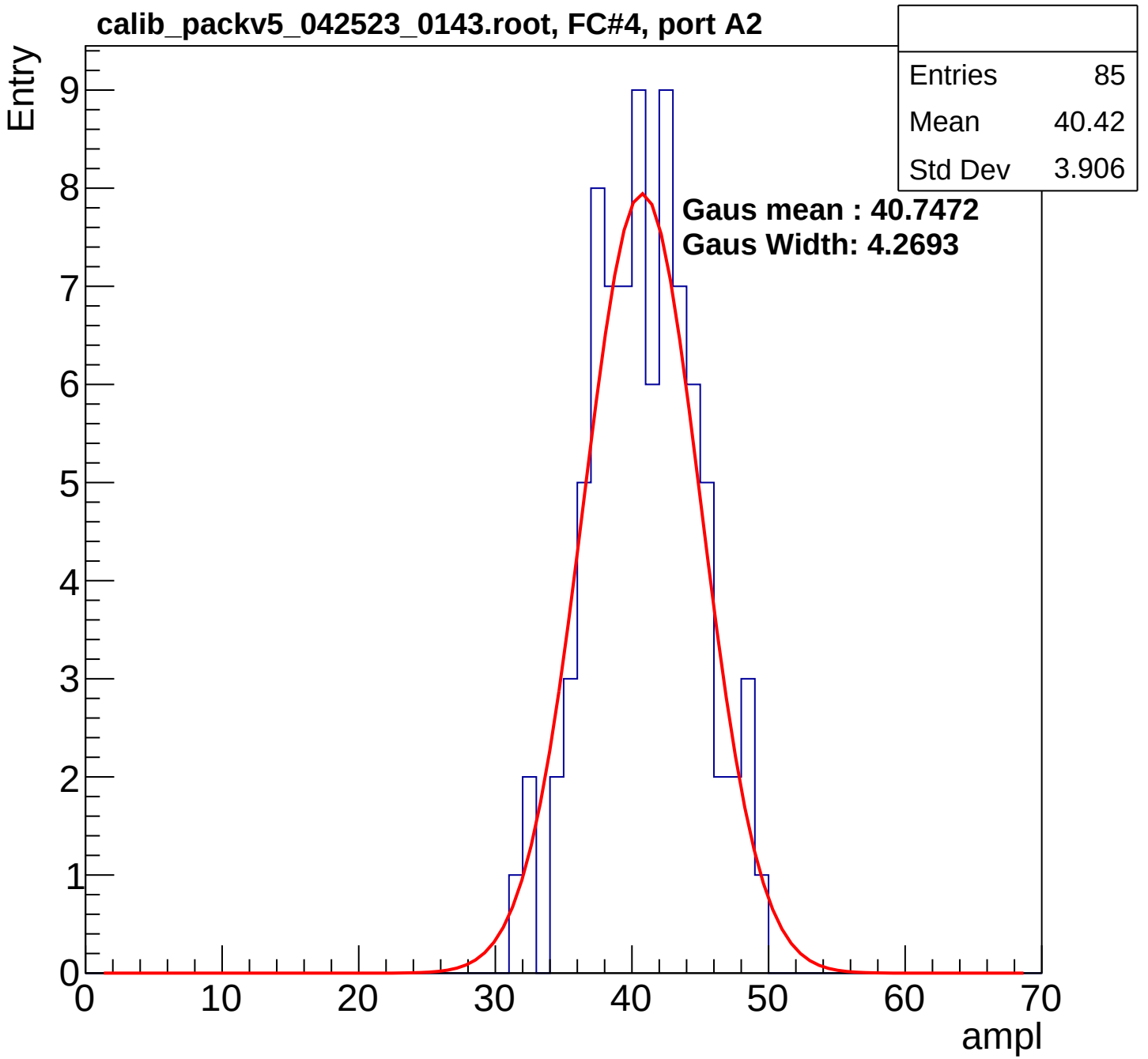
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch76, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 77
Mean 27.21
Std Dev 3.829
Gaus mean : 27.7927
Gaus Width: 3.8658
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch76, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 32.89
Std Dev 5.587
Gaus mean : 34.1445
Gaus Width: 3.6878
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U17-ch76, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 85
Mean 40.42
Std Dev 3.906
Gaus mean : 40.7472
Gaus Width: 4.2693
Entry
ampl
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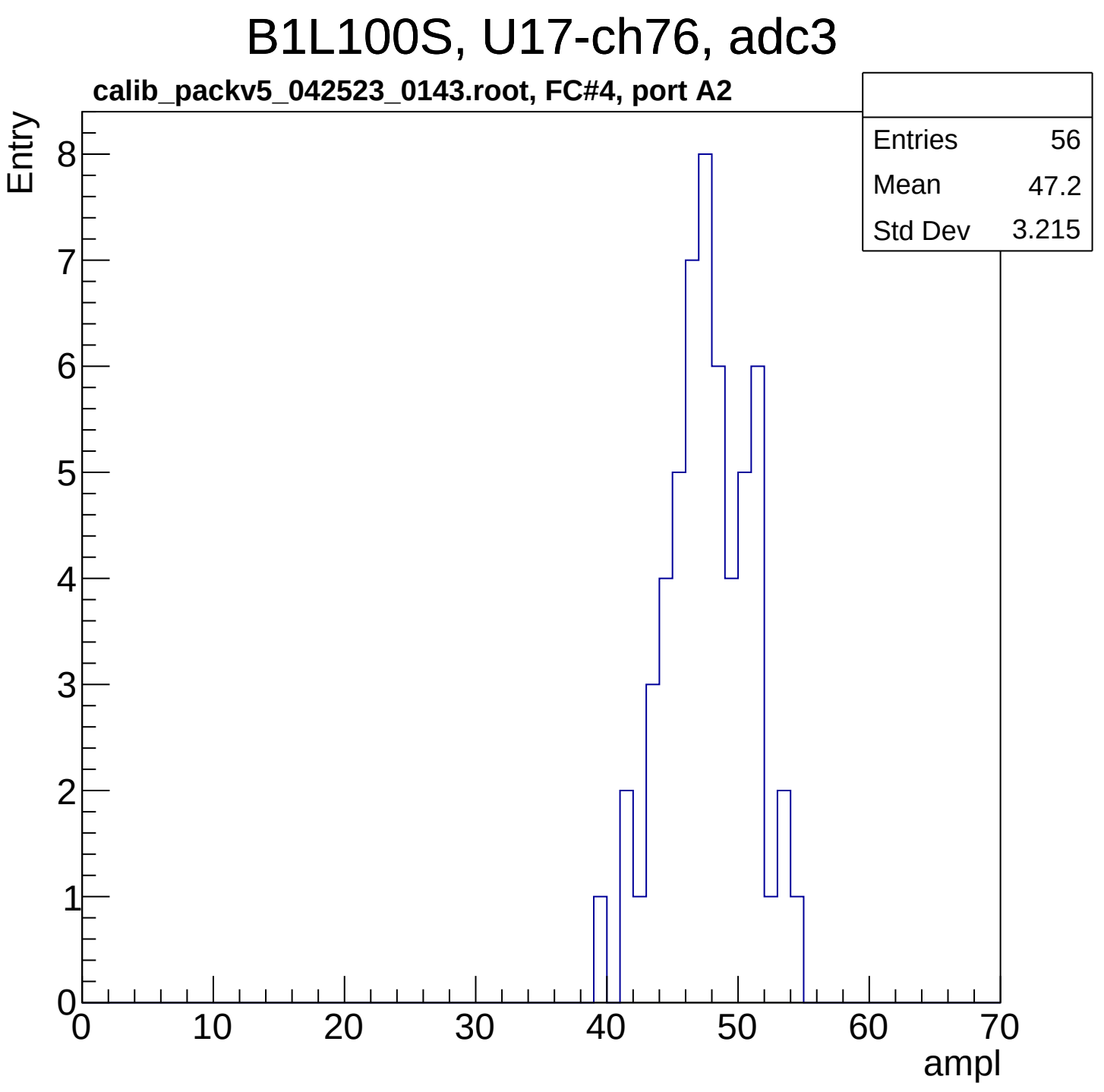
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch76, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 47.2
Std Dev 3.215
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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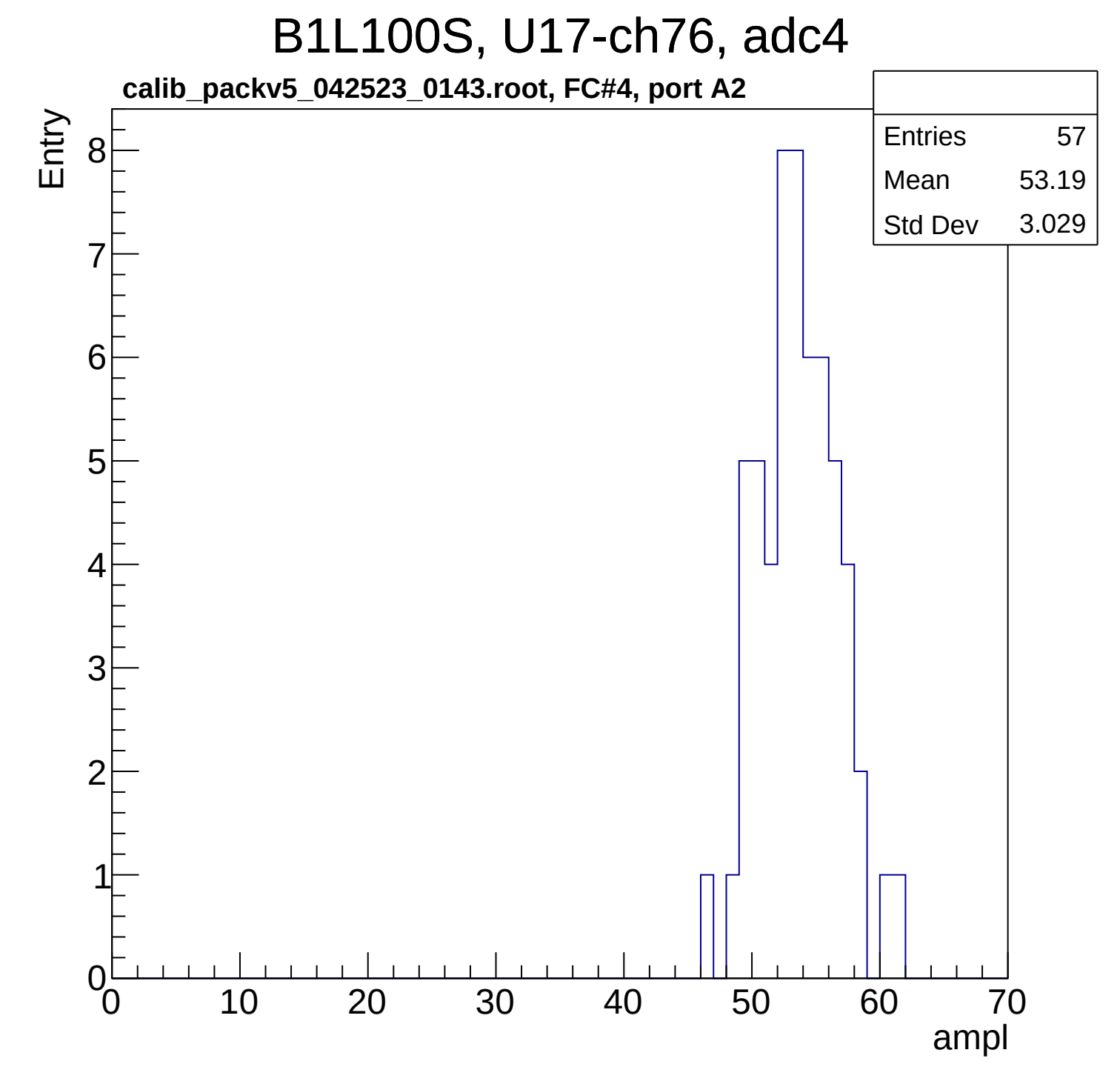
B1L100S, U17-ch76, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 53.19
Std Dev 3.029
Entry
ampl
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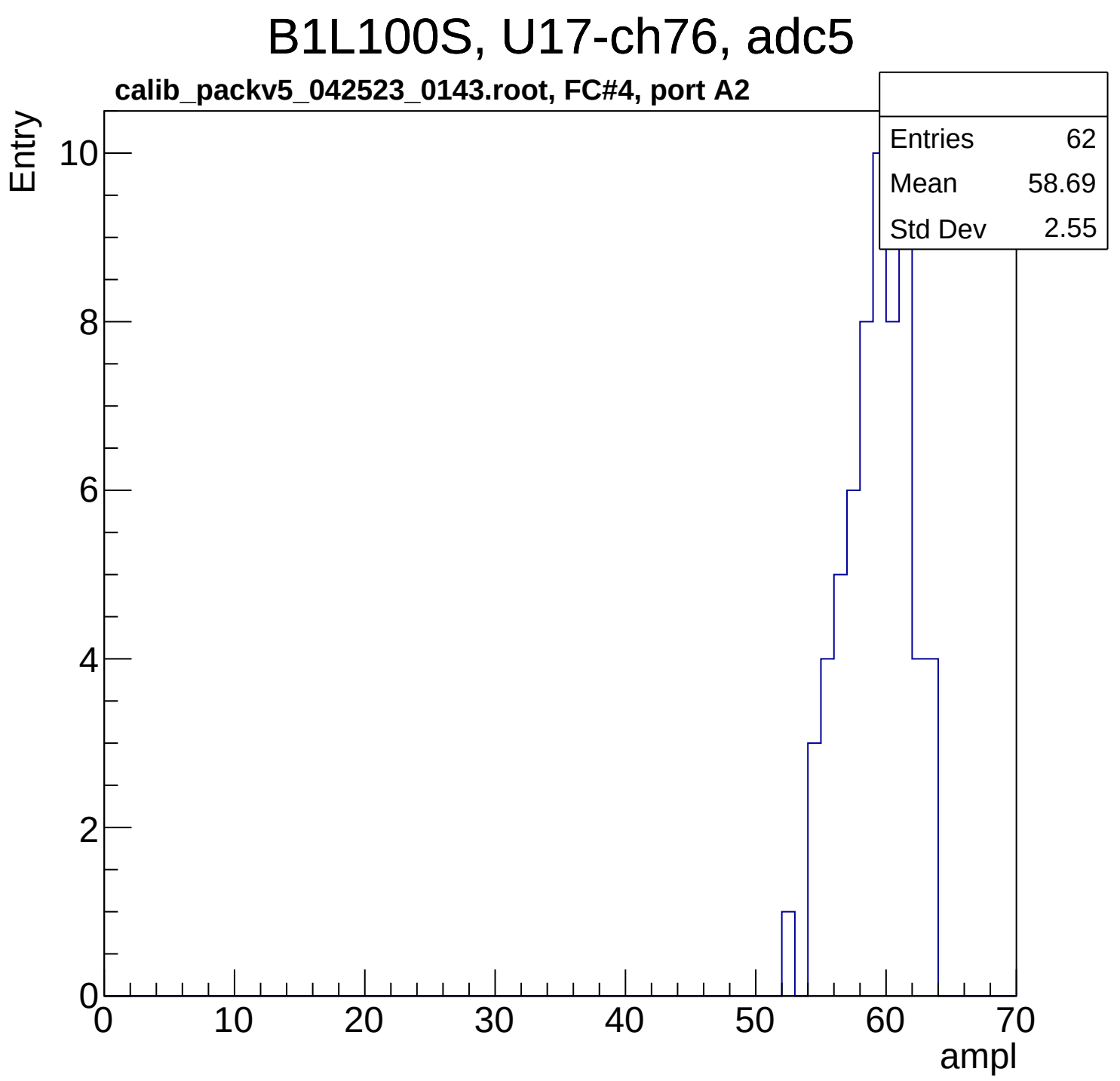
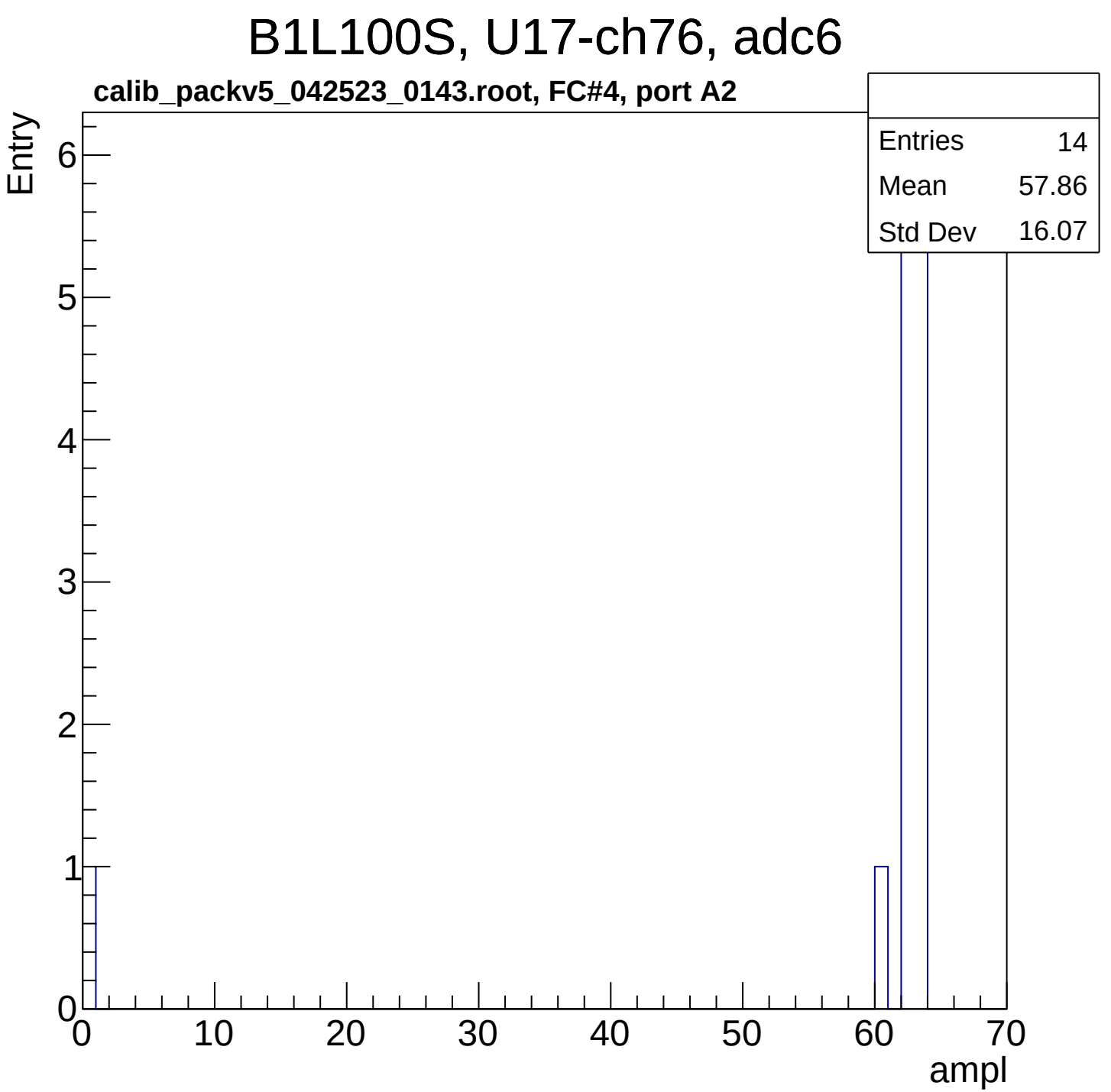
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch76, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 58.69
Std Dev 2.55
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U17-ch76, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 14
Mean 57.86
Std Dev 16.07
Entry
ampl
0
1
2
3
4
5
6
0
10
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30
40
50
60
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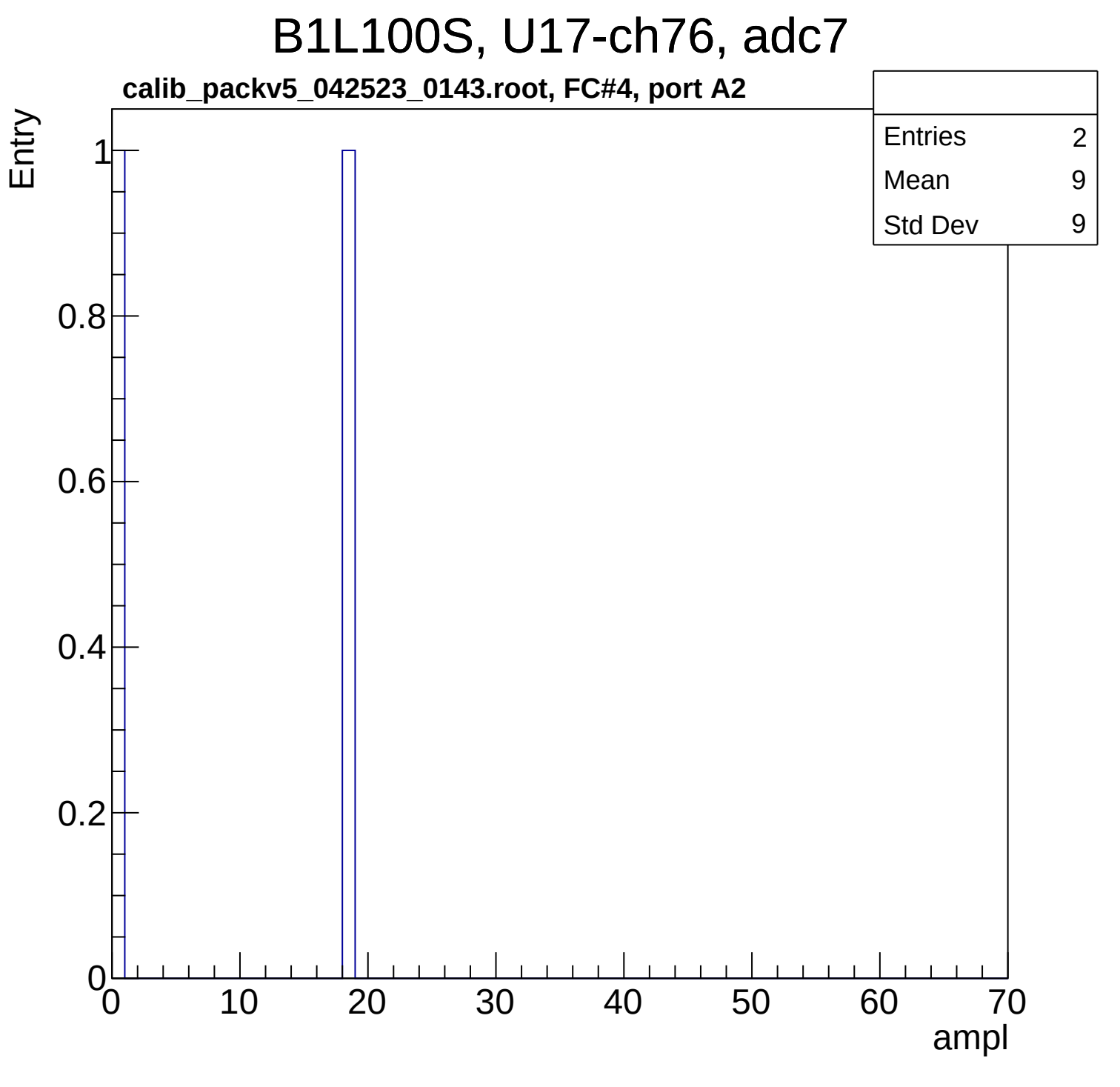
B1L100S, U17-ch76, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 9
Std Dev 9
Entry
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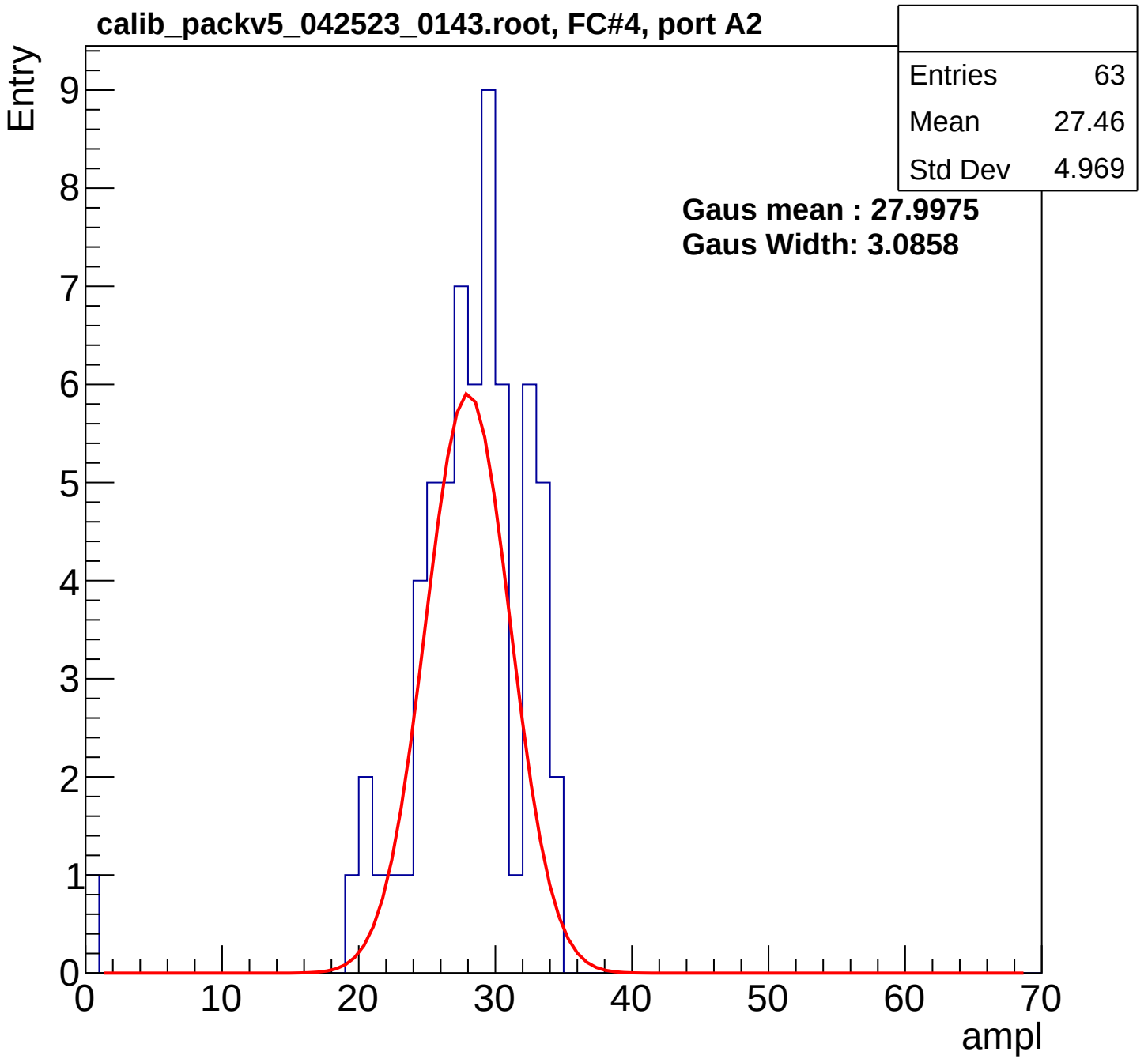
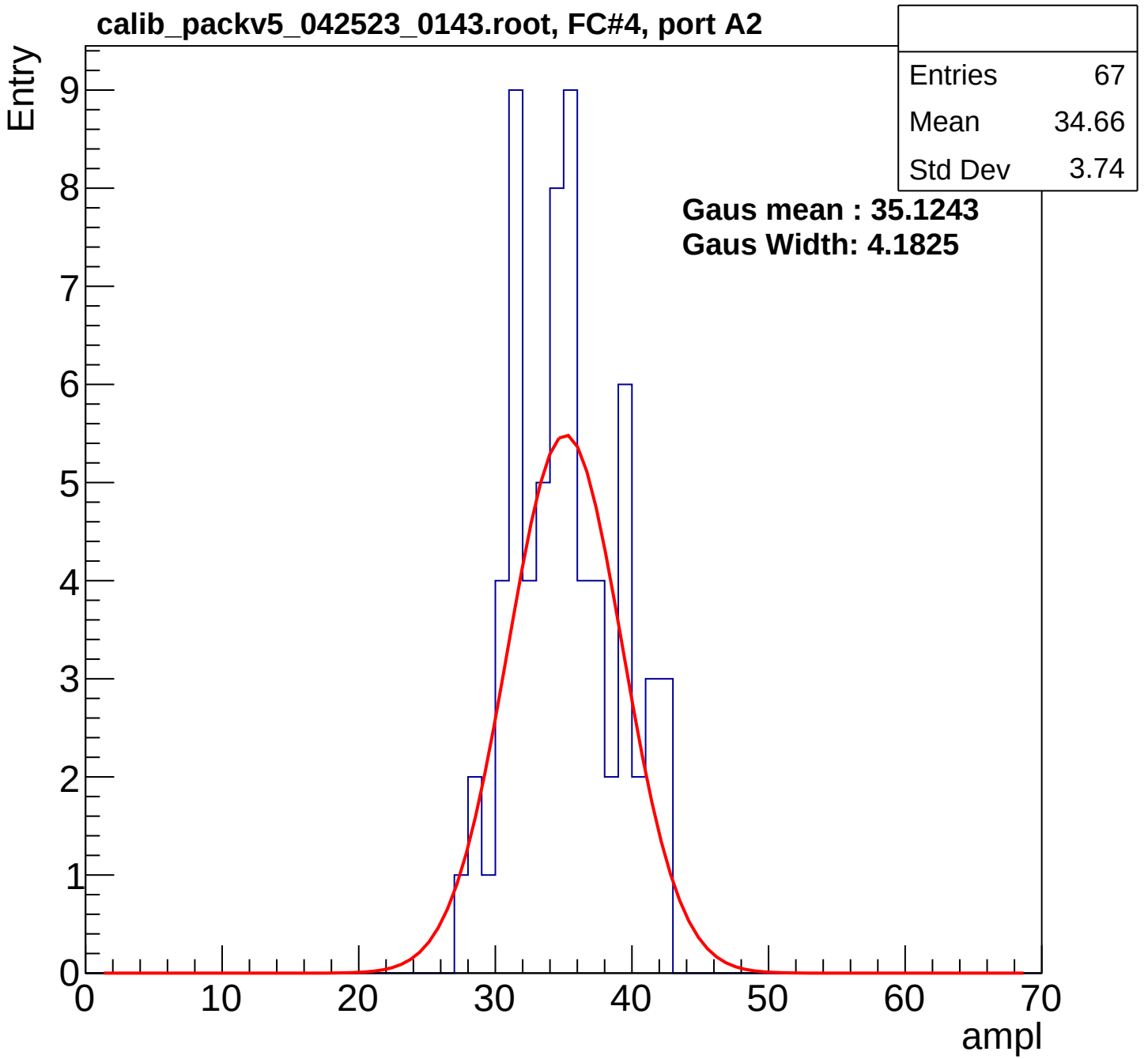
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch77, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 27.46
Std Dev 4.969
Gaus mean : 27.9975
Gaus Width: 3.0858
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch77, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 34.66
Std Dev 3.74
Gaus mean : 35.1243
Gaus Width: 4.1825
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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40
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60
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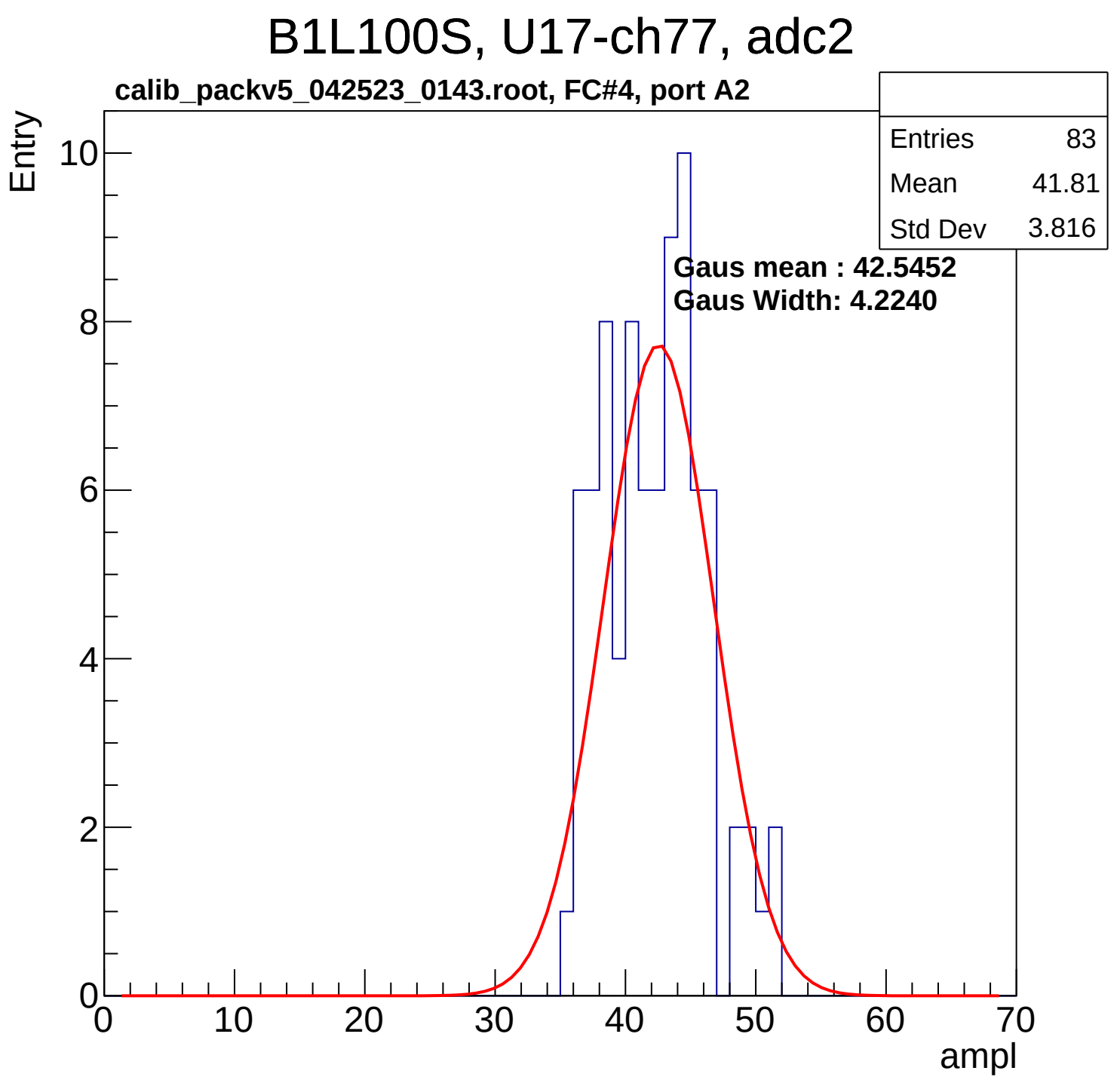
B1L100S, U17-ch77, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 83
Mean 41.81
Std Dev 3.816
Gaus mean : 42.5452
Gaus Width: 4.2240
Entry
ampl
0
2
4
6
8
10
0
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40
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60
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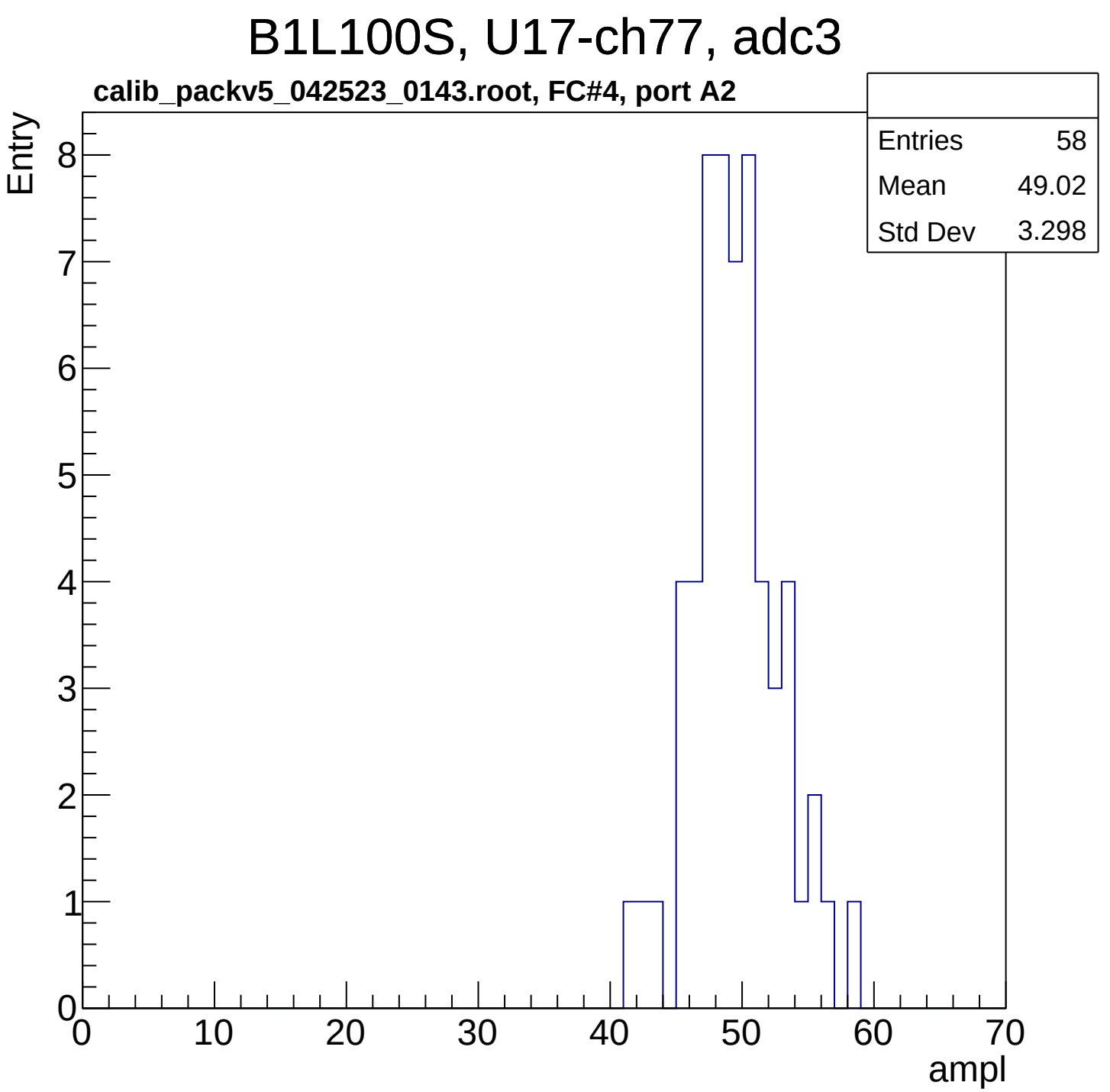
B1L100S, U17-ch77, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 49.02
Std Dev 3.298
Entry
ampl
0
1
2
3
4
5
6
7
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0
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40
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60
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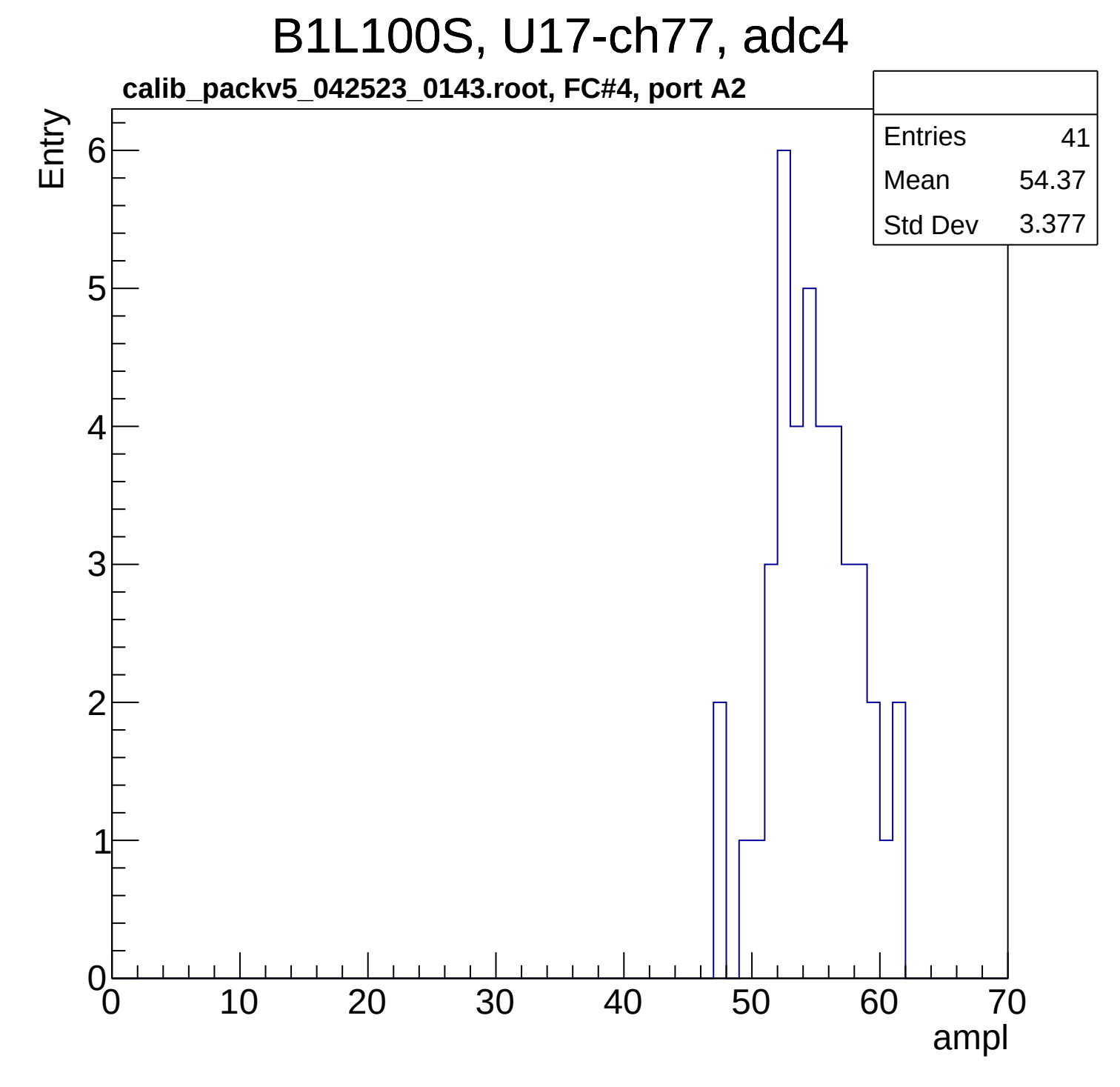
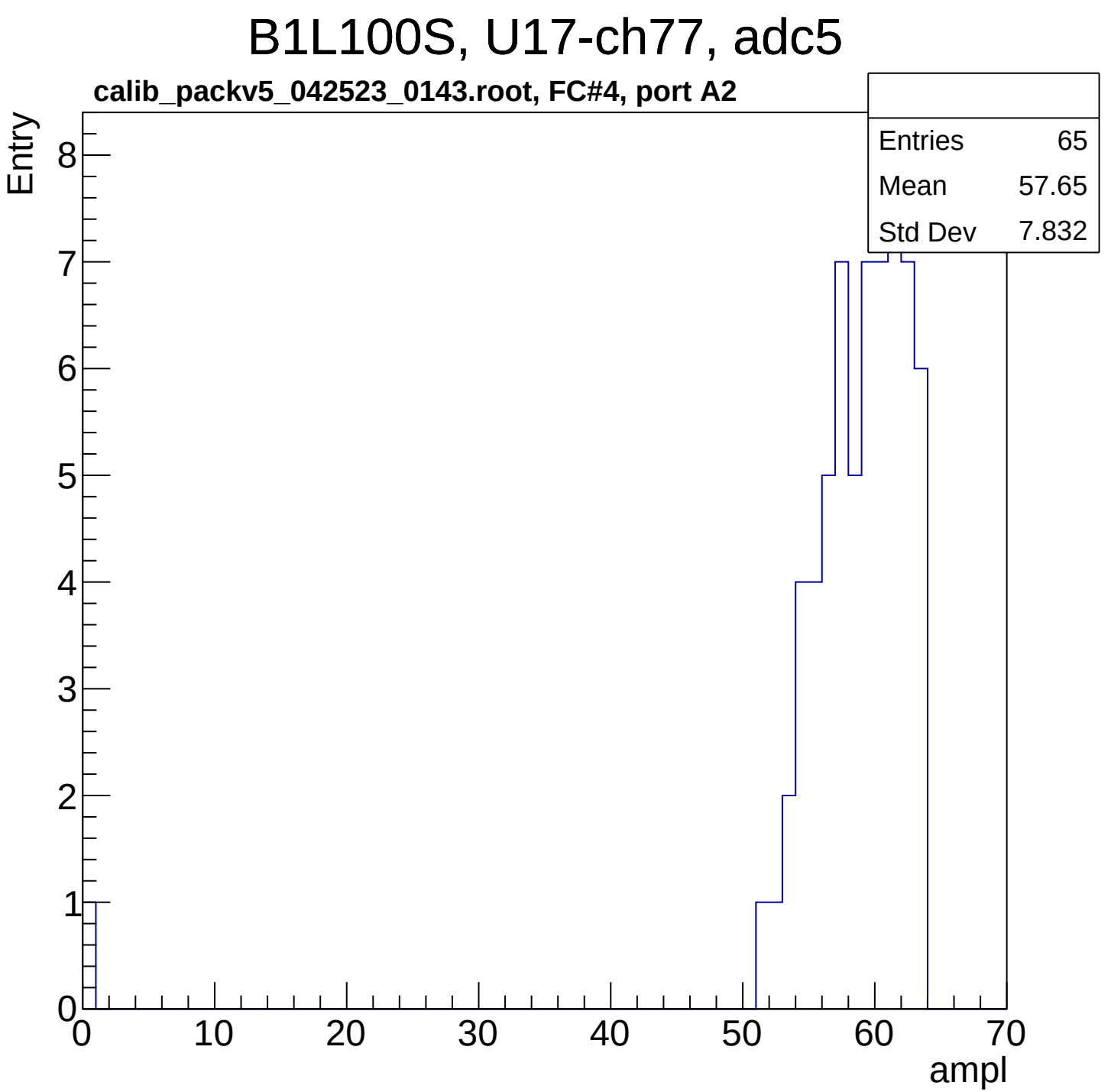
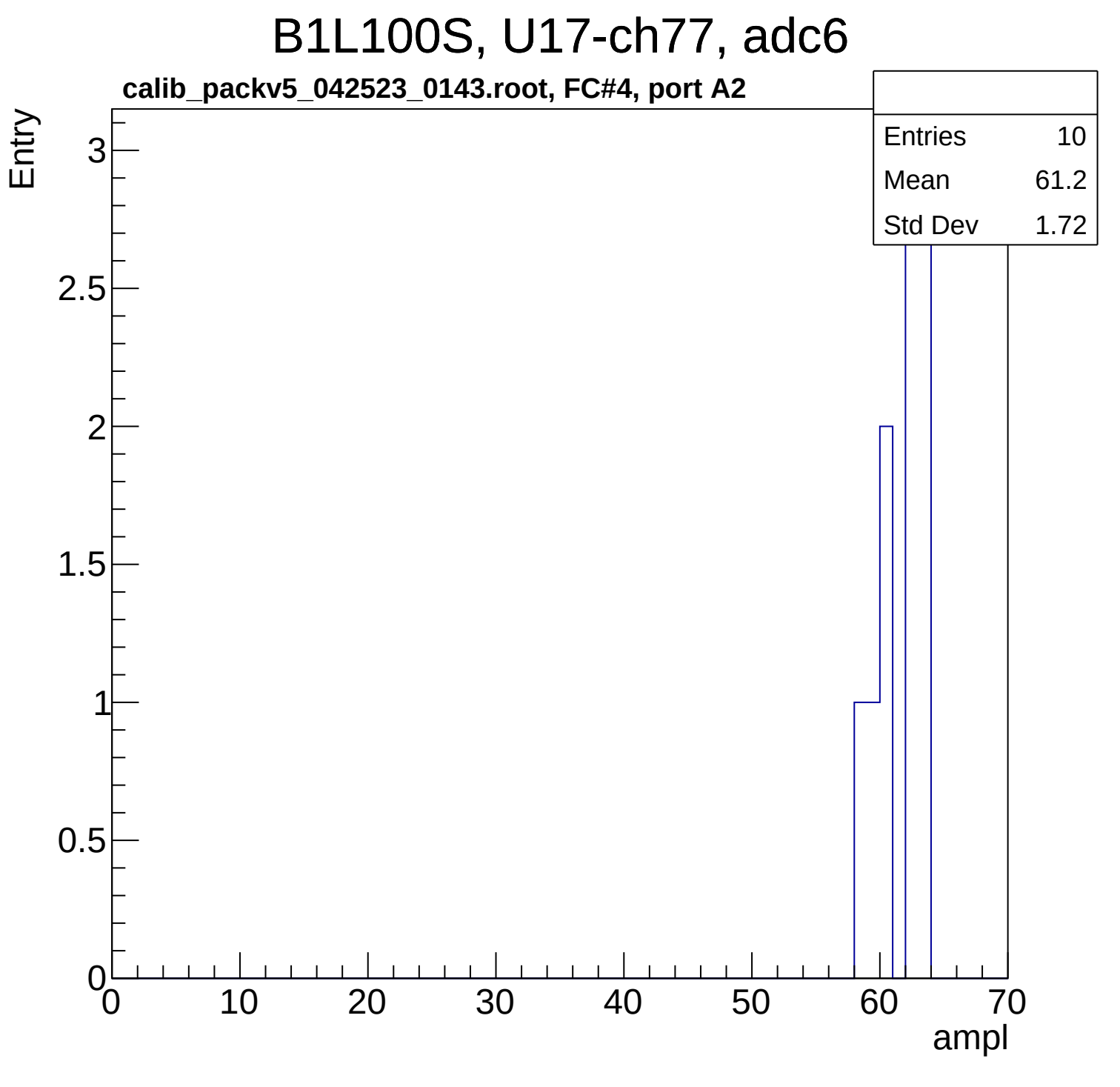
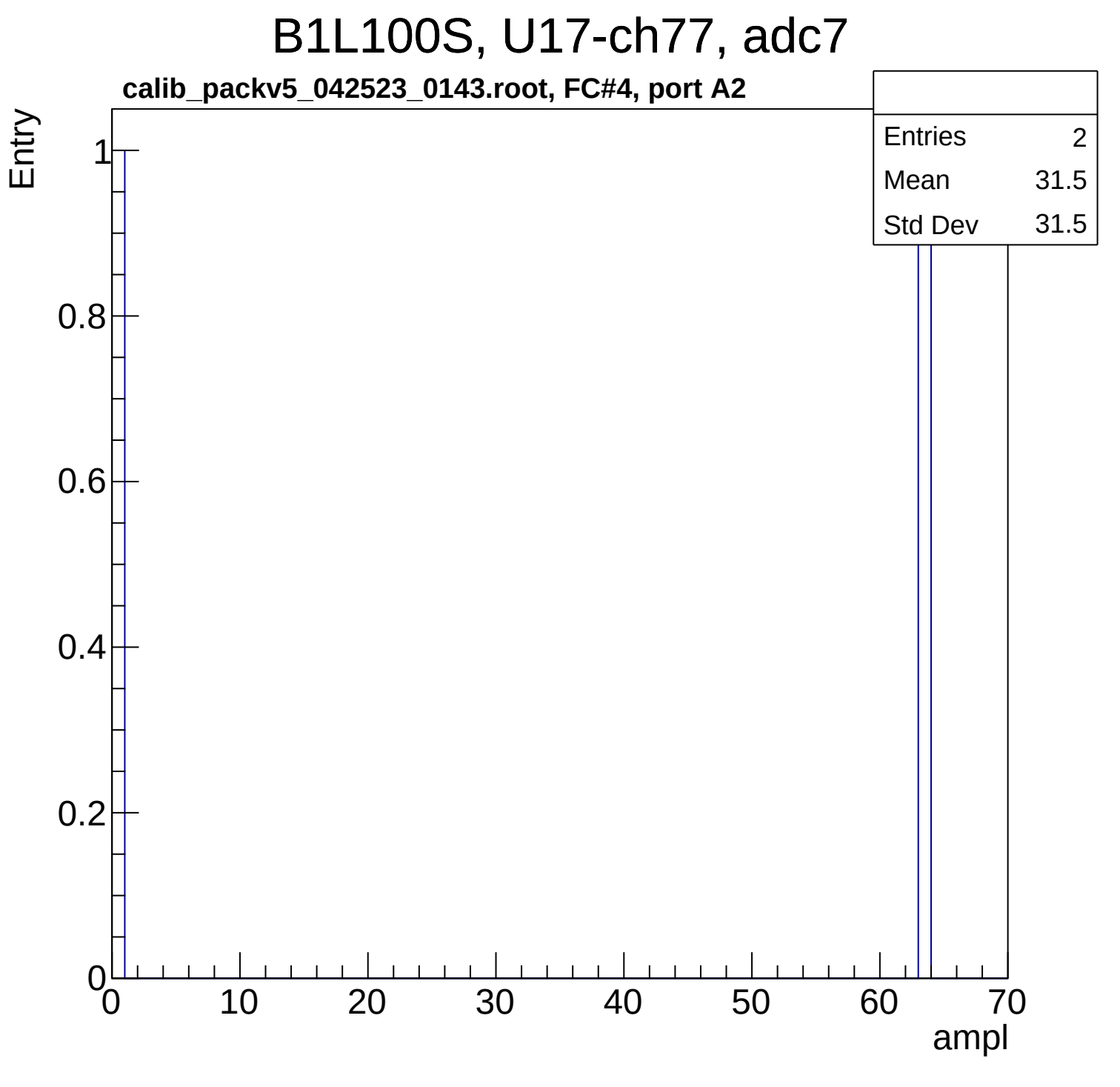
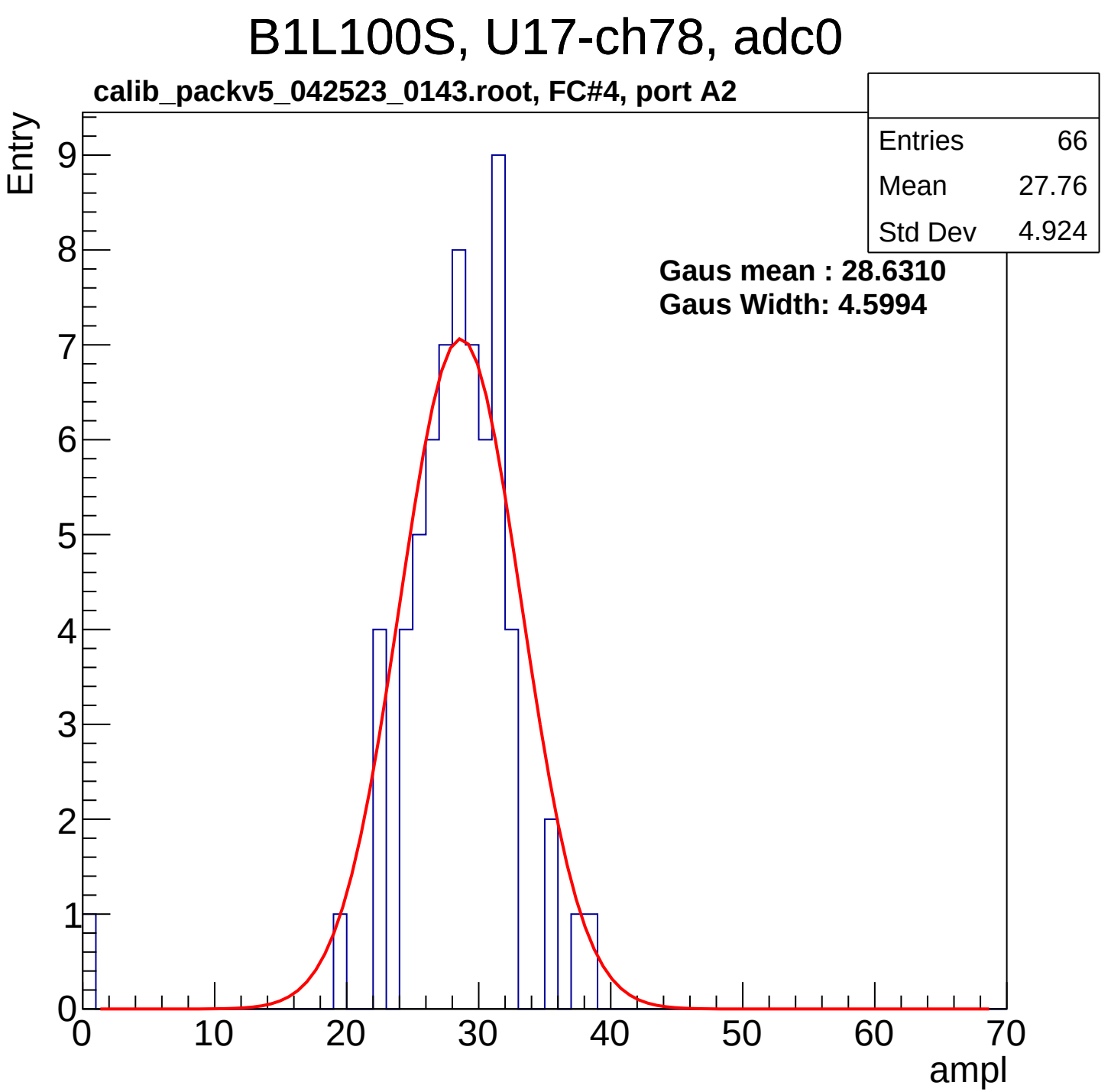
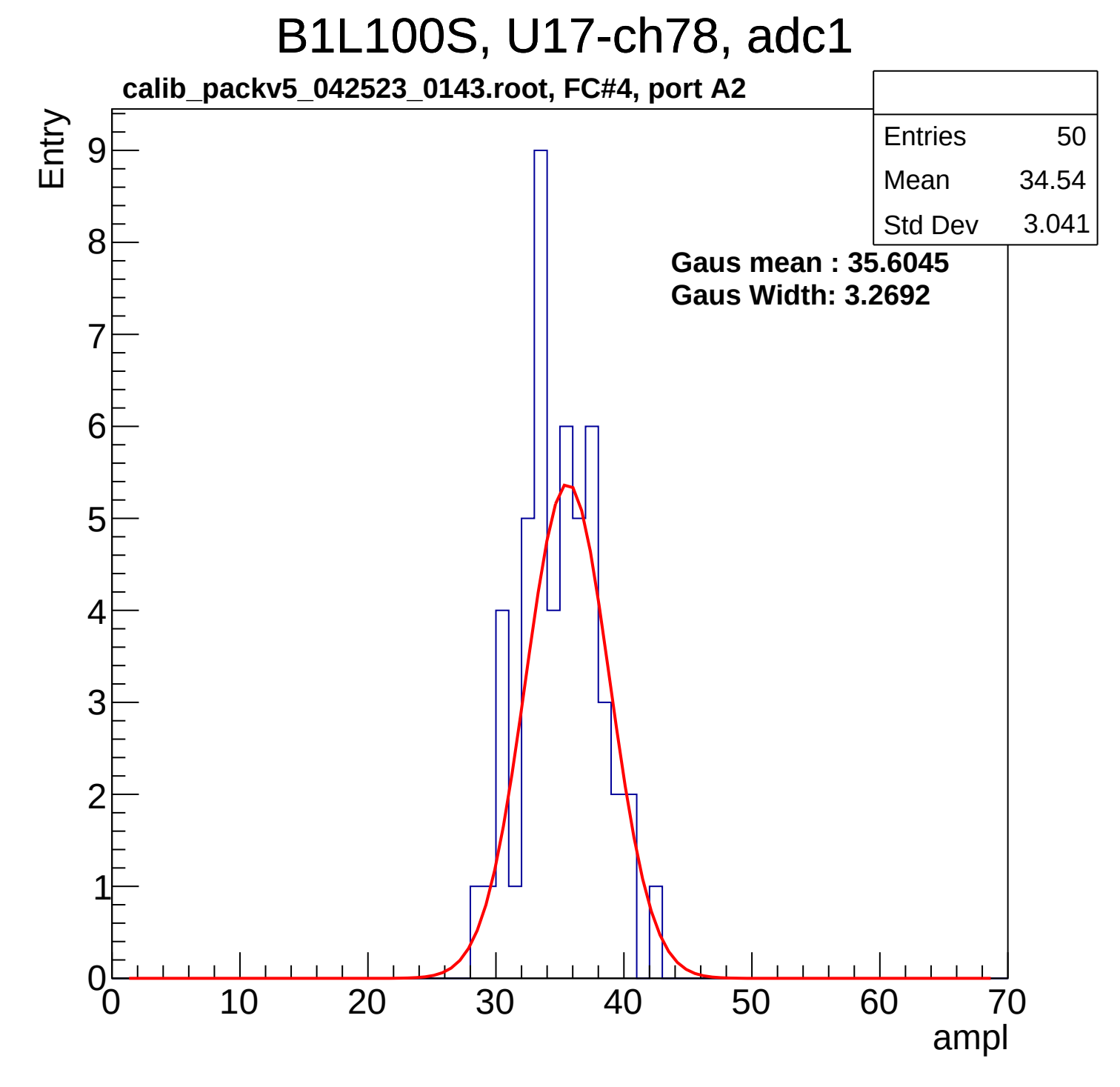

B1L100S, U17-ch77, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 41
Mean 54.37
Std Dev 3.377
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

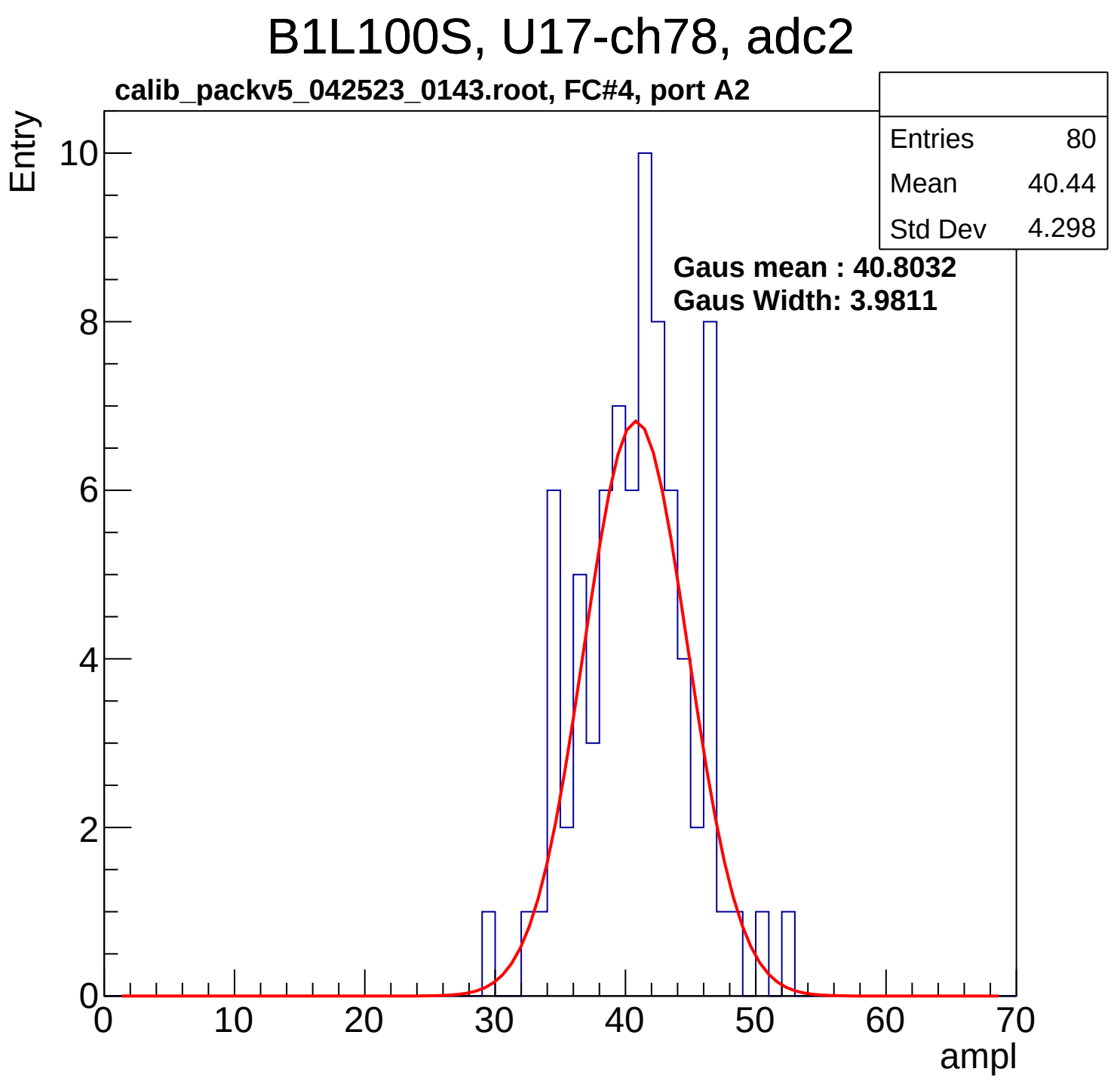

B1L100S, U17-ch77, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 57.65
Std Dev 7.832
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

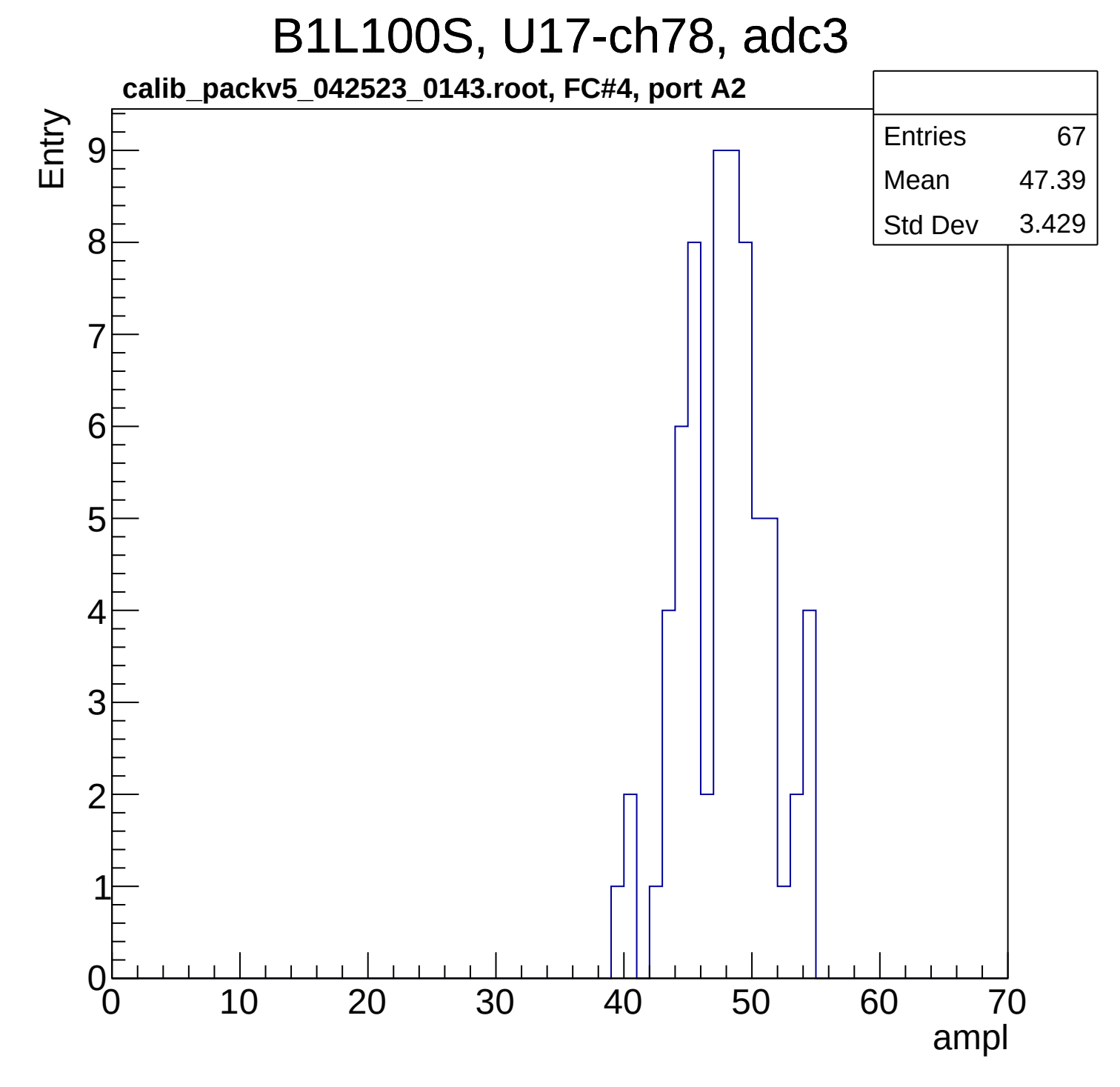

B1L100S, U17-ch77, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 10
Mean 61.2
Std Dev 1.72
Entry
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl

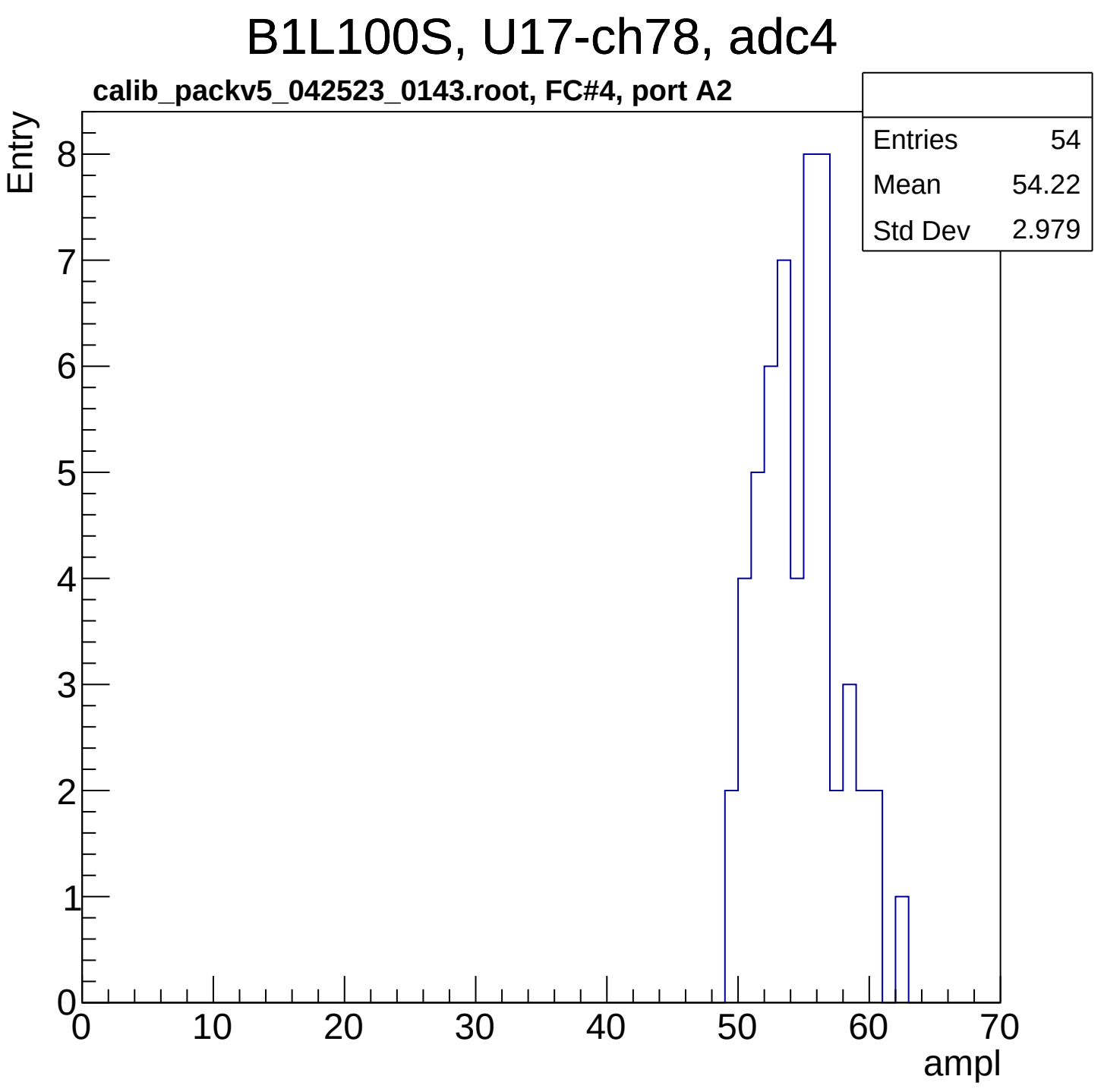

B1L100S, U17-ch77, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 31.5
Std Dev 31.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch78, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 27.76
Std Dev 4.924
Gaus mean : 28.6310
Gaus Width: 4.5994
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch78, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 34.54
Std Dev 3.041
Gaus mean : 35.6045
Gaus Width: 3.2692
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch78, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 80
Mean 40.44
Std Dev 4.298
Gaus mean : 40.8032
Gaus Width: 3.9811
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U17-ch78, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 47.39
Std Dev 3.429
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch78, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 54.22
Std Dev 2.979
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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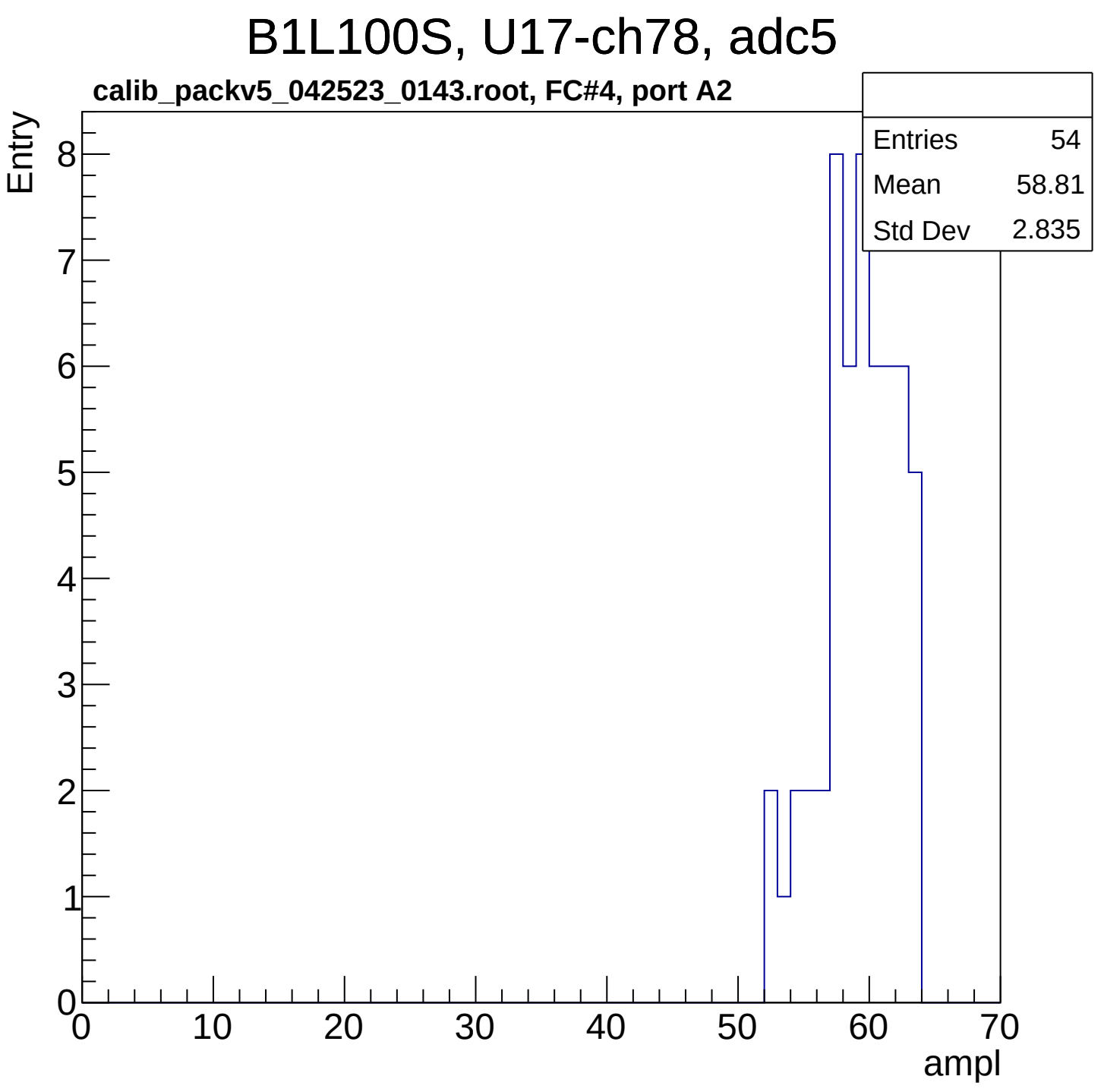
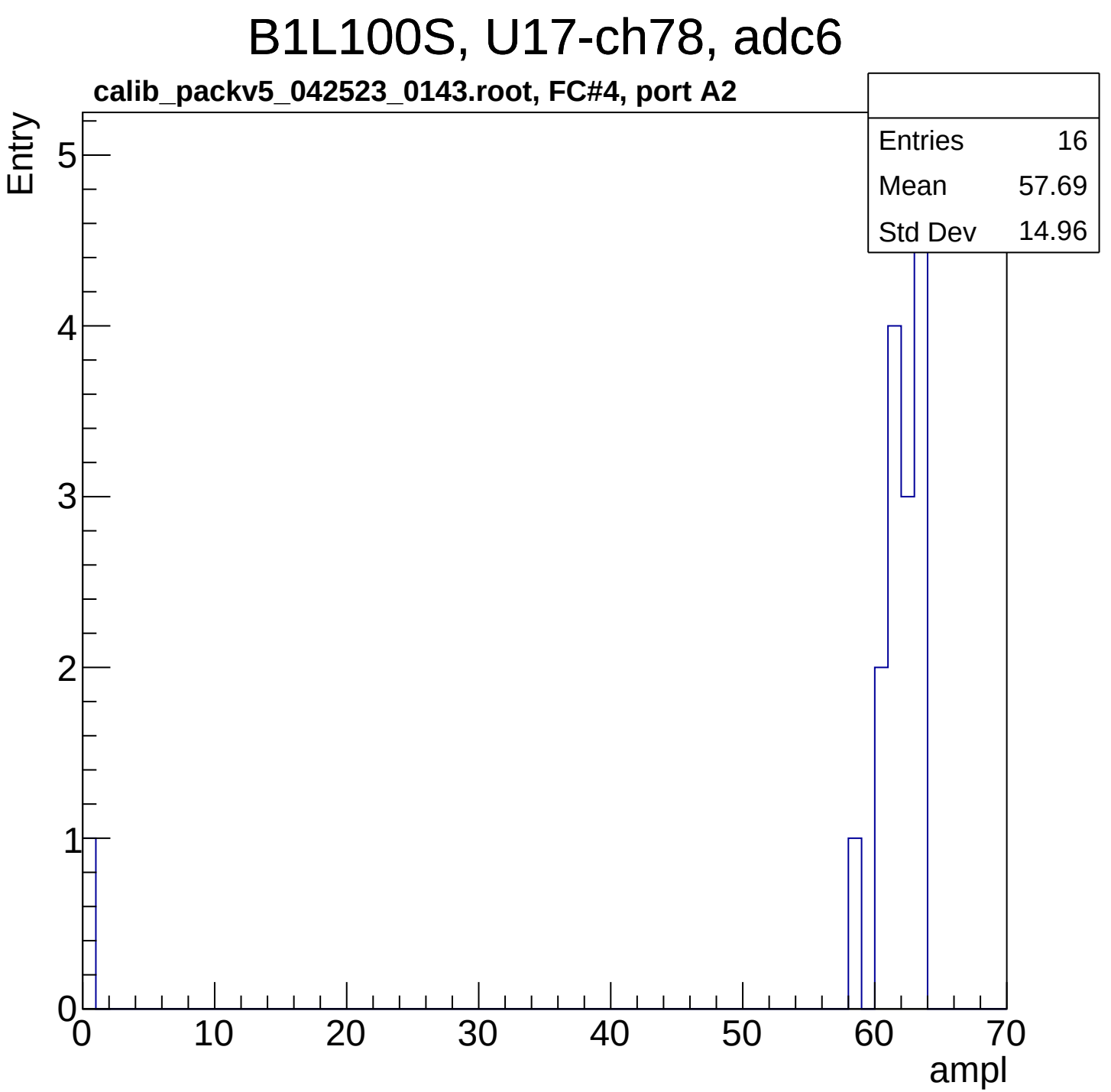
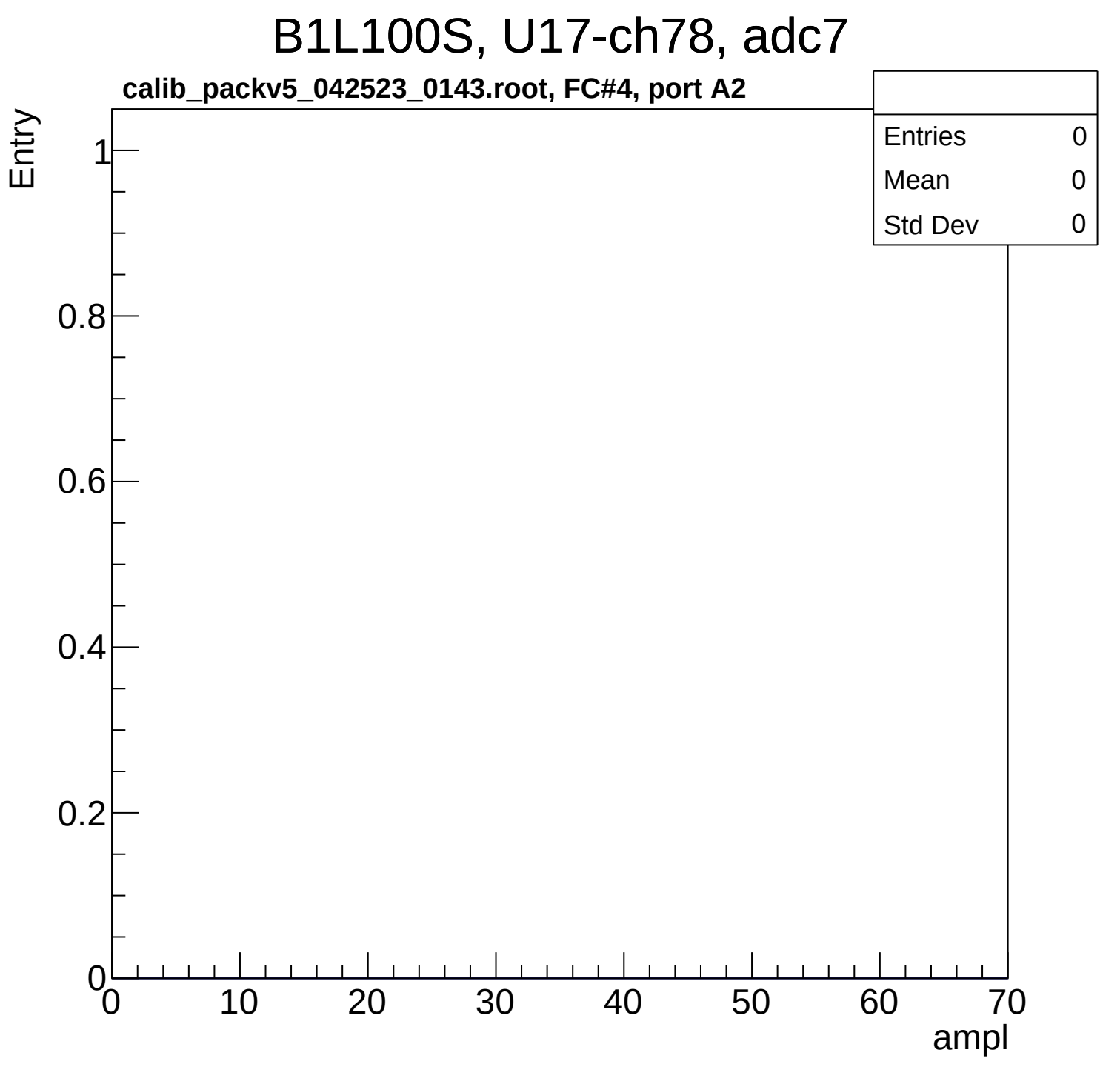
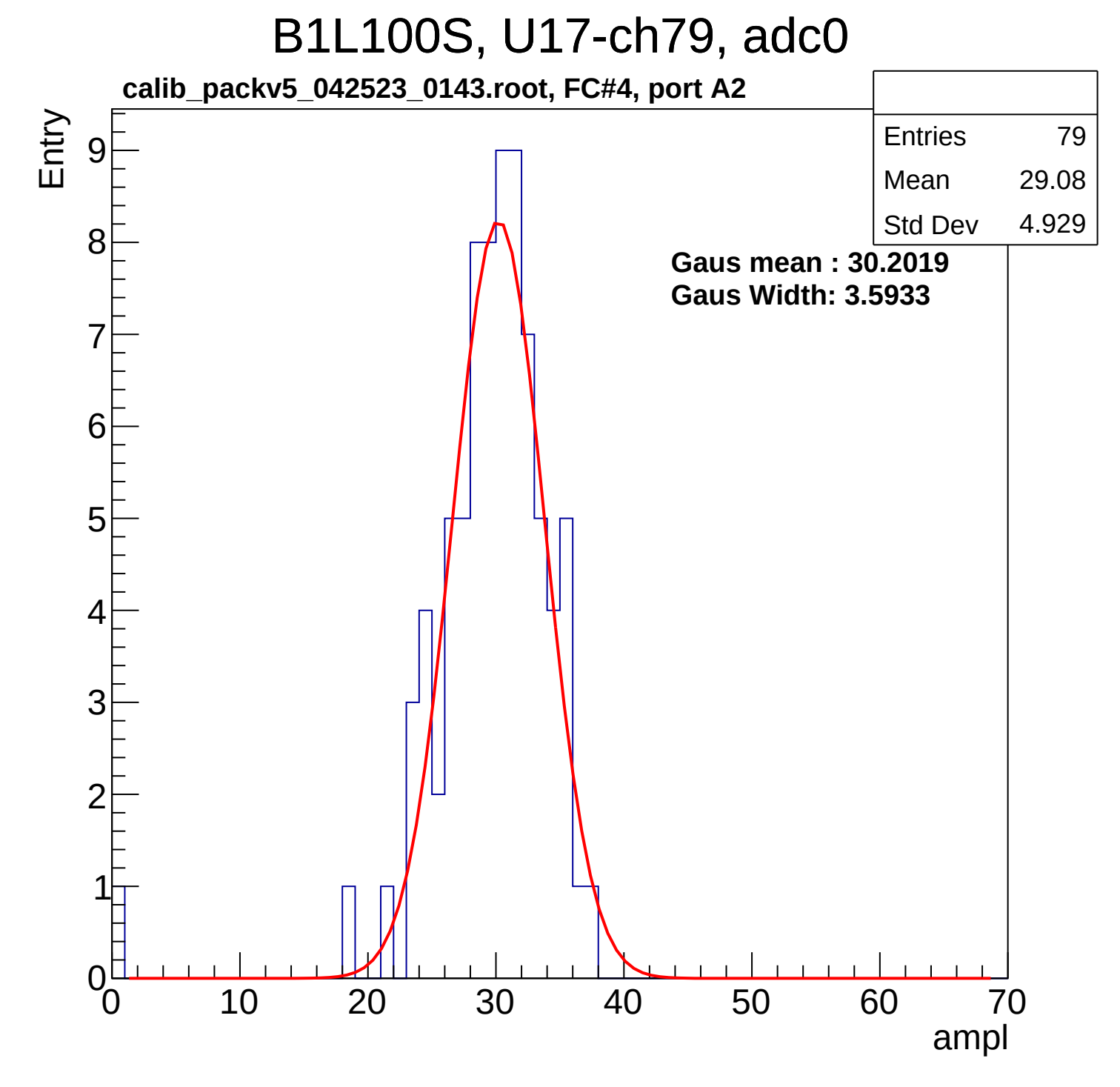
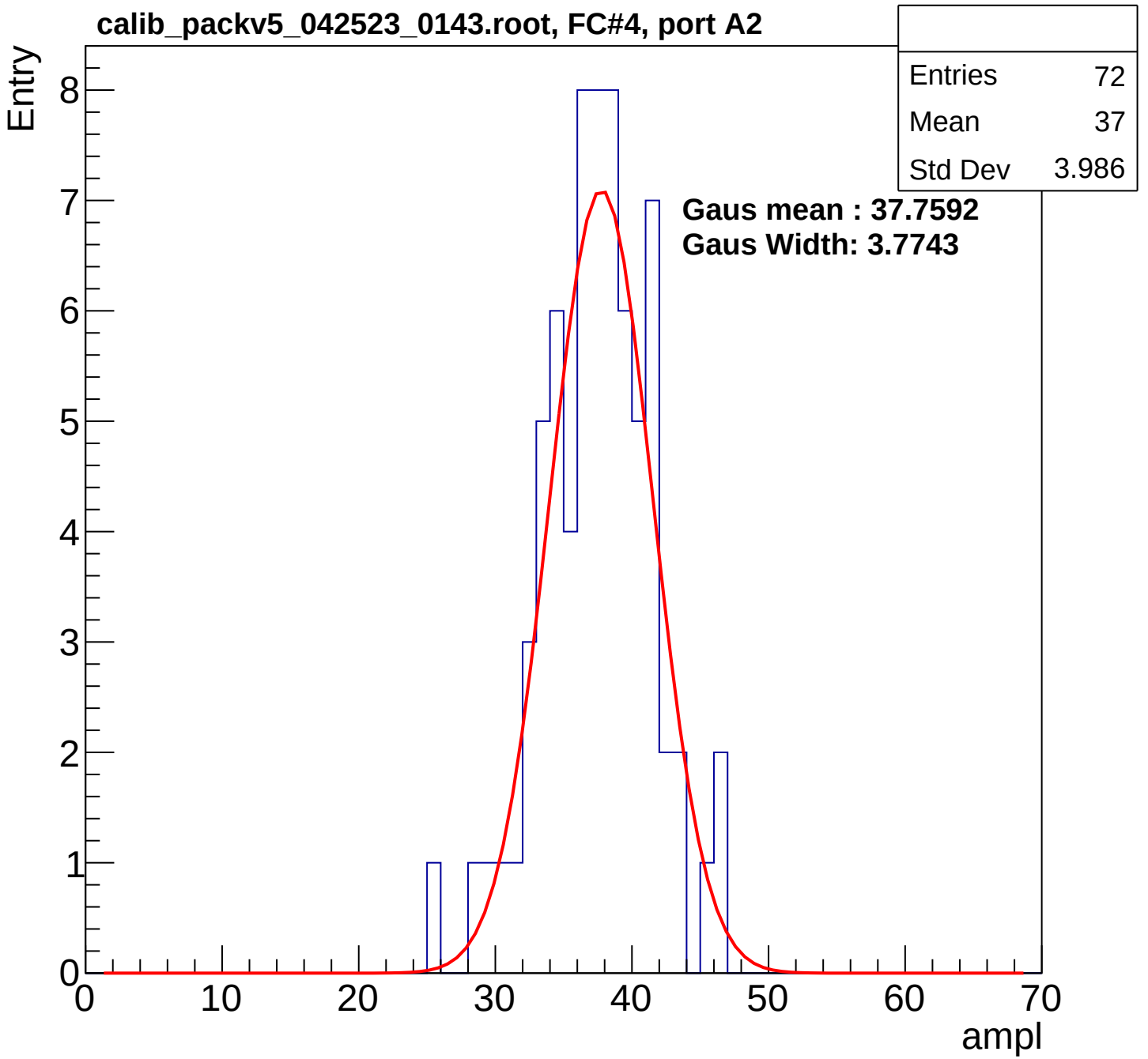
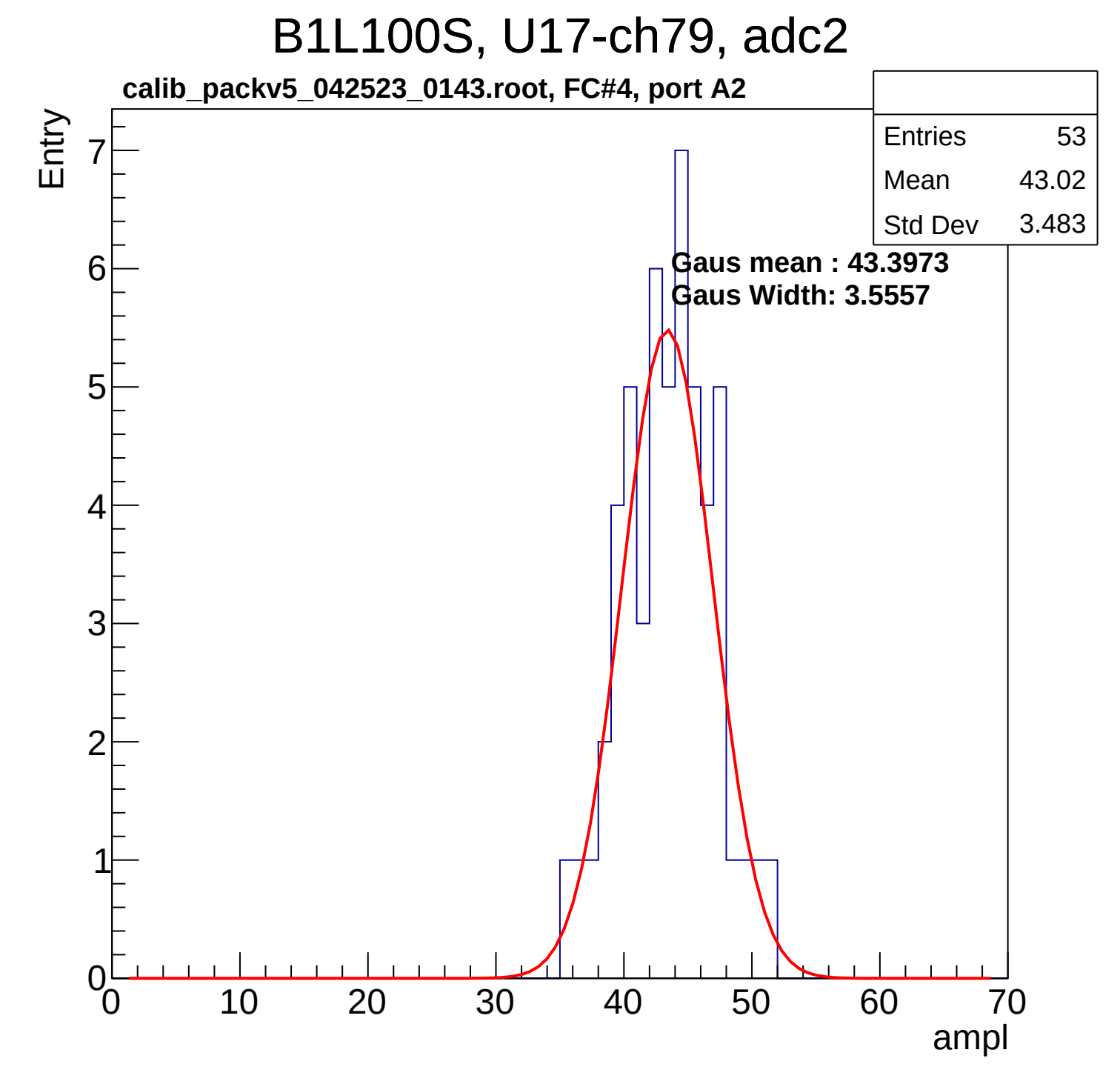

B1L100S, U17-ch78, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 58.81
Std Dev 2.835
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

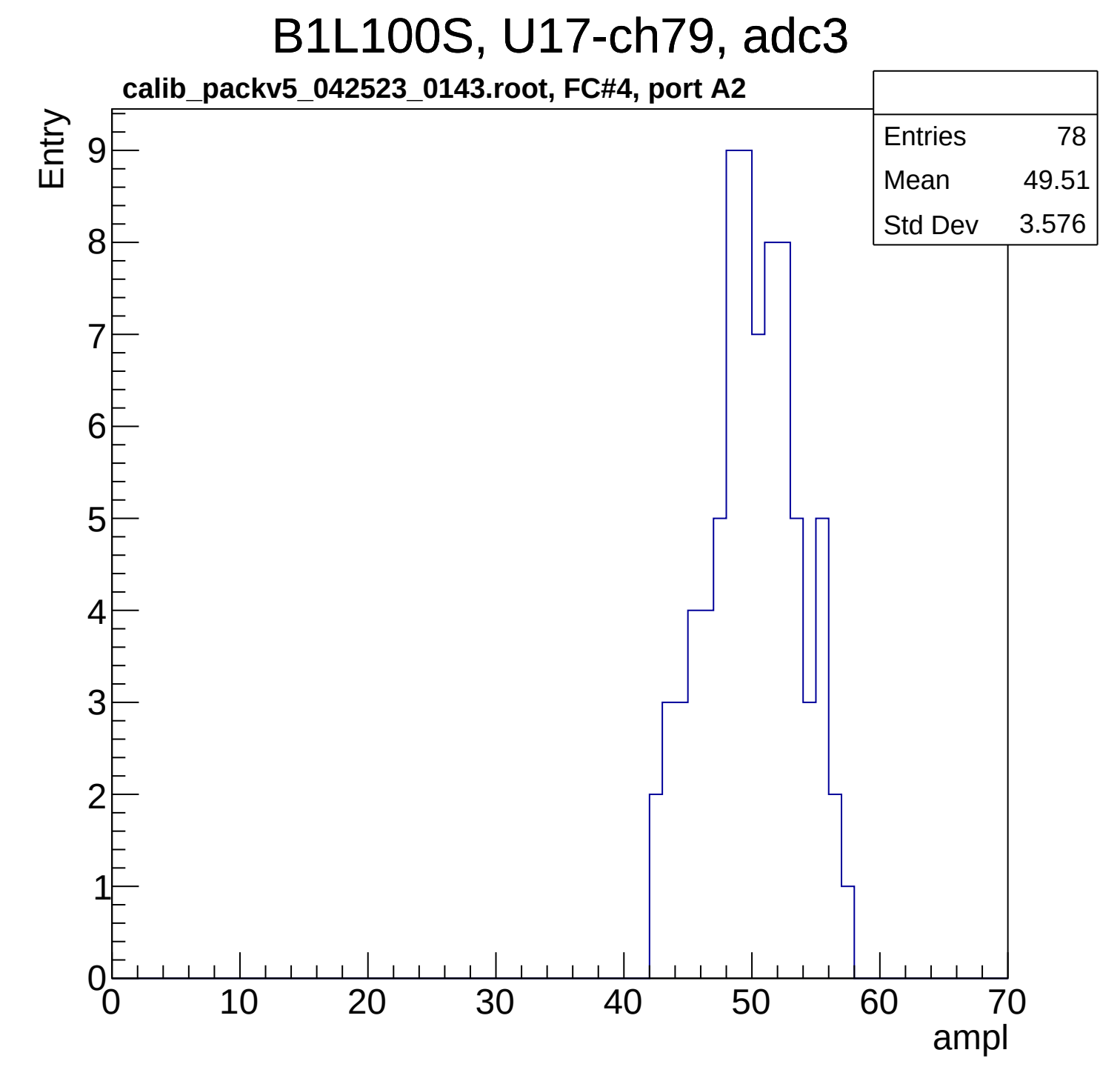

B1L100S, U17-ch78, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 16
Mean 57.69
Std Dev 14.96
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch78, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch79, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 79
Mean 29.08
Std Dev 4.929
Gaus mean : 30.2019
Gaus Width: 3.5933
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch79, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 37
Std Dev 3.986
Gaus mean : 37.7592
Gaus Width: 3.7743
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch79, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 43.02
Std Dev 3.483
Gaus mean : 43.3973
Gaus Width: 3.5557
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U17-ch79, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 78
Mean 49.51
Std Dev 3.576
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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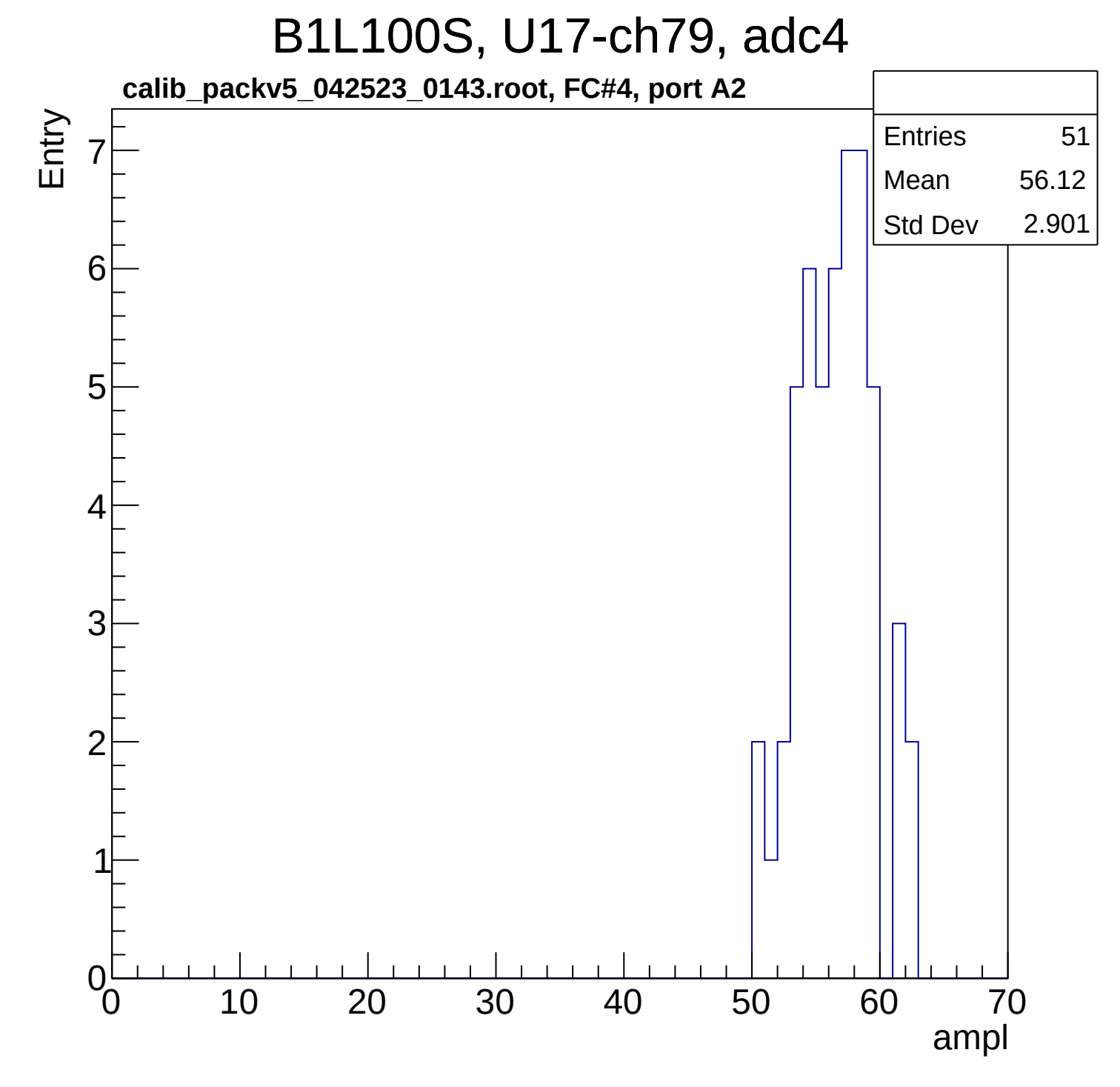
B1L100S, U17-ch79, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 56.12
Std Dev 2.901
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
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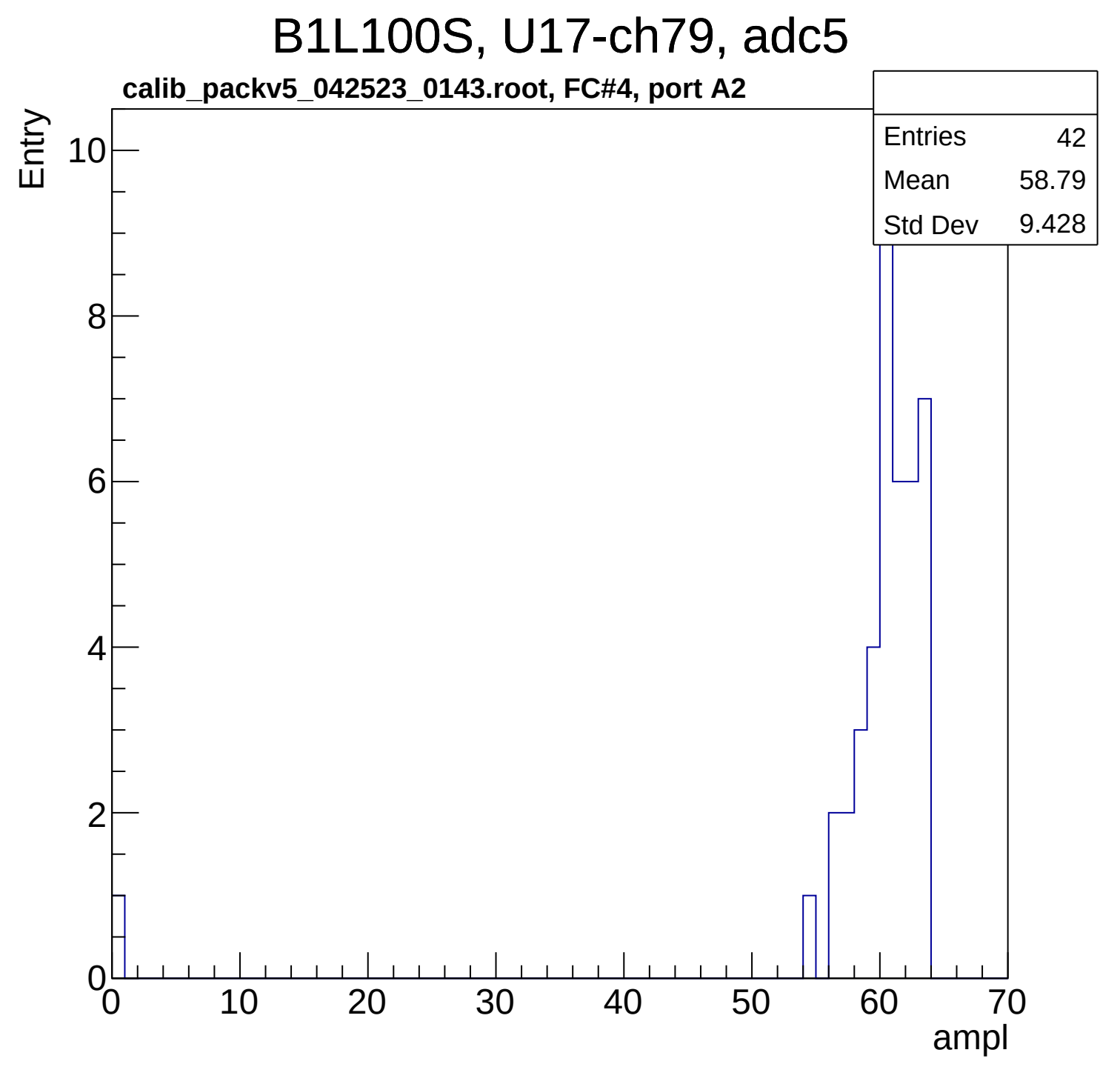
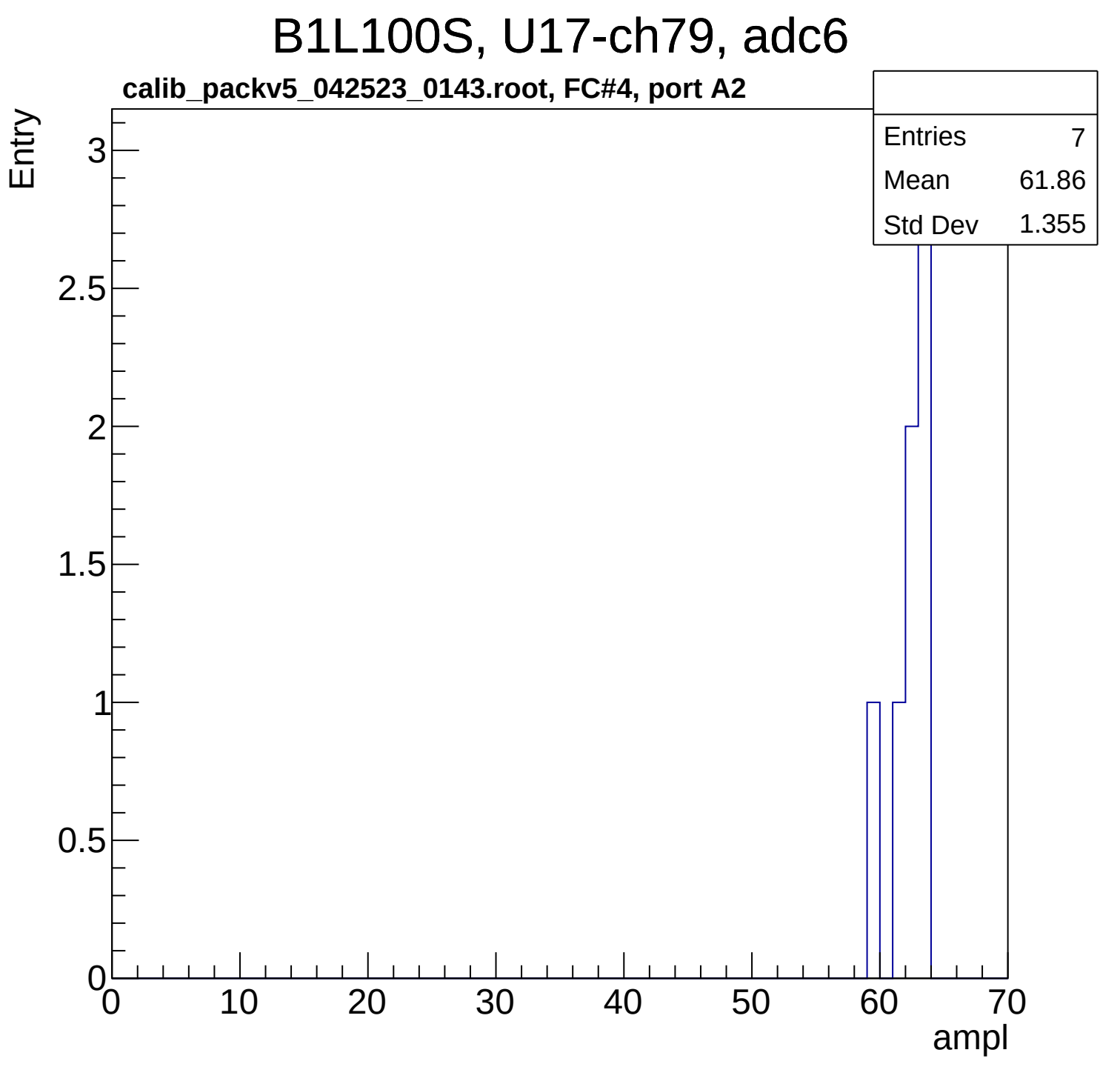
40
50
60
70


B1L100S, U17-ch79, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 42
Mean 58.79
Std Dev 9.428
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U17-ch79, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 7
Mean 61.86
Std Dev 1.355
Entry
ampl
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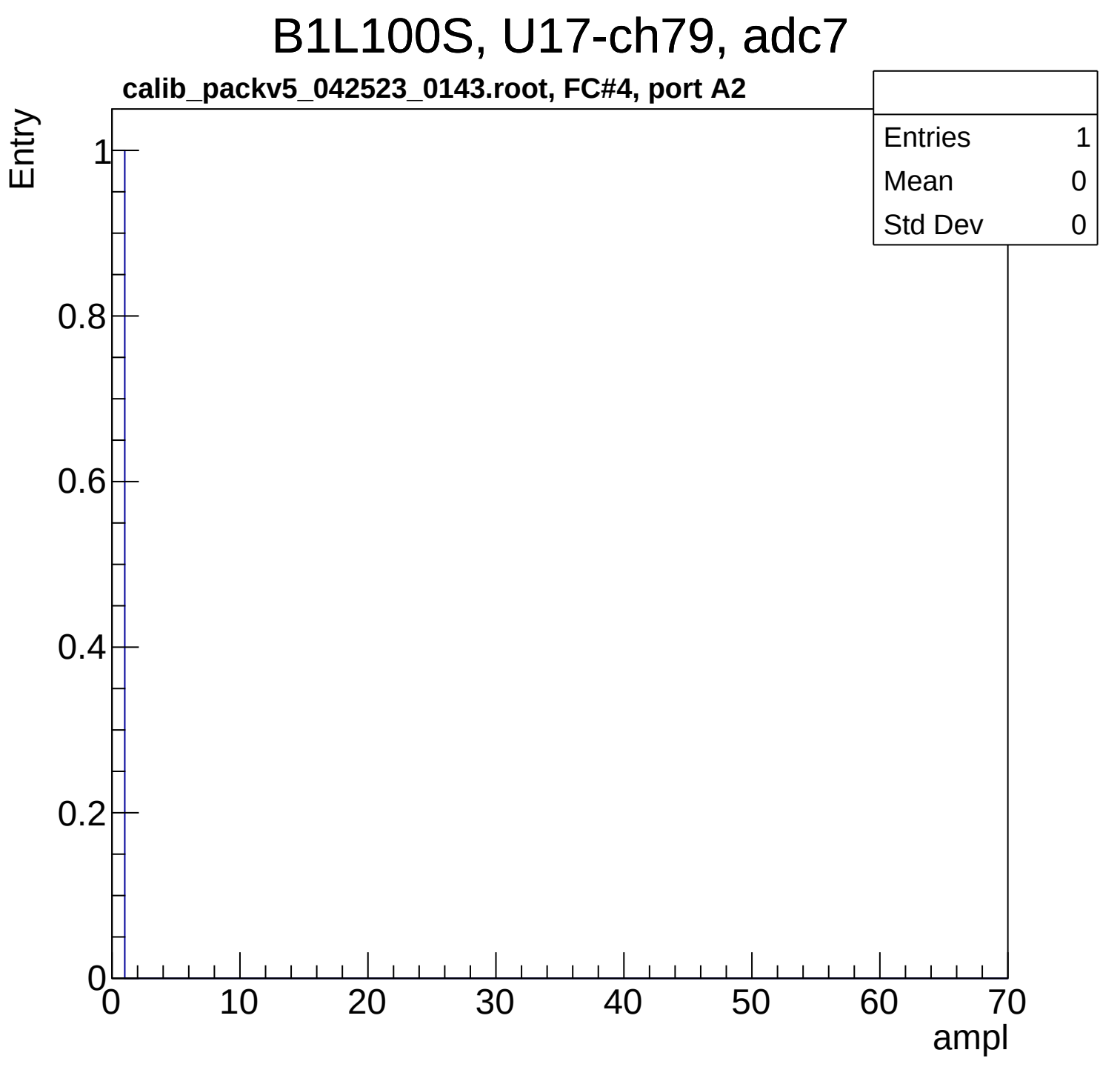
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L100S, U17-ch79, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
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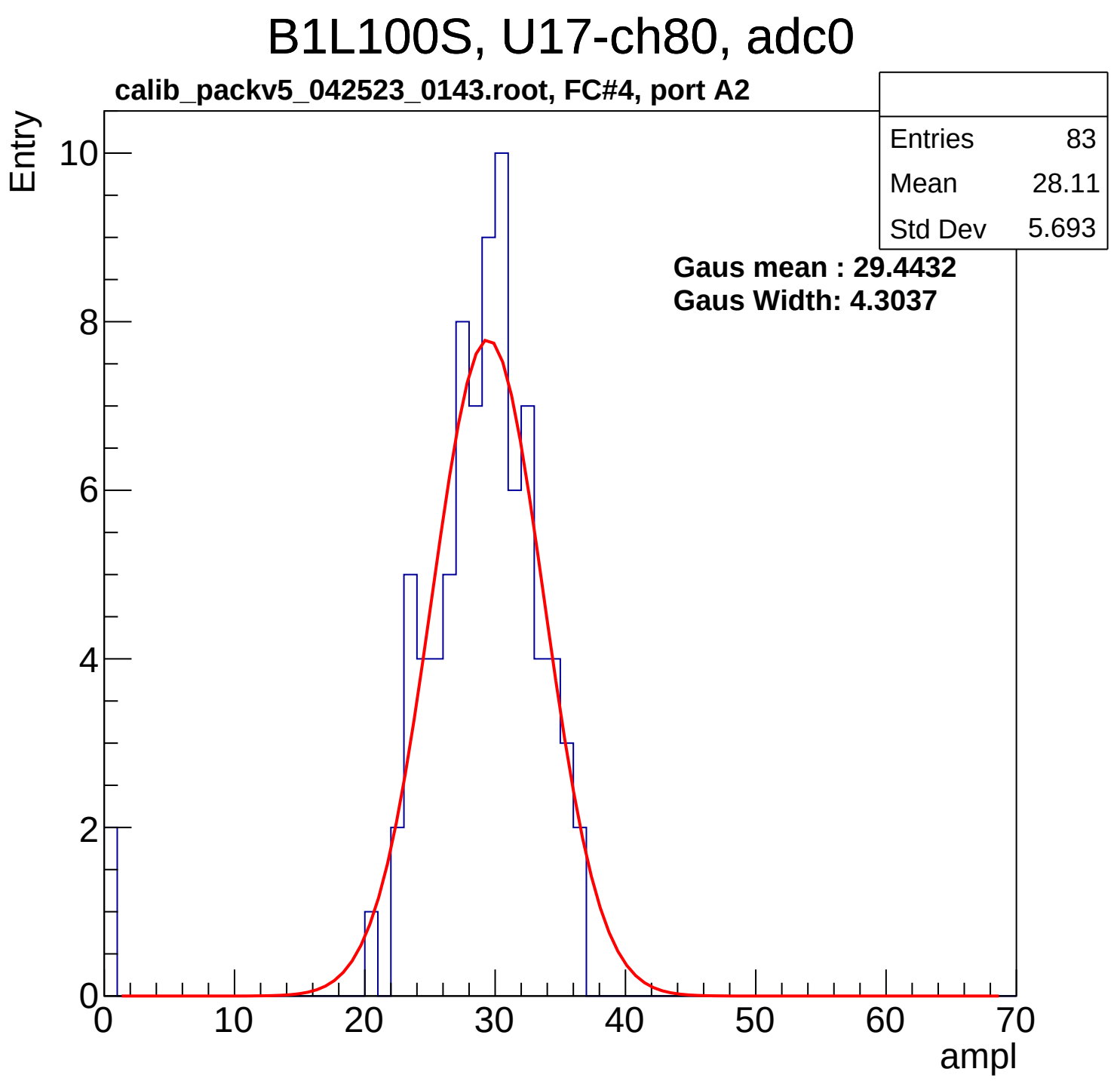
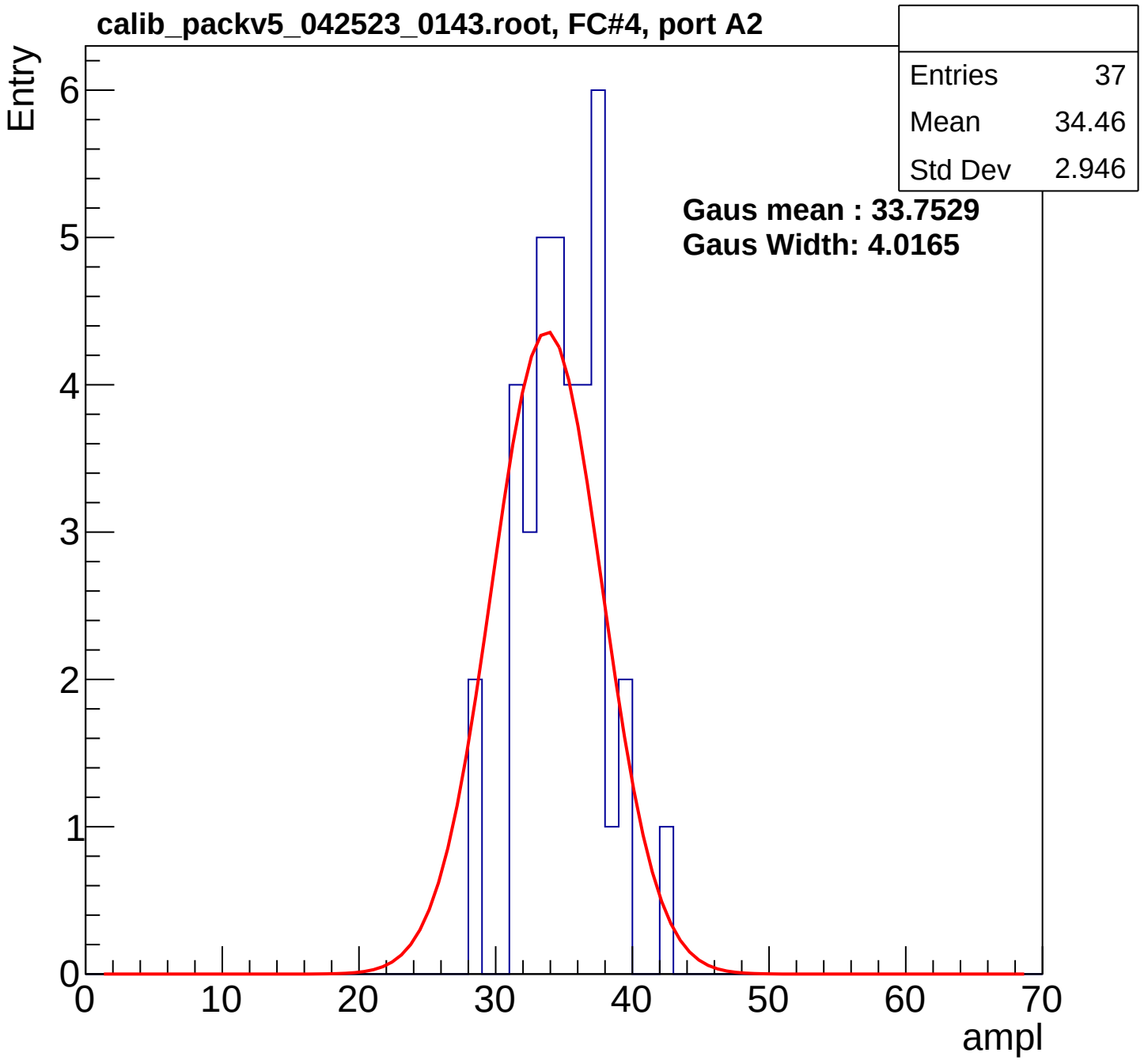
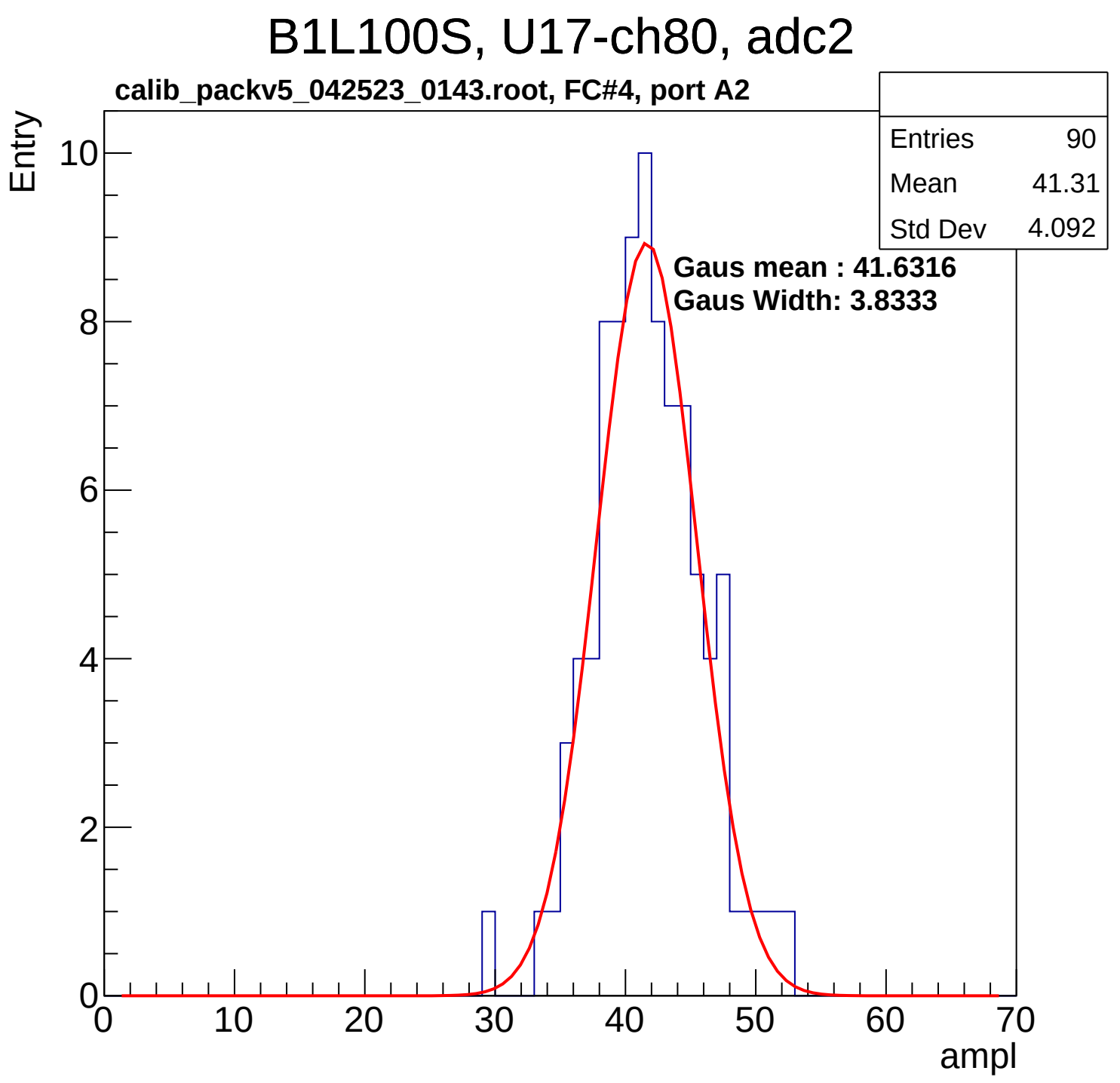
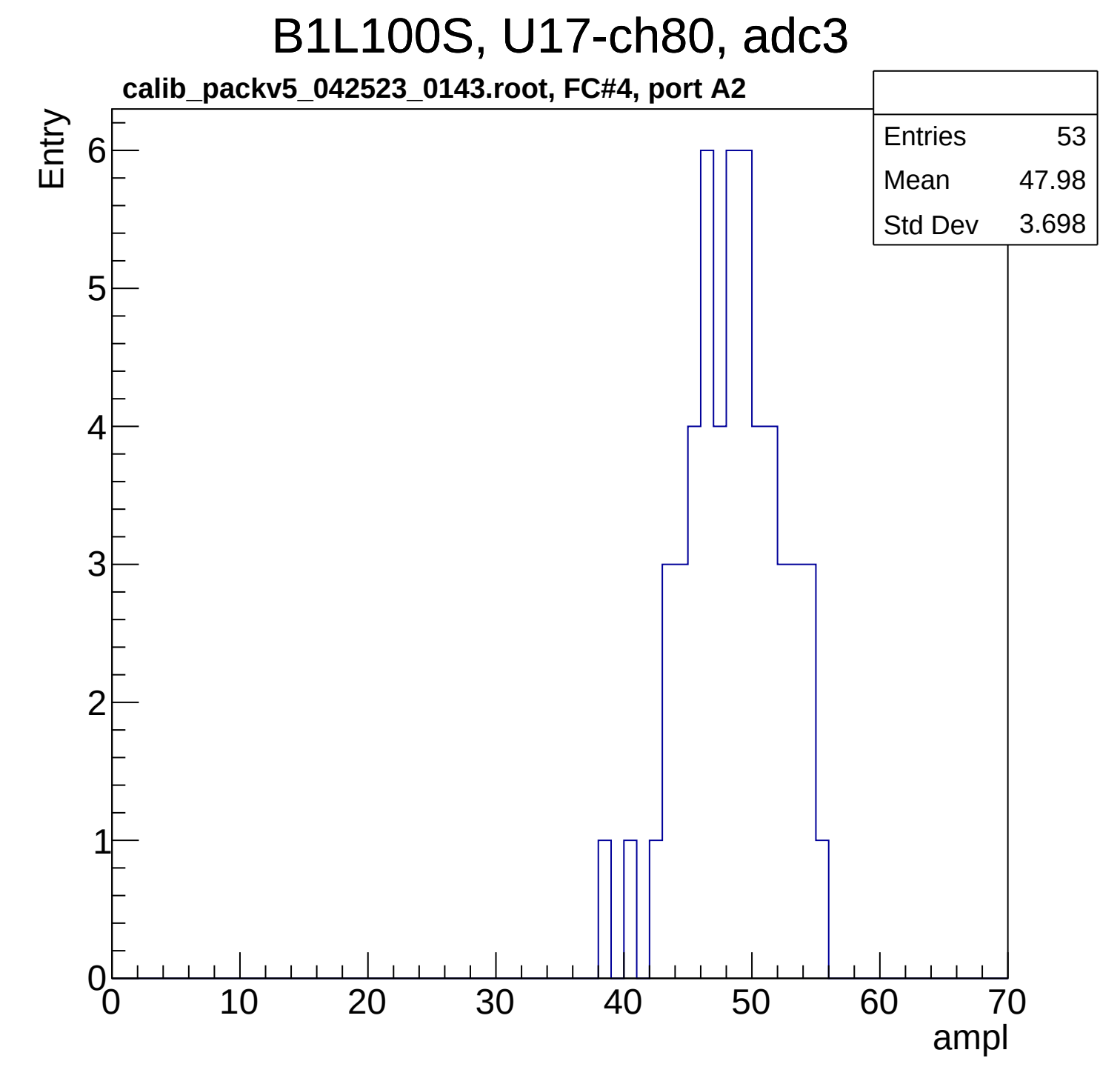
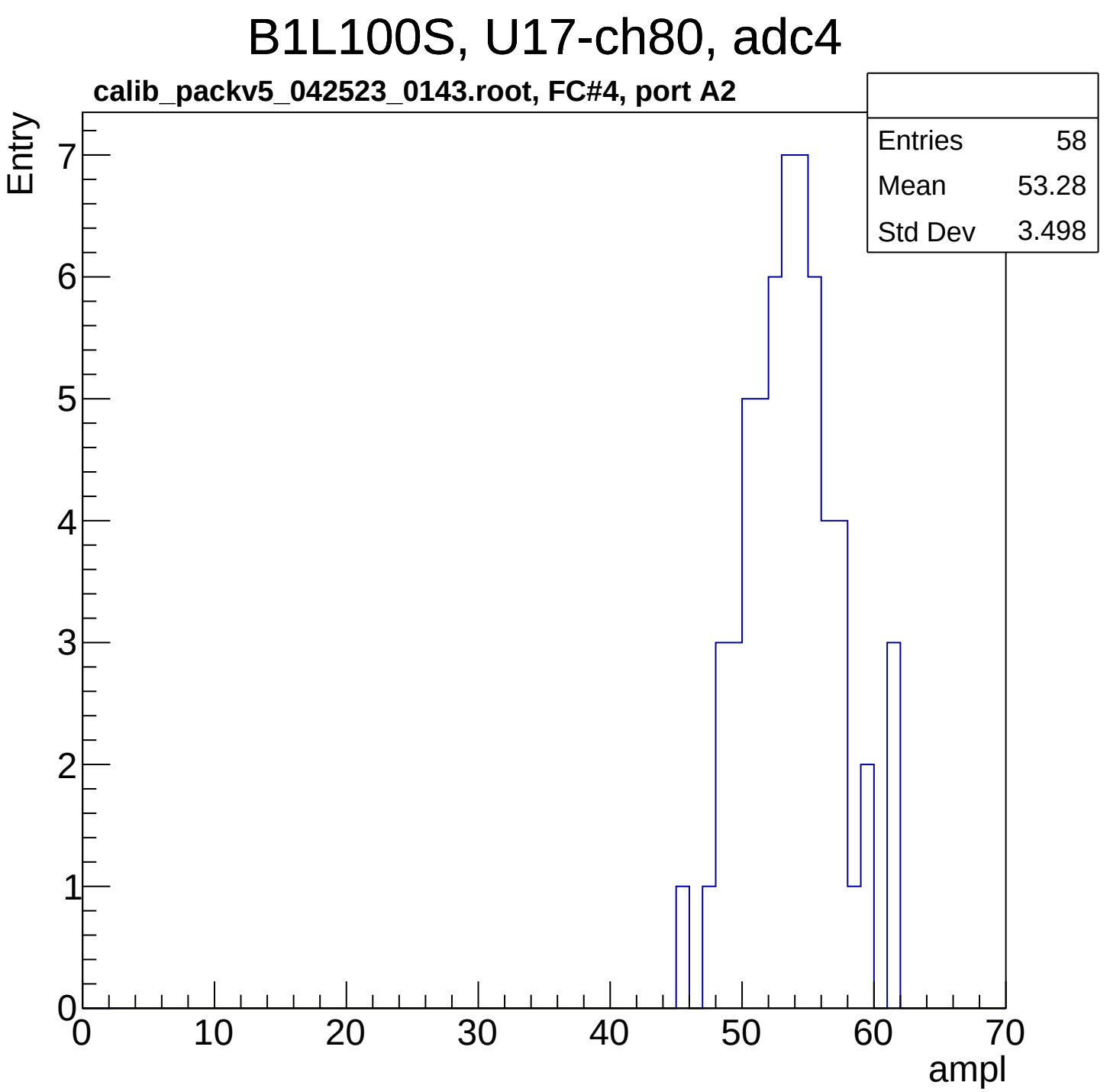
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

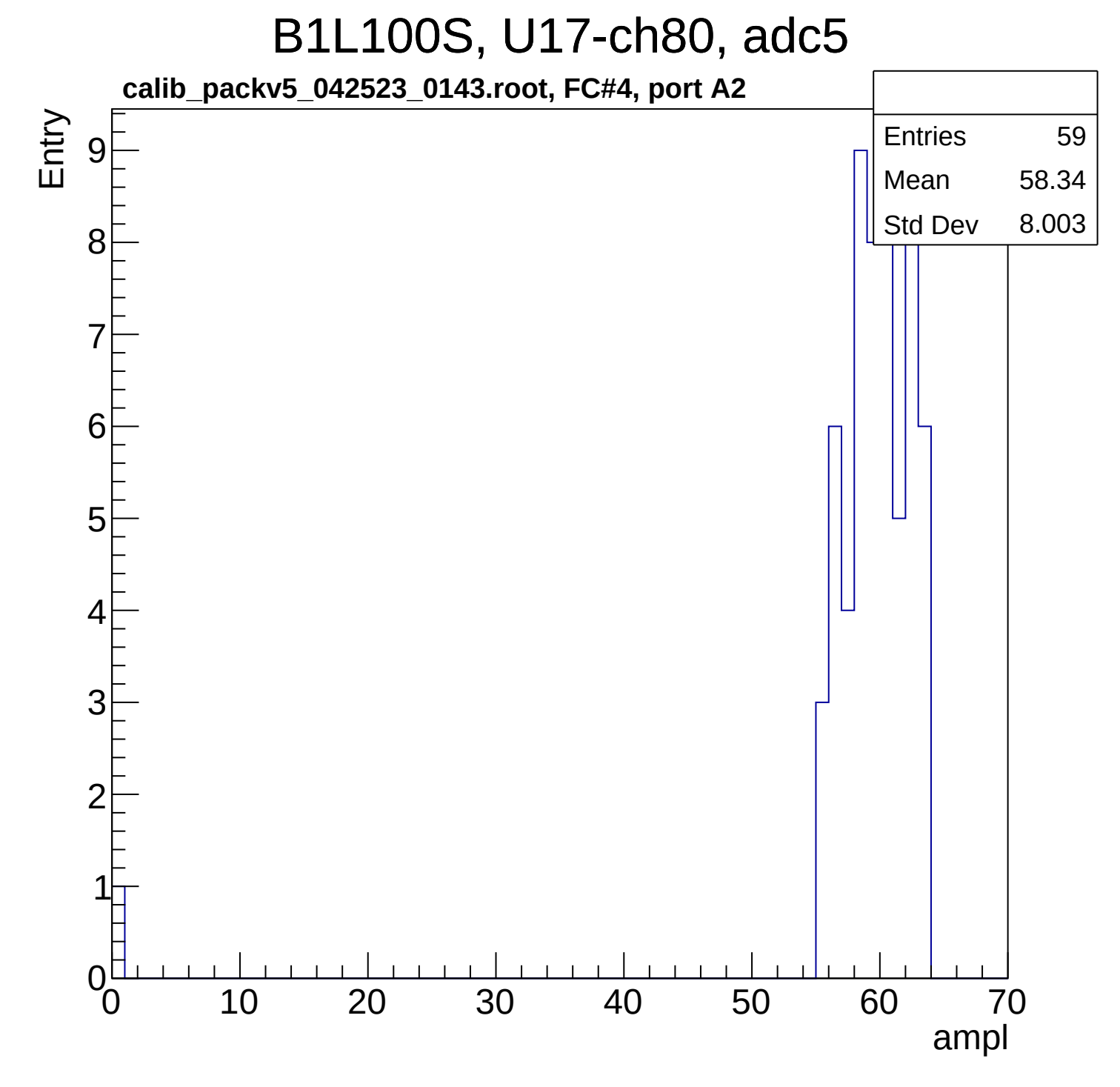

B1L100S, U17-ch80, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 83
Mean 28.11
Std Dev 5.693
Gaus mean : 29.4432
Gaus Width: 4.3037
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U17-ch80, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 37
Mean 34.46
Std Dev 2.946
Gaus mean : 33.7529
Gaus Width: 4.0165
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L100S, U17-ch80, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 90
Mean 41.31
Std Dev 4.092
Gaus mean : 41.6316
Gaus Width: 3.8333
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U17-ch80, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 47.98
Std Dev 3.698
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L100S, U17-ch80, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 53.28
Std Dev 3.498
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U17-ch80, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 58.34
Std Dev 8.003
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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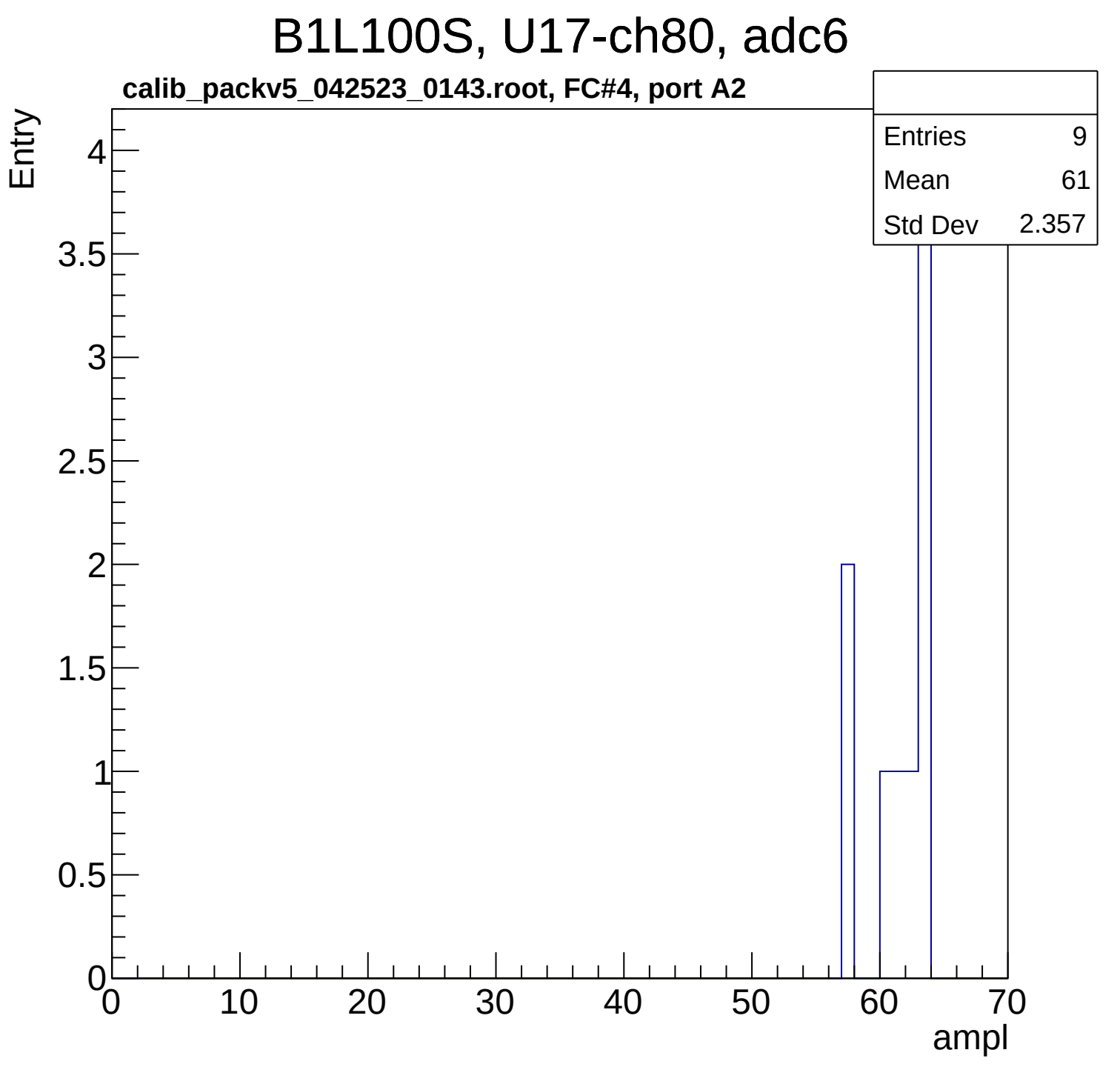
B1L100S, U17-ch80, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 9
Mean 61
Std Dev 2.357
Entry
ampl
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0.5
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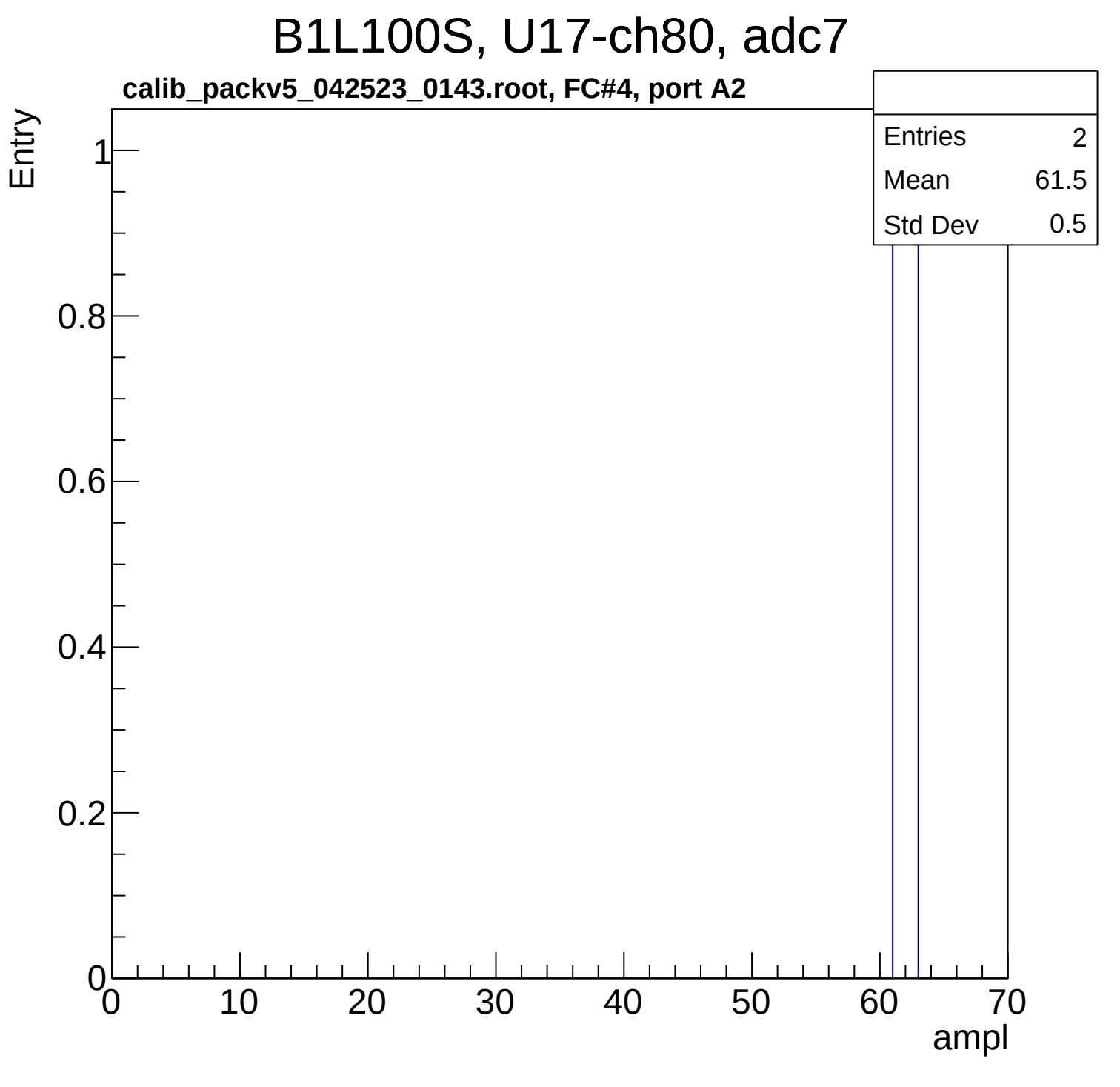
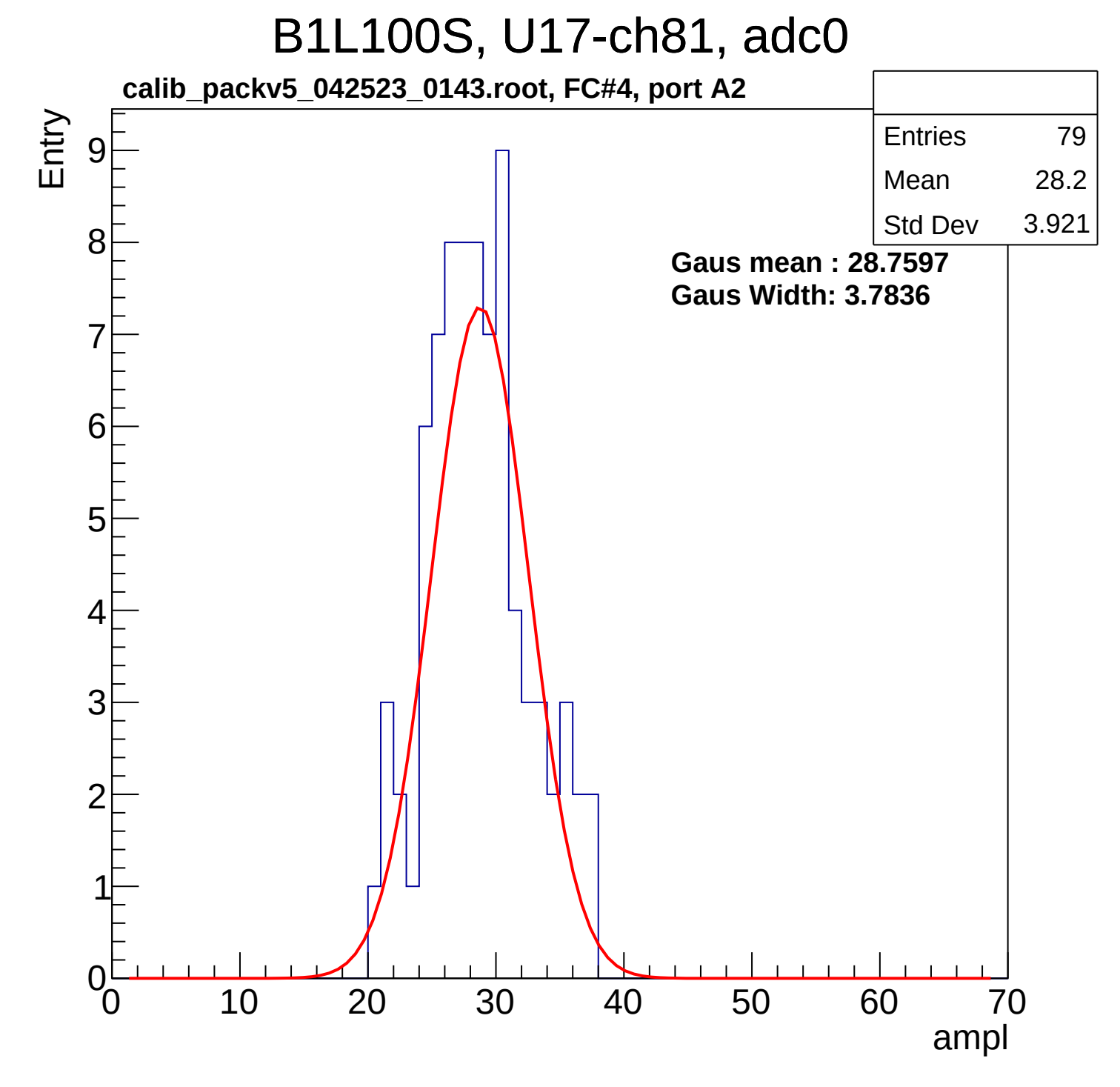
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L100S, U17-ch80, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 61.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch81, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 79
Mean 28.2
Std Dev 3.921
Gaus mean : 28.7597
Gaus Width: 3.7836
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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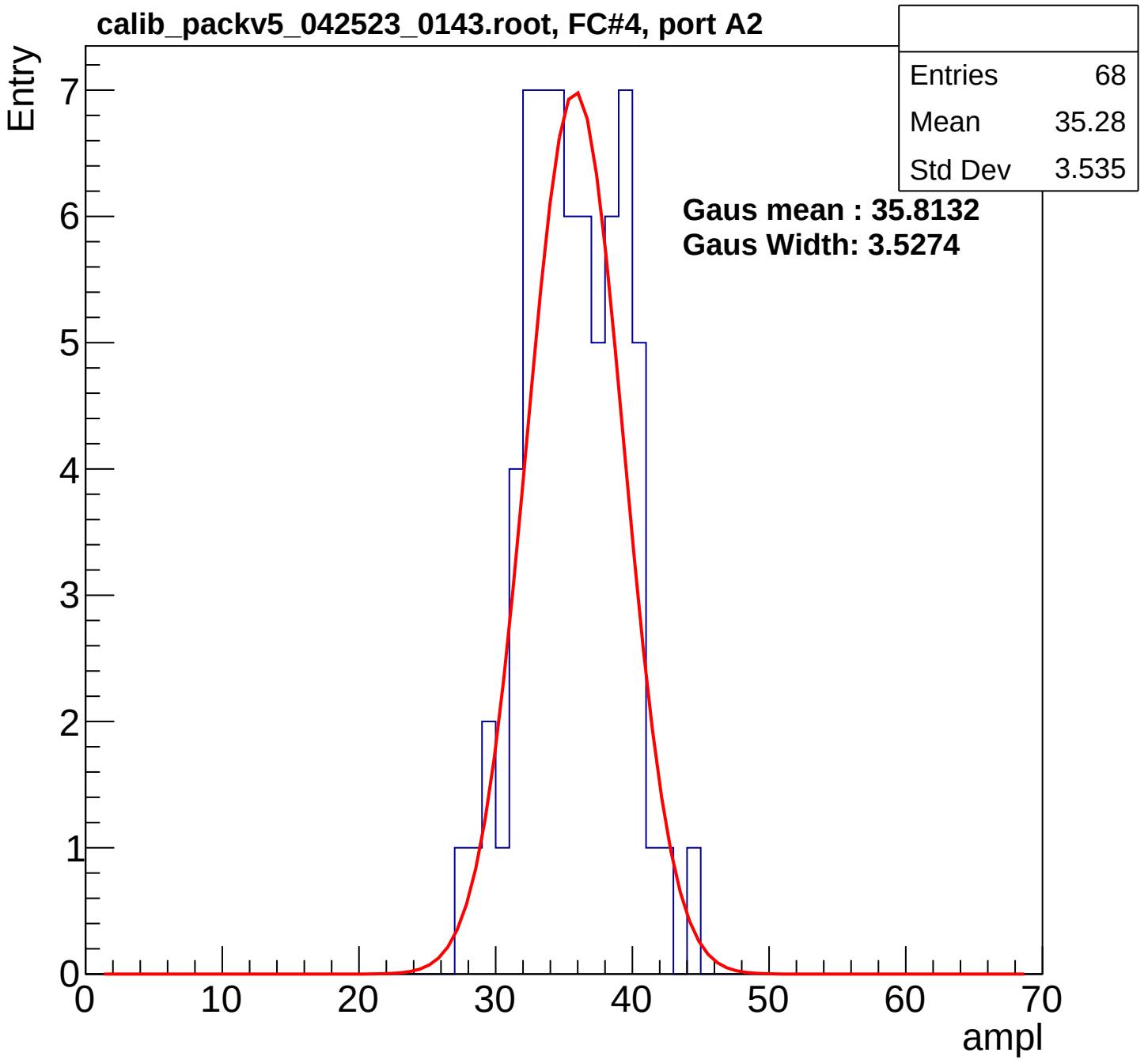
B1L100S, U17-ch81, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 35.28
Std Dev 3.535
Gaus mean : 35.8132
Gaus Width: 3.5274
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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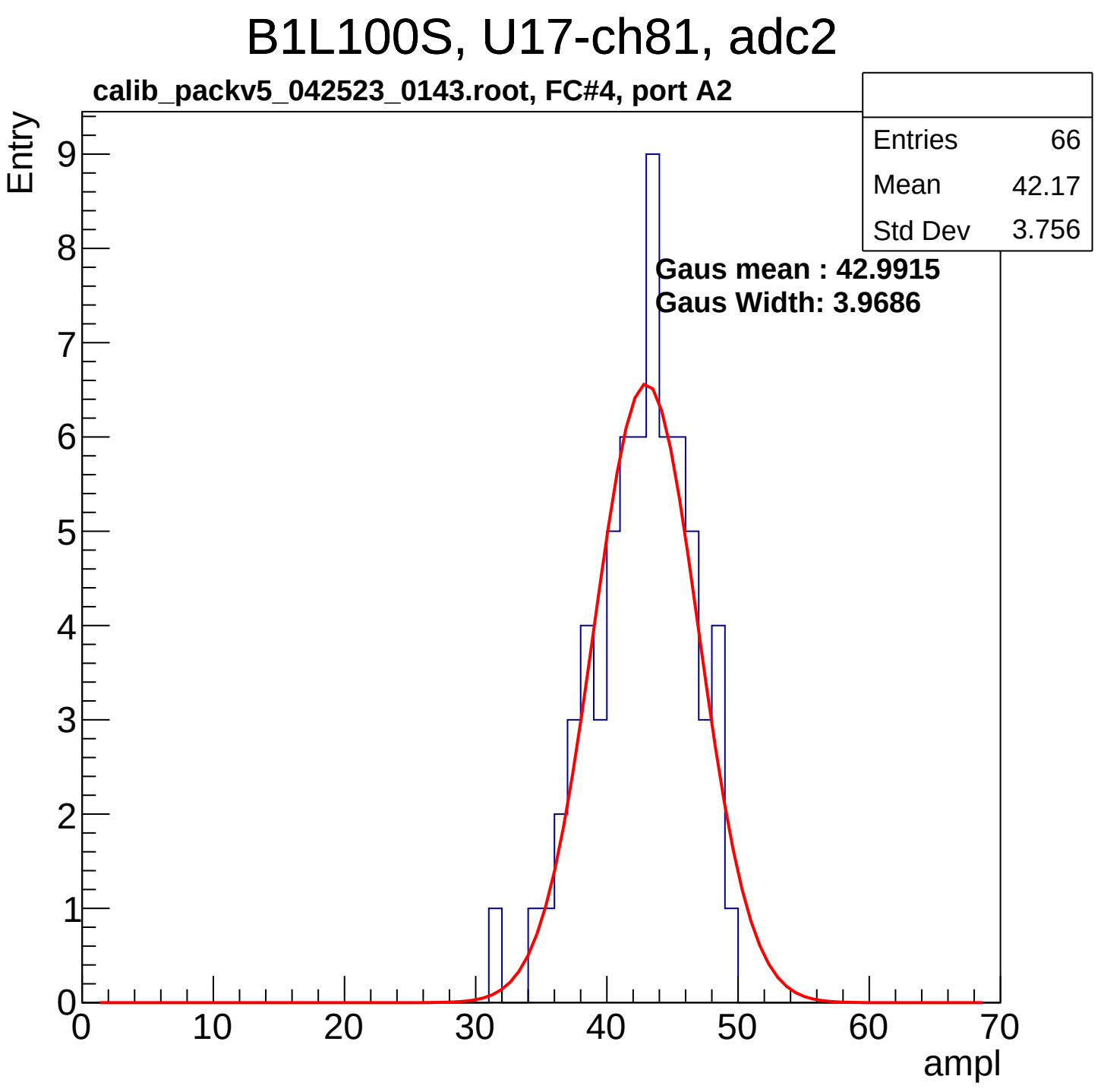
B1L100S, U17-ch81, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 42.17
Std Dev 3.756
Gaus mean : 42.9915
Gaus Width: 3.9686
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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40
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60
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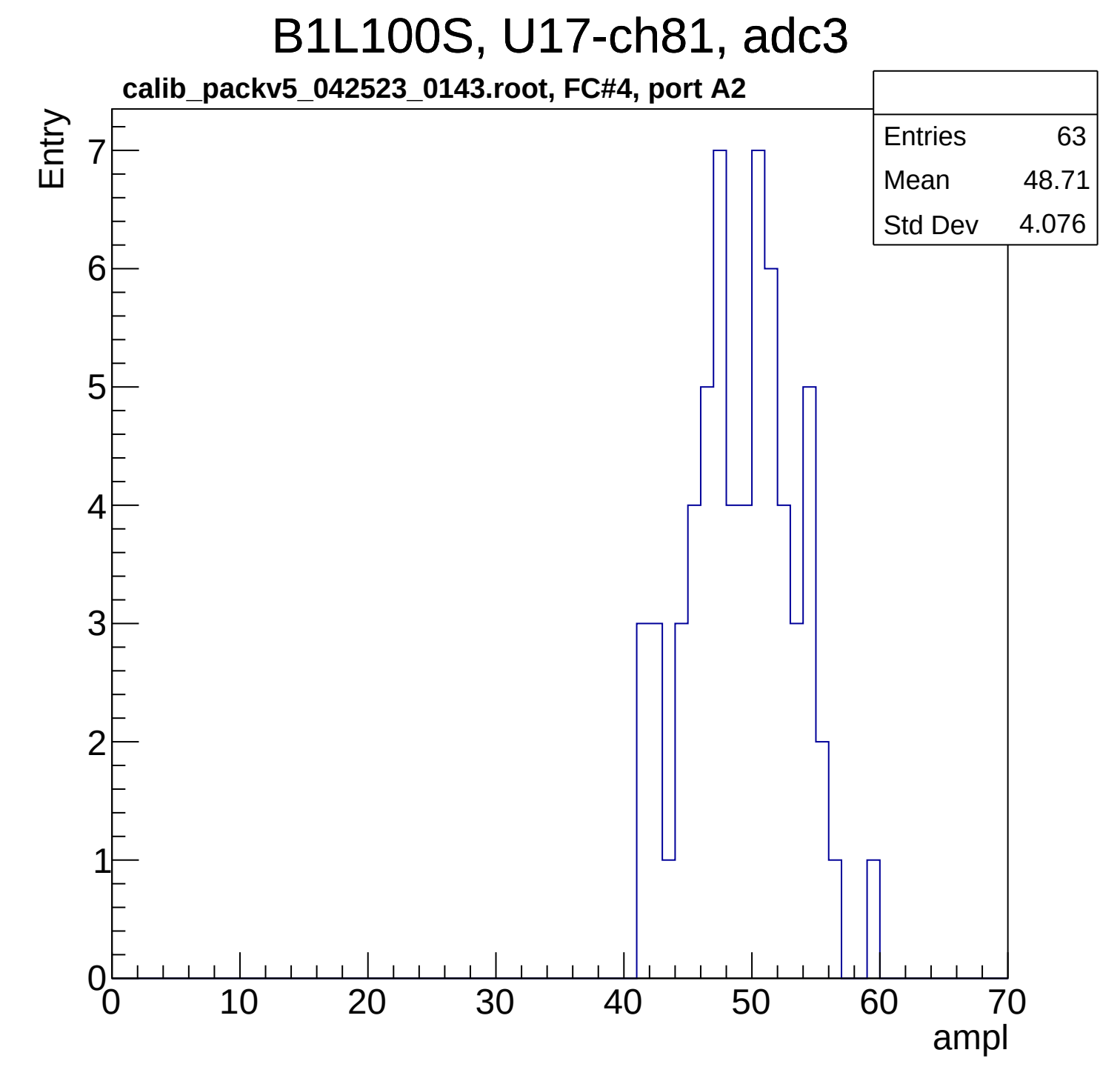
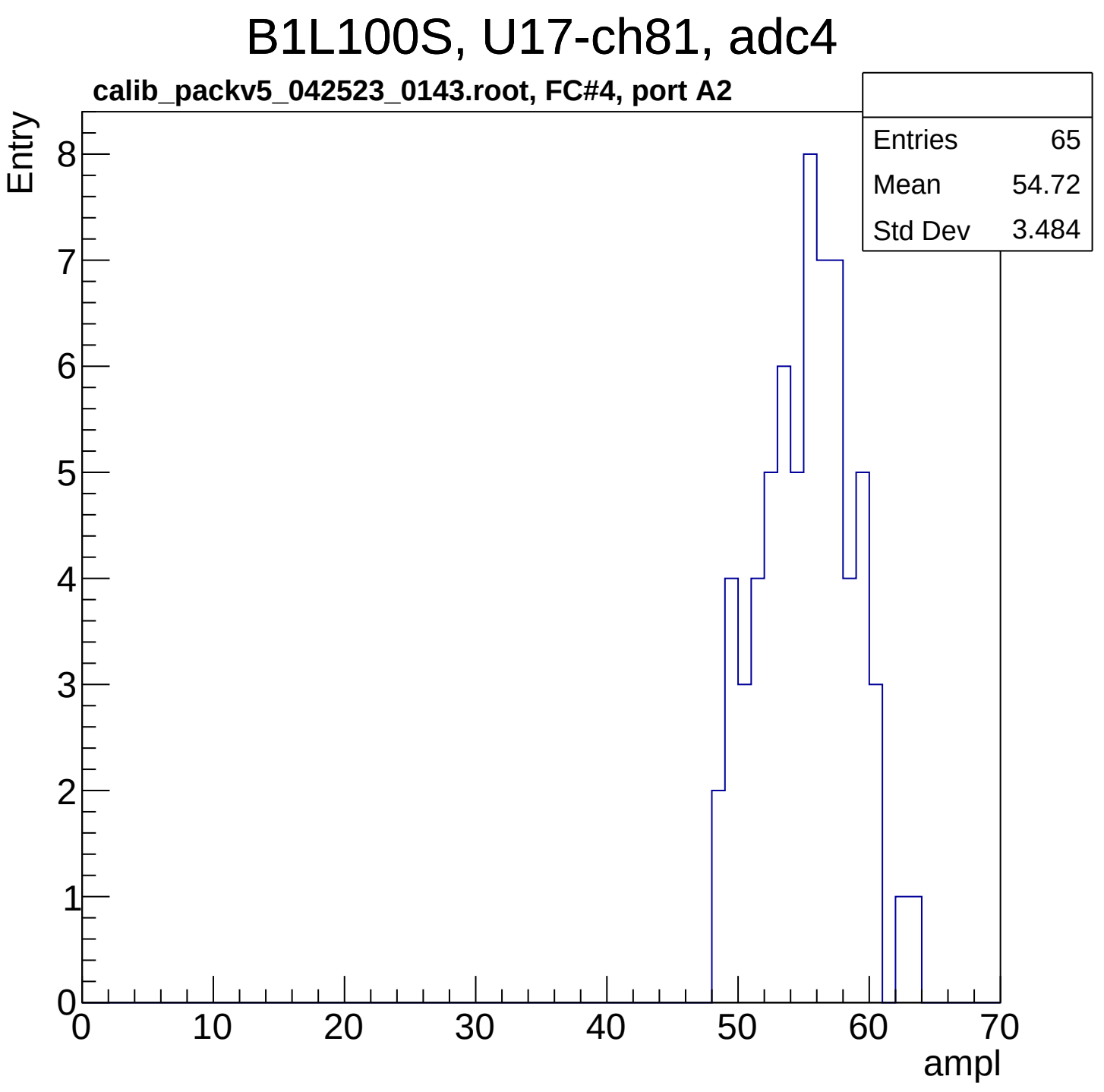
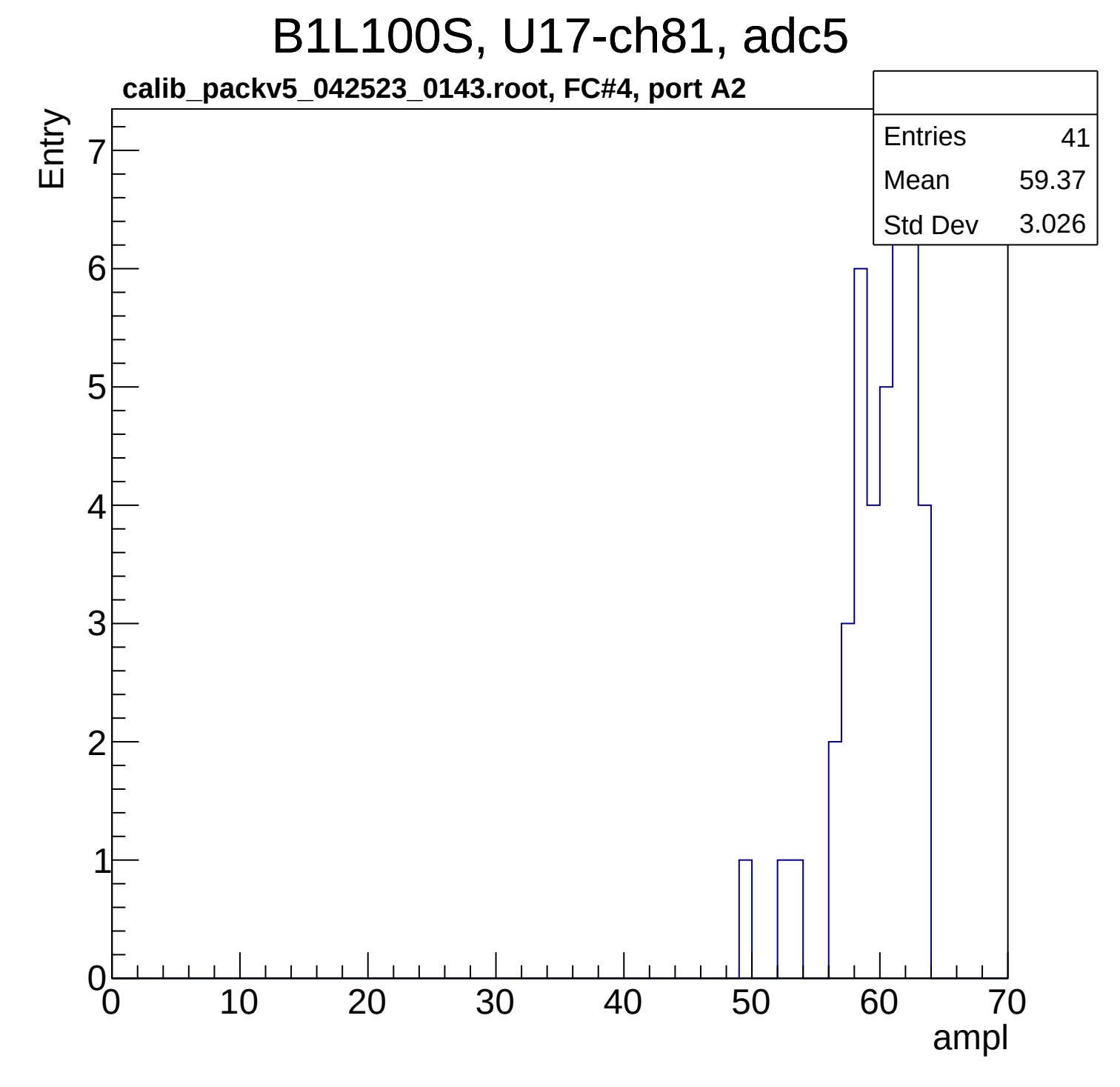
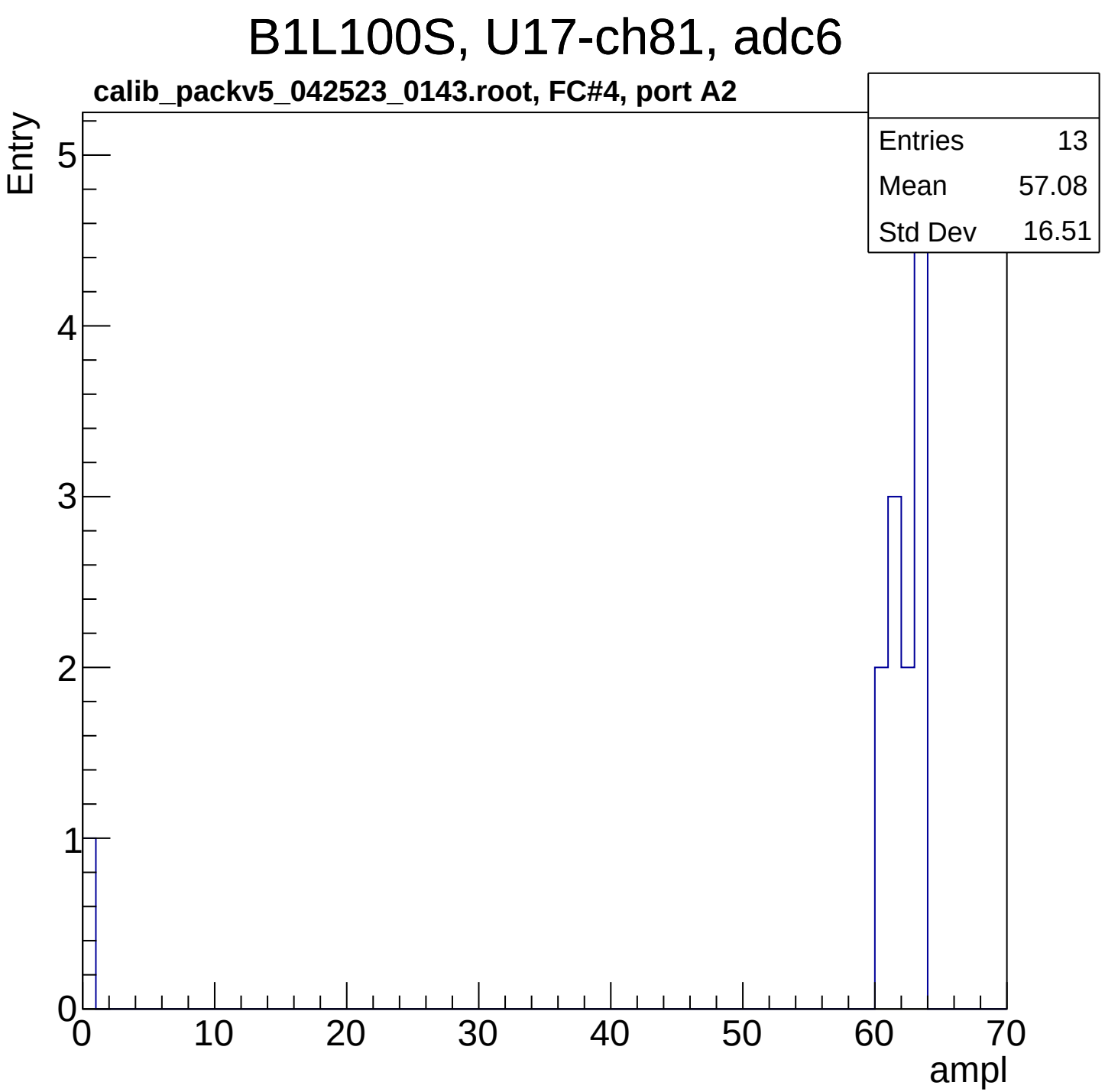
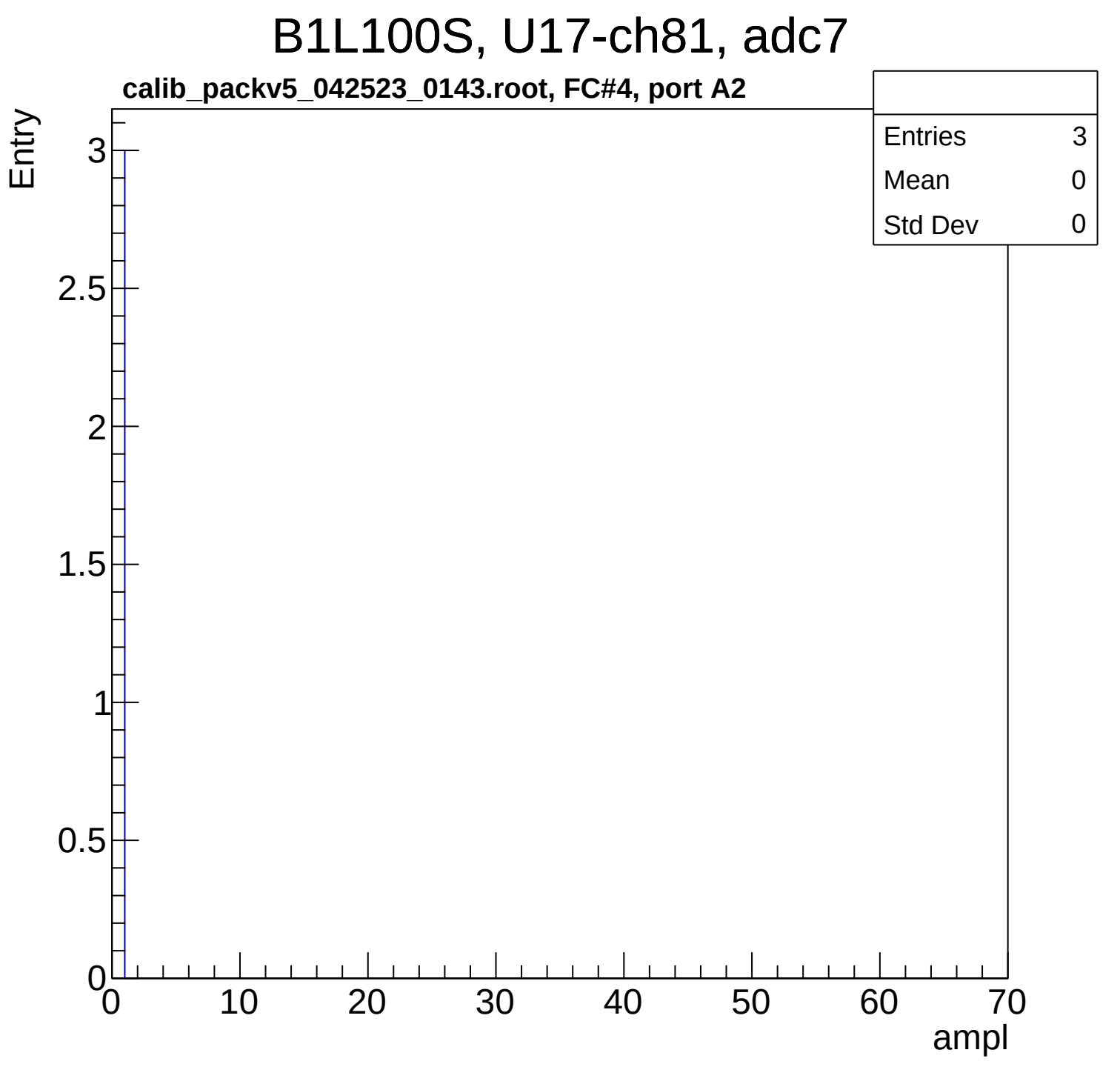

B1L100S, U17-ch81, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 48.71
Std Dev 4.076
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U17-ch81, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 54.72
Std Dev 3.484
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch81, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 41
Mean 59.37
Std Dev 3.026
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U17-ch81, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 13
Mean 57.08
Std Dev 16.51
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch81, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 0
Std Dev 0
Entry
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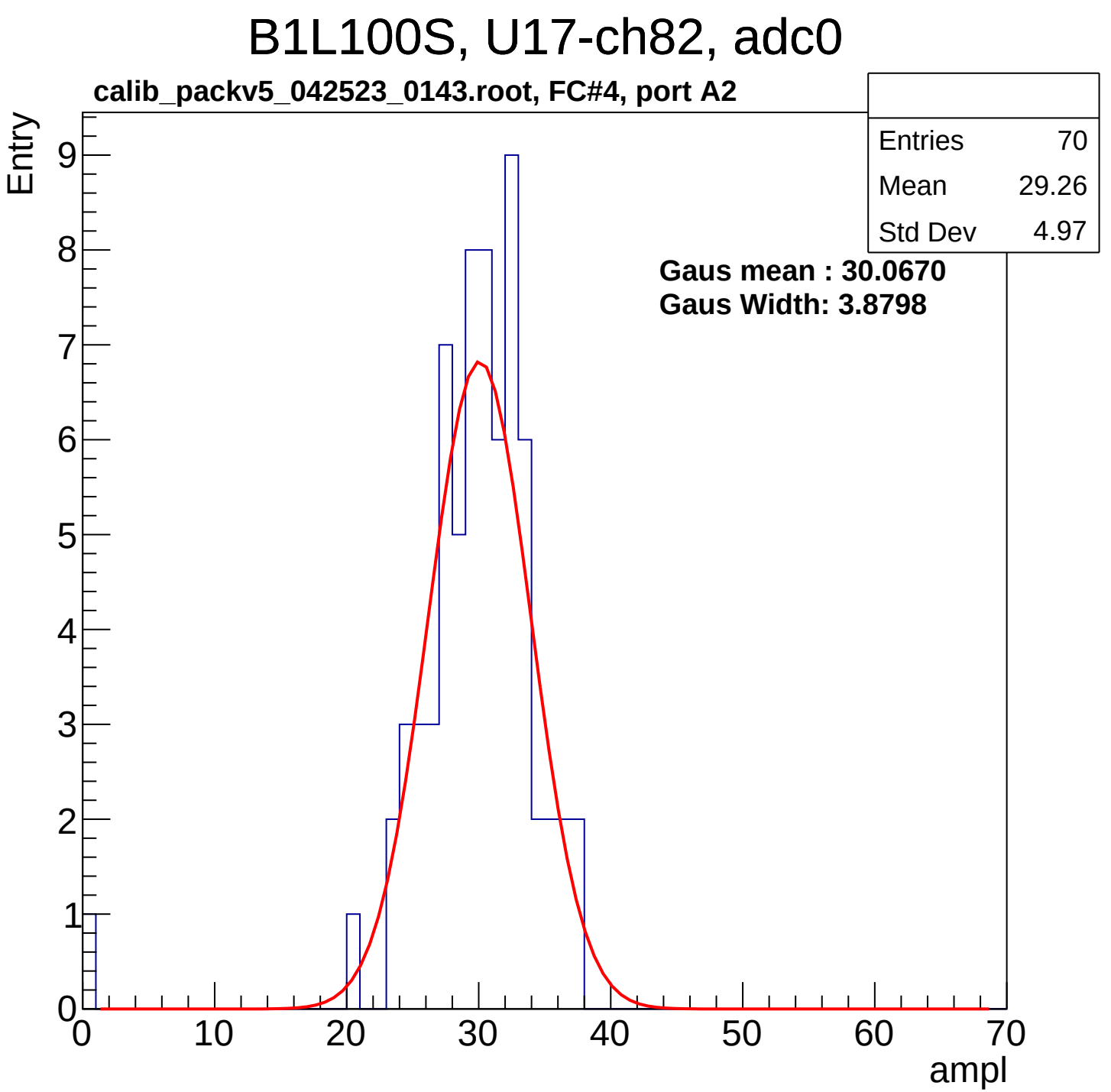
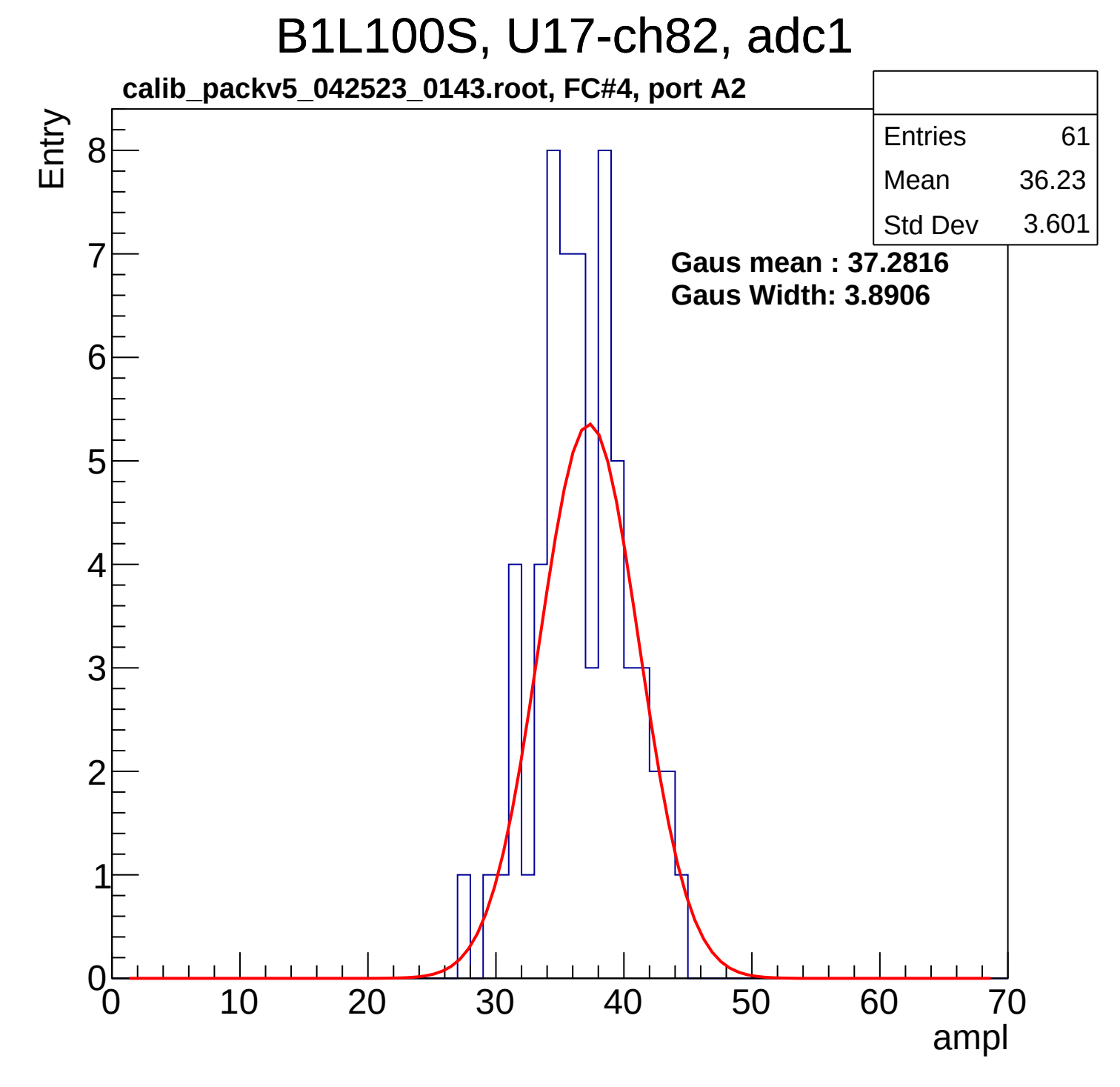
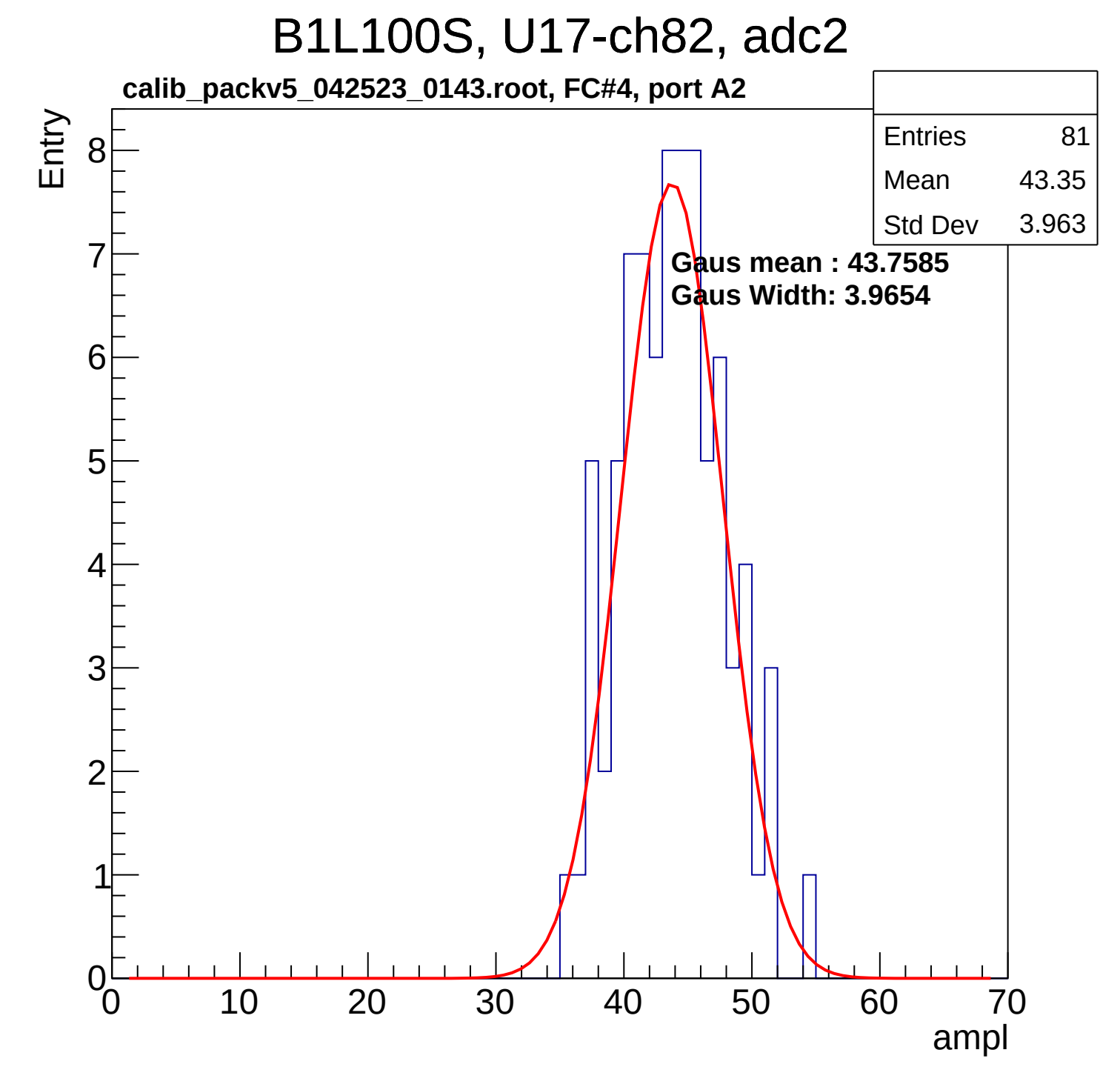
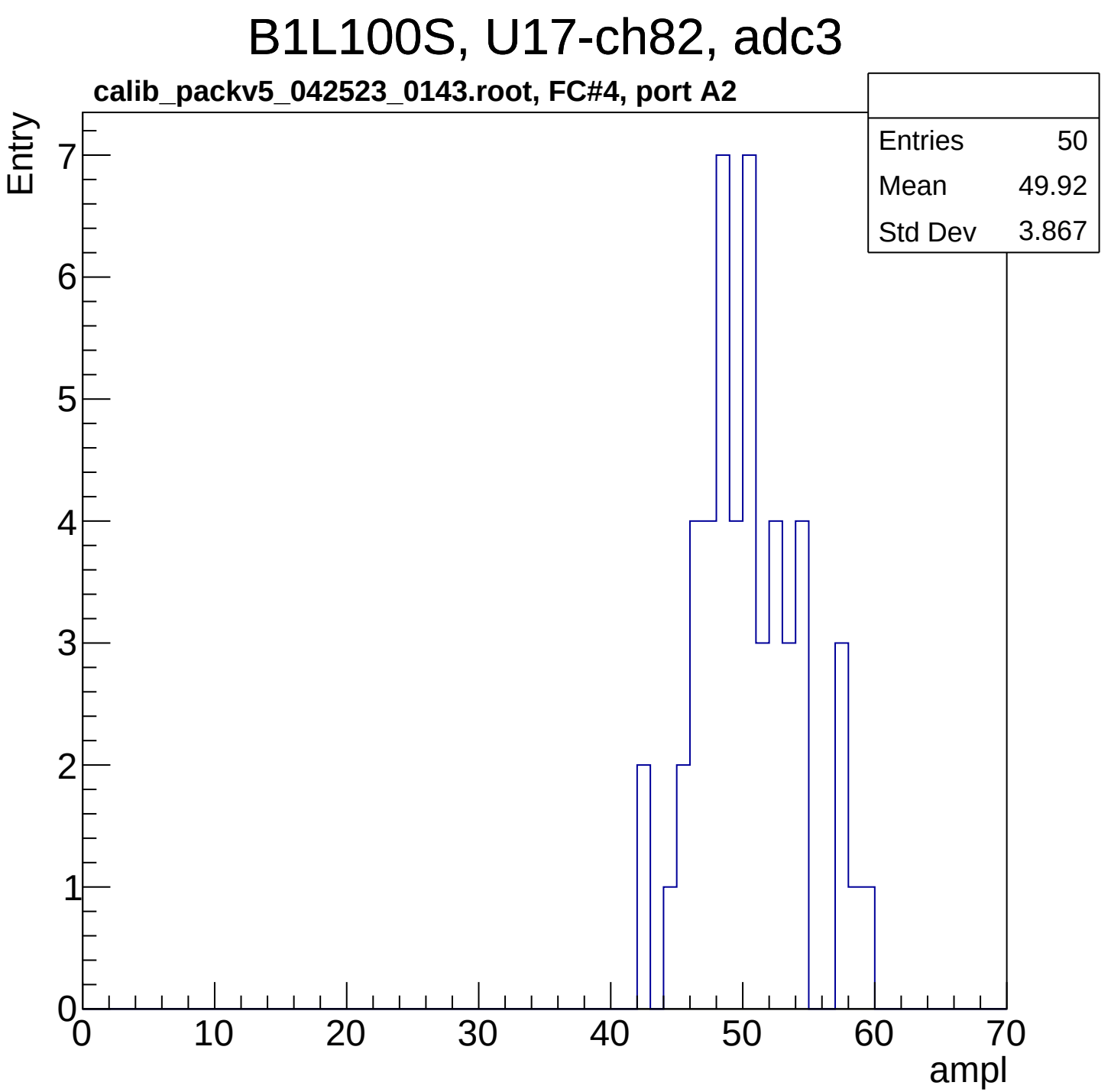
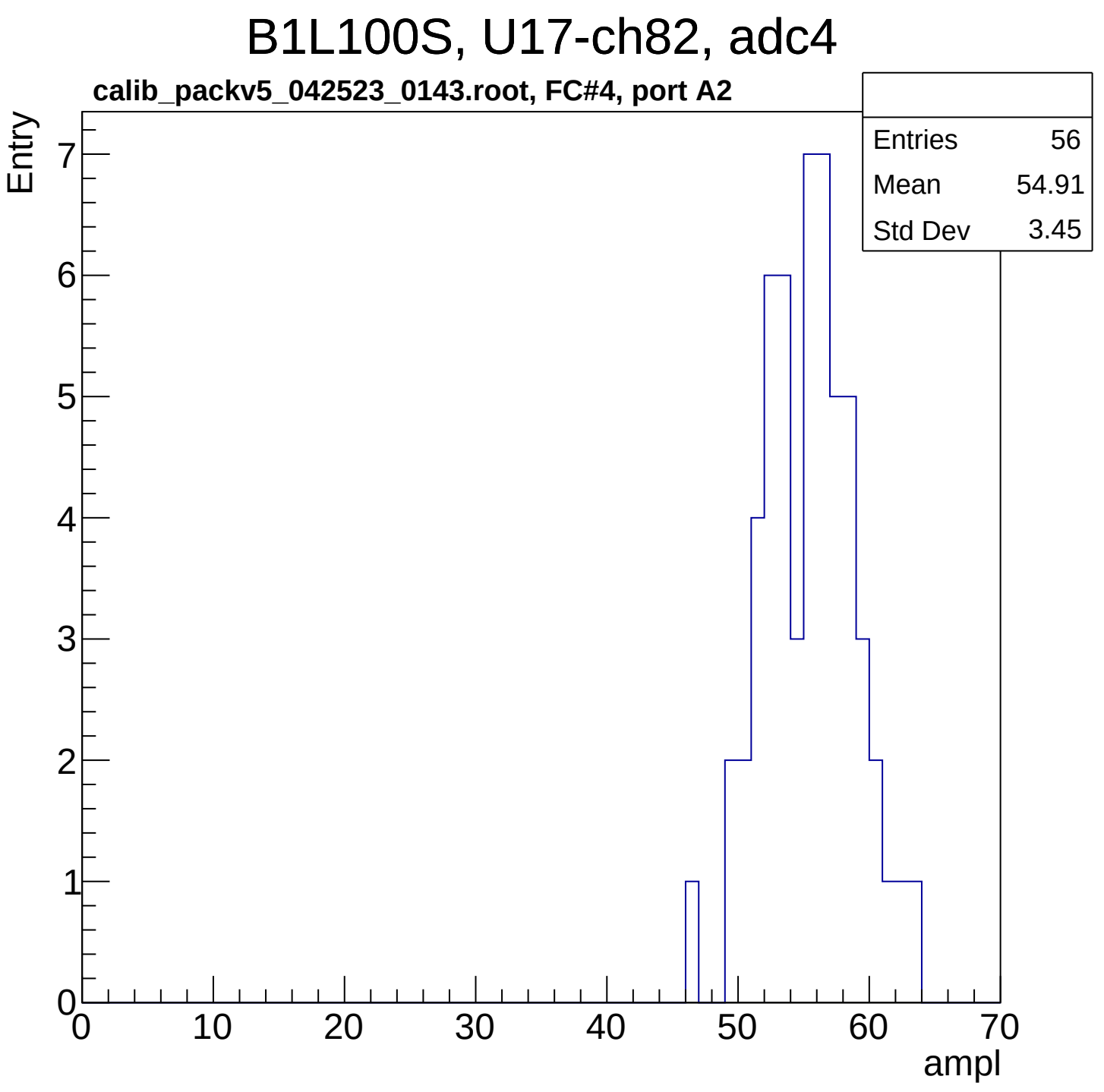
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl

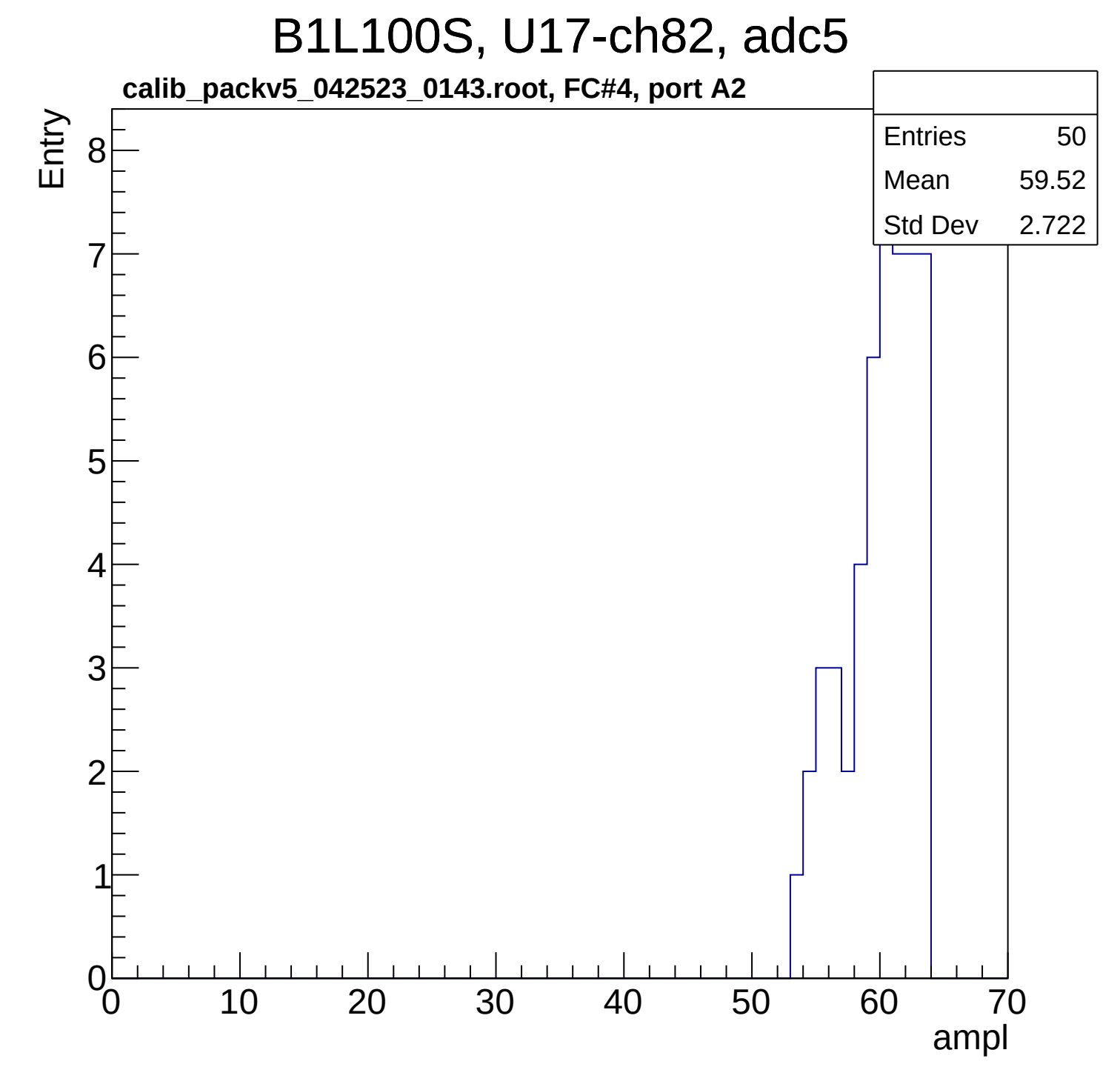

B1L100S, U17-ch82, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 29.26
Std Dev 4.97
Gaus mean : 30.0670
Gaus Width: 3.8798
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch82, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 36.23
Std Dev 3.601
Gaus mean : 37.2816
Gaus Width: 3.8906
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch82, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 81
Mean 43.35
Std Dev 3.963
Gaus mean : 43.7585
Gaus Width: 3.9654
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch82, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 49.92
Std Dev 3.867
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U17-ch82, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 54.91
Std Dev 3.45
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U17-ch82, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 59.52
Std Dev 2.722
Entry
ampl
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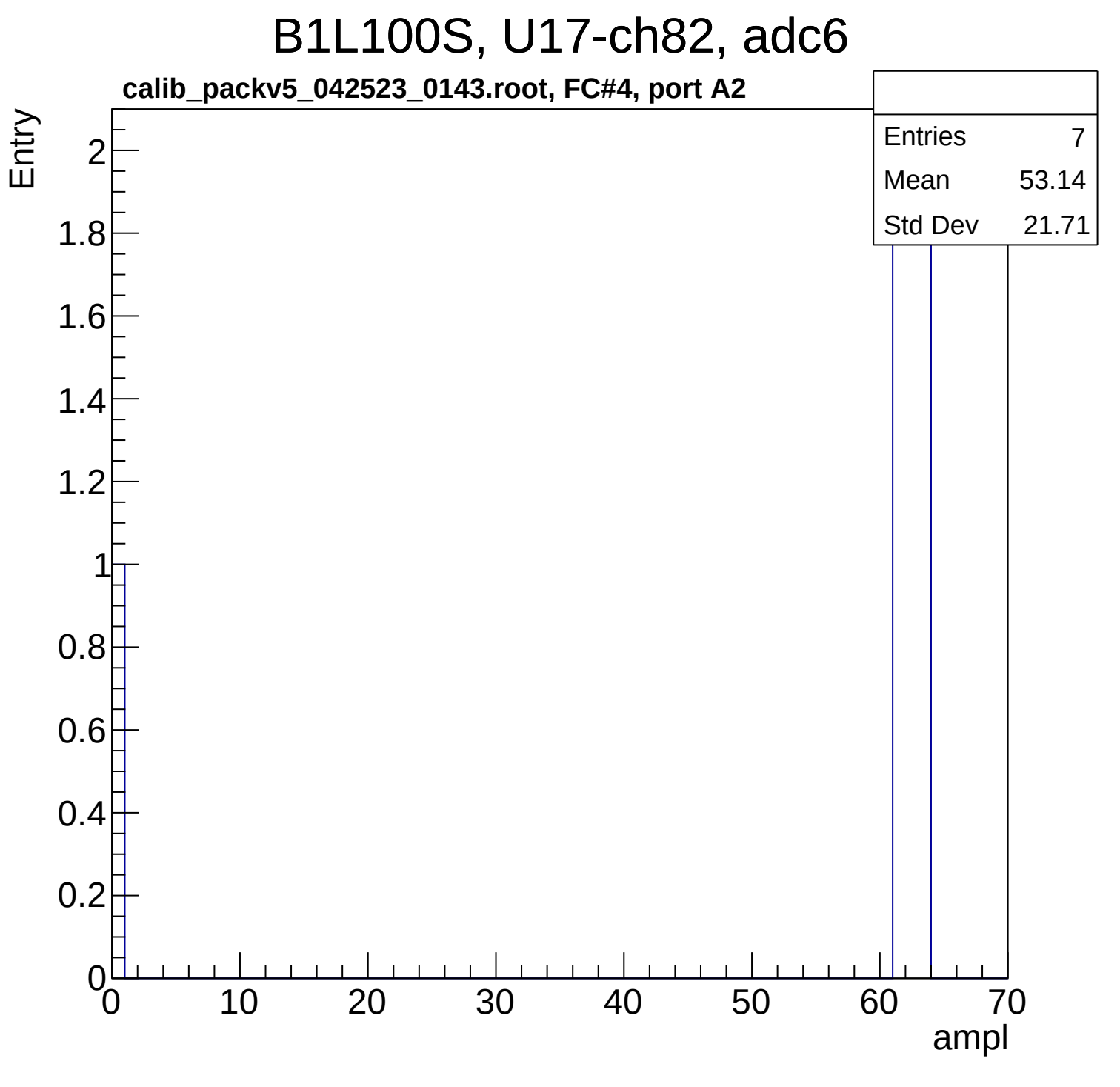
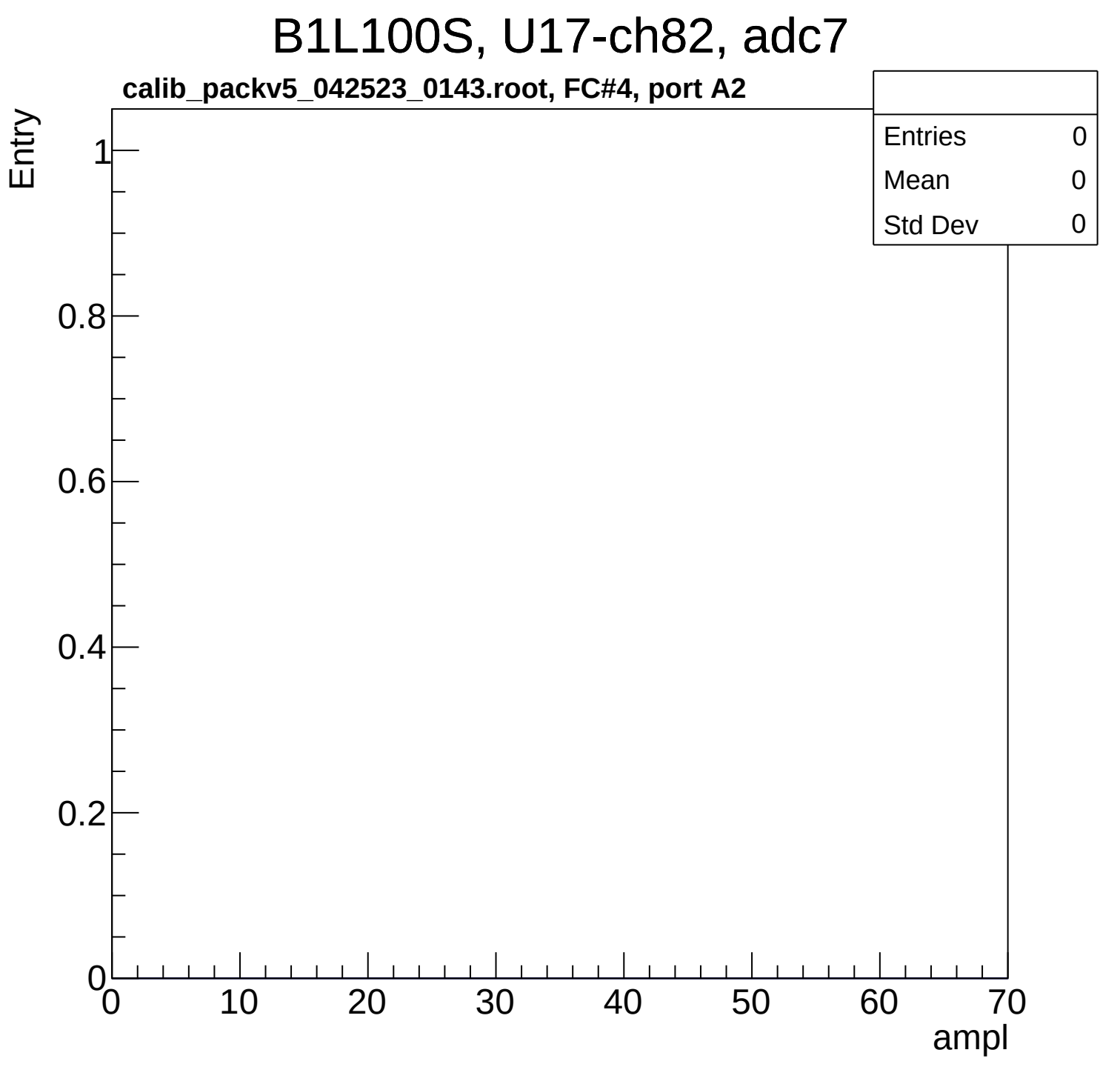
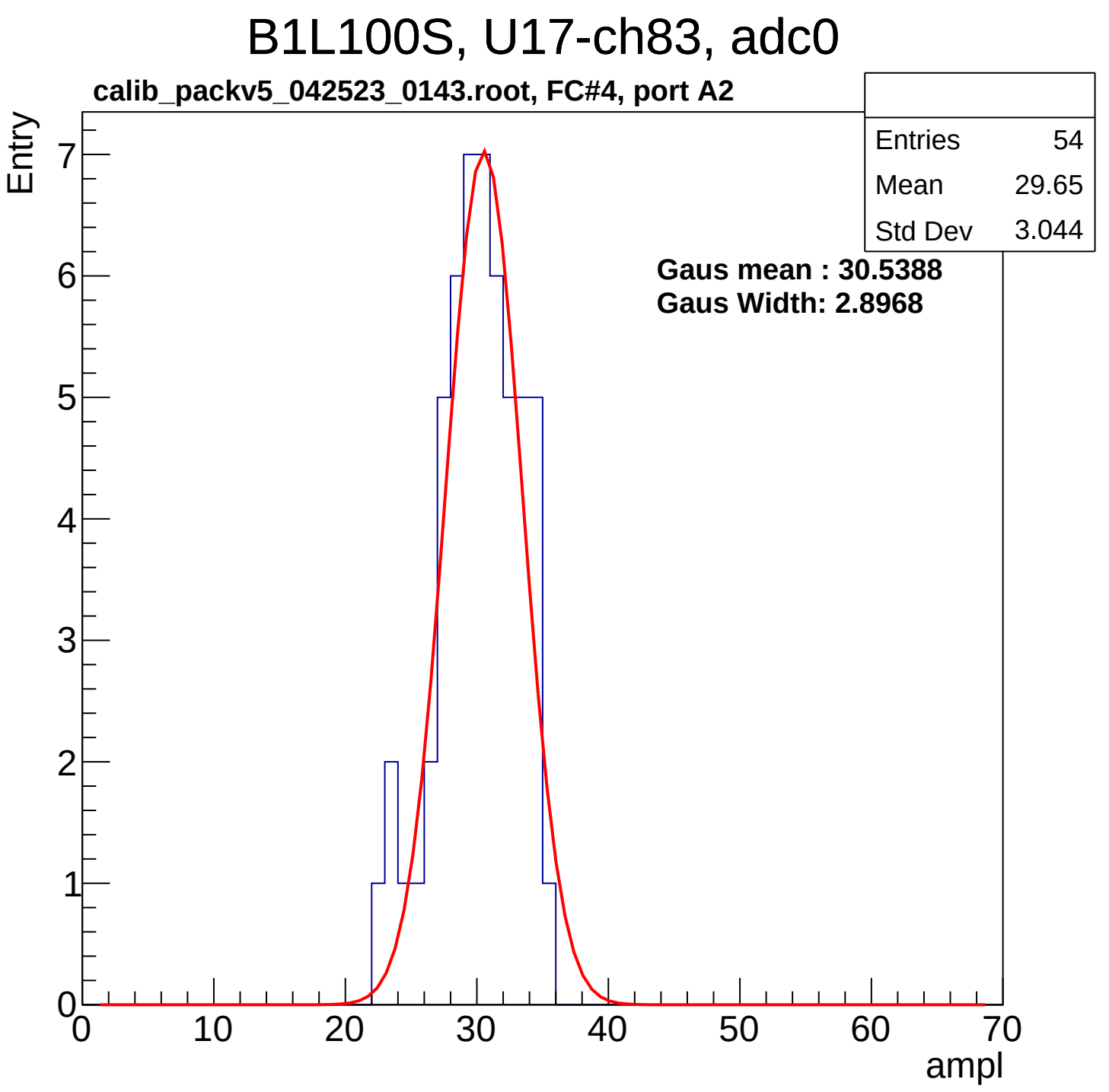
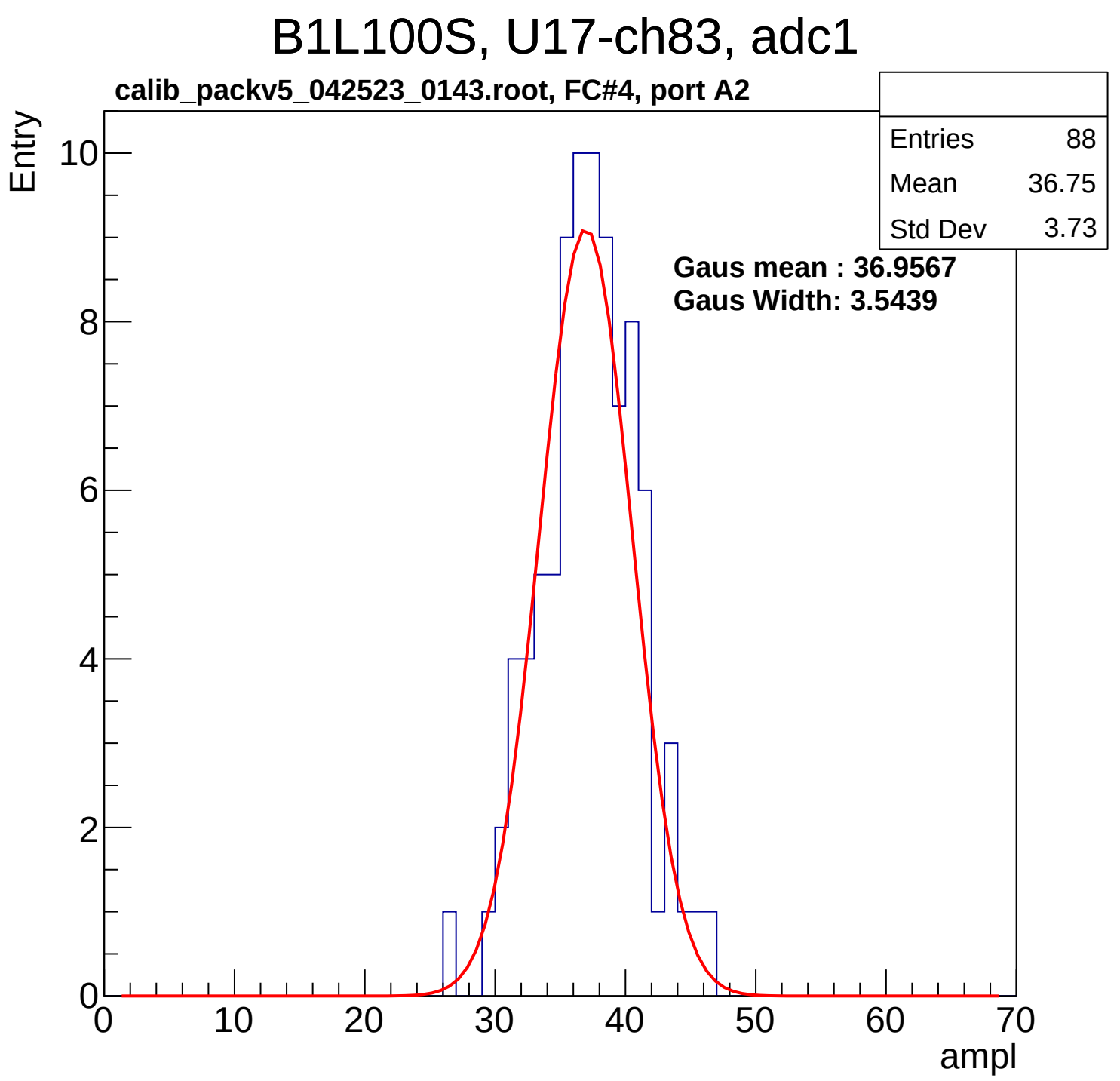
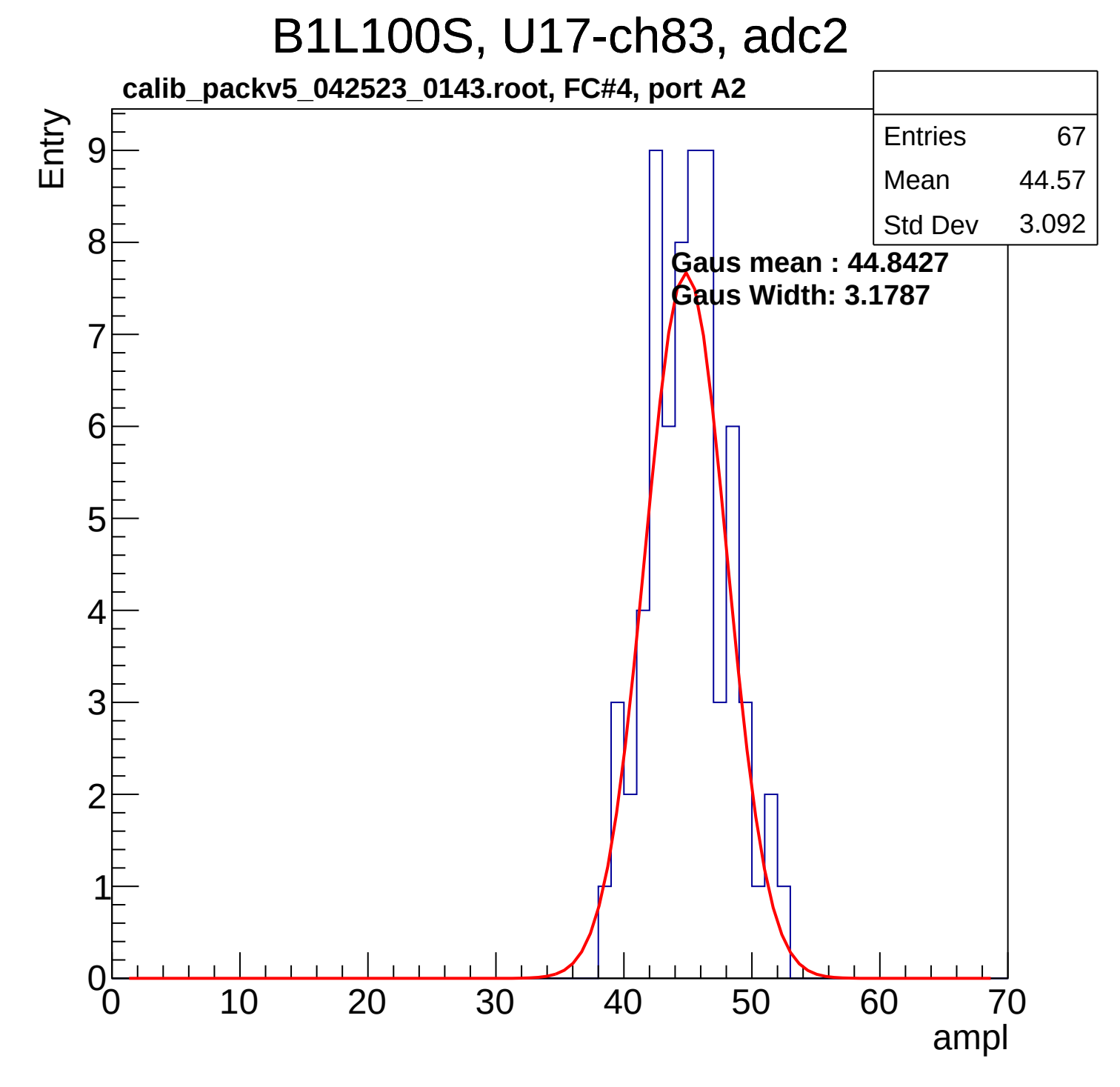
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch82, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 7
Mean 53.14
Std Dev 21.71
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L100S, U17-ch82, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch83, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 29.65
Std Dev 3.044
Gaus mean : 30.5388
Gaus Width: 2.8968
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U17-ch83, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 88
Mean 36.75
Std Dev 3.73
Gaus mean : 36.9567
Gaus Width: 3.5439
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U17-ch83, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 44.57
Std Dev 3.092
Gaus mean : 44.8427
Gaus Width: 3.1787
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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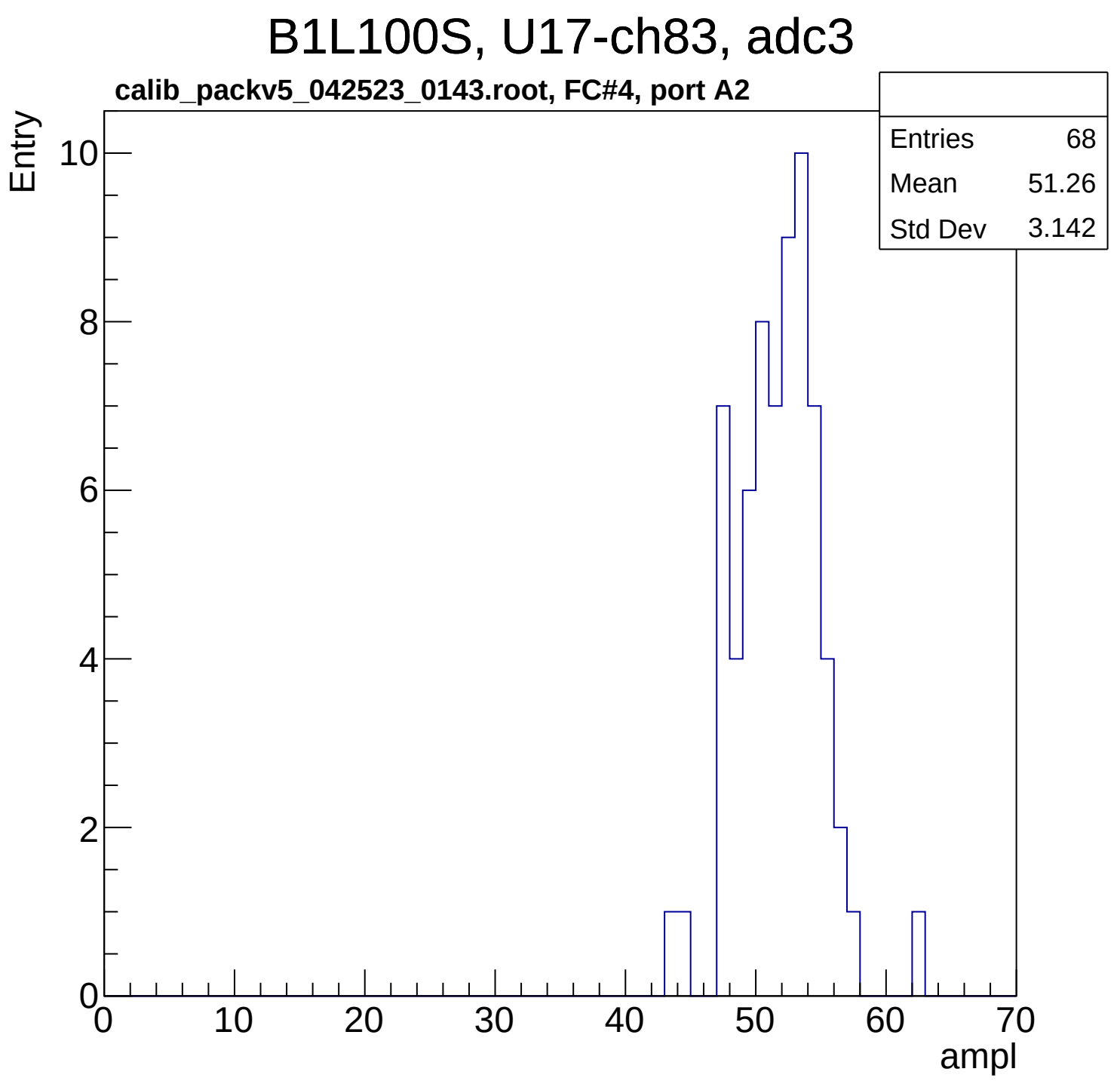
B1L100S, U17-ch83, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 51.26
Std Dev 3.142
Entry
ampl
0
2
4
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0
10
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60
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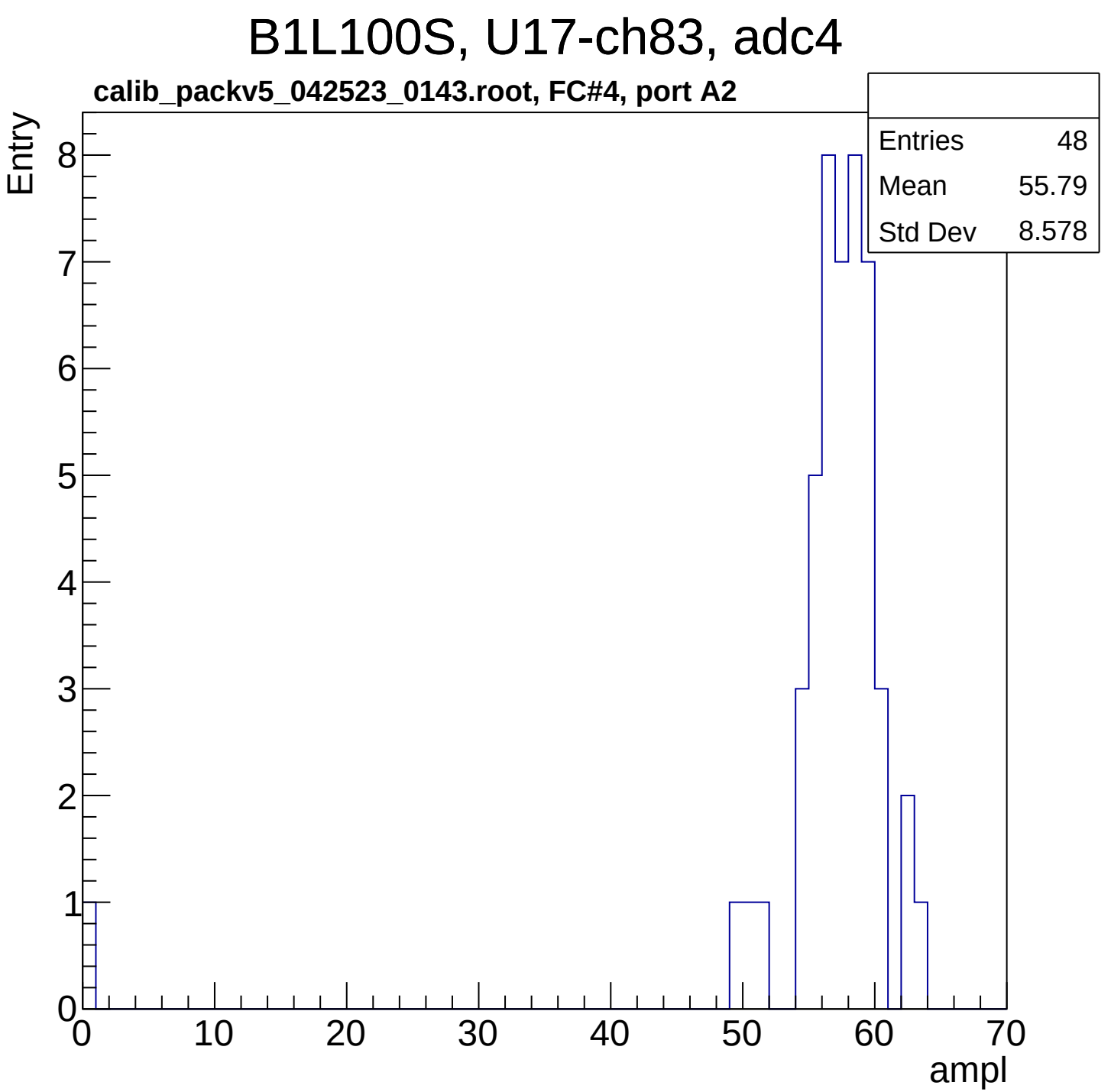
B1L100S, U17-ch83, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 48
Mean 55.79
Std Dev 8.578
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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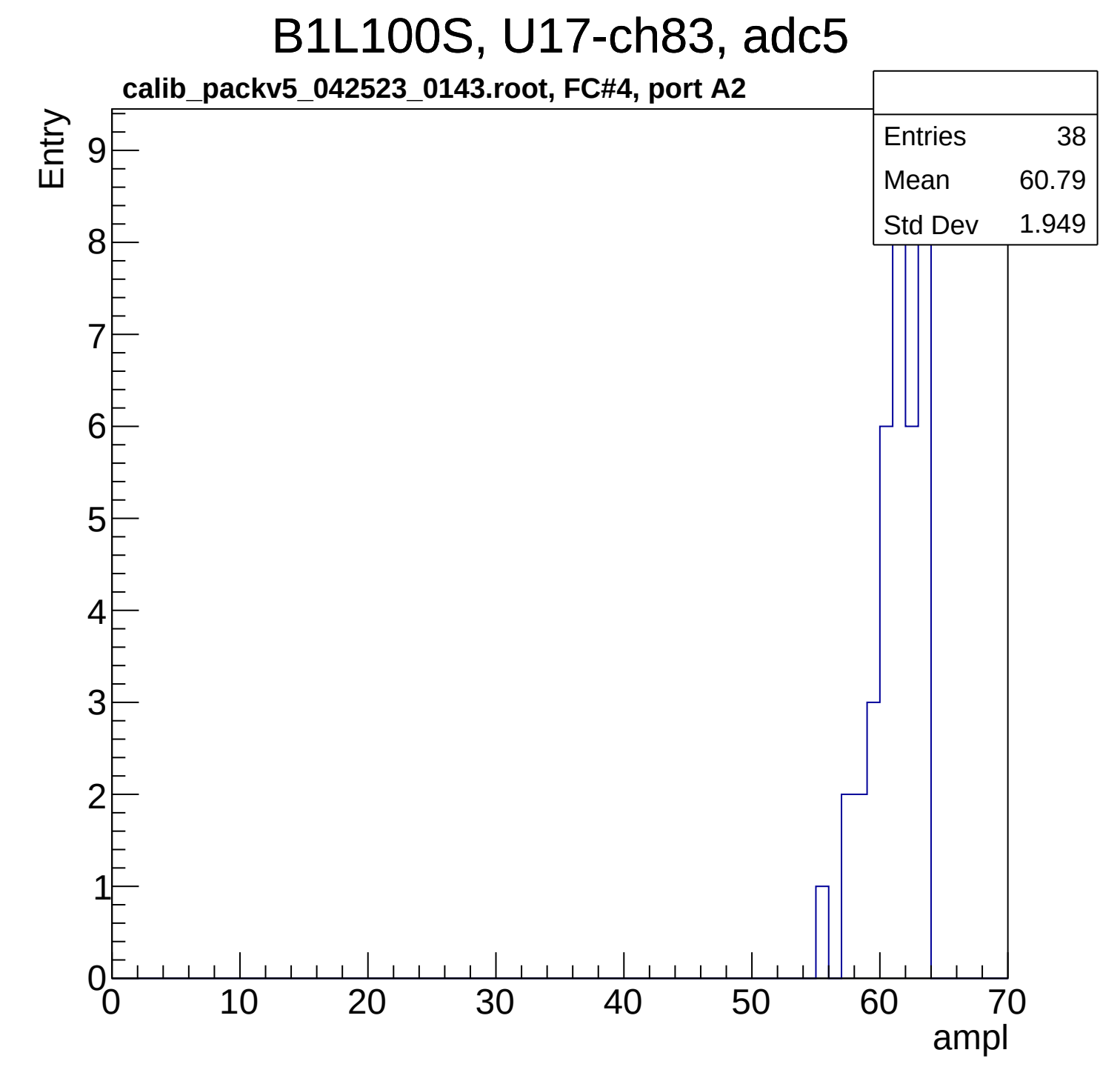
B1L100S, U17-ch83, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 38
Mean 60.79
Std Dev 1.949
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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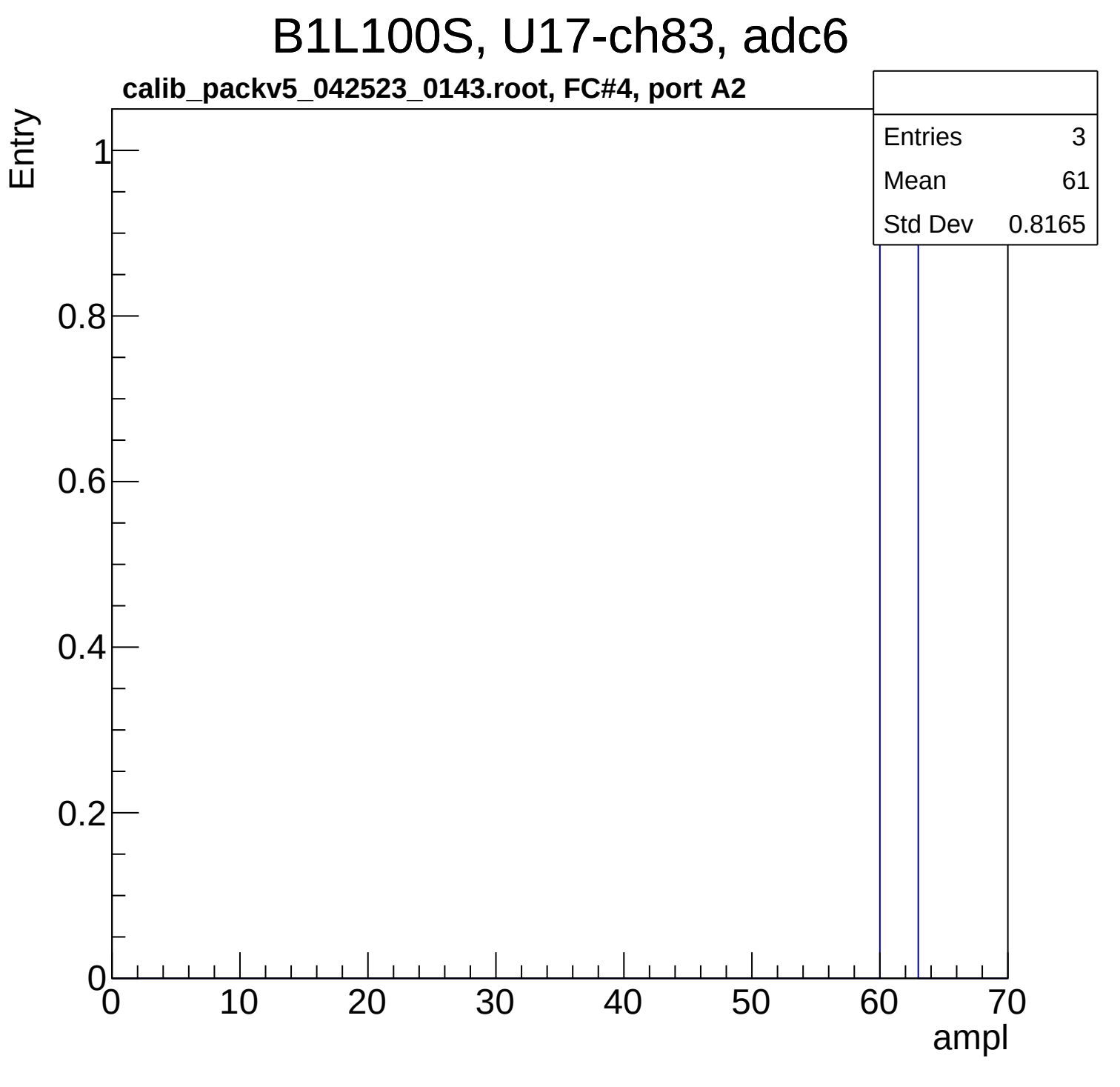
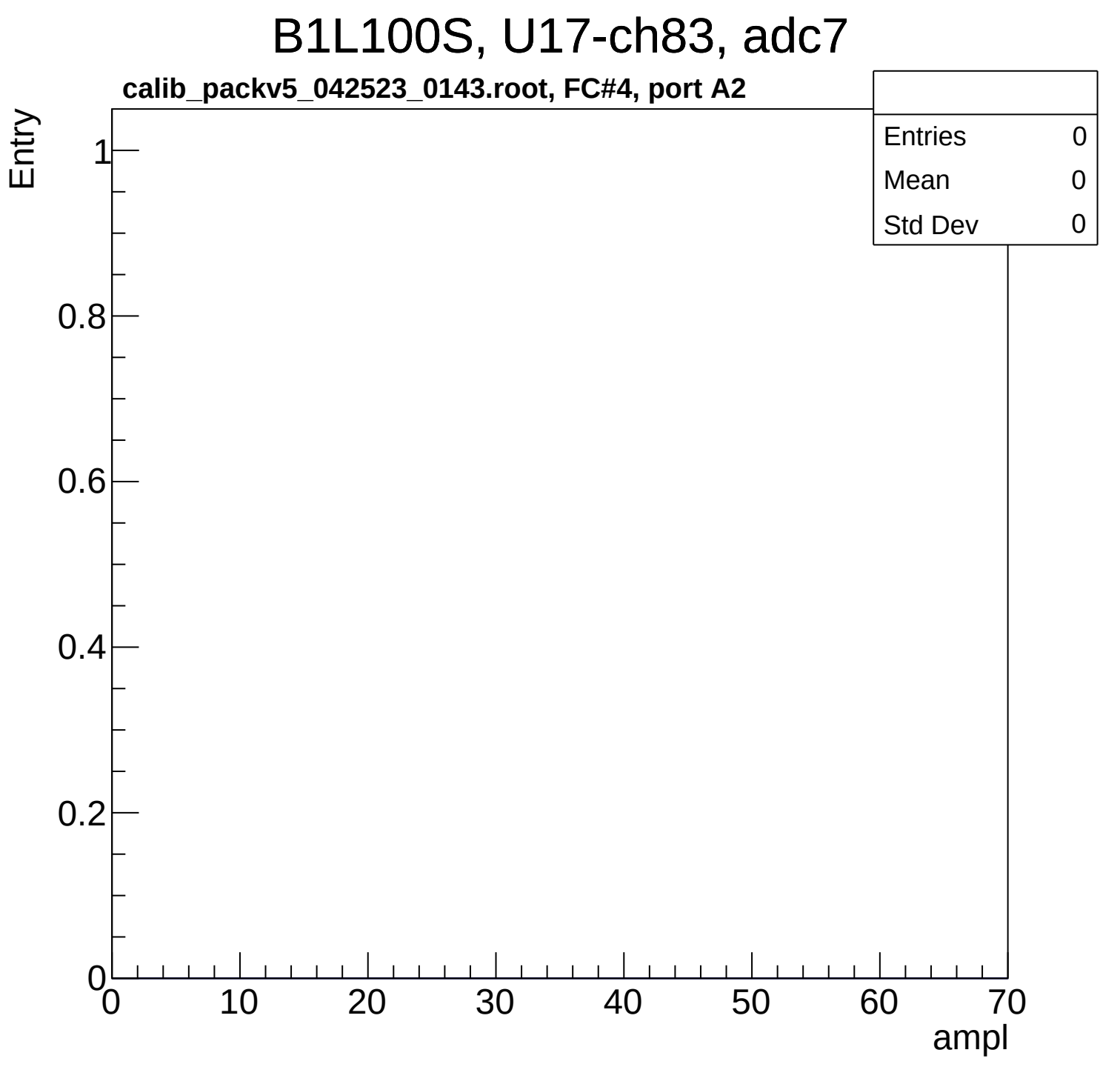

B1L100S, U17-ch83, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 61
Std Dev 0.8165
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch83, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
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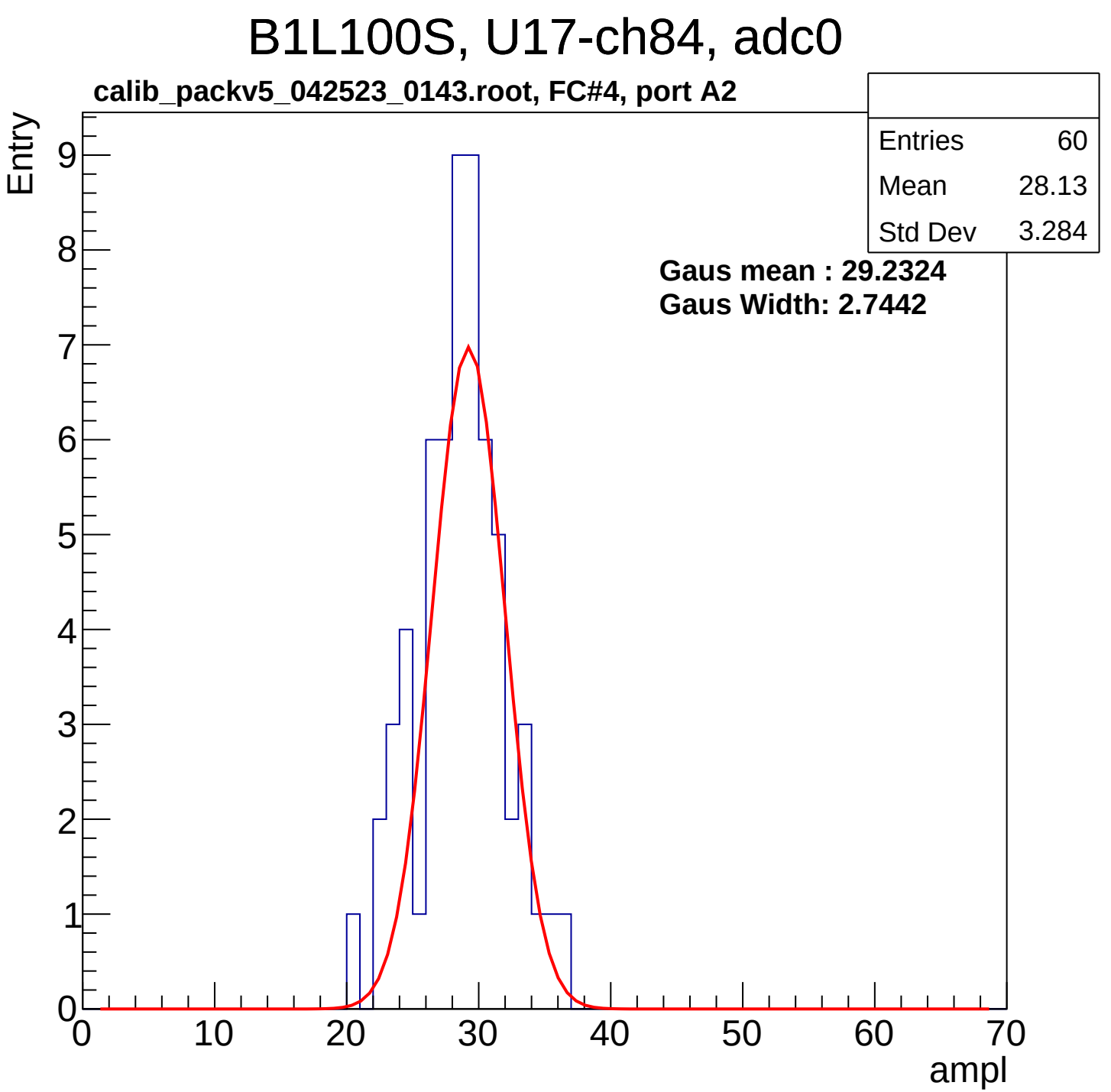
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch84, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 28.13
Std Dev 3.284
Gaus mean : 29.2324
Gaus Width: 2.7442
Entry
ampl
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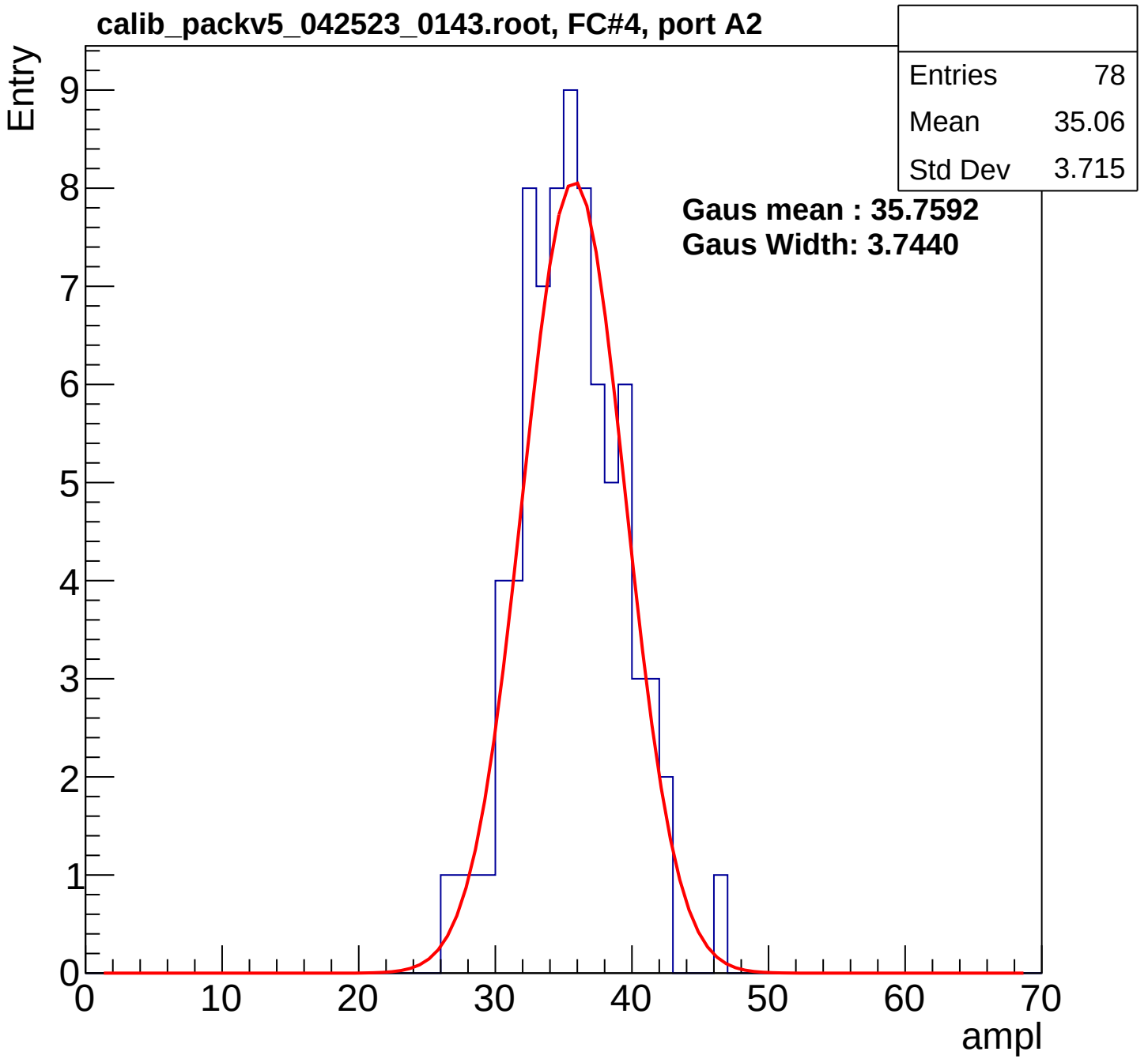
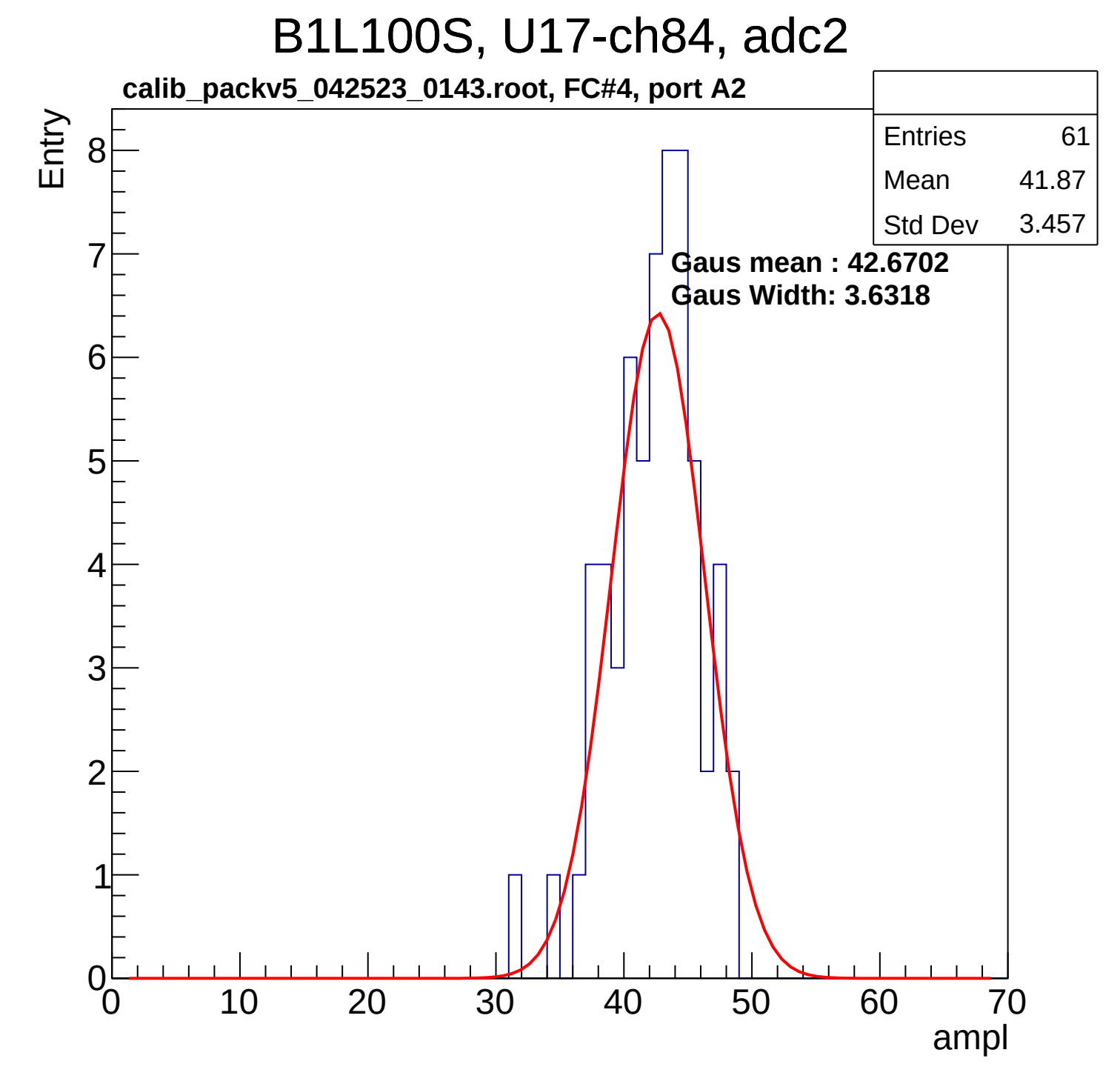
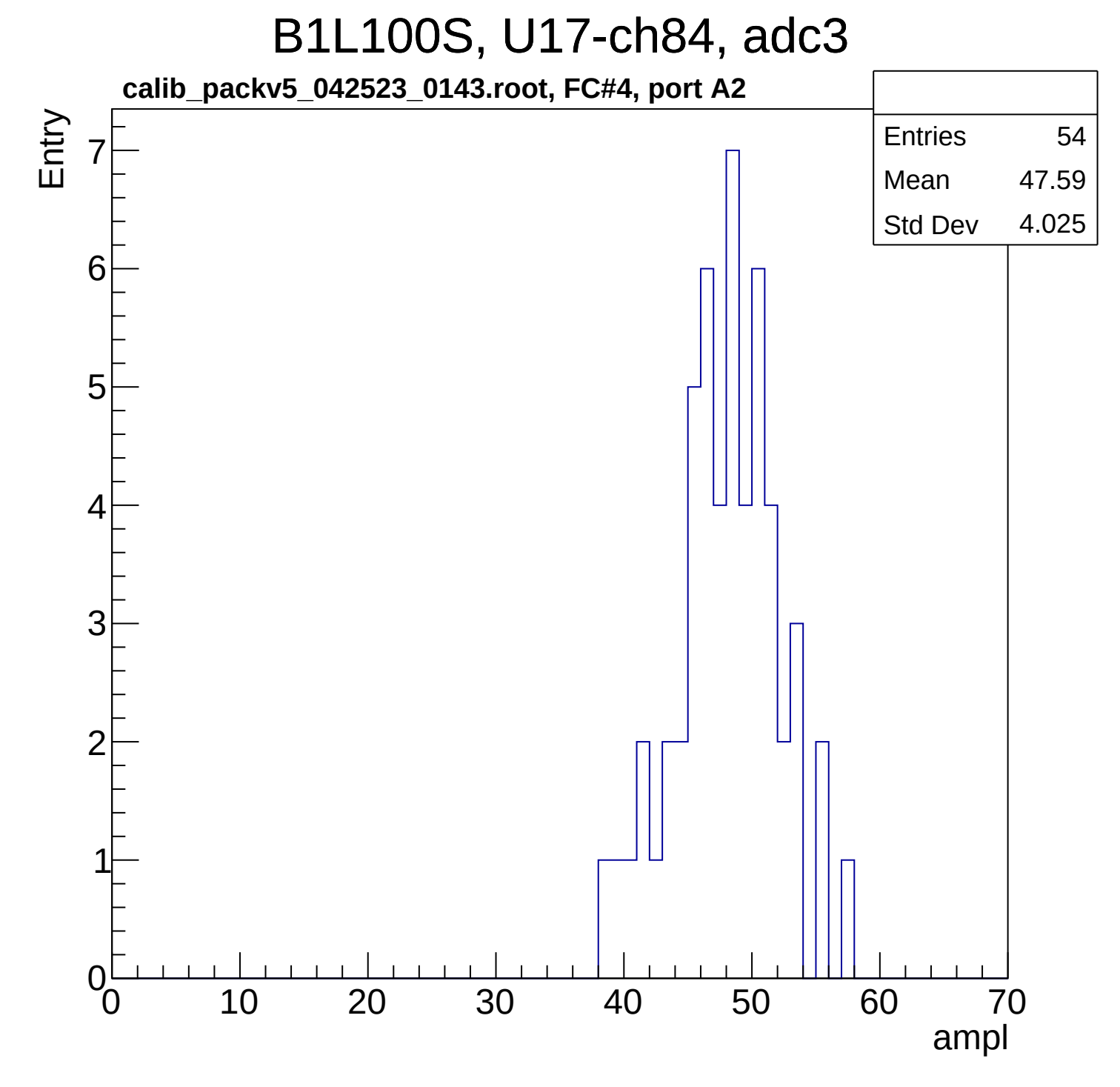
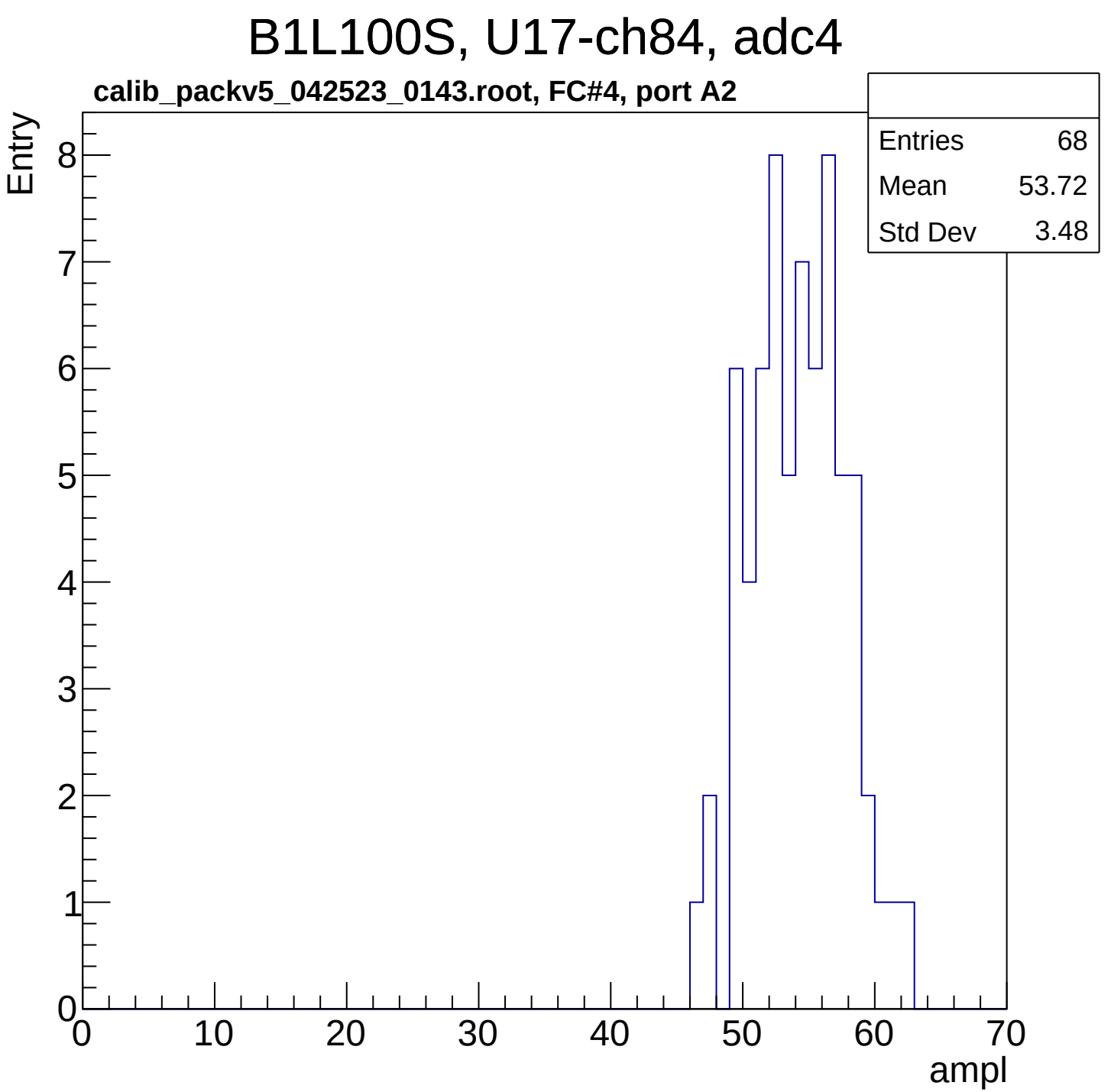
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch84, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 78
Mean 35.06
Std Dev 3.715
Gaus mean : 35.7592
Gaus Width: 3.7440
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch84, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 41.87
Std Dev 3.457
Gaus mean : 42.6702
Gaus Width: 3.6318
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch84, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 47.59
Std Dev 4.025
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U17-ch84, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 53.72
Std Dev 3.48
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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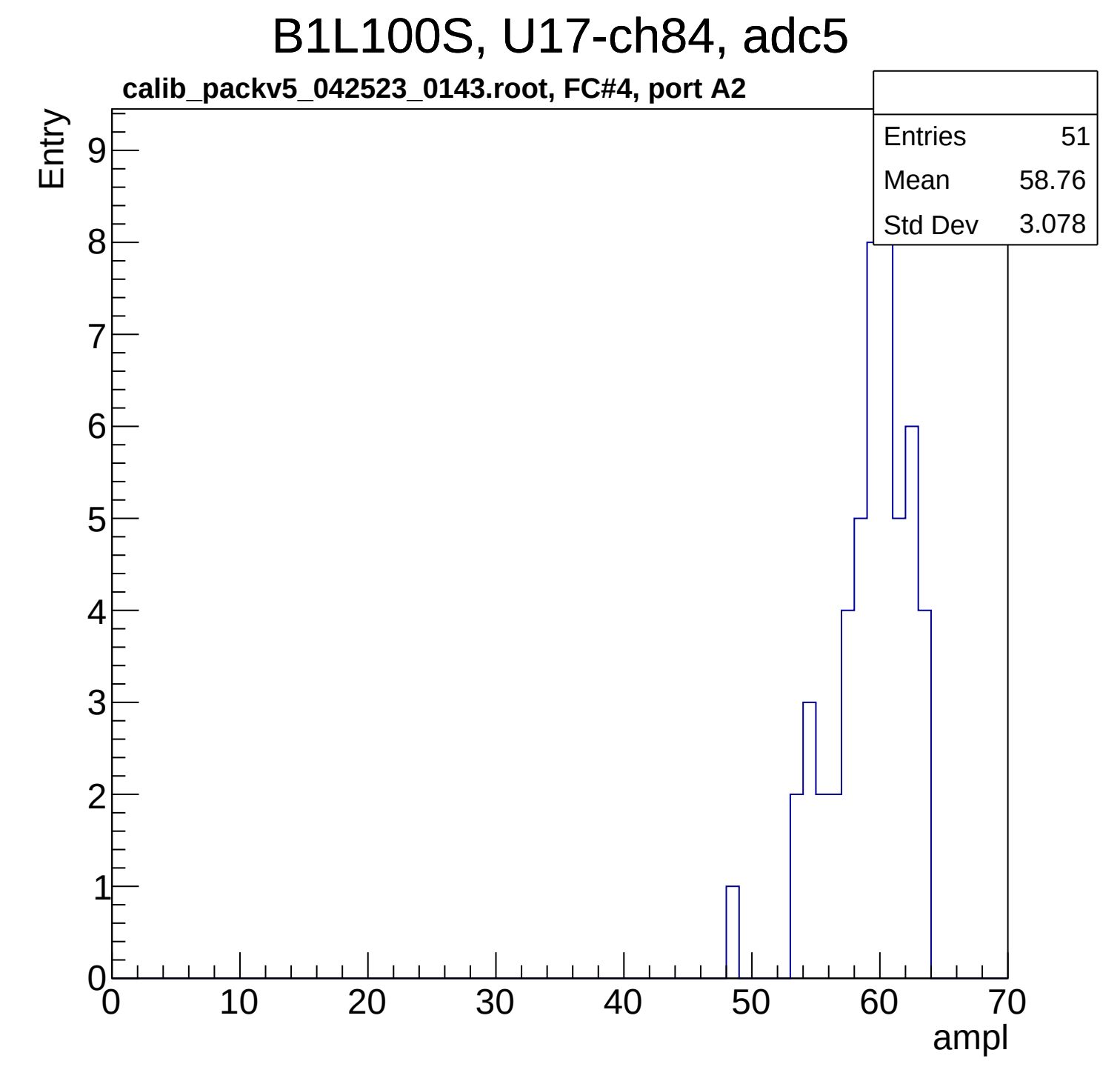
B1L100S, U17-ch84, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 58.76
Std Dev 3.078
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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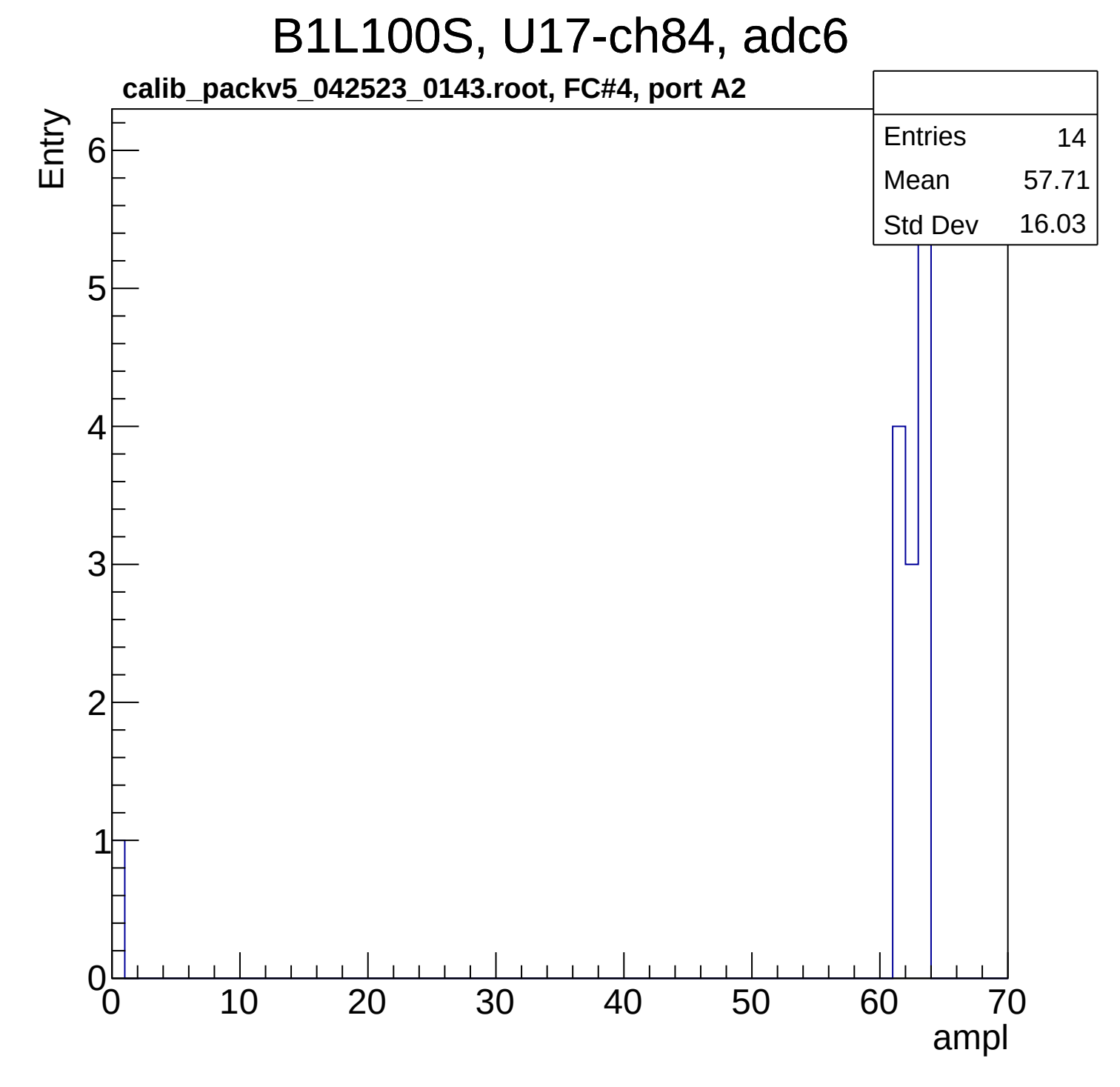
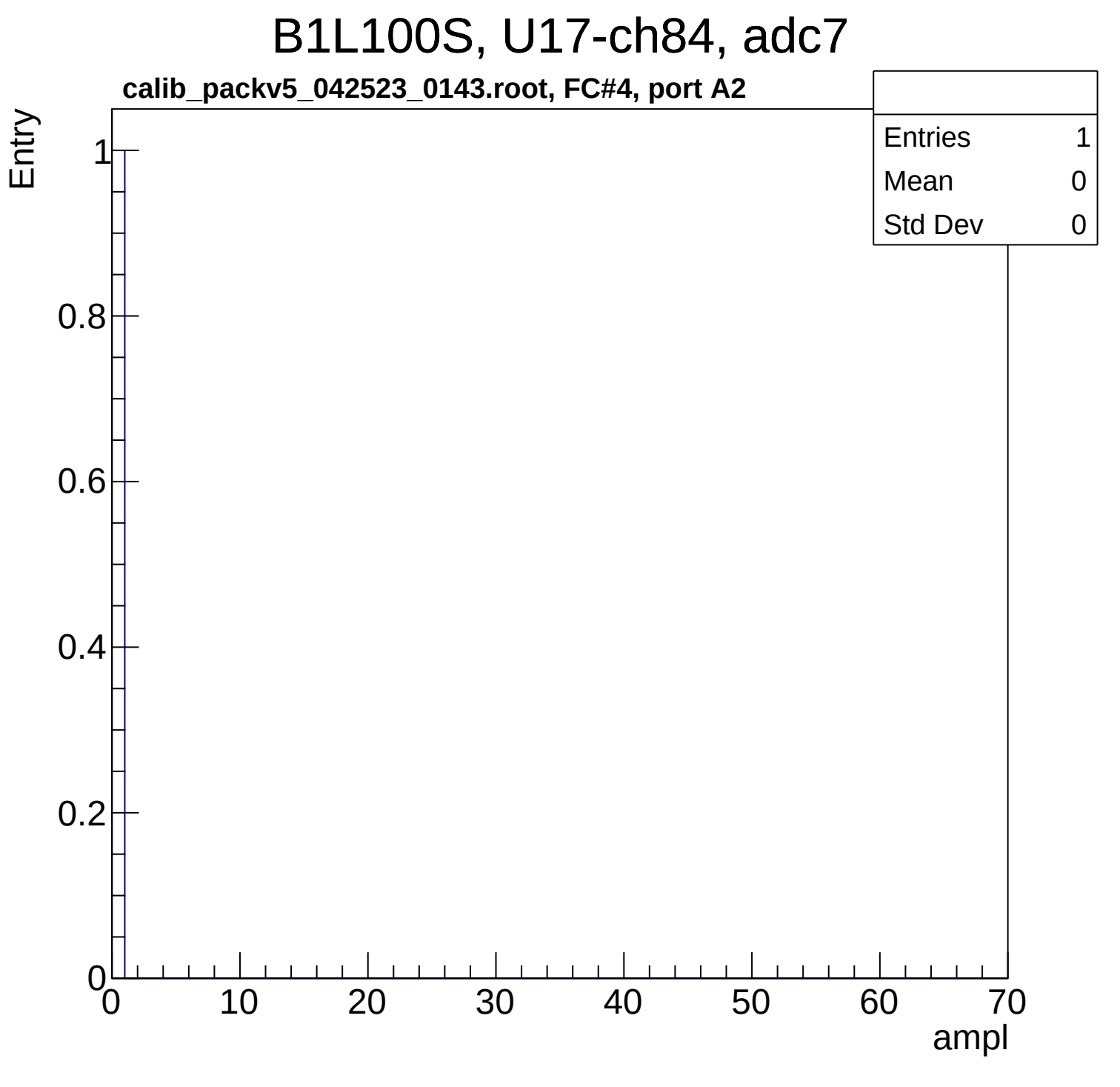
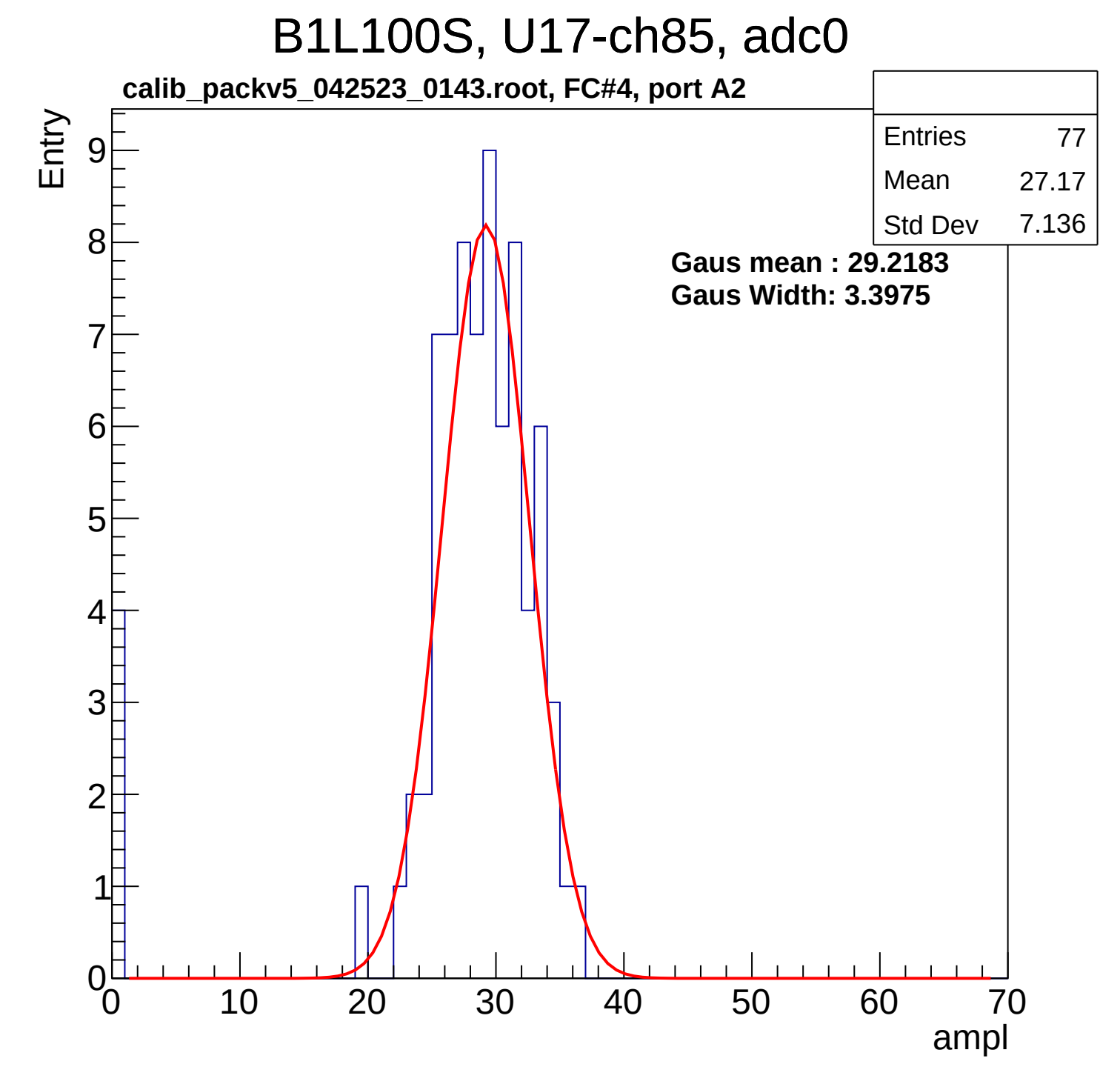
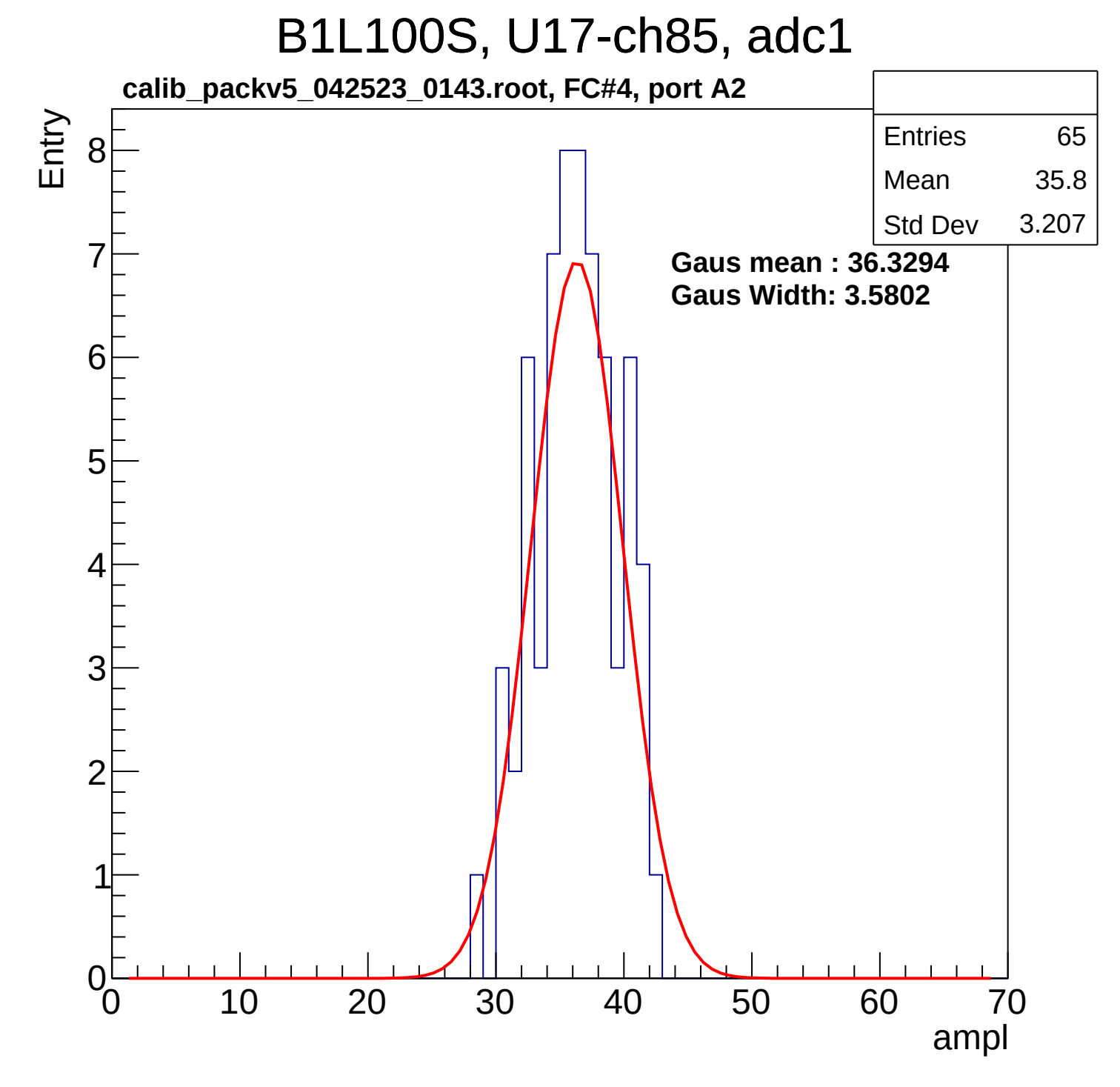

B1L100S, U17-ch84, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 14
Mean 57.71
Std Dev 16.03
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L100S, U17-ch84, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch85, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 77
Mean 27.17
Std Dev 7.136
Gaus mean : 29.2183
Gaus Width: 3.3975
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch85, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 35.8
Std Dev 3.207
Gaus mean : 36.3294
Gaus Width: 3.5802
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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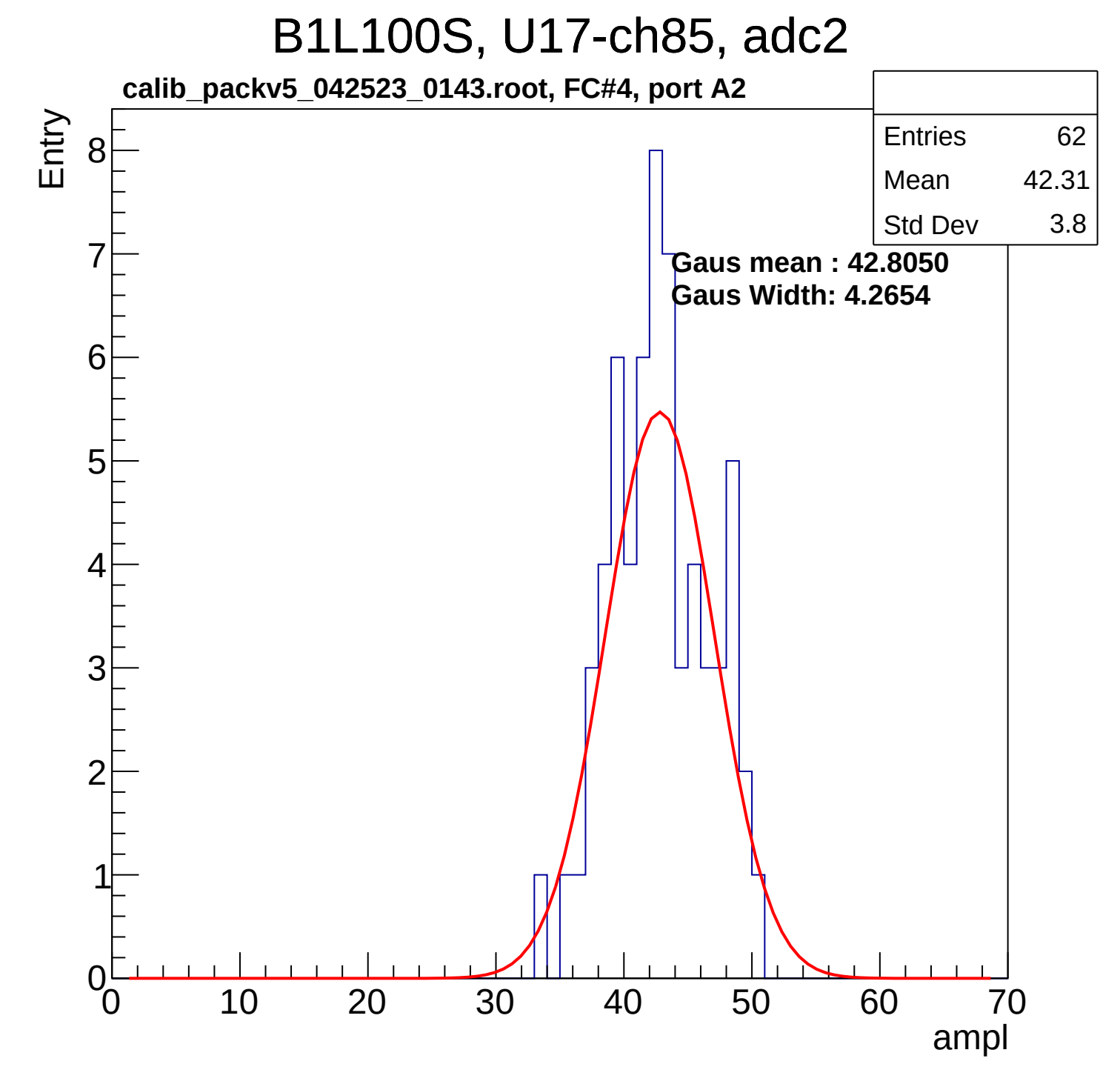
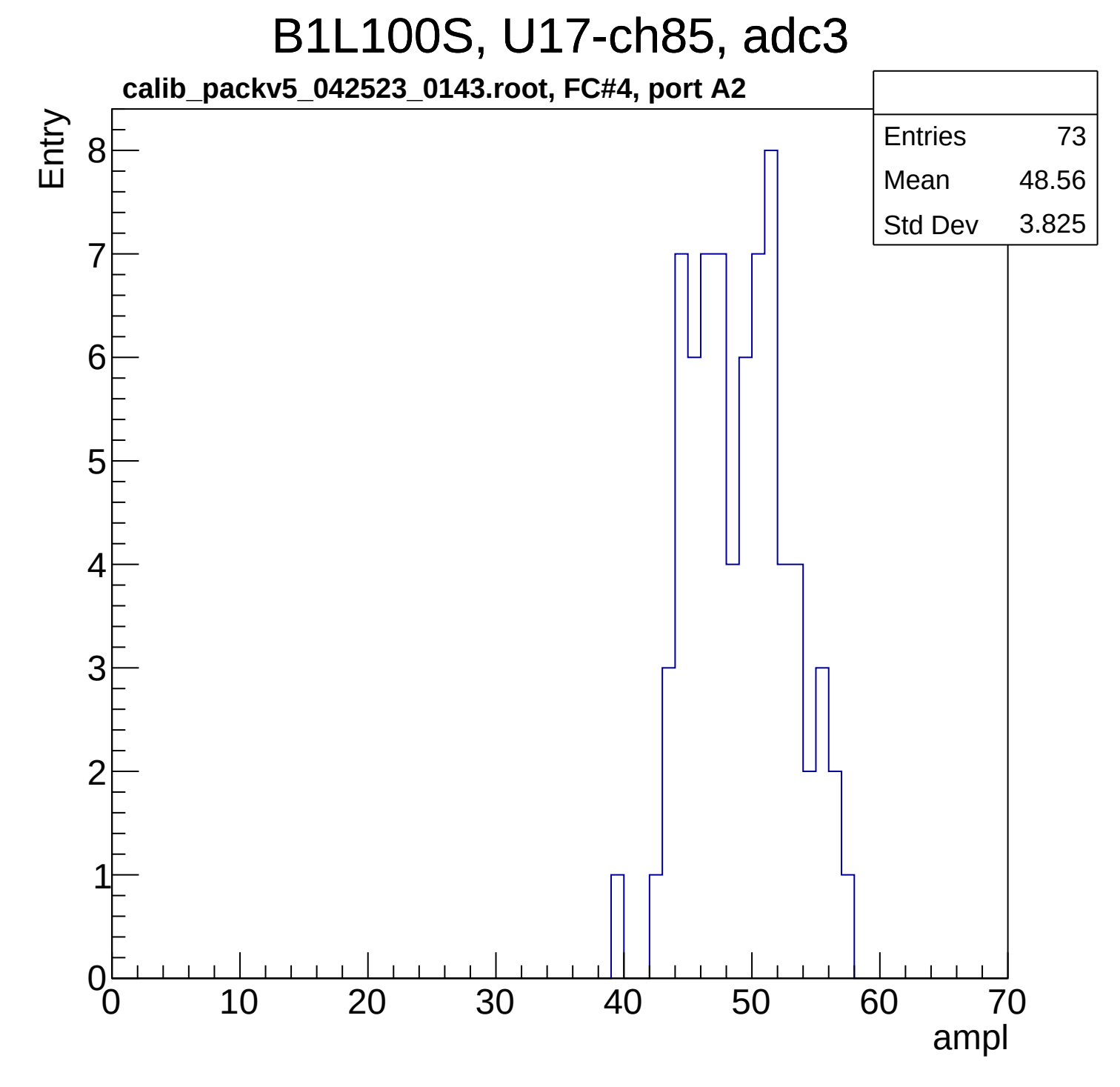
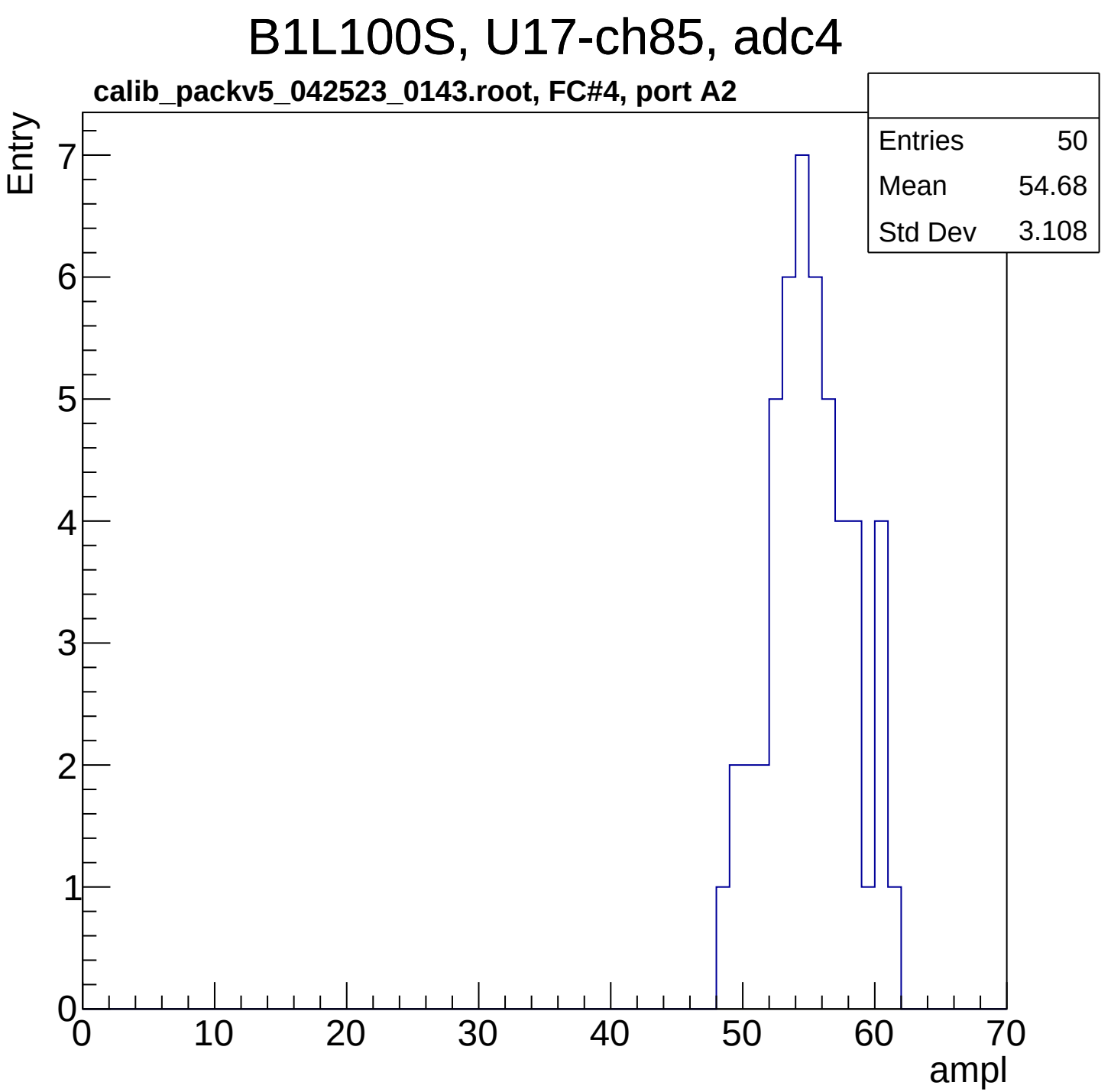
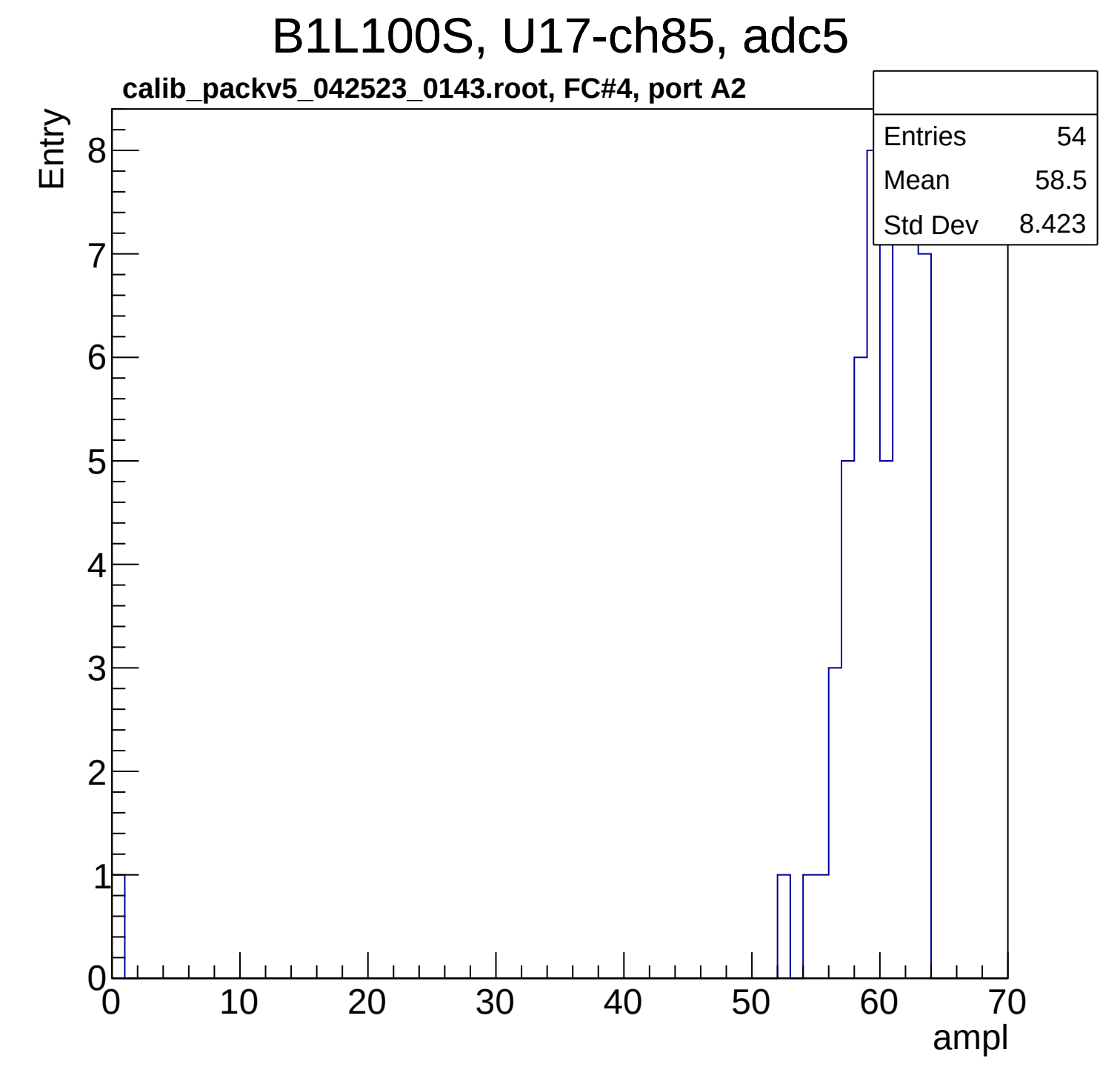
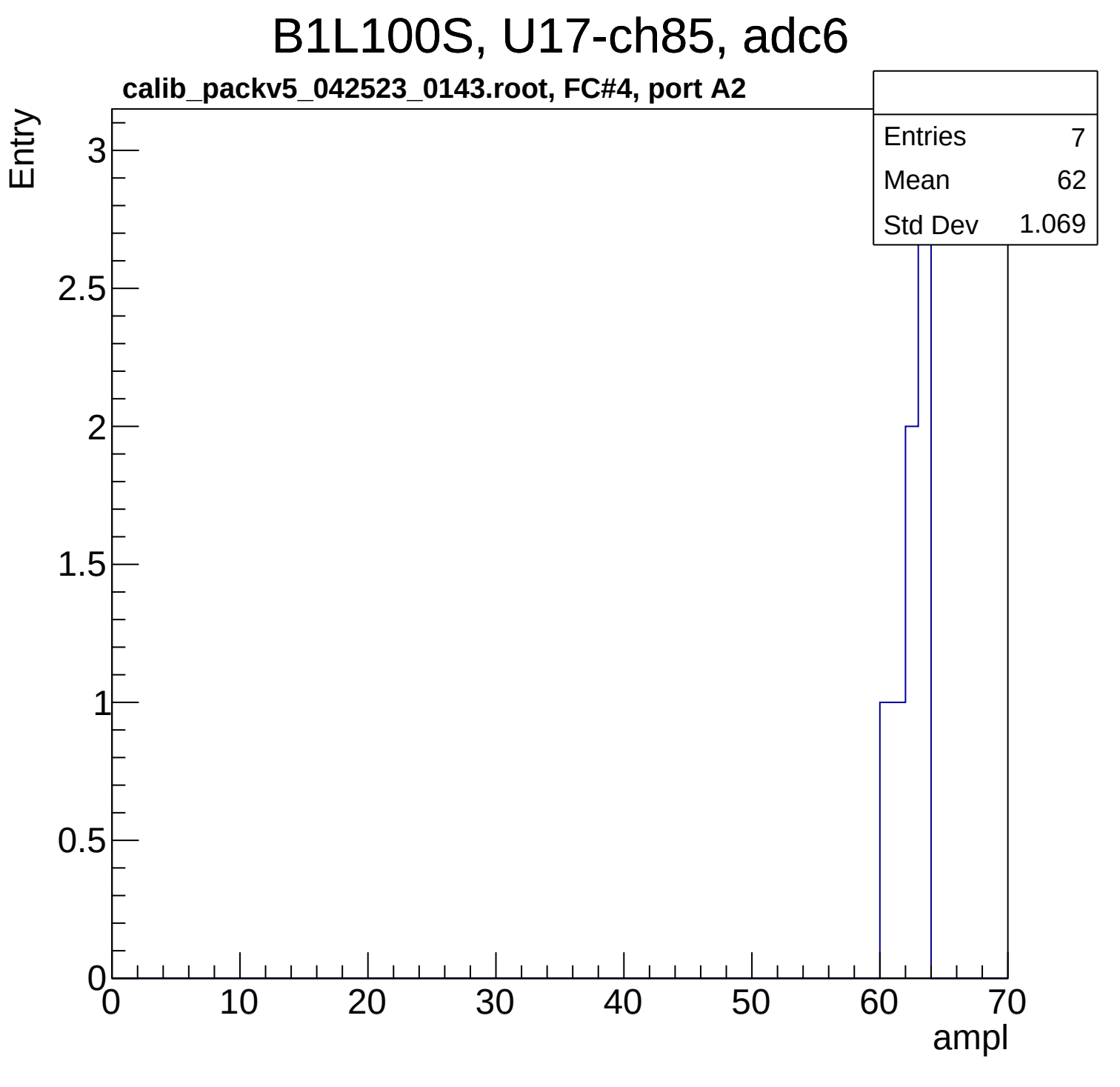
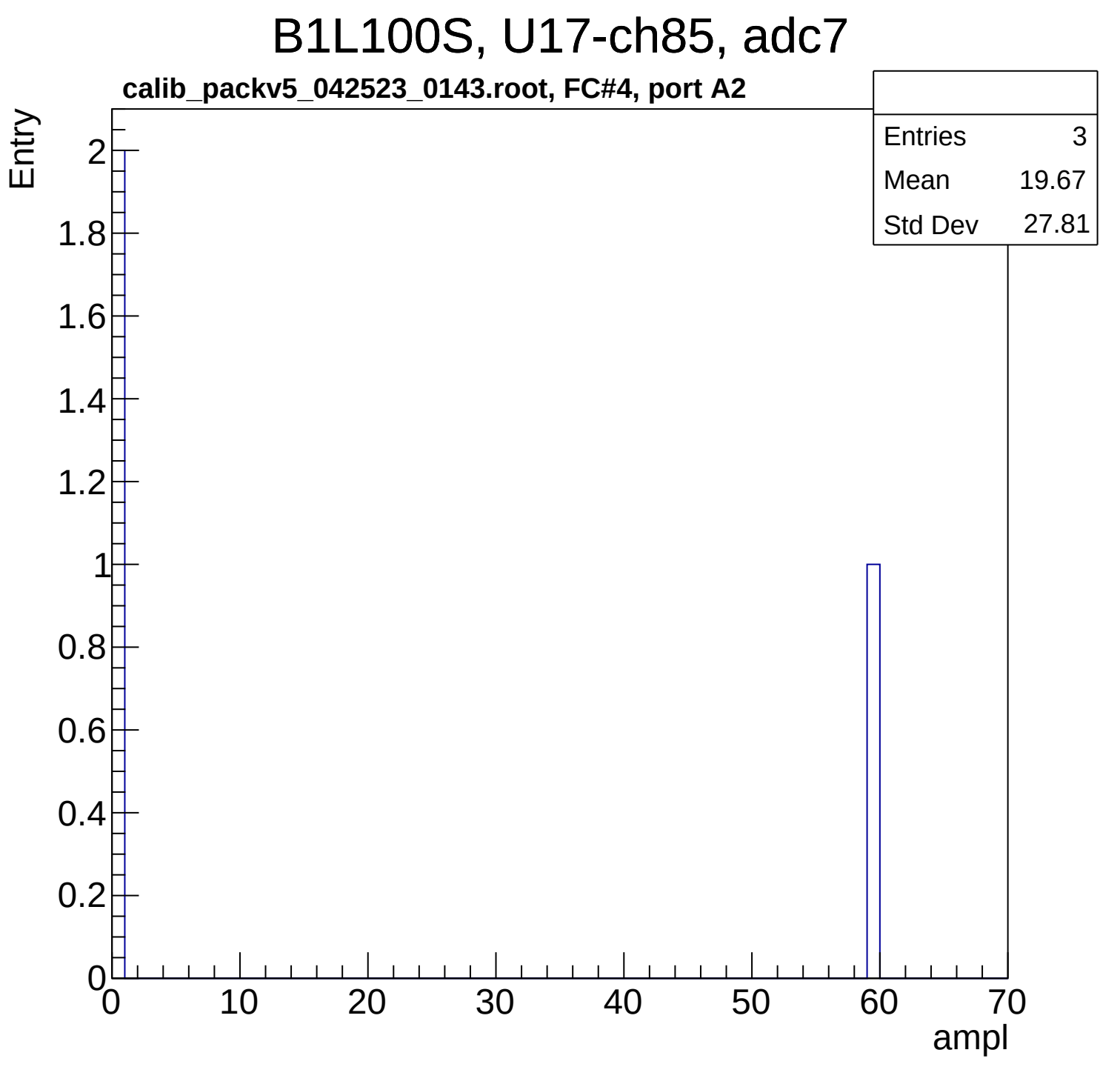

B1L100S, U17-ch85, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 42.31
Std Dev 3.8
Gaus mean : 42.8050
Gaus Width: 4.2654
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

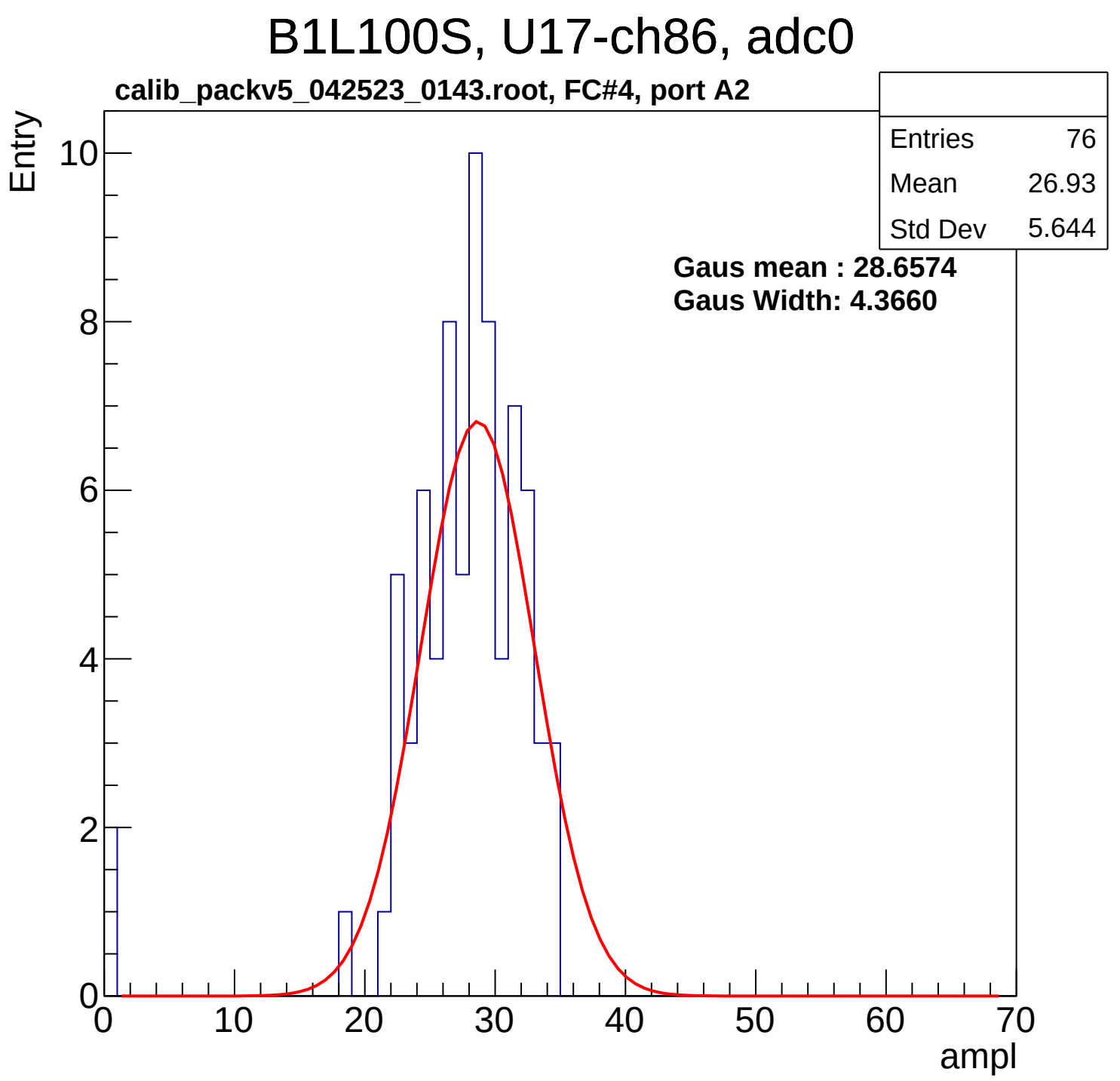

B1L100S, U17-ch85, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 48.56
Std Dev 3.825
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

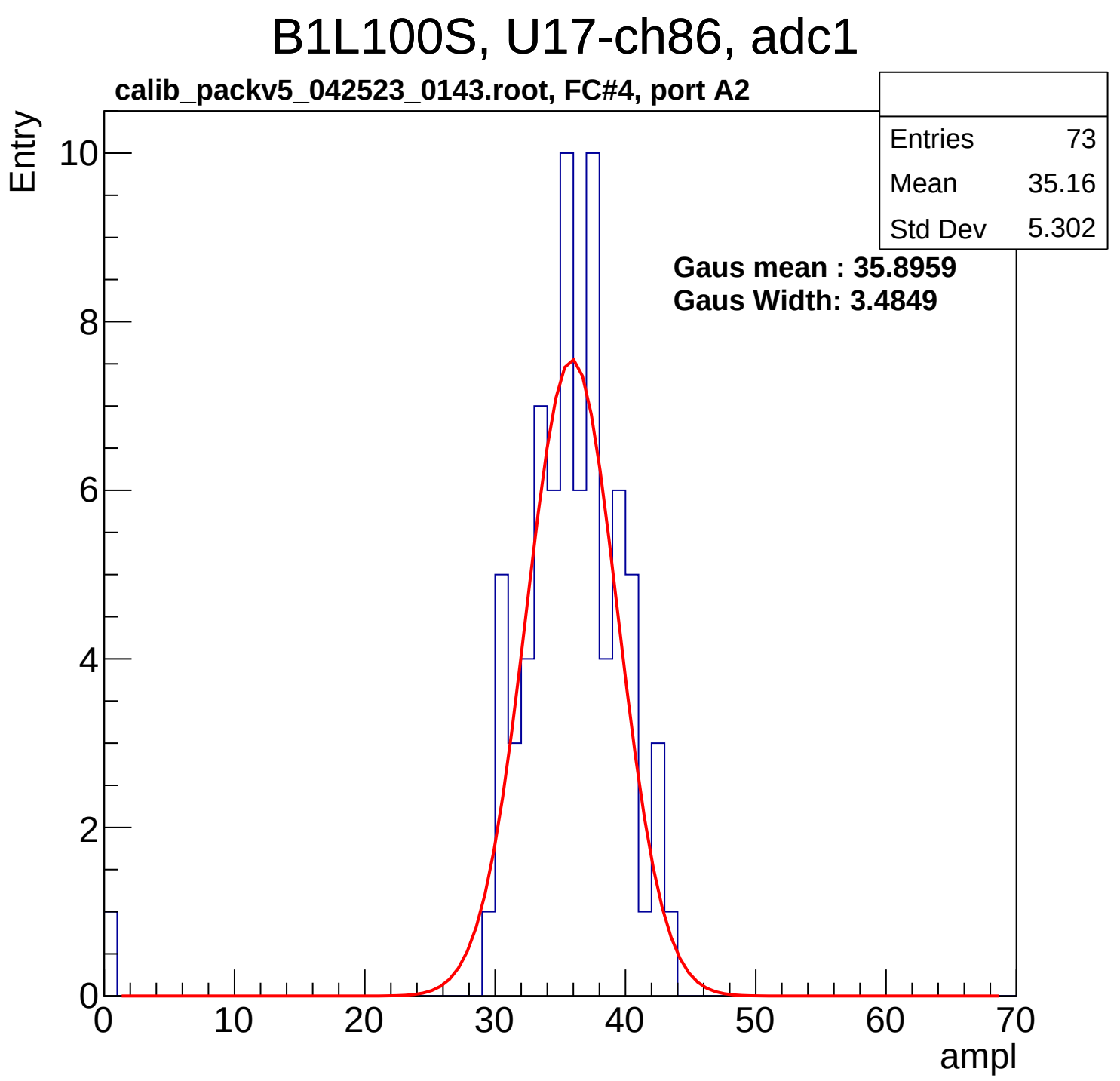

B1L100S, U17-ch85, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 54.68
Std Dev 3.108
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

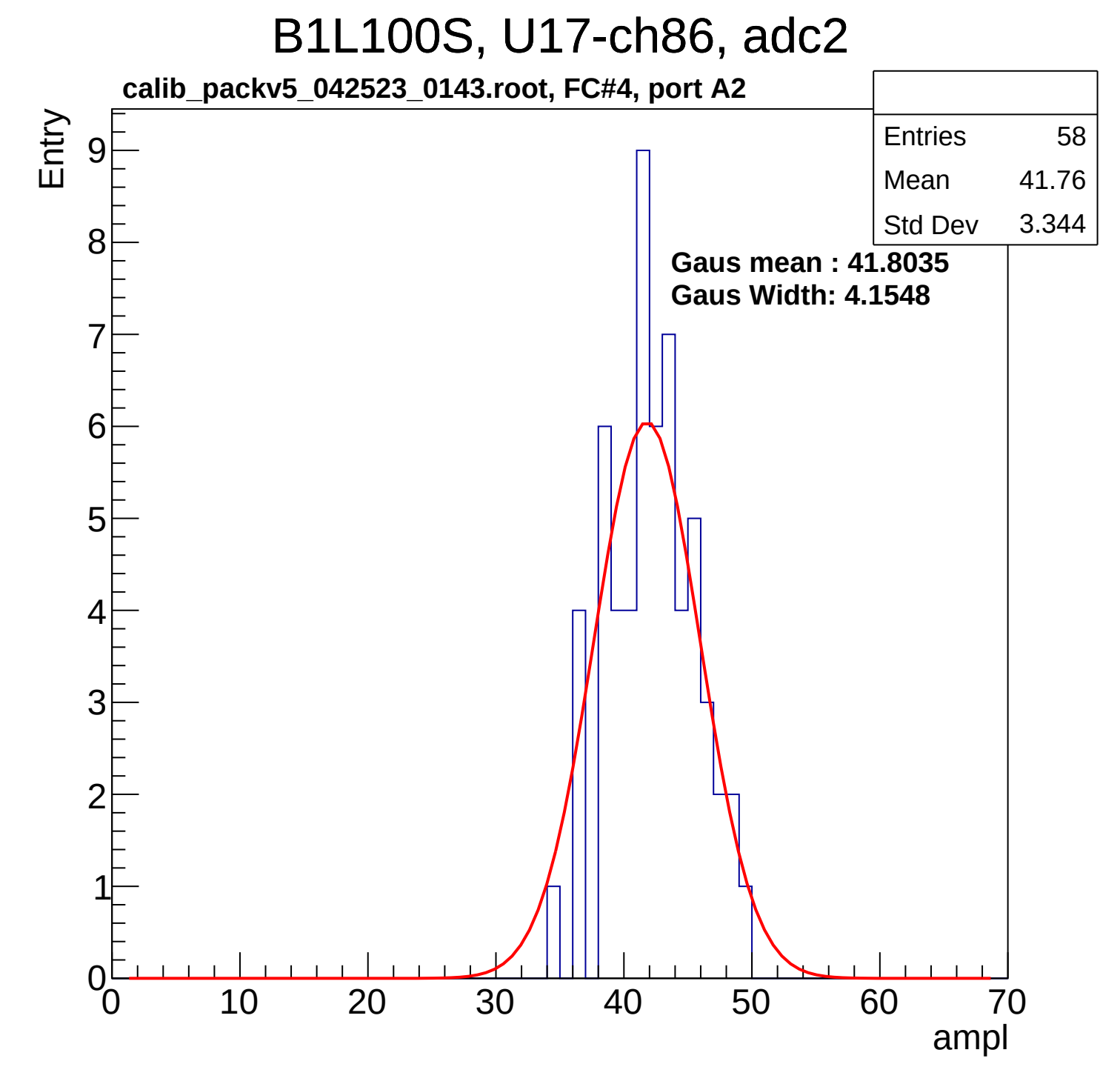

B1L100S, U17-ch85, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 58.5
Std Dev 8.423
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch85, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 7
Mean 62
Std Dev 1.069
Entry
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch85, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 19.67
Std Dev 27.81
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L100S, U17-ch86, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 76
Mean 26.93
Std Dev 5.644
Gaus mean : 28.6574
Gaus Width: 4.3660
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U17-ch86, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 35.16
Std Dev 5.302
Gaus mean : 35.8959
Gaus Width: 3.4849
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U17-ch86, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 41.76
Std Dev 3.344
Gaus mean : 41.8035
Gaus Width: 4.1548
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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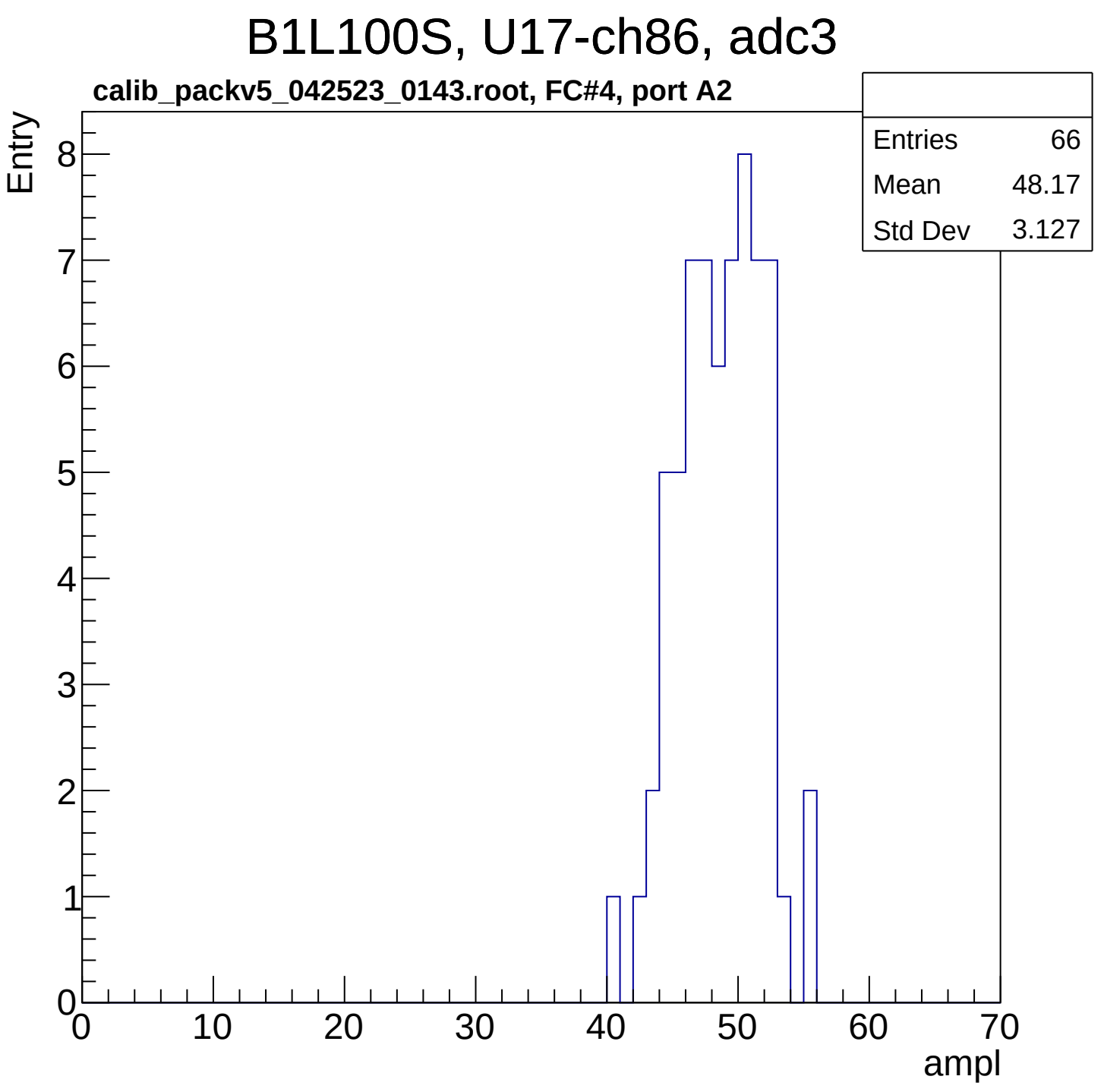
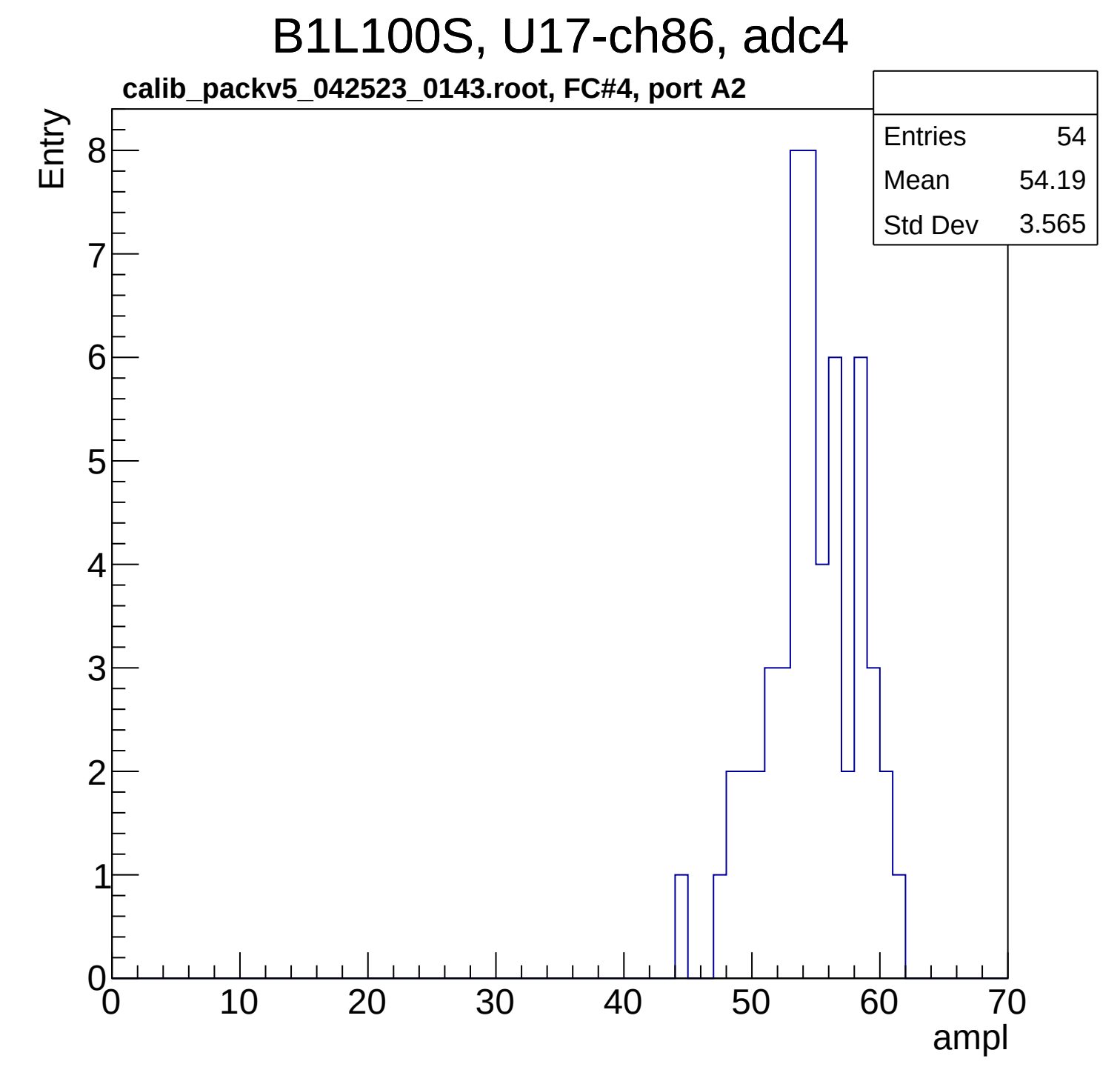
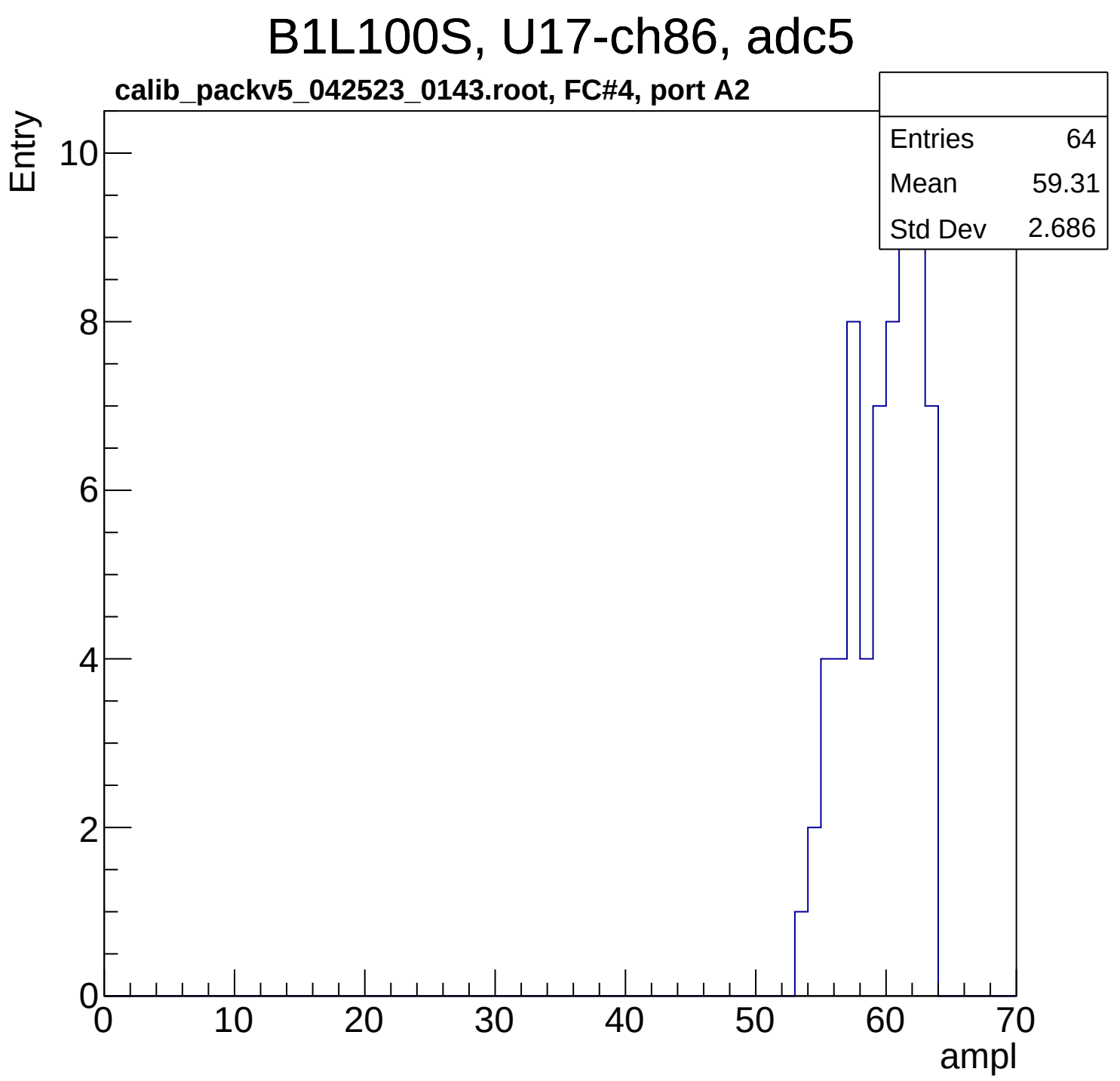
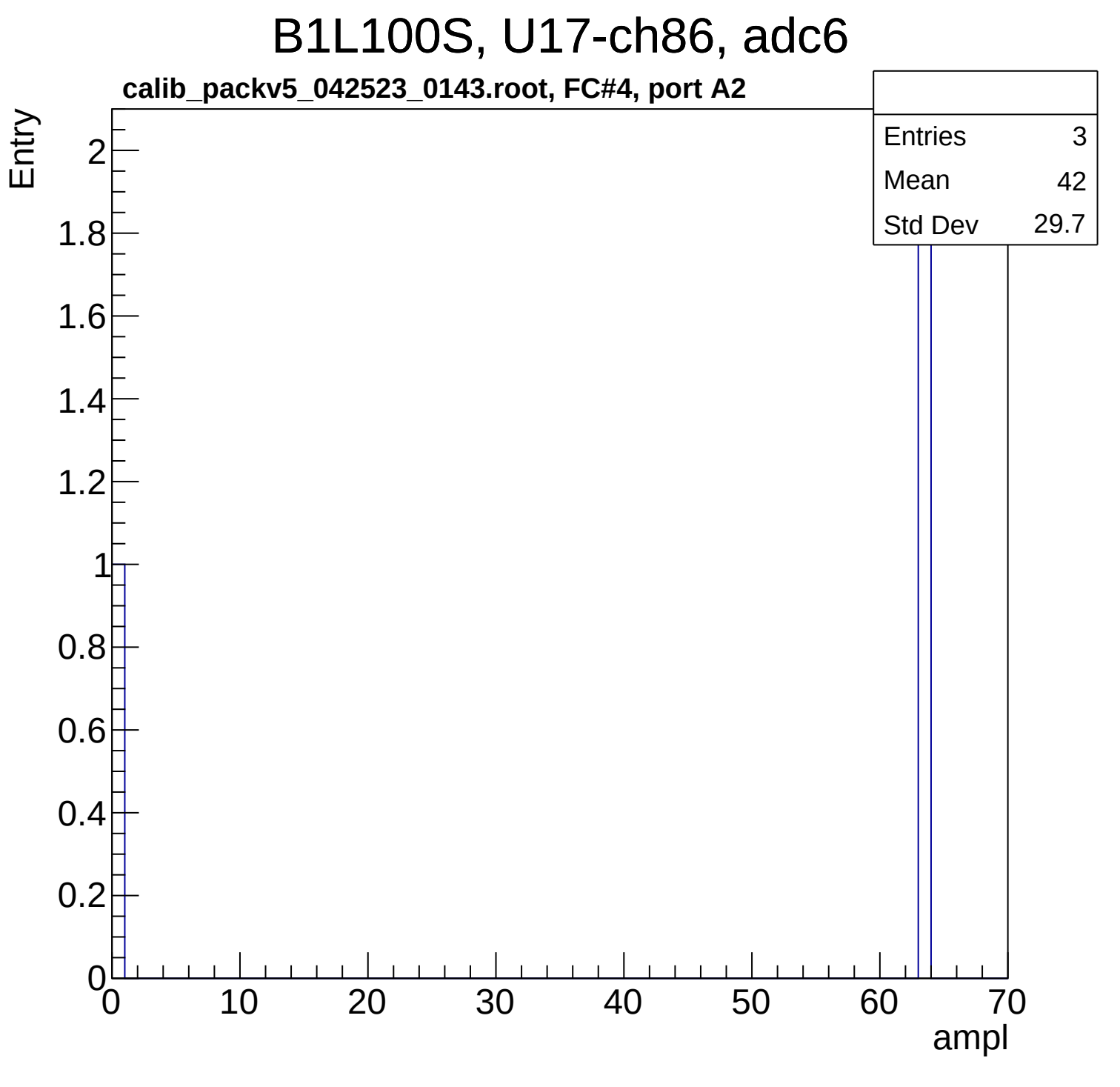
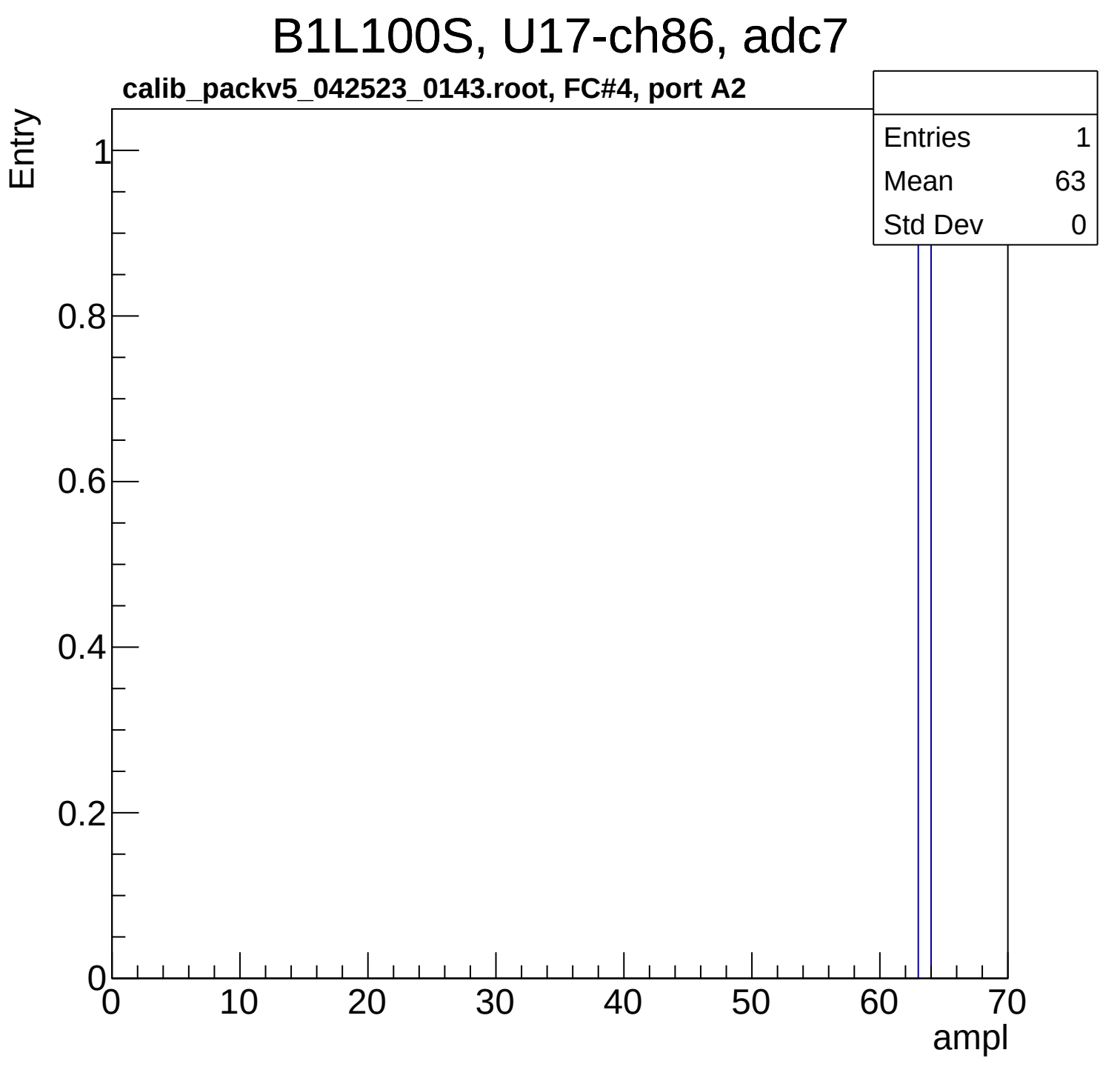
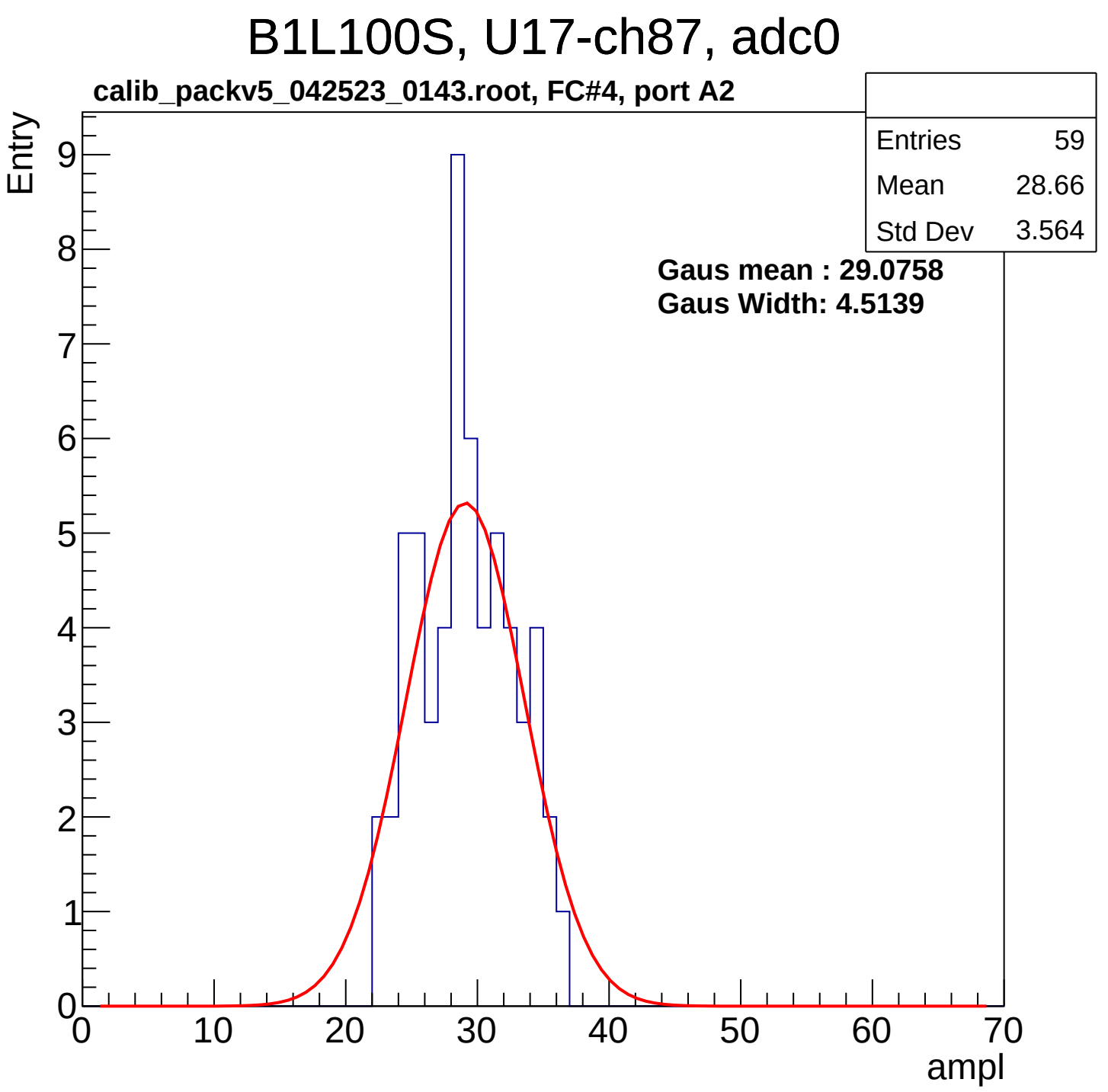

B1L100S, U17-ch86, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 48.17
Std Dev 3.127
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch86, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 54.19
Std Dev 3.565
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch86, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 59.31
Std Dev 2.686
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U17-ch86, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 42
Std Dev 29.7
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L100S, U17-ch86, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch87, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 28.66
Std Dev 3.564
Gaus mean : 29.0758
Gaus Width: 4.5139
Entry
ampl
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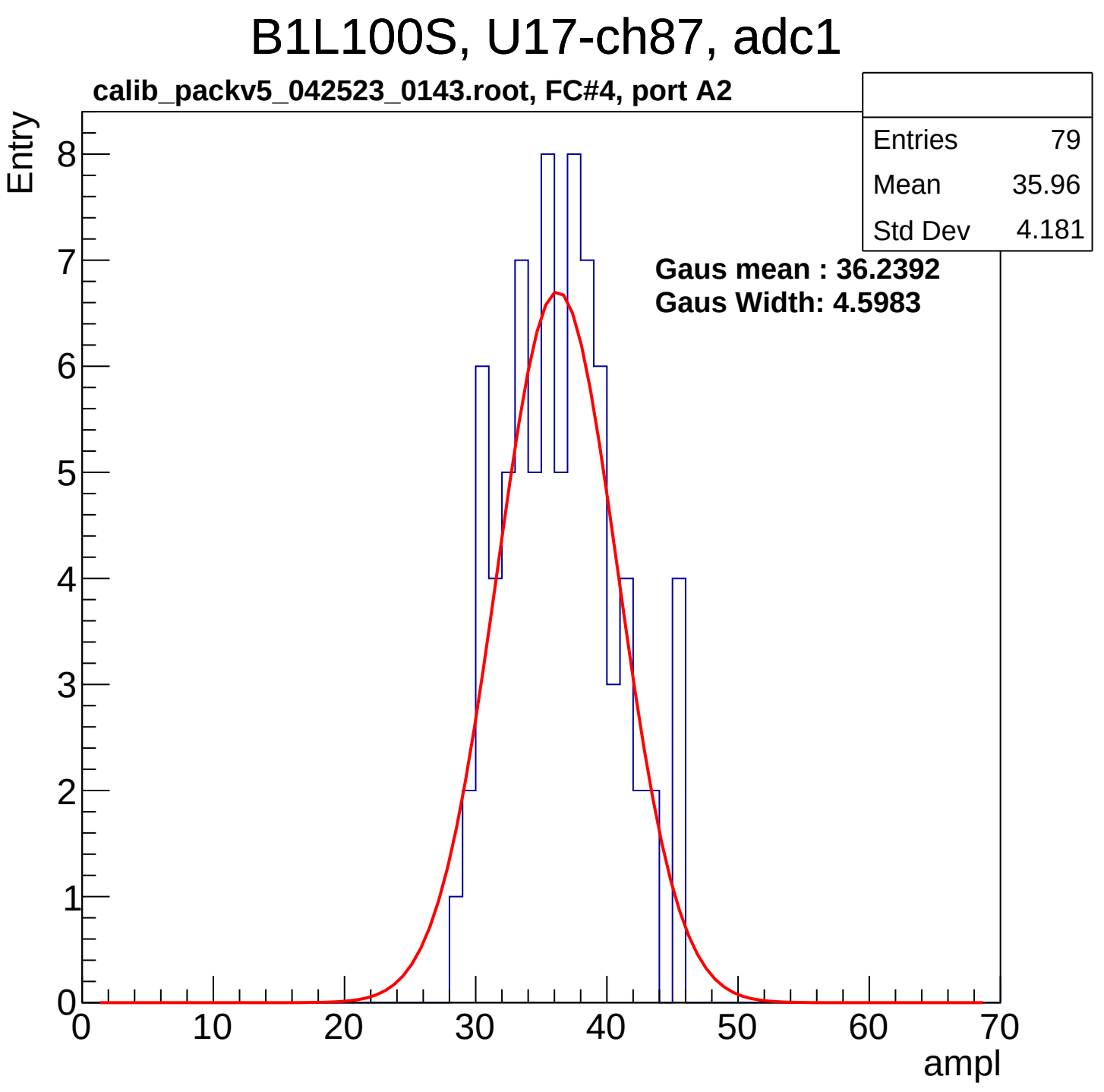
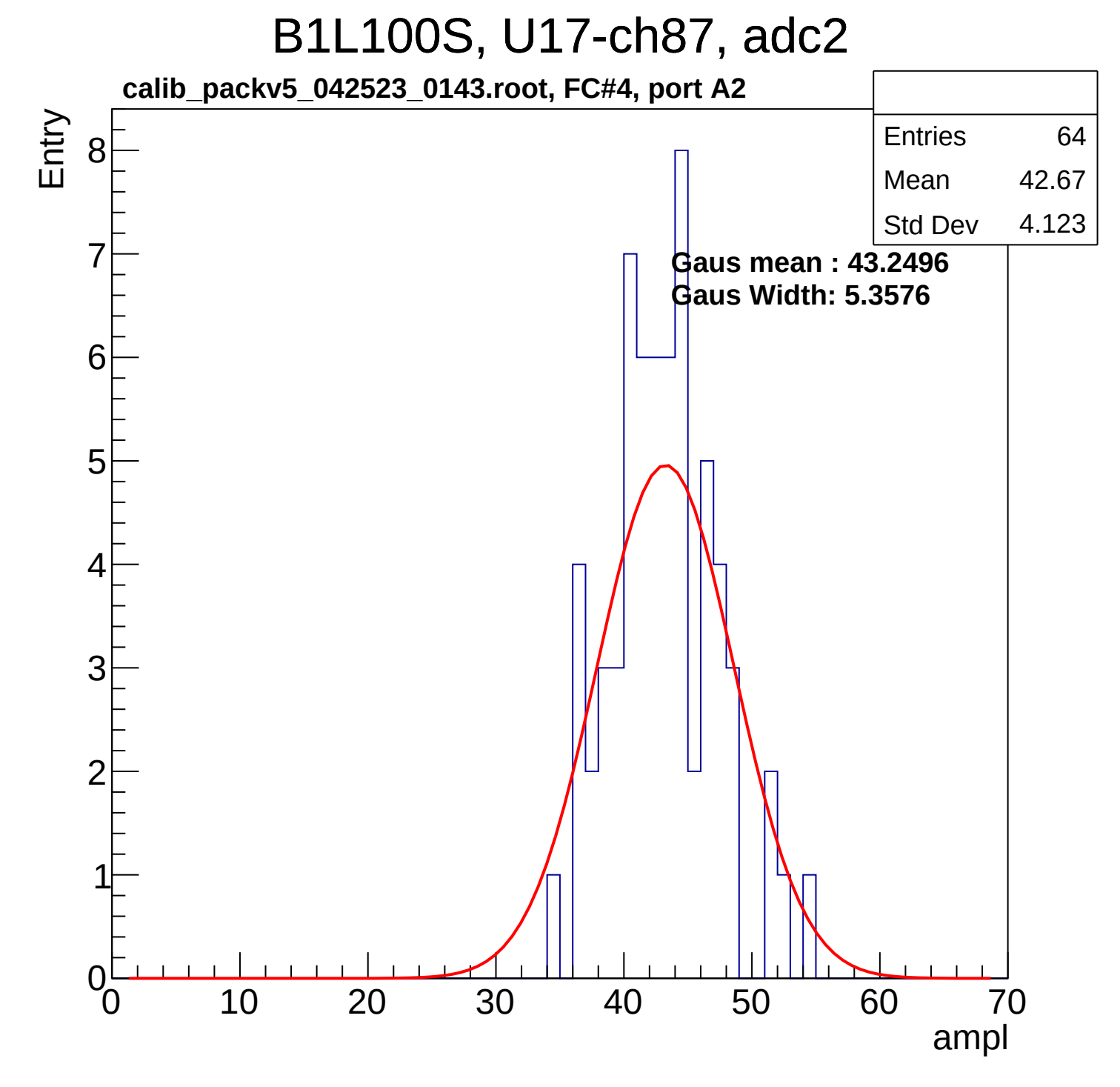
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch87, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 79
Mean 35.96
Std Dev 4.181
Gaus mean : 36.2392
Gaus Width: 4.5983
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch87, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 42.67
Std Dev 4.123
Gaus mean : 43.2496
Gaus Width: 5.3576
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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20
30
40
50
60
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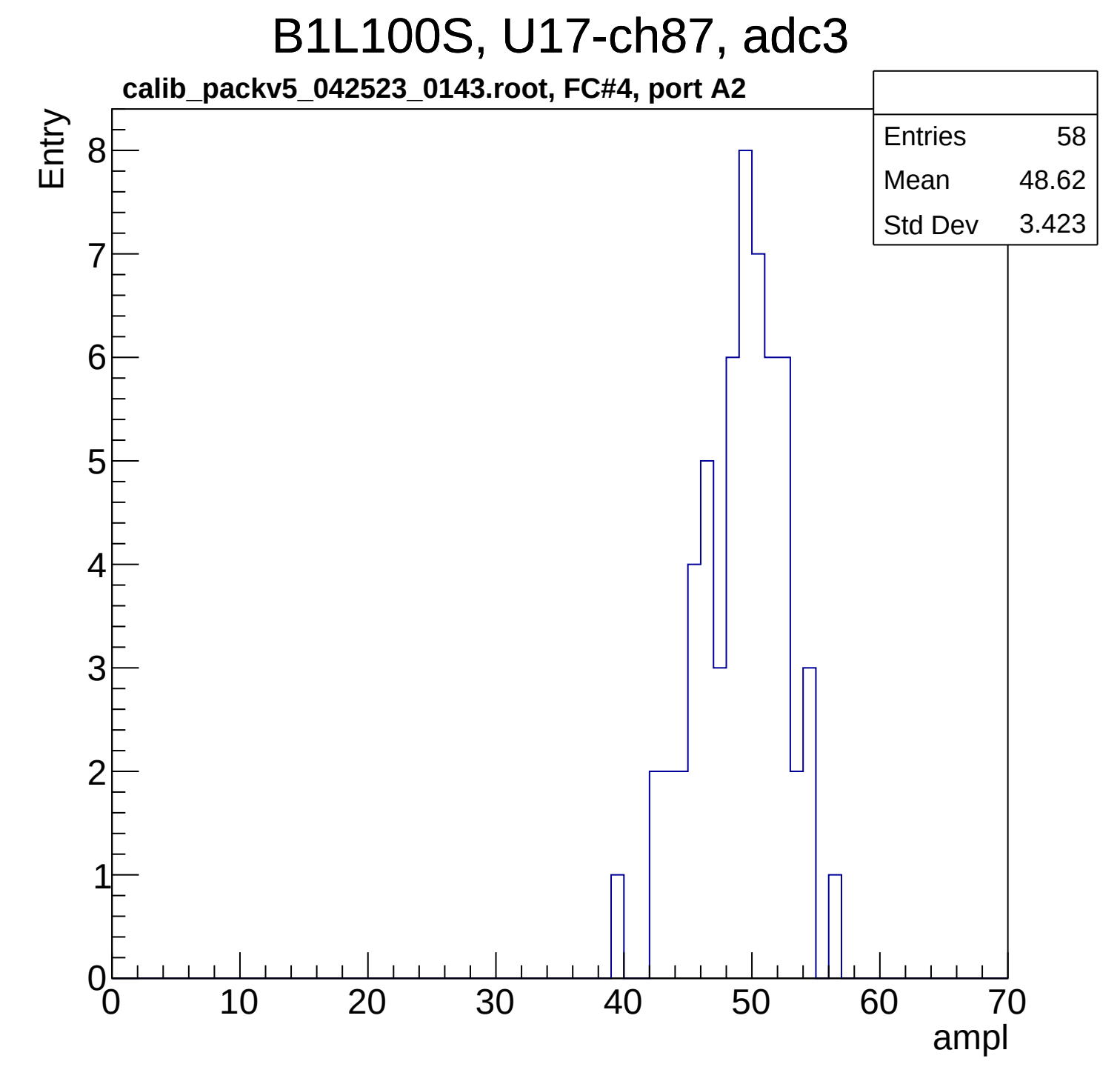
B1L100S, U17-ch87, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 48.62
Std Dev 3.423
Entry
ampl
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2
3
4
5
6
7
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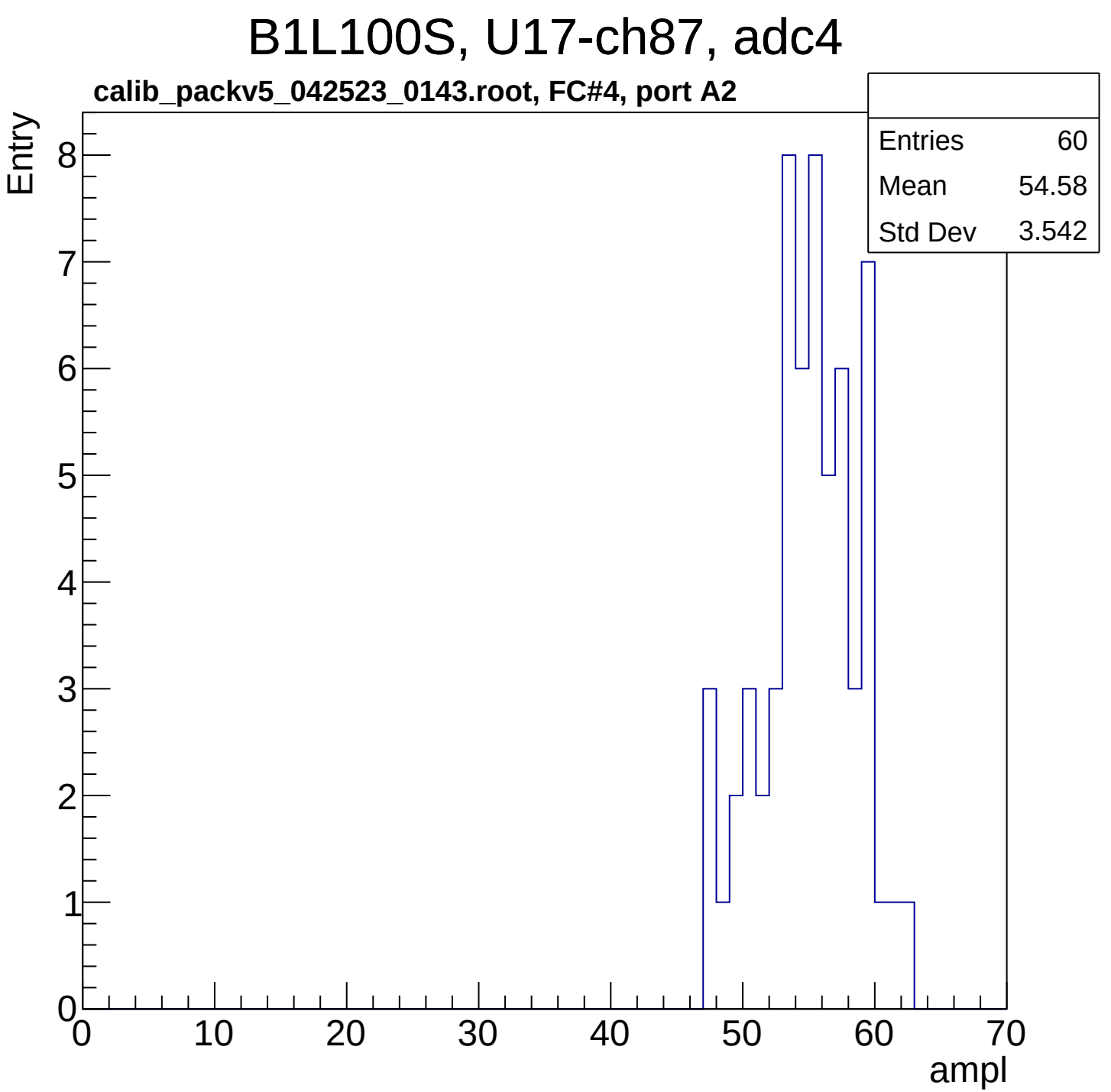
0
10
20
30
40
50
60
70


B1L100S, U17-ch87, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 54.58
Std Dev 3.542
Entry
ampl
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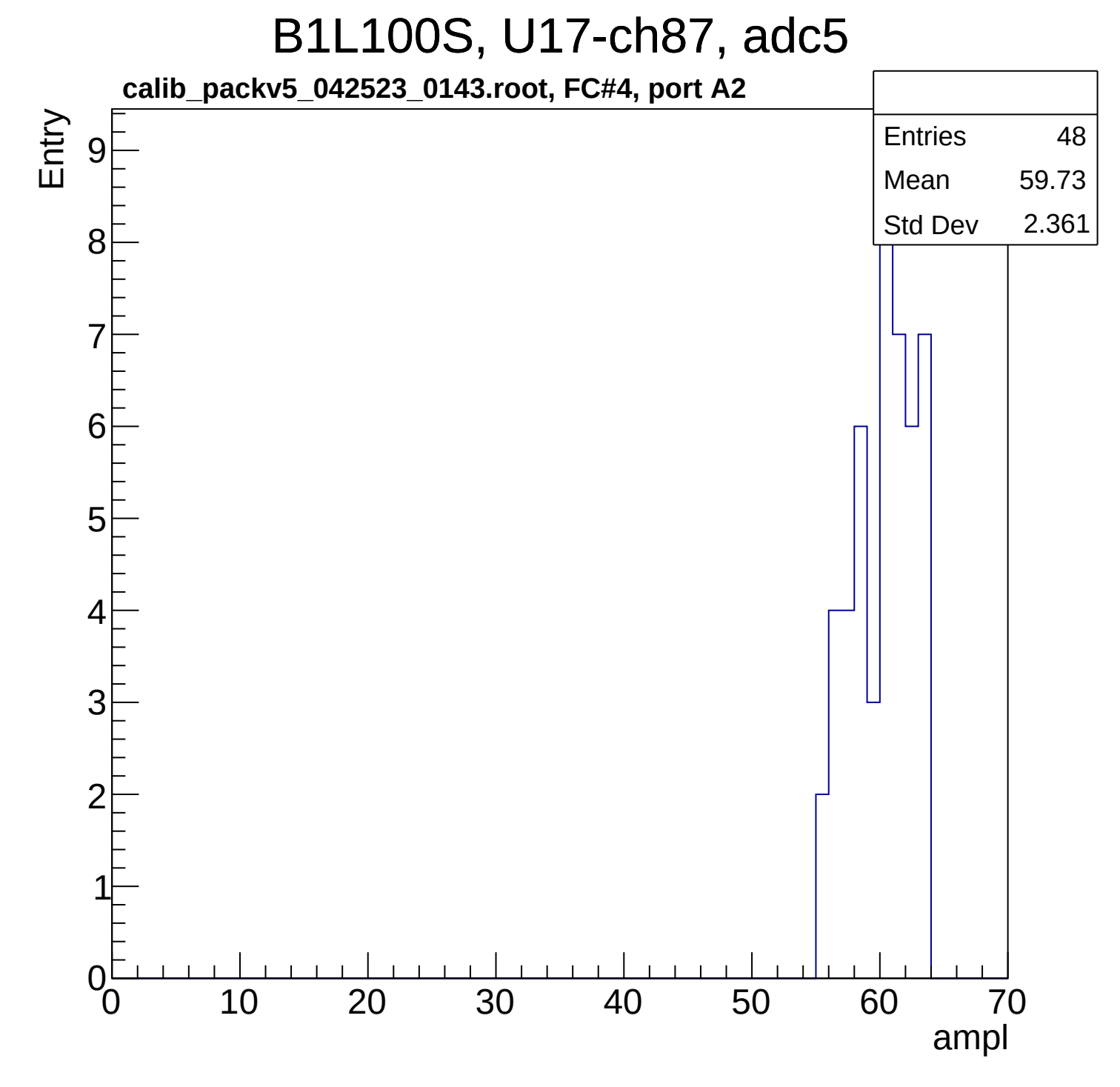
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch87, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 48
Mean 59.73
Std Dev 2.361
Entry
ampl
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2
3
4
5
6
7
8
9
0
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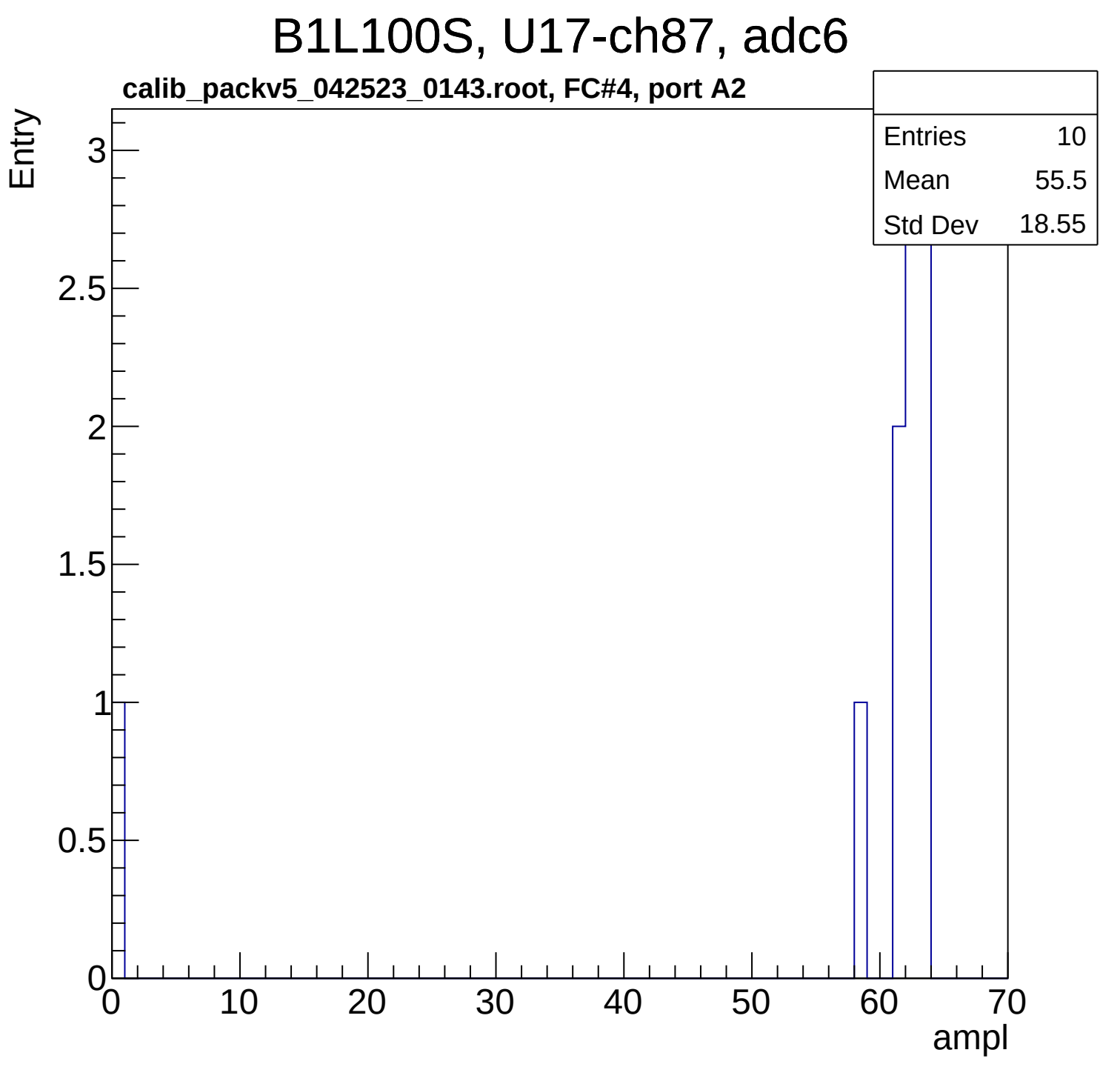
20
30
40
50
60
70


B1L100S, U17-ch87, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 10
Mean 55.5
Std Dev 18.55
Entry
ampl
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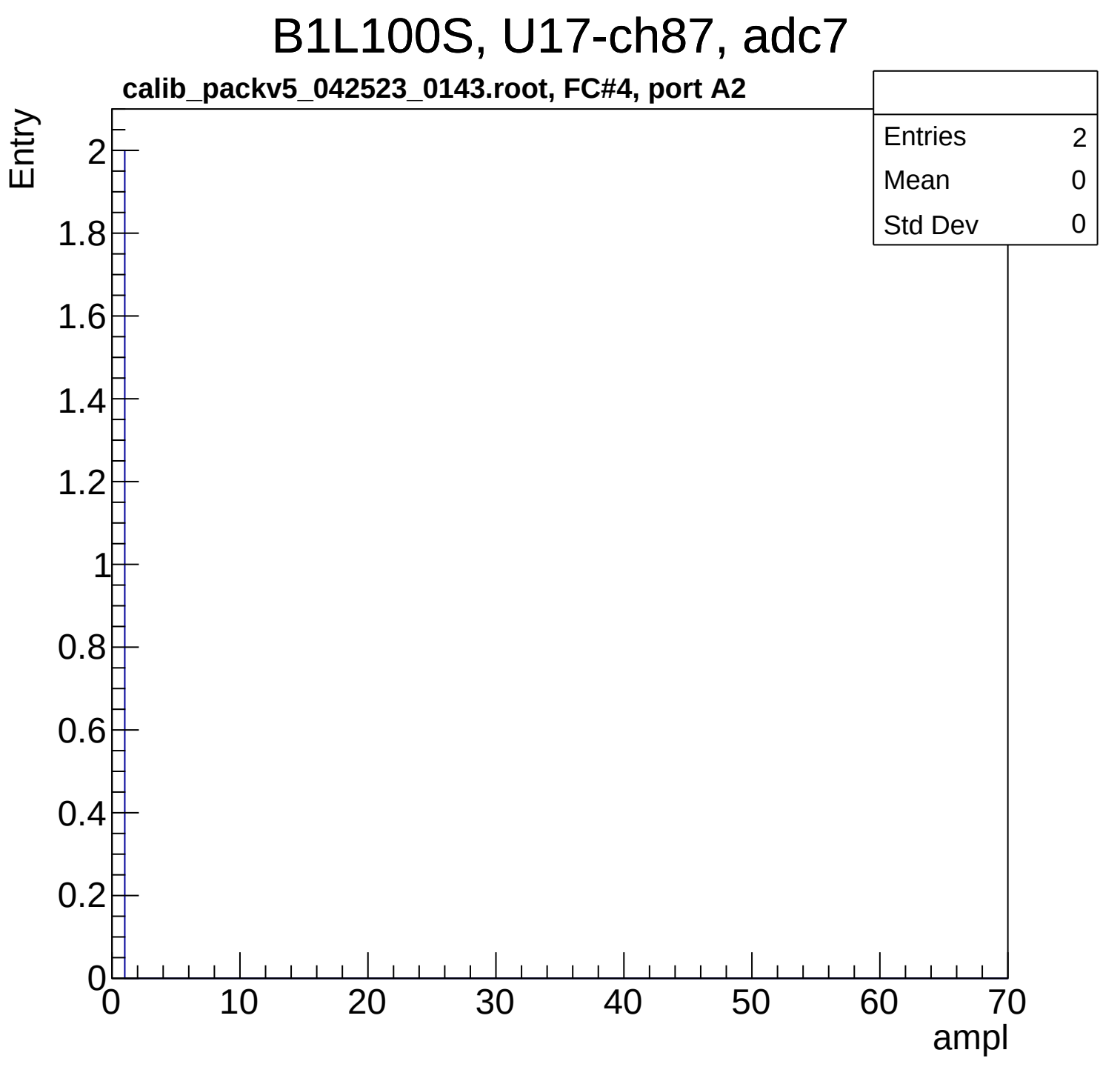
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L100S, U17-ch87, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
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0.8
0.6
0.4
0.2
0
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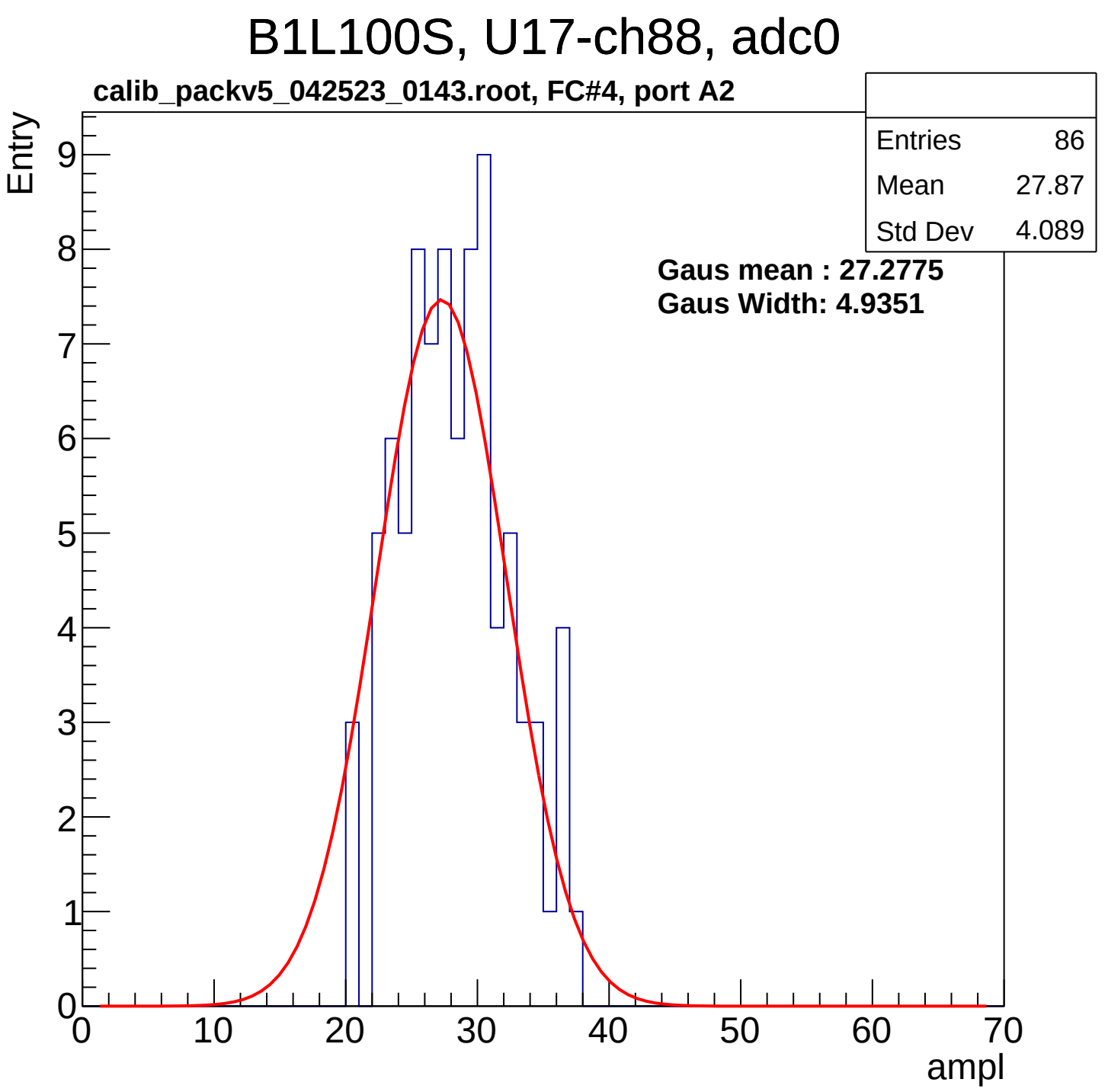
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch88, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 86
Mean 27.87
Std Dev 4.089
Gaus mean : 27.2775
Gaus Width: 4.9351
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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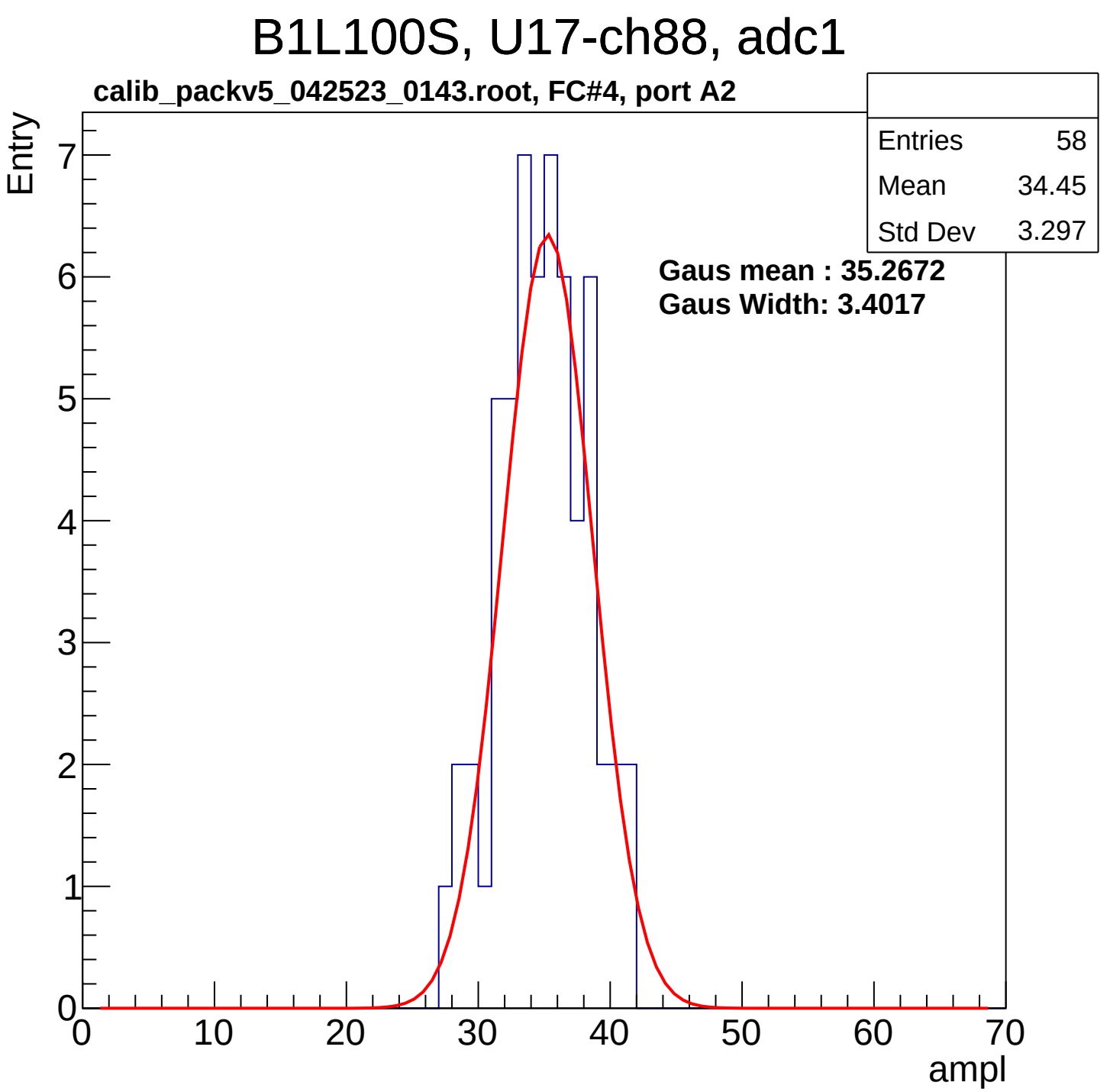
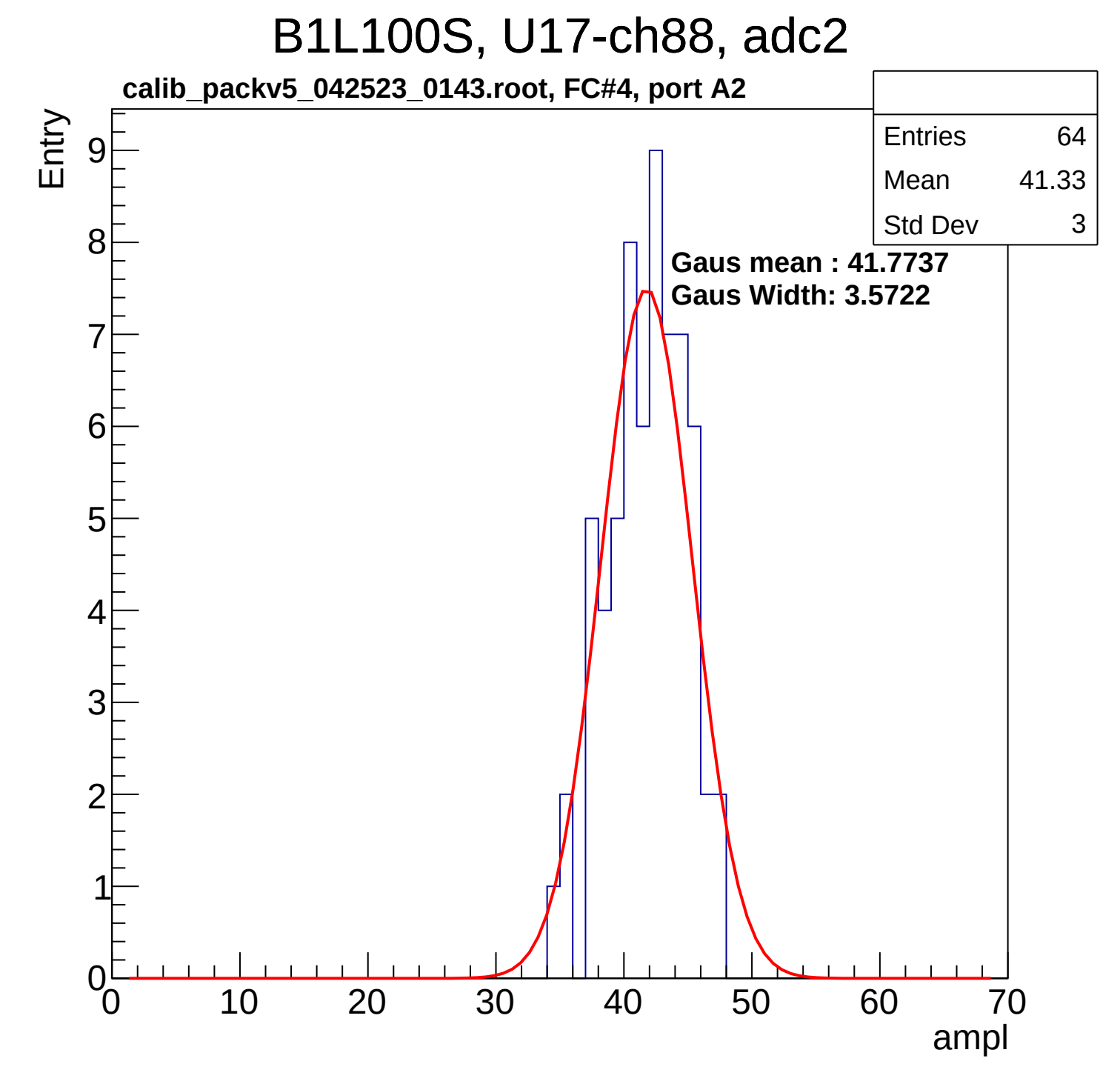

B1L100S, U17-ch88, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 34.45
Std Dev 3.297
Gaus mean : 35.2672
Gaus Width: 3.4017
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U17-ch88, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 41.33
Std Dev 3
Gaus mean : 41.7737
Gaus Width: 3.5722
Entry
ampl
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10
20
30
40
50
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1
2
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4
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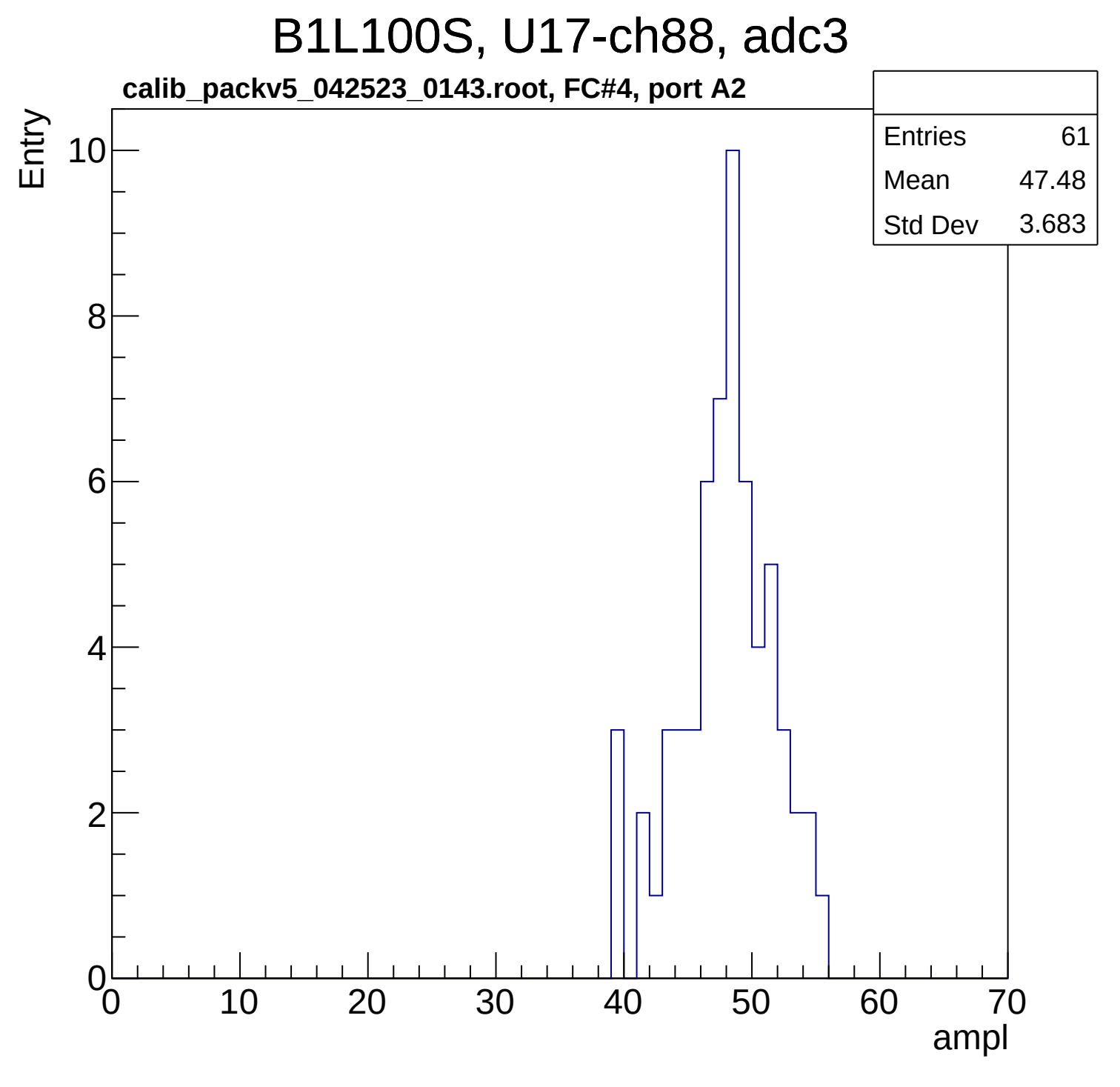
6
7
8
9


B1L100S, U17-ch88, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 47.48
Std Dev 3.683
Entry
ampl
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2
4
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8
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0
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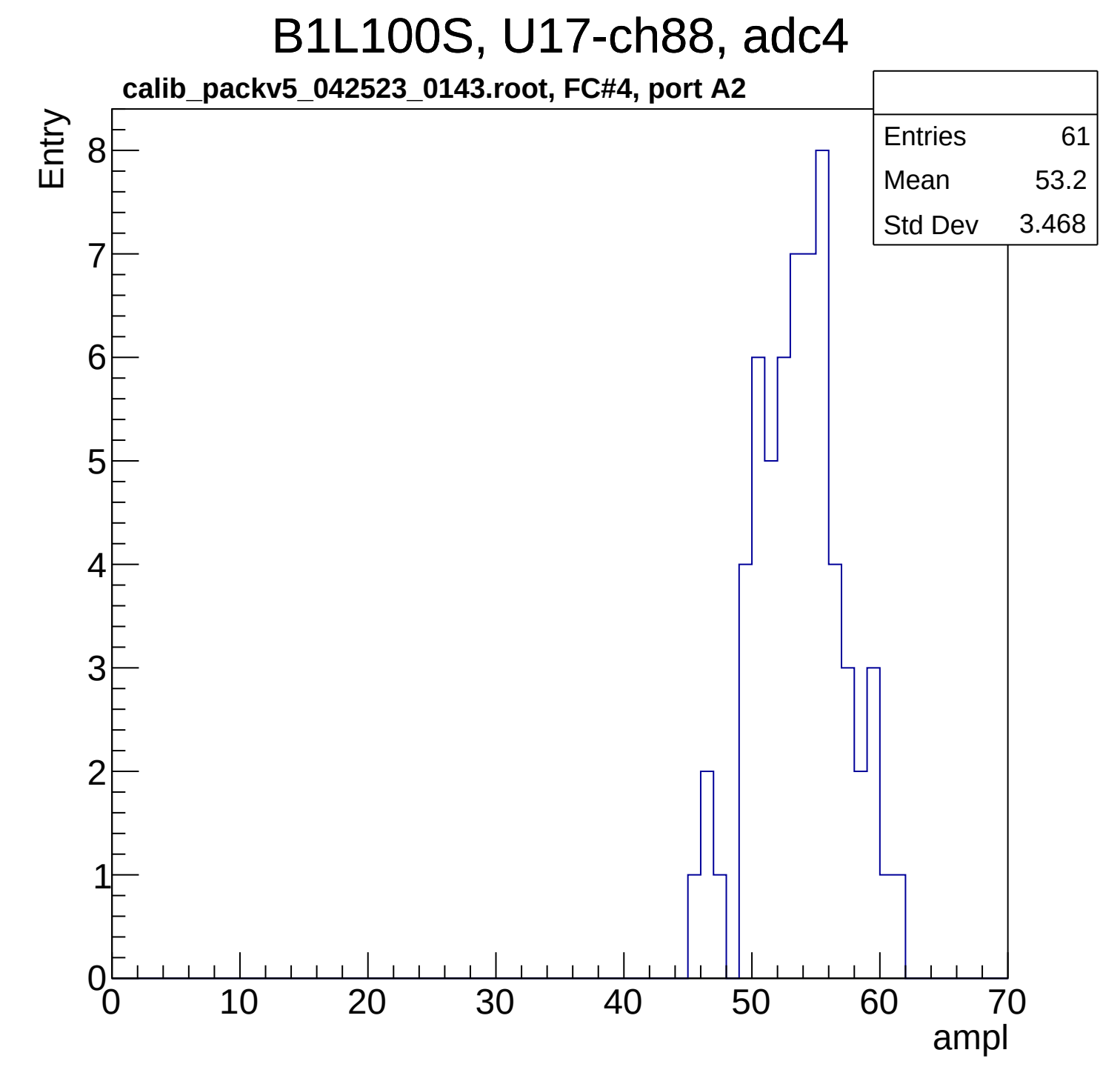
40
50
60
70


B1L100S, U17-ch88, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 53.2
Std Dev 3.468
Entry
ampl
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2
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60
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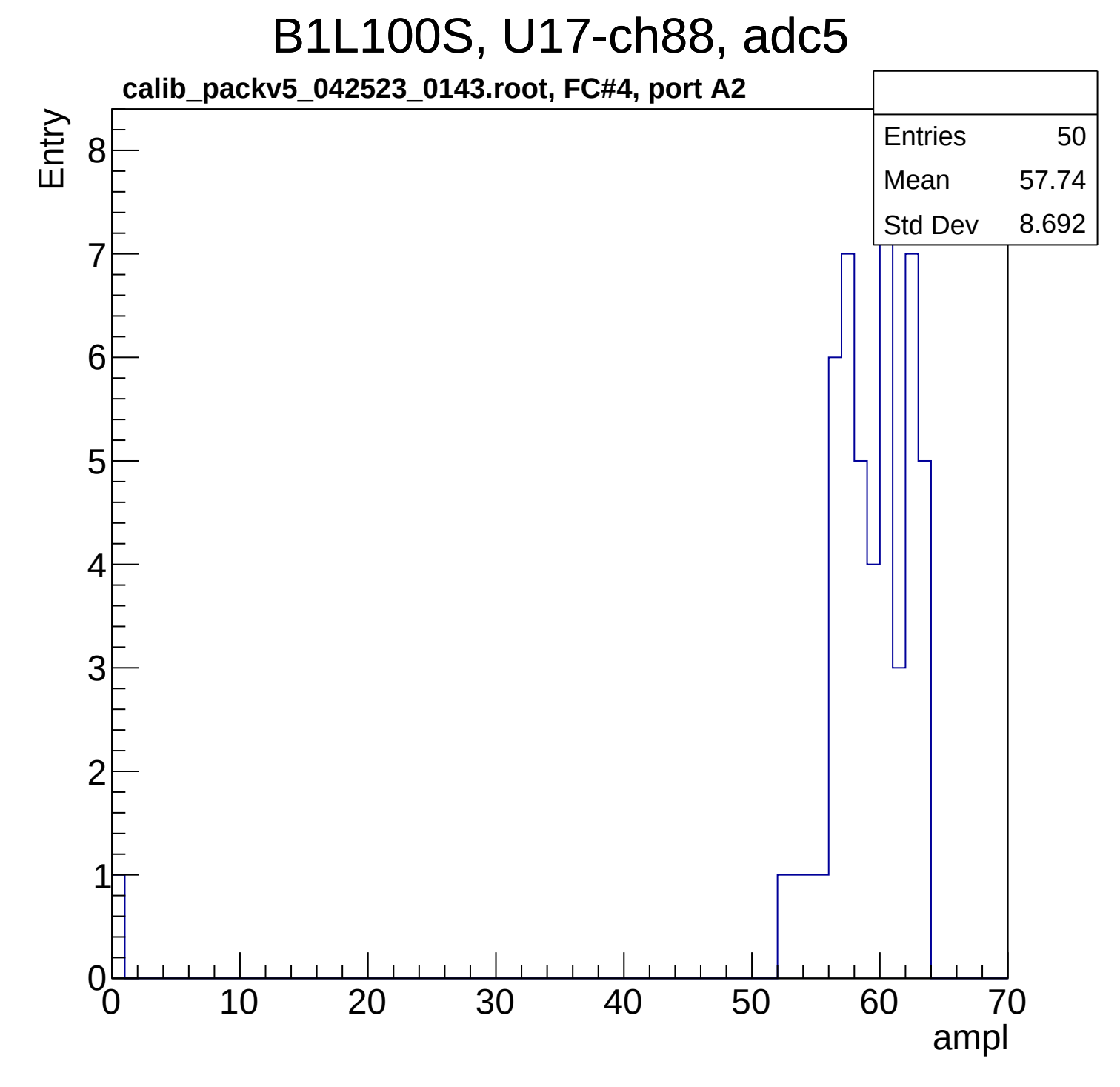
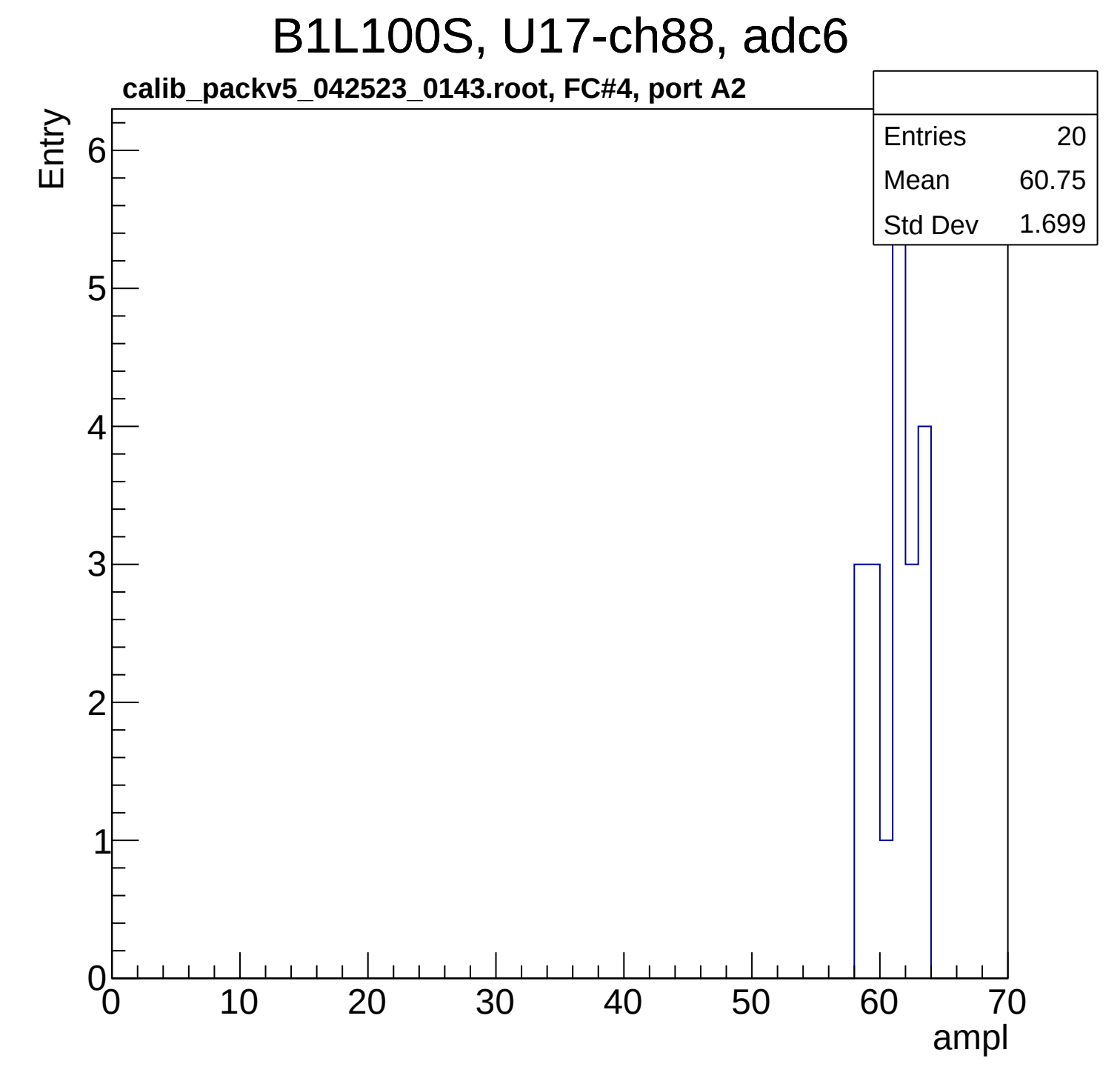
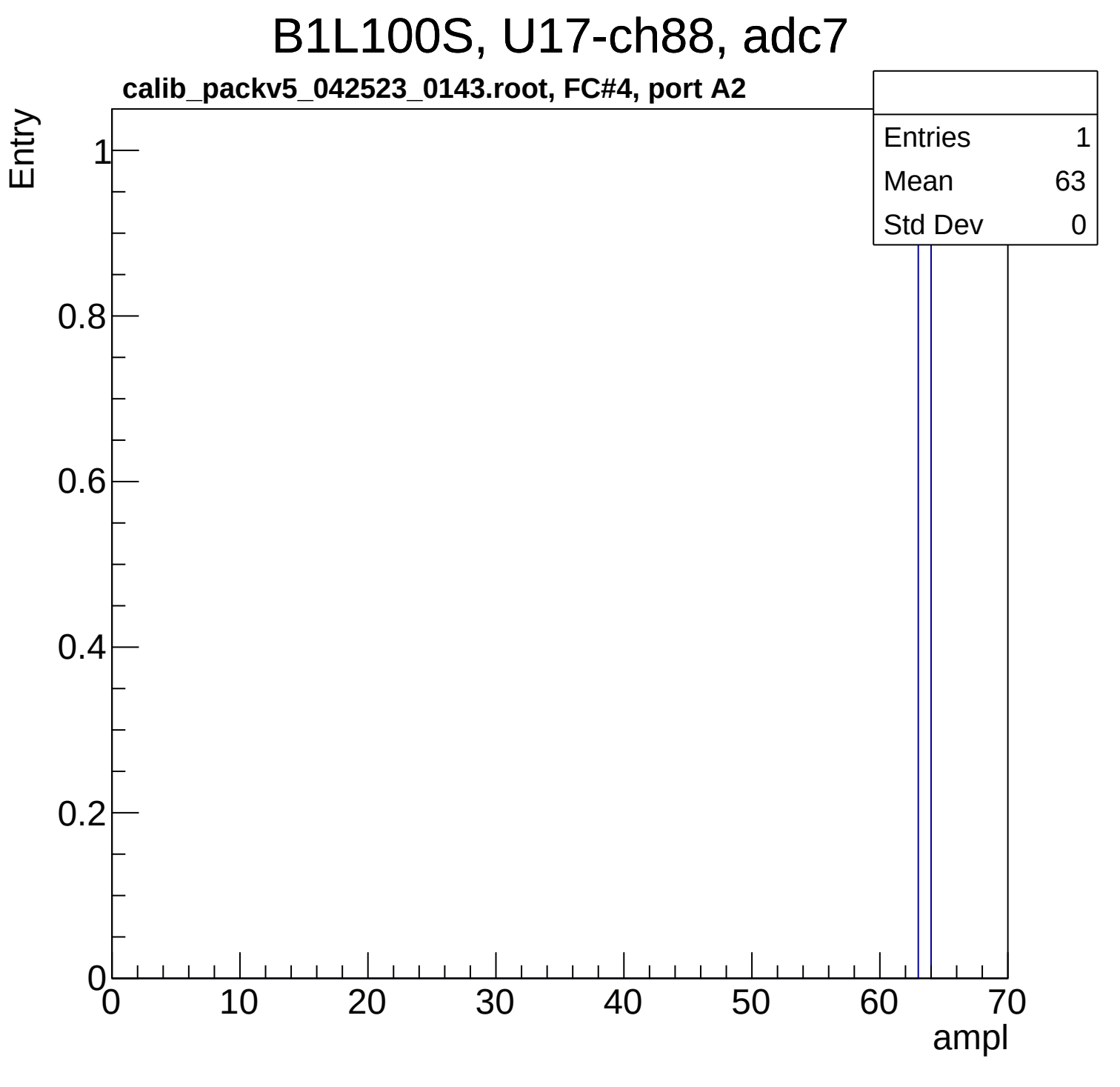
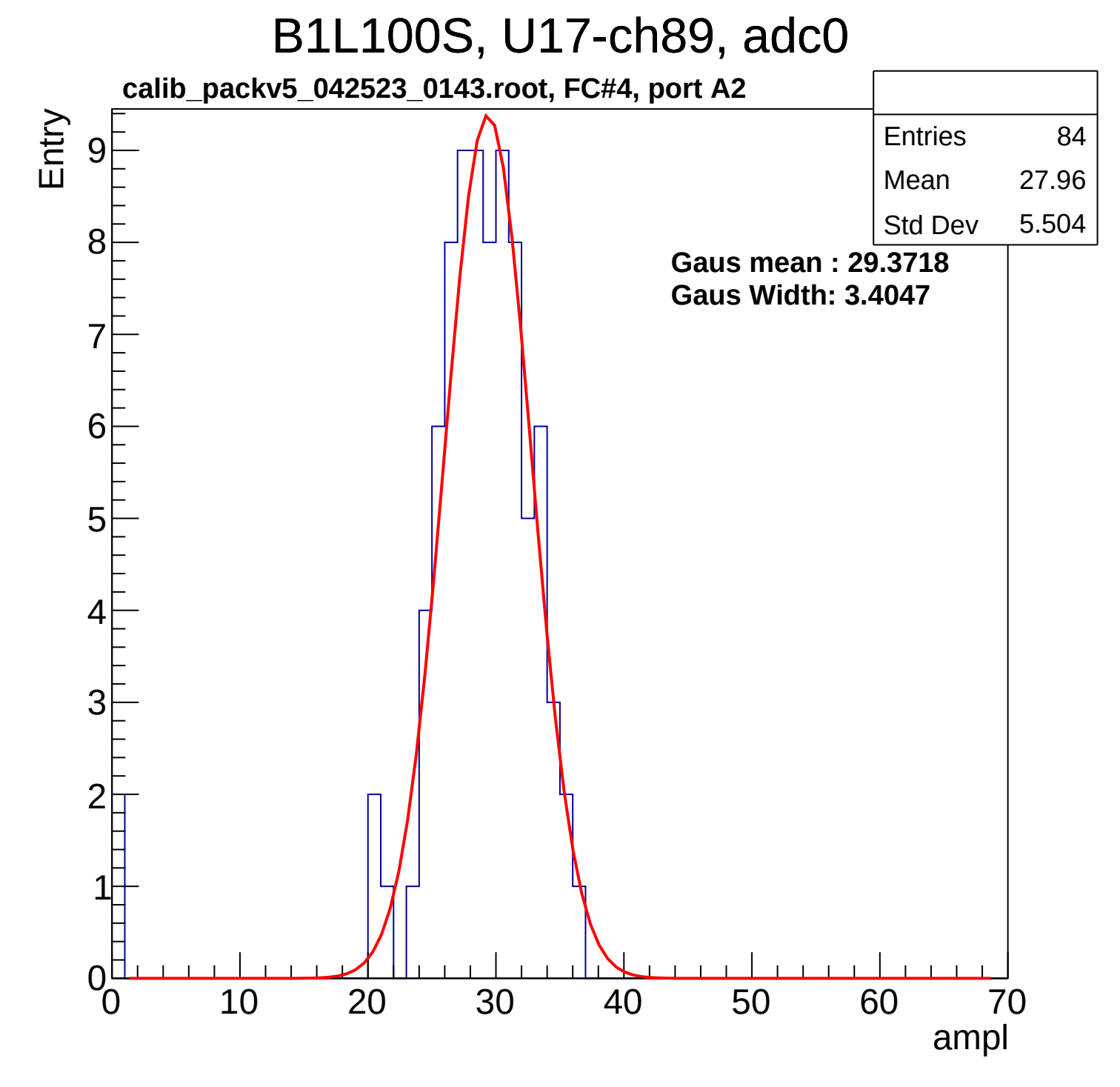
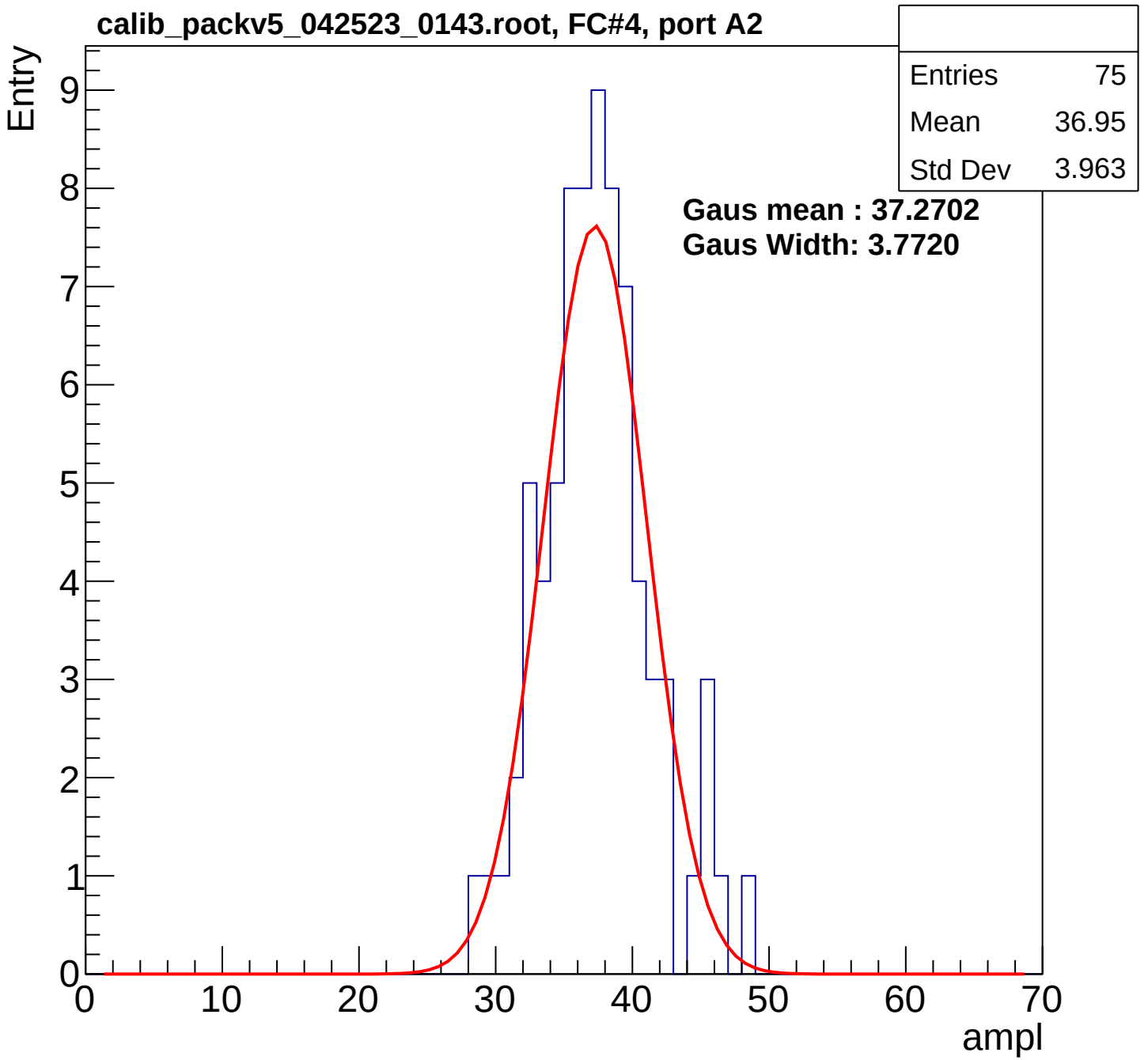

B1L100S, U17-ch88, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 57.74
Std Dev 8.692
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch88, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 20
Mean 60.75
Std Dev 1.699
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch88, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch89, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 84
Mean 27.96
Std Dev 5.504
Gaus mean : 29.3718
Gaus Width: 3.4047
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch89, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 75
Mean 36.95
Std Dev 3.963
Gaus mean : 37.2702
Gaus Width: 3.7720
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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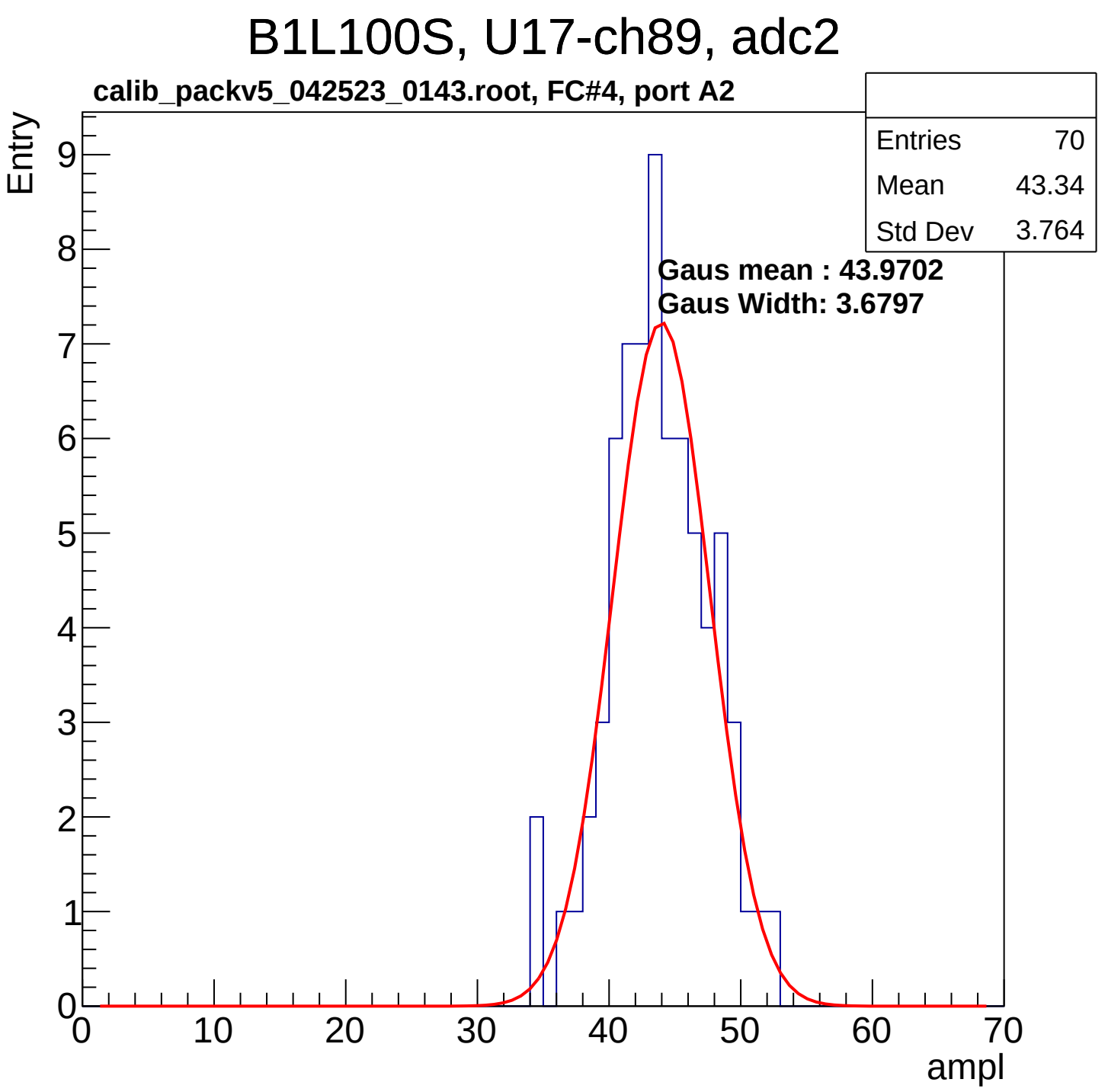
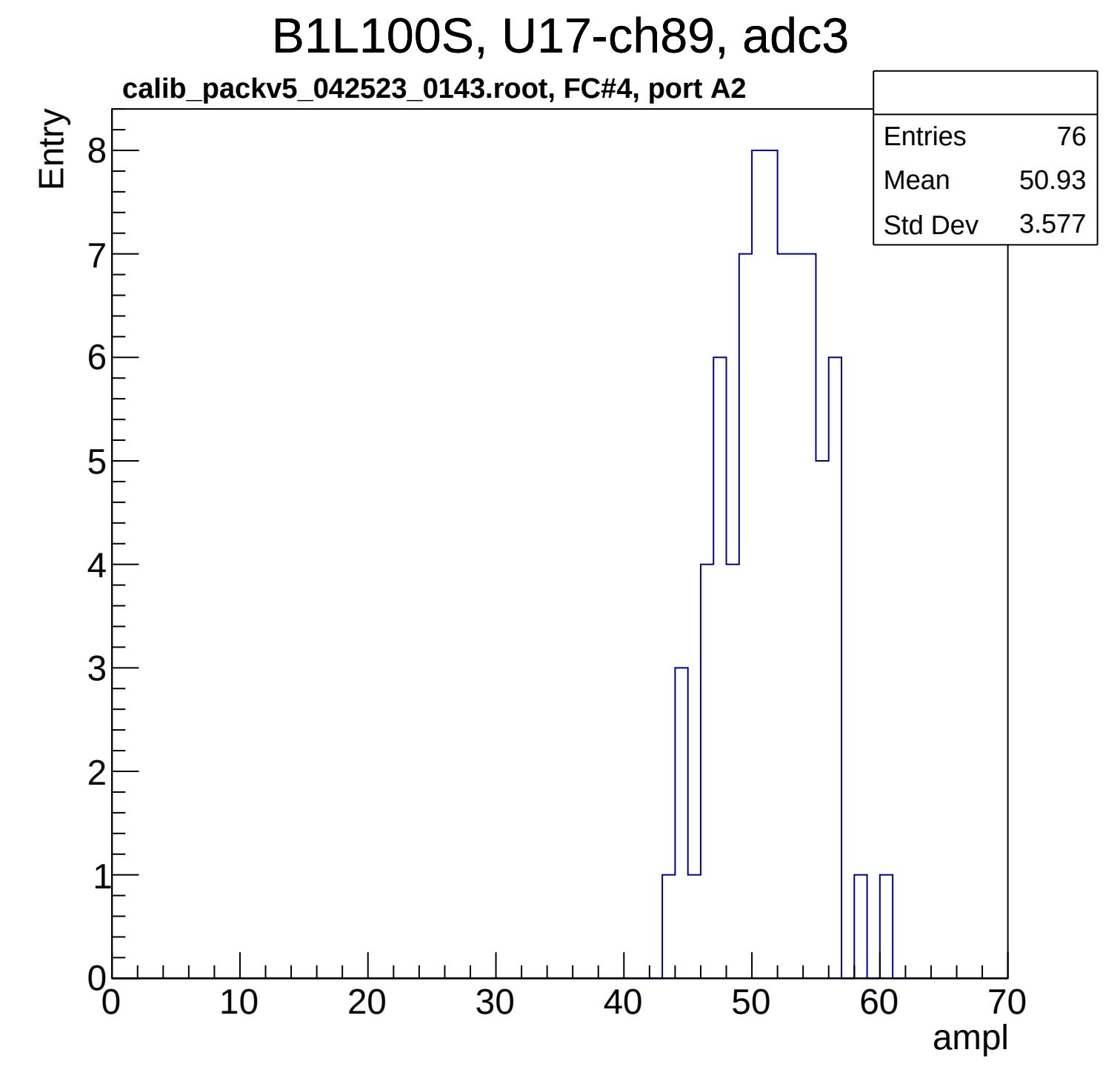
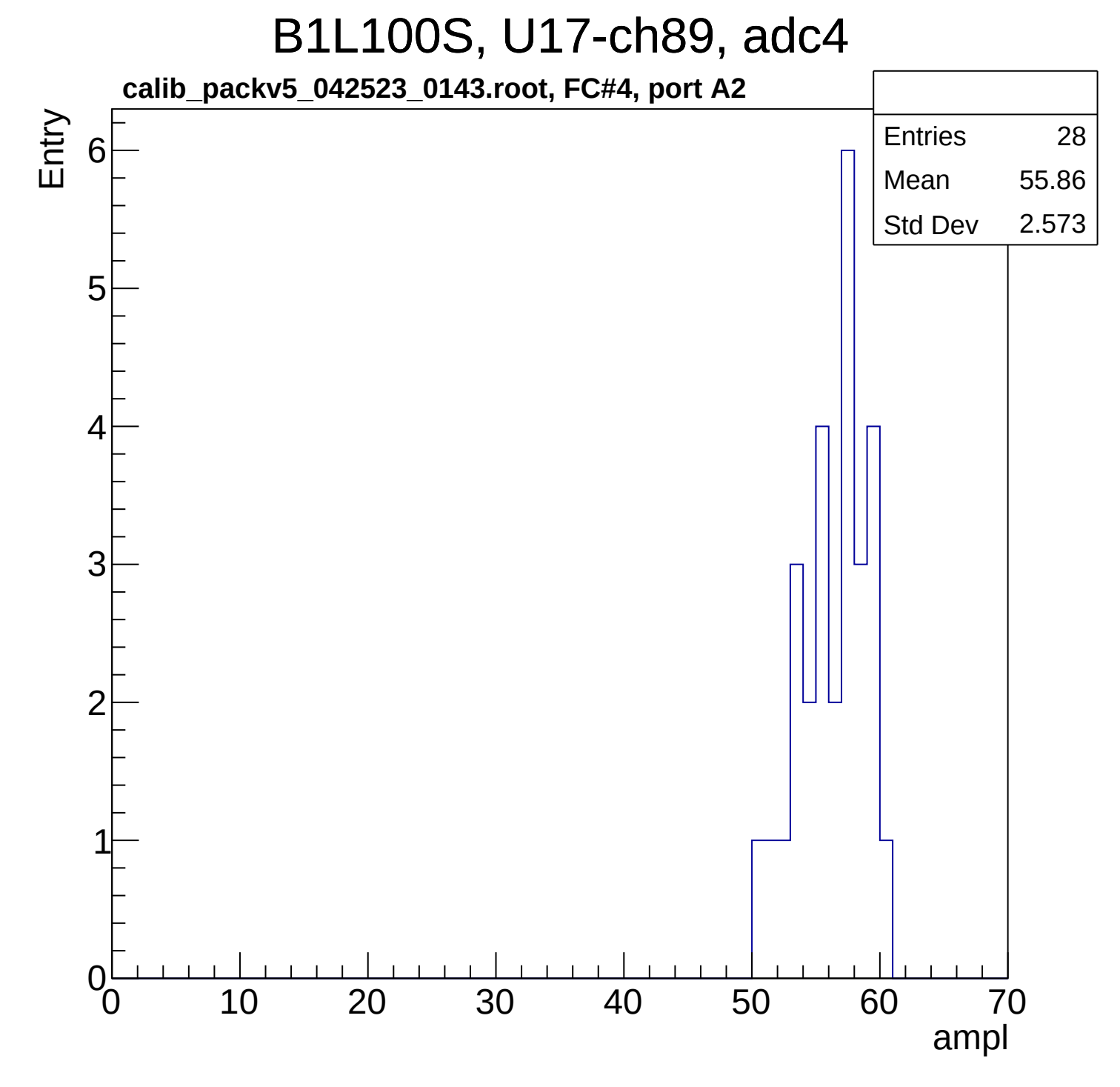
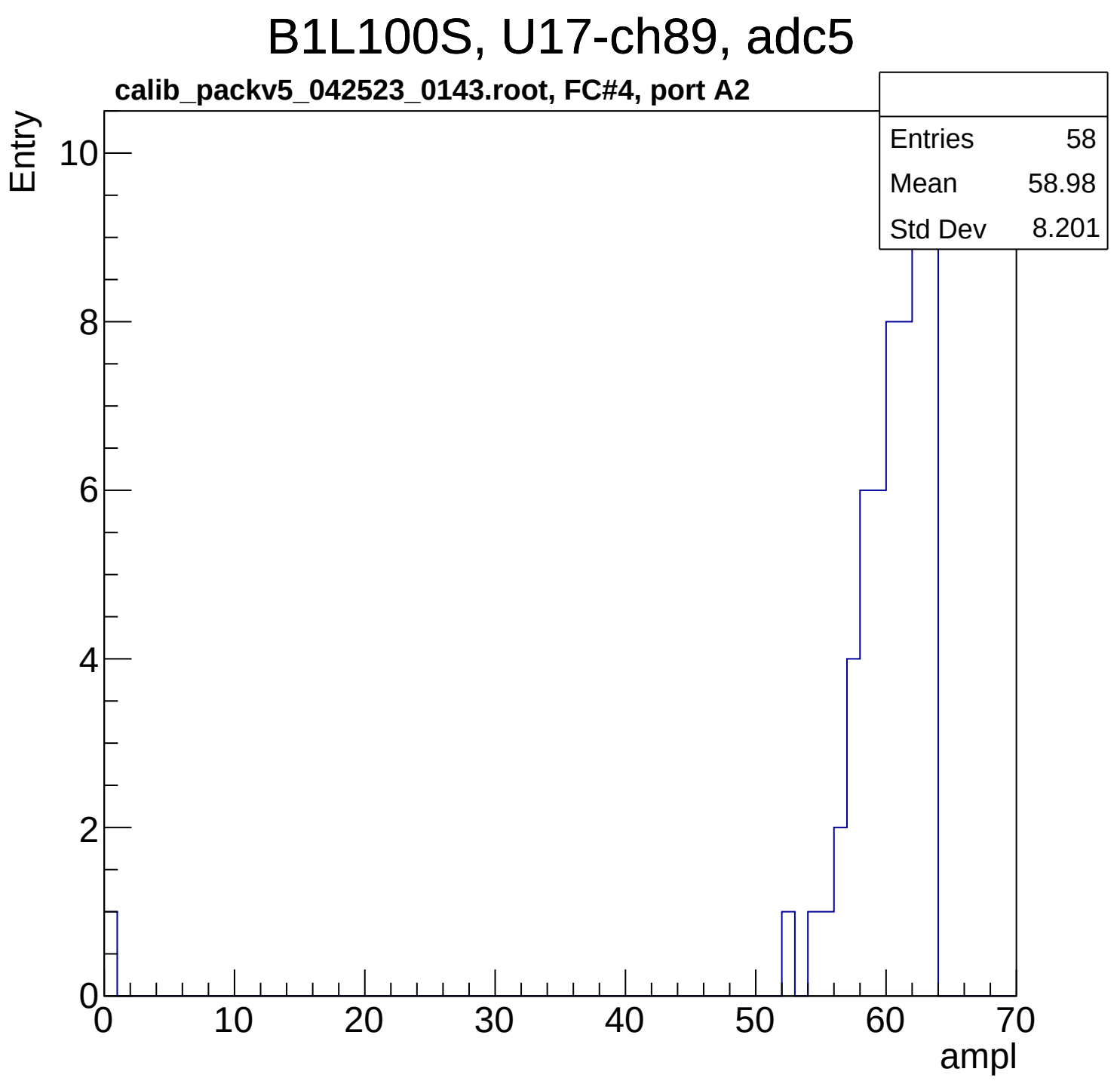
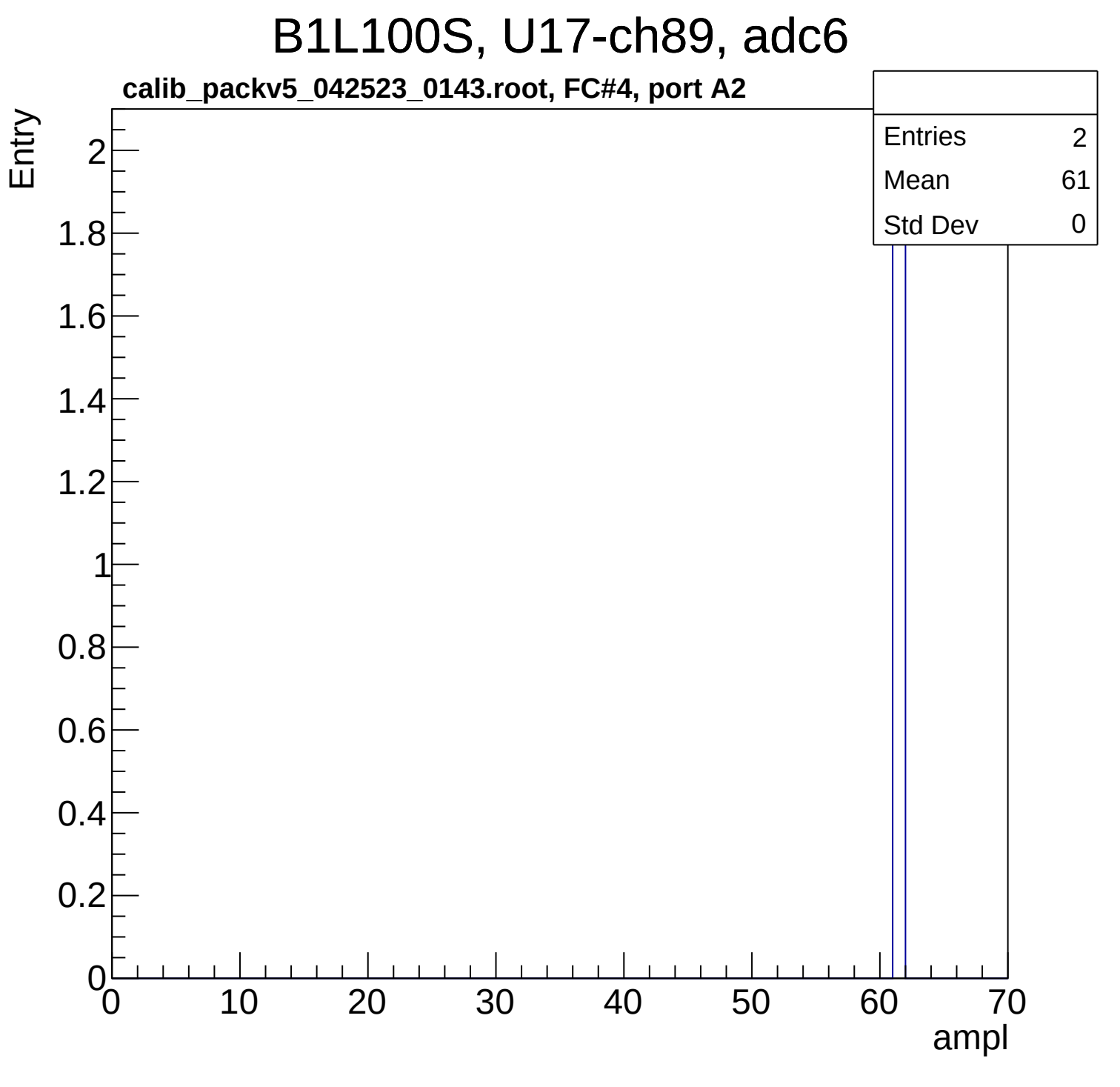
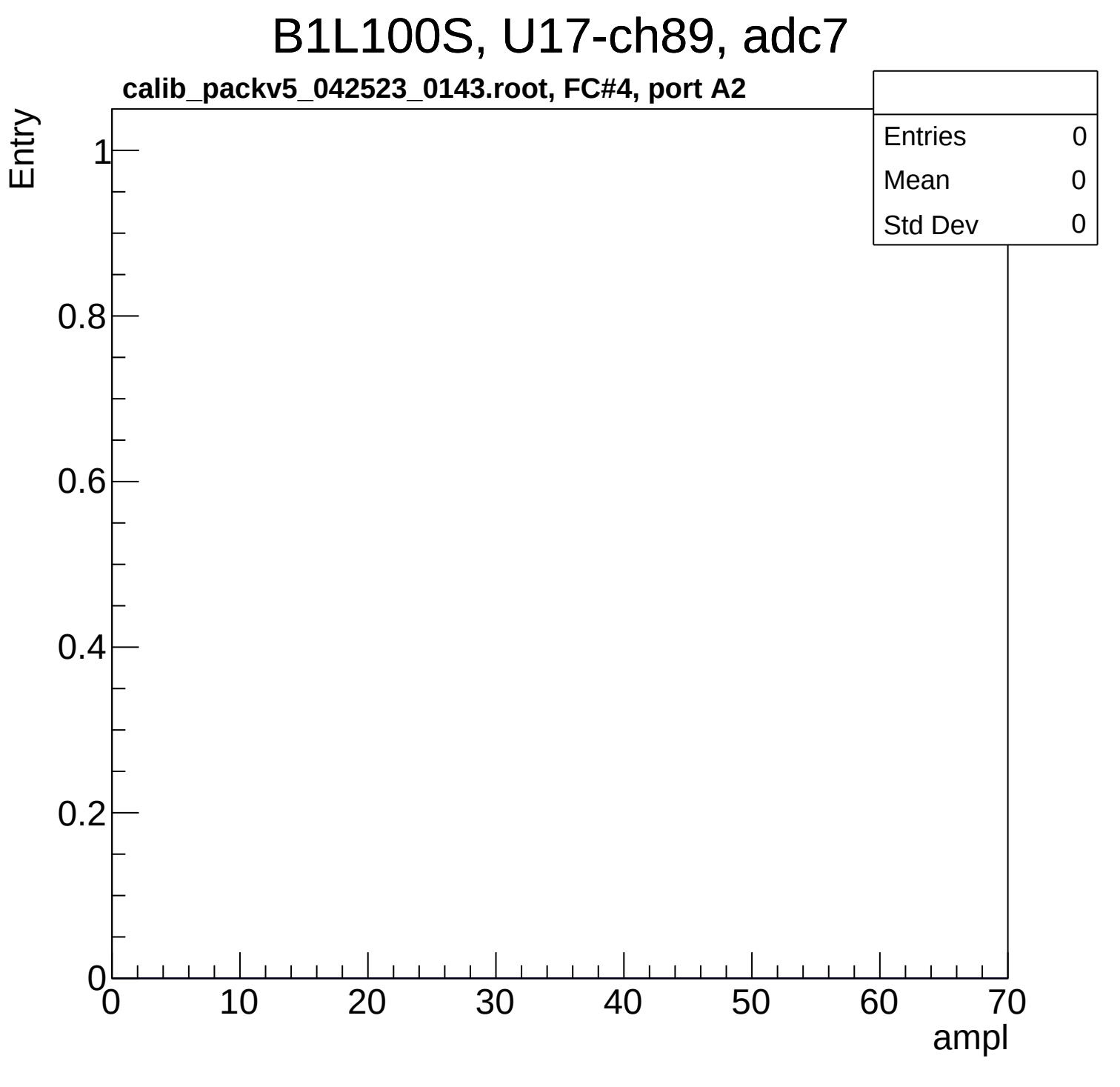

B1L100S, U17-ch89, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 43.34
Std Dev 3.764
Gaus mean : 43.9702
Gaus Width: 3.6797
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

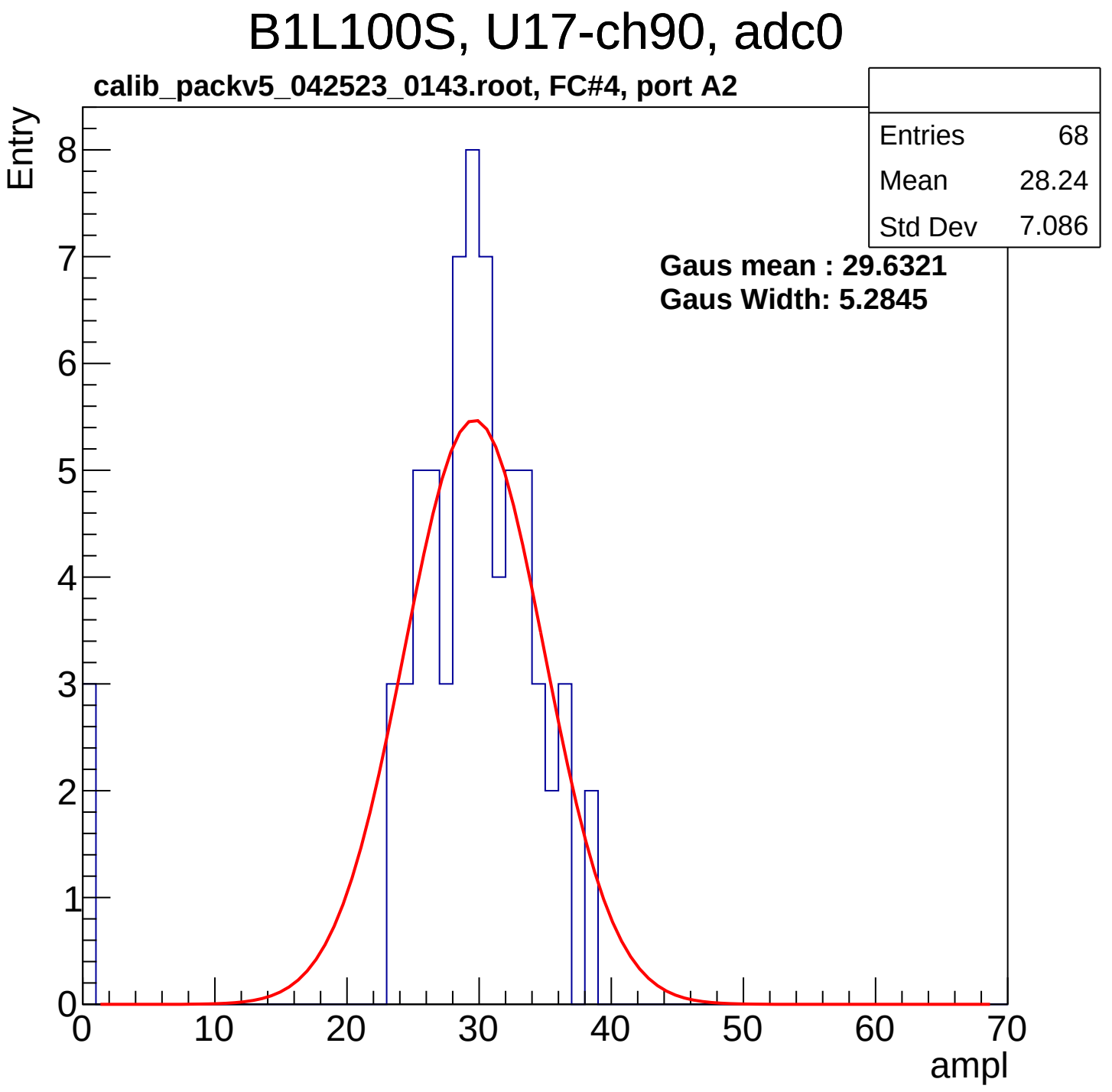

B1L100S, U17-ch89, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 76
Mean 50.93
Std Dev 3.577
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

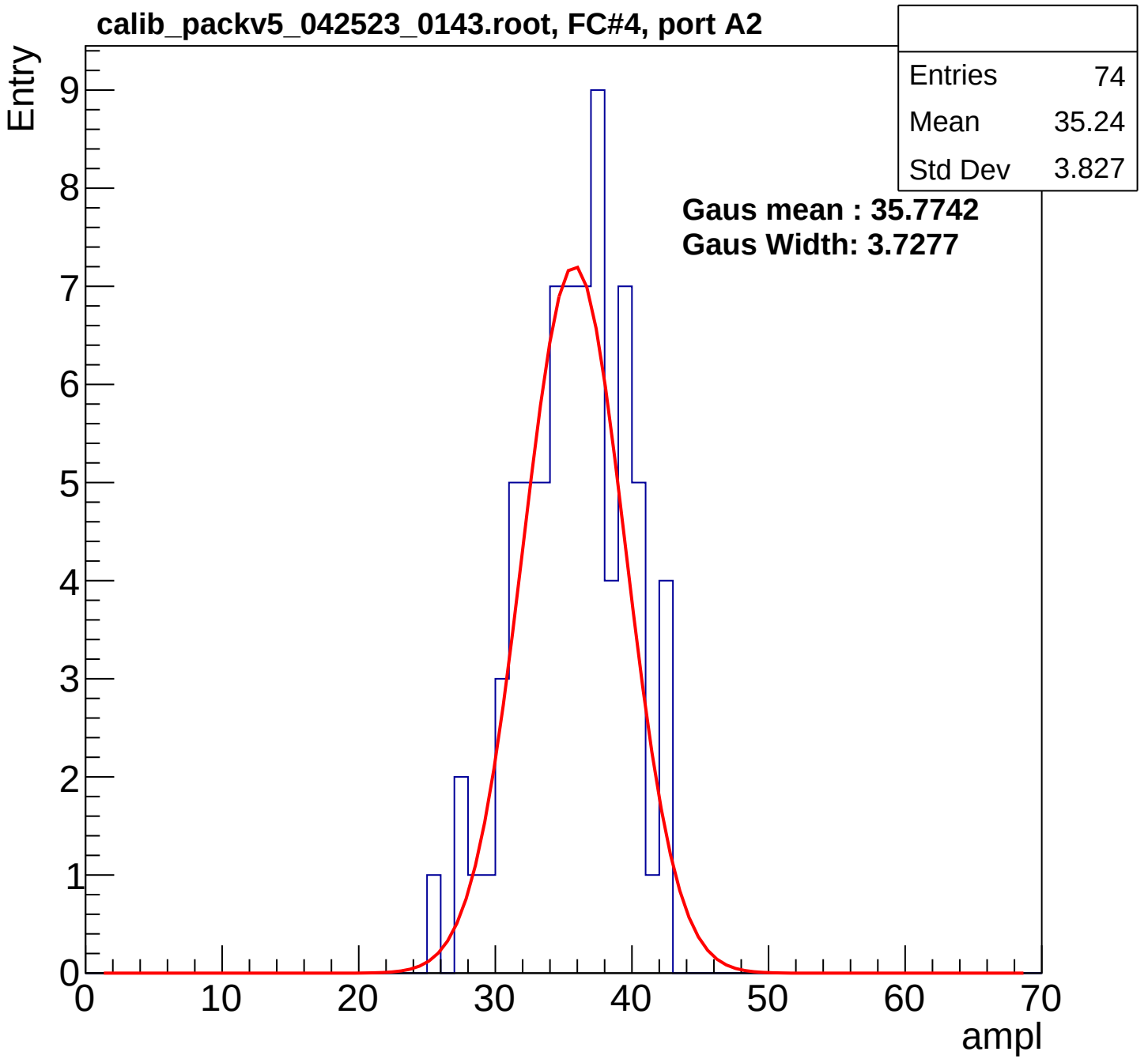

B1L100S, U17-ch89, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 28
Mean 55.86
Std Dev 2.573
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

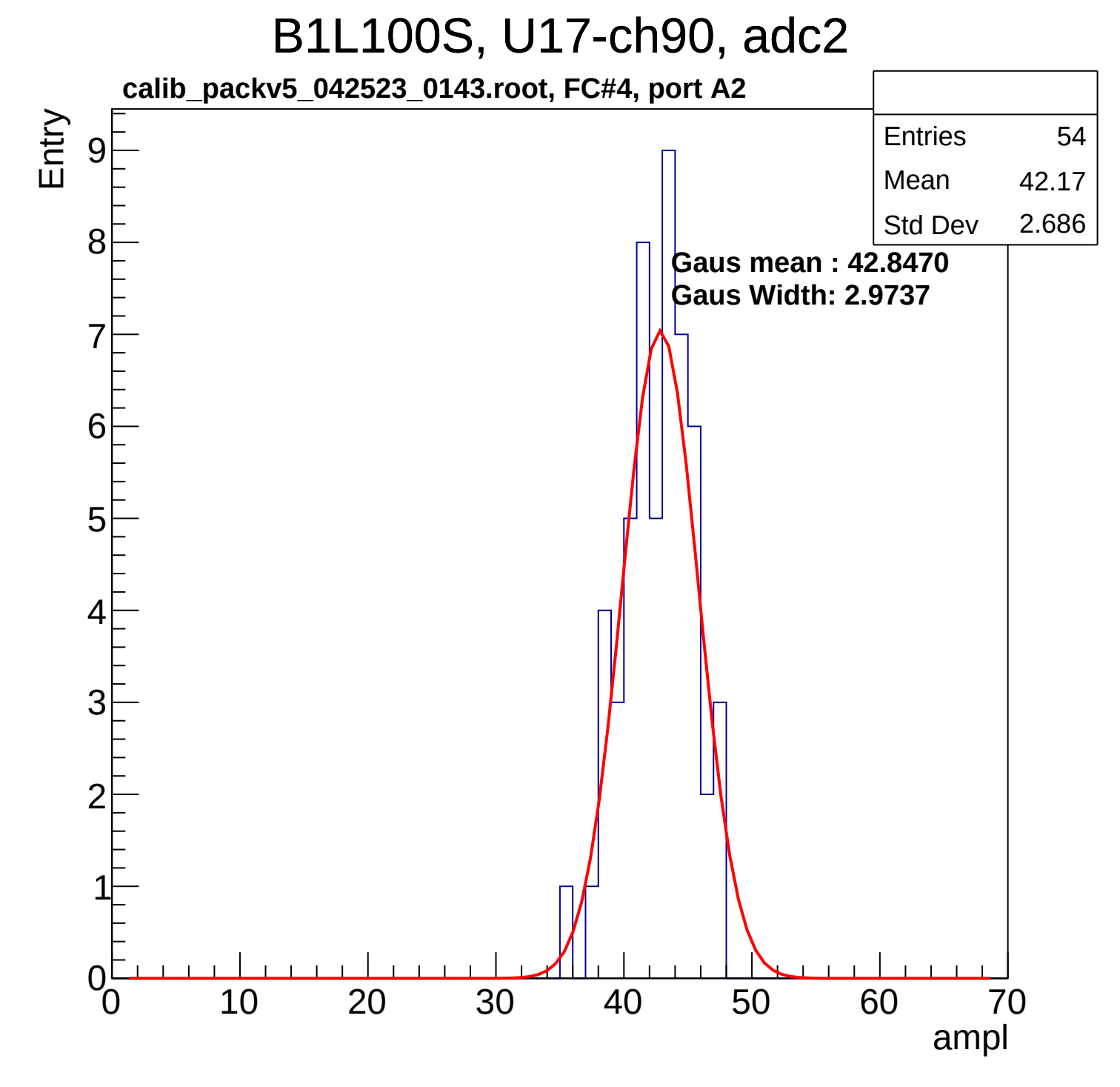

B1L100S, U17-ch89, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 58.98
Std Dev 8.201
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch89, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 61
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L100S, U17-ch89, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch90, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 28.24
Std Dev 7.086
Gaus mean : 29.6321
Gaus Width: 5.2845
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch90, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 74
Mean 35.24
Std Dev 3.827
Gaus mean : 35.7742
Gaus Width: 3.7277
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L100S, U17-ch90, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 42.17
Std Dev 2.686
Gaus mean : 42.8470
Gaus Width: 2.9737
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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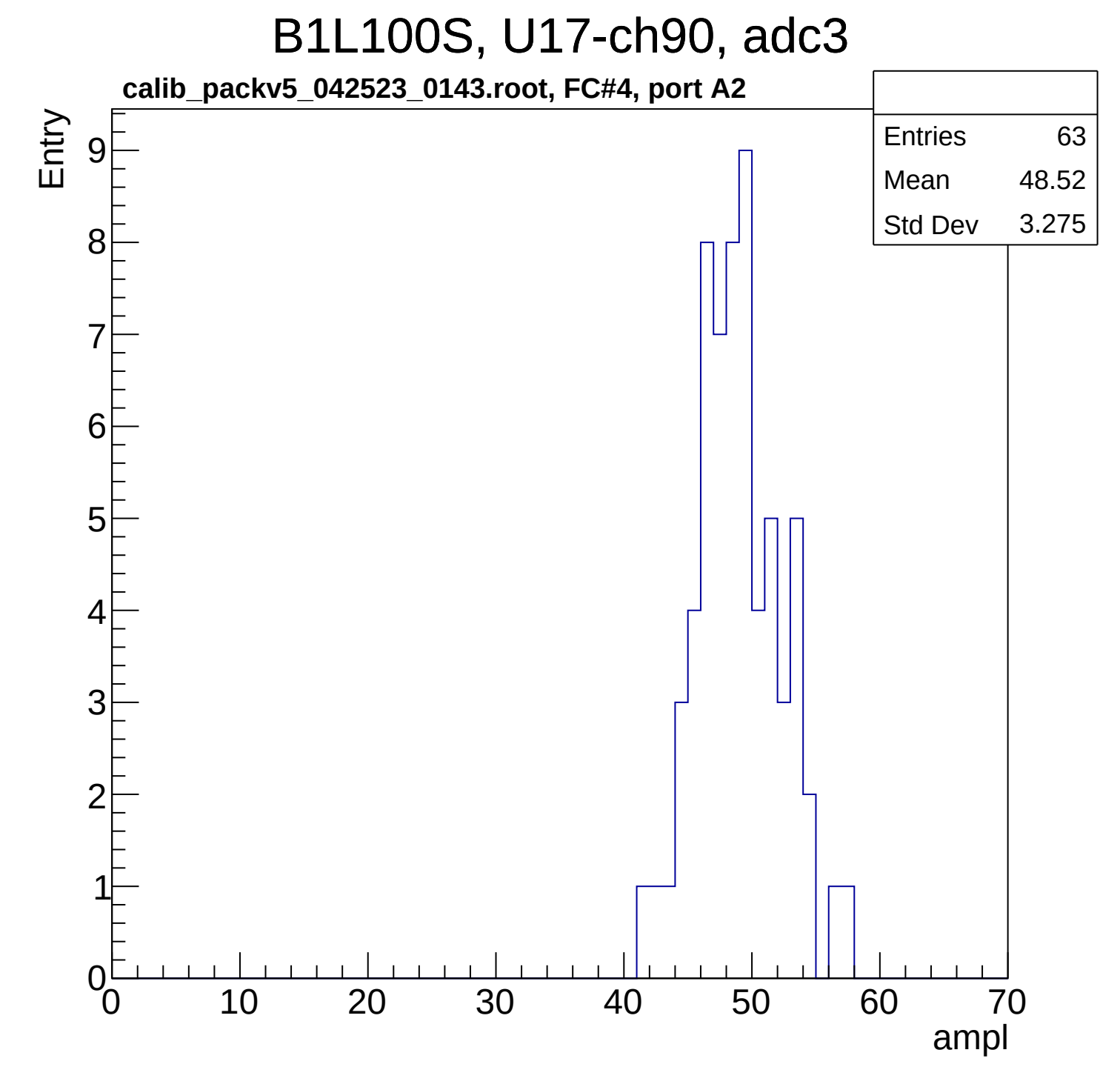
B1L100S, U17-ch90, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 48.52
Std Dev 3.275
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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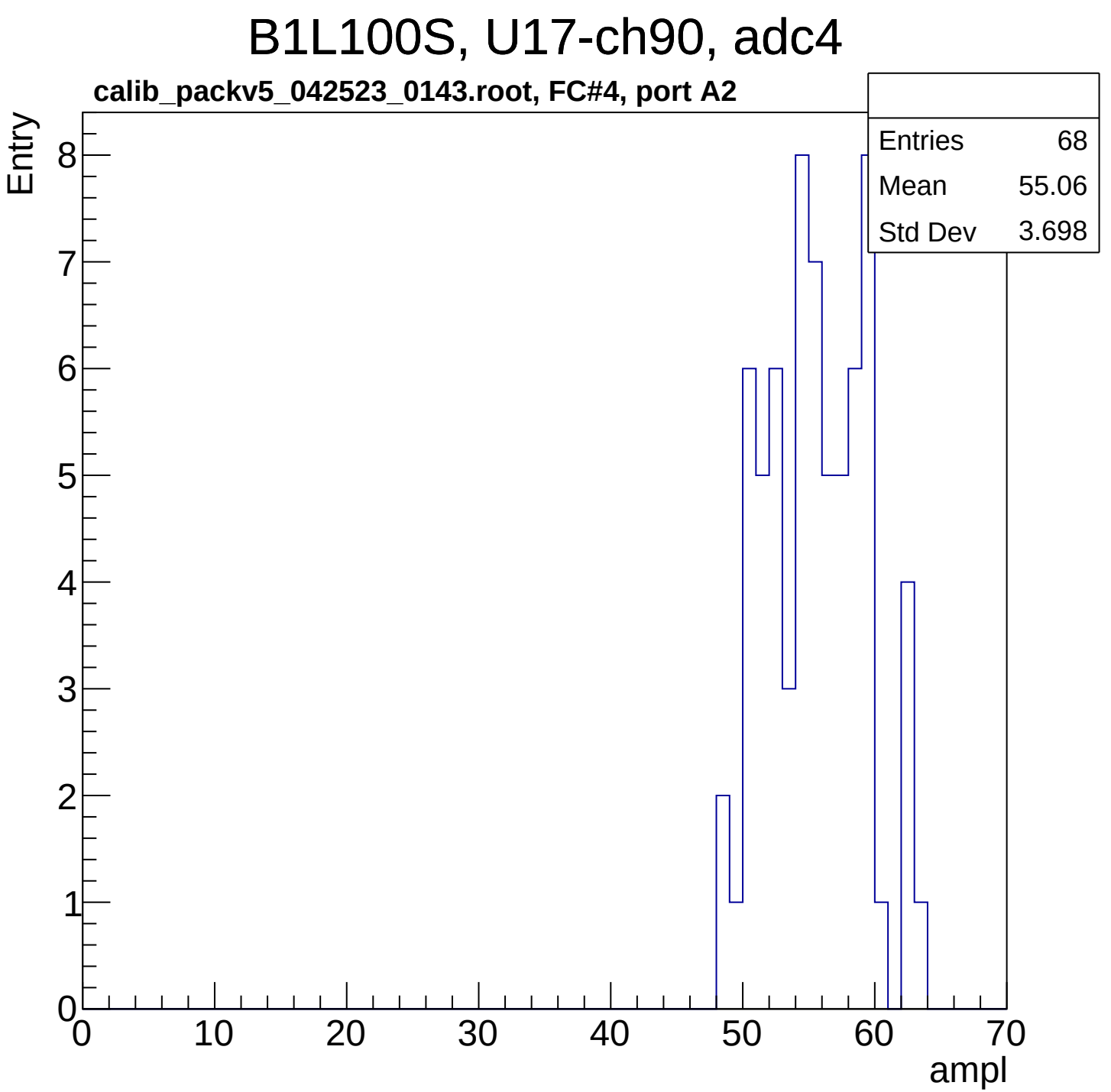
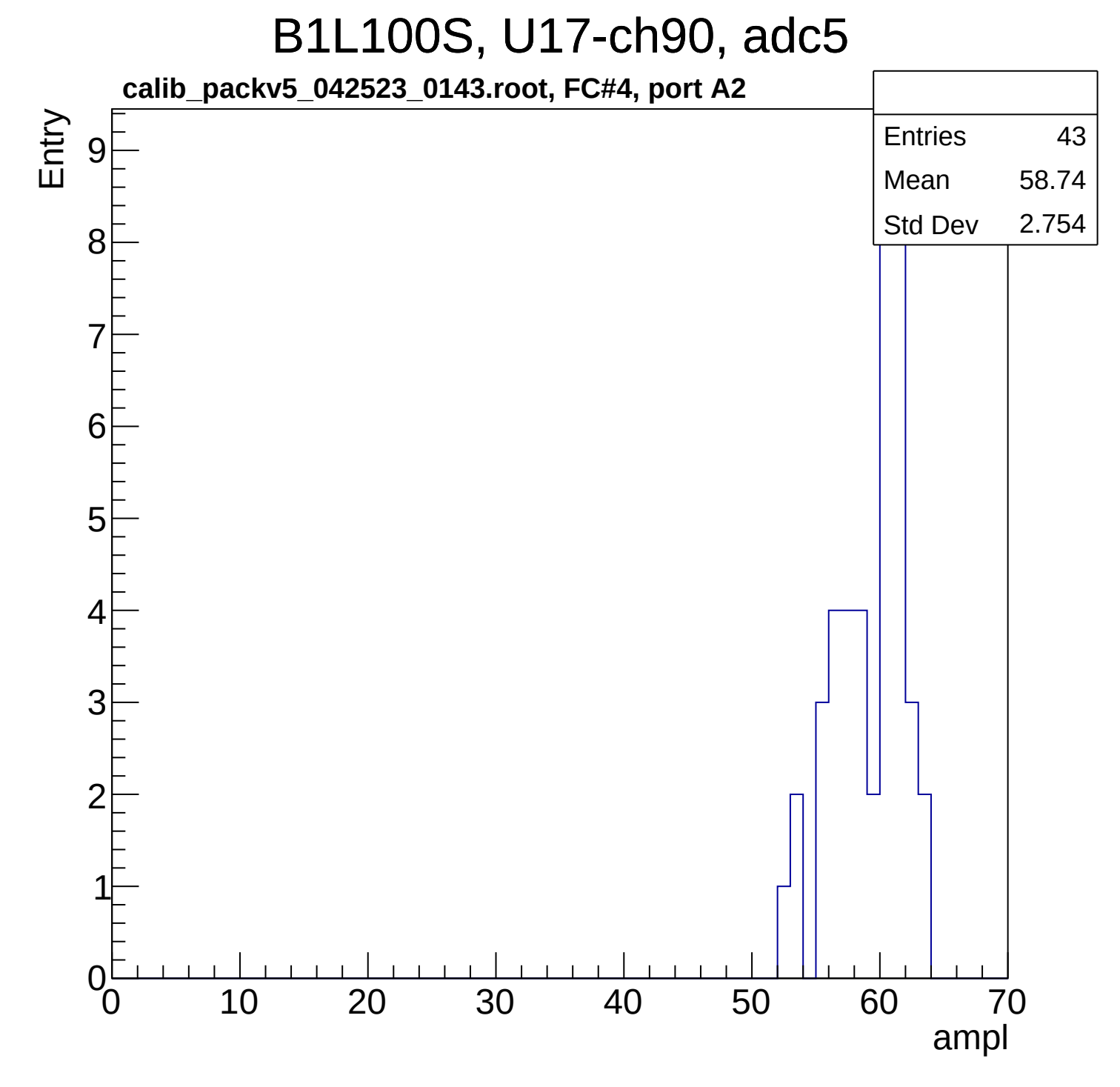
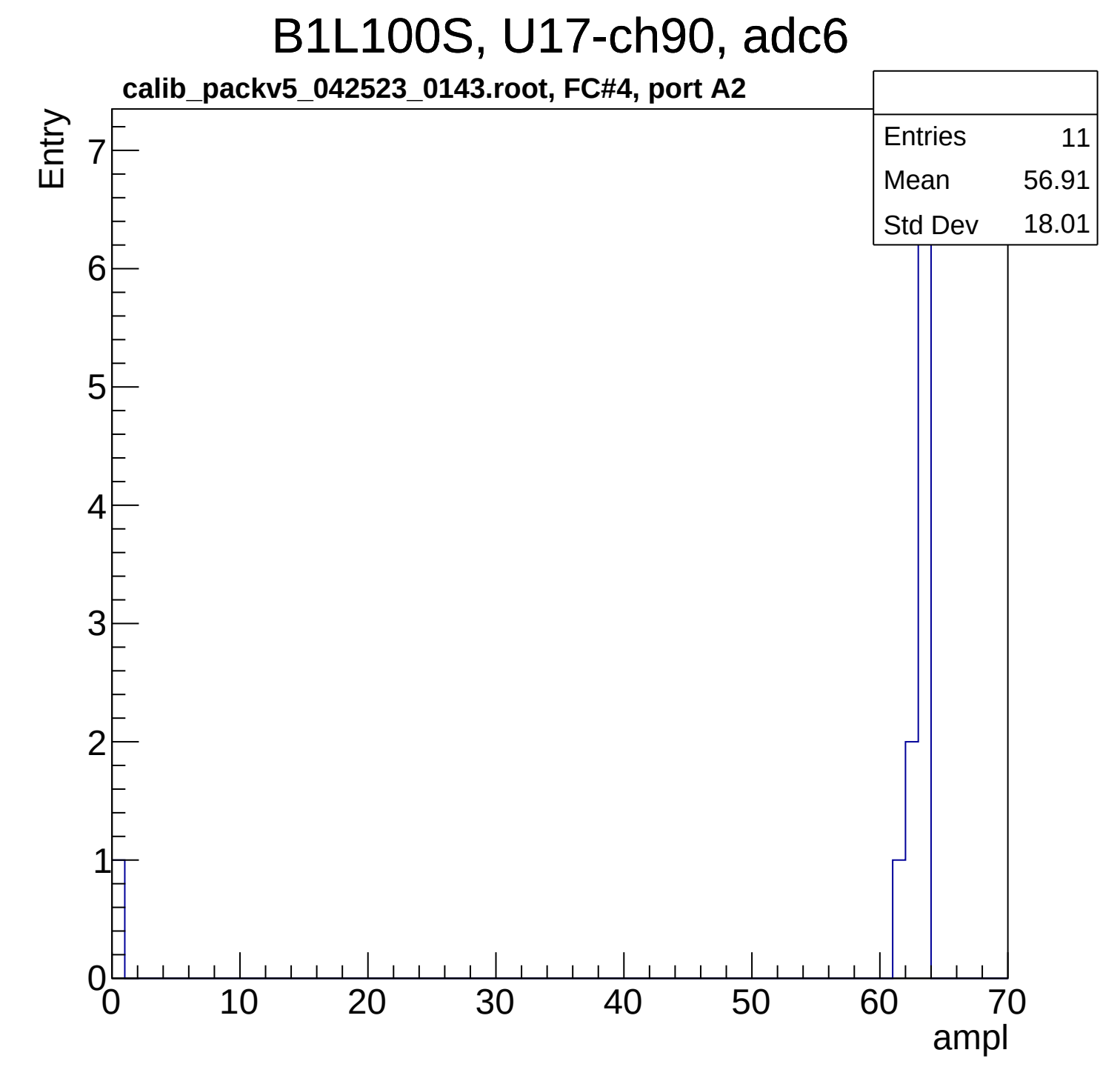
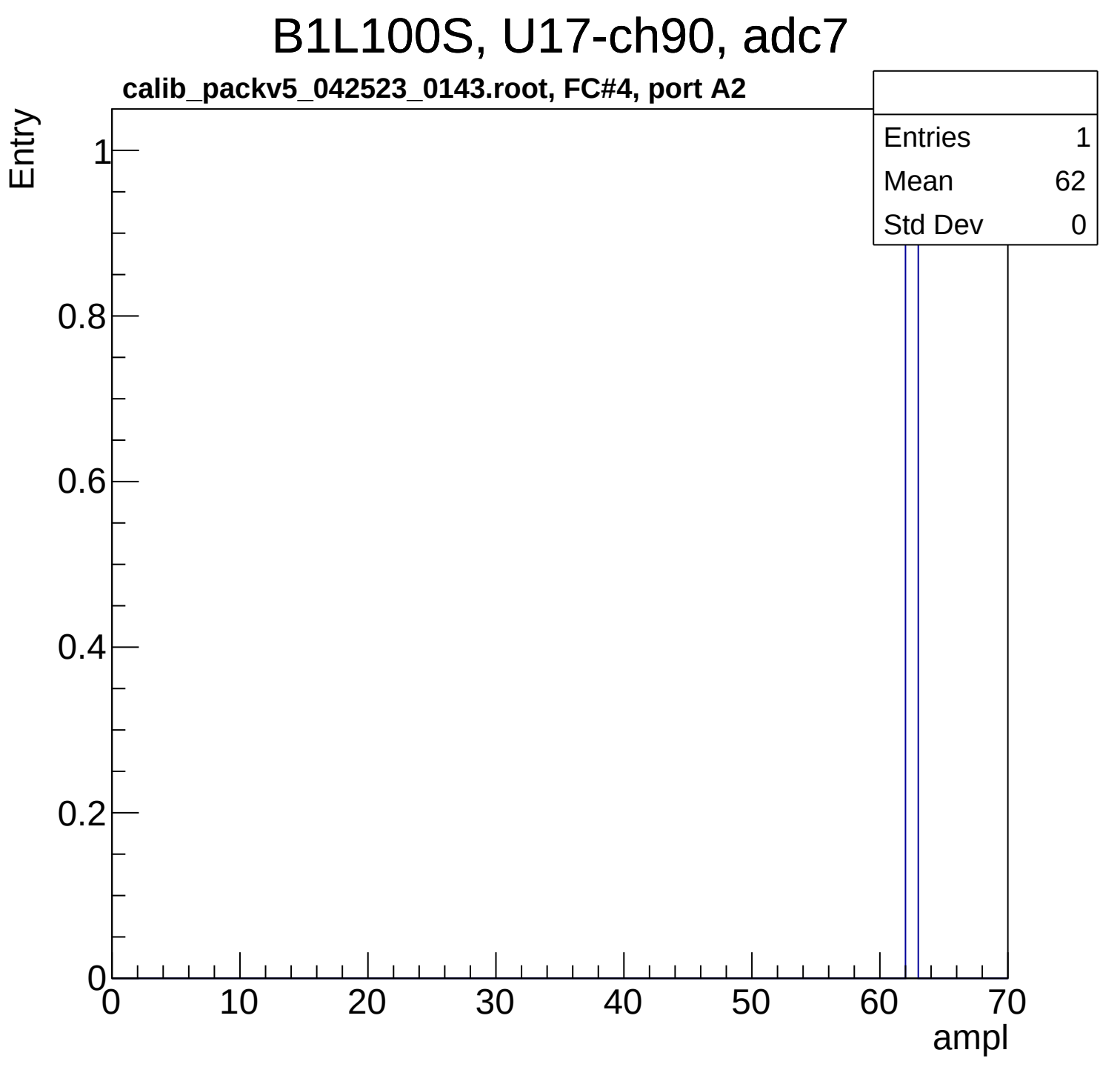
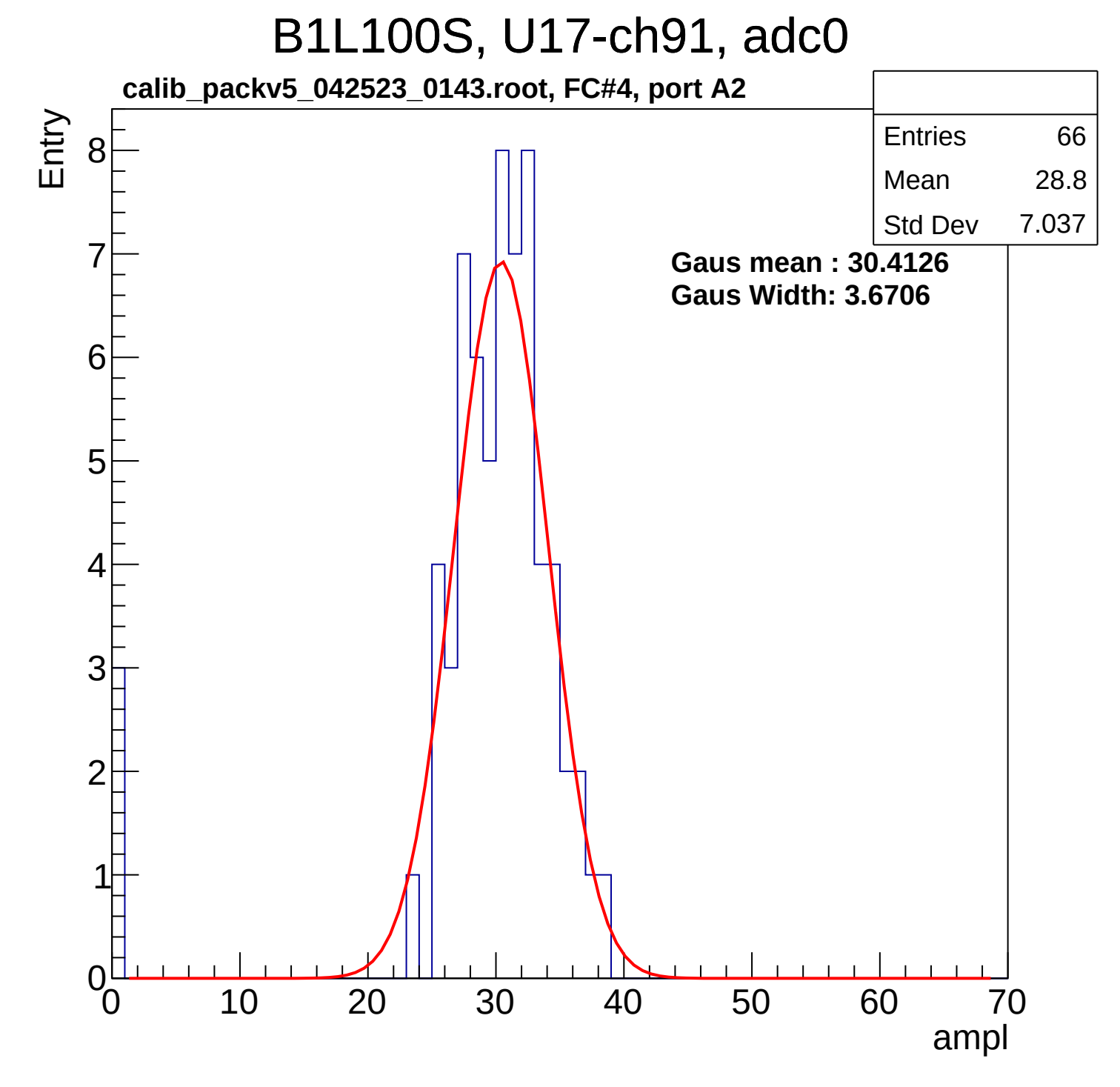

B1L100S, U17-ch90, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 55.06
Std Dev 3.698
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch90, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 43
Mean 58.74
Std Dev 2.754
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch90, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 11
Mean 56.91
Std Dev 18.01
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U17-ch90, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 62
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch91, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 28.8
Std Dev 7.037
Gaus mean : 30.4126
Gaus Width: 3.6706
Entry
ampl
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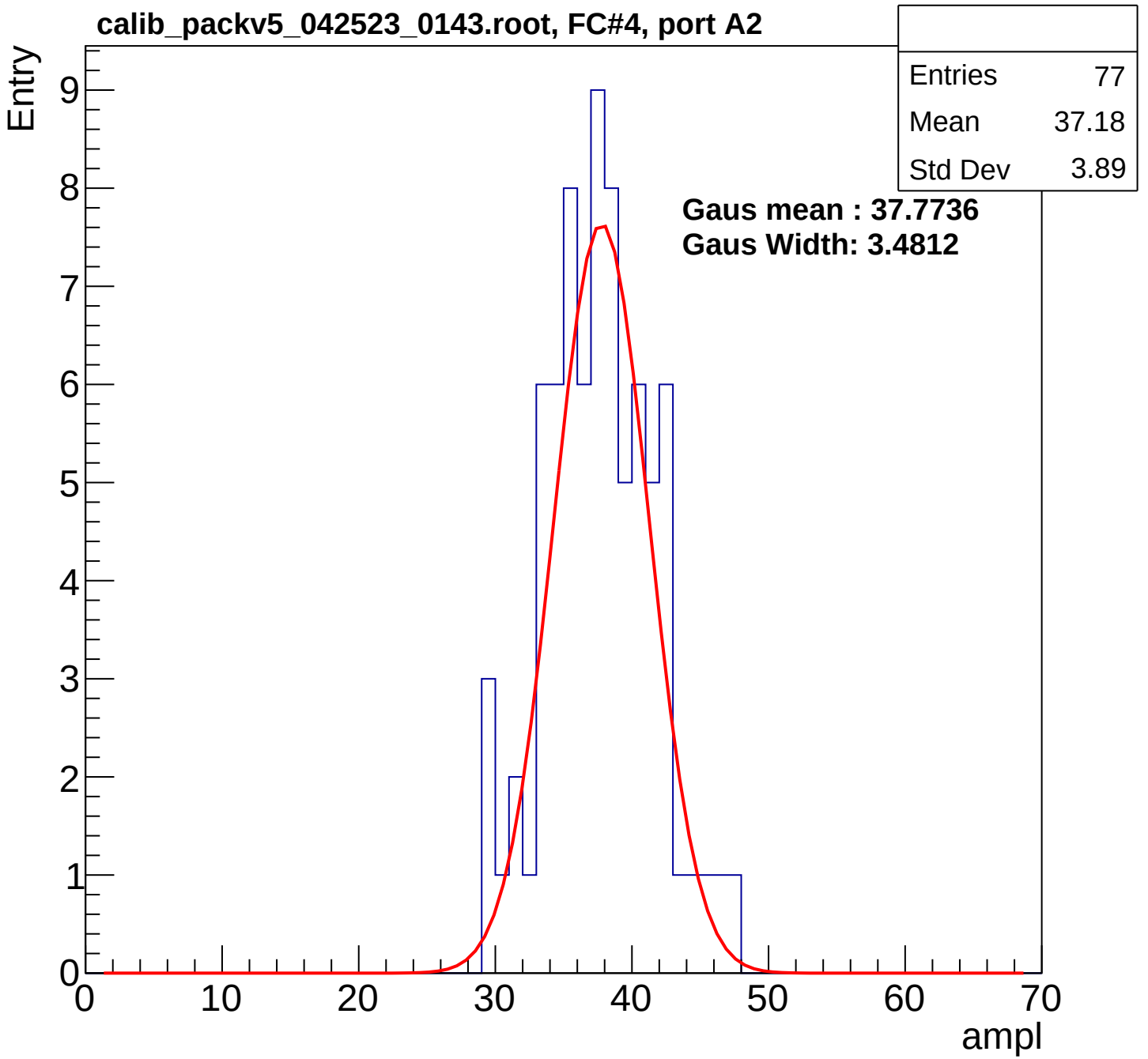
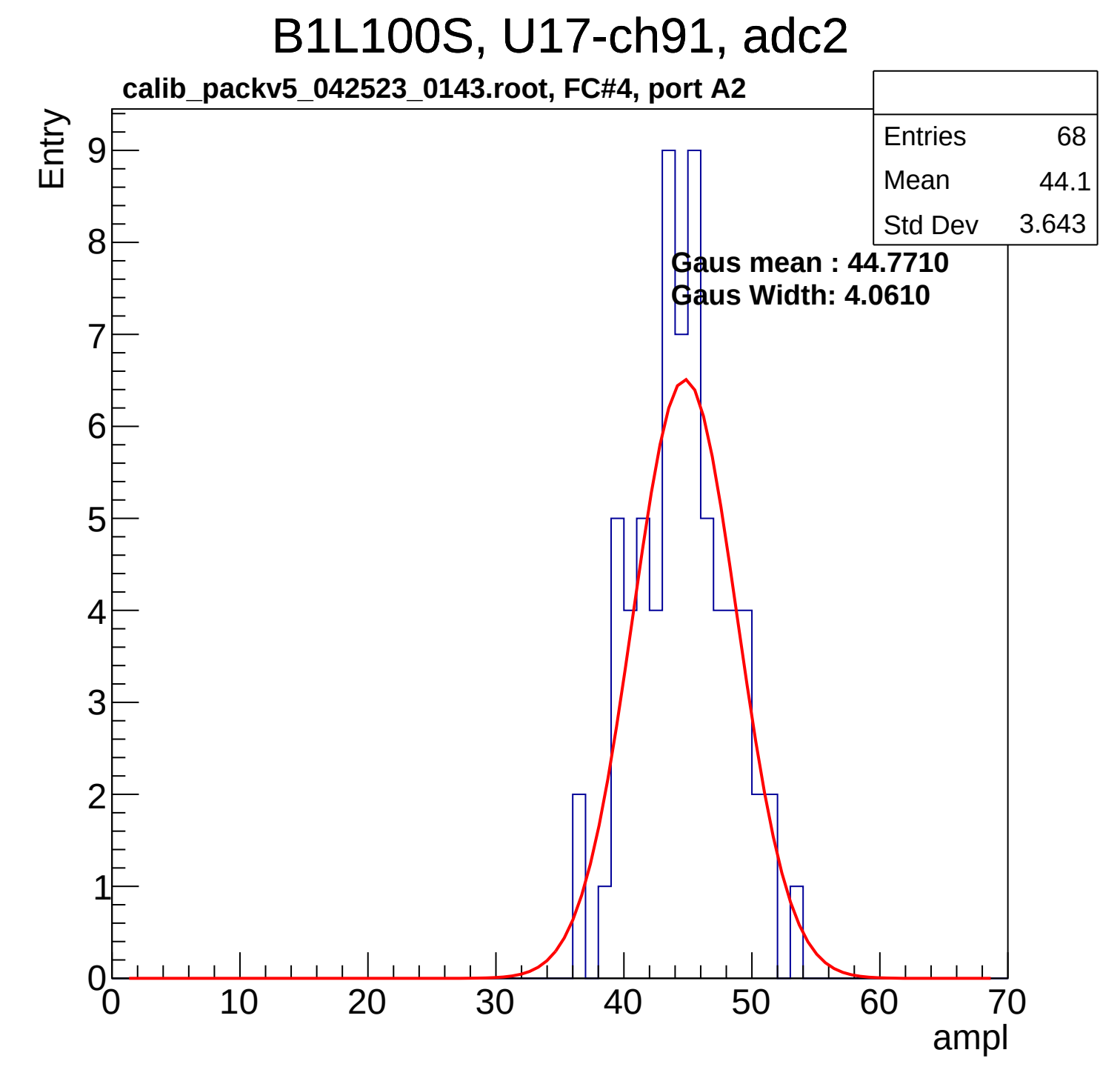
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch91, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 77
Mean 37.18
Std Dev 3.89
Gaus mean : 37.7736
Gaus Width: 3.4812
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch91, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 44.1
Std Dev 3.643
Gaus mean : 44.7710
Gaus Width: 4.0610
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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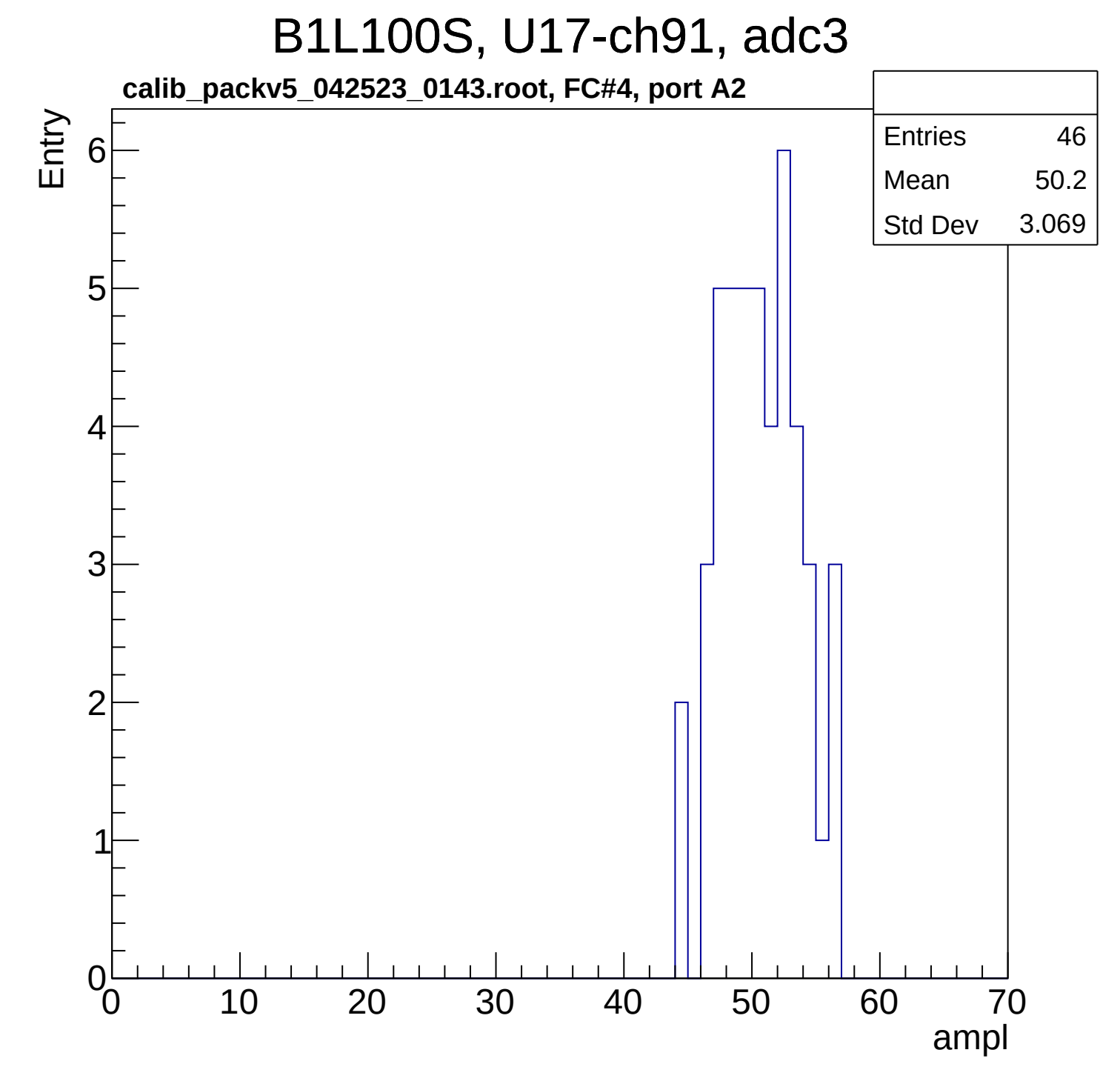
B1L100S, U17-ch91, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 46
Mean 50.2
Std Dev 3.069
Entry
ampl
0
1
2
3
4
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0
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20
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40
50
60
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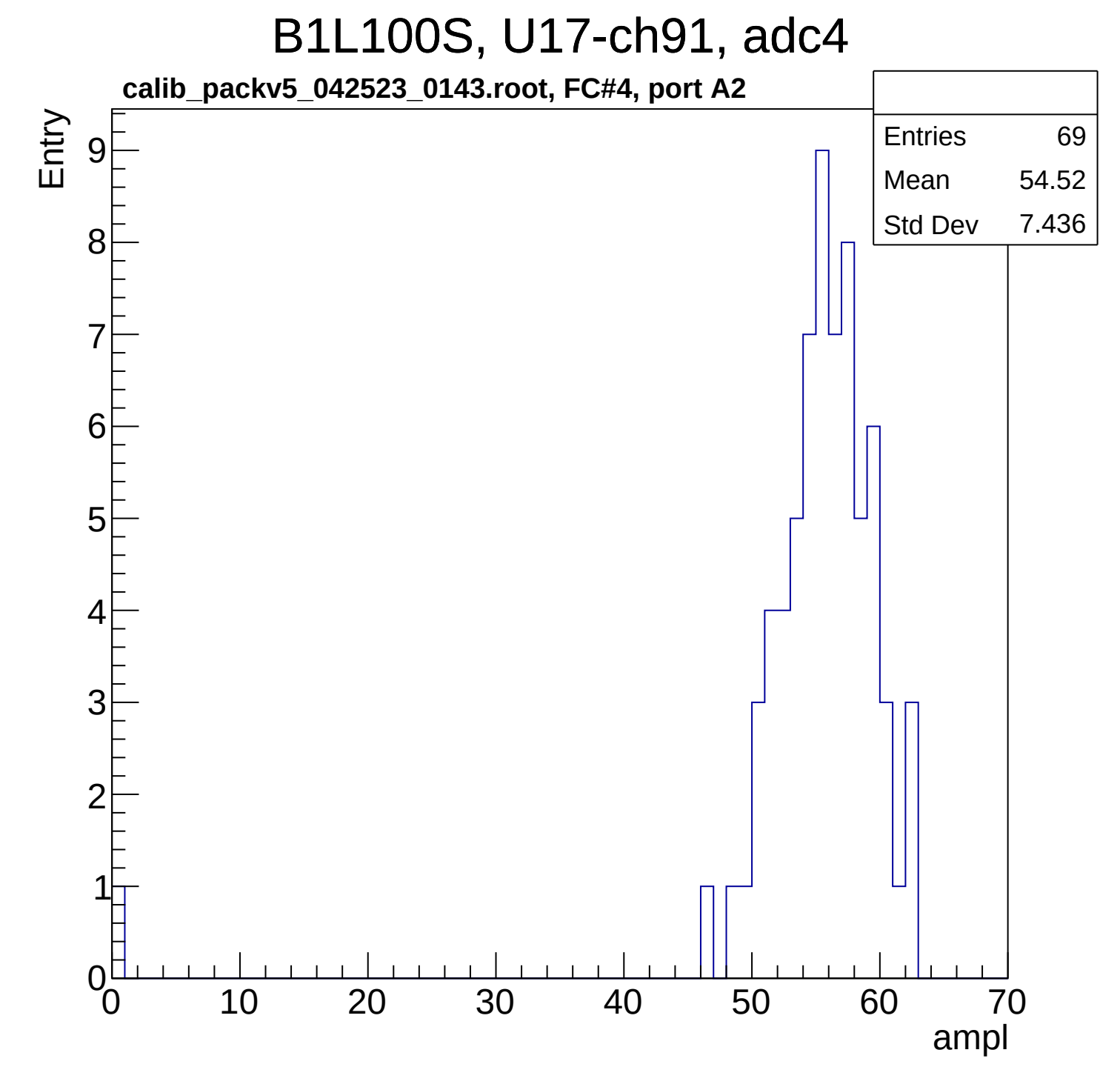
B1L100S, U17-ch91, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 54.52
Std Dev 7.436
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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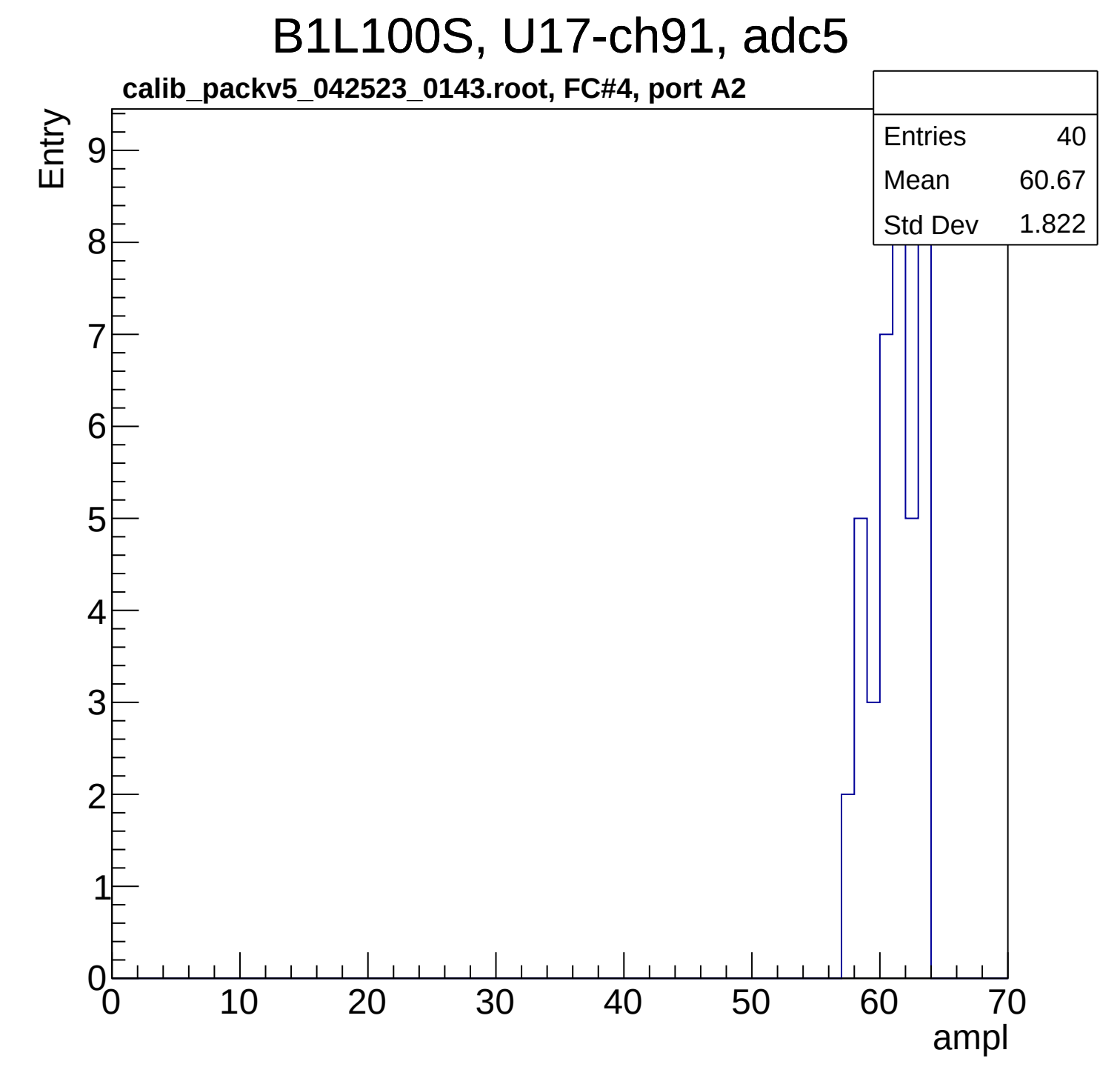
B1L100S, U17-ch91, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 40
Mean 60.67
Std Dev 1.822
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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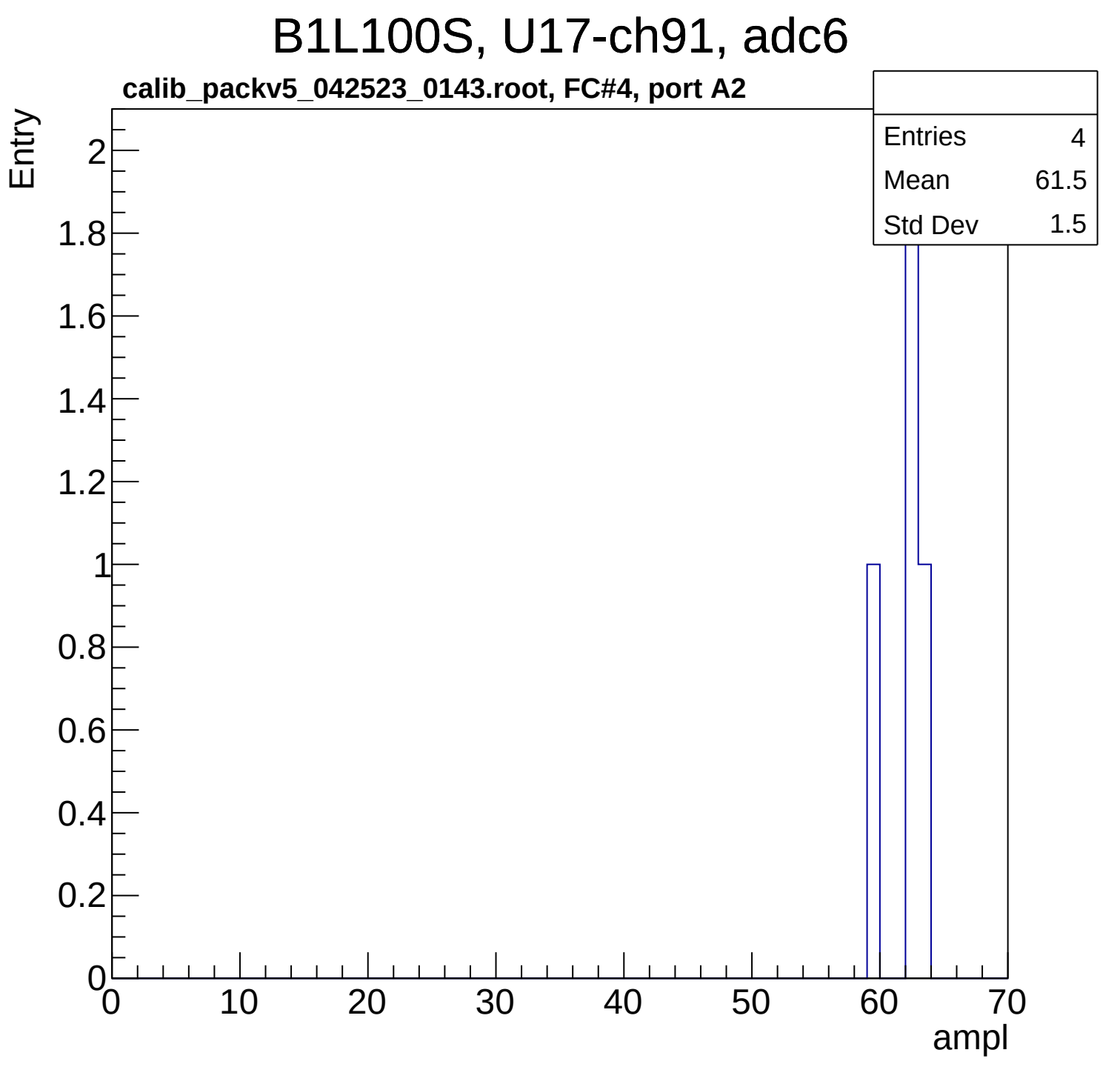
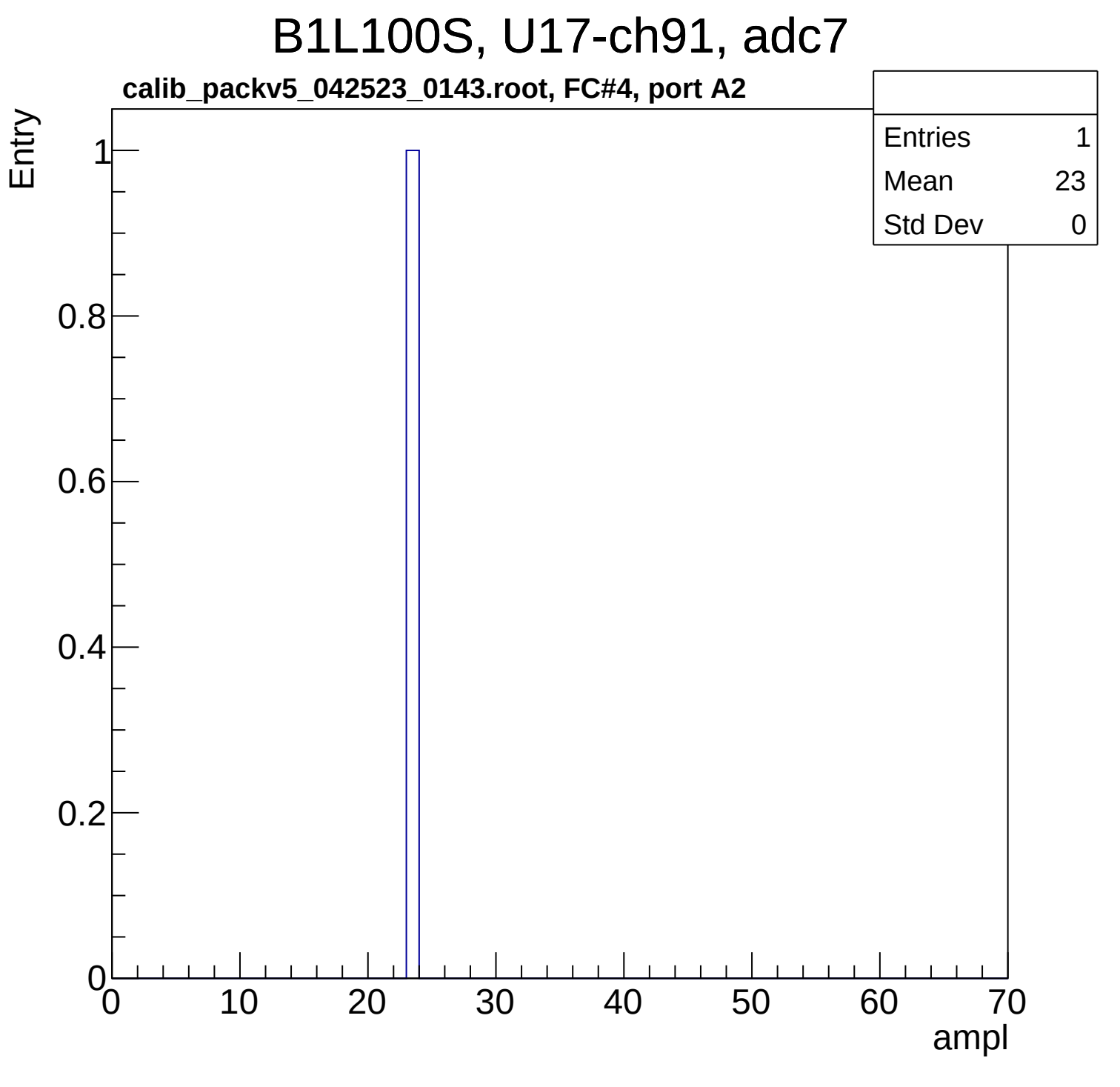

B1L100S, U17-ch91, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 4
Mean 61.5
Std Dev 1.5
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L100S, U17-ch91, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 23
Std Dev 0
Entry
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0.6
0.4
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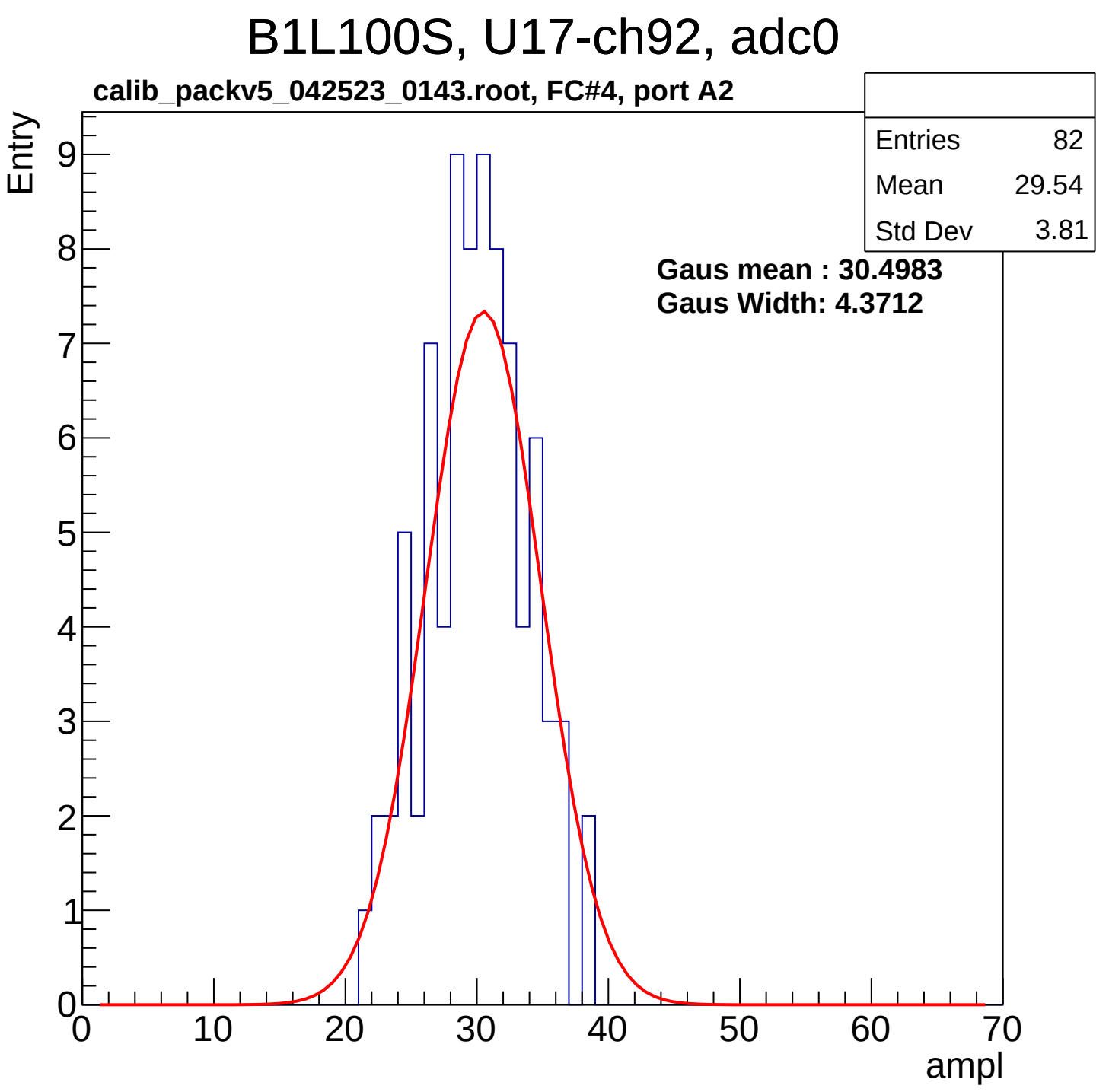
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch92, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 82
Mean 29.54
Std Dev 3.81
Gaus mean : 30.4983
Gaus Width: 4.3712
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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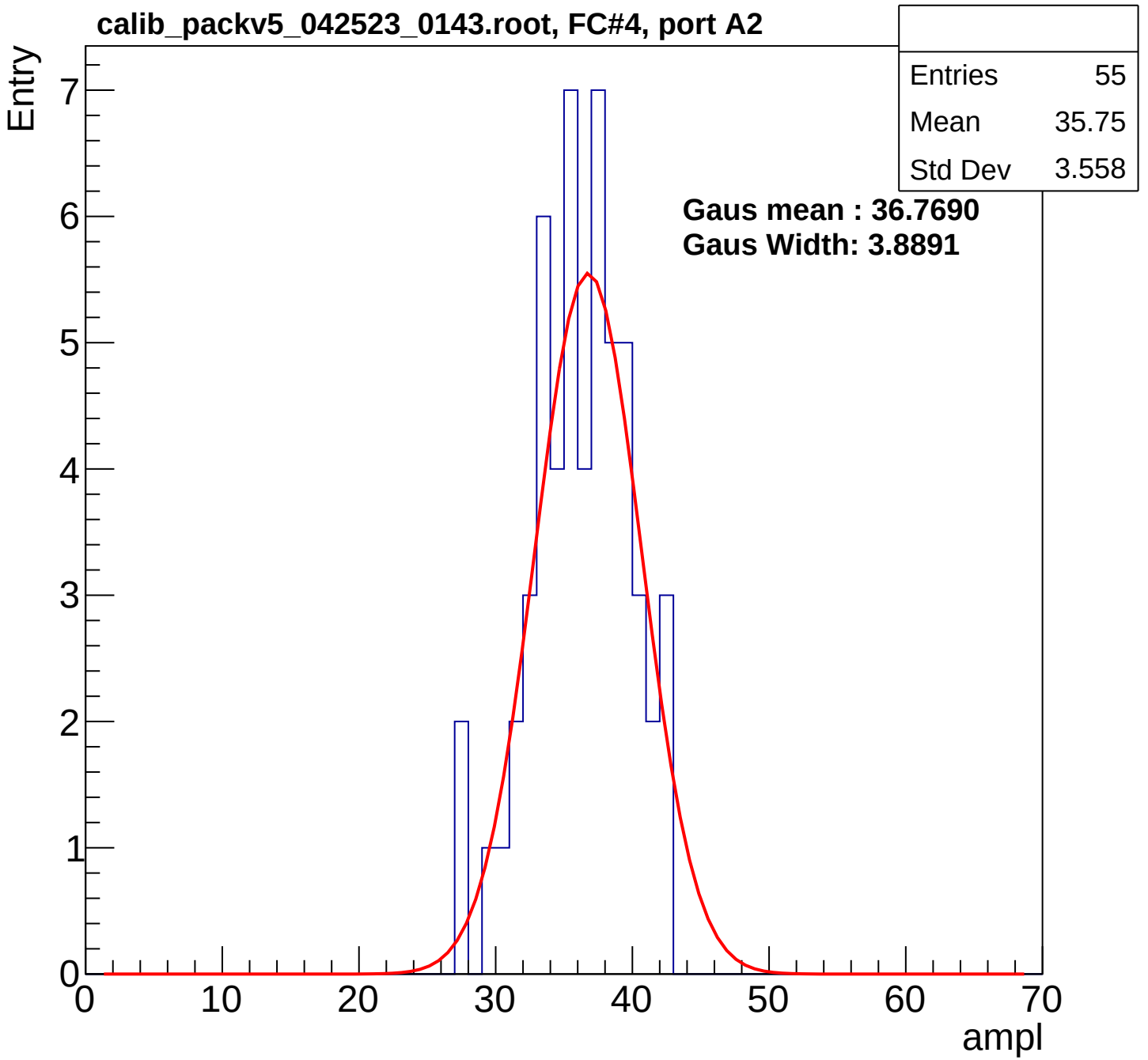
B1L100S, U17-ch92, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 35.75
Std Dev 3.558
Gaus mean : 36.7690
Gaus Width: 3.8891
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
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60
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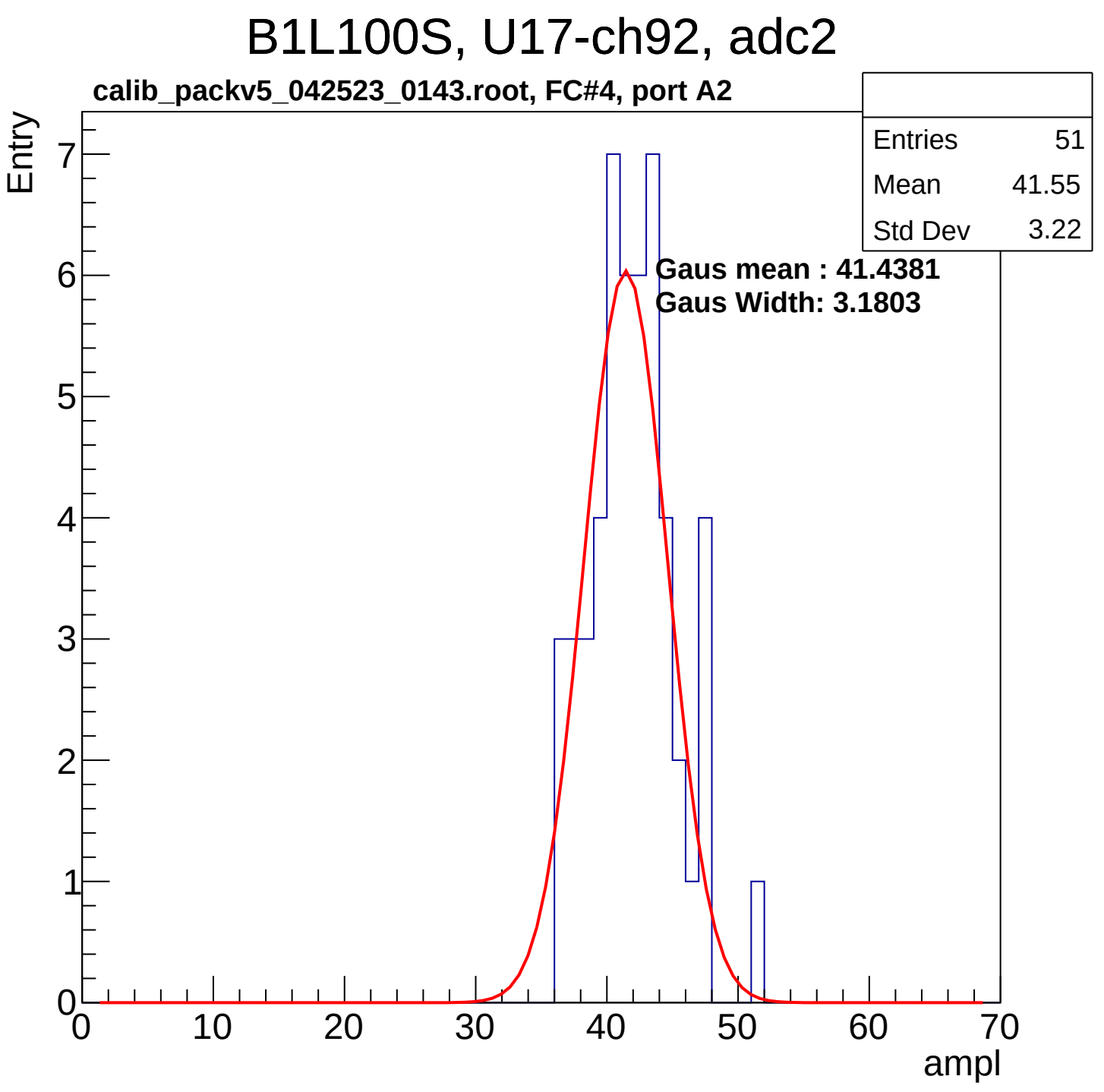
B1L100S, U17-ch92, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 41.55
Std Dev 3.22
Gaus mean : 41.4381
Gaus Width: 3.1803
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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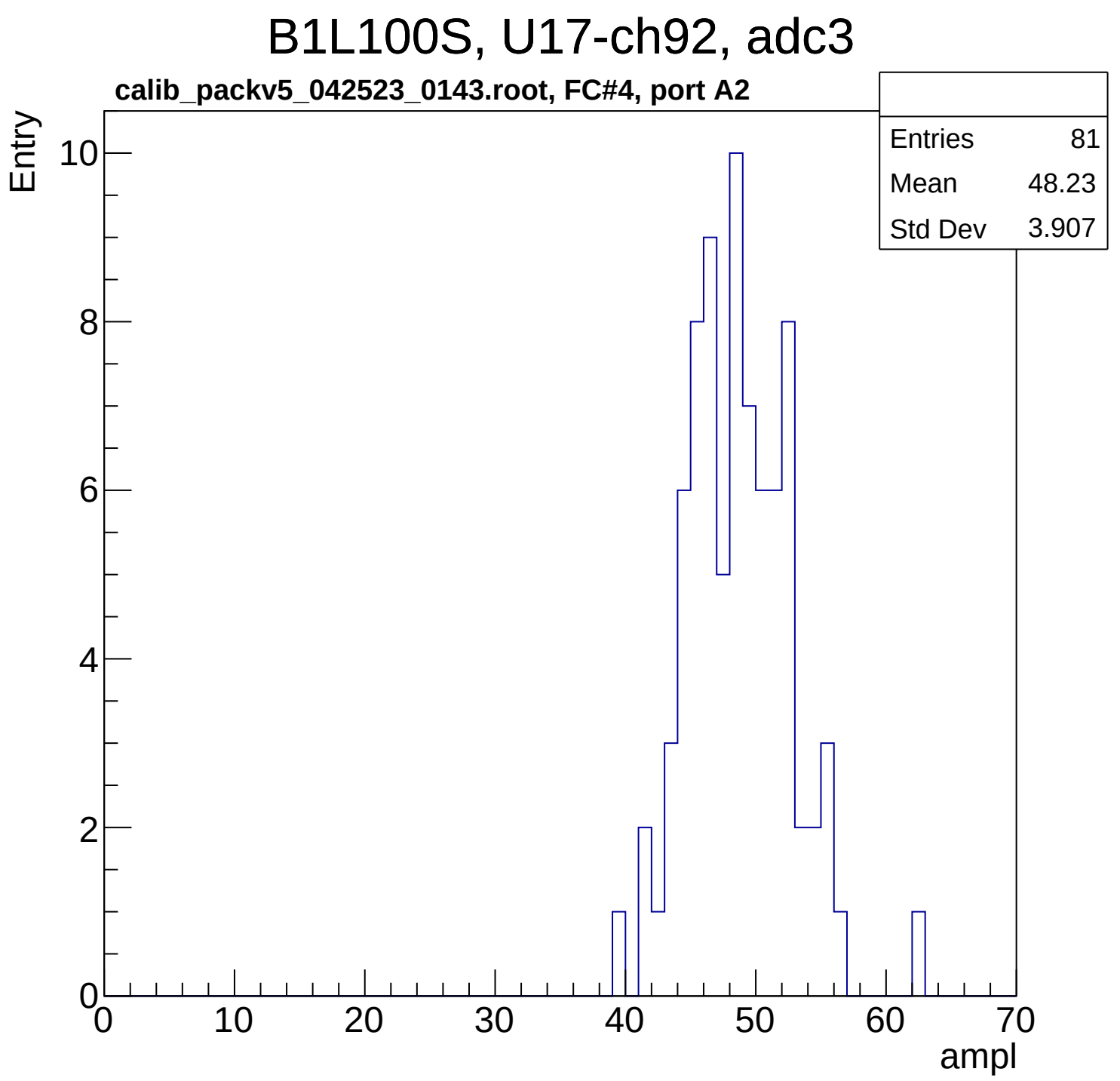
B1L100S, U17-ch92, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 81
Mean 48.23
Std Dev 3.907
Entry
ampl
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0
10
20
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40
50
60
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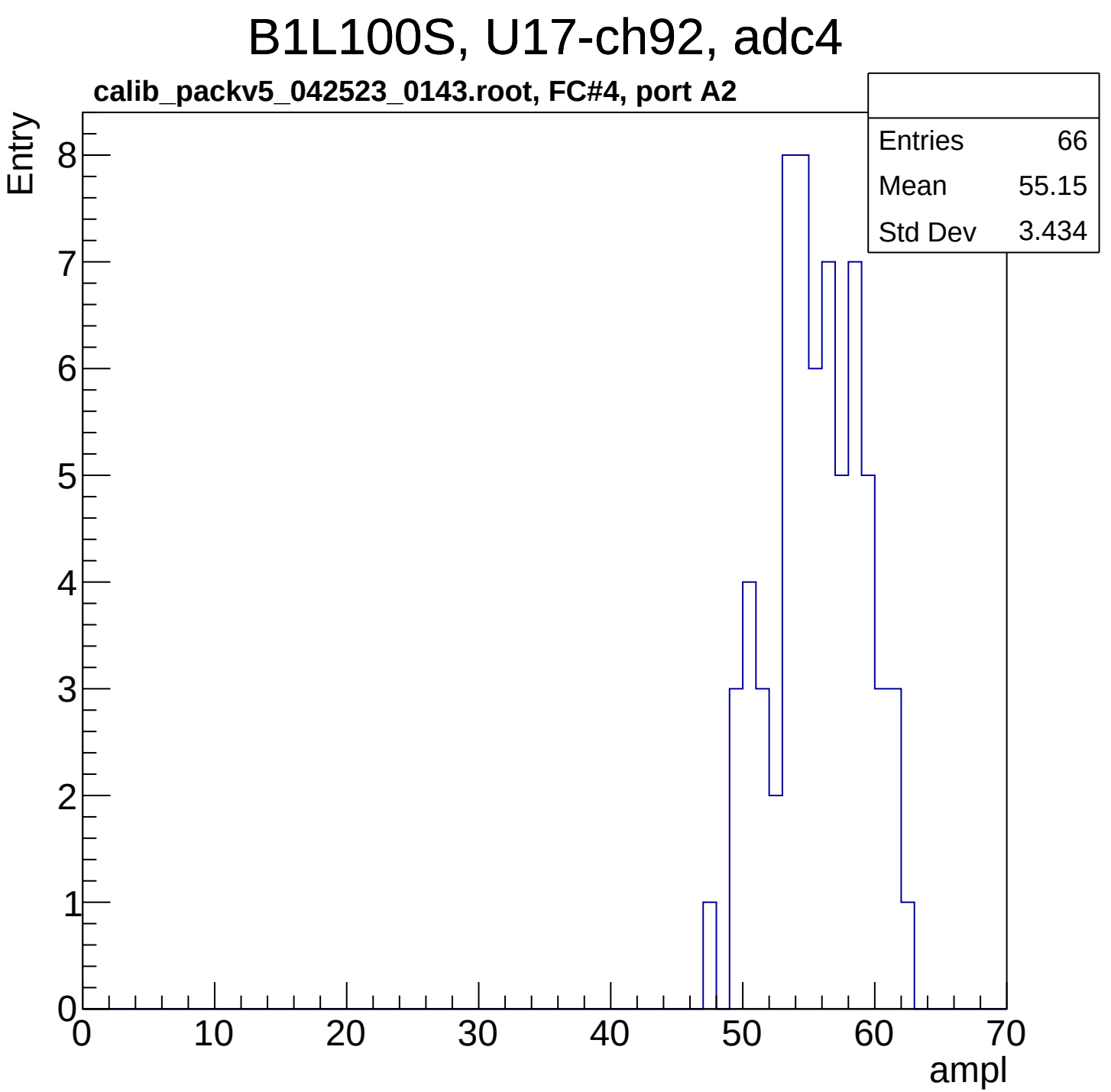
B1L100S, U17-ch92, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 55.15
Std Dev 3.434
Entry
ampl
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1
2
3
4
5
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7
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0
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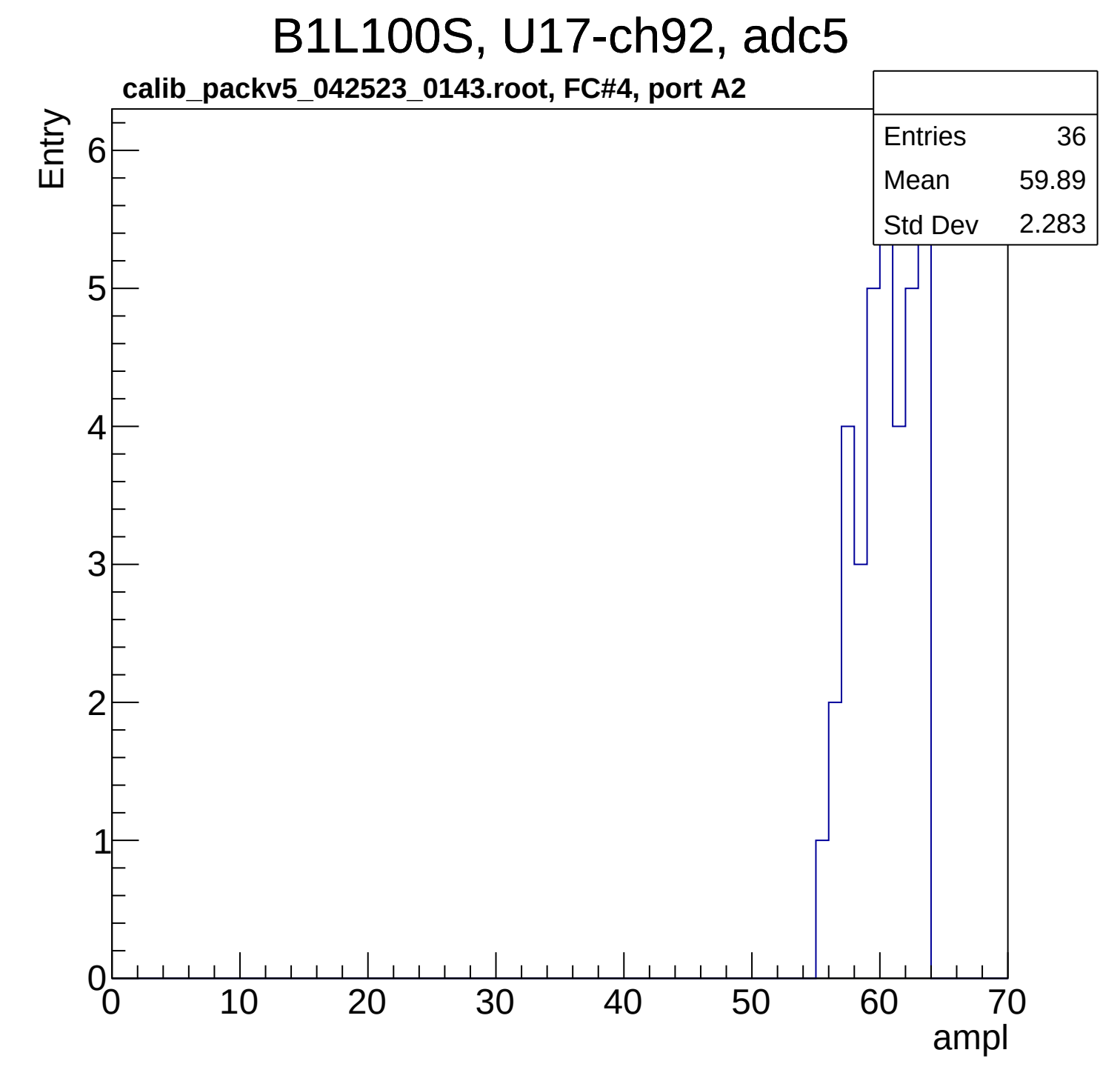
B1L100S, U17-ch92, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 36
Mean 59.89
Std Dev 2.283
Entry
ampl
0
1
2
3
4
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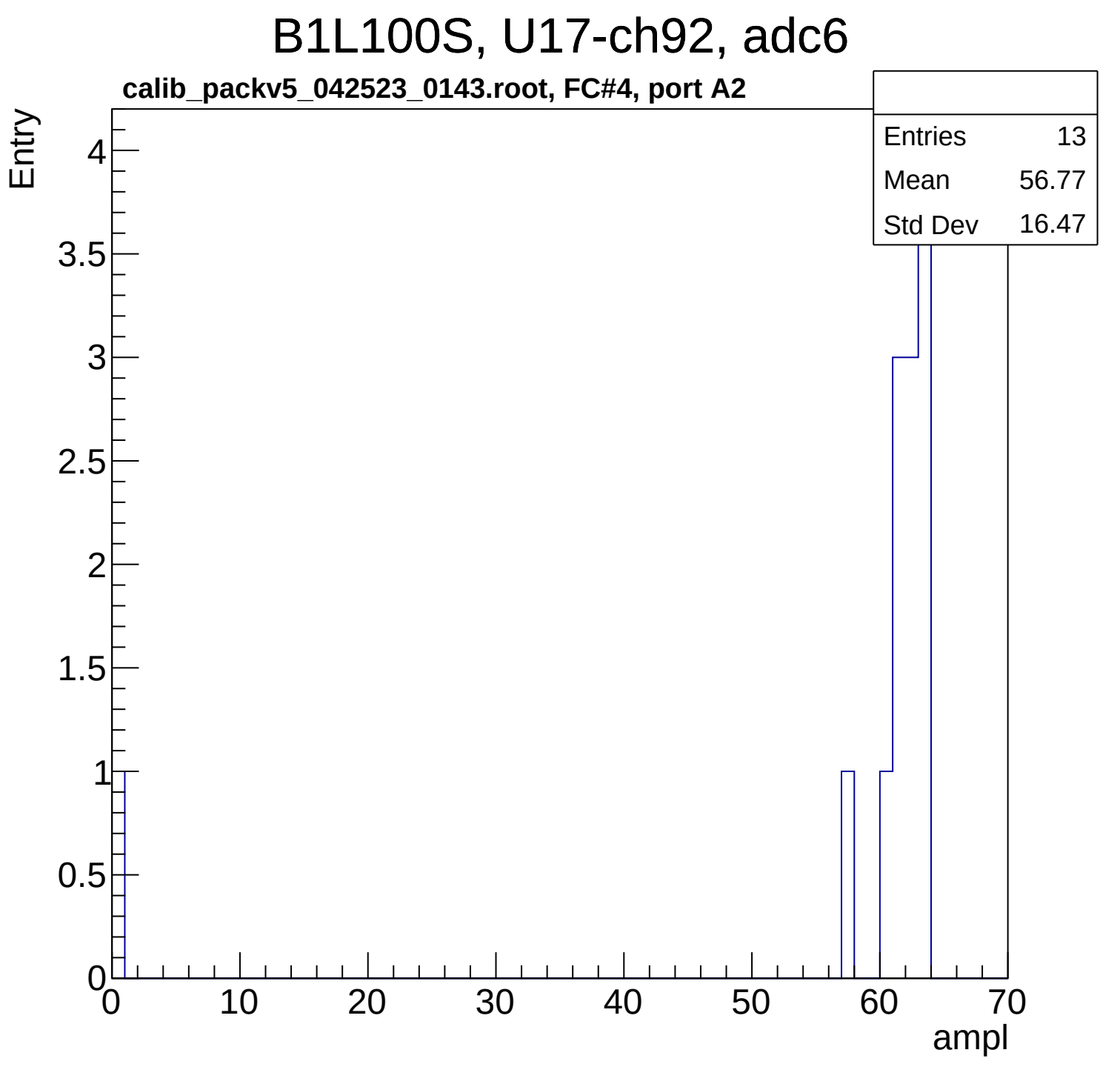
B1L100S, U17-ch92, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 13
Mean 56.77
Std Dev 16.47
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
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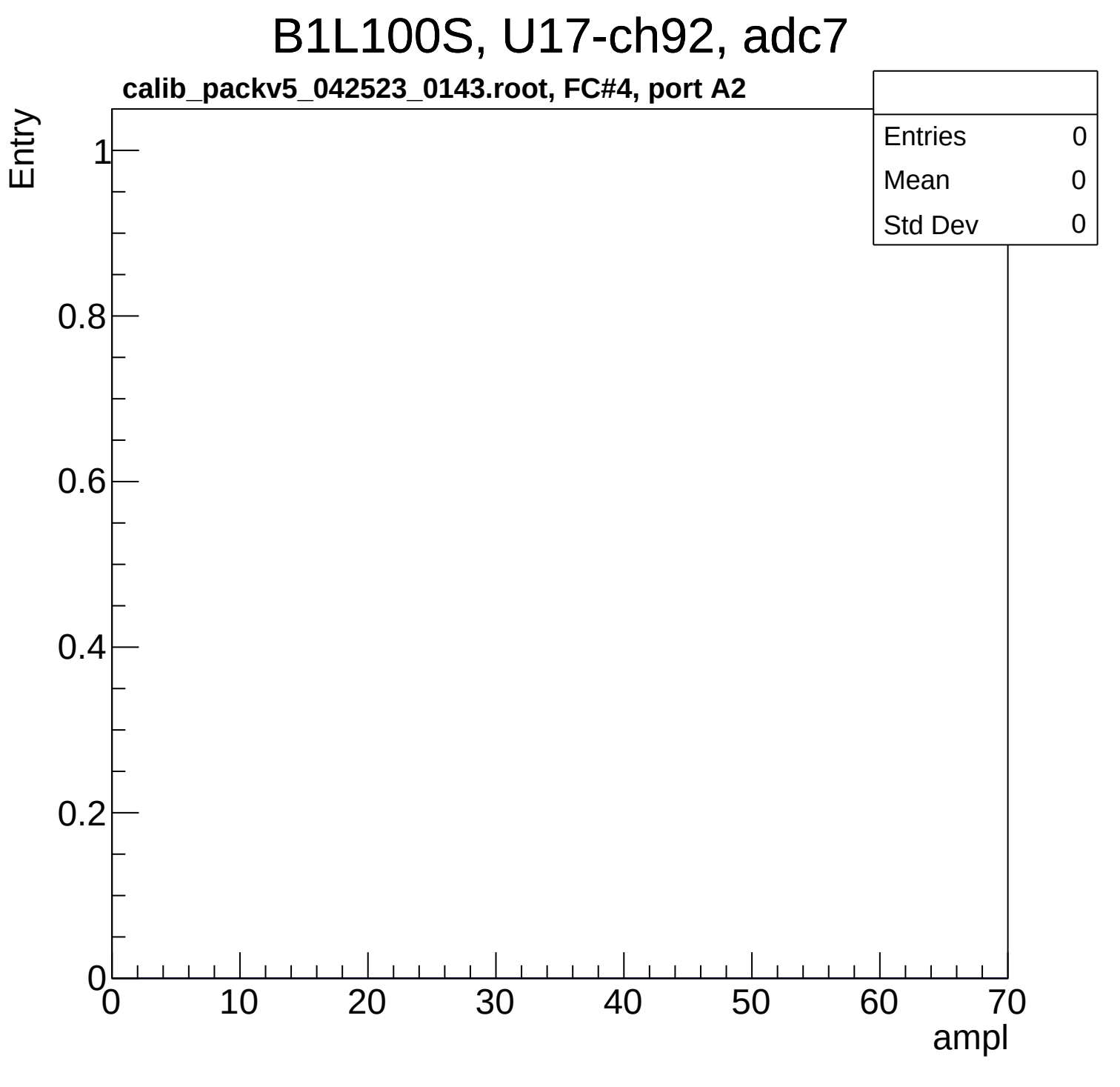
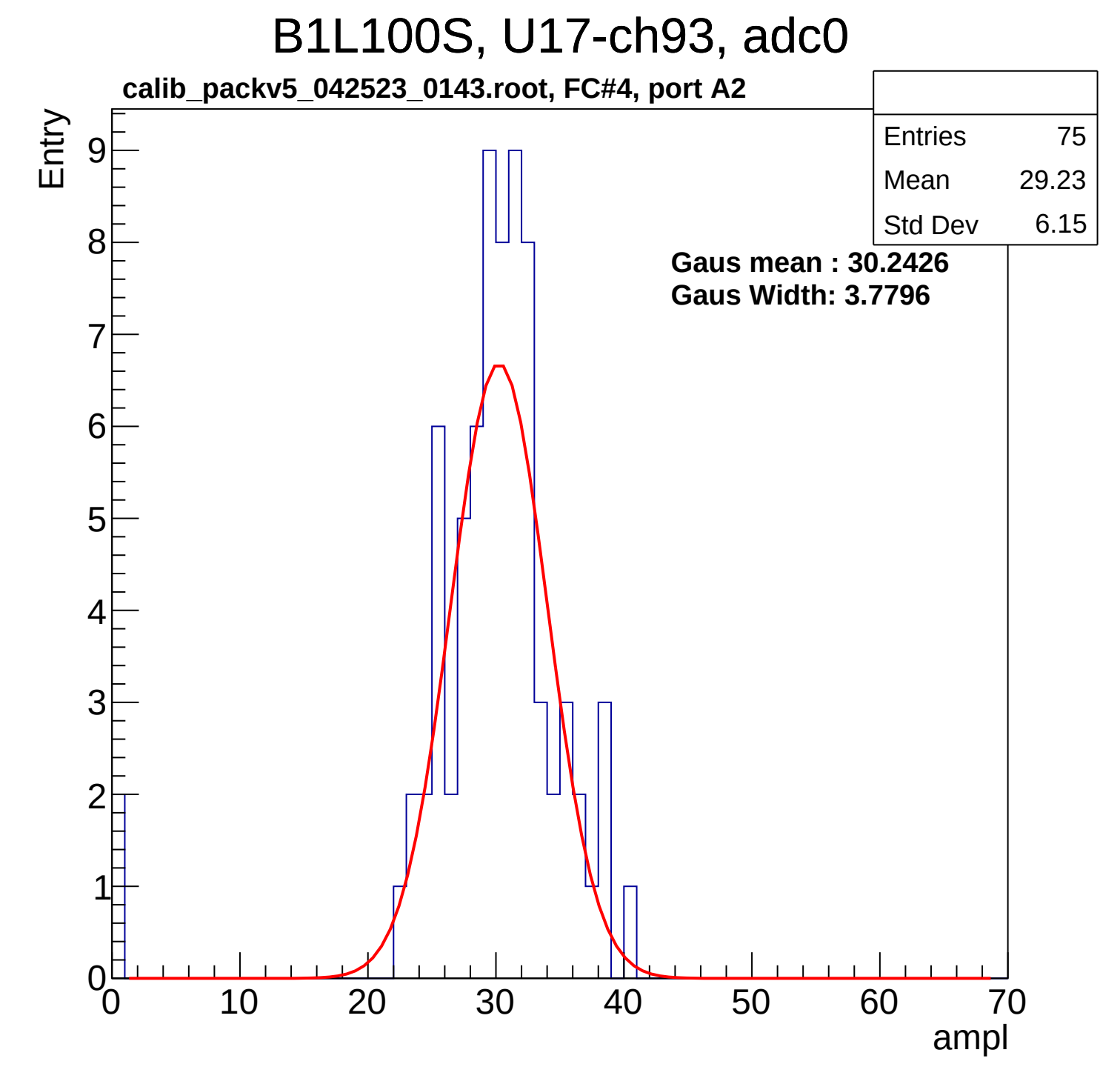

B1L100S, U17-ch92, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch93, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 75
Mean 29.23
Std Dev 6.15
Gaus mean : 30.2426
Gaus Width: 3.7796
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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20
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40
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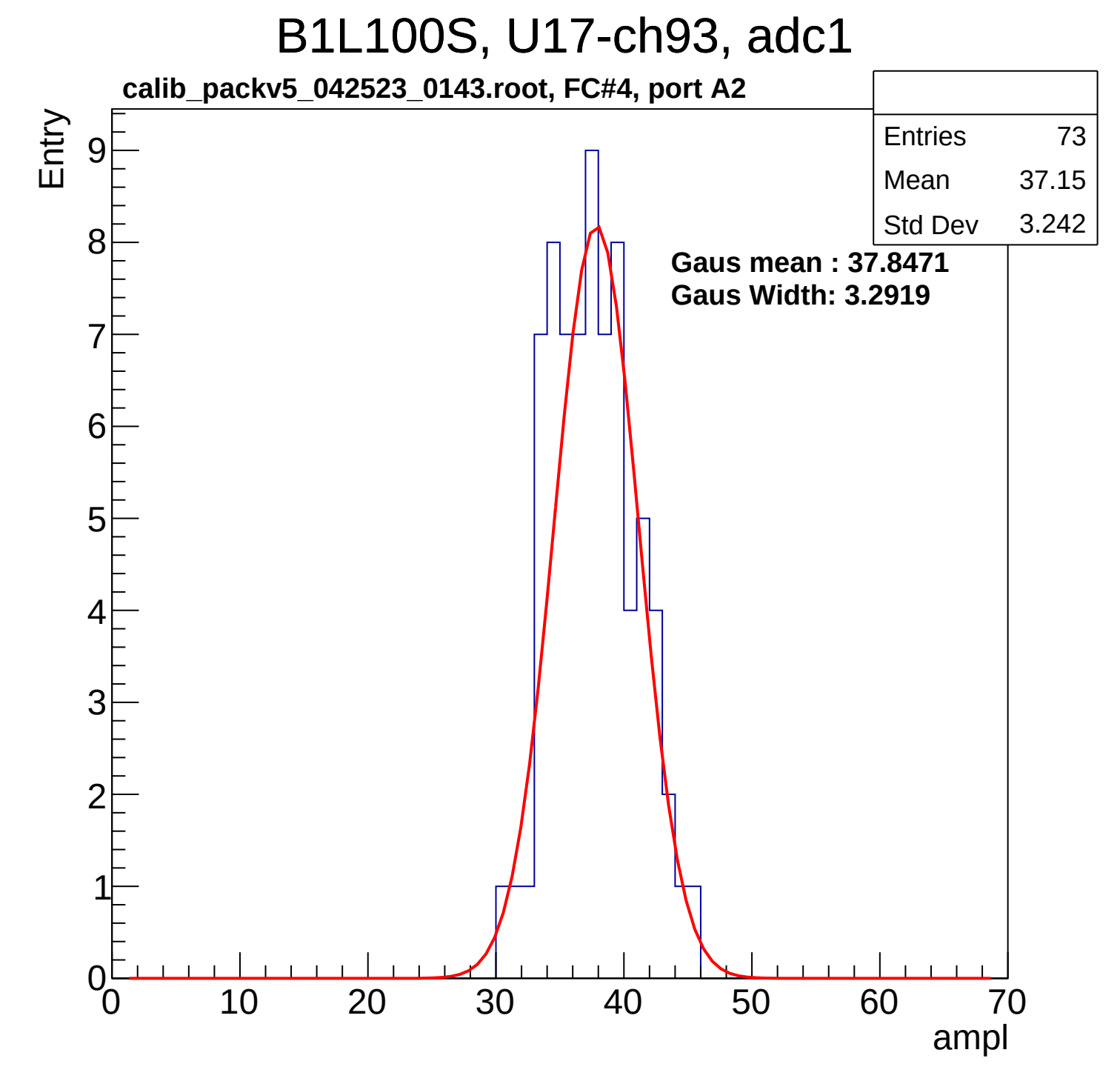
B1L100S, U17-ch93, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 37.15
Std Dev 3.242
Gaus mean : 37.8471
Gaus Width: 3.2919
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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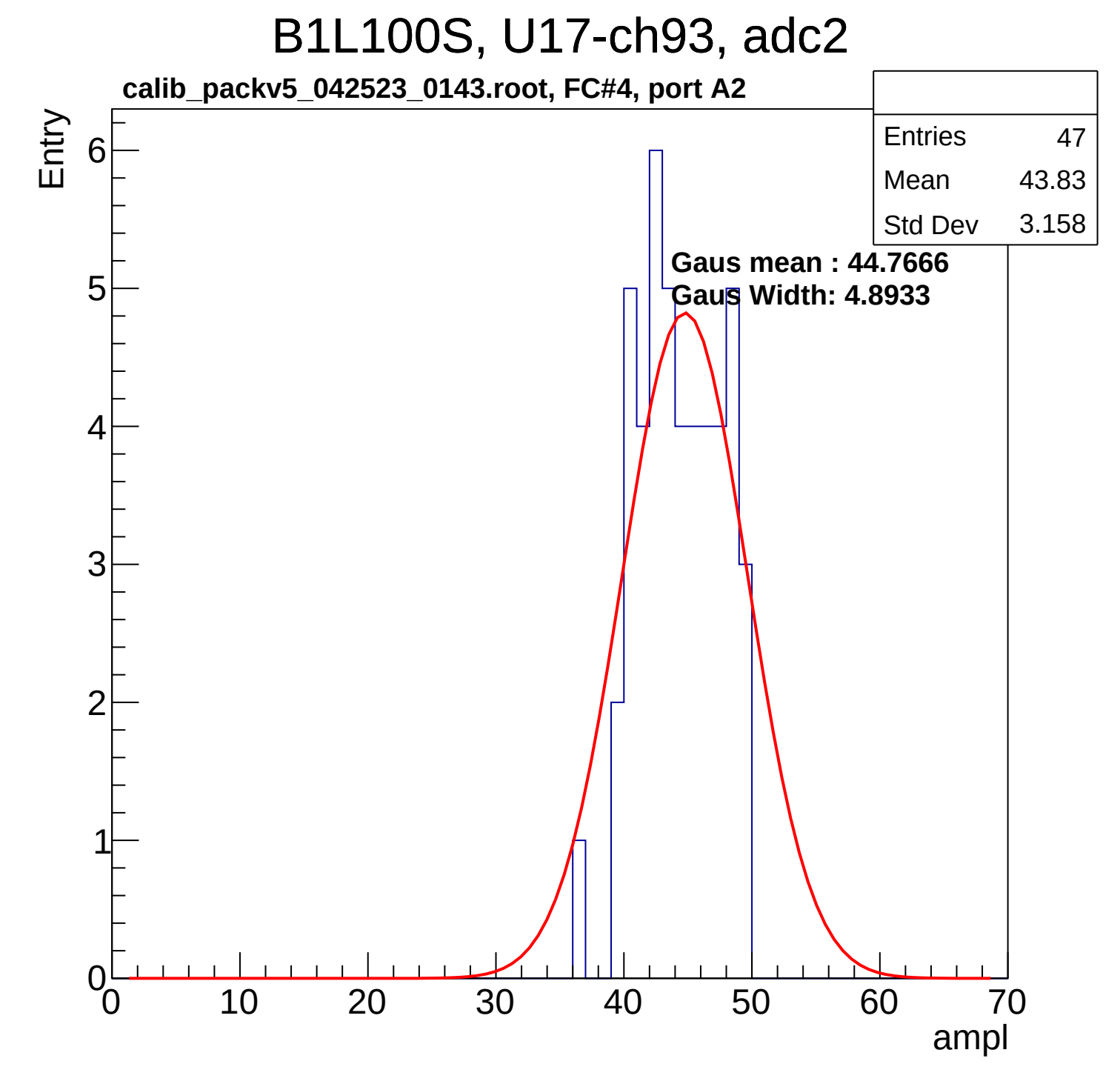
B1L100S, U17-ch93, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 47
Mean 43.83
Std Dev 3.158
Gaus mean : 44.7666
Gaus Width: 4.8933
Entry
ampl
0
1
2
3
4
5
6
0
10
20
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40
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60
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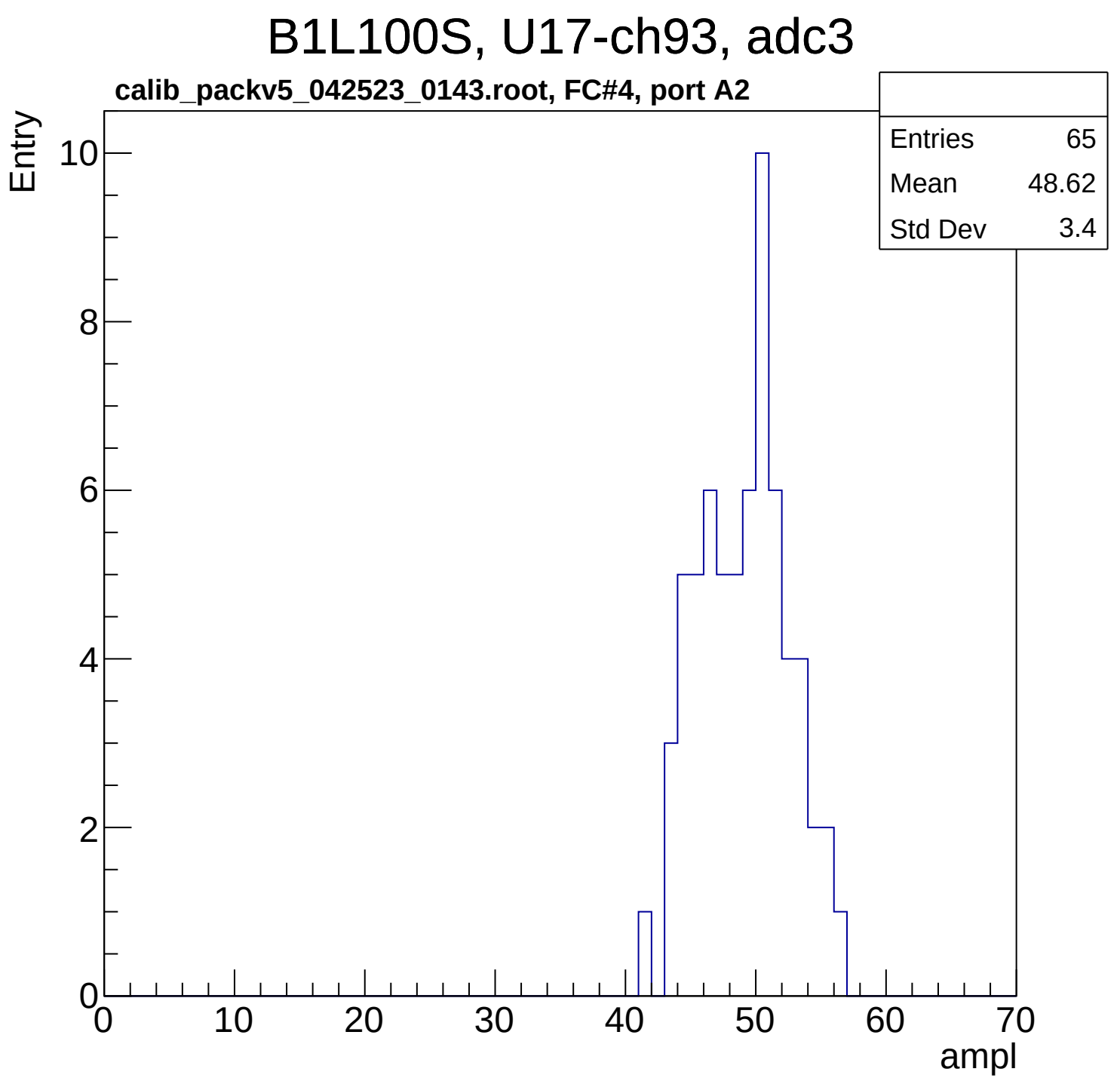
B1L100S, U17-ch93, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 48.62
Std Dev 3.4
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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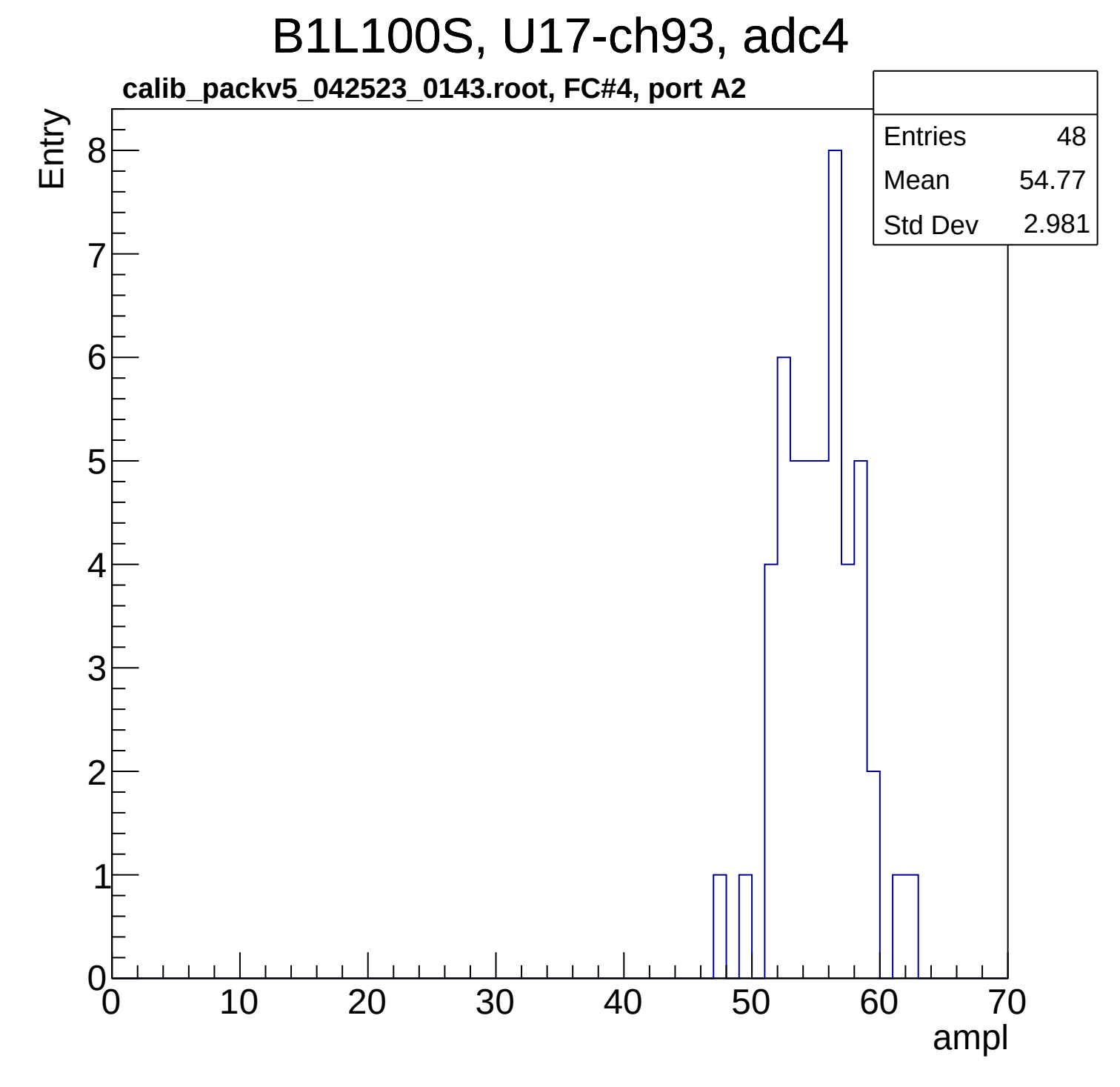
B1L100S, U17-ch93, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 48
Mean 54.77
Std Dev 2.981
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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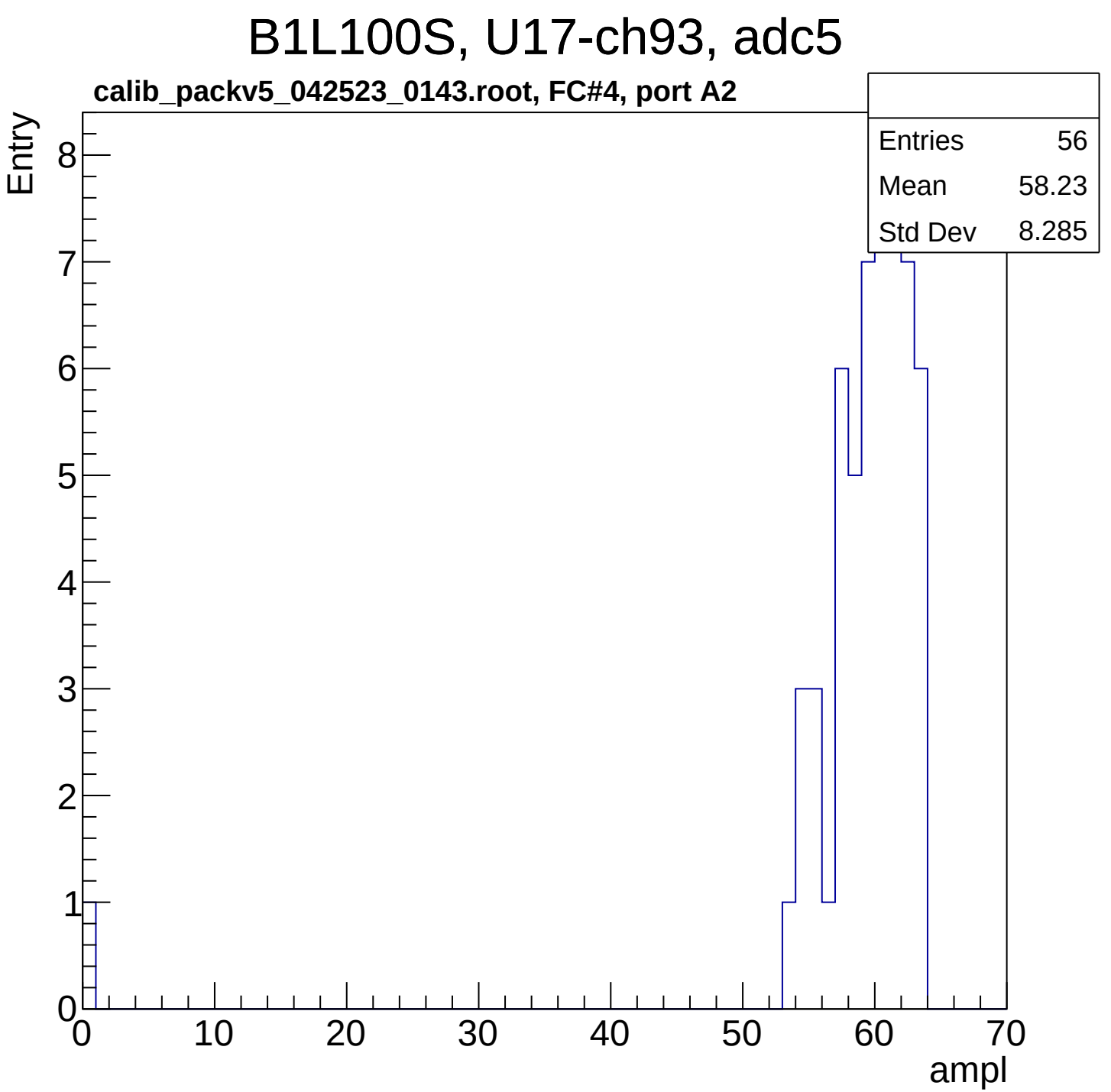
B1L100S, U17-ch93, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 58.23
Std Dev 8.285
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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60
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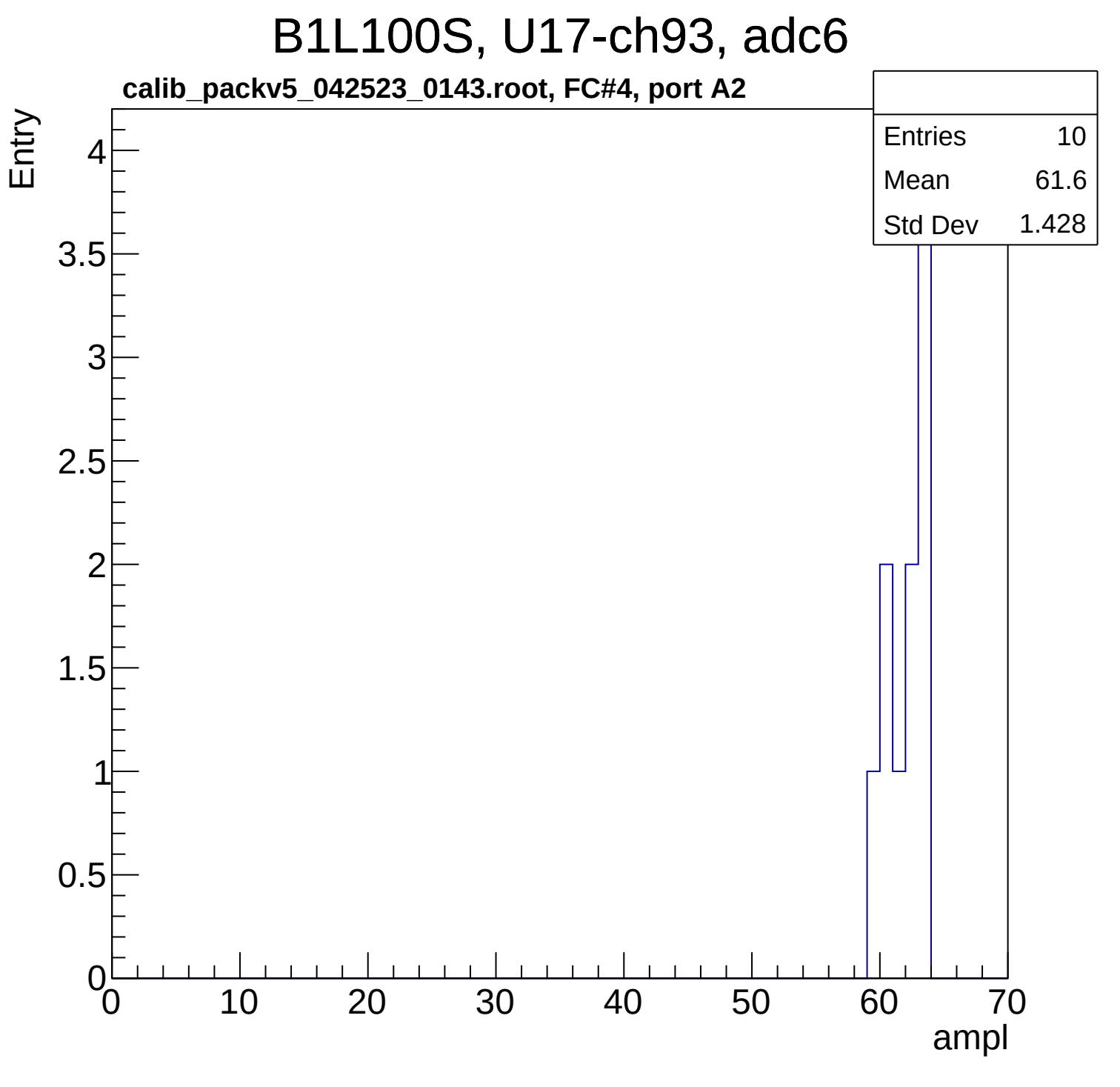
B1L100S, U17-ch93, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 10
Mean 61.6
Std Dev 1.428
Entry
ampl
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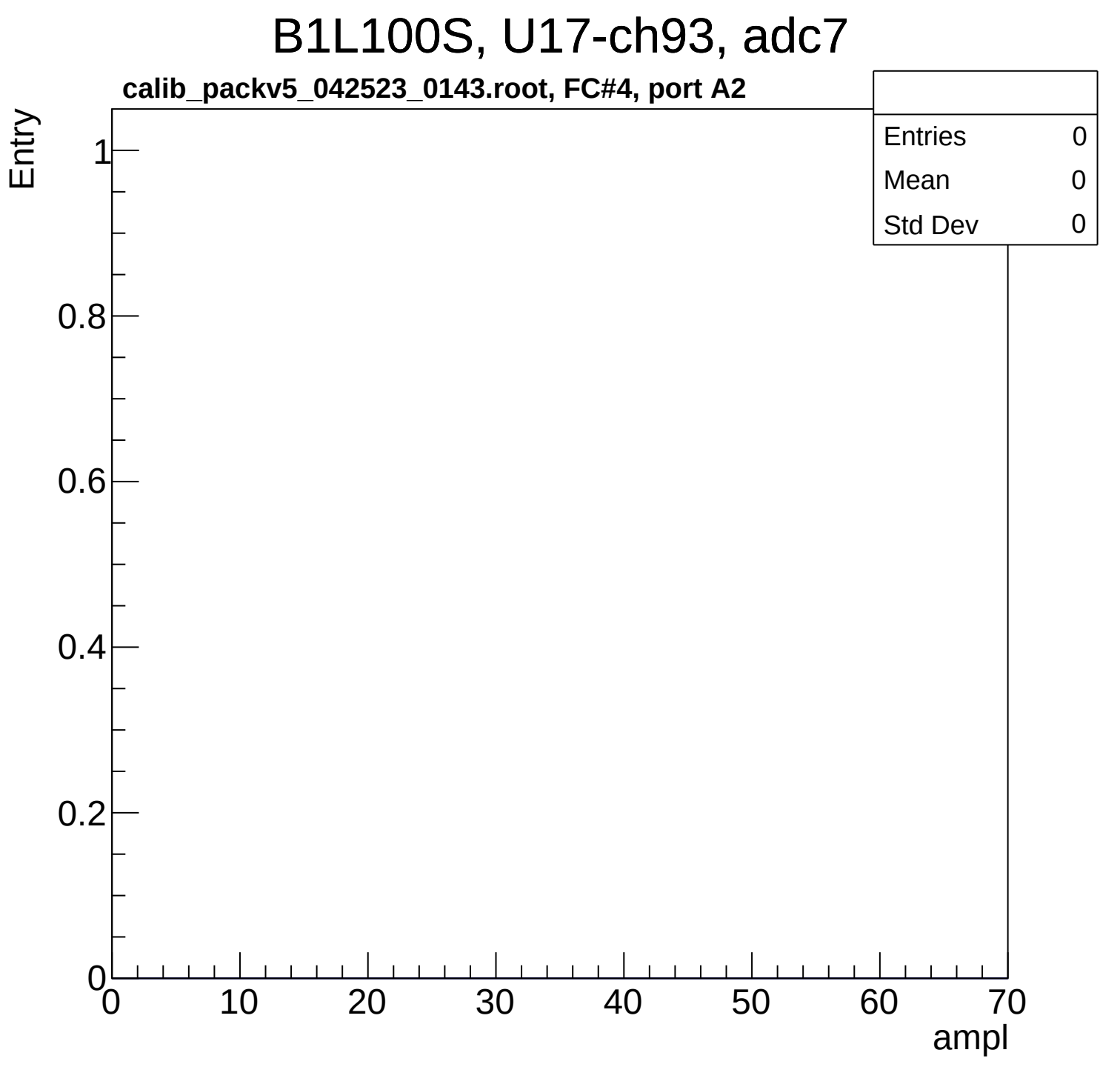
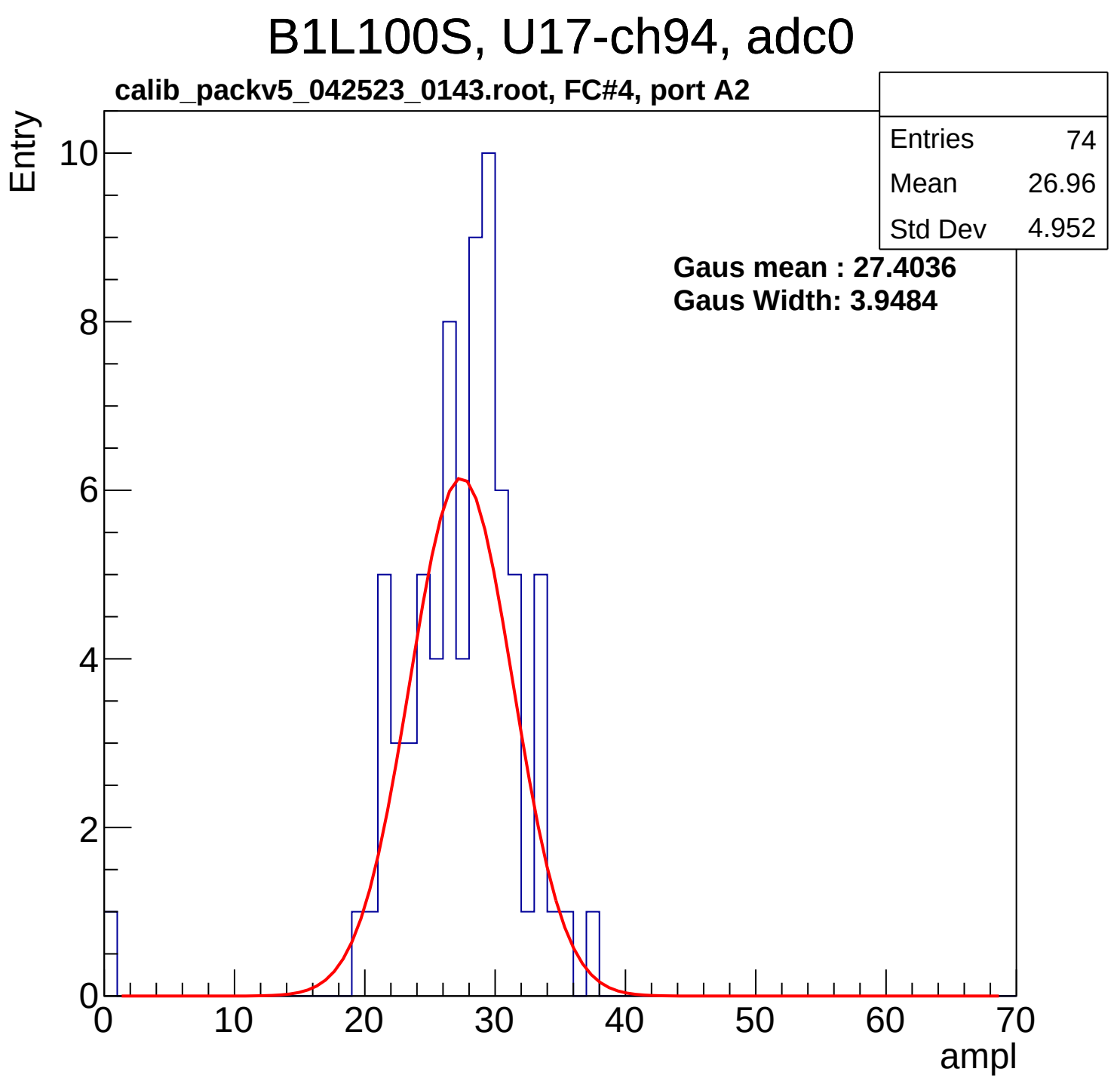
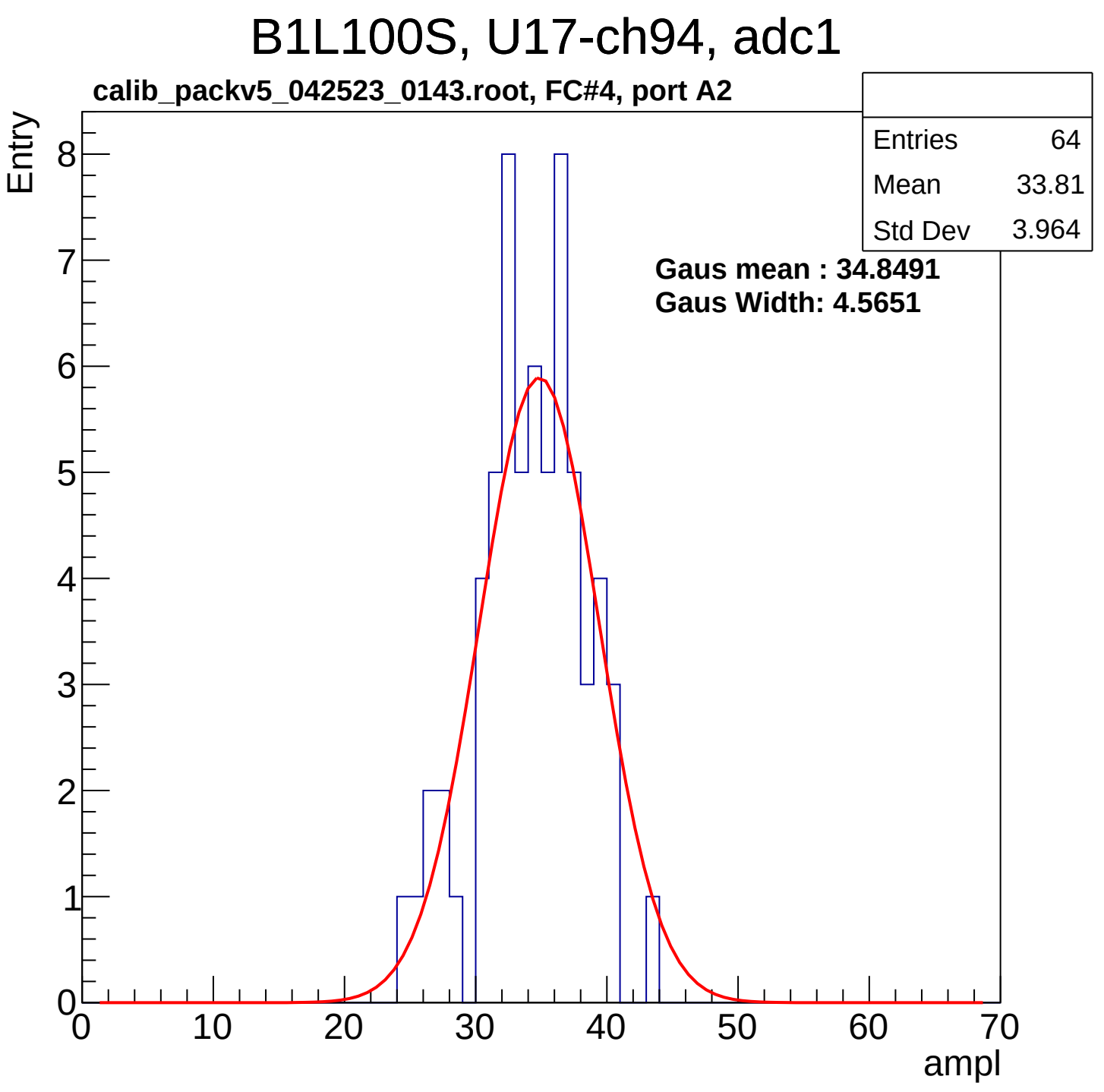
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L100S, U17-ch93, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch94, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 74
Mean 26.96
Std Dev 4.952
Gaus mean : 27.4036
Gaus Width: 3.9484
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U17-ch94, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 33.81
Std Dev 3.964
Gaus mean : 34.8491
Gaus Width: 4.5651
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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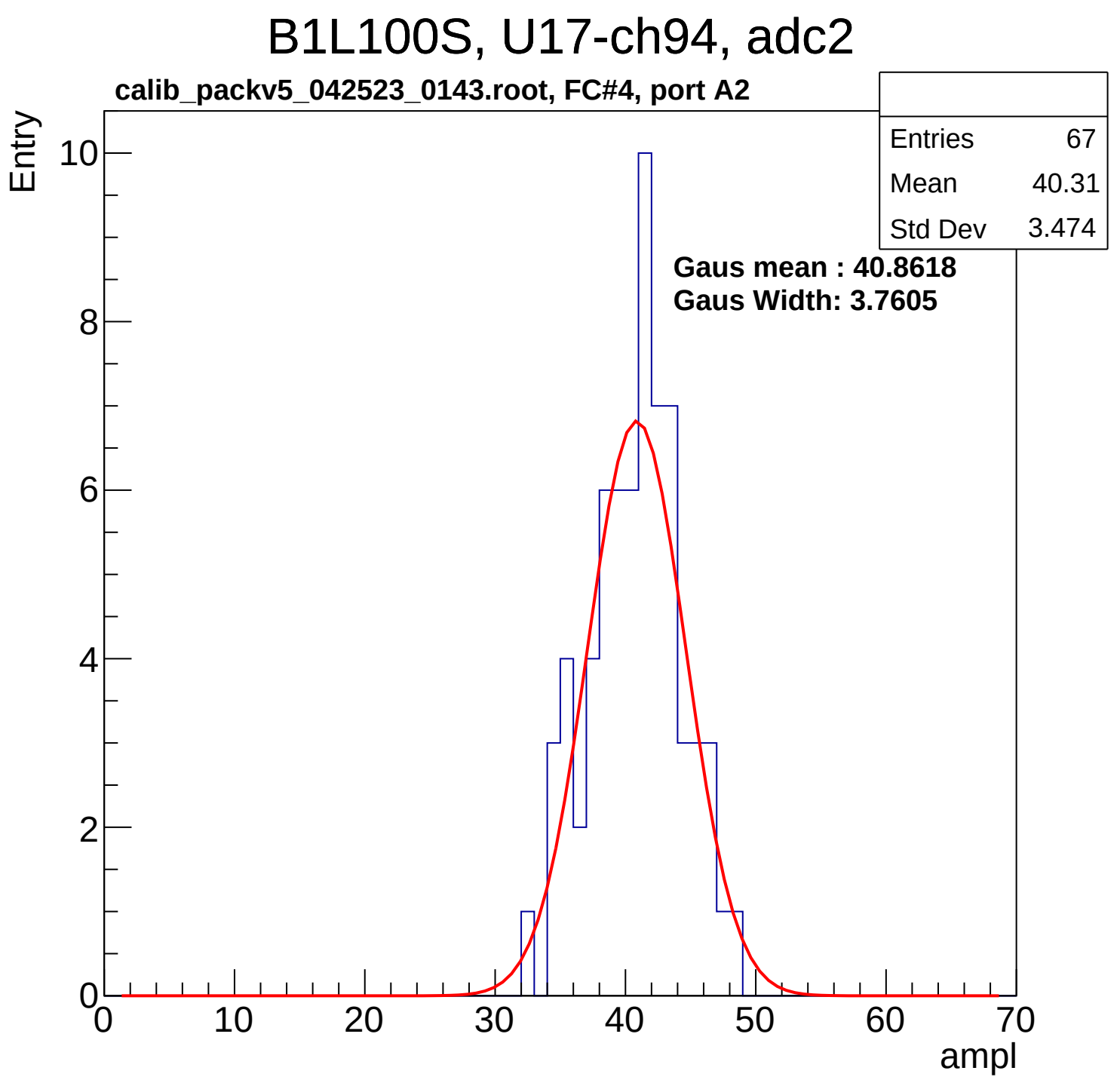
B1L100S, U17-ch94, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 40.31
Std Dev 3.474
Gaus mean : 40.8618
Gaus Width: 3.7605
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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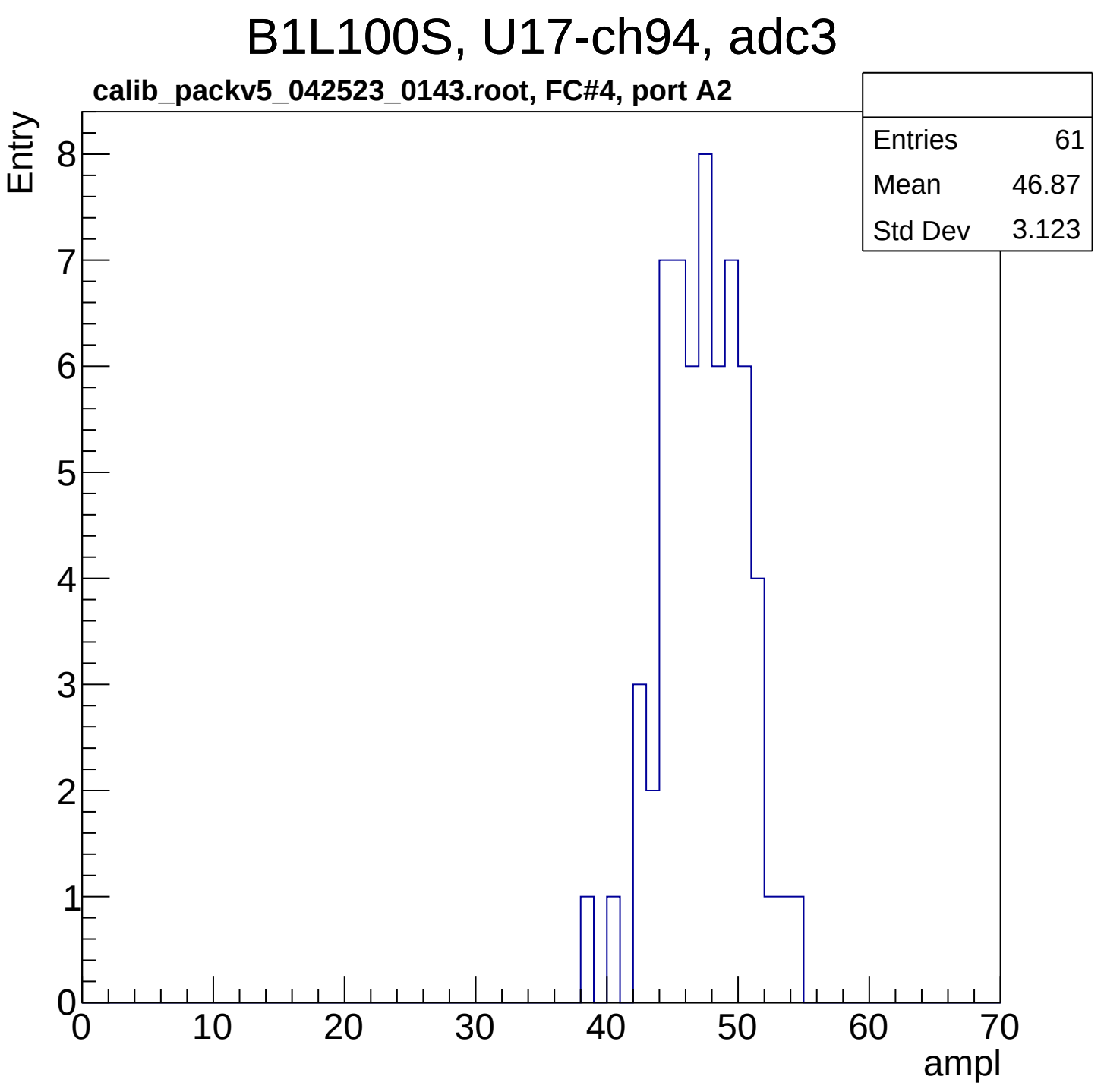
B1L100S, U17-ch94, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 46.87
Std Dev 3.123
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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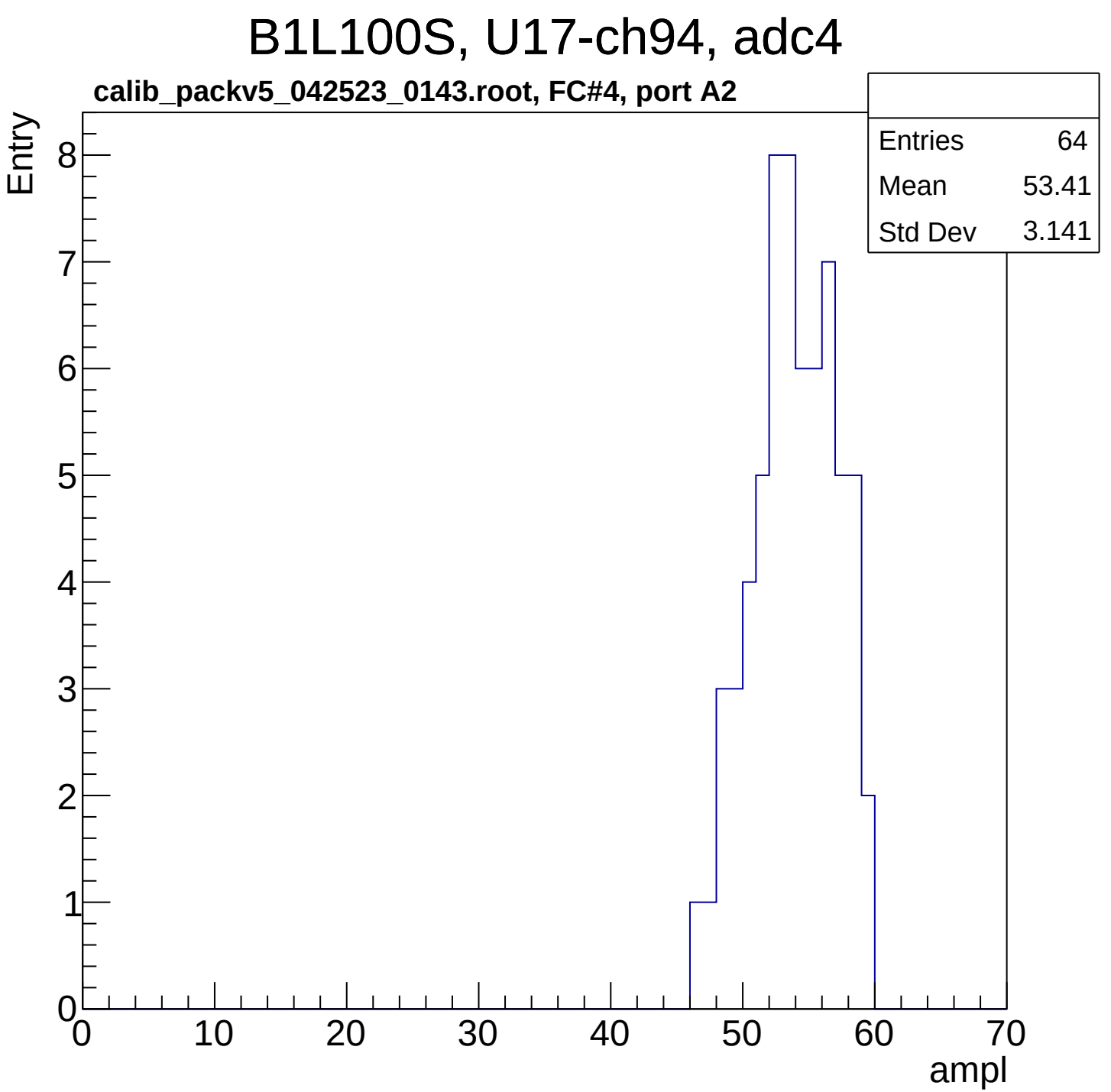
B1L100S, U17-ch94, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 53.41
Std Dev 3.141
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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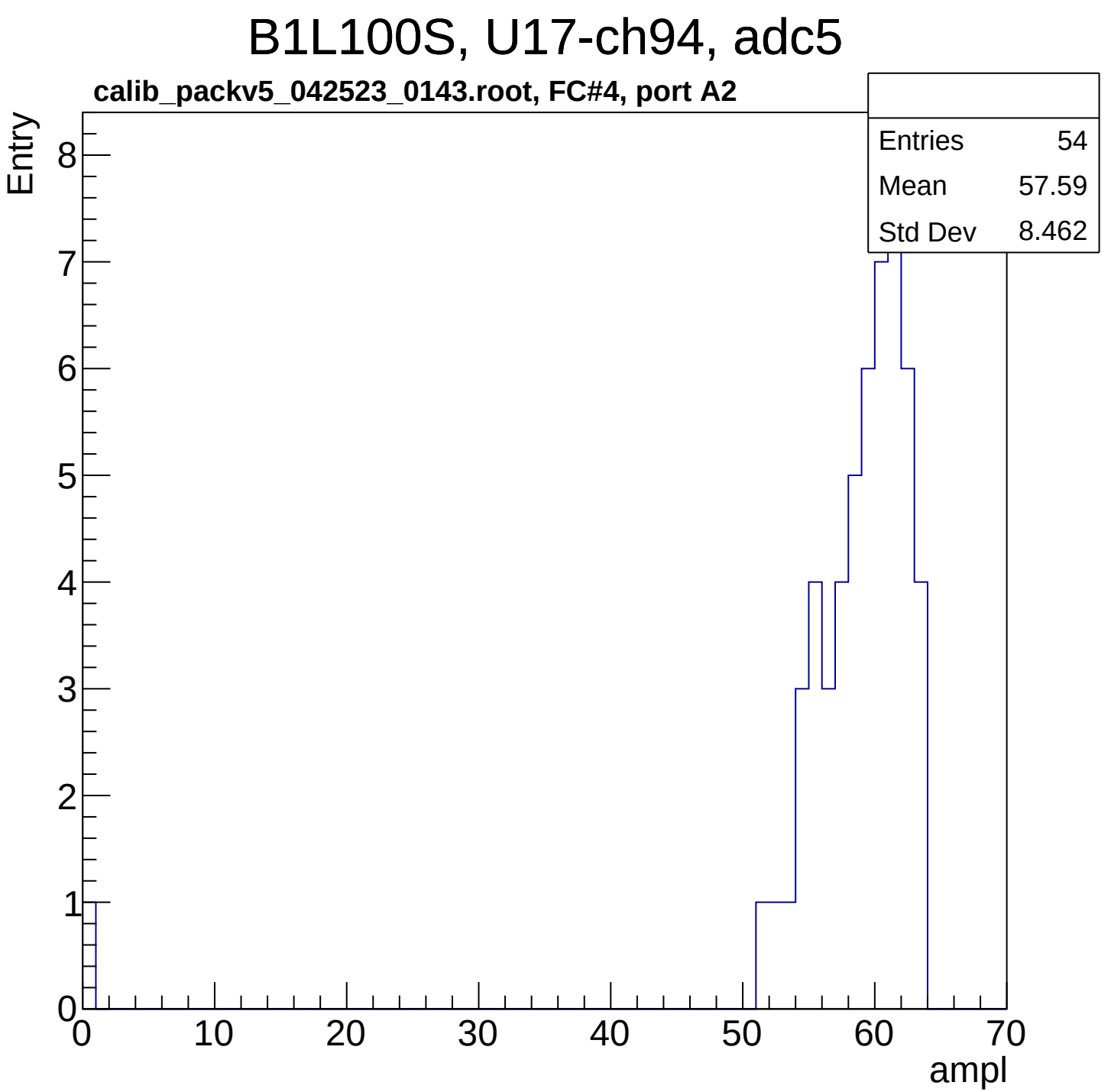
B1L100S, U17-ch94, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 57.59
Std Dev 8.462
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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60
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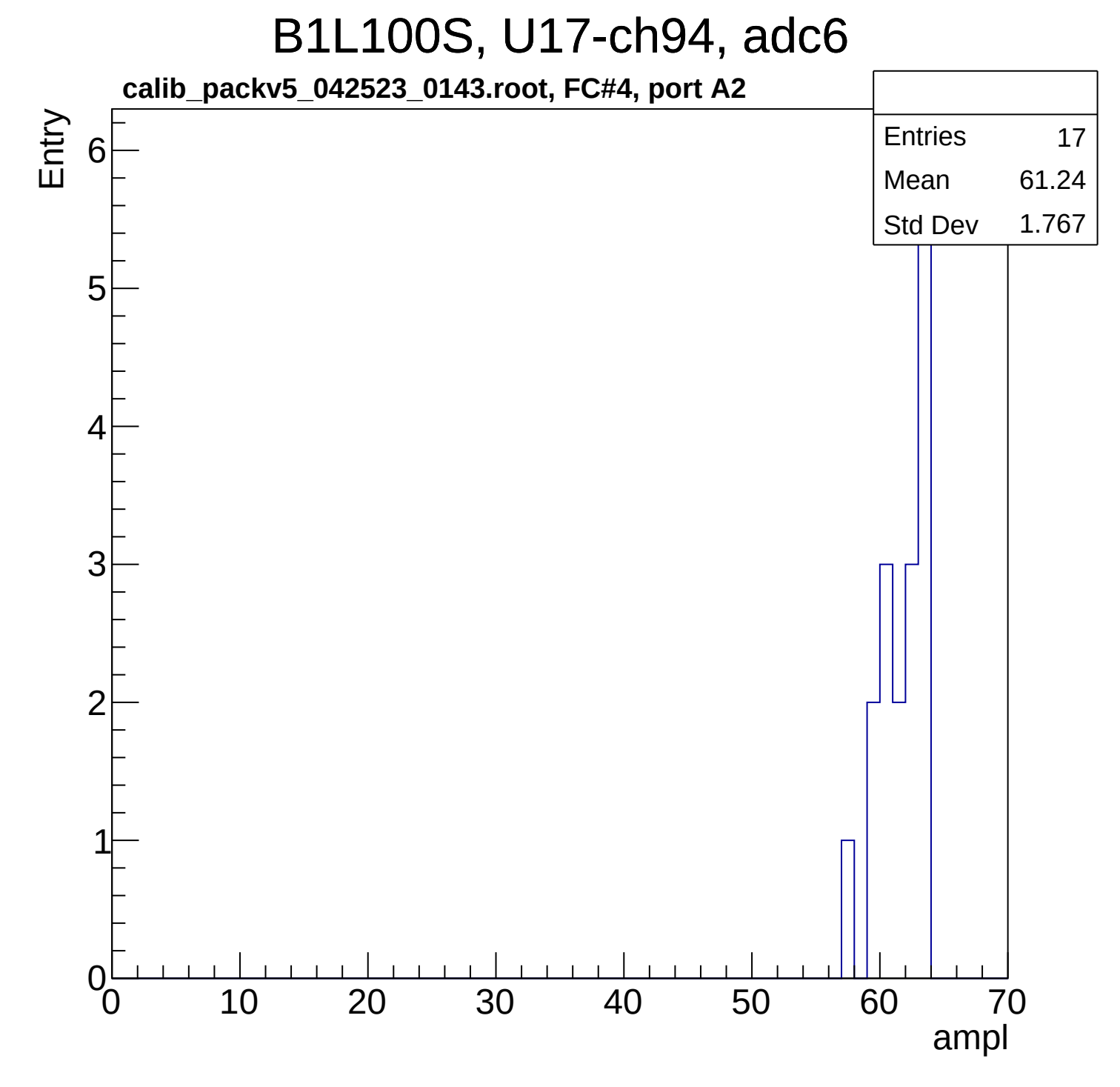
B1L100S, U17-ch94, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 17
Mean 61.24
Std Dev 1.767
Entry
ampl
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2
3
4
5
6
0
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20
30
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50
60
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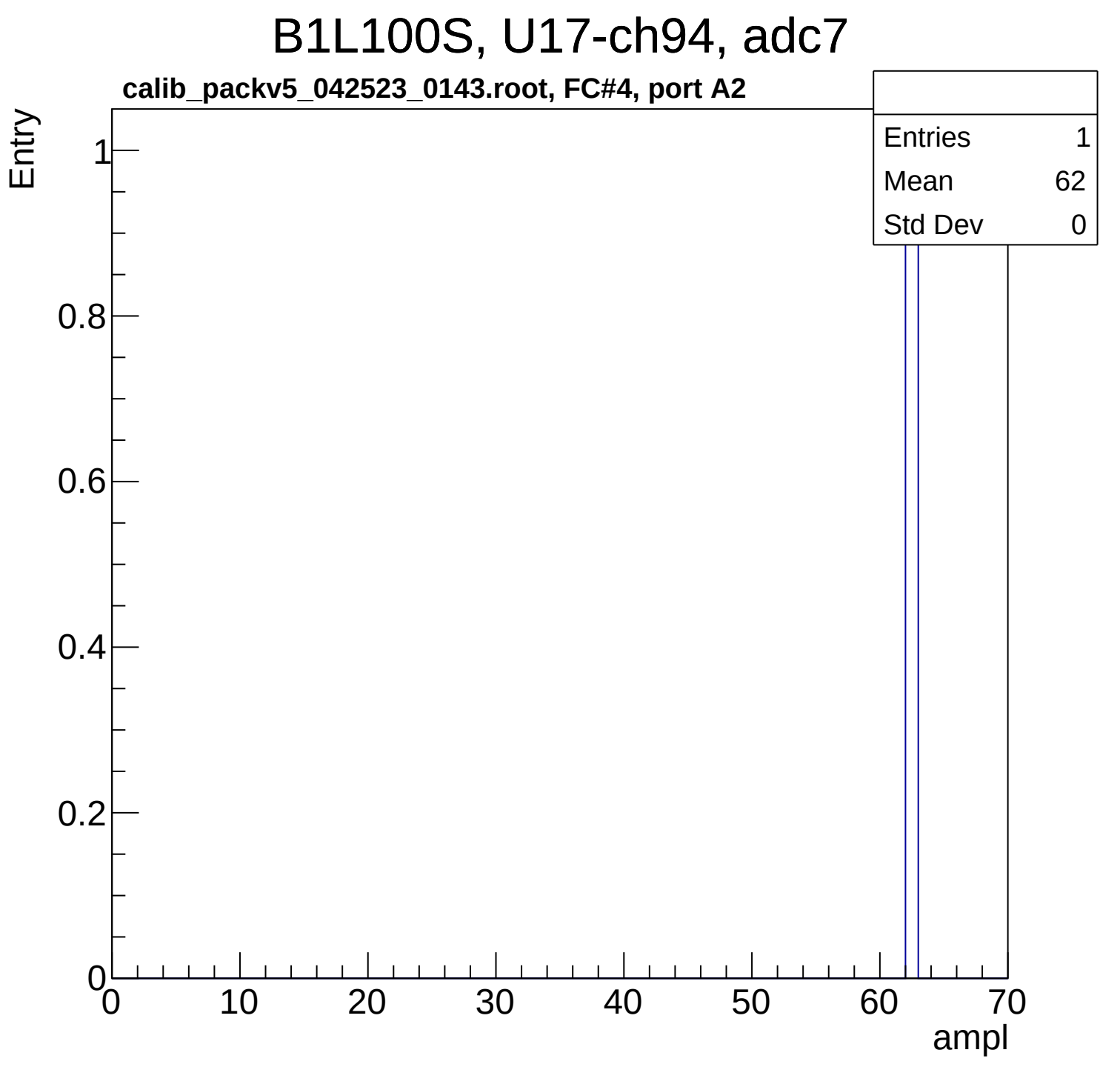
B1L100S, U17-ch94, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 62
Std Dev 0
Entry
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0.6
0.4
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10
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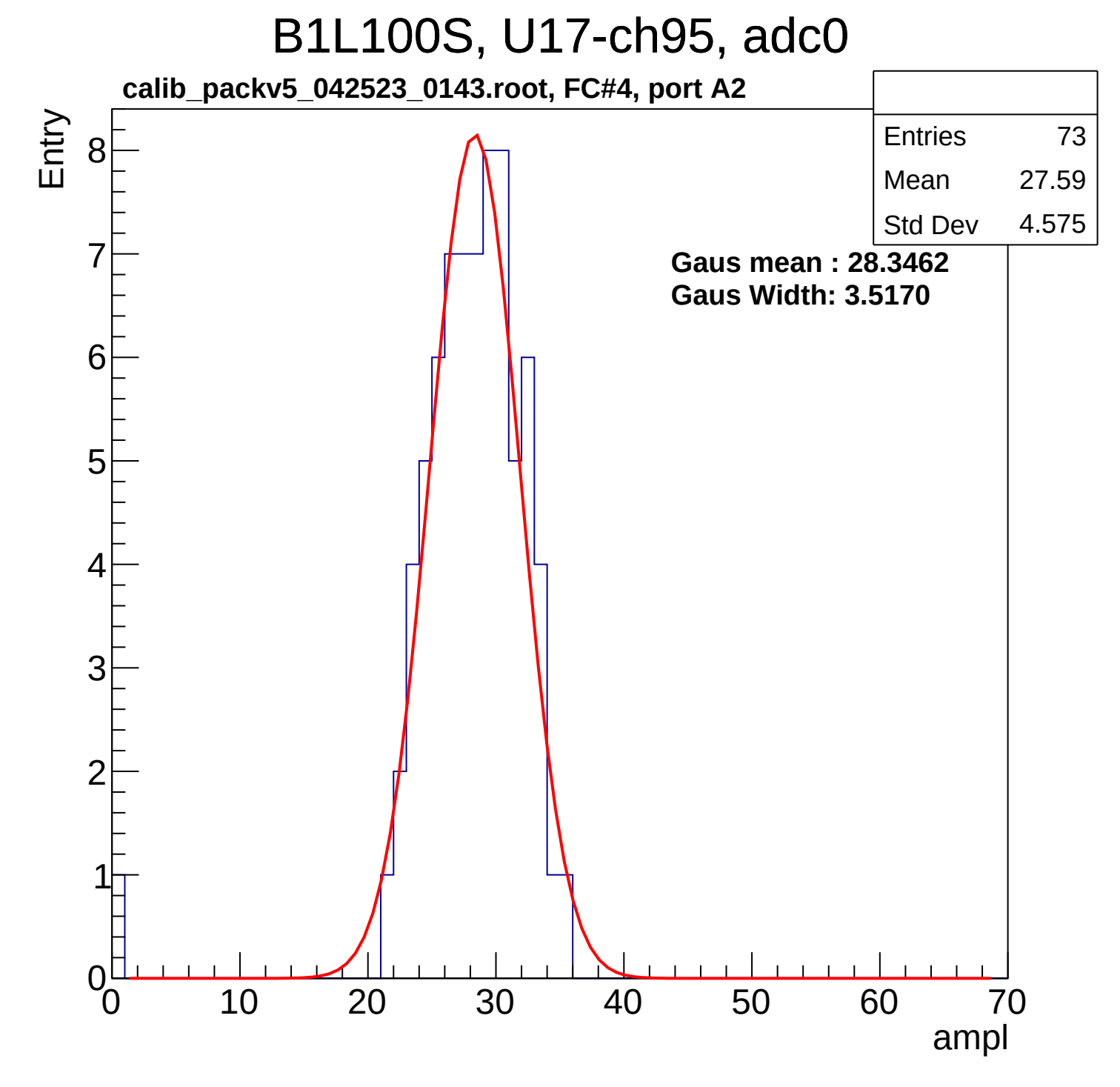
50
60
70
ampl


B1L100S, U17-ch95, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 27.59
Std Dev 4.575
Gaus mean : 28.3462
Gaus Width: 3.5170
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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40
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60
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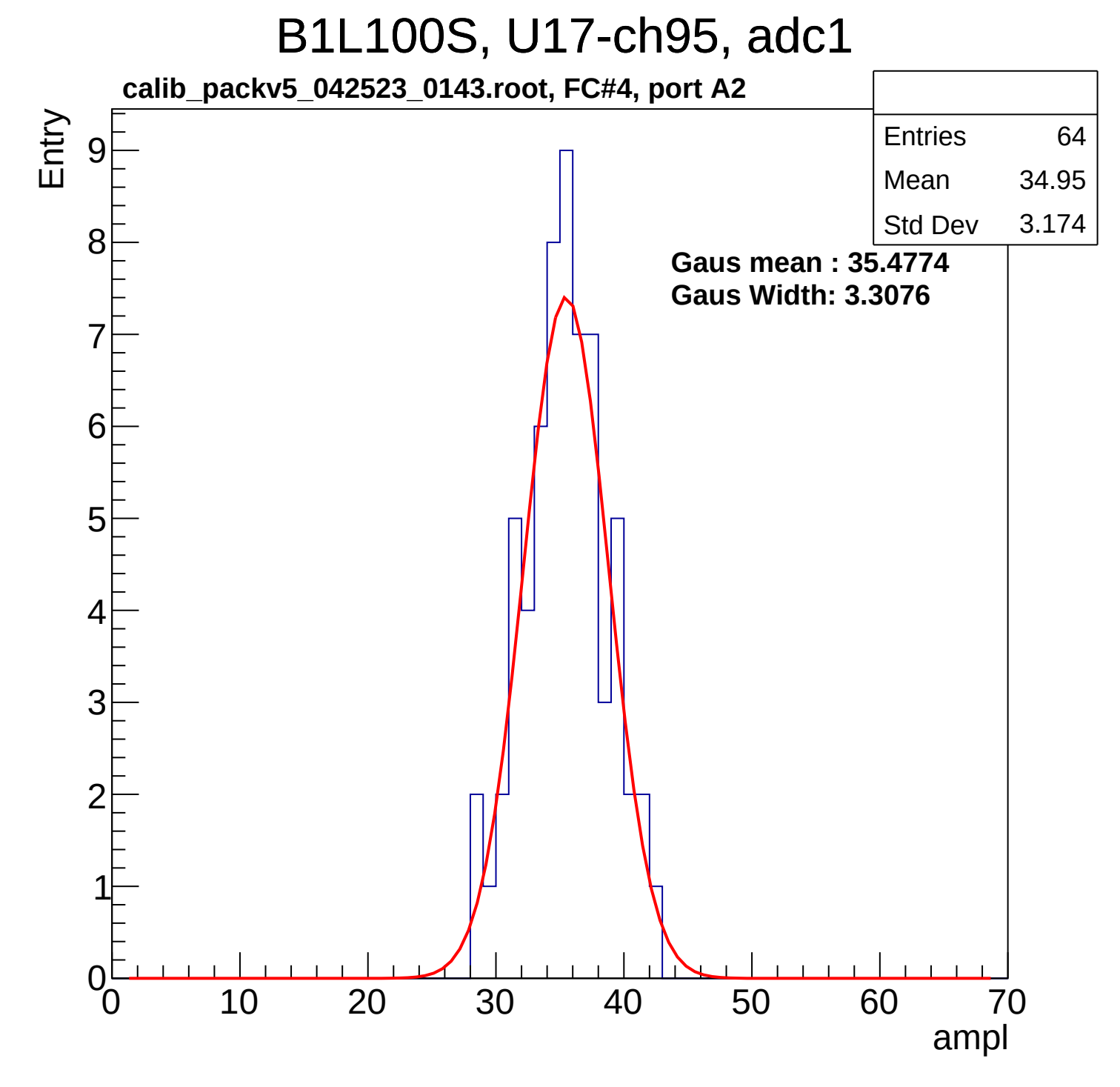
B1L100S, U17-ch95, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 34.95
Std Dev 3.174
Gaus mean : 35.4774
Gaus Width: 3.3076
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
30
40
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60
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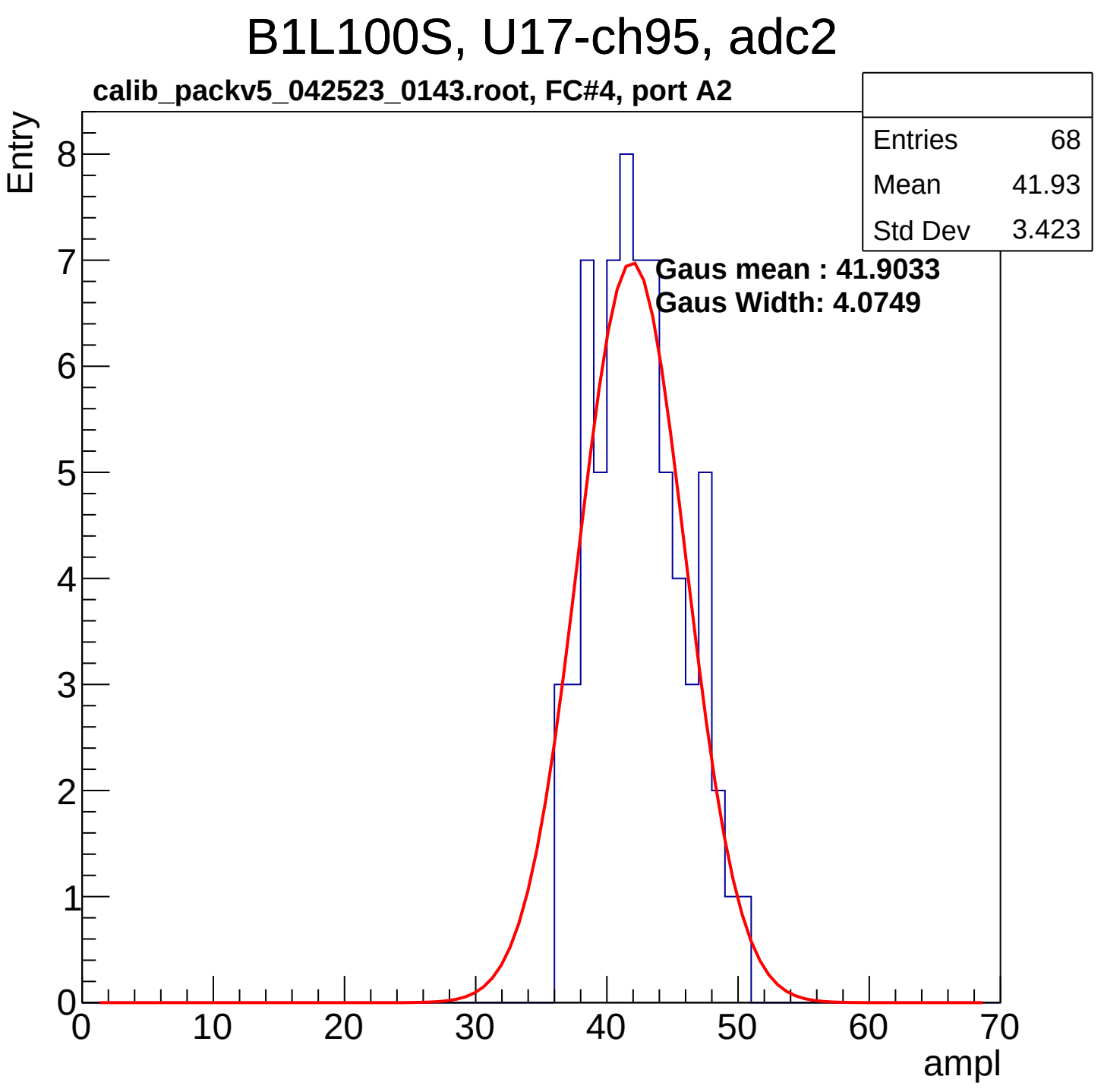
B1L100S, U17-ch95, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 41.93
Std Dev 3.423
Gaus mean : 41.9033
Gaus Width: 4.0749
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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40
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60
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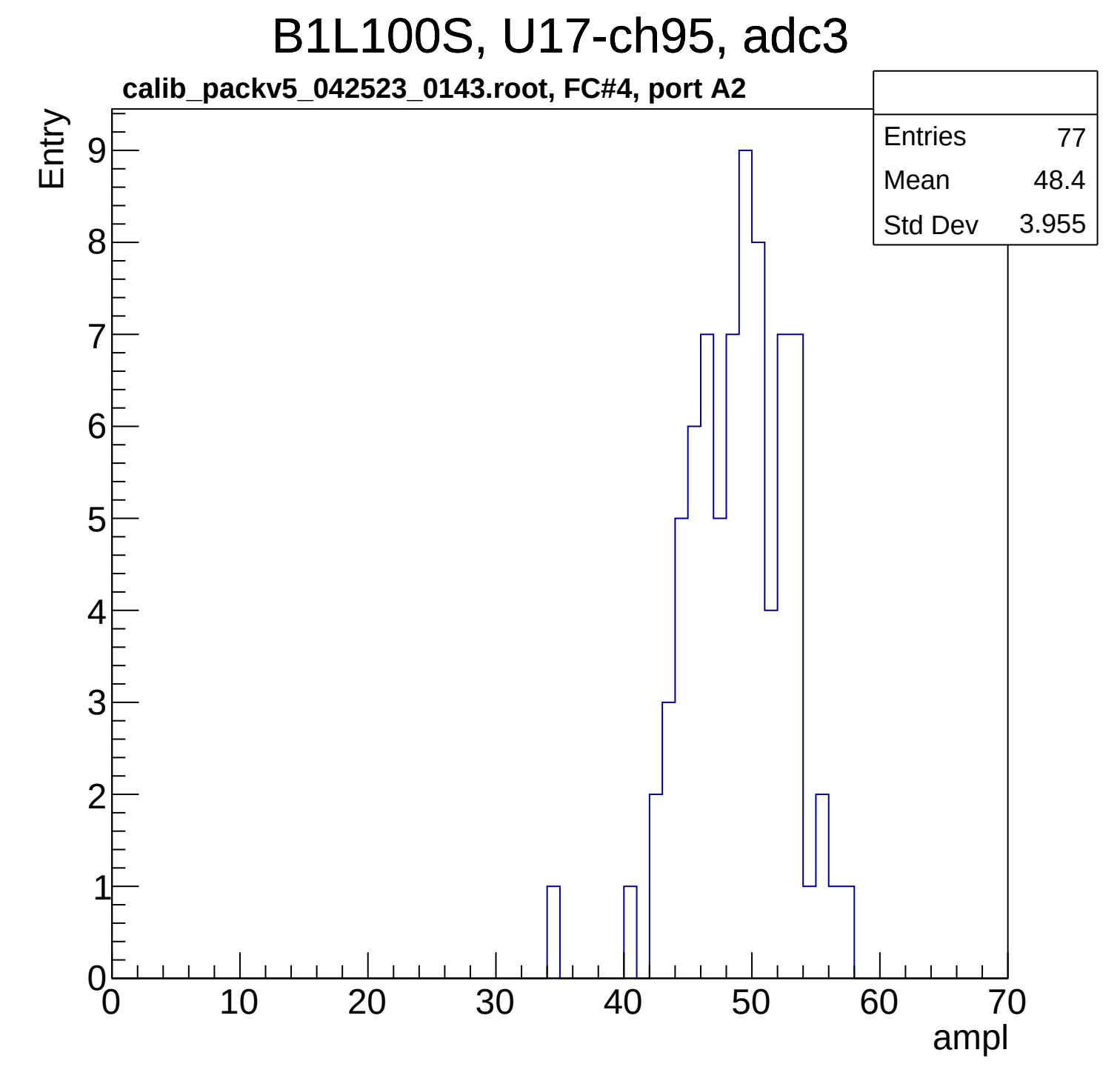
B1L100S, U17-ch95, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 77
Mean 48.4
Std Dev 3.955
Entry
ampl
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4
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6
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8
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0
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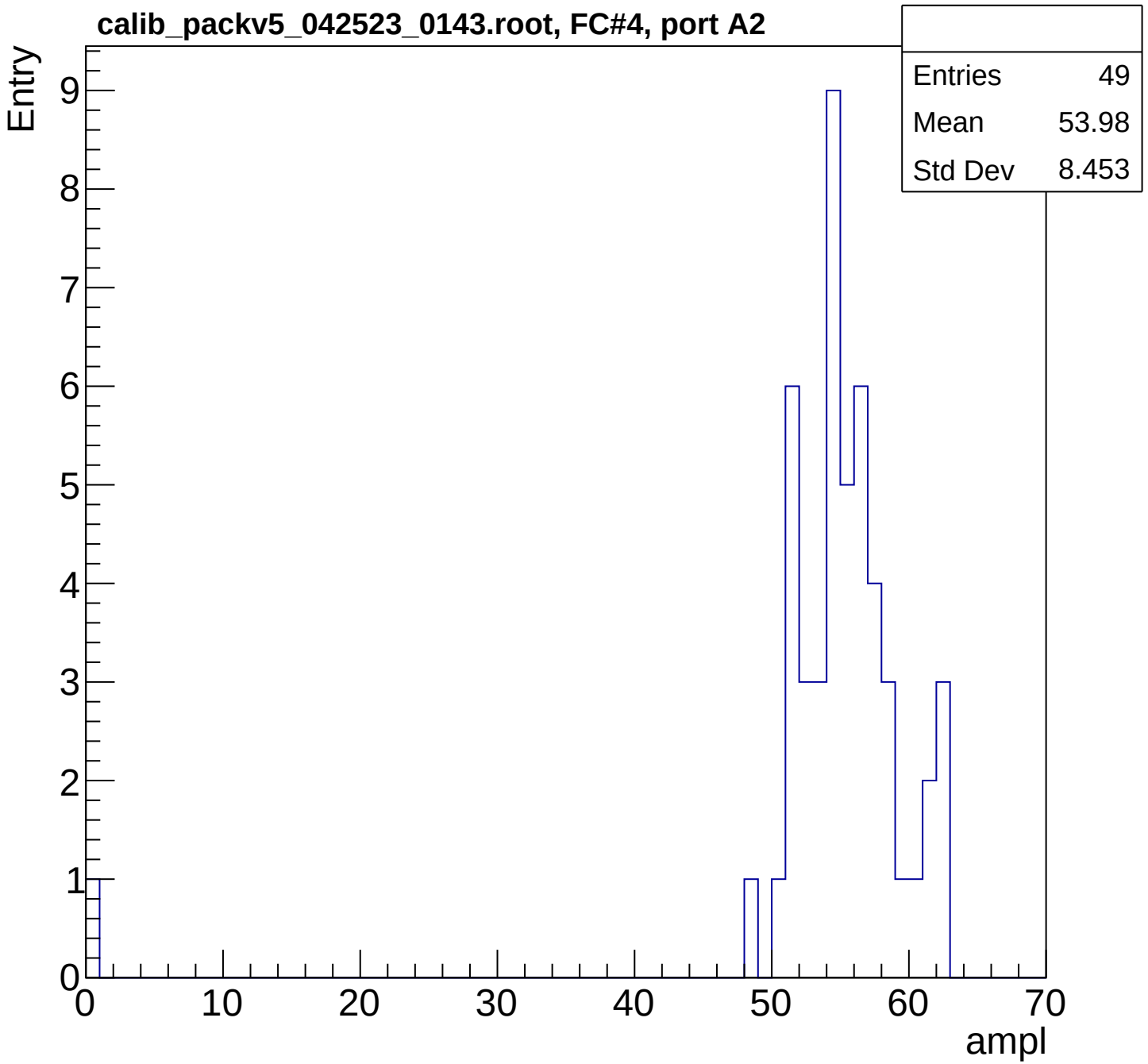
B1L100S, U17-ch95, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 49
Mean 53.98
Std Dev 8.453
Entry
ampl
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3
4
5
6
7
8
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0
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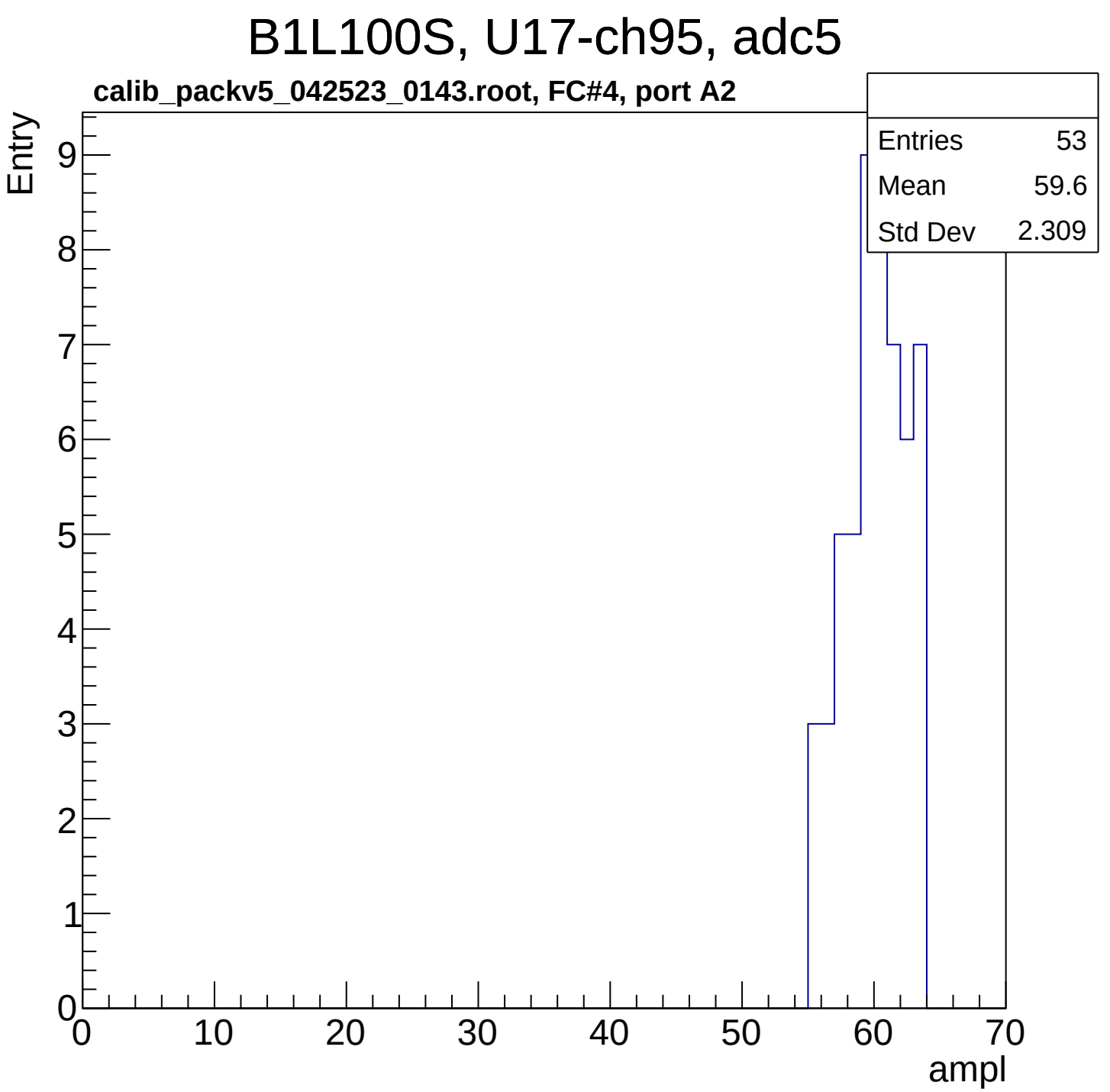
B1L100S, U17-ch95, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 59.6
Std Dev 2.309
Entry
ampl
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2
3
4
5
6
7
8
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0
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20
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60
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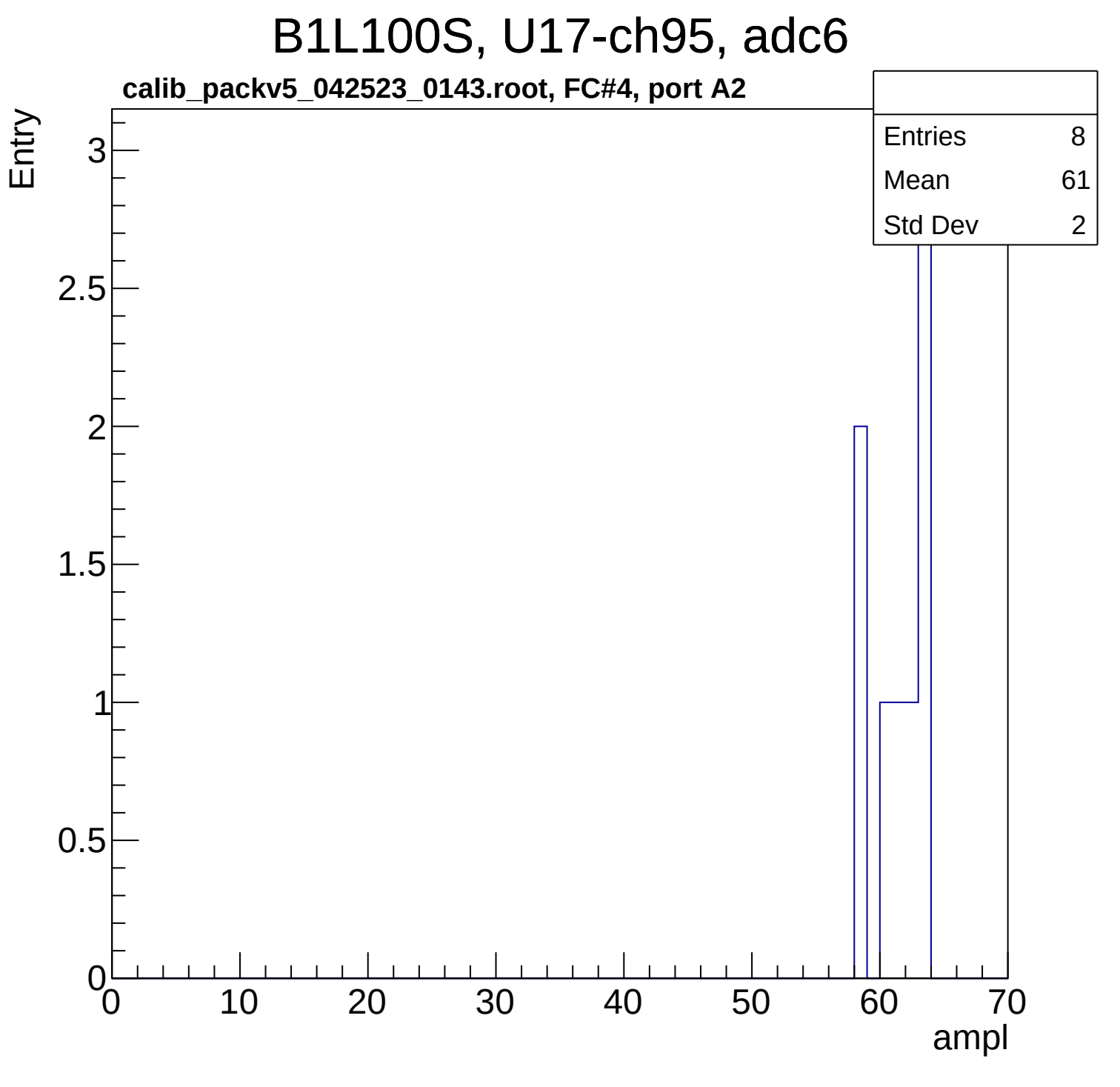
B1L100S, U17-ch95, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 8
Mean 61
Std Dev 2
Entry
ampl
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1
1.5
2
2.5
3
0
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20
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40
50
60
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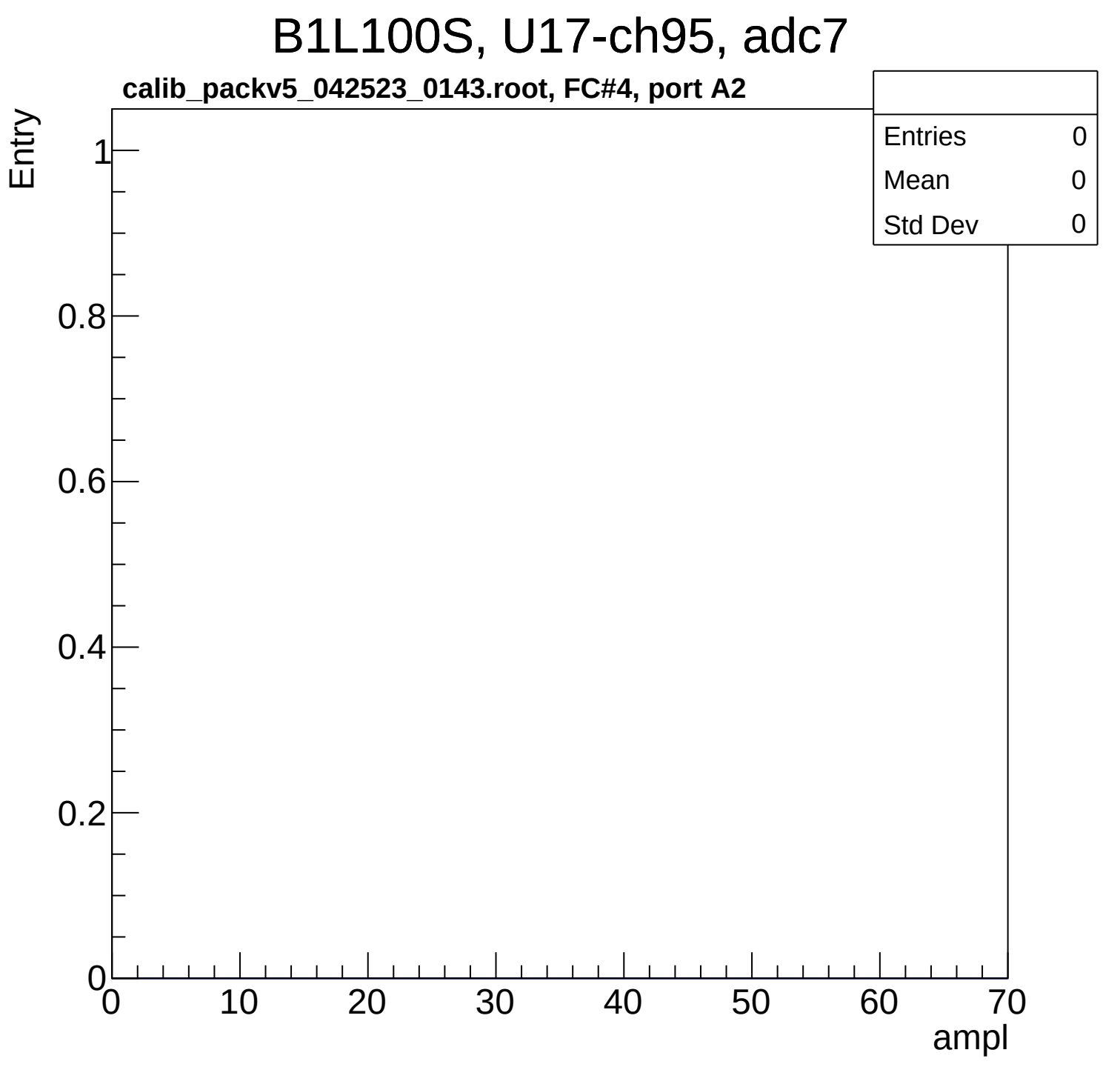
B1L100S, U17-ch95, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
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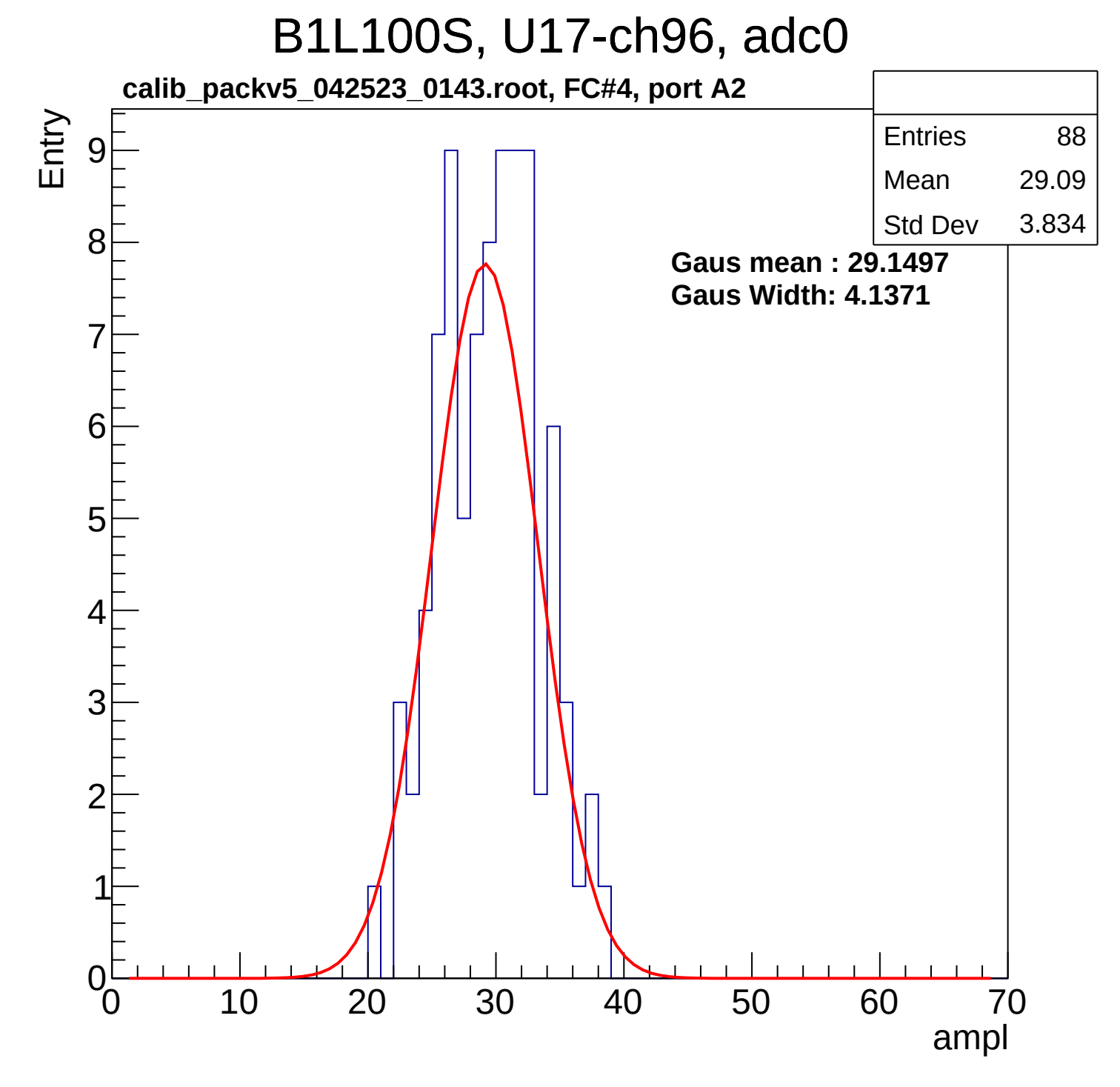
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch96, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 88
Mean 29.09
Std Dev 3.834
Gaus mean : 29.1497
Gaus Width: 4.1371
Entry
ampl
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2
3
4
5
6
7
8
9
0
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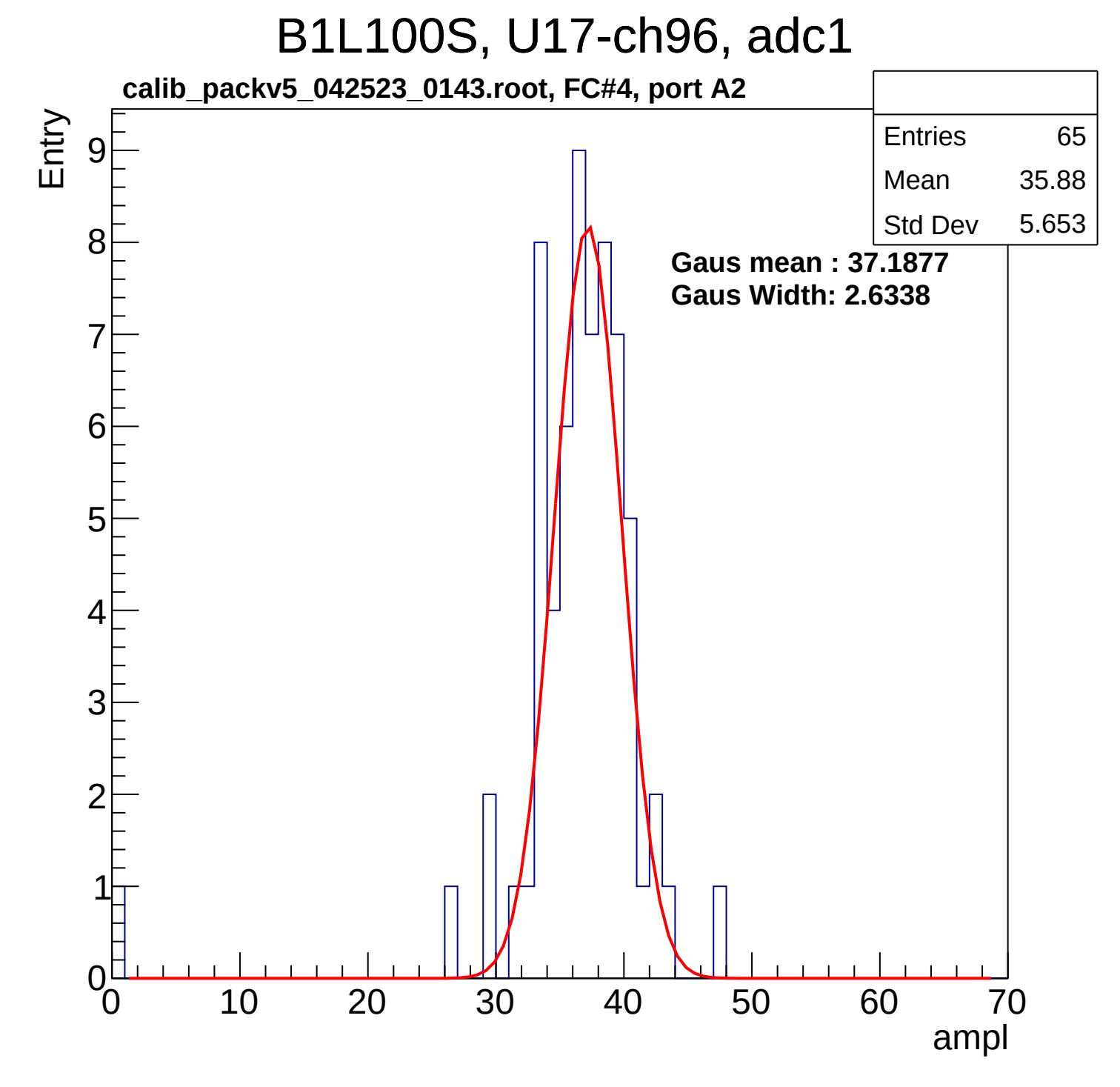
B1L100S, U17-ch96, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 35.88
Std Dev 5.653
Gaus mean : 37.1877
Gaus Width: 2.6338
Entry
ampl
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2
3
4
5
6
7
8
9
0
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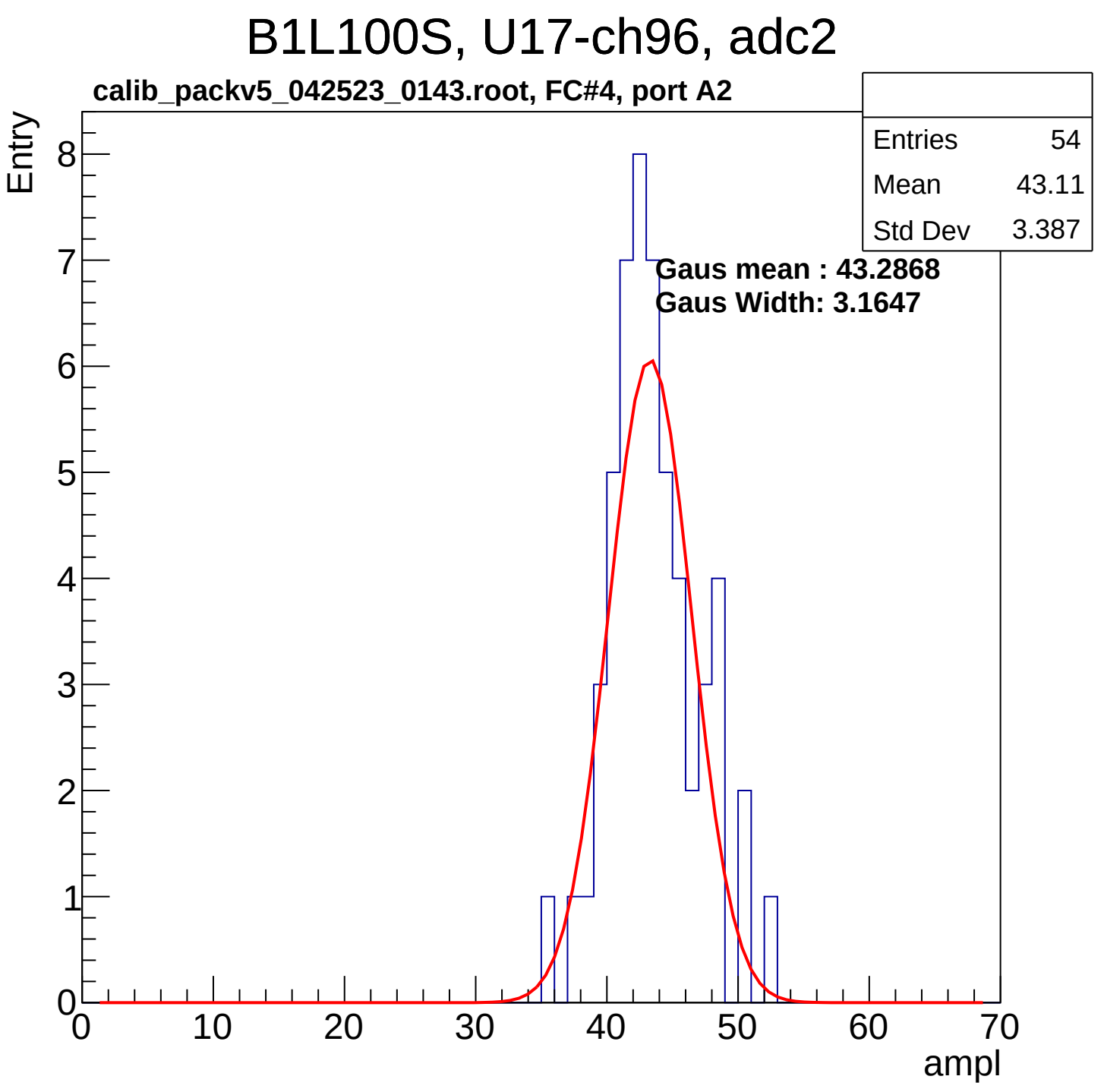
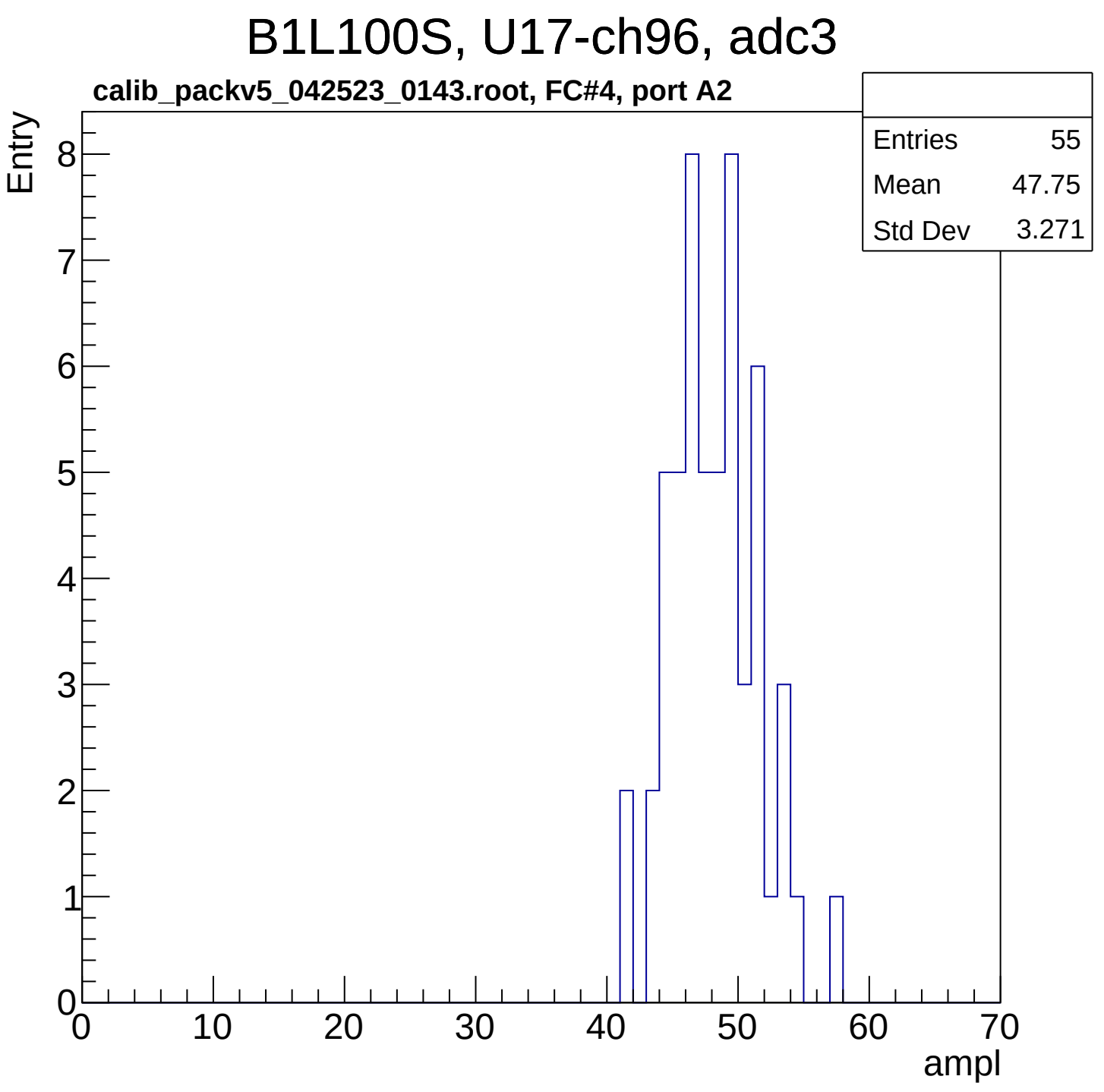

B1L100S, U17-ch96, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 43.11
Std Dev 3.387
Gaus mean : 43.2868
Gaus Width: 3.1647
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch96, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 47.75
Std Dev 3.271
Entry
ampl
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1
2
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4
5
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7
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0
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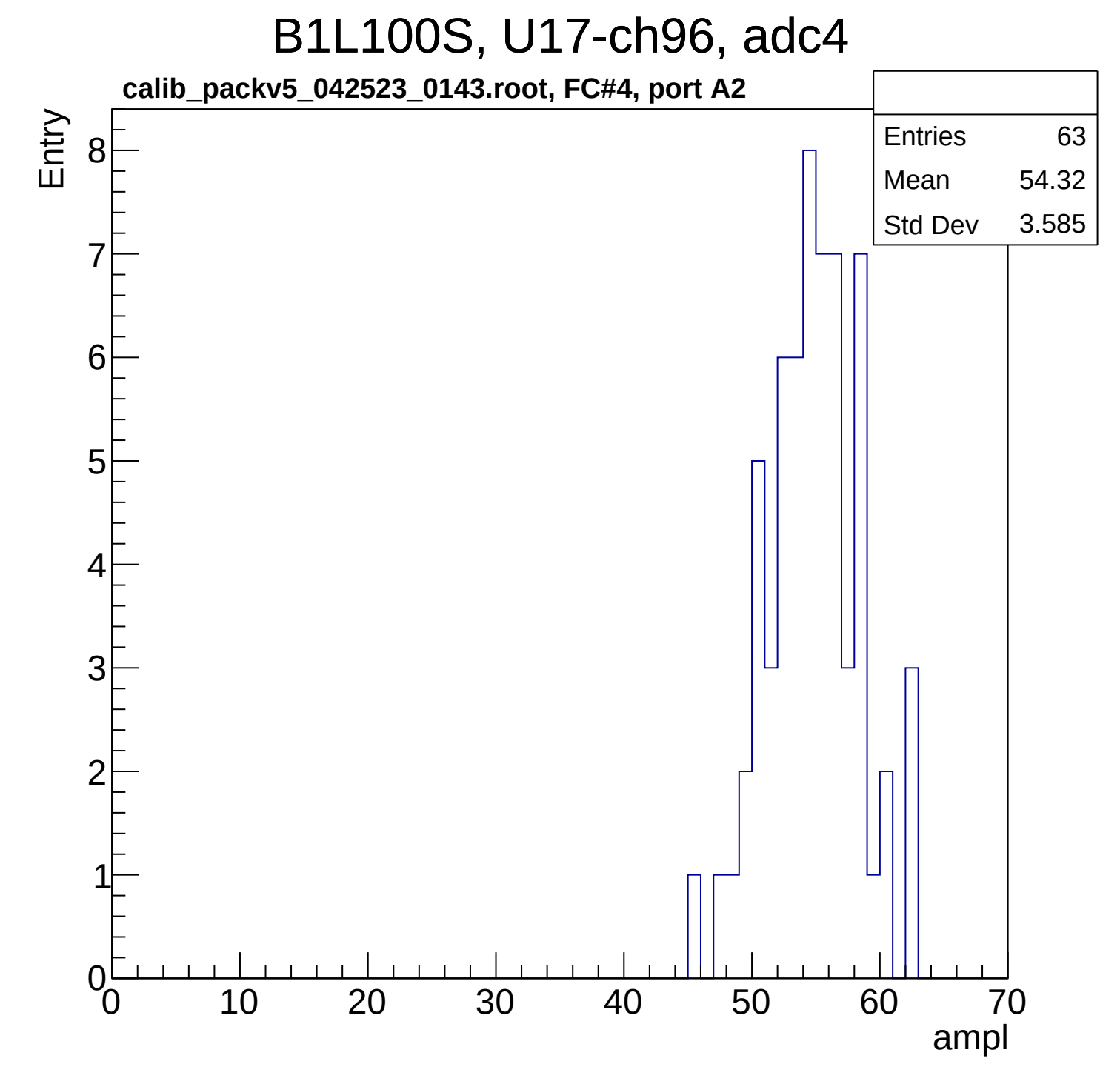
B1L100S, U17-ch96, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 54.32
Std Dev 3.585
Entry
ampl
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1
2
3
4
5
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7
8
0
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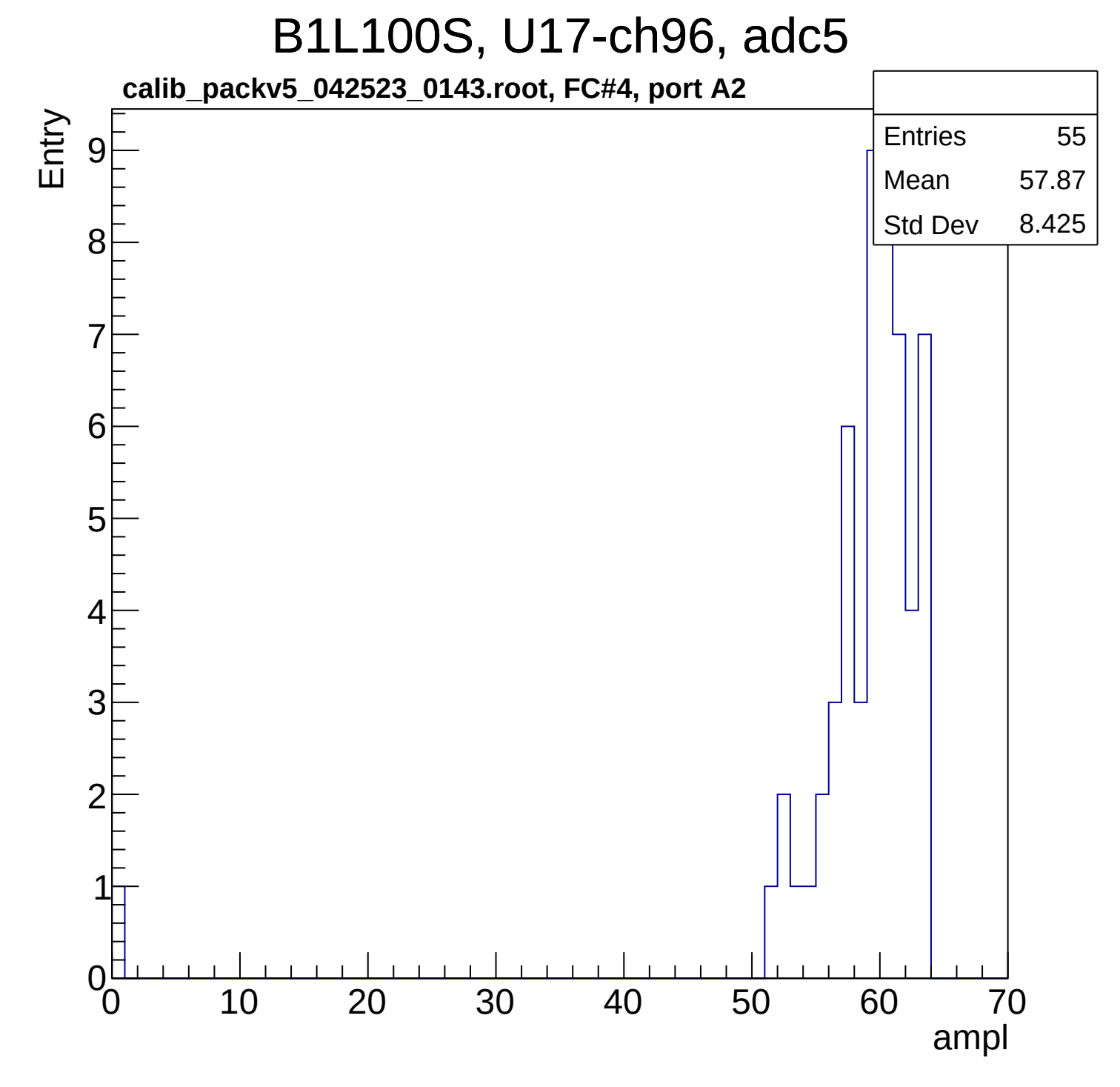
B1L100S, U17-ch96, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 57.87
Std Dev 8.425
Entry
ampl
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3
4
5
6
7
8
9
0
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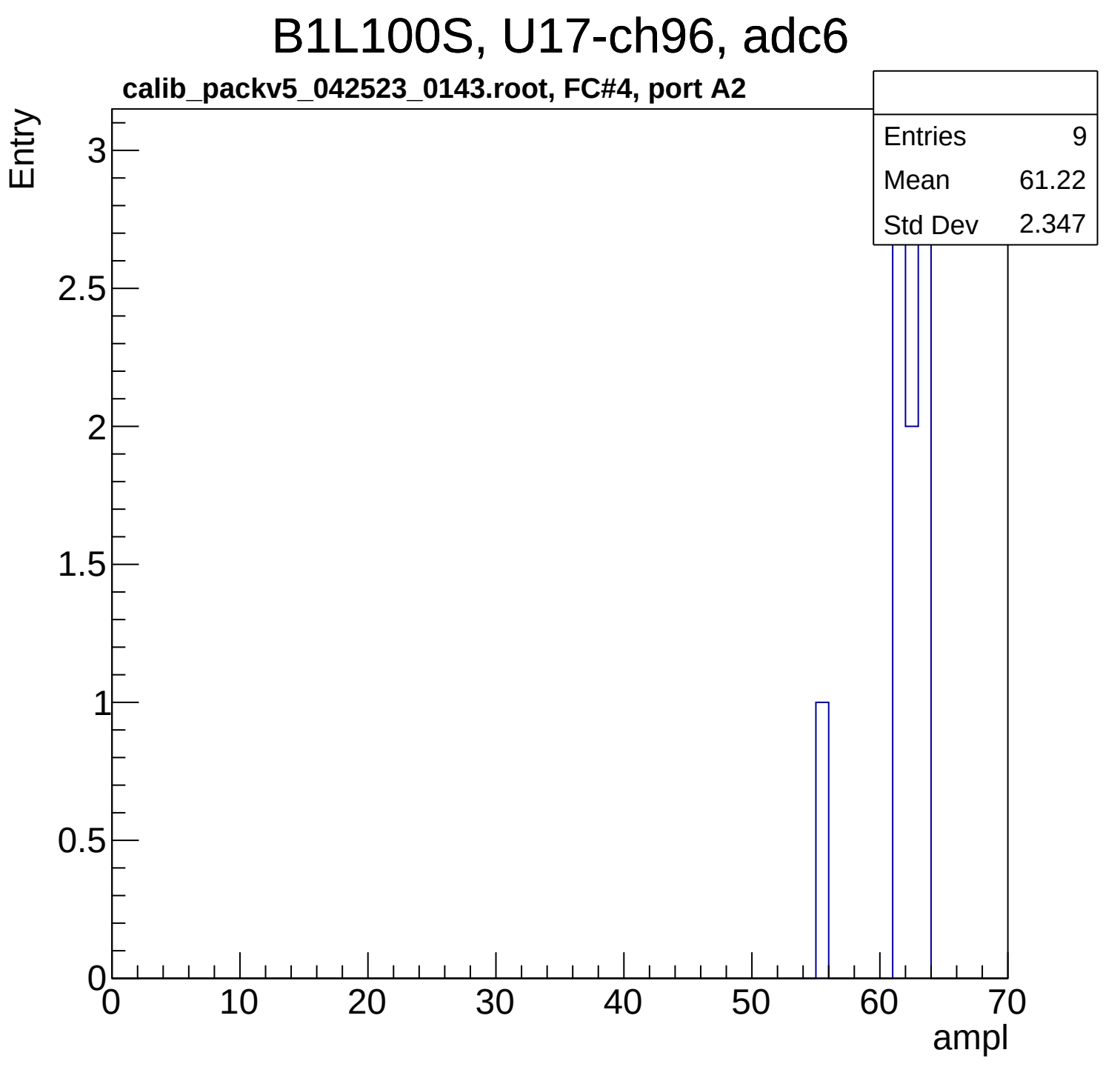
B1L100S, U17-ch96, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 9
Mean 61.22
Std Dev 2.347
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
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40
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60
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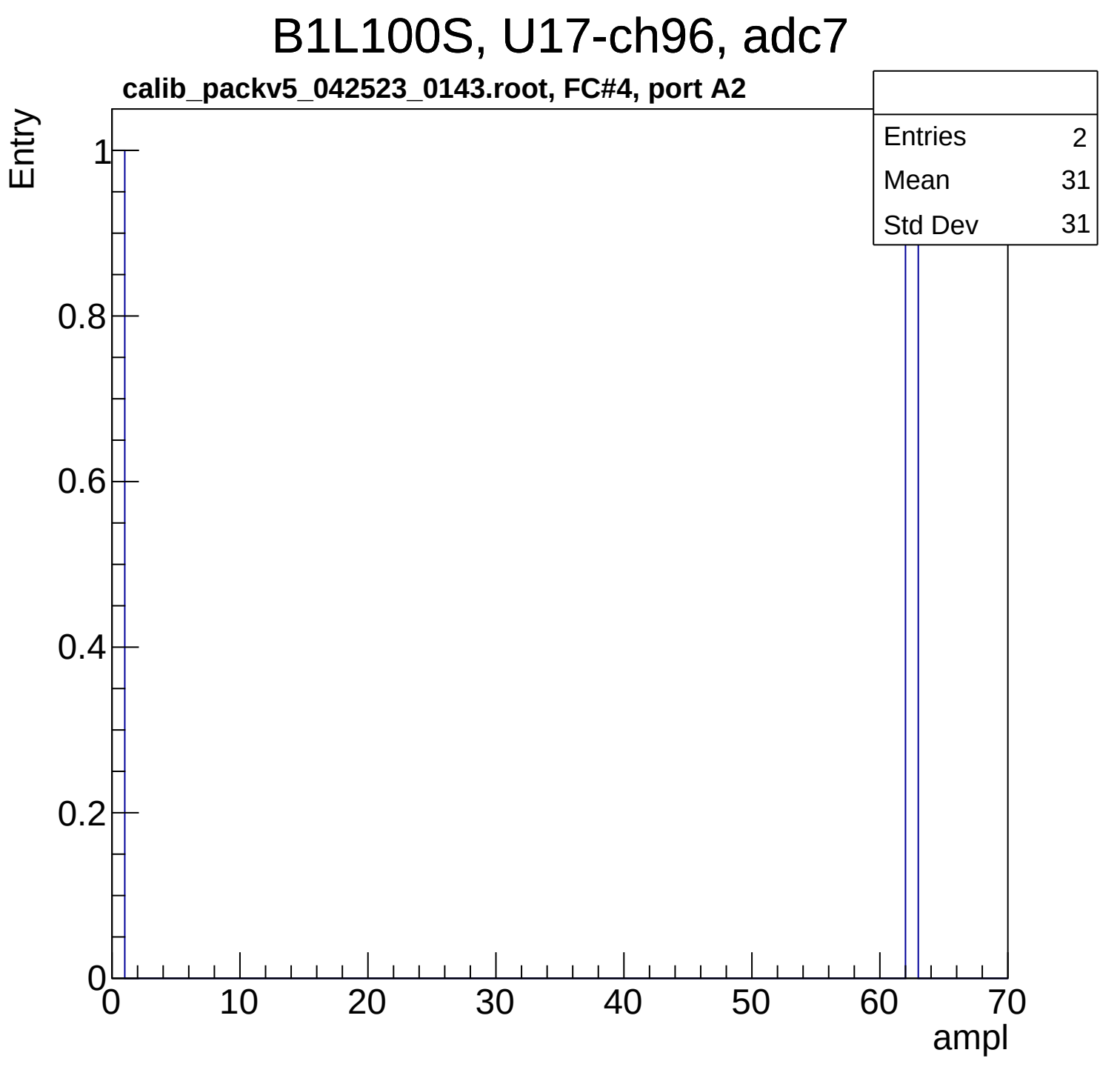
B1L100S, U17-ch96, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 31
Std Dev 31
Entry
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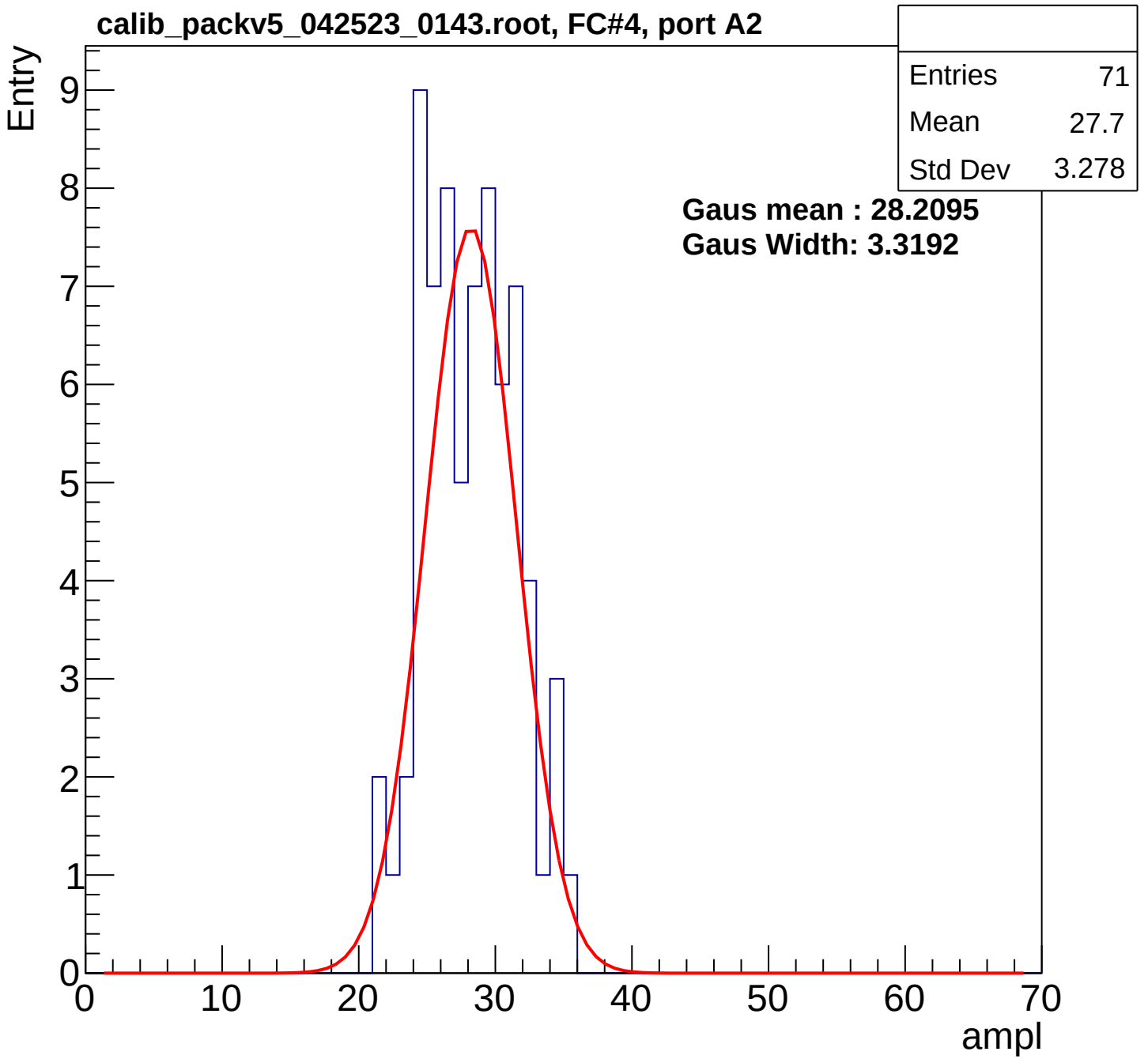
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch97, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 27.7
Std Dev 3.278
Gaus mean : 28.2095
Gaus Width: 3.3192
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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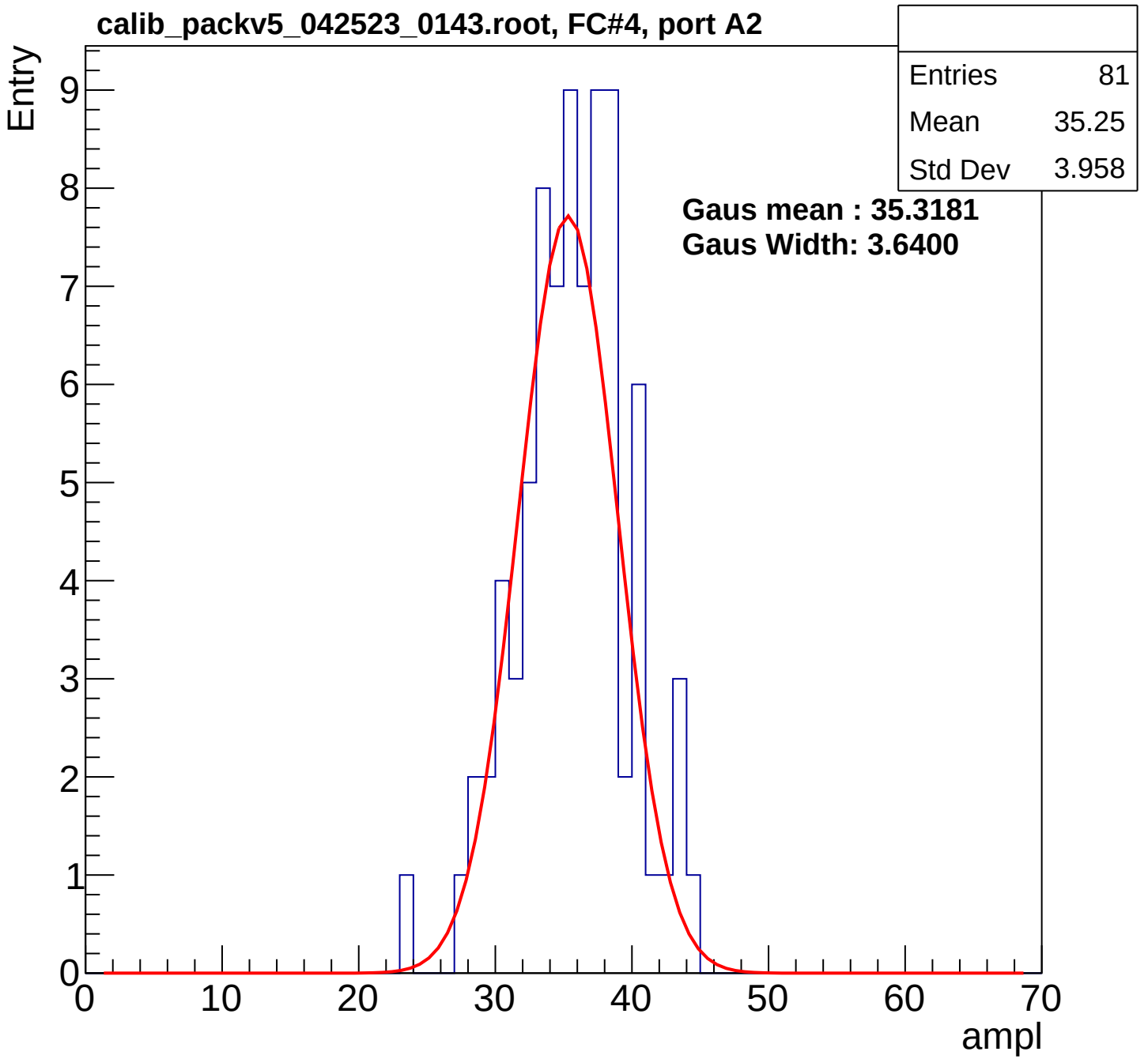
B1L100S, U17-ch97, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 81
Mean 35.25
Std Dev 3.958
Gaus mean : 35.3181
Gaus Width: 3.6400
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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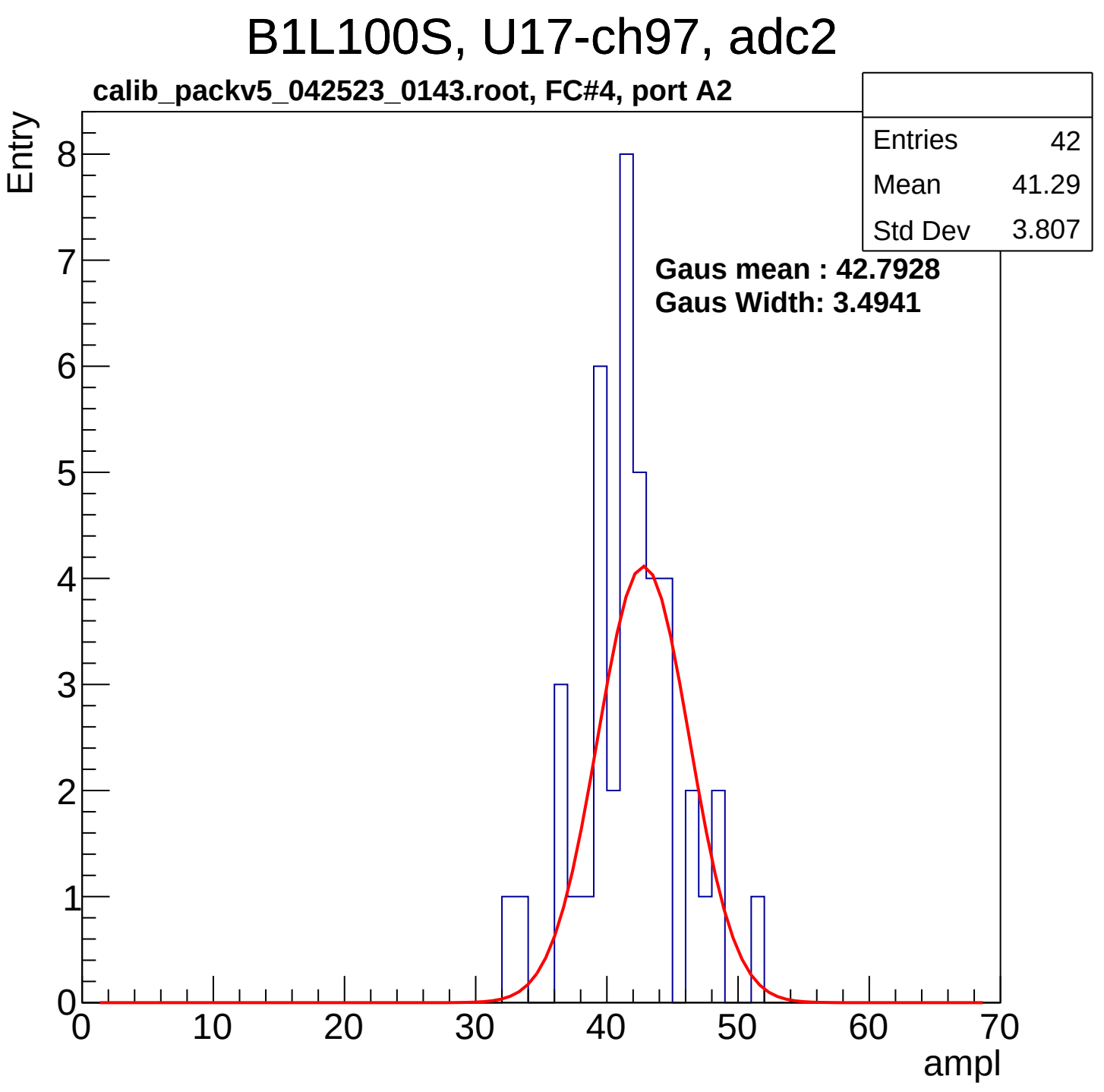
B1L100S, U17-ch97, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 42
Mean 41.29
Std Dev 3.807
Gaus mean : 42.7928
Gaus Width: 3.4941
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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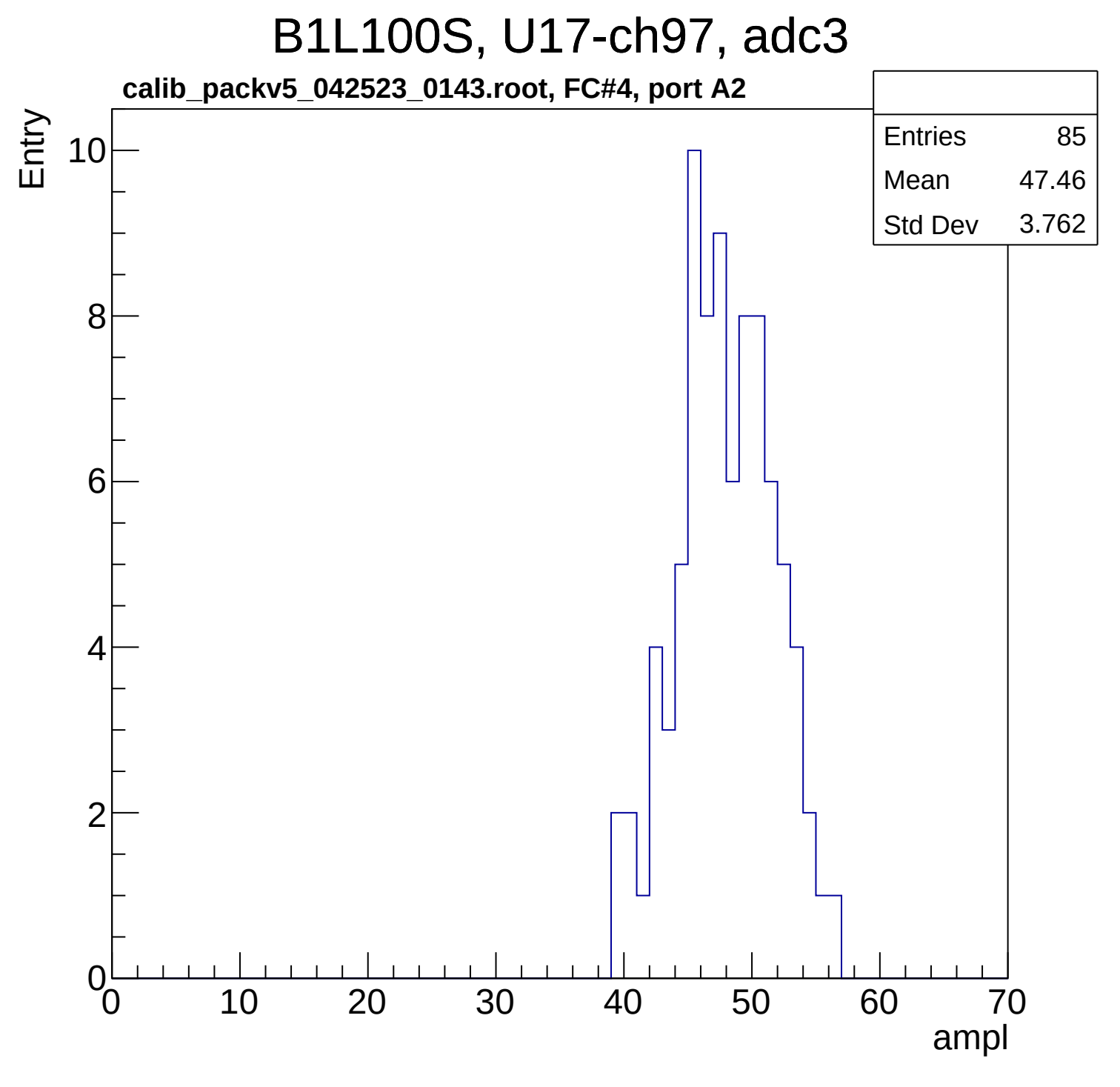
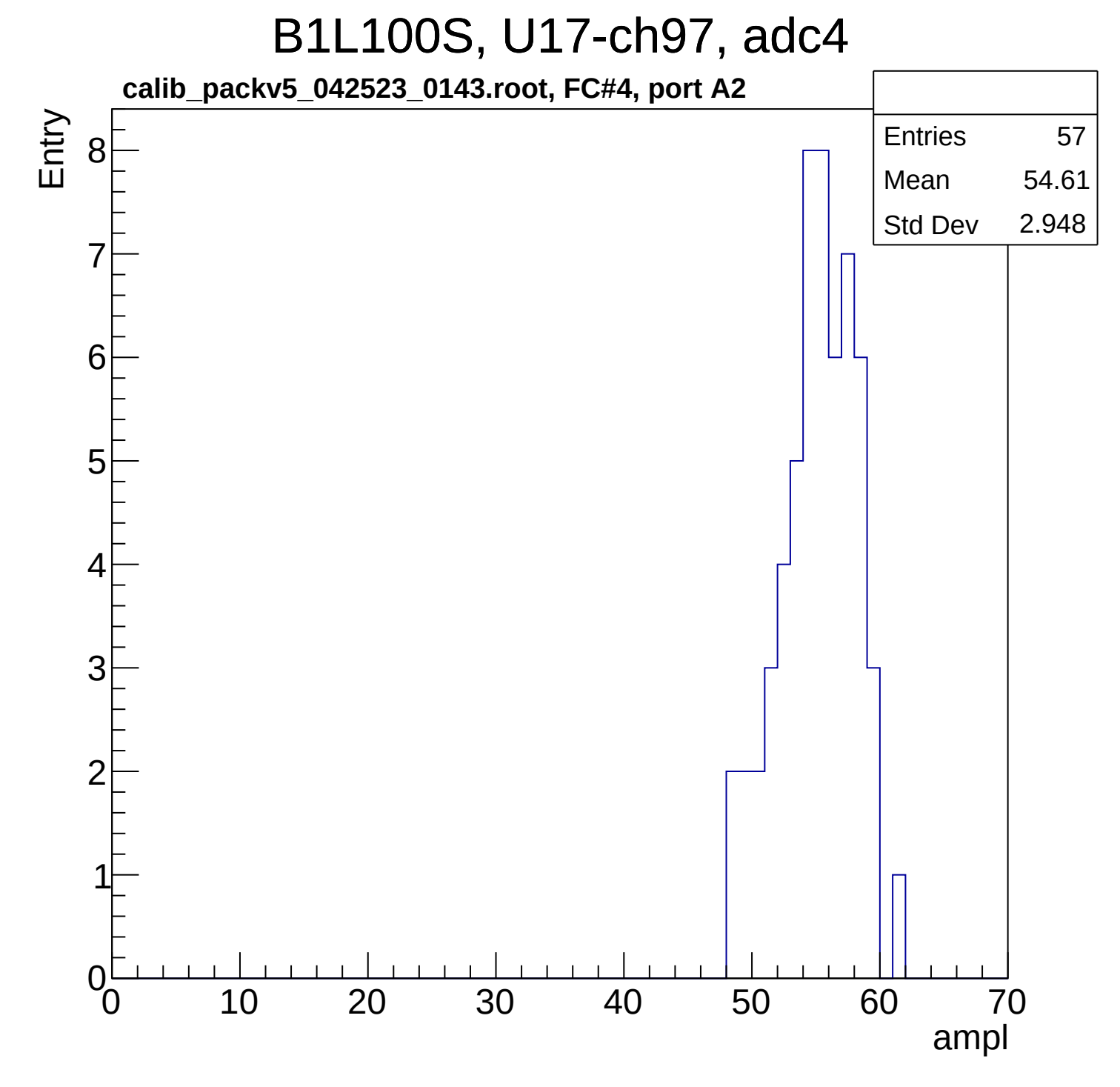
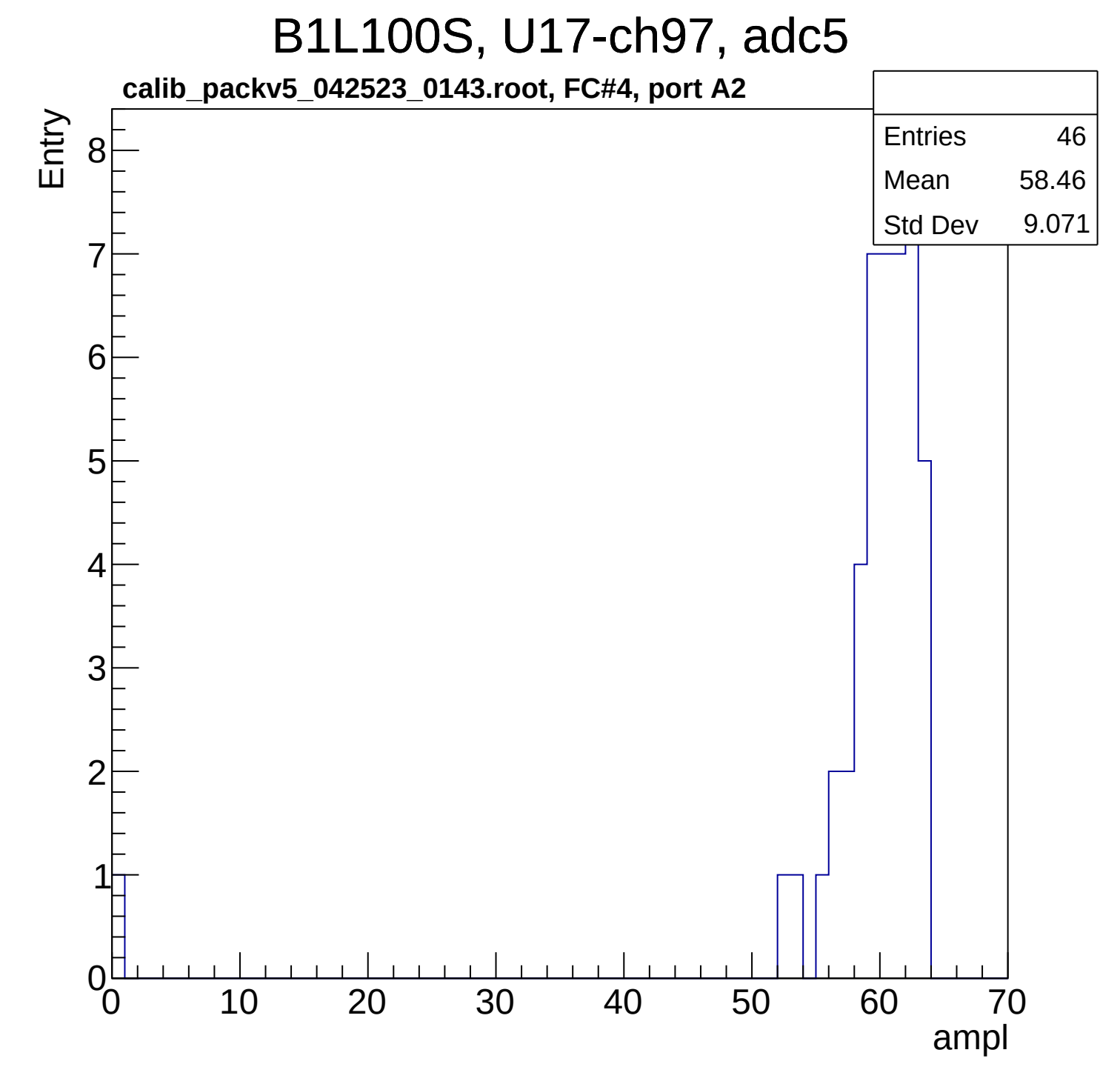

B1L100S, U17-ch97, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 85
Mean 47.46
Std Dev 3.762
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U17-ch97, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 54.61
Std Dev 2.948
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch97, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 46
Mean 58.46
Std Dev 9.071
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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20
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60
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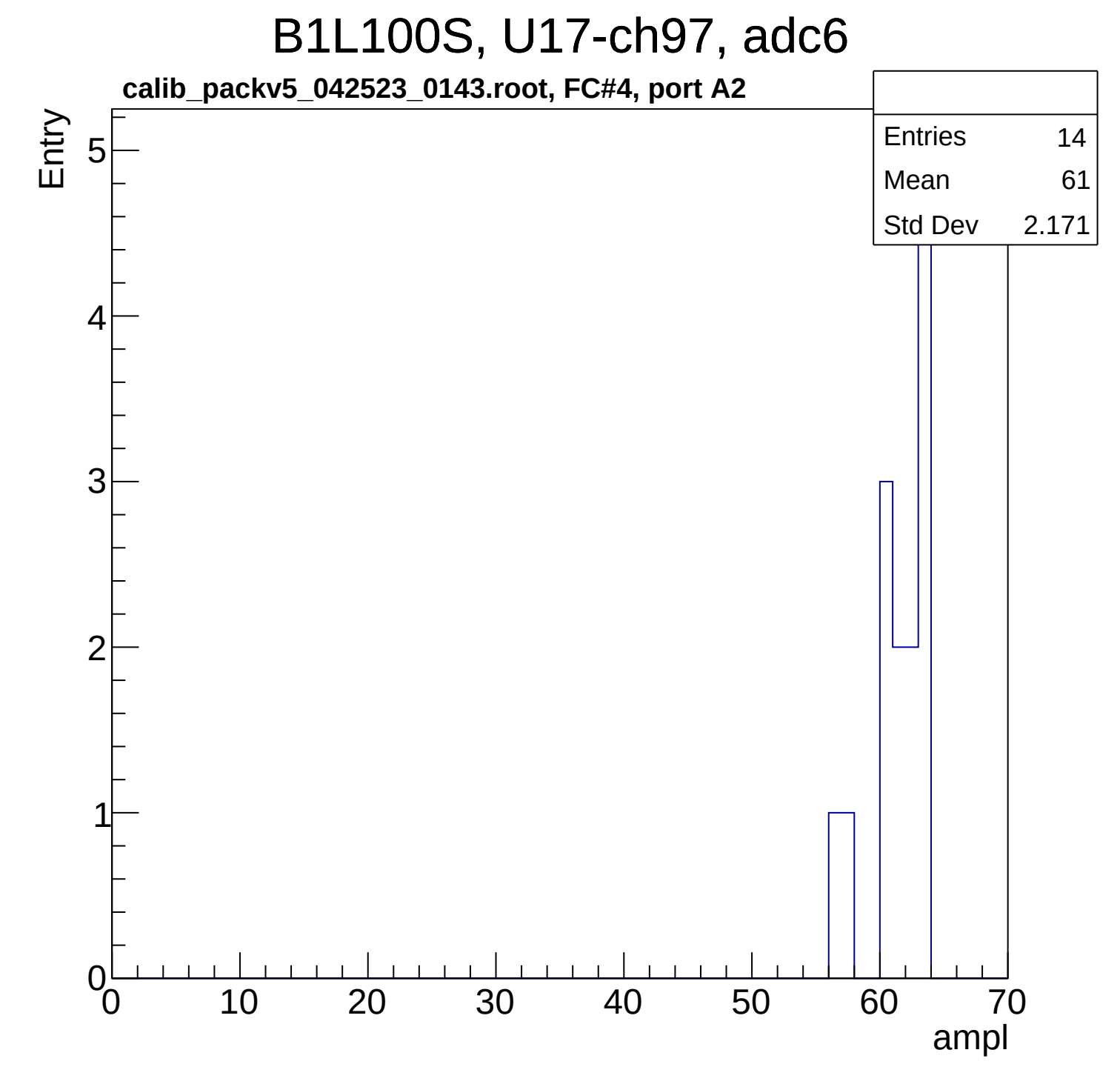
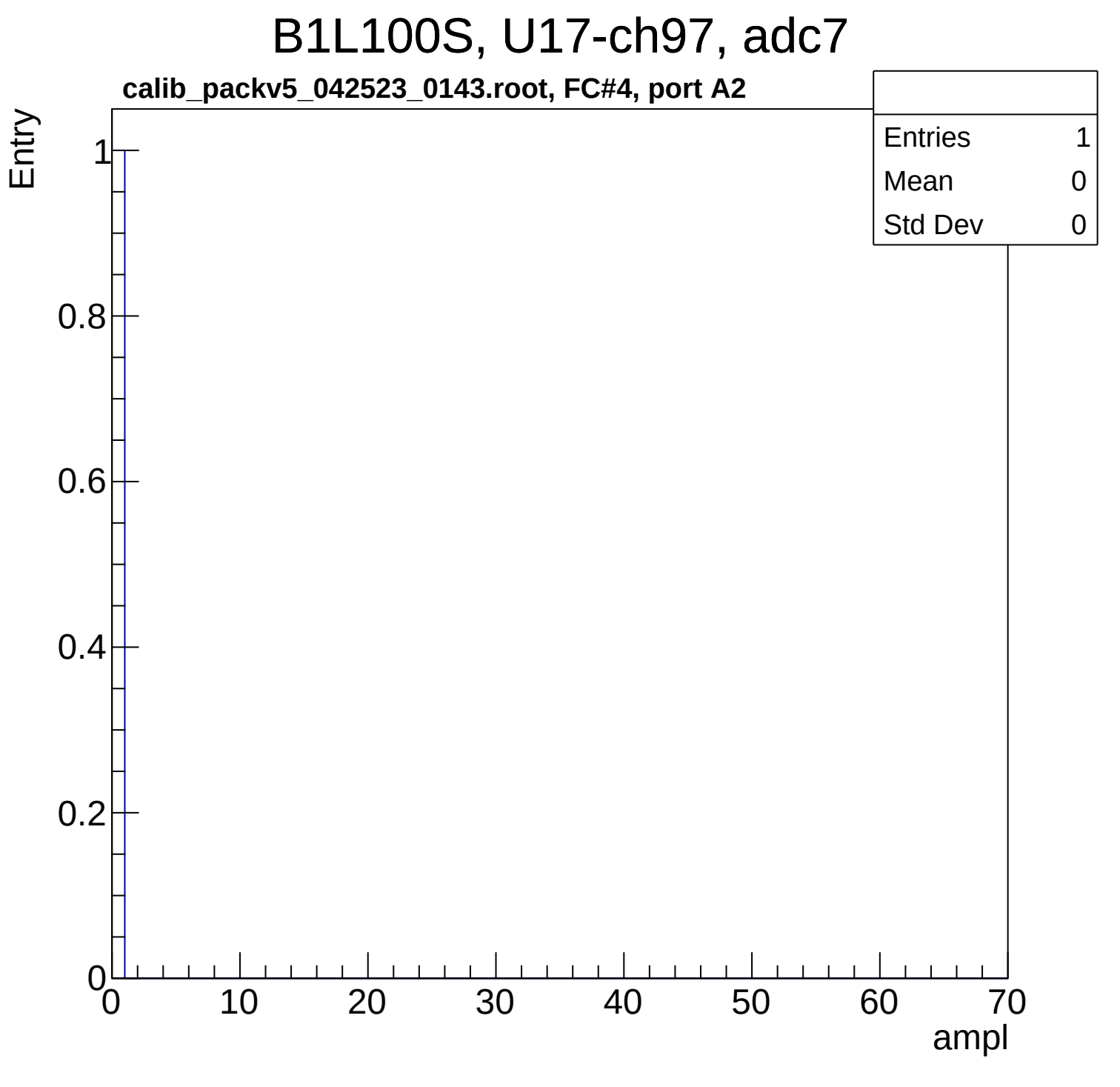
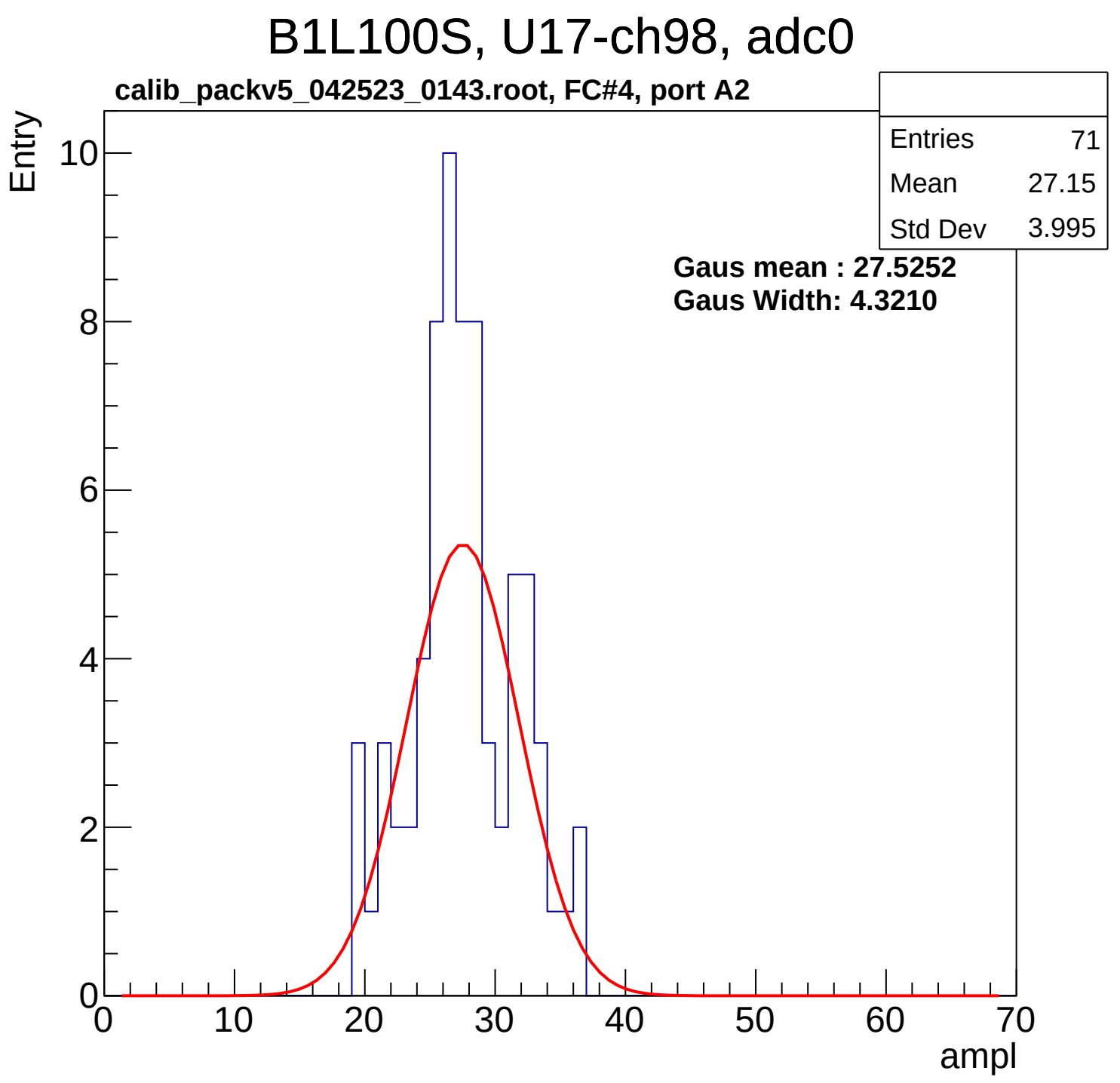
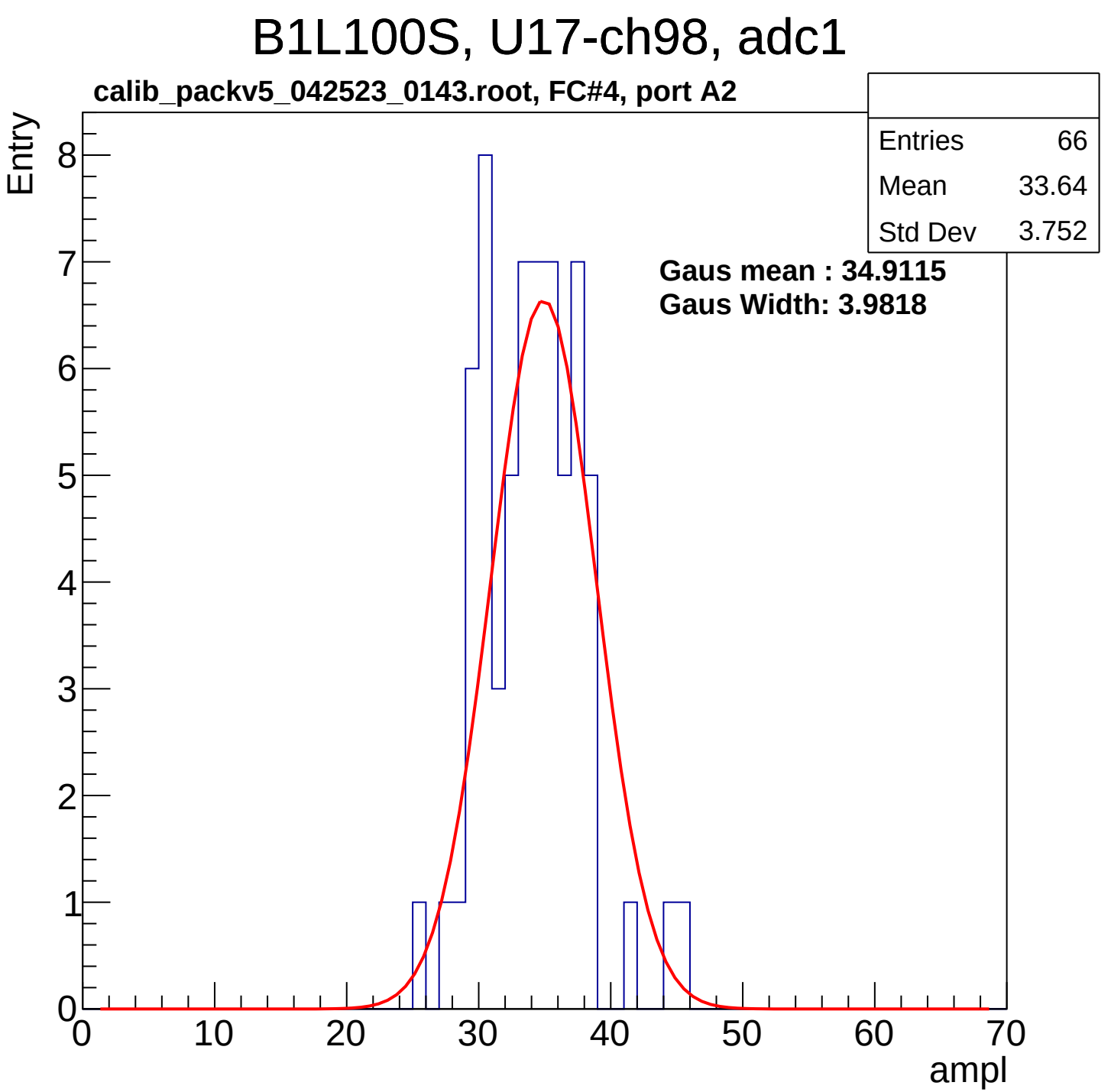

B1L100S, U17-ch97, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 14
Mean 61
Std Dev 2.171
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L100S, U17-ch97, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch98, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 27.15
Std Dev 3.995
Gaus mean : 27.5252
Gaus Width: 4.3210
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U17-ch98, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 33.64
Std Dev 3.752
Gaus mean : 34.9115
Gaus Width: 3.9818
Entry
ampl
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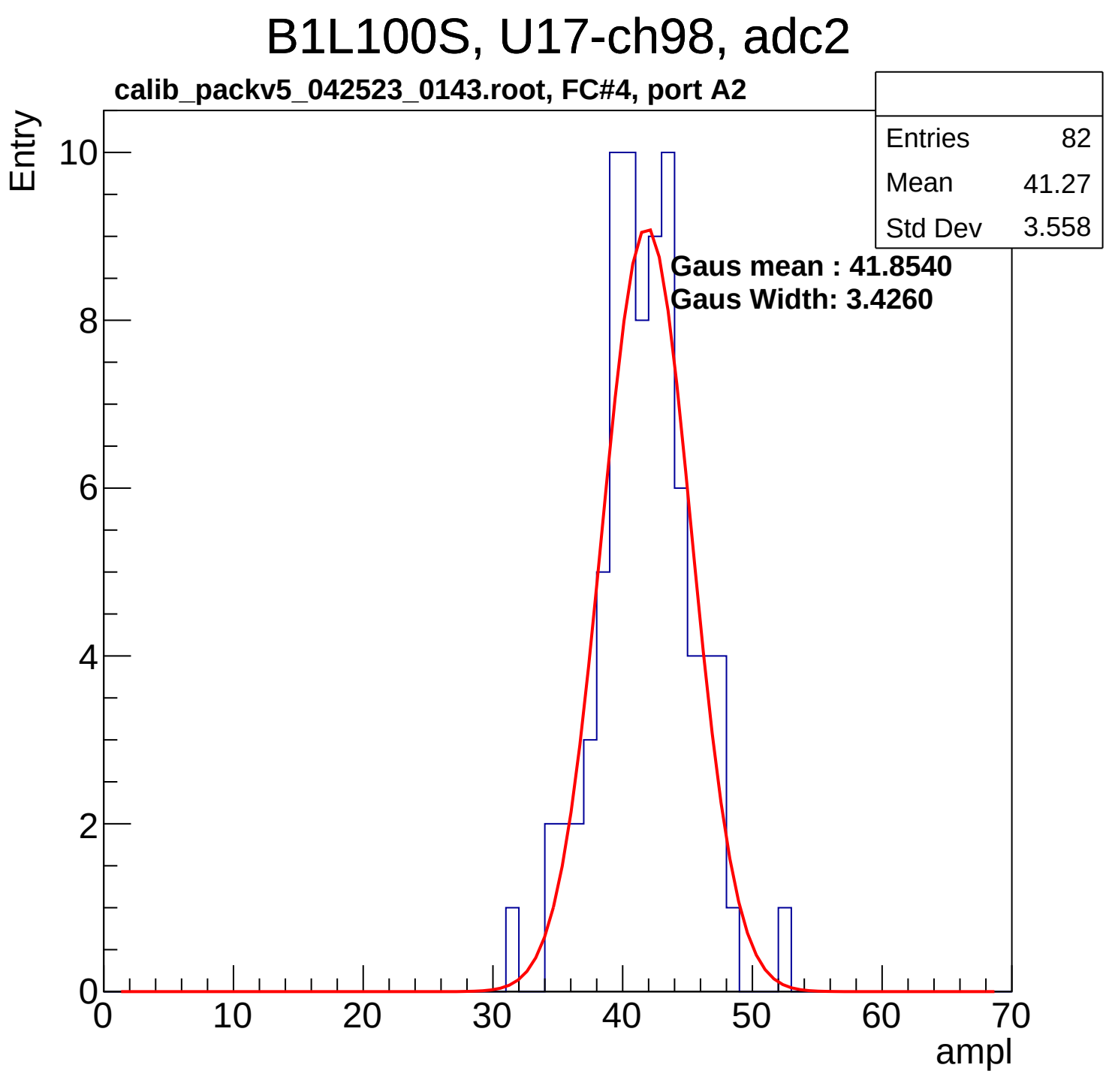
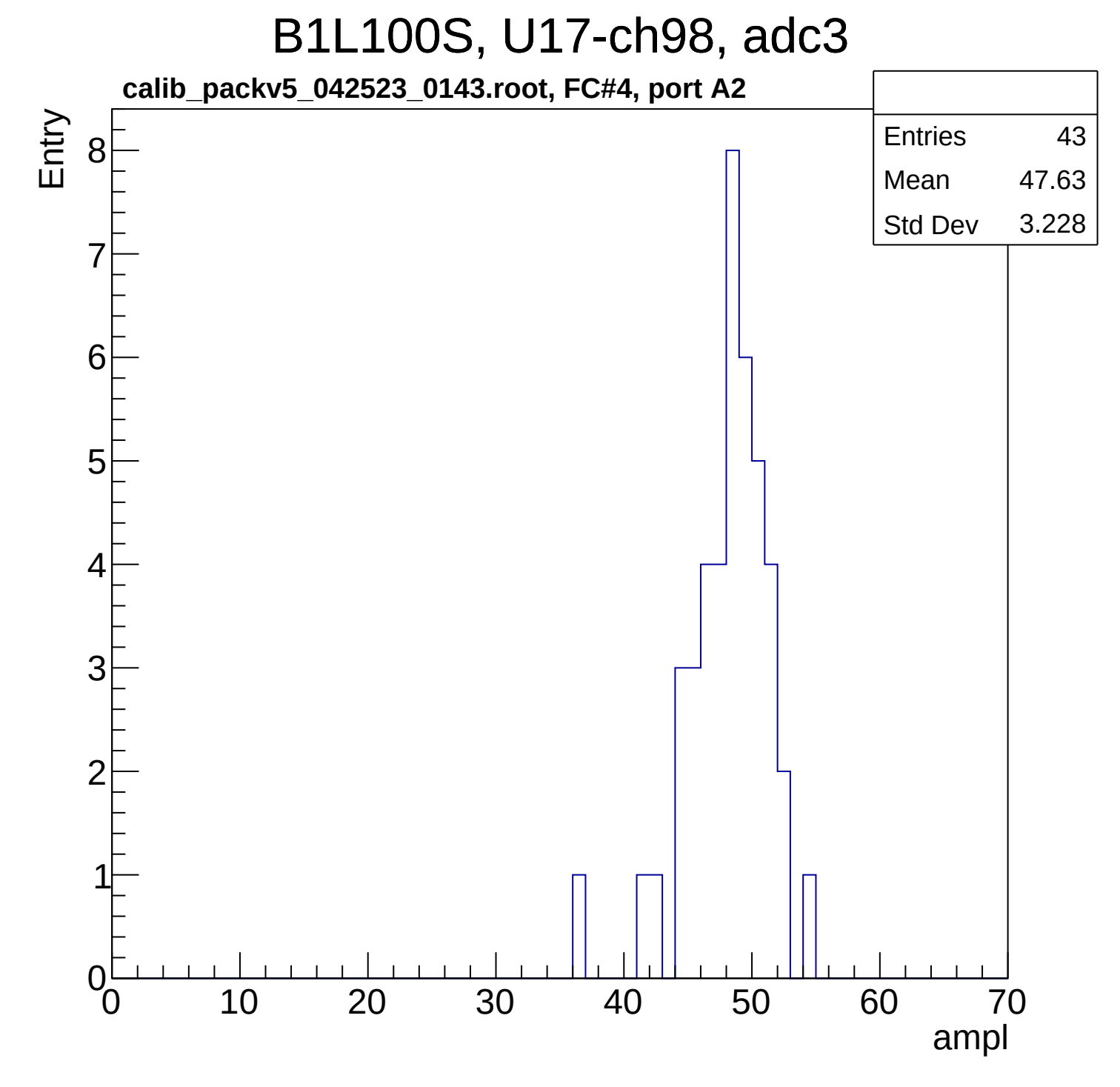
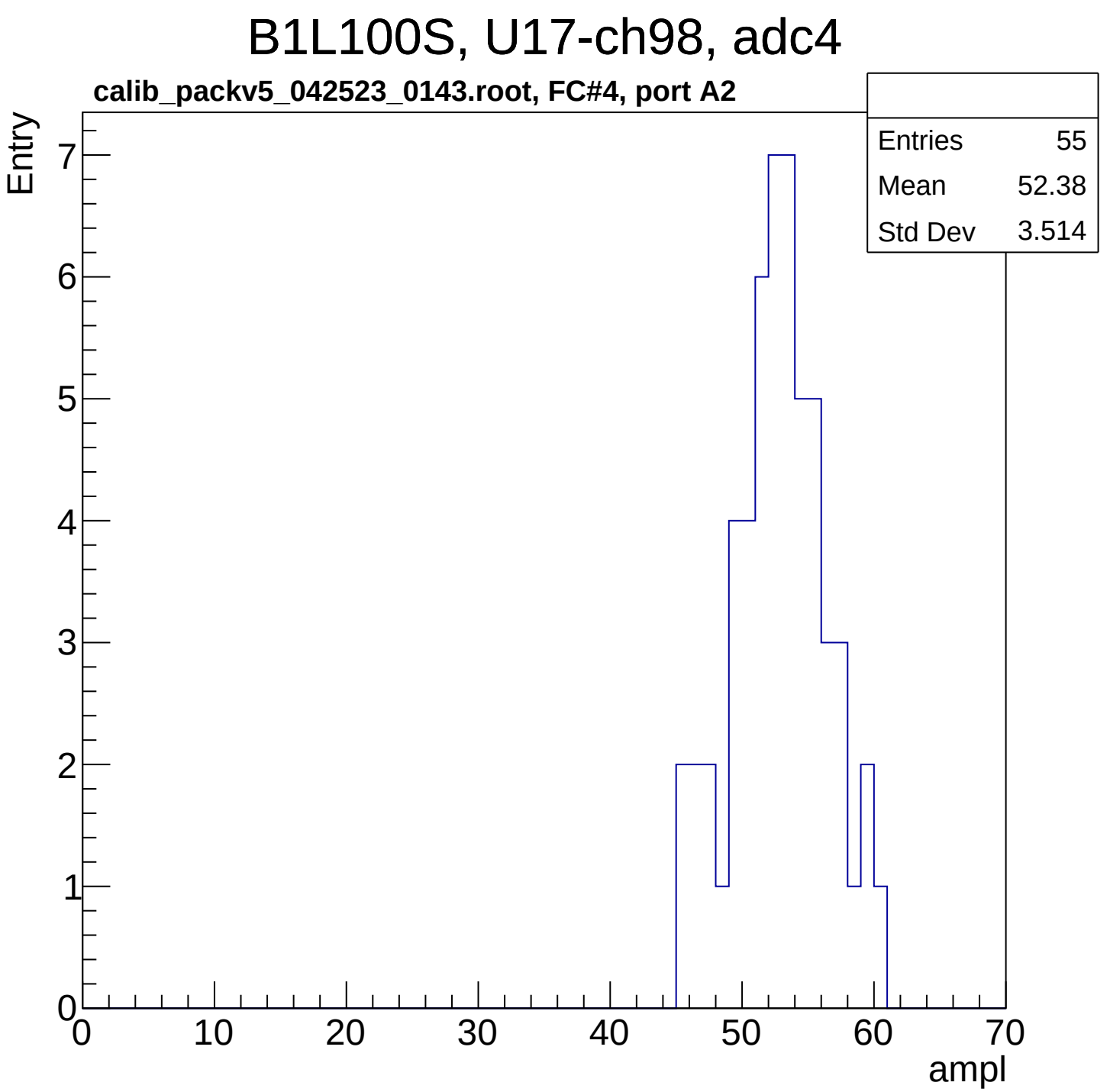
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch98, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 82
Mean 41.27
Std Dev 3.558
Gaus mean : 41.8540
Gaus Width: 3.4260
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U17-ch98, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 43
Mean 47.63
Std Dev 3.228
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch98, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 52.38
Std Dev 3.514
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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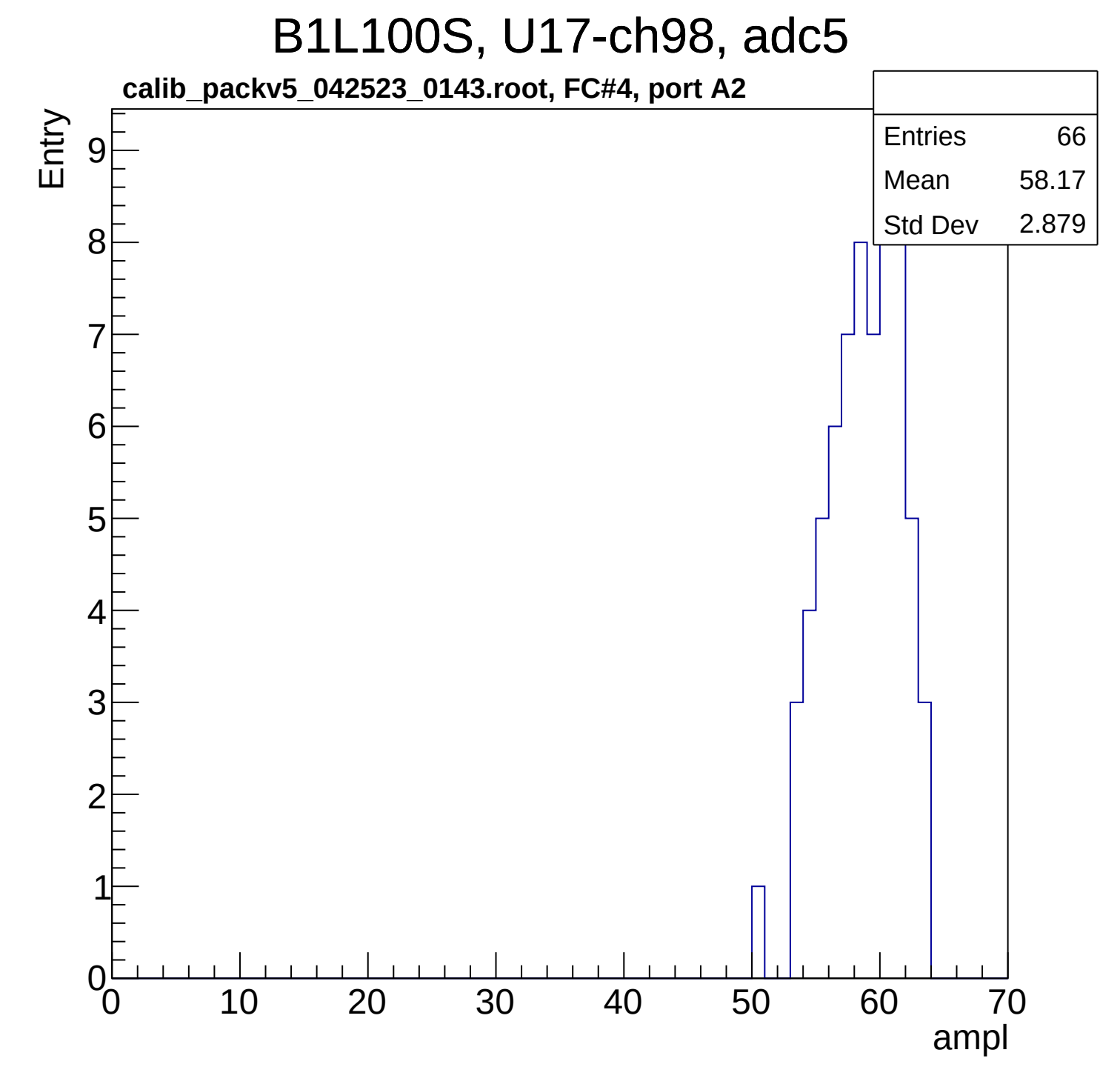
B1L100S, U17-ch98, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 58.17
Std Dev 2.879
Entry
ampl
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3
4
5
6
7
8
9
0
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60
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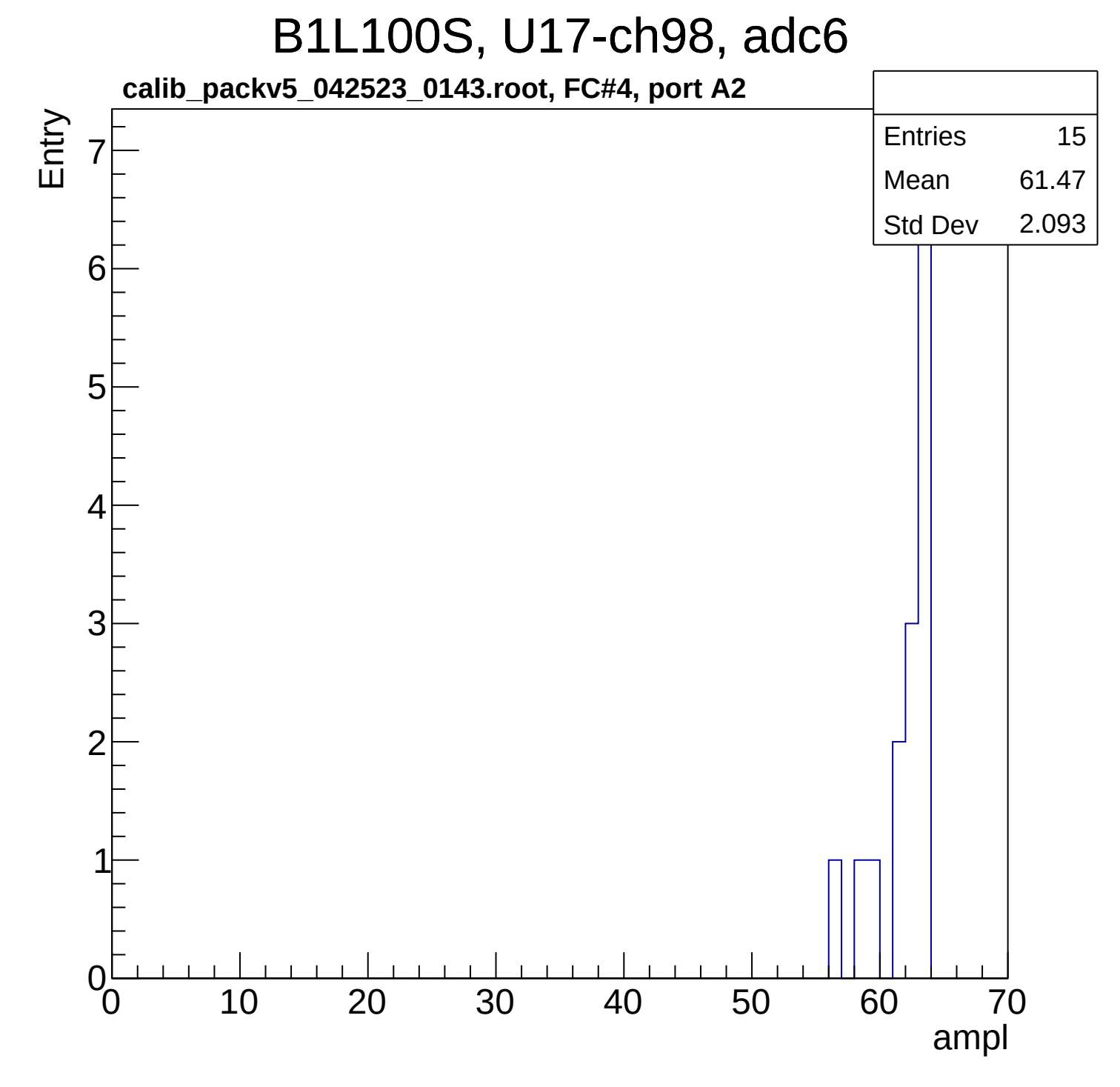
B1L100S, U17-ch98, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 15
Mean 61.47
Std Dev 2.093
Entry
ampl
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1
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3
4
5
6
7
0
10
20
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60
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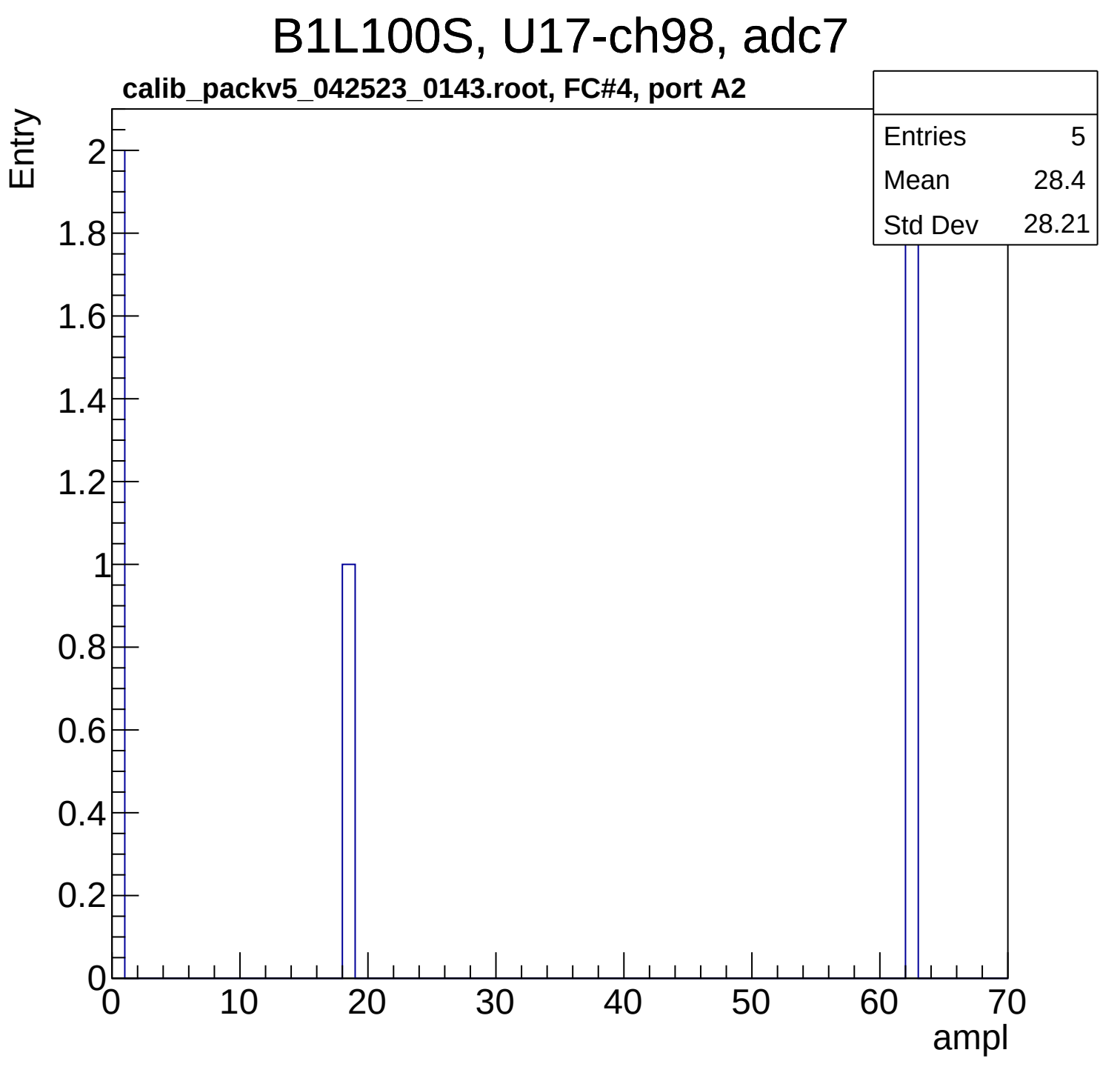
B1L100S, U17-ch98, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 5
Mean 28.4
Std Dev 28.21
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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40
50
60
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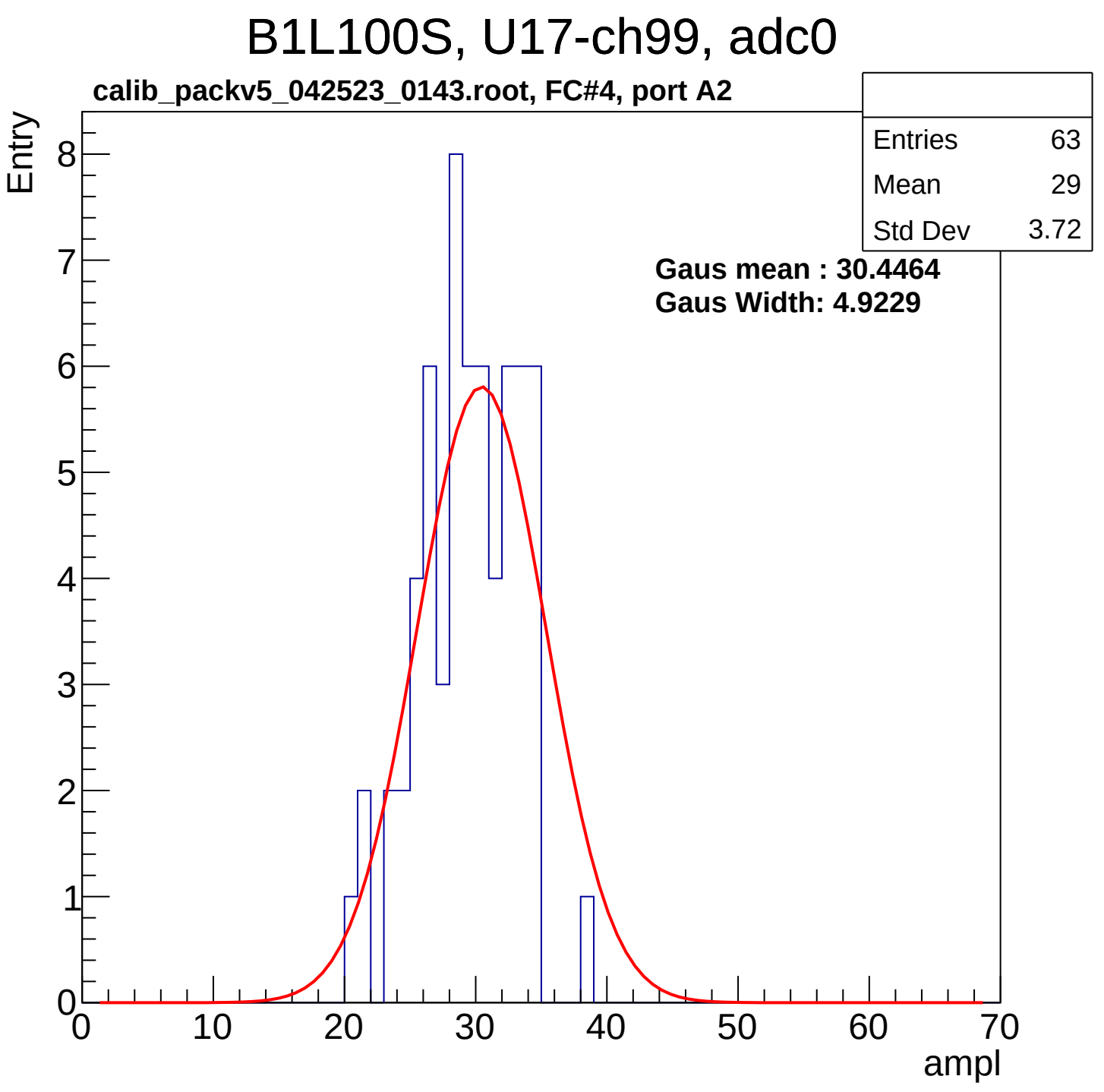
B1L100S, U17-ch99, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 29
Std Dev 3.72
Gaus mean : 30.4464
Gaus Width: 4.9229
Entry
ampl
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1
2
3
4
5
6
7
8
0
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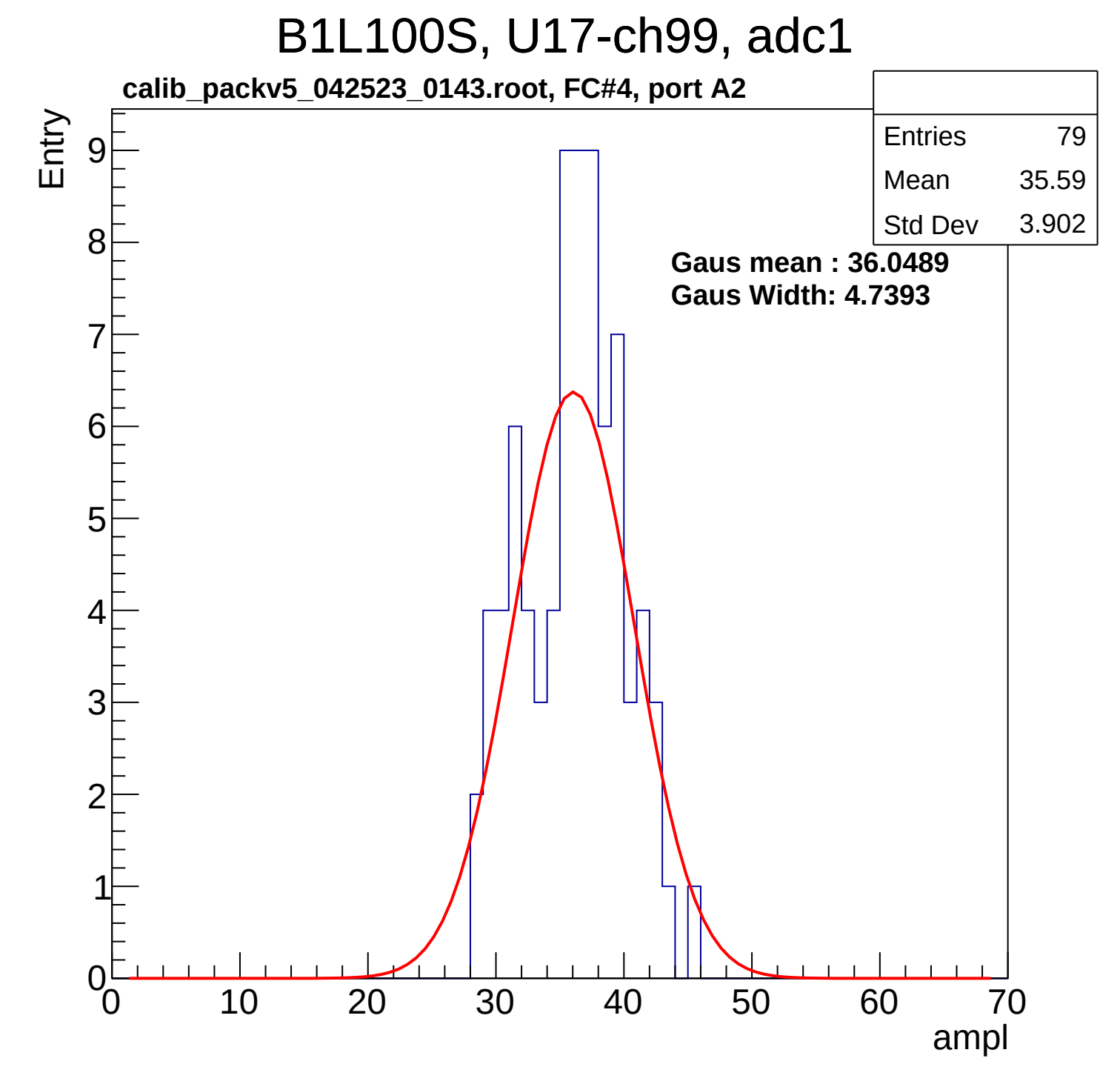
20
30
40
50
60
70


B1L100S, U17-ch99, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 79
Mean 35.59
Std Dev 3.902
Gaus mean : 36.0489
Gaus Width: 4.7393
Entry
ampl
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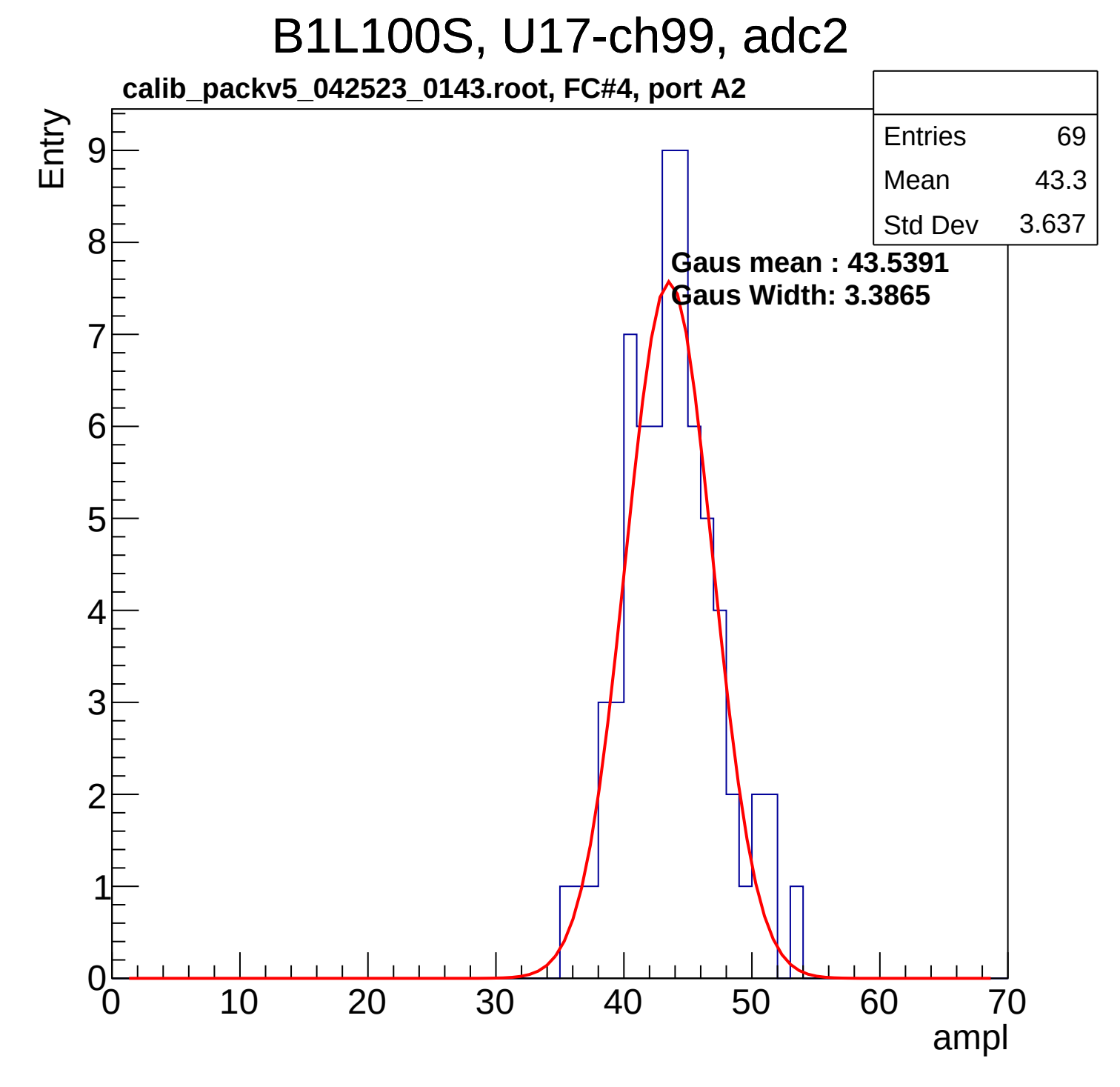
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch99, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 43.3
Std Dev 3.637
Gaus mean : 43.5391
Gaus Width: 3.3865
Entry
ampl
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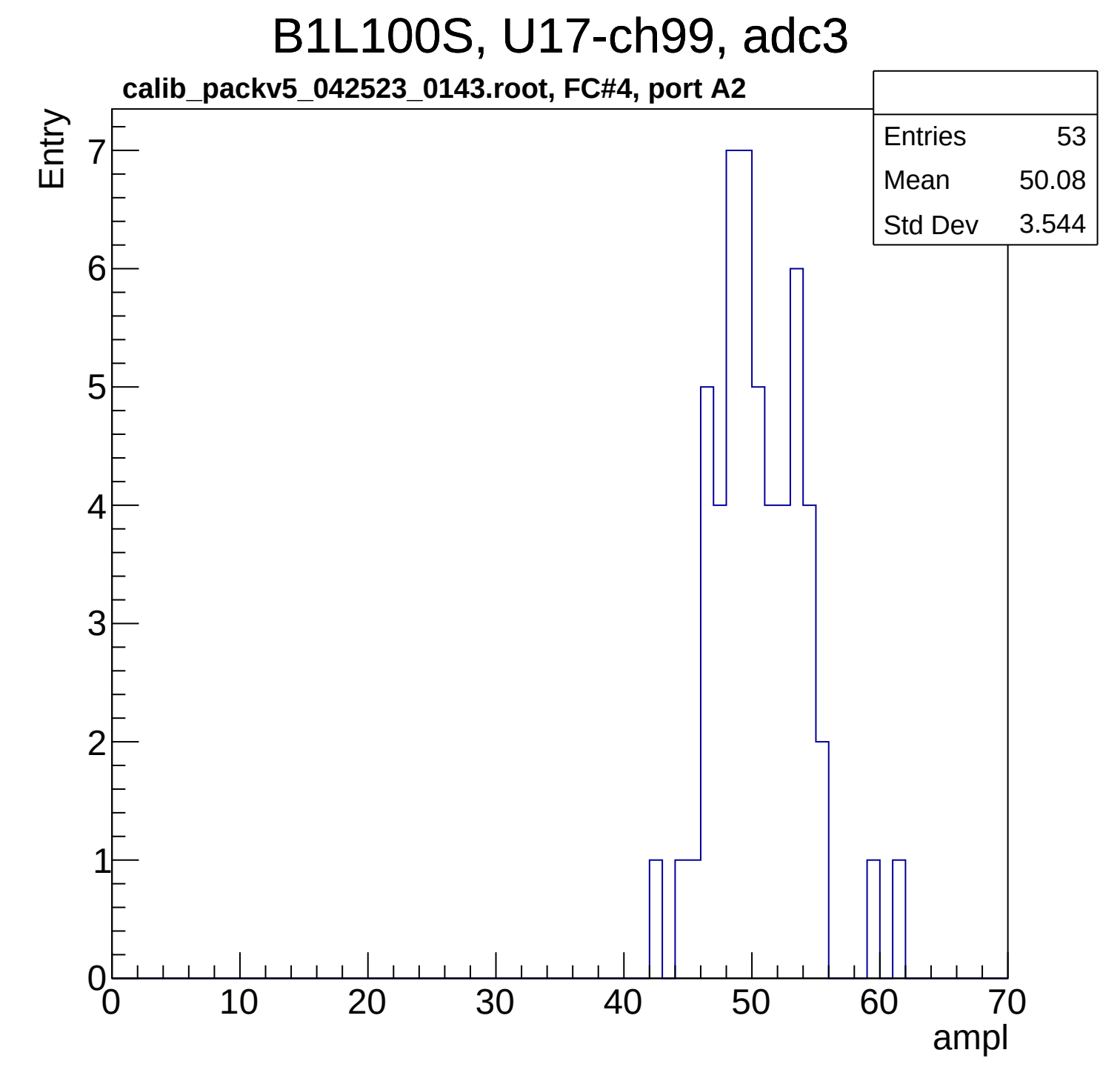
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L100S, U17-ch99, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 50.08
Std Dev 3.544
Entry
ampl
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1
2
3
4
5
6
7
0
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20
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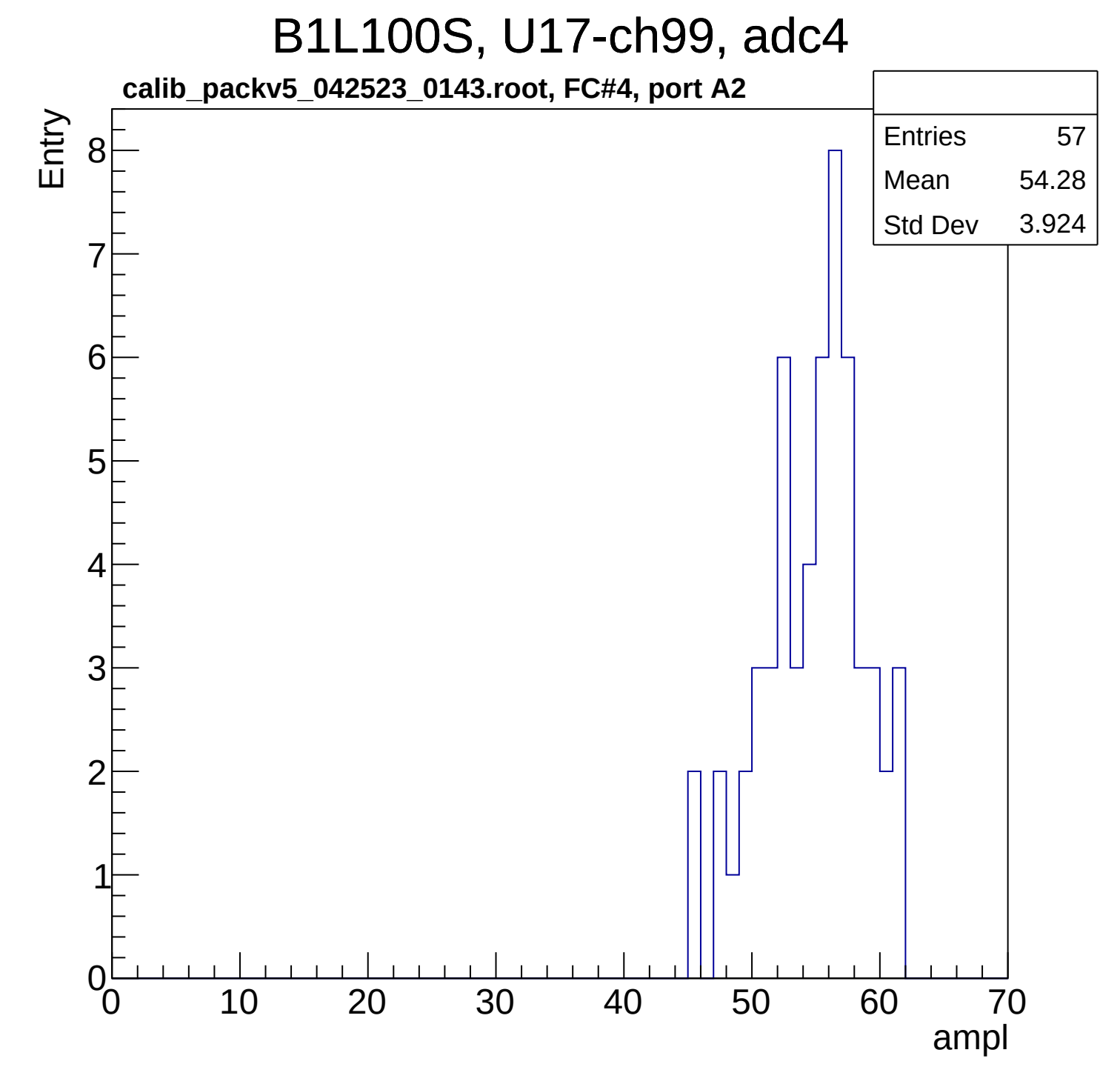
40
50
60
70


B1L100S, U17-ch99, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 54.28
Std Dev 3.924
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
50
60
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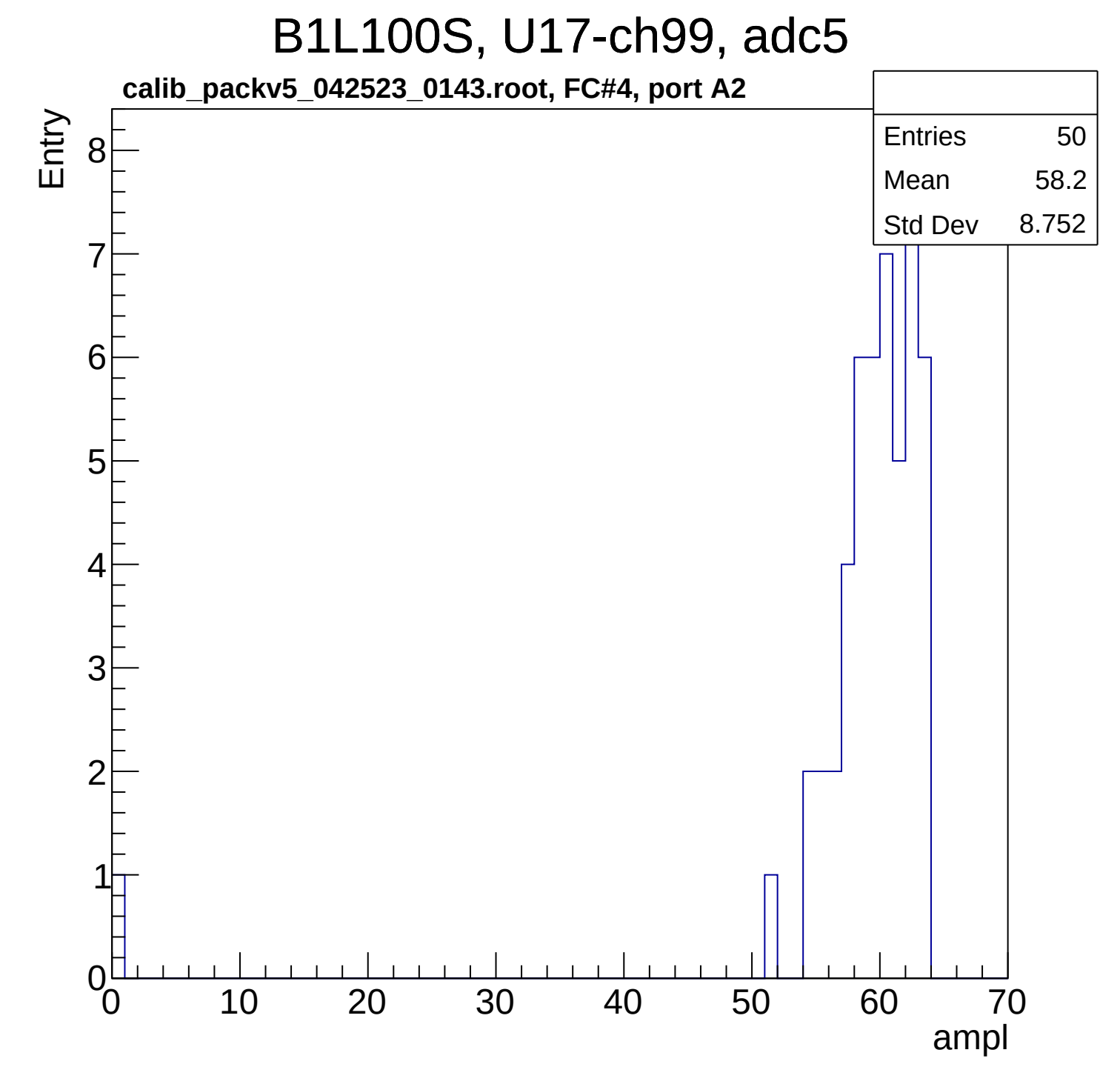
B1L100S, U17-ch99, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 58.2
Std Dev 8.752
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
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50
60
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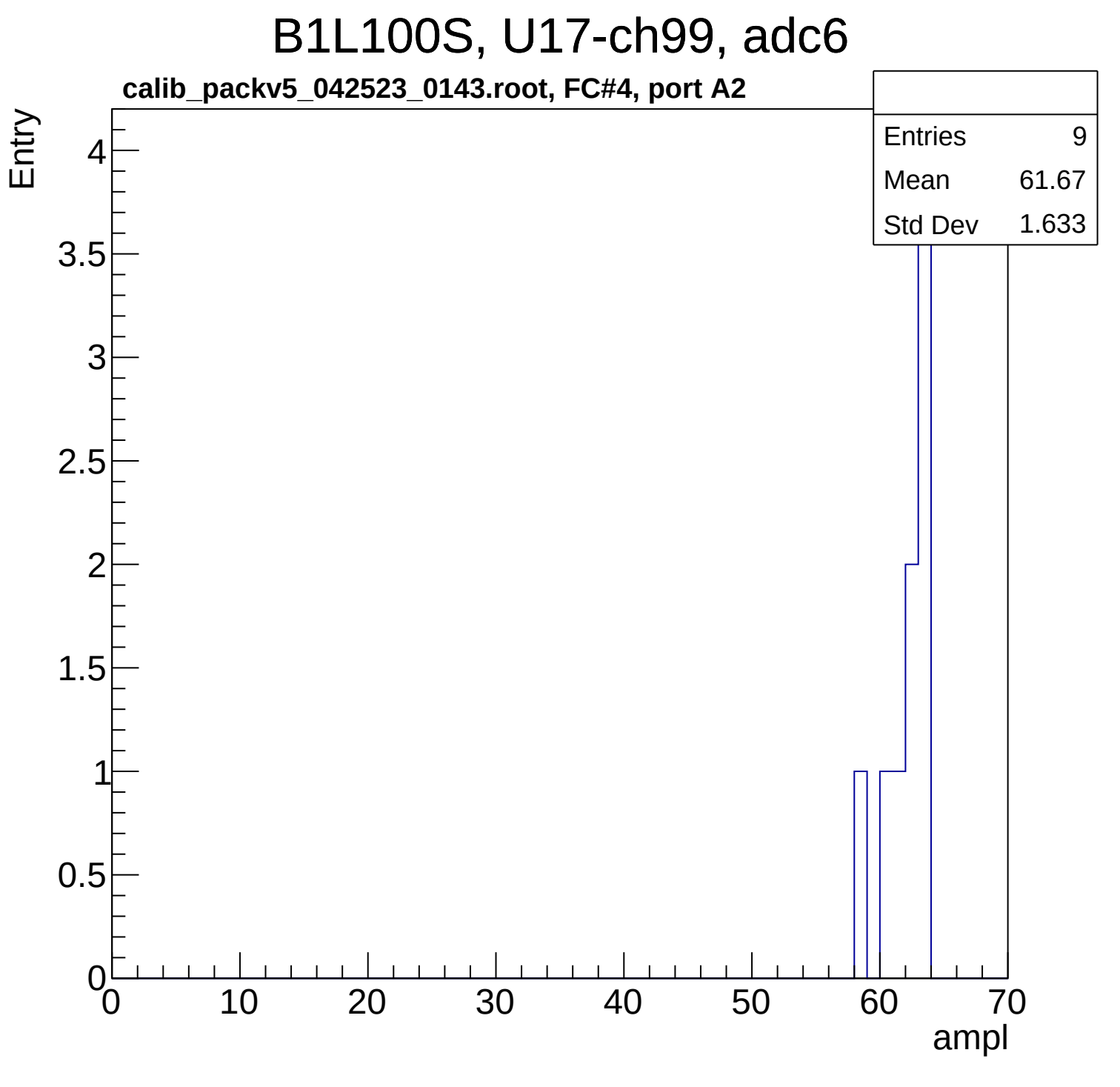
B1L100S, U17-ch99, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 9
Mean 61.67
Std Dev 1.633
Entry
ampl
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1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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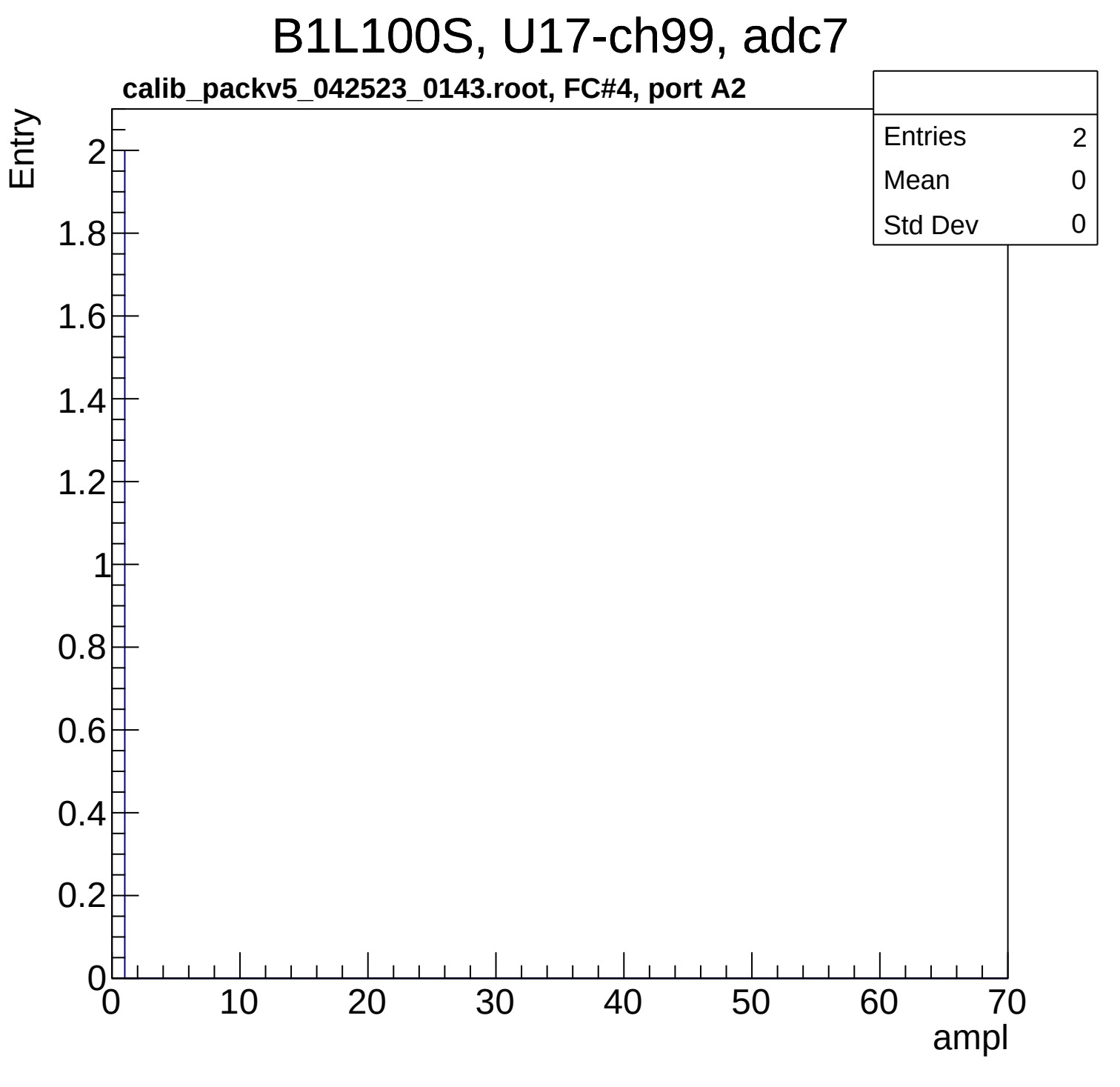
B1L100S, U17-ch99, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
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0.6
0.4
0.2
0
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10
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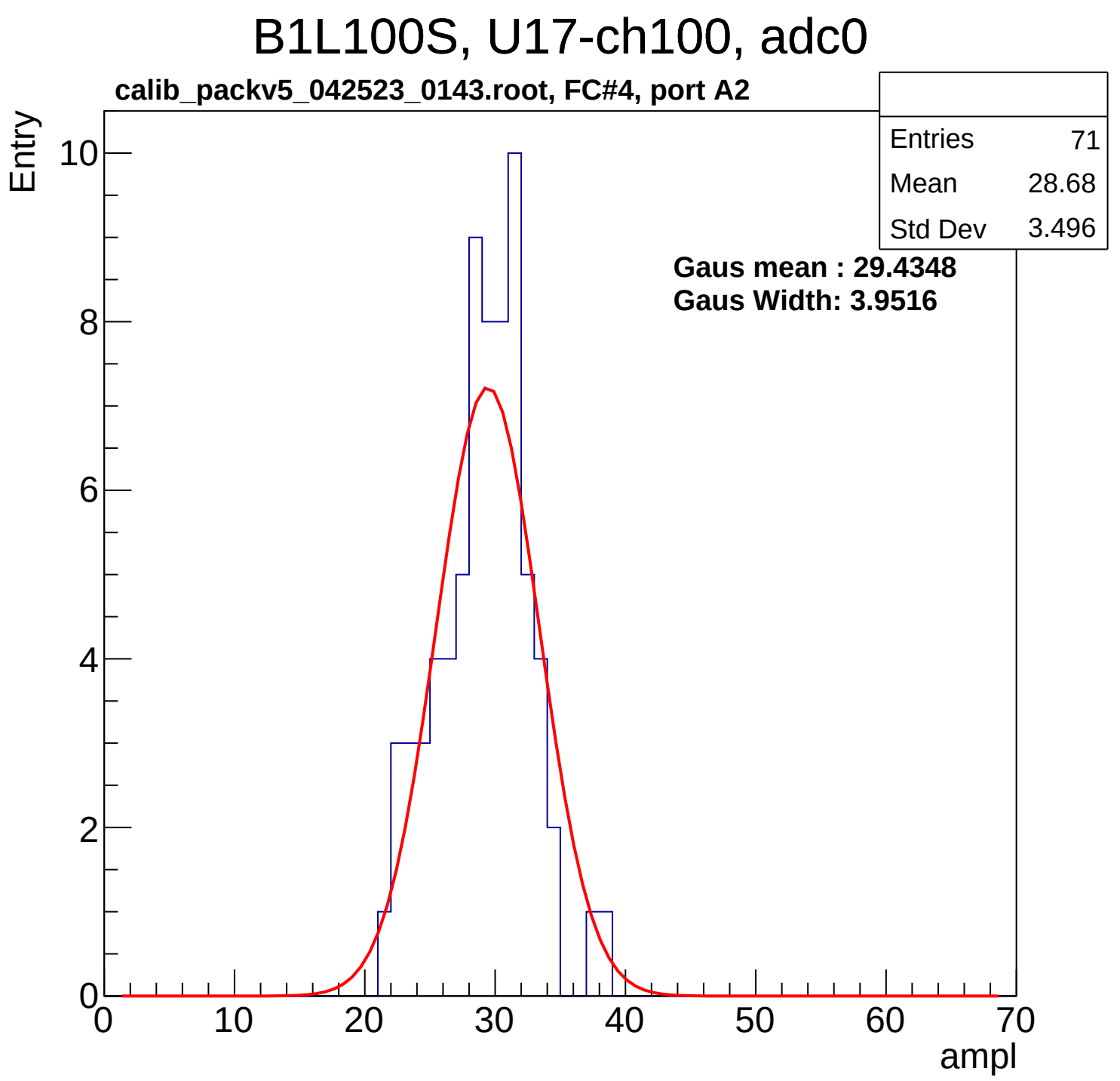
50
60
70
ampl


B1L100S, U17-ch100, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 28.68
Std Dev 3.496
Gaus mean : 29.4348
Gaus Width: 3.9516
Entry
ampl
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2
4
6
8
10
0
10
20
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40
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60
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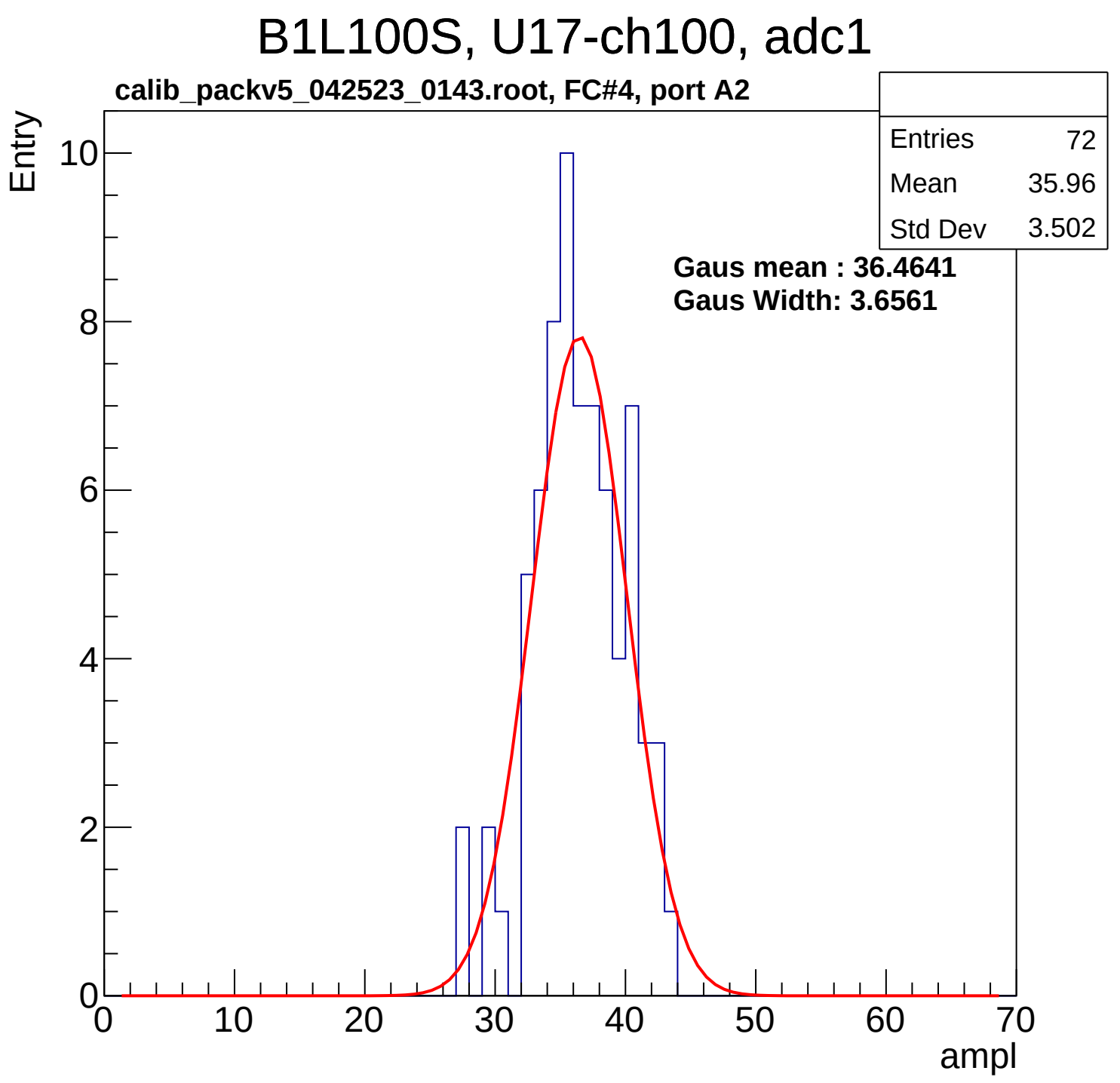
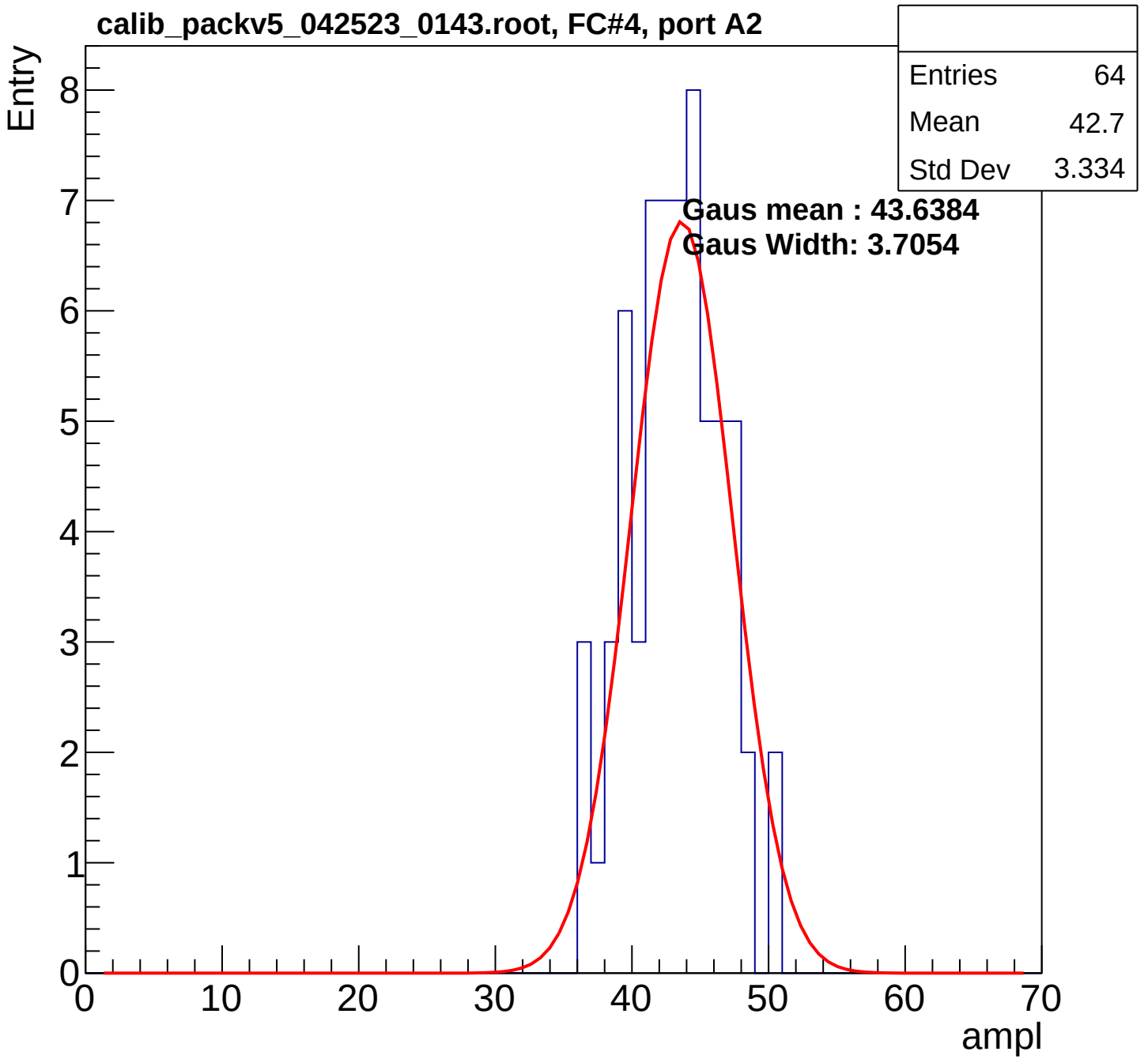

B1L100S, U17-ch100, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 35.96
Std Dev 3.502
Gaus mean : 36.4641
Gaus Width: 3.6561
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U17-ch100, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 42.7
Std Dev 3.334
Gaus mean : 43.6384
Gaus Width: 3.7054
Entry
ampl
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1
2
3
4
5
6
7
8
0
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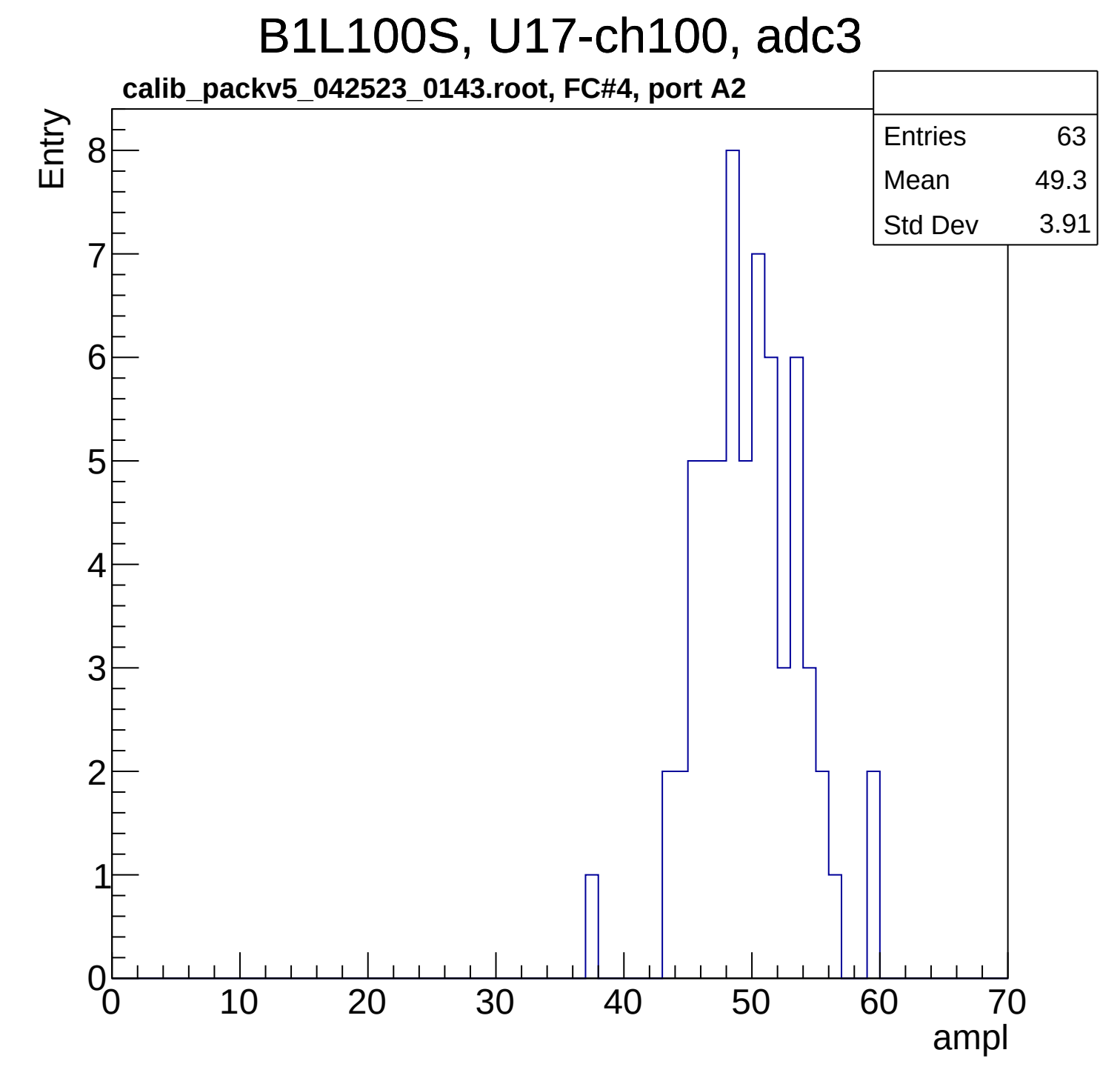
B1L100S, U17-ch100, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 49.3
Std Dev 3.91
Entry
ampl
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0
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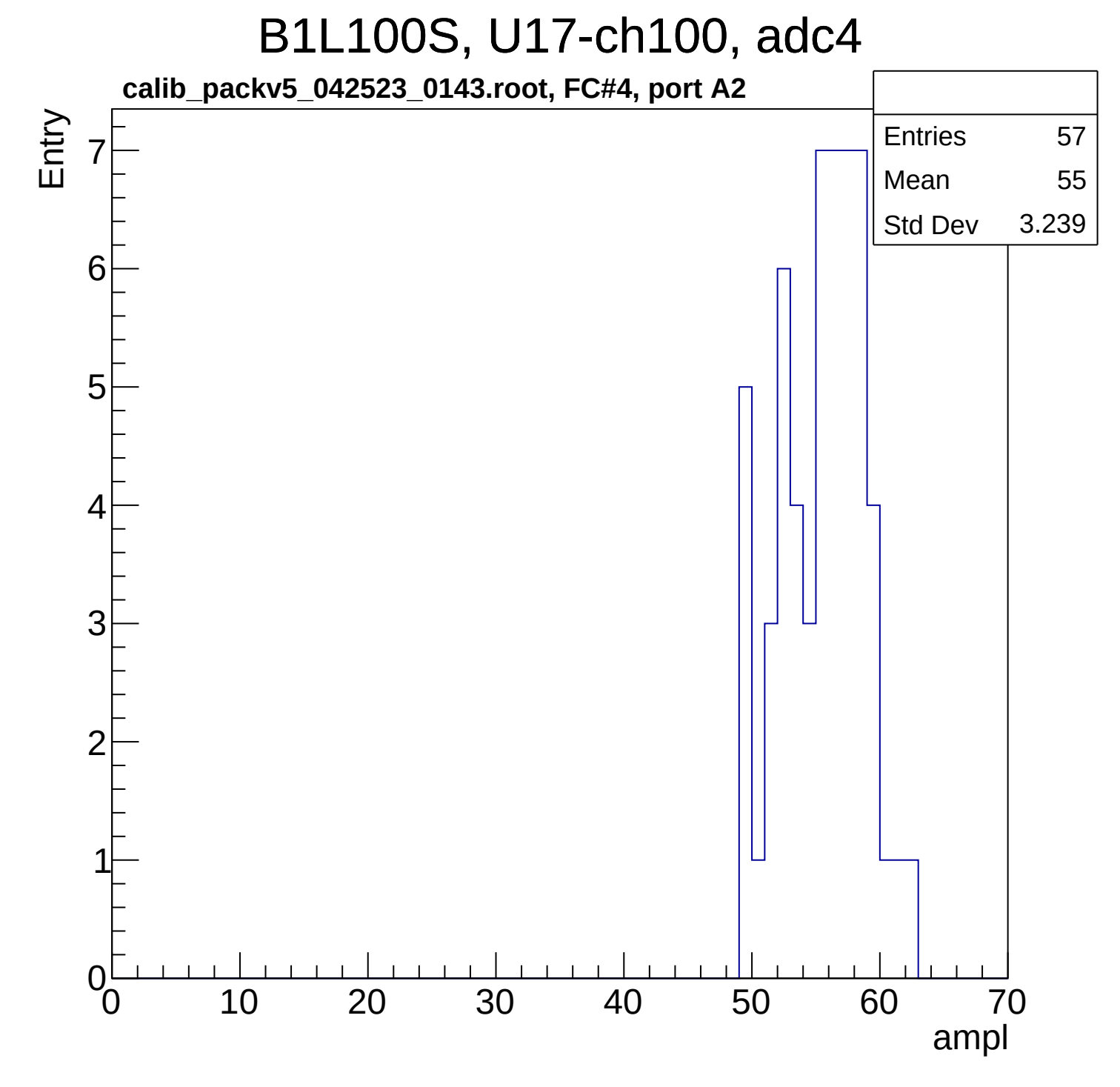
B1L100S, U17-ch100, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 55
Std Dev 3.239
Entry
ampl
0
1
2
3
4
5
6
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0
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60
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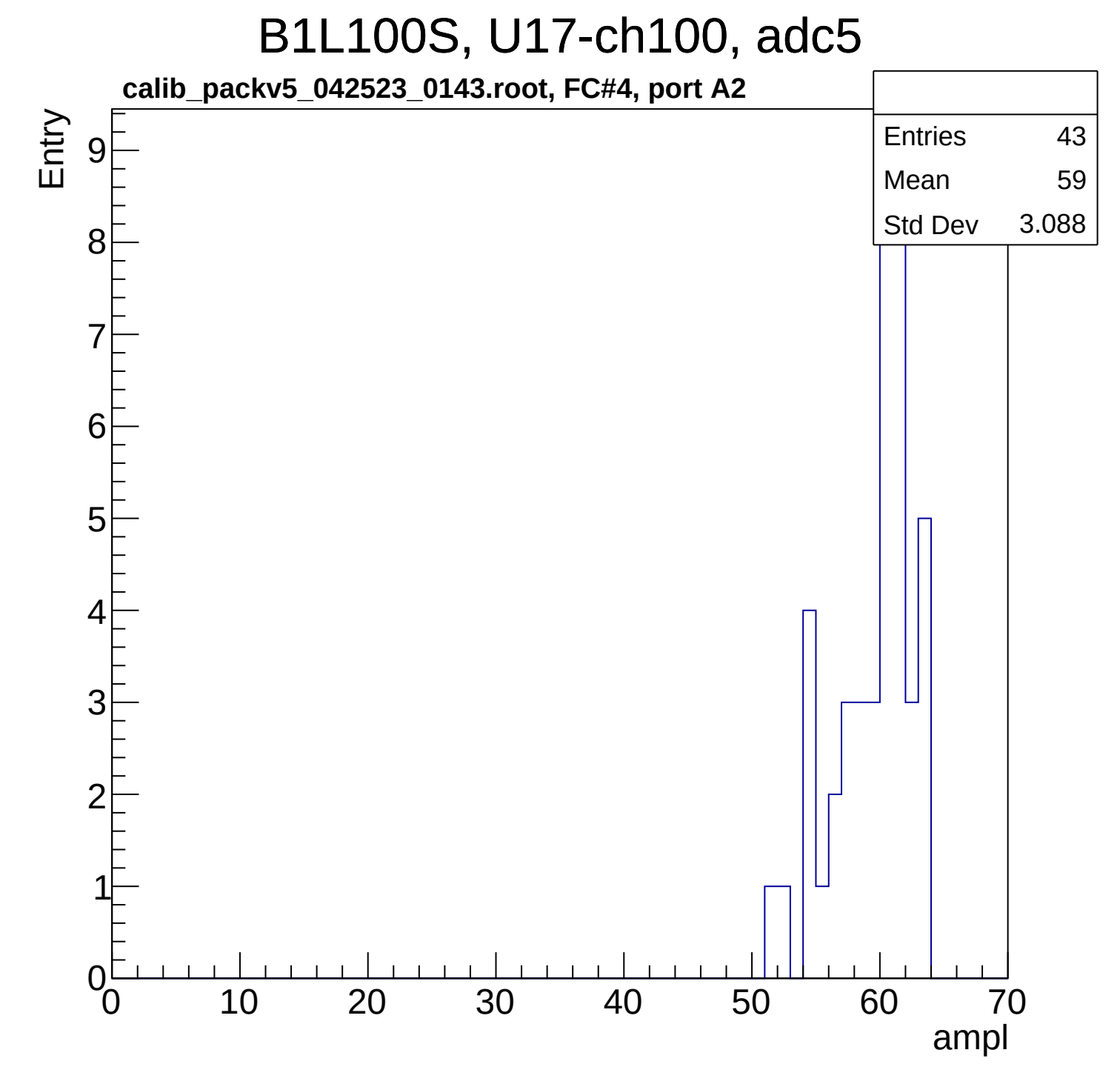
B1L100S, U17-ch100, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 43
Mean 59
Std Dev 3.088
Entry
ampl
0
1
2
3
4
5
6
7
8
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0
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60
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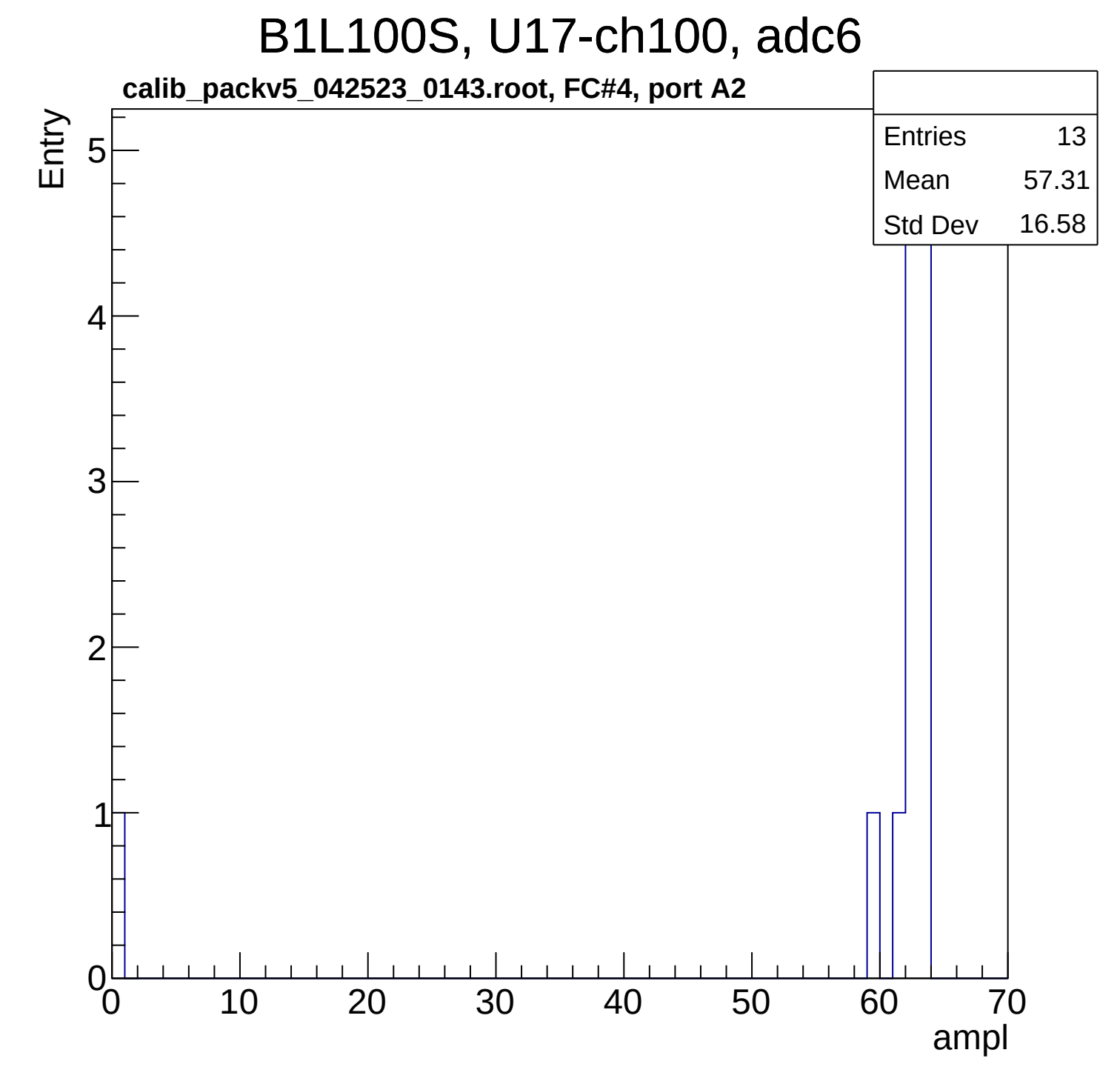
B1L100S, U17-ch100, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 13
Mean 57.31
Std Dev 16.58
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
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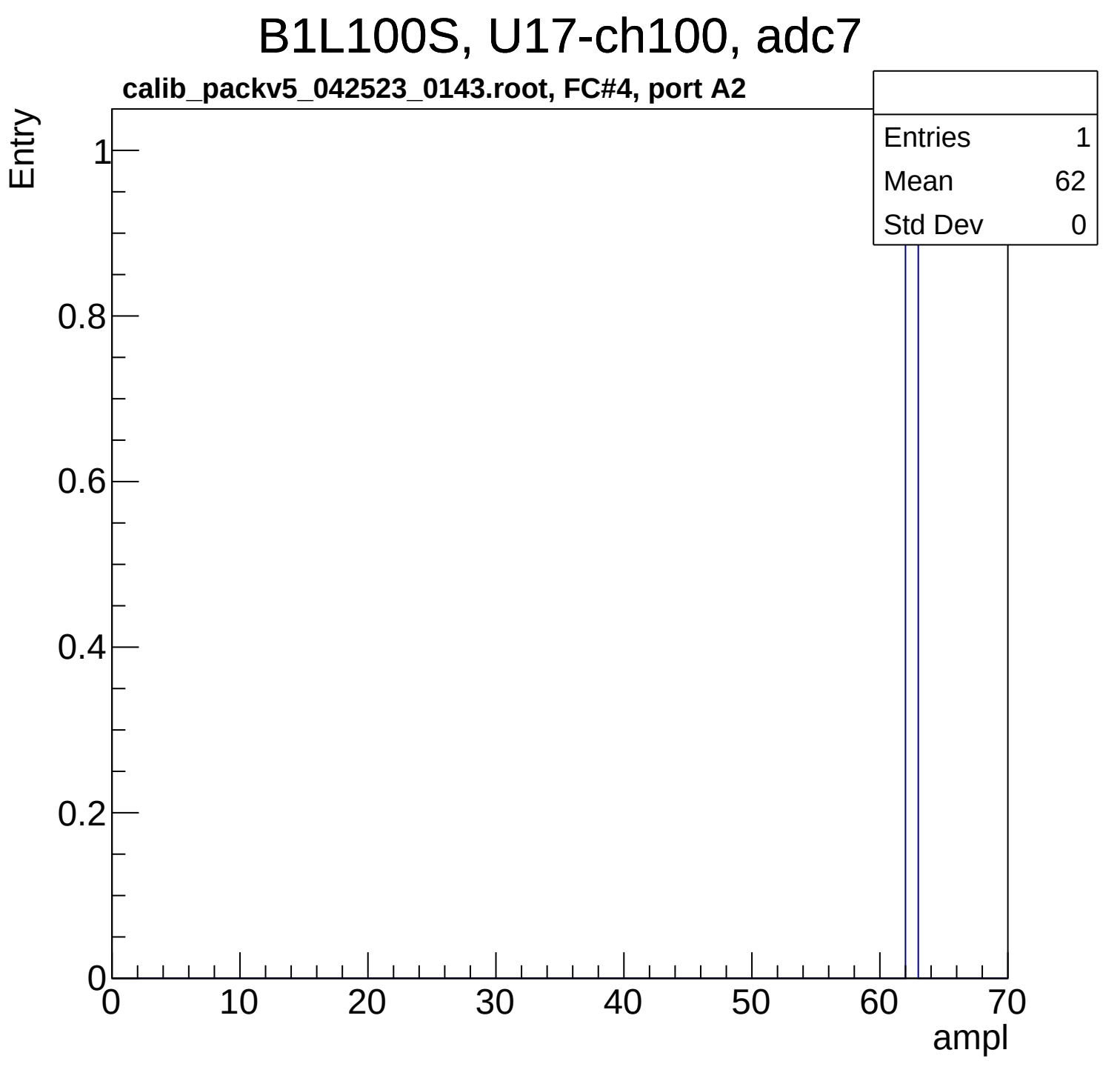
B1L100S, U17-ch100, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 62
Std Dev 0
Entry
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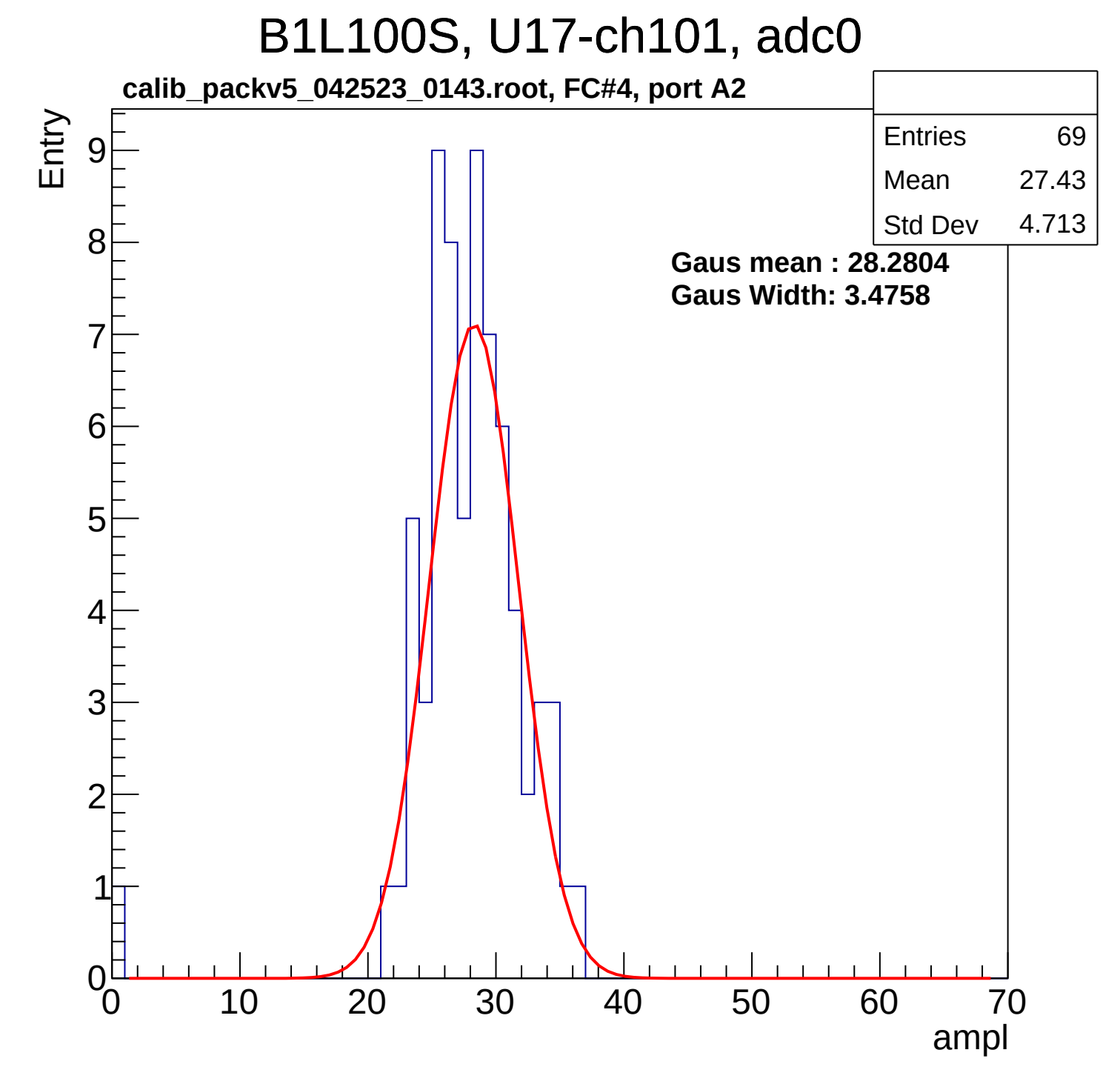
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch101, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 27.43
Std Dev 4.713
Gaus mean : 28.2804
Gaus Width: 3.4758
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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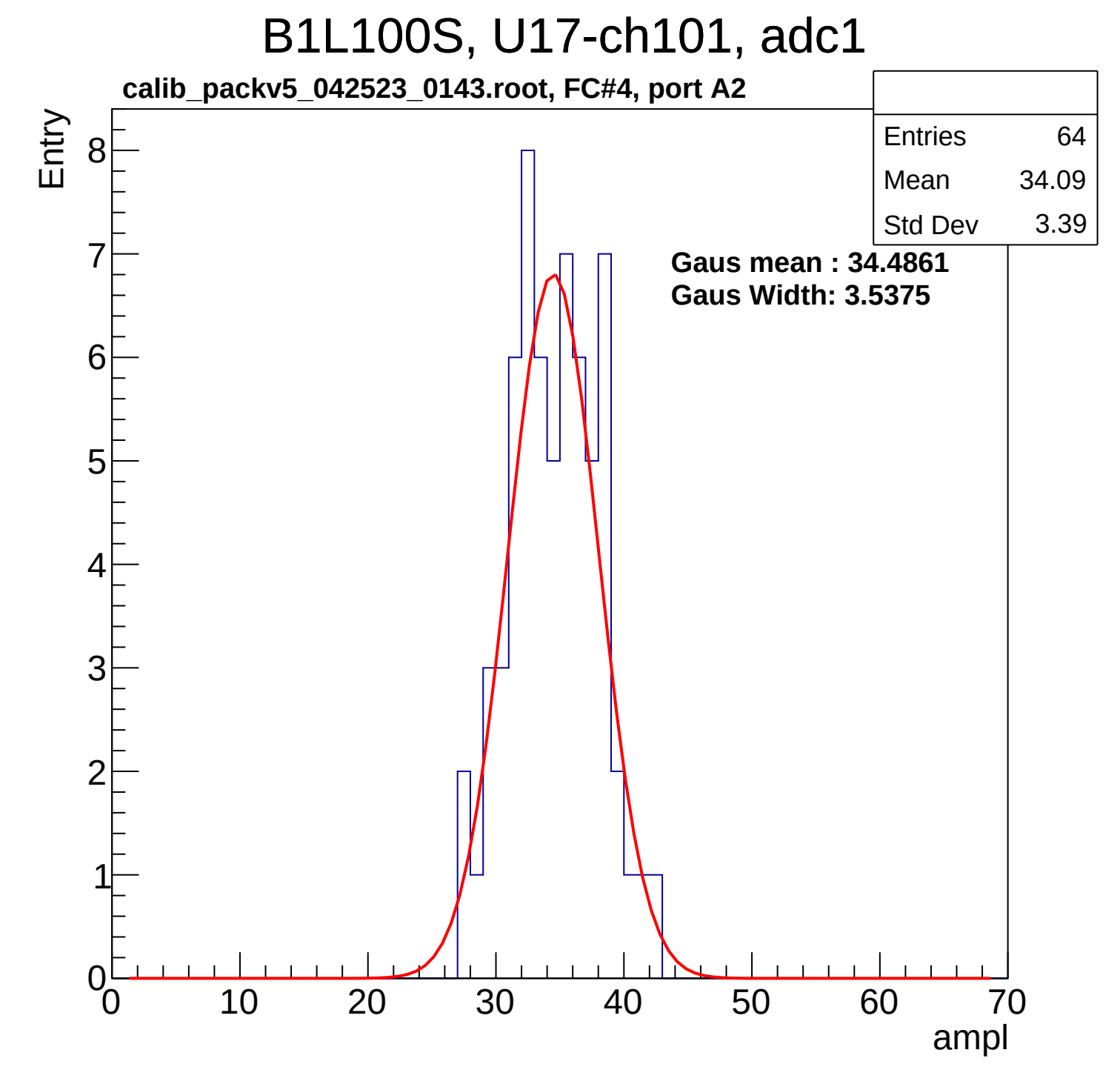
B1L100S, U17-ch101, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 34.09
Std Dev 3.39
Gaus mean : 34.4861
Gaus Width: 3.5375
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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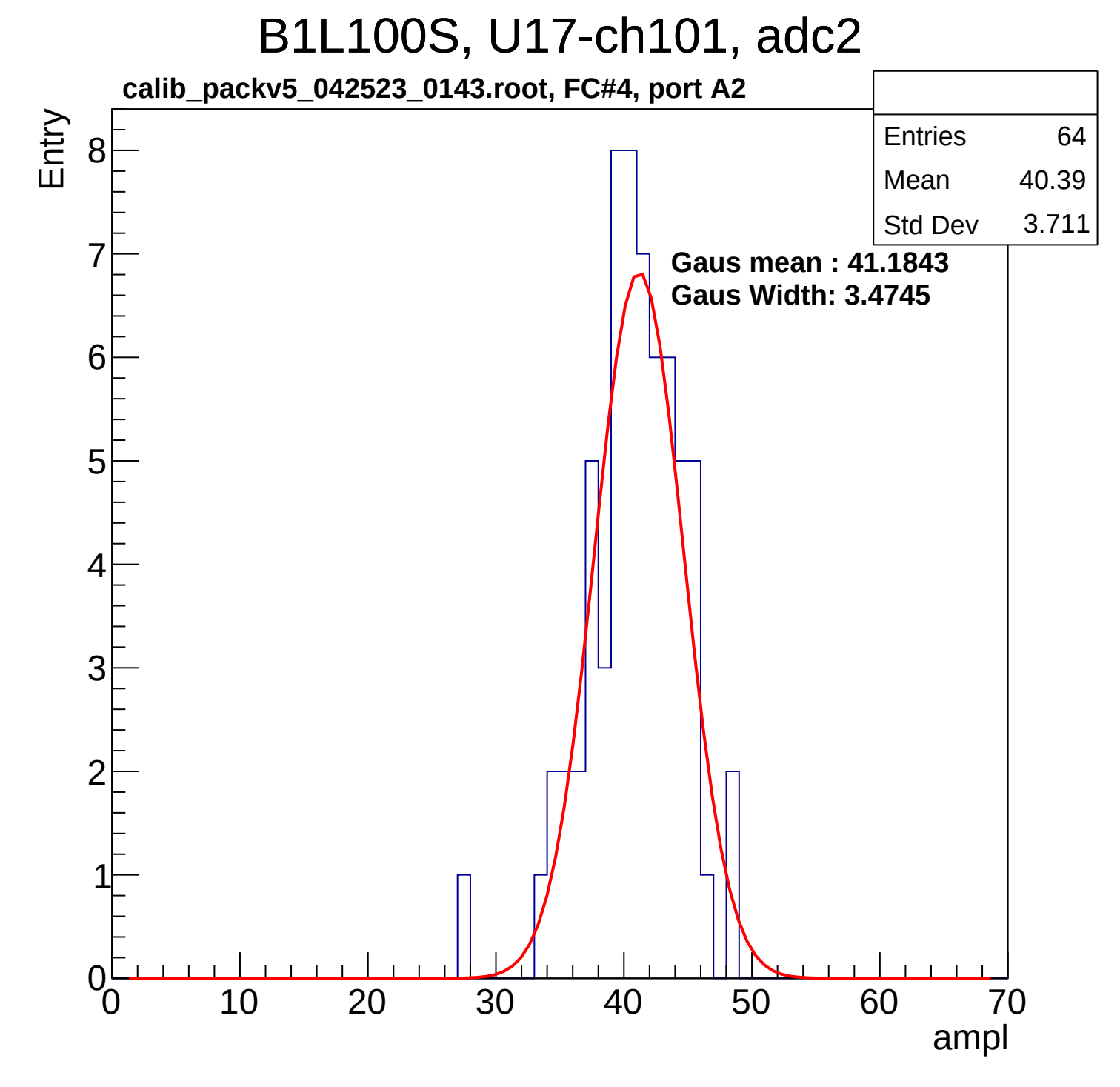
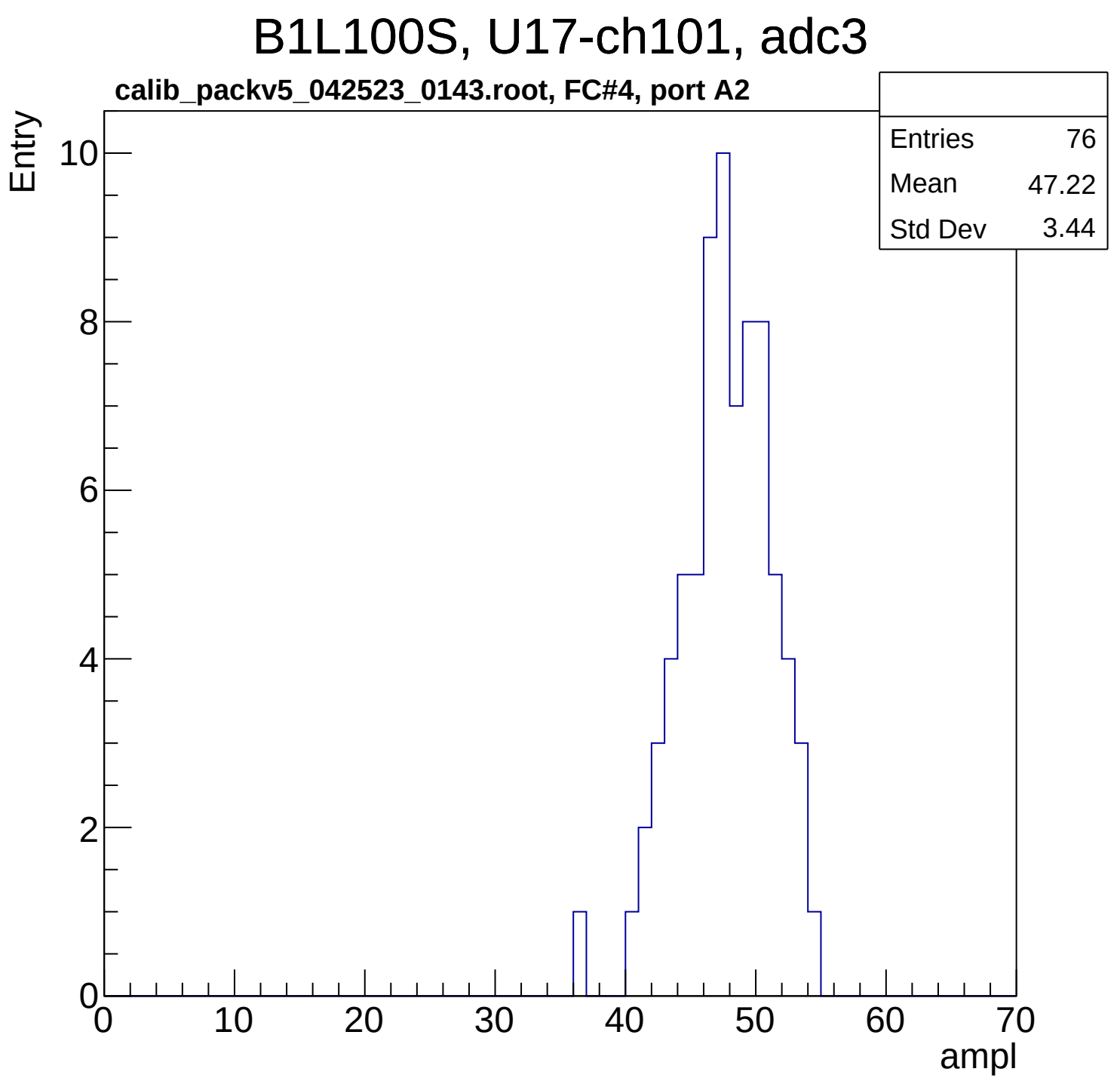
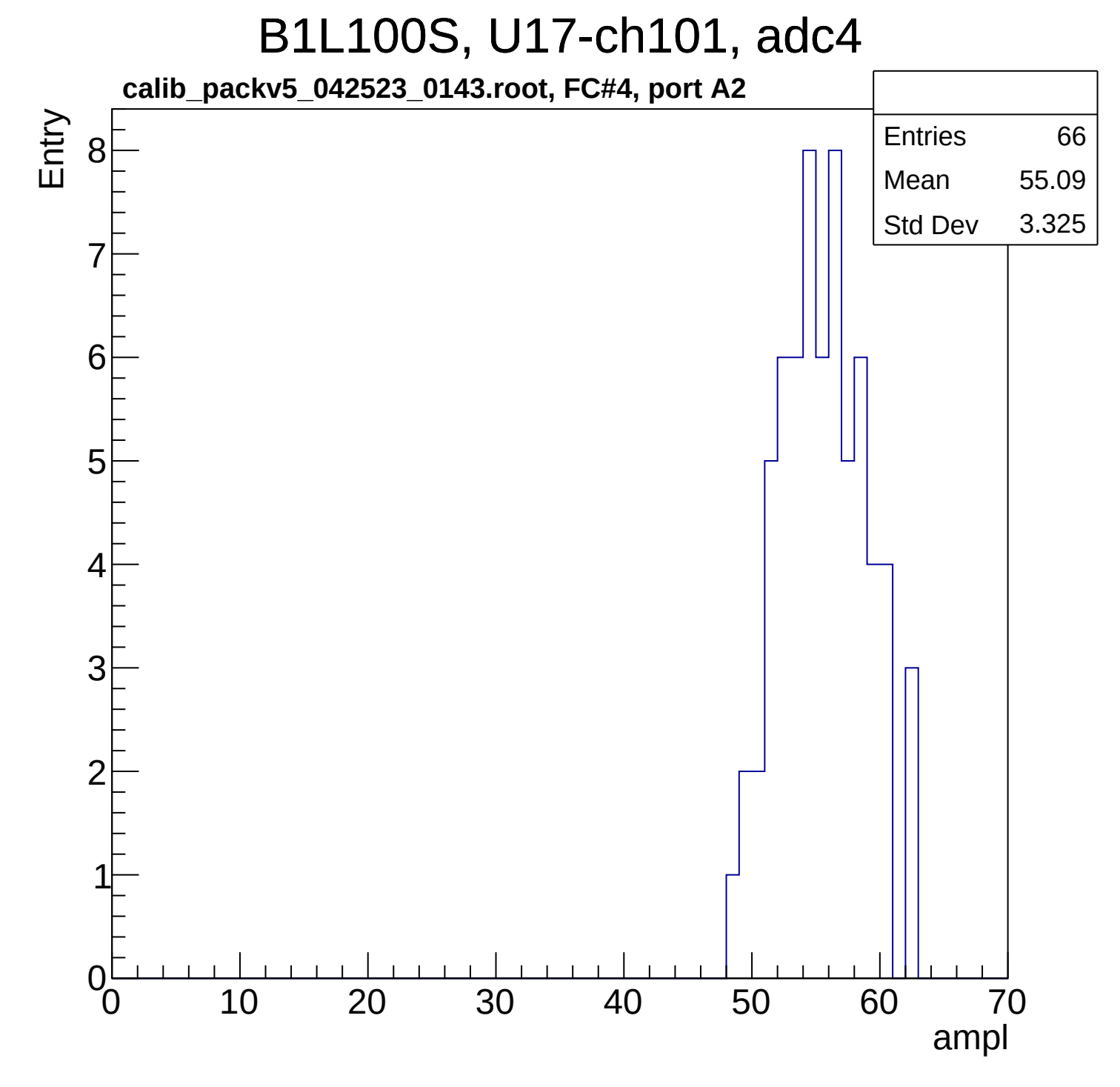

B1L100S, U17-ch101, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 40.39
Std Dev 3.711
Gaus mean : 41.1843
Gaus Width: 3.4745
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch101, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 76
Mean 47.22
Std Dev 3.44
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U17-ch101, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 55.09
Std Dev 3.325
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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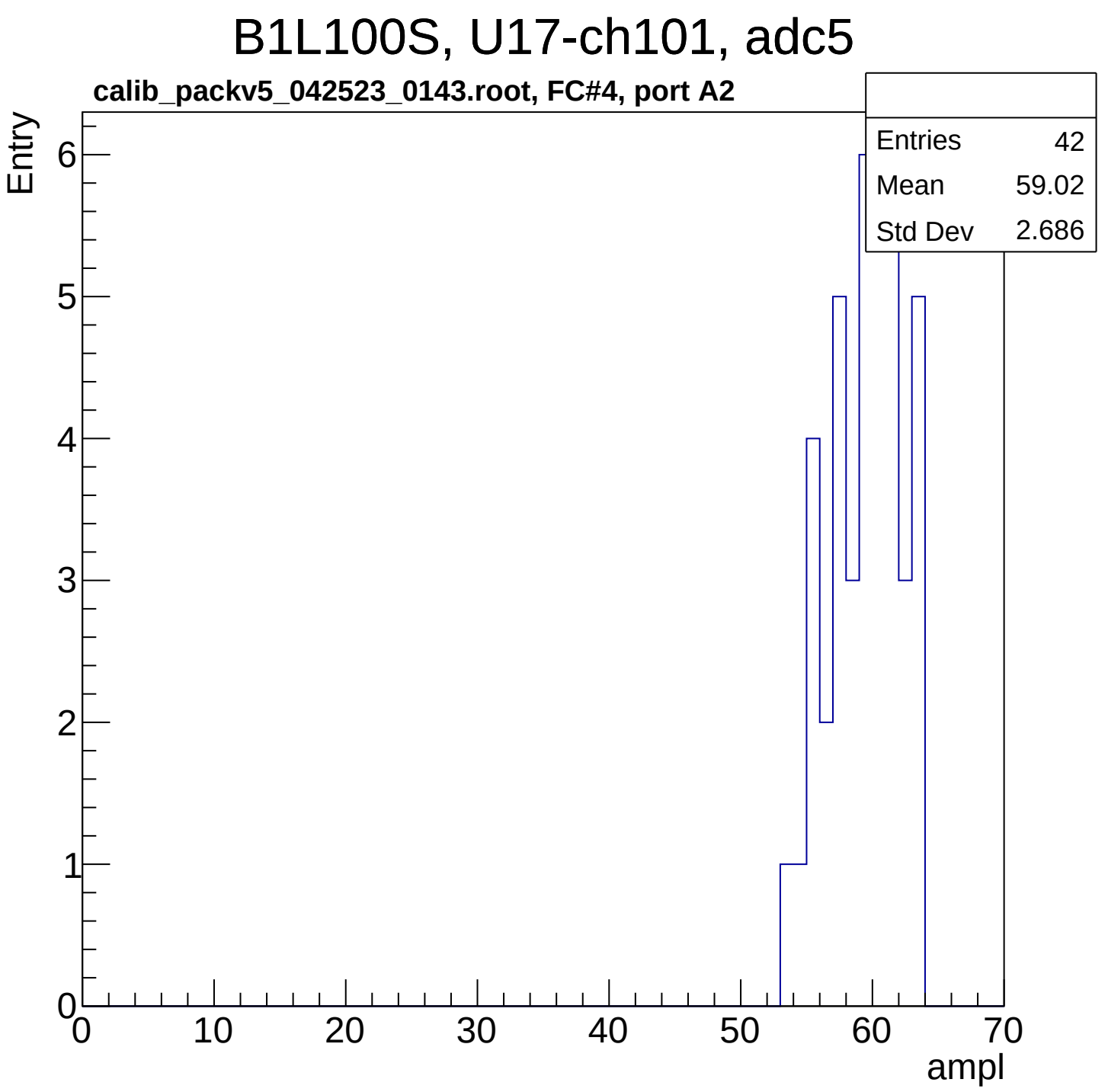
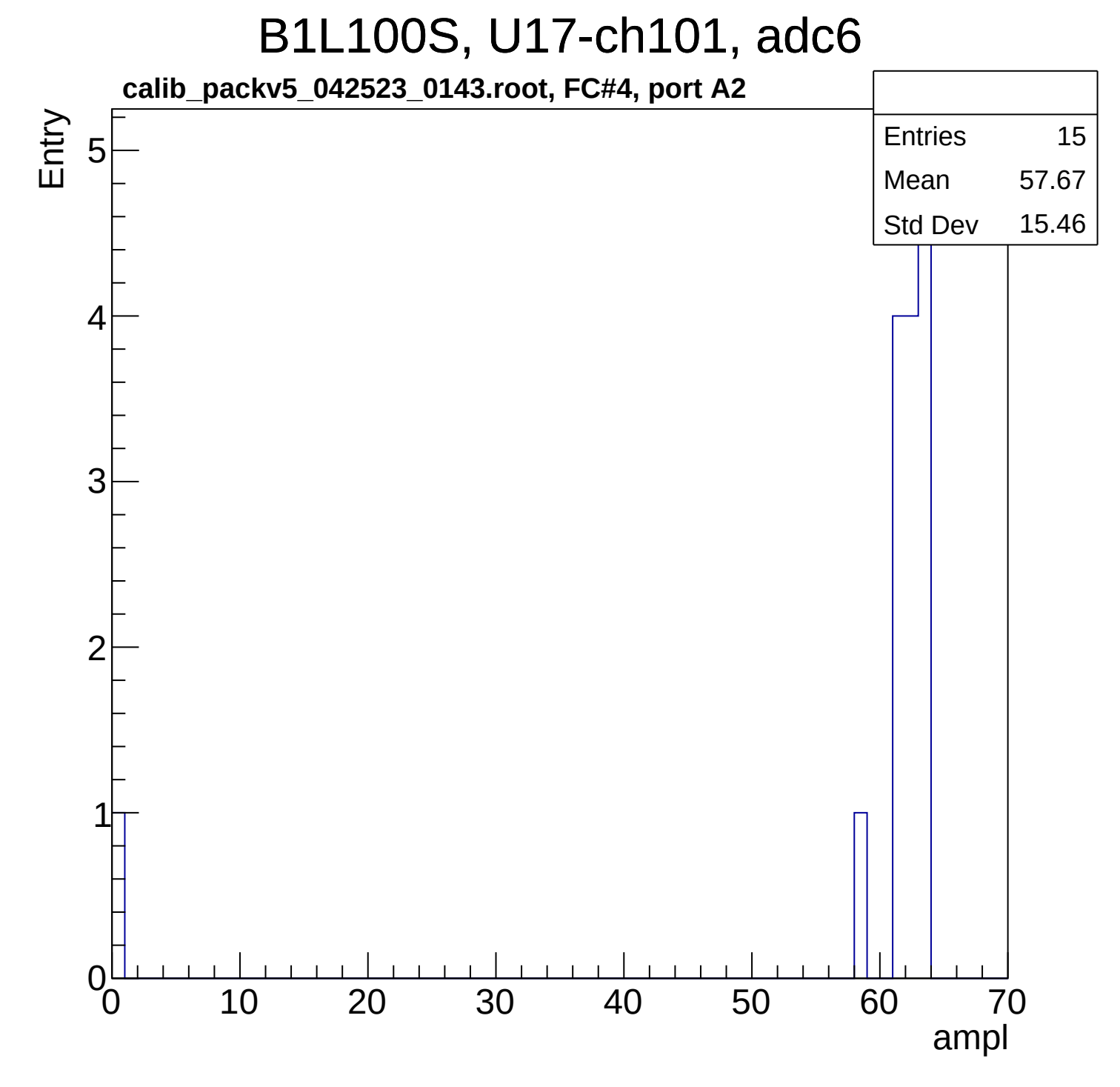
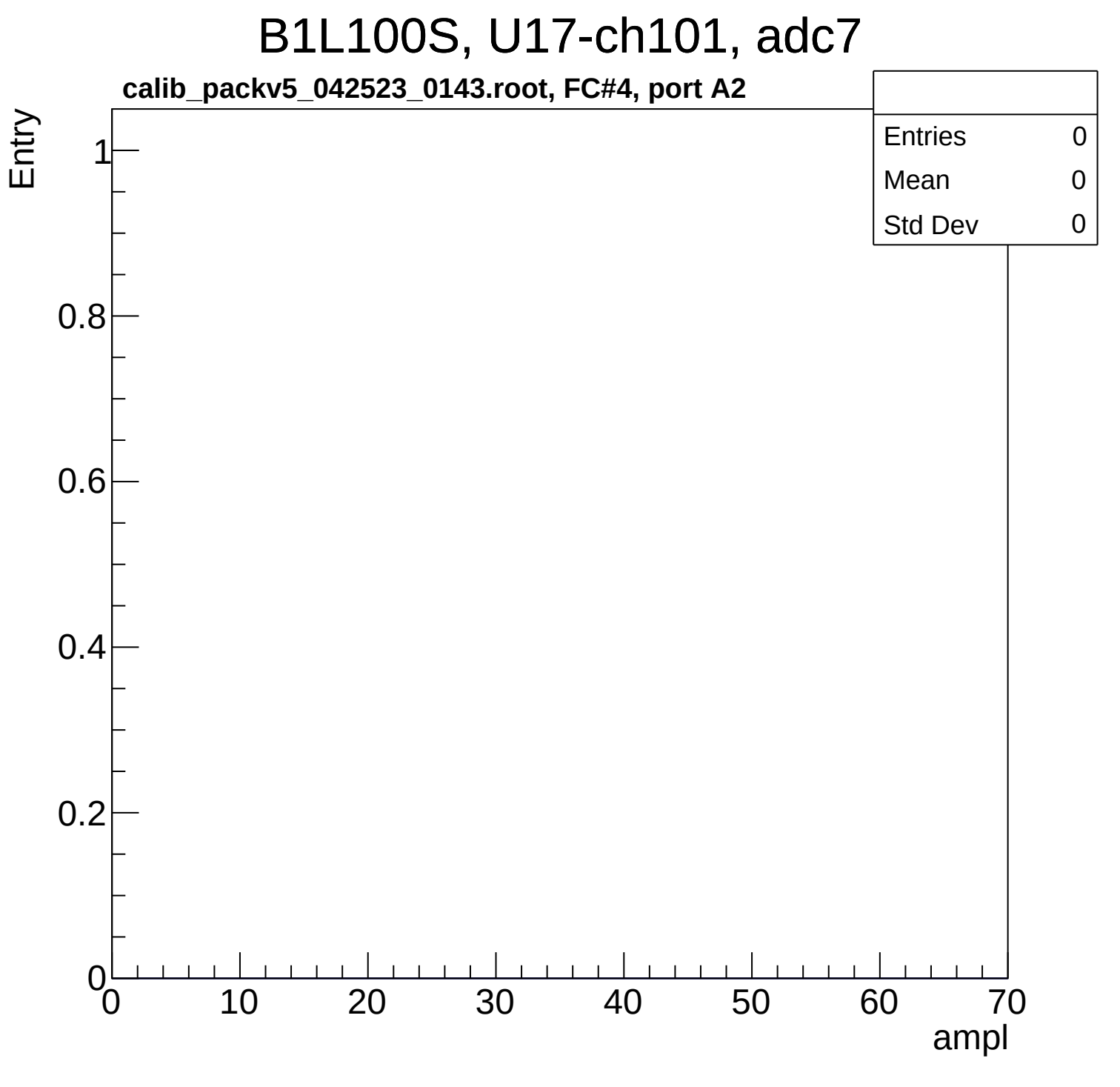
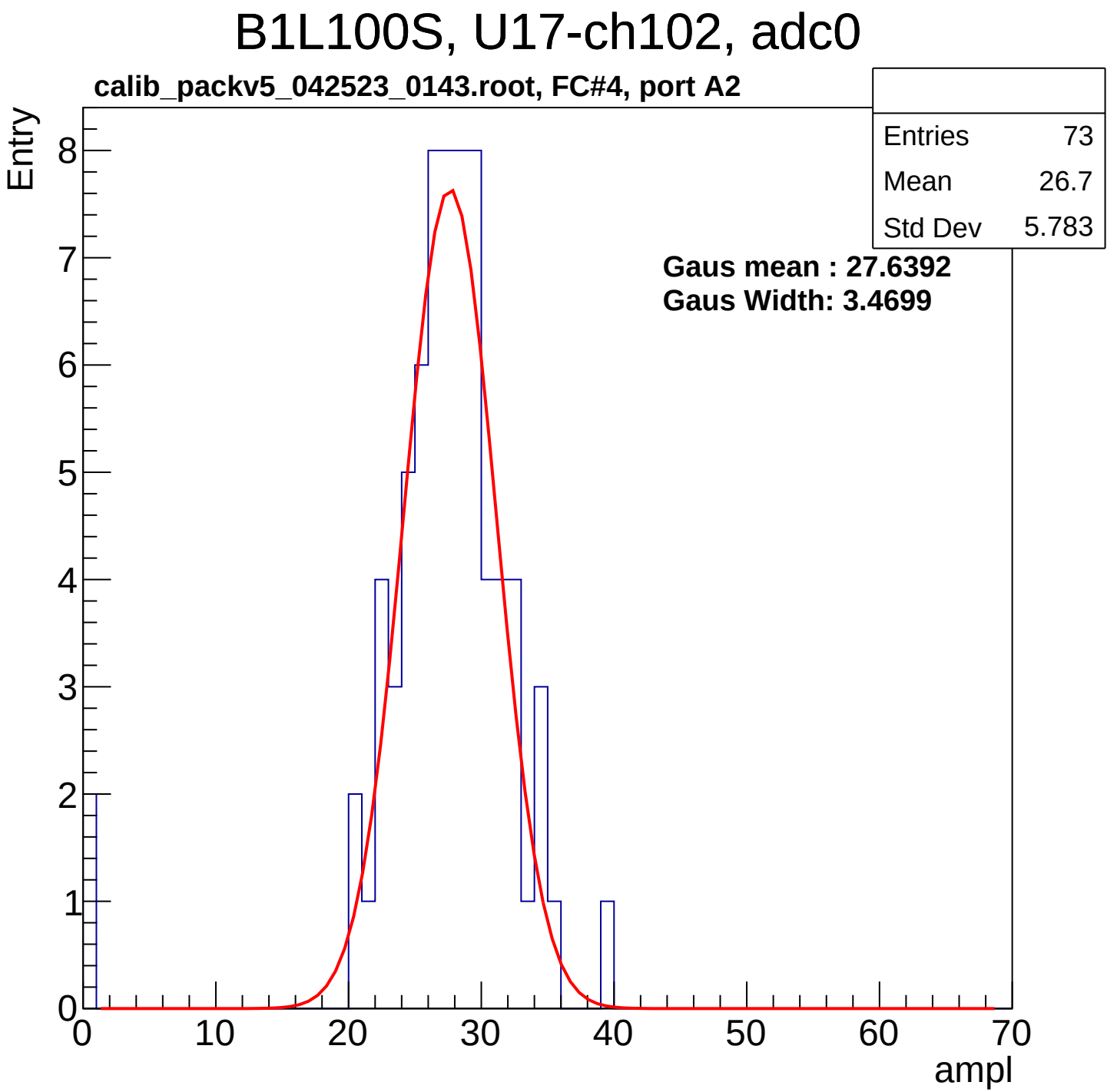
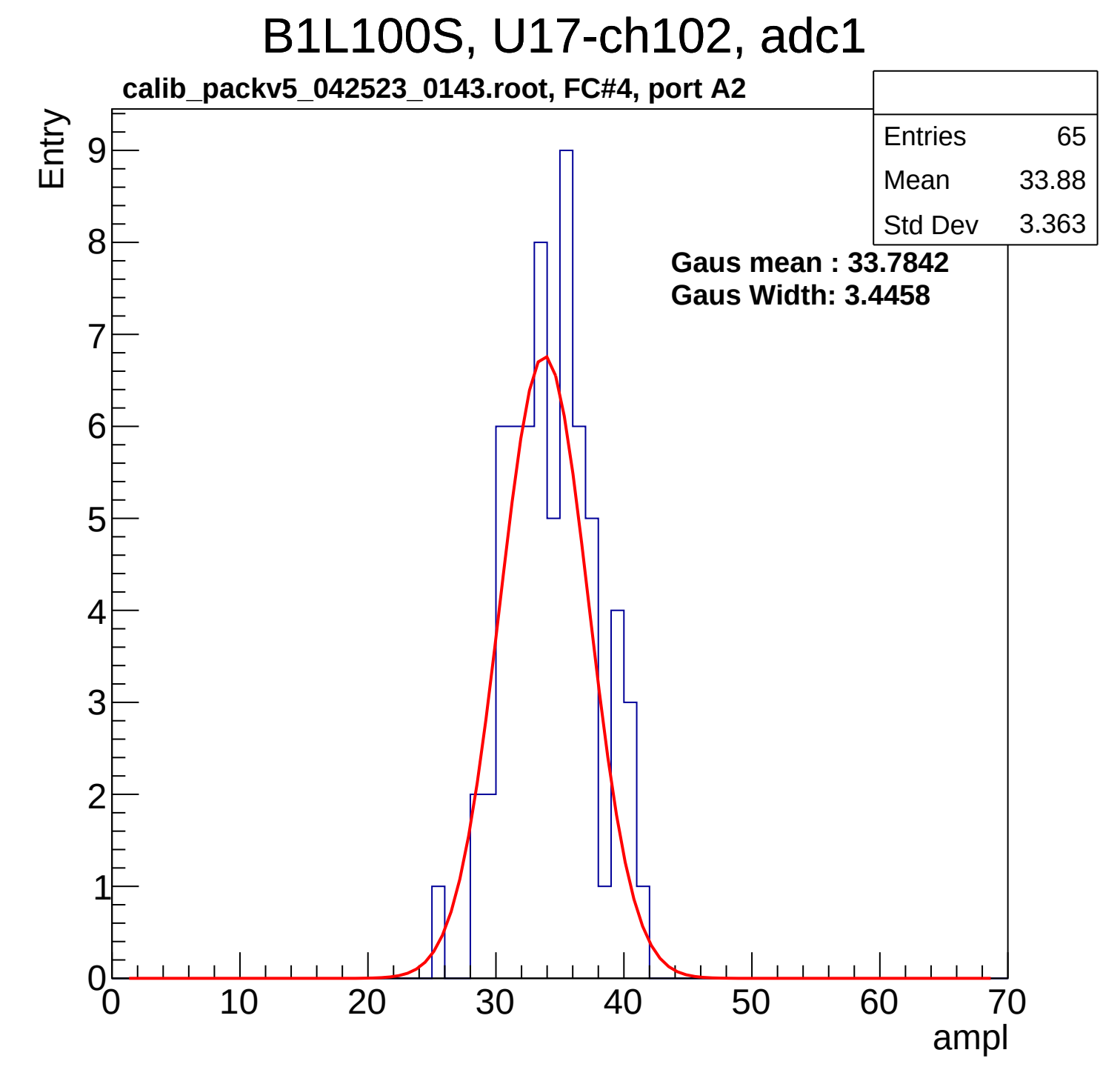
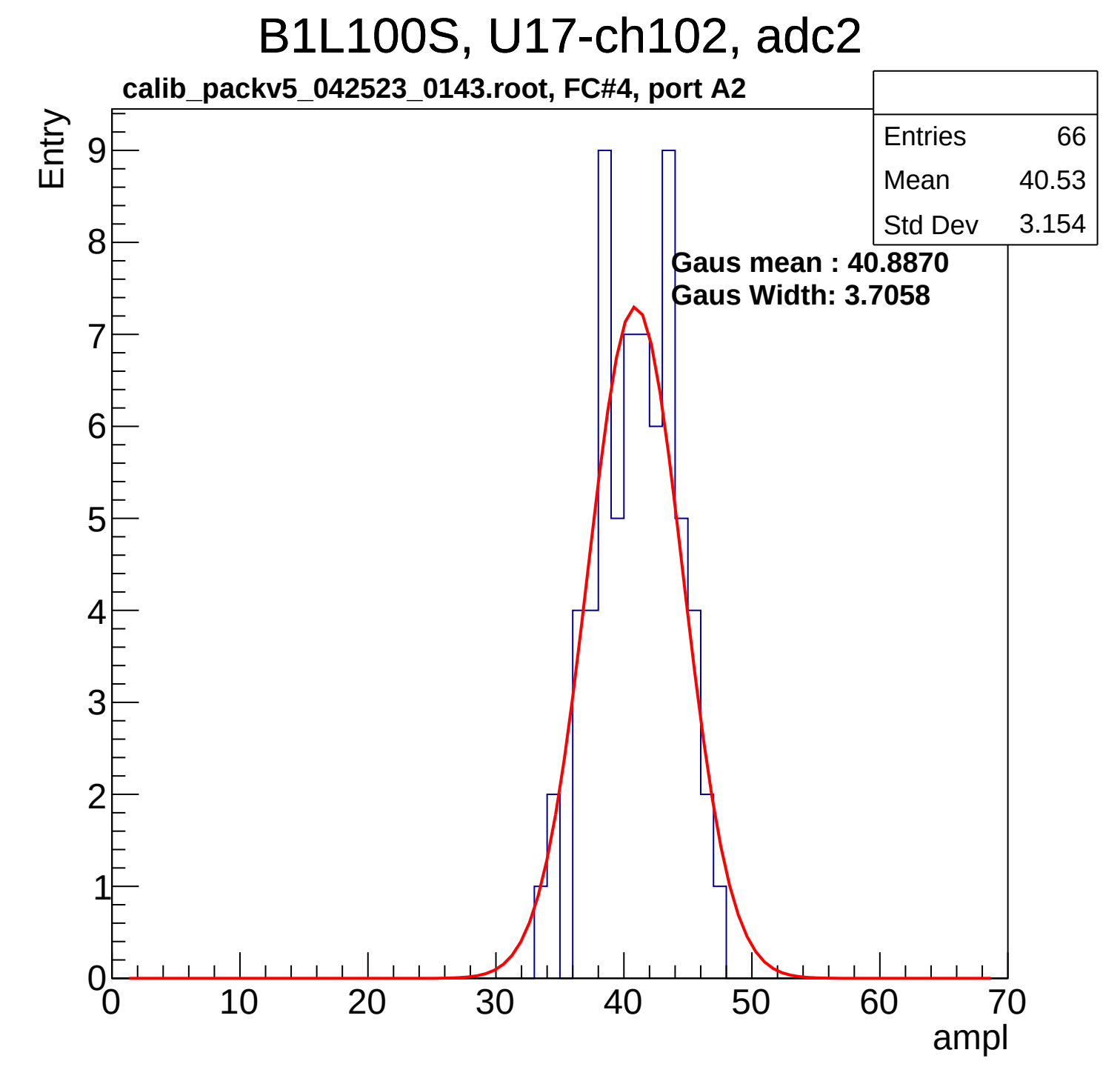

B1L100S, U17-ch101, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 42
Mean 59.02
Std Dev 2.686
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

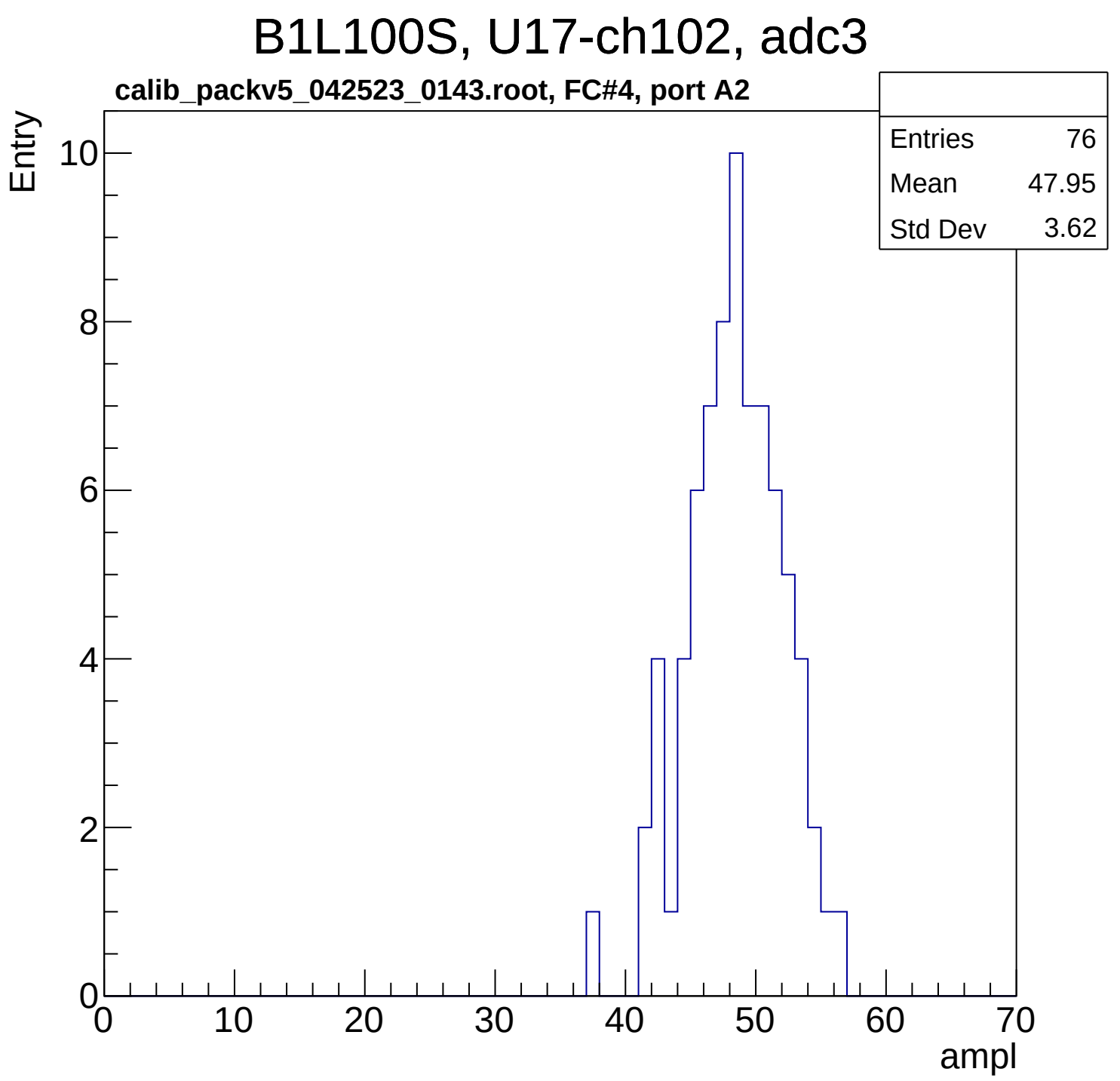

B1L100S, U17-ch101, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 15
Mean 57.67
Std Dev 15.46
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

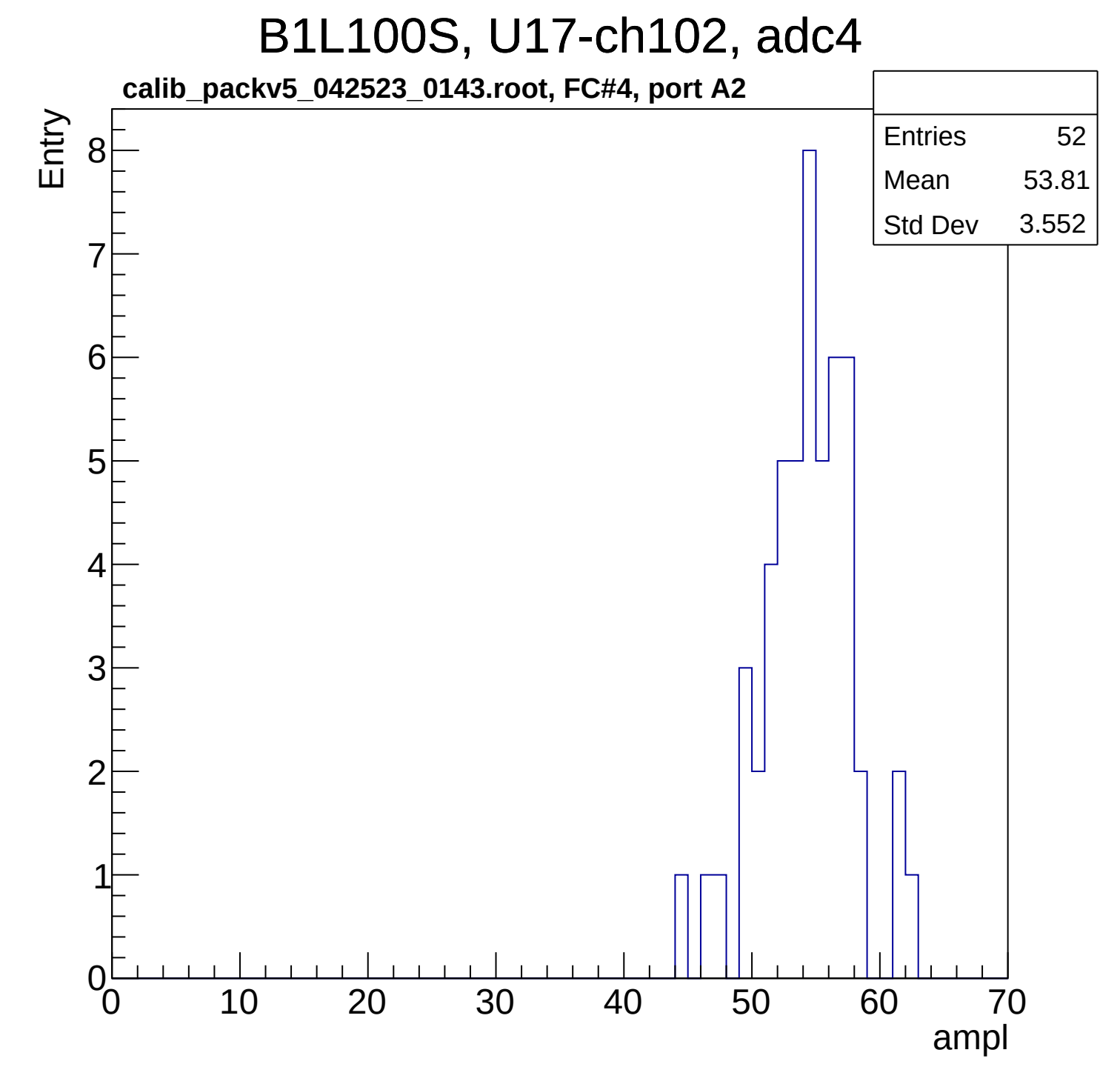

B1L100S, U17-ch101, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch102, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 26.7
Std Dev 5.783
Gaus mean : 27.6392
Gaus Width: 3.4699
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch102, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 33.88
Std Dev 3.363
Gaus mean : 33.7842
Gaus Width: 3.4458
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch102, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 40.53
Std Dev 3.154
Gaus mean : 40.8870
Gaus Width: 3.7058
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch102, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 76
Mean 47.95
Std Dev 3.62
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch102, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 52
Mean 53.81
Std Dev 3.552
Entry
ampl
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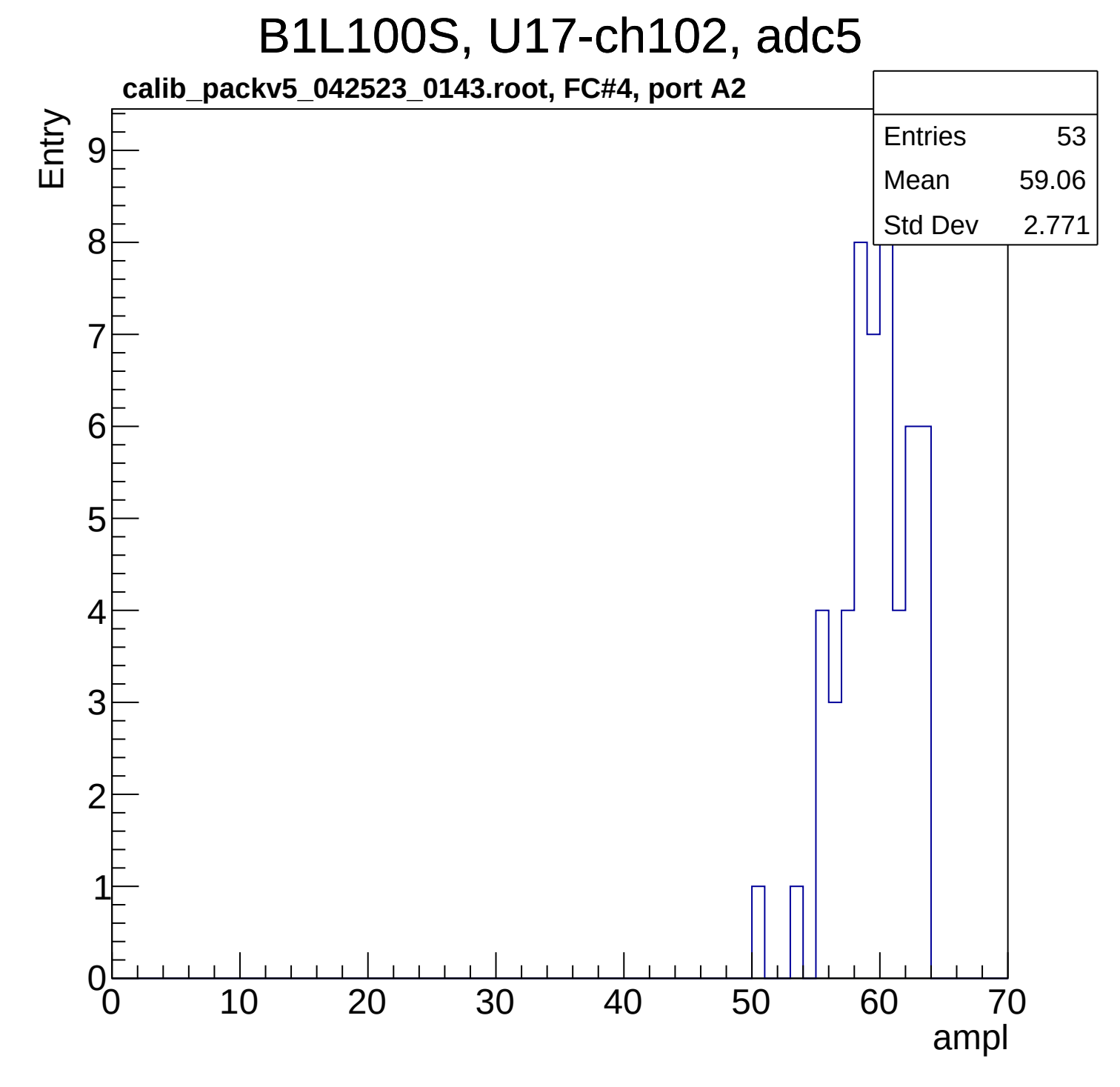
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch102, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 59.06
Std Dev 2.771
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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60
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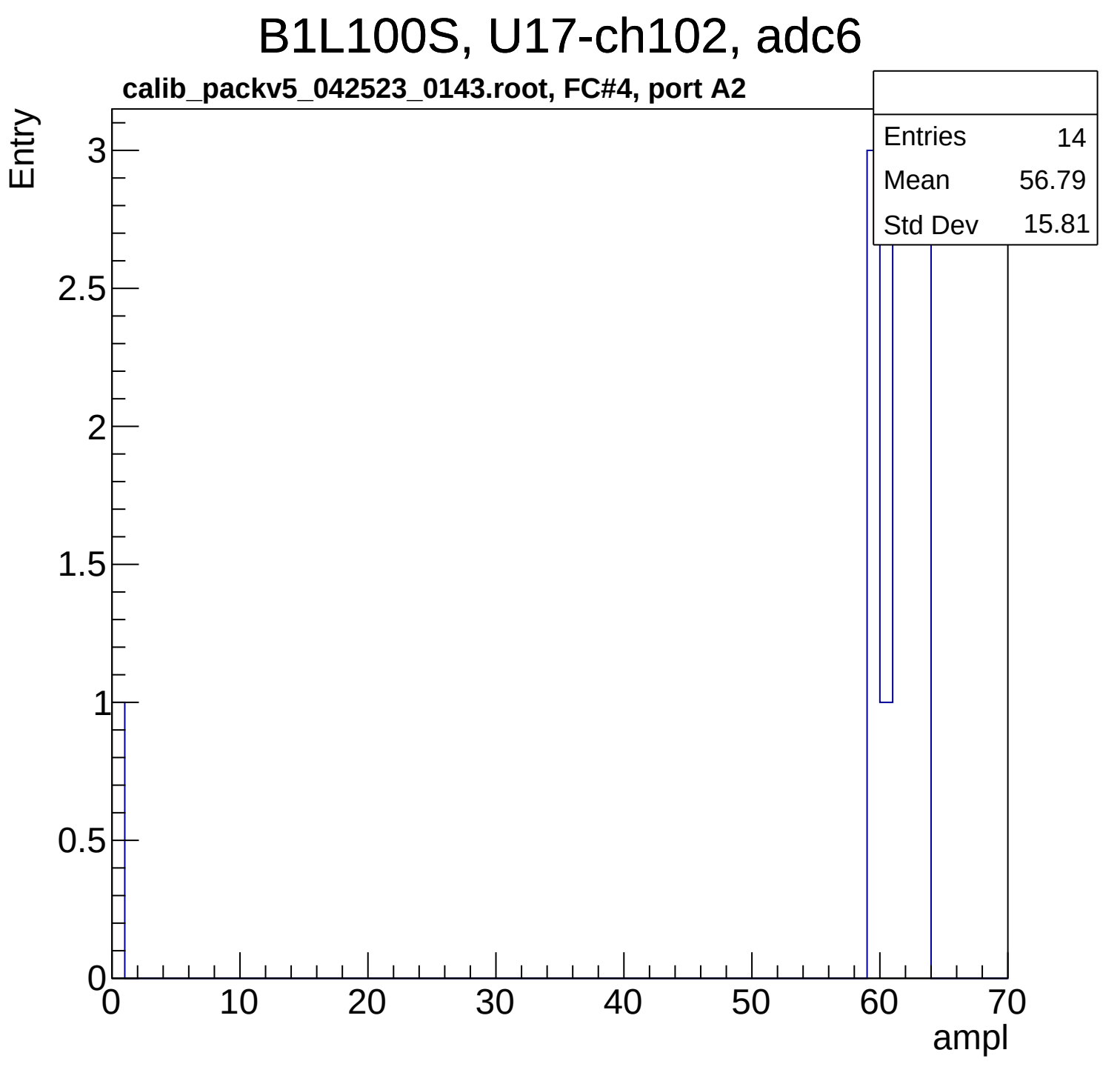
B1L100S, U17-ch102, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 14
Mean 56.79
Std Dev 15.81
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
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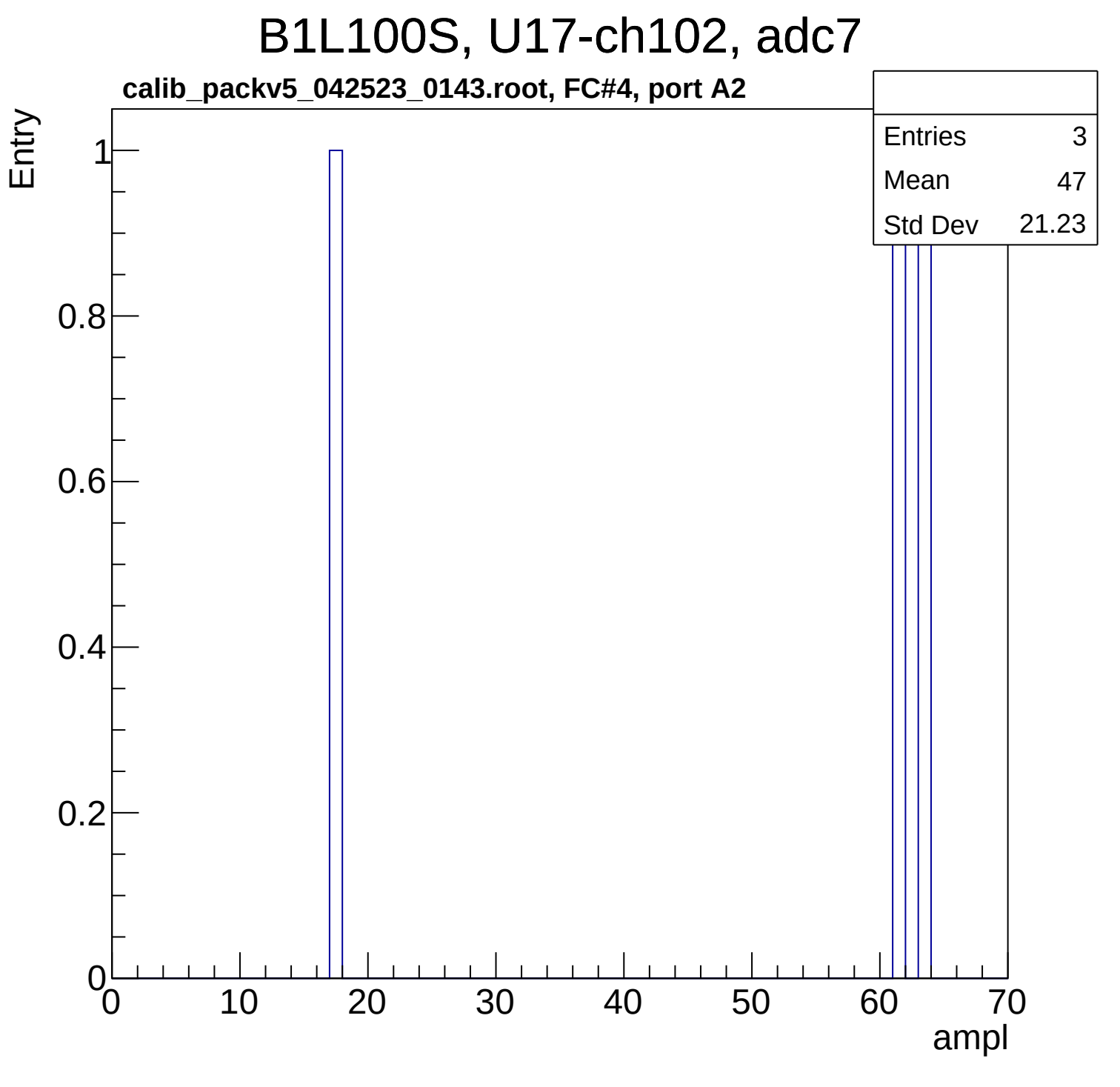
40
50
60
70


B1L100S, U17-ch102, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 47
Std Dev 21.23
Entry
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0.6
0.4
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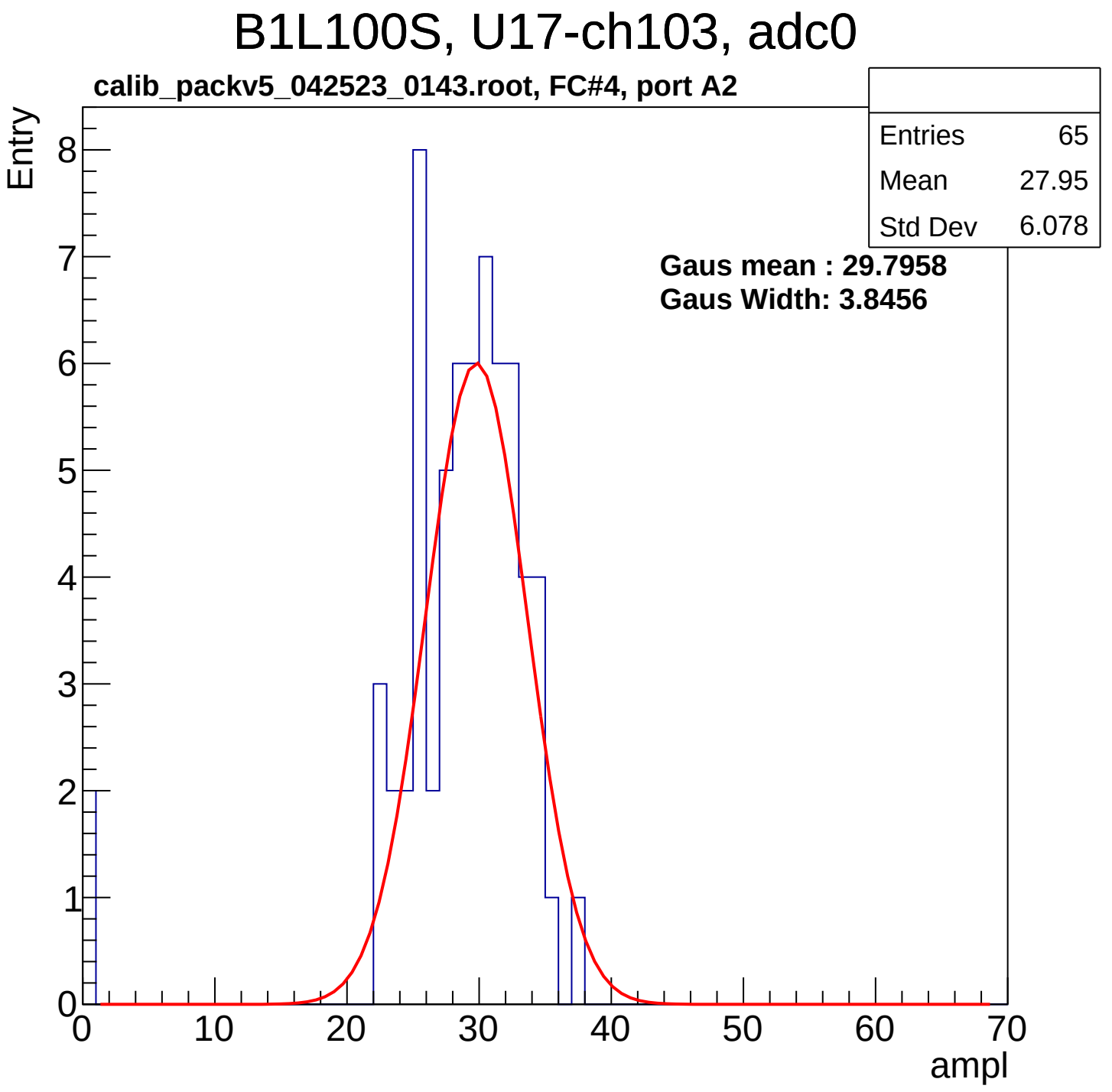
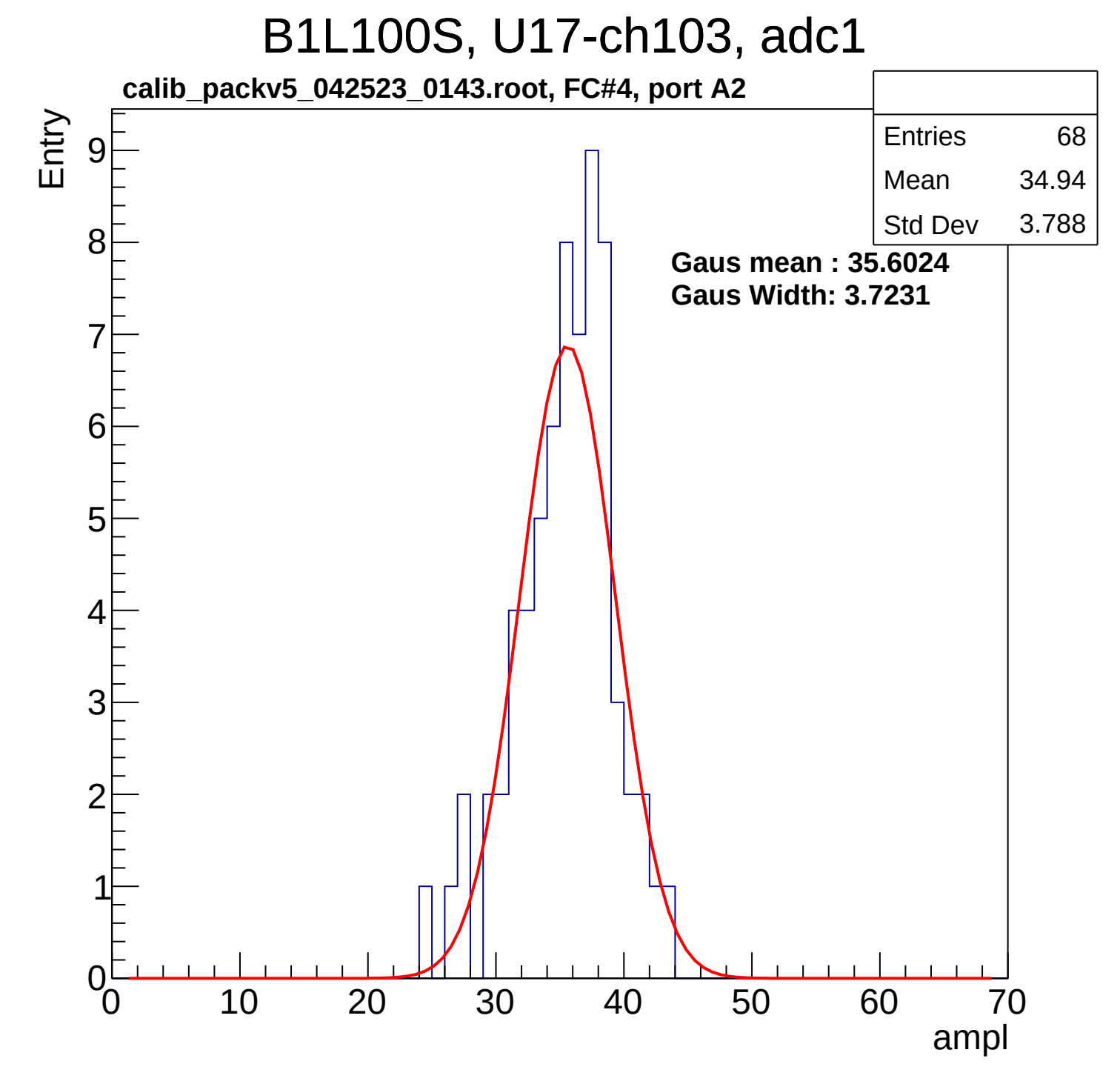
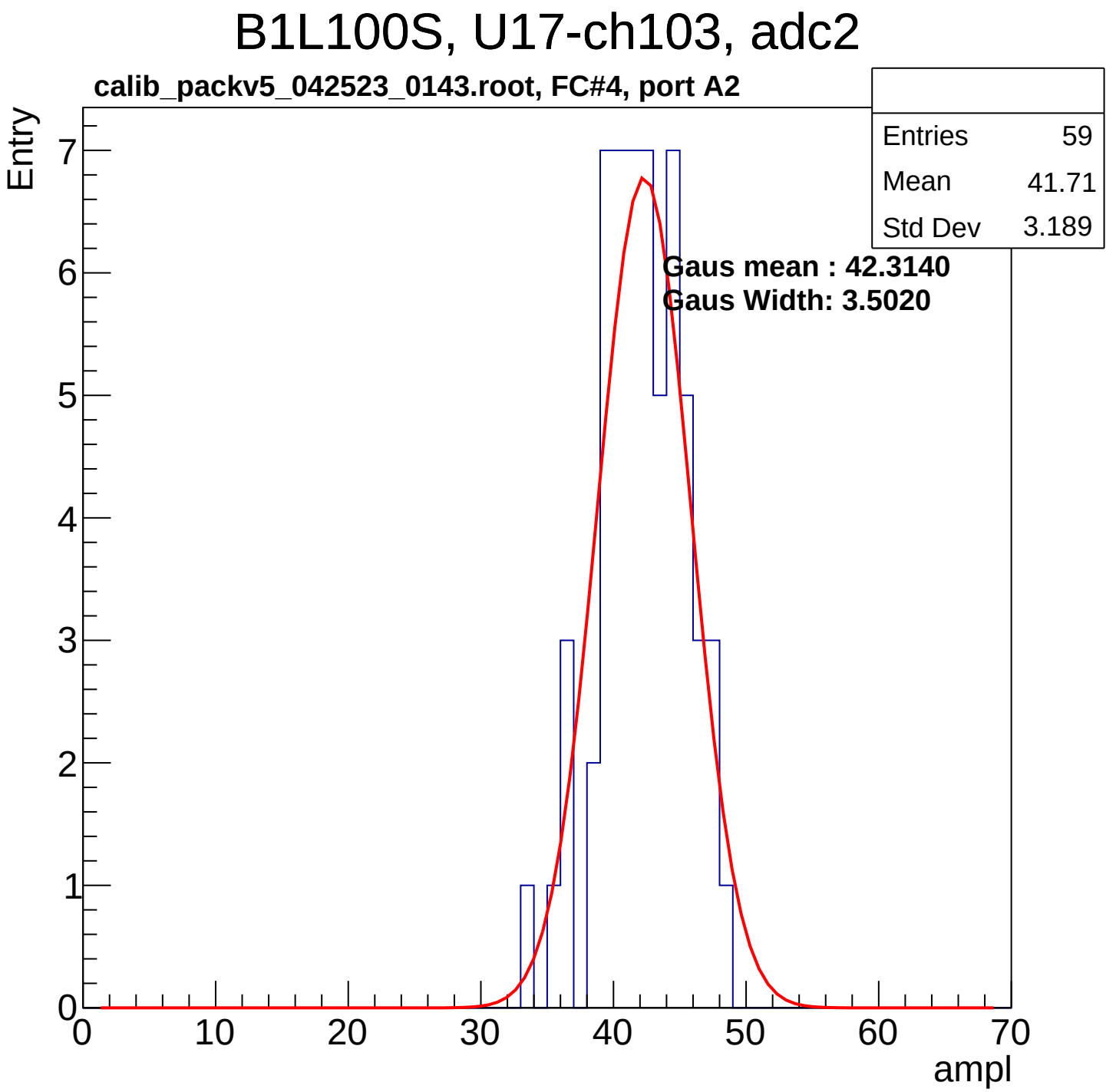
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch103, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 27.95
Std Dev 6.078
Gaus mean : 29.7958
Gaus Width: 3.8456
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch103, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 34.94
Std Dev 3.788
Gaus mean : 35.6024
Gaus Width: 3.7231
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch103, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 41.71
Std Dev 3.189
Gaus mean : 42.3140
Gaus Width: 3.5020
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
50
60
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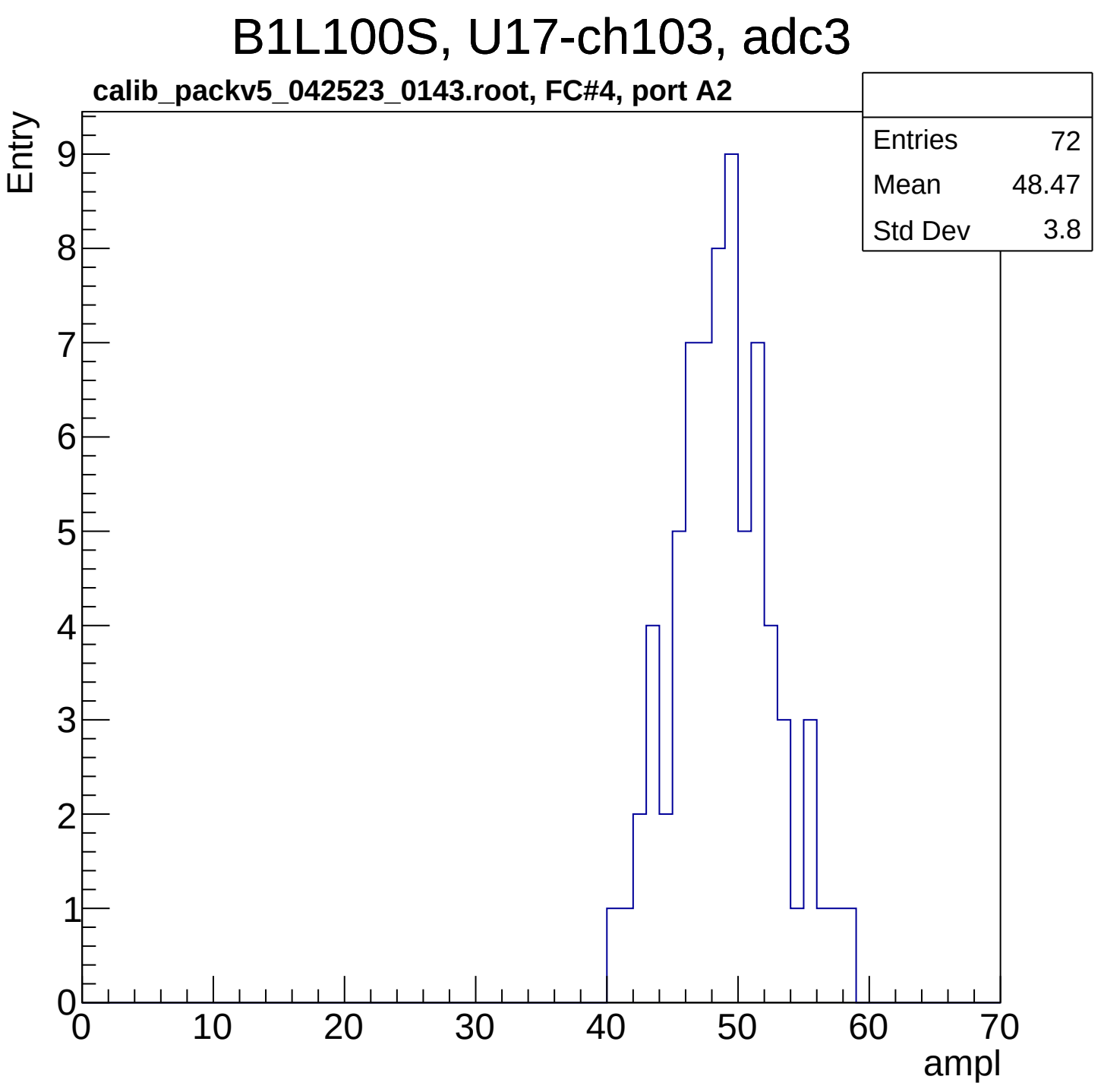
B1L100S, U17-ch103, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 48.47
Std Dev 3.8
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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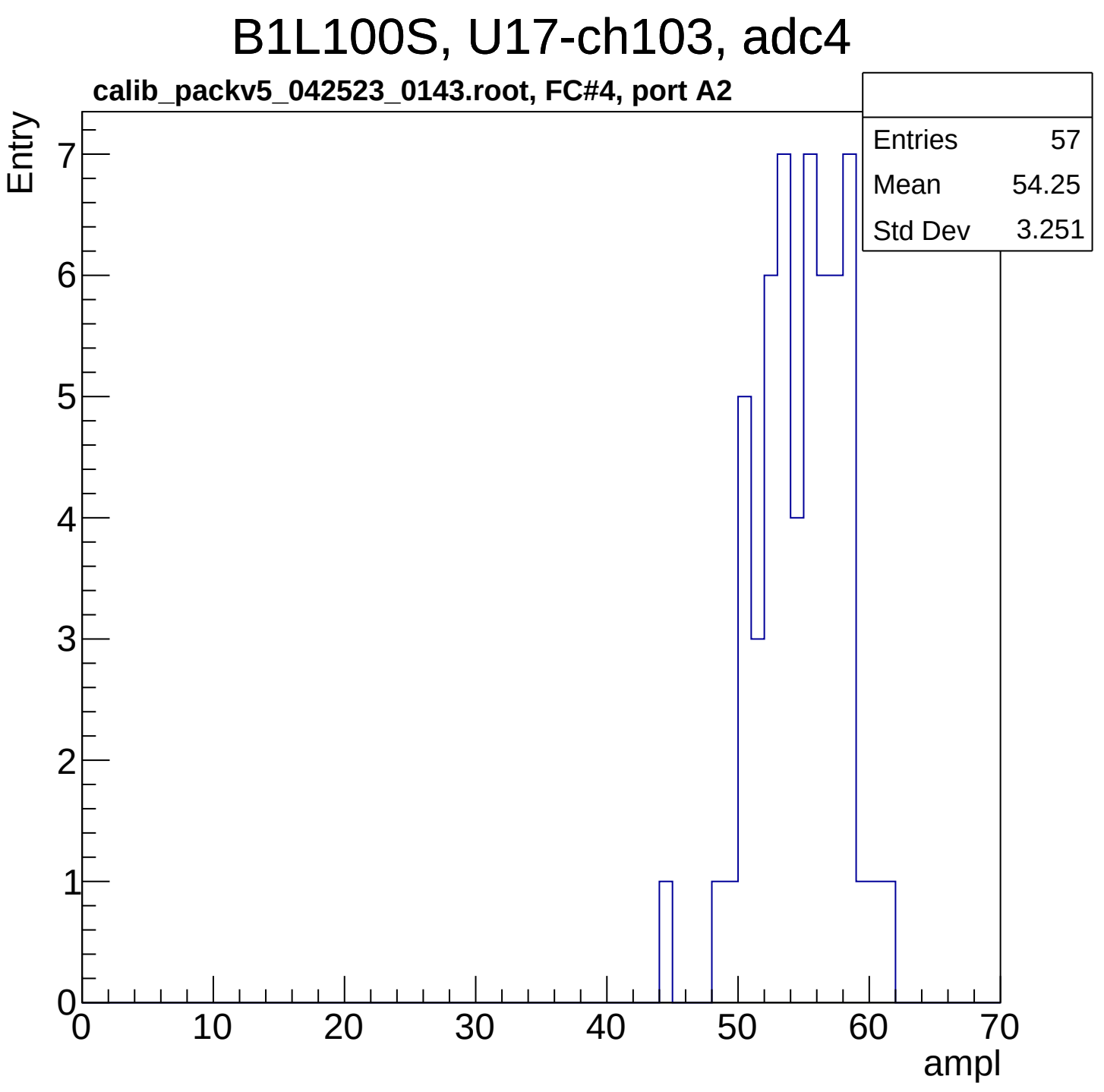
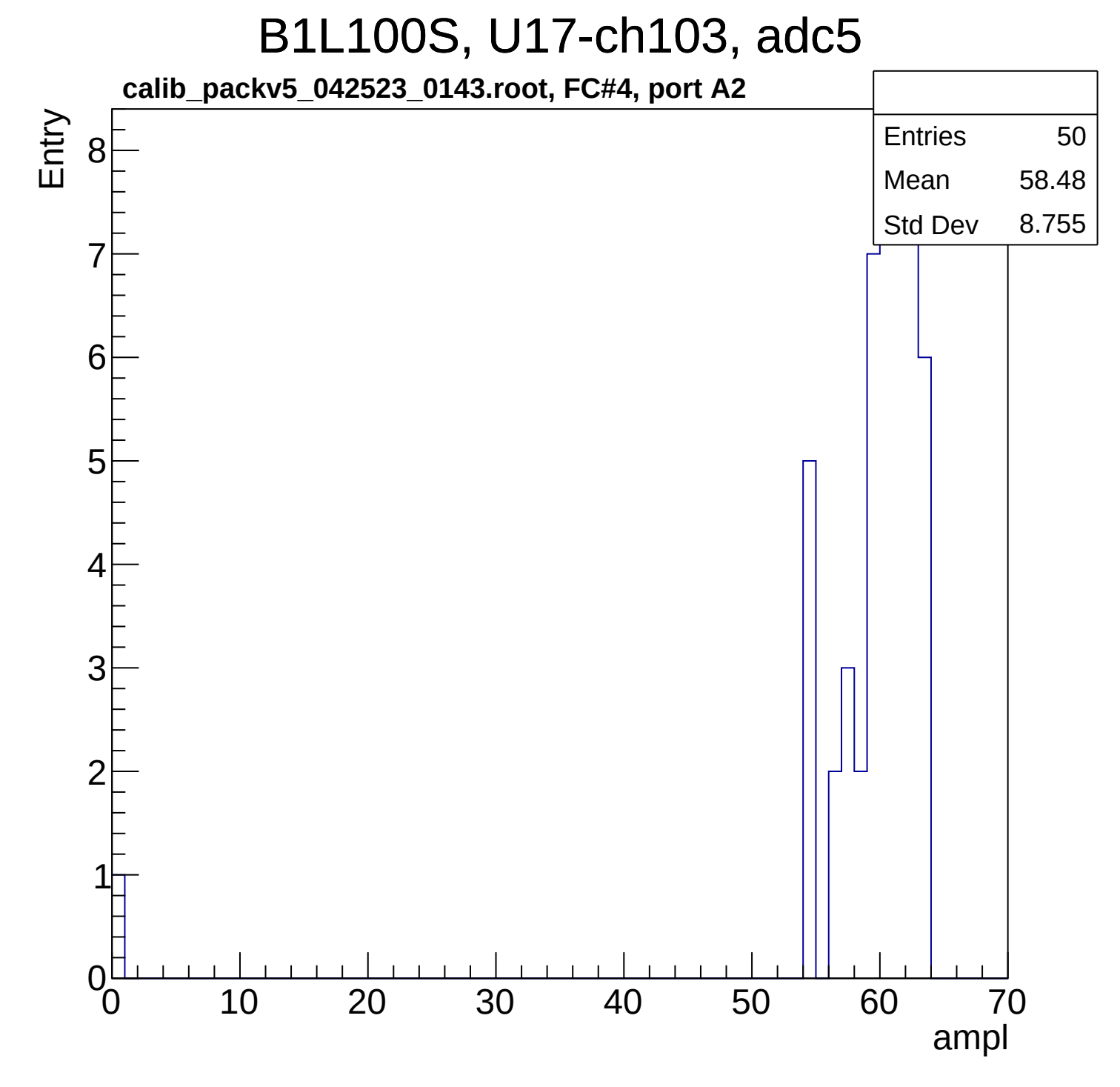
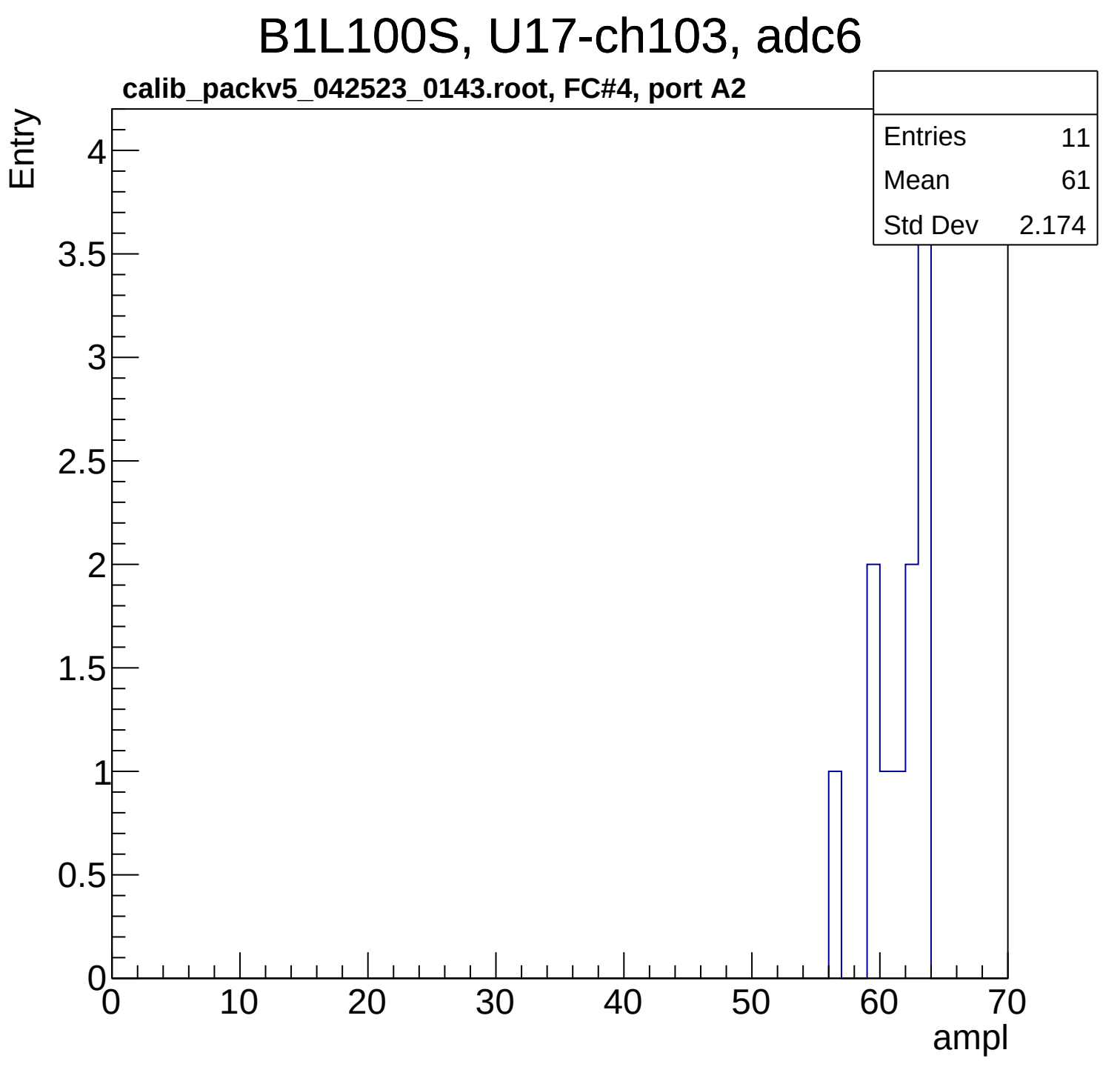

B1L100S, U17-ch103, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 54.25
Std Dev 3.251
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U17-ch103, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 58.48
Std Dev 8.755
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch103, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 11
Mean 61
Std Dev 2.174
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
10
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60
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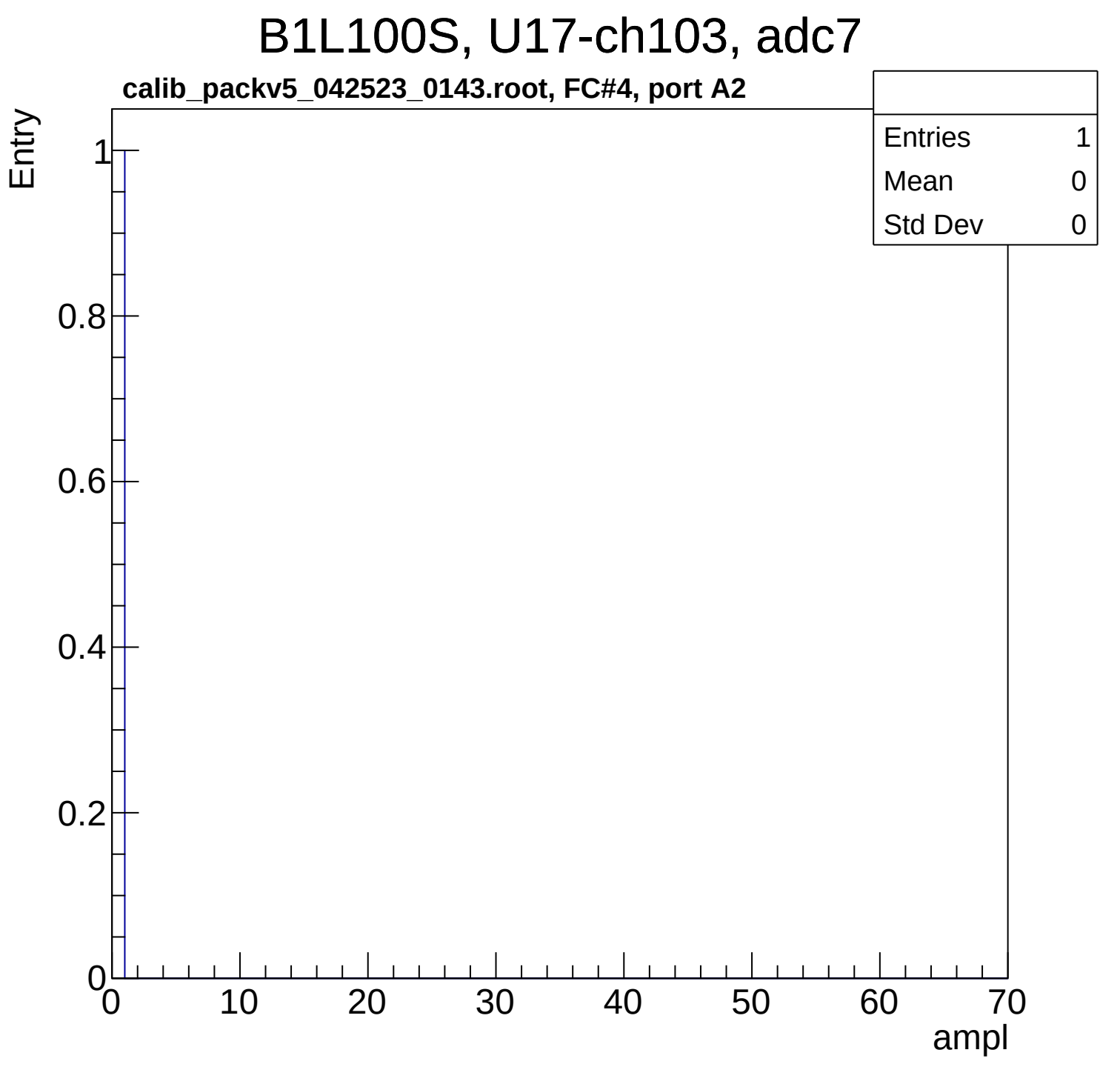
B1L100S, U17-ch103, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
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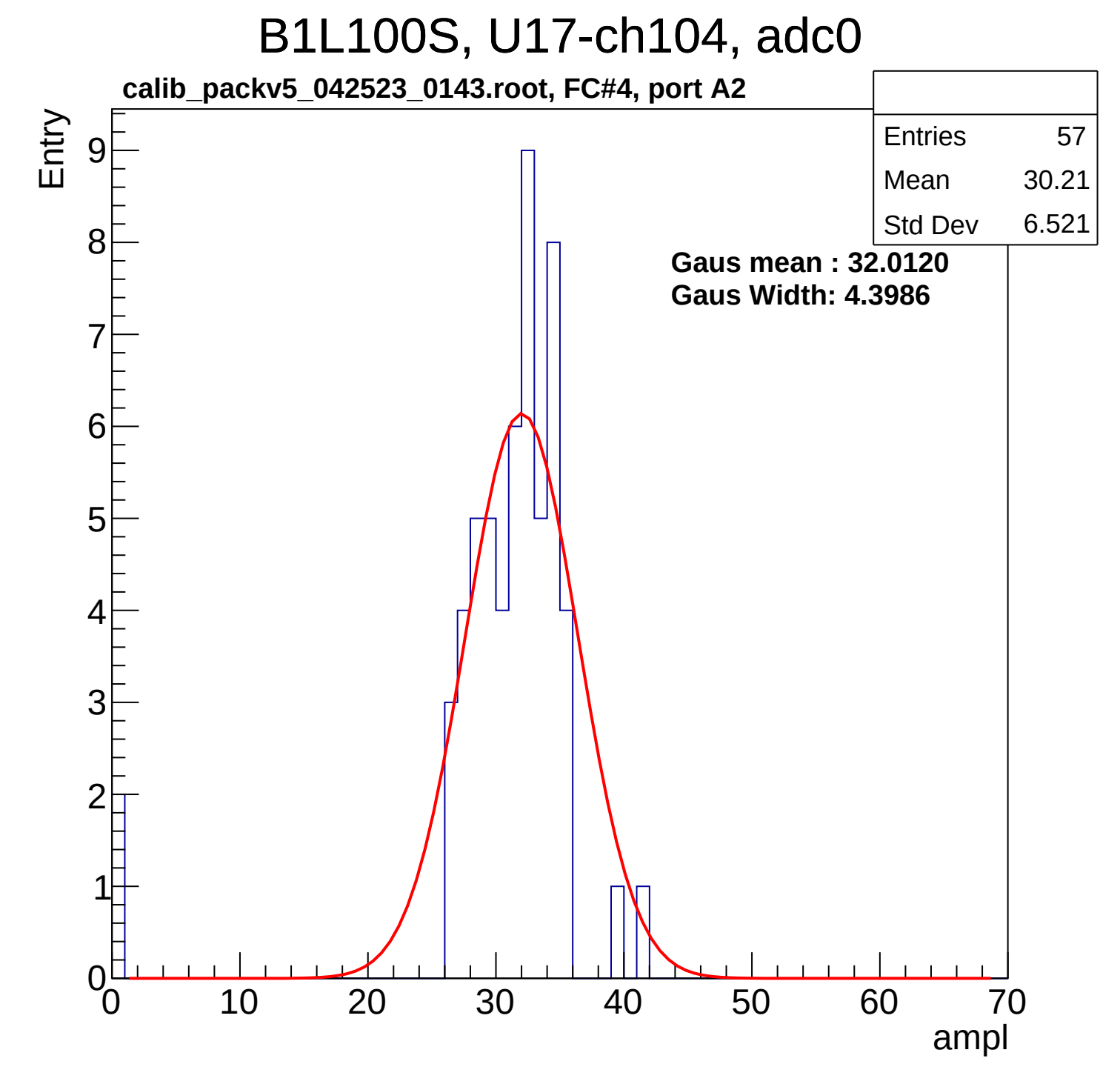
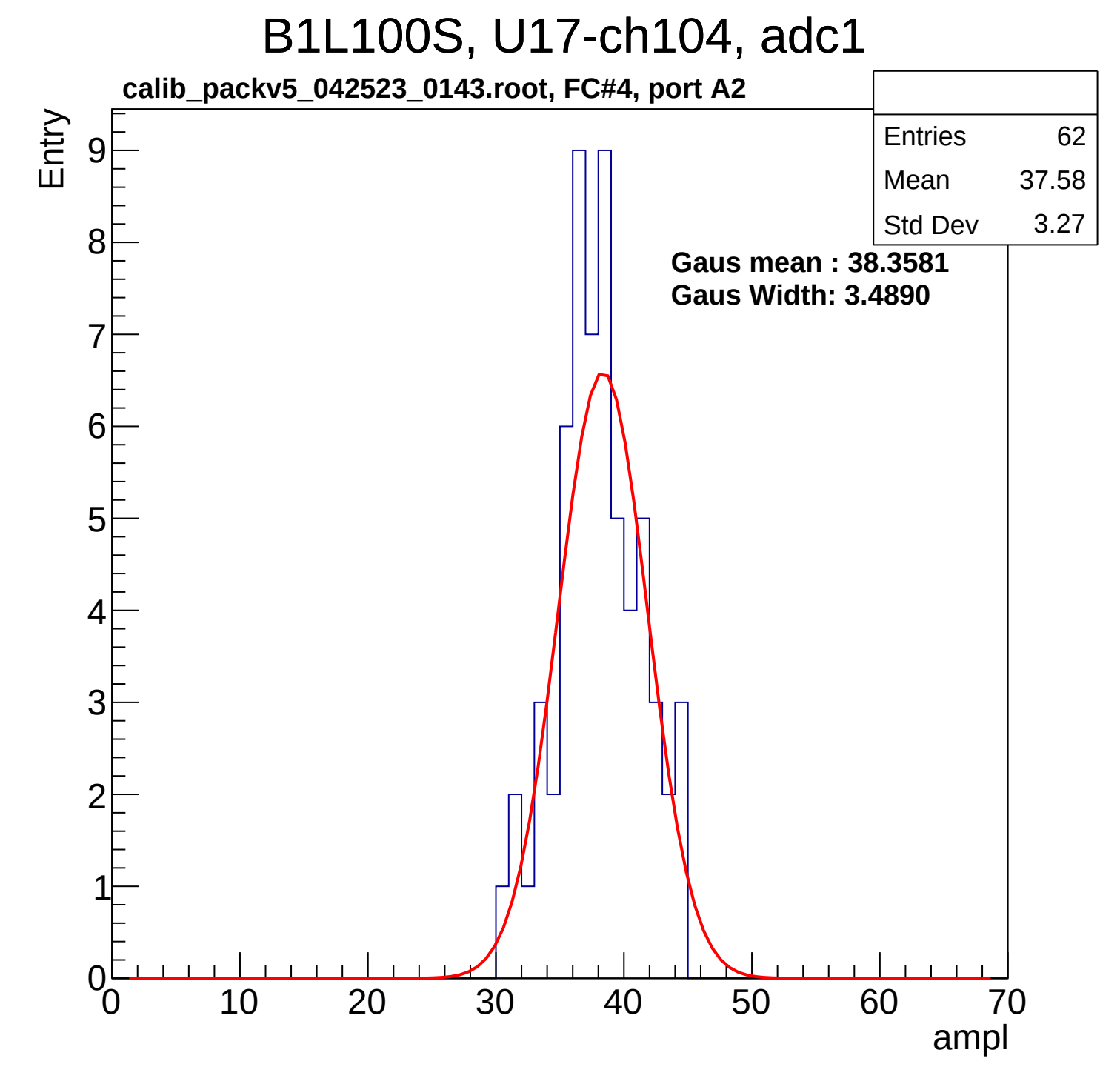
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch104, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 30.21
Std Dev 6.521
Gaus mean : 32.0120
Gaus Width: 4.3986
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch104, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 37.58
Std Dev 3.27
Gaus mean : 38.3581
Gaus Width: 3.4890
Entry
ampl
0
1
2
3
4
5
6
7
8
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0
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40
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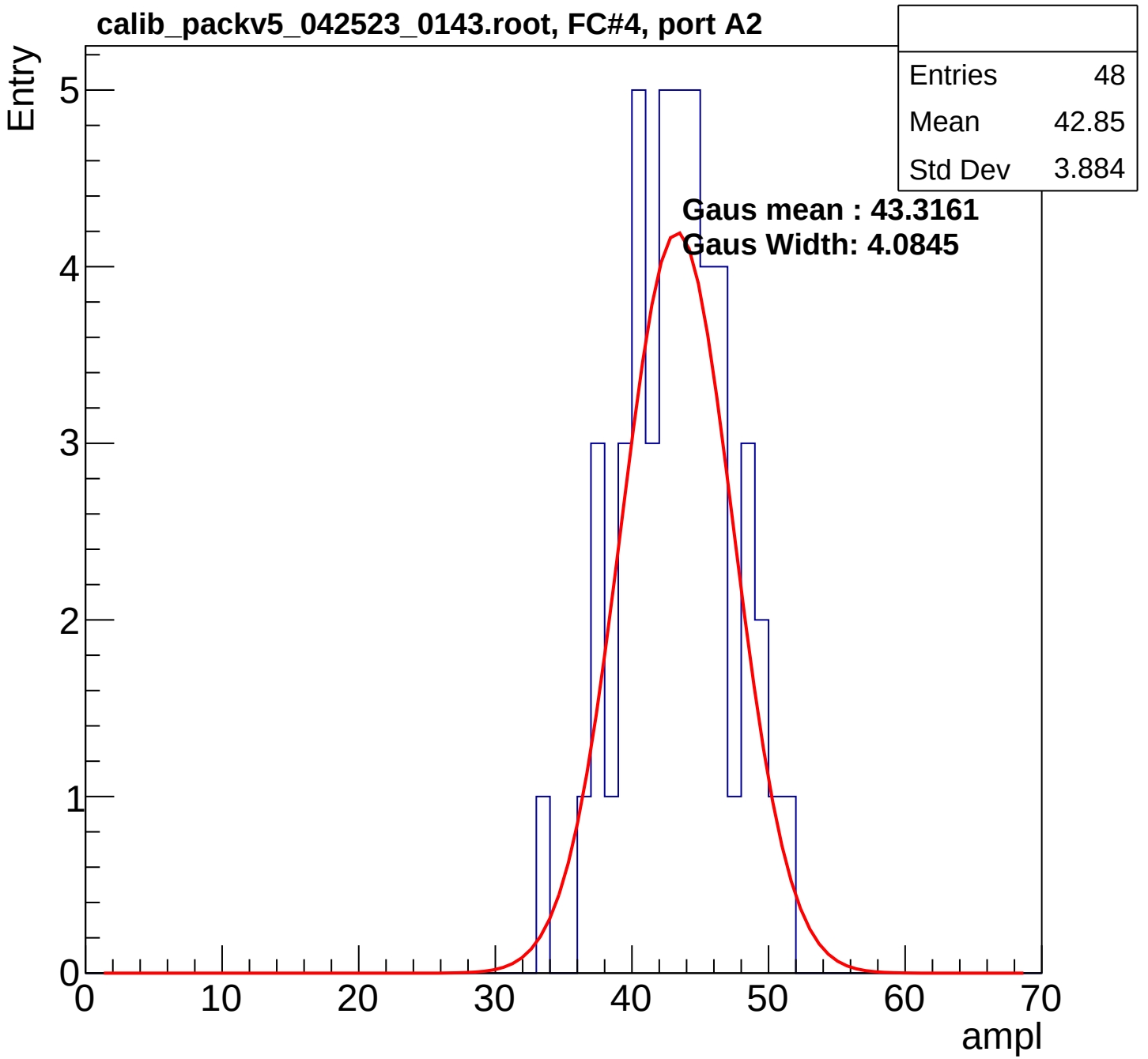
B1L100S, U17-ch104, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 48
Mean 42.85
Std Dev 3.884
Gaus mean : 43.3161
Gaus Width: 4.0845
Entry
ampl
0
1
2
3
4
5
0
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20
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40
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60
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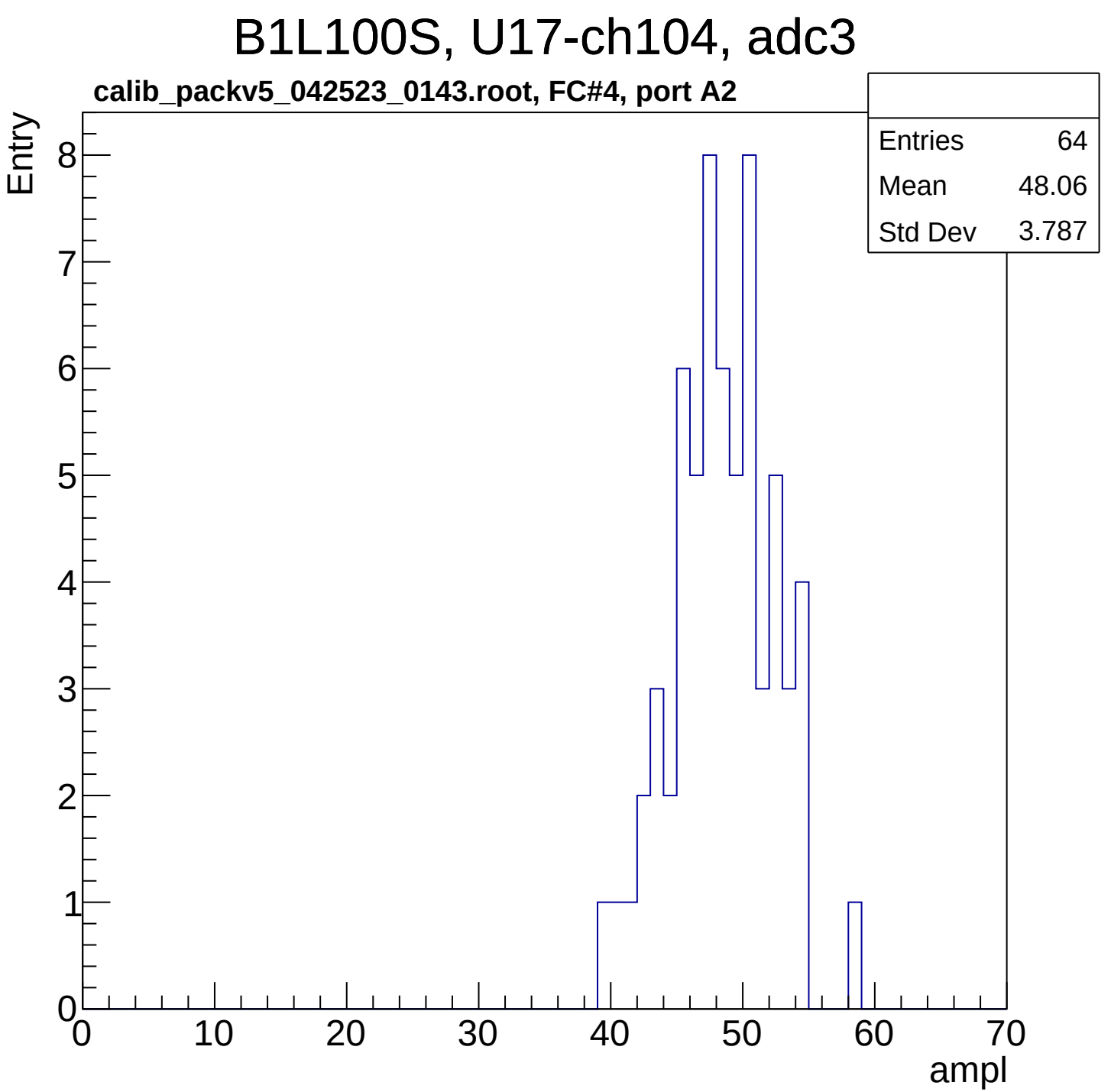
B1L100S, U17-ch104, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 48.06
Std Dev 3.787
Entry
ampl
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1
2
3
4
5
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0
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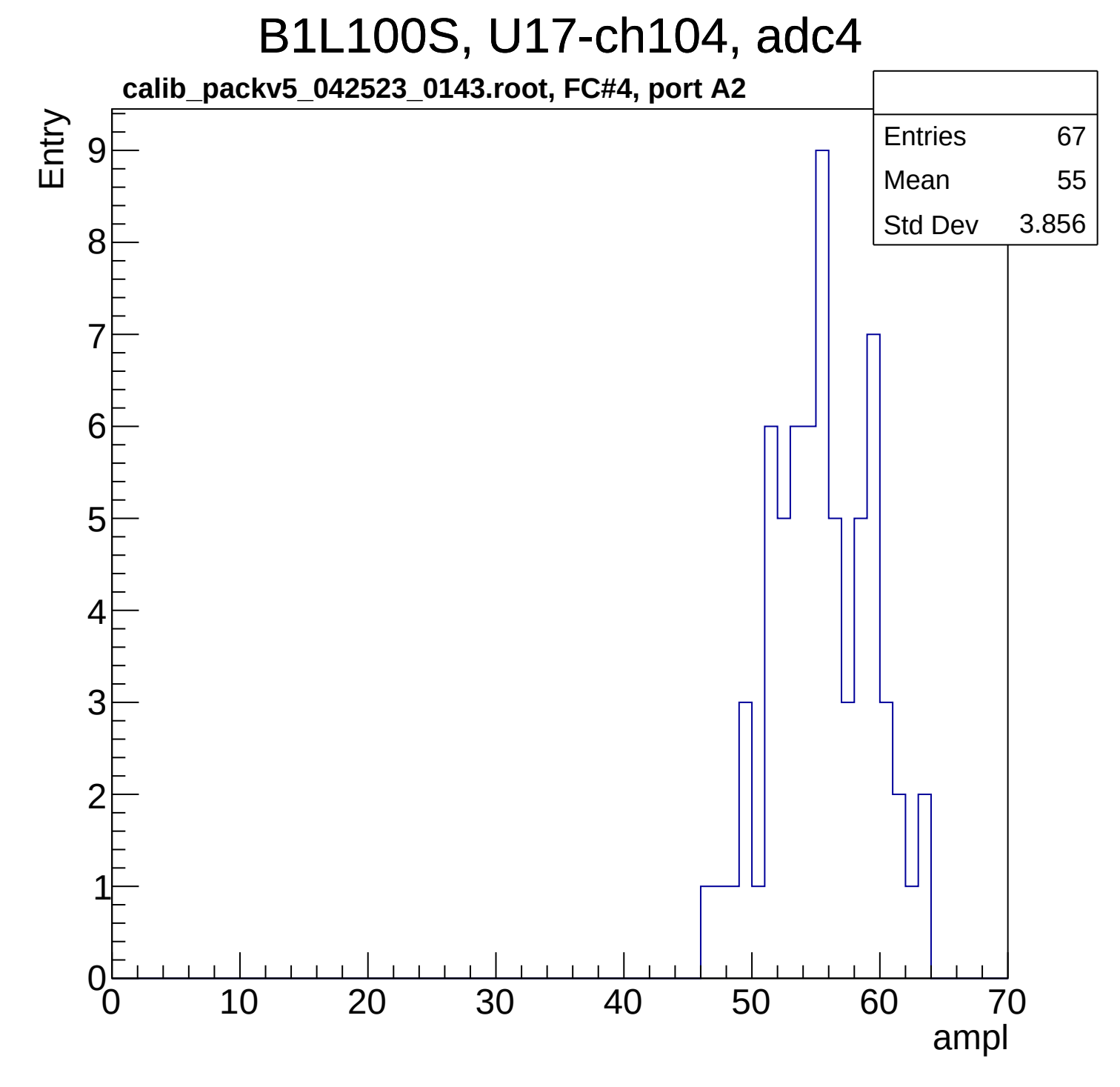
B1L100S, U17-ch104, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 55
Std Dev 3.856
Entry
ampl
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2
3
4
5
6
7
8
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0
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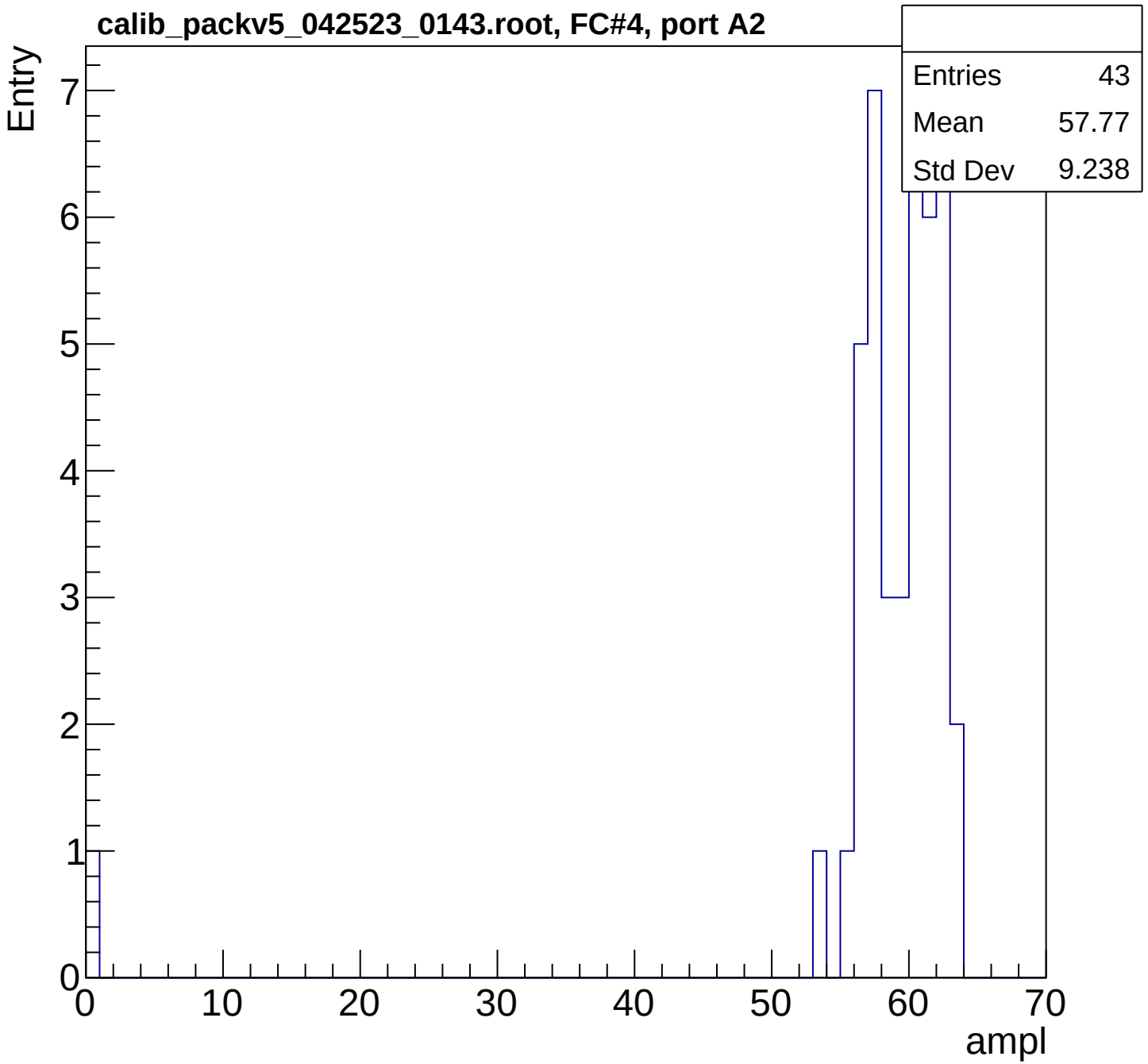
B1L100S, U17-ch104, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 43
Mean 57.77
Std Dev 9.238
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
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60
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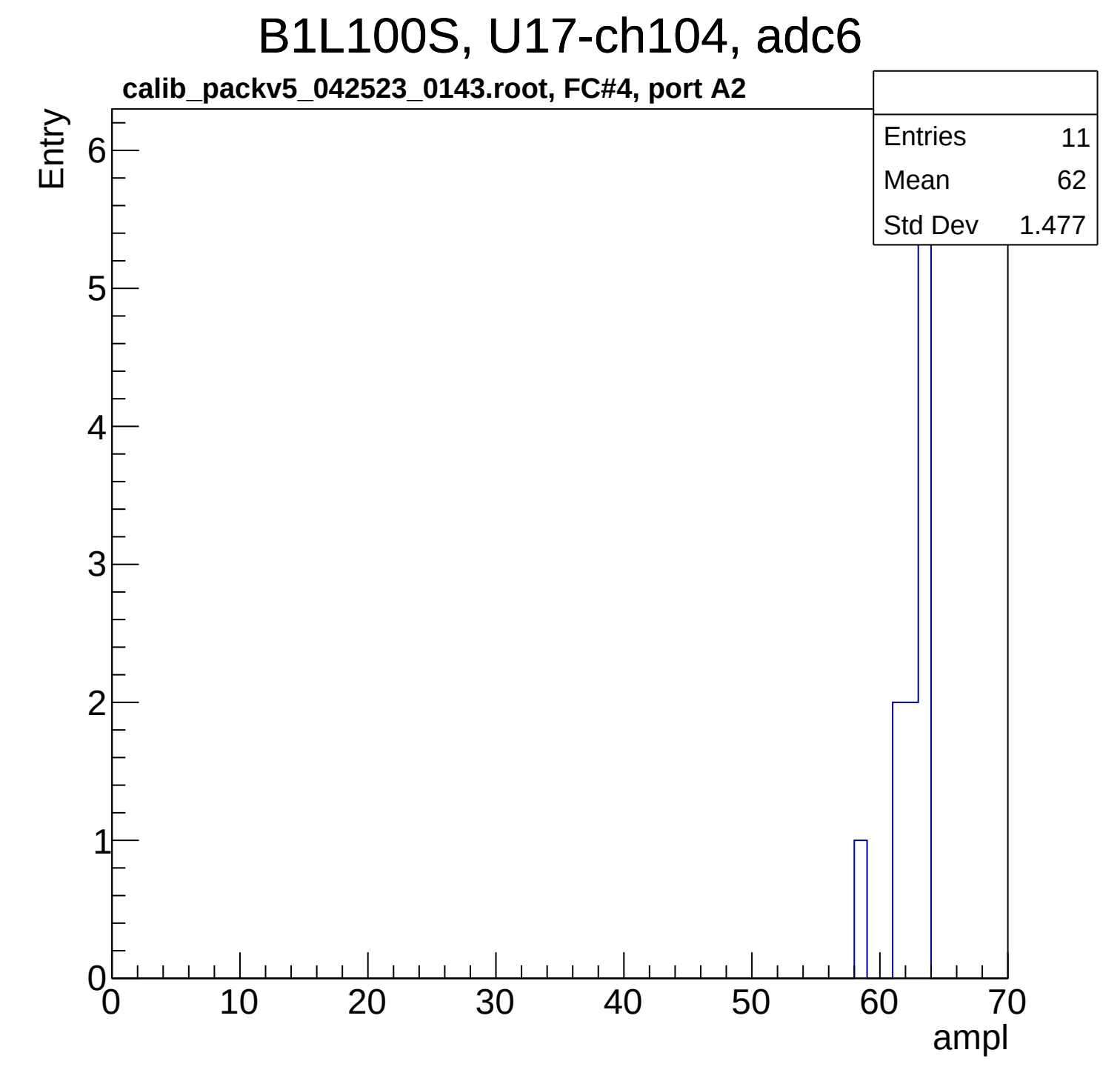
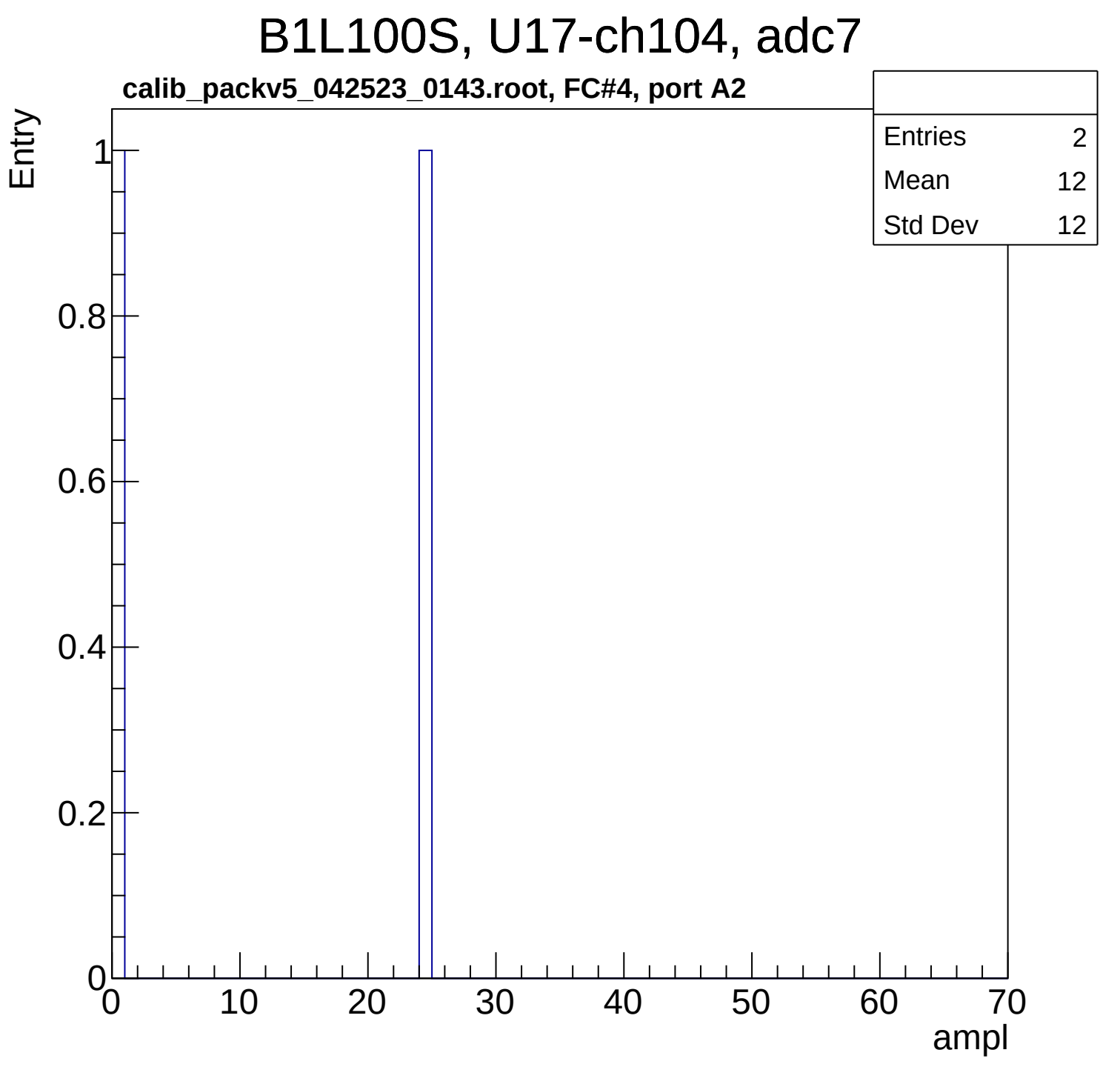
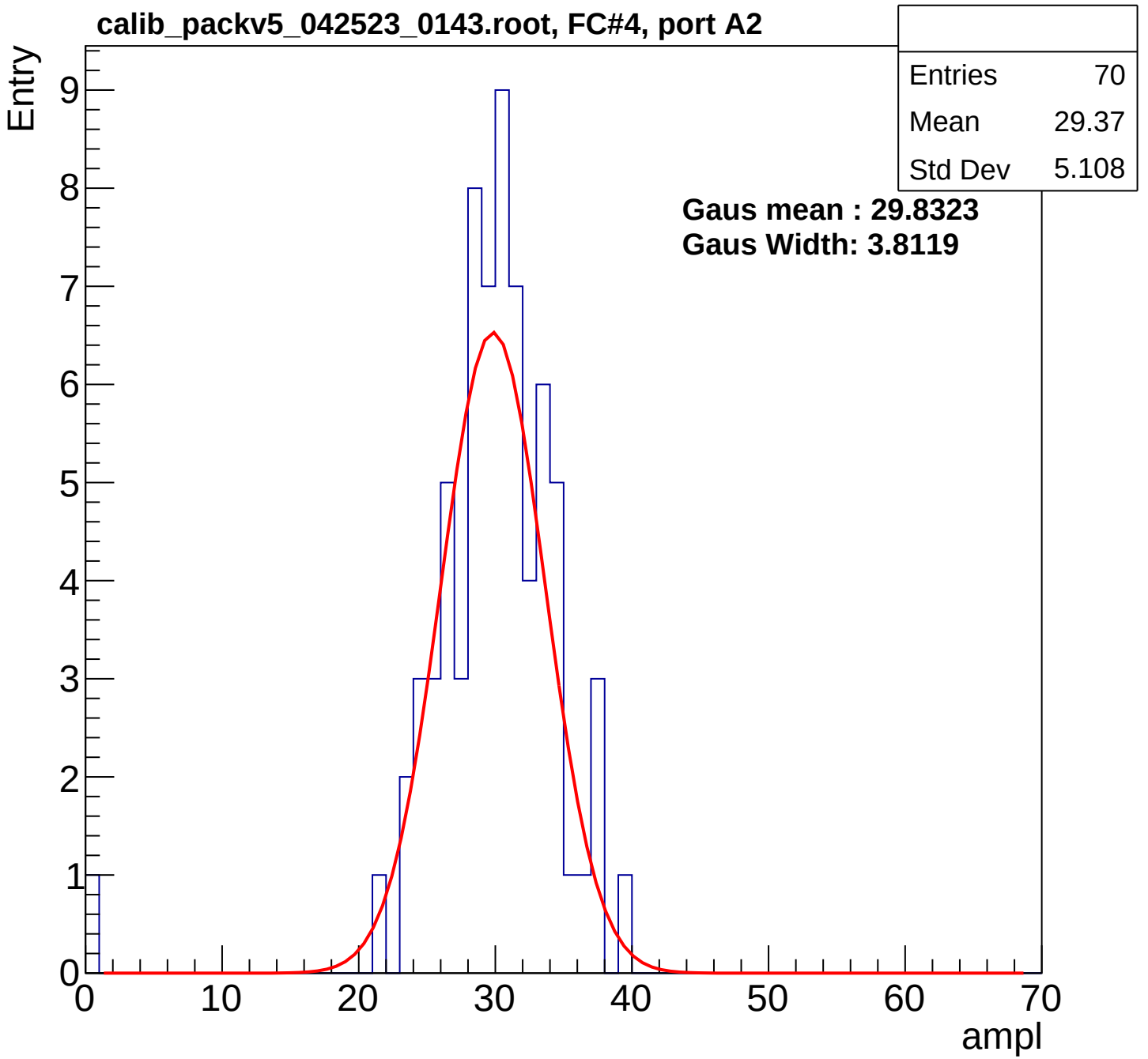

B1L100S, U17-ch104, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 11
Mean 62
Std Dev 1.477
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch104, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 12
Std Dev 12
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch105, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 29.37
Std Dev 5.108
Gaus mean : 29.8323
Gaus Width: 3.8119
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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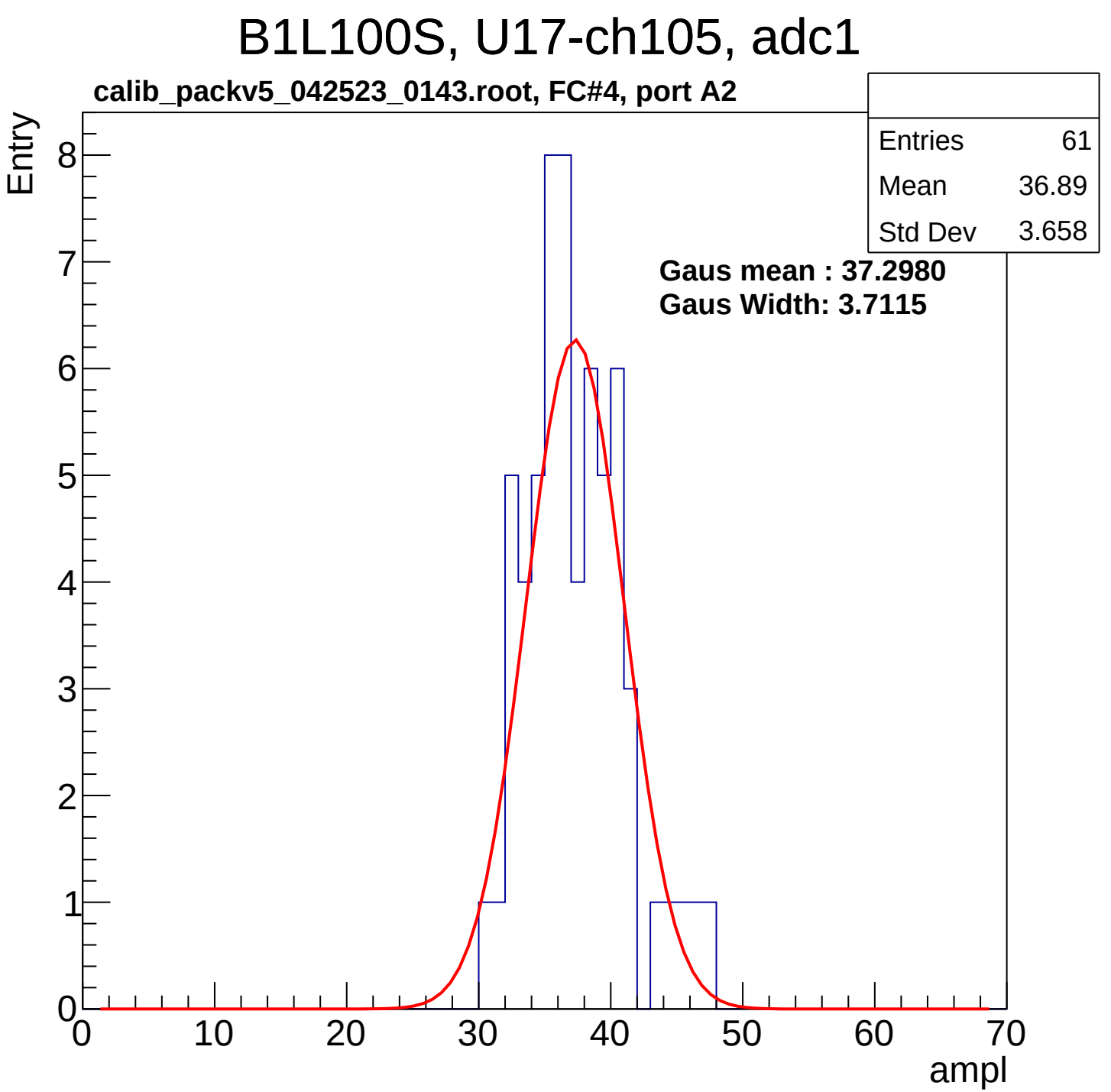
B1L100S, U17-ch105, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 36.89
Std Dev 3.658
Gaus mean : 37.2980
Gaus Width: 3.7115
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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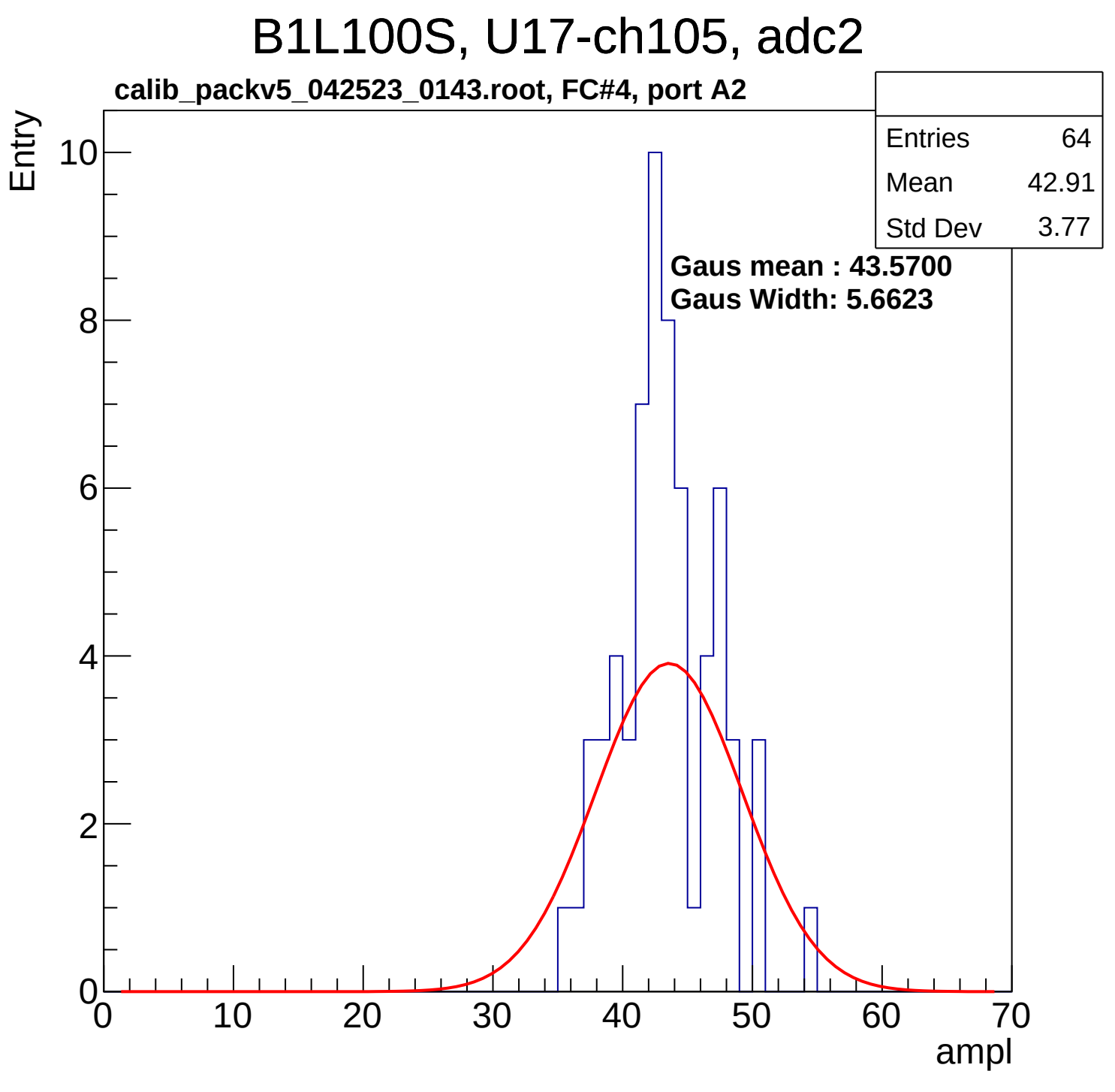
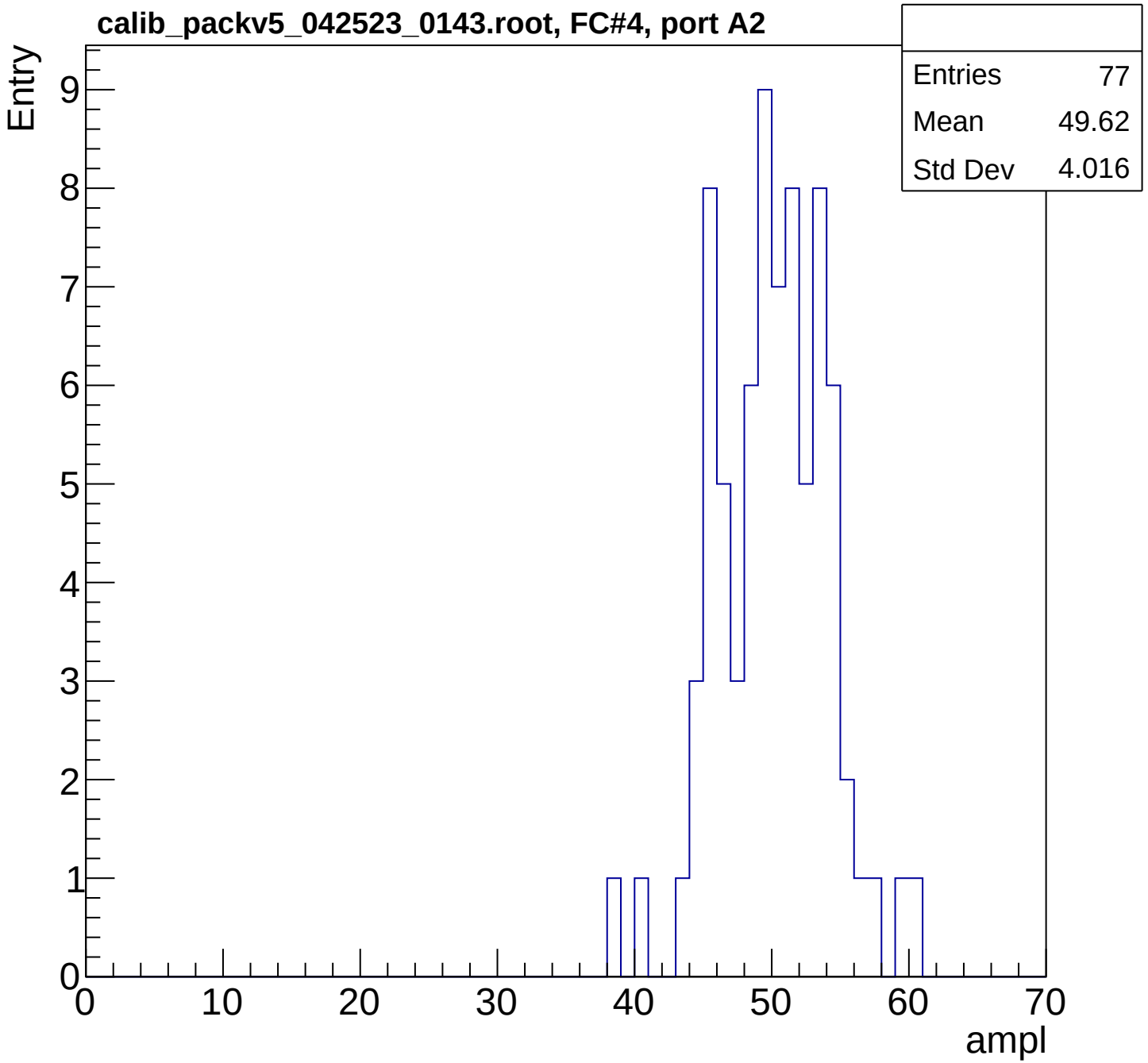

B1L100S, U17-ch105, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 42.91
Std Dev 3.77
Gaus mean : 43.5700
Gaus Width: 5.6623
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U17-ch105, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 77
Mean 49.62
Std Dev 4.016
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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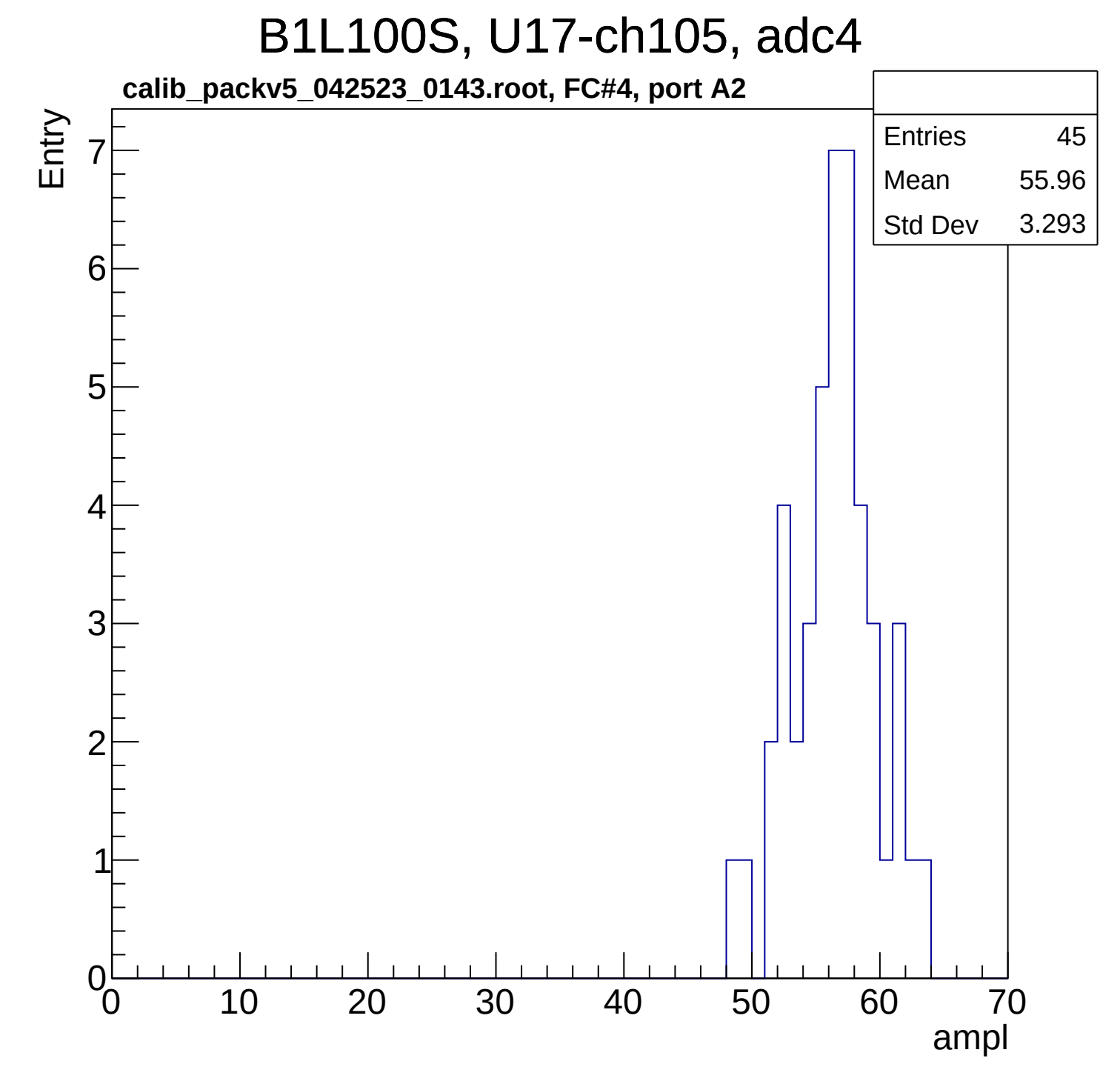
B1L100S, U17-ch105, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 45
Mean 55.96
Std Dev 3.293
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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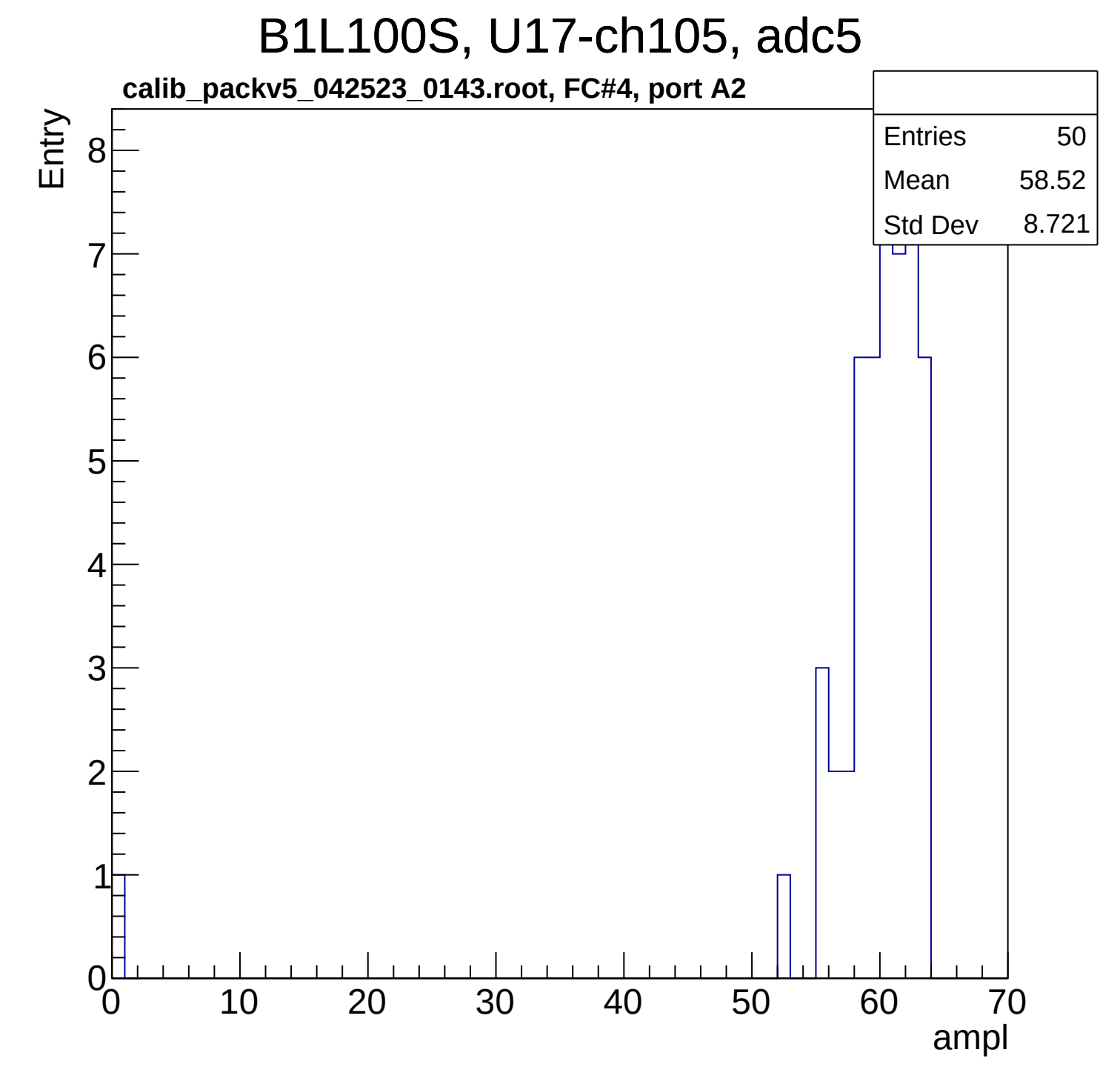
B1L100S, U17-ch105, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 58.52
Std Dev 8.721
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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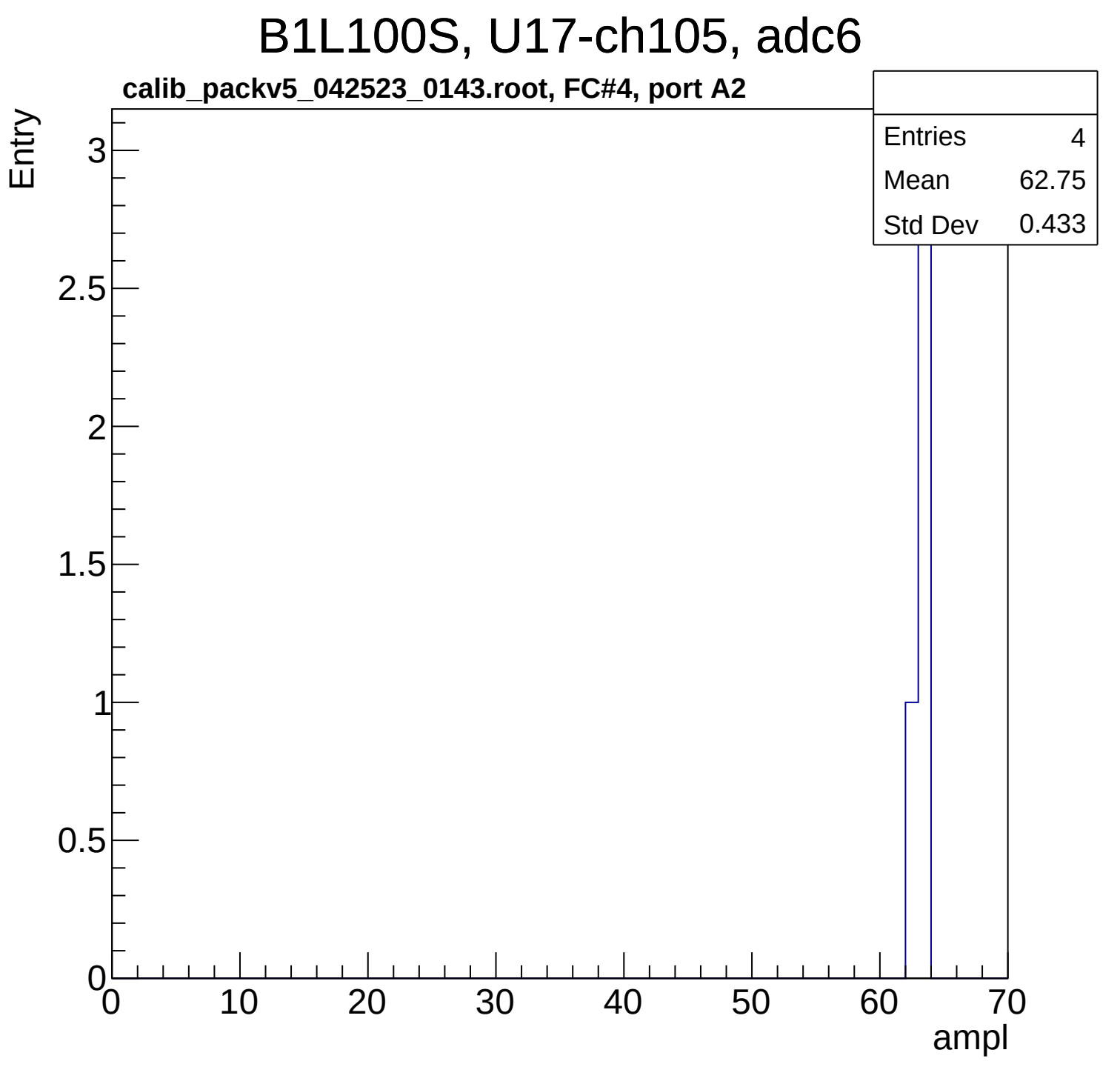
B1L100S, U17-ch105, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 4
Mean 62.75
Std Dev 0.433
Entry
ampl
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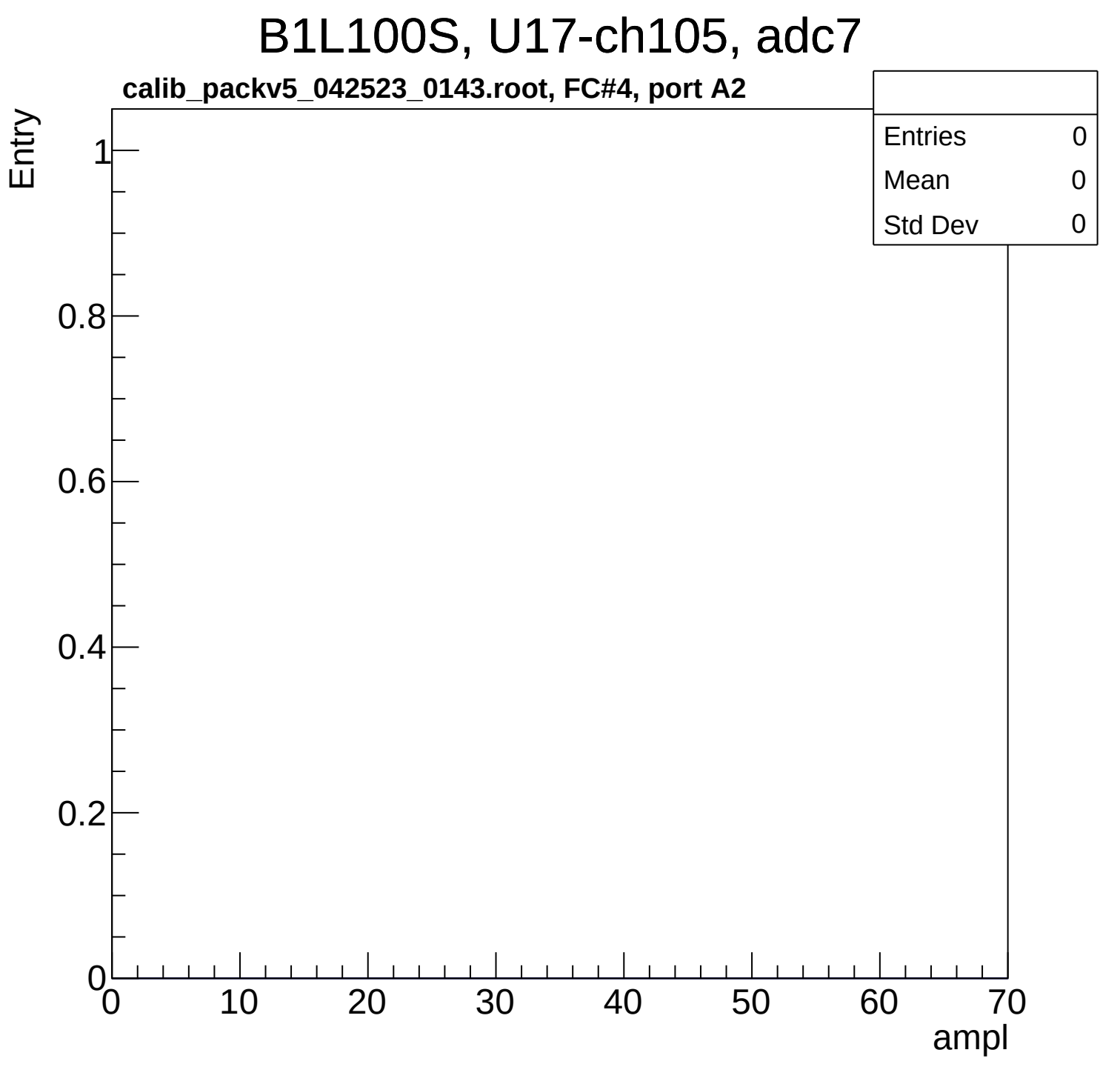
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L100S, U17-ch105, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
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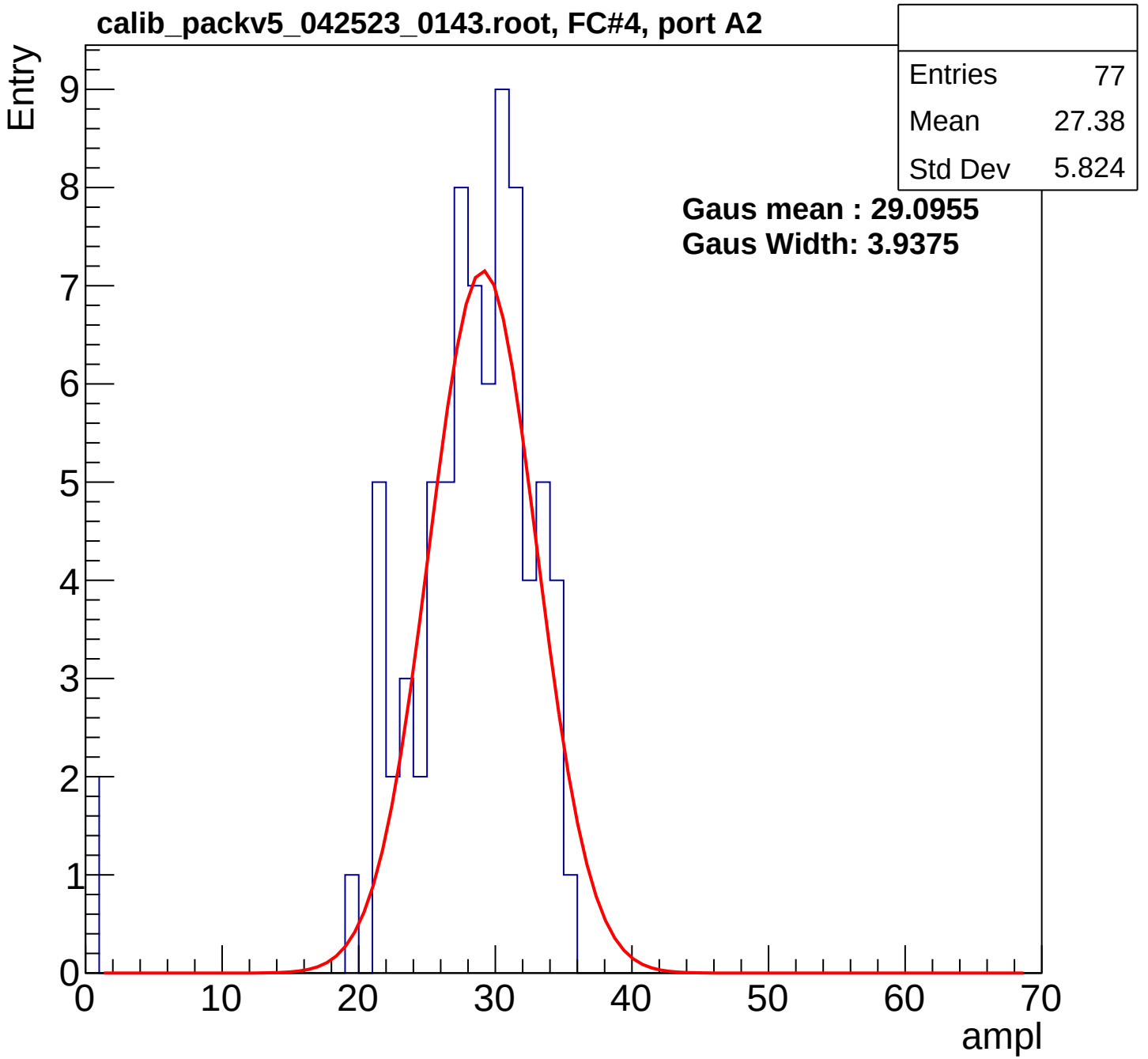
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch106, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 77
Mean 27.38
Std Dev 5.824
Gaus mean : 29.0955
Gaus Width: 3.9375
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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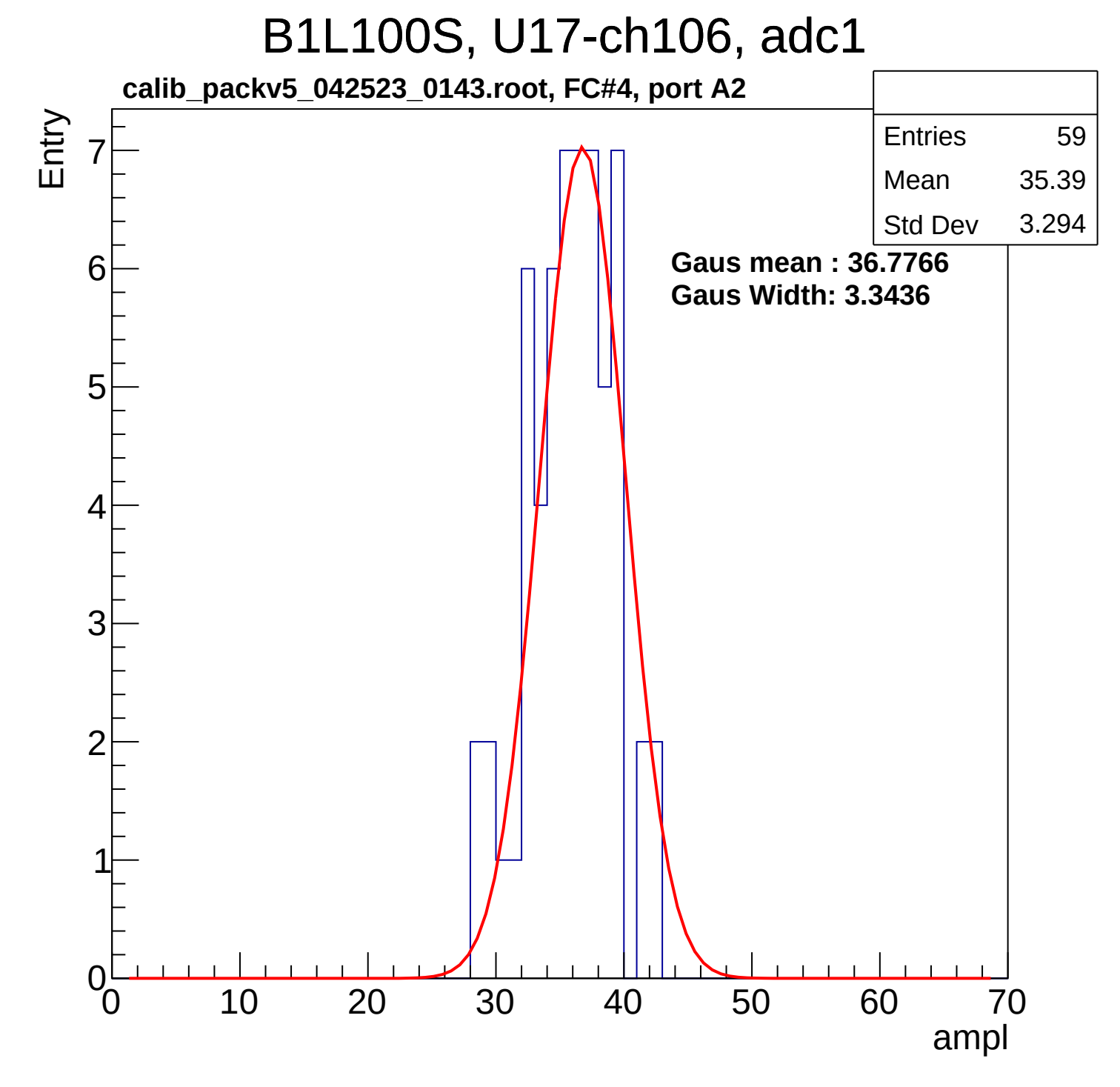
B1L100S, U17-ch106, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 35.39
Std Dev 3.294
Gaus mean : 36.7766
Gaus Width: 3.3436
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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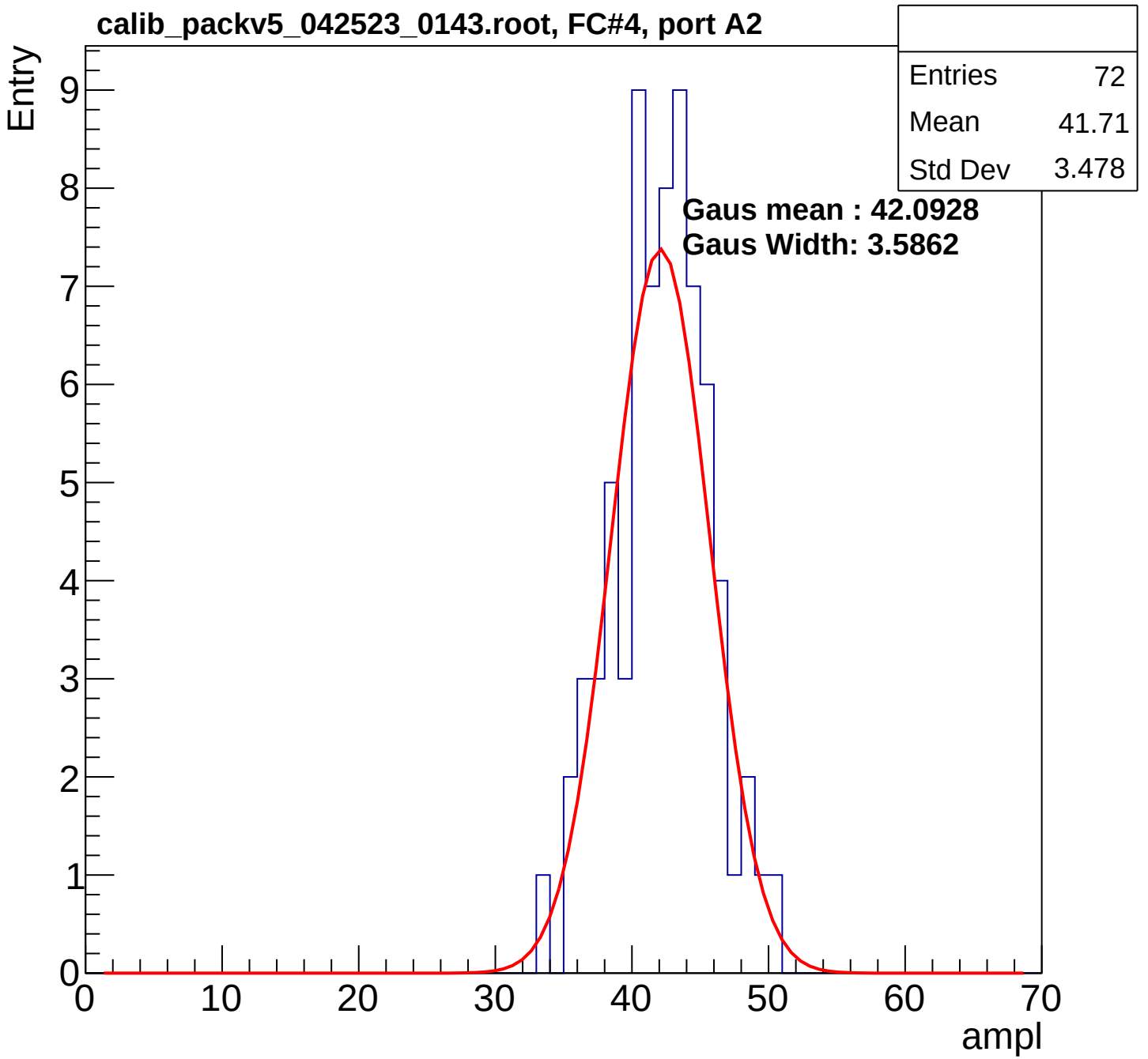
B1L100S, U17-ch106, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 41.71
Std Dev 3.478
Gaus mean : 42.0928
Gaus Width: 3.5862
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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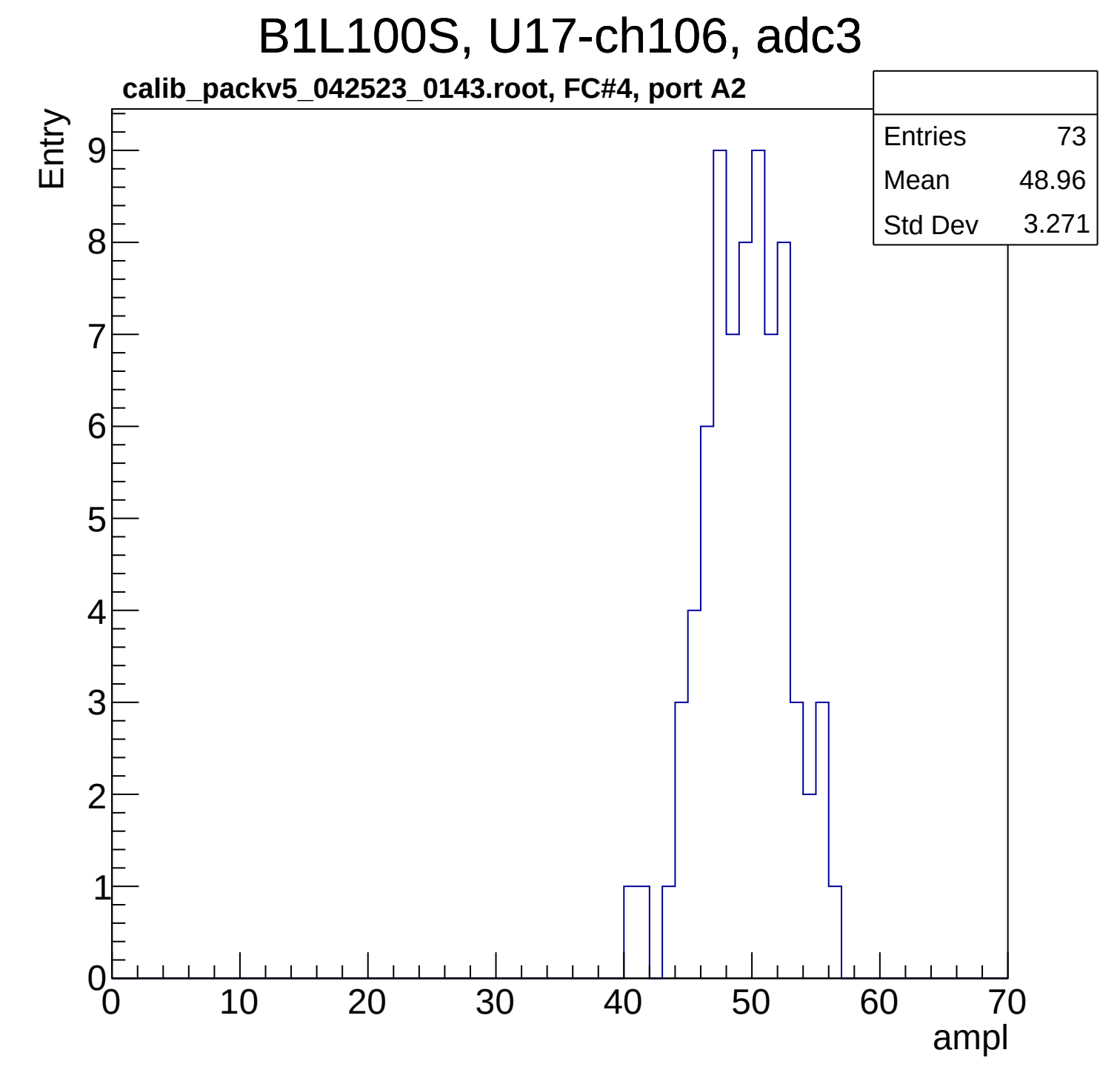
B1L100S, U17-ch106, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 48.96
Std Dev 3.271
Entry
ampl
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2
3
4
5
6
7
8
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0
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60
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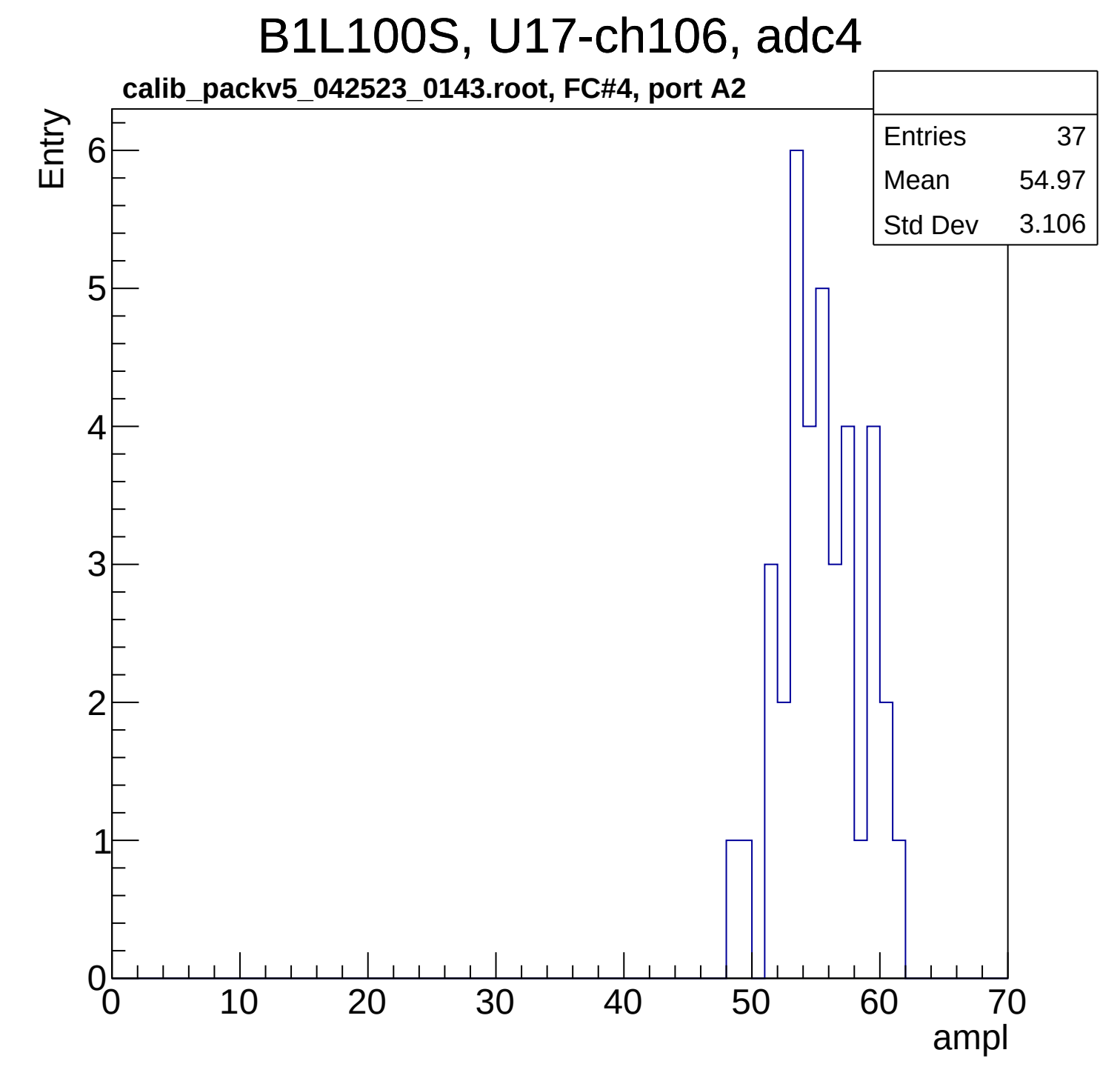
B1L100S, U17-ch106, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 37
Mean 54.97
Std Dev 3.106
Entry
ampl
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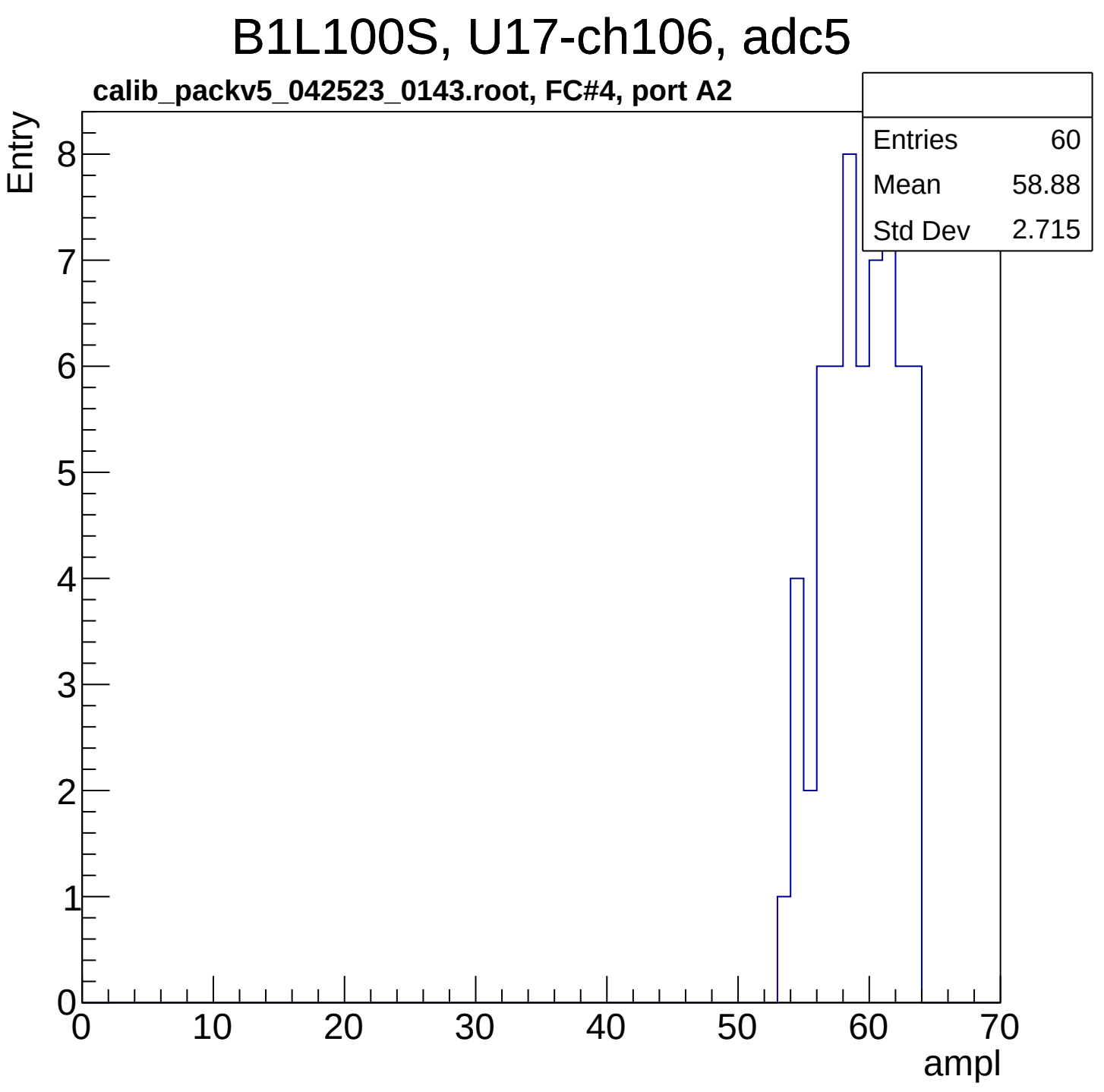
B1L100S, U17-ch106, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 58.88
Std Dev 2.715
Entry
ampl
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4
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6
7
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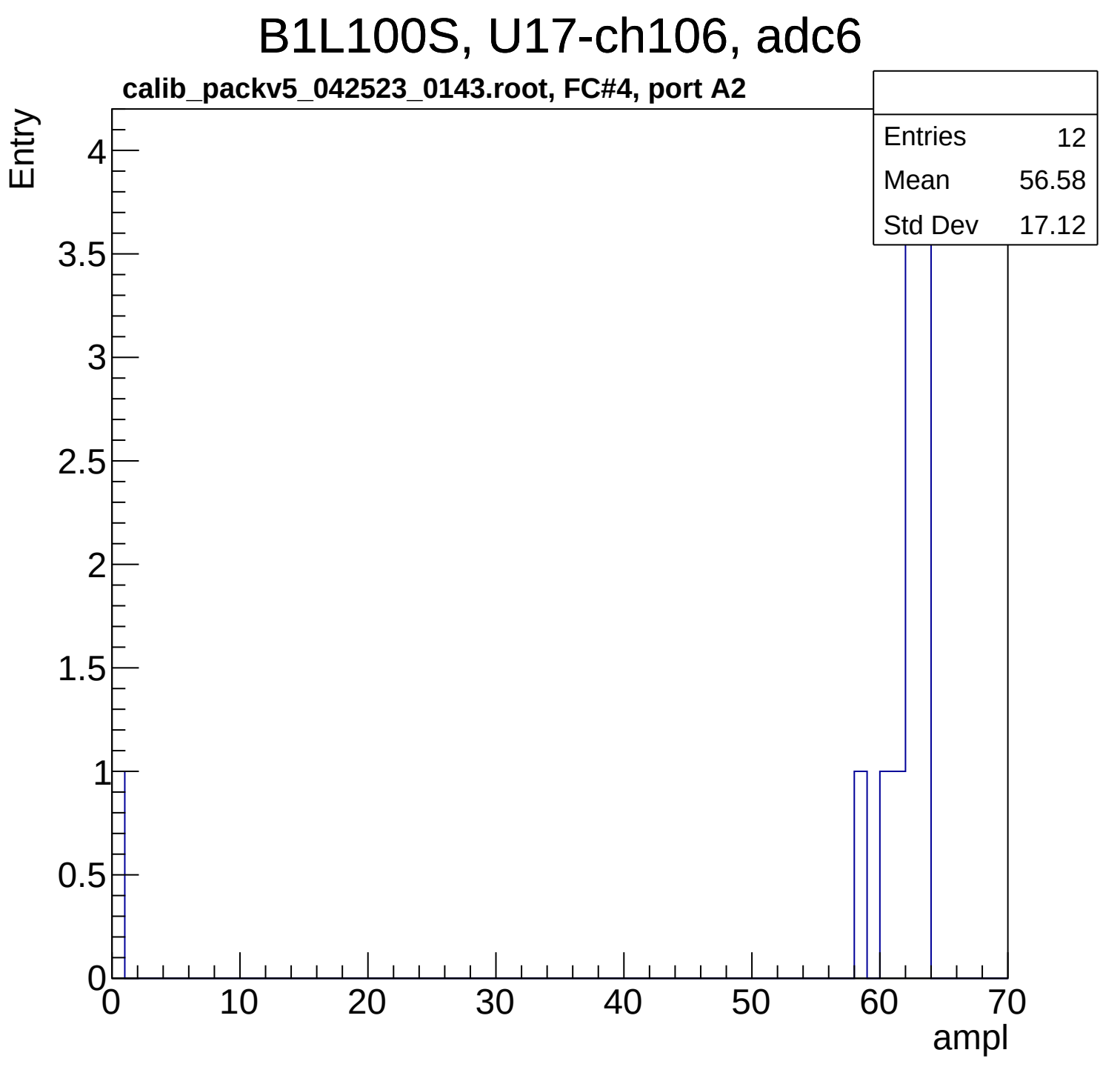
B1L100S, U17-ch106, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 12
Mean 56.58
Std Dev 17.12
Entry
ampl
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2
2.5
3
3.5
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0
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40
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60
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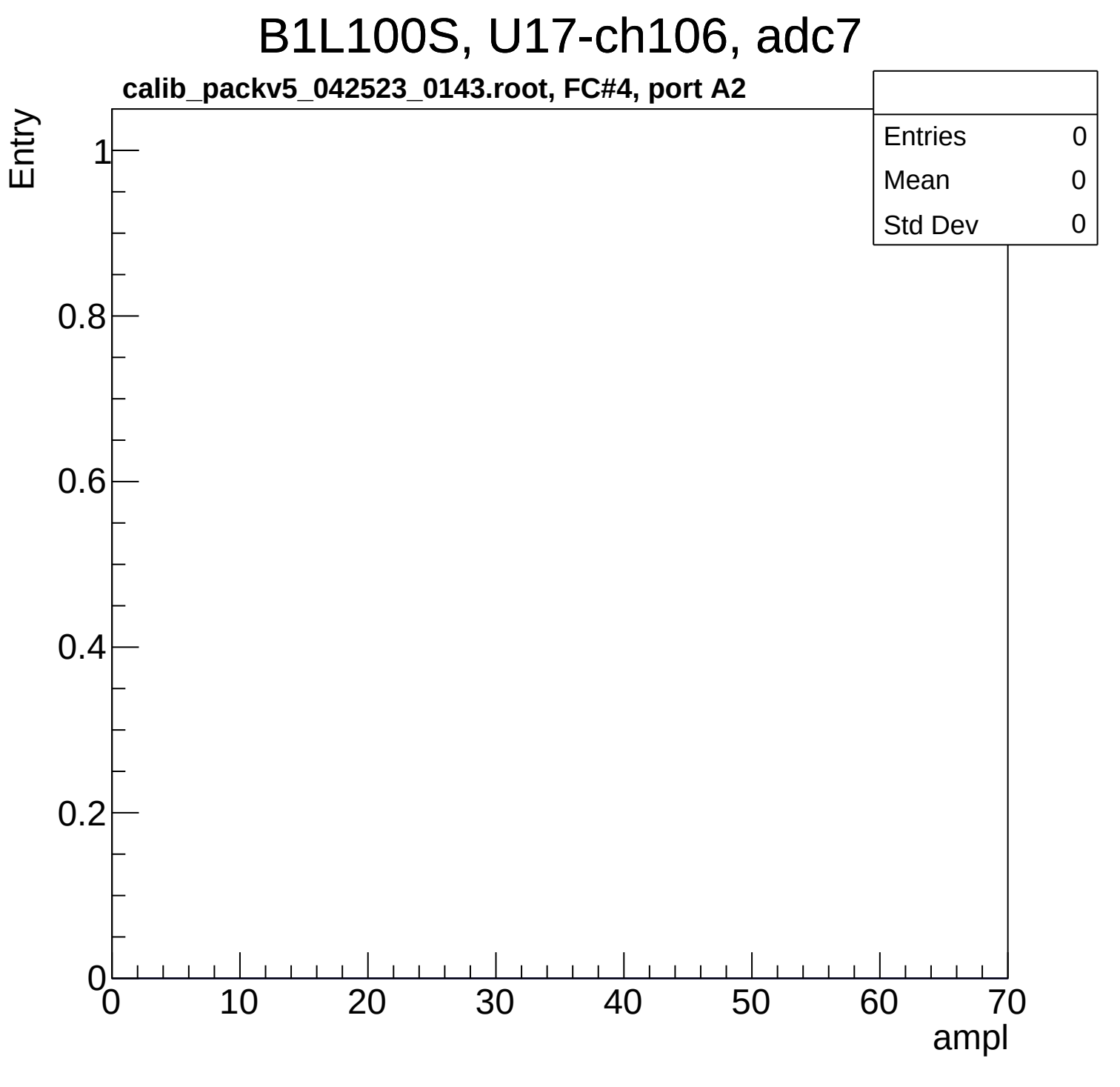
B1L100S, U17-ch106, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
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0.6
0.4
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10
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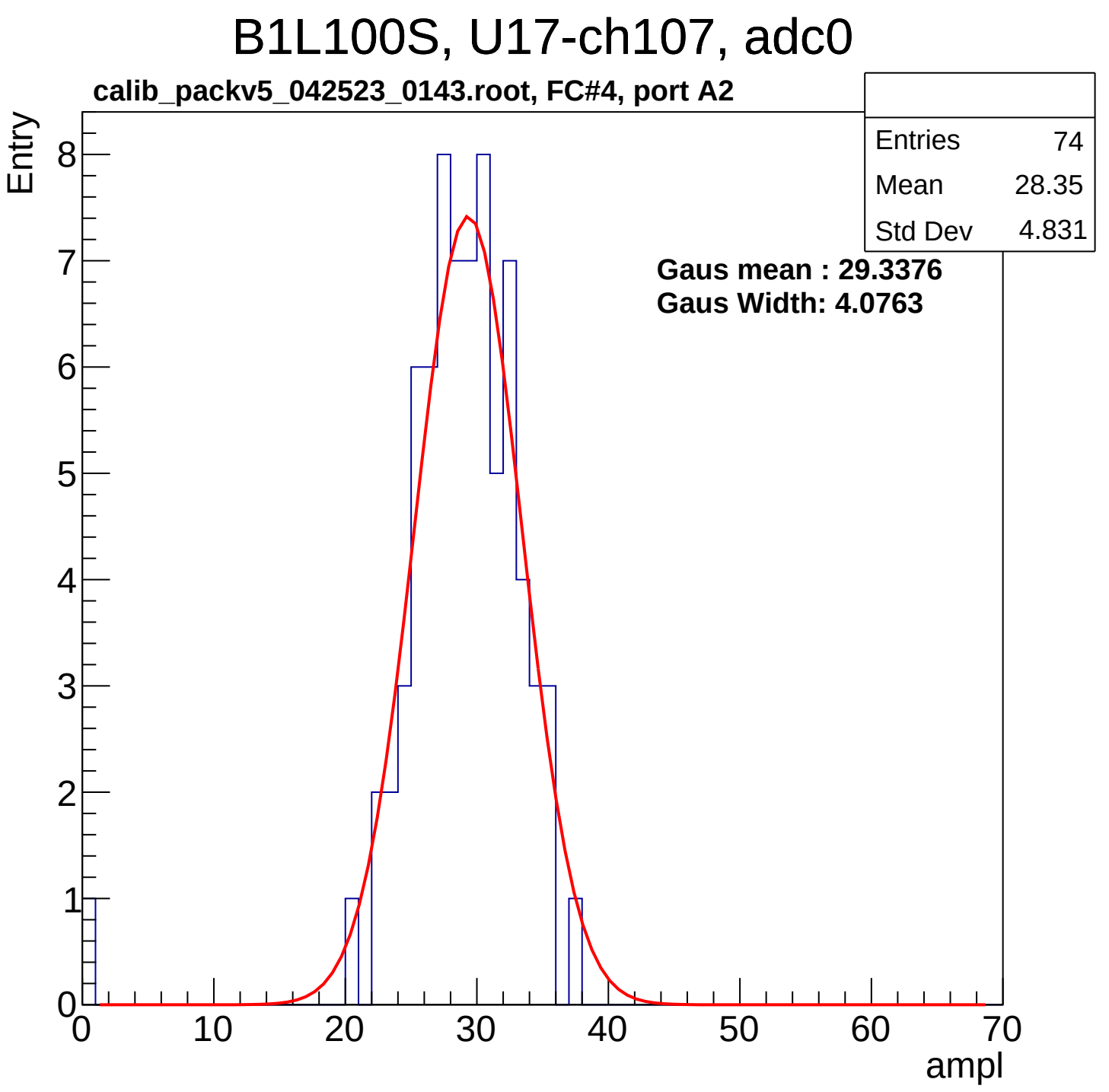
30
40
50
60
70
ampl


B1L100S, U17-ch107, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 74
Mean 28.35
Std Dev 4.831
Gaus mean : 29.3376
Gaus Width: 4.0763
Entry
ampl
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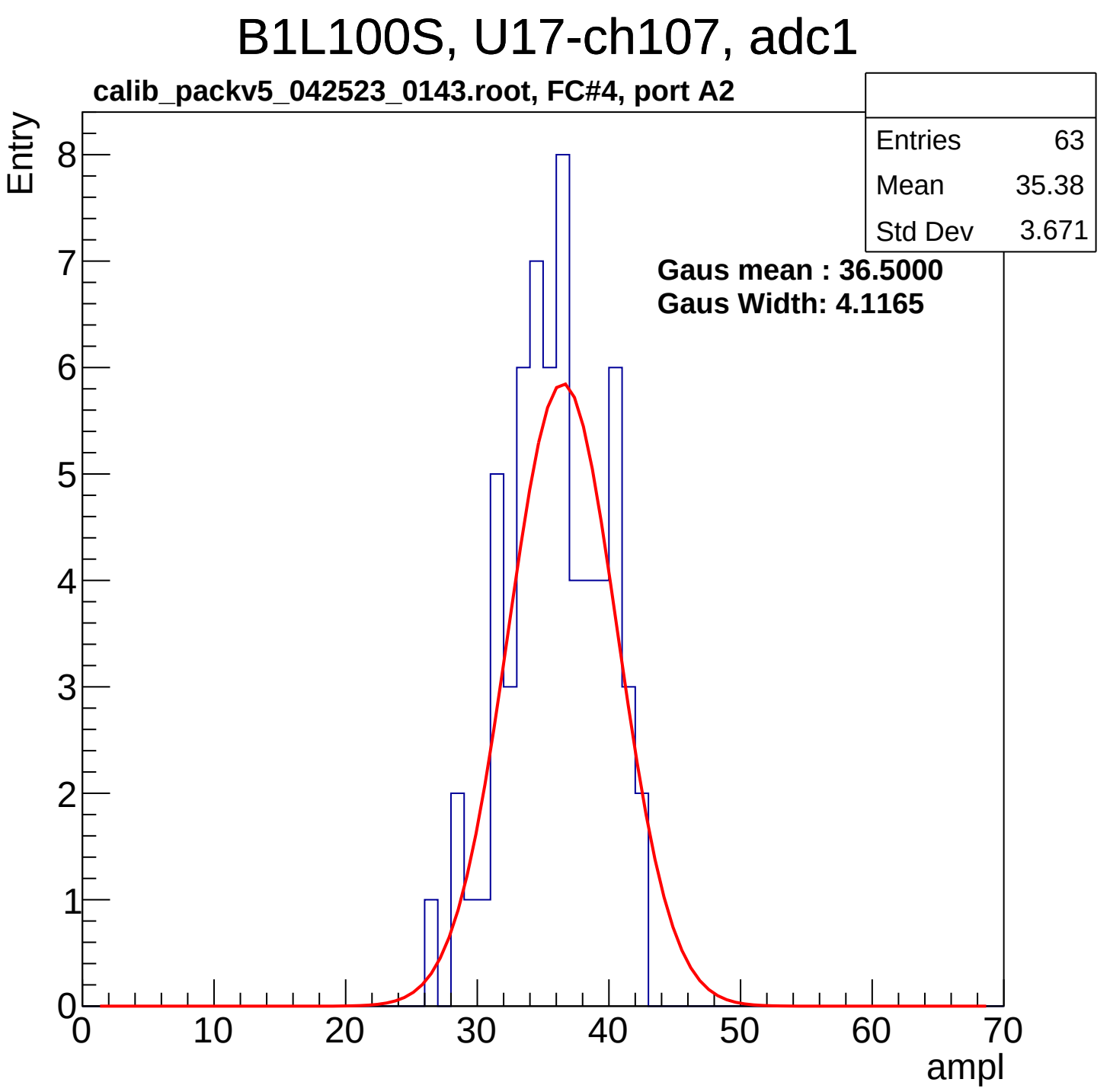
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch107, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 35.38
Std Dev 3.671
Gaus mean : 36.5000
Gaus Width: 4.1165
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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40
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60
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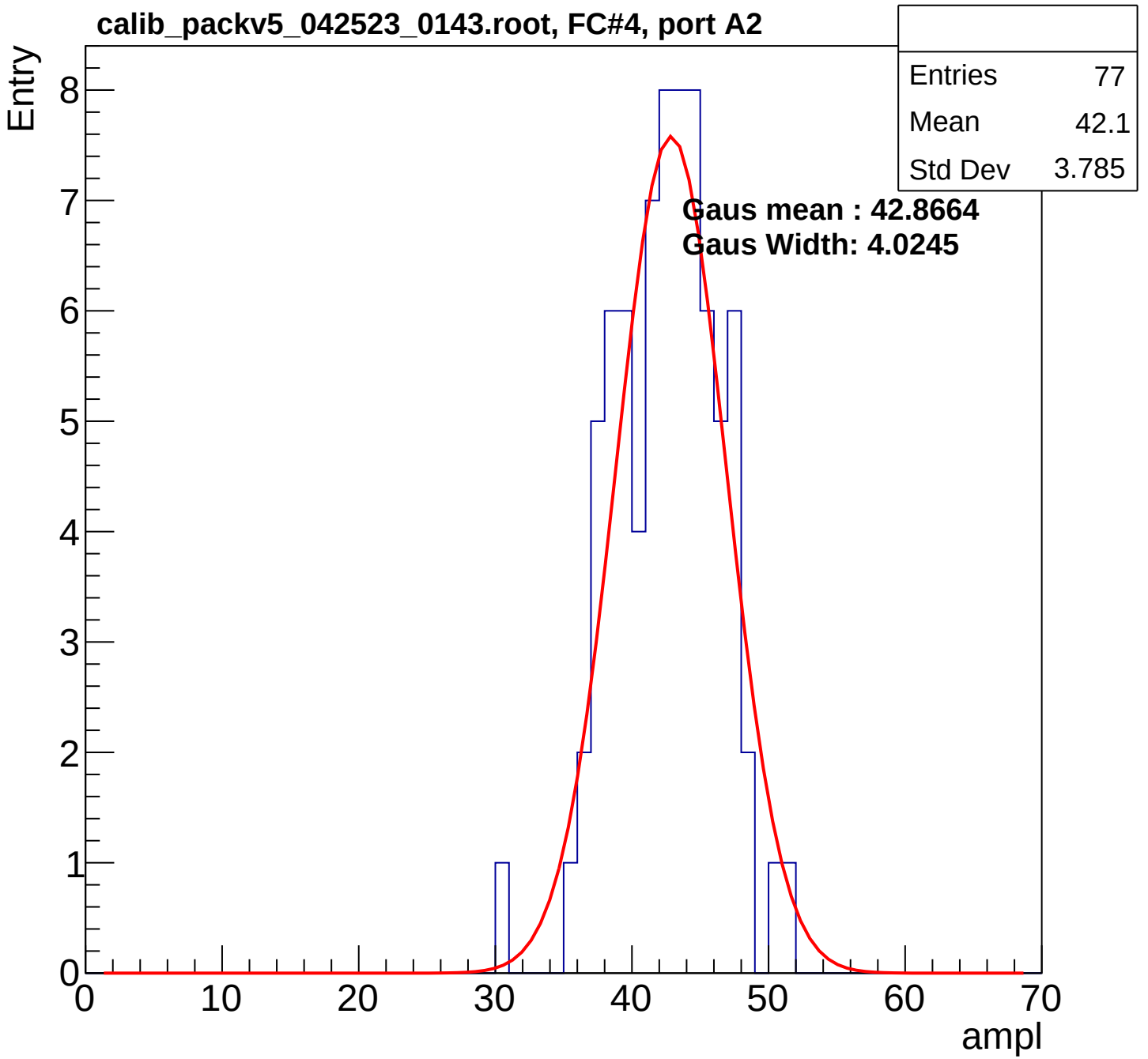
B1L100S, U17-ch107, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 77
Mean 42.1
Std Dev 3.785
Gaus mean : 42.8664
Gaus Width: 4.0245
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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40
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60
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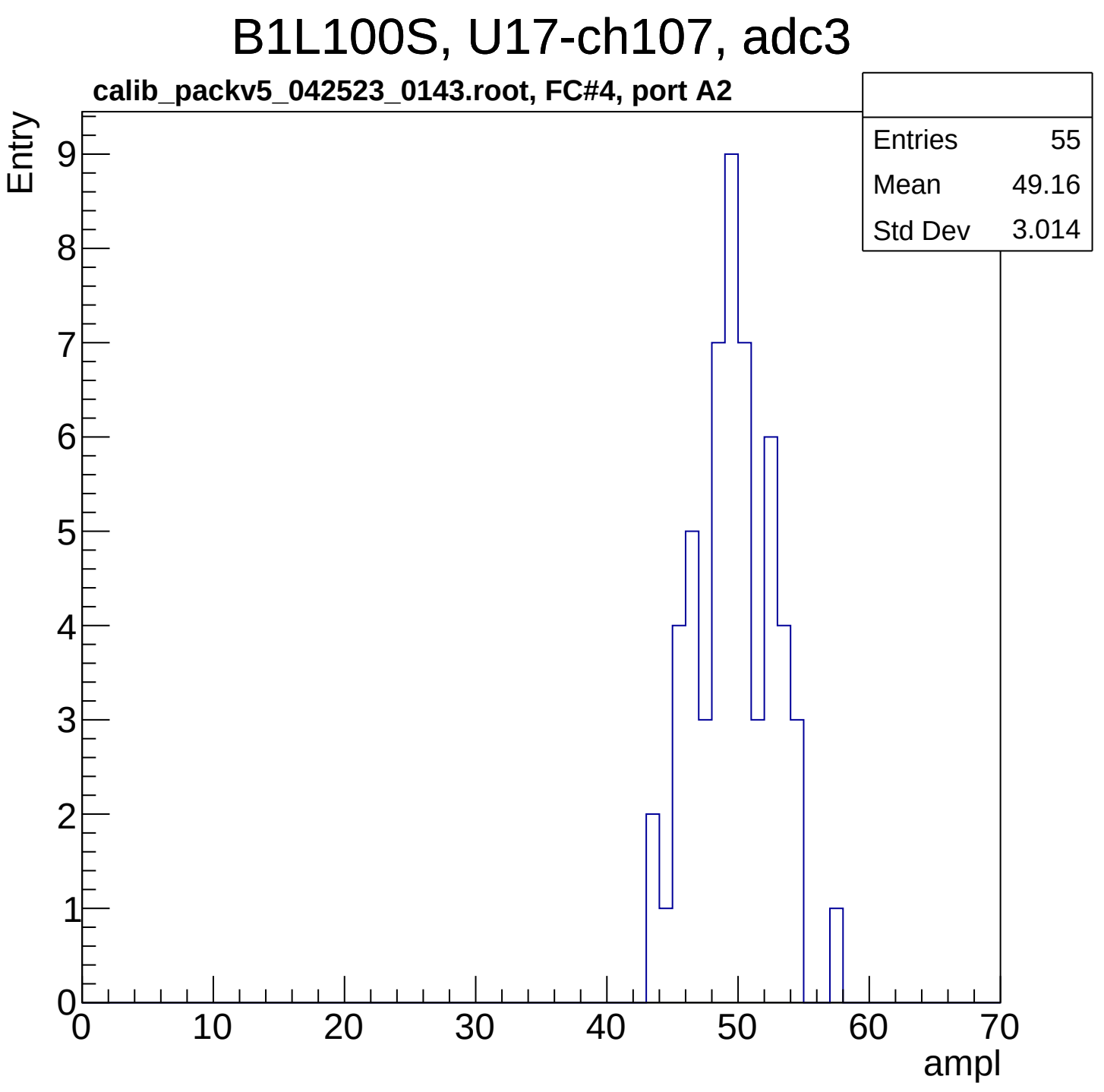
B1L100S, U17-ch107, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 49.16
Std Dev 3.014
Entry
ampl
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2
3
4
5
6
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8
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0
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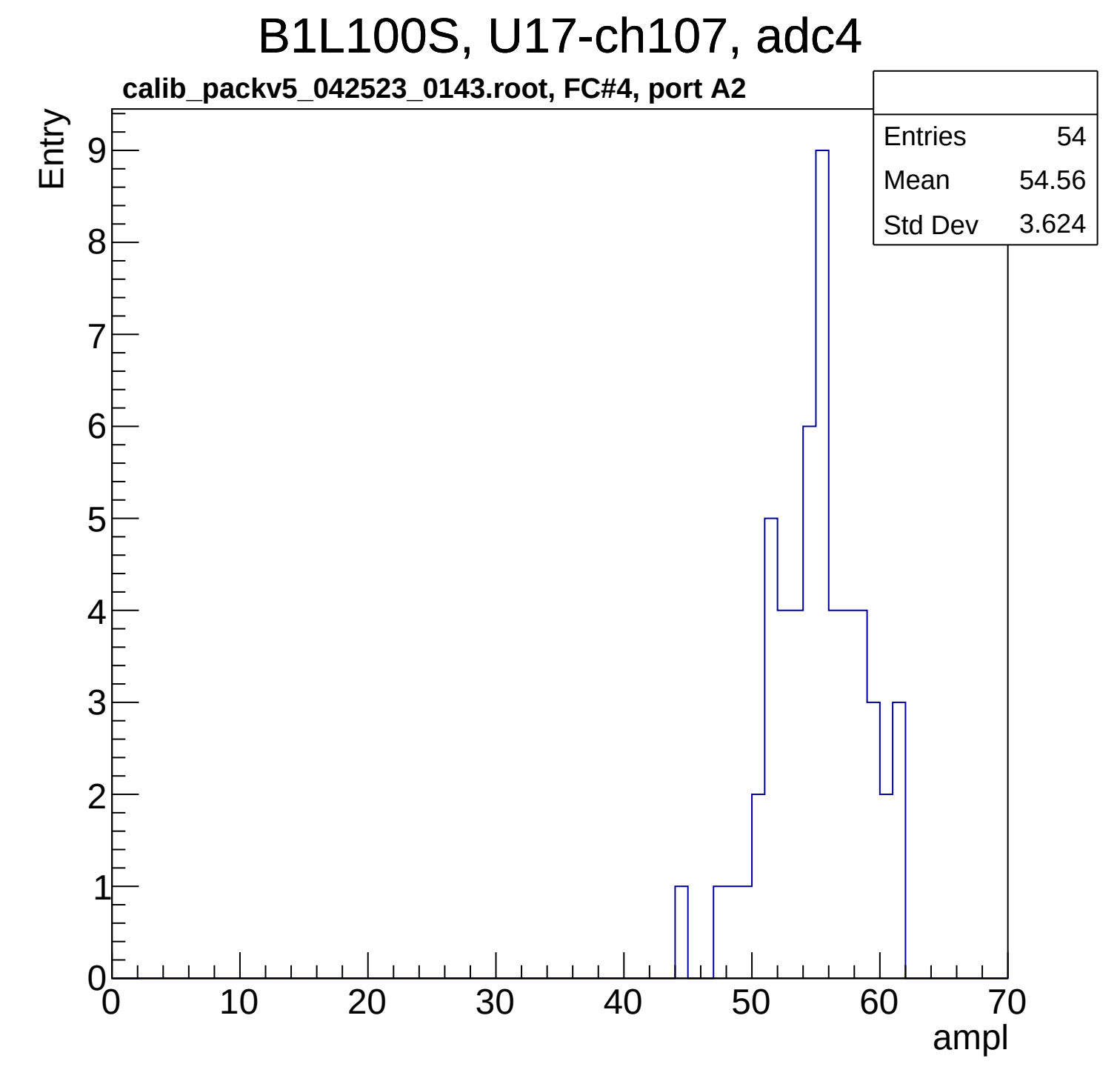
B1L100S, U17-ch107, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 54.56
Std Dev 3.624
Entry
ampl
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2
3
4
5
6
7
8
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0
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20
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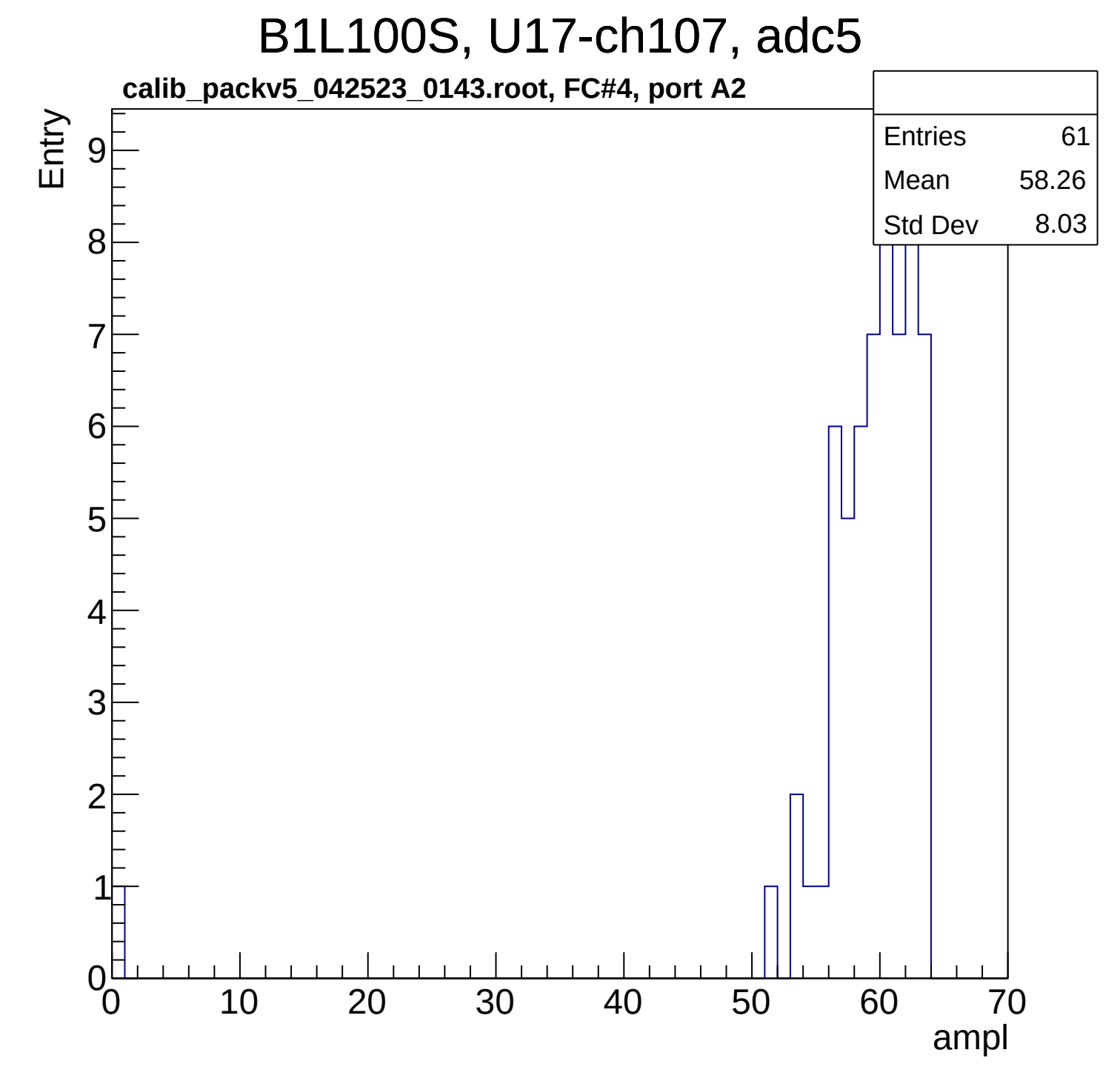
B1L100S, U17-ch107, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 58.26
Std Dev 8.03
Entry
ampl
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2
3
4
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7
8
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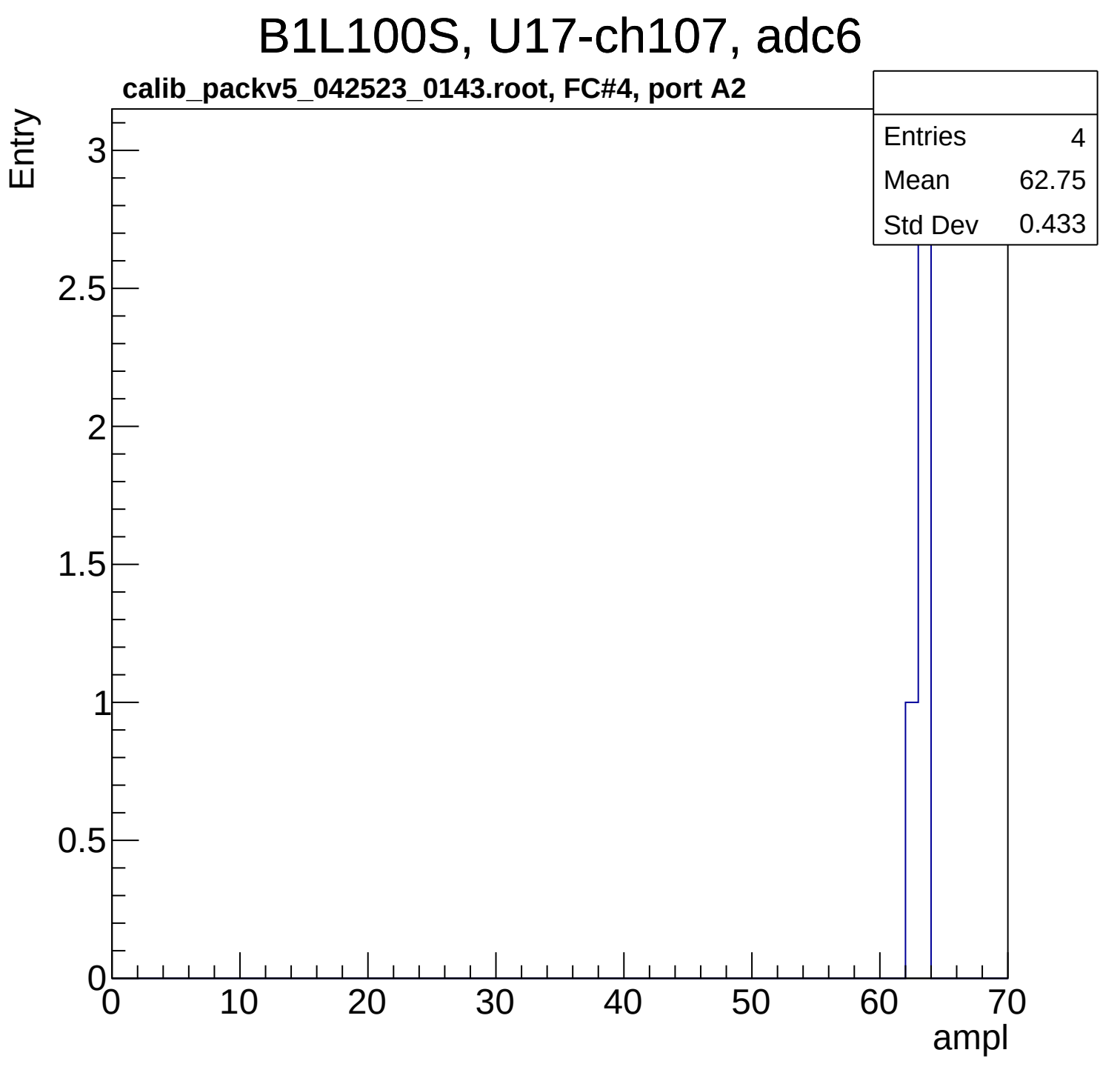
B1L100S, U17-ch107, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 4
Mean 62.75
Std Dev 0.433
Entry
ampl
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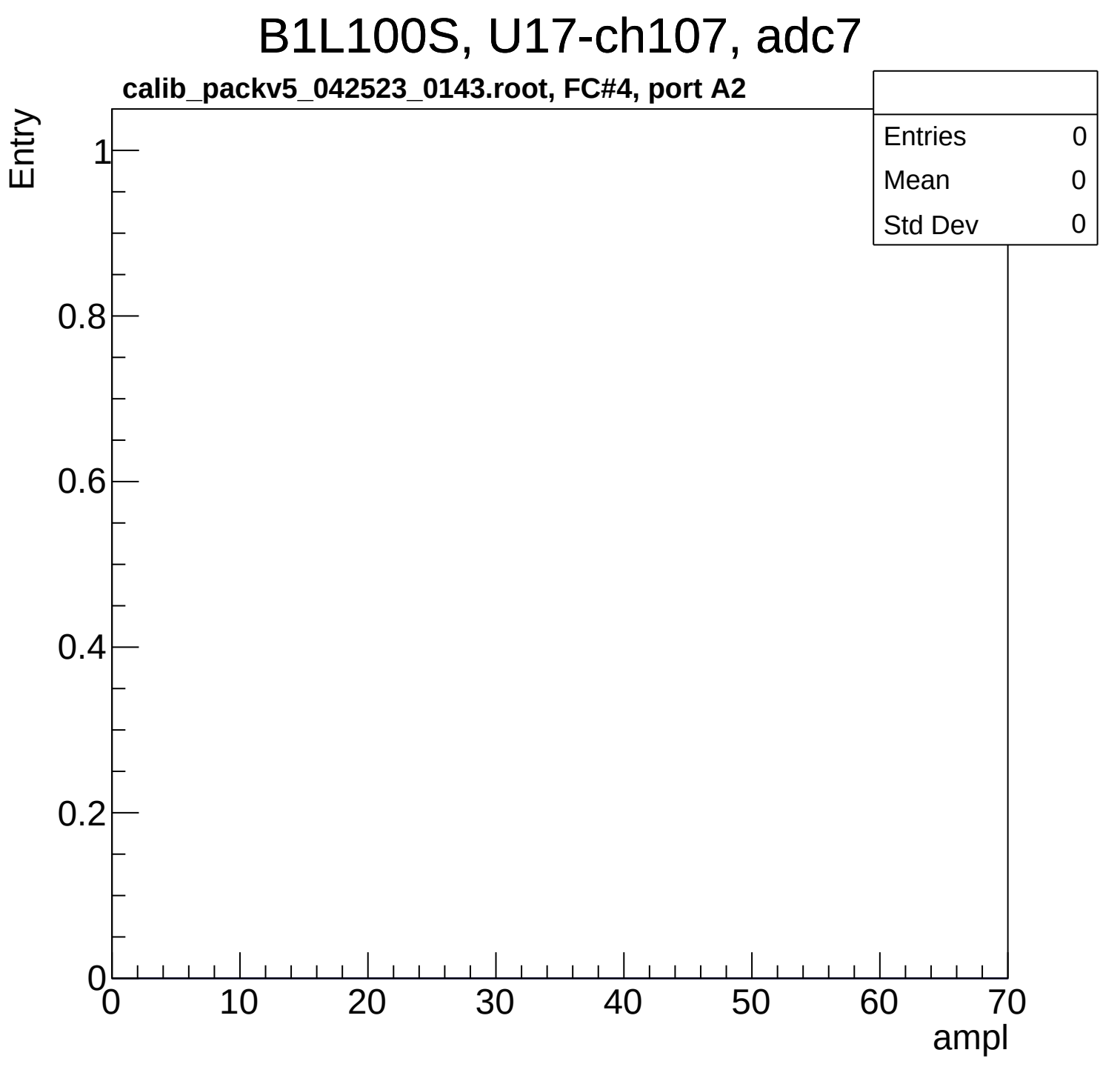
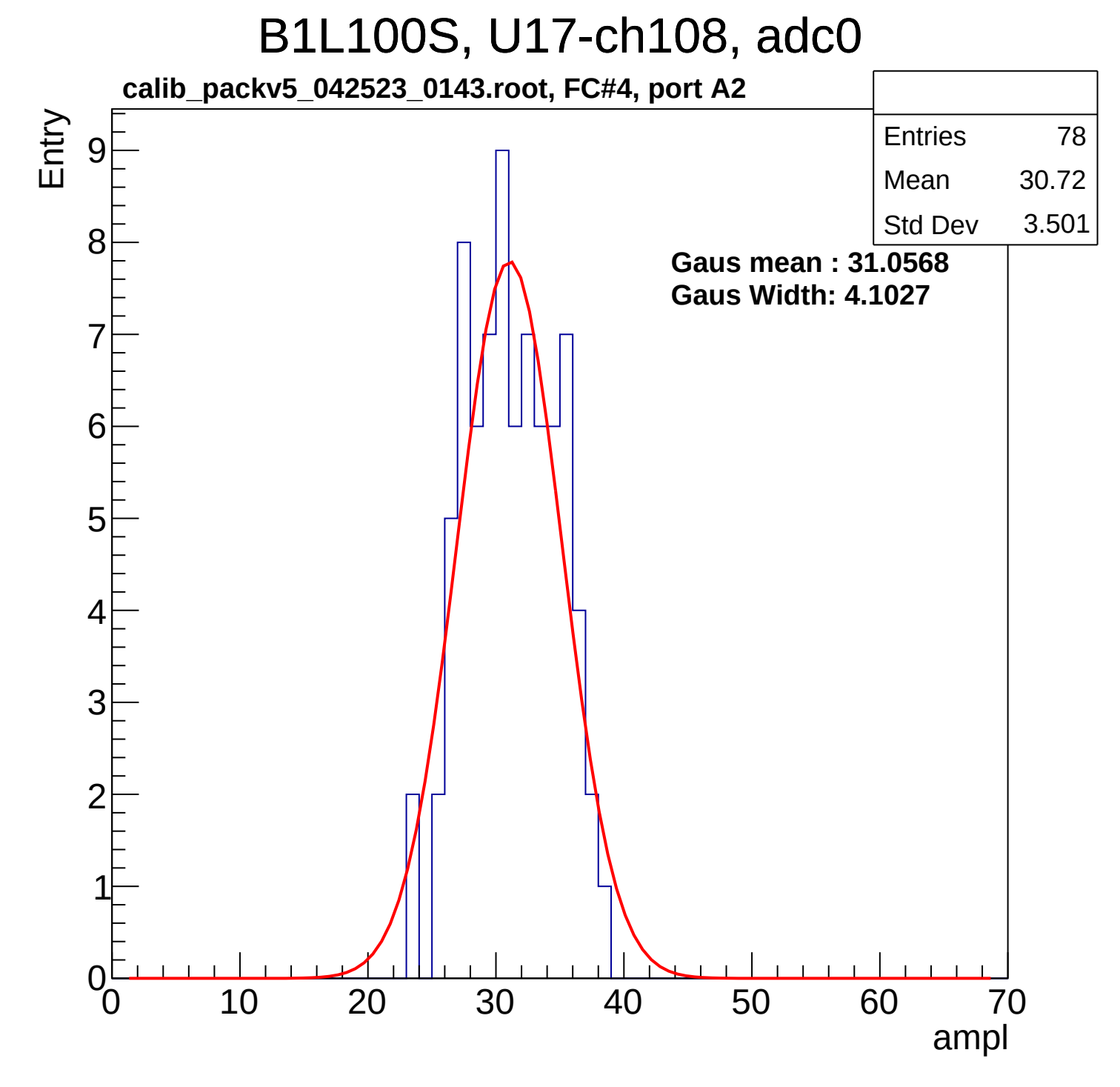
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L100S, U17-ch107, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch108, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 78
Mean 30.72
Std Dev 3.501
Gaus mean : 31.0568
Gaus Width: 4.1027
Entry
ampl
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2
3
4
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6
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0
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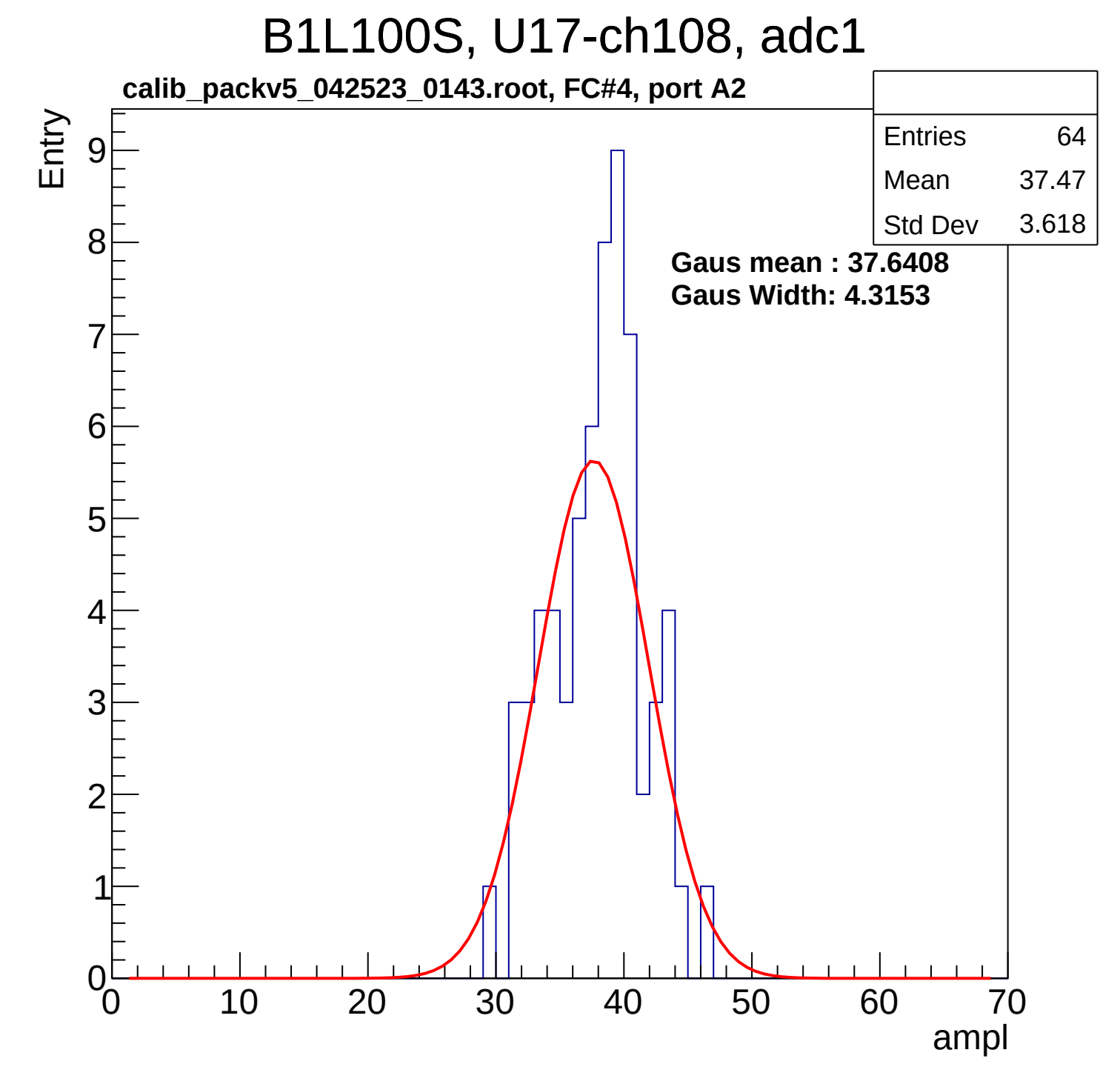
B1L100S, U17-ch108, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 37.47
Std Dev 3.618
Gaus mean : 37.6408
Gaus Width: 4.3153
Entry
ampl
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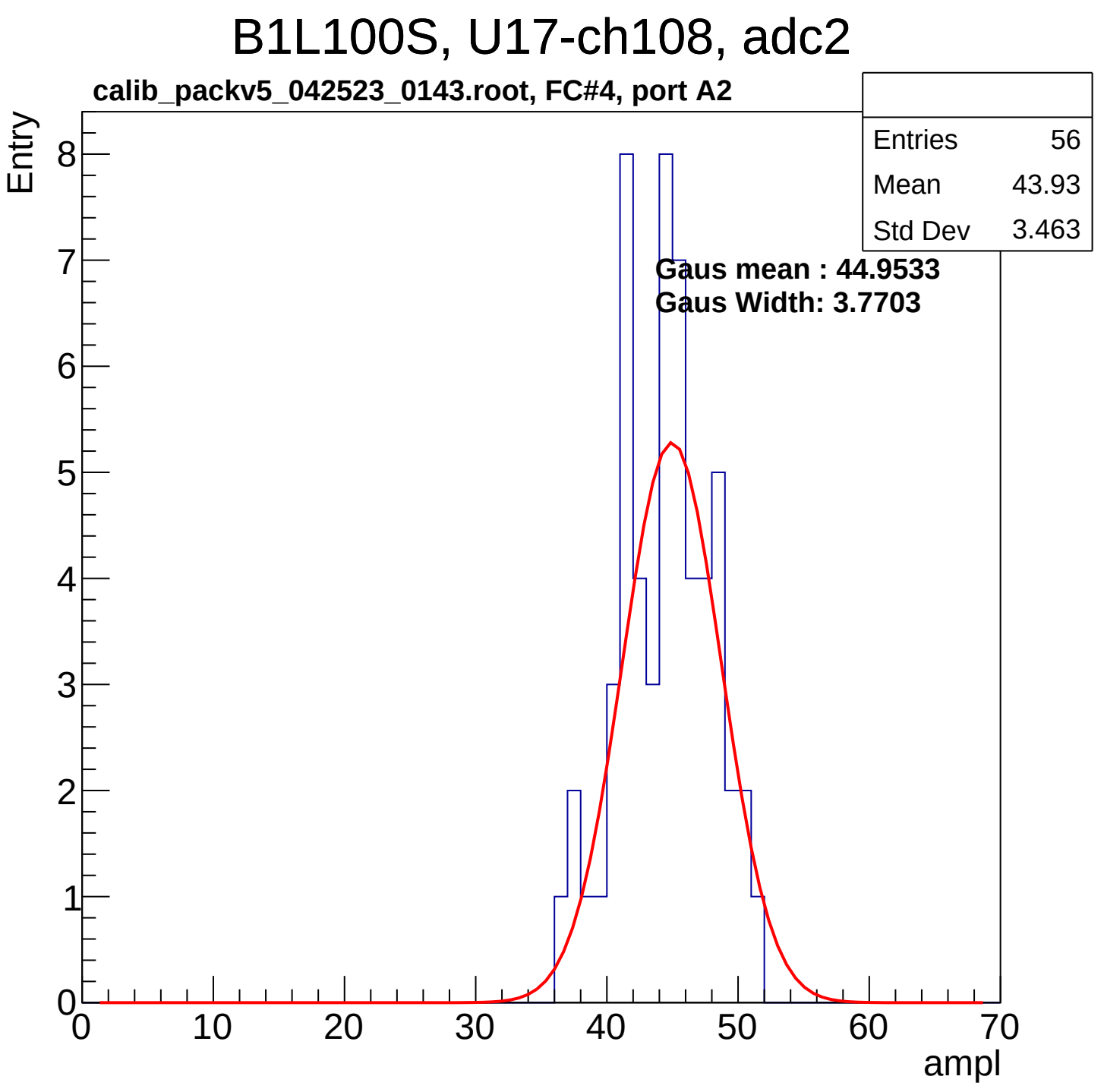
B1L100S, U17-ch108, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 43.93
Std Dev 3.463
Gaus mean : 44.9533
Gaus Width: 3.7703
Entry
ampl
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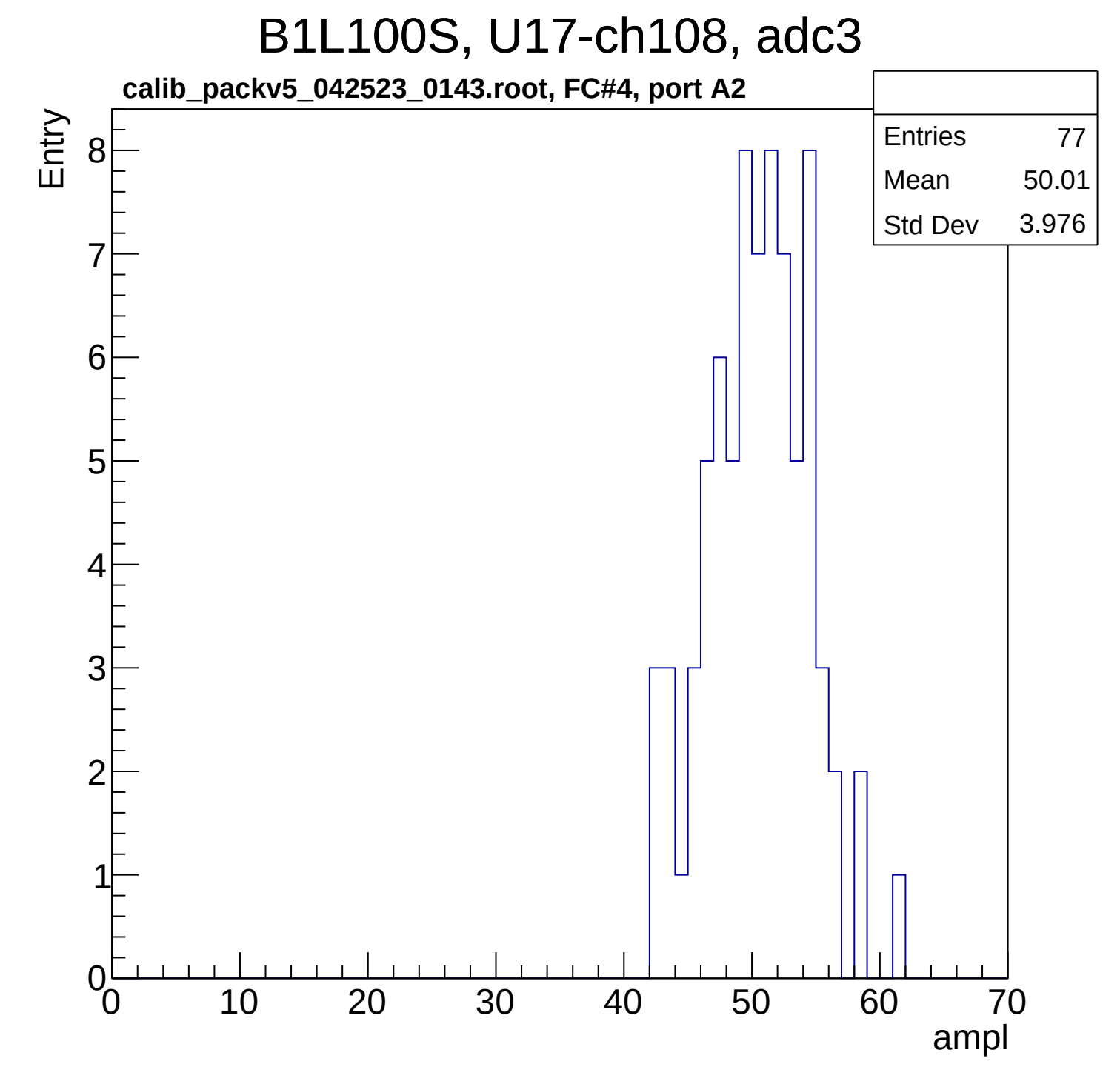
B1L100S, U17-ch108, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 77
Mean 50.01
Std Dev 3.976
Entry
ampl
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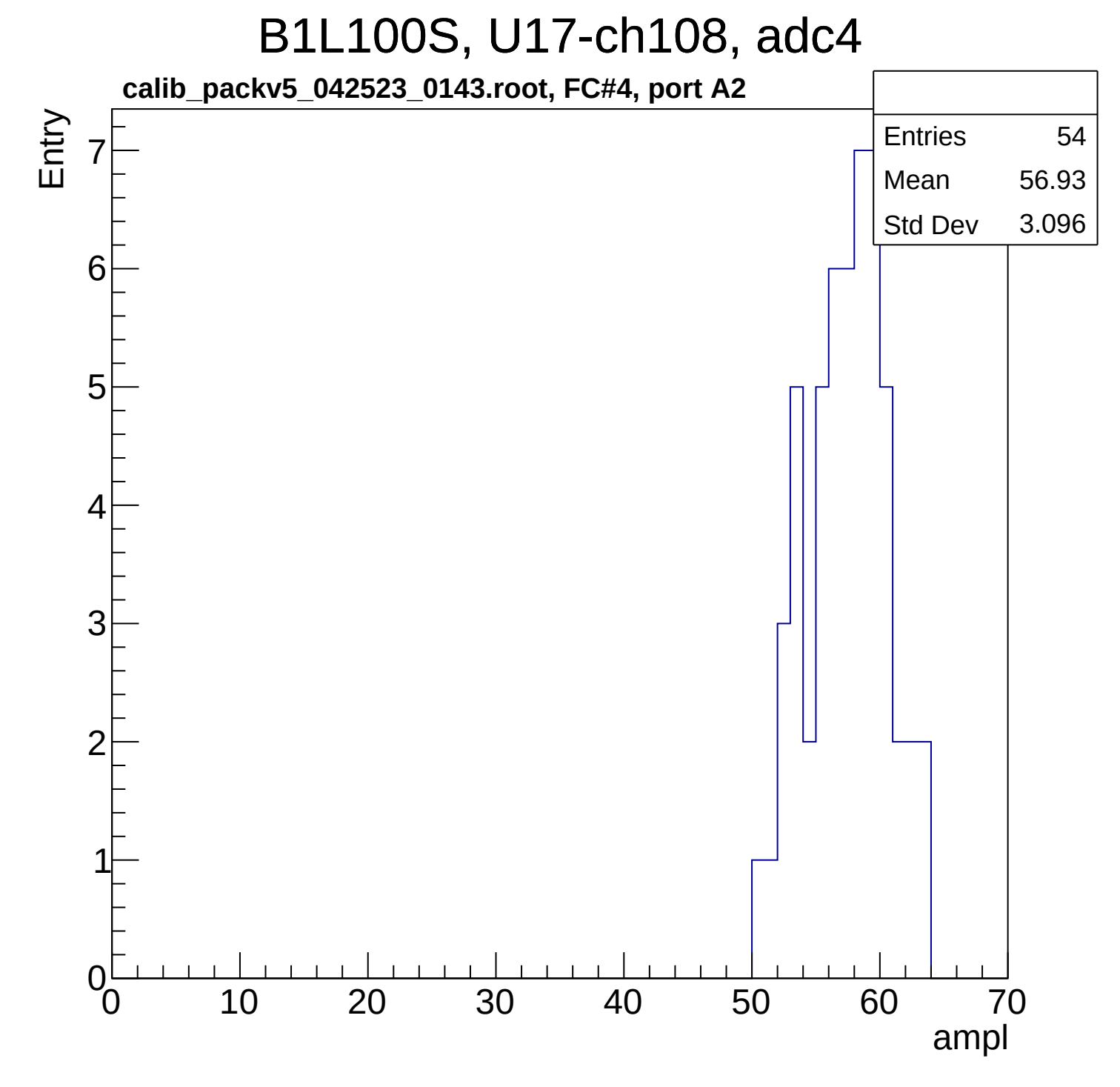
B1L100S, U17-ch108, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 56.93
Std Dev 3.096
Entry
ampl
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1
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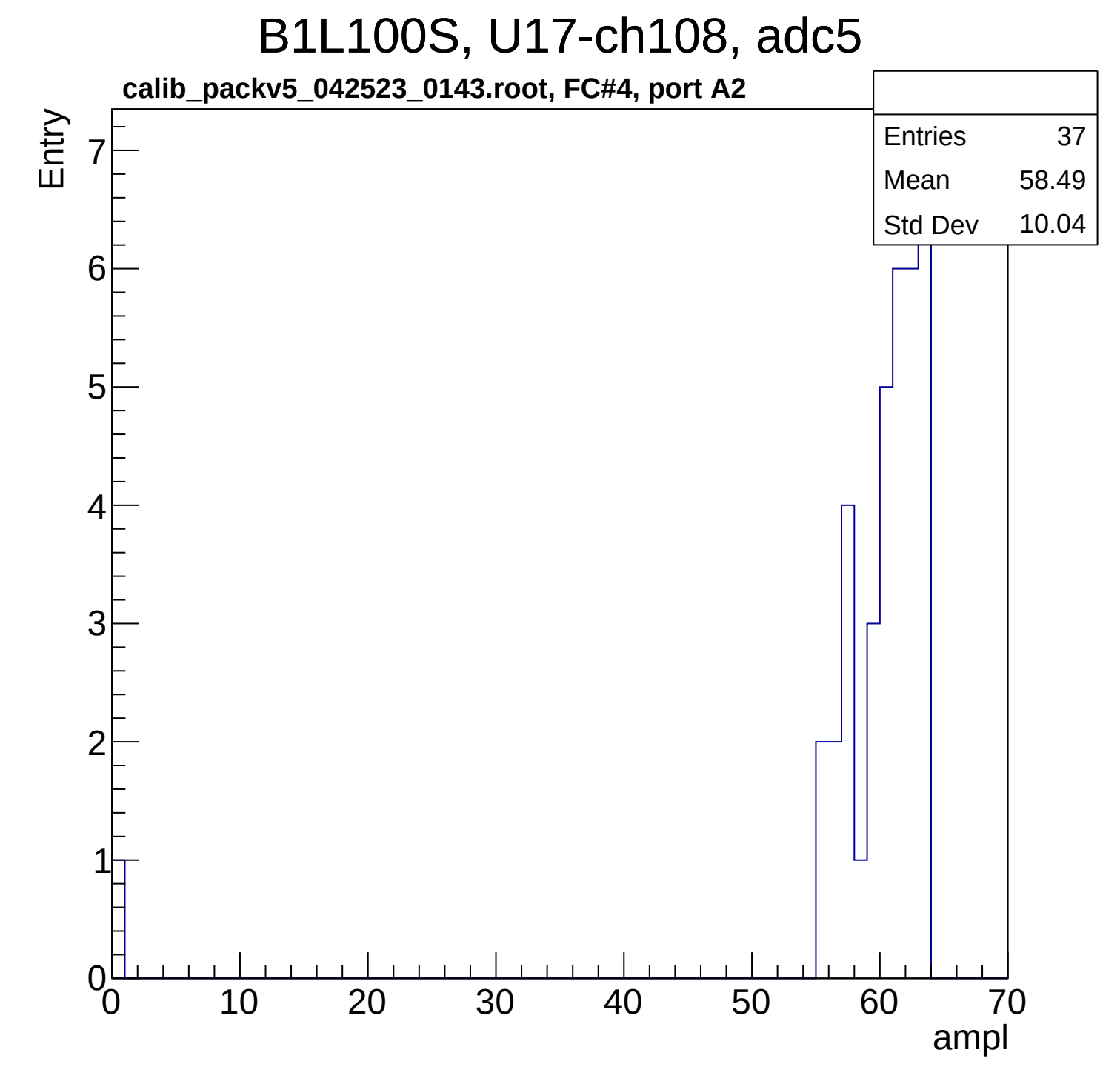
B1L100S, U17-ch108, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 37
Mean 58.49
Std Dev 10.04
Entry
ampl
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1
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4
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0
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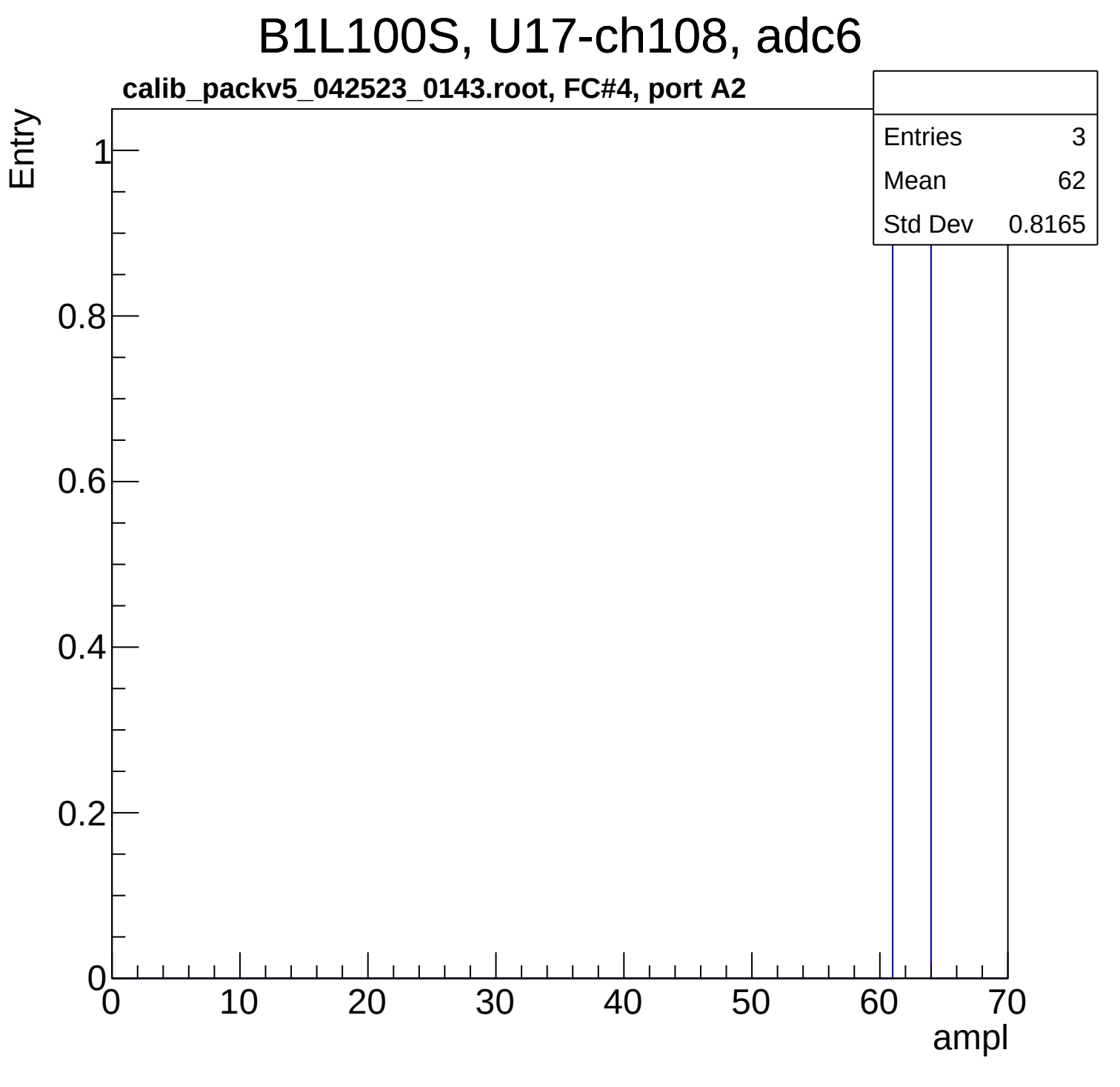
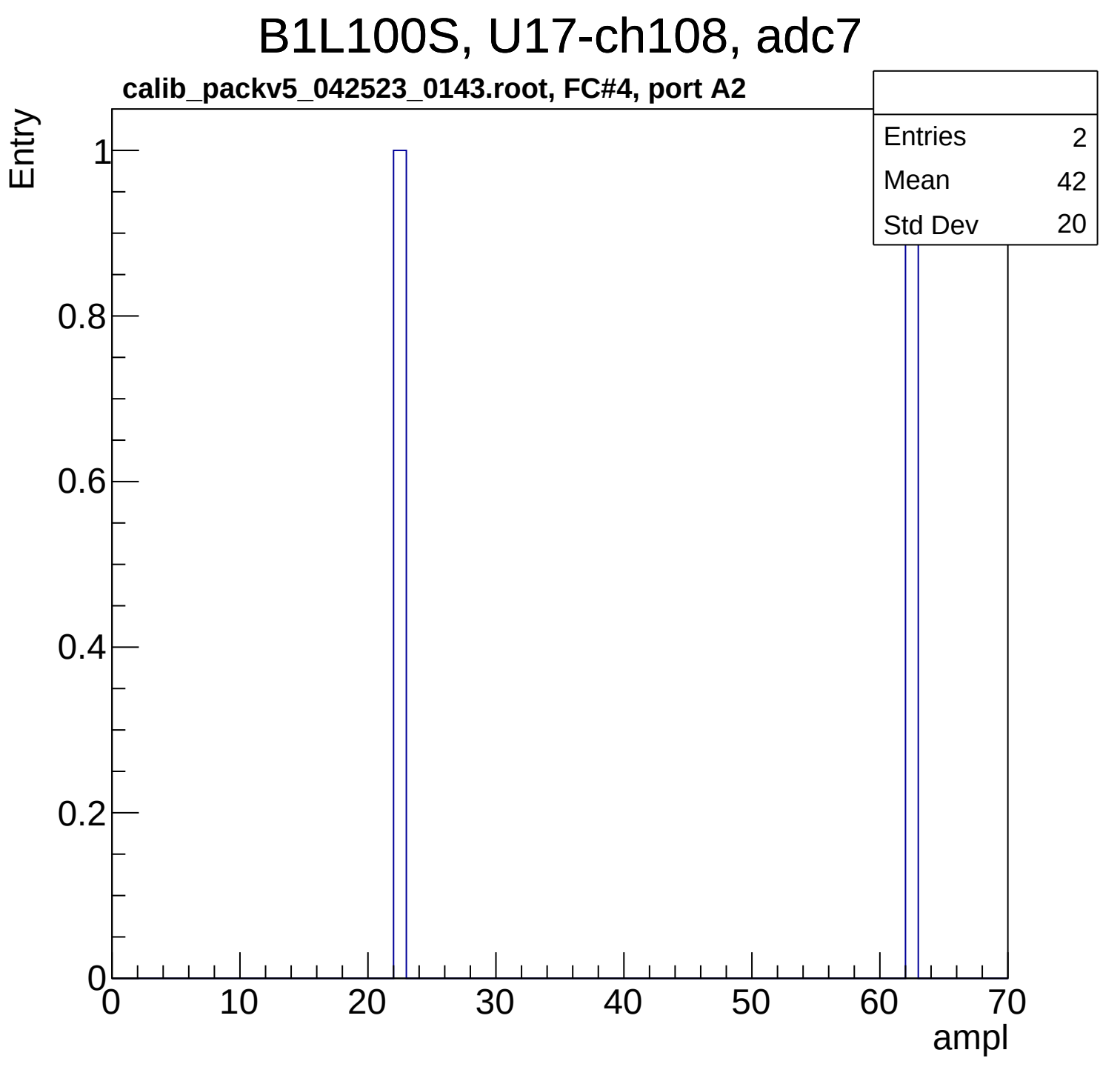

B1L100S, U17-ch108, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 62
Std Dev 0.8165
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch108, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 42
Std Dev 20
Entry
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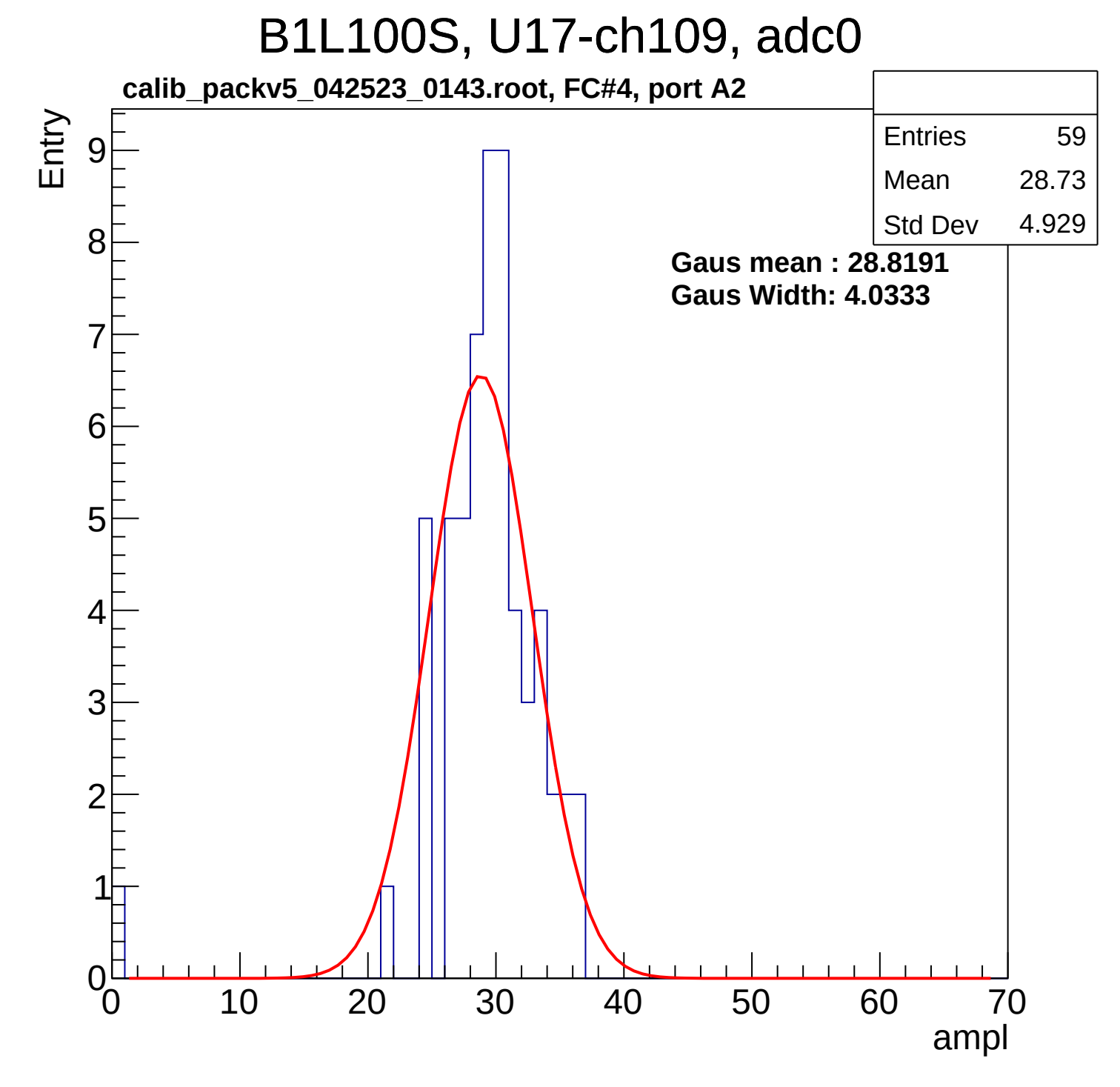
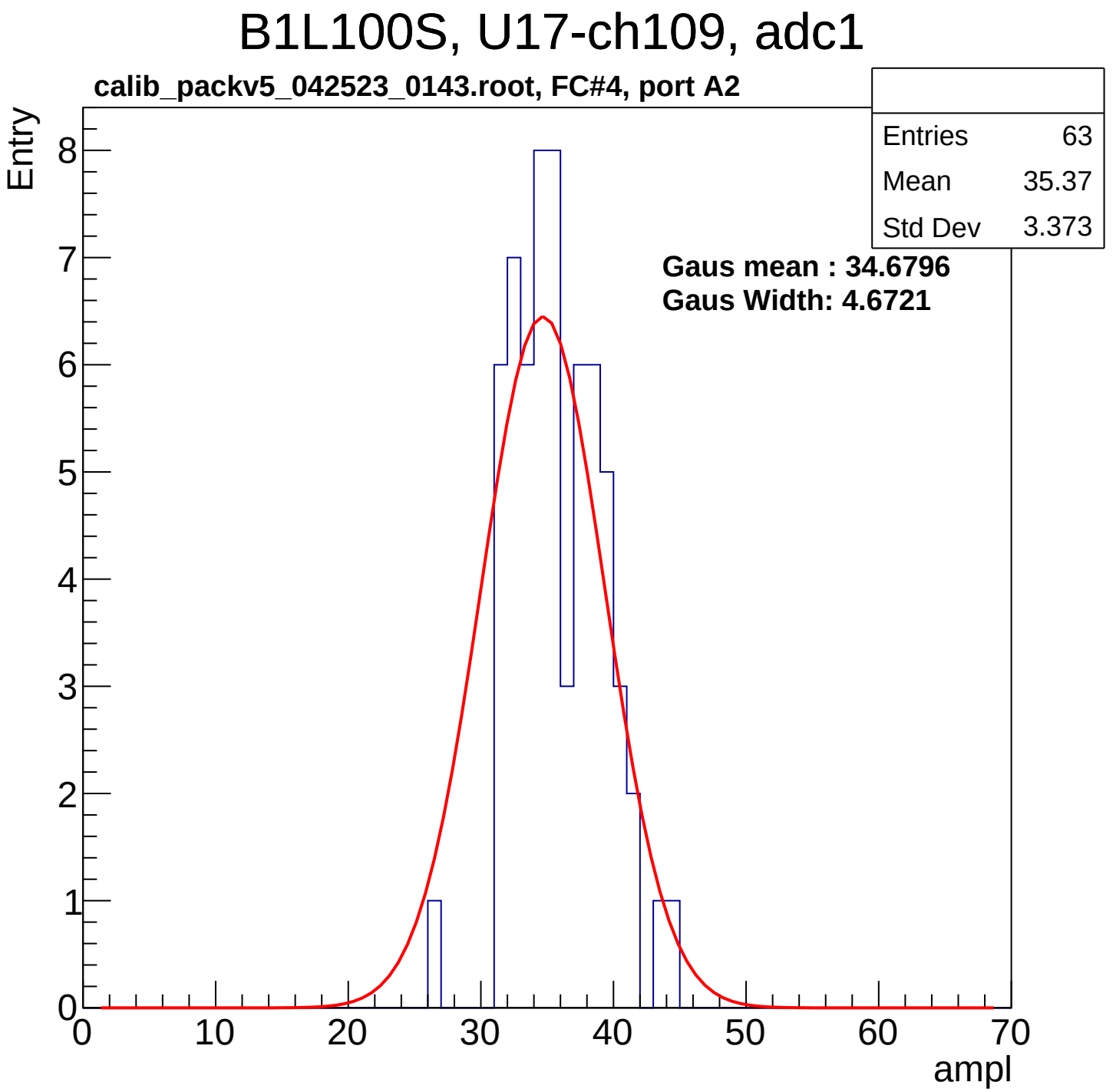
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch109, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 28.73
Std Dev 4.929
Gaus mean : 28.8191
Gaus Width: 4.0333
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch109, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 35.37
Std Dev 3.373
Gaus mean : 34.6796
Gaus Width: 4.6721
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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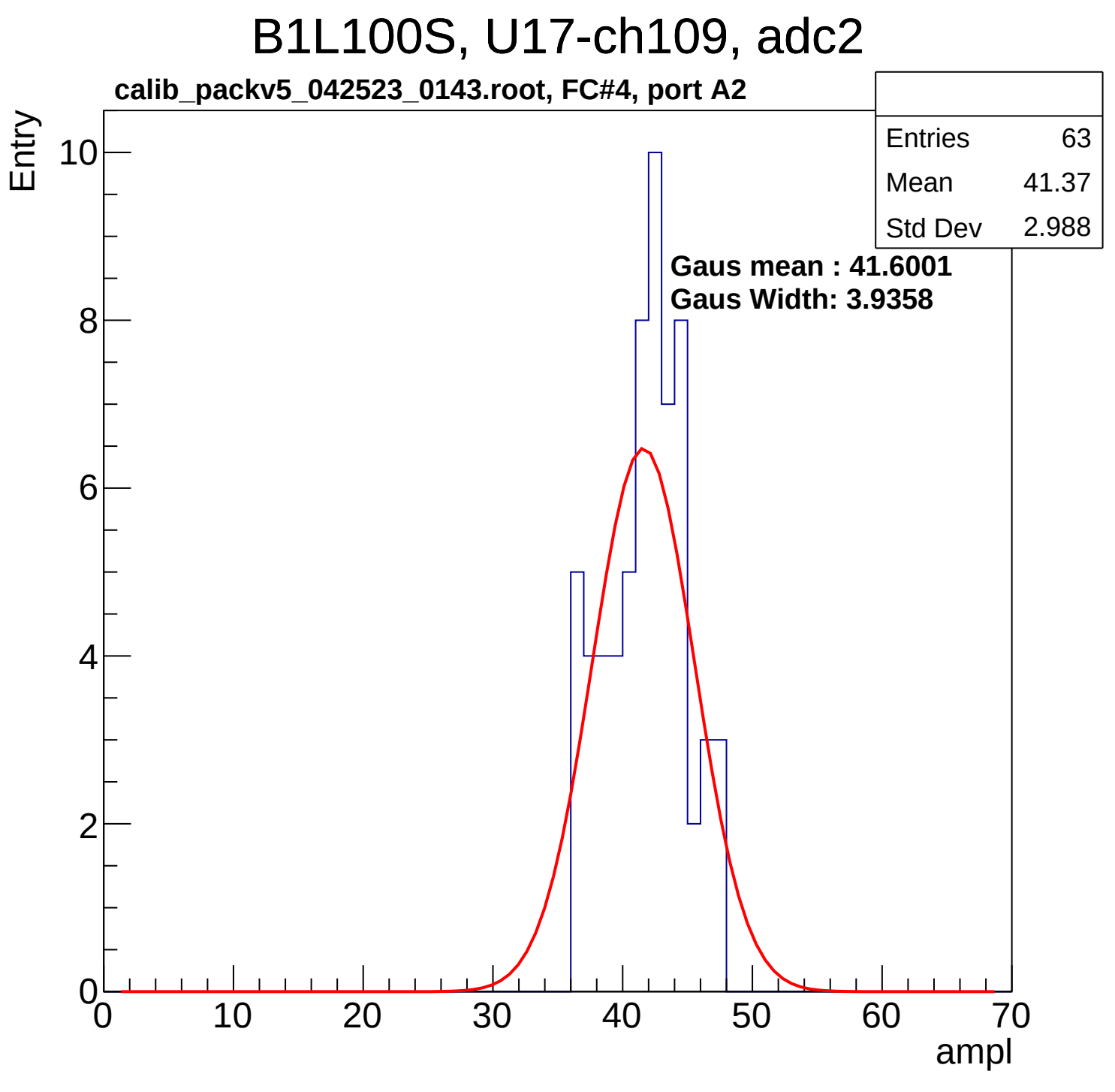
B1L100S, U17-ch109, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 41.37
Std Dev 2.988
Gaus mean : 41.6001
Gaus Width: 3.9358
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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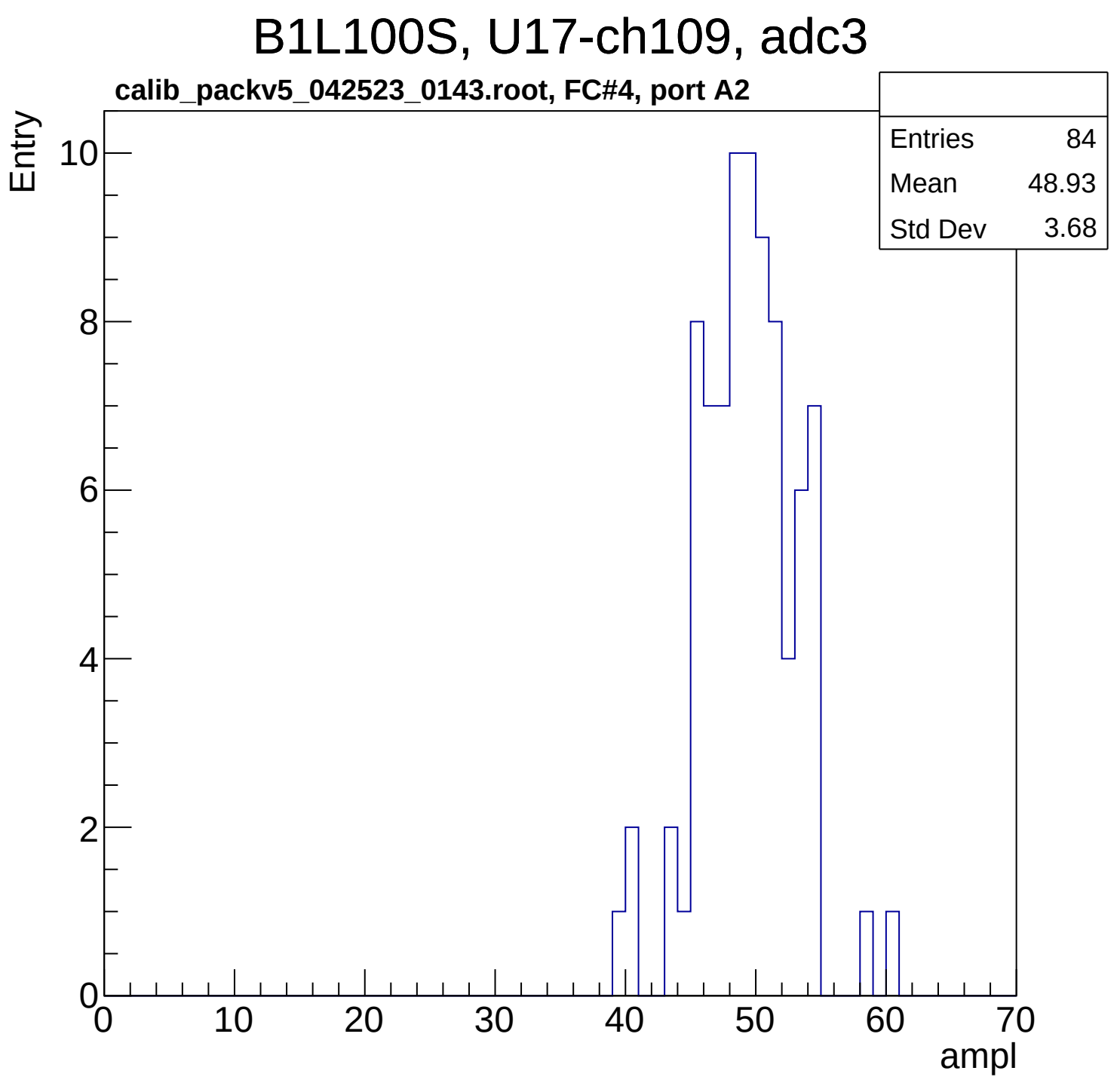
B1L100S, U17-ch109, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 84
Mean 48.93
Std Dev 3.68
Entry
ampl
0
2
4
6
8
10
0
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20
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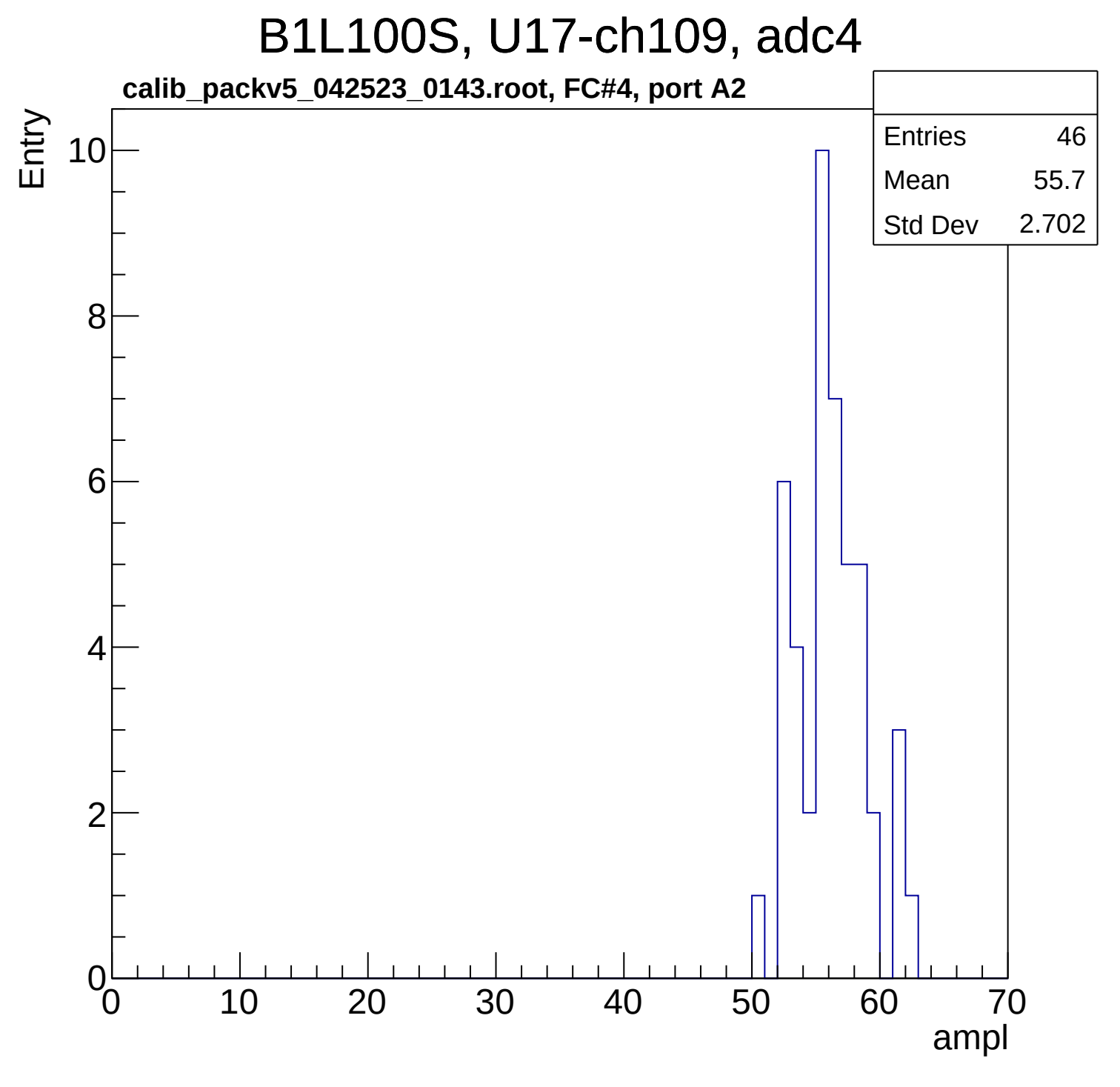
40
50
60
70


B1L100S, U17-ch109, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 46
Mean 55.7
Std Dev 2.702
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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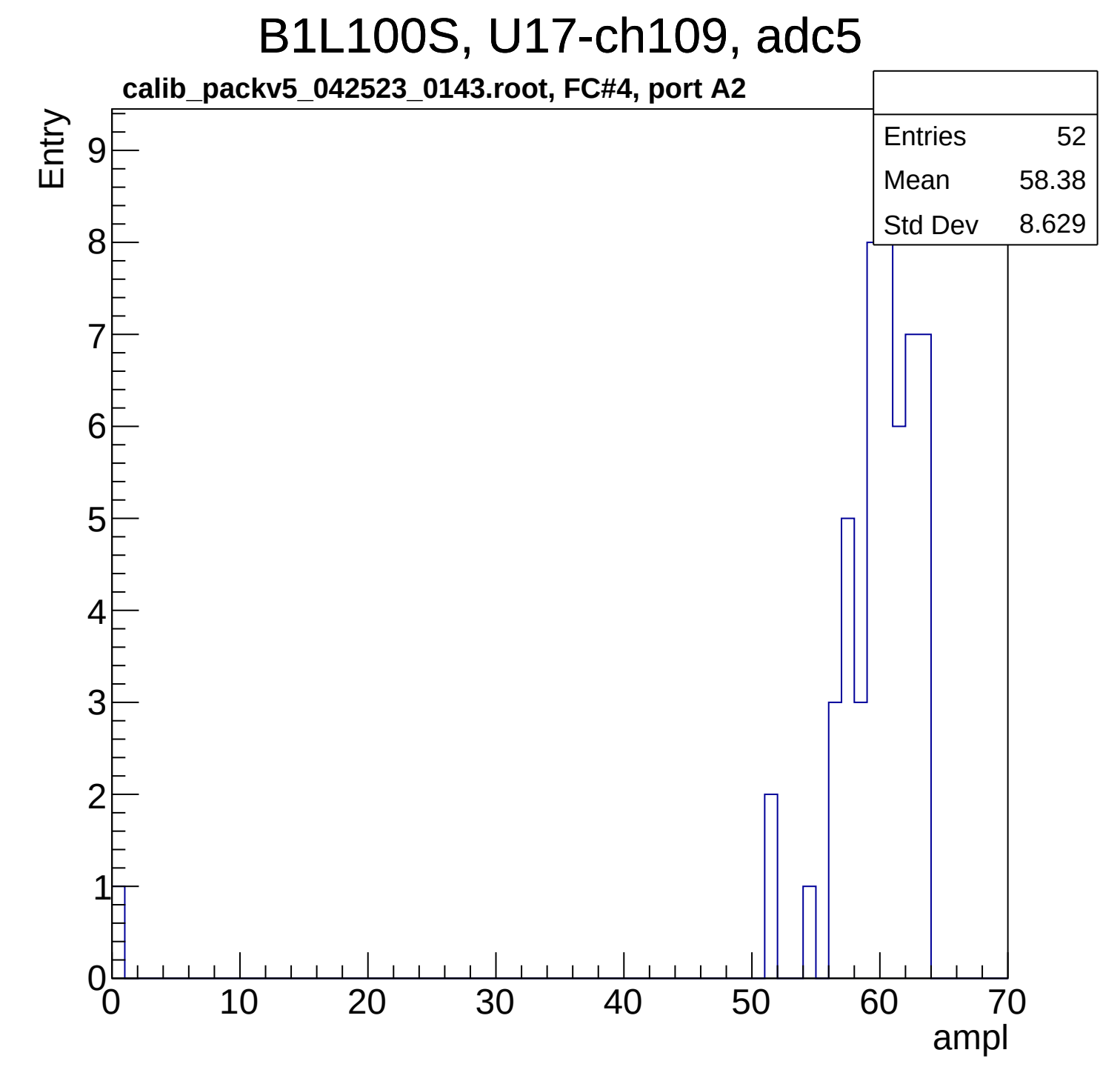
B1L100S, U17-ch109, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 52
Mean 58.38
Std Dev 8.629
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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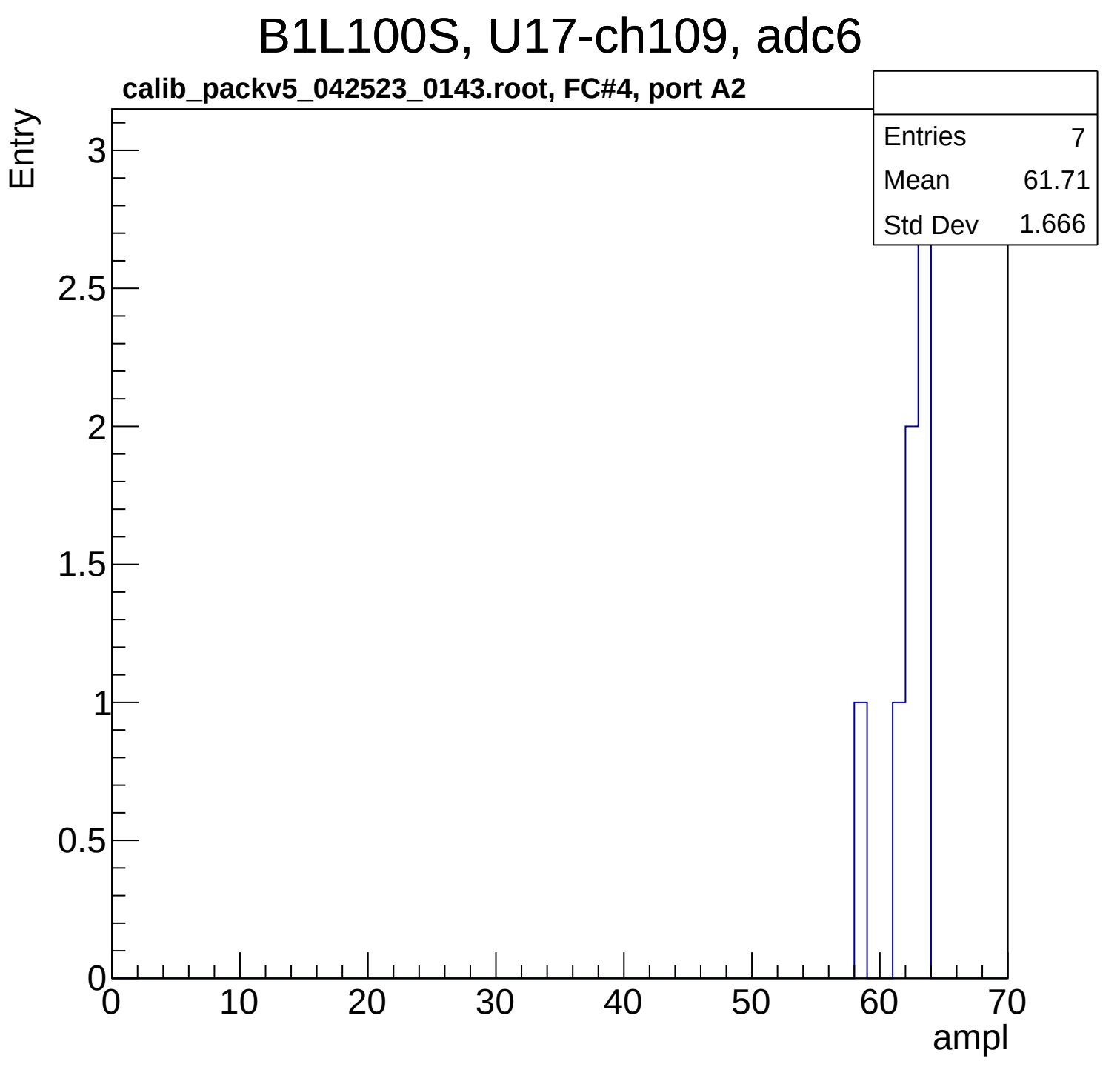
B1L100S, U17-ch109, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 7
Mean 61.71
Std Dev 1.666
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
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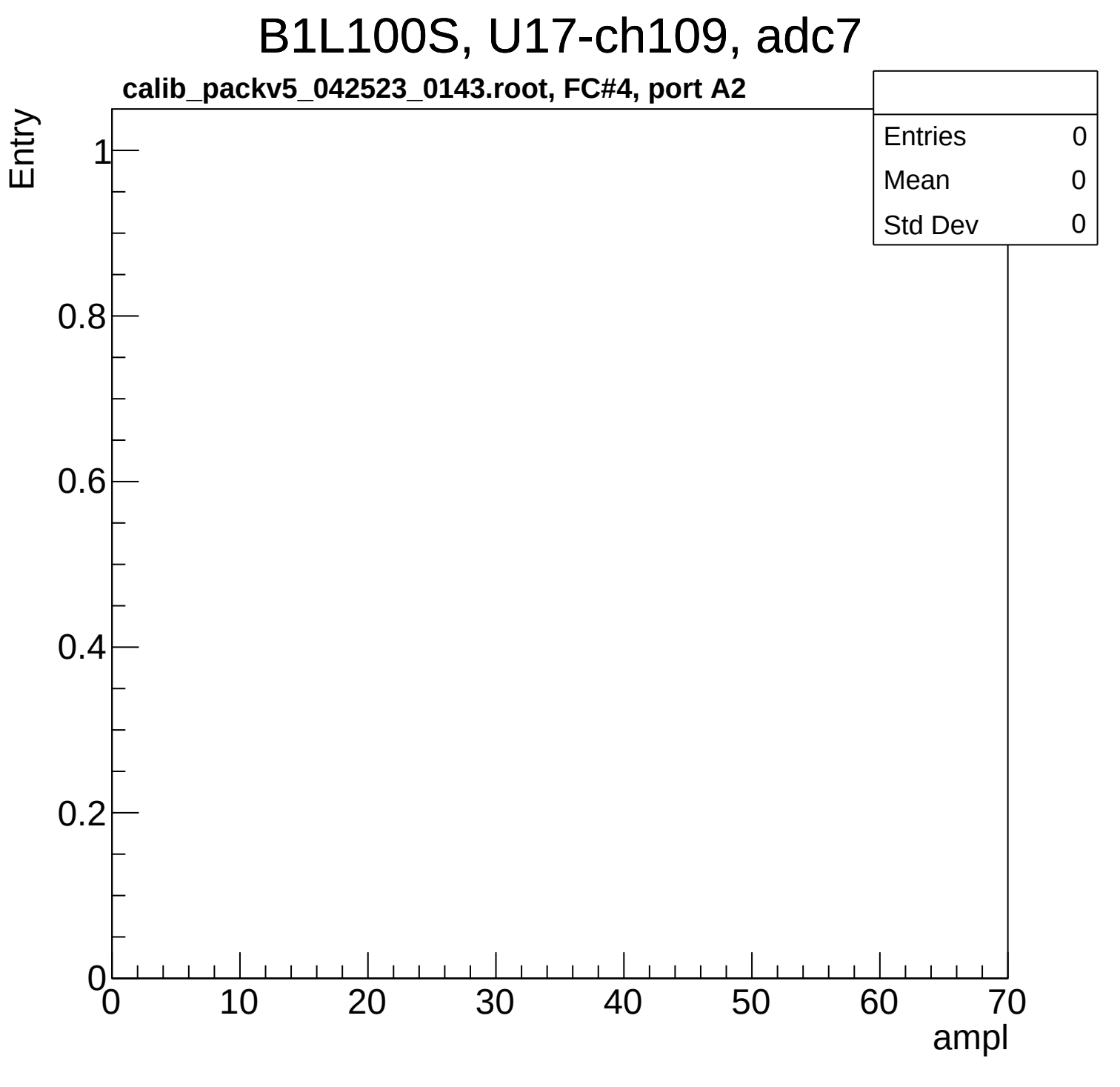
B1L100S, U17-ch109, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
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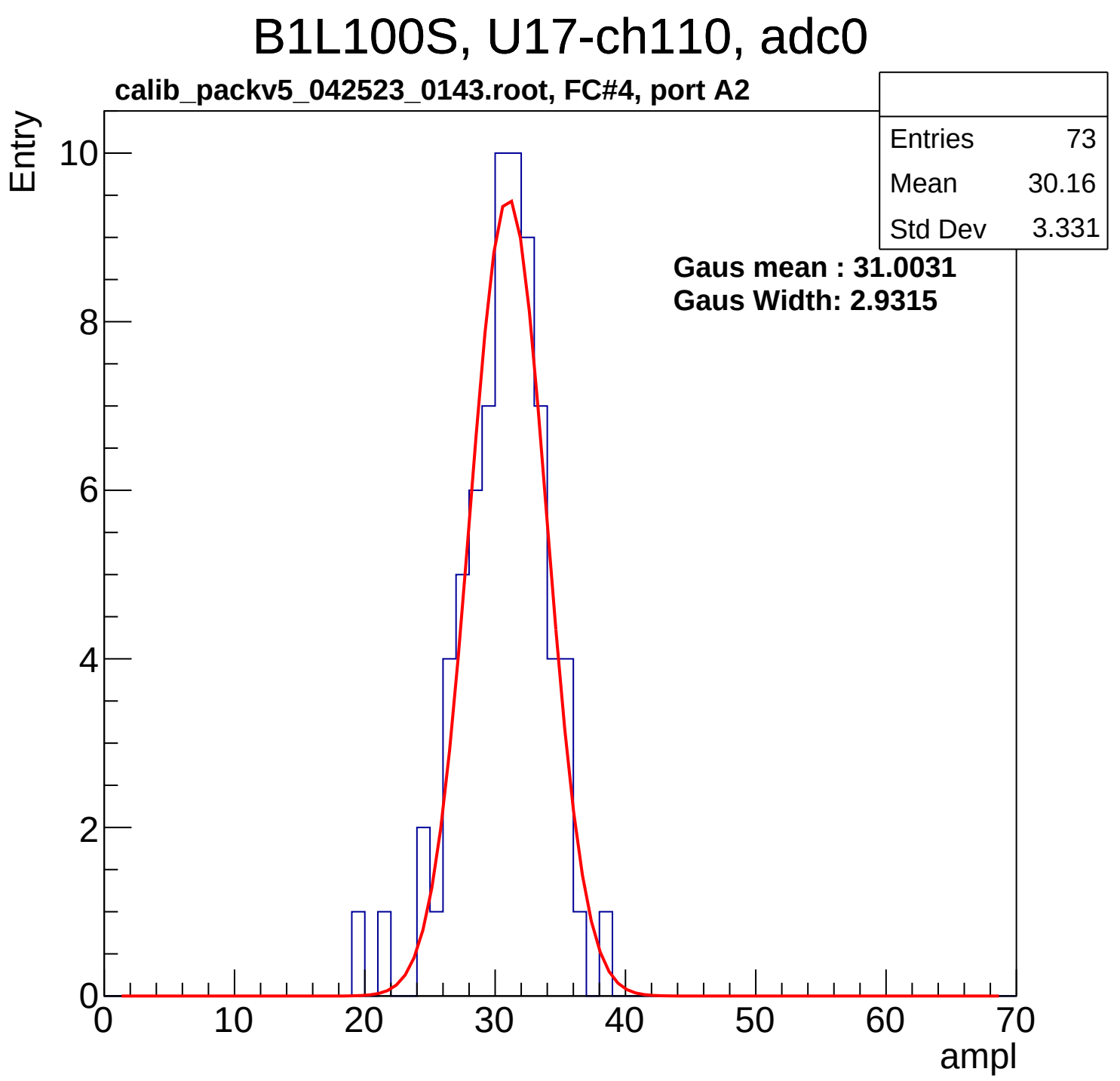
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch110, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 30.16
Std Dev 3.331
Gaus mean : 31.0031
Gaus Width: 2.9315
Entry
ampl
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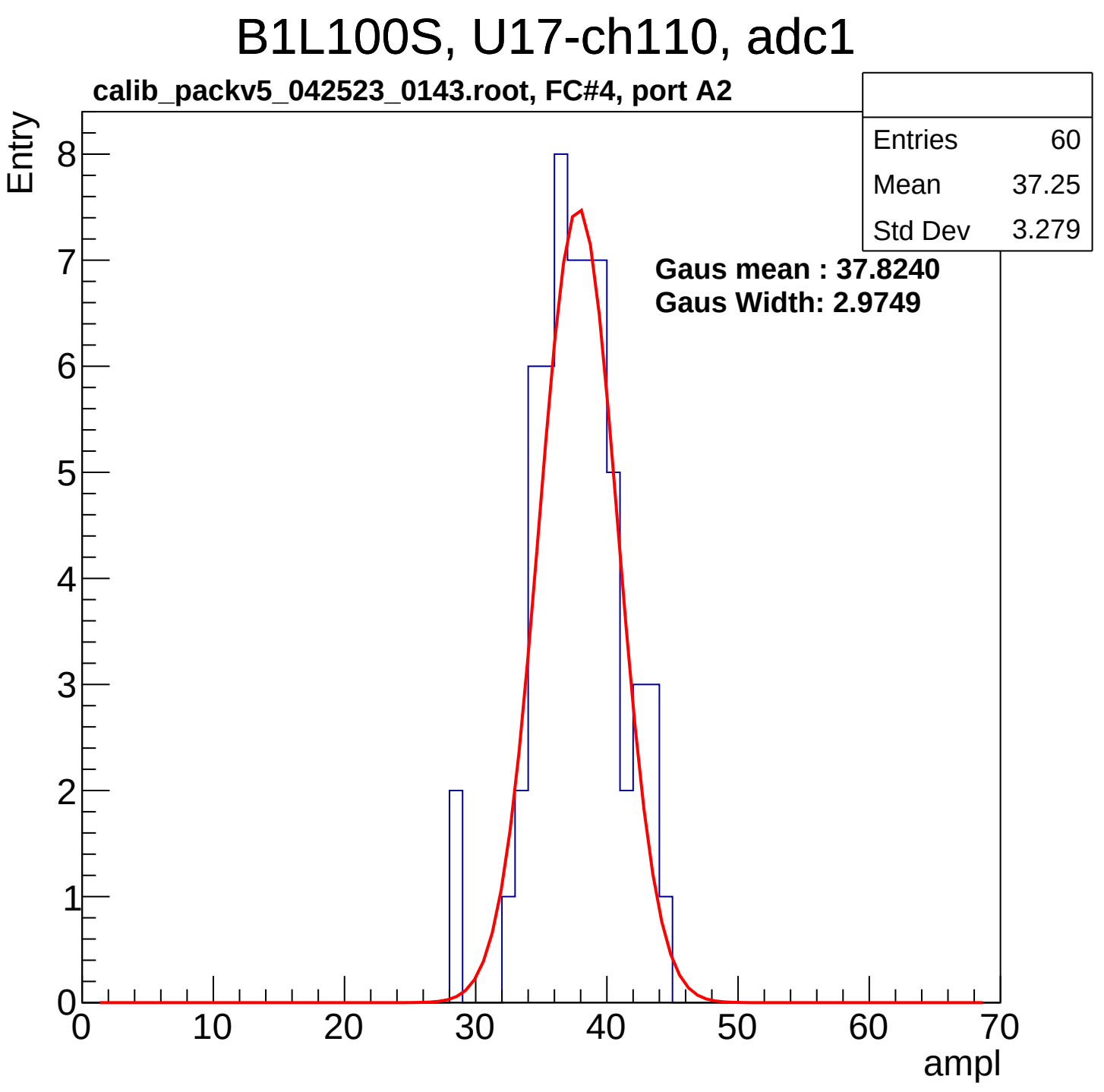
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U17-ch110, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 37.25
Std Dev 3.279
Gaus mean : 37.8240
Gaus Width: 2.9749
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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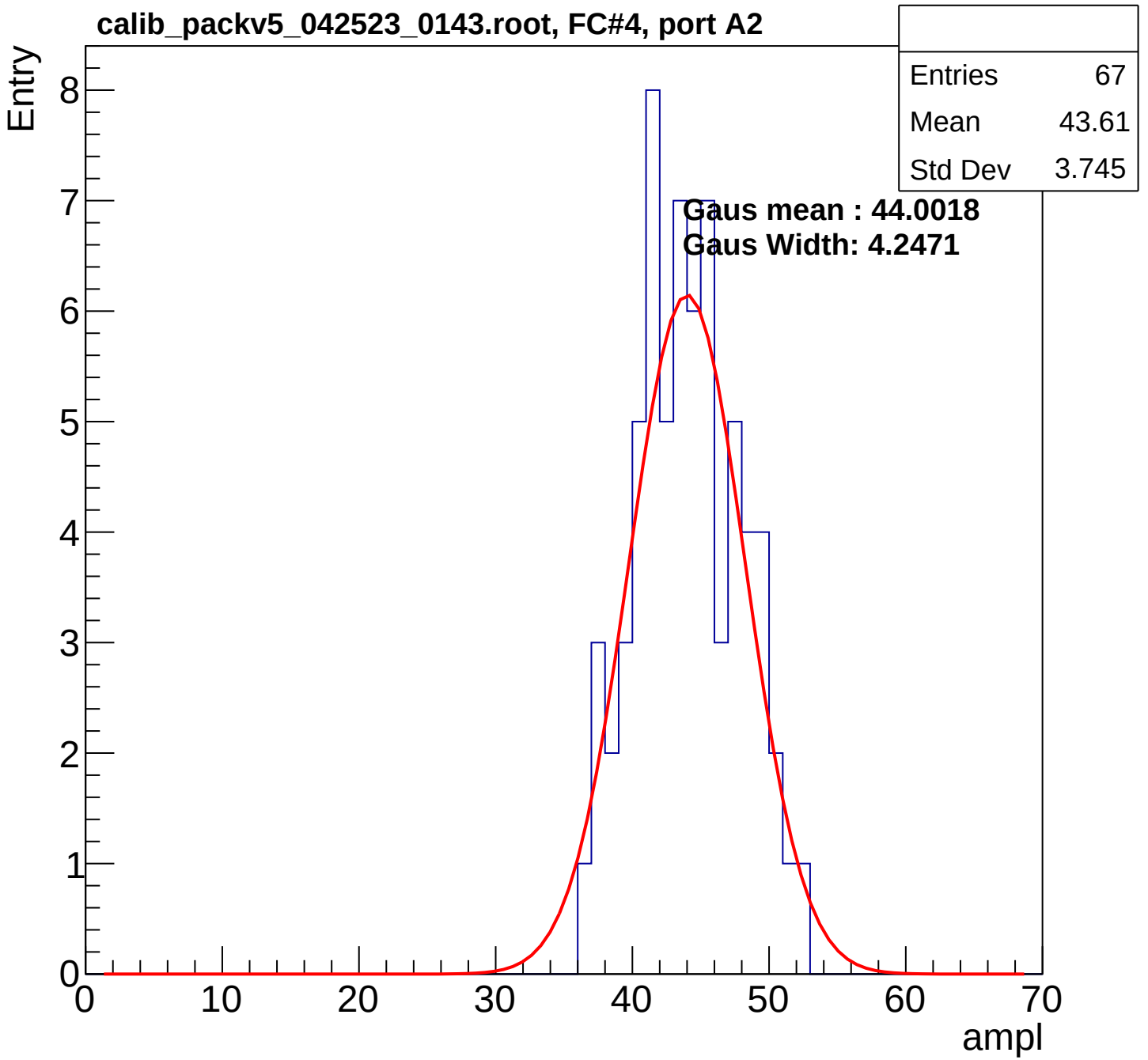
B1L100S, U17-ch110, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 43.61
Std Dev 3.745
Gaus mean : 44.0018
Gaus Width: 4.2471
Entry
ampl
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0
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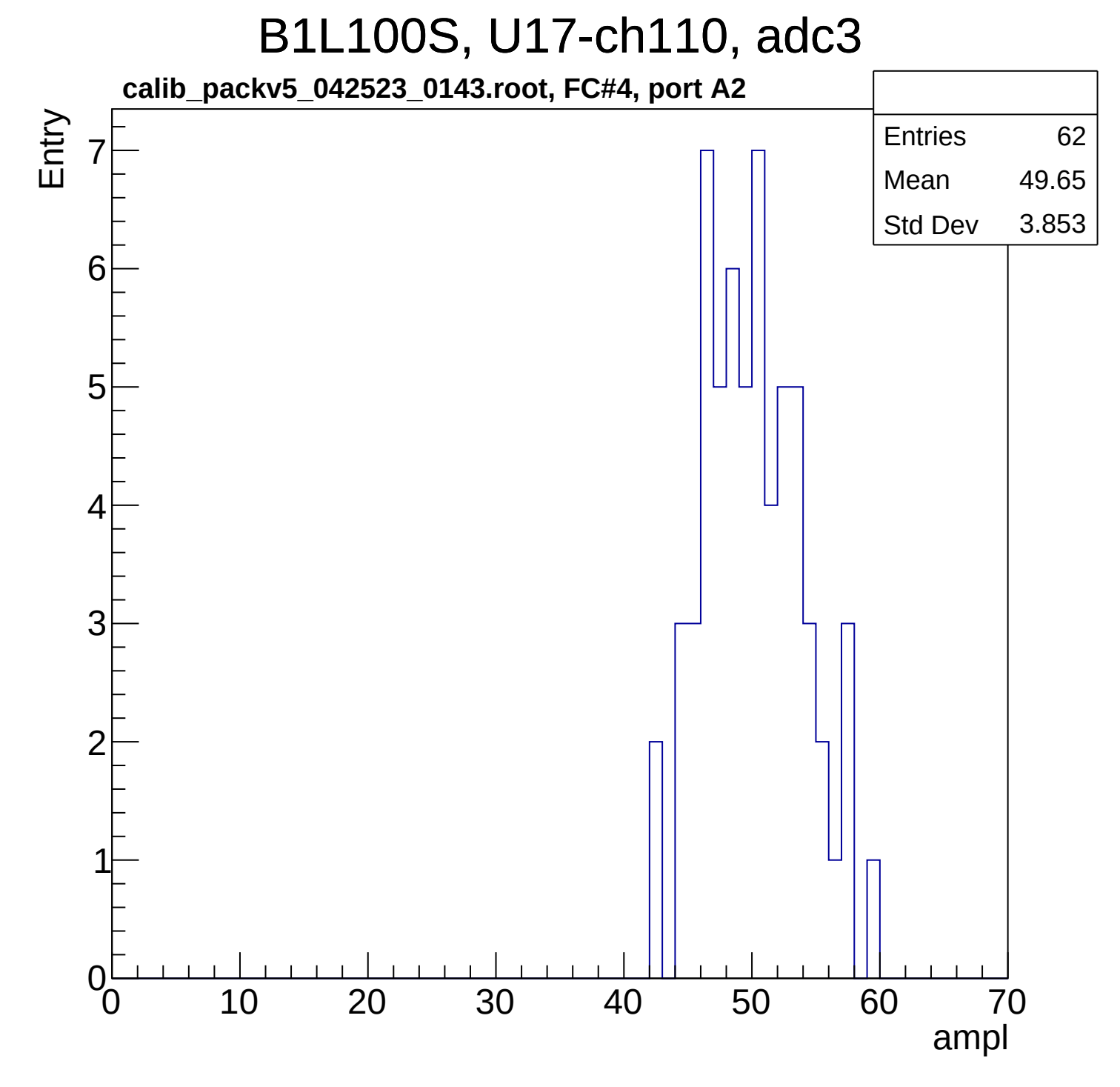
B1L100S, U17-ch110, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 49.65
Std Dev 3.853
Entry
ampl
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0
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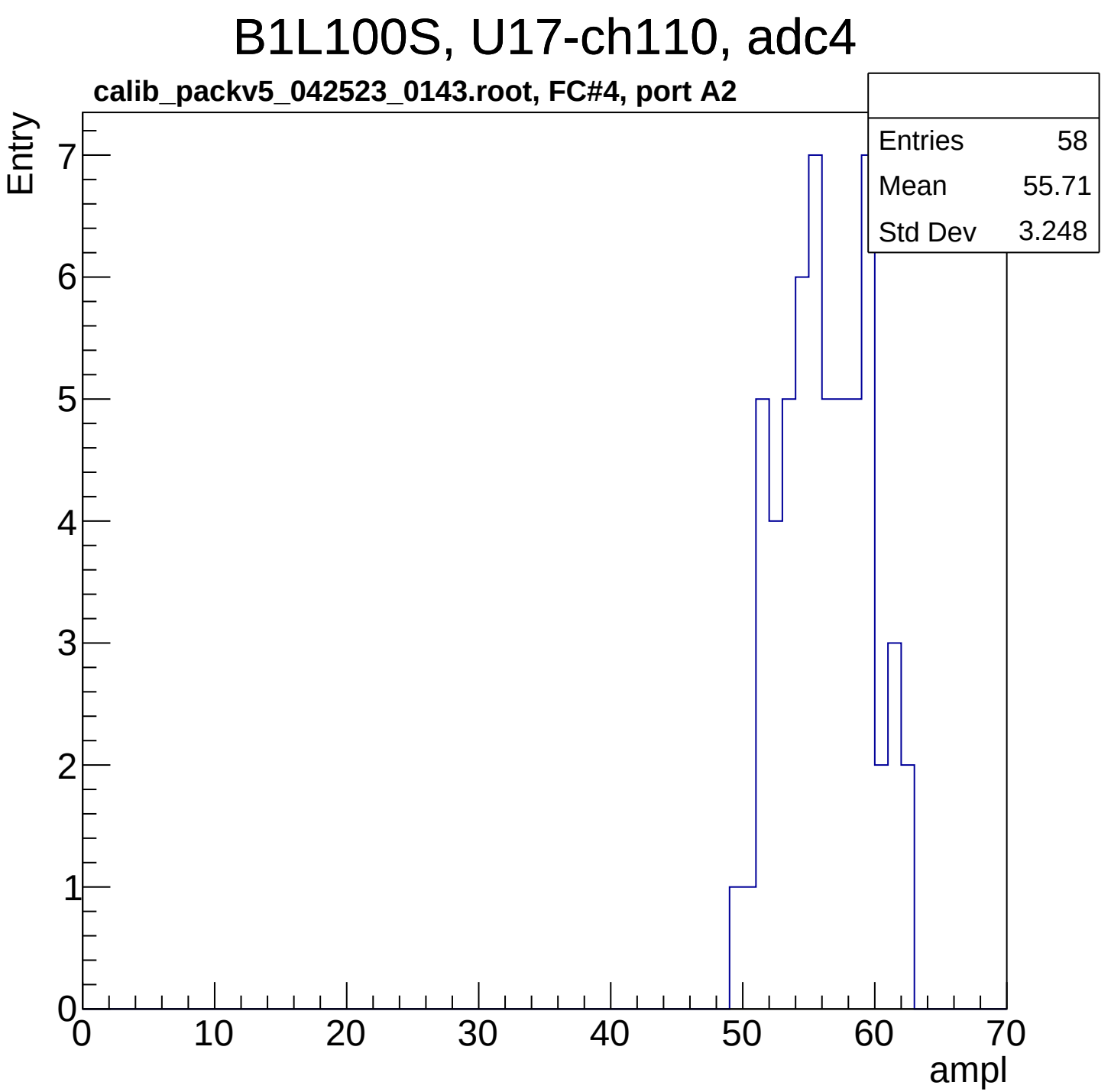
B1L100S, U17-ch110, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 55.71
Std Dev 3.248
Entry
ampl
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0
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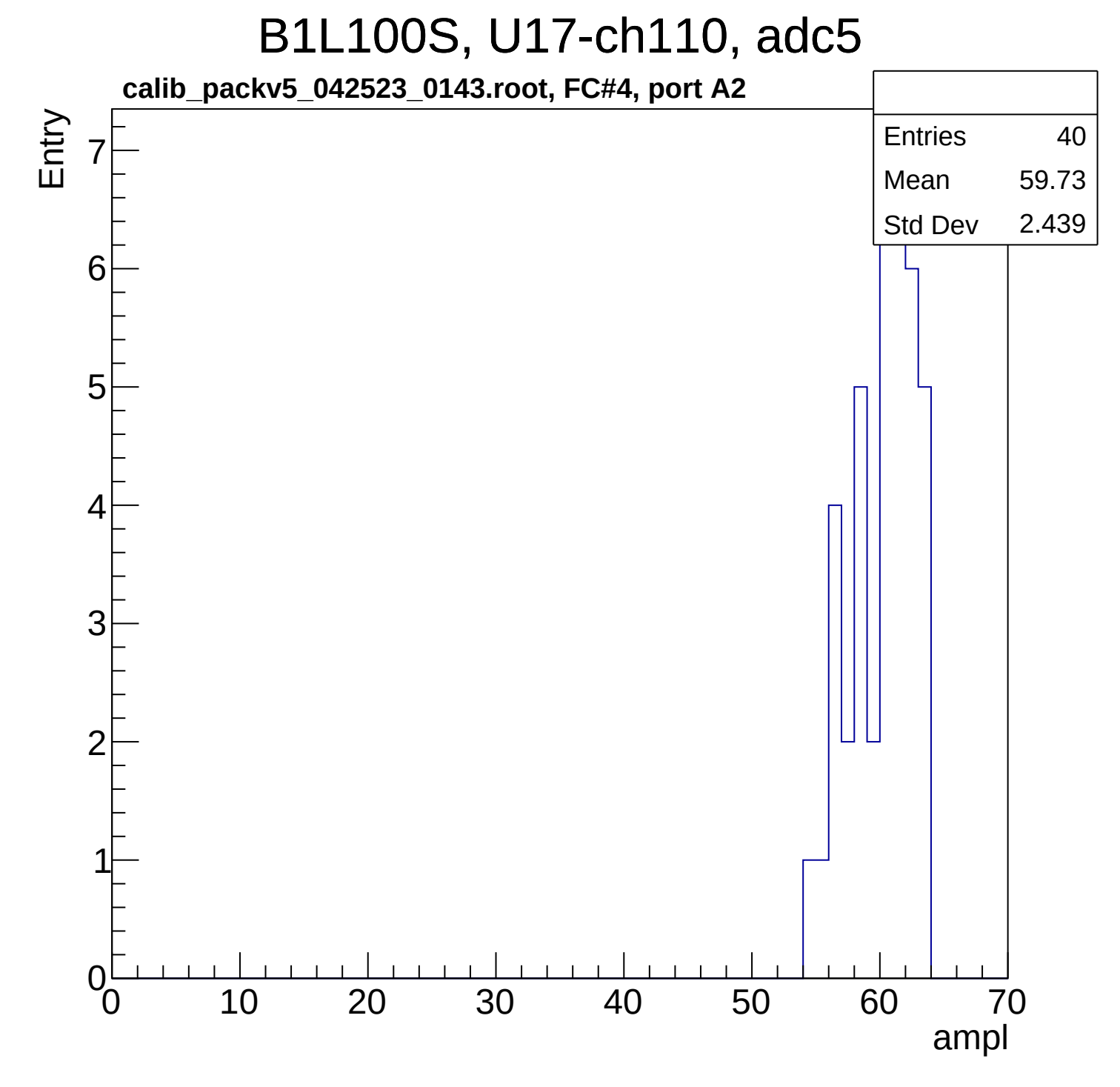
B1L100S, U17-ch110, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 40
Mean 59.73
Std Dev 2.439
Entry
ampl
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4
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0
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60
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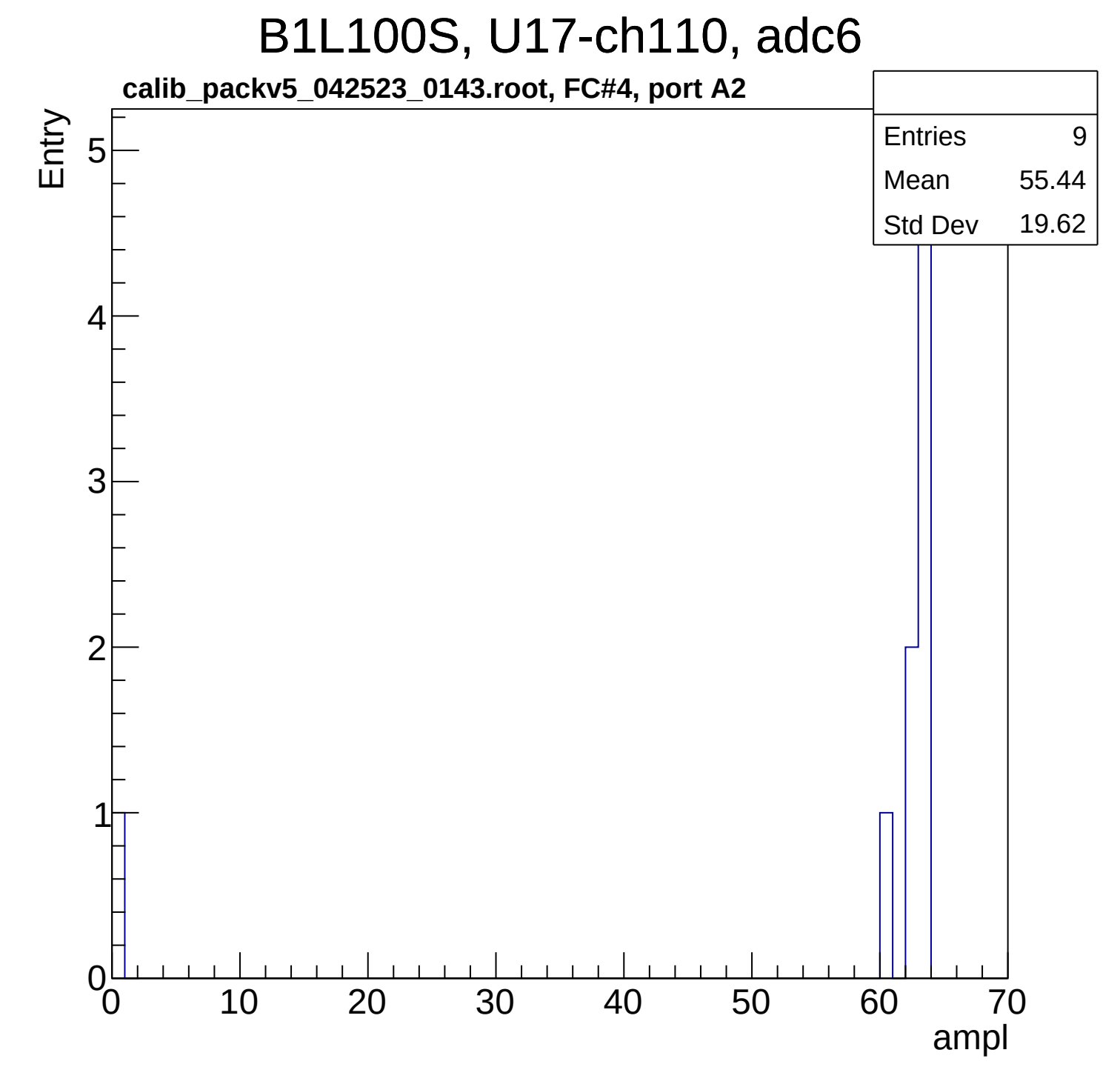
B1L100S, U17-ch110, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 9
Mean 55.44
Std Dev 19.62
Entry
ampl
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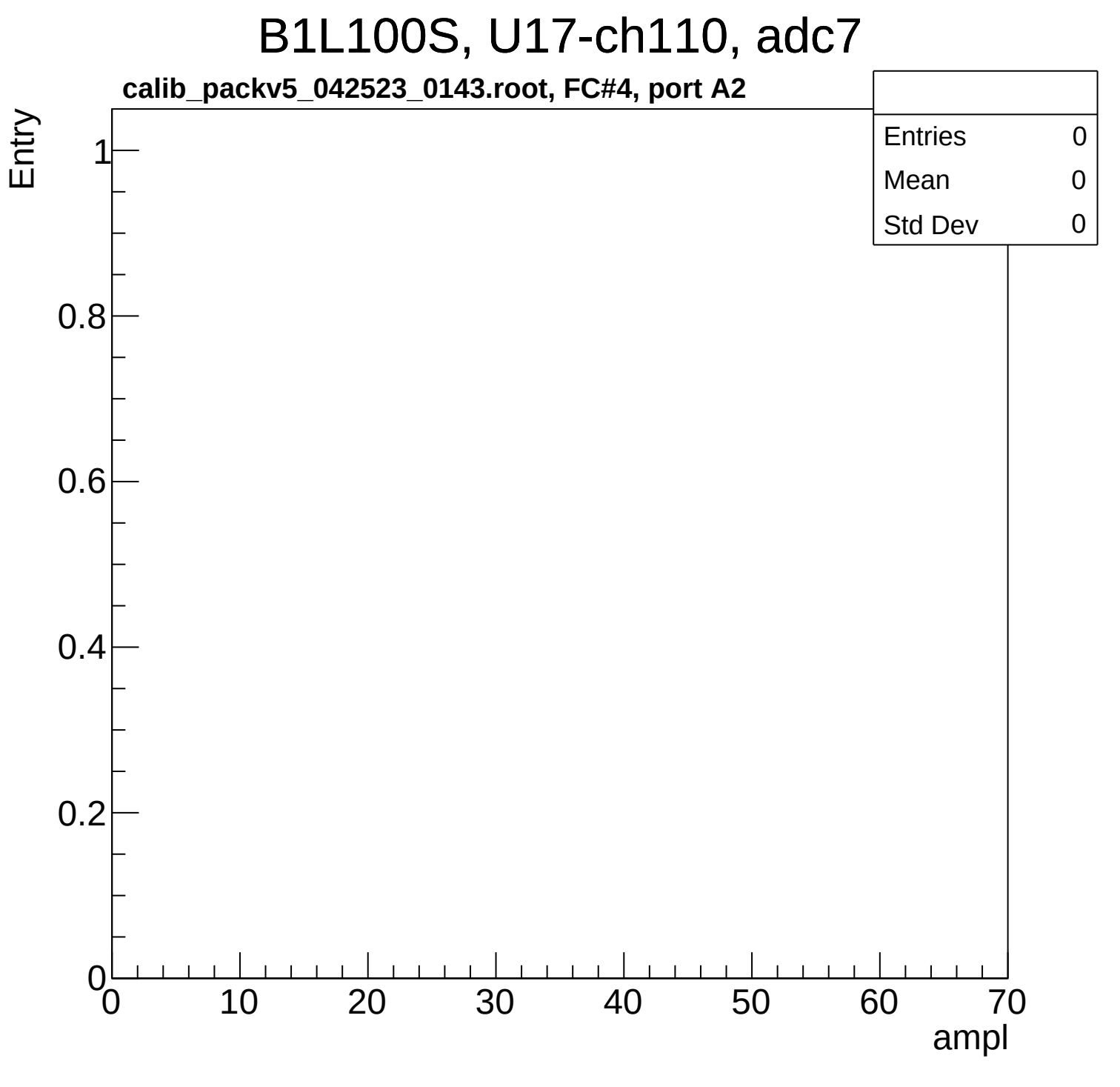
B1L100S, U17-ch110, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
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10
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50
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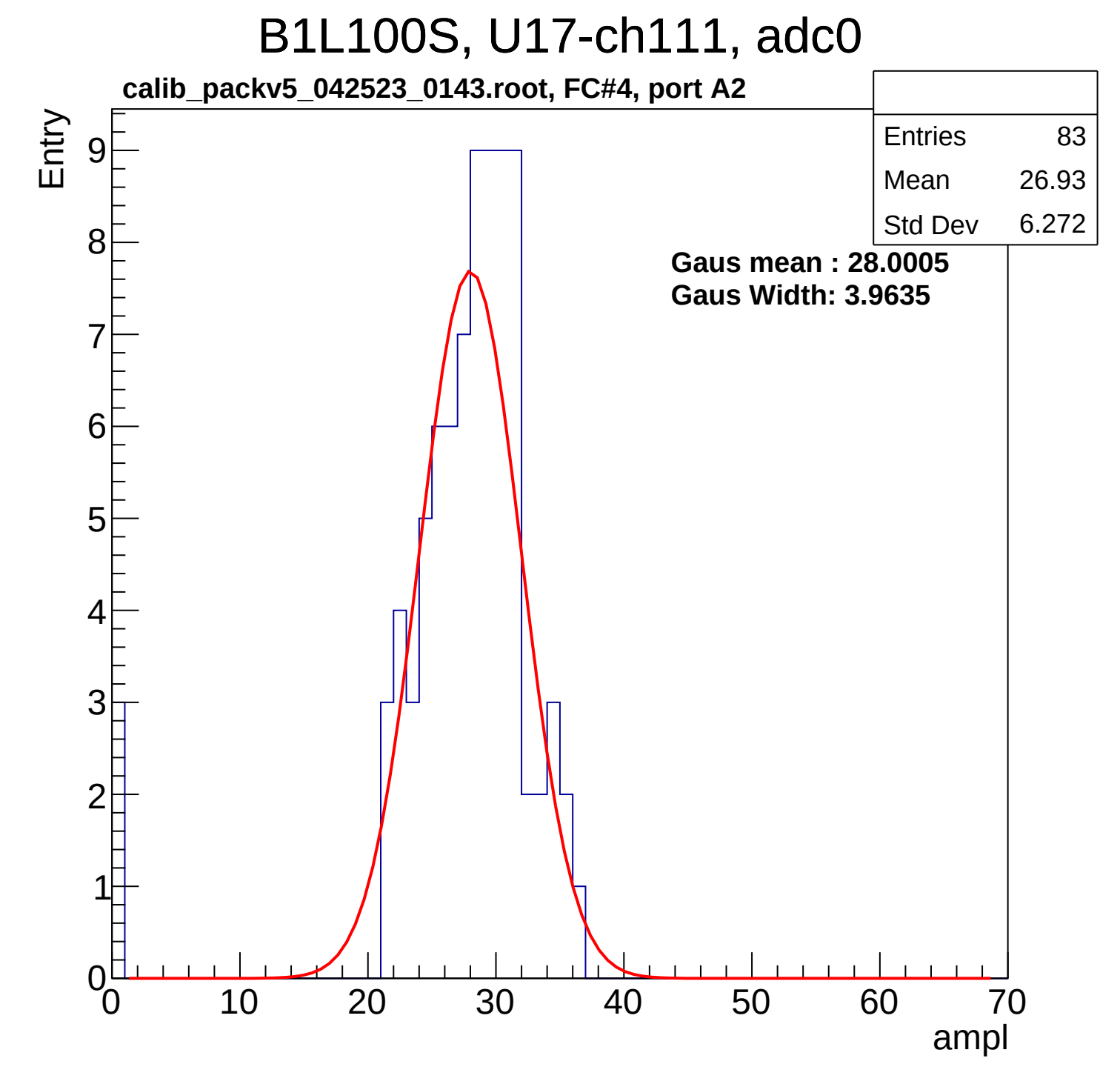
70
ampl


B1L100S, U17-ch111, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 83
Mean 26.93
Std Dev 6.272
Gaus mean : 28.0005
Gaus Width: 3.9635
Entry
ampl
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3
4
5
6
7
8
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0
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40
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60
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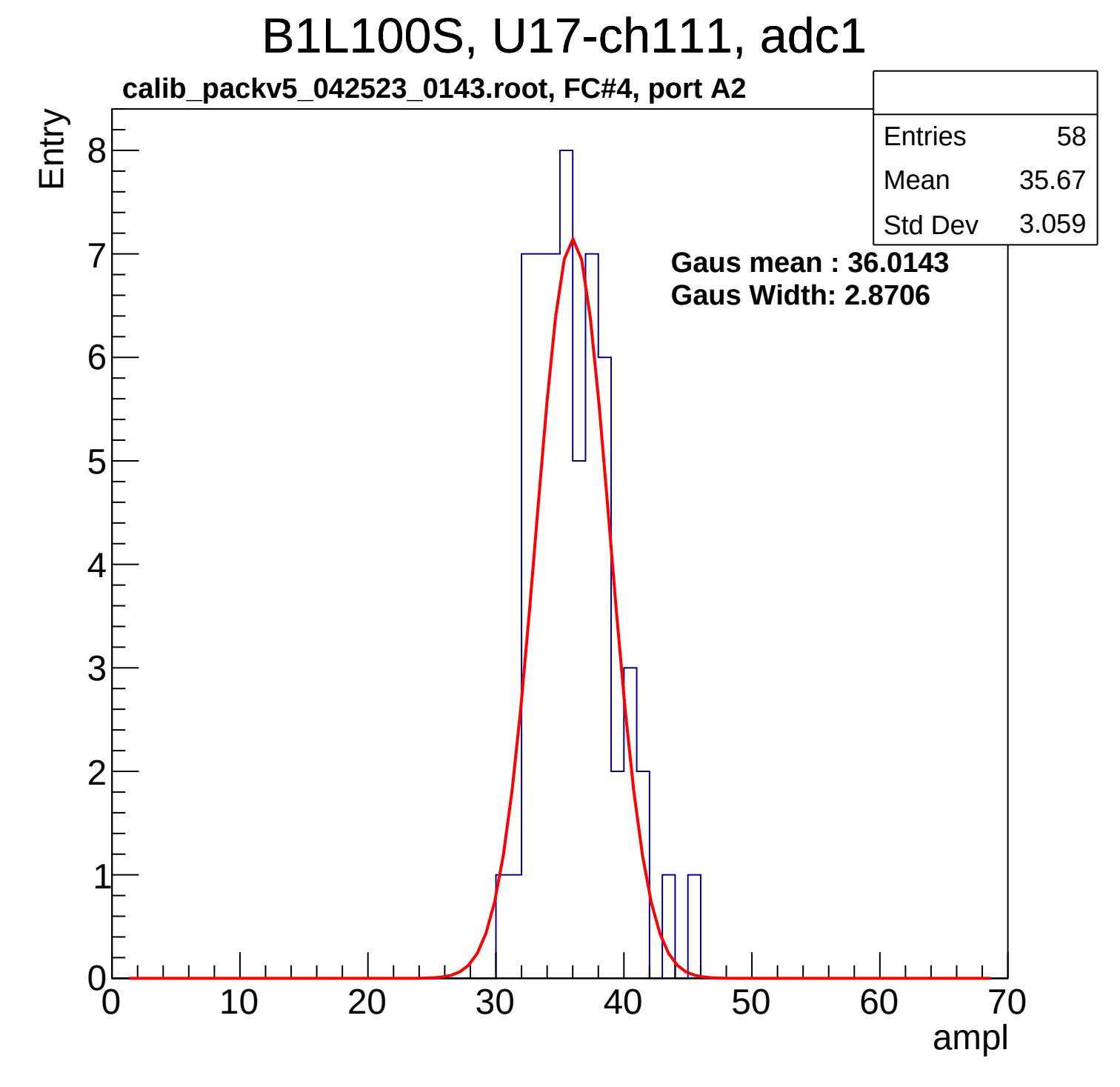
B1L100S, U17-ch111, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 35.67
Std Dev 3.059
Gaus mean : 36.0143
Gaus Width: 2.8706
Entry
ampl
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2
3
4
5
6
7
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0
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60
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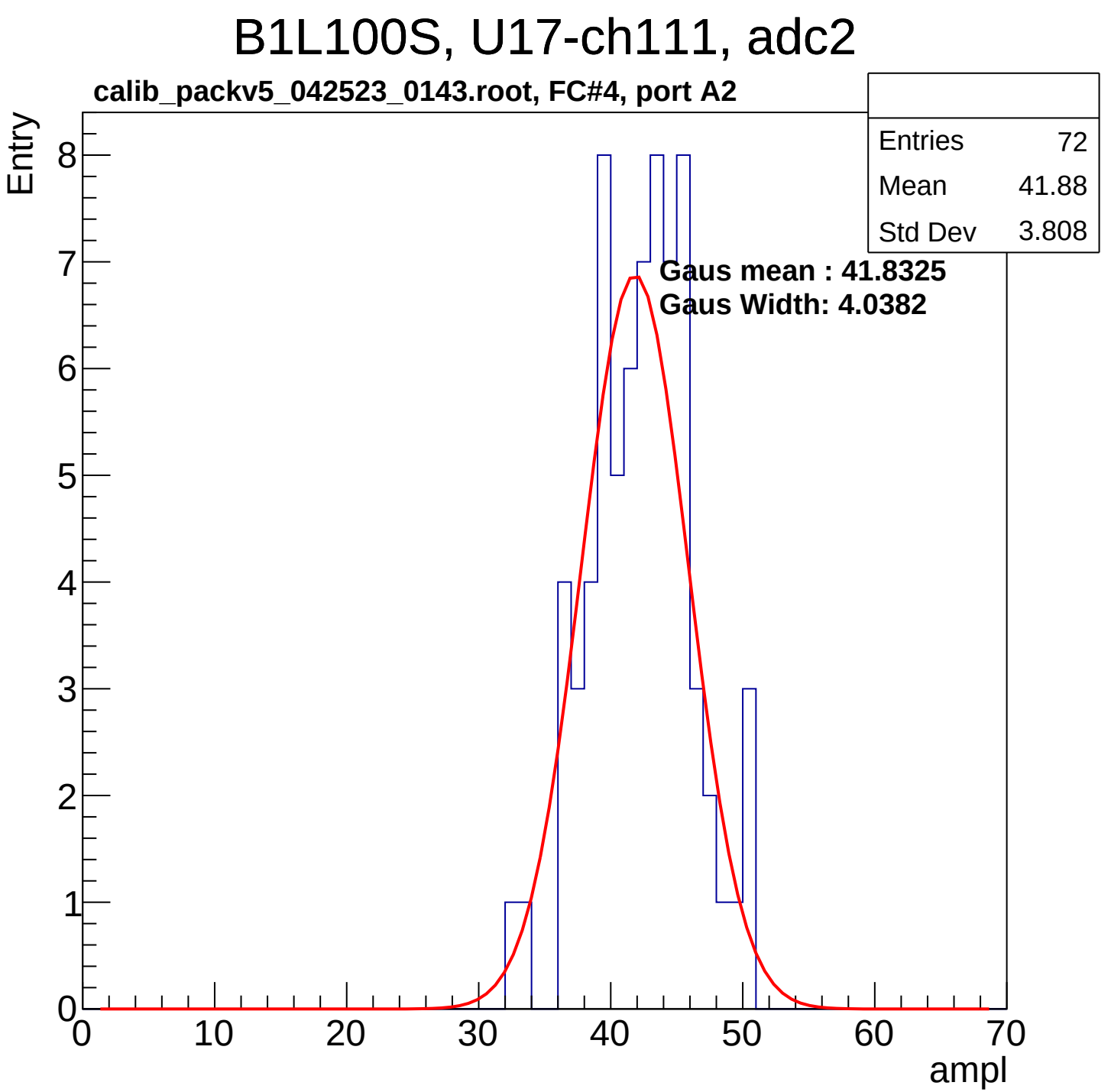
B1L100S, U17-ch111, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 41.88
Std Dev 3.808
Gaus mean : 41.8325
Gaus Width: 4.0382
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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60
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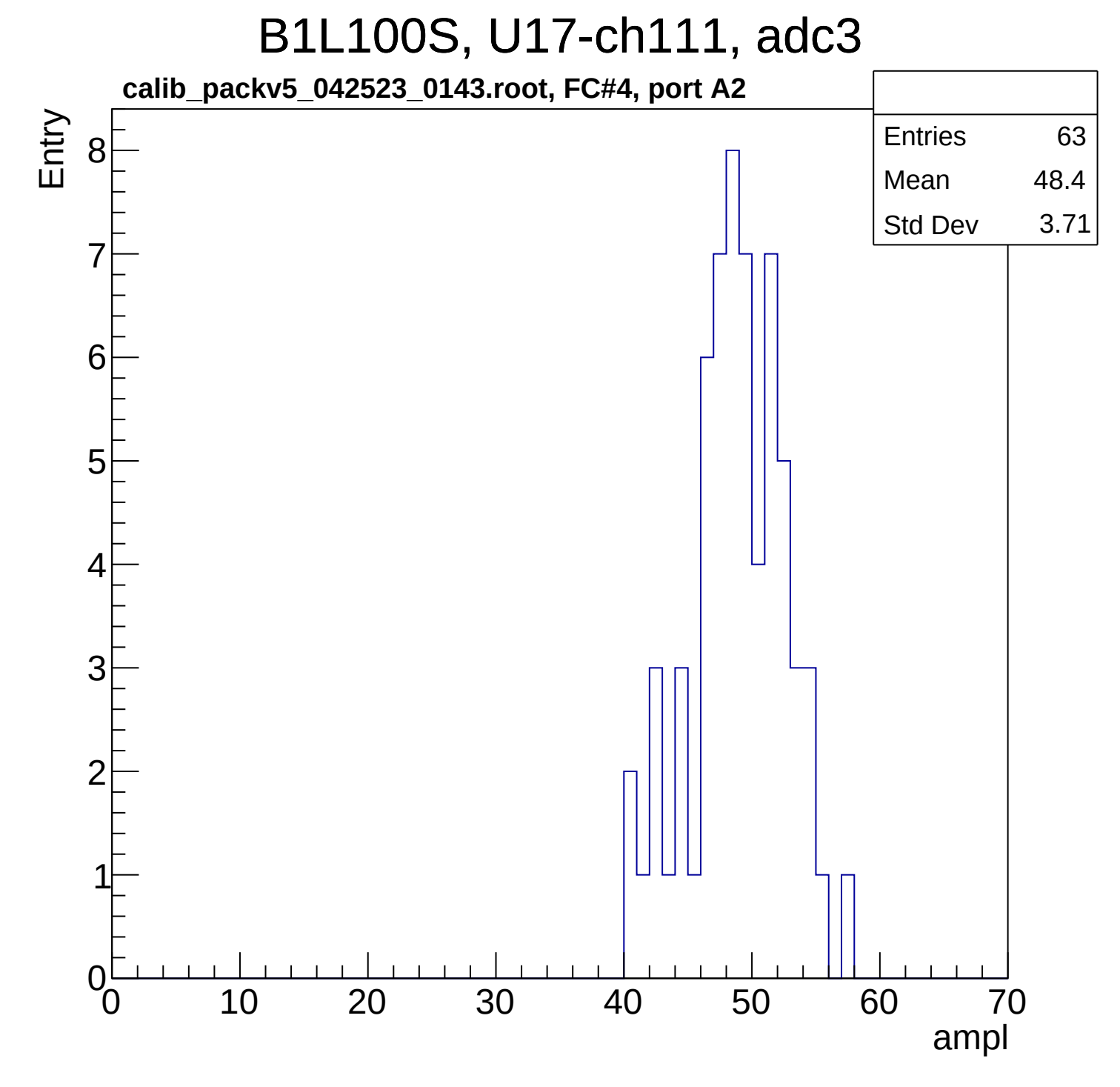
B1L100S, U17-ch111, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 48.4
Std Dev 3.71
Entry
ampl
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3
4
5
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0
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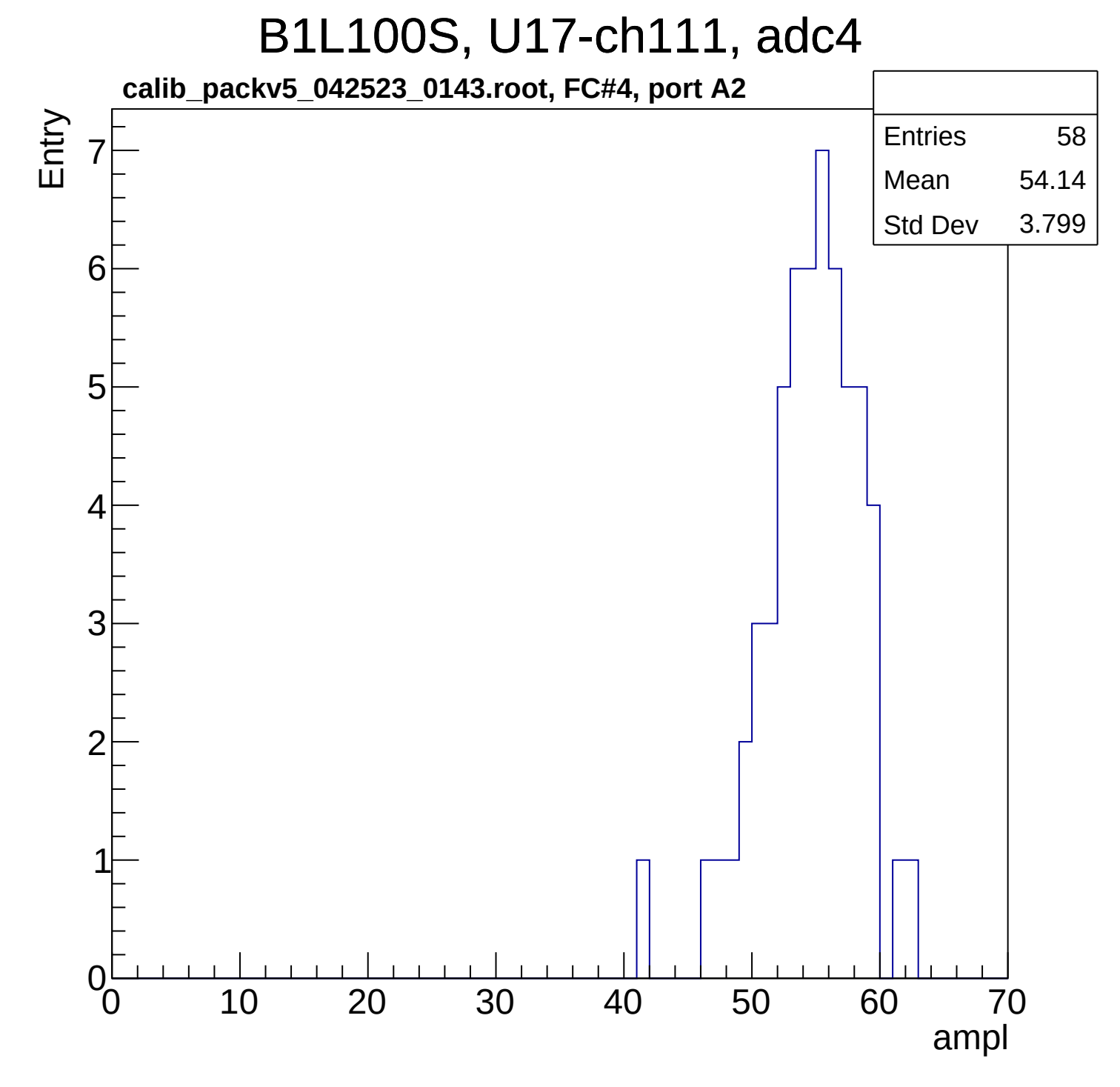
B1L100S, U17-ch111, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 54.14
Std Dev 3.799
Entry
ampl
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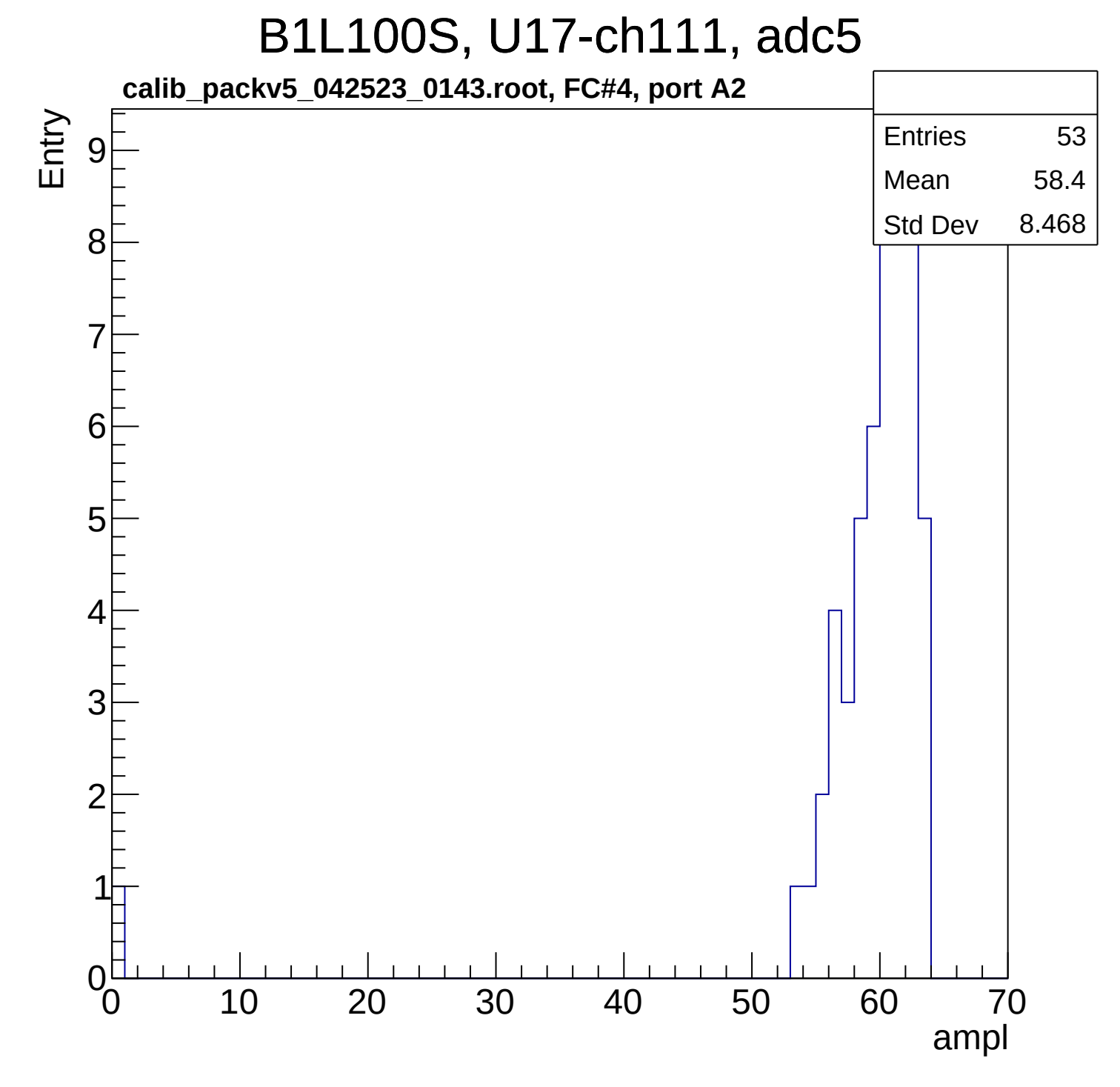
B1L100S, U17-ch111, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 58.4
Std Dev 8.468
Entry
ampl
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6
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0
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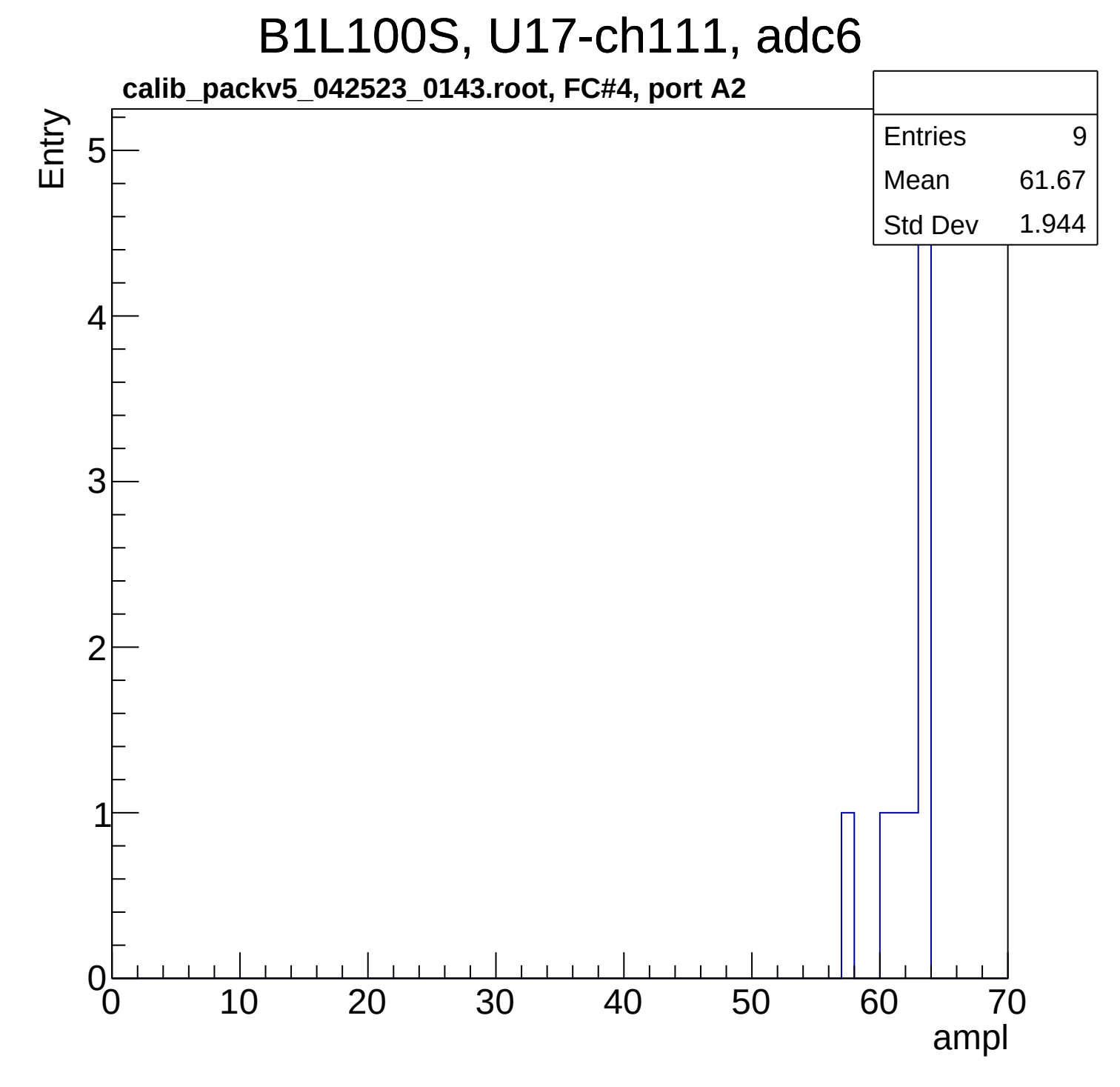
B1L100S, U17-ch111, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 9
Mean 61.67
Std Dev 1.944
Entry
ampl
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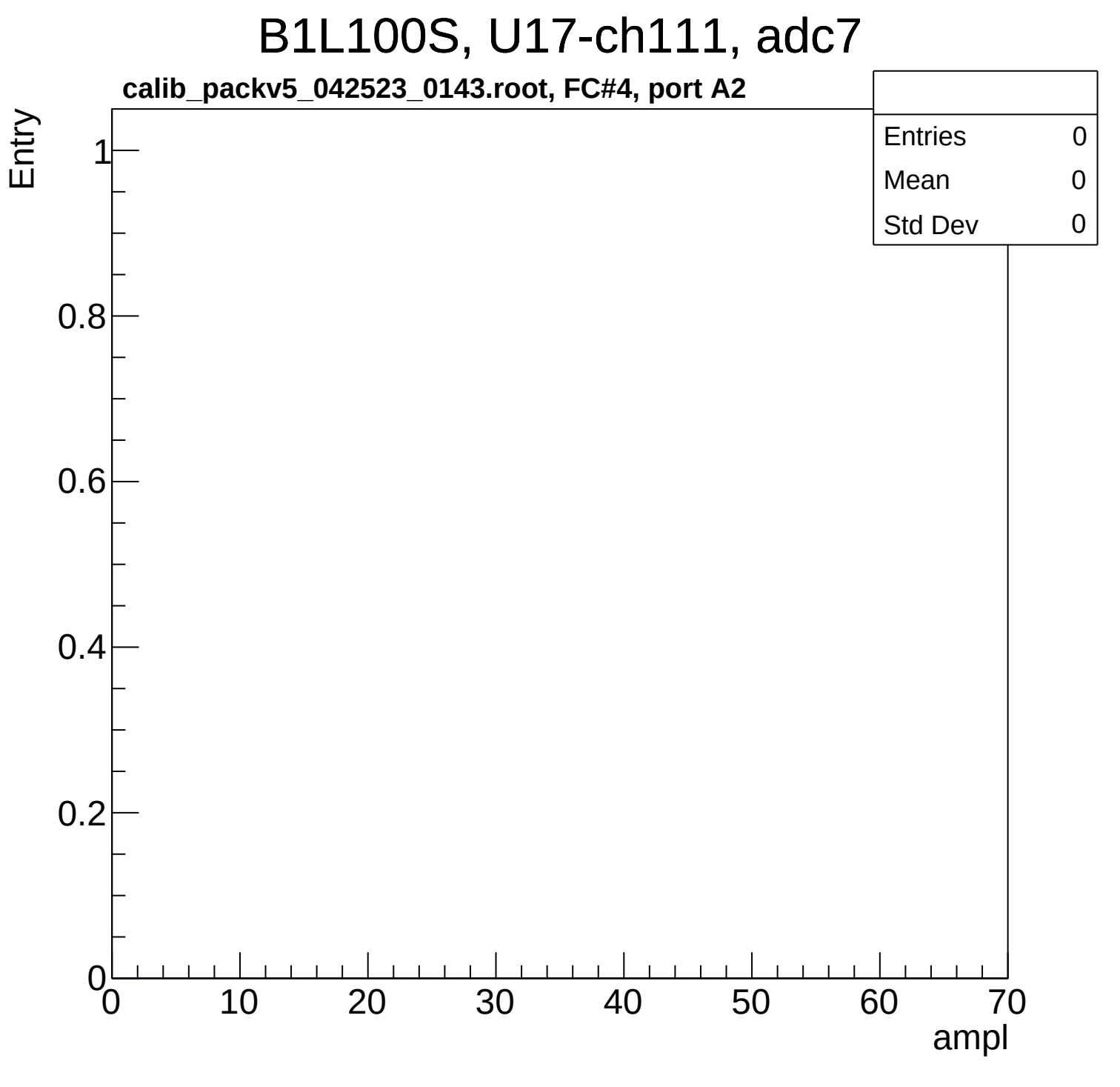
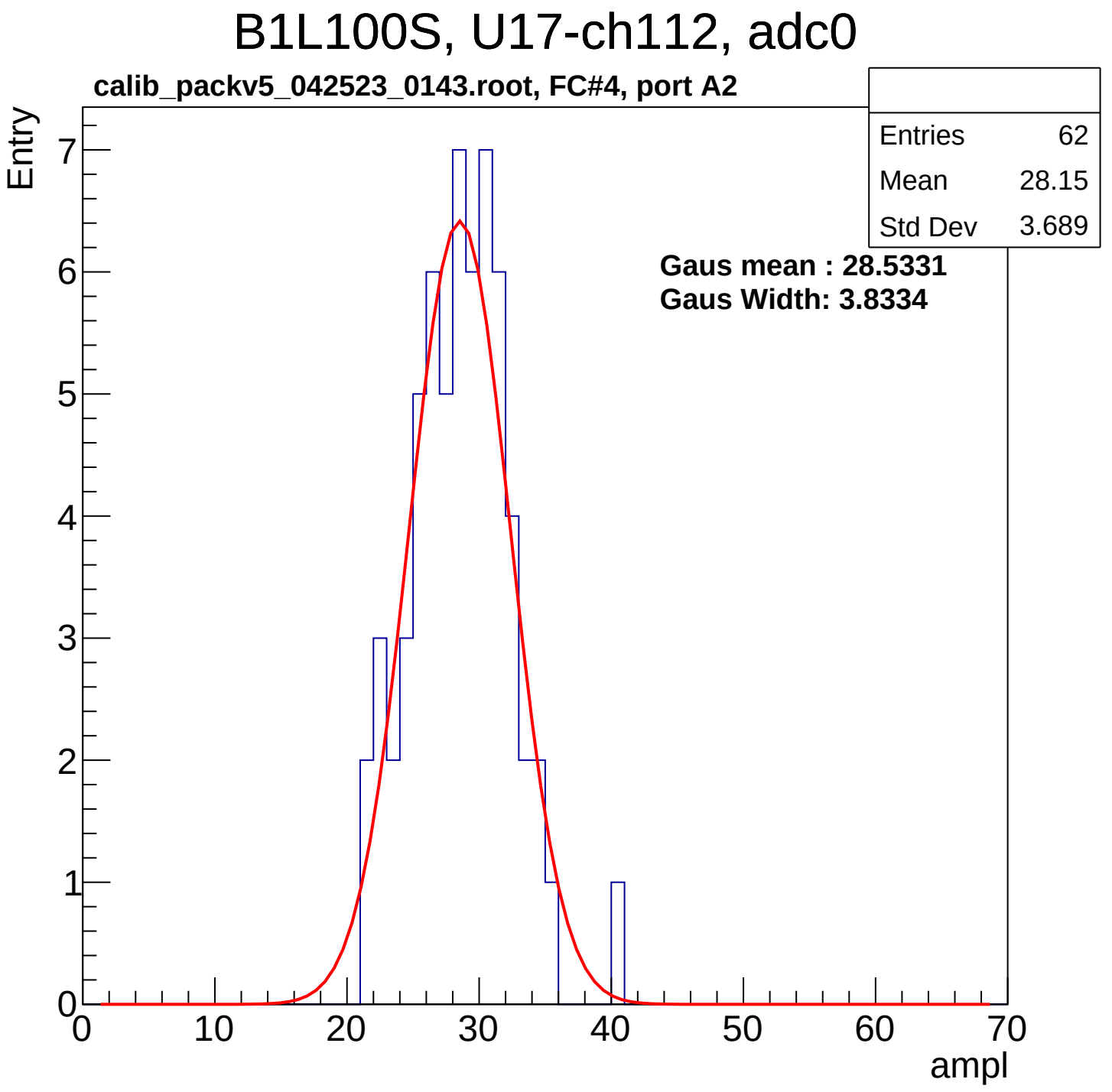
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L100S, U17-ch111, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch112, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 28.15
Std Dev 3.689
Gaus mean : 28.5331
Gaus Width: 3.8334
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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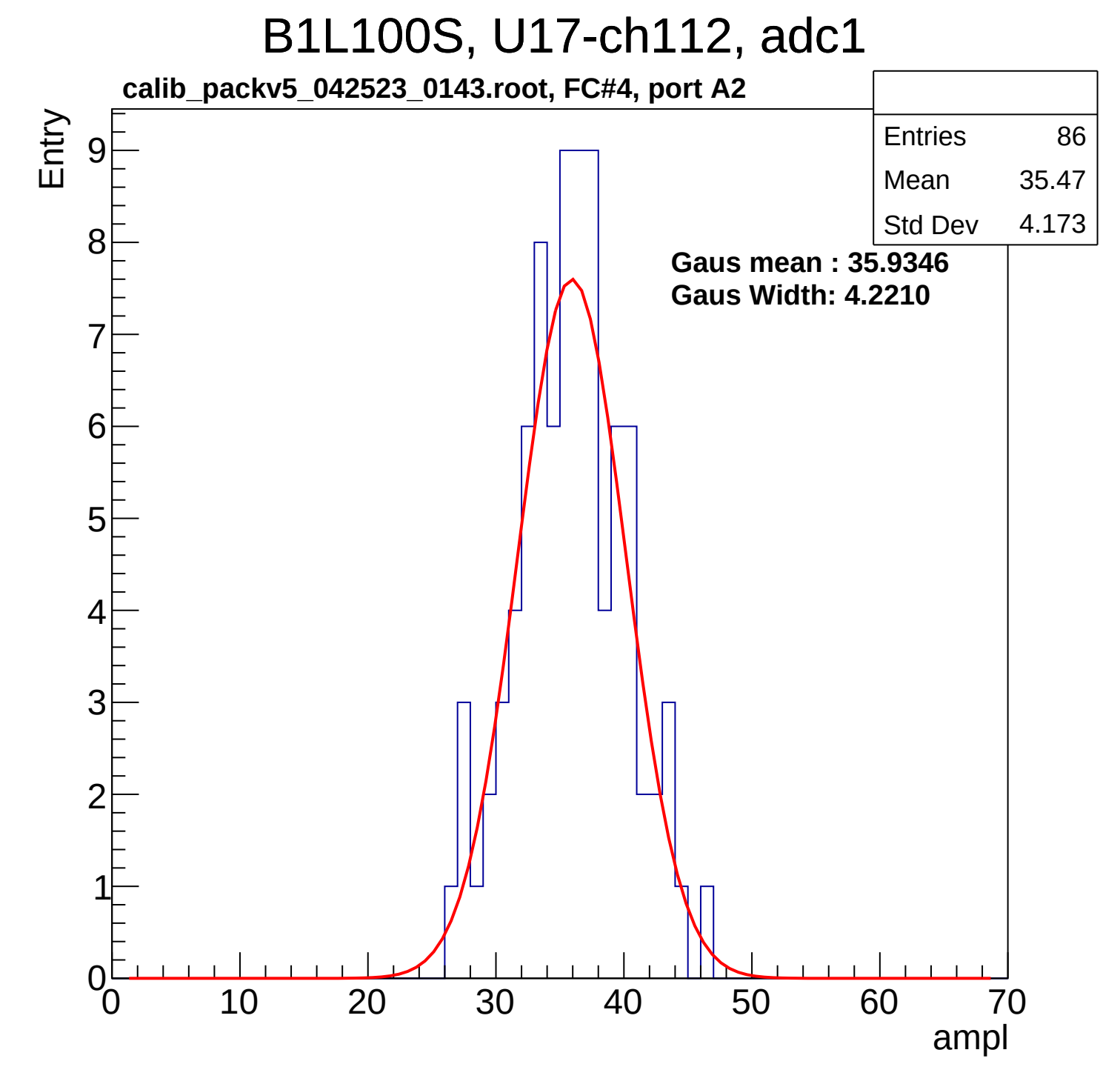
B1L100S, U17-ch112, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 86
Mean 35.47
Std Dev 4.173
Gaus mean : 35.9346
Gaus Width: 4.2210
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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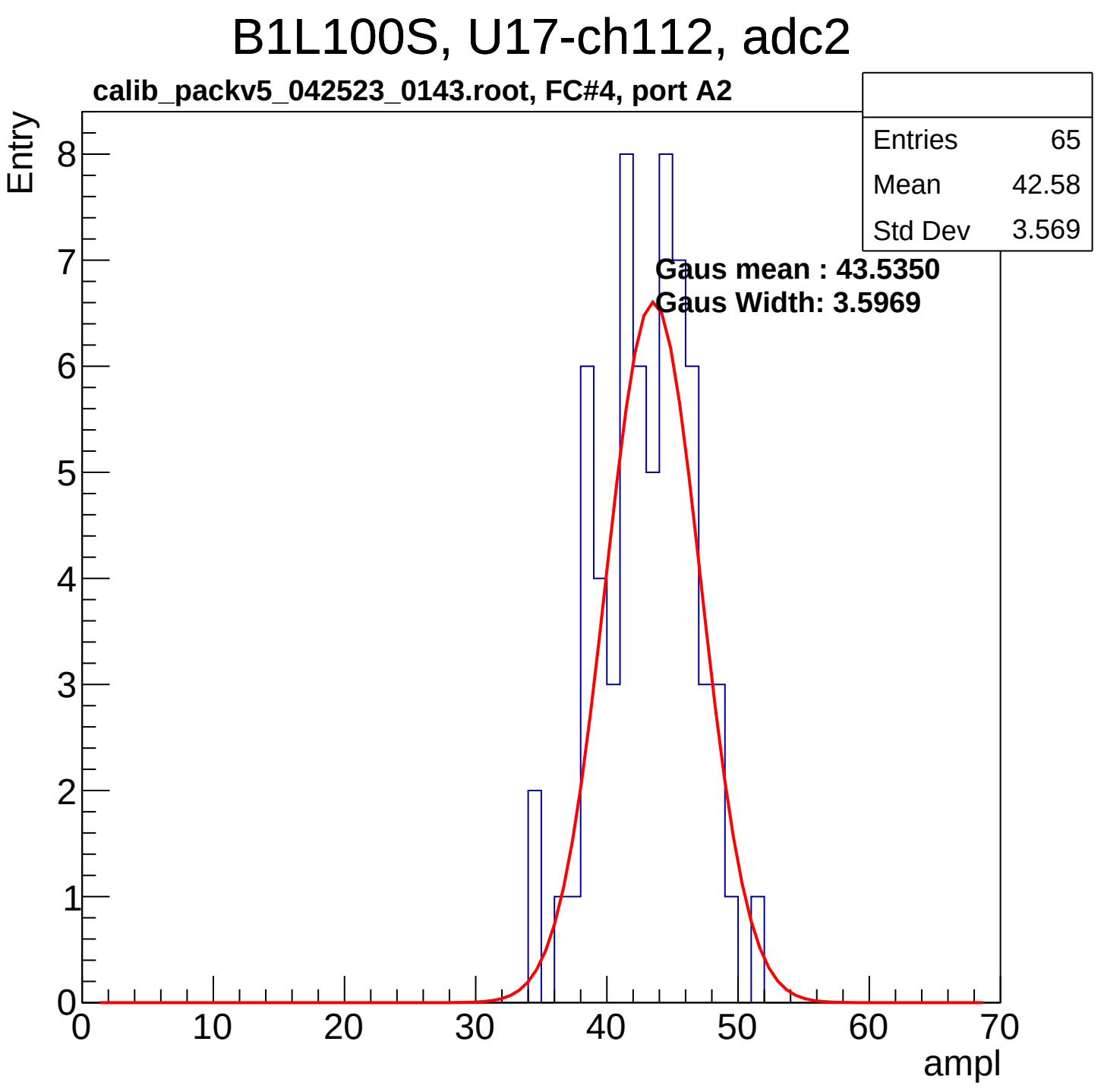
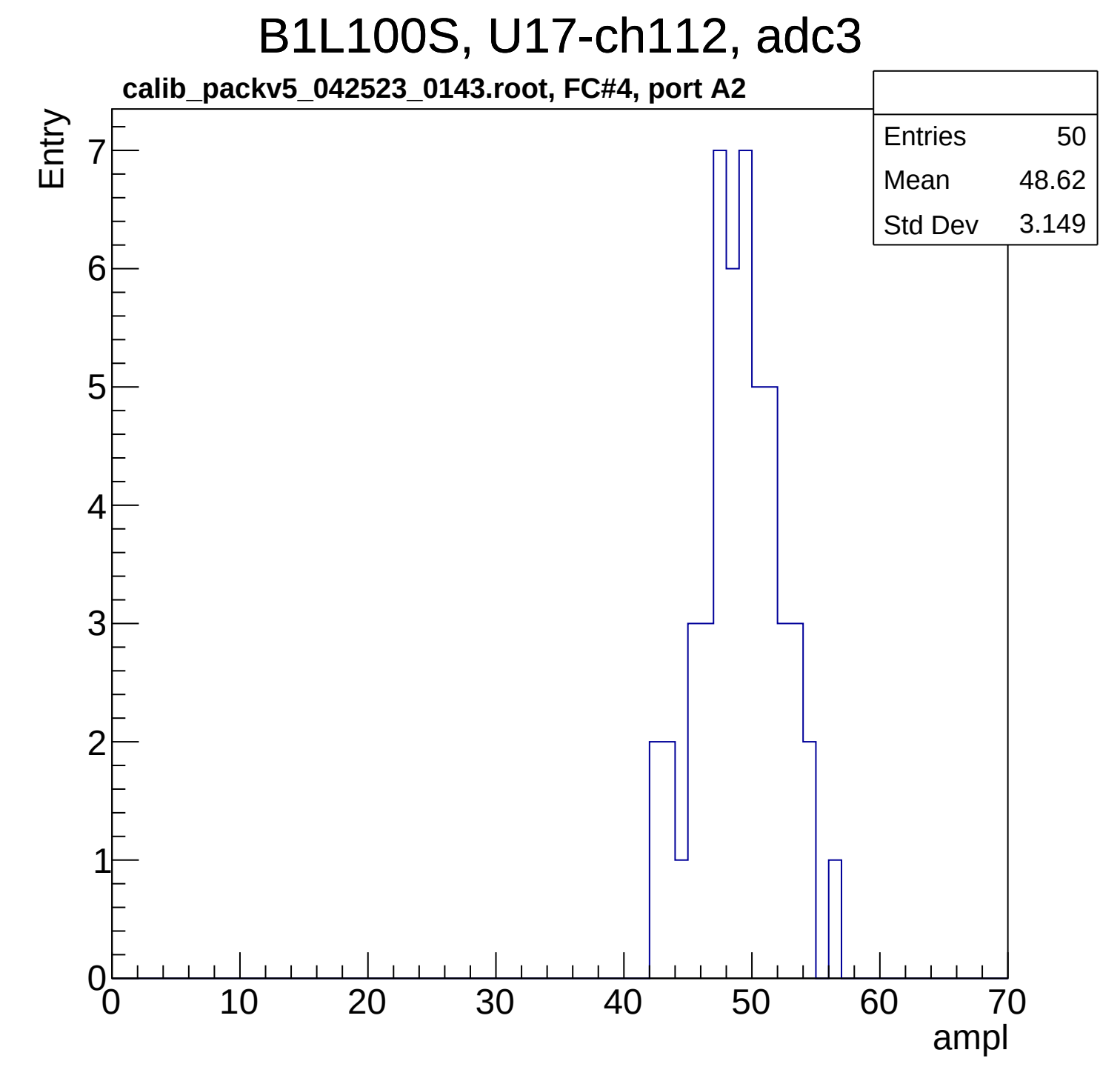

B1L100S, U17-ch112, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 42.58
Std Dev 3.569
Gaus mean : 43.5350
Gaus Width: 3.5969
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch112, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 48.62
Std Dev 3.149
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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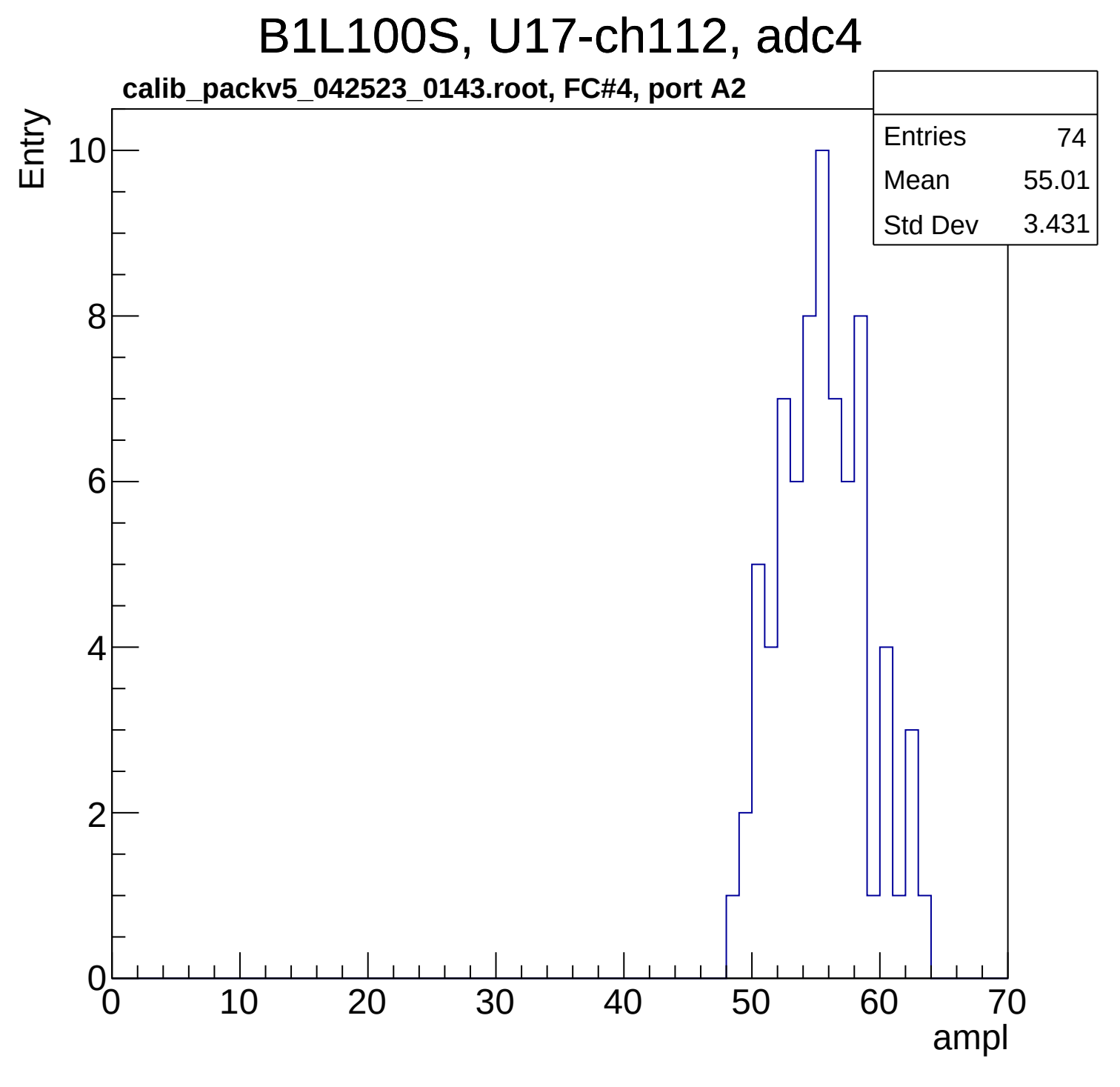
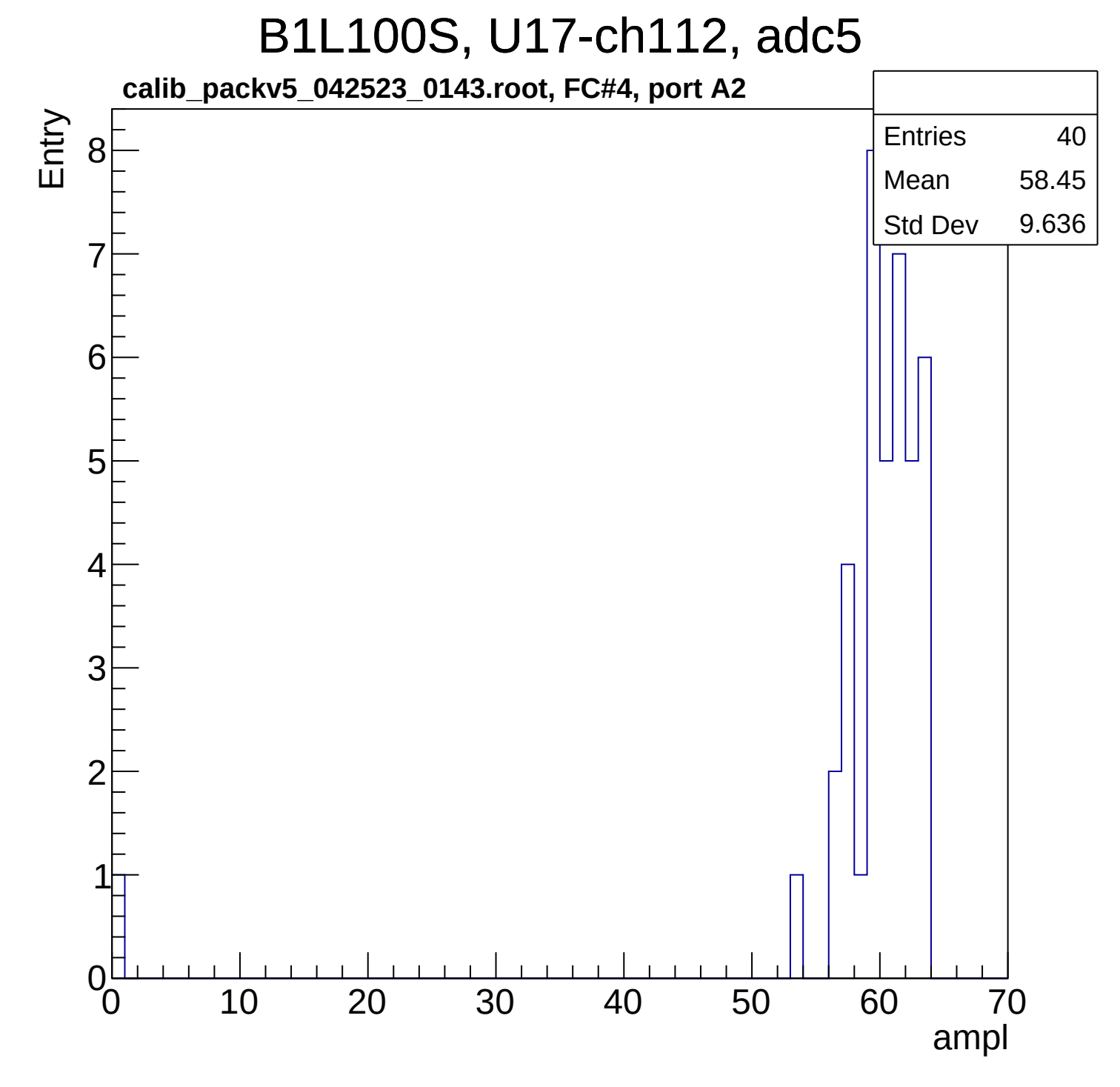

B1L100S, U17-ch112, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 74
Mean 55.01
Std Dev 3.431
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U17-ch112, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 40
Mean 58.45
Std Dev 9.636
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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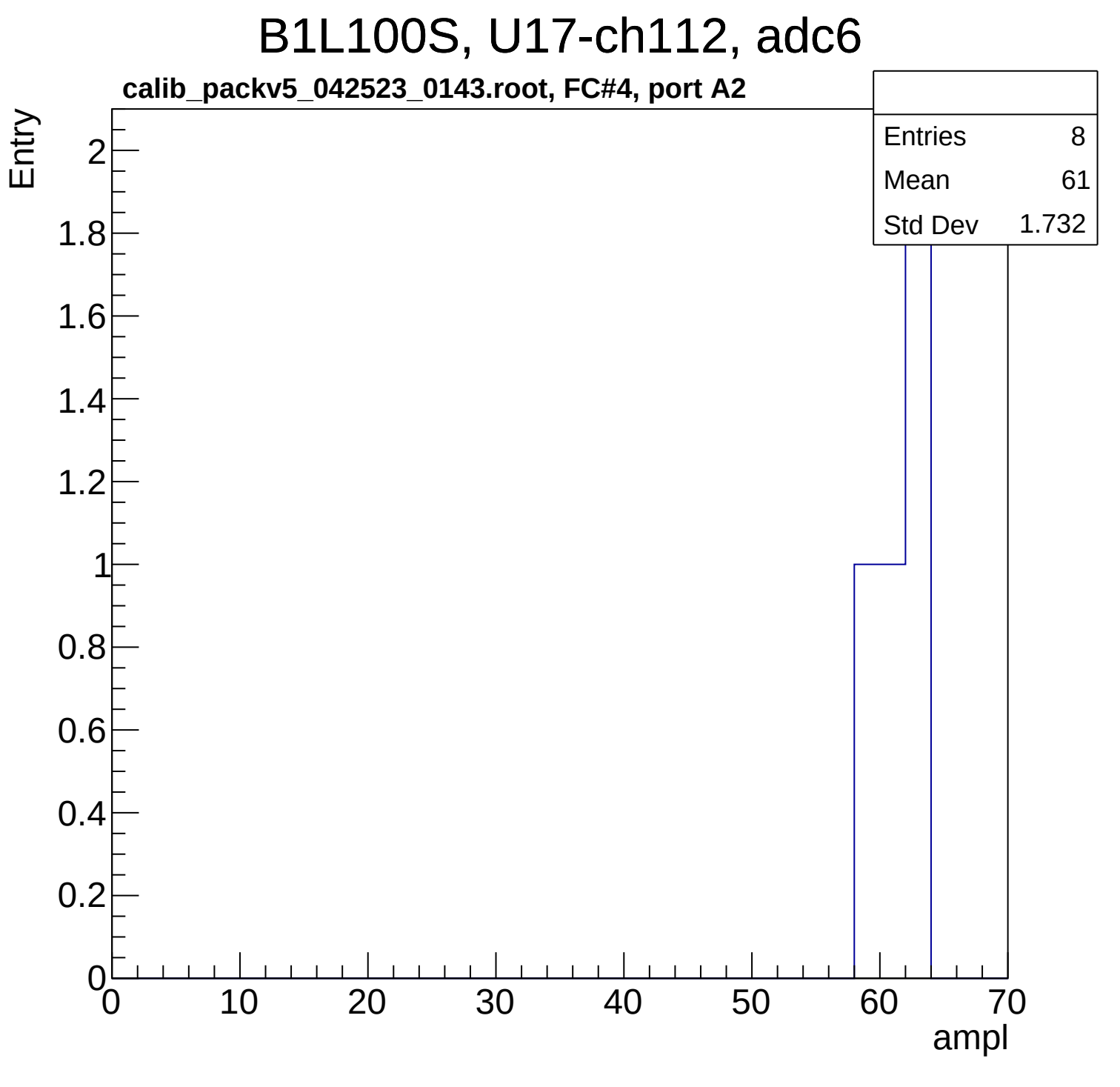
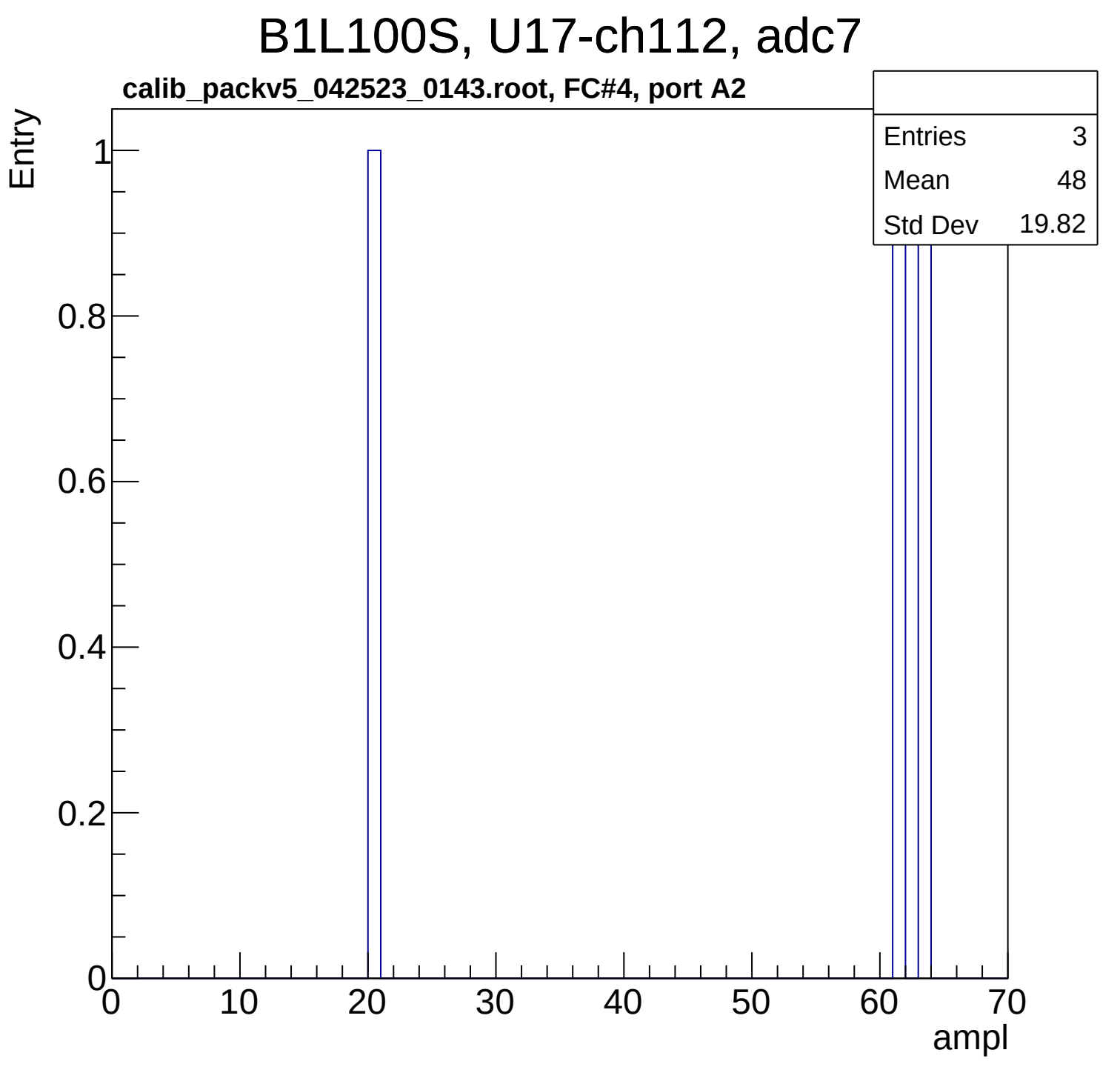
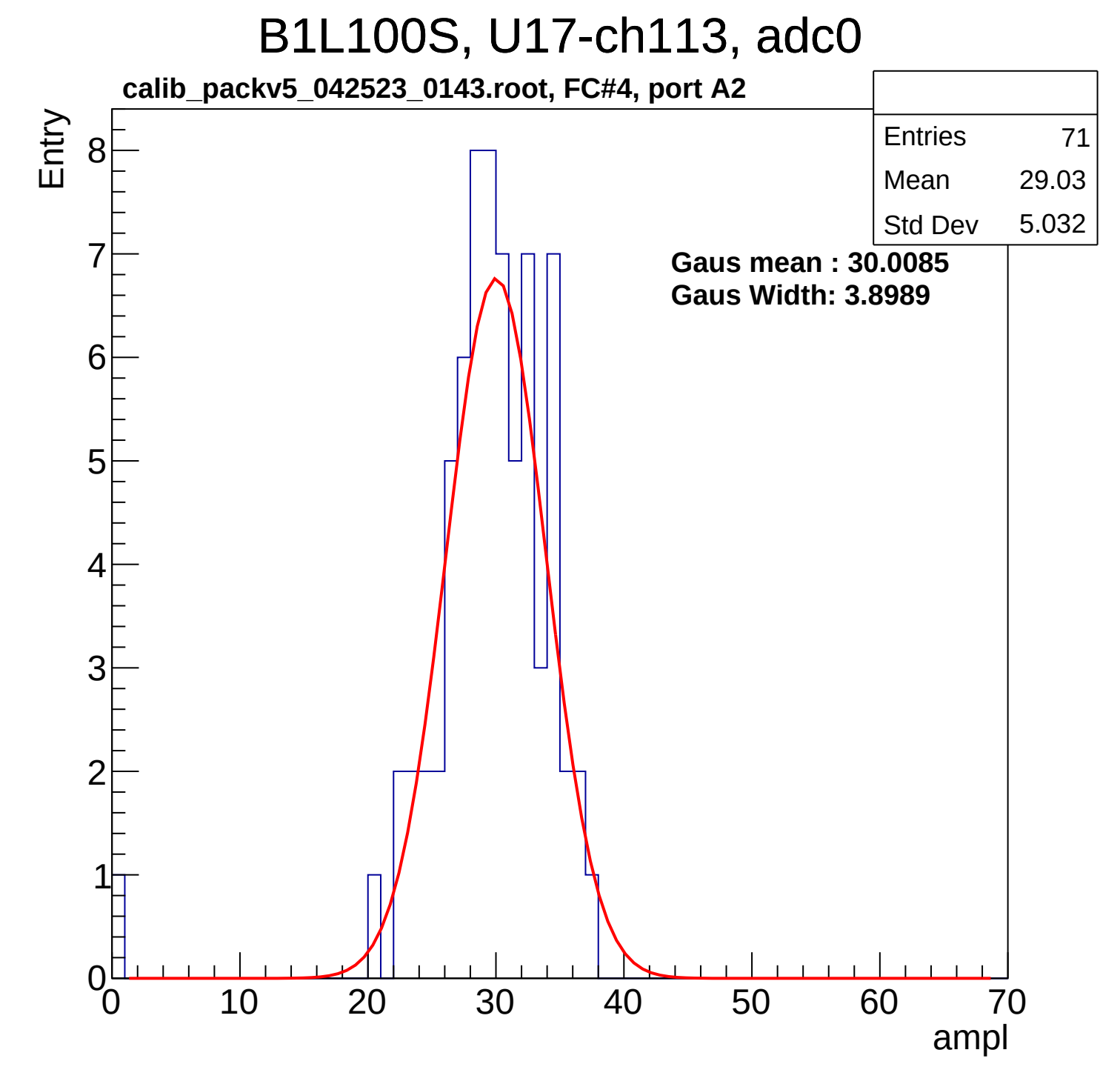
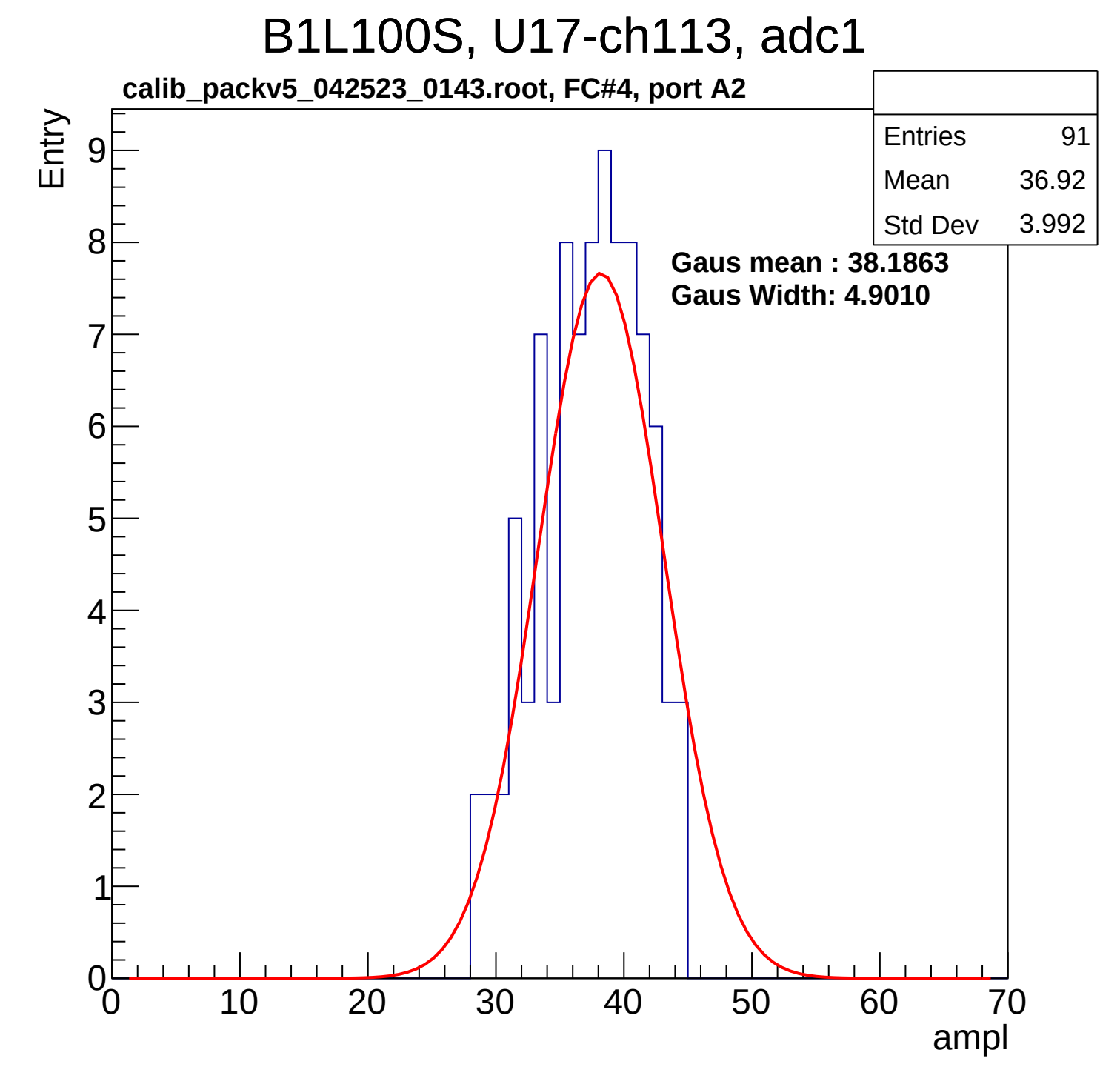
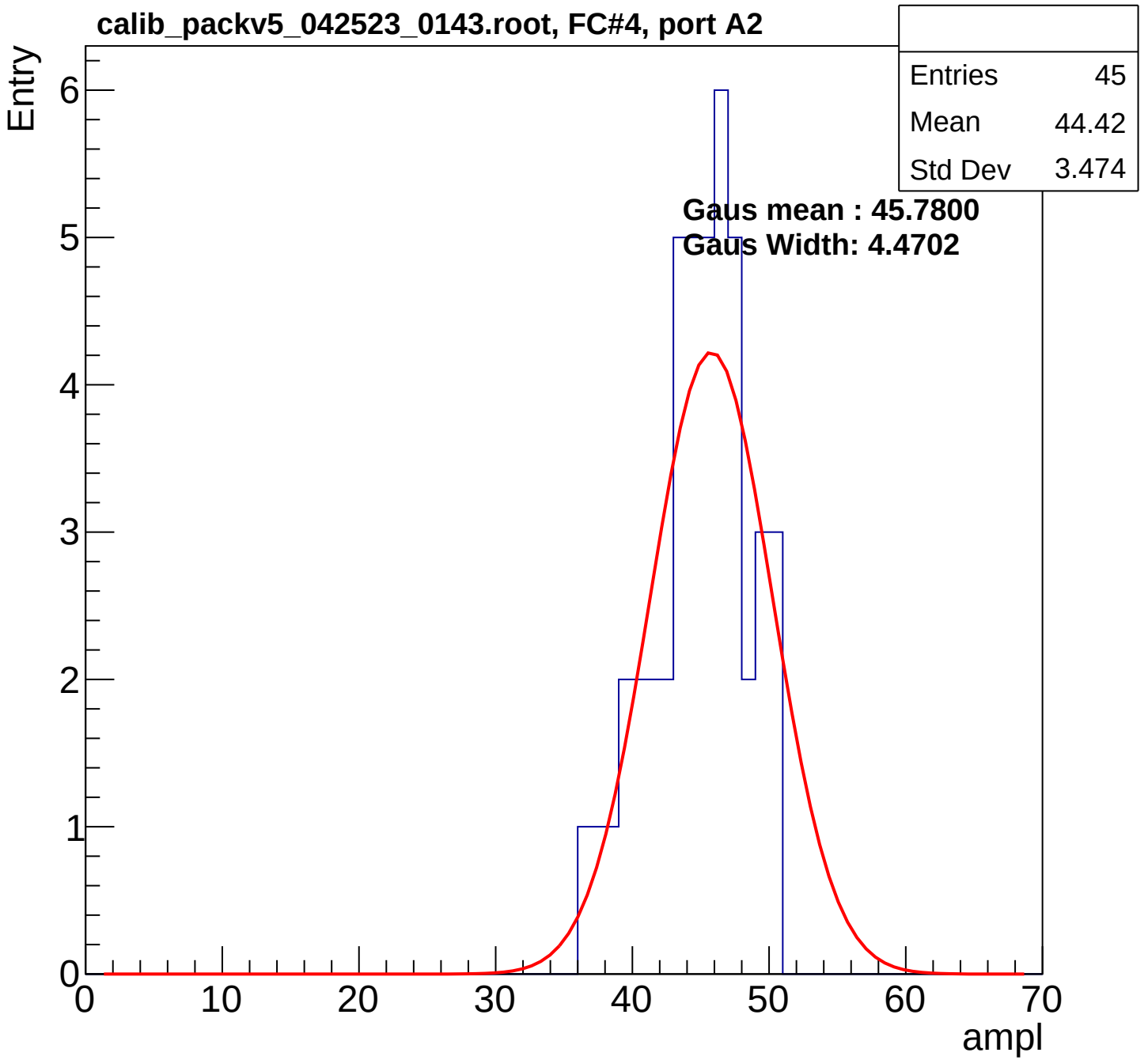
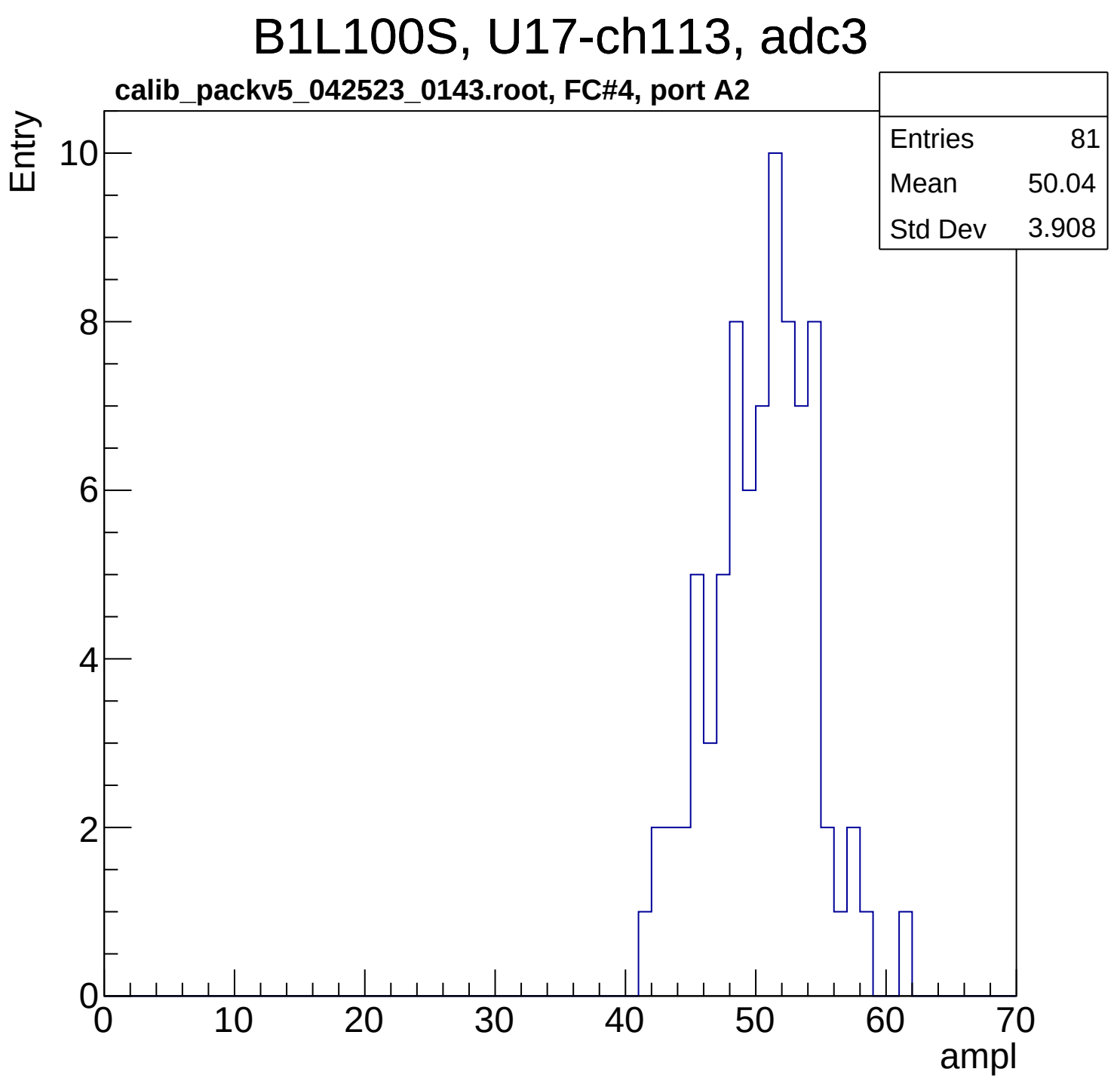

B1L100S, U17-ch112, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 8
Mean 61
Std Dev 1.732
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

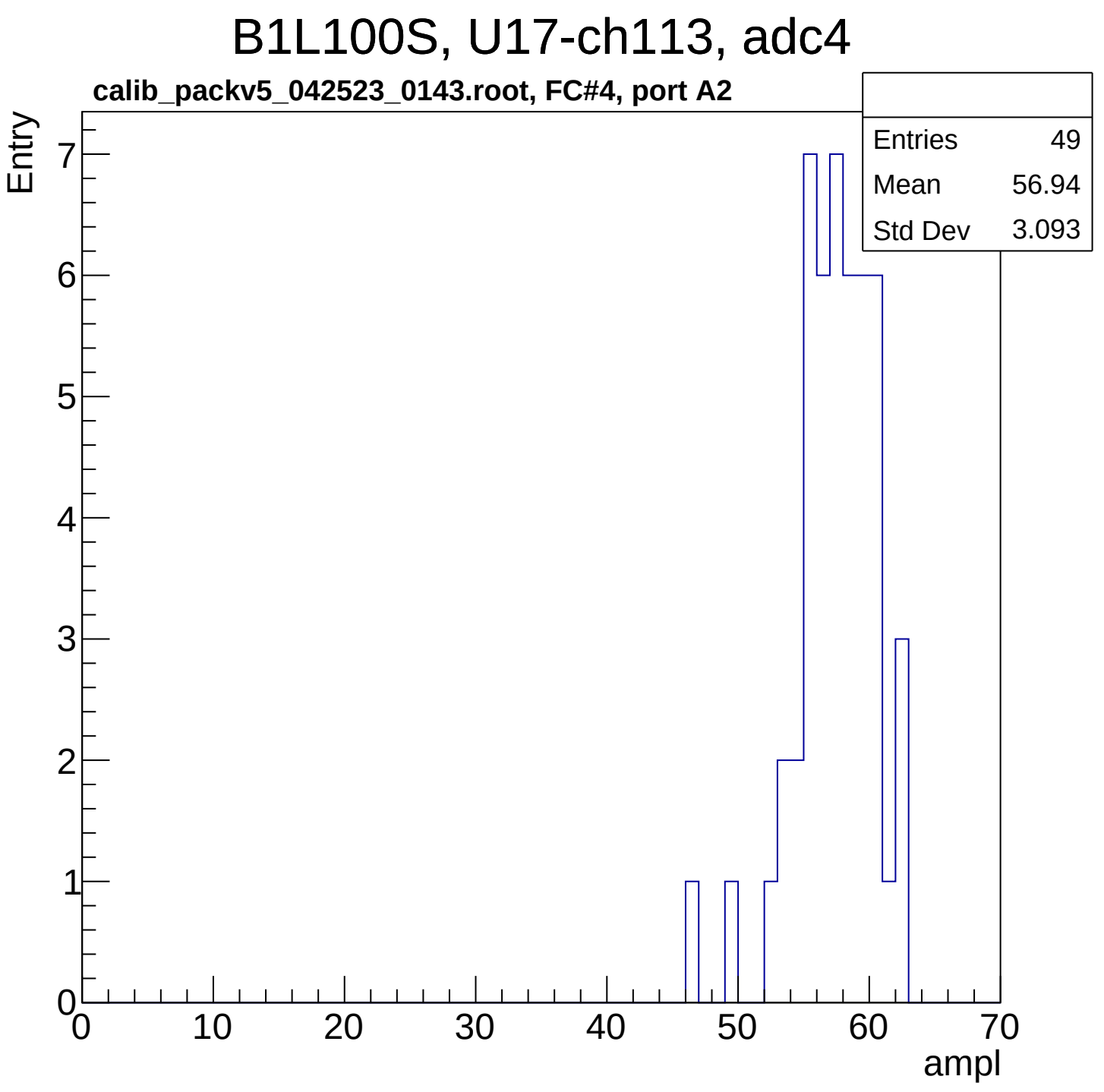

B1L100S, U17-ch112, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 48
Std Dev 19.82
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

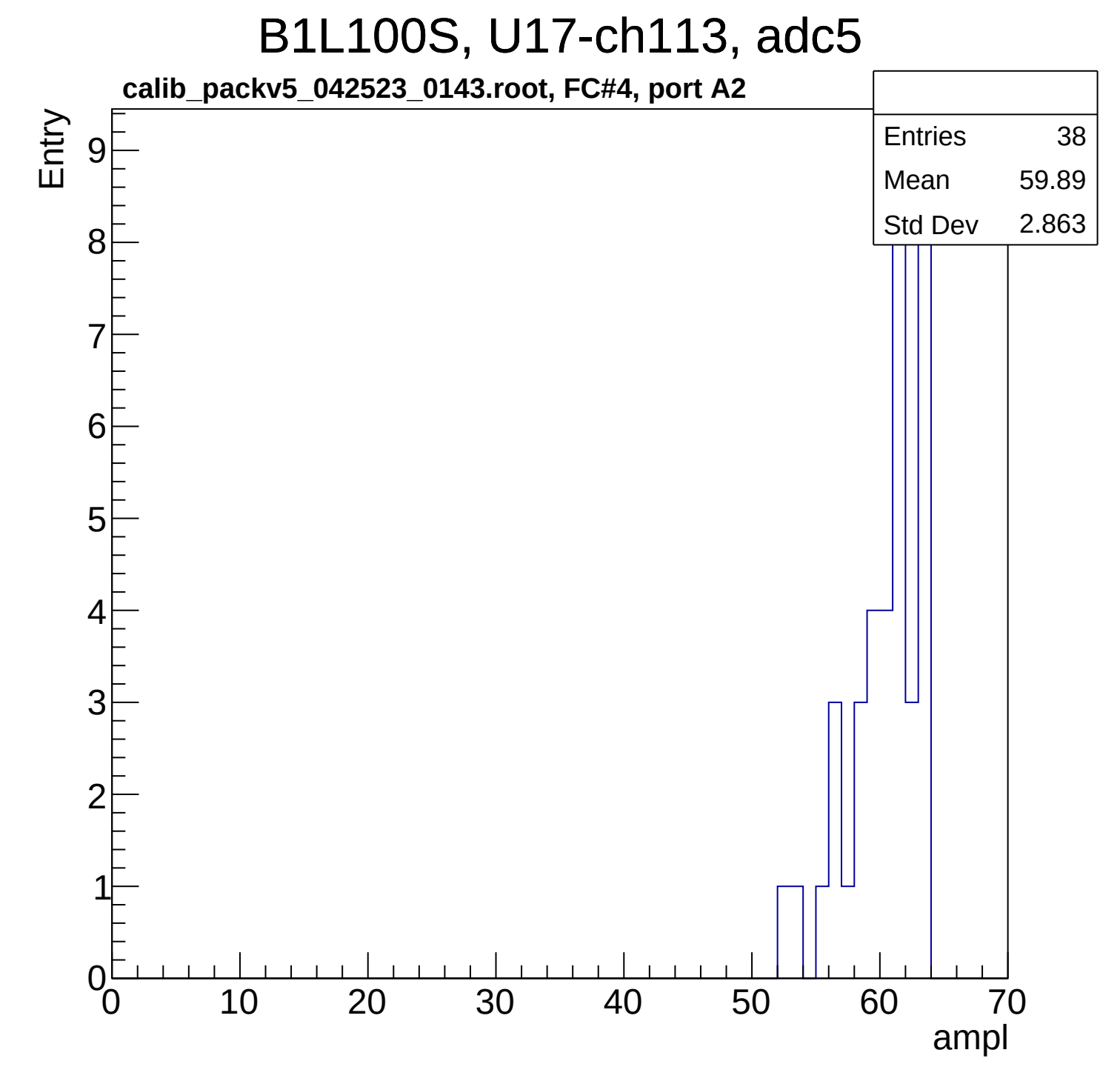

B1L100S, U17-ch113, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 29.03
Std Dev 5.032
Gaus mean : 30.0085
Gaus Width: 3.8989
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

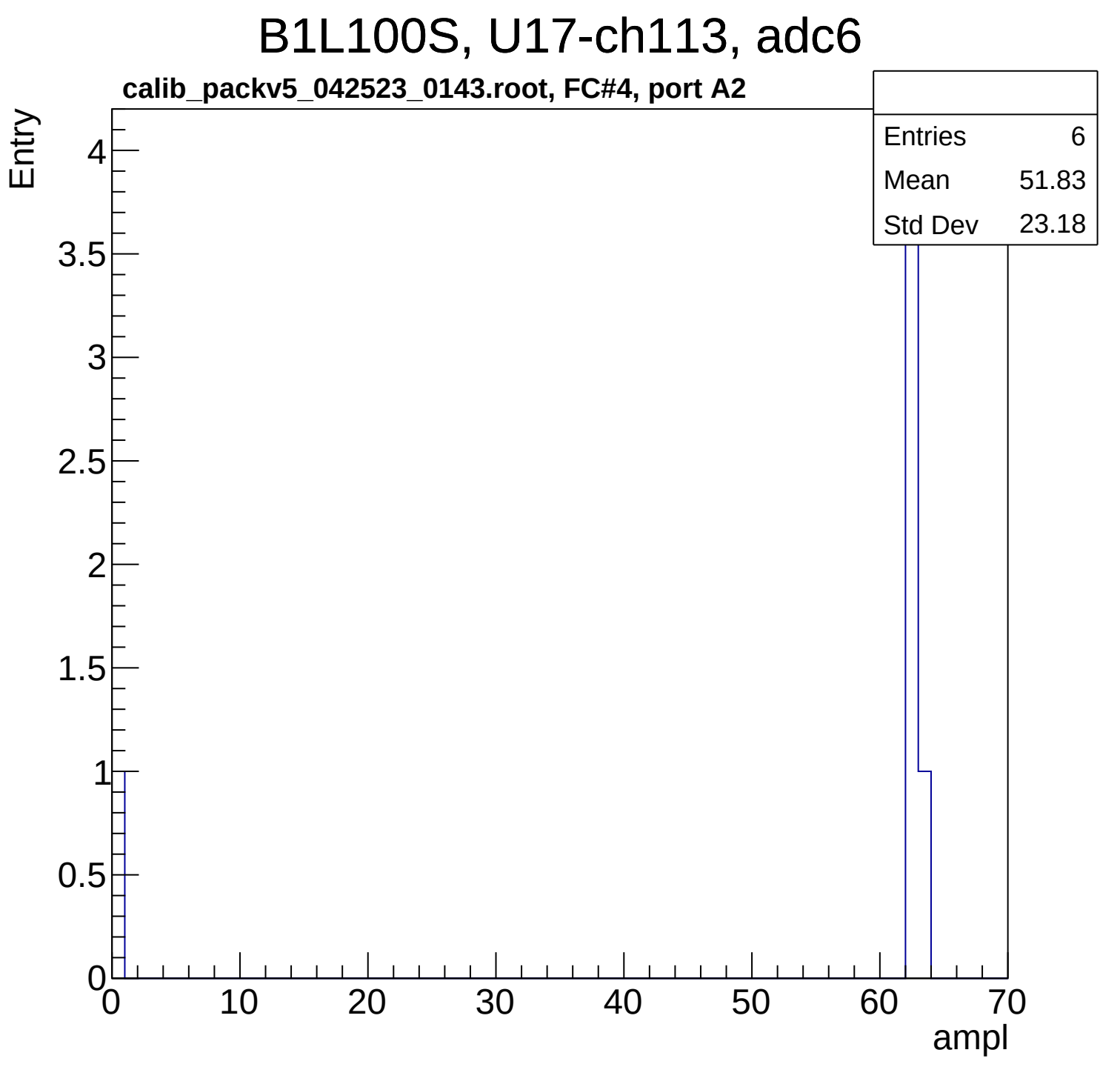

B1L100S, U17-ch113, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 91
Mean 36.92
Std Dev 3.992
Gaus mean : 38.1863
Gaus Width: 4.9010
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

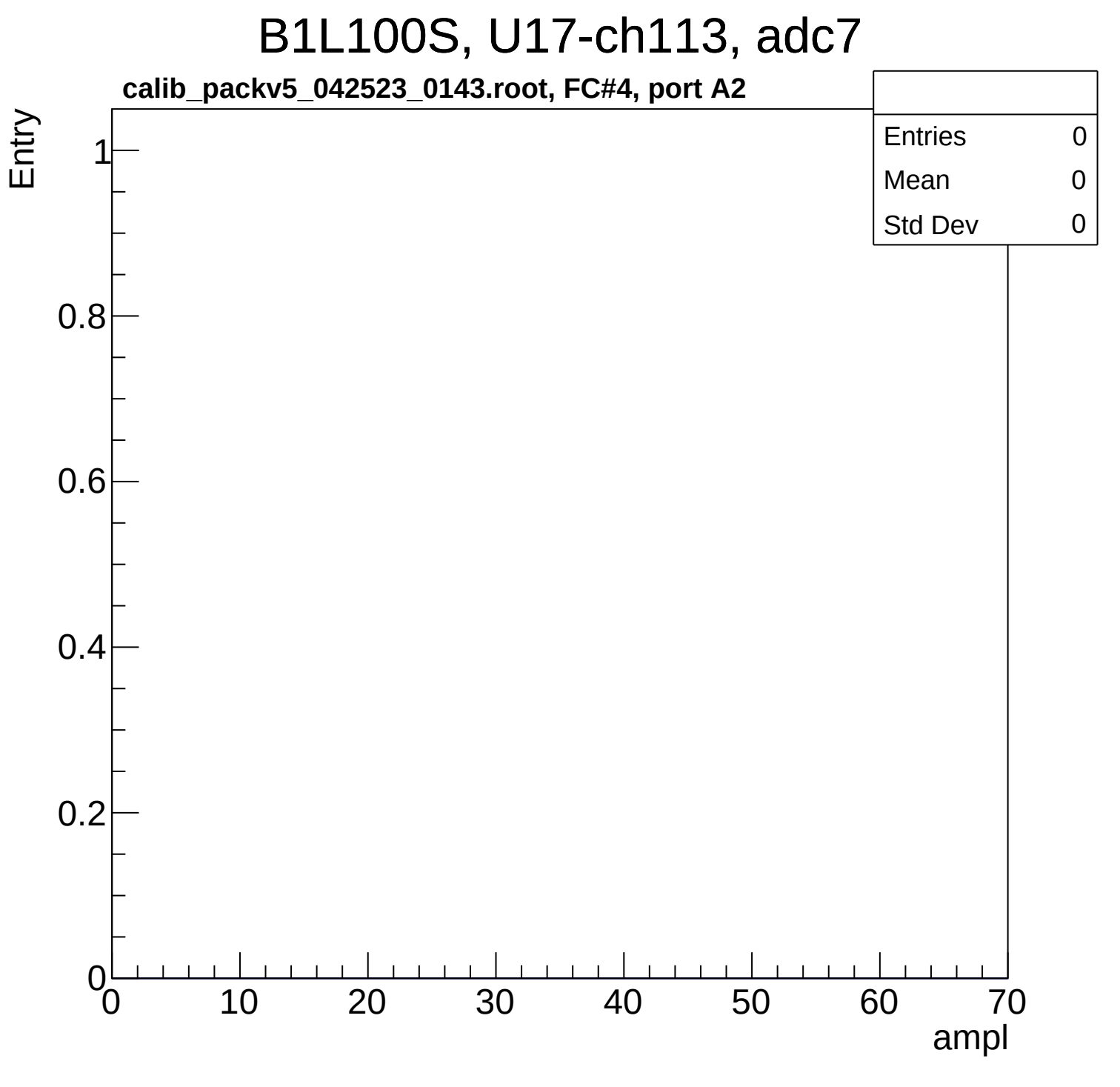

B1L100S, U17-ch113, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 45
Mean 44.42
Std Dev 3.474
Gaus mean : 45.7800
Gaus Width: 4.4702
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

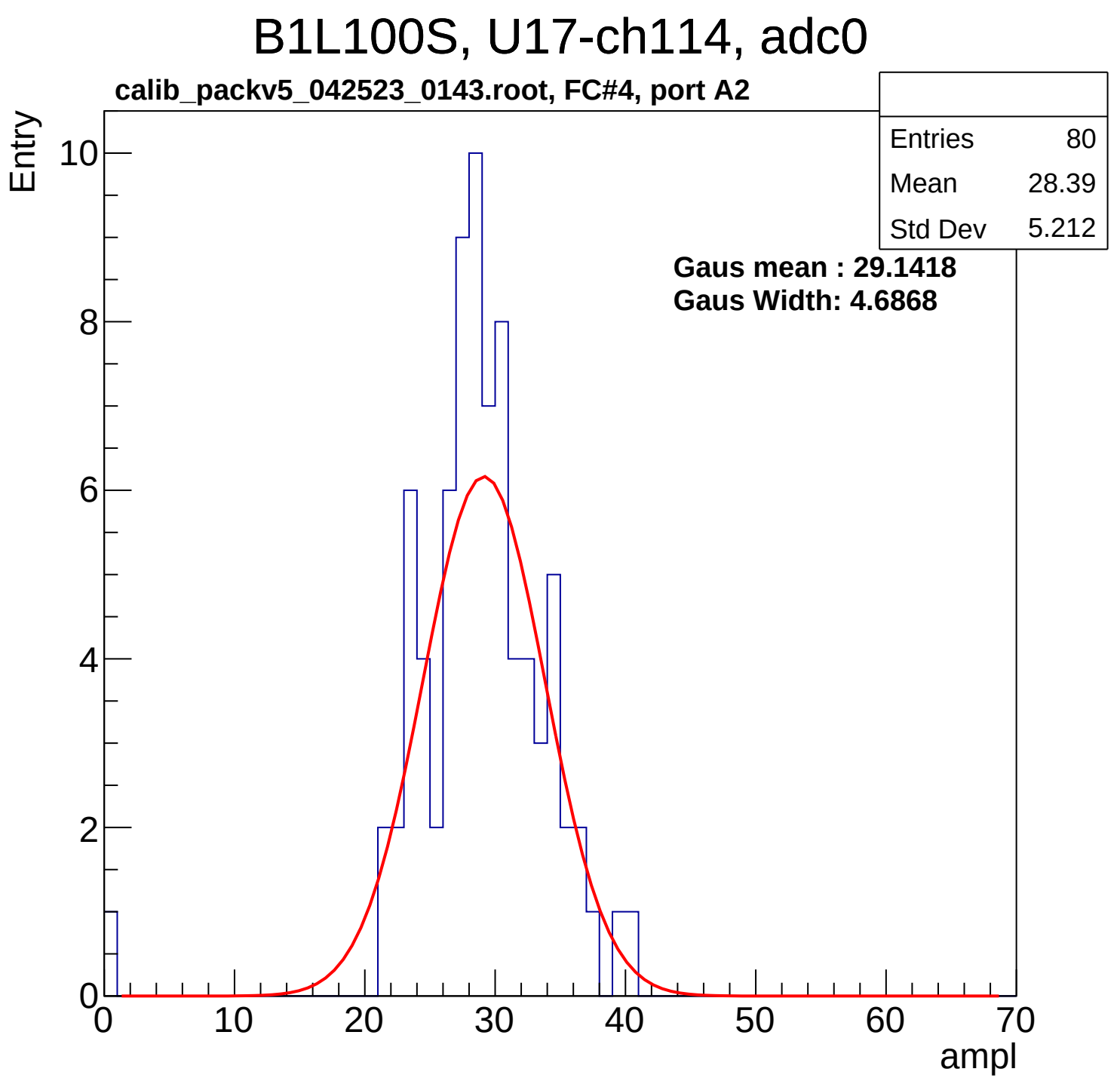

B1L100S, U17-ch113, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 81
Mean 50.04
Std Dev 3.908
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

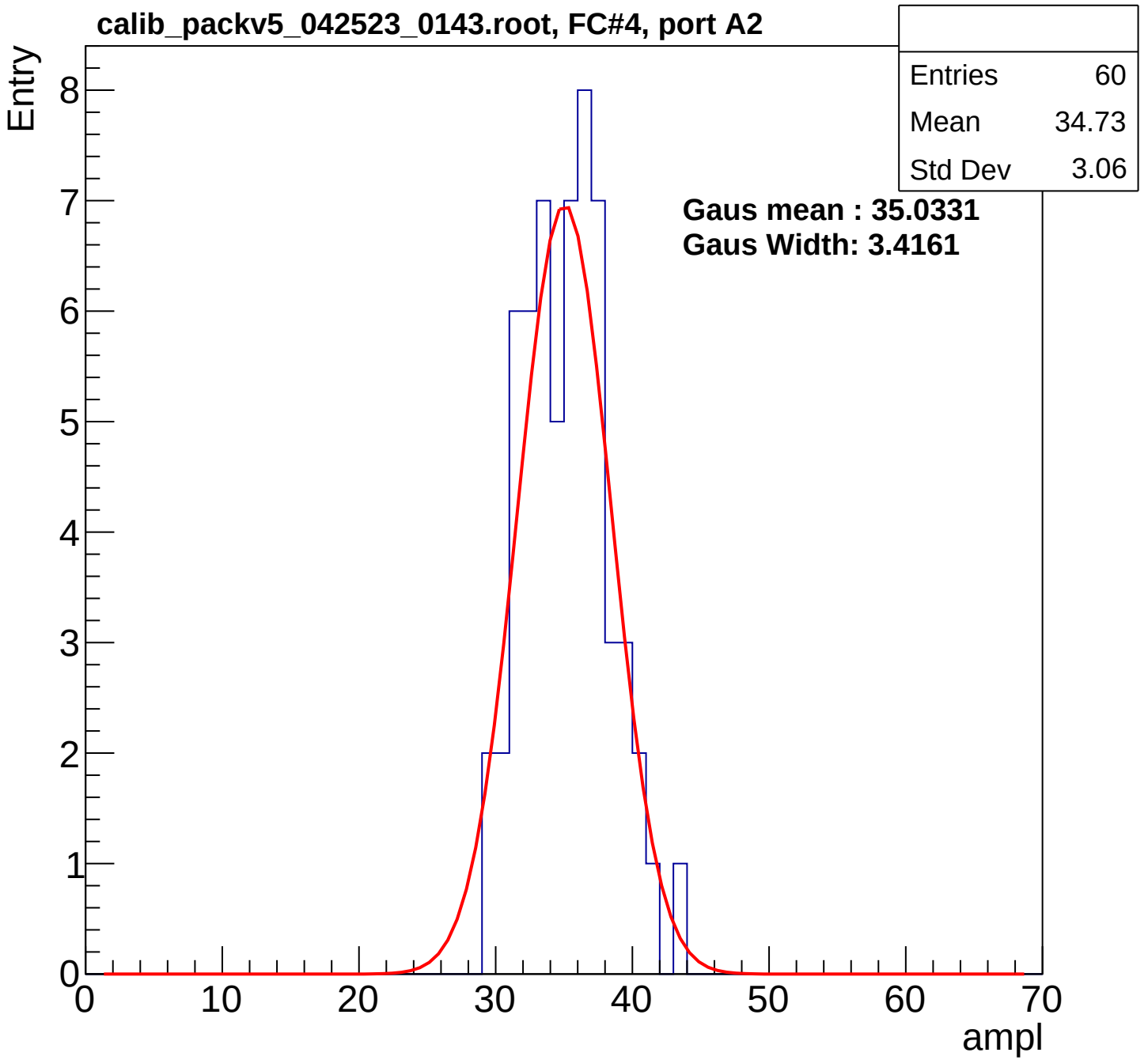

B1L100S, U17-ch113, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 49
Mean 56.94
Std Dev 3.093
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

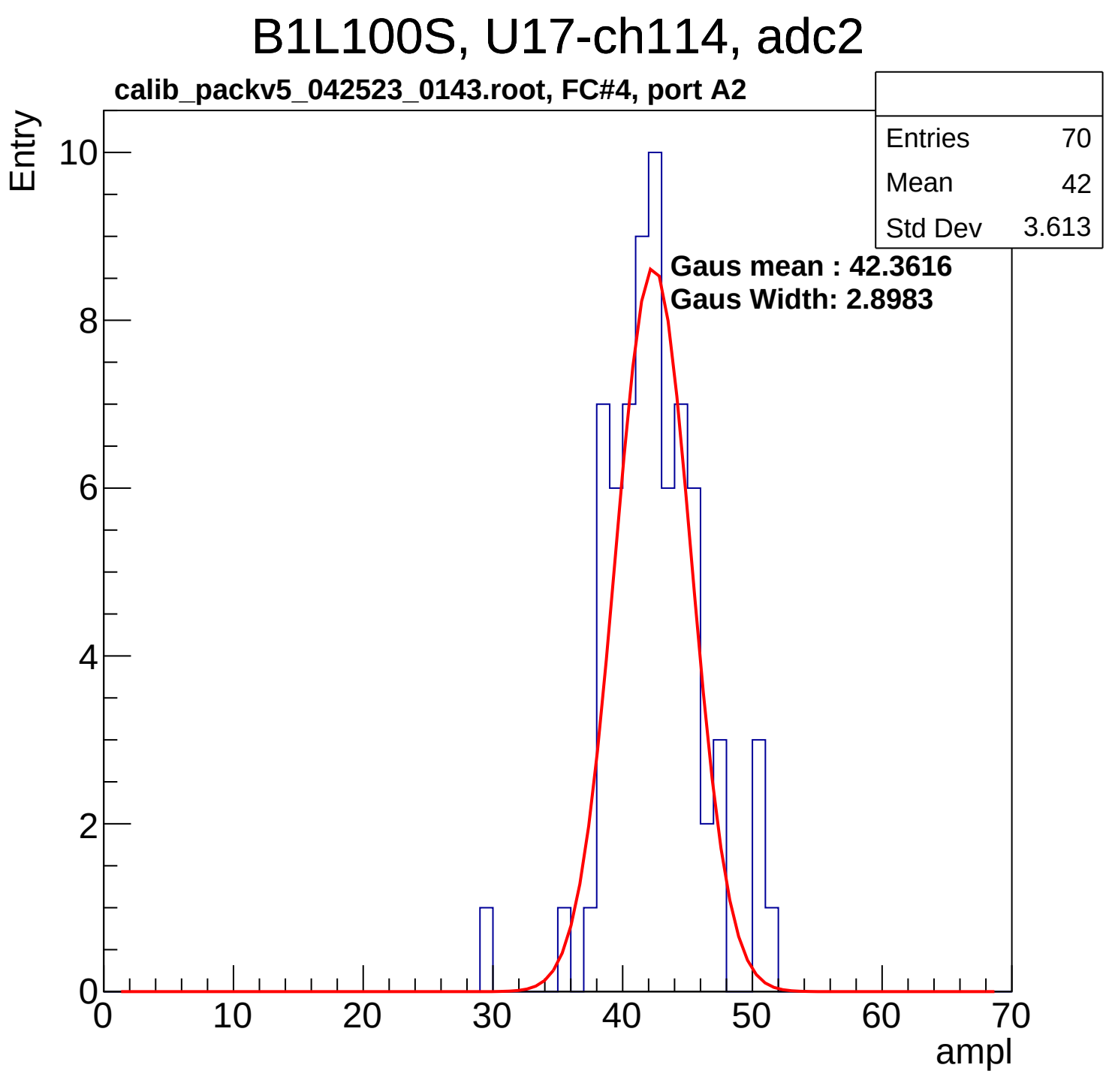

B1L100S, U17-ch113, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 38
Mean 59.89
Std Dev 2.863
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch113, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 6
Mean 51.83
Std Dev 23.18
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L100S, U17-ch113, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch114, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 80
Mean 28.39
Std Dev 5.212
Gaus mean : 29.1418
Gaus Width: 4.6868
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U17-ch114, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 34.73
Std Dev 3.06
Gaus mean : 35.0331
Gaus Width: 3.4161
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch114, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 42
Std Dev 3.613
Gaus mean : 42.3616
Gaus Width: 2.8983
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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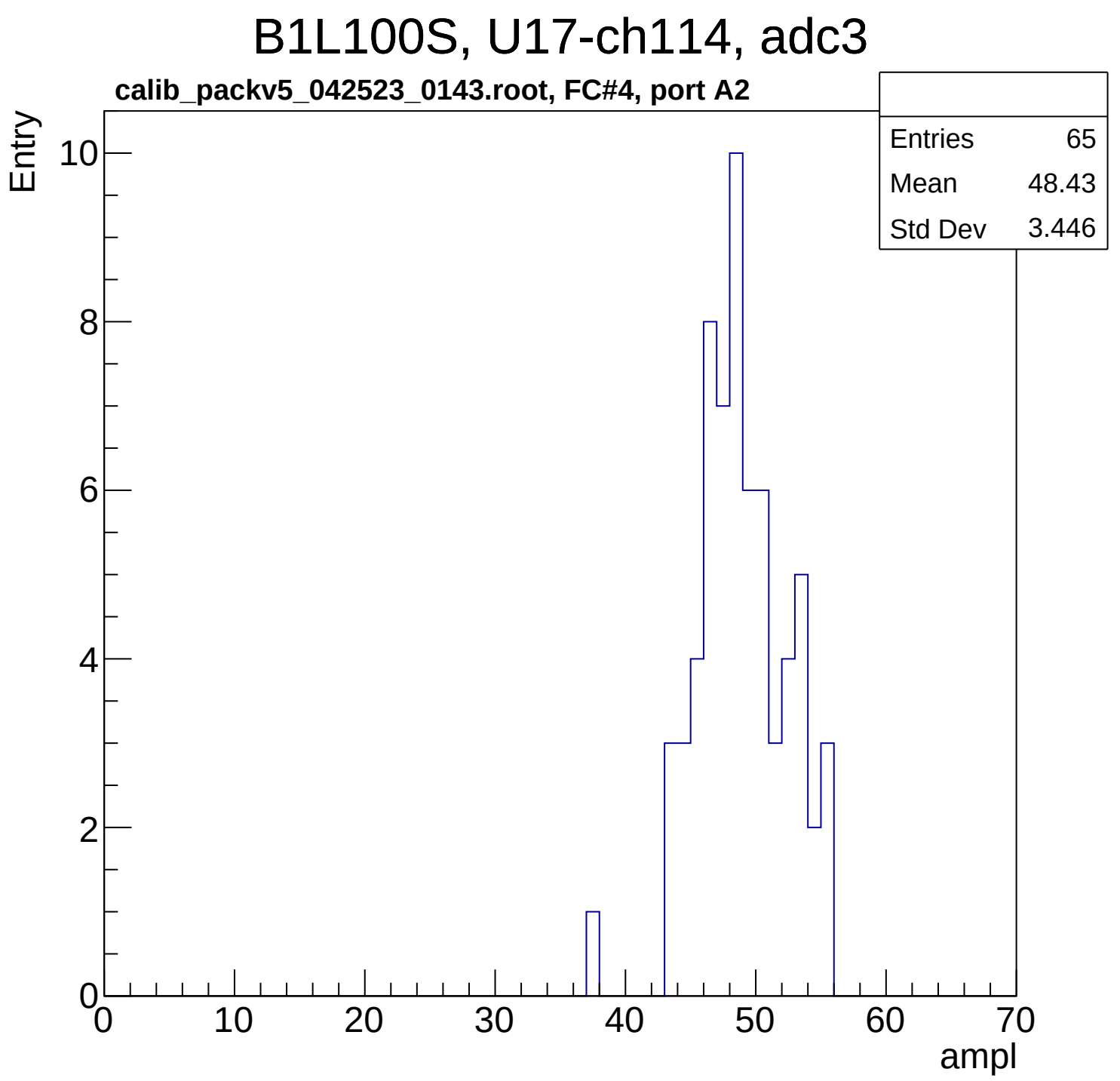
B1L100S, U17-ch114, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 48.43
Std Dev 3.446
Entry
ampl
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2
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6
8
10
0
10
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40
50
60
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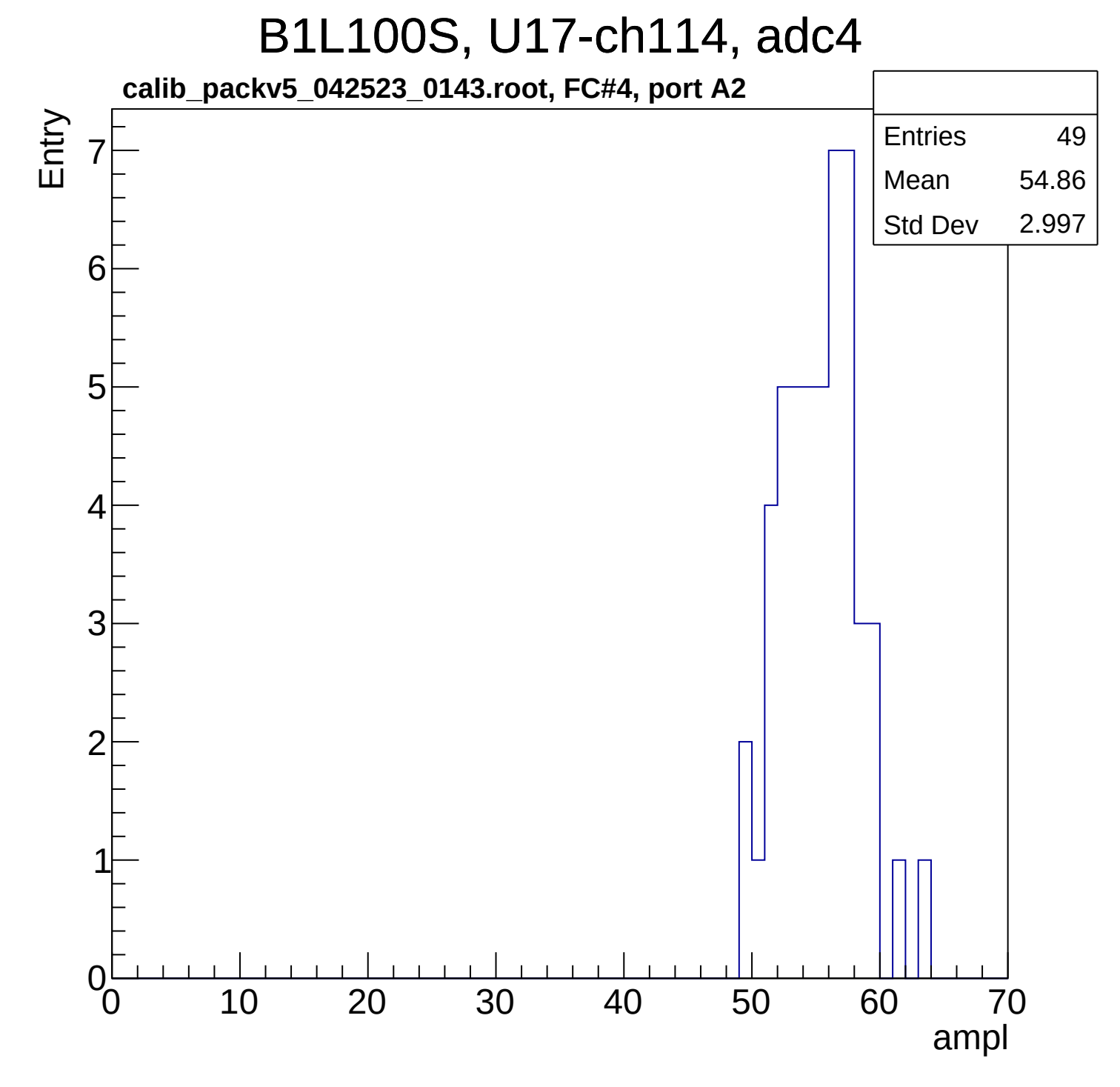
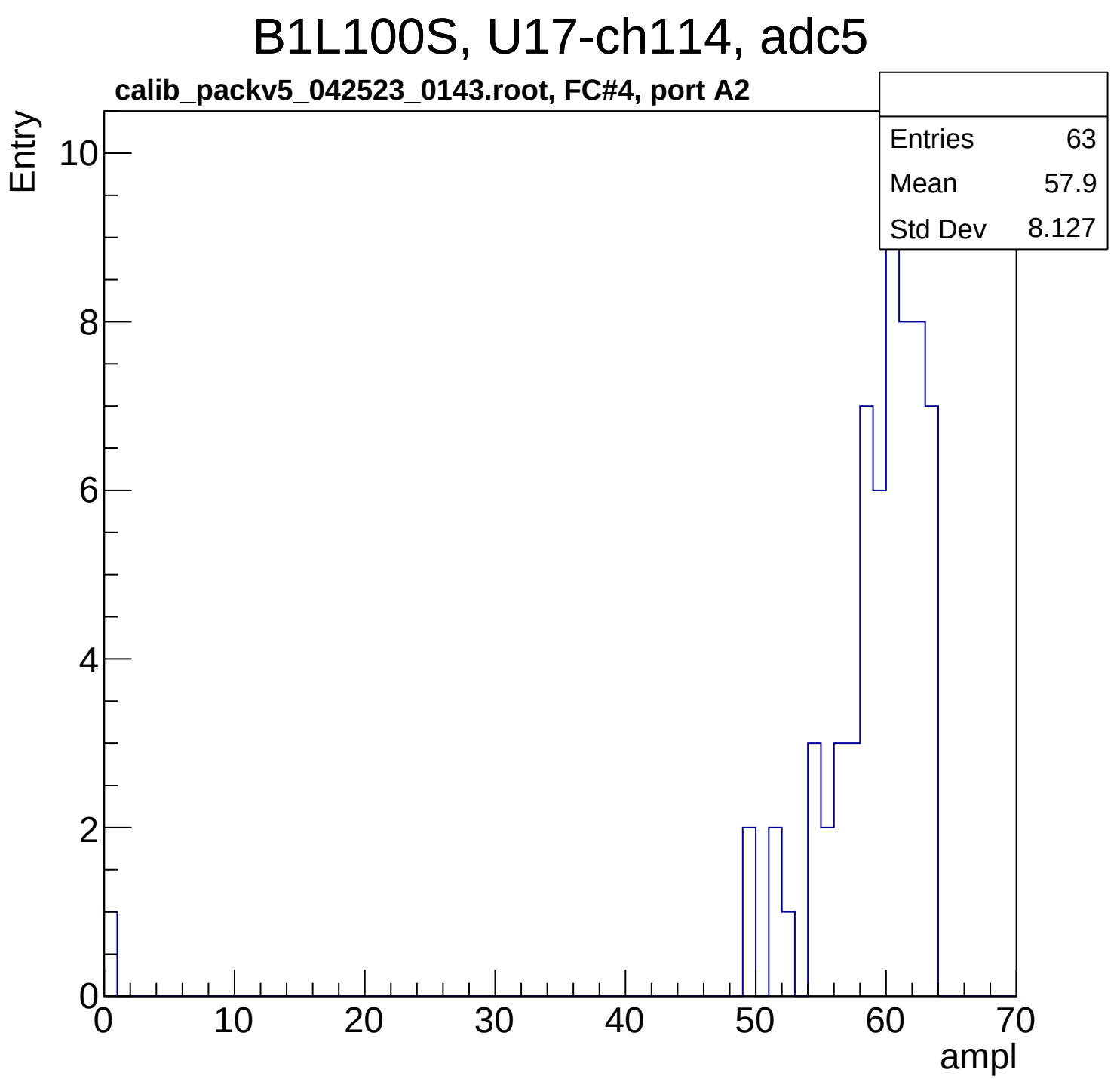

B1L100S, U17-ch114, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 49
Mean 54.86
Std Dev 2.997
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U17-ch114, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 57.9
Std Dev 8.127
Entry
ampl
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8
10
0
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20
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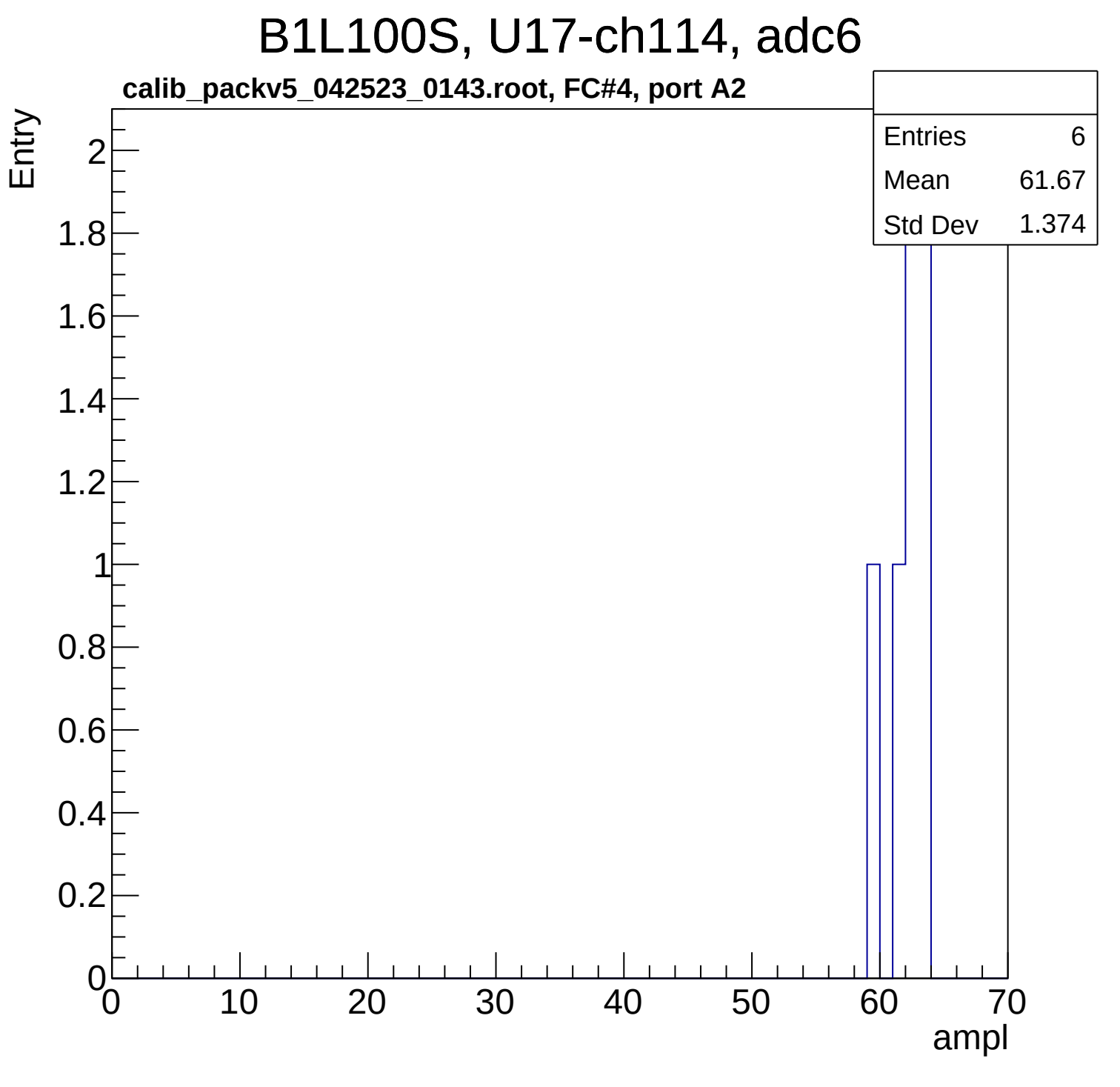
40
50
60
70


B1L100S, U17-ch114, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 6
Mean 61.67
Std Dev 1.374
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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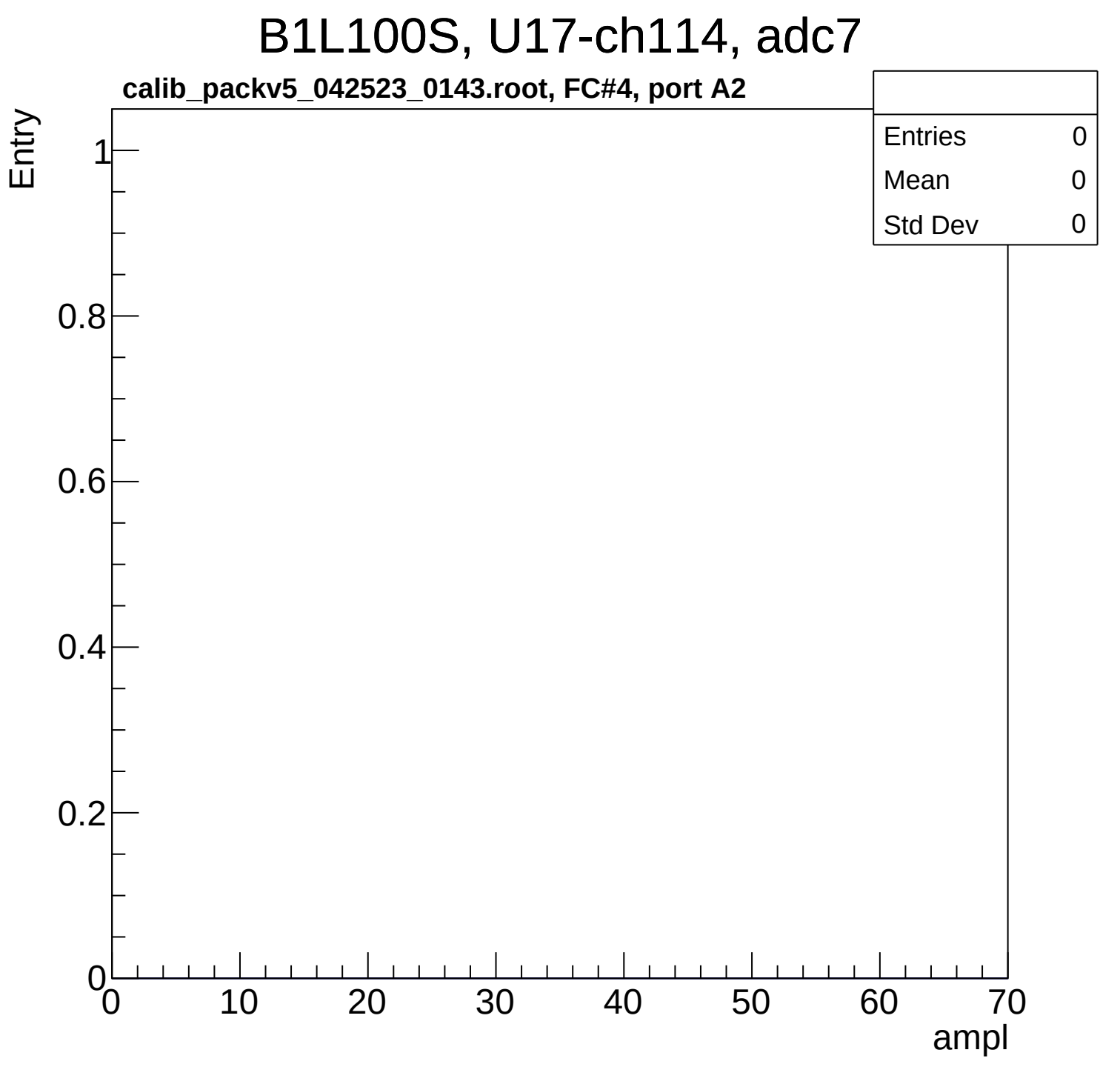
40
50
60
70


B1L100S, U17-ch114, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
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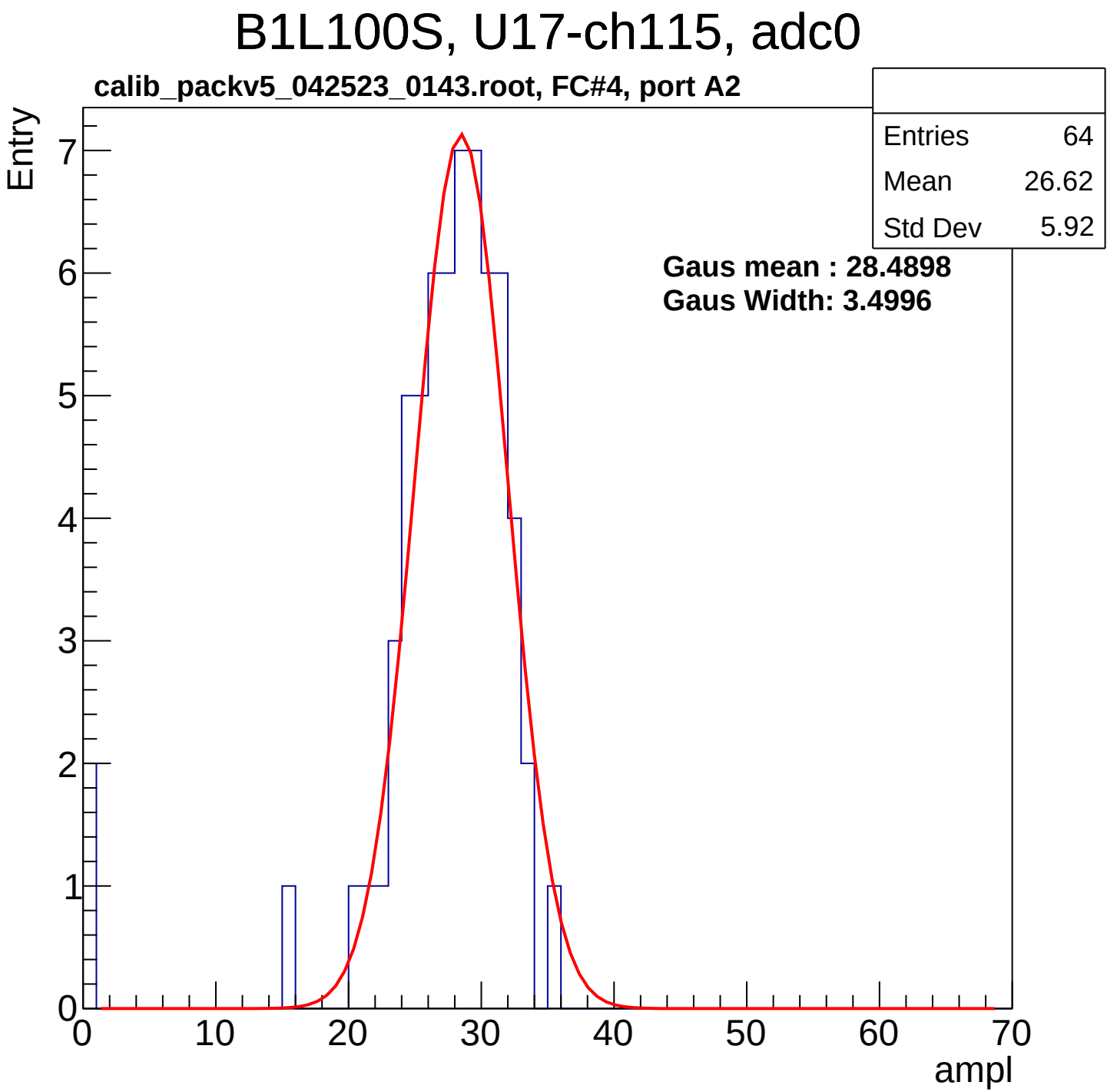
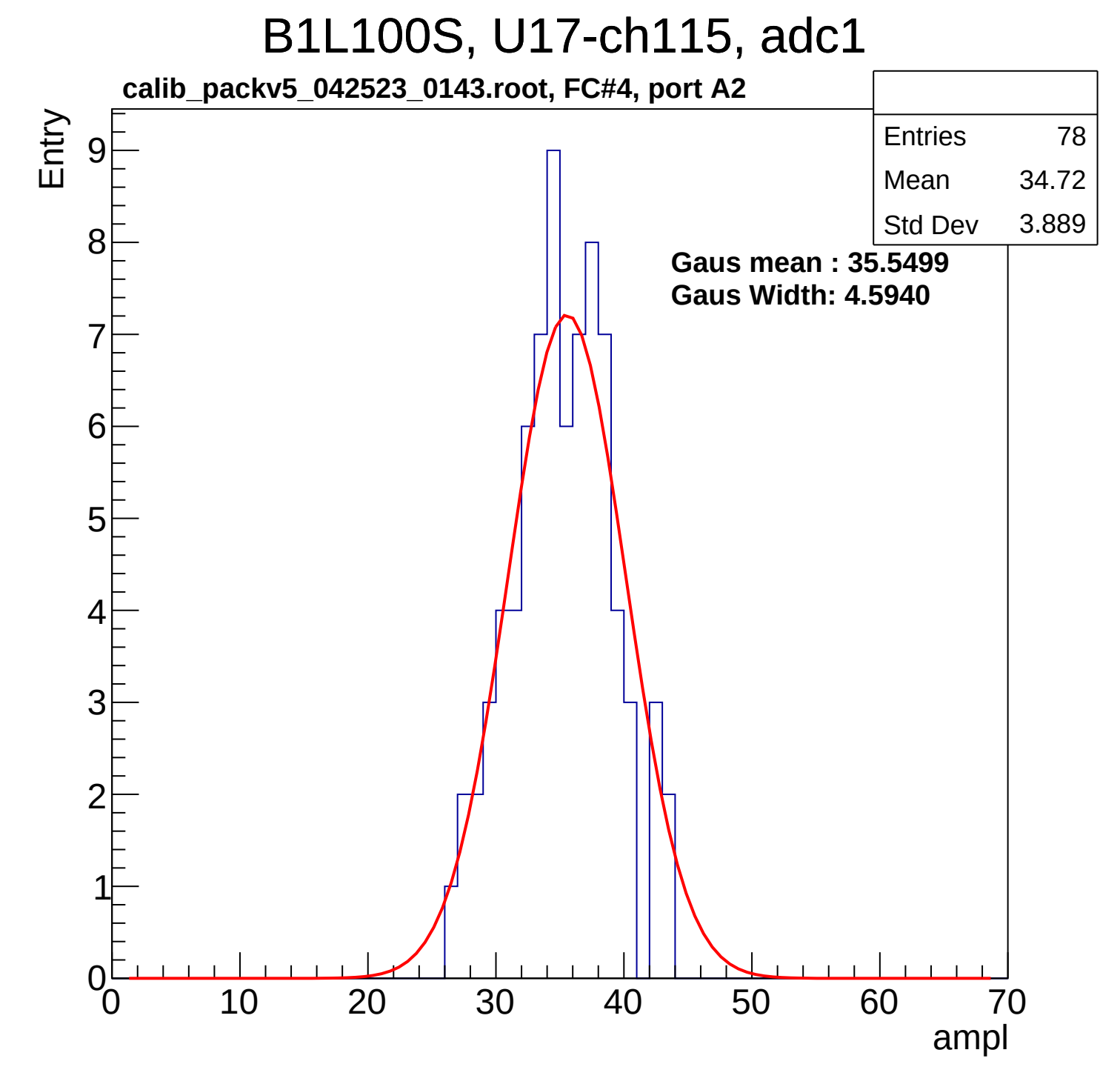
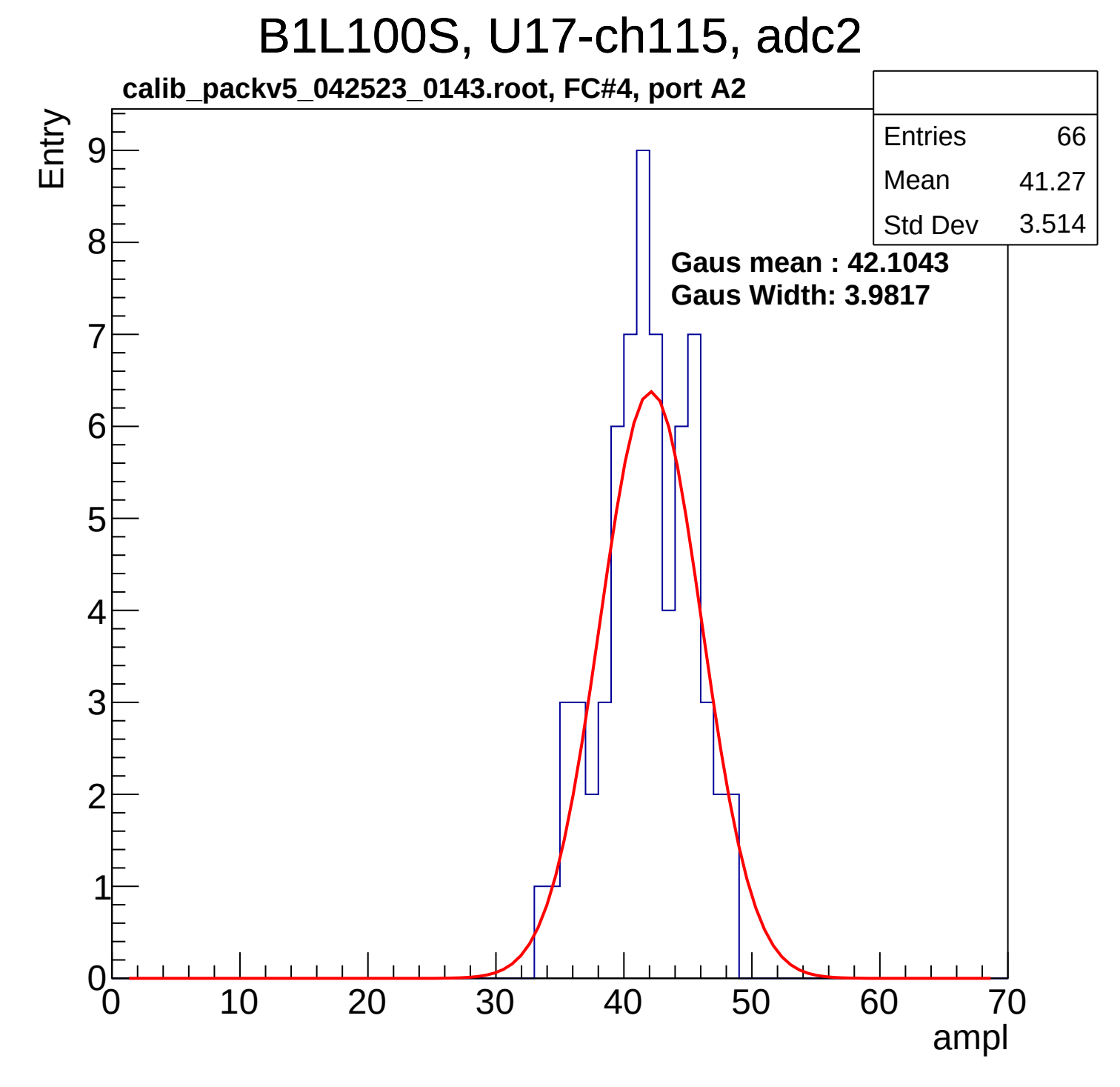
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch115, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 26.62
Std Dev 5.92
Gaus mean : 28.4898
Gaus Width: 3.4996
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U17-ch115, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 78
Mean 34.72
Std Dev 3.889
Gaus mean : 35.5499
Gaus Width: 4.5940
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch115, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 41.27
Std Dev 3.514
Gaus mean : 42.1043
Gaus Width: 3.9817
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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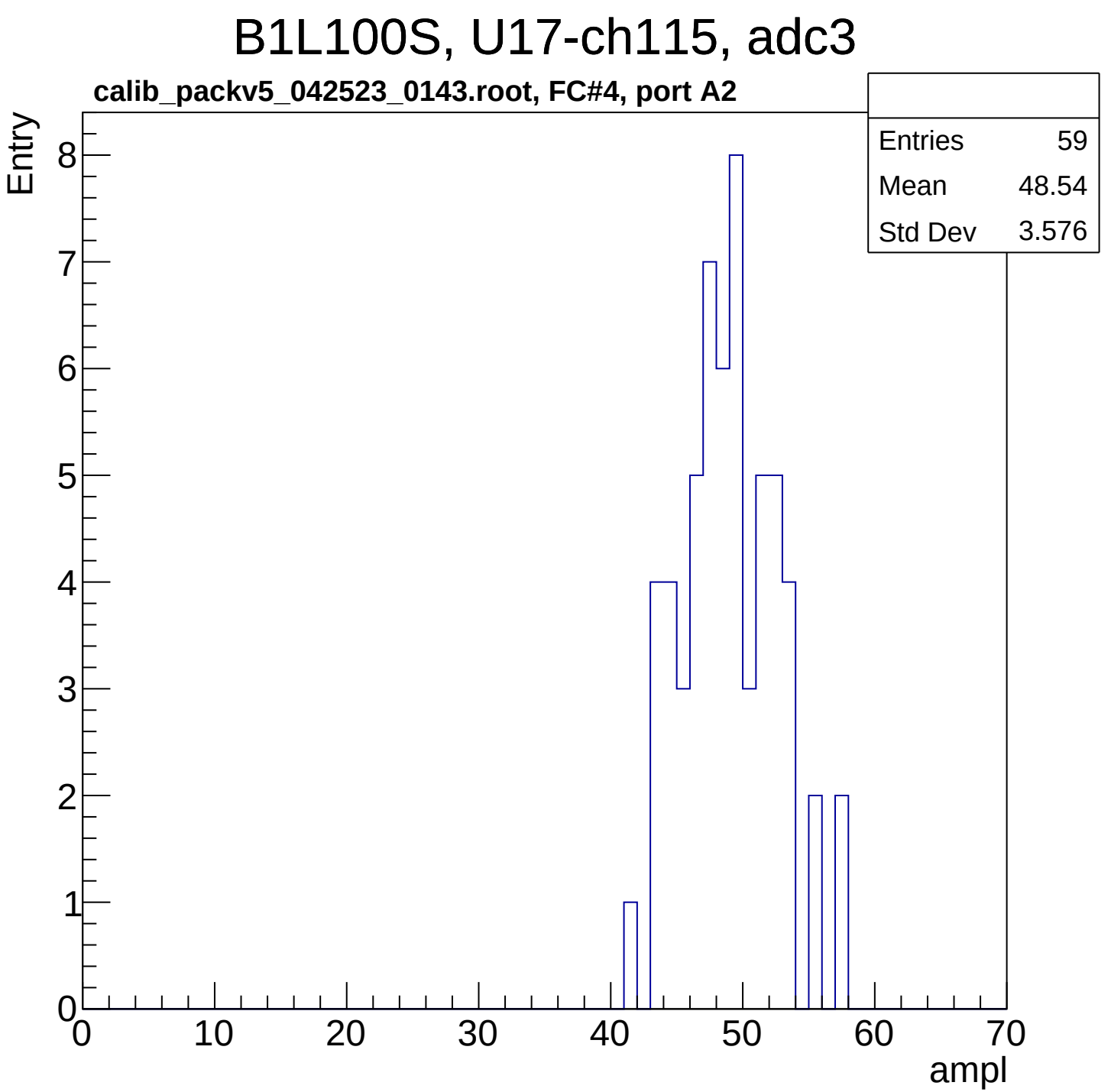
B1L100S, U17-ch115, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 48.54
Std Dev 3.576
Entry
ampl
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1
2
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4
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7
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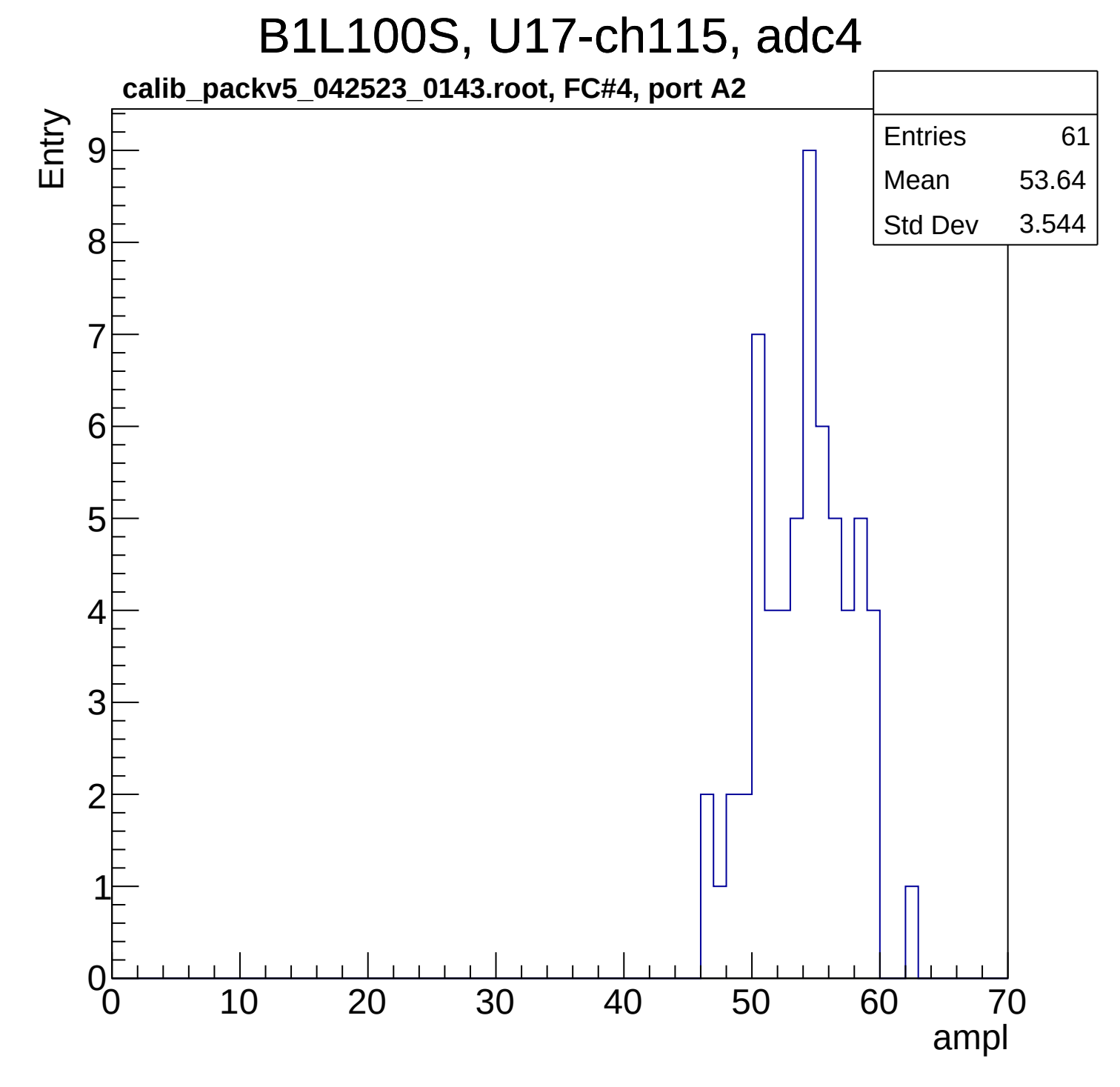
B1L100S, U17-ch115, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 53.64
Std Dev 3.544
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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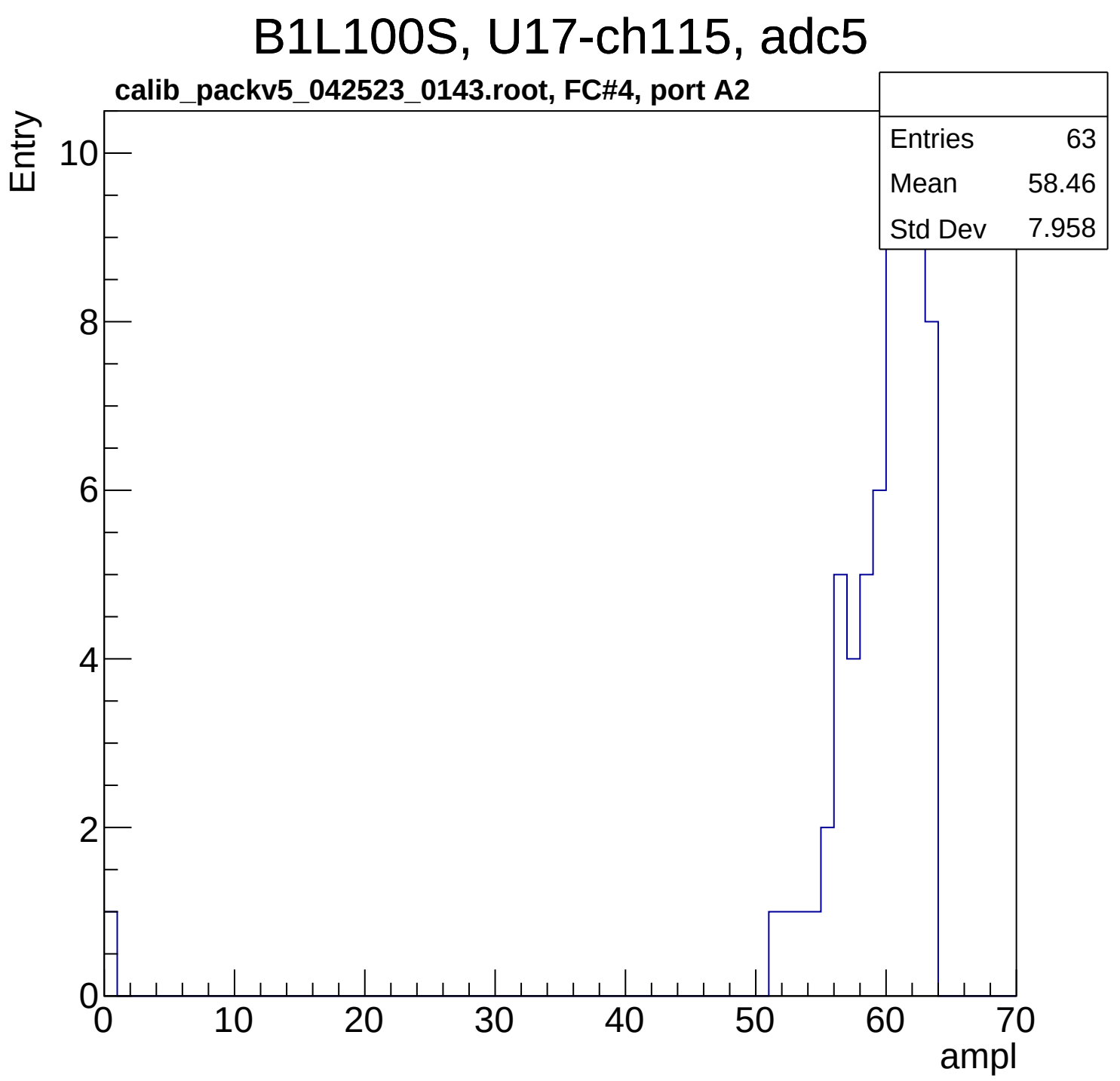
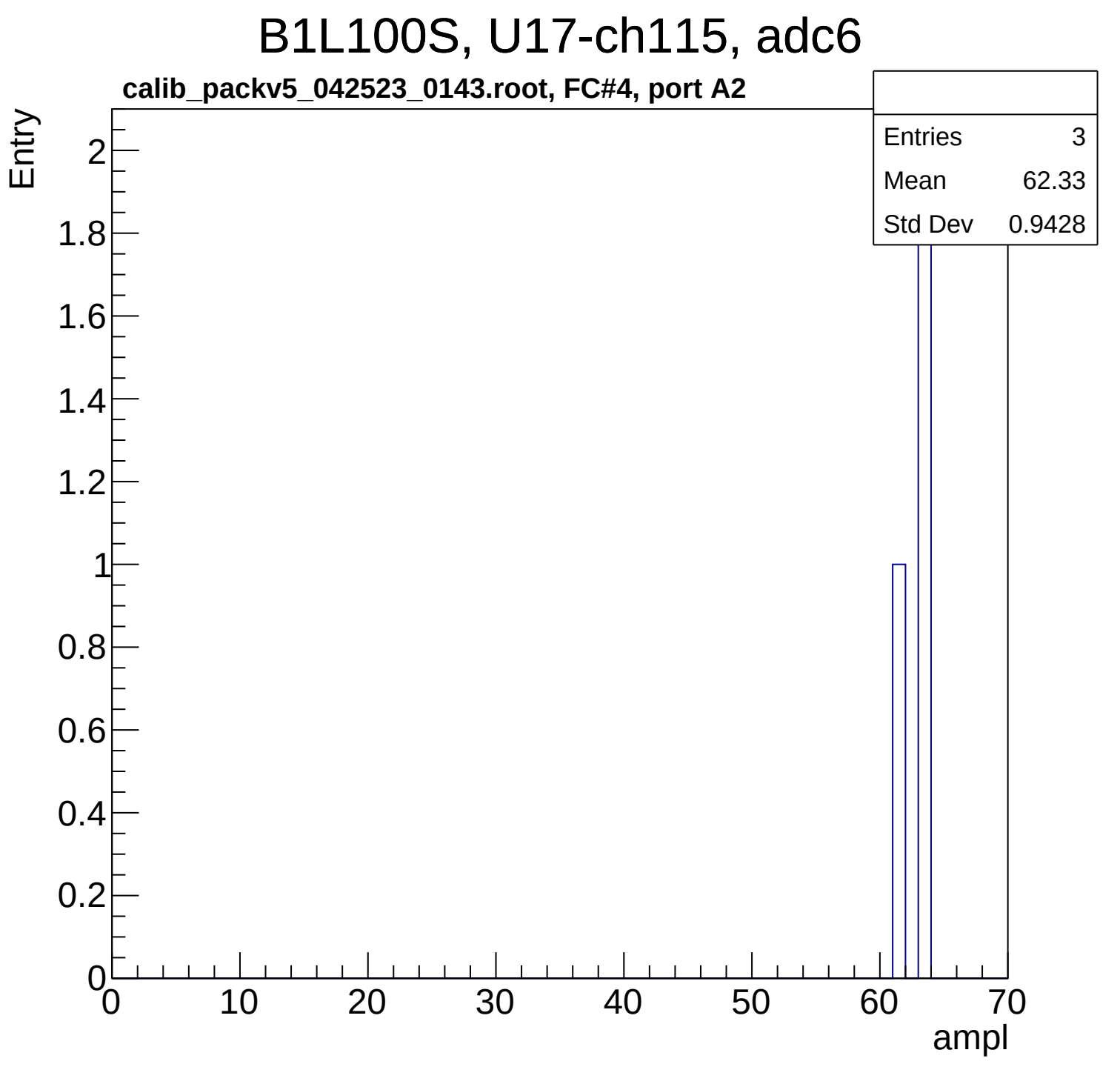
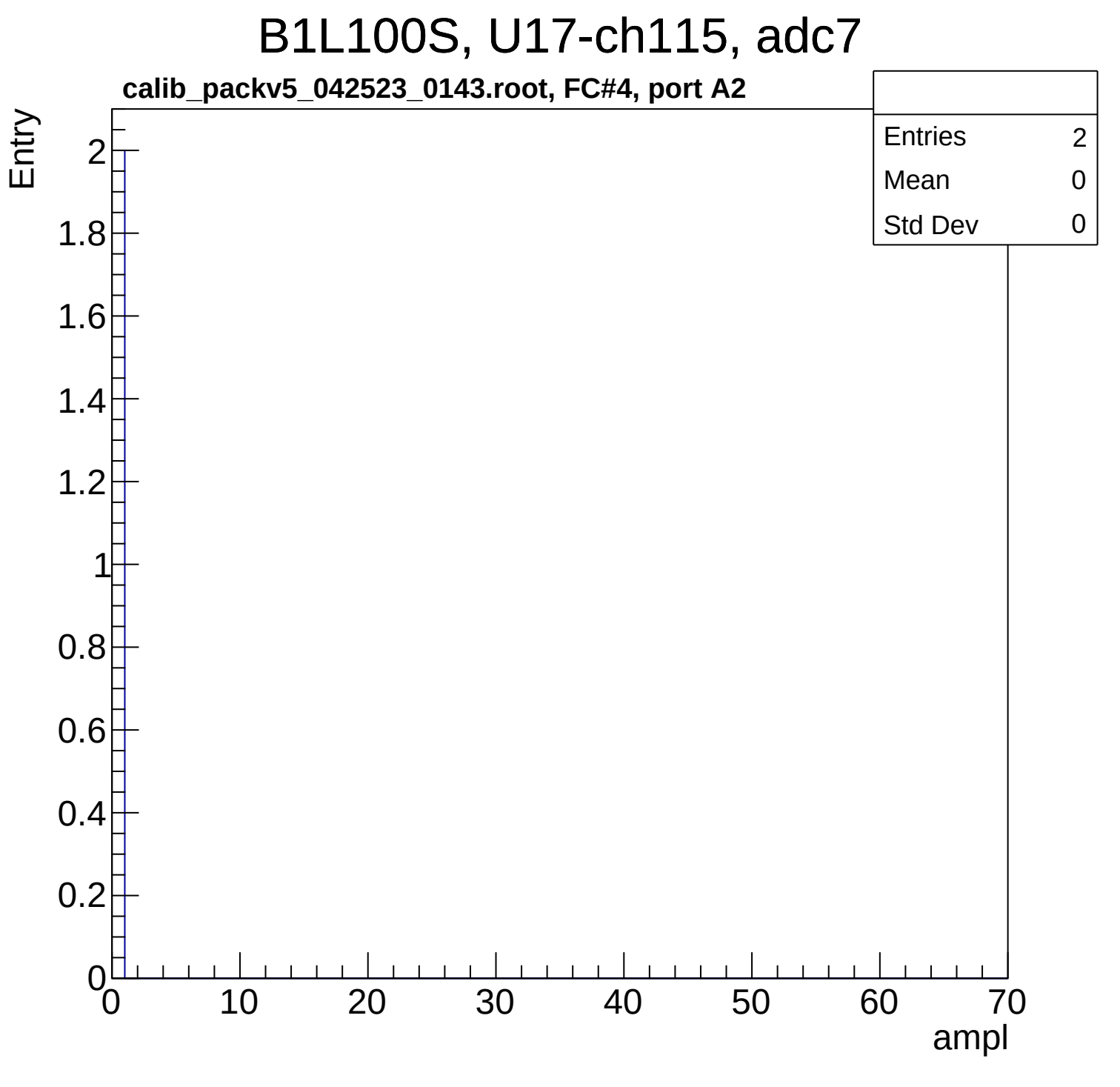
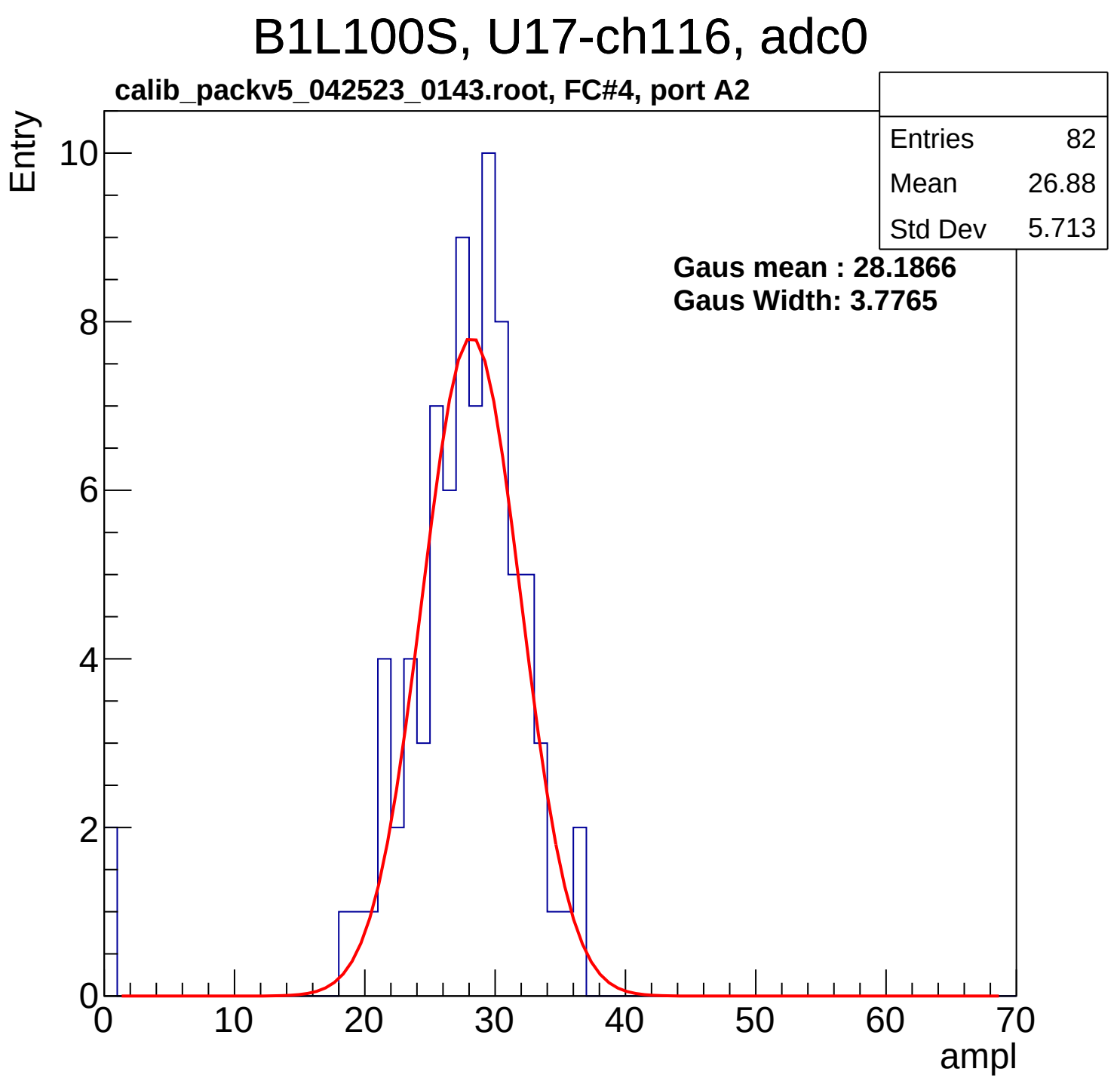
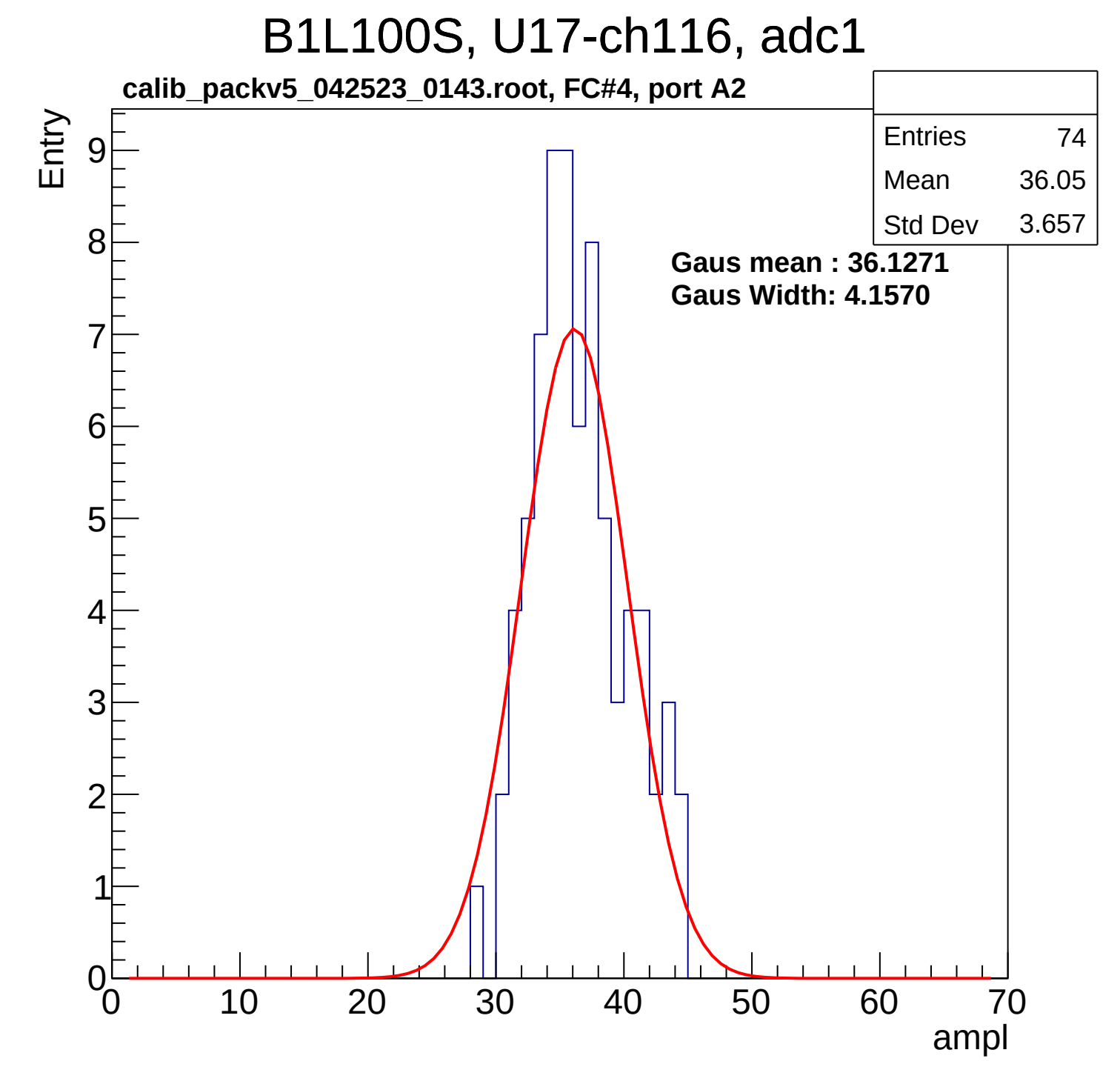
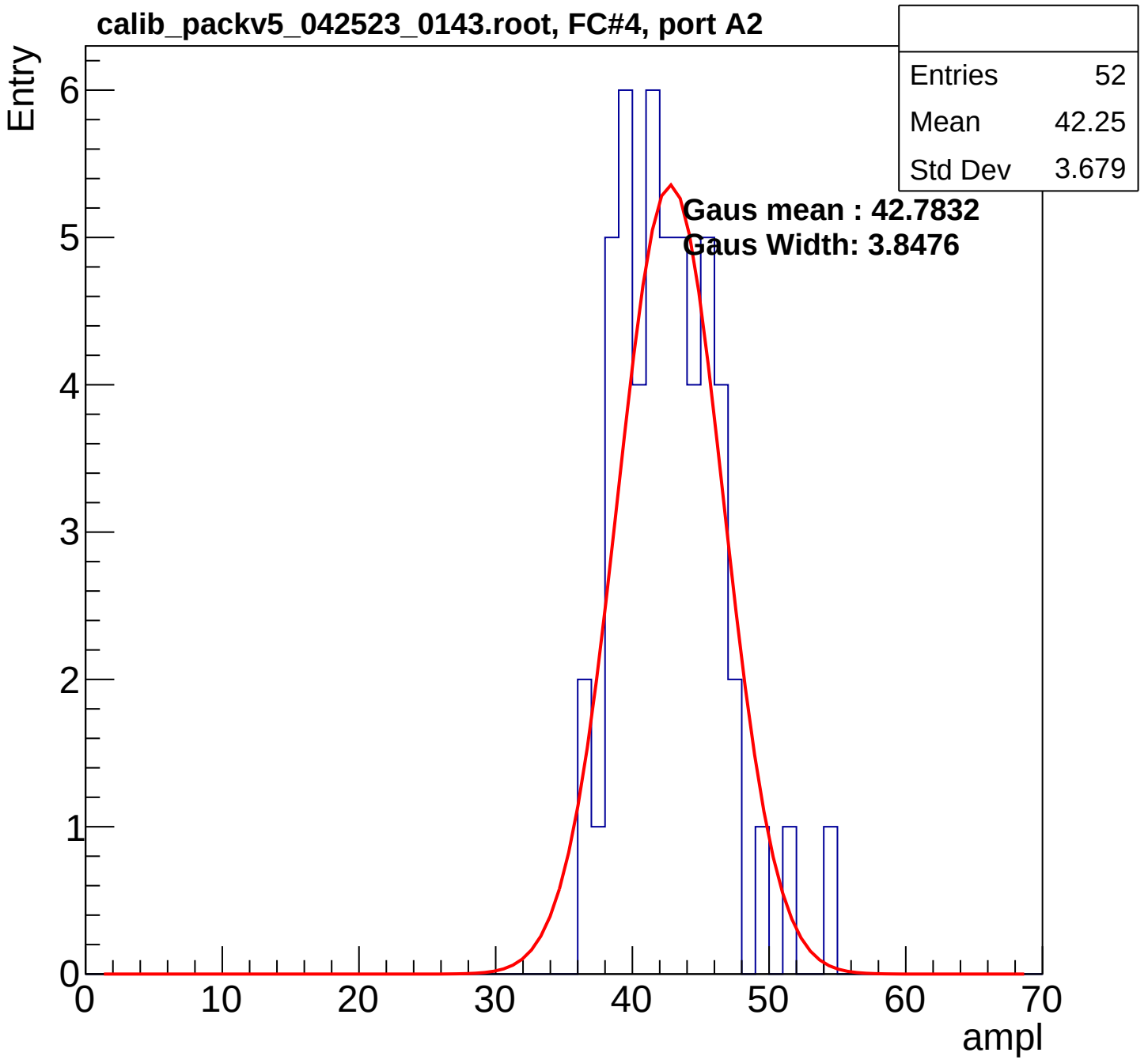

B1L100S, U17-ch115, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 58.46
Std Dev 7.958
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

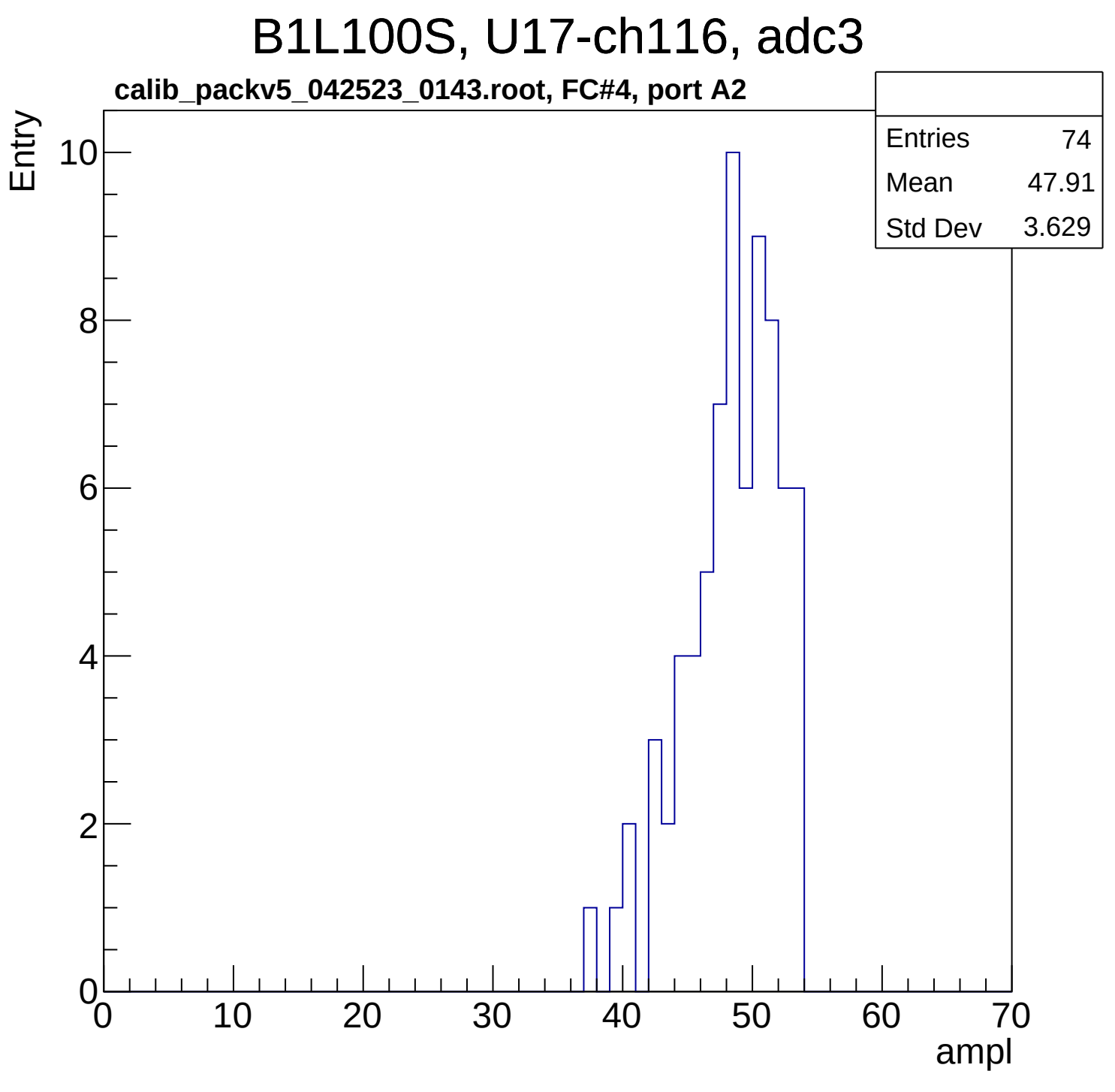

B1L100S, U17-ch115, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 62.33
Std Dev 0.9428
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

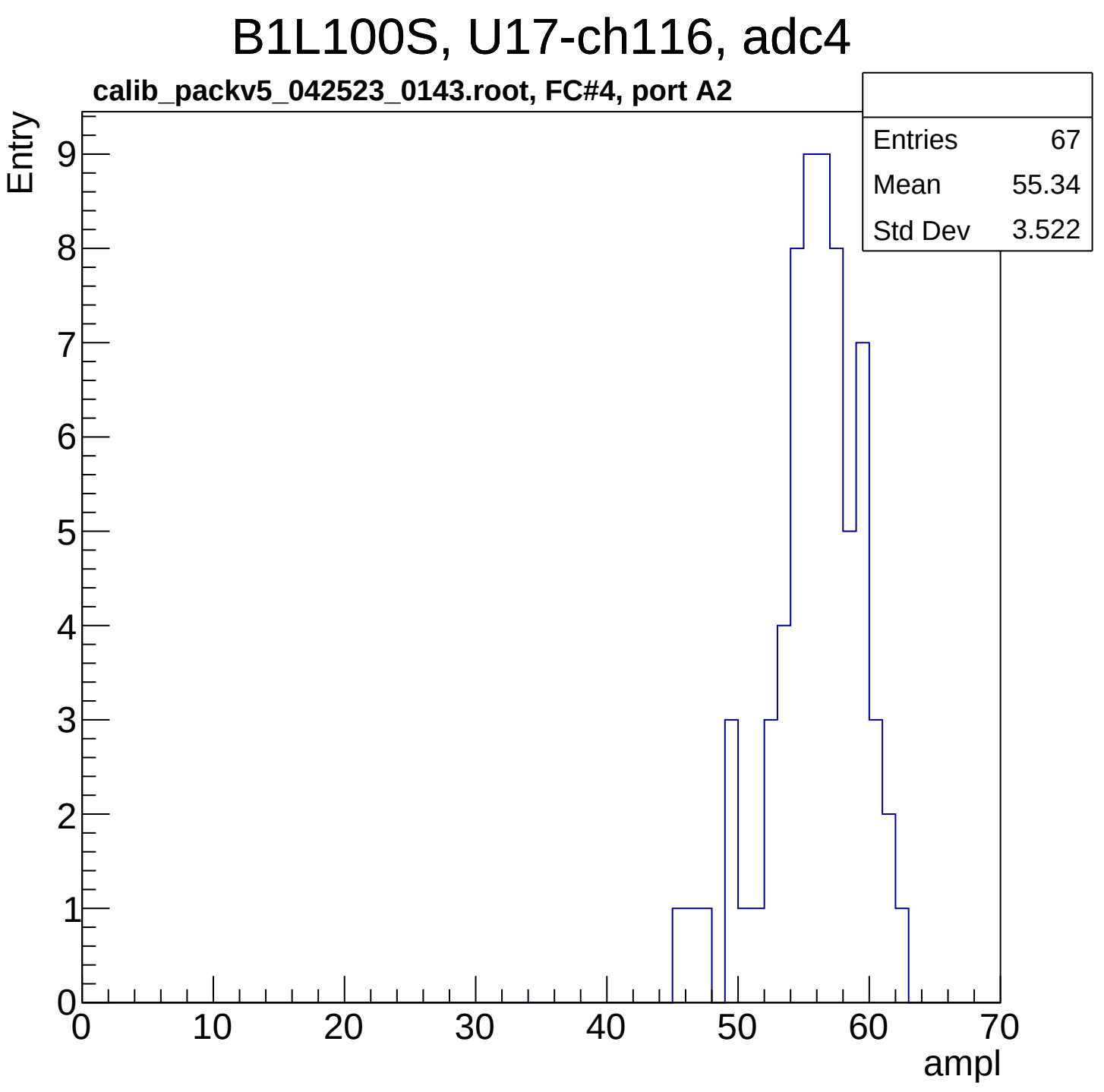

B1L100S, U17-ch115, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

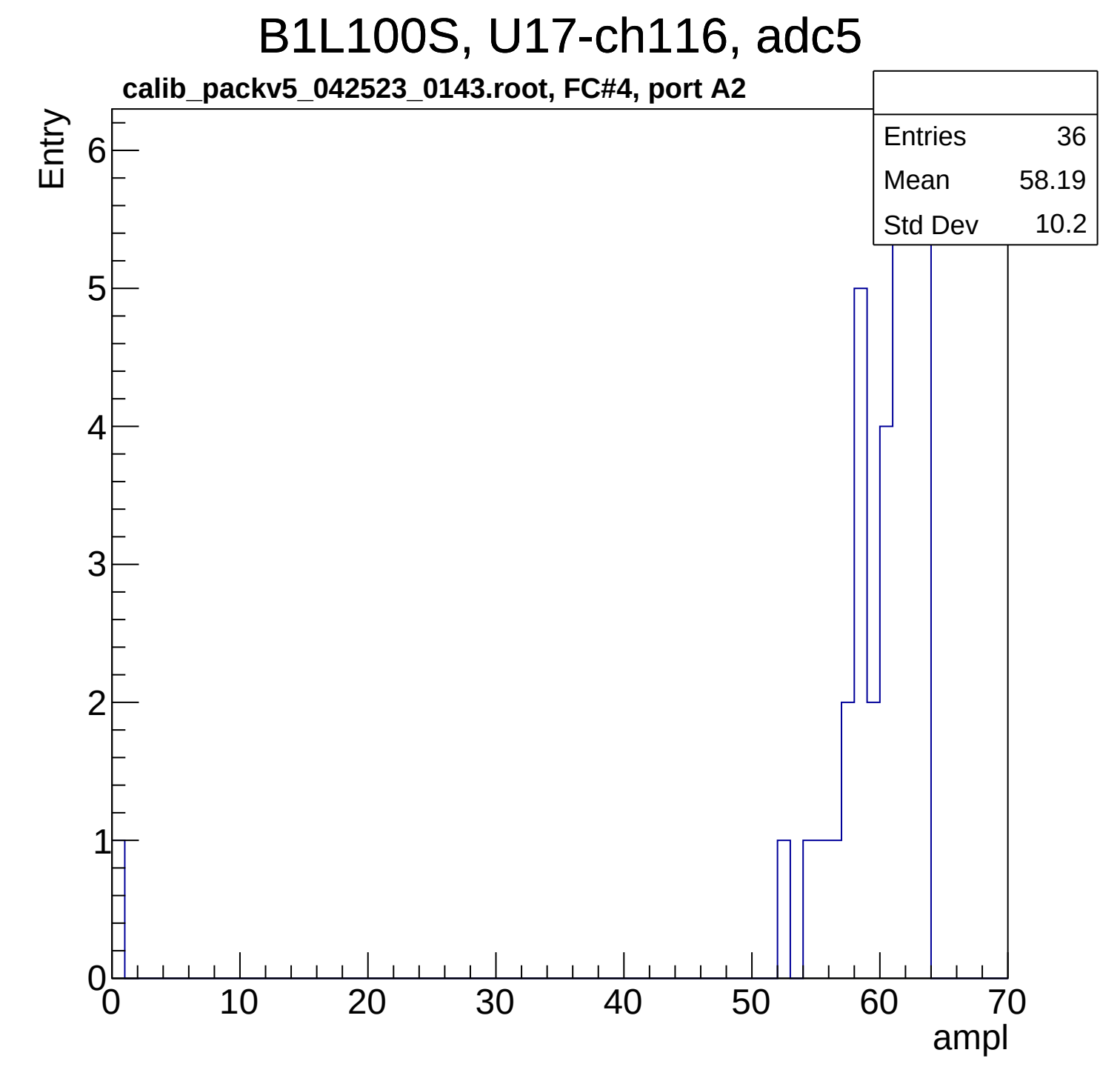

B1L100S, U17-ch116, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 82
Mean 26.88
Std Dev 5.713
Gaus mean : 28.1866
Gaus Width: 3.7765
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

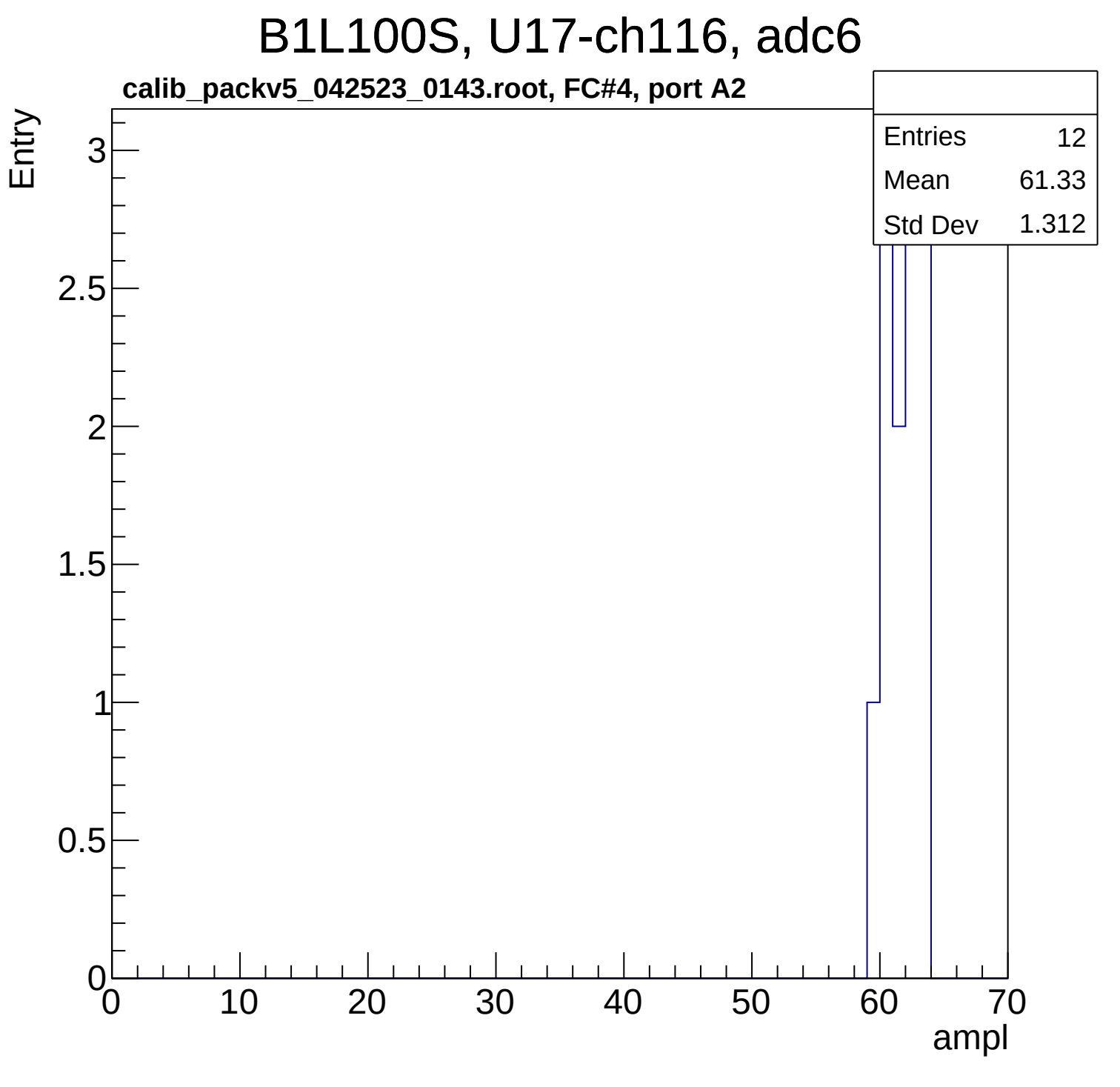

B1L100S, U17-ch116, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 74
Mean 36.05
Std Dev 3.657
Gaus mean : 36.1271
Gaus Width: 4.1570
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

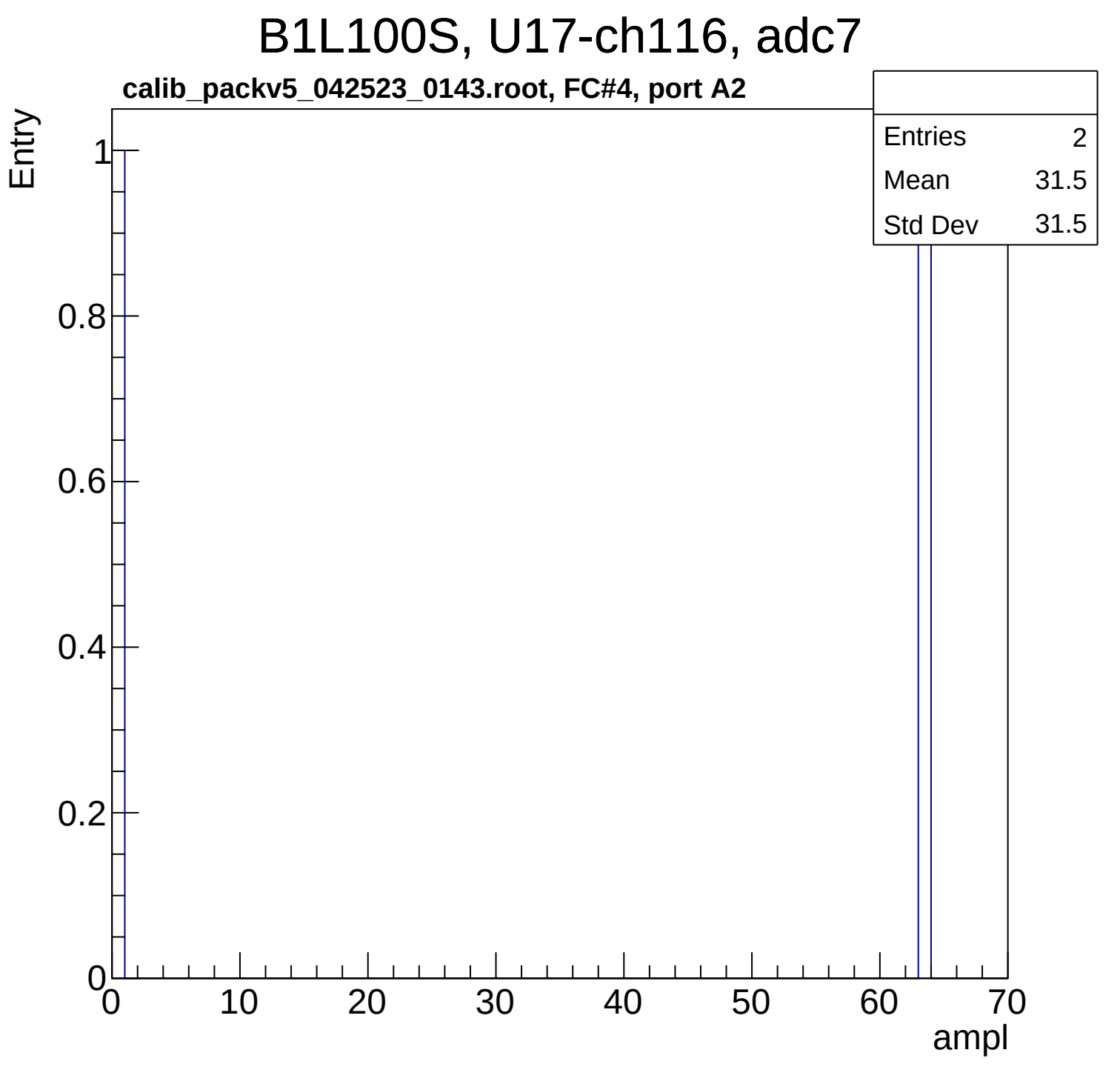

B1L100S, U17-ch116, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 52
Mean 42.25
Std Dev 3.679
Gaus mean : 42.7832
Gaus Width: 3.8476
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

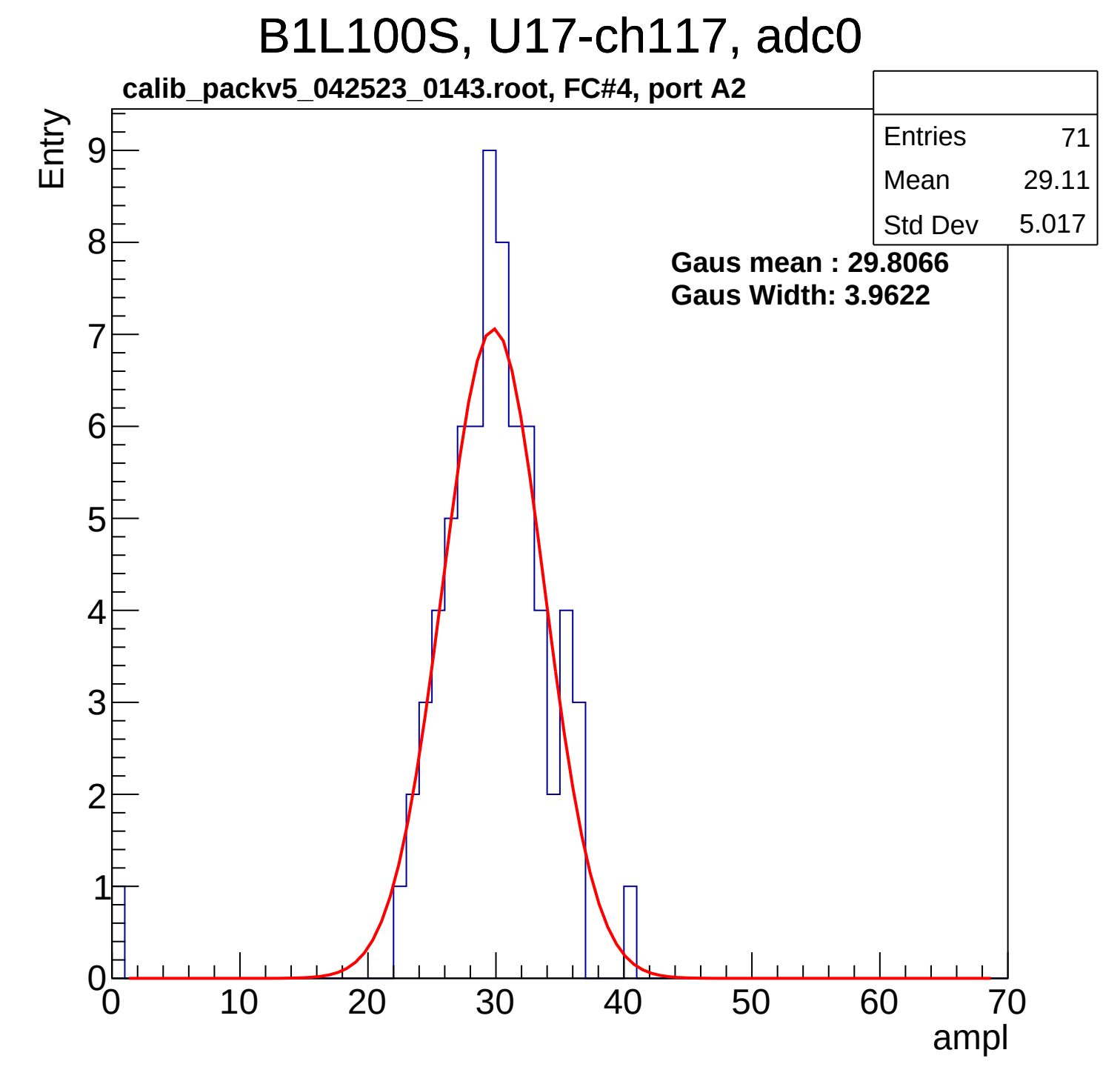

B1L100S, U17-ch116, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 74
Mean 47.91
Std Dev 3.629
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

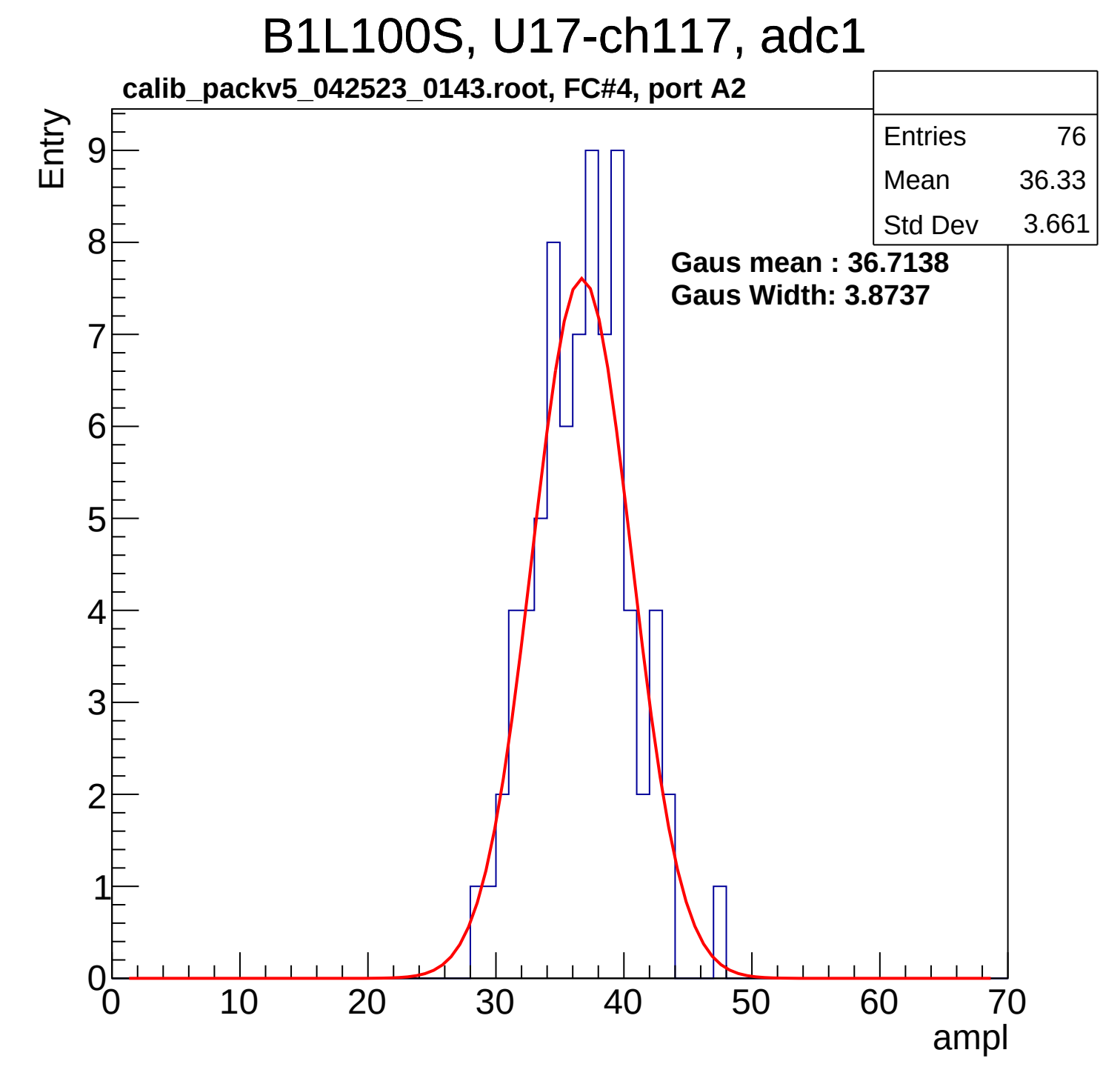

B1L100S, U17-ch116, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 55.34
Std Dev 3.522
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

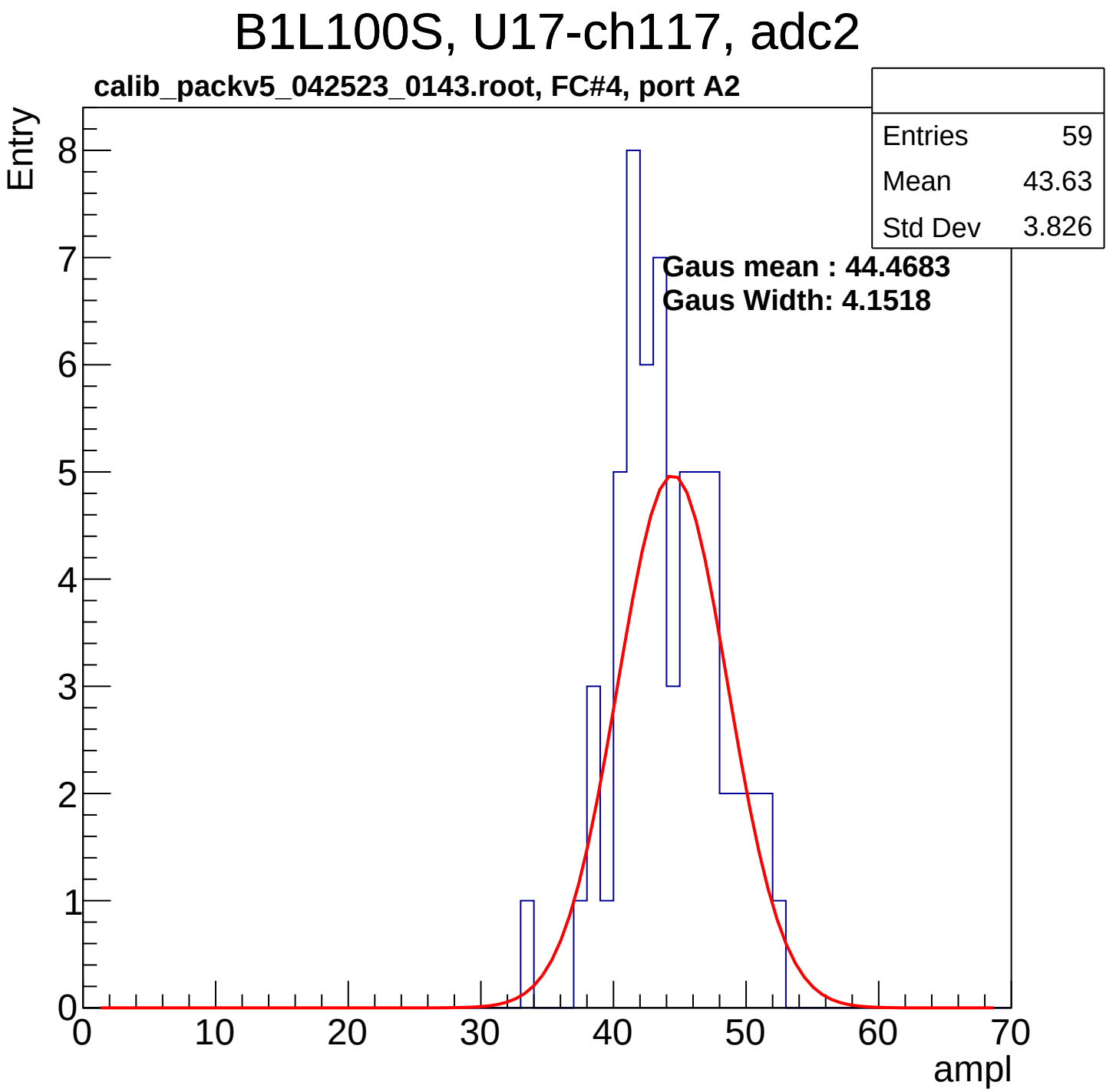

B1L100S, U17-ch116, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 36
Mean 58.19
Std Dev 10.2
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

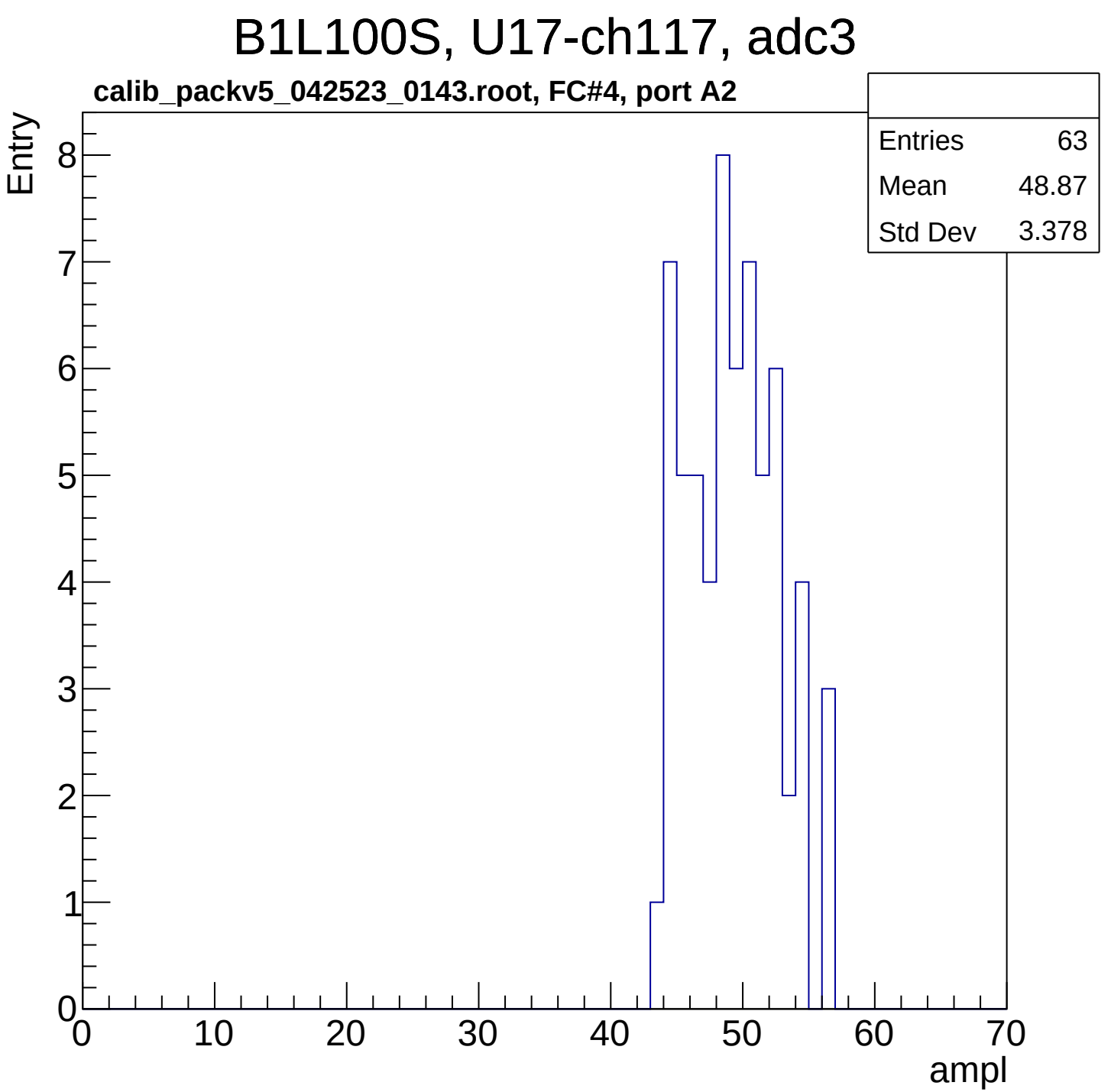

B1L100S, U17-ch116, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 12
Mean 61.33
Std Dev 1.312
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

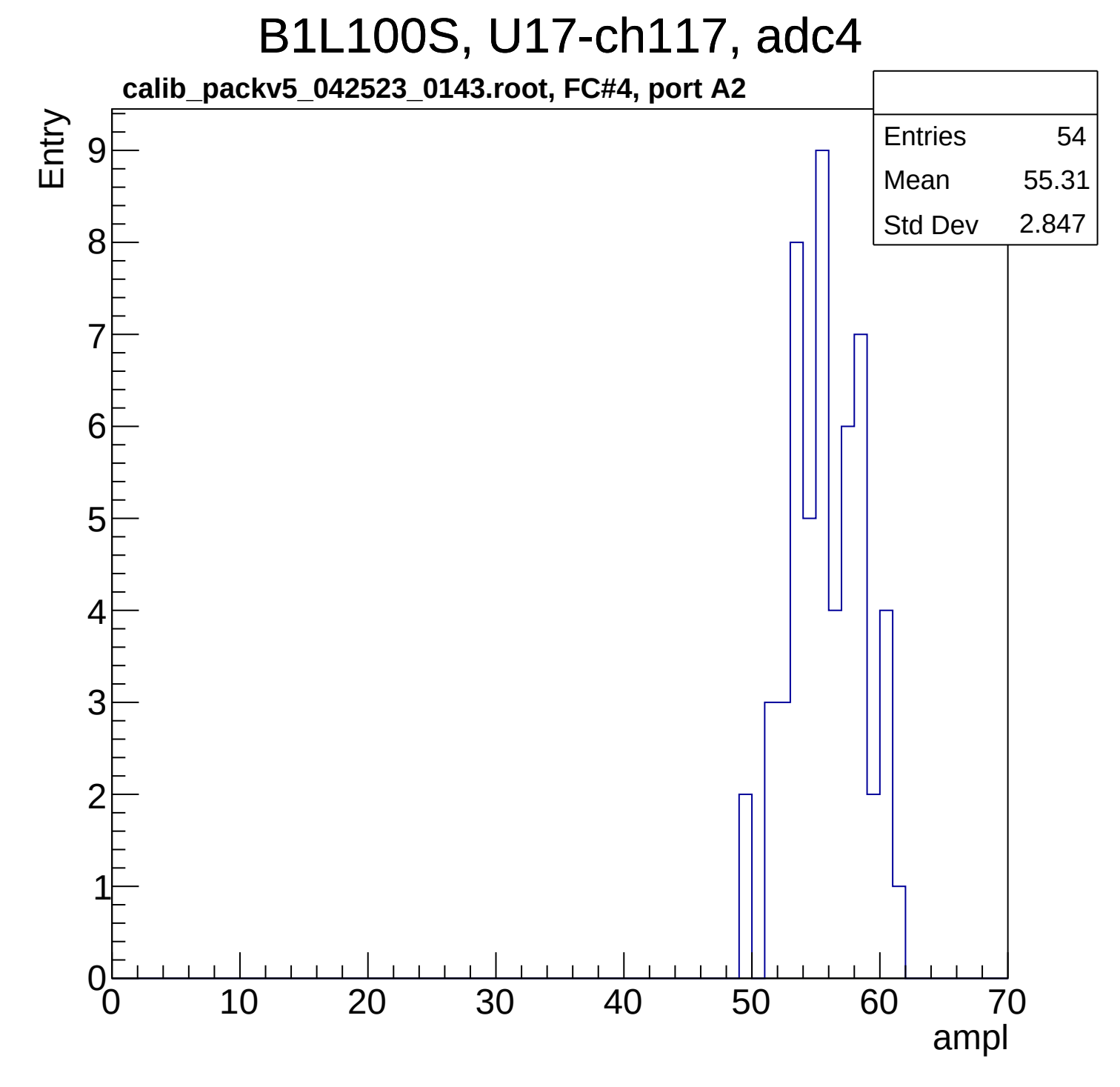

B1L100S, U17-ch116, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 31.5
Std Dev 31.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

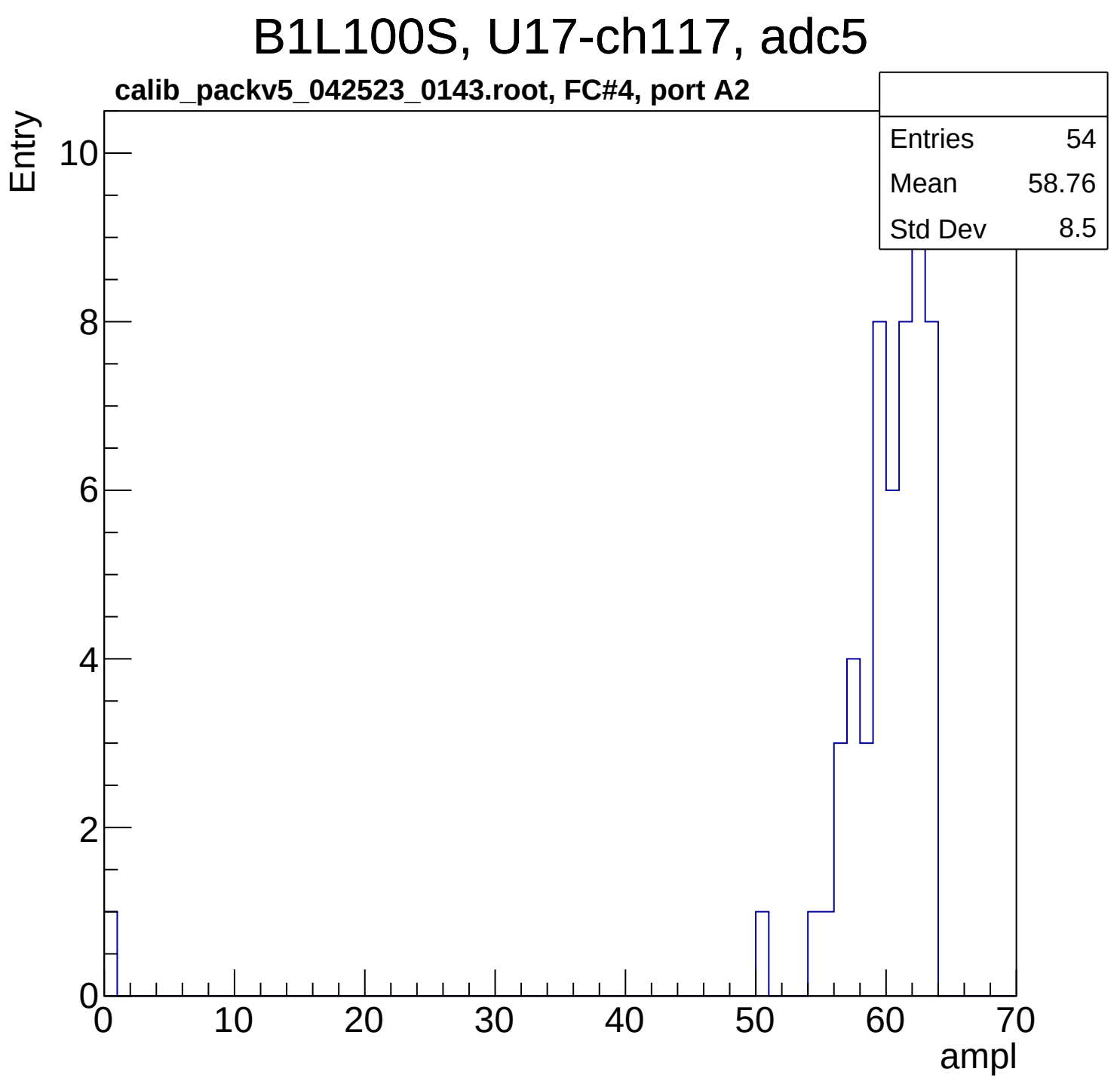

B1L100S, U17-ch117, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 29.11
Std Dev 5.017
Gaus mean : 29.8066
Gaus Width: 3.9622
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

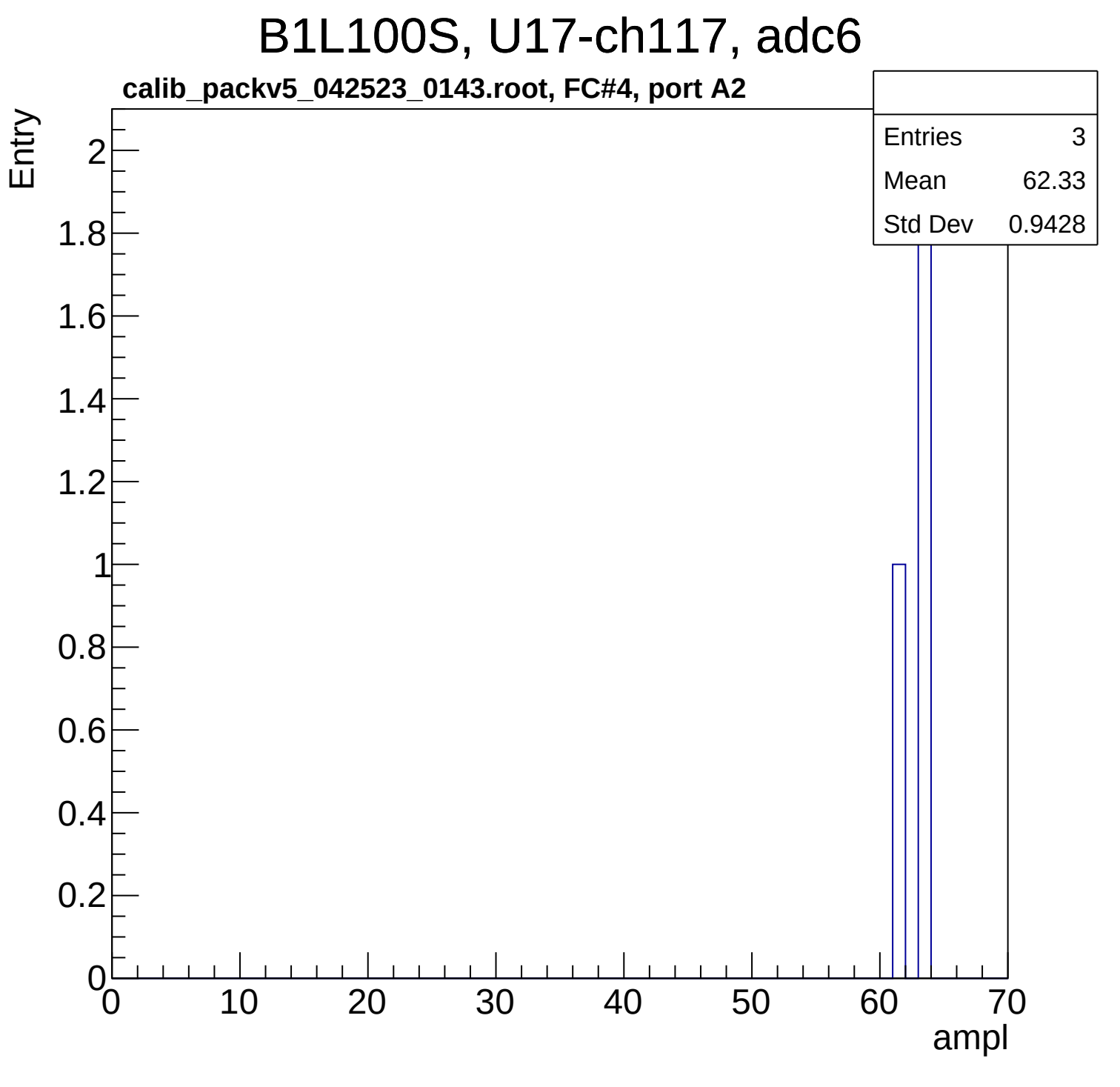

B1L100S, U17-ch117, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 76
Mean 36.33
Std Dev 3.661
Gaus mean : 36.7138
Gaus Width: 3.8737
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

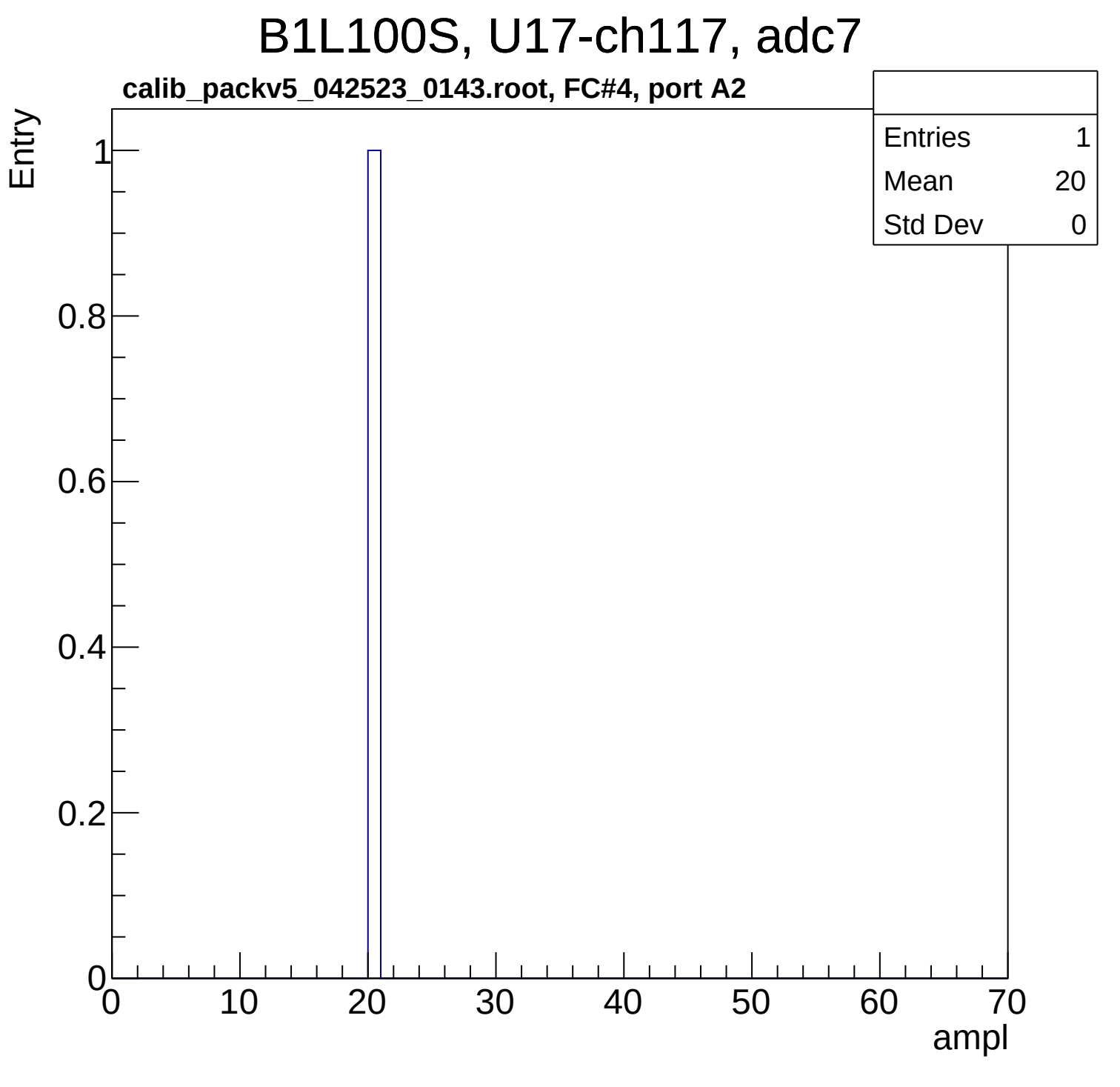

B1L100S, U17-ch117, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 43.63
Std Dev 3.826
Gaus mean : 44.4683
Gaus Width: 4.1518
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

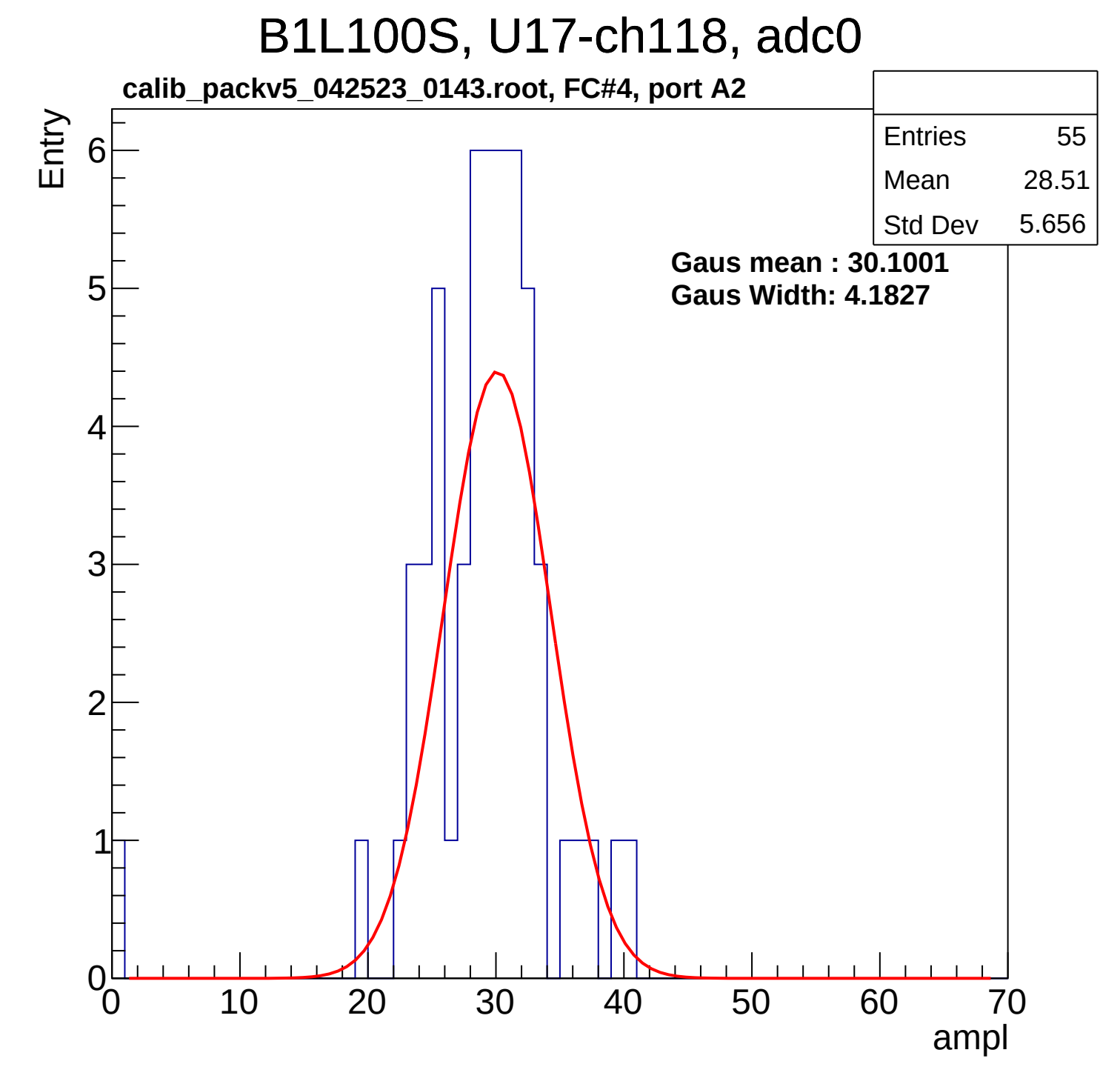

B1L100S, U17-ch117, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 48.87
Std Dev 3.378
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

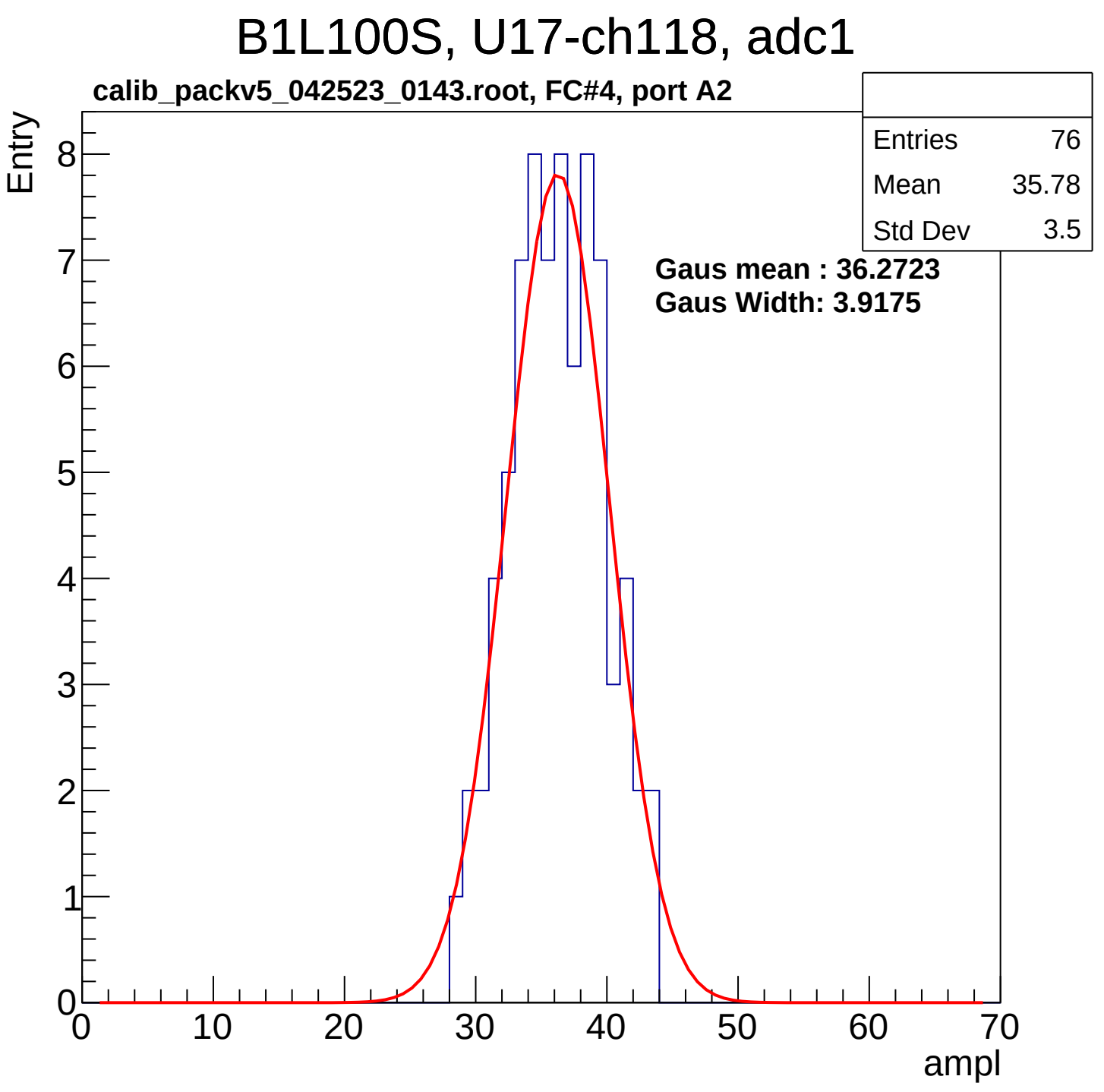

B1L100S, U17-ch117, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 55.31
Std Dev 2.847
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

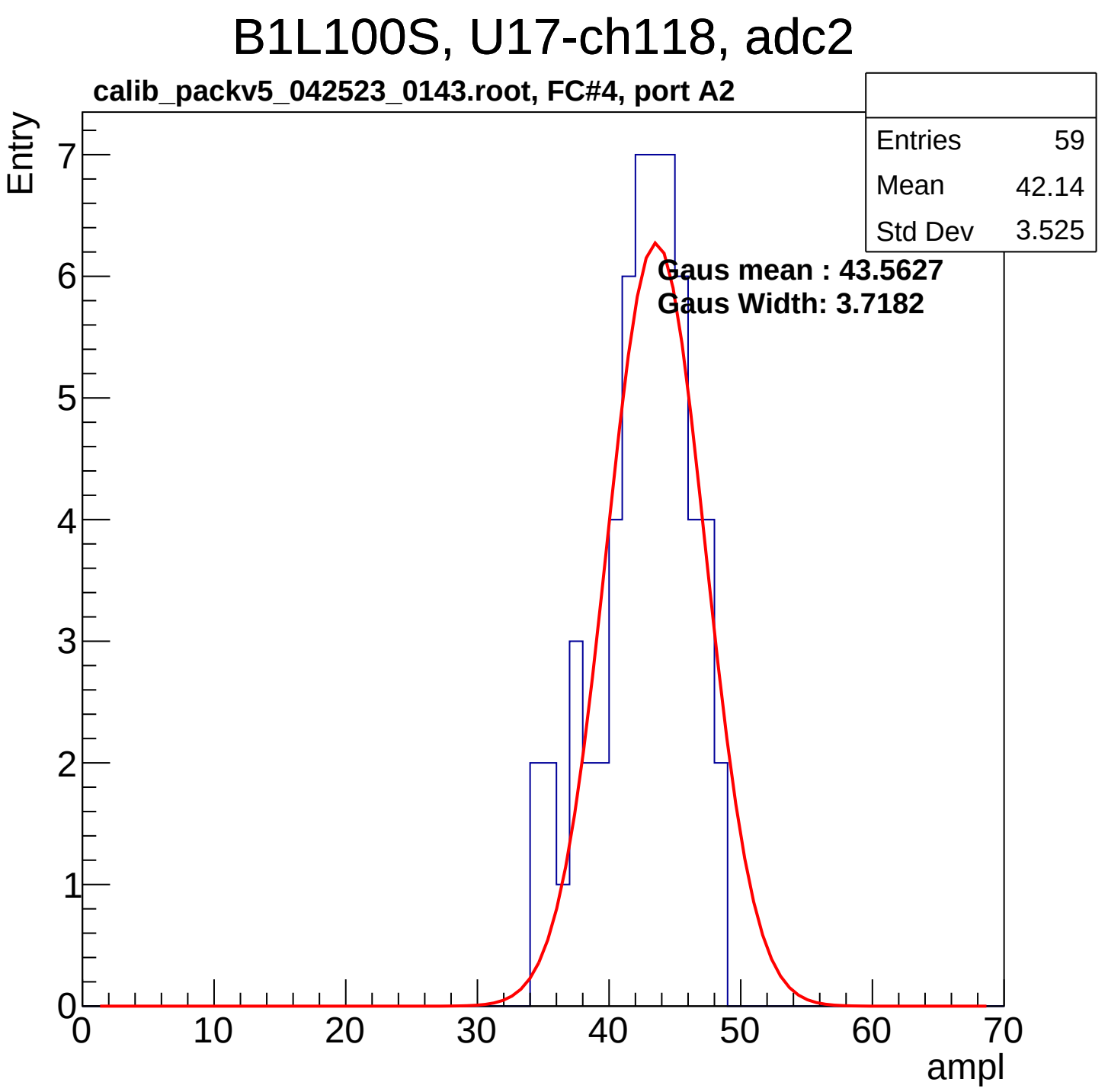

B1L100S, U17-ch117, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 58.76
Std Dev 8.5
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

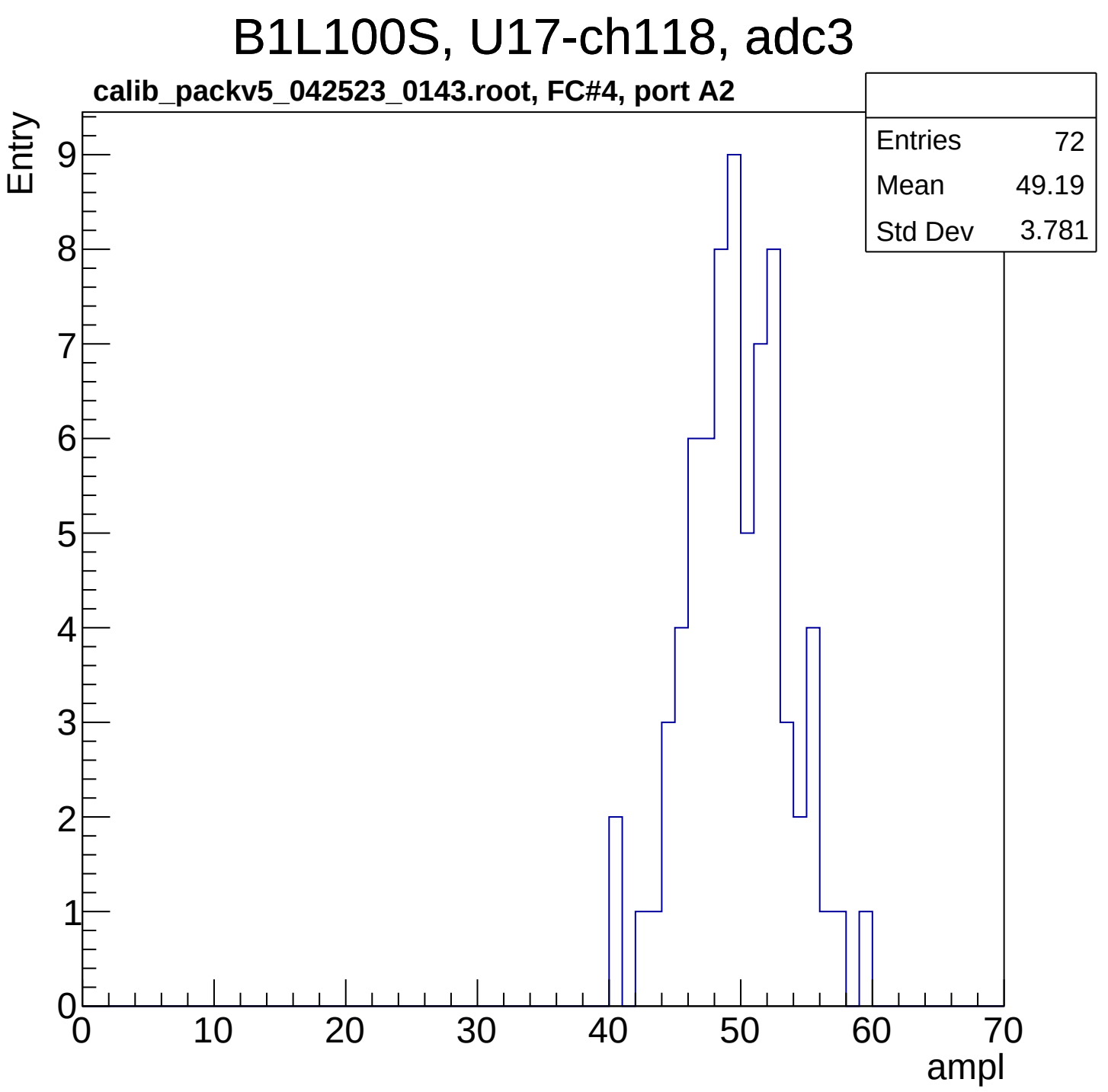

B1L100S, U17-ch117, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 62.33
Std Dev 0.9428
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L100S, U17-ch117, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 20
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B1L100S, U17-ch118, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 28.51
Std Dev 5.656
Gaus mean : 30.1001
Gaus Width: 4.1827
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L100S, U17-ch118, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 76
Mean 35.78
Std Dev 3.5
Gaus mean : 36.2723
Gaus Width: 3.9175
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch118, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 42.14
Std Dev 3.525
Gaus mean : 43.5627
Gaus Width: 3.7182
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U17-ch118, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 49.19
Std Dev 3.781
Entry
ampl
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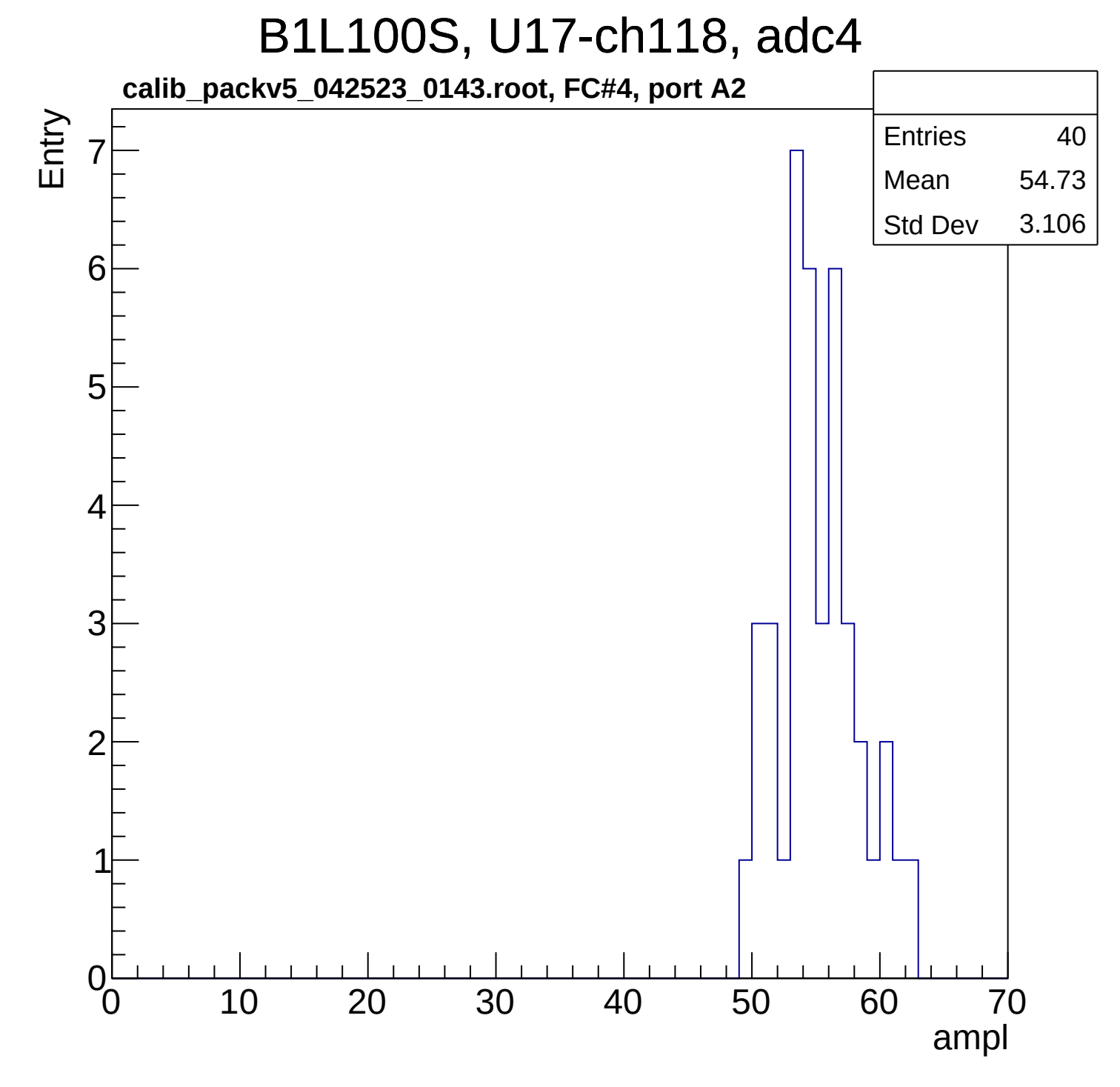
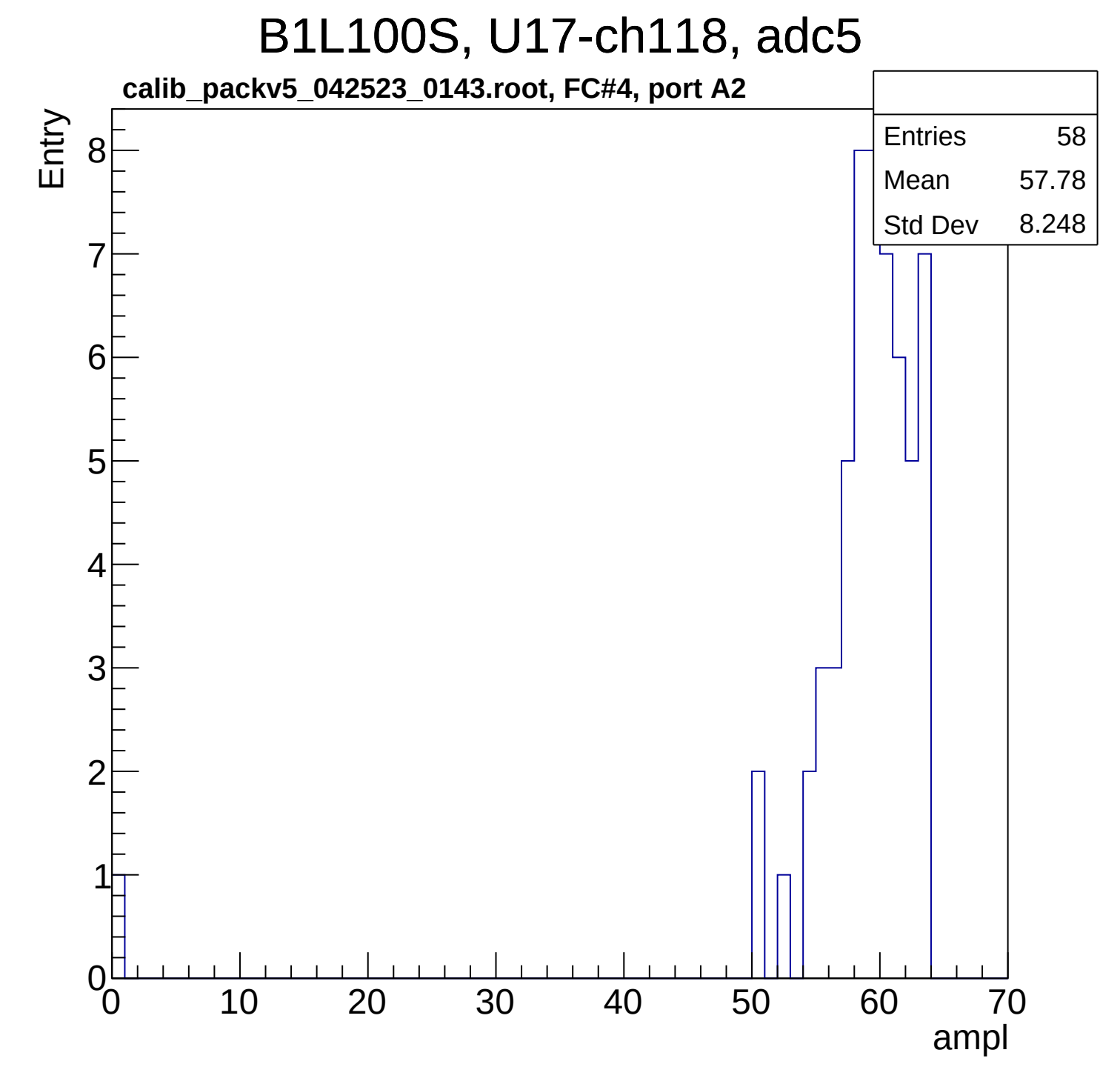
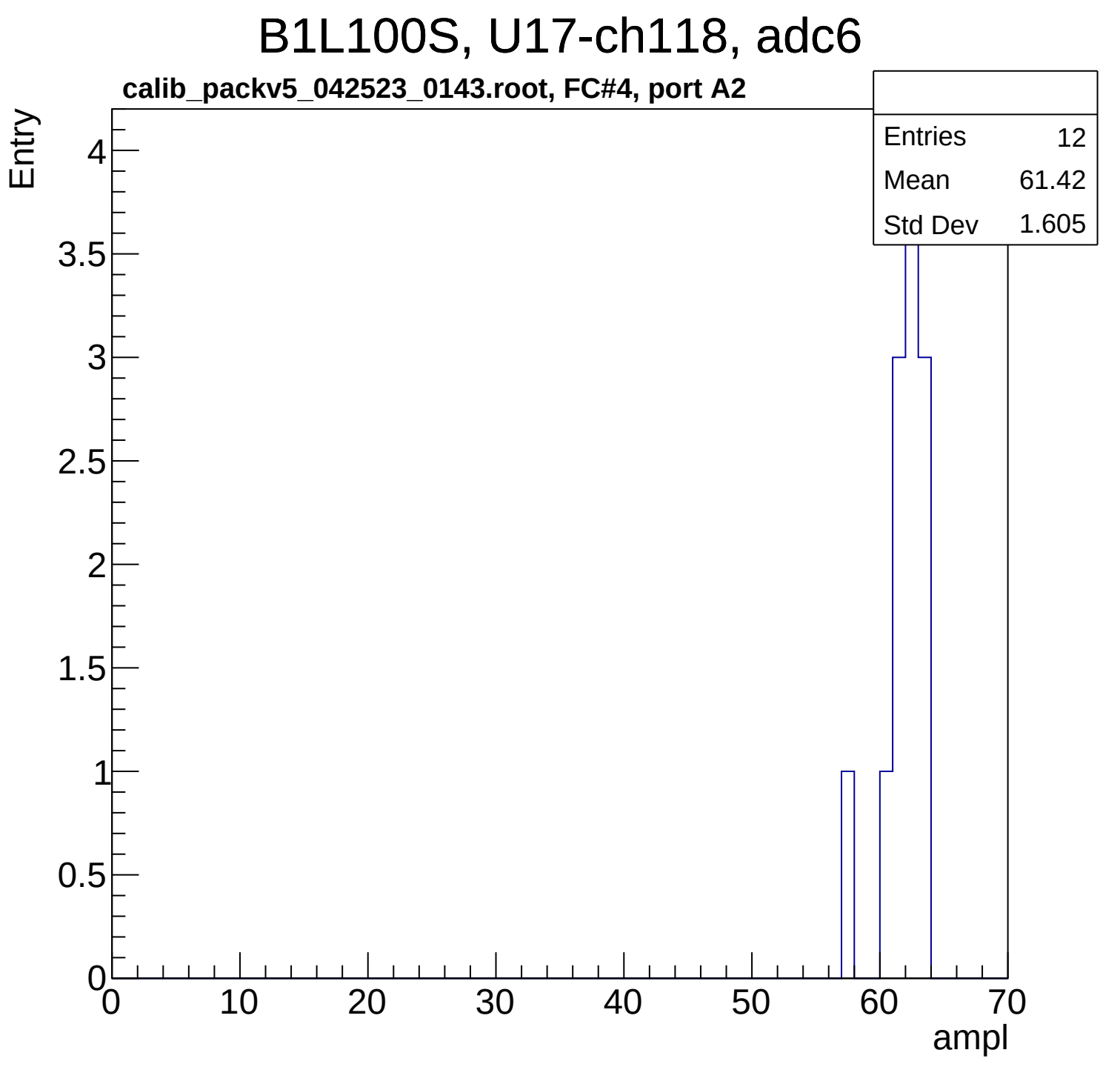
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch118, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 40
Mean 54.73
Std Dev 3.106
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U17-ch118, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 57.78
Std Dev 8.248
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch118, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 12
Mean 61.42
Std Dev 1.605
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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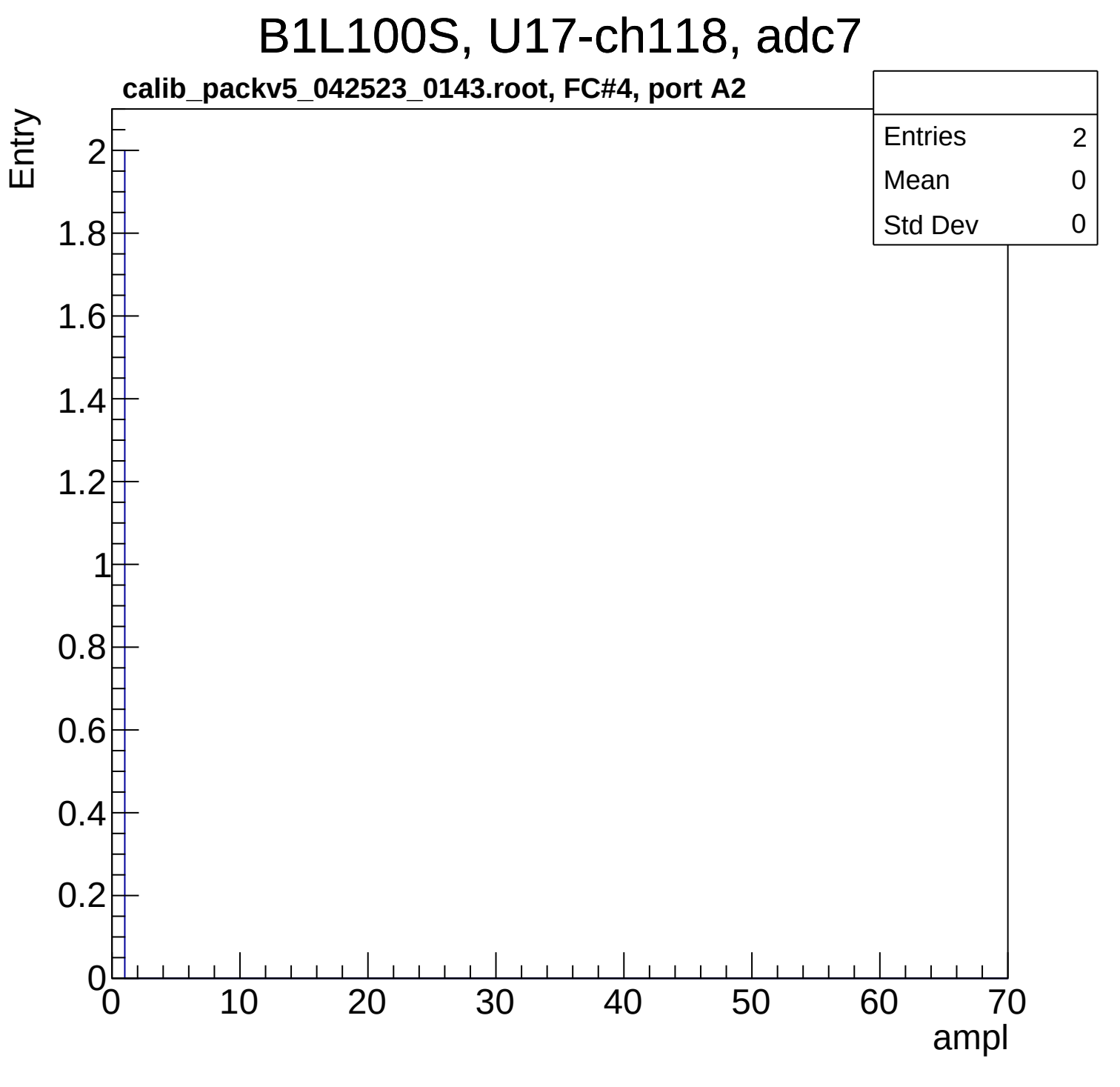
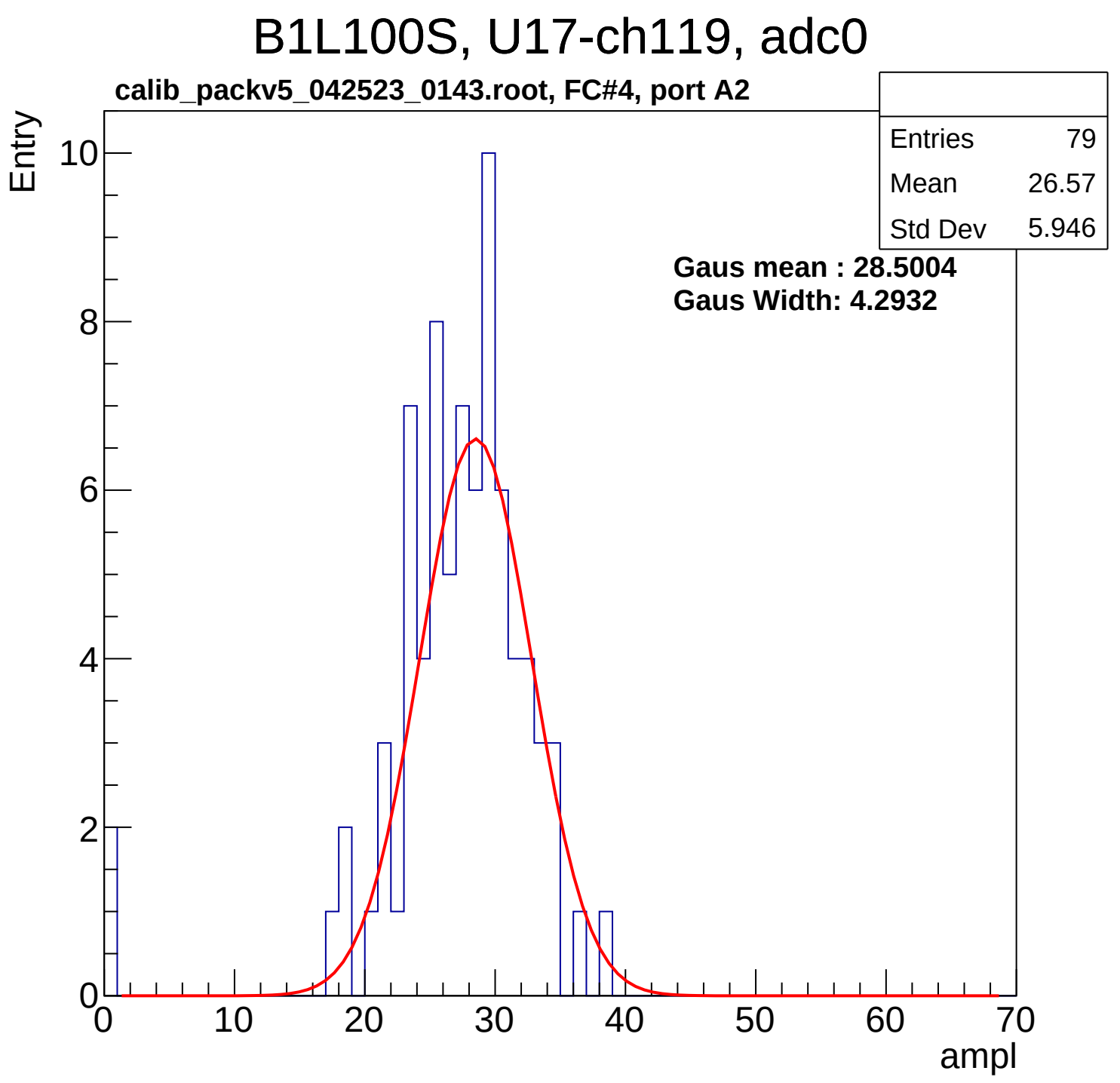
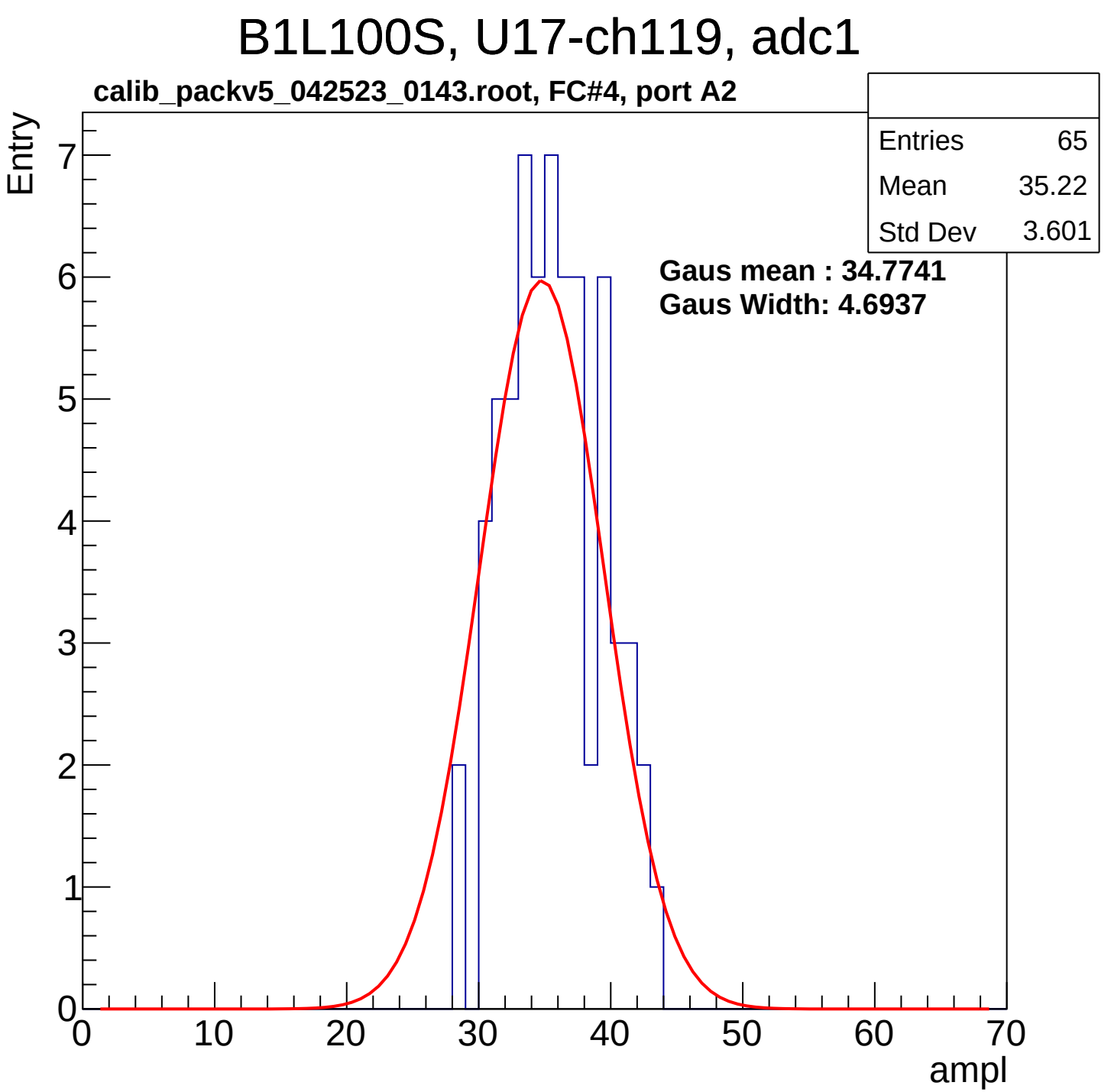
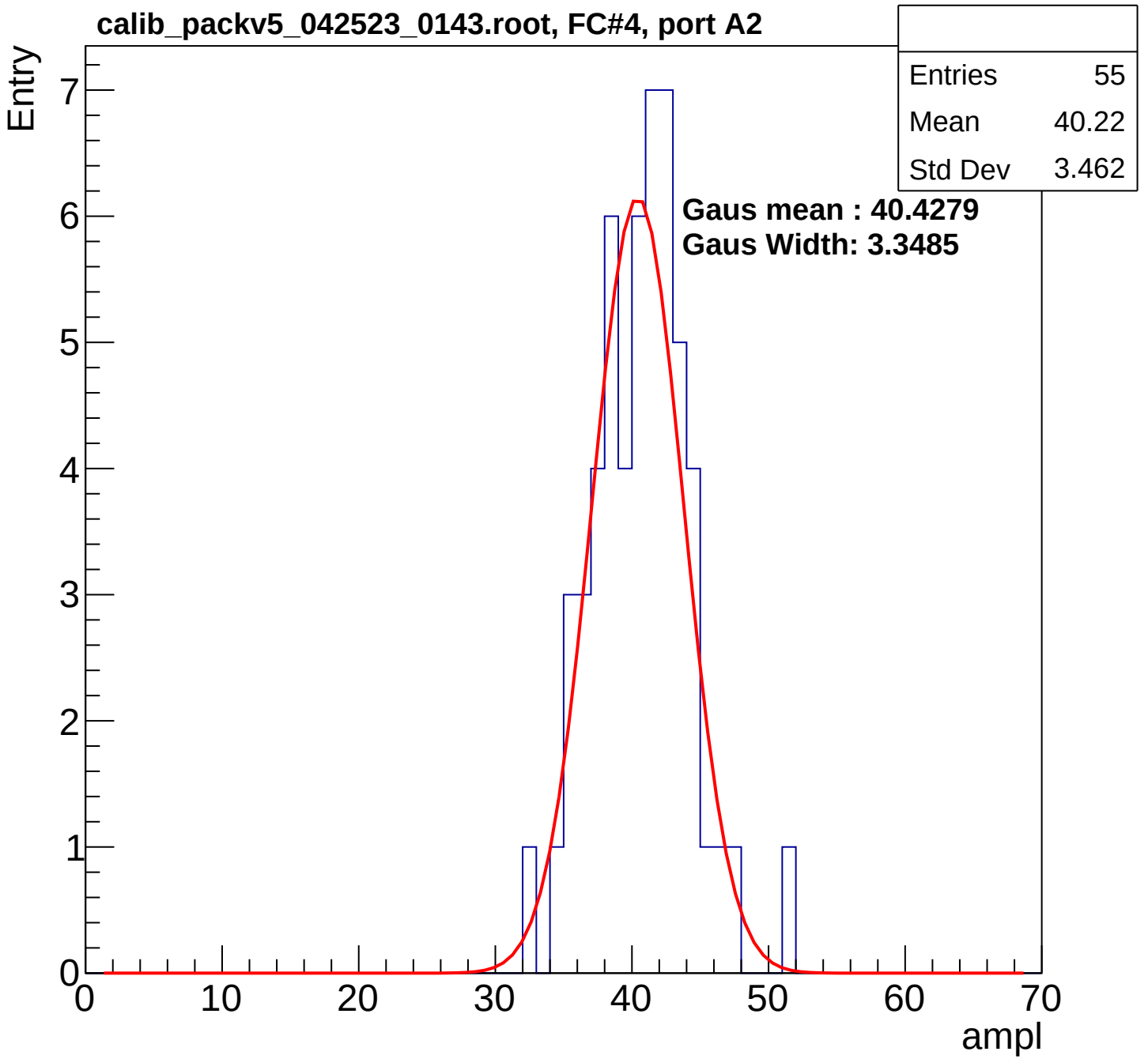
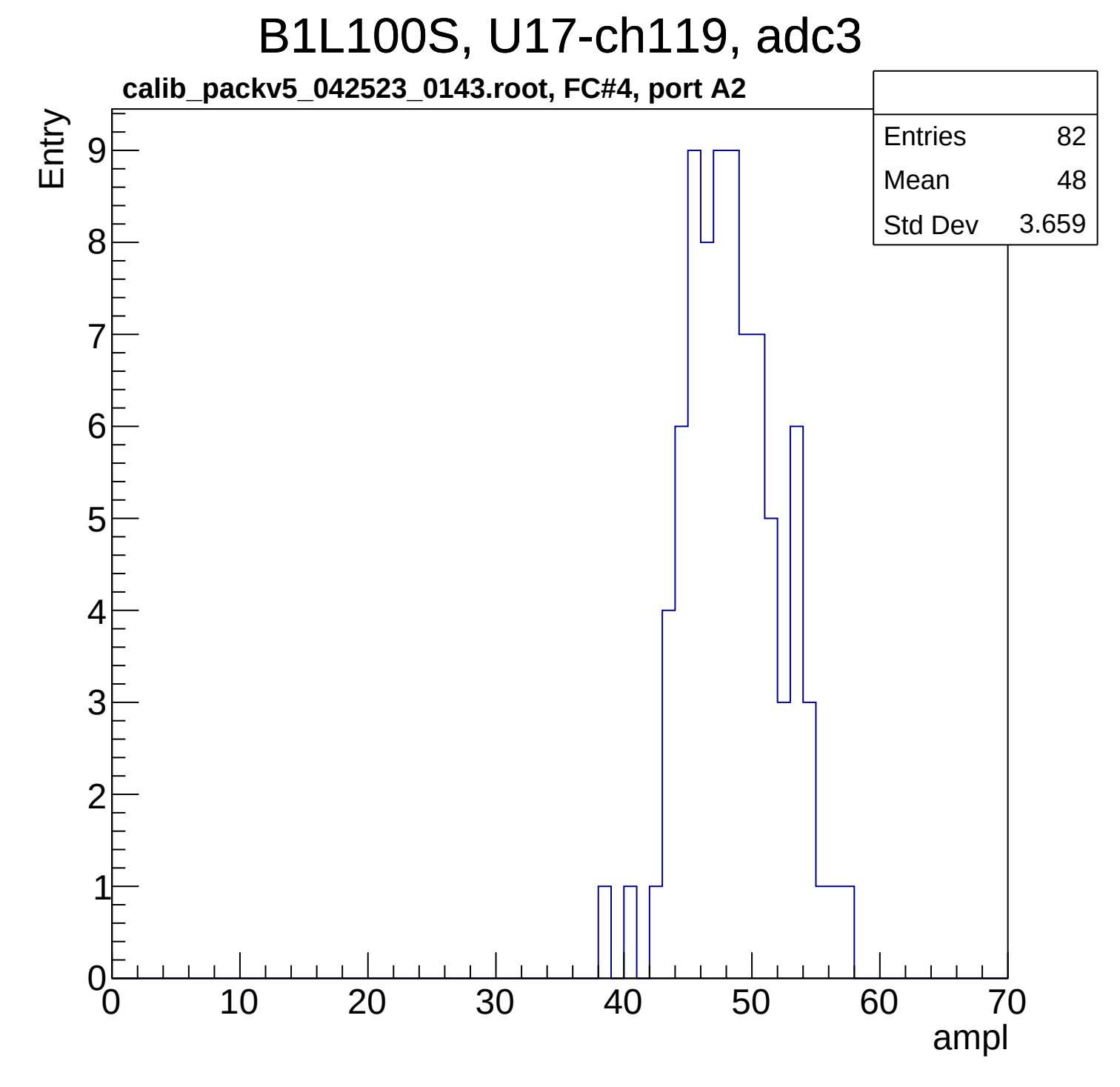
40
50
60
70

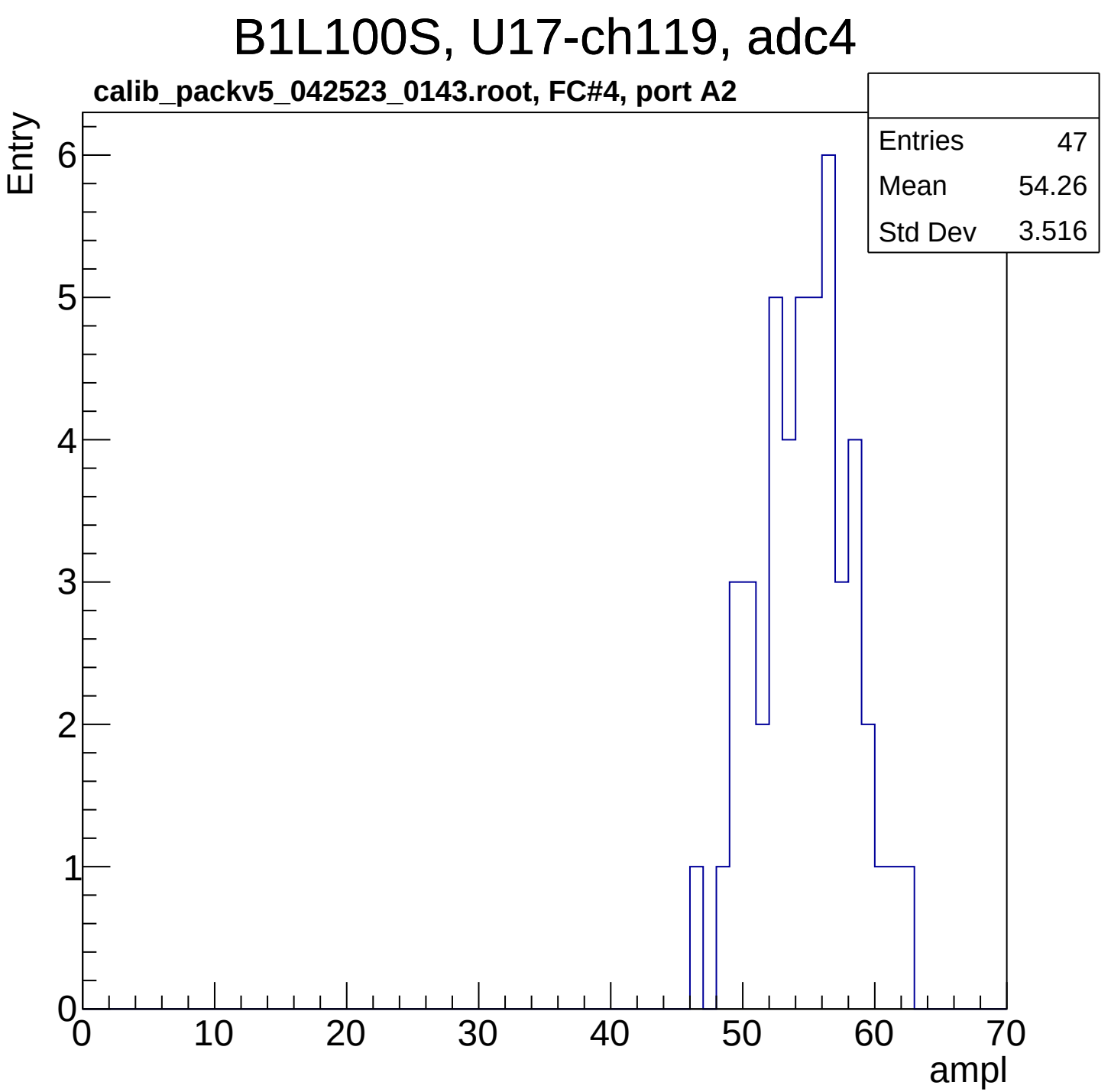

B1L100S, U17-ch118, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

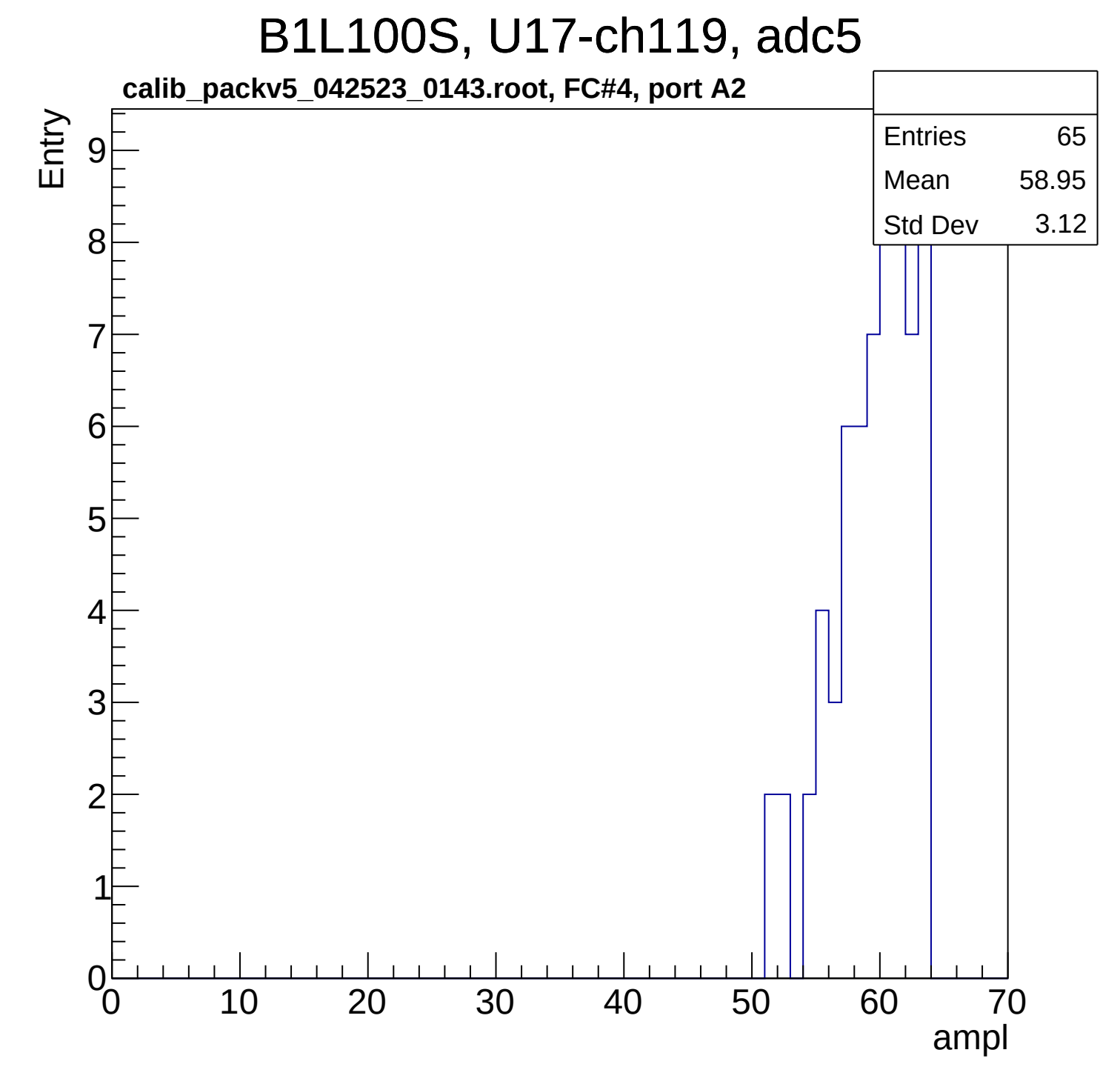

B1L100S, U17-ch119, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 79
Mean 26.57
Std Dev 5.946
Gaus mean : 28.5004
Gaus Width: 4.2932
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U17-ch119, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 35.22
Std Dev 3.601
Gaus mean : 34.7741
Gaus Width: 4.6937
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U17-ch119, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 40.22
Std Dev 3.462
Gaus mean : 40.4279
Gaus Width: 3.3485
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U17-ch119, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 82
Mean 48
Std Dev 3.659
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch119, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 47
Mean 54.26
Std Dev 3.516
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L100S, U17-ch119, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 58.95
Std Dev 3.12
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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40
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60
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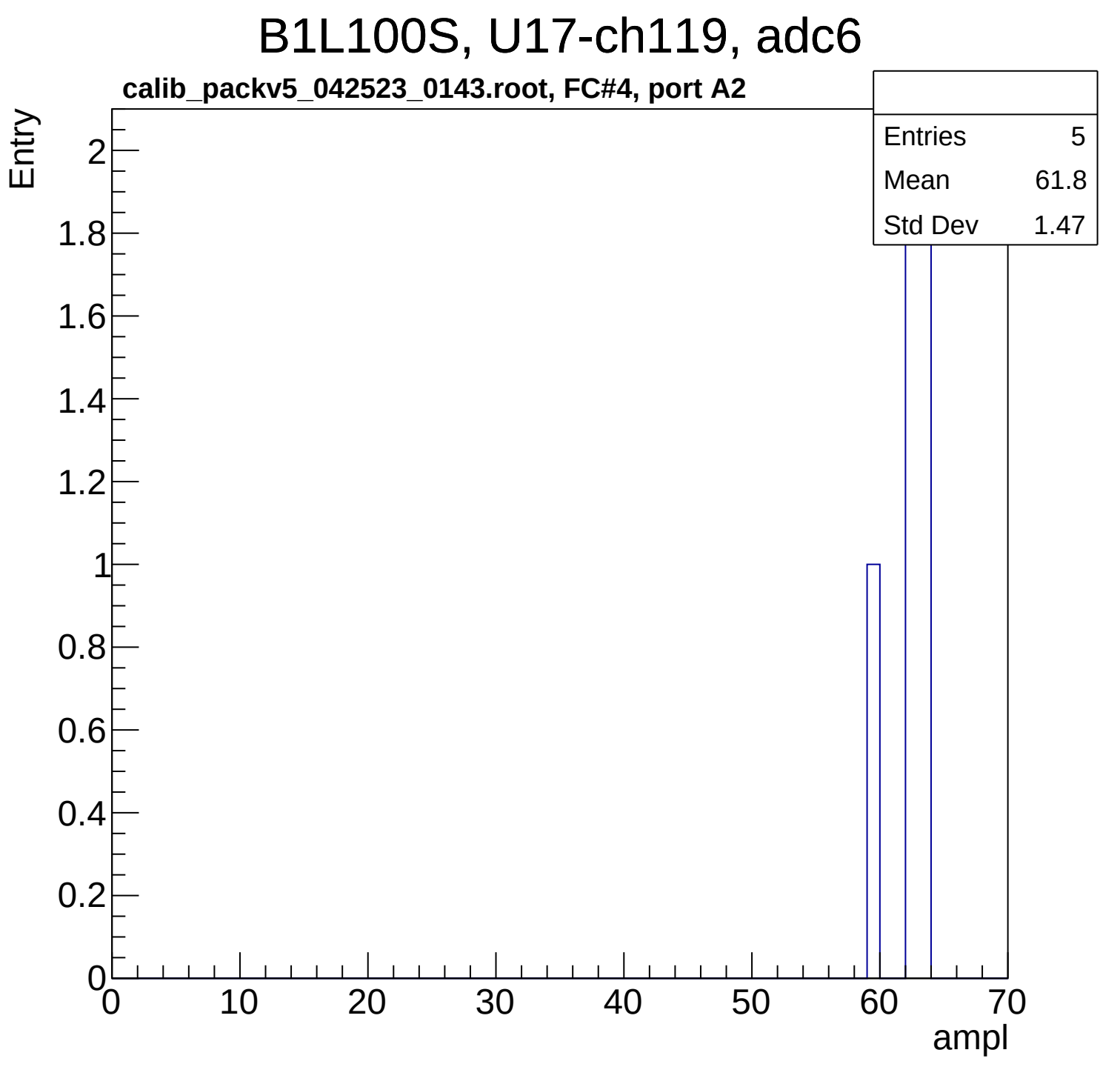
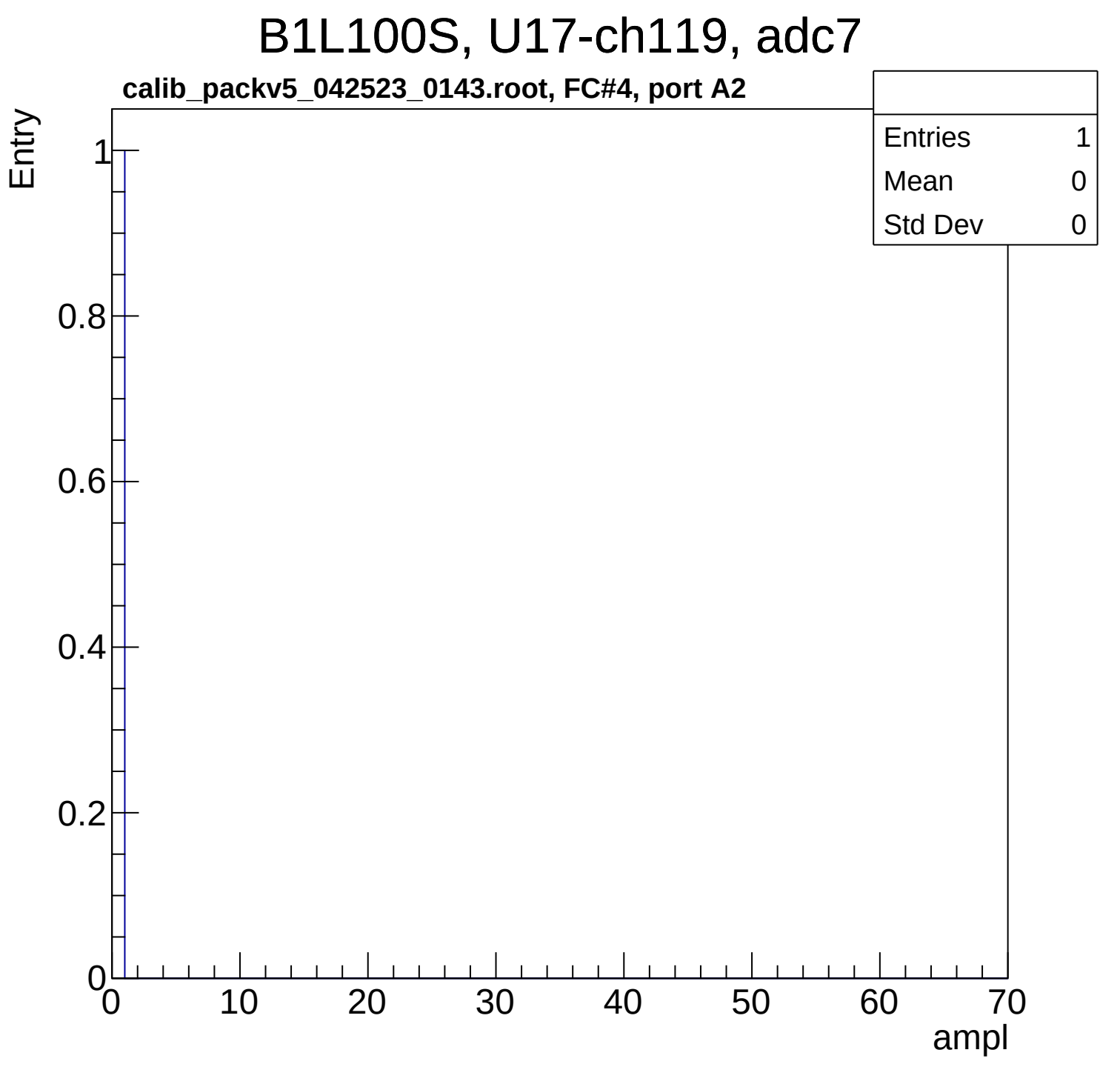
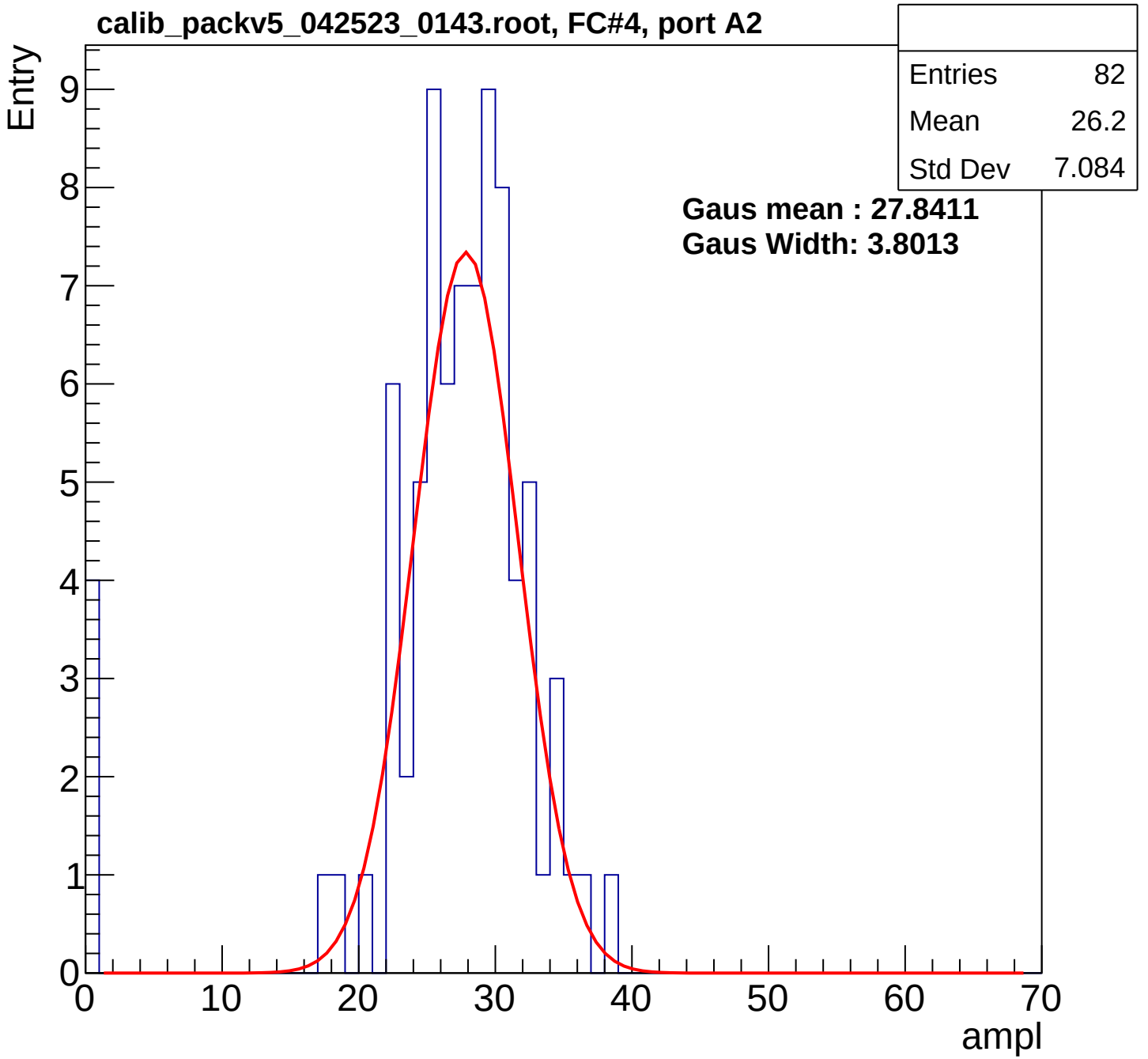
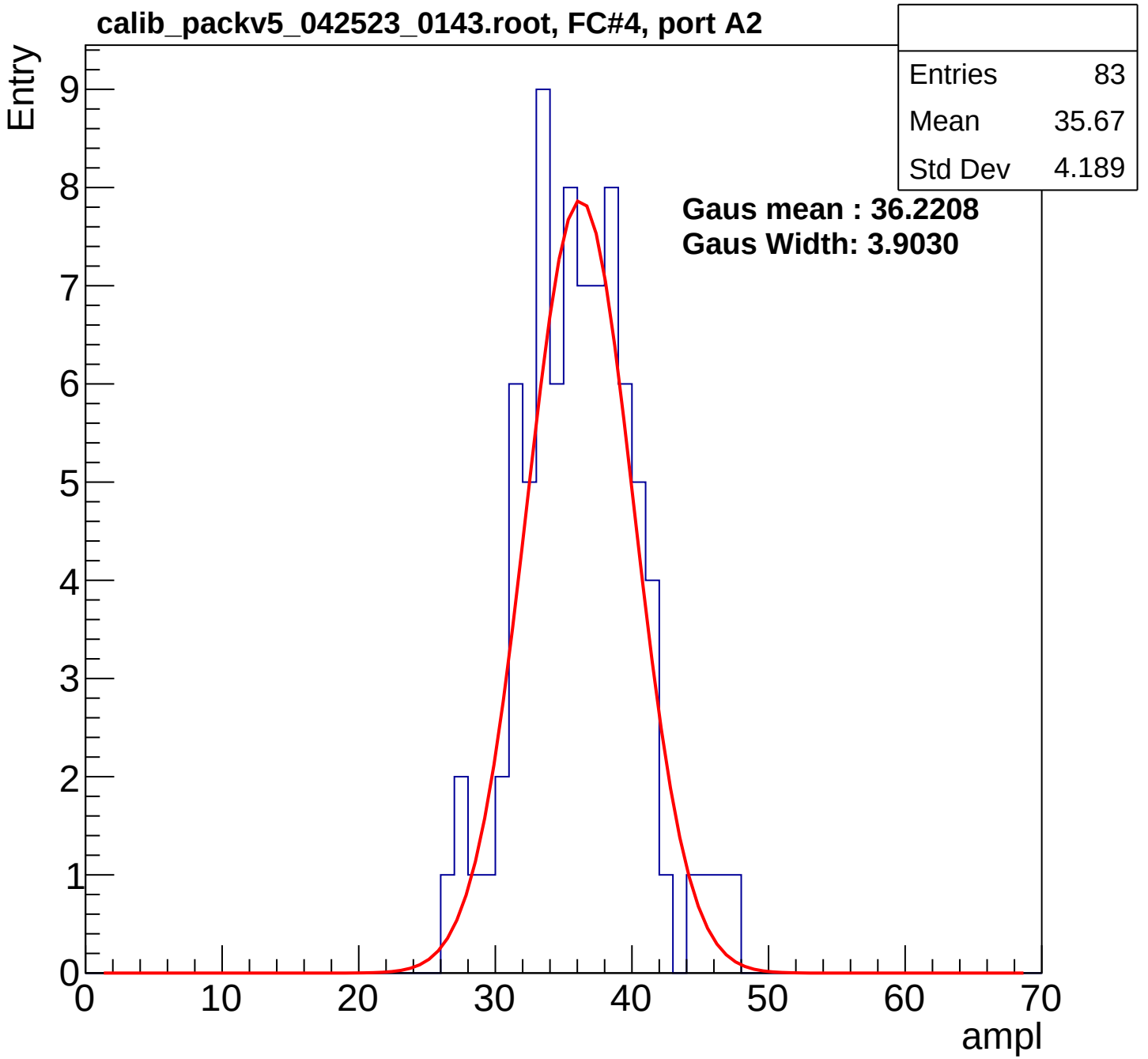

B1L100S, U17-ch119, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 5
Mean 61.8
Std Dev 1.47
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L100S, U17-ch119, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch120, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 82
Mean 26.2
Std Dev 7.084
Gaus mean : 27.8411
Gaus Width: 3.8013
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch120, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 83
Mean 35.67
Std Dev 4.189
Gaus mean : 36.2208
Gaus Width: 3.9030
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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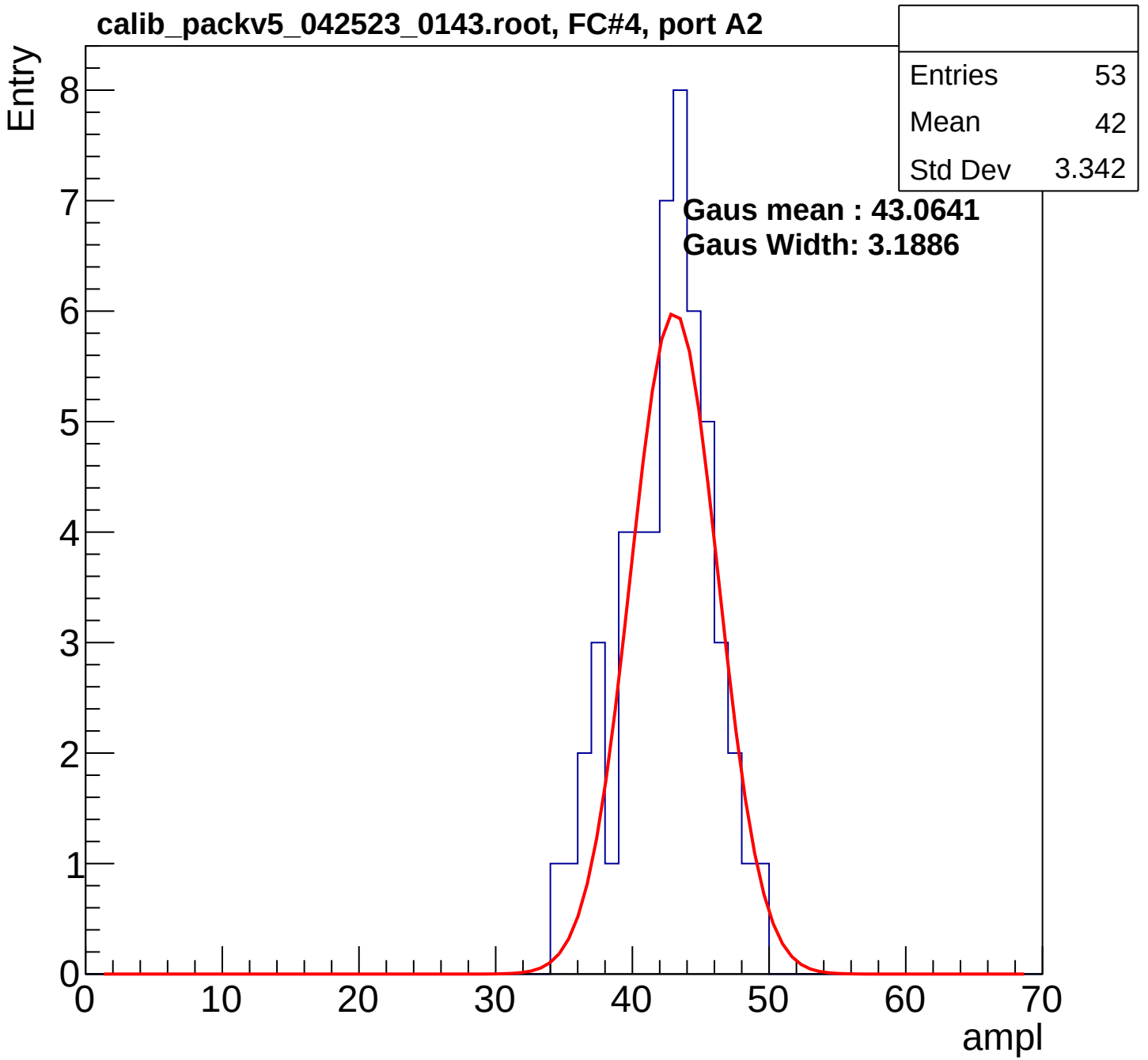
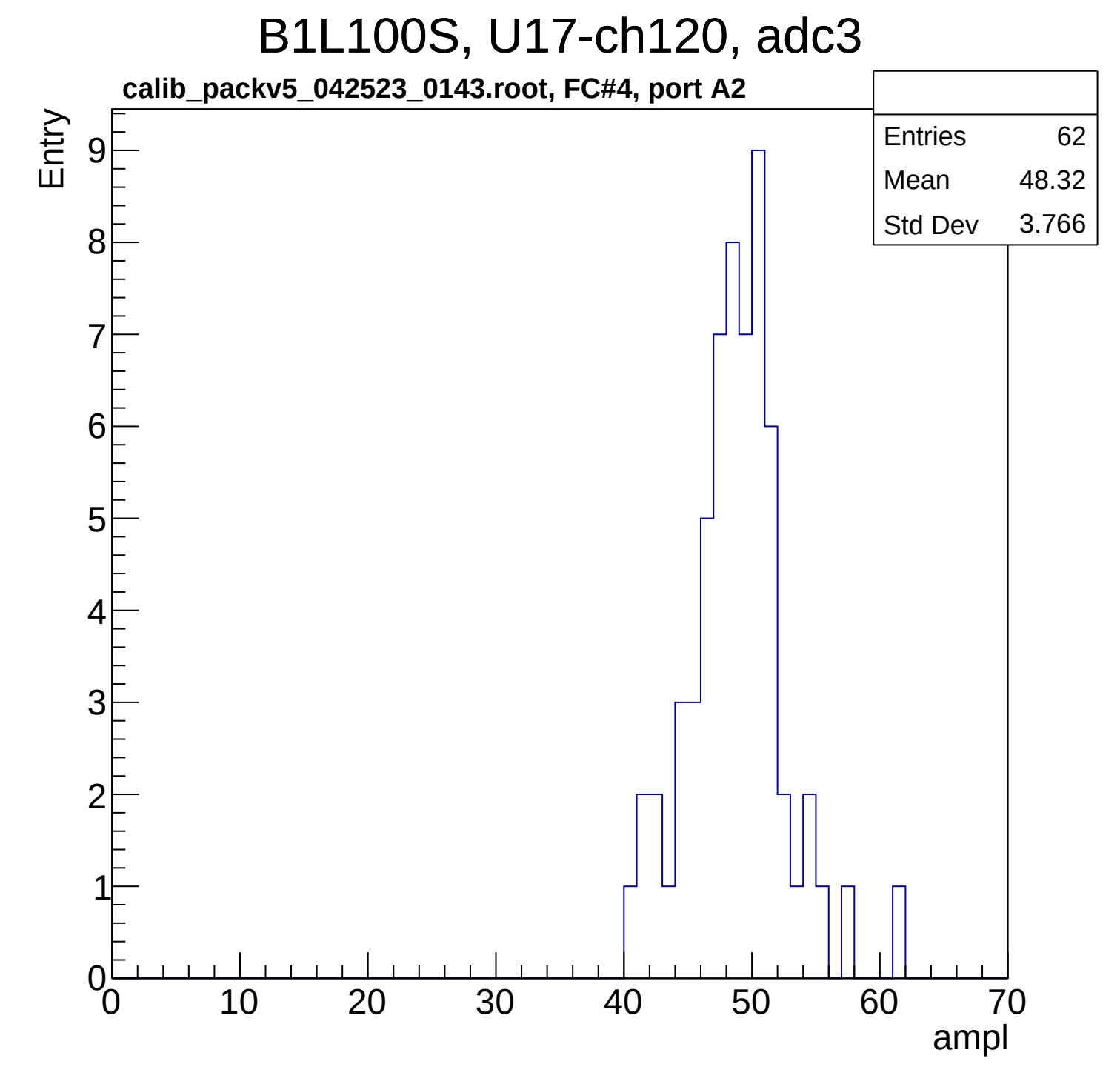
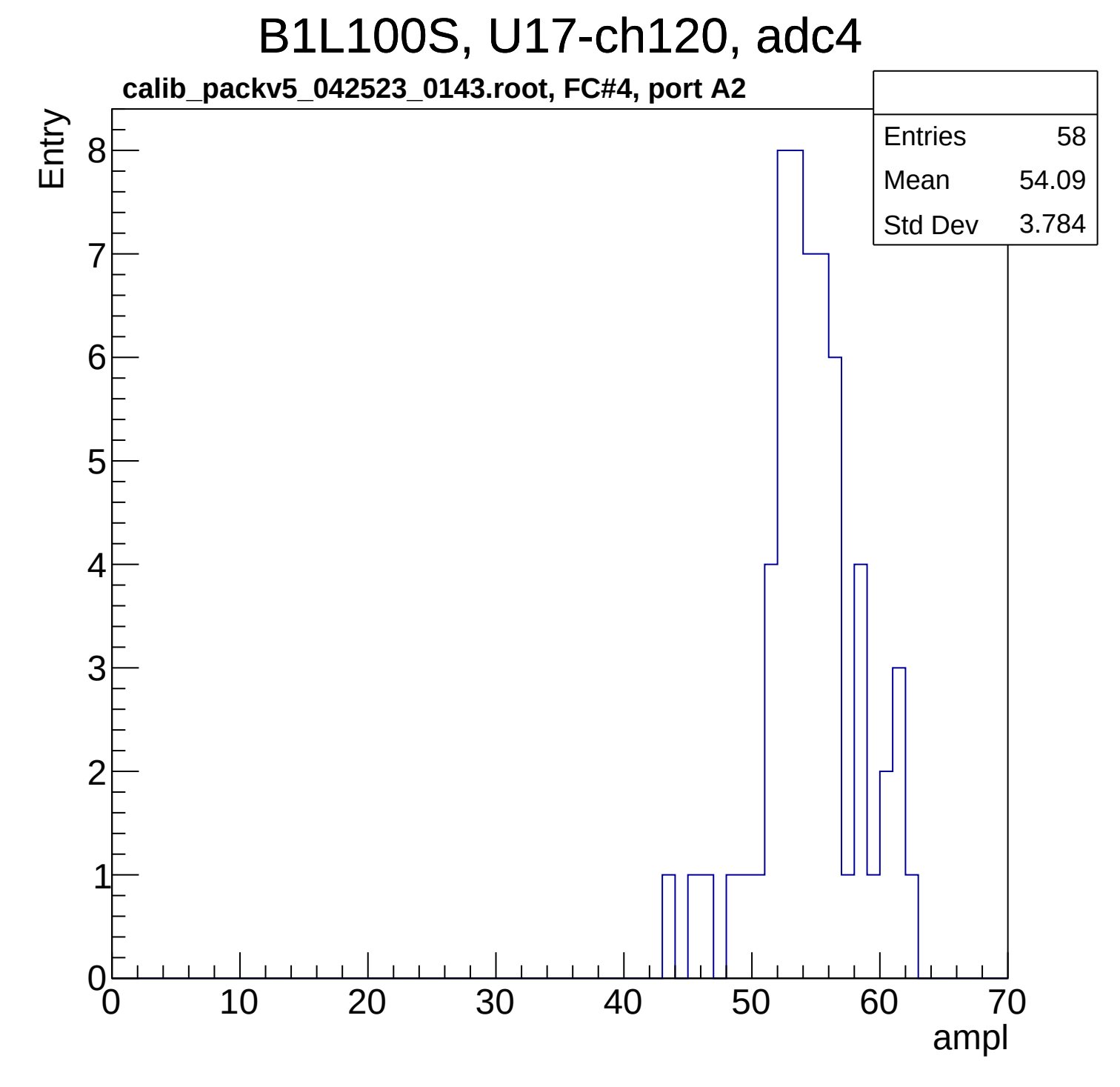
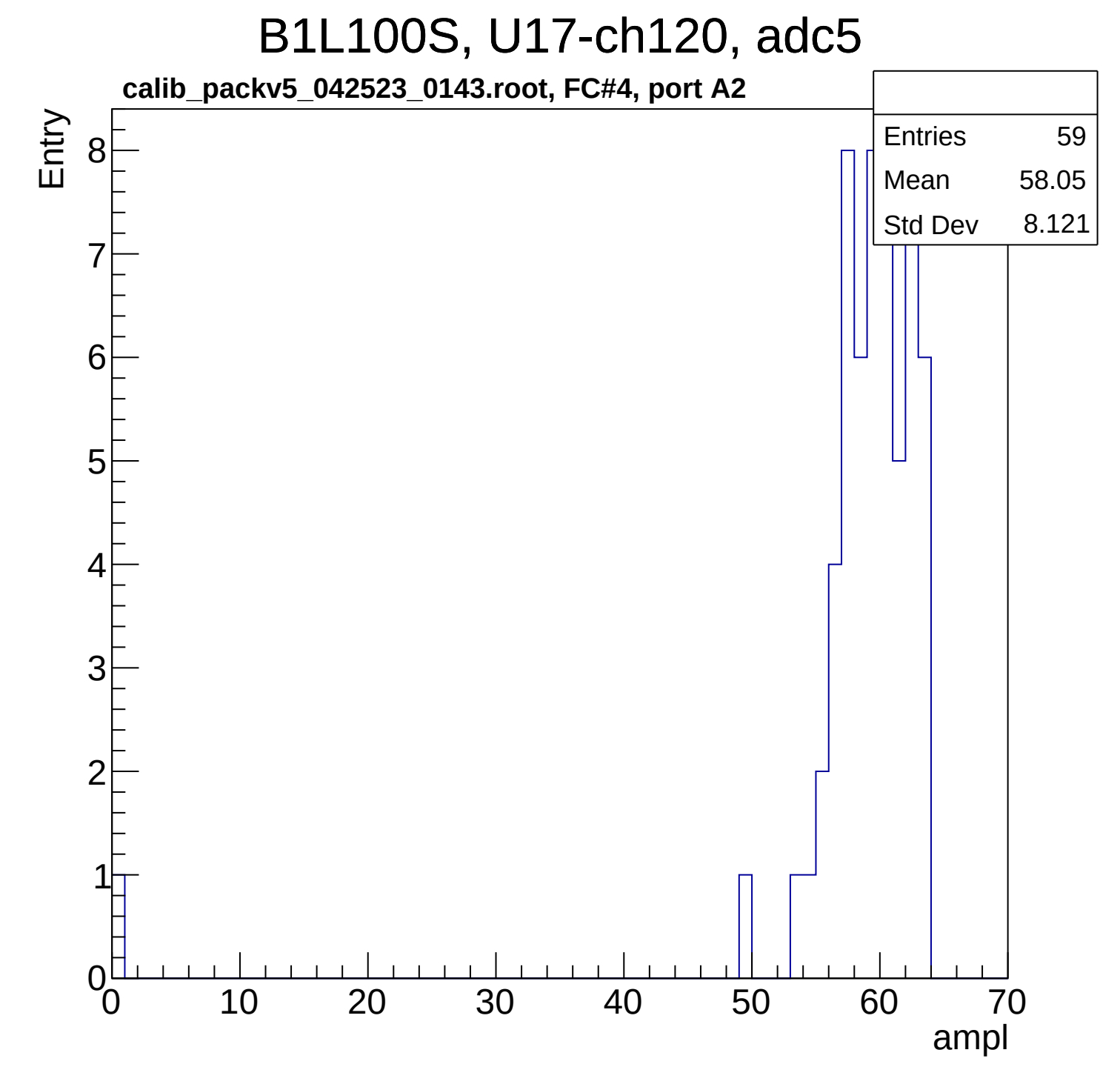
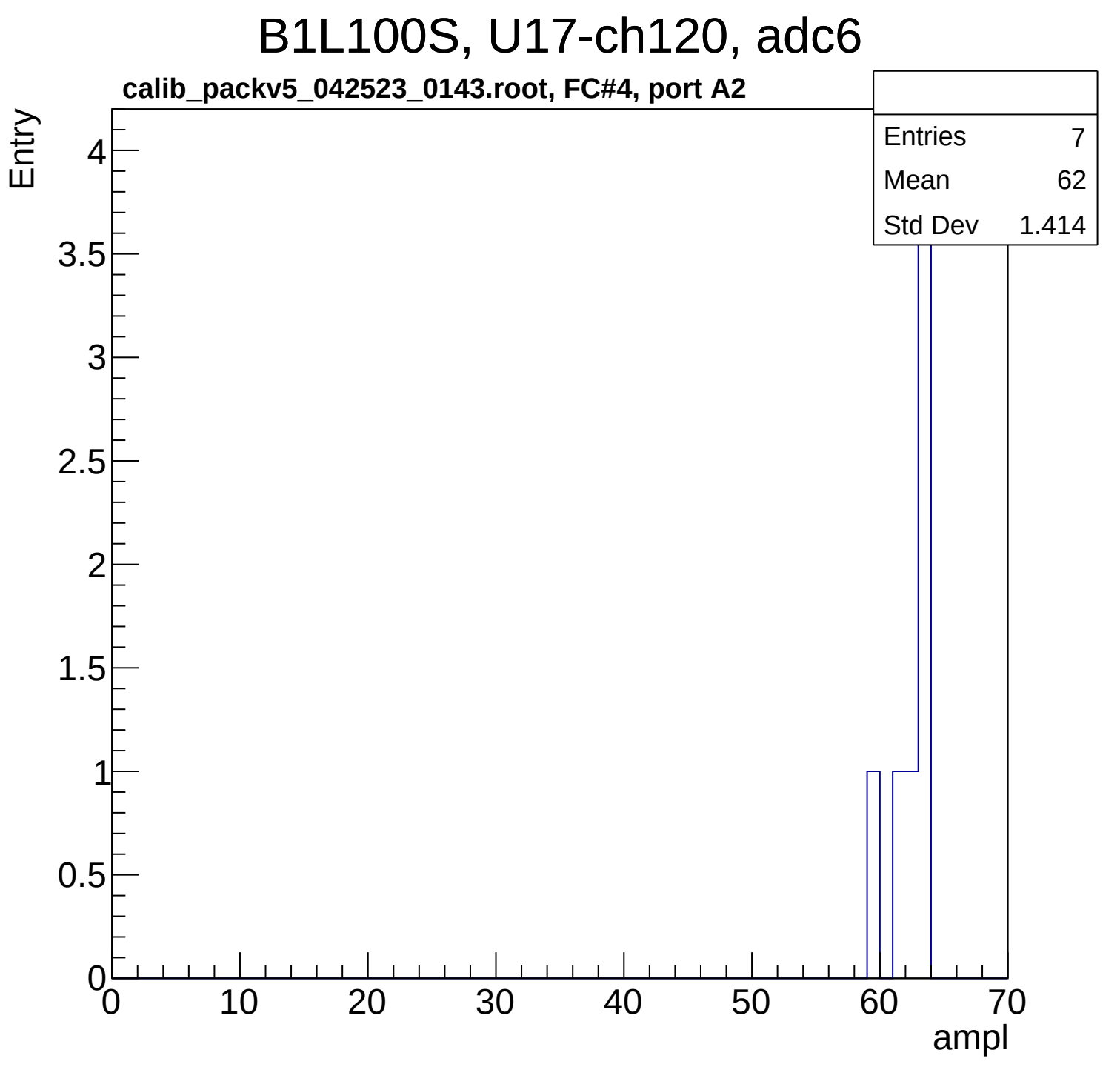
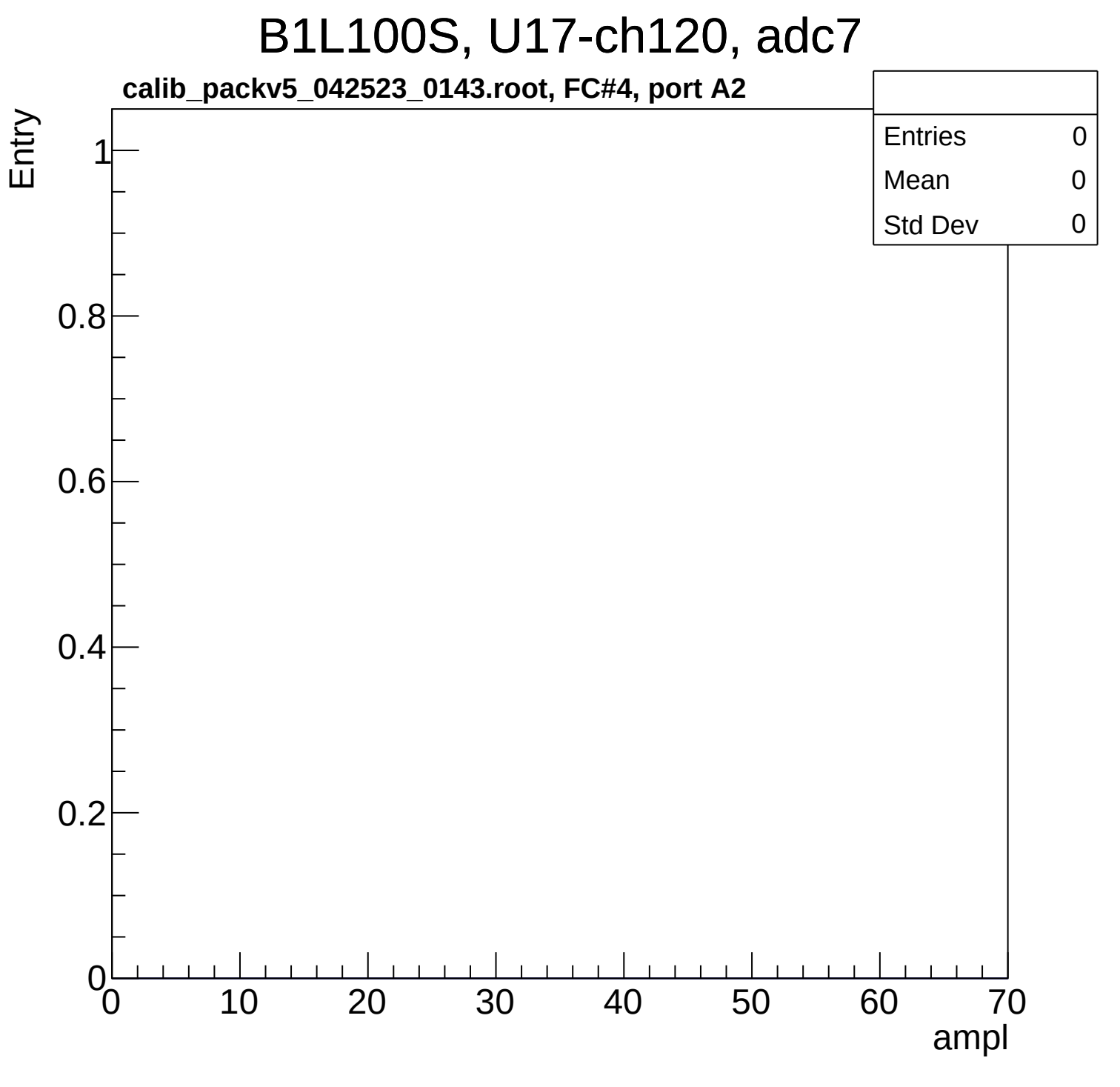

B1L100S, U17-ch120, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 42
Std Dev 3.342
Gaus mean : 43.0641
Gaus Width: 3.1886
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

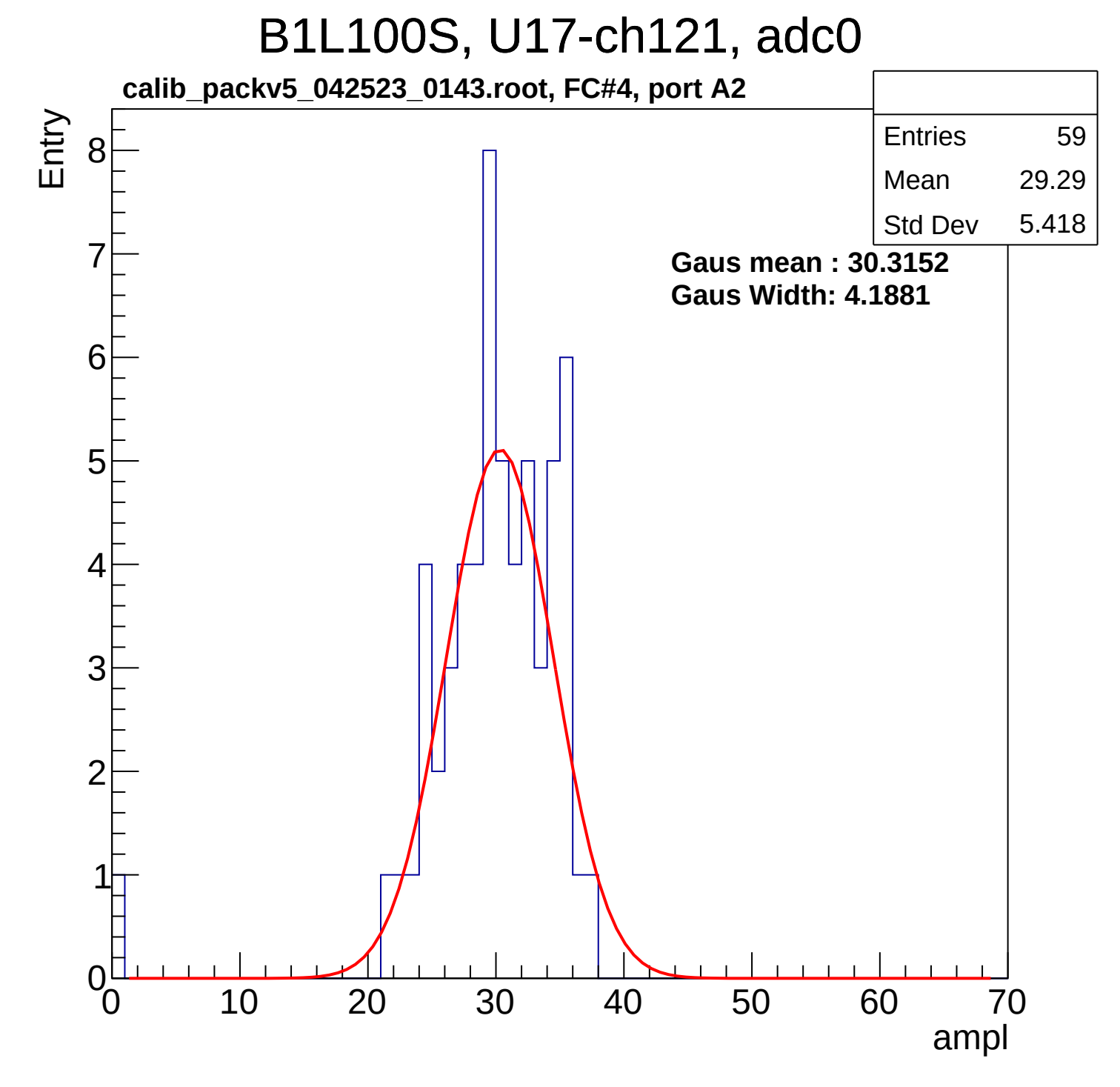

B1L100S, U17-ch120, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 48.32
Std Dev 3.766
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

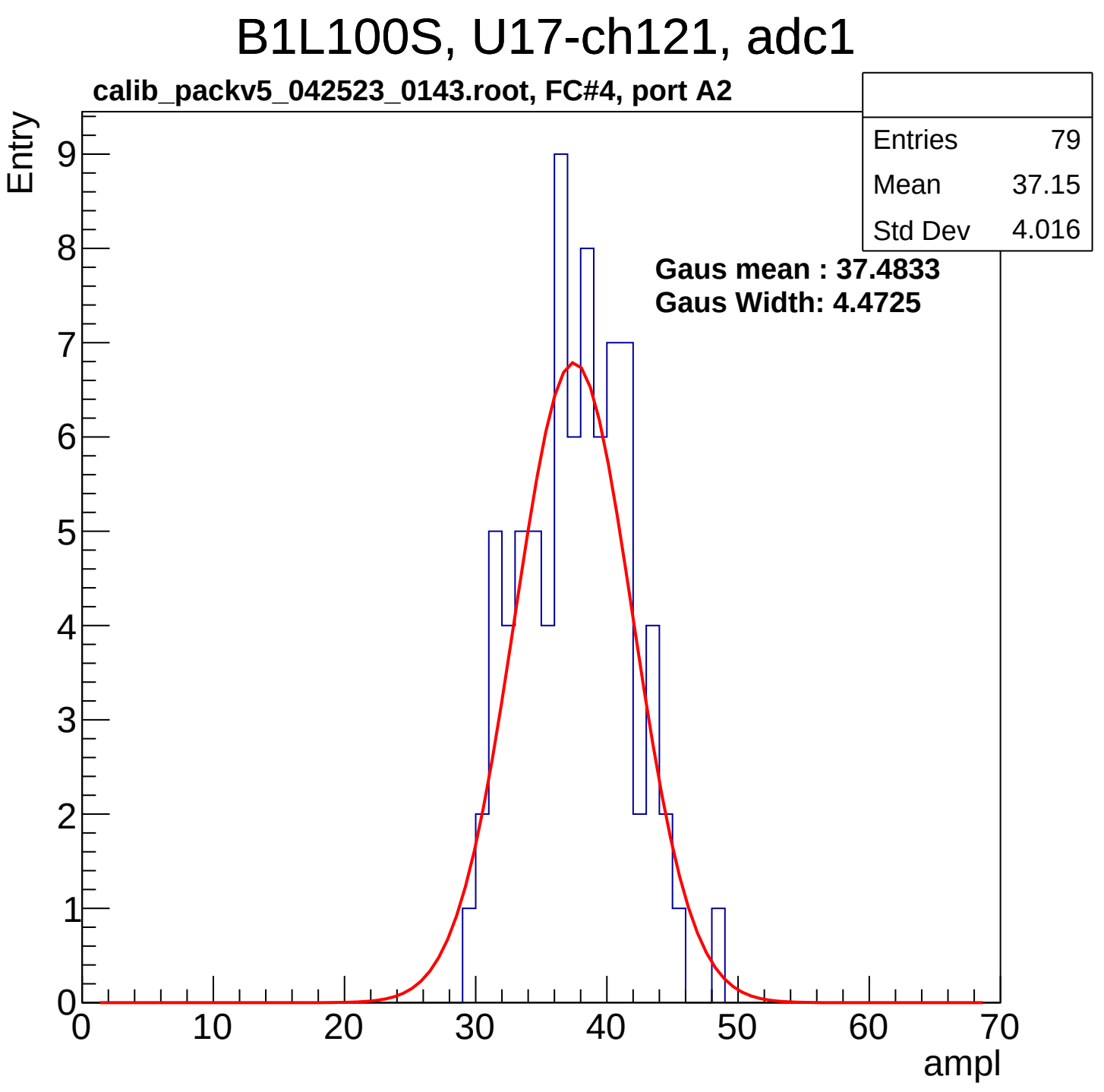

B1L100S, U17-ch120, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 54.09
Std Dev 3.784
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

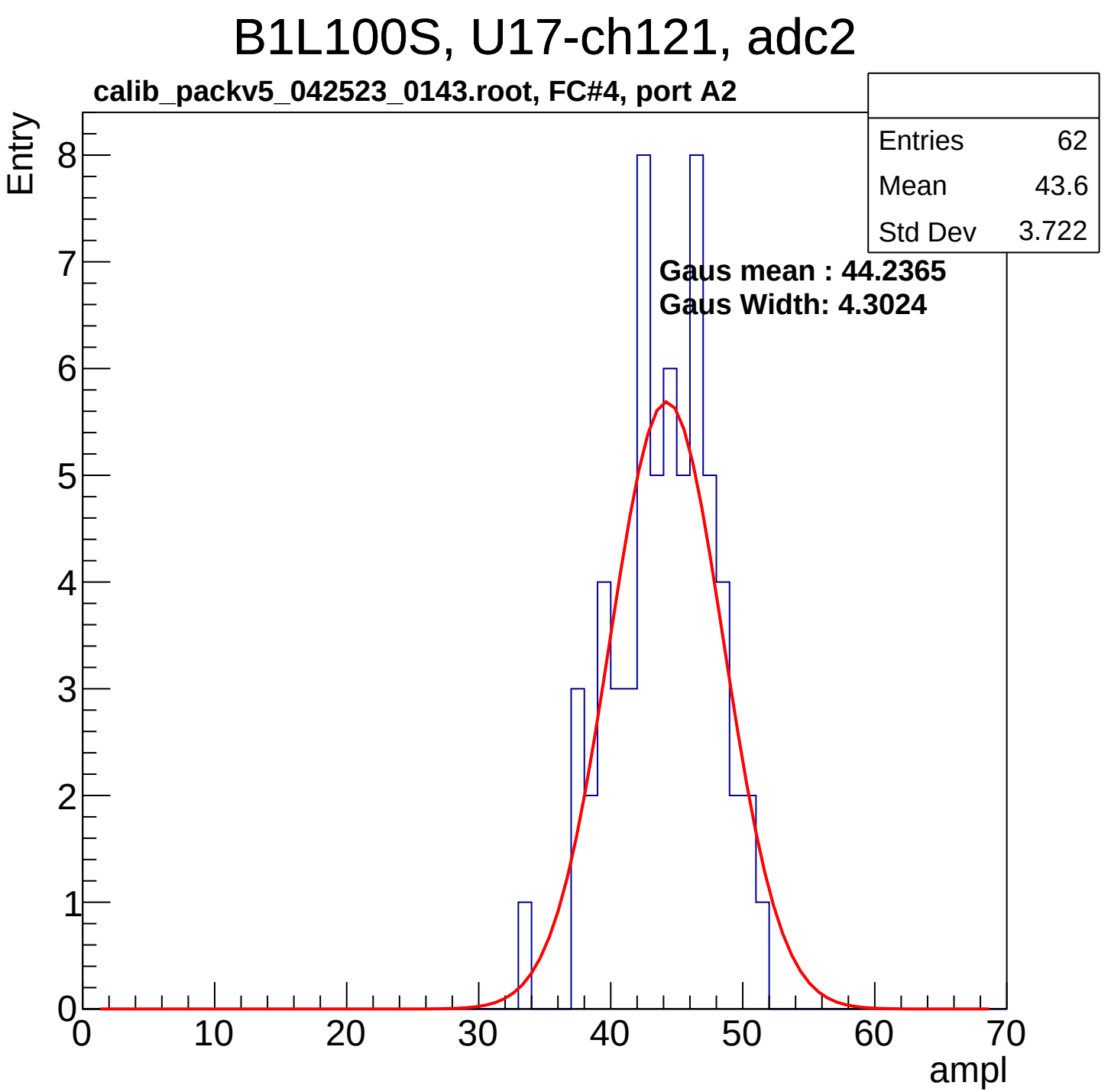

B1L100S, U17-ch120, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 58.05
Std Dev 8.121
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

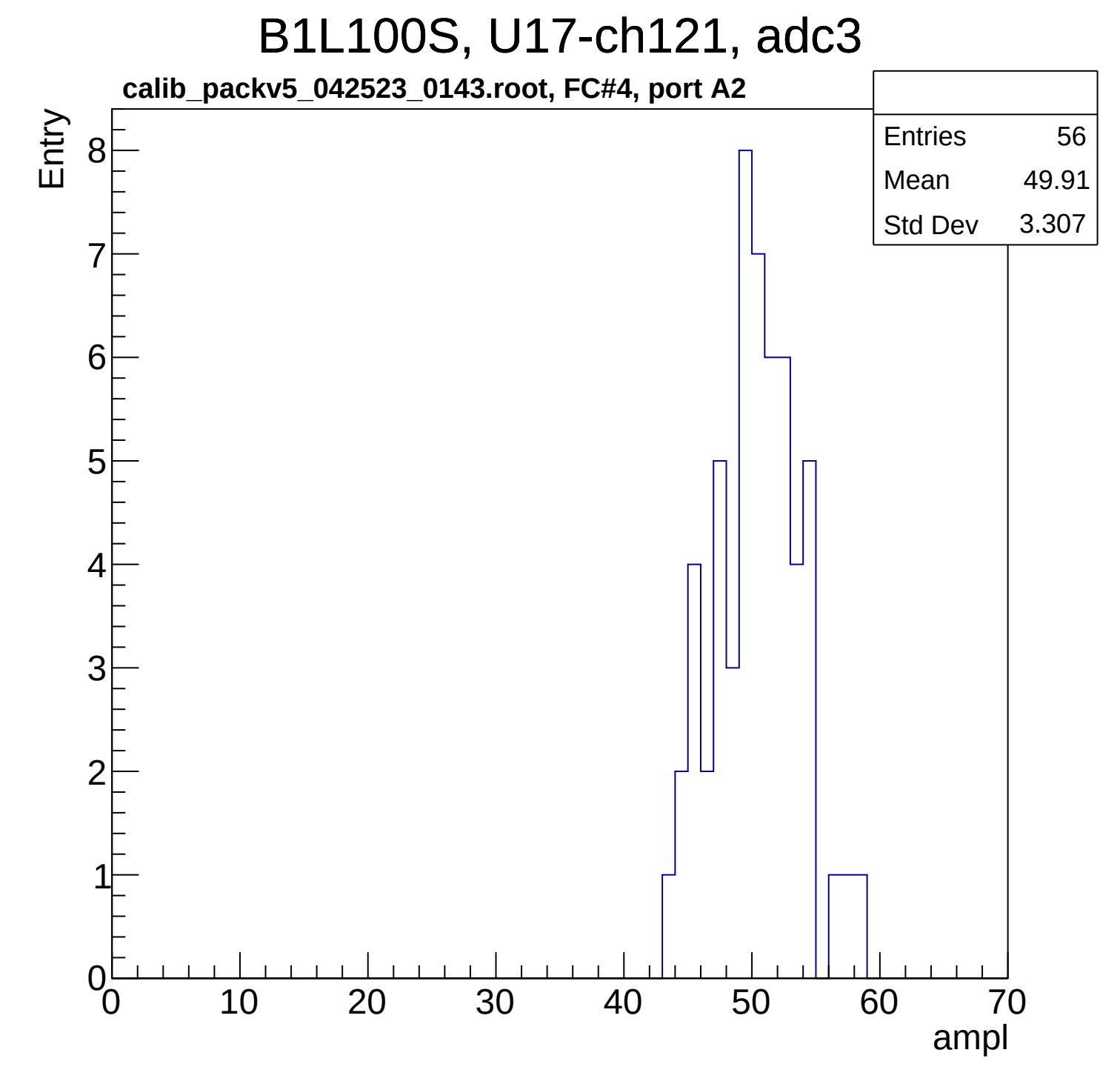

B1L100S, U17-ch120, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 7
Mean 62
Std Dev 1.414
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

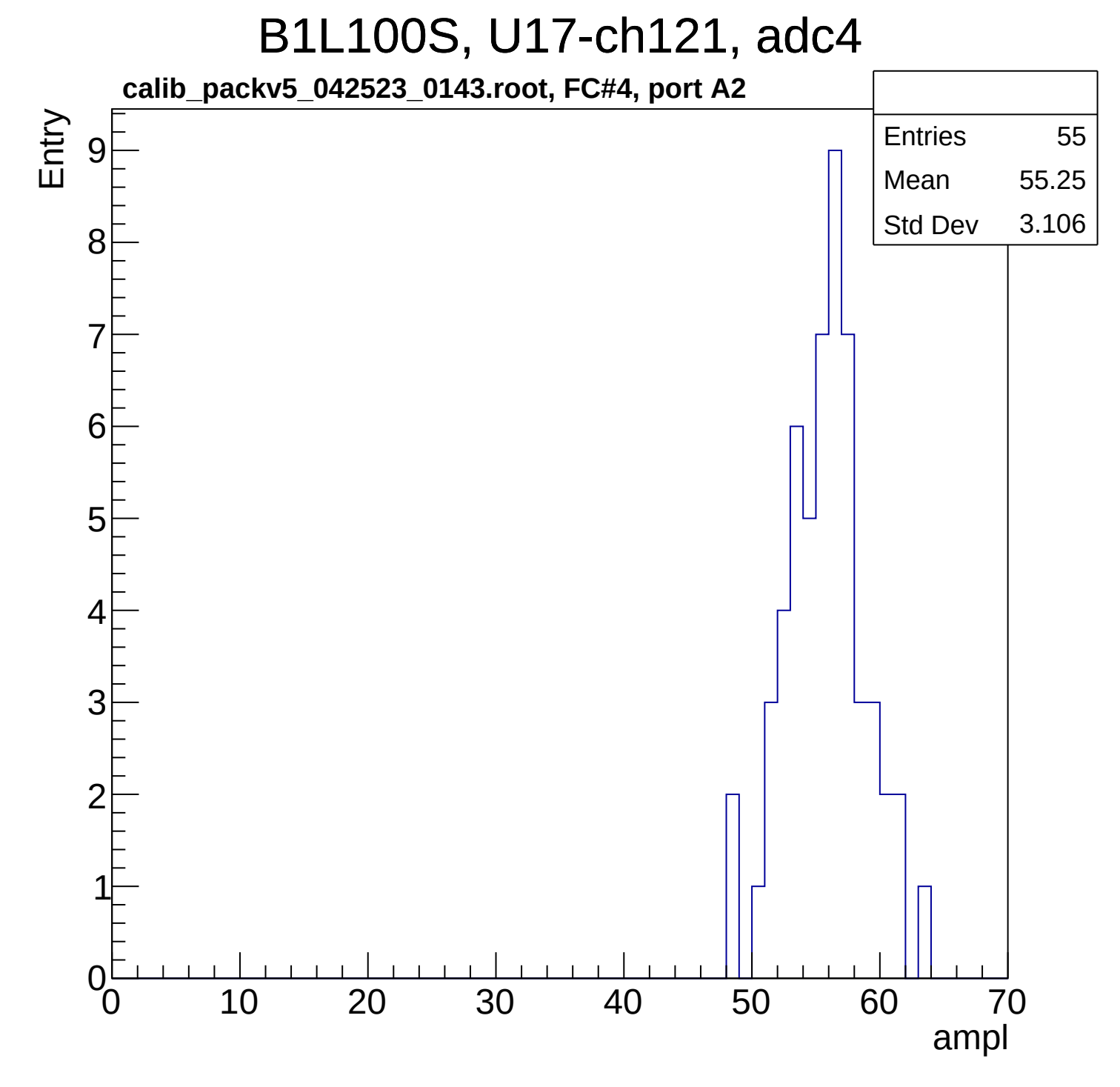

B1L100S, U17-ch120, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch121, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 29.29
Std Dev 5.418
Gaus mean : 30.3152
Gaus Width: 4.1881
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch121, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 79
Mean 37.15
Std Dev 4.016
Gaus mean : 37.4833
Gaus Width: 4.4725
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L100S, U17-ch121, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 43.6
Std Dev 3.722
Gaus mean : 44.2365
Gaus Width: 4.3024
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch121, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 49.91
Std Dev 3.307
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch121, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 55.25
Std Dev 3.106
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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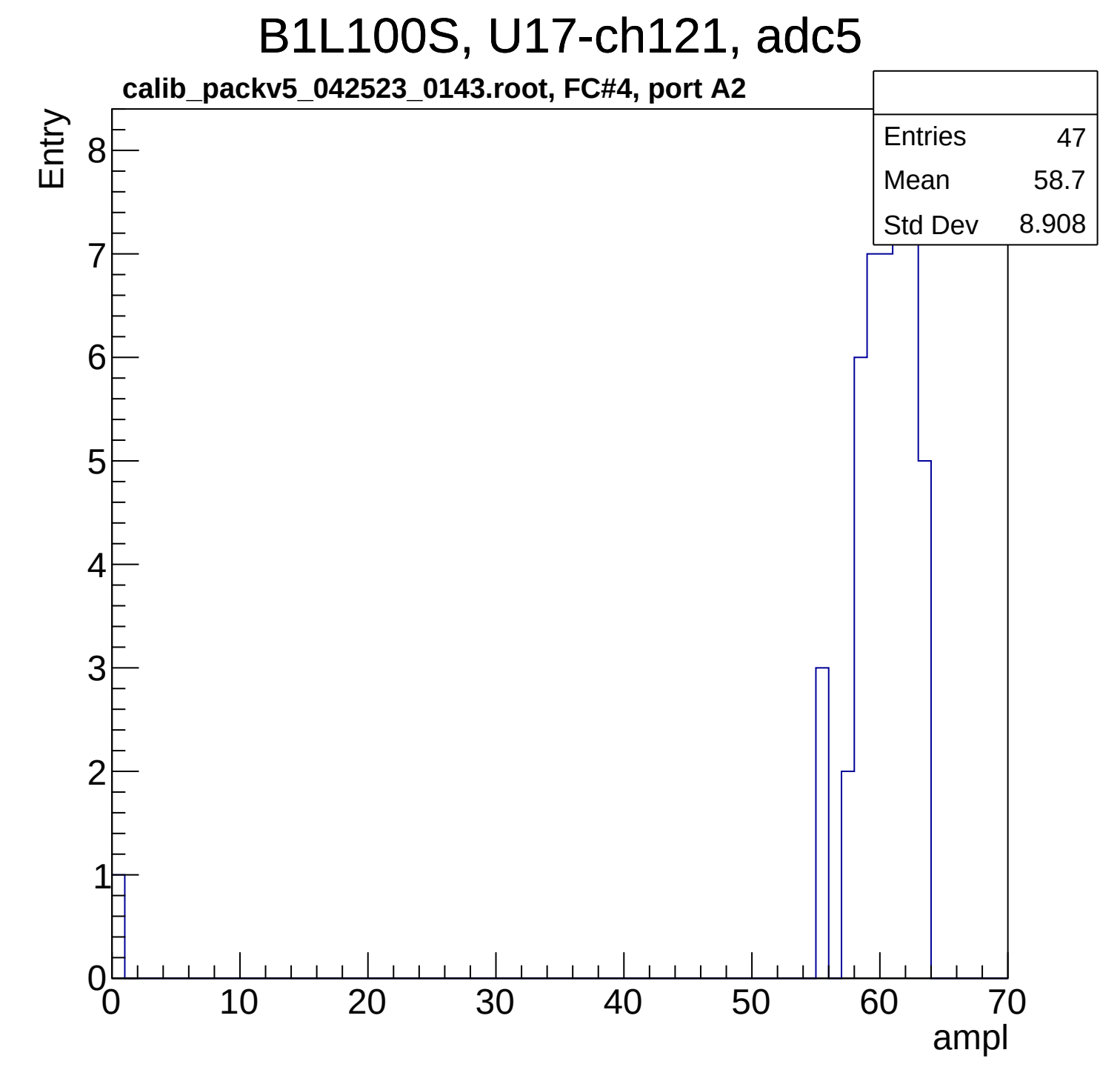
40
50
60
70


B1L100S, U17-ch121, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 47
Mean 58.7
Std Dev 8.908
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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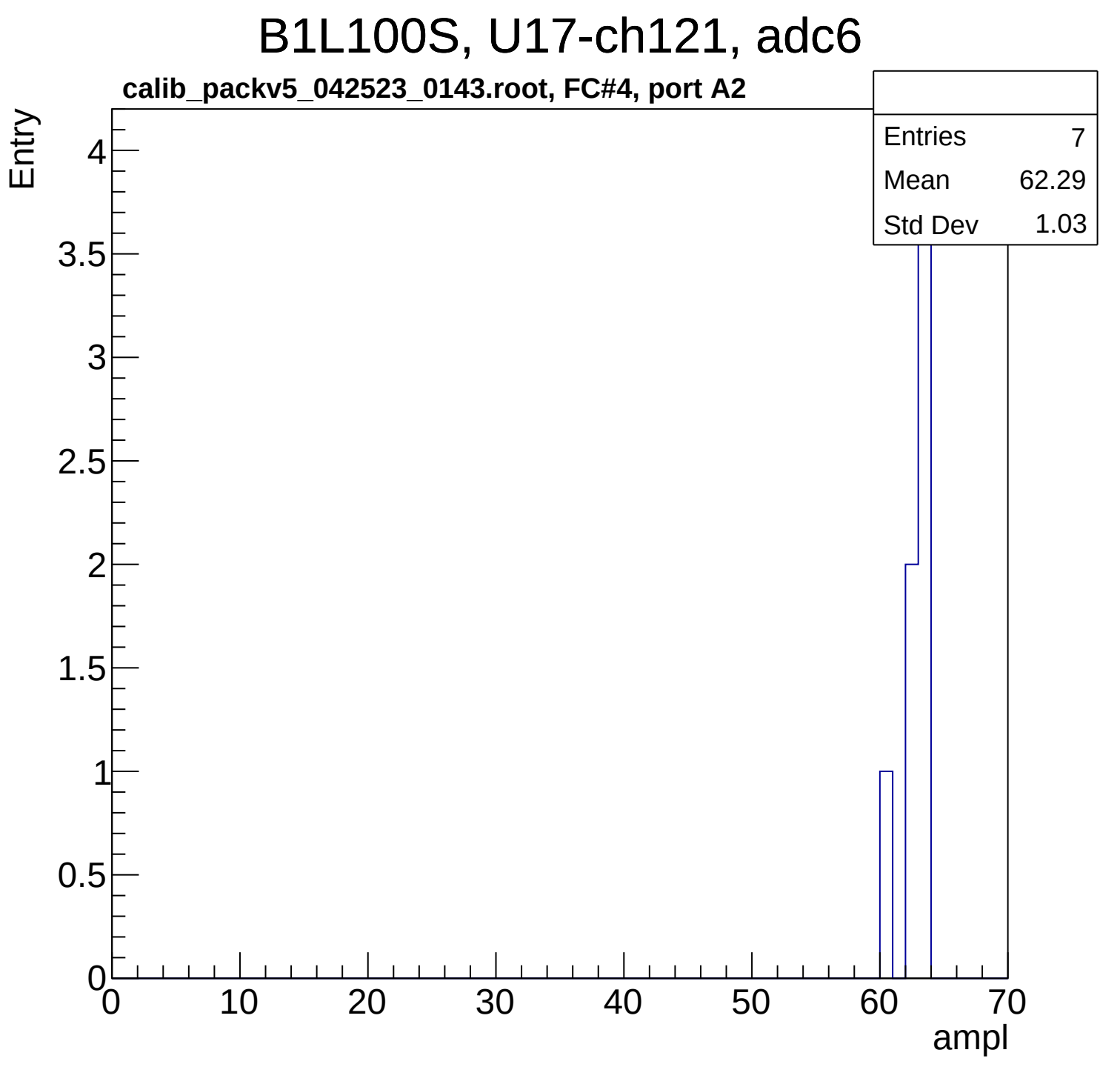
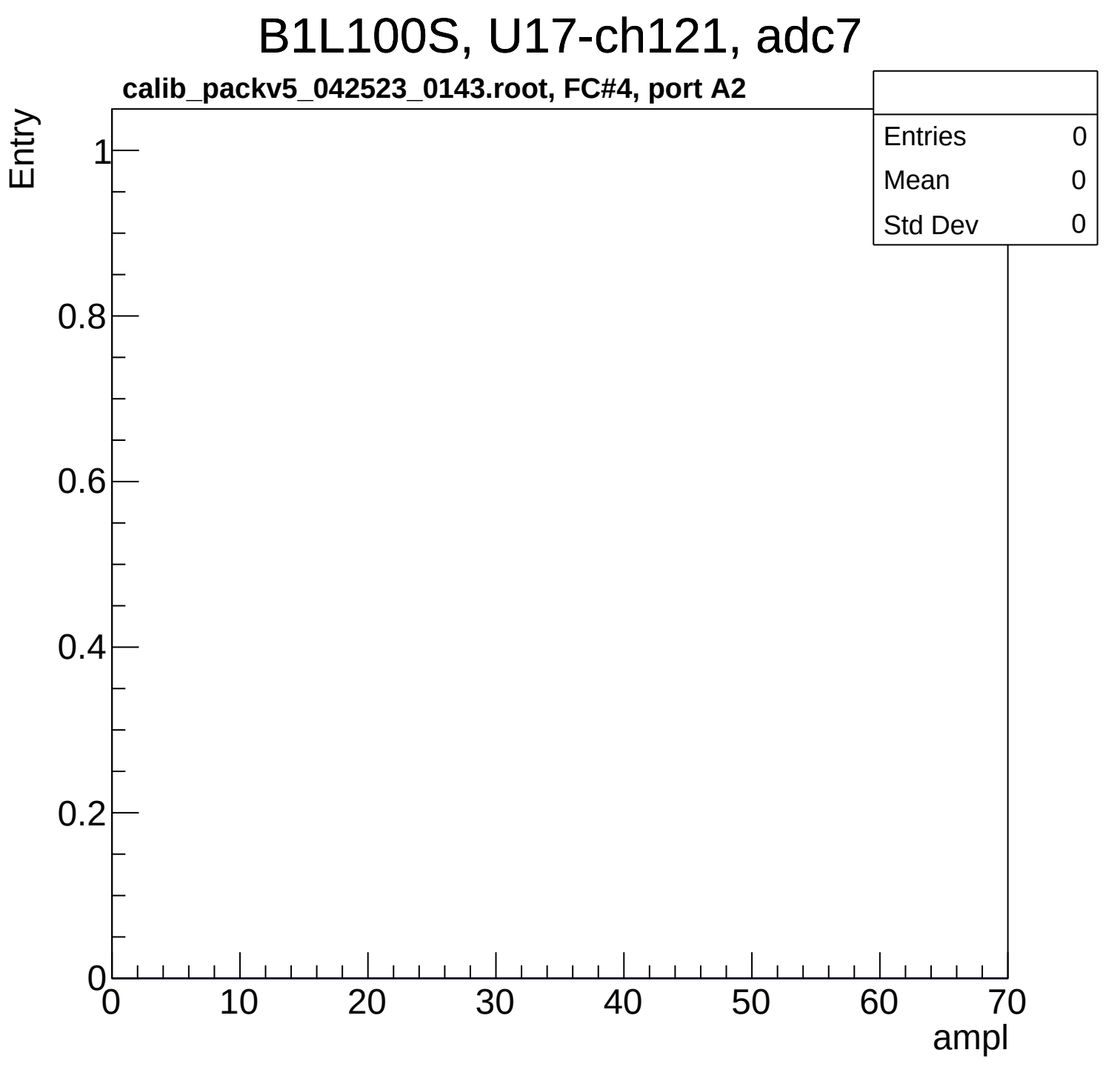
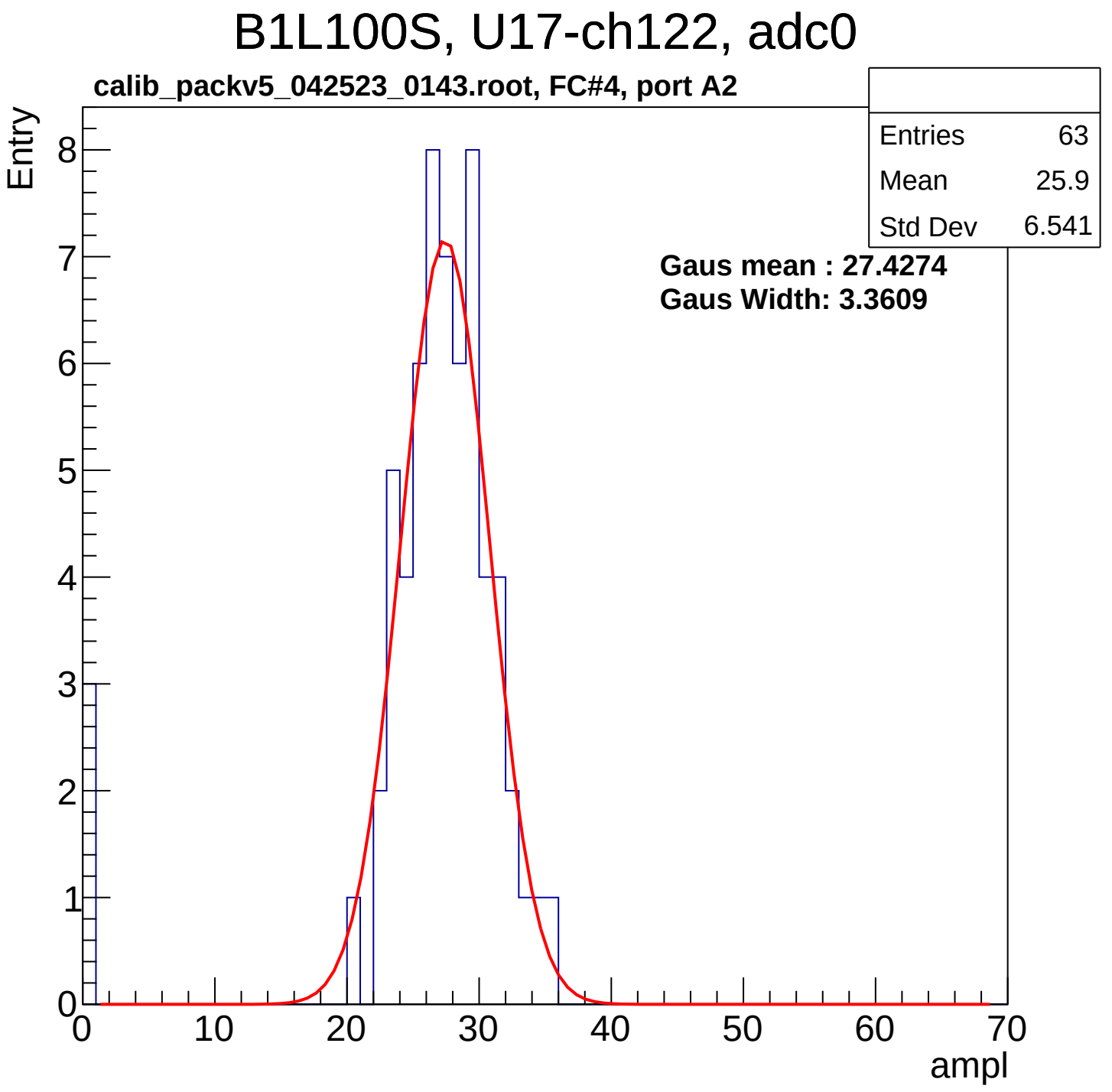
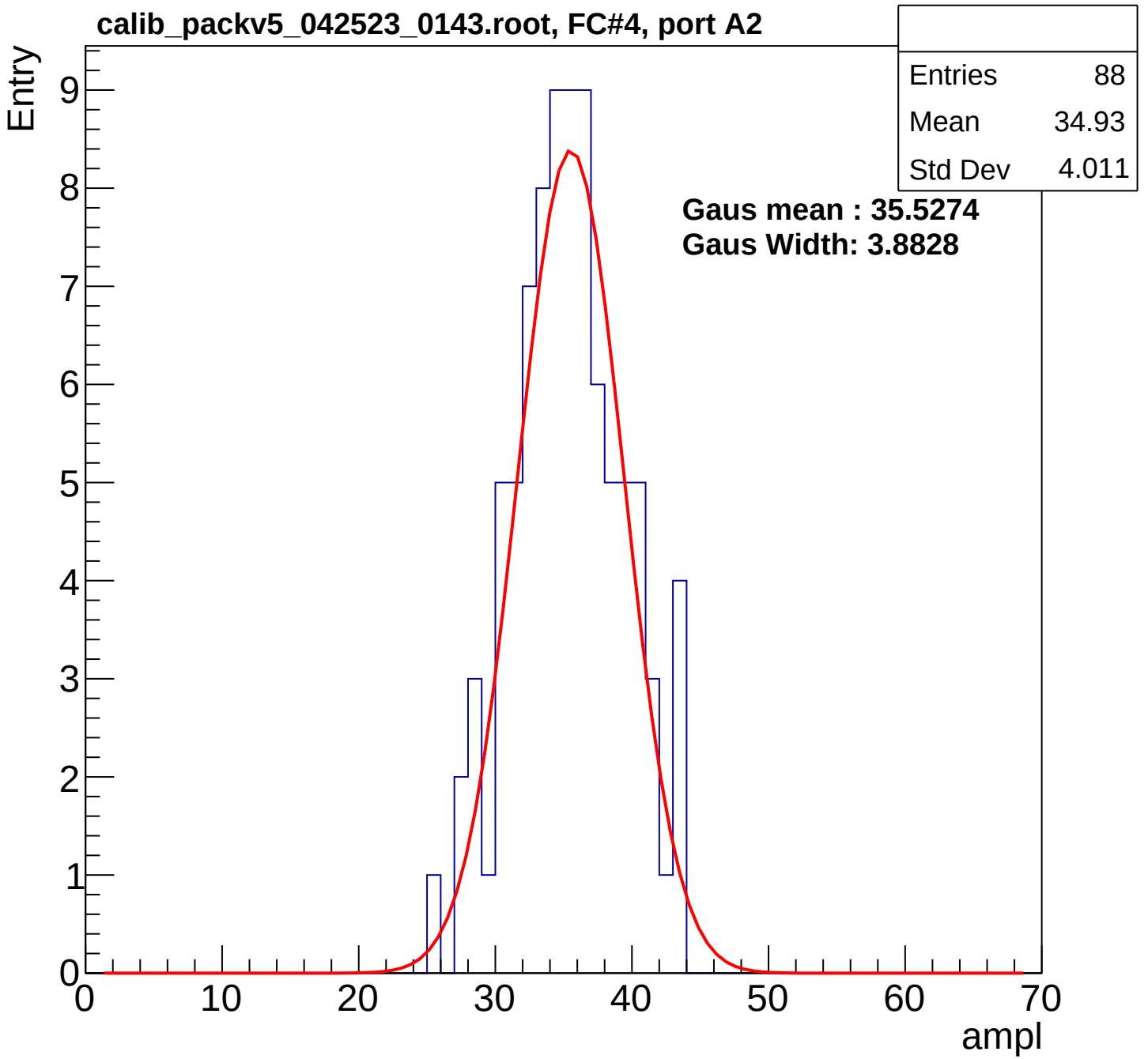
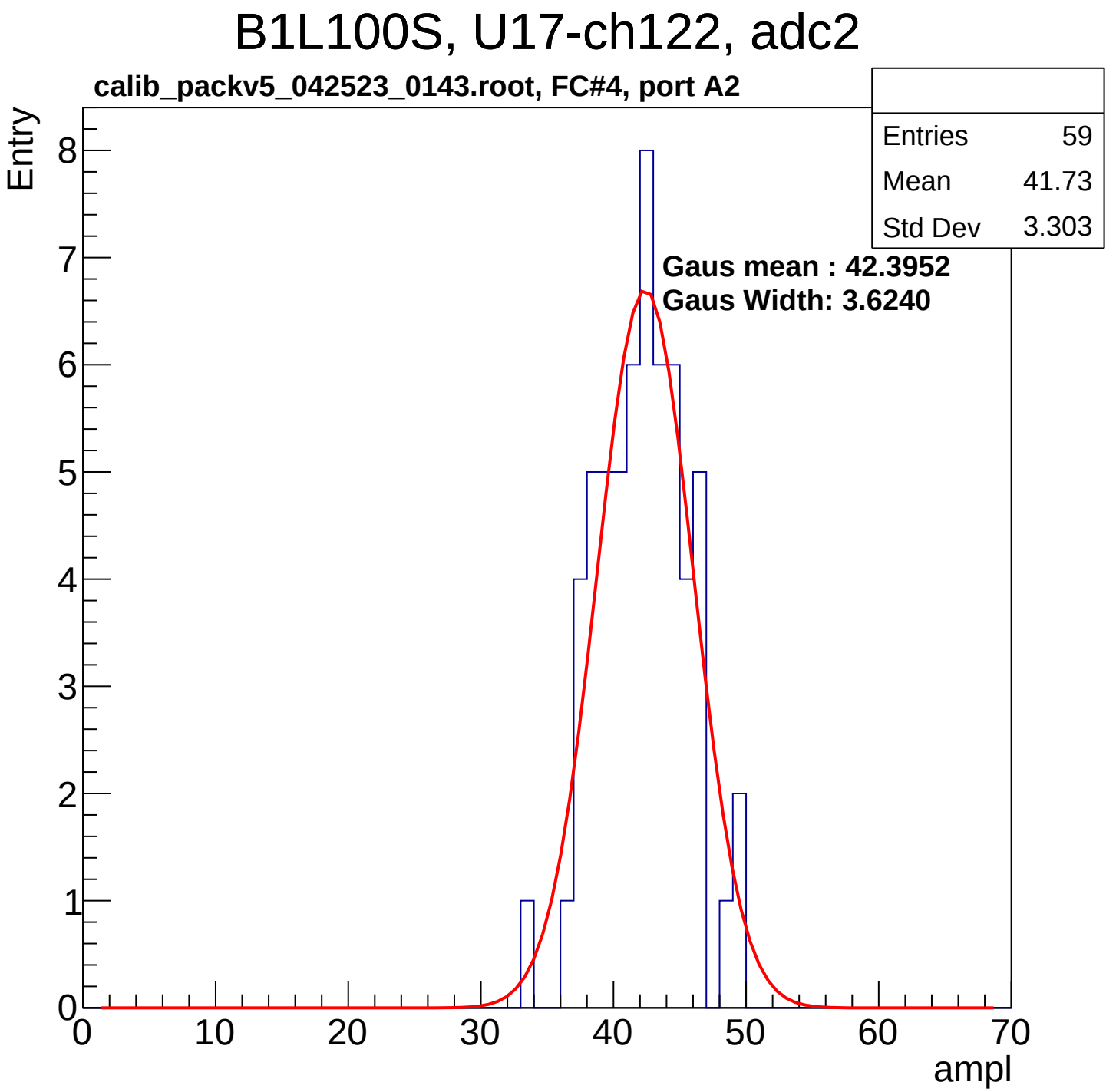
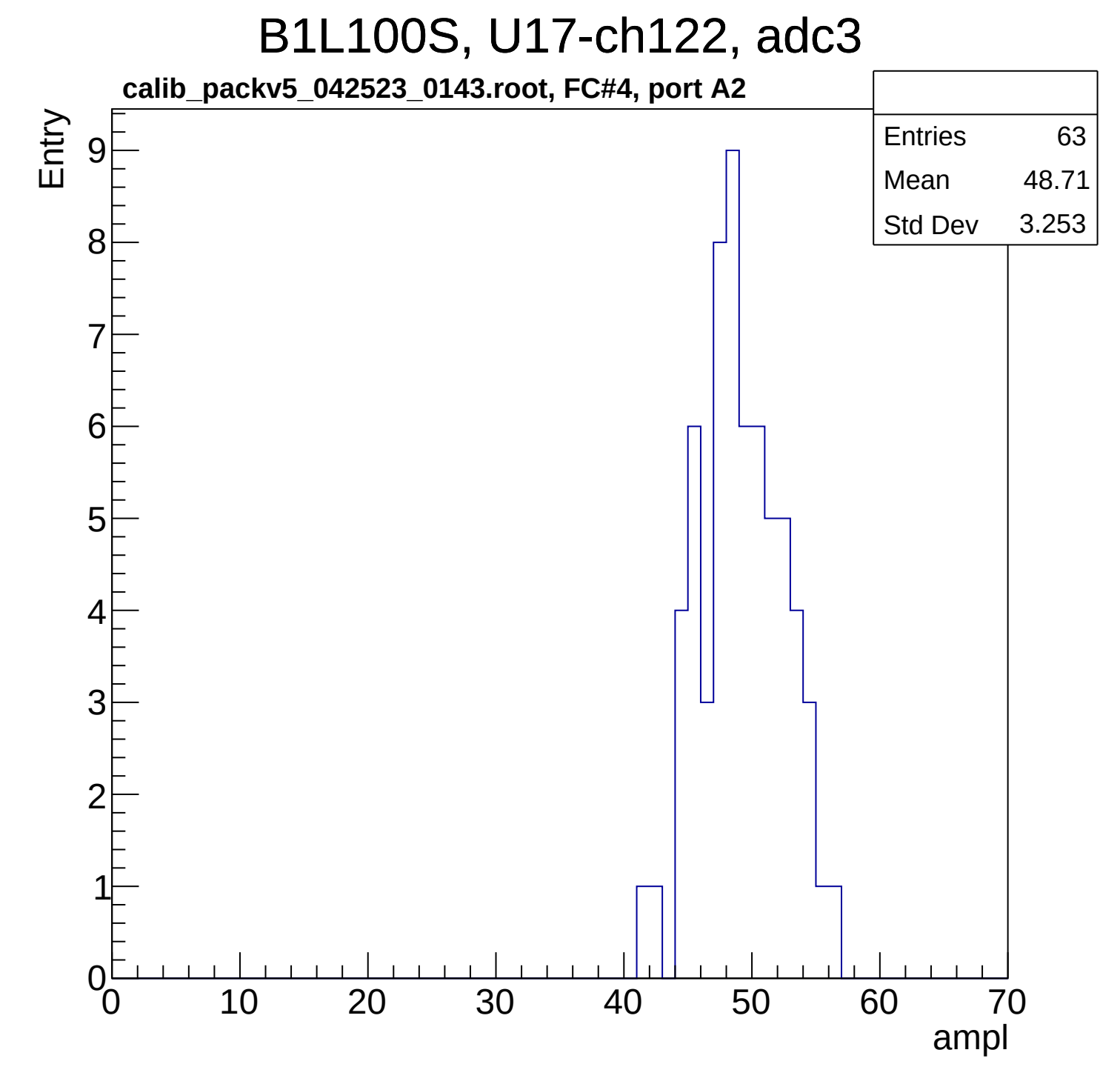

B1L100S, U17-ch121, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 7
Mean 62.29
Std Dev 1.03
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L100S, U17-ch121, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch122, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 25.9
Std Dev 6.541
Gaus mean : 27.4274
Gaus Width: 3.3609
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch122, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 88
Mean 34.93
Std Dev 4.011
Gaus mean : 35.5274
Gaus Width: 3.8828
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch122, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 41.73
Std Dev 3.303
Gaus mean : 42.3952
Gaus Width: 3.6240
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch122, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 48.71
Std Dev 3.253
Entry
ampl
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3
4
5
6
7
8
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0
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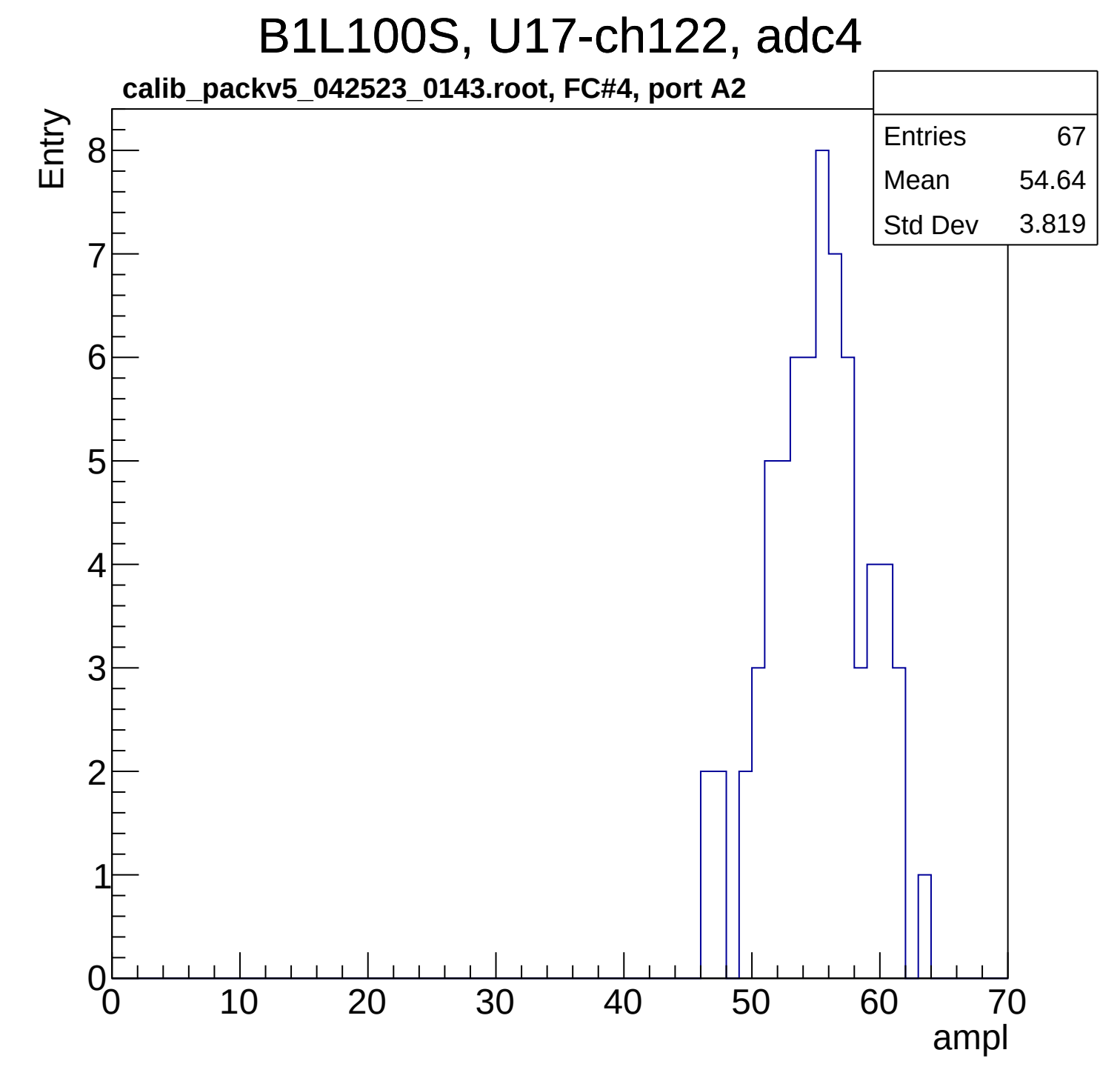
50
60
70


B1L100S, U17-ch122, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 54.64
Std Dev 3.819
Entry
ampl
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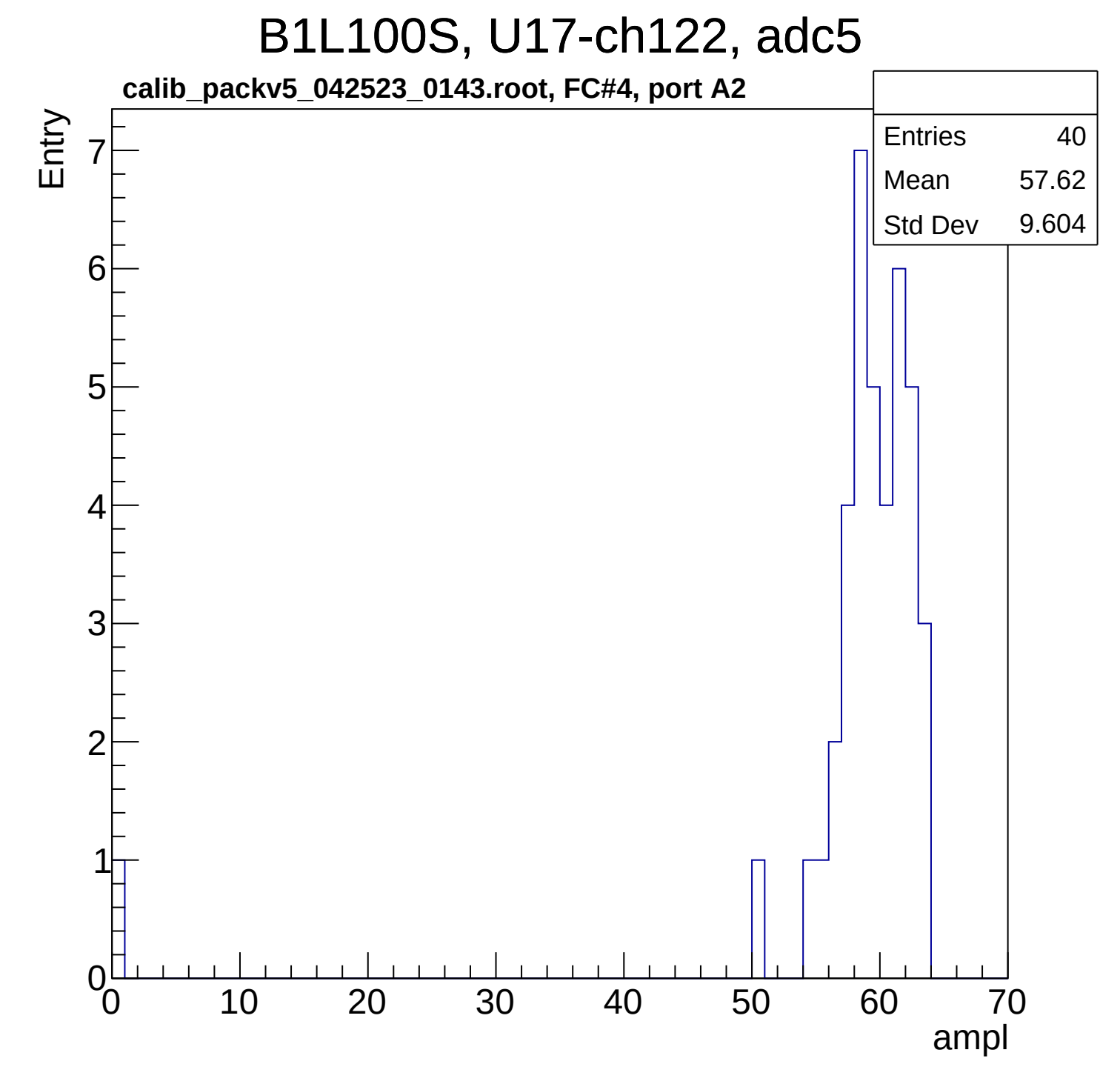
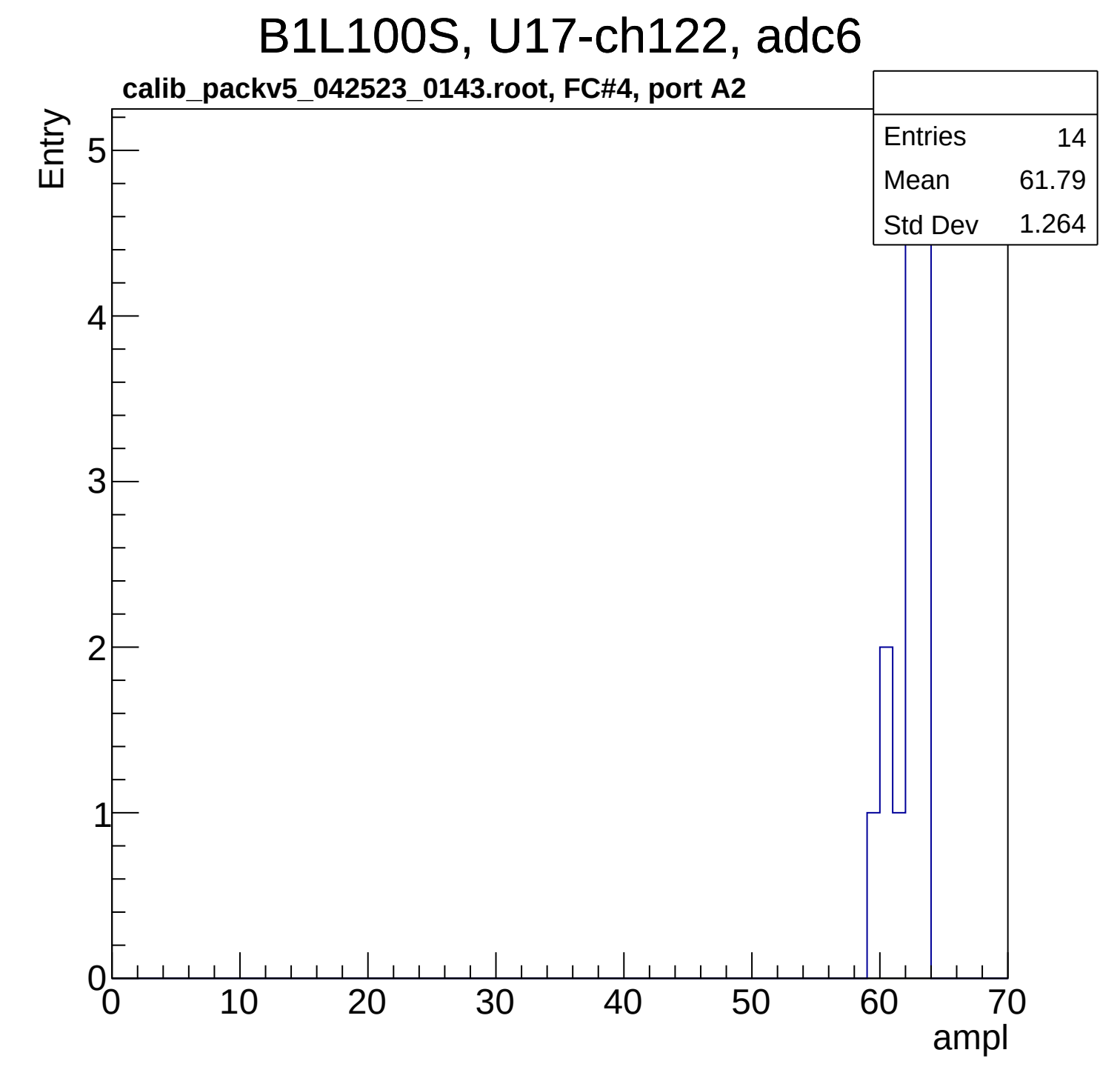
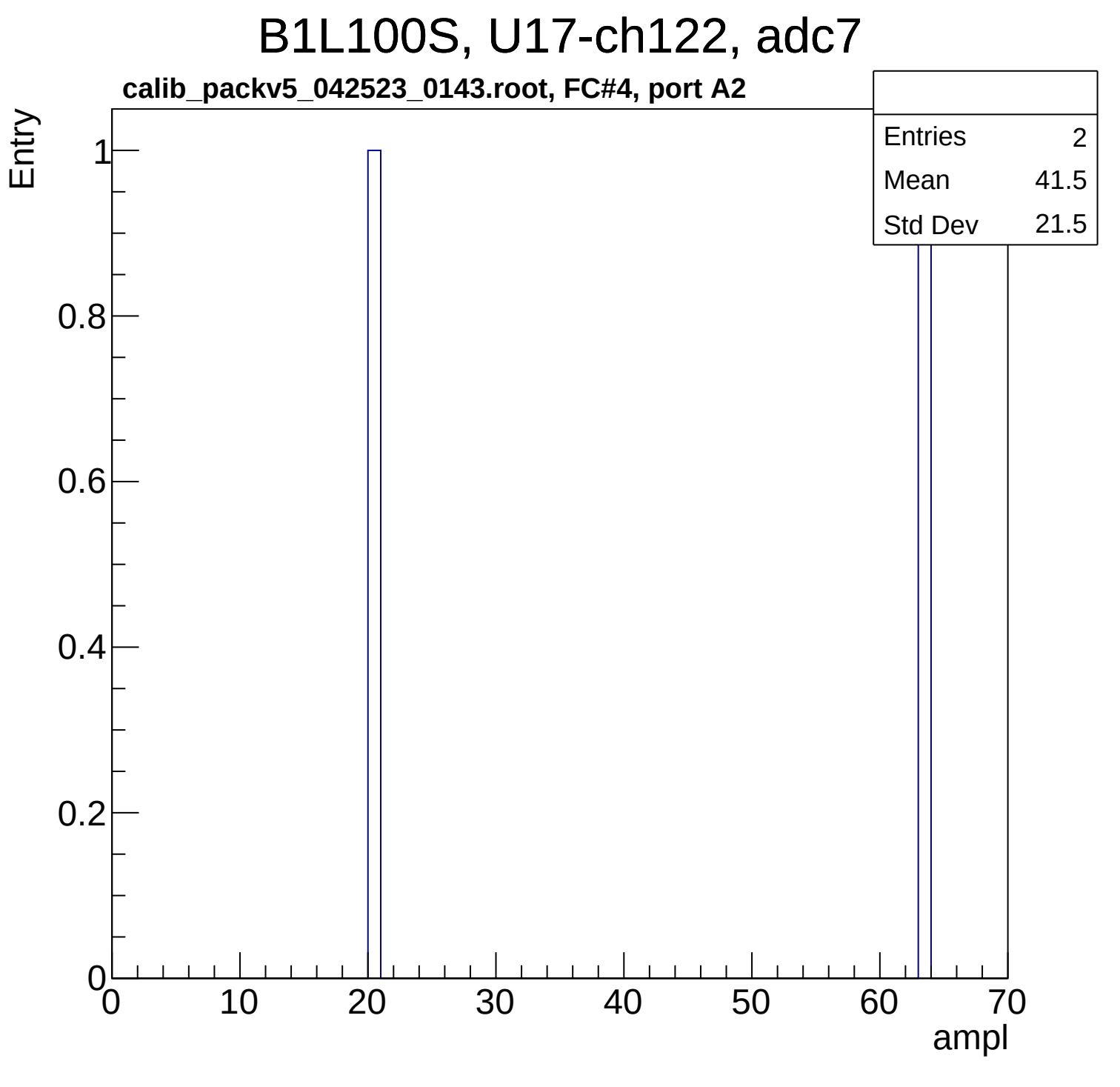
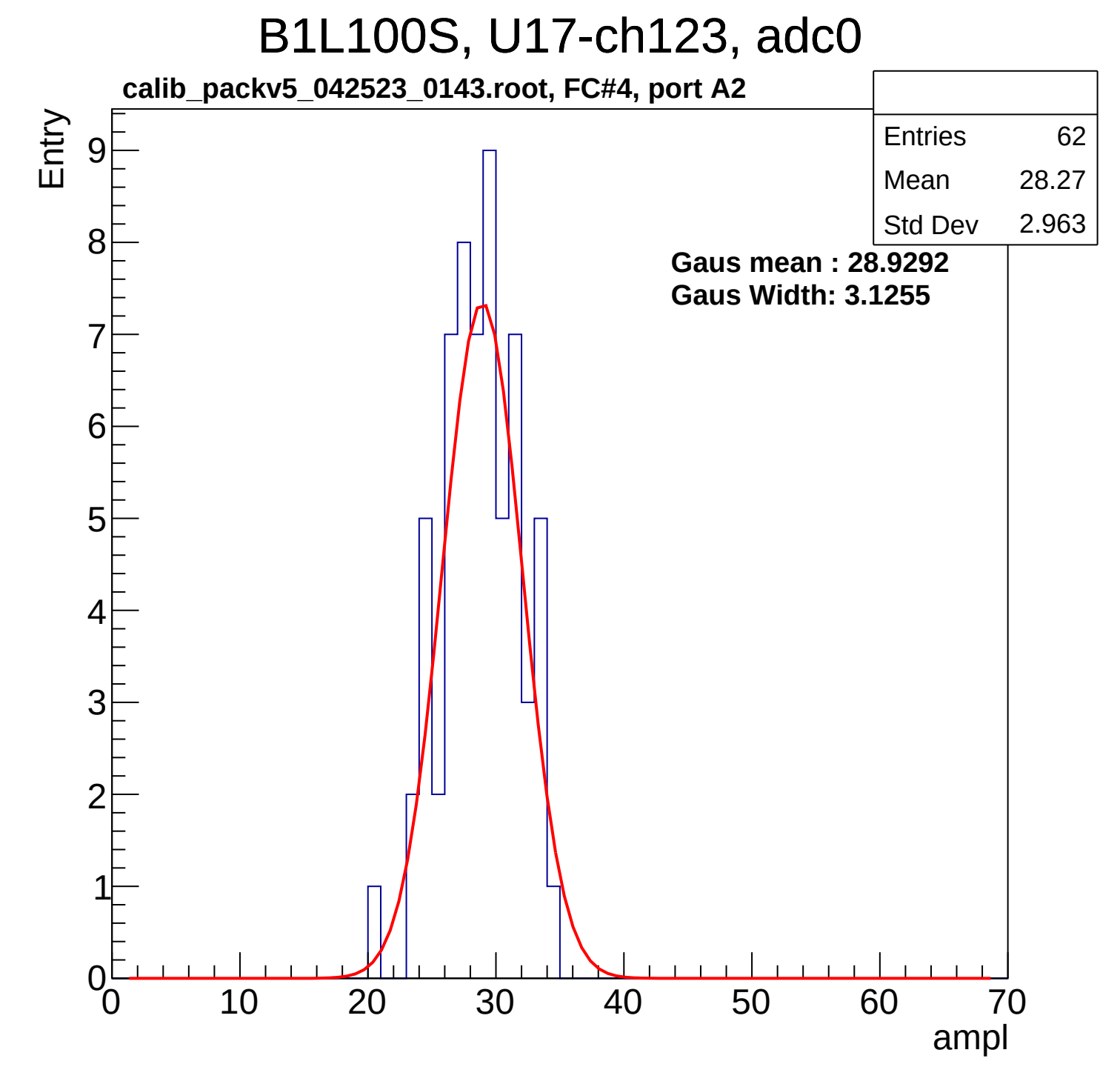
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch122, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 40
Mean 57.62
Std Dev 9.604
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U17-ch122, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 14
Mean 61.79
Std Dev 1.264
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L100S, U17-ch122, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 41.5
Std Dev 21.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch123, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 28.27
Std Dev 2.963
Gaus mean : 28.9292
Gaus Width: 3.1255
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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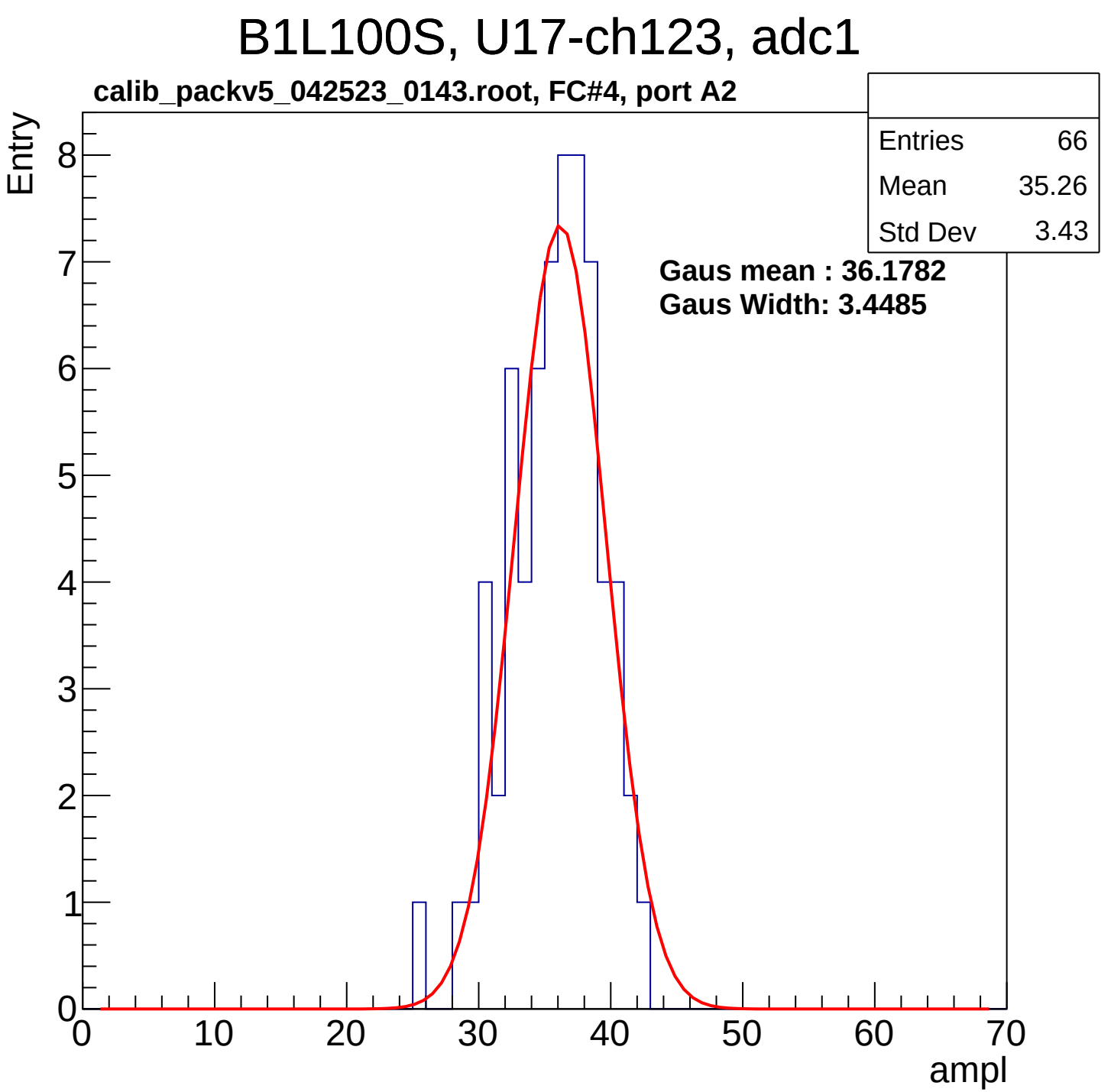
B1L100S, U17-ch123, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 35.26
Std Dev 3.43
Gaus mean : 36.1782
Gaus Width: 3.4485
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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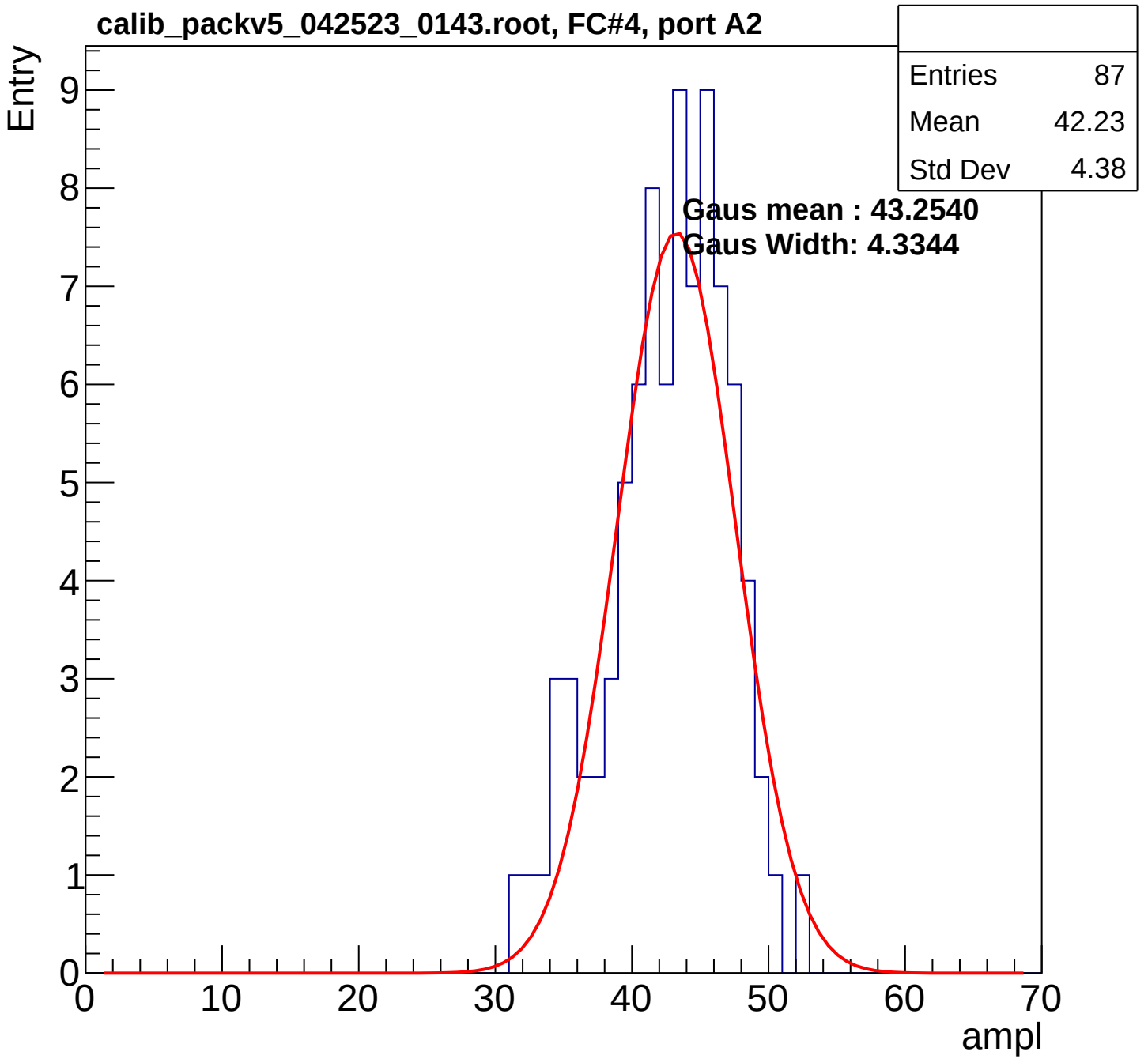
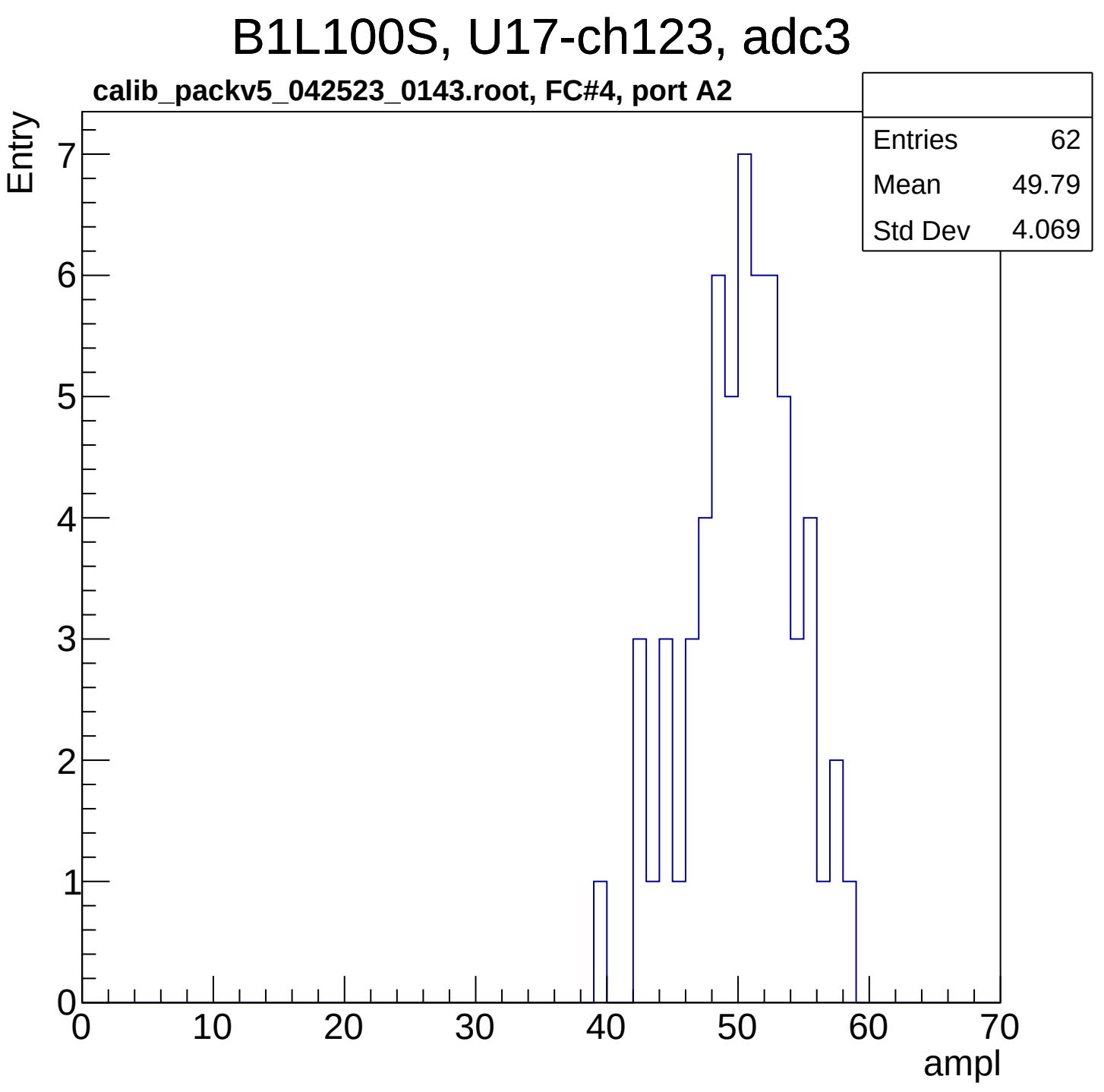

B1L100S, U17-ch123, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 87
Mean 42.23
Std Dev 4.38
Gaus mean : 43.2540
Gaus Width: 4.3344
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch123, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 49.79
Std Dev 4.069
Entry
ampl
0
1
2
3
4
5
6
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0
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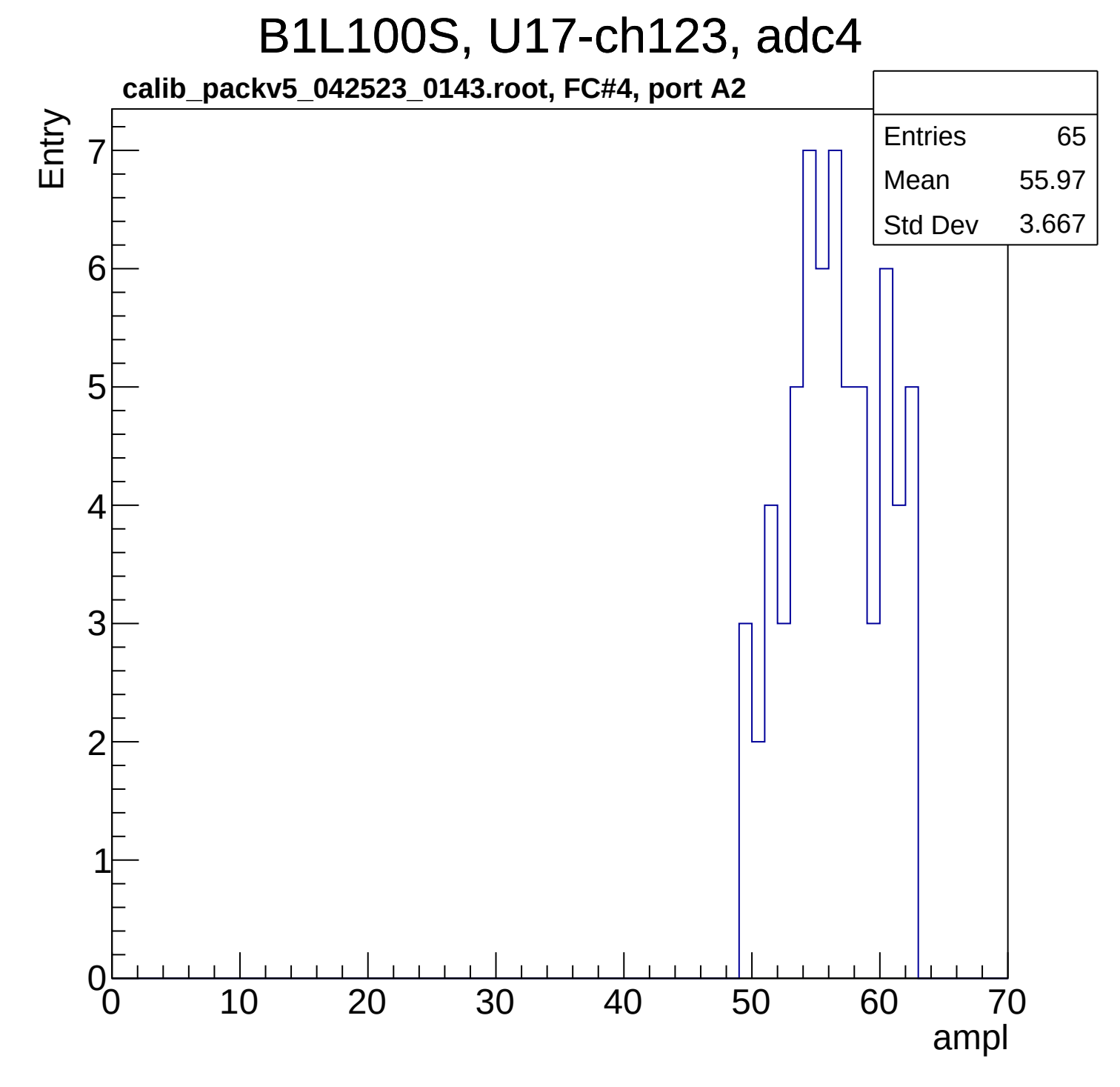
B1L100S, U17-ch123, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 55.97
Std Dev 3.667
Entry
ampl
0
1
2
3
4
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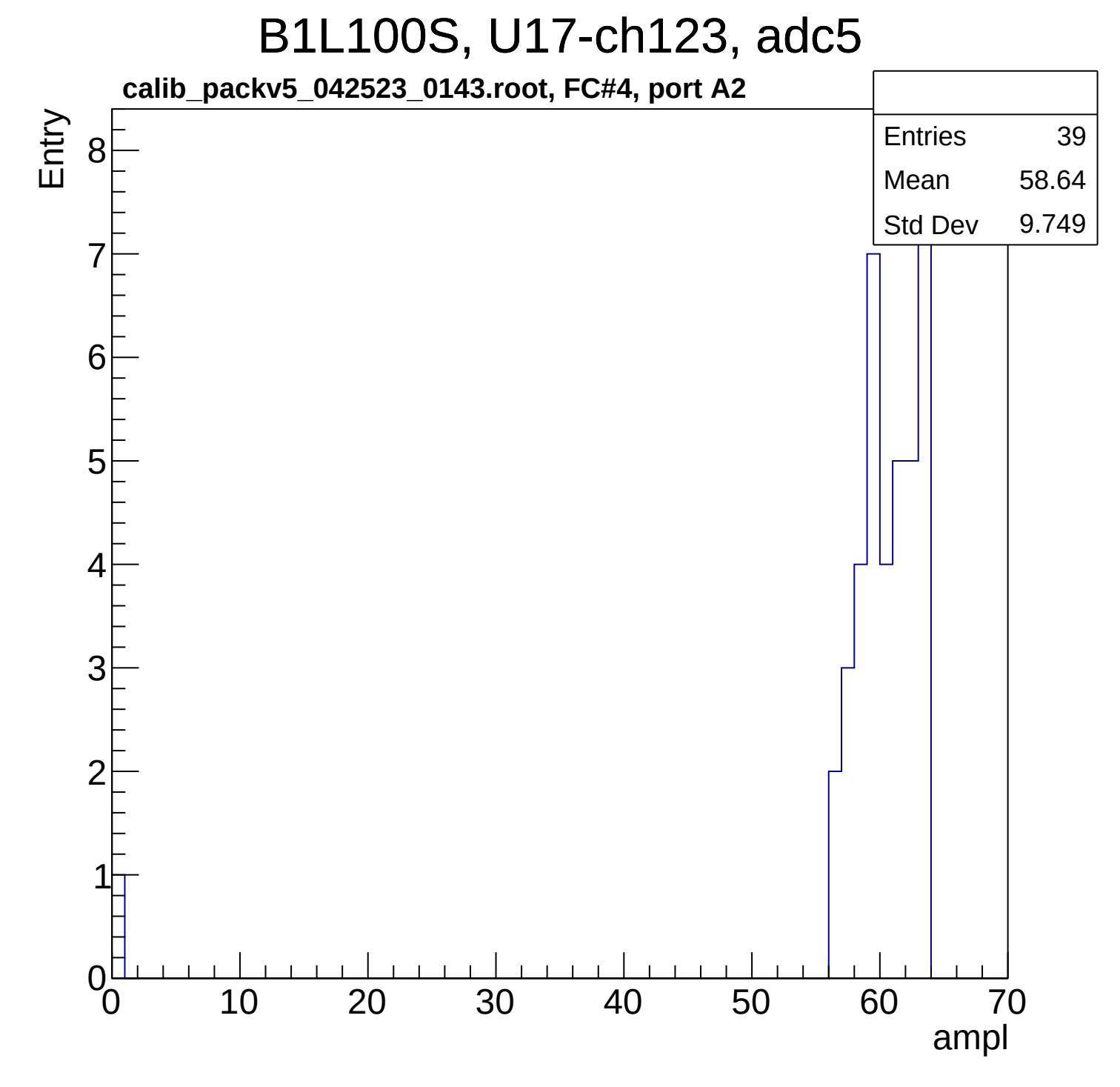
B1L100S, U17-ch123, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 39
Mean 58.64
Std Dev 9.749
Entry
ampl
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1
2
3
4
5
6
7
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0
10
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40
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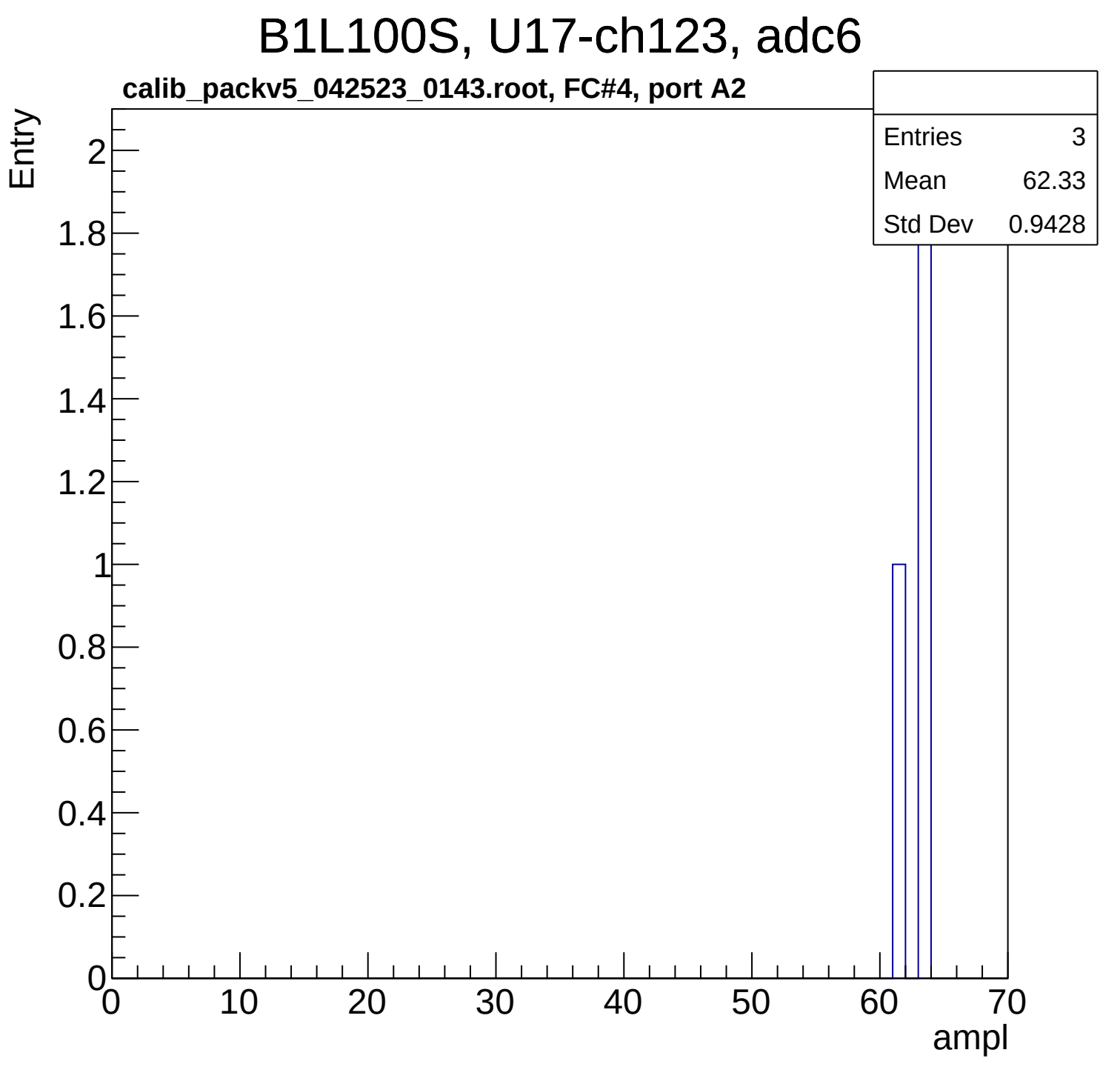
B1L100S, U17-ch123, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 62.33
Std Dev 0.9428
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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40
50
60
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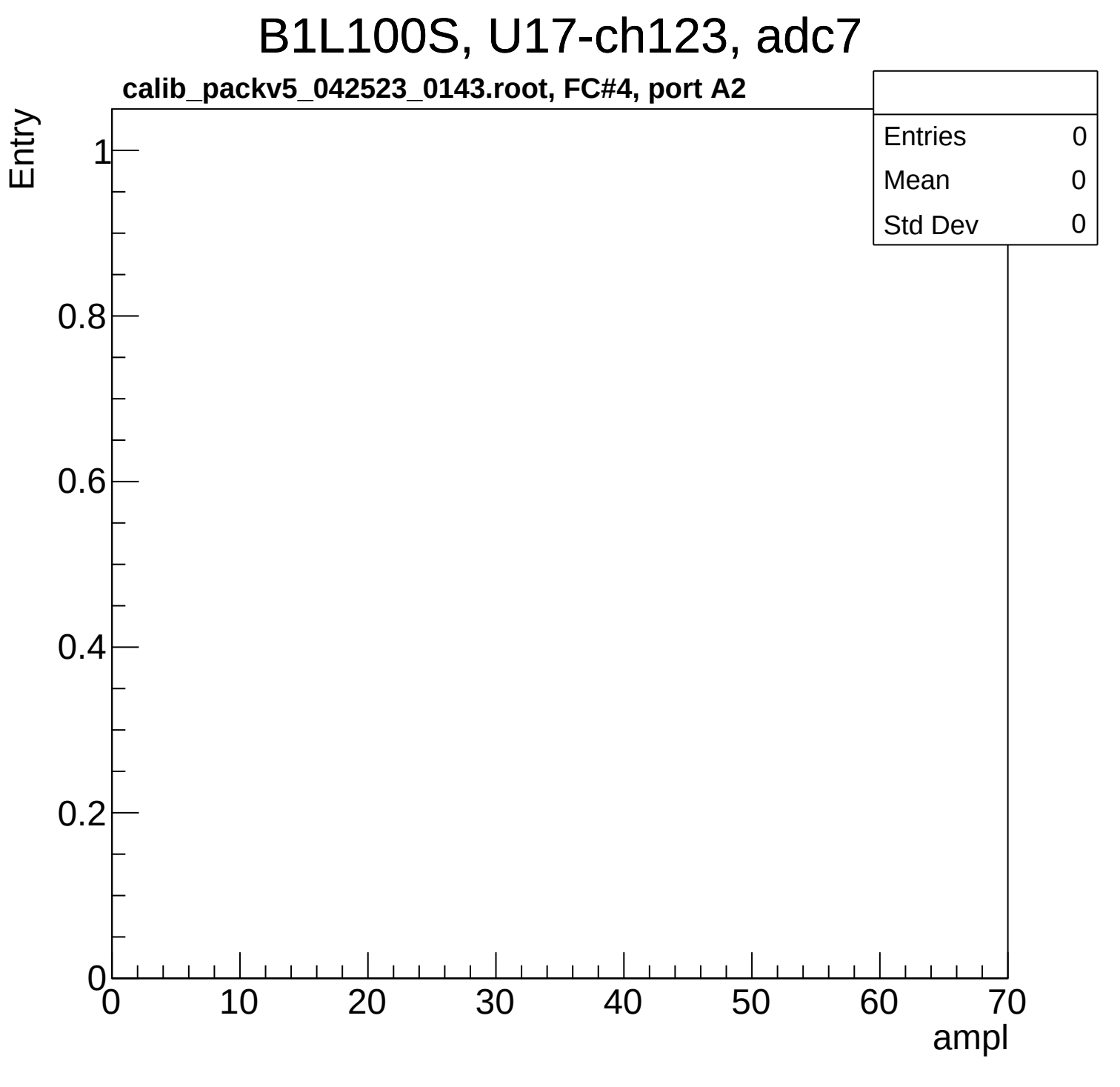
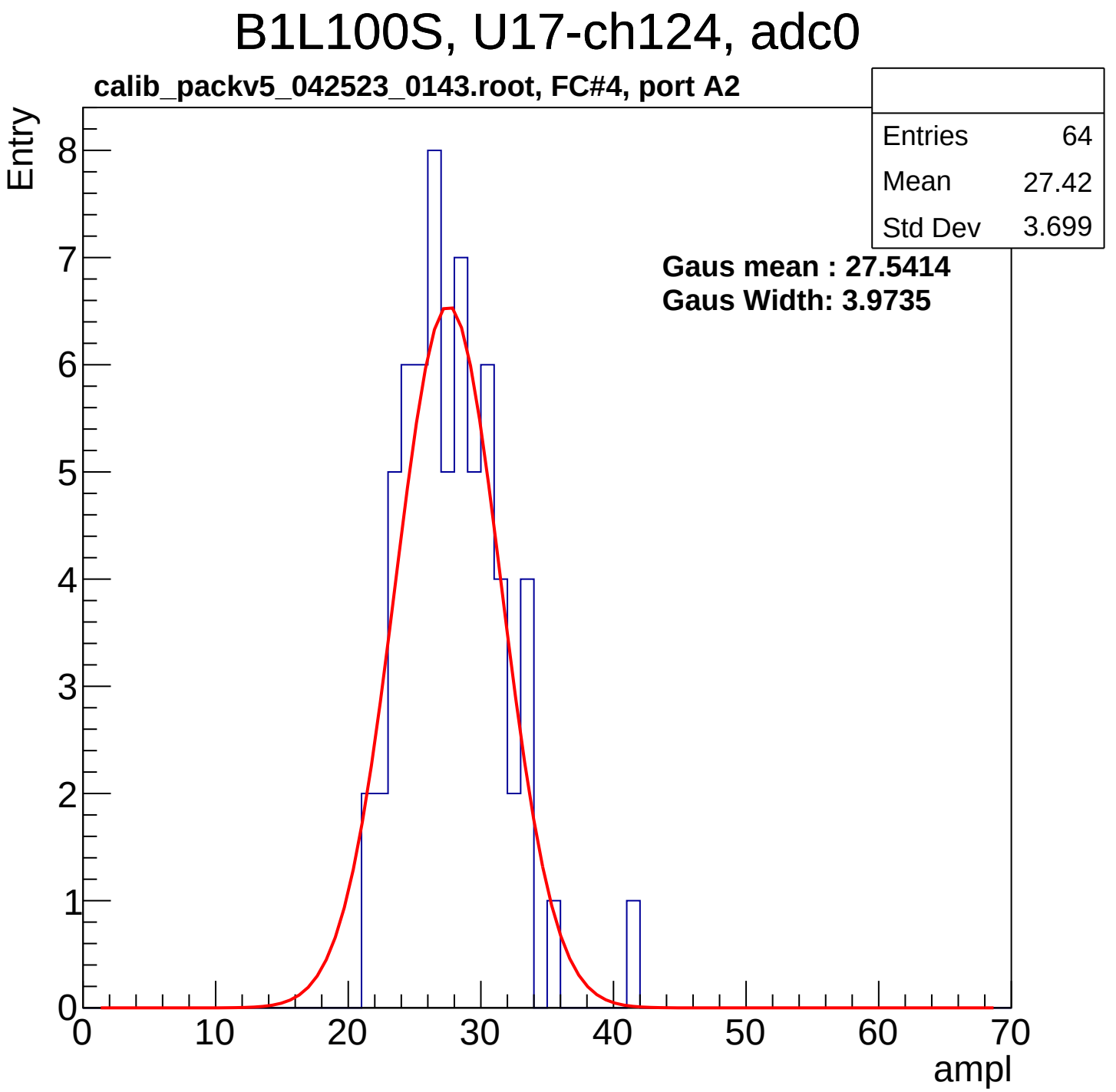

B1L100S, U17-ch123, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch124, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 27.42
Std Dev 3.699
Gaus mean : 27.5414
Gaus Width: 3.9735
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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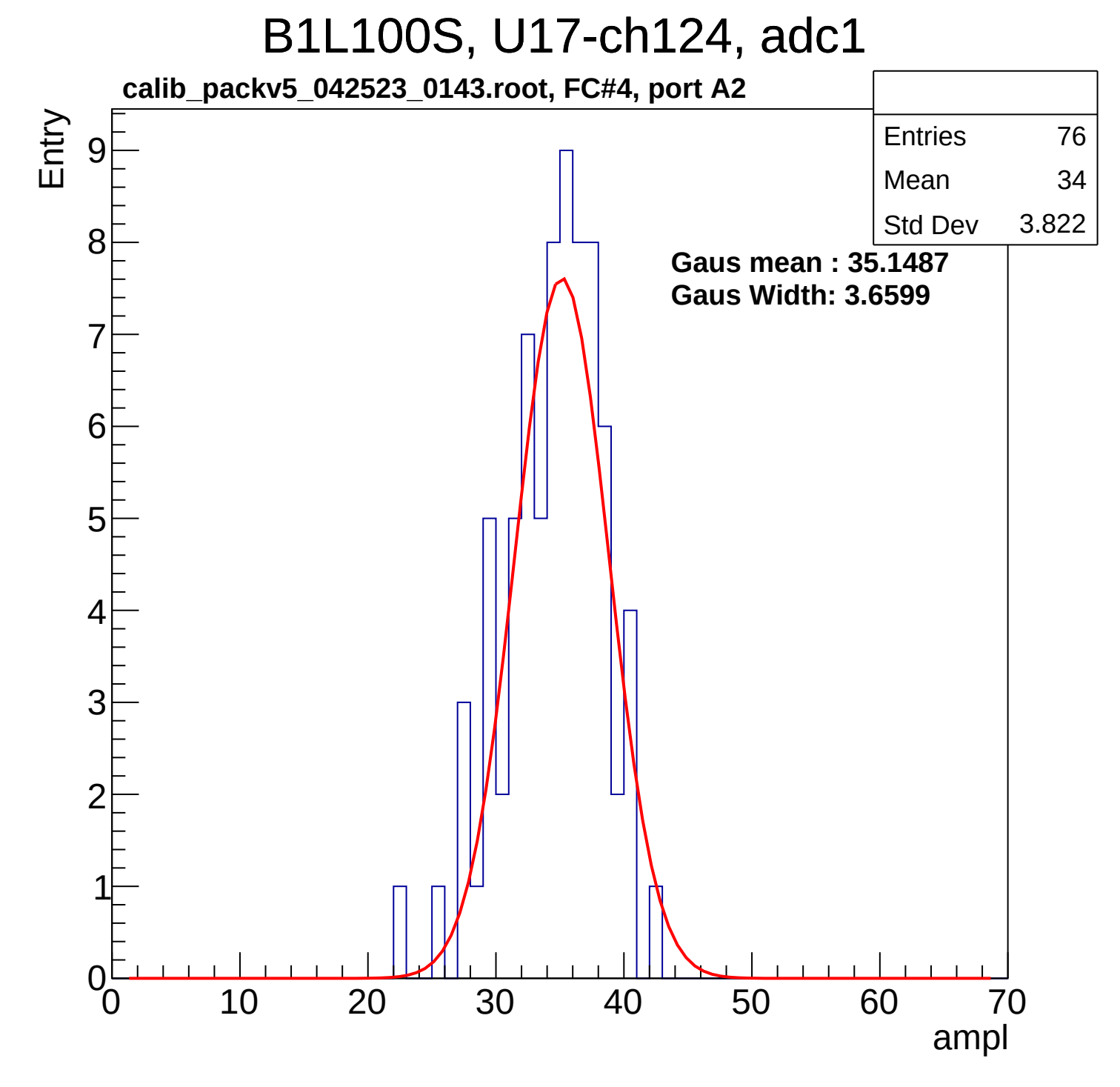
B1L100S, U17-ch124, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 76
Mean 34
Std Dev 3.822
Gaus mean : 35.1487
Gaus Width: 3.6599
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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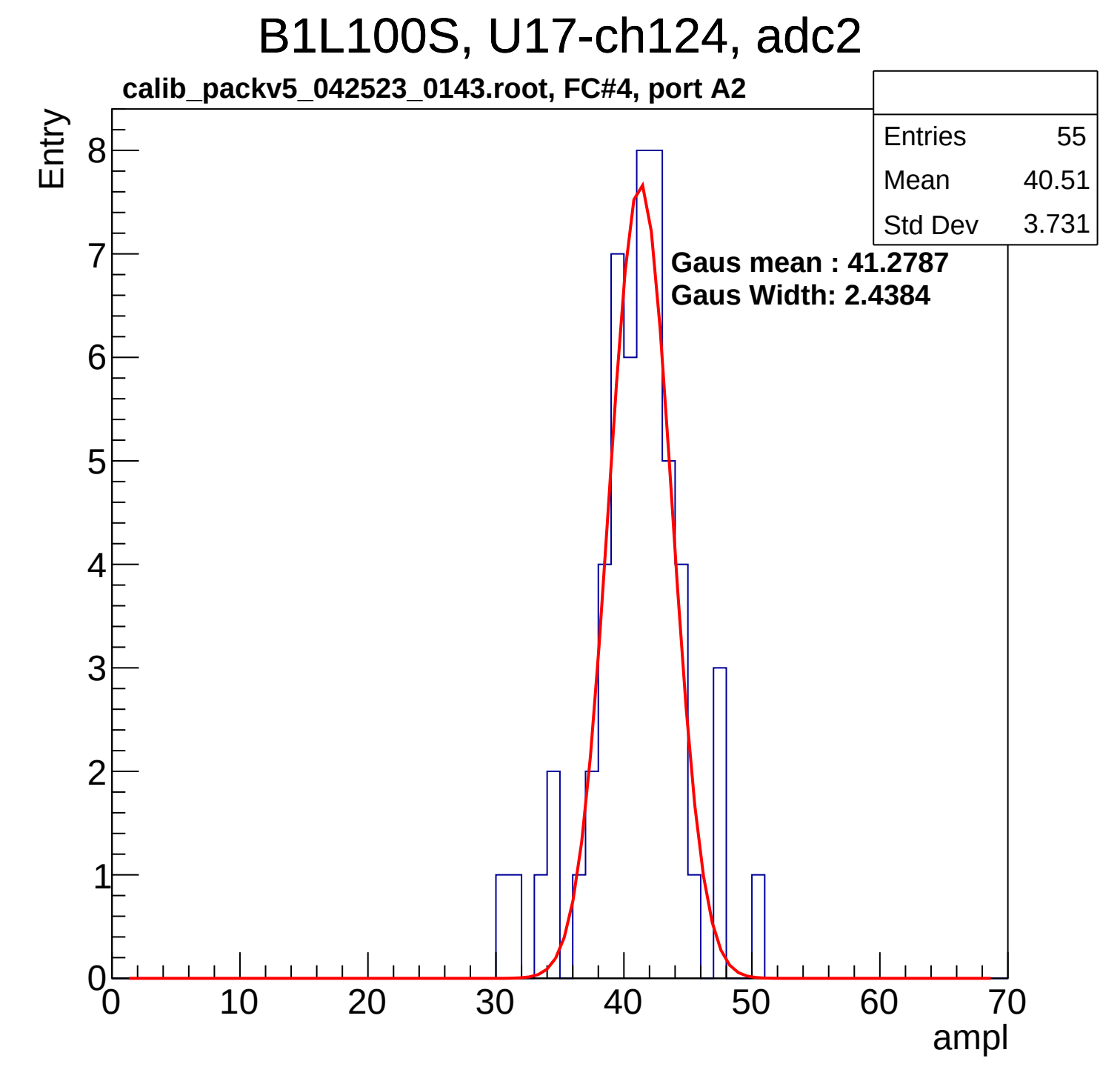
B1L100S, U17-ch124, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 40.51
Std Dev 3.731
Gaus mean : 41.2787
Gaus Width: 2.4384
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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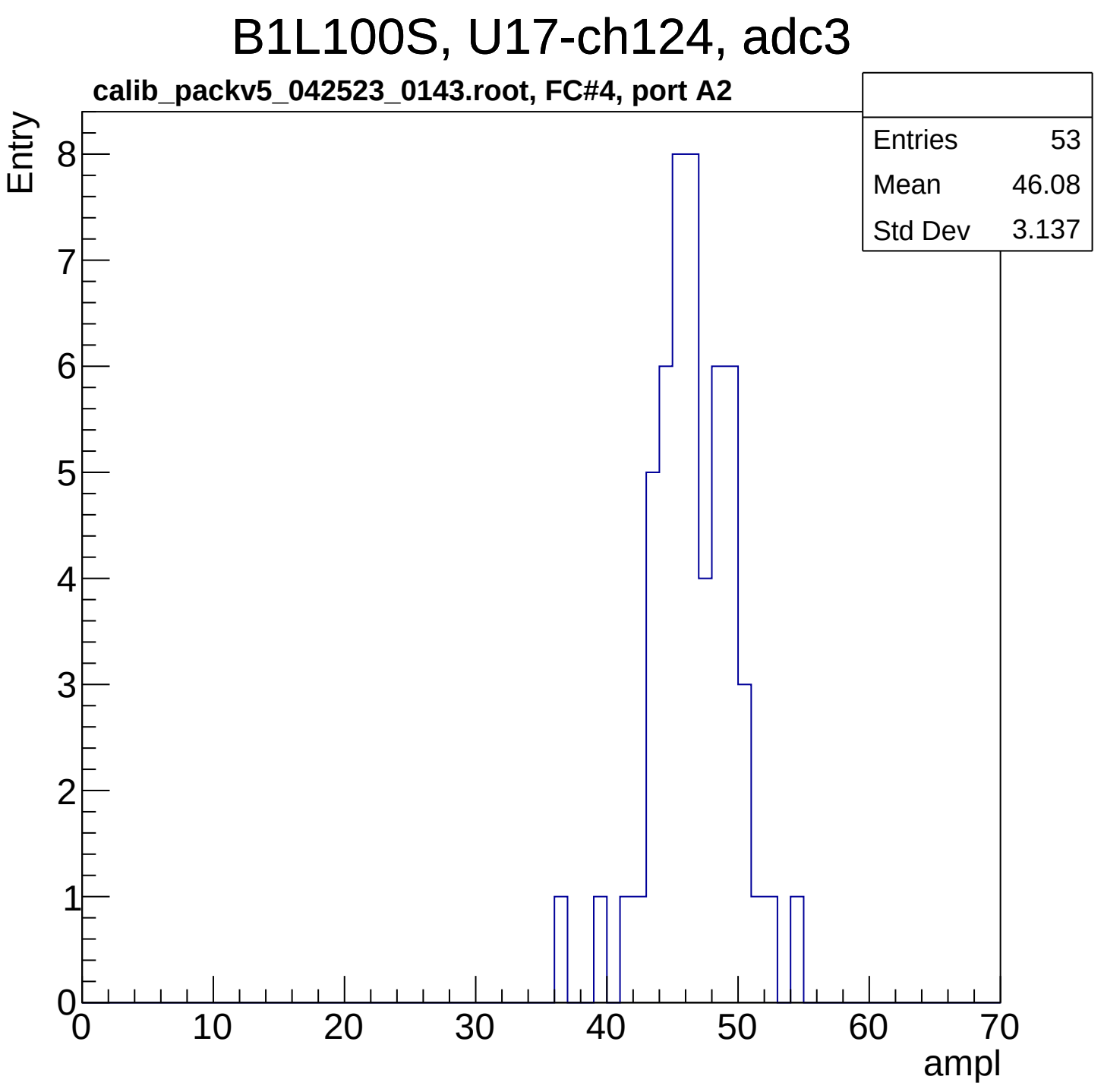
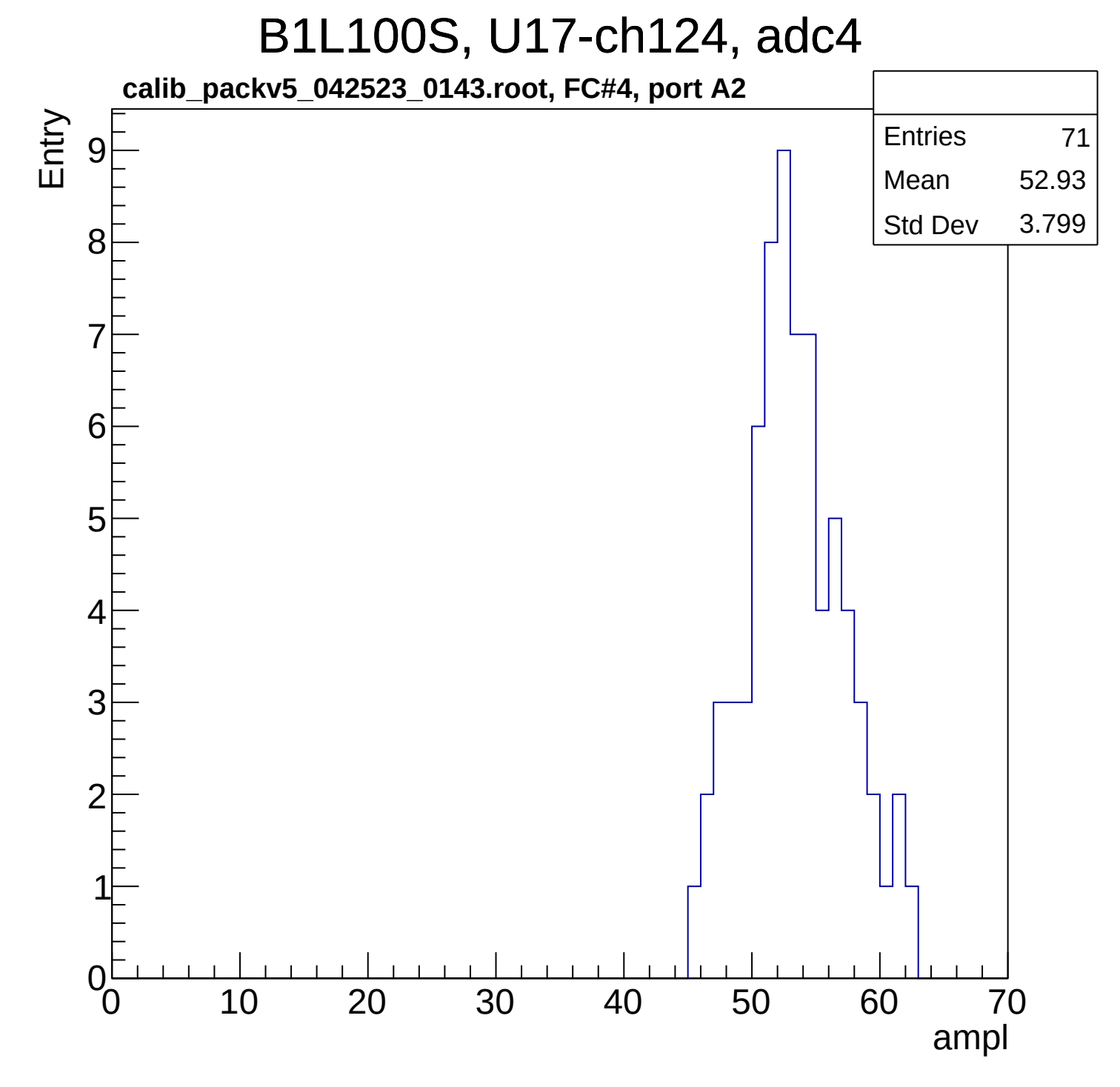
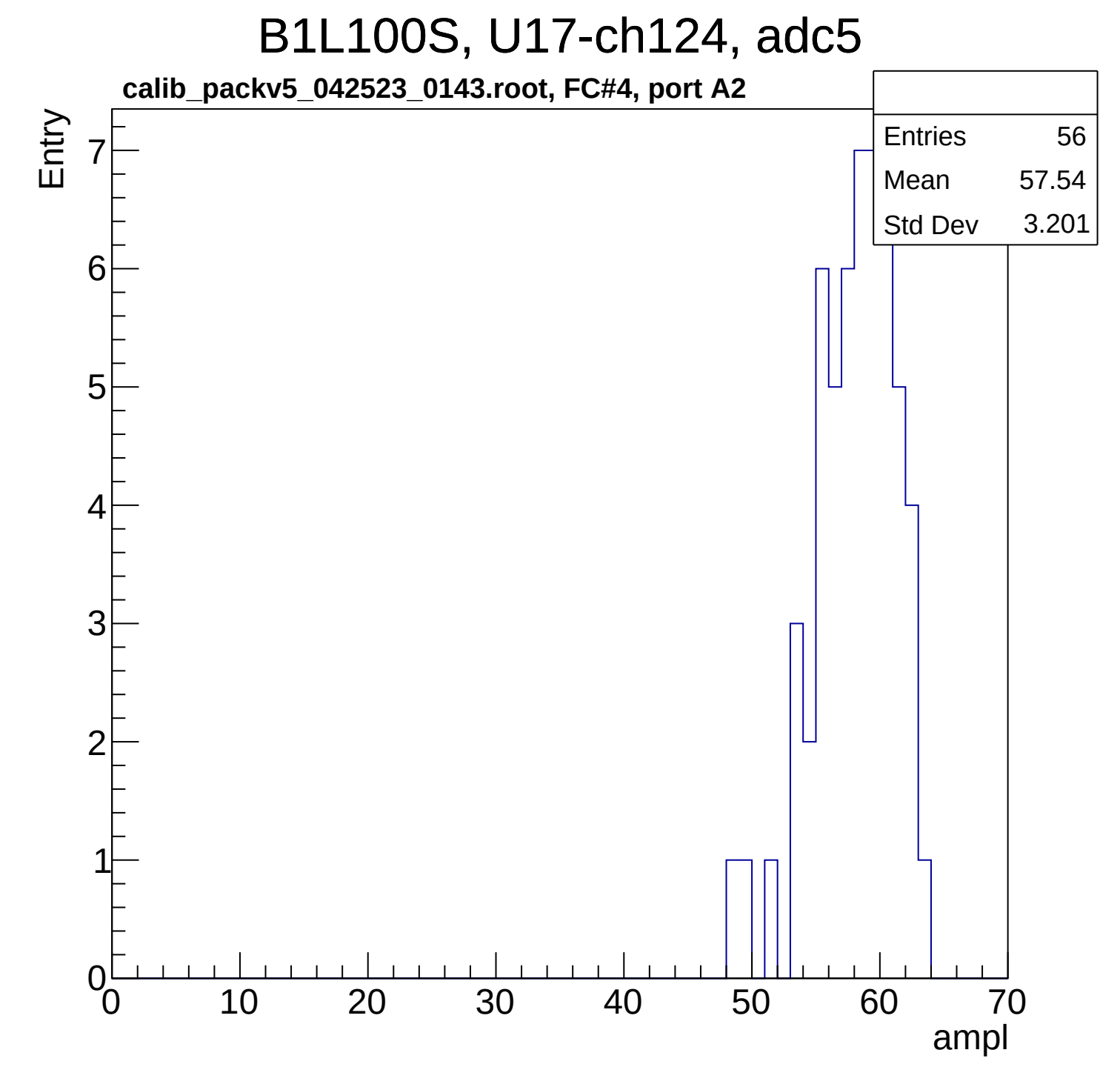

B1L100S, U17-ch124, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 46.08
Std Dev 3.137
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch124, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 52.93
Std Dev 3.799
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch124, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 57.54
Std Dev 3.201
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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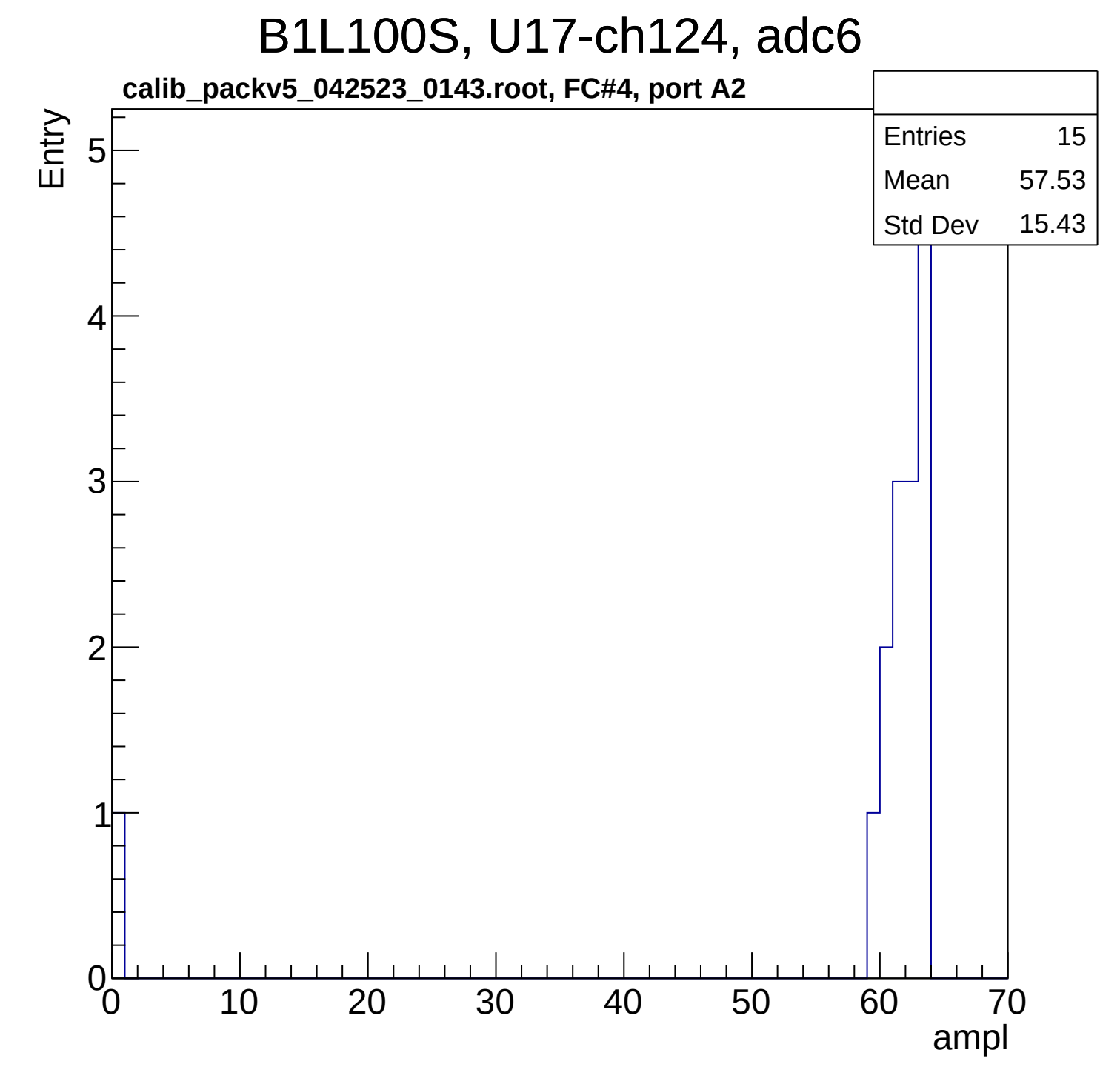
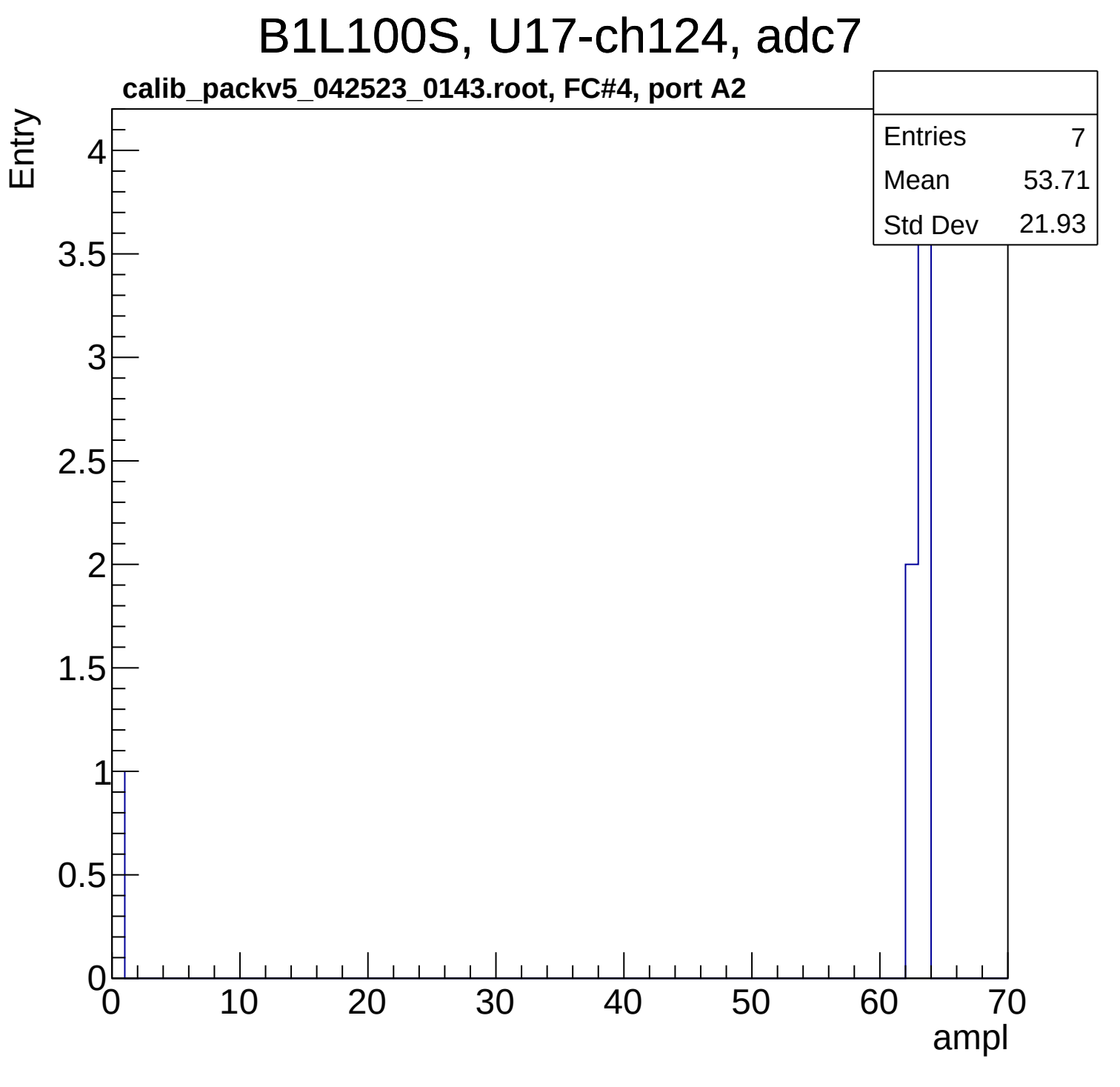
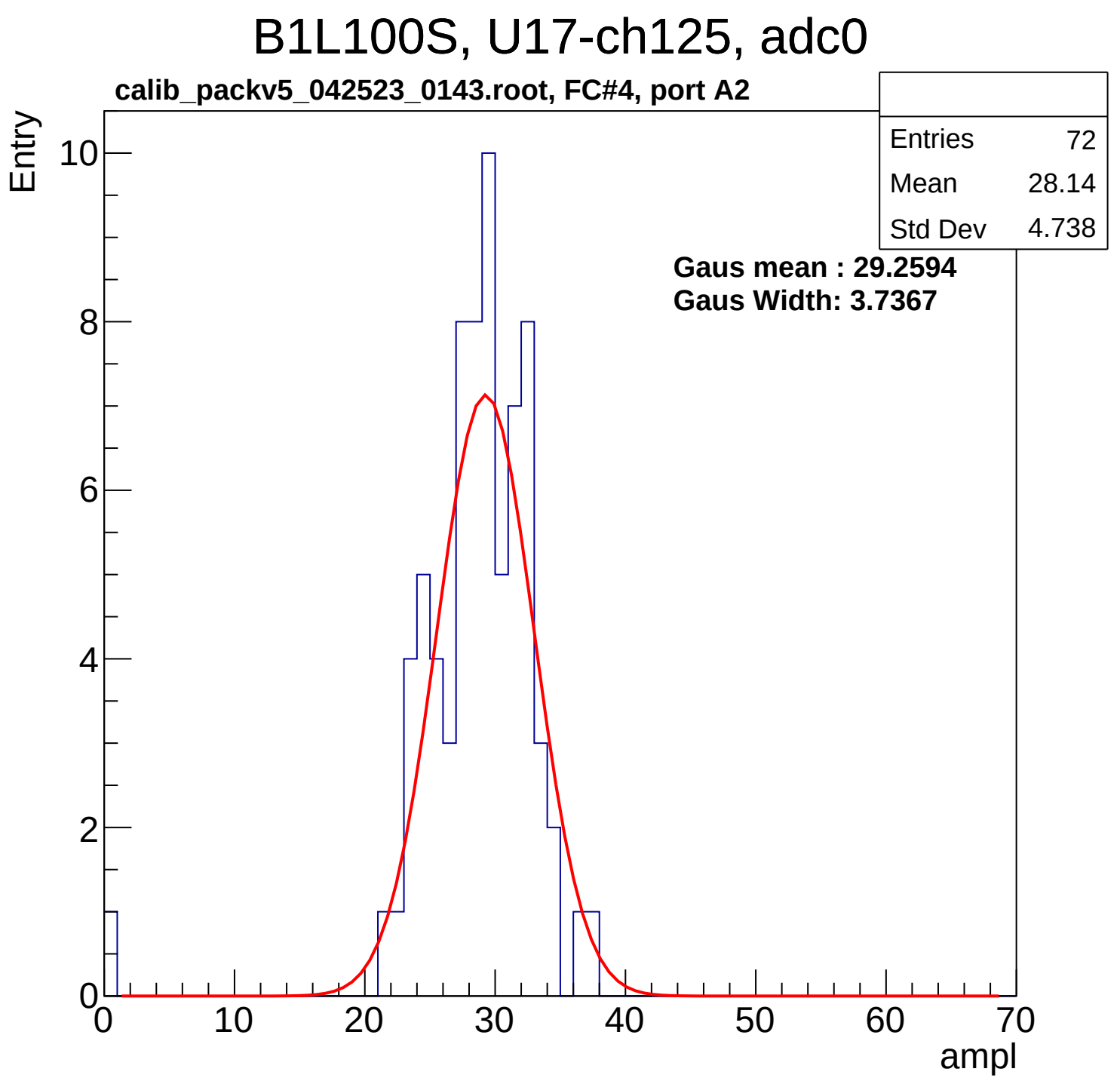
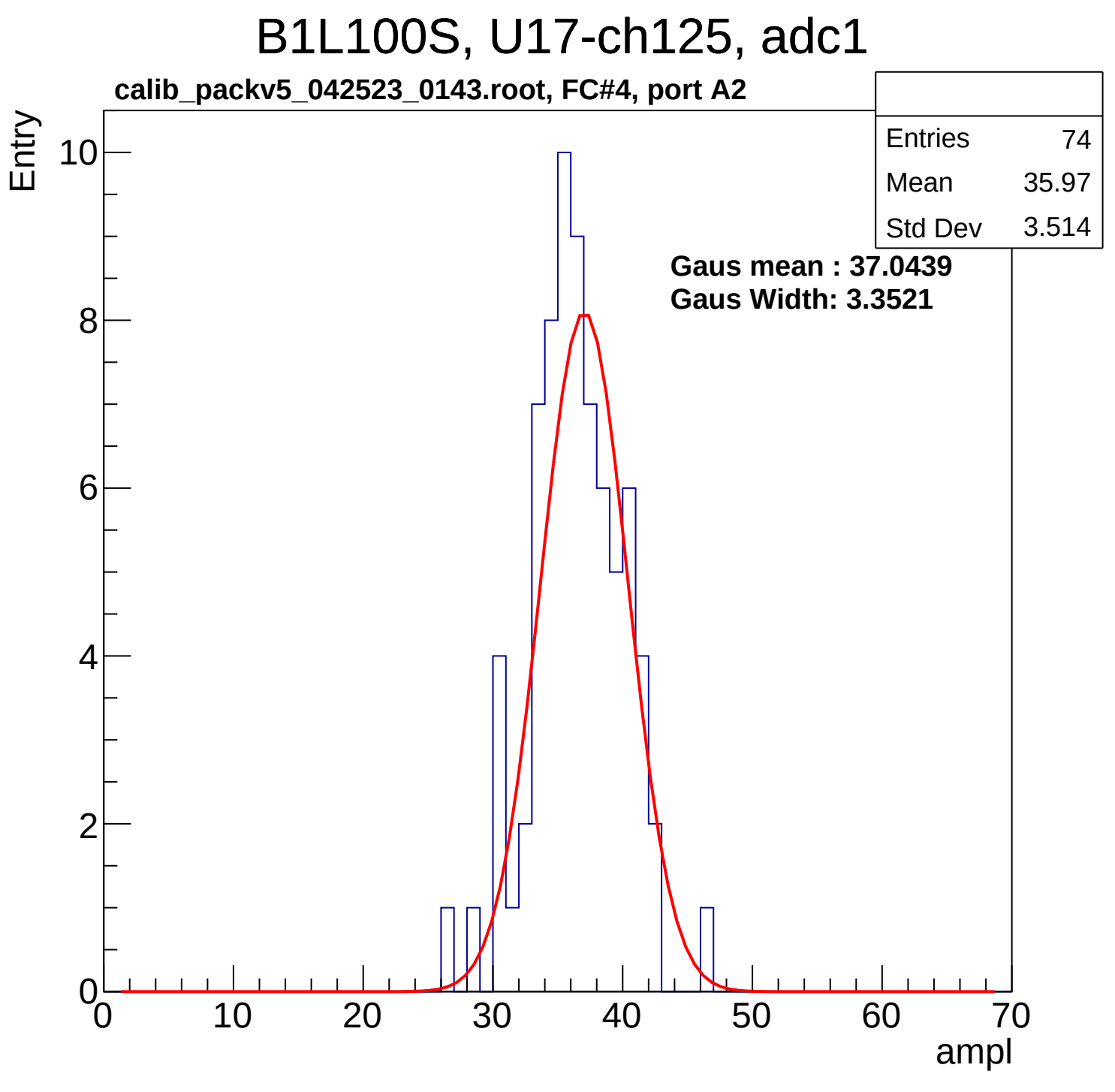
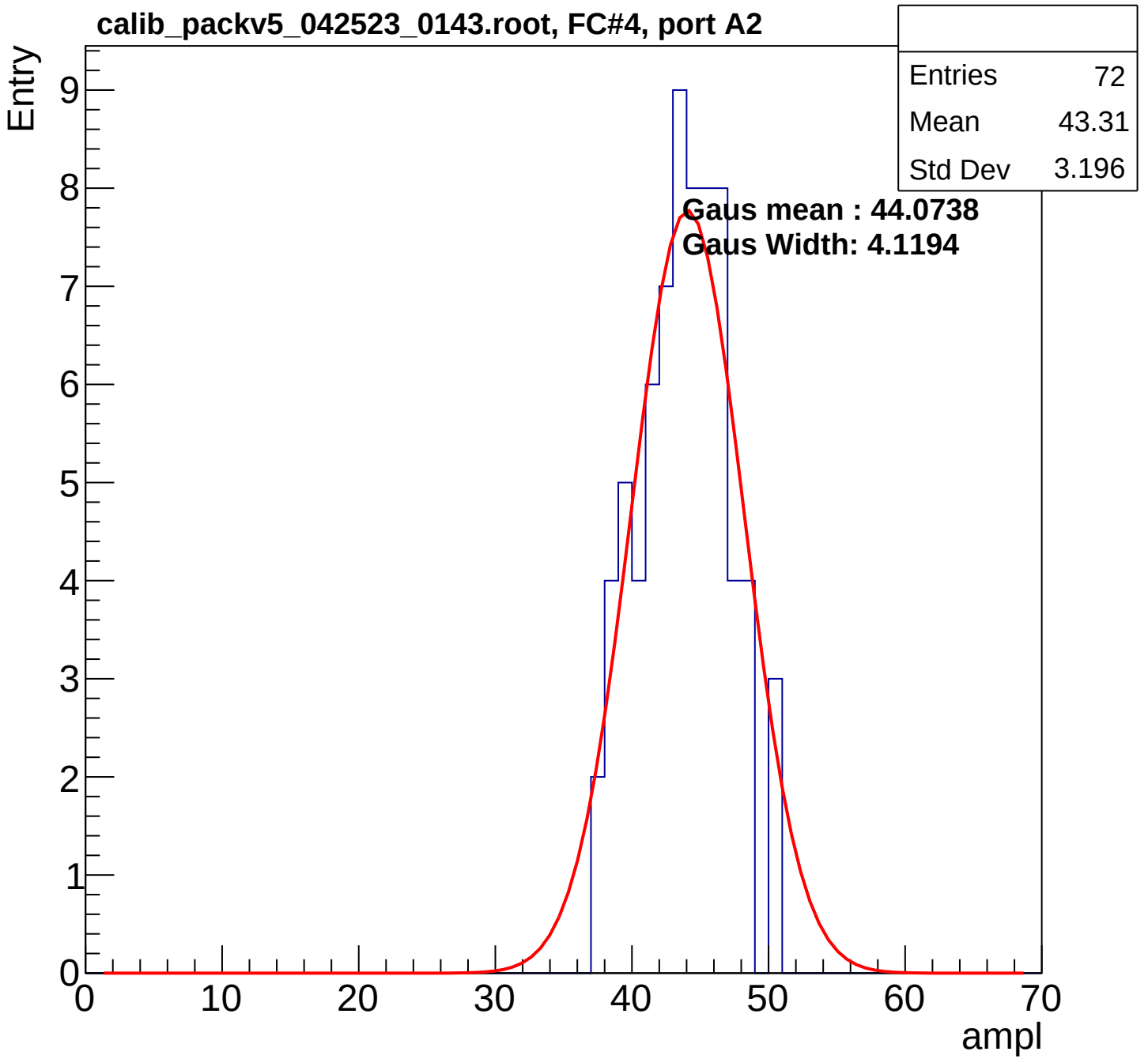
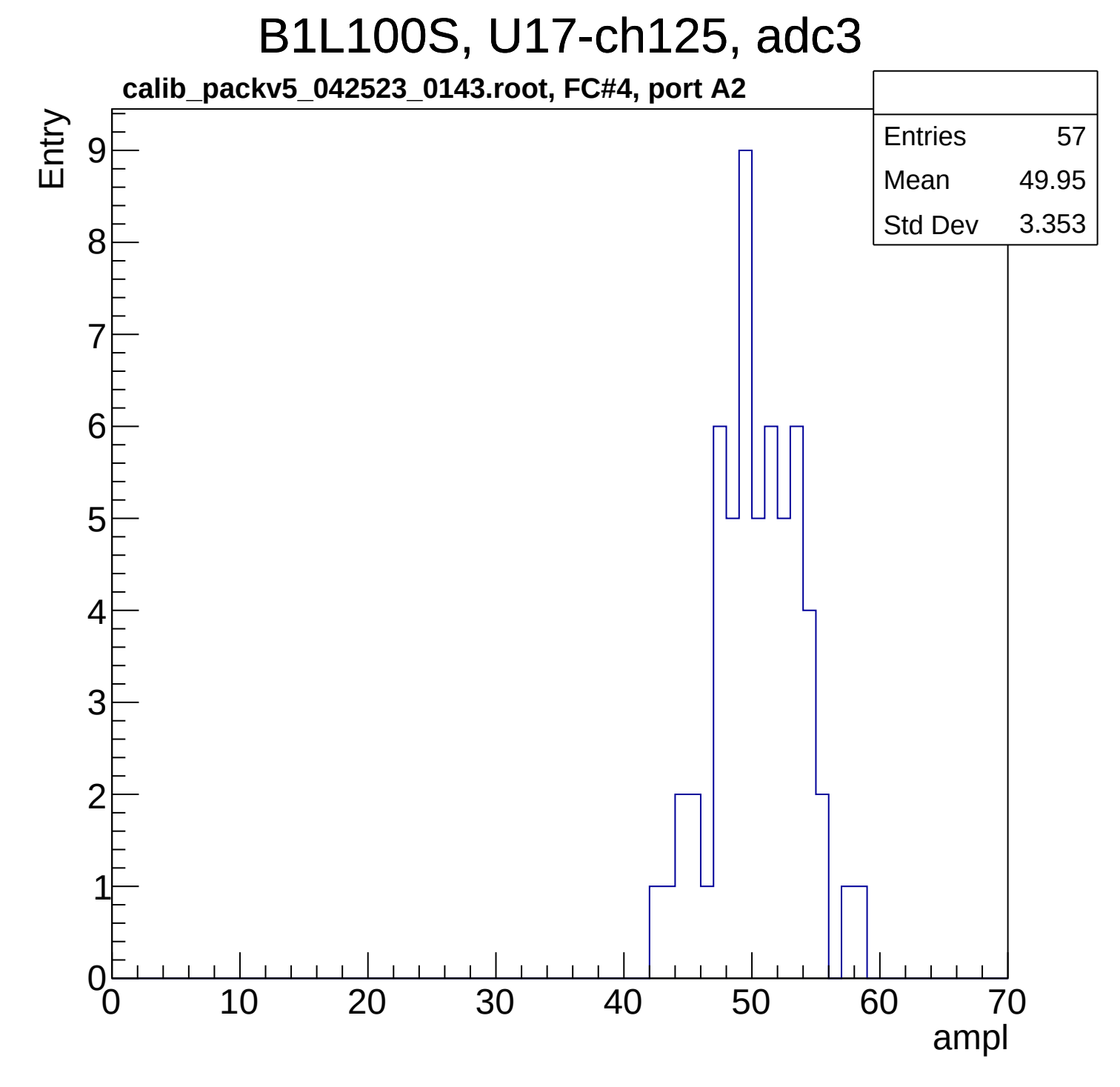

B1L100S, U17-ch124, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 15
Mean 57.53
Std Dev 15.43
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L100S, U17-ch124, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 7
Mean 53.71
Std Dev 21.93
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L100S, U17-ch125, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 28.14
Std Dev 4.738
Gaus mean : 29.2594
Gaus Width: 3.7367
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U17-ch125, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 74
Mean 35.97
Std Dev 3.514
Gaus mean : 37.0439
Gaus Width: 3.3521
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L100S, U17-ch125, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 43.31
Std Dev 3.196
Gaus mean : 44.0738
Gaus Width: 4.1194
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch125, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 49.95
Std Dev 3.353
Entry
ampl
0
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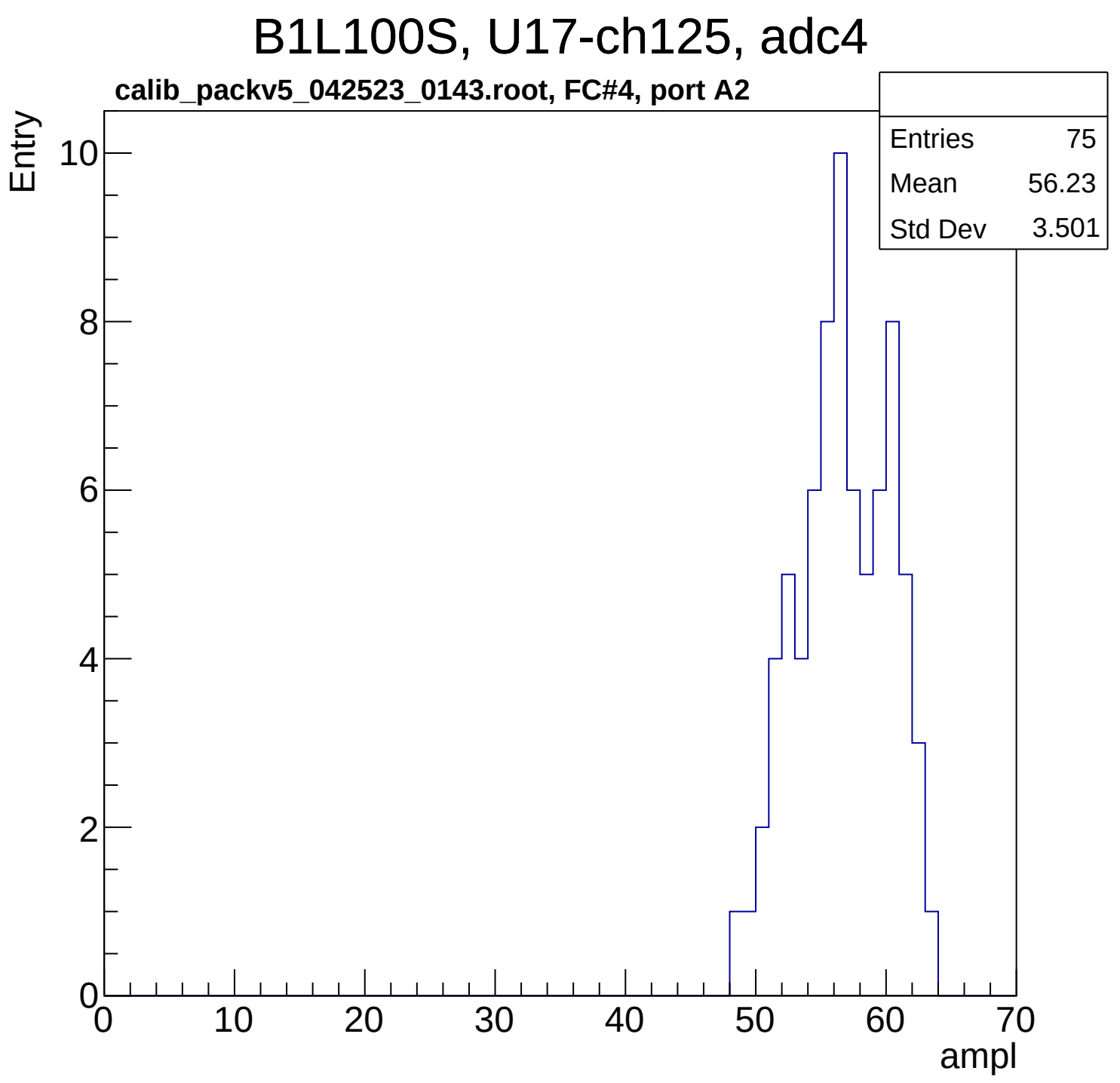
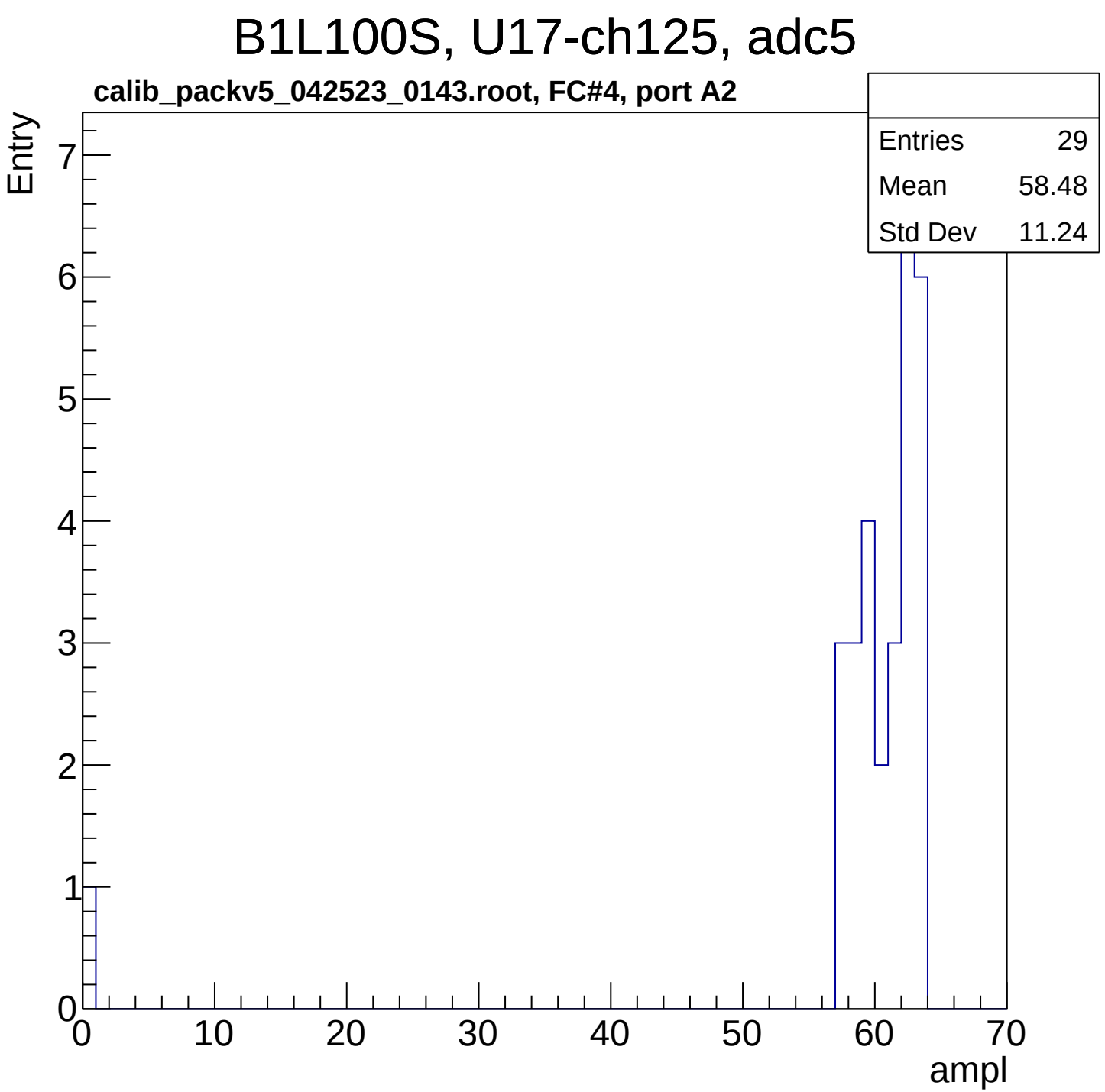
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch125, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 75
Mean 56.23
Std Dev 3.501
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch125, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 29
Mean 58.48
Std Dev 11.24
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
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60
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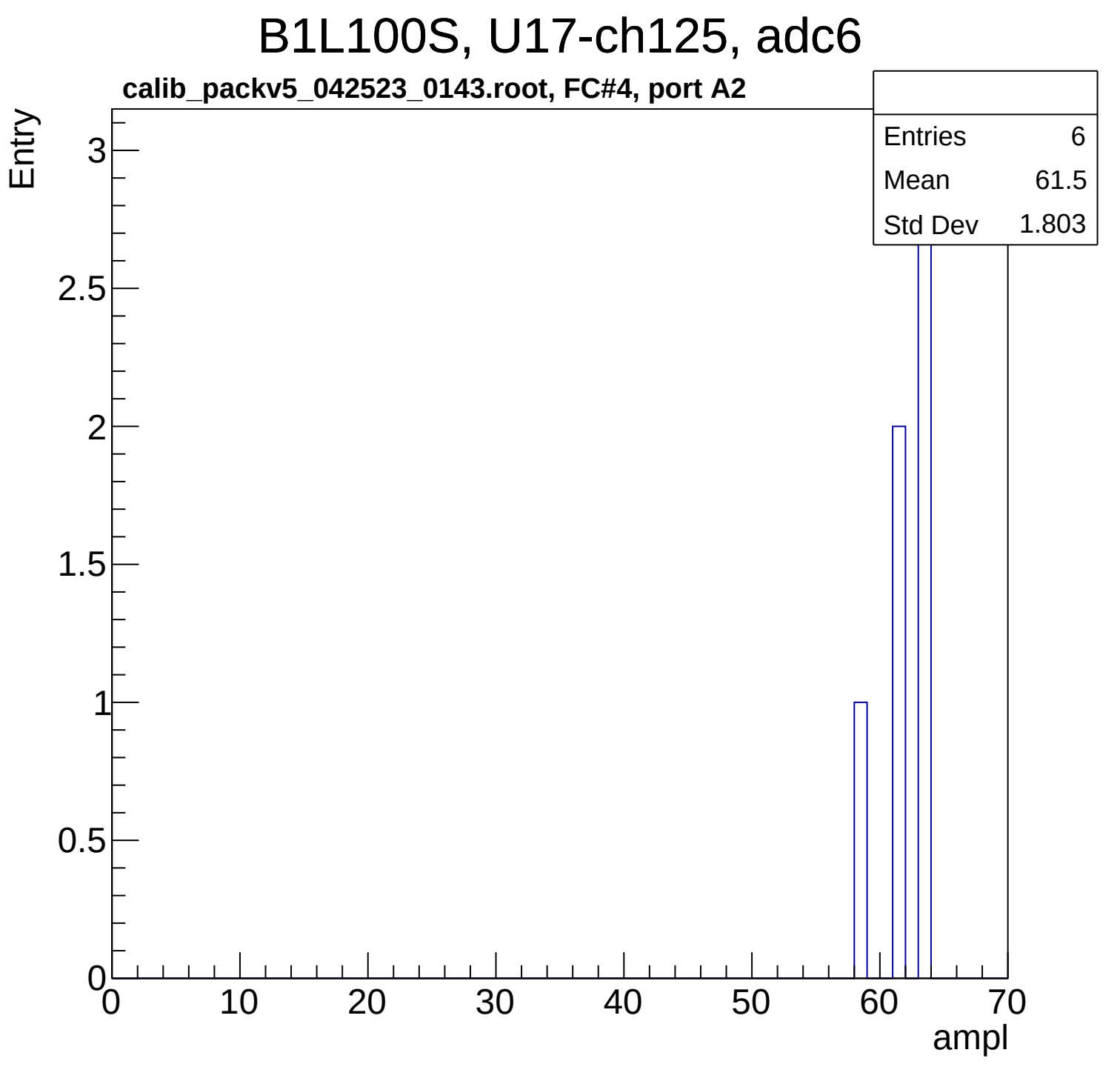
B1L100S, U17-ch125, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 6
Mean 61.5
Std Dev 1.803
Entry
ampl
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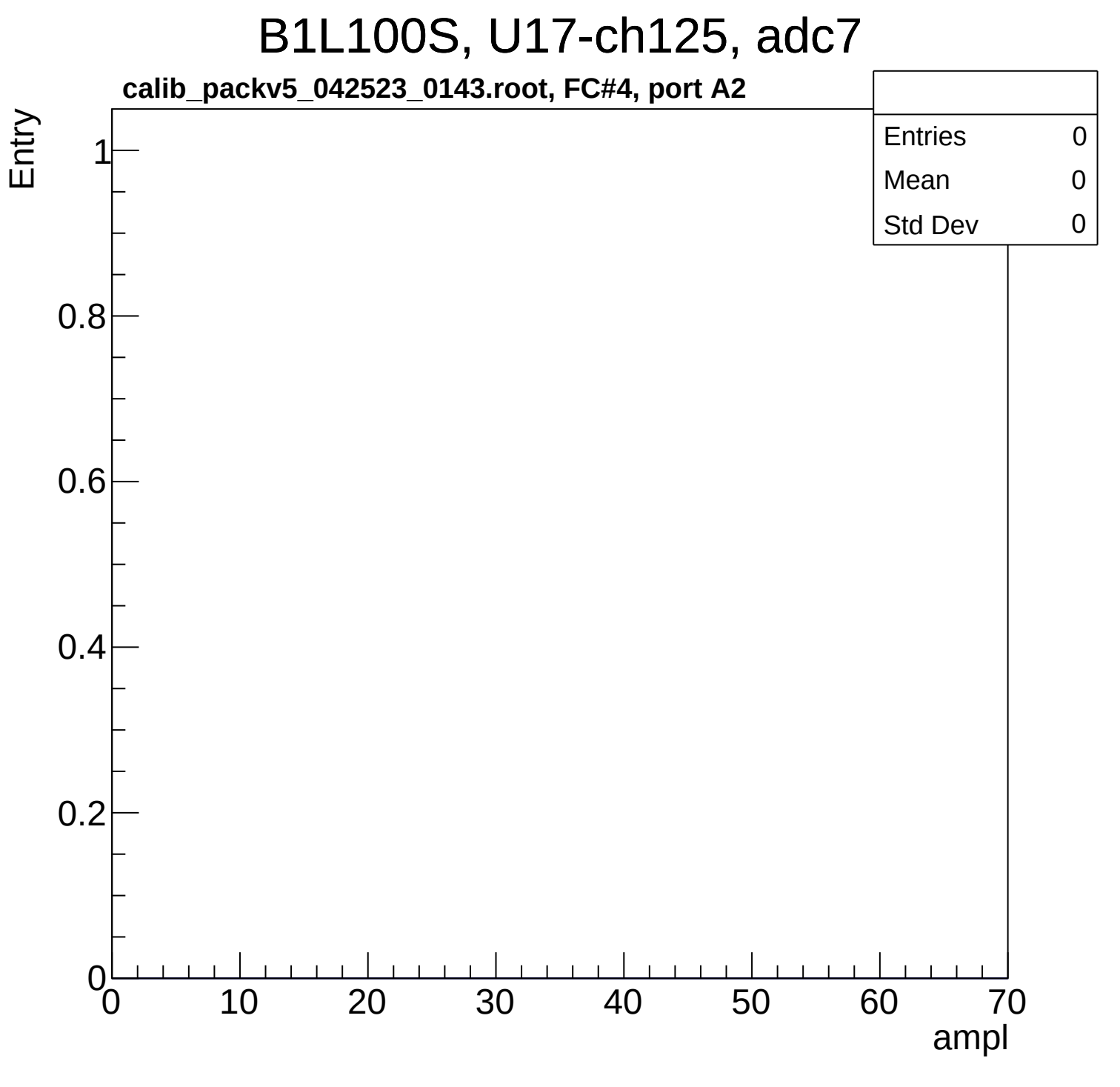
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L100S, U17-ch125, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
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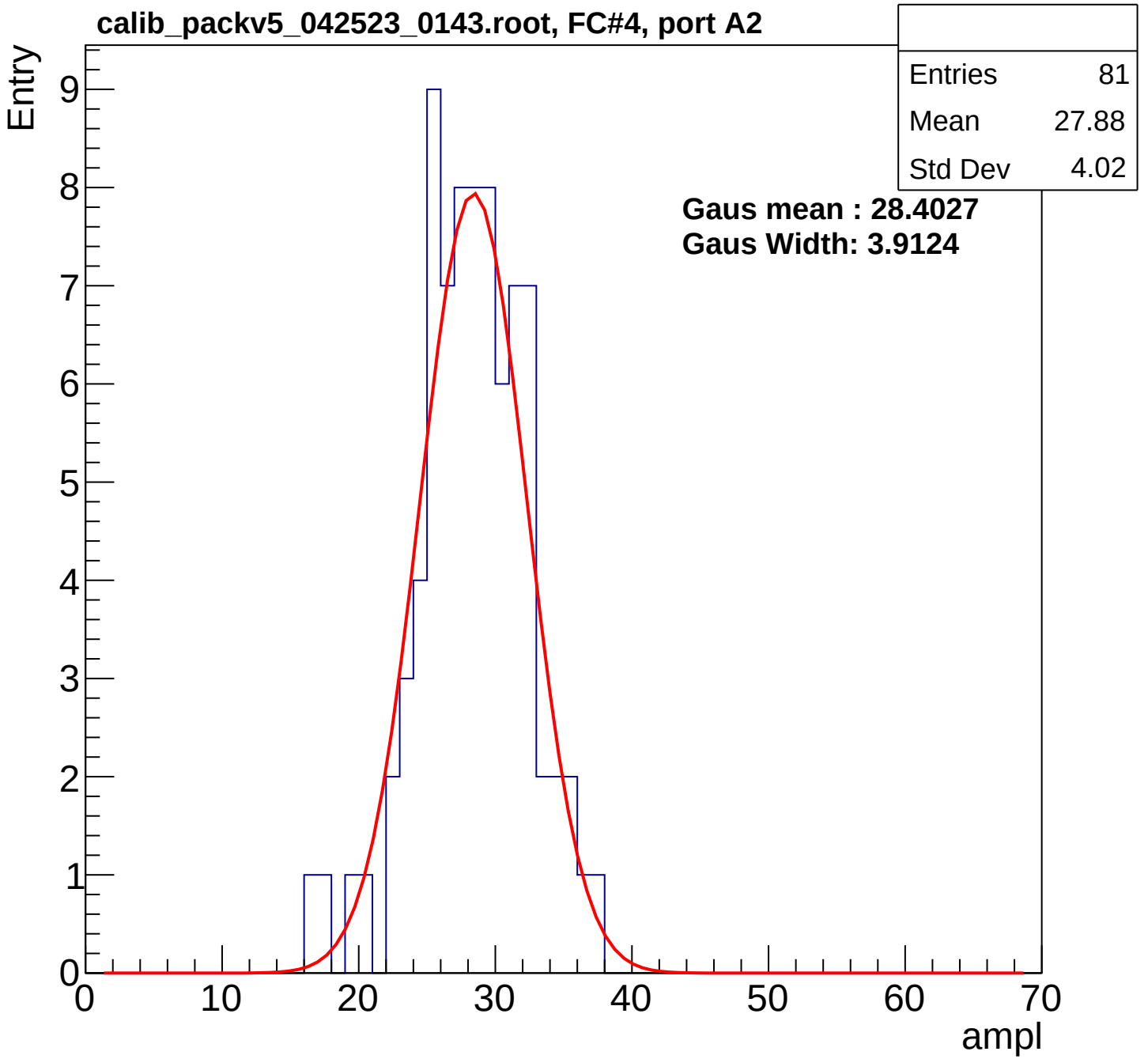
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch126, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 81
Mean 27.88
Std Dev 4.02
Gaus mean : 28.4027
Gaus Width: 3.9124
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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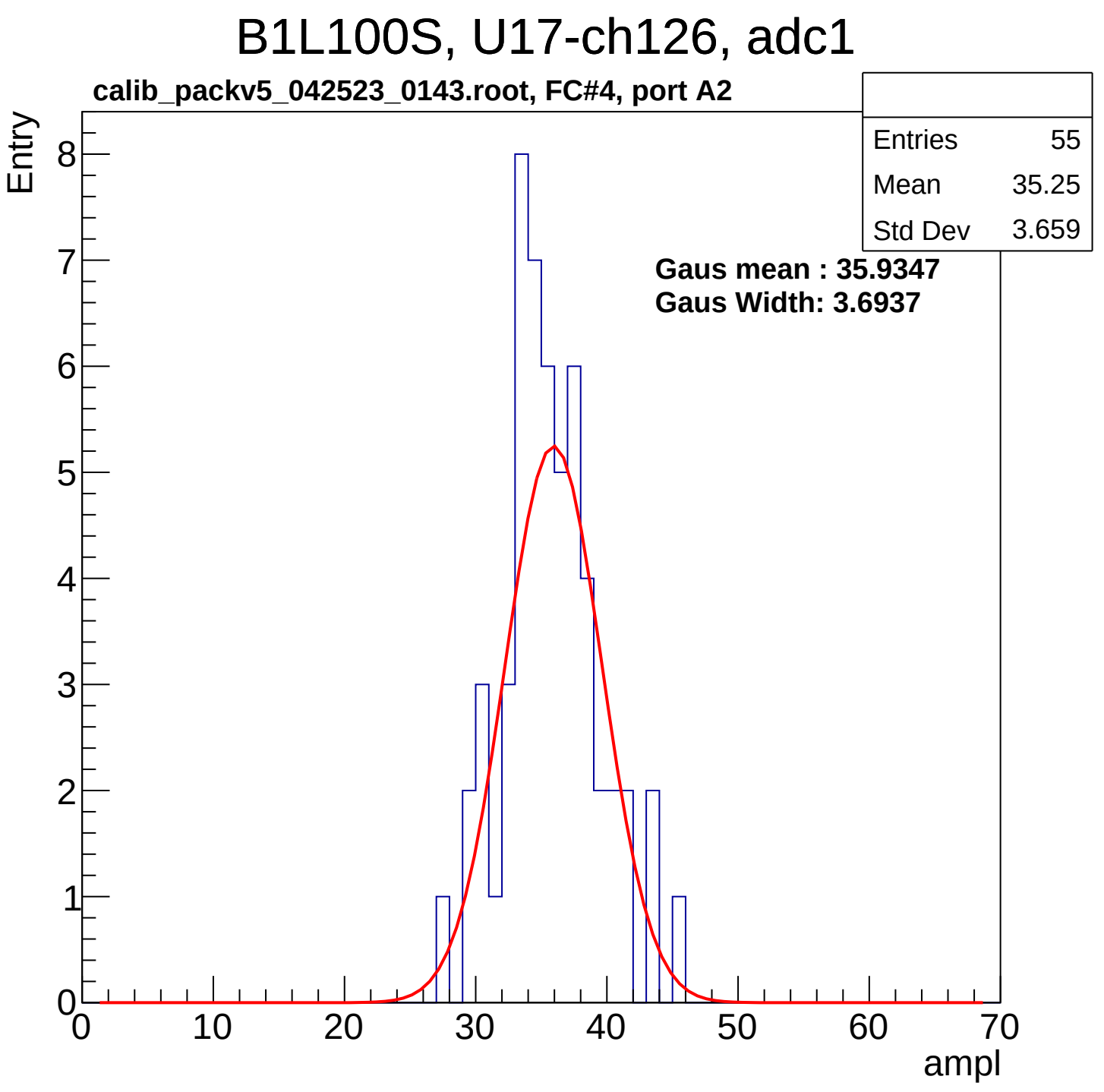
40
50
60
70


B1L100S, U17-ch126, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 35.25
Std Dev 3.659
Gaus mean : 35.9347
Gaus Width: 3.6937
Entry
ampl
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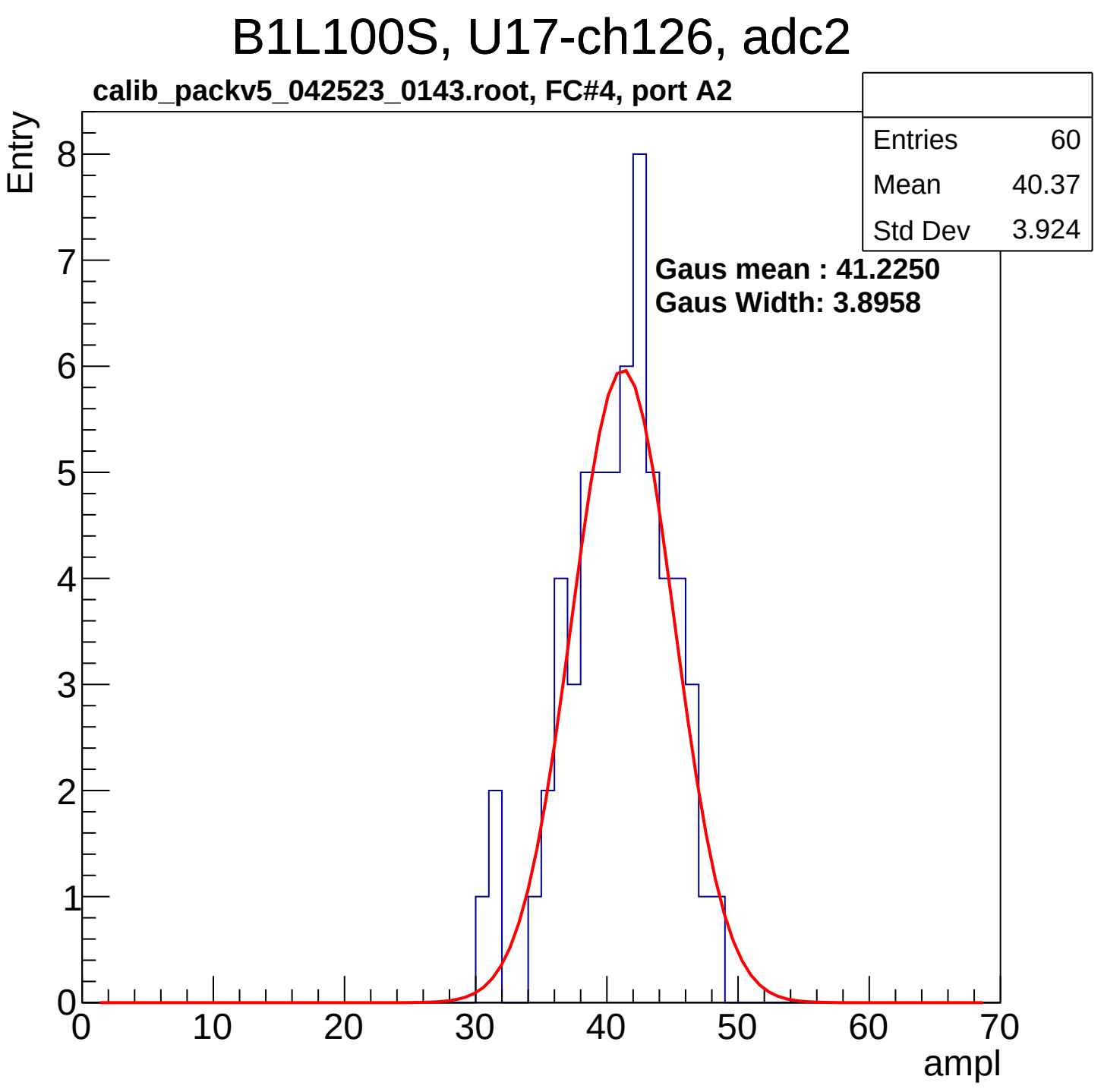
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch126, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 40.37
Std Dev 3.924
Gaus mean : 41.2250
Gaus Width: 3.8958
Entry
ampl
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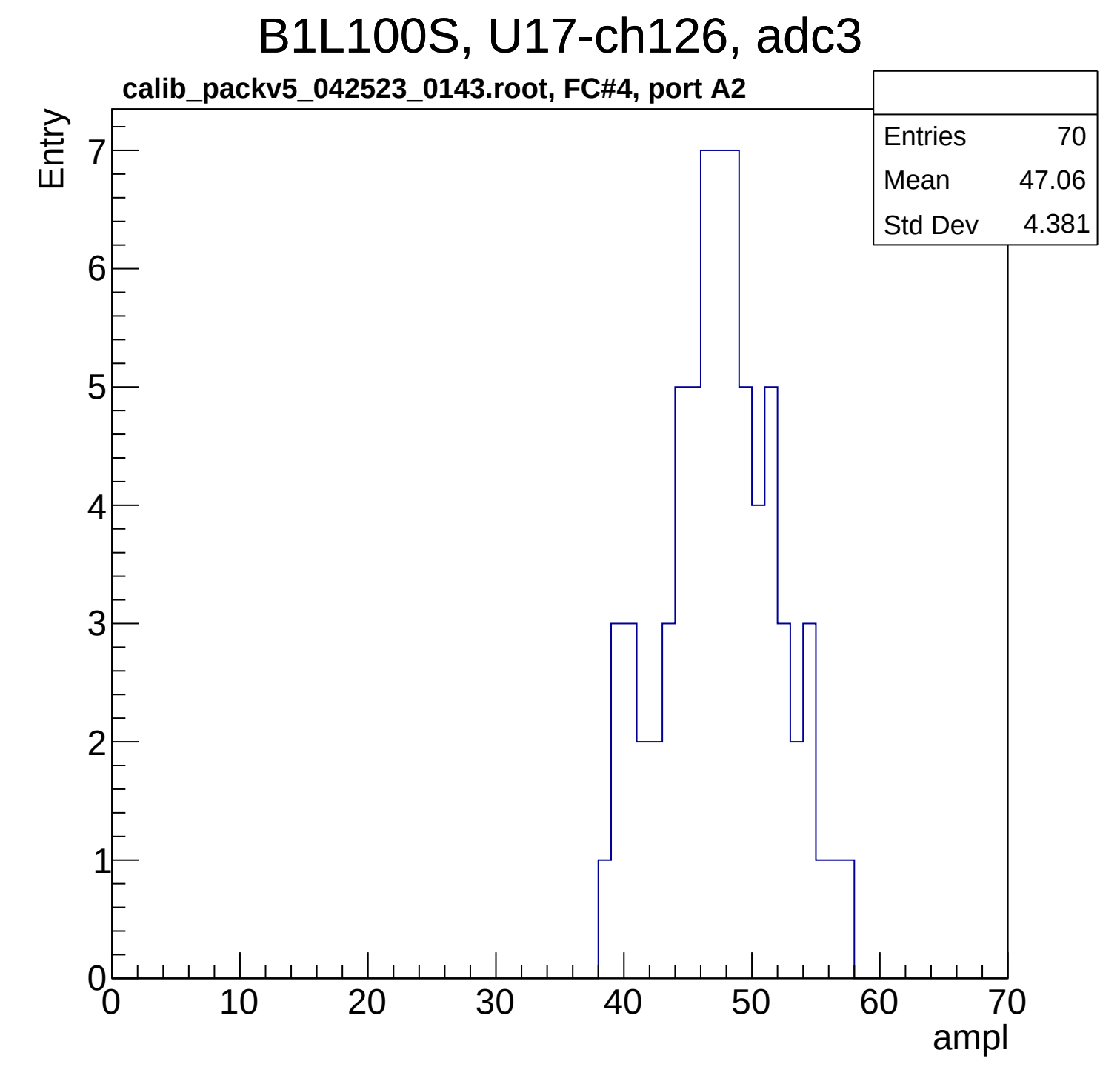
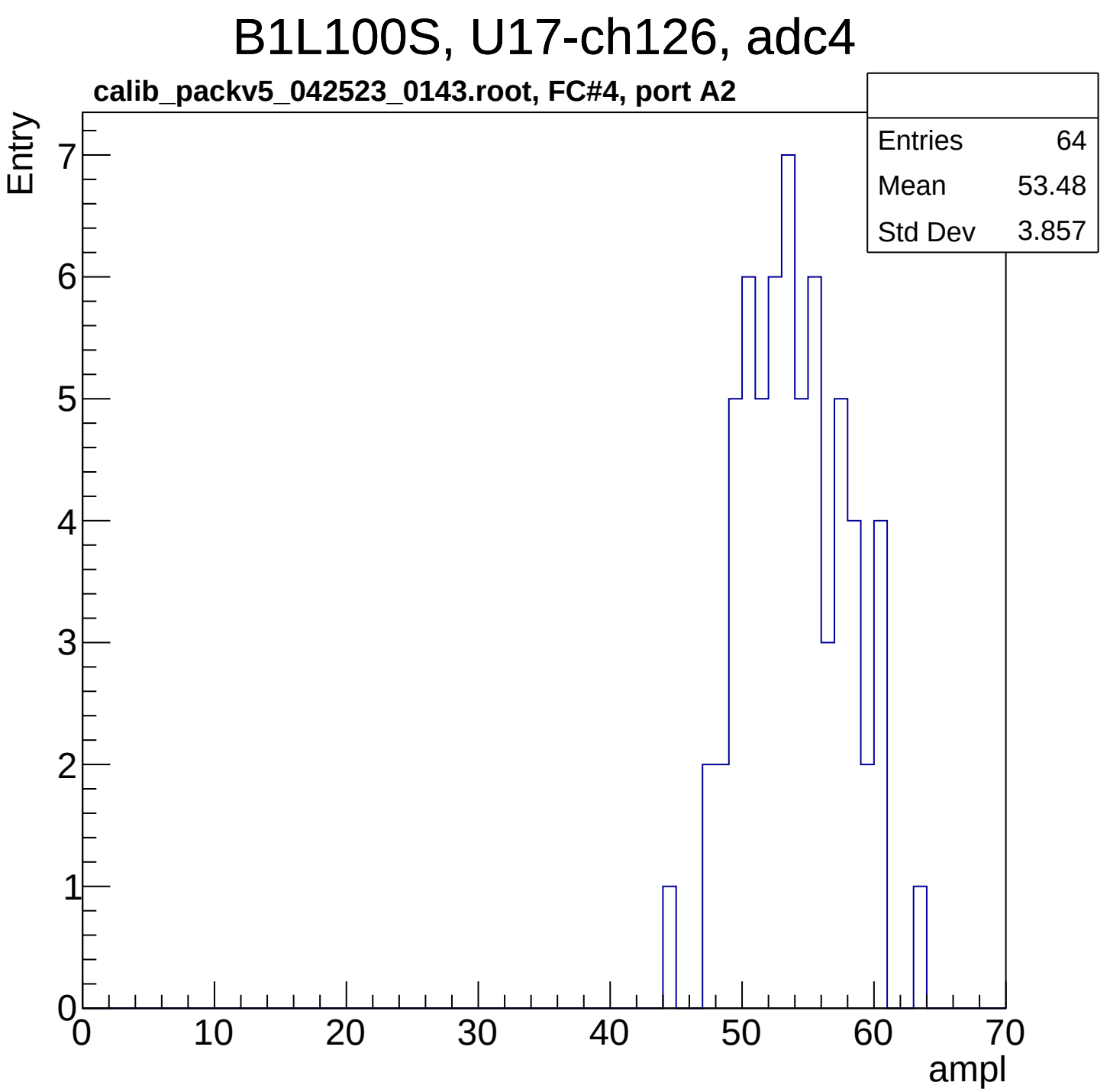
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch126, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 47.06
Std Dev 4.381
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U17-ch126, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 53.48
Std Dev 3.857
Entry
ampl
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1
2
3
4
5
6
7
0
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20
30
40
50
60
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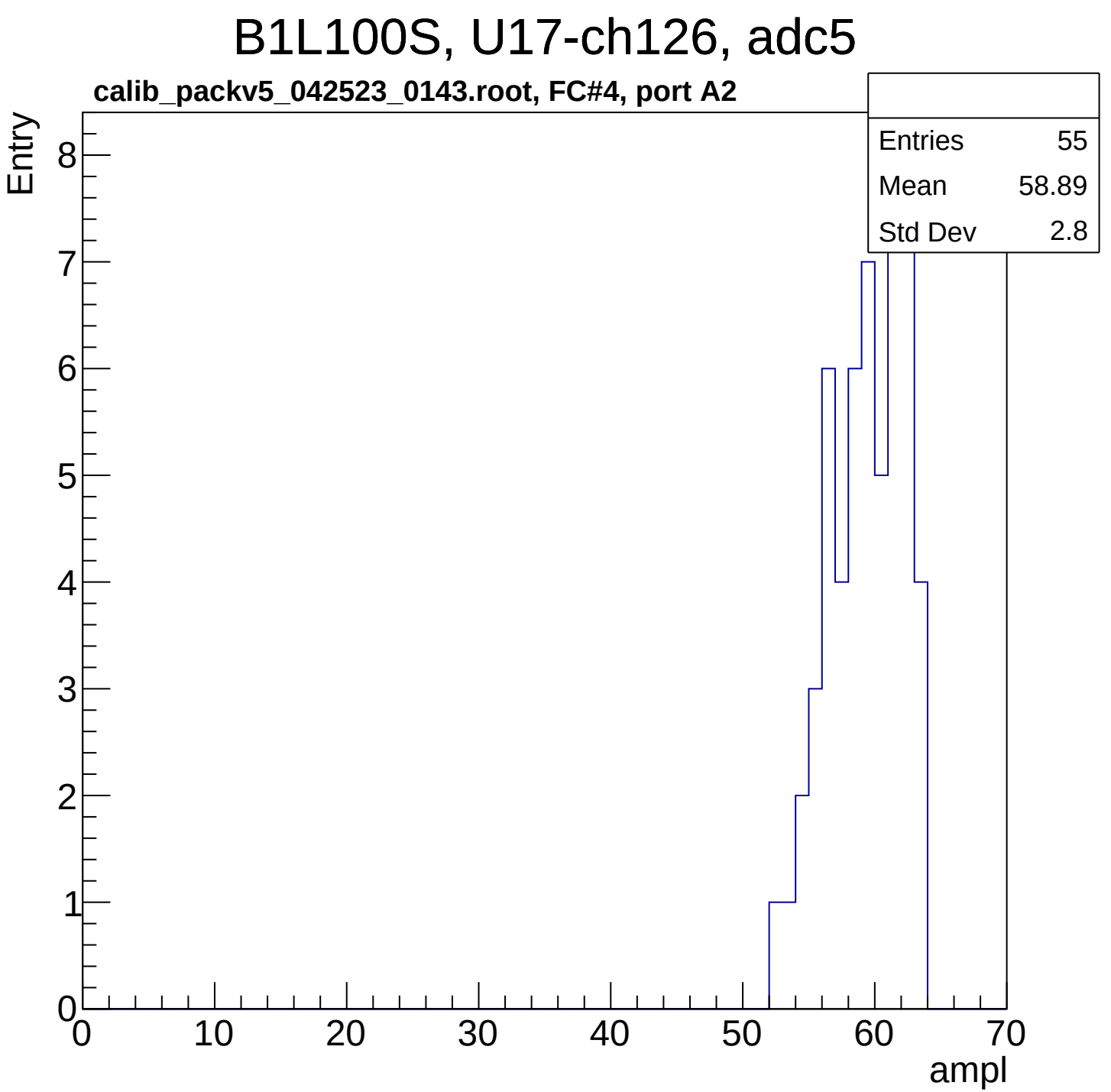
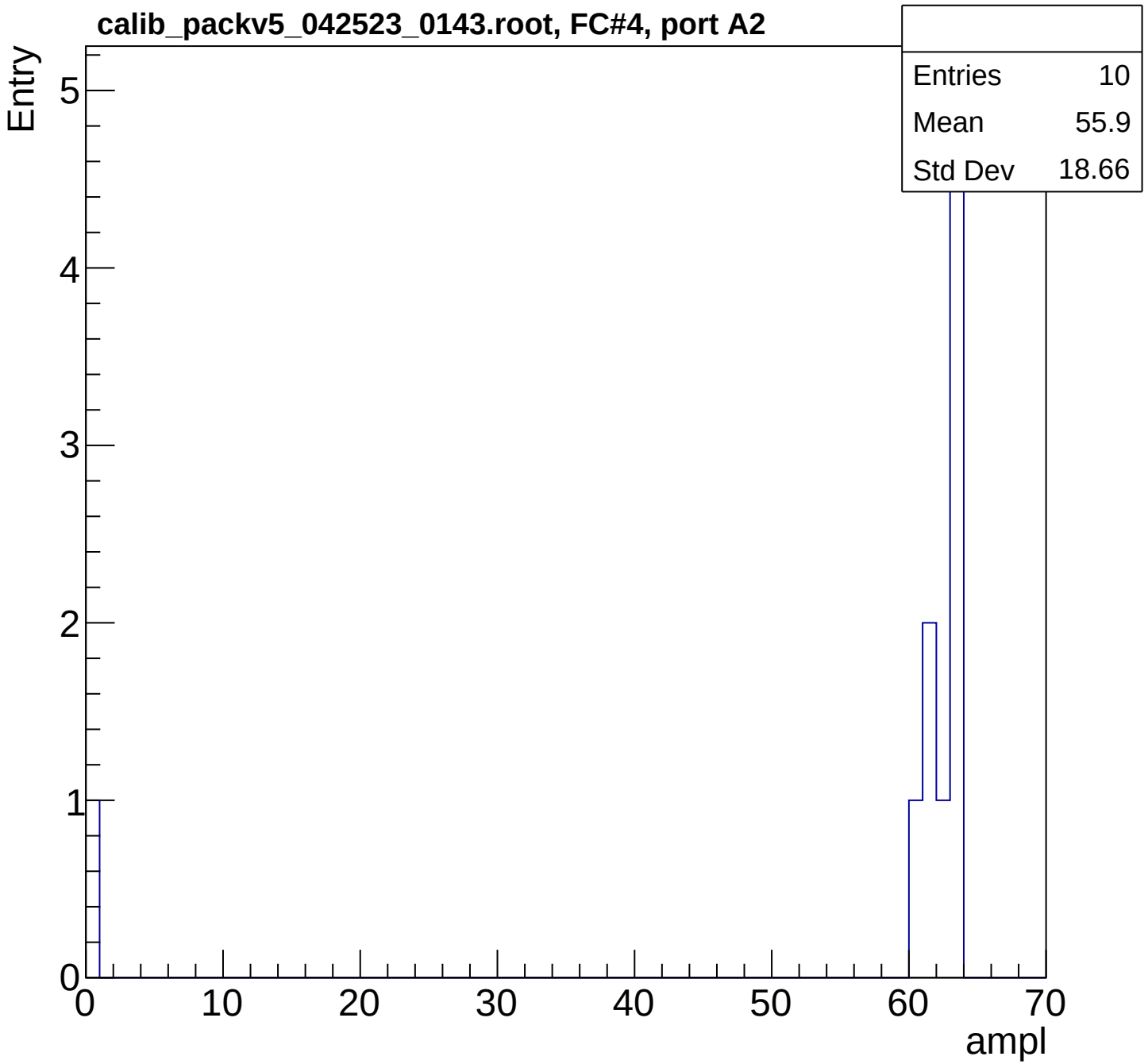
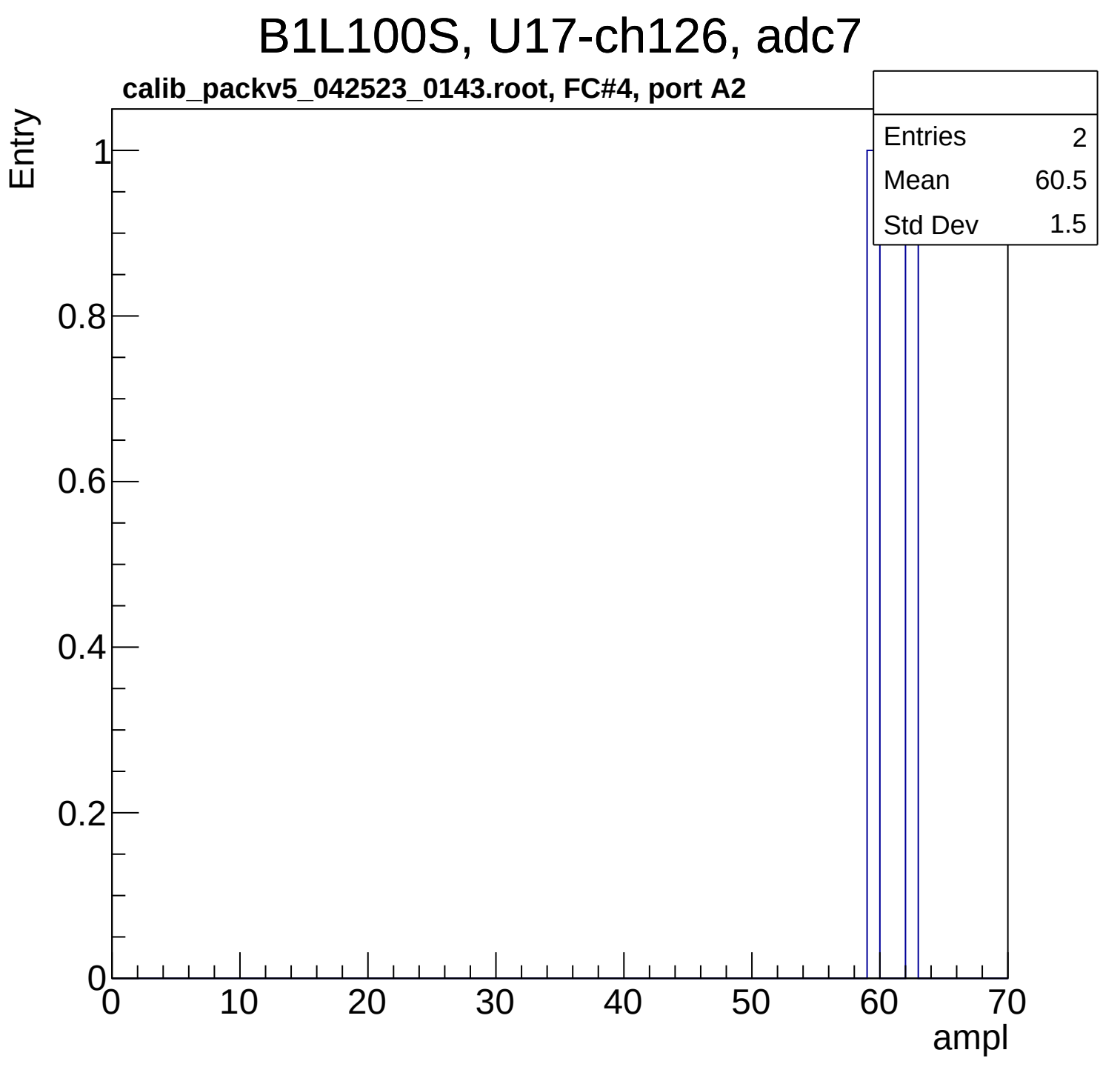

B1L100S, U17-ch126, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 58.89
Std Dev 2.8
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch126, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 10
Mean 55.9
Std Dev 18.66
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch126, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 60.5
Std Dev 1.5
Entry
ampl
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0.2
0.4
0.6
0.8
1
0
10
20
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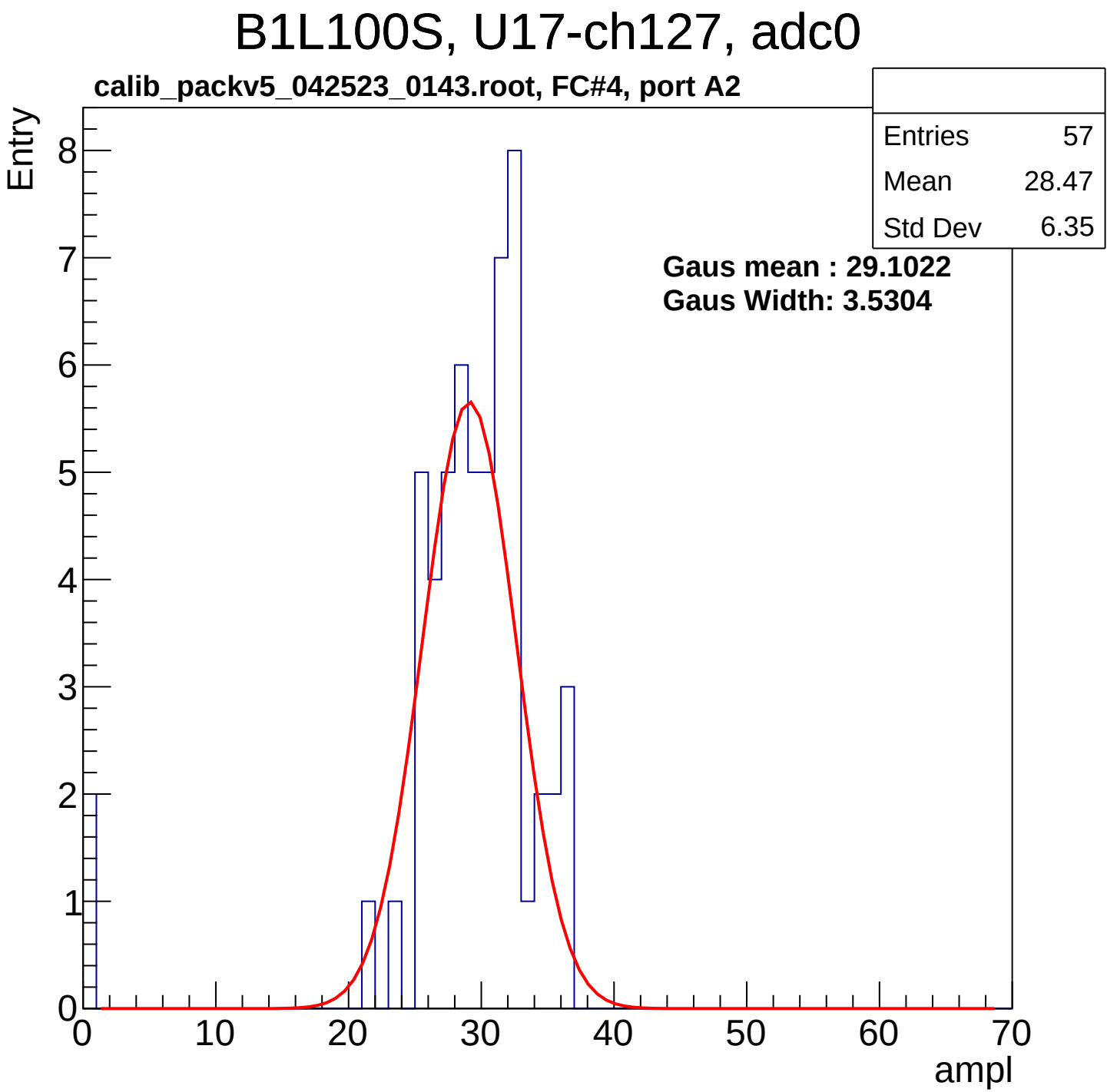
40
50
60
70


B1L100S, U17-ch127, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 28.47
Std Dev 6.35
Gaus mean : 29.1022
Gaus Width: 3.5304
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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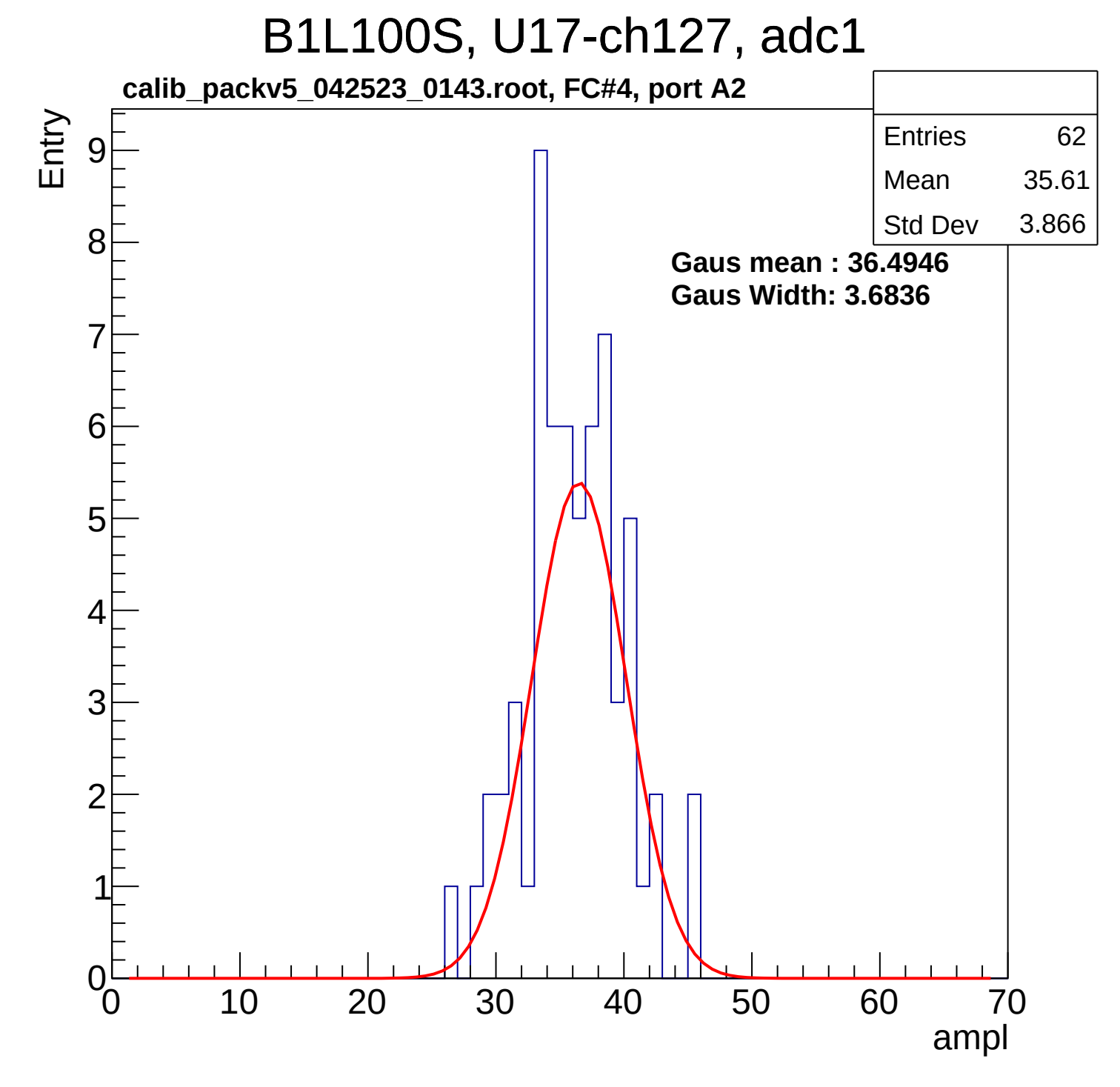
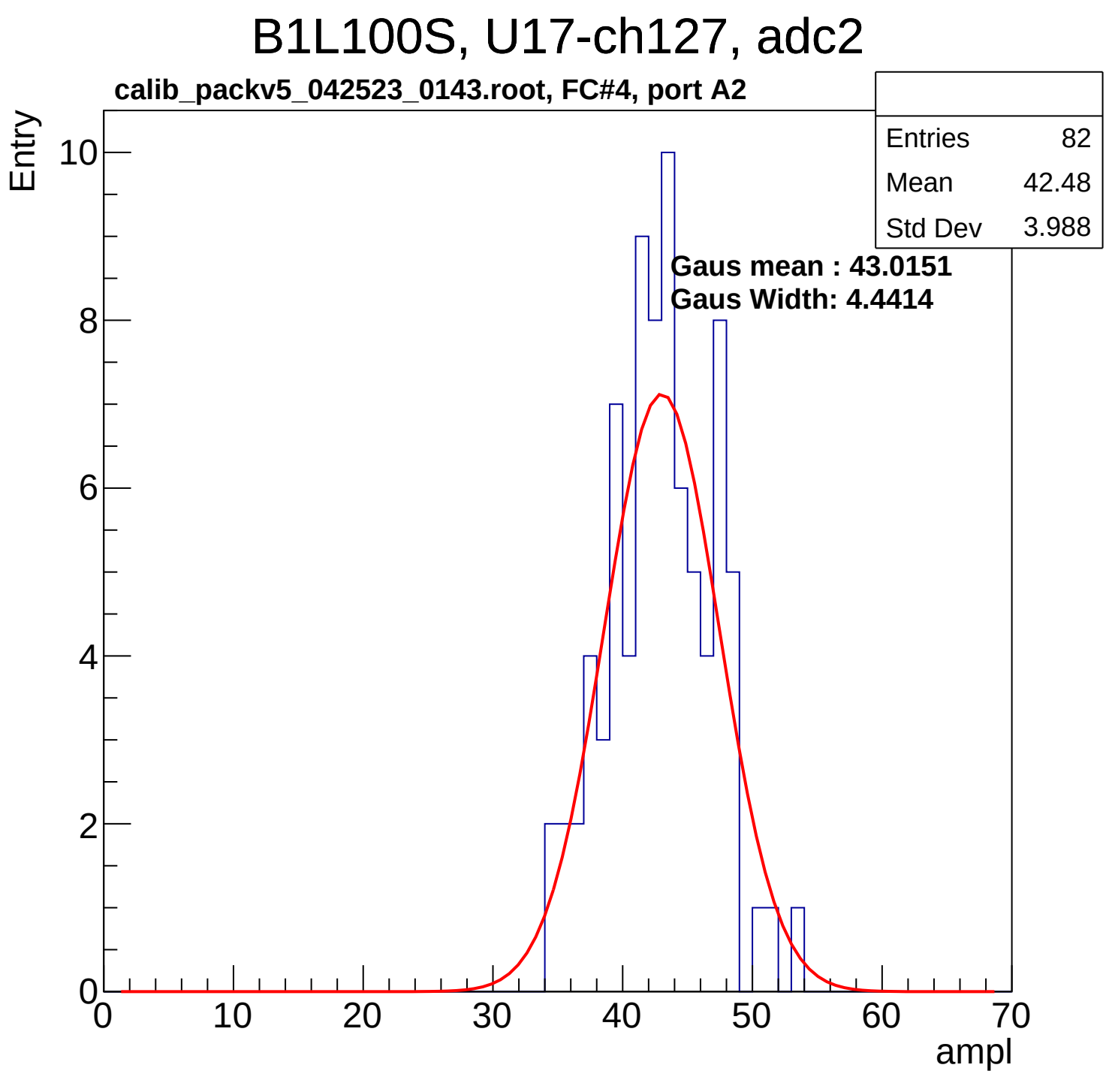
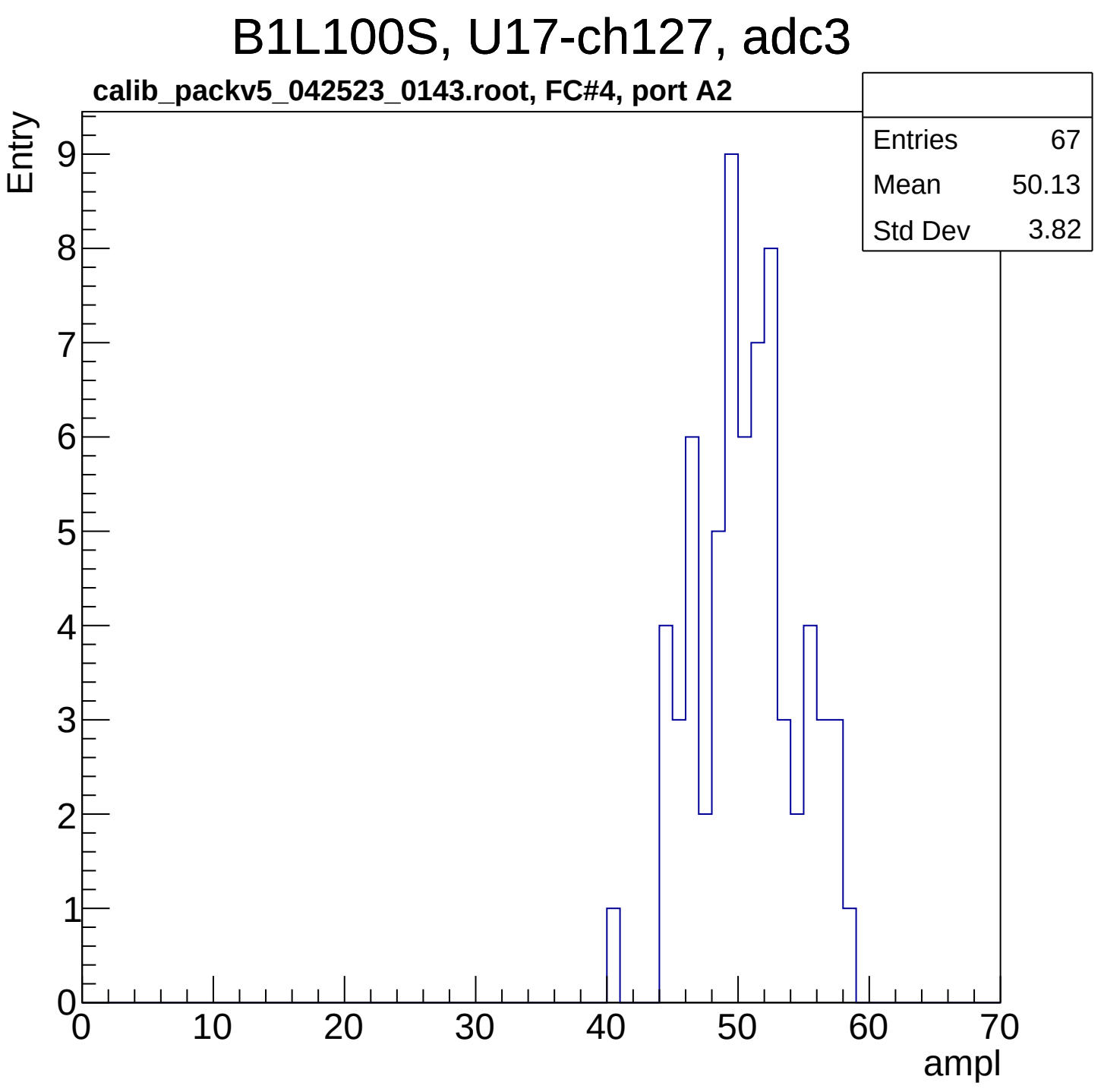
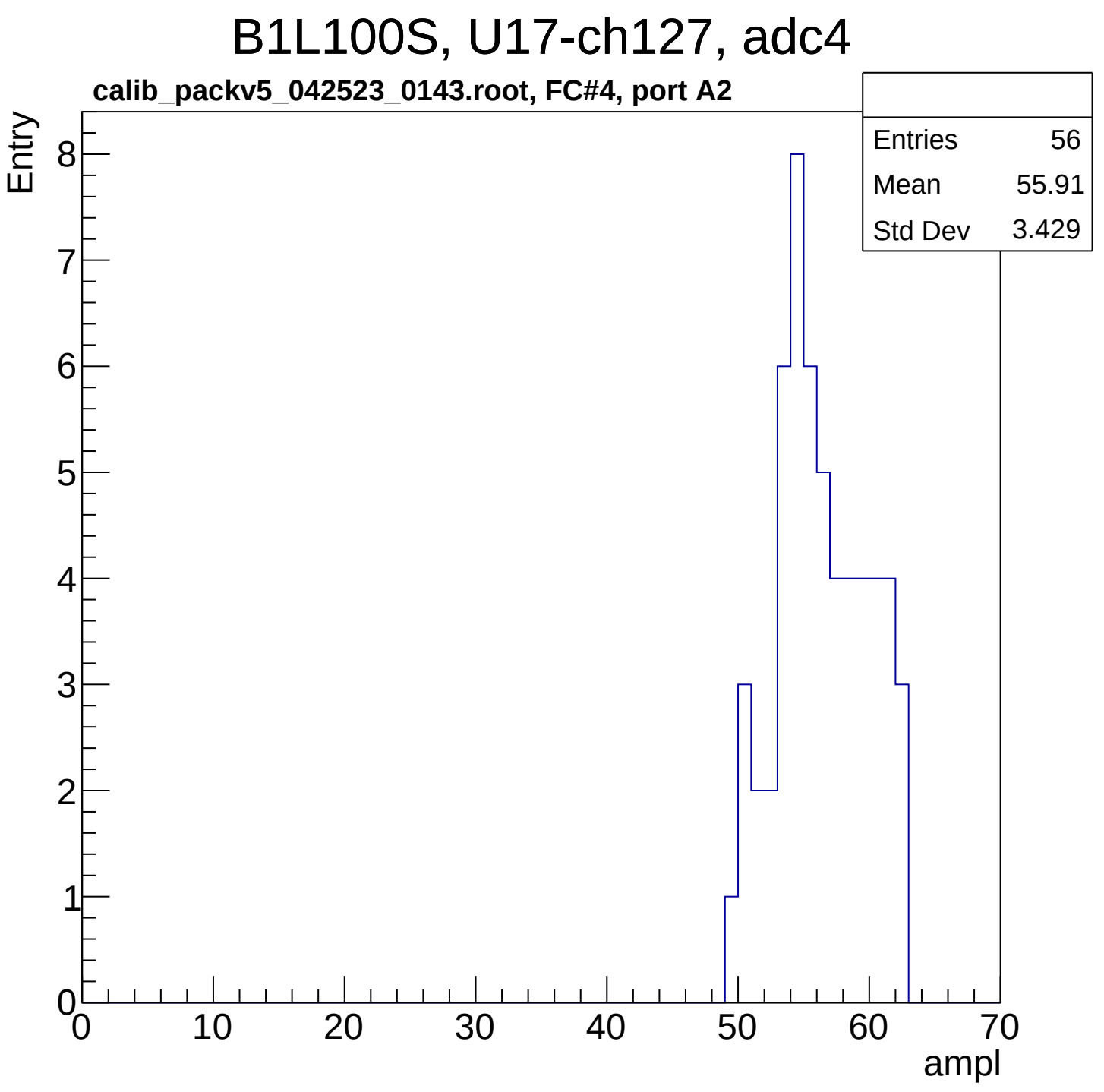
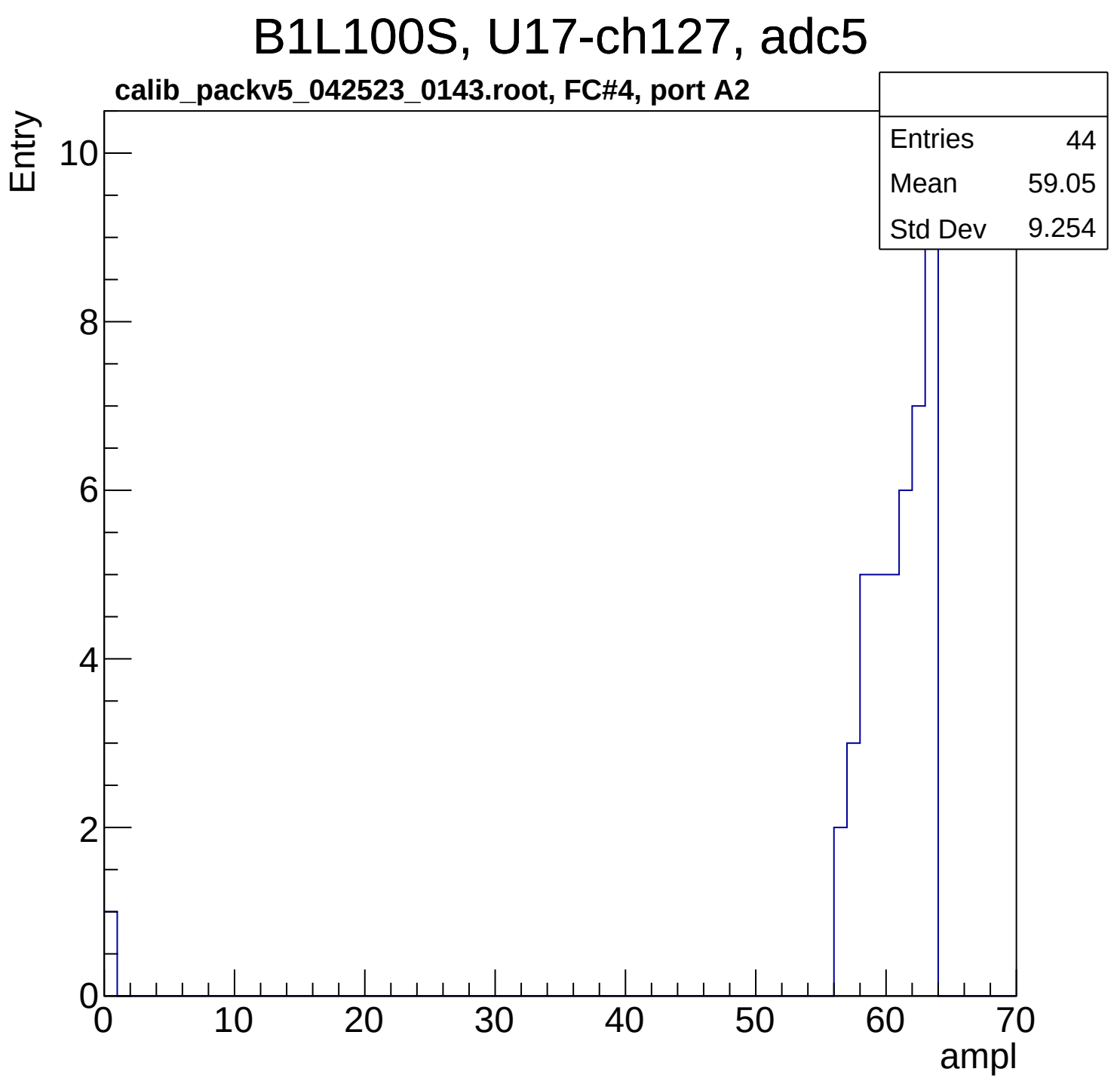
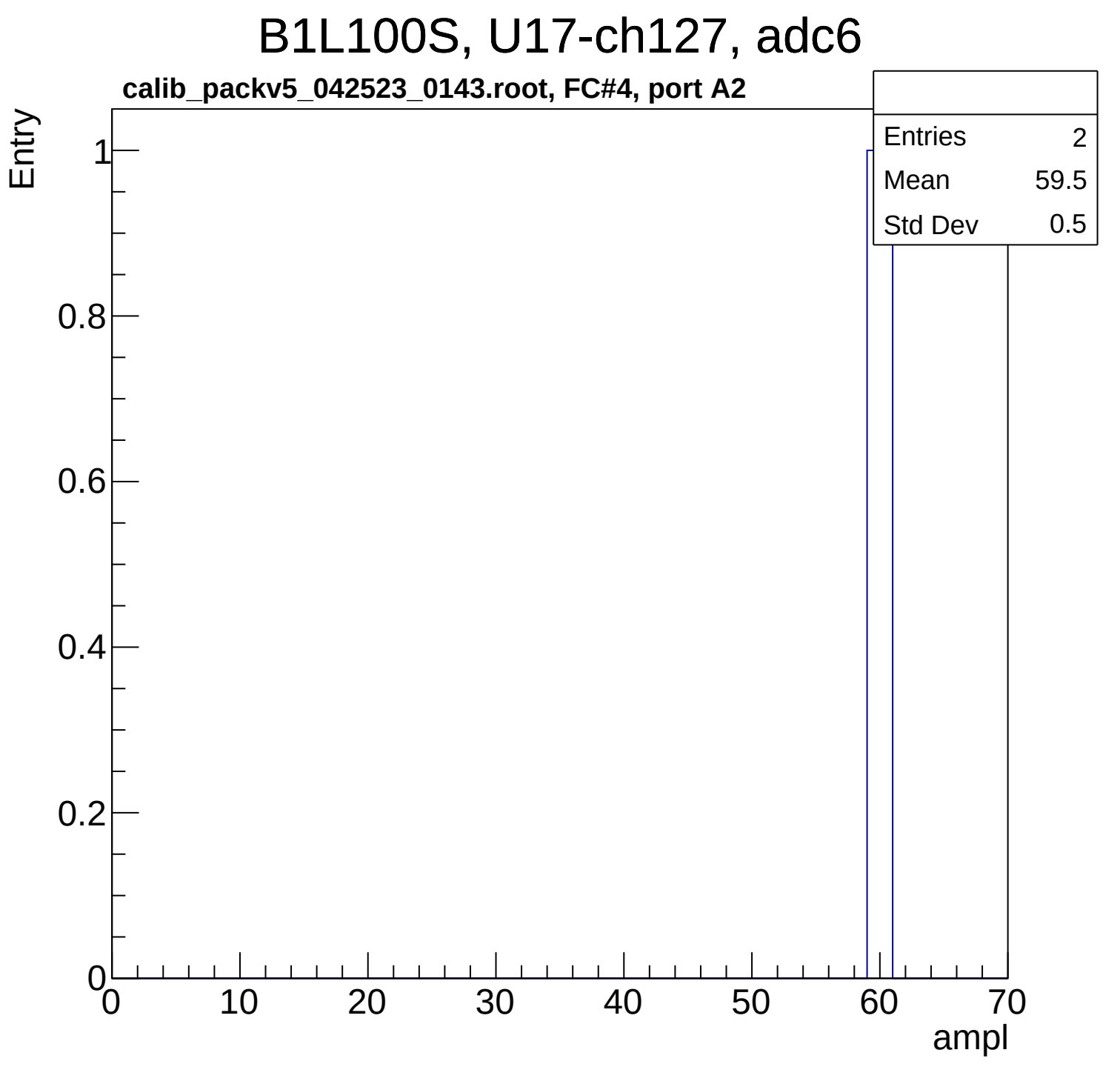

B1L100S, U17-ch127, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 35.61
Std Dev 3.866
Gaus mean : 36.4946
Gaus Width: 3.6836
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

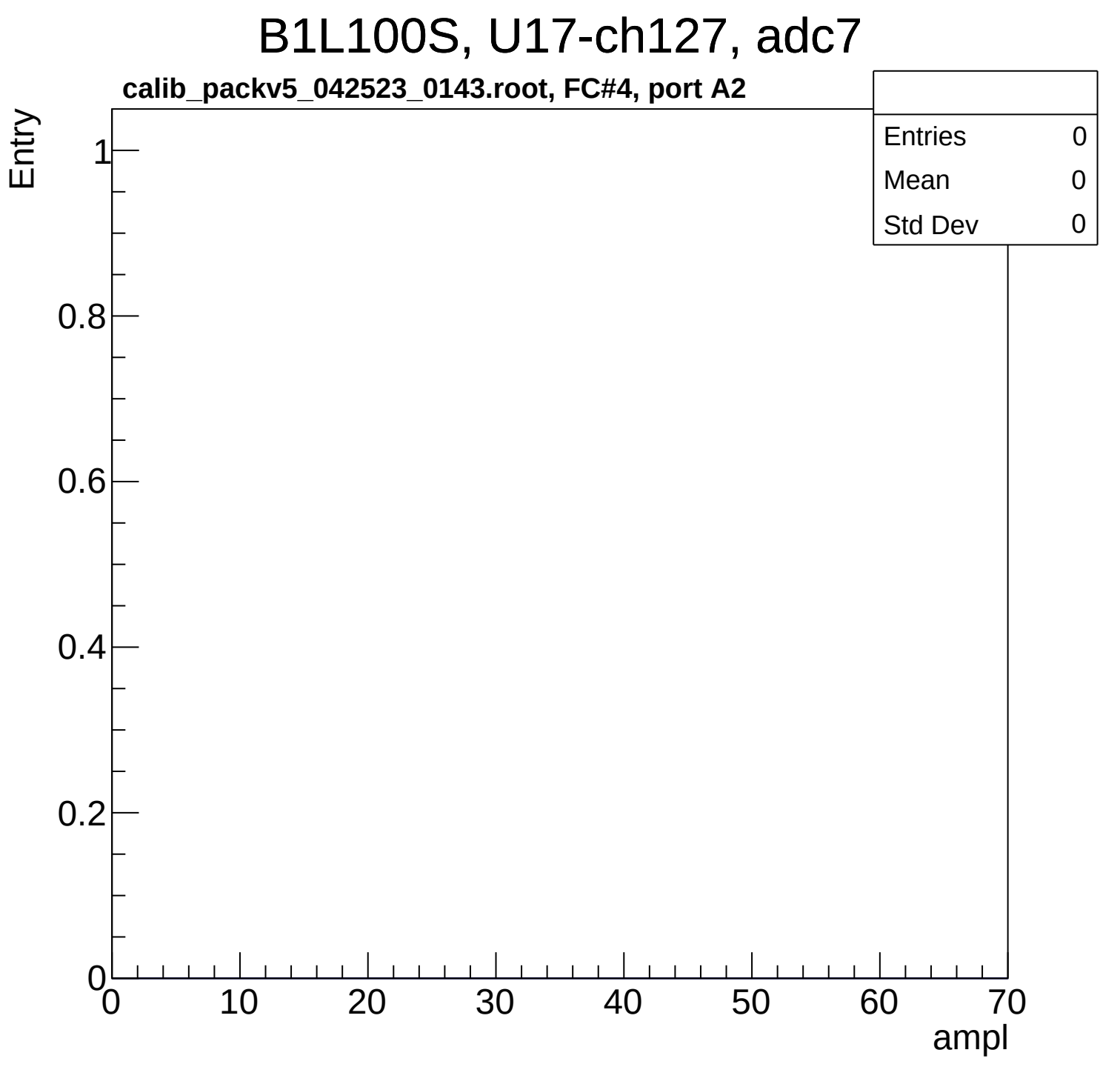

B1L100S, U17-ch127, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 82
Mean 42.48
Std Dev 3.988
Gaus mean : 43.0151
Gaus Width: 4.4414
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

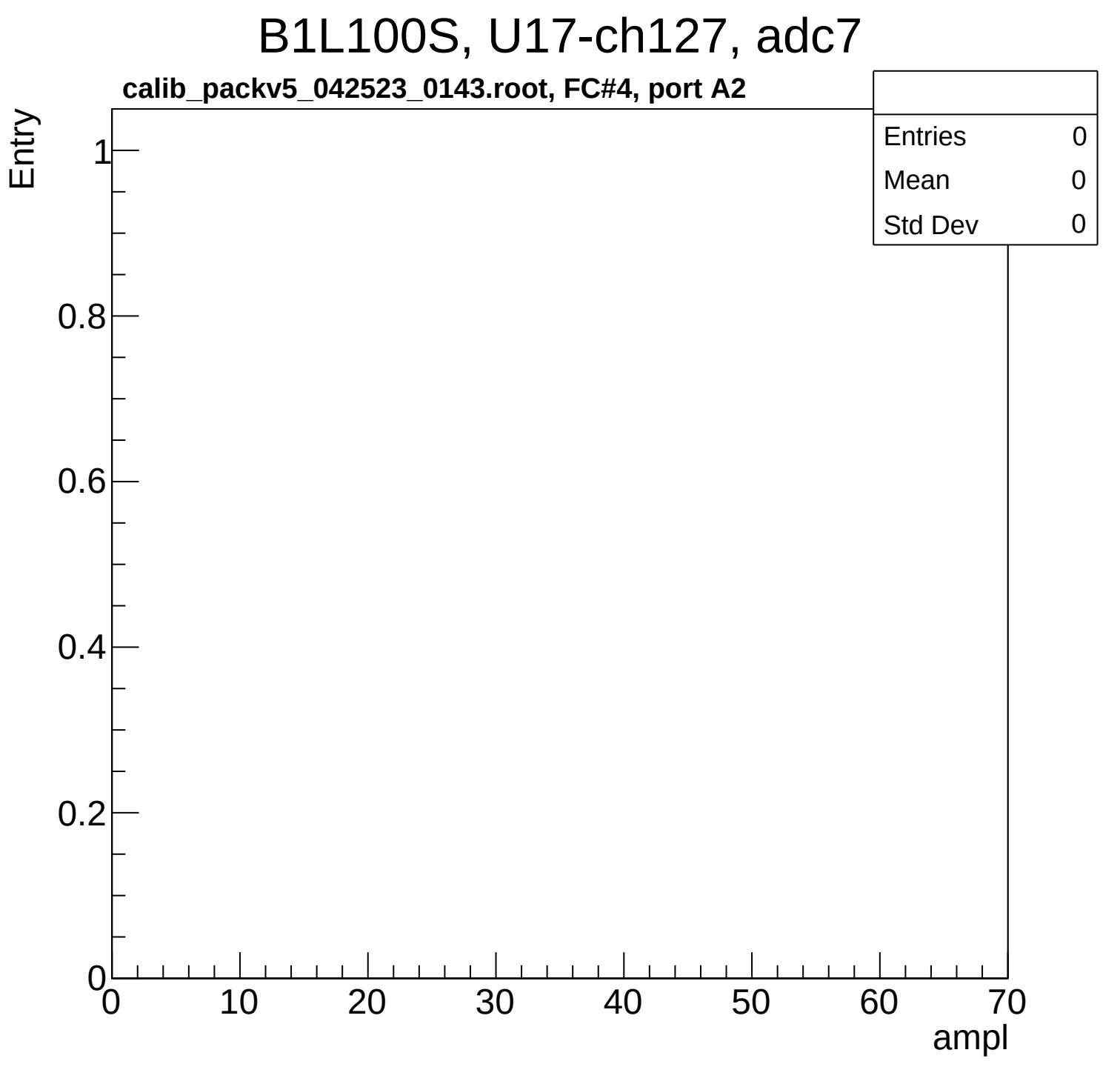

B1L100S, U17-ch127, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 50.13
Std Dev 3.82
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U17-ch127, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 55.91
Std Dev 3.429
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U17-ch127, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 44
Mean 59.05
Std Dev 9.254
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch127, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 59.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch127, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U17-ch127, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl